EXPERIMENTS ON A THREE-CORE CELL
FOR HIGH-SPEED MEMORIES

J. Raffel and S. Bradspies

Staff Members
Lincoln Laboratory
Massachusetts Institute of Technology
Lexington, Massachusetts

Magnetic Memories

The coincident-current magnetic-core memory was suggested in 1949 by Jay W. Forrester[1] as a reliable, random-access storage medium. Development of the first working memory of this type, for the Memory Test Computer at M.I.T., established conclusively the superiority of such a memory over competitive systems and paved the way for others to exploit the new device.

The coincident-current memory uses two properties of ferromagnetic materials[2], (Fig. 1) non-linearity and remanence, to perform the basic functions, selection and storage, required of a multiple-register memory. As shown in Fig. 2, each core in an array lies at the intersection of a unique set of x, y, and z coordinate wires. The remanent-flux state of a given core determines whether it holds a ONE or a ZERO. Simultaneous half-amplitude current excitations on one of each set of x and y lines cause a single core in each z or digit plane to receive full switching current while all other cores in the plane remain essentially unchanged. If the core holds a ONE, a large voltage is induced on a sense winding which links all the cores in a digit plane; a ZERO produces a small output. In order to write into the core, currents opposite in direction to the original excitations are supplied, and the core is switched back to the ONE state. If a ZERO is to be written into any digit plane, a half-amplitude pulse in the read direction is also applied during write time on the appropriate digit winding; thus, the core is prevented from switching to the ONE state.

Two important characteristics of this system are:

1. An entire row and column in each digit plane are "half-driven," producing small, spurious outputs on the sense winding which tend to mask the signal from the selected core.

2. Switching time of the core is fixed by the knee of the hysteresis loop of the material since this establishes the allowable current excitations on the coordinate lines.

These are the two outstanding limitations on the coincident-current memory. The first tends to limit the size of the array from which a signal can be easily detected and places fine restrictions on core uniformity. The second limits the speed of operation which depends on the switching time of the core. It has been found experimentally that the product of switching time and net field applied to the core is approximately a constant, S_W, (called the switching coefficient) for a given material[3]. The governing equation is:

$$S_W = (H - H_0) \, T$$

where T is switching time, H is applied field, and H_0 is an intercept value usually related to the knee of the loop. The restrictions on current range impose a corresponding restriction on memory cycle time, or the time between successive memory accesses.

These two limitations are the price paid for performing both selection and storage functions in a single core.

External Selection

A system has been developed[4] which essentially assigns the performance of these two functions to separate cores and thereby overcome the restrictions mentioned above. A similar system has been proposed independently by Dr. R. J. Slutz of the National Bureau of Standards[5].

Consider the problem of using switch cores in a magnetic-core memory to perform the selection function completely external to the memory cores themselves. Such a selection system must be capable of subjecting any memory core in a selected register to either of two cycles:

Read, Write ZERO $(R-W_0)$
or Read, Write ONE $(R-W_1)$

without exciting any other cores in the array. (A ZERO and a ONE are stored in the usual manner as shown on the hysteresis loop of Fig. 1.) For cycle $R-W_0$, it is only necessary to have a sequence which begins and ends with a current pulse of positive polarity. For the $R-W_1$ cycle, all that is required is that the first pulse be positive and the last negative. These two cycles are shown in Fig. 3. Note that a switch core must always be reset to its original flux state before the start of a new cycle, that is, its output will always be symmetrical and made up of two oppositely poled pulses. This is

ideal for the R-W_1 cycle since it can be performed by a single switch core.
The R-W_0 cycle cannot come from a single core, however, but can be
produced by the combination of two switch-core outputs (A and B,
Fig. 4). The two cycles thus obtained are shown in Fig. 4.

The A and B drives are shown overlapped for minimum time,
yielding a three-beat cycle. It is evident from above that the minimum
number of switch cores needed is one per register to supply output A
(each core in the register receives it) and one core per bit to supply
output B (each core may or may not receive this, depending on whether
a ONE or a ZERO is being written). A winding through all the B cores of
a given digit plane can be used to provide an inhibit current which
prevents output B when a ONE is to be written. Although only one A core
is theoretically required per register, the system described here uses
one per bit, thus making the cell a symmetrical three-core unit (Fig. 5)
for ease of construction and to eliminate the large size core needed to
drive an entire register.

The switch cores are all biased by a negative current. A two
dimensional system of excitations switches a single core while only
driving other switch cores in the plane along the saturated portion of
the hysteresis loop. The output currents from these partially-selected
switch cores are the only excitations passed on to non-selected memory
cores.

By a complete separation of switching and memory functions,
the cores are no longer restricted by the critical requirements on
driving currents and hysteresis-loop squareness imposed by coincident-
current operation. The hysteresis loop required for a coincident-cur-
rent memory is shown in Fig. 1. Ideally, the loops required for switch
and memory cores in the proposed system could be as shown in Fig. 6.
The main requirement of the switch core is that it be saturable; of
the memory core, that it have two distinct remanent-flux states. The
poorer the saturability of the switch core the greater the partial-
select excitations the memory core must withstand without changing flux
state.

Experimental Results

In order to determine the feasibility of this system and to
measure its operating characteristics, a series of experiments was per-
formed on individual three-core cells. These were aimed at seeing how
operation was affected by variations in the flux ratio between switch
and memory cores, coupling-loop impedance, input current, pulse timing,
and core material.

Experiments[6] indicate that for best operation the switch core
should have at least 6 times as much flux as the memory core, and the
coupling loop between the two cores should be resistive. Scope photo-
graphs for a cell incorporating these principles are shown in Fig. 7.

Figs. 7a and b show typical voltage outputs for the two switch cores when ONEs and ZEROs are being stored alternately. Fig. 7c shows the memory-core outputs for a ONE and a ZERO superposed. Ideally, the switch core should contain just sufficient flux to support the voltage drop in both the coupling loop and the memory core. Coupling-loop resistance must be large enough so that the inductive time constant of the switch-core secondary is short thus making it possible to squeeze the pulses close together. It cannot, of course, be made larger without limit, otherwise insufficient secondary current will be supplied to switch the memory core. Fig. 8 shows ONE and ZERO outputs superposed for each of three improper designs. In Fig. 8a, the switch core has insufficient flux and does not completely switch the memory core. In Fig. 8b, the coupling loop has no added resistance, and the current pulses decay slowly making it impossible to run the pulses close together. (The cell operates perfectly if pulses are spaced further apart giving an overall cycle time of 3 microseconds.) In Fig. 8c, too much resistance has been added to the loop, limiting secondary current so that the memory core does not switch fully. In all three cases it is almost impossible to distinguish between a ONE and ZERO.

In experimenting with various core materials, it was found that a wide range could be made to work satisfactorily. The best results were obtained, of course, for materials having the squarest loops. Here it was possible to obtain a ONE-to-ZERO ratio of about 15 to 1, ONE-to-half-select ratio of 250 to 1, and a complete cycle time of 0.4 microsecond. (Voltage ratios are for peak values.) As in coincident-current memories, a canceling sense winding minimizes the effects of partially selected outputs. For such a winding the difference between partial-select outputs for a core holding a ONE and for a core holding a ZERO becomes the significant factor. For the cell tested, this difference was too small to measure accurately.

Memory Criteria

The memory system described above is only one of a very large number which uses the magnetic core as its basic element. Any engineering design which attempts to translate this into a practical working device might well use the following criteria to measure and evaluate various systems:

1. Reliability, which is most easily estimated by tube count and margins;

2. Size (number of registers x number of places = number of bits);

3. Cycle time, the minimum time between successive readouts;

4. Cost, mainly determined by core specifications
    and quantity, wiring complexity, and tube count.

Design Considerations

The principal disadvantages of the three-core-cell memory
lie in the increased complexity of construction and the large number
of cores which are used. The construction difficulties arise primarily
from the small coupling loops linking each memory core to its two
switch cores. Such problems tend to increase core interspacing. As
a result, it is felt that this type of system will be most useful in
memories of relatively small size, up to a few thousand registers.
Since the problem of half-select noise in coincident-current memories
is not too significant in these small sizes, one of the principal
advantages of the three-core system is wasted. It would seem that
the greatest advance could be made by concentrating on speedier cycle
times as the main goal for the system since - ideally - there is no
upper limit to the excitations which can be applied to the cores.
The principal problem is that the high currents needed here mean
more tubes; also, faster switching times mean larger back voltages
from cores (possibly counterbalanced by a reduction in flux through a
change in core size and/or material).

The power generated in the core goes up as the square of the
speed. This is because the energy required per cycle to switch a core
is roughly proportioned to the inverse switching time, and the number
of cycles possible per second increases at about the same rate. The
heat generated in the core because of this power loss can have a
serious effect on the pulse response of ferrite materials. Fortunately,
there is a wide range of core characteristics over which this system
should work well so that system operation ought not to be too sensi-
tive to heating at these high speeds.

Probably the most important single criterion for choosing
cores for this system is a low value of the switching coefficient S_W,
which implies relatively low driving currents for a given speed of
operation and low power loss with consequently reduced heating.

Preliminary Design of Plane

Successful experimentation with three-core cells has led to
a preliminary design for a single 16 x 16 plane (Fig. 9). This plane
will use novel construction methods to overcome the wiring complexities
inherent in the system. The switch cores (both A and B) are all on one
side of a single board. The memory core is on the other side suspended
between two lugs on a piece of bus. The resistance wire, which forms
the small coupling loops when connected to the lugs, is wound on in
continuous lengths rather than being handled in small separate pieces.
The grid of driving lines is wired on the switch cores in much the same
way as in a conventional coincident-current memory.

The switch cores to be used in this plane will be 80 mils O.D., 50 mils I.D., 30 mils height, or about one-and-one-half times the size of the memory core used in the Memory Test Computer. The memory core will be about one-sixth the size of the switch core. At present, there is no simple way to fabricate such a small core. For this experimental plane, the simple expedient of boiling down larger cores in acid will be used. The plane will be designed to operate with a complete cycle time of less than 1 microsecond. It is felt that this is fast enough to be a worthwhile goal without entailing too many complications in the associated electronics. The core material will be an experimental mixture provided by the General Ceramics Company. The memory core signals should be of the order of 0.2 or 0.3 volt. It is hoped that the driving currents required will be no higher than about 2 amperes.

The long-range practicality of this type of memory system depends largely on the ability of alternative devices to do the same job. At the present time, the coincident-current memory seems to be the only other system which offers the possibility of operating within the range of 1-microsecond cycle time. This would require the use of a high-coercive-force material which still maintains the requisite hysteresis-loop squareness at high pulse rates. The development of such materials is, in any case, a worthwhile goal along with the long-range problem of reducing S_W (and, therefore, power requirements) for memory materials in general.

JR/dg

Drawings: A-61950
             A-58815
             A-61951
             A-61952
             A-61953
             A-61954
             A-61997
             A-61998
             A-61955

REFERENCE BIBLIOGRAPHY

1. Forrester, Jay W., Digital Information Storage in Three Dimensions Using Magnetic Cores, Report R-187 (May 16, 1950), M.I.T. Servomechanisms Laboratory.

2. Papian, William N., A Coincident-Current Magnetic Memory Unit, Report R-192 (August 31, 1950), M.I.T. Servomechanisms Laboratory.

3. Menyuk, N., Energy Dissipation in Square-Loop Ferromagnetic Materials with Specific Application to Switch Cores, Report M-2160 (May 12, 1953), Division 6, Lincoln Laboratory.

4. Raffel, J. I., Switch for Register Selection in a Magnetic-Core Memory, Report R-234, Pages 75-78, (May 24, 1954), Division 6, Lincoln Laboratory.

5. Slutz, R. J., Tri-Core Magnetic Memory, National Bureau of Standards Quarterly Progress Report of the Program on Computer Components and Techniques, (July 1 through September 30, 1953).

6. Bradspies, S., A Magnetic-Core Memory with External Selection, S.M. Thesis (January 1955), Electrical Engineering Department, M.I.T.
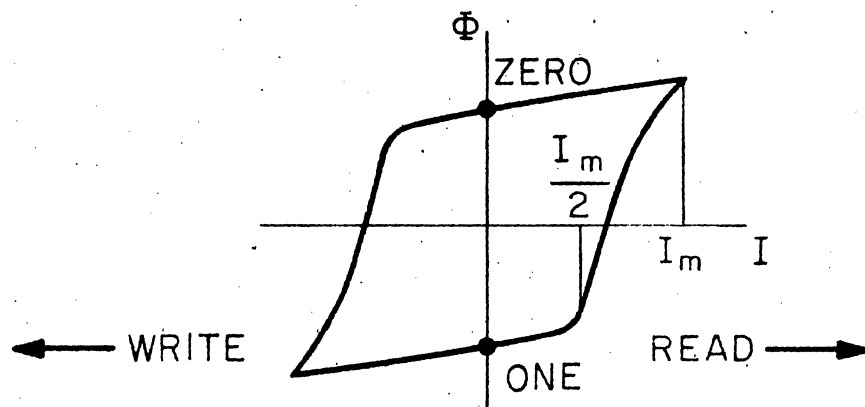
FIG 1
TYPICAL MEMORY CORE HYSTERESIS LOOP

$\frac{I_m}{2}$

z_2

$\frac{I_m}{2}$

Z_1

$\frac{I_m}{2}$

Z_0

y_1 $\frac{I_m}{2}$

X_2 $\frac{I_m}{2}$
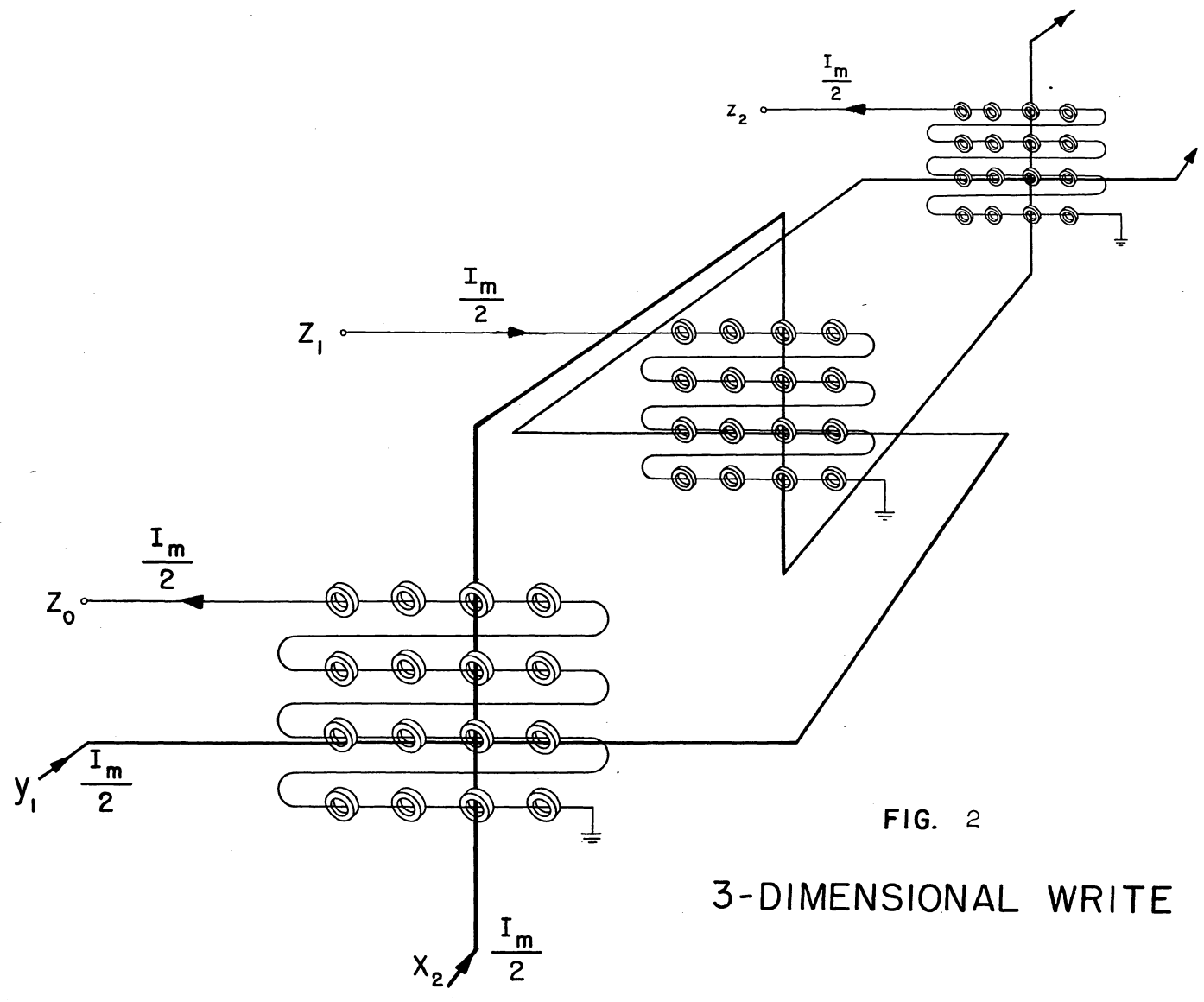
FIG. 2

3-DIMENSIONAL WRITE
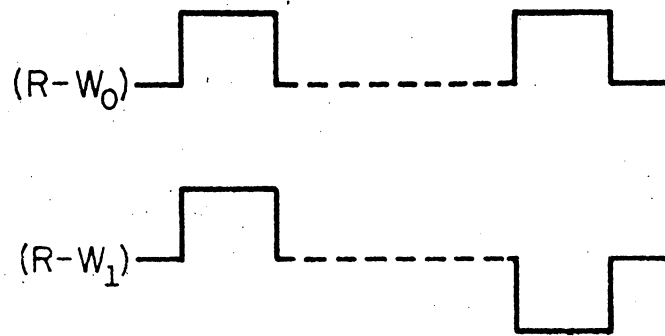
FIG. 3

PULSE SEQUENCES REQUIRED FOR
DRIVING MEMORY

$(R-W_0)$

OUTPUT A   OUTPUT B

$(R-W_1)$

OUTPUT A   OUTPUT B
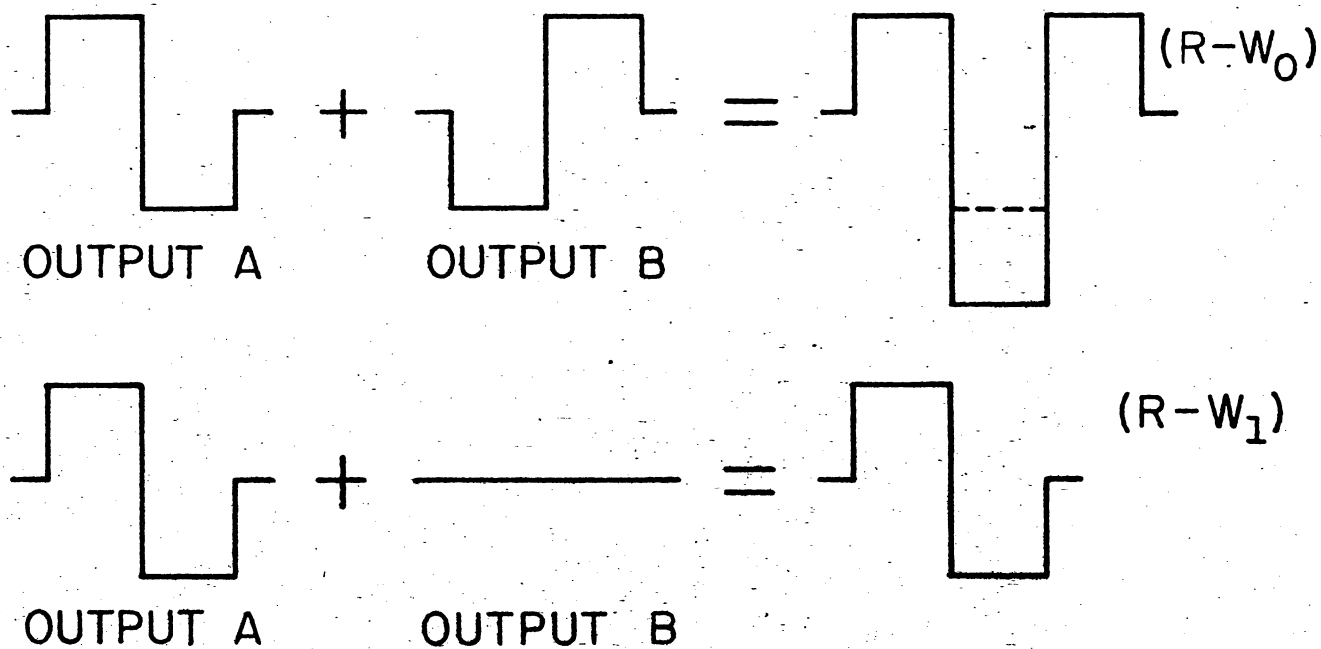
FIG. 4

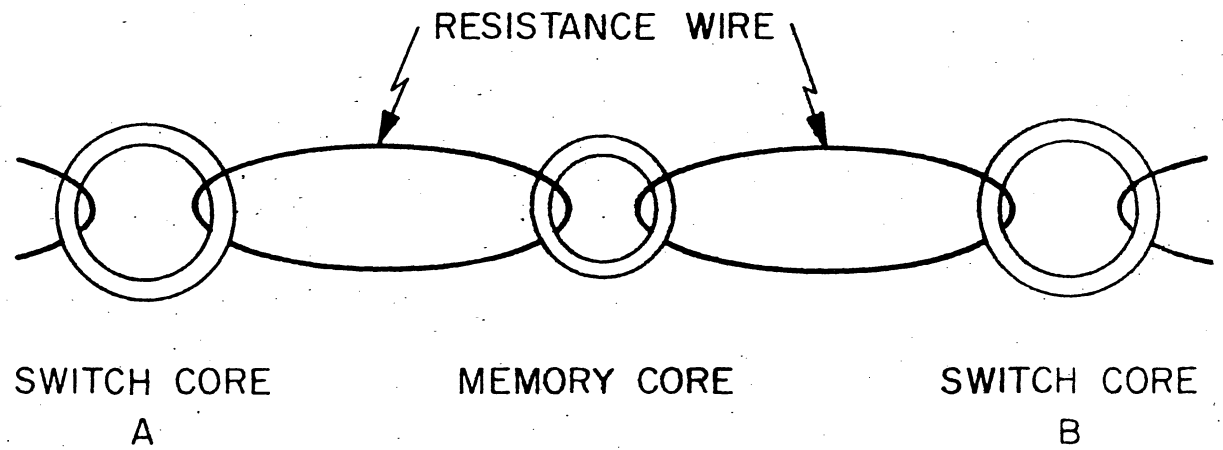COMBINED OUTPUTS TO PRODUCE $R-W_0$ AND $R-W_1$ CYCLES

RESISTANCE WIRE

SWITCH CORE
A

MEMORY CORE

SWITCH CORE
B

FIG. 5
THREE CORE CELL
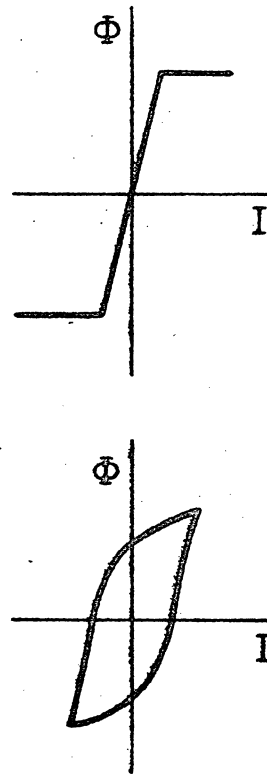
FIG. 6

THEORETICALLY USABLE SWITCH AND MEMORY CORE LOOPS
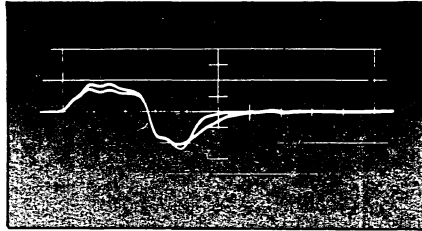
SUPERPOSED VOLTAGES ACROSS SWITCH CORE A
FOR READING ONES AND ZEROS
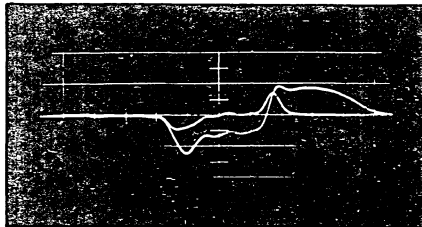
SUPERPOSED VOLTAGES ACROSS SWITCH CORE B
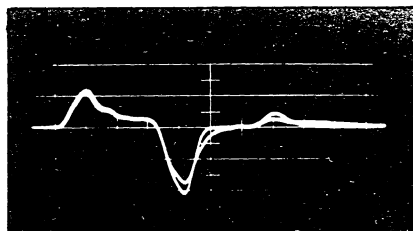FOR WRITING ONES AND ZEROS
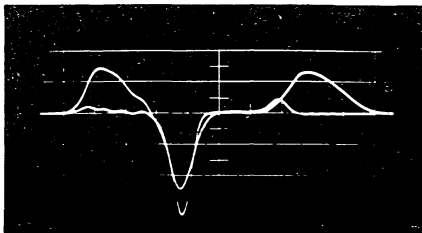
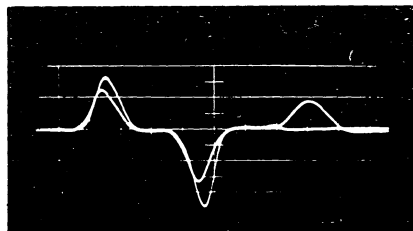SUPERPOSED MEMORY CORE OUTPUT FOR
ONE AND ZERO

FIG. 7

TYPICAL CELL VOLTAGES
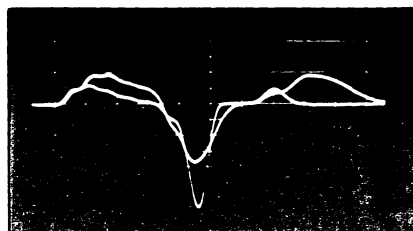
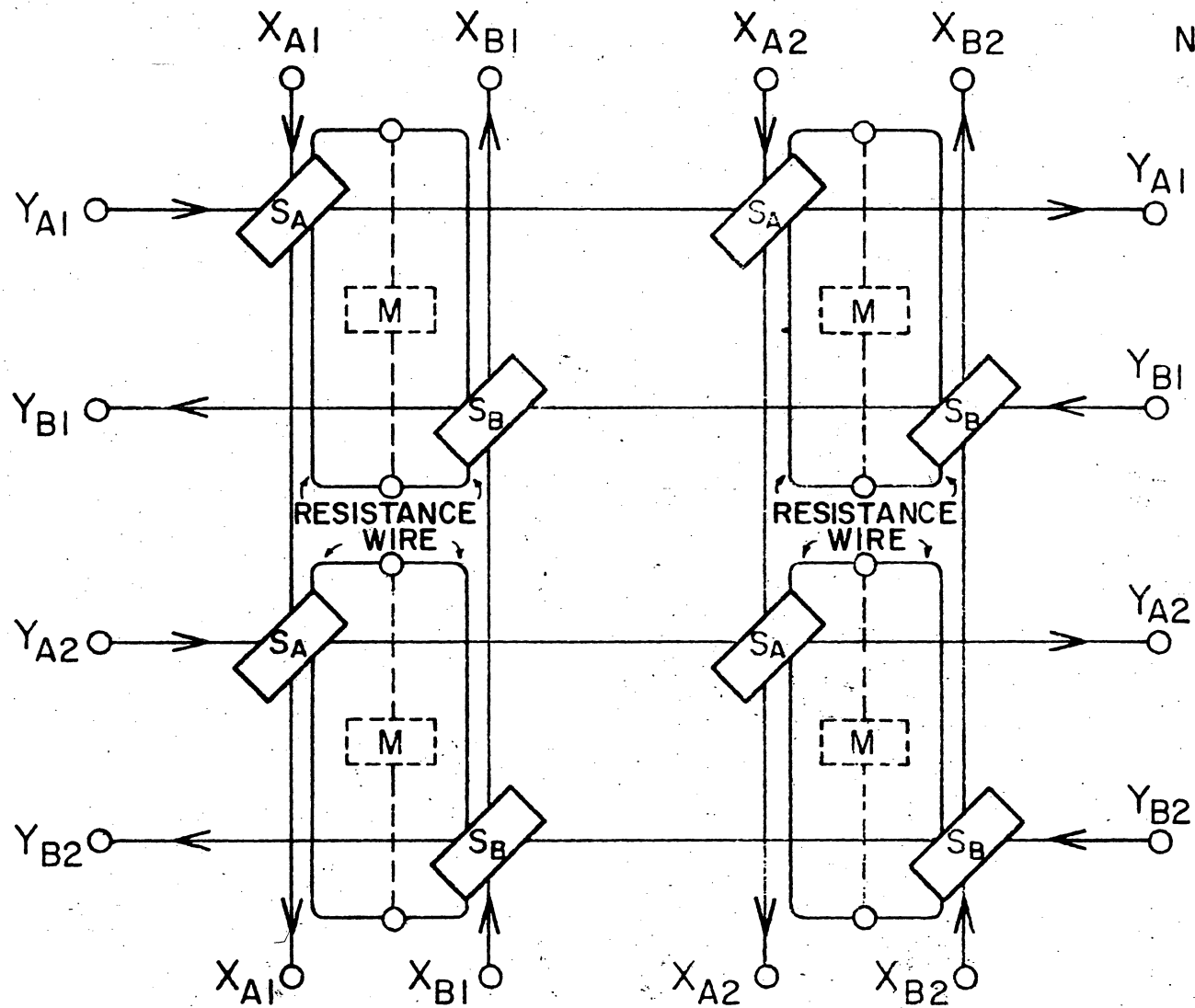CASE OF TOO LITTLE FLUX IN SWITCH CORE

TOO MUCH RESISTANCE IN COUPLING LOOP

TOO LITTLE RESISTANCE IN COUPLING LOOP

FIG. 8

MEMORY CORE OUTPUT, ZEROS AND ONES

FOR THREE CASES OF IMPROPER DESIGN

NOTE:

SWITCH CORES ARE ON ONE SIDE OF PHENOLIC BOARD, MEMORY CORES ON THE OTHER. NOT SHOWN ARE BIAS WINDINGS LINKING EACH SET OF SWITCH CORES AND SENSE WINDING LINKING MEMORY CORES.

FIG. 9

2 X 2 MEMORY PLANE USING THREE CORES PER CELL