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SUBJECT: DISPLAY LINE DRIVER (INDIVIDUAL STAGE ANALYSIS)

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Abstract: The original M-note described the operation of the display line driver in general terms. The purpose of this supplement is to thoroughly analyse the individual stages, presenting sufficient data for the evaluation of the circuit and also for troubleshooting in case of eventual failure. Operating margins, frequency response, power supply requirements and maintenance data for the individual stages are presented.

The results of the margins indicate that the circuit will operate satisfactorily when any tube falls below 60% of bogie, and, in the majority of cases, considerably below 60%.

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1.0 GENERAL DESCRIPTION

The display line driver is an amplifier which receives a voltage signal from one of the display decoders, amplifies this signal to 3.7 times its value and feeds the output to 74, 126, or 252 parallel display tube input circuits through approximately 1700 feet of coaxial cable (K109A). The line driver contains a gain control to insure that each one can be set to exactly the same gain. The circuit exists in three pluggable units which are one preamplifier P.U. 3006481 and two output P.U.'s 3006482. See 6M-3284, paragraphs 1.1 and 1.2 for a description of the line driver as a differential amplifier and as a mean level regulator. The schematic for this circuit is shown in drawing E75792.

2.0 OUTPUT LOAD SPECIFICATIONS

This paragraph supercedes paragraph 2.0 of 6M-3284. Figure 2.0.1 (SA 65536) is a diagram of the actual input circuit to each pair of deflection plates in a console. This circuit provides a slight control of the gain and position of the signal to accomodate manufacturing tolerances in display tubes. The values of some of the components in the console input are different depending upon the particular plates being driven. Table 2.0.1, referring to Figure 2.0.1 (SA 65536) shows these differences.

Table 2.0.1 ACTUAL CONSOLE INPUT CIRCUIT COMPONENTS (Fig. 2.0.1)

S.D.		R_1	C_1	R_2
	H. Char. Sel.	47K 1W 1%	1000 pf	620K 1W 1%
	V. Char. Sel.	47K 1W 1%	680 pf	360K 1W 1%
	H. Char. Comp.	47K 1W 1%	1000 pf	560K 1W 1%
	V. Char. Comp.	47K 1W 1%	1000 pf	560K 1W 1%
D.D.				
Fed in Parallel By One Line Driver	H. Char. Sel.	47K 2W 1%	270 pf	300K 2W 1%
	H. Char. Comp.	47K 2W 1%	270 pf	300K 2W 1%
Fed in Parallel By One Line Driver	V. Char. Sel.	47K 2W 1%	270 pf	300K 2W 1%
	V. Char. Comp.	47K 2W 1%	270 pf	300K 2W 1%
	H. Char. Defl.	5.1K 2W 1%	1000 pf	100K 2W 1%
	V. Char. Defl.	5.1K 2W 1%	1000 pf	100K 2W 1%

Table 2.0.1 Con't				
D.D. Auxiliary Console		R_1	C_1	R_2
Fed in Parallel By One Line Driver	H. Char. Sel.	47K 1W 1%	390 pf	300K 1W 1%
	H. Char. Comp.	47K 1W 1%	390 pf	300K 1W 1%
Fed in Parallel By One Line Driver	V. Char. Sel.	47K 1W 1%	390 pf	300K 1W 1%
	V. Char. Comp.	47K 1W 1%	390 pf	300K 1W 1%
	H. Char. Defl.	5.1K 1W 1%	1500 pf	100K 1W 1%
	V. Char. Defl.	5.1K 1W 1%	1500 pf	100K 1W 1%

The equivalent console input circuit is shown in Figure 2.0.2 (SA 65537) and the various values depending upon the pair of plates being driven, are indicated in Table 2.0.2.

Table 2.0.2 EQUIVALENT CONSOLE INPUT CIRCUIT (Fig. 2.0.2)					
		R_2	C_2	R_1	C_1
S.D. Console S.D.	V. Sel.	506K	190 pf	232 K	51 pf
	H. Sel.	760	192	224	55
	V. Comp.	206	215	225	51
	H. Comp.	704	199	227	45
S.D. Console D.D.	V. Sel. & Comp.	174	255	107	79
	H. Sel. & Comp.	174	250	107	75
	V. Defl.	106	216	216	69
	H. Defl.	106	212	216	75
D.D. Aux. Console	V. Sel. & Comp.	210	235	111	103
	H. Sel. & Comp.	210	245	111	105
	V. Defl.	120	212	210	106
	H. Defl.	156	247	217	84

The total equivalent load presented to each line driver including the cables and all consoles takes the same configuration as shown in Figure 2.0.2 (SA 65537). The values of each arm in this case are given in Table 2.0.3.

Table 2.0.3		TOTAL EQUIVALENT LOAD TO EACH AMPLIFIER				MAX. VOLTS REQUIRED PUSH PULL
		R_2	C_2	R_1	C_1	
S.D.	V. Sel.	6.84 K	.044 μf	3.14 K	.0038 μf	221 V.
	H. Sel.	10.25	.044	3.02	.0041	118
	V. Comp.	9.55	.046	3.04	.0038	134
	H. Comp.	9.5	.045	3.07	.0033	134
D.D.	V. Sel. & Comp.	1.33	.073	.893	.011	276
	H. Sel. & Comp.	1.33	.073	.893	.011	276
	V. Defl.	.91	.070	1.75	.010	375
	H. Defl.	1.0	.071	1.78	.010	375

2.1 OUTPUT VOLTAGE REQUIREMENTS

For optimum performance of the display tubes, the mean level of the output signal should be held at +45 volts at all times. A special regulator circuit is incorporated to stabilize this mean level. The maximum push-pull voltage required out of any line driver depends upon the particular lines it is feeding. These values are tabulated in the last column of Table 2.0.3. (Example: For a maximum of 375 V. push-pull required, each output terminal of the amplifier must swing from +139 volts to -49 volts.) The rise time should be sufficient to permit the output voltage to arrive to 99.9% of its final value within 20 microseconds.

2.2 INPUT SIGNAL SPECIFICATIONS

The maximum output of a decoder is approximately 240 volts push-pull with a mean level of +150 volts. This output can be controlled by varying the termination on the decoder. For maximum output, the output impedance of the decoder is 11.2 kilohms from each output terminal to +150 volts. As the output voltage is decreased the output impedance is also decreased approaching zero output impedance for zero output volts. For the exact relationship between decoder output voltage and decoder output impedance see 6M-3971.

3.0 INDIVIDUAL STAGE ANALYSIS

3.1 Output Stage

Figure 3.1.1 (SA 61516) shows the circuit schematic of the output stage. The circuit exists in two identical pluggable units 3006482. Drawings 3007699 and 3007701 show the required card assembly and detail to make up this circuit.

Seven tubes in parallel make up each side of this push-pull power amplifier stage. Provision is built-in for this stage to be used with less tubes per side if an application arises where less output power is required. All data presented here refers to seven tubes per side. The circuit is designed to drive the large capacitive, small resistive load of any of the analogue lines (mentioned in Table 2.0.3) feeding the electrostatic deflecting plates of the Charactron and Typotron.

Each of the S.D. lines (to the Charactron) present practically identical loads to the line drivers and similarly each of the D.D. lines (to the Typotron) load the line drivers practically identically. The complex frequency response of this output stage is expressed by four different equations depending upon the lines being fed (S.D. or D.D.) and the mode of operation of the line driver (differential mode, or common mode).

The complex response for S.D. considering the amplifier operating in the differential mode, is (referring to MIT Comp. Book, #880 Pg. 42)

(eq. 3.1.1)

$$\frac{e_o}{e_{IN}} = K_1 G_1 = 20\,db\ \frac{(-1)\left(1 - j\frac{f}{5.07\times10^9}\right)}{\left(1 + j\frac{f}{14.8\times10^3}\right)\left(1 + j\frac{f}{391\times10^6}\right)}$$

The common mode response for S.D. is:

(eq. 3.1.2)

$$\frac{e_o}{e_{IN}} = K_2 G_2 = 21.3\,db\ \frac{(-1)\left(1 - j\frac{f}{5.07\times10^9}\right)}{\left(1 + j\frac{f}{14.9\times10^3}\right)\left(1 + j\frac{f}{392\times10^6}\right)}$$

For D.D. the differential mode response is:

(eq. 3.1.3)

$$\frac{e_o}{e_{IN}} = K_3 G_3 = 16.8\,db\ \frac{(-1)\left(1 - j\frac{f}{5.07\times10^9}\right)}{\left(1 + j\frac{f}{12.5\times10^3}\right)\left(1 + j\frac{f}{391\times10^3}\right)}$$

And the common mode response is:

$$(\text{eq. } 3.1.4)\quad \frac{e_o}{e_{IN}} = K_4 G_4 = 20\,db\,\frac{(-1)\left(1-j\frac{f}{5.07\times10^9}\right)}{\left(1-j\frac{f}{10.7\times10^3}\right)\left(1+j\frac{f}{391\times10^6}\right)}$$

Since these 4 equations are so close, the normalized amplitude and the phase response of all four are given in Figure 3.1.2 (SB 48741-G)

The notation KG with different subscripts to distinguish between responses of different stages or circuits is used throughout this paper. K equals the d-c gain of the circuit under consideration and G equals the frequency variant portion of the amplitude and phase response. This form for the response is used to simplify the graphical solution of the equations.

Consider a circuit with two output terminals (A and B) and two input points (A^1 and B^1). The differential mode output is defined as the voltage at A minus the voltage at B. The common mode output is the mean value of the voltage at A and the voltage B, i.e.,

$$\frac{\text{Voltage at A + voltage at B}}{2}$$

Similarly the differential mode input is the voltage at A^1 minus the voltage at B^1 and the common mode input is:

$$\frac{\text{Voltage at } A^1 + \text{voltage at } B^1}{2}$$

The differential mode response is the ratio of the differential mode output to the differential mode input. The common mode response is the ratio of the common mode output to the common mode input.

Data useful for evaluation and maintenance of this circuit is given in the following tables for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V.

Table 3.1.1 VOLTAGE MEASUREMENTS (referred to ground)	
Point	Voltage (in volts d-c)
3a or 3b	+45
5a or 5b	-172.5
6a or 6b	+41 V.
7a or 7b	+37.2

Table 3.1.2 COMPONENT LOADING

Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
V_1-R3$_{a,b}$ thru V_7R50$_{a,b}$, 4.7K 47W 5% (per resistor)	205	43.7	8.94
R_{v1p} thru R_{v7p} 47 ohm 2W 5% (per resistor)	4	87.4	0.359
R_{v1s} thru R_{v7s} 39 ohm $\frac{1}{2}$ W 5% (per resistor)	0.21	5.38	0.0012
R_{v1g} thru R_{v7g} 100 ohm $\frac{1}{2}$ W 5%	0	0	0
R50-1 680 ohm 47W 5%	52.6	77.4	4.07
C100 0.47 µf 200 V.	37.4	----	----
V_1 thru V_7 6146 P-K (per tube)	191	87.4	16.7
V_1 thru V_7 6146 SC-K (per tube)	187	5.38	1.01

Table 3.1.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
+250	1225	306
+90	77.4	6.96
-150	1300	195

Figure 3.1.3 (SA 48736-G) shows how this circuit behaves as the +90 volt marginal check line is varied. Different values of gm for each side of the output circuit were simulated by operating the stage with less tubes in parallel. Under normal operating conditions the amplifier will fail when the gm of each side of the output stage falls below 50% of bogie. With a 40 volt downward swing to +50 volts on the +90 volt marginal check line the circuit will operate until the average gm of the output stage is below 61% of bogie for a 1 K load or below 53% of bogie for a 500 ohm load. The circuit fails sooner under the 1 K load condition because of the larger voltage swing required at the output than for the 500 ohm load condition.

Failure is considered to occur when the line driver output waveform changes in amplitude or when the rise time exceeds specifications.

3.2 OUTPUT DRIVER STAGE

Figure 3.2.1 (SA 61262) indicates the circuitry of the output driver cathode follower which supplies the necessary power to drive the output stage. Drawings 3006878 and 3006879 show the required card assembly and detail to form this circuit.

The complex expressions for the gain of this stage are stated in the following two equations. (Refer to MIT Comp. Book #648, Pg. 45, for detailed solution.)

For the differential mode:

(eq. 3.2.1)

$$\frac{e_o}{e_{IN}} = K_5 G_5 = -2.01\,db\ \frac{\left(1 + j\,\frac{f}{53.1 \times 10^6}\right)}{\left(1 + j\,\frac{f}{4.7 \times 10^6}\right)}$$

For the common mode:

(eq. 3.2.2)

$$\frac{e_o}{e_{IN}} = K_6 G_6 = -2.46db\ \frac{\left(1+j\,\frac{f}{3.26\times10^6}\right)\left(1+j\,\frac{f}{49.8\times10^6}\right)}{\left(1+j\,\frac{f}{1.30\times10^6}\right)\left(1+j\,\frac{f}{12.7\times10^6}\right)}$$

Figure 3.2.2 (SB 48742-G) is a graph of eq. 3.2.1 and eq. 3.2.2 showing the normalized amplitude and the phase response of this stage as it operates in the differential mode and the common mode.

Data useful for evaluation and maintenance of this circuit is given in the following tables.

The data is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V.

Table 3.2.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
9	-40
5a or 5b	-172.5
10a or 10b	-197

Table 3.2.2 COMPONENT LOADING			
Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R47-7 thru R47-11 6.8K 1W 5% (per resistor)	40	5.89	0.236
R47-1 thru R47-6 27K 2W 5% (per resistor)	127.5	4.72	0.601
RV8-1, RV8-4 1K ½W 5%	0	0	0
V8a or V8b, 5998	122.5	14.2	1.74

Table 3.2.3 POWER SUPPLY REQUIREMENTS		
Voltage (in volts)	Current (in ma.)	Power (in watts)
-300 (B7)	28.4	8.52

When the -300 volt marginal check line (B7) is swung down we check V8, V7, V4, and V3b. We check V5 and V6 when this marginal check line is swung up. Each of these tubes will be considered separately in the appropriate individual stage analysis where all of the other tubes in the amplifier will be assumed to be at bogie gm.

Figure 3.2.3 (SA 48739-G) shows where the amplifier fails depending upon the amount of marginal check voltage and the condition of $V8_a$ and $V8_b$. Under normal operating conditions the amplifier will fail when the gm of $V8_a$ and $V8_b$ (5998) falls to 8% of bogie gm. If the -300 volt marginal check line (B7) is swung down to -315 volts, then the amplifier will fail if the gm of $V8_a$ and $V8_b$ has gone below 58% of bogie gm.

3.3 BUFFER CATHODE FOLLOWER

The circuit schematic for the buffer cathode follower is shown in Figure 3.3.1 (SA 65907). The card assembly and detail required to form this circuit are shown on drawings 3006876 and 3006877.

The complex expressions for the gain of this stage are given in the following two equations (refer to MIT Comp. Book #648, Pg. 51).

For the differential mode:

$$\text{(eq. 3.3.1)}\quad \frac{e_o}{e_{IN}} = K_7 G_7 = -9.05\,db\,\frac{\left(1+j\frac{f}{23.4\times10^3}\right)\left(1+j\frac{f}{92.8\times10^6}\right)}{\left(1+j\frac{f}{52.9\times10^3}\right)\left(1+j\frac{f}{17.7\times10^6}\right)}$$

For the common mode:

$$\text{(eq. 3.3.2)}\quad \frac{e_o}{e_{IN}} = K_8 G_8 = -9.05\text{db}\,\frac{\left(1+j\frac{f}{23.4\times10^3}\right)\left(1+j\frac{f}{92.8\times10^6}\right)}{\left(1+j\frac{f}{51.6\times10^3}\right)\left(1+j\frac{f}{14.1\times10^6}\right)}$$

Figure 3.3.2 (SB 48743-G) is a graph of equation 3.3.1 and equation 3.3.2 showing both the differential mode and common mode responses of this stage.

Data useful for the evaluation and maintenance of this stage is given in the following three tables. The data is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V.

Table 3.3.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
10a or 10b	-197
11a or 11b	-15
12a or 12b	17.5

Table 3.3.2 COMPONENT LOADING

Components	Voltage (in volts)	Current (in ma.)	Power (in watts)
R42-1 or R42-2 68K 2W 1%	182	2.67	0.486
R42-3 or R42-4 39K 2W 1%	103	2.67	0.275
C42-2 or C42-3 100pf 500. V.	182	----	----
$V7_a$ or $V7_b$, Z2177	165	2.67	0.440

Table 3.3.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
+150	5.34	0.80
-300 (B7)	5.34	1.60

Figure 3.3.3 (SA 48740-G) shows where the amplifier fails depending upon the amount of marginal check voltage and the condition of V_{7a} and V_{7b}. Under normal operating conditions the amplifier will fail when the gm of V_{7a} and V_{7b} falls to 18% of bogie gm. If the -300 volt marginal check line (B_7) is moved to -315 volts the amplifier will fail if the gm of V_{7a} or V_{7b} has gone below 23% of bogie gm.

3.4 DIFFERENTIAL AMPLIFIER STAGE

Figure 3.4.1 (SA 61708) shows the circuitry of the differential amplifier stage. Drawings 3006874, 3070187, 3006875, 3070186 show the required card assemblies and details for this circuit.

The differential compensation control R35-1 allows for an optimum adjustment of frequency response and Nyquist stability for differential mode signals in spite of differences between line drivers due to tolerances of components.

The complex expressions for gain of this stage are stated in the following three equations (refer to MIT Comp. Book #880, Pg. 23).

For the differential mode with R35-1 equal to zero ohms.

(eq. 3.4.1)

$$\frac{e_o}{e_{IN}} = K_{9a} G_{9a} = 44.7db \; \frac{(-1)\left(1+j\frac{f}{58.9\times10^3}\right)\left(1-j\frac{f}{90.9\times10^9}\right)}{\left(1+j\frac{f}{5.63\times10^3}\right)\left(1+j\frac{f}{118\times10^3}\right)}$$

For the differential mode with R35-1 equal to 50K.

(eq. 3.4.2)

$$\frac{e_o}{e_{IN}} = K_{9b} G_{9b} = 44.7db \; \frac{(-1)\left(1+j\frac{f}{21.2\times10^3}\right)\left(1+j\frac{f}{58.9\times10^3}\right)\left(1-j\frac{f}{91.0\times10^9}\right)}{\left(1+j\frac{f}{32.2\times10^3}\right)\left(1+j\frac{f}{4.97\times10^3}\right)\left(1+j\frac{f}{968\times10^3}\right)}$$

For the common mode the response is:

(eq. 3.4.3)

$$\frac{e_o}{e_{IN}} = K_{10} G_{10} = 7.15db \; \frac{(-1)\left(1+j\frac{f}{59.0\times10^3}\right)\left(1+j\frac{f}{6.60\times10^6}\right)\left(1-j\frac{f}{6.55\times10^6}\right)}{\left(1+j\frac{f}{9.39\times10^3}\right)\left(1+j\frac{f}{1.12\times10^6}\right)\left(1+j\frac{f}{23.0\times10^6}\right)}$$

The normalized amplitude and the phase responses of this stage as stated in equations 3.4.1 and 3.4.2 are plotted in Figure 3.4.2 (SB 48744-G). Similarly a plot of equation 3.4.3 is given in Figure 3.4.3 (SB 48745-G).

Data useful for evaluation and maintenance of this circuit is given in the following three tables. The data is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V while the other is biased at +180 V.

Table 3.4.1 VOLTAGE MEASURMENTS (referred to ground)

Point	Voltage (in volts d-c)
12a or 12b	-17.5
13	-137
14a or 14b	-140

Table 3.4.2 COMPONENT LOADING

Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R39-1, 2, 6, or 7 180K 2W 5% (per resistor)	267.5	1.48	0.396
R39-8 or 9 39K 2W 5%	163	4.17	0.680
R39-3 or 5 18K ½W 5%	0	0	0
R35-1 50K pot.	0	0	0
C39-1, 3 150 pf 500 V.	17	0	0
C39-2 150 pf 500 V.	0	0	0
V_5 or V_6, 6136, P-K	119.5	2.96	0.354
V_5 or V_6, 6136, SC-K	137	1.21	0.166

Table 3.4.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
+250	5.92	1.48
-300 (C_3)	8.34	2.50

Figure 3.4.4 (SA 48746-G) shows a plot of marginal check data as taken on this stage. To simulate the gm of the tubes decreasing, the screen voltage was decreased and readings were taken at points of failure caused under various combinations of screen voltage and marginal check line voltage. Under normal operating conditions the circuit will fail when the gm of V_5 and V_6 falls below 11% of bogie gm. This failure point is determined from point A of Figure 3.4.4. From point B of this same figure we determine when the circuit will fail under a 15 volt positive swing on the marginal check line. When the -300 volt marginal check line (B_7) is swung up to -285 volt, the circuit will fail when the gm of V_5 and V_6 has decreased to 50% of bogie.

3.5 INPUT CIRCUIT TO DIFFERENTIAL AMPLIFIER

Figure 3.5.1 (SA 61709) shows the input circuit to the differential amplifier. The drawings which show the necessary card assemblies and details are 3006880, 3070187, 3006881, and 3070186. First the response of this stage to differential mode signals is considered. Provision is made to adjust the ratio of currents flowing through each half of the input circuit (V_{4a} and V_{4b}) by means of a position control. This allows a control of the d-c levels at the inputs to the differential amplifier, points 14a and 14b, despite component differences in each half of the line driver push pull stages. The position of the beam in the display tube can thus be controlled manually.

The differential output is at the plates of V4 (14a and 14b) with the input between points E5, or E6, and E7 or E8.

The response of this signal is given in the following equation (refer to MIT Comp. Book #880 Pg. 46 for complete solution.) The gain control is set for a normal overall gain from the line driver of 3.7.

(eq. 3.5.1)

$$\frac{e_o}{e_{IN}} = K_{11} G_{11} = -9.41\,db\,\frac{\left(1+j\frac{f}{140\times10^6}\right)\left(1+j\frac{f}{1.51\times10^6}\right)}{\left(1+j\frac{f}{136\times10^6}\right)\left(1+j\frac{f}{87.2\times10^3}\right)\left(1+j\frac{f}{1.93\times10^6}\right)}$$

Another differential response associated with this stage is the output produced between the plates of V_{4a} (14a) and V_{4b} (14b) (the grids of the differential amplifier V_5 and V_6) due to a differential signal between the feedback terminals C1 and C_5. This transfer function is given in the following equation (refer to MIT Comp. Book #880 Pg. 49)

(eq. 3.5.2)

$$\frac{e_o}{e_{IN}} = K_{13} G_{13} = -20.84\,db\,\frac{\left(1+j\frac{f}{67.7\times10^3}\right)\left(1+j\frac{f}{140\times10^6}\right)}{\left(1+j\frac{f}{87.9\times10^3}\right)\left(1+j\frac{f}{1.92\times10^6}\right)\left(1+j\frac{f}{137\times10^6}\right)}$$

Figure 3.5.2 (SB 48754-G) is the graph showing the normalized amplitude and the phase response for eq. 3.5.1 and 3.5.2.

The response of this stage to a common mode signal which has its output at the plate and input at the grid of V_{4a} or V_{4b} is given in the following expression (refer to MIT Comp. Book #880 Pg. 31) for complete solution.

(eq. 3.5.3)

$$\frac{e_o}{e_{IN}} = K_{15}G_{15} = 17.2db \frac{(-1)\left(1+j\frac{f}{884\times10^3}\right)\left(1-j\frac{f}{4.53\times10^6}\right)\left(1+j\frac{f}{130\times10^6}\right)}{\left(1+j\frac{f}{116\times10^3}\right)\left(1+j\frac{f}{1.24\times10^6}\right)\left(1+j\frac{f}{136\times10^6}\right)}$$

Figure 3.5.3 (SB 48753-G) is a plot of eq. 3.5.3 and shows the normalized amplitude and the phase response of this stage for common mode signals.

A fourth response associated with this stage is for an output at the grids of the differential amplifier (V_5 or V_6) due to a common mode signal appearing at the feedback terminals C_1 and C_5. The following equation gives this response (see MIT Comp. Book #880 Pg. 55) for complete solution.

(eq. 3.5.4)

$$\frac{e_o}{e_{IN}} = K_{14}G_{14} = -16.1db \quad \frac{\left(1+j\frac{f}{67.7\times10^3}\right)\left(1+j\frac{f}{140\times10^6}\right)}{\left(1+j\frac{f}{88.3\times10^3}\right)\left(1+j\frac{f}{138\times10^6}\right)}$$

The fifth and last response for this stage is for an output at the grids of the differential amplifier (V_5 or V_6) due to a common mode signal appearing at an input terminal to the amplifier E_5, E_6, E_7, or E_8. This response is stated in the next equation (see MIT Comp. Book #880. Pg. 54).

(eq. 3.5.5)

$$\frac{e_o}{e_{IN}} = K_{12}G_{12} = -9.38db \frac{\left(1+j\frac{f}{884\times10^3}\right)\left(1+j\frac{f}{140\times10^6}\right)}{\left(1+j\frac{f}{87.1\times10^3}\right)\left(1+j\frac{f}{1.12\times10^6}\right)\left(1+j\frac{f}{136\times10^6}\right)}$$

Figure 3.5.4 (SB 48762-G) is a plot of equations 3.5.4 and 3.5.5.

Voltage, current, and power data for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V. is given in the following three tables.

Table 3.5.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
14a or 14b	-140
15	-270
26a or 26b	+180
27a or 27b	+150
C1 or C5	+45

Table 3.5.2 COMPONENT LOADING

Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R27-4, 5, R30-4, 5 0.47M 2W 1% (per resistor)	320	0.68	0.218
R27-3, 6 R30-3, 6 0.47M 2W 1% (per resistor)	290	0.617	0.179
R35-5, 6 39K 1W 1% (per resistor)	14.2	0.364	0.0052
R27-1, 2, 7, 8, R30-1, 2, 7, 8 0.47M 1W 1% (per resistor)	85.4	0.182	0.016
C27-1, 2, 3, 4 C30-1, 2, 3, 4 5pf 500 V. (per capacitor)	85.4	0	0
R35-4 82K 2W 1%	0	0	0
R35-3 50K 2W pot.	0	0	0
R V4-3, R V4-8 10K 1W 1% (per resistor)	28.6	2.86	0.082
Position Control 1K 2W pot.	1.4	2.86	0.008 (required)
V4a or V4b Z2177	130	2.86	0.372

Table 3.5.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
-300 (C_3)	5.72	1.72

Figure 3.5.5. (SA 48737-G) shows how the voltage on the plate and on the cathode of V_{4a} or V_{4b} varies as the -300 volt marginal check line B_7 is varied. It is seen that when the marginal check voltage is increased in a negative direction the plate to cathode voltage on each half of V4 is decreased and the plate current is increased. This therefore, is the direction of swing on the marginal check line which can move the operating point of V4 so as to cause the line driver to fail earlier. Under normal operating conditions the line driver will fail if the gm of V_{4a} and V_{4b} drops to 44% of bogie gm. If the marginal check line is moved to -315 volts the driver fails if the gm of each half of V4 drops below 76% of bogie.

Figure 3.5.6 (SA 48738-G) shows a plot of line driver failure points using the axes of V4 filament voltage and marginal check line excursion. A comparison is made between a Z2177 and a 6072 tube, the 6072 having about one half the gm of a Z2177. This curve shows that for a down V4 (50% down when a 6072 is used for the Z2177) the line driver failure will occur with a smaller excursion on the -300 volt marginal check line, B7. This simply serves as an additional indication that this particular marginal check line effectively checks V4. The filament voltage has no effect on the failure point until a critical value is reached which then abruptly causes failure regardless of the amount of marginal check voltage.

3.6 REFERENCE DRIVER CATHODE FOLLOWER

The circuit schematic for the reference driver is given in Figure 3.6.1 (SA 61710). The card assembly and detail for this stage is given in drawings 3006870 and 3006871. The gain for this stage is given in the following expression (refer to MIT Comp. Book #648 Pg. 53).

(eq. 3.6.1)

$$\frac{e_o}{e_{IN}} = K_{16} G_{16} = -18.1\,db\, \frac{\left(1+j\frac{f}{78.6\times10^3}\right)\left(1+j\frac{f}{92.8\times10^6}\right)}{\left(1+j\frac{f}{290\times10^3}\right)\left(1+j\frac{f}{20.7\times10^6}\right)}$$

Figure 3.6.2 (SB 48757-G) is the plot of eq. 3.6.1 and shows the normalized amplitude and the phase response of this stage.

Information helpful in evaluating and maintaining this circuit is given in the following three tables. The data is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V.

Table 3.6.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
16	-271
17	-77

Table 3.6.1 VOLTAGE MEASUREMENTS (Con't)	
Point	Voltage (in volts d-c)
18	-80

Table 3.6.2 COMPONENT LOADING			
Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R19-1 11K 1W 1%	29	2.6	0.076
R19-2 75K 2W 1%	194	2.6	0.505
C19-1 27pf 500 V.	194	0	0
V_{3b} $\frac{1}{2}$Z2177	167	2.6	0.434

Table 3.6.3 POWER SUPPLY REQUIREMENTS		
Voltage (in volts)	Current (in ma.)	Power (in watts)
+90	2.6	0.234
-300 (C_3)	2.6	0.780

Figure 3.6.3 (SA 48735-G) is a graph of points of failure for the line driver under various combinations of V_{3b} plate supply voltage and -300 volt marginal check line (B_7) voltage. By decreasing the plate supply voltage on this stage, we simulate the action of the tube as it decreases in gm. From the curve it is seen that the lower the gm of the tube, the smaller is the marginal check line excursion (in the negative direction) required to cause failure. Using data from this curve at point A and operating data for this stage and the tube characteristics it turns out that under normal operating conditions the line driver will fail when V_{3b} drops below 10% of its bogie gm. If the -300 volt marginal check line (B_7) is moved to -315 volts then the line driver will fail at point B of Figure 3.6.3 if the gm of V_{3b} drops below 14% of its bogie value.

3.7 REFERENCE AMPLIFIER

The circuit schematic for the reference amplifier is given in Figure 3.7.1 (SA 61711). The required card assemblies and details are shown on drawings 3006872, 3006900, 3070187, 3006873, 3006901 and 3070186.

The mean level compensation control (R35-2) allows for an optimum adjustment of frequency response and Nyguist stability for common mode signals in spite of differences between line drivers due to tolerances of components.

The mean level adjust control (R16-3) allows the mean level reference voltage to be manually preset so that the desired +45 volt mean level at the output of the line driver can be obtained despite differences between line drivers due to tolerances of components.

The complex response of this stage is given in the following two equations. The input is at the grid of V_{3a} and the output is taken at the plate of V_1. (See MIT Comp. Book #648 Pg. 54 for complete solution).

For R35-2 equal to zero:

(eq. 3.7.1)

$$\frac{e_o}{e_{IN}} = K_{17a} G_{17a} = 43.2\,db\ \frac{\left(1+j\frac{f}{159\times10^6}\right)\left(1+j\frac{f}{79.6\times10^6}\right)}{\left(1+j\frac{f}{160}\right)\left(1+j\frac{f}{102\times10^6}\right)}$$

For R35-2 equal to 5K

(eq. 3.7.2)

$$\frac{e_o}{e_{IN}} = K_{17b} G_{17b} = 43.2\,db\ \frac{\left(1+j\frac{f}{159\times10^6}\right)\left(1+j\frac{f}{79.6\times10^6}\right)\left(1+j\frac{f}{3.18\times10^3}\right)}{\left(1+j\frac{f}{157}\right)\left(1+j\frac{f}{4.24\times10^6}\right)\left(1+j\frac{f}{61.8\times10^6}\right)}$$

The normalized amplitude and the phase response as given by these two equations is plotted in Figure 3.7.2 (SB 48758-G).

Operating data for this stage which is helpful in evaluating and maintaining the circuit is given in the next three tables. The data (as for all corresponding tables in the other sections) is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V.

Table 3.7.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
18	-80
19	-148
20	-150
21	-172
22	-150

Table 3.7.2 COMPONENT LOADING

Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R10-3 120K 2W 5%	330	2.75	0.907
R35-2 .5K 2W pot.	0	0	0
R10-8, 9 39K 2W 5% (per resistor)	152	3.90	0.594
R16-1 100K 1W 1%	150	1.50	0.225
R16-2 1M ½W 5%	86	0.086	0.0074
R16-3 50K 2W pot.	22	1.50	0.112 (required)
R16-5 33K 1W 5%	128	3.88	0.497
C35-1 .01μf 600 V.	80	0	0
C10-2 .01 μf 600 V.	150	0	0
V_1 6136 P-K	68	2.75	0.187
V1 6136 SC-K	148	1.10	0.163
V_{3a} ½Z2177	148	3.95	0.585
V16-1 WA5783	86	2.38	0.205
V16-2 WA 5783	86	2.29	0.197

Table 3.7.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
+250	2.75	0.687
-300 (D_8)	7.8	2.34
-300 (C_3)	3.88	1.16

Figure 3.7.3 (SA 48760-G) is a plot of points of failure for the line driver depending upon the amount of V_{3a} plate supply voltage and -300 volt marginal check line (D_8) voltage. Decreasing values of plate supply voltage were used to simulate V_{3a} decreasing in gm. From the information on Figure 3.7.3 (at pt. A), operating data for this stage and the tube characteristic curve it is determined that under normal operating conditions the line driver will fail when the gm of V_{3a} has

dropped below 19% of bogie. If the -300 volt marginal check line D_8 is swung to -360 volts failure will occur if the gm of V_{3a} has fallen below 33% of bogie. No effective means for marginal checking V_1 has been found.

3.8 INPUT CIRCUIT TO REFERENCE AMPLIFIER

Figure 3.8.1 (SA 65906) shows the circuitry for this stage. The necessary card assemblies and details are shown on drawings 3006872, 3006900, 3006870, 3006873, 3006901 and 3006871.

The mean level rejection control is provided so that the value of resistance from each feedback terminal (C_1 and C_5) to the plate of V_2 can be made exactly equal. This balance of resistive values is necessary so that the differential signals appearing at the feedback terminals do not affect the mean level of the circuit.

The following equation gives the complex response of this stage for a mean level input at C_1 and C_5 and an output at the plate of V_2 (refer to MIT Comp. Book #880 Pg. 41)

(eq. 3.8.1)

$$\frac{e_o}{e_{IN}} = K_{18}G_{18} = -0.832\,db\,\frac{\left(1+j\frac{f}{71.8\times10^3}\right)\left(1+j\frac{f}{72.2\times10^3}\right)\left(1+j\frac{f}{129\times10^6}\right)}{\left(1+j\frac{f}{59.6\times10^3}\right)\left(1+j\frac{f}{70.3\times10^3}\right)\left(1+j\frac{f}{817\times10^3}\right)\left(1+j\frac{f}{125\times10^6}\right)}$$

The plot of this equation showing the normalized amplitude and the phase response of this stage is given in Figure 3.8.2 (SB 48759-G)

Data which may be used for evaluating and maintaining this stage is given in the following three tables. This data is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 while the other is biased at +180 V.

Table 3.8.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
C_1 or C_5	+45
22	-150
23	-214
24	-257
25	-256

Table 3.8.2 COMPONENT LOADING

Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R19-5, 6 27K 1W 1% (per resistor)	68.9	2.55	0.176
R19-3, 4 47K 2W 1% (per resistor)	120	2.55	0.306
R16-4 5K 2W pot.	6.1	2.55	0.045 (required)
C19-4, 5 82 pf 500 V.	68.9	0	0
C19-2, 3 47pf 500 V.	120	0	0
R10-6 10K 1W 1%	44	4.4ma	0.194
R10-7 68K 1W 1%	44	0.65	0.0286
R10-1, 2 330K 1W 1%	43	0.130	0.0056
R10-5 82K 2W 5%	214	2.61	0.558
C10-1 .01 μf 600 V.	43	0	0
V_2 Z2177 (per section)	106	2.55	0.271
V16-3 WA 5783	86	2.48	0.214

Table 3.8.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
-300 (D8)	7.66	2.30

Figure 3.8.3 (SA 48761-G) is a graph of marginal check data for V2. As the -300 volt marginal check line D8 is swung in the positive direction the plate to cathode voltage on V_2 decreases and the plate current through V2 remains constant. This direction of marginal check line swing effectively checks V_2. Under normal operating conditions the line driver will fail if the gm of V2 falls below 31% of bogie. If the -300 volt marginal check line D8 is moved to -275 volts the amplifier will fail if the gm of V_2 is below 58% of bogie.

Signed Henry E. Zieman
H. E. Zieman

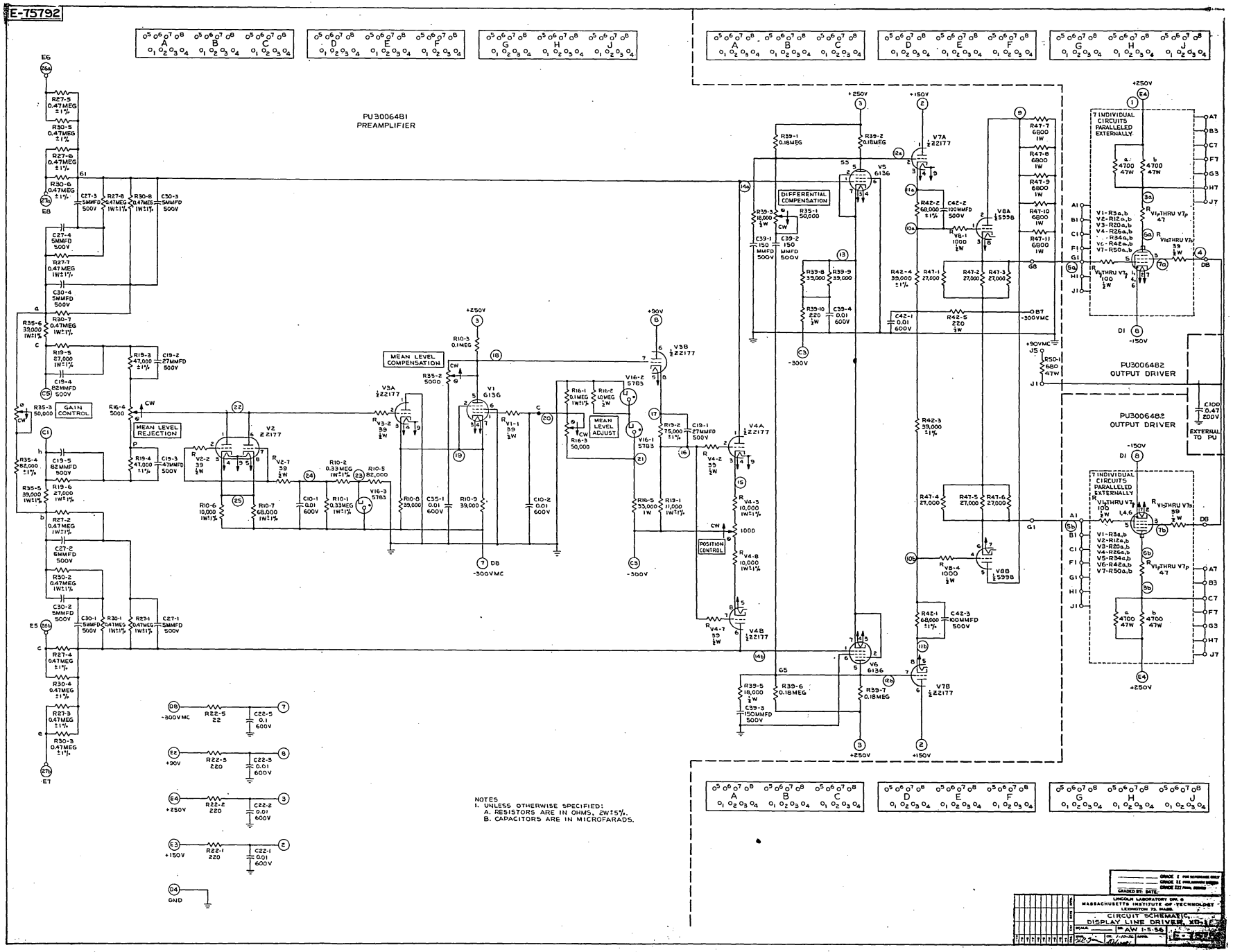
HEZ:JK:ej

Signed Joseph Kriensky
J. Kriensky

Attachments:

Fig. 1	E 75792
Fig. 2.0.1	SA 65536
Fig. 2.0.2	SA 65537
Fig. 3.1.1	SA 61516
Fig. 3.1.2	SB 48741-G
Fig. 3.1.3	SA 48736-G
Fig. 3.2.1	SA 61262
Fig. 3.2.2	SB 48742-G
Fig. 3.2.3	SA 48739-G
Fig. 3.3.1	SA 65907
Fig. 3.3.2	SB 48743-G
Fig. 3.3.3	SA 48740-G
Fig. 3.4.1	SA 61708
Fig. 3.4.2	SB 48744-G
Fig. 3.4.3	SB 48745-G
Fig. 3.4.4	SA 48746-G
Fig. 3.5.1	SA 61709
Fig. 3.5.2	SB 48754-G
Fig. 3.5.3	SB 48753-G
Fig. 3.5.4	SB 48762-G
Fig. 3.5.5	SA 48737-G
Fig. 3.5.6	SA 48738-G
Fig. 3.6.1	SA 61710
Fig. 3.6.2	SA 48757-G
Fig. 3.6.3	SA 48735-G
Fig. 3.7.1	SA 61711
Fig. 3.7.2	SB 48758-G
Fig. 3.7.3	SA 48760-G
Fig. 3.8.1	SA 65906
Fig. 3.8.2	SB 48759-G
Fig. 3.8.3	SA 48761-G

E-75792


PU3006481
PREAMPLIFIER
PU3006482
OUTPUT DRIVER
PU3006482
OUTPUT DRIVER
DIFFERENTIAL COMPENSATION
MEAN LEVEL COMPENSATION
MEAN LEVEL REJECTION
GAIN CONTROL
MEAN LEVEL ADJUST
POSITION CONTROL
7 INDIVIDUAL CIRCUITS PARALLELED EXTERNALLY.
EXTERNAL TO PU
+250V
+150V
+90V
-300V
-150V
GND
NOTES
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTORS ARE IN OHMS, 2W ±5%.
B. CAPACITORS ARE IN MICROFARADS.
CIRCUIT SCHEMATIC
DISPLAY LINE DRIVER, XD-1
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.
SCALE — NONE
DRAWN — AW 1-5-56
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

SA-65536

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY

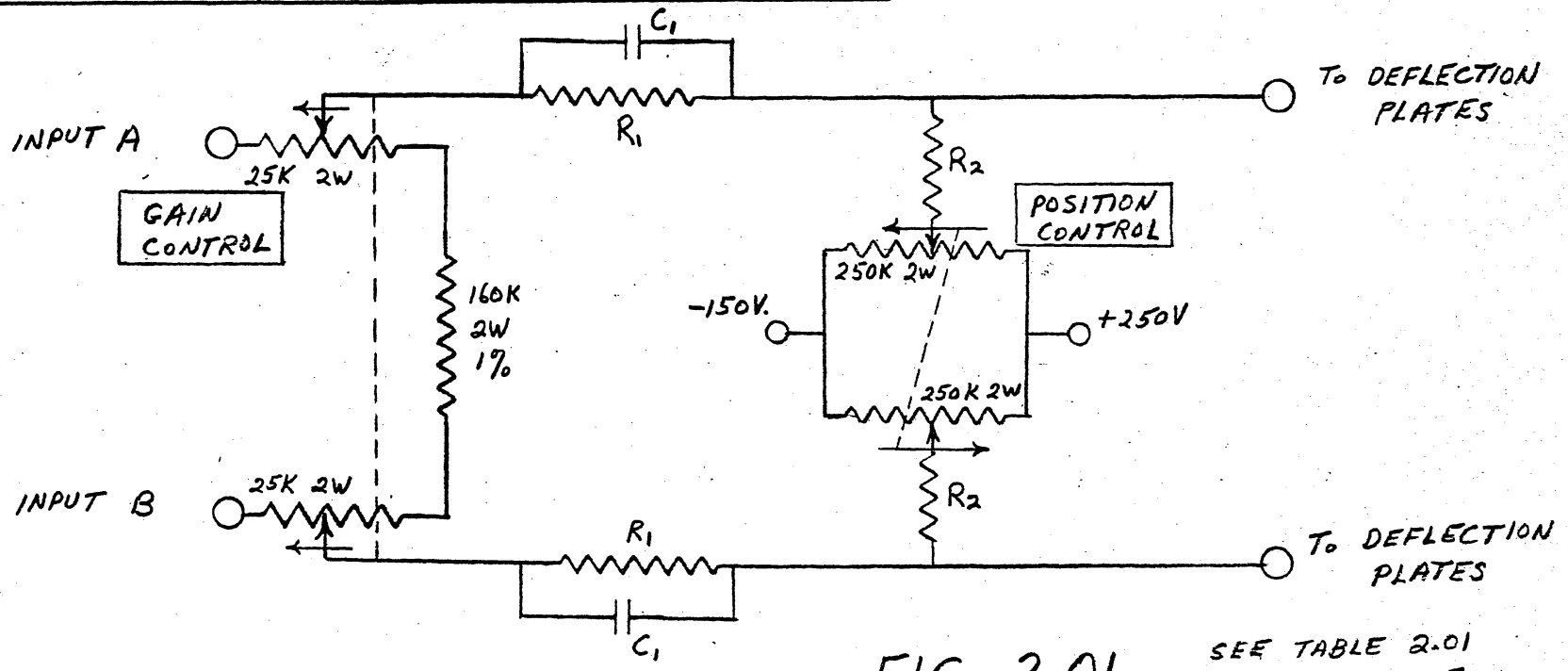


FIG. 2.01

SEE TABLE 2.01 FOR VALUES OF R_1, C_1 and R_2

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-20			
-19			
-18			
-17			
-16			
-15			
-14			
-13			
-12			
-11			
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2			
-1			

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

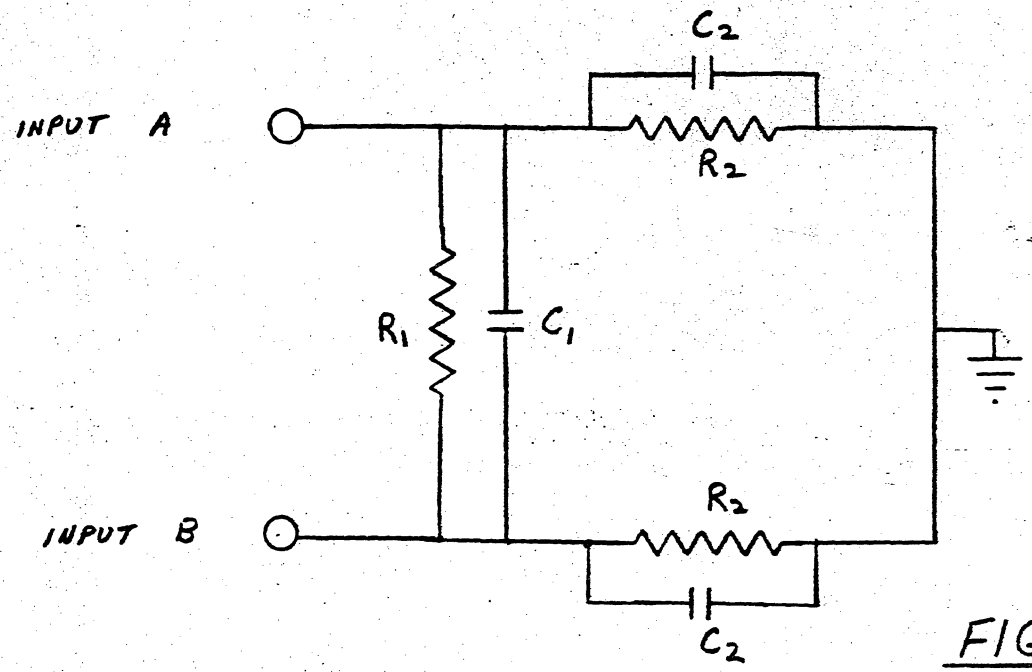
CONSOLE GAIN AND POSITION CONTROL

SCALE: DR. J. Krinsky
ENG. J. Krinsky CK. APPD.
SA-65536

8M-7-54-Boston Blue Print

SA- 65537

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



FOR INPUT CKT. TO ONE CONSOLE
SEE TABLE 2.02

FOR TOTAL LOAD ON EACH DRIVER
SEE TABLE 2.03

FIG. 2.02

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-20			
-19			
-18			
-17			
-16			
-15			
-14			
-13			
-12			
-11			
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2			
-1			

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

EQUIVALENT CIRCUIT

SCALE:
DR. J. Krainsky
ENG. J. Krainsky
CK.
APPD.

SA- 655 37

8M-7-54-Boston Blue Print

SA- 61516

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY

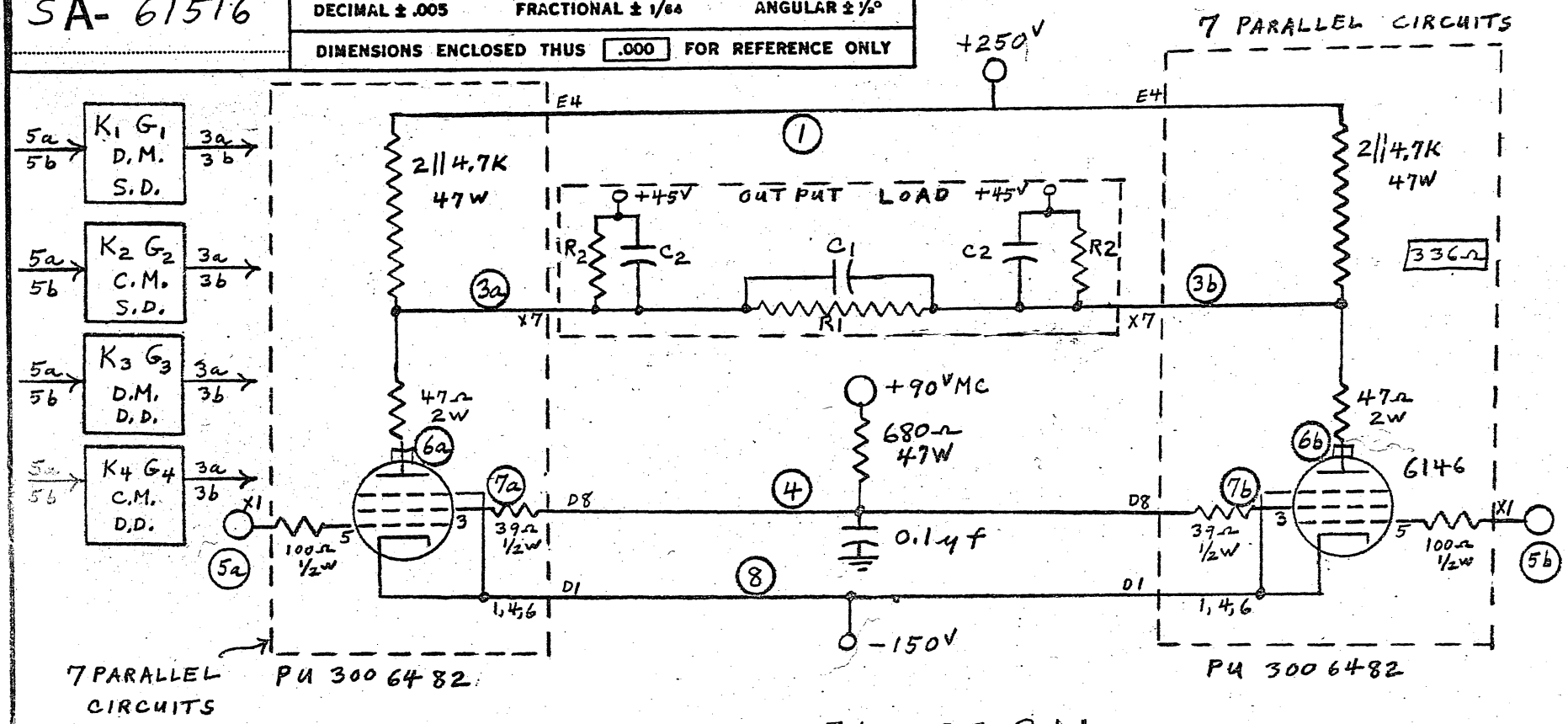


FIGURE 3.1.1

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-20			
-19			
-18			
-17			
-16			
-15			
-14			
-13			
-12			
-11			
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3		13/4/56	HEZ
-2		7/2/56	HEZ
-1		24/10/57	HEZ

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

LINE DRIVER OUTPUT STAGE

SCALE:
DR. H E Zieman
ENG. H. E. Zieman
CK.
APPD.

SA- 61516

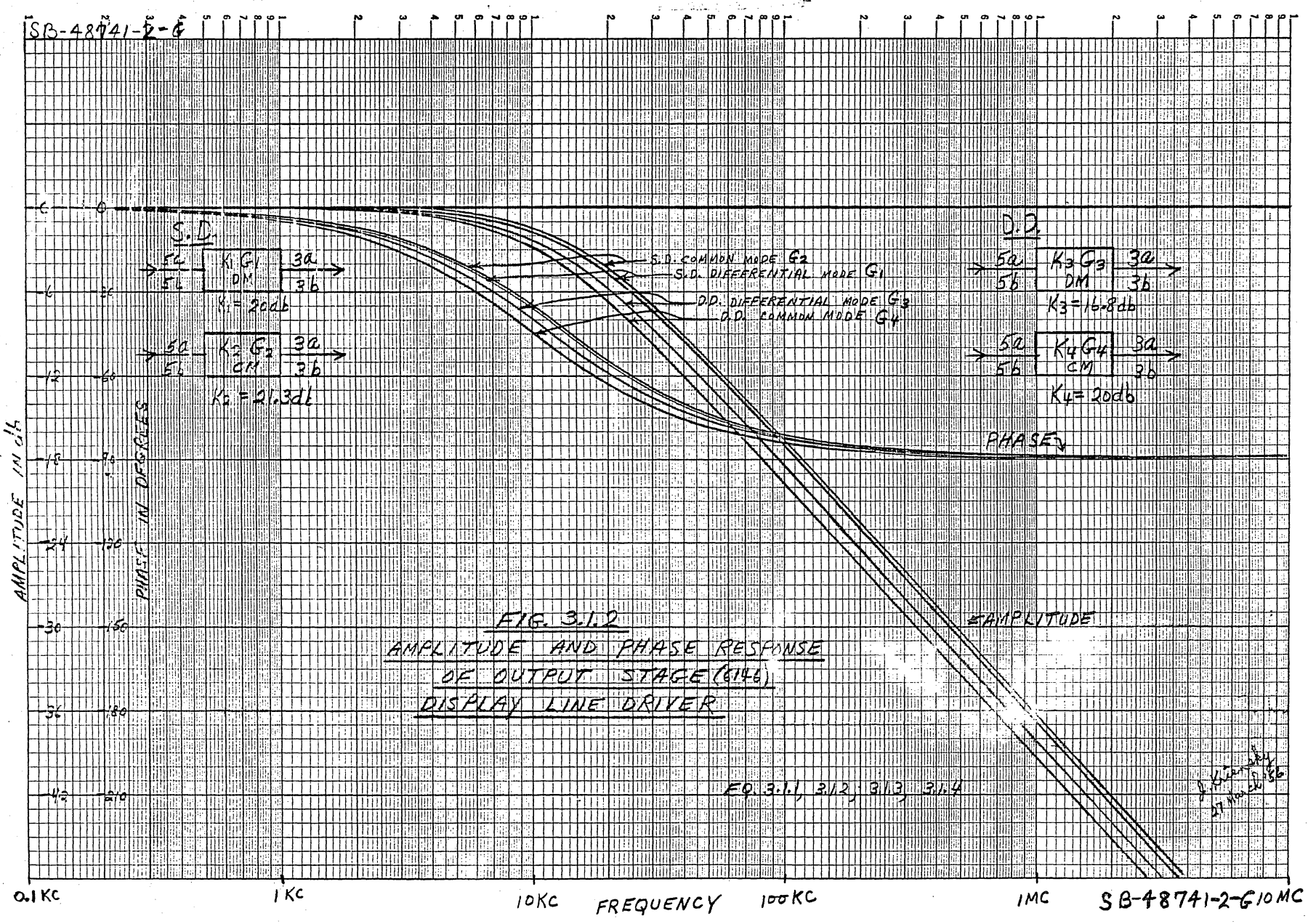
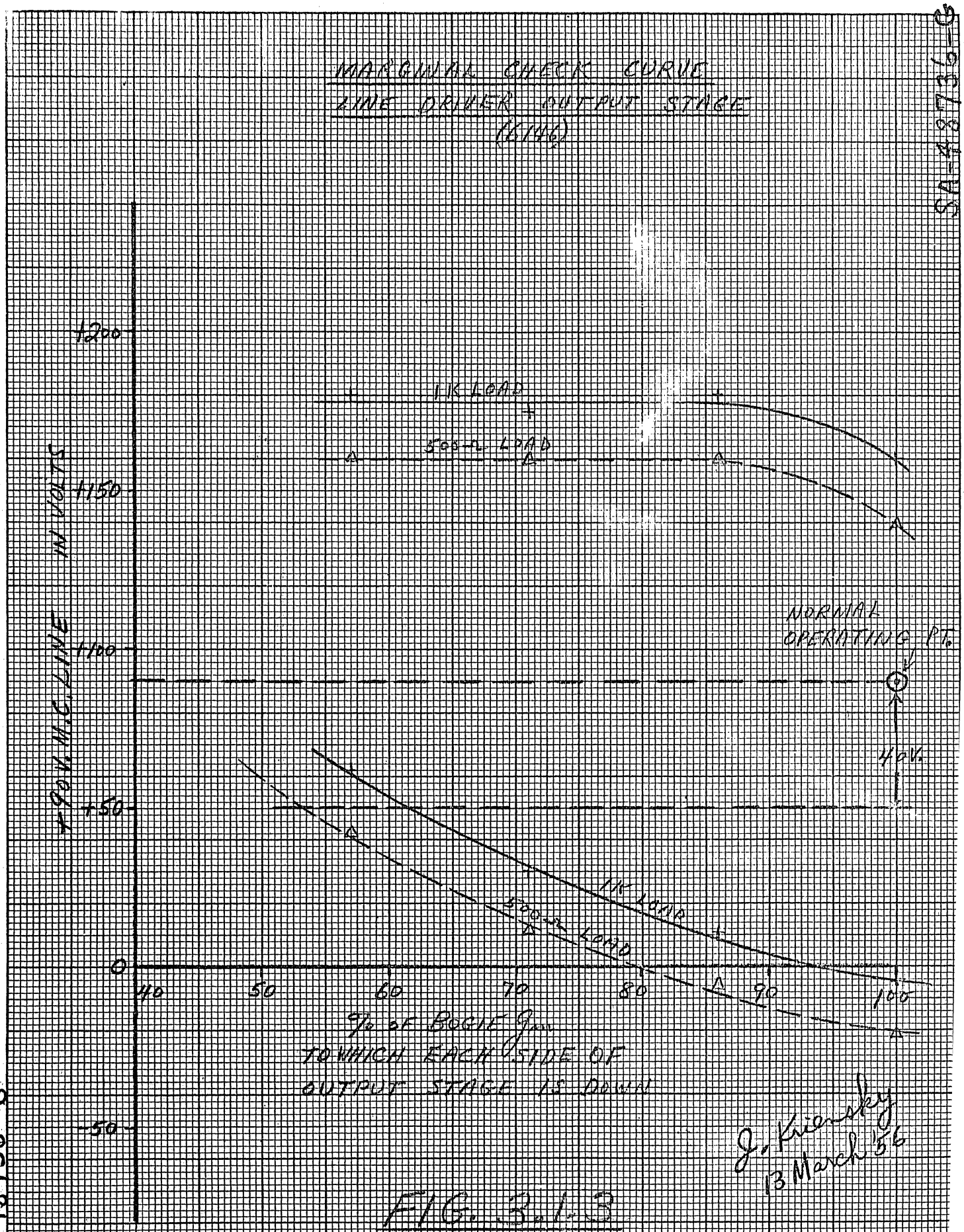


FIG. 3.1.2
AMPLITUDE AND PHASE RESPONSE
OF OUTPUT STAGE (6146)
DISPLAY LINE DRIVER

EQ. 3.1.1, 3.1.2, 3.1.3, 3.1.4

SA-48736-1-0

MARGINAL CHECK CURVE
LINE DRIVER OUTPUT STAGE
(6146)



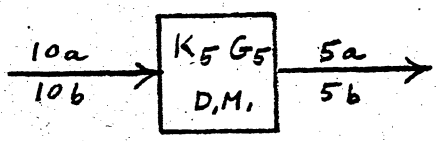
J. Kiorsky
13 March '56

FIG. 3.1-3

SA-48736-G

SA- 61262

SEE CARD ASSEMBLY
300 6878
SLOT 47



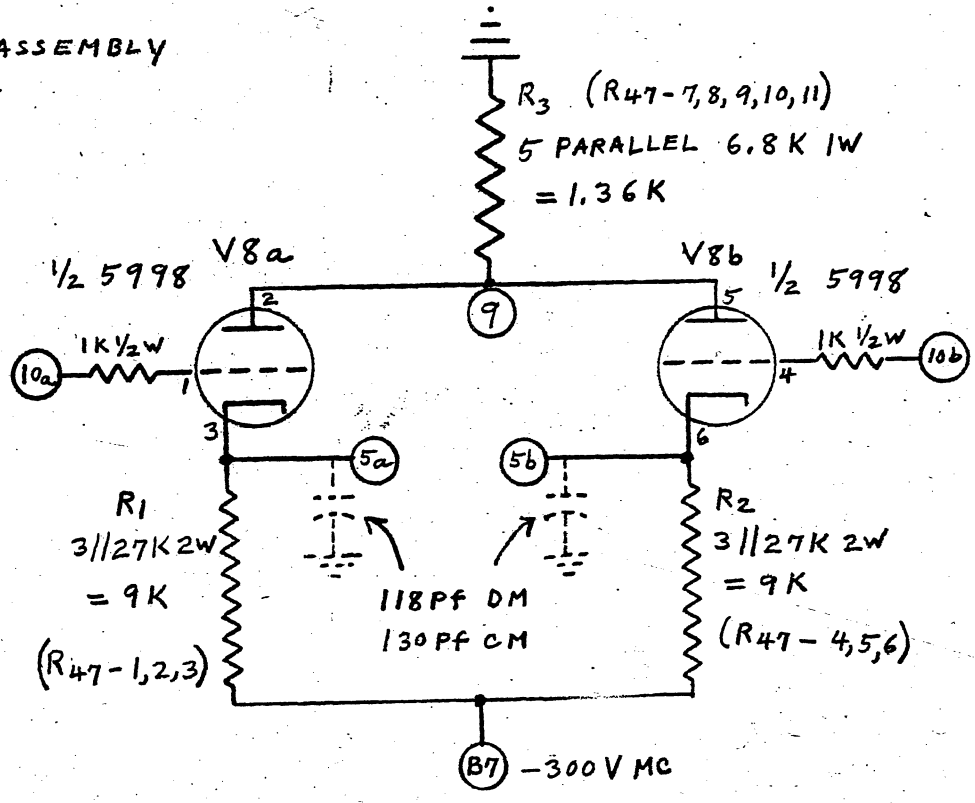


FIGURE 3.2.1

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3		13/4/55	HE Z
-2		7/2/56	HE Z
-1		24/10/55	HE Z

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO.

OUTPUT DRIVER STAGE

SCALE:	DR. HE Zieman	
ENG. HE Zieman	CK.	APPD.

SA- 61262

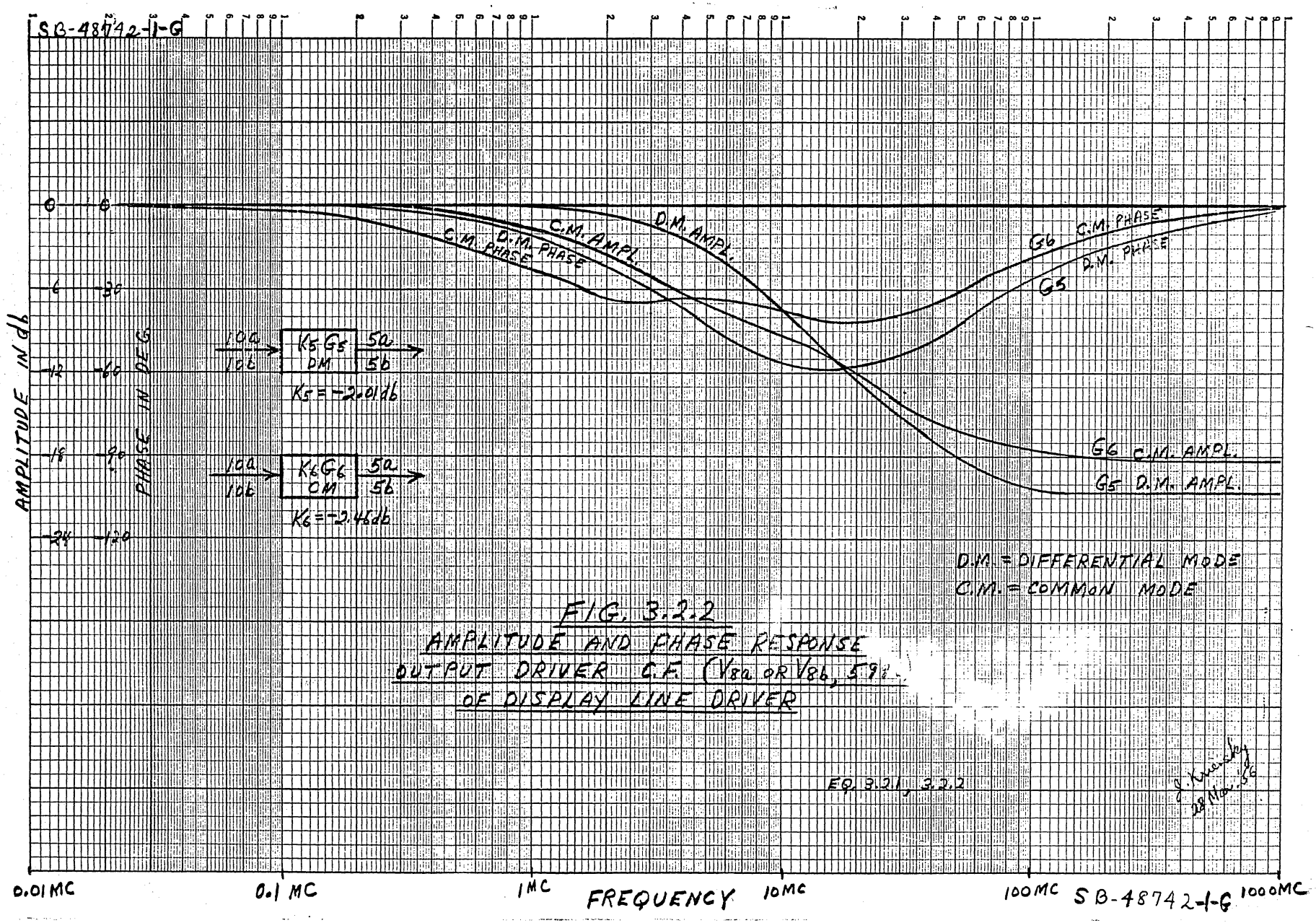


FIG. 3.2.2

AMPLITUDE AND PHASE RESPONSE
OUTPUT DRIVER C.F. (V_{8a} OR V_{8b}, 5 PL.)
OF DISPLAY LINE DRIVER

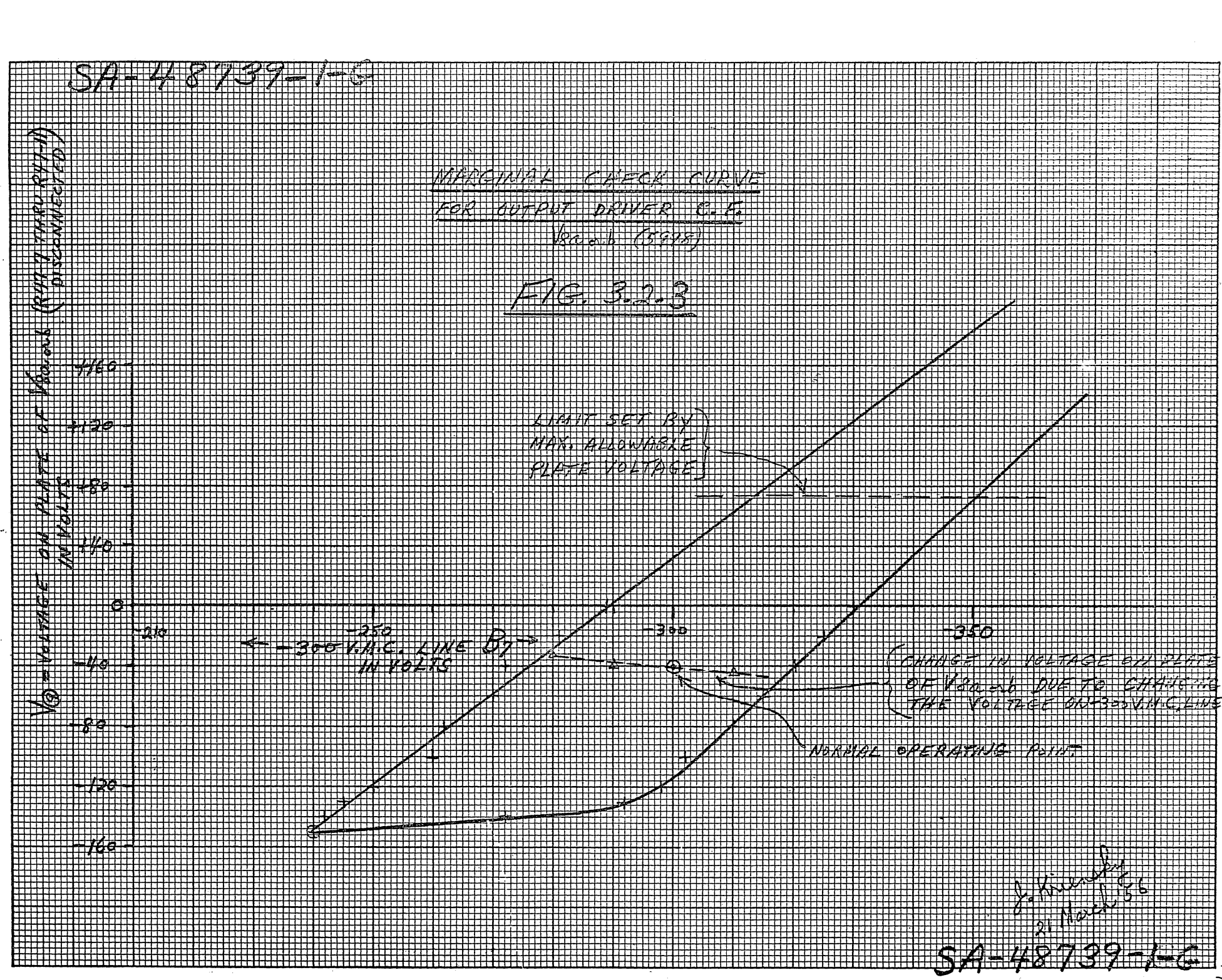
EQ. 3.2.1, 3.2.2

S. Whitby
28 Nov. '56

SA-48739-1-C

MARGINAL CHECK CURVE
FOR OUTPUT DRIVER C. F.
V_{R6ab} (6998)

FIG. 3-2-3

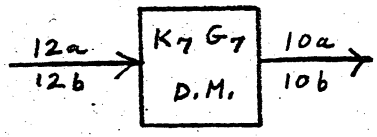


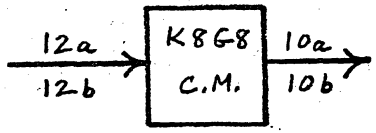
J. Kinderman
21 March 46

SA-48739-1-C

SA-65907

SEE CARD ASSEMBLY
3006876
SLOT 42





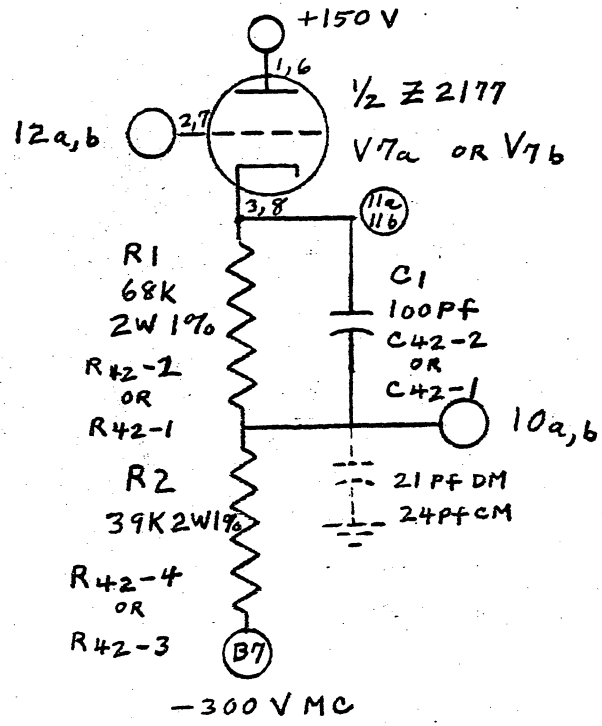


FIGURE 3.3.1

										APPD.
										DATE
										CN#
10	9	8	7	6	5	4	3	2	1	CHG.

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BUFFER CATHODE FOLLOWER

SCALE:	DR. H E Zieman	SA-65907
ENG. H.E. Zieman	CK.	APPD.

SB-48743-1-6

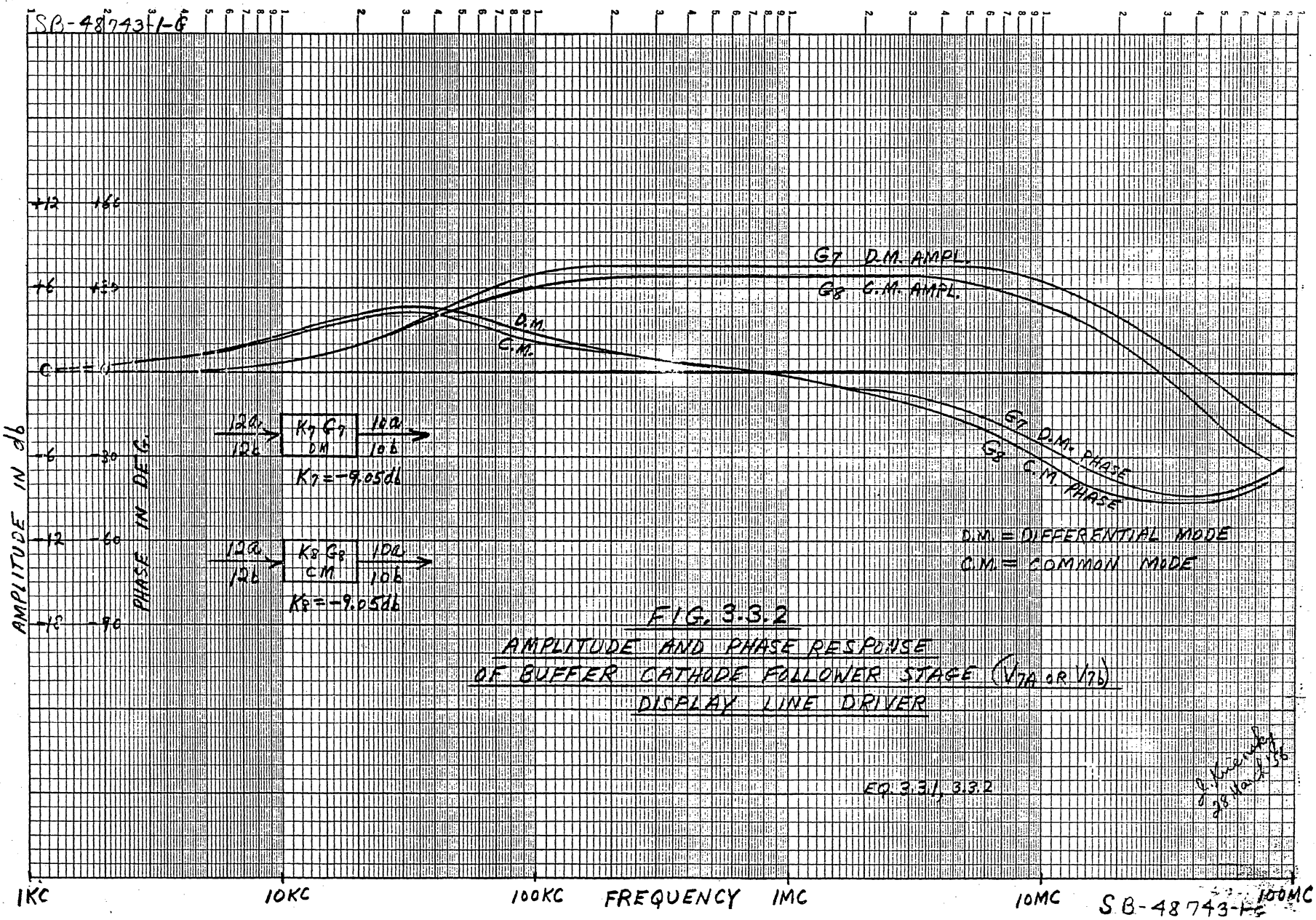


FIG. 3.3.2

AMPLITUDE AND PHASE RESPONSE OF BUFFER CATHODE FOLLOWER STAGE (V_{7A} OR V_{7B}) DISPLAY LINE DRIVER

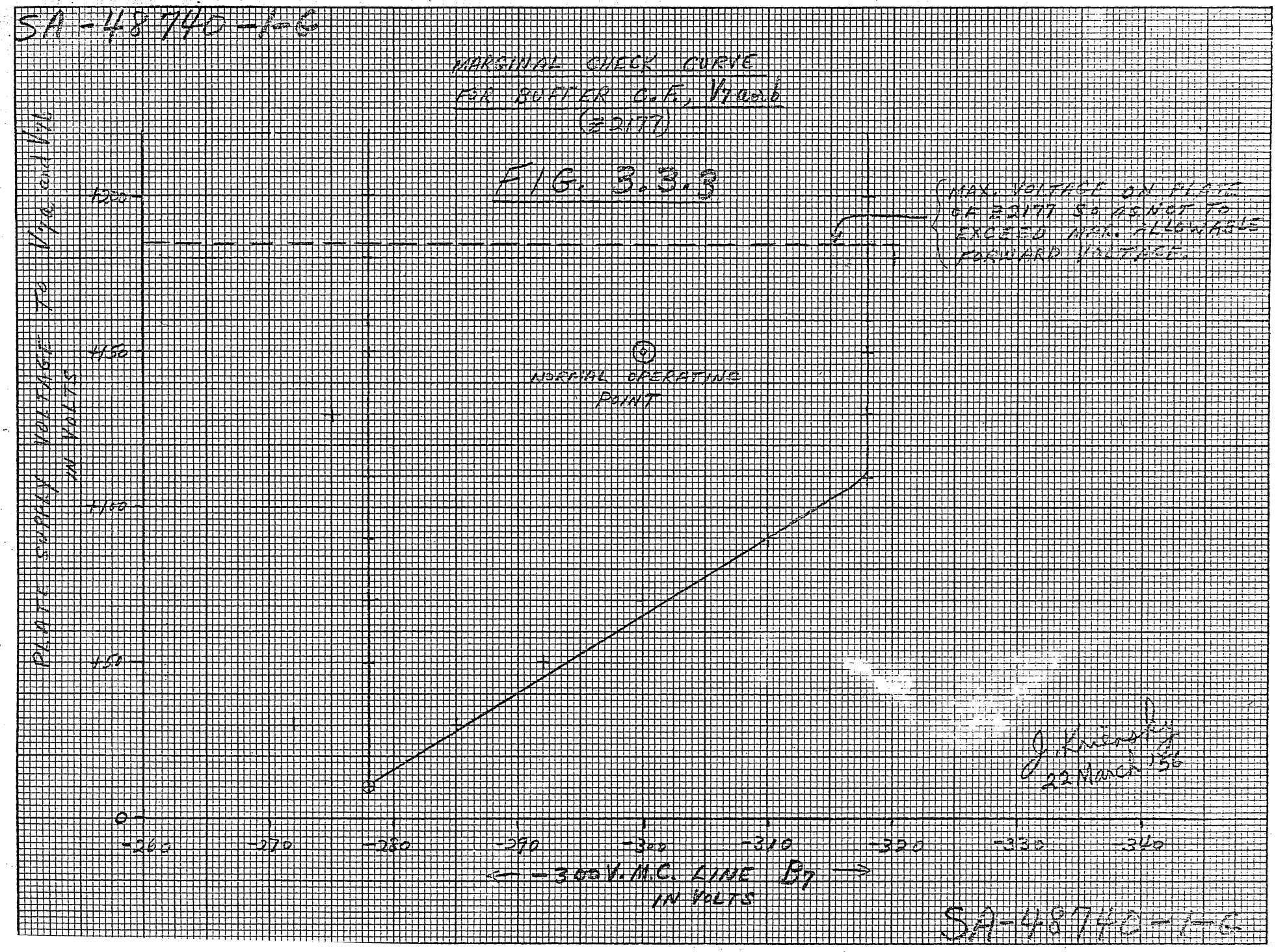
EQ. 3.3.1, 3.3.2

SB-48743-F6

SA-4877/D-1-C

MARGINAL CHECK CURVE
FOR BUFFER C.F., V1 and 6
(≅ 22177)

FIG. 3.3.3



SA-61708

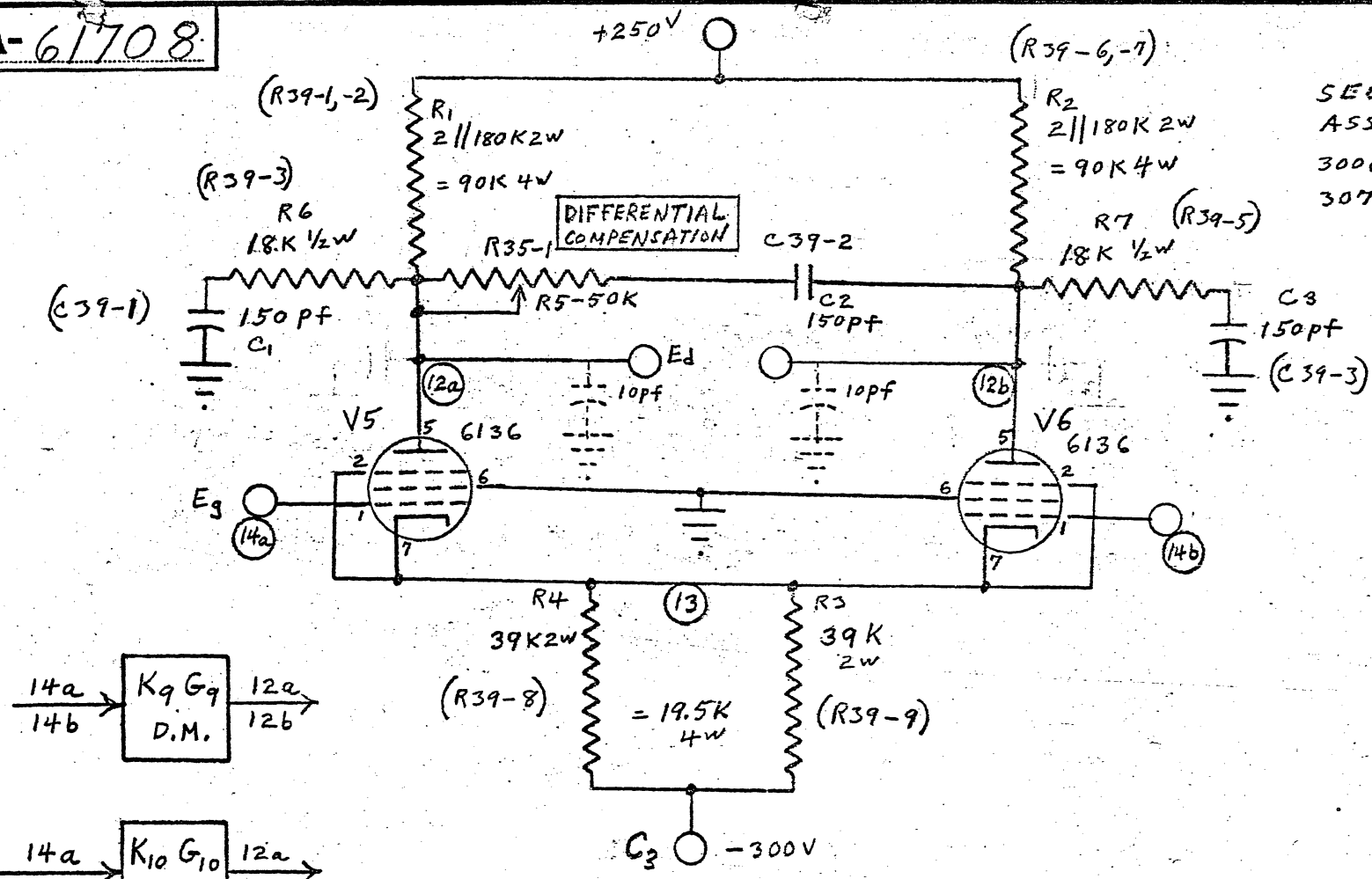


FIGURE 3.4.1

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3		13/4/56	HE Z
-2		7/2/56	HE Z
-1		24/10/55	HE Z

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
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DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO.

DIFFERENTIAL AMPLIFIER

SCALE:

DR. H E Zieman

ENG. H E Zieman

CK.

APPD.

SA-61708

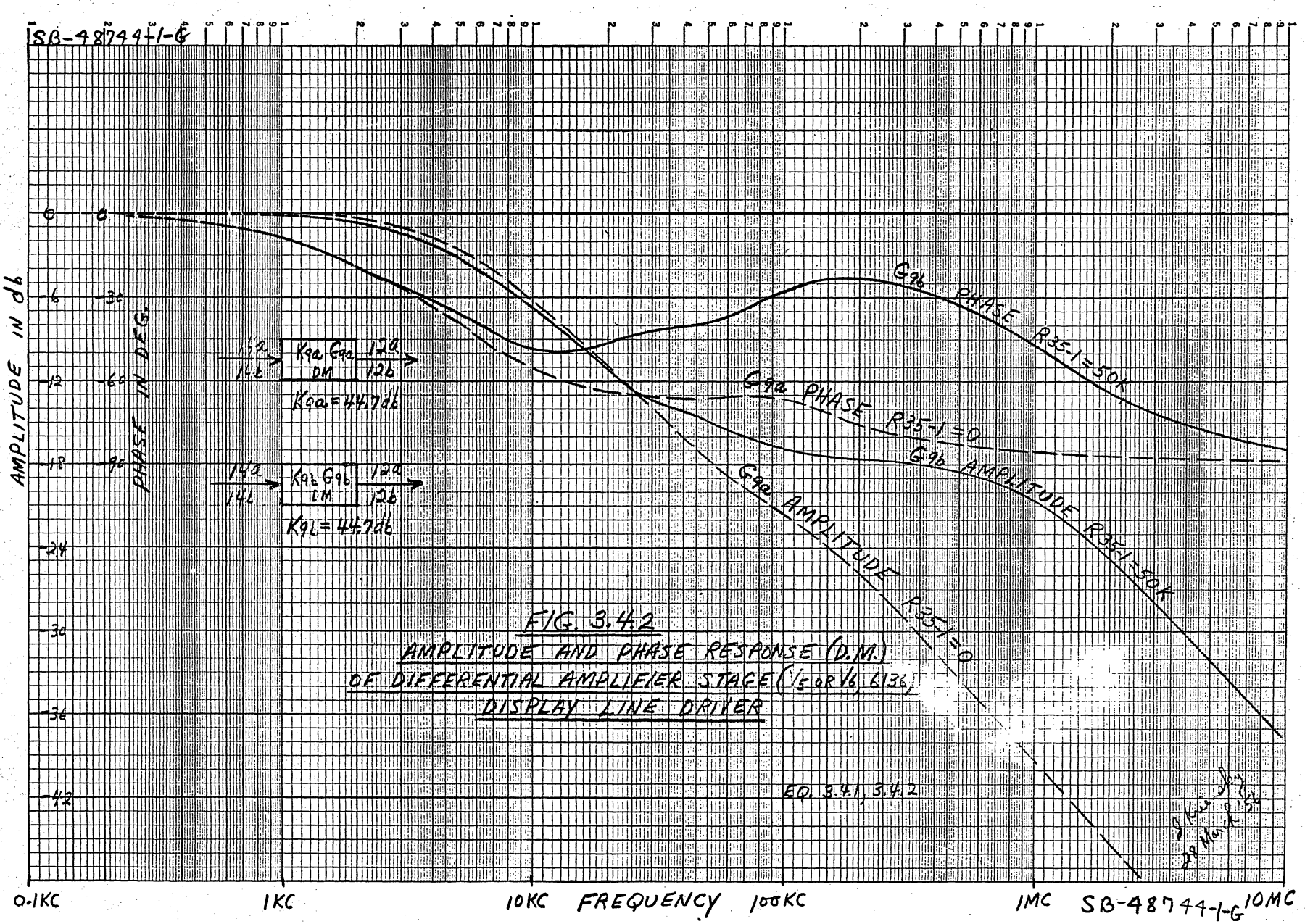


FIG. 3.4.2
AMPLITUDE AND PHASE RESPONSE (D.M.)
OF DIFFERENTIAL AMPLIFIER STAGE (½ OR V6, 6136)
DISPLAY LINE DRIVER

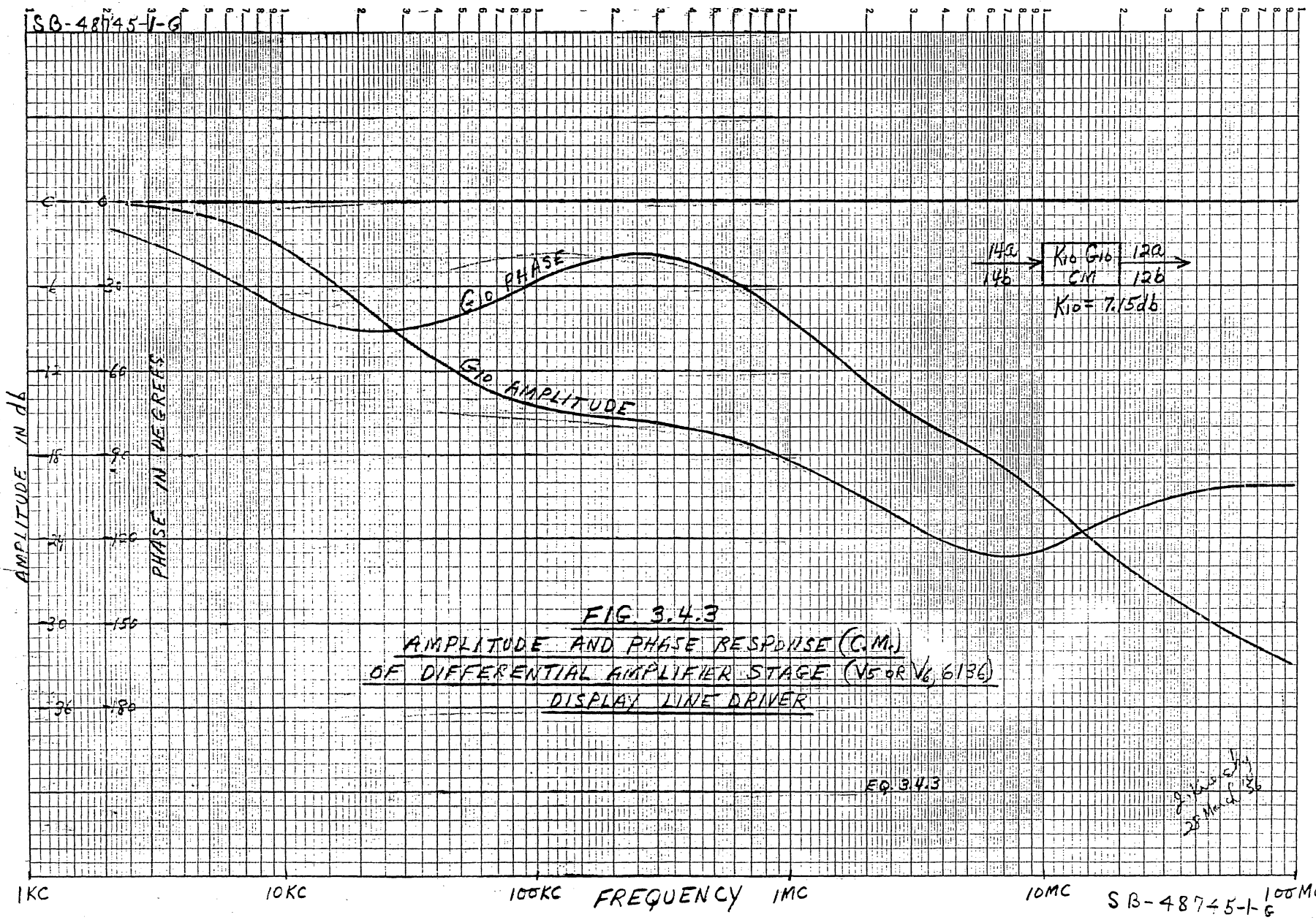
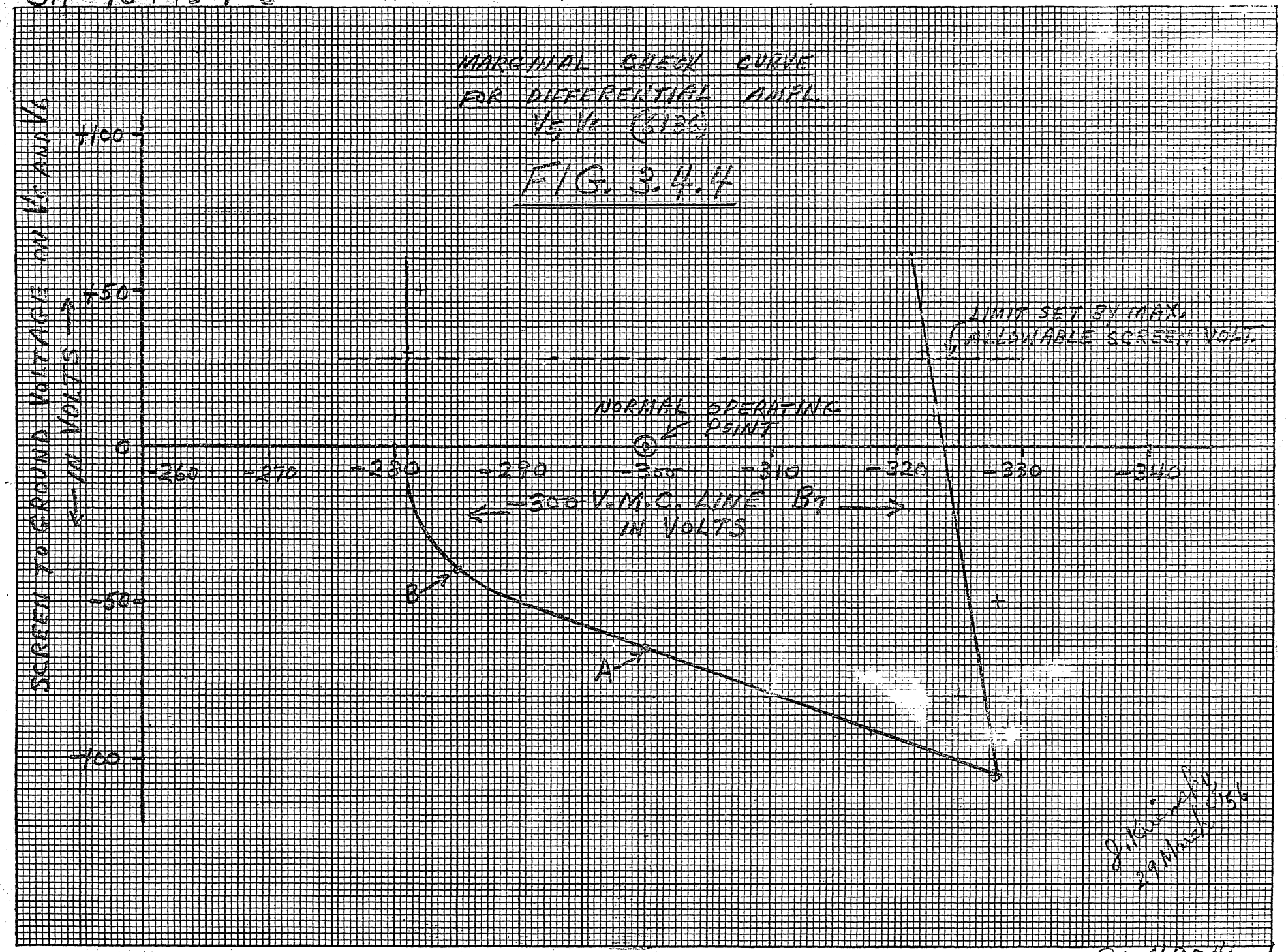


FIG. 3.4.3

AMPLITUDE AND PHASE RESPONSE (C.M.)
OF DIFFERENTIAL AMPLIFIER STAGE (V5 OR V6, 6136)
DISPLAY LINE DRIVER

EQ. 3.4.3

SA-48746-1-C



SA-48746-1-G

SA- 61709

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY

PLATE LOAD CIRCUIT
ON CARD ASSEMBLIES
300 6880 (27,30)
307 0187 (35)

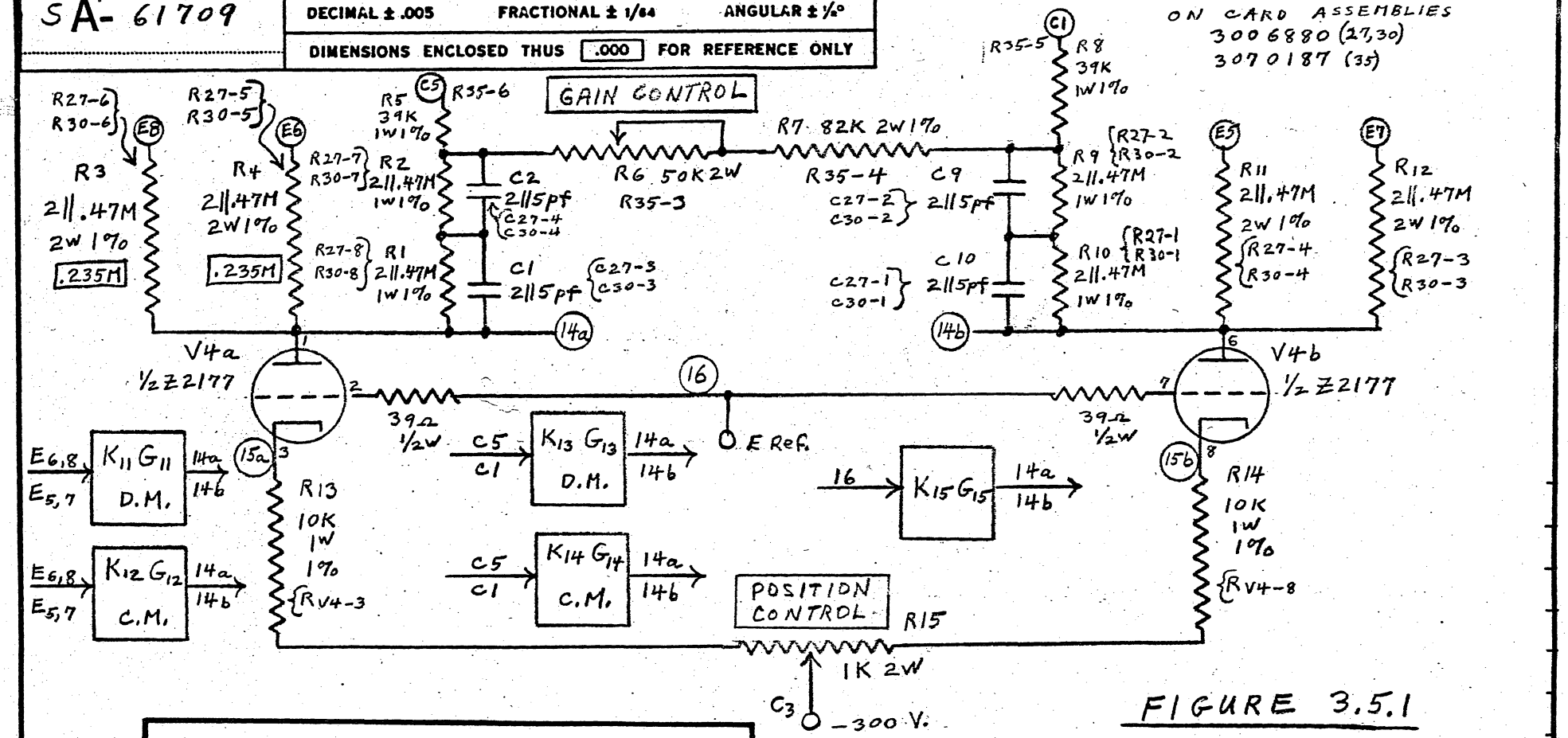


FIGURE 3.5.1

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-3		13/4/55	HE Z
-2		7/2/56	HE Z
-1		25/10/55	HEZ

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

INPUT CIRCUIT TO DIFFERENTIAL AMPLIFIER

SCALE:	DR. HE Zieman	SA- 61709
ENG. HE Zieman	CK.	APPD.

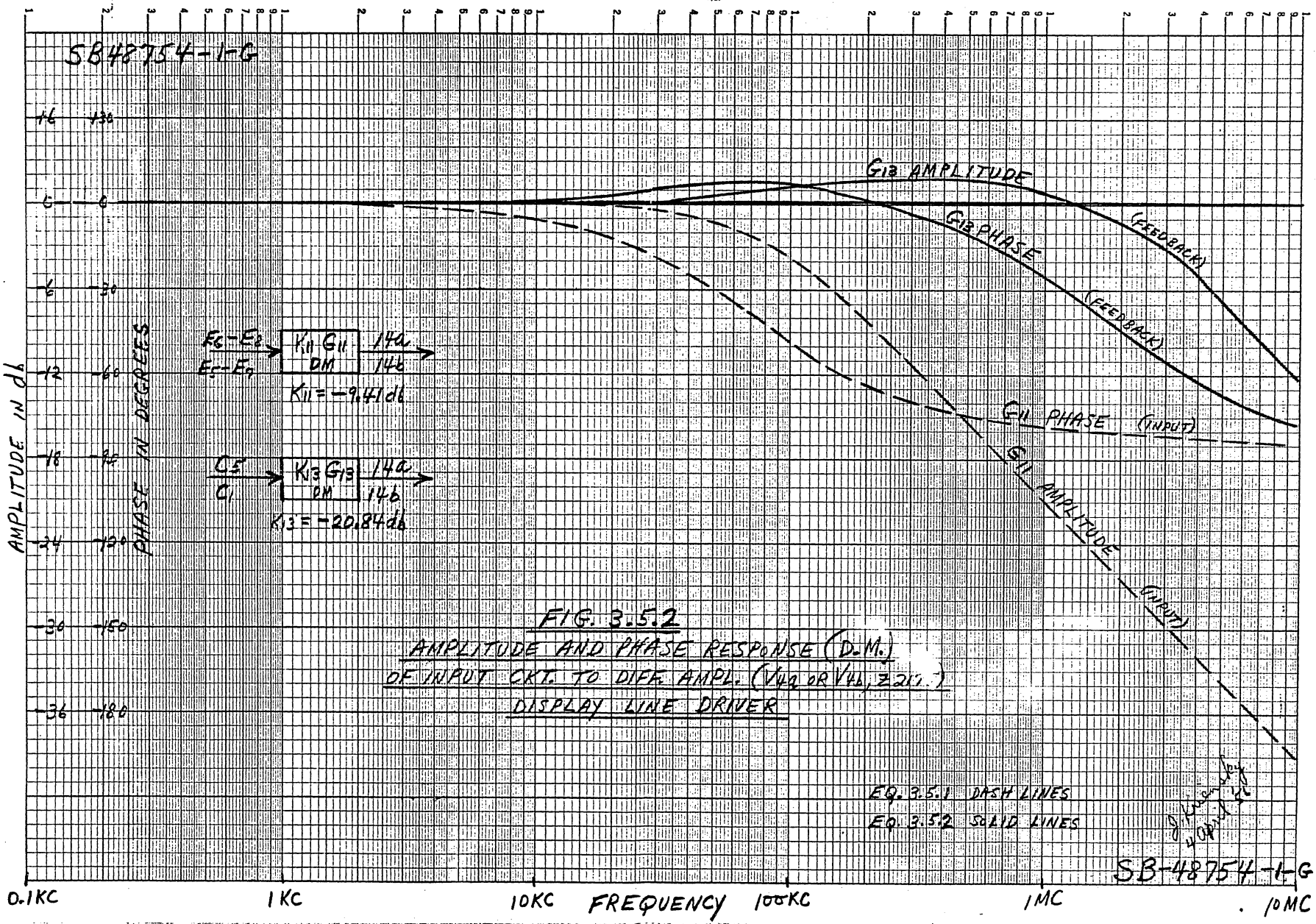


FIG. 3.5.2

AMPLITUDE AND PHASE RESPONSE (D.M.) OF INPUT CKT. TO DIFF. AMPL. (V_{4Q} OR V_{4L}, Z21) DISPLAY LINE DRIVER

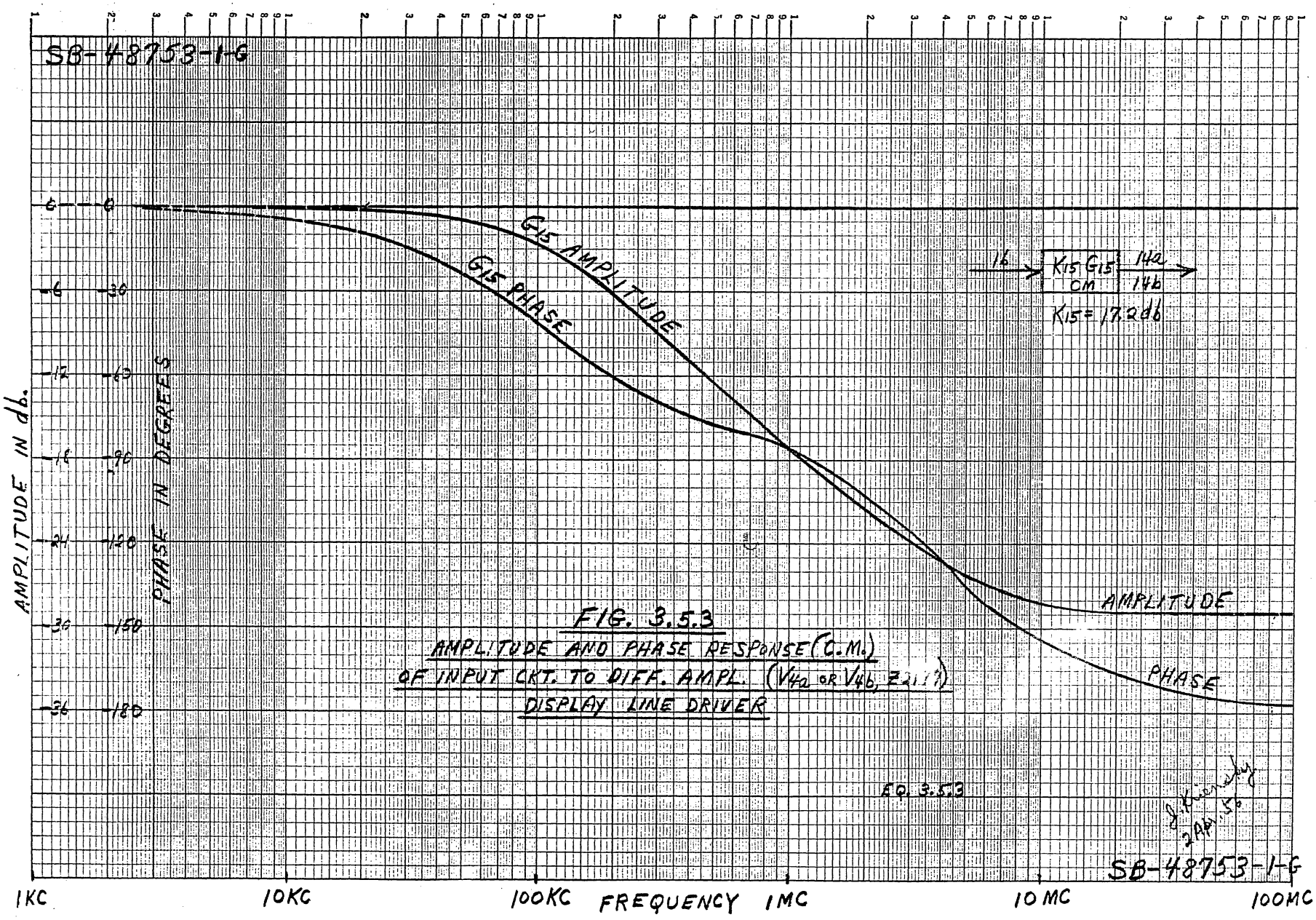


FIG. 3.5.3

AMPLITUDE AND PHASE RESPONSE (C.M.) OF INPUT CKT. TO DIFF. AMPL. (V_{14a} OR V_{14b}, Z21) DISPLAY LINE DRIVER

EQ. 3.5.3

2 APR 58

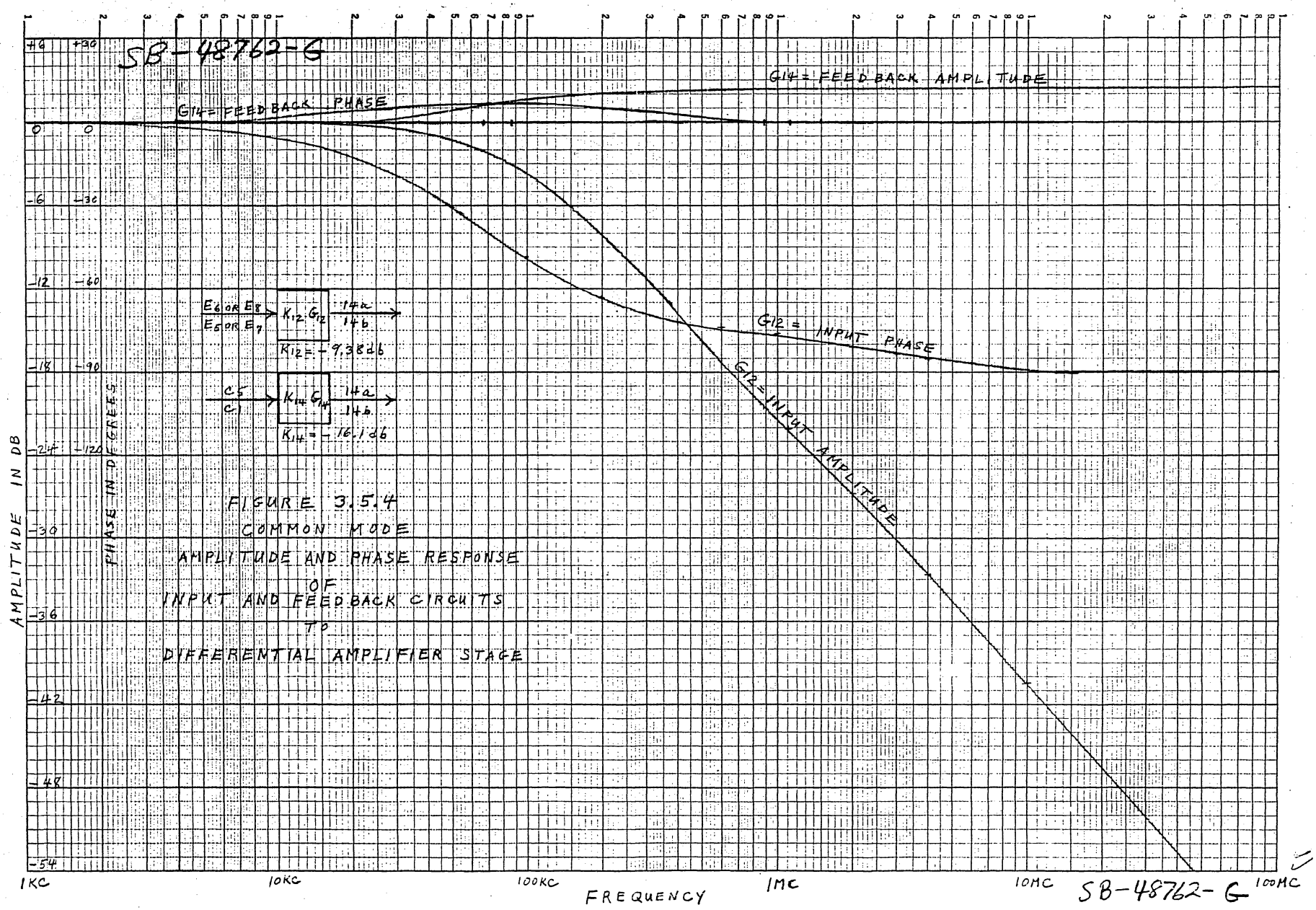


FIGURE 3.5.4
COMMON MODE
AMPLITUDE AND PHASE RESPONSE
OF
INPUT AND FEEDBACK CIRCUITS
TO
DIFFERENTIAL AMPLIFIER STAGE

SB-48762-G

MARGINAL CHECK CURVE #1
FOR INPUT CKT. TO DIFF. AMPL. (V_{in2} or V_{in1})

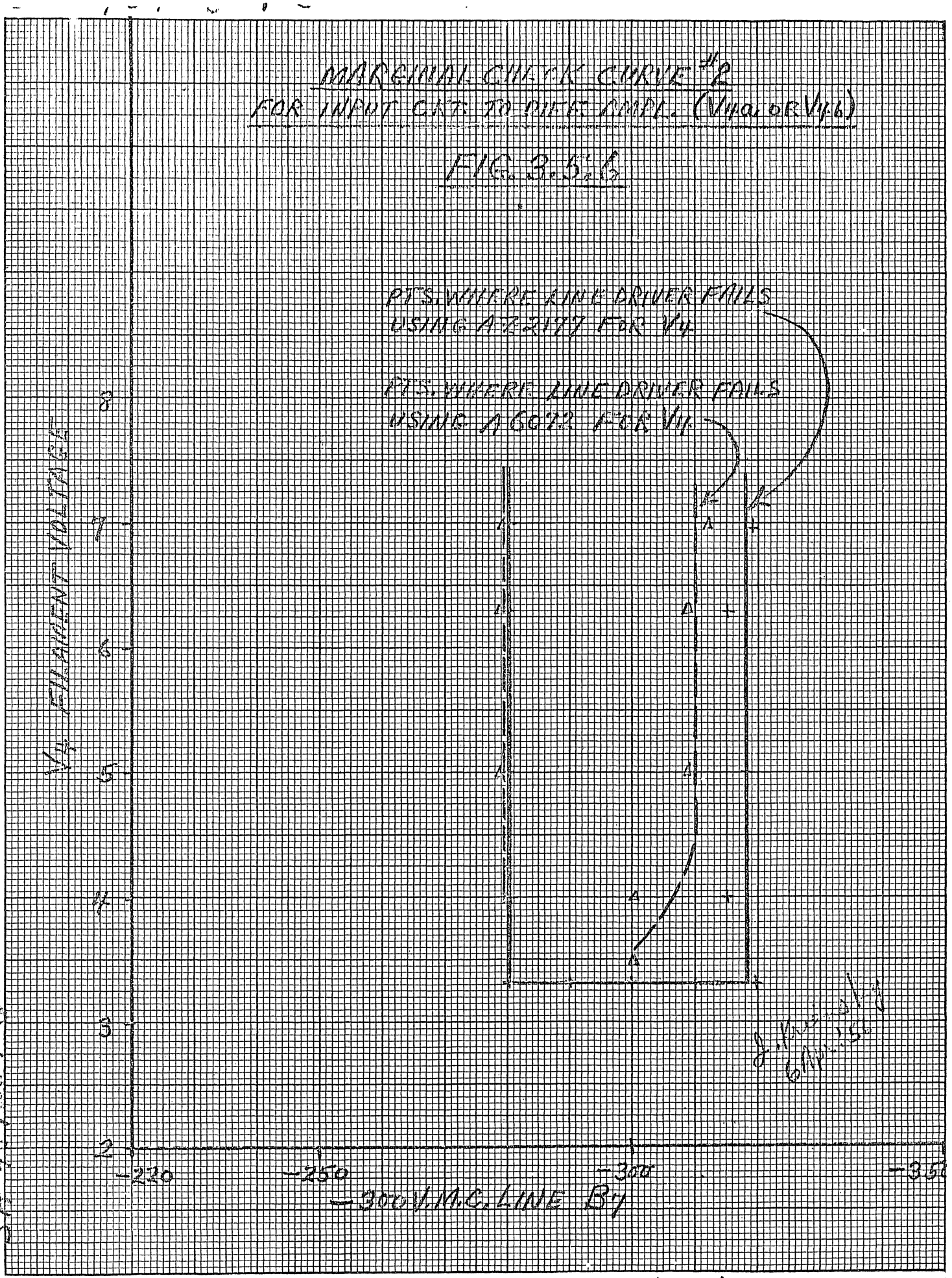
FIG. 3.5.5

SA-4873-2-G

SA-4873-2-G

MARGINAL CHECK CURVE #2
FOR INPUT CKT. TO PIER AMPL. (V_{in} or V_{ik})

FIG. 3.5.6



SA-48738-1-G

SA-61710

SEE CARD ASSEMBLY
300 6870
SLOT 19

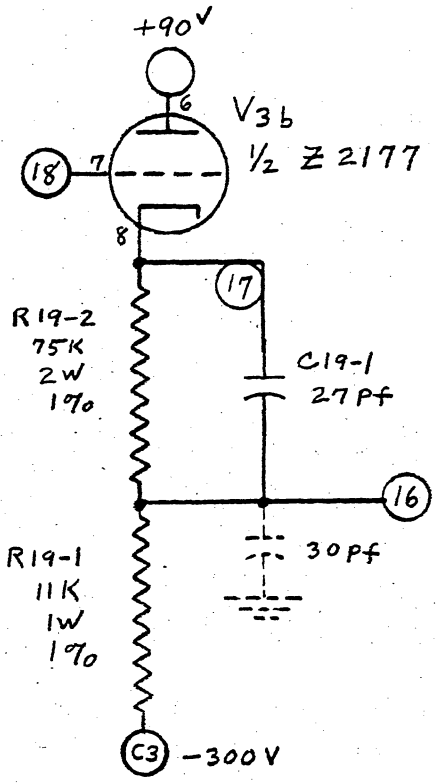


FIGURE 3.6.1

CHG.	APPD.	DATE	CN#
10			
9			
8			
7			
6			
5			
4			
3	HEZ	13/4/56	
2	HEZ	7/2/56	
1	HEZ	24/10/55	

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REFERENCE DRIVER

SCALE:	DR. HE Zieman	SA-61710
ENG. HE Zieman	CK.	APPD.

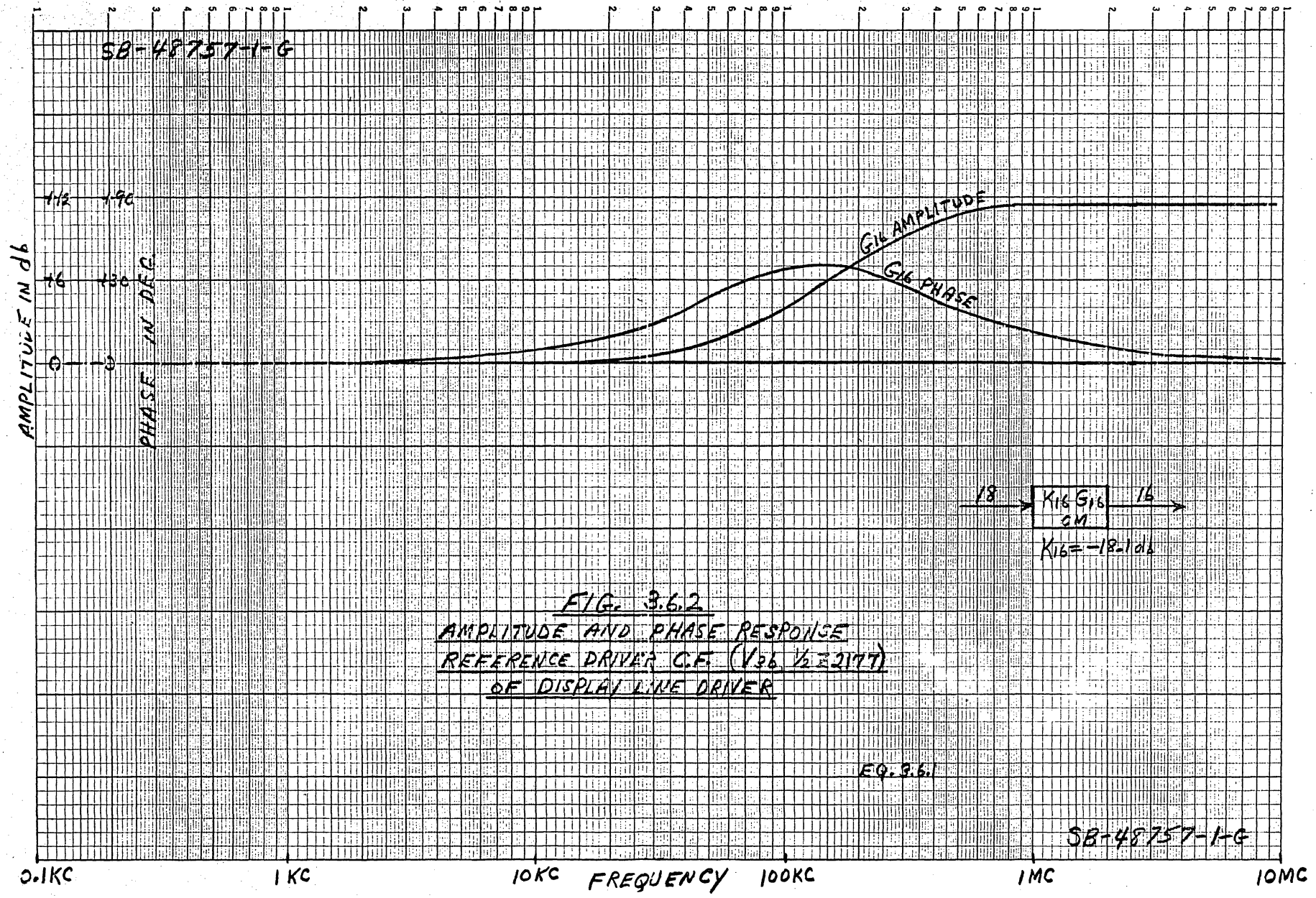


FIG. 3.6.2
AMPLITUDE AND PHASE RESPONCE
REFERENCE DRIVER C.F. (V36 ½ E2177)
OF DISPLAY LINE DRIVER

SA-48735-G

MARGINAL CHECK CURVE FOR REFERENCE DRIVER C.F. V36 (½ Z2177)

MAX. VOLTAGE ON PLATE OF Z2177 (V36) SO AS NOT TO EXCEED MAX. ALLOWABLE FORWARD VOLTAGE OF 200 V.

NORMAL OPERATING POINT

PLATE VOLTAGE ON V36 → IN VOLTS

+100
+50
0
-50
-100

-260 -270 -280 -290 -300 -310 -320 -330 -340

← -300 MC LINE B1 → IN VOLTS

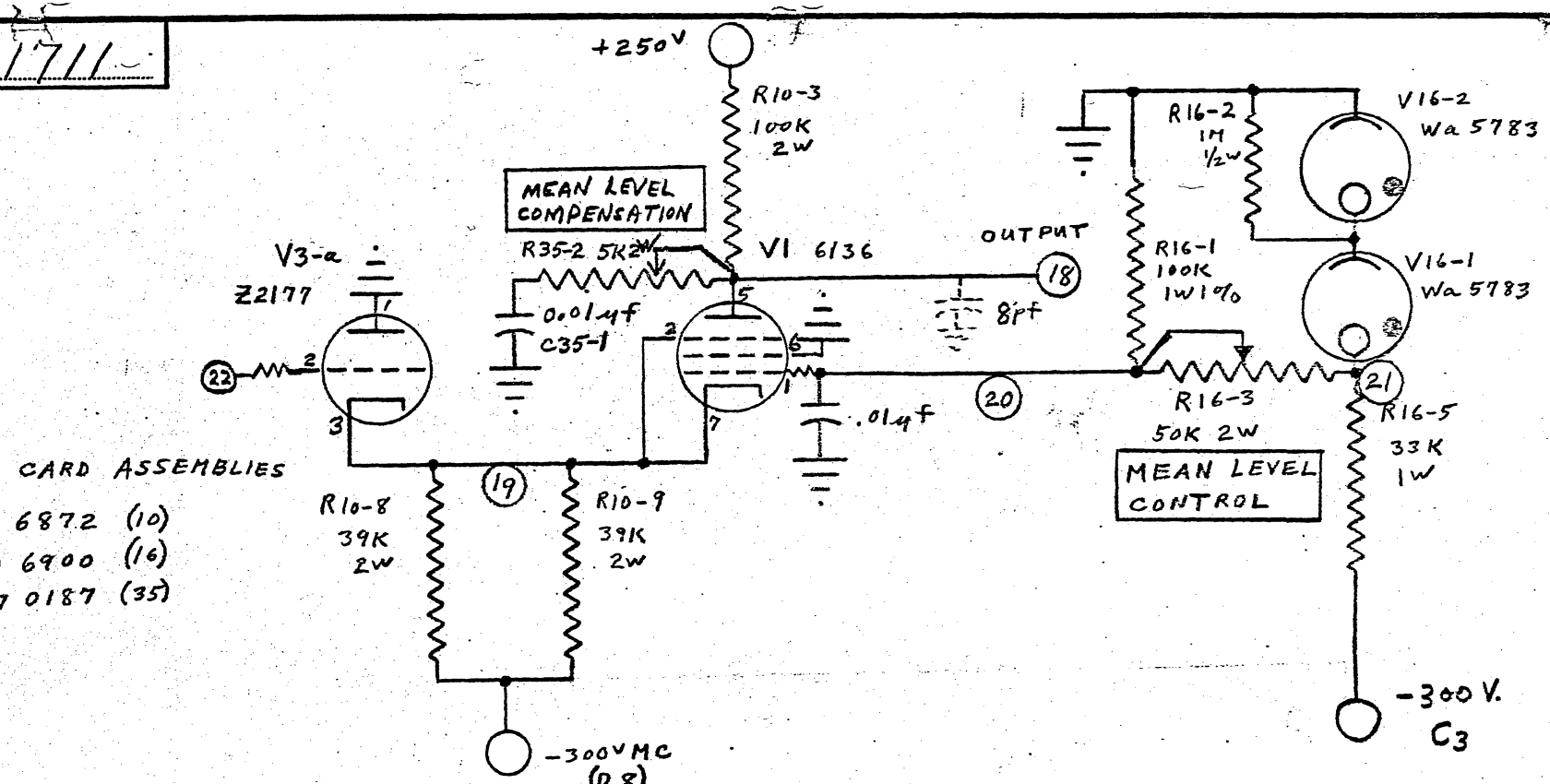
A

B

FIG. 9.6.3

SA-48735-G

SA-61711



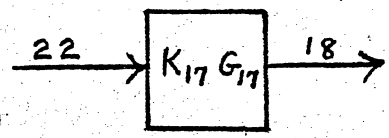


FIGURE 3.7.1

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3		13/4/56	HE Z
-2		7/2/56	HE 2
-1		24/10/57	[illegible]

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO.

REFERENCE AMPLIFIER

SCALE:	DR. H E Ziman	
ENG. H E Ziman	CK.	APPD.

SA-61711

V

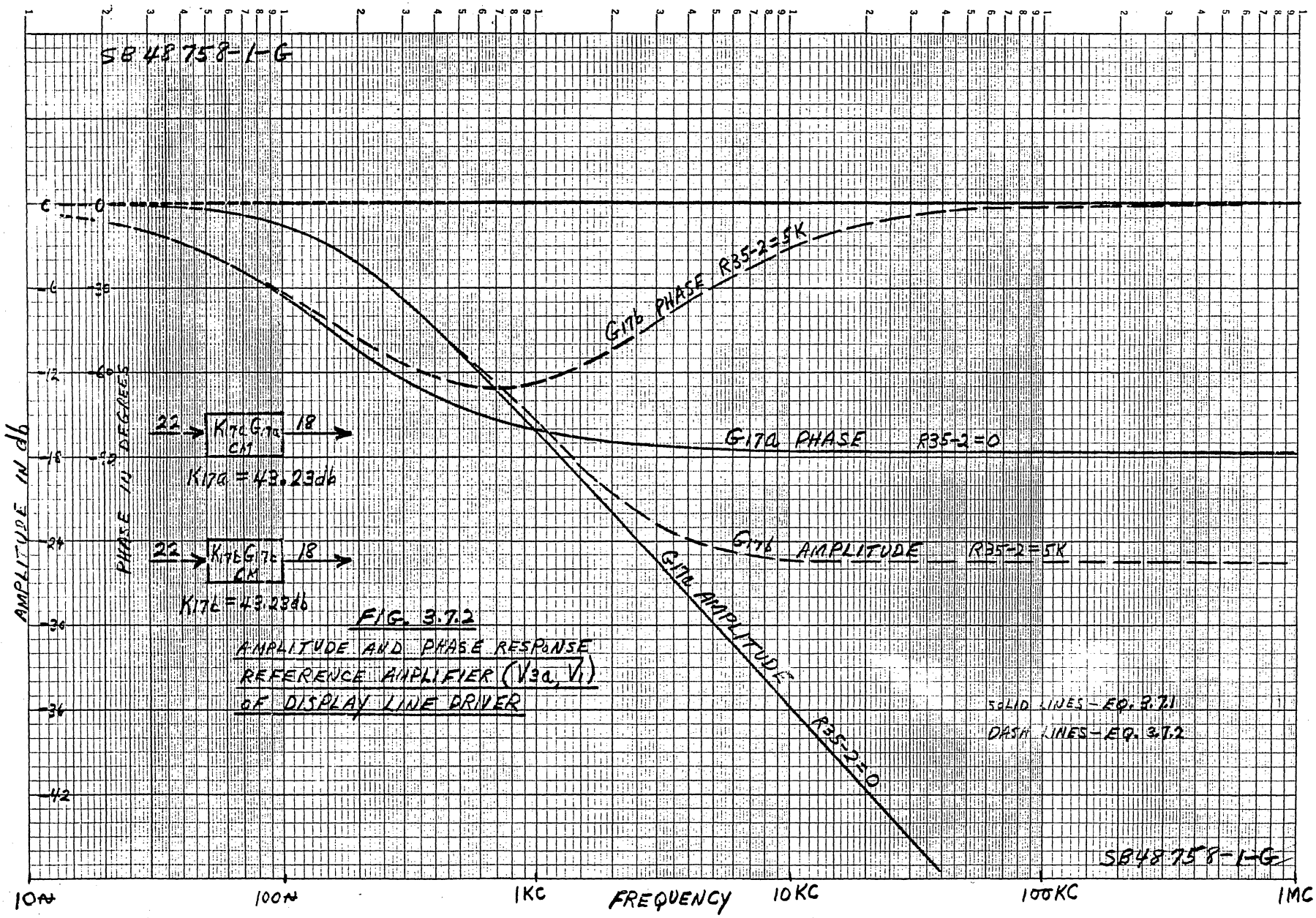
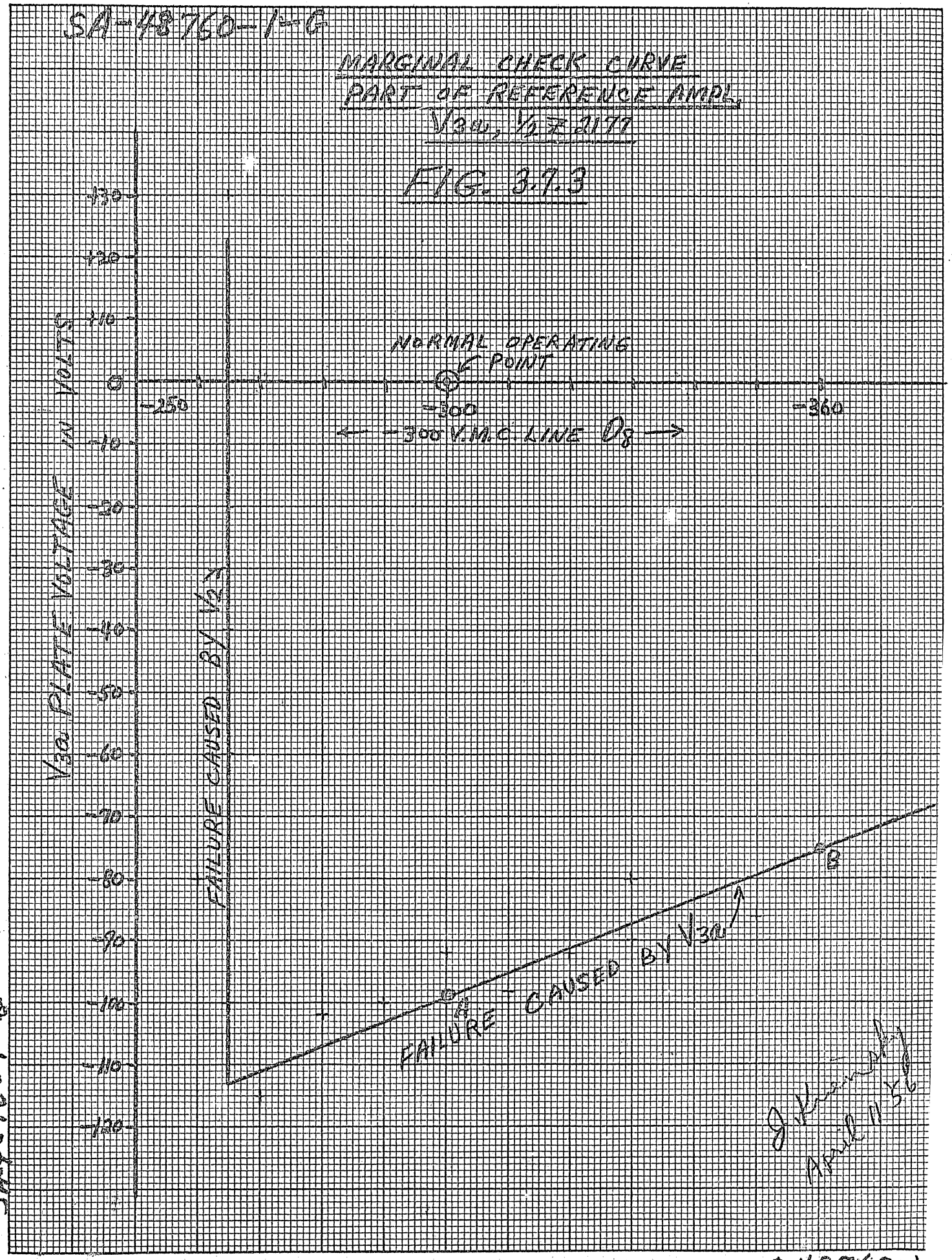


FIG. 3.7.2
AMPLITUDE AND PHASE RESPONSE
REFERENCE AMPLIFIER (V_{3a}, V_1)
OF DISPLAY LINE DRIVER

SA-48760-1-G

MARGINAL CHECK CURVE
PART OF REFERENCE AMPL.
V_{30}, $V_{\frac{1}{2}}$ #2177

FIG. 3.7.3



SA-48760-1-G

SA 48760-1

SA-65906

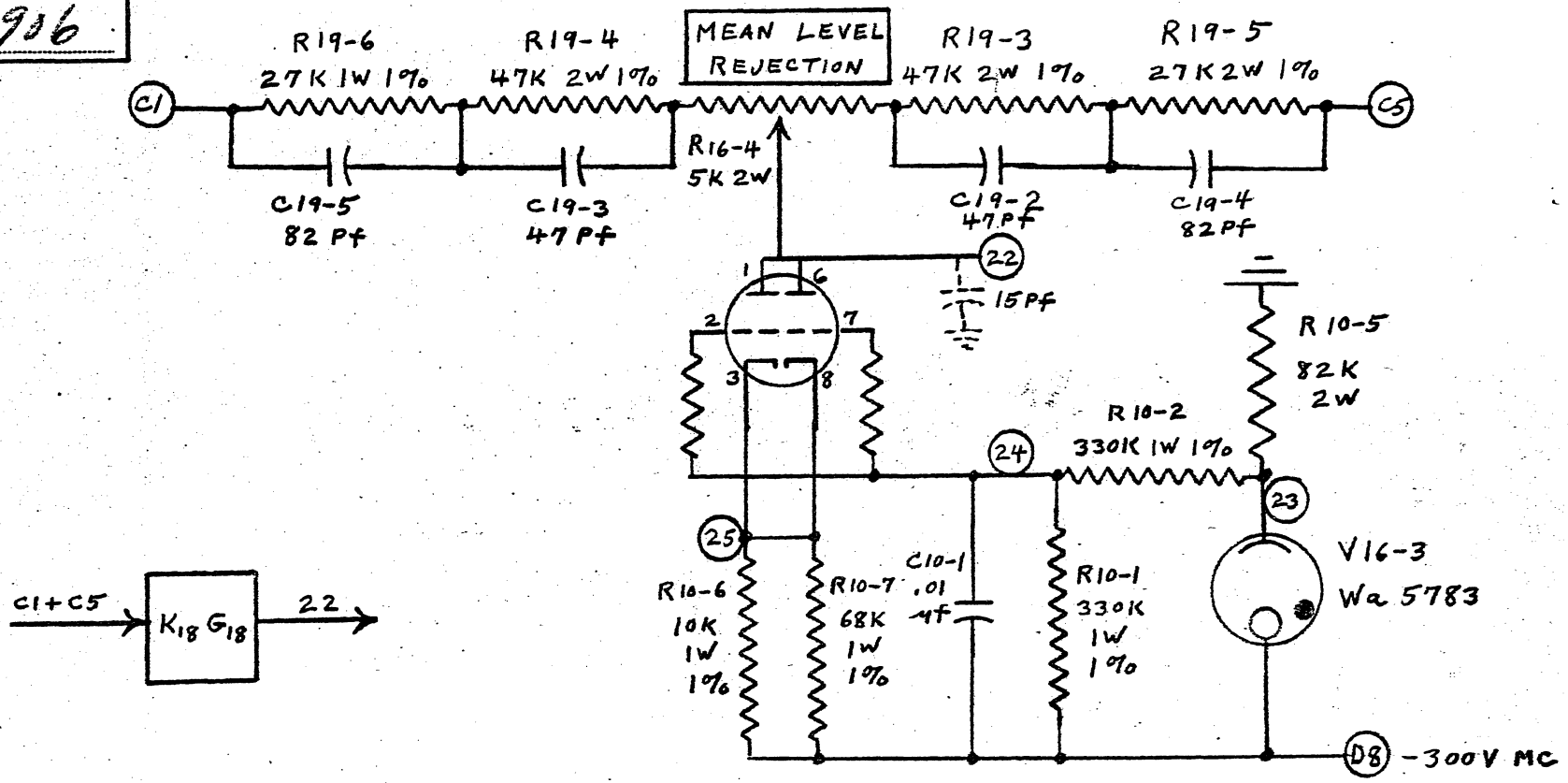


FIGURE 3.8.1

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2			
-1			

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INPUT CIRCUIT TO REFERENCE AMPLIFIER

SCALE:	DR. H E Ziemer	SA-65906
ENG. H E Ziemer	CK.	APPD.

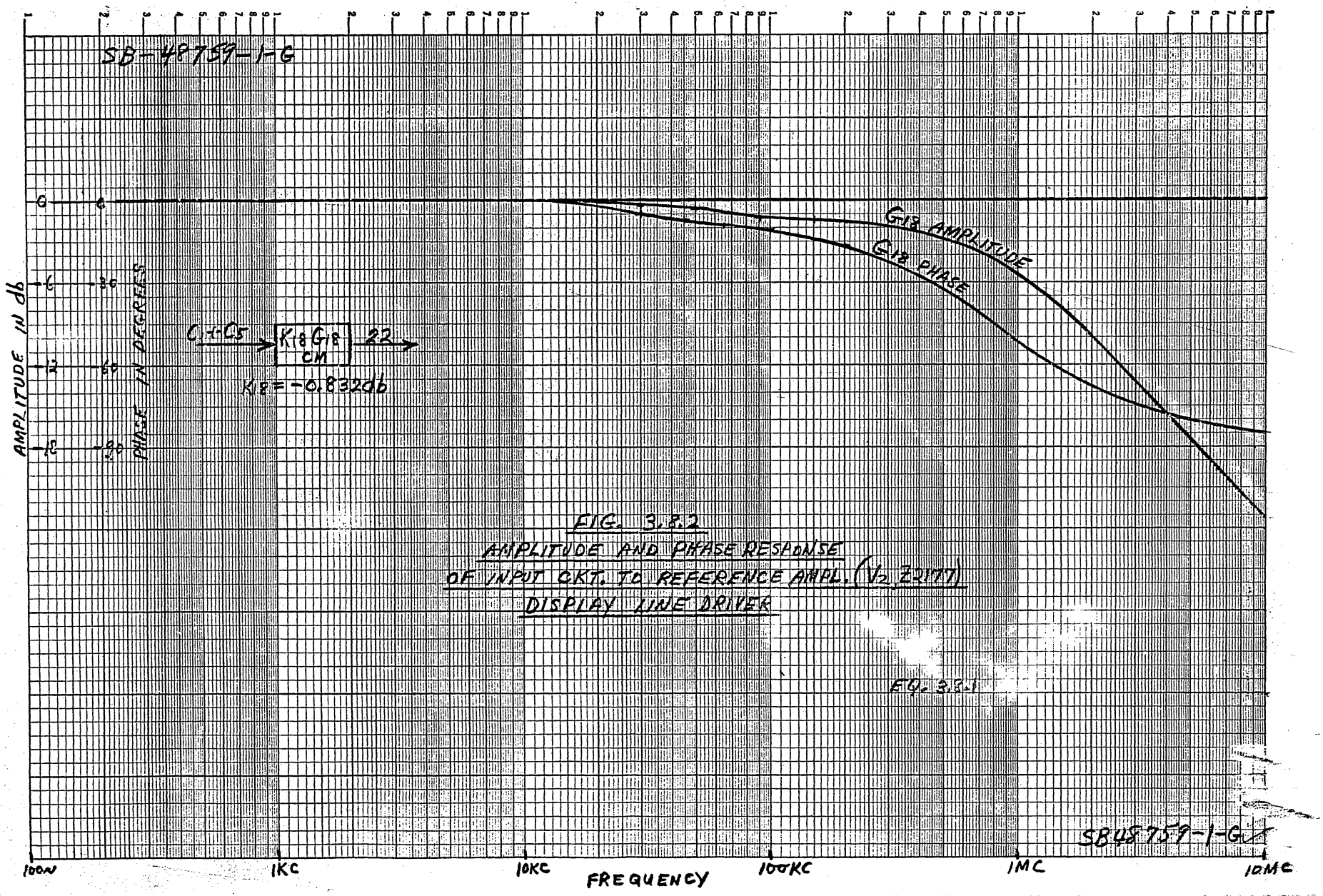
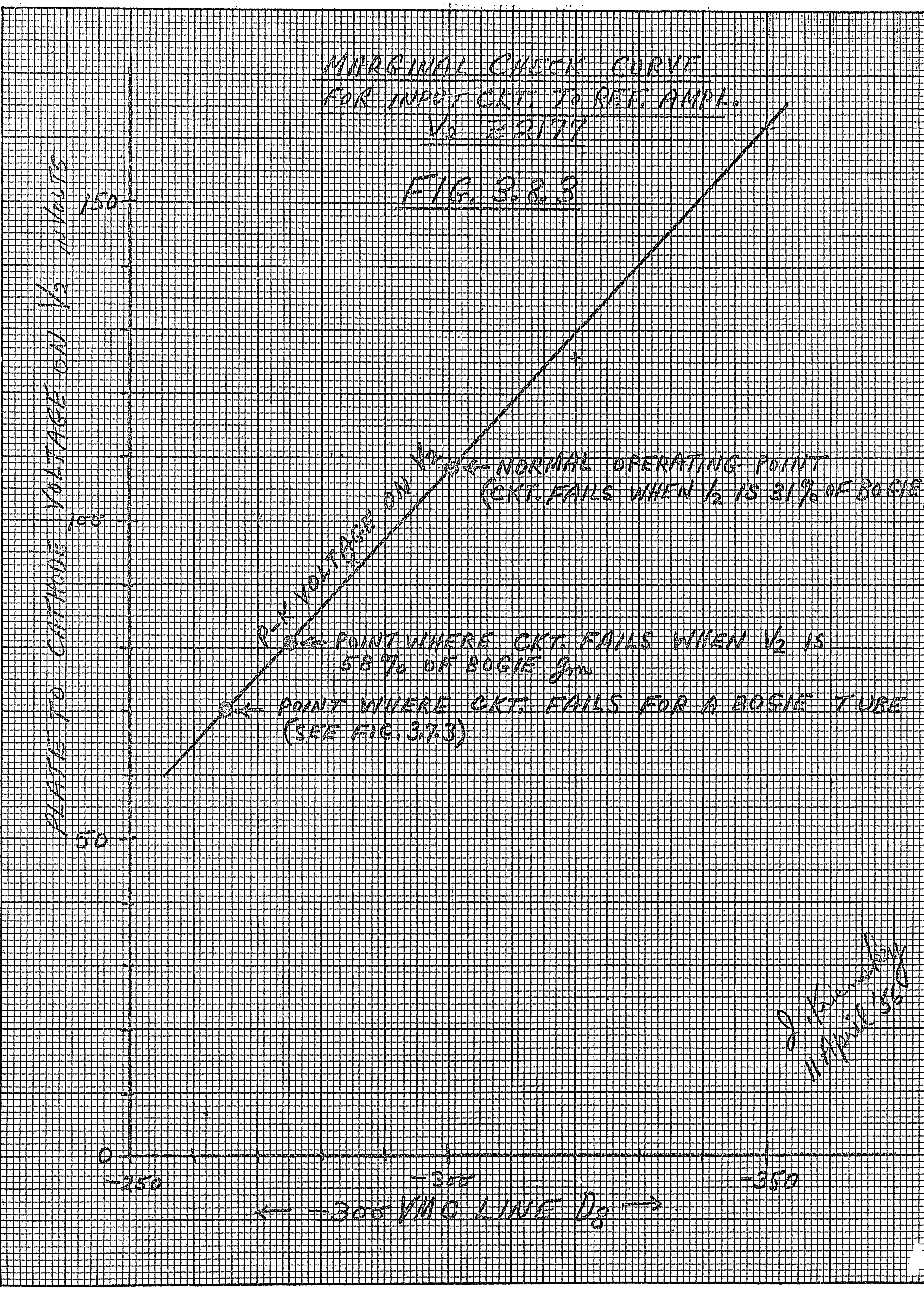


FIG. 3.8.2

AMPLITUDE AND PHASE RESPONSE OF INPUT CKT. TO REFERENCE AMPL. (V_2, Z2177) DISPLAY LINE DRIVER

Eq. 3.8-1

SA-48761-G



SA-48.76-1-G