Digital Computer Laboratory
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Subject: BLOCK DIAGRAMS: MEMORY ADDRESS REGISTER AND MEMORY BUFFER REGISTER

To: R. A. Nelson, N. H. Taylor, and Group 62 Section Heads

From: R. P. Mayer and W. N. Papian

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This note is intended to satisfy item I (General Description of Function Needed) of the WWII time schedule on these subjects.

The magnetic-core memory system for WWII involves the use of a memory address register (for specifying the memory register to be used) and a memory buffer register (for handling the number being inserted or removed from the specified memory register).

The primary function of this set of registers is to provide a unified memory control system which converts between the standard pulses used in the main sections of the computer and the special control signals necessary for proper operation of the memory cores. The memory buffer register also provides for parity counting and parity checking.

These registers include the register flip-flops, any necessary read-in, read-out, and check gate tubes, any timing and control equipment which is not considered part of central control, and any equipment necessary to connect the flip-flops to the circuits which are considered part of the memory system (see M-1964 and M-1965). In general, on any memory cycle, both these registers must supply signals to the remainder of the memory system until the end of the write part of the cycle.

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