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ELECTRICAL ENGINEERING DEPARTMENT

MASTER'S THESIS PROPOSAL

TITLE: A Binary Adder Using Magnetic-Core Flip-Flops

BRIEF STATEMENT OF THE PROBLEM

This thesis will consist of two parts: first, an investigation of a circuit similar to an electronic flip-flop; and second, a study of the possibility and practicability of using this circuit in a binary adder.

HISTORY OF THE PROBLEM UP TO THE PRESENT TIME

Almost from the beginning of electronic digital computers, the poor reliability of electronic tubes has caused trouble. The recently developed magnetic materials with almost rectangular hysteresis loops offer the possibility of replacing tubes that are used as two-valued elements (i.e., elements which at all times are in one of two stable states). If a magnetic core is used in an application where it is always kept (except for the brief time of switching) at one or the other of the extremes of its hysteresis loop (at plus or minus b_r), it can be thought of as a two-valued element. Throughout this paper, it is assumed that the cores are used in this way.

Cores are available which can be switched from one state to the other in a time comparable to the switching time of a tube and which seem to be practically indestructible under all conditions of computer operation. However, for the following reasons they are not as convenient as tubes in most applications:

a. In order to determine the state of a core, i.e., to determine the information it holds, the information must be destroyed. The state of a core can be determined only by applying a value of mmf sufficient to switch it to a particular extreme of its hysteresis loop. If it was already at that extreme, there is little change in flux, and hence little voltage is generated in a sensing winding on the core. On the other hand, if it was initially at the other extreme of its hysteresis loop, a large change of flux results and a large voltage is developed in the sensing winding. Therefore, if the information is not to be lost in the process, it must be temporarily stored and replaced or else permanently transferred to another core.

b. Signal energy is lost in a core when it is switched.

c. Circuits involving magnetic cores do not inherently have the isolating property of tubes which prevents backward flow of information. They can be made to have this property, but at the price of added components and increased losses in the circuit.

That magnetic cores can be used in digital computer logical circuits has been shown by M. K. Haynes in a thesis at the University of Illinois.[1] The circuits investigated by Mr. Haynes, however, were for serial-type computers and were very slow compared to a parallel computer such as Whirlwind I. The investigations in this thesis will be directed toward an arithmetic element for a parallel computer.

A very important component of electronic parallel digital computers is the electronic flip-flop. This is a device which has two stable states of operation (one of two tubes conducting). It can be set to either state or changed from its existing state to the other one (complemented) by the application of a single voltage pulse. A similar device which uses magnetic cores instead of tubes can be developed from a circuit which has been designed by D. A. Buck[2] (see Fig. 1). However, the state of the electronic flip-flop is continuously indicated by easily discernible voltage levels. Since this is not the case with this magnetic-core flip-flop, it cannot simply replace the electronic flip-flop in most applications.

A circuit has been qualitatively designed which is similar to the adder used in Whirlwind I and which is adapted to the use of the above-mentioned magnetic-core flip-flops (see Fig. 2). It is believed that this design can be improved or perhaps replaced by a better logical circuit which will still use the new flip-flops. Also, this flip-flop shows promise of being useful in other applications than adders (for example, it can certainly be used in a counter).

The circuit designed by Buck was built and used by him in a test setup. It was found that the one built would not operate with a pulse repetition frequency (prf) greater than 109 kc, and that the ratio of a signal pulse from a core containing information to the pulse from a core containing no information (called "signal-to-noise ratio") was not satisfactory for some applications.

OPERATION OF THE MAGNETIC-CORE FLIP-FLOP

A magnetic core inherently has two of the above-mentioned properties of electronic flip-flops; that is, it can be used, as described on page 1, in such a manner that it has two stable remanent states and can be set to either of them. However, a core cannot be complemented, and this is the main problem in designing a magnetic-core flip-flop.

Reduced to general terms, it can be said that an electronic flip-flop is complemented as follows. Initially, one of the two tubes is conducting and the other is cut off. In order to complement the flip-flop, a

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1. Haynes, M. K., Magnetic Cores as Elements of Digital Computing Machines, Technical Report to the Office of Naval Research, Contract N6ori71, Task Order XXIV, Project ONR NR 048 094, August 28, 1950.

2. Buck, D. A., Binary Counting with Magnetic Cores, Engineering Note E-438, Digital Computer Laboratory, M. I. T., December 6, 1951. Page 3.

short voltage pulse (0.1 microsecond in Whirlwind I) is applied so as to momentarily render both tubes unable to conduct. After the pulse is over, the circuit "remembers", by the relative charge on the two "crossover" capacitors, which tube had been conducting initially and causes the other tube to conduct.

The magnetic-core flip-flop of Fig. 1 has two main cores, labeled "A" and "B", and two auxiliary cores, labeled "C" and "D". Cores C and D serve the same purpose in this flip-flop as the "crossover" capacitors do in electronic flip-flops. The cores are coupled by circuits which contain rectifiers and resistors so arranged as to permit current flow only where it is desired during a particular operation (for example, it is often desirable for current to flow when a core is switched from one extreme of its hysteresis loop to the other, but not when it is switched from the second extreme to the first). One of the main cores is normally at an extreme of its hysteresis loop, plus ϕ_r, while the other main core is at minus ϕ_r. (In Fig. 1, the direction of plus ϕ_r is defined as upward). Cores C and D are normally at minus ϕ_r. In each of the following examples of operation let us assume that core A is initially at plus ϕ_r.

Case 1. Complementing. A current pulse on the complement winding (W-1), as indicated in Fig. 1, will cause a flux in an opposite direction to that of plus ϕ_r; hence, a voltage pulse will be obtained on the signal winding on core A (W-7). Also, a voltage will be developed across the coupling winding between cores A and C (W-2) of such a polarity as to switch core C to plus ϕ_r. A short time later, a current pulse is applied to a winding on core C (W-4), as shown in the diagram, and this switches core C back to minus ϕ_r. When this happens, current flows in the winding which couples cores C and B (W-3) in such a manner as to switch core B to plus ϕ_r. However, this switching from minus ϕ_r to plus ϕ_r does not produce a signal from core B because of the rectifier in the signal winding on core B (W-8).

It will be noted that the current pulse which switches core C back to minus ϕ_r is applied at the same time to a winding on core D. However, since that core is already at minus ϕ_r, the pulse has no effect. In the thesis work this pulse will probably be obtained, using a delay line and amplifier, from the first pulse, but in a computer it would probably be supplied by a separate clock-pulse generator.

To summarize the description of complementing: (1) the state of the circuit has been changed from the original condition of core A at plus ϕ_r and core B at minus ϕ_r to the condition of core B at plus ϕ_r and core A at minus ϕ_r (cores C and D are the same as they were initially); and (2) a signal has been obtained from core A. In other words, the circuit has been complemented and a signal has been obtained that indicates which core was initially at plus ϕ_r. Similarly, the next current pulse on W-1 will restore the circuit to its original condition and produce a signal from core B. The process can be repeated indefinitely.

Case 2. Write ONE. In order to define the conditions of this flip-flop in a convenient manner for what follows, let us make the following

definitions:

1. When core A is at plus $\hat{b}_r$, the flip-flop is "set to ONE."

2. When core B is at plus $\hat{b}_r$, the flip-flop is "set to ZERO" or, alternatively, "cleared."

To set the flip-flop to ONE, a current pulse must be applied to the "Write ONE" winding (W-9), which, it will be noted, is located on core B. If the circuit is already set to ONE, then core B is at minus $\hat{b}_r$ and the current pulse will not tend to switch the core. Hence, no significant voltage pulse will be generated, and the circuit will remain set to ONE. However, if the circuit is initially set to ZERO then the current pulse will switch core B to minus $\hat{b}_r$, a voltage pulse will be generated in the signal winding on core B, and a voltage will be generated in W-5 which will switch core D to plus $\hat{b}_r$. A short time later a current pulse is applied on W-4. This switches core D back to minus $\hat{b}_r$ and causes core A to be switched to plus $\hat{b}_r$. Thus, the circuit has been set to ONE and, if it was initially set to ZERO, a signal has been obtained from core B.

Case 3. Clear. To clear (i.e., set to ZERO), the process is just the reverse of Case 2. The "Clear" pulse is applied to the "Clear" winding (W-10) and, regardless of the initial state of the circuit, the sequence ends with core B at plus $\hat{b}_r$ and core A at minus $\hat{b}_r$. If the circuit was initially cleared, then no signal is obtained, but if it was initially set to ONE, then a voltage pulse is obtained from core A.

Summary of Properties of Magnetic-Core Flip-flop. As has been noted, this circuit can be set to either of two states and can be complemented. From the point of view of computer logical circuit design, the properties of the circuit can be thought of as follows (see Fig. 1-b):

1. If the circuit is at ONE, then a pulse applied to either the "Complement" or the "Clear" winding will result in a voltage pulse from core A and will set the circuit to ZERO. A pulse applied to the "Write ONE" winding will result in no change.

2. If the circuit is at ZERO, then a pulse applied to either the "Complement" or the "Write ONE" winding will result in a voltage pulse from core B and will set the circuit to ONE. A pulse applied to the "Clear" winding will result in no change.

OPERATION OF THE BINARY ADDER OF FIG. 2

This adder uses the same basic property of binary addition that the Whirlwind I adder uses. This property can be described in the following way. Consider two binary numbers, each of k digits, which are to be added. The least significant digit is the first digit, the second least significant is the second, the n^{th} least significant is the n^{th}. To add the two numbers, first add the corresponding digits of each number. Then consider the less significant digit in each result to be the partial sum and the more significant digit to be the carry, as shown in Table 1, page 5. The final sum can now be obtained from the partial sums and carries by the following rule:

The final sum in the m^{th} column is the complement of the partial sum in that column if the carry in the m^{th} column is ONE and the partial sums in all the columns between the m^{th} and the n^{th} are ONES for some value of m that is greater than zero and less than n_{th}. If this condition cannot be fulfilled, then the final sum in the n^{th} column is the same as the partial sum in that column.

Table 1

	5th Digit Column		4th Digit Column		3rd Digit Column		2nd Digit Column		1st Digit Column	
1st number	1		1		0		1		1	
2nd number	1		0		1		0		1	
	1	0	0	1	0	1	0	1	1	0
	Carry	Partial Sum	Carry	Partial Sum	Carry	Partial Sum	Carry	Partial Sum	Carry	Partial Sum
Final Sum	1	1		0		0		0		0

In the example given, this can be observed to be true. Also, it will be noted that the final sum may have one digit more than either of the numbers added. Therefore, the above rule applies for $0 < n \leq (k+1)$, and the partial sum in the $(k+1)^{th}$ column is always ZERO.

In the binary adder shown in Fig. 2, the digits of the two numbers to be added will be represented by current pulses for ONES, no pulses for ZEROS. Initially, all flip-flops are set to ZERO and all the carry cores (labeled C) are at minus δ_r.

First, the digits of the first number are applied to the corresponding input lines (all are applied simultaneously). The input lines correspond to the complement lines of the flip-flops (see Fig. 1). Next, the digits of the second number are applied. Now if both digits applied to any input were ONES, then the flip-flop associated with that input will have been switched from ZERO to ONE and back to ZERO. The switching from ONE to ZERO causes an output pulse on the ONE line from the flip-flop, and this pulse will switch

the associated carry core to plus b_r. Thus, after the application of the two numbers, the partial sums will reside in the flip-flops and the carries will reside in the carry cores. If a current pulse is now applied to the carry line (which is one winding linking all carry cores), output pulses will be obtained from those cores which were at plus b_r. Each of these pulses will be applied to the input of the digit column next higher than the column in which it originated and will complement that flip-flop. If that flip-flop held a ONE, then the resulting signal on its ONE line will complement the next higher flip-flop, and so on until a flip-flop is reached which holds a partial sum of ZERO. It should be noted that we are able to pulse all of the carry cores simultaneously because a digit column cannot hold both a partial sum of ONE and a carry of ONE when two numbers are added.

After the above sequence of events, according to the aforementioned rule, the final sum will reside in the flip-flops. It can be read out by simultaneously pulsing the "clear" lines on all the flip-flops (see Fig. 1; these lines are not shown on Fig. 2). (This can be done by pulsing one wire which links all the flip-flops.) The result will be that pulses will occur on the ONE lines of all the flip-flops that hold ONES, no pulses will be obtained from the flip-flops which hold ZEROS, and all the flip-flops will be cleared and ready for the next addition. The output signals can be gated to a bus (this circuitry is not represented in Fig. 2) and from there to storage of wherever desired.

The above discussion has not explained the functions of the gates shown in Fig. 2. They are necessary because it is essential that certain portions of the circuit be isolated from other portions during certain events but essential that they be coupled during other events. Their functions will be explained in the following paragraphs.

It will be noted that when the carry line is pulsed it may be desirable to have the signal from the ONE line of one flip-flop complement the next higher flip-flop. However, a signal also comes from the ONE line of a flip-flop if that flip-flop receives two ONES as input digits, and this signal must not complement the adjacent flip-flop. Therefore, the lower row of gates is necessary, and these gates allow a signal from a flip-flop to complement its neighbor only if the carry line is being pulsed at the same time.

The upper row of gates is required for similar reasons. When both input digits to a flip-flop are ONES, a pulse occurs on the ONE line and is required to switch the associated carry core to plus b_r. However, suppose that a flip-flop holds a ONE and that, when the carry line is pulsed, a signal from the next lower column tries to complement it. If the ONE line of that flip-flop is directly coupled to its carry core, then it will be very difficult to complement that flip-flop. The reason is that at this same time the carry core is saturated by the carry pulse; therefore, the winding on it has a very low inductance and presents practically a short circuit to the ONE line of the flip-flop. Although this difficulty could possibly be overcome, there is another problem which makes these gates necessary. When the final sum is read out, pulses occur on the ONE lines of all flip-flops which hold ONES. If these pulses are allowed to switch the associated carry cores, then they will not be in the state required for the next addition, and clearing the adder becomes quite a problem. To get around these difficulties, a gate is provided which allows a pulse from a flip-flop to switch a carry core

only if an input digit is applied at the same time.

It will just be noted in passing that whenever one of these gates is on, the other is off. This may lead eventually to a simplification of the circuit.

PROPOSED PROCEDURE

A magnetic-core flip-flop (Fig. 1) will be built and tested. The current and power requirements will be determined under various conditions of loading and as a function of prf. Since it is desirable to use a prf of one megacycle or more, ferritic cores will be used and an attempt will be made to increase the usable prf to about ten times that used by Buck (see page 2). The crystal rectifiers shown in the circuit are for preventing backward flow of information and/or removing the load from a core being switched. An attempt will be made to find an optimum arrangement of the rectifiers so that the number of crystals is as small as possible and yet the signal-to-noise ratio (as defined on page 2) is satisfactory. Attempts will be made in all cases to correlate experimental work with theory in as quantitative a manner as possible.

An attempt will be made to incorporate the above-mentioned flip-flop into a binary adder. The circuit just described will serve as a starting point, but an attempt will be made to improve or change this design so as to eliminate tubes and rectifiers as completely as possible. An investigation will be made to determine if the gates should be magnetic or vacuum tube, but preliminary examination shows that, for this particular adder, gate tubes will probably be preferable because of greater power gain and speed.

EQUIPMENT NEEDS

The equipment required will be fairly simple and readily available in the Digital Computer Laboratory. Specifically, the main items will be:

(a) Pulse generators (at least 2)
(b) Oscilloscope
(c) Magnetic cores of the ferritic type with "rectangular" hysteresis loops.
(d) Miscellaneous meters and circuitry

ESTIMATED DIVISION OF TIME

(a) Preparation of proposal	75 hours
(b) Further study of the literature	25 hours
(c) Experimental work and analysis	230 hours
(d) Correlation of results and formulation of deductions and conclusions	40 hours
(e) Preparation of thesis report	80 hours
(f) Total	450 hours

SIGNATURE AND DATE

Robert C. Sims

Robert C. Sims

March 20, 1952

References

The parenthetical note at the end of each reference points out the material that is applicable to this thesis; it is not a summary of the contents of the reference.

1. Everett, R. R., and Swain, F. E., Whirlwind I Computer Block Diagrams, Report R-127, Servomechanisms Laboratory, M. I. T., September 4, 1947, (2 volumes). (Information about the Whirlwind I arithmetic element.)

2. Forrester, Jay W., Digital Information Storage in Three Dimensions Using Magnetic Cores, Report R-187, Servomechanisms Laboratory, M. I. T., May 16, 1950. (Discussion of a particular application for magnetic cores and of magnetic core switching speed.)

3. Harvard University Computation Laboratory, Progress Reports 3, 4 and 5, Investigations for Design of Digital Calculating Machinery, 1949. (General background on the subject of magnetic materials in computers.)

4. Papian, W. N., A Coincident-Current Magnetic Memory Unit, Report R-192, Servomechanisms Laboratory, M. I. T., September 4, 1947. (Analytical and experimental work on magnetic-core circuits and description of testing procedures and techniques.)

SUPERVISION AGREEMENT

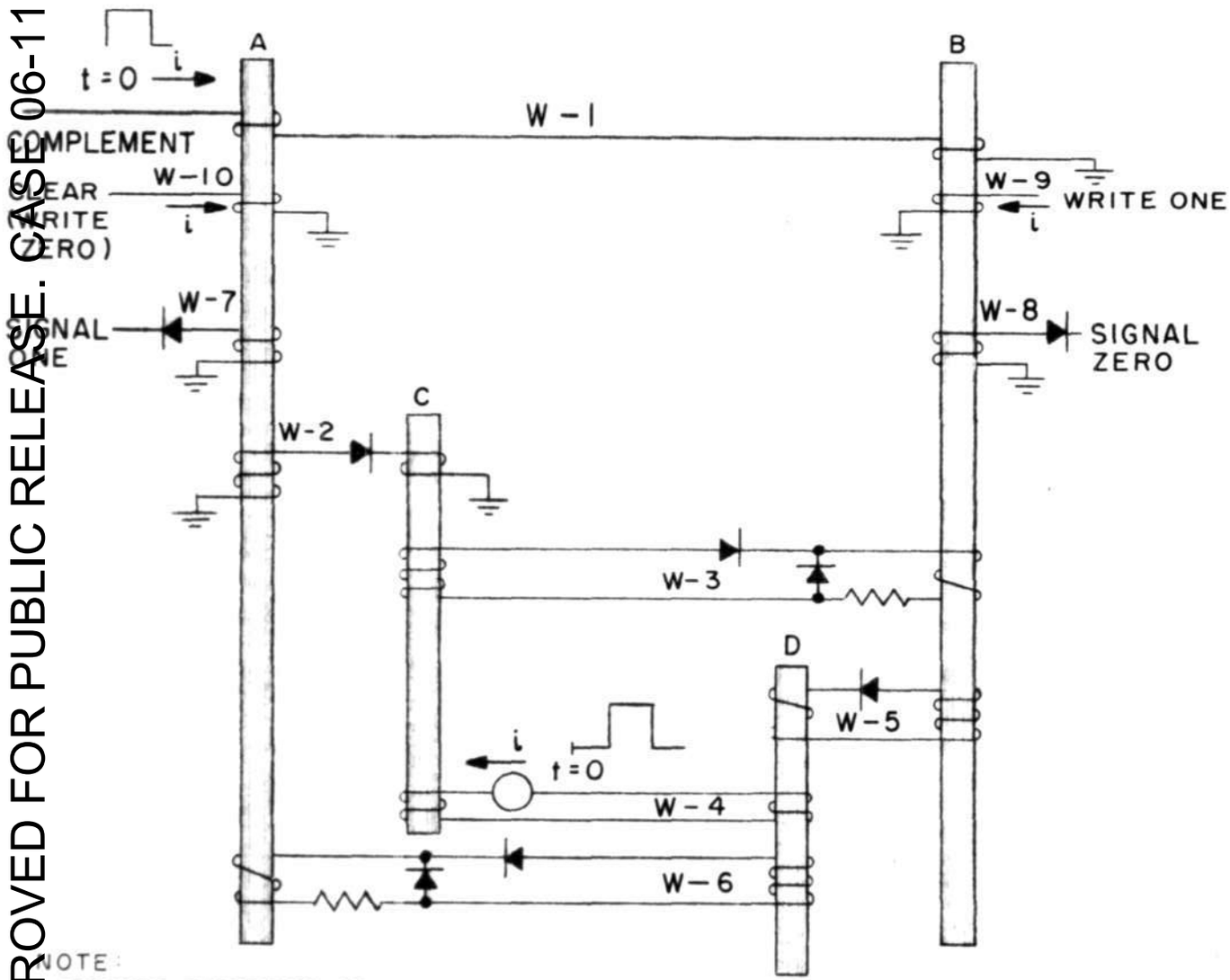
The problem described here seems adequate for a Master's research. The undersigned agrees to supervise the research and evaluate the thesis.

Approved: Norman H. Taylor
Norman H. Taylor

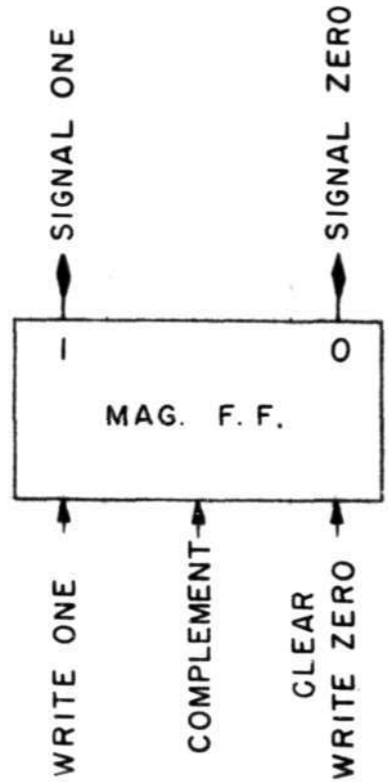
RCS/jk

Drawings attached:

A-51002-1 Fig. 1
A-51001 Fig. 2



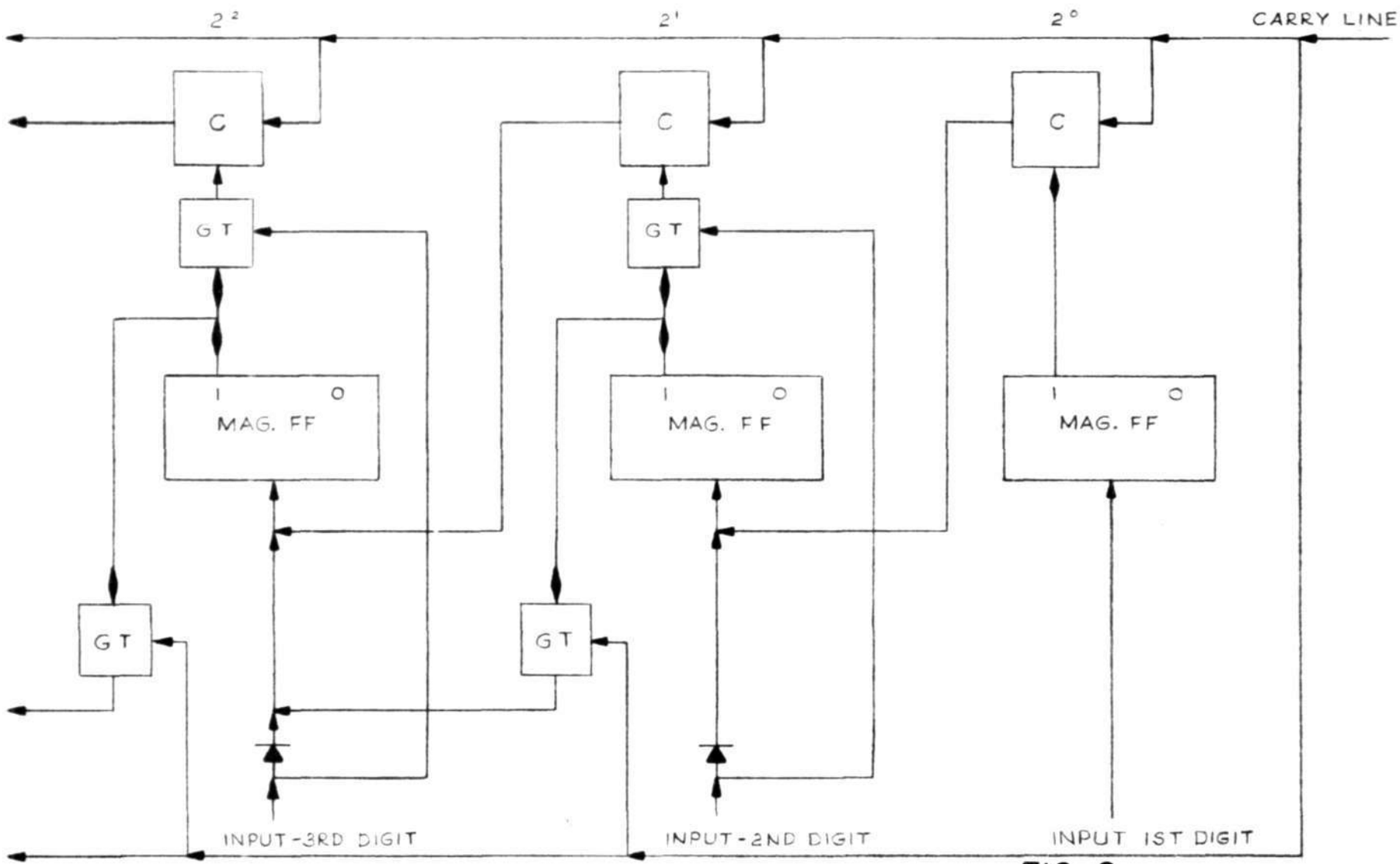
a. CIRCUIT



b. BLOCK DIAGRAM

FIG. 1

MAGNETIC FLIP FLOP



LEGEND:

C= MAGNETIC CORE
C'S ARE WOUND SO THAT IF A CORE HAS RECEIVED A PULSE FROM ITS ASSOCIATED FF, THEN THE CARRY PULSE WILL CAUSE A SIGNAL ON THE OUTGOING LINE.

FIG. 2

A BINARY ADDER USING A MAGNETIC FLIP-FLOP (SEE FIG. 1)