Division 6 - Lincoln Laboratory
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SUBJECT: SPECIFICATIONS FOR THE CENTRAL COMPUTER SYSTEM FOR THE AN/FSQ-7, SUPPLEMENT 4

To: S. H. Dodd

From: R. R. Shorey

Date: 24 October 1955

Approved: H. E. Anderson
H. E. Anderson

Abstract: The AN/FSQ-7 specifications for the Central Computer System as recommended by Lincoln Laboratory were listed in 6M-3291 (released by T.I.R. #1-57), 6M-3291 Supplement 1 (released by T.I.R. #1-66), 6M-3291 Supplement 2 (released by T.I.R. #1-78) and 6M-3291 Supplement 3 (released by T.I.R. #1-93). This supplement (supplement 4) lists status changes and modifications in the following areas:

(a) Revision of the memory element specifications.

(b) Concurrence on previously released but unconcurred amendments to the PERSELBSN code specifications.

(c) Clarification to the arithmetic element specifications.

(d) Revision of the 723 card punch specifications.

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1.0 INTRODUCTION

The specifications for the Central Computer System of the AN/FSQ-7 are defined by Lincoln Laboratory Memorandum 6M-3291, Specifications for the Central Computer System for AN/FSQ-7, (released by T.I.R. #1-57) and supplements 1, 2, and 3 (released by T.I.R. #1-66, 1-78, and 1-97). Modifications to and changes in the status of specifications since the release of 6M-3291 and supplements 1, 2, and 3 are listed but not described in detail in this supplement. In addition, Lincoln Laboratory recommendations on the importance of modifications are included. "Concurrence" as used below means that Lincoln and IBM have agreed on the adequacy of the technical design specified in a particular document.

2.0 SPECIFICATIONS

2.1 Memory Element

IBM document S-12 (PH57-21002), Memory Element Specifications for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central, dated 16 September 1955 received concurrence as noted in the document itself. This document is a revision and compilation of the previously concurred memory element specifications and all supplements. It supersedes D-14, D-14-1, D-14-2, and applicable sections of D-70.

IBM document S-12 specifies that the memory cycle time for the production AN/FSQ-7 machines will be 6 micro-seconds as previously recommended in section 1.1 of 6M-3291 dated 28 January 1955. This specification change was made on the basis of existing AN/FSQ-7 memory circuit design.

2.2 Arithmetic Element

IBM document D-6-3, Clock Register, dated 29 September 1955 received concurrence in a letter dated 13 October 1955. This document is an amendment to the arithmetic element specifications to clarify the operation of the clock register. (Reference section 2.1 of 6M-3291.)

2.3 Instruction Codes

a. IBM document D-16-7, PERSELBSN Codes, dated 19 July 1955, is an amendment to the PERSELBSN Code specifications and was described in section 2.4 of 6M-3291, Supplement 3, dated 24 August 1955. At the time of release, this specification had not received formal Lincoln-IBM technical concurrence. This concurrence has now been accomplished as noted in a letter dated 24 August 1955. As stated in section 2.4 of 6M-3291, Supplement 3, dated 24 August 1955, Lincoln recommends that the codes specified in D-16-7 be incorporated in the initial machine.

b. IBM document D-97, A Revision of the 723 Punch Circuits to Eliminate Programs and a Saving of Computer Time on XD-1 and XD-2, dated 23 March 1955, received concurrence in a letter dated 23 September 1955. This document specifies certain wiring changes to be made to the 723 punch machines to minimize in/out breaks and to eliminate need for subprogram routines. Lincoln recommends that these modifications be incorporated initially if possible. If they cannot be provided initially, they should be retrofitted to all machines. (Reference section 8.1 of 6M-3291).

SIGNED: R R Shorey
R. R. Shorey

RRS:ero

REFERENCE LIST OF CENTRAL COMPUTER SYSTEM SPECIFICATIONS CONTAINED IN 6M-3291,SUPP. #4

Document No.	Title	Linc.Lab. Doc.Rm.No.	Comments
MEMORY ELEMENT			
S-12	Memory Element Specs. for AN/FSQ-7 Combat Direction Central and AN/FSQ-7 Combat Control Central PH57-21002 dated 16 September 1955		Supersedes D-14, D-14-1, D-14-2, and D-70
INSTRUCTION CODES			
D-16-7	Concurrence letter, dated 24 August 1955	6DR-446	
D-97	A revision of the 723 Punch Circuits to Eliminate Programs and a Saving of Computer Time on XD-1 and XD-2, dated 23 March 1955	6DR-459	Amendment to Card Machines Specifications
D-97	Concurrence Letter, dated 28 September 1955	6DR-459	
ARITHMETIC ELEMENT			
D-6-3	Clock Register, dated 29 September 1955	6DR-471	Clarification to initial specification
D-6-3	Concurrence letter, dated 13 October 1955	6DR-472	

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