MEMOREX MODEL 660-0

DISC DRIVE

MAINTENANCE MANUAL A

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PREFACE

This manual is prepared for use by Memorex field engineers (FE); to assist them in maintenance and calibration of the Memorex Model 660-0 Disc Drive.

In preparing the manual, it is assumed that the FE is familiar with basic maintenance techniques and fundamental electronics; with emphasis on integrated circuit logic.

General text and diagrams included in this manual are not covered by Engineering Change (EC) control. Diagrams directly under EC control are included in the companion manual, Maintenance Manual B. (201655)

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SECTION 1

GENERAL INFORMATION

1.1 GENERAL DESCRIPTION

The Memorex Model 660-0 Disc Drive is a direct access storage unit which reads and writes information on Memorex Mark VI, IBM 2316, or equivalent disc packs.

Model 660-0 disc drives (referred to as drives) receive commands and data from the central processing unit (CPU) through a Memorex Model 661 Storage Control Unit (referred to as control unit in this book). Up to nine drives can be attached to the control unit. Figure 1-1 illustrates system configuration when more than one drive is connected to a single control unit.

The 660-0 drive stores or reads data onto a magnetically coated disc pack by rotating the disc pack at a high rate of speed and then inserting a bank of read/write heads which write or read information on the individual discs.

1.1.1 Disc Pack

The storage medium for the 660-0 disc drive is a disc pack which consists of eleven aluminum magnetic oxide coated discs which are mounted 0.4 inches apart on a common hub. Bit information is recorded on the 20 inner disc surfaces. This information is

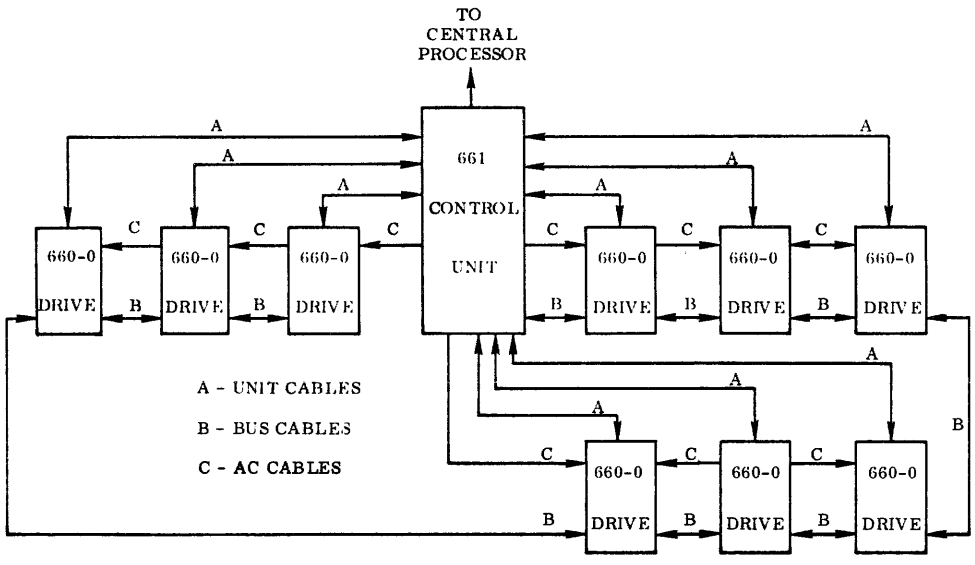


Figure 1-1. System Configuration

recorded on 203 concentric circles (track 000 to track 202) on each disc surface. Since corresponding tracks on all 20 surfaces are vertically aligned, they are considered information cylinders. There are 203 cylinders per pack. Cylinders 200, 201, and 202 are ordinarily reserved as spares under the control of initialization routines.

The disc pack is installed by raising the operator cover and lowering the disc pack onto the spindle. It is secured to the spindle by turning the disc pack handle clockwise until it comes to a full stop. Once the disc pack is secured, its plastic cover can be removed, the operator cover closed, and the machine started. Interlocks prevent the drive motor from starting until the disc pack cover has been removed and the operator cover closed.

1.1.2 Basic Drive Operations

The basic operations of the 660-0 are: first seek, seeks other than the first seek, write, and read.

After the 660-0 disc drive has a disc pack installed and it is started, it performs an automatic first seek. That is, the read/write heads are automatically positioned to cylinder 000 (home position) in order to establish a reference cylinder. During a first seek, the heads (mounted on the carriage) move all the way out to the forward stop. After the carriage comes to rest against the forward stop, it then makes a normal reverse seek to home position.

For seeks other than a first seek, the control unit initiates a seek command and the heads are positioned directly to the designated cylinder.

Writing is performed by a magnetic recording head which flies close to the surface of the disc while the disc rotates rapidly under or over it.

The same magnetic head is used for writing and reading data.

1.1.3 Machine Parameters

DISC PACK CHARACTERISTICS

Recording discs	11
Recording surfaces	20
Tracks per surface	200 plus 3 spares
Disc pack weight, lb	14 (approximate)
Coating material	Magnetic oxide

HEADS

Number of heads	20
Construction	Electromagnetic coils

WRITE OPERATION

Technique	Double-frequency non-return to zero; magnetizing of oxide-coated disc surface

READ OPERATION

Technique	Double-frequency non-return to zero; head coils detect bits. Data is sent to control unit as stream of binary bits.

1.1.4 Visual Orientation

Figures 1-1a through 1-5 illustrate the basic machine parts of the 660-0 disc drive with the covers removed. The front and back covers are attached to the main frame by magnetic strips and they pull off. The operator control panel cover lifts off from the rear after two latches at the back of the machine are released. The shroud area cover can be removed in the same way.

1.1.5 Communication Lines

Below is a list of communication lines which connect the 660-0 disc drive to the control unit. To see the name changes these signals undergo when entering or leaving the drive refer to the following system logic diagrams: Line Driver (LD100), Line Driver (LD110), Line Receiver (LR100), Read/Write Gating (RW110), and Sequence In and Out (SL100).

DATA LINES

A. Read/write data (coax)

OUTPUT LINES

A. Cylinder address register (eight lines)
B. Unit is selected (status line)
C. Unit attention (one per drive)
D. Selected unit write I sense (status line)
E. Selected unit on line (status line)
F. Selected unit busy (status line)
G. Selected unit seek incomplete (status line)
H. Selected index (status line)
I. Selected unit read only (status line)
J. Selected unit pack change (status line)
K. Selected unit end of cylinder (status line)
L. Selected file unsafe (status line)

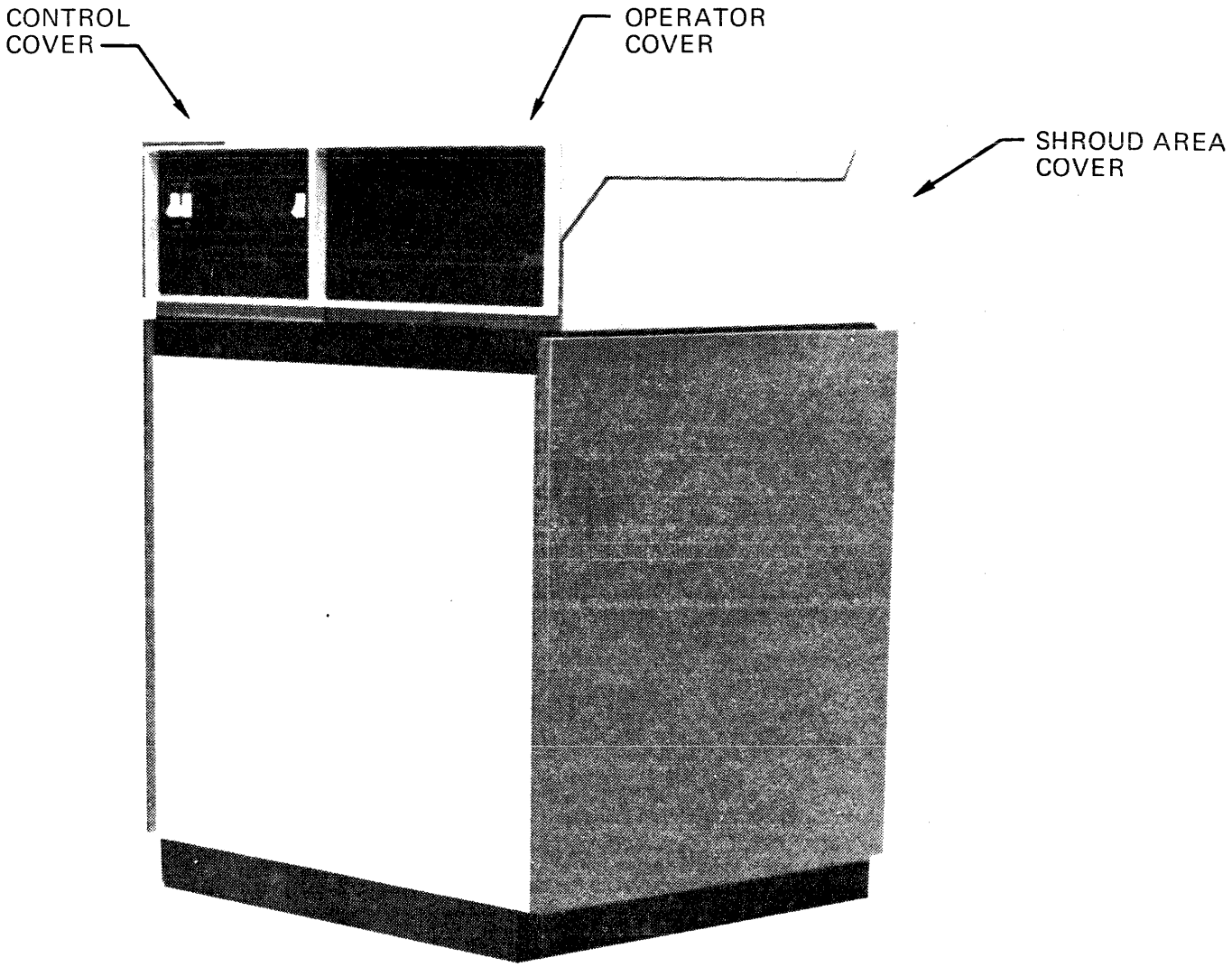


Figure 1-1a. Front View of 660-0 Disc Drive

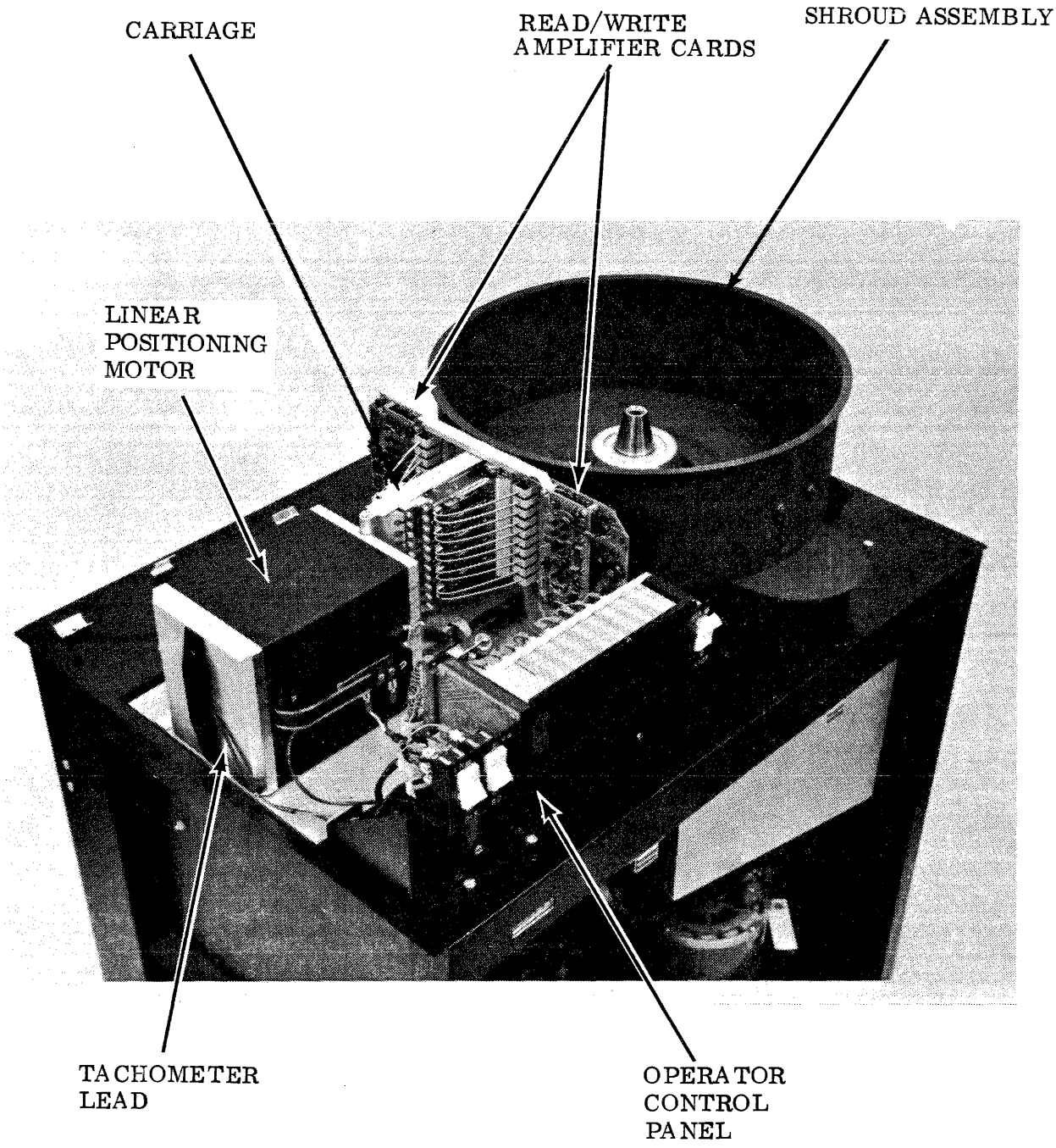


Figure 1-2. View From Front Left

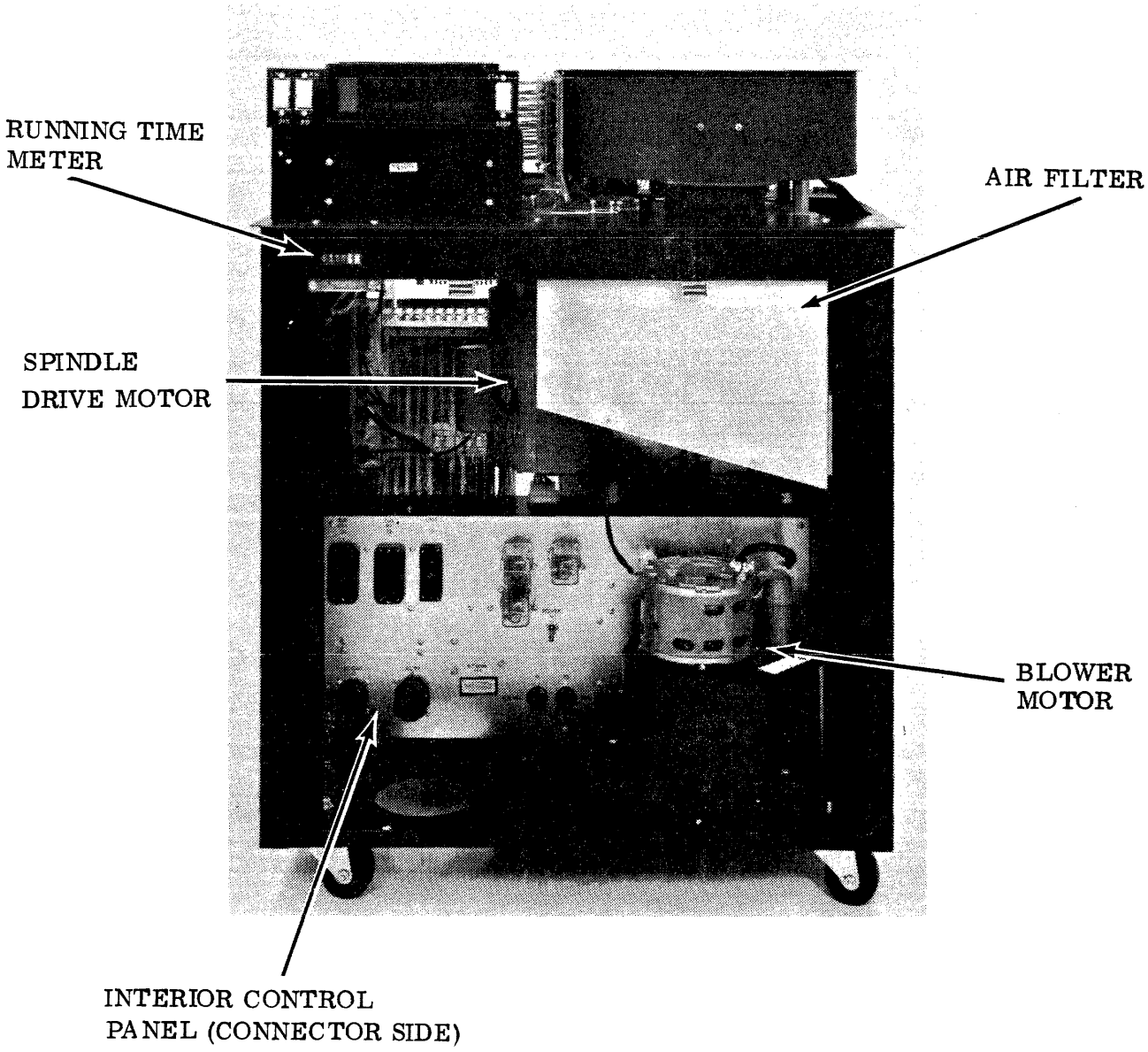


Figure 1-3. Front View

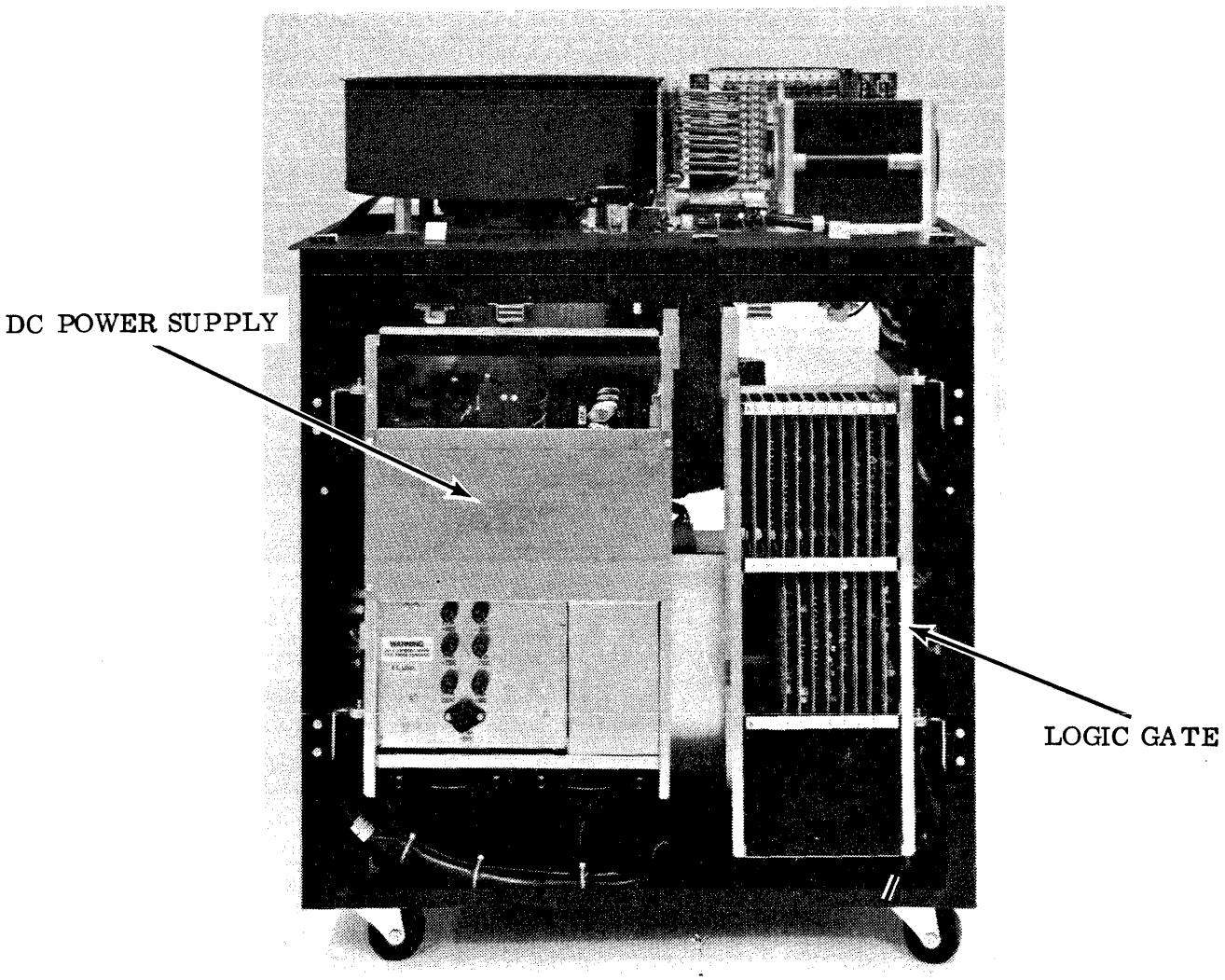


Figure 1-4. Rear View

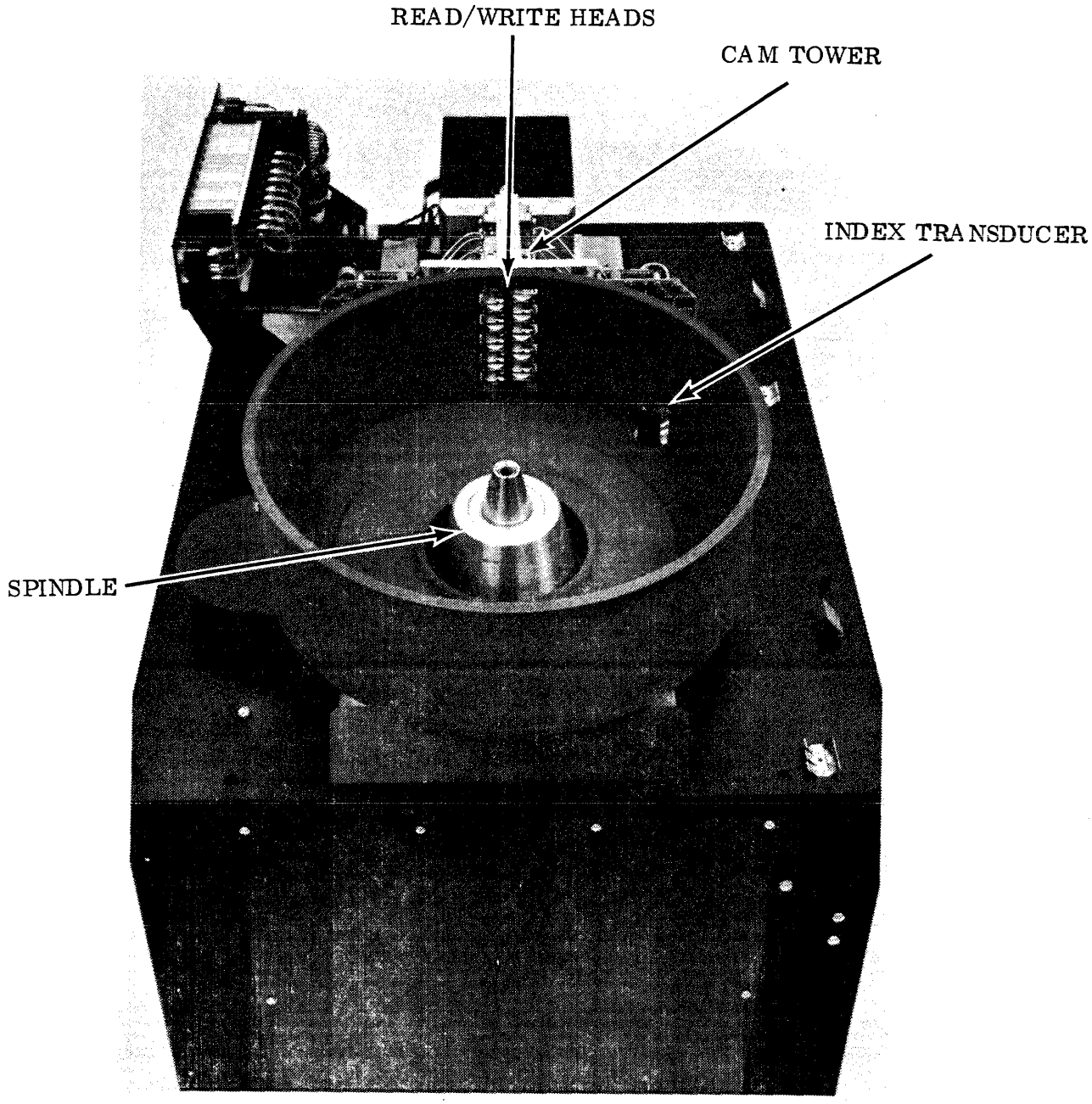


Figure 1-5. View From Rear Left

M. Sequence power out

N. Sequence out

O. Heads extended (switch closure to ground when heads extended)

INPUT LINES

A. Unit bus (eight lines)

B. Select unit (one per drive)

C. Control (tag line)

D. Set head (tag line)

E. Set cylinder (tag line)

F. Sequence in

G. Controlled ground

H. Sequence power in

1.1.6 Operator Control Panel

Figure 1-6 shows the operator control panel. The functions of switches and indicators are as follows:

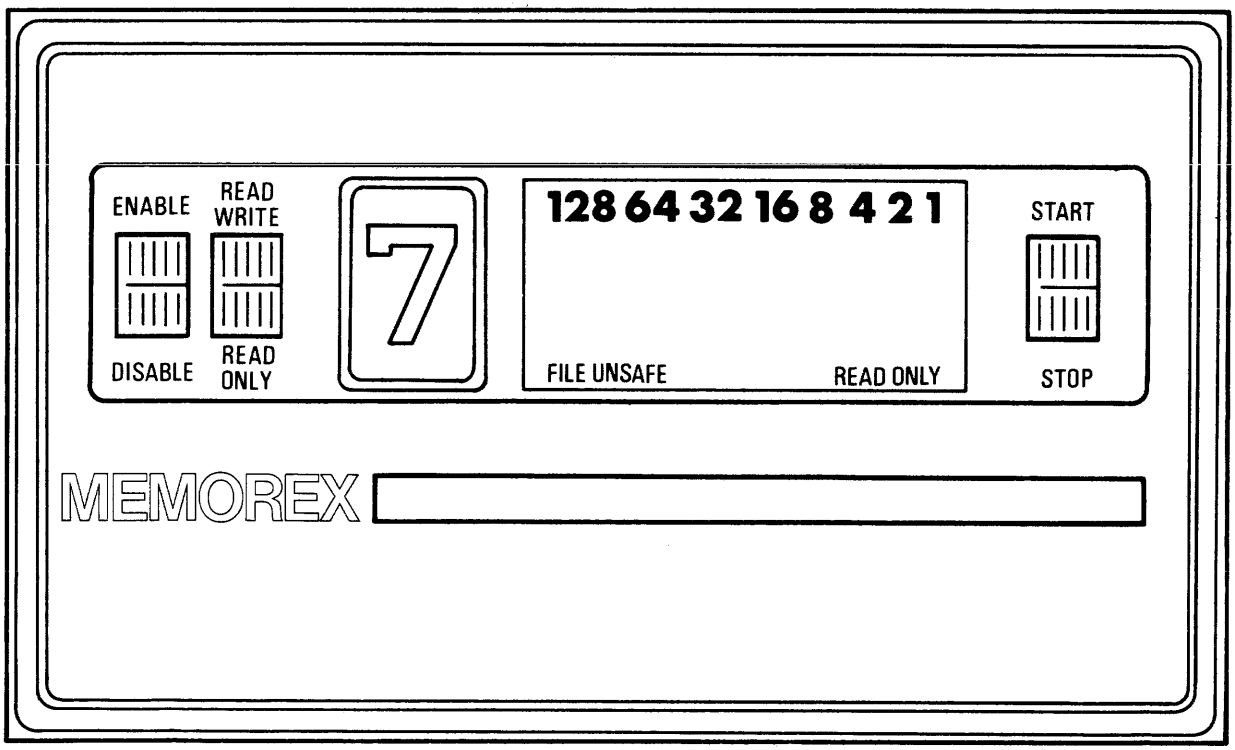


Figure 1-6. Operator Control Panel

A. ENABLE-DISABLE Switch (FE use only)

ENABLE Position — The switch enables the logical connection between the control unit and the drive.

DISABLE Position — The switch disables the logical connection between the control unit and the drive.

If the drive is performing an operation under the command of the control unit, changing the state of the switch will not change off-line logic until the control unit deselects. Upon next select, off line status is returned to the control unit.

B. READ/WRITE - READ ONLY Switch

When in the READ/WRITE position, this switch enables both the read and write circuitry. In the READ ONLY position it disables the write and erase circuitry to allow READ ONLY operation.

C. UNIT NUMBER/READY Indicator (green)

The unit number plug is combined with this indicator. The plug number is permanently marked to correspond to the factory-coded number on the plug. The unit number plug can be changed easily to reflect the logical unit number of the drive in the system. This indicator illuminates when the drive is ready for instructions; i.e., when the drive has reached operational speed and the heads are positioned to track 000 on the initial load operation. The indicator goes off when the STOP switch is pressed or when system power is dropped. The indicator also goes off if the detent remains unseated for 100 ms or longer.

D. FILE MONITOR Indicators

The access position indicator continuously identifies the cylinder where the heads are positioned.

This group of eight lights provides a weighted binary readout of the cylinder position (specified in the last seek command) of the access mechanism. A red light indicates a FILE UNSAFE condition; this indicator illuminates when the safety circuits determine that the drive is not usable. A white light indicates that the READ ONLY mode is selected; this indicator illuminates when the write and erase circuits are disabled by the READ ONLY switch.

E. START-STOP Switch

This switch initiates the 60-second power-on sequence when placed to START. Interlocks prevent the drive from starting if the disc pack is improperly installed or the operator cover is not closed. When positioned to STOP and power to the motor cuts off, the carriage moves in a reverse direction to pull the heads out of the pack. Electrodynamic braking power is applied to the drive motor to stop pack rotation in 15 seconds.

SECTION 2

THEORY OF OPERATION

The 660-0 disc drive cabinet houses the following functional areas: read/write head positioning mechanism, spindle drive mechanism, and control circuitry (logic boards). These areas and the timing and operations are described in this section.

2.1 READ/WRITE HEAD POSITIONING MECHANISM

The read/write heads are inserted into the disc pack by the linear positioning motor. This motor has a stationary permanent magnet surrounding a moveable bobbin-wound armature. The armature slides in and out of the magnet through a hole in one of the magnet's faceplates. Fastened to the armature is the Tee-block which holds the head-arm assemblies. The Tee-block is mounted on a carriage that moves freely on ball bearing rollers along hardened aluminum tracks. Movement of the armature in and out of the permanent magnet moves the carriage forward and back and is determined by current which is generated in the servo system (see Servo System logic card description, section 2.8.13).

The head-arm assemblies are mounted in two banks of ten each. Half the head faces are positioned upward and the other half facing downward to record on both the top and bottom surfaces of the disc. When the banks are retracted (withdrawn from the pack), plastic unload cams attached to the aluminum tower which arches over the head arms bear against a ramp surface (an integral part of the head arm) thus separating the heads by countering the loading force. The heads are separated enough to clear the discs during load and unload operations.

When the heads are inserted into the disc pack, the ramp rides off its cam. When the ramp is clear of the cam, spring tension from the head arm forces the head toward the disc surface. As the disc pack rotates an air cushion, or bearing, between the head and disc surface is created. This air cushion keeps the heads at the required flying height.

2.2 DETENT MECHANISM

To make certain the read/write heads are positioned to the desired cylinder and remain at that cylinder, a rack of teeth called the detent rack is mounted on the carriage directly under the array of head arms. As the carriage moves along the track during positioning, the detent rack moves with it. Each tooth on the rack corresponds to two adjacent cylinders on the disc pack. A double detent pawl is mounted on the carriage way opposite the rack. Each pawl has a set of teeth with the same pitch as the rack teeth and the two pawls are offset

from one another by half their pitch. This offset spacing allows the pawl to engage the rack in twice as many positions as there are teeth. When one pawl is engaged, the other rests on top of the adjacent rack tooth. Therefore, one detent pawl engages at all odd-cylinder positions while the other engages at all even-cylinder positions.

Track numbers are determined by counting the number of teeth on the detent rack. This counting is accomplished by the cylinder transducer which is mounted adjacent to the detent pawls, opposite the detent rack.

2.3 SPINDLE DRIVE SYSTEM AND INDEX TRANSDUCER

The spindle drive system rotates the disc pack. This system includes the spindle drive motor, spindle, and drive belt.

The 1/2 horsepower motor transfers torque to the spindle drive pulley by a simple belt loop. Tension on the belt is maintained by a special motor shock mounting; therefore no idler pulley is used.

The drive motor also serves as a dynamic brake for the disc pack drive. When the STOP switch on the operator control panel is pressed, ac power to the motor is cut off and dc power (55 volts) is applied to the motor for approximately 15 seconds, causing it to stop.

The disc pack spindle is bolted into a hole in the baseplate. The spindle pulley is below the baseplate and its disc mounting surface is above the baseplate. A disc pack is secured to the spindle cone by a locking shaft within the spindle and Belleville washers below the spindle pulley.

The spindle assembly includes a mechanical lock which engages when the operator cover is raised to load or unload a disc pack. When this cover is lifted, an arm on the cover tilts back the index transducer. This movement causes a pawl under the baseplate to engage one of several notches in the spindle pulley. While the cover is raised the pawl will prevent the spindle from turning. This lock can be bypassed by removing the shroud area cover from the machine. The assembly also includes a pack-on switch which automatically closes when a disc pack is installed. This switch is a safety feature and must be closed for the spindle drive motor to operate.

The bottom plate of the disc pack has a single slot notched in its edge. The index transducer recognizes this slot as the track index marker and also uses it for up-speed detection.

2.4 TIMING

The control unit must satisfy certain timing requirements in order to instruct a drive to perform operations. The timing requirements associated with several basic drive operations are defined by the timing diagrams in Figure 2-1.

2.4.1 Seek to Specified Cylinder and Head (Timing Diagram A)

In a seek operation, the control unit moves the drive's carriage to a new cylinder address and causes the head setting circuits to partially enable one of the 20 heads. To do this it must:

A. Set the new cylinder address into the CAR
B. Reset the head register
C. Set the new head address into the head register
D. Start the seek with a Seek Start signal.

2.4.2 Read (Timing Diagram B)

When the heads are positioned at the correct cylinder with the appropriate address in the head register, the control unit can cause the drive to begin reading. To do this the control unit must:

A. Raise the Control tag line and Unit Bus 5 to select the head
B. Raise the Control tag line and Unit Bus 1 to enable the read gate.

A read operation can be initiated whenever the drive's Busy line to the control unit is inactive. Valid read data appears on the Read Data output line within 10 μs after the Control tag line enables the Select Head and Read lines.

2.4.3 Write (Timing Diagram C)

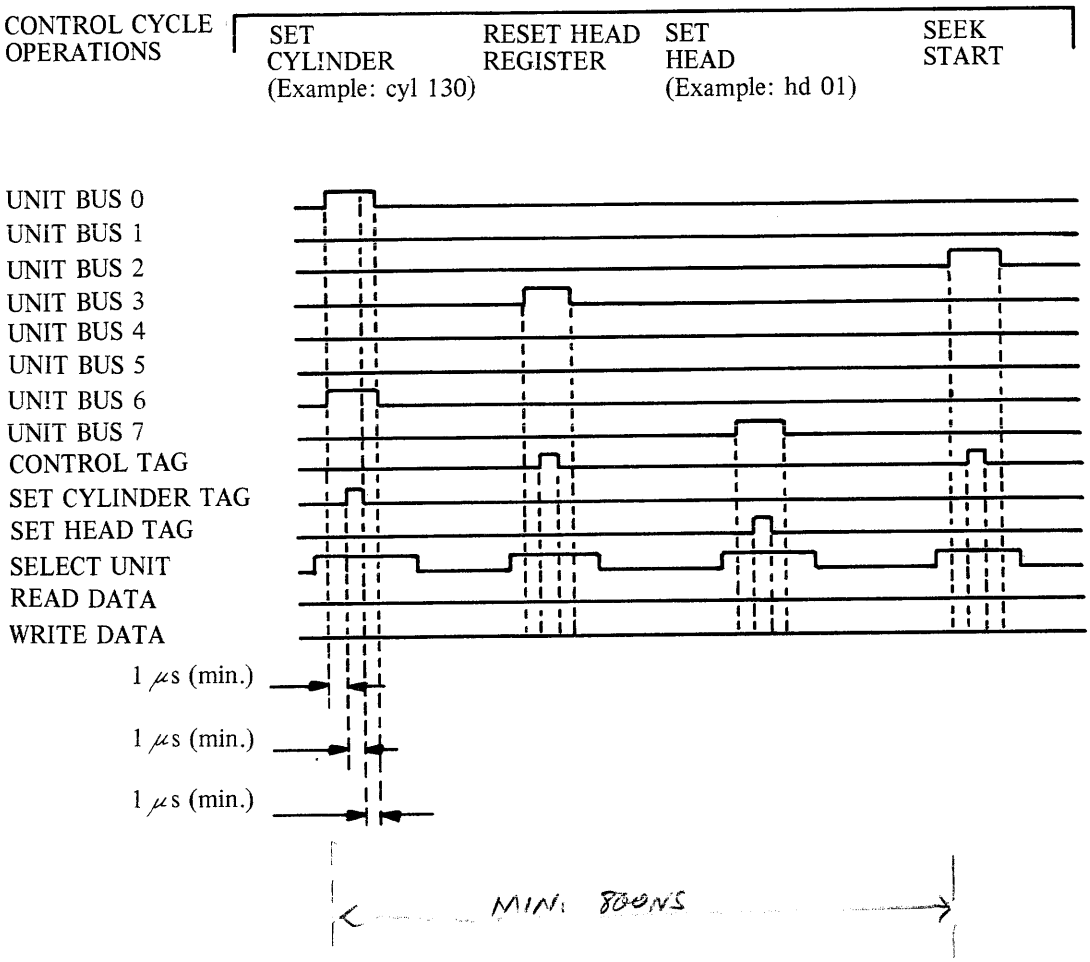
When the heads are positioned at the correct cylinder with the appropriate address in the head register, the control unit can cause the head to begin writing. To do this the control unit must:

A. Raise Unit Bus 0 (Write) and, Unit Bus 4 (Erase) simultaneously, and then raise Unit Bus 5 (Select Head).

B. Then raise the Control tag line. This must not occur sooner than 18 μs after a read operation ends* or else the erase current transient might alter data on the disc surface.

*A write operation is usually preceded by a read operation. This is because the control unit verifies that the heads are correctly positioned and that the correct head is selected by reading some characteristic track address information before beginning a write operation.

TIMING DIAGRAM A



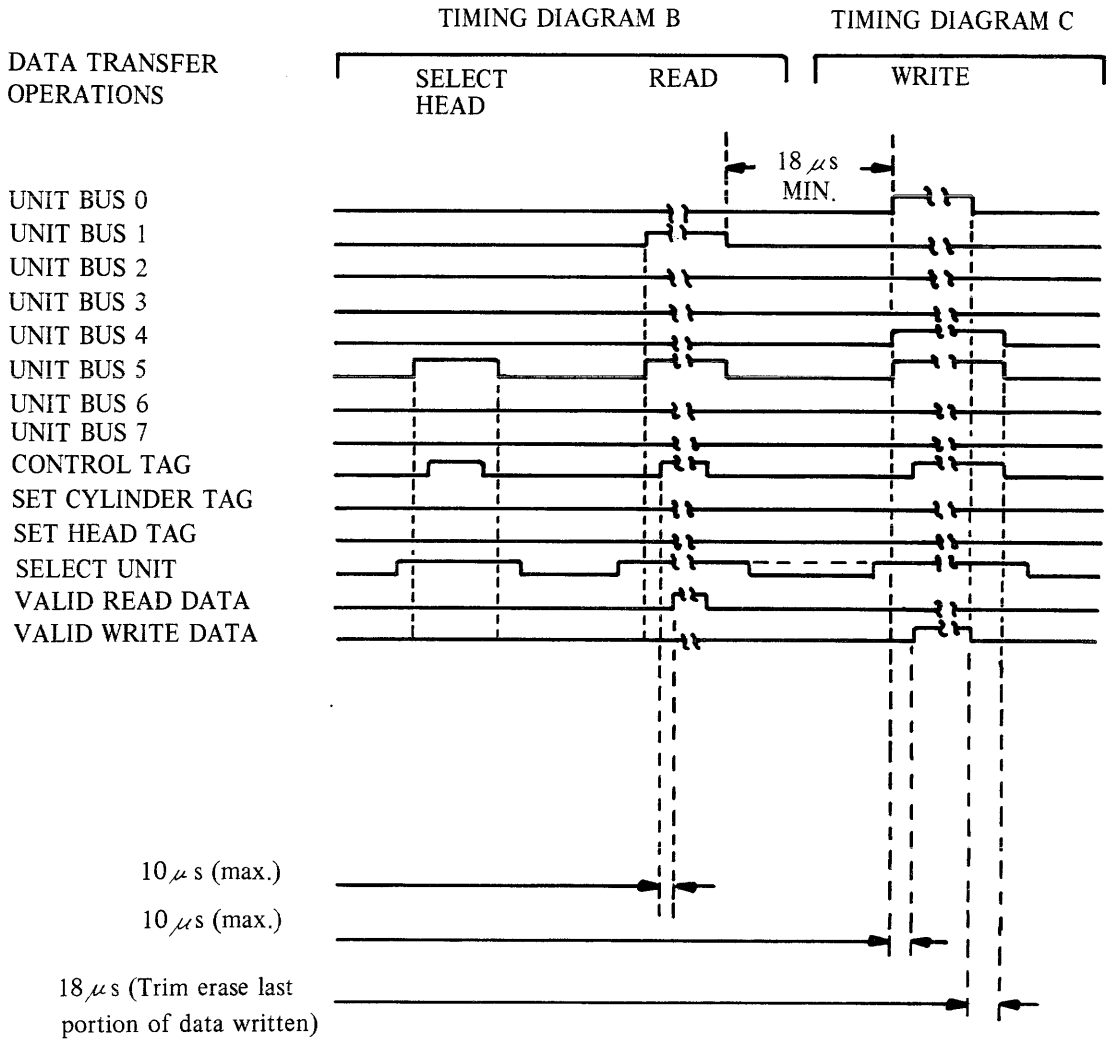
GENERAL TIMING DIAGRAM NOTES

1. These diagrams apply to signals at disc pack drive connectors. No allowance is made for propagation delays.

2. Select Unit must always be raised before a command is given so control unit can check to be sure only one unit is being selected.

3. All 1 μs times have the tolerance ±200 ns.

Figure 2-1. General Timing Diagram (Sheet 1 of 3)



* On a read or write operation, control tag's trailing edge must occur before bus lines are changed.

** Select unit may be left enabled between read and write operations.

Figure 2-1. General Timing Diagram (Sheet 2 of 3)

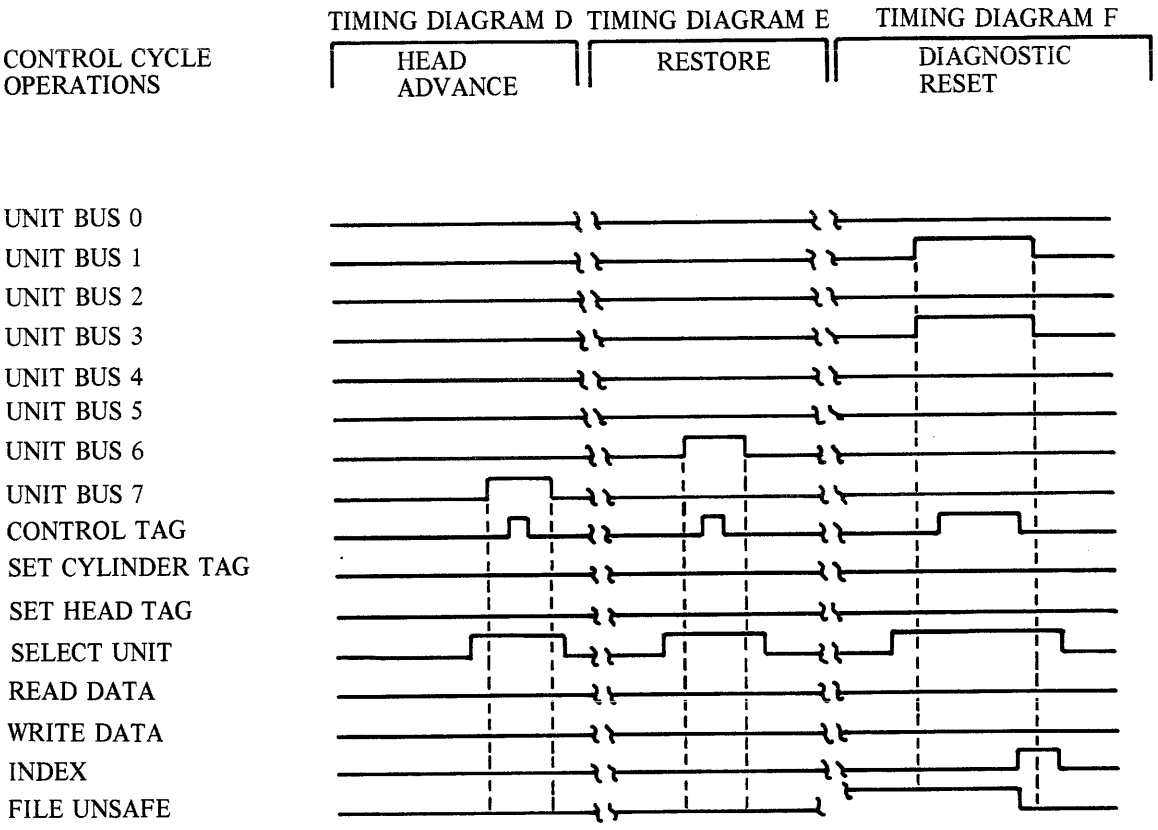


Figure 2-1. General Timing Diagram (Sheet 3 of 3)

C. When concluding a write operation, Unit Bus 4 must be held active for 18 μs after Unit Bus 0 is dropped to allow the erase current to erase all the way to the end of the track. Since the erase poles trail the write gap by 0.005", removing erase current at the same time the write gate is disabled would leave 0.005" of untrimmed data.

Write and erase can be selected any time the Ready line to the control unit is active, the drive is not reading, and the READ/WRITE-READ ONLY switch is in the READ/WRITE position (FE function only). Valid write data appears on the disc surface no later than 10 μs after the Control tag line enables the Select Head and Write lines.

2.4.4 Head Advance (Timing Diagram D)

When a read or write operation uses the tracks of a cylinder in a consecutive sequence, head selection advances one head at a time from the first head selected to the head located at the end of the cylinder. To do this, the control unit must:

A. Raise the Select Unit line
B. Raise Unit Bus 7 (Head Advance line during control cycle)
C. Raise the Control tag line to enable the Head Advance line.

When the head address increments to 20 (one more than the highest head address), the drive sends an End of Cylinder signal to the control unit. The head address can be advanced if no other head is already selected.

2.4.5 Restore (Timing Diagram E)

Whenever the exact position of the heads is in doubt, the control unit can cause them to move to a known position (cylinder 000) by initiating a restore (recalibrate) operation. To do this it must:

A. Raise the Select Unit line
B. Raise Unit Bus 6 (Restore line during control cycle)
C. Raise the Control tag line.

A restore command can be issued at any time except during a read or write operation.

2.4.6 Reset Attention

The drive logic which generates the Attention signal to the control unit can be reset by a Reset Attention command from the control unit. To do this it must:

A. Raise the Select Unit line

B. Raise Unit Bus 1 (Read line during control cycle)

C. Raise the Control tag line.

The control unit uses the same lines to initiate Reset Attention as it does for Read because Reset Attention is most frequently used just before a read operation. However, Reset Attention can be issued at any time except during a write operation.

2.4.7 Diagnostic Reset (Timing Diagram F)

The Diagnostic Reset command is used to reset the file unsafe logic in the drive when that logic has been set as part of a diagnostic routine. To issue a Diagnostic Reset command, the control unit must:

A. Raise the Select Unit line

B. Raise Unit Bus 1 and Unit Bus 3

C. Raise the Control tag line.

The Diagnostic Reset command can be issued at any time except during a write operation.

2.5 FIRST SEEK

When the START switch on the operator control panel is pressed (assuming that the disc drive is connected to a control unit and that the main power switch is ON), power is supplied to the spindle drive motor and the disc pack begins rotating. During a 60-second warm-up delay, the servo sequencer logic, cylinder address register (CAR), present address register (PAR), and delay timers (Seek Incomplete, Forward Seek and Ready) are held reset. When the warm-up delay is over, the servo sequencer logic is enabled. The servo sequencer logic consists of four flip-flops and associated gates which initiate each step (logic state) in any seek or restore sequence. This logic controls the progress of the servo and other access logic from state to state. The sequencing logic is synchronized by free-running clock pulses generated by the transducer oscillator.

The first strobe pulse following the warm-up delay steps the Servo Sequencer into the first state in a first seek sequence (this sequence is identical to a restore sequence*). At this point, a brief Forward Seek delay is initiated. This delay has no function at this time since the detents are not engaged. It is intended for forward seeks and restore operations to allow the detents to disengage (pick) before applying current to the servo. Following this

*There is one insignificant difference. A first seek always begins with the carriage fully retracted; the carriage could be at any position along the carriage way at the beginning of a restore operation.

delay, a prescribed amount of current is fed to the linear motor to start it moving forward slowly.

The Servo Sequencer monitors the forward velocity line and senses when the line goes true and subsequently false. The CAR and PAR reset signals are removed when the line goes true. When the line goes false, it indicates that the carriage has come to rest against the forward carriage stop. With the carriage at the forward carriage stop, the forward current to the linear motor is removed and a holding current is applied. This holding current keeps the carriage stable while the logic prepares to begin a reverse seek.

A count of 202 is forced into the direct set inputs of the PAR. A present address of 202 is used even though the carriage is actually positioned beyond cylinder 203. This is because there are 203 teeth on the pack that are counted, and the logic on the transducer amplifier board causes the logic to miss the first count during the reverse portion of a first seek or restore operation. Another Forward Seek delay is begun, and a Seek Incomplete delay begins. As soon as the Forward Seek delay times out, the Servo Sequencer logic initiates a normal reverse seek to cylinder 000 (since the CAR flip-flops are still reset, the carriage destination is cylinder 000). The Seek Incomplete delay determines the amount of time the positioning mechanism is allotted to complete the seek before a seek incomplete signal is sent to the control unit.

An adder circuit derives the algebraic difference between the CAR and PAR contents. This difference is the number of cylinders the carriage must travel to arrive at cylinder 000. The output of the adder is converted to a voltage that corresponds to a velocity desired for a seek of this length. This voltage is converted to a current which is applied to the linear motor. The motor accelerates the carriage toward cylinder 000.

As the carriage (and linear motor bobbin) move, a voltage is induced in the tachometer. This voltage is fed back and compared with the desired velocity voltage. Current to the motor is controlled by the algebraic difference of the desired voltage and the actual voltage. Consequently, the current is increased, decreased, or reversed, depending on the relative values of the desired and actual velocity voltages.

As the carriage approaches its destination, the voltage programming the desired velocity is decreased by steps. Each time it decreases, it drops below the actual velocity fed back by the tachometer. The excess of actual voltage causes the carriage to decelerate at each step.

When the carriage reaches cylinder 000, contents of the CAR and PAR agree (difference is 0). This generates a compare signal which causes the reverse current to the motor to be replaced by a small amount of forward current. Momentum carries the carriage almost one

cylinder past cylinder 000. By then, the forward current overcomes momentum and causes the carriage to reverse direction of travel. The compare signal also activates the detent actuator logic so that the detent pawls are in the process of engaging the rack during the turnaround period. Since the carriage reverses direction before one of the pawls can completely set, it is detented while traveling forward. As soon as the tachometer senses the lack of forward velocity, a Ready delay is initiated. This delay provides time to allow the small mechanical vibrations caused by detenting to be dampened before a Not Busy signal is sent to the control unit. Following this delay, the drive signals the control unit that it is ready for use.

If, for some reason, the carriage is not detented within the time allowed by the Seek Incomplete delay, a Seek Incomplete signal is sent to the control unit, which will normally respond by initiating a restore operation. A restore operation is identical to a first seek. Its purpose is to bring the carriage to a known position (cylinder 000).

2.6 SEEKS OTHER THAN THE FIRST SEEK

The control unit initiates a seek while a drive is in the ready state. To do this it must first select the drive. It then transfers the address of the cylinder to the drive on the eight Unit Bus lines. This address is gated into the CAR in the drive during the Set Cylinder cycle. Next, the head register is cleared when Unit Bus line 3 goes low during the Control cycle. The head address is then transferred to the drive on Unit Bus lines 3 through 7 and gated into the head register during the Set Head cycle. Finally, the drive is enabled to begin the seek when Unit Bus Line 2 goes low during the Control cycle. This generates a Seek Start signal in the drive logic.

The Seek Start signal causes the Servo Sequencer logic (refer to the First Seek discussion for a description of the Servo Sequencer logic) to advance to the first state in a normal seek sequence. In this state, a comparison (algebraic addition) is made between the complement of destination address (which is stored in the CAR) and the present address of the carriage (whichis stored in the PAR). If these two addresses are the same, no seek is performed. If they are different, the difference represents the number of cylinders the carriage must travel to reach its destination. The sense of the carry out of the adder determines the direction of travel (false = forward seek and true = reverse seek).

2.6.1 Forward Seek

If the comparison by the adder logic results in a Forward Seek, a brief Forward Seek delay is begun and holding current to the linear motor is dropped. The delay gives the carriage time to relax its forward pressure against the detent pawls after holding current drops so that the detent actuator logic can pick the detent pawls clear of the detent rack. At the

same time the Forward Seek delay begins, a Seek Incomplete delay is initiated. As soon as the Forward Seek delay times out, the detent actuator logic disengages the detent pawl, and Seek Forward signals are generated. One of these signals enables the output of the adder logic and the other enables the up-down counter in the PAR.

Output of the adder goes to speed decode logic which encodes the difference into a series of seven forward or reverse velocity signals. These velocity signals are converted by the Servo System to a voltage that corresponds to a programmed velocity. This voltage is converted to a current which is applied to the linear motor. For longer seeks the peak velocity will be greater.

As the carriage reaches each new cylinder, the cylinder transducer amplifier generates a count pulse that alters the PAR contents by one (increases during forward seeks, decreases during reverse seeks). When the contents of the PAR equals the contents of the CAR, the carriage has reached the destination cylinder. At this point, a Compare signal is generated and the last step of the positioning voltage is dropped. In its place, a low level Forward Detent Velocity signal is generated. The Compare signal activates detent actuator logic so that the detent pawls begin to engage (set). When one of the detent pawls fully sets against a detent rack tooth, the carriage stops moving. The forward velocity detector senses this and causes the Forward Detent Velocity signal to be replaced by a small Holding Current signal, also in the forward direction. The Ready delay is initiated. This delay provides time to allow the small mechanical vibrations of the carriage to be dampened before the Busy signal to the control unit is dropped. Following this delay, the drive signals the control unit that it is ready for the next operation. In addition to the Busy signal, the drive sends an Attention signal to the control unit. This signal serves as an interrupt to the control unit and as soon as it completes whatever operation it is engaged in at the time it reselects the drive and instructs it to perform some operation (probably a read or write operation).

If, for some reason, the carriage is not detented within the time allowed by the Seek Incomplete delay, a Seek Incomplete signal is sent to the control unit along with an Attention signal. The control unit responds by initiating a restore operation. A restore operation is identical to a first seek. Its purpose is to bring the carriage to a known position (cylinder 000).

2.6.2 Reverse Seek

A reverse seek differs little from a forward seek. If the adder logic generates a reverse seek command instead of a forward seek command, the detent pawl is picked immediately and reverse current is applied to the linear motor as soon as holding current is dropped. This is possible because of the relative slopes of the detent pawl teeth and detent rack teeth.

When the carriage is traveling backwards, the detent pawls will not lock up against a tooth face. When the destination cylinder is reached during a reverse seek (Compare signal is generated) the programmed reverse velocity is replaced by Forward Detent Velocity current and the detent pawls begin to engage just as during a forward seek. However, momentum carries the carriage almost one full cylinder past the destination cylinder before the forward detent velocity current can overcome it and reverse the direction of travel. The carriage begins moving forward and then the detent pawl sets. This turnaround portion of a reverse seek is necessary to allow the detent pawls to engage while the carriage is moving forward. As soon as the forward velocity detector senses that the carriage has stopped moving, the Ready delay begins. Following the delay, the Attention signal is sent and the Busy signal to the control unit is dropped.

2.7 READ/WRITE OPERATIONS

After the heads are positioned to the designated cylinder, the control unit selects one head to read. It does this by first activating the Select Unit line and then Unit Bus 1 (read gate) and Unit Bus 5 (Select Head) followed by the Control tag line which enables the bus lines. To initiate a write operation, the control unit first activates the Select Unit line, and then Unit Bus 0 (write gate), Unit Bus 4 (erase gate), followed by the Control tag line which enables the bus lines.

Although the ultimate purpose of the seek may be to write data on the track, the selected head will usually be instructed to read first, because it is necessary for the system to verify the accuracy of the seek by reading bytes of information which identify the track (e.g., home address). However, since it is easier to understand the read operation after learning how data is recorded, the write process is described first.

2.7.1 Write Operation

Information is recorded on a disc surface using the double-frequency nonreturn-to-zero technique. The stream of data is received from the control unit as a series of clock and data pulses. Every 400 ns (2.5 MHz), a clock pulse arrives, establishing a time base; the interval from clock pulse to clock pulse is called a bit cell time. If there is no data pulse between two clock pulses, that bit cell time represents a binary 0. A bit cell time containing a data pulse midway between two clock pulses (200 ns after a clock pulse and 200 ns before the next clock pulse) represents a binary 1.

These pulses enter the write logic where they are detected by a line receiver. The pulse output of the line receiver toggles a complementary flip-flop. The outputs of the flip-flop are used alternately to cause the polarity of a flux field in the read/write head to reverse each time a pulse is received. The flux field is used to polarize ferric-oxide particles on the disc surface as the disc rotates under the head. Each flux reversal causes a polarity

reversal in the recorded track. Consequently, each polarity change in the recorded track corresponds to either a clock or data pulse and is called a bit.

The read/write head used by the drive consists of a ferrite core with ends separated by a very small gap. A center-tapped coil is wound around a portion of the core. When current passes through the coil in one direction, a flux field builds up across the gap in the core. This is shown in Figure 2-2. The polarity of the flux field depends on the polarity of the current.

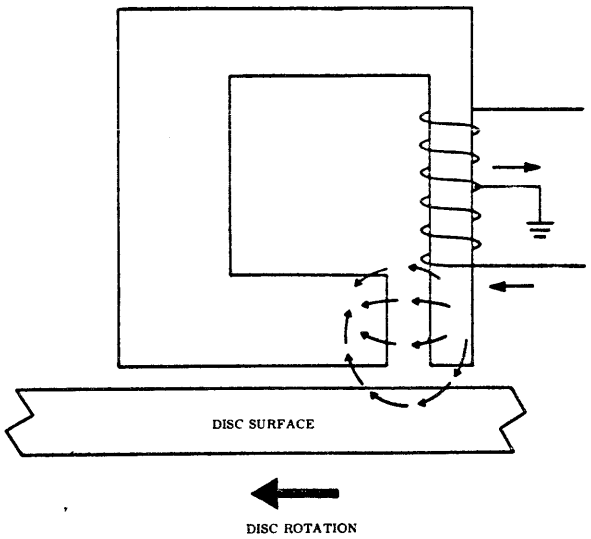


Figure 2-2. Read/Write Coils and Gap

When the head is loaded (flying just above the disc surface) the gap in the core is close enough to the disc surface for the flux field to flow into the disc coating and magnetize its ferric-oxide particles. This is the flux field that reverses with each clock or data pulse, recording a series of binary ones and zeros that corresponds to the series received from the control unit. See Figure 2-3.

As a track of data is being written, narrow bands on each side of the track are erased to allow for slight variations in head positioning. It assures that there is no residual data along the edges of the new track from the previous recording. Side trimming is accomplished by a horseshoe-shaped electromagnet which is fixed to the core of the read/write gap and then under the side trim erase poles. See Figure 2-4.

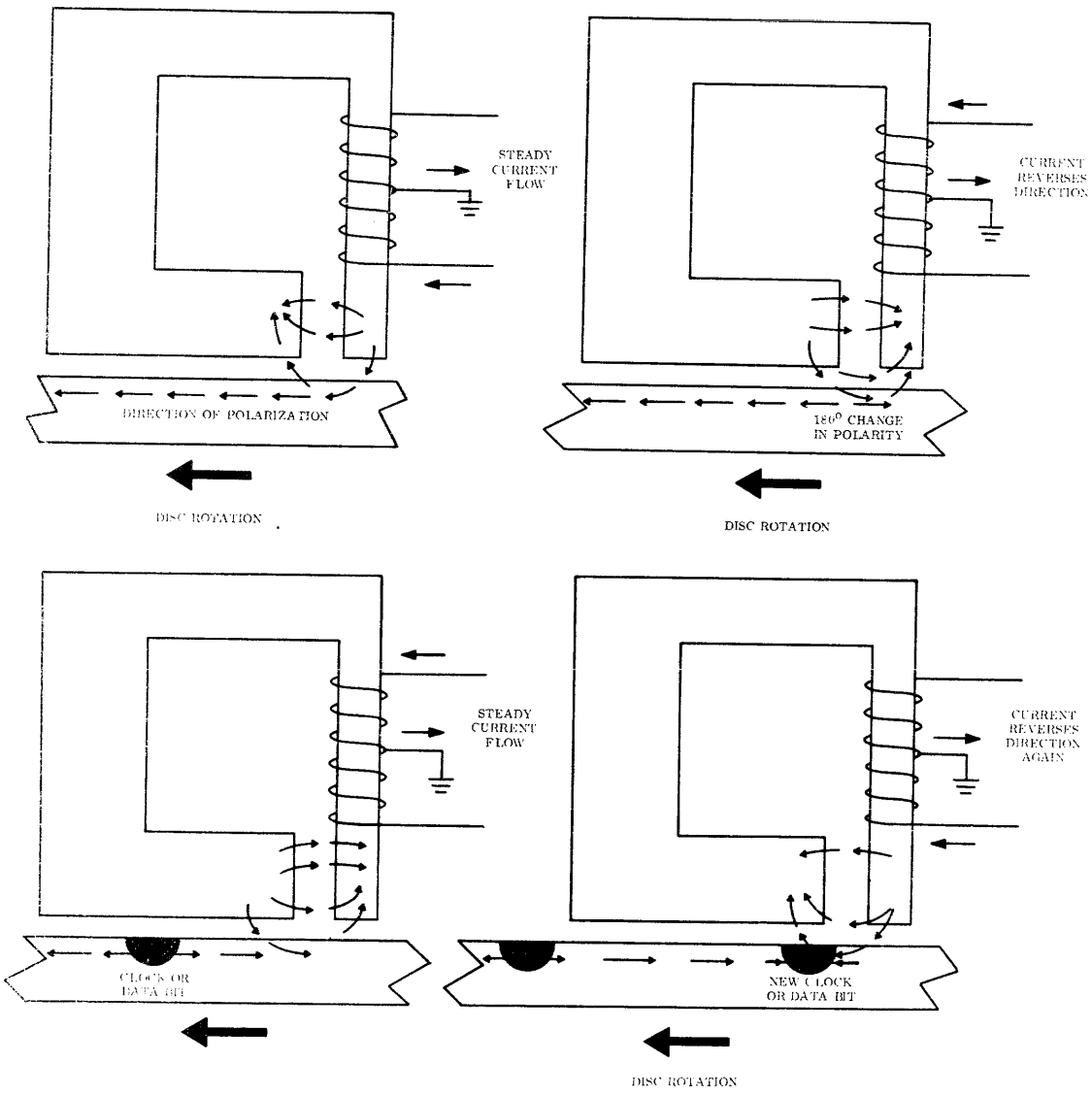


Figure 2-3. Bit Generation by Flux Reversal

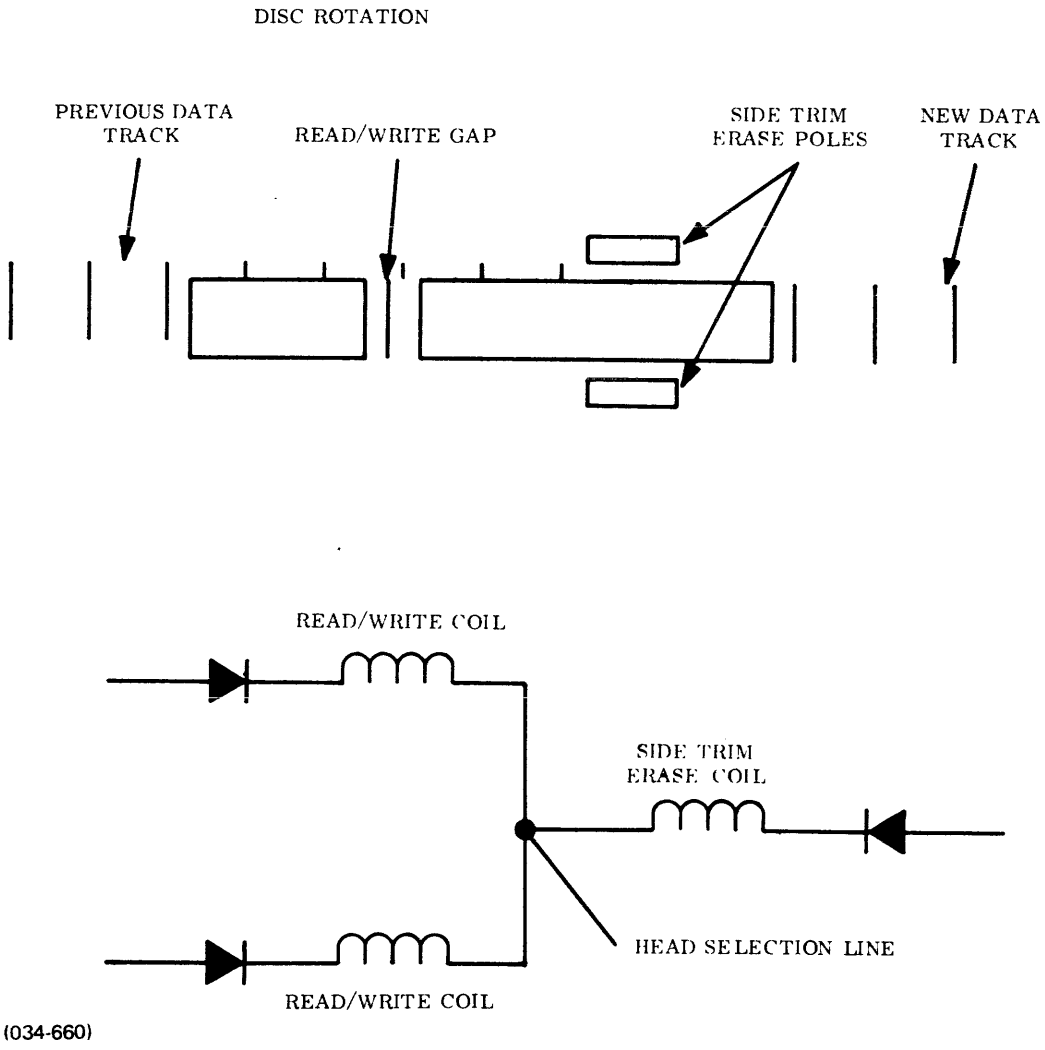


Figure 2-4. Side Trim Erase Concept

The coil on the erase poles is actually a pair of series-wound coils which are connected to the read/write coils in a Y configuration. The common point of these coils is tied to the head selection logic. See Figure 2-4. When the head is selected to write and erase (the common point goes low), direct current is applied to the erase coils. The steady flux induced by the direct current eliminates any unwanted polarity reversals (bits) along the sides of the new data track.

In addition to clearing a band of disc surface on each side of the track, the side trim erase ensures a written track width of 0.007".

2.7.2 Read Operation

During a read operation, the selected head flies over a previously written data track. As a length of track that is magnetized in one direction passes under the read/write gap, the steady magnetic field of the track induces no voltage in the read/write coil. Therefore, no voltage output appears on the read/write coil leads. Whenever a bit passes under the gap, the direction of magnetic flux reverses under the read/write coil and a signal is induced into the read/write coil, providing a signal to the read preamplifier.

The read preamplifier differentiates this head output signal so that each voltage peak becomes a zero crossing. That is, in the output of the read preamplifier, the zero crossings represent data bits. This output goes to the read amplifier via line drivers.

The read amplifier filters and amplifies read preamplifier output. The amplified read signal is then limited to produce a square wave which is then shaped into a series of pulses of 70 ns duration. These pulses are replicas of the original clock and data pulses received from the control unit.

2.8 LOGIC DESCRIPTIONS AND THEORY

Descriptions of the individual logic boards are presented on the following pages. Maintenance Manual, Volume B contains the logic diagrams for each engineering change (EC) level in effect at the time the manual is published.

Where differences in the EC levels are significant, certain paragraphs within a description may be marked as applicable to a particular EC level only, or more than one logic description may be provided to ensure clarity. In all other cases, a single description applies to all configurations.

In order to select the proper description for a particular version of an assembly:

A. Check the EC level of the printed circuit board

B. Locate the drawing(s) in Maintenance Manual Volume B, applicable to the board design level

C. Locate and read the proper description while referring to the logic diagram.

2.8.1 Read/Write Gating (A01) (Use Read/Write Gating System Logic Diagram RW110.)

The 660-0 disc drive uses a single line for both transmitting and receiving data. That is, data to be written on the disc and data read off the disc flows on the same line. This is + Read/Write Data at pin C which is connected to the control unit. The read/write gating circuitry (top of print RW110) accomplished this as follows:

A. Read.

When reading the data off the disc, the data read enters as - Read Data at pin 2 and is routed to the read data driver. If the command signal + Read Gate from the control/safety logic is high, gate 1A-3 is enabled which enables gate 1A-6. This enables the read data driver to pass the - Read Data signal. This signal which is read off the disc leaves the board at pin C to the control unit.

B. Write.

Data to be written onto the disc enters the board from the control unit at pin C. It is routed to the write data receiver. If the command signal + Write Gate from the control/safety logic is high, gate 1A-11 is enabled which enables gate 1A-8, which in turn enables the write data receiver allowing the data to be written to leave the board as a - Write Data signal. This signal is amplified by the write amplifier on A09 before being written onto the disc.

2.8.2 Module Change (Use Read/Write Gating System Logic Diagram RW110)

When the unit number plug is inserted into its slot, the - Select Unit signal at pin S goes low. This causes the output of the module change amplifier 4A-6 to go high, triggering the pulse shaper. The pulse shaper generates a pulse (- Module Change) which sets the restore latch on the servo sequencer decode logic A04. This assures that a restore to cylinder 000 is performed whenever a new unit number plug is inserted into the operator control panel of the drive. The - Module Change pulse also sets the pack change latch which sends the status signal + Pack Change back to the control unit. A - Retract Heads command from the power up sequencing and control logic A08 can also set the pack change latch.

If the drive is Busy (+ Busy at pin 19 is high), the AND gate 2A-6 is blocked at its pin 5 and the + Pack Change signal cannot be generated. The drive is Busy when Seek Ready is high, On Line is high, and Seek Incomplete is high.

The purpose of the 13 μs single shot circuit (5A) is to delay the dropping of + Busy for 13 μs after + Unit Is Selected goes high.

2.8.3 Lamp Drivers (A02) (Use Lamp Driver System Logic Diagram CP200.)

Since all lamp drivers on A02 are basically the same, only one circuit will be described: the lamp driver which lights the FILE UNSAFE lamp on the operator control panel.

When the signal + File Unsafe (which enters on pin Y) is low, the output of the lamp driver circuit is high, thus preventing current from flowing through bulbs DS13 and DS14 and illuminating them.

When a file unsafe condition occurs in the drive (see Control Safety B07 logic description), the signal + File Unsafe goes high and the output of the lamp driver circuit goes low, grounding one side of the bulbs. Since the other side of the bulbs are connected to +24 RAW DC, they illuminate.

2.8.4 Servo Sequencer (A03) (Use Servo Sequencer System Logic Diagram SC130 and Servo Sequencer State Diagram AC100.)

The purpose of the Servo Sequencer logic board (A03) is to provide a set of signals to the Servo Sequencer Decode logic (A04) to initiate required operations such as a forward seek, reverse seek, restore; or to reset the CAR, PAR, or timers. Refer to the Servo Sequencer Decode (A04) description for a complete list of the conditions and operations initiated by Servo Sequencer Decode logic.

The control state signals are generated by four J-K flip-flops which comprise the state counter. In addition, a - Clear signal, which also serves as the direct reset input to the four flip-flops, goes to the On-Line and Attention latches on A04. The two conditions (set or reset) possible for each of the four J-K flip-flops provide 16 possible states that the system can assume. The 16 states are shown in the Servo Sequencer State diagram, AC110. Each circle in the state diagram represents one unique state and the four digits within each circle define the conditions of the four J-K flip-flops. These flip-flops will be called A, B, C, and D throughout this description. A logical 1 in the circle indicates that the corresponding flip-flop is set and a logical 0 means that it is reset. The list of callouts next to each circle represents the operation to be performed while the Servo Sequencer logic is in the given state. These output conditions are decoded by the Servo Sequencer Decode logic board (A04).

Transitions, or changes from state to state are represented by arrows on the state diagram. Callouts on each arrow indicate conditions that must be met to allow that specific transition. A closed loop (i.e., an arrow which begins and ends at the same state) indicates conditions which, when they are met, will cause the system to remain in that state. A set of Boolean equations which summarizes the prerequisites for each flip-flop's set and reset state is given at the end of this description.

All transitions, except those involving Seek Incomplete (T1 on state diagram) require that only one flip-flop change state. Thus, for each change of state arrow in the state diagram, there is a single gate on the Servo Sequencer logic board that will cause the particular flip-flop to change its state. For example, the transition from state 1 (0001) to state 5 (0101) occurs after the Forward Seek delay (T2) times out. This transition requires that the B flip-flop be set by a one on its J input. This logical function is fulfilled by NAND gate 1B-8 and NOR gate 1C-8.

Transfer of the flip-flops from one state to another is synchronized by the trailing edge of the - Strobe B (clock) pulse, which is inverted by 3D-8. The pulse is generated by the cylinder transducer oscillator and enters board A03 on pin 14. In the following discussion, it is assumed that the transfer in states does not occur until the next strobe pulse.

2.8.4.1 First Seek and Restore

During the 60-second warm-up delay, T5 signal, - Seek Enable, which arrives at A03 pin 21 as a high level, is inverted by 5D-11, NORed by 2D-11, and inverted again by 3D-6 to reset all four J-K flip-flops through their direct reset inputs. This low level leaves the board on pin 13 as the - Clear signal, which resets the Attention and On Line latches on the Servo Sequencer Decode logic board. In this state (0000), the CAR, PAR, and timers are reset. When T5 times out, - Seek Enable goes low which enables the Servo Sequencer logic. This initiates a restore sequence. This means first seek and restore are identical once the Servo Sequencer is enabled.

On the next strobe, flip-flop D is set by the inverted output of AND gate 2B-12 and NOR gate 2B-8, which are enabled because flip-flops A, B, and C are reset. The logic is now at state 0001 where the CAR and PAR are still reset but the timers are now enabled. The Seek Start and Restore-flip-flops on A04 are reset to prevent a new seek start or restore signal from entering the logic. The logic remains at state 0001 until + T2, the Forward Seek delay, times out. When + T2, which enters A03 on pin 11, goes high, AND gate 1B-8 is enabled and its output is NORed by 1C-8. This sets flip-flop B, bringing the logic to state 0101. This state results in the generation of the signal - Force Forward Slow, which goes to the adder

and speed decode logic. The logic will remain in this state until forward velocity is detected, at which time flip-flop D will be reset on the trailing edge of the next strobe pulse via AND gate 5D-8 and NOR gate 5A-8, resulting in state 0100.

When motion in the carriage is detected, the signal + Forward Velocity at pin 18 goes high, setting the forward flip-flop. Since + Forward Velocity may go true momentarily due to noise induced into the tachometer by the initial current surge into the linear motor, diode CR1 prevents the setting of the Forward flip-flop while the heads are retracted.

When the Forward flip-flop is set, AND gate 5C-6 and NOR gate 5D-6 sets flip-flop C. The logic is now at state 0110 and forward motion is being monitored. The CAR and PAR are no longer held reset. The logic will continue in this state until the carriage comes to rest against the forward stop. When forward motion is no longer detected, the Forward flip-flop is reset and AND gate 1A-6 and NOR gate 2B-8 sets flip-flop D so that the logic is at state 0111. Holding current is applied to the linear motor to hold the carriage firmly against the forward stop while a force count of 202 is entered into the PAR through the direct set inputs. The Forward Seek delay (T2) begins, and when it times out, AND gate 2B-6 and NOR gate 5B-8 sets flip-flop A. This causes the logic to move to state 1111.

This is the normal reverse seek state. Since CAR was cleared until state 0110 and PAR was preset to 202 in state 0111, a normal reverse seek to cylinder 000 is initiated. The Seek Start and the Restore flip-flops on A04 remain reset.

2.8.4.2 Reverse Seek

If T1 times out before the counter logic counts 202 cylinders, causing the adder to declare a compare condition, AND gates 4C-12, 4A-6, and 5D-8 will reset flip-flops B, C, and D respectively (this is one of the two transitions which involves a change of state in more than one flip-flop). Resetting flip-flops B, C, and D would put the logic into the seek incomplete (1000) state. If, however, a compare condition is reached before T1, the logic transfers to state 1101 because AND gate 4A-8 and NOR gate 3A-8 reset flip-flop C. The Seek Start and the Restore flip-flops on A04 are still reset.

2.8.4.3 Detent

The Servo Sequencer Decode logic A04 sends a + Detent signal to the detent actuator, allowing the detent pawls to begin dropping, and a - FWD Detent Velocity signal to the servo drivers on B04. It is still possible for T1 to time out and, if it does so while the logic is in state 1101, the logic will transfer to state 1000 (this is the second transition involving more than one flip-flop). During normal operation, the - FWD Detent Velocity signal on A04 will

cause the servo to reverse the polarity of the motor current and the carriage to reverse its direction of travel. Forward motion sensing logic will then detect the forward movement of the carriage, causing the logic to transfer to state 1100. This occurs when AND gate 5B-6 and NOR gate 5A-8 reset flip-flop D. No change in external conditions takes place at this time. The logic is waiting for one of two events to occur, which will determine which state the logic moves to next. If T1 times out before zero velocity (lack of forward motion) is detected, the logic will go to state 1000, the seek incomplete state. If the detent pawl engages the rack and stops the carriage before T1 times out, zero velocity is detected and the logic transfers to state 1110. AND gate 5C-6 and NOR gate 5D-6 set flip-flop C. In this state, the detent is in, the timers are reset, holding current is applied to the linear motor, and the Seek Start and Restore flip-flops on A04 are held reset. On the trailing edge of the next strobe, the logic moves to state 1010. AND gate 4C-8 and NOR gate 4C-6 reset flip-flop B. The detent is in and holding current keeps the carriage steady. The Ready delay, T4, starts. When it times out, AND gate 1D-6 and NOR gate 2D-6 reset flip-flop A, resulting in state 0010.

2.8.4.4 Ready

This is the ready state. The logic returns to this state after successful completion of any servo positioning operation. The Servo Sequencer Decode logic sends a Not Busy signal to the control unit and the timers are reset. Since the Seek Start and the Restore flip-flops on A04 are not held reset in this state, either one can be set by the control unit, taking the logic out of the ready state. A + Restore signal will reset flip-flop C through AND gate 4A-12 and NOR gate 3A-8. This transfers the system to state 0000, the first state of the Restore sequence described above.

2.8.4.5 Seek Start

A + Seek Start signal will enable AND gate 1A-8 and NOR gate 2B-8, setting flip-flop D. This will transfer the logic to state 0011. In this state, the logic is ready for a seek operation. When the cylinder address is set into the CAR (prior to starting a seek), the + Compare line indicates whether the address set into CAR is different from the present location of the carriage as stored in the PAR. If + Compare is high, the system is seeking the cylinder at which it is presently located. This causes the sequencer to return to the ready state (0010) through gates 5B-12 and 5A-8, resetting flip-flop D. If, on the other hand, - Compare is high, a seek is required. AND gate 3A-6 and NOR gate 5B-8 set flip-flop A, bringing the logic to state 1011. The delay timers (T1 through T4) are now running. If the + Carry line is high at this time, it will enable AND gate 1C-12 and NOR gate 1C-8, which will set

flip-flop B. This will cause the logic to transfer to the reverse state 1111, initiating a reverse seek. The sequence of states following state 1111 is described above.

2.8.4.6 Forward Seek

The carriage is still positioned at cylinder 000; however, the + Carry line is probably low, indicating a forward seek. In this case, the logic will wait until T2 times out. At this point, AND gate 5A-6 resets flip-flop C, resulting in state 1001. A forward seek to the address in the CAR is initiated. From this state, the logic can either continue on through the normal seek sequence by transferring to the detent state (1101) when a compare condition is reached or it can transfer to the seek incomplete state (1000) if T1 times out first. The sequence of states following state 1101 is described above.

2.8.4.7 Seek Incomplete

If the Seek Incomplete delay (T1) times out or if a File Unsafe condition occurs in states 1001, 1100, 1101, 1111, or 0101 a transfer occurs to the seek incomplete state (1000) as described above. In this state the timers are reset and a + Seek Incomplete signal is sent to the control unit. The Servo Sequencer Decode logic removes all its outputs to the servo and disables the servo driver. The Servo Sequencer logic awaits initiation of a Selected Unit Restore signal by the control unit. A - Restore signal, inverted by 2D-3, enables AND gate 1D-8 and NOR gate 2D-6 and allows the system to transfer to state 0000, which is the first state of the restore sequence described above.

SUMMARY OF PREREQUISITES FOR SET AND RESET STATES OF FLIP-FLOPS

$$J_A = (\text{T1 FF} \cdot \overline{C} \cdot D) + (\overline{\text{COMPARE}} \cdot \overline{B} \cdot D \cdot C) + (D \cdot C \cdot \text{T2})$$

$$K_A = (\text{T4} \cdot C \cdot \overline{D} \cdot \overline{B}) + (\overline{B} \cdot \overline{D} \cdot \overline{C} \cdot \text{RESTORE})$$

$$J_B = (\text{COMPARE} \cdot \overline{\text{T1 FF}} \cdot D \cdot A) + (A \cdot D \cdot \text{CARRY}) + (D \cdot \overline{A} \cdot \overline{C} \cdot \text{T2})$$

$$K_B = (A \cdot C \cdot \overline{D}) + (\overline{C} \cdot \text{T1 FF})$$

$$J_C = (\overline{\text{FWD FF}} \cdot \overline{\text{T1 FF}} \cdot D \cdot B) + (B \cdot \overline{D} \cdot \overline{A})$$

$$K_C = (\text{COMPARE} \cdot A \cdot D) + (D \cdot A \cdot \text{T1 FF}) + (D \cdot A \cdot \text{T2} \cdot \overline{B}) + (\overline{B} \cdot \overline{A} \cdot \text{RESTORE})$$

$$J_D = (\overline{\text{FWD FF}} \cdot B \cdot C \cdot \overline{A}) + (\overline{A} \cdot \text{SEEK START} \cdot \overline{\text{RESTORE}} \cdot \overline{B}) + (\overline{A} \cdot \overline{B} \cdot \overline{C})$$

$$K_D = (\text{T1 FF} \cdot A) + (\overline{B} \cdot C \cdot \text{COMPARE}) + (\overline{C} \cdot B \cdot \text{FWD FF})$$

2.8.5 Servo Sequencer Decode (A04) (Use Servo Sequencer Decode System Logic Diagram SC140.)

The Servo Sequencer Decode logic on A04 decodes the four output signals of the Servo Sequencer logic into signals to be used by various logic systems in the drive. Some are also sent to the control unit as status lines.

The four Servo Sequencer signals (-A, -B, -C, and -D) which originate at the $\overline{Q}$ outputs of the four JK flip-flops on A03 enter A04 at pins 4, 5, 8, and 9, respectively. They are then inverted by inverters 1D-2, 1D-12, 1D-10, and gate 2D-11. The outputs of these inverters are again inverted, resulting in a total of eight outputs. These outputs are labeled +A, +B, +C, +D, -A, -B, -C, and -D, and go in various combinations to the set of positive NAND gates and one positive NOR gate which comprise the decode logic (upper right and lower right-hand section of print). Some gates use only two of the signals as inputs, while others use three or four. Two multiple input gates also use the set outputs of the Seek Start latch and the Restore latch. These latches store the control unit Seek or Restore commands during execution. When the signals - Selected Unit Control and + Unit Bus 2 become active, the Seek Start latch is set. The Restore latch sets on - Selected Unit Control and + Unit Bus 6. When the necessary combination of inverter outputs are high, a particular gate or gates will be enabled. The output of the gates which are enabled goes to other logic in the drive and/or to the control unit. For example, if the input lines to inverters 1D-2 and 1D-10 are both high, while the inputs to inverters 1D-12 and 2D-11 are low, the eight inverter outputs will be in these states: -A, +B, -C, and +D are high and +A, -B, +C, and -D are low. This combination of levels will not enable gates 4D-1 and 3D-11. Gate 4D-1 resets the Seek Start and Restore latches and sets the Attention latch. Gate 3D-11 generates the signal - Force Fwd Slow. Other outputs from the Servo Sequencer Decode board include:

A. - Holding Current

When this line is low, holding current is applied to the positioning motor, keeping a light force on the carriage in the forward direction against the engaged detent pawl.

B. - FWD Detent Velocity

This line goes to the operational amplifiers in the servo to select the proper current value for the positioning motor to move the carriage forward at detent velocity.

C. - Seek Forward

This line goes to the Adder and Speed Decode logic to enable the forward direction adder gates.

D. + Seek Forward

This line goes to the PAR to enable the counter to count up during a forward seek.

E. - Seek Reverse

This line goes to the PAR to enable the counter to count down during a reverse seek.

F. + Seek Reverse

This line goes to the Adder and Speed Decode logic to enable the reverse direction adder gates.

G. - Force Fwd Slow

This line goes to the Adder and Speed Decode logic to simulate an address difference of 4 and select the corresponding forward velocity.

H. - Force Count

This line goes to the direct set inputs of the PAR flip-flops to force in a present address of 202 to the Control Safety logic to generate a signal which resets the head register, and to the Cylinder Transducer Amplifier board to prevent the cylinder transducer from generating count pulses.

I. + Seek Ready

This line goes to the Control Safety logic to partially enable the gate which generates a - Set Cylinder Signal. It also goes to the control unit as a status line.

J. + Seek Incomplete

This line goes to the Index/Upspeed logic to turn off the READY lamp driver and to disable the servo. It also goes to the control unit as a status line in addition to being used by the Servo Protection logic B02.

K. + Seek Start

This line goes to the Servo Sequencer logic as one of the condition lines which change the states of the four state flip-flops.

L. - Restore

This line goes to the Servo Sequencer logic as one of the condition lines which change the states of the four state flip-flops.

M. + On Line.

This line goes to the control unit as a status line.

N. + Attention

This line goes to the control unit as a status line.

Not all the outputs of the Servo Sequencer Decode board are conditioned by the eight inverter outputs. The two latches discussed earlier are responsible for the signals + Seek Start and - Restore. + Seek Start is generated at the set output of the Seek Start latch when it is set by + Unit Bus 2 going high during the control cycle (Unit Bus 2 is + Seek Start during the control cycle). - Restore is generated at the set output of the Restore latch when it is set by + Unit Bus 6 going high during the control cycle. Both latches are enabled by an inverted - Selected Unit Control.

The On Line latch is held reset by the signal - Clear until the 60-second warm-up delay times out. During this period, the signal + On Line is low, indicating to the control unit that the disc drive is not on line. The On Line latch is also held reset if the signal + Enable is low (ENABLE-DISABLE switch in the DISABLE position). + On Line goes high when the On Line latch is set. This occurs when the output of 3C-8 goes low (in the READY state with Seek Start false). A high + On Line informs the control unit that the drive is on line.

The Attention latch is also held reset by the signal - Clear until the 60-second warm-up delay times out. The signal - Reset Attention initiated by the control unit can also reset the Attention latch. When signals +D and +B satisfy gate 4D-1, the Seek Start and Restore latches are reset and the Attention latch is set. However, the signal + Attention is not gated to the control unit because gate 5B-12 is disabled. Gate 5B-12 is enabled when gate 3C-8 is satisfied upon entering the READY state, 0010.

2.8.6 Adder and Speed Decode (A05) (Use Adder and Speed Decode System Logic Diagram SC120.)

The Adder and Speed Decode logic (A05) detects the difference between the contents of the CAR and the PAR. If the registers have identical contents, the Compare signal is enabled. If the register contents are different, the logic generates outputs to the Servo Control board (B04) which determine the direction and velocity at which the access mechanism must move in order to move the heads to the address contained by the CAR. Once it is determined for a particular seek the direction output signal, Carry, remains fixed for the duration of the seek. However, the velocity outputs are continually updated during the time the seek is in progress. This allows the specification of an optimum velocity profile which positions the heads to their required location in the least possible time consistent with the limitations of

power into the servo and the mechanical constraints of the positioning and detenting mechanisms. Since the PAR operates as a counter during a seek, its contents will change as each new cylinder position is reached until, at the required cylinder, PAR and CAR contain equal addresses.

The logic signals used by the compare circuit and by the speed decode circuits are the outputs of an 8-bit adder. This adder is implemented with eight full adder elements, labeled 8-Bit Adder on the print. The inputs to the adder are the true outputs of the PAR and the complement outputs of the CAR. The carry out of the most significant bit of the adder (128) determines the sign of the difference and, thus, the direction of motion required to move the heads to the required address. When the signal Carry is true, the reverse direction is specified. To provide the required adder operation when the PAR contents are greater than the CAR contents, a carry is inserted into the least significant bit of the adder. This function is accomplished by connecting the Seek Reverse signal (from the Servo Sequencer Decode board) to the least significant bit carry in of the 8-bit adder.

When reverse movement is required (the signal Carry is true), the complement of the sum outputs of the adder are used by the compare logic and the speed decode logic; for the forward direction, the true sum outputs are used. The selection of true on complement is done by the signals + Seek Reverse and - Seek Forward. These signals are used in the selection function depending on whether the true or complement output signal is required. For the compare function, the eight input AND gate 4D-8 makes the compare for forward seeks. Its output is selected by negative AND gate 4B-10 when the signal + Seek Reverse is false (which implies Seek Forward is true). For reverse seeks, the eight input AND gate 4C-8 makes the compare using complement adder outputs. Its output is selected by the signal - Seek Reverse at negative AND gate 4B-13. Positive OR gate 5D-4 combines the forward and reverse compare outputs to provide the required output signal - Compare.

The speed decode logic is designed to generate a series of signals to be used by the D - A Converter on the Servo Control board. For the four higher order velocities (both forward and reverse) the object is to have only one line of the four true for any particular difference. For instance, the Reverse Velocity 5 signal is true when the difference is 16 cylinders or greater and no higher order reverse velocity signal is true.

The lower order velocity signals (1, 2, and 3) are the algebriac difference between the contents of the CAR and PAR except for Reverse Velocity 1 which is enabled only when the difference is exactly one cylinder. Figure 2-4A shows the decoded velocity outputs for differences of 0 through 202, both positive and negative.

There are two logic inputs to the board which force a particular velocity output independent of the contents of the address register. Force Forward Slow, the signal true during

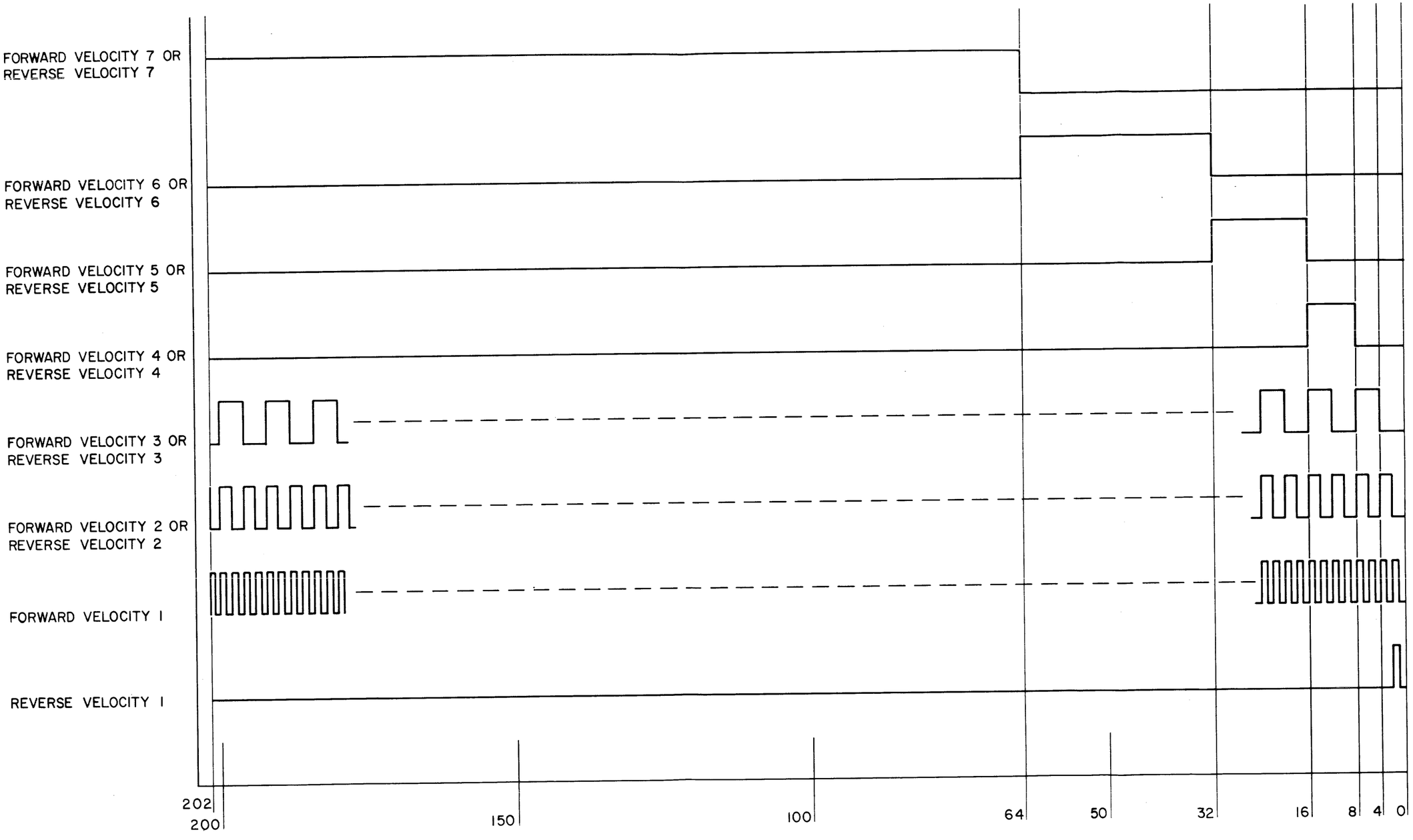


Figure 2-4A. Speed Decode; Velocity vs CAR-PAR Difference

the forward portion of a restore operation, will cause a Forward Velocity 4 signal to be enabled. Retract Heads, generated in the Power Up Sequencing and Control Logic, will cause a Reverse Velocity 4 signal to be enabled to assure that the heads are retracted from the pack when the spindle drive motor is turned off.

2.8.7 Cylinder/Present Address Register (A06) (Use Cylinder/Present Address Reg. System Logic Diagram SC110.)

The CAR receives the cylinder address from the control unit and stores it for comparison by the Adder and Speed Decode (A05) logic. This address represents the cylinder to which the heads must be positioned.

The PAR counts the pulses from the cylinder transducer amplifier (B06) and gives an electrical indication of the present head position to the Adder and Speed Decode logic. It also sends its outputs to the present address indicator lamps on the operator control panel. If the CAR and PAR outputs are identical, the heads are at the desired cylinder. If these register outputs are not identical, the servo in the drive moves the heads until the pulses received from the cylinder transducer amplifier change the present address to equal the cylinder address, hence the heads become positioned to the desired cylinder.

2.8.7.1 Cylinder Address Register

The CAR consists of eight D-type flip-flops: 1, 2, 4, 8, 16, 32, 64, and 128. It receives its input instructions at the D inputs of the flip-flops from the control unit when the signal - Set Cylinder goes low via unit bus lines 7, 6, 5, 4, 3, 2, and 1, respectively. The Q outputs of the flip-flops (+ outputs) go back to the control unit through line drivers for confirmation that the proper address was received. The $\overline{Q}$ outputs (- outputs) are routed to the Adder and Speed Decode circuitry. Bit 128 is also inverted and sent to the Write Logic (A09).

2.8.7.2 Present Address Register/Counter

The PAR consists of eight D-type flip-flops with a counter circuit. The register/counter can either add to or subtract from the register's present contents with each - Cyl Count signal. The counter counts up or down depending on whether the signal + Seek Forward or - Seek Reverse is active.

In preparation for the reverse portion of a restore operation, the PAR is directly set by - Force Count to a count of 202 (note that register/counter elements 2, 8, 64, and 128, a total of 202, are directly set by - Force Count). In this operation the PAR is first reset by + CAR/PAR Reset. Since the direct set inputs of the 1, 4, 16, and 32-bit register

flip-flops are not connected to - Force Count, and therefore cannot be reset, the signals + PAR 1, + PAR 4, + PAR 16, and + PAR 32 are low. The low signal - Force Count causes the remaining PAR signals to be high, resulting in a weighted value of 202.

2.8.7.3 Up-Count Operation (Present Address Register)

Assuming all the D flip-flops in the PAR are initially reset (cylinder 000) and the signal + Seek Forward is active, the register/counter is ready to count. On the first - Cyl Count pulse from the cylinder transducer amplifier, register/counter 1 sets and the signal + PAR 1 is generated. On the next - Cyl Count, register/counter 1 resets and register/counter 2 sets and the signal + PAR 2 is generated. The next - Cyl Count causes + PAR 1 and + PAR 2 (binary weight of 3) to be generated and so on.

2.8.7.4 Down-Count Operation (Present Address Register)

For down-count operation of the PAR register/counter, the - Seek Reverse signal must be active. Then with each - Cyl Count pulse the register/counter counts down by 1.

2.8.8 Head Selection and Register (A07) (Use Head Selection and Register System Logic Diagram RW100.)

The Head Selection and Register logic receives the head address information from the control unit and stores it in the head register. The output of the head register is decoded into - Line Select signals which activate the desired read/write head to either read or write. The logic on this board is also used to generate the safety signals - Head Select Error and + End of Cylinder.

The reset outputs of each flip-flop in the head register/counter (except bit 1) go to an AND gate. These AND gates are also conditioned by the signal + Select Head. If + Select Head is high, the set and reset outputs of the four head register flip-flops are gated to the Line Select decode circuit 4D BCD/DEC which generates the 10 - Line Select signals.

The inputs to the Line Select decode circuit consist of various combinations of the inverted set and reset outputs of the head register flip-flops (excluding bit 1). Depending on which flip-flops are set by the + Unit Bus and + Set Head lines, one of the 10 - Line Select lines will be selected.

Each - Line Select line is capable of partially enabling two read/write heads. One of each pair of heads is gated by a set of read, write, and erase signals called - Read (Left), - Write (Left), and - Erase (Left). The other head in each pair is gated by a similar set of

signals called - Read (Right), - Write (Right), and - Erase (Right). Thus, if - Line Select 5 is low while the signals - Write (Left) and - Erase (Left) are low, the (Left) head on - Line Select 5 will write and erase.

Each of the 20 heads is selected by a combination of: one of the 10 - Line Select lines and one or two of the (Left) or (Right) lines (one line if the head must read and two lines if it must write and erase). This technique uses what is known as 2 by 10 matrix selection. The 20 heads are classified in two groups of 10: one group of 10 (Left) heads and one group of 10 (Right) heads.

The (Right) heads are selected with the three signals: - Read (Right), - Write (Right), and - Erase (Right). The (Left) heads are selected with the three signals: - Read (Left), - Write (Left), and - Erase (Left). These signals determine whether the (Right) or (Left) heads read, or write and erase. For instance, to accomplish reading on the (Right) heads, the signal - Read (Right) must be low. For the (Right) heads to write and erase, the signals - Write (Right) and - Erase (Right) must be low. Similar requirements apply to the (Left) heads.

Selection of the three (Right) signals instead of the three (Left) signals depends on the relative states of the bit 1 and bit 2 flip-flops of the head register. If both flip-flops are in the same state (both set or both reset), the 2D-8, 2D-3, and 2D-6 gates are partially enabled. If the states of the two flip-flops are different (bit 1 set and bit 2 reset, or bit 1 reset and bit 2 set), the 1D-6, 1D-11, and 1D-8 gates are partially enabled. To summarize, the trio of (Right) gates is partially enabled when the states of the bit 1 and bit 2 flip-flops are the same, and the trio of (Left) gates is partially enabled when the states are different. The signal + Left Select also leaves the board if the (Left) gates are partially enabled.

Selection of read, write, and erase functions is the responsibility of the three input lines: + Read Gate, + Write Gate, and + Erase Gate. Each signal partially enables two gates, one in the trio of (Right) gates and one in the trio of (Left) gates. For example, if + Read Gate is high while the (Right) gates are partially enabled, the signal - Read (Right) is generated. The signal - Read (Right) goes to the Read Amplifier board (A10) where it enables appropriate circuitry for (Right) side operation.

It should be remembered that a write operation must always be accompanied by an erase operation. For example, when + Read Gate is high, + Write Gate and + Erase Gate are both low. When + Write Gate is high, Erase Gate must also be high and + Read Gate is low.

All inputs to the head register are blocked by the output of gate 5C-13 when either + Read gate or + Erase gate is high at the input of OR gate 2B-4 and + Index is low at the input of gate 5C-10. This condition disables gate 5C-10 which results in the blocking of + Head Advance, + Set Head, and + Reset Head Reg, respectively. The output of gate 4B-6 blocks the Unit Bus signals.

2.8.8.1 Head Advance

The S_D inputs of the flip-flops 1, 2, 4, 8, and 16 in the head register are derived from the + Unit Bus lines 7, 6, 5, 4, and 3, respectively. The head register operates as a five-stage binary ripple counter when the signal Reg Adv at input C of flip-flop 1 is pulsed. If none of the head register flip-flops are directly set by the Set signals at their S_D inputs, the head register will count each time a Reg Adv pulse is applied to flip-flop 1. The head register will count until the maximum head address is reached (10011 in binary or 19 in base 10).

When a head selection is programmed, one of the Set signals at the direct set (S_D) inputs of the head register flip-flops is active, and the head register will only count until it reaches that directly set flip-flop. Then the outputs of the head register flip-flops partially enable the decoding gates which consist of gates 5B-11, 5D-6, 5D-3, and 4B-11. When the signal + Select Head which enters the board on pin F goes high, it enables the proper decoding gates. The outputs of the decoding gates are further decoded into the proper - Line Select signal which helps activate the desired read/write head.

2.8.8.2 End of Cyl/Head Select Error

Two other signals are generated on this board in addition to the Line Select signals and the (Left)(Right) signals. They are + End of Cylinder and - Head Select Error. The signal + End of Cylinder informs the control unit when the drive has advanced to head address 20 or beyond. The signal - Head Select Error goes to the Control/Safety logic (B07) if an unsafe (to the disc) condition exists within the logic or its programming.

When the head register has advanced to a numerical value which enables - Line Select 9, the high Q output of the bit-16 flip-flop partially enables AND gate 1C-8. Other inputs to AND gate 1C-6 are + Unit Is Selected and the output of NOR gate 5B-8 which is active whenever the bit-4 or bit-8 register flip-flop is set. The $\overline{Q}$ output of the bit-16 flip-flop helps generate the signal - Sixteen.

The next Reg Adv pulse after - Line Select 9 has been activated sets flip-flop 1. The following Reg Adv pulse resets flip-flop 1 causing flip-flop 2 to reset. This in turn causes flip-flop 4 to set, and its low $\overline{Q}$ output enables OR gate 5B-8. The high output of 5B-8 enables gate 1C-8 whose output is inverted by 5D-11 to become + End of Cylinder.

Exceeding the legal head address and attempting to select a head is considered a head selection error. For that reason, the low out of 1C-8 enables another OR gate 1C-6. If the + Select Head line is high at this time, it enables AND gate 5D-8 generating the signal - Head Select Error.

The - Head Select Error signal is also generated when both - Erase (Left) and - Erase (Right) lines, or both - Write (Left) and - Write (Right) lines are selected simultaneously (a condition only possible if there is a circuit failure). Either of these conditions will satisfy OR gate 1C-6 which causes AND gate 5D-8 to generate the signal - Head Select Error. Again, this assumes that the signal + Select Head is active. The - Head Select Error signal goes to the Control Safety logic to help generate a - File Unsafe signal.

2.8.9 Power-Up Sequencing and Control (A08) (Use Power-Up Sequencing and Control System Logic Diagram SL110 and Sequencing In and Out System Logic Diagram SL100.)

The Power Up Sequencing and Control and Sequence In and Out logic A08 prevents simultaneous starting of two or more drives in a multiple drive system. Since the starting current of the spindle drive motor is much higher than the running current, simultaneous starting of drives could result in a power line overload. If a unit in a string of units has its primary power turned off, circuitry on A08 causes that unit to be bypassed. The Power Up Sequencing and Control logic provides a 60-second delay after the spindle drive motor reaches operating speed to allow the disc pack temperature to stabilize before generating signals needed by the Control Safety, Servo Sequencer, and Index/Upspeed logic. Other signals generated by the Power-Up Sequencing and Control logic are used by the Servo Sequence Decode and Adder/Speed Decode logic. Signals are also generated for use by the cylinder transducer amplifier and the control unit. Finally, the retract heads signals and the 15-second dynamic braking signals originate in the Power-Up Sequencing and Control logic.

In the following discussion, these conditions are assumed to exist unless noted otherwise (see Power-Up Sequencing and Control System Logic Diagram SL110).

A. The Door Closed-Door Open switch is in the Door Closed position enabling the Door Closed latch and causing pin 1 of gate 5C-12 to be high.

B. A disc pack is installed on the unit.

C. The Main Power switch S1 on the Interior Control Panel is on, providing the necessary dc voltages for logic and relay operation.

D. The Heads Extended-Heads Retracted switch is in the Heads Retracted position resetting the Heads Extended latch and causing a low signal on pin 9 of gate 5C-8 and a high signal on pin 9 of gate 4B-10 and pin 1 of gate 4B-3. The Heads Retracted

position also puts a high signal on pin 6 of gate 4A-4, enabling it. Its low output partially enables AND gate 4A-1.

E. The START-STOP switch on the operator control panel is in the START position causing a high signal on pin 13 of gate 5C-12 and pin 1 of gate 4C-3, and a low signal on pin 2 of gate 4B-3.

2.8.9.1 Power-Up

If the disc drive is one unit in a string of several, the individual units must be automatically powered up one at a time to prevent power line overloading. The first drive to power up provides a sequence signal to the second drive so that it can power up. When it powers up, it provides a sequence signal to the third drive so that it can power up. This sequencing continues until the last drive in the string is supplied with the sequence signal.

In the following discussion it is assumed that the disc drive is the first one in a string and provides a sequencing signal to the next drive in the string.

When the initial power is turned on and while current is building up in the coil of the Sequence Bypass Relay K1 (see Sequence In and Out System Logic diagram SL100), the Sequence Latch is held reset by the ground through CR-6 and a K1 relay contact. This signal, called Power Up Reset, is also used by the Line Drivers, Hi Low Voltage Detector, and Control Safety logic. As soon as K1 opens, the forced reset condition on the Sequence latch is removed.

When the control unit generates the signals + Sequence In and Controlled Ground, the Sequence In Relay K3 energizes. This causes the Sequence Latch to set, its output going high. This high signal is applied to pin 5 of gate 4C-6 (see print SL110), partially enabling it, and to pin 2 of gate 5C-12, enabling it. The low output of gate 5C-12 is inverted by gate 4A-1 causing the command signals - Retract Heads to be inactive. The output of gate 4A-1 also enables OR gate 5A-4, whose low output is inverted by gate 5B-6. The high out of gate 5B-6 turns on transistor Q1. Q1 furnishes a ground path for the running time meter and spindle drive motor relays. The spindle drive motor relay energizes and applies primary ac voltage to the spindle drive motor. The motor starts and causes the spindle and disc pack to begin rotating.

When the spindle drive motor reaches 70% of its operating speed, the signal + Up Speed goes high. It is inverted by gate 5B-8 and routed to the input of OR gate 4C-3 causing its output to go high enabling gate 4C-6, generating the signal + Sequence Out which causes the signal - Sequence Out Dvr on print SL100 to go low. This energizes the Sequence Out relay K4 which generates the + Sequence Out to the next drive on the string. The next drive begins its power up sequence.

The low signal out of gate 5B-8 (see print SL110) is also applied to one input of AND gate 5A-1. The other input of AND gate 5A-1 went low at the same time Q1 turned on. Gate 5A-1 is enabled and its output goes high, is inverted twice by gates 5A-10 and 5A-13, and applied as a high level at the input of the 60-second delay circuit and to pin 13 of gate 5B-11. The delay circuit starts. Sixty seconds later, pin 12 of gate 5B-11 goes high, enabling it. The low output of gate 5B-11 is applied to OR gate 5B-3 enabling it, generating the signals + Seek Enable and - Seek Enable. These signals go to the Control Safety, Servo Sequencer, and Index/Upspeed boards to enable the logic on those boards to perform their respective functions in a first seek sequence. When the heads start to move into the disc pack, the Heads Extended-Heads Retracted switch moves to the Heads Extended position. The output of the Heads Extended latch reverse. This causes pin 6 of OR gate 4A-4 to go low; but since pin 5 remains high (+ Up Speed signal is still present), the signals + Retract Heads and - Retract Heads remain inactive. The Heads Extended position of the switch also causes a low signal to be applied to pin 9 of AND gate 4A-10. This enables gate 4A-10 because the other input to this gate is the - Seek Enable signal, which is low. The high output of gate 4A-10 is routed to gate 5A-4 to keep the disc pack motor running and to gate 5A-10 to assure that the two seek enable signals remain active.

If no ac power is applied to the disc drive just discussed (S1 on the interior control panel is OFF) the Sequence Bypass Relay K1 does not become energized. However, the Sequence Out Relay K4 still becomes energized (by Sequence In power) but without any up-speed delay. The drive accomplishes this as follows: (1) the power to the Sequence In Relay K3 is applied from the control unit or the previous drive, and it is energized, (2) since the Sequence Bypass Relay K1 is not energized, its upper set of contacts in addition to contacts 4 and 7 of K3 supply a Controlled Ground (through CR15) to pin B of the Sequence Out Relay K4, thus energizing it. The signal + Sequence Out is sent to the next drive with no delays. In other words, a drive without ac power is bypassed in the power up sequencing.

If a disc pack drive unit in a string of units has its START-STOP switch in the STOP position, pin 1 of gate 4C-3 is low, enabling that gate. The high output of gate 4C-3 partially enables AND gate 4C-6. When the Sequence Latch is set (+ Sequence latch high), either by the control unit or by a preceding disk pack drive unit, gate 4C-6 is enabled and its output goes low. This signal is inverted by gate 4C-8, generating the signal + Sequence Out which causes a Sequence Out signal to be routed to the next drive in the string.

In this STOP position, the disc pack motor never starts running because pin 13 of gate 5C-12 is low, generating the command signals + Retract Heads and - Retract Heads. Since the heads are retracted, pin 9 of gate 4A-10 is high causing its output to be low. Negative NAND gate 4A-1 is disabled and the transistor Q1 is turned OFF. This means primary ac power is prevented from being applied to the spindle drive motor.

2.8.9.2 Power-Down

To power down the unit, the START-STOP switch is placed in the STOP position. The start latch resets and pin 2 of AND gate 4B-3 goes high, partially enabling it. Pin 13 of AND gate 5C-12 goes low, disabling it and causing its output to go high. This high signal is inverted by gate 4A-1 and the command signals + Retract Heads and - Retract Heads become active. The heads begin to retract and the Servo Sequencer logic A03 is reset to state 0000. When the heads are fully retracted, the Heads Extended-Heads Retracted switch changes to the Heads Retracted position. The Heads Extended latch resets and pin 9 of gate 4A-10 goes high disabling it. Its output goes low and disables gate 5A-4. The output of gate 5A-4 goes high turning transistor Q1 off. K2, the motor relay, switches the spindle drive motor leads from primary ac voltage to the dynamic braking circuit. The Heads Retracted position of the switch also causes pin 1 of AND gate 4B-3 to go high, enabling it. This signal is inverted by gate 4B-6 and the 15-second delay circuit begins timing out. For 15 seconds, gate 4B-8 is enabled and dynamic braking current is applied to the spindle drive motor, stopping it. See the Delay Timer logic description for a detailed description of the time delay circuits.

The control unit powers down a string of units by removing the Controlled Ground signal, which de-energizes the sequence in relay K3, and resets the Sequence latch. The low output of the Sequence latch disables gate 5C-12 which causes the Retract Heads signals to become active. The heads retract and Q1 turns off. Dynamic braking is not applied in this case so the spindle drive motor coasts slowly to a stop.

If the operator cover is opened while the machine is running, pin 1 of gate 5C-12 will go low, disabling it. The heads will retract and the motor and meter relay will be disabled. Dynamic braking will not be applied in this case.

The READ/WRITE-READ ONLY, the ENABLE-DISABLE, the START-STOP, and the Door Open-Door Closed switches are connected to interface latches as shown. The RC/latch combination acts as an antibounce circuit by holding its output until the switch arm contacts the opposite side. The Heads Extended-Heads Retracted switch antibounce circuit contains diodes CR2 and CR10. CR10 prevents resistors in the antibounce circuit from activating Q1 on the Servo Control board when the Heads Extended-Heads Retracted switch is closed.

If the READ/WRITE-READ ONLY switch is placed in the READ ONLY position, R1 is grounded and the Read Only latch is set; pin 13 of gate 3D-11 goes high and pin 1 of gate 3D-3 goes low. If the signal - Unit Is Selected is inactive (high) gate 3D-11 is enabled and its output goes low. The second Read Only latch is set and the signal + Read Only goes high. This signal is sent back to the control unit and to the READ ONLY indicator on the operator control panel. The READ ONLY indicator illuminates. The ENABLE-DISABLE switch controls the Enable latch in a similar fashion.

If the unit is selected (-Unit Selected is low) the READ/WRITE-READ ONLY and the ENABLE-DISABLE switches have no effect while the unit is performing an operation.

2.8.10 Write Logic/Read Amplifier (A09/A10) (Use Write Logic System Logic Diagram RW120, Read Amplifier System Logic Diagram RW140, and Read/Write Amp Left and Right System Logic Diagram RW130)

The data to be written onto the disc pack (- Write Data) is routed from the Read/Write Gating board (A01 print RW110) to pin 2 of the Write Logic board (A09 print RW120). This data, in the form of pulses, passes through the driver and into the Write flip-flop. The output of the flip-flop is amplified by a differential amplifier whose push-pull output (+ Write Data and - Write Data) is sent out of pins 4 and 3 to the Read/Write Amp (Left) and the Read Write Amp (Right) as indicated on the Read/Write Amp Left and Right System Logic Diagram print RW130.

Because the write data is sent to both left and right read/write amps simultaneously, provision must be made for selecting either the left or right amplifier.

The left column of heads and its associated circuitry is a mirror image of the right column of heads and its associated circuitry. Therefore, only the operation of the right column of heads will be discussed in detail.

So that the right column of heads can write, the signal - Write (Right) which enters pin D of the Write Logic (A09 print RW120) from the Head Selection and Register logic must be active. Applying a low level to gate 2D-4 turns it on which causes the current driver (I Drv) to generate the signal + Write I (Right). This signal goes to pin D of the Read/Write Amp (Right) board (print RW130) to enable the write current driver.

The write data which was sent out from pins 4 and 3 of the Write logic enters the Read/Write Amp (Right) at pins B and C respectively. This data is routed to the appropriate gating diodes to the selected head. Which one of the heads is selected depends on which one of the Line Select signals is active. The data is written onto the disc surface facing the selected head.

When the drive is writing (either left or right bank of heads), the Any Write Sense circuit detects either Write I (Right) or Write I (Left) and generates the Any Write I (Sense) signal at pin 20 which is used by the Write Select latch on the Control Safety board B06 and which is sent to the control unit as a status line. If both Write I (Right) and Write ((Left) become active at the same time, the signals are ANDed and activate the Two Write Sense circuit which causes - Two Write I (Sense) at pin 16 to become active. This signal sets the Multi Write latch on the Control Safety Board which causes the signal File Unsafe to become active.

If the CAR has been programmed to cylinder 128 or greater, the signal - CAR 128 which enters at pin C on the Write logic board is active. This results in the Level Set signal turning on, shunting some of the current supplied by the current drivers (I Drv). Thus, the magnitude of the signals + Write I (Right) and + Write I (Left) is less for the higher numbered (inner) cylinders of the disc pack. This is done because the heads fly closer to the disc surface and the bit density is greater at the inner cylinders, thus requiring reduced head current.

While the head is writing it must also be erased on both sides of the newly recorded track in order to remove any trace of previous information, which, because of head positioning tolerances, would otherwise remain and affect disc pack interchangeability. The signal - Erase (Right) at pin F of the Write logic accomplishes this by enabling the current driver which generates signal + Erase I (Right). This signal supplies the current to output pin 10 which connects to the right column of erase heads. The actual head selected for erase current is determined by the Line Select signals. The signal + Erase I (Left) which leaves the board at pin 9 is generated in similar fashion.

The fact that the drive is erasing is sensed by the Any Erase Sense circuit which generates the signal - Any Erase I (Sense) at pin 21 which is used by the No Erase I latch on the Control Safety board. If both Erase I (Left) and Erase I (Right) become active at the same time, the outputs of the erase current drivers (points TP7 and TP6) are ANDed and actuate the two Erase Sense circuit which causes - Two Erase I (Sense) at pin 6 to become active. This signal sets the Multi Erase latch on the Control Safety board which causes the signal File Unsafe to become active.

Under certain conditions it is necessary to prevent any writing on the disc. In these cases the Control Safety logic generates the signal - Write/Erase Inhibit, which enters the Write logic at pin H, turning on gate 2D-8. The write and erase current is shunted to ground, through CR7, CR8, CR9, and CR26, preventing it from entering the coil on the selected head.

When the drive is not writing, the signal + Write Gate entering at pin 7 is not active (low). This level is inverted causing the Clamp circuit to clamp both the signals Write I (Right) and Write I (Left).

A 4.1 μs single shot (S.S. 4.1 μs), activated by - Any Erase I (Sense) or - Any Write I (Sense) is used to detect short duration Write Gate or Erase Gate signals for diagnostic testing. Erase or Write Gate signals of duration less than 4.1 μsec will force true the two Erase I or two Write I signals respectively, causing the drive to enter the File Unsafe condition.

2.8.10.1 Read

Because the left column of heads and its associated read circuitry is a mirror image of the right column of heads and its associated circuitry, only the right column of heads is discussed.

The same head selection technique is used for reading as is used for writing. On the Read/Write Amp (Right) board (print RW130) the signal from the head is coupled through diode gates CR36 through CR39. The state of these diodes is determined by the Read Driver Q13 and Q14. When Q13 and Q14 are turned on, the diode gates are energized allowing the signal from the selected head to pass into Amp Q1 through Q6. The signal + Read Driver (Right), which enters the Read/Write Amp (Right) board on pin 13, controls the state of Q13 and Q14.

The signal read off the disc is amplified by Amp Q1 through Q6. The outputs of this differential amplifier are further amplified by two more differential amplifiers consisting of Q7/Q8 and Q9/Q10 (Q9/Q10 is a differentiator stage).

The output of Q9 and Q10 is applied via a four-transistor low-impedance coax driver (Q11, Q12, Q13 and Q14) to the Read Amplifier (A10 print RW140) as the signal Read Preamp Right. This signal enters the Read Amplifier on pins 20 and 21. The signal from the Read/Write Amp (Left) enters on pins 18 and 19. A diode selection gate Preamp Select, controlled by Q1, Q2, Q3, and Q4 chooses either the left or the right signal for amplification by the Read Amplifier. The signal + Left Select, which enters the Read Amplifier on pin 17, determines which diode will be turned on. If the signal + Left Select is low, the signal Read Preamp Right will pass and be routed to the 3.5 mc filter, four limiters, the pulse shaper, the gated detector, and the line driver Q27 to become - Read Data.

2.8.10.2 Other Circuits

In addition to the circuits described above, the Write logic board (A09 print RW120) contains the circuit for generating the signal - AC Write. The head inductance causes voltage

spikes at the Read/Write Amplifier (Right) when write current is switched. These pulses go to pin E of J21 (RW130) and are routed to the Write logic (A09 print RW120) pin 8 where they are amplified and changed from an ac signal into a dc level - AC Write (Sense) which is sent to the Control Safety logic. The time constant of the circuit is such that a steady stream of pulses at the 1F rate (2.5 MHz) is needed to generate the - AC Write signal.

The Read Amplifier (A10 print RW140) contains the line select drivers which receive their signals from the Head Selection and Register logic. These line select drivers supply the required voltage levels to the head select transistors on the Read/Write Amplifier boards. Each line select driver connects to two head select transistors, one on the Read/Write Amplifier Left and one on the Read/Write Amplifier Right.

2.8.11 System Protection (B02) (Use System Protection Logic Diagram SC155 and Servo Driver System Logic Diagram SC170)

The System Protection circuit protects the linear motor bobbin winding from overheating should the carriage fail to retract within 400 ms after Retract Heads has been commanded. Following this period the protection circuit limits the amount of current applied to the bobbin winding by clamping the signal Programmed Current (see SC170) for 110 ms out of each 140 ms duration.

The System Protection circuit also detects any seek attempts during a clamp operation and causes a File Unsafe to be generated under this invalid condition.

2.8.11.1 Linear Motion Protection Circuit Operation

When the signal + Retract Heads goes high, a reverse velocity to the linear motor is forced by the servo system and the heads begin retracting out of the pack. After the signal + Retract Heads is inverted by gate 1C-6, it triggers the single shot delay circuit 3A whose output is delayed from going high for 400 ms. Normally, during this 400 ms, complete head retraction takes place. After this time the linear motor protection circuit, although turned on, is not utilized because, upon retraction, the effect of the rectangular clamping waveform is overridden by 100% clamping. When the 400 ms times out, gate 1C-8 is enabled which in turn enables OR gate 1C-11. The high output of 1C-11 turns on the free-running rectangular waveform generator, which consists of 140 ms astable generator 2A-6 and 30 ms one shot 2A-9. The high output of 1C-11 also opens AND gate 2C-12 to the waveform. The rectangular waveform is clamped to become the signal-Servo Clamp which is applied directly to the signal Programmed Current (see SC170). The signal - Servo Clamp goes active 110 ms out of each 140 ms, clamping the Programmed Current and drastically limits power to the bobbin windings for approximately 80% of each 140-ms period. This limits average bobbin current to a safe value if the heads fail to retract. The current that is applied for 30 ms of each 140 ms period provides enough energy to bring the carriage and heads to a fully retracted position.

Loss of +5 V from the +5 volt logic supply will also cause the linear motor protection circuit to operate. The linear motor protection circuit can still operate with loss of machine logic supply voltage because it uses its own supply for all its voltages. Upon loss of the +5 V logic supply, the output from the +5 V Servo Supply, +5 V(s) causes the output of gate 1C-6 to go low, initiating a chain of events identical to that described for Retract Heads.

A + Seek Incomplete signal, after a 1 μs delay, also causes the linear motor protection circuit to operate.

2.8.11.2 System Unsafe Circuit Operation

The servo unsafe latch and the overtemp latch are initially set by - Pwr Up Reset or by manually pressing the CE Reset button S1. If the heads have not been commanded to retract, + Retract Heads is low (normal operating condition) and the output of gate 1C-6 is high, partially enabling AND gate 2C-8. If a clamp operation (caused by + Seek Incomplete) is in progress, the output of gate 2C-12 is pulsing low, partially enabling AND gate 2B-1.

At this time, any seek attempt will cause the output of 2B-13 to go low. This enables 2B-1, which enables 2C-8 setting the servo unsafe latch. OR gate 1C-3 is enabled and the signal - System Unsafe is generated. The signal - System Unsafe in turn causes a File Unsafe to be generated.

OR gate 1C-3 can also be enabled by the setting of the overtemp latch. This also causes a - System Unsafe.

2.8.12 Delay Timers (B03) (Use Delay Timers System Logic Diagram SC150.)

The delay timer circuits contained on the Delay Timer board B03 generate five signals of the required duration for use by the Servo Sequencer logic and the Power Up Sequencing and Control logic. These durations, in general, are times required for certain mechanical functions.

The delay timer circuits generating the signals +T1, +T2, and +T4 all have basically the same design except that each time delay network has a different RC value which determines the duration of the delay. Because of this similarity, only the Delay Timer circuit associated with +T1 will be explained in detail. All timers used by the Servo Sequencer logic are reset and started with the same signal + Reset Timers.

When the signal + Reset Timers is decoded in the Servo Sequencer Decode logic, it is applied to pin 7 of the Delay Timers logic card. This signal is inverted by gate 2D-8 and applied as a low to the reset input of the Seek Incomplete Delay latch, resetting it. The signal is also inverted by gate 7D-1 and applied as a high to the 100 ms Time Delay circuit

Q1-Q5. This high signal, which must be 10 μs or longer, resets the Time Delay circuit if it has not timed out. Since the 100 ms Time Delay circuit requires a low-going signal to initiate it, nothing happens until the + Reset Timers signal goes low. When it does, the output of gate 7D-1 goes low initiating the Time Delay. This delays the signal for 100 ms before it sets the Seek Incomplete Delay latch. This means the signal +T1 was delayed 100 ms after the signal + Reset Timers went low. The signals +T2, and +T4 are generated in similar fashion.

The signal +T6, labeled (15-Second Dynamic Braking), is used by the Power Up Sequencing and Control logic A08 to limit the application of dynamic braking current to the spindle drive motor to 15 seconds. This current is applied to the spindle drive motor when the START-STOP switch on the operator control panel is placed in the STOP position.

When the signal + Start T6 is low the Dynamic Braking latch is reset. The AND gate 3D-8 is disabled and its high output resets the Time Delay circuit. The high reset output of the latch is routed back to one input of the AND gate 3D-8, partially enabling it. When the signal + Start T6 goes high, it is applied to the other input of AND gate 3D-8 enabling it, causing its output to go low. This low signal is delayed 15 seconds by the 15-Second Time Delay circuit Q21-Q25. When the time delay circuit times out, the Dynamic Braking latch is set. Thus, the signal +T6 goes low 15 seconds after the application of the signal + Start T6. This 15-second delay is used in dynamic braking.

The circuit used to generate the signal +T5, labeled (60-Second Warm-Up), uses two 10-second time delays, a latch, and a two-bit ripple counter for its operation. Signal +T5 is used in the seek enable circuit in the Power Up Sequence and Control Logic A08.

When the signal + Start T5 is low, the latch 3D-11/4D-12 and the Warm-Up Time Counter (two-bit) 1D-12/1D-9 are reset. When the signal + Start T5 goes high it is applied to the input of the AND gate 4D-8. The other inputs of gate 4D-8 are high as a result of the previous resetting of the latch and the warm-up time counter. Gate 4D-8 has three high inputs so its output goes low. Ten seconds later, because of the 10-second Time Delay Q26-Q30, the latch sets. Once the latch is set, the low reset output of the latch disables gate 4D-8 and the high set output of the latch enables gate 4D-6. The output of gate 4D-6 goes low and 10 seconds later, because of the 10-Second Time Delay Q31-Q35, the latch resets. The latch and the two 10-second timers toggle once every 20 seconds. The set output of the latch is fed to the clock input of the first J-K flip-flop of the warm-up time counter. This counter counts the number of times the latch is reset. Gate 2D-3 decodes a count of three. Three consecutive 20-second delays produce one 60-second delay. The signal is inverted by gate 2D-6 and labeled +T5 (60-Second Warm-Up). The low out of 2D-3 is also fed back to the input of gates 4D-6 and 4D-8 stopping additional toggling of the latch.

2.8.13 Servo System (B04 and C01) (Use Servo Control System Logic Diagram SC160, Servo Driver System Logic Diagram SC170, and ±15 Volt Servo Supply Systems Logic Diagram SC180.)

Carriage positioning in the drive is accomplished by a feedback control system called a servo system. This servo system consists of a linear motor, a linear tachometer (tach), two analog control printed circuit boards (Servo Control B04 print SC160, and Servo Driver C01 print SC170), and four digital control printed circuit boards (Cylinder/Present Address Registers A06, Adder and Speed Decode A05, Servo Sequencer A03, and Servo Sequencer Decode A04).

2.8.13.1 Basic Operation

Before a seek is initiated, the control unit sends the new cylinder address to the drive where it is stored in the CAR. Adder logic in the Adder and Speed Decode logic computes the algebraic difference between the cylinder address and the present address (which is stored in the PAR). This difference is the number of tracks that the linear motor must move the carriage to arrive at the new cylinder requested by the control unit. If all interlock and other requirements are satisfied so that the drive is capable of performing a seek, the servo system is enabled, allowing the track difference (in the form of logic signals) to be converted by the Servo Control board to a voltage that corresponds to a programmed velocity. This voltage is sent to the Servo Driver board where it is converted to a current and applied to the linear motor. This current will cause the linear motor to move either forward or back, depending upon the sign (plus or minus) of the algebraic difference as soon as the detent pawl is picked (disengaged). A minus sign means the carriage must move backwards to get to the cylinder requested by the control unit, a plus sign means the carriage must move forward.

At this point the pawl is picked and 2.0 ms later the carriage starts to move, generating a voltage in the linear tachometer. The voltage varies according to the velocity of the carriage. The tach output is amplified by the tach buffer amplifier and fed back negatively to the velocity error amplifier. The carriage continues to accelerate and the tach output continues to increase until carriage velocity reaches the level prescribed for the specific track difference. At this point, the tach feedback voltage level is equal to the programmed velocity voltage level and carriage motion is held at a constant velocity. This is called the programmed velocity. While the carriage is traveling, the cylinder transducer counts rack teeth. The transducer amplifier output signals, which correspond to new track addresses, are sent to a counter in the PAR. The counter increases or decreases the present address by one as each new track is reached. The carriage maintains its programmed velocity until the

difference between the present address and the cylinder address equals the next lower power of two. Each power of two track difference is a boundary where the servo control input is stepped down to allow the carriage to decelerate. The power of two boundaries are 64, 32, 16, 8, 4, 2, and 1. For example, if the original track difference is 130, the first boundary is reached when the carriage is 64 tracks from its destination. If the original difference is 12, the first boundary is at eight.

As each boundary is crossed, a new logical input is sent from the Adder and Speed Decode logic to the Servo Control board, providing a new lower programmed velocity. Since this new velocity level is lower than the tach output, the excess of negative feedback from the tach causes motor current to reverse; the carriage slows down until the new programmed velocity is reached (tach voltage output equals programmed voltage input). The last boundary crossed during the seek is the one track boundary. The corresponding velocity is called the forward detent velocity. This level provides current in the forward direction regardless of whether the carriage is performing a forward or reverse seek. When this boundary is reached, the detent actuator is signalled to engage (set) the pawl against the next tooth in the rack. During a forward seek, the carriage travels forward until the pawl sets and stops it. During a reverse seek, the carriage reverses direction while the pawl is dropping; the pawl sets while the carriage is moving forward. As the carriage stops, the + Forward Velocity logic signal from the forward velocity detector goes low, initiating a delay which allows the small mechanical vibrations caused by detenting to be damped. After the delay times out, the drive signals the control unit that it is ready to read or write.

2.8.13.2 Servo Operation by Functional Blocks

The Servo Control board (B04 print SC160) and Servo Driver board (C01 print SC170) circuits can be studied as six interdependent functional blocks: (1) digital to analog network, (2) Tach Buffer Amplifier 5B, (3) Velocity Error Amplifier 4A, (4) current drivers, (5) Forward Velocity Detector 5D, and (6) safety circuits. There are also ± 15-volt regulators on the Servo Driver board (as shown on print SC180) which satisfy the ±15-volt requirements of B04 and C01. All other ±15-volt requirements in the drive are satisfied by the system ±15-volt supplies. This separation of supplies enables an emergency retract of the carriage from any cylinder, under full servo control (i.e., at a controlled constant velocity). This emergency retract occurs as a result of loss of power. Residual voltage on large electrolytic capacitors in the system power supplies provide retract current after loss of ac power.

A. Digital to Analog Network (B04 print SC160)

Each of the following logical inputs of B04 (seven forward velocities, seven reverse velocities, holding current, and forward detent velocity) control solid state switches which connect precision resistors to ±15-volts when the switches are activated. For each activated switch, a precise amount of current flows through the velocity scaling resistors to the summing junction of the Velocity Error Amplifier 4A.

B. Tach Buffer Amplifier 5B (B04 print SC160)

Since the output resistance of the tach is too high to permit it to drive the various required loads directly, it is buffered with an amplifier. The tach output is shunted with a resistor to adjust the tach scale factor to 0.1-volt/inch/sec. Therefore, a 5-volt output from the amplifier indicates a 50-ips velocity level. The resistance between the amplifier and the summing junction converts the analog voltage to an analog current which varies as a function of carriage velocity. A potentiometer (R84) is included to compensate for tach scale factor variations from one drive to another.

C. Velocity Error Amplifier 4A (B04 print SC160)

The operational amplifier circuit 4A amplifies the algebraic sum of the analog current from the digital-to-analog resistor network (which represents desired velocity) and the analog current from the tach amp (which represents actual velocity). Any difference between the two currents results in an output voltage from 4A. This serves as an input to the current driver which generates motor current with a polarity determined by whichever analog current is greater (programmed or tach amp). If the current generated by the tach buffer amplifier output is greater, the polarity of the current in the motor coil reverses and causes the carriage to decelerate. If the programmed current is greater, the current in the motor coil causes the carriage to accelerate. If the currents are equal, there is no output from 4A and the carriage coasts at the programmed velocity. The clamp circuits CR16 through CR19 limit the output of 4A to ± 9 volts. The offset adjustment potentiometer R77 corrects for the offset voltage errors of both the tach buffer amplifier and the velocity error amplifier. This adjustment is made at the factory, and field adjustment is not normally needed unless the velocity error amplifier is replaced.

D. Current Drivers (C01 print SC170)

The Servo Driver is a current driver of a bridge design whose scale factor and temperature sensitivities are controlled by operational amplifiers and 1% components. Half of the bridge is activated by positive going output from the Velocity Error Amplifier 4A on B04. As the output of 4A crosses 0 volts in the positive direction, the output of operational amplifier 1A (C01 print SC170) goes high, turning on the drive transistors it controls. This completes the path for current from the +55-volt line through the linear motor as well as through R5, the 0.25-ohm current sampling resistor, to ground. When the voltage across the resistor is equal to the scaled down input voltage, as seen at the input of 1A, the output of 1A changes to whatever voltage is necessary to hold the current constant. Since 2A is connected in an inverting mode, its output is low at that time, turning off its half of the bridge. Inversely, as the output of the Velocity Error Amplifier on B04 passes through 0 volts in the negative direction, operational amplifier 2A (C01 print SC170) turns on the drive transistors in its half of the bridge while 1A becomes inactive. There is a small dead zone near 0 volts which prevents both sides of the driver from turning on simultaneously. As additional protection against this condition, symmetrical shunting circuits are connected to the outputs of operational amplifiers 2A and 1A. When one half the bridge is activated (either operational amplifier 2A or 1A is on) the output of the opposite operational amplifier is shunted to ground by a transistor.

The Servo Driver has a scale factor of ±1.275 amp per volt. That means that +2 volts input causes 2.55 amps to flow in the motor coil.

The Servo Driver can be disabled by the logic signal, + Servo Disable on the Loss of the -15(s) volt supply. This clamps both operational amplifier outputs to approximately +0.8 volt, preventing motor current from flowing in either direction regardless of the amount of error amplifier output voltage.

The Servo Driver is also disabled by the combination of signals + Emergency Retract (high) and - Heads Retracted SW (low). If the carriage undergoes an emergency retract as a result of loss of +5 volts in the logic, the signal + Servo Disable cannot go high to disable the Servo Driver logic. However, as soon as the Heads Extended - Retracted switch senses that the heads are fully retracted, - Heads Retracted goes low and the Servo Disable logic is activated.

E. Forward Velocity Detector (B04 print SC160)

Operational amplifier 5D is connected as a Schmitt trigger with a +100-mv trigger level and 50 mv of hysteresis. During carriage acceleration in a forward seek, + Forward Velocity goes high as the velocity reaches 0.75 ips and the tach amp reaches 0.075 volt. The signal + Forward Velocity remains high during the rest of the acceleration portion of the seek and during deceleration until the carriage velocity drops below 0.5 ips (+50 mv from the tach amp). + Forward Velocity goes low after the pawl has engaged the rack and reduced the carriage velocity from 1.5 ips (forward detent velocity) to 0.5 ips. As + Forward Velocity goes low, the logic disables the - FWD Detent Velocity command to the digital-to-analog network and enables the - Holding Current input. This supplies 250 ma to the linear motor.

F. Safety Circuits

There are several safety circuits which protect the servo system. The first is a clamp circuit (see B04 print SC160) which restricts the maximum error amp output to +2.9 and -1.2 volts any time - Holding Current is active (i.e., when the carriage is stationary). The normal output at this time is +200 mv, so the clamp has no effect. If the carriage were manually forced back and forth, the tach would feed the error amp a signal which would cause at least 5 amps of motor current to flow. This would force the servo driver transistor to operate under abnormally high current and voltage conditions. The clamp restricts maximum motor current to less than 3.7 amps, which is a safe value.

A second safety circuit provides overtemperature protection to both the servo Driver transistors, and the motor bobbin (see B04 print SC180). Whenever bobbin temperature exceeds 100°C or the servo power transistors overheat, the signal + Over Temp goes high, disabling the servo and causing a file unsafe condition. Any condition that could cause the heads to crash (e.g., turning S1 off) will override the servo disable and withdraw the heads.

A circuit, consisting of Q33 and Q34, on B04 print SC160, provides controlled reverse velocity to retract the heads if 5 volts is lost. Both transistors turn on when 5 volts goes to 0 volts, causing CR12 to break down. The programmed current for retracting the heads is then provided by R62.

The signal - Servo Clamp, from the Servo Protection board B02, limits Programmed Current during conditions specified in the B02 logic card description. This is accomplished by turning on a bilateral clamp connected directly to the error amplifier output.

2.8.14 Index and Upspeed (B05) (Use Index and Upspeed System Logic Diagram SL150.)

As the disc pack rotates, the index transducer generates a dipulse each time an index slot passes it. The index transducer amplifier on B06 amplifies the dipulse and applies it to B05 as + Index at pin 19. The Index and Upspeed logic B05 converts this signal into a 35 μs pulse which is utilized by the control unit and by other circuits on the board. One of its purposes is to determine when the disc pack is up to speed. In addition to utilizing index pulses for determining whether or not the spindle drive motor is up to speed, the Index and Upspeed logic decodes the following signals: + Unit Ready, + Servo Disable, and + Pick. It inverts the signal + Read Gate for use in the Read Amplifier A10.

2.8.14.1 Index Detection

In this model disc drive, the $\overline{Q}$ output of flip-flop 4B output pin 6 is physically grounded with a jumper wire forcing it low and partially enabling AND gate 5C-4.

When the index transducer senses a slot in the index disc, a high logic signal from the index amplifier is applied to pin 19 of B05. This high signal initiates the 35 μs delay circuit which provides a high input to gate 4C-13. The delay circuit output will stay high as long as its input is high, but will go low 35 μs after its input goes low. When the Index pulse on pin 19 goes low, it is inverted by 4C-1 to provide a high input to gate 4C-13. At this time both inputs to gate 4C-13 are true and its output goes low creating a 35 μs Index pulse. The R-C network (R1-C11) provides immunity from short bursts of noise on input pin 19. The low output of gate 4C-13 enables AND gate 5C-4 whose output goes high generating the signal + Index which leaves the board on pin 6.

The signal + Index is also sent to the up-speed circuitry (middle of the print).

Sector mode operation is not used in the 660-0, therefore the sector circuits (upper right-hand section of print) will not be discussed.

2.8.14.2 Up-Speed Detection

The rate at which index pulses leave gate 5C-4 and 4D-3 determines whether or not the disc pack is up to the required speed. The up-speed detection circuit consists of gates 3C-8, 3C-11, and 5C-10; Index flip-flop, A flip-flop, and B flip-flop plus the two 37-ms Up Speed Delay Circuits A and B.

The spindle drive motor starts turning and accelerates when the disc pack drive is turned on.

To generate the signal + Up Speed, both flip-flops A and B must be set at the same time. This will cause the $\overline{Q}$ outputs of both flip-flops to be low thus enabling AND gate 5C-10 whose output generates the signal + Up-Speed.

During the time the spindle drive motor is accelerating, the slow rate of the - Index pulses is clocking the Index flip-flop alternately so that the state of the Q and $\overline{Q}$ outputs are reversing each time an index pulse occurs. At the same time, AND gates 3C-8 and 3C-11 are strobed by the signal + Index so that one or the other gates is enabled depending on the output state of the Index flip-flop. At the slower spindle drive motor speed, the 37-ms Up Speed Delay circuits alternately time out and alternately reset flip-flops A and B. Therefore, while the index pulse rate is low (low motor speed), the two flip-flops (A and B) are never in the same state.

As the motor speed increases, the alternation of the Index flip-flop becomes faster and at 70% of motor operating speed, the Up Speed Delay Circuits no longer have sufficient time to time out. Flip-flops A and B are now both set. Because the Up Speed Delay circuits never time out, both flip-flops A and B are being clocked and set continuously without ever being reset. The $\overline{Q}$ outputs of flip-flops A and B are both low, enabling AND gate 5C-10 thus generating the signal + Up-Speed. The signal + Up-Speed is routed to the Power Up Sequencing and Control logic to indicate that the disc pack is up to speed.

If the disc pack speed drops, such as during belt breakage, the reverse of the up-speed sequence described above will take place and the signal + Up-Speed will go low.

The complete loss of index pulses (such as during a circuit or transducer failure) will also cause the signal + Up Speed to go low. When this happens, the Index flip-flop is no longer toggled and the 37-ms Up Speed Delay circuits time out and reset, flip-flops A and B.

A number of unrelated functions are also provided by logic on the printed circuit board; these are:

A. The signal + Read Gate is inverted by gate 5C-1 becoming - Read Gate. It is used by the Read Amplifier.

B. The individual disc drive is ready (+ Unit Ready) if gate 2D-6 has all high inputs. During these conditions the large unit number indicator on the operator control panel will light. This indicator will not light if the signals - File Unsafe or + Seek Incomplete are active or if - Seek Enable is inactive.

C. The gate 1C-6 will generate a + Servo Disable signal if gate 1D-8 is low. This condition occurs if the signals + Unit Ready and either - Seek Enable or + Retract Heads are inactive.

D. The signal + Pick is generated by decoding an inverted -D, -A, and -C and then generating a fixed duration pulse with the circuit consisting of 4C-10, 3D-4, R3, and C14. This signal is used by the actuator driver.

2.8.15 Transducer Amplifier (B06) (Use Transducer Amplifier System Logic Diagram SC100.)

The control unit initiates a seek by sending a new address to the CAR. The output of the CAR is compared to the PAR address. The computed difference between the two addresses represents the number of cylinders the heads must travel to the new address. As the heads move, the position of the heads is monitored constantly by a cylinder count scheme, which sends a count pulse to the PAR each time the heads reach a new cylinder. Each pulse increases or decreases (depending on the direction of head travel) the PAR count by one, which decreases the difference between the PAR and CAR by one. When the difference is zero, the heads are at the addressed cylinder and a detent engages to inhibit head movement.

Information within a disc pack is recorded on 20 surfaces, with each surface having 203 concentric circles (track 000 to track 202). Since corresponding tracks on all 10 discs are vertically aligned, the corresponding 20 tracks are considered information cylinders; there are 203 cylinders, i.e., 20 track-000's, 20 track-111's, 20 track-202's, etc.

As the heads are positioned from one cylinder to another, the linear travel of the carriage is monitored by accurately counting the number of cylinders reached. This is accomplished by the cylinder count scheme (Figure 2-5), which consists of a rack of teeth, (called the detent rack), a double detent pawl, a double sensor cylinder transducer, a 145 kHz oscillator, and associated amplification and logic circuits.

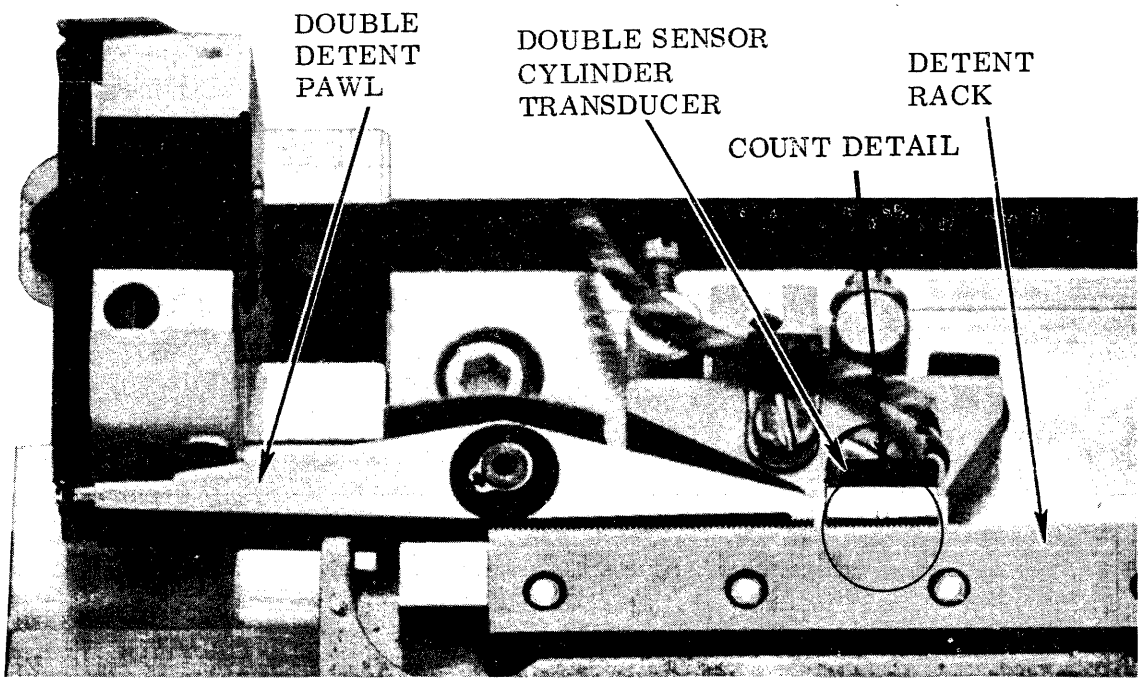


Figure 2-5. Detent Pawl, Detent Rack, and Cylinder Transducer Locations

As shown in Figure 2-5 the detent rack is mounted on the carriage and as the carriage moves the detent rack moves with it. Spacing of the rack teeth is 0.020". The double detent pawl and cylinder transducer are mounted opposite the detent rack, on the carriage way, and are stationary.

The number and spacing of the rack teeth, and the alignment of the rack teeth with respect to the transducer sensors and the sensor spacing, is such that each rack tooth represents a cylinder count as a rack tooth passes a sensor (see Figure 2-5, COUNT DETAIL).

The purpose of the detent pawl is two-fold: as a seek is completed, it engages the rack teeth and inhibits head movement until a new seek is initiated, and as it engages it ensures the final finite track positioning for the heads.

Each pawl has a set of teeth with the same pitch as the rack teeth. The two pawls are offset from each other by one-half their pitch (0.010"). This offset spacing allows the pawl assembly to engage the rack in twice as many positions as there are rack teeth, i.e., when one pawl is engaged the other rests on the adjacent rack tooth. One detent pawl engages at all odd-cylinder positions while the other engages at all even-cylinder positions.

The purpose of the cylinder transducer is to generate an output each time a new cylinder is reached (i.e., each time a rack tooth reaches a sensor). Thus, the teeth in the detent rack (which move as the carriage moves) are counted as they reach a sensor. As shown in Figure 2-6, the sensors are spaced apart so that when a rack tooth is opposite one sensor, a valley is opposite the other sensor. The two sensors are primary-secondary pairs. The primaries are in series and are driven by a 145 kHz Colpitts-type oscillator at a level of about 3 volts peak-to-peak. The secondaries are connected series opposing so that the outputs are 180° out of phase.

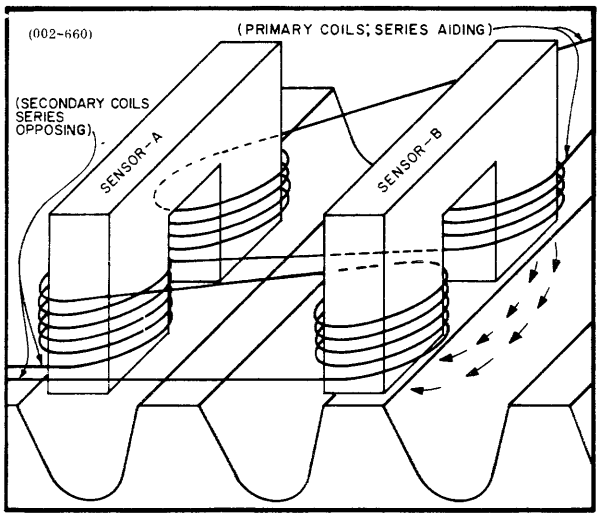


Figure 2-6. Cylinder Transducer Coupling

Each time a rack tooth reaches a sensor, it couples the primary-secondary pair so that a maximum transducer secondary output exists because of the sensor coupled (see Figure 2-6, sensor B). At this time sensor A is opposite a valley (between two teeth) and its output is minimum, as well as being 180° out of phase. As the carriage moves to an adjacent cylinder, the rack tooth to sensor relationship changes so that the output of sensor A is maximum. Sensor B is now opposite a valley and its output is minimum. At this time, the transducer secondary output is maximum because of sensor A coupling. During the period that the rack-to-sensor relationship was changing from coupling sensor B to coupling sensor A, a point was reached so that both sensors were equally coupled for an instant, and since the two sensor secondaries are connected series opposing, the two equal outputs partially cancel so that the resultant transducer secondary output is a minimum (null) (see Figure 2-7). Thus, there is always maximum output from the transducer secondary when a sensor is coupled and minimum output when both sensors are equally coupled and their outputs are equal.

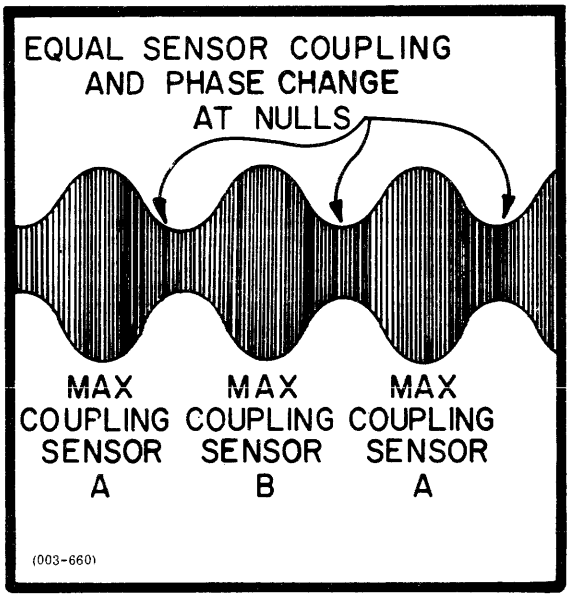


Figure 2-7. Added Transducer Secondary Outputs

The cylinder transducer amplifier uses the combination of the envelope amplitude and the phase change to generate the cylinder count pulses as the carriage moves from cylinder to cylinder.

The cylinder transducer amplifier logic also generates the two timing signals, + Clock and - Strobe B, which synchronize the Servo Sequencer logic. The index transducer amplifier is a part of B06, but is described in the Index/Upspeed description. Although the AC Fail Detection circuit and the Hi-Low Detection circuit are functionally a part of B06, they are discussed in greater detail in the Power Supply description.

2.8.15.1 Strobe Pulse Generation

In addition to exciting the cylinder transducer primary winding, the sine wave output of the 145 kHz Colpitts-type oscillator is applied to the clock comparator. This comparator has thresholds of 25 mv above and below zero volts and converts the oscillator signal to a nearly symmetrical square wave in a period of approximately 7 μs (see Figure 2-8).

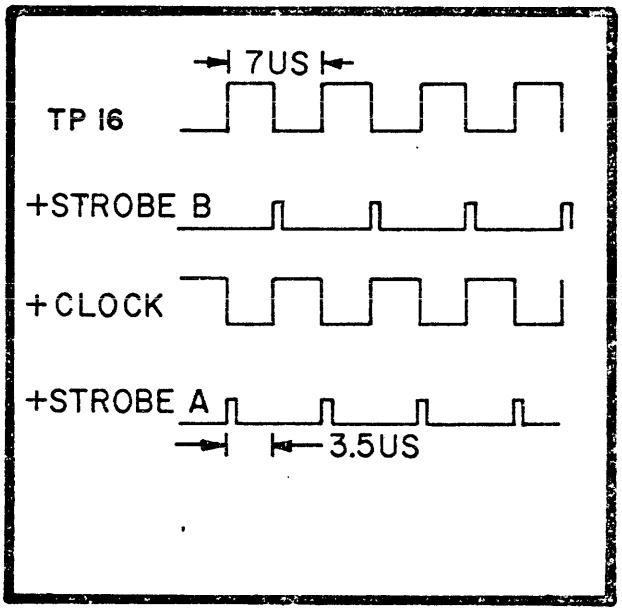


Figure 2-8. Strobe Pulse Relationships

The output of the clock comparator goes directly to a 150-ns one-shot which triggers on the negative going edge of the square wave, and generates a positive pulse, + Strobe B (see Figure 2-8). The square wave out of the clock comparator is also inverted by gate 2B-12 and leaves the board as + Clock. The + Clock signal also goes to another 150-ns one-shot which triggers on the negative going edge of the square wave, generating the signal + Strobe A. The pulse + Strobe A follows the pulse + Strobe B by 3.5 μs, and the pulses are used as clocking signals for various flip-flops on the board. These strobe and clock signals are generated continuously regardless of whether or not the carriage is moving.

2.8.15.2 Cylinder Count Generation

The output of the cylinder transducer secondary winding is connected to the arm level comparator and the count comparator. Because of transformer action and the effect of a shunt capacitor, the output signal from the secondary winding of the cylinder transducer is shifted 90° with respect to the output of the 145 kHz oscillator. This difference in phase allows the strobe pulses to perform their sampling while the output is near peak amplitude (see Figure 2-9).

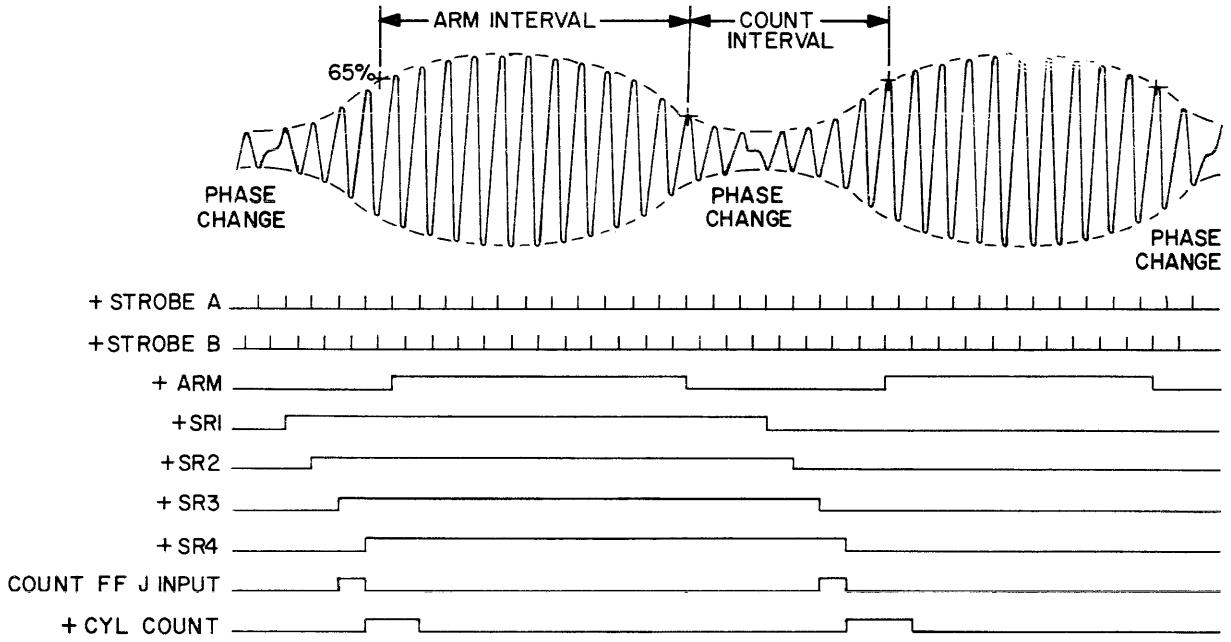


Figure 2-9. Transducer Amplifier Timing Relationships

Since the threshold of the count comparator is almost zero volts, its output follows the output of the secondary of the cylinder transducer. Assuming that the circuit has just armed during a phase B tooth, and the cylinder transducer is just starting to couple across a phase A tooth, the output of the count comparator during + Strobe A time is low. This low signal is inverted by gate 2B-10 and applied as a high level to the shift register.

The shift register serves as a filter to assure that a count signal will only be generated when there is actually a valid change in phase at the transducer output. Any short duration transients will be ignored by this circuit.

As the amplitude of the modulation envelope increases to 65% of its peak amplitude, the arm level comparator turns on and prepares the circuit to generate another Cyl Count signal when the phase changes again.

The Delta Phase Detect circuit detects a difference in the state of SR4 and SR3 as a phase change regardless of whether the cylinder transducer is moving from a phase A tooth to a phase B tooth or from a phase B tooth to a phase A tooth.

To assure that short term transients will not cause unwanted inputs to the Cylinder Count flip-flop, the Delta Phase Detect circuit is included as an exclusive OR circuit at the input of AND gate 3B-6. This circuit requires that at the time of a detection of change of phase, the first stage (SR1) of the shift register be in the same state as that of the third stage (SR3). Thus, any noise present at the count comparator input that is of two clock

periods duration or less (14 μs or less) and which has been shifted down the register as an apparent change of phase, will be ignored because the output of the $\overline{\text{Delta}}$ Phase Detect circuit will not be true at the required time. However, there will be several hundred clock times available for detecting the phase change even at the highest carriage speeds so that any phase change missed because of unwanted noise will still be detected before the cylinder transducer output changes phase again.

If the carriage should continue for a short distance after a compare and move into the area where the Cyl Count flip-flop becomes armed by the increasing envelope amplitude of the next tooth, the count circuitry would generate a cylinder count output when the carriage reversed and moved through a null on its way to the proper detent position. To prevent this invalid count, the signal - Compare is connected to the inputs of the Delta Phase Detect circuit to disable AND gate 3B-6 during a compare condition. Therefore, the Cyl Count signal will not be generated during this condition.

The Restore and Initialization logic, made up of the Dly Count flip-flop and the Enable flip-flop, is effective only at the beginning of the reverse seek portion of a restore or first seek operation. These two flip-flops are directly reset by the signal - Force Count when the count of 202 is forced into the PAR as the carriage is stationary at its forward stop. The output of the Dly Count flip-flop is connected to AND gate 3B-6, disabling it until the first Strobe A time after the Arm flip-flop is set.

To allow the 203 counts that are detected between the forward carriage stop and cylinder zero to be compatible with the count of 202 which is loaded into the PAR, the clock input to Cyl Count flip-flop is delayed one full cylinder count by the action of Enable flip-flop.

Once the first rack tooth is passed on the reverse portion of a restore or first seek operation, both the Dly Count flip-flop and the Enable flip-flop will be set and stay set until another restore or first seek operation is initiated.

Figure 2-10 shows the restore initialization timing relationships (counting from the carriage stop on a restore operation).

2.8.16 Control/Safety (B07) (Use Control/Safety System Logic Diagram SL200.)

The Control Safety logic B07 takes signals from the control unit and from within the drive and decodes them into signals which initiate operations, inhibit operations, and/or serve as status signals to the control unit. The Control Safety logic also decodes any unsafe conditions which might harm data on the disc pack. For instance, trying to read and erase at the same time is considered an unsafe (to the data) condition.

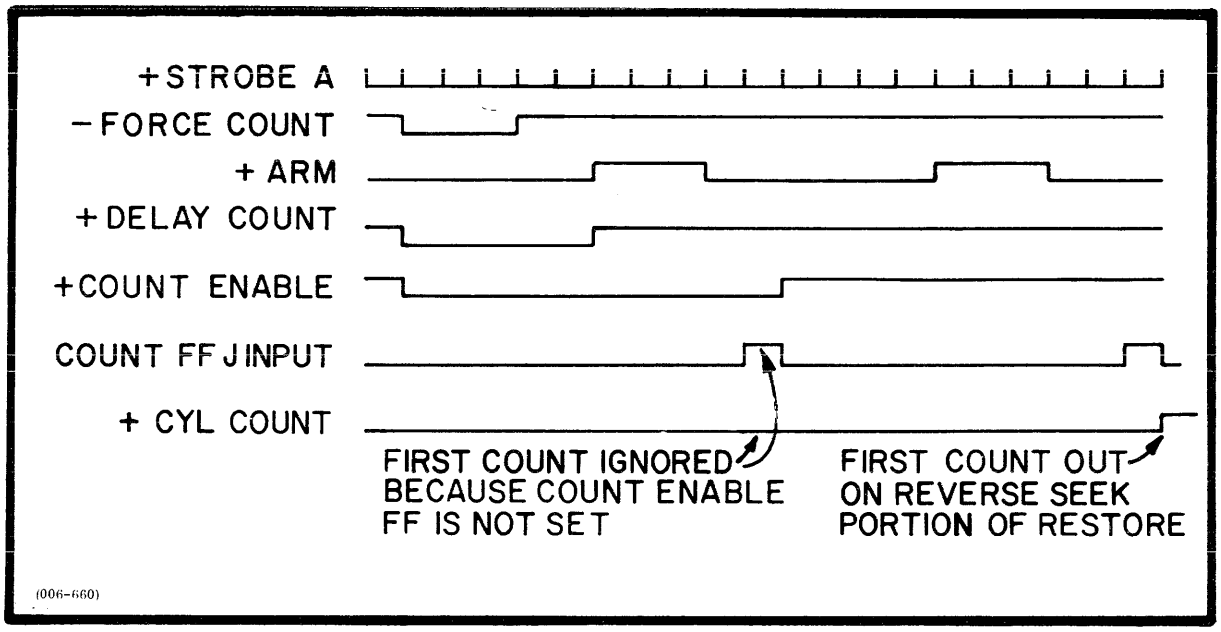


Figure 2-10. Restore Initialization

If an unsafe condition is decoded, the Control Safety logic generates a File Unsafe signal which disables the servo, lights the FILE UNSAFE lamp on the operator control panel, and goes to the control unit as a status line. Also, as a result of an unsafe condition, the Control Safety logic generates a Write/Erase Inhibit signal which clamps the write current drivers. This prevents the heads from writing during the unsafe condition.

The Control Safety logic on B07 is responsible for decoding the following control signals from the Unit Bus lines from the control unit, tag lines from the control unit, and various conditioning signals from elsewhere in the logic.

A. + Unit Is Selected and - Unit Is Selected

The signal + Unit Is Selected leaves the board on pin 4 and is sent to the control unit as a status line to tell the control unit that the drive has been selected. The signal - Unit Is Selected leaves the board on pin K and enables the line drivers associated with the CAR and status lines on B08 and B09, respectively. For the Unit Is Selected signals to be active, inverter D2-2 must be enabled. It is enabled if + Select Unit (from the control unit) is high. The - Power Up Reset signal clamps the + Select Unit signal low to prevent transients on the interface during power turn on and power turn off.

B. - Set Cylinder

This signal leaves the board on pin T. It enters the Cylinder/Present Address Register board A06 on pin 18 where its purpose is to clock the eight D-type flip-flops in the CAR. This signal is derived from the signals + Unit Is Selected (from D2-4), + Seek Ready (from the Servo Sequencer Decode logic), and + Set Cylinder (tag line from the control unit). When these signals are high, AND gate D3-12 is enabled and its output goes low, generating the signal - Set Cylinder.

C. + Set Head

This signal leaves B07 on pin S and enters the head selection and register board A07 on pin K. Its purpose is to enable the direct set inputs of the five head register flip-flops. One or more of the five flip-flops are set by selecting one or more of the five unit bus lines which also partially enable the five gates. The signal + Set Head is derived from a high + Unit Is Selected (from D2-4) and +Set Head (tag line from the control unit). When these signals are high, AND gate C3-11 is enabled and its output goes low. This signal is inverted by D4-4 to become + Set Head.

D. - Selected Unit Control

This signal leaves the board on pin 9 and enters the Servo Sequencer Decode board A04 on pin T. After it is inverted, it serves as the clock input to the Seek Start and Restore flip-flops. The signal - Selected Unit Control is the low output of AND gate C1-8 when it is enabled. The AND gate C1-8 is enabled when + Control (tag line from the control unit), + Select Unit (from the control unit), + Enable (output of the Enable latch), and - File Unsafe (no unsafe condition exists) are all high. When these signals are high, the output of AND gate C1-8 goes low generating the signal - Selected Unit Control.

E. - Reset Attention

This signal leaves the board on pin F and enters the Servo Sequencer Decode board A04 on pin X. Its purpose is to reset the Attention latch. This occurs when the signals + Unit Bus 1 (bus line from the control unit), + Select Unit (tag line from the control unit) and + Control (tag line from the control unit) are all high. If these conditions are met, AND gate D1-12 is enabled; its low output is the signal - Reset Attention. This signal is not dependent on either the Enable latch or File Unsafe.

F. + Write Gate

This signal leaves the board on pin 15. It enters the Head Selection and Register board A07 on pin 5 where it partially enables the write (Left) and write (Right) gates. It is the sum of + Selected Unit Control (output of inverter C2-12), + Unit Bus 0 (Select Write Gate), and - Read Only (READ/WRITE mode is selected on the READ/WRITE - READ ONLY switch). These conditions enable gate D3-8 whose low output is inverted by inverter D4-6 to become + Write Gate.

G. + Read Gate

This signal leaves the board on pin W. It enters the Head Selection and Register board A07 on pin 6 where it partially enables the read (Left) and read (Right) gates and gates the Read Data signal from Read Amplifier board A10. It is generated when AND gate C4-11 is enabled; i.e., when + Unit Bus 1 (Select Read Gate) and + Selected Unit Control (from inverter C2-12) are both high. When these conditions are met, the low output of gate C4-11 is inverted by inverter D4-12 to become + Read Gate.

H. + Erase Gate

This signal leaves the board on pin 8. It enters the Head Selection and Register board A07 on pin 4 where it partially enables the erase (Left) and erase (Right) gates. It is generated when AND gate D3-6 is enabled, i.e., when - Read Only (READ/WRITE mode is selected on the READ/WRITE - READ ONLY switch), + Unit Bus 4 (Select Erase Gate), and + Selected Unit Control (from inverter C2-12) are all high. When these conditions are met, the low output of gate D3-6 is inverted by inverter C2-4 to become + Erase Gate.

I. + Reset Head Reg

This signal leaves the board on pin 17. It enters the Head Selection and Register board A07 on pin L and is used for resetting the five head register flip-flops. It can be generated by either of two conditions. A low on the input pin V (- Force Count) will satisfy OR gate C4-6, producing + Reset Head Reg. The signal - Force Count is generated by the Servo Sequencer Decode when an address of 202 is forced into the PAR as part of a first seek or restore operation. This means the head register is cleared each time a restore operation occurs. The signal + Reset Head Reg can also be derived from the output of AND gate C4-3. This gate is enabled by + Selected Unit Control (from inverter C2-12) and + Unit Bus 3 (reset head register). The low output of C4-3 is inverted by C4-6 and becomes + Reset Head Reg.

J. + Select Head

This signal leaves the board on pin X. It enters the Head Selection and Register board A07 on pin F where it partially enables the outputs of the bit 2, 4, 8, and 16 flip-flops in the head register, causing the head decoding logic to select the head whose address is contained in the register. It is generated when AND gate D5-3 is enabled; i.e., when + Unit Bus 5 (Select Head) and + Selected Unit Control (from inverter C2-12) are both high. When these conditions are met, the low output of gate D5-3 is inverted by inverter D4-10 to become + Select Head.

K. + Head Advance

This signal leaves the board on pin Y. It enters the Head Selection and Register board A07 on pin 7 and is used to increment the head register. Its purpose is to increase the head register contents by one with each advance pulse. This signal is derived from the signals + Unit Bus 7 (Select Head Advance) and + Selected Unit Control (from C2-12). When these two signals are high, AND gate D5-6 is enabled and its output goes low. Inverter D4-8 inverts this low signal, generating the signal + Head Advance.

In addition to generating the above control signals, the Control Safety logic generates file unsafe signals from twelve separate file unsafe conditions. Each category of unsafe condition or combination of conditions has its own latch for storing occurrences of the condition. The outputs of these latches are ORed into a 12-wide OR gating structure which generates the signal + File Unsafe.

The conditions which are capable of setting each of the twelve unsafe condition latches are explained in the paragraphs below. Transistors Q1, Q2, and Q3 delay the enabling or disabling of Write Gate and Erase Gate signals as far as latches 1, 2, and 3 are concerned, to allow the sense signals to stabilize before sampling for an unsafe condition.

A. No AC Write (Test Point 1)

If the write gates in the Head Selection and Register logic have been selected but no voltage changes at the write current driver output are detected, a file unsafe condition exists. When this occurs, the signal (Write Gate) at the output of Q1 is high and - AC Write (Sense) entering B07 on pin N is also high. These two high signals satisfy AND gate B3-3 enabling it; its output goes low. This low signal sets the No AC Write latch and the signal No AC Write at TP1 goes low. This low signal enables OR gate B2-8 whose output goes high. The high output of B2-8 is inverted by C2-10 whose low going output enables the OR gate C3-6 thus generating the signal + File Unsafe. The signal + File Unsafe is inverted by inverters D2-6 and D2-12 to become - Write/Erase Inhibit and - File Unsafe respectively.

B. No Erase I (Test Point 2)

If the write gates in the Head Selection and Register logic have been selected but no erase current is being applied to the erase coils, a file unsafe condition exists.

When this occurs, the signal (Write Gate) at the output of Q1 is high, and the signal - Any Erase I (Sense) entering B07 on pin 11 is high. These high signals satisfy AND gate B3-6. Gate B3-6 is enabled and its output goes low, setting the No Erase I latch. The low signal, No Erase I at TP2 enables OR gate B2-8 which causes the output of OR gate C3-6 to go high thus generating the signal + File Unsafe.

C. Erase Select (Test Point 3)

If erase current is being applied to the erase coils but the erase gates in the Head Selection and Register logic have not been selected, a file unsafe condition exists. When this occurs, the output of gate D3-6 is high, causing Q3 to be off, its output being high. (Note that the output of gate D3-6, when inverted by C2-4 becomes + Erase Gate.) At the same time, the output of inverter D2-8 is high because the signal - Any Erase I (Sense) entering the board on pin 11 is low. Gate B3-11 is enabled and its low going output sets the Erase Select latch. The signal Erase Select at TP3 goes low and enables OR gate B2-8 which causes the output of OR gate C3-6 to go high thus generating the signal + File Unsafe.

D. Write Select (Test Point 4)

If write current is being applied to the write coils but the write gates in the Head Selection and Register logic have not been selected, a file unsafe condition exists. When this occurs, the output of gate D3-8 is high, causing Q2 to be off, its output being high. (Note that the output of gate D3-8, when inverted by D4-6, becomes + Write Gate.) At the same time, the output of inverter D2-10 is high because the signal - Any Write I (Sense) entering the board on pin L is low. Gate B3-11 is enabled and its low going output sets the Write Select latch. The signal Write Select at TP4 goes low and enables OR gate B2-8 which causes the output of OR gate C3-6 to go high thus generating the signal + File Unsafe.

E. Erase and Not Ready (Test Point 5)

If the erase gates in the Head Selection and Register logic have been selected but the drive is not ready to seek, a file unsafe condition exists. When this occurs, the signal + Erase Gate at the output of inverter C2-4 is high, partially enabling AND gate C3-3. If the drive is not ready to seek, the signal + Seek Ready which enters B07 on pin 16 is low. It is inverted by inverter D4-2 and applied as a high to the other input of AND gate C3-3 enabling it. The output of C3-3 goes low and sets the Erase and Not Ready latch. The signal Erase and Not ready at TP5 goes low and enables OR gate B2-8 which causes the output of OR gate C3-6 to go high thus generating the signal + File Unsafe.

F. Write and Not Ready (Test Point 6)

If the write gates in the Head Selection and Register logic have been selected but the drive is not ready to seek, a file unsafe condition exists. When this occurs, the signal + Write Gate at the output of inverter D4-6 is high, partially enabling AND gate C3-8. If the drive is not ready to seek, the signal + Seek Ready which enters B07 on pin 16 is low. It is inverted by inverter D4-2 and applied as a high to the other input of AND gate C3-8 enabling it. The output of C3-8 goes low and sets the Write and Not Ready latch. The signal Write and Not Ready at TP6 goes low and enables OR gate B2-8 which causes the output of OR gate C3-6 to go high thus generating the signal + File Unsafe.

G. Erase and Read (Test Point 7)

If the erase gates and the read gates in the Head Selection and Register logic have been selected simultaneously, a file unsafe condition exists. When this occurs, the signal + Read Gate at the output of inverter D4-12 is high, partially enabling AND gate D5-11. At the same time, the signal + Erase Gate at the output of inverter C2-4 is also high. AND gate D5-11 is enabled and its low going output sets the Erase and Read latch. The signal Erase and Read at TP7 goes low and enables OR gate B2-8 which causes the output of OR gate C3-6 to go high thus generating the signal + File Unsafe.

H. Write and Read (Test Point 8)

If the write gates and the read gates in the Head Selection and Register logic have been selected simultaneously, a file unsafe condition exists. When this occurs, the signal + Write Gate at the output of inverter D4-6 is high, partially enabling AND gate D5-8. At the same time, the signal + Read Gate at the output of inverter D4-12 is also high. AND gate D5-8 is enabled and its low going output sets the Write and Read latch. The signal Write and Read at TP8 goes low and enables OR gate B2-8 which causes the output of OR gate C3-6 to go high thus generating the signal + File Unsafe.

I. System Unsafe (Test Point 9)

If the servo driver or the linear motor bobbin overheats, a file unsafe condition exists. When this occurs, the signal - System Unsafe, which enters the board on pin 10, goes low and sets the System Unsafe latch. The output of the latch at TP9 goes low and enables OR gate B5-8 thus generating the signal + File Unsafe.

J. Head Select (Test Point 10)

If any of the conditions that constitute a head select error occur (see Head Selection and Register description), a file unsafe condition exists. When this occurs, the signal - Head Select Error, which enters the board on pin E, goes low and sets the Head Select latch. The output of the latch at TP10 goes low and enables OR gate B5-8 thus generating the signal + File Unsafe.

K. Multi Erase (Test Point 13)

If the drive attempts to supply erase current to both the right and left bank of heads simultaneously, a file unsafe condition exists. When this occurs, - Two Erase I (Sense) which enters B07 on pin 19 goes low, setting the Multi Erase latch. The signal Multi Erase at TP13 goes low and enables OR gate B5-8 which causes the output of OR gate C3-6 to go high thus generating the signal + File Unsafe.

L. Multi Write (Test Point 14)

If the drive attempts to supply write current to both the right and left bank of heads simultaneously, a file unsafe condition exists. When this occurs, - Two Write I (Sense) which enters B07 on pin C goes low, setting the Multi Write latch. The signal Multi Write at TP14 goes low and enables OR gate B5-8 which causes the output of OR gate C3-6 to go high thus generating the signal + File Unsafe.

The 12 unsafe condition latches are reset simultaneously by the signal which comes from gate C1-6. This signal can be generated by any of three conditions. When the signal + Seek Enable, entering the board on pin 22 is low, it enables OR gate D1-8 which causes the output of gate C1-6 to go low. This is the method for initializing the latches when power is turned off. The second condition for generating this signal is the grounding of the - CE Reset line. This can be accomplished by either grounding pin 18 or by pressing the CE Reset button S1 on B07 PC Board. Doing this will also enable OR gate D1-8 which causes the reset signal to go low. The third method of generating a reset signal is by enabling the AND gate D1-6 (Diagnostic Reset). To enable this AND gate, the signals + Unit Bus 1, + Select Unit and + Control must all be high. If these conditions are met, AND gate D1-12 is enabled and its low output is inverted by inverter C2-2 which partially enables AND gate D1-6. The signals + Index and + Unit Bus 3 must also be high to enable AND gate D1-6. When this gate is enabled, its low output enables OR gate D1-8 which causes the output of gate C1-6 to go low thus re-setting the 12 unsafe condition latches.

The FE can disable the File Unsafe logic while diagnosing a field problem. There are two ways to accomplish this. Connecting pin 18 to ground will hold all latches reset and cause the file to ignore any unsafe condition which may occur. The second method consists of jumpering pin B to ground. This is probably the more useful technique since it allows any unsafe condition which may occur to set the appropriate latch, but prevents the unsafe signal from reaching the rest of the drive logic. It is very important that this jumper be removed when service is completed so that the safety circuits can reactivate.

2.8.17 Line Drivers (B08, B09) and Line Receivers (B10) (Use Line Driver System Logic Diagrams LD100 and LD110, and Line Receiver Logic Diagram LR100.)

Since the control unit is located several feet from the drive, care must be taken to make certain that critical lines do not pick up noise spikes, which will degrade the signal on these lines. In order for cable capacitance and line losses to be of little consequence, line drivers are used to transmit the signals along these lines. And, line receivers are used on the receiving end of the cables. They act as signal translators and amplify the signals.

2.8.17.1 Line Drivers (B08 and B09)

Since all line drivers on B08 and B09 are basically the same, only one circuit will be explained -- the line driver which transmits the signal + On Line. (See the Line Drivers System Logic Diagram LD110.)

When the drive under discussion has been selected, the signal - Unit Is Selected entering pin 14 goes low. It is inverted by gate 3B-10 whose high output partially enables AND gate 4B-13. When the signal + On Line becomes active it goes high and satisfies AND gate 4B-13 whose output in turn goes low. This low output causes the voltage at the input of the Line Driver circuit to go low and turns it on. The Line Driver circuit has sufficient power to drive the long interface line without significantly degrading the signal. If - Power Up Reset goes active (low), the top eight line driver gates are disabled to prevent intermittent status line conditions during ac power up or down while other drives are being used.

An output level of + 1.15 volts or greater is a logical ZERO; - 1.52 volts or less is a logical ONE.

2.8.17.2 Line Receivers (B10)

Since all line receivers on B10 are basically the same, only one circuit will be explained --the line receiver which receives the signal - Unit Bus 4 from the control unit. (See the Line Receiver System Logic Diagram LR100.)

An input level of -0.2 volts or less is received as a logical ONE, +0.4 or greater, a logical ZERO. When the signal - Unit Bus 4 (entering at pin 16) becomes active it goes low, turning the Line Rcvr circuit on, thus generating the signal + Unit Bus 4 which leaves the board at pin T.

2.8.18 Actuator Driver (CO4) (Use Actuator Drivers System Logic Diagram SC200.)

The detent actuator consists of a permanent horseshoe magnet with a ferromagnetic reed in the gap between poles. The base of the reed is stationary, but the reed is flexible enough for its top to bend from one permanent magnet pole to the other. Two coils are wrapped in opposite directions around the reed. When current is sent through one coil, the reed is polarized in one direction and the top of the reed is attracted to one permanent magnet pole. Current applied to the other coil reverses polarity in the reed so that it transfers to the other permanent magnet pole.

When the reed moves toward one pole (because of current in the coil), it pushes a plunger rod. In turn, this rod pushes against one end of the detent pawls, causing them to pick (disengage from the detent rack). When the reed transfers to the other pole (because of current in the other coil), it releases the plunger rod. With no pressure against the plunger rod, the spring-loaded detent pawls set (engage with the detent rack).

The Actuator Driver logic is responsible for providing the required amount of current to one of the two actuator reed coils in order to either pick or set the detent pawls.

2.8.18.1 Normal Seek

In the following discussion, it is assumed that the drive is about to perform a normal seek; the detent pawl is set, the signal + Detent is high and there is no current flowing in either actuator coil. As a result of the last set operation, the reed is against the set pole of the permanent magnet, applying no force to the plunger rod.

2.8.18.2 Pick

When + Detent goes low in preparation for a seek operation, it applies a low to the Driver Amplifier Q8/Q9 turning Q8 off. With Q8 off, Q9 turns on. The base of Q17* goes high and that transistor turns on. This supplies current to the pick coil. This current reverses the polarity of the actuator reed so that it transfers over to the pick pole of the permanent magnet. As the reed transfers, it pushes the plunger rod against the detent pawls, causing them to disengage from the rack. As the current increases through Q17 and the pick coil, a positive voltage develops across R18. This slight positive bias is coupled to the Driver Amplifier Q8/Q9, restricting the current flow through it. This in turn limits the current through Q17 and the pick coil to a desired value.

The low + Detent signal also turns off the Driver Amplifier Q10/Q11. The base of Q18 goes high, turning that transistor on. This provides holding current to the pick coil as long as + Detent remains low. Holding current keeps the actuator reed in the pick position to assure that the detents stay picked throughout the seek operation.

Since holding current is sufficient to keep the actuator reed in the pick position once it has completed the transfer, pick current is maintained only long enough to assure that the detent pawls are picked. The 2.0 msec one shot Q3, 5, 6, and 7 hold it for 2.0 ms. Then that current is dropped. During the 2.0 ms there is both pick current and holding current in the pick coil. For the remainder of the seek, there is only holding current in the pick coil.

2.8.18.3 Set

Until the carriage reaches the target cylinder and the Adder and Speed Decode logic recognizes a compare condition, + Detent remains low.

*Q17, the pick transistor, Q18, the holding current driver and Q19, the set transistor are located on the heat sink No. 4 and not on the Actuator Driver board.

When the target cylinder is reached and the signal + Detent goes high, the 2.0 msec One Shot Q12, 13, and 14 begins timing out. At the same time, CR4 becomes back biased and turns off. This causes the Driver Amplifier Q15/Q16 to turn on which causes the base of the set coil drive transistor Q19 to go high, turning it on. Current begins flowing in the set coil and the reed swings to the set pole piece. This releases the plunger rod, allowing the spring-loaded detent pawl to engage. As the current increases through Q19 and the set coil, a positive voltage is developed across R36, which limits the current through the set coil drive transistor Q19 and the set coil to a desired value.

During the 2.0 ms charge time, current flowing through Q19 flows in the set coil. When the 2.0 msec One Shot times out, the set coil current ceases. The attraction of the set pole piece to the permanent magnet holds the reed in the set position until current is generated in the pick coil.

2.8.18.4 Special Conditions

Provision has been made to supply additional current in the pick coil to pick the detent pawls before a first seek.

This is done because, before a first seek, the carriage is retracted. This means the detent pawl teeth are not resting against the detent rack and the pawls are pivoted further in the set direction than they are when the carriage is not retracted. Consequently, the backs of the pawls are pushing the plunger rod back against the actuator reed. At other times, when the carriage is not retracted, there is no force against the actuator reed other than the attraction of the set pole to the permanent magnet. The reed is able to develop momentum before it has to overcome the spring load on the detent pawls. However, before a first seek, this load resists the actuator reed from the start, requiring more current in the pick coil to complete the reed transfer in the time required.

This extra current is generated whenever the signal + CAR/PAR Reset is high (pin 12). This high turns inverter Q17 on, shunting some of the base current from the Driver Amplifier Q8/Q9 during the 2.0 ms pick drive pulse. This decreases the current limiting influence of Q8 on Q9, allowing more current to flow through the pick transistor Q17 and the pick coil.

When a restore operation is initiated, the signal + Pick at pin 17 goes high to assure that a new 2.0 ms pick drive pulse is generated.

This high on pin 17 turns on Q4, which causes the 2.0 msec One Shot Q3, 5, 6, and 7 to begin timing out. This, in turn, allows the Driver Amplifier Q8/Q9 and Q17 to conduct. As a result, current is supplied to the pick coil and the detent pawls disengage. Two ms later current is removed from the pick coil.

2.9 POWER SUPPLY DESCRIPTIONS (Use the drawings indicated in the individual descriptions below.)

The disc pack drive receives its primary ac power from the control unit, or if in a string of drives, it receives its ac power from the previous drive in the string (see AC Power Distribution System Logic Diagram ZD100).

The three-phase primary ac voltage enters the drive at J1 (the AC IN connector) on the interior control panel. In addition to supplying primary ac power for the machine, these three voltage lines are directly connected to J2 (AC OUT connector) where they supply primary power to the next drive in a string of drives.

Within the drive, two of the three primary power lines are connected to S1, the DPST power ON-OFF switch, which is also located on the interior control panel. Phases are rotated between drives to minimize the load on each of the available phases.

In addition to the primary power lines, 115 Vac enters J1 to provide power at a duplex outlet (not provided in 50 Hz drive). This power is also routed to J2 to supply convenience outlet voltage to the next drive in the string. Chassis ground also enters the drive at J1 and leaves it at J2 for the next drive in the string of drives.

The drive provides its own dc power. This is regulated in two stages. The first regulation occurs at the main power transformer, T1 (see Raw DC Distribution print ZD200). This is ferroresonant and is capable of 3% to 5% line load regulation. The +5, ±15, and ±36 dc voltages are further regulated by solid state series regulators as needed by both the logic and analog circuits.

The relays and lamps are powered by +24 Raw DC (unregulated) which is rectified directly from T1. It does have the benefit of the transformer regulation, however.

Another voltage that is not regulated is +55 raw DC. It is used by the linear motor servo, drive motor braking circuit, and detent actuator. This voltage is taken from across a large capacitor (22,000 mfd) to provide the large short term surges of current required to accelerate the linear motor and to provide adequate energy storage to retract the heads from the pack in case of an ac power failure.

2.9.1 Basic Operation

When S1 (see print ZD100), the power switch on the Primary AC Power schematic, is turned ON, the primary power is routed through fuses F1 and F2 and line filters FL1 and FL2 to pins 1 and 3 of J9. It is then applied to the input of the power transformer T1 (see print ZD200). The secondary outputs (approximate clipped sinewaves because of the

ferroresonant action) are rectified to supply voltages for the generation of various regulated dc voltages used throughout the drive. This ac input voltage to T1 is also applied to the power supply fans B4 and B5 and the logic fan B3. These fans begin rotating as soon as the power switch is turned on.

The output of the secondary windings (pin 6 and pin 8) is bridge rectified by CR4 to become +24 raw DC at the right side of fuse F7. This rectified voltage is filtered by capacitors C6 and C7 (after passing through isolating diode CR5) and supplies voltage to the ±15 volt regulator on C02 (see print ZD220). This +24 raw DC is also applied to one side of both relay coils of K1 and K2 (see print ZD100). The other sides of K1 and K2 are connected to pin 12 of J10 which is routed to the Relay Driver (-K1/K2 Pick) on the Power Up Sequencing and Control board. If -K1/K2 Pick is active (see Power Up Sequencing and Control logic description), K1 and K2 coils are energized. At this time the contacts of K2 apply the primary power to the disc motor (spindle drive motor) and the disc pack spindle begins rotating. At the same time, two sets of contacts on K1 apply the primary power to the blower motor and it begins cooling the interior of the drive. Another set of K1 contacts connect to 24 Vac which comes from pin 6 of T1. The other side of these contacts go to the elapsed time meter which begins counting elapsed time.

During this time the various regulators supply regulated dc voltages used throughout the drive.

When the START/STOP switch on the operator control panel is placed in the STOP position, a dc dynamic braking voltage is applied to the disc motor (spindle drive motor) as follows: when the STOP position is selected, the signal GND = Pick K1 and K2 goes inactive and the arms of K2 switch to the upper contacts as shown on print ZD100. The heads retract, the elapsed time meter stops, and the dc signal Dynamic Brake is applied to pin B on the actuator driver (SC200). Transistors Q1 and Q2 on this schematic turn on, causing the signal GND = Dynamic Brake (see print ZD100) which supplies ground path for the +55 volt supply bringing the disc motor to a stop within 15 seconds.

2.9.2 ±15 Volt Supply (Main)

The ±15 volt power supply is located on board C02. For the following description use the ±15V and 5V Power Supply schematic diagram XC020.

A closed loop regulator design is used in both the +15 and the -15 volt supplies. The +15 volt regulator is shown above the ground line on the schematic; the -15 volt regulator is shown below the ground line. Because the -15 volt regulator is basically a mirror image of the +15 volt regulator, only the +15 volt regulator will be described.

The reference voltage for the +15 volt regulator is developed across the zener diode CR1 whose operating voltage is derived through R6 which is connected to the +15 volt regulated output line. The slightly positive temperature coefficient of CR1 is cancelled by the negative temperature coefficient of the base to emitter voltage of the error amplifier Q3. The current through Q3 determines the voltage drop across R2 and R1 which allows just enough current to reach the base of the pass element (Q15 of the Q1/Q15 Darlington pair) to support the total load current requirement while delivering the desired voltage output. This total load current flows through the emitter of Q15 and the resistor R4.

Completing the loop, a sample of the output voltage is taken at potentiometer R8 and applied to the base of Q3. This sample of voltage (approximately 7.5 volts) determines the exact voltage delivered by the supply.

If the load current increases significantly (such as during a short circuit on the +15 volt line), the voltage drop across R4 increases, causing Q2 to conduct more heavily. The increased collector current of Q2 causes R2 and R1 to drop a larger voltage which reduces the conduction of Q1 and Q15 thus limiting the load current to a safe value without damaging the pass transistor Q15.

2.9.3 +5 Volt Supply

The +5 volt supply is located on board C02. For the following description use the ±15V and 5V Power Supply schematic diagram XC020. The +5 volt supply is on the lower portion of the schematic.

The regulator used in the +5 volt supply is of the closed loop variety. The zener diode CR3 which derives its operating voltage from the +15 volt supply via R21 feeds a voltage divider R22, R23 which holds the base of Q9 at a constant voltage level. The voltage at the collector of Q10 (base of Q8) allows the proper current to reach the base of the pass elements Q11 and Q12 in order to conduct the load current while delivering the desired voltage at the output. The load current flows through the resistive network consisting of R26, R27, and R28 which is in series with the pass elements.

A sample of the output voltage is taken at R31 (approximately 2.5 volts) and applied to the base of Q10. This sample of voltage determines the exact voltage delivered by the supply and can be adjusted with R31.

As the load increases (such as during a short circuit on the +5 volt line) the voltage drop across the resistive network R26, R27 and R28 increases, causing Q7 to conduct more heavily. With Q7 conducting heavily, a lower voltage is placed on the base of Q8 reducing its conduction which in turn reduces the conduction of Q11 and Q12 thus limiting the load current to a safe value without damaging the pass elements Q11 and Q12.

2.9.4 ±36 Volt Supply

The ±36 volt power supply is located on board C03. For the following description use the 36V Power Supply, AC Power Fail schematic diagram XC030.

A closed loop regulator design is used in both the +36 and the -36 volt supplies. The +36 volt regulator is shown above the ground line on the schematic; the -36 volt regulator is shown below the ground line. Because the -36 volt regulator is basically a mirror image of the +36 volt regulator, only the +36 volt regulator will be described.

The reference voltage for the +36 volt regulator is developed across the zener diode CR1 whose operating voltage is derived through R6 which is connected to the +36 volt output line. The slightly positive temperature coefficient of CR1 is cancelled by the negative temperature coefficient of the base to emitter voltage of the error amplifier Q3. The current through Q3 determines the voltage drop across R2 and R1 which allows just enough current to reach the base of the pass element (Q20 of the Q1/Q20 Darlington pair) to support the total load current requirement while delivering the desired voltage output. This total load current flows through the emitter of Q20 and the resistor R4.

Completing the loop, a sample of the output voltage is taken at R8 and applied to the base of Q3. This sample of voltage (approximately 7.5 volts) determines the exact voltage delivered by the supply.

If the load current increases significantly (such as during an excess load on the +36 volt line), the voltage drop across R4 increases, causing Q2 to conduct more heavily. The increased collector current of Q2 causes R2 and R1 to drop a larger voltage which reduces the conduction of Q1 and Q20 thus limiting the load current to a safe value without damaging the pass transistor Q20.

2.9.5 AC Fail Detection

The AC Fail Detection circuit is located on board C03. For the following description, use the 36V Power Supply, AC Power Fail schematic diagram XC030. The AC Fail Detection circuit is shown in the lower portion of the schematic.

The AC Fail Detection circuit uses a differential amplifier to compare a known dc voltage with rectified ac voltage from the main power transformer T1. If the ac voltage fails, an emergency retract signal is generated which retracts the heads before the disc can be damaged by crashing heads while the spindle drive motor coasts to a stop.

The reference voltage for the reference side of the differential amplifier Q7/Q8 is developed across the zener diode CR7 whose operating voltage is derived through R23 which

is connected to the +55 Vdc supply at pin 7. Although the 55 volts dc is derived from the transformer T1, it holds steady for several seconds even after ac voltage is removed because it is taken off a large filter capacitor (C3 on DC Power Distribution schematic diagram). The resistive divider network R24/R25 holds the base of Q7 at a constant 3.4 volts.

The ac voltage for the ac detection side of the differential amplifier Q7/Q8 comes from pins 5 and 9 of the primary power transformer T1 (DC Power Distribution schematic diagram). These pins are routed to C03 pins 6 and 8 where the ac voltage is full wave rectified by diodes CR3 and CR8. Capacitor C12 is chosen to provide a time constant of several cycles of ac. The zener diode CR5 and resistor R22 cause the voltage at the top of R28 to be high enough to turn Q8 on which turns Q7 off when ac is present on T1. The high voltage at the collector of Q7 causes Q9 to turn off which keeps the output line at pin P (+Emergency Retract) low while ac is present at the power transformer T1.

If primary ac voltage is removed (power failure or if the power switch S1 on the interior control panel is turned off), the voltage is removed from the base of Q8, turning it off. The +55 volts at pin 7 remains for several seconds after the ac power is removed, Q7 turns on. The low voltage at the collector of Q7 turns on Q9 which passes dc current to generate the signal +Emergency Retract which leaves the board on pin P. The signal +Emergency Retract causes the heads to retract. Figure 2-11 shows the decaying voltage on capacitor C12 after ac power is removed from the drive. The 5V undervoltage detector has been disabled in this figure since it will also operate after ac power is removed and generate an Emergency Retract signal.

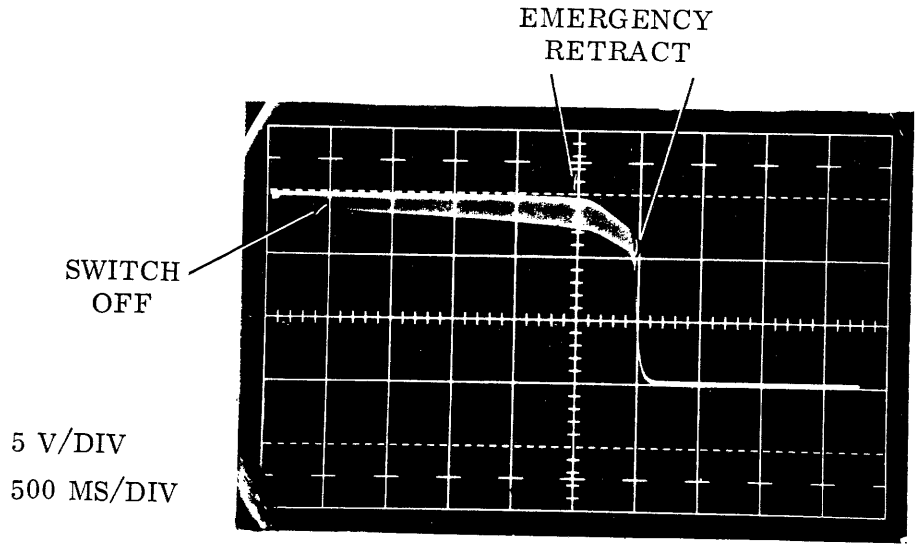


Figure 2-11. C12 Decay Voltage

2.9.6 ±15 Volt Supply (Servo)

The ±15 volt servo power supply is located on the Servo Driver board C01. For the following description use the Servo Driver schematic diagram XC010. The ±15 volt servo power supply is shown on the lower portion of the schematic. Because the -15 volt regulator is basically a mirror image of the +15 volt regulator, only the +15 volt regulator will be described.

The reference voltage for this regulator is developed across the zener diode CR15 whose operating voltage is derived through R32 which is connected to the +15 volt servo voltage output line. The cathode of CR15 is connected to the emitter of Q10 whose collector current determines the voltage drop across R29 and R31. This voltage drop allows just enough bias on the pass transistor's (Q5) base to support the total load current requirement while delivering the desired voltage output. This total load current flows through the emitter of Q5 and the resistors R30 and R47.

The output voltage is sampled by the base of Q10 via the potentiometer R35. This sample of voltage (approximately 7.5 volts) determines the exact voltage delivered by the supply.

If the load current increases, tending to decrease the output voltage, the voltage drop across R29 and 39 decreases, thus placing the base of Q5 at a more positive voltage with respect to its emitter, causing Q5 to conduct more heavily. This extra load current, during this condition, re-establishes the output to +15 volts.

2.9.7 Hi-Lo Voltage Detection

The purpose of the hi-lo voltage detection circuit is to disable the +5 volt supply if that supply goes above or below predetermined voltage levels. It does this by shorting out the +5 volt supply with a silicon controlled rectifier (SCR). The loss of the +5 volts causes the heads to retract in addition to protecting all logic in the machine by removing the logic operating voltage.

The hi-lo voltage detection circuit is located on board B06. For the following description, use the transducer amplifier schematic diagram XB060. The hi-lo voltage detection circuit is shown on the lower right hand portion of the schematic.

The +5 volt supply is connected, through R43, to the inverting input of comparator A4 and the inverting input of comparator A3. The non-inverting input of A4 is connected to the reference voltage developed from the 5.6 volt zener diode CR5. Therefore, during normal conditions input (pin 3) of A4 is positive with respect to input (pin 2). Hence, the output of A4 is a positive voltage. This positive voltage is routed through R48 and turns on Q10. Q7 and Q8 are turned off and the output at pin 1 is low. Pin 1 is connected to the gate of a SCR which

is connected between the +5 volt power supply line and ground. Thus, under normal conditions, the +5 volt power supply remains unaffected.

If the +5 volt power supply increases in voltage to greater than +5.4 volts, the inverting input of A4 becomes positive with respect to its non-inverting input and A4's output goes negative. This negative output turns off Q10. Q7 and Q8 turn on generating the signal + Fire Crowbar SCR at pin 1. The SCR fires and shorts out the +5 volt supply. The A4 output also forces the signal + Emergency Retract high (pin 21) to cause the heads to retract.

Also during normal conditions, the non-inverting input (pin 3) of A3 is negative with respect to the inverting input (pin 2) because of voltage division across R64, R46, and R47. Hence, the output of A3 is a negative voltage during normal conditions. This output is also held low during conditions of power up (when the 5V has not yet reached its regulated value) by the signal - Pwr Up Reset entering the board on pin 20.

If the +5 volt supply decreases to a voltage of less than 4.8 volts, the inverting input of A3 becomes negative with respect to its non-inverting input and A3's output goes positive, generating the signals + Emergency Retract and + Fire Crowbar.

2.10 POWER-DOWN

2.10.1 By Operator

When the START-STOP switch is placed in the STOP position, the heads begin to retract and the Servo Sequencer logic resets to state 0000. This assures that the servo system will be prepared to perform a first seek following the next power up. When the heads are fully retracted, the Heads Extended-Heads Retracted switch transfers to the Heads Retracted position. A safety interlock prevents turn-off of the drive motor unless the heads return to the fully retracted position. The disc pack motor leads are switched from primary ac voltage to the dynamic braking circuit. Dynamic braking current (dc) is applied to the motor for 15 seconds, bringing the motor, spindle and disc pack to a smooth halt.

2.10.2 By Control Unit

When the control unit powers down a drive it removes the controlled ground line, resetting the sequence latch. The output of the sequence latch causes the heads to retract and ac voltage to be removed from the disc pack motor. Dynamic braking is not applied in this case so the disc pack motor slowly coasts to a stop.

SECTION 3

INSTALLATION

3.1 GENERAL

The following information is provided as a guide for installing a Model 660-0 disc drive. It outlines basic procedures which should bring the drive on line in a short time. These procedures are not intended as a substitute for whatever standard practice the customer may have for equipment installation.

3.2 UNCRATING AND INSPECTION

A. Examine the corrugated sleeve covering the drive and visible portions of the drive. If signs of damage are found, note them on the freight bill before releasing the carrier.

B. Cut the nylon strap that holds the corrugated sleeve in place.

C. Lift the corrugated sleeve off the drive.

NOTE

The corrugated sleeve is slotted and creased so that it can be used as a mailing carton.

D. Remove the open cable container from the top of the drive.

E. Lift the polyethylene bag off the drive.

F. Remove the tape from around the drive.

G. Remove the back panel, lift out the gate block and swing open the logic gate.

H. Remove the tape and cardboard that hold the PC boards in place.

I. Remove both top covers.

J. Remove the tape that holds the Tee-block to the positioning motor.

NOTE

If practical, all packaging materials should be saved for repacking the drive for shipment or storage.

3.3 REPACKING FOR SHIPMENT OR STORAGE

To Be Supplied.

To Be Supplied

Figure 3-1. 660-0 Packaging

3.4 ENVIRONMENT

The disc drive should be placed so that there is 3' of clearance at both the front and rear of the machine. This allows room to remove the front and rear panels for maintenance. Room Temperature range should be 60^{O}F to 90^{O}F with temperature changes less than 15^{O}F per hour.

3.5 INSTALLATION

An appropriate Memorex Off-Line Tester and a CE alignment disc pack (yellow shield, P/N 150405) are needed to properly perform the necessary operational checks on the drive. To prepare the drive for operation, proceed as follows:

A. Check to be certain that all printed circuit boards are secure in their connectors.

B. Check to be certain that the head plugs are connected to the connectors on the Read/Write Amplifier boards.

CAUTION

Make sure the Read/Write Amplifier Left and Read/Write Amplifier Right boards (adjacent to the cam tower) are installed and secure in their connections. If not, the Read Amplifier board A10 will be damaged when the interior control panel power switch S1 is turned on.

C. Check the head shoes for dirt (some dirt might have accumulated during shipment). If necessary, clean the heads, following the procedure given in paragraph 4-13.

D. Check to be certain the power switch, S1 on the interior control panel, is in the OFF (down) position. Connect the primary ac power cable (all cables are shipped in a separate carton) between the AC IN connector, J1, on the interior control panel and the control unit.

NOTE

Because the disc drive has ground currents in excess of 5.0 milliamperes, the control unit to which these drives are connected must have electrical grounding that contains the following:

1. An insulated grounding conductor that is identical to the grounded and ungrounded branch-circuit supply conductors except that it is finished to show a green color (or green with a yellow stripe) is to be installed as part of the branch circuit that supplies the unit or system.

2. The grounding conductor mentioned in item 1 is to be grounded at the service equipment.

3. The attachment-plug receptacles in the vicinity of the unit or system are all to be of a grounding type, and the grounding conductors serving these receptacles are to be connected to the grounding conductor that serves the unit or system.

If the drive is part of a string of drives, all drives except the one connected to control unit ac power receive their power via the AC OUT connector (J2) on the previous drive. All cables which are connected to the drive must enter the machine through the cable hole in the bottom of the machine.

NOTE

The maximum three-phase current which can be fed through the ac connections on any drive to power it and succeeding drives in the string is 26.0 amps per phase.

E. Check to be certain that the switches on the operator control panel are all down.

F. Install the FE pack on the drive. Move the carriage out by hand a short distance to check that the heads will not hit the edges of the discs.

NOTE

This procedure is included to prevent attempting a first seek with heads which might be out of line as a result of damage during shipment.

G. Connect the Model 120-2 Off-Line Tester to the drive as instructed in the Model 120-2 instruction manual.

H. Insert the desired unit number plug into the vertical slot in the operator control panel.

I. Turn the main power switch, S1, ON. The logic and power supply cooling fans will come on. Examine the machine for any signs of component overheating.

J. Position the START-STOP switch on the operator control panel to START. The disc pack will begin rotating and the main blower will come on. Following a pack temperature stabilization delay of 60 seconds, the heads will move out to the forward stop and then perform a reverse seek to cylinder 000. If any head chattering (the sound the heads make when they come in contact with the disc) occurs, power down immediately by positioning to STOP. Head chattering means that either a head(s) or disc pack is damaged. If no head chattering occurs, proceed with the installation check out.

K. Check head alignment as described in Section 4.7.

L. Check the index transducer circumferential alignment. The procedure for this check can be found in Section 4.4.2.

M. Use the off-line tester to perform random seeks in the AUTOCYCLE mode for 10 minutes. Then seek to cylinder 000. Verify that the carriage is at cylinder 000 by checking the cylinder scale on top of the Tee-block.

N. Select STOP with the START-STOP switch. Make certain that the disc pack comes to a complete stop in 10 to 15 seconds after STOP has been selected. This verifies that dynamic braking is working properly.

O. Attach the kick panels to the bottom of the machine with the clips which are already mounted. Replace the two top covers. Be sure the shroud area cover (right hand) is closed while installing it. Otherwise, the door-open interlock arm may not properly engage the paddle on the index transducer.

P. Install the two rear caster locks. To do this, turn the rear casters so that they face front to rear (rollers positioned nearest the outside of the cabinet) and use the screws provided to secure the locks to the bottom of the main frame from inside the cabinet.

Q. Select START with the START-STOP switch. When the disc drive motor comes up to speed, open the operator cover door. When it is open about 1", the heads should retract and the motor should shut off. Close the operator cover door.

R. Use the Off-Line Tester to make a quick write/read check.

1. Select READ/WRITE with the READ/WRITE-READ ONLY switch.
2. Write all ones with any head on cylinders 000 and 128.
3. Select the READ mode. Monitor the output of the Read Amplifier, A10, by connecting an oscilloscope to pin 4 of A10.
4. The double frequency (2F) pulses observed on the oscilloscope should be at a 5 MHz rate with less than ±10 ns jitter between adjacent pulses.

5. Write all zeros with the same head on cylinders 000 and 128. The single frequency pulses (1F) should be at a 2.5 MHz rate.

6. Disconnect the oscilloscope.

S. Select STOP with the START-STOP switch, turn the main power switch, S1, OFF and disconnect the Model 120-2 Off-Line Tester.

T. Connect the control unit Bus cable to the BUS IN connector, J3, on the interior control panel of the drive. If the drive is not the first drive in a string of drives, connect the cable that comes from the Bus Out connector, J4, of the previous drive to the Bus In connector, J3.

U. If the drive is the only drive or the last drive in a string of drives, plug a line terminator assembly into the Bus Out connector, J4.

V. Connect the proper Unit cable from the control unit to the Unit connector, J5, on the interior control panel. The control unit has a separate Unit cable for each drive.

W. When all cables are connected, replace the sheet metal cable cover.

X. All 660-0 machines, as they are shipped from the factory, have their Index/Sector boards (located in slot B05 on the logic door at the back of the machine and labeled IXR3) wired for the index only mode. Sector mode is a jumper-selected feature and is not needed in the 660-0.

Y. Turn the main power switch, S1, ON. Replace the front and rear panels.

Z. If the Model 660-0 is part of a string of drives (but not the last drive) it should be checked for proper power up sequencing. To do this, first make certain a disc pack is on the drive and the disc pack cover is closed. Leave the drive's START-STOP switch in the STOP position. Place the next drive's START-STOP switch in the START position. In a power up sequence from the control unit, the drive under test will not come on; it will be bypassed and the next drive in the string will turn on.

AA. To make certain that the next drive turns on when the drive being installed comes up to speed, place the START-STOP switch on both drives in the START position. Power up from the control unit and observe the first drive come up to speed (70% of spindle drive motor speed). At this time, the spindle drive motor on the second drive should begin rotating. Select STOP with the START-STOP switch.

BB. The drive is now ready for use.

SECTION 4.0
MAINTENANCE PROCEDURES

The procedures in this section are provided as an aid for servicing a drive. Alignment and adjustment procedures described herein should not be employed unless a problem has been specifically identified by careful troubleshooting analysis.

4.1 SAFETY PRECAUTIONS

Although the drive utilizes solid-state circuitry, the presence of primary ac voltage and the existence of moving parts requires caution when servicing the machine. The use of standard safety practices and observing the precautions listed below and elsewhere in this manual will prevent personal injury or damage to the drive.

Whenever working on primary power circuits, make certain the drive is unplugged at the AC IN and AC OUT connectors.

Unplug or plug in printed circuit boards only if the main power switch (S1) on the interior control panel is off.

Never spin a disc pack without the shroud assembly being in place.

Keep hands away from fast seeking read/write head arms.

Keep watches and tools away from the linear positioning motor, as it is surrounded by a strong magnetic field.

Keep hands away from the drive belt.

Never force an electrical seek without a spinning disc pack unless all head assemblies have been removed. Read/Write heads or disc surface could be damaged.

Do not operate the drive with the Read Amplifier board present, but with either Read/Write Amplifier (left or right) unplugged. Damage may result to the Read Amplifier board.

Grounding any back panel pin for test purposes may be necessary; however, do not connect any pin to a supply voltage unless directed by a test procedure or damage can result.

Unless absolutely necessary, do not apply power to the drive with the power supply gates swung out.

4.2 TOOLS AND TEST EQUIPMENT REQUIRED

A list of tools and test equipment useful in maintaining and repairing the drive is given in Table 4-1. Items asterisked are necessary to perform procedures in this section. Other items are for making repairs, for performing service operations that can not be easily performed with standard tools, or for installation of future field changes.

TABLE 4-1. TOOLS AND TEST EQUIPMENT

ITEM	DESCRIPTION
Volt Meter	VTVM, 10, 50 and 100 vdc scale, 1% accuracy
Oscilloscope	Dual trace, to 50 MHz, with two 1:1 probes
20 Surface Disc Drive Special Tools	Memorex Kit P/N 202148 CONSISTING OF: *Logic Extender PCB (P/N 1981) *Power Supply Extender PCB (P/N 1986) *20 Surface CE Disc Pack (P/N 150405) Amp Coax Pin Extractor (P/N 150690) Amp Pin Extractor 16-20G (P/N 150691) Amp Pin Extractor 10GA (P/N 150692) Elco Pin Extractor (P/N 150792) Marking Ink Solvent (P/N 153503) Fastener Field Kit (P/N 200505) *Carriage Moving Tool (P/N 200515) Detent Replacement Tool (P/N 200540) *Head Clamp Torque Wrench (P/N 200552) Wirewrap Tool (P/N 200553) Wire Unwrap Tool (P/N 200554) *Head Adjustment Tool (P/N 200555) *Lubrication Kit (P/N 200824) *Head Weldment Preloader (P/N 200945)

TABLE 4-1. TOOLS AND TEST EQUIPMENT (Continued)

ITEM	DESCRIPTION
20 Surface Disc Drive Special Tools (Cont)	Carriage Torque Wrench (P/N 200965) *120-2 Off-Line Disc Drive Tester (P/N 201291) *Head Cleaning Kit (P/N 202159) Carriage Alignment Tool Gauge (P/N 201452) Carriage Alignment Tool Arm (P/N 201453) EC Level Marking Kit (P/N 202147) CONSISTING OF: Marker Strap (P/N 5077) Stone Stamp Pad (P/N 153501) Permanent Marking Ink (P/N 153502) Rubber Stamp, 4 numeral (P/N 153504) Nylon Marking Pen (P/N 153505) EC Level Marker, 5/16 x 3/4 (P/N 201418)

4.3 POWER SUPPLY ADJUSTMENTS

Before proceeding with any other maintenance adjustment, always check the power supply voltages using the procedures given below. If the output of an individual power supply is within the limits specified do not change the adjustment. If a power supply output is outside the specified limits, adjust the output potentiometer so that the power supply delivers the exact voltage required.

4.3.1 ±15V +5V Power Supply

Adjustment of the ±15V + 5V Power Supply (P/N 001911) requires separate adjustment procedures for each power supply output. These procedures are given in the following paragraphs, and require the use of a voltmeter with an accuracy of at least 1%.

NOTE

Always have a drive running and warmed up (on for at least 15 minutes) before checking or adjusting a power supply.

4.3.1.1 ±15 Volt Supply

Check for +15 vdc at TP3 on board C02. If the output at TP3 is not within the range +14.25 to +15.75 volts, adjust potentiometer R8 to provide +15.0 volts at TP3. To increase the voltage output, turn the potentiometer clockwise.

Check for -15 vdc at TP2 on board C02. If the output at TP2 is not within the range -14.25 to -15.75 volts, adjust potentiometer R18 to provide -15.0 volts at TP2. To increase the voltage output, turn the potentiometer clockwise.

4.3.1.2 +5 Volt Supply

The +5 volt power supply is factory set and does not normally require field adjustment. The output voltage from this supply is monitored by a 5 Volt High-Low Detector circuit located on the Transducer Amplifier PC board (B06).

If the output of the +5 volt power supply should exceed the threshold of the high detector, or fall below the level of the low detector, the circuits will trigger silicon controlled rectifier SCR 1 (located on the side of the logic gate), thus clamping the +5 volt power supply to ground. This initiates an Emergency Heads Retract signal and causes the drive to shut off.

There are two designs of High-Low Detector circuits in existence, and procedures for adjusting the +5 volt power supply are dependent upon which design is used. The design configuration may be determined by noting the EC level of the Transducer Amplifier PC board (TAMP).

A. Adjustment procedure for drives with <u>TAMP at EC level 480 or lower</u>

NOTE

This procedure requires a voltmeter capable of resolving +5.0 volts with an accuracy of ±5.0 millivolts.

1. Measure the high threshold at TP8 of board B06. It must be +5.20 ±0.01 volts. If the threshold is out of this range, adjust

potentiometer R44 (bottom potentiometer on board B04) until the voltage at TP8 is +5.20 ±0.01 volts.

2. Measure the low threshold at TP4 of board B06. It must be 4.80 ±0.05 volts. If the threshold is out of this range, board B06 must be replaced.

3. Measure the +5 volt power supply level at TP6 of board B06. It must be +5.00 ±0.05 volts. If the threshold is out of this range, adjust potentiometer R31 (middle potentiometer on board C02) until the voltage at TP6 is +5.00 ±0.01 volts.

4. Test the operation of the 5 Volt High-Low Detector circuit in accordance with paragraph C below.

B. Adjustment procedure for drives with TAMP at EC level 487 or higher

NOTE

This procedure requires a voltmeter that has a ±2% to ±5% accuracy and can be used as a null detector (i.e., differentially).

1. The voltage at TP8 of board B06 is factory set by means of a precision zener diode to +5.60 ±0.05 volts and is not field adjustable. Verify that this voltage is correct within the accuracy of the instrument.

NOTE

The zener voltage above is used to generate the high and low thresholds, and a reference voltage. This reference voltage is brought out to TP26 of board B06.

2. The reference voltage at TP26 of board B06 is factory set to +5.10 ±0.06 volts and is not field adjustable. Verify that this

voltage is correct, within the accuracy of the instrument.

NOTE

The 5 volt power supply in a drive with a TAMP at EC 487 or higher is nominally set to +5.1 volts. The high threshold is 5.4 volts and the low threshold is 4.8 volts, thus giving a dc noise immunity of ±0.3 volt nominal.

3. Measure the voltage difference between the reference voltage at TP26 of board B06 and the 5 Volt Supply level at TP6 of board B06. The voltage must be ±0.05 volt. If not, adjust potentiometer R31 on board C02 (middle potentiometer) until the voltage difference between TP6 and TP26 of B06 is 0 volts ±10 millivolts.

4. Test the operation of the 5 Volt High-Low Detector circuit in accordance with paragraph C below.

C. Test procedure for 5 Volt High-Low Detector Circuit, all EC levels

1. Allow the drive to complete a First Seek.

2. Jumper pin 22 to pin 18 of the TAMP PC board (B06). This raises the voltage on the high detector above the high threshold, causing the following actions which must be verified.

   (a) The +5 volt power supply output is clamped to ground (between 0.0 and +1.2 volts).

   (b) The carriage is fully retracted.

   (c) The servo is disabled (i.e., no motor current is measured at current sense resistor R5).

3. Turn off the main power switch (S1) and Start/Stop switch (S2).

4. Turn on the main power switch. The level of the +5 volt power supply must go to its nominal value, +5.0 volts for drives with TAMP PC boards of EC 480 or lower, and +5.1 volts for drives with TAMP PC boards of EC 487 or higher.

5. Jumper pin 22 of the TAMP PC board to ground (any pin A or Z). This lowers the voltage on the low detector below the low threshold, which must clamp the level of the +5 volt power supply to ground. Verify that the 5 volt level is between 0.0 and +1.2 volts.

6. Return the drive to service.

4.3.2 ±36 Volt Supply

With the machine running and warmed up (on for at least fifteen minutes), check for +36 vdc at TP4 on board C03. If the output at TP4 is not within the range +35.0 to +37.0 volts, adjust potentiometer R8 to provide +36.0 volts at TP4. To increase the voltage output, turn the potentiometer clockwise.

Check for -36 vdc at TP1 on board C03. If the output at TP1 is not within the range -35.0 to -37.0 volts, adjust potentiometer R18 to provide -36.0 volts at TP1. To increase the voltage output, turn the potentiometer clockwise.

4.3.3 ±15 Volts Servo Power Supply

This ±15 volts is used by boards C01 and B04 and is independent of the ±15 volt supply described previously in this section.

With the machine running and warmed up (on for at least 15 minutes), check for +15 volts at TP4 on board C01: If the output at TP4 is not within the range +14.6 to +15.4 volts, adjust potentiometer R35 to provide 15 volts at TP4. To increase the voltage output, turn the potentiometer clockwise.

Check for -15 volts at TP3 on board C01. If the output at TP3 is not within the range -14.6 to -15.4 volts, adjust potentiometer R41 to provide -15.0 volts at TP3. To increase the voltage output, turn the potentiometer clockwise.

This power supply adjustment procedure is also included as part of the servo adjustment procedure, given elsewhere in this section.

4.3.4 +5 Volts Servo Power Supply

The +5 volt servo power supply is contained on Servo Protect PC board B02 (when present), and is not field adjustable. Verify that the voltage at TP11 on board B02 is between +5.0 volts to +5.2 volts. If not, board B02 must be replaced.

4.4 INDEX TRANSDUCER BLOCK ALIGNMENT

Accuracy of carriage tracking and alignment of the index transducer block are checked using the burst track located at cylinder 118 of the CE disc pack (yellow shield; P/N 150405). The following alignment check and adjustment procedures assume that the preparations described in paragraph 4.7.1 have been completed.

4.4.1 Transducer to Index Disc Gap (Radial Adjustment)

The gap between the index disc and the back of the index transducer is set at the factory to assure correct amplitude at the transducer output. No field adjustment is normally necessary unless an index transducer is defective. This adjustment is important to keep the contact between the disc and the index transducer to a minimum. Failure to do so may produce contamination, which could lead to HDI. If a check of the transducer outputs indicates that adjustment of the gap is necessary, perform the following steps.

A. Install a disc pack on the drive and leave the drive turned off.

B. Loosen the locking nut on the radial adjustment set screw. This screw is located on the back of the index transducer.

C. Turn the set screw counterclockwise while rotating the disc pack by hand.

D. Stop turning the set screw when the disc begins to rub slightly against the index transducer.

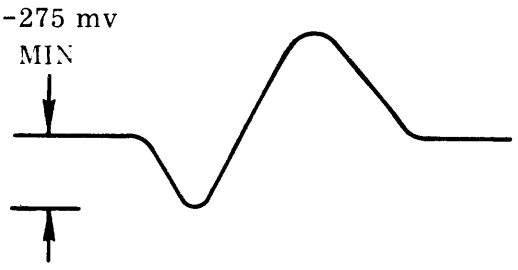
E. Turn the set screw in one fourth turn (90^{O} clockwise) so that the disc no longer rubs against the index transducer.

F. Hold the set screw steady and tighten the locking nut.

G. Start the drive and with both top covers on and closed, measure the amplitude of the negative lobe at TP20 on board B06. If it is less than 275 mv (Figure 4-1), the adjustment has been performed incorrectly or the transducer is defective.

NOTE

This adjustment affects the transducer circumferential alignment. Transducer circumferential alignment must be checked after the radial adjustment is completed.



(042-660)

Figure 4-1. Index Transducer Waveshape

4.4.2 Index Transducer Circumferential Alignment Check

A. Install a CE alignment disc pack and connect an off-line tester to the drive. Refer to the operating manual that accompanies the tester for instructions on how to install and operate the tester.

B. Use an oscilloscope with direct probes (1:1 attenuation). Set the display to A-B. Set the vertical scale at 50 mv/cm and the sweep-speed to 1 μs/cm.

Connect the two scope probes to E3 and E7 on the Read Preamplifier board that is mounted on the Read/Write Amplifier (Left) board. Sync on +Index (TP2 on board B05).

C. Turn the drive on, position the carriage to cylinder 118, and select head 09.

D. Check the pulse burst timing of the selected head. The scope trace should resemble the one illustrated in Figure 4-2. The pulse burst should occur 3 μs $\pm$2 μs after the leading edge of +Index.

E. Repeat the check on head 10. If the pulse burst timing is off for both of these heads, the index transducer block requires alignment.

4.4.3 Index Transducer Circumferential Alignment

While observing the burst track display (Figure 4-2) on the scope, tighten the adjustment nut slightly (Figure 4-3). If tightening the nut causes the pulse burst to appear closer to the 3 $\pm$2 μs range after index, continue tightening until they fall within that range. If not, loosen the nut until the pulse burst occurs after the optimum interval.

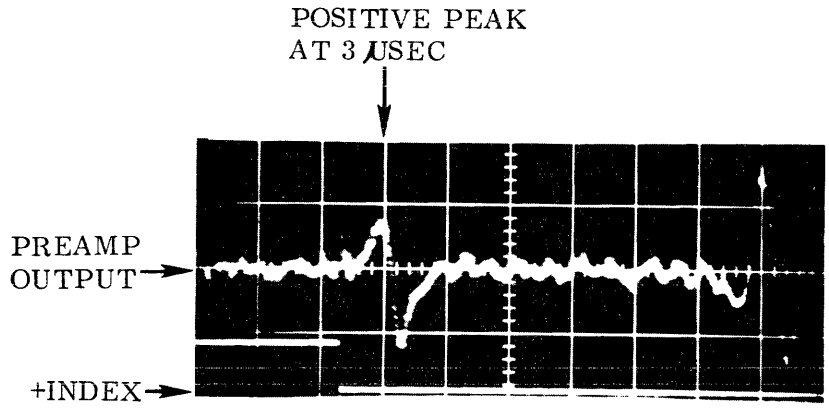


Figure 4-2. Pulse Burst

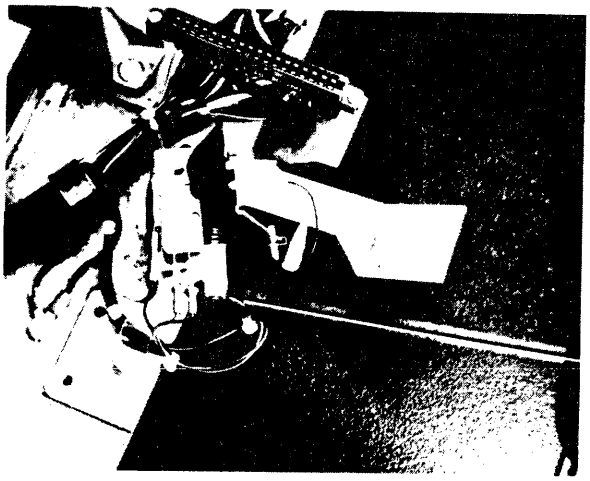


Figure 4-3. Index Transducer

4.5 CYLINDER TRANSDUCER REQUIREMENTS AND ADJUSTMENTS

Two sources of seek errors related to the cylinder transducer are: (1) incorrect amplitude at the transducer secondary output, and (2) incorrect time relationship between the generation of count pulses and the setting of the detent pawl. Both sources can be diagnosed by an oscilloscope check.

4.5.1 Alignment Specifications

The following list and Figure 4-4 define specifications for acceptable cylinder transducer alignment. The first three items relate to error source (1) above, the last two relate to error source (2) above.

A. Transducer oscillator output must be 3.0 volts ±0.15 volts peak-to-peak.

B. Peak-to-peak crest amplitude (the maximum output achieved between two adjacent null regions), when the carriage is not detented, must be within the range of 400 mv to 1400 mv. This is true at all points along the rack.

C. Null amplitude anywhere along the rack must be less than 80 mv peak-to-peak.

D. The ratio of the maximum peak-to-peak crest amplitude to the minimum peak-to-peak crest amplitude for adjacent crests must be 1.2 to 1.0. This is defined as the crest ratio.

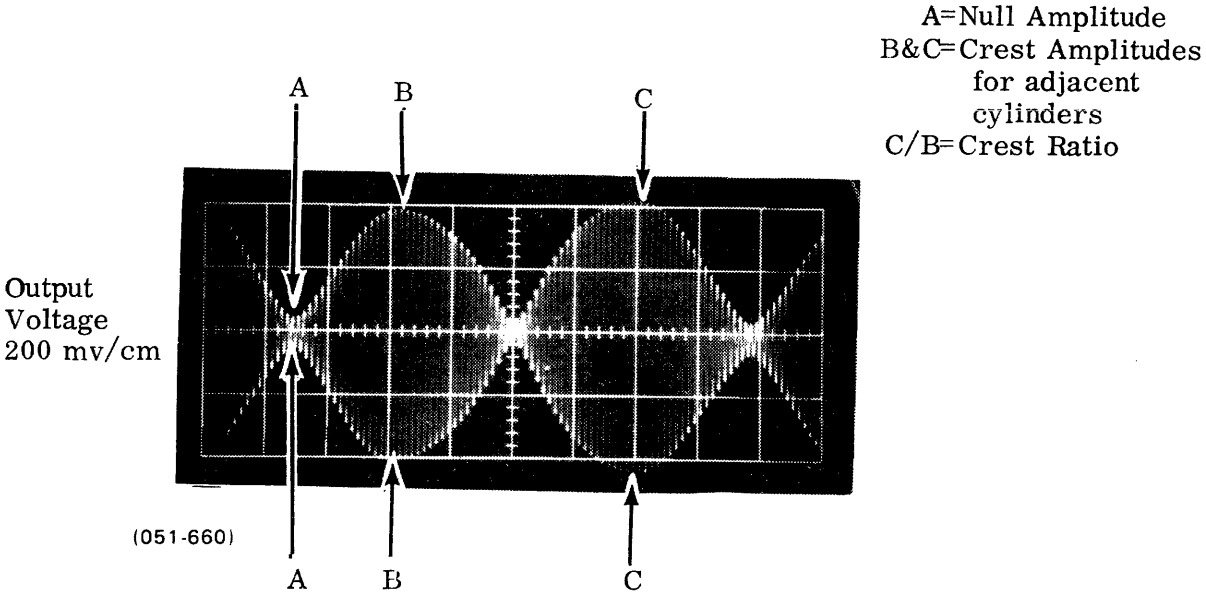


Figure 4-4. Transducer Output

E. Peak-to-peak amplitude when the carriage is detented must be between 70% and 90% of the peak-to-peak crest amplitude associated with the detented position. This requirement applies for all detented cylinder positions.

Where these values specify maximum and minimum levels, levels above the minimum or below the maximum specified are acceptable.

4.5.2 Transducer Oscillator Check

The oscillator signal is applied to the primary winding of the transducer. Before examining the cylinder transducer output characteristics, it is important to be sure the oscillator output is within tolerance.

A. Set the oscilloscope vertical scale to 1 volt/cm.

B. Connect the scope probe to pin 16 of the TAMP board (B06). The output should be 3.0 volts ±0.15 volts peak-to-peak.

C. If the oscillator output is outside the required range, adjust R4 on B06 until the output meets the specifications.

4.5.3 Transducer Alignment Check

Remove the shroud assembly to gain access to the cylinder transducer and detent mechanism. For steps that require manually positioning and detenting the carriage, the servo and detent actuator should be disabled by removing fuse F4, the +55 vdc fuse, and carefully loading the heads by hand with no pack installed on the drive. Contact of a head's surface with the opposing head will not cause damage if the loading is done slowly and carefully.

For steps in the procedure that require small carriage movements, e.g., moving to an adjacent cylinder to determine crest ratio, the use of a carriage moving tool (P/N 200515) is recommended. This tool is installed as follows:

A. Move the carriage to a convenient position.

B. Screw the hand wheel well onto the threaded shaft of the tool.

C. Insert the shaft of the tool through the hole in the plastic block on the back of the linear motor and screw it all the way into the threaded hole in the end of the tachometer rod attached to the Tee-block.

D. Spin the handwheel clockwise until it comes to rest against the plastic block.

The wheel can then be turned clockwise to move the carriage slowly in the reverse direction until the desired position is reached.

CAUTION

Be sure to remove the tool before re-enabling the servo and performing seeks, or damage may result to the tool or linear motor.

4.5.3.1 Check Position Indicator Scale

Move the carriage by hand to the home position (cylinder 000). Although the scale on top of the Tee-block identifies home position, its accuracy should be checked by examining the position of the detent pawls with respect to the rack (refer to Figure 4-5). When the carriage is in the home position, the bottom pawl is engaged and there are two rack teeth in back of the top pawl. A small dental mirror is useful for observing the tooth-pawl relationship without removing head assemblies from the drive.

4.5.3.2 Transducer Amplitude Check

A. Set the oscilloscopes vertical scale to 100 mv/cm and the sweep-speed to 5 ms/cm.

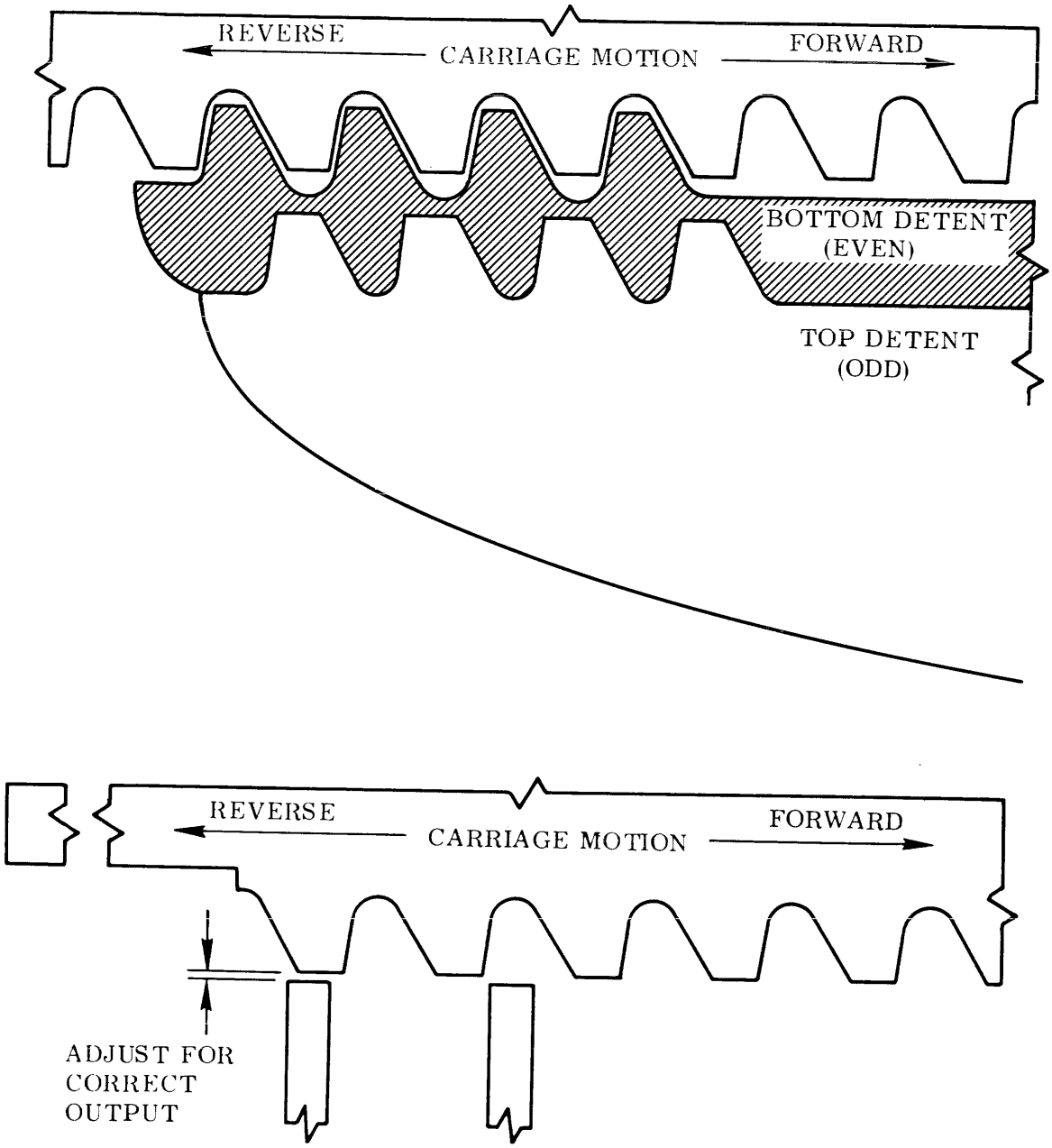


Figure 4-5. Rack and Cylinder Transducer at Cylinder 202

B. Connect the scope probe to pin 8 of board B06.

C. Observe the scope trace while moving the carriage by hand (at a moderate speed) over the range of cylinders 000 to 202. Note the changing crest and null values along the rack. In particular, note the following characteristics:

1. The maximum peak-to-peak crest value along the rack

2. The minimum peak-to-peak crest value along the rack

3. The peak-to-peak null value along the rack

D. The values of the crests and nulls must conform to the specifications outlined in paragraph 4.5.1, steps B and C.

4.5.3.3 Transducer to Pawl Setting Time Relationship Check

Seek errors can be caused by the detent pawl setting too soon or too late after a compare condition is reached. This problem can be corrected by pivoting the transducer slightly until the pair of primary-secondary coils are properly aligned with the rack teeth and their output is balanced.

A. Detent the carriage at cylinder 202 (as indicated on the position indicator).

NOTE

While performing the following operation observe the scope trace closely; it is important to detect slight changes in the waveform. This operation may require several tries before confident observations are obtained.

B. Carefully move the carriage back one cylinder (i.e., to cylinder 201), using the carriage moving tool.

The waveform must increase slightly and then decrease. The value of the initial detent output should be 70% to 90% of the crest value. Be sure to simulate holding current when checking amplitude while the carriage is detented. This can be done by pressing forward on the Tee-block.

C. Move the carriage back one more cylinder (i.e., to cylinder 200). The waveform must conform to the above.

D. The ratio of the highest crest value to the lowest crest value (for adjacent positions) as determined during steps B and C above must not exceed 1.2 to 1.0.

E. Remove the carriage moving tool and manually move the carriage back and forth, observing the areas which appear to have higher crest ratios than that determined in A and B above.

The detented output percentage of the crest ratio must be within specifications over the entire range of cylinder positions.

F. Refer to section 4.5.4 or 4.5.5 for adjustment procedures, if required.

4.5.3.4 Transducer to Pawl Positional Relationship Check

The following check should be made to verify that any field adjustments made to the transducer are correct. Improper positional alignment will result in consistent seek errors and will cause the drive to restore to an incorrect cylinder position.

A. Move the carriage to rest against the forward carriage stop.

B. Detent at this position.

C. Mount the carriage moving tool on the linear motor.

D. Slowly move the carriage in the reverse direction by turning the wheel clockwise (with slight forward pressure) against the Tee-block.

E. Observe the secondary output of the cylinder transducer and allow the carriage to detent at each position as the carriage is moved back.

F. Stop at the first detented position after observing the first true null. Ignore the false, high amplitude, null which occurs first as the carriage is backed away from the stop.

The cylinder position arrived at must be 202 as read on the position indicator scale.

Failure to detent at cylinder position 202 after the above procedure indicates either a cylinder transducer adjusted to the wrong tooth on the rack or an improperly adjusted cylinder position indicator scale. Repeat the appropriate checks in this procedure to determine which error is present and correct it.

4.5.4 Cylinder Transducer Partial Realignment Procedures

If seek errors occur and if the cylinder transducer characteristics are found deficient (as a result of performing the analysis described in paragraph 4.5.3), the problem may be corrected by alignment. The procedures in paragraph 4.5.4.1 are designed to increase or decrease the transducer output amplitude as needed.

The procedures in paragraph 4.5.4.2 are designed to assure that the generation of count pulses occurs when the detent rack teeth are in the correct position with respect to the detent pawl teeth. This relationship is important because it determines whether or not the detent pawl sets at the right instant following Compare.

4.5.4.1 Amplitude Adjustment

If the crest amplitude is too low at one or more points along the rack, make the adjustment described in steps A through C below. If a null is too high, make the adjustment described in step D below.

A. Move the carriage to the cylinder which showed the lowest crest amplitude.

B. With the blade of a beryllium screwdriver set against the back of the leaf spring (A in Figure 4-6), tap the handle of the screwdriver lightly until the amplitude increases the necessary amount. This technique is capable of increasing the amplitude by about 50 mv. If the deficiency is greater than that, turn the drawback screw (B in Figure 4-6) counterclockwise a quarter turn. If necessary, tap the leaf spring again.

C. Check for clearance between the transducer and rack by pushing against the back of the transducer (where the coils are -- not at the base). If there is clearance, output of the secondary coils will increase. If the output does not increase, the transducer is too close to the rack and step D should be performed.

D. To draw the transducer back away from the rack (to provide clearance or to decrease a high null), turn the draw-back screw clockwise slightly until there is either enough clearance or the null amplitude is low enough. If correcting a high null, perform this operation with the carriage at the position where the highest null was observed.

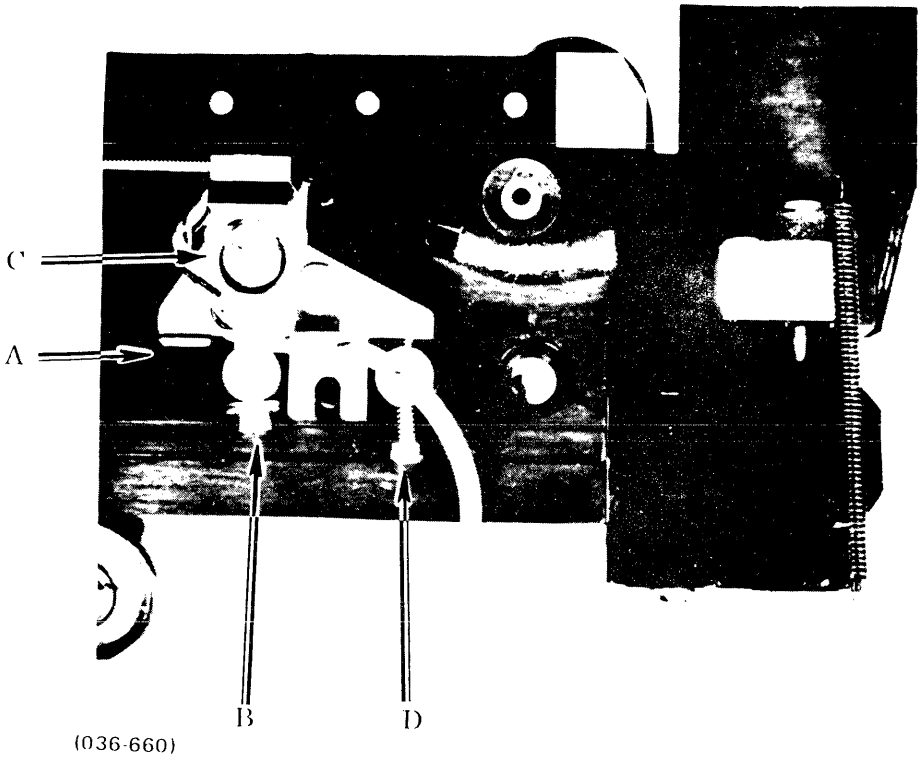


Figure 4-6. Cylinder Transducer Adjustment Details

E. Move the carriage to any other cylinder positions which showed low peaks or high nulls. The new output at these positions should be satisfactory since the adjustment was made at the worst case cylinder position.

4.5.4.2 Detented Output and Crest Ratio Adjustment

If the detented-output to crest-output relationship or crest ratio is out of tolerance, it may be possible to readjust by the following procedure. If it is convenient, it is recommended that the transducer be completely readjusted following the procedure in paragraph 4.5.5.

A. Detent the carriage at the cylinder position of highest percentage (as determined in section 4.5.3.3) detent to crest relationship.

If the highest percentage is 70% or less, completely readjust per paragraph 4.5.5. If greater than 70% perform step B.

B. Turn screw D (Figure 4-6) clockwise to reduce the detented amplitude by 10%. If the amplitude starts to increase, keep turning clockwise to raise the amplitude to the crest, then down to within 70% to 90% of the crest. It is advisable to stop at 90% on the first try to allow readjustment later, if additional specifications of amplitude and crest ratio are not met.

C. Re-check all specifications per paragraph 4.5.3.

4.5.5 Transducer Adjustment Procedure

Use the following procedure when it is desired to completely readjust the cylinder transducer, i.e., when a new transducer is being installed.

A. Retract the carriage.

B. Loosen the hold-down screw (C in Figure 4-6).

C. Loosen the retract screw (B in Figure 4-6), two turns.

D. Slowly back the pivot screw (D in Figure 4-6), off so that the leaf spring can pivot the transducer clockwise. Stop turning when the transducer rests against the dowel pin (E in Figure 4-6).

E. Re-tighten the hold down screw C, until slight resistance is felt.

F. Tighten screw B until the carriage rack just clears the cylinder transducer pole face. The average output from the transducer should be above 350 mv to aid meeting future amplitude requirements.

G. Detent at any convenient cylinder position.

H. Turn screw D clockwise until the first crest in amplitude is observed. Continue turning this screw until an amplitude of 70% to 90% of the crest value is reached.

I. Detent to an immediately adjacent cylinder position and verify that the detented amplitude is within 70% to 90% of the associated crest value. It may be necessary to readjust the value set in step H to a different value within the 70% to 90% range in order to meet both step H and I requirements.

J. Check for the specifications given in paragraph 4.5.1, steps B, C, and D as described in paragraphs 4.5.3.2 and 4.5.3.3. If necessary, adjust the detented output to another value in the 70% to 90% range in order to meet these additional amplitude, crest ratio, and clearance requirements. This procedure may require several iterations before all specifications are satisfied.

4.6 SERVO ADJUSTMENT

4.6.1 Servo Setup Procedure

This procedure describes routines to be followed for making the three basic servo adjustments on the Servo Control board (B04): (1) offset, (2) reverse turnaround, (3) maximum seek time. These adjustments cannot be made unless the cylinder transducer is properly aligned. Before proceeding with the servo setup, check cylinder transducer alignment as described in paragraph 4.5.

4.6.1.1 ±15 Volts to Servo

The Servo Driver board (C01) has two potentiometers that are adjusted at the factory to provide the ±15 volts used by boards C01 and B04 (this ±15 volts

is independent from the ±15 volts supplied to other logic). Although these potentiometers are set at the factory and will not normally require field adjustment, the voltages should be verified before making any adjustments to the servo.

A. Connect a scope ground lead or VOM common lead to TP7 on board C01.

B. Connect a scope probe or +VOM lead to TP4 on board C01. The output at TP4 should be between +14.6 volts to +15.4 volts. If the output is outside this range, adjust R35 (bottom potentiometer on board C01, labeled +15) to provide +15.0 volts at TP4.

C. Move the scope probe or +VOM lead to TP3 on board C01. The output at TP3 should be between -14.6 volts to -15.4 volts. If the output is outside this range, adjust R41 (top potentiometer on board C01, labeled -15) to provide -15.0 volts at TP3.

4.6.1.2 Offset Adjustment

The offset adjustment regulates holding current. To check this adjustment:

A. Initiate a seek or restore operation to set up holding current.

B. Connect a scope probe to TP5 on board C01 or TP2 on board B04.

C. If the output is not +200 mv ±10 mv, check the inputs to board B04. An explanation for the excessive output may be that some other input(s) besides - Holding Current is active.

NOTE

If one or more other inputs to board B04 are active following a seek or restore operation, there is a problem originating elsewhere in the logic.

D. If -Holding Current is the only active input to board B04, adjust R77 (the middle potentiometer on board B04, labeled 0) until the output is +200 mv.

NOTE

This adjustment should never be necessary unless the error amplifier (A4 on board B04) is replaced.

4.6.1.3 Reverse Turnaround Adjustment

The reverse turnaround adjustment controls the amount of time allowed for the carriage to stop and go forward at the end of a reverse seek, prior to engaging the detent. Incorrect reverse turnaround time may result in seek errors, and may also cause data errors due to off track position of the heads due to vibrations which do not damp out sufficiently before data transfer is attempted. To verify that the reverse turnaround setting is correct, proceed as follows:

A. Connect a scope probe to TP3 on board B04. This is the tachometer output test point. Connect the external sync lead to TP5 on board A06 so that the trace will sync on +Seek Reverse.

B. Set the vertical scale at 100 mv/division and the sweep speed at 2 ms/division. Set the trigger slope to +.

C. Initiate a series of alternate seeks between cylinders 96 and 100, using the off-line tester. The resulting scope trace should resemble the one shown in Figure 4-7.

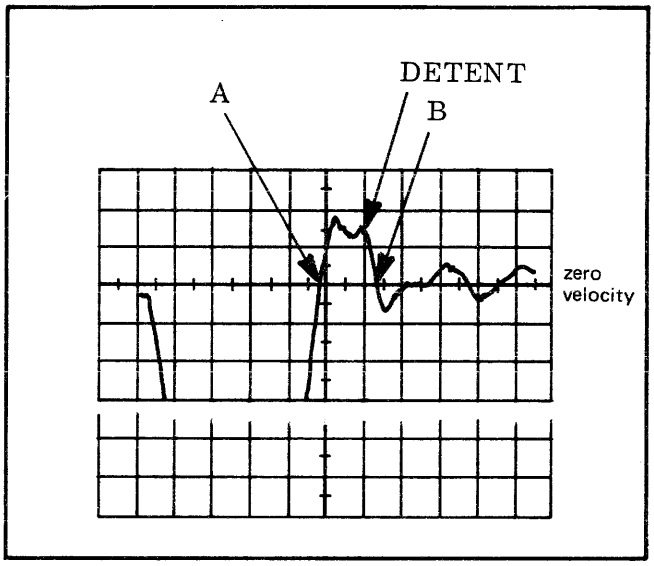


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Figure 4-7. Four Cylinder Alternate Seeks

NOTE

The portion of the trace between A and B represents the forward motion of the carriage following turnaround. Typically, this period is longer at the cylinder 000 end of the rack. It is ordinarily about 0.5 ms shorter at the cylinder 200 end of the rack.

D. The turnaround period must be between 1.5 and 6.5 ms. For initial adjustments, adjust R31 (the top position on board B04, labeled R) to obtain 1.5 to 1.7 ms. Adjustment at the lower end of specification leads to better performance.

E. The peak voltage amplitude during turnaround must always be between 100 mv and 300 mv. Out of tolerance readings indicates a need for readjustment of R31 or possible circuit defects, requiring replacement of boards C01 or B04.

F. At the time of contact between the detent pawl and rack (as shown in Figure 4-7), the voltage must be less than 200 mv.

G. The above requirements must be met for all four cylinder seeks, and R31 readjusted as required. Observations between cylinders 96-100, 097-101, and 198-202 are usually sufficient to verify all variations in seeks.

H. Switch the off-line tester operating mode to Sequential Reverse Seeks. The reverse turnaround period must exceed 2.0 ms. If the reverse turnaround is not within the time specified, readjust R31 then repeat steps C through G above.

4.6.1.4 Maximum Seek Time Adjustment

The maximum seek time potentiometer (R84) corrects for variations in the tachometer and ±15 volt servo power supplies by providing an optimum maximum seek velocity.

A. Be certain all 20 heads are installed on the Tee-block so that carriage/Tee-block mass is normal.

B. Connect the scope probe to TP3 on board B04 (tachometer output). Connect the external sync probe to TP4 on board A06 (+Forward Seek).

C. Set the vertical scale at 500 mv/division and the sweep speed at 10 ms/division.

D. Initiate 200 cylinder seeks from cylinder 000 to cylinder 200 and back. This is the alternate cycle mode when the off-line tester is used. The resulting scope trace should resemble the one shown in Figure 4-8.

NOTE

The total forward seek time is represented by the portion of the trace between C and D. This period should be 62 ±2 ms.

E. If the time from point C to point D is not 62 ms, adjust R84 (the bottom potentiometer on board B04, labeled M) until the maximum seek time is 62 ms.

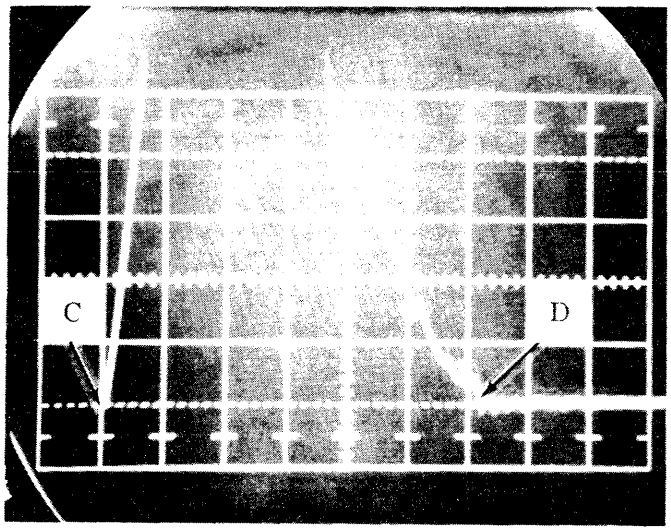


Figure 4-8. 200 Cylinder Seeks (Forward)

4.7 OFF-LINE HEAD ALIGNMENT

4.7.1 Head Alignment Check

The following preparations must be made before head alignment can be analyzed.

A. See that the shroud is in place.

CAUTION

Be certain the carriage and heads are fully retracted before installing or removing a disc pack.

B. Install a CE alignment disc pack.

CAUTION

Do not operate a drive with the RWAL or RWAR boards removed or damage to the hex inverters (D3 & D4) on certain earlier versions of the RAMP boards may result.

C. Preparation of the off-line tester. To substitute an off-line tester for the control unit, perform the following steps (ignore steps 1 and 2 below and perform step D if an off-line tester is not available).

1. Check to be certain all switches on the off-line tester are in the off position.

2. Disconnect P13 and P14 on the logic gate Bus In, Bus Out and Unit cables and install the off-line tester cables.

D. Head and Pack Thermal Equilibrium. The temperature stabilization cycle, which assures standard operating temperature during head alignment, is performed as follows:

1. Run the drive for 1 hour with a disc pack installed and all covers on.

2. Run the drive for 20 minutes with a CE alignment pack installed and the control cover off.

E. Scope Connection. Use a scope with direct probes (1:1 attenuation), setting the display to A-B so the two test points are read differentially. Set the vertical scale at 5 mv/cm and the sweep speed to approximately 3 ms/cm (or enough to observe one complete revolution).

Connect the two scope probes to E3 and E7 on either the right Read Preamplifier board or the left Read Preamplifier board, depending on which head is to be checked. Use the left Read Preamplifier board for heads 1, 2, 5, 6, 9, 10, 13, 14, 17 and 18 and the right Read Preamplifier board for the other 10 heads. Sync externally on +Index (TP2 on board B05).

NOTE

Connecting a jumper wire on the back panel from A10-04 to A10C will provide a cleaner signal at the output of the read preamp and make the scope presentations more readable. Be sure this jumper is removed when head alignment checks are completed.

Once the above preparations have been completed, the off-line head alignment check is performed as follows: Perform steps A through C and bypass step D if an off-line tester is being used. If an off-line tester is not available, ignore steps A through C and perform step D.

A. Position the heads to cylinder 73 with the off-line tester. Refer to the manual that accompanies the tester for operating instructions.

B. Select one of the heads with the off-line tester.

C. Select the READ mode with the tester. When the head starts reading, the scope trace should resemble the curve in Figure 4-9.

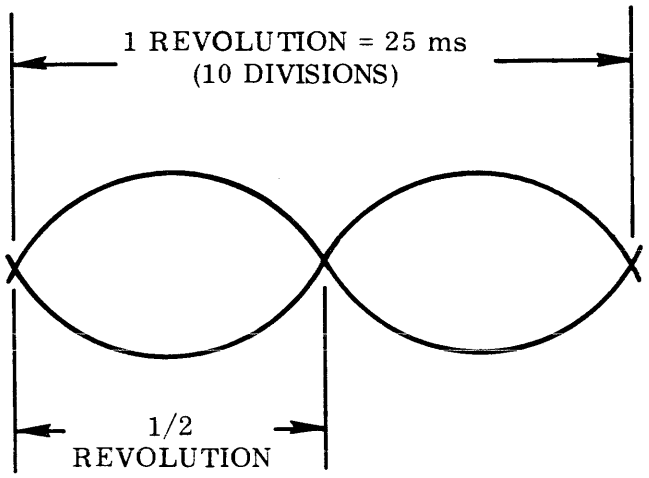


Figure 4-9. Head Alignment Read Signal at One Revolution

D. The following steps must be performed if an off-line tester is not used.

1. Position the heads to cylinder 73 via the control unit.

2. Select one of the heads by jumpering the appropriate Head Select line to ground. This can be accomplished at the Line Select input lines on the Read Amplifier board (A10). For best results all the heads should be checked to arrive at an average alignment.

3. A read signal should appear on the scope; the trace will resemble the curve in Figure 4-9.

E. The first zero crossing is at +Index. The third zero crossing should occur 10 divisions later (this is determined by the sweep speed

setting on the oscilloscope). If the head is properly aligned, the second zero crossing will fall on, or very near, the centerline of the display, i.e., the two lobes of the trace will be equal.

Record the amount of deviation (if any) of the second zero crossing from the centerline on the scope.

F. Repeat check E above for all the heads.

G. All the heads should be checked so that they are aligned with respect to each other, as well as with respect to the reference cylinder. To do this, calculate the average deviation of all the heads that do not deviate more than ±0.8 division from the centerline. All the heads must be within ±0.4 division from the average deviation for all heads and ±0.8 division from the centerline on the scope.

H. Adjust any head that does not meet the requirements outlined in step G to within ±0.2 division of the average deviation.

NOTE

Do not adjust any head that is within the tolerances.

4.7.2 Head Alignment

The following alignment procedure assumes that the conditions necessary for performing a head alignment check (described in paragraph 4.7.1 are satisfied. In addition, check to be certain that all switches on the off-line tester are off and the off-line tester cables are properly connected.)

A. Position the heads to cylinder 73 of the CE alignment disc pack.

B. Select the head that is to be aligned.

NOTE

If all the heads on the front side of the Tee-block (B and D type heads) are to be aligned, start with the bottom assembly and work up.

If all the heads on the back side of the Tee-block (A and C type heads) are to be aligned, start with the top assembly and work down.

C. Select the READ mode with the off-line tester.

D. Loosen the four screws holding the two clamps which hold the head-arm assembly in place just enough to allow the assembly to move when moderate pressure is applied (Figure 4-10).

E. Pull lightly against the tab on the head-arm assembly so that the assembly moves all the way back in its slot against the Tee-block.

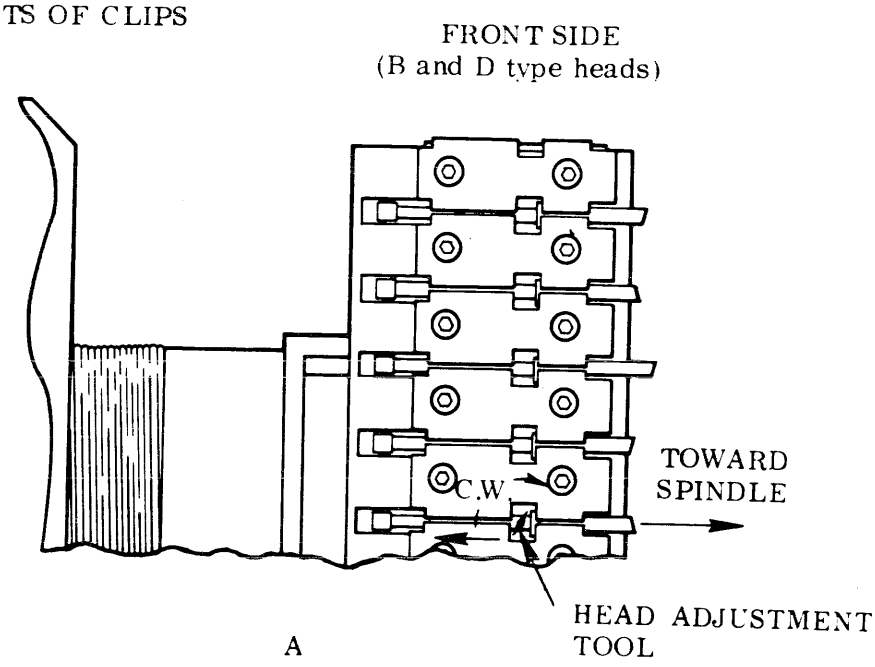
F. Tighten one of the clips (bottom clip for a B or D type head; top clip for an A or C type head) to restrict its movement without restricting the movement of the head-arm assembly

NOTE

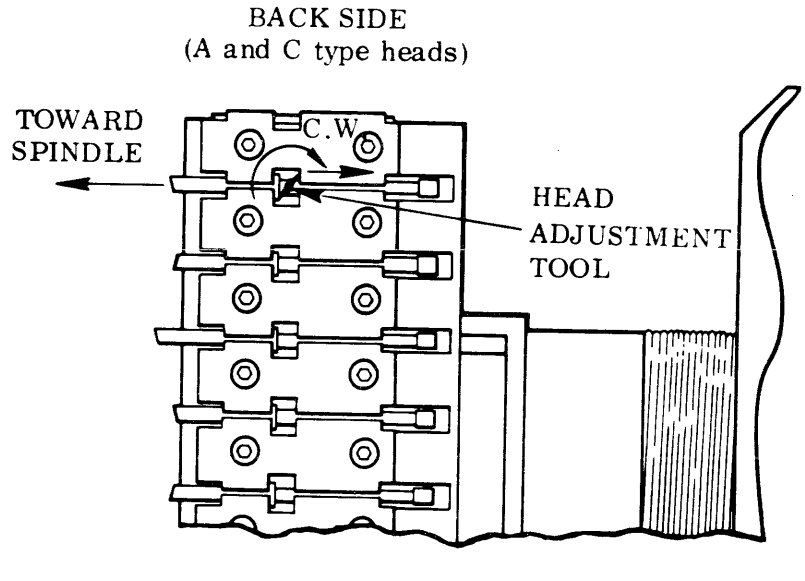
The alignment tool should always push back against the clip that is tightened down. Since the tool twists clockwise, the bottom clip must be tightened on the front side of the Tee-block and the top clip on the back side.

G. While observing the trace on the scope, carefully twist the alignment tool clockwise so the assembly moves forward (toward the spindle). Stop twisting as soon as the second zero crossing falls within the tolerances listed in paragraph 4.7.1, step G.

NOTE: THIS ILLUSTRATION SHOWS ONLY THE TOP 10 SETS OF CLIPS



A



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B

Figure 4-10. Head-Arm Mounting Clips and Alignment Slots

H. If the head goes too far forward, reperform steps E through G.

NOTE

Do not try to align the head while pushing the assembly back. Always align the head while adjusting it in the forward direction.

I. Before tightening the second clip, check the alignment of the adjacent head(s). To do this, it is necessary to deselect the head just aligned and select an adjacent head.

J. When the adjacent heads are aligned, tighten all clips with the Memorex head clamp torque wrench (P/N 200552).

4.8 HEAD-ARM ASSEMBLY REPLACEMENT

A. Remove the shroud area and control covers from the drive.

B. Disconnect the head plug from its board.

C. Remove the two side clamps (one above and one below the head arm) which hold the assembly in the Tee-block slot (Figure 4-10).

D. Grip the head arm assembly at points A, B, and C (Figure 4-11) with the Memorex head arm assembly replacement (preloader) tool (P/N 200945).

E. Close the jaws of the tool so that the head arm assembly leaf spring is bent back enough to clear the cam supporting it.

CAUTION

Do not touch the head shoe face or press against the flexure. Refer to Figure 4-11, points D and E. Even slight pressure against the flexure could bend it and impair the head's flying attitude.

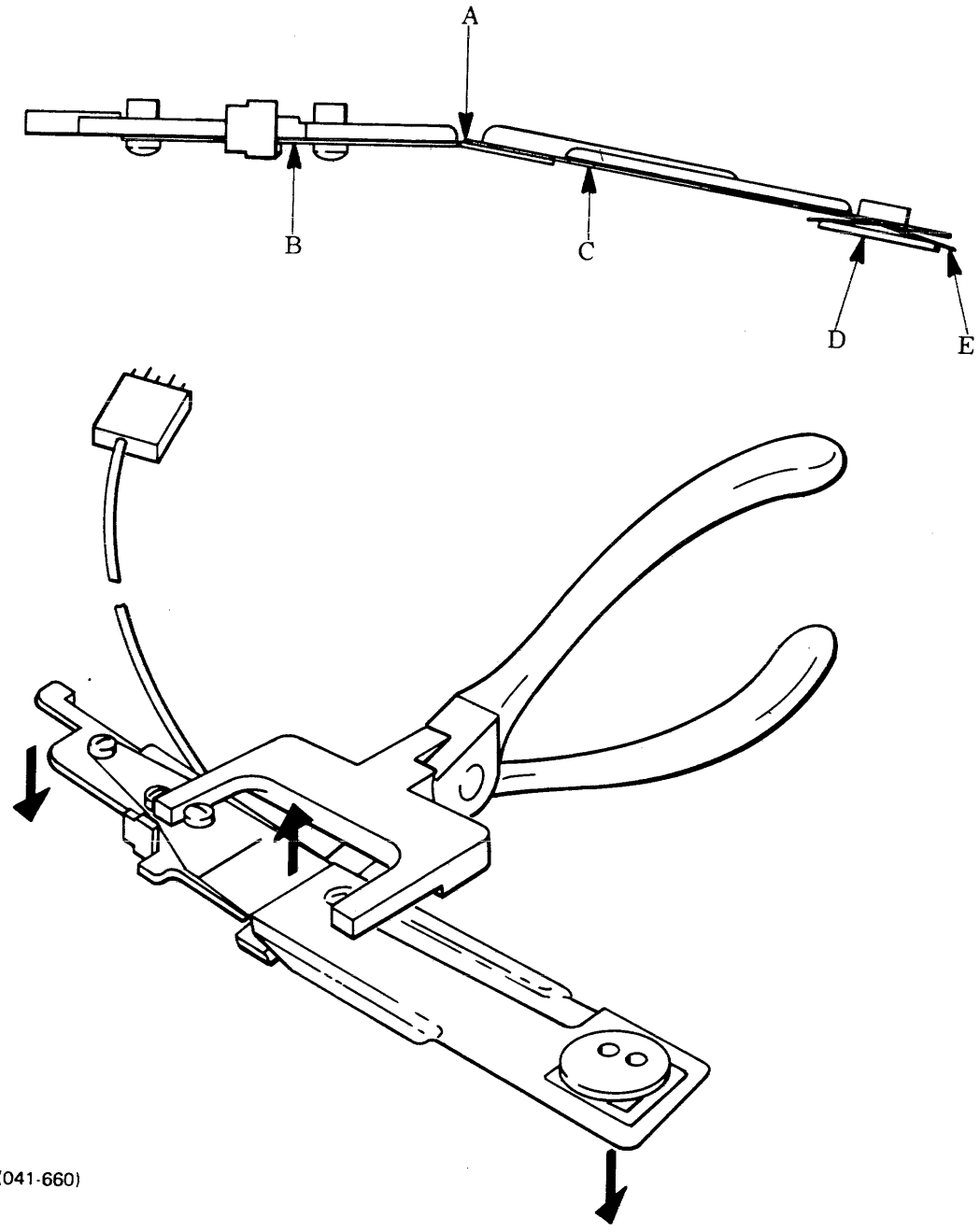

Figure 4-11. Preloading the Head-Arm Assembly for Installation

F. While holding the jaws of the tool closed, extract the assembly from the Tee-block slot.

G. To install a head-arm assembly, reverse steps A through E.

NOTE

When the head is properly mounted, the bleed holes are located in the leading half of the head shoe (relative to disc pack rotation).

Whenever a read/write head is replaced, an alignment check must be made on it and the two adjacent heads (one adjacent head if the replaced head is at the top or bottom of the Tee-block). This is advisable because the adjacent head-arm assemblies may move slightly when the clips they share with the replaced head are removed.

4.9 SPINDLE DRIVE MOTOR REPLACEMENT

4.9.1 Motor Plate Assembly Removal

A. On the interior control panel, turn the main power switch (S1) off and disconnect the drive motor power plug.

B. Remove the spindle drive belt (see paragraph 4.10 for removal procedure).

C. Place a support block on the cross member of the interior control panel under the drive motor to hold it in place during removal.

D. Break the adhesive bond holding the three shoulder screws (Figure 4-12) and loosen the screws.

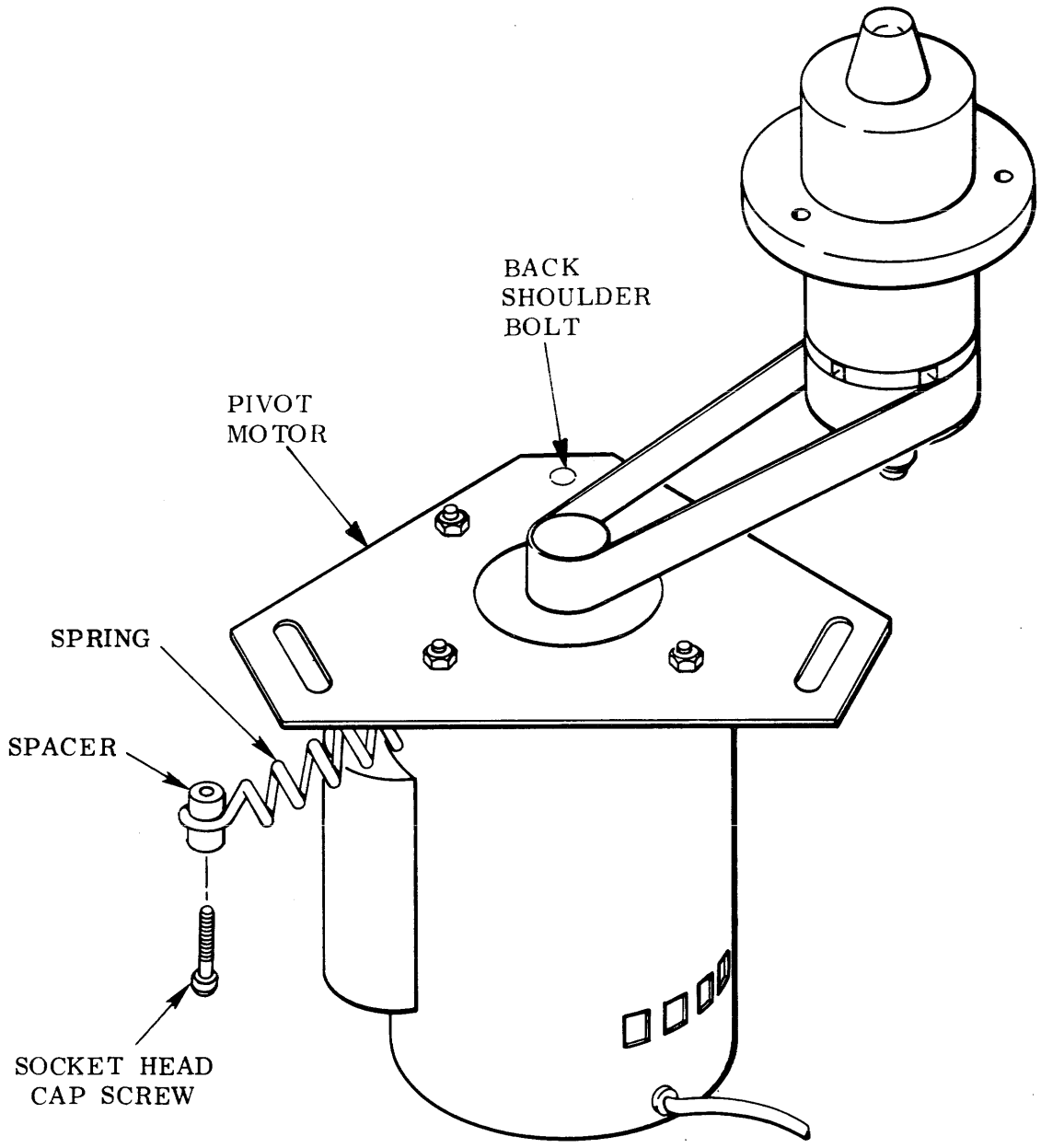

Figure 4-12. Drive Motor and Mount Assembly

E. Pivot the motor plate assembly slightly to extend the belt tension spring. Remove the two shoulder screws and plastic washers in the slotted area.

F. Allow the motor plate assembly to pivot back, releasing tension on the spring, and remove the remaining shoulder screw and washer.

G. Lift the motor plate assembly from the drive.

H. Remove the four sets of nuts and lock washers, offset bracket, vibration mount - hex standoff assembly and pulley.

4.9.2 Motor Plate Assembly Installation

A. Install the vibration mount - hex standoff assembly, offset bracket, and four sets of nuts and lockwashers.

NOTE

Be certain the spring bracket orientation corresponds to Figure 4-12.

B. Install the motor plate to the vibration mount studs and secure with the four nuts and lock washers.

C. Install the motor pulley and position it on the motor shaft so that the distance from the top face of the pulley to the top surface of the motor plate is 0.240 ±0.015 inches.

D. Apply adhesive (P/N 110877) to the shoulder screw threads.

E. With the motor supported by a block, insert the shoulder screw and washer in the pivot hole located in the deck plate. Snug down the screw (finger tight).

F. Fit the free end of the belt tension spring into the groove on the post and pivot the motor plate assembly slightly to extend the spring.

G. Install the two shoulder screws and washers in the slotted holes.

H. Allow the motor plate assembly to pivot back, releasing tension on the spring.

I. Tighten all three shoulder screws to approximately 10 inch-lb of torque. Excessive tightening will indent the aluminum base plate or break off the screw head.

J. Install the drive belt (refer to paragraph 4.10 for installation procedure).

K. Insert the drive motor power plug in its socket.

4.10 SPINDLE DRIVE BELT REPLACEMENT

A. On the interior control panel, turn the main power switch (S1) off and unplug the spindle drive motor.

B. Pivot the drive motor on its back shoulder bolt (Figure 4-12); this will allow enough slack in the belt for it to drop off the pulleys.

C. Slip the belt between the pack-on switch and the bottom of the spindle, and remove the belt from the drive.

D. If the pulleys are not clean, clean them with isopropyl alcohol.

E. Install a new belt.

NOTE

Be sure the replacement belt is the right length for the drive: 60 Hz drives use P/N 200230; 50 Hz drives use P/N 200253.

The smooth side of the belt should be inside against the pulley faces.

The belt should be centered on the flat of the motor pulley.

F. Check the pack-on switch clearance; refer to paragraph 4.11 for details.

4.11 SPINDLE ASSEMBLY REPLACEMENT

A. With the main power switch (S1) off, remove the shroud area cover, shroud assembly and spindle drive belt (refer to paragraph 4.10 for belt removal procedure).

B. Remove all four spindle flange bolts.

C. Lift the spindle out of the baseplate.

D. Install new spindle assembly (P/N 200003) and tighten the flange bolts securely.

NOTE

Be sure the new spindle pulley is clean; if it isn't, clean it with isopropyl alcohol.

E. Replace the spindle drive belt.

F. Check brake pawl-to-pulley clearance. If necessary, deform the linkage rod to provide the necessary clearance (0.100 ±0.050 inches). See Figure 4-13.

G. Install a disc pack on the spindle and check clearance between the bottom of the spindle and the lower contact arm of the pack-on switch (see Figure 4-14). If necessary, deform the upper contact arm of the switch to allow 0.025 ±0.010 inches of clearance.

H. Remove disc pack and replace the shroud assembly.

I. Check head alignment. (Refer to paragraph 4.7 for head alignment procedure.)

4.12 TORSION ROD REPLACEMENT (located in shroud area cover)

A. Turn off the main power switch (S1) located on the interior control panel.

B. Remove the disc pack, if one is installed.

C. Remove control cover.

D. Remove the shroud area cover:

1. Release the two latches located at the back of the drive where the top cover meets the main frame.

2. Tilt the rear of the cover assembly up to approximately 5^{o}.

3. Pull the assembly toward the front of the drive approximately 3/4 inch.

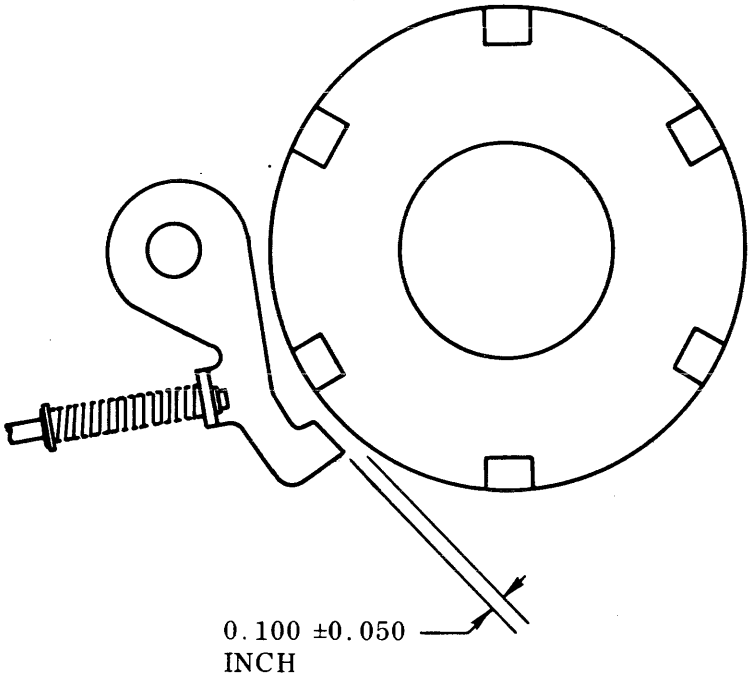

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Figure 4-13. Brake Pawl-to-Spindle Pulley Clearance

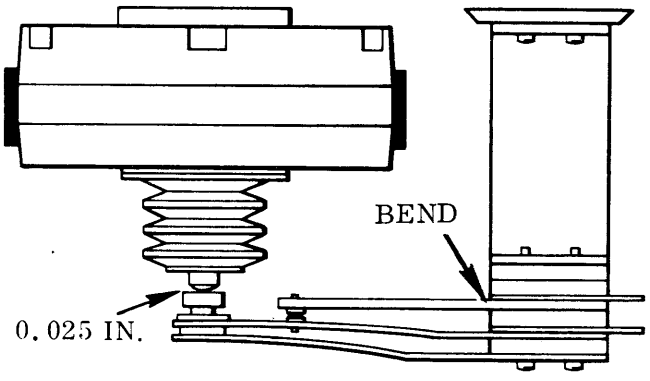

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Figure 4-14. Pack On Switch to Spindle Clearance

4. Lift the cover straight up and off the machine.

CAUTION

Do not hit the index transducer or the PC board mounted on the cam tower. Hold the cover with both hands in a way that will keep the door closed no matter how the cover assembly is tilted. This is important for the next step.

E. Stand the shroud area cover assembly on a clean, flat surface in a vertical position (90^{o} from normal on its rear surface).

F. Allow the door to lie back gently into a fully open position. This releases tension on the torsion bars.

G. Remove the two metal clamps which bundle the four torsion bars.

H. Lift the torsion bars out of their respective slots in the two plastic bearing blocks.

NOTE

Rods which miss contact with the hinge (when the door is fully open) by more than 0.03 inch should be replaced.

I. Install torsion rods by reversing steps D through G.

NOTE

The first two rods installed should always be on the same side (i.e., install the upper rod and the lower rod on one side; then install the upper and lower rods on the other side).

J. Lubricate the rods sparingly at points of fricting with a silicone grease (P/N 110875).

4.13 INDICATOR LAMP REPLACEMENT

CAUTION

Do not replace lamps by removing the front glass. Removing the glass may scratch the film insert behind the glass.

A. Remove the rear panel of the machine by pulling it out from the top; it is held on by magnetic clips.

B. Release the two latches located at the back of the drive where the control cover meets the main frame.

C. Lift the control cover from the rear.

D. On the rear of the operator control panel assembly, remove the lamp socket plate.

E. Tilt the lamp socket plate to expose the front of the bulbs.

F. To remove a bulb, pull it straight out. These are slide base sockets, not threaded sockets.

G. Replace the lamp socket plate.

4.14 PREVENTIVE MAINTENANCE

Preventive maintenance for the drive consists of both scheduled and unscheduled maintenance routines. A tabulation of preventive maintenance routines is given in Table 4-2. The table lists the periodicity, where applicable, and references the paragraph where the procedure to be performed is given.

Maintenance operations should be performed at the indicated intervals to assure reliable operation of the drive. Preventive maintenance should be limited to these routines as long as the drive is functioning normally.

TABLE 4-2. PREVENTIVE MAINTENANCE CHART

PROCEDURE	REFERENCE	PERIODICTY
Detent Rack Cleaning and Pawl Lubrication	4.14.1	60 days
Head Inspection and Cleaning	4.14.2	30 days
Spindle Oiling	4.14.3	60 days
Detent Pawl Oiling	4.14.4	60 days
Spindle Brake Oiling	4.14.5	60 days
Carriage Way Oiling	4.14.6	60 days
Detent Pawl/Rack Oiling	4.14.7	60 days
Head Unload Cams Replacement	4.14.8	1 year
HDI Prevention and Recovery	4.14.9	As Required
Linear Tachometer Maintenance	4.14.10	As Required
Logic Circuit Check	4.14.11	60 days

4.14.1 Detent Rack Cleaning and Pawl Lubrication

Clean the surface of the detent rack with a soft bristle brush dampened with 90% isopropyl alcohol. Apply a small amount of grease to the flat surface of both detent pawls where the actuator push rod makes contact.

4.14.2 Head Inspection and Cleaning

Check the bearing surfaces and bleed holes of the heads for contamination. Contamination is the presence of slight oxide streaks on the bearing surfaces, oxide buildup around the periphery, or an excessive accumulation of oxide or other foreign material in the bleed holes. Clean only those heads that show signs of contamination. If dark brown or black streaks (burned oxide or aluminum) exist on a bearing surface, the head has experienced Head to Disc Interference (see paragraph 4.14.9) and must be replaced.

If the head shoes need cleaning, clean the heads per the following procedure using a head cleaning kit (P/N 202159).

A. Remove the shroud area top cover, the disc pack, and the shroud assembly. Turn the main power switch (S1) located on the interior control panel off.

B. Move the carriage out by hand until the load/unload ramp is just at the point of riding off the cam. Do not load the heads.

C. Wrap a Kimwipe* tissue around a head paddle (a wooden tongue depressor will do) and dampen (do not soak) one end of it with 91% isopropyl alcohol (9% distilled water). Wipe the bearing surface of each head thoroughly with the dampened portion of the Kimwipe. After wiping the bearing surface with the dampened end of the paddle, push the paddle further into the assembly and use the dry portion of the Kimwipe to dry the surface of the head. Remove the paddle by pushing it toward the center of the carriage until it is clear of the cleaned head and then pull it out. This technique will prevent the dampened portion of the Kimwipe from contacting the cleaned surface of the head.

CAUTION

It is extremely important that the surface of the head be dried immediately after cleaning with alcohol to prevent evaporation which will result in a residue on the bearing surface.

D. After all contaminated heads have been cleaned, check the flexures and arm assemblies for loose pieces of Kimwipe tissue and remove them.

E. Return the carriage to the retracted position and inspect the gimbal flexures and arms for broken welds. Replace any defective assemblies.

*Kimwipe is a trade mark of Kimberly Clark.

F. Replace the shroud assembly and disc pack and turn the main power switch back on.

G. Start the drive.

H. Replace both top covers.

NOTE

There is no scheduled preventive maintenance for disc packs. If the packs are handled properly and the drive is maintained regularly, there is no need for pack cleaning.

4.14.3 Spindle Oiling

Apply a drop of number 10 oil in the top of the spindle to ensure easy removal of the disc packs.

4.14.4 Detent Pawl Oiling

Apply two drops of number 10 oil between the detent pawls.

4.14.5 Spindle Brake Oiling

Place a drop of number 10 oil between the washer and pawl of the mechanical spindle brake. Compress the spring on the brake spindle to seperate the washer and pawl.

4.14.6 Carriage Way Oiling

Clean the carriage way with a Kimwipe dampened with 90% isopropyl alcohol and wipe dry. Apply a light coat of number 10 oil on the carriage way (under the rollers).

4.14.7 Detent Pawl/Rack Oiling

Apply a drop of number 10 oil to the surface of the detent pawl and the detent rack to provide rust protection. Clean the face of the cylinder transducer with a Kimwipe dampened with 90% isopropyl alcohol.

4.14.8 Head Unload Cam Replacement

A. Turn off the main power switch (S1).

B. Remove both top covers. Remove the shroud assembly.

C. Carefully push the carriage all the way out to the forward stop.

D. Unscrew the cam screws and remove the old cams by pulling them first along the head arms away from the cam support, and then sideways away from the arms.

E. Leaving the carriage in the forward position, install the new cams in the reverse order of step C. Make sure the cams are pushed against the sides of the recesses in the cam support before the screws are tightened. If the cams were installed properly, there will be clearance between the outer edges of the head arm assemblies and the vertical surfaces of the cams.

F. Push the carriage back (away from the spindle) until the heads are fully unloaded.

G. Re-install the shroud assembly and top covers.

4.14.9 Prevention, Recognition and Recovery from HDI

As stated previously, the shoe does not contact the disc, but rides above it on a lubricating film of air.

Head to Disc Interference (HDI) results when the lubricating air film fails. The main causes of HDI are foreign particles in the lubricating film, contamination buildup on the surface of the shoe or disc, or a defective disc surface.

Because of the catastrophic propagation tendency of HDI, preventive techniques should be employed to minimize susceptibility, recognition symptoms should be clearly understood, and proper recovery procedures should be followed. Discussions of these areas are given in the following subparagraphs.

4.14.9.1 Prevention of HDI

A. Preventive Maintenance

Proper preventive maintenance of the drive at the scheduled periods; especially the head/arm assemblies, filtration system, moving parts and head cams.

B. Handling and Storage

Packs should always be stored with the covers on, and only in cabinets that are clean and free of dust and foreign particles. The pack covers (top and bottom) should also be together when the pack is removed, and stored in a clean location. Any cracked or broken covers should be replaced immediately. Disc packs should be handled with care to avoid dropping or bumping. Never place a dropped pack on a drive.

C. Access Door

Never leave the access door on a drive open unnecessarily. The longer it is open, the greater the susceptibility to contamination.

D. Pack Labels

Use only manufacturer recommended pack labels, installed in the specified locations. Labels that work loose are a source of contamination.

CAUTION

Tobacco smoke and ashes can create serious contamination problems for disc drives and disc packs.

4.14.9.2 Recognition of HDI

HDI may be recognized by one or more of the following symptoms:

A. Repetitive Hard Read Errors

Because of adverse propagation effect, do not move any pack with repetitive hard read errors to more than one additional drive. If errors persist, then the possibility of HDI exists and must be investigated.

B. Audible Tinkling Sound

An audible tinkling sound from the disc which may progress to a screech.

C. Visible Damage

Visible damage on any surface characterized by one of the following:

1. Any scratch (radial, tangential or diagonal) where the aluminum substrate is exposed.

2. Concentric adjacent scratches of any length.

3. A single scratch over three inches (approximately) in length.

4. Imbedded particles.

NOTE

The edge of a disc may have aluminum visible and not indicate HDI.

D. Oxide on Bearing Surface in Shoe

Dark brown (oxide) or black streaks (burned oxide and/or aluminum) anywhere on the bearing surface indicates HDI. Slight oxide streaks on the bearing surface, oxide buildup around the periphery, or contamination in the bleed holes may not indicate HDI.

A discoloration of the epoxy around the read/write core also indicates HDI.

4.14.9.3 Recovery from HDI

A. Inspect all heads and determine which ones are involved in the HDI.

B. Replace heads involved in the HDI and clean the remaining heads as described in paragraph 4.14.2.

C. Inspect all disc packs which were recently on the drive in question for possible damage. If any surface in a pack is badly damaged (cannot be restored to operation by cleaning) then the pack must be replaced. Clean only those disc surfaces that are contaminated or have been involved in the HDI. The cleaning procedure is as follows:

1. Remove access plate from side of the shroud assembly on the drive.

2. Install disc pack.

3. Wrap a Kimwipe around a cleaning paddle (wooden tongue depressor will do) and dampen (do not soak) one side with 91% isopropyl alcohol (9% distilled water).

4. Insert paddle between discs and exert light pressure on surface to be cleaned while manually rotating the pack.

5. Slowly withdraw the paddle while the pack is rotating.

6. Immediately turn paddle over and dry the cleaned surface while slowly rotating the pack. Make sure the alcohol is not allowed to evaporate, or harmful residues will form.

7. Slowly withdraw the paddle while the pack is rotating.

8. Check for and remove any remnant pieces of Kimwipe.

9. Replace access plate on the side of the shroud assembly.

D. Mount a good disc pack on the recovered drive and power up. After the drive comes to ready, power down, and check for possible HDI. If there are no indications of HDI, power up and run in a random seek mode for 15 minutes. Power down and check for possible HDI. If no indication of HDI exists, align the replaced heads, clean the inner surfaces of the shroud and restore the drive to operation. If HDI occurs during any of the above operations, repeat the entire recovery procedure.

E. If the damaged pack was salvageable, then certify the pack by placing it on a drive and following the procedures outlined in step D.

F. Check all the heads in all the drives that the damaged pack was used on for possible HDI. If any indication of HDI exists, repeat the entire recovery procedure for each drive affected.

4.14.10 Linear Tachometer Maintenance

A faulty linear tachometer can result in seek errors. Two likely areas of trouble with the tachometer are tach rod interference and tach rod demagnetization.

4.14.10.1 Tach Rod Interference (Rubbing)

To check for tach rod interference, proceed as follows:

A. Disable servo by removing F4, the +55 vdc power supply fuse.

B. Install CE alignment disc pack and start drive.

C. Manually position the carriage to the forward stop.

D. Remove the plastic tach retainer from the rear of the linear motor by removing the two mounting screws.

E. Note the relationship of the tach rod to the tach coil as the carriage is manually re-positioned to the fully retracted position. The tach rod must not rub against the tach coil sufficient to move the coil. Although full clearance should exist between the tach rod and the tach coil, a slight rubbing (insufficient to move coil) is acceptable.

F. If rubbing is excessive, replace the complete tach assembly.

4.14.10.2 Tach Rod Demagnetization

Tach rod demagnetization can be caused in several ways:

A. Contact with steel or magnetic objects such as linear motor magnets, tools, or tach coil retaining springs.

B. Dropping the tach rod.

C. High temperature - over temperature condition on the linear motor which damages the bobbin.

D. Tach rod to tach coil interference.

A demagnetized tach rod can be detected by performing the Maximum Seek Time adjustment as given in section 4.6.1.4. If the 60 ms maximum 200 track seek time cannot be met, replace the entire tach assembly.

4.14.11 Logic Circuits Check

The drive must be connected to the control unit and operating with a CE alignment disc pack before the following checks can be made.

4.14.11.1 Seek Incomplete Check

A. With the control unit, perform diagnostic (HEX) 40 to the drive with track 207 programmed on the control unit's DATA switches. This is an illegal address and should cause a seek incomplete in the drive. Seek incomplete can be verified by observing the UNIT NUMBER/READY indicator on the operator control panel going out.

CAUTION

If the UNIT NUMBER/READY indicator does not go out, press STOP on the drive's START/STOP switch. Failure to do this will cause damage to the bobbin.

B. After verifying a seek incomplete condition, perform a restore operation by pressing the drive's START/STOP switch to STOP.

C. Remove diagnostic (HEX) 40.

D. After the disc stops spinning, START the drive.

4.14.11.2 Up Speed Check

A. Remove the rear panel of the drive.

B. Swing open the logic gate (See figure 1-4). Do not swing open the dc power supply gate.

C. Momentarily ground pin 4 of logic card B06. The heads must retract out of the pack due to the loss of up speed.

D. Close the logic gate and replace the rear panel.

4.14.11.3 System Protection Check

A. Place the START/STOP switch in the STOP position.

B. Remove the control cover (See figure 1-1a) so that the carriage is accessible.

C. Move the carriage out by hand until the head retract switches turn off. The servo motor should try to retract the heads with a pulsating current which can be felt. This confirms proper operation of the system protection circuit.

CAUTION

Do not move the heads out into a stationary disc pack. HDI could result when the heads come in contact with the disc surfaces.

D. After verifying proper operation of the system protection circuit, replace the control cover.

4.8 Functional Description of Interface Lines ~~(continued)~~

INPUT LINES (continued)

LINE NAME FROM CONTROLLER	FUNCTION DURING VARIOUS CYCLES I. Control Cycle	II. Set Cylinder	III. Set Head
Bus 0	Set Write	Cylinder 128	
Bus 1	Set Read*	Cylinder 64	
Bus 2	Seek Start	Cylinder 32	
Bus 3	Reset head register*	Cylinder 16	Head 16
Bus 4	Set erase	Cylinder 8	Head 8
Bus 5	Select head	Cylinder 4	Head 4
Bus 6	Restore	Cylinder 2	Head 2
Bus 7	Set head advance	Cylinder 1	Head 1

TAG LINES
- Control
- Set Cylinder
- Set Head ~~and Direction~~

*NOTE: Control tag, with Bus 1 and Bus 3 both a ONE, causes a diagnostic reset of FILE UNSAFE.

TO RESET FILE UNSAFE OUTPUT BUS 1, BUS 3 & CONTROL TAG

ENG. CHANGE NO.										
SHEET AFFECTED										
DATE										