MEMOREX
Equipment Group

ENGINEERING SPECIFICATION

Number 882000

Sheet 1 of 186

FUNCTIONAL SUBSYSTEM SPECIFICATION 7300 PROCESSOR

EC CONTROL: MIDWEST PRODUCT DEVELOPMENT LABORATORY

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1.0 SCOPE

This document defines the characteristics and properties of the Memorex 7300 Processor, S/N 4 and beyond.

1.1 Index

2.0 APPLICABLE DOCUMENTS

The following documents form a part of this specification. to the extent specified herein.

Any conflicts between applicable documents and/or this document shall be referred to the cognizant engineering group for interpretation, clarification, and resolution.

2.1 Functional Specification

882052 Integrated File Adapter

882053 Integrated Communications Adapter

882046 Integrated Line Printer Adapter (S/N 4 thru 11)

882067 Integrated Card Reader Adapter (S/N 4 thru 11)

882045 Integrated Reader-Punch Adapter

882076 Integrated Card Reader Adapter (S/N 12 and beyond)

882051 Basic Data Channel

882059 Power System

882068 7300 Main Storage

2.2 Other Reference Documents

881803 TTL High Speed Ground Rules

881805 TTL Medium Speed Ground Rules

881828 TTL1-TTL2 Interface Ground Rules

881879 Final Assembly, Type MSC70 Module

881986 Printed Circuit Board Design Guide

882019 A.C. Power Requirements for Equipment

882020 Environmental Requirements for Equipment

890500 7200/7300 Processor Machine Feature Index

882038 7300 Processor Test Specification

Midwest Operations Quality Assurance Manual

3.0 REQUIREMENTS

The 7300 Processor shall meet the requirements as stated within this Section.

The 7300 Processor shall support the Main Storage facility referenced in Section 2.1 and shall conform to the Address, Data and Control Signal conventions as described within that applicable document.

3.1 General Description

The Memorex 7300 Processor shall be defined as a micro-program controlled, I/O oriented, Business Data Processor as shown in Figure 1.

The Central Processing Unit shall provide "multi-state" processing and shall consist of five functional units designated as Control Storage, Arithmetic Logic Unit, Register File, Register Option and Timing/Control. Operations within the CPU shall be performed, primarily, in 16-bit parallel mode.

The 7300 Processor cabinet shall house the processor elements which, in addition to the Central Processing Unit and Main Storage, shall include Integrated Adapters for communicating with Disc Drives, Line Printers, Card Equipment, and various Terminal devices with the latter including a Keyboard/Printer for manual entry and "hard copy" display of data. Binary data entry and display shall also be possible from the 7300 System Control Panel which shall be mounted on the front of the 7300 Processor Cabinet.

Communications with Disk Drives and Terminal devices shall be handled by the Integrated File Adapter (IFA), and the Integrated Communications Adapter, (ICA), respectively. Communication with other types of I/O equipment shall be effected by means of I/O Channel(s), either via adapters within the 7300 Processor cabinet or through compatible external controllers.

See Figure 1 for the 7300 Processor Block Diagram.

See Figure 2 for the approximate placement of Processor elements within the 7300 Cabinet.

3.1.1 Processor Organization

The Central Processing Unit shall be capable of assuming any one of ten unique "states" as determined by the output of a Resource Allocation Network.

Eight of these Processor States, designated 0 through 7, shall be unique by means of the assignment of registers within the Register File. This assignment of Registers shall be accomplished such that normal Micro-command execution in one of these Processor States shall not affect the contents of those registers assigned to the remaining Processor States. Thus, the implementation of Processor States 0 through 7 shall be accomplished primarily by means of partitioning the Register File. For each of these eight Processor States, the registers assigned, and normally reserved exclusively for their use, shall be referred to as "Dedicated Resources". All other resources within the CPU for which no exclusive assignments are made, shall be commonly available to all these Processor States and shall be referred to as "Common Resources".

Figure 3 depicts the fundamental partitioning of the Register File.

The ninth state of the Central Processing Unit, designated Console State, shall be unique as a result of functional assignment to a portion of Control Storage. The Console State shall access its assigned portion of Control Storage in conjunction with certain switch settings on the 7300 System Control Panel. In addition, logic within the Timing/Control area shall be reserved for Console State usage in the case of operations which shall not be Micro-command controlled, namely Control Storage Read and Control Storage Write operations.

The tenth state of the Central Processing Unit, designated Null State, shall be unique to the extent that it shall control CPU operation in the absence of resource utilization on the part of the other nine Processor States. The Null State shall require usage of the Timing/Control logic only, for the purpose of resynchronizing resource requirement requests for Processor States 0 through 7 and the Console State.

The minimum duration of any one Processor State shall be an 800 n/s interval during which the execution of a maximum of eight micro-commands shall be possible. This interval shall be referred to as a "major cycle". (The number of Micro-commands which may be executed during a major cycle shall be dependent on the nature of the Micro-commands themselves, up to a maximum of eight).

The maximum duration of any one Processor State shall be determined according to the occurrence of resource utilization requests, the priority of all such requests, and the ability (under Micro-command control) of a Processor state to utilize consecutive major cycles. The maximum duration of any one Processor State shall always be equal to an integral number of major cycles. The maximum duration of each major cycle shall be determined according to whether a Main Storage reference is required, whether the Error Correcting Code (ECC) Feature is present when a Main Storage reference occurs and whether the associated Processor State has met all the criteria for consecutive cycle operation. As a result, the maximum duration of one major cycle shall be 1.2 u/s, with all 100 n/s increments from 800 n/s through 1/2 u/s being possible as determined by the combination (s) of the conditions previously mentioned and as depicted in the following chart.

ECC Feature Present
Main Storage Reference
Consecutive Cycle Mode
Total Major Cycle Interval

ECC Feature Present	Main Storage Reference	Consecutive Cycle Mode	Total Major Cycle Interval	
No	No	No	E0 E1 E2 E3 E4 E5 E6 E7	.8 u/s
No	No	Yes	E0 E1 E2 E3 E4 E5 E6 E7 E8 E9	1.0 u/s
No	Yes	No	E0 E0′ E1 E2 E3 E4 E5 E6 E7	.9 u/s
No	Yes	Yes	E0 E0′ E1 E2 E3 E4 E5 E6 E7 E8 E9	1.1 u/s
Yes	Yes	No	E0 E0′ E0″ E1 E2 E3 E4 E5 E6 E7	1.0 u/s
Yes	Yes	Yes	E0 E0′ E0″ E1 E2 E3 E4 E5 E6 E7 E8 E9	1.2 u/s

NOTES:
1. E0, E0′, E0″, and E1 through E9 represent minor cycle intervals of 100 n/s each.
2. E0 through E7 provide Micro-command execution.
3. E8 and E9 provide hardware operations associated with Consecutive Cycle Mode operations.
4. E0′ provides a hardware idler associated with Main Storage reference cycles.
5. E0″ provides a hardware idler associated with Main Storage reference cycles in the presence of the ECC Feature.

Figure 4 depicts the fundamental timing sequence involved in a Multi-State Operation involving Processor States 0 through 7, without priority, and using minimum interval major cycles each.

3.1.2 Register File

The Register File shall be divided into four major groups designated as follows:

Basic Register File
Extended Register File, Group I
Extended Register File, Group II
Extended Register File, Group III

Three of these major groups shall be further partitioned for the purpose of creating dedicated resources corresponding to Processor States 0 through 7. For a diagram depicting Register File organization, see Figure 3.

a. The Basic Register File shall consist of 256 16-bit registers which are general purpose and under Micro-command control only. These 256 registers shall be divided into 8 sets of 32 registers each, corresponding to the 8 Processor States having 32 Registers each. Logically, these registers shall be arranged in a matrix of 8 columns by 32 rows. Normal Micro-command execution shall be confined to the column corresponding to the Processor State of the CPU. A special mode of Micro-command execution referred to as "Boundary Crossing Mode" shall permit any Processor State to reference the registers in other Processor State columns.

b. The Extended Register File, Group I, shall consist of 16 18-bit registers which are special purpose and under hardware as well as Micro-command control. Eight of these registers shall be allocated, one each to Processor States 0 through 7 and shall be designated as "F Registers" with only the right-most 16-bits being used. The contents of the appropriate F Register shall be read in advance of the major cycle(s) allocated to a Processor State, shall be available for Micro-command modification during the major cycle(s) allocated to a Processor State and, if altered by Micro-command, shall be updated in the appropriate F Register after the completion of the major cycle allocated to a Processor State, all under hardware control. The remaining eight of these Registers shall be allocated, one each to Processor States 0 through 7 and shall be designated as "Pu Registers". The contents of the appropriate Pu Register shall be hardware controlled in a manner similar to that previously described for the F Register.

However, the purpose of the Pu Register shall be related to Control Store Address, Overflow/Link status and Skip/Control Store Parity Error Status. For a diagram depicting the timing relationships of the hardware controlled sequences for F and Pu, see Figure 4. Logically, the registers within this Group are arranged in a matrix of 8 columns by 2 rows. Normal Micro-command execution shall be confined to the column corresponding to the Processor State of the CPU. A special mode of Micro-command execution referred to as "Boundary Crossing Mode" shall permit any Processor State to reference a single register in other Processor State columns per major cycle.

NOTE: Special conventions shall apply when addressing Pu by means of Micro-commands. Moreover, the left-most 2 bit positions of Pu which relate to Skip/Control Storage Parity Error status shall be reserved primarily for hardware control.

c. The Extended Register File, Group II shall consist of 10 16-bit registers commonly available to all Processor States. Two of these registers, designated "Tie Breaker (T)", and "Privileged Mode, (PM)", shall be under Micro-command control only and shall serve as general purpose, common resource registers. The remaining eight of these registers shall be under hardware as well as Micro-command control and shall serve as varying, special purpose, common resource registers. Micro-command control of the special purpose registers within this group must meet special conventions as determined by the varying hardware controlled functions performed at the inputs and/or outputs of these registers.

d. The Extended Register File, Group III shall consist of a maximum of 64 16-bit registers, architectually a part of the Register File but physically a part of the Integrated Adapters and I/O Channels within the 7300 Processor. (It is not within the scope of this document to describe the actual numbers, widths or functions of the registers within this Group. Such information shall be provided by the appropriate documents in Section 2.1). For the directly addressable maximum, these 64 registers shall be divided into 4 sets of 16 registers each, corresponding to Processor States 0 through 3, having 16 registers each. Logically, these registers shall be arranged in a matrix of 4 columns by 16 rows. Micro-command execution shall be unconditionally confined to the column corresponding to the Processor State of the CPU.

NOTE: The Register Address, Data and Control signal conventions for communicating with the Extended Register File, Group III are provided in Section 3.2.4.

3.1.3 Register Option

The Register Option shall provide the means for enhancing the 7300 Processor by accomodating the following Selectable Register Features:

Relocation and Protection Feature
Basic Storage Protection Feature
Job Accounting Feature
Error Correction Code Feature (Register Set)

Each of these Selectable Register Features shall be supported within the Register Option through the implementation of a separate group of special purpose registers. However, the Relocation and Protection Feature and the Basic Storage Protection Feature shall be mutually exclusive.

As a result of the highly specialized and dynamic functional requirements on the part of all of these features, the operations within the Register Option shall occur primarily under hardware control. Micro-command access to the registers within the Register Option shall be effected only by means of special Main Storage reference cycles and shall be allowed for all Processor States.

a. The Relocation and Protection Feature shall consist of a Segment Tag File, a Segment Table, a Protection Matrix and an Address-Mode Register.

   The Segment Tag File shall consist of 259 4-bit Tag Registers corresponding to left-most extension to all 256 registers in the Basic Register File and the Parity Error (PE), Console Address (CA), and Console Data (CD) Registers in the Extended Register File, Group II. The Segment Tag File shall provide expansion of Main Storage Address capabilities from 65,536 bytes to 1,048,576 bytes.

   The Segment Table shall consist of 16 registers, each containing 32 bits of logical significance. Segment Table entries shall provide Main Storage Address relocation and Main Storage protection based on the partitioning of Main Storage into a maximum of 16 segments, (Each Main Storage Segment shall contain 256 bytes minimum and 65,536 bytes maximum).

The Access Protection Matrix shall consist of 16 16-bit registers and shall provide read and write protection for each Main Storage segment on a Processor State basis.

The Address-Mode Register shall be a 16-bit register and shall provide controls for both the relocation and protection mechanisms on a Processor State basis.

b. The Basic Storage Protection Feature shall consist of 3 16-bit registers referred to as "Bounds Registers". This option shall provide Main Storage Protection, in Pages of 256 bytes each, during Main Storage write operations on the part of Processor States 5, 6, and 7.

c. The Job Accounting Feature shall consist of 8 32-bit registers corresponding to Processor States 0 through 7. During each major cycle allocated to one of these Processor States, the contents of the associated 32-bit register shall be incremented by one.

d. Error Correction Code Feature (Register Set)

The Error Correction Code Feature shall be implemented within Main Storage and shall be described by the appropriate document listed in 2.1.

The Register Set, associated with ECC but accessed as a part of the Register Option shall provide 4 16-bit quantities relevant to the serviceability and availability aspects of Main Storage in the presence of the ECC Feature.

3.1.4 Arithmetic Logic Unit (ALU)

The Arithmetic Logic Unit shall consist of those registers and logical networks required for implementation of the Micro-command repertoire.

All quantities read from the Register File under Micro-command control shall use the ALU as the immediate destination. All quantities written into the Register File, under Micro-command control, (with the exception of the CSS Register), shall be generated by or transferred by way of the ALU.

In addition to its arithmetic and logical facilities, the ALU shall accomodate the registers and data paths required for the transmission of Main Storage Addresses and the transmission/reception of Main Storage Data, (Where registers within the Register Option are to be read or written under Micro-command control, the Main Storage related facilities within the ALU shall also be used).

Operations between the Register File and the ALU as well as operations internal to the ALU itself shall occur in 100 n/s or 200 n/s as determined by the nature of the operation to be performed. The fundamental execution time of 100 n/s shall be referred to as a "minor cycle". When operations requiring 200 n/s are performed, two minor cycles shall be used for execution.

The ALU shall contain the following Registers and Networks:

a. Au: 16-bit Feeder Register, Multiple-inputs.

b. Bu: 16-bit Feeder Register, Multiple-inputs.

c. Forced Carry: Single Bit Adder Feeder, right-most bit position.

d. Inner-Carry: 4-bit Group Carry Register providing correction parameters for decimal arithmetic performed in Excess – 3 notation.

e. S Register: 16-bit Main Storage Address Register, byte addressing format.

f. D Register: 16-bit Register providing data to Main Storage during word and byte write operations.

g. Shift Network: Left shifter, 32 bits wide, 0 to 15 bit positions per pass, end-off left-most, zeros in right-most, Au/Bu format.

h. Adder: 16-bit parallel, full add, four 4-bit Groups with inter-Group carries Micro-command conditioned for decimal arithmetic.

i. ALU Status: Overflow, Link, Au = Zero, Au = Bu, Au > Bu algebraic, Au > Bu logical, Au < Bu algebraic, Au < Bu logical.

j. Bit Sense: Au set or clear on bit position basis and Au set or clear, left to right scan including a Bu adder for scan result addition.

k. Constant Generator: Immediate operand generator, (including Processor State number).

l. ALU Fan-In: Multi-input, multi-format multiplexer providing data to the Register File during write operations, (includes Boolean functions for Au/Bu).

m. D Fan-In: Three-input, 16-bit parallel multiplexer providing the data path from Main Storage, the D Register, and the Register Option to Au and the ALU Fan-In.

See Figure 5 for a Block Diagram of the ALU.

3.1.5 Control Storage

The Control Storage facility shall be divided into two major areas referred to as "Control Storage proper" and the "Address Table".

a. Control Storage proper shall consist of a maximum of 16,384, 14-bit words, (These 14-bit words shall be treated as 16-bit quantities in which bit positions 09 and 10 shall be unused and always in the clear state).

Control Storage proper shall be addressed by means of an address register referred to as "Su".

When the contents of Control Storage proper are to be read, translated, and executed as Micro-commands, two 16-bit registers referred to as "Fu1" and "Fu2" shall buffer the output of Control Storage proper. Micro-commands shall be duplicated in Fu1 and Fu2 and horizontal parity checking shall be performed on the contents of Fu2. Within Fu2, an even number of bits in the set state shall constitute a Control Storage Parity Error with respect to Micro-command translation.

Control Storage proper shall be divided into a maximum of 4 groups of 4096 words each. Console State operations which shall be performed under Micro-command control as selected and initiated at the 7300 System Control Panel shall be confined to the first of these four groups. However, locations in Control Storage proper referred to as "RNI0", RNI1", "RNI2", "CS-PE", "MS-PE" and "Illegal Address" shall be defined within all 4 groups. For a definition of all hardware generated, address constants, see 3.5.

When the contents of Control Storage proper are to be read but not treated as Micro-commands, the Control Storage Scan (CSS) Register within the Extended Register File, Group II shall buffer the output of Control Storage proper. When such operations are performed for the purpose of hardware controlled checking, Control Storage proper shall be divided into a maximum of 64 pages of 256 words each. Within each 256 word page, longitudinal parity checking shall occur. Within each page an even number of bits in the set state in any of the 14 individual bit position columns shall constitute a Control Storage Parity Error with respect to hardware controlled checking.

b. The Address Table shall consist of a maximum of 1024, 10-bit words.

When the contents of the Address Table are to be read under Micro-command control, the Address Table shall be addressed by means of decoding the output of the D Fan-In Network of the ALU. The contents of the Address Table location thus referenced shall be checked for odd horizontal parity and in the absence of a parity error, the right-most 9 bits shall be buffered into a register referred to as "Pp".

After completion of the associated major cycle, the contents of the Pp Register shall be written into the appropriate Processor State's Pu Register. In this manner, the aforementioned Micro-command shall utilize the Address Table to perform a Decode Branch without affecting access to Control Storage proper on the part of any other Processor State.

When the contents of the Address Table are to be read under hardware control, the Address Table shall be addressed by means of the Su Register. When such operations are performed, the direct output of the Address Table shall be transmitted to the Console Data Register Display indicators on the 7300 System Control Panel and simultaneously checked for odd horizontal parity.

For a detailed description of these sequences, see 3.5.

For a Block Diagram of Control Storage, See Figure 6.

3.1.6 Main Storage

Main Storage facilities for the 7300 Processor shall be described by the appropriate document listed in 2.1.

In addition to the conventional Address, Data and Control signal requirements, the following general statements shall apply to the CPU/Main Storage relationship within the 7300 Processor.

a. Word (16-bit) and byte (8-bit) operations shall be supported, including the means for error checking (and error correction in the presence of the ECC Feature).

b. In the absence of the Relocation and Protection Feature, the CPU shall address a maximum of 65,536 bytes.

c. In the presence of the Relocation and Protection Feature, the CPU shall address a maximum of 1,048,576 bytes.

d. References to Main Storage Addresses not physically present in the Main Storage facility shall result in an "Out of Range" condition and shall cause the CPU to perform a hardware trap of the associated Processor State. See 3.5.2, item e.

e. The CPU shall provide allowances within the Resource Allocation Network for "Refresh" cycle requirements on the part of the Main Storage facility.

f. To minimize the impact of Refresh requirements on CPU operation, the Main Storage facility shall be capable of performing Refresh cycles independently of, and in parallel with, CPU major cycles whenever such major cycles do not involve Main Storage references on the part of the CPU.

3.1.7 Micro-Command Repertoire

The Micro-command Repertoire shall consist of 65 basic Micro-commands catagorized into the following functional classes.

Register File Read
Register File Write
Register File Read, Main Storage Related
Register File Write, Main Storage Related
Immediate Operand
Shift
Sense
Skip
Branch
Control

a. The Register File Read class shall provide 7 basic Micro-commands including data transfers in both the true and 1's complement states. (Forced Carry Register manipulation shall be used in order to effect 2's complement operations). These Micro-commands shall each require 1 minor cycle for execution.

b. The Register File Write class shall provide 10 basic Micro-commands including direct data transfer, status transfer, Boolean and additive operations. These micro-commands shall each require 1 minor cycle for execution except for those cases of additive and comparative operations in which Adder and Comparator propagations, respectively, have not over-lapped the execution of a previous Micro-command(s) and 2 minor cycles for execution shall be provided under hardware control.

c. The Register File Read, Main Storage Related class shall provide 11 basic Micro-commands, each requiring one minor cycle for execution provided they occur on the proper minor cycles within a major cycle. Additional minor cycles shall be allowed under hardware control so as to result in proper execution when such Micro-commands are translated during minor cycles having an improper timing relationship with Main Storage operations.

d. The Register File Write, Main Storage Related class shall provide 2 basic Micro-commands, each requiring a minimum of 1 minor cycle for execution with the same hardware controls for timing adjustments as previously described for the Register File Read, Main Storage Related class.

e. The Immediate Operand class shall provide 6 basic Micro-commands including immediate operands in byte, nybl and bit formats. These Micro-commands shall each require 1 minor cycle for execution.

f. The Shift class shall provide 4 basic Micro-commands involving the use of Au/Bu and the Shift Network. These Micro-commands shall each require 2 minor cycles for execution.

g. The Sense class shall provide 4 basic Micro-commands involving the use of Au/Bu, the Au Sense Network and the Bu adder. These Micro-commands shall each require 2 minor cycles for execution.

h. The Skip class shall provide 8 basic Micro-commands including zero, non-zero, and bit sensing in Au as well as logical comparisons between Au and Bu. These Micro-commands shall each require 1 minor cycle for execution when a skip is not performed and 2 minor cycles for execution when a skip is performed.

i. The Branch class shall provide 6 basic Micro-commands including Function Decode, Format Decode, Address Constant and Partial Address branch capabilities. Except for the Format Decode and Address constant branches, these Micro-commands shall require 1 minor cycle when executed during the last minor cycle of a major cycle and 2 minor cycles if executed at any other time in the major cycle. The Format Decode (Address Table) and Address Constant (RNI area) branches shall require the remainder of the major cycle in which they are read for execution, (1 to 8 minor cycles).

j. The Control class shall provide 7 basic Micro-commands of varying complexity and execution times. The Micro-commands within this class shall provide the means for Timing, Input/Output Termination and Boundary Crossing Mode Micro-command control.

3.1.8 Resource Allocation

Processor State determination shall be performed on a major cycle basis by means of a Resource Allocation Network. Thus, utilization of shared resources on the part of dedicated resources within the 7300 Processor shall be based on the inputs to,and subsequent outputs from this Resource Allocation Network for each major cycle interval.

Without considering priorities, the Resource Allocation Network receives resource requests (and allocates resource utilization equally for these requests) from the following areas:

Main Storage: Refresh

Processor State 0: Busy Flip/Flop, Bit 00 of B/A Register
Processor State 1: Busy Flip/Flop, Bit 01 of B/A Register
Processor State 2: Busy Flip/Flop, Bit 02 of B/A Register
Processor State 3: Busy Flip/Flop, Bit 03 of B/A Register
Processor State 4: Busy Flip/Flop, Bit 04 of B/A Register
Processor State 5: Busy Flip/Flop, Bit 05 of B/A Register
Processor State 6: Busy Flip/Flop, Bit 06 of B/A Register
Processor State 7: Busy Flip/Flop, Bit 07 of B/A Register

Console State: Console Request Flip/Flop

Note: The B/A Register referred to as containing the Busy Flip/Flops for Processor States 0 through 7 shall be a special purpose, common resource register within the Extended Register File, Group II as previously designated in 3.1.2.

Each Main Storage Refresh request shall have unconditional priority over all other resource requests and shall result in a major cycle Null State, 800 n/s in duration. This Null State shall also result from the absence of all resource requests as listed above.

Priority allowances shall be made within the Resource Allocation Network for Processor States 0, 1, 2, and 3 only, with priority occurring in that order. Thus in priority mode, any two Processor states within this group shall be capable of obtaining equal utilization of the shared resources to the exclusion of all other Processor States (except Main Storage Refresh requests).

The ability of a Processor State to utilize consecutive major cycles shall effect resource utilization when simultaneously operating in priority mode. Thus Processor States 0, 1, 2, and 3 shall have the capability of obtaining exclusive utilization of the shared resources (except for Main Storage Refresh operations).

3.1.9 System Control Panel (Console)

The 7300 System Control Panel shall provide the means for manually monitoring and controlling operations within the 7300 Processor. The switches and indicators on the System Control Panel shall be effective only in conjunction with associated hardware and Micro-command sequences within the 7300 Processor.

The 7300 System Control Panel shall be divided into 4 funtional areas as follows:

Operator Group
Programmer Group
Maintenance Group
Communications Activity Display Group

Indicators within each of these groups shall be active at all times. Likewise the controls contained within the Operator Group shall be enabled at all times. However, controls within Programmer Group shall be enabled only when the System Control Panel is in Program or Maintenance Mode and controls within the Maintenance Group shall be enabled only when the System Control Panel is in Maintenance Mode.

a. The Operator Group shall provide the means for applying and removing power to the Processor, selecting and initializing Reset/Load and Auto-load sequences, disabling the Console Alarm, adjusting the Console Speaker Volume and clearing Processor and I/O Fault indications. In addition, Lamp and Alarm tests may be performed by means of a control within the Operator Group.

b. The Programmer Group shall provide the means for controlling and monitoring Processor State activities within the 7300 Processor.

c. The Maintenance Group, in conjunction with the Program Group, shall provide the means for controlling and monitoring fault isolation procedures and operations within the 7300 Processor.

d. The Communications Activity Display Group shall provide the means for monitoring the activities performed by the Communications Channels within the 7300 Processor.

Throughout the remainder of this specification, the System Control Panel shall be referred to as the Console, for the sake of brevity.

3.1.10 Implementation

The 7300 Processor shall utilize Transistor-Transistor Logic (TTL), and both bipolar and metal-oxide-semiconductors memories. Except for MOS Main Storage, all semiconductors in the machine shall be silicon devices. Small (SSI), medium (MSI) and large (LSI) scale integration shall be used.

The design of the machine shall utilize conservative worst case design rules and modular construction to enhance reliability, availability, and serviceability.

3.2 Register File

The addressing mechanism for the Register File shall have the potential for directly addressing 512_{10} registers. However, the implementation of the addressing mechanism shall confine the 7300 Processor to addressability of 346 unique registers within the Register File. Despite the restriction of Extended Register File, Group III addressability to only the associated Processor States 0 through 3, all registers within the Register File shall be numerically designated in hexadecimal notation conforming to "Boundary Crossing Mode" format.

00 06	07	08 09 10	11 12 13 14 15
NOT USED	E	STATE	REGISTER

Bits 00 through 06 shall not be used but shall be referred to as being in the clear state for the purpose of 16-bit hexadecimal notation.

Bit 07 in the clear state shall specify the Basic Register File and in the set state shall specify the Extended Register File.

Bits 08, 09 and 10 shall specify the Processor State number when applicable.

Bits 11, 12, 13, 14 and 15 shall specify the Register number within the Basic or Extended Group as specified by Bit 07 and for the appropriate Processor State as specified by bits 08, 09 and 10 where applicable.

The storage facilities within the Register File shall be volatile in nature, i.e. the contents of the Register File shall be lost when power is removed. Moreover, the contents of the Register File shall be unpredictable and undefined after power is applied except for those registers affected by the System Reset associated with the Power-on sequence. With the exception of the Extended Register File, Group III, the effects of System Reset on the Register File are described in 3.10.3.8. For the effects of System Reset on the Extended Register File, Group III, see the appropriate document listed in 2.1.

Where Register File characteristics are associated with only particular Micro-commands, these Micro-commands shall be referenced by mnemonics. Each mnemonic is associated with an individual Micro-command as described in 3.8.3 through 3.8.12.

3.2.1 Basic Register File

The Basic Register File shall consist of 256 16-bit registers, 32 registers each for Processor States 0 through 7, using the following hexadecimal notation, inclusively:

Processor State	Register Numbers
0	0000 → 001F
1	0020 → 003F
2	0040 → 005F
3	0060 → 007F
4	0080 → 009F
5	00A0 → 00BF
6	00C0 → 00DF
7	00E0 → 00FF

The registers within this group represent general purpose registers under Micro-command control only, dedicated to the appropriate Processor States as shown.

For the purpose of recording status conditions under Micro-command control (CMP, CMU, RNI1 and RNI2 Micro-commands) the left-most 8-bits of any register in the Basic Register File may be written without affecting its right-most 8-bits.

System Reset shall not affect the registers within the Basic Register File.

For each Processor State, Registers 1E and 1F within the Basic Register File shall be special to the extent that their direct Micro-command use in addressing Main Storage (LS1, LS2, LSE, LSF) shall result in hardware operations during the associated major cycle such that registers within the Register Option shall be referenced in lieu of Main Storage

3.2.2 Extended Register File, Group I

The Extended Register File Group I shall consist of 16 18-bit registers, 2 registers each for Processor States 0 through 7. These registers shall be designated as F and Pu for Processor States 0 through 7 using the following hexadecimal notation:

Processor State	F Register	Pu Register
0	0100	0101
1	0120	0121
2	0140	0141
3	0160	0161
4	0180	0181
5	01A0	01A1
6	01C0	01C1
7	01E0	01E1

3.2.2.1 F Register

The left-most 2 bits of each of these 18-bit Registers shall be unused.

a. The contents of the appropriate F Register shall be read in advance of the major cycles allocated to Processor States 0 through 7 by means of a hardware controlled minor cycle referred to as R1, (When one of these Processor States utilizes consecutive major cycles, the R1 operation shall not be performed).

b. Once read, the contents of the appropriate F Register shall be held throughout each major cycle in a common resource register, also referred to as F, in the Timing/ Control section of the 7300 Processor. Thus the contents of the appropriate F Register within the Extended Register File, Group I shall be immediately available for Micro-command modification during each of the minimum 8 minor cycles comprising a major cycle (referred to as E0 through E7). The contents of the common resource F Register shall be capable, under Micro-command control, of direct participation in the formation of register numbers, shift counts, branch addresses, and bit position values as described in 3.8.1. In addition, the contents of the common resource F Register shall be capable of modifying the bit position within the adder from which the Link status bit is derived as described in 3.4.7.2.

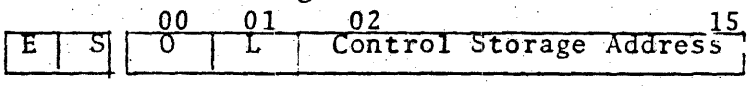
Micro-commands which address the F Register in Normal Mode, (Not Boundary Crossing Mode) shall utilize the common resource F Register. Any such Micro-commands performed for the purpose of writing the F Register, (such as CLR, RNI1, and RNI2), should not be performed during the first minor cycle, E0, of a major cycle since such operations may lead to machine malfunctions in the course of executing hardware controlled multi-state sequencing.

Micro-commands which address the F Register in Boundary Crossing Mode shall utilize the appropriate F Register within the Extended Register File, Group I, provided such Micro-commands are executed during minor cycles E3 or E4. Any such Micro-commands executed in minor cycles other than E3 or E4 shall not be hardware supported and may lead to invalid results.

c. For those major cycles in which Micro-command execution involves the writing of the common resource F Register, the contents of the associated Extended Register File, Group I, F Register shall be appropriately updated after the completion of such major cycles allocated to Processor States 0 through 7. This operation shall be performed by means of a hardware controlled minor cycle referred to as W1.

3.2.2.2 Pu Register

Each of the 8 Pu Registers shall be formatted as follows:



The left-most 2 bits shall be hardware controlled status bits relating to Control Storage Parity Error and Skip conditions, designated E and S, respectively. These bits shall be inaccessible for Micro-command Control purposes except in the case of Micro-commands which address Pu for the purpose of performing write references in Boundary Crossing Mode. Such Micro-commands shall clear both of these status bits.

Bit positions 00 and 01 shall provide Overflow and Link status, respectively, and are arithmetically defined in 3.4.7.

Bit positions 02 through 15 shall provide a Control Storage Address for Control Storage proper only.

a. The contents of the appropriate Pu Register shall be read in advance of the major cycles allocated to Processor States 0 through 7 by means of a hardware controlled minor cycle referred to as R0. (When one of these Processor States utilizes consecutive major cycles, the R0 operation shall be effective during minor cycle E8 and shall use the contents of the Pp Register in lieu of Pu, provided the previous major cycle did not involve the execution of a CI01 or CI02 Micro-command which resulted in the suppression of Pp).

b. Once read, the contents of the appropriate Pu Register shall be held throughout each major cycle in a common resource register referred to as Su, the Control Storage Address Register. Thus, the contents of the appropriate Pu Register within the Extended Register File, Group I shall be immediately available for addressing Control Storage proper and supplying/recording arithmetic status during each of the minor cycles comprising a major cycle.

The Control Storage Address portion of Su, Bits 02 through 15, shall be incremented by one under hardware control whenever execution of successive Micro-commands is required as a result of in-line Micro-code. Likewise, only these bits within Su shall be capable of alteration for the accomplishment of branch operations under Micro-command control whether for explicit functions limited to FNJ, FRJ, FZJ, JMP, RNI1 and RNI2 or for implicit functions limited to CLR, STA, STB, and AND providing the Pu Register is addressed in Normal Mode, (Not Boundary Crossing Mode).

The Arithmetic Status portion of Su, Bits 00 and 01, shall reflect Overflow and Link conditions relative to the execution of each DSUM Micro-command. The Overflow and Link status bits shall also be clocked by each SUM Micro-command provided the left-most byte of the common resource F Register is not equal to 50, 51, 52, or 53 in hexadecimal notation. (The clocking of current arithmetic status shall also be conditioned by the DIG and CORC Micro-commands as described in 3.8.7).

Micro-commands which address Pu in normal Mode for the purpose of performing a read reference shall obtain the Address portion of Pu from the common resource Pp Register (the last Blockpoint Address) and the Arithmetic Status portion of Pu from the Su Register.

Micro-commands which address the Pu Register in Boundary Crossing Mode shall utilize the appropriate Pu Register within the Extended Register File, Group I, provided such Micro-commands are executed during minor cycles E3 or E4. Any such Micro-commands executed in minor cycles other than E3 or E4 shall not be hardware supported and may lead to invalid results. (When any Processor State references its own Pu Register in Boundary Crossing Mode for the purpose of performing a write reference, the effectiveness of the operation shall be conditioned by the "Housekeeping" function described in item c.

c. The contents of the associated Extended Register File, Group I Pu Register shall be appropriately updated after the completion of each major cycle allocated to Processor States 0 through 7 by means of a hardware controlled minor cycle referred to as WO. (The WO operation shall not be performed after major cycles involving the execution of a CI01 or CI02 Micro-command which resulted in the suppression of Pp).

Micro-commands which address the Extended Register File, Group I, F and Pu Registers shall be limited to CLR, STA, STB and AND when performed in Boundary Crossing Mode.

3.2.3 Extended Register File, Group II.

The Extended Register File, Group II shall consist of 10 16-bit registers representing common resource facilities for the Console State as well as Processor States 0 through 7. The State number portion of the Boundary Crossing Mode address format shall not be applicable for these registers since any combination of these 3 bits shall be allowed. However, for the sake of simplicity these bits are treated as being in the clear state for the purpose of providing the following numerical designations in hexadecimal notation.

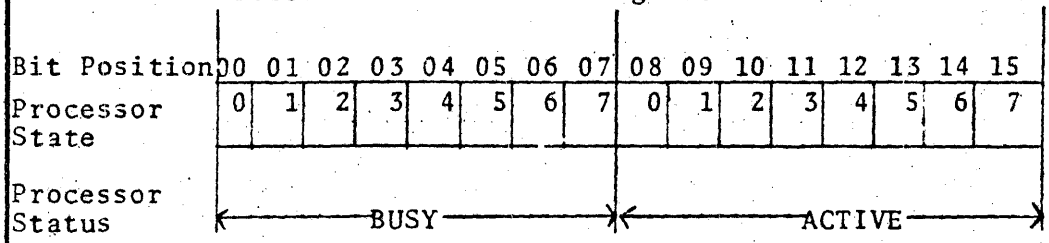
Register Name	Register Number
Busy Active (B/A)	0102
Real Time Clock (RTC)	0103
Tie-Breaker (T)	0104
Parity Error (PE)	0105
Control (C)	0106
Privileged Mode (PM)	0107
Boundary Crossing (BC)	0108
Control Storage Scan (CSS)	0109
Console Address (CA)	010A
Console Data (CD)	010B

NOTE: The Busy/Active (B/A) Register shall also be addressed by numbers 0122, 0142, 0162, 0182, 01A2, 01C2 and 01E2. The equivalent addressing anomaly shall also exist for the remaining 9 registers within this group.

Read references to the ALU under Micro-command control shall be provided for all the registers within this group. Write references from the ALU under Micro-command control shall be provided for all the registers within this group except the Parity Error (PE), Real Time Clock (RTC), and Control Storage Scan (CSS) Registers.

3.2.3.1 Busy/Active Register (B/A)

This 16-bit register referred to as B/A shall provide Busy and Active status indications for each of the Processor States 0 through 7.



a. The set outputs from the bit position in the left-most byte of the B/A Register (Busy Flip/Flops) shall provide inputs to the Resource Allocation Network in the form of resource requests on the part of Processor States 0 through 7.

The Busy Flip/Flop for Processor State 4 shall be conditioned at the input to the Resource Allocation Network by a disable associated with Breakpoint stop as described in 3.10.3.18.

The set outputs of the 16 bit positions of the B/A Register shall be available for selection as inputs to the Console Data Register Display indicators as described in 3.10.3.7.

b. The inputs from the ALU to the bit positions in the left-most byte of the B/A Register shall not be hardware conditioned for Processor States 5, 6, and 7 but shall be conditioned on a bit-by-bit basis by the state of the bits in the right-most byte of the B/A Register (Active Flip/Flops) in the following manner for Processor States 0 through 4:

For Processor States 0 and 4 the appropriate Busy Flip/Flop shall not change from the set to the clear state under Micro-command control during any minor cycle in which the associated Active Flip/Flop is in the set state.

For Processor States 1, 2, and 3 the appropriate Busy Flip/Flop shall not change from the clear to the set state under Micro-command control during any minor cycle in which the associated Active Flip/Flop is in the set state.

c. The Busy Flip/Flop for Processor State 4 shall be provided with a set input for each increment of the Real Time Clock (RTC) Register as described in 3.2.3.2.

Each of the Busy Flip/Flops for Processor States 0 through 7 shall be provided with set inputs which shall be appropriately Console switch controlled as described in 3.10.3.19 and 3.10.3.20.

Each of the Busy Flip/Flops for Processor States 0 through 3 shall be provided with set inputs which shall be enabled by the appropriate Request signal supplied by Extended Register File, Group III controls as described in 3.2.4.9, conditioned by the corresponding Processor Control Select switch as described in 3.10.3.18 and disabled during minor cycles E6/E7 and E8/E9 associated with Consecutive Cycle operations.

Each of the Busy Flip/Flops for Processor States 1, 2 and 3 shall be provided with set inputs which shall be enabled by the appropriate Attention signal supplied by Extended Register File, Group III controls as described in 3.2.4.10, enabled by the cleared state of the appropriate Active Flip/Flop, conditioned by the Processor Control Select switches described in 3.10.3.18, and disabled during minor cycles E6, E7, E8 and E9.

d. Each of the Busy Flip/Flops for Processor States 5, 6 and 7 shall be provided with clear inputs which shall be enabled at the beginning of minor cycle E4 by the clear state of the appropriate Active Flip/Flop. These clear inputs shall clear the appropriate Busy Flip/Flop provided Micro-command execution begins at Control Store Address $X00X_{16}$ for the major cycle allocated to the associated Processor State. This clear input shall also clear the appropriate Busy Flip/Flop when Cycle Step operation is selected by means of the Console control described in 3.10.4.27.

Each of the Busy Flip/Flops for Processor States 0 through 4 shall be provided with clear inputs for Stop/Step operations which shall be Console switch controlled as described in 3.10.3.18 and 3.10.4.27.

Each of the Busy Flip/Flops for Processor States 0 through 7 shall be provided with clear inputs for Breakpoint operations which shall be Console switch controlled as described in 3.10.3.15 through 3.10.3.18.

Each of the Busy Flip/Flops for Processor States 0 and 4 shall be provided with clear inputs which shall be enabled by the clear state of the appropriate Active Flip/Flop when the execution of CI01 and CI02 Micro-commands on the part of the associated Processor State results in the suppression of the Pp Register as described in 3.8.12.5.

Each of the Busy Flip/Flops for Processor States 1, 2, and 3 shall be provided with clear inputs which shall be enabled when the execution of CI01 and CI02 Micro-commands on the part of the associated Processor State results in the suppression of the Pp Register as described in 3.8.12.5.

e. The inputs from the ALU to the bit position in the right-most byte of the B/A Register (Active Flip/Flops) shall be under Micro-command control only.

Bit positions 13, 14 and 15 of the B/A Register, corresponding to Processor States 5, 6, and 7 Active Flip/Flops, shall be provided with set and clear inputs for Processor Run and Step/Stop operations which shall be Console switch controlled as described in 3.10.3.18 through 3.10.3.20.

3.2.3.2 Real Time Clock (RTC)

The contents of this register shall be incremented by one under hardware control every 1.6384 m/s. Each increment operation shall be synchronous to the extent that it shall occur only during minor cycle E7.

The contents of this register may be read but not written under Micro-command control. Attempts to write this register by means of Micro-command control shall result in no operation, (other than the clocking of the Pp Register for Blockpoint purposes). Upon completion of the power-on sequence the contents of this register shall begin incrementing from an unpredictable initial count, not affected by System Reset.

For every tenth increment operation performed on the contents of the RTC Register a set input shall be provided to the Busy Flip/Flop for Processor State 4. This set input shall be conditioned by the Console Executive Disable control described in 3.10.4.26 and the sequence described in 3.10.2.4 relative to Autoload and System Reset.

The set outputs of the 16 bit positions of the RTC Register shall be available for selection as inputs to the Console Data Register Display indicators as described in 3.10.3.7.

3.2.3.3 Tie-Breaker (T)

This 16-bit common resource register contained within the Extended Register File, Group II shall be under Micro-command control only.

3.2.3.4 Parity Error (PE)

The contents of this 16-bit register shall be under Micro-command control for read but not write references.

Attempts to write this register under Micro-command control shall result in no operation (other than the clocking of the Pp Register for Blockpoint purposes).

Hardware control of this register shall be such that, in the event of detected addressing or data errors associated with Main Storage references, the contents of this register shall provide the Physical Main Storage address of the last such error to occur.

The input to this 16-bit register shall consist of a Main Storage Address only. This register shall be clocked under hardware control when each of the conditions described by items a through c have been satisfied and any one or more of the conditions described by items d through f have been simultaneously met.

a. Minor cycle E7 of any major cycle in which a Main Storage reference is performed, and

b. The state of the Console control described in 3.10.4.16 is such that Storage Parity is not disabled, and

c. The address to which the Main Storage reference is performed is not "Out of Bounds" as determined by either the Basic Storage Protection Feature or the Relocation and Protection Feature, and

d. The address to which the Main Storage reference is performed is not physically present in the System, (Out of Range), or

e. The Main Storage reference cycle is a read operation in the absence of the ECC Feature, and invalid parity is detected in either the left-most or right-most data byte, or

f. The Main Storage reference cycle is a read operation in the presence of the ECC Feature, and an uncorrectable error is detected in either the left-most or right-most data byte.

The set outputs of the 16-bit positions of the PE Register shall be available for selection as inputs to the Console Address Register Display indicators as described in 3.10.3.4.

NOTE: The address clocked into the PE Register shall always be a Physical Main Storage Address regardless of the absence or presence of the Relocation and Protection Feature and regardless of the Console controls described in 3.10.3.12 and 3.10.3.14. However, in the presence of the Relocation and Protection Feature, the PE Segment Tag Register within the Register Option shall contain the left-most 4-bits required to completely define the 20-bit Physical Main Storage Address at which the error occurred as previously defined in items a through f.

3.2.3.5 Control (C)

This 16-bit register shall provide the controls for conditioning Priority Modes for Processor States 0 through 3 and enabling Consecutive Cycle Modes for Processor States 0 through 7.

Bit Position	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
Processor State	0	1	2	3	0	1	2	3	0	1	2	3	4	5	6	7
Control	ENABLE PRIORITY				INVOKE PRIORITY				CONSECUTIVE CYCLE ENABLE							

The contents of this register shall be under Micro-command control for the purpose of performing read and write operations from the ALU.

In addition, the set outputs of the 16-bit positions of this register shall be interpreted by the Timing/Control section of the CPU for the purpose of providing Priority and Consecutive Cycle Modes of operation for the associated Processor States.

a. The Invoke Priority outputs of the C Register shall be conditioned at the input to the Resource Allocation Network by the appropriate set state outputs of the B/A Register. Processor States for which these signals are coincident after resynchronization shall have the potential for disproportionately greater use of the common resources. See 3.9.

b. The Enable Priority outputs of the C Register shall be conditioned at the input to the Resource Allocation Network by the appropriate set state outputs of the B/A Register and the appropriate Priority signals supplied by the Extended Register File, Group III controls as described in 3.2.4.11. Processor States for which these signals are coincident after resynchronization shall have the potential for disproportionately greater use of the common resources. See 3.9.

c. At the beginning of each major cycle allocated to Processor States 0 through 7, the appropriate Consecutive Cycle Enable shall be taken from the C Register set state output and stored in a single common resource Flip/Flop in the Timing/Control section. This Consecutive Cycle Enable Flip/Flop shall be used in its set state to provide hardware control such that the Resource Allocation Network shall be capable of scheduling the next successive major cycle for the same Processor State as the current major cycle.

Without respect to Priority Mode, the Consecutive Cycle Enable shall provide the means for one of the Processor States 0 through 7 to utilize consecutive major cycles in the absence of resource utilization requests on the part of all other Processor States.

With respect to Priority Mode, the Consecutive Cycle Enable shall provide the means for one of the Processor States 0 through 3 to utilize consecutive major cycles in spite of the presence of resource utilization requests on the part of Processor States 4 through 7 or any other Processor State 0 through 3 of lower priority.

See 3.9 for a further description of Priority Mode, Consecutive Cycle Mode and their inter-dependencies.

3.2.3.6 Privileged Mode (PM)

This 16-bit common resource register contained within the Extended Register File, Group II shall be under Micro-command control only.

3.2.3.7 Boundary Crossing (BC)

This 16-bit register shall be under Micro-command control for read and write references from the ALU.

The set state outputs from the 9 right-most bit positions shall be interpreted under hardware control during the execution of Micro-commands in Boundary Crossing Mode. The general format for the BC Register is described in 3.2.

The set outputs of the 16 bit positions of the BC Register shall be available for selection as inputs to the Console Data Register Display indicators as described in 3.10.3.7.

During the execution of Micro-commands performed in Boundary Crossing Mode, the contents of the BC Register shall participate as follows:

a. The Basic Register File shall be addressed for the Processor State designated by the BC Register, (Bits 08 through 10), at the register number resulting from the "inclusive or" of the BC designated register and the Micro-command designated register, (Bits 11 through 15), provided both the BC Register, (Bit 07 clear), and the associated Micro-command, (Bits 06 and 07 clear) designate the Basic Register File.

b. The Extended Register File, Group I shall be addressed during minor cycles E3 and E4 at the address designated by the contents of the BC Register, (Bit 07 shall be set and bits 11 through 14 shall be clear within the BC Register to effect the selection of a register within this group, Bits 08 through 10 designating Processor State.

c. The Extended Register File, Group II shall be addressed, independently of Processor State designators, at the register number resulting from the "inclusive or" of the BC designated register and the Micro-command designated register, (Bits 12 through 15), provided the BC Register specifies the Extended Register File, (Bit 07 set), and both the BC Register and the Micro-command designators, (Bit 11 clear), specify Group II. When unassigned registers within this group (C, D, E, and F) are referenced for read operations, zeroes shall be supplied. No operation shall occur when unassigned registers within this group are referenced for write operations.

d. The Extended Register File, Group III shall be addressed for the Processor State, 0 through 3, performing the operation at the register number resulting from the "inclusive or" of the BC designated register and the Micro-command designated register, (Bits 12 through 15), provided the Micro-command designators specify this Group, (Bit 06, 07, and 11 set). The BC Register does not participate for this operation in bit positions 07 through 11 and the term "Boundary Crossing Mode" becomes somewhat of a misnomer.

Boundary Crossing operations not described in items a through d shall be undefined. Moreover, write references which address the BC Register in Boundary Crossing Mode shall not be hardware supported and may result in machine malfunction.

3.2.3.8 Control Storage Scan (CSS)

The contents of this 16-bit register shall be under Micro-command control for read and write operations. However, all Micro-commands, with the exception of ROM, which address the CSS Register for the purpose of performing write operations shall result in clearing it. The ROM Micro-command shall clock the output from Control Store proper into the CSS Register in a J-K fashion, i.e. for each bit position having a set data input the clock shall cause the associated Flip/Flop to assume the set state when previously clear or the clear state when previously set; for each Flip/Flop having a clear data input the clock shall have no effect on the state of the associated Flip/Flop. The data inputs to the CSS Register in the bit 09 and 10 positions shall be confined by hardware means to the clear state.

The CSS Register shall be hardware controlled for clearing and clocking purposes during Control Storage Read Operations performed by means of the Console controls as described in 3.10.3.11. Moreover, the set outputs of the CSS Register in all bit positions except 09 and 10 shall be hardware translated for the purpose of detecting invalid longitudinal parity as required by Console initiated operations described in 3.10.3.11.

The set outputs of the 16 bit positions of the CSS Register shall be available for selection as inputs to the Console Data Register Display indicators as described in 3.10.3.7.

3.2.3.9 Console Address (CA)

This 16-bit register shall be under Micro-program control for the purpose of performing read and write operations from the ALU.

Each of the 16 bit positions of the CA Register shall be provided with a set input under Console control as described in 3.10.3.2.

Each of the 16 bit positions of the CA Register shall be provided with a clear input under a single Console control as described in 3.10.3.3.

The set outputs of the 16 bit positions of the CA Register shall be available for selection as inputs to the Console Address Register Display indicators as described in 3.10.3.4.

NOTE: When the CA Register is used under Micro-command control in conjunction with the set and clear inputs available to the Console controls, allowances for switch contact bounce must be made in or by means of the Micro-command timing sequences as required.

3.2.3.10 Console Data (CD)

This 16-bit register shall be under Micro-program control for the purpose of performing read and write operations from the ALU.

Each of the 16 bit positions of the CD Register shall be provided with a set input under Console control as described in 3.10.3.5.

Each of the 16 bit positions of the CD Register shall be provided with a clear input under a single Console control as described in 3.10.3.6.

The set outputs of the 16 bit positions of the CD Register shall be available for selection as inputs to the Console Data Register Display indicators as described in 3.10.3.7.

NOTE: When the CD Register is used under Micro-command control in conjunction with the set and clear inputs available to the Console controls, allowances for switch contact bounce must be made in or by means of the Micro-command timing sequences as required.

3.2.4 Extended Register File, Group III

The registers which make up this group are architecturally a part of the Register File but physically a part of the Integrated Disk Adapter, Communications Adapter and I/O Channels within the 7300 Processor. The special purpose, dedicated registers within this Group shall provide varied Micro-command and hardware controlled functions as described by the appropriate documents listed in 2.1.

The common resources within the CPU shall provide the address, data and control signal allowances required for implementation of the Extended Register File, Group III as described herein. All signals for which the designated abbreviations are preceded by a plus (+) sign shall be active per the associated descriptions when in the logical 1 (high) state. All signals for which the designated abbreviations are preceded by a minus (-) sign shall be active per the associated descriptions when in the logical 0 (low) state.

All signals originating within the CPU for the purpose of providing register address, data and control information to the Extended Register File, Group III, shall be capable of fanout to ten unit loads of the TTL1 Family as described by the appropriate documents listed in 2.2. Moreover, with the exception of the Execute signals described in 3.2.4.1, this output facility from the CPU shall consist of a single set of signals to be shared by the 4 Processor States, 0 through 3, such that no more than two unit loads of the TTL1 Family shall be required by any one Processor State for any one CPU output signal.

All signals received by the CPU for the purpose of obtaining data and control information from the Extended Register File, Group III, shall not be required, on the part of the CPU, to provide fanout capabilities in excess of two unit loads of the TTL1 Family. All such data and control signals shall be independently generated by each of the four Processor States, 0 through 3, and shall be individually received and selected within the CPU on a Processor State basis.

3.2.4.1 Execute

These 4 control signals from the CPU shall be abbreviated +EXCT-0 through +EXCT-3 and shall individually correspond to Processor States 0 through 3.

These signals shall provide the means for conditioning the interpretation of the remaining output signals from the CPU (with the exception of the System Reset I/O signal described in 3.2.4.6), which shall be shared by Processor States 0 through 3 in accomplishing the implementation of the Extended Register File, Group III facilities.

The appropriate Execute signal shall be active during each major cycle allocated to Processor States 0 through 3 except during minor cycles E8 and E9 associated with Consecutive Cycle operations.
For timing relationships, see Figure 7.

3.2.4.2 Extended Register Number

These 4 register address signals from the CPU shall be abbreviated +ERNG3-00 through +ERNG3-03 and shall represent a register number for which +ERNG3-00 shall be the left-most bit and +ERNG3-03 shall be the right-most bit.

These signals shall be shared by Processor States 0 through 3 and shall provide the means for specifying a register number (1 of 16) as designated under Format 1 Micro-command control according to the descriptions in 3.2.3.7, item d, and 3.8.1.1, item c, for Boundary Crossing and Normal Modes respectively. The +ERNG3-00 through +ERNG3-03 signals, shall correspond to bit positions 12 through 15, respectively, of the Micro-command and BC Register formats.

For timing relationships, see Figure 7.

3.2.4.3 Extended Register Out

These 16 data signals from the CPU shall be abbreviated +ERO-00 through +ERO-15 and shall represent the data output from the ALU Fan-in Network for which +ERO-00 shall be the left-most bit and +ERO-15 shall be the right-most bit.

These signals shall be shared by Processor States 0 through 3 and shall provide the means for transferring data from the ALU to the Extended Register File, Group III under Format 1 Micro-command control.

For timing relationships, see Figure 7.

3.2.4.4 Extended Register Write

This single control signal from the CPU shall be abbreviated +ERFG3WR and shall indicate the execution of each Format 1 Micro-command designating the Extended Register File, Group III, for the purpose of performing a write reference.

This write control signal shall be shared by Processor States 0 through 3 and shall be active during all minor cycles in which an AND, CLR, EOR, IOR, SDB, SDW, STA or STB Micro-command is executed for which the Extended Register File is designated according to 3.2.3.7, item d and 3.8.1.1, item c, for Boundary Crossing and Normal Modes, respectively. However, in the case of SDB and SDW Micro-commands, translated to minor cycle E5 during major cycles in which Main Storage or Register Option read references are performed, this signal shall not assume the active state until minor cycle E5.

For timing relationships, see Figure 7.

3.2.4.5 Clocks

These five control signals from the CPU shall be abbreviated +CLOCK-00, +CLOCK-20, +CLOCK-40, +CLOCK-60 and +CLOCK-80 and shall provide the means for establishing five unique phase times during every minor cycle.

These five timing control signals shall be shared by Processor States 0 through 3 and shall have their active state leading edges separated by intervals equal to 20% of the duration of the minor cycle as designated by their aforementioned abbreviations. Thus, the leading edge of +CLOCK-00 shall occur at the beginning of each minor cycle, +CLOCK-20 shall occur after 20% of each minor cycle has expired, +CLOCK-40 shall occur after 40% of each minor cycle has expired, etc. After the leading edge, each clock signal shall remain active for an interval equal to 30% of the minor cycle duration, subject to variations of ±5% of the minor cycle duration.

3.2.4.6 System Reset I/O

This single control signal from the CPU shall be abbreviated +SR-IO and shall provide the means for establishing initial operating states for control and data mechanisms as required within the Extended Register File, Group III facilities.

This control line shall assume the active state until the completion of each power-on sequence, during the initialization of each Reset/Load sequence provided the Console is not in Maintenance Mode, during the initialization of each Auto-load sequence and during the depression of the Console System Reset switch as described in 3.10.3.8. The Extended Register Out signals described in 3.2.4.3 shall be inactive for a minimum of 300 n/s prior to the active state of the System Reset I/O signal and shall remain inactive for a minimum of 300 n/s after the System Reset I/O signal has changed from the active to the inactive state. Once active, the System Reset I/O signal shall remain active for a minimum of 2 u/s.

All output signals from the CPU shall be inactive during the occurrence of the System Reset I/O with the exception of the Clock signals described in 3.2.4.5.

3.2.4.7 Extended Register In

These 64 data signals to the CPU shall be divided into 4 sets of 16 parallel signals each, with each set corresponding to one of the Processor States 0 through 3. The set associated with Processor State 0 shall be abbreviated +ERI0-00 through +ERI0-15. The remaining 3 sets shall be similarly abbreviated such that the first numeric shall correspond to the Processor State (through 3) and the second and third numerics shall correspond to the bit position (00, left-most through 15, right-most) within each set. These input signals shall provide the means for performing data transfers from the Extended Register File, Group III to the ALU under Format 1 Micro-command control.

During all major cycles allocated to Processor States 0 through 3, the appropriate set of 16 signals shall be selected from these 64 input data signals and shall be transferred to the ALU under Formal 1 Micro-command control when read references are performed with the Extended Register File, Group III designated according to 3.2.3.7, Item d and 3.8.1.1, Item c for Boundary Crossing and Normal Modes, respectively.

For timing requirements, see Figure 7.

3.2.4.8 Extended Register Read

This single control signal from the CPU shall be abbreviated +ERFG3RD and shall indicate the execution of each Formal 1 Micro-command designating the Extended Register File, Group III for the purpose of performing a read reference.

This read control signal shall be shared by Processor States 0 through 3 and shall be active during all minor cycles in which a CLA, LAB, LAW, LAW\, LBL, LBW, LBW\, LDB, LDW, or LDW\ Micro-command is executed for which the Extended Register File is designated according to 3.2.3.7, item d and 3.8.1.1, item c, for Boundary Crossing and Normal Modes, respectively.

For timing relationships, see Figure 7.

3.2.4.9 Request

These 4 control signals to the CPU shall be abbreviated -REQ-0 through -REQ-3, individually corresponding to Processor States 0 through 3. These signals shall provide the means for accomplishing resource utilization requests as originated on a Processor State basis within the Extended Register File, Group III control logic.

These control signals shall be accommodated at the set inputs of the associated Busy Flip/Flops in the B/A Register as described in 3.2.3.1, item c. These set inputs shall be resynchronized to the extent that they shall be disabled during minor cycles E6, E7,E8, and E9.

When the associated Processor State, 0 through 3, requires a major cycle, the appropriate Request signal shall be active until a major cycle is allocated as indicated by the active state of the associated Execute signal described in 3.2.4.1. When the corresponding Request and Execute signals are simultaneously active, the allocation of an additional major cycle for the associated Processor State shall depend on the timing of their simultaneity with respect to resynchronization of the B/A Register as described in 3.9 and Micro-command control effecting the contents of the B/A Register during the current major cycle as established by firmware conventions for each of the Processor States, 0 through 3.

3.2.4.10 Attention

These 3 control signals to the CPU shall be abbreviated -ATTN-1, -ATTN-2 and -ATTN-3 corresponding to Processor States 1, 2, and 3,respectively. These signals shall provide an additional means for accomplishing resource utilization requests as originated on a Processor State basis within the Extended Register File, Group III control logic for Processor States 1, 2, and 3.

These control signals shall be accommodated at the set inputs of the associated Busy Flip/Flops in the B/A Register as described in 3.2.3.1, item c. These set inputs shall be resynchronized to the extent that they shall be disabled during minor cycles E6, E7, E8, and E9.

When the associated Processor State, 1 through 3, requires a major cycle, the appropriate Attention signal shall be active (but enabled at the set input to the associated Busy Flip/Flop only when the corresponding Active Flip/Flop is in the cleared state as described in 3.2.3.1, item c) until a major cycle is allocated as indicated by the active state of the associated Execute signal described in 3.2.4.1. When the corresponding Attention and Execute signals are simultaneously active in the presence of the cleared state of the associated Active Flip/Flop, the allocation of an additional major cycle for the associated Processor State shall depend on the timing of their simultaniety with respect to resynchronization of the B/A Register as described in 3.9 and Micro-command control affecting the contents of the B/A Register during the current major cycle as established by firmware conventions for each of the Processor States, 0 through 3.

3.2.4.11 Priority

These 4 control signals to the CPU shall be abbreviated +PRI-0 through +PRI-3, individually corresponding to Processor States 0 through 3. These signals shall provide the means for accomplishing disproportionately greater use of the common resources on the part of Processor States 0 through 3 by means of establishing Priority Modes of operation on their behalf. These signals shall be originated on a Processor State basis within the Extended Register File Group III control logic but shall be individually conditioned under Micro-command control only, by means of the associated Enable Priority Flip/Flops in the C Register as described in 3.2.3.5, item b.

The active state of these Priority signals shall be effective only when the associated Processor State has both its Busy and Enable Priority Flip/Flops in the set state. The coincidence of these conditions shall be resynchronized for each Processor State 0 through 3, at the inputs to the Resource Allocation Network as described in 3.9.

3.2.4.12 End of Transfer

These 4 control signals to the CPU shall be abbreviated -EOT-0 through -EOT-3, individually corresponding to Processor States 0 through 3. In the active state, these signals shall provide the means for accomplishing an I/O Exit during the execution of CIO1 and CIO2 Micro-commands as described in 3.8.12.5. These signals shall be originated on a Processor State basis within the Extended Register File, Group III control logic.

During each major cycle allocated to Processor States 0 through 3, the state of the associated End of Transfer signal must be stable during, and for 200 n/s prior to, the execution of CIO1 and CIO2 Micro-commands in order to obtain predictable results. When the associated signal is not synchronous to the extent just described, the execution of CIO1 and CIO2 Micro-commands may result in machine malfunction.

3.2.4.13 I/O Exit

This single control signal from the CPU shall be abbreviated +IOEXIT and shall be shared by Processor States 0 through 3.

This output control signal shall be active during the execution of CIO1 or CIO2 Micro-commands only, under the conditions described in 3.8.12.5.

For timing relationships, see Figure 7.

3.3 Register Option

The Register Option shall be functionally divided into four parts as related to the following Selectable Register Features:
The Relocation and Protection Feature
The Basic Storage Protection Feature
The Job Accounting Feature
The ECC Feature (Register Set)

The Relocation and Protection Feature and Basic Storage Protection Feature shall be mutually exclusive.

The registers and networks within each of these features shall provide the means for accomplishing the associated operations as described in 3.3.1 through 3.3.4. The majority of these operations shall be under hardware control as specified herein and shall be accomplished dynamically as required. When registers within these features must be referenced under Micro-command control for the purpose of transferring data between the CPU and the Register Option, a major cycle shall be required similar to Main Storage references. Register Option references under Micro-command control shall be differentiated from Main Storage references as described in 3.8.5.1. Register Option read references shall be differentiated from write references under Micro-command control in the same manner as for Main Storage references as described in 3.8.5.2.

During all Register Option references, the contents of the S Register in the ALU section of the CPU shall designate the register number according to the following format:

00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15

(S)=

NOT USED	FEATURE	STATE	REGISTER

a. Bits 00 through 03 shall not be used but shall be referred to as being in the clear state for the purpose of 16-bit hexadecimal notation.

b. Bits 04 through 07 shall specify the feature, or register set within a feature, according to the following hexadecimal notation.

0: Relocation and Protection Feature : Segment Tag File
1: Relocation and Protection Feature : Protect Matrix
2: Relocation and Protection Feature : Segment Relocation Table

3: Relocation and Protection Feature: Address-Mode Register
4: Relocation and Protection Feature: Parity Error Tag Register
5: Basic Storage Protection Feature: Bounds Registers
6: Job Accounting Feature: Job Accounting Registers
7: Not Used.
8/9: ECC Feature: Main Storage Data Register
A/B: ECC Feature: Log Register
C/D: ECC Feature: Generated Check Bits
E/F: ECC Feature: Read Check Bits

c. Bits 08 through 10 shall specify a Processor State when referencing the Segment Tag File, the Protection Matrix, the Bounds Registers and the Job Accounting Registers. For all other Register Option references these bits shall be unused but shall be referred to as being in the clear state for the purpose of 16-bit hexadecimal notation.

d. Bits 11 through 15 shall specify a register number (1 of 32) when referencing the Segment Tag File. Bits 11 through 14 shall specify a double-word register number when referencing the Segment Relocation Table with bit 15 specifying the left-most word when in the clear state and the right-most word when in the set state. Bit 15 shall also be used to specify the left-most word in the clear state and the right-most word in the set state when referencing the double-word registers within the Job Accounting Feature. Finally bit 15 in the clear state shall specify the Write Restriction bits and in the set state shall specify the Read Restriction bits when referencing the Protection Matrix. For all cases just described in which bits 11 through 14 are unused, and for all cases in which bits 11 through 15 are unused, they shall be referred to as being in the clear state for the purpose of hexadecimal notation.

3.3.1 Relocation and Protection Feature

The Relocation and Protection feature shall expand the Main Storage Address capabilities of the 7300 Processor from 65,536 bytes to 1,048,576 bytes. In addition, this feature shall provide the facilities for dynamically performing Main Storage Address relocation and Main Storage protection on a Processor State basis.

a. The expansion of Main Storage Addresses shall be accomplished for Processor States 0 through 7 through the implementation of a Segment Tag File containing 256 4-bit entries. These 4-bit values, referred to as Segment Tags, shall serve as left-most extensions to each of the corresponding 256 16-bit registers comprising the Basic Register File within the CPU. The 20 bit Main Storage Address thus provided shall be referred to as the System Address.

   Address expansion shall be accomplished with respect to 7300 Console operations by means of Segment Tag additions to the associated CA and CD Registers. Likewise, a Segment Tag addition shall be provided for the PE Register such that a 20-bit Main Storage Address may be recorded during each Main Storage reference for which a Main Storage Parity Error Trap occurs.

   For purposes of performing relocation and protection, the System Address shall be divided such that the left-most 4-bits shall represent a Segment Tag and the right-most 16-bits shall represent a Displacement. This 16-bit Displacement shall be further divided, into bytes, such that the left-most 8-bits shall be referred to as a Page Displacement and the right-most 8-bits shall be referred to as a Byte Displacement. The Byte Displacement shall not participate in Main Storage Address relocation and Main Storage protection operations.

b. Relocation shall be performed on a Main Storage page basis for which each page shall consist of 256 bytes. (Thus, Physical Main Storage Addresses shall be capable of expressing 4096 pages). Relocation shall be accomplished through the implementation of a Segment Relocation Table containing 16-24-bit entries in a 32-bit format for which 8 bits shall be defined as being in the clear state. The 4-bit Segment Tag portion of the 20-bit System Address described in item a, shall be used to reference 1 of the 16 entries in the Segment Relocation Table. The Page Displacement Portion of the 20-bit System Address shall be added (right-justified, zeroes extended) to the right-most 12-bit output of the Segment Relocation Table.

Thus, a 20-bit Physical Address shall be provided to Main Storage for which dynamic relocation has been performed for the left-most 12-bits. These relocation operations shall be based on the System Address designation of 1 of 16 Main Storage Segments comprised of a maximum of 256 pages each. (For clarification, see 3.3.1.2 and its accompanying diagrams).

c. Storage Protection shall be accomplished during the course of performing relocation, by means of hardware checks involving the Validity bit contained left-most in each Segment Relocation Table entry, by means of hardware checks involving the comparison of the maximum page number (also designated within the left-most word of each Segment Relocation Table entry) with the Page Displacement portion of the System Address, and by means of hardware checks involving the Read and Write restriction bits contained within the Protection Matrix on a Processor State and Segment Tag basis. For clarification, see 3.3.1.2 and 3.3.1.3 and their accompanying diagrams. All Main Storage Addressing violations thus detected, shall result in a hardware trap sequence (Control Storage Address $X01_{16}$) at the end of the current major cycle allocated to Processor States 0 through 7. Once the hardware trap sequence has been performed for the associated Processor State 0 through 7, further operations relative to the Main Storage Addressing violation shall be considered totally under Micro-command control beginning at Control Storage Address $X01_{16}$.

Main Storage protection during Console State operations shall not be provided.

d. Relocation and protection operations shall be conditioned on a Processor State basis by means of an Address-Mode Register. The contents of the 16-bit Address-Mode Register shall specify; neither relocation nor protection, relocation only, or relocation and protection for each individual Processor State, 0 through 7.

With respect to relocation controls, the Address-Mode Register function shall be accomplished for Console State operations involving Main Storage references by means of the Console Main Storage, Relocate/Off switch described in 3.10.3.12.

3.3.1.1 Segment Tags

259 Segment Tag Registers shall be provided by the Relocation and Protection Feature, not including the 4-bit, left-most extension to the S Register which shall be under Load S Micro-command control as described in 3.8.5.1 for the purpose of accommodating Segment Tag values.

a. The Segment Tag File shall consist of 256 4-bit Registers with one-for-one correspondence to the registers within the Basic Register File.

During each minor cycle associated with a major cycle in which a Register Option reference is not performed, the Segment Tag File shall be addressed by Format 1 Micro-commands identically to the Basic Register File as described in 3.8.1.1, item c. Moreover, Format 1 Micro-commands shall be implicitly capable of performing Register File read and write references in which the Segment Tag File shall participate as described in 3.8.5.1 and 3.8.5.7. Likewise, all Format 1 Micro-commands which perform write references to the Basic Register File, shall implicitly transfer the contents of the 4-bit S Register Segment Tag Extension to the appropriate register number within the Segment Tag File, whenever Micro-command execution for the associated major cycle begins at Control Storage Address $X00X_{16}$, (RNI), or when immediately preceded by an IDX Micro-command as described in 3.8.5.7.

During each major cycle for which a Register Option reference is performed, the Segment Tag File shall be addressed according to the contents of the right-most 16 bits of the S Register using the following hexadecimal notation:

Processor State	Register Numbers
0	0000 - 001F
1	0020 - 003F
2	0040 - 005F
3	0060 - 007F
4	0080 - 009F
5	00A0 - 00BF
6	00C0 - 00DF
7	00E0 - 00FF

With respect to 16-bit data paths, Register Option write references to the Segment Tag File shall only make use of the outputs from the right-most 4 bit positions of the D Register and Register Option read references from the Segment Tag File shall transfer zeroes to the D Fan-In Network in the left-most 12 bit positions, Segment Tag data to the right-most 4 bit positions.

b. The CA and CD Segment Tag Registers shall be subject to Console controls to the extent described in 3.10.3.2 and 3.10.3.5, respectively.

Implicit Micro-command control of these Segment Tag registers shall be limited to the extent required for implementation of the Console Operations described in 3.10.3.11, items d, f, and g, and shall not include incremental capabilities.

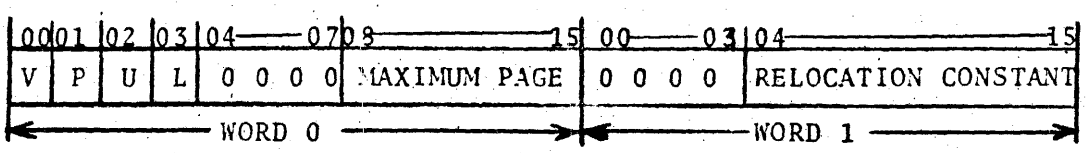
The means for performing Register Option references under Micro-command control shall not be provided for the CA and CD Segment Tag Registers.

c. The PE Segment Tag Register shall operate identically to the PE Register described in 3.2.3.4 with respect to Micro-command controlled write references and all hardware controls.

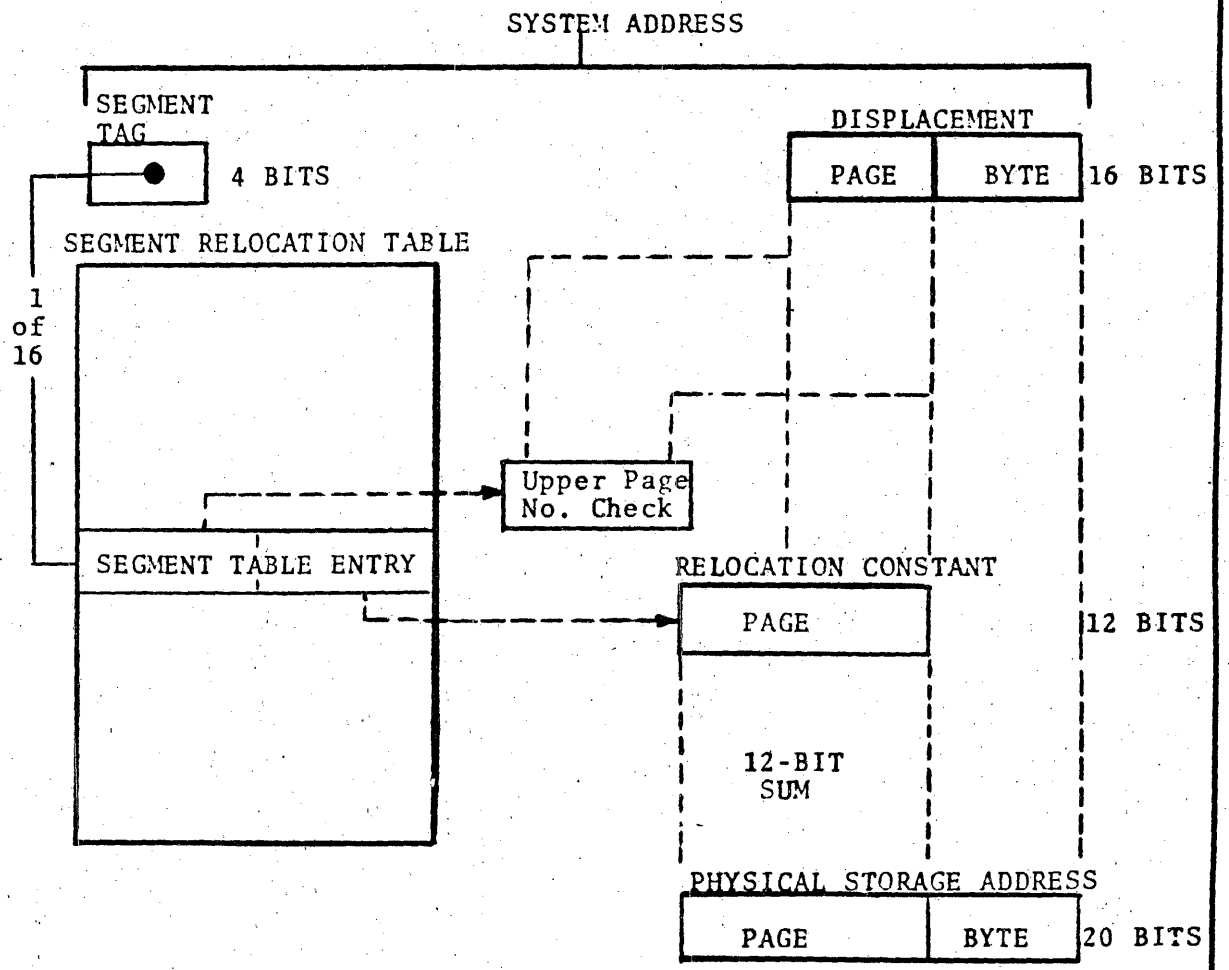
The PE Segment Tag Register shall be read under Micro-command control only by means of Register Option read references for which the right-most 16 bits of the S Register are equal to 0400_{16}. The data format for such references shall conform to that previously described for the Segment Tag File in item a, namely, zeroes in the left-most 12 bit positions, Segment Tag data in the right-most 4 bit positions.

3.3.1.2 Segment Relocation Table

The Segment Relocation Table shall consist of 16 24-bit registers formatted as 32-bit double-words as follows:



For the purpose of performing dynamic Main Storage Address relocation and Main Storage protection on a segment/page basis, the Segment Relocation Table shall be addressed and its Maximum Page (Word 0, bits 08 through 15) and Relocation Constant (Word 1, bits 04 through 15) fields shall be utilized as shown in the following diagram.



a. For the purpose of performing Main Storage Address relocation and Main Storage protection on a segment/page basis, the contents of each entry in the Segment Relocation Table shall be specifically utilized as follows:

When the "V" designator (Word 0, Bit 00; validity) is in the cleared state or when the "Maximum Page" field (Word 0, Bits 08 through 15) is exceeded in value (unsigned) by the Page Displacement portion of the System Address, a Main Storage Addressing violation shall be detected.

The Relocation Constant (Word 1, Bits 04 through 15) shall be added in 2's complement to the Page Displacement portion of the System Address to provide the left-most 12 bits of the Physical Address. (With respect to the 12-bit Relocation Constant, the Page Displacement shall be added right-justified, with zeroes extended).

The "P", "U", and "L" designators (Word 0, bits 01 through 03) along with the two fields of zeroes (Word 0, Bits 04 through 07 and Word 1, Bits 00 through 03) shall be unused.

b. For the purpose of performing Register Option references under Micro-command control, the Segment Relocation Table shall be addressed by the right-most 16-bits of the S Register according to the following hexadecimal notation:

SEGMENT RELOCATION TABLE Double Word Entry	REGISTER NUMBER Word 0 / Word 1
0	0200 / 0201
1	0202 / 0203
2	0204 / 0205
3	0206 / 0207
4	0208 / 0209
5	020A / 020B
6	020C / 020D
7	020E / 020F
8	0210 / 0211
9	0212 / 0213
A	0214 / 0215
B	0216 / 0217
C	0218 / 0219
D	021A / 021B
E	021C / 021D
F	021E / 021F

The Segment Relocation Table shall not be physically present in"fields of zeroes"positions (Word 0, Bit 04 through 07 and Word 1, Bits 00 through 03) and Register Option write references which transfer non-zero values to these bit positions within the Segment Relocation Table shall have no effect on these fields. Likewise, zeroes shall always be obtained for these fields when Register Option read references are performed from the Segment Relocation Table.

3.3.1.3 Protection Matrix

The Protection Matrix shall consist of 16 16-bit registers and shall provide the means for performing dynamic Main Storage Protection with respect to privacy (read restrictions) and integrity (write restrictions). This shall be achieved on the basis of individual Processor States, 0 through 7, having individual read and write restrictions for each of the Main Storage segments as defined by the Segment Tag (designating a segment number) portion of the System Address.

a. When Main Storage references are performed on the part of Processor States 0 through 7, and the read or write nature of the references to the designated segment are restricted by the set state of the corresponding bit in the Protection matrix, a Main Storage Addressing violation shall be detected.

The functional arrangement of the restriction bits within the Protection Matrix is shown in the following diagram for which segment numbers of 0 through F in hexadecimal notation correspond to bit positions 00 through 15, respectively, in each of these 16 Processor State related registers.

SEGMENT NUMBER

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Write Restriction	0																
	1																
	2																
Processor No.	3																
	4																
	5																
	6																
	7																
Read Restriction	0																
	1																
	2																
Processor No.	3																
	4																
	5																
	6																
	7																

b. For the purpose of performing Register Option references under Micro-command Control, the Protection Matrix shall be addressed by the right-most 16 bits of the S Register according to the following hexadecimal notation.

Processor State	Register Number Write Restriction/Read Restriction
0	0100/0101
1	0120/0121
2	0140/0141
3	0160/0161
4	0180/0181
5	01A0/01A1
6	01C0/01C1
7	01E0/01E1

3.3.1.4 Address-Mode Register

The Address Mode Register shall consist of 16-bits and shall provide the means for conditioning dynamic relocation and protection operations on a Processor State basis.

The Address-Mode Register shall contain an "R" designator bit for each Processor State, 0 through 7, in the left-most byte and a "D" designator bit for each Processor State, 0 through 7, in the right-most byte in the following format.

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
"R" Designators								"D" Designators							

During each Main Storage reference on the part of Processor States 0 through 7 the appropriate "R" and "D" designators shall be hardware interpreted for the associated Processor States as follows:

a. When the "R" designator is clear, neither relocation nor protection shall be performed. The 20-bit System Main Storage Address shall be used directly as the Physical Main Storage Address. The detection of Main Storage Address violations shall have no effect.

b. When the "R" designator is set and the "D" designator is clear, dynamic Main Storage Address relocation shall occur. The 20-bit System Address shall be converted to a 20-bit Physical Address as described in 3.3.1.2. The detection of Main Storage Address violations shall have no effect except when the "V" designator is clear for the associated Segment Relocation Table entry in which case a hardware trap sequence shall be performed and Main Storage write operations shall be disabled.

c. When the "R" and "D" designators are both set, dynamic Main Storage Address relocation shall occur and the detection of any Main Storage Address violations shall result in a hardware trap sequence with Main Storage write operations disabled.

The Address-Mode Register shall be referenced under Micro-command control only by means of Register Option references for which the right-most 16-bits of the S Register are equal to 0300_{16}.

The contents of the Address Mode register shall be cleared by System Reset as described in 3.10.3.8.

3.3.2 Basic Storage Protection Feature

The Basic Storage Protection Feature shall consist of 3 16-bit registers, referred to as Bounds Registers, and shall provide the means for accomplishing dynamic Main Storage protection, during write references only, on the part of Processor States 5, 6, and 7. This protection shall be provided on the basis of Main Storage pages consisting of 256 bytes each.

a. Each of the 3 Bounds Registers associated with Processor States 5, 6, and 7 shall be formatted as follows:

00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15

Upper Bounds	Lower Bounds

The Upper Bounds field shall designate a maximum Main Storage page number and the Lower Bounds field shall designate a minimum Main Storage page number.

When the Upper and Lower Bounds fields are equal, Main Storage write references shall be confined to that Main Storage page as performed on the part of the associated Processor State. When the contents of any Bounds Register are equal to $FF00_{16}$, Main Storage protection shall be disabled for write references performed on the part of the associated Processor State.

b. During each Main Storage write reference, performed on the part of Processor States 5,6, and 7, the contents of the appropriate bounds Register shall be read. When the left-most 8 bits (page number) contained in the S Register are greater than the associated Upper Bounds field or less than the Lower Bounds field, a Main Storage Addressing violation shall be detected. A Main Storage Addressing violation thus detected shall result in a hardware trap sequence (Control Storage Address $X010_{16}$) at the end of the major cycle and shall disable the

Main Storage write reference. Once the hardware trap sequence has been performed for the associated Processor State 5, 6, or 7, the Main Storage Addressing violation shall be considered totally under Micro-command control beginning at Control Storage Address $X010_{16}$.

c. For the purpose of performing Register Option references under Micro-command control, the Bounds Registers shall be addressed by the right-most 16 bits of the S Register according to the following hexadecimal notation:

Processor State	Register Number
5	05A0
6	05C0
7	05E0

3.3.3 Job Accounting Feature

The Job Accounting Feature shall consist of 8 32-bit registers corresponding to Processor States 0 through 7 and shall provide the means for accounting for all major cycles allocated to these processor states on an individual basis.

a. During each major cycle allocated to Processor States 0 through 7, the contents of the appropriate Job Accounting Register shall be increased by one except during Register Option references to the Job Accounting Feature itself.

b. For the purpose of performing Register Option references under Micro-command control, the Job Accounting Registers shall be addressed by the right-most 16-bits of the S Register according to the following hexadecimal notation:

Job Accounting Register Processor State	Register Number Word 0 / Word 1
0	0600 / 0601
1	0620 / 0621
2	0640 / 0641
3	0660 / 0661
4	0680 / 0681
5	06A0 / 06A1
6	06C0 / 06C1
7	06E0 / 06E1

When the Job Accounting feature is addressed under Micro-command control for the purpose of performing Register Option write references, the entire 32-bit contents (Word 0, left-most 16-bits and Word 1, right-most 16-bits) shall be cleared within the appropriate Job Accounting Register regardless of the Word 0/Word 1 designation (Bit 15 of the S Register) and irrespective of the contents of the D Register.

3.3.4 ECC Feature (Register Set)

The Register Set associated with the ECC Feature shall consist of 4 16-bit quantities for which the format and function are described by the applicable document listed in 2.1.

Register Option read references under Micro-command control shall provide the means for addressing the ECC Register set from the CPU for the purpose of transferring the associated 16-bit quantities from Main Storage to the CPU. The right-most 16-bits of the S Register shall address the ECC Register Set during Register Option read references according to the following hexadecimal notation.

ECC Register Set	Register Numbers
Main Storage Data Register	0800 or 0900
Log Register	0A00 or 0B00
Generated Check Bits	0C00 or 0D00
Read Check Bits	0E00 or 0F00

3.4 ALU

The Arithmetic Logic Unit (ALU) shall consist of those registers and logical networks required for implementation of the Micro-command repertoire.

3.4.1 Au Register

The Au Register shall consist of 16-bits, designated 00 through 15 from left to right. During operations with signed magnitudes, the left-most bit, 00, shall be treated as the sign bit position.

a. The Au Register shall accommodate the following inputs:

Register File (True and 1's complement states)
Shift Network (Left-most output, 16 bits)
Bit Sense (1 of 16 code)
D Fan-In Network (True and 1's complement states)

b. The Au Register shall provide outputs to the following:

Shift Network (Left-most input, 16 bits)
Bit Sense (Bit multiplex and bit scan)
ALU Fan-In Network (Direct)
ALU Fan-In Network (Additively combined with Bu)
ALU Fan-In Network (Logically combined with Bu)
Compare (Compared with Bu and with zero)

The Au Register shall be cleared by the occurrence of a System Reset as described in 3.10.3.8, item d.

The Au Register shall be set by means of the Console control described in 3.10.4.20, item a.

The contents of the Au Register shall be available at the Console Data Register Display indicators when selected by means of the Console control as described in 3.10.3.7.

3.4.2 Bu Register

The Bu Register shall consist of 16 bits, designated 00 through 15 from left to right. During operations with signed magnitudes, the left-most bit, 00, shall be treated as the sign bit position.

a. The Bu Register shall accommodate the following inputs:

Register File (True and 1's complement states)
Shift Network (Right-most output, 16 bits)
Bit Sense (Bu Adder)
Constant Generator

b. The Bu Register shall provide outputs to the following:

Shift Network (Right-most input, 16 bits)
Bit Sense (Bu Adder)
ALU Fan-In Network (Direct)
ALU Fan-In Network (Additively combined with Au)
ALU Fan-In Network (Logically combined with Au)
Compare (Logically and Algebraically with Au)

The Bu Register shall be cleared by the occurrence of a System Reset as described in 3.10.3.8, item d.

The Bu Register shall be set by means of the Console control described in 3.10.4.20, item b.

The contents of the Bu Register shall be available at the Console Data Register Display indicators when selected by means of the Console Control as described in 3.10.3.7.

3.4.3 Force Carry Register

The Force Carry Register shall consist of a single Flip/Flop accommodating set, clear and Link Status Bit inputs under Micro-command control. The output from the Force Carry Register shall serve as a carry input to the right-most bit, 15, of the Adder described in 3.4.5.

The Force Carry Register shall be cleared by the occurrence of a System Reset as described in 3.10.3.8, item d.

The Force Carry Register shall not be set, but at the carry input to the Adder it shall appear to be in the set state during the simultaneous selection of the Console controls as described in 3.10.4.20, item c.

3.4.4 Inner Carry Register

The Inner Carry Register shall consist of 4 Flip/Flops with carry inputs from the Adder only. These inputs from the Adder shall consist of group carry signals designated 0, 1, 2, and 3 corresponding to carries generated from or propagated through bits 00, 04, 08 and 12 respectively. These group carry signals from the Adder shall be transferred (clocked) to the Inner Carry Register during the execution of DSUM Micro-commands as described in 3.8.4.8.

The outputs from the Inner Carry Register shall be individually translated within the Constant Generator in such a way as to provide corresponding n/bl (4-bit group) inputs to the Bu Register as described for the CORC Micro-command in 3.8.7.6.

3.4.5 Adder

The Adder shall consist of an additive network for arithmetically combining the contents of the Au and Bu Registers. The Adder shall also accommodate the output of the Force Carry Register as a carry input to the right-most bit position, 15.

The inner carry mechanism within the Adder shall be based on 4-bit groups providing carry translations to the inputs of the Inner Carry Register. Likewise, the inner carry mechanism shall accommodate a disabling input such that inter-group carry inputs shall be in the cleared state only, following the execution of DIG and CORC Micro-commands as described in 3.8.7.5 and 3.8.7.6, respectively.

The output of the Adder shall be available to the ALU Fan-In Network for selection during write references to the Register File under Micro-command control.

The output of the Adder shall be available at the Console Data Register Display indicators when selected by means of the Console Control as described in 3.10.3.7.

3.4.6 Shift Network

The Shift Network shall provide the means for implementing the Shift class of Micro-commands described in 3.8.8.

Within two minor cycles, the Shift Network facilities shall be capable of selecting a Shift-count, performing a 2's complement of the shift count as Micro-command designated, and shifting the 32-bit combined contents of the Au/Bu Registers 0 to 15_{10} places left, end-off, zeroes inserted.

3.4.7 ALU Status

ALU Status facilities shall consist of the means for translating Overflow, Link and Au Register comparison conditions.

3.4.7.1 Overflow

Overflow status shall be transferred to the Su Register, bit 00 position, by means of SUM and DSUM Micro-commands as described in 3.8.4.7 and 3.8.4.8, respectively.

Overflow shall be defined as occurring whenever the contents of the Au and Bu Registers have the same sign, but produce at the output of the Adder an oppositely signed Sum; $Au_{00} \neq Sum_{00}$ and $Sum_{00} \neq Bu_{00}$.

Overflow Status thus contained in the Su Register shall be transferred to the Basic Register File, bit 00, by means of RNI1 and RNI2 Micro-commands as described in 3.8.11.5 and 3.8.11.6, respectively.

3.4.7.2 Link

Link Status shall be transferred to the Su Register, bit 01 position, by means of SUM and DSUM Micro-commands as described in 3.8.4.7 and 3.8.4.8, respectively.

a. Link Status shall be defined as occurring whenever a carry output exists from bit position 00 of the Adder, provided the left-most byte of the common resource F Register is not equal to 50, 51, 52 or 53 in hexadecimal notation.

b. When the left-most byte of the common resource F Register is equal to 50, 51, 52 or 53 in hexadecimal notation, Link Status shall be defined as occurring whenever a carry output exists from bit position 08 of the Adder.

Link status thus contained in the Su Register shall be transferred to the Basic Register File, bit 03, by means of RNI1 and RNI2 Micro-commands as described in 3.8.11.5 and 3.8.11.6, respectively.

NOTE: The carry output from a particular bit position may be generated by that bit position itself or generated anywhere to the right of that bit position provided carry propagation occurs in all participating bit positions to the left of its generation.

3.4.7.3 Compare

Compare status relative to the contents of the Au Register shall be provided within the ALU for the purpose of performing CMP (3.8.4.9), CMU (3.8.4.10), SKZ (3.8.10.1), SKN (3.8.10.2), SKG (3.8.10.5), SKL (3.8.10.6), SKE (3.8.10.7), SKE\ (3.8.10.8), FZJ (3.8.11.3), CI01 (3.8.12.5, item a) and CI02 (3.8.12.5, item b) Micro-commands.

Each of the following conditions shall be translated for the associated Micro-commands.

(Au) equal to zero: SKZ, FZJ
(Au) not equal to zero: SKN
(Au)equal to (Bu): CMP, CUM, SKE, CI01
(Au) not equal to (Bu): SKE\, CI02
(Au) algebraically greater then (Bu): CMP
(Au) logically greater than (Bu): CMP, CMU, SKG
(Au) algebraically less than (Bu): CMP
(Au) logically less than (Bu): CMP, CMU, SKL

3.4.8 Bit Sense

Bit sense logic within the ALU shall provide the means for testing the contents of the Au Register under Micro-command control relative to the state of an individual bit position (bit multiplex) or with respect to a left to right search (bit scan) in which case the result of scanning Au shall result in an addition to the contents of the Bu Register.

3.4.8.1 Au Bit

The output of the Au Register shall be bit multiplexed for the purpose of implementing the SKB and SKB\ Micro-commands described in 3.8.10.3 and 3.8.10.4, respectively.

3.4.8.2 Au Scan

The output of the Au Register shall be scanned and the scan result encoded for the purpose of implementing the Bit Sense class of Micro-commands described in 3.8.9.

3.4.8.3 Bu Adder

The Bu Adder shall provide the means for adding the result of the Au scan operation to the contents of the Bu Register. According to the first bit position sensed in Au as described in 3.8.9, the following values in hexadecimal notation shall be correspondingly added to the contents of the Bu Register.

Au Bit Position Detected	Bu Addend
00	0000
01	0001
02	0002
03	0003
04	0004
05	0005
06	0006
07	0007
08	0008
09	0009
10	000A
11	000B
12	000C
13	000D
14	000E
15	000F
None	0010

3.4.9 Constant Generator

The Constant Generator shall provide immediate operands to the Bu Register as required by the Immediate Operand class of Micro-commands described in 3.8.7 as well as the Load S Micro-commands described in 3.8.5.1.

3.4.10 ALU Fan-In Network

The ALU Fan-In Network shall provide the means for selecting ALU data to be transferred to the Register File under Micro-command control. During major cycles allocated to the Null State, the ALU Fan-In Network shall provide the means for selecting ALU data to be transferred to the Console Data Register Display indicators under Console switch control as described in 3.10.3.7.

The output of the ALU Fan-In Network shall selectively provide the following:

Au Register
Bu Register
D Fan-In Network (Full Word)
D Fan-In Network (Byte 0)
D Fan-In Network (Byte 1)
Sum of Au and Bu
Exclusive Or of Au and Bu
Inclusive Or of Au and Bu
Logical Product of Au and Bu
Compare Status of Au and Bu (left-most byte)
ALU Status of Overflow and Link (left-most byte)
Zeroes

3.4.11 S Register

The 16-bit S Register shall provide the means for addressing Main Storage and the Register Option.

The input to the S Register shall be provided from the Register File under Load S Micro-command control as described in 3.8.5.1.

The output from the S Register shall be provided to Main Storage by way of the Register Option, (Basic Storage Protection Feature or Relocation and Protection Feature). In addition, the output of the S Register shall be used for Breakpoint stop operations as described in 3.10.3.13, item a, and shall be available to the Console Address Register Display indicators when selected by means of the Console control as described in 3.10.3.4.

In the presence of the Relocation and Protection Feature, the S Register shall be left-most extended by 4 bit positions as described in 3.3.1.1.

3.4.12 D Register

The 16-bit D Register shall provide the means for transferring data to Main Storage and the Register Option.

The input to the D Register shall be provided from the Register File under Micro-command control.

The output from the D Register shall be provided to Main Storage by way of the Register Option, (Basic Storage Protection Feature or Relocation and Protection Feature). During Main Storage references performing partial (byte) write operations under Micro-command control, the output from the D Register shall be sent to Main Storage such that the right-most byte shall be duplicated in the left-most byte position as described in 3.8.5.4.

In addition the output of the D Registers shall be provided to the D Fan-In Network.

Micro-commands related to the D Register are described in 3.8.5 and 3.8.6, including timing constraints.

The D Register shall be cleared by the occurrence of a System Reset as described in 3.10.3.8, item d.

The D Register shall be set by means of the Console controls described in 3.10.4.20, item c.

The contents of the D Register (by way of the D Fan-In and ALU Fan-In Networks) shall be available at the Console Data Register Display indicators when selected by means of the Console control as described in 3.10.3.7.

3.4.13 D Fan-In Network

This 16-bit fan-in shall provide the means for transferring data from Main Storage, the Register Option, and the D Register to the Au Register and the ALU Fan-In Network.

In addition, the output of the D Fan-In Network shall be provided to the Shift Network for selection as a shift-count (Bits 12 through 15) and shall be provided to the Address Table addressing mechanism, in lieu of Su, for the purpose of executing FRJ Micro-commands (Bits 00 through 08 and bit 12 of the D Fan-In Network output).

Timing constraints with respect to hardware control of the inputs to the D Fan-In Network are described in 3.8.5.

3.5 Control Storage

Control Storage shall be divided into two functional areas referred to as Control Storage proper and the Address Table.

Control Storage proper shall provide the means for storing Micro-commands to be read, translated and executed under hardware control.

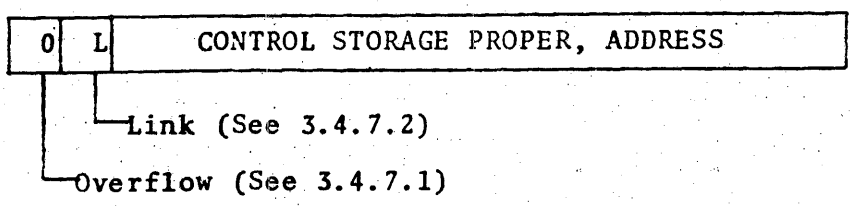
The Address Table shall provide the means for storing Control Storage Addresses such that FRJ Micro-commands may perform high speed branch operations for decoding purposes. (See 3.8.11.2).

All Control Storage references, read and write, which are performed for purposes not directly related to Micro-command execution shall be associated with provisions for 7300 Processor maintainability and availability. Such operations, performed under hardware control as initialized from the Console, shall be referred to as Control Storage Read and Control Storage Write operations as described in 3.10.3.11, items h and i, respectively.

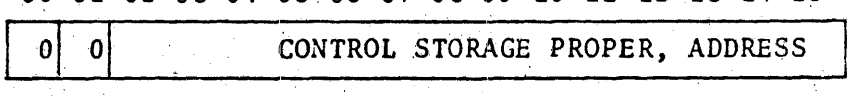
3.5.1 Su

The Su Register shall provide the only means for directly addressing Control Storage proper. During all operations not involving Micro-command execution, (namely, Control Storage Read and Control Storage Write, Console operations), the Su Register shall provide the only means for directly addressing the Address Table.

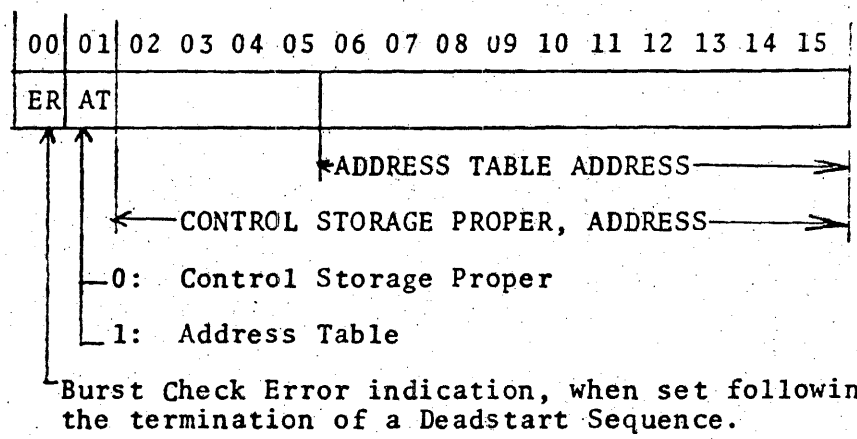
a. During Micro-command execution, the Su Register shall have the following format and shall be displayed as such by the Console Address Register Display indicators when selected according to 3.10.3.4.



b. During Micro-command execution, the Su Register shall have the following format for Breakpoint purposes as described in 3.10.3.13, item b, provided the Su Register is not selected as the input to the Console Address Register Display indicators.



c. During Control Storage references performed by the Console State for the express purpose of reading or writing Control Storage, the Su Register shall have the following format and Micro-command execution shall be excluded.



3.5.2 Address Constants

Control Storage proper shall be addressed such that Micro-command execution shall begin, for the appropriate Processor States and under the designated conditions, at the address constants as follows:

a. Control Storage proper shall be referred to as RNI0 at addresses 0000, 1000, 2000, and 3000 in hexadecimal notation. These address constants shall be designated in a combined form as $X000_{16}$ and shall be hardware generated to the extent described in 3.10.4.18.

b. Control Storage proper shall be referred to as RNI1, at addresses 0002, 1002, 2002 and 3002 in hexadecimal notation. These address constants shall be designated in a combined form as $X002_{16}$ and shall be explicitly generated under Micro-command control as described in 3.8.11.5.

c. Control Storage proper shall be referred to as RNI2 at addresses 0009, 1009, 2009 and 3009 in hexadecimal notation. These address constants shall be designated in a combined form a $X009_{16}$ and shall be explicitly generated under Micro-command control as described in 3.8.11.6.

NOTE: The RNI0, RNI1 and RNI2 addresses shall be hardware translated at the beginning of each major cycle for Breakpoint purposes as described in 3.10.3.13 through 3.10.3.17, for Stop/Step operations as described in 3.10.3.18, and for implicit Segment Tag write transfers as described in 3.3.1.1, item a.

d. Control Storage proper shall be referenced during Illegal Address trap sequences at addresses 0010, 1010, 2010, and 3010 in hexadecimal notation. These address constants shall be designated in a combined form as $X010_{16}$ and shall be hardware generated as a result of Main Storage Address violations detected and enabled as described in 3.3.1 and 3.3.2.

e. Control Storage proper shall be referenced during Main Storage Parity Error trap sequences at addresses 0018, 1018, 2018, and 3018 in hexadecimal notation. These address constants shall be designated in a combined form as $X018_{16}$ and shall be hardware generated for Processor States 0 through 7 as described in 3.10.4.4 with the exception that "Out of Range" addresses shall be included with the detection of Parity Errors during Main Storage read references in the absence of the ECC Feature as well as the detection of non-correctable data errors during Main Storage read references in the presence of the ECC Feature. The occurrence of all hardware controlled trap sequences to addresses $X018_{16}$ shall be conditioned by the state of the Storage Parity Disable switch described in 3.10.4.16. Once this trap sequence has occurred for the associated Processor State, further operations relative to the Main Storage Parity Error shall be considered totally under Micro-command control.

f. Control Storage proper shall be referenced during Control Storage Parity Error trap sequences at addresses 0028, 1028, 2028 and 3028 in hexadecimal notation. These address constants shall be designated in a combined form as $X028_{16}$ and shall be hardware generated, for Processor States 0 through 7 only, as described in 3.10.4.5. Likewise, the occurrence of trap sequences to addresses $X028_{16}$ shall be conditioned by the state of the Storage Parity Disable switch described in 3.10.4.16. Once this trap sequence has occurred for the associated Processor State, further operations relative to the Control Store Parity Error shall be considered under Micro-command control.

NOTE: The order of precedence for the trap sequence shall be: Control Storage Parity Error, Main Storage Parity Error and Illegal Address as described in items f, e, and d, respectively. However, Main Storage Parity shall not be checked when Main Storage Address violations are detected as described in 3.3.1 and 3.3.2.

For items a through f in which the left-most 2-bits of the 14-bit address constants are not specifically designated, the value of the left-most 2-bits shall be derived identically to the manner described in 3.8.11, item b.

Trap Sequences, items d, e, and f, shall occur on minor cycle E7 and shall set the Busy Flip/Flop for the associated Processor State 0 through 7, under hardware control. Thus, Processor States 0 through 7 may not be stopped at the end of any major cycle in which such trap conditions are hardware detected, when the stop operation is expected to be achieved during that major cycle through the clearing of the associated Busy Flip/Flop, whether by means of Micro-command control on the part of the effected Processor State, or by means of the associated Console controls as described in 3.10.3.18.

g. Control Storage proper shall be addressed at 0100_{16} for Console State operations as described in 3.10.3.11, items a and g.

h. Control Storage proper shall be addressed at 0103_{16} for Console State operations as described in 3.10.3.11, items b and f.

i. Control Storage proper shall be addressed at 0106_{16} for Console State operations as described in 3.10.3.11, item c.

j. Control Storage proper shall be addressed at $010C_{16}$ for Console State operations as described in 3.10.3.11, item d.

k. Control Storage proper shall be addressed at 0112_{16} for Alternate Autoload sequence initialization as described in 3.10.2.4 and 3.10.2.5.

l. Control Storage proper shall be addressed at 0113_{16} for Primary Autoload initialization as described in 3.10.2.4 and 3.10.2.5.

3.5.3 Address Table

The Address Table shall consist of a minimum of 256 10-bit words. Address Table sizes of 512, 768, and 1024 10-bit words shall be possible on an optional basis.

a. The 256 word Address Table shall be addressed by the contents of Su as described in 3.5.1, item c, during Console State read and write references not involving Micro-command execution.

The 256 word Address Table shall be addressed by the output of the D Fan-In Network for a minimum of 2 minor cycles prior to the execution of the FRJ Micro-command described in 3.8.11.2. Bits 00 through 08 and bit 12 from the D Fan-In Network shall be encoded from 10 bits into 8 address bits substituted for the right-most bits from Su as follows:

D FAN-IN	← Su SUBSTITUTE TO THE ADDRESS TABLE →							
00 through 07	08	09	10	11	12	13	14	15
2X,3X,AX,BX	0	0	DF_{00}	DF_{03}	XB or XC-XF	XA or XC-XF	DF_{08}	DF_{12}
6X, 7X	0	1	0	DF_{03}	DF_{04}	DF_{05}	DF_{08}	DF_{12}
0X,1X,4X,5X 8X,9X,CX,DX	0	1	1	DF_{00}	DF_{01}	DF_{03}	DF_{04}	DF_{05}
EX	1	0	DF_{04}	DF_{05}	DF_{06}	DF_{07}	DF_{08}	DF_{12}
FX	1	1	DF_{04}	DF_{05}	DF_{06}	DF_{07}	DF_{08}	DF_{12}

The data output from the Address Table to the Console Data Register Display indicators shall be in the following format during Console read operations.

	00	01	02	03	04	05	06	07 08 09 10 11 12 13 14 15
Parity	P	0	0	0	0	1	DF_{03}	ADDRESS TABLE DATA

The data input to the Address Table from the Console Data Register shall be in the same format shown above with the exception of bits 01 through 06 which shall be unused during Console write operations.

The data output from the Address Table, transferred to bit positions 04 through 15 of the [illegible] Register during the execution of FRJ Micro-commands, shall correspond to the associated bit positions 04 through 15 also shown in the above format.

Horizontal parity for the Address Table, during both Console read operations and FRJ Micro-command execution, shall be valid when the total number of bits in the set state is odd for bit positions 00 and 07 through 15 only, i.e. without respect to the state of bits 01 through 06.

b. The 512 word Address Table is undefined with respect to address and data conventions at the present time.

c. The 768 word Address Table is undefined with respect to address and data conventions at the present time.

d. The 1024 word Address Table is undefined with respect to address and data conventions at the present time.

3.5.4 Control Storage, Read/Write

The means for performing Control Storage Read and Control Storage Write operations under hardware control shall be provided in a manner mutually exclusive with Micro-command execution. Such operations shall be selected and controlled through the use of the Console switches as described in 3.10.3.9 through 3.10.3.11.

3.5.5 Control Storage Read

The Console State shall be used to implement Control Storage Read operations under hardware control as described in 3.10.3.11, item h.

3.5.6 Control Storage Write

The Console State shall be used to implement Control Storage Write operations under hardware control as described in 3.10.3.11, item i.

Reset/Load sequences shall simulate Console operations to the extent described in 3.5.7.3, 3.5.8.2, and 3.5.9.2.

3.5.7 Reset/Load Sequence

The Reset/Load Sequence shall be initiated from one of three sources.

a. The trailing edge of Power-On System Reset at the completion of a power-up sequence.

b. The Reset/Load Switch as described in 3.10.2.12.

c. The presence of a Restart Reset/Load signal as described in 3.5.8.5.

The Reset/Load sequence shall consist of those operations described in 3.5.7.1 through 3.5.7.5.

3.5.7.1 Reset/Load System Reset

A System Reset shall be performed for a minimum of .4 m/s and a maximum of .6 m/s. For a description of the effects of Reset Load, see 3.10.3.8.

3.5.7.2 Reset/Load Pause

The trailing edge of System Reset shall generate a pause of 2.5 u/s minimum to 3.5 u/s maximum, to allow IFA logic to stabilize.

3.5.7.3 Reset/Load Initialization

Upon completion of the pause, the Reset/Load Flip-Flop shall set, and force the following conditions:

a. Reset/Load Initiate, see 3.5.8.1.

b. Control Storage Write; this signal is in parallel with and performs the same function as the Control Storage Write Operation selected from the Console, (See 3.10.3.11). This signal shall be disabled when the Console is in Maintenance Mode. Thus, Control Storage Write Operations shall be selected by means of the Console Mode Select Switch only, when the Console is in Maintenance Mode.

c. Console Stop; this signal is in parallel with and performs the same function as the Console Control Select switch, Stop/Step position, (See 3.10.3.9).

3.5.7.4 Reset/Load Data Transfer

a. Upon receiving the Reset/Load Initiate signal, the Integrated File Adapter or Integrated Card Adapter, as determined by the state of the Primary Source signal described in 3.5.8.3, shall transmit Data as described in 3.5.8.8, and 3.5.9.8, with Data Strobes as described in 3.5.8.2, and 3.5.9.2, respectively.

b. The Reset/Load sequence shall write data into Control Storage proper until all addresses present have been written, (16,384 words maximum, 1024 word increments), and shall then write data into the Address Table until all addresses present have been written (1024 words maximum, 256 word increments). The sizes of Control Storage proper and the Address Table may be selected for maximums of 4096 words and 256 words, respectively, by means of the Select CS Minimum control as described in 3.10.4.19.

3.5.7.5 Reset/Load Termination

Termination of the Reset/Load shall be accomplished by the clearing of the Reset/Load Flip/Flop, through one of the following means.

a. Generation of the End Out Signal as described in 3.5.8.7, with the Load Select Switch in the Primary position.

b. Generation of the End In signal as described in 3.5.9.5, with the Load Select Switch in the Alternate position.

c. The occurrence of a System Reset.

3.5.8 Primary Loader

The Primary Loader Logic shall utilize the following signals to interface the ALU and the Integrated File Adapter (IFA), in order to accomplish a Control Storage (including the Address Table) Reset/Load.

3.5.8.1 Reset/Load Initiate

A level from the loader logic which, in the high state, shall indicate a Reset/Load is to be initiated from the source specified by the state of the Disc Source signal described in 3.5.8.3.

The leading edge and trailing edge of this signal shall be generated by the setting and clearing, respectively, of the Reset/Load Flip/Flop described in 3.5.7.3.

3.5.8.2 Primary Data Strobe

A pulse from the IFA which, in the low state, shall indicate that 16 bits of input Data are available on the Primary Source Data Lines described in 3.5.8.8.

This pulse shall initiate a sequence which clears the Console Data Register, strobes the Primary Source Data Lines into the Console Data Register, and generates a Console Run signal. This Run signal shall be in parallel with and shall perform the same function as, the Console Run Control described in 3.10.3.10.

See Figure 8 for timing relationships.

3.5.8.3 Primary Source

A level from the Loader Logic which, in the high state, shall indicate that the Primary Load Source is to be used for the Reset/Load.

This level shall be generated by the Load Select switch described in 3.10.2.5.

3.5.8.4 Maintenance Out

A level from the Loader logic which, in the high state, indicates the Console is being operated in Maintenance Mode.

This signal shall be generated by the Maintenance Mode Switch described in 3.10.4.1.

3.5.8.5 Restart Reset/Load

A 50 n/s minimum width pulse from the IFA which, in the low state, shall indicate that a burst check error has been detected during a Control Storage Load, or shall indicate that a Control Storage Load Command has been issued to the IFA by means of a Micro-command routine.

This signal reinitiates the Reset/Load sequence if not disabled by means of the Restart Reset/Load Disable described in 3.5.8.6.

3.5.8.6 Restart Reset/Load Disable

A pulse from the IFA, which shall occur 50 n/s before and shall remain for 50 n/s after the Restart Reset/Load pulse for the purpose of disabling the restart operation.

This signal shall disable the Restart Reset/Load signal when a burst check error has been detected and the Console is in Maintenance Mode.

3.5.8.7 End Out

A pulse, from the Loader Logic which, in the high state, shall indicate that Control Storage, (Including the Address Table) has been completely loaded.

This signal shall assume the high state from 1 to 2 u/s after the next to the last word is transferred and shall return to the low state from 1 to 2 u/s after the last word is transferred. Minimum high state pulse width shall be 3 u/s

3.5.8.8 Primary Source Data Lines

Sixteen (16) levels from the IFA which, in the high state, shall provide Primary Source input data (true state) for the duration of the Primary Data Strobe signal.

See Figure 8 for timing relationships.

3.5.9 Alternate Loader

The Alternate Loader logic shall utilize the following signals to interface the CPU and the Integrated Card Reader Adapter, (ICRA), in order to accomplish a Control Storage (including the Address Table) Reset/Load.

NOTE: The Alternate Loader shall be capable of performing a Main Storage Load when the Console is in Maintenance Mode and the Console Operation Select switch is the MS-WR position, (See 3.10.3.11).

3.5.9.1 Alternate Reset/Load Initiate

See 3.5.8.1

3.5.9.2 Alternate Data Strobe

A pulse from the ICRA which, in the low state, shall indicate that 4 bits of input data are available on the Alternate Source Data Lines as described in 3.5.9.8.

This pulse shall initiate a sequence which clears the Console Data Register, strobes the Alternate Source Data Lines into the Console Data Register, and generates a Console Run signal. This Run signal shall be in parallel with, and shall perform the same function as, the Console Run control described in 3.10.3.10.

See Figure 8 for timing relationships.

3.5.9.3 Alternate Source

The Primary Source signal described in 3.5.8.3, in the low state, shall indicate that the Alternate Load source is to be used for the Reset/Load.

3.5.9.4 Maintenance Out

See 3.5.8.4.

3.5.9.5 End In

A 50 n/s minimum width pulse from the ICRA which, in the low state, shall indicate that the ICRA has completed its data transfer, (See 3.5.7.6, for Reset/Load Termination).

3.5.9.6 Nybl Zero

A pulse from the ICRA which, in the low state, shall indicate that the Alternate Source Data Lines correspond to the left-most 4 bits, (Nybl Zero), of a 16-bit word.

See Figure 8 for timing relationships.

3.5.9.7 Nybl Three

A pulse from the ICRA which, in the low state, shall indicate that the Alternate Source Data Lines correspond to the right-most 4 bits, (Nybl Three), of a 16-bit word.

See Figure 8 for timing relationships.

3.5.9.8 Alternate Source Data Lines

Four (4) levels from the ICRA which, in the high state shall provide Alternate Source input data (true state) for the duration of the Alternate Data Strobe signal. Each 4-bit input received on these lines shall be treated as a nybl and shall be assembled into a 16-bit word, working from left to right, in the Console Data Register.

See Figure 8 for timing relationships.

3.6 Main Storage

Main Storage facilities for the 7300 Processor shall be described by the appropriate documents listed in 2.1. Although Address, Data and Control signal conventions are only generally described herein, by 3.6.1 through 3.6.3, respectively, the CPU shall conform to the precise specifications as contained in the appropriate reference documents listed in 2.1.

3.6.1 Address

Address signals to Main Storage shall be provided by the CPU via the Basic Storage Protection Feature or the Relocation and Protection Feature, with the exception of item c, as follows:

a. Nineteen (19) Word Address signals shall be supplied to Main Storage.

b. Two (2) additional signals shall be supplied and shall be Byte Address related to the extent that their encoding shall provide full read reference, Byte 0 write reference (left-most), Byte 1 write reference (right-most), and full write reference designations to Main Storage.

c. Three (3) signals shall be supplied to Main Storage for the purpose of addressing the Register Set associated with the ECC Feature (Note: These signals shall bypass the Register Option and be directly supplied to Main Storage from the CPU).

3.6.2 Data

a. Sixteen (16) Data Signals shall be provided to Main Storage via the Register Option in the same manner previously described for the Address signals in 3.6.1. Two (2) additional signals shall be supplied directly from the ALU section of the CPU to Main Storage and shall be Data related to the extent that each shall provide odd horizontal parity designation for the associated Data byte.

b. Sixteen (16) Data signals shall be received directly from Main Storage by the ALU section of the CPU (D Fan-In Network). Two (2) additional signals shall be received from Main Storage and shall be Data related to the extent that, in the absence of the ECC Feature, each shall provide odd horizontal parity designation for the associated Data byte. As such, they shall be checked for validity by the CPU. (In the presence of the ECC Feature, these sixteen data signals shall provide the output from the ECC associated Register

Set when addressed by means of the signals described in 3.6.1, item c.).

3.6.3 Control

Control signals shall be exchanged between the CPU and Main Storage as follows:

a. A single Clock signal shall be supplied to Main Storage and shall provide the CPU timing reference for Main Storage operations.

b. A single Access Enable signal shall be supplied to Main Storage for the purpose of designating the need for a Main Storage reference on the part of the CPU.

c. A single Refresh signal shall be received from Main Storage for the purpose of allocating Null State major cycles within the CPU. Main Storage references shall not occur during major cycles allocated to the Null State.

d. A single Out of Range signal shall be received from Main Storage for the purpose of detecting Main Storage references on the part of the CPU to Main Storage Addresses not physically present within the 7300 Processor.

e. In the presence of the ECC Feature an associated signal shall be received from Main Storage such that horizontal parity checking of Main Storage data shall be disabled within the CPU and the ECC Error signal from Main Storage indicating an uncorrectable data error shall be enabled within the CPU.

3.7 Basic Timing

With respect to Multi-State capabilities, the basic timing of the CPU shall be performed as shown in Figure 4.

With respect to Single-State operations using consecutive major cycles, the basic timing departure from that shown in Figure 4 is described in 3.7.1, item b.

3.7.1 State Initialization

State initialization shall occur prior to every major cycle allocated to Processor States other than the Null State and shall occur under hardware control.

a. When Processor States 0 through 7 are allocated major cycles such that consecutive major cycles are not allocated to the same Processor State, initialization shall occur during minor cycles R0 and R1 in parallel with E6 and E7, respectively.

   R0 shall transfer the contents of the appropriate Pu Register from the Extended Register File, Group I to the Su Register.

   R1 shall access Control Store proper at the Control Store Address contained in Su. In addition, R1 shall transfer the contents of the appropriate F Register from the Extended Register File, Group I, to the common resource F Register, (Clocked at the beginning of minor cycle E0).

b. When Processor States 0 through 7 are allocated consecutive major cycles for the same Processor State, initialization shall occur during minor cycles E8 and E9, appended to the major cycle as illustrated in 3.1.1.

   Minor cycle R1 shall be suppressed and R0 shall be extended to occur in parallel with E6 as previously described in item a, as well as minor cycles E7 through E9. Minor cycles E8 and E9 shall occur, in that order, after E7 and prior to E0 for the purpose of implementing consecutive major cycles for the same Processor State, 0 through 7.

   Minor cycle E8 shall transfer the contents of the Pp Register to Su when the operation has not been suppressed as described in 3.8.12.5. Minor cycle E8 shall transfer the contents of the appropriate Pu Register from the Extended Register File, Group I, to the Su Register when the Pp Register has been suppressed as described in 3.8.12.5.

Minor cycle E9 shall access Control Store proper at the Control Store Address contained in Su. At the end of E9, a major cycle shall begin on minor cycle E0 with the execution of the Micro-command thus accessed, on the part of the appropriate Processor State, provided the associated Busy Flip/Flop has remained in the set state. When the associated Busy Flip/Flop is in the clear state during minor cycle E8, minor cycle E9 shall cause a Null State major cycle to begin on the following minor cycle E0.

c. For all major cycles allocated to the Console State for the purpose of performing operations under Micro-command control, major cycle R0 shall transfer an address constant to Su according to 3.5.2 and minor cycle R1 shall clear the common resource F Register in addition to accessing Control Store proper. R0 and R1 shall occur in parallel with E6 and E7, respectively, during the initialization of major cycles thus allocated to the Console State.

3.7.2 State Execution

Once initialized as described in 3.7.1, Processor States 0 through 7 and the Console State shall be capable of executing one Micro-command during each of the eight minor cycles beginning with E0 and continuing through E7. The actual number of Micro-commands executed during one major cycle shall depend on the nature of the Micro-commands themselves, up to a maximum of eight.

Note: As a result of the "Su+1" inputs to the Su and Pp Registers, (in conjunction with the compensation provided by the P_b, ("P buffer"), Register as required for the R0/R1 look-ahead utilization of the Su Register), Branch Micro-commands providing less than 14-bits of branch address shall have the anomalous characteristics as described in 3.8.11.

3.7.3 State Housekeeping

State housekeeping shall occur after every major cycle allocated to Processor States 0 through 7 under hardware control.

Housekeeping operations shall occur during minor cycles W0 and W1 in parallel with E0 and E1, respectively.

W0 shall transfer the contents of the Pp Register to the appropriate Pu Register within the Extended Register File, Group I, provided the transfer has not been suppressed as described in 3.8.12.5. The W0 operation shall update both the Arithmetic status (Bits 00 and 01) and the Control Store Address (Bits 02 through 15) portions of the appropriate Pu Register unless suppressed as described in 3.8.12.5 in which case the entire contents of the appropriate Pu Register shall be left unchanged, (including the "E" and "S" hardware controlled status bits as described in 3.2.2.2).

W1 shall appropriately update the associated F Register within the Extended Register File, Group I, provided the F Register was designated by one or more Micro-commands for the purpose of performing a write reference during the preceding major cycle.

NOTE: As a result of the W1 timing equivalence to minor cycle E1, in conjunction with the compensation provided by the F_b, ("F buffer"), Register as required for the E7 to E0 timing transition, the restricted addressability for F Register write references shall exist during minor cycle E0 as described in 3.8.2.4, item b.

3.8 Micro-command Repertoire

The Micro-command Repertoire shall consist of 65 basic Micro-commands. These 65 basic Micro-commands shall be grouped into 10 classes as described in 3.8.3 through 3.8.12.

Each of the basic 65 Micro-commands shall consist of 14-bit codes, arranged into a 16-bit format such that bit positions 09 and 10 are unused and always in the clear state.

Micro-commands shall be read from Control Storage proper and temporarily stored, i duplicate, by means of registers referred to as ul and Fu2 within the Timing/ Control section of the CPU. The duplicated Micro-commands thus contained in the Ful and Fu2 Registers are translated and executed, in parallel with the access for the next Micro-command, in an iterative fashion under hardware control.

3.8.1 Format

Micro-command formats are shown for each of the 65 basic Micro-commands in 3.8.3 through 3.8.12. However, as a result of the Micro-command modifications which are possible with respect to register number for Register File references, bit position for Skip operations and bit position for Immediate Operand entries, separate formats are described in 3.8.1.1 through 3.8.1.3 relative to these capabilities.

Micro-command modifications shall be based on the state of the bit positions of the right-most byte of the common resource F Register. The contents of this F Register shall be influenced by hardware control at the beginning of each major cycle to the extent described in 3.2.2.1.

3.8.1.1 Register Number

Micro-commands for which the register number may be modified shall have the following format, referred to as Format 1.

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
f				s_0	s_1	a	b	p	0	0	x				

a. The 4-bit "f" field (Bits 00 through 03) shall provide the fundamental function code.

b. The "s_0" and "s_1" designators (Bits 04 and 05, respectively) shall provide the sub-function code.

c. The "a" and "b" designators (Bits 06 and 07, respectively) shall determine the manner in which the register number is formed for the purpose of referencing the Register File:

When "a" and "b" are clear, the Basic Register File shall be referenced at the register number described by the "x" field (Bits 11 through 15) as defined in item f.

When "a" is set and "b" is clear the Basic Register File shall be referenced at the register number described by the "x" field after an "inclusive or" is performed between bits 13, 14, and 15 of the "x" field and bits 09, 10, and 11 of the common resource F Register.

When "a" is clear and "b" is set, the Basic Register File shall be referenced at the register number described by the "x" field after an "inclusive or" is performed between bits 13, 14 and 15 of the "x" field and bits 13, 14, and 15 of the common resource F Register.

When "a" and "b" are set, the Extended Register File shall be referenced at the register number described by the "x" field.

d. The "P" designator (bit 08) shall provide valid horizontal parity when the total number of bits in the set state is odd for the entire 16-bit contents of the Fu2 Register and applies to all Micro-commands.

e. The two unused bit positions (Bits 09 and 10) shall be in the clear state for all Micro-commands.

f. The 5-bit "x" field (Bits 11 through 15) shall provide the register number (1 of 32) for the purpose of referencing the Register File, subject to the "inclusive or" operations described in item c when "a" and "b" are unlike.

When the Processor State portion of the register number is applicable and Format 1 Micro-commands are executed in Normal Mode (not Boundary Crossing Mode), the Processor State portion of the register number shall be determined according to the Processor State executing the Micro-command. When Format 1 Micro-commands reference the Extended Register File, the Group I, II and III selection is made according to the state of bits 11, 12, 13 and 14 of the "X" field. When bits 11 through 14 are clear, Group I shall be selected. When bit 11 is clear and bits 12 through 14 are set, in any combination, Group II shall be selected. When bit 11 is set, Group III shall be selected.

When Format 1 Micro-commands are executed in Boundary Crossing Mode, the register number is determined as described in 3.2.3.7.

3.8.1.2 Bit Position Skip

Micro-commands for which a bit position skip may be modified shall have the following format, referred to as Format 2.

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
f				s_0	s_1	a	b	P	0	0	s_2	x			

a. The 4-bit "f" field (Bits 00 through 03) shall provide the fundamental function code for all Micro-commands.

b. The "s_0", "s_1", and "s_2" designators (Bits 04, 05 and 11, respectively) shall provide the sub-function code.

c. The "a" and "b" designators (Bits 06 and 07, respectively) shall determine the manner in which the bit position is formed for the purpose of selecting a bit within the Au Register as a Skip parameter.

When "a" and "b" are clear, the selected bit position in Au shall be described by the "x" field (Bits 12 through 15) as defined in item f.

When "a" is set and "b" is clear, the selected bit position in Au shall be described by the "x" field after an "inclusive or" is performed between the "x" field and bits 08 through 11 of the common resource F Register.

When "a" is clear and "b" is set, the selected bit position in Au shall be described by the "x" field after an "inclusive or" is performed between the "x" field and bits 12 through 15 of the common resource F Register.

When "a" and "b" are set, the selected bit position in Au shall be described by the "x" field after an "inclusive or" is performed between the "x" field, bits 08 through 11 of the common resource F Register, and bits 12 through 15 of the common resource F Register.

d. The "P" designator (Bit 08) shall provide valid horizontal parity when the total number of bits in the set state is odd for the entire 16-bit contents of the Fu2 Register and applies to all Micro-commands.

e. The two unused bit positions (Bits 09 and 10) shall be in the clear state for all Micro-comands.

f. The 4-bit "x" field (Bits 12 through 15) shall provide the bit position (1 of 16) to be selected within Au, subject to the "inclusive or" operations described in item c when "a" and/or "b" are set.

3.8.1.3 Bit Position Immediate Operand

Micro-commands for which a bit position Immediate Operand may be modified shall have the following format, referred to as Format 3.

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
f				s_0	s_1	a	b	P	0	0		x			

a. The 4-bit "f" field (Bits 00 through 03) shall provide the fundamental function code for all Micro-commands.

b. The "s_0" and "s_1" designators (Bits 04 and 05, respectively) shall provide the sub-function code.

c. The "a" and "b" designators (Bits 06 and 07, respectively) shall determine the manner in which the bit position is formed for the purpose of selecting a bit (or bits) within the Bu Register for Immediate Operand entry.

When "a" and "b" are clear, the selected bit position in Bu shall be described by the "x" field (Bits 12 through 15) as defined in item f.

When "a" is set and "b" is clear, the selected bit position in Bu shall be described by the "x" field after an "inclusive or" is performed between the "x" field and bits 08 through 11 of the common resource F Register.

When "a" is clear and "b' is set, the selected bit position in Bu shall be described by the "x" field after an "inclusive or" is performed between the "x" field and bits 12 through 15 of the common resource F Register.

When "a" and "b" are set, the bit position selected in the left-most byte position of the Bu Register shall correspond to the Processor State, 0 through 7, which performs the Micro-command. This "1 of 8" bit entry performed for the left-most byte position of the Bu Register shall be duplicated in the right most byte position of Bu. This operation shall occur independently of the value of the "x" field.

d. The "P" designator (Bit 08) shall provide valid horizontal parity when the total number of bits in the set state is odd for the entire 16-bit contents of the Fu2 Register and applies to all Micro-commands.

e. The two unused bit positions (Bits 09 and 10) shall be in the clear state for all Micro-commands. The undesignated bit position (Bit 11) shall have no effect on Micro-command execution except to the extent that it shall participate in the formation of valid horizontal parity as described in item d.

f. The 4-bit "x" field (Bits 12 through 15) shall provide the bit position (1 of 16) to be selected within Bu except when "a" and "b" are set and subject to the "inclusive or" operations described in item c when "a" and "b" are unlike.

3.8.2 Characteristics

With respect to each of the 65 basic Micro-commands, characteristics related to Mnemonic, Format, Blockpoint, Register File Addressability and Timing requirements are provided in Figure 9.

The significance of each of these characteristics is described in 3.8.2.1 through 3.8.2.4.

3.8.2.1 Mnemonics

Mnemonics shall consist of 3 or 4 alpha-numeric characters and are shown in Figure 9 in alpha-numeric order. Complementary operations are denoted by use of the special character, \.

3.8.2.2 Format

Formats 1, 2, and 3 as described in 3.8.1.1 through 3.8.1.3 are shown in Figure 9 for each of the 65 Micro-command Mnemonics as applicable.

3.8.2.3 Blockpoint

When the "multi-state" processing capabilities characteristic of the 7300 Processor are utilized, allowances must be made for the execution of Micro-commands in non-contiguous major cycles for each of the Processor States involved. All Micro-commands executed during the course of each major cycle shall not base their execution on the state of the common resource registers within the ALU except where the execution of previous Micro-commands within the same major cycle has influenced the state of such registers. Thus the first Micro-command executed in each major cycle shall make no assumptions whatsoever with respect to the contents of the common resource registers within the ALU whenever "multi-state" processing may have occurred, i.e. the previous major cycle was allocated to a different Processor State than the current major cycle.

A convention, using the Micro-commands shown in Figure 9 as Blockpoints, shall facilitate the coding of Micro-command sequences such that valid results shall be obtained during "multi-state" operations. Micro-commands designated as Blockpoints shall record the Control Storage Address of the next Micro-command in a register referred to as the Pp Register, in addition to performing the operations described in 3.8.3 through 3.8.12.

As previously described in 3.2.2.2, Micro-command execution for each major cycle allocated to Processor States 0 through 7 shall begin at the Control Storage Address designated by the contents of the associated Pu Register. Likewise, upon completion of each major cycle allocated to Processor States 0 through 7 the associated Pu Register shall be updated (written) to reflect the contents of the Pp Register (unless suppressed by execution of a CI01 or CI02 Micro-command). Thus, each major cycle allocated to Processor States 0 through 7 shall involve the execution of at least one Blockpoint Micro-command. Moreover, the Micro-commands following a Blockpoint Micro-command shall make no assumptions relative to the contents of the common resource registers in the ALU unless such Micro-commands are known to occur within the same major cycle as the last Blockpoint Micro-command. When the last Blockpoint occurs on a minor cycle other than E7 for any major cycle allocated to Processor States 0 through 7, the Micro-commands executed after the last Blockpoint shall be repeated during the next major cycle allocated to the associated Processor State.

3.8.2.4 Register File Addressability

For the purpose of performing read and write references to the Extended Register File, access shall be allowed to those registers and groups for the Micro-commands as shown in Figure 9.

The general addressability indications provided in Figure 9 apply to the associated Micro-commands when executed in Normal Mode only and are subject to specific constraints described in 3.2. Boundary Crossing Mode addressability is likewise described in 3.2.

a. Where addressability shall be provided for any Extended Register File group, addressability of the Basic Register File shall be possible for the same Micro-commands as shown in Figure 9.

b. Extended Register File, Group I addressability shall be indicated uniquely for the F and Pu Registers as shown in Figure 9.

Micro-commands for which F Register addressability shall be provided, should not occur for the purpose of performing write operations during minor cycle E0. Such operations shall not be hardware supported and may result in machine malfunction.

Micro-commands for which Pu Register addressability shall be provided shall reference the Address portion of the Pp Register and Arithmetic Status portion of the Su Register during read operations. Micro-commands for which Pu Register addressability shall be provided shall reference the applicable bit positions, in the Address portions only, of the Pp and Su Registers during write operations as specifically described in 3.8.4 and 3.8.11.

c. Extended Register File, Group II addressability shall be provided for those Micro-commands shown in Figure 9, subject to the constraints described in 3.2.3.

d. Extended Register File, Group III addressability shall be provided for those Micro-commands shown in Figure 9, subject to the constraints described in the associated documents listed in 2.1.

3.8.2.5 Timing

Micro-command execution times shall be provided by Figure 9 in terms of the number of minor cycles required in the best (minimum) and worst (maximum) cases.

In addition to the minimum, minor cycles shall be hardware inserted as required for the following conditions:

a. Additive Micro-commands SUM and DSUM and comparative Micro-commands CMP and CMU shall require one additional minor cycle when adder and comparator propagations, respectively, have not overlapped the execution of one or more previous Micro-commands, (Blockpoint shall be deferred until the second cycle when applicable.

b. Main Storage Related Micro-commands shall require an appropriate number of additional minor cycles when the minor cycle in which they are translated for execution does not correspond to the timing requirements of Main Storage.

c. Branch Micro-commands capable of referencing the applicable bit positions in the Address portion of the Su Register shall require one additional minor cycle when executed in any minor cycle other than E7. (FNJ, JMP, and AND, CLR, STA, STB when the Pu Register is designated).

d. Branch Micro-commands capable of referencing the applicable bit positions in the Address portion of the Pp Register only, shall require as many additional minor cycles as remain in the major cycle. (FRJ, FZJ with the contents of Au equal to zero, RNI1 and RNI2).

e. Control Micro-commands CI01, CI02, ROM and SYNC shall require as many additional minor cycles as remain in the major cycle.

NOTE: With respect to Micro-command control and timing, when asynchronous signals are read, resolve time must be allowed before any actions dependent on the state of such signals are taken. When input signals are subject to change during the minor cycle in which they are read, settling time of 200 n/s must be allowed. For example, if an LAW Micro-command designating the Extended Register File Group II CA Register is performed and any Skip Micro-command (or a Jump Micro-command such as STA designating Pu) is performed within 200 n/s, such Micro-command may result in machine malfunction. This resolve time requirement must be accommodated under Micro-command control and in the case of this example could consist of, immediately following the LAW, two NØPs or an STA and LAW combination specifying an otherwise unused register within the Register File or, an SHF designating a shift of zero, etc. Such precautions are particularly applicable to the Extended Register File, Group III facilities.

3.8.3 Register File Read Micro-commands

The Micro-commands in this class shall provide the means for performing Register File read references which are unrelated to Main Storage operations.

3.8.3.1 Load Au Word

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
LAW	1	1	0	1	0	0	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the output from the Register File to the Au Register with the register number for the read reference designated according to 3.8.1.1.

3.8.3.2 Load Au Complement

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
LAW\	1	1	0	1	0	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the 1's complement of the output from the Register File to the Au Register with the register number for the read reference designated according to 3.8.1.1. In addition, the Force Carry Register shall be set.

3.8.3.3 Load Bu Word

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
LBW	0	1	1	0	0	0	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the output from the Register File to the Bu Register with the register number for the read reference designated according to 3.8.1.1. In addition, the Force Carry Register shall be cleared.

3.8.3.4 Load Bu Complement

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
LBW\	0	1	1	0	0	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the 1's complement of the output of the Register File to the Bu Register with the register number for the read reference designated according to 3.8.1. . In addition, the Force Carry Register shall be set.

3.8.3.5 Load Au and Bu

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
LAB	1	1	0	1	1	0	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the output of the Register File to both the Au and Bu Registers with the register number for the read reference designated according to 3.8.1.1. In addition, the Force Carry Register shall be cleared.

3.8.3.6 Clear Au

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
CLA	1	1	0	1	1	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the output of the Register file to the Bu Register with the register number for the read reference designated according to 3.8.1.1. In addition, the Au Register shall be cleared and the Force Carry Register shall be set.

3.8.3.7 Load Bu Link

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
LBL	0	1	1	1	1	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the output of the Register File to the Bu Register with the register number for the read reference designated according to 3.8.1.1. In addition, the state of the Link status bit shall be transferred from the Arithmetic Status portion of Su to the Force Carry Register.

3.8.4 Register File Write Micro-commands.

The Micro-commands in this class shall provide the means for performing Register File write references which are unrelated to Main Storage operations.

NOTE: The CLR, STA, STB and AND Micro-commands shall effect a Branch operation when the Pu Register is designated.

3.8.4.1 Clear Contents of Register (Designated by x)

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
CLR	0	0	0	1	0	0	a	b	P	0	0	x				

This Format 1 Micro-command shall clear the contents of the Register File at the register number designated according to 3.8.1.1. (See 3.8.2.4, item b restriction).

3.8.4.2 Store Au

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
STA	0	0	0	1	0	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the contents of the Au Register to the Register File with the register number for the write reference designated according to 3.8.1.1.

3.8.4.3 Store Bu

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
STB	0	0	0	1	1	0	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the contents of the Bu Register to the Register File with register number for the write reference designated according to 3.8.1.1.

3.8.4.4 Logical Product, Au and Bu

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
AND	0	0	0	1	1	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the logical product of the contents of the Au and Bu Registers to the Register File with the register number for the write reference designated according to 3.8.1.1.

The logical product operation shall be performed for each bit position of Au and Bu Registers according to the following truth table.

Au	Bu	Logical Product
0	0	0
0	1	0
1	0	0
1	1	1

3.8.4.5 Inclusive Or, Au and Bu

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
IOR	0	1	0	0	1	0	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the inclusive or of the contents of the Au and Bu Registers to the Register File with the register number for the write reference designated according to 3.8.1.1.

The inclusive or operation shall be performed for each bit position of the Au and Bu Registers according to the following truth table.

Au	Bu	Inclusive Or
0	0	0
0	1	1
1	0	1
1	1	1

3.8.4.6 Exclusive Or, Au and Bu

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
EOR	0	1	0	0	1	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the exclusive or of the contents of the Au and Bu Registers to the Register File with the register number for the write reference designated according to 3.8.1.1.

The exclusive or operation shall be performed for each bit position of the Au and Bu Registers according to the following truth table.

Au	Bu	Exclusive Or
0	0	0
0	1	1
1	0	1
1	1	0

3.8.4.7 Sum, Au and Bu

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SUM	0	0	1	0	0	0	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the sum of the Au (16 bits), Bu (16 bits) and Force Carry (1 bit, right justified) Registers to the Register File with the register number for the write reference designated according to 3.8.1.1.

In addition, the Overflow and Link status conditions relative to the current sum shall be transferred to the Arithmetic status portion of Su provided the left-most byte contained in the common resource F Register is not equal to 50, 51, 52, or 53 in hexadecimal notation and provided the Au or Bu Registers have been cleared, set, or clocked since the last execution of a DIG or CORC Micro-command.

3.8.4.8 Decimal Sum, Au and Bu

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
DSUM	0	0	1	0	0	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the sum of the Au (16 bits), Bu (16 bits) and Force Carry (1 bit, right justified) Registers to the Register File with the register number for the write reference designated according to 3.8.1.1. The carry outputs from each of the adder groups (4-bit nybls) shall be transferred to the Inner Carry Register.

In addition, the Overflow and Link status conditions relative to the current Sum shall be transferred to the Arithmetic status portion of Su provided the Au or Bu Registers have been cleared, set, or clocked since the last execution of a DIG or CORC Micro-command.

NOTE: The Link status bit shall be derived at the carry output from the right-most byte of the adder, instead of the left-most byte of the adder, whenever the left-most byte of the common resource F Register is equal to 50, 51, 52 or 53 in hexadecimal notation.

3.8.4.9 Sign and Magnitude Compare

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
CMP	0	0	1	0	1	0	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the algebraic (signed), and logical (unsigned), compare status, relative to the contents of the Au and Bu Registers, to the Register File where the register number for the write reference shall be designated according to 3.8.1.1.

When the Basic Register File is designated, only bits 00 through 07 of the appropriate register shall be written, according to the left-most byte position of the following table.

When the Extended Register File is designated and addressability of the designated register is specifically provided, the full 16-bit compare status shall be provided as follows:

ALGEBRAIC	LOGICAL	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
(A) > (B)	(A) > (B)	0	1	0	0	0	1	0	0	1	→						1
(A) > (B)	(A) < (B)	0	1	0	0	0	0	1	0	1	→						1
(A) < (B)	(A) < (B)	0	0	1	0	0	0	1	0	1	→						1
(A) < (B)	(A) > (B)	0	0	1	0	0	1	0	0	1	→						1
(A) = (B)		0	0	0	1	0	0	0	1	1	→						1

3.8.4.10 Magnitude Compare

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
CMU	0	0	1	0	1	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the logical (unsigned) compare status, relative to the contents of the Au and Bu Registers, to the Register File where the register number for the write reference shall be designated according to 3.8.1.1.

When the Basic Register File is designated, only bits 00 through 07 of the appropriate register shall be written according to the left-most byte position of the following table.

When the Extended Register is designated and addressability of the designated register is specifically provided, the full 16-bit compare status shall be provided as follows:

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
(Au) > (Bu)	0	1	0	0	0	1	0	0	1	→	→	→	→	→	→	1
(Au) < (Bu)	0	0	1	0	0	0	1	0	1	→	→	→	→	→	→	1
(Au) = (Bu)	0	0	0	1	0	0	0	1	1	→	→	→	→	→	→	1

3.8.5 Register File Read, Main Storage Related Micro-commands.

The Micro-commands in this class shall provide the means for performing Register File read references which are related to, or may be related to, Main Storage (or Register Option) operations. Micro-commands LS1, LSF, LS2 and LSE shall be unconditionally related to Main Storage (or Register Option) operations. The LDW, LDW\, and LDB Micro-commands shall be Main Storage (or Register Option) related only when they are executed during minor cycle E1 immediately following the execution of an LS1, LSF, LS2 or LSE Micro-command at minor cycle E0. All other Micro-commands in this class shall be Main Storage (or Register Option) related when they occur after, but within the same major cycle as LS1, LSF, LS2 or LSE Micro-commands executed for the purpose of performing Main Storage (or Register Option) read operations.

The selection of an input to the D Fan-In Network within the ALU shall be conditioned by the Micro-commands within this class in the following manner:

a. During Main Storage Read operations, the data from Main Storage shall be selected at the D Fan-In Network from minor cycle E4 through minor cycle E7.

b. During Register Option Read operations, the data from the Register Option shall be selected at the D Fan-In Network from minor cycle E4 through minor cycle E7.

c. For the purpose of making D Fan-In Network selection only, Register Option Read operations which specify the Register set associated with the ECC Feature shall be treated as Main Storage Read operations.

d. During all minor cycles other than those described in items a, b, and c, the D Register shall be selected at the D Fan-In Network.

3.8.5.1 Load S

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
LS1	0	0	1	1	0	0	a	b	P	0	0	x				
LSF	0	0	1	1	0	1	a	b	P	0	0	x				
LS2	0	0	1	1	1	0	a	b	P	0	0	x				
LSE	0	0	1	1	1	1	a	b	P	0	0	x				

These Format 1 Micro-commands shall transfer the output from the Register File to the S Register, when executed on minor cycle E0, with the register number for the Register File read reference designated according to 3.8.1.1.

a. When executed during minor cycle E0 on the part of Processor States 0 through 7 with bits 11, 12, 13 and 14 set (register number 1E or 1F) or when executed during minor cycle E0 on the part of the Console State with the Console Operation Select switch in the RO-RD or RO-WR position (See 3.10.3.11), these Micro-commands shall cause hardware interpretation of the remainder of the appropriate major cycle to be associated with a Register Option reference.

b. When executed during minor cycle E0 on the part of Processor States 0 through 7 with bits 11, 12, 13 or 14 clear in any combination (not register number 1E or 1F) or when executed during minor cycle E0 on the part of the Console State with the Console Mode Select switch in any applicable position other than RO-RD or RO-WR (See 3.10.3.11), these Micro-commands shall cause hardware interpretation of the remainder of the appropriate major cycle to be associated with a Main Storage reference.

c. When executed during minor cycle E0, in the presence of the Basic Storage Protection Feature, the Relocation and Protection Feature or the ECC Feature, these Micro-commands shall require an additional minor cycle referred to as E0'. When executed during minor cycle E0, in the presence of the Basic Storage Protection and ECC Features or the Relocation and Protection and ECC Features, these Micro-commands shall require two additional minor cycles referred to as E0' and E0". Minor cycles E0' and E0" shall be hardware inserted.

d. When executed during any minor cycle other than E0, the contents of the S Register shall not be affected by these Micro-commands. Moreover, the nature of each major cycle with respect to its association with Register Option or Main Storage references shall be hardware interpreted during minor cycle E0 only and shall not be altered by the execution of these Micro-commands during minor cycles other than E0. When executed during any minor cycle other than E0, the associated Load S Micro-command shall be held in the Fu1 and Fu2 Registers for the remainder of the major cycle. Thus, each Load S Micro-command occurring on minor cycles other than E0, must be immediately preceded by a Blockpoint Micro-command for Processor States 0 through 7.

These Format 1, Load S Micro-commands shall transfer the output of the Register File to the Au Register, regardless of the minor cycle in which they are executed, with the register number of the Register File Read reference designated according to 3.8.1.1. Likewise, the Bu and Force Carry Registers shall be affected according to the following:

e. The LS1 Micro-command shall cause 0000_{16} to be transferred to the Bu Register and the Force Carry Register shall be set.

f. The LSF Micro-command shall cause $FFFF_{16}$ to be transferred to the Bu Register and the Force Carry Register shall be cleared.

g. The LS2 Micro-command shall cause 0001_{16} to be transferred to the Bu Register and the Force Carry Register shall be set.

h. The LSE Micro-command shall cause $FFFE_{16}$ to be transferred to the Bu Register and the Force Carry Register shall be cleared.

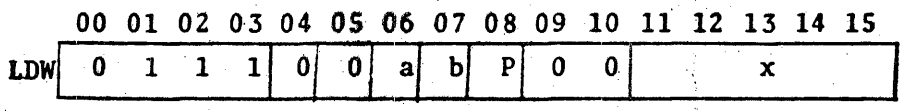
In the presence of the Relocation and Protection Feature, Load S Micro-commands executed during minor cycle E0 shall result in the transfer of the Segment Tag, associated with the designated register number, to be transferred to the left-most 4-bit extension of the S Register as contained within the Relocation and Protection Feature.

Although the Load S Micro-commands shall be capable of execution in a single minor cycle, E0, as reflected by Figure 9, the following restrictions shall apply:

i. In the presence of the Basic Storage Protection or the Relocation and Protection Features, the Load S Micro-commands shall require 2 minor cycles, the second consisting of a special hardware inserted cycle referred to as E0'.

j. In the presence of one of the features described above and in the additional presence of the ECC Feature, the Load S Micro-commands shall require 3 minor cycles, the second and third consisting of special hardware inserted cycles referred to as E0' and E0", respectively.

3.8.5.2 Load D Word



This Format 1 Micro-command shall transfer the output from the Register File to the D Register with the register number for the Register File read reference designated according to 3.8.1.1.

When executed during minor cycle E1, immediately following an LS1, LSF, LS2 or LSE Micro-command at minor cycle E0, this Micro-command shall result in a Main Storage or Register Option write reference involving a full transfer of the D Register output. In such cases, alteration of the contents of the D Register by means of Micro-commands during minor cycles E2 through E7, may result in machine malfunction. The word locations of the write reference within Main Storage, or within the Register Option, shall be designated by the contents of the S Register (Bit 15 irrelevant except for Breakpoint) and shall be subject to appropriate hardware validity checks on the part of the Basic Storage Protection or Relocation and Protection Features. Write references thus performed shall involve 16 data bits when validly addressed.

3.8.5.3 Load D Complement

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
LDW\	0	1	1	1	0	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the 1's complement of the output from the Register File to the D Register with the register number for the Register File read reference designated according to 3.8.1.1.

For a description of the relationship of this Micro-command to Main Storage and Register Option write references see the comments in 3.8.5.2.

3.8.5.4 Load D Byte

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
LDB	0	1	1	1	1	0	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the output from the Register File to the D Register with the register number for the Register File read reference designated according to 3.8.1.1.

When executed during minor cycle E1, immediately following an LS1, LSF, LS2, or LSE Micro-command at minor cycle E0, this Micro-command shall result in a Main Storage write reference involving a partial transfer of the D Register output for which the right-most byte shall be duplicated in the left-most byte position, (the D Register output to the D Fan-In Network shall not be affected). In such cases, alteration of the contents of the D Register by means of Micro-commands during minor cycles E2 through E7, may result in machine malfunction. The byte location of the write reference within Main Storage shall be designated by the contents of the S Register and shall be subject to appropriate hardware validity checks on the part of the Basic Storage Protection or Relocation and Protection Features. Write references thus performed shall involve the transfer of only the left-most data byte where bit 15 of the S Register is clear or the transfer of only the right-most data byte where bit 15 of the S Register is set, when validly addressed.

3.8.5.5 D To Au, True

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
DTA	1	1	0	0	0	0	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the output from the Register File to the Bu Register with the register number for the Register File read reference designated according to 3.8.1.1. In addition, this Micro-command shall transfer the output from the D Fan-In Network to the Au Register and shall clear the Force Carry Register.

When initially translated on minor cycle E1, E2, or E3 during any major cycle in which a Main Storage or Register Option read reference is performed, this Micro-command shall be held in the Fu1 and Fu2 Registers and repeatedly executed during each minor cycle up to and including E4, under hardware control.

3.8.5.6 D to Au, Complement

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
DTA\	1	1	0	0	0	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the 1's complement of the output from the Register File to the Bu Register with the register number for the Register File read reference designated according to 3.8.1.1. In addition, this Micro-command shall transfer the output from the D Fan-In Network to the Au Register and shall set the Force Carry Register.

During Main Storage and Register Option read references, hardware controlled timing constraints shall be exercised as described in 3.8.5.5.

3.8.5.7 Index

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
IDX	1	1	0	0	1	0	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the output from the Register File to the Bu Register provided the resultant register number for the Register File read reference does not have the 3 right-most bits (13, 14 and 15) in the clear state when designated according to 3.8.1.1.

This Micro-command shall simply clear the Bu Register provided the resultant register number for the Register File read reference has the 3 right-most bits (13, 14 and 15) in the clear state when designated according to 3.8.1.1.

In addition, this Micro-command shall unconditionally transfer the output of the D Fan-In Network to the Au Register and shall clear the Force Carry Register.

During Main Storage and Register Option read references, hardware controlled timing constraints shall be exercised as described in 3.8.5.5.

In the presence of the Relocation and Protection Feature, the IDX Micro-command shall also serve as the implicit Micro-command control mechanism for dynamic Segment Tag write references. Each IDX Micro-command shall allow the next Register File write reference, performed under Micro-command control, to occur such that the associated Segment Tag shall also be written. The Segment Tag value so written shall correspond to the Segment Tag value read during the last LS1, LSF, LS2, or LSE Micro-command, whenever the associated IDX Micro-command simply cleared the Bu Register. Alternatively, the Segment Tag value so written shall correspond to the Segment Tag value read during the associated IDX Micro-command whenever this associated IDX Micro-command performed a transfer of the Register File output to the Bu Register.

3.8.5.8 D False to Au

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
DFA	1	1	0	0	1	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the output of the Register File to the Bu Register with the register number for the Register File read reference designated according to 3.8.1.1.

In addition the 1's complement of the output from the D Fan-In Network shall be transferred to the Au Register and the Force Carry Register shall be set.

During Main Storage and Register Option read references, hardware controlled timing constraints shall be exercised as described in 3.8.5.5.

3.8.6 Register File Write, Main Storage Related Micro-commands.

The Micro-commands within this class shall provide the means for performing Register File write references which may be related to Main Storage or Register Option read operations.

The Micro-commands within this class shall be Main Storage or Register Option related when they occur after, but in the same major cycle as LS1, LSF, LS2, or LSF Micro-commands which are executed for the purpose of performing Main Storage or Register Option read operations as defined in 3.8.5.1 through 3.8.5.4.

When initially translated on minor cycle E1, E2, E3 or E4 during any major cycle in which a Main Storage or Register Option read reference is performed, these Micro-commands shall be held in the Fu1 and Fu2 Registers and repeatedly executed during each minor cycle up to and including E5, under hardware control.

3.8.6.1 Store D Word

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SDW	0	1	0	0	0	0	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the output of the D Fan-In Network to the Register File with the register number for the Register File write reference designated according to 3.8.1.1.

3.8.6.2 Store D Byte

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SDB	0	1	0	0	0	1	a	b	P	0	0	x				

This Format 1 Micro-command shall transfer the right-most byte or left-most byte from the output of the D Fan-In Network (as determined by the state of bit 15 of the S Register) to the Register File in the right-most byte position, along with zeroes in the left-most byte position. The register number for the Register File write reference shall be determined according to 3.8.1.1.

When bit 15 of the S Register is in the clear state, the left-most byte of the D Fan-Out Network shall be selected at the right-most byte input to the Register File and zeroes at the left-most byte input to the Register File.

When bit 15 of the S Register is in the set state, the right-most byte of the D Fan-Out Network shall be selected at the right-most byte input to the Register File and zeroes at the left-most byte input to the Register File.

3.8.7 Immediate Operand Micro-commands.

The Micro-commands within this class shall provide the means for transferring immediate operands to the Bu-Register. These immediate operands shall be contained within the Micro-commands themselves, with the exception of CORC and special cases of the LBB and LBB\ Micro-commands.

Undesignated bit positions within these Micro-commands shall have no effect on Micro-command execution except to the extent that they shall participate in the formation of valid parity.

3.8.7.1 Enter Bu Upper

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
EBU	1	0	1	0	N_0				P	0	0		N_1			

The N_0/N_1 fields of this Micro-command shall be transferred to the left-most byte position of the Bu Register. The right-most byte position of the Bu Register shall remain unchanged.

3.8.7.2 Enter Bu Lower

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
EBL	1	0	1	1	N_0				P	0	0		N_1			

The N_0/N_1 fields of this Micro-command shall be transferred to the right-most byte position of the Bu Register. In addition, the left-most byte position of the Bu Register shall be cleared.

3.8.7.3 Load Bu Bit

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
LBB	0	1	1	0	1	0	a	b	P	0	0		x			

This Format 3 Micro-command shall transfer a 16-bit immediate operand to the Bu Register.

When the "a" and "b" designators are not set, the 16-bit immediate operand shall consist of a single bit in the set state with the remaining 15 bits in the clear state. The bit position to be set shall be designated according to 3.8.1.3.

When the "a" and "b" designators are set, the 16-bit operand shall consist of two bits in the set state, one in each byte position, with the remaining 14 bits in the clear state. The left-most bit position to be set shall correspond to the Processor State, 0 through 7, in which the Micro-command is executed and the left-most byte shall be duplicated in the right-most byte position as described in 3.8.1.3.

In addition, the Force Carry Register shall be cleared.

3.8.7.4 Load Bu Bit Complement

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
LBB\	0	1	1	0	1	1	a	b	P	0	0		x			

This Format 3 Micro-command shall transfer a 16-bit immediate operand to the Bu Register.

When the "a" and "b" designators are not set, the 16-bit immediate operand shall consist of a single bit in the clear state with the remaining 15 bits in the set state. The bit position to be cleared shall be designated according to 3.8.1.3.

When the "a" and "b" designators are set, the 16-bit operand shall consist of two bits in the clear state, one in each byte position, with the remaining 14-bits in the set state. The left-most bit position to be cleared shall correspond to the Processor State, 0 through 7, in which the Micro-command is executed and the left-most byte shall be duplicated in the right-most byte position as described in 3.8.1.3.

In addition, the Force Carry Register shall be set.

3.8.7.5 Digit Duplication

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
DIG	1	1	1	1	1	0			P	0	0		x			

The "x" field of this Micro-command shall be transferred to each nybl (4-bit group) position of the Bu Register. In addition, the Force Carry Register shall be cleared.

Execution of this Micro-command shall inhibit the group carry mechanisms within the adder such that each 4-bit nybl may be independently added with group carry inputs in the clear state. Likewise, the clocking of the Overflow and Link conditions within the Arithmetic portion of the Su Register shall be inhibited by the execution of this Micro-command. These disables shall remain in effect until the Au or Bu Registers are cleared, set or clocked by Micro-commands other than DIG and CORC.

3.8.7.6 Correct Code

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
CORC	1	1	1	1	1	1			P	0	0					

This Micro-command shall transfer a 16-bit immediate operand to the Bu Register where the value of each nybl (4-bit group) shall be independently determined by the state of the associated bit position in the Inner Carry Register.

Where the bit positions in the Inner Carry Register are set, the associated nybls shall have the value of 3 in hexadecimal notation.

Where the bit positions in the Inner Carry Register are clear, the associated nybls shall have the value of D in hexadecimal notation.

In addition, the Force Carry Register shall be cleared.

Execution of this Micro-command shall inhibit the group carry mechanisms within the adder such that each 4-bit nybl may be independently added with group carry inputs in the clear state. Likewise, the clocking of the Overflow and Link conditions within the Arithmetic portion of the Su Register shall be inhibited by the execution of this Micro-command. These disables shall remain in effect until the Au or Bu Registers are cleared, set or clocked by Micro-commands other than DIG and CORC.

3.8.8 Shift Micro-commands

The Micro-commands within this class shall provide the means for left shifting the contents of the Au/Bu Registers. Shift counts of 4 bits shall be Micro-command designated in true or 2's complement form, for shifts from 0 to 15_{10} binary places. Bits shifted from the Au Register shall be end-off, (lost). Bits from the Bu Register shall be shifted into the Au Register with zeroes inserted into the right-most bit positions of the Bu Register.

Undesignated bit positions within these Micro-commands shall have no effect on Micro-command execution except to the extent that they shall participate in the formation of valid parity.

3.8.8.1 Shift Left

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SHF	1	1	1	0	0	0			P	0	0	0	x			

This Micro-command shall shift the contents of the Au/Bu Registers left the number of bit positions designated by the "x" field.

3.8.8.2 Shift Right

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SHR	1	1	1	0	0	1			P	0	0	0	x			

This Micro-command shall shift the contents of the Au/Bu Registers left the number of bit positions designated by the 2's complement of the "x" field.

3.8.8.3 Left Shift (Dependent Count).

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
DLS	1	1	1	0	1	0			P	0	0	0				

This Micro-command shall shift the contents of the Au/Bu Registers left the number of bit positions designated by the shift count.

The shift count shall be obtained from bit positions 08 through 11 of the common resource F Register when bit position 01 of this common resource F Register is set.

The shift count shall be obtained from the output of the D Fan-In Network in the right-most bit positions (12 thru 15) when bit position 01 of the common resource F Register is clear. During major cycles which perform a Main Storage or Register Option read reference, the selection of the input to the D Fan-In Network shall change from the D Register to the Main Storage data or Register Option data inputs, respectively, during minor cycle E4. Thus DLS Micro-commands which obtain the shift count under these conditions, shall provide unpredictable results when executed during minor cycles E4/E5.

3.8.8.4 Right Shift (Dependent Count)

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
DRS	1	1	1	0	1	1			P	0	0	0				

This Micro-command shall shift the contents of the Au/Bu Registers left the number of bit positions designated by the 2's complement of the shift count.

The shift count shall be obtained in the same manner as previously described for the DLS Micro-command in 3.8.8.3.

3.8.9 Bit Sense Micro-commands.

The Micro-commands within this class shall provide the means for scanning the contents of the Au Register, from left to right, for the purpose of detecting the first bit position in the set or cleared state as specified by the associated Micro-command. Bit positions thus detected shall be cleared or set within the Au Register as specified by the SR1 and SS0 Micro-commands, respectively. A value corresponding to the bit position detected, 00 through 15_{10}, shall be added to the contents of the Bu Register. When the entire Au Register is scanned without detection of a bit in the specified state, 16_{10} shall be added to the contents of the Bu Register.

Undesignated bit positions within these Micro-commands shall not affect Micro-command execution except to the extent that they shall participate in the formation of valid parity.

3.8.9.1 Sense for Zero

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SR0	1	1	1	0	0	0			P	0	0	1				

This Micro-command shall scan the Au Register for detection of the first bit position in the clear state, and shall increase the contents of the Bu Register according to the result of the scan.

The contents of the Au Register shall remain unchanged.

3.8.9.2 Sense for One

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SSI	1	1	1	0	0	1			P			1				

This Micro-command shall scan the Au Register for the detection of the first bit position in the set state and shall increase the contents of the Bu Register according to the results of the scan.

The contents of the Au shall remain unchanged.

3.8.9.3 Sense and Set for Zero

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SS0	1	1	1	0	1	0			P	0	0	1				

This Micro-command shall scan the Au Register for detection of the first bit position in the clear state and shall increase the contents of the Bu Register according to the results of the scan.

The Au Register shall be set in the first bit position detected in the clear state when the contents of the Au Register are not equal to $FFFF_{16}$.

3.8.9.4 Sense and Reset for One

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SR1	1	1	1	0	1	1			P			1				

This Micro-command shall scan the Au Register for the detection of the first bit position in the set state and shall increase the contents of the Bu Register according to the results of the scan.

The Au Register shall be cleared in the first bit position detected in the set state when the contents of the Au Register are not equal to 0000_{16}.

3.8.10 Skip Micro-commands

The Micro-commands within this class shall provide the means for skipping the execution of the next successive Micro-command when the specified conditions within the Au Register are met. These Micro-commands shall require one minor cycle for translation and an additional minor cycle to accomplish the skipping of the next successive Micro-command when the specified conditions are met. Skip Micro-commands for which the specified conditions are met as initially translated during minor cycle E7, shall skip the next successive Micro-command during minor cycle E0 of the next appropriately allocated major cycle.

NOTE: When the contents of the Au or Bu Registers are logically ambiguous as a result of transferring asynchronous signals into them, the execution of Skip Micro-commands without an allowance for resolve time may result in machine malfunction in the form of undefined and unpredictable Micro-command execution. See 3.8.2.5.

Undesignated bit positions within these Micro-commands shall have no effect on Micro-command execution except to the extent that they shall participate in the formation of valid parity.

3.8.10.1 Skip if Au is Zero

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SKZ	0	1	0	1	0	0			P	0	0	0				

This Micro-command shall skip the execution of the next successive Micro-command when the contents of the Au Register are equal to 0000_{16}.

3.8.10.2 Skip if Au is Non-Zero

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SKN	0	1	0	1	0	1			P	0	0	0				

This Micro-command shall skip the execution of the next successive Micro-command when the contents of the Au Register are not equal to 0000_{16}.

3.8.10.3 Skip if Au Bit is a One.

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SKB	0	1	0	1	1	0	a	b	P	0	0	0	x			

This Format 2 Micro-command shall skip the execution of the next successive Micro-command when the content of the Au Register is in the set state at the bit position designated according to 3.8.1.2.

3.8.10.4 Skip if Au Bit is a Zero.

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SKB	0	1	0	1	1	1	a	b	P	0	0	0	x			

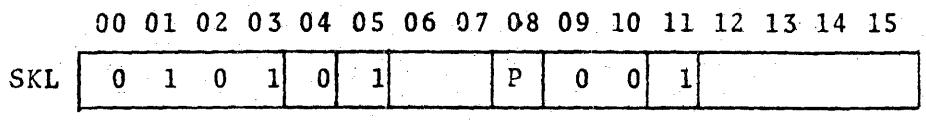
This Format 2 Micro-command shall skip the execution of the next successive Micro-command when the content of the Au Register is in the clear state at the bit position designated according to 3.8.1.2.

3.8.10.5 Skip if Au > Bu

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SKG	0	1	0	1	0	0			P	0	0	1				

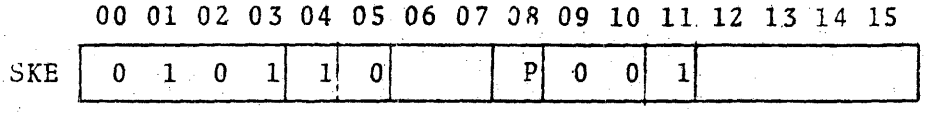
This Micro-command shall skip the execution of the next successive Micro-command when the contents of the Au Register are logically (unsigned) greater than the contents of the Bu Register.

3.8.10.6 Skip if Au < Bu



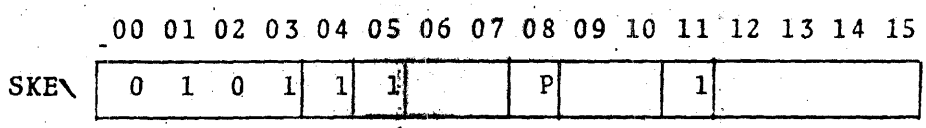
This Micro-command shall skip the execution of the next successive Micro-command when the contents of the Au Register are logically (unsigned) less than the contents of the Bu Register.

3.8.10.7 Skip if Au = Bu



This Micro-command shall skip the execution of the next successive Micro-command when the contents of the Au Register are equal to the contents of the Bu Register, bit-for-bit.

3.8.10.8 Skip if Au ≠ Bu



This Micro-command shall skip the execution of the next Micro-command when the contents of the Au Register are not equal to the contents of the Bu Register, bit-for-bit.

3.8.11 Branch Micro-commands

In addition to the CLR, STA, STB and AND Micro-commands which shall effect a Branch operation when the Pu Register is designated as described in 3.8.4, the six Micro-commands in this class shall explicitly provide the means for performing branch operations.

As opposed to the implicit Micro-commands previously mentioned and described in 3.8.4, the explicit Micro-commands in this class shall be capable of only partial write references to the right-most address portions of the Su and Pp Registers as follows:

a. The JMP Micro-command shall write only Bits 08 through 15 of the Su and/or Pp Registers. Bits 02 through 07 shall be under hardware control and shall be incremented by one when JMP Micro-commands occur at Control Storage Addresses $XXFF_{16}$. Likewise, bits 02 through 07 shall be incremented by one when JMP Micro-commands occur at Control Storage Addresses $XXFE_{16}$ during any minor cycles other than E6 and/or E7.

b. The FNJ, FRJ, FZJ, RNI1 and RNI2 Micro-commands shall write only Bits 04 through 15 of the Su and/or Pp Registers. Bits 02 and 03 shall be under hardware control and shall be incremented by one when these Micro-commands occur at Control Storage Addresses $XFFF_{16}$. Likewise, bits 02 and 03 shall be incremented by one when these Micro-commands occur at Control Storage Addresses $XFFE_{16}$ during any minor cycles other than E6 and/or E7.

Execution of RNI1, RNI2 and FZJ Micro-commands shall be additionally dependent on the state of the Instruction Repeat switch as described in 3.10.4.18, to the extent that the branch addresses associated with these Micro-commands may be altered from values of $X002_{16}$ and $X009_{16}$ to a value of $X000_{16}$.

Undesignated bit positions within these Micro-commands shall have no effect on Micro-command execution except to the extent that they shall participate in the formation of valid parity.

3.8.11.1 Function Decode Jump

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
FNJ	0	0	0	0	0	1	I	I_0	P	0	0	I_1				

This Micro-command shall transfer a 12-bit branch address to the Su Register, (except during minor cycles E6 and E7), and the Pp Register, in bit positions 04 through 15.

This 12-bit branch address shall be based on the I, I_0 and I_1 Micro-command designators as well as the contents of the common resource F Register, (for which bit positions shall be referred to as F_{00} through F_{15}).

a. When the I designator (bit 06) is clear, the 12-bit branch address at the designated inputs to the Su and Pp Registers shall have the following format:

04	05	06	07	08	09	10	11	12	13	14	15
I_0	I_1					F_{04}	F_{05}	F_{06}	F_{07}	0	0

b. When the I designator (bit 06) is set, the 12-bit branch address at the designated inputs to the Su and Pp Registers shall have the following format:

04	05	06	07	08	09	10	11	12	13	14	15
I_0	I_1					0	0	F_{08}	1	0	0

3.8.11.2 Format Decode Jump

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
FRJ	0	0	0	0	1	0			P	0	0					

This Micro-command shall transfer a 12-bit branch address to the Pp Register in bit positions 04 through 15. (The output of the D Fan-In Network must be stable 200 n/s prior to the execution of this Micro-command).

This 12-bit branch address shall be obtained by reading the output of the Address Table (9 bits of address, 1 bit for parity) and inserting 3 hardware translated bits. The conventions for addressing the Address Table and formatting its output are described in 3.5.3.

Once read, this Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle, with the transfer from the Address Table to the Pp Register occurring only during the first minor cycle of its execution.

3.8.11.3 Zero Jump

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
FZJ	0	0	0	0	1	1			P							

This Micro-command shall transfer a 12-bit branch address of 009_{16} to the Pp Register in bit positions 04 through 15 on the first minor cycle in which it is executed.

When the contents of the Au Register are not equal to 0000_{16}, no further operations shall be performed on the part of this Micro-command, and hardware control shall proceed to the execution of the next Micro-command as available at the output of Control Storage proper.

When the contents of the Au Register are equal to 0000_{16}, the Fu1 and Fu2 Register clocks shall be disabled for the remainder of the major cycle and no further operations shall be performed on the part of the current Processor State with respect to Micro-command execution.

3.8.11.4 Jump

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
JMP	1	0	0	1	N_0				P	0	0		N_1			

This Micro-command shall transfer an 8-bit branch address consisting of the N_0/N_1 fields to the Su Register, (except during minor cycles E6 and E7), and the Pp Register, in bit positions 08 through 15.

Thus, this Micro-command provides the means for performing branch operations within 256-word page boundaries of Control Storage proper, with the exceptions noted in 3.8.11, item a.

3.8.11.5 Read Next Instruction 1

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
RNI1	1	0	0	0	0	0	a	b	P	0	0	x				

This Micro-command shall transfer a 12-bit branch address of 002_{16} to the Pp Register in bit positions 04 through 15 on the first minor cycle in which it is translated.

In addition, this Format 1 Micro-command shall transfer the Overflow and Link bits from the Arithmetic status portion of Su to the Basic Register File with the register number for the partial write reference designated according to 3.8.1.1. This transfer shall be confined to the Basic Register File as a result of disabling the write operation when the "a" and "b" designators for this Micro-command are both in the set state and constitutes an exception to Format 1 Micro-command addressability. The Basic Register File shall be written in the left-most 8 bit positions such that Overflow shall be transferred to bit 00, bits 01, 02 and 04 through 07 shall be cleared, and Link shall be transferred to bit 03. The right-most 8-bits shall remain unchanged.

Once read, this Micro-command shall be held in the Fu1 and Fu2 Registers for the remainder of the major cycle.

3.8.11.6 Read Next Instruction 2

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
RNI2	1	0	0	0	0	1	a	b	P	0	0	x				

This Micro-command shall transfer a 12-bit branch address of 009_{16} to the Pp Register in bit positions 04 through 15 on the first minor cycle in which it is translated.

In all other respects, this Micro-command shall execute identically to the RNI1 Micro-command as described in 3.8.11.5.

3.8.12 Control Micro-commands

The Micro-commands within this class shall provide the means for performing Timing, Input/Output Termination and Boundary Crossing Mode operations.

Undesignated bit positions within these Micro-commands shall have no effect on Micro-command execution except to the extent that they shall participate in the formation of valid parity.

3.8.12.1 No Operation

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
NOP	0	0	0	0	0	0			P	0	0					

This Micro-command shall not influence CPU operations for the minor cycle during which it is contained in the Ful and Fu2 Registers.

3.8.12.2 Resynchronize

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SYNC	1	1	1	1	0	0			P	0	0	1				

This Micro-command shall transfer the Control Storage Address of the next successive Micro-command to bit positions 02 through 15 of the Pp Register on the first minor cycle in which it is executed.

Once read, this Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle.

Thus, the execution of a SYNC Micro-command shall result in the establishment of minor cycle E0 for the execution of the next successive Micro-command during the next major cycle allocated to the associated Processor State.

3.8.12.3 Invoke/Revoke Boundary Crossing Mode

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
IVK	1	1	1	1	0	1			P	0	0	1				
RVK	1	1	1	1	0	1			P	0	0	0				

During all minor cycles following the execution of an IVK Micro-command, up to and including the minor cycle in which an RVK Micro-command is executed, Boundary Crossing Mode shall be in effect with respect to the designation of register numbers on the part of all Micro-commands performing Register File references.

The Boundary Crossing Mode of designating register numbers by means of the contents of the BC Register is described in 3.2.3.7 including timing constraints where applicable.

The Normal Mode of designating register numbers by means of Format 1 Micro-commands only, is described in 3.8.1.1.

3.8.12.4 Read Control Memory

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
ROM	1	1	1	1	0	0			P	0	0	0				

This Micro-command shall transfer the Control Storage Address of the next successive Micro-command to bit positions 02 through 15 of the Pp Register on the first minor cycle in which it is executed.

Control Storage proper shall be read referenced at the address contained in the Bu Register and the output of Control Storage proper shall be subsequently transferred to the CSS Register (J-K inputs as described in 3.2.3.8) on the second minor cycle involved in the execution of this Micro-command.

Once read, this Micro-command shall be held in the Fu1 and Fu2 Registers for the remainder of the major cycle. ROM Micro-commands which begin execution on minor cycles E6 or E7 shall be undefined with respect to the data transfer to the CSS Register. Thus, meaningful execution of each ROM Micro-command shall require that an allowance be made for a minimum of 3 contiguous minor cycles in the same major cycle as shown in Figure 9. This allowance must be provided under Micro-command control.

3.8.12.5 Compare I/O

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
CIO1	1	0	0	0	1	0	1	1	P	0	0					
CIO2	1	0	0	0	1	1	1	1	P	0	0					

These Micro-commands shall transfer the Control Storage Address of the next successive Micro-command to bit positions 02 through 15 of the Pp Register on the first minor cycle in which they are executed.

Once read, these Micro-commands shall be held in the Ful and Fu2 Registers for the remainder of the major cycle.

Operations performed in the further execution of these Micro-commands shall be dependent upon the comparison of the contents of the Au and Bu Registers as well as the state of the appropriate End of Transfer signal when performed for Processor States 0 through 3. See 3.2.4.12 for a description of the End of Transfer signals.

a. When the contents of the Au Register are equal to the contents of the Bu Register, bit-for-bit, or in the presence of the appropriate End of transfer signal when applicable, the CI01 Micro-command shall provide an I/O Exit signal as described in 3.2.4.13 at the end of the first minor cycle of execution only.

b. When the contents of the Au Register are not equal to the contents of the Bu Register, bit-for-bit, or in the presence of the appropriate End of Transfer signal when applicable, the CI02 Micro-command shall provide an I/O Exit signal as described in 3.2.4.13 at the end of the first minor cycle of the execution only.

When these Micro-commands provide an I/O Exit signal at the end of the first minor cycle of their execution, no other operations shall be performed.

When these Micro-commands do not provide an I/O Exit signal at the end of the first minor cycle of their execution, the transfer of the contents of the Pp Register to the appropriate Pu Register (to the Su Register during consecutive major cycles for the same Processor State) which would otherwise occur during minor cycle W0, shall be suppressed. In addition, a pulse shall be applied to the clear input of the appropriate Busy Flip/Flop in the B/A Register for Processor States 0 through 4 at the end of the first minor cycle of execution of these Micro-commands in which an I/O Exit signal is not provided, as described in 3.2.3.1, item d.

Execution of these Micro-commands beginning on minor cycle E7 shall not be hardware supported and may result in machine malfunction.

3.9 Resource Allocation

Resource allocation shall be accomplished on a major cycle basis by means of the Resource Allocation Network as generally described in 3.1.8.

The Resource Allocation Network shall resynchronize all resource requests from Processor States 0 through 7 and the Console State, during minor cycle E1 at a time equivalent to CLOCK-60 as defined in 3.2.4.5.

The Refresh request from Main Storage shall occur synchronously and shall have unconditional priority over all other resource requests.

3.9.1 Non-Priority Mode

In the absence of Priority Mode operations, the Resource Allocation Network shall proportionately allocate major cycles to the requesting Processor States. This equal allocation of major cycles shall occur repetitiously, for the Processor States involved, in the following sequential order:

PROCESSOR STATE 0
PROCESSOR STATE 1
PROCESSOR STATE 2
PROCESSOR STATE 3
PROCESSOR STATE 4
PROCESSOR STATE 5
PROCESSOR STATE 6
PROCESSOR STATE 7
CONSOLE STATE

When more than one of these resource requests occur, (after the Main Storage Refresh requirements have been accounted for), resource allocation shall take place in the following manner.

Total Number of Requesting Processor States	Resource Allocation per State
2	50.0%
3	33.3%
4	25.0%
5	20.0%
6	16.6%
7	14.2%
8	12.5%
9	11.1%

3.9.2 Priority Mode

The Resource Allocation Network shall additionally resynchronize all resource requests from Processor States 0 through 3, relative to their coincidence with the associated Invoke Priority signals as described in 3.2.3.5 and relative to their combined coincidence with the associated Enable Priority and Priority signals as described in 3.2.3.5 and 3.2.4.11, respectively. These resynchronization activities shall occur during every minor cycle E1 at a time equivalent to CLOCK-60 as defined in 3.2.4.5.

Each Priority Mode request on the part of Processor States 0 through 3 shall have unconditional priority over all Non-Priority Mode requests. When more than two Priority Mode requests occur, priority shall be granted in the following order:

PROCESSOR STATE 0
PROCESSOR STATE 1
PROCESSOR STATE 2
PROCESSOR STATE 3

In the absence of Consecutive Cycle operations, Priority Mode requests shall result, (after the Main Storage Refresh requirements have been accounted for), in 50% of the resource utilization allocated to each Processor State so requesting, up to a maximum of two such States. When three or four Processor States have made simultaneous Priority Mode requests, only the two Processor States having highest priority shall be recognized. In such cases, these two Processor States shall equally share utilization of the resources to the exclusion of all other Processor States, (except for Null States performed as a result of Main Storage Refresh requests).

3.9.3 Non-Consecutive Cycle Mode

Without respect to Priority Mode operations, Non-Consecutive Cycle Mode shall affect resource allocation only when a single Processor State, 0 through 7, is requesting resource utilization in the absence of all other requests.

Thus, major cycles shall be alternately allocated between the single requesting Processor State and the Null State unless the appropriate Consecutive Cycle Enable is set as described in 3.2.3.5.

3.9.4 Consecutive Cycle Mode

Without respect to Priority Mode operations, Consecutive Cycle Mode shall affect resource allocation only when a single Processor State, 0 through 7, is requesting resource utilization in the absence of all other requests.

Thus, major cycles shall be consecutively allocated to the single requesting Processor State when the appropriate Consecutive Cycle Enable is set as described in 3.2.3.5. Consecutive Cycle Mode shall be accomplished by means of basic timing modifications as described in 3.8.1, item b.

NOTE: The Console State shall be unconditionally capable of utilizing consecutive major cycles without the basic timing modifications which shall be required for Processor States 0 through 7. See 3.7.1, item c.

3.9.5 Priority with Consecutive Cycle Mode

When both Priority and Consecutive Cycle Modes of operation are correspondingly specified for one or more Processor States, the highest priority Processor State thus requesting resource utilization shall obtain exclusive allocation of the resources, (with the exception of the Null State resulting from Main Storage Refresh requests).

NOTE: Each major cycle performed in this combined Priority and Consecutive Cycle Mode of operation shall be unconditionally followed by a Null State major cycle when the associated Busy Flip/Flop is cleared. See 3.7.1, item b.

3.10 System Control Panel (Console)

The Console description within this Section shall apply to the Console as implemented for Serial 8 and beyond.

Controls and indicators on the 7300 Console shall be arranged in four major groups as follows:

Operator Group (See Figure 10)
Program Group (See Figure 11)
Maintenance Group (See Figure 12)
Communications Activity Display Group (See Figure 13)

The relative positions of these groups is shown in Figure 14.

3.10.1 Mechanical

The Console Control Panel shall be approximately 28" H, 22"W, 11.5"D and positioned at the front of the 7300 Processor cabinet. For maintenance purposes, the control and indicator portions of the panel shall be capable of being pivoted 90 degrees into a mechanically locked position so as to be easily accessed from the P. C. module (card) side of the 7300 Processor cabinet.

3.10.2 Operator Group

With the exception of the Power On and Power Off switches as described in 3.10.2.2 and 3.10.2.3, respectively, the Operator Group of controls shall be enabled at all times. This group of controls shall provide the operator with the basic means for control of the 7300 Processor.

3.10.2.1 Emergency Pull

This control shall be a latching pull switch. Once pulled, a mechanical reset shall be required. The resetting mechanism shall be located behind the Console Control Panel such that it is accessible only by opening the Console Control Panel enclosure.

When pulled, this switch causes all A.C. and D.C. power to drop immediately, by-passing the normal power-down sequence. This action shall be referred to as Emergency Power Off (EPO).

CAUTION: OPERATION OF THIS CONTROL MAY RESULT IN PHYSICAL DAMAGE TO THE SYSTEM.

3.10.2.2 Power On

This control shall be a momentary push-button switch with an indicator.

The effect of this switch shall be conditioned by the Local/Remote Control described in 3.10.4. In Remote Control Mode the Power On switch shall have no effect. In Local Control Mode the depression of the Power On switch shall initialize the power-up sequence.

The indicator shall be on when the power-up sequence is initialized and shall remain on until a power-down sequence has been completed, i.e. during power sequencing and when power is on.

NOTE: Upon completion of the power-up sequence, a Reset/Load sequence shall be automatically initialized. Moreover, upon completion of the Reset/Load sequence, an Autoload sequence shall be automatically initialized provided the Maintenance Group controls have not been enabled. For a description of the Reset/Load and Autoload sequences, see 3.10.2.12 and 3.10.2.4, respectively.

3.10.2.3 Power Off

This control shall be a momentary push-button switch with an indicator.

The effect of this switch shall be conditioned by the Local/Remote Control as described in 3.10.4. In Remote Control Mode, the power off switch shall have no effect. In Local Control Mode, the depression of the Power Off switch shall initialize the power-down sequence.

The indicator shall be on unless one of the following conditions exist:

a. No primary power is available.

b. The Main Disconnect switch is off.

c. An EPO (Emergency Power Off) has occurred.

d. Power is on, i.e. that period between the completion of the power-up sequence and the initialization of the power-down sequence.

3.10.2.4 Autoload

This control shall be a momentary push-button switch with an indicator. When depressed, this switch shall initialize an Autoload sequence, and the indicator shall be on until the switch is released. The Autoload sequence shall consist of the following:

a. A System Reset shall be performed for a minimum of .4 m/s and a maximum of .6 m/s. For a description of the effects of System Reset, see 3.10.3.8.

b. Upon completion of the System Reset, the Busy F/F for Processor State 4 (Bit 04 of the Busy/Active Register) shall be set. This setting input shall be removed at the beginning of the first major cycle allocated to Processor State 4.

c. On the first major cycle allocated to Processor State 4, the Control Storage address shall be forced such that micro-code execution begins at address 0112_{16} or 0113_{16} as determined by the Load Select switch described in 3.10.2.5.

NOTE: At this point, the Autoload sequence shall be considered totally under micro-code control.

d. Real Time Clock increment pulses shall be enabled at the set input of the Busy F/F for Processor State 4. This enable shall exist until a System Reset occurs. These increment pulses shall be further conditioned by the Executive Disable switch as described in 3.10.4.27.

3.10.2.5 Load Select: Primary/Alternate

This control shall be a toggle switch.

This switch shall determine the state of the right-most bit of the Control Storage Address generated during the Autoload sequence. In the Primary, (down) position, the right-most bit shall be set, resulting in a Control Storage Address of 0113_{16}. In the Alternate, (up) position, the right-most bit shall be clear, resulting in a Control Storage Address of 0112_{16}.

This switch shall also determine the device interface selected within the Control Storage Loader logic during the Reset/Load sequence. In the Primary, (down) position, the Control Storage Loader shall interface Integrated File Adapter-type (IFA) signals. In the Alternate, (up) position, the Control Storage Loader shall interface Integrated Card Adapter-type (ICA) signals.

3.10.2.6 Speaker Volume

This control shall be a one-turn potentiometer which controls the potential volume level of the Console loudspeaker. Rotation of this control fully counter-clockwise shall reduce speaker volume to inaudibility. Rotation of this control fully clockwise shall provide the potential for maximum speaker volume.

For a description of the digital inputs and their relative effects on the console speaker's frequency and volume see 3.10.3.5.

3.10.2.7 Processor Fault

This control shall be a momentary push-button switch with an indicator.

The indicator shall be on when any of the following processor faults occur.

a. Control Storage Parity Error.

b. Main Storage Parity Error

c. D.C. Fault

d. Over-Temperature Condition.

Depression of the Processor Fault switch shall neither correct nor initialize recovery activities for any of these faults.

When the indicator is on as a result of Control or Main Storage Parity Error faults, depression of the switch shall cause the indicator to be off. The indicator shall remain off until the switch is released and no further Parity Errors occur.

When the indicator is on as a result of a D.C. Fault or an Overtemperature Condition, the Processor Fault switch shall have no effect.

Each of these Processor Faults shall have individual indicators within the Maintenance Group controls as described in Section 3.10.4.

3.10.2.8 I/O Fault

This control shall be a momentary push-button switch with an indicator.

The indicator shall be on when any of the following I/O faults occur.

a. Channel 1 Transmission Parity Error

b. Channel 2 Transmission Parity Error

c. Channel 1 Control Check Error

d. Channel 2 Control Check Error

e. Burst Check Error (during a Reset/Load sequence involving a File-type device only).

f. Failure of an IFA attached File to retract heads during the power down sequence.

Depression of the I/O Fault switch shall neither correct nor initialize recovery activities for any of these errors.

Depression of the I/O Fault switch shall cause the indicator to be off. The indicator shall remain off until the switch is released and no further I/O Faults occur.

Each of these I/O Faults shall have individual indicators within the Maintenance Group controls as described in Section 3.10.4.

3.10.2.9 Lamp Test

This control shall be a momentary push-button switch with an indicator.

When depressed, this switch shall cause all Console indicators to be on. When released, all Console indicators shall be off to the extent of the effects of this switch i.e. indicators shall remain on wherever the conditions for the on state otherwise exist.

When depressed, this switch shall also cause the Alarm to be audible. When released, the same effect for Alarm operation applies as for indicator operation as previously described.

3.10.2.10 Alarm

The Alarm shall be an audible signal only. The Alarm shall be on when the Lamp Test Switch is depressed or when any of the following conditions exist within the System.

a. Blower failure within the Processor, (interpreted as an over-temperature condition).

b. A D.C. Fault.

c. Failure of an IFA attached File to retract heads during the power-down sequence.

Each of these conditions could result in physical damage within the System. When blower failure or D.C. Fault conditions persist for approximately 60 seconds, the power-down sequence shall be automatically initialized. When the heads fail to retract during the power-down sequence, D.C. power within the Processor shall be removed but the power-down sequence shall be suspended at that point for as long as the heads remain extended.

3.10.2.11 Alarm Disable

This control shall be a momentary push-button switch with an indicator.

When the Alarm is audible, depressing the switch shall cause the Alarm to be off (disabled) and the Alarm Disable indicator to be on. When the switch is released and the condition(s) which cause the alarm no longer exists, the alarm shall be enabled (but inaudible unless and until fault conditions reoccur) and the Alarm Disable indicator shall be off.

3.10.2.12 Reset/Load

This control shall be a momentary push-button switch with an indicator.

Depression of this switch shall initialize a Deadstart sequence, and the indicator shall be on until the switch is released. The Reset/Load sequence shall consist of the following:

a. A System Reset shall be performed for a minimum of .4 m/s and a maximum of .6 m/s provided the Maintenance Group Controls have not been enabled. When the Maintenance Group Controls have been enabled, this System Reset shall be omitted from the Reset/Load sequence. For a description of the effects of System Reset, see 3.10.3.8.

b. Upon completion of the System Reset when applicable, the Control Storage Loader shall transfer data into Control Storage using either a Primary or Alternate device adapter as the source, where the selection is determined by the state of the Load Select switch described in 3.10.2.5. For a description of the Primary and Alternate sequences and signal conventions, see 3.5.8 and 3.5.9, respectively.

c. The Reset/Load sequence shall write data into Control Storage proper until all addresses present have been written, (16,384 words maximum, 1024 word increments), and shall then write data into the Address Table until all addresses present have been written (1024 words maximum, 256 word increments). The sizes of Control Storage proper and the Address Table may be selected for maximums of 4096 words and 256 words, respectively, by means of the Select CS Minimum control as described in 3.10.4.

d. Upon completion of the Reset/Load Sequence, an Autoload sequence shall be initialized provided the Maintenance Group Controls have not been enabled.

For additional details concerning the Reset/Load Sequence, see 3.5.7, 3.5.8, and 3.5.9.

3.10.3 Programmer Group

This group of controls shall be enabled only when the Console is in Program Mode or Maintenance Mode. When the Console is not in Program Mode and not in Maintenance Mode, the switches within this group shall have no effect. However, indicators within this group shall be enabled at all times.

3.10.3.1 Program Mode

This control shall be a push-on, push-off switch with an indicator. The indicator shall be on only when the Console is in Program Mode, i.e. the indicator shall be off when the Console is in Maintenance Mode.

Depression of the Program Mode switch to the on position shall enable all controls in the Program Group.

Depression of the Program Mode switch to the off position shall disable all controls in the Program Group provided the Maintenance Mode switch is also off.

Note: Program Mode and Maintenance Mode shall be mutually exclusive and Maintenance Mode shall have precedence when both selections are made simultaneously.

3.10.3.2 Console Address Register Display (20 bits)

These 20 controls shall be momentary, push-button switches with indicators. These switches and indicators shall be horizontally positioned as 5 groups of 4 bits each. Within the left-most group, bits shall be individually designated from left to right, X0 through X3. Within the right-most 4 groups, bits shall be individually designated from left to right, 00 through 15.

a. Console Address Register Display: X0 - X3

These switches and indicators shall not be functional unless the Relocation and Protection Feature is present in the 7300 Processor.

In the presence of the Relocation and Protection Feature, and when enabled, depression of these switches shall cause corresponding bits to be set in the Segment Tag Portion of the Console Address Register only. The indicators shall be on for corresponding bit positions that are set and off for corresponding bit positions that are clear in the Segment Tag portions of the S, Console Address, and PE Registers as determined by the Console Address Register Select described in 3.10.3.4.

b. Console Address Register Display: 00 - 15

When enabled, depression of these switches shall cause corresponding bits to be set in the Console Address Register only. The indicators shall be on for corresponding bit positions that are clear in the Su, S, Console Address, and PE Registers as determined by the Console Address Register Select described in 3.10.3.4.

3.10.3.3 Clear Address

This control shall be a momentary push-button switch.

When enabled, depression of this switch shall clear all bit positions of the Console Address Register only. The clear signal resulting from the depression of this switch shall continue until the switch is released.

3.10.3.4 Console Address Register Select

This control shall be a rotary switch with 4 panel designated positions. In a clockwise direction, the positions of this switch shall be designated Su, S, Address, and PE.

The Su and PE positions of this switch shall be enabled only when the Console is in Maintenance Mode as described in 3.10.4.1.

When enabled, the position of this switch determines whether Su, S, Console Address, or PE Register contents are transmitted to the Console Address Register Display indicators. In the presence of the Relocation and Protection Feature, the S position of this switch shall be further conditioned by the System/Physical control described in 3.10.3.14.

The Console Address Register Select switch shall be overridden by CS-RD and CS-WR selections at the Console Mode Select switch as described in 3.10.3.11.

NOTE: When controls within the Programmer Group do not otherwise influence the selection of the Register whose contents are transmitted to the Console Address Register Display indicators, the contents of the Console Address Register shall be selected.

3.10.3.5 Console Data Register Display (20 Bits)

These 20 controls shall be momentary push-button switches with indicators. These switches and indicators shall be horizontally positioned as 5 groups of 4 bits each. Within the left-most group, bits shall be individually designated from left to right X0 through X3. Within the right-most 4 groups, bits shall be individually designated from left to right, 00 through 15.

a. Console Data Register Display: X0-X3

These switches and indicators shall not be functional unless the Relocation and Protection Feature is present in the 7300 Processor.

In the presence of the Relocation and Protection feature, and when enabled, depression of these switches shall cause corresponding bits to be set in the Segment Tag portion of the Console Data Register only. The indicators shall be on for corresponding bit positions that are set and off for corresponding bit positions that are clear in the Segment Tag portions of the Console Data Register only.

b. Console Data Register Display: 00 - 15

When enabled, depression of these switches shall cause corresponding bits to be set in the Console Data Register only. The indicators shall be on for corresponding bit positions that are set and off for corresponding bit positions that are clear at Fu2, Fu1, RTC, CSS, B/A, Console Data, D, Au, Bu, SUM or BC outputs as determined by the Console Data Register Select described in 3.10.3.7.

The digital inputs to the Console Data Register Display lamp drivers in bit positions 13, 14, and 15 shall also be used as inputs to the Console Speaker drivers. Bit 15 shall have minimum control on Speaker coil current, bit 14 shall have approximately twice the control of bit 15 (+3 decibels), and bit 13 shall have approximately four times the control of bit 15 (+6 decibels).

3.10.3.6 Clear Data

This control shall be a momentary push-button switch.

When enabled, depression of this switch shall clear all bit positions of the Console Data Register only. The clear signal resulting from the depression of this switch shall continue until the switch is released.

3.10.3.7 Console Data Register Select

This control shall be a rotary switch, with 11 panel designated positions. In a clockwise direction the positions of this switch shall be designated Fu2, Ful, RTC, CSS, B/A, Data, D, Au, Bu, SUM, and BC.

The Fu2, Ful, RTC, CSS, D, Au, Bu, SUM and BC positions of this switch shall be enabled only when the Console is in Maintenance Mode as described in 3.10.4.1.

When enabled, the position of this switch determines whether Fu2, Ful, RTC, CSS, B/A, Console Data, BC, or the output from the ALU shall be transmitted to the Console Data Register Display indicators. In the D, Au, Bu, and SUM positions, the output of the ALU shall be selected. The output of the ALU shall be controlled by micro-command except during Null State cycles. Thus, when enabled, and during Null State cycles, switch positions of D, Au, Bu, and SUM shall be effective in selecting these outputs for transmission to the Console Data Register Display indicators.

The Console Data Register Select switch shall be over-ridden by CS-RD and CS-WR selections at the Console Mode Select switch as described in 3.10.3.11.

NOTE: When Controls with the Programmer Group do not otherwise influence the selection of the Register whose contents are transmitted to the Console Data Register Display indicators, the contents of Console Data Register shall be selected.

3.10.3.8 System Reset

This control shall be a momentary push-button switch with an indicator.

When enabled, depression of this switch shall result in a System Reset sequence and the indicator shall be on until the switch is released. The System Reset sequence shall consist of the following:

a. The output of the ALU shall be driven to the clear state.

b. The eight (8) Pu Registers within the Extended Register File, Group I, shall be cleared.

c. The B/A, T, Q, PM, BC, CSS, Console Address and Console Data Registers within the Extended Register File, Group II shall be cleared.

d. The Au, Bu, D and Forced Carry Registers within the ALU shall be cleared.

e. A reset signal shall be transmitted to the Extended Register File, Group III. (For the effects of this signal within the integrated adapters, see the appropriate document listed in 2.0).

f. The Resource Allocation Network shall be forced to issue Null cycles only.

g. The timing mechanism shall be forced to issue ten(10) minor cycles per major cycle, (E0 through E9).

h. The Su, Ful, and Fu2 Registers at the periphery of Control Storage shall be cleared.

i. The RTC Increment pulses shall be disabled at the set input of the Busy Flip-Flop for Processor State 4, (Bit 04 of the Busy/Active Register).

j. The logical inter-lock which is set by a Breakpoint Stop operation with Processor State 4, (and when set, disables the output of the Busy Flip/Flop for Processor State 4 from appearing at the input of the Resource Allocation Network), shall be cleared.

k. In the presence of the Relocation and Protection Feature, the Addressing Mode Register shall be cleared.

The System Reset sequence resulting from the depression of this switch shall continue until the switch is released.

3.10.3.9 Console Control Select: Stop/Step, Normal, Breakpoint

This control shall be a 3 position toggle switch.

When enabled, the position of this switch shall determine the mode in which Console Operations are performed. (Console Operations shall be selected by means of the Console Mode Select switch described in 3.10.3.11 and initialized by means of the Console Run Switch described in 3.10.3.10).

NOTE: Some Console Operations shall stop, despite the position of this switch, when error conditions occur as described in 3.10.3.11.

a. Stop/Step

In the Stop/Step, (up), position, this switch shall cause the Console Request Flip/Flop to clear at the beginning of E4 during all major cycles allocated to the Console State.

As a result, when Console Operations are already occurring, and this switch is moved to the Stop/Step position, the Console Operation shall stop, i.e. Stop Mode. For each initialization of Console Operation with this switch already in the Stop/Step position, a single major cycle shall be allocated to the Console, i.e. Step Mode. (Console Operation shall be initialized by means of the Console Run switch described in 3.10.3.10).

b. Normal

In the Normal, (center), position, this switch shall have no effect on the Console Request Flip/Flop, i.e. once initialized, Console Operation shall be performed continuously.

c. Breakpoint

In the Breakpoint, (down), position, this switch shall cause the Console Request Flip/Flop to clear at the beginning of E4 during all major cycles allocated to the Console in which a Breakpoint Comparison occurs and is applicable. (Console Operations for which Breakpoint stops are applicable are described in 3.10.3.11).

3.10.3.10 Console Run

This control shall be a momentary push-button switch with an indicator. The indicator shall be on during all major cycles allocated to the Console State.

When enabled, depression of this switch shall result in a single pulse, approximately 100 n/s in duration at the set input to the Console Request Flip/Flop.

As a result, each depression of this switch, when enabled, shall initialize a Console Operation provided the Console Mode Select switch, as described in 3.10.3.11, is also in an ena ed position.

3.10.3.11 Console Mode Select

This control shall be a rotary switch with 9 panel designated positions. In a clockwise direction, the positions of this switch shall be designated RO-WR, RO-RD, RF-WR, RF-RD, OFF, MS-RD, MS-WR, CS-RD, and CS-WR.

The CS-RD and CS-WR positions of this switch shall be enabled only when the Console is in Maintenance Mode as described in 3.10.4.1.

When enabled, the position of this switch shall select the type of Console Operation to be initialized when the Console Run Switch is depressed.

a. RO-WR

This position of the Console Mode Select switch shall have the following effects during all major cycles allocated to the Console State.

Micro-command execution shall be forced to begin at Control Storage Address 0100_{16}.

Micro-command sequences which would otherwise result in Main Storage Write operations shall be altered by hardware control into Register Option Write Operations.

Clocks shall be disabled at the micro-command translations for the Console Address Register .

b. RO-RD

This position of the Console Mode Select switch shall have the following effects during all major cycles allocated to the Console State.

Micro-command execution shall be forced to begin at Control Storage Address 0103_{16}.

Micro-command sequences which would otherwise result in Main Storage Read operations shall be altered by hardware control into Register Option Read Operations.

Clocks shall be disabled at the Micro-command translations for the Console Address Register.

c. RF-WR

This position of the Console Mode Select switch shall have the following effects during all major cycles allocated to the Console State.

Micro-command execution shall be forced to begin at Control Storage Address 0106_{16}.

In the presence of the Relocation and Protection Feature, Micro-command sequences which perform Register File Write operations in Boundary Crossing Mode shall be supplemented by hardware control to include participation of the Segment Tags for the Basic Register File.

d. RF-RD

This position of the Console Mode Select switch shall have the following effects during all major cycles allocated to the Console State.

Micro-command execution shall be forced to begin at Control Storage Address $010C_{16}$.

In the presence of the Relocation and Protection Feature, micro-command sequences which perform Register File Read operations in Boundary Crossing Mode shall be supplemented by hardware control to include participation of the Segment Tags for the Basic Register File.

e. OFF

This position of the Console Mode Select switch shall cause a clear signal at the Console Request Flip/Flop. This clear signal shall continue until the switch is moved from the OFF position.

NOTE: A Clear signal shall also be provided to the Console Request Flip/Flop during the time the Console Operation Select switch is between positions. Thus a change in Console Operation Selection while the Console is running shall result in stopping the Console Operation.

f. MS-RD

This position of the Console Mode Select switch shall have the following effects during all major cycles allocated to the Console State.

Micro-command execution shall be forced to begin at Control Storage Address 0103_{16}.

The Console Request Flip/Flop shall be cleared at the beginning at E7 when the Micro-command sequence performs a Main Storage Read and a Parity Error occurs, (an additional Main Storage reference for the Console shall not occur). This Parity Error stop shall be conditioned by the Storage Parity Disable control as described in 3.10.4.16.

The Console Request Flip/Flop shall be cleared at the beginning of E4 when the Micro-command sequence performs a Main Storage reference, the Main Storage Address compares bit-for-bit with the Breakpoint Address selection, and the Console Control Select switch is in the Breakpoint position.

The right-most 16-bits of the Console Address Register shall be cleared during E7 when the Micro-command sequence performs a Main Storage reference at an address which is not physically present, (Out of Range).

When the right-most bit (bit 15) of the Main Storage Address Register, S, is set, clocks shall be disabled at the Micro-command translations for the Console Address Register.

NOTE: In the presence of the Relocation and Protection Feature, the contents of the Main Storage Address Register, S, shall be interpreted as either a System or a Physical Main Storage Address as determined by the position of the Console Main Storage, Relocate/Off switch described in 3.10.3.12. Likewise, in the presence of the Relocation and Protection Feature, the Main Storage Address which is compared with the Breakpoint Address selection shall be either a System or Physical Main Storage Address as determined by the position of the System/Physical switch described in 3.10.3.14.

g. MS-WR

This position of the Console Mode Select switch shall have the following effects during all major cycles allocated to the Console State.

Micro-command execution shall be forced to begin at Control Storage Address 0100_{16}.

The Console Request Flip/Flop shall be cleared at the beginning of E4 when the Micro-command sequence performs a Main Storage reference, the Main Storage Address compares bit-for-bit with the Breakpoint Address selection, and the Console Control Select switch is in the Breakpoint position.

The right-most 16-bits of the Console Address Register shall be cleared during E7 when the Micro-command sequence performs a Main Storage reference at an address which is not physically present, (Out of Range).

When the right-most bit (bit 15) of the Main Storage Address Register, S, is set, clocks shall be disabled at the Micro-command translations for the Console Address Register.

NOTE: In the presence of the Relocation and Protection Feature, the contents of the Main Storage Address Register, S, shall be interpreted as either a System or a Physical Main Storage Address as determined by the position of the Console Main Storage, Relocate/Off switch described in 3.10.3.12. Likewise, in the presence of the Relocation and Protection Feature, the Main Storage Address which is compared with the Breakpoint Address selection shall be either a System or Physical Main Storage Address as determined by the position of the System/Physical switch described in 3.10.3.14.

h. CS-RD

This position of the Console Mode Select switch shall provide the means for selecting Control Storage Read operations to be performed under hardware control.

During Control Storage Read operations as initiated from the Console, the associated hardware sequences shall be mutually exclusive with Micro-command execution on the part of any Processor State.

This position of the Console Mode Select switch shall over-ride the Console Address Register and Console Data Register Select switches. The Console Address Register Display indicators shall be used in the right-most 16-bit positions to display the Control Storage address as contained in Su. The Console Data Register Display indicators shall be used in the right-most 16-bit positions to display Control Storage data as contained in the CSS Register for Control Storage proper, and as available at the input to the Pp Register for the Address Table.

During Control Storage Read operations, the contents of the Su Register shall be incremented by one at the beginning of each major cycle allocated to the Console State except on the first cycle following System Reset. Thus, the data indicated by the Console Address Register Display shall correspond to the contents of the Control Storage address indicated by the Console Address Register Display at the end of each major cycle allocated to the Console State.

In Stop/Step Mode, Control Storage Read operations shall reference a single Control Storage Address for each depression of the Console Run switch.

In Normal Mode, Control Storage Read operations initialized by depression of the Console Run switch shall attempt to scan all Control Storage locations physically present in the 7300 Processor. Longitudinal parity shall be checked for Control Storage proper and horizontal parity shall be checked for the Address Table. In the event of a Parity Error, the operation shall stop unless disabled by the Storage Parity Disable control described in 3.10.4. In the absence of a Parity Error stop, the complete scan shall occur repeatedly, including parity checking, until manually stopped from the Console.

In Breakpoint Mode, Control Storage Read operations initialized by depression of the Console Run switch shall attempt to scan all Control Storage locations physically present in the 7300 Processor. In the event that the Control Storage address contained in Su compares bit-for-bit with the Breakpoing Address selection, the operation shall stop. If the operation stops in Control Storage proper, the Console Data Register Display shall indicate the cumulative longitudinal check word for the associated page of 256 words, up to and including the address indicated by the Console Address Register Display. In the absence of a Breakpoint stop, a complete scan shall occur repeatedly until manually stopped from the Console.

The sizes of Control Storage proper and the Address Table may be selected for maximums of 4096 words and 256 words, respectively, by means of the Select CS Minimum control as described in 3.10.4.19.

i. CS-WR

This position of the Console Mode Select switch shall provide the means for selecting Control Storage Write operations to be performed under hardware control.

During Control Storage Write operations as initiated from the Console, the associated hardware sequences shall be mutually exclusive with Micro-command execution on the part of any Processor State.

This position of the Console Mode Select switch shall over-ride the Console Address Register and Console Data Register Select switches. The Console Address Register Display indicators shall be used in the right-most 16-bit positions to display the Control Storage Address as contained in Su. The Console Data Register Display indicators shall be used in the right-most 16-bit positions to display data to be written into Control Storage as contained in the Console Data Register.

During Control Storage Write operations, the contents of the Su Register shall be incremented by one after the data transfer is performed during each major cycle allocated to the Console State. Thus, the data indicated by the Console Data Register Display shall correspond to the data to be written at the Control Storage address indicated by the Console Address Register Display at the beginning of each major cycle allocated to the Console State.

In Stop/Step Mode, Control Storage Write operations shall write at a single Control Storage Address for each depression of the Console Run switch.

In Normal Mode, Control Storage Write operations initialized by depression of the Console Run switch, shall attempt to write all Control Storage locations physically present in the 7300 Processor. Once initialized, a complete write operation shall occur repeatedly until manually stopped from the Console.

In Breakpoint Mode, Control Storage Write operations initialized by means of the Console Run switch shall attempt to write all Control Storage locations physically present in the 7300 Processor. In the event that the Control Storage address contained in Su compares bit-for-bit with the Breakpoint Address selection, the operation shall stop prior to writing at that address. In the absence of a Breakpoint stop a complete write operation shall occur repeatedly until manually stopped from the Console.

The sizes of Control Storage proper and the Address Table may be selected for maximums of 4096 words and 256 words, respectively, by means of the Select CS Minimum control as described in 3.10.4.19.

3.10.3.12 Console Main Storage,Relocate/Off

This control shall be a 2 position toggle switch.

In the absence of the Relocation and Protection Feature this switch shall have no effect.

When enabled and during major cycles allocated to the Console State for the purpose of referencing Main Storage, the position of this switch shall determine whether the contents of the S Register shall be interpreted as a System or Physical Main Storage Address. In the Relocate (up) position, the contents of the S Register shall be interpreted as a System Main Storage Address and shall be converted by the relocation mechanism into a Physical Main Storage Address. In the Off (down) position, the contents of the S Register shall be directly interpreted as a Physical Main Storage Address and shall by-pass the relocation mechanism.

3.10.3.13 Breakpoint Address Select

Each of these 5 controls shall be a 16-position rotary switch.

In the absence of the Relocation and Protection Feature, the left-most switch shall have no effect.

These switches shall supply a 20-bit Breakpoint Address selection, expressed as 5 digits in hexadecimal notation.

a. The Breakpoint Address selection shall be compared bit-for-bit with Main Storage addresses. In the presence of the Relocation and Protection feature the full 20-bit Breakpoint Address shall be compared against the System or Physical Main Storage Address as determined by the position of the System/Physical control described in 3.10.3.14. In the absence of the Relocation and Protection Feature only the right-most 16-bits of the Breakpoint Address shall be compared with the contents of the S Register.

For Main Storage references on the part of the Console State, in Breakpoint Mode, a comparison between the Breakpoint Address and the Main Storage Address shall result in a Breakpoint stop.

For Main Storage references on the part of Processor States 0 through 7, in Breakpoint Mode, a comparison between the Breakpoint Address and the Main Storage Address shall result in a Breakpoint Stop for the appropriate Processor State provided the nature of the Main Storage reference has met one or more of the selections described in 3.10.3.15, 3.10.3.16, and 3.10.3.17.

b. The Breakpoint Address Selection shall be compared bit-for-bit with Control Storage Addresses. Only the right-most 16-bits of the Breakpoint Address shall be compared with the contents of the Su Register.

For Control Storage references on the part of the Console State, in Breakpoint Mode, a comparison between the Breakpoint Address and the contents of Su shall result in a Breakpoint stop.

For Control Storage references on the part of any Processor State, a comparison between the Breakpoint Address and the contents of Su shall provide a synchronization signal on TP 8 of the P. C. Module at 1A04 at the end of the minor cycle in which the comparison occurred.

NOTE: When the Console Address Register Select switch is enabled and in the Su position, the two left-most bits of Su which provide Overflow and Link status for Processor States 0 through 7 shall participate in the Breakpoint Address comparison; see 3.5.1, Su Formats.

3.10.3.14 Breakpoint Mode Select: System/Physical

This control shall be a 2-position toggle switch.

In the absence of the Relocation and Protection Feature this switch shall have no effect.

In the presence of the Relocation and Protection Feature, the position of this switch shall determine whether System or Physical Main Storage Addresses shall be compared with the Breakpoint Address selection. Likewise, the position of this switch shall determine whether System or Physical Main Storage Addresses shall be transmitted to the Console Address Register Display indicators when the Select switch is enabled and in the S position. System Main Storage Addresses shall be selected as described when this switch is enabled and in the System (up) position. Physical Main Storage Addresses shall be selected as described when this switch is disabled or in the Physical (down) position.

3.10.3.15 Breakpoint Mode Select: Read Instr/Øff

This control shall be a 2-position toggle switch.

When enabled and in the Read Instr (up) position, this switch shall enable a Breakpoint stop for Processor States 0 through 7 during major cycles which perform a Main Storage reference by beginning Micro-command execution at Control Storage Address $X00X_{16}$, i.e. RNIX, see 3.5.2.

In the Off (down) position, this switch shall not provide the Breakpoint stop enable just described.

3.10.3.16 Breakpoint Mode Select: Read Data/Øff

This control shall be a 2-position toggle switch.

When enabled and in the Read Data (up) position, this switch shall enable a Breakpoint stop for Processor States 0 through 7 during major cycles which perform a Main Storage read reference by beginning Micro-command execution at Control Storage Addresses other than $X00X_{16}$, i.e. not RNIX, see 3.5.2.

In the Off (down) position, this switch shall not provide the Breakpoint stop enable just described.

3.10.3.17 Breakpoint Mode Select: Write Data/Øff

This control shall be a 2-position toggle switch.

When enabled and in the Write Data (up) position, this switch shall enable a Breakpoint stop for Processor States 0 through 7 during major cycles which perform a Main Storage write reference by beginning Micro-command execution at Control Storage addresses other than $X00X_{16}$, i.e., not RNI, see 3.5.2.

In the Off (down) position, this switch shall not provide the Breakpoint stop enable just described.

3.10.3.18 Processor Control Select: Stop/Step, Normal, Breakpoint.

These 8 switches shall be 3-position toggle switches. These switches shall be designated 0 through 7, left to right, and shall individually correspond to Processor States 0 through 7.

a. When enabled and in the Stop/Step (up) position, these switches shall enable a clear input to the associated Busy Flip/Flop in the B/A Register at the beginning of E4 for each major cycle allocated to Processor States 0 through 7. This clear input shall clear the appropriate Busy Flip/Flop provided Micro-command execution begins at Control Storage Address $X00X_{16}$ for the major cycle allocated to the associated Processor State. This clear input shall also clear the appropriate Busy Flip/Flop when Cycle Step operation is selected by means of the control described in 3.10.4.27.

When enabled and in the Stop/Step (up) position, these switches shall directly apply a clear input to the associated Active Flip/Flops in the B/A Register for Processor States 5, 6, and 7. Thus, the enabling of a clear input to the Busy Flip/Flop as previously described shall be indirectly accomplished for Processor States 5, 6, and 7.

When enabled and in the Stop/Step (up) position, these switches shall disable the respective Request and Attention, (See 3.2.4) set inputs to the appropriate Busy Flip/Flops for Processor States 0, 1, 2, and 3.

b. In the Normal (center) position, these switches shall have no effect.

c. When enabled and in the Breakpoint (down) position, these switches shall enable a clear input to the associated Busy Flip/Flop in the B/A Register at the beginning of E4 for each major cycle allocated to Processor States 0 through 7.

This clear input shall clear the appropriate Busy Flip/Flop provided a Breakpoint Address comparison occurs as described in 3.10.3.13 and provided the nature of the Main Storage reference has satisfied one or more of the selections described in 3.10.3.15, 3.10.3.16, and 3.10.3.17.

Note: When a Breakpoint Stop is performed for Processor State 4, the output of the Busy Flip/Flop for this Processor State shall be disabled at the input to the Resource Allocation Network. Independent of its Busy Flip/Flop, major cycles shall not be allocated to Processor State 4 until this disable is removed by restarting Processor State 4 through the use of the Processor Run and Select Controls described in 3.10.3.19 and 3.10.3.20, respectively, or until the occurrence of a System Reset as described in 3.10.3.8.

3.10.3.19 Processor Run

This control shall be a momentary push-button switch with an indicator. The indicator shall be on when the switch is enabled and depressed, and remain on until the switch is released or disabled.

When enabled, depression of this switch shall result in a single pulse at the set input of each Busy Flip/Flop in the B/A Register. This pulse shall be further conditioned at these set inputs, by the position of the Processor Select control described in 3.10.3.20.

The leading edge of the Run pulse shall occur upon depression of the Run switch and the trailing edge of the Run pulse, independent of the Run switch, shall occur at the beginning of the major cycle allocated to the Processor State selected by means of the Processor Select Control described in 3.10.3.20.

3.10.3.20 Processor Select

This control shall be a rotary switch with 8 panel designated positions. In a clockwise direction, the positions of this switch shall be designated 0 through 7.

The position of this switch shall enable the Run pulse described in 3.10.3.19 at the set input of an individual Busy Flip/Flop, corresponding to the Processor State number 0 through 7 selected.

3.10.3.21 Processor State Display

This Display shall consist of 8 indicators designated from left to right as 0 through 7.

During each major cycle allocated to Processor States 0 through 7, the corresponding indicator shall be on.

3.10.4 Maintenance Group

Controls within this group shall be enabled only when the Console is in Maintenance Mode unless otherwise specified. However, indicators within this group shall be enabled at all times.

3.10.4.1 Maintenance Mode

This control shall be a push-on, push-off switch with an indicator. The indicator shall be on only when the Console is in Maintenance Mode.

Depression of the Maintenance Mode switch to the on position shall place the Console in Maintenance Mode. All controls in the Maintenance and Program groups shall be enabled and the Program Mode indicator shall be off.

Depression of the Maintenance Mode switch to the off position shall remove the Console from Maintenance Mode. All controls in the Maintenance Group shall be disabled unless otherwise specified. All controls in the Program Group shall be restored to dependency on the state of the Program Mode switch, including the state of the Program Mode indicator.

3.10.4.2 MS Parity Byte 0

This control shall consist of an indicator only.

In the absence of the ECC Feature, this indicator shall display the state of the parity bit associated with the left-most byte of data as supplied by Main Storage. The indicator shall be on when the parity bit is set and off when the parity bit is clear.

In the presence of the ECC Feature, this indicator shall be off.

3.10.4.3 MS Parity Byte 1

This control shall consist of an indicator only.

In the absence of the ECC Feature, this indicator shall display the state of the parity bit associated with the right-most byte of data as supplied by Main Storage. The indicator shall be on when the parity bit is set and off when the parity bit is clear.

In the presence of the ECC Feature, this indicator shall be off.

3.10.4.4 MS Parity Error

This control shall consist of an indicator only.

This indicator shall display the state of the Main Storage Parity Error Flip/Flop. The indicator shall be on when the Main Storage Parity Error Flip/Flop is set and off when the Main Storage Parity Error Flip/Flop is clear.

In the absence of theECC Feature, this Parity Error Flip/Flop shall set during Main Storage read references in which the total number of bits in the set state, including the parity bit, is even for either the left-most or right-most byte positions.

In the presence of the ECC Feature, this Parity Error Flip/Flop shall set during Main Storage read references in which non-correctable data errors are detected by the ECC Feature.

The Main Storage Parity Error Flip/Flop shall not set during Main Storage references to "Out of Range" or "Out of Bounds" addresses but shall set independently of the Storage Parity Disable control described in 3.10.4.16.

Once set, the Main Storage Parity Error Flip/Flop shall be cleared only by means of a System Reset or operation of the Processor Fault control described in 3.10.2.7.

3.10.4.5 CS Parity Error

Tnis control shall be an indicator only.

This indicator shall display the state of the Control Storage Parity Error Flip/Flop. The indicator shall be on when the Control Storage Parity Error Flip/Flop is set and off when the Control Storage Parity Error Flip/Flop is clear.

The Control Storage Parity Error Flip/Flop shall set for each of the following:

a. When a Micro-command as contained in the Fu2 Register consists of an even number of bits in the set state for any Processor State other than the Null State.

b. When the longitudinal check character as contained in the CSS Register reflects an even number of bits in any bit position column on a 256 word Page basis, during Control Storage Read operations initiated from the Console in Normal Mode (for Control Storage proper, only).

c. When the output of the Address Table, whether referenced by Micro-command or by hardware Control Storage Read operation, contains an even number of bits in the set state.

The Control Storage Parity Error Flip/Flop shall set independently of the Storage Parity Disable Control described in 3.10.4.16.

Once set, the Control Storage Parity Error Flip/Flop shall be cleared only by means of a System Reset or operation of the Processor Fault Control described in 3.10.2.7.

3.10.4.6 D.C. Fault

This control shall be an indicator only.

This indicator shall be on when any D.C. power supply within the 7300 Processor is not within its associated allowable output range for normal operation. The indicator shall remain on for as long as such a condition persists.

3.10.4.7 Overtemperature

This control shall be an indicator only.

This indicator shall be on as a result of either a blower failure or an overtemperature condition within the 7300 cabinet. These conditions shall result in an audible Alarm and in the event that they persist for approximately 60 seconds, a power-down sequence shall be initialized. See 3.10.2.10.

3.10.4.8 Heads Extended

This control shall be an indicator only.

This indicator shall be on when the heads in one or more IFA attached Files fail to retract during a power-down sequence. This condition shall result in an audible Alarm and suspension of the power-down sequence as described in 3.10.2.10.

3.10.4.9 Burst Check

This control shall be an indicator only.

This indicator shall be on when a Burst Check Error is detected during a Reset/Load sequence involving a File as the input device.

Once detected, the Burst Check Error indicator shall remain on until a System Reset occurs, (a System Reset shall occur during the initialization of a Reset/Load sequence when the Console is not in Maintenance Mode.

3.10.4.10 Channel 1 Data Check

This control shall consist of an indicator only.

This indicator shall display the state of the Channel 1, Transmission Check Flip/Flop/ The indicator shall be on when the Transmission Check Flip/Flop is set and off when the Transmission Check Flip/Flop is clear.

The Channel 1 Transmission Check Flip/Flop shall set when the I/O Channel detects a parity error on incoming data, i.e. a byte of data from an adapter in which the total number of bits in the set state, including the parity bit, is even.

Once set, the Channel 1 Transmission Check Flip/Flop shall be cleared only under Micro-command control or by means of a System Reset.

Channel 1 shall be associated with Processor State 1 and shall provide the corresponding Extended Register, Group III facilities as described by the appropriate document listed in 2.0.

In the absence of Channel 1 this indicator shall be off.

3.10.4.11 Channel 1 Control Check

This control shall consist of an indicator only.

This indicator shall display the state of the Channel 1, Control Check Flip/Flop. The indicator shall be on when the Control Check Flip/Flop is set and off when the Control Check Flip/Flop is clear.

The Channel 1 Control Check Flip/Flop shall set when the I/O Channel detects concurrence of more than one Tag In Line (Address In, Service In, Data In and Status In; or Select In and Operational In) or concurrence of Command Out and Service Out.

Once Set the Channel 1 Control Check Flip/Flop shall be cleared only under Micro-command control or by means of a System Reset.

In the absence of Channel 1 this indicator shall be off.

3.10.4.12 Channel 2 Data Check

This control shall consist of an indicator only.

This indicator shall provide a display for Channel 2, associated with Processor State 2, equivalent to the Channel 1 Data Check described in 3.10.4.10.

3.10.4.13 Channel 2 Control Check

This control shall be an indicator only.

This indicator shall provide a display for Channel 2, associated with Processor State 2, equivalent to the Channel 1 Control Check described in 3.10.4.11.

3.10.4.14 Select Even Parity, Byte 0

This control shall be a push-on, push-off switch with an indicator. The indicator shall be on when the switch is enabled and depressed to the on position. The indicator shall be off when the switch is disabled or depressed to the off position.

In the presence of the ECC Feature, this switch shall have no effect.

In the absence of the ECC Feature, when enabled, and when depressed to the on position, this switch shall cause the parity bit associated with the left-most 8 bits of data transmitted to Main Storage to be generated such that the total number of bits in the set state, including this parity bit, is even. Thus all Main Storage write references performed under these conditions shall result in Main Storage Parity Error detection during subsequent Main Storage read references at the affected Main Storage Addresses.

When disabled or depressed to the off position, this switch shall have no effect.

3.10.4.15 Select Even Parity, Byte 1

This control shall be a push-on, push-off switch with an indicator. The indicator shall be on when the switch is enabled and depressed to the on position. The indicator shall be off when the switch is disabled or depressed to the off position.

In the presence of the ECC Feature this switch shall have no effect.

In the absence of the ECC Feature, when enabled, and when depressed to the on position, this switch shall cause the parity bit associated with the right-most 8 bits of data transmitted to Main Storage to be generated such that the total number of bits in the set state, including this parity bit, is even. Thus, all Main Storage write references performed under these conditions shall result in Main Storage Parity Error detection during subsequent Main Storage read references at the affected Main Storage Addresses.

When disabled or depressed to the off position, this switch shall have no effect.

3.10.4.16 Storage Parity Disable/Off

This control shall be a 2-position toggle switch.

When enabled and in the Storage Parity Disable (up) position, this switch shall disable the hardware trap sequences which would otherwise occur for Processor States 0 through 7 in the event of Control Storage Parity Error detection (Control Storage Trap Address $X028_{16}$) and Main Storage Parity Error detection (Control Storage Trap Address $X018_{16}$). In addition, this switch shall disable Console stop operations which would otherwise occur in the event of Control Storage or Main Storage Parity Error detection during read references on the part of the Console State.

This switch shall not affect the Main Storage and Control Storage Parity Error displays described in 3.10.4.4 and 3.10.4.5 respectively.

When disabled or in the Off (down) position, this switch shall have no effect.

3.10.4.17 CS Disable/Off

This control shall be a 2-position toggle switch.

When enabled and in the CS Disable (up) position, this switch shall disable the output of Control Storage proper such that all read references shall result in an output of 14 bits in the clear state. In addition, this switch shall enable a clock to the Pp Register during every minor cycle. Finally, this switch shall disable Control Storage Parity Error detection for Processor STates 0 through 7 during read references to Control Storage proper.

When disabled or in the Off (down) position, this switch shall have no effect.

3.10.4.18 Instruction Repeat/Off

This control shall be a 2-position toggle switch.

When enabled and in the Instruction Repeat (up) position, this switch shall alter the execution of the RNI1 and RNI2 Micro-commands such that Control Storage Branch Addresses of $X002_{16}$ and $X009_{16}$ for these two Micro-commands, respectively, shall be converted to $X000_{16}$. Likewise, this switch shall alter the execution of the FZJ Micro-command to the extent that the Control Storage Branch Address of $X009_{16}$ shall be converted to $X000_{16}$.

When disabled or in the Off (down) position, this switch shall have no effect.

3.10.4.19 Select CS Minimum/Off

This control shall be a push-on, push-off switch with an indicator. The indicator shall be on when the switch is enabled and depressed to the on position. The indicator shall be off when the switch is disabled or depressed to the off position.

When enabled and in the Select CS Minimum (up) position, this switch shall select Control Storage sizes of 4096 words maximum for Control Storage proper and 256 words maximum for the Address Table.

NOTE: Hardware control information relative to the sizes of Control Storage proper and the Address Table shall be effective only during Console Control Storage Read, Console Control Storage Write and Reset/Load operations.

When disabled or depressed to the off position, this switch shall have no effect.

3.10.4.20 Set D, Set Au, Set Bu

These controls shall consist of 2 push-on, push-off switches with individual indicators. The left-hand switch shall be additionally designated "Set Au" and the right-hand switch shall be additionally designated "Set Bu". For each of these switches, the indicator shall be on when the switches are enabled and the associated switch is depressed to the on position.

a. When enabled and depressed to the on position, the Set Au switch shall result in the setting of the 16-Flip/Flops comprising the Au Register during every minor cycle the switch remains in the enabled on position.

b. When enabled and depressed to the on position, the Set Bu switch shall result in the setting of the 16 Flip/Flops comprising the Bu Register during every minor cycle the switch remains in the enabled on position.

c. When both the Au and Bu switches are enabled and depressed to the on positions simultaneously, the 16 Flip/Flops comprising the D Register shall be set for every minor cycle these switches remain in the enabled on positions. Likewise, a carry shall be forced into the right-most bit position of the Adder.

When disabled or depressed to the off position, these switches shall have no effect.

3.10.4.21 Time Meter

This control shall be a 7 decimal digit meter.

This meter shall provide the total accumulated time during which logic power has been applied to the 7300 Processor. The meter shall provide this reading in hundredths of hours and shall operate independently of Console Maintenance Mode.

3.10.4.22 Voltmeter

This control shall be a linear scale meter and shall operate independently of Console Maintenance Mode.

This meter shall provide power supply voltage measurements in per cent deviation from nominal values, with 0% deviation at scale center. Meter deviations to the left shall indicate low voltage magnitudes and deviation to the right shall indicate high voltage magnitudes regardless of the positive or negative character of the voltages selected by means of the Voltage Select control described in 3.10.4.23.

3.10.4.23 Voltage Select

This control shall be rotary switch with 14 panel designated positions. In a clockwise direction the positions of this switch shall be designated OFF, +28, +24, +23.3, +19.8, +12, +5A, +5B, +5C, +3, -3, -5, -12 and OFF.

The numerically designated positions of this switch shall select the associated voltage for measurement by means of the Voltmeter described in 3.10.4.22.

When in the Off position, this switch shall select a 0% reading at the Voltmeter.

3.10.4.24 Logic A, Logic B, Main Storage Adjusts

These controls shall consist of 3 ten-turn potentiometers. Each of these potentiometers shall be screw driver adjustable.

These controls shall be designated from left to right, "Logic A", "Logic B", and "Main Storage" and shall provide the means for adjusting the associated voltages independently of Console Maintenance Mode.

3.10.4.25 Power Mode, Remote/Local

This control shall be a 2-position toggle switch and shall operate independently of Console Maintenance Mode.

In the Remote (up) position, this switch shall place the 7300 Processor power system in Remote Control Mode. For a description of Remote Control Mode, see the appropriate document listed in 2.1.

In the Local (down) position, this switch shall place the 7300 Processor power system in Local Mode, under control of the Power On and Power Off switches described in 3.10.2.2 and 3.10.2.3 respectively.

The position of this switch shall not effect the operation of the Emergency Pull control described in 3.10.2.1.

3.10.4.26 Executive Disable/Off

This control shall be a 2-position toggle switch.

When enabled and in the Executive Disable (up) position, this switch shall disable a set input to the Busy Flip/Flop for Processor State 4 (Bit 04 of the B/A Register). The set input disabled by this switch shall occur for each increment of the RTC Register provided the additional enable described in 3.10.2.4 is satisfied.

In the Off (down) position, this switch shall have no effect.

3.10.4.27 Cycle Step/Off

This control shall be a 2-position toggle switch.

When enabled and in the Cycle Step (up) position, this switch shall enable a clear input to the appropriate Busy Flip/Flop in the B/A Register at the beginning of E4 for each major cycle allocated to Processor States 0 through 7.

This clear input to each of the Busy Flip/Flops shall be further conditioned on an individual basis by the Stop/Step (up) position of the appropriate Processor Operation Mode control as described in 3.10.3.18.

In the Off (down) position, this switch shall have no effect.

3.10.5 Communications Activity Display Group

This Display Group shall consist of a matrix of indicators arranged as 16 columns by 9 rows. Each column shall correspond to a Communications Channel facility which may be accomodated within the 7300 Processor. Although space is reserved within the matrix for 16 Communications Channels, indication of Communications Activity shall be provided for only those Channels physically present in the 7300 Processor.

The row-by-row, (from bottom to top), description of these indicators is specified in 3.10.5.1 through 3.10.5.9.

3.10.5.1 Enable (EN)

When on, the indicators within this row shall indicate that the associated Channel adapters are enabled and therefore not in the System Reset or Loop Test mode.

3.10.5.2 Ring Indicator (CE)

When on, the indicators within this row shall indicate that the associated Channel is receiving a ringing signal.

NOTE: Under normal System operation, calls should be answered on the leading-edge of the ringing signal. Thus the on condition of these indicators should imply either a malfunction in the associated Channel or that the associated Channel is not enabled.

3.10.5.3 Off Hook (OH)

When on, the indicators within this row shall indicate that the associated Channel has operated this signal to obtain dial tone and to generate the desired dial digits when originating a call. (Dial digits shall be generated by pulsing this signal).

3.10.5.4 Data Set Ready (CC)

When on, the indicators within this row shall indicate that the associated Channel is connected to a Communication line and has completed the transmission of the answer tone.

3.10.5.5 Secondary Received Line Signal Detector (SCF)

When on, the indicators within this row shall indicate that the associated Channel has properly received the Secondary Channel Line signal where applicable.

NOTE: This signal shall be used to indicate circuit assurance status and thus, signal the interrupt condition.

3.10.5.6 Received Line Signal Detector (CF)

When on, the indicators within this row shall indicate that the associated Channel modem is receiving a signal which meets its suitability criteria for demodulation, and in the case of half duplex Channels, that the Line Adapter is in receive mode.

3.10.5.7 Clear to Send (CB)

When on, the indicators within this row shall indicate that the associated Channels are in a transmit condition.

3.10.5.8 Transmitted Data (BA)

When on, the indicators within this row shall indicate that the associated Channels are in the spacing condition, binary zero.

When off, the indicators within this row shall indicate that the associated Channels are in the marking condition, binary one.

3.10.5.9 Received Data (BB)

When on, the indicators within this row shall indicate that the associated Channels are in the spacing condition, binary zero.

When off, the indicators within this row shall indicate that the associated Channels are in the marking condition, binary one.

NOTE: Depending on the Transmission Facility utilized by each Communications Channel, certain Status Indicators as described in 3.10.5.1 through 3.10.5.9 may not be applicable.

3.11 Reliability, Availability, Serviceability

The design parameters described in 3.1.10 with respect to the implementation of the 7300 Processor, shall contribute sufficient reliability characteristics as required to achieve the MTBF goal described in 3.11.1.

Console capabilities described in 3.10.2 through 3.10.4, as well as modular packaging of the 7300 Processor elements, shall contribute sufficient serviceability characteristics as required to achieve the MTTR goal, described in 3.11.2, provided such hardware characteristics are complemented by means of exerciser, fault detection and fault isolation procedures, including software/firmware routines.

3.11.1 MTBF

The mean time between failure goal for the CPU portion of the 7300 Processor shall be 4,000 hours (Failure Rate = .25/1000 hours).

3.11.2 MTTR

The mean time to repair goal for the 7300 Processor shall be 2 hours.

3.12 Mechanical

The 7300 Processor cabinet, including the Console, shall be physically dimensioned according to Figure 15 and 16. (Conceptual cabinet sketch is provided by Figure 17 for reference only).

Maximum weight shall be 1350 lbs.

3.13 Environmental

The Memorex 7300 shall conform to 882020 with the following exception:

Acoustical Noise; Noise shall not exceed 35 db.

3.14 Power System

The 7300 Processor power system shall conform to 882059 with input voltages of 208/230V, 50 or 60 Hz.

4.0 QUALITY ASSURANCE PROVISIONS

This section establishes requirements and procedures implemented to produce a product with maximum performance and reliability.

4.1 Components

In the context of this section, components shall be construed to include all piece parts from which the Processor is constructed.

All components shall be documented and controlled to a sufficient degree to assure proper form, fit, and function.

Components which significantly affect performance and reliability, and which are purchased by Memorex for use in the product shall be procured only from sources which have been determined to be acceptable by Component Engineering.

All components shall be purchased and inspected in accord with all applicable documentation. Components which do not meet all requirements shall not be used without the prior written authorization of the cognizant engineering group.

4.2 Construction

The machine shall be constructed and inspected in accordance with all applicable engineering drawings and specifications. Construction processes and techniques shall be such that no damage or subsequent degradation results to any component.

4.3 Prior to shipment, each machine shall be operated for at least 50 hours (power-on time) under the approved Final System Inspection procedure. This inspection shall verify all mechanical and electrical operations of the machine. The machine shall be powered by an A-C input which is equivalent to the destination requirements. During this inspection, each machine shall be exercised with appropriate software to demonstrate, with the highest possible confidence level, the software execution required by the particular configuration.

4.4 Qualification Testing

A complete qualification test in accord with 882038 shall be run periodically to assure conformance with all provisions of applicable specifications.

5.0 PREPARATION FOR DELIVERY

Shipment of the machine shall require separation of the Console Table from the Main Cabinet. Disconnected wiring shall be clearly labeled to facilitate rapid reconnection in the field.

All doors and removable panels shall be securely fastened shut by tape or strapping. Particular care shall be taken not to scratch or mar painted surfaces, or to bend any sheet metal. No straps shall be permitted to cross the console panel to prevent damage to the controls.

Standard shipment shall be by electronic padded van, and packaging shall be designed for optimum protection under this mode of transportation. Special crating shall be designed to meet the requirements for air shipment and for alternate methods of surface shipment.

Prior to packing, Quality Assurance shall verify that all required inspection has been performed. An inspector shall check during packaging to insure that approved packing specifications are followed and that external marking of the packages is correct and legible. The inspector shall check the units on the van to insure that adequate tie downs and blocking are used, and shall only release the shipment when all requirements are met.

6.0 NOTES

With respect to the 7300 Processor the following terms have been used inter-changeably:

Console Address Register - M Register
Console Data Register - N Register
Logical One - "1", high, set.
Logical zero - "0", low, clear
Read Instr - RNI (Read Next Instruction)
Read Data - ROP (Read Operand)
Reset - Clear
Reset/Load - Deadstart
Run - Go, (Processor States 0 through 7)
Selectable Register Features - Register Option
Store Data - STO (Store Operand)
System Control Panel - Console
System Reset - Master Clear

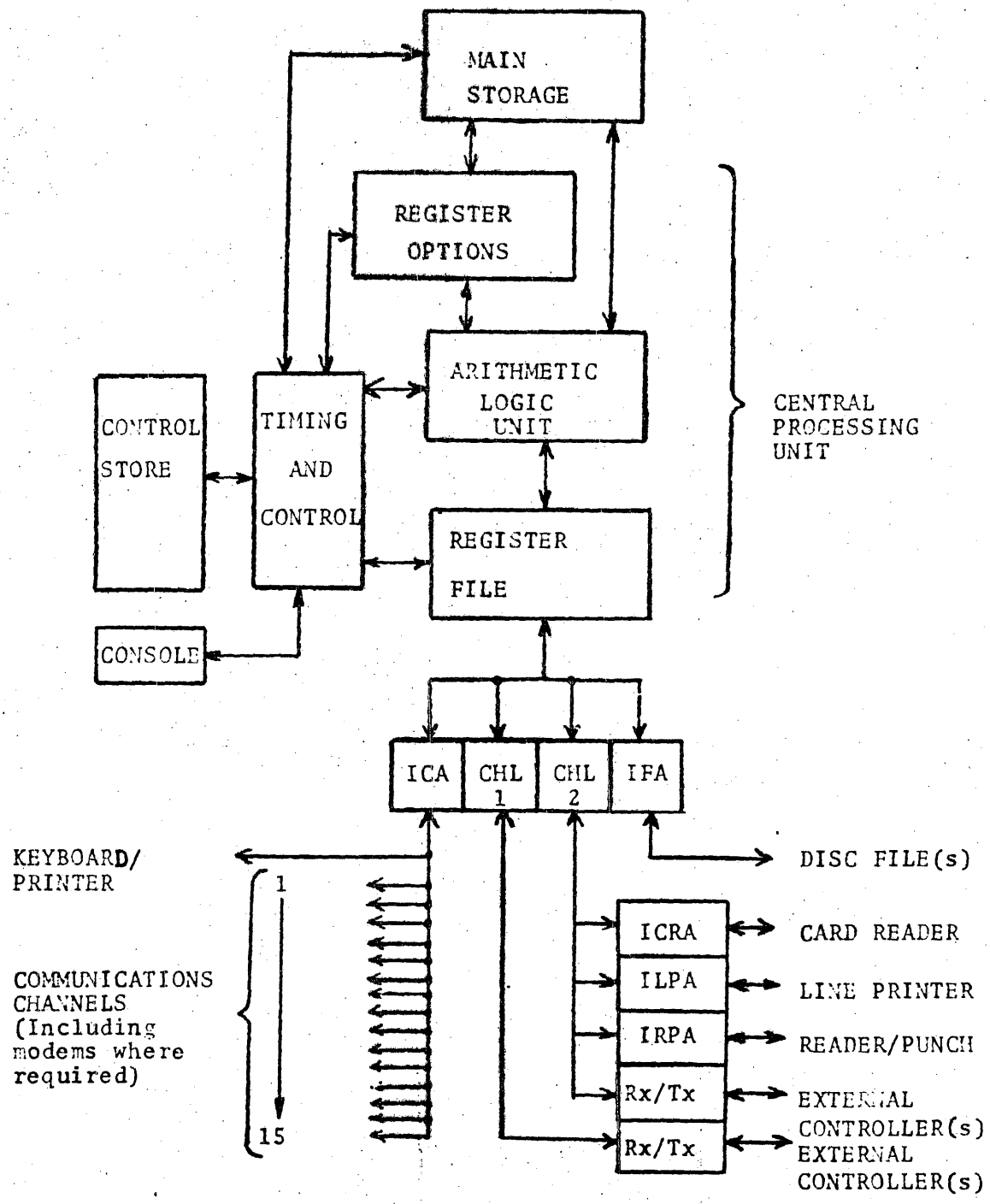


FIGURE 1:

7300 PROCESSOR BLOCK DIAGRAM

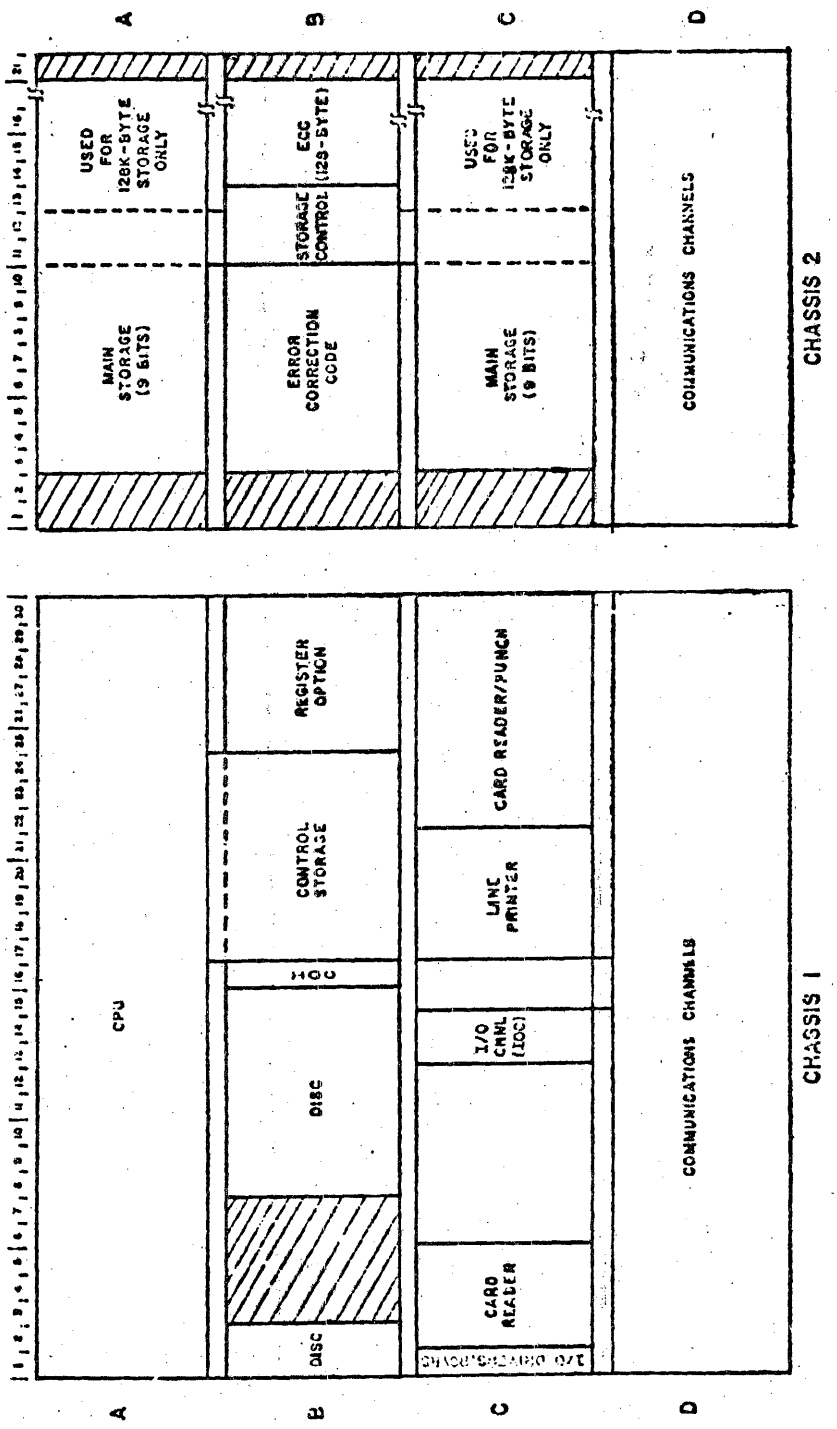


FIGURE 2

PROCESSOR ELEMENTS WITHIN THE 7300 PROCESSOR CABINET

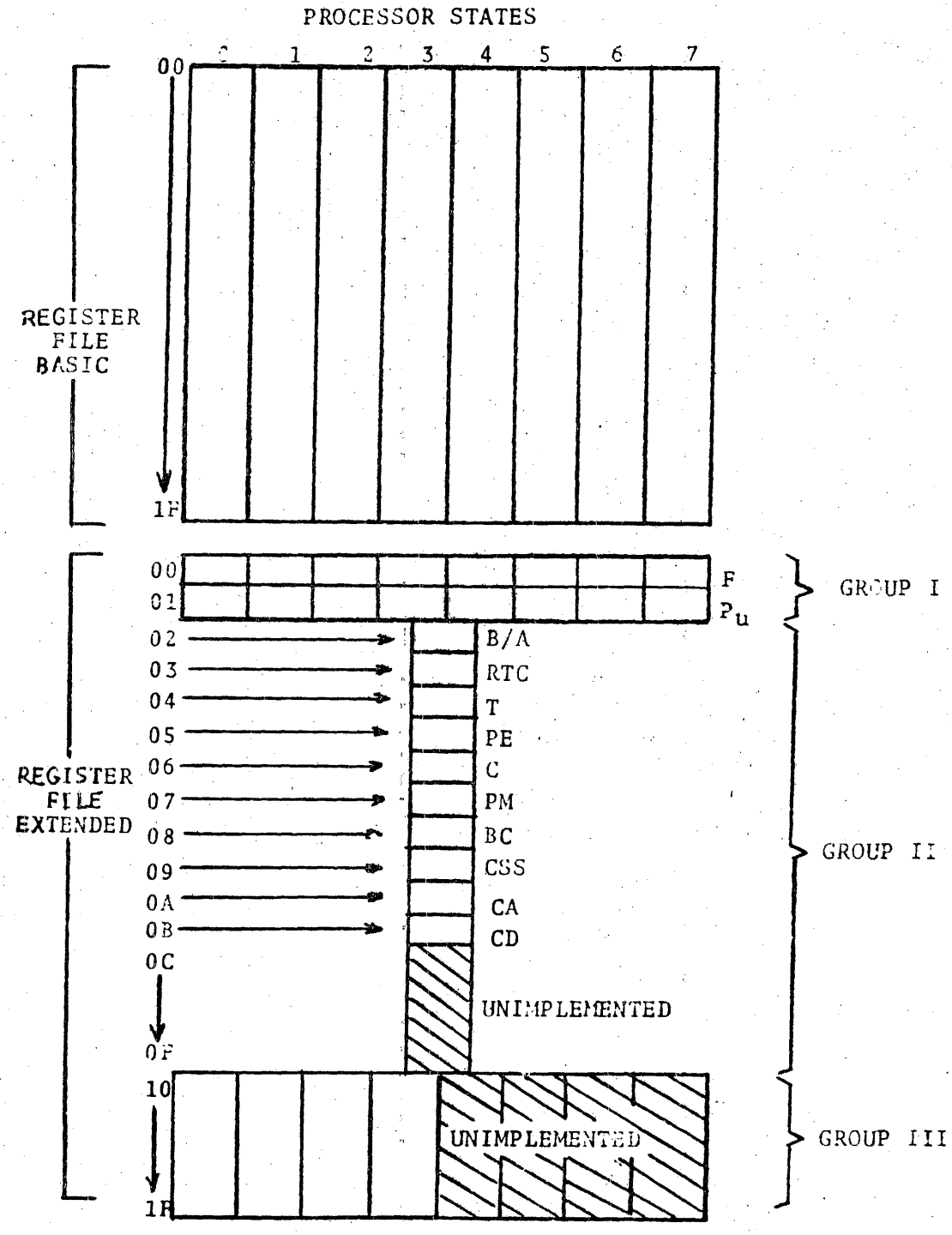


FIGURE 3:
REGISTER FILE ORGANIZATION (HEXADECIMAL NOTATION)

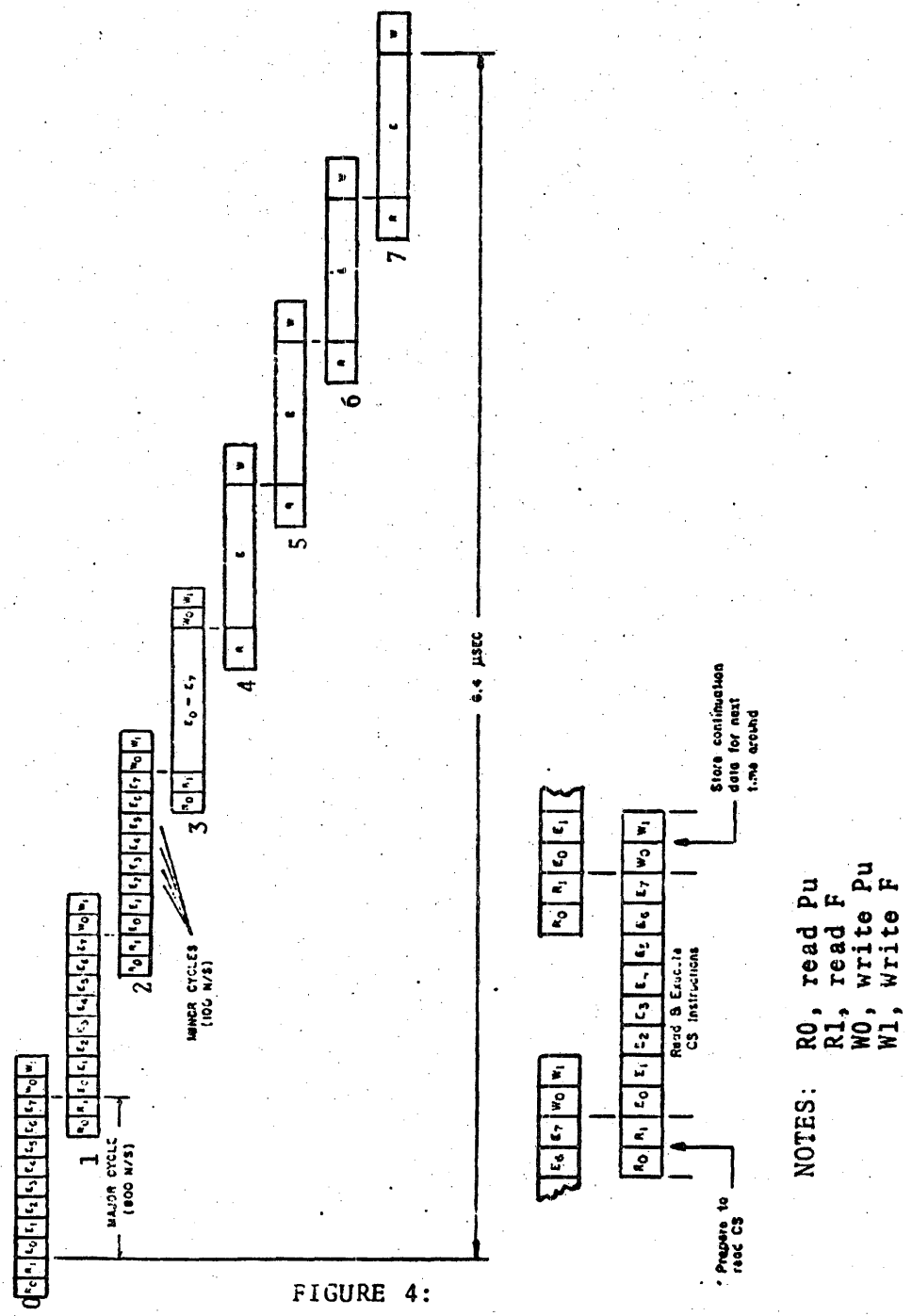


FIGURE 4:

MULTI-STATE SEQUENCE FOR PROCESSOR STATES 0 THROUGH 7 WITHOUT PRIORITY

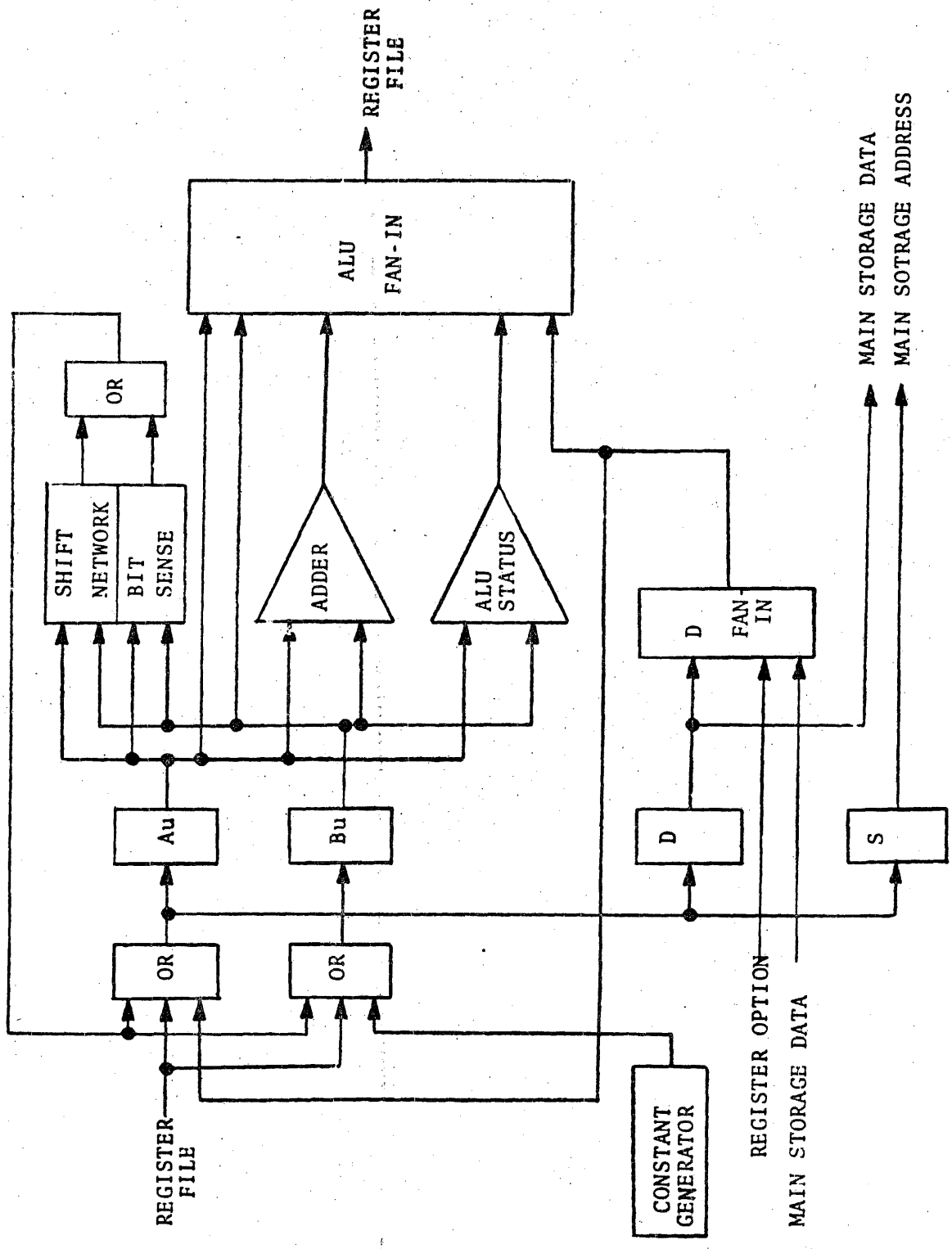


FIGURE 5 - ALU BLOCK DIAGRAM

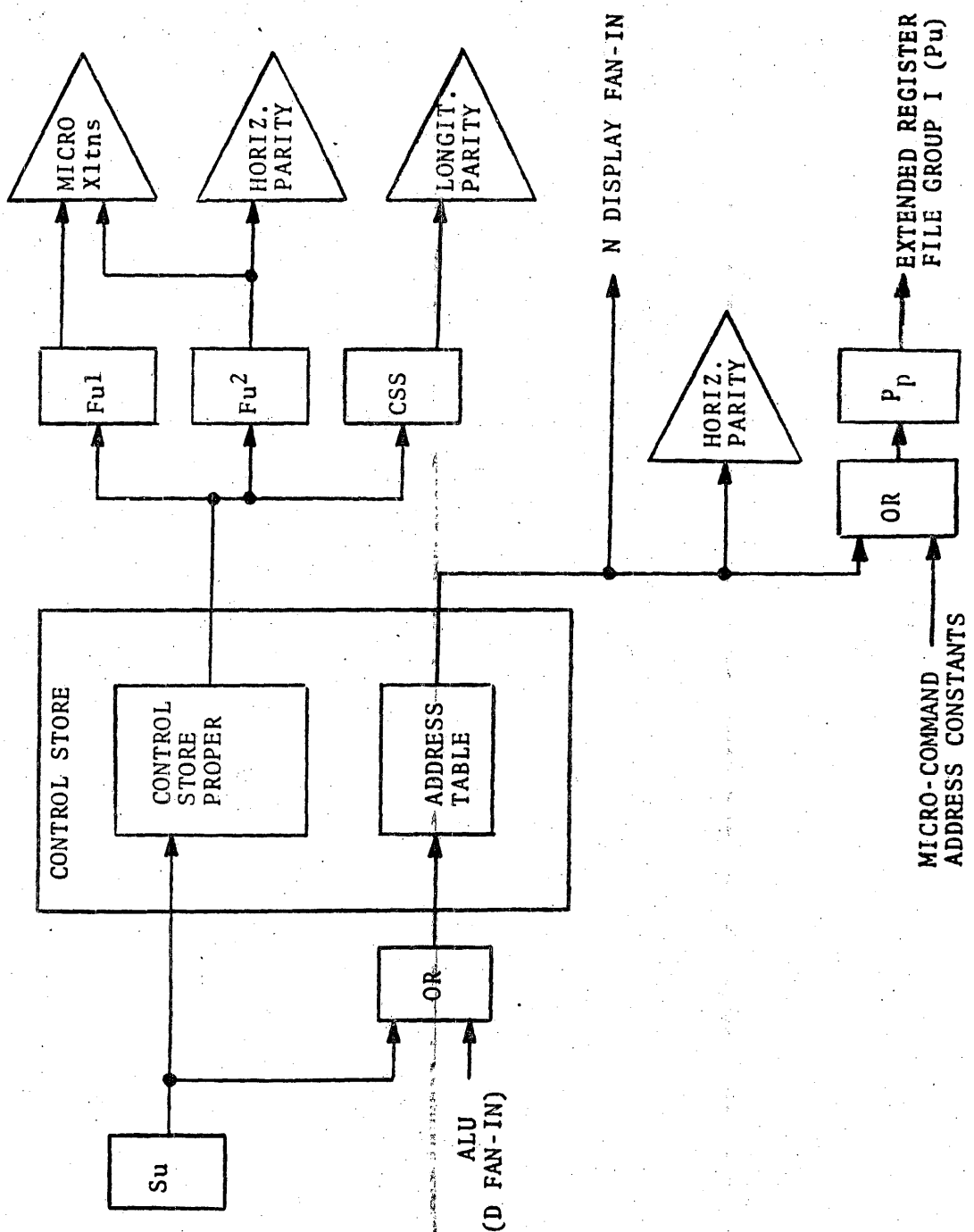
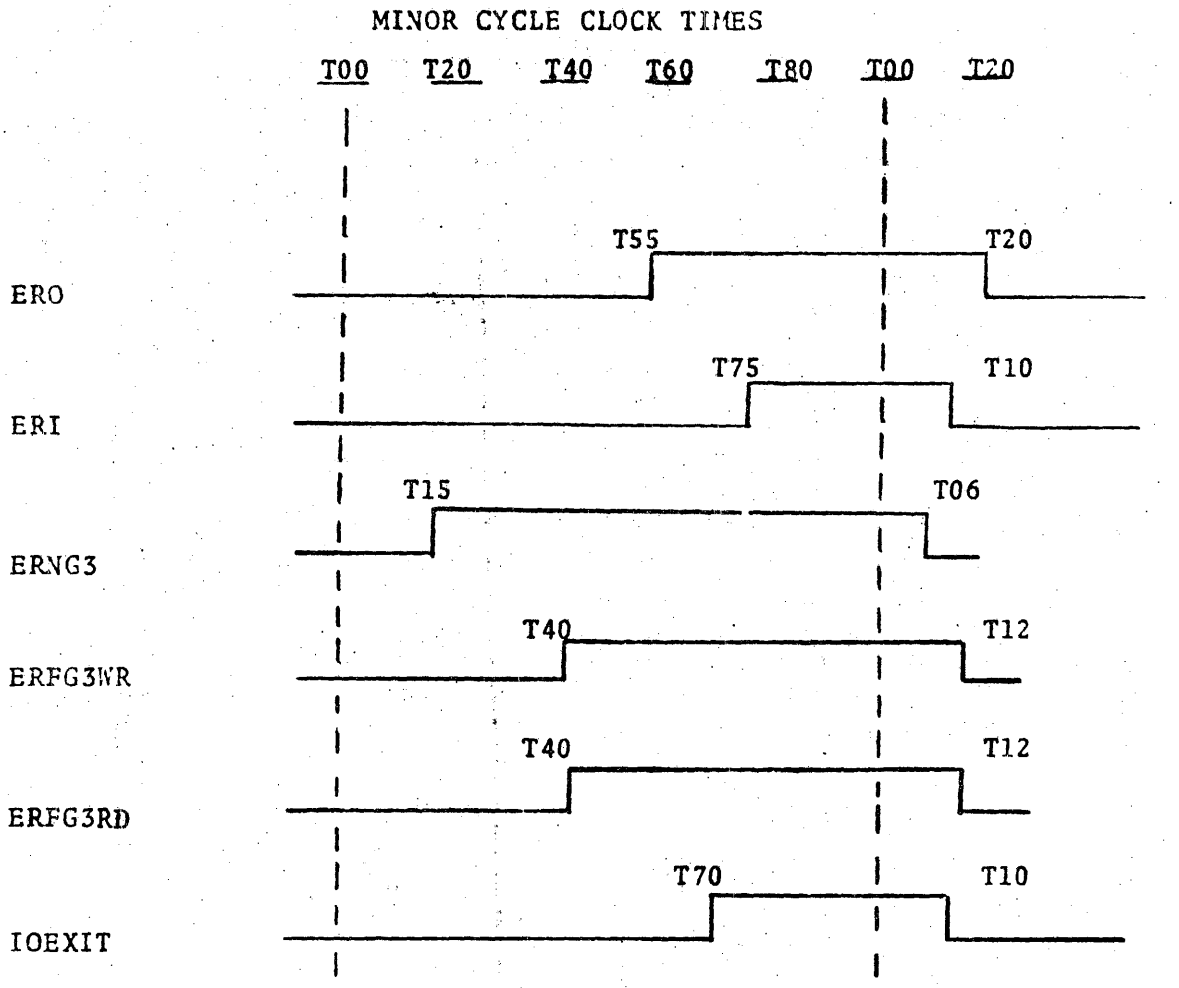


FIGURE 6 - CONTROL STORE AND PERIPHERY



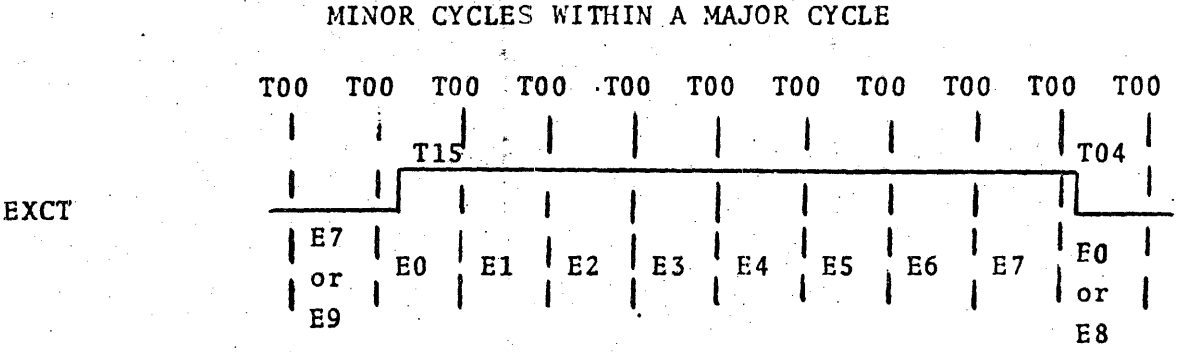
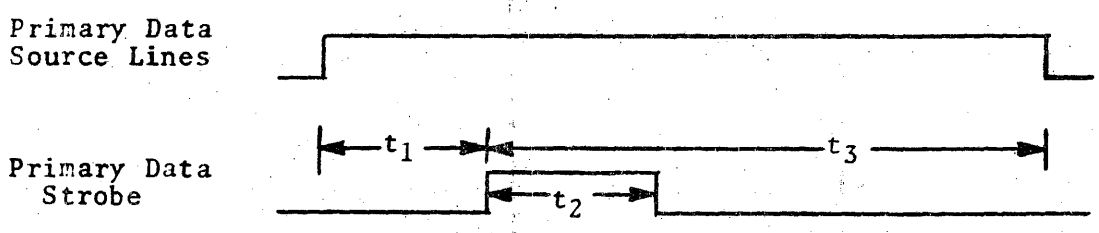


FIGURE 7: EXTENDED REGISTER FILE, GROUP III SIGNAL TIMINC

PRIMARY LOADER DATA TIMING

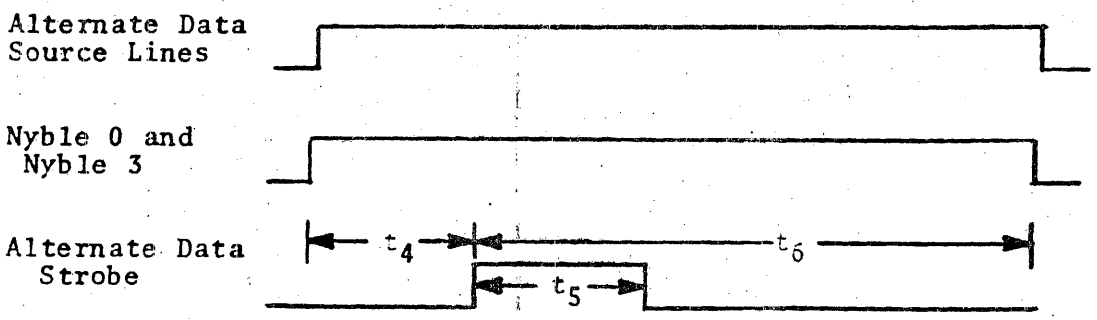


t_1 = 50 nsec minimum

t_2 = 50 nsec minimum

t_3 = 1 usec minimum

ALTERNATE LOADER DATA TIMING



t_4 = 50 nsec minimum

t_5 = 50 nsec minimum

t_6 = 1 usec minimum

FIGURE 8

MNEMONIC	FORMAT	BLOCK-POINT	REGISTER FILE ADDRESSABILITY GROUP I F	GROUP I Pu	GROUP II	GROUP III	MINOR CYCLES MIN.	MAX.
AND	1	X	X	X	X	X	1	1
CIO1		X					1	8
CIO2		X					1	8
CLA	1		X	X	X	X	1	1
CLR	1	X	X	X	X	X	1	1
CMP	1	X	X		X		1	2
CMU	1	X	X		X		1	2
CORC							1	1
DFA	1		X	X	X		1	4
DIG							1	1
DLS							2	2
DRS							2	2
DSUM	1	X	X		X		1	2
DTA	1		X	X	X		1	4
DTA\	1		X	X	X		1	4
EBL							1	1
EBU							1	1
EOR	1	X	X		X	X	1	1
FNJ		X		X			1	2
FRJ		X		X			1	8
FZJ		X		X			1	8
IDX	1		X	X	X		1	4
IOR	1	X	X		X	X	1	1
IVK							1	1
JMP		X		X			1	2
LAB	1		X	X	X	X	1	1
LAW	1		X	X	X	X	1	1
LAW\	1		X	X	X	X	1	1
LBB	3						1	1
LBB\	3						1	1
LBL	1		X	X	X	X	1	1
LBW	1		X	X	X	X	1	1
LBW\	1		X	X	X	X	1	1

FIGURE 9: MICRO-COMMAND CHARACTERISTICS

NOTE: Minor cycle minimums and maximums do not account for special minor cycles of E0′, E0″, E8 and E9.

MNEMONIC	FORMAT	BLOCK-POINT	REGISTER FILE ADDRESSABILITY GROUP I F	GROUP I Pu	GROUP II	GROUP III	MINOR CYCLES MIN.	MAX.
LDB	1		X	X	X	X	1	1
LDW	1		X	X	X	X	1	1
LDW\	1		X	X	X	X	1	1
LSE	1		X	X	X		1	7
LSF	1		X	X	X		1	7
LS1	1		X	X	X		1	7
LS2	1		X	X	X		1	7
NOP							1	1
RNI1		X	X	X	X		1	8
RNI2		X	X	X	X		1	8
ROM		X					3	8
RVK							1	1
SDB	1	X	X		X	X	1	5
SDW	1	X	X		X	X	1	5
SHF							2	2
SHR							2	2
SKB	2	X					1	2
SKB\	2	X					1	2
SKE		X					1	2
SKE\		X					1	2
SKG		X					1	2
SKL		X					1	2
SKN		X					1	2
SKZ		X					1	2
SR0							2	2
SR1							2	2
SS0							2	2
SS1							2	2
STA	1	X	X	X	X	X	1	2
STB	1	X	X	X	X	X	1	2
SUM	1	X	X		X		1	2
SYNC		X					1	8

FIGURE 9: (CONTINUED) MICRO-COMMAND CHARACTERISTICS

NOTE: Minor cycle minimums and maximums do not account for special minor cycles of E0′, E0″, E8 and E9.

FIGURE 10: 7300 CONSOLE-OPERATOR GROUP

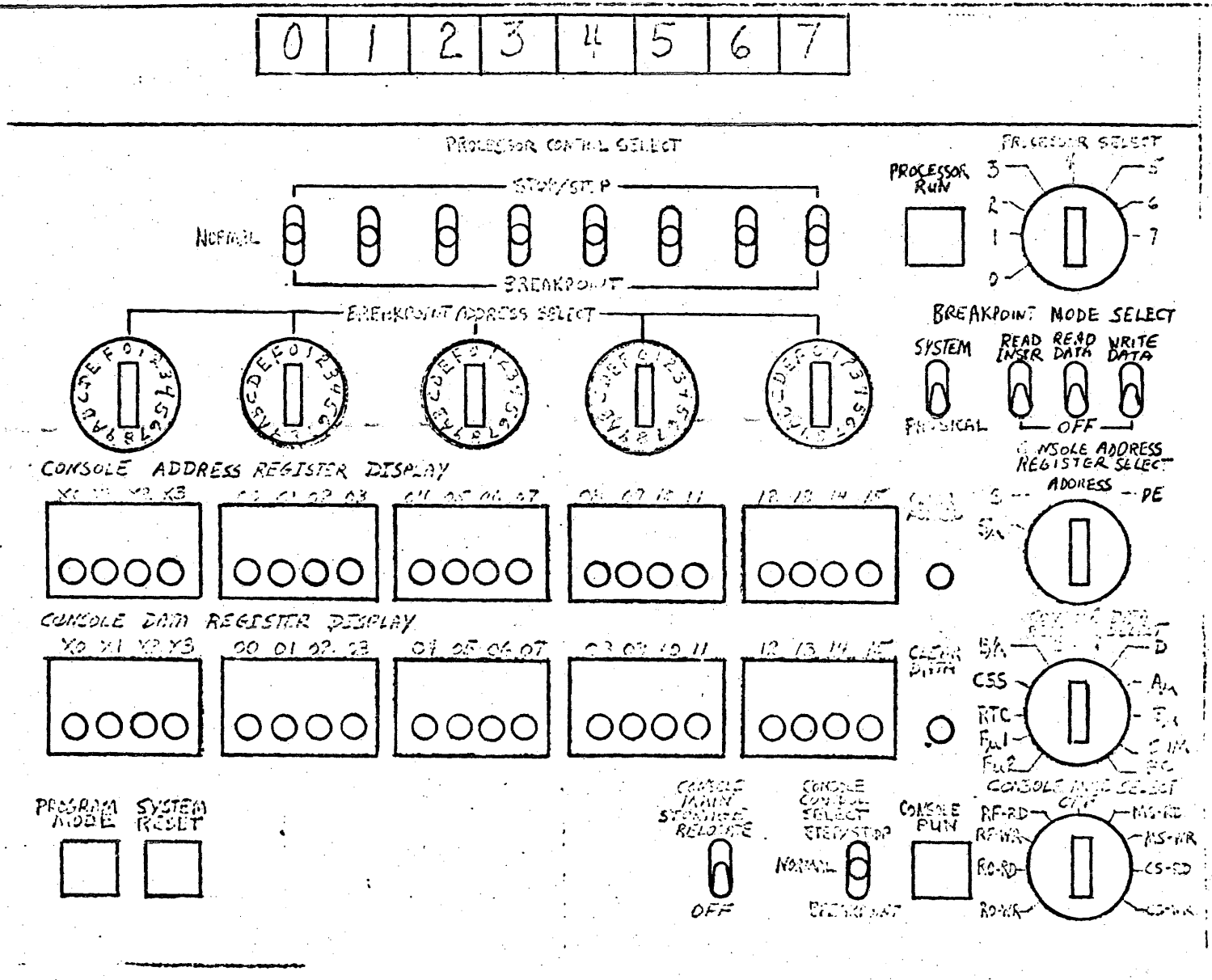


FIGURE 11: 7300 CONSOLE-PROGRAM GROUP

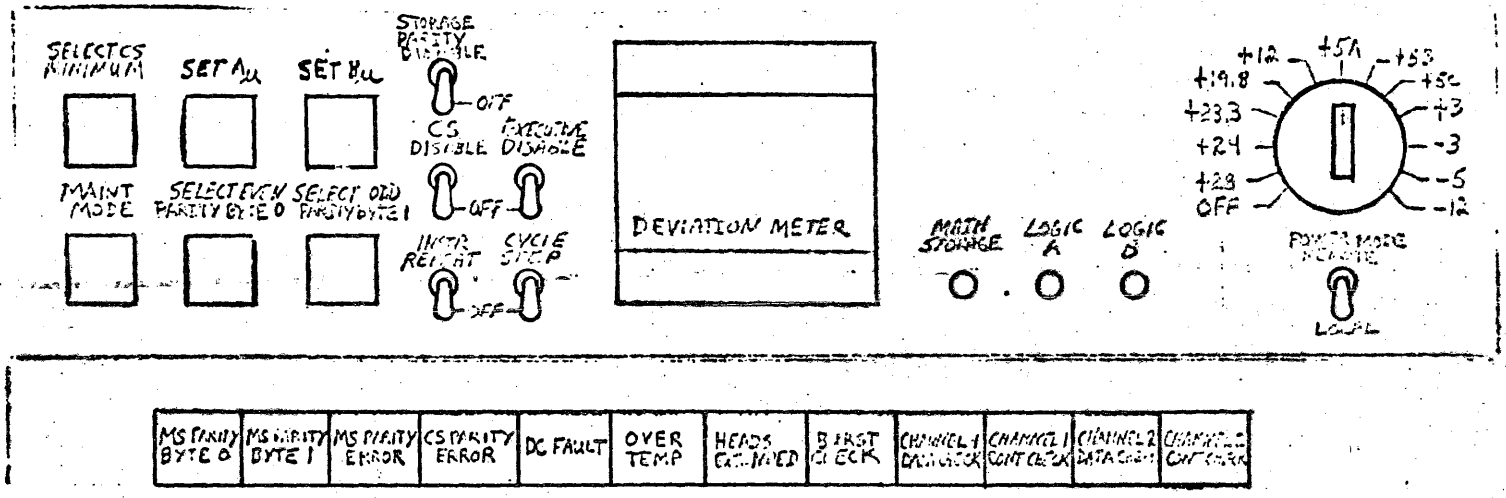


FIGURE 12: 7300 CONSOLE-MAINTENANCE GROUP

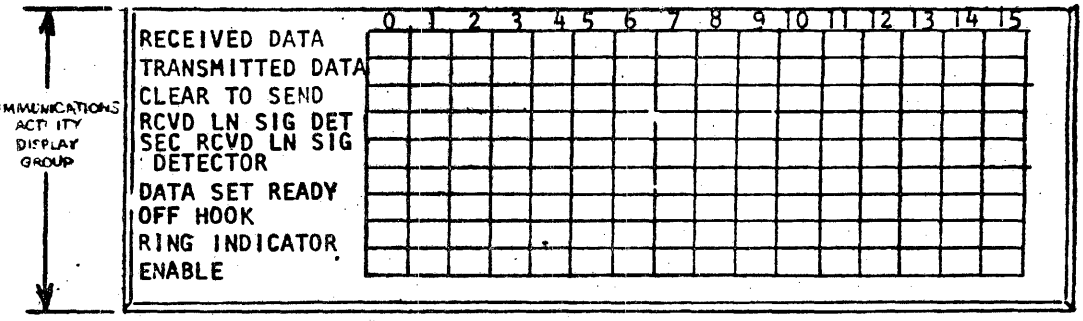


FIGURE 13: 7300 CONSOLE COMMUNICATIONS ACTIVITY DISPLAY GROUP

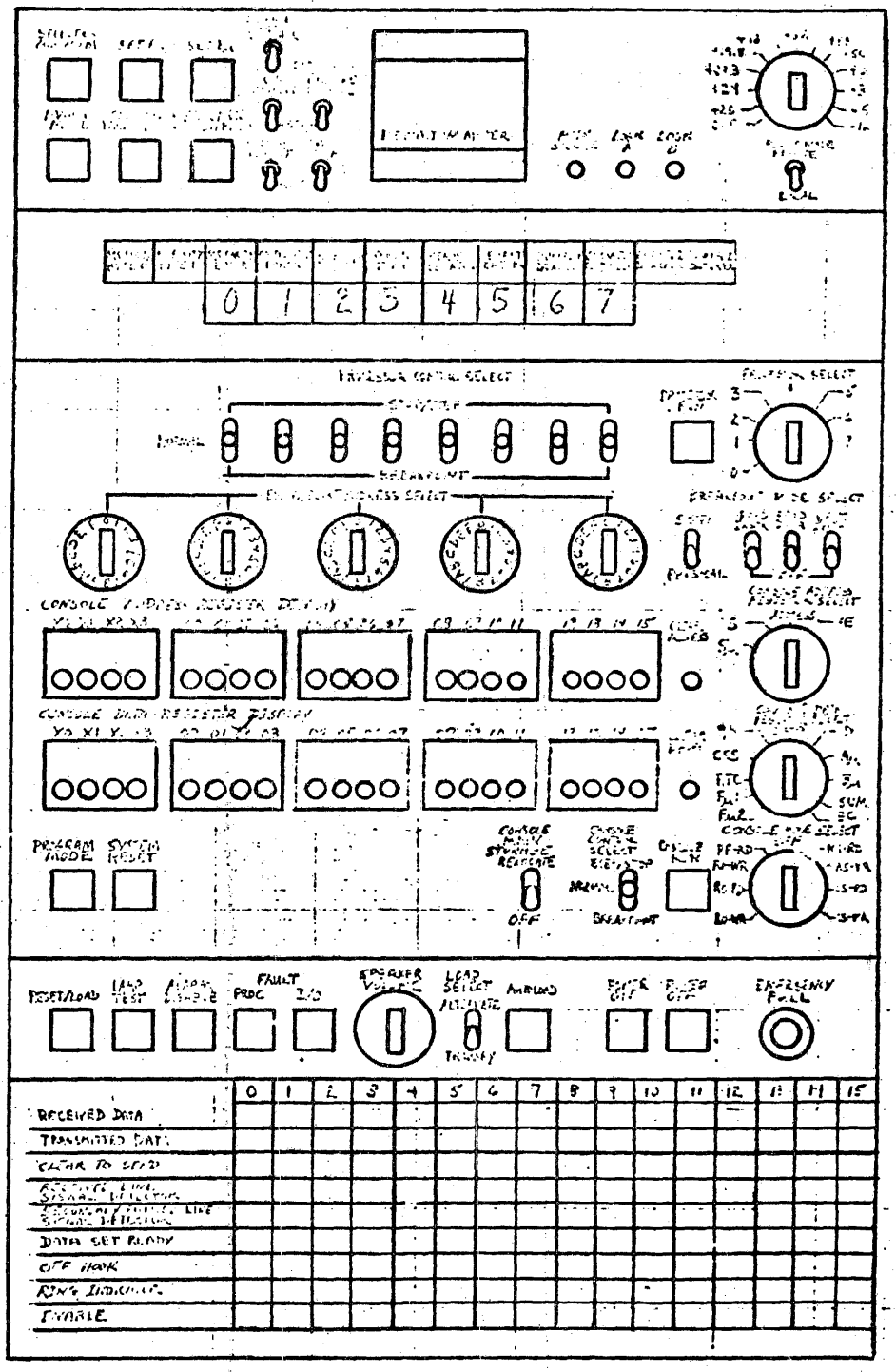


FIGURE 14: 730C CONSOLE

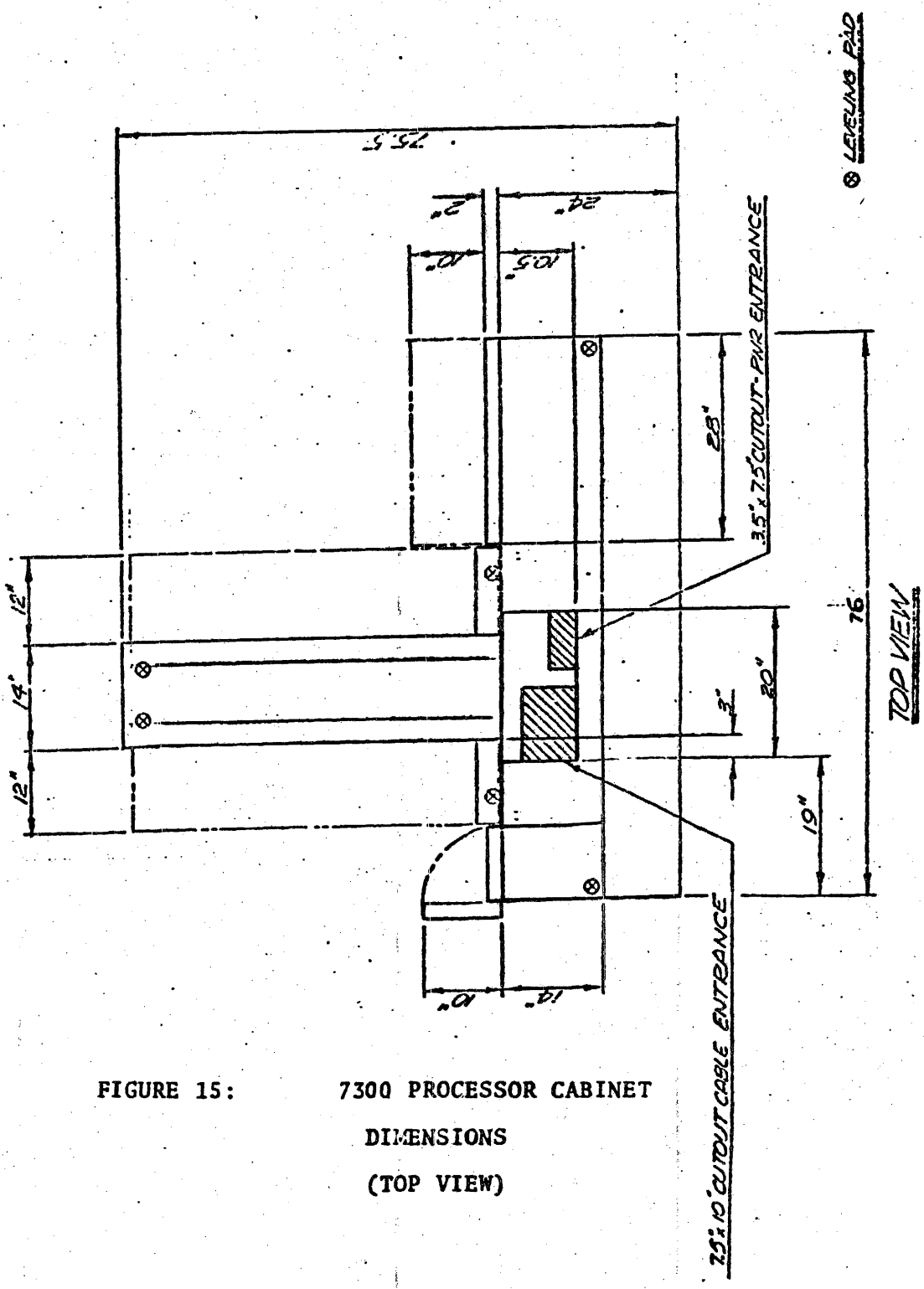


FIGURE 15: 7300 PROCESSOR CABINET DIMENSIONS (TOP VIEW)

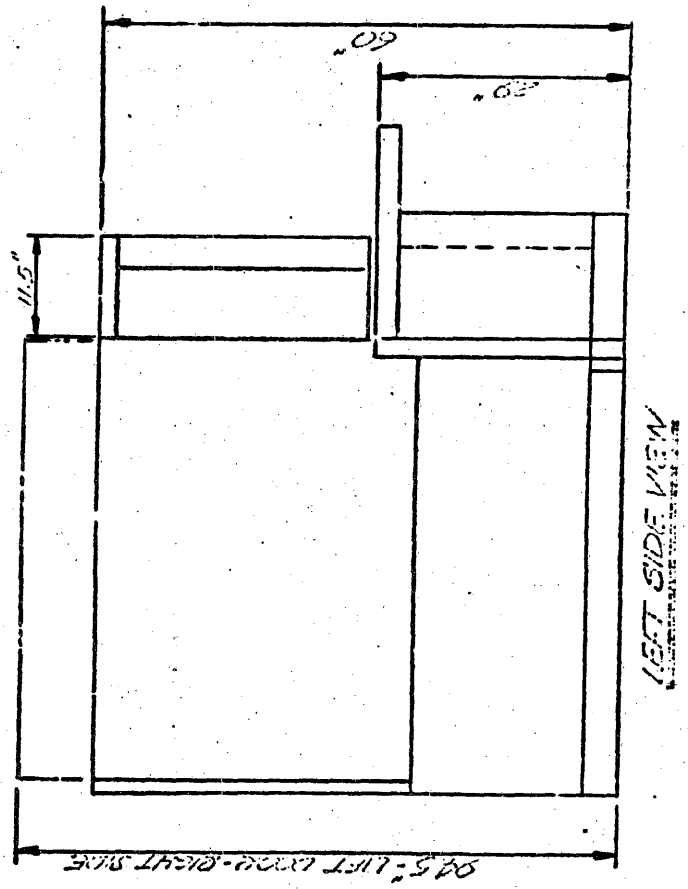


FIGURE 16: 7300 PROCESSOR CABINET DIMENSIONS

(LEFT SIDE VIEW)

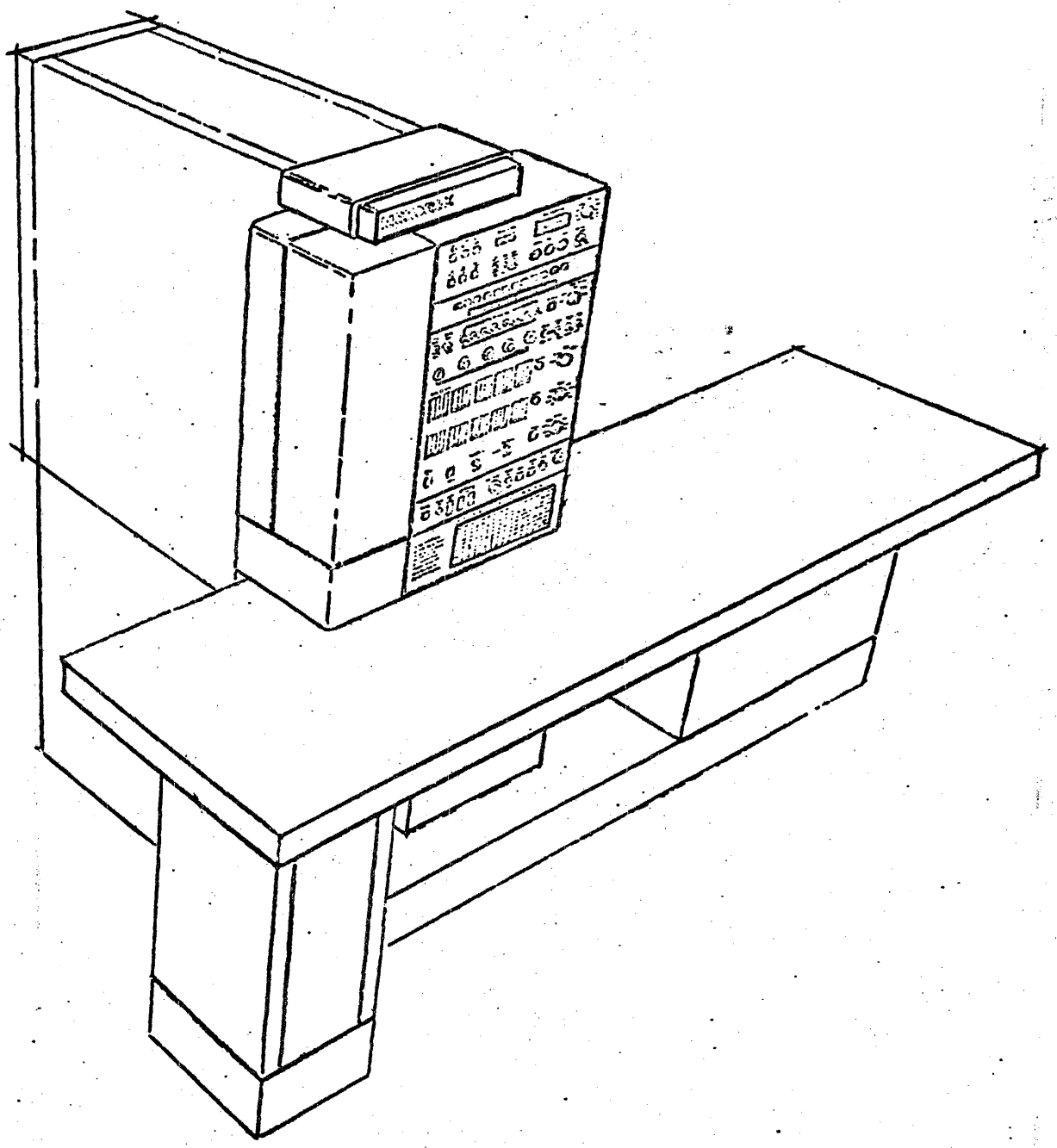


FIGURE 17: 7300 PROCESSOR CABINET: CONCEPT