MLSI-BA11-200X/300X

SERIES OF CHASSIS ASSEMBLIES AND BASIC BOX SYSTEMS

For use with DEC™ LSI-11™ Computers

INSTRUCTION MANUAL

MDB SYSTEMS, INC.

MLSI-BA11-200X/300X

SERIES OF CHASSIS ASSEMBLIES AND BASIC BOX SYSTEMS

For use with DEC™ LSI-11™ Computers

INSTRUCTION MANUAL

MDB
1995 North Batavia Street
Orange, Ca 92613-5508
(714) 998-6900
TWX: 910-953-1339

Document Part Number: 80033664
Document Revision Level: A

WARNING

This equipment generates, uses, and may emit radio frequency energy. If not installed in accordance with the information provided in this instruction manual, it may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense, may be required to take whatever measures are necessary to correct the interference.

The postage-prepaid READER'S COMMENTS page at the end of this instruction manual requests the user's critical evaluation to assist us in preparing future documentation.

Price: $10.00

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

LIST OF TABLES

LIST OF ILLUSTRATIONS

CHAPTER 1

GENERAL DESCRIPTION

1.1 SCOPE OF MANUAL

This instruction manual provides a general description of the MLSI-BA11 Series of Chassis Assemblies which are to be used with the Digital Equipment Corporation LSI-11 family of Q-bus computers.

Included in this manual are descriptions of the backplane/card guide assembly, power fail sequencing circuitry, the power supply, use of the rear distribution panel, and recommended placement of system modules. Also provided are assembly drawings and schematic diagrams to aid in troubleshooting.

1.2 REFERENCE DOCUMENTS

Before configuring a Q-bus-based computer system, it is highly recommended that the you become familiar with LSI-11 operation and Q-bus architecture. The following reference documents may be used in conjunction with this instruction manual to ensure an adequate understanding of system operation.

- DEC Microcomputers and Memories Handbook
- DEC Microcomputer Processor Handbok
- DEC Microcomputer Interfaces Handbook
- DEC Peripherals Handbook

1.3 PRODUCT OVERVIEW

The MLSI-BA11 Series consists of front or rear-loading system chassis assemblies which may be used with Q-bus-based microprocessors and associated interface modules. (Refer to Table 1-1 for a complete list of MLSI-BA11 Model Designations.)

Included with each chassis in the MLSI-BA11 Series is a removable front panel and a backplane/card guide assembly with 22-bit addressing capability and factory installed removable Q-bus termination. The backplane can accommodate sixteen (16) dual-size modules, eight (8) quad-size modules, or a user-selected combination of both dual and quad modules.

Also included is a triple output regulated switching power supply which provides +5V dc at 37 amps, +12V dc at 4 amps, and -12V dc at 1 amp. The chassis are also equipped with three cooling fans which provide 300 cfm of air circulation.

The Switch Control Panel located on the chassis front panel contains three illuminated push-button switches (DC ON, LTC, and HALT) and one indicator (RUN) which manipulate and monitor certain operational functions of the system. The switch panel provides integral ON/OFF power fail sequencing.

The Rear Cable Distribution Panel facilitates the connection of cables between modules installed in the system backplane and user peripheral devices. Cable connections are made internally at the distribution panel bulkhead connectors, with external interface cables installed from the panel to the peripheral devices.

Also mounted on the rear chassis panel is a rocker style AC power ON/OFF circuit breaker switch. AC input power is accomplished by means of a removable 8-foot line cord which is connected to the line filter/voltage selector.

The chassis assembly can be easily mounted in a standard 19-inch RETMA-type cabinet. Slide or rack mounting assemblies may be used.

The overall dimensions of the MLSI-BA11-200X/300X Series of Chassis Assemblies are as follows:

- Height: 5.25 inches (13.34 cm)
- Width: 19.00 inches (48.26 cm)
- Depth: 18.00 inches (45.72 cm)
- Weight: 30.00 pounds (13.60 kg)

Table 1-1 provides a complete list of the various configurations of the MLSI-BA11-200X/300X Series.

Table 1-1
MLSI-BA11-2000 Model Designations

Model Number	AC Input Power	Module Loading
MLSI-BA11-2000-F	110 VAC, 50/60 Hz	Front
MLSI-BA11-2000-R	110 VAC, 50/60 Hz	Rear
MLSI-BA11-2002-F	220 VAC, 50/60 Hz	Front
MLSI-BA11-2002-R	220 VAC, 50/60 Hz	Rear

MLSI-BA11-3000 Model Designations

Model Number	AC Input Power	Module Loading
MLSI-BA11-3000-F	110 VAC, 50/60 Hz	Front
MLSI-BA11-3000-R	110 VAC, 50/60 Hz	Rear
MLSI-BA11-3002-F	220 VAC, 50/60 Hz	Front
MLSI-BA11-3002-R	220 VAC, 50/60 Hz	Rear

AC Input Power is also commonly referred to as 115 VAC and 230 VAC.

CHAPTER 2

Q-BUS BACKPLANE CONFIGURATION

2.1 INTRODUCTION

This chapter describes the backplane/card guide assembly utilized in the MLSI-BA11 Series of Chassis Assemblies. Designated the MLSI-BPA84-E-F/R, the backplane is wired for standard LSI-11 Q-bus signals, and is equipped with full 22-bit addressing capability. The assembly is also provided with full-length card guides to ensure maximum support for the modules installed in the backplane.

Provided in this chapter is information pertaining to the configuration and use of the MLSI-BPA84-E Backplane/Card Guide Assembly, and a complete list of Q-bus signals.

2.2 MLSI-BPA84-E-F/R BACKPLANE CARD GUIDE ASSEMBLY

The MLSI-BPA84-E-F/R Backplane Card Guide Assembly is a pre-wired, multilayer, printed circuit LSI-11 backplane which provides sixteen (16) dual or eight (8) quad standard Q-bus slots. These slots will accommodate a total of 16 dual-size modules, 8 quad-size modules, or a user-selected combination of both dual and quad modules.

For example, a quad-size LSI-11/23-PLUS CPU (KDF11-BA) and 14 dual-size modules may be installed in the backplane. The backplane may also be used with LSI-11/23 (KDF11-AA), LSI-11/2 (KD11-HA), or LSI-11 (KD11-F) microprocessors.

The overall dimensions of the MLSI-BPA84-E-F/R Backplane Card/Guide Assembly are as follows:

NOTE

Since all slots have 22-bit addressing, KDJ11-BF and PMI memory must not be installed in the backplane.

2.4 DEC-COMPATIBLE MODULES

The MLSI-BPA84-E Backplane will accommodate sixteen dual-size, eight quad-size DEC-compatible modules, or a user-selected combination of both. Figure 2-3 provides pin assignments for DEC-compatible modules, and Table 2-1 lists required module dimensions.

Figure 2-3
DEC-Compatible Module Pin Assignments

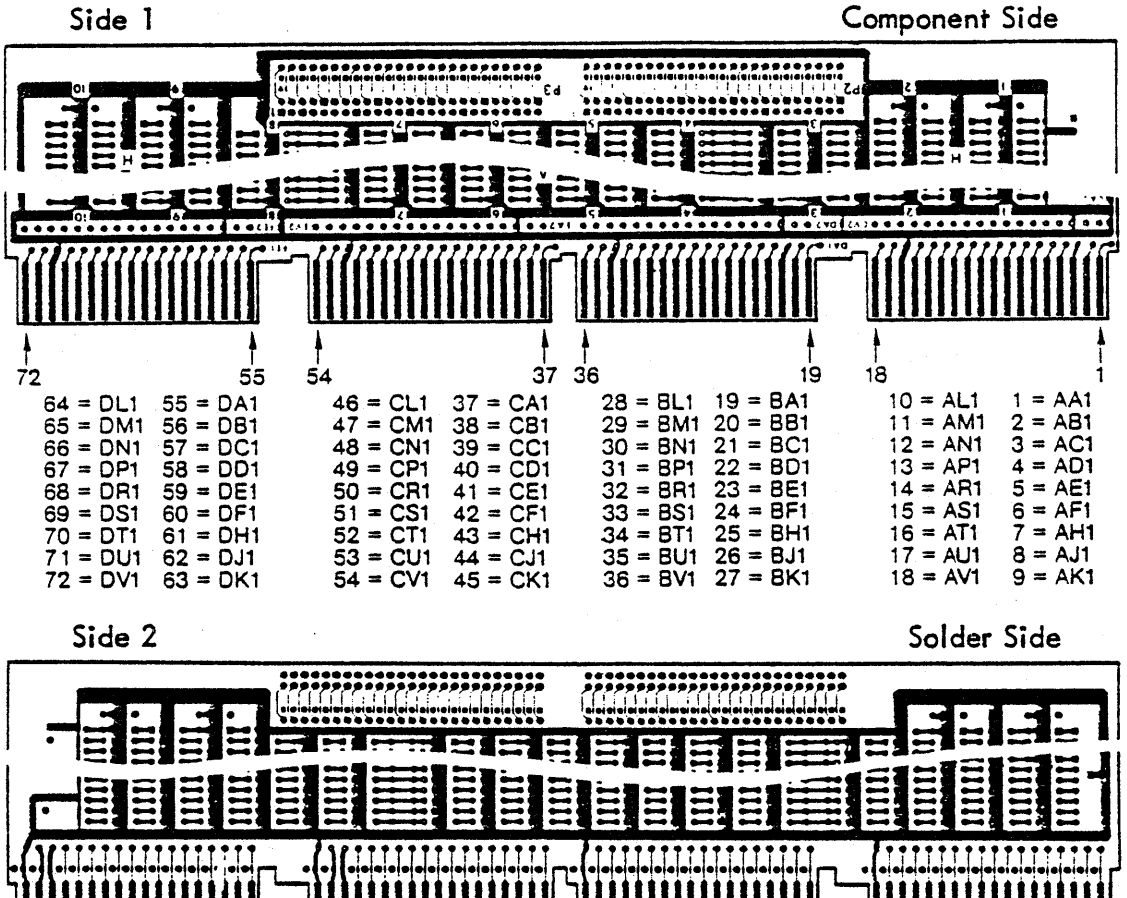


Table 2-1
DEC-Compatible Module Dimensions

Module Size	Height	Width
Quad	8.42" (21.40 cm)	10.44" (26.50 cm)
Dual	8.42" (21.40 cm)	5.20" (13.20 cm)
Single	8.42" (21.40 cm)	2.44" (6.20 cm)

2.5 Q-BUS BACKPLANE INTERFACE SIGNALS

Table 2-2 lists and defines signals present at the LSI-11 Q-bus backplane/module interface. Most Q-bus signals are active (true) when at a low level (0 volts), and are inactive (false) when at a high level (+3 volts). However, bus signals BDCOK H and BPOK H are active when high, and are noted as such in the following table.

For more detailed information regarding interface signals and timing, refer to the DEC Microcomputers and Memories Handbook or Microcomputer Processor Handbook.

Table 2-2
Q-bus Backplane Interface Signals

Bus Pin	Mneumonic	Description
AA1 (CA1)	BIRQ5 L	Priority Level 5 Interrupt Request.
AB1 (CB1)	BIRQ6 L	Priority Level 6 Interrupt Request.
AC1 (CC1)	BDAL16 L	Extended address bit 16.
AD1 (CD1)	BDAL17 L	Extended address bit 17.
AE1 (CE1)	SSPARE	Spare pin, not assigned on the backplane; available for user connection.
AF1 (CF1)	SRUN L	Run light signal.
AH1 (CH1)	SRUN L	Run light signal.

(continued)

Table 2-2
Q-bus Backplane Interface Signals (continued)

Bus Pin	Mneumonic	Description
AJ1 (CJ1)	GND	Signal ground.
AK1 (CK1)	MSPAREA	Maintenance spare. Normally connected to bus pin AL1 (CL1) on the backplane.
AL1 (CL1)	MSPAREA	Maintenance spare. Normally connected to bus pin AK1 (CK1) on the backplane.
AM1 (CM1)	GND	Signal ground.
AN1 (CN1)	BDMR L	Direct Memory Access (DMA) Request. Asserted by a device to request control of the bus (bus mastership). If the processor is not the bus master, nor asserting BSYNC L, it grants bus master status to the requesting device by asserting the signal BDMGO L. The requesting device responds by negating BDMR L and asserting BSACK L.
AP1 (CP1)	BHALT L	Processor Halt. A device will cause the processor to halt normal program execution by asserting BHALT L.
AR1 (CR1)	BREF L	Memory Refresh. When BREF L is asserted, the processor will perform a memory refresh that forces all dynamic memory devices to be activated for each BSYNC L/ BDIN L bus transaction.
AS1 (CS1)	+ 12B	+ 12 V dc battery power.
AT1 (CT1)	GND	Signal ground.

(continued)

Table 2-2
Q-bus Backplane Interface Signals (continued)

Bus Pin	Mneumonic	Description
AU1 (CU1)	PSPARE	Power spare, not assigned. This pin is not recommended for use.
AV1 (CV1)	+ 5B	+ 5 V battery power.
AA2 (CA2)	+ 5V	+ 5 V dc power.
AB2 (CB2)	- 12V	- 12 V dc power.
AC2 (CC2)	GND	Signal ground.
AD2 (CD2)	+ 12V	+ 12 V dc power.
AE2 (CE2)	BDOUT L	Data Output. Implies that valid data is available on bus lines BDAL00 L through BDAL15 L and, with reference to the bus master device, that an output transfer is in process. The slave device that responds to the BDOUT L signal must assert BRPLY L to complete the data transfer.
AF2 (CF2)	BRPLY L	Reply. Asserted in response to BDIN L or BDOUT L. The signal indicates that input data is available on the BDAL bus, or that output data has been accepted from the bus.
AH2 (CH2)	BDIN L	Data Input. When BSYNC L is asserted, BDIN L indicates an input transfer from the active bus master. When the signal BSYNC L is not asserted, it implies that an interrupt operation is in process.

(continued)

Table 2-2
Q-bus Backplane Interface Signals (continued)

Bus Pin	Mneumonic	Description
AJ2 (CJ2)	BSYNC L	Synchronize. Asserted by the bus master device when it has placed an address on bus lines BDAL00 L through BDAL21 L.
AK2 (CK2)	BWTBT L	Write/Byte. Controls the bus cycle in either of two ways, as follows: 1. Asserted with leading edge of BSYNC L to indicate that an output sequence will follow (DATO or DATOB). 2. Asserted, while BDOUT L is asserted, for byte addressing in a DATOB cycle.
AL2 (CL2)	BIRQ4 L	Priority Level 4 Interrupt Request.
AM2 (CM2)	BIAKI L	Interrupt Acknowledge. This signal is asserted by the processor in response to the signal BIRQ L. Causes the device to put an interrupt vector on the bus.
AN2 (CN2)	BIAKO L	Interrupt Acknowledge Out. Normally asserted to the device having the next-lower priority on the interrupt daisy-chain, and appears at BIAKI L input to the device. If the module stores an interrupt request BIAKO L is negated at the next device.

(continued)

Table 2-2
Q-bus Backplane Interface Signals (continued)

Bus Pin	Mneumonic	Description
AP2 (CP2)	BBS7 L	Bank 7 Select. Indicates that the address on the bus is for the upper 4K bank. When BSYNC L is asserted, BBS7 L will remain active until the addressing of the bus cycle is completed.
AR2 (CR2)	BDMGI L	DMA Bus Grant Input.
AS2 (CS2)	BDMGO L	DMA Bus Grant Output. This processor-generated signal is daisy-chained through all DMA devices on the bus. When asserted, the signal BDMGI L grants bus master status to the DMA device requesting the bus that has the highest priority. If a higher-priority DMA device has no active bus request, BDMGO L passes from that device to the BDMGI L input of the next DMA device. If the higher-priority device has an active bus request, that device inhibits its BDMGO L output. A DMA device requests the bus by asserting BDMR L.
AT2 (CT2)	BINIT L	Initialize. This signal is generated by the processor during a power-up or reset operation. BINIT L clears all devices on the I/O bus.
AU2 (CU2)	BDAL00 L	Bit 0. One of the data/address bus lines used to transfer all address and data information. This signal is bidirectional.
AV2 (CV2)	BDAL01 L	Bit 1. Data/Address bit.

(continued)

Table 2-2
Q-bus Backplane Interface Signals (continued)

Bus Pin	Mneumonic	Description
BA1 (DA1)	BDCOK H	DC Power OK. Asserted when the system dc voltage level is suitable for reliable system operation. BDCOK H is active when high.
BB1 (DB1)	BPOK H	AC Power OK. Asserted when primary power is within limits assuring reliable system operation. BPOK H is active when high.
BC1 (DC1)	BDAL18 L	Bit 18. One of the extended address bus lines used to transfer address information.
BD1 (DD1)	BDAL19 L	Extended address bit 19.
BE1 (DE1)	BDAL20 L	Extended address bit 20.
BF1 (DF1)	BDAL21 L	Extended address bit 21.
BH1 (DH1)	SSPARE	Special spare pin that is not assigned; available for user connection.
BJ1 (DJ1)	GND	Signal ground.
BK1 (DK1)	MSPAREB	Maintenance spare. Normally connected to bus pin BL1 (DL1) on the backplane.
BL1 (DL1)	MSPAREB	Maintenance spare. Normally connected to bus pin BK1 (DK1) on the backplane.
BM1 (DM1)	GND	Signal ground.
BN1 (DN1)	BSACK L	Bus Grant Acknowledge. This signal is asserted by a DMA device in response to the processor's BDMGO L signal, indicating that the device is now the bus master.

(continued)

Table 2-2
Q-bus Backplane Interface Signals (continued)

Bus Pin	Mneumonic	Description
BP1 (DP1)	BIRQ7 L	Priority Level 7 Interrupt Request.
BR1 (DR1)	BEVNT L	External Event Interrupt Request. Using BEVNT L, Line Time Clock interrupts occur every 16 2/3 msec for a 60 Hz line frequency, and every 20 msec for a 50 Hz line frequency.
BS1 (DS1)	+ 12B	+ 12 V battery power.
BT1 (DT1)	GND	Signal ground.
BU1 (DU1)	PSPARE	Power spare, not assigned. This pin is not recommended for use.
BV1 (DV1)	+ 5V	+ 5 V dc power.
BA2 (DA2)	+ 5V	+ 5 V dc power.
BB2 (DB2)	- 12V	- 12 V dc power.
BC2 (DC2)	GND	Signal ground.
BD2 (DD2)	+ 12V	+ 12 V dc power.
BE2 (DE2)	BDAL02 L	Bit 2. One of the data/address bus lines used to transfer all address and data information. This signal is bidirectional.
BF2 (DF2)	BDAL03 L	Bit 3. Data/Address bit.
BH2 (DH2)	BDAL04 L	Bit 4. Data/Address bit.
BJ2 (DJ2)	BDAL05 L	Bit 5. Data/Address bit.
BK2 (DK2)	BDAL06 L	Bit 6. Data/Address bit.
BL2 (DL2)	BDAL07 L	Bit 7. Data/Address bit.

(continued)

Table 2-2
Q-bus Backplane Interface Signals (continued)

Bus Pin	Mneumonic	Description
BM2 (DM2)	BDAL08 L	Bit 8. Data/Address bit.
BN2 (DN2)	BDAL09 L	Bit 9. Data/Address bit.
BP2 (DP2)	BDAL10 L	Bit 10. Data/Address bit.
BR2 (DR2)	BDAL11 L	Bit 11. Data/Address bit.
BS2 (DS2)	BDAL12 L	Bit 12. Data/Address bit.
BT2 (DT2)	BDAL13 L	Bit 13. Data/Address bit.
BU2 (DU2)	BDAL14 L	Bit 14. Data/Address bit.
BV2 (DV2)	BDAL15 L	Bit 15. Data/Address bit.

CHAPTER 3

SWITCH/INDICATOR CONTROL PANEL

3.1 INTRODUCTION

This chapter describes the proper operation, function, and adjustment of the Switch/Indicator Control Panel utilized in the MLSI-BAll Series of Chassis Assemblies.

3.2 SWITCH/INDICATOR CONTROL PANEL

The Switch/Indicator Control Panel is a complete subassembly consisting of a printed circuit board (MLSI-PSM23 Power Sequencing Module), switches and lighted indicators, and a mounting panel.

The Control Panel manipulates the operation of the Micro/11 system by use of switches. It monitors, via lighted displays, certain operational functions of the system including DC ON, RUN, LTC, and HALT. In addition, the Power Sequencing Module continuously monitors power supply voltages to ensure reliable computer operation.

The MLSI-PSM23 is designed to monitor AC line voltage and DC power and cause a power-down sequence to occur if the voltages fall below the following parameters:

AC Voltage	+12 VDC	+5 VDC
98 V	11.3 V	4.6 V

Upon detection of voltages outside of the specified parameters, the Power Sequencing Module will initiate a power-down sequence as shown in Figure 3-2, indicating voltage abnormalities.

The Switch/Indicator Control Panel is electrically connected to the power supply and the chassis backplane via removable flat cables.

The Power Sequencing Module requires dc power from the power supply, as follows:

- +5 volts dc at 51 milliamps
- +12 volts dc at 1.2 milliamps

Figure 3-1 shows the location of the Control Panel switches and indicators. Table 3-1 lists and defines the function of each switch and indicator on the panel.

Figure 3-1
Switch/Indicator Control Panel

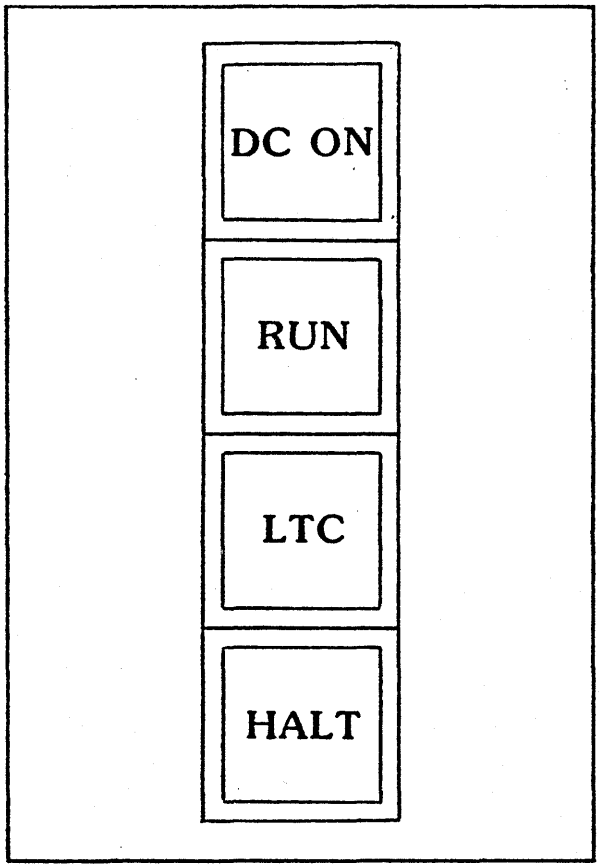


Table 3-1
Function of Control Panel Switches and Indicators

Switch/Lamp	Position	Function
DC ON*	On (Lamp On)	When the DC ON switch is depressed, a power-down sequence is initiated, which, in turn, causes the CPU to assert the signal BINIT L on the bus (Q-bus is initialized). When the DC ON switch is released, a power-up sequence is initiated. The illuminated DC ON lamp indicates that AC and DC voltages are at acceptable levels.
	(Lamp Off)	When the DC ON indicator is off, it indicates that AC and DC voltages are not at acceptable levels, and a power fail sequence is initiated.
RUN (Lamp only)	Lamp On	When the RUN indicator is illuminated, it signifies that the processor is executing a program. The RUN indicator turns off 200 microseconds after program execution is completed.
	Lamp Off	When off, the indicator signifies that the CPU is not executing programs.
LTC	On (Lamp On)	When the LTC switch is depressed and locked, the Line Time Clock feature is activated, asserting and negating the BEVNTL interrupt line at a 50 Hz or 60 Hz rate.
	Off (Lamp Off)	Disables the switchable LTC feature. (This switch does not effect the programmable LTC on the CPU.

(continued)

Table 3-1
Function of Control Panel Switches and Indicators (cont.)

Switch/Lamp	Position	Function
HALT	On (Lamp On)	When the HALT switch is depressed and locked, the signal BHALT L is asserted on the bus by the Control Panel. This switch halts execution of the current program without powering-down the system. The processor executes the ODT microcode and a single instruction for each "P" keystroke on the console terminal keyboard.
	Off (Lamp Off)	Negates the signal BHALT L to allow the processor to resume normal program execution.

* The function of the DC ON switch may be altered slightly by reconfiguring a jumper on the MLSI-PSM23 module. As configured at the factory (jumper B-C installed), the DC ON switch will function as described in Table 3-1. However, if jumper B-C is removed and jumper A-C is installed, the DC ON switch may be used to toggle the BDCOK H line ONLY, and will have no effect upon the BPOK H line. Consequently, a normal power-up sequence will NOT be initiated when the DC ON switch is activated. The reason for this particular configuration is that some controllers initialize when the signal BDCOK H is encountered.

NOTE

The HALT and LTC indicators do not specify a halt or line time clock activity that has been asserted on the bus by another module. These Switch Control Panel indicators represent only a HALT or LTC activity that has been directly asserted by the Power Sequencing Module/Switch Control Panel.

3.3 THEORY OF OPERATION

The following paragraphs describe the theory of operation of the Power Sequencing Module in terms of logic diagram #44040372 contained at the end of this manual.

3.3.1 AC Voltage Detector (BPOK H)

After AC power is turned on, a 24 VAC reference voltage originating from a transformer mounted within the power supply enclosure (AC1, AC2) is rectified and the resulting half-cycles appear at voltage comparator 2K(R). This circuit compares the sample AC voltage with a 2.4V or 2.6V reference at 2K(R)-3.

The first, and subsequent half-cycles of the normal line voltage sample causes the output of comparator 2K(R) to be a pulse having an interval of 8.35-milliseconds. This is one-half the AC input line frequency at 60 Hz. (A 50 Hz input would have a pulse interval of 10-milliseconds.) This pulse triggers a re-triggerable one-shot having a period of 12-milliseconds.

The resulting signal ACOK is ANDed with DCOK and triggers an 80-millisecond one-shot. After the 80-millisecond period, the output of this one-shot clocks the POK flip-flop, asserting the signal BPOK H to indicate normal AC voltage levels.

3.3.2 DC Voltage Detector (BDCOK H)

The +12V dc and +5V dc supply bus voltages are monitored by voltage comparators 2F(R) and 2F(L), which compare the bus voltage with a 1.8 volt reference at 2F-3. If the voltage on the +5V dc bus falls below 4.6V dc, or if the +12V dc bus falls below 11.3V dc, the output of 2F(R) or 2F(L) goes low and clears POK flip-flop 2A. This causes optical isolator 1B to stop conducting, which enables FET Q1 to conduct, which deasserts the signal BPOK H.

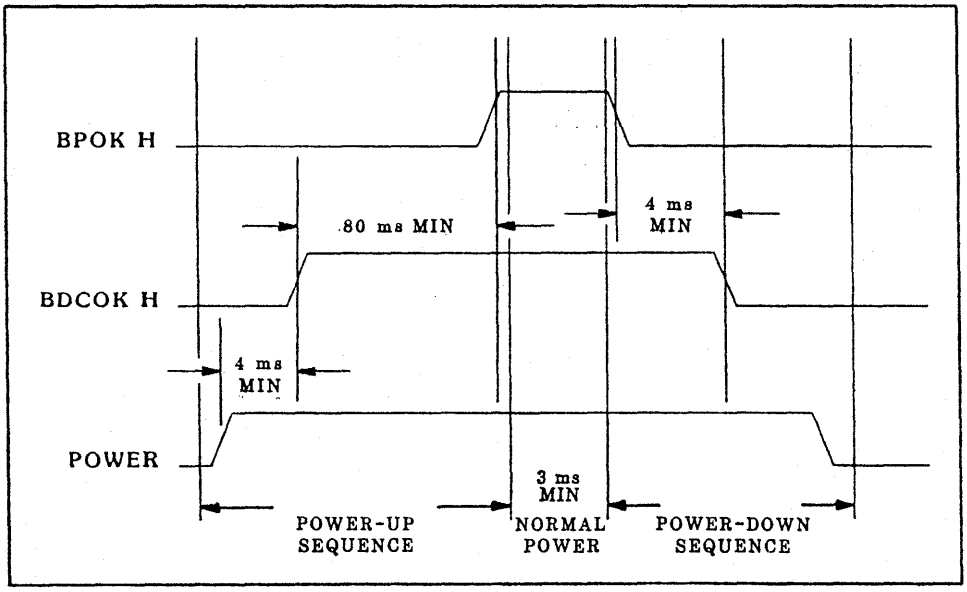
When POK goes low, a pulse appears at 2C-11, which triggers 2C (4-millisecond one-shot). After 4-milliseconds, DCOK deasserts, causing optical isolator 1C to stop conducting which, in turn, causes FET Q2 to conduct and deassert the signal BDCOK H.

Upon power-up, the output of comparator 2F(R) and 2F(L) go high and are ANDed with ACOK, triggering 2C. After the 4-millisecond delay, DCOK is set, which applies BDCOK H to the bus via the optical isolator and FET.

The DC ON indicator is illuminated by the assertion of the signal DCOK.

Figure 3-2 is a simplified timing diagram which illustrates the PSM power-up/power-down sequence in relation to the AC and DC Voltage Detectors.

Figure 3-2
PSM Power-Up/Power-Down Timing Diagram



3.3.3 RUN Indicator

Whenever the processor is in the RUN mode and executing programs, a train of pulses having intervals of 3 to 5 milliseconds appears on the SRUN L line. These pulses trigger a re-triggerable one-shot having a period of 200-milliseconds. While the pulses are present, and for 200-milliseconds after the pulses are removed, the RUNLIT line remains asserted to illuminate the RUN indicator on the Control Panel.

200 msec after the processor is placed in the HALT mode, or power is turned off, the one-shot reverts to its stable state, causing the RUNLIT line to deassert and turn off the RUN indicator.

3.3.4 HALT Control

When the HALT switch on Control Panel is set to the normal position (switch out, indicator off), the signal BHALT L is deasserted on the bus and the processor is free to resume normal program execution.

When the switch is depressed and locked (indicator on), the signal BHALT L is asserted on the bus, placing the system in the HALT mode and causing the processor to execute the console ODT mode.

NOTE

In the HALT mode, the processor will continue to execute memory refresh operations and respond to DMA requests.

The cross-coupled inverters 2H-8 and 2H-6 remove the effects of switch bounce when the HALT switch is operated.

3.3.5 Line Time Clock

The Power Sequencing Module can enable the generation of the signal BEVNT L as a periodic interrupt at the frequency of the AC input power source (i.e., 50 Hz or 60 Hz). This serves as the Line Time Clock signal.

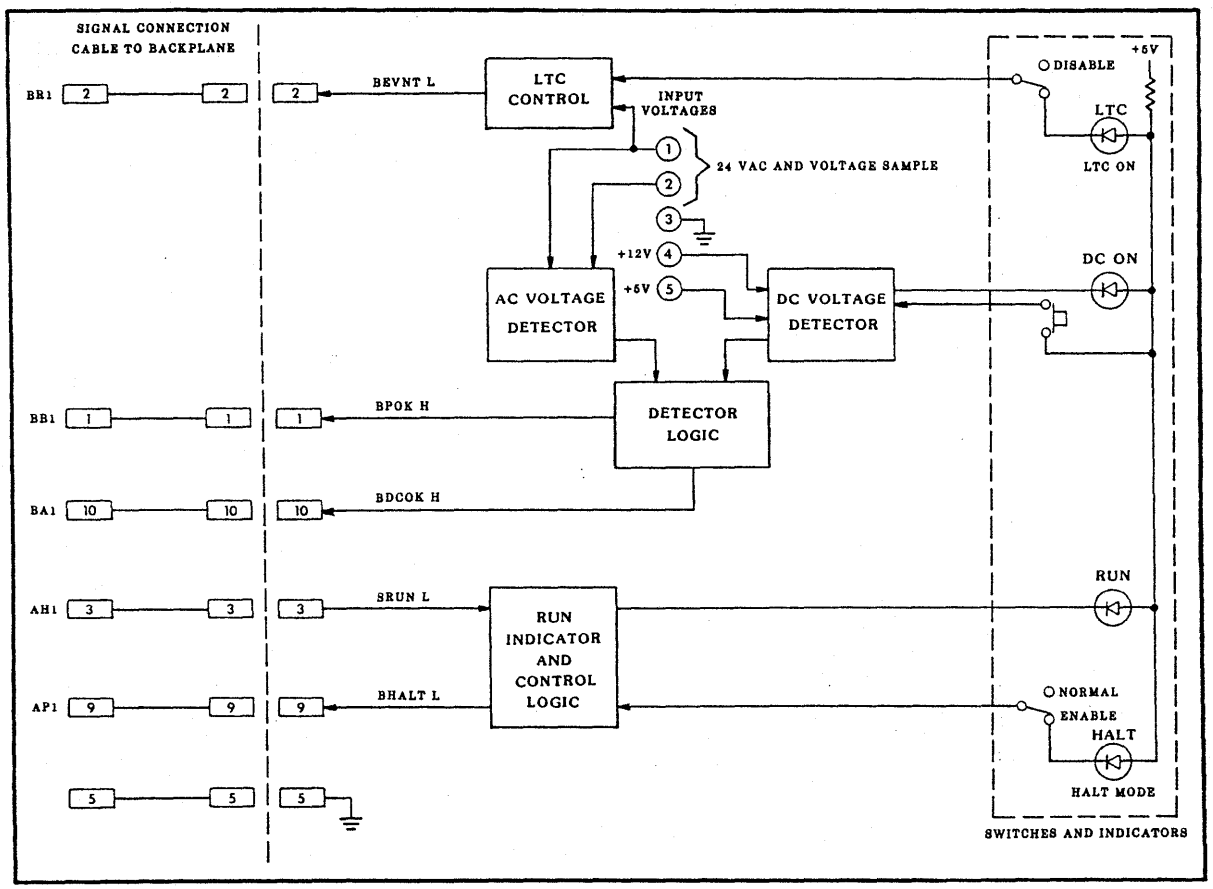
One side of a 24 VAC voltage reference is half-wave rectified by CR10 and shaped by components CR9, C11, and R31, creating a pulse that occurs every 16 2/3 msec for a 60 Hz line frequency, and every 20 msec for a 50 Hz line frequency. This pulse is applied to driver 2K(L), creating the signal BEVNT L.

When the LTC switch on the Control Panel is set to the normal position (LTC disabled, indicator off), the signal BEVNT L is always high. When the LTC switch is depressed and locked, the Line Time Clock is enabled and the LTC indicator is illuminated.

The cross-coupled inverters 2H-1 and 2H-4 remove the effects of switch bounce when the LTC switch is operated.

Figure 3-3 illustrates the general functional organization of circuitry on the MLSI-PSM23 module.

Figure 3-3
Power Sequencing Module, Simplified Block Diagram



3.4 PSM ADJUSTMENT PROCEDURES

The Power Sequencing Module is calibrated and adjusted at the factory prior to shipment; therefore, no periodic checks or adjustments are required. However, should the module or individual components ever need to be replaced in the field, it may be necessary to readjust the AC and DC voltage monitoring circuits. Adjustment procedures are described in the following paragraphs.

The following test equipment is required to perform adjustments on the Power Sequencing Module:

1. AC/DC Voltmeter (Digital preferred).
2. AC Variable Transformer (Variac or equivalent).

With the appropriate test equipment, adjust the Power Sequencing Module as follows:

1. Remove all printed circuit boards from the backplane assembly.

2. Connect the AC line cord from the chassis to the AC variable transformer.

3. Connect the AC voltmeter across the variable transformer output.

4. Apply AC power to the chassis and adjust the variable transformer to 98 VAC for a 115 VAC input voltage (185 VAC for a 230 VAC input voltage).

5. At this time, the DC ON indicator on the Switch Control Panel may or may not be lighted. If the indicator is off, adjust potentiometer R40 on the MLSI-PSM23 module until the DC ON turns on.

6. Then, adjust R40 again until the DC ON indicator just goes out.

7. Check the voltmeter to verify that the AC voltage is at 98 volts +.2V or -.5V when the DC ON indicator turns off. (For 230 VAC operation, the AC voltage observed on the voltmeter should be 185 volts ±.5V.)

8. Then, adjust the AC voltage up to 106 volts ±.5V (201 volts ±1V for 230 VAC operation). At this voltage, the DC ON indicator should illuminate, and should remain lighted as the AC voltage is adjusted to approximately 115 volts (230 volts for 230 VAC operation).

CHAPTER 4

THE POWER SUPPLY

4.1 INTRODUCTION

This chapter provides a description of the power supply utilized in the MLSI-BA11 Series of Chassis Assemblies. Also included are necessary procedures for converting the chassis for an AC input voltage different from that configured at the factory.

4.2 THE POWER SUPPLY

The power supply is a regulated switching power supply which provides three dc output voltages. Refer to the power supply schematic diagram (#99-0013-001) contained at the end of this instruction manual for details. Power supply specifications are provided in Table 4-1.

Table 4-1
Power Supply Specifications

Output Voltage	+5V dc	+12V dc	-12V dc
Current	37 amps	4 amps	1 amp
Line Regulation	0.2 %	0.2 %	0.2 %
Load Regulation	0.2 %	±0.5 %	±0.5 %
Ripple and Noise	50 mV P-P	100 mV P-P	100 mV P-P

(continued)

Table 4-1
Power Supply Specifications (continued)

Input Voltage: 90 - 132 VAC 180 - 264 VAC	
Input Frequency: 47 - 440 Hz	
Operating Temperature: 0 - 50 degrees Celsius	
Height: 2.50" (6.60 cm)	Width: 5.00" (8.25 cm)
Length: 13.50" (40.40 cm)	Weight: 5.5 lbs. (2.5 kg)

The power supply is factory-configured for the required input voltage, either 115 VAC or 230 VAC, depending upon the model designation specified at the time of order. (Refer to Table 1-1 for a complete list of the available MLSI-BAll Series Model Designations.)

The power supply is protected by a fuse and circuit breaker which is integral to the AC ON/OFF switch. These items are all located on the rear panel of the system chassis. For use with 115 VAC input voltage, the fuse is rated for 5.0 amperes; for use with 230 VAC input voltage, the fuse is rated for 2.5 amperes.

In addition to the protective input fuse on the chassis rear panel, the power supply is provided with a completely self-contained 5.0 amp fuse, which is used for either 115 VAC or 230 VAC input voltage.

IMPORTANT NOTES

1. For proper voltage operation, the power supply must always be connected to the Power Sequencing Module, which serves as the essential voltage load for the power supply.

2. To ensure that the power supply will regulate properly at ±12V dc, the system load must be enough to draw a minimum of 3.0 amps at +5V dc. If the load is insufficient, the DC ON indicator will extinguish after a period of time.

3. The 115/230 VAC jumper (located near the AC terminal block) must be removed from the power supply when used for 230 VAC operation, and must be installed for 115 VAC operation.

4.3 AC POWER CONNECTION

An AC input power connector is located on the rear of the chassis box. Simply plug the provided power cord to the AC input connector and to an appropriate AC receptable.

Apply AC power to the MLSI-BA11 chassis by placing the AC ON/OFF rocker-style switch on the rear of the chassis in the ON position.

4.4 AC INPUT POWER CONVERSION

If necessary to configure the MLSI-BA11 Series chassis for operation with an AC input voltage different from that configured at the factory, perform the conversion procedures outlined in the following paragraphs.

4.4.1 Chassis Conversion

To convert the MLSI-BA11 Series chassis from 115 VAC to 230 VAC input power (or from 230 VAC to 115 VAC), perform the following:

1. Locate the AC input connector on the rear of the chassis assembly. Situated beside the AC input connector is the fuse compartment, containing a voltage selector printed circuit board and a protective fuse.

2. Remove the AC line cord from the power connector.

3. Slide the transparent window (covering the fuse compartment) to the left (open position).

4. Move the FUSE PULL lever to its left-most position. This causes the protective fuse to be released from the fuse holder.

5. Insert a pointed tool (such as a small screwdriver) into the hole in the small voltage selector PCB mounted in the fuse compartment and remove the PCB.

6. The voltage selector PCB contains the markings "120" and "240" to specify the AC input voltage ("120" = 115 VAC and "240" = 230 VAC). Position the voltage selector PCB as required for the AC input voltage to be used, and reinstall it in the fuse compartment. For 115 VAC operation, the "120" must be up and visible when the PCB is inserted in the compartment. For 230 VAC operation, the "240" must be up and visible when

installed. DO NOT turn the voltage selector PCB upside-down.

7. Once the voltage selector PCB is installed properly, move the FUSE PULL lever back to its original position (to the right).

8. Insert an appropriate protective slow-blow fuse in the fuse holder. The fuse should be rated for 5 amps when used with 115 VAC input voltage, and 2.5 amps when used with 230 VAC input voltage.

9. Close the transparent sliding window and reconnect an appropriate AC power cord, making sure the plug is compatible with either 115 VAC or 230 VAC.

4.4.2 Power Supply Conversion

In addition to the necessary modifications on the rear of the chassis, the MLSI-BA11 power supply must also be modified for the required AC input voltage. Simply remove the power supply top cover and remove the 115/230 VAC jumper from the power supply for 230 VAC operation, and install the jumper for 115 VAC operation. The 115/230 VAC jumper is located beside the power supply AC terminal block.

4.4.3 Power Sequencing Module Conversion

The Power Sequencing Module (MLSI-PSM23) must also be adjusted for the required AC input voltage. The necessary adjustments for 115 VAC and 230 VAC operation are described in paragraph 3.4.

The "B" size option plates are removed for utilization of DEC's DZV11 or DLV11-J, or MDB's MLSI-DLV11-J and DMA Systems Modules such as the MLSI-F-DR11-W, MLSI-F-DR11-B, and MLSI-F-DRV11-B.

The two "B" size option plates and the adapter bracket in locations "A/B" and "C1/C2" can be removed as one unit to accommodate MDB's 8-port or 16-port DZ11 multiplexor distribution panels (MLSI-F-DZ11-A and MLSI-F-DZ11-E, respectively).

The "D" size option plate is removed to accommodate disk or tape controllers (i.e., MLSI-F-RM11, MLSI-F-TM11, MLSI-F-TS11).

Consult the factory or an MDB Systems sales representative for a complete listing of modules which may be used with the Rear Cable Distribution Panel.

CHAPTER 6

RECOMMENDED PLACEMENT OF MODULES

6.1 INTRODUCTION

This chapter describes the recommended placement of modules in a standard MLSI-BA11-2000 system chassis. Prior to configuring an LSI-11-based computer system, you should become familiar with the operation and bus architecture of the LSI-11 family of computers by referring to the DEC Microcomputers and Memories Handbook or Microcomputer Processor Handbook.

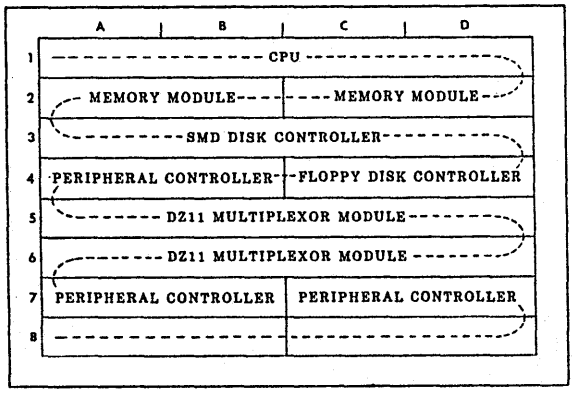
User discretion is advised in the configuration of an appropriate computer system. The examples discussed in this chapter are recommendations only.

Also included in this chapter is information pertaining to chassis installation and the initial power-up sequence.

6.2 RECOMMENDED MODULE PLACEMENT

Figure 6-1 shows a recommended placement of DEC-compatible modules in the MLSI-BPA84-E Backplane/Card Guide Assembly.

Figure 6-1
Recommended Module Placement



NOTE

The chassis is shown as viewed from the front (module-loading) side with the component sides of the modules facing upward.

The dashed lines indicate the Q-bus priority daisy chain. Priority for modules depends upon closeness to the processor; that is, the modules installed closest to the CPU have a higher interrupt priority than the modules that follow. However, if a module with four-level interrupt capability is used, it may be installed in any backplane slot and still retain its preassigned interrupt priority level.

The CPU should always be installed in the first slot of the backplane. In Figure 6-1, a quad-size CPU (i.e., LSI-11/23-PLUS) is installed in slot 1.

Memory modules might be installed as shown. The memory module in slot 2 C-D is the first module in position to receive the Q-bus signals after the CPU.

A Direct Memory Access (DMA) module, such as the SMD Disk Controller and the Floppy Disk Controller in the example provided, should follow the memory modules in the priority sequence.

After the DMA devices, programmed I/O devices, such as the MLSI-F-DZ11 8-port multiplexor, might be installed.

Following the multiplexor modules, your system configuration might require the installation of peripheral controller modules (i.e., MLSI-F-LP11).

The final backplane slot (8 A-B) may be utilized for a variety of applications. For system expansion, a Backplane Jumper/Cable Assembly (MLSI-BCV2A/B) or Bus Repeater Assembly (MLSI-DB11-R) may be installed. Note that the Bus Repeater should be used if the total number of modules in the system exceeds twenty dc bus

If no system expansion is required, the Terminator should be retained, leaving the backplane slot available for the installation of a functional module, such as the peripheral controller shown in the example.

NOTE

If necessary to leave an open slot in the priority daisy chain sequence, a Bus Grant Continuity Card (MLSI-BGC or equivalent) must be inserted in the "A" and "C" portion only of the vacant location. These devices transfer the DMA and Interrupt Bus Grant to the next module in the daisy chain.

6.3 CHASSIS INSTALLATION

The MLSI-BA11 Series of Chassis Assemblies can be easily slide or rack mounted in a standard 19-inch RETMA-type rack or cabinet. Front retaining flanges are predrilled on the chassis to accommodate machine screws for chassis retention.

To facilitate the optional slide mounting of the chassis (MLSI-SMO), all chassis are equipped with factory-drilled holes with tapped, self-clenching fasteners (PEM nuts) installed. Provided at the end of this manual is a drawing showing installation of the chassis slide mount option.

PRECAUTIONARY NOTES

1: For chassis that are not mounted on slides, it is recommended that the chassis be supported on rails to preclude damage to the front retaining flanges.

2. It is recommended that the chassis be removed from the cabinet before shipping to prevent possible damage. In addition, all modules should be removed from the chassis prior to shipping and reinstalled at the destination site.

3. Three cooling fans which provide 300 cfm air circulation are located on the side panel of the chassis. Proper air circulation is vital to reliable system cooling and operation. To preclude overheating and possible system damage, DO NOT restrict air flow through the chassis assembly.

6.4 CHASSIS POWER-UP SEQUENCE

After all modules are installed as recommended or required, and the necessary cables are securely connected. apply power to the chassis assembly by placing the AC ON/OFF rocker-style switch on the rear of the chassis in the ON position. When the system is configured for the ODT mode, the following power-up sequence should occur when power is initially applied to the chassis:

1. The DC ON indicator on the Switch/Indicator Control Panel should illuminate and remain in this state. When lighted, this indicator signifies that AC line voltage and DC power are acceptable for reliable system operation.

2. The RUN indicator should flash momentarily and then turn off. (If the RUN indicator remains illuminated in the ODT mode, a malfunction exists in the system.)

3. The LTC switch is normally disabled at the factory before shipment; therefore, the LTC indicator should be off when the system is powered-up for the first time. To enable line time clock interrupts, simply depress the LTC switch, which causes the indicator to light.

4. The HALT indicator should not be illuminated upon system power-up (the switch should be out). If the indicator is lighted (switch in), it signifies that the system is in the HALT mode and the normal power-up sequence is inhibited. To disable the HALT mode and enable the system to operate freely, simply press and release the HALT switch.

NOTE

In certain processor bootstrap modes, the chassis assembly may perform a power-up sequence different from the one described above. Refer to appropriate DEC documentation for additional information.

CHAPTER 7

MAINTENANCE AND REPAIR

7.1 MAINTENANCE

In the event of apparent malfunction, refer to the schematic diagrams and assembly drawings contained in the following pages. Check to make sure that all connectors are secure and that control panel switches are properly set.

Repair the chassis assembly using appropriate skills, techniques, and materials. If you wish MDB Systems to repair the chassis, contact the Customer Service Department and request a Return Material Authorization (RMA) number. After return authorization is obtained, pack the chassis assembly carefully, along with your best evaluation of trouble symptoms, and ship it, prepaid, to MDB Systems, Inc.

7.2 DRAWINGS

The following pages contain schematic diagrams and assembly drawings which may be useful in maintaining and repairing the chassis assembly.

CHAPTER 8

REAR CABLE DISTRIBUTION PANEL ASSEMBLY FOR MDB BASIC BOX SYSTEMS

8.1 INTROUCTION

This chapter describes the function and configurations of the MLSI-BAll-200X Rear Cable Distribution Panel Assembly supplied with the Basic Box Systems listed in Table 8-1.

Table 8-1

MDB MODEL NO.	CPU TYPE	CPU SIZE	BOOTSTRAP CHIP	MEMORY CAPACITY	MEMORY SIZE	NUMBER OF SERIAL PORTS	NUMBER OF UNUSED SLOTS
MLSI-S1-11/23+200X-F/R	KDF11-BA	QUAD	MXV11-A2	256KB	DUAL	2	1 Dual, 6 Quad or 13 Dual
MLSI-S2-11/23+200X-F/R	KDF11-BA	QUAD	MXV11-A2	512KB	DUAL	2	1 Dual, 6 Quad or 13 Dual
MLSI-S3-11/23+200X-F/R	KDF11-BA	QUAD	MXV11-A2	1MB	DUAL	2	1 Dual, 6 Quad or 13 Dual
MLSI-S4-11/23+200X-F/R	KDF11-BA	QUAD	MXV11-A2	2MB	DUAL	2	1 Dual, 6 Quad or 13 Dual

8.2 REAR CABLE DISTRIBUTION PANEL

The Rear Cable Distribution Panel Assembly facilitates the connection of cables between modules installed in the system backplane and user peripheral devices. Cable connections are made internally at the distribution panel bulkhead connectors, with external interface cables installed from the panel to the peripheral devices.

NOTE

To reduce radiated noise, shielded interface cables should be used. (Shielded cables may be purchased from MDB Systems, obtained from other sources, or supplied by the user.)

As supplied from the factory, the Rear Cable Distribution Panel contains a dual-port EIA RS-232-C Distribution Board with two male 25-pin bulkhead connectors (A0 and A1). Connectors A0 and A1 are provided for the connection of two internal mass terminated 10-conductor flat cables from the serial port connectors of a module installed in the backplane.

For example, since an LSI-11/23-PLUS processor is used, the cables may be installed from the CPU serial line unit (SLU) connectors (J1 and J2) to A0 and A1, respectively, of the RS-232-C Distribution Board.

Each port of the RS-232-C Distribution Board is configured at the factory for Transmit Data on pin 3, Receive Data on pin 2. In effect, this configuration provides a limited "null-modem" cable capability, thereby minimizing the number of different types of cables required for various applications. You may reconfigure the board, via jumper plugs, for the standard RS-232-C capability; that is, with Transmit Data on pin 2 and Receive Data on pin 3.

The required jumper settings for RS-232-C and "null-modem" configurations are shown below. The jumper connections shown under J1 are for the console serial line unit (line 0), and those listed under J2 are for the secondary serial line unit (line 1).

	RS-232-C		Null Modem	
Signal	J1	J2	J1	J2
Transmit Data	A2-A3	C2-C3	A2-B2	C2-D2
Receive Data	B2-B3	D2-D3	A3-B3	C3-D3

Factory-configuration

The board may also be configured to provide EIA RS-423-compatible signals for Transmit and Receive Data. It also contains provisions to operate with a DEC DLV11-KA and allows the use of an external clock.

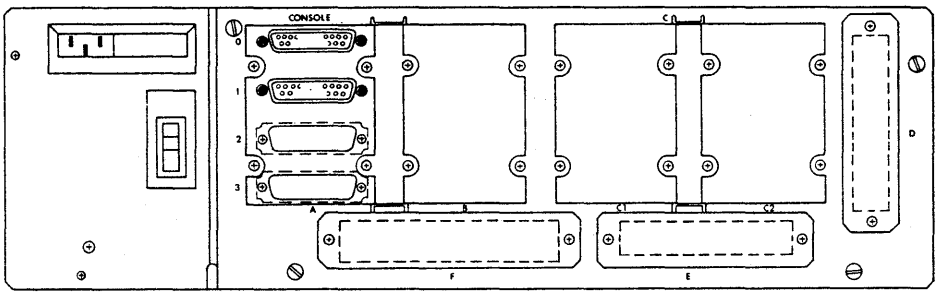
For additional jumper information, a schematic diagram (#44040540) and an assembly drawing (#45040540) of the RS-232-C Distribution Board are provided at the end of this manual.

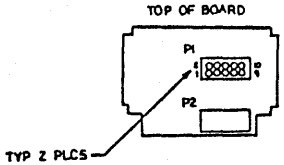
The design of the Rear Cable Distribution Panel also provides for future system expansion. The panel can accommodate a wide variety of MDB modules as well as DEC modules with cable kits. Figure 8-1 is a pictorial view of the Rear Cable Distribution Panel Assembly.

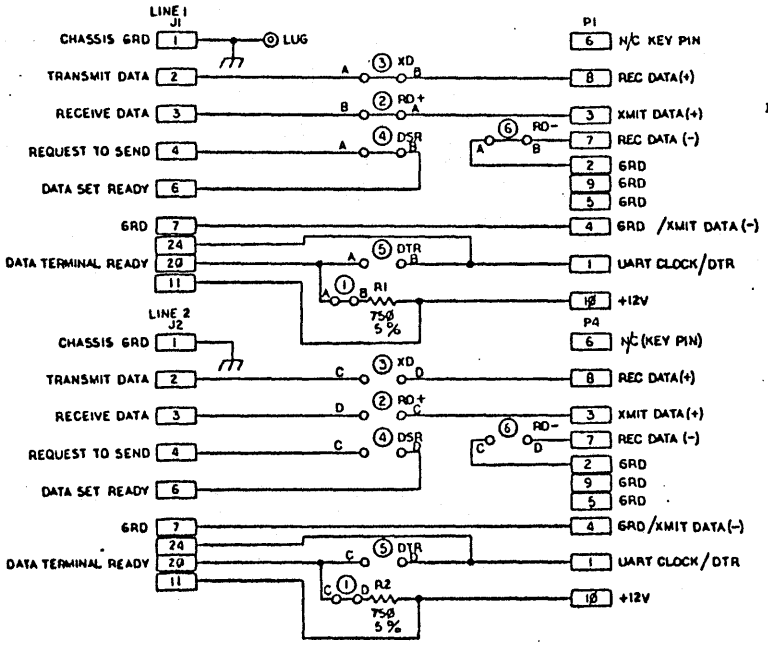
Refer to Chapter 5 for further details.

Figure 8-1

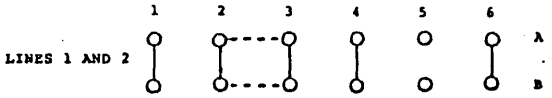
Rear Cable Distribution Panel Assembly





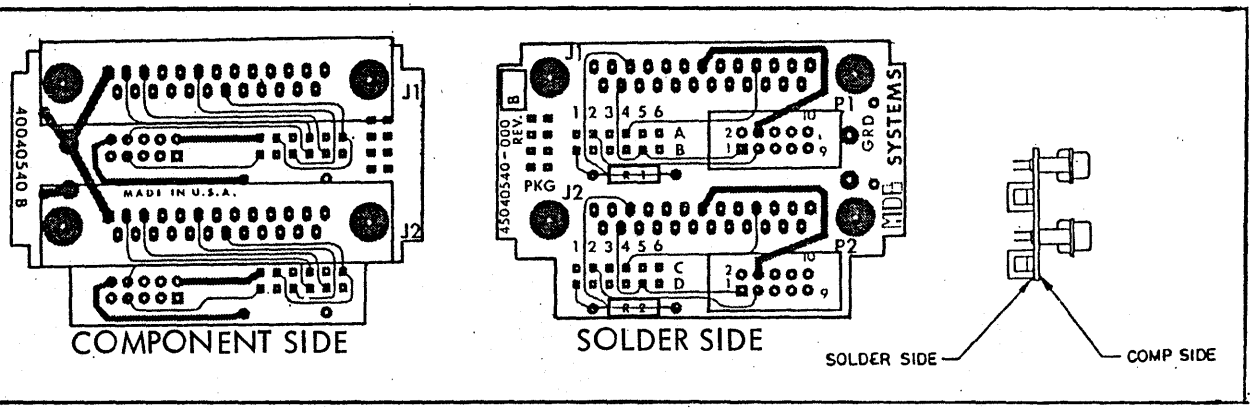


JUMPER PLACEMENT MAP AS SHIPPED



BOARD AS SHIPPED HAS TRANSMIT DATA ON PIN 3 AND RECEIVED DATA ON PIN 2.
TO TRANSPOSE DATA REORIENT JUMPERS BETWEEN 2 AND 3 AS SHOWN IN DASHED LINES.

JUMPER CONFIGURATION CHART		
LINES	1	2
TRANSMIT PIN 2	A 2 - 3	C 2 - 3
RECEIVE PIN 3	B 2 - 3	D 2 - 3
TRANSMIT PIN 3 *	2 A - B	2 C - D
RECEIVE PIN 2 *	3 A - B	3 C - D
REQUEST TO SEND TIED TO DATA SET READY	* 4 A - B	* 4 C - D
RS-232 - RECEIVE	6 A - B	6 C - D
RS-423 RECEIVE ENABLE	6 A - B	6 C - D
DTR / AUX INPUT	5 A - B	5 C - D
+12V OUT *	1 A - B	1 C - D
RS-422 REC DATA WIRE WRAP	6B-4A	6D-4C



*INDICATES AS SHIPPED

MDB SYSTEMS, INC.
DRAWN J MCNEILLY
SIZE D | PROD NO 51648 | DWG NO 45040540 | B1

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A	ECO NO 1928	5-82	
	B	ECO NO. 2105 RELEASE TO PRODUCTION	8-16-82	
	BI	ECO NO. 2697	2-16-84	

DWG. NO. 44040372 SH 1 REV. BI

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES °

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

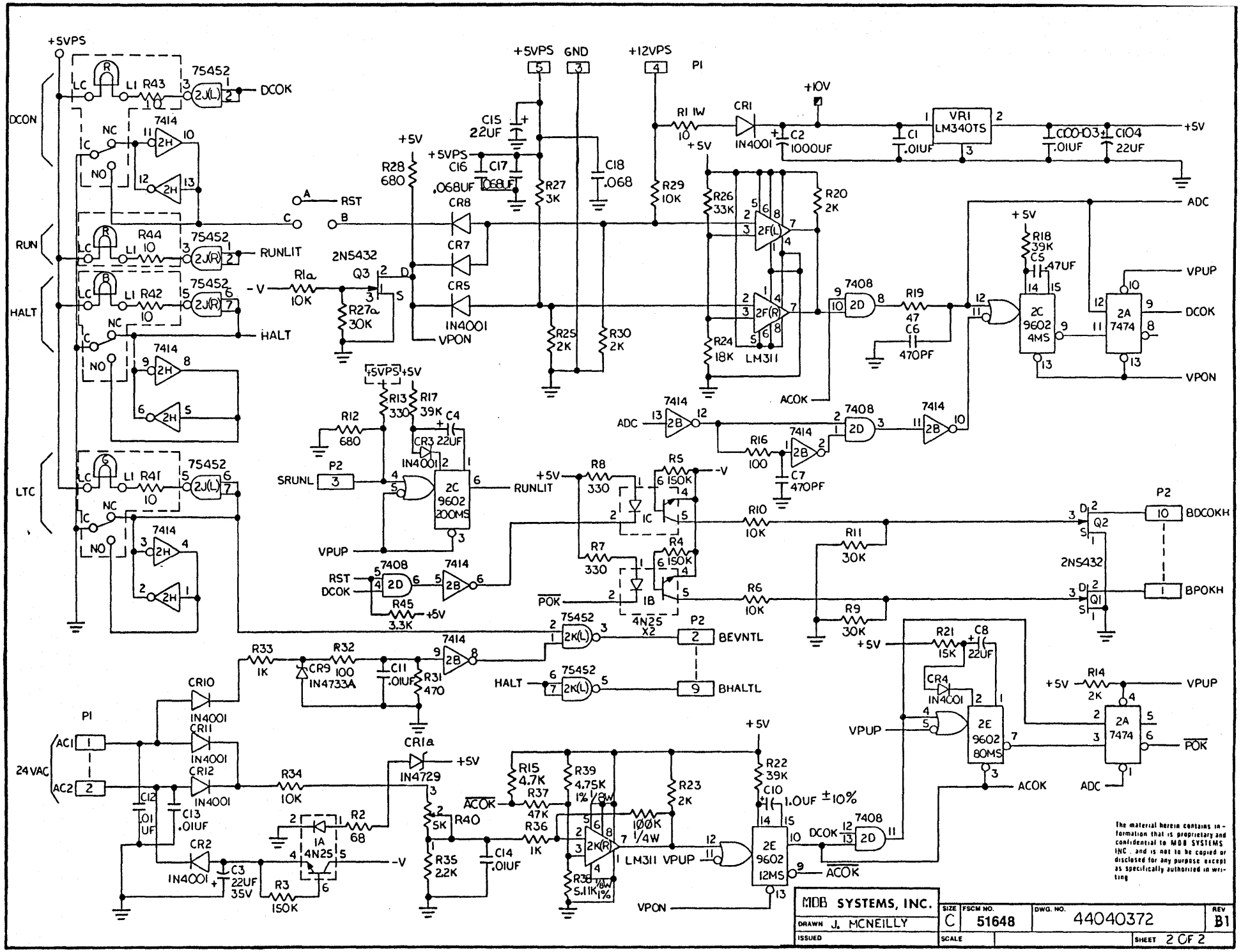
APPROVALS	DATE
DRAWN J.MC.	5-82
CHECKED	5-82
ISSUED	5-82

MDB SYSTEMS, INC.

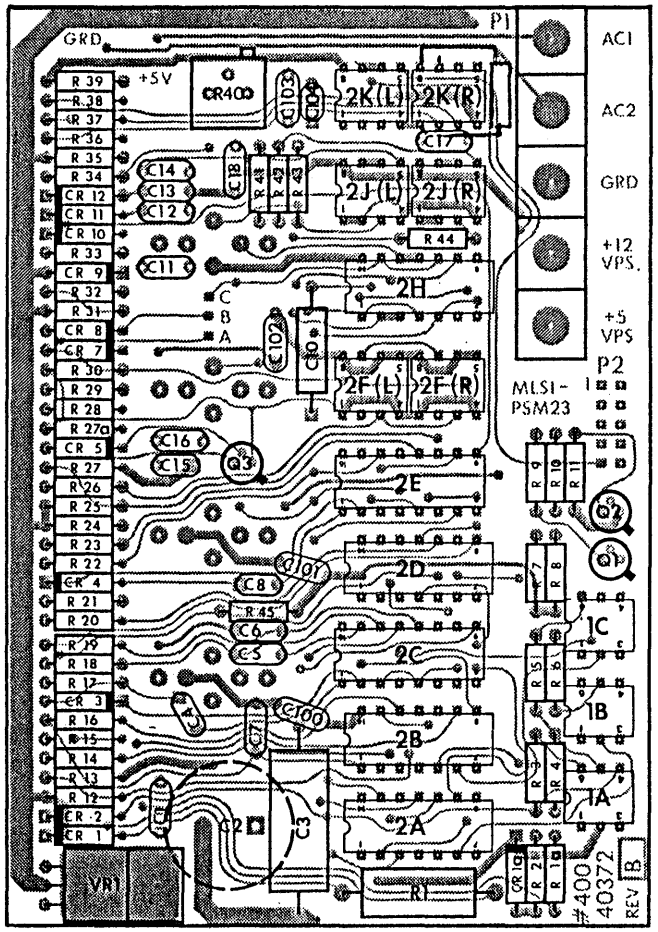
MLSI - PSM23

SIZE	FSCM NO.	DWG. NO.	REV.
C	51648	44040372	BI

SCALE NONE SHEET 1 OF 2


+5VPS
DCON
RUN
HALT
LTC
75452
7414
DCOK
RUNLIT
HALT
R43
R44
R42
R41
RST
2N5432
Q3
R1a
-V
R27a
30K
CR8
CR7
CR5
IN4001
VPON
+5VPS GND +12VPS
P1
C15 22UF
C16 .068UF
C17 .068UF
C18 .068
R28 680
R27 3K
R25 2K
R30 2K
R1 1W
CR1
IN4001
+10V
C2 1000UF
C1 .01UF
VR1 LM340T5
C103 .01UF
C104 22UF
R29 10K
R26 33K
R20 2K
R24 18K
LM311
ACOK
ADC
R18 39K
C5 47UF
R19 47
C6 470PF
2C 9602 4MS
2A 7474
VPUP
R13 330
R17 39K
R12 680
C4 22UF
CR3 IN4001
P2
SRUNL
2C 9602 200MS
R8 330
R5 150K
R10 10K
R7 330
R4 150K
R6 10K
R11 30K
R9 30K
Q2
Q1
2N5432
BDCOKH
BPOKH
POK
4N25 X2
R45 3.3K
75452
BEVNTL
BHALTL
R33 1K
R32 100
CR9 IN4733A
C11 .01UF
R31 470
CR10
CR11
CR12
CR1a
IN4729
AC1
AC2
24VAC
R34 10K
C12 .01 UF
C13 .01UF
C3 22UF 35V
R3 150K
R2 68
1A 4N25
R40 5K
R35 2.2K
C14 .01UF
R15 4.7K
R37 47K
R36 1K
R39 4.75K 1% 1/8W
R38 5.11K 1/8W 1%
100K 1/4W
R23 2K
R22 39K
C10 1.0UF ±10%
2E 9602 12MS
2E 9602 80MS
R21 15K
C8 22UF
CR4 IN4001
R14 2K
2A 7474
The material herein contains information that is proprietary and confidential to MDB SYSTEMS INC. and is not to be copied or disclosed for any purpose except as specifically authorized in writing
MDB SYSTEMS, INC.
DRAWN J. MCNEILLY
ISSUED
SIZE C
FSCM NO. 51648
DWG. NO. 44040372
REV B1
SCALE
SHEET 2 OF 2

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ECO NO 1928	5-82	
	B	ECO NO. 2105 RELEASE TO PRODUCTION	8-16-82	
	B2	ECO NO. 2697	2-16-84	



DWG NO 44040372 SH 1 REV B1

ASSEMBLY DWG.

QTY REQD	FSCM NO	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.X ±.1
.XX ±
.XXX ±

CONTRACT NO

APPROVALS	DATE
DRAWN J.MC.	5-82
CHECKED	5-82
ISSUED	5-82

MDB SYSTEMS, INC.

MLSI - PSM23

SIZE C | FSCM NO 51648 | DWG NO 44040372 | REV B2

SCALE NONE | SHEET 1 OF 2

MATERIAL

FINISH

NEXT ASSY | USED ON

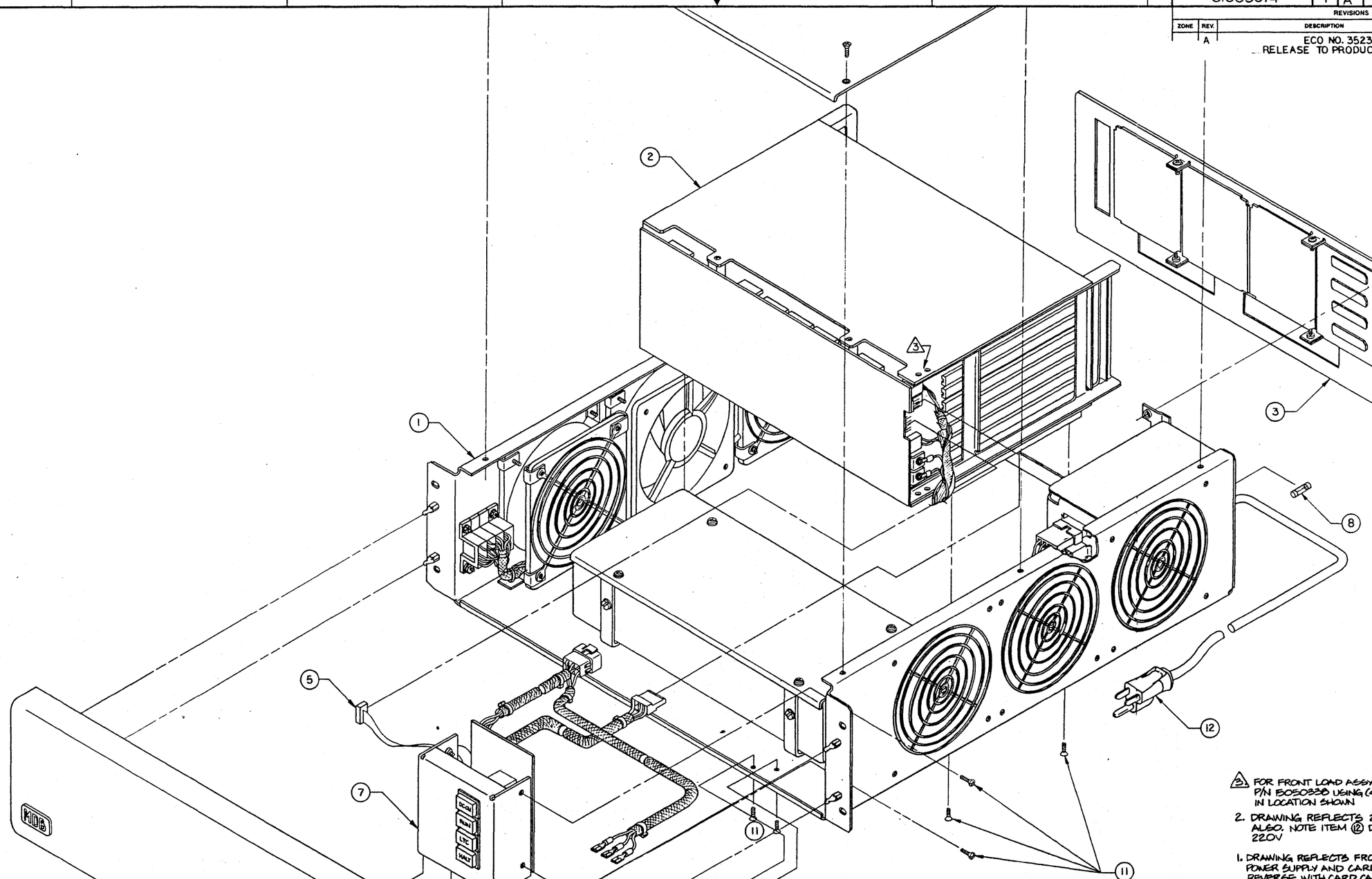
APPLICATION

DO NOT SCALE DRAWING

DWG. NO.	SH	REV.
01033674	1	A

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A	ECO NO. 3523 RELEASE TO PRODUCTION	2-6-86	



3. FOR FRONT LOAD ASSY INSTALL CABLE BACKSTOP P/N 8050338 USING (4) 4-40 X ¼" PH. FLT HD SCREWS IN LOCATION SHOWN
2. DRAWING REFLECTS 220V CONFIGURATION ALSO. NOTE ITEM (12) DOES NOT EXIST FOR 220V
1. DRAWING REFLECTS FRONT LOAD ASSY ALSO. POWER SUPPLY AND CARD CAGE LOCATIONS REVERSE WITH CARD CAGE ROTATING 180°, (CARD CAGE FACES FRONT OF CHASSIS)

NOTE: UNLESS OTHERWISE SPECIFIED

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. MCNEILLY	1-86
CHECKED	2-86
ISSUED	2-7-86

MDB SYSTEMS, INC.

MLSI-BAII-2000 R

SIZE	FSCM NO.	DWG. NO.	REV.
D	51648	01033674	A

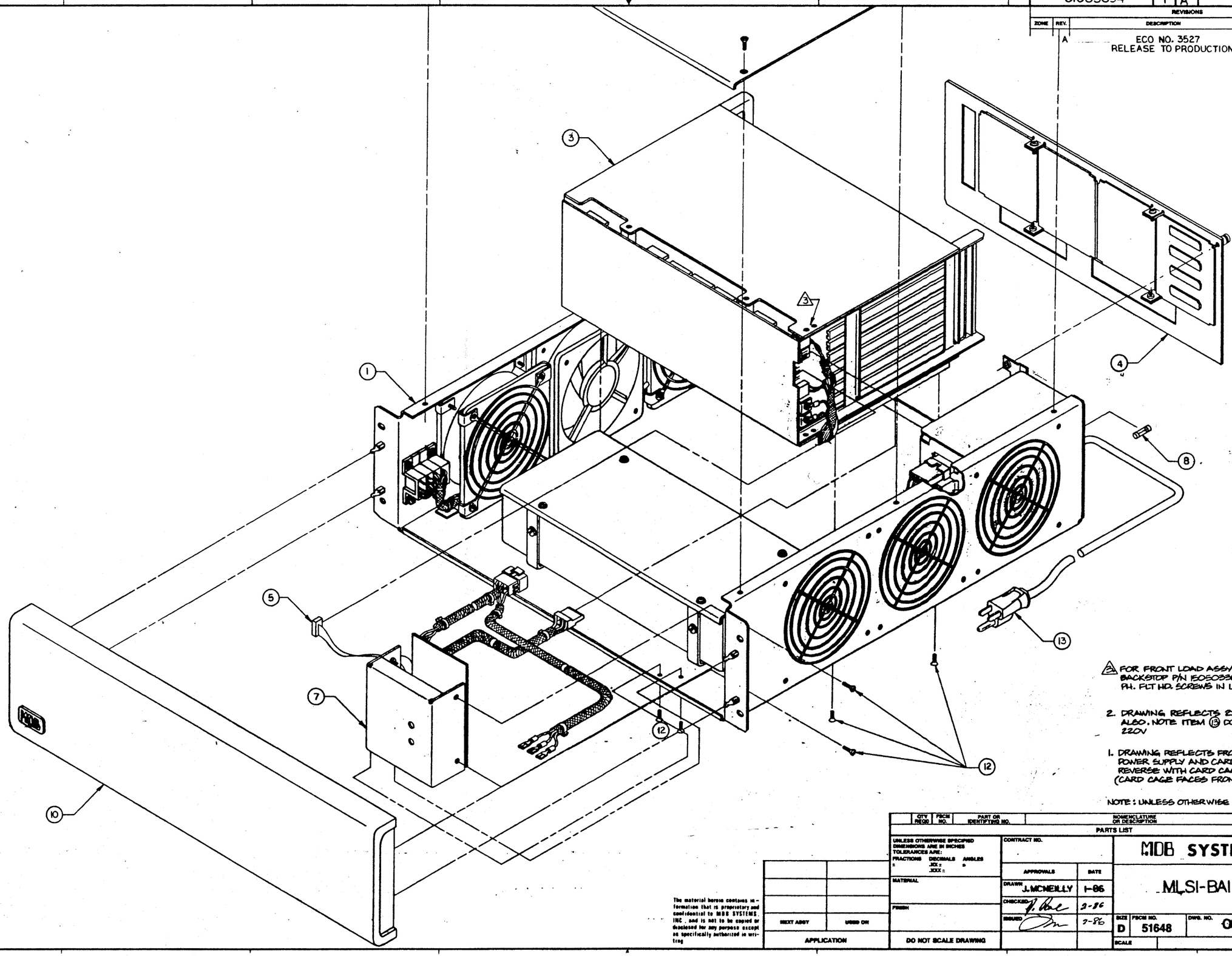
SCALE

SHEET 1 OF 1

DWG. NO. 01033694	SH 1	REV. A

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A	ECO NO. 3527 RELEASE TO PRODUCTION	2-7-86	



⚠2 FOR FRONT LOAD ASSY INSTALL CABLE BACKSTOP P/N 1505338 USING (4) 4-40 x ¼" PH. FLT HD. SCREWS IN LOCATION SHOWN

2. DRAWING REFLECTS 220V CONFIGURATION ALSO. NOTE ITEM (13) DOES NOT EXIST FOR 220V

1. DRAWING REFLECTS FRONT LOAD ASSY ALSO. POWER SUPPLY AND CARD CAGE LOCATIONS REVERSE WITH CARD CAGE ROTATING 180° (CARD CAGE FACES FRONT OF CHASSIS)

NOTE: UNLESS OTHERWISE SPECIFIED

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES °

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J.MCNEILLY	1-86
CHECKED	2-86
ISSUED	2-86

MDB SYSTEMS, INC.

MLSI-BAII-3000 R

SIZE D | FSCM NO. 51648 | DWG. NO. 01033694 | REV. A

SCALE | SHEET 1 OF 1

READER'S COMMENTS

Document Title _____

Document Part Number _____ Revision _____ Date _____

Name _____ Company _____

Title _____ Dept. _____

Address _____ State _____ Zip _____

This document is intended to provide accurate and meaningful information to help you properly operate and efficiently maintain equipment manufactured by MDB Systems, Inc. To this end, we welcome your comments regarding any errors, discrepancies or omissions you may have discovered, or any suggestions for improving the overall instruction manual. This postage-paid form is provided for your convenience. Your comments will be appreciated and should be useful input at the next revision of this document.

TECHNICAL OR CLERICAL ERRORS:
(Specify Page Numbers)

SUGGESTIONS FOR IMPROVEMENT:

MDB SYSTEMS INC.
1995 North Batavia Street
Box 5508
Orange, CA 92613-5508
(714) 998-6900
TWX 910-593-1393

No Postage necessary if Mailed in the United States

BUSINESS REPLY MAIL

First Class Mail Permit No. 1091 Orange, CA

Postage will be paid by

MDB SYSTEMS, INC.
1995 North Batavia Street
Box 5508
Orange, California 92613-9990

Attn: Documentation Dept.

MDB SYSTEMS, INC.
1995 North Batavia Street
Box 5508
Orange, California 92613-5508
(714) 998-6900
TWX: 910-593-1339