QRGB-ALPHA
Color Video Controller

MANUAL No. 166-A50-02/02

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matrox
electronic systems ltd.

US & CANADA:
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514-735-1182 TELEX: 05-825451

EUROPE:
HERENGRACHT 22, 4924 BH DRIMMELEN, HOLLAND
TEL: 01626-3850 TELEX: 74341 MATRX NL

FEATURES

- FIRMWARE OR SOFTWARE CHARACTER FONT
- Q-BUS PLUG-IN
- SOFTWARE PROGRAMMABLE FORMAT
- KEYBOARD INTERFACE
- MULTIPLE HEIGHT CHARACTERS
- COLOR ALPHANUMERICS
- TWO CHARACTER GENERATORS
- UNDERLINE AND BLINK
- FONT OF UP TO 512 CHARACTERS
- LIGHT PEN

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1.0 SPECIFICATIONS:

OPTIONS:

- Stand alone version
  - Standard 80 CHAR/LINE MAX.
  - Special 132 CHAR/LINE MAX.
- Slave version
  - Standard 80 CHAR/LINE MAX. ONLY

BUS:

- The QRGB-Alpha is completely compatible with the LSI-11 Q-BUS.

DISPLAY FORMAT:

- The display format is established by a programmed I/O initialization routine.
- The maximum number of character columns (standard version) is 80 using a standard video monitor with a horizontal display time of 49.5 us.
- The maximum number of displayed character rows is 48 for American systems (60Hz) and 52 for European systems (50Hz).
- The maximum number of characters in any given format is 4K with color or 8K without color.
- Characters may be selected as normal, double, triple or quadruple height and each of these heights can be halved in Interlaced Sync and Video Mode.
- Height of character cells can be up to 32 scan lines/field.
- There are 16 possible software selected dot clock frequencies derived from the crystal controlled clock.
- Character cells can be software programmed to have 6, 7, 8, 9, 10 or 11 dots horizontally.
- The display can be centered on the CRT by software programming the vertical and horizontal sync positions.

CHARACTER ATTRIBUTES:

- Color. The foreground and background of each character cell can be independently assigned one of 8 colors: red, green, blue, amber, blue-green, violet, black, or white.
- Blink. The foreground and background of each character cell can be independently assigned to blink at 2Hz (3.1 duty cycle).
- Underline. Characters can be assigned the underline attribute, which inverts the video in the 12th horizontal segment of the character cell.
- Extended height. The extended height attribute causes half of the assigned character to expand vertically to fill the entire character cell: the top half is expanded in odd numbered rows, and the bottom half is expanded in even numbered rows. This attribute can be used to construct large characters (two rows High) for text requiring special emphasis such as titles.
- Foreground Disable. This attribute allows characters to be written into display memory, but displays only the character cell background.
- Foreground Disable and Foreground Blink are mutually exclusive. Underline and Extended Height are mutually exclusive as well. In both cases, one of the two attributes is selected for use on any given board by straps.

1.0 SPECIFICATIONS (Cont'd):

CHARACTER GENERATION:

- Positions are provided for two character generators.
- One of the two character generators can be selected by programmed I/O or by bit 7 of the character code. The latter method effectively combines the two generators as one double-size unit.
- Character generators can be ROM (Matrox MCH-01), EPROM (2516), or RAM (4016).
- The standard board is shipped with one MCH-01, which provides 128 upper case, lower case, and graphics characters.
- The character generation circuit can be strapped to reduce the character sets in both positions from 128 to 64 characters, releasing bit 6 of the character code for attribute enable. The MCH-01's reduced character set does not include lower case and graphics characters.
- RAM character generators can be accessed via the bus, allowing software to establish a character set of up to 512 characters.
- Transparent or non-transparent access to character generator.

KEYBOARD INTERFACE:

- 8 bit ASCII codes are latched into the QRGB-Alpha by a positive going keyboard strobe.
- The C.P.U. inputs keyboard data from the QRGB-Alpha's keyboard register.

DISPLAY MEMORY:- 4K words or 8K bytes.
- Memory mapped or 256 byte movable window.
- Display Memory access time varies from access to access depending on when the access occurs with respect to the display refresh cycle: the worst case access time depends on the number of horizontal dots per character cell (See table below). The best case is 315ns, and average access time approaches 450ns as formats become less dense.
- Characters and their attributes can be accessed separately (byte XFER or together (word XFER)

DOTS PER CELL HORIZONTALLY	6	7	8	9	10	11
Worst Case Time From BDINL or BDOUTL to BREPLYL	870ns	1050ns	1130ns	1220ns	960ns	1050ns

- Access to all on-board RAM can be disabled by software.

I/O:
- I/O access time is 1.5us.
- Byte transfer only.

SCROLL:
- The display can be moved up and down with respect to the Display Memory.

LIGHT PEN:
- The position of a light-pen can be input from the QRGB-Alpha if a light-pen strobe and light-pen enable signal are provided.

VIDEO DISABLE:
- The video output can be software disabled.

1.0 SPECIFICATIONS (Cont'd):

SLAVE MODE: - The slave version of the QRGB-Alpha can be slaved to the QRGB-GRAPH (a Matrox color graphics card) to provide a combined alphanumeric and color graphics display.

T.V. STANDARD:
- European (50Hz) and American (60Hz) operation.
- Fully functional with any 15 MHz video monitor.
- Compatible with standard and direct drive monitors.

INPUTS (EXTERNAL TO BUS):

- Light-Pen Strobe: positive pulse no longer than one character clock cycle.
- Light-Pen enable: active high
- External Field sync
- External Clock
- External Character Clocksync
- 4 TTL graphics signals

Inputs from QRGB-Graph when the QRGB is used in slave mode.

OUTPUTS (EXTERNAL TO BUS):

- 4 Composite video signals:
  - red, green, blue, and grey scale.
  - 75 Ohm, 1 V P-P, -5% with load.
- 3 TTL video outputs: red, green, and blue.
- Composite blanking.
- Vertical and horizontal sync: these two signals can be strapped negative or positive going.

CONNECTORS:
- A-D 4 36 Pin edge connectors: Q-Bus signals.
- J1, 10 Pin right angle header AMP 87578-2; Composite video.
- J2, 10 Pin right angle header, AMP 87578-2: TTL video and power service.
- J3, 50 Pin Molex right angle header 10-55-3505: video bus for slave mode.
- J4, 26 Pin right angle header Molex 10-55-3265: keyboard and lightpen interface.

POWER REQUIREMENTS:

- 5V 5% @ 3 amps

DIMENSIONS: - Standard Quad Height card size: 12 inches wide by 10.457 inches high by 0.5 inches thick.

2.0 FUNCTIONAL DESCRIPTION:

The QRGB-Alpha is a LSI-11 BUS compatible alphanumeric video controller card, which has a software programmable text format and a complete set of colour character attributes. It also has, among other features; a cursor, a light pen register, and a scroll capability. Character and character attribute information for each character cell in the display is stored in a memory mapped display memory, which is automatically masked from the display during CPU accesses to prevent streaking on the display.

2.1 FORMAT:

The text format is established by a programmed I/O initialization of a series of on-board registers. Many different formats are possible within boundaries defined by a maximum number of character columns, a maximum number of character rows, and a maximum number of character cells. The maximum number of columns is 80. The maximum number of character rows, as shown in Table 2.1, depends on the interlace mode and whether the system is American (60Hz) or European (50Hz).

	INTERLACED SYNC & VIDEO	NON INTERLACED SYNC & VIDEO
AMERICAN	48 Rows	25 Rows
EUROPEAN	52 Rows	28 Rows

Table 2.1 - MAXIMUM CHARACTER ROWS

The maximum number of character cells is 8K with limited attributes and 4K with full attributes.

The QRGB-Alpha's text format can be programmed via a control register to have normal, double, triple, or quadruple height characters, and each of these heights can be halved in the Interlaced Sync and Video Mode, providing 6 different character heights. This feature allows proper character proportions to be maintained in both dense and sparce formats; however, because the larger characters occupy most of the available vertical character cell space, there are certain restrictions on their use: lower case and graphics characters can not be used with quadruple height characters, and the underline character attribute can not be used with triple or quadruple height characters.

Character cell dimensions, not to be confused with character dimensions, can also be software programmed. Cells can be up to 32 scan lines per field high, and they can be 6, 7, 8, 9, 10 or 11 dots wide. Differences between character dimensions and possible character cell dimensions provide a variety of possibilities for inter-row and inter-column spacing.

2.2 CHARACTER ATTRIBUTES:

One of the QRGB-Alpha's most important strengths is its large and versatile character attribute set, which comprises Foreground and Background Colour, Foreground and Background Blink, Underline, Extended Height, Foreground Disable, and (when paired with the QRGB-Graph) Graphics Disable. Any character cell's foreground and background can be independently assigned one of 8 colours: red, green, blue, amber, blue-green, violet, black, or white. The foreground and background can also be independently assigned to blink at 2 Hz. If a character is assigned the Underline attribute, the 12th horizontal segment of it's character cell becomes the foreground colour. The Extended Height attribute causes half of the assigned character to expand vertically to fill the entire cell: the top half is expanded in odd numbered rows, and the bottom half is expanded in even numbered rows. By arranging the expanded tops of letters over the expanded bottoms of the same letters, characters two rows high can be assembled for titles or other text requiring special emphasis. The Foreground Disable attribute allows characters to be written into the display memory while displaying only the background of the corresponding character cells.

The above character attributes are enabled by attribute enable bits stored with the character codes in the Display Memory. A series of straps and a control register bit are used to determine which bit will enable which attribute; however, because of the way they are implemented, there are the following restrictions on which attributes may be included in any given configuration: Foreground Disable precludes Foreground Blink, and Underline precludes Extended Height.

2.3 DISPLAY MEMORY:

The QRGB-Alpha's Display Memory can be operated in two modes: Normal Text Mode and Extended Text Mode. When the QRGB-Alpha is in Normal Text Mode, each character in the display has a corresponding 16 bit word in the Display Memory. This word is composed of a 6, 7, 8, or 9 bit ASCII character code with the remaining bits used for attribute enable. In this mode the display can have up to 4K characters. When the QRGB-Alpha is in Extended Text Mode, each character in the display has only one byte corresponding to it in the Display Memory. This byte is composed of a 6, 7, or 8 bit ASCII code with the remaining bits, if any, used to enable attributes. The Extended Text Mode provides twice as many characters (up to 8K) as the Normal Text Mode; however, it reduces the number of attributes per character and does not allow color. Access to memory in either of the above modes can be disabled by programmed I/O, allowing several boards to occupy the same address space.

The QRGB-Alpha can be strapped to occupy 8K or 256 addresses of the system address space. In the latter case the 256 addresses are mapped into different parts of the Display Memory by an I/O operation.

Access time for the QRGB-Alpha's display memory depends on when an access is initiated with respect to the display refresh cycle and is also affected by the clock configuration. The best case is 300ns from BSYNCL to BRPLYL; and the worst case, varies from 870ns with 6 dots per cell to 1220ns with 9 dots per cell. Average access time approaches 450ns as the formats become less dense.

2.3 DISPLAY MEMORY (Cont'd):

The standard QRGB-Alpha uses straight binary addressing to access display memory because it makes most efficient use of RAM; however, it can be provided with a special CRTC that allows row and column addressing as well. Figure 2.1 illustrates the two forms of addressing by showing the character cell addresses (decimal) for the first two rows of a format 80 characters wide. Note that row and column addressing leaves sections of memory unused.

Figure 2.1 - BINARY ADDRESSING VS ROW AND COLUMN ADDRESSING

Figure 2.2 shows how the RGB-Alpha occupies system address space.

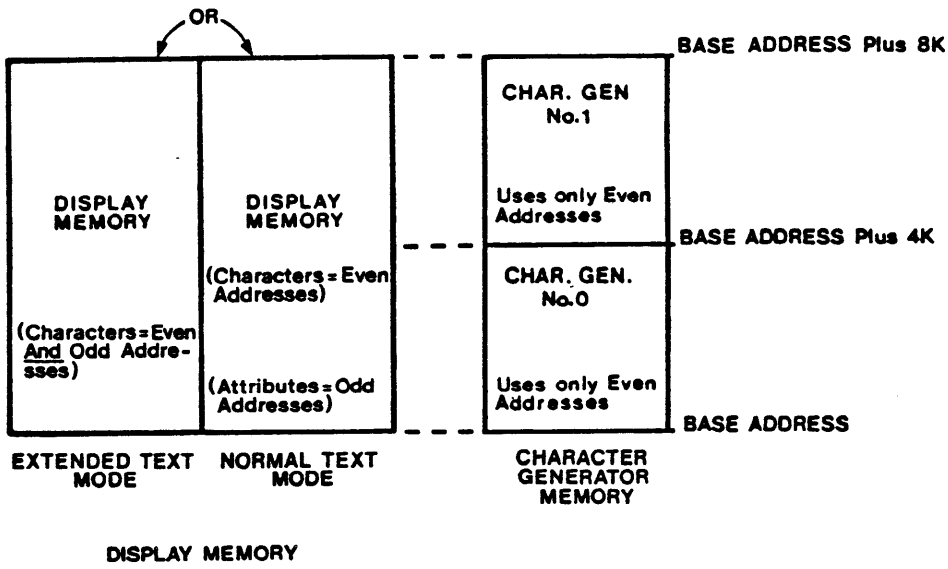


Figure 2.2 ADDRESS SPACE DISTRIBUTION

2.4 CHARACTER GENERATION:

The RGB-Alpha has positions for two character generator memories, and they can be ROM, EPROM or RAM. Selection between the two character generators can be made by a control register bit or by bit 7 or 8 of the character code, depending on a strap. The latter method effectively combines the two character generators as one double size unit capable of holding video information for up to 512 different characters. Off-board accesses to and from the character generators can be transparent or non-transparent. Transparent accesses can be made at anytime without disrupting the display but require fast memory (150ns). Non-transparent accesses can use slow memory (300ns) but must be done during vertical blanking to avoid disrupting the display. In both cases the character generators occupy the space shown in figure 2.2 and can be accessed directly or through the 256 byte window.

2.4 CHARACTER GENERATION (Cont'd):

Transparent accesses can be made at anytime without disrupting the display but require fast memory (150ns). Non-transparent accesses can use slow memory (300ns) but must be done during vertical blanking to avoid disrupting the display. In both cases the character generators occupy the space shown in figure 2.2 and can be accessed directly or through the 256 byte window.

Normally the QRGB-Alpha is supplied with one Matrox MCH-01 character generator, which has a set of 128 uppercase, lowercase, and graphics characters. Straps can be installed to disable the lowercase and graphics characters, halving the character set. The advantage of this reduced character set is that it only requires 6 bit ASCII codes, making bits 6 and 7 available for attribute enable. The reduced set is also required with quadruple height characters since there is not enough room in a character cell for quadruple height graphics characters or lower case descenders.

The MCH-01 character generator ROM uses 16 bytes per character; however, user programmed character generators can use 16 or 8 bytes per character. When 8 bytes per character are used, there can be up to 256 characters in each character generator, and an Attribute Memory bit can be used to switch between the two character generators, providing a font of 512 characters.

2.5 KEYBOARD INTERFACE:

Another useful QRGB-Alpha feature is the keyboard interface, which facilitates its use as a terminal. 8 Bit ASCII codes from a keyboard are made available to the CPU in a I/O mapped register. A flag is used to inform the CPU that data is ready.

2.6 GRAPHICS INTERFACE:

Provision has been made for the QRGB-Alpha to be used with a colour graphics controller, the QRGB-Graph, to produce a combination colour graphics and alphanumeric display. When this is done, graphics data is routed through the QRGB-Alpha, and a character attribute enable bit can be used to disable graphics in assigned character cells.

2.7 OUTPUTS:

The QRGB-Alpha has 4 composite video outputs: grey scale, red, blue, and green. Any of these output, can also be used as a source of composite sync. Three TTL colour video outputs are also provided, and a control register bit allows all video signals to be disabled.

The QRGB-Alpha also has separate outputs for horizontal and vertical sync pulses, which can be independently strapped as negative or positive going. Since the width and position of these pulses are programmable, the QRGB-Alpha can easily be used with direct drive as well as standard monitors.

3.0 FAMILIARIZATION PROCEDURE:

The QRGB-Alpha is thoroughly tested before shipping and this section is intended more to familiarize the user with the board than to test it.

1. Visually inspect the board for any shipping damage.
2. Plug the board into a LSI-11 system, connect video output No. One to a video monitor using standard sync. (See section 8 for connections), and turn on the power.
3. Using the following programming procedure (table 3.1), initialize the board. The result should be a 25 row by 80 column format having normal height character cells 7 dots wide, and a non-interlaced raster. Note that table 3.1 contains two data columns: one to be used with American systems and one to be used with European systems. The procedure is only valid when the boards straps are in the "as-shipped" configuration.

3.0 FAMILIARIZATION PROCEDURE (Cont'd):

STEP	DATA 60Hz	DATA 50Hz	I/O LOCATION	COMMENTS
1	371_8	371_8	764004_8	Control Register # 1 is programmed for 6 dots/cell, Dot Clock Divider of 2, and Video Enabled
2	010_8	010_8	764006_8	Control Register # 2 is programmed for Character Generator Access Disabled, Display Memory Access Enabled, Normal Character Height, No Extended Height, and Character Generator # 2 Selected.
3	000_8	000_8	764000_8	The Horizontal Total is Written to CRTC-RØ
4	146_8	152_8	764002_8	
5	001_8	001_8	764000_8	The Format Width (80) is Written to CRTC-R1
6	120_8	120_8	764002_8	
7	002_8	002_8	764000_8	The Horizontal Sync Pulse Position is written to CRTC-R2
8	126_8	131_8	764002_8	
9	003_8	003_8	764000_8	The Widths of the Horizontal and Vertical Sync Pulses are Written to CRTC-R3
10	070_8	110_8	764002_8	
11	004_8	004_8	764000_8	The Vertical Total is Written to CRTC-R4
12	032_8	036_8	764002_8	
13	005_8	005_8	764000_8	The Vertical Adjust Parameter is Written to CRTC-R5
14	000_8	002_8	764002_8	
15	006_8	006_8	764000_8	The Format Height (25) is Written to CRTC-R6
16	031_8	031_8	764002_8	
17	007_8	007_8	764000_8	The Vertical Sync Pulse Position is Written to CRTC-R7
18	031_8	033_8	764002_8	
19	010_8	010_8	764000_8	CRTC-R8 is Programmed for Non-Interlace Mode and no Character Skew
20	000_8	000_8	764002_8	
21	011_8	011_8	764000_8	The Number of Scan Lines per Character Row Minus One is Written to CRTC-R9
22	011_8	011_8	764002_8	
23	012_8	012_8	764000_8	CRTC-R1Ø and R11 are programmed to provide a Cursor that covers the entire Character Cell and Blinks
24	100_8	100_8	764002_8	
25	013_8	013_8	764000_8	
26	011_8	011_8	764002_8	
27	014_8	014_8	764000_8	CRTC-R12 and R13 are Initialized so that the top Left Text Character is in Display Memory Location Ø.
28	000_8	000_8	764002_8	
29	015_8	015_8	764000_8	
30	000_8	000_8	764002_8	
31	016_8	016_8	764000_8	CRTC-R14 and R15 are Initialized to put the Cursor at Location Ø
32	000_8	000_8	764002_8	
33	017_8	017_8	764000_8	
34	000_8	000_8	764002_8	
Follow steps 1 through 34 in order, outputting the appropriate data (50 or 60Hz) to the coresponding location indicated in the I/O location column.				

Table 3.1 - INTITAL CHECK-OUT PROGRAMMING PROCEDURE

4.0 PROGRAMMING:

The QRGB-Alpha text format is programmed by writing format parameters into a series of registers during a programmed I/O initialization routine. The Control Registers, the Keyboard Register and the Flag Register are accessed by direct I/O, and a further 18 CRTC registers are indirectly accessed via the Address Register and the Data Port. The directly accessed locations are described in subsection 4.2 where their as-shipped I/O addresses are given and boxes are provided for new I/O addresses resulting from changes in the I/O position straps. The indirectly accessed locations are described in the CRTC data sheets in section 12.

Parameters for a variety of formats are given in subsection 3.1; if the user requires a format not included, he can calculate the necessary parameters by following the examples in subsections 4.3 and 4.4.

4.1 PROGRAMMING TABLES:

Table 4.1 describes 6 different formats and table 4.2 gives the parameters required to program those formats. Note that there are separate columns for European and American parameters.

	1	2	3	4	5	6
FORMAT	80 x 48	80 x 25	40 x 24	35 x 12	28 x 8	16 x 7
DOTS/CELL	6	7	7	8	10	7
CHARACTER HEIGHT	Half Normal	Normal	Normal	Double	Triple	Quadruple
INTERLACE MODE	Video & Sync	NoInterlace	Sync Only	No Interlace	No Interlace	No Interlace
CRYSTAL FREQUENCY	11.6666MHz	11.6666MHz	11.6666MHz	11.6666MHz	11.6666MHz	11.6666MHz
MEMORY BYTES USED	3840	2000	960	420	224	112

Table 4.1 - TYPICAL FORMATS

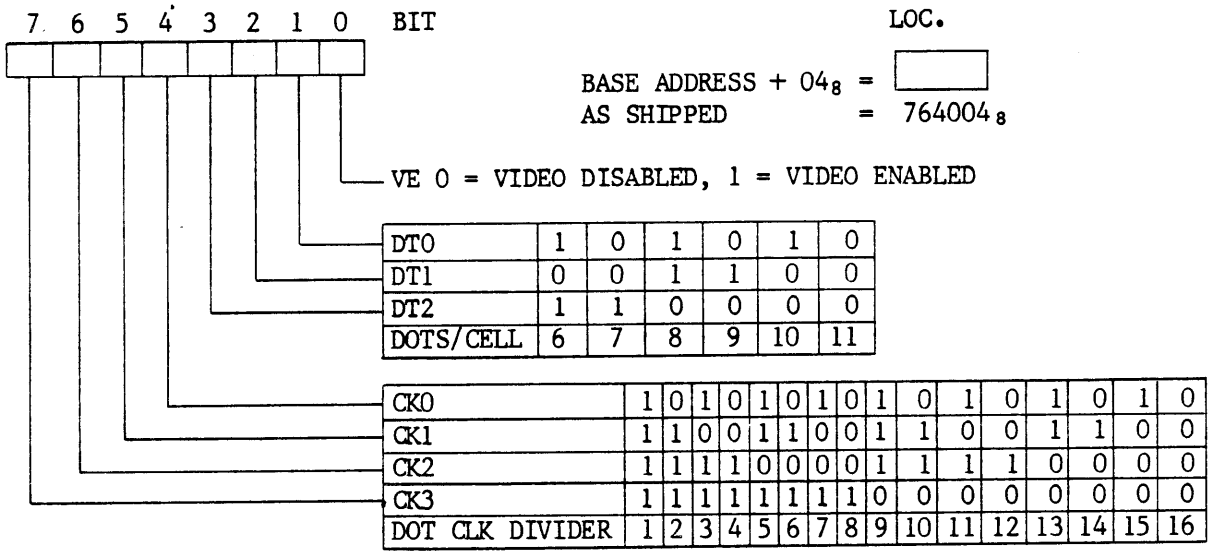
	1		2		3		4		5		6	
FORMAT	80 x 48		80 x 25		40 x 24		35 x 12		28 x 8		16 x 7	
AMERICAN/EUROPEAN	60Hz	50Hz	60Hz	50Hz	60Hz	50Hz	60Hz	50Hz	60Hz	50Hz	60Hz	50Hz
CONTROL REG. # 1	371_8	371_8	371_8	371_8	351_8	351_8	347_8	347_8	343_8	343_8	271_8	271_8
CONTROL REG. # 2	011_8	011_8	010_8	010_8	010_8	010_8	030_8	030_8	050_8	050_8	070_8	070_8
CRTC-R0	151_8	151_8	146_8	152_8	064_8	064_8	055_8	056_8	044_8	044_8	024_8	024_8
CRTC-R1	120_8	120_8	120_8	120_8	050_8	050_8	043_8	043_8	034_8	034_8	020_8	020_8
CRTC-R2	130_8	130_8	126_8	131_8	055_8	055_8	047_8	050_8	040_8	040_8	023_8	023_8
CRTC-R3	070_8	070_8	070_8	110_8	064_8	104_8	064_8	104_8	063_8	103_8	062_8	102_8
CRTC-R4	063_8	075_8	032_8	036_8	031_8	036_8	014_8	016_8	007_8	011_8	007_8	010_8
CRTC-R5	001_8	003_8	000_8	002_8	002_8	004_8	004_8	012_8	027_8	017_8	010_8	035_8
CRTC-R6	060_8	060_8	031_8	031_8	030_8	030_8	014_8	014_8	010_8	010_8	007_8	007_8
CRTC-R7	061_8	066_8	031_8	033_8	030_8	033_8	014_8	015_8	010_8	011_8	007_8	010_8
CRTC-R8	003_8	003_8	000_8	000_8	001_8	001_8	000_8	000_8	000_8	000_8	000_8	000_8
CRTC-R9	010_8	010_8	011_8	011_8	011_8	011_8	023_8	023_8	035_8	035_8	037_8	037_8
CRTC-R10	100_8	100_8	100_8	100_8	100_8	100_8	100_8	100_8	100_8	100_8	100_8	100_8
CRTC-R11	010_8	010_8	011_8	011_8	011_8	011_8	023_8	023_8	035_8	035_8	037_8	037_8
CRTC-R12	000_8	000_8	000_8	000_8	000_8	000_8	000_8	000_8	000_8	000_8	000_8	000_8
CRTC-R13	000_8	000_8	000_8	000_8	000_8	000_8	000_8	000_8	000_8	000_8	000_8	000_8

Table 4.2 - PROGRAMMING PARAMETER FOR FORMATS IN TABLE 4.1

4.2 I/O LOCATIONS: NOTE: ONLY BYTE TRANSFERS SHOULD BE USED FOR I/O ACCESS.

4.2.1. CONTROL REGISTER ONE:

WRITE ONLY



DT0	1	0	1	0	1	0
DT1	0	0	1	1	0	0
DT2	1	1	0	0	0	0
DOTS/CELL	6	7	8	9	10	11

CK0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
CK1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
CK2	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
CK3	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
DOT CLK DIVIDER	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

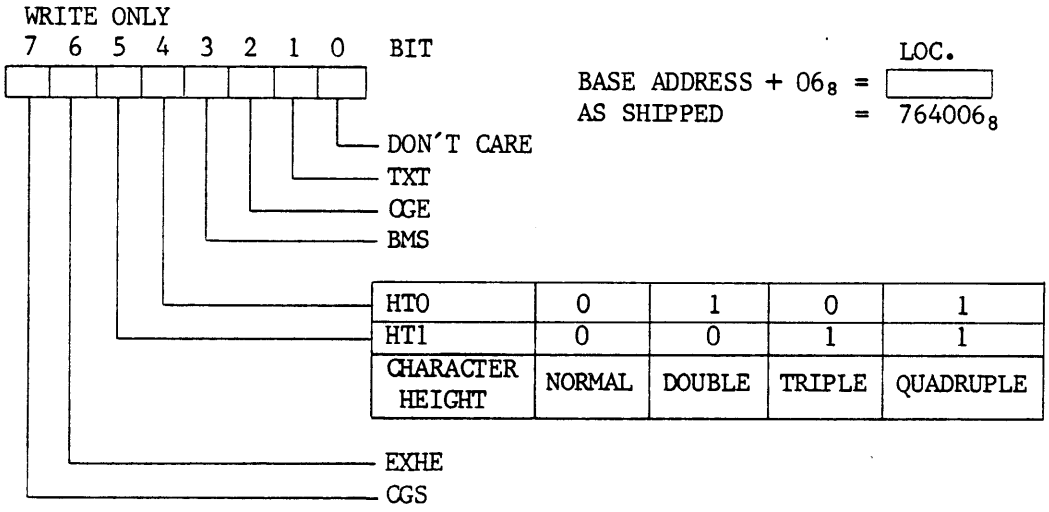
BIT 0 VE. When this bit is zero, all video outputs are disabled. When this bit is one, all video outputs are enabled.

BIT 1-3 DT0, DT1, DT2. These bits set the number of dots per cell horizontally. See table above.

BIT 4-7 CK0 -CK3. These bits program the dot clock frequency as a fraction of the crystal clock. See table above.

$$\text{DOT CLK FREQUENCY} = \frac{\text{XTAL FREQ}}{\text{DOT CLK DIVIDER}}$$

5.2.2 CONTROL REGISTER TWO:

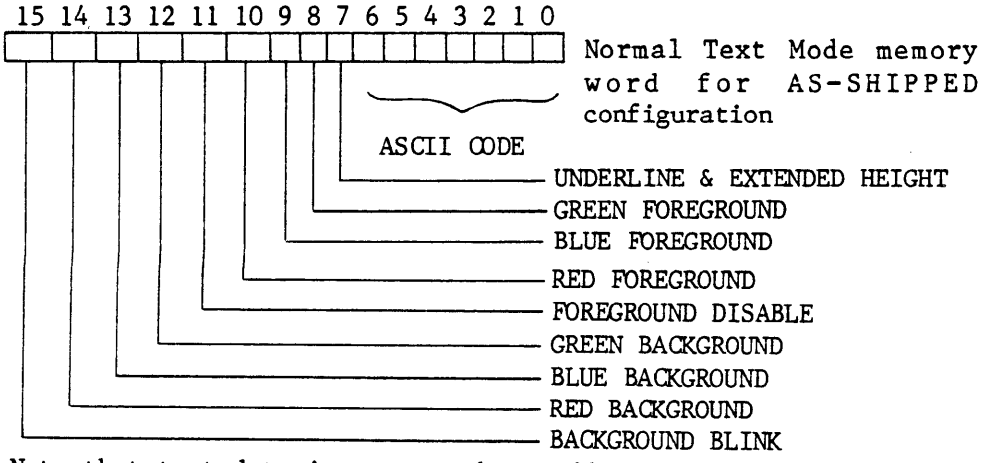


HT0	0	1	0	1
HT1	0	0	1	1
CHARACTER HEIGHT	NORMAL	DOUBLE	TRIPLE	QUADRUPLE

BIT 1

TxT. When this bit is zero the Display Memory is accessed in Normal Text Mode. When this bit is one the Display Memory is accessed in Extended Text Mode. Note that strap changes are also required (see section 5.7).

Normal Text Mode: Each character in the display has a corresponding 16 bit word in the Display Memory. Since only word locations are used, all characters in the display are addressed at even Display Memory locations. The first character cell (position set by CRTC R12 and R13) is addressed at the Display Memory's base address, the second character cell is addressed at the base address plus 2, and so on. The words in the Display Memory are composed of a 6, 7, 8, or 9 bit ASCII character code with the remaining bits used for attribute enable. Some of the attribute bits are permanently assigned specific attributes but others can be assigned different attributes via straps (see section 5.7). The following figure shows the as-shipped configuration of the memory word when the board is in Normal Text Mode.



Note that text data is at even byte addresses and attribute data is at odd byte addresses. Byte transfers can be used to access tex and attribute data separately.

4.2.2 CONTROL REGISTER 2:

Extended Text Mode: Each character in the display has a corresponding 8 bit byte in the Display Memory and it is composed of a 6, 7, or 8 bit ASCII character code with any remaining bits used for attribute enable. This mode increases the possible number of characters in the display from 4K to 8K; however, it disallows color attributes and reduces the remaining attributes to one or two.

BIT 2 — CGE. When this bit is one, the character generator memory space can be accessed from the bus. When this bit is zero the character generator memory space can not be accessed from the bus and the display is enabled. (Also see section 5.3.)

BIT 3 — BMS. When this bit is one, access to the Memory is enabled. When this bit is zero, access to the Memory is disabled.

BITS 4 AND 5 — HT0 and HT1. These two bits determine whether the format characters will be normal, double, triple or quadruple height (see table above, also Section 4.5).

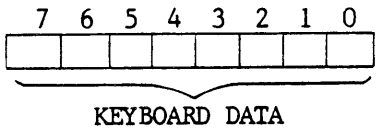
BIT 6 — EXHE. When this bit is one, the extended height character attribute is enabled. When this bit is zero the extended height character attribute is disabled (also see section 2.2).

BIT 7 — CGS. When this BIT is one, character generator no. 1 is enable and character generator no. 0 is disabled. When this bit is zero, character generator no. 1 is disabled and character generator no. 0 is enabled. The function of this bit also depends on a strap (see section 5.6). When shipped character generator No. 0 is installed.

All Control Register bits go to zero when the board is reset.

4.2.3 KEYBOARD REGISTER:

READ ONLY



LOC.

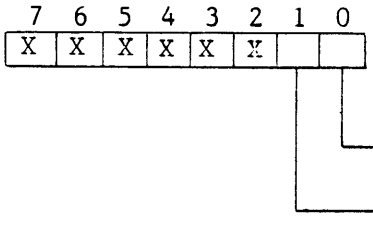
BASE ADDRESS + 04_8 = [ ]

AS SHIPPED = 764004_8

When the QRGB-Alpha's keyboard interface is used, this register contains the last 8 bit ASCII character code entered by the keyboard. A flag (next subsection) can be used to inform to CPU that the register is ready to be read.

4.2.4 FLAG REGISTER:

READ ONLY



LOC.

BASE ADDRESS + 06_8 = [ ]

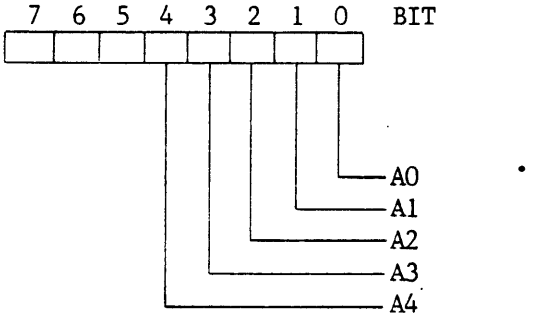
AS SHIPPED = 764006_8

BIT 0 KB FLAG. When this bit is one, the Keyboard Register is ready to be read. When this bit is zero, the keyboard Register is not ready to be read.

BIT 1 VS FLAG. This bit is one during the vertical sync pulse and zero when the vertical sync pulse is not active.

4.2.5 CRTC ADDRESS REGISTER:

WRITE ONLY



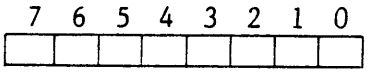
LOC.

BASE ADDRESS + 00_8 = [ ]

AS SHIPPED = 764000_8

BIT 0 - 4 CRTC Register Address. When one of the CRTC programming registers (R0 - R18) is accessed, its address is placed in this register then it is accessed through the CRTC data port (see 4.2.6). Descriptions and addresses of the CRTC registers accessed in this manner are found in the CRTC data sheets in section 12.

4.2.6 CRTC DATA PORT:



LOC.

BASE ADDRESS + 02_8 = [ ]$_8$

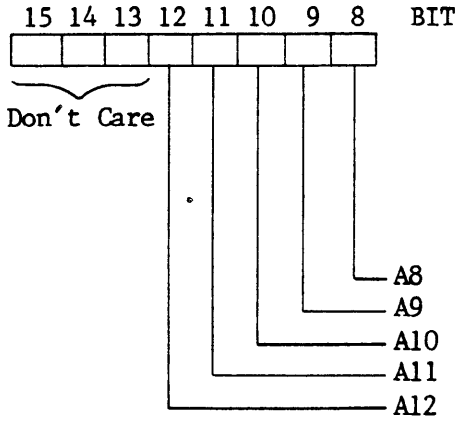
AS SHIPPED = 764002_8

DATA FOR CRTC REGISTERS

After the address of a CRTC register (R0 - R18) has been placed in the Address Register, the register is accessed via this location.

4.2.7 WINDOW MODE REGISTER:

WRITE ONLY



LOC.

BASE ADDRESS + 01_8 = ☐

AS SHIPPED = 764001_8

NOTE that this register has redundant addressing and can also be accessed at base address plus 3, 5, or 7.

256 MODE BASE ADDRESS BITS

When the QRGB-Alpha is strapped to use a 256 address window into the system address space, this register contains the 5 most significant bits of the base address of the 256 address section of the Display Memory that is accessed through that window.

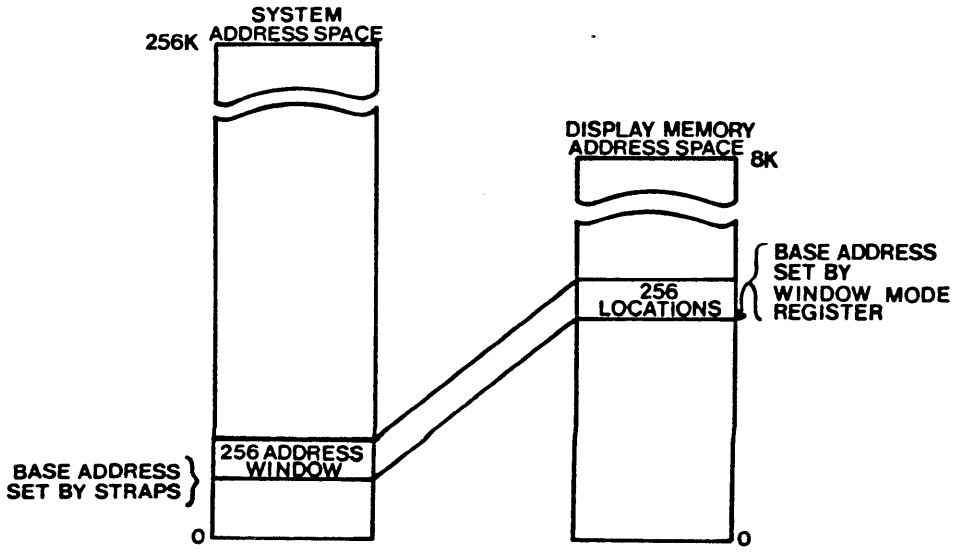


Figure 4.1 - MEMORY MAPPING

4.3 FORMAT PARAMETER CALCULATION EXAMPLE ONE:

The following example shows a step by step procedure which can be used to calculate format parameters. Before starting the calculations the user must define the format he requires by choosing the number of character rows, the number of character columns, the number of dots per character cell, the character height, and any inter row spacing. He should also know the horizontal active video period of the video monitor to be used.

Characteristics of Monitor used in this Example:

- American standard (60 Hz): Vertical scan period = 16.66 ms
  Horizontal scan period = 63.5 us
- Displayed portion of horizontal scan = 51 us Max.

QRGB-Alpha Crystal Frequency:

- 11.6666 MHz (Standard)

Required Format:

- 80 Characters per horizontal row.
- 24 horizontal rows of characters.
- 7 horizontal dots per character cell.
- 10 scan lines per horizontal row.
- The tentative horizontal display time is chosen to be the same as the monitors maximum horizontal display time (51 us) in order to maximize the display width. If the user required larger margins he would reduce this value accordingly.

1. The first step is to calculate the Tentative Dot Clock Frequency. This value is used in subsequent calculations, and the actual dot clock frequency is determined once the Dot Clock Divider has been selected.

$$\text{Tentative Dot Clock Frequency} = \frac{\text{Characters/line x Dots/Character cell}}{\text{Tentative Horizontal Display Time}}$$

$$= \frac{80 \times 7}{51 \text{ us}}$$

$$= 10.98 \text{ MHz}$$

2. Using the above calculated Tentative Dot Clock Frequency calculate the Ideal Dot Clock Divider and using it as a reference, choose the actual Dot Clock Divider.

$$\text{Ideal Dot Clock Divider} = \frac{\text{Crystal Frequency}}{\text{Tentative Dot Clock Frequency}}$$

$$= \frac{11.6666 \text{ MHz}}{10.98 \text{ MHz}}$$

$$= 1.06$$

$$\text{Actual Dot Clock Divider} = 1$$

4.3 FORMAT PARAMETER CALCULATION EXAMPLE ONE (Cont'd):

When the Tentative Horizontal Display Time is chosen equal to the monitor's maximum horizontal display time, the Actual Dot Clock Divider must be chosen as an integer smaller than the Ideal Dot Clock Divider otherwise the display will overshoot the CRT. If, however, the user allows for margins when choosing the Tentative Horizontal Display Time, the nearest integer, higher or lower, can be chosen.

3. Calculate the actual Dot Clock Frequency.

$$\text{Dot Clock Frequency} = \frac{\text{Crystal Frequency}}{\text{Dot Clock Divider}}$$

$$= \frac{11.6666 \text{ MHz}}{1}$$

$$= 11.6666 \text{ MHz}$$

4. Calculate the actual Horizontal Display Time.

$$\text{Horizontal Display Time} = \frac{\text{Characters/Line x Dots/Character Cell}}{\text{Dot Clock Frequency}}$$

$$= \frac{80 \times 7}{11.6666 \text{ MHz}}$$

$$= 48.0 \text{ us}$$

This is an acceptable display width, and the resulting 1.5 us margins will allow for differences in monitors. If, after doing these calculations, the user finds that the margins are too large, he has the option of changing the crystal (see example # 2). Another solution, actually a pseudo-solution, would be to increase the dots per cell, distributing the excess margin space between characters.

5. Calculate the Character Clock Frequency.

$$\text{Character Clock Frequency} = \frac{\text{Dot Clock Frequency}}{\text{Dots/Character Cell}}$$

$$= \frac{11.6666 \text{ MHz}}{7}$$

$$= 1.6666 \text{ MHz}$$

6. Calculate the Horizontal Total so that the total horizontal scan period is equal to 63.5 us ±5% (american monitor horizontal scan period). The Horizontal Total is the total number of character clock cycles per scan line. This value minus one will be placed in CRTC Register 0.

.3 FORMAT PARAMETER CALCULATION EXAMPLE ONE (Cont'd):

Tentative Horizontal Total = Character Clock Frequency x Monitor Horizontal Scan Period

= (1.6666 MHz x 63.5 us)

= 105.8

Horizontal Total = Nearest Even Integer = 106 (152_8)

An even number must be selected when the interlaced mode is to be used.

7. Calculate the Horizontal Scan Time.

$$\text{Horizontal Scan Time} = \frac{\text{Horizontal Total}}{\text{Character Clock Frequency}}$$

$$= \frac{106}{1.6666 \text{ MHz}}$$

= 63.6 us

8. Calculate the Character Row Period.

Character Row Period = Scan lines/Character Row x Horizontal Scan Time

= 10 x 63.6 us

= 636 us

9. Calculate the Vertical Total, which is the total number of complete character rows per vertical scan. This value minus one will be placed in CRTC register 4.

$$\text{Tentative Vertical Total} = \frac{\text{Vertical Scan Period}}{\text{Character Row Period}}$$

$$= \frac{16.66 \text{ ms}}{636 \text{ us}}$$

= 26.19

Vertical Total = Nearest Lower Integer = 26 (32_8)

10. Calculate the Vertical Total Adjust, which will be placed in CRTC Register 5 to adjust the vertical scan frequency to 60Hz.

$$\text{Tentative V. Total Adjust} = \frac{\text{Vertical Scan Period} - \text{V. Total} \times \text{Character Row Period}}{\text{Horizontal Scan Period}}$$

$$= \frac{16.66 \text{ ms} - 26 \times 636 \text{ us}}{63.6 \text{ us}}$$

= 1.95

Vertical Total Adjust = Closest integer = 2

4.3 FORMAT PARAMETER CALCULATION EXAMPLE ONE (Cont'd):

11. Determine the Horizontal Sync Position, which is the non-displayed character position where the horizontal sync pulse is generated. It is chosen so that the display is centered on the CRT and, as a result, is dependent on the format width. Some trial and error may be required, but if the Horizontal Sync Position is set 1/3 of the way through the undisplayed character positions, the result should be an acceptable starting point.

$$\text{Horizontal Sync Position} = \text{H. Displayed} + \frac{\text{H. Total} - \text{H. Displayed}}{3}$$

$$= 80 + \frac{(105 - 80)}{3}$$

$$= 88\ (130_8)$$

This value will be placed in CRTC Register 2.

12. Determine the Vertical Sync Position, which is the non-displayed character row position where the vertical sync pulse is generated. This position determines the displayed text's vertical position, and is set a little less than half way through the non-displayed character row positions. This value will be placed in CRTC Register 7.

$$\text{Vertical Sync Position} = \text{Vertical Displayed} + \frac{\text{Vertical Non-Displayed}}{2}$$

$$= 24 + \frac{1}{2}$$

$$= 24.5$$

$$\text{Next Smaller Integer} = 24\ (30_8)$$

13. Determine the Horizontal and Vertical Sync Widths. The width of sync pulses may depend on the type of monitor used; however, with most standard monitors the horizontal sync pulse should be 5 us $\pm$0.5 us long, and the vertical sync pulse should be about 190 us long. Sync pulses for direct drive monitors will, of course, be much longer. Horizontal and vertical Sync Width are calculated in character clock periods and Horizontal Scan Times respectively, and these values are placed in CRTC Register 3.

$$\text{Tentative H. Sync Width} = \frac{\text{Horizontal Sync Pulse Length}}{\text{Character Clock Period}}$$

$$= \frac{5\text{ us}}{.6\text{ us}}$$

$$= 8.33$$

Horizontal Sync Width = Nearest Integer = 8

4.3 FORMAT PARAMETER CALCULATION EXAMPLE ONE (Cont'd):

$$\text{Tentative Vertical Sync Width} = \frac{\text{Vertical Sync Pulse Length}}{\text{Horizontal Scan Time}}$$

$$= \frac{190 \text{ us}}{63.6 \text{ us}}$$

$$= 2.99$$

Vertical Sync Width = Nearest Integer = 3

4.4 FORMAT PARAMETER CALCULATION - EXAMPLE TWO (CHANGING THE CRYSTAL):

With certain formats the available dot clock dividers (1 through 16) may not allow the display to be as wide as the user might wish. In such a case he has the option of changing the crystal frequency.

For example, if a 20 x 64 display of character cells 6 dots wide is programmed using the standard 11.6666 MHz clock, the maximum horizontal display time will be calculated to be 33 us, using the procedure in example one. The display would only occupy 3/5 of the available horizontal display space; however, if the user chose a divider of 2 he could increase the horizontal display time to 48 us by changing the crystal as follows:

$$\text{Crystal Frequency} = \frac{\text{Characters/Row x Dots/Character x Dot Clock Divider}}{\text{Required Horizontal Display Time}}$$

$$= \frac{64 \times 6 \times 2}{48 \text{ us}}$$

$$= 16 \text{ MHz}$$

As shipped, the QRGB-Alpha can use any crystal frequency between 10Mhz and 16MHz. If a lower frequency is to be used the time constant (R7 and C31) on the XACK/ one shot will have to be increased. Note, however, that it is neither necessary nor advisable to use crystals below 8MHz. Dot clock frequencies on the standard version should not be programmed at more than 12MHz.

4.5 CHARACTER HEIGHT PROGRAMMING CONSIDERATIONS:

Figure 4.1 illustrates the different character heights programmable via the Control Register. The heights are shown in scan lines per field, and the scan lines per character height relationship is that observed when the CRTC's non-interlaced mode is used. When the CRTC's interlaced sync and video mode is used, the number of scan lines per character height is the same as shown in figure 4.1 ; however, they are divided between alternate fields offset from each other by half a horizontal scan period, and as a result, the character heights are actually halved. Although this last mode, by halving normal and triple height characters, provides for half height and one and one half height characters respectively, it must be remembered that it also halves the refresh rate, and flicker can occur if monitors with long persistence phosphore are not used.

4.5 CHARACTER HEIGHT PROGRAMMING CONSIDERATIONS (Cont'd):

The maximum number of scan lines per character row per field is 32. This fact, when considered while comparing the character font in section 7 with figure 4.1, shows that there are not enough available scan lines to display lower case descenders or full graphics characters when quadruple height characters are used. As a result, the RGB-Alpha must be strapped for the reduced character set (64 characters) when that height is used. For similar reasons the underline character attribute can not be used with triple or quadruple height.

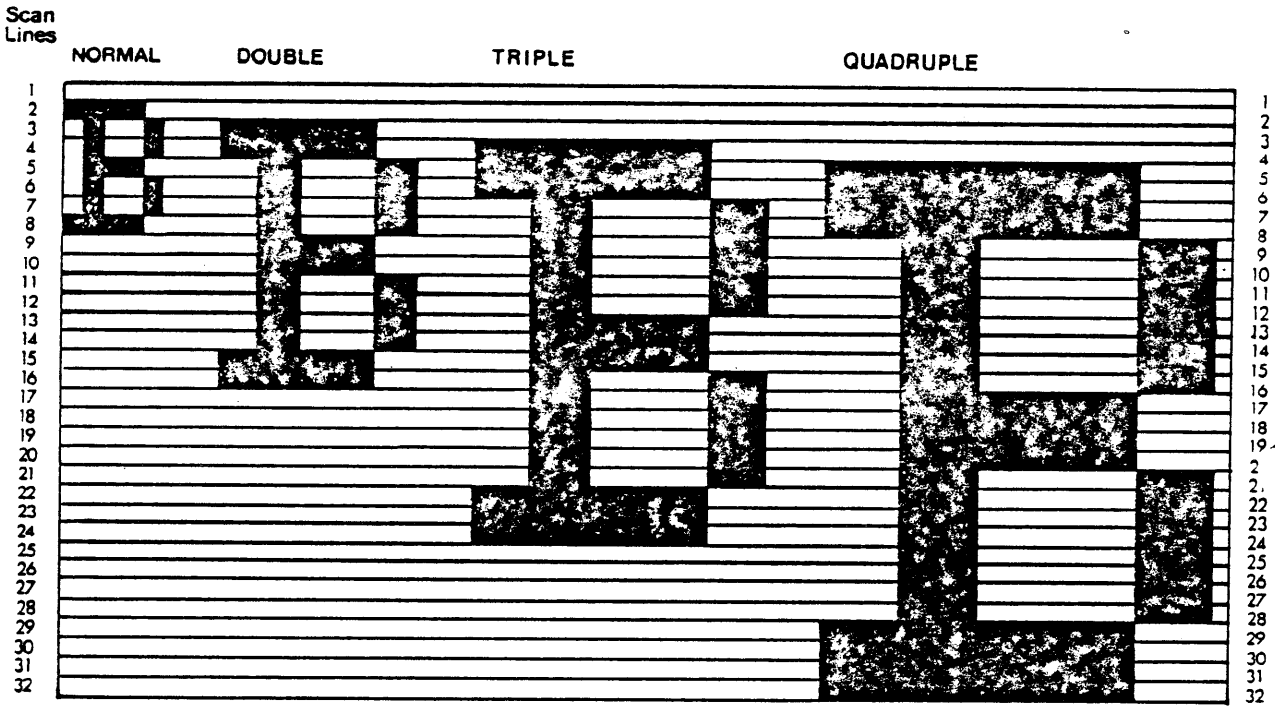


Figure 4.1 - CHARACTER HEIGHT

5.0 STRAPS:

The following section describes the QRGB-Alpha's strap options. Straps are implemented by connecting numbered wire wrap pins that are labeled on the P.C.B. silk screen. Straps are referred to in the following manner:

14-15 IN, indicates that wire wrap pin 14 is connected to wire wrap pin 15
14-15 OUT, indicates that wire wrap pin 14 is not connected to wire wrap pin 15
14←→15, indicates that wire wrap pin 14 is connected to wire wrap pin 15.

5.1 DISPLAY MEMORY BASE ADDRESS STRAPS:

As previously mentioned the display memory can be accessed in two ways: in a 8K section of system address space or through a 256 address window that is mapped into the Display Memory by the Window Mode Register (see section 4.2.7). Table 5.1 and 5.2 shows the strap configurations for both these access modes.

BASE ADDRESS BIT	AD15	AD14	AD13
CORRESPONDING STRAP	47-50	49-52	48-51
STRAP STATE FOR BIT=1	OUT	OUT	OUT
STRAP STATE FOR BIT=0	IN	IN	IN
ALSO STRAP 6-12 IN, 12-13 OUT, 27-28 IN, 28-29 OUT			

Table 5.1 - STRAPS FOR 8K ADDRESS SPACE

BASE ADDRESS	AD17	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
CORRESPONDING STRAP	36-34	35-33	47-50	49-52	48-51	10-4	11-5	7-1	8-2	9-3
STRAP STATE FOR BIT 1	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
STRAP STATE FOR BIT 0	OUT	OUT	IN	IN	IN	IN	IN	IN	IN	IN
ALSO STRAP 12-6 OUT, 13-12 IN, 27-28 OUT, 28-29 IN.										

Table 5.2 - STRAPS FOR 256 ADDRESS WINDOW POSITION

Example: When the board is shipped it is strapped with a 256 address window at location 764400_8, by the following strap configuration: 9-3 OUT, 8-2 IN, 7-1 IN, 11-5 OUT, 10-4 IN, 48-51 OUT, 49-52 OUT, 47-50 OUT, 35-33 IN, 34-36 IN.

5.2 I/O BASE ADDRESS STRAPS:

Table 5.3 shows how the QRGB-Alpha's I/O locations can be strapped on any 8 location boundary.

BASE ADDRESS BIT	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3
Corresponding Strap	19-14	20-15	21-16	22-17	23-18	46-41	45-40	44-39	43-38	42-37
Strap State for Bit = 0	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN
Strap State for Bit = 1	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT

Table 5.3 - I/O POSITION STRAPS

Example: When it is shipped the QRGB-Alpha I/O locations are positioned on base address 764000_8 by the following straps: 42-37 IN, 43-38 IN, 44-39 IN, 45-40 IN, 46-41 IN, 23-18 IN, 22-17 IN, 21-16 IN, 20-15 OUT, 19-14 IN. Note that if the system being used does not have memory management, these straps will automatically place the I/O space at 164000_8.

5.3 CHARACTER GENERATOR ACCESS STRAPS:

The Character Generator Memory can be accessed in transparent or non-transparent mode. The transparent mode allows the character generator to be accessed at any time without disrupting the display; however, it does require that the character generator be fast (150ns access with standard crystal). When the non-transparent mode is implemented, the memory can be slower (1.5us), but the display will be disrupted if access is not made during vertical blanking.

Transparent Access: 31-32 IN, 31-30 OUT, (As Shipped)
Non-Transparent Access: 30-31 IN, 31-32 OUT

5.4 VERTICAL AND HORIZONTAL SYNC/DRIVE STRAPS:

Straps can be installed to provide vertical and horizontal $\overline{\text{sync}}$ signals at pins 9 and 1 respectively of J3.

VERTICAL SYNC AT PIN 9 OF J3 = 82-83 IN
HORIZONTAL SYNC AT PIN 8 OF J3 = 76-77 IN

Vertical and horizontal drive signals can be strapped to be negative going or positive going.

VERTICAL DRIVE NEGATIVE GOING = 91-92 OUT, POSITIVE GOING = 91-92 IN
HORIZONTAL DRIVE NEGATIVE GOING = 87-88, POSITIVE GOING = 87-88 IN

When shipped sync signals are strapped as negative going and there are no $\overline{\text{sync}}$ signals on J3.

5.5 CHARACTER FONT SIZE STRAPS:

The QRGB-Alpha can be strapped to use 6 bit, 7 bit, 8 bit or 9 bit ASCII character codes to address fonts of 64, 128, 256, and 512 characters respectively. Normally, the 128 character configuration is used since it allows the full MCH-01 character set to be addressed while releasing D7 for attribute enable. The 64 character configuration does not address the MCH-01's lower case or graphics characters; however, it does provide an extra attribute enable bit (D6) which can be useful when the Display Memory is used in Extended Text Mode.

Although the MCH-01 only provides 128 characters, two methods can be used to address customized fonts of up to 256 characters. One method is to have each of the two character generator memory chips contain half of the 256 characters, and to strap D7 to address one chip or the other. The second method is to fit 256 characters into one of the character generator memories by reducing character cell height to 8 dots -D7 is strapped to replace R3 as character generator memory address CA3. Table 5.9 through 5.12 show the four strap configurations. Note that when CAB is not connected to D7 it is connected to CGS which allows character generator memory selection via Control Register 1.

A font of 512 characters can be generated by using two character generators of 25 characters each. A bit from the Attribute Memory must be strapped to CAB to address one or the other.

5.5 CHARACTER FONT SIZE STRAPS (Cont'd):

SOURCE	PIN	STRAP	PIN	DESTINATION
D5/	67	←	66	M6
D6	56			
D7	59		61	M8
SD7	29			
CGS	26	←	25	CAB
SD8	55			
R3	53	←	54	CA3

Table 5.9 - 64 CHARACTERS

SOURCE	PIN	STRAP	PIN	DESTINATION
D5/	67		66	M6
D6	56	←		
D7	59		61	M8
SD7	24			
CGS	26	←	25	CAB
SD8	55			
R3	53	←	54	CA3

Table 5.10- 128 CHARACTERS (AS-SHIPPED)

SOURCE	PIN	STRAP	PIN	DESTINATION
D5/	67		66	M6
D6	56	←		
D7	59		61	M8
SD7	24	→		
CGS	26		25	CAB
SD8	55			
R3	53	←	54	CA3

Table 5.11 - 256 CHARACTERS (2 CHIPS)

SOURCE	PIN	STRAP	PIN	DESTINATION
D5/	67		66	M6
D6	66	←		
D7	59	←	61	M8
SD7	24			
CGS	26	←	25	CAB
SD8	55	→		
R3	53		54	CA3

Table 5.12 - 256 CHARACTERS (1 CHIP)

5.6 CHARACTER ATTRIBUTE STRAPS:

SOURCE	PIN	STRAPS EXAMPLE	PIN	DESTINATION
D5	67		66	M6
D6	56	←		
D7	59	←	57	Underline (ULN)
GND	58	→	68	Extended Height (EXH)
H2	75			
$\overline{LD14}$	64	→	61	M8 (Single Character Generator, 256 Char.)
H3	63			
GND	74	→	65	Red Foreground (LD10)
H6	62			
GND	71	→	73	Foreground Blink of Foreground Disable*
H7	60			
GND	69	→	72	Red Background (LD14)
			70	Background Blink (BB)

* Foreground Blink = 86-85 IN, 85-84 OUT
Foreground Disable = 86-85 OUT, 85-84 IN (As shipped)

Table 5.13 - ATTRIBUTE STRAPPING PINS AND AS-SHIPPED STRAPS

5.6 CHARACTER ATTRIBUTE STRAPS (Cont'd):

Table 5.13 shows the wire wrap pins that are used to select character attributes to be enabled by data from the Display Memory. It also shows the pins used to select the 64 or 128 character set (6 bit or 7 bit ASCII character codes), and it gives the strap configurations implemented at the factory (as-shipped straps). The as-shipped configuration enables the use of all attributes except Foreground Blink, which is somewhat redundant when Background Blink is used. Note that D7 is strapped to enable both Underline and Extended Height. This is possible when the standard Character Height PROM is used (see sec 6.5) because Underline is not functional when Extended Height is used, and Extended Height can be disabled via Control Register 1 when Underline is used.

The as-shipped configuration uses a font of 128 characters which allows D7 to enable an attribute. If, however, a set of 256 characters is implemented (see section 5.5) D7 is not available for this purpose, and an attribute must be dropped. Underline/Extended Height can be dropped or another attribute can be sacrificed in its favour. In any case, the attribute line not used must be strapped to ground.

When the QRGB-Alpha is used in Extended Text Mode, colour attributes are not possible. The red output is used to provide monochrome video, and the Red Foreground and Red Background lines must be strapped accordingly. Red Foreground (Pin 65) must be strapped to LD14 (Pin 64) and Red Background (Pin 72) can be strapped to either ground or an attribute enable bit, if one is available; in the former case video is always normal; in the latter ease video is inverted when the attribute enable bit (D6 or D7) is high. Table 5.14 shows the wire wrap pins used for attribute configuration when Extended Text Mode is used, and it gives an example strap configuration for 128 characters with D7 enabling inverted video. Note that all unused attribute lines are grounded.

SOURCE	PIN	STRAP EXAMPLE	PIN	DESTINATION
D5	67		66	M6
D6	56		57	Underline (ULN)
D7	59		68	Extended Height (EXA)
GND	58		61	M8 (256 Characters in Single Generator)
$\overline{\text{LD14}}$	64		65	Red Foreground (LD10)
GND	74		73	Foreground Blink or Foreground Disable*
GND	71		72	Red Background (LD14)
GND	69		74	Background Blink (33)
*Foreground Blink = 86-85 IN, 85-84 OUT Foreground Disable = 86-85 OUT, 85-84 IN (As Shipped)				

Table 5.14 - ATTRIBUTE STRAP EXAMPLE FOR EXTENDED TEXT MODE

5.7 GRAPHICS DISABLE STRAPS:

When the QRGB-Alpha is used with the RGB-Graph graphics controller card, one of the background bits can be used to disable graphics in the background of any given character cell. There is, however, the restriction that the background colour strapped to disable graphics must be present in the background of all character cells. For example, if Blue Background (H5) is used, background colours are limited to blue, violet, blue-green, and white; if black, green, red or amber are used, graphics is enabled. Table 5.15 shows the straps that must be installed to select one of the background colours as graphics disable.

BACKGROUND COLOR	STRAPS		
	80-81	74-81	78-81
H6, RED	OUT	OUT	IN
H5, BLUE	OUT	IN	OUT
H4, GREEN	IN	OUT	OUT

Table 5.15 - GRAPHICS DISABLE STRAPS

6.0 CIRCUIT DESCRIPTION:

The schematics at the back of this manual and the block diagram in figure 6.1 should be referred to as the following circuit description is read. Note that where more than one gate is found in one I.C. that gate will be referred to in the following manner: A30-10 indicates the gate in A30 which has its output at pin 10.

6.0 CIRCUIT DESCRIPION (Cont'd):

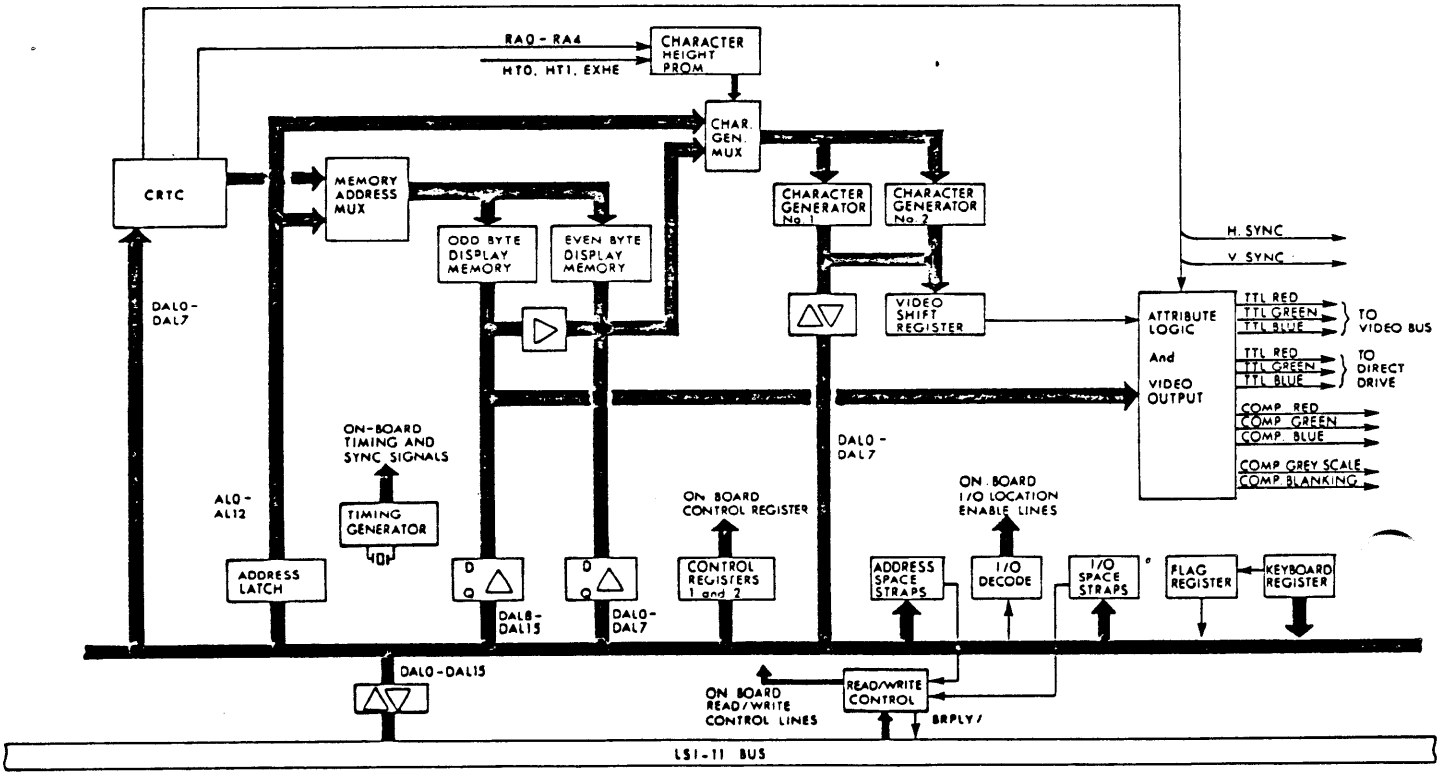


Figure 6.1 - QRGB-ALPHA BLOCK DIAGRAM

6.1 CRTC:

A LSI software programmable C.R.T. controller (CRTC) is used in the QRGB-Alpha. Once programmed, this I.C. (A30) using the Character Clock for synchronization, produces horizontal and vertical sync signals and generates sequential addresses, scanning through the display memory to refresh the display.

Data sheets on the CRTC are provided in section 12 and should be read for a full understanding of its functions.

.2 CLOCK CIRCUIT:

The QRGB-Alpha's clock circuit consists of a crystal controlled oscillator, and three programmable dividers arranged as illustrated in figure 6.2.

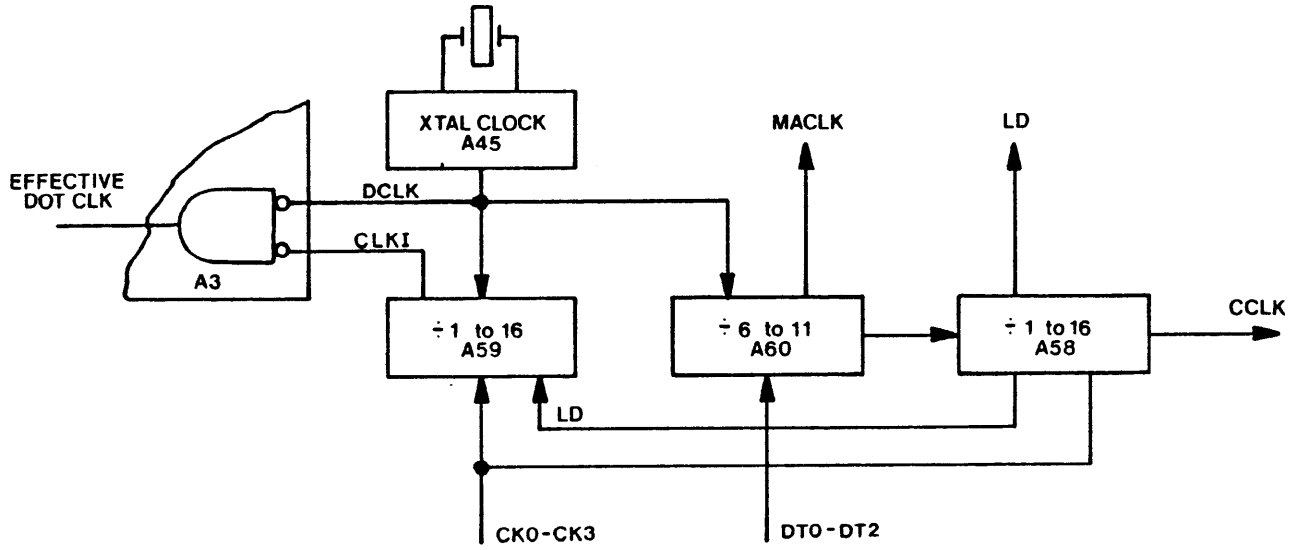


Figure 6.2 - PROGRAMMABLE CLOCK

A clock inhibit signal (CLKI) is produced in A59 by dividing the DCLK by a ratio set by CK0 through CK3 from Control Register 0 (A42). CLKI is used to inhibit DCLK in the serial shift register (A3), producing a programmable effective dot clock frequency. A60 divides DCLK by a divide of 6 to 11 depending on DT0 through DT2 from Control Register 0, and A58 divides the resulting signal by the same ratio used in A59, producing a Character Clock (CCLK) that is a submultiple of the effective dot clock frequency. The load signal (LD) is also produced in A58; it is used to synchronize DCLK with CCLK and to synchronize the video output section. The Memory Access Clock (MACLK), produced by A60, is used by the memory access control circuit described in section 6.8. Figure 6.3 shows a set of clock pulses for a typical format.

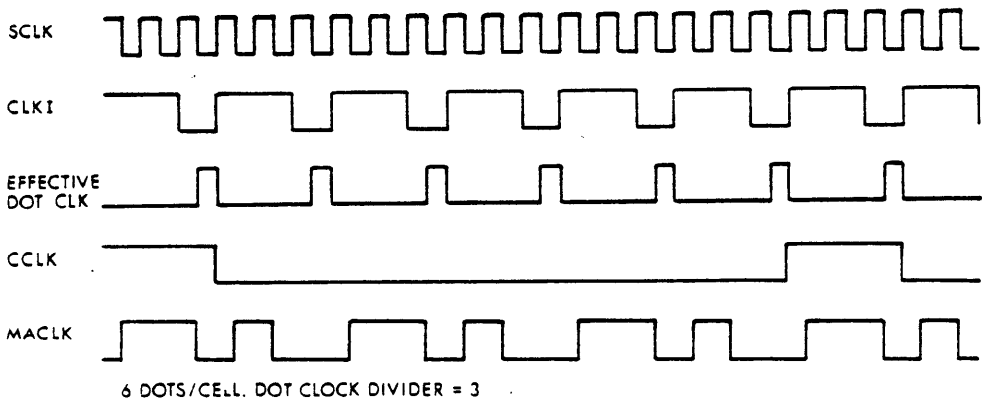


Figure 6.3 - TYPICAL CLOCK TIMING

6.3 DISPLAY MEMORY:

Figure 6.4 shows a simplified block diagram of the Display Memory and its associated access circuits. The block called High Low Select Logic determines how the Display Memory is accessed by decoding signals from the Control Register along with read/write signals, timing signals, and address bits.

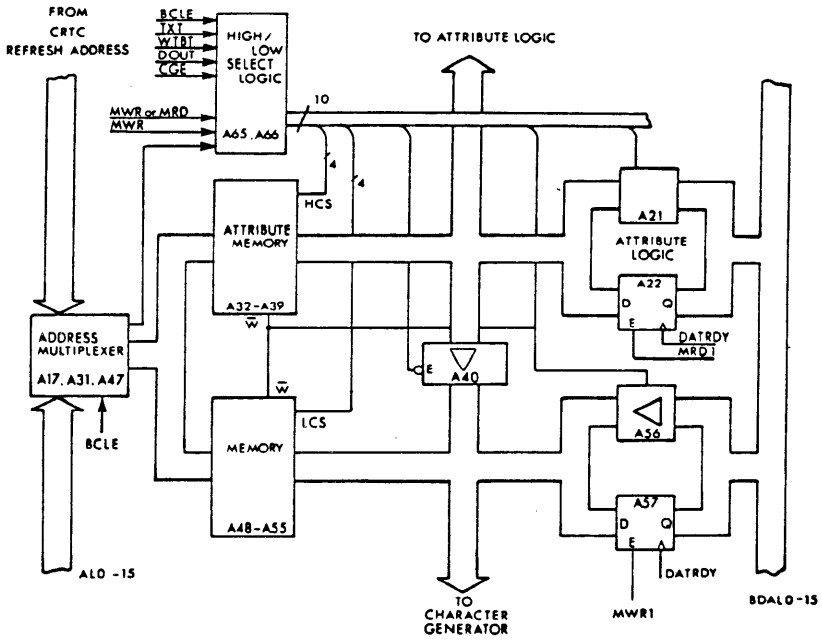


Figure 6.4 - DISPLAY MEMORY

6.4 CHARACTER GENERATOR:

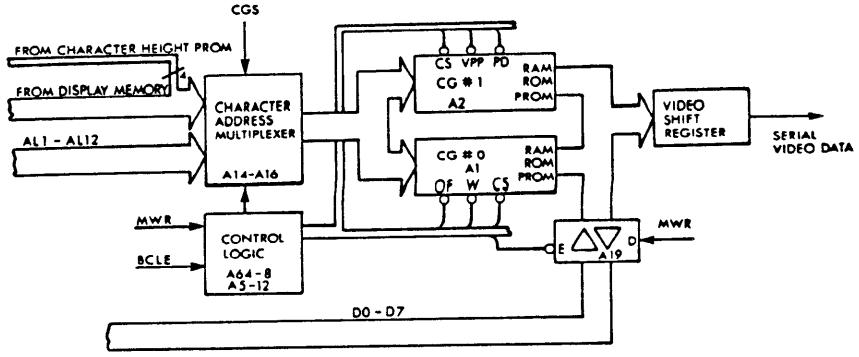


Figure 6.4 - CHARACTER GENERATOR

6.4 CHARACTER GENERATOR (Cont'd):

The QRGB-Alpha has positions for two character generator memories that can be either ROM (2316), EPROM (2516), or RAM (4016). The character generators can be used independently by selecting one or the other by CGS from Control Register 1, or a strap can be implemented which allows bit 7 of the character code to address one or the other, effectively combining the two 128 character memories as one font of 256 characters.

Figure 6.5 shows a block diagram of the character generator section. The multiplexer normally allows character codes from the Display Memory plus four bits from the Character Height PROM to address the character generator memory; however, when the character generator memory is accessed from off-board, the control logic causes the multiplexers to switch the address lines to the system bus.

6.5 CHARACTER HEIGHT LOGIC:

Character height functions on the QRGB-Alpha depend upon the PROM (A46) referred to as the Character Height PROM (C.H.P.). This PROM is divided into 16 sections of 32 locations each, as illustrated in figure 6.7, and addressing within each of these sections is done by RA0 through RA4 from the CRTC. (The CRTC can be programmed to use up to 32 scan lines per character row; RA0-RA4 represent the scan line count as the CRTC moves down through each character row.) When RA0-RA4 address a particular C.H.P. location, the 4 bit contents of that location, along with a character code from the Display Memory, address a byte in the Character Generator Memory (C.G.M.): the C.H.P. provides the least significant part of the address.

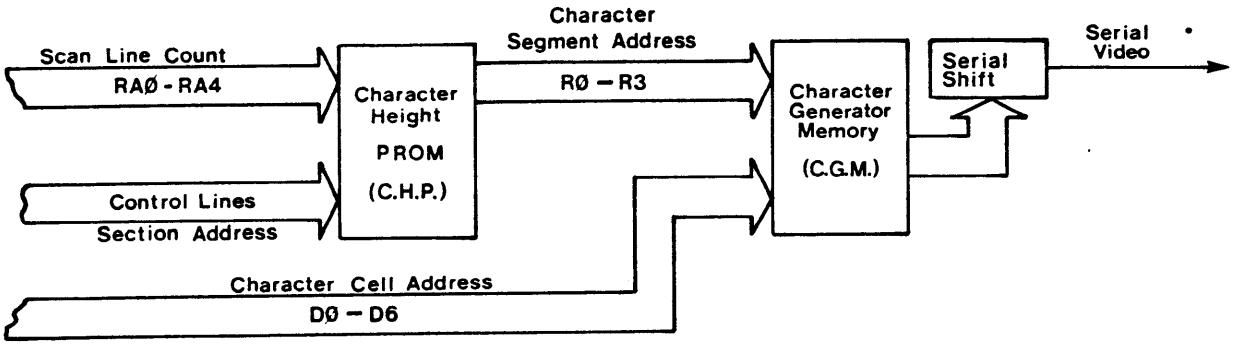


Figure 6.6 - SIMPLIFIED BLOCK DIAGRAM

The part of the C.G.M. address that comes from the Display Memory addresses small C.G.M. sections that contain the video information for one particular character. The four bits coming from the C.H.P. addresses individual bytes within these sections. Each byte is the video information for one horizontal section of the character cell. For example, looking at the character cell in figure 6.8, it is seen that 00100100 is the video information addressed by 2H from the C.H.P. As these bytes of video information are addressed, they are sent out to the display where they are stacked to form whole characters.

6.5 CHARACTER HEIGHT LOGIC (Cont'd):

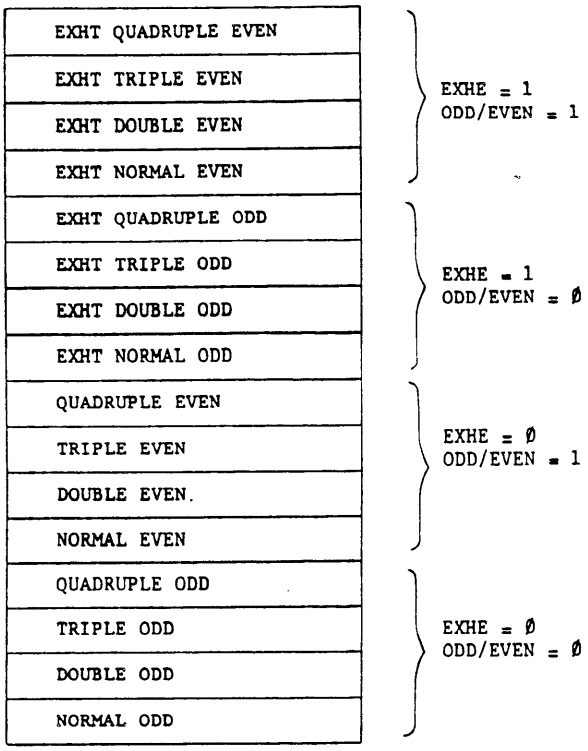


Figure 6.7 - CHARACTER HEIGHT PROM

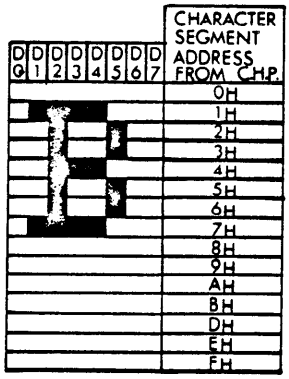


Figure 6.8 - CHARACTER CELL

Each 32 location section of the C.H.P. corresponds to a different addressing mode for the C.G.M. and the one selected is determined by HT0, HT1, EXH, EXHE, and an odd/even row signal from A62-9.

The addressing mode is determined by the way C.G.M. addresses are stored in the Character Height PROM. For example, in the Normal Height section, each location contains a different C.G.M. address, so when RA0-RA4 are addressing within that section, they cause a different segment of video data to be accessed on each consecutive scan line in the character row. On the other hand, in the Triple Height section of the C.H.P., each C.G.M. address is repeated three times in three consecutive addresses, and as a result, RA0-RA4 cause the same video data to be displayed on three consecutive scan lines, producing a character three times as high as a normal height character. Figure 4.1 shows the number of scan lines occupied by the different character heights.

5 CHARACTER HEIGHT LOGIC (Cont'd):

As explained in section 2.2, the Extended Height (EXHT) character attribute allows characters to be formed in two parts: the top half in a odd numbered row and the bottom half in the following even numbered row. In this way some characters in the text can be made larger that the rest. Eight C.H.P. sections are required to implement this function: an even row section (top of character) and an odd row section 1 (bottom of character) for each of the four character heights. Each of these EXHT sections has a different arrangement of C.G.M. addresses. In the EXHT Double Height section for even numbered rows, for example, each C.G.M. address is repeated 4 times, but only the first 5 addresses are given; as a result, the top half of the character is displayed in the same number of scan lines as an entire ordinary double height character. In the EXHT Double Height section for odd numbered rows, each C.G.M. address is also repeated four times, but only the video segments 5H-9H (see figure 6.8) are given, and only the bottom of the character is displayed. Note that because only 10 bytes of video information are used per character, the CRTC must, with one exeption, be programmed for exactly 10, 20, or 30 scan lines per row when Extended Height is used. The exeption is Quad Height where 32 scan lines per row can be used.

Also note that because the odd/even signal is present even when extended height is not used, two identical C.H.P. sections are required for each of the ordinary character heights.

6.6 CHARACTER ATTRIBUTE LOGIC:

When the QRGB-Alpha is in Normal Text Mode (see section 4.2.2) each odd memory byte contains 8 bits of attribute data: three bits for foreground colour, three bits for background colour, one bit for foreground blink or Foreground Disable, and one bit for background blink. Depending on the size of the ASCII code used, certain bits of the even bytes can also be used for attribute enable: bits 6 and 7 when 6 bit codes are used, and bit 7 alone when 7 bit codes are used. Before the attribute enable bits get to the attribute logic, some of them pass through the strapping area shown in figure 6.9. The straps indicated are those installed in the standard version at the factory.

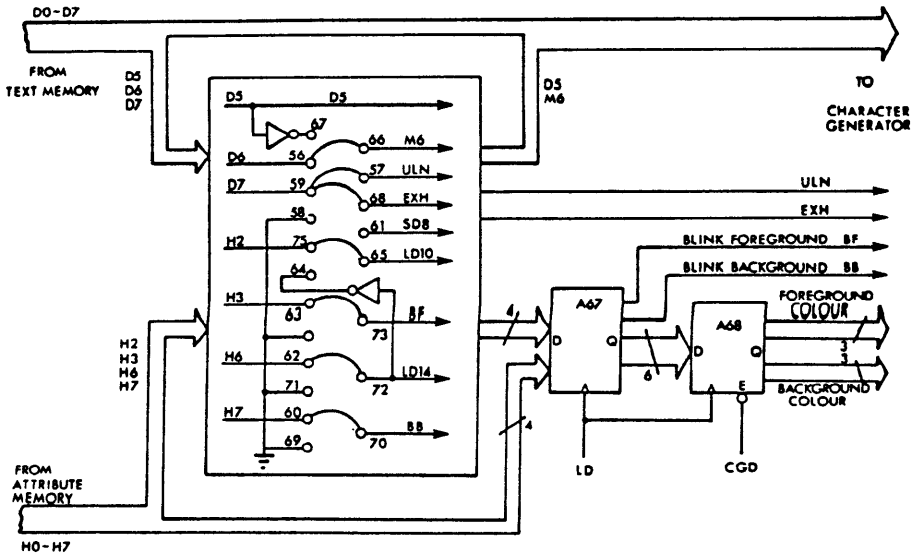


Figure 6.9 - ATTRIBUTE STRAPPING AREA

6.6 CHARACTER ATTRIBUTE LOGIC (Cont'd):

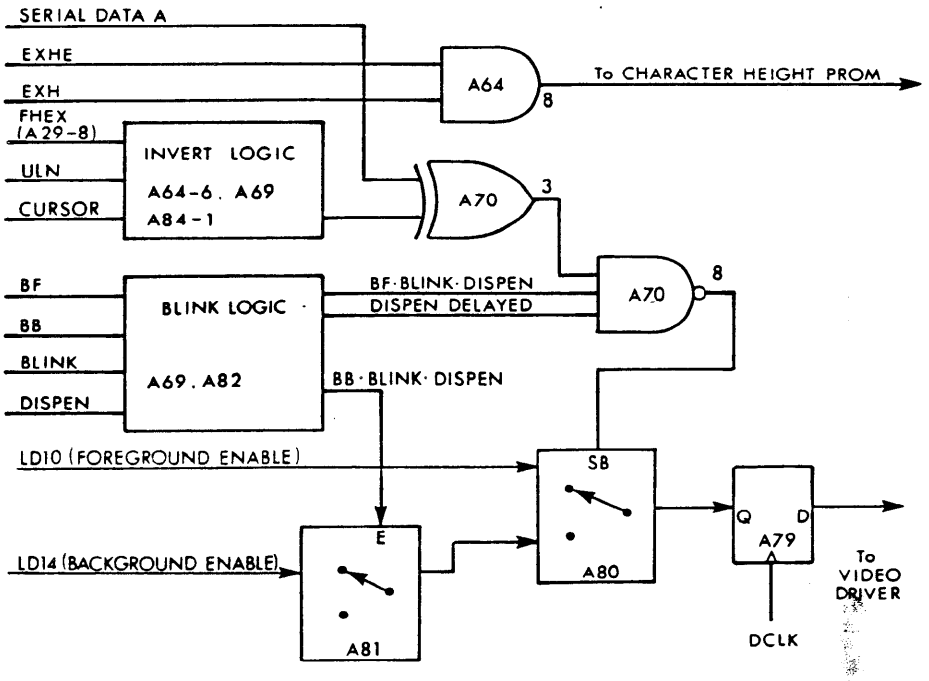


Figure 6.10 - ATTRIBUTE LOGIC

Figure 6.10 provides a simple block diagram of the character attribute logic. The colour attribute bits are converted into video signals in A80 which switches between foreground and background colour in response to the serial video signal. If the QRGB-Graph is used with the QRGB-Alpha, one of the background colour bits is used to switch A81 between background colour and graphics colour. The serial video signal can be disabled in A70 by the BF.BLINK signal, which oscillates at 2.8 Hz when foreground blink is enabled; or by DISPEN, which provides horizontal and vertical blanking. The exclusive OR gate, A84-3, inverts the serial video signal when the cursor signal from the CRTC is high or when both FHex and ULN are high. FHex indicates the portion of the character cell that must be inverted to underline a character, and it is decoded by A29 when Character Height PROM outputs, R0-R4, are all high (in effect FH). The Character Height PROM is programmed to produce FH during the 12th horizontal segment of each character cell; however, it should be noted that in many formats there is no 12th segment. Also note that the Extended Height Character attribute can be disabled by EXHE from Control Register 1.

6.7 VIDEO OUTPUT:

Red, green, and blue TTL video signals from A79 are mixed with horizontal and vertical sync signals in transistors Q4, Q5, Q6, and Q7, which drive the red, green, blue, and grey scale composite video signals. Q7 is a little different from the other colour drives in that it has two inputs from A79. In normal operation both these inputs receive exactly the same data (green); however, when the QRGB-Alpha is used with its companion graphics board, the QRGB-Graph, which has four bits of colour information two different bits go to Q7 where they can produce 4 different levels of green.

6.8 DISPLAY MEMORY ACCESS CONTROL:

As previously mentioned, both the system CPU and the CRTC can access the Display Memory. The CPU can do both read and write accesses, which it does to manipulate text. The CRTC, on the other hand, can only read the Display memory, which it does to refresh the display.

Since display refresh is an on-going process, it takes precedence over CPU accesses, which are less frequent; and the three multiplexers, (A17, A31, A47), normally connect the Display Memory address lines to the CRTC. The CRTC accesses the Display Memory only when CCLK is high, at which time the display data is placed in the latches of A17, A31, A47, A67, and A68. Because these latches mask the character generator from the Display Memory, the CPU can access the Display Memory whenever CCLK is low without disturbing the display. The signal which gives the CPU access to the Display Memory is BCLE. BCLE is produced by the two flip flops in A88 on the first rising edge of MACLK after both MRD + MWR and CCLK/ are present. BCLE switches the Display Memory's address multiplexers and data buffers to the system bus. When the external access is a read, data is latched into A57 and A22 by the trailing edge of BCLE. In this way, the CPU can pick up the data when it is able to, and display refresh can continue on with the next CCLK high cycle.

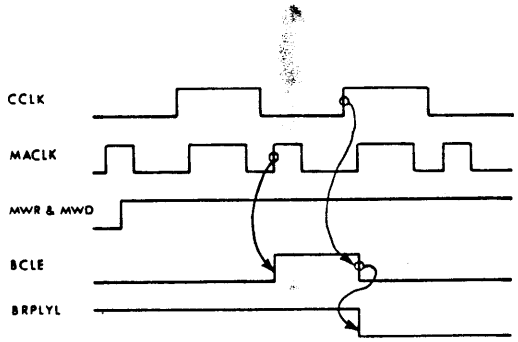


Figure 6.11 - EXTERNAL CPU ACCESS TO DISPALY MEMORY (6 DOTS/CELL)

Figure 6.11 shows the timing for a typical Display Memory access by the system CPU. Note that MWR + MWD is initiated by the CPU and can occur anywhere in the CCLK/MACLK cycle. The access time from BDINL or BDOUTL to BRPLYL depends on when in the cycle BDINL or BDOUTL occur and on MACLK which changes with the number of dots per cell programmed.

The character generator memories are accessed in a similar manner when they are strapped for transparent access (see section 5.3).

6.9 ADDRESS SPACE LOGIC:

The base address of the on-board RAM and I/O locations are determined by comparing address lines to a strapped logic condition via a series of bus comparators: A7 and A41 set the I/O space, and A28 and A6 set the memory address space. When a correct match is made, the read and write signals are gated through to the board via A13.

6.10 I/O DECODE:

I/O addresses are decoded in A26, and the resulting signals enable the I/O read/write functions on the board. The signals on pins 22 and 24 of the CRTC determine which CRTC location is to be accessed and whether the access is a write or a read; the operation is clocked at pin 23 by a pulse from A76-10. This clock pulse is produced by A44 when either of the first two I/O addresses is decoded.

6.11 BRPLYL:

The BRPLYL circuit is composed of Q2, A44-6, A12-10 and 12-4. The one shot, A44, is triggered by any I/O or memory access and generates BRPLYL when its Q output goes low. During I/O access or non-transparent Character Generator Memory accesses, it waits the full timing period of 1.5 us before going low; however, during Display memory accesses, it is prematurely pulled by low BCLE/.

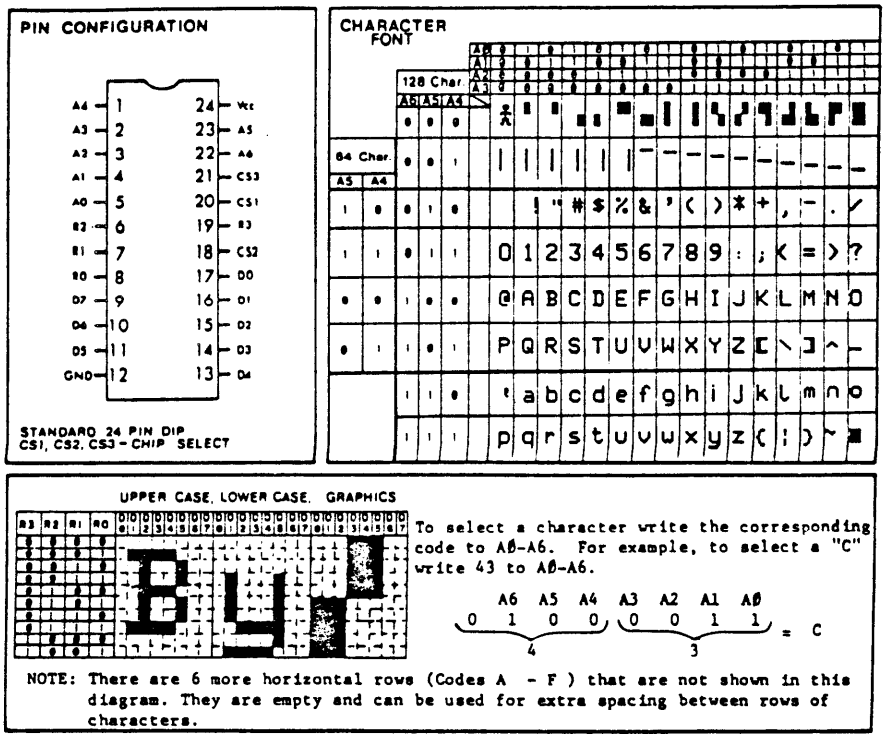
6.12 KEYBOARD INTERFACE:

The Keyboard interface is composed of A72 and A71. Data from the keyboard is latched into A71 by the keyboard strobe which also clocks A72 setting the keyboard flag in the Flag Register. When the CPU reads the Keyboard Register (A71) it presets A72.

7.0 MCH-01 CHARACTER GENERATOR:

The QRGB-Alpha is provided with the Matrox MCH-01 character generator, which has a set of 128 characters. The board can be configured to use all 128 characters with a 7 bit ASCII code or to use a reduced set of 64 characters with a 6 bit ASCII code. In th latter case, the graphics and lower case characters are not used (see sec 5.6 foı straps).

It should be noted that the MCH-01 is pin compatible with the 2516 EPROM. This allows the user to replace the MCH-01 with his own custom character generator.



8.0 CONNECTORS:

8.1 BUS CONNECTOR (P1):

The bus connector consists of four 36 pin edge connectors, A, B, C, and D which are collectively referred to as P1. The pin-out of these connectors is given in tables 8.1 through 8.4.

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
AA1	N.C.	AA2	+5V
AB1	N.C.	AB2	N.C.
AC1	BAL16L	AC2	GROUND
AD1	BAL17L	AD2	N.C.
AE1	N.C.	AE2	BDOUTL
AF1	N.C.	AF2	BRPLYL
AH1	N.C.	AH2	BDINL
AJ1	GROUND, SYSTEM SIGNAL GROUND	AJ2	BSYNCL
AK1	N.C.	AK2	BWTBTL
AL1	N.C.	AL2	N.C.
AM1	GROUND	AM2	BIAKIL
AN1	N.C.	AN2	BIAKOL
AP1	N.C.	AP2	BBS7L
AR1	N.C.	AR2	BDM61L
AS1	N.C.	AS2	BDM60L
AT1	GROUND, SYSTEM SIGNAL GROUND	AT2	BINITL
AU1	N.C.	AU2	BDALØL
AV1	N.C.	AV2	BDAL1L

Table 8.1 - P1-A

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
BA1	N.C.	BA2	+5V
BB1	N.C.	BB2	N.C.
BC1	N.C.	BC2	GROUND
BD1	N.C.	BD2	N.C.
BE1	N.C.	BE2	BDAL2L
BF1	N.C.	BF2	BDAL3L
BH1	N.C.	BH2	BDAL4L
BJ1	GROUND	BJ2	BDAL5L
BK1	N.C.	BK2	BDAL6L
BL1	N.C.	BL2	BDAL7L
BM1	GROUND	BM2	BDAL8L
BN1	N.C.	BN2	BDAL9L
BP1	N.C.	BP2	BDAL10L
BR1	N.C.	BR2	BDAL11L
BS1	N.C.	BS2	BDAL12L
BT1	GROUND	BT2	BDAL13L
BU1	N.C.	BU2	BDAL14L
BV1	+5V	BV2	BDAL15L

Table 8.2 - P1-B

8.3 J2 (COMPOSITE VIDEO):

J2 is an 10 pin right angle header (AMP 87578-2) used to output the composite vide signals. The pin assignment is shown in table 8.6.

PIN	SIGNAL	PIN	SIGNAL
1	COMPOSITE GREY SCALE	6	GROUND
2	GROUND	7	COMPOSITE BLUE
3	COMPOSITE RED	8	GROUND
4	GROUND	9	RESERVED
5	COMPOSITE GREEN	10	GROUND

Table 8.6 - J2 PIN ASSIGNMENT

8.4 J3 (VIDEO BUS):

J3 is a 50 pin right angle header (Molex 10-55-3505), and it is mainly used to interface the QRGB-Alpha with its sister graphics card, the RGB-Graph. Table 8.7 shows the pin assignment.

PIN	SIGNAL	PIN	SIGNAL
1	GROUND	26	N.C.
2	EXTERNAL CLOCK	27	
3	GROUND	28	GROUND
4	EXTERNAL CCLK SYNC/	29	RESERVED
5	GROUND	30	
6	EXTERNAL FIELD SYNC	31	
7	GROUND	32	
8	HORIZONTAL SYNC/	33	
9	VERTICAL SYNC/	34	
10	COMPOSITE BLANKING/	35	
11	GROUND	36	
12	QRGB-GRAPH #1 INPUT	37	GROUND
13		38	RED TTL VIDEO OUTPUT
14		39	BLUE TTL VIDEO OUTPUT
15		40	GREEN TTL VIDEO OUTPUT
16	N.C.	41	BG TTL VIDEO
17		42	GROUND
18		43	RESERVED
19		44	
20		45	
21		46	
22		47	
23		48	GROUND
24		49	RESERVED
25		50	

Table 8.7 - J3 PIN ASSIGNMENT

8.1 BUS CONNECTORS (P1) A and B (Cont'd):

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
CA1 ↑ ↓	N.C.	CA2	+5V
		CB2	N.C.
		CC2	GROUND
		CD2 ↕ CL2	N.C.
		CM2	BIAKIL
		CN2	BIAKOL
		CP2	N.C.
		CR2	BDM61L
		CS2	BDM60L
		AT2 ↓	N.C.

Table 8.3 - P1-C

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
DA1 ↕ DS1		DA2	+5V
		DB2	N.C.
		DC2	GROUND
DT1	GROUND	DD2 ↕ DV2	NOT CONNECTED
DU1	N.C.		
DV1	-5V		

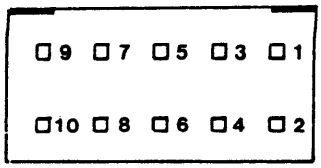
Table 8.4 - P1-D

8.2 J1 (TTL VIDEO AND POWER SOURCE):

J1 is a 10 pin right angle header (AMP 87578-2), and supplies TTL video. Table 8.5 shows the pin assignment.

PIN	SIGNAL	PIN	SIGNAL
1	H. DRIVE/	6	GROUND
2	GROUND	7	TTL BLUE
3	TTL RED	8	GROUND
4	GROUND	9	V. DRIVE/
5	TTL GREEN	10	GROUND

Table 8.5 - J1 PIN ASSIGNMENT



PIN CONFIGURATION LOOKING INTO J1 OR J2

8.5 J4 (KEYBOARD, LIGHT PEN):

J4 is a 26 pin right angle header (Molex 10-55-3265), and it is used for keyboard and light-pen signals. Table 8.8 shows the pin assignment.

PIN	SIGNAL	PIN	SIGNAL
1	+5V	2	+5V
3	KD3	4	GROUND
5	KD2	6	GROUND
7	KD1	8	GROUND
9	KD0	10	GROUND
11	KD7	12	GROUND
13	KD6	14	GROUND
15	KD5	16	GROUND
17	KD4	18	GROUND
19	LPEN EN	20	GROUND
21	LPEN STR	22	GROUND
23	N.C.	24	K STB
25	+5V	26	+5V

Table 8.8 - J4 PIN ASSIGNMENT

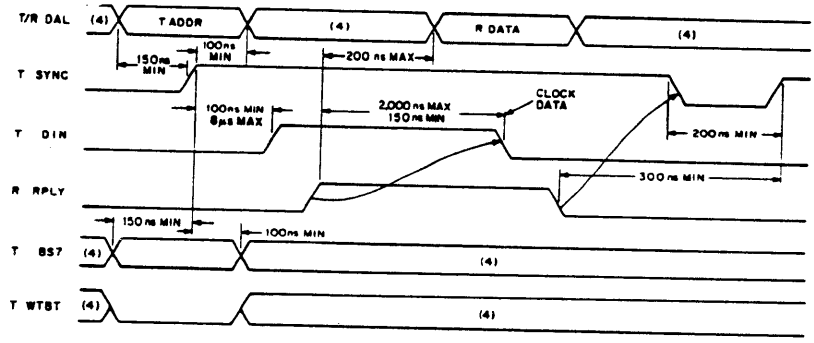
9.0 READ/WRITE TIMING:

The QRGB-Alpha conforms to the standard LSI-11 timing set out in figures 9.1 and 9.2. The time from BDINL or BDOUTL to BREPLY varies depending on the type of access, the character cell format, the XTAL frequency, and the position of the access request with respect to the internal refresh cycle. It is always 1500ns for access to registers an access to character generator memory when it is strapped in the non-transparent mode (see section 5.4). Table 9.1 shows the worst and best case access times for the Display Memory and the Character Generator when the as-shipped crystal is used. The average access time decreases as formats become less dense.

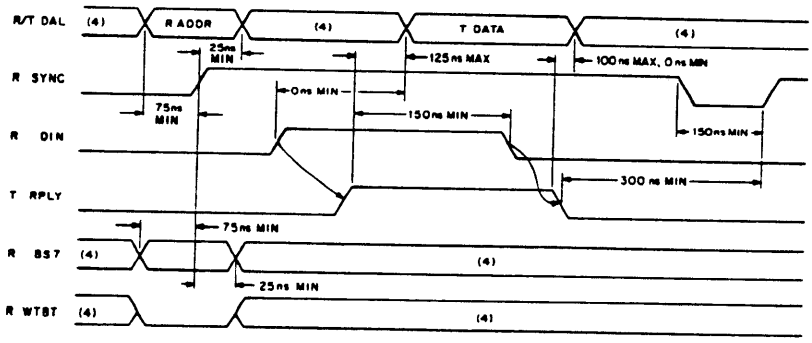
HORIZONTAL DOTS PER CELL		6	7	8	9	10	11
Time from BDINL or BDOUTL to BRPLY	WORST CASE	870ns	1050ns	1130ns	1220ns	960ns	1050ns
	BEST CASE	315ns	400ns	400ns	400ns	315ns	400ns

Table 9.1 - ACCESS TIMES

9.0 READ/WRITE TIMING (Cont'd):



TIMING AT MASTER DEVICE



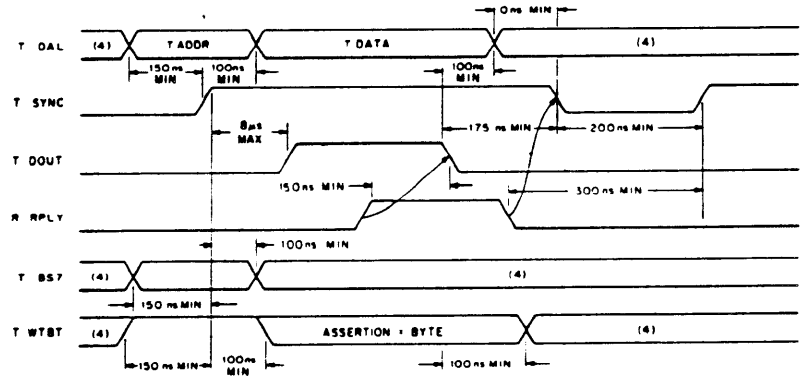
TIMING AT SLAVE DEVICE

NOTES:

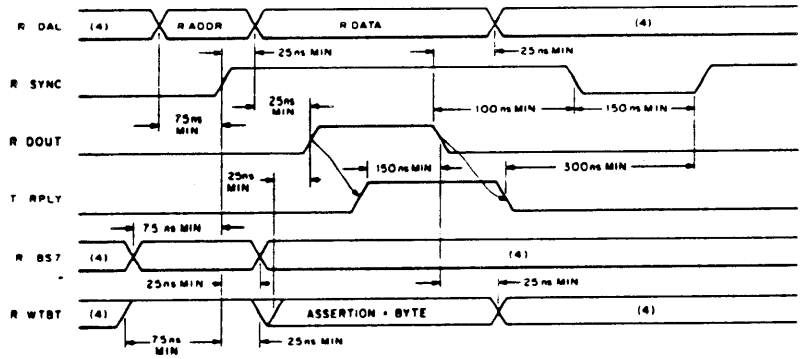
1. Timing shown at Master and Slave Device Bus Driver inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix
4. Don't care condition

Figure 9.1 - LSI-11 DAT/ BUS CYCLE TIMING

9.0 READ/WRITE TIMING (Cont'd):



TIMING AT MASTER DEVICE



TIMING AT SLAVE DEVICE

NOTES

1. Timing shown at Master and Slave Device Bus Driver inputs and Bus Receiver Outputs
2. Signal name prefixes are defined below
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix
4. Don't care condition

Figure 9.2 - LSI-11 DATO or DATOB BUS CYCLE TIMING

10.0 MAINTENANCE & WARRANTY:

Matrox products are warranted against defects in materials and workmanship for a period of 180 days from date of delivery. We will repair or replace products which prove to be defective during the warranty period, provided they are returned to Matrox Electronic Systems Limited. No other warranty is expressed or implied. We are not liable for consequential damages.

11.0 ORDERING INFORMATION:

The QRGB-Alpha can be ordered directly from Matrox Electronic Systems Limited or from its worldwide network of distributors.

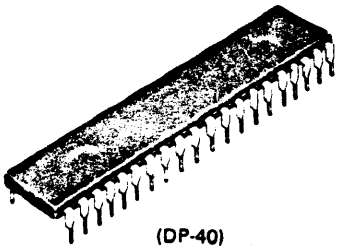
CRTC DATA SHEETS

HD6845S, HD68A45S, HD68B45S

CRTC (CRT Controller)

The CRTC is a LSI controller which is designed to provide an interface for microcomputers to raster scan type CRT displays. The CRTC belongs to the HMCS6800 LSI Family and has full compatibility with MPU in both data lines and control lines. Its primary function is to generate timing signal which is necessary for raster scan type CRT display according to the specification programmed by MPU. The CRTC is also designed as a programmable controller, so applicable to wide-range CRT display from small low-functioning character display up to raster type full graphic display as well as large high-functioning limited graphic display.

HD6845SP, HD68A45SP, HD68B45SP

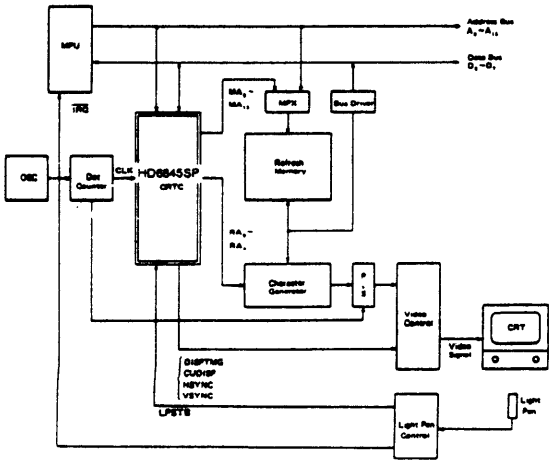


(DP-40)

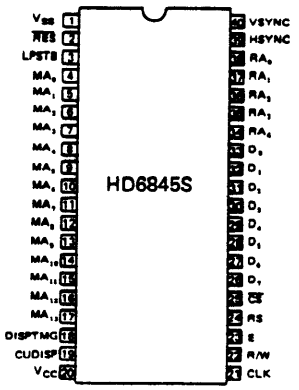
■ FEATURES

- Number of Displayed Characters on the Screen, Vertical Dot Format of One Character, Horizontal and Vertical Sync Signal, Display Timing Signal are Programmable
- 3.7 MHz High Speed Display Operation
- Line Buffer-less Refreshing
- 14-bit Refresh Memory Address Output (16k Words max. Access)
- Programmable Interlace/Non-interlace Scan Mode
- Built-in Cursor Control Function
- Programmable Cursor Height and its Blink
- Built-in Light Pen Detection Function
- Paging and Scrolling Capability
- TTL Compatible
- Single +5V Power Supply
- Upward compatible with MC6845

■ SYSTEM BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ORDERING INFORMATION

CRTC	Bus Timing	CRT Display Timing
HD6845SP	1.0 MHz	3.7 MHz max.
HD68A45SP	1.5 MHz	
HD68B45SP	2.0 MHz	

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} *	−0.3 ~ +7.0	V
Input Voltage	V_{in} *	−0.3 ~ +7.0	V
Operating Temperature	T_{opr}	− 20 ~ + 75	°C
Storage Temperature	T_{stg}	− 55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC} *	4.75	5	5.25	V
Input Voltage	V_{IL} *	−0.3	−	0.8	V
	V_{IH} *	2.0	−	V_{CC}	V
Operating Temperature	T_{opr}	− 20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = 0V, Ta = −20~+75°C, unless otherwise noted.)

Item	Symbol	Test Condition		min	typ	max	Unit
Input "High" Voltage	V_{IH}			2.0	−	V_{CC}	V
Input "Low" Voltage	V_{IL}			−0.3	−	0.8	V
Input Leakage Current	I_{in}	V_{in} = 0 ~ 5.25V (Except D_0~D_7)		−2.5	−	2.5	μA
Three-State Input Current (off-state)	I_{TSI}	V_{in} = 0.4 ~ 2.4V V_{CC} = 5.25V (D_0~ D_7)		− 10	−	10	μA
Output "High" Voltage	V_{OH}	I_{LOAD} = −205 μA (D_0~ D_7)		2.4	−	−	V
		I_{LOAD} = −100 μA (Other Outputs)					
Output "Low" Voltage	V_{OL}	I_{LOAD} = 1.6 mA		−	−	0.4	V
Input Capacitance	C_{in}	V_{in} = 0 Ta = 25°C f = 1.0 MHz	D_0 ~ D_7	−	−	12.5	pF
			Other Inputs	−	−	10.0	pF
Output Capacitance	C_{out}	V_{in} = 0V, Ta = 25°C, f = 1.0 MHz		−	−	10.0	pF
Power Dissipation	P_D			−	600	1000	mW

- AC CHARACTERISTICS (V_{CC} = 5V ±5%, V_{SS} = 0V, Ta = -20~+75°C, unless otherwise noted.)

1. TIMING OF CRTC SIGNAL

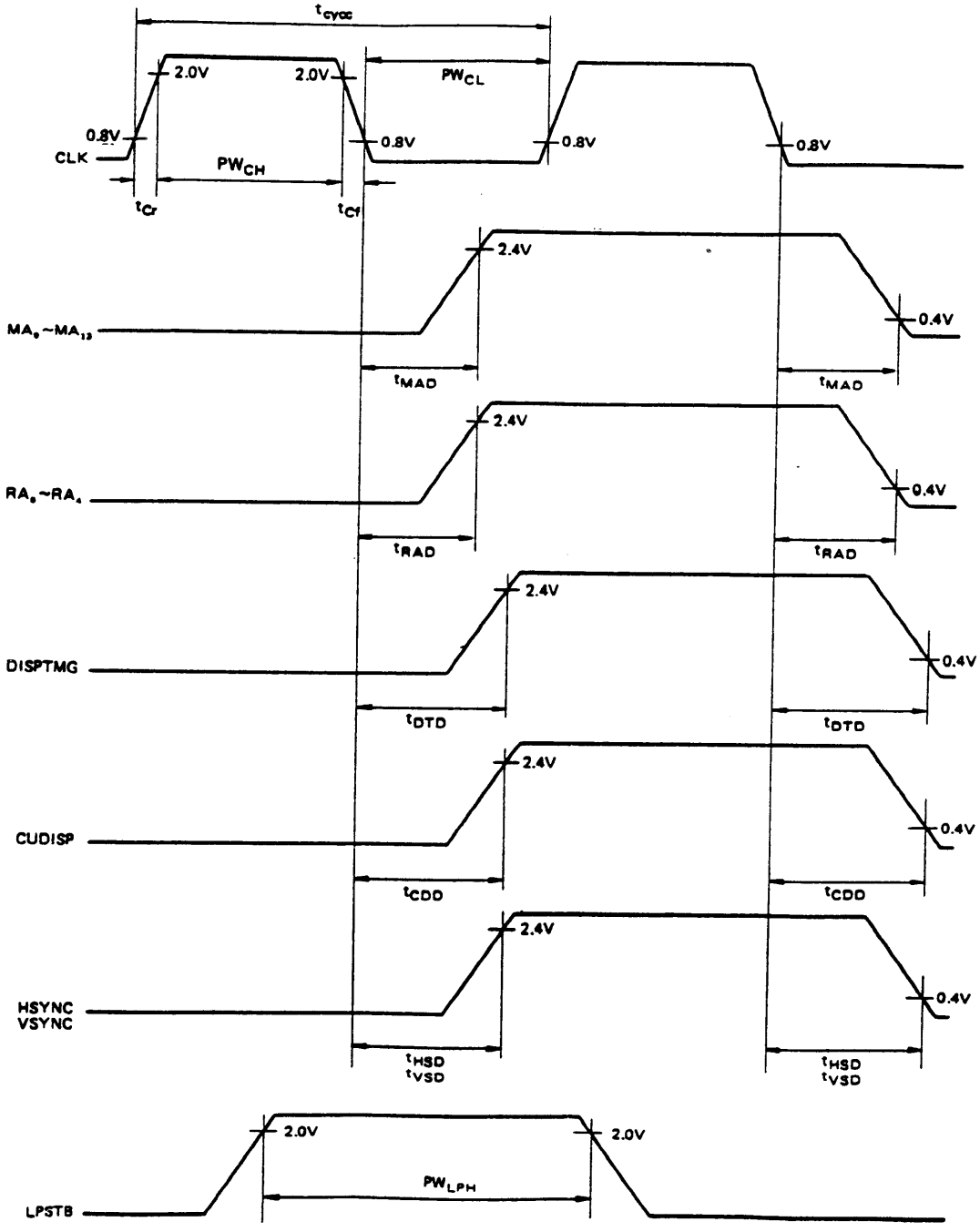
Item	Symbol	Test Condition	min	typ	max	Unit
Clock Cycle Time	t_{cycc}	Fig. 1	270	–	–	ns
Clock "High" Pulse Width	PW_{CH}		130	–	–	ns
Clock "Low" Pulse Width	PW_{CL}		130	–	–	ns
Rise and Fall Time for Clock Input	t_{Cr}, t_{Cf}		–	–	20	ns
Memory Address Delay Time	t_{MAD}		–	–	160	ns
Raster Address Delay Time	t_{RAD}		–	–	160	ns
DISPTMG Delay Time	t_{DTD}		–	–	250	ns
CUDISP Delay Time	t_{CDD}		–	–	250	ns
Horizontal Sync Delay Time	t_{HSD}		–	–	200	ns
Vertical Sync Delay Time	t_{VSD}		–	–	250	ns
Light Pen Strobe Pulse Width	PW_{LPH}		60	–	–	ns
Light Pen Strobe	t_{LPD1}	Fig. 2	–	–	70	ns
Uncertain Time of Acceptance	t_{LPD2}		–	–	0	ns

2. MPU READ TIMING

Item	Symbol	Test Condition	HD6845SP			HD68A45SP			HD68B45SP			Unit
			min	typ	max	min	typ	max	min	typ	max	
Enable Cycle Time	t_{cycE}	Fig. 3	1.0	–	–	0.666	–	–	0.5	–	–	μs
Enable "High" Pulse Width	PW_{EH}		0.45	–	–	0.280	–	–	0.22	–	–	μs
Enable "Low" Pulse Width	PW_{EL}		0.40	–	–	0.280	–	–	0.21	–	–	μs
Enable Rise and Fall Time	t_{Er}, t_{Ef}		–	–	25	–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}		140	–	–	140	–	–	70	–	–	ns
Data Delay Time	t_{DDR}		–	–	320	–	–	220	–	–	180	ns
Data Hold Time	t_H		10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}		10	–	–	10	–	–	10	–	–	ns
Data Access Time	t_{ACC}		–	–	460	–	–	360	–	–	250	ns

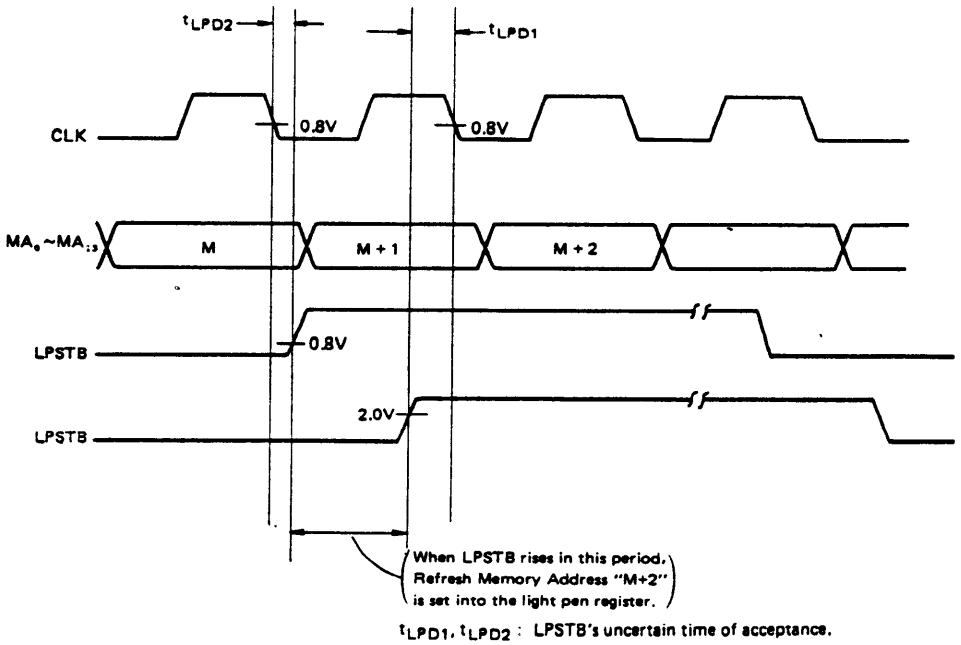
3. MPU WRITE TIMING

Item	Symbol	Test Condition	HD6845SP			HD68A45SP			HD68B45SP			Unit
			min	typ	max	min	typ	max	min	typ	max	
Enable Cycle Time	t_{cycE}	Fig. 4	1.0	–	–	0.666	–	–	0.5	–	–	μs
Enable "High" Pulse Width	PW_{EH}		0.45	–	–	0.280	–	–	0.22	–	–	μs
Enable "Low" Pulse Width	PW_{EL}		0.40	–	–	0.280	–	–	0.21	–	–	μs
Enable Rise and Fall Time	t_{Er}, t_{Ef}		–	–	25	–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}		140	–	–	140	–	–	70	–	–	ns
Data Set Up Time	t_{DSW}		195	–	–	80	–	–	60	–	–	ns
Data Hold Time	t_H		10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}		10	–	–	10	–	–	10	–	–	ns



This Figure shows the relation in time between CLK signal and each output signals. Output sequence is shown in Figs. 9 ~ 15.

Figure 1 Time Chart of the CRTC



t_{LPD1}, t_{LPD2} : LPSTB's uncertain time of acceptance.

Figure 2 LPSTB Input Timing & Refresh Memory Address that is set into the light pen register.

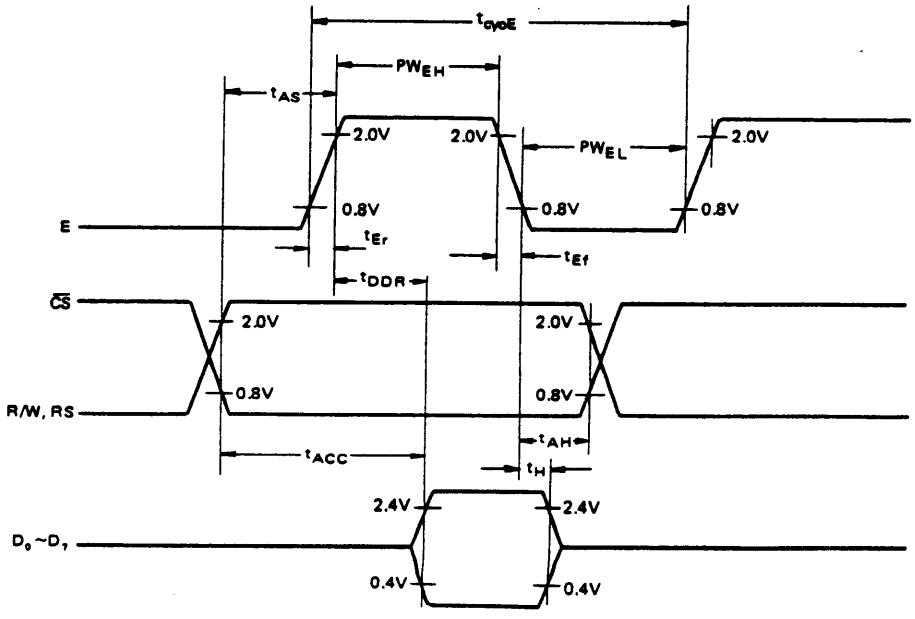


Figure 3 Read Sequence

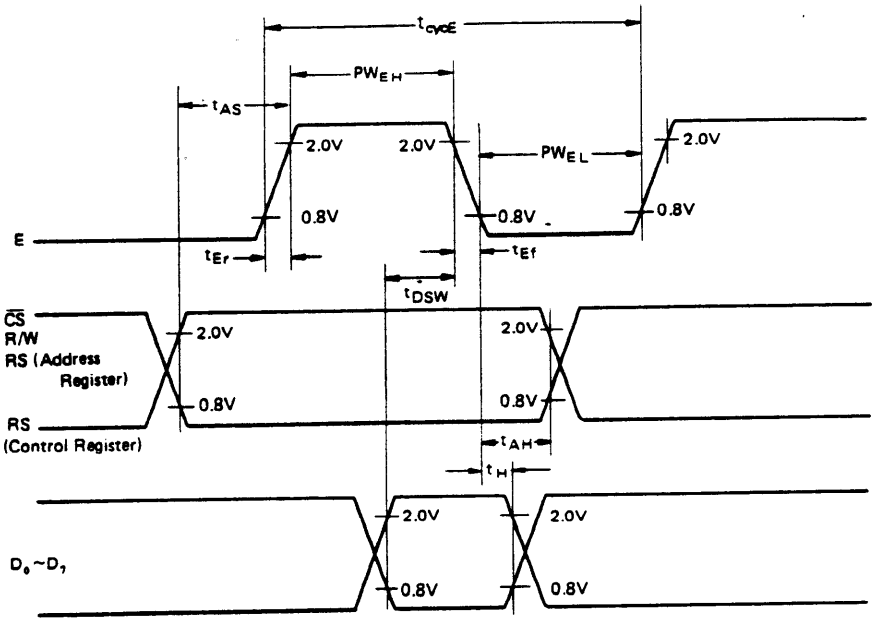


Figure 4 Write Sequence

■ SYSTEM DESCRIPTION

The CRTC is a LSI which is connected with MPU and CRT display device to control CRT display. The CRTC consists of internal register group, horizontal and vertical timing circuits, linear address generator, cursor control circuit, and light pen detection circuit. Horizontal and vertical timing circuit generate RA_0~RA_4, DISPTMG, HSYNC, and VSYNC. RA_0~RA_4 are raster address signals and used as input signals for Character Generator. DISPTMG, HSYNC, and VSYNC signals are received by video control circuit. This horizontal and vertical timing circuit consists of internal counter and comparator circuit. Linear address generator generates refresh memory address MA_0 ~MA_{13} to be used for refreshing the screen. By these address signals, refresh memory is accessed periodically. As 14 refresh memory address signals are prepared, 16k words max are accessible. Moreover, the use of start address register enables paging and scrolling. Light pen detection circuit detects light pen position on the screen. When light pen strobe signal is received, light pen register memorizes linear address generated by linear address generator in order to memorize where light pen is on the screen. Cursor control circuit controls the position of cursor, its height, and its blink.

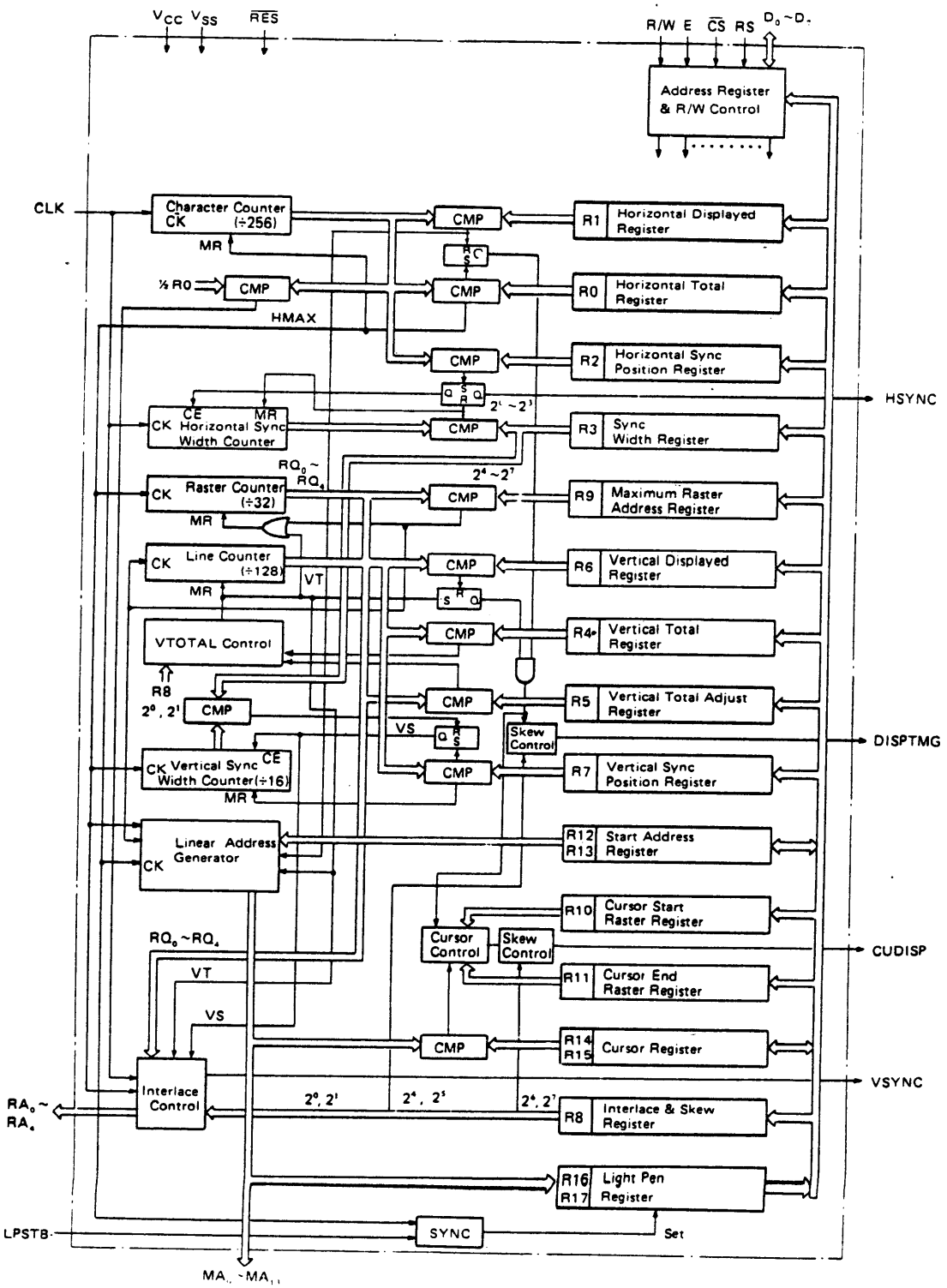


Figure 5 Internal Block Diagram of the CRTC

■ FUNCTION OF SIGNAL LINE

The CRTC provides 13 interface signals to MPU and 25 interface signals to CRT display.

• Interface Signals to MPU

Bi-directional Data Bus (D_0~D_7)

Bi-directional data bus(D_0~D_7) are used for data transfer between the CRTC and MPU. The data bus outputs are 3-state buffers and remain in the high-impedance state except when MPU performs a CRTC read operation.

Read/Write (R/W)

R/W signal controls the direction of data transfer between the CRTC and MPU. When R/W is at "High" level, data of CRTC is transfered to MPU. When R/W is at "Low" level, data of MPU is transfered to CRTC.

Chip Select ($\overline{CS}$)

Chip Select signal ($\overline{CS}$) is used to address the CRTC. When $\overline{CS}$ is at "Low" level, it enables R/W operation to CRTC internal registers. Normally this signal is derived from decoded address signal of MPU under the condition that VMA signal of MPU is at "High" level.

Register Select (RS)

Register Select signal (RS) is used to select the address register and 18 control registers of the CRTC. When RS is at "Low" level, the address register is selected and when RS is at "High" level, control registers are selected. This signal is normally a derivative of the lowest bit (A0) of MPU address bus.

Enable(E)

Enable signal (E) is used as strobe signal in MPU R/W operation with the CRTC internal registers. This signal is normally a derivative of the HMCS6800 System ϕ_2 clock.

Reset ($\overline{RES}$)

Reset signal ($\overline{RES}$) is an input signal used to reset the CRTC.

When $\overline{RES}$ is at "Low" level, it forces the CRTC into the following status.

1) All the counters in the CRTC are cleared and the device stops the display operation.
2) All the outputs go down to "Low" level.
3) Control registers in the CRTC are not affected and remain unchanged.

This signal is different from other HMCS6800 family LSIs in the following functions and has restrictions for usage.

1) $\overline{RES}$ signal has capability of reset function only when LPSTB is at "Low" level.
2) The CRTC starts the display operation immediately after $\overline{RES}$ signal goes "High".

This statement seems to be in error. At Matrox we have found that one field is blanked out following the release of RES.

• Interface Signals to CRT Display Device

Character Clock (CLK)

CLK is a standard clock input signal which defines character timing for the CRTC display operation. This signal is normally derived from the external high-speed dot timing logic.

Horizontal Sync (HSYNC)

HSYNC is an active "High" level signal which provides horizontal synchronization for display device.

Vertical Sync (VSYNC)

VSYNC is an active "High" level signal which provides vertical synchronization for display device.

Display Timing (DISPTMG)

DISPTMG is an active "High" level signal which defines the display period in horizontal and vertical raster scanning. It is necessary to enable video signal only when DISPTMG is at "High" level.

Refresh Memory Address (MA_0~MA_{13})

MA_0~MA_{13} are refresh memory address signals which are used to access to refresh memory in order to refresh the CRT screen periodically. These outputs enables 16k words max. refresh memory access. So, for instance, these are applicable up to 2000 characters/screen and 8-page system.

Raster Address (RA_0~RA_4)

RA_0~RA_4 are raster address signals which are used to select the raster of the character generator or graphic pattern generator etc.

Cursor Display (CUDISP)

CUDISP is an active "High" level video signal which is used to display the cursor on the CRT screen. This output is inhibited while DISPTMG is at "Low" level. Normally this output is mixed with video signal and provided to the CRT display device.

Light Pen Strobe (LPSTB)

LPSTB is an active "High" level input signal which accepts strobe pulse detected by the light pen and control circuit. When this signal is activated, the refresh memory address (MA_0~MA_{13}) which are shown in Fig. 2 are stored in the 14-bit light pen register. The stored refresh memory address need to be corrected in software, taking the delay time of the display device, light pen, and light pen control circuits into account.

■ REGISTER DESCRIPTION

Table 1 Internal Registers Assignment

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register Name	Program Unit	READ	WRITE	Data Bit 7	6	5	4	3	2	1	0
1	×	×	×	×	×	×			–	–	–								
0	0	×	×	×	×	×	AR	Address Register	–	×	O								
0	1	0	0	0	0	0	R0	Horizontal Total *	Character	×	O								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Character	×	O								
0	1	0	0	0	1	0	R2	Horizontal Sync* Position	Character	×	O								
0	1	0	0	0	1	1	R3	Sync Width	Vertical-Raster, Horizontal-Character	×	O	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0	0	1	0	0	R4	Vertical Total *	Line	×	O								
0	1	0	0	1	0	1	R5	Vertical Total Adjust	Raster	×	O								
0	1	0	0	1	1	0	R6	Vertical Displayed	Line	×	O								
0	1	0	0	1	1	1	R7	Vertical Sync * Position	Line	×	O								
0	1	0	1	0	0	0	R8	Interlace & Skew	–	×	O	C1	C0	D1	D0			V	S
0	1	0	1	0	0	1	R9	Maximum Raster Address	Raster	×	O								
0	1	0	1	0	1	0	R10	Cursor Start Raster	Raster	×	O		B	P					
0	1	0	1	0	1	1	R11	Cursor End Raster	Raster	×	O								
0	1	0	1	1	0	0	R12	Start Address(H)	–	O	O								
0	1	0	1	1	0	1	R13	Start Address(L)	–	O	O								
0	1	0	1	1	1	0	R14	Cursor(H)	–	O	O								
0	1	0	1	1	1	1	R15	Cursor (L)	–	O	O								
0	1	1	0	0	0	0	R16	Light Pen(H)	–	O	×								
0	1	1	0	0	0	1	R17	Light Pen(L)	–	O	×								

[NOTE] 1. The Registers marked *: (Written Value) = (Specified Value) – 1
2. Written Value of R9 is mentioned below.
1) Non-interlace Mode / Interlace Sync Mode: (Written Value Nr) = (Specified Value) – 1
2) Interlace Sync & Video Mode: (Written Value Nr) = (Specified Value) – 2
3. C0 and C1 specify skew of CUDISP output signal.
D0 and D1 specify skew of DISPTMG output signal.
When S is "1", V specifies video mode. S specifies the Interlace Sync Mode.
4. B specifies the cursor blink. P specifies the cursor blink period.
5. wv0~wv3 specify the pulse width of Vertical Sync Signal.
wh0~wh3 specify the pulse width of Horizontal Sync Signal.
6. R0 is ordinally programmed to be odd number in interlace mode.
7. O; Yes, ×; No

- **Address Register (AR)**

This is a 5-bit register used to select 18 internal control registers (R0~R17). Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to R0~R17 requires, first of all, to write the address of corresponding control register into this register. When RS and $\overline{CS}$ are at "Low" level, this register is selected.

- **Horizontal Total Register (R0)**

This is a register used to program total number of horizontal characters per line including the retrace period. The data is 8-bit and its value should be programmed according to the specification of the CRT. When M is total number of characters, (M-1) shall be programmed to this register. When programming for interlace mode, M must be even.

- **Horizontal Displayed Register (R1)**

This is a register used to program the number of horizontal displayed characters per line. Data is 8-bit and any number that is smaller than that of horizontal total characters can be programmed.

- **Horizontal Sync Position Register (R2)**

This is a register used to program horizontal sync position as multiples of the character clock period. Data is 8-bit and any number that is lower than the horizontal total number can be programmed. When H is character number of horizontal Sync Position, (H-1) shall be programmed to this register. When programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

- **Sync Width Register (R3)**

This is a register used to program the horizontal sync pulse width and the vertical sync pulse width. The horizontal sync pulse width is programmed in the lower 4-bit as multiples of the character clock period. "0" cannot be programmed. The vertical sync pulse width is programmed in higher 4-bit as multiples of the raster period. When "0" is programmed in higher 4-bit, 16 raster period (16H) is specified.

- **Vertical Total Register (R4)**

This is a register used to program total number of lines per frame including vertical retrace period. The data is within 7-bit and its value should be programmed according to the specification of the CRTC. When N is total number of lines, (N-1) shall be programmed to this register.

- **Vertical Total Adjust Register (R5)**

This is a register used to program the optimum number to adjust total number of rasters per field. This register enables to decide the number of vertical deflection frequency more strictly.

- **Vertical Displayed Register (R6)**

This is a register used to program the number of displayed character rows on the CRT screen. Data is 7-bit and any number that is smaller than that of vertical total characters can be programmed.

Table 2 Pulse Width of Vertical Sync Signal

VSW				Pulse Width
2^7	2^6	2^5	2^4	
0	0	0	0	16H
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

H; Raster period

Table 3 Pulse Width of Horizontal Sync Signal

HSW				Pulse Width
2^3	2^2	2^1	2^0	
0	0	0	0	– (Note)
0	0	0	1	1 CH
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

CH; Character clock period
(Note) HSW = "0" cannot be used.

• **Vertical Sync Position Register (R7)**

This is a register used to program the vertical sync position on the screen as multiples of the horizontal character line period. Data is 7-bit and any number that is equal to or less than vertical total characters can be programmed. When V is character number of vertical sync position, (V-1) shall be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

• **Interlace and Skew Register (R8)**

This is a register used to program raster scan mode and skew (delay) of CUDISP signal and DISPTMG signal.

Interlace Mode Program Bit (V, S)

Raster scan mode is programmed in the V, S bit.

Table 4 Interlace Mode (2^1, 2^0)

V	S	Raster Scan Mode
0	0	Non-interlace Mode
1	0	
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

In the non-interlace mode, the rasters of even number field and odd number field are scanned duplicatedly. In the interlace sync mode, the rasters of odd number field are scanned in the middle of even number field. Then it is controlled to display the same character pattern in two fields. In the interlace sync and video mode, the raster scan method is the same as the interlace sync mode, but it is controlled to display different character pattern in two field.

Skew Program Bit (C1, C0, D1, D0)

These are used to program the skew (delay) of CUDISP signal and DISPTMG signal.

Skew of these two kinds of signals are programmed separately.

Table 5 DISPTMG Skew Bit (2^7, 2^6)

D1	D0	DISPTMG Signal
0	0	Non-skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

Table 6 Cursor Skew Bit (2^5, 2^4)

C1	C0	Non-skew
0	0	Non-skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

Skew function is used to delay the output timing of CUDISP and DISPTMG signals in LSI for the time to access refresh memory, character generator or pattern generator, and to make the same phase with serial video signal.

• **Maximum Raster Address Register (R9)**

This is a register used to program maximum raster address within 5-bit. This register defines total number of rasters per character including space. This register is programmed as follows.

Non-interlace Mode, Interlace Sync Mode

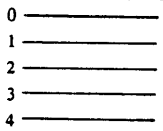
When total number of rasters is RN, (RN-1) shall be programmed.

Interlace Sync & Video Mode

When total number of rasters is RN, (RN-2) shall be programmed.

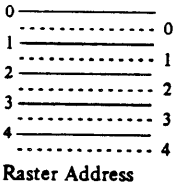
This manual defines total number of rasters in non-interlace mode, interlace sync mode and interlace sync & video mode as follows:

Non-interlace Mode



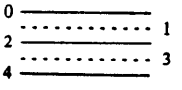
Total Number of Rasters 5
Programmed Value Nr = 4
(The same as displayed total number of rasters)

Interlace Sync Mode



Total Number of Rasters 5
Programmed Value Nr = 4
(In the interlace sync mode, total number of rasters in both the even and odd fields is ten. On programming, the half of it is defined as total number of rasters.)

Interlace Sync & Video Mode



Total Number of Rasters 5
Programmed Value Nr = 3
(Total number of rasters displayed in the even field and the odd field.)

• **Cursor Start Raster Register (R10)**

This is a register used to program the cursor start raster address by lower 5-bit (2^0~2^4) and the cursor display mode by higher 2-bit (2^5, 2^6).

Table 7 Cursor Display Mode (2^6, 2^5)

B	P	Cursor Display Mode
0	0	Non-blink
0	1	Cursor Non-display
1	0	Blink, 16 Field Period
1	1	Blink, 32 Field Period

Blink Period

- **Cursor End Raster Register (R11)**
  This is register used to program the cursor end raster address.

- **Start Address Register (R12, R13)**
  These are used to program the first address of refresh memory to read out.
  Paging and scrolling is easily performed using this register. This register can be read but the higher 2-bit (2^6, 2^7) of R12 are always "0".

- **Cursor Register (R14, R15)**
  These two read/write registers stores the cursor location. The higher 2-bit (2^6, 2^7) of R14 are always "0".

- **Light Pen Register (R16, R17)**
  These read only registers are used to catch the detection address of the light pen. The higher 2-bit (2^6, 2^7) of R16 are always "0". Its value needs to be corrected by software because there is time delay from address output of the CRTC to signal input LPSTB pin of the CRTC in the process that raster is lit after address output and light pen detects it. Moreover, delay time shown in Fig. 2 needs to be taken into account.

Restriction on Programming Internal Register

1) $0 < Nhd < Nht + 1 \leqq 256$
2) $0 < Nvd < Nvt + 1 \leqq 128$
3) $0 \leqq Nhsp \leqq Nht$
4) $0 \leqq Nvsp \leqq Nvt$*
5) $0 \leqq N_{CSTART} \leqq N_{CEND} \leqq Nr$ (Non-interlace, Interlace sync mode)
   $0 \leqq N_{CSTART} \leqq N_{CEND} \leqq Nr + 1$ (Interlace sync & video mode)
6) $2 \leqq Nr \leqq 30$
7) $3 \leqq Nht$ (Except non-interlace mode)
   $5 \leqq Nht$ (Non-interlace mode only)

* In the interlace mode, pulse width is changed ±½ raster time when vertical sync signal extends over two fields.

Notes for Use

The method of directly using the value programmed in the internal register of LSI for controlling the CRT is adopted. Consequently, the display may flicker on the screen when the contents of the registers are changed from bus side asyncronously with the display operation.

Cursor Register

Writing into this register at frequent intervals for moving the cursor should be performed during horizontal and vertical retrace period.

Start Address Register

Writing into the start address register at frequent intervals for scrolling and paging should be performed during horizontal and vertical display period.

It is desirable to avoid programming other registers during display operation.

■ OPERATION OF THE CRTC

- **Time Chart of CRT Interface Signals**
  The following example shows the display operation in which values of Table 8 are programmed to the CRTC internal registers. Fig. 6 shows the CRT screen format. Fig. 9 shows the time chart of signals output from the CRTC.

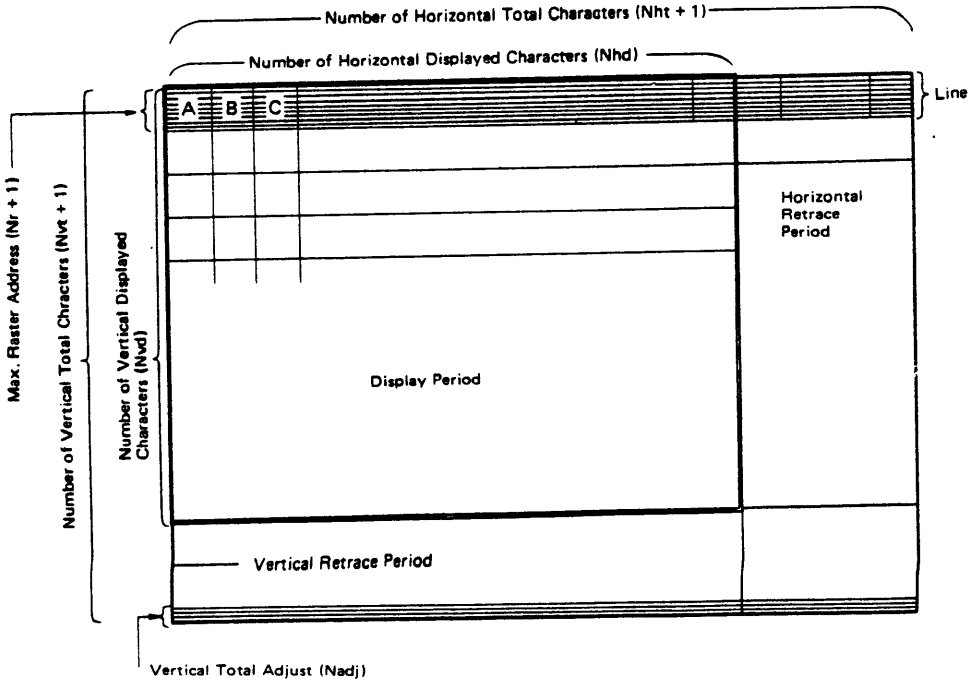


Figure 6 CRT screen Format

Table 8 Programmed Values into the Registers

Register	Register Name	Value	Register	Register Name	Value
R0	Horizontal Total	Nht	R9	Max. Raster Address	Nr
R1	Horizontal Displayed	Nhd	R10	Cursor Start Raster	
R2	Horizontal Sync Position	Nhsp	R11	Cursor End Raster	
R3	Sync Width	Nvsw, Nhsw	R12	Start Address (H)	0
R4	Vertical Total	Nvt	R13	Start Address (L)	0
R5	Vertical Total Adjust	Nadj	R14	Cursor (H)	
R6	Vertical Displayed	Nvd	R15	Cursor (L)	
R7	Vertical Sync Position	Nvsp	R16	Light Pen (H)	
R8	Interlace & Skew		R17	Light Pen (L)	

[NOTE] Nhd<Nht, Nvd<Nvt

The relation between values of Refresh Memory Address ($MA_0 \sim MA_{13}$) and Raster Address ($RA_0 \sim RA_4$) and the display position on the screen is shown in Fig. 15. Fig. 15 shows the case where the value of Start Address is 0.

- **Interlace Control**

Fig. 7 shows an example where the same character is displayed in the non-interlace mode, interlace sync mode, and video mode.

Non-interlace Mode Display

In non-interlace mode, each field is scanned duplicatedly. The values of raster addresses ($RA_0 \sim RA_4$) are counted up one from 0.

Interlace Sync Mode Display

In the interlace sync mode, raster addressed in the even field and the odd field are the same as addressed in the noninterlace mode. One character pattern is displayed mutually and its displayed position in the odd field is set at 1/2 raster space down from that in the even field.

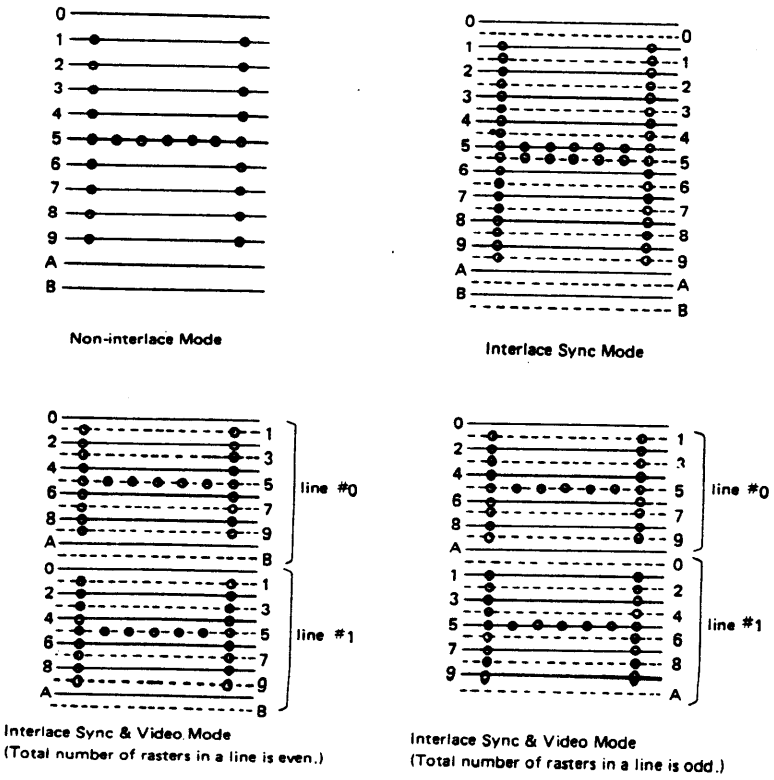


Figure 7 Example of Raster Scan Display

Interlace Sync & Video Mode Display

In interlace sync & video mode, the output raster address when the number of rasters is even is different from that when the number of rasters is odd.

Table 9 The Output of Raster Address in Interlace Sync & Video Mode

Total Number of Rasters in a Line \ Field		Even Field	Odd Field
Even		Even Address	Odd Address
Odd	Even Line*	Even Address	Odd Address
	Odd Line*	Odd Address	Even Address

* Internal line address begins from 0.

1) Total number of rasters in a line is even;

When number of rasters is programmed to be even, even raster address is output in the even field and odd raster address is output in the odd field.

2) Total number of rasters in a line is odd;

When total number of rasters is programmed to be odd, odd and even addresses are reversed according to the odd and even lines in each field. In this case, the difference in numbers of dots displayed between even field and odd field is usually smaller the case of 1). Then interlace can be displayed more stably.

[NOTE] The wide disparity of dots between number of dots between even field and odd field influences beam current of CRT. CRT, which has a stable high-voltage part, can make interlace display normal. On the contrary, CRT, which has unstable high-voltage part, moves deflection angle of beam current and also dots displayed in the even and odd fields may be shifted. Characters appears distroting on a border of the screen. So 2) programming has an effect to decrease such evil influences as mentioned above. Fig. 12 shows fine chart in each mode when interlace is performed.

- **Cursor Control**

Fig. 8 shows the display patterns where each value is programmed to the cursor start raster register and the cursor end raster register. Programmed values to the cursor start raster register and the cursor end raster register need to be under the following condition.

Cursor Start Raster Register ≦ Cursor End Raster Register ≦ Maximum Raster Address Register.

Time chart of CUDISP output signal is shown in Fig. 13 and Fig. 14.

■ INTERFACE TO DISPLAY CONTROL UNIT

Fig. 16 shows the interface between the CRTC and display control unit. Display control unit is mainly composed of Refresh Memory, Character Generator, and Video Control circuit. For refresh memory, 14 Memory Address line (0~16383) max are provided and for character generator, 5 Raster Address line (0~31) max are provided. For video control circuit, DISPTMG, CUDISP, HSYNC, and VSYNC signals are sent out. DISPTMG signal is used to control the blank period of video signal. CUDISP signal is used as video signal to display the cursor on the CRT screen. Moreover, HSYNC and VSYNC signals are used as drive signals respectively for CRT horizontal and vertical deflection circuits.

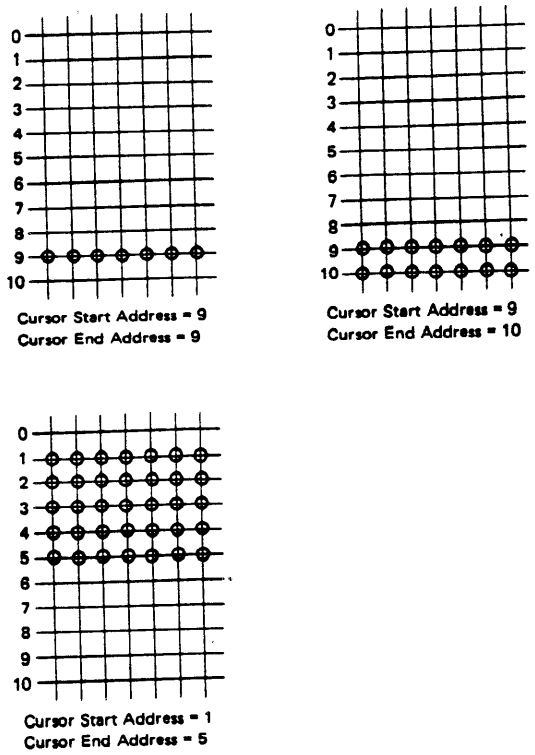


Figure 8 Cursor Control

Outputs from video control circuit, (video signals and sync signals) are provided to CRT display unit to control the deflection and brightness of CRT, thus characters are displayed on the screen.

Fig. 17 shows detailed block diagram of display control unit. This shows how to use CUDISP and DISPTMG signals. CUDISP and DISPTMG signals should be used being latched at least one time at external flip-flop F1 and F2. Flip-flop F1 and F2 function to make one-character delay time so as to synchronize them with video signal from parallel-serial converter. High-speed D type flip-flop as TTL is used for this purpose. After being delayed at F1 and F2 DISPTMG signal is AND-ed with character video signal, and CUDISP signal is OR-ed with output from AND gate. By using this circuitry, blanking of horizontal and vertical retrace time is controlled. And cursor video is mixed with character video signal.

Fig. 17 shows the example in the case that both refresh memory and CG can be accessed for horizontal one character time. Time chart for this case is shown in Fig. 20. This method is used when a few character needed to be displayed in horizontal direction on the screen.

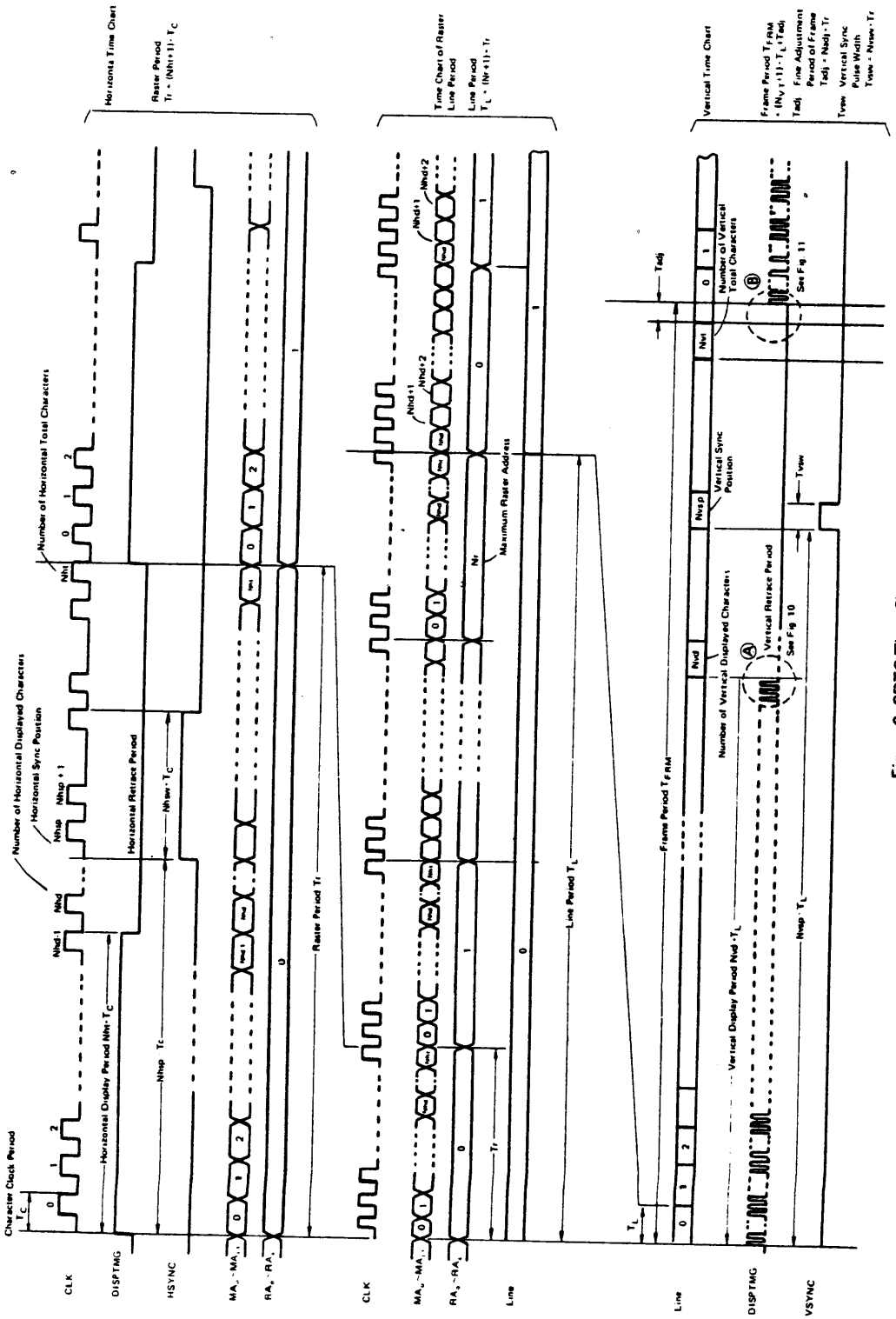


Figure 9 CRTC Time Chart

(Output waveform of horizontal & vertical display in the case where values shown in Table 8 are Programmed to each register.)

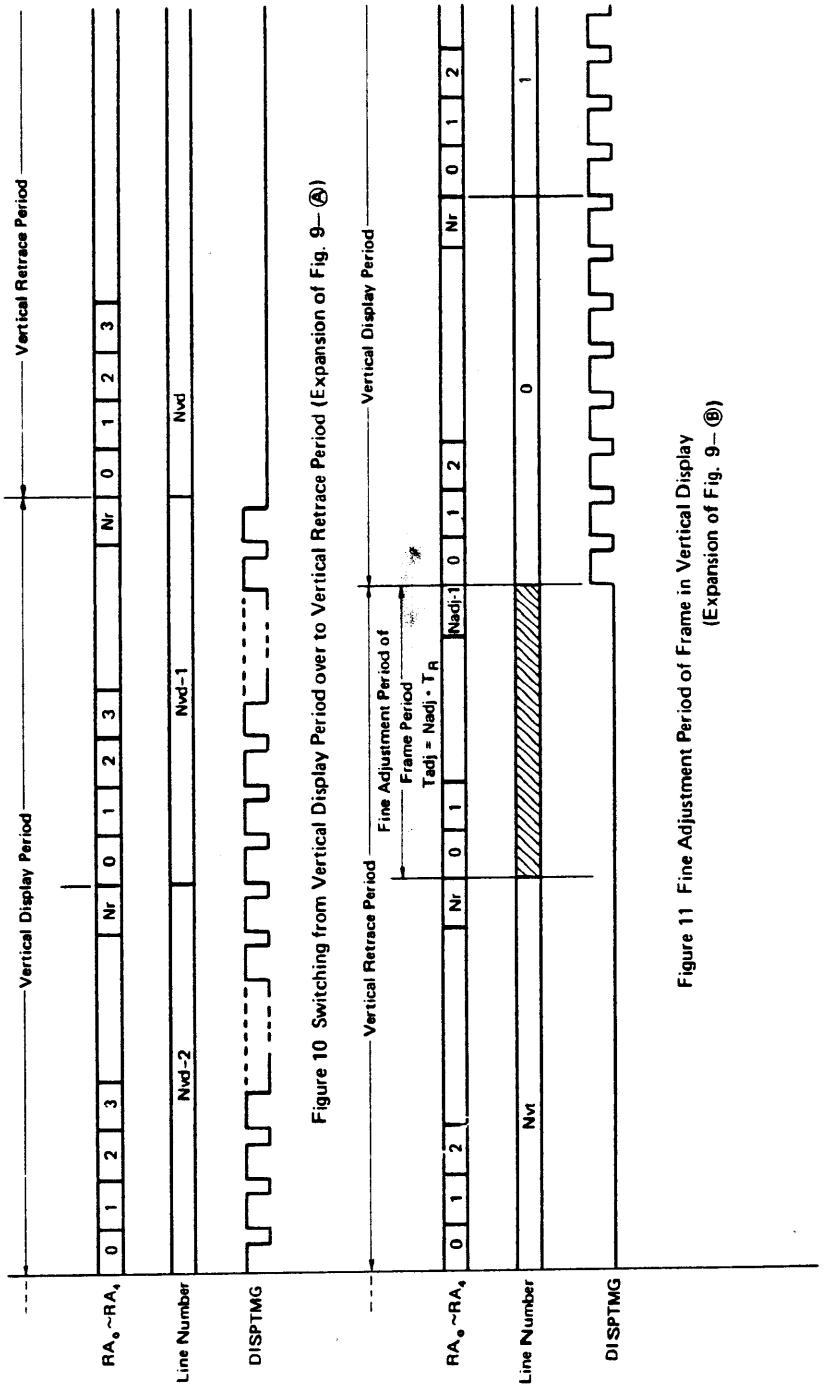


Figure 10 Switching from Vertical Display Period over to Vertical Retrace Period (Expansion of Fig. 9–Ⓐ)

Figure 11 Fine Adjustment Period of Frame in Vertical Display (Expansion of Fig. 9–Ⓑ)

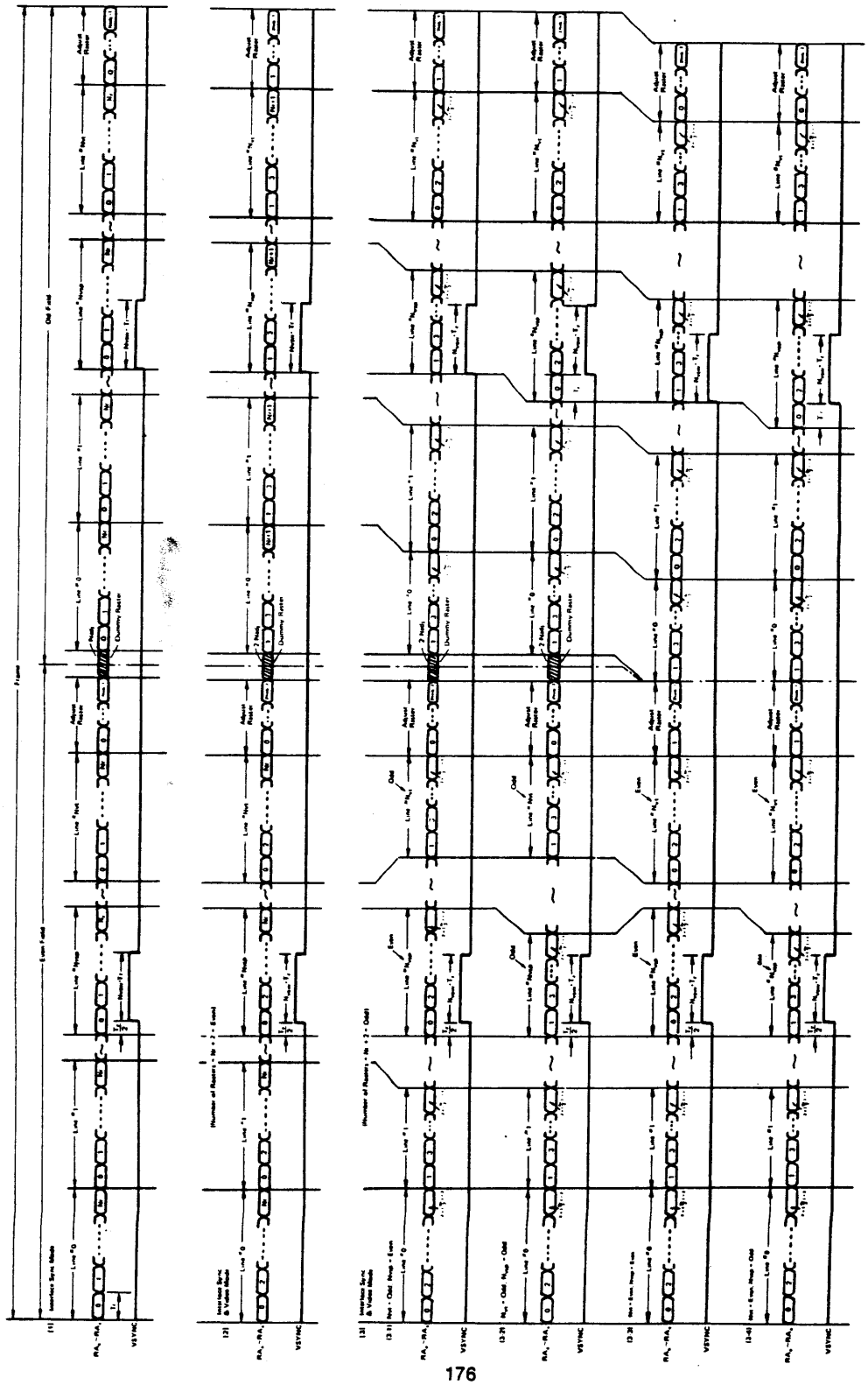


Figure 12 Interlace Control

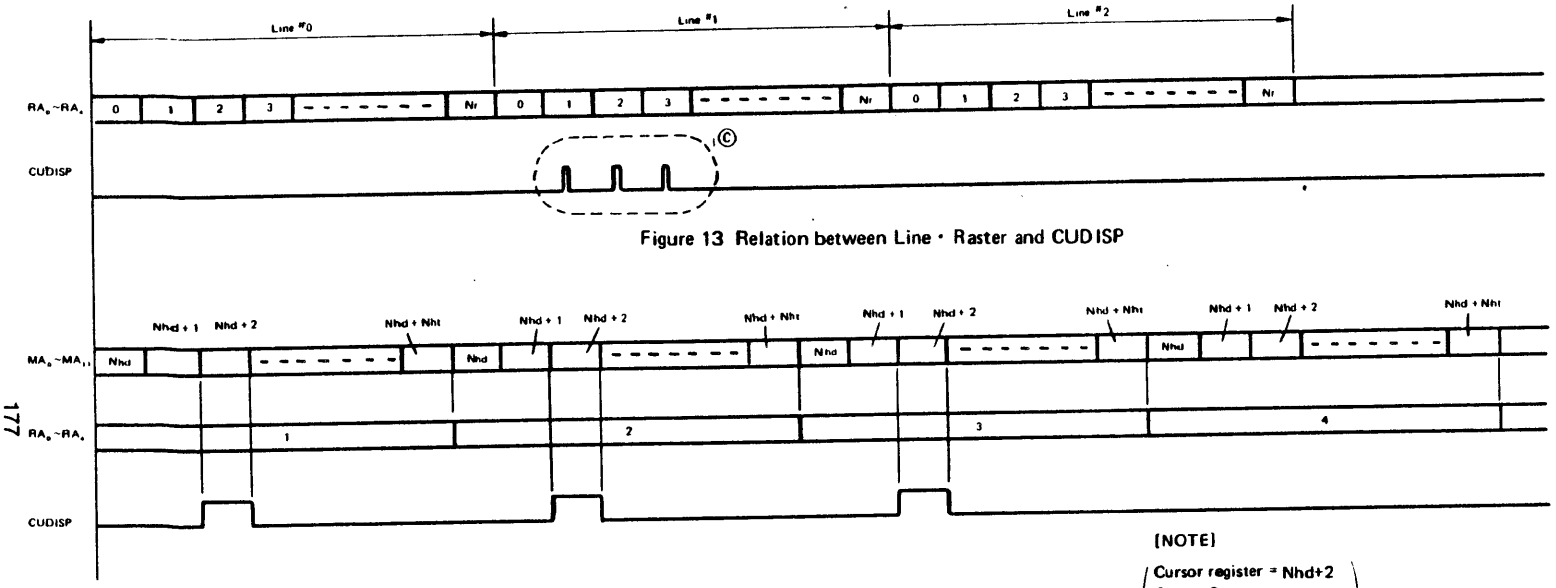


Figure 13 Relation between Line · Raster and CUDISP

(NOTE)

(Cursor register = Nhd+2
Cursor Start
Raster Register = 1
Cursor End
Raster Register = 3
are Programmed in cursor display mode.

In blink mode, it is changed into display or non-display mode when field period is 16 or 32-time period.

Figure 14 CUDISP Output Timing (Exapnsion of Fig. 13-©)

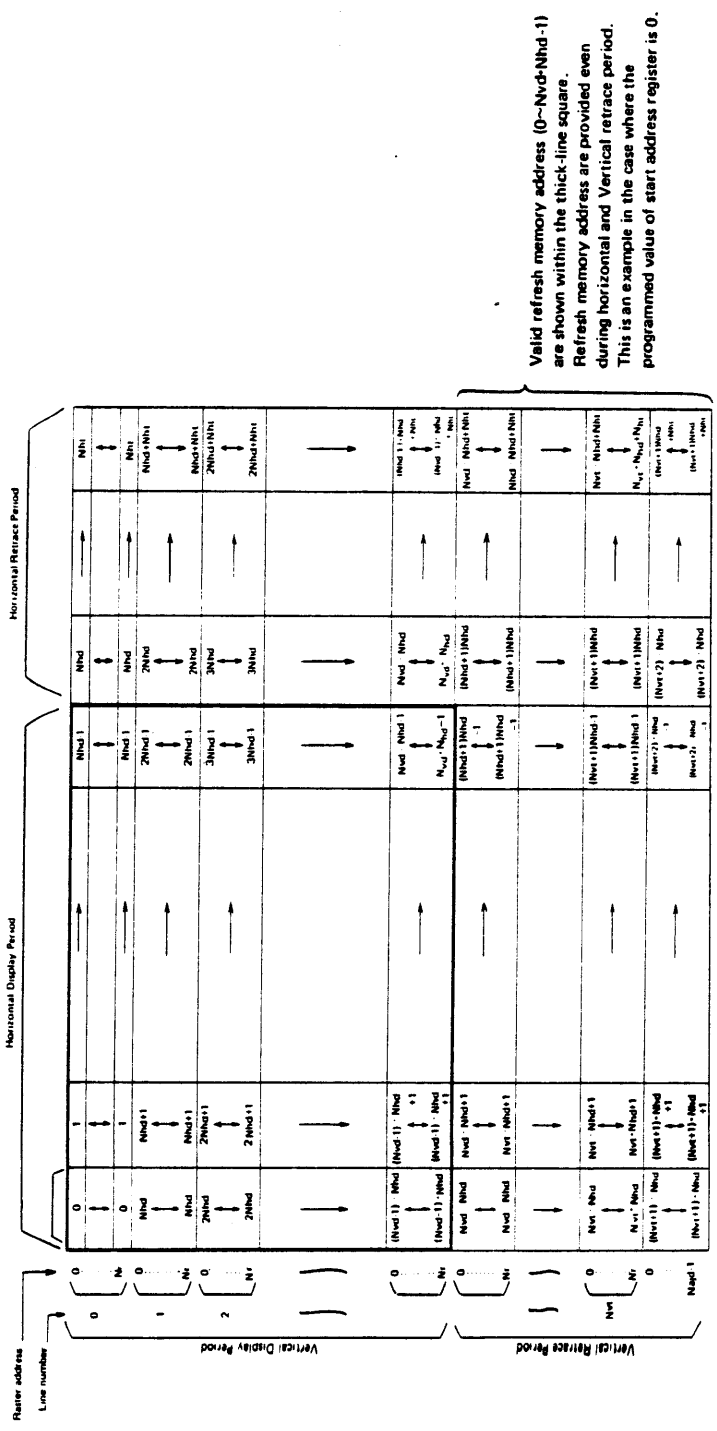


Figure 15 Refresh Memory Address (MA_0~MA_{13})

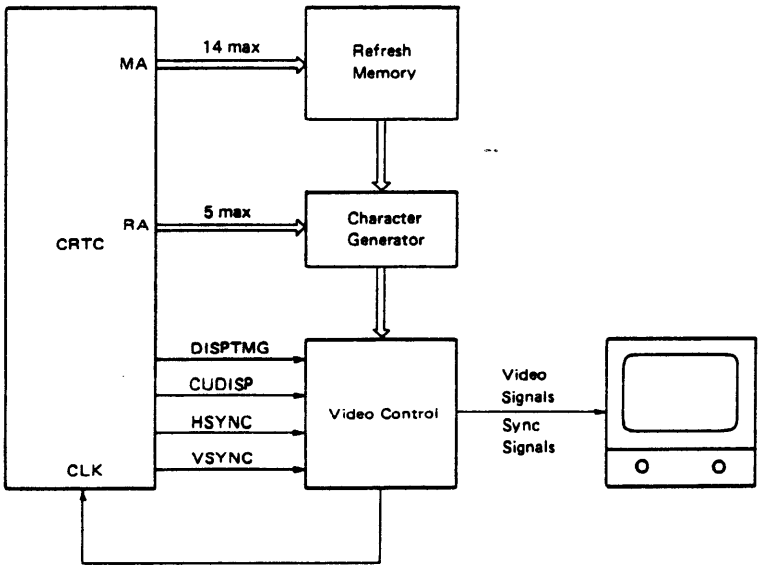


Figure 16 Interface to Display Control Unit

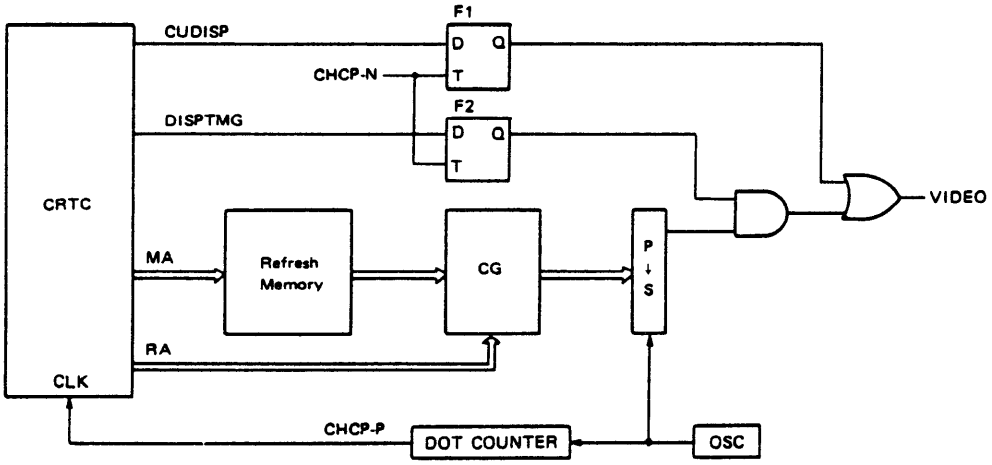


Figure 17 Display Control Unit (1)

When many characters are displayed in horizontal direction on the screen, and horizontal one-character time is so short that both refresh memory and CG cannot be accessed, the circuitry shown in Fig. 18 should be used. In this case refresh memory output shall be latched and CG shall be accessed at the next cycle. The time chart in this case is shown in Fig. 21. CUDISP and DISPTMG signals should be provided after being delayed by one-character time by using skew bit of interlace & skew register (R8). Moreover, when there are some troubles about delay time of MA during horizontal one-character time on high-speed display operation, system shown in Fig.19 is adopted. The time chart in this case is shown in Fig.22. Character video signal is delayed for two-character time because each MA outputs and refresh memory outputs are latched, and they are made to be in phase with CUDISP and DISPTMG signals by delaying for two-character time. Table 10 shows the circuitry selection standard of display units.

Table 10 Circuitry Standard of Display Control Unit

Case	Relation among t_{CH}, RM and CG	Block Diagram	Interlace & Skew Register Bit Programming			
			C1	C0	D1	D0
1	t_{CH} > RM Access + CG Access + t_{MAD}	Fig. 17	0	0	0	0
2	RM Access + CG Access + $t_{MAD} \geqq t_{CH}$ > RM Access + t_{MAD}	Fig. 18	0	1	0	1
3	RM Access + $t_{MAD} \geqq t_{CH}$ > RM Access	Fig. 19	1	0	1	0

t_{CH} : CHCP Period; t_{MAD} : MA Delay

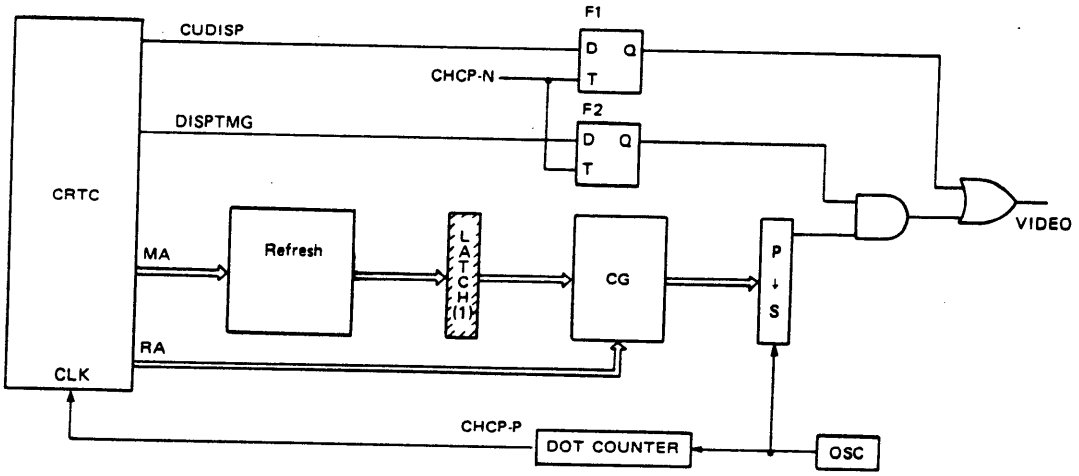


Figure 18 Display Control Unit (2)

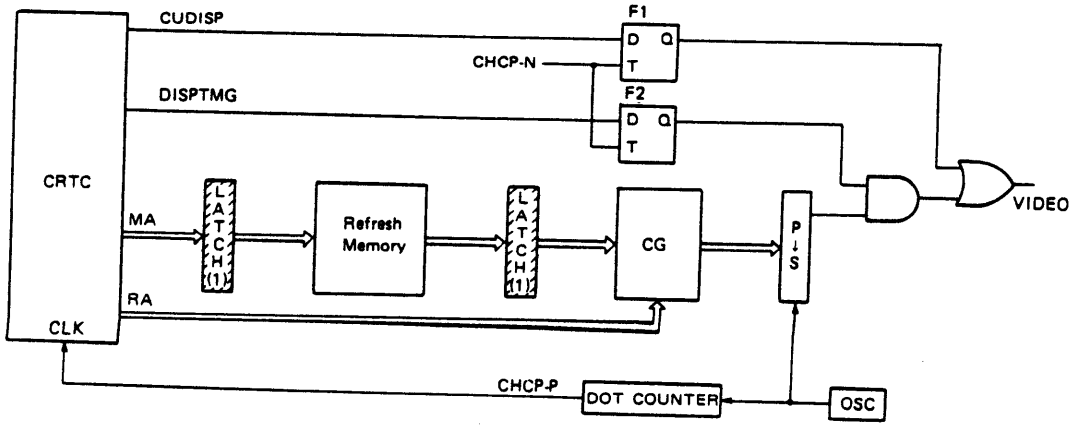


Figure 19 Display Control Unit (For high-speed display operation) (3)

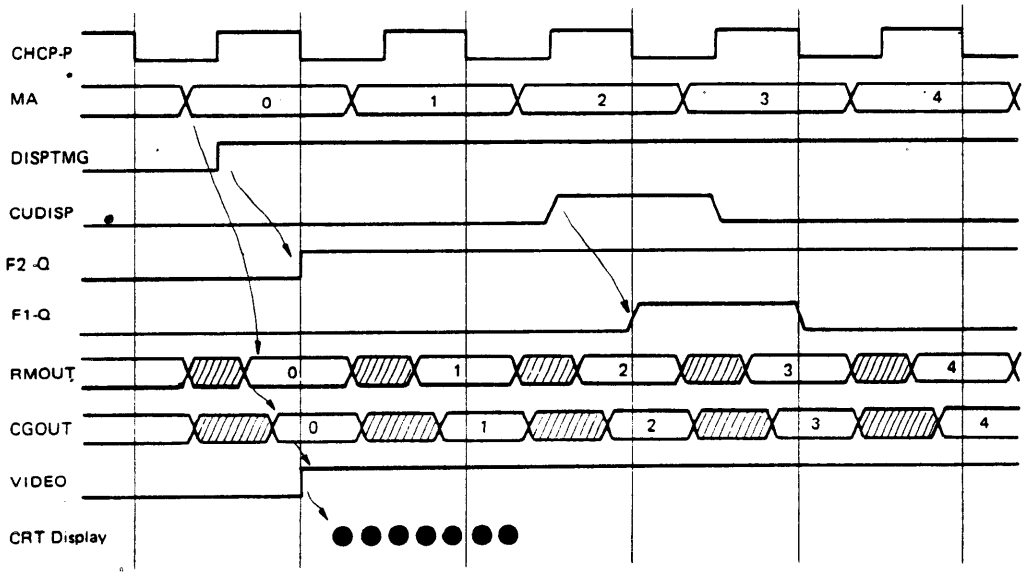


Figure 20 Time Chart of Display Control Unit (1)

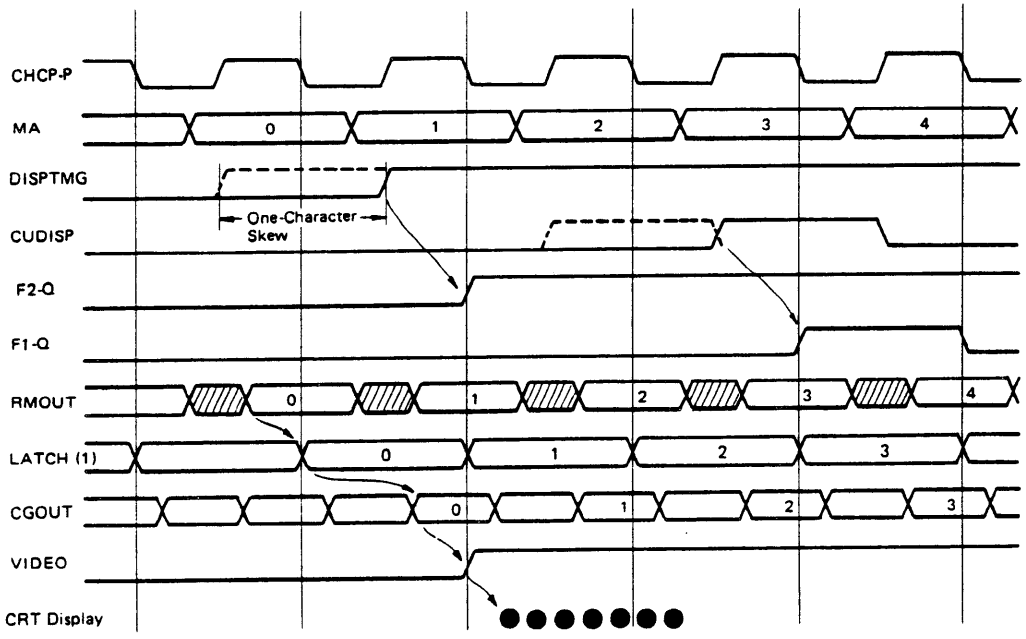


Figure 21 Time Chart of Display Control Unit (2)

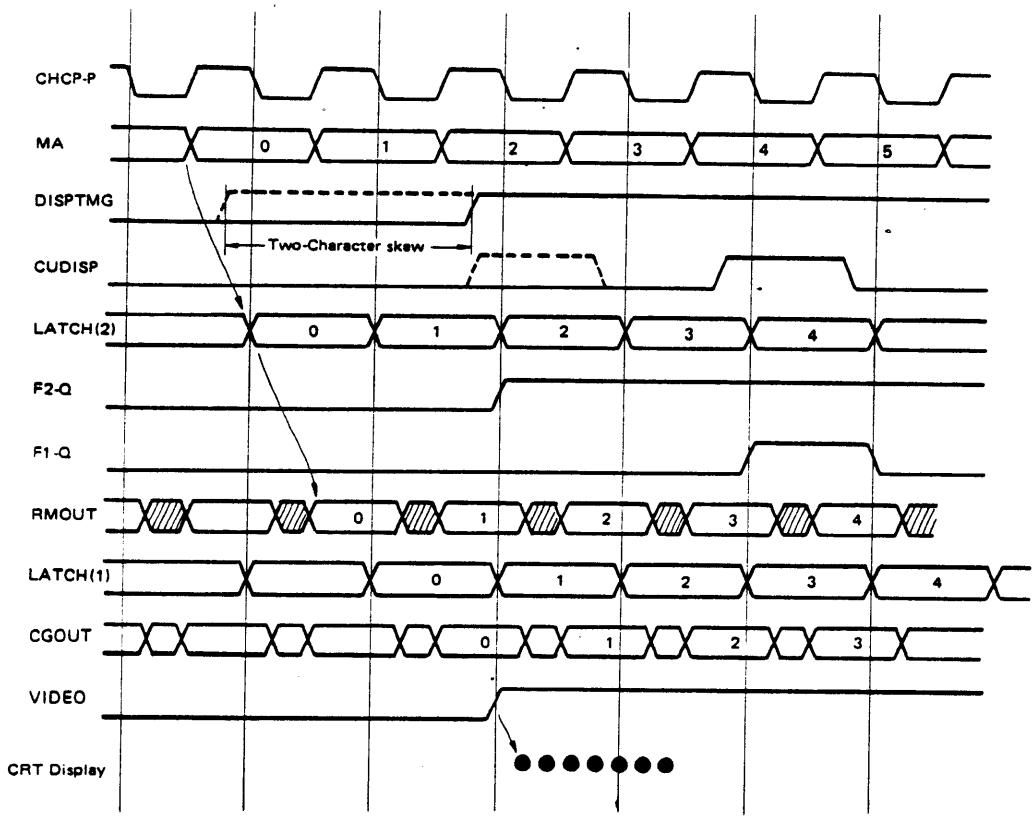


Figure 23 Time Chart of Display Unit (3)

■ HOW TO DECIDE PARAMETERS SET ON THE CRTC

• How to Decide Parameters Based on Specification of CRT Display Unit (Monitor)

Number of Horizontal Total Characters

Horizontal deflection frequency fh is given by specification of CRT display unit. Number of horizontal total characters is determined by the following equation.

$$fh = \frac{1}{t_C\,(Nht + 1)}$$

where,

t_C : Cycle Time of CLK (Character Clock)
Nht : Programmed Value of Horizontal Total Register (R0)

Number of Vertical Total Characters

Vertical deflection frequency is given by specification of CRT display unit. Number of vertical Total characters is determined by the following equation.

1) Non-interlace Mode
$Rt = (Nvt + 1)(Nr + 1) + Nadj$
2) Interlace Sync Mode
$Rt = (Nvt + 1)(Nr + 1) + Nadj + 0.5$
3) Interlace Sync & Video Mode

$$Rt = \frac{(Nvt + 1)(Nr + 2) + 2Nadj}{2} \quad \cdots\cdots\cdots\cdots \text{(a)}$$

$$Rt = \frac{(Nvt + 1)(Nr + 2) + 2Nadj + 1}{2} \quad \cdots\cdots\cdots\cdots \text{(b)}$$

(a) is applied when both total numbers of vertical characters (Nvt + 1) and that of rasters in a line (Nr + 2) are odd.
(b) is applied when total number of rasters (Nr + 2) is even, or when (Nr + 2) is odd and total number of vertical characters (Nvt + 1) is even.

where,

Rt : Number of Total Rasters per frame (Including retrace period)
Nvt : Programmed Value of Vertical Total Register (R4)
Nr : Programmed Value of Maximum Raster Address Register (R9)
Nadj : Programmed Value of Vertical Total Adjust Register (R5)

Horizontal Sync Pulse Width

Horizontal sync pulse width is programmed to low order 4-bit of horizontal sync width register (R3) in unit of horizontal character time. Programmed value can be selected within from 1 to 15.

Horizontal Sync Position

As shown in Fig. 24, horizontal sync position is normally selected to be in the middle of horizontal blank period. But there are some cases where its optimum sync position is not located in the middle of horizontal blank period according to specification of CRT. Therefore, horizontal sync position should be determined by specification of CRT. Horizontal sync pulse position is programmed in unit of horizontal character time.

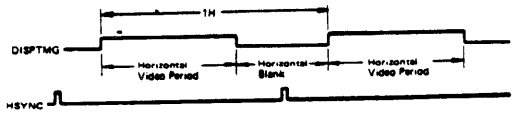


Figure 24 Time Chart of HSYNC

Vertical Sync Pulse Width

Vertical Sync Pulse Width is programmed to high order 4-bit of vertical sync pulse width register (R3) in unit of raster period. Programmed value can be selected within from 1 to 16.

Vertical Sync Position

As shown in Fig. 25, vertical sync position is normally selected to be in the middle of vertical blank period. But there are some cases where its optimum sync position is not located in the middle of vertical blank period according to specification of CRT. Therefore, vertical sync position should be determined by specification of CRT. Vertical sync pulse position is programmed to vertical sync position register (R7) in unit of line period.

- **How to Decide Parameters Based on Screen Format**

Dot Number of Characters (Horizontal)

Dot number of characters (horizontal) is determined by character font and character space. An example is shown in Fig. 26. More strictly, dot number of characters (horizontal) N is determined by external N-counter. Character space is set by means shown in Fig. 27.

Dot Number of Characters (Vertical)

Dot number of characters (vertical) is determined by characters font and line space. An example is shown in Fig. 26. Dot number of characters (vertical) is programmed to maximum raster address (register R9) of CRTC. When Nr is programmed

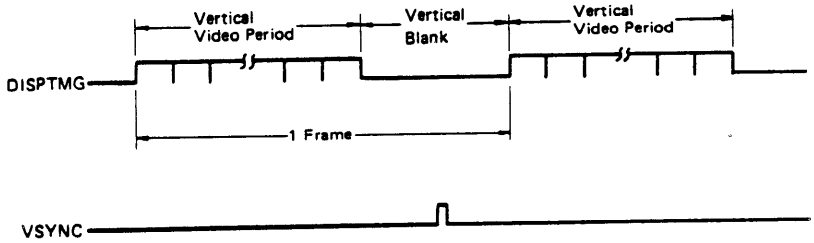


Figure 25 Time Chart of VSYNC

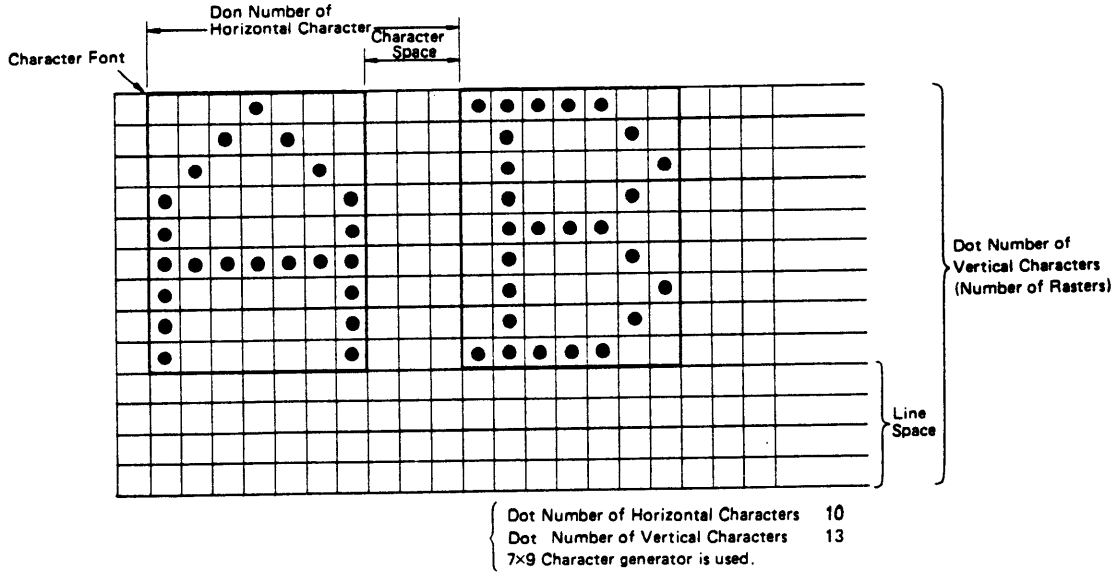


Figure 26 Dot Number of Horizontal and Vertical Characters

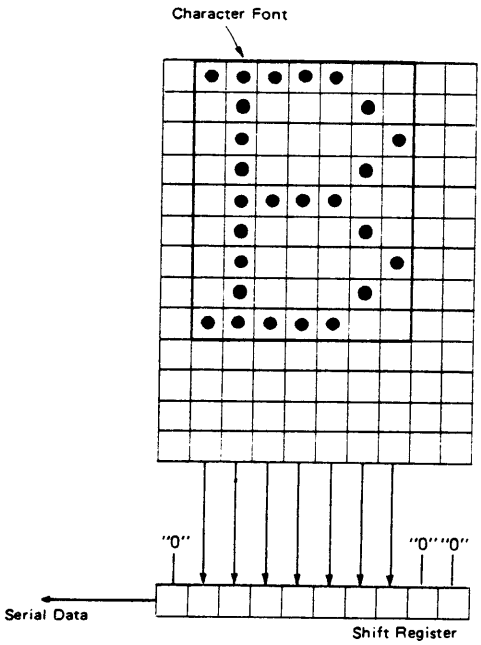


Figure 27 How to Make Character Space

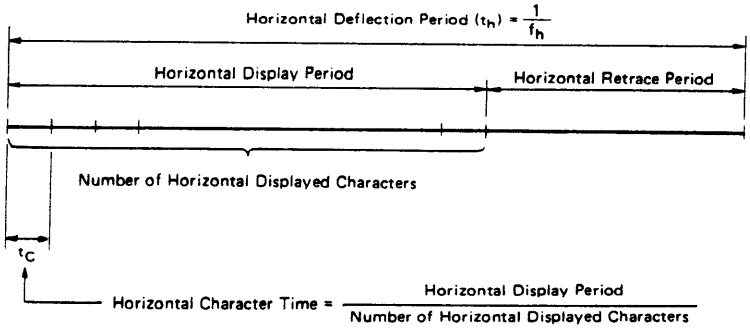


Figure 28 Number of Horizontal Displayed Characters

value of R9, dot number of characters (vertical) is (Nr+1).

Number of Horizontal Displayed Characters

Number of horizontal displayed characters is programmed to horizontal displayed register (R1) of the CRTC. Programmed value is based on screen format. Horizontal display period, which is given by specification of horizontal deflection frequency and horizontal retrace period of CRT display unit, determines horizontal character time, being divided by number of horizontal displayed characters. Moreover, its cycle time and access time which are necessary for CRT display system are determined by horizontal character time.

Number of Vertical Displayed Characters

Number of vertical displayed characters is programmed to vertical displayed register (R6). Programmed value is based on screen format. As specification of vertical deflection frequency of CRT determines number of total rasters (Rt) including vertical retrace period and the relation between number of vertical displayed character and total number of rasters on a screen is as mentioned above, CRT which is suitable for desired screen format should be selected.

For optimum screen format, it is necessary to adjust number of rasters per line, number of vertical displayed characters, and total adjust raster (Nadj) within specification of vertical deflection frequency.

Scan Mode

The CRTC can program three-scan modes shown in Table 11 to interlace mode register (R8). An example of character display in each scan mode is shown in Fig. 7.

Table 11 Program of Scan Mode

2^1	2^0	Scan Mode	Main Usage
0	0	Non-interlace	Normal Display of Characters & Figures
1	0		
0	1	Interlace Sync	Fine Display of Characters & Figures
1	1	Interlace Sync & Video	Display of Many Characters & Figures Without Using High-resolution CRT

[NOTE] In the interlace mode, the number of times per sec. in raster scanning on one spot on the screen is half as many as that in non-interlace mode. Therefore, when persistence of luminescence is short, flickering may happen. It is necessary to select optimum scan mode for the system, taking characteristics of CRT, raster scan speed, and number of displayed characters and figures into account.

Cursor Display Method

Cursor start raster register and cursor end raster register (R10, R11) enable programming the display modes shown in Table 7 and display patterns shown in Fig. 8. Therefore, it is possible to change the method of cursor display dynamically according to the system conditions as well as to realize the cursor display that meets the system requirements.

Start Address

Start address resisters (R12, R13) give an offset to the address of refresh memory to read out. This enables paging and scrolling easily.

Cursor Register

Cursor registers (R14, R15) enable programming the cursor display position on the screen. As for cursor address, it is not X, Y address but linear address that is programmed.

■ EXAMPLES OF APPLIED CIRCUIT OF THE CRTC

Fig. 30 shows an example of application of the CRTC to monochrome character display. Its specification is shown in Table 12. Moreover, specification of CRT display unit is shown in Table 13 and initializing values for the CRTC are shown in Table 14.

Table 12 Specification of Applied Circuit

Item	Specification															
Character Format	5 × 7 Dot															
Character Space	Horizontal : 3 Dot Vertical : 5 Dot															
One Character Time	1 μs															
Number of Displayed Characters	40 characters × 16 lines = 640 characters															
Access Method to Refresh Memory	Snychronous Method (DISPTMG Read)															
Refresh Memory	1 kB															
Address Map		2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	Refresh Memory	0	0	0	0	0	0	*	*	*	*	*	*	*	*	*	*
	CRTC Address Register	0	0	0	1	0	0	×	×	×	×	×	×	×	×	×	0
	CRTC Control Register	0	0	0	1	0	0	×	×	×	×	×	×	×	×	×	1
	× ... don't care, * ... 0 or 1																
Synchronization Method	HVSYNC Method															

Table 13 Specification of Character Display

Item	Specification
Scan Mode	Non-interlace
Horizontal Deflection Frequency	15.625 kHz
Vertical Deflection Frequency	60.1 Hz
Dot Frequency	8 MHz
Character Dot (Horizontal × Vertical)	8 × 12 (Character Font 5 × 9)
Number of Displayed Characters (Row x Line)	40 × 16
HSYNC Width	4 μs
VSYNC Width	3 H
Cursor Display	Raster 9 ~ 10, Blink 16 Field Period
Paging, Scrolling	Not used

Table 14 Initializing Values for Character Display

Register	Name	Symbol	Initializing Value Hex (Decimal)
R0	Horizontal Total	Nht	3F (63)
R1	Horizontal Displayed	Nhd	28 (40)
R2	Horizontal Sync Position	Nhsp	34 (52)
R3	Sync Width	Nvsw, Nhsw	34
R4	Vertical Total	Nvt	14 (20)
R5	Vertical Total Adjust	Nadj	08 (8)
R6	Vertical Displayed	Nvd	10 (16)
R7	Vertical Sync Position	Nvsp	13 (19)
R8	Interlace & Skew		00
R9	Maximum Raster Address	Nr	0B (11)
R10	Cursor Start Raster	B, P, NCSTART	49
R11	Cursor End Raster	NCEND	0A (10)
R12	Start Address (H)		00 (0)
R13	Start Address (L)		00 (0)
R14	Cursor (H)		00 (0)
R15	Cursor (L)		00 (0)

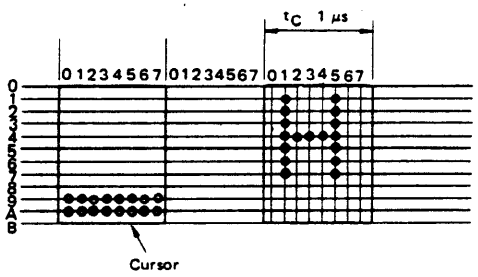
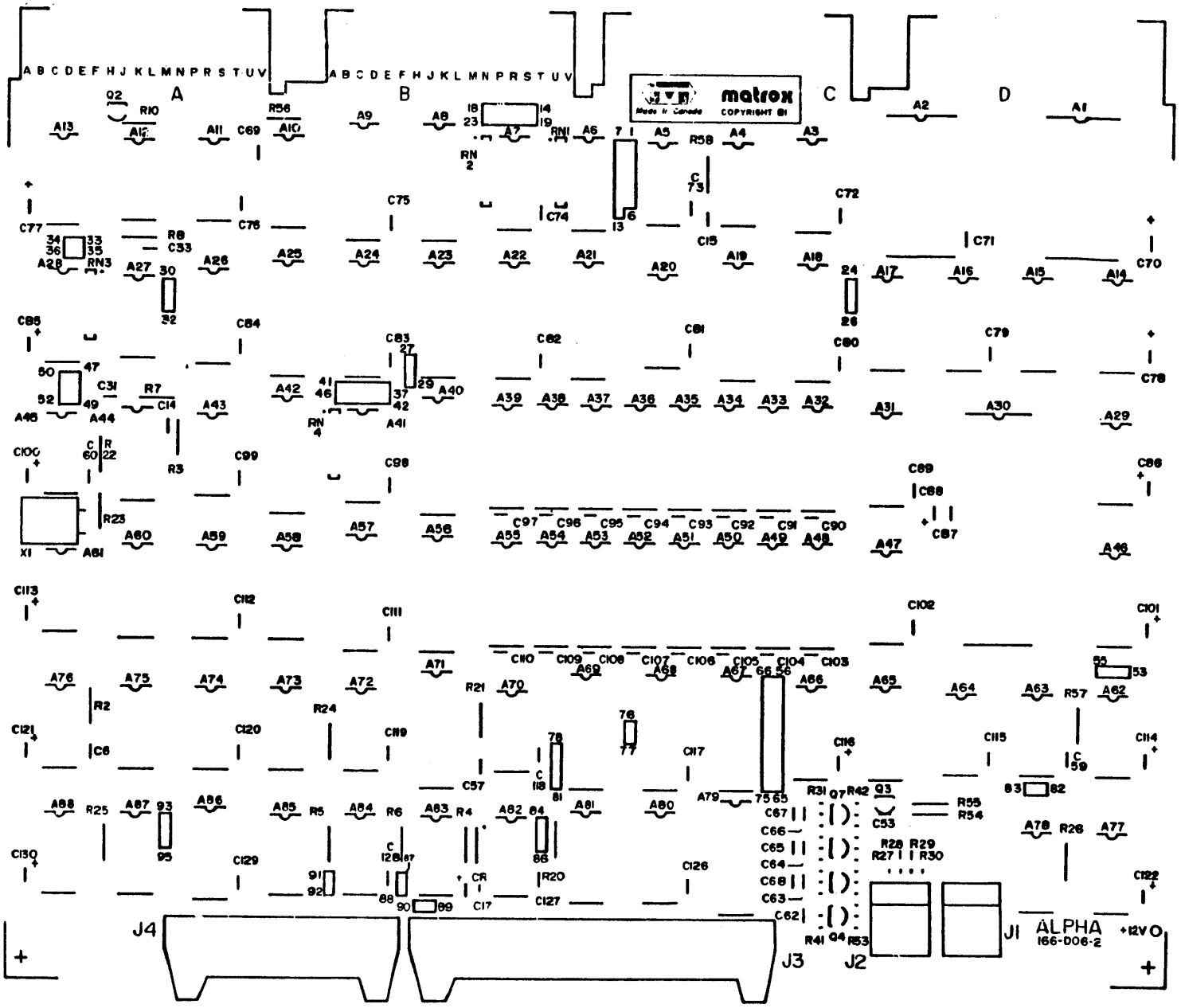
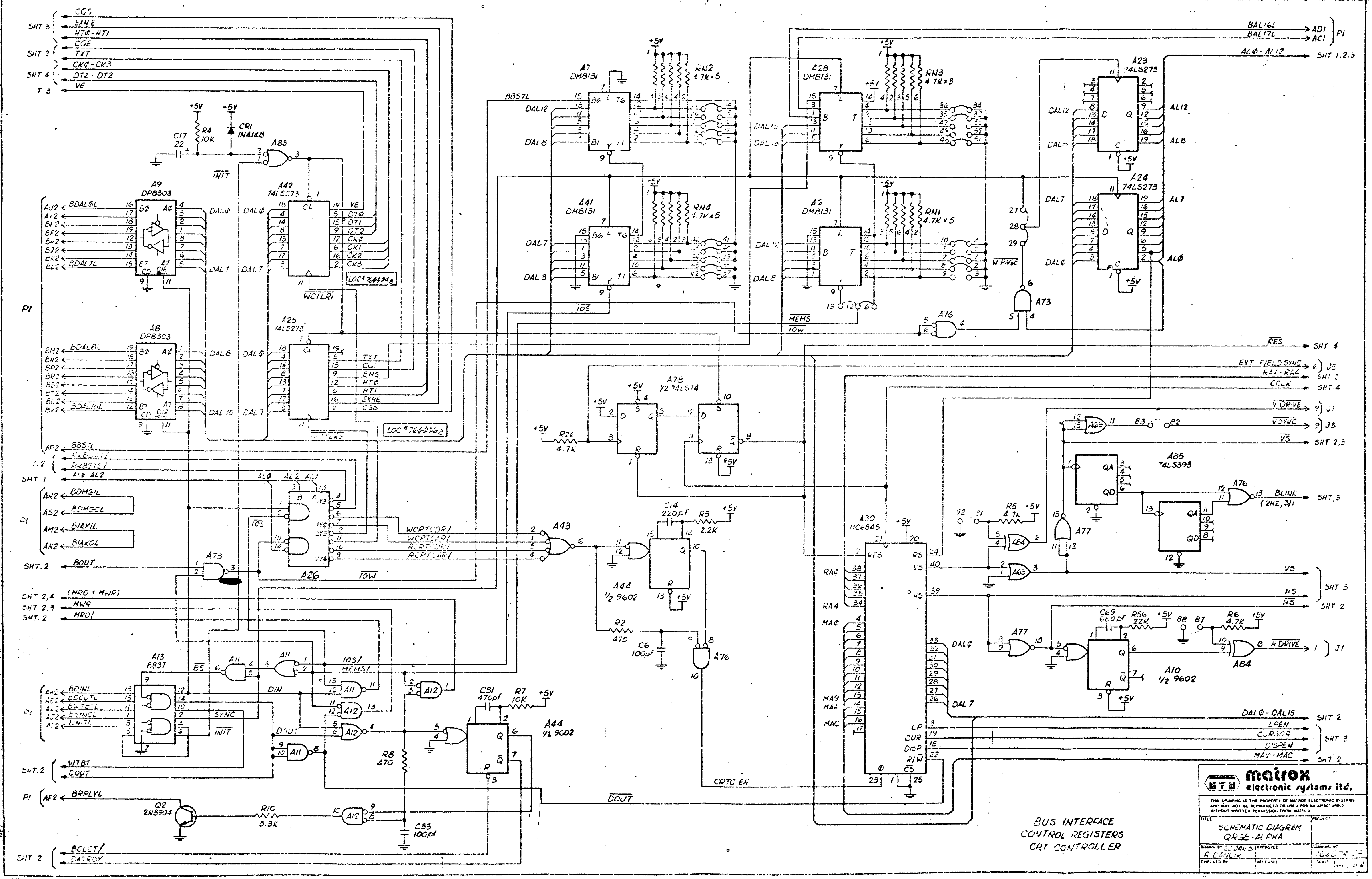
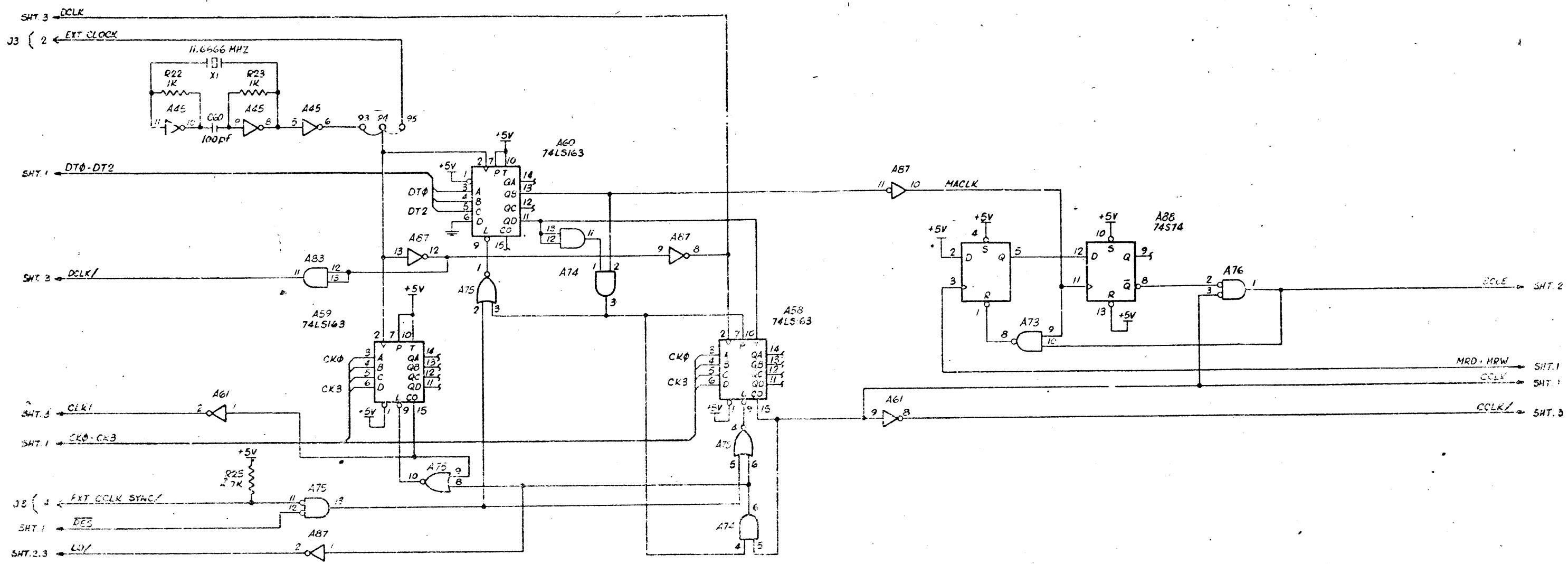


Figure 29 Non-interlace Display (Example)

DRAWINGS


matrox
COPYRIGHT 81
Made in Canada
J4
J3
J2
J1
ALPHA
166-006-2
+12VO


BUS INTERFACE
CONTROL REGISTERS
CRT CONTROLLER
matrox electronic systems ltd.
SCHEMATIC DIAGRAM
QRGB-ALPHA
A9 DP8303
A8 DP8303
A42 74LS273
A25 74LS273
A7 DM8131
A41 DM8131
A28 DM8131
A6 DM8131
A23 74LS273
A24 74LS273
A13 6837
A26
A43
A44 1/2 9602
A78 1/2 74LS74
A30 MC6845
A85 74LS393
A10 1/2 9602
Q2 2N3904
RN1 4.7K x 5
RN2 4.7K x 5
RN3 4.7K x 5
RN4 4.7K x 5



PARTS #	IC REFERENCE	OPTION	+5V	GND
74LS00	A4 [illegible] -2		14	7
74LS02	A12 [illegible] 76,77		14	7
74LS04	A5,46 [illegible] 67		14	7
74LS08	A4-9 [illegible] 74,83		14	7
74S10	A40		14	7
74LS21	A20,43		14	7
74S02	A76		14	7
74LS32	A43		14	7
74LS74	A64 [illegible] 72,77-88		14	7
74LS86	A44		14	7
74S08	A27		14	7
74S153	A[illegible]7		16	8
74LS155	A26,66		16	8
74S157	A14-17,31,47		16	8
74LS157	A80,81		16	8
74LS163	A58,59,60		16	8
74LS166	A3		16	8
74LS244	A26,51		20	10
74LS245	A18,40		20	10
74LS273	A[illegible] 23-25,42 [illegible]		20	10
74LS368	A5[illegible]		16	8
74LS374	A32,57,71		20	10
74LS393	A58		14	7
74S571	A46		16	5
MC1401	A42		24	12
2114LC150	A32,39,48-55		18	9
HD46505SP1	A30		20	1
DP8304	A[illegible]9		20	10
DM8131	A6,7,26,41		16	8
DP8437	A13		16	5
9602	A10,44		16	5

PARTS #	IC REFERENCE	SPARES
74LS02	A76	1
74LS04	A67	3
74LS[illegible]	A75	1
74LS[illegible]	A63	1
74LS[illegible]	A86	1
[illegible]	A10	1
9602	A44	1

NOTE :

1. UNLESS OTHERWISE SPECIFIED:
   - ALL RESISTORS ARE IN OHMS, 1/4 W, 10%.
   - ALL CAPACITORS ARE MICROFARAD.

PROGRAMMABLE TIMING

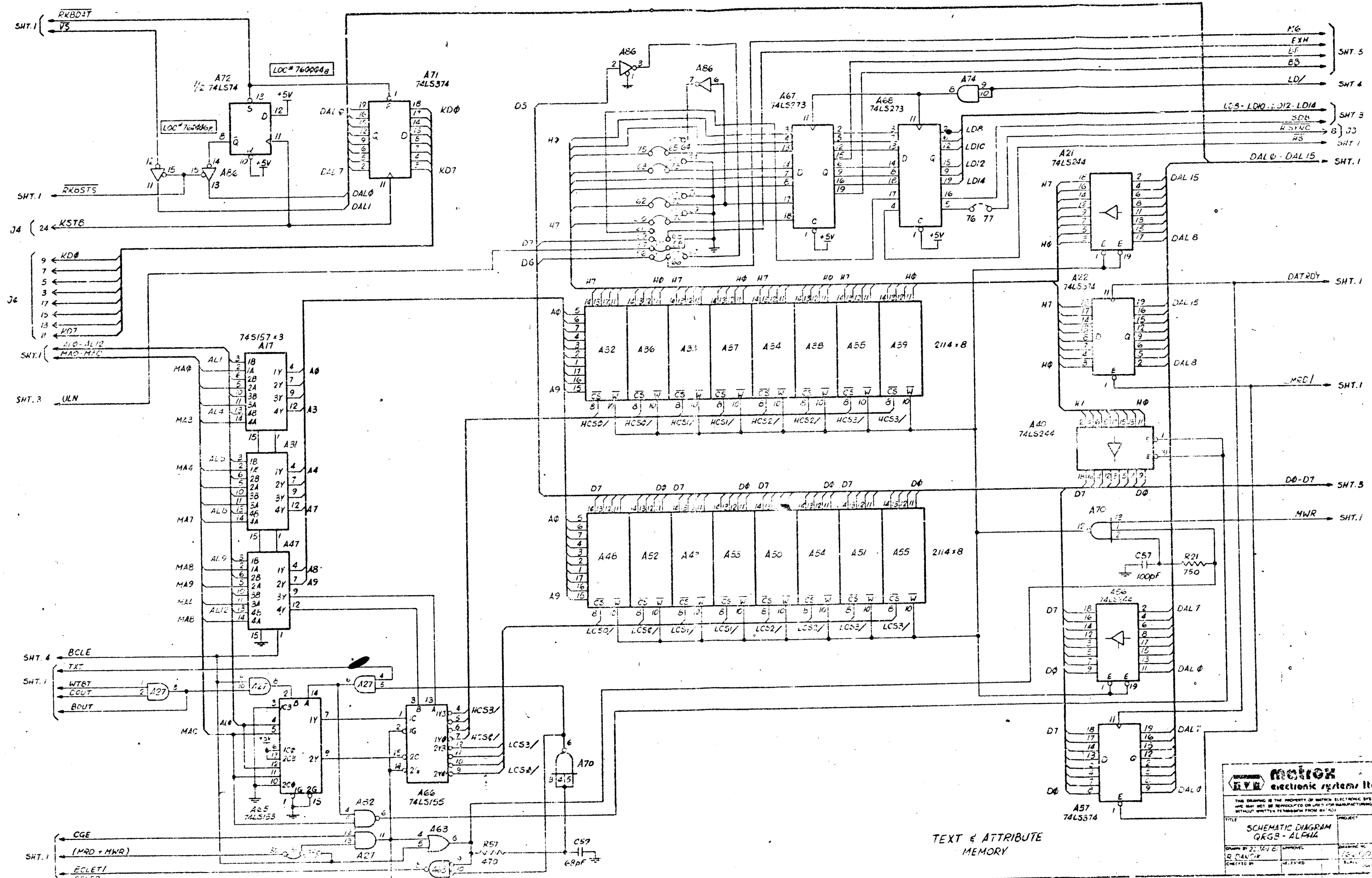
RVD metron electronic systems ltd.

TITLE: SCHEMATIC DIAGRAM GRGB - ALPHA

PROJECT:

DRAWN BY: [illegible] DATE: [illegible]

CHECKED BY: RELEASE: [illegible]


RKBDAT
VS
SHT. 1
A72
1/2 74LS74
LOC# 760004 8
LOC# 760436 P
A71
74LS374
DAL Ø
DAL 7
KDØ
KD7
+5V
A86
RKBSTS
SHT. 1
DALØ
DAL1
J4
24 KSTB
KDØ
KD7
J6
AIØ - AL12
MAØ - MA12
SHT. 1
745157 x 3
A17
MAØ
MA3
MA4
MA7
MA8
MA9
MAL
MAB
AØ
A3
A4
A7
A8
A9
A31
A47
SHT. 3 ULN
SHT. 4 BCLE
TXT
SHT. 1 WTBT
COUT
BOUT
MAC
A27
A21
A85
74LS155
A66
74LS155
HCSØ/
HCS1/
HCS2/
HCS3/
LCSØ/
LCS1/
LCS2/
LCS3/
A70
A62
A63
CGE
SHT. 1 (MRD + MWR)
ECLET1
SHT. 3 ECLEØ
R57
470
C57
68pF
D5
D6
D7
H7
H6
A67
74LS273
A68
74LS273
A74
LDA
LDIC
LDI2
LDI4
76 77
+5V
A32 A36 A33 A37 A34 A38 A35 A39
A48 A52 A49 A53 A50 A54 A51 A55
2114 x 8
A21
74LS244
A22
74LS374
A40
74LS244
A56
74LS244
A57
74LS374
DAL 15
DAL 8
DAL 7
DALØ
DAL 11
DATRDY
MRD/
DØ-D7
MWR
C57
100pF
R21
750
M6
EXH
LP
BB
LD/
LDB - LDIØ : DI2 · LDI4
SDN
RSYNC
MS
DALØ - DAL 15
SHT. 5
SHT. 4
SHT. 3
SHT. 1
J3
TEXT & ATTRIBUTE MEMORY
metrox electronic systems ltd.
SCHEMATIC DIAGRAM
GREB - ALPHA

DISPENS

CHARACTERS GENERATOR
ATTRIBUTES PROCESSING
VIDEO OUTPUTS

matrox electronic systems ltd.

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