MAC 16 OPTIONS
REFERENCE MANUAL
(INTERIM)

November 1969

FOREWORD

This document is an interim manual containing
Engineering design data. Information in this
manual is supplemented, and in some instances,
superceded, by information available in the fol-
lowing manuals:

MAC 16 Reference Manual

MAC 16 Interface Manual

MAC 16 Computer Maintenance Manual

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SECTION I

MAC 16 PROCESSOR OPTIONS

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PROCESSOR OPTIONS

      Processor options consist of add on features that improve the performance of the computer. They are provided with the addition of Printed Circuit (PC) cards and wired PC connectors in the computer's mainframe. Card slots 1-7, 10 and 11 are used for these options. This is summarized in Table 1.

Multiply/Divide -MD or -ME

      This option provides two new instructions: MPY and DIV. Refer to page 3-14 of the Computer Reference Manual. The instruction execution time for Divide is now 14 microseconds instead of 13 microseconds as given in the manual.

      In case of an overflow on Multiply (when minus one is squared) and Divide (when divisor is less than or equal to the dividend), the operands are not modified and the overflow indicator is set "on."

      The Multiply/Divide option is located in card slots 4 and 5 (-MD) or slots 1 and 2 (-ME). It is a separate high speed arithmetic unit contained on two logic cards. The MPU card contains control logic and the MPR card contains registers and a full-adder.

Multiplex Data Channel - MC1 to -MC5

      This option provides hardware control of data communication with up to 16 device controllers. A set of two I/O control words for each device controller is held within fixed locations in memory. One control word specifies block length of the data in characters or words, and the other specifies memory address of data and defines the mode of communication. In the character mode of data communication the Multiplex Data Channel, MDC, packs or unpacks characters. The MDC provides system data rates up to 200 KC in the multiplex mode

Table 1. Processor Options

Option	Designator		
Multiply/Divide	-MD	MPR, MPU	4, 5
Multiplex Data Channel			
Interrupts 1 and 3	-MC1	MDU, MDR, LAD-4	3, 4, 5
Interrupts 1, 3 to 7	-MC2	MDU, MDR LAD-8	3, 4, 5
Interrupts 8 to 15	-MC3	MDU, MDR, LAD-8	3, 4, 5
Interrupts 1, 3 to 15	-MC4	MDU, MDR, LAD-16	3, 4, 5
Interrupts 8 to 23	-MC5	MDU, MDR, LAD-16	3, 4, 5
Interrupts 4, 8, 16	-14	LAD-4	11 (basic)
	-18, -116	LAD-8, LAD-16	11
Interrupts 20, 24, 32	-120, -124, -132	LAD-16	11
		LAD-4, LAD-8 or LAD-16	7
Interrupts 36, 40, 48	-136, -140, -148	LAD-16	11
		LAD-16	7
		LAD-4, LAD-8 or LAD-16	2
Interrupts 52, 56, 64	-152, -156, -164	LAD-16	11
		LAD-16	7
		LAD-16	2
		LAD-4, LAD-8 or LAD-16	1
Line Driver	-LD	ICB-1	6
Line Receiver	-LR	ICB-2	1
Cable Driver	-GD	GAD	6
Cable Receiver	-GR	GAR	1
Bootstrap, TTY	-BT	BAD-T	10
Bootstrap, HSPT	-BH	BAD-H	10
Memory Interleave	-MI	none	none

and a data rate of 333 KC in the burst mode for a single controller.

Device Controllers that are controlled by the MDC are connected to the computer via the Programmed Data Channel, PDC, in the normal manner with one exception. That is, service request lines from the controllers are connected to a priority level logic card, LAD, that is a part of the MDC. This card may have a four, eight or sixteen level interrupt assembly depending upon the number of device controllers that are connected to the MDC.

Each device controller that is controlled by the MDC also must be assigned an interrupt level in the Central Processor Unit, CPU. A set of five, standard interrupt level assignments have been made and are summarized in Table 2.

The five interrupt assignments depend upon the number of device controllers that are controlled by the PDC and on the number of CPU interrupts that are provided.

-MCl, The MDC controls one or two device controllers. The CPU contains the basic four interrupts, -14. The MDC uses CPU interrupt levels 1 and 3. Priority two can be used if standard I/O service request is modified.

-MC2, The MDC controls from one to six device controllers. The CPU contains eight interrupts, -18. The MDC uses CPU interrupt levels 1, 3, 4 to 7. Priority two can be used if standard I/O service request is modified.

-MC3, The MDC controls from one to eight device controllers. The CPU contains sixteen interrupts, -116. The MDC uses CPU interrupt levels 8 to 15.

-MC4, The MDC controls from one to fourteen device controllers. The CPU contains sixteen interrupts, -116. The MDC uses CPU interrupt levels 1, 3, to 15. Priority two can be used if standard I/O service request is modified.

-MC5, The MDC controls from one to sixteen device controllers. The CPU contains at lease 24 interrupts, -124. The MDC uses CPU interrupt levels 8 to 23.

Table 2. MDC Option Configuration

CPU Interrupts	MDC Option Designators				
	-MC1	-MC2	-MC3	-MC4	-MC5
	Number of device controllers on MDC				
	1 or 2	1 to 6	1 to 8	1 to 14	1 to 16
0 - not available to MDC					
1	1	1		1	
2 - available to MDC if standard I/O is modified	(2)	(2)		(2)	
3	3*	3		3	
4		4		4	
5		5		5	
6		6		6	
7		7*		7	
8			0	8	0
9			1	9	1
10			2	10	2
11			3	11	3
12			4	12	4
13			5	13	5
14			6	14	6
15			7*	15*	7*
16					8
17					9
18					10
19					11
20					12
21					13
22					14
23					15*

* Highest level may not be available if power fail safe option is included.

The MDC consists of three PC cards: MDU, MDR and a LAD. They occupy slots 3, 4 and 5. MDU provides control logic and MDR provides register logic. The LAD card is a regular processor interrupt level PC card.

Interrupt Expansion -14, -18, -116, -120, -124, -132, -136, -140, -148, -152, -156, -164.

The basic MAC 16 contains four interrupt levels, -14. They are provided on one PC card, LAD. This card has three assemblies: four interrupts, eight interrupts and sixteen interrupts. Each interrupt represents a flip flop within the computer's Program Level Register, L. An interrupt signal may set its corresponding flip flop in this register at any time that the computer is "on."

Interrupt expansion up to 20, 24, or 32 requires a second LAD card in slot 11. Interrupt expansion up to 36, 40, or 48 requires a third LAD card in slot 2, and expansion to 52, 56 or 64 requires a fourth LAD card in slot 1.

It is occasionally necessary for LEC to provide receiver gates and external connections for external interrupt signals. Up to 11 interrupt signals can be interfaced by the service request logic provided on an LD or GD option module. These would be used by controllers which are interconnected to the CPU via the External PDC. Other remote interrupt signals may require special termination and if so, special options can be provided for these cases.

Line Driver -LD and Line Receiver -LR

A logic card called ICB is available in two assemblies: as a line driver and as a line receiver. The Line Driver option is wired into slot six. It provides long line drive on the PDC interface. It can drive up to 50 feet of twisted pair cable and can drive up to three line receivers. The Line Receiver option is only an external chassis option. Line Drivers and Line Receivers are required when MAC 16 device controllers are provided in an external chassis. A PDC cable set (three connectors with 41 pin Winchester connectors) are required for the interconnect. Cables are not included with the -LD or _LR options.

They are ordered separately.

The -LD and -LR options include a set of external cable connectors in their chassis.

It is not necessary to sell a line receiver with a line driver if the customer wishes to connect directly to the line driver. The interface is the same as the PDC except that all signals are inverted.

A complete description of the line driver and line receiver options is available in the MAC 16 Computer Interface Manual. Also see entries S-29, SS-30, SS-31 of the Computer Project Notebook.

Cable Driver -GD and Cable Receiver -GR

This option is similar to the Line Driver option, -LD, except that more drive is provided with discrete components instead of TTL, IC components. The Cable Driver option can drive up to 200 feet of PDC cable.

The cable driver option is provided with a PC card called GAD which is wired into slot 6. It has the same pin assignments as the ICB card that is used for the -LD option. The -GD option also provides three 41 pin external connectors for the PDC cables.

The Cable Receiver option, -GR, that is available for an external chassis is provided with a second PC card called GAR. The same PDC cables that connect line drivers and line receivers are used for interconnect.

Bootstrap, TTY   -BT

This option is the provision of a read-only, diode memory of 64 words. A bootstrap program is provided that can be automatically entered into the computer's memory and executed. The program will read a paper tape from the Teletype reader. The paper tape may be punched with any program in the bootstrap format.

It is easy to modify this fixed program by location of diodes on a matrix. Therefore, the option can be used for special functions.

Bootstrap, HSPT   -BH

This is the provision of the same diode memory in slot 10 as the -BT option. The fixed program is modified to read paper tape from the HSPT Reader. This option requires that the HSPT Controller (-HC) option is also included.

Memory Interleave   -MI

As presently defined this option does not include hardware; and is, therefore, a MAC 16 capability. It is the capability to suspend the computer at the end of its current instruction and to obtain control of the processor. It is the same capability that is used to provide the Multiplex Data Channel (-MC) and Multiply/Divide (-MD) options.

A special controller could be developed by the customer to take advantage of this capability. This controller could be used to access memory or processor registers. This controller should be located in slots 1, 2, 3, 4 or 5 replacing the -MC and -MD options. Location of the special Memory Interleave Controller in the mainframe is important to minimize wire lengths.

A complete description of this feature is being prepared for the MAC 16 Computer Interface Manual.

Combination Options

Different wire lists are required for different combinations of Processor Options. This difference occurs in the "daisy-chaining" of the PDC interface. The PDC is always wired to connector A of slot 8. The Line (Cable) Driver, (-LD), Multiplex Data Channel (-MC) and Multiply Divide (-MD) options also connect to the PDC interface. All connections to the PDC are pin for pin on connector A.

In order to minimize wire lists for combination options, the line (cable) driver, connector A will always be wired in whenever any one or all of the three options -LD (or -GD), -MC, -MD are designated.

The Multiply/Divide option (-MD) occupies slots 4 and 5 when the MDC option is not provided. If it is provided, the Multiply/Divide (-ME) cards occupy slots 1 and 2.

Figure 1 represents the PDC interface wiring for mainframe options.

Figure 1. PDC Mainframe Connections

PROCESSOR OPTIONS

	CARD SLOTS							
	1	2	3	4	5	6	7	8
Line (Cable) Driver Card: Wiring: -LD						-LD ICB	TTY-? YAD	-HC RAD
Multi/Div. Only or Mult/Div. & Line Driver -MD or -LD/MD				MPR	MPU	ICB	YAD	RAD
Mpx Data Chan. or Mpx. Data Chan. and Line Driver -MC or -LD/MC			MDU	MDR	LAD	ICB	YAD	RAD
Mult/Div and Mpx Data Chans or Mult/Div, Mpx. Data Chan and Line Drvr -ME/MC or -LD/ME/MC	MPR	MPU	MDU	MDR	LAD	ICB	YAD	RAD

MULTIPLY/DIVIDE OPTION

The multiply and divide calling sequences for software, and the entries for hardware multiply and divide are defined below. Any software generated using these entries may operate on any MAC-16, whether it contains the hardware multiply/divide option or not.

The calling sequences (entries) are:

Multiply: Divide:
multiplicand in A register   most sig half of dividend in A register
MPY   DIV
JMM   MPY   JMM   DIV
PTR   multiplier   PTR least sig half of dividend (also R)
PTR   least sig half of product   PTR   divisor
(return) – most sig half of product in A register (return) – quotient in A register

hardware timing: 10 microseconds   hardware timing: 13 microseconds
software timing: ∼350 μ sec average   software timing: ∼800 μ sec
                  ∼700 μ sec worst case

The double word fixed-point format is changed from

to
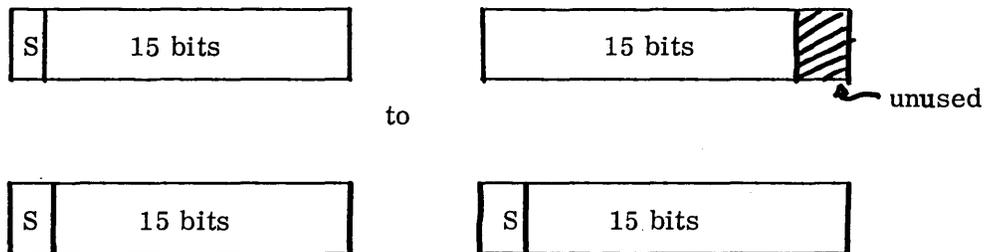
MULTIPLEX DATA CHANNEL, MDC

1.0   SYSTEM DESCRIPTION

The Multiplex Data Channel, MDC, is a MAC 16 option that will control data communication between the computer's memory and up to 16 device controllers connected to the Program Data Channel, PDC. The MDC control consists of accessing the data word, controlling the I/O transfer with the device controller, and monitoring the length of the record. The MDC does automatically with hardware what is normally accomplished in an interrupt service routine with software. Thus, by cutting the program overhead in I/O operations, the MDC facilitates greater overall data and throughput rates. The MDC will operate with any device controller that has a standard PDC interface.

Maximum data rates with the MDC are 200KC in the normal mode of operation and 333 KC in the burst mode. Both Input and Output devices may be accommodated in any combination; and, character devices may have their data packed and unpacked automatically. Devices may be assigned a relative priority according to system requirements, and a unique interrupt occurs automatically at the end of each record transfer.

1.1   Operation of the MDC

Up to 16 device controllers on the PDC may operate with the MDC if their unique Service Request signals are wired to the MDC hardware option instead of to program level interrupts. This will allow the MDC hardware to respond to a service request instead of requiring an interrupt service routine response. When the MDC detects a service request it will respond by automatically forcing the computer into an idle state between instructions, during which time the memory is accessed for address and block length, and the data is transferred to or from memory. In normal mode, the program automatically resumes execution until the next service request; and when the entire record has been transferred, the MDC will send a service request to the CPU that will cause a priority interrupt, thus informing the program of completion.

1.1.1   Channel Control Words

Associated with each device controller are two control words, CW1 and CW2, previously stored in memory by the program. CW1 provides a 16 bit memory address of the data to be transferred. CW2 provides a 13 bit block length field and a 3 bit mode field. The word formats are as follows:

```
0                              15
 ┌─────────────────────────────┐
 │        Memory Address        │
 └─────────────────────────────┘
            CW1
```

```
0   2 3                        15
 ┌─────┬────────────────────────┐
 │Mode │      Block Length       │
 └─────┴────────────────────────┘
            CW2
```
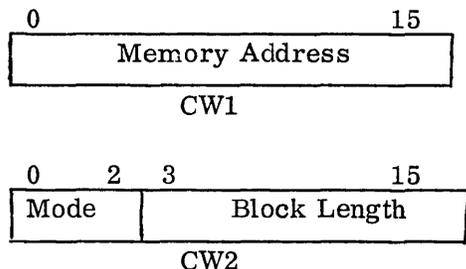
CW1 is incremented upon each word transferred and the block length is decremented each service request. Eight modes of operation are specified in the mode field, combinations of input or output, normal or burst, and word or byte.

1.1.1.1 Memory Address

CW1 is initialized before an I/O operation with a starting address. During the I/O operation CW1 will contain the address of the next data to be accessed and after the I/O operation is complete it will contain the address of the last data accessed plus 1.

1.1.1.2 Block Length

The block length field of CW2 is initialized before the I/O operation with the number (binary) of bytes or words to be transferred. During the I/O operation it will contain the number of bytes or words yet to be transferred and after the I/O operation is complete the block length field will normally contain zeros. If the record was terminated early, the block length will contain the number of words or bytes not transferred.

1.1.1.3 Mode Field

Bits 0 to 2 of CW2 provide 8 communication modes. The logic of the MDC examines these three bits to control its operation.

Bit	0	1
0	Output	Input
1	normal	burst
2	byte	word

The 8 modes are summarized as follows:

MDC COMMUNICATION MODES SELECTED BY CW2

CW2 Bits 0 1 2	Mode	Operation
0 0 0	Output, Normal, Byte	Obtain a word from memory address CW1. If bit position 15 of CW2 (block length) is a one, transmit the right byte and increment CW1. If bit position 15 of CW2 is a zero, transmit the left byte. Decrement CW2. Return CW1 and CW2 to memory.
0 0 1	Output, Normal, Word	Obtain a word from memory address CW1. Transmit this word. Increment CW1. Decrement CW2. Return CW1 and CW2 to memory.
0 1 0	Output, Burst, Byte	Obtain a word from memory address CW1. If bit position 15 of CW2 (block length) is a one, transmit the right byte and increment CW1. If bit position 15 of CW2 is a zero, transmit the left byte. Decrement CW2. Hold CW1 and CW2 for the next service request from the same device controller.
0 1 1	Output, Burst, Word	Obtain a word from memory address CW1. Transmit this word. Increment CW1. Decrement CW2. Hold CW1 and CW2 for the next service request from the same device controller.

1 0 0	Input, Normal, Byte	Receive a byte on data input lines 7 to 15. If position 15 of CW2 (block length) is a one, insert this byte into the right half of memory address CW1 and increment CW1. If bit position 15 of CW2 is a zero, insert this byte into the left half of memory address CW1, Decrement CW2. Return CW1 and CW2 to memory.
1 0 1	Input, Normal, Word	Receive a word (up to 16 bits) on the data input lines. Write this word into memory address CW1. Decrement CW2. Increment CW1. Return CW1 and CW2 to memory.
1 1 0	Input, Burst, Byte	Receive a byte on data input lines 7 to 15. If bit position 15 of CW2 is a one, insert this byte into the right half of memory address CW1 and increment CW1. If bit position 15 of CW2 is a zero, insert this byte into the left half of memory address CW1. Decrement CW2. Hold CW1 and CW2 for the next service request from the same device controller.
1 1 1	Input, Burst, Word	Receive a word (up to 16 bits) on the data input line. Write this word into memory address CW1. Decrement CW2. Increment CW1. Hold CW1 and CW2 for the next service request from the same device controller.

1.1.2 Executive Page

The fixed memory locations of channel control words is in the Executive Page, where each of the 16 possible device controllers is associated with a program priority level. The two channel control words CW1 and CW2 may be conveniently stored and examined by the program, and an end of record interrupt can automatically direct program flow to a terminating routine. The program levels assigned to MDC device controllers is a system variable, but in most cases, levels 8-23 will be assigned. The degree of priority assigned to each device controller will match the corresponding program priority level.

1.1.2.1 Control Word Locations

In the set of 4 locations associated with each program priority level, the MDC control words occupy 2 locations as shown:

Word	Program	MDC
0	P	(P)
1	X	CW1
2	A	CW2
3	Status	(Status)

While an MDC device controller is active, words 1 and 2, (normally X and A), will be accessed by the MDC to determine memory address, block length, and mode. Words 0 and 3, (P and Status) will not be accessed by the MDC.

1.1.2.2 Priority Level Assignment

Usually program priority levels 8-23 will be assigned to MDC device controllers. The corresponding locations in the executive page for each of the 16 device controllers is shown in the table.

Program level		Executive Page Locations				Relative device priority
Dec.	Hex.	(P)	CW1	CW2	(Status)	
8	08	0020	0021	0022	0023	0
9	09	24	25	26	27	1
10	0A	28	29	2A	2B	2
11	0B	2C	2D	2E	2F	3
12	0C	0030	0031	0032	0033	4
13	0D	34	35	36	37	5
14	0E	38	39	3A	3B	6
15	0F	3C	3D	3E	3F	7
16	10	0040	0041	0042	0043	8
17	11	44	45	46	47	9
18	12	48	49	4A	4B	10
19	13	4C	4D	4E	4F	11
20	14	0050	0051	0052	0053	12
21	15	54	55	56	57	13
22	16	58	59	5A	5B	14
23	17	5C	5D	5E	5F	15

1.1.2.3   MDC Interrupt

At the termination of an I/O operation a complete record has been buffered in or out. The MDC detects either that the block length has been counted down to zero or that the device has terminated the record. It then sends a service request to the program priority level associated with that device controller. When an interrupt at that level occurs, the registers in the executive page will be loaded into the CPU's operating registers as if a normal interrupt had occurred. The CPU will begin execution of a program at P, where the necessary stop commands should be executed. To activate a new buffer, this program level should be left before initializing the control words again and starting the device.

1.1.3   MDC System Configurations

The MDC may satisfy a variety of system configurations, from a few I/O devices to many. A few device controllers may be used or 16 maximum, all of which may be actively buffering data simultaneously. Each device controller may have from 1 to 16 I/O devices for a maximum of 256 devices, but only 1 device per device controller may be active at a time. A variety of device addresses may be assigned depending upon program priority level assignments. And, device controllers may be fully duplexed for both input and output as long as both modes do not operate in simultaneous buffers.

1.1.3.1 Device Controller Options

The MDC may operate with any number of device controllers, from 1 to 16, by selectively wiring in those service requests and program priority levels desired. The various options possible are as follows:

Option	Number of Device Controllers	Hardware Required
1	1 only	MDC, MDR
2	from 1 to 4	MDU, MDR, LAD-4
3	from 1 to 8	MDU, MDR, LAD-8
4	from 1 to 16	MDU, MDR, LAD-16

1.1.3.2 Device Address

The program priority levels assigned to MDC device controllers determines at least 4 bits of device address that must be assigned. In the simple case, if the MDC is assigned levels 0-15, the device controllers must have addresses X0-XF (Hex), where the decoding of X by a device controller is arbitrary. In particular, since the standard levels assigned are 8-23, the device addresses assigned are 08-17 (Hex). In this case 5 bits of address are predetermined and only 3 bits are arbitrary. The alternate device address assignments for the standard wiring are: 28-37, 48-57, 68-77, 88-97, A8-B7, C8-D7, or E8-F7. In any case, device controllers are assigned a set of 16 consecutive addresses with the 4 or 5 least significant bits determined by level assignment.

1.1.3.3 Multiple Device Controllers

If a controller has more than one device attached to it, the arbitrary bits of the device address identify the particular device. ECO and ESI instructions will use the full 8 bit device address to select or sense the device. Device controllers may accept commands for inactive devices (such as rewind tape) while another is actively transferring data with the MDC as long as service requests associated with those commands can be selectively inhibited.

1.1.4 System Operation with MDC

Initializing a buffer for a device controller connected to the MDC is analogus to PDC operation. Constants are stored (P, CW1 and CW2) and a command is issued to the device. Once initialized, the buffer continues automonously until an interrupt occurs. Additional buffers may be initialized at any time and normal programmed I/O to a non-MDC device is allowed in both interrupt and non-interrupt modes. All active devices will be transferring data over the same I/O data bus (PDC) on a time shared basis. Maximum data rates through the MDC are a function of certain system variables which affect the response time to a service request; i.e., longest instruction being executed, relative priority of device controllers, number of devices active on the MDC, etc. Certain free running devices require quick program response to the termination of a buffer.

1.1.4.1 Initializing a Buffer

Storing P, CW1, and CW2, does not in itself start the I/O operation with the MDC. The device controller must be issued a command to start (input or output) with interrupts allowed. The MDC will not react until the first service request is raised by the device controller, indicating a request for data. If the block length of CW2 is non-zero the MDC will attempt a data transfer with the device.

If the block length is zero (failure to initialize CW2), the MDC will not attempt to transfer data, but send a service request (interrupt) to the CPU; and because the device controller did not transfer data, the device service request will remain active. For this reason the control words must be properly initialized before the ECO command to allow interrupts is executed.

1.1.4.2 Terminating a Buffer

An interrupt from an MDC device calls for either of two actions, reinitialization of the buffer or the termination. Terminating consists of stopping the device and inhibiting interrupts (service requests). This command must be issued before another service request is raised or the MDC will begin cycling on zero block length. The minimum time from the last service request to the time when a stop command can be executed is 25 microseconds.

1.1.4.3 Data Rates, Response Times

Maximum data rate in the normal mode is 200KC, either for words or bytes, one device or 16 devices. The 200KC figure comes from the fact that 5 1-microsecond cycles are required for each word or byte transferred. If there is more than one device active on the MDC, the maximum rate must be shared on a relative priority basis. Device controllers must have adequate buffering to hold data for the length of time it takes the MDC to service all devices of a higher relative priority plus the maximum possible response time to the first service request. The maximum possible response time is the execution time of the longest instruction being executed plus 1 cycle. (Shift-15 is 5+1 = 6 microseconds, hardware Divide is 13+1 = 14 microseconds). With 16 devices active, the device controller of the lowest relative priority must be able to hold data 5x16+14=94 microseconds, or longer. Without data buffer registers this device could transfer data no faster than about 10KC. In fact, devices of higher priority with rates higher than 12.5KC would degrade the maximum data rate of the lowest even further. In general, the system determines the maximum data rate for a device on a given priority. The MDC will not detect a timing error if it occurs but most device controllers are designed to do so, making the information available in the controller's status word.

1.1.4.4 Burst Mode

If the burst mode is designated in CW2 for any device on the MDC, no program execution will occur after the first service request from that device. Usually, the burst mode will be used with those devices that have a long start or search time followed by a high data rate. Rates of any other active device – either MDC or normal PDC – must be less than the total block transfer time of the burst device. The maximum data rate for the burst device itself is 333KC, with increments of 1 microsecond added for waiting on rates less than that.

1.1.4.5 Unknown Record Lengths

The MDC will input from devices that have unknown record lengths, magnetic tape, for example. The records may be read in either the burst or normal mode. Termination of the data transfer will be under the control of the device controller, which will sense the end of the record and not acknowledge the next data transfer. The block length in CW2 would have been initialized with some number greater than the length of the record (8,191 words or bytes maximum); and, after the termination the block length in CW2 (or A) will be a number equal to the original block length less the actual length of the record, less the number of "extra" service requests that the controlle requires to terminate. The memory address in CW1 (or X) will be the address of the last word

or byte of the record increased by the number of extra service requests.

Example:

A device controller will issue one extra service request at the end of a 10 character record. When the MDC attempts to input on the last service request, the device controller will not acknowledge. The I/O operation is performed in the normal and byte mode. The contents of CW1 and CW2 are:

	Before		After
CW1	0100		0106
CW2	800F		8004

The contents of memory will be:

Addr			
0100	no change	1st	
101	2nd	3rd	
102	4th	5th	bytes of
103	6th	7th	record
104	8th	9th	
105	10th	zeros	
106	no change		
107			
108			

The number of extra service requests following the last character of a record is a characteristic of the device controller. The MDC only knows to terminate the data transfer by detecting no acknowledge. If there are any more service requests after the one that was not acknowledged the block length and memory address will be counted for each.

1.2   I/O Instructions

The four I/O Instructions, EDO, EDI, ECO, and ESI may be used with any device controller connected to the MDC. Programming with these instructions should be as if the device controller were operating in inhibited interrupt mode. In most cases, only the ECO and ESI instructions are used in programming a device on the MDC. EDO and EDI may be executed, but only if the special requirements of a device controller need them.

1.2.1   ECO and ESI

ECO. Used to allow interrupt and start device before the I/O operation, and after the I/O operation, to stop the device and inhibit the interrupt. The ECO may be used for any other special functions required by the device controller.

ESI. Used to sense the status of a device controller. The ESI should not be executed while an I/O operation is in progress because data may be lost.

1.2.1.1 Command and Status Formats

The format of commands and status will be as defined in the description for a particular device controller. Communication using an ECO or ESI is through the A Register, as normally.

1.2.1.2 ECO Device Selection

If a device controller on the MDC controls more than one device, the ECO instruction may serve the purpose of selecting which device is to transfer data.

1.2.2 EDI and EDO

The EDI or EDO instructions may be executed to transfer a final data word after the I/O operation is complete, if the device controller so requires. For example, after stopping a paper tape reader one or two more characters may be read (depending upon timing). An EDI (in inhibited interrupt mode) will input a character into the A Register if the device controller is ready to input.

1.2.3 EAI

The EAI instruction serves no useful function to devices connected to the MDC. Device controllers will not be wired to respond to an EAI.

1.3 Program Requirements

The primary difference between programming for MDC I/O and programmed I/O is that the MDC transfers data asynchronously with respect to program decision logic. It is necessary to completely input a record before making decisions on the data, for example; and on output, the full record must have been operated upon before a buffer is initiated to send it to a device. If so desired, incoming data can be monitored by observing the progress of a buffer. The control words CW1 and CW2 may be read to find the address of the last data to be input. And computation of an output record may likewise be in process if it is known that the computation will proceed faster than the output device will accept data. But more typically, programs are written such that buffers are traded back and forth – computation proceeding upon one record while the next is being buffered in or out. In going back and forth between buffers the program must execute a buffer turn around, which may or may not limit the data rate. In a real time situation where data is input, computed upon, and output, the critical time may be buffer turn around, and it may be necessary to stop a device between records.

1.3.1 Rules for Programming

The following rules should be observed for programs using devices on the MDC.

1.3.1.1 Interrupt Inhibit in CPU

Interrupts should be allowed in the CPU. If interrupts are inhibited in the CPU the end of record interrupt from a device on the MDC may be missed or delayed. Otherwise, the Inhibit Interrupt does not affect the normal transfer of data.

1.3.1.2 Interrupt Inhibit in Device Controller

Interrupts (service requests) should be allowed in device controllers actively transferring data with the MDC. No data will be transferred (by the MDC) if the device interrupt is inhibited. In those inactive devices on the MDC that normally request data when at rest (example: HSPT Punch) the device interrupts should be inhibited. If not, the MDC will attempt to service the device.

1.3.1.3 Sensing Status

An ESI to a device actively transferring data with the MDC should not be executed or data will be lost. Status may be sensed before and after the data transfer as normally.

1.3.1.4 Halting the CPU

The CPU should not be halted when a buffer is active. Since the MDC requires the internal CPU clock, a halt will cause the MDC to lose data, and the device may not be properly stopped at the end of its current record.

1.3.2 The Active Buffer

An MDC buffer is made active by allowing a device controller to send service requests to the MDC. The MDC reacts to any service request in same manner; i.e., by accessing CW1 and CW2 for that device and attempting a transfer of data. The idle state only occurs after the completion of the current instruction so allowances should be made for devices with high data rates. An active buffer will remain active until the interrupt is inhibited in the device controller.

1.3.2.1 The Idle State

The MDC will cause an idle state at the end of an instruction, at the end of the 6 microsecond transition from one priority level to another, or during the quiescent state. The idle state will not be entered after a single cycle instruction. If hardware MPY/DIV is installed the idle state will not be entered until the MPY or DIV instruction has completed execution. If an MDC service request is pending at the same time a higher level program priority is set, the idle state for the MDC will be entered first.

1.3.2.2 Quiescent State

The MDC will service active buffers in the quiescent state. If a priority interrupt occurs in the quiescent state while the MDC is servicing a device, the new program level will not be entered until the service has finished. Since in the quiescent state new program levels may be entered while the interrupts are inhibited in the CPU, the termination of a buffer will always cause an interrupt.

1.3.3 A Typical MDC Driver Routine

A typical use of the MDC might be to operate on a stream of data. In this type of operation the CPU may be required to (1) input a record (a line or card image), (2) operate on the record, and (3) output a record.

Without knowing anything about the execution times of each of the three operations, a driver routine can be written for the MDC that will maximize the overlap. A method of alternating buffers is suggested here. In this scheme the CPU is operating on record N, while inputting record N+1 and outputting record N-1. Four buffer areas are required for data: two input buffers and two output. Two flags are required: a flag for the input device and a flag for the output device. Each flag is set when the buffer for that device is initialized and reset when the buffer is finished. Assume that while operating on record N, neither its source area (where the record was input) nor its destination area (where the record will be later output) can be used until the operation on that record is finished. Then if record N+1 is completely input, the input buffer for record N+2 may not be initialized until the operation on record N has finished. Likewise, if record N-1 has been completely output, the output buffer for record N may not be initialized until the operation on record N has finished. In the program level for each device, the CPU should stop the device, inhibit service requests, and reset the device flag. Initialization for the next buffer will be in the main part of the routine after the operation on the current record has finished and after the respective flag of each device has been reset. It will consist of storing the control words, starting the device, allowing the service request, and setting the flag. Since it is not known which device, input or output, will finish before the other, the looping on flags reset will have to be split into two paths. Also, assuming the last record will be some kind of an END record, provision must be made for preventing any additional records being input if not desired. The use of a stop flag is suggested. A flow chart for this hypothetical driver is shown.

2.0 CONTROLLER DESCRIPTION

The MDC consists of three standard size PC cards installed in the CPU main frame and wired into the back panel nest. Other options may be required to work in conjunction with the MDC, such as a second LAD board (providing up to 32 priorities) and various combinations of I/O device controllers. In general, each system with an MDC will be slightly different. Supplementary documentation will be provided to completely define a given installation.

2.1 Logic Description

Logic of the MDC can be described in the following bread areas: registers, service requests, algorithm, control states, control flip flops, micro-ops, instruction decode, and address generation. For more complete details refer to the block diagram, flow chart, and logic diagram.

2.1.1 Registers

The MDC contains three registers, a data register (C), a register for CW2 (B), and a priority register (L) for service requests. C and B are located on the register board MDR and L is located on LAD-MDC.

2.1.1.1 C Register

C holds the data word during an input or output operation. It is a full 16 bit register constructed of D-type flip flops. The data path into C is from the CPU function bus. The outputs of C are gated onto the PDC data bus, either a full 16 bit word or the left 8 bit byte onto the right byte position.

MDC Driver, Alternate Buffers

Start

Reset flags:
$0 \rightarrow IN, \phi UT,$
END

Initialize
Input Buf 1
$1 \rightarrow IN$

Is
END — Yes → C

No

Initialize
Input Buf 2
$1 \rightarrow IN$ → A

Is
IN = 0

No   Yes

B

Operate on
Input Buf 2
Fill
Output Buf 2

Is
$\phi UT = 0$ — Yes → Initialize
Output Buf 2
$1 \rightarrow \phi UT$

No

Is
IN = 0

No   Yes

Is
END — No → Initialize
Input Buf 2
$1 \rightarrow IN$

Yes

Set flag
$1 \rightarrow END$

Is
$\phi UT = 0$ — Yes

No

Initialize
Output Buf 2
$1 \rightarrow \phi UT$

Is
END = 1 — Yes → C

No

A

SHEET 1

1-27
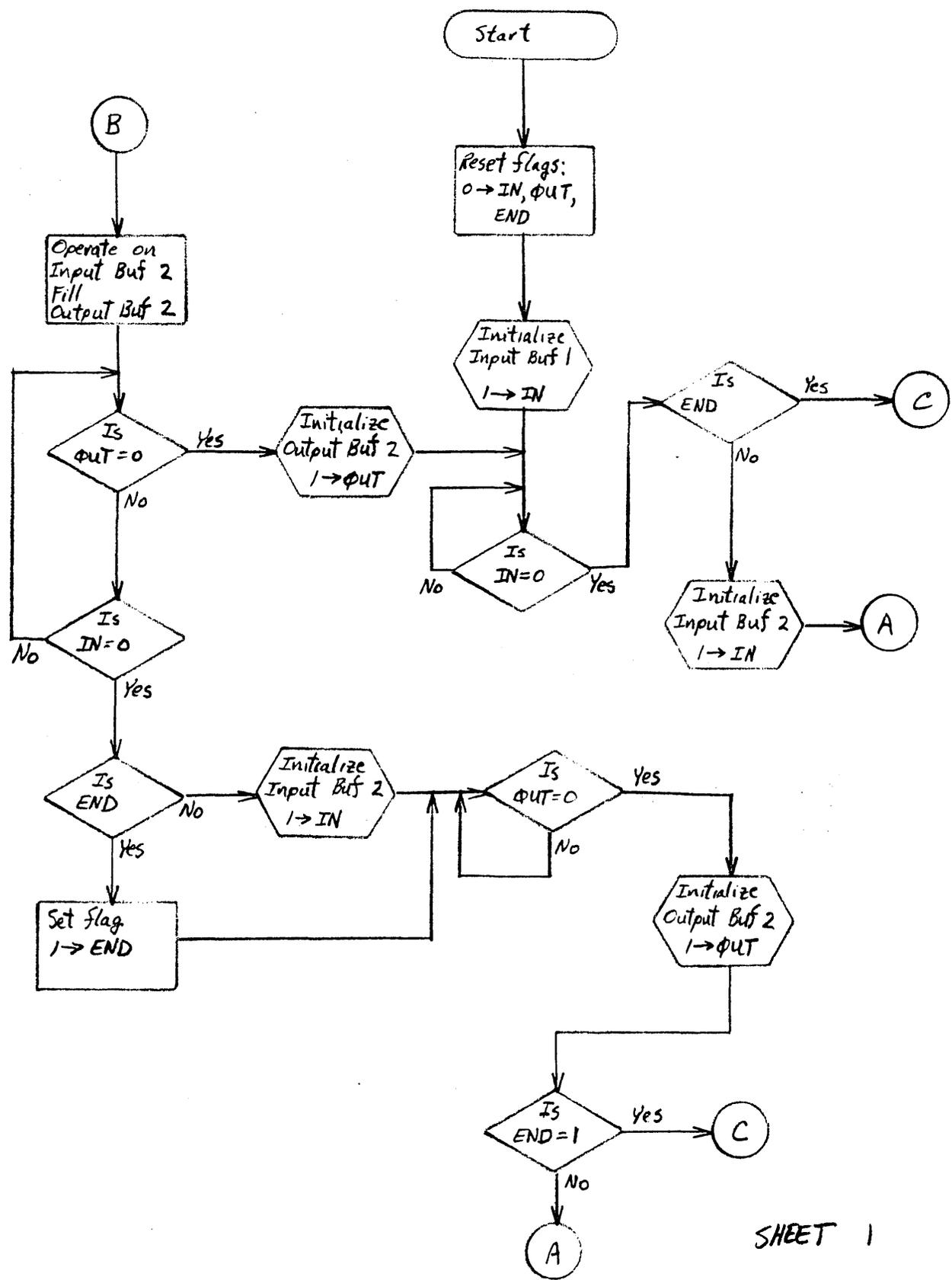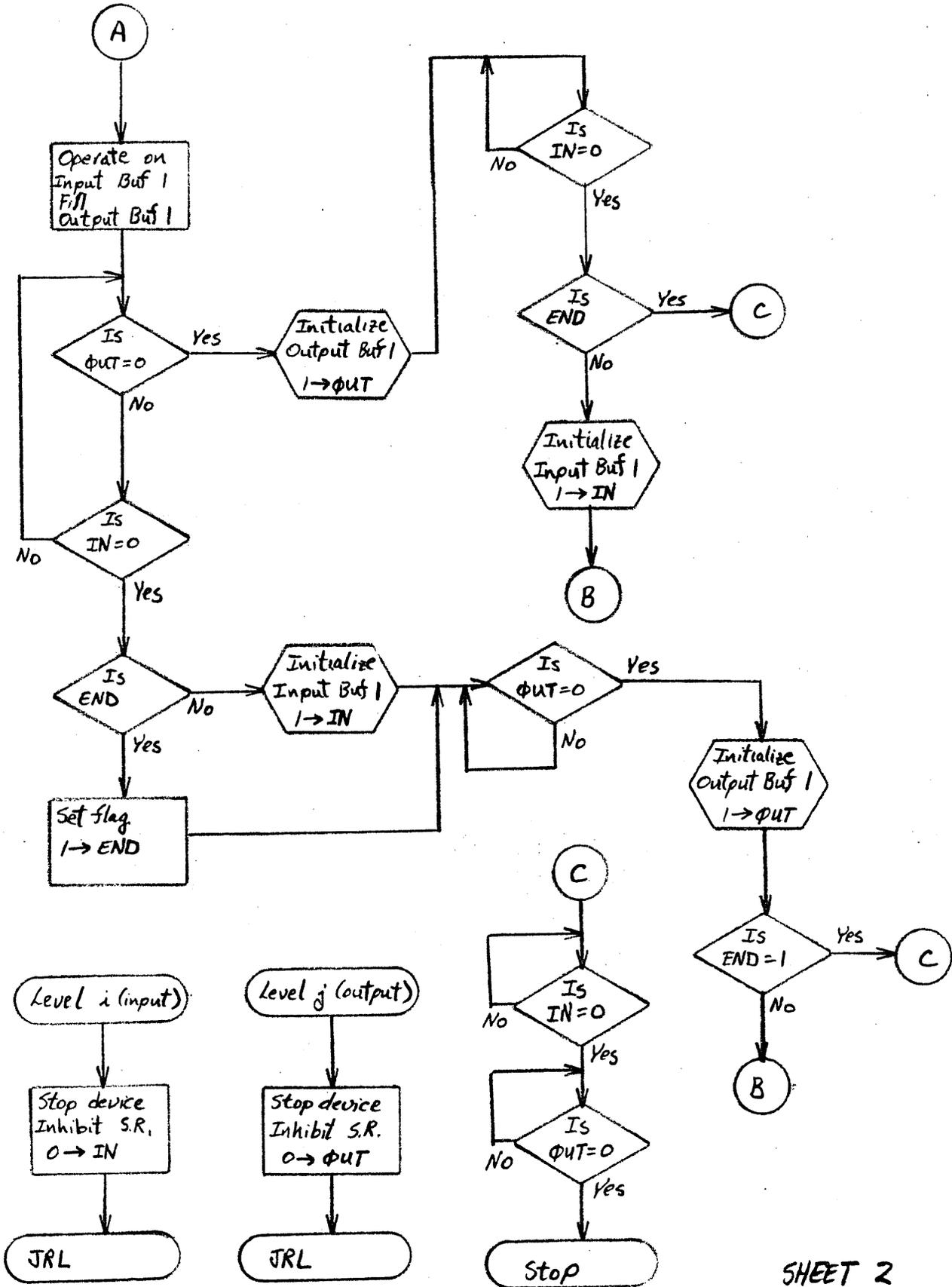
SHEET 2

2.1.1.2 B Register

B holds Control Word 2 which contains the mode bits (Input/Output, Burst/Normal, and Word/ Byte) and the Block Length. The data paths into and out of B is via the CPU function bus. Associated with bits 3-15 of B is a binary down counter. The mode bits are not affected by the counter.

2.1.1.3 L Register

Service Requests are remembered in the dual rank L Register which determines priority of devices. Each of 16 possible service requests directly sets a flip flop in the upper rank of L, and the upper rank is transferred to the lower rank once each machine execution cycle. The lower rank is encoded into a 4 bit device number which is held in 4 flip flops during the idle state.

2.1.2   Service Requests

If any of the 16 flip flops is set in the lower rank of L, the signal SERV-P indicates to the MDC logic that an idle request should be initiated. Once the MDC is in the idle state, however, SERV-P is ignored and only the service request corresponding to the device number is used. The device number is decoded into 16 decode gates, which are in turn, anded with the corresponding service request, and ored together to form a signal called selected service request SSRA-P. Associated with the selected service request are two flip flops, SSR and KSR, that provide the logic with a signal HSRA-P which is essentially the selected service request synchronized with the input/output control lines, JEDI-N and JEDO-N. This logic differentiates between an old service request and a new one for a selected device while ignoring service requests from other devices.

2.1.3   Algorithm

The algorithms for input and output are slightly different. Both use the same set of control states, but in a different sequence. For details of the algorithm see the flow chart. Briefly, the sequence of machine cycles is as follows:

1) Access CW2 and transfer contents to B.
2) Access CW1 and transfer contents to W. Decrement B13-15 if not zero.
3) If input, increment W and store in CW1. If output, access W and transfer the contents to C.
4) If input, store data in W. If output, increment W and store in CW1.
5) Store B in CW2.

Variations and qualifications of this algorithm of course depend upon the modes burst/normal and word/byte. And further, the sequence will be qualified by device acknowledge.

2.1.4   Control States

The MDC algorithm is controlled by 7 flip flops, one per control state. Each state is a full 1 microsecond machine cycle and includes slots S0, S1, S2, and S3. Transition from one control state to another is on the trailing edge of S3. The function of each control state is as follows:

State	Function
A	Access CW2 (Read cycle)
B	Access CW1 (Read cycle)
C	Access CW1 (Store cycle)
D	Access data (Read or store cycle)
E	Access CW2 (Store cycle)
F	Extra output cycle
X	Wait cycle (Burst mode)

2.1.5   Control Flip Flops and Signals

The following is a list of control flip flops in the MDC and their function.

FF	Function
KEO	Data Out control line. Same as JEDO-N.
KEI	Data In control line. Same as JEDI-N.
KAQ	Acknowledge. Set by JACK-N.
KID	Idle request. Same as JRID-N.

The following is a list of control signals. These signals are identical to bits 0, 1, 2, and 15 of CW2.

Sig.	Function	Bit
KIOA-P	Input = 1, Output = 0	0
KBNA-P	Burst = 1, Normal = 0	1
KWBA-P	Word = 1, Byte = 0	2
KRLA-P	Right = 1, Left = 0	15

2.1.6   Micro-Ops

Micro-ops in the MDC can be put into two groups, (1) those that cause micro-operations in the CPU, and (2) those that cause micro-operations within the MDC. Each is listed here with its function.

2.1.6.1 Micro-Ops CPU

Mnemonic	Function
MUMCA-N	Memory cycle
MUUYA-N	Read left byte
MUUZA-N	Read right byte
MUZDU-N	Clear D Register
MUMXP-N	LP5-0 to M08-13
MUM14-N	1 to M14
MUM15-N	1 to M15
MUMIA-N	F bus to M
MUWIA-N	F bus to W
MUWOA-N	W to O bus
MUDIA-N	F bus to D

MUDOA-N	D to O bus
MUJJA-N	Inhibit A to PDC
MUJOA-N	PDC to O bus
MURLA-N	O bus right to F bus left
MULLA-N	Inhibit O bus left to F bus left
MUSSA-N	Adder to F bus
MUETA-N	1 to Adder Carry-In

2.1.6.2 Micro-Ops MDC

Mnemonic	Function
EORL-P	End of record Service Request
MHLA-N	L upper to L lower
MZLH-P	Clear L upper
REBF-P	B to F bus
RCBD-P	Count B down
RCZB-N	Clear B, Clear decoded L lower
RELL-P	C left to PDC left (byte)
RERR-P	C right to PDC right (byte)
RELR-P	C left to PDC right (byte)
RCFC-P	F bus to C
RCFB-P	F bus to B
MFLA-P	Set decoded L lower
RCSF-P	Set Device Number Flip Flops

2.1.7 Instruction Decode

The MDC must anticipate the end of an instruction to set the first control state A. Bits 0-7
of the I register are decoded by the MDC to provide a signal HSAJ-P that will be true for those
instructions terminating execution in the TEA state. The "double execute" class of instructions
will not cause state A to be set until TEB state. Likewise, the Shift instructions will not set
the A state until the shift count has been counted down to zero. The instruction decode for
hardware MPY or DIV are not included in the MDC instruction decode since they must first
enter the idle state under their own control before terminating execution. After MPY or DIV
at least one more instruction will be executed before control state A can be set.

2.1.8 Address Generation

From the 4 device number flip flops two addresses must be generated, the address in the
executive page of either CW1 or CW2, and the Device Address of the device controller being
serviced.

2.1.8.1 Executive Page Address

The MDC transfers an executive page address into the M register via the same path that the CPU
uses to access program level registers. This transfer path is mechanized as a two port entry
into M08-13 by a set of gates in the MDC. The signal HMEM-P selects either the program level
register LP0-5 or the device number flip flops FF0-3 according to whether the MDC is initiating
a memory cycle or not. The device number flip flops are wired to generate the proper address
for the executive words corresponding to the program priority level assigned to each device
controller. Bits 14 and 15 of M are set by micro-ops.

2.1.8.2 Device Address

Once a device controller on the MDC is assigned a particular program priority level 4 or 5 bits of the device address are determined. The remaining bits of the device address may be assigned 1's or 0's by wiring ground to certain pins. The device address is ored onto the 8 address lines of the PDC only during an MDC service of the device.

2.2 Hardware Configuration

Only one basic hardware configuration of the MDC can exist but slight variations may be tailored to different system requirements. Most variations will be differences in back panel wiring affecting priority level assignment, device address, etc. A few systems may use a LAD-8, LAD-4, or no LAD. Here again only minor wiring differences will occur. For the following discussion, the standard MDC system is assumed.

2.2.1 Cards

The MDC option consists of three standard size printed circuit cards MDR, MDU, and LAD-MDC. These cards must be installed for the CPU to function. Other LAD cards may be required to expand the number of program levels but these are considered a separate option.

2.2.1.1 MDR

The MDR board contains the MDC registers. It is installed in location __4__ and contains 66 integrated circuits. Maximum power consumption is 1.13A of +5V.

2.2.1.2 MDU

The MDU board contains the MDC micro-ops, It is installed in location __3__ and contains 74 integrated circuits. Maximum power consumption is 1.46A of +5V.

2.2.1.3 LAD-MDC

The LAD-MDC board contains the service request priority register. It is installed in location __5__ and contains 57 integrated circuits. Maximum power consumption is 1.1A of +5V.

2.2.2 Wiring

The MDR, MDU, and LAD-MDC boards are installed in the CPU main frame and connected to the back panel wire nest by point-to-point wiring. No other special connectors are involved except those required for I/O device controllers. The wires may be broken down into 6 groups: (1) CPU clock and timing signals, (2) Micro-ops, (3) Interconnects, (4) PDC bus, (5) Service Requests from controllers, and (6) Service Requests to CPU priority level.

2.2.2.1 CPU Clock and Timing Signals

This group of wires includes the clocks CA, CB, the slots S0-3, certain control states, and other internal CPU signals. The mnemonics are the identical four letter mnemonic as used in the CPU logic, preceeded by a C. Fan out for these signals is provided on the MDU board.

2.2.2.2 Micro-Ops

This group of signal wires originate on the MDU and go to the CPU where they drive the CPU micro-ops. They are typically tied collector drivers. The mnemonics are the same as the micro-op they drive, but preceeded by a M.

2.2.2.3 Interconnects

This group of wires are interconnections between the MDR, MDU, and LAD-MDC boards. They are four letter mnemonics.

2.2.2.4 PDC Bus

The PDC data bus and control signals are bussed onto the MDU and MDR boards on the standard pins. Their four letter mnemonic begins with a J. Typically the signals are tied collector circuits. From the MDC they may be jumpered to another device controller or to a line driver/receiver board.

2.2.2.5 Service Requests from Device Controllers

There is one service request per device controller, 16 possible, and they are wired up to the LAD-MDC and MDR. The four letter mnemonics are called out in the MDC prints as SR____, but in the various device controllers they may have different mnemonics. Normally, the service requests go to a CPU LAD board, so if a device controller is to be changed from normal PDC operation to MDC operation, the wire must be physically moved.

2.2.2.6 Service Requests to CPU Priority Level

These wires, 16 possible, go from the MDR board to a LAD board in the CPU. The four letter mnemonic begins with JL. Not all of them may be wired in, depending upon the I/O configuration. Unused priority levels in the CPU must be grounded, but in the MDC an unused service request driver may be left unterminated.

2.2.3 Test Points

Most significant signals are available for probing on the back panel connectors, A and B. None are available on the test connector C.

ICB INTERFACE MODULE

The ICB module design provides for two complementary configurations: ICB-CPU Driver; ICB-I/O Receiver. The CPU Driver is used within the computer to drive and to receive from the external PDC cables. The I/O Receiver provides the capability to interface to the PDC cables to form an I/O bus identical to the internal CPU PDC.

The following characteristics apply to both ICB configurations.

1. Driving Element – an SN7440N with a series 68 ohm resistor.

2. Receiving Element – any of SN7400 family or equivalent.

3. Cable Length – up to 50 feet.

4. Loading–

    a. One to three SN7400 loads

    b. If a fourth load is required, a resistor of $390\Omega \pm 2\%$ must be placed between the input of the receiving gate and ground.

5. Signal Delay –

    a. Cable insertion delay is 1.5 nsec per foot.

    b. Gate pair – delay is 55 nsec (20/35).

    NOTE: For additional information on the ICB Interface Module refer to the MAC 16 Interface Reference Manual.

MEMORY INTERLEAVE

GENERAL

The MAC 16 is provided with an optional high data rate input-output channel called the Multiplex Data Channel, MDC. The MDC will service up to sixteen input-output device controllers on a priority demand basis. Data communication is controlled by sixteen pairs of pre-stored control words that specify the type of communication, block length and memory address. The control words are located in fixed memory locations. The types of communication that may be selected are in-out, burst or single datum and byte or word. Maximum communication rates are 200KC in the non burst mode or 333KC in the burst mode.

The MDC functions by temporarily placing the processor into an "idle" state at the end of its current instruction. It then takes control of the processor's memory word register (D Register), memory address register (M Register) and memory control lines in order to access memory. The MDC also uses other hardware functions of the processor to modify control words.

This "external" control and access to the MAC 16 Processor is available to the user who wishes to design an input-output channel that satisfies his own system requirements better than those functions of the multiplex Data Channel. This report specifies the available signals and connector pins and describes the logic design requirements for this special device.

This device is called the Memory Interleave Channel. If it is provided with its own hardware memory address register, it may interleave memory cycles in-between processor instructions at a burst rate of up to one megacycle. Data may be either read or written into memory. Control for packing eight bit bytes into a 16 bit word is provided. Access to all memory (up to 65D) is possible.

In general, the Memory Interleave Channel may be designed to be as complex as is required. If it provides a memory address, it can load it into the processor's internal M register, and initiate a memory cycle. Data to be written is then loaded into the processor register, or, data to be read is output from the D Register near the end of the cycle. Special input signals are provided for manipulating the register transfers and initiating the memory cycle. These control signals are referred to as micro-operations. Also provided are timing signals derived from the computer's internal clocking source. The timing signals are combined with the Memory Interleave Channel's own logic to generate the micro-operations at the proper time. Memory cycles are interleaved between instructions and sharing the processor's D and M Registers does not interfere with program execution other than to temporarily suspend processing.

The Memory Interleave Channel may be initialized with starting address via the Programmed Data Channel (PDC) or a starting address may be stored in memory at a specific location. If an address is stored in memory the interleave channel may use the processor's internal parallel adder to increment it once for each word transferred. The block length may also be stored in memory, but there are no provisions available for internally counting the block length down to zero.

Likewise provisions for comparing a terminating address to the current address would have to be mechanized externally in the Memory Interleave Channel. When the block of I/O data has been completely transferred, the Memory Interleave Channel may communicate with the program by setting a priority interrupt. Up to 64 levels of interrupt are available as a separate option. For details of interfacing to the PDC refer to the MAC 16 I/O Interface Manual.

MEMORY INTERFACE

Four data paths are provided for interfacing to memory, two input and two output. These paths are "fan-in" and "fan-out" pins of four parts of the processor. This is shown in the following diagram. The data paths are as follows:

1. Function Bus Input. Data may be loaded into either the M or D Registers via this path, however, packing of byte data must be performed externally.

2. I/O Data Bus Input. This is the standard PDC data bus, but data may be input only. Byte data may be packed into the D Register and address may enter the M Register.

3. Function Bus Output. The D Register may be output via this path, but micro-operations for unpacking byte data are not available.

4. D Register Output. The actual D Register is available for output. The earliest possible access is via this path.

CIRCUIT INTERFACE REQUIREMENTS

Circuits to be used throughout are TTL integrated circuits series 7400 or equivalent. All input signals are to be open collector (7401 or 7405) with only one driving source. (Collector resistors are not required at the source since they are already installed at the destination). Output signals are typical 7400 series outputs and should not be loaded by more than one 7400 series load, or equivalent.

The electronics is to be mounted on three MAC 16 standard size PC boards and installed in the MAC 16 mainframe where back panel wiring should be kept to a minimum. The three card slots of the MDC may be used. If the Memory Interleave Channel is not wired into the processor's mainframe, it must be located within 18 inches of the available interface pins. Clock signals provided for timing should not go through more than two inverterpair delays from interface out to interface in.

The logic conventions in the MAC 16 are as follows:
(Mnemonic) – N means negative polarity. A logic true is a low signal.
(Mnemonic) – P means positive polarity. A logic true is a high signal.

IDLE REQUEST AND RESPONSE

Since the computer is normally executing instructions and accessing memory, the Memory Interleave Channel must first request an idle state before initiating a memory cycle. The following signal, a flip flop to be provided by the Memory Interleave logic, causes the computer to assume an idle state:

MEMORY

ADDRESS

DATA

Micro
Operations

M Register

D Register

Function Bus

I/O Data Bus

Clocks

Input Paths

Output Paths
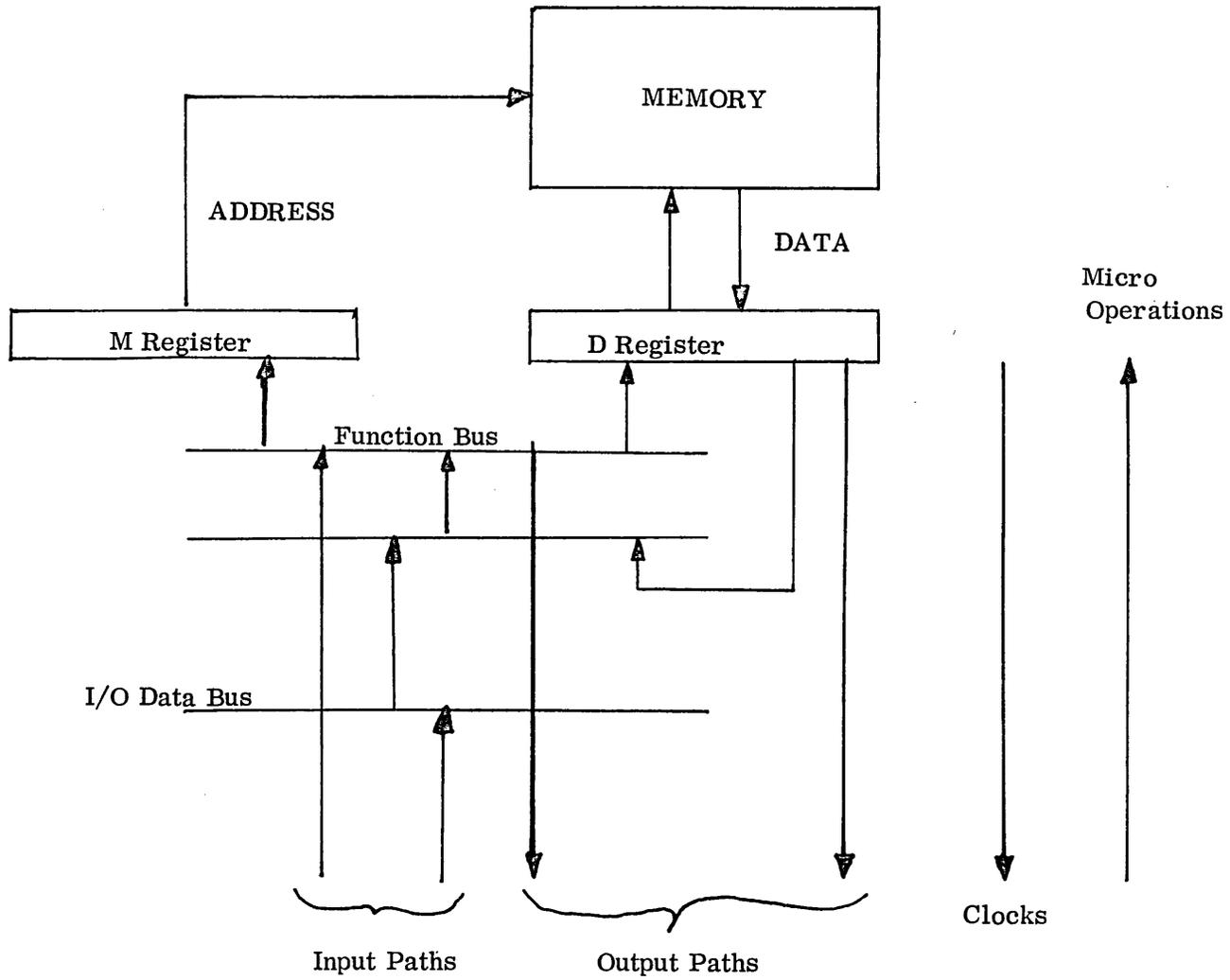
MEMORY INTERLEAVE CHANNEL

Signal	Connector	Pin	Name	Description
JRID-N	A 15	25	Idle Request.	A flip flop to be set and reset by the "SO" clock pulse.
JSOA-N	A08	63	"SO" clock pulse.	250 nanosecond pulse provided for timing.

No memory cycles should be started until the computer has responded with the following:

JIDL-N	A12	53	Idle Response.	A flip flop indicating computer is in an idle state.

To release the computer from an idle state, the idle request flip flop, JRID-N, should be reset on the "SO" clock pulse of the last memory cycle desired.

Idle Request Timing

The delay between the idle request and the time the computer goes into an idle state is variable depending on the instruction being executed and machine state. The quickest response would be 1 microsecond. The longest delay would be the execution time of the longest instruction. (Shift, with N=15 is 5 microseconds, Divide is 13 microseconds). An idle request will not be honored after a single cycle instruction.

Quiescent State

The Memory Interleave Channel may cycle the memory while the computer is in the quiescent state. An idle request is required as above, the computer will not respond by going into the idle state. As long as the idle request is active the computer will be locked up in the quiescent state and the memory may be cycled. Quiescent state is determined by the following signal:

CTQSS-P   B13   70   Quiescent state

Idle Request In A Machine With Hardware Multiply/Divide

Since the MAC 16 hardware Multiply/Divide option also uses the idle state, the Memory Interleave Channel may not signal an idle request if either of these two instructions is being executed. The necessary logic to prevent an idle request conflict should be a lockout flip flop which remembers that a Multiply or Divide instruction was read from memory during the instruction fetch cycle (TIN). To mechanize this logic, the following signals are provided:

Signal	Connector	Pin	Name
CIMPY-N	B15	29	Multiply decode
CIDIV-N	B15	32	Divide decode
CTINL-P	B12	09	Instruction fetch state, TIN
CTS3R-N	A15	39	"S3" slot
CTCBR-N	A11	34	"CB" clock

The lockout flip flop is set or reset at state TIN, slot S3 and clock CB. This logic should be included in the logic for idle request (which is normally set on "SO" clock). If hardware Multiply/Divide is not installed, this logic can be left out.

Memory Control Signals

Memory cycles are controlled by the following micro-operations:

Signal	Connector	Pin	Name	Description
MUMCA-N	A13	41	Memory cycle request.	250 nanosecond pulse at "SO" clock time.
MUUYA-N	B13	46	Read left byte.	250 nanosecond pulse at "SO" clock time.
MUUZA-N	B13	47	Read right byte.	250 nanosecond pulse at "S1" clock time.
MUZDU-N	A13	63	Data register clear.	250 nanosecond.
JSOA-N	A08	63	Clock pulse "SO".	250 nanosecond.
CTS1R-N	A19	22	Clock pulse "S1".	

The memory cycle request must occur at "SO" clock time. The read left and right byte micro-operations (MUUYA-N and MUUZA-N) control the strobing of data into the D Register, thus providing for packing of byte data in a single cycle. (Neither MUUYA-N nor MUUZA-N would be pulsed for a full 16 bit word write operation). If either byte is to be read from memory, the Data (D) Register clear (MUZDU-N) must be pulsed to clear out previous data. The "SO" and "S1" clocks are provided to syncronize the memory cycle micro-operations with the computer's internal timing requirements.

Timing for memory cycle control is shown in the following timing chart.

Memory Address

The memory address is loaded into the M Register by the following micro-operations:

Signal	Connector	Pin	Description
MUJJA-N	B12	35	Inhibit A to I/O data bus.
MUJOA-N	B13	43	Gate I/O data bus to internal operand bus. 250 nanosecond pulse at SO" clock time.
MUMIA-N	A13	22	Internal function bus to memory address (M) register. 250 nanosecond pulse at "SO" clock time.
JSOA-N	A08	63	Clock pulse "SO". 250 nanosecond pulse provided for timing.

I/O Data Bus Input

The following signals provide an input data path to the processor's internal operand bus.

Signal	Connector	Pin	Name	
JOOA-N	B18	63	Data bit	00
JO1A-N	B18	61		01
JO2A-N	B18	59		02
JO3A-N	B18	57		03
JO4A-N	B18	29		04
JO5A-N	B18	31		05
JO6A-N	B18	27		06
JO7A-N	B18	25		07
JO8A-n	A08	12		08

MEMORY CYCLE 1μsec

JSOA-N

CTSIR-N

JRID-N

CTDLS-P

MUMCA-N

MUUYA-N, MUUZA-N

MUZDU-N

MUJ0A-N

MUMIA-N

MUJJA-N

MUD0A-N

CTS3R-N

CTCBR-N

MUJJA-N

MUJ0A-N

MUDIA-N

JL03-P

J09A-N	A08	10	09	These pins are
J10A-N	A08	08	10	likely to change
J11A-N	A08	06	11	depending upon I/O
J12A-N	A08	20	12	controllers installed.
J13A-N	A08	18	13	
J14A-N	A08	16	14	
J15A-N	A08	14	15	

To use the I/O Data Bus the following micro-operation must inhibit the normal gating of the processor's A Register:

MUJJA-N	B12	35	Inibit A gated to I/O data bus. A pulse held for the duration of the data transfer.

Function Bus Input

An alternate data input path is provided via the computer function bus. Data must be gated into the function bus only for that clock period during which the data is transferred.

Signal	Connector	Pin	Name	
MB00A-N	B16	09	Data Bit	00
MB01A-N	A16	10		01
MB02A-N	B16	61		02
MB03A-N	B16	27		03
MB04A-N	B16	28		04
MB05A-N	A16	12		05
MB06A-N	A16	31		06
MB07A-N	A16	67		07
MB08A-N	B16	05		08
MB09A-N	A16	14		09
MB10A-N	A16	63		10
MB11A-N	A16	48		11
MB12A-N	A16	46		12
MB13A-N	A16	41		13
MB14A-N	A16	34		14
MB15A-N	A16	36		15

Byte packing must be performed externally if this datapath is used.

Function Bus Output

Data may be output from the computer function bus via the following signals:

CF00A-P	A11	32	Data Bit	00
CF01A-P	A11	30		01
CF02A-P	A11	18		02
CF03A-P	A11	28		03
CF04A-P	A11	54		04
CF05A-P	A11	52		05
CF06A-P	A11	48		06
CF07A-P	A11	50		07
CF08A-P	B11	26		08

CF09A-P	B11	24		09
CF10A-P	B11	20		10
CF11A-P	B11	22		11
CF12A-P	B11	56		12
CF13A-P	B11	54		13
CF14A-P	B11	48		14
CF15A-P	B11	52		15

D Register Output

Data read from memory may be read directly from the D Register via the following signals:

CD00R-N	B18	51	Data Bit	00
CD01R-N	B18	49		01
CD02R-N	B18	41		02
CD03R-N	B18	36		03
CD04R-N	B18	18		04
CD05R-N	B18	16		05
CD06R-N	B18	07		06
CD07R-N	B18	06		07
CD08R-N	A18	60		08
CD09R-N	A18	57		09
CD10R-N	A18	49		10
CD11R-N	A18	47		11
CD12R-N	A18	28		12
CD13R-N	A18	24		13
CD14R-N	A18	15		14
CD15R-N	B13	11		15

This data path is to be used only if an earlier access is desired.

Writing Data In Memory

Data to be written into memory must first be transferred into the processor's D Register.

Via the I/O data bus:

MUJJA-N	B12	35	Inhibit A to I/O data bus
MUJOA-N	B13	43	Gate I/O data bus to operand bus
MUDIA-N	B14	47	Gate function bus to D register
CTS1R-N	A19	22	Clock pulse. 250 nanosecond pulse provided for timing.

The D Register must be loaded at the computer clock CTS1R-N, which is a 250 nanosecond clock pulse following a memory cycle request at "S0". The D Register may not be disturbed until the next "S1" clock.

Via the function bus:

MUDIA-N	B14	47	Gate function bus to D
CTS1R-N	A19	22	"S1" clock pulse

Writing Bytes Into Memory

Byte packing may be performed during a write operation if data is input via the I/O data bus. Two micro-operations are provided to enable "right byte to left" or "right byte to right".

MURLA-N	B14	03	Right to left	Bits 8-15 of operand bus go to bits 0-7 of function bus.
MULLA-N	B14	56	Right to right	Bits 8-15 of operand bus go to bits 8-15 of function bus.

These micro-operations are 250 nanosecond pulses occurring at "S1" clock concurrent with a transfer into the D Register.

If data is input via the function bus, the bytes must be positioned prior to transfer into the D Register and the unused byte position zeroed out. A full 16-bit transfer will occur. Because read strobe timing occurs after the data transfer into the D Register, the unused byte will be read and restored without change.

Reading Data From Memory

After a memory cycle request at "S0" the data is available in the D Register at "S3". Transfer from the D Register can be via the function bus output or directly from the D Register.

Via the Function Bus:

Signal	Connector	Pin	Name	Description
MUDOA-N	B13	16	Gate D register to function bus. 250 nanosecond pulse at CTS3R-N clock time.
CTS3R-N	A15	39	Clock pulse "S3". 250 nanoseconds provided for timing.
CTCBR-N	A11	34	Clock pulse "CB". 100 nanoseconds provided for data sampling.

The data may be sampled no sooner than the "CB" clock pulse which occurs near the trailing edge of "S3".

Directly From the D Register

Data may be sampled as early as the leading edge of "S3" if desired.

Reading Bytes from Memory

Unpacking of byte data must be performed by the Memory Interleave Channel. The full 16-bit word must be read each memory cycle.

Split Memory Cycle

No provisions are made for read-modify-restore. Two full memory cycles must be executed for each address or data word that is to be read and modified.

Incrementing A Non-Stored Memory Address

The memory address is most easily incremented externally. The incremented address may be entered into the M Register no sooner than the "S0" clock of the next memory cycle.

General Reset

The following signal is provided for resetting control flip flops on power up, or when I/O Reset is depressed on the Computer Control panel.

JGRI-N	A08	60	I/O Reset

Incrementing A Stored Address

If the memory address is stored in memory it may be conveniently read, incremented by passing it through the processor's internal parallel adder, and rewritten into memory. The following micro-operations control the operation:

MUDOA-N	B13	16	D to operand bus
MUWIA-N	A13	59	Function bus to W
MUSSA-N	B14	57	Add W and operand bus
MUETA-N	A14	41	Carry-in to adder
MUDIA-N	B14	47	Function bus to D
CTS3R-N	A15	39	"S3" clock. 250 nanoseconds
CT01S-P	B13	40	"S01" clock. 500 nanoseconds
CTS1R-N	A19	22	"S1" clock. 250 nanoseconds

The D Register's content is transferred to the W Register after being read from memory on "S3". An addition is performed with micro-operations MUETA-N and MUSSA-N. The "W+1" is transferred back to the D Register with MUDIA-N, in time to be rewritten on the next memory cycle. Both MUSSA-N and MUETA-N should be 500 nanosecond pulses on the "S01" clock. The W Register will still contain the address before being incremented and on the third memory cycle it may be transferred into the M Register for accessing the data word.

MUWOA-N	A13	25	W to operand bus
MUMIA-N	A13	22	Function bus to M
JS0A-N	A08	63	"S0" clock

In the above sequence the three memory cycles are as follows:

1. Access a fixed location for memory address
2. Increment memory address and rewrite
3. Access data word

This is shown in the following timing chart.

Setting Program Priority Level

A program priority level (interrupt) may be set to notify the program that a full block of data has been input or output. Three levels supplied in a basic machine may be used for this function. The input signals are:

JL01-P	A11	08	Program level 1
JL02-P	A11	18	Program level 2
JL03-P	A11	36	Program level 3
CT23S-P	B14	04	Clock "S23". A 500 nanosecond pulse provided for timing.

MEM CYCLES (1) ◄──►◄ (2) ►◄─►◄ (3) ►

JSOA-N

CTS1R-N

CTO15-P

MUMCA-N

MUUYA-N, MUUZA-N

MUZDU-N

MUD0A-N

MUWIA-N

MUSSA-N

MUETA-N

MUDIA-N

CTS3R-N

MUW0A-N

MUMIA-N
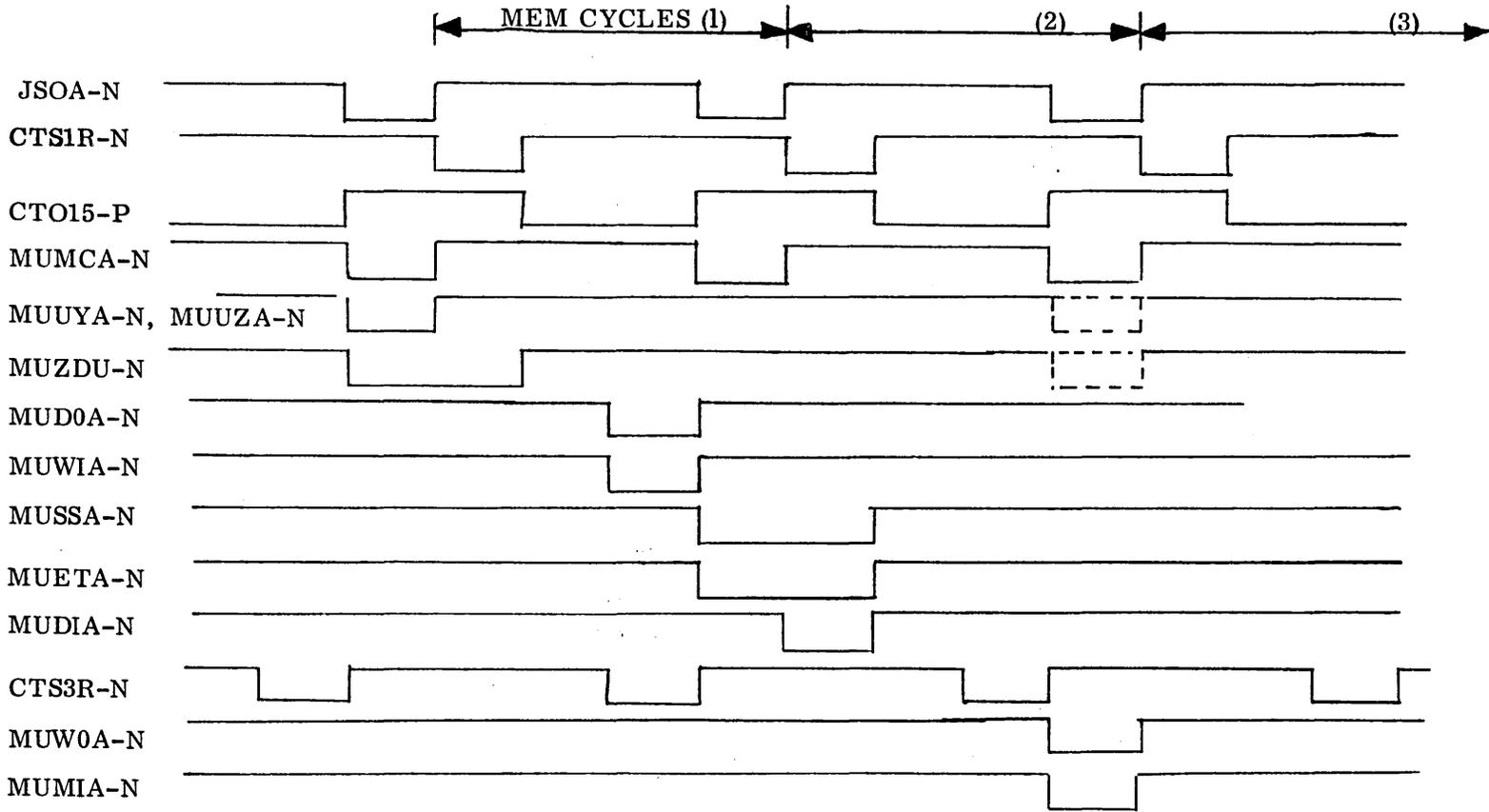
INCREMENTING A STORED ADDRESS

Any pulse setting a program priority level should be at least 500 nanoseconds in width. A convenient time to set it may be on the "S23" clock of the last memory cycle. The computer will execute at least one more instruction before acting on the interrupt. (Note: The driving source for setting a priority level should be a 7400, or equivalent).

Simultaneous Buffers and a Single Level

The Memory Interleave Channel may be designed to work with as many input or output devices as is practical. In fact, if the data rates are slow enough the channel may be buffering data to more than one device in simultanious operation. In the case of simultaneous buffers it is the responsibility of the Memory Interleave Channel to monitor memory addresses, block lengths, and other control information. The addresses and control words for the various devices in operation maybe stored in memory but the channel must remember the fixed locations in order to have access when a memory cycle is required. When a particular buffer is finished (block length counted down to zero) the channel may set an individual priority level assigned to that buffer. This would require a priority level assigned to each active buffer. Enough levels of program priority may not be available in some systems. The MAC 16 has provisions for allowing more than one device to send interrupts over a single priority level.

A description of how this is possible is contained in the I/O Interface Manual. But generally, the various devices must have their interrupt requests daisy chained in such a manner that any ambiguity is removed as far as the program is concerned. The Memory Interleave Channel may take on characteristics of an I/O device itself, communicating with the program through the PDC. The program may execute an EAI instruction, for example, to find out which device had just completed its buffer. Or the channel may assemble a word indicating the present status of active and inactive buffers.

PROGRAMMED DATA CHANNEL, PDC

I. GENERAL

A. The primary communication path between the MAC-16 and its peripheral equipment
is through the Programmed Data Channel (PDC). The PDC exists as part of the basic
CPU although portions (such as line drivers and receivers) are not added until certain
hardware options are selected. By definition the PDC consists of all necessary hardware
and control to present a standard interface to a peripheral device. A device with a PDC
interface may communicate (1) through the A Register in the CPU (basic), (2) directly with
memory via the MDC (optional), or (3) with a satellite buffering controller (theoretical)
which in turn might communicate as in (1) or (2). The primary intention of this specifi-
cation is to fix the PDC interface in a general manner without going into the discussion
as to how to manipulate data through the A Register of the CPU, in this sense becoming
a hardware specification rather than one for software. For the specifics of how each
peripheral device should be programmed, see the appropriate description for that particu-
lar device controller.

B. The PDC is capable of two levels of hardware interface, the (1) "common-collector"
level, and (2) the "driver-receiver" level. The basic CPU contains the common-collector
level which passes data through the A register. Up to 5 device controllers may be
selected as options to communicate with the basic CPU without the requirement for line
drivers and receivers. The actual number of peripheral device controllers is limited,
of course, by the space available in the mainframe. To add additional device controllers,
a set of line drivers and receivers are added to the basic CPU and to each new chassis of
controllers, each of which in turn may contain up to 6 controllers at the common-collector
level as space permits. The line driver-receiver interface is capable of communicating
with up to 10 external chassis; therefore, the maximum number of device controllers in
a fully expanded Programmed Data Channel is 65, due to loading considerations. (Up to
255 unique device addresses are allowable if some device controllers can control more
than one device). Cable length and propagation delay are other factors which may limit
the maximum MAC-16 I/O system on the PDC. The block diagram of an expanded PDC
is shown on page 2.

NOTE: For additional information on the PDC refer to the MAC 16 Interface Reference
Manual.

Programmed Data Channel.
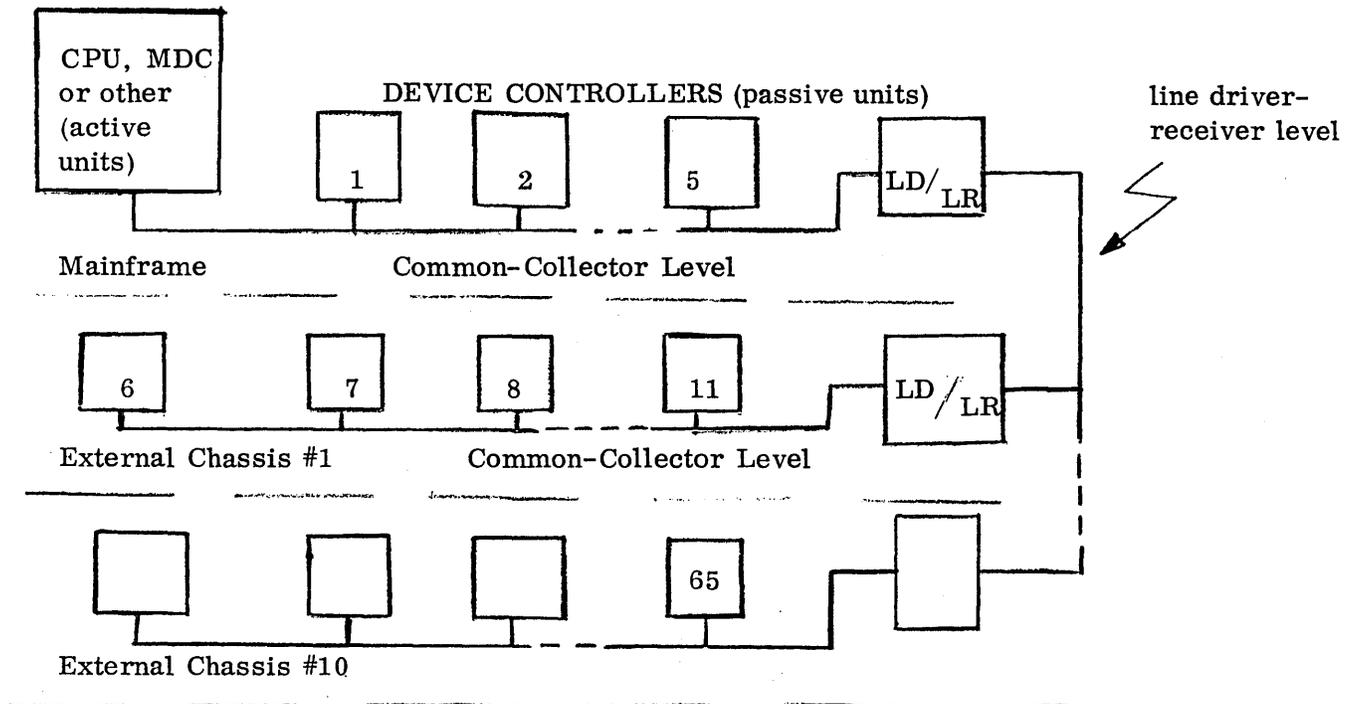
II. Hardware Interface at "Common-Collector" Level

A. Mnemonics

J00N-N,..., J15N-N (16) Data (input or output), bidirectional, negative polarity

J08M-N,..., J15M-N (8) Device Address, output, negative polarity

JL01-P,..., JL63-P (63) Service Requests, input, positive polarity

JEDI-N (1) External Data In, output, negative polarity

JEDØ-N (1) External Data Out, output, negative polarity

JESI-N (1) External Status In, output, negative polarity

JECØ-N (1) External Command Out, output, negative polarity

JEAI-N (1) External Address In, output, negative polarity

JSTR-N (1) Strobe, output, negative polarity

JS0A-N (1) Clock S0, output, negative polarity

JACK-N (1) Acknowledge, input, negative polarity

JGRI-N (1) I/O Reset, output, negative polarity

B. Circuits

All circuits at the "common-collector" level are TTL (TI 7400 series), or equivalent. Power gates are used on those signals that require only a single driving source, and common collector gates where more than one source is possible. A maximum of 7 tied collectors is permitted, or 1 line receiver and 6 tied collectors. Each output signal may drive 7 TTL input loads or 1 line driver and 6 TTL loads maximum.

D.   Rise and Fall Times (overall spec)

At the "common-collector" interface the signal rise and fall times must fall outside the minimum and inside the maximum specified time as measured at the 10-90% points.

For t min. specified:
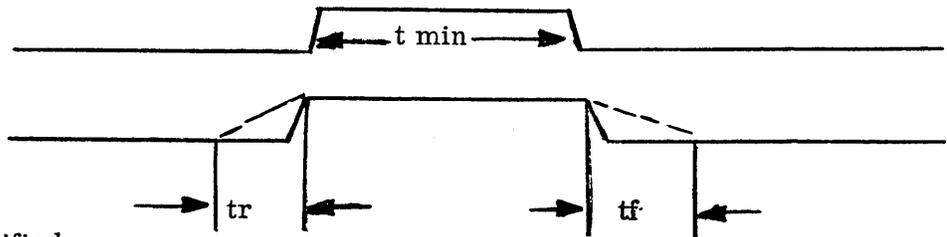
For t max. specified:
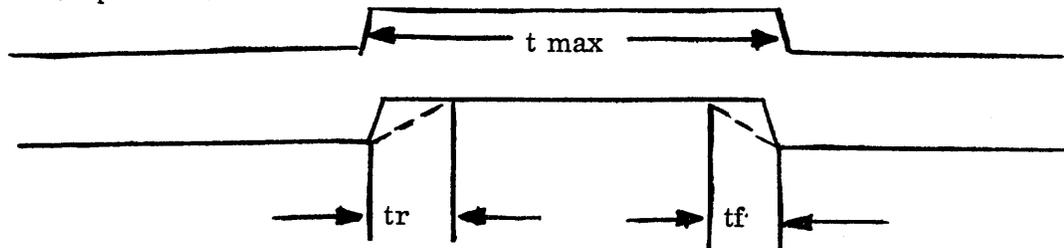
III.   Hardware Interface at "Driver-Receiver" Level

See MAC 16 Interface Manual.

IV.   Theory of Operation.

A.   Control Signals JEDI, JEDØ, JESI, JECØ.

The operation of Data In, Data Out, Status In, and Command Out are all similar in timing. Each of the four control signals calls for the transfer of a full 16-bit word to or from the device controller over the bidirectional data bus. To cover differential delays due to propagation and logic, each of the control signals is followed 500 nsec later by a strobe, JSTR, which the device controller must use for the gating of data. Only one control signal will be active at any one time and its duration will be 2 μsec, typically.

Control signal
(JEDI, JEDØ, JESI, or JECØ)

Strobe (JSTR)

250 nsec

500 nsec

2μsec
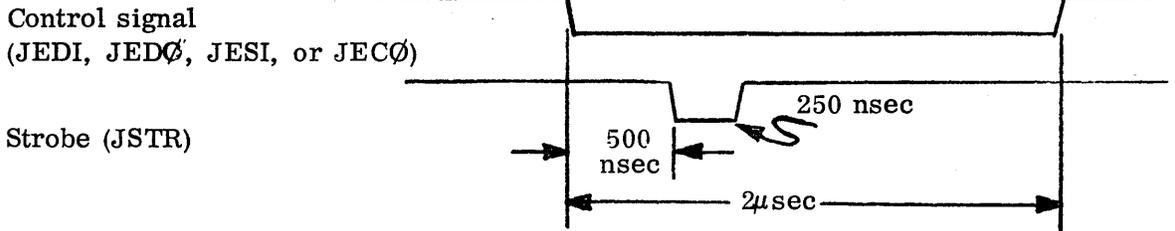
The width of the strobe will be 250 nsec. (Note: In this, and in all following discussions signal timing is specified with respect to the internal clock of the active unit, the CPU, MDC, or other. Delays due to logic and propagation will vary according to system configuration, and must not exceed the minimum time requirements where specified).

B. Device Address

J08M-N most significant ⎫
J09M-N ⎪
J10M-N ⎬ M field
J11M-N ⎭

J12N-N ⎫
J13N-N ⎪
J14N-N ⎬ N field
J15N-N least significant ⎭
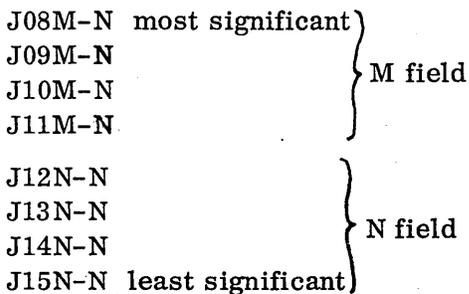
Device address is gated to the PDC in conjunction with the four (4) control signals, JEDI, JEDØ, JECØ, JESI, providing a unique address for each device controller. Each device controller must decode the address and respond no sooner than the leading edge of Strobe if it is to be selected. Typically 500 nsec is allowed for differential delays due to propagation and decode before Strobe occurs.

Device Address
(J08M...J15M)

Strobe (JSTR)

500 nsec

Control Signal
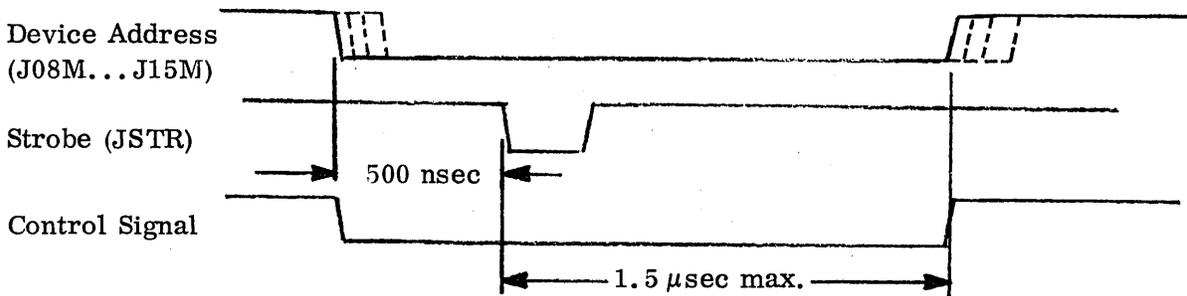
1.5 μsec max.

After the leading edge of Strobe, the Device Address lines will remain static as long as one of the four (4) control lines is active (1.5 μsec max).

Because the Device Address lines may follow the M & N fields of the CPU Instruction Register, or be in transition at some unknown time, logic decisions based on the decoding of the address is prohibited outside the interval between Strobe and the trailing edge of a control line.

C.   Acknowledge,JACK,with JEDØ, JEDI, JECØ.

    Response of the device controller is detected by the active unit over the input signal line JACK.   To the CPU, MDC, or other,the JACK response means the data word transfer has been successful.   The absence of a JACK response could mean either of two things, depending on the particular device: either that (1) the word transfer was not successful due to a system failure of some sort, or (2) the end of a fixed record length has been reached (as when inputting a record of unknown length from magnetic tape).

It is a requirement of the device controller that it respond with JACK for the three control signals JEDØ, JEDI and JECØ.   Specifically, the JACK response carries the following meanings: (1) for JEDI.   The input data word has been placed on the bidirectional data bus and may be sampled. (2) for JEDØ.   The output data word has been sampled by the device controller. (3) for JECØ.   The output command word has been sampled by the device controller.   (The active unit will not attempt to output the command again).

Normally, the selected device controller can use the strobe JSTR to generate the JACK response, but if unusual differential delays of input data are possible, JACK should be delayed accordingly.   If JACK is delayed more than 1.5 μsec after the leading edge of JSTR, the active unit will assume it was missing and not sample the data bus if inputting.   The width of JACK may be from 50 to 500 nsec.

Control Signal
(JEDI, JEDØ, or JECØ)

Strobe (JSTR)

Acknowledge (JACK)

1.5 μsec max
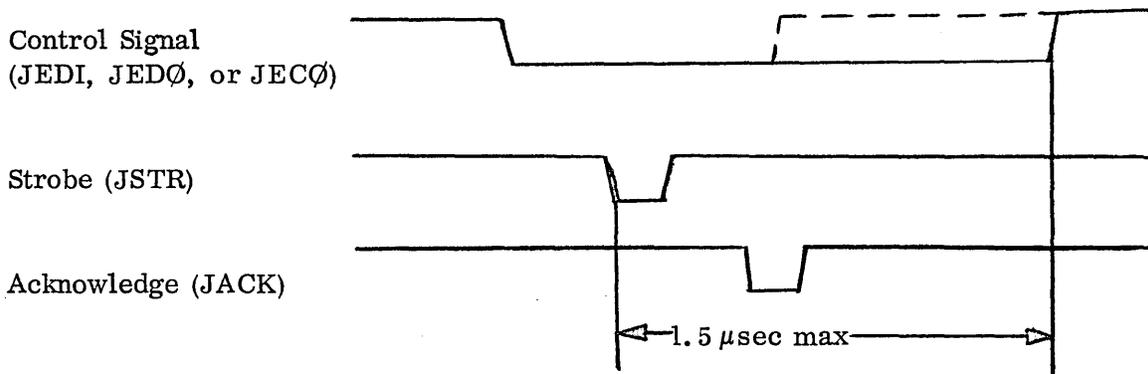
To achieve the highest data rate possible over the PDC, the active unit may use the JACK response to disable the control signal (and likewise disable device address and data); therefore, the device controller should not assume validity of data or address after the trailing edge of the control signal.

D.   Input Data or Status, JEDI, JESI

    When inputting, the active unit will sample the bidirectional data bus into a register no later than 25 nsec before the trailing edge of the control signal.

Control Signal (JEDI, JESI)

Strobe (JSTR)

Data (J00N–J15N)

Data sample (in-active unit)

25 nsec
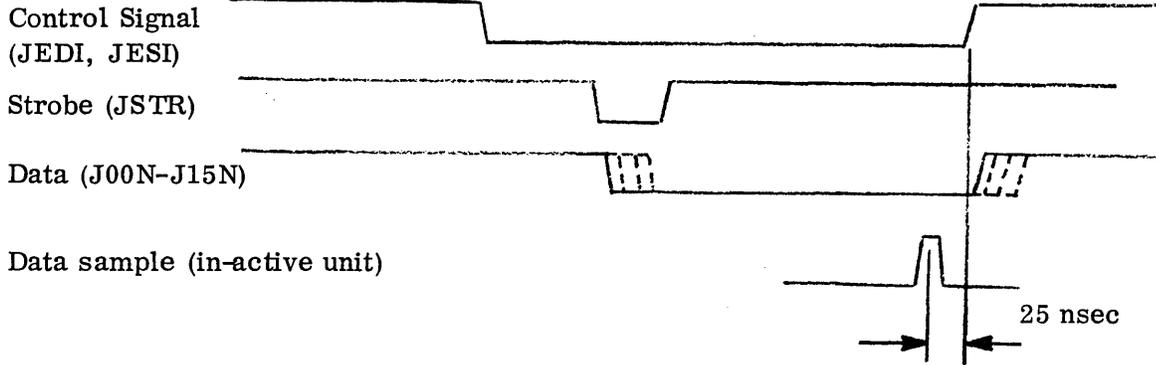
The selected device controller should enable the gating of data or status to the bus at the leading edge of Strobe JSTR, and disable it at the trailing edge of the control signal JEDI or JESI.

Any delay in the enable of data should be reflected in the acknowledge response JACK. Delay in the enable of status will be undetected by the active unit.

E. Output Data or Command, JEDØ, JECØ

When outputting, the active unit will enable data or command to the bus concurrent with the device address and hold it static until the trailing edge of the control signal. The selected device should sample the data bus into a register on the leading edge of Strobe, JSTR.

Control Signal (JEDØ, JECØ)

Strobe (JSTR)

Data (J00N–J15N)

Data Sample (in device controller)
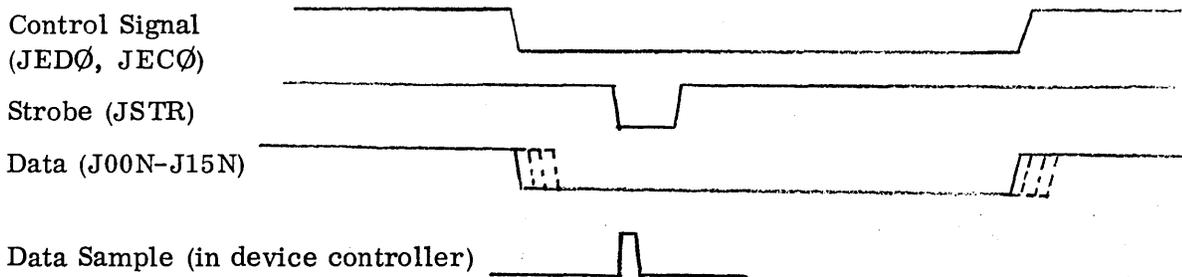
Any necessary delay in the data sample should be reflected in the acknowledge response JACK.

F. Service Requests JL01,...,JL63

Service requests when honored by the CPU become interrupts to a new program level. Normally, the CPU would then service the device controller with a data transfer. Service requests to the MDC or some other active unit should cause the same interface response, although an interrupt in the CPU may not occur.

Service requests are asynchronously occurring pulses or levels which are graded accordingly to priority by the active unit. Higher numbered service requests have higher priority. At the "common collector" interface, service requests are the only signals with positive polarity. Service request JL00 does not exist on the PDC.

Programmed Data Channel

Minimum pulse width

Service Request

JL01,..., JL63
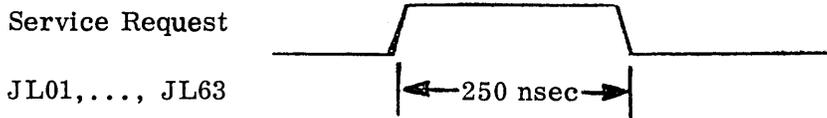
|←—250 nsec—→|

For maximum request rate the service request shall fall and rise again within
750 nsec after the leading edge of the "selected" strobe. * Minimum down time
is 50 nsec.

Strobe (JSTR)

Service Request

50 nsec
min.

(New Service Request)

750 nsec
max. for highest data rate
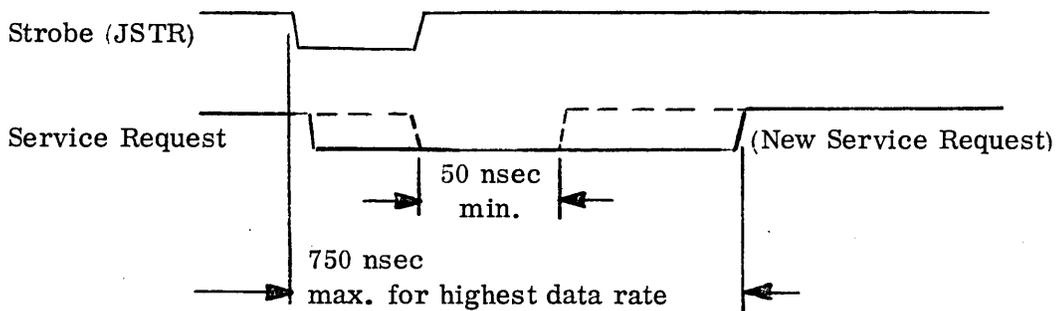
* The "selected" strobe is determined by device controller address at the time
a control signal is active.

For slower devices the trailing edge delay of an old service request shall be no more
than 1.75 μ sec after the leading edge of the selected strobe.

Strobe (JSTR)

Service Request

——1.75 μsec max ——→
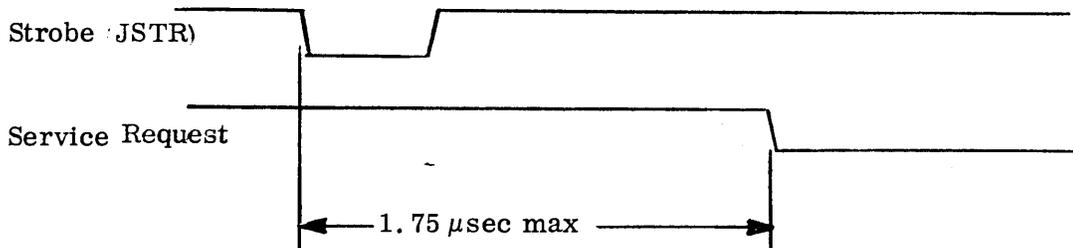
G. Shared Interrupt Level, JEAI.

A single Interrupt Level may be shared among device controllers by cascading (or
daisy chaining) each service request from controller to controller. Logic must be associated
with the service request at each stage (i.e., in each device controller) to prevent a request
conflict (in the event that more than one controller attempt service requests simultaneously).
The logic requirement is as follows:

No device controller may raise its service request signal later than the last clock
(JS0A) preceding a JEAI, nor earlier than the first JS0A following a JEAI.

JSOA

JEAI

Service Request   (latest preceding JEAI)

Service Request   (earliest following JEAI)

|← 3.75 μsec →|
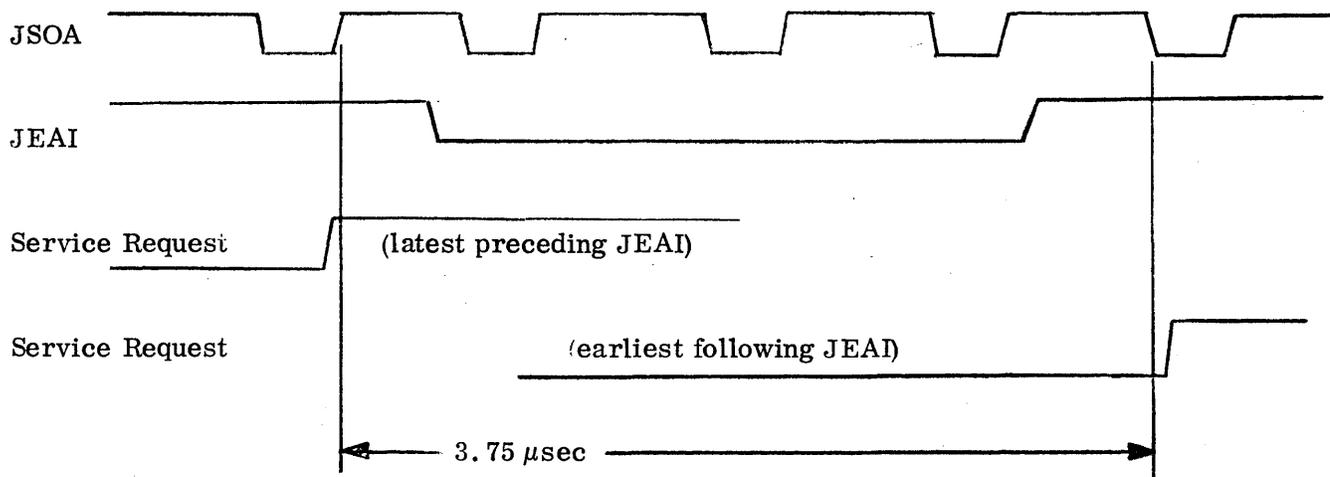
Service Request lock-out will not exceed 3.75 μsec maximum.

(Note : The primary purpose of the clock pulse JSOA is to prevent new service requests from occurring during JEAI. The clock may be used in the device controller for other tasks, however; but control signals other than JEAI may vary in time with respect to it. The width of JSOA is 250 nsec.)

Priority of device controllers on a single shared interrupt level must be handled logically in each device controller. Each device controller is required to gate the service request from a higher priority device on to the next lower priority device until the interrupt request level interface at the CPU is reached. The device with the highest priority, then, is logically the farthest away. No device with a pending service request may respond to a JEAI (and Strobe) if a device of higher priority has its service request high.

The maximum propagation delay of a service request from the highest priority device to the lowest priority device on a single shared interrupt level shall be no more than 1 μsec maximum. If no device controller of a higher priority has a service request high, a lower priority device may respond to a JEAI if its own service request is high. The device is required to gate its unique device address onto the bidirectional data bus in bit positions 08-15. The timing is similar to that for JEDI and JESI, although the active unit will ignore any acknowledge response, JACK. The device address is sampled by the active unit 1.5 μsec after the leading edge of Strobe, JSTR, and the gating of address to data bus is to be disabled after the trailing edge of JEAI.

Address In (JEAI)

Strobe (JSTR)

Address (Data bus)

Address sample (in active unit)

|← 1.5 μsec →|
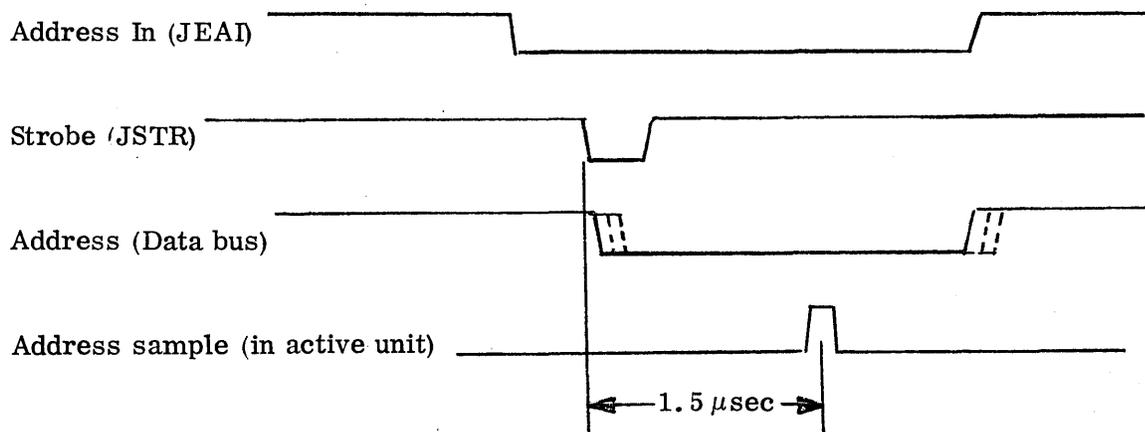
H.   I/O Reset, JGRI.

Device controllers may be reset from the CPU control panel via the signal JGRI.
An automatic reset will occur when power is turned on at the CPU.   The function of reset
is to prevent run-away conditions in the peripheral devices and to perform initial set-up
of control logic where required.   The signal is a DC level which follows the action of the
control panel switch.

SECTION II

MAC 16 MEMORY OPTIONS

MAC 16 MEMORY OPTIONS

MEMORY OPTIONS

Memory options separate into two parts. One part contains those options that modify the computer chassis. The other part contains options that are located in the memory expansion chassis.

<u>Computer Chassis Memory Options</u>

These options include:
      Computer Chassis Memory 0K, 4K or 8K
      Memory Expansion Capability
      Direct Memory Access
      Memory Parity
      Memory Protect

Computer Chassis Memory -0, -4, -8

The basic MAC 16 contains a 4K x 16 memory. As an option, a second 4K x 16 memory may be added to the computer chassis. It is also possible to order a MAC 16 without memory in the main-frame, but this system must include the Memory Expansion Capability and an external memory.

Memory Expansion Capability -X

This option includes the modifications to the computer chassis that allow connection to an external memory. It includes the provision of memory interface drive and receive gates, modification to memory bank select logic, and external cable connectors that are wired-in to connect to the external memory.

Direct Memory Access (DMA) -D

The memory interface lines are made available to a second memory controller device at a set of external connectors. The computer's timing logic is modified to allow a second memory controller access to memory within one memory cycle. The computer is temporarily halted during this operation.

In the standard configurations all of the system's memory is connected to the DMA.

Memory Parity -P

The memory parity option in the computer chassis requires replacement of each basic 4K x 16 memory with a 4K x 18 memory. It also includes the provision of parity generate and check logic. An odd parity bit is generated and checked on each eight bit byte of the 16 bit word.

Memory parity is also a Memory Expansion chassis option. If parity is required it must be provided on all of the system's memory.

When a parity error is detected a signal is generated that can be assigned an interrupt level. Parity errors may be detected on any memory read cycle. If the parity error occurs on an instruction read cycle, the instruction is executed anyway.

Memory Protect -T

This option provides the ability to set any memory module into a read-regenerate mode only. It is a Computer Chassis option as well as a Memory Expansion Chassis option. Each memory module, 4K or two 4K's in the computer chassis or external memory modules may be individually protected from modification. A memory module is protected if its protect line is "on".

Protection from clear-write cycles on the first 4K of memory (addresses 0000 to 4095) does not include the first 256 words (Executive Space) of memory. This is independent of whether or not the main-frame contains memory modules. Protection of external memories is in 4K increments even though external memories are 8K stacks.

A set of 16 memory protect lines may be provided for the maximum memory size of 65K. Two of these lines connect to the main-frame and each Memory Expansion Chassis contains six lines for its maximum 24K memory.

Whenever a write operation is attempted into a protected memory a protect error signal is generated for that memory bank.

Control of memory protect lines may be manual or under program control.

A special chassis that contains 16 lamps (a power supply) and 16 switches can be provided for manual control. The switches can be wired to set memory protect signals "on" and the lamps can be used to indicate the memory bank when a protect error occurs.

(Note: This special chassis also has utility when used with the external input and output channel options).

Program control of memory protect may be provided via the External Output Channel, -X0, and External Input Channel, -XI. Flip flops of the output channel may be assigned to control memory bank protection. Flip flops of the input channel may be used to indicate the memory bank that was protected when a write operation was attempted.

Memory Option Cards

Main-frame memory options are provided with the addition of five new PC cards: FIO, TND, YCD, DMA and DMD.

FIO - This card contains logic for fan-out and fan-in of the external memory interface. It also includes parity logic. Two assemblies of this card are available. One assembly (FIO-1) contains both fan-in-out logic and parity check and generate logic. The assembly (FIO-2) contains fan-in-out logic only. The FIO card is wired into slot 20 when the parity option is specified or when memory expansion to the Memory Expansion Chassis is specified without the Direct Memory Access option.

TND - This card contains the basic timing for the processor and also provides for the Direct Memory Access (DMA) option and the Memory Protect Option. This card replaces the basic TAD card in slot 19 whenever memory expansion over 8K without DMA or DMA is specified. It is also required when Memory Protect is included.

At present, this card has only one assembly.

YCD - This card contains two sets of Y select drivers for the computer chassis memory module. It must be used when the TND card is used and the computer contains 4K or 8K of memory. It occupies slot 30 and has one assembly so that field expansion from 4K to 8K does not require a different assembly.

DMA and DMD - These two cards provide the Direct Memory Access option. They also provide fan-in-out logic for external memory. The DMA, DMD cards occupy slots 21 and 23, thereby replacing the first 4K (SAD and HAD) memory cards. It is not possible to have more than 4K of memory in the computer chassis with the DMA option.

The DMA card contains address switching logic; the DMD card contains data switching logic for 16 bits only. A second assembly of the DMD card called DMP also contains parity logic when both DMA and parity options are selected.

These computer chassis memory option cards, along with basic memory cards: SAD, HAD, and TAD occupy slots 19, 20, 21, 23, 27, 28 and 30 to provide thirty-two combinations of memory options. This is shown in Table 1.

TABLE 1. COMPUTER CHASSIS MEMORY OPTIONS

0K IN MAIN-FRAME	4K IN MAIN-FRAME	8K IN MAIN-FRAME	MEM EXPANSION CAPABILITY	DIRECT MEMORY ACCESS	MEMORY PARITY	MEMORY PROTECT	DESIG-NATOR	19	20	21	23	27	28	30	Wire List
	4						-4	TAD-4	-	HAD-16	SAD-16	-	-	-	Basic
		8					-8	TAD-4	-	HAD-16	SAD-16	SAD-16	HAD-16	TAD-8	1
	4				P		-4P	TAD-4	FIO-1	HAD-18	SAD-18	-	-	-	2
		8			P		-8P	TAD-4	FIO-1	HAD-18	SAD-18	SAD-18	HAD-18	TAD-8	2
0			X				-0X	TND	FIO-2	-	-	-	-	-	3
	4		X				-4X	TND	FIO-2	HAD-16	SAD-16	-	-	YCD	3
		8	X				-8X	TND	FIO 2	HAD-16	SAD-16	SAD-16	HAD-16	YCD	3
0			X	D			-0XD	TND	-	DMA	DMD	-	-	-	4
	4			D			-4D	TND	-	DMA	DMD	SAD-16	HAD-16	YCD	4
	4		X	D			-4XD	TND	-	DMA	DMD	SAD-16	HAD-16	YCD	4
0			X		P		-0XP	TND	FIO-1	-	-	-	-	-	3
	4		X		P		-4XP	TND	FIO-1	HAD-18	SAD-18	-	-	YCD	3
		8	X		P		-8XP	TND	FIO-1	HAD-18	SAD-18	SAD-18	HAD-18	YCD	3
0			X			-T	-0X-T	TND	FIO-2	-	-	-	-	-	3
	4					-T	-4-T	TND	-	HAD-16	SAD-16	-	-	YCD	3
		8				-T	-8-T	TND	-	HAD-16	SAD-16	SAD-16	HAD 16	YCD	3
	4		X			-T	-4X-T	TND	FIO-2	HAD-16	SAD-16	-	-	YCD	3
		8	X			-T	-8X-T	TND	FIO-2	HAD-16	SAD-16	SAD-16	HAD-16	YCD	3
0			X	D	P		-0XDP	TND		DMA	DMP	-	-	-	4
	4			D	P		-4DP	TND		DMA	DMP	SAD-18	HAD-18	YCD	4
	4		X	D	P		-4XDP	TND		DMA	DMP	SAD-18	HAD-18	YCD	4
0			X		P	-T	-0XP-T	TND	FIO 1	-	-	-	-	-	3
	4				P	-T	-4P-T	TND	FIO-1	HAD-18	SAD-18	-	-	YCD	3
		8			P	-T	-8P-T	TND	FIO-1	HAD-18	SAD-18	SAD-18	HAD-18	YCD	3
	4		X		P	-T	-4XP-T	TND	FIO-1	HAD-18	SAD-18	-	-	YCD	3
		8	X		P	-T	-8XP-T	TND	FIO-1	HAD-18	SAD-18	SAD-18	HAD-18	YCD	3
0			X	D		-T	-0XD-T	TND	-	DMA	DMD	-	-	-	4
	4			D		-T	-4D-T	TND	-	DMA	DMD	SAD-16	HAD-16	YCD	4
	4		X	D		-T	-4XD-T	TND	-	DMA	DMD	SAD-16	HAD-16	YCD	4
	4			D	P	-T	-4DP-T	TND		DMA	DMP	SAD-18	HAD-18	YCD	4
0			X	D	P	-T	-0XDP-T	TND		DMA	DMP	-	-	-	4
	4		X	D	P	-T	-4XDP-T	TND		DMA	DMP	SAD-18	HAD-18	YCD	4

Wire Lists: 1. add 4K wires
2. add 4K and parity wires
3. and 8K, expansion and parity wires
4. remove first 4K, add second 4K, DMA and parity wires

The SAD card contains a 4096 word memory stack. It has two assemblies:

      SAD-16 a 4K x 16 stack
      SAD-18 a 4K x 18 stack

The HAD card contains inhibit drivers. It also has a 16 bit word assembly and an 18 bit word assembly, HAD-16 and HAD-18.

The TAD card contains basic timing circuits and Y select drivers for a 4K stack. It has two assemblies:

      TAD-4 timing and Y select drivers
      TAD-8 Y select drivers only

Wire List Combinations

In order to reduce the number of different wire lists for all combinations of computer chassis memory options and in order to allow memory expansion in the field, sets of memory options are combined and wired into the main-frame.

The following combinatorial rules apply:

1.   Anytime a computer chassis memory option other than expansion to 8K and parity without external memory is specified, the Memory Expansion Capability is wired in.

2.   Anytime a computer chassis memory option is specified, all connectors in slots 19 to 30 are wired for the maximum case and field insertion of memory option cards.

The standard wire lists are as follows:

1.   Expansion to 8K   -8
                                                            Wired for -8

    The basic computer is wired to include a second 4K x 16 stack in slots 27 and 28. A TAD card with Y-select drivers only is wired into slot 30.

                                                   -4P, -8P
2.   Memory Parity in Computer Chassis   Wired for -8P

    The basic 4K x 16 memory is replaced with a 4K x 18 memory. The chassis is wired to include two 4K x 18 memories and an FIO card is wired into slot 20.

                                     -0X, -4X -8X or -0XP, -4XP, -8XP
3.   Memory Expansion Capability without DMA   Wired for -8XP

    If memory expansion to an external memory is required, the computer chassis is wired to include two 4K x 18 memories. A set of external connectors is added to connect to the Memory Expansion Chassis. Slot 20 is wired for an FIO card. A TND card replaces the TAD card, and slot 30 is wired for a YCD card. 4K or 8K of memory may be added to the computer at anytime by inserting a YCD card and SAD's and HAD's.

4. Memory Expansion and Direct Memory Access   -0XD, -4D, -4XD or -0XDP, -4DP, -4XDP
                                                       Wired for -4XDP

Inclusion of the Direct Memory Access option always causes the computer to be wired for
memory expansion. The FIO card is not required. The basic SAD and HAD card connectors
in slots 21 and 23 are rewired for the DMA and DMD cards. Slots 27 and 28 are wired for
a computer chassis 4K x 16 memory. (SAD and HAD).

Memory Protect, -T, is an add on option. An external connector the provides for two protect
lines and two protect error lines is added to the processor chassis. The two sets of lines
control the protect option on the two 4K memories within the processor chassis.

Additional Options

The design of memory option modules has been such as to allow for a number of other options not stated above. It is possible to split memory for operating a portion on DMA and the remainder simultaneously without DMA. It is possible to operate with two DMA's. However, these options are not being offered as standard and their availability is "upon request" requiring Engineering support.

Memory Expansion Options

Memory expansion beyond the maximum 8K that may be provided in the computer chassis is provided by adding one, two or three Memory Expansion Chassis (model designator MEC). Each Memory Expansion Chassis contains up to three 8K x 16 or 8K x 18 CE 100 type memory systems. It is designed to be rack mounted immediately above, below or to the side of the computer chassis. Interconnect cables are provided on the front, wire-wrap side of the chasses.

A second type of external memory chassis is also available. This is the Memory/Controller Chassis (model designator MCC). This chassis can contain up to two 8K x 16 or 8K x 18 memory systems plus nine MAC 16 size logic cards. These cards usually represent device controllers and a line receiver, -LR, is located in slot 1. (This would be designated MCC-8-LR or MCC-16-LR plus other controller options indicated).

Each 8K memory module contains the core stack and the following PC cards:

Name	Function	Quantity
MTM	Memory Timing Module	1
SPM	Switch Pair Module	4
OIM	Output Interface Module	1
DCM	Dual Card Module (Stack Current Source)	1
BCE	Bit Circuit Extender	8
BCP	Byte Control and Protect	1
SSS	System and Stack Select	1

Both external memory chasses are 17-1/2 inches high and contain the fan-pack option, -FP. Each contains a +12 volt power supply.

Memory Expansion Chassis   MEC

This chassis contains two rows of card guides and connectors for insertion of standard CE100 printed circuit cards. These cards are approximately six inches high and seven inches deep. They fit standard MAC 16 72 pin connectors.

This chassis is always wired for three 8K x 16 memory systems. It is wired with external connectors to connect to the MAC 16's memory interface.

External memory interface connectors are provided in pairs so that up to three memory chasses may be "daisy chained". The maximum MAC 16 memory size of 65K may be attained in several combinations. The most straight forward configuration would be with three external memory chasses where two contain 24K and the third contains 16K. Memory expansion over 24K requires an additional power supply.

Each Memory Expansion Chassis contains the ability to define the 4K module address of its memory modules. The most significant four bits of the memory address are encoded to provide six bank select lines. This is selected with jumper wires. The following rules must be followed on bank address selction. The two 4K banks of an 8K module must be consecutively numbered. If a bank is selected as bank 0, addresses 0 to 4095, it must be the first 8K module of the expansion memory. In this case, the computer chassis must not contain any memory. Anytime that the computer chassis contains memory, they are banks 0 and 1 by definition.

Memory Expansion Chassis Options

The Memory Expansion Chassis, MEC has the following options:

        Memory size   MEC-8, MEC-16, MEC-24
        Memory Parity   MEC-8P MEC-16P, MEC-24P
        Memory Protect   MEC-8-T MEC-16-T, MEC-24-T or MEC-8P-T MEC-16P-T,
                MEC-24P-T.

Memory Size   -8, -16, -24

The MEC is always wired for three 8K x 16 memory modules. This allows field expansion to 24K if only 8K or 16K is delivered.

Memory Parity   -8P, -16P, -24P

The parity option requires that the 8K x 16 stacks be replaced with 8K x 18 stacks. It is also required that the computer chassis contain the parity option. The parity check and generate logic is contained on the FIO card of the computer.

Memory Protect - T

The memory protect option on the external memory adds an external connector for six memory protect wires and six memory protect error wires. This allows a protect option on any 4K bank of addresses of the maximum 24K memory.

Logic in the MEC will not allow a clear-write cycle to occur in a 4K bank if its protect line is "on". If this is attempted, logic will generate a memory protect error on the corresponding error line. These protect lines and error lines may be handled manually or under program control as in the computer chassis memory protect option.

If one of the 4K external memory banks is wired to be bank zero, addresses 0000 to 4095, then the first 256 words of this bank are not protected.

Memory/Controller Chassis   MCC

This chassis contains two rows of card guides and connectors for up to two 8K, CE100 memory systems and room for nine MAC 16 PC cards.

It is always wired for 16K of memory. It is connected in the system similar to the Memory Expansion Chassis described above.

Memory/Controller Chassis Options

The Memory/Controller Chassis, MCC has the following options:

    Memory Size MCC-8, MCC-16

    Memory Parity MCC-8P, MCC-16P

    Memory Protect MCC-8-T, MCC-16-T, or MCC-8P-T, MCC-16P-T

    Line (Cable) Receiver   -LR (-GR)

    Line (Cable) Driver   -LD (-GD)

    Device Controllers:

        High Speed Paper Tape -HC
        Teletype Controller - TC
        Drum Controller -DM
        Card Reader Controller -CR
        Line Printer Controller -LP
        Mag Tape Controller -M9
        Data Modems -YM, -YS
        External In Channel -XI
        External Out Channel -X0
        Others to be specified

Memory Size -8, -16

The MCC is always wired for 16K. This allows field expansion if only 8K is delivered.

Memory Parity -8P, -16P

Same as for the MEC.

Memory Protect - T

Four memory protect and four protect error lines are provided. Otherwise, this option is as described for the MEC.

Device Controller Options

The MCC may be wired to contain several device controllers. Location of a device controller is the same slot positions in MCC as it is in the computer chassis.
"Device Controller Options and Peripheral Devices".

DMA/CONTROLLER INTERFACE

Direct Memory Access/Controller Interface Description

I.   General Description

The DMA option requires two boards, one for control and address switching, the other for data switching. Registers for storage of memory address and data input by the peripheral are provided in the DMA logic, which permits high data transfer rates.

The basic DMA consists of a 2-port switch implemented on the two (2) boards. A third DMA entry port can be added to the switch by adding a second data switching board, identical to the first. The control and address switching board contains the control logic required to handle two peripherals and the CPU.

II.   Operating Modes

Two (2) modes of operation are available to the peripheral controller. One is a high speed, or "burst" mode, the other, a fully interlocked mode. In the former, the controller must supply updated access request and address to the DMA within $3/4\,\mu$sec of generation of the Acknowledge signal by the DMA. Data, if being input, may arrive slightly (about 250 nanoseconds) later. The Acknowledge signal is returned to the controller after the DMA has stored the address and begun the memory cycle. The Acknowledge signal does not mean that the input data, if any, has been stored. Transfer of data will be described later. The $3/4\,\mu$sec includes transmission time in each direction, and reaction time of the controller. If the timing restriction is met, cycles at 10^6 per second can be achieved.

In the interlock mode, no restriction is placed upon the delay between receipt of Acknowledge and dropping of Request by the peripheral controller. An interlock in the DMA prevents more than one reaction to the Request. The DMA holds the Acknowledge signal high until the controller drops its Request line. The Acknowledge signal is then dropped, and the controller may then initiate another cycle by raising the Request line when the address lines are stable.

III. Control Signals Between Controller and DMA

The various control signals are listed in the order in which they would normally become enabled.

A.   Request - Controller to DMA

The Request signal indicates to the DMA that the controller wishes to access memory, and has put the memory address on the 16 address lines. The DMA services Requests from controller #2 only if controller #1 is not requesting access. The CPU is serviced only if no controller is on request.

2-14

The Request signal is answered by an Acknowledge signal from the DMA, signifying that a memory operation has begun. The Request signal may then be operated in one of two ways, depending upon whether the controller is using "burst", or interlock, mode.

If in burst mode, the controller need not drop the Request line if another cycle is desired. It must, however, ensure that the next memory address is at the DMA within 3/4 μsec of the time when the DMA originated the Acknowledge. Thus, the controller has 3/4 μsec - 2 transmission delays to react to the Acknowledge. If it desires no further access, it must drop its Request immediately, so that the DMA sees no Request at 3/4 μsec after Acknowledge.

If the interlock mode is in force, the controller may leave the Request line high after seeing Acknowledge - no repeated cycles will result from it. After it drops the Request, the Acknowledge will be dropped, thus informing the controller that the end of Request has been seen. The controller may then raise Request again.

If a single controller is on the DMA, and if it drops its Request within 1/4 μsec upon seeing Acknowledge, it can access memory at 500KC. If two controllers are on the DMA, they may operate in an interlaced manner, effectively monopolizing the memory.

B.   Acknowledge - DMA to Controller

Immediately (60 nanoseconds) after the DMA has stored the address from, and just as it initiates a memory cycle for, a controller, it sends the Acknowledge signal to the controller. The signal does not mean that the DMA has stored input data, if a Write operation is indicated. However, the address lines need not be maintained after Acknowledge.

In the burst mode, the Acknowledge signal is maintained for 350 nanoseconds, then is dropped.

In the interlock mode, the Acknowledge signal is maintained until the DMA has seen the end of the Request signal, at which time, it also drops. The controller may then request another cycle.

Since four (4) transmission delays occur in exchanging control signals, the cycle rates possible in interlock mode are impossible to guarantee. However, 1/4 μsec per exchange and 1/4 μsec reaction time in the controller will still permit 333 KC cycle rate.

C.   Byte Controls - Controller to DMA

The two (2) byte controls, in combination with Request, define the type of memory operation required. The byte controls must be established

within 50 nanoseconds after Request, but it is assumed that they will normally be established at the same time.

A high byte line indicates a clear-write operation, a low line implies read-restore. No write, or read, commands are required. The byte lines may be dropped after Acknowledge is seen.

D.   Data Input Control - Controller to DMA

In Clear/Write operations, data to be written need not be available at the beginning of the cycle. The DMA is designed to allow the controller to supply input data after the cycle has started, delayed by up to 250 nanoseconds after Acknowledge was generated. The controller must take into account transmission delays if it uses a delayed input. The data must be stable at the time the DMA samples the data lines.

If the controller wishes to get rid of its data earlier, it may use its own data transfer signal for storing the data bus contents in the DMA data register. The logic for doing this is enabled by the controller, and permits the latter to effect the transfer by a negative pulse of at least 75 nanoseconds' width at any time after Acknowledge is generated and before the time when the write operation begins. The latter is 250 nanoseconds after Acknowledge was generated. Naturally, the data lines must be stable when the controller issues its transfer, and transmission delays must be considered. Transfer occurs on the leading edge of the pulse.

E.   Data Available - DMA to Controller

Coincident with the switching of the read data onto the bi-directional data bus, the switch control signal is sent to the controller. It may be used within the controller. If the negative true signals on the data bus directly set FF's in a previously cleared register, the trailing edge of the data available signal may be used simply to indicate end of data transfer. If the bus signals are inverted, then strobed into a register by the data available signal, only single-sided gating may be used, because the front edges of the control and data signals are not consistently leading or following the other. D. A. is a 250 nanosecond, positive, pulse, starting about 450 nanoseconds after Acknowledge.

F.   Error - DMA to Controller

If the controller attempts to write into protected memory, an Error FF is set, which prevents any response to further cycle requests from that controller. This line informs the controller of its error.

G.   Error Clear - Controller to DMA

This line provides a means for resetting the memory protect error FF. If held low, it disables the Error FF.

H.   Parity Error - DMA to Controller

This line carries a positive, 250 nanosecond pulse if a full or partial read-restore operation detected a parity error during the cycle.

IV.   Address Transfer

The sixteen (16) address lines from the controller carry positive true logic. They must be established not later than Request, and must be maintained until Acknowledge. The load is one (1) unit.

V.   Data Transfer

The transfer of data between controller and DMA is over one set of lines, 16 in all. A bi-directional data bus was selected to save pins on the data switching board, and to conform to the data transfer method used on the PDC and MDC.

The bi-directional bus requires that open collector drivers be used at both ends of the line, and that the driver on one end be non-conducting when the other end is sending data. Negative true signals are required.

When sending data to the DMA, the controller need not place the data on the bus until near the end of the clear operation of the memory. About 250 nanoseconds' delay is permitted after Acknowledge is seen. If a read operation is taking place, the receiving register must be cleared and waiting within 400 nanoseconds after Acknowledge.

The presence of output data on the lines will be signalled by the Data Available signal, which will start about 450 nanoseconds after Acknowledge, and will last for 250 nanoseconds.

The DMA will always supply output data when storing of data is not requested. Thus, the controller may write into one byte and read out the other in a single access.

No parity is switched through, or generated by, the DMA. If the memory is provided with parity checking, an error detected during a cycle by the controller will cause an error signal to be sent to the controller. The error may also cause a program interrupt in the computer. No other action than simply passing along the fact that an error occurred is taken by the DMA.

VI.   DMA Options

The DMA and TND boards have been designed to permit simultaneous memory access, whenever two independent memory systems are used. Such would be the case where the CPU has 4K of SAD, HAD memory, and the DMA controls one nest of CE 100. Another case would be a system with two nests of CE 100 type memory each with a self-contained timing system.

In each case, one memory unit can be attached to the CPU, the other to the DMA. For so long as the CPU accesses its dedicated memory, simultaneous access by CPU and peripheral controller is possible.

The SAD and CE 100 memories can be both connected to the DMA so that the controller (s) may operate in all parts of the memory system. In this case, any conflict results in stopping CPU operations.

Any number of DMA devices may be used in the system. However, the number of individually controllable memory sections determines the practical limit to use of multiple DMA's. A DMA must control all or none of a memory section (constraints may be put upon the addresses available to a controller). To control a section of memory by more than one DMA is not feasible or possible, because simultaneous use of that section is not possible in any case.

In summary, each DMA provides for access by the CPU and one or two controllers to a section of memory capable of independent control.

VII.   Two Controllers on a DMA

By adding one data switching board, a second controller can be put on the DMA. Its priority will be second to the original controller. Even if the second controller is operating in burst mode, the original controller will take precedence.

DESIGN NOTES FOR DMA

I. GENERAL COMMENTS

The DMA design provides the following:

A. A single DMA channel is provided on two cards. The amount of logic perhaps does not warrant using two cards, but the number of pins required for address and two way data switching exceeds 144.

B. Another Selector Data Channel, SDC, can be connected to the DMA by adding one card – the data switching card. The address switching card contains logic for a second SDC. The two data cards are simply paralleled.

C. Data communication with the SDC is on a bi-directional data bus. This was done mainly to conserve pins, and to conform to PDC communication interface.

D. The DMA generates conflict signals, and their complements, for quieting the time slot, TS, and CPU clock logic on the timing board, TND.

E. Two modes of SDC control are provided. The SDC can operate in either a burst mode or interlock mode. Using the fomer, the SDC must ensure that a new requrest, with its concomitant address, is present at the DMA within $3/4\,\mu$S of receipt of acknowledge of former set. If so, 10^6 transfer rate is possible. The "single op" latch in the DMA control logic is disabled during the operation. The interlock mode releases the SDC from any timing restriction on dropping its Request line. The DMA ignores the Request line, having serviced it, until it is dropped. The DMA drops the Acknowledge only after the request is dropped.

F. The SDC may use one of two methods for input of data during clear-write ops. It may pulse a strobe line to transfer the word on the data bus into the data register of the DMA after receiving Acknowledge. Alternatively, it may provide no strobe signal, in which case the DMA timing logic automatically transfers the bus data at about 200 nanoseconds after Acknowledge. This dual feature provides some flexibility to the SDC in data input timing.

G. A "data available" signal is provided for the SDC when the memory switch has stored the byte, or word, read from memory, and has put it on the data bus.

* A Selector Data Channel, SDC, is a device that provides DMA interface with up to four I/O Controller. The I/O controller interface is the same as the PDC or MDC interface. The SDC may be replaced with a special I/O Controller that connects to the DMA.

H. During partial clear/write operations, the read-restored portion of the word is placed on its data lines. The SDC may write into one byte and read the other, if it desires.

I. If the SDC causes a memory protect error, a FF in the DMA is set, and further DMA's by that device are prevented. The FF is output to the SDC, and is reset by some external signal.

Design Notes for DMA
X.   Direct Memory Access Channel Description

X.1   Introduction

The DMAC is a device by use of which one or two external devices, hereinafter
called the Peripheral Memory Controller (PMC),[*] may directly access the
MAC 16 memory, on a cycle stealing basis, without recourse to program
interrupts or CPU I/0 commands. The PMC must supply to the DMAC the
address of the memory cell to be accessed, along with data (if writing),
and byte selection, mode control, and request signals. The PMC is given
precedence over the CPU in accessing the memory. During PMC access
the CPU is caused to enter a quiet state.

Storage for both address and data is provided within the DMAC, so that
high transfer rates are possible.

X.2   DMAC Operating Modes

The DMAC provides two modes of operation. They are: Interlocked mode,
and Burst (high transfer rate) mode. The mode selection is controlled by a
line from the PMC.

X.2.1   Interlocked Mode

The normal sequence of exchange of control signals between PMC and DMAC
is started by a request for access from PMC to DMAC. When the latter has
begun a memory access for the PMC, it sends to it an acknowledge signal.
The DMAC, at the same time, sets a flip-flop which prevents further response
to the request signal. The flip-flop is reset only when the request signal is
dropped. Thus, in the Interlocked mode, no restriction is placed upon the
length of time that a PMC may continue its request signal after receipt of
acknowledge – no redundant operations result. The PMC must drop request,
and observe the resultant termination of the acknowledge signal, before it
can again request access.

X.2.2   Burst Mode

The four exchanges of control signals implicit in the Interlocked mode
prevent realization of the maximum possible access rate (10^6 per second)
by the PMC. Therefore, the interlock, or "single operation, " flip-flop
may be disabled by the PMC to achieve the higher rate. Without the
interlock the PMC must control its request signal with greater precision.
If it desires consecutive accesses, it may continuously maintain the request
signal. If so, it must ensure that the next address is at the DMAC within
$3/4\mu$s of the time when the latter issued the acknowledge for the current request.
On the other hand, if the PMC wishes no further access, it must ensure that
the request signal is terminated sufficiently early to be off at the DMAC
within the same $3/4\mu$s period, or a redundant access will result. In the

* The PMC may be a Selector Data Channel, SDC.

Burst mode, transmission delays to and from the DMAC must be taken into account for proper operation. In the Interlocked mode they need not be considered in the design of the PMC, they merely reduce the transfer rate.

X.2.3 Input Data Transfer Options

Another operation feature under the control of the PMC is the manner by which data is transferred from PMC to DMAC during write operations. Since data input to the DMAC is not required until the write portion of the memory cycle, the PMC need not provide it as early as the address. An internal transfer signal within the DMAC is available, which will strobe the data lines at a fixed time after acknowledge. However, the PMC may suppress this internal signal and supply its own transfer pulse, at any earlier time after seeing Acknowledge, if it wishes to dispose of its data earlier. The method of transfer is controlled by a wire from the PMC.

X.3 DMAC Configurations

X.3.1 Two PMC's on One DMAC

The basic DMAC provides for access to the core memory, or a portion therof, by one PMC. The PMC and the CPU connect to the DMAC, and compete for access to the memory. The PMC is given precedence. The DMAC requires two circuit boards, one for address switching and control, the other for data switching.

A second PMC may be connected to the DMAC by adding a second data switching board. The second PMC is given intermediate priority between the original PMC and the CPU. The priority is not influenced by the operating mode selected by either PMC.

X.3.2 Two or More DMAC's

Where permitted by memory system design, the memory may be divided into sections, each controlled by a different DMAC. Presumably, the CPU would attach to each such DMAC, while the PMC's would be assigned to different DMAC's. It is not feasible, or possible, to control a section of memory by more than one DMAC, because only one memory operation at a time can be carried out within a section of memory controlled by common addressing and timing logic, in any case.

If an PMC is connected to more than one DMAC, the PMC should provide a separate request signal for each DMAC. Only the request line to the proper DMAC should be enabled, otherwise nonexistant addresses will be accessed, incorrect data received, and time wasted.

Whenever requests by different PMC's or by an PMC and the CPU, are to different DMAC's, simultaneous memory accesses can occur.

X.3.3 One DMAC Controlling Less Than the Entire Memory

It is possible to divide the memory system between one DMAC and the CPU. When the CPU and the PMC are competing for access to the DMAC controlled memory, the CPU must wart. However, if the CPU is accessing its reserved memory simultaneous access by the CPU and the PMC is possible.

X.4 Control Signals Between PMC and DMAC

The control signals which interconnect the PMC and DMAC are listed and described in the sequence in which they occur in normal operation.

X.4.1 Request - PMC to DMAC

The Request signal is answered by an Acknowledge signal from the MS, signifying that a memory operation has begun. The Request signal may then be operated in one of two ways, depending upon whether the controller is using "Burst", or Interlock, mode.

If in Burst mode, the PMC need not drop the Request line if another DMA is desired. It must, however, ensure that the next memory address is at the DMAC within $3/4\mu$sec of the time when the DMAC originated the Acknowledge. Thus, the controller has $3/4\mu$sec – 2 transmission delays to react to the Acknowledge. If it desires no further DMA, it must drop its Request immediately, so that the MS sees no Request at $3/4\mu$sec after Acknowledge.

If the Interlock mode is in force, the PMC may leave the Request line high after seeing Acknowledge – no repeated DMA's will result from it. After it drops the Request, the Acknowledge will be dropped, thus informing the PMC that the end of Request has been seen. The PMC may then raise Request again.

If a single PMC is on the DMAC, and if it drops its Request within $1/4$ μsec upon seeing Acknowledge, it can access memory at 500KC. If two controllers are on the DMAC, they may operate in an interlaced manner, effectively monopolizing the memory. The Request signal is enabling in the negative state. The D.C. load is about 5 ma.

Design Notes for DMA

X.4.2 Acknowledge – DMAC to PMC

Immediately (60 nanoseconds) after the DMAC has stored the address from, and just as it initiates a memory cycle for, and PMC it sends the Acknowledge signal to the PMC. The signal does not mean that the DMAC has stored input data, if a write operation is indicated. However, the address lines need not be maintained after Acknowledge.

In the Burst mode, the Acknowledge signal is maintained for 350 nanoseconds, then is dropped.

In the Interlock mode, the Acknowledge signal is maintained until the DMAC has seen the end of the Request signal, at which time, it also drops. The controller may then request another access.

Since four (4) transmission delays occur in exchanging control signals, the DMA rates possible in Interlock mode are impossible to guarantee. However, $1/4\mu sec$ per exchange and $1/4\mu sec$ reaction time in the PMC will still permit 333 KC DMA rate. Acknowledge PMC as a positive true signal.

X.4.3 Byte Controls – PMC to DMAC

The two (2) byte controls, in combination with Request, define the type of memory operation required. The byte controls must be established within 50 nanoseconds after Request, but it is assumed that they will normally be established at the same time.

A high byte line indicates a clear-write operation, a low line implies read-restore. No write, or read, commands are required. The byte lines may be dropped after Acknowledge is seen.

X.4.4 Data Input Control – PMC to DMAC

In Clear/Write operation, data to be written need not be available at the beginning of the cycle. Most computers take advantage of this fact to overlap arithmetic and memory operations. The DMAC is designed to allow the PMC to supply input data after the cycle has started, delayed by up to 250 nanoseconds after Acknowledge was generated. The PMC must take into account transmission delays if it uses a delayed input. The data must be stable at the time the DMAC samples the data lines.

If the PMC wishes to get rid of its data earlier, it may use its own data transfer signal for storing the data bus contents in the DMAC data register. The logic for doing this is enabled by the PMC, and permits the latter to effect the transfer by a negative, 75 nanoseconds wide, pulse at any time after Acknowledge is generated and before the time when the write operation begins. The latter is 250 nanoseconds after Acknowledge was generated. Naturally, the data lines must be stable when the PMC

Design Notes for DMA

issues its transfer, and transmission delays must be considered. Transfer occurs on the leading edge of the pulse. The data lines should be allowed about 100ns to settle before transfer. The low condition of the enable line will permit the remote transfer pulse to be used. The pulse line required a negative signal.

X.4.5 Data Available - DMAC to PMC

Coincident with the switching of the read data onto the bi-directional data bus, the switch control signal is sent to the controller. It may be used within the controller, if certain precautions be taken. If the negative true signals on the data bus directly set FF's in a previously cleared register, the trailing edge of the Data Available signal may be used simply to indicate end of data transfer. If the bus signals are inverted, then strobed into a register by the data available signal, only single-sided gating may be used, because the front edges of the control and data signals are not consistently leading or following the other. D. A. is a 250 nanosecond, positive pulse, starting about 450 nanseconds after Acknowledge.

X.4.6 Error - DMAC to PMC

If the PMC attempts to write into protected memory, and Error FF is set, which prevents any response to further Request from that PMC. A positive signal on this line informs the PMC of its error.

X.4.7 Error Clear - PMC to DMAC

A negative pulse on this line resets the memory protect Error FF. If held low, it disables the Error FF.

X.4.8 Parity Error - DMAC to PMC

This line carries a positive, 250 nanosecond pulse if a full or partial read-restore operation detected a parity error during DMA.

X.5 Address Transfer

The sixteen (16) address lines from the controller carry positive true logic. They must be established not later than Request, and must be maintained until Acknowledge. The load is one (1) unit.

X.6 Data Transfer

The transfer of data between PMC and DMAC is over one set of lines, 16 in all. A bi-directional data bus was selected to save pins on the data switching board, and to conform to the data transfer method used on the PDC and MDC.

The bi-directional bus requires that open collector drivers be used at both ends of the line, and that the driver on one end be non-conducting when the other end is sending data. Negative true signals are required.

When sending data to the DMAC, the PMC need not place the data on the bus until near the end of the clear operation of the memory. About 250 nanoseconds' delay is permitted, after Acknowledge is seen. If a read operation is taking place, the receiving register must be cleared and waiting within 400 nanoseconds after Acknowledge

The presence of output data on the lines will be signalled by the Data Available signal, which will start about 450 nanoseconds after Acknowledge, and will last for 250 nanoseconds.

The DMAC will always supply output data when storing of data is not requested. Thus, the PMC may write into one byte, and read out the other, in a single DMA.

No parity is switched through, or generated by, the DMAC. If the memory is provided with parity checking, an error detected during a DMA by an PMC will cause an error signal to be sent to the PMC. The error may also cause a program interrupt in the computer. No other action than simply passing along the fact that an error occurred is taken by the DMAC.

X.7 A Typical PMC Design

The typical PMC must interface with three systems in order to properly perform its function. First, it must interface with the data source, such as the magnetic drum, disc, or tape.

The PMC will fetch data from, or supply data to, these media, and provide buffer storage and compatible interfaces between these devices and the bi-directional data channel to the DMAC.

The second interface is to the DMAC, and has been described in previous sections.

The third interface is with the PDC of the CPU. This interface provides for initiation and control of the PMC by the CPU.

X.7.1 Design Features Relating to the PDC Interface

The PMC will, as a device on the, PDC, be assigned a device number. It must include in its design logic for recognitions of those EC∅'s addressed to itself.

Design Notes for DMA

The CPU will, by means of the ECØ command (and perhaps EDØ) initiate
the _____ . This operation includes supplying the starting address, and the
block length, to the PMC. These will be stored in two ripple counters, one
arranged to increment, the other to decrement. The CPU will also provide
start and stop signals to the PMC.

As the PMC executes DMA's, it increments the address counter and decrements
the block length counter. Since address storage is provided within the DMAC,
the PMC design must only ensure that Request is not made until the counter
has stabilized. When the block length counter reaches zero, the PMC will
issue a Service Request (SR) to the CPU.

The SR feature must be capable of suppression by the ECØ. Also, it must conform
to the requirement of not changing SR during and EAI command. The PMC must
place its own device number on the PDC bus when it is the highest priority SR in
effect during the EAI.

The PMC should also respond to an ESI command. The information supplied
therein may include availability, state of block length counter (empty or not)
etc.

SECTION III

MAC 16 DEVICE CONTROLLER OPTIONS

MAC 16 DEVICE CONTROLLER OPTIONS

CONTROLLER OPTIONS

Computer control and communication with a peripheral, input-output device requires a logic unit that matches the computer's Programmed Data Channel, PDC, with the electrical characteristics of the device. This unit is called a Controller. It provides response to computer generated instructions, data buffering and signal level switching between the PDC and the device.

A very complete description of the functions of a Controller and typical logic designs of its functions is presented within the MAC 16 Interface Reference Manual.

Computer chassis slots 1 through 9 are available for installation of Controllers in the computer's main-frame. These slot positions are also used for Processor Options which have priority over Controllers. When main-frame slots are not available for all the desired Controllers, either an External Controller Chassis, ECC, or a Memory Controller Chassis, MCC, must be provided.

Whenever Controllers are provided outside of the Computer Chassis, a Line Driver, -LD, (or Cable Driver, -GD) must be provided in the main-frame and a Line Receiver, -LR, (or Cable Receiver -GR) must be provided in the external chassis.

Controllers require one or two MAC 16 PC cards, a cable connector and cable to the peripheral device and the device or devices. When Controllers are specified attention must be given to the location of the devices and the interconnecting cable lengths.

Controllers that are being developed for the MAC 16 are summarized in Table 1.

TABLE 1. MAC 16 Controllers

Controller	Designator	PC Cards	Slots	Device Models	Device Designator
First Teletype Controller Second Teletype Controller Third Teletype Controller	–TC1 –TC2 –TC3	YAD 2 YAD's 3 YAD's	9 9, 7 9, 7, 6	ASR–33TC or ASR –33 TZ ASR–35 KSR–35	TT3 TT5 TK5
High Speed Paper Tape Reader and Punch Controller	–HC	RAD	8	Digitronics Model 2540 EP Paper Tape Reader Without Spooler	PRN
				Digitronic's Model 2540 EP Paper Tape Reader With Model 6012 Handler	PRS
				Digitronic's Model 1560 Paper Tape Punch Style B Package With Control Electronics Package A1.	PPN
				Digitronic's Model 1560 Paper Tape Punch Style C Package With Control Electronics Package C1.	PPS
External Data Input Channel	–XI	EIC	4		
External Data Output Channel	–X0	EOC	5		
Drum Memory Controller	–DM	DCA DCB	1 2	Vermont Research Inc. Model 1004–S–32 Model 1004–S–64	DM1–32 DM1–64
	–DN	DCA DCB	7 8	Model 1004–S–128 Model 1016–32 Model 1016–256 Model 1016–512 Model 1032–256 Model 1032–512	DM1–128 DM2–128 DM2–256 DM2–512 DM3–256 DM3–512

Table 1. MAC 16 Controllers (Continued)

Controller	Designator	PC Cards	Slots	Device Models	Device Designator
Drum Memory Controller (continued)				Model 1032–1024 Model 2032–256 Model 2032–512 Model 2032–1024 Model 2064–512 Model 2064–1024 Model 2064–2048	DM3–1024 DM4–256 DM4–512 DM4–1024 DM5–512 DM5–1024 DM5–2048
Line Printer Controller	–LP –LO	LPC LPC	3 6	Data Products Mod 2310 Model 2410	LPD LPE
Card Reader Controller For CRD	–CD –CE	CRC–1 CRC–1	7 6	Data Products Corp SR–300	CRD
Card Reader Controller for CRG	–CG –CF	CRC–2 CRC–2	7 6	General Design Inc GDI–100	CRG
Magnetic Tape Controller 9 Track, 800 BPI	–M9	MTC MT9	1 2	Peripheral Equip. Corp. Model 6840–9	M49
	–N9	MTC MT9	7 8	Model 6820–9	M29
Magnetic Tape Controller 7 Track, 556 or 800 BPI	–M7	MTC MT7	1 2	Peripheral Equip. Corp. Model 6X40–7	M47
	–N7	MTC MT7	7 8	Model 6X20–7	M27
Data Modem Low Speed Asynchronous	–YM	YAM	7	Bell 103A, 103F Bell 202C, 202D Friden 7100 Dura 1041 SCM Klein Schmidt 311 RCA 70–52	
Data Modem, High Speed Synchronous Without Dial Up	–YS	YHS, YHD–1	1 2	Bell 201 A or B Saunders 120 Crt UNIVAC Uniscope Raytheon DIDS–400 (Many Others)	
	–YT	YHS YHD–1	7 8		
Data Modem, High Speed Synchronous With Dial Up	–YD	YHS YHD–2	1 2	Bell 201A or B with Bell 801. Several EIA Standard Terminals	
	–YE	YHS YHD–2	7 8		

Teletype Controller   TC1, TC2, TC3

This controller provides duplexed communication with a Teletype ASR33, ASR35 or KSR 35.
It consists of both a receiver buffer and a transmitter buffer which provides simultaneous
input and output. The receiver accepts a serial input of 11 bits per character where one bit
represents a start bit, 8 bit data character and two bits represent end of character. Input
is at 10 characters per second. The controller transfers the 8 bit character in parallel
to the computer. The receiver accepts data from a keyboard or paper tape reader.

The transmitter accepts an 8 bit character from the computer and transmits it to the punch
and/or print device serally as an 11 bit character at 110 band.

The Teletype Controller, TC1, is contained on one logic card, YAD. This is located in
slot position 9 of the computer chassis.

A second Teletype Controller, TC2, may be added. It occupies slot 7 unless more than
16 interrupts are provided. In that case it must be located in an external chassis.

A third Teletype Controller, TC3, is assigned to slot 6. This conflicts with the Line Driver
option, -LD. The Line Driver option has priority if both are specified, however, an LE
option places the Line Driver in slot 5.

The three Teletype Controllers use six of the 256 device addresses as follows:

MN Field

02	TTY Transmitter #1
03	TTY Receiver #1
04	TTY Transmitter #2
05	TTY Receiver #1
06	TTY Transmitter #3
07	TTY Transmitter #3

A modification to each teletype device is made by LEC. This is the addition of a relay to allow
computer control of the reader on-off switch. The device's functions such as response to
"who are you" is disabled, and the signal current level is changed from 60 ma to 20 ma.

High Speed Paper Tape Reader and Punch Controller   -HC

This controller includes two parts. An input buffer for a paper tape reader and an output
buffer for a paper tape punch. Both input and output may be in operation simultaneously.

Communication with the HSPT Reader is 8 bit parallel at 300 characters per second.
Communication with the HSPT Punch is 8 bit parallel at 60 characters per second.

The HSPT Controller is contained on one logic card, RAD. It occupies slot 8 in the computer
chassis. Connector A of this slot position is always wired with the PDC interface whether
the HC option is included or not.

The HSPT Controller uses two device addresses: 08 for the HSPT Punch and 09 for the HSPT
Reader.

The HSPT Controller is designed to communicate with a Digitronics Model 2540 EP Tape
Handler and a Digitronics (formally INVAC) Model 1560 Paper Tape Punch.

External Data Input Channel   –XI

This unit is not a special device controller because it is not designed to control a particular
device. It is useful to receive external signals from a variety of devices. It consists of two
identical and independent sections, each consisting of a 16 bit register that holds external
signals until they are input to the computer. External signals may be pulses or levels. The
external lines or contents of the buffer register, 16 bits at a time, may be read into the
computer's accumulator by execution of ESI or EDI instructions.

The External Data Input Channel, –XI, is contained on one logic card, EIC. It's computer
chassis position is slot 3. This conflicts with the Multiplex Data Channel option, –MC, if
it is also required. In that case, the EIC card must be located in an external chassis.
The XI option includes two wired in 41 pin external connectors, one for each XI register.

The External Data Input Channel uses two device addresses, one for each XI register.

External Data Output Channel   –X0

This unit is not a controller for a special device but it could be used for that purpose under
program control. It consists of two identical and independent sections, each consisting of
a 16 bit register and control that can be set under programmed instructions. These registers
are used for general external output.

The External Data Output Channel, -XO, is contained on one logic card, EOC. Its computer chassis position is slot 5. This conflicts with the Multiplex Data Channel option -MC', if it is also required. In that case, the EOC card must be located in an external chassis. The X0 option includes two wired-in 41 pin external connector, one for each XO register.

The External Data Output Channel uses two device addresses, one for each XO register.

The External Data Input and Output Channels may be used for a variety of applications. They are designed to allow computer to computer communication via the PDC of two MAC's. They can provide external sense and drive lines to a customers special systems equipment. They are useful for man-machine communication when a switch/lamp panel is provided.

<u>Drum Memory Controller</u>   – DM or –DN

The Drum Controller provides computer interface with one or two magnetic drum memories. Drum capacity ranges from 32,768 16 bit words on one drum to 4,194,304 16 bit words on two drums. Drum data rates may be 62,000, 31,000, 15,500, 7,750 or 3,875 words per second. The data rate is selected by a single jumper installed in the back-plane wiring of the Drum Controller. Data is addressed in 64 word sectors on the 10 inch drums or 128 word sectors on the large 20 inch drums. The controller communicates with the drum serially and with the computer in 16 bit parallel words. The controller records and checks a parity bit on the drum.

The controller is designed to use Vermont Research Inc. magnetic drums, Models 1004, 1016, 1032, 2032 and 2064. Each drum requires an additional power supply and special drum mounting in a cabinet. The following panel heights are required for the 10 inch drums:

	Height With P.S.
Model 1004	19 1/4 inches
Model 1016	28 inches
Model 1032	38 1/2 inches

The 20 inch drums do not fit a standard 19 inch relay rack. They are too wide. A special cabinet will be required for them.

The Drum Controller requires two logic cards, DCA and DCB. They are assigned slots 1 and 2 when an MDC is not included (-DM) or slots 7 and 8 when an MDC is included (-DN).

The Drum Controller uses eight device addresses. The three least significant bits are used to define controller operation modes.

Line Printer Controller   -LP or -LO

This controller drives a Data Products Model 2310 Line Printer. This printer prints a
modified version of the ASCII code. It contains a 20 character buffer that prints each time
the 20th character is received or when a format control character is received. Up to
80 columns may be printed per line.

The Line Printer Controller transmits an eight bit character in parallel to the Line Printer.
Special characters are used to control the printer.

The Line Printer Controller requires one logic card, LPC. It is assigned to slot 3 for
option -LP or slot 6 for option -LO in the computer chassis.

The Line Printer Controller uses one device address

This same controller should be capable of controlling and transmitting to the Model 2410
Line Printer that prints 132 columns when that device is available.

Card Reader Controller   -CD, CG or -CE or -CF

Two assemblies of this controller are developed. One receives data from a Data Products
Corp. Model SR-300 (-CD or -CE) and the other receives data from a General Design Inc.
Model GDI-100 (-CG or- CF). Both card readers photoelectrically read 300 cards per
minute, column by column. A card character is a 12 bit binary number with a one bit
representing a row-punch in the card. Computer conversion routines are provided to change
input data to a coded format.

The Card Reader Controller requires one logic card, CRC. It contains two assemblies:
CRC-1 for the Data Products card reader and CAC-2 for the G.D.I. card reader. The card
may be located in slot 7 for options CD and CE or slot 6 for CG and CF.

The Card Reader Controller is assigned one device address.

Magnetic Tape Controller, 9 Track   –M9 – N9

This controller provides control and communication with up to four Magnetic Tape units.
It communicates with the computer in either a full word, 16 bits, or charcter, 8 bits, mode.
It causes data to be written in standard IBM compatable, 9 track format at 800 characters
per inch. It reads data from the tape in the same format. It communicates with one tape
unit at a time.

The Magnetic Tape Controller requires two logic cards, MTC and MT 9. They are assigned
to slots 1 and 2 (–M9) when the Multiply/Divide option is not included or to slots 7 and 8
(–N9).

The Magnetic Tape Controller is designed to interface with Peripheral Equipment Corp.
Models 6840-9 or 6820-9. The difference between the two models is that the 6840 includes
a read-after-write capability while the 6820 does not. The Magnetic Tape Controller
operation for either unit is selected by a jumper installed in the back-plane wiring of the
controller.

The Magnetic Tape Controller uses one device address. Selection of the magnetic tape unit
is by a Connect command.

Magnetic Tape Controller, 7 Track   –M7, –N7

This controller is similar to the 9 track controller except that it provides communication
with one of four Magnetic Tape Units in an IBM compatable 7 track format. One of two
recording rates may be selected: 556 characters per inch or 800 characters per inch. The
selection is made by a switch on each magnetic tape unit.

This controller is currently not under development. Documentation will be available at a
later date.

The 7 track Magnetic Tape Controller will use one of the cards of the 9 track controller plus
a special card of its own. They will be assigned the same slot positions as a 9 track controller.

The 7 track controller will provide control and communication with Peripheral Equipment Corp.
Models 6X40-7 or 6X20-7.

The Magnetic Tape Controller, 7 track, uses one device address. Selection of the magnetic
tape unit is by a connect command.

This controller may also be used for a 200 character per inch recording rate. This will be
selected with a jumper wire.

Data Modem, Low Speed, Asynchronous   -YM

The controller provides a full duplex RS 232 B interface between the computer and a Bell Type 103A, 103F or equivalent asynchronous data set. Data communication between the computer and this modem controller is 8 bit parallel. Communication with a data set is by 8 level, 11 unit serial start-stop code. The standard communication rate is 10 characters per second (110 band serial bit rate). Optional clock rates can be provided by special order up to the maximum 300 band data set capacity.

The controller may be wired for fully automatic DDD switched network call answering and termination when used with the 103A data set and its associated 804B1 control unit. Optional wiring facilities are provided for manual answering and termination when alternate telephone communication is desired.

This controller requires one logic card called YAM. It is assigned to slot 7. It requires two device addresses, one for input and one for output.

Data Modem, High Speed Synchronous

Without Dial Up	-YS
With Dial Up	-YD

This controller provides an 8 bit character buffer and control between the computer and RS 232 B, bit serial synchronous Bell System 201A, 201B or equivalent modems. The controller may be used for two wire half duplex or four wire full duplex data communication over voice grade, switched network or dedicated telephone lines. The controller checks parity of each received 8 bit character. The controller does not generate parity for output data.

Data transmission rates are determined by the data modem and communication line characteristics.

This controller requires two logic cards, YHS and YHD. They are assigned to slots 1 and 2 in the computer chassis. The YHD card has two assemblies; one for the dial up option with a Bell 801A or 801C and one without.

The High Speed Data Modem Controller requires two device addresses.

YAD TELETYPE WRITER CONTROLLER

1.0   SYSTEM DESCRIPTION.

An ASR33 Teletypewriter set is used with the basic MAC-16 Computer for input/output communication. This set is comprised of a Keyboard, Printer, Paper Tape Reader and Punch which operate at a maximum speed of 10 characters per second. The YAD Teletype Writer Controller provides command, control and data buffering for communication with the MAC-16 Programmed Data Channel bus, PDC, and the ASR33 Teletype Writer. Full duplex operation is provided. This allows simultaneous output of data from the computer to the Teletype Writer Printer and/or Punch, and input of data to the MAC-16 Computer from the Keyboard or Reader.

The ASR33 receives and transmits 8 level 11 unit serial code at a 110 baud rate. The Printer utilizes 7 levels, with 64 code combinations assigned to print characters (including "space"), and 3 to non-printing functions (line feed, carriage return and bell). The 8th level (most significant bit) is ignored by the printer and may be either one or zero. The Punch will accept and punch all 256 permutations. The Reader similarly will read all 256 code arrangements. The Keyboard can generate all printer character and function code combinations, with the 8th level MSB always being a ONE.

The YAD Teletype Writer Controller communication with the MAC-16 Computer PDC data bus is eight-bit parallel character transfer under computer control. The YAD Controller provides the parallel to serial and serial to parallel conversions, and sunchronizing means to allow bidirectional Computer/Teletype Writer data transfers.

1.1   Teletypewriter Operation.

The ASR33 Printer uses 8-1/2 inch wide continuous roll paper for data print-out. All printing character code arrangements received will be printed, and the Printer will perform all functions (line feed, carriage return and bell) whether or not tape punching is enabled or inhibited.

The Punch uses 1 inch wide oiled paper roll tape. When the Punch is ON, each character received will be recorded with ones represented by holes and zeroes by no holes.

The ASR33 has 3 basic manual controls:
   1.   Local-Off-Line rotary switch.
   2.   Reader START-STOP-FREE lever.
   3.   Punch OFF, ON, REL and BSP pushbuttons.

1.1.1   Local-Off-Line Rotary Switch Functions.

OFF: Motor off, no operation.
LOCAL: Off-Line. Can prepare or duplicate program tapes.
LINE: On-line. Operational with MAC-16 Computer.

1.1.2   Reader Start-Stop-Free Lever.

STOP: Inhibits Reader operation.
FREE: Releases tape drive for manual removal or positioning of tape.
START: In local mode, starts tape reader if tape is loaded. In LINE mode,
         transfers Reader start/stop control to MAC-16 Computer.

1.1.3   Punch Pushbuttons.

OFF (locking): Inhibits tape punching. Page printing only allowed.
ON (locking): Enables tape punching in addition to page printing.
REL (non-locking): Releases tape drive for manual removal or movement of tape.
BSP (non-locking): Backspaces tape one character each time it is depressed.

1.2   Controller Operation.

The YAD Teletype Writer Controller is divided into two functional sections –
Receiver, and Transmitter. The Receiver assembles serial data characters
from the ASR33 Keyboard or Reader into 8-bit parallel character format for
input to the MAC-16 Computer. The Transmitter accepts computer outputs in
8 bit parallel bytes, and transmits each byte in 8 level 11 unit serial Teletype
Writer code to the ASR33 Printer and Punch.

A Controller Transmitter is assigned an even eight-bit binary station address
(not all zeroes); the associated Receiver is assigned the next higher odd binary
number address.

The Receiver is conditioned to accept data from the Teletype Writer Keyboard
whenever the ASR33 is "on line". Data transmission from the Reader is controlled
by MAC-16 Computer commands (ECO instructions). The Transmitter is condi-
tioned to accept a MAC-16 Computer data output byte (ASR "on line") resulting
from an EDO instruction at any time, except during the period a previous byte is
being transmitted to the ASR Punch and/or Printer.

Each functional section can operate independently in two basic modes, program
interrupt or non-interrupt. This is a programmer option with Computer ECO
command control as described in the MAC-16 Computer reference manual. Full
duplex input/output data transfers can be made in either operational mode. Each
section contains its individual program interrupt level logic; each may use its
own unique interrupt request line, or share a comman interrupt request line in
any procedence level order with other Device Controllers.

Immediately following CPU Power On automatic reset, and following each CPU control panel I/O Reset switch operation, the TTY controller is in initialized status, as follows:

1. Receiver and Transmitter service requests (program interrupts) are suppressed.

2. The TTY tape reader is inhibited from reading tape.

3. The Receiver section is conditioned to accept data transmission from the ASR keyboard, a CPU Start Tape or Allow Interrupt Command (ECO instruction).

4. The Transmitter section is conditioned to accept a CPU data out transfer (EDO instruction) or an Allow Interrupt command (ECO instruction).

The Transmitter's initialized status is a "service required" state. The service request that is normally issued in this state is suppressed, however. A CPU transmitter addressed "Allow Interrupt Command" (ECO) when executed as the initial CPU to transmitter instruction, immediately releases the suppressed service request and a program interrupt signal is placed on the PDC interrupt line. This interrupt can be removed by a CPU "Data Out" instruction (EDO) or by a CPU "Address In" instruction (EAI). An EAI instruction clears the transmitter's "service required state". No further transmitter interrupt will be issued until a CPU "Data Output" instruction (EDO) has been executed and the character has been transmitted to the Teletypewriter, and the transmitter again reaches the serve required state. A CPU "Inhibit Interrupt Command" (ECO) issued prior to completion of transmission to the ASR suppresses the program interrupt which would otherwise occur. An "Allow Interrupt Command" (ECO) subsequently executed before another Data Transfer instruction (EDO) performs as described during initialized status operation.

1.2.1   Program Interrupt Operation.

The Receiver transmits an interrupt signal to the MAC-16 Computer each time a new character has been received from the Teletype Writer and assembled. This interrupt signal is maintained until the computer responds with a "data in" or "address in" signal (EDI or EAI instruction), or until the ASR initiates transmission of a new character. If a "data in" response is not made before transmission of a new Teletype Writer character begins, the controller receiver does not acknowledge the "data in" request and discards the previous data.

The Receiver ignores a "data in" signal when a valid byte is not available for transfer and after a valid byte has once been transferred in response to a previous EDI instruction.

The Transmitter sends an interrupt signal to the MAC-16 Computer each time the eighth data bit (unit 9 of the 11 unit Teletype Writer code) of a computer output byte has been transmitted to the ASR. This interrupt signal is maintained until the MAC-16 Computer output another byte (EDO instruction) or responds with an "address in" signal (EAI instruction).

1.2.2   Non-Interrupt Operation.

The Receiver does not transmit an interrupt signal to the MAC-16 Computer after assembling a Teletype Writer character, and ignores an "address in" (EAI instruc-

tion) signal. A "data in" signal (EDI instruction) is acknowledged and a byte transfer made in response to the first "data in" signal following the assembly of each Teletype Writer character, except when this signal occurs after the ASR has initiated transmission of a new character. In this case the previous character is discarded and the "data in" signal is not acknowledged.

The Transmitter does not send an interrupt signal to the MAC-16 Computer after completion of data transmission, and ignores an "address in" signal (EAI instruction). One "data out" signal only (EDO instruction) is acknowledged and accompanying data byte accepted after transmission has been completed of each previous byte transfer.

1.3   I/O INSTRUCTION.

1.3.1   The ECO instruction performs as described in the MAC-16 Reference Manual. The M and N fields of the ECO instruction define the Receiver or Transmitter address. All valid commands are accepted and a Controller "Acknowledge" signal returned.

The right byte of the A Register defines the command. Two commands (para. 1.3.1.3 and 1.3.1.6) apply to either the Receiver or Transmitter section, as defined by the instruction M and N fields. Six commands apply to Receiver functions only. The eight valid command words are defined below.

1.3.1.1 Read Tape - XX01

This Receiver addressed command initiates the reading of tape on the Reader.

1.3.1.2 Stop Tape - XX02

This Receiver addressed command terminates the reading of tape after the next character has been received.

1.3.1.3 Interrupt Inhibit - XX04

This Receiver or Transmitter addressed command prevents the Controller Receiver or Transmitter from issuing an interrupt request to the CPU regardless of data transfer requirements.

1.3.1.4 Read Tape and Inhibit Receiver Interrupt - XX05

This Receiver addressed command initiates reading of tape and prevents the Receiver from issuing an interrupt request.

1.3.1.5 Stop Tape and Inhibit Receiver Interrupt - XX06

This Receiver addressed command terminates the reading of tape after the next character has been received, and prevents the Receiver from issuing an interrupt request.

1.3.1.6   Interrupt Allowed - XX08

This Receiver or Transmitter addressed command allows the Controller Receiver or Transmitter to issue an interrupt request to signify that a data input transfer is required.

1.3.1.7   Read Tape and Allow Reciver Interrupt - XX09

This Receiver addressed command initiates the reading of tape and allows the Receiver to issue an interrupt request to signify that a data transfer is required.

1.3.1.8   Stop Tape and Allow Receiver Interrupt - XX0A

This Receiver addressed command allows the Receiver to issue an interrupt request to signify that a data transfer is required, and terminates the reading of tape after the next character has been received.

1.3.2   EDI

The EDI instruction performs as described in the MAC-16 Computer Reference manual. The M and N fields of the EDI instruction define the Controller Receiver address. A "data in" signal is transmitted to the controller. An "acknowledge" signal from the Controller signifies data has been placed on PDC data bus lines 8 through 15. Absence of an acknowledge signal signifies no data is available for transfer.

The most significant data bit is placed on line 8, in descending order with the LSB on line 15.

1.3.3   EDO

The EDO instruction performs as described in the MAC-16 Computer Reference manual. The M and N fields of the EDO instruction define the Controller Transmitter address. The right byte of the A Register is placed on PDC data bus lines 8 through 15, with the byte MSB on line 8, in descending order, with the LSB on line 15. A "data out" signal is transmitted to the Controller. An "acknowledge" signal from the Controller signifies data has been transferred. Absence on an acknowledge signal signifies a data transfer is refused at this time.

1.3.4   EAI

The EAI instruction performs as described in the MAC-16 Computer Reference manual. An "address in" signal is transmitted on the PDC. When a Controller interrupt request is active, the address of the section requesting service is placed on the PDC data bus lines 8 through 15. The address MSB is placed on line 8, in descending order with the LSB on line 15. The Controller does not return an "acknowledge" signal.

1.4   Program Requirements

The normal Controller operational mode is with Receiver and Transmitter program interrupts allowed. An active interrupt request signal is cleared at the completion of service by an EAI, EDI, or EDO instruction as applicable. Each of these instructions shall be followed by an additional instruction before a JRL instruction is executed to insure that this interrupt level signal has dropped.

Certain programming restrictions are required to operate the Receiver in the interrupt inhibited mode. The Reader and CPU timing are asynchronous, and CPU service (EDI instructions) must be offered at a faster rate than tape data characters are read to preclude timing errors.

1.4.1   ECO Instruction Commands

The A Register contents must be limited to the eight valid command words defined in Section 1.3.1.

1.4.1.1   TELETYPE WRITER READ TAPE

This command initiates the reading of tape on the Teletype Writer unit when all conditions below are true:

1.   Tape is loaded in the Reader.
2.   ASR is "on line".
3.   Reader level is in "START" position.
4.   No ASR Keyboard initiated character is being transmitted to the Controller.

1.4.1.2   TELETYPE WRITER STOP TAPE

1.4.1.2.1   Interrupt Inhibited Mode
This command issued within 22 milliseconds following a Controller "acknowledge" signal response to an EDI instruction stops tape reading after one additional character has been received.

This command issued later than 33 milliseconds following a Controller "acknowledge" signal response to an EDI instruction stops tape reading after two additional characters have been received.

1.4.1.2.2   Interrupt Allowed Mode
This command issued within 31 milliseconds following an interrupt request stops tape reading after two additional characters have been received.

1.4.1.3   INTERRUPT INHIBIT

1.4.1.3.1   Receiver Addressed
This command immediately suppresses an existing Receiver interrupt request signal, and prevents transmission of further interrupts. Any Receiver service required condition subsequent to this command is stored by the Receiver. (See section 1.4.2).

1.4.1.3.2   Transmitter Addressed

This command immediately suppresses an existing Transmitter interrupt request signal, and prevents transmission of further interrupts. Any Transmitter service required condition subsequent to this command is stored by the Transmitter. (See section 1.4.3).

1.4.1.4   Read Tape and Inhibit Receiver Interrupt

This command combines all requirements and functions discussed in paragraphs 1.4.1.2 and 1.4.1.3.1.

1.4.1.5   Stop Tape and Inhibit Receiver Interrupt

This command combines all requirements and functions discussed in paragraphs 1.4.1.2 and 1.4.1.3.1.

1.4.1.6   INTERRUPT ALLOWED

1.4.1.6.1   Receiver Addressed

Controller response to this command is immediate. A suppressed service required status (para. 1.4.1.3.1) if still valid, allows the controller to reissue the interrupt request. (See section 1.4.2).

1.4.1.6.2   Transmitter Addressed

Controller response to this command is immediate. A suppressed service required status (para. 1.4.1.3.2) if still valid, allows the controller to reissue the interrupt request. (See section 1.4.3).

1.4.1.7   Read Tape and Allow Receiver Interrupt

This command combines all requirements and functions discussed in paragraphs 1.4.1.1 and 1.4.1.6.1.

1.4.1.8   Stop Tape and Allow Receiver Interrupt

This command combines all requirements and functions discussed in paragraph 1.4.1.2 and 1.4.1.6.2.

1.4.2   EDI INSTRUCTION

Controller execution of this instruction's "data in" request clears the Receiver interrupt request and service required status in both interrupt inhibited and interrupt allowed modes.

1.4.2.1   INTERRUPT INHIBITED MODE

An EDI instruction shall be issued at intervals not exceeding 8.8 milliseconds. ASR data may be lost if this interval is exceeded.

1.4.2.2   INTERRUPT ALLOWED MODE

An EDI instruction shall follow a Receiver interrupt request within 8.8 milliseconds. The Controller may discard this character after this time interval.

1.4.3   EDO INSTRUCTION

A Controller "acknowledge" response to this instruction's "Data Out" signal clears the Transmitter service required state in both interrupt inhibit and interrupt allowed operational modes. This response also clears the Transmitter interrupt request signal in the Transmitter Interrupt Allowed operational mode.

Failure of the Controller to "acknowledge" this data out request signals the CPU that the previous data byte punch operation is not finished.

1.4.4   EAI INSTRUCTION

1.4.4.1   Receiver

This instruction is ignored in the Receiver Interrupt Inhibit mode. The Controller Receiver will respond to the "Address In" signal only while the Receiver interrupt request is the highest active interrupt level. Response to this siganl terminates the Receiver interrupt request but does not clear the service required (EDI instruction) status.

1.4.4.2   Transmitter

This instruction is ignored in the Transmitter Interrupt Inhibit mode. The Controller Transmitter will respond to the "Address In" signal only while the Transmitter interrupt request is the highest active interrupt level. Response to this signal terminates the Transmitter interrupt request.

RAD HIGH SPEED PERFORATED TAPE CONTROLLER

1.0   SYSTEM DESCRIPTION

A Digitronics speed paper tape (HSPT) reader and/or punch may be used with the
LEC-16 computer for input/output communication. The Digitronics Model 2540
tape reader operates at a maximum rate of 300 characters per second, while the
Model 1560 punch operates at a maximum rate of 60 cps. The HSPT Controller
provides command, control, status and data buffering for communication with
LEC-16 Programmed Data Channel bus, PDC, and the reader and punch. Full
duplex operation is provided. This allows simultaneous output of data from the
computer to the tape punch, and input of data from the tape reader to the computer.

The HSPT controller communication with the PDC data bus is 8-bit parallel
transfer under computer control. The controller communication with the punch
and reader is also parallel 8-bit character transfer, with the controller providing
temporary data storage to achieve synchronism with the computer transfer timing.

1.1   Reader and Punch Operation

Both devices use 1 inch wide 8-level paper, mylar, or mylar-foil tape with light
transmissivity of 40% or less. Data ONE bits are represented by punched holes,
and ZEROES by no holes. Characters are perforated in EAI Standard punched
tape format, with 10 character per inch spacing.

The Model 2540 tape reader may optionally be supplied with a Model 6011A tape
handler to accommodate 175 feet of 4.5 mil, or 300 feet of 2.5 mil tape. The
Model 1560 punch may also be supplied with tape take-up spooling provisions, using
reels identical with the Model 6011A reels.

1.1.1   Tape Reader

(To be supplied later) (Tape char.)

1.1.2   Tape Punch

(To be supplied later)

1.2   Controller Operation

The HSPT Controller is divided into two functional sections - receiver, and transmitter.

The controller transmitter is assigned an even eight-bit binary station address (excluding an all-zero address). The associated receiver is assigned the next larger odd binary number address.

The receiver controls the starting and stopping of the tape reader in response to computer ECO instruction commands. It stores the 8-bit character sensed by the tape reader as a character passes the read head. This stored data is updated each time a new character is sensed. An EDI instruction "Data In" signal received during the time interval between successive characters causes the receiver to place the stored byte on the PDC data bus lines.

The transmitter accepts computer output in 8-bit parallel bytes (EDO instruction). The controller initiates one punch operation for each EDO data byte. The maximum data transfer rate is 60 bytes per second.

Each functional section can operate independently in two basic modes, program interrupt or non-interrupt. This is a programmer option with computer ECO command control as described in the LEC-17 reference manual. Full duplex input/output data transfers can be made in either operational mode. Each section contains its individual program interrupt level logic; each may utilize its own unique interrupt request line, or share a common interrupt request line in any precedence level order with other device controllers.

The operational status of each device is monitored by the controller. Two receiver status indicator, "Timing Error" and "Device Not Ready" (DNR), are placed on the PDC data bus in response to a signal. One transmitter status indicator, DNR, is similarily checked by a transmitter addressed "Status In" signal.

1.2.1   Program Interrupt Operation

The receiver transmits an interrupt signal to the CPU each time a new character has been received from the tape reader. This interrupt signal is maintained until the computer responds with a "Data In", "Address In", or "Status In" signal (EDI, EAI, or ESI instruction).

If an EDI "Data In" signal response to an interrupt is not made before a new character has been received from the reader, the "Timing Error" status indicator is set. Subsequent EDI instructions will not be acknowledged until this status indicator has been reset. The timing error status indicator is

reset by any receiver command (ECO instruction) on a "Status In" signal (ESI instruction). An EDI "Data In" signal received while the timing error status indicator is up, places the current contents of the receiver buffer on the PDC data bus lines and clears the interrupt request.

A "Read Tape" command (ECO instruction) issued while the Tape Reader is not operational (DNR status), is acknowledged and initiates an interrupt signal. This interrupt can be cleared by an EDI, EAI, or ESI instruction. The receiver does not respond to a "Data In" signal when a valid byte is not available for transfer.

The transmitter sends an interrupt signal to the computer each time a computer output byte has been transmitted to the punch. This interrupt signal is maintained until the computer outputs another byte (EDO instruction) or responds with an "Address In" or "Status In" signal (EAI or ESI instruction).

An EDO instruction "Data Out" signal issued while the tape punch is in DNR status (ref. section 1.3.5.2) is not acknowledged. The controller immediately issues an interrupt request; the output data byte is accepted however, and the controller performs a normal punch cycle sequence.

An interrupt signal initiated by the EDO "Data Out" signal while the punch DNR status indicator is set, is cleared by an EAI or ESI instruction.

The punch status indicator is reset by an ESI instruction after the "Device Not Ready" conditions have been cleared by manual intervention.

1.2.2   Non-Interrupt Operation

The receiver does not transmit an interrupt signal to the computer after receiving a character, and ignores an "Address In" (EAI instruction) signal. A "Data In" signal (EDI instruction) is acknowledged and a byte transfer made in response to the first "Data In" signal following the receipt of each character, except when this signal occurs after the reader has transmitted a new character. In this case the previous character is discarded and the data in signal is not acknowledged. The timing error status indicator is set and no further EDI instructions will be acknowledged until this status bit is cleared. Each "Data In" signal received while the timing error status signal is up, places the current contents of the receiver buffer on the PDC data bus lines.

The timing error status indicator is cleared by any receiver command (ECO instruction) or a "Status In" signal (ESI instruction).

A "Read Tape" command (ECO instruction) issued while the reader and/or tape handler are not ready (DNR status) is acknowledged, and an interrupt request initiated. An EDI following this interrupt is not acknowledged. The interrupt is cleared by an ESI or EAI instruction.

The transmitter acknowledges and accepts a "Data Out" signal (EDO instruction) and completes a punch cycle sequence. It does not send an interrupt signal after completing the punch operation, and does not respond to an "Address In" signal (EAI instruction). Another EDO instruction signal is not acknowledged or data transfer effected until the preceding data byte has been punched.

An EDO instruction "Data Out" signal issued with the punch DNR indicator set is not acknowledged. The data transfer is accepted, however, and the controller performs a normal punch cycle operation.

1.3 I/O INSTRUCTION

1.3.1   The ECO instruction performs as described in the LEC-16 Reference Manual. The M and N fields of the ECO instruction define the receiver or transmitter address. All valid commands are accepted and a controller "Acknowledge" signal returned.

The right byte of the A register defines the command. Two commands (para. 1.3.1.3 and 1.3.1.6) apply to either the receiver or transmitter section, as defined by the instruction M and N fields. Six commands apply to receiver functions only. The eight valid command words are defined below.

1.3.1.1   Read Tape - XX01

This receiver-addressed command initiates the reading of tape on the tape reader.

1.3.1.2   Stop Tape - XX02

This receiver-addressed command terminates the reading of tape after the next character has been received.

1.3.1.3   Interrupt Inhibit - XX04

This receiver or transmitter addressed command prevents the controller receiver or transmitter from issuing an interrupt request to the CPU regardless of data transfer requirements.

1.3.1.4   Read Tape and Inhibit Receiver Interrupt - XX05

This receiver addressed command initiates reading of tape and prevents the receiver from issuing an interrupt request.

1.3.1.5   Stop Tape and Inhibit Receiver Interrupt - XX06

This receiver addressed command terminates the reading of tape after the next character has been received, and prevents the receiver from issuing an interrupt request.

1.3.1.6   Interrupt Allowed - XX08

This receiver or transmitter addressed command allows the controller receiver or transmitter to issue an interrupt request to signify that a data input transfer is required.

1.3.1.7   Read Tape and Allow Receiver Interrupt - XX09

This receiver addressed command initiates the reading of tape and allows the receiver to issue an interrupt request to signify that a data transfer is required.

1.3.1.8   Stop Tape and Allow Receiver Interrupt - XX0A

This receiver addressed command allows the receiver to issue an interrupt request to signify that a data transfer is required, and terminates the reading of tape after the next character has been received.

1.3.2   EDI

The EDI instruction performs as described in the reference manual. The M & N fields of the EDI instruction define the controller receiver address. A "Data In" signal is transmitted to the controller. An "Acknowledge" signal from the controller signifies valid data has been placed on PDC data bus lines 8 through 15. Absence of an acknowledge signal signifies that data placed on the PDC data bus is invalid due to a timing error or the tape reader DNR status, or that a new data character has not been received since the previous EDI instruction transfer.

The most significant data bit is placed on line 8, in descending order with the LSB on line 15.

1.3.3   EDO

The EDO instruction performs as described in the reference manual. The M & N fields of the EDO instruction define the controller transmitter address. The right byte of the A register is placed on PDC data bus lines 8 through 15, with the byte MSB on line 8, in descending order, with the LSB on line 15. A "Data Out" signal is transmitted to the controller. An "Acknowledge" signal from the controller signifies data has been transferred. Absence of an "Acknowledge" signal signifies that the previous data transfer punch operation is not completed, or that the punch is in DNR status.

1.3.4   EAI

The EAI instruction performs as described in the reference manual. An "Address In" signal is transmitted on the PDC. When a controller interrupt request is active, the address of the section requesting service is placed on the PDC data bus lines 8 through 15. The address MSB is placed on line 8, in descending order with the LSB on line 15. The controller does not return an "Acknowledge" signal.

1.3.5   ESI

The ESI instruction performs as described in the reference manual. The M & N fields of the instruction define the controller device address. A "Status In" signal is transmitted to the controller. The controller places its status byte on PDC data bus lines 8 through 15 as defined below. The controller does not return an "Acknowledge" signal.

STATUS BYTE FORMAT

1.3.5.1   Device Not Ready (DNR)   HEX 40

This status byte from the receiver section signifies the Tape Reader is not fully operational as:

1)   Tape reader power is off, or
2)   Tape reader control switch is in LOAD position.

When the Model 6011A tape handler is installed, this status byte can also signify the handler is rewinding tape.

1.3.5.2   Device Not Ready (DNR)   HEX 40

This status byte from the transmitter section signifies that the Tape Punch is not fully operational as:

1)   Tape punch power is off, or
2)   Punch is out of tape, or
3)   Tape is within 2.5 inches of end of tape. (See section 1.4.5.2).

1.3.5.3   Timing Error   HEX 04

This receiver status byte signifies failure of the CPU to request a data in transfer (EDI instruction) before one or more tape characters have been received since the previous EDI instruction was executed.

1.4   Program Requirements

The normal controller operational mode is with receiver and transmitter
program interrupts allowed. An active interrupt request signal is cleared
at the completion of service by an EAI, EDI, ESI, or EDO instruction as
applicable. Each of these instructions shall be followed by an additional
instruction before a JRL instruction is executed to insure that this interrupt
level signal has dropped.

Certain programming restrictions are required to operate the receiver in the
interrupt inhibited mode. The tape reader and CPU timing are asynchronous,
and CPU service (EDI instructions) must be offered at a faster rate than tape
data characters are read to preclude timing errors.

1.4.1   ECO Instruction Commands

The A register contents must be limited to the eight valid command words
defined in Section 1.3.1.

1.4.1.1   Read Tape

This command initiates operation of the tape reader when conditions 1, 2, and
3 below are true:

    1)   Tape reader control switch is in "RUN" position.
    2)   Tape spooler power switch is in "ON" position.
    3)   Tape spooler rewind switch is in "OFF" position.

The tape reader is in DNR status when any of the above three conditions are
not true.

This command resets the timing error status indicator.

The tape reader reads a minimum of two tape characters in response to this
command.

1.4.1.2   Stop Tape

The controller stores this command. The command is executed after the
next tape character has been received. This data is stored in the receiver
data buffer and held until a "Data In" (EDI instruction) signal transfers the
byte to the PDC data bus.

The stop tape command must follow within 100 microseconds after the receiver
has acknowledged a "Data In" signal (EDI instruction), which complies with the
requirements of section 1.4.2, to insure stopping tape reading on the following
character.

This command also clears the timing error status indicator.

1.4.1.3   INTERRUPT INHIBIT

1.4.1.3.1   Receiver Addressed

This command immediately suppresses an existing receiver interrupt request signal, and prevents transmission of further interrupts. Any receiver service required condition subsequent to this command is stored by the receiver. (See section 1.4.2). This command also clears the timing error status indicator.

1.4.1.3.2   Transmitter Addressed

This command immediately suppresses an existing transmitter interrupt request signal, and prevents transmission of further interrupts. Any transmitter service required condition subsequent to this command is stored by the transmitter. (See section 1.4.3).

1.4.1.4   Read Tape and Inhibit Receiver Interrupt

This command combines all requirements and functions discussed in paragraphs 1.4.1.2 and 1.4.1.3.1.

1.4.1.5   Stop Tape and Inhibit Receiver Interrupt

This command combines all requirements and functions discussed in paragraphs 1.4.1.2 and 1.4.1.3.1.

1.4.1.6   INTERRUPT ALLOWED

1.4.1.6.1   Receiver Addressed

Controller response to this command is immediate. A suppressed service required status (para. 1.4.1.3.1) if still valid, allows the controller to reissue the interrupt request. (See section 1.4.2). This command also clears the timing error status indicator.

1.4.1.6.2   Transmitter Addressed

Controller response to this command is immediate. A suppressed service required status (para. 1.4.1.3.2) if still valid, allows the controller to reissue the interrupt request. (See section 1.4.3).

1.4.1.7   Read Tape and Allow Receiver Interrupt

This command combines all requirements and functions discussed in paragraphs 1.4.1.1 and 1.4.1.6.1.

1.4.1.8   Stop Tape and Allow Receiver Interrupt

This command combines all requirements and functions discussed in paragraph 1.4.1.2 and 1.4.1.6.2.

1.4.2   EDI Instruction

Controller execution of this instruction "Data In" request, clears the receiver service required state in both interrupt inhibit and interrupt allow modes.

Failure of the controller to acknowledge this data in request signals the CPU that valid data is not being transferred. (See section 1.3.2 and 1.4.5).

1.4.2.1   Interrupt Inhibited Mode

An EDI instruction shall be issued at intervals not exceeding 3 milliseconds. Invalid data may be transfered if this interval is exceeded, and reader timing error status indicator set.

1.4.2.2   Interrupt Allowed Mode

The minimum time between tape characters is 3.0 milliseconds. CPU operation at higher priority program levels for continous periods approaching 3,000 machine cycles may suppress the receiver interrupt request signal until a new tape character has been received, and reader timing error status set. Programming must preclude this possibility to avoid tape data loss.

1.4.3   EDO Instruction

A controller "Acknowledge" response to this instruction's "Data Out" signal clears the transmitter service required state in both interrupt inhibit and interrupt allowed operational modes. This response also clears the transmitter interrupt request signal in the Transmitter Interrupt Allowed operational mode.

Failure of the controller to "Acknowledge" this data out request signals the CPU that the previous data byte punch operation is not finished, or that the punch is in DNR status. (Sections 1.3.3 and 1.4.5).

1.4.4   EAI Instruction

1.4.4.1   Receiver

This instruction is ignored in the Receiver Interrupt Inhibit mode. The controller receiver will respond to the "Address In" signal only while the receiver interrupt request is the highest active interrupt level. Response to this signal terminates the receiver interrupt request but does not clear the service required (EDI instruction) status, timing error indicator, or device not ready status.

1.4.4.2   Transmitter

This instruction is ignored in the Transmitter Interrupt Inhibit mode. The controller transmitter will respond to the "Address In" signal only while the transmitter interrupt request is the highest active interrupt level. Response to this signal terminates the transmitter interrupt request.

1.4.5   ESI Instruction

The controller will respond to the "Status In" signal each time the ESI instruction is executed. Response to this "Status In" signal clears the interrupt request and status indicator of the device addressed.

1.4.5.1   Status words placed on the right byte PDC data bus lines in response to a receiver addressed ESI instruction "Status In" signal following an unacknowledged "Data In" signal (EDI instruction), have the following significance:

    1)   HEX 00:   Lack of acknowledgement because a new tape character has not yet been received since previous data transfer to CPU.

    2)   HEX 04:   Lack of acknowledgement due to timing error. Data on PDC bus is not tape character following previous data transfer to CPU.

    3)   HEX 40:   Lack of acknowledgement due to tape reader not operational. Manual intervention is required.

1.4.5.2   Status words placed on the right byte PDC data bus lines in response to a transmitter addressed ESI instruction "Status In" signal following an unacknowledged "Data Out" signal (EDO instruction) have the following significance:

    1)   HEX 00:   Lack of acknowledgement due to transmitter still busy with transfer of previous data byte to punch.

    2)   HEX 40:   If preceding data out signals have been acknowledged, tape is within 2.5 inches of end. Data transfer from unacknowledged EDO signal is being punched, and one more data out transfer can be accepted and punched after the next interrupt request is issued.

    3)   HEX 40:   If initial EDO instruction "Data Out" signal is not acknowledged, cause is one or more of the following conditions requiring manual intervention:
    a. Punch power off.
    b. Out of tape.
    c. Within 2.5 inches of end of tape.

EXTERNAL DATA INPUT CHANNEL (EDIC)

1.   System Description

A primary communication link with MAC 16 computer and any external device
is through the Program Data Channel (PDC). The External Data Input Channel
(EDIC) provides a standard interface between MAC 16's PDC and external
input devices. The input device may be an External Output Data Channel
(EDOC) located in another CPU. Thus, communication between computers can
be established. One printed circuit board (EIC) contains the necessary control
and logic functions for fully buffered sixteen bit words from two devices.

2.   Operation of Controller

The controller interface with the CPU is compatible with the PDC and will
accept valid command signals, input data, and operate in either interrupt
allow or interrupt inhibit modes. An acknowledge signal is returned upon
successful transfer of a data word or acceptance of a valid ECO.

The signals are transmitted to and received from the device with TTL logic
gates. The controller may function with an external device by one of three
methods: (1) with busy/ready signals, (2) without ready signal, and (3)
direct access.

2.1   Busy/Ready Signals

This provides for the transfer of a series of data words that are produced by
the device upon demand of the controller. The controller will accept data
from the device and return a busy signal which indicates the data has been
accepted. The controller will remain busy until the data has been transferred
to the CPU. After transfer to the CPU, the controller will issue a not busy
signal to the device and accept data if or when the device has a new word for
transfer and has indicated with a ready signal.

The busy and ready signals can be in either level or pulse mode and are inde-
pendent of one another, thereby offering four useful combinations.

External Data Input Channel (EDIC)

2.1.1   Pulse Mode

The input (ready) pulse may be either a positive or negative going pulse. The negative going edge clears a flip-flop that indicates the device is ready to transmit a new data word.

The controller issues two negative going pulses approximately 500 nanoseconds wide. These pulses on separate output lines are: (1) when the controller register information is transferred to the CPU signifying it is not busy, and awaiting data, and (2) when the controller has accepted a new data word signifying it is busy.

2.1.2   Level Mode

In the level mode of operation, a low level on the ready line indicates the device is ready to send data. A high level indicates the device is not ready.

The output (busy) line to the device is high when busy and low when not busy.

2.2   Without Ready Signal

In the event the device used cannot issue a ready signal, a bypass jumper (ready bypass) may be used. The controller will sample the input data lines each microsecond. The information stored during the SOA clock pulse prior to an EDI is placed on the data bus.

2.3   Direct Access

During an ESI command, the information on the device data lines will be placed on the PDC data bus. Direct access by this means is possible whether or not the busy ready signals are used.

3.0   I/O Instruction

3.1   External Command Out (ECO)

MN Field

All eight bits of the MN field define the controller address. The following restrictions are placed on the two least significant bits:

        J15N-N must be "1" (odd address only)
        J14N-N defines channel A or B
                "0" = Channel A
                "1" = Channel B

Accumulator Contents

Only two output commands will initiate controller action. The least significant eight bits of the accumulator contents are decoded.

XX04 Interrupt Inhibit: This command prevents the controller from issuing an interrupt request to the CPU regardless of the data transfer requirements and immediately suppress an existing interrupt request.

XX08 Interrupt Allowed: This command allows the controller to issue an interrupt request. An interrupt request signal signifies the device is ready and a data transfer is required.

Acknowledge

An Acknowledge will always be returned for the two valid commands regardless of data transfer requirements.

Service Request

An interrupt inhibit ECO will always drop the service request. An interrupt allow ECO does not issue a service request but if the data buffer register is "empty", a service request will be issued shortly after acknowledging this ECO.

3.2 External Data Output (EDO)

The EDO instruction is not a valid command and will be ignored.

Acknowledge

An EDO will not be acknowledged.

Service Request

There will be no change in the service request signal.

3.3 External Status In (ESI)

MN Field

All eight (8) bits of the address field specify the device address.

Accumulator

The information on the device data lines are transferred to the accumulator over the PPC data bus.

Acknowledge

An ESI will not be acknowledged.

Service Request

The service request signal will not change.

External Data Input Channel (EDIC)

3.4   External Address In (EAI)

MN Field

The MN field is not used in the controller response to an EAI.

Accumulator Contents

The contents of the accumulator is the address of the device if it has issued a
service request and has the highest precedence.

Acknowledge

An acknowledge is not issued for an EAI.

Service Request

The service request signal will be dropped.

3.5   External Data In (EDI)

MN Field

All eight (8) bits of the address field specify the device address.

Accumulator Contents

If an acknowledge has been received, the contents of the accumulator is the
data word stored in the buffer register during the last "word transfer" from
the device. If an acknowledge is not received, the contents of the accumu-
lator is zero.

Acknowledge

An acknowledge will be issued if the controller has a data word to be trans-
ferred to the computer.

Service Request

The issuance of an Acknowledge signal will cause an existing service request
to be dropped. The service request will be reissued when the controller has
a new word for transfer.

If the controller is in the interrupt inhibit mode, data strobed into the register
will not cause a service request to be issued.

EXTERNAL DATA OUTPUT CHANNEL (EDOC)

1. System Description

A primary communication link with the MAC 16 computer and any external device is through the Program Data Channel (PDC). The External Data Output Channel (EDOC) provides a standard interface between MAC 16 and external devices. One board contains the necessary control and logic functions for fully buffered outputs to two external devices.

1.1 Operation of Controller

Any device that accepts and receives signals compatible with TTL logic and performs the following functions can be connected to an EDOC.

a. Accept data only when the ready signal is active.
b. Send a not busy signal only when the device is able to accept data.

There are two lines available for status signals which may be used.

1.2 I/O Instruction

1.2.1 ECO

The Controller will respond to only two commands, Interrupt Inhibit and Interrupt Allowed. These valid commands are accepted and an acknowledge signal is returned.

The right byte of the A register defines the command.

1.2.1.1 Interrupt Inhibit XX04

This command prevents the controller from issuing an interrupt request to the CPU regardless of the data transfer requirements.

1.2.1.2 Interrupt Allowed XX08

This command allows the Controller to issue an interrupt request to signify the device is not busy and a data transfer is required.

1.2.1.3 Invalid Commands

If the Controller is in the interrupt mode an invalid command will cause the controller to drop its

service request. If the controller is in the non-interrupt mode an invalid command will not result in any changes in output levels. The controller will not acknowledge an invalid command.

1.2.2 EDO

The External Data Output instruction performs as described in the reference manual. The M and N fields on the PDC address bus are decoded and allow the contents of the A register to be strobed in. Data transfer can be accomplished in the interrupt inhibit mode or interrupt allowed mode. Upon successful transfer of data an acknowledge signal is sent to the CPU.

1.2.2.1 EDO with Interrupt Inhibited

The acknowledge response in this mode sets a busy FF and signals the device data is ready. The device indicates acceptance of this data by issuing a not busy signal which resets the busy FF. If the device is busy, the device is inoperative etc. the EDO will not be acknowledged. A means of bypassing the busy FF is provided.

1.2.2.2 EDO with Interrupt Allowed

The acknowledge response in this mode sets a busy FF, signals the device data is ready and clears the service request. The device indicates acceptance of the data by issuing a not busy signal which resets the busy FF and sends a service request to the CPU. Failure of the controller to acknowledge an EDO signifies the last data word is still in the controller register, the device is busy, the device is off line, etc. A means of bypassing the busy FF is provided.

1.2.3 ESI

The External Status In instruction performs as described in the reference manual. A status in signal transmitted to the controller places the status of the device addressed on the PDC data bus lines 14 and 15. The status bits are defined by the particular device used. The controller does not return an acknowledge signal.

1.2.4 EAI

The External Address Input instruction performs as described in the reference manual. When an address in signal is transmitted with the interrupt request active, the address of the section requesting service is placed on the PDC data bus lines 8 through 15. The address MSB is on line 8, in descending order with the LSB on line 15. The controller does not return an acknowledge signal.

1.2.5 EDI

The External Data Input instruction is not valid. If the controller is in the interrupt mode it will cause the service request to be dropped. In the non-interrupt mode no changes in output levels will occur. An EDI instruction will not be acknowledged.

1.3 Program Requirements

The normal mode of operation is with the controller in the interrupt allowed mode. An active interrupt request signal is cleared at the completion of service by an EAI, ESI or EDO instruction. Each of these instructions shall be followed by an additional instruction before a JRL instruction is executed to insure that this interrupt level signal is dropped.

1.3.1 ECO Instruction

The A register's contents must be limited to the two valid command words defined in paragraph 1.2.1.

1.3.1.1 Interrupt Allowed

This command immediately raises the interrupt signal providing the device is not busy or at the time the device becomes not busy.

1.3.1.2 Interrupt Inhibit

This command immediately suppresses an existing interrupt request and prevents the transmission of further interrupts.

1.3.2 EDO Instruction

The acknowledge response to this instruction clears the service request. Failure of the controller to acknowledge this data output command signals the CPU that the previous operation is not completed or the device is in a not ready status. After the controller has accepted data and the device has completed its output operation the not busy signal raises the service request.

1.3.3 ESI Instruction

The controller will respond to the status in signal each time the ESI instruction is executed by placing the status of the device on the last two bits of the PDC data bus. The service request is cleared at this time.

1.3.4 EAI Instruction

In the interrupt inhibit mode the External Address Input command is ignored. There will be a response, in the interrupt mode, only if the interrupt request is the highest active interrupt level. The address in signal clears the interrupt request and places the device address on the PDC address bus.

1.3.5 EDI Instruction

This is not a valid command for an output device. A data in signal will clear any existing service request.

DCA, DCB DISC/DRUM CONTROLLER

1.0   System Description
The Disc/Drum Controller provides command control and data buffering between the MAC 16 computer and any of the Vermont Research Corporation Drums or Discs using the standard VRC interface. The controller has the capability of controlling two Discs/Drums each with the following characteristics:

1.1   Capacity

Minimum –   32,768 16 bit words
Maximum – 4,194,304 16 bit words

Expansion from minimum to maximum is in several increments, and the elements required for expansion are field expandable. When the controller is operating with two Discs/Drums, both units must have the same number of tracks.

1.2   Data Transfer Rates

The data rate between controller and the Disc/Drum is at a bit rate of approximately 2 Mhz. The data rates between the computer and the controller is variable in the following manner:

     1:1 Word Interlace – 62,000 Word/Sec.
     2:1 Word Interlace – 31,000 Word/Sec.
     4:1 Word Interlace – 15,500 Word/Sec.
     8:1 Word Interlace – 7,750 Word/Sec.
    16:1 Word Interlace – 3,875 Word/Sec.

These various data rates are achieved by the same controller using different word interlace ratios. The change in interlace ratio is accomplished by a change in the back plane wiring of the DCA board. This variation in data rate allows the controller to be used at low rates on the PDC, higher rates on the MDC and the SDC.

2.0   I/O Instructions

2.1   ECO

MN Field – Device Address
The most significant five (5) bits of the address field specifies the Disc/Drum Controller address. The least significant three (3) bits define the controller operation modes.

J13N – Inhibit Interrupt/Allow Interrupt

J14N – Write

J15N – Read

The six operation modes are:

000 – Allow Interrupt

001 – Allow Interrupt - Read

010 – Allow Interrupt - Write

100 – Inhibit Interrupt

101 – Inhibit Interrupt - Read

110 – Inhibit Interrupt - Write

Accumulator Contents – Sector Address

The contents of the Accumulator specifies the address of the starting data sector.
The sector size is normally 64 data words, except in the case of the two largest
VRC units having 20 inch diameter drums where the sector size is 128 words.

The least significant 15 bits provide an address range of 0–32,767 sectors which
allow 4 M words of memory capacity per unit; Bit O selects which unit.

Acknowledge

Acknowledge will be issued if the controller is not "busy", i.e. not performing a
previously specified Read or Write Command. However, the controller will
accept/acknowledge an Allow or Inhibit Interrupt only mode command when busy,
Acknowledge will not be issued when the Disc/Drum heads are not actuated.

Service Request

The controller does not issue a Service Request in response to an ECØ. However,
in the case of an Allow Interrupt-Write operation, since the data buffer register will
be initially "empty", a Service Request will be issued shortly after acknowledging
this ECØ.

In the case of an Allow Interrupt-Read operation, after the command is terminated
and after the controller has completed all required operation steps and is now capable
of accepting an EDI, it will issue a Service Request.

DCA, DCB, Disc/Drum Controller

If a Service Request is active and an ECØ is accepted and acknowledged, the Service Request is dropped

Operation

Read and Write operations are continuous starting with the first word of a specified sector until "terminated." The termination of a command is determined by the failure of the CPU to respond to a data transfer Service Request within the Controller data word holding time.

2.2   EDØ
        MN Field – Device Address

The most significant five (5) bits of the address field specifies the Disc/Drum Controller address. The least significant three (3) bits are disregarded.

Accumulator Contents – Output Data

The contents of the Accumulator is the data word to be stored at the next location on the Disc/Drum.

Acknowledge

Acknowledge will be issued if the controller can accept the data and store it on the Disc/Drum.

Service Request

The Controller shall issue a Service Request to the CPU, if in the Interrupt Allowed mode, when the data word buffer of the Controller can accept data.

If a Service Request is active, and an EDØ for this Controller is received and acknowledged, the Service Request is dropped.

If Service Request is active and a Timing Error occurs, the Service Request will remain active and the Controller will assume the data transfer to be completed. This action is a termination of the transfer and the Controller will initiate such steps as required to complete this command and to accept the next ECØ, EAI or ESI command.

Operation

The Controller will accept the data word presented and will record that word on the Disc/Drum with odd parity. The Controller will write the first word transferred to it in the first word location of the sector specified. It will continue recording data in sequential locations until terminated. The last word transferred to the Controller

prior to termination will be the last word written.

Recording a sufficiently large data block will require the Controller to change both sector and track addresses of the Disc/Drum with no loss of Disc/Drum latency.

2.3 EDI

MN Field - Device Address

The most significant five (5) bits of the address field specifies the Disc/Drum Controller address. The least significant three (3) bits are disregarded.

Accumulator Contents - Input Data

If an acknowledge has been received, the contents of the Accumulator is the data word stored at the last location accessed on the Disc/Drum. If an acknowledge is not received, the contents of the Accumulator is zero.

Acknowledge

Acknowledge will be issued if the Controller has a data word to be transferred to the computer.

Service Request

The Controller shall issue a Service Request to the CPU, if in the Interrupt Allowed mode, when the data word buffer of the Controller has data to transmit to the CPU.

If a Service Request is active and an EDI for the Controller is received and acknowledged, the Service Request is dropped. If the Service Request is active and a Timing Error occurs, the Service Request will remain active and the Controller will assume the data transfer to be completed. This action is a "termination" of the transfer and the Controller will initiate such steps as required to complete this command and to prepare to accept the next ECØ, EAI, or ESI command.

Operation

The Controller reads the data words in sequence starting with the first word of the sector addressed. It will continue to read data until terminated or until a Parity Error is detected. A Parity Error will initiate a termination of the command.

Reading a sufficiently large data block will require the Controller to change both sector and track addresses of the Disc/Drum with no loss of Disc/Drum latency.

2.4 ESI
MN Field – Device Address

The most significant five (5) bits of the address field specifies the Disc/Drum Controller address. The least significant three (3) bits are disregarded.

Accumulator Contents – Input Status

The unique bits of the Accumulator specifies the status of the Controller and of the Disc/Drum System.

        Bit 0 –
            1 –
            2 –
            3 –
            4 –
            5 –
            6 –
            7 –
            8 – Controller Busy
            9 – Device Not Ready
           10 – Parity Error
           11 – Write Lockout Error
           12 –
           13 – Timing Error/Termination
           14 – Out of Synchronization
           15 – Illegal Address Selected

Acknowledge

Acknowledge is not issued for an ESI.

Service Request

If a Service Request is active and an ESI for this Controller is received, Service Request shall be dropped.

2.5 EAI
MN Field

The MN field is not used in the Controller response to an EAI.

Accumulator Contents – Device Address

The contents of the Accumulator is the address of the Disc/Drum Controller if it has issued a Service Request and has highest precedence.

Acknowledge

Acknowledge is not issued for an EAL.

Service Request

Service Request is not issued for an EAI.

If a Service Request is active and an EAI is received where the Controller responds with its address, the Service Request will be dropped.

LINE PRINTER CONTROLLER

1.0   SYSTEM DESCRIPTION

The Data Products Model 2310 Line Printer prints any character of a 64-character
set from 356 80-column lines per minute to 1110 20-column lines per minute.
(See Paragraph 6.0 for character set definition).

1.1   Operator's Control Panel

The operator's control panel is as follows:

1.   Indicators
      Power – illuminated when power is on.
      Ready – illuminated when power is on, all interlocks are closed and
          paper is loaded.
      On Line – illuminated when printer is in the ready condition and the
          On Line switch has been actuated.

2.   Switches
      On Line/Off Line – A three-position momentary action toggle switch.
      The upper position of the switch puts the printer On Line and illuminates
      the On Line indicator. The outer position, where the actuator normally
      rests, is a null position. The lower position puts the printer Off Line
      and extinguishes the On Line indicator. In order to put the printer On
      Line, the Ready indicator must be illuminated.

      Paper Step – A momentary contact toggle switch that advances the
      paper one line. This switch is disabled when the printer is On Line.

      Top of Form – A momentary contact. Top of Form position is defined
      as paper perforation aligned with plainly marked line located above the
      print station.

1.2   Maintenance Panel

The Maintenance Panel is as follows:

1.   Indicators
       Drum Gate – illuminated when drum gate is unlatched.

       Paper Fault – illuminated when paper is torn or missing.

       Print Inhibit – illuminated when print inhibit siwtch is on.

2.   Switches
       Main Power Switch – circuit breaker which provides operator power
       control.

       Master Clear Switch – momentary toggle switch that initializes all
       control functions.

       Print Inhibit Switch – inhibits hammer drivers, otherwise the printer
       functions.

1.3   Paper Handling

The printer handles standard edge punched paper with widths up to 9-7/8", the
length must be 11" long.

To load paper, swing drum gate open and place paper in Top of Form position.
The left tractor does not move. The right tractor adjust for paper width and
horizontal paper tension. Vertical paper tension is automatically provided upon
closing drum gate.

2.0   ECO

A.   <u>MN Field</u>

       All eight bits are utilized for address determination.

B.   <u>Acknowledge and Operation Modes</u>

       Valid Operation Modes:
            XX04 – Inhibit Interrupt – Acknowledge
            XX08 – Allow Interrupt – Acknowledge

C. Service Request

    1. The controller shall not issue a Service Request in response to an ECO.

    2. The controller, if in Allow Interrupt mode, shall issue a Service Request upon controller buffer empty.

    3. If Service Request is active and an ECO which inhibits interrupt is accepted and acknowledged, the Service Request shall be dropped.

3.0 EDO

A. MN Field

All eight bits are utilized for device address determination.

B. Accumulator Contents

If an acknowledge has been received, the word in the accumulator has been transferred to the controller for output to printer. The left byte shall be odd numbered print column and the right byte shall be even numbered print column, provided a NOP character has not been issued.

C. Acknowledge

Acknowledge shall be issued if controller accepts data word.

D. Service Request

If Service Request is active and EDO is accepted and acknowledged, the Service Request shall be dropped.

4.0 ESI

A. MN Field

All eight bits are utilized for device address determination.

B. Accumulator Contents

"A" Register bit 15 shall set to "1" when printer is not ready. These conditions are: 1) power off, 2) drum gate open, 3) paper not loaded, 4) overtemperature condition exists in paper drive motor, 5) printer not on-line.

C.   Acknowledge

There is no acknowledge issued for ESI.

D.   Service Request

If Service Request is active and ESI with correct address is issued, Service Request will be dropped.

5.0   EAI

A.   MN Field

The MN field is not used in the controller response to an EAI.

B.   Accumulator Contents

The contents of Accumulator is address of Line Printer Controller if it has issued a Service Request and has highest precedence.

C.   Acknowledge

There is no acknowledge issued for EAI

D.   Service Request

Service Request shall be dropped if active and has highest precedence.

6.0   Line Printer Program Notes

The printer buffer is a 20-character buffer and printer will print automatically upon receiving 20th character and advance to next 20 character zone.

To print less than 20 characters, it is necessary to issue a Format Control Character. The Format Control Characters are Paper Feed, Form Feed, Carriage Return which will cause the print out of any characters in print buffer, perform their given function, and return count to first print character.

The coded character set is a modified version of American Standard Code for Information Interchange (ASCII) as follows:

b7 b6 b5	0 0 0	0 1 0	0 1 1	1 0 0	1 0 1
b4 b3 b2 b1					
0 0 0 0		Space	Ø	@	P
0 0 0 1		!	1	A	Q
0 0 1 0		"	2	B	R
0 0 1 1		#	3	C	S
0 1 0 0		$	4	D	T
0 1 0 1		%	5	E	U
0 1 1 0		&	6	F	V
0 1 1 1		'	7	G	W
1 0 0 0		(	8	H	X
1 0 0 1		)	9	I	Y
1 0 1 0	PF	*	:	J	Z
1 0 1 1		+	;	K	[
1 1 0 0	FF	'	<	L	◊
1 1 0 1	CR	-	=	M	]
1 1 1 0		.	>	N	∧
1 1 1 1		/	?	0	♡

The "A" Register will be as follows:

"A" Register Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	X	B7	B6	B5	B4	B3	B2	B1	X	B7	B6	B5	B4	B3	B2	B1

A no operation character is defined as not advancing the print position. This character is any byte that B1 through B7 equals zero.

If in Allow Interrupt mode, failure of an EDO to acknowledge in response to service request should occur only when the line printer went into the not ready condition. The not ready condition occurs whenever the line printer is placed in off-line mode, or the drum gate open, or paper missing or torn.

The minimum time possible for service request after issuing EDO is two microseconds. The typical time will be 10 microseconds until 20 characters are received or format control character is issued.

CRC CARD READER CONTROLLER

1.0   SYSTEM DESCRIPTION

Data Products SR-300 Punched Card Reader photoelectrically reads column by column standard 80 column punched cards at the maximum rate of 300 cards per minute. The CRC Card Reader Controller provides command, control and data buffering for communication with the MAC 16 Programmed Data Channel (PDC).

1.1   Card Reader Control Panel

A.   There are four control switches whose functions are:

1) Power On – Supplies power to Card Reader
2) Power Off – Eliminates power to Card Reader
3) Start – Drive Motor on and Read Process ready
4) Stop – Drive Motor off

B.   There are four indicators whose functions are:

1) Ready – illuminate when Card Reader ready
2) Read – Illuminate when Read Check error occurs
3) Feed – Illuminate when Feed Check error occurs
4) Hopper – Illuminates when input hopper empty or output stacker full

1.2   Loading Procedure

A.   The input hopper capacity is maximum of 600 cards. When input hopper has less than 200 cards the card weight must be used.

B.   The output stacker capacity is maximum of 600 cards. Cards may be removed from stacker while Card Reader is in operation.

2.0   ECO

A.   <u>MN Field</u>
All eight bits are utilized for device address determination.

B.   <u>Acknowledge and Operation Modes</u>
There are 11 valid operation modes, five of which are unconditional with all others conditional on Card Reader ready and not busy.

These operation modes are as follows:

XX01 – Read one card – acknowledge if not busy.
XX05 – Read one card, inhibit interrupt – acknowledge if not busy
XX09 – Read one card, allow interrupt – acknowledge if not busy
XX02 – Read continuous – acknowledge if not busy
XX06 – Read continuous, inhibit interrupt – acknowledge if not busy
XX0A – Read continuous, allow interrupt – acknowledge if not busy
XX10 – Stop continuous read – acknowledge
XX14 – Stop continuous read, inhibit interrupt – acknowledge
XX18 – Stop continuous read, allow interrupt – acknowledge
XX04 – Inhibit interrupt – acknowledge
XX08 – Allow interrupt – acknowledge

C.   Service Request
1) The CRC shall not issue a Service Request in response to an ECO.
2) The CRC, if in Allow Interrupt mode, shall issue a Service Request upon receiving each character from Card Reader.
3) The CRC, if in Allow Interrupt mode, shall issue a Service Request for each error that occurs.
4) If Service Request is active and an ECO is accepted and acknowledged, the Service Request shall be dropped.

3.0   EDI

A.   MN Field
All eight bits are utilized for device address determination.

B.   Accumulator Contents
If an acknowledge has been received, the contents of the Accumulator shall be the last character read by Card Reader. This character shall have the following format:

"A" Register Bit	4	5	6	7	8	9	10	11	12	13	14	15
Card row		12	11	0	1	2	3	4	5	6	7	8	9

If an acknowledge is not received the contents of accumulator is zero.

C.   Acknowledge
Acknowledge shall be issued if CRC has a word to be transferred to computer.

D.   Service Request
The CRC, if in Allow Interrupt mode, shall issue a Service Request upon receiving each character from Card Reader. If Service Request is active and an EDI is accepted and acknowledged, the Service Request shall be dropped.

4.0   ESI

A.   MN Field
All eight bits are utilized for device address determination.

B.   Accumulator Contents

        "A" Register Bit

        15   - Set to "1" when Card Reader not ready. These conditions are·
                                    1) Transport jam, 2) non-feed, 3) stacker jam, 4) stacker
                                    full, 5) hopper empty, 6) false feed, 7) power off, 8) test
                                    mode, 9) open interlock, 10) START switch depressed.

                                    Operator action is required to clear above inoperable conditions.

        14   - Set to "1" when Card Reader has Read Check. These conditions
                                    are 1) unacceptable light and dark responses of data photo
                                    sensors, 2) misregistration of card. This error is corrected
                                    by operator depressing START switch on Card Reader.

        13   - Set to "1" when Card Reader has Feed Check. This condition
                                    is 1) card does not reach read station, 2) card does not pass
                                    through read station in the specified time. The drive motor will
                                    be stopped, thereby requiring operator action.

        12   - Set to "1" when overrun condition occurs. This condition
                                    is failure to execute EDI before next column is read. This
                                    error flip flop is reset by CRC acceptance of ECO or by ESI
                                    command.

C.   Acknowledge
        There is no acknowledge issued for ESI.

D.   Service Request
        If Service Request is active and an ESI with correct address is received, Service
        Request shall be dropped.

5.0   EAI

A.   MN Field
        The MN field is not used in the CRC response to an EAI.

B.   Accumulator Contents
        The contents of Accumulator is address of CRC if it has issued a Service Request and
        has highest precedence.

C.   Acknowledge
        Acknowledge is not issued for EAI.

D.   Service Request
        If service request is active and CRC has highest precedence the Service Request shall
        be dropped.

6.0   CARD READER PROGRAM NOTES

A.   Card Feed Rate and Data Rate
         The Card Reader feeds 300 cards per minute or one card every 200 milliseconds. There-
         fore, when utilizing Read One Card Command it will be approximately 200 milliseconds
         between acceptance of this command.

         Stop Continuous Read Command may be executed any time between reading of Column 1
         through Column 80 to prevent next card feed. If Stop Continuous Read Command is
         issued after Column 80, the next card may be fed.

         The time from issue of Read One Card Command to presence of Column 1 in Controller
         ready for transmission to Conputer is approximately 40 milliseconds. Thereafter from
         Column 1 through Column 80 the characters will be ready for transmission to computer
         approximately 2 milliseconds apart.

B.   Card Reader Feed Control
         The Card Reader Feed Control flip flops are reset whenever the Card Reader is
         inoperable and feed control ECO will not acknowledge. Therefore when these conditions
         occur an ECO must be issued to continue reading when the error condition is corrected.

         In the absence of these error conditions, ECO's may be issued utilizing the valid
         operation codes described in ECO description. Further, an EDI will not acknowledge
         when Card Reader is inoperable. Note: overrun condition is considered an inoperable
         condition.

C.   Card Reader Status
         Card Reader Status may be determined by execution of ESI command at any time. See
         ESI command definition. Whenever ECO does not acknowledge and ESI shows no error,
         Card Reader is busy reading card.

MAGNETIC TAPE CONTROLLER - 9 Track

1.   SYSTEM DESCRIPTION

The system is capable of generating or reading a nine (9) track IBM compatible magnetic tape.

1.1   Tape Transport Description

The PEC model 6840-9 is a nine track, single capstan drive, 25 inch per second tape transport capable of reading and writing 800 characters per inch. The data transfer rate is one character per 50 microseconds. (20K Hz)

The control panel contains the following operator controls and indicators:

Power
Alternate action pushbutton switch/indicator for AC power.

Load
A momentary action pushbutton switch/indicator which on first operation applies tension to the tape and allows manual load or rewind command and on second operation advances tape to beginning of tape (BOT) marker.

Rewind
A momentary action pushbutton switch/indicator that is enabled only when the tape unit is off line and will rewind tape at 150 ips to BOT when depressed. If already at BOT then tape will rewind completely.

On Line
A momentary action pushbutton switch/indicator that alternately places the unit on line or off line each time it is depressed.

Write Enable
Indicator only that is illuminated when power is on and a reel of tape with a write enable ring is mounted on the transport.

Forward

An alternate action pushbutton switch/indicator which is enabled in the off line mode will alternately move tape forward at 25 ips or stops tape each time it is depressed.

Reverse

An alternate action pushbutton switch/indicator which is enabled in the off line mode will alternately move tape in the reverse direction at 25 ips or stop tape each time it is depressed.

The maximum tape capacity of this machine is 2400 feet on a 10-1/2 inch reel.

1.2   Controller Description

Two printed circuit boards, MTC and MTD containing approximately 160 integrated circuit packages, incorporate the logic and timing functions required.

The controller can be interfaced with the MAC-16 computer using either the programmed data channel (PDC) or the multiplex data channel (MDC). When on the PDC the controller may operate in either the interrupt inhibit or interrupt allow modes. Data may be transferred in either word or byte format. The transfer rate is 20,000 bytes per second or 10,000 words per second. Failure to transfer within the required time will cause loss of data in which case an error indicator is set.

The controller will be capable of communicating (on an individual basis) with up to four (4) tape units. Information is transferred between controller and tape unit, eight (8) bits (one byte) at a time at a 20K Hz rate. A parity bit generated by the controller is also transferred and recorded.

Data will be recorded in IBM Compatible Nine (9) Track Format. The Cyclic Redundancy Check (CRC) character will be recorded, but the controller will not be able to read the CRC or perform an error correction. Parity will be checked during Read and Read After Write. Both Vertical Redundancy Check (VRC) and Longitudinal Redundancy Check (LRC) will be used for the parity check.

3.   I/O INSTRUCTION

3.1   External Command Out (ECO)

3.1.1   MN Field

All eight bits of the M and N fields are used for tape controller address selection.

3.1.2   Accumulator Contents

The right byte defines the controller command.

3.1.2.1   Clear - 00

This instruction will reset the controller. All interrupt selections and signals will be reset. The CLEAR instruction will reset all error conditions, set end of operation status, and stop tape motion.

3.1.2.2   Allow Interrupt - Bit 12 = "1"

This instruction will allow the controller to issue a service request each time it is ready for another data transfer or an end of operation (EOO) has occurred and the unit is ready to receive another instruction.

3.1.2.3   Inhibit Interrupt - Bit 13 = "1"

This instruction will inhibit an existing service request and prevent the issuance of any future service request.

3.1.2.4   Allow EOO Interrupt Only - Bits 12 and 13 = "1"

This instruction will allow a service request only at the end of operation, i.e., the tape is stopped between records or at BOT. Any existing service request due to data transfer requirement will be dropped.

3.1.2.5   Connect 8C through F

This instruction will address the tape unit using bits 14 and 15 of the connect command. All subsequent ECO, EDO, EDI, and ESI commands will be directed to the addressed tape unit.

Bit 14	Bit 15	Tape Unit
0	0	#1
0	1	#2
1	0	#3
1	1	#4

3.1.2.6   Read Byte or Word

These instructions will select the Read mode, reset end of operation status, and
start forward tape motion. Status and error conditions as a result of the previous
operation will also be reset. Once tape motion has been started, it will continue
until an interblock gap has been detected, at which time end of operation status
will set. Interrupt on end of operation may be used to interrupt the computer
when end of operation status sets. Parity (VRC) will be checked as each byte is
read from the tape. Also (LRC) Parity will be checked at the end of the record.

Buffer available status will be set when the controller has data ready for transfer
to the computer. The buffer available interrupt may be used to interrupt the
computer at this time.

3.1.2.6.1   Read Byte -01

The buffer available status will be set after each byte is read from the tape.
The data transfer rate will be 20 KHZ in this mode. The computer has approxi-
mately 45 μsec. to read the byte of data following the setting of buffer available
status. Lost data status will be set if data is not read with this time.

3.1.2.6.2   Read Word -03

In this read mode two (2) bytes of data will be assembled to form a 16-bit word.
The 16-bit word will be transferred to the computer at a 10 KHZ rate. Following
the setting of the buffer available status, the computer has approximately 95 μsec
to read the data. If data is not read within this time, the lost data status will
be set.

If a tape block contains an odd number of bytes, the last word transferred to the
computer will contain a right byte of hexadecimal 00 and the length error status
will be set.

1st Byte	2nd Byte
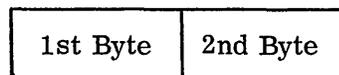
3.1.2.7   Write Byte or Word

A write instruction will select the write mode, reset end of operation status, and
start tape motion. Also, status and error conditions from a previous operation
will be reset. The controller will reject a write instruction if the selected tape
unit is file protected. Odd parity will be computed and recorded with each byte
of data. At the end of the block of data, a Cyclic Redundancy Check (CRC)
character and a Longitudinal Redundancy Check (LRC) character will be recorded.
Read after write parity check wll be used to check that data is being recorded
without errors.

If the tape is positioned at load point, a write instruction will move tape 3.75 inches before starting to record the block of data.

End of operation status will set after the Read after Write Logic has checked the LRC parity and tape has stopped.

Lost data status will be set if the computer tries to transfer data after end of block sequence has been started.

3.1.2.7.1   Write Byte - 10

This mode will record data bits 8 through 15 of the data from the computer. Recording of data will continue until the computer fails to transfer data to the controller within 45 μsec after buffer available status sets. If the computer does not transfer data within this time, the controller will reset buffer available status, generate the interblock gap and stop tape motion.

3.1.2.7.2   Write Word - 12

In this write mode, the 16-bit data word transferred from the computer will be disassembled by the controller and recorded as two 8-bit bytes. The ten KHZ transfer rate will allow about 95 μsec for computer to transfer a word after buffer available status is set. If the computer does not transfer a data word within the 95 μsec time period the controller will reset buffer available status, generate the interblock gap and stop tape motion.

1st Byte	2nd Byte
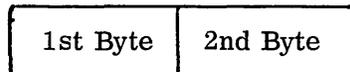
3.1.2.8   Write Tape Mark - 13

The tape mark is a standard end of file record consisting of one byte (hexadecimal 13) followed by an LRC character. Approximately 3.75 inches of tape is erased prior to recording the tape mark. End of operation status will set after tape has stopped. Also, the tape mark status will be set.

3.1.2.9   Set Erase - 73

The set erase instruction will set an indicator in the controller. There is no tape motion at this time. When the next write order is received by the controller, approximately 3.75 inch tape is erased before recording the block of data. If the next instruction received is other than a write instruction, this indicator is immediately reset.

3.1.2.10   Space Instructions

Space	Record	Forward	22
Space	Record	Backward	42
Space	File	Forward	20
Space	File	Backward	40

The four space instructions permit moving of tape over a record or file in either a forward or reverse direction. If load point is encountered when spacing tape in reverse, tape motion will stop and an end of operation status is set. A back space instruction will be rejected if the tape is positioned at loadpoint.

The end of operation status will set at the end of all spacing instructions. If a tape mark (EOF) is encountered when spacing tape the tape mark status will be set at the same time as the end of operation status.

If a forward spacing instruction moves the tape completely off the supply reel, the end of operation status will be set.

3.1.2.11   Rewind - 60

The rewind instruction will start a high speed rewind on the selected tape transport. The tape will be positioned on the load point marker at the end of the rewind operation. End-of-operation and rewinding status will set when the controller accepts the rewind instruction.

The Ready Busy Interrupt may be used with the rewind instruction to signal the computer when the rewind operation is complete.

The rewind instruction will be rejected if the tape is positioned at load point.

3.1.2.12   Off Line - 62

This instruction will cause the unit to switch to the off line mode. The operator must manually place the unit on line before the controller can operate on it.

3.1.3   Acknowledge

An ECO affecting the interrupt modes (paragraphs 3.1.2.2; 3.1.2.3; 3.1.2.4) will always be performed. If bits 12/13 are the only ones true or they are combined with others to form command which can be executed then the ECO will be acknowledged.

3.1.4   Service Request

The service request will always be set to the mode indicated by bits 12 and 13. If they are both false ("0") then the interrupt flip-flops will not be affected.

3.2   External Data Output (EDO)

3.2.1   MN Field

All eight bits are used for controller address selection.

3.2.2   Accumulator Contents

If the EDO is acknowledged, the data in the accumulator will be transferred
to the controller buffer. If using the write byte mode, only 8 least significant
bits will be recorded. All 16 bits will be recorded when using the write word
mode. (Two 8 bit bytes).

3.2.3   Acknowledge

An EDO will only be acknowledged if the controller buffer is available, i.e.,
it is empty and the previous ECO acknowledged was a write command.

3.2.4   Service Request

A service request will be dropped each time an EDO is acknowledged. The
service request will be reissued when the controller is ready to accept a new
word or when tape motion has stopped at the end of operation (EOO).

3.3   External Data In EDI

3.3.1   MN Field

All eight bits are used for controller address selection.

3.3.2   Accumulator Contents

If the EDI is acknowledged the data in the controller buffer will be transferred
to the accumulator. When using the read byte mode the byte of data will be
placed in the accumulator bits eight through fifteen. In the read word mode
two (2) bytes are transferred to the accumulator.

3.3.3   Acknowledge

An EDI will only be acknowledged if the controller buffer is available, i.e., it
has a new word to be transferred and the previous ECO acknowledged was a
read command.

3.3.4   Service Request

A service request will be dropped each time an EDI is acknowledged. The service request will be reissued when the controller has a word ready for transfer or when tape motion has stopped at EOO.

3.4   External Status In ESI

3.4.1   MN Field

All eight bits are used for controller address selection.

3.4.2   Accumulator Contents

The accumulator will contain the following status information, a "1" indicating the condition is true.

Status Response	Bit
Not Ready (Tape Unit)	9
Busy (Controller)	8
Load Point	12
End of Tape	14
File Protect	11
Tape Mark (EOF)	15
Rewinding	6
Buffer Not Available	5
Length Error	4
Lost Data	13
Parity Error	10

3.4.2.1   Not Ready

Selected tape unit does not have power on, tape loaded, or is not in the on line mode.

3.4.2.2   Busy

Tape motion in progress on the tape unit. A forward, reverse, or rewind operation will cause the tape unit to go busy. Busy status will reset when tape motion halts.

The controller will reject a new instruction, when the busy status is set.

3.4.2.3   Load Point

Tape is positioned at the load point marker. Back space and rewind instructions will be rejected when the load point status is set.

3.4.2.4   End of Tape

The end of tape status will set if the last forward tape motion operation causes the end of tape marker to be sensed. Any operation may be initiated while this bit is set, but forward operations may run the tape off the supply reel. The status bit will stay set until a backward operation encounters the end of tape marker, tape unit dropped off line, or a different tape unit is connected.

3.4.2.5   File Protect

Writing is not allowed on the tape. Insertion of the write ring in the tape supply reel will reset the file protect status. A write instruction will be rejected if the file protect status is set.

3.4.2.6   Tape Mark (EOF)

The status will be set if the last record read or spaced over was a tape mark record. The status bit will also be set after writing a tape mark.

3.4.2.7   Rewinding

The selected tape unit is in the process of rewinding.

3.4.2.8   Buffer Not Available

The buffer available status will reset when the controller has data (word or byte) ready for transfer to the computer when in the read mode. The status bit will also be reset when the controller is ready to receive another word or byte, during a write operation.

Execution of an EDI or EDO will set the buffer not available status. The EDI or EDO instruction will be rejected if that status is set.

3.4.2.9   Length Error

The length error status will set upon the completion of a start word read operation if the block that was just read contained an odd number of bytes. The last word transferred to the computer will contain a hexadecimal 00 in the eight (8) least significant bits if the length error status is set.

3.4.2.10   Lost Data

The lost data status will set if the computer does not transfer data in the time allowed when in the read mode. The status bit will also set in the write data mode if the computer tries to transfer data to the controller after an end of block sequence starts or if end of operation status is set.

3.4.2.11   Parity Error

The parity error status will set if the controller detects a vertical redundancy check error or a longitudinal redundancy check error. Parity error checks are performed on read and write data operation.

3.4.3   Acknowledge

An ESI will not be acknowledged.

3.4.4   Service Request

An existing service request will be dropped.

3.5   External Address In EAI

3.5.1   MN Field

The MN field is not used in the controller response to an EAI.

3.5.2   Accumulator Contents

The contents of the accumulator is the address of the controller if it has issued a service request and has the highest precedence.

3.5.3   Acknowledge

An acknowledge is not issued for an EAI.

3.5.4   Service Request

The service request signal will be dropped.

SYSTEMS DESCRIPTION OF DATA MODEMS

1.   INTRODUCTION:

This paper describes the functions and features of the Modem Controllers now designed or proposed for the MAC 16 computer system. It also lists representative terminals used by them.

Definitions of terms used may be found in Section 4.

2.   SYSTEMS DESCRIPTION:

| MAC 16 | Modem Controller | Data Set | Communication Line | Data Set | Remote Terminal |
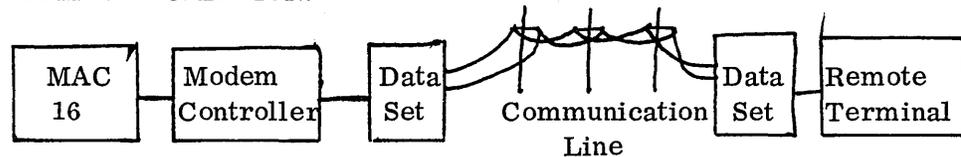
In effect, a data set acts as an interface between a telephone line and a user device. The data set provides a common interface to the user device, specified in Electronic Industries Association Standard RS-232-B. This common interface theoretically enables equipment manufacturers to design terminals that can operate with many data sets. However, different types of data sets have subsets of, or additional signals not covered by RS-232-B. Therefore on line terminals are frequently designed to operate with only one specific type of data set.

MAC 16 has not been designed to interface directly to a data set. Instead it uses a series of Modem Controllers to interface MAC to various data sets. This provides MAC with the ability to communicate with a wide range of terminals over a variety of communication facilities.

The Modem Controller provides those functions necessary to take data from the CPU and present it in an acceptable form to the telephone facility, and vice versa.

Broadly, the functions of a Modem Controller are these:

a. Serial to Parallel and Parallel to serial conversion.
   The Modem Controllers proposed or designed thus far,
   interface with serial data sets. Data are received from
   the CPU in parallel and presented to the Data set serially.
   Data are received from the data set serially and presented
   to the CPU in parallel. The Modem Controller performs
   the conversion.

b. Timing:
   Transmission is accomplished at a fixed rate of speed
   although this rate may vary from terminal system to
   terminal system. It is a function of the Modem Controller
   to handle this data at the proper rate.

c. Control:
   The Modem Controller controls the rate at which data
   are requested from the CPU. It provides status information
   and service requests. It controls features on the data
   set necessary to establish and maintain communication.

d. Signal level conversion. The data sets operate with signal
   levels that are quite different from the computer logic voltage
   levels. The Modem Controller performs the signal level
   conversion.

Communications Facilities:

The Modem Controllers currently proposed for the MAC 16 operate over private,
using either point to point or party line techniques, or switched telephone lines.
They are designed to operate with a subset of the currently available communications
facilities.

However, a majority of the presently considered on line terminals operate within the framework of this same subset. Due to the standardization efforts of the United States of America Standards Institute it is expected that most future terminals of the type considered desirable for operation with MAC will also operate within the framework accommodated by these Modem Controllers.

3.0   There are presently three Modem Controllers under consideration

1.   YHS -   High Speed Synchronous. Able to provide efficient high speed operation. Can communicate with a majority of currently available commercial terminals that operate in a synchronous fashion utilizing 201 type data sets

2.   YAM -   Lower speed synchronous. Primarily intended for communication with Teletypwriter terminals.

3.   YAS -   Expanded version of YAM. Able to operate over a wider selection of speeds, formats and communications facilities. Intended to replace YAM.

These Modem Controllers are discussed more fully in the following pages.

3.1   YHS

YHS is a synchronous Modem Controller designed to operate with Bell 201 Data Sets at speeds of up to 2400 bits per second. It can transmit and receive at higher speeds using other manufacturers equivalent data sets, for example the Rixon Sebit 48C at 4800 bits per second.

Synchronous communication is attractive because of the high speeds attainable and the greater efficiency of coding: 8 bits per character instead of the 10 or 11 required in an asynchronous system. In addition, a large number of on line terminals are available that communicate synchronously.

YHS is designed to operate at speeds of up to 4800 bps or higher. Its options, its double buffering feature and sophisticated CPU interfacing procedures provide efficient and flexible communications capability for the MAC 16 computing system.

YHS - Input

In synchronous transmission data are usually transferred out of the sending terminal under control of a clock signal provided by the data set.

At the receiving end, the data set reconstructs the clock and presents the transmitted data to the terminal device along with the clock signal. When YHS is receiving, it uses this clock to gate the data into an 8 bit shift register. When an 8 bit character has been assembled, it is transferred from the shift register to an 8 bit buffer register, thereby freeing the shift register to take the next character of data. At the time of transfer, a service request is issued to MAC. If MAC does not respond before the next character has been completely loaded into the shift register a timing error will result. If MAC does respond in time with an EDI, the data are transferred and the buffer register is made ready to accept the next character.

At a 2KC clock rate MAC will receive an input Service request every 4ms. As data are loaded into the shift register a parity check is made. The result of this check is presented over the most significant line of the PDC bus along with the data. If the parity check found that the number of 1 bits were odd PDC bus line 0 will have a 1 on it, if even, a 0.

It is up to the software to determine whether the parity is correct for the character.

Clock pulses are received from the data set prior to the time the actual data is received. As there are no start or stop bits attached to the data characters, synchronisim of YHS with the data stream must be established through the use of SYN characters. At the beginning of each transmission the sending terminal sends SYN characters. YHS decodes these and conditions itself to take the serial data stream and group the the bits into the proper byte. The basic YHS Modem Controller expects to see at least two SYN characters prior to the start of data. The SYN character may be strapped for any code except FF_{16}.

As an option YHS may be strapped to examine for only one SYN, again any code except FF_{16}. As a further option YHS may be strapped not to examine for any SYN characters but to synchronize itself on the first space (0) bit received. This allows any code to be used as the first character in the data block that will present a 0 to the line as the first bit transmitted. However, this is risky as a spurious space bit prior to the start of data will, the great majority of the time, cause YHS to be out of synchronism. Synchronism cannot be re established for, as a minimum, the duration of that block of data.

YHS – Output

Data are presented to YHS over the PDC in parallel, utilizing the least significant 8 lines.

These data are loaded into an 8 bit buffer register. At the appropriate time YHS loads these data into an 8 bit shift register. The data are then shifted out serially to the data set under timing provided by the data set clock.

At the time data are transferred from the buffer register to the shift register, YHS raises a service request to MAC for another character of data. If MAC does not respond with another character before the character in process has been completely shifted out, loss of synchronization with the receiving terminal results. To inform MAC that this has occurred an output timing error service request is issued.

The YHS may be used over the switched network in a half duplex mode at 2000 bits per second when operating with a Bell 201A data set.

It can optionally be equipped with a Bell 801A or 801C Automatic Call Unit so that the computer can cause automatic dial up of the remote terminal. The data set can be strapped for automatic answering of a call initiated by the remote terminal site.

In dedicated line service, the YHS can operate over a 2 wire line in a half duplex mode, or over a four wire line in either half or full duplex mode. With four wire facilities either point to point or party line systems may be used. Over private lines, using the Bell 201B data set, speed is 2400 bps.

Higher speed transmission is possible when using compatible data sets of other manufacture.

YHS occupies two slots in the card cage.

The commands used to control YHS are:

a. Inhibit Output Interrupt

b. Allow Output Interrupt

c. Inhibit Input Interrupt

d. Allow Input Interrupt

e. Request to send

f. End of transmission

g. Record Separator

h. CPU Terminal Ready

i. Terminal off

j. Call Request *

k. Abandon Call*

l. Dialing Complete*

Service Requests to MAC are:

a. Input Data Ready

b. Output Data Request

c. Input Timing Error

d. Output Timing Error

e. Data Set Ready

f. Data Set Not Ready

g. Present Next Digit*

h. Abandon Call and Retry*

* Used only with Auto Dial Option

YHS Summary

Bell Data Set	201A	201B
Facility	Dial up	Private
Mode	**half duplex**	2 wire – half duplex 4 wire – half or full duplex point to point or party line
Speed	20U0 bps	2400 bps
Features		
Auto Call	X	
Auto Answer	X	
Alternate Voice	X	

Typical Applications*

Sanders 720 CRT Display

UNIVAC UNISCOPE – 300 Visual Communication Terminal

Raytheon DIDS–400 CRT

Burroughs Display System

Bunker Ramo 200 Data Display System

Computer Communications CC30

GE Datanet 30

IBM 2780 Data Transmission terminal

Remote card reading, card punching and printing

UNIVAC DCT 2000 Data Communication Terminal

Similar to IBM 2780

MAC 16 to MAC 16 or other suitably equipped computer.

* NOTE: Terminals listed for all modem controllers are based on what is believed to be accurate information. However due to possible misunderstanding of manufacturers specifications, and due to changes, deletions and introduction of new devices, it is recommended that manufacturers sales representatives be contacted for confirmation before committing to accept any given terminal as an on line peripheral to MAC 16.

3.2   YAM

YAM is a low to medium speed asynchronous Modem Controller. It will operate over switched or dedicated telephone lines with Bell 103A, 103F, 202C, 202D data sets or equivalent data sets of other manufacture.

It operates using 8 level, 11 unit Teletype format, i.e., 8 data bits preceeded by one start bit and followed by 2 stop bits.

Unlike YHS, YAM does not receive a clock from the data set and characters need not be contiguous. YAM does not decode for SYN characters. Synchronism is maintained only over a single character, the start bit flagging the beginning of a character and the stop bits the end.

As YAM was designed to operate at lower speeds, it lacks the double buffering feature and the sophisticated service request handling of YHS.

Characters are presented to YAM serially by bit from the data set. A start bit causes the logic to count the next 8 bits and assume them to be a character. When the second stop bit is received, an interrupt is generated. MAC has approximately one bit time to EDI the data. At 300 bits per second, this is approximately 3.3ms. If the EDI is received too late, it will not be acknowledged. On input YAM strips the start and stop bits and transfers only the 8 data bits.

Parity is neither checked nor generated by YAM.

Data are presented to MAC and received from MAC in parallel over the 8 least significant bit lines of the PDC. The first bit received or to be transmitted will occupy A15 of the accumulator. With the majority of remote terminals, this will be the least significant bit of the character.

On output, 8 data bits are presented to YAM in parallel by MAC. YAM adds the start and stop bits and presents the character serially by bit to the data set. During transmission of the second stop bit YAM generates an Output Interrupt to MAC. If MAC does not respond immediately no harm is done as in asynchronous transmission characters need not be contiguous.

In dial up systems, YAM cannot be fitted with the Automatic Call feature. However the data set can be arranged to provide automatic answering.

The commands used to control YAM are:

Input interrupt inhibit

Output interrupt inhibit

Input interrupt allowed

Output interrupt allowed

Request to send

End of Transmission

Following is a summary of the types of service YAM can be operated with:

Data Set	103A	103F	202C	202D
Facility	Dial up	Private	Dial up	Private
Mode	half or full duplex	2 wire–half or full duplex party line or point to point	half duplex	2 wire – half duplex point to point 4 wire – half or full duplex, point to point or party line.
Speed	110-300b/s	110-300 b/s	110-1200b/s	110-1800 b/s
Features				
Auto Answer & Termination	X		X	
Alternate Voice	X		X	

YAM occupies one slot in the card cage.

YAM is intended to be an interim device. It will eventually be superceded by YAS.

YAM - Typical Applications

    Teletype 33, 35.

    Friden 7100 Conversational Terminal

    Dura Solid State 1041 Data Terminal

    SCM Kleinschmidt 311 Electronic Data Printer

    RCA 70 Video Data Terminal

3.3   YAS - High Speed Asynchronous Modem Controller

YAS will provide greatly expanded capabilities over YAM, which it is intended to replace. Where YAM operates only with an 8 bit, 11 unit, code using one start and 2 stop bits, YAS will operate using 5, 6, 7 or 8 bit codes, one start and one or two stop bits. Like YHS it will provide double buffering and more flexible and sophisticated service request and command handling. These features will enable YAS to operate with a much greater variety of remote terminals.

No detailed discussion will be included here as the YAS Modem Controller is in the design stage, however, the general characteristics are shown in the following summary chart.

YAS

Bell Data Set*	103A	103F	202C	202D
Facility	Dial Up	Private	Dial Up	Private
Mode	Half or full duplex	2 wire Half or full duplex, point to point or party line.	Half duplex	2 wire - point to poin 4 wire - half or full duplex, point to point or party line.
Speed	75-300 b/s	75-300 b/s	75-1200 b/s	75-1800 b/s
Features				
Auto Dial	X		X	
Auto Answer	X		X	
Alt Voice	X	X	X	X
Reverse Channel				X (2 wire line only)

* Or equivalent

Typical Applications:

All those listed for YAM plus

Sanders 720 CRT

Raytheon DIDS 402 CRT

IBM 2260 CRT

Burroughs 93S1 CRT

Bunker Ramo 200 CRT

Computer Communications CC30 CRT

GE Datanet 30 CRT

RCA 70 CRT

Stromberg Carlson SC-1100 CRT

Digitronics D-401 On Line Printer Terminal

NCR C-740 Remote Line Printer

IBM 2780 Data Transmission Terminal

Analex 4000 Remote Printer Terminal

IBM 1050 Data Communication System

IBM 2740 Data Terminal

Friden Collectabdata 30 Data Acquisition System

IBM 1030 Data Collection System

Teletype 28, 32

Bell Data Speed 2 Paper Tape Sender and Receiver

Dartex Mag Tape Terminal

Certain models of Tally Paper Tape Transmission equipment

4.0   Definitions

While the following defintions are by no means universally used, for the purposes of this document the following will apply.

a.   Data Set.

A device that provides an interface between user equipment and the telephone network. The Modem-Controllers have been designed to interface with Bell System data sets. However, where data sets are provided with the same characteristics by other manufacturers, they may be used in place of Bell System sets. Non-Bell data sets are manu-factured by Collins, Rixon, and Milgo among others.

b.   Full duplex.

Simultaneous transmission and reception of data over the same communi-cation facility.

c.   Half duplex.

Non-simultaneous transmission and reception of data over a communi-cation facility. In half duplex operation data can only be sent one way at a time.

d.   2 Wire service. Refers to leased line service where the facility provided is physically two wires, signal and return. With most data sets this limits the system to half duplex operation only. However, with Bell 103 series data sets full duplex operation can be obtained over 2 wire service. Dial up service is functionally 2 wire.

e.   4 wire service. Equivalent to two 2 wire lines. Permits full duplex operation of terminal systems. However, many terminal systems use 4 wire service yet operate in a half duplex fashion, as 4 wire service drastically cuts the time necessary to stop transmission at one end, "turn the line around" and begin transmission from the other end. Typically 4 wire leased lines are only 10% - 20% more expensive than 2 wire.

f.   Synchronous data set. A data set such as the Bell 201 or 203 which transmits a clock signal along with the data.

The clock, which may be provided by the data set or by customer equipment is used to control timing of data from the transmitting equipment. It is regenerated by the receiving data set and provided along with the data signal to facilitate input of data.

g.   Asynchronous data set.   A data set which does not provide clock information to either the transmitting or receiving terminal.

h.   Synchronous format.   Typically, data transmitted via synchronous data sets do not contain start/stop bits.   Data are transmitted serially as contiguous n bit bytes.   The data set clock is used to reconstruct the received characters.

i.   Asynchronous format.   Typically, characters transmitted via asynchronous data sets are preceeded by a space (zero) start bit and followed by one or two mark (one) bits.   The receiving terminal must provide its own timing to reconstruct the received character, however, as each character is framed, bit timing is reinitiated on each character.

NOTE: While uncommon, examples are found of data being transmitted in synchronous format via asynchronous data sets and vice versa.   These systems cannot be accommodated by the presently considered Modem-Controllers.

j.   SYN.   In synchronous systems, where start and stop bits are not used, clocks are usually received at the data set before the actual data stream. Therefore in order to group the incoming bits into their proper bytes synchronism must somehow be established.   This is usually accomplished by preceeding the message block with one or more unique SYN characters. (USASI proposed standard calls for four).   When the receiving device recognizes the SYN character it synchronizes its timing and counters accordingly.

k.   Mark, Mark Hold.   In data communications terminology a mark is a "one" bit.   Mark hold refers to the state of the communication line being held in a mark state (transmitting continuous one bits) between message blocks.

l.   Space.   A zero bit.

m.   Private or Dedicated line.   A unique leased line routed through the telephone network between two or more terminals.   Usually higher quality than switched lines, permitting higher transmission rates.   Available full time or at scheduled times of the day.

n.   Switched or DDD (Direct Distance Dialing) line.   Ordinary dial up telephone service.   A dial-up connection can be established between two terminals either manually or automatically, after which data can be transmitted.

o.   ACU, Automatic Calling Unit.   A device provided by the Bell System that allows a device to automatically dial up a remote terminal over the switched network.   The remote terminal must be equipped with automatic answering facilities, also provided by Bell as part of the data set facility.

p.   Reverse Channel.   A feature available on some data sets that allows low speed signalling by a receiving terminal while data is being transmitted to it.   Typically used as a go-no go condition indicator of the receiving terminal.   Available with 2 wire service only.

q.   Point to Point.   On a leased line having a single line with one terminal at each end.   Switched calls are inherently point to point.

r.   Party line.   In 4 wire leased line systems several terminals may share a line.   Terminals are selected for transmitting or receiving by polling techniques.

YAM MODEM I/O BUFFER

1.0 SYSTEM DESCRIPTION

The YAM Modem I/O Buffer provides a full duplex RS 232B interface between the MAC 16 computer and a Bell Type 103A, 103F, or equivalent asynchronous data set. Data communication between the CPU and buffer is by 8 bit parallel transfers, with buffer/data set communication by 8 level 11 unit serial start-stop code format. The standard buffer data transfer rate is 10 characters per second (110 baud serial bit rate). Optional clock rates can be provided up to the maximum 300 baud data set capacity.

The buffer may be strapped for fully automatic DDD switched network call answering and termination when used with the Type 103A data set and its associated Type 804B1 control unit. Optional strapping facilities are provided for manual answering and termination when alternate telephonic communication is desired.

When used with the Type 103F data set, the buffer provides automatic operation over a dedicated private line.

The buffer is mounted on one standard sized MAC 16 printed circuit card.

1.1 DATA SET OPERATION

1.1.1 Switched Network Data Set Operation

This service provides for alternate voice and data communications in the exchange and toll switched voice message (DDD) Network. When fully automatic unattended CPU operation is utilized with the Type 103A data set, the 804 B1 control unit "AUTO" key is maintained depressed. Data communication is initiated when a remote terminal dials the CPU assigned telephone number. Whenever the CPU is not in HALT or power off condition, the call is accepted and data channel establishment proceeds. The CPU data set transmits a tone to the originating terminal, whose attendant then switches his control unit from TALK to DATA. The channel is established in approximately 4 seconds.

Two operational procedures are possible to initiate data communication after channel establishment:
1. Initial transmission from the CPU;
2. Initial transmission from the calling terminal.

Using the first procedure, operation of the buffer must be with transmitter service requests allowed. As soon as the channel establishment is completed, the YAM buffer issues a transmitter service request to the CPU, which then outputs an Enquiry (who are you?) character to the calling terminal. After terminal identification has been received by the CPU, data communication can proceed.

Using the second procedure, operation of the buffer must be with receiver service requests allowed. The calling terminal transmits his identification to the CPU after observing that channel establishment has been completed. This observation may be by visual (indicator lamp), aural (monitor speaker) means, or by noting elapsed time after switching to DATA, depending on the calling terminal data set used.

When data communication is finished, the originating terminal switches back to TALK, and hangs up. The buffer then signals the CPU data set to disconnect from the line.

The buffer will answer a "wrong number" call briefly, but will automatically hang up, after sensing the call is not from a data terminal, thus clearing the station for receipt of bonafide calls.

When attended alternate voice/data operation is used, the Type 804B1 control unit is left with the TALK button depressed between calls. In this mode, incoming calls must be answered manually After the voice communication is completed, the CPU attendant depresses the control unit DATA button, and channel establishment proceeds as discussed above for automatic operation. It is necessary now, however, that the line disconnect be accomplished by the CPU attendant. He must first switch his control unit back to TALK, and then hang up by replacing the handset in its cradle. This requires that the attendant know when data communication is completed.

The Type 804B1 control unit is equipped with six push buttons for control of the station:

DATA - (nonlocking; releases any depressed locking key) - If the Talk key has been depressed, and the telephone handset is off the cradle, the DATA key transfers the set from the voice mode to the data mode. It is illuminated when the set is in the data mode.

TALK - (locking) - When depressed and the handset is lifted the set is placed in the voice mode. If it had been in the data mode, it is transferred to the voice mode.

TEST 1 - (nonlocking) - Places the data set in the answer mode for test purposes. This key should be used only when and as directed by Telephone Company personnel. It is illuminated when the data set is in the test mode. If activated accidently, the test mode may be cancelled by operating the DATA key.

TEST 2 - (nonlocking) - Returns the set from the answering to the originating mode for test. This key should be used only when and as directed by Telephone Company personnel.

LOCAL - (locking) - Places data set in the local mode. In this mode signals sent into circuit BA (Transmitted Data) appear on circuit BB (Received Data). This permits customers to make a ch of the continuity of the interface connections and of the signal handling stages adjacent to the interface in the customer's equipment. It may be released by depressing the DATA, TALK, or AUTO keys.

AUTO - (locking) - when automatic answer is provided on a key-controlled basis, this key is depressed to enable the feature. Circuit CD (Data Terminal Ready) must also be "ON" for the feature to function. The key is illuminated when depressed. It may be released by depressing the DATA, TALK, or LOCAL keys.

1.1.2 Dedicated Line Operation

This service, using a Type 103F data set, provides for digital data communication only between the CPU and one or more remote terminals connected by private (non dial-up) telephone quality lines. Voice communication, if required, must be arranged separately.

For two-point service (CPU and one remote terminal) data communication may be initiated at either end at any time. Multi-point networks are possible in various configurations. The operational restrictions and non-contention arrangements required must be determined for each specific network and are not discussed here.

1.2 BUFFER OPERATION

The YAM buffer comprises three functional sections: receiver, transmitter, and control.

The receiver accepts 8 level 11 unit serial data characters from the data set, strips off the start and two stop bits, and assembles the 8 data bits in a register for parallel input to the CPU in response to an EDI instruction.

The receiver contains a gated clock, set for the specific serial bit rate used by the remote terminal transmitter. A service request is issued to the CPU each time a new data character has been assembled. Service requests can be suppressed by CPU command when such operation is required.

The transmitter accepts an 8 bit data byte from the computer PDC data bus lines 08 through 15 in response to an EDO instruction. The buffer appends a start and two stop bits and serially transmits this formatted character to the data set. A service request is issued to the CPU after transmission of each character. Service requests can be suppressed by CPU command when required.

The control section monitors the data set for incoming calls and provides the signals and timing required for answering and termiating such calls in the automatic mode. This section accepts CPU command and control instructions to synchronize data transfers, allow or inhibit service requests, and in dedicated line (Type 103F data set) usage, provide a request to send signal to the data set when data output is desired.

Transmitter and receiver service requests may be used on individual program level interrupt lines, or may be shared on one common interrupt line with other controllers in any precedence order.

The buffer transmitter section is assigned an even eight-bit binary station address (excluding an all-zero address). The receiver section is assigned the next larger odd binary address.

1.3 I/O Instruction

The buffer responds to the ECO, EDO, EDI and EAI instructions as described in the MAC 16 Reference Manual. The M and N fields of each instruction define the receiver or transmitter address.

1.3.1 The buffer accepts four ECO commands and returns an Acknowledge signal. Two comman are valid for both switched network and dedicated line service. The other two commands are used for dedicated line service only. (See Sec. 1.4, Programming Requirements). The right byte of the A register defines the command.

1.3.1.1 Interrupt Inhibit   XXX4

This receiver or transmitter addressed command prevents the buffer receiver or transmitter respectively from issuing a service request to the CPU regardless of data transfer requirements.

1.3.1.2 Interrupt Allowed   XXX8

This receiver or transmitter addressed command allows the buffer receiver or transmitter respectively to issue a service request to signify a data transfer is required (receiver case) or possible (transmitter case).

1.3.1.3 Request to Send   XXX1

This command is addressed to the buffer receiver, and instructs the buffer to command the CPU Type 103 F data set to request a clear to Send response from the remote data terminal.

1.3.1.4 End of Transmission   XXX2

This command is addressed to the buffer receiver, and instructs the buffer to command the CPU data set to drop the Request to Send signal to the remote data terminal.

1.3.2 EDI

The EDI instruction performs as described in the reference manual. The M and N fields of the EDI instruction define the controller receiver address. A "data in" signal is transmitted to the controller. An "acknowledge" signal from the controller signifies data has been placed on PDC data bus lines 8 through 15. Absence of an acknowledge signal signifies no data is available for transfer.

The most significant data bit is placed on line 8, in descending order with the LSB on line 15.

1.3.3 EDO

The EDO instruction performs as described in the reference manual. The M and N fields of the EDO instruction define the controller transmitter address. The right byte of the A register is placed on PDC data bus lines 8 through 15, with the byte MSB on line 8, in descending order, with the LSB on line 15. A "data out" signal is transmitted to the controller. An "acknowledge" signal from the controller signifies data has been transferred. Absence of an acknowledge signal signifies a data transfer is refused at this time.

1.3.4 EAI

The EAI instruction performs as described in the reference manual. An "address in" signal is transmitted on the PDC. When a controller interrupt request is active, the address of the section requesting service is placed on the PDC data bus lines 8 through 15. The address MSB is placed on line 8, in descending order with the LSB on line 15.

1.4 PROGRAM REQUIREMENTS

The normal controller operational mode is with Receiver and Transmitter program interrupts allowed. An active interrupt request signal is cleared at the completion of service by an EAI, EDI or EDO instruction as applicable. Each of these three instructions shall be followed by an additional instruction before a JRL instruction is executed to ensure that this interrupt level signal has dropped.

1.4.1 ECO Instruction Commands

The A register contents shall be limited to the four command words defined in Sec. 1.3.1.

All ECO's will be acknowledged regardless of the state of the YAM buffer and data set.

1.4.1.1 ECO Addressed To Receiver

a) Inhibit Interrupt – $A_{13} = 1$

Prevents the receiver from issuing an interrupt when requiring service.

b) Allow Interrupt – $A_{12} = 1$

Allows the receiver to issue an interrupt when requiring service.

Commands a) and b) are valid with both switched network and dedicated private line data sets.

c) Request to Send – $A_{15} = 1$

Turns on carrier in data set to place remote data set in receive state.

d) End of Transmission – $A_{14} = 1$

Turns off carrier in data set to terminate transmission.

Commands c) and d) are valid only with dedicated private line data sets.

1.4.1.2 ECO Addressed to Transmitter

a) Inhibit Interrupt – $A_{13} = 1$

Prevents the transmitter from issuing an interrupt when requiring service.

b) Allow Interrupt – $A_{12} = 1$

Allows the transmitter to interrupt when requiring service.

These two commands are valid with both switched network and dedicated private line data sets.

1.4.2 EDI Addressed To Receiver

If data is available, the EDI will be acknowledged and the data inserted into A, where:

A_{15} = Leading serial bit
A_{14} = second " "
A_{13} = third " "
A_{12} = fourth " "
A_{11} = fifth " "
A_{10} = sixth " "
A_9 = seventh " "
A_8 = last " "
A_{0-7} = 0

The conversion of ASCII characters to tape code is as defined in SS-14.

If an EDI is issued but not acknowledged: A_{0-15} = 0.

1.4.3 EDO Addressed To Transmitter

If the transmitter can accept the data, it will acknowledge the command. The result will be:

A_{0-7} = Disregarded

A_{8-15} = Transmitted to data set where:

A_{15} = leading serial bit thru A_8 = last serial bit

The contents of A is not disturbed.

If the transmitter cannot accept the data, it is not acknowledged.

There is no requirement of time upon the issuance of a service requesting interrupt.

1.4.4 ESI Addressed to Receiver or Transmitter

No status information is available and therefore:
A_{0-15} = 0

1.4.5 EAI – Not Addressed

If interrupts are inhibited no response is permitted therefore: $A_0 - A_{15}$ = 0.

If interrupts are allowed, the section with the highest precedence on a shared interrupt level who is requesting service will respond. The result will be: $A_0 - A_7$ = 0

$A_8 - A_{15}$ = Device address where:

A_8 - Most significant address bit thru

A_{15} - least significant address bit.

An EAI command is not acknowledged.

1.4.6 Summary

Input Commands	A_{12}	A_{13}	A_{14}	A_{15}	Ack.
1. Inhibit Interrupt	0	1	X	X	Yes
2. Allow Interrupt	1	0	X	X	Yes
Output Commands					
1. Inhibit Interrupt	0	1	X	X	Yes
2. Allow Interrupt	1	0	X	X	Yes
Communication Commands (Addressed to Receiver)					
1. Request to Send	X	X	0	1	Yes
2. End of Transmission	X	X	1	0	Yes

Input EDI

1. Acknowledge if data available.
2. Input $A_0 - A_7$ are zero.

   Last serial bit to A_8 thru Leading serial bit to A_{15}.
3. Must be issued within one serial data set bit period or data will be lost.
4. Receiver service request terminates.

Output EDO

1. Acknowledge if data can be accepted.
2. Output A_8 to last serial bit thru

   A_{15} to leading serial bit.
3. No time requirement for issuance to protect data. However, it should be issued within one serial bit period of service request to maintain maximum output rate.
4. Transmitter service request terminates.

EAI

1. Does not acknowledge.
2. Input highest priority interrupting section address, MSB to A_8 thru

   LSB to A_{15}
3. Responding to section service request terminates.

1.4.7 Programming Considerations

1. The buffer initiatized state (following I/O reset) is:

   A) Transmitter and Receiver interrupts inhibited.

   B) End of Transmission signal to data set (103F).

2. An ECO allow transmitter interrupt command following initialization causes the transmitter to issue an immediate service request when an incoming data call has been established.

3. With switched network procedure 1 (Section 1.1.1) automatic call answering and disconnect, a transmitter service request is required to interrupt the CPU to initiate data transfers. Therefore the transmitter service request following the last EDO must not be cleared by an EAI. This final service request will be maintained until the calling terminal switches from DATA to TALK. To avoid a long hang-up in this program level, an end of transmission sequence should be programmed to alert the remote attendant to prepare to terminate the cal This sequence should follow the final EDO with an ECO inhibit interrupt and include a timing sub-routine to test for call termination. This requires an ECO allow interrupt command at one second (approximate) intervals to test for absence of a transmitter service request indicating call disconnect.

4. With switched network procedure 2 (section 1.1.1), a receiver service request is required to interrupt the CPU to initiate data transfers. Using this procedure, the final EDO is followed by an ECO inhibit transmitter interrupts. No further termination sequence is required to drop from the transmitter program level. The receiver must be left in the interrupt allowed state for recognition of subsequent data calls.

5. Using dedicated line data sets of the 103F type, I/O reset should be followed by an ECO allow receiver interrupts to condition the buffer for call reception. On two-point networks, an ECO Request to Send command may also be executed.

A time interval of 265 milliseconds after an ECO Request to Send elapses before the answering terminal responds with a clear to Send signal. During this set-up period, an EDO will not be acknowledged nor output data accepted by the buffer. No delay is incurred hereafter until an ECO End of Transmission command is executed, causing the answering terminal to drop its Clear to Send signal. Full duplex communication may be conducted anytime both terminals are in the Request to Send state.

3.0 INTERFACE, YAM BUFFER TO DATA SET

The buffer interface signals meet the functional and electrical requirements of EIA Standard RS23 Selection of applicable input and output signals is made to correspond with those required by the particular data set used.

3.1 The available input/output interface signals are listed below, together with the corresponding RS232B interface connector pin assignment. Circuit identification and function conform to the RS232B definitions, with Input being to data set, and Output being from data set:

YAM Pin	Circuit	I/O	Function	EIA Pin
None	AA	–	Protective Grd	1
B-57	BA	I	Transmitted Data	2
B-65	BB	O	Received Data	3
B-63	CA	I	Request To Send	4
B-49	CB	O	Clear To Send	5
B-53	AB	–	Signal Grd	7
B-47	CD	I	Terminal Ready	20
B-55	CE	O	Ringing Indicator	22

Alternative use can be made of several functions for specific operational modes. Such optional usage must be determined for each unique system requirement:

		Alternative Use		
YAM Pin	Circuit	I/O	Function	EIA Pin
B-66	CY	I	Originate Mode	11
B-63	CX	I	Local Mode	12
B-49	CF	O	Carrier Detector	8
B-55	CC	O	Data Set Ready	6

Data set circuits AA and AB are internally tied to the data set frame and power cord safety ground. AC power for the data set should be obtained from the same circuit used to power the CPU if possible to reduce ground noise currents.

3.2 Electrical Characteristics

YAM Input Loading
Resistance $6800 \pm 3\%$ ohms
Internal Voltage $\leqslant \pm 1$ volt

YAM Output Signal (3000 ohm load)
Negative level -5.2 ± 0.2 volts
Max. short circuit current   12.5 milliamperes

Positive Level $+8.5 \pm 3$ volts
Max. short circuit current   37 milliamperes

YHS HIGH SPEED SYNCHRONOUS MODEM CONTROLLER SYSTEM

1.0   SYSTEM DESCRIPTION

The YHS Controller, used in conjunction with the YHD Modem Interface adapter, provides an 8-bit character buffered line control between the MAC 16 Programmed Data Channel and EIA Standard RS232-B Interface bit-serial synchronous data sets. The controller may be used for 2-wire half duplex (HDX) or 4-wire full-duplex (FDX) data communication over voice grade switched network or private dedicated telephone lines.

The YHD interface adapter is available with an optional capability for providing automatic call placement under program control when used with the Bell System 801A or 801C Automatic Call Unit.

The YHS/YHD system will operate at data transmission rates determined by the data modems used. Compatible modems include the following and their equivalents:

Bell System 201A – Switched Network	–2000 bits/second
Bell System 201B – Dedicated Line	–2400 bits/second
SE BIT 48C – Conditioned Line	–4800 bits/second

The controller system is capable of operating at higher bit rates with suitable modem/ communication facilities. The controller is designed to operate synchronously with the data set transmitter and receiver internal clocks.

1.1   Synchronous Modem Description

1.1.1   Bell System 201A/201B Data Sets

These data sets may be used with 2 or 4 wire telephone lines. The Model 201A is designed, primarily, for switched network service while the 201B is normally used for dedicated line service. The sets operate at a fixed bit rate as established by an internal transmitter clock. Beginning and end of message codes must be supplied and recognized by the user terminal equipment.

Terminal output data bits must be synchronized with the data set transmitter clock, and input data bits sampled in synchronism with the data set receiver clock. The sets operate on a bit basis, making data communication independent of the user's format.

In two-wire half duplex operation, the data set receivers at both ends of the link are on during quiescent periods. When a terminal has data to transmit, it issues a "Request to Send" signal to its modem. The modem will return a "Clear to Send" signal to the terminal approximately 150 milliseconds later to indicate transmission may begin. The receiving end data set will issue a "Carrier On" signal to its terminal approximately 100 milliseconds after the sender's "Request to Send" is initiated, and will begin supplying receiver clock pulses to the terminal.

When the originating terminal has completed his transmission, the "Request to Send" signal is dropped, and the data set transfers back to the receiving condition. The receiving end data terminal is now clear to issue a "Request to Send" signal, wait for its data set's "Clear to Send" response, and begin transmitting. The 150 millisecond line turn-around delay may in special cases be optionally reduced to approximately 9 milliseconds where very short lines are used.

In four-wire full duplex operation, both terminals may leave their "Request to Send" signals active continuously, and transmission may be conducted by either terminal at any time.

1.1.2   Rixon SEBIT 48C Modem

This modem is designed for continuous 4-wire full duplex unattended operation over conditioned dedicated lines. Each end may transmit at will. The Request to Send signals at both ends are normally maintained active to maintain bit clock synchronism.

This modem can be set to operate at 4800, 4400 or 4000 bits per second by means of a panel switch.

1.1.3   Miscellaneous Modems

A number of other modems are available with compatible interface characteristics. The YHS/YHD system can be used with the majority of these data sets. The YHD Automatic Call Control option can be used only with data sets designed to interface with the Bell System 801A or 801C Automatic Call Units or equivalent.

1.2   Controller Description

The YHS controller provides the bi-directional control, serial/parallel data conversions, and computer to modem synchronization functions.

The YHD adapter provides data and control signal level conversion between the TTL logic used in the YHS assembly, and the EIA RS232B modem interface logic and control levels. The YHD also contains the control and interface adapters required for automatic dialing when this option is installed. The call control section interfaces directly with the Bell System 801A and 801C Automatic Call Units.

1.2.1   YHS Input Section

This section accepts serial data from the modem receiver, searches for synchronizing characters to establish byte grouping, assembles each 8-bit byte in a shift register for parallel transfer to the CPU, and checks parity of each byte. A service request is issued to the computer after each byte has been assembled. The parity check is a count of the number of ONE bits in a byte. If this count is even, bit 10 of the status indicator register is set to 1; if odd, bit 10 is 0.

This section has four basic operational states:

1.   Quiescent
2.   Armed
3.   Framing
4.   Run

The QUIESCENT state is entered in two ways:

A.   I/O Reset
B.   Data Set CARRIER OFF indication

In the quiescent state, the controller monitors the data set carrier detector for the CARRIER ON condition, which signifies received data is valid.

The ARMED state is entered in three ways:

A.   Recognition of CARRIER ON while in QUIESCENT state.
B.   Failure to achieve framing while in FRAMING state.
C.   Execution on ECO "RECORD SEPARATOR" command while in RUN state.

In the armed state, the input section monitors the incoming data line continuously for a one-to-zero transition indicating the start of transmission from the remote terminal.

The FRAMING state is entered by:

A.   Recognition of first one-to-zero transition while in ARMED state.

In the framing state, the controller tests the serial bit stream for an 8-bit sync character. When this character is recognized, the following 8 bits are assembled in the input shift register. This register is tested when full, and if the contents check as the sync character, framing is assumed and a service request issued to the CPU. If this byte is not the correct sync code, the controller drops back to the ARMED state, and again searches for the next one-to-zero transition.

The RUN state is entered when:

> A. Two contiguous identical sync characters are recognized while in the FRAMING state.

The controller remains in the RUN state after achieving framing until the data set CARRIER ON signal drops, or a Record Separator command is executed. The carrier off indication drops the controller to the quiescent state, while the record separator command drops it to the armed state.

The service request issued upon ahcieveing framing synchronization must be serviced with an EDI instruction to clear the register of the second sync character. Failure to service before another 8-bit byte has been assembled constitutes a timing error. The initial sync character is purged by the controller and does not require a data transfer to the computer.

While in the RUN mode, the controller input section accumulates each sequential group of eight bits following framing in the input shift register. Each group is checked for parity and a service request for a data transfer is issued. The 8 information bits are placed on the PDC data bus right byte lines in response to execution of an EDI instruction, wit the leading serial bit to A15, through the last serial bit to A08.

The parity check status bit is available via an ESI instruction.

Data and parity status are available for transfer following issuance of the service request for seven serial bit intervals before they are replaced by subsequent data. A data transfer (EDI) must be made within this interval to avoid error and data loss; parity status may be ignored (no ESI) or transferred at the programmer's option without causing a timing error.

1.2.2   YHS Output Section

This section accepts computer output data in 8-bit parrallel bytes, and serially shifts the data to the modem transmitter in synchronism with the data set clock.

Output data is placed in a holding register in response to an EDI instruction whenever this register is empty, and the data set is in a suitable operational mode. When the modem has been placed in the Clean to Send state in response to a computer "Request to Send" command, the holding register contents are transferred to a shift register for transmission to the data set. The buffer is then available for another output transfer, and a service request is issued to the CPU. This request must be serviced within seven bit-clock intervals to maintain frame synchronization for the remote receiving data set. Failure to do so constitutes a timing error.

This section maintains a "MARK HOLD" (logic ONE) level on the modem transmitter input line whenever data is not be transmitted.

The output section does not check nor generate parity.

With the automatic call control option installed in the YHD assembly, the four most significant bits of the holding register (accumulator bits 08, 09, 10 and 11) are used to present the BCD number digits of the station being called to the Bell System 801 automatic call unit (ACU). During this automatic dialing procedure, accumulator bits 12, 13, 14 and 15 are ignored and may be either ones or zeroes. Dialing timing for transfer of number digits to the controller is under control of the ACU. Each time the ACU is ready for the next digit to be dialed, the controller issues a service request for this transfer. After the computer has responded with the final number digit, an ECO "Dialing Complete" command must be executed to notify the controller this is the last such transfer.

1.2.3   YHS Address

The controller is assigned two 8-bit addresses, which are identical through the seven most significant bits. The input section is assigned a "1" least significant bit, while the output section is assigned a "0" least significant bit.

1.2.4   YHD Interface Adapter

The basic YHD assembly contains six line receivers and three line drivers which condition the modem bi-polar control and data signal levels to the zero/plus five volt levels compatible with the YHS integrated circuit logic levels.

The YHD assembly with the Automatic Call Control option installed contains three additional line receivers and six line drivers, as well as the control logic required to operate with the Bell System 801 series Automatic Call Units.

1.3   I/O Instruction

Computer/Modem/Auto Call Unit communications are normally controlled through the MAC 16 program interrupt structure. Service requests from either the controller input or output sections can be individually allowed or inhibited under program control.

Service requests are issued for the following conditions (basic YHD adapter without auto call option):

1.	Data Set goes to READY state.	(Output Section)
2.	Data Set goes to NOT READY state.	(Output Section)
3.	Input timing error.	(Input Section)
4.	Output timing error.	(Output Section)
5.	Input data available for transfer.	(Input Section)
6.	Output data can be accepted.	(Output Section)

With the automatic call option installed on the YHD assembly, service requests are also issued for:

1. Each ACU PRESENT NEXT DIGIT request.   (Output Section)
2. Abandon Call response from ACU.   (Output Section)

1.3.1   ECO - External Command Out

The M and N fields of the instruction define the controller section address. ODD binary number addresses select the INPUT section; EVEN binary number addresses select the OUTPUT section.

Bits 12, 13, 14 and 15 of the accumulator define the command. Bits 0 through 11 are ignored.

All commands are accepted and acknowledged regardless of the operating state of the controller and data set except REQUEST TO SEND and CALL REQUEST. (Sec. 1.3.1.7 and 1.3.1.10).

A service request is not issued in response to an ECO.

An Input-addressed ECO clears an active input service request.

An Output-addressed ECO accepted and acknowledged clears an active output service request.

1.3.1.1 Inhibit Output Interrupts. MN field = EVEN. Accumulator = XXX4.

This command drops an existing output section service request and prevents the issuance of further service requests. The section's "service required" status is not altered.

1.3.1.2 Inhibit Input Interrupts. MN field - ODD. Accumulator = XXX4.

This command drops an existing input section service request and prevents the issuance of further service requests. This section's "service required" status is not altered.

1.3.1.3 Allow Output Interrupts. MN field = EVEN. Accumulator = XXX8.

This command allows the output section to issue service requests as defined in Sec. 1.3. Execution of this command allows an existing "service required" status interrupt to be issued immediately.

1.3.1.4   Allow Input Interrupts. MN field = ODD. Accumulator = XXX8.

This command allows the input section to issue service requests as defined in Sec. 1.3. Execution of this command allows an existing "service required" status interrupt to be issued immediately.

1.3.1.5   CPU Terminal Ready. MN field = ODD. Accumulator = XXX9.

This command allows the data set to enter the data mode.

With the automatic answer data set option, this command allows an incoming call to be automatically answered.

With the automatic call unit option (ACU), this command must have been executed prior to execution of a Call Request command to enable the ACU to accept the request.

1.3.1.6   Terminal Off. MN field = ODD. Accumulator = XXX5.

This command forces the data set to exit from the data mode. With the automatic answer data set option, this command must be executed to terminate an incoming call and allow the data set to go on hook.

With the automatic call unit option (ACU), use of this command is determined by customer selection of one of two ACU disconnect options available. (See Sec. 1.3.6).

1.3.1.7   Request to Send. MN field = EVEN. Accumulator = XXX1.

This command causes the data set to activate its transmitter to send carrier to the remote terminal modem receiver. This command is not acknowledged unless the CPU data set is in the data mode.

1.3.1.8   End of Transmission. MN field = EVEN. Accumulator = XXX5.

This command causes the data set to deactivate its transmitter and cease sending carrier to the remote terminal modem.

1.3.1.9   Record Separator. MN field = ODD. Accumulator = XXX1.

This command causes the controller to drop its sync lock with an incoming data serial bit stream and sets the input section in the ARMED state.

1.3.1.10   Call Request. MN field = EVEN. Accumulator = XXX9.

This command is used only with the Automatic Call Unit option. This command is not acknowledged if the communication line is busy with an incoming call. If acknowledged, the 801 series Auto Call Unit goes "off hook" and obtains a communication line to its central exchange. Upon receipt of dial tone, the ACU causes the controller to issue a service request for the first digit to be dialed.

1.3.1.11   Dialing Complete.   MN field = EVEN.   Accumulator = XXXD

This command is used only with the Automatic Call Unit option. This
command signifies to the controller that all dialing digits have been
output. This command must be executed following the EDO transferring
the last dial digit, preferably within 20 microseconds.

1.3.1.12   Enable Disconnect.   MN field = EVEN.   Accumulator = XXXC

This command is used only with the Automatic All Unit option, and then
only following an acknowledged Call Request command, i.e,, a call
automatically dialed by the ACU is in progress.

Exact usage of this command is determined by customer selection of one
of two ACU disconnect options available. (See Section 1.3.6.11.).

1.3.2   EDO-External Data Out

The M and N fields of the instruction define the controller section address.
The N field is an EVEN binary number.

1.3.2.1   Data Transfer

If the EDO is acknowledged, the contents of the right byte of the accumulator
have been transferred to the output section holding register.

1.3.2.2   Acknowledge

An EDO will be acknowledged only when the holding register is available to
accept new data. This register is available:

> . when the previous byte has been transferred to the output
> section shift register for transmission to the modem, and
> the output timing error indicator is clear;

> . following execution of a Request to Send command and
> prior to the data set Clear to Send response. (See
> Section 1.3.6.3.); and

> . following an ACU service request to Present Next Digit.

1.3.3   EDI-External Data In

The M and N fields of the instruction define the controller section address. The N field is an ODD binary number.

1.3.3.1   Accumulator Contents

If the EDI is acknowledged, the contents of the Accumulator right byte shall be the last character received from the modem. The leading serial bit received shall be in A_{15} through the last serial bit received in A_8. A_7 through A_0 = 0. If an acknowledge is not issued, the content of the accumulator = 0.

1.3.3.2   Acknowledge

An EDI will be acknowledged when the controller has new data to transfer and the input timing error indicator is clear. The input section service request will be dropped.

1.3.4   EAI-External Address In

The M and N fields of the instruction are not used in the controller response to an EAI.

1.3.4.1   Accumulator Contents

The contents of the accumulator is the address of the controller section issuing a service request which has the highest precedence.

1.3.4.2   Acknowledge

An acknowledge is not issued in response to an EAI.

1.3.4.3   Service Request

The service request of the section responding is dropped.

1.3.5   ESI-External Status In

The M and N fields of the instruction define the controller section address. The N field is an ODD binary number for the input section; the N field is an EVEN binary number for the output section.

An acknowledge is not issued in response to an ESI.

An ESI will be accepted at any time.

1.3.5.1   Accumulator Contents-Input Addressed

The accumulator will contain the following status information, a "1" indicating the condition is true:

STATUS CONDITION	ACCUMULATOR BIT
Input Timing Error	13
Data Set Carrier On	12

1.3.5.2   Accumulator Contents-Output Section Addressed

The accumulator will contain the following status information, a "1" indicating the condition is true:

STATUS CONDITION	ACCUMULATOR BIT
Data Set Ready	15
Output Timing Error	13
Clear to Send	12
*Present Next Digit	11
*Abandon Call, Retry	9
*Data Line Occupied	8

*Used only with Automatic Call Unit option.

1.3.5.3   Service Request

The service request of the section responding is dropped.

1.3.5.4   Status Indicators

The Timing Error status indicator of the responding section is cleared.

The Abandon Call, Retry status indicator is cleared by an Output section addressed ESI.

The Carrier On status indicator is not altered.

The Data Set Ready status indicator is not altered.

The Data Line Occupied status indicator is not altered.

The Present Next Digit status indicator is not altered.

The Clear To Send status indicator is not altered.

1.3.6   Programming Requirements

1.3.6.1   General Operation

Specific programming requirements depend on customer selection of options available with different modems, ACU options when the automatic call YHD option is used, 2 or 4 wire communication circuits, and remote terminal characteristics. The basic functions and procedures generally common to the majority of data link configurations are described below.

1.3.6.2   Preparation for Data Communication

The majority of applicable modems require a Data Terminal Ready signal to enable the data set to transmit and receive data. The controller must be placed in this mode by the ECO CPU TERMINAL READY command. This primes the data set to accept incoming calls if the automatic answering option is used; to enter data communication mode if manual answering is used; to place a call to a remote terminal if the automatic call unit option is used. The controller must be maintained in this mode until data communication is finished.

1.3.6.3   CPU Data Out–Data Link Established

The modem must be enabled to transmit and the remote terminal modem establish receiving bit synchronization before data can be output from the computer. The controller must be placed in this mode by the ECO REQUEST TO SEND command, followed shortly (preferably within 100 microseconds maximum delay) by an EDO SYNC character. This SYNC character is the ASCII SYN code 96_{16} for the standard YHS assembly.

No further CPU service is required after issuing the EDO SYNC word until an interrupt signal, CLEAR TO SEND, is received from the modem. The request should be serviced by a second EDO SYNC (96_{16}) within 7 data set bit times. The controller will issue another service request as soon as this second SYNC byte has been cleared from the holding register. This interrrupt, and subsequent ones issued after each new byte has been cleared, must be serviced by EDO instructions outputing the desired data. Each EDO must be issued within the 7 data set bit time limit to avoid a timing error, which would normally result in loss of character framing by the receiving terminal.

1.3.6.4   CPU Data Out-Transmission Completed, Prepare for Data In

The CPU should terminate its output message using the end of message format
established for the particular remote terminal being accessed.   The final EDO
byte should be FF_{16} (Rubout).   The service request generated when this
character is cleared from the holding register should be servied by an ECO
END OF TRANSMISSION. This command will shut down the modem transmitter
and allow the remote terminal to issue a request to send signal to its data set.

NOTE: The final EDO rubout character is not actually transmitted
         to the remote terminal, but is a "filler" for the controller
         while the previous EOM character is being serially trans-
         mitted. If this EDO is not issued, a timing error would
         result and a service request issued.   In this event, an ESI
         is required to clear this condition, as well as the ECO EOT
         command.

1.3.6.5   CPU Data In-Data Link Established

Assuming half-duplex operation, and the previous communication being CPU
Data Out, the controller input section will be in the quiescent state.   Shortly
after the remote terminal issues a Request To Send to its modem (approxi-
mately 9 milliseconds) the CPU-end modem will issue its CARRIER ON signal
and generate receiver clock pulses.   The input data line will be at "Mark
Hold" until the remote terminal transmits its first SYNC 96_{16} character. This
will be tested by the controller, and the second SYNC character checked. As-
suming framing is achieved, the controller will issue a service request to the
CPU.   This should be serviced by an EDI within seven (7) serial bit intervals
time.   The character can be checked or discarded by the program.   Each
ensuing 8-bit character received will initiate another service request, again
requiring service within the seven (7) bit time limit to maintain framing syn-
chronization.

1.3.6.6   CPU Data In-End of Transmission

As soon as the CPU recognized the completion of transmission from the re-
mote terminal, it should execute an ECO RECORD SEPARATOR command.
This will drop the input section of the controller to the Armed State.   If the
remote terminal drops its Request To Send signal following the transmission
of its final character, the controller input section will revert to the Quiescent
state.   In either (or both) events, it will be enabled to look for the start of a
new message.

If the final transmission from the remote terminal is not followed by either
of the above terminations (Record Separator command or remote terminal

dropping Request to Send) the controller will continue to issue service requests at the character framing rate.

1.3.6.7   Full Duplex Operation-Request to Send Maintained Active

Several possible programming methods may be followed.

A.   Assuming both terminals have achieved character framing, each can maintain this synchronization by servicing both input and output data interrupts to obviate timing errors.   The input transfer may be discarded, and FF_{16} output characters transmitted to maintain optimum bit synchronization signals on the line. With this mode of operation, either end may transmit at will, and transmission and receiving SYNC framing maintained without requiring further SYNC character outputing at the start of each new message.

B.   The remote terminal may place a "Mark Hold" signal on its send circuit and maintain this until ready to output a new message. The CPU in this case should issue a Record Separator command immediately after having received the EOM character from the previous message, thus entering the Armed State at the input section.   It is now necessary to re-achieve framing as described in paragraph 1.3.6.5, following the carrier on indication.

The controller output section will raise its timing error status indicator (and issue a service request when this first occurs) if the rubout characters are not transferred by EDO Instructions.
The interrupt signal may be suppressed by execution of an ECO INHIBIT OUTPUT INTERRUPTS. It is then necessary to clear the timing error status by an output section ESI before transmitting new data.   Output interrupts should also be allowed.   It is possible that a new timing error status may occur between the clearing of the suppressed interrupt status and execution of the EDO instruction.   This may happen if the data set transmit clock transition indicating start of a new word occurs between execution of the ESI and EDO instructions. In this event, the EDO will not be acknowledged and a new timing error interrupt issued.   A second ESI and EDO must be executed, re-presenting the output character.

Output data requirements to re-establish remote terminal receiver framing using this mode of operation must be determined for the particular terminal characteristics.

1.3.6.8   CPU Automatic Call Answering

Assuming the data set has the automatic call answering option installed, the CPU must condition the controller and modem to accept incoming calls by

executing an ECO CPU TERMINAL READY command. When the modem has accepted the call and entered the DATA state, a service request is issued. This should be serviced by an ESI addressed to the output section. This status byte should indicate DATA SET READY (Bit 15 = 1). Communication may now be initiated by either end as discussed in paragraphs 1.3.6.3 through 1.3.6.6.

1.3.6.9   CPU Automatic Line Disconnect-No ACU

When the CPU is ready to terminate an incoming call which was answered either automatically (paragraph 1.3.6.8) or manually by an operator who transferred the modem to the data mode by means of the Bell System 804 Data Auxiliary Set, it must issue an ECO TERMINAL OFF command. The controller will issue a service request approximately 150 milliseconds later. This request should be serviced by an ESI instruction addressed to the output section. This status byte should indicate DATA SET NOT READY (Bit 15 = 0). This status assures that the line disconnect has been completed, and an ECO CPU TERMINAL READY may now be executed to prime the data set to answer a subsequent incoming call.

1.3.6.10   CPU AUTOMATIC Call Origination-ACU Option

An ECO CPU TERMINAL READY command must be executed to condition the controller, data set and automatic call control unit for communication. An ESI may be issued to the output section to determine if the communication line is busy or available. (The line may have been occupied by an incoming call). If the line is busy, the status byte will indicate Data Line Occupied (Bit 8 = 1). If the line is being used for data communication, this byte will also indicate Data Set Ready (Bit 15 = 1) and may or may not indicate Clear to Send or Output Timing Error, depending upon the immediate status.

If the status byte indicates the line is available (Bits 8, 9, 11, 12 and 15 all equal 0), an ECO CALL REQUEST may be executed. (If this command is issued while the line is busy, it will not be acknowledged). No further CPU action is required after the call request is issued until the ACU issues a Present Next Digit signal to the controller. This initiates a service request to the CPU which should be serviced by an EDO instruction. The accumulator should contain the first digit number to be dialed in 8421 BCD format, with the highest order bit in A_8, through the lowest order bit in A_{11}. A service request will be issued each time the ACU raises its Present Next Digit line; these requests should be serviced with EDO instructions, the accumulator progressively containing the digit bits for each digit to be dialed. After the last digit has been output, the EDO should be followed by an ECO DIALING COMPLETE command. This command can be executed immediately following the EDO, and must be issued no later than ten milliseconds after the EDO.

A service request will be issued to the CPU sometime later. This may range from a minimum of approximately 200 milliseconds to a maximum of 40 seconds. This request should be serviced by an ESI. If the status byte indicates Data Set Ready (Bit 15 = 1) communication can begin as described in paragraph 1.3.6.3.

(The full status byte will be 91_{16}).

If the status byte indicated Abandon Call, Retry (Bit 9 = 1), the call has not been completed and the CPU should execute an ECO <u>ENABLE DISCONNECT</u> command. This will cancel the incompleted call request. Another service request will be issued from 175 milliseconds to approximately one second later, indicating the disconnect has occurred. This request should be serviced with an ESI to verify that status indicator bits 8 and 11 equal zero. A new try may now be made by again issuing a Call Request command.

1.3.6.11   Call Termination-CPU Originated Call, ACU Option

Two call termination options are available with the Bell System Automatic Call Units. The termination procedure differs for these two options as described below.

A.   ACU Call Termination Option Z (Bell 801A ACU); Terminate Call, after DSS goes ON, via Data Set (Bell 801C ACU).

With this option, the CPU must execute an ECO <u>ENABLE DISCONNECT</u> command followed by an ECO <u>TERMINAL OFF</u> command to allow both the automatic call unit and the modem to hang up and release the communication line. The Enable Disconnect command must not be executed while ACU dialing is in progress or the line will be released before the call is completed. This command should preferably be issued shortly after the service request which resulted on successful completion of the call (status byte 91_{16}, reference paragraph 1.3.6.10). This command is not required this early, but must be executed before the Terminal Off command is issued. The Terminal Off command is used as described in paragraph 1.3.6.9.

Incoming calls and calls placed manually via the Bell System 804B Data Auxiliary Set from the CPU terminal end are terminated as described in paragraph 1.3.6.9. The ACU has not been activated in this case, and it is not necessary to execute the Enable Disconnect command.

B.   Call Termination by ACU Via CRQ (Bell System 801A ACU); Terminate Call, after DSS goes ON, via CRQ (Bell 801C ACU).

These are the "normal" options for these two units.

With these options, the CPU must not rescind the CALL REQUEST command via an ENABLE DISCONNECT command until all data communication has been finished and it is desired to disconnect the line. With both models of the ACU, call termination is achieved by issuing the ENABLE DISCONNECT command only, when the call has been placed automatically by the CPU.

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Incoming calls, or manually dialed calls from the CPU end,
cannot be automatically terminated via the ENABLE DISCONNECT
command.   They may be terminated by executing the TERMINAL
OFF command.

SECTION IV

MAC 16 HARDWARE OPTIONS

MAC 16 HARDWARE OPTIONS

MAC 16 Hardware options are grouped into six types. These are:

1. Chassis with options,
2. Cabinets with options, panels and installations,
3. Power Supplies with options and cables,
4. Control Panels with options and harness lengths,
5. Input/Output cables,
6. Spare Parts including PC Modules.

CHASSIS – MAC, ECC, MEC, MCC

There are four models of chassis including the computer mainframe chassis, MAC. The other three are the External Controller Chassis, ECC; Memory Extension Chassis, MEC; and the Memory/Controller Chassis, MCC.

MAC – Mainframe Chassis

This is the computer mainframe card reset. It is designed for front insertion and mounting into a standard 19 inch RETMA relay rack. It requires 17-1/2 inches of front panel space. It is 17 inches deep.

The mainframe chassis contains 25 card guides for mounting standard size (CC104) MAC PC modules in slots 1 to 21, 23, 27, 28 and 30. It is manufactured with 13 pairs of card connectors plus one connector in slot 8 that contains the I/O interface   It is necessary to add connectors in slot positions 1 to 8, 20, 27, 28 and 30 when options are added to MAC.

ECC - External Controller Chassis

This chassis is the same as the mainframe chassis, MAC, except that it contains a full set of 30 pairs of card guides. It is used for Controller Options when there is no room in the mainframe for the total system requirements.

The ECC is also useful for special customer logic modules. Attention must be given to additional power requirements when this chassis is filled with special hardware. When this chassis contains MAC 16 Controllers it must also include a Line Receiver option, -LR or -GR, in slot 6.

MEC - Memory Expansion Chassis

This chassis is the same size as the other types of chassis, but it contains two rows of smaller PC cards (CC102) and up to three 8K x 16 or 8K x 18 memory stacks. It is used for memory expansion.

It can be located above, below or to the side of the mainframe chassis.

The MEC contains one 12 volt power supply and fan pack. It uses the computer's power supply for its other power requirements.

Cable connectors are provided on the MEC for "daisy chaining" up to three MEC's to the computer chassis.

MCC - Memory/Controller Chassis

This chassis contains two rows of smaller PC cards and up to two 8K x 16 or 8K x 18 memory stacks. Eight card slot locations are also provided for installation of large MAC 16 PC cards. The MCC is the same size as the other three types of chassis.

The MCC also contains a 12 volt power supply and a fan pack.

Chassis Options

Each chassis may contain several options. The mainframe chassis may contain any of the Processor Options.

All three chassis: MAC, ECC and MCC may contain any of the Controller Options that were described in S-45. When controller options are designated for an external chassis (such as ECC-HC-M9-CD-LR) they are assigned the same slot positions as they are in the mainframe. This is shown in Table 1.

Table 2 presents the claim level for slot assignments in external chassis. The lowest numbered claim has highest priority. Other option combinations will require special wire list generation.

TABLE 1. ECC or MCC Controller Slots

Controller Option	Designator	PC Card	Slot
First Teletype	-TC1	YAD	9 (ECC only)
Second Teletype	-TC2	YAD	7
Third Teletype	-TC3	YAD	8
High Speed Paper Tape	-HC	RAD	8
External Data Input	-XI	EIC	4
External Data Output	-XO	EOC	5
Drum	-DM	DCB DCA	1 2
	-DN	DCB DCA	7 8
Line Printer	-LP	LPC	3
Card Reader	-CD or -CG	CRC	7
Magnetic Tape	-M9 or -M7	MTC MT9 or MT7	2 1
Data Modem, Low	-YM	YAM	7
Data Modem, High	-YS or-YD	YHS YHD	1 2
Line Receiver	-LR or -GR	ICB-2 or GAR	6
Line Driver	-LE or -GE	ICB-1 or GAD	7

TABLE 2. ECC or MCC Slot Claims

Slots	1	2	3	4	5	6	7	8	9
Claim 1	-YS or -YD		-LP	-XI	-XO	-LR or -GR	-LE or -GE	HC	-TC1
Claim 2	-DM						-CD or -CG	-TC3	
Claim 3	-M9 or -M7						-TC2		
Claim 4							-DN		

The memory expansion chassis, MEC and MCC require specification of the size of memory that they contain, such as MEC-16.

Fan Packs: -FP, -FV, -FN

All MAC 16 hardware requires that the air is kept moving at 100 cubic feet per minute. This can be provided with one of three fan-pack options. All four chassis are designed for mounting a fan pack assembly within their base without requiring additional rack panel height. A two fan assembly, -FP, is provided for MAC without options installed in slots 1 through 8. A triangle assembly of three fans, -FV, is provided for MAC with options installed in any of slots 1 through 8. A straight line assembly of three fans, -FN, is provided for each the ECC chassis as an option. This fan assembly is provided as a basic part of the MEC and MCC chassis.

CABINETS CSN, CSP, CRR

There are two standard size cabinets provided with removable back and side panels and an air filter. One is 30 inches high and the other is 61 inches high. There are two versions of the 30 inch cabinet. One comes with a Control Panel mounted on its table top. This is Model CSP and it can contain a computer chassis and a power supply. A three foot control panel harness (-H3) must be provided with this cabinet. The other 30 inch cabinet is Model CSN. It does not contain a Control Panel on its table top. It is primarily used for system expansion purposes. Both 30 inch cabinets provide 22-3/4 inches of 19 inch relay rack mounting. They are 25 inches wide and 24 inches deep. They must be provided with the fan pack option. All MAC 16 cabinets are designed so that they may be bolted side by side. The unexposed side panels are removed to facilitate cabling between the cabinets. Three option kits are provided such that two short cabinets may be connected, SCS; two tall cabinets may be connected, TCT; and a short and tall cabinet may be connected, SCT.

The 61 inch cabinet is model CRR. It provides 54-1/4 inches of 19 inch relay rack mounting. It is 25 inches wide and 24 inches deep.

Cabinet Options: -TS, -TR

One option is provided with each cabinet. This is the provision of aluminum extrusion trim rails on each side of the front of a cabinet. For the cabinet models CSN and CSP this option designator is: -TS. For the CRR cabinet this option designator is -TR.

Cabinet Panels and Doors: -D, -DS, -KP, -C01 through -C20

The front of each cabinet requires panels or doors to cover installed equipment or spaces to eliminate air flow leakage.

The lowest or bottom cover can be a "door". It is not a hinged door but it is a panel that is secured with two pins along the bottom edge so that it can be swung out from the top. The door is available in two heights: 21 inches, option -D; and 17-1/2 inches, option -DS. When the 17-1/2 inch door is used, a 3-1/2 inch snap-on kick panel should be used under this door. This is option -KP.

Snap-on front panels are available in sizes from 1-3/4 inches to 35 inches in increments of 1-3/4 inches. Model designators for these panels are -C01 through -C20.

Installations: -R1 through -R5, -S1

Installation drawings are provided for different configurations of I/O devices, chassis and panels. To date there are five installations for the tall cabinet, CRR, and one for the short cabinet CSP. Marketing is currently developing other "basic" installation drawings.

The short cabinet installation, -S1, contains a 5-1/4 inch power supply and a 17-1/2 inch MAC chassis.

The following five installations for the CRR cabinet are available:

	Equipment	Designator	Panels	Inches
-R1				
	Remote Control Panel	CP -H3 or CK-H3	-B	10-1/2
	HSPT Reader	PRS or PRN		7
	HSPT Punch	PPS or PPN		10-1/2
	Blank Panel		-C02	3-1/2
	Power Supply	PL or PA	-D	5-1/4
	Processor	MAC		17-1/2
	Air Filter, Kick Panel		-KP	1-3/4
				56
-R2				
	Remote Control Panel	CP-H3 or CK-H3	-B	10-1/2
	blank panel		-C12	21
	Power Supply	PL or PA		5-1/4
	Processor	MAC		17-1/2
	Air Filter, Kick Panel		-KP	1-3/4
				56
-R3				
	Control Panel	CP-HS or CK-HS	-B	–
	& Processor	MAC	-P	17-1/2
	blank panel		-C09	15-3/4
	Door over		-D	21
	Power Supply	PL-K4 or PA-K4		–
	Air Filter, Kick Panel		-KP	1-3/4
				56
-R4	(Non Standard)			
	Control Panel	CP-HS or CK-HS	-B	
	& Processor	MAC	-P	17-1/2
	HSPT Reader	PRS or PRN		7
	HSPT Punch	PPS or PPN		10-1/2
	Door over		-DS	17-1/2
	Power Supply	PA-K4 or PL-K4		
	Air Filter, Kick Panel		-KP	3-1/2
				56

-R5
      Control Panel   CP-HS or CK-HS   -B

      & Processor   MAC   -P   17-1/2

      HSPT Reader   PRS or PRN   7

      blank panel   -C04   7

      Door over   -D   21

      Power Supply   PA-K4 or PL-K4

      Air Filter, Kick Panel   -KP   3-1/2

                                                      56

POWER SUPPLIES PL, PA

There are two models of system power supplies. One is an assembly of four separate,
modular power supplies in a Lockheed, 5-1/4 inch chassis, PL. The other is a multiple
output supply that is custom designed for the MAC 16, PA. Both supplies provide four DC
voltage outputs; +5V, -6V, +18V and a temperature variable output of 21 to 32V.

The PA supply provides more output power than the PL supply and has master-slave, paralleling
capability on its +5V output for up to four units. It is intended that the PA supply will replace
the PL supply.

Table 3 summarizes the output currents of the two supplies.

Detailed information regarding the power supply specifications can be found in the Power
Supply Maintenance Manual, TM1009000188 for the PL Model and specification control drawing
1007000039 for the PA Model.

TABLE 3. Power Supply Currents

POWER SUPPLY ASSEMBLY	POWER OUTPUT (CURRENT IN AMPERES)			
	+5V	-6V	+18V	Memory Drive Voltage
Model PA 1005000550 (Mfg. Ault, Inc.) with 0°C to +60°C input air at 100 CFM	0-21A	0-3A	1.0A-4.2A	(21V to 32V range); 0-10A @ 32V
Model PL 2003000188 (Mfg. Lambda/LEC) ambient operating temperature -20°C to +60°C with convection cooling.	0-8A	(0-7V range); 0-1.4A	0-4.7A	(22V to 32V range); 0-3.9A @ 32V

The system designer must consider power requirements as memory is expanded and options are added.

Power Supply Options -FL, -FS, -PD

Both power supply models may be provided with a "fail-safe" option. This is the detection of a powe line failure and the generation of an interrupt signal to the computer at least 250 microseconds before output power falls below usable levels. A threshold control (screwdriver adjustable from the power supply front panel) allows the circuit interrupt trip point to be set between 110 to 100 VAC.

The fail-safe option for the PL model is designated -FL. The fail-safe option for the PA model is designated -FS. Fail-safe is the only option provided with the PL model.

A combination of four useful options is provided with the PA model. These are the line failure detection (above) plus line recovery detection, a line frequency pulse and a relay contact closure. The combination option is designated -PD.

The line recovery detection is the provision of an automatic reset and restart signal to the computer and an interrupt signal when the line power is above an adjustable threshold. This threshold is also screwdriver adjustable.

The line frequency pulse electronics provide one interrupt signal (pulse) to the computer for each full cycle of the AC input line. Line frequency may range from 47 to 63 Hz. This interrupt signal may be used by the programmer for special functions such as interval timing, elapsed time counting and alarm clocks.

The relay contact closure is used to signal the loss of either -6V, +5V or +21 to 32V regulated outputs. It is used as an alarm to signal this failure condition.

Power Supply Cables: -KS, -K2, -K4

Power supply cables are provided for the -6V, +18V and the 22 to 32V outputs. These cables may be the standard length of two feet, -KS, or they may be, optionally, four feet, -K2, or six feet, -K4, in length.

The +5V output and its return are distributed with 14 gauge, multiple stranded, insulated wire. It is also provided in 2, 4 and 6 foot lengths.

CONTROL PANELS CP, CK

The two models of control panels are the same except that one, CK, contains a keylock. The keylock is not treated as an option because it is not added to the standard panel, CP. It must be provided when the control panel is originally assembled.

The keylock, when "on", inhibits the function of all control panel switches except the SOP switch (set zero priority). This allows the computer to be locked on or off.

A description of the control panel and its functions may be found in Section 6 of the Computer Reference Manual.

Control Panel Options - B, -P

Two control panel options are related to the covering of the panel and the bottom of a 17-1/2 inch chassis to which it may be attached. A plastic bezel, -B, that is a "picture frame" is available to snap over the 10-1/2 inch control panel. This provides an air seal when the panel is attached to a chassis in a cabinet. It contains the company name and MAC 16 logo.

A seven inch snap-on panel, -P, is provided to cover the bottom of the 17-1/2 inch chassis.

Control Panel Harness -HS, -H3, -H8, -H13, -H20

As an option, the control panel may be located remote from the MAC chassis. This is possible with the provision of various control panel harnesses. The standard harness length, -HS, is used when the panel is hinged to the MAC chassis. Other harness lengths are 3, 8, 13 and 20 feet.

I/O CABLES IOC5, IOC10, IOC20, IOC30, IOC40, IOC50

A standard cable is available for system interconnection. It is capable of handling 20 signals with 20 twisted pair lines. Each cable end is terminated with a Winchester MRAC41P connector at both ends. 24 gauge stranded wire is used.   .

The cables may be 5, 10, 20, 30, 40 or 50 feet in length. At present only lengths up to 20 feet are available.

A set of three cables is required for extension of the computer's Programmed Data Channel (PDC) to external device controllers that require a 16 bit data communication. A set of two cables is required for device controllers that require an 8 bit (or less) data communication.

SPARE PARTS LWV, LGH, ICP, CNC, CNR

All of the Processor, Memory, Controller and Hardware Options that have been described may be purchased as separate models with options. Furthermore, each logic card of the computer may be purchased separately.

Two other PC cards are available for logic building blocks. They are provided without IC components so that the customer may select the desired types of components. One card, the LWV, contains dual-in-line-package, space for ten integrated circuits. This card is standard MAC 16 size with two 72 pin connector pads. All circuit leads are brought to the external connectors for wiring of special functions.

A second card has dual-in-line-package space for up to 112 integrated circuits. Wiring of these circuits is with jumpers on the board or with special wire-wrap IC sockets. When the wire-wrap IC sockets are used, this board requires two chassis slot positions.

A package of TTL, SN74 series, integrated circuit components, ICP, may be purchased as MAC 16 spares. At least one of every type component used is provided or 10% of the quantity in the basic computer not to exceed 10 is provided.

Two spare connector packages with mounting hardware are available. A package containing two PC module, 72 pin, connectors, CNC, is provided. A package containing one Winchester, MRAC41P connector for mating the I/O cables is provided, CNR.

jc

SECTION V

CARD SLOT ASSIGNMENTS FOR OPTIONS

OPTION SLOT ASSIGNMENTS

Table 1 lists the options by name and designator. Note that many options have two designators. This is because more than one slot assignment has been given to these options. Note also that slot assignments for some options vary between the two computer models: MAC 16 and MAC 16D.

Tables 2 and 3 display the claim level for each slot position. The lower numbered claims have highest priority. Tables such as these can be used by the system designer to select mainframe otpions by circling or marking the desired options. It can be seen that slot assignments have been assigned such that useful computer systems can be configured with all option cards contained in the mainframe.

Slot assignments in the external chasses ECC and MCC are the same as those shown for the MAC 16.

Table 1. Option Slot Assignments

Option	Designator	Printed Circuit Cards	Slots	Model
Multiply/Divide	- MD	MPR, MPU	4, 5	MAC 16, MAC 16D
	- ME	MPR, MPU	1, 2	MAC 16, MAC 16D
Multiplex Data Channel Interrupts 1 and 3	- MC1, -I4	MDU, MDR, LAD-4	3, 4, 5	MAC 16, MAC 16D
Interrupts 1, 3 and 7	- MC2, -I8	MDU, MDR, LAD-8	3, 4, 5	MAC 16, MAC 16D
Interrupts 8 to 15	- MC , -I16	MDU, MDR, LAD-8	3, 4, 5	MAC 16, MAC 16D
Interrupts 1, 3 to 15	- MC4, -I16	MDU, MDR, LAD-16	3, 4, 5	MAC 16, MAC 16D
Interrupts 8 to 23	- MC5, -I24	MDU, MDR, LAD-16 and LAD-4 or LAD-8	3, 4, 5 7	MAC 16
	- MC5, -J24	MDU, MDR, LAD-16 and LAD-4 or LAD-8	3, 4, 5 6	MAC 16D
Interrupts 4, 8, 16	-I4 I8 I18	LAD-4 or LAD-8 or LAD-16	11	MAC 16
	-J4, -J8, -J16	LAD-4 or LAD-8 or LAD-16	11	MAC 16D
20, 24, 32	-I20, -I24, -I32	LAD-16 and LAD-4 or LAD-8 or LAD-16	11 7	MAC 16
	-J20, -J24, -J32	LAD-16 and LAD-4 or LAD-8 or LAD-16	10 6	MAC 16D
36, 40, 48	-I36, -I40, -I48	LAD-16, LAD-16 and LAD-4 or LAD-8 or LAD-16	11, 7 2	MAC 16
	-J36, -J40, -J48	LAD-16, LAD-16 and LAD-4 or LAD-8 or LAD-16	10, 6 2	MAC 16D
52, 56, 64	-I52, -I56, -I64	LAD-16, LAD-16, LAD-16 & LAD-4 or LAD-8 or LAD-16	11, 7, 2 1	MAC 16
	-J52, -J56, -J64	LAD-16, LAD-16, LAD-16 & LAD-4 or LAD-8 or LAD-16	10, 6, 2	MAC 16D
Line Driver	-LD	ICB-1	6	MAC 16
	-LE	ICB-1	7	MAC 16D
Line Receiver	-LR	ICB-2	1	MAC 16, MAC 16D
Cable Driver	-GD	GAD	6	MAC 16
	-GE	GAD	7	MAC 16D
Cable Receiver	-GR	GAR	1	MAC 16, MAC 16D
Bootstrap TTY	-BT	BAD-T	10	MAC 16
	-BY	BAD-T	9	MAC 16D
Bootstrap HSPT	-BH	BAD-H	10	MAC 16
	-BS	BAD-H	9	MAC 16D
Memory Interleave	-MI	Customer Specials	1-3	MAC 16, MAC 16D
1st Teletype Controller	-TC1	YAD	9	MAC 16
	-TD1	YAD	8	MAC 16D
2nd Teletype Controller	-TC2	YAD, YAD	9, 7	MAC 16
	-TD2	YAD, YAD	8, 6	MAC 16D

Table 1. Option Slot Assignments (continued)

Option	Designator	Printed Circuit Cards	Slots	Model
3rd Teletype Controller	-TC3	YAD, YAD, YAD	9, 7, 6	MAC 16
	-TD3	YAD, YAD, YAD	8, 6, 7	MAC 16D
High Speed Paper Tape Reader and Punch Controller	-HC	RAD	8	MAC 16
	-HD	RAD	6	MAC 16D
External Data Input Chan.	-XI	EIC	4	MAC 16, MAC 16D
External Data Output Chan.	-XO	EOC	5	MAC 16, MAC 16D
Drum Controller	-DM	DCB, DCA	1, 2	MAC 16, MAC 16D
	-DN	DCB, DCA	7, 8	MAC 16
Line Printer Controller	-LP	LPC	3	MAC 16, MAC 16D
	-LO	LPC	6	MAC 16, MAC 16D
Card Reader Controller for SR-300	-CD	CRC-1	7	MAC 16, MAC 16D
	-CE	CRC-1	6	MAC 16
Card Reader Controller for GDI-100	-CG	CRC-2	7	MAC 16, MAC 16D
	-CF	CRC-2	6	MAC 16
Magnetic Tape Controller 9 Track, 800 BPI	-M9	MTC, MT9	1, 2	MAC 16, MAC 16D
	-N9	MTC, MT9	7, 8	MAC 16
Magnetic Tape Controller 7 Track, 556 or 800 BPI	-M7	MTC, MT7	1, 2	MAC 16, MAC 16D
	-N7	MTC, MT7	7, 8	MAC 16
Data Modem Low Speed, Asynchronous	-YM	YAM	7	MAC 16, MAC 16D
Data Modem High Speed, Synchronous without dial up	-YS	YHS, YHD-1	1, 2	MAC 16, MAC 16D
	-YT	YHS, YHD-1	7, 8	MAC 16
Data Modem High Speed Synchronous with dial up	-YD	YHS, YHD-2	1, 2	MAC 16, MAC 16D
	-YE	YHS, YHD-2	7, 8	MAC 16

Table 2. MAC 16 Slot Claims

Slots	1	2	3	4	5	6	7	8
Claim 1	I52-64	I36-48	MI	MD		LD or GD	I20-32	HC
Claim 2	ME		MC5			CE of CF	MC5	
Claim 3	DM		MC1 to MC4			LO	N9 or N7	
Claim 4	M9 or M7		LP	XI	XO	T03	DN	
Claim 5	YS or YD						YT or YE	
Claim 6	LR or GR						YM	
Claim 7							TC2	

Table 3. MAC16D Slot Claims

Slots	1	2	3	4	5	6	7
Claim 1	J52-64	J36-48	MI	MD		J20-32	LE or GE
Claim 2	ME		MC5			J24	CD or CG
Claim 3	DM		MC1 to MC4			HD	YM
Claim 4	M9 or M7		LP	XI	XO	LO	TD3
Claim 5	YS or YD					TD2	
Claim 6	LR or GR						

MAIN FRAME OPTION CONFIGURATIONS

Table 4. MAC 16 Memory Options is used to develop the proper memory option designates such as -8, -4P, -4XD, etc. Any combination that includes an 8D is not allowed. This is not the case with the MAC 16D. The internal memory size -0, -4 or -8 must be designated. The remaining four options are optional.

Table 5. MAC 16 Mainframe Options is used to assure that card slot positions are available for different combination of options.

To use Table 5, first select Processor Options. Note the slots used. Then select Controller Options in the non-used slot positions.

Any combination of options that cannot be configured from Table 2 will require engineering development.

TABLE 1. MAC 16 MEMORY OPTIONS

INTERNAL MEMORY SIZE	-0					SELECT ONE
	-4					
	-8		NO D			
EXPANSION CAPABILITY		X				SELECT NONE OR ONE
DIRECT MEMORY ACCESS			D			SELECT NONE OR ONE
PARITY				P		SELECT NONE OR ONE
PROTECT					T	SELECT NONE OR ONE

WRITE SELECTION HERE

MAC 16- | | | | |

TABLE 2. MAC 16 MAINFRAME OPTIONS

PROCESSOR OPTIONS

PROCESSOR OPTIONS	1	2	3	4	5	6	7	8	9	10	11	SELECT
											-I4,-I8 -I16	
							-I20,-I24 -I32				✓	
INTERRUPTS		-I36,-I44 -I48					✓				✓	SELECT ONE
	-I53,-I56 -I64	✓					✓				✓	
BOOTSTRAP TTY										-BT		SELECT NONE OR ONE
BOOTSTRAP HSPT										-BH		
LINE DRIVER ONLY						-LD						
CABLE DRIVER ONLY						-GD						
MULT/DIV. ONLY				-MD								
MULTIPLEX DATA CHAN. ONLY				-MC1							-I4+	
				-MC2							-I8+	
				-MC3							-I8+	
				-MC4							-I16+	
				-MC5			-I24+				✓	
MULT/DIV & LINE DR.				-MD	/LD							
MULT/DIV & CABLE DR.				-MD	/GD							
MULTIPLEX DATA CHAN. & LINE DRIVER				-MC1/LD							-I4+	
				-MC2/LD							-I8+	
				-MC3/LD							-I8+	
				-MC4/LD							-I16+	SELECT NONE OR ONE
				-MC5/LD			-I24+				✓	
MULTIPLEX DATA CHAN. & CABLE DRIVER				-MC1/GD							-I4+	
				-MC2/GD							-I8+	
				-MC3/GD							-I8+	
				-MC4/GD							-I16+	
				-MC5/GD			-I24+				✓	
MULTIPLEX DATA CHAN. & MULT/DIV			-MC1/ME								-I4+	
			-MC2/ME								-I8+	
			-MC3/ME								-I8+	
			-MC4/ME								-I16+	
			-MC5/ME				-I24+				✓	
MULTIPLEX DATA CHAN., MULT/DIV & LINE DRIVER			-MC1/ME/LD								-I4+	
			-MC2/ME/LD								-I8+	
			-MC3/ME/LD								-I8+	
			-MC4/ME/LD								-I16+	
			-MC5/ME/LD				-I24+				✓	
MULTIPLEX DATA CHAN., MULT/DIV & CABLE DRIVER			-MC1/ME/GD								-I4+	
			-MC2/ME/GD								-I8+	
			-MC3/ME/GD								-I8+	
			-MC4/ME/GD								-I16+	
			-MC5/ME/GD				-I24+				✓	
CONTROL PANEL HARNESS											-HS	
											-H3	
											-H8	SELECT ONE
											-H13	
											-H20	

CONTROLLER OPTIONS

CONTROLLER OPTIONS	1	2	3	4	5	6	7	8	9	10	11	-	
HSPT READER-PUNCH								-HC					SELECT NONE OR ONE
1, 2 OR 3 TELETYPES						-TC3	-TC2		-TC1				SELECT NONE OR ONE
MAGNETIC DRUM	-DM						-DN						SELECT NONE OR ONE
MAGNETIC TAPE	-M9						-N9						SELECT NONE OR ONE
LINE PRINTER			-LP			-L0							SELECT NONE OR ONE
CARD READER						-CE							SELECT NONE OR ONE
EXTERNAL INPUT				-XI									SELECT NONE OR ONE
EXTERNAL OUTPUT					-X0								SELECT NONE OR ONE
DATA MODEM SLOW							-YM						SELECT NONE OR ONE
MODEM HIGH SPEED	-YS						-YT						SELECT NONE OR ONE
MODEM HIGH DIAL	-YD						-YE						SELECT NONE OR ONE
LINE RECEIVER	-LR												SELECT NONE OR ONE
CHECK USED SLOTS									-TC_	-B__	-I___	-H__	

Table 2. MAC 16 Mainframe Options

5-9/5-10