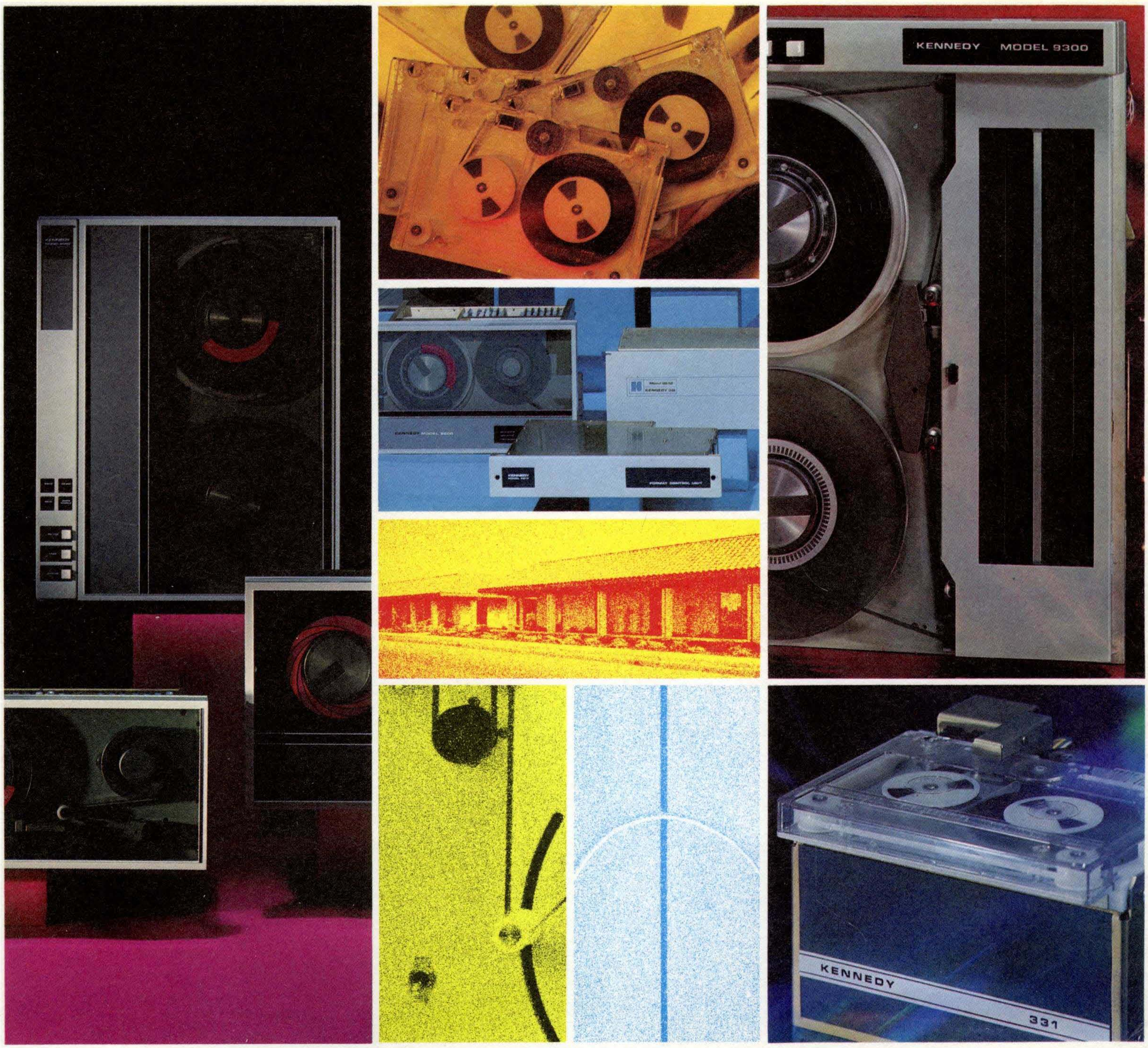
Operation and maintenance manual

KENNEDY CO.

MODEL 9832	PART NO. 192-9832-094	INTERFACE STD
SPEED 25 IPS	DENSITY 800 CPI	TRACKS 9
MODIFICATIONS 512 BUFFER		

Model 9832
Buffered Tape Transport



Model 9832
Buffered Digital Magnetic Recorder

This manual consists of two volumes. Volume 1 describes the interface and formatter module circuitry, while volume 2 describes the tape transport portion of the unit. A parts list for the entire Model 9832 is provided in this first volume, making the parts list in volume 2 inapplicable. Sections 2, 3, and 4 are omitted from the first volume, since this material is covered in volume 2.

Volume 2 is the manual for the tape transport, describing the Model 9832 with the formatter module removed.

MODEL	PART NO.
9832	192-9832-094
INTERFACE	**TRACKS**
DTL/TTL ZERO TRUE	9
SPEED (IPS)	**DENSITY (BPI)**
25	800
MODIFICATIONS	
512 BUFFER	
DATA RATE (CHARACTERS/SEC)	
WRITE	**READ**
ASYNCHRONOUS 0 TO 250 kHz. NO DATA LOSS: 800 BPI 10.3 kHz	ASYNCHRONOUS 0 TO 250 kHz

SECTION I

APPLICATION DATA

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APPLICATION DATA

1.1 INTRODUCTION

The Model 9832 consists of a Model 9800 synchronous tape transport with a built-in buffered formatter. The formatter is modular and has been mechanically integrated into the Model 9800 tape transport, and is electrically connected to the 9800 input/output plugs by means of a connector board at the end of a cable from the formatter module. It derives its power from the Model 9800 tape transport.

The door, which contains the controls and indicators, is changed to provide an END OF FILE pushbutton and a DATA IN MEMORY indicator.

If the connector board from the formatter module is removed, the normal I/O connectors for a 9800 are exposed, and the unit may be used or tested as a standard 9800, and may be connected to an interface designed for it.

The unit provides a simplified interface that can accept or supply data asynchronously at data rates of 0 to 250,000 characters per second. Data will be accepted without interruption if the average data rate over the period of one record does not exceed the rate shown in Figure 1-1. When the data rate exceeds this value, a busy signal appears at the interface, which may be used to control the source to interrupt data.

The interface contains two independent memories, each of which is capable of storing a complete record of the length specified for the particular machine (512, 1024, 2048 character blocks).

Incoming data is fed into an empty memory and the input data stream is transferred to the other memory when an end of record command is received, or when the memory capacity is filled. As soon as a memory is filled, a readout to tape takes place. This is the limit which establishes the maximum operating frequency for no data loss shown in Figures 1-1 and 1-2.

A busy signal is available to the interface if a memory is not empty when the opposite memory has been filled. This busy signal may be used to control the data source to stop data in this condition. The busy signal may also appear in machines equipped with read after write check if a read error occurs and the block must be rewritten. The busy signal occurs within 2 microseconds after the end of record command which caused the busy condition. Additional inputs include the end of record command, which will terminate a record and which should be applied within the buffer length specified. An end of file input is also provided to generate the end of file sequence on tape.

All formatting electronics - parity generator, cyclic redundancy check character generator, gap control, etc. - are included within ther system. The standard tape speed is 25 inches per second.

The 9832 can be supplied configured for nine-track 800 bpi operation or seven-track 200, 556, and 800 bpi operation. Read after write check with automatic backspace, erase, and rewrite is standard in both the seven- and nine-track configurations.

1.2 MODEL DESIGNATIONS

The Model 9832 is an 8.5 inch reel synchronous tape transport with a built-in read/write buffered formatter. Read after write check is standard, and automatic retry on tape error is standard.

1.3 ELECTRICAL AND MECHANICAL SPECIFICATIONS

A summary of specifications for the Model 9832 series is shown in Table 1-1.

1.4 CONTROLS AND INDICATORS

Controls and indicators are shown in Figure 1-4.

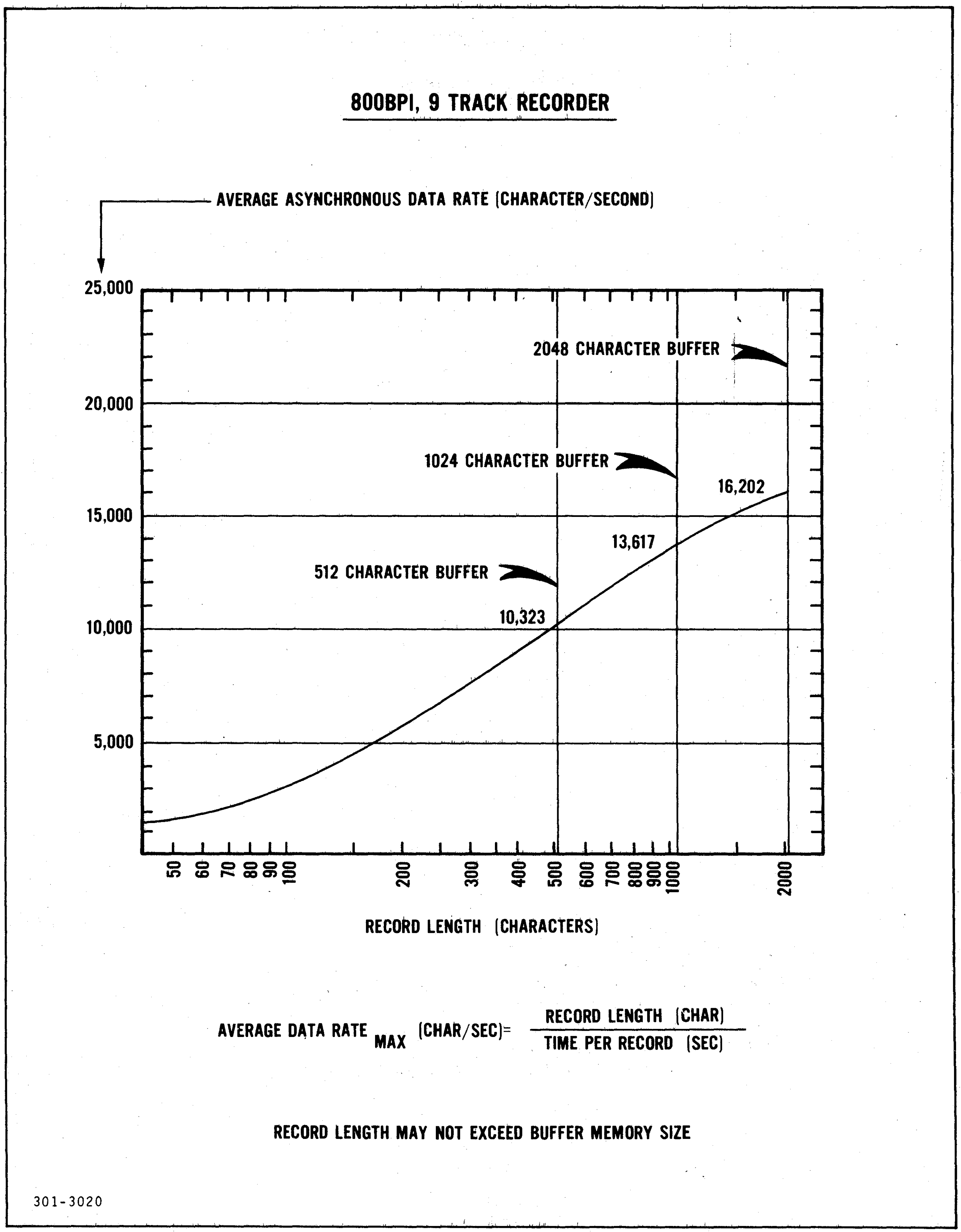
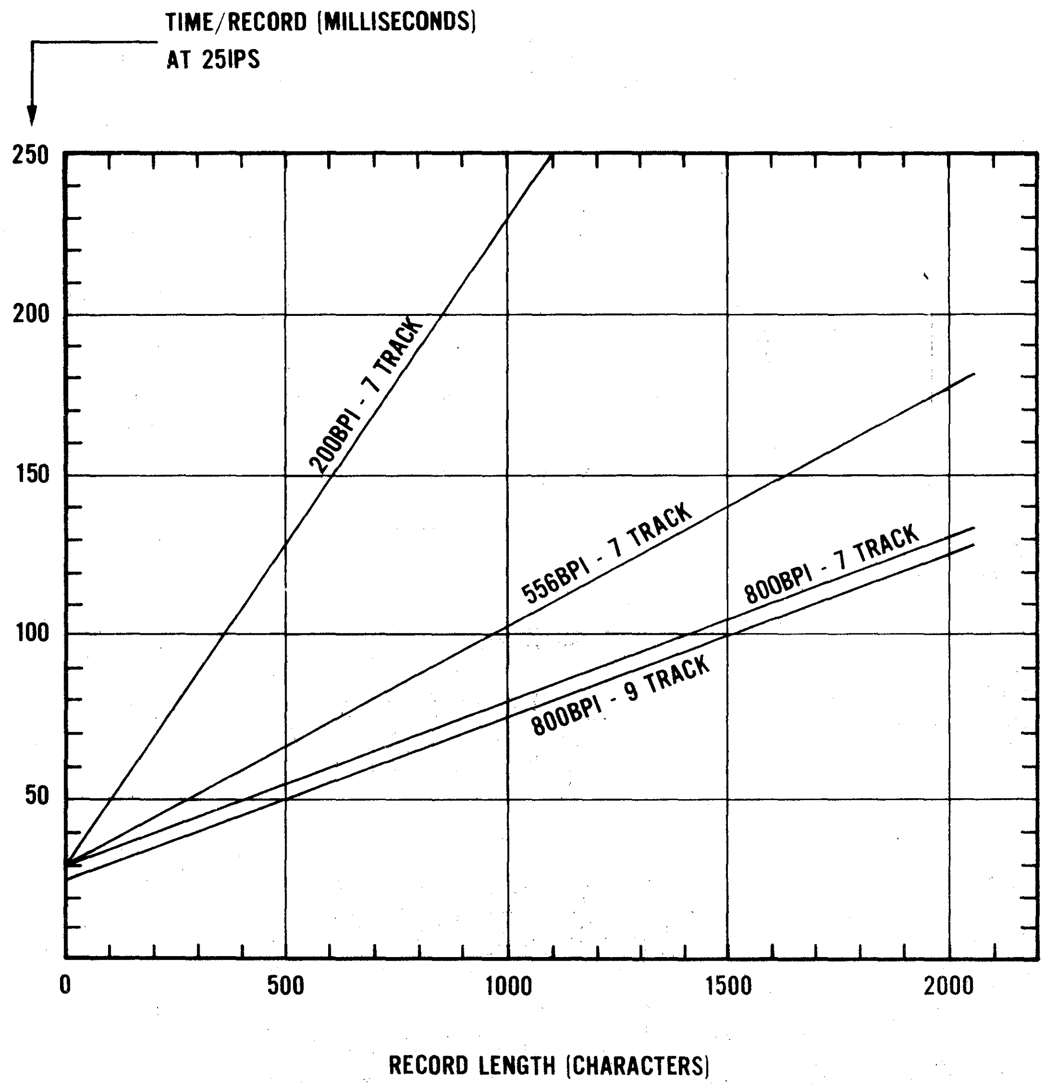


Figure 1-1. Maximum Average Asynchronous Data Rate as Function of Record Length and Recorder Speed

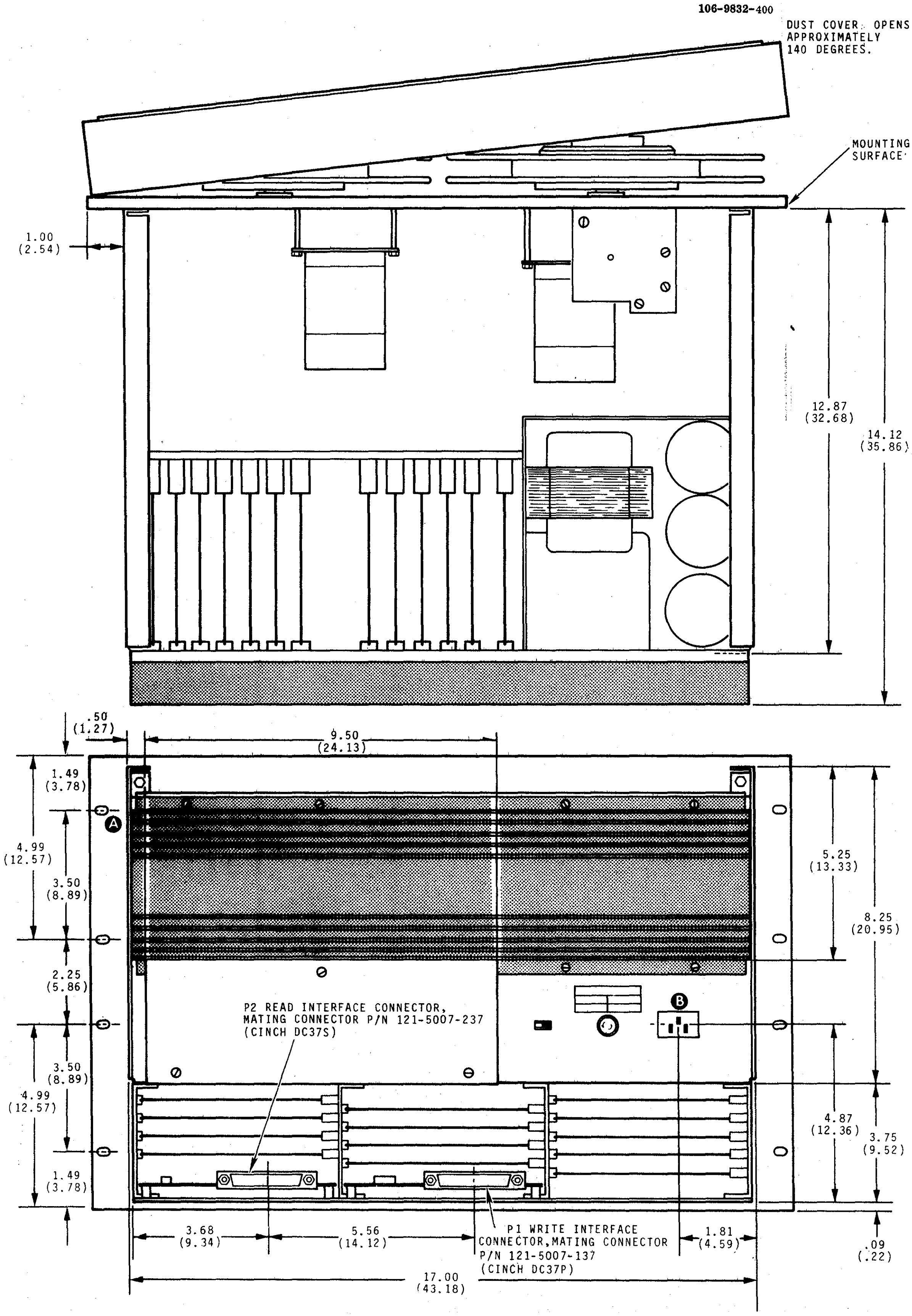


$$\text{TIME/RECORD (SECOND)} = \frac{K + \dfrac{\text{RECORD LENGTH (CHARACTERS)}}{\text{DENSITY (CPI)}}}{\text{SPEED (IN./SEC)}}$$

K = 0.60 FOR 9 TRACK
K = 0.75 FOR 7 TRACK

301-3021

Figure 1-2. Time Required to Execute One Record as Function of Record Length



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B INPUT POWER CONNECTOR (POWER CABLE 125-0068-001 SUPPLIED WITH UNIT)

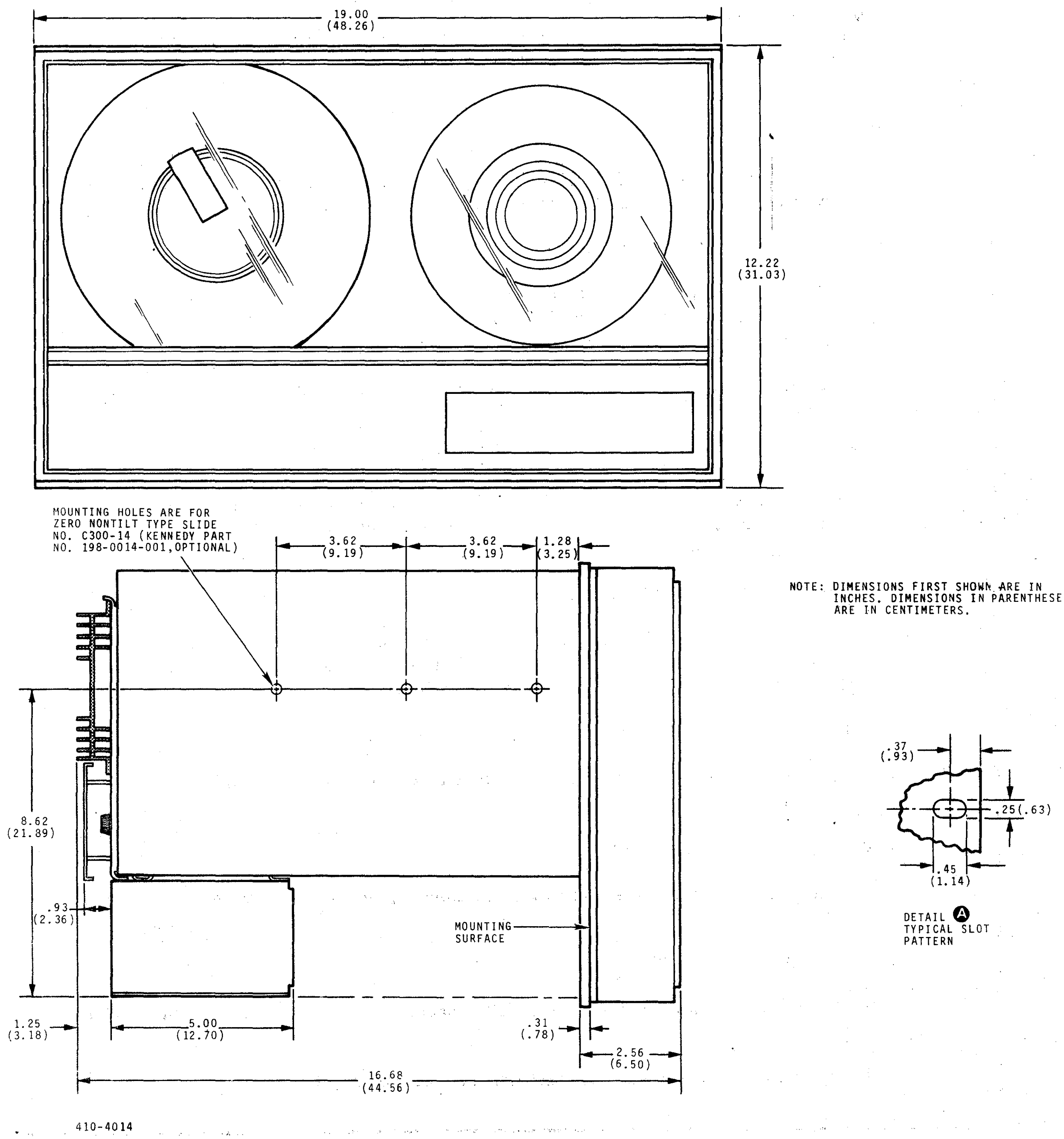
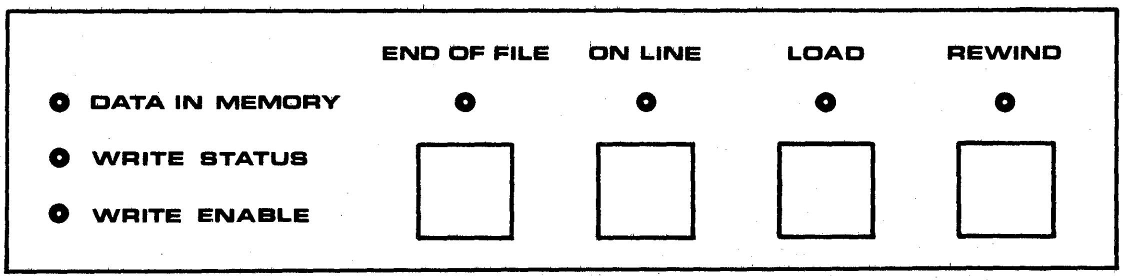


Figure 1-3. Outline and Installation Drawing, Model 9832



END OF FILE PUSHBUTTON/INDICATOR

A momentary pushbutton, which is used to generate an end of file sequence before rewinding the tape if these commands are not generated from the customer interface.

ON LINE PUSHBUTTON/INDICATOR

A momentary pushbutton, which functions as alternate action. When first activated the tape unit is placed in an on-line condition; when the tape unit is on line it can be remotely selected and will be ready if tape is loaded to or past the load point. When activated again it takes the unit off line. The LED indicator is illuminated in the on-line condition. A short time lag is built in between closure and action to prevent accidental operation.

LOAD PUSHBUTTON/INDICATOR

The momentary pushbutton activates the reel servos (tensions tape) and starts the load sequence. The LED indicator is illuminated when the reel servos are activated and tape is tensioned.

REWIND PUSHBUTTON/INDICATOR

The momentary pushbutton activates a rewind operation. This control is enabled only when tape is tensioned and unit is off line. The LED indicator is illuminated during either a local or remote rewind operation.

WRITE STATUS INDICATOR

This indicator is illuminated whenever tape unit is on line, selected, and write status is selected.

DATA IN MEMORY INDICATOR

Illuminated whenever there is data in the memory which has not been transferred to tape.

WRITE ENABLE INDICATOR

Illuminated whenever a reel with a write enable ring is mounted on the supply (file) hub.

LOAD and REWIND pushbuttons are disabled when the tape unit is on line.

Figure 1-4. Controls and Indicators

Maximum block length (specify)	512, 1024, or 2048 characters
Tape transport speed	25 ips
Density (specify)	200, 556, 800 bits/inch
Tracks (specify)	7 or 9 tracks
Zero data loss average transfer rate	See Figure 1-1
Incremental write and formatting	Standard
Read after write check and automatic correction	Standard
Incremental read	Standard
Automatic retry on read error	Standard
Memory error check	Option
Size (see Figure 1-3)	12.25 x 19 x 16.68" (31.1 x 48.3 x 42.4 cm)
Voltage	115v or 230v ±10%
Line frequency	50 to 60 Hz
Power	350 VA maximum
Weight	50 lb (23 kg)
Temperature	+2° to 50° C
Cooling	Convection

Table 1-1.
Summary of Specifications for Model 9832 Buffered Digital Magnetic Tape Transport

(Specifications are for buffered system. See Model 9800 manual for additional detailed specifications relating to tape transport.)

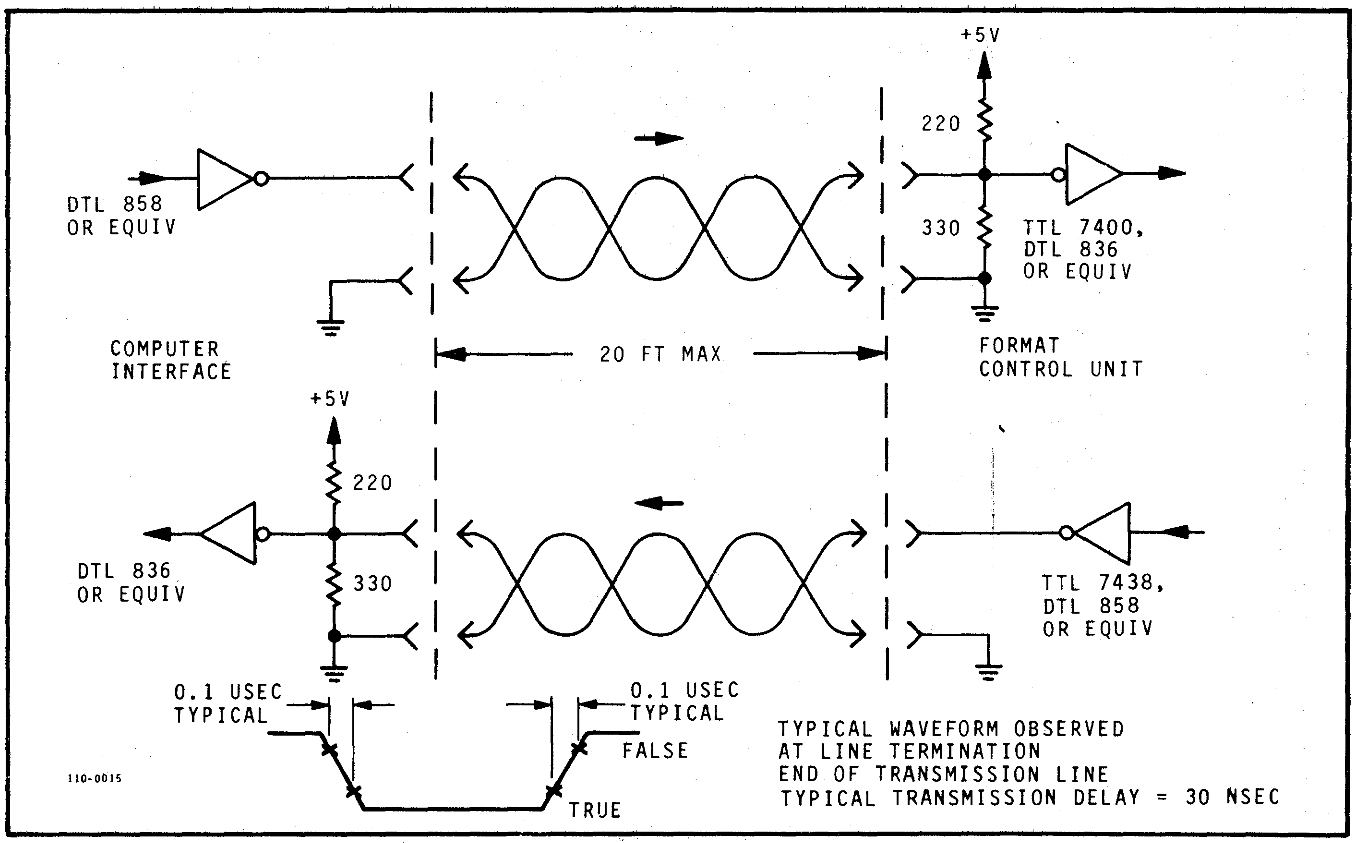


Figure 1-5. Typical Interface Configuration

1.5 INTERFACE CHARACTERISTICS

1.5.1 INTERFACE CONNECTIONS

The interface connector on the Model 9832 is designed for twisted pair inputs and outputs. For each active pin there is a ground pin. The mating interface connector, a 37-pin edge connector, and its mounting hardware are supplied with the tape unit.

1.5.2 INTERFACE SIGNAL CHARACTERISTICS

The Model 9832 tape unit responds to zero true inputs and provides zero true outputs. Each signal input is terminated in such a manner as to provide matching for twisted pair cables (see Figure 1-5). Each output line is driven with an open collector driver. For best results, typical interfacing circuit configuration shown in Figure 1-5 should be used. The recommended twisted pair cable will reduce the magnitude of intercable crosstalk. Unless otherwise specified, all wires should be 24 AWG minimum with a minimum insulation thickness of 0.01 inch. Each pair should have not less than one twist per inch and the input/output cable should not exceed 20 feet in length.

1.5.3 INPUT SIGNAL DESCRIPTION

The input receiver circuits, due to zero true current sinking logic design, will interpret a disconnected wire or removal of power at the transmitter as a logic zero or false condition. The logic 1 or true state requires 25 ma current sink with less than 0.4 volt. The logic zero or false state will be 3 volts due to the input matching resistors (see Figure 1-6). The recommended input pulse width is 2 μsec, and the rise and fall times for pulses and levels must be less than 0.5 μsec.

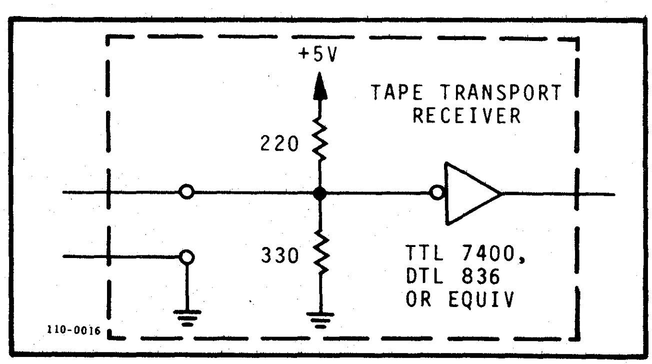


Figure 1-6. Typical Receiver Circuit

1.5.4 OUTPUT SIGNAL DESCRIPTION

Each output line is driven with an open collector current sinking logic driver which is capable of sinking up to 40 ma in the true state. All outputs are disabled (false) when FORMATTER ENABLE input is false.

1.5.5 INTERFACE INPUT SIGNALS — WRITE

FORMATTER ENABLE

FEN	Level	P1-18

Must be true to enable system. When false, most inputs except INITIALIZE are disregarded and all outputs are disabled. This input should normally be wired true, but if it is switched false during a tape pass an initialize pulse should be applied before it is switched true again.

WRITE STATUS SELECT

WSEL	Level	P1-5

Must be true whenever write commands or end of record commands are being applied. It may be but need not be false during rewind.

WSEL must be true when the tape transport is at loadpoint if tape is to be written. A BOT gap is then written automatically and the system will then be ready to write data. Conversely, if WSEL is false when at load point, READ will be selected and two records will be read into the buffer. It follows then that if WSEL is not false after a RWD, the formatter will cause another BOT gap to be written and will be ready to write. If the tape is then unloaded, an unwanted glitch may be recorded on tape which is a problem to some readers. To avoid this WSEL or FEN should be made false after the RWD command has been accepted. WSEL or FEN should then be simultaneously reapplied in the desired condition after the transport is at load point to start a new run.

WRITE DATA INPUTS

WD( )

Nine Track	Seven Track	
WD0	PEVEN	P1-10
WD1		P1-11
WD2	WDB	P1-12
WD3	WDA	P1-13
WD4	WD8	P1-14
WD5	WD4	P1-15
WD6	WD2	P1-16
WD7	WD1	P1-17

Eight lines for nine-track operation; six lines for seven-track operation. These are levels that if true at WDS time will result in a flux transition being recorded on tape (transport is in the write mode). Data inputs must have settled prior to 0.1 μsec after the leading edge of the WDS pulse and must remain quiescent for a minimum of 2 μsec. The data lines may be at any condition at other times.

PEVEN (Seven track only)	Level	P1-10

Selects parity to be written on tape and selects parity to be checked when reading. Even parity is selected if input is true; odd parity is selected if input is false. This is a setup line and must be at its selected level whenever FEN is true, and should not be changed during a tape run.

WRITE DATA STROBE

WDS	Pulse	P1-6

A pulse of 2 μsec minimum width for each character to be written. Writing occurs approximately 0.5 μsec after the leading edge of the WDS. Internal circuitry provides this delay which also discriminates against transients of less than 100 nsec in duration. This internal delay also allows the user equipment to strobe out the data and write data strobe with the same pulse and prevents critical timing when this is done. The write data strobe may be any length greater than 2 μsec, but must go to its false condition for a minimum of 2 μsec between WDS pulses. This command should not be given if BUSY is true or READY is false.

END OF RECORD COMMAND

EORC	Pulse	P1-7

The end of record command is used to signal the termination of the record and to initiate the writing of check characters and gaps. It is a 2 μsec minimum pulse and may be applied any time after the trailing edge of the WDS pulse corresponding to the last character in the record which is being terminated. EORC causes the input lines to be switched to the alternate memory. This transfer time is 20 μsec maximum. Therefore the leading edge of the next WDS pulse must not occur until 20 μsec after the trailing edge of the EORC.

If no EORC is received prior to filling the memory, an internal EORC is generated resulting in n character blocks, where n is the memory size of the unit.

This command should not be given if BUSY is true.

END OF FILE COMMAND

EOFC Pulse P1-8

The EOFC is a pulse of 2 μsec minimum duration. WDS and EORC should be quiescent when it is applied. EOFC causes a gap and end of file character and its check character to be written. If there is data in memory at the time it is applied, an internal EORC is given to write this last record on tape first, and then the EOFC sequence takes place.

This command should not be given if BUSY is true or READY is false. No other commands should be given for a period of 100 ms after EOFC is given.

REWIND COMMAND

REWC Pulse P1-9

The REWC is a pulse of 2 μsec minimum duration. All other commands should be completed when this command is given in the 9832. REWC results in a rewind to load point. See WSEL for further details of the operation.

This command should not be given if BUSY is true.

1.5.6 INTERFACE OUTPUT SIGNALS — WRITE

WRITE READY STATUS

WRDY Level P1-1

A level that is true when ON LINE is true, a write enable ring is mounted on the supply hub, and the transport is on tape. (That is, when the initial load sequence is complete.)

Level is false during rewind.

LOAD POINT

LDP Level P1-2

A level that is true when the load point marker is under the photosensor and the transport is not rewinding. (Circuitry using this output should not use the edges as triggers.)

END OF TAPE

EOT Level P1-3

A level that is true when the end of tape marker is under the photosensor. (Circuitry using this output should not use the edges as triggers.)

MEMORY BUSY

BUSY Level P1-4

This level will go true whenever a memory is filled and the alternate memory is not available because enough time was not available to dump the contents onto tape. It will remain false as long as the data rates do not exceed the rates shown in Figures 1-1 and 1-2. It may go true at lesser rates only if the tape error correction option is used, when an error and its rewrite sequence occur. The timing of the BUSY signal is arranged so that it will go true within 1 μsec of the leading edge of the EORC (or internal EORC) which called for transfer to a full memory. This is early enough to use this line to inhibit the next WDS.

The BUSY line is also true during LOAD POINT DELAY, REWIND, and during the EOF sequence. BUSY should be used in the customer equipment to inhibit all commands, since they will not be accepted when BUSY is true. After the LOAD POINT BUSY sequence, 100 ms must elapse before an EOR pulse is applied. Signals on this line during read operations should be ignored.

TAPE ERROR

TER Level P1-19

This signal goes true whenever an error is detected while writing on tape. It is not synchronized with input signals, but indicates an internal operation and error which will be corrected. It is useful to indicate the quality of the tape being used. One level occurs for each record in error.

1.5.7 INTERNAL FEATURES — WRITE

The read after write check option provides automatic rewrite of a block of data if vertical or longitudinal parity shows an error during the read mode. The sequence is as follows:

a. Record is written on tape.
b. A read head is 0.15" (0.30" for seven-track) downstream, reads the data, and checks for vertical and horizontal parity.
c. If no error is found the normal sequence is not interrupted.
d. If an error is found, the tape is stopped and run in reverse to the beginning of the record in error.
e. The tape is run forward in the erase mode for a distance slightly greater than the record length.
f. The record is written again from memory. If read successfully normal operation continues.

g. The sequence is repeated until it is successfully written.
h. Depending on data rates, this sequence can cause a BUSY signal.

1.5.8 INTERFACE INPUT SIGNALS — READ

READ OUT ONE CHARACTER

ROOC Pulse P2-6

When true, directs buffer to read out a character. (Not recognized if RDA is false.)

HOLD

HOLD Level P2-2

When true, prevents refill of buffer from tape to allow additional readouts of blocks in memory. This level is particularly useful in data communication applications. This level may be applied any time after the EOR output of the previous block but before the EOR output for the block being read out.

STOP SEARCH

STOP Pulse P2-3

When true, stops read search after completion of read-in of record from tape. Data in memory may still be read out until empty. (RDA false.)

Note automatic STOP SEARCH is provided by formatter under any of the following conditions:

a. In read if 25 feet of blank tape passes head and no data is found.

b. In read if the last record read into memory was a file mark and the EOT marker is passed.

c. In read if the EOT marker is passed and a file mark is detected.

INITIALIZE

INIT Pulse P2-4

Initializes system. Not required under normal operation, since internal presets are provided. May be used to clear an automatic stop search if it is desired to search a tape with gaps greater than 25 feet, or to search for data after an EOT. (Tape may then run off end.) May also be used to clear an external stop search.

Initialize is not conditioned by DEVICE ENABLE or WRITE SELECT.

1.5.9 INTERFACE OUTPUT SIGNALS — READ

READ DATA AVAILABLE

RDA Level P2-1

When true, indicates that a block of data has been transferred from tape and is ready to be read out.

READ DATA OUTPUTS

RD( ) Level

Nine Track	Seven Track	
RD0		P2-10
RD1		P2-11
RD2	RDB	P2-12
RD3	RDA	P2-13
RD4	RD8	P2-14
RD5	RD4	P2-15
RD6	RD2	P2-16
RD7	RD1	P2-17

True when data is 1. Must be used in conjunction with READ DATA STROBE.

READ DATA STROBE

RDS Pulse P2-9

Occurs 100 nsec after ROOC. Read data changes to a new character 200 nsec following the trailing edge of RDS.

READ END OF RECORD

REOR Pulse P2-7

When true, indicates that previous character was last character of its block. Occurs less than 1 microsecond after READ DATA STROBE.

READ END OF FILE

REOF Level P2-8

Indicates that the record available is a file mark. The record must be read out in the normal manner (ROOC) to proceed to the next record. The data read will be the file mark character. This level brackets the RDS for the record and may be used to inhibit RDS in the external system.

READ BLOCK IN ERROR

RBIE Level P2-18

When true, indicates that a permanent read error occurred within the block that is being read out. Readout may be done normally. This level is used to determine how block is handled in user equipment. The error indication occurs as soon as the block is in the buffer and terminates when the last character of the block is read out. A permanent read error is defined as a block that had a VRC or LRC error, and which could not be read after two retries. (An option is available to increase the number of retries to 7 or 15.)

1.5.10 INTERNAL FEATURES — READ

The buffered memory formatter has been designed to provide a new order of simplicity in interface. The function of rereading if an error is detected is built in, and the sequence is as follows:

a. One of the two buffers is available by completing readout of that buffer.

b. A readout from tape to buffer takes place. If no error is detected, data available is held true and readout to interface is available.

c. If error is detected, the tape backspaces one block and rereads until an error-free block is in memory or until two passes have been made.

d. If the block cannot be read in two passes, an error register is set.

e. When the memory section with the unrecoverable error is available to the interface, the error register is gated to the READ BLOCK IN ERROR output.

f. The data may be read out normally for reconstruction or may be read out and discarded by using the READ BLOCK IN ERROR line to control the discard.

Another built-in feature is the HOLD function. By making this line true a block of data in memory may be read out and retained to be read out again. This is useful in data communication transmission where an answer back line is used to acknowledge satisfactory receipt of a block. The block may be reread as often as desired. When the hold is cleared, the data from the next block is immediately available.

1.5.11 OPTIONS

MEMORY ERROR

MEMER	Pulse	P2-19

This signal is provided to allow a parity check on the memory. Parity is generated at the input of the memory and checked at the output. The signal is random in length and usually indicates a component failure.

ABORT

ABORT	Pulse	P2-5

This signal is used in the write mode to abort a partial record which has been placed into memory and prevents its transfer to tape. The pulse may occur at any time before an EOR pulse is applied. It will abort the data after the previous EOR pulse.

When this option is ordered the automatic EORC, which normally occurs when the memory is full, is disabled, and it becomes the user's responsibility to limit the number of characters to be less than the maximum block length. Also the internal EOFC, which normally occurs if no EORC is received immediately before the EOFC, is disabled.

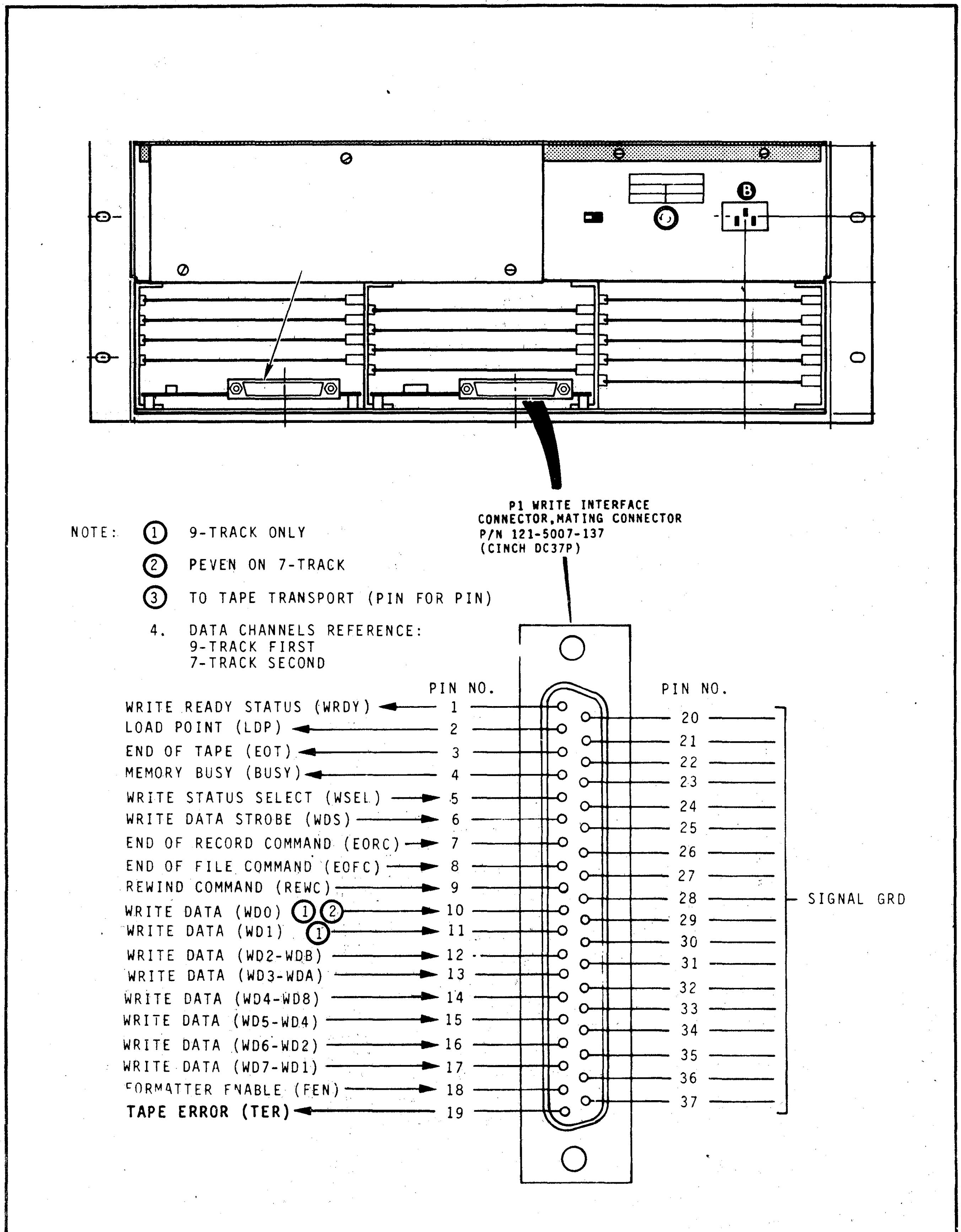


Figure 1-7. Model 9832 P1 Pin Interface Connector and Pin List

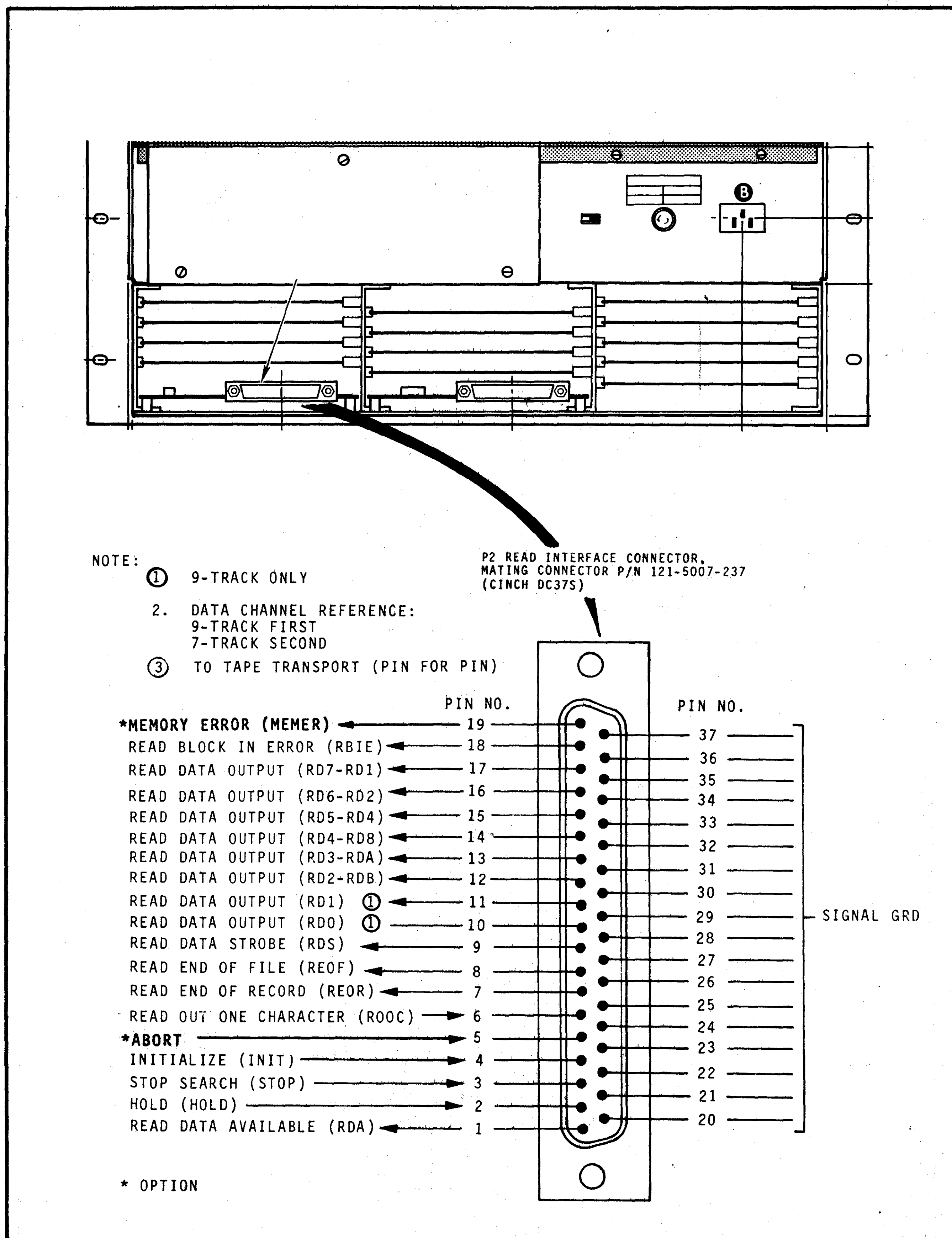


Figure 1-8. Model 9832 P2 Interface Connector and Pin List

SECTION III

THEORY OF OPERATION

SECTION III
THEORY OF OPERATION

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

This section describes the theory of operation of the formatter on a functional basis. Since the unit is of modular design using easily replaceable circuit cards, the detailed circuit descriptions are placed with their respective schematics in Section VI.

3.2 WRITE CIRCUITS

3.2.1 INTRODUCTION

The following paragraphs describe the write circuitry used in reading data into the memories, its readout, and the formatting electronics, including the end-of-file and error detection circuits. The following modules are involved in performing these functions:

Memory Input Control Type 3516
Memory Counter Type 3607
Memory Type 3638/3938
Tape Timing Control Type 3633
Tape Motion Control Type 3616
CRC Control Type 3578
CRC Register Type 3639
Time Pulse Generator Type 3640

A block diagram of the write memory and formatting circuits is included as Figure 3-1. A timing diagram, Figure 3-2, provides an overall view of the timing functions involved in the memory control.

3.2.2 WRITE TIMING CIRCUITS

To better understand the operation of the formatter, it is essential to distinguish between the various clocks used in the read-in and read-out cycles. Each clock is discussed individually here and should be referred to when studying the various functions performed by the formatter.

3.2.2.1 WRITE STEP and WRITE COMMAND $\overline{\text{WCMD1}}$

WRITE STEP is the asynchronous input interface clock used to strobe the data into the buffer. WRITE STEP may be of any duration greater than the minimum of 2 μsec. It is supplied to Time Pulse Generator Type 3640, where a one-shot network generates the actual read-in clock WRITE COMMAND $\overline{\text{WCMD1}}$. $\overline{\text{WCMD1}}$ is 1 μsec in duration regardless of the duration of the WRITE STEP, and is delayed approximately 0.5 μsec after the leading edge of WRITE STEP. $\overline{\text{WCMD1}}$ becomes the memory clock XCLK during the read-in segment of the data cycle as described in section 3.2.4. It is used to clock the data into the memory and advance the memory counter.

3.2.2.2 Master Oscillator and Readout Time Pulses

While the read-in clock $\overline{\text{WCMD1}}$ is asynchronous, allowing the data to be supplied to the recorder at any rate below the maximum specified in Section I of the manual, the readout functions are synchronous, since the data is written on tape at a preselected density: 200, 556, or 800 cpi. The synchronous clocks are generated by a crystal-controlled master oscillator located on Time Pulse Generator Type 3640. The crystal frequency is a function of the tape speed, as tabulated on the schematic for that module. For speeds lower than 20 ips a flip-flop is used to divide the crystal frequency by two. The crystal frequency is supplied to a dividing network used to produce the four available data frequencies: MO200, MO556, MO800, and MO1600. The readout time pulses, ROTP1 through ROTP4, are derived from these data synchronized crystal controlled frequencies. The clock frequency for which the machine is selected, for example MO800 for 800 cpi, is supplied to Tape Motion Control 3616 as READOUT OSCILLATOR ROOSC. The tape motion control module includes a series of four consecutive one-shots that generate READOUT TIME PULSES ROTP1 through 4. These are consecutive 1 μsec pulses separated by a short delay; thus the leading edge of ROTP2 is delayed slightly after the trailing edge of ROTP1, and ROTP3's leading edge is slightly delayed after the trailing edge of ROTP2, and so on. The readout time pulses are used during the synchronous readout functions in which the data is read from the memories onto the tape. ROTP3 is used as READOUT CLOCK ROCLK, clocking the data from the memories to the CRC register. ROTP2 becomes WRITE CLOCK WCLK used to toggle the CRC register flip-flops and the write buffer flip-flops. In addition, the readout time pulses are used to synchronize the error detection functions, the check character generation, and others during the readout operation.

The master oscillator frequency divided by two is supplied as the PUMP CLOCK PUCLK. This clock is supplied to Memory Counter Type 3607 to be used as the memory clock XCLK following the WRITE

COMMAND $\overline{WCMD1}$ and before READOUT CLOCK ROCLK2. It is used to "pump" the data to the output of the buffer before it is read out by the readout clock.

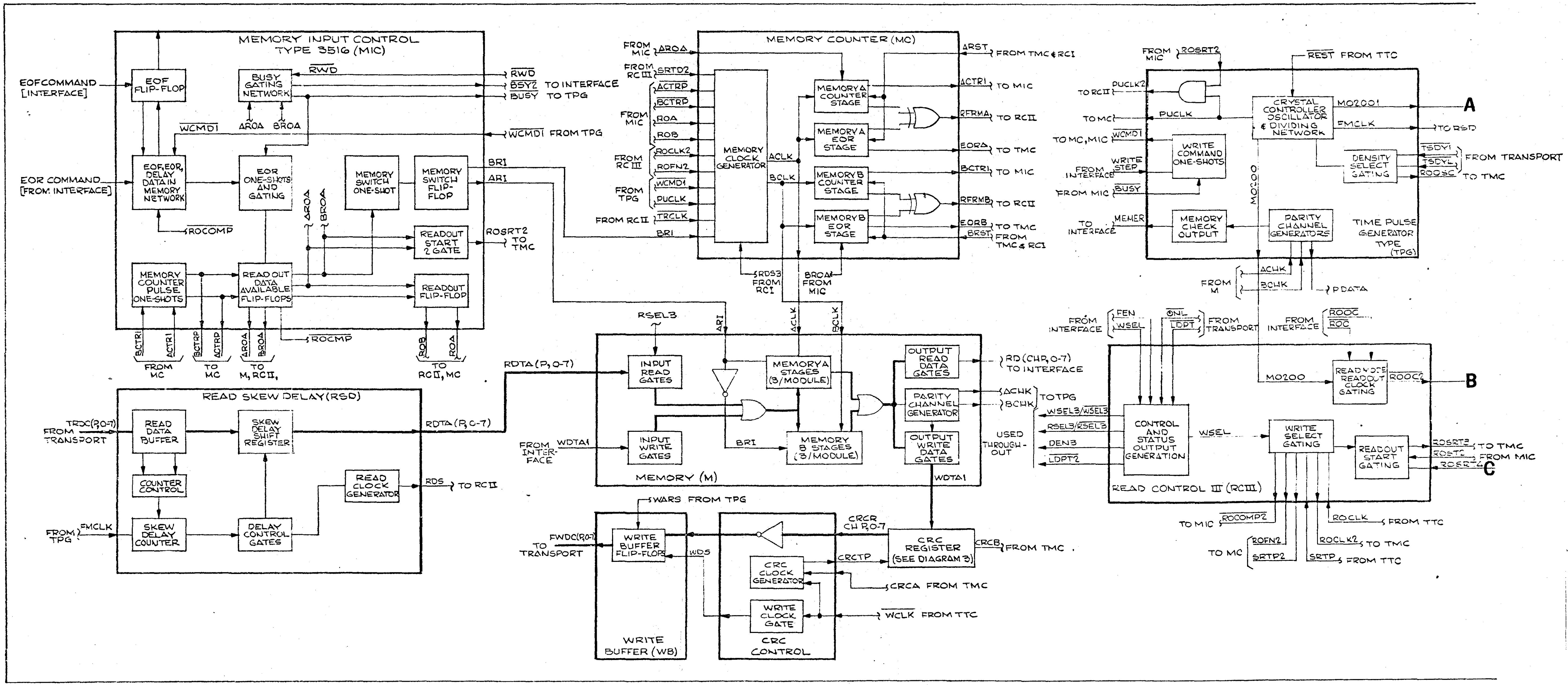
In addition to being used as the readout frequency for 200 cpi recorders, MO200 is also gated with $\overline{REST}$, the static state of the program control counter (see section 3.2.5). $\overline{REST}$ is high (false) whenever the tape is moving, gating MO200 through as MO2001. MO2001 is supplied to Tape Timing Control Type 3633, where it is used to advance the delay counter. MO2001 effectively divides each inch of tape into 200 segments, regardless of the readout data frequency, and is used to time the start, stop, erase, file mark and BOT delays, as well as the blank tape detector in the read section.

3.2.3 MEMORY READ-IN AND READOUT CONTROL

The principal functions of the read-in and readout control are performed by the Memory Input Control Type 3516 module. When the recorder is initially turned on, formatter preset pulse $\overline{FREST}$ clears the two readout available flip-flops, setting the two readout available levels AROA and BROA false, indicating that there is no data available for readout. Since initially neither memory — A or B — contains any data, both are available for read-in, and it is irrelevant which memory receives data first; hence the read-in flip-flop, which controls which memory is to receive data, is in an indeterminate state, with either B READ IN BRI or A READ IN ARI true. ARI is supplied to the Memory Type 3638/3938 module. If ARI is high it enables a set of gates that supplies interface data DTA1 0 through 7 to memory A. ARI false would enable a second set of gates which supplies the data to memory B. Once the whole block of data has been received by the memory, the interface issues an EOR command that switches the next incoming block to the empty memory; in addition, the EOR command initiates the readout sequence, in which the data from the filled memory is written on tape. If no EOR command is received, the memory receiving data will be filled to its capacity, which varies according to the buffer size from 512 to 2048 characters. Once the memory is filled, the memory counter associated with that memory, located on Memory Counter Type 3607, issues COUNTER PULSE XCTR (X standing for either memory A or B) which is substituted for the EOR command to initiate the memory switch and the readout sequence ending the block. The execution of an EOR sequence is delayed by a pair of one-shots in series, the first of which delays the EOR execution by approximately 6.6 μsec to allow the EOR command to be given simultaneously with the last character of the block. The second one-shot supplies a 1.5 μsec pulse that initiates the readout and fires yet a third one-shot. The third one-shot is the memory switch one-shot which supplies a 5 μsec pulse, whose trailing edge toggles the memory read-in flip-flop. Hence there is a delay of approximately 13 μsec between an EOR command and the actual completion of the memory read-in switch. It is recommended, however, that the next data block be delayed at least 15 μsec following an EOR command.

As described above, the second of the two EOR one-shots initiates the readout sequence. This occurs as follows: The pulse generated by the EOR one-shot (or alternately, if an EOR is not given, the memory pulse XCTR1) sets the readout available flip-flop of the memory that was last reading in. Either AROA or BROA then goes true, which in turn causes READ OUT START 2 ROSRT2 to go true. ROSRT2 is supplied to Tape Motion Control Type 3616 where it generates a PROGRAM ADVANCE PADV to advance the program control counter on Tape Timing Control Type 3633 from stage $\overline{Q}_0$ to $\overline{Q}_1$ (see section 3.2.5). This initiates the start delay, allowing the tape to ramp up and start the readout of the memory onto the tape. When the memory has completed its readout and the tape has come to a stop, a READ OUT COMPLETE pulse $\overline{ROCOMP}$ is supplied from the tape timing control module and clears the readout available flip-flop of the memory that was reading out, terminating the readout sequence.

The read-in and readout sequences described above apply during normal conditions when the input data rate does not exceed the limits specified in Section I of this manual. However, when the data input rate from the interface exceeds the allowable rate, or when an error is detected in read-after-write models, a different condition exists. In that case both AROA and BROA go true, indicating that both memory A and B have data available for readout. This causes a $\overline{BUSY}$ signal to be generated by the memory input control module which disables the EOR one-shots, inhibiting any memory read-in switch in response to an EOR command. The memory switch is delayed until $\overline{BUSY}$ goes false when one of the memories has completed its readout and is available for read-in. $\overline{BUSY}$ is also supplied to the Memory Select and Interface Type 3515 where it inhibits any WRITE COMMANDS $\overline{WCMD1}$, thus inhibiting any data from being read into the memories. $\overline{BUSY}$ from the memory input control module is also wire-OR'd with $\overline{BUSY}$ from the tape timing control module, which holds $\overline{BUSY}$ true when load point is detected or when an EOR command is given until either the load sequence or the end of file sequence is completed. $\overline{BUSY}$ is supplied to the interface as $\overline{BSY2}$ where it can be used to inhibit any incoming data and commands.


MEMORY INPUT CONTROL TYPE 3516 (MIC)
EOF COMMAND [INTERFACE]
EOF FLIP-FLOP
BUSY GATING NETWORK
RWD
RWD
BSY2 TO INTERFACE
BUSY TO TPG
AROA
BROA
WCMD1
WCMD1 FROM TPG
EOR COMMAND [FROM INTERFACE]
EOF, EOR, DELAY DATA IN MEMORY NETWORK
EOR ONE-SHOTS AND GATING
MEMORY SWITCH ONE-SHOT
MEMORY SWITCH FLIP-FLOP
BR1
AR1
ROCOMP
READOUT START 2 GATE
ROSRT2 TO TMC
MEMORY COUNTER PULSE ONE-SHOTS
READ OUT DATA AVAILABLE FLIP-FLOPS
READOUT FLIP-FLOP
ROCMP
BCTR1
ACTR1
BCTRP
ACTRP
AROA
BROA
ROB
ROA
FROM MC
TO MC
TO M, RC II,
TO RC II, MC
MEMORY COUNTER (MC)
FROM MIC
FROM RC III
FROM MIC
FROM RC III
FROM TPG
FROM RC II
ARST FROM TMC & RC1
SRTD2
ACTRP
BCTRP
ROA
ROB
ROCLK2
ROFN2
WCMD1
PUCLK
TRCLK
BR1
MEMORY CLOCK GENERATOR
ACLK
BCLK
MEMORY A COUNTER STAGE
MEMORY A EOR STAGE
MEMORY B COUNTER STAGE
MEMORY B EOR STAGE
ACTR1 TO MIC
RFRMA TO RC II
EORA TO TMC
BCTR1 TO MIC
RFRMB TO RC II
EORB TO TMC
BRST FROM TMC & RC1
RDS3 FROM RC1
BROA FROM MIC
FROM MIC ROSRT2
REST FROM TTC
PUCLK2 TO RC II
TO MC
PUCLK
TO MC, MIC WCMD1
CRYSTAL CONTROLLER OSCILLATOR & DIVIDING NETWORK
MO2001
A
FMCLK TO RSD
FROM INTERFACE WRITE STEP
WRITE COMMAND ONE-SHOTS
DENSITY SELECT GATING
TSDY1
TSDYL
FROM TRANSPORT
ROOSC TO TMC
FROM MIC BUSY
TO INTERFACE MEMER
MEMORY CHECK OUTPUT
MO200
PARITY CHANNEL GENERATORS
TIME PULSE GENERATOR TYPE (TPG)
FROM M
ACHK
BCHK
P DATA
RSEL3
AR1
ACLK
BCLK
INPUT READ GATES
MEMORY A STAGES (3/MODULE)
OUTPUT READ DATA GATES
RD (CHP, 0-7) TO INTERFACE
RDTA (P, 0-7)
PARITY CHANNEL GENERATOR
ACHK
BCHK
TO TPG
FROM INTERFACE WDTA1
INPUT WRITE GATES
BR1
MEMORY B STAGES (3/MODULE)
OUTPUT WRITE DATA GATES
MEMORY (M)
WDTA1
USED THROUGH-OUT
READ SKEW DELAY (RSD)
TRDC(P, 0-7) FROM TRANSPORT
READ DATA BUFFER
SKEW DELAY SHIFT REGISTER
RDTA (P, 0-7)
COUNTER CONTROL
READ CLOCK GENERATOR
RDS TO RC II
FROM TPG FMCLK
SKEW DELAY COUNTER
DELAY CONTROL GATES
WARS FROM TPG
FWDC(P, 0-7) TO TRANSPORT
WRITE BUFFER FLIP-FLOPS
WDS
CRCR CH P, 0-7
CRC REGISTER (SEE DIAGRAM 3)
CRCB FROM TMC
CRCTP
CRC CLOCK GENERATOR
CRCA FROM TMC
WRITE CLOCK GATE
WCLK FROM TTC
WRITE BUFFER (WB)
CRC CONTROL
FROM INTERFACE
FEN
WSEL
ONL
LDPT
FROM TRANSPORT
FROM INTERFACE
ROOC
ROC
MO200
READ MODE READOUT CLOCK GATING
ROOC2
B
WSEL3/WSEL3
RSEL3/RSEL3
DEN3
LDPT2
CONTROL AND STATUS OUTPUT GENERATION
WSEL
WRITE SELECT GATING
READOUT START GATING
ROSRT2 TO TMC
ROSTC
ROSRT FROM MIC
C
READ CONTROL III (RC III)
TO MIC ROCOMP2
ROCLK FROM TTC
TO MC ROFN2
ROCLK2 TO TMC
SRTP2
SRTP FROM TTC

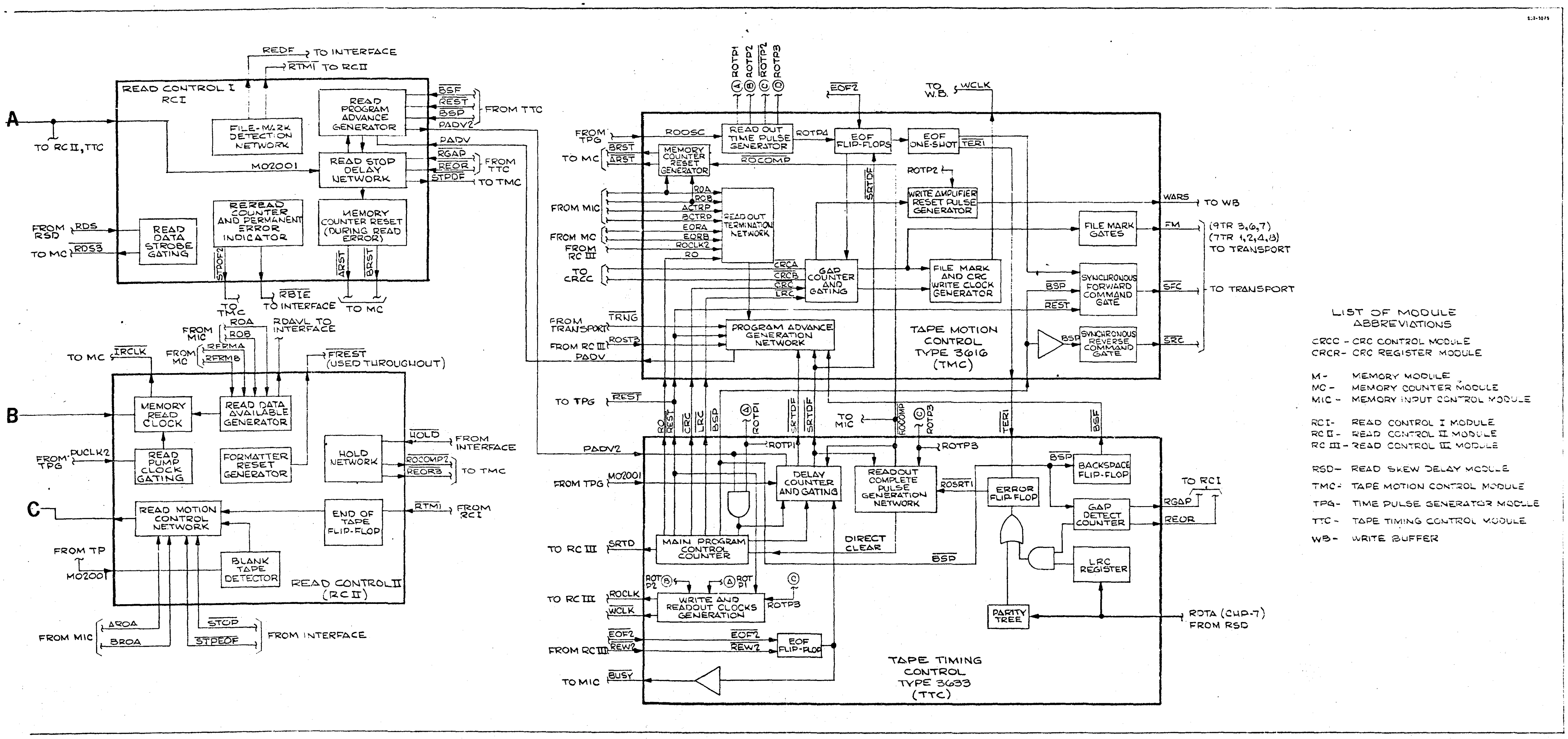


Figure 3-1. System Block Diagram

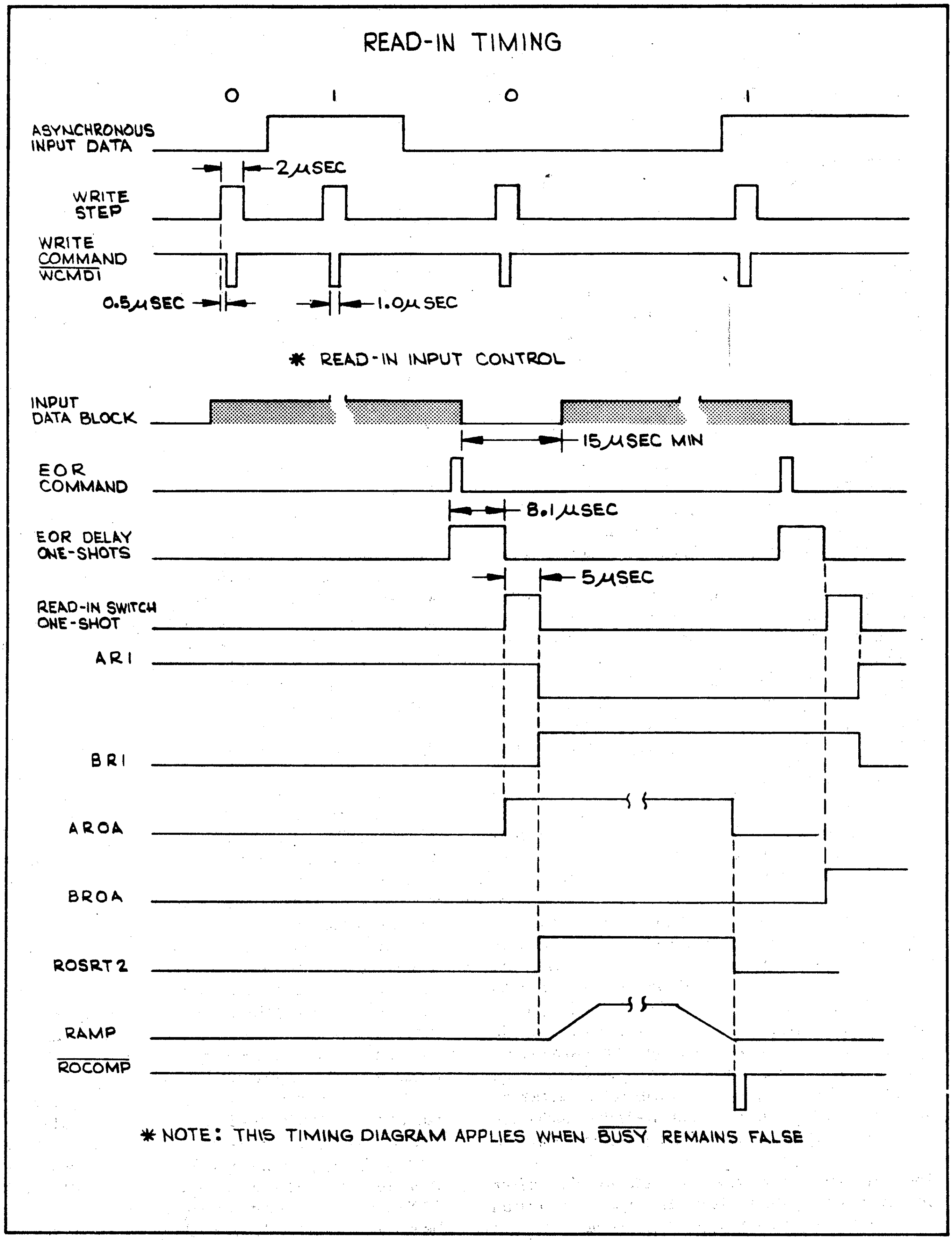


Figure 3-2. Timing Diagram

3.2.4 DATA FLOW AND BUFFER OPERATION

The dual buffer formatter contains two separate memories, A and B. Each memory varies in size from 512 to 2048 character capacity. The buffer stages are divided among three memory modules, each module containing three channels for each buffer. Thus one module contains channels 5, 6, and 7 for buffers A and B, another contains channels 3, 4, and 5, and the third contains channels 0, 1, and optionally (when the memory check option is used) channel P. The write data channels are supplied from the interface as DTA1 0 through 7 (for nine-track recorders) to the memory module. The memory module contains two sets of input gates, one receiving the write data and the other the read data. During the write operation the write input gates are enabled, routing the data to the memory input gates. Only half the memory input gates are enabled, gating the data to the memory stages of either buffer A or B.

A MEMORY READ IN (ARI) generated on the memory input control module controls which buffer receives the data. If ARI is true (high) the write data would be gated to the buffer A memory stages; ARI false would gate the data to the buffer B memory stages.

The read data channels, RDTA P, and 0 through 7 (supplied from the deskew/gap delay module), are similarly routed to the input of one of the memory stages, as determined by the status of ARI. The data channels, both the read and write, are then shifted through the memory stages by the respective memory clock, either ACLK or BCLK (henceforth referred to as XCLK). Each memory stage consists of a number of memory chips which varies according to the buffer size. Each memory chip is basically a shift register, usually with a 256 bit capacity (other chips may be used). The memory clock pulses shift the data down the register to the output, and then strobes it out to the transport if it is write data, or to the interface if it is read data. Each buffer has two counters associated with it to keep track of the data read into it. These counters, the memory stage counter and the EOR stage counter, are situated on the Memory Counter Type 3607 module and are also toggled by the memory clock XCLK. Each counter consists of several divide-by-sixteen counters in series, and each has twice the memory stage capacity. The memory clock XCLK combines three distinct clocks for the write mode and three other clocks for the read mode. The read and the write clocks are basically similar clocks with the order reversed.

The following paragraphs will describe the buffer operation during the write mode only. (See section 3.3.2 for a description of the read memory clock.)

During a write operation the asynchronous clock WRITE COMMAND $\overline{\text{WCMD1}}$, derived from the WRITE STEP on the time pulse generator module, is first supplied as XCLK to strobe the input write data from the interface into the memory. At this time only the memory counter is enabled while the EOR counter is disabled by READ OUT AVAILABLE XROA false.

When a complete record is fed into the memory and an EOR command is given by the interface, the $\overline{\text{WCMD1}}$ are terminated. At this time the memory input control module indicates that there is data available for readout, XROA going true. The memory input control module then issues a READ OUT START ROSRT2 level to the tape timing control module, moving the program control counter on that module from the REST state ($\overline{Q_0}$) to the start delay state ($\overline{Q_1}$), supplying START DELAY SRTD true. SRTD is returned to the memory counter module, where the memory clocks are generated, setting a flip-flop which enables the PUMP CLOCK PUCLK to become the memory clock XCLK. PUCLK (see section 3.2.2) is a square wave at half the master oscillator frequency used to advance the data along the memory to its output. Note that when the PUCLK is supplied as the memory clock the EOR counter is enabled as well by XROA true; thus both counters as well as the memory are toggled by XCLK at this time. Assuming that the memory size is N_m and that the record length read into the memory is N_r, then the number of PUCLK supplied to the memory is $N_p = N_m - N_r$, or the difference between the record length and the memory size. Once the pump clock has advanced the data to the output stage of the memory, the memory counter has counted to the memory capacity, since it has counted the N_r $\overline{\text{WCMD1}}$ pulses plus the N_p PUCLK pulses, equaling $N_r + N_p = N_m$. The memory counter then generates COUNTER PULSE XTR1. XTR1 is supplied to the memory counter card where it clears a flip-flop that inhibits PUCLK while enabling READ OUT CLOCK ROCLK to become memory clock XCLK. ROCLK is generated on the tape timing control module by gating data synchronized READ OUT TIME PULSE ROTP3 (see section 3.2.2) with READ OUT RO. RO is true during the readout stage of the program control counter; hence ROCLK is supplied exclusively during readout. ROCLK strobes the data from the memory output to the tape via the path described below. ROCLK also advances both counters until the whole block has been read out. Following N_r ROCLK pulses, when the block is completely read out, the EOR counter has counted to the memory capacity, since it has already counted the N_m pump pulses ($N_r + N_p = N_m$). At this time the EOR counter issues END OF RECORD (EORX) pulse, indicating that the whole record has been read out. EORX is supplied to the tape motion control module where it generates a PROGRAM ADVANCE PADV pulse which advances the program control counter on the tape timing control module from Q_2, the readout state, to Q_3, the CRC state (for nine-track recorders). Following the writing of the CRC and LRC check characters the tape comes to a stop and the readout is complete.

As the data is read out from the memory as WDTA1, it is supplied to the CRC register module to generate the CRC character, consequently to the CRC control module which in turn supplies it to the write buffer module. The write buffer contains a set of flip-flops which are toggled by the WRITE DATA STROBE $\overline{\text{WDS}}$, supplying the data to the tape transport. The output data of the memories is also recycled back to the input of the memory stages. As ROCLK is strobing the data out, it is simultaneously strobing it back to the memory from which it was read out, and it keeps advancing the memory counter. Thus when the data block is completely read out, it is stored again in the memory. If the block on tape is good and no read-after-write errors are detected, the tape timing control module generates READOUT COMPLETE PULSE $\overline{\text{ROCOMP}}$ which in turn causes the COUNTER RESET PULSE $\overline{\text{XRST}}$ to be generated on the tape motion control module. $\overline{\text{XRST}}$ resets the memory counter of the memory which has just completed its readout, in effect erasing the data from that memory and making it available for the next block. Should the record written on tape be erroneous, $\overline{\text{ROCOMP}}$ is inhibited, and the memory counter is not reset, retaining the data in the memory. The program control counter on the tape timing module then proceeds to state $\overline{Q_6}$, starting an error sequence in which the transport backspaces, erases the erroneous block, and rewrites it until it is written correctly (see section 3.2.5).

The above description applies in the case where the record written into the memory is shorter than the memory's capacity. If no EOR is given by the interface before the memory is filled, a slightly different sequence occurs. The memory counter issues a counter pulse XCTR1 when the memory is filled; XCTR1 is then supplied to the memory input control module and is substituted for an EOR command. It sets the READ OUT AVAILABLE flip-flop, setting XROA high, and it also switches the memory clock XCLK on the memory readout control module from $\overline{\text{WCMD1}}$ to the PUMP CLOCK PUCLK. The rest of the memory cycle is as described above.

3.2.5 TAPE FORMATTING CONTROL

3.2.5.1 Introduction

The tape motion and data formatting control functions are performed by Tape Timing Control Type 3633 and Tape Motion Control Type 3616. The principal components used in performing these functions are the program control counter, the delay counter, and the gap counter.

3.2.5.2 Program Control Counter

The program control counter is located on the tape timing control module. It consists of a divide-by-sixteen counter and a binary to octal decoder. There are eight program states, $\overline{Q_0}$ through $\overline{Q_7}$, whose functions are tabulated below.

	Output of Program Counter	Function Performed	
	Q_0	REST	Tape is stationary
	Q_1	SRTD	Start delay, tape ramps up to speed
	Q_2	RO	Read out, one of the memories is read onto tape
	Q_3	CRC	The CRC character is written on tape
	Q_4	LRC	The LRC character is written on tape
	Q_5	STOP DELAY	The stop delay gate is enabled if no error is detected
only during error sequence	Q_6	BSP	Tape backspaces over erroneous block
	Q_7	ERASE DELAY	Erase delay gate is enabled, erroneous block is erased

The actual motion command, SYNCHRONOUS FORWARD ($\overline{SFC}$) and SYNCHRONOUS REVERSE ($\overline{SRC}$) are generated by a pair of NAND gates on the tape motion control module. The SFC gate is enabled by DEVICE ENABLE 3 (DEN3) true. It is activated by $\overline{REST}$ and $\overline{BSP}$ false; e.g., whenever the program control counter is not in the $\overline{REST}$ or backspace states $\overline{SFC}$ goes true, and the tape moves forward. When backspace $\overline{BSP}$ goes true during an error sequence, $\overline{SFC}$ is inhibited while the backspace gate is activated, generating $\overline{SRC}$ true.

To advance the program control counter from one state to the next during the write mode, PROGRAM ADVANCE PADV is supplied from the tape motion control module. PADV is combined with certain "jump" commands used during the read mode (see section 3.3.3.1) and is then supplied as PADV2 to the tape timing control module. PADV2 gates READOUT TIME PULSE ROTP1 (see section 3.2.2) to the clock input of the program control counter. Initially the program counter is in the $\overline{REST}$ state, with no tape motion. When one of the memories is filled and has data available for readout, the memory input control module supplies READ OUT START ROSRT2 true. ROSRT2 is gated through read control III module where it is used during the read cycle (see section 3.3.3.1); it is then supplied as ROSRT3 to the tape motion control module. ROSRT3 is gated with $\overline{REST}$ and $\overline{TRNG}$ to supply PADV true. This moves the counter from $\overline{Q_0}$ to $\overline{Q_1}$. $\overline{Q_1}$ true is inverted and output as START DELAY SRTD true. SRTD true also enables the START DELAY gate, which is activated by the delay counter following the start delay (during which the tape ramps up to speed), generating $\overline{SRTDF}$ true to the tape motion control module. SRTD true initiates the actual tape ramp-up, setting $\overline{SFC}$ true, while $\overline{SRTDF}$, which comes at the end of the start delay, is used to generate the next PADV to advance the program from $\overline{Q_1}$ to $\overline{Q_2}$, the readout state. The program remains in the readout state until one of the memories is read out completely onto the tape. During the readout mode RO true gates ROTP1 to set a flip-flop whose output enables both WRITE CLOCK $\overline{WCLK}$ and READ OUT CLOCK $\overline{ROCLK}$. $\overline{WCLK}$ is generated by gating ROTP2 (see section 3.2.3) with DEVICE ENABLE DEN2. It is routed through the CRC control module to the CRC register where it is used to toggle the CRC register flip-flops; it is also supplied to the write buffer module as WRITE DATA STROBE $\overline{WDS}$ to toggle the write buffer flip-flops, supplying the data to the transport. $\overline{ROCLK}$ is generated by gating ROTP3 with the output of the RO flip-flop, and is supplied to the memory counter module to become the memory clock XCLK. ROCLK is thus slightly delayed after $\overline{WCLK}$ (since ROTP3 is delayed after ROTP2), the reason being that first the character at the output of the memory should be written onto tape before the next character is supplied to the memory's output. Once the whole block has been read, the EOR counter on the memory counter module (see section 3.2.4) issues an EORX pulse to the tape motion control module. EORX is gated with READ OUT ROX from the memory input control module, and is used to set a flip-flop whose output generates the next PADV. PADV true is returned to the tape timing control module to advance the program control counter from $\overline{Q_2}$ to $\overline{Q_3}$, the CRC state (for nine-track recorders). $\overline{CRC}$ true is supplied to the tape motion control module to initiate the writing of the CRC character (see section 3.2.6). When the CRC clock is generated it also issues the next PADV, advancing the program control counter from $\overline{Q_3}$ to $\overline{Q_4}$, the LRC state. When the LRC character is written on tape (see section 3.2.7) another PADV is generated which moves the program control counter from $\overline{Q_4}$ to $\overline{Q_5}$, the stop delay state. $\overline{Q_5}$ true enables the stop delay gate, which is activated following the stop delay, generating $\overline{STPDF}$ true to initiate the rampdown. $\overline{STPDF}$ is also gated with $\overline{ROSRTI}$, the output of the error flip-flop, which goes true when an error is detected. If no error is detected $\overline{ROSRTI}$ stays high and enables $\overline{STPDF}$ to be gated through to set the readout-complete flip-flop. When the flip-flop is set its 0 output goes low and direct-clears the program control counter, returning it to the $\overline{REST}$ state, $\overline{Q_0}$, and completing the readout cycle. The 1 output of the readout flip-flop generates READ OUT COMPLETE pulse $\overline{ROCOMP}$. $\overline{ROCOMP}$ signifies that the data is written on tape correctly; it is supplied to the tape motion control module to generate COUNTER RESET $\overline{XRST}$, used to reset the counter of the memory that was reading out. $\overline{ROCOMP}$ is also supplied to the memory input control module where it clears the data available flip-flop, indicating that the memory is available to receive the next data block.

A different condition exists when an error is detected by the error detection circuits on the tape timing control module. In that case either a VRC error or an LRC error (see section 3.2.7) sets the error flip-flop also situated on the tape timing control module. This sets $\overline{ROSRTI}$ true (low), preventing the readout-complete flip-flop from being set at the end of the stop delay. Consequently $\overline{ROCOMP}$ is not generated and the program control counter is not reset. Instead, $\overline{STPDF}$ is supplied to the tape motion control module where it generates an additional PADV, advancing the program control counter on the tape timing control module from $\overline{Q_5}$ to $\overline{Q_6}$, the backspace state. The program control counter then outputs $\overline{BSP}$ true to the tape motion control module, which in turn generates SYNCHRONOUS REVERSE COMMAND

$\overline{\text{SRC}}$, causing the transport to backspace. On the tape timing control module $\overline{\text{BSP}}$ true is inverted and enables the set input of the backspace flip-flop. The transport continues to backspace until the gap-detect counter (described below) detects the gap preceding the erroneous record; the tenth character of the gap sets the backspace flip-flop, generating END BACKSPACE $\overline{\text{BSF}}$ true to the tape motion control module.

$\overline{\text{BSF}}$ true causes another PADV to be generated; this PADV is delayed slightly in seven-track machines, allowing the transport to backspace further to make up for the different read/write head spacing. The program control counter is then advanced from $\overline{Q_6}$ to $\overline{Q_7}$, the erase state. $\overline{\text{BSP}}$ then goes false and $\overline{\text{SRC}}$ is inhibited. $\overline{Q_7}$ true enables the erase delay gate and clears the backspace flip-flop. The erase delay gate is activated following a delay determined by the delay counter according to the capacity of the buffer. At this time the transport is moving forward, and erasing the erroneous block. Following the erase delay the erase delay gate is activated, generating $\overline{\text{SRTDF}}$ true. This causes another PADV to be generated by the tape motion control module, moving the program control counter from $\overline{Q_7}$ to $\overline{Q_1}$, starting the tape ramp-up and continuing the readout cycle, as described above. This process is repeated until the block is written correctly on tape.

3.2.5.3 Delay Counter

The delay counter, located on the tape timing control module, is used to time the start, stop, erase, file mark, and beginning of tape delays. It consists of three divide-by-sixteen counters in tandem. The counter is advanced by MO2001, a crystal-controlled frequency which effectively divides each inch of tape into 200 increments. MO2001 is supplied continuously from the time pulse generator module whenever the program control counter is not in the $\overline{\text{REST}}$ state, e.g., the tape is in motion.

Each time PADV is given the delay counter is reset; thus, whenever the program status changes the delay counter starts counting from 0. Four NAND gates are used to generate the different delays in conjunction with the counter: a start delay gate, a stop delay gate, an erase delay gate, and a gate used for both the end of file and the beginning of tape delays. Straps are used to provide different start and stop delays for nine-track and seven-track machines, to allow for the difference in read/write head spacing; it is 0.15 inch in nine-track machines and 0.30 inch in seven-track machines. The erase delay also varies according to the buffer size, since the portion of tape to be erased should be greater than the longest block that can be received by the memories.

3.2.5.4 Gap Counter

The gap counter, located on the tape motion control module, is used to time the LRC and CRC check characters in the gap. The counter consists of a divide-by-sixteen counter in tandem with a binary to octal decoder. The gap counter is advanced by data frequency pulse ROTP3. When the main program control counter moves from the RO mode to the $\overline{\text{CRC}}$ mode, $\overline{\text{CRC}}$ true gates ROTP3 to the clock input of the counter. On the count of two, equivalent to the third character space of the interrecord block, the counter issues CRCA, the first of two pulses needed for the writing of the CRC character; CRCA is used to toggle the CRC flip-flops on the CRC register an additional time before the CRC character is written on tape (see section 3.2.7.6). On the third count of the counter, equivalent to the fourth character space of the gap, CRCB is issued; CRCB is used to enable the output gates of the CRC register to allow the CRC character to be written on tape. On the seventh counter count, equivalent to the eighth character space of the gap, the gap counter outputs a pulse which gates ROTP2 through as WRITE AMPLIFIER RESET PULSE ($\overline{\text{WARS}}$). $\overline{\text{WARS}}$ is supplied to the write buffer module to return the flip-flops to a known state as required for the writing of the LRC character.

In seven-track recorders the strapping is changed so that $\overline{\text{WARS}}$ is given on the fourth character count of the gap, since in seven-track the LRC character is written on the four character spaces following the last data byte of the block.

3.2.5.5 Gap Detector

The gap detector is used to supply the LRC check pulse and to terminate the backspace operation during an error sequence, as well as during a read operation. The gap detector consists of a divide-by-sixteen counter, a flip-flop and associated gates. It is clocked by the data synchronized pulse ROTP1, but READ DATA STROBE (RDS) supplied from the read skew/delay gap detect module resets the counter during the data. When the interrecord gap is read, RDS is no longer supplied, and the counter keeps counting. On the third count it activates a gate which outputs READ END OF RECORD $\overline{\text{REOR}}$. On the tenth count it activates another gate which generates the LRC CHECK pulse, used to enable the LRC gate (see section 3.2.7). On the twelfth count of the gap detector a third gate is activated, generating READ GAP (RGAP) true. During a backspace operation, the tenth count of the gap is used to set the backspace flip-flop, generating $\overline{\text{BSF}}$. $\overline{\text{BSF}}$ true generates a PADV and terminates the backspace.

3.2.6 ERROR CHECK CHARACTERS AND READ-AFTER-WRITE CHECK

3.2.6.1 Introduction

In addition to the vertical parity check, nine-track recorders generate two check characters: the cyclic redundancy check (CRC), written four character spaces following the last data byte of the block, and the longitudinal redundancy check (LRC), written four character spaces following the CRC character. Seven-track recorders generate only the LRC character four character spaces following the last data byte of the block. The nature of the check characters and the process of their generation are described below. The error detection circuits contained in models with read-after-write electronics are described at the end of this section.

3.2.6.2 CRC Character

The cards used to generate the cyclic redundancy check (CRC) character are used in nine-track recorders exclusively. This check character is written at the end of each block, four character spaces after the final data character. The character itself is derived from the content of the block utilizing comparison circuits and shift registers, according to a prescribed method to derive a specific character, which can be checked when the tape is read in the computer system. Under certain conditions the computer is also able to reconstruct correct data, utilizing this check character, to arithmetically recover accurate data where errors existed within the block. The circuits that generate the CRCC are based on a complex equation that reduces the mathematical probability of an undetected error almost to zero. The formula itself is beyond the scope of this description and is not required for an understanding of the circuits for troubleshooting. The CRCC is generated by the CRC Register Type 3639, with some of the necessary functions supplied by CRC Control Type 3578. The CRC register consists basically of a nine-bit shift register connected as a ring counter. Figure 3-3 is a simplified diagram of the logic used. The input data, WDATA1, supplied from the memory readout control cards, is shifted from bit P toward bit 0, 0 toward 1, and so on, with bit 7 returning toward bit P. The subsequent stage of each bit is determined by the present state of the previous bit in the register, the present state of the data input to the given bit, and (in bits 2 through 5 only) the present state of bit 7. In tracks P, 0, 1, 6, and 7, the data input of the CRCR bit is compared with the present output of the previous stage in the CRCR. The comparison occurs in the first of two exclusive-OR gates. The output of that gate becomes an input to the second exclusive-OR gate. The other input of the second gate is the output of the same bit. The J-K flip-flops of the register are toggled by the CRC clock, CRCTP, supplied from the CRC control module. During the block, CRCTP consists of the write clock $\overline{\text{WCLK}}$, used to toggle the write amplifiers. During the gap, on the third character space following the last data byte, the gap counter on the tape motion control module supplies pulse $\overline{\text{CRCA}}$ which gates an additional ROTP2 pulse through as CRCTP. This toggles the CRC register an additional time following the data. On the fourth character space of the interrecord gap the gap counter issues pulse $\overline{\text{CRCB}}$ which is gated through the CRC control module to the CRC register. This pulse is used to enable the output gates of the shift register, thus transferring the actual CRC character to the tape on the fourth character space of the gap. Note that the CRC character written on tape is not the character contained in the shift register, but is derived from it. To facilitate troubleshooting a table of the CRC characters and the contents of the CRC register for all-1 blocks is given with the circuit description of the CRC register module in Section VI of the manual. The data channels output by the CRC register module are supplied to a set of gates located on the CRC Control Type 3578 module. The gates are enabled by WRITE SELECT WSEL2 true during the write mode, supplying the data to the write buffer module. The write buffer contains a set of output drivers which supply the data to the tape transport to be written on tape.

3.2.6.3 LRC Character

Following the writing of the CRC character (on nine-track recorders) the main program control counter on the tape timing control module moves from state $\overline{Q_3}$ to $\overline{Q_4}$, supplying $\overline{\text{LRC}}$ true to the tape motion control. This enables the gap counter on that module, and on the seventh character count, equivalent to the eighth character space of the interrecord gap, the gap counter issues a pulse which gates READ OUT TIME PULSE ROTP2 as WRITE AMPLIFIER RESET $\overline{\text{WARS}}$ to return the write amplifier flip-flops to a known state for the writing of the LRC character on tape. On seven-track recorders the strapping to the gap counter is changed so that $\overline{\text{WARS}}$ is issued on the third count, or the fourth character space of the gap.

3.2.6.4 Read-After-Write Check

Tape Timing Control Type 3633 includes a parity tree to check for the correct vertical parity, and an LRC register to check for an LRC error. READ DATA RDATA channels 0 through 7 are supplied from

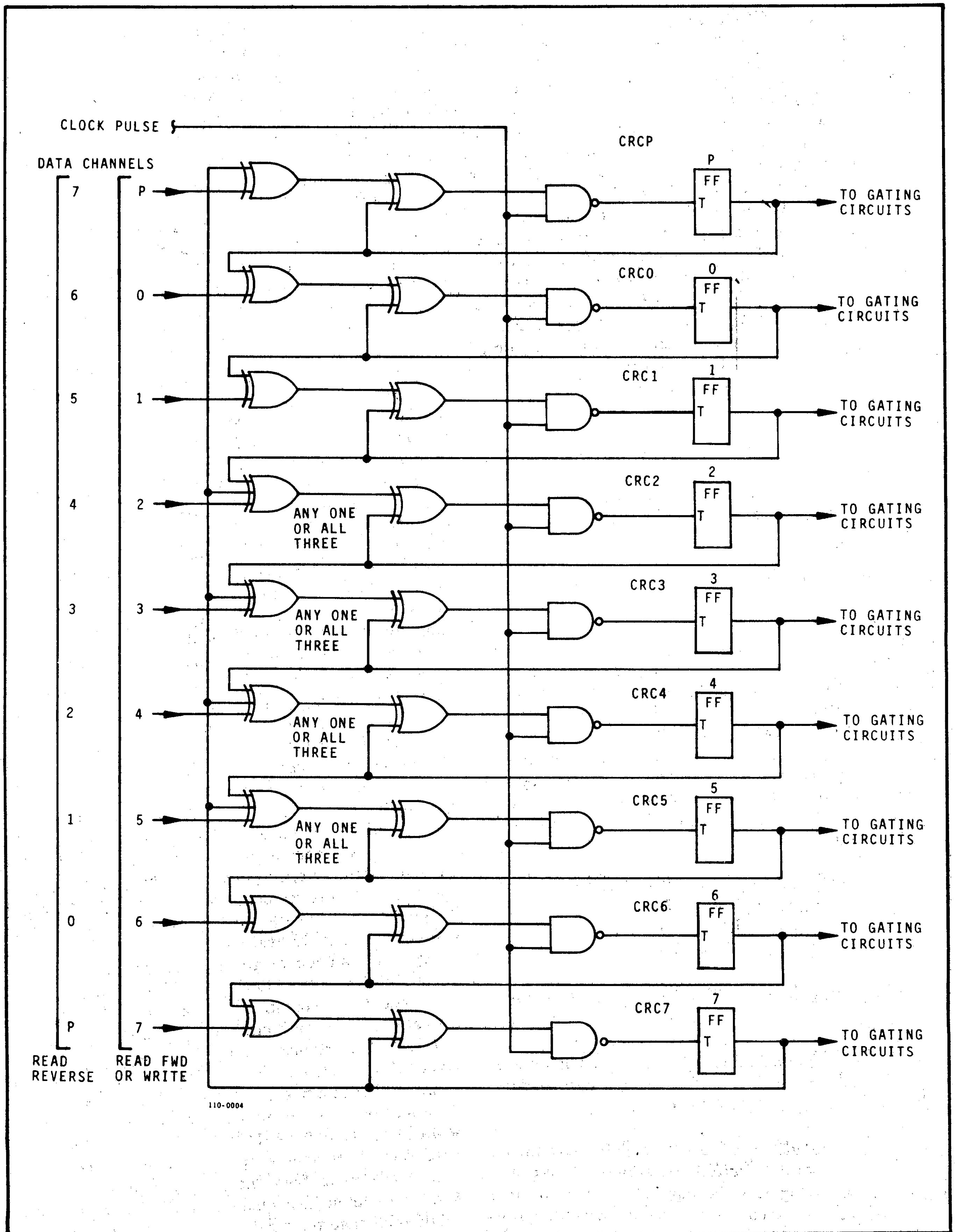


Figure 3-3. CRC Logic Diagram

the read skew delay/gap detect module to the parity tree and to the LRC register. The register consists of nine J-K flip-flops (seven for seven-track recorders) which are toggled by the READ DATA STROBE $\overline{RDS}$. The tape timing control module also contains a read gap detector consisting of a divide-by-sixteen counter with associated gating. READ OUT TIME PULSE ROTP1 is used to advance the gap detection counter, while each READ DATA STROBE clears the counter. When data is no longer detected $\overline{RDS}$ no longer clears the gap detector, and on the third ROTP1 count following the end of the data a READ END OF RECORD $\overline{REOR}$ is generated. On the tenth count of the gap an LRC CHECK pulse is generated, which is used to enable the LRC check gate. All the $\overline{Q}$ outputs of the LRC register are flip-flops connected to a NOR gate. Should any output be low when the LRC CHECK pulse is generated, an LRC error is detected.

Either the VRC error or LRC error sets the error flip-flop, causing the recorder to enter the error sequence, in which the transport backspaces, erases the erroneous block and rewrites it, as described in section 3.2.5.

3.3 READ CIRCUITS

3.3.1 INTRODUCTION

The reading of the data by the buffered formatter is quite similar to its writing, performed in reverse. The memory input control functions and buffer operation are nearly identical in the read and write modes, and it is highly recommended that the write circuits description be studied in detail before reading this section. This section concentrates in main on the read and control operations performed by the following modules:

Read Skew Delay/Gap Detect Type 3641
Read Control I Type 3817
Read Control II Type 3618
Read Control III Type 3660

3.3.2 READ DATA FLOW AND BUFFER OPERATION

The read data is supplied from the tape transport as RDTAP, and 0 through 7 (for nine-track recorders) to the deskew/gap delay module.

The module includes two sets of flip-flops, one of which is used as a data buffer that stores the incoming data, supplying it to the input of the second set of flip-flops. The second set is the skew delay register, which is toggled at the approximate midpoint of the character space by a skew counter output, also generated on that module. The skew counter is enabled by the first 1 bit of each character, and counts to approximately half the character space of the data being read. The character space is adjusted by a set of gates according to the density of the data. The output of the skew counter then toggles the skew delay register, supplying the deskewed data RDTA P, 0 through 7, to the memory module for storage and to the tape timing control module for error detection. For a complete description of the buffer operation see the buffer description of the write circuits, section 3.2.4. The buffer operation is identical in both the read and write, except for the different memory clocks used. The read input gates of the memories are enabled by READ SELECT and the read data is supplied to the available buffer, as determined by the state of A MEMORY READ IN ARI, supplied from the memory input control module. The memory clock during the read mode is similar to the write memory clock with the order reversed. First, the synchronous READ DATA STROBE, the read clock supplied from the skew delay/gap detect module, is supplied to the memory counter module, where it is gated through as the memory clock, either ACLK or BCLK, strobing the read data into the memory and toggling the memory counter. Once a whole record is read into the memory, RDS is terminated and pump clock PUCLK2 is used to shift the data record along the memory to its output. PUCLK2 is the same pump clock that is used in the write mode, except that it is gated with READ OUT START 2 (supplied from the memory input control module), and hence is supplied only when there is data available for readout. Once the data is at the output of the memory, the memory counter module generates RECORD FRAME RFRMA or RFRMB, to indicate that the data is valid. RFRMX (X standing for either A or B) is generated by the memory counter and the EOR counter stages (located on the memory counter module) of the memory that contains the read data. RFRMX is generated only during the period in which valid read data is available at the output of the memory, and is used to generate READ DATA AVAILABLE RDAVL true to the interface (on read control II module), indicating that a read data record is available for readout. Once RDAVL goes true, PUCLK2 is inhibited, and the asynchronous readout clock READ OUT ONE CHARACTER $\overline{ROOC}$ becomes the read memory clock. $\overline{ROOC}$ is supplied from the interface to read control III module, where it is OR'd with READ OUT CONTINUOUSLY $\overline{ROC}$ clock. The readout continuously option uses one of the crystal-generated data frequencies as the readout clock instead of an asynchronous clock from the interface. In either case the readout clock is supplied as READ OUT ONE CHARACTER ROOC2 to read control II module, where it is used to generate the INCREMENTAL READ CLOCK $\overline{IRCLK}$. $\overline{IRCLK}$ combines both the read pump clock PUCLK2 and ROOC2, and is supplied to the memory counter module, becoming the read memory clock. $\overline{IRCLK}$ strobes the data as RD P, 0 through 7, from the memories to the interface until the whole block is read out.

3.3.3 TAPE MOTION CONTROL DURING THE READ MODE

3.3.3.1 PROGRAM ADVANCE PADV2

During the read mode, the tape transport searches for data until both memories are filled, or until other conditions cause it to stop, as described below.

As in the write mode, the tape motion during the read mode is controlled by the program control counter on the tape timing control module. PROGRAM ADVANCE 2 PADV2 is used to advance the program control counter from one stage of operation to the next. PADV2 combines the program advance commands used in the write mode with additional "jump" commands used in the read, causing the counter to skip states that are not used during the read operation. For a complete description of the program control counter operation see section 3.2.5.

Read control I module generates two additional jump commands which are included in PADV2. When BACKSPACE FLIP-FLOP $\overline{BSF}$ goes true at the end of a read backspace operation, read control I generates a PADV2 command which causes the program control counter to skip over state $\overline{Q_7}$, the erase state during the write mode. An additional program advance command is generated after a block of data is read from the tape to keep the tape moving in a forward direction until the read stop delay is generated.

3.3.3.2 READ OUT START 4

In the read mode, the transport continuously searches for data until one of the following conditions is met: a) both buffers are filled; b) end of tape is detected, followed by a file mark; c) 25 feet of blank tape have been read; d) optionally, whenever an end-of-file tape mark has been detected; e) a STOP command has been issued by the interface. When none of the above conditions is true, read control II module generates READ OUT START 4. $\overline{ROSRT4}$ is routed through read control III module to the tape motion control module, where it generates PADV true, preventing the main program control counter from returning to $\overline{Q_0}$, the REST state. When any of the above conditions is met, $\overline{ROSRT4}$ is inhibited and the tape comes to a stop following the read stop delay. Thus when both buffers are full, or an end of tape is detected, or a file mark is detected, or 25 feet of blank tape are read, or a STOP command is issued, or (optionally) whenever any file mark is read, read control II module inhibits $\overline{ROSRT4}$, allowing the program control counter to go to the $\overline{REST}$ state.

3.3.3.3 READ STOP DELAY

On the tenth character of the interrecord gap, the tape timing control module issues READ GAP $\overline{RGAP}$ true to read control I module. This enables the read stop delay counter, located on read control I, and on the count of 8, equivalent to 0.04 inch of tape after the read gap has been detected, it issues STOP DELAY END $\overline{STPDF}$ true. $\overline{STPDF}$ is supplied to the tape timing control module where it returns the program control counter to the $\overline{REST}$ state, inhibiting the SYNCHRONOUS FORWARD COMMAND SFC on the tape motion control module, and causing the transport to ramp down to a stop.

3.3.4 READ ERROR SEQUENCE

If a read error is detected by the error detection circuits situated on the tape timing control module (see section 3.2.6), the transport automatically rereads the erroneous block a specified number of times, or until the block is read correctly. This operation is performed by read control I module as described below. When an error is detected, the tape timing control module supplies $\overline{ROSRT1}$ true to read control I module. This causes a MEMORY COUNTER RESET pulse either ARST or BRST to be generated, resetting the memory counters of the memory that contains the erroneous block, in effect erasing the data from that memory. The tape timing control module then causes the recorder to backspace over the erroneous block and reread it. The number of times the block is reread is determined by a counter located on read control I; this number can be 2, 4, or 8 times, as desired. Before the last rereading, read control I issues TAPE ERROR INHIBIT $\overline{TERI}$ to the tape timing control module, inhibiting the error detection circuits. In that case a permanent error indication READ BLOCK IN ERROR $\overline{RBIE}$ is supplied to the interface from read control I; this indication is delayed until it is resynchronized with the data read by the interface.

3.3.5 END OF FILE TAPE MARK DETECTION

The end of file mark is detected on the read control I module. The deskewed read data channels are supplied to a gating system located on that module that decodes both the nine-track and seven-track file marks. The decoding gates operate in such a way as to ignore any data character during a block that happens to be identical to the file mark, but recognizes only a block that contains nothing but file mark characters; e.g., the file mark itself. Once the file mark is detected, read control I issues TAPE ERROR INHIBIT $\overline{\text{TERI}}$ to the tape timing control module, preventing the tape mark from being detected as an error. Two tape mark indications are then issued; the first, $\overline{\text{RTMI}}$, is issued as soon as the gap following the tape mark is detected. $\overline{\text{RTMI}}$ is supplied to the read control II module to initiate the tape rampdown following the file mark detection, if the stop on EOF option is used. However, the second file mark indication, READ END OF FILE REOF, supplied to the interface, is delayed until it is resynchronized with the data being read by the interface. After the interface has received the other memory's data, the second file mark indication is issued.

3.3.6 HOLD OPTION

This option becomes particularly useful in data communication applications. When an error is detected during transmission of data, the block being transmitted may be recycled back into the memory and resent another time. When the interface issues $\overline{\text{HOLD}}$ true, read control II module inhibits READ OUT COMPLETE pulse $\overline{\text{ROCOMP2}}$ from being generated at the end of the readout, thus preventing the memory counter reset pulses from being issued. This retains the data block in the memory and it may be reread. Once HOLD goes false, $\overline{\text{ROCOMP2}}$ is issued, terminating the readout.

3.3.7 MEMORY CHECK OPTION

The memory check option provides for an error check of the memory stages. During a write mode, a parity tree is used to generate a parity check of the input write data channels, and during the read mode the P channel from the tape is cycled through the memory. An additional memory stage is provided for the parity channel, and the outputs of the memory stages are supplied to another parity tree. If one of the memory stages is defective, the output data will have the wrong parity, and a memory error indication will be supplied. The parity trees used in the memory check have the initial stages on the memory modules themselves. The final stages of the parity trees are situated on the time pulse generator module, which supplies the MEMORY ERROR indication $\overline{\text{MEMER}}$ true to the memory counter module. There the memory error indication is delayed until the erroneous block is made available to the interface, and is then output as MEMORY ERROR $\overline{\text{MEMER2}}$ to the interface.

SECTION V

PARTS IDENTIFICATION

SECTION V

PARTS IDENTIFICATION

5.1 SPARE PARTS ORDERING INFORMATION

This section describes the replaceable parts in your tape unit which are available only from Kennedy Company. Many parts of the unit are common commercial parts and can be obtained locally from the manufacturer. These parts are marked with the manufacturer's name and part number and are not listed herein.

The serial number and part number of the tape unit are the keys to numerous engineering details applying to your unit. These numbers are located on the serial number tag located on the rear panel of the unit. When ordering spare parts, accessories, or tools always specify the serial number and part number of your unit.

Changes to Kennedy units are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. If a part you have ordered has been replaced by a new part, a Kennedy representative will contact you concerning any change in part number.

All part orders should be addressed directly to Kennedy Company, Parts Order Department, 540 West Woodbury Road, Altadena, Ca 91001, telephone (213) 798-0953, TWX 910-588-3751.

5.2 IN-WARRANTY REPAIR PARTS ORDERING INFORMATION

Repair parts for in-warranty units are made available on an exchange basis through the Kennedy Company Customer Engineering Department.

The serial number and part number of the tape unit are necessary in order to insure shipment of the proper replacement parts.

All inquiries should be directed to Kennedy Company, Customer Engineering Department, 540 West Woodbury Road, Altadena, Ca 91001, telephone (213) 798-0953, TWX 910-588-3751.

5.3 EXPORT ORDERS

Customers outside the United States and Canada are served by Kennedy Company international sales agents. All correspondence regarding your tape unit should be directed to your sales agent. If you prefer, correspondence may be addressed directly to Kennedy Company, Parts Order Department, 540 West Woodbury Road, Altadena, Ca 91001, TWX 910-588-3751, cable KENNEDYCO.

5.4 ILLUSTRATED PARTS LIST

To assist in part identification an illustrated parts list is included in this section with references to photographs of the machine. All major parts are shown but those considered replaceable are indicated by the first three digits of the part number being 198. These items are listed again in the replaceable parts list together with correct part numbers for reordering.

5.5 FIELD KITS

Some replacement components may be supplied in the form of repair or field change kits. The repair kits contain parts that are matched or assembled and adjusted at the factory because of complexity or to aid the field technician. The components ordered as field kits either by correspondence with Kennedy service engineers or by direct order will be supplied with complete installation instructions. The change kits are intended for standard or special options not originally included in the unit.

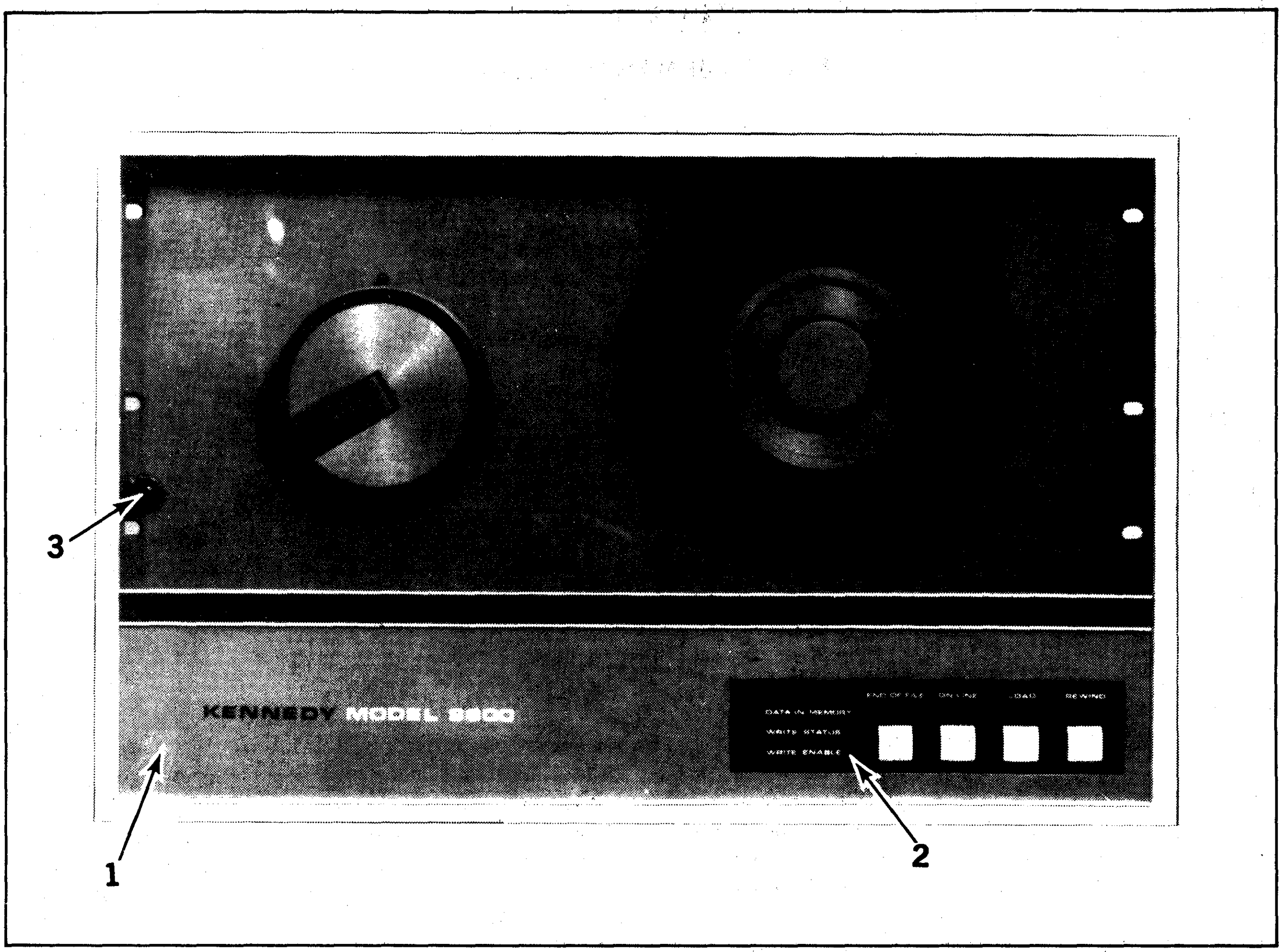


Figure 5-1. Model 9832 Chassis: Front View (Dust Cover Closed)

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-1

ITEM	PART NO.	DESCRIPTION
5-1-1	190-3373-004	Dust Cover Assembly
5-1-2	890-3371-005	Control Panel Assembly
5-1-3	191-2915-001	Door Latch
5-1-3	128-0003-002	Door Catch

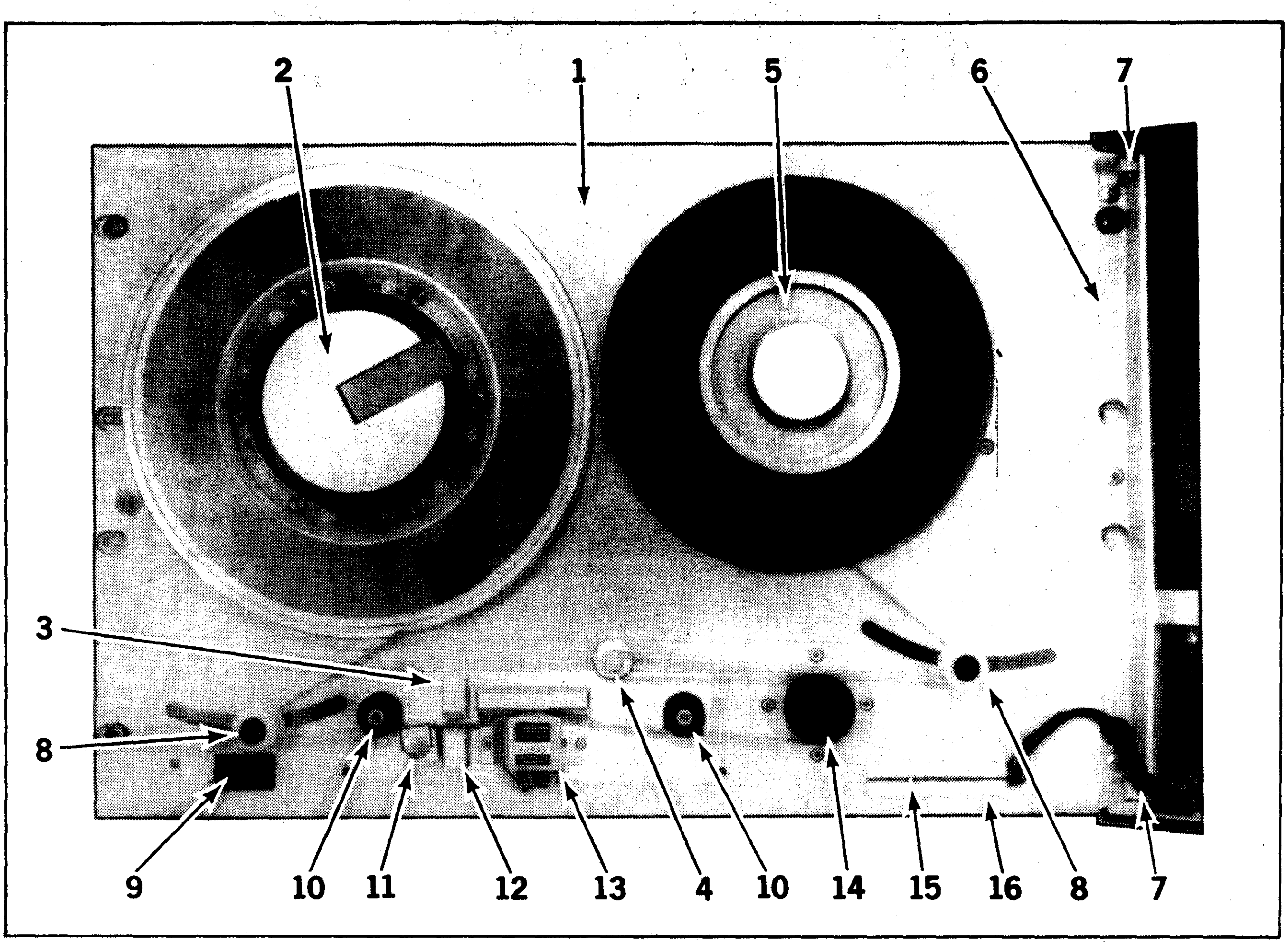


Figure 5-2. Model 9832 Chassis: Front View (Dust Cover Open)

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-2

ITEM	PART NO.	DESCRIPTION
5-2-1	190-3955-002	Deck Assembly
5-2-2	890-2744-001	Quick Release Hub
5-2-2	198-0010-001	Hub Bearing Assembly
5-2-2	825-0030-006	O-Ring
5-2-2	828-0090-001	Spring Washer
5-2-3	890-1138-001	Load Point/EOT Photosensor Assembly
5-2-4	890-2627-001	Idler Assembly
5-2-5	890-2772-002	Takeup Hub Assembly
5-2-6	291-2964-005	Dust Cover Mount
5-2-7	191-2966-001	Hinge Pin
5-2-8	890-2647-002	Tension Roller Guide Assembly
5-2-9	851-0038-001	Power Switch
5-2-10	890-1509-001	Split Tape Guide Assembly
5-2-11	190-2747-001	Tape Cleaner Assembly
5-2-12	890-1139-001	Broken Tape Photosensor Assembly
5-2-13	198-2399-010	Head and Head Mounting Assembly, 9 Track Read and Write
5-2-13	198-2399-020	Head and Head Mounting Assembly, 9 Track Read Only
5-2-13	198-2399-003	Head and Head Mounting Assembly, 7 Track Read and Write
5-2-14	890-2605-001	Capstan

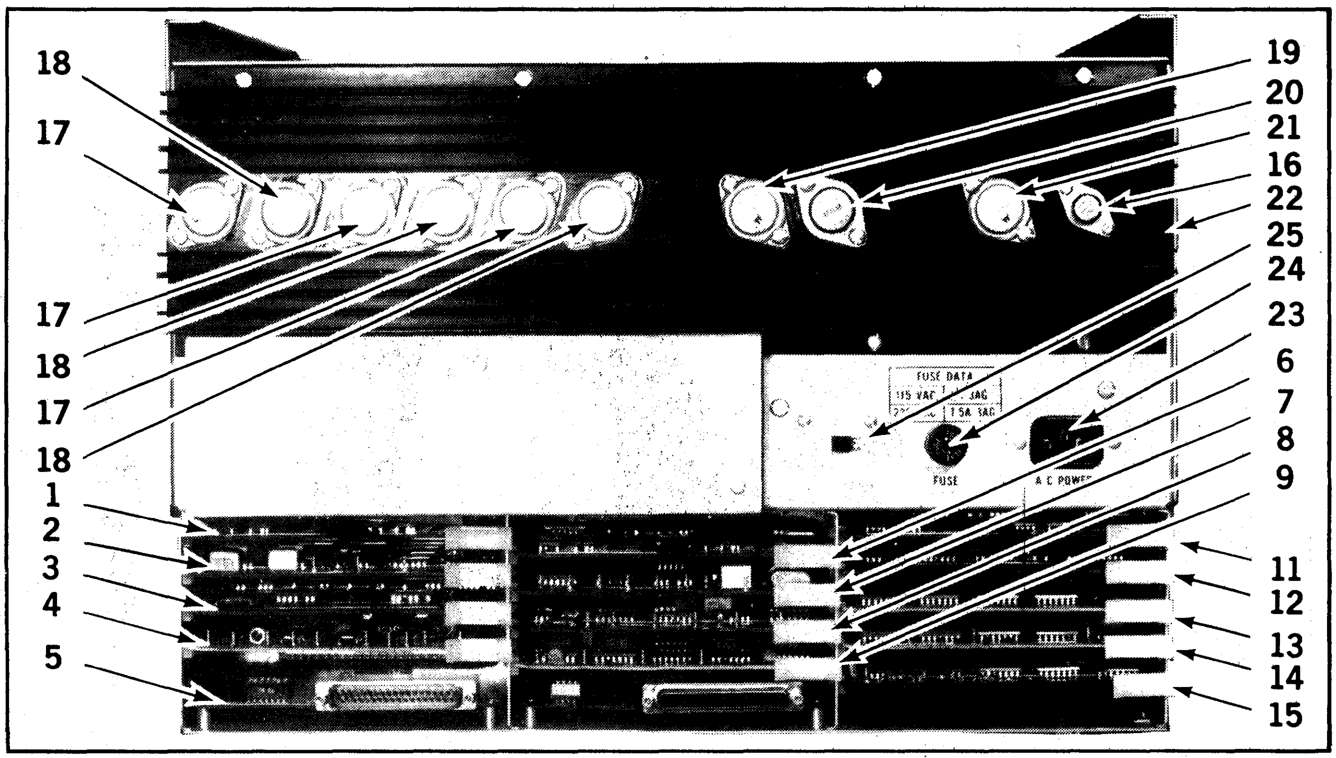


Figure 5-3. Model 9832 Chassis - Rear View

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-3

ITEM	PART NO.	DESCRIPTION	NOTES
5-3-1	890-3638-xxx	Memory Board	1
5-3-2	890-3616-xxx	Tape Motion Control Baord	1
5-3-3	890-3578-xxx	CRC Control Board	1
5-3-4	890-3639-xxx	CRC Register Board	1
5-3-5	890-4463-002	Interface Board and Connector	1
5-3-6	890-3638-xxx	Memory Board	1
5-3-7	890-3640-xxx	Time Pulse Generator Board	1
5-3-8	890-3516-xxx	Memory Input Control	1
5-3-9	890-3607-xxx	Memory Counter	1
5-3-10	890-4463-001	Interface Board and Connector	1
5-3-11	890-3638-xxx	Memory Board	1
5-3-12	890-3660-xxx	Read Control Board	1
5-3-13	890-3618-xxx	Read Control Board	1
5-3-14	890-3817-xxx	Read Control Board	1
5-3-15	890-3633-xxx	Tape Timing Control	1
5-3-16	148-0075-001	Power Transistor, Type 2N4910	
5-3-17	148-0122-001	Power Transistor, Type MJ802 Motorola	
5-3-18	148-0121-001	Power Transistor, Type MJ4502 Motorola	
5-3-19	148-0102-003	Power Transistor, Type MJ900 Motorola	
5-3-20	148-0102-004	Power Transistor, Type MJ1000 Motorola	
5-3-21	148-0053-001	Power Transistor, Type 2N3055	
5-3-22	890-4352-001	Voltage Regulator PC Board	
5-3-22	890-4441-001	Regulator and Servo Assembly	
5-3-23	127-0003-001	Power Receptacle	
5-3-24	151-0802-001	Fuseholder	
5-3-24	851-0133-030	Fuse, 3AG, 3A (115 vac operation, box of 5)	
5-3-24	851-0133-015	Fuse, 3AG, 1.5A (220 vac operation, box of 5)	
5-3-25	851-5001-103	Switch, 115/220 vac	

NOTE 1: When ordering board, replace -xxx with dash number stamped on the original circuit board.

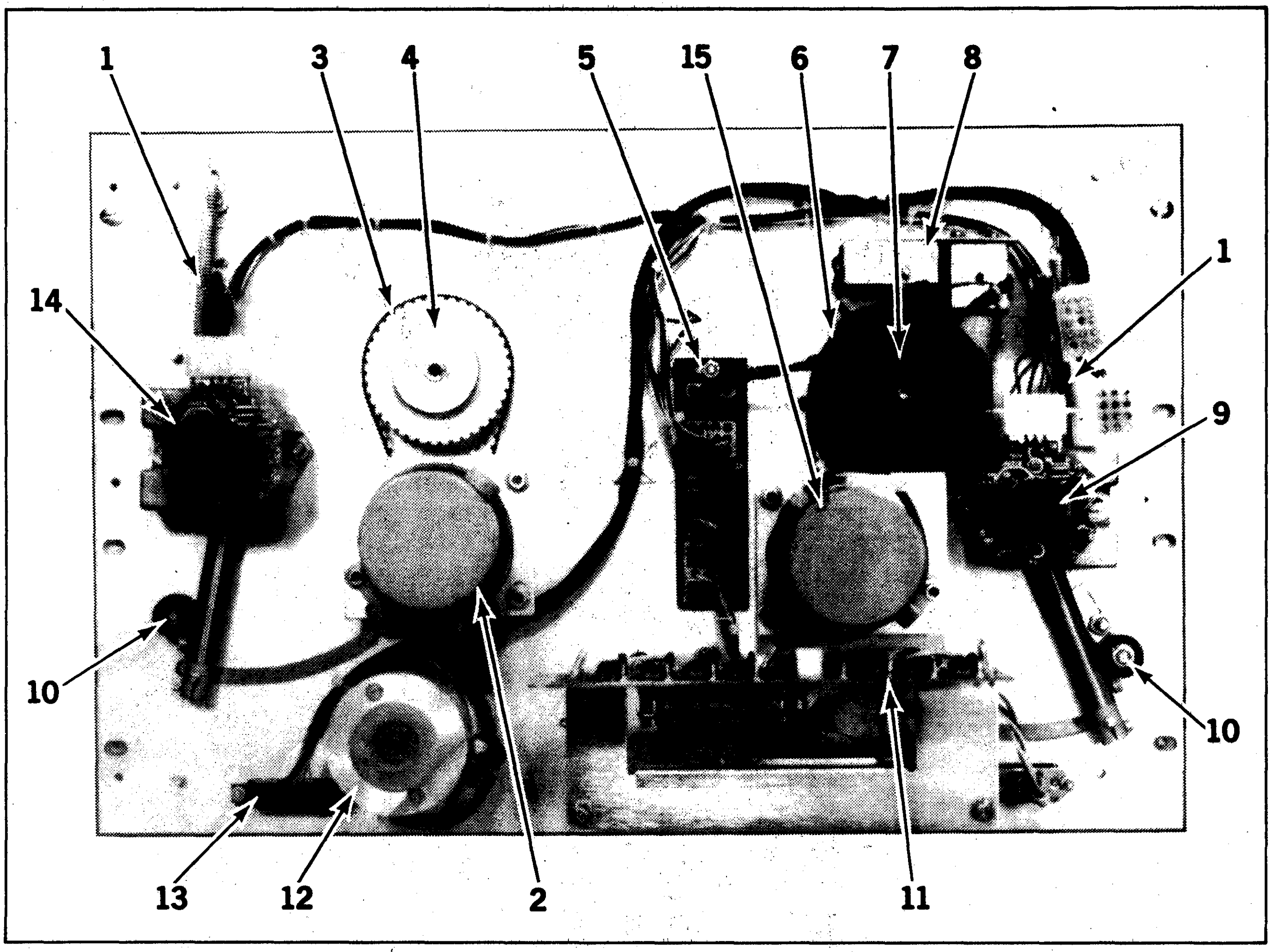


Figure 5-4. Model 9832 Chassis: Rear View (Power Supply Removed)

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-4

ITEM	PART NO.	DESCRIPTION	NOTE
5-4-1	825-0017-003	Extension Spring	
5-4-2	890-4438-002	Takeup Reel Motor Assembly, 16 Tooth	
5-4-3	825-0004-002	Takeup Reel Drive Belt	
5-4-4	191-0805-001	Takeup Reel Drive Pulley	
5-4-5	890-4013-001	Connector PC Board Assembly	
5-4-6	825-0004-003	Supply Reel Drive Belt	
5-4-7	191-2643-001	Supply Reel Drive Pulley	
5-4-8	890-2641-001	File Protect Switch Assembly	
5-4-9	198-0009-011	Supply Reel Magpot Sensor Assembly, complete	
5-4-9	890-4210-002	Magpot PC Board Assembly	
5-4-10	828-0067-001	Recessed Bumper	
5-4-11	890-3631-xxx	Read Preamplifier Assembly	1
5-4-12	890-2484-001	Capstan Motor Assembly	
5-4-13	121-0145-004	20 Pin Connector	
5-4-14	198-0009-012	Takeup Reel Magpot Sensor Assembly, complete	
5-4-14	890-4210-002	Magpot PC Board	
5-4-15	890-4438-001	Supply Reel Motor Assembly, 14 Tooth	

NOTE 1: Refer to dash number stamped on circuit board to determine complete part number.

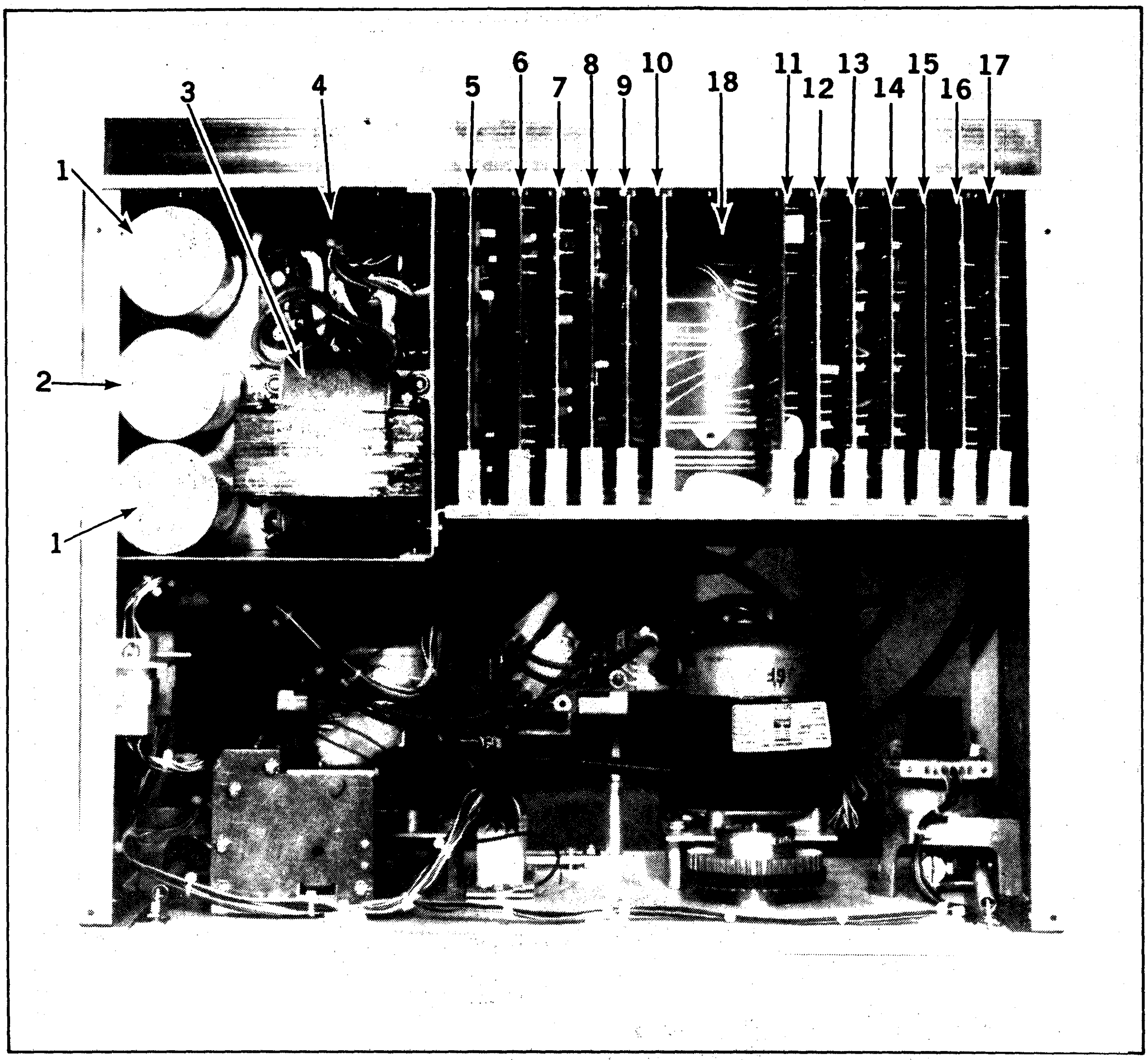


Figure 5-5. Model 9832 Tape Transport: Top View

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-5

ITEM	PART NO.	DESCRIPTION
5-5-1	815-3625-199	Capacitor, Aluminum, Electrolytic, 19K mfd, 25 vdc
5-5-2	815-3610-449	Capacitor, Electrolytic, 44K mfd, 10 vdc
5-5-3	890-4474-001	Power Transformer Assembly
5-5-5 thru 5-5-18		For part number, see Recomended Spare Parts List

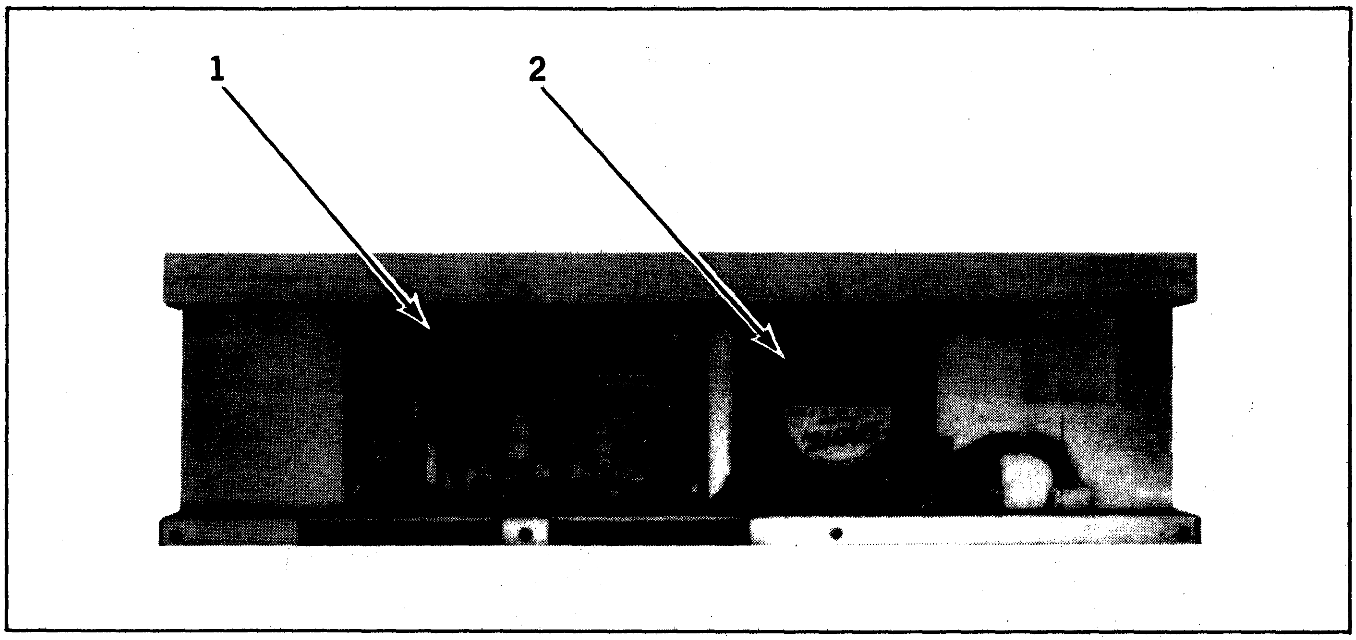


Figure 5-6. Model 9832 Chassis - Front View (Shown Separated From 9800 Tape Transport)

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-6

ITEM	PART NO.	DESCRIPTION
5-6-1	190-4480-001	Power Supply Regulator PC Board
5-6-2	126-0007-001	Fan, Pamotor Model 8110, 24 VDC
5-6-2	125-0032-001	Fan, Rotron Model PNLY2A1 (AC versions)

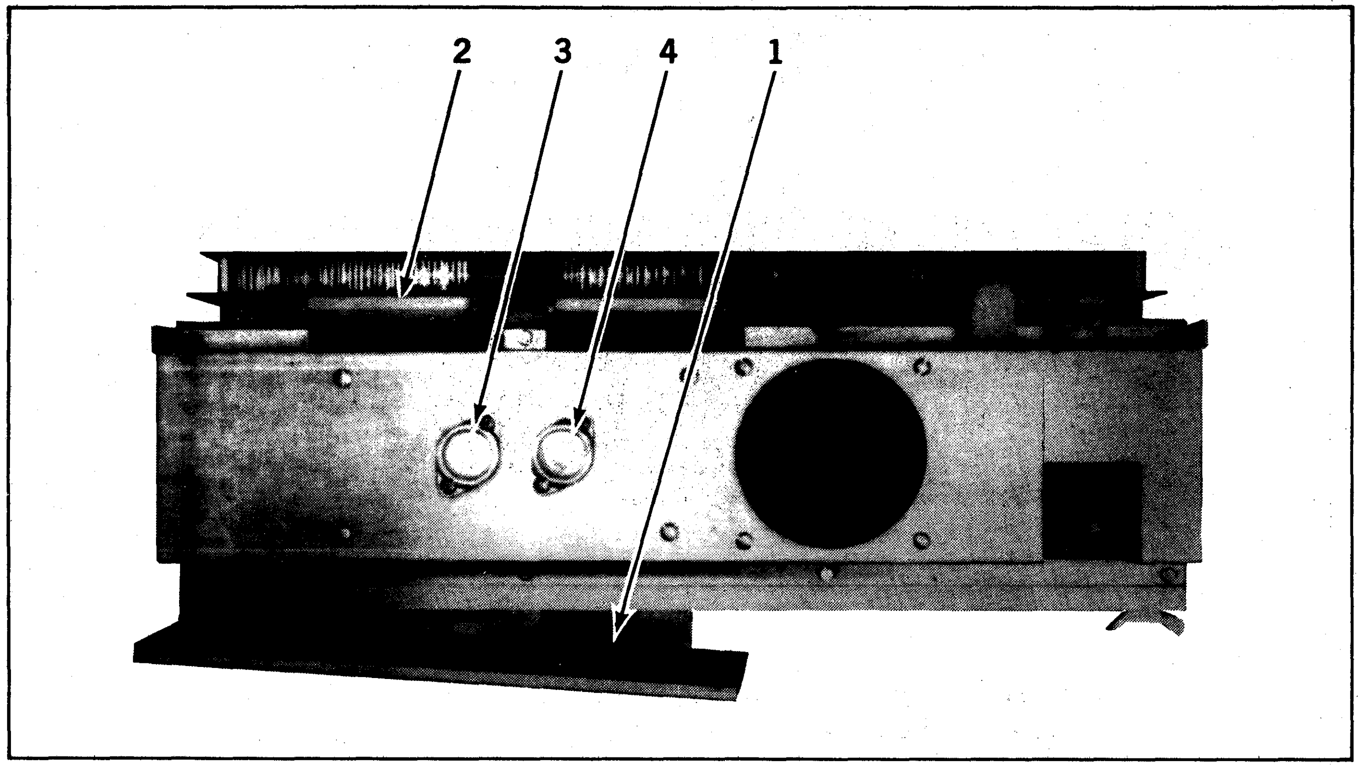


Figure 5-7. Model 9832 Chassis - Top View (Shown Separated From 9800 Tape Transport)

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-7

ITEM	PART NO.	DESCRIPTION
5-7-1	190-4461-001	Connector PC Board
5-7-2	190-4462-001	Masterboard
5-7-3	148-0122-001	Transistor-Power Silicon, MJ802
5-7-4	148-0102-003	Transistor

RECOMMENDED SPARE PARTS LIST

Item No.	Part No.	Description	Qty	Note
5-1-2	890-3371-005	Control Panel Assembly	1	
5-2-2	198-0010-001	Hub Bearing Assembly	1	
5-2-3	890-1138-001	Load Point/EOT Photosensor Assembly	1	
5-2-4	890-2627-001	Idler Assembly	1	
5-2-8	890-2647-002	Tension Roller Guide Assembly	1	
5-2-9	851-0038-001	Power Switch	1	
5-2-10	851-1509-001	Split Tape Guide Assembly	1	
5-2-12	890-1139-001	Broken Tape Photosensor Assembly	1	
5-2-13	198-2399-010	Head and Head Mounting Assembly, 9 Track RAW	1	
5-2-13	198-2399-003	Head and Head Mounting Assembly, 7 Track RAW	1	
5-2-14	890-2605-001	Capstan	1	
5-3-1	890-3638-xxx	Memory Board	1	1
5-3-2	890-3616-xxx	Tape Motion Control Board	1	1
5-3-3	890-3578-xxx	CRC Control Board	1	1
5-3-4	890-3639-xxx	CRC Register Board	1	1
5-3-5	890-4463-002	Interface Board and Connector	1	
5-3-6	890-3638-xxx	Memory Board	1	1
5-3-7	890-3640-xxx	Time Pulse Generator Board	1	1
5-3-8	890-3516-xxx	Memory Input Control	1	1
5-3-9	890-3607-xxx	Memory Counter	1	1
5-3-10	890-4463-001	Interface Board and Connector	1	
5-3-11	890-3638-xxx	Memory Board	1	1
5-3-12	890-3660-xxx	Read Control Board	1	1
5-3-13	890-3618-xxx	Read Control Board	1	1
5-3-14	890-3817-xxx	Read Control Board	1	1
5-3-15	890-3633-xxx	Tape Timing Control	1	1
5-3-16	848-0075-001	Power Transistor, Type 2N4910		
5-3-22	890-4352-001	Voltage Regulator PC Board	1	
5-3-22	890-4441-001	Regulator and Servo Assembly, complete	1	
5-3-24	851-0133-030	Fuse, 3AG, 3A (115 vac use, box of 5)	1	
5-3-24	851-0133-015	Fuse, 3AG, 1.5A (220 vac use, box of 5)	1	
5-3-25	851-5001-103	Switch, 115/220 vac	1	
5-4-1	825-0017-003	Extension Spring	2	
5-4-2	890-4438-002	Takeup Reel Motor Assembly, 16 Tooth	1	
5-4-3	825-0004-002	Takeup Reel Drive Belt	1	
5-4-5	890-4013-001	Connector PC Board Assembly	1	
5-4-6	825-0004-003	Supply Reel Drive Belt	1	
5-4-8	890-2641-001	File Protect Switch Assembly	1	
5-4-9	198-0009-011	Supply Reel Magpot Sensor, complete	1	
5-4-9	890-4210-002	Magpot PC Board Assembly	1	
5-4-11	890-3631-xxx	Read Preamplifier Assembly	1	1
5-4-12	890-2484-004	Capstan Motor Assembly	1	
5-4-14	198-0009-012	Takeup Reel Magpot Sensor Assembly, complete	1	
5-4-14	890-4210-002	Magpot PC Board Assembly	1	
5-4-15	890-4438-001	Supply Reel Motor Assembly, 14 Tooth	1	
5-5-1	815-3625-199	Capacitor, Electrolytic, 19K mfd, 25 vdc	1	
5-5-2	815-3610-449	Capacitor, Electrolytic, 44K mfd, 10 vdc	1	
5-5-3	890-4474-001	Power Transformer Assembly	1	
5-5-5	890-4306-xxx	Servo Preamplifier PC Board	1	1
5-5-6	890-3844-xxx	Sensor Amplifer/Driver PC Board	1	1

NOTE 1: PC board dash number will vary depending upon machine specifications. Refer to the circuit board identification card in the machine or check the PC board for the stamped dash number.

RECOMMENDED SPARE PARTS LIST
(Continued)

Item No.	Part No.	Description	Qty	Notes
5-5-7	890-3645-xxx	Ramp Generator PC Board	1	1
5-5-8	890-3843-xxx	Pushbutton Control PC Board	1	1
5-5-9	890-3842-xxx	Interface Control PC Board	1	1
5-5-11	890-3845-xxx	Delay Timing PC Board	1	1
5-5-11	890-4118-xxx	7 Track Delay Timing PC Board	1	1
5-5-11	890-4365-xxx	Dual Density Control PC Board (Dual Density Models)	1	1
5-5-11	890-4209-xxx	Read Control Logic	1	1
5-5-12	890-4179-xxx	Read Amplifier/Clipping Level Control	1	1
5-5-12	890-4188-xxx	Read Amplifier/Clipping Level Control (1600 cpi Models)	1	1
5-5-12	890-4367-xxx	Dual P Channel Clipping Level Control (Dual Density Models)	1	1
OR:	890-6367-xxx	Dual P Channel Clipping Control (Dual Density Models)	1	1
5-5-13	890-4178-xxx	Quad Read Amplifier PC Board	1	1
5-5-13	890-4139-xxx	Quad PE Read Detector (PE Models)	1	1
5-5-13	890-4385-xxx	Quad Read Amplifier PC Board (Dual Density Models)	1	1
5-5-14	890-4178-xxx	Quad Read Amplifier PC Board	1	1
5-5-14	890-4385-xxx	Quad Read Amplifier PC Board (Dual Density Models)	1	1
OR:	890-6385-xxx	Quad Read Amplifier (Dual Density Models)	1	1
5-5-16	890-3848-xxx	Four Channel Write Amplifier PC Board	1	1
5-5-16	890-4207-xxx	Four Channel PE Write Amplifier (PE Models)	1	1
5-5-16	890-4366-xxx	Four Channel Write Amplifier (Dual Density Models)	1	1
5-5-17	890-3849-xxx	Five Channel Write Amplifier	1	1
5-5-17	890-4208-xxx	Five Channel PE Write Amplifier (PE Models)	1	1
5-5-17	890-4368-xxx	Five Channel Write Amplifer (Dual Density Models)	1	1
5-5-18	890-4206-001	Masterboard	1	
5-5-18	890-4509-001	Masterboard (Dual Density Models)	1	
Not shown	825-0068-001	Power Cord (115 vac use)	1	
Not shown	821-9000-003	Power Cord (230 vac use)	1	
Not shown	198-0103-001	Brush Replacement Kit, Capstan Motor Tachometer	1	
Not shown	198-0075-001	Brush Replacement Kit, Reel Motor (4 brushes)	1	
Not shown	198-0100-001	Hub Repair Kit	1	2

NOTE 1: PC board dash number will vary depending upon machine specifications. Refer to the circuit board identification card in the machine or check the PC board for the stamped dash number.

NOTE 2: Hub repair kit contains items subject to wear, i.e: O ring, reel drive latch, and thrust washer.

SECTION VI

WIRING AND SCHEMATIC DIAGRAMS

SECTION VI
WIRING AND SCHEMATIC DIAGRAMS

CIRCUIT CARD IDENTIFICATION		
LOC.	TYPE	FUNCTION
1	3638-001	MEMORY
2	3660-002	READ CONTROL III
3	3618-001	READ CONTROL II
4	3817-002	READ CONTROL I
5	3633-101	TAPE TIMING CONTROL

CIRCUIT CARD IDENTIFICATION		
LOC.	TYPE	FUNCTION
6	3638-002	MEMORY
7	3640-002	TIME PULSE GENERATOR
8	3516-004	MEMORY INPUT CONTROL
9	3607-002	MEMORY COUNTER
10	4463-001	INTERFACE

CIRCUIT CARD IDENTIFICATION		
LOC.	TYPE	FUNCTION
11	3638-002	MEMORY
12	3616-003	TAPE MOTION CONTROL
13	3578-001	CRC CONTROL
14	3639-001	CRC REGISTER
15	4463-002	INTERFACE

NOTES TO SCHEMATIC SECTION

Certain conventions have been observed in preparing schematics for this manual:

1. Resistor values are given in ohms. If wattage is unspecified the resistor may be either 1/4 or 1/2 watt.

2. Capacitor values may be given in picofarads or microfarads. Those values for which neither designation is provided are assumed to be obvious from circuit function. Filter capacitors on certain supply lines do not have logic significance. In general, they are not shown on schematics. On PC board silkscreens they are designated as CF.

3. Normally, IC power connections are on pins 14 (+5v) and 7 (ground) for 14 pin packages, and 16 (+5v) and 8 (ground) for 16 pin packages. Some ICs — 7476, 7492, 7493 for example — have power connections on pin 5 (+5v) and pin 10 (ground). Operational amplifiers in the 8 pin package have power connections on pin 4 (-Vcc) and pin 7 (+Vcc). Power connections are not shown unless they are nonstandard.

4. Where multiple inputs are tied together only one pin may be designated on the schematic.

5. Unused inputs that are tied high are not normally indicated unless the connection has logic significance.

6. From and to designations are intended to describe inputs and outputs only. The same signal may be connected to several other points not shown on a particular drawing.

7. Abbreviations used in from and to designations are as follows:

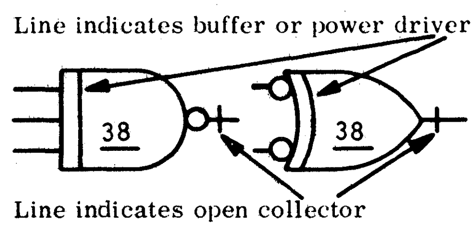
CI	Control Interface
PBC	Pushbutton Control
RG	Ramp Generator
SA	Sensor Amplifier/Driver
DT	Delay Timing
RA/CL	Read Amplifier/Clipping Level
RA	Quad Read Amplifier
WA1	Four Channel Write Amplifier
WA2	Five Channel Write Amplifier

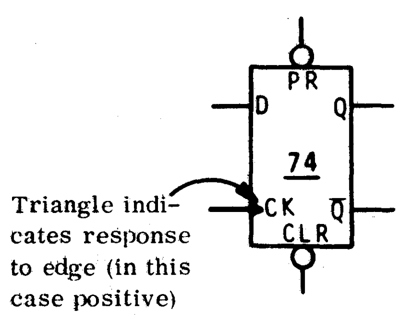
8. Positive logic is shown for all internal connections. Interface connections are zero true but the bar is omitted.

9. Integrated circuit symbols contain a circuit designator that corresponds to the number silkscreened onto the circuit module above an underlined number representing the IC type.

   The IC type number is abbreviated and omits the portions of the manufacturer's type number pertaining to case and vendor identification. Further, since the TTL 7400 series makes up most of the circuitry, the 74 is omitted on these. Thus a 00 designation indicates a 7400 quad two input NAND gate. T.I.'s complete part number is SN7400N. In multifunctional units in close proximity to each other the type designation may be omitted. The type designation may appear outside the symbol if the symbol is too small.

   Military Standard 806C is the base for logic symbols. Additional conventions are shown below.



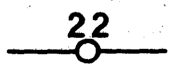


10. Semiconductor types on schematics may be replaced by their functional equivalents. If not indicated, diodes are 1N914, NPN transistors are 2N2714, and PNP transistors are MPS6517.

11. Unless otherwise specified, light emitting diodes are FLV102 or equivalent.

12. Module connector pins are shown as

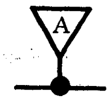
where no further connection is shown on the schematic, and as



when there is a connection shown.

13. Where an input is represented by an arrow instead of a complete line, the input source is designated. Where outputs are so shown their destinations may not be shown.

14. Some schematics of modules include certain external elements which aid in understanding the circuit function. In this case all the connections to the element may not be shown in the interest of clarity.

15. 

designates a test point provided on the module. Letters proceed from top to bottom of card with the ground test point, if present, as the bottommost terminal.

16. Socket terminals are designated with numbers for component side connections and letters for circuit side connections when a double sided socket is used. These are the designations on the socket. When a single sided socket is provided, all connections are designated by letters regardless of which side of the board they lie on the etch. Letters follow the 22 pin alphabet, ABCDEFHJKLMNPRSTUVWXYZ; numbers are 1 through 22.

TYPE 3640 TIME PULSE GENERATOR

CIRCUIT DESCRIPTION

This module performs the following functions:

a. Contains the master oscillator and dividing network

b. Generates the pump clock

c. Generates MO2001 clock

d. Outputs WRITE COMMAND $\overline{\text{WCMD1}}$

e. Supplies the parity channel output

This module contains a crystal-controlled master clock oscillator and a clock dividing network, used to generate all the synchronous clocks used in the formatter. The crystal-controlled master clock is a square-wave generator consisting of two inverter sections of IC14 with a quartz crystal Y1 connected in the feedback loop. The crystal frequency is selected as a function of tape speed, as shown in the tabulation on the schematic diagram. For tape speeds of 20 ips and higher, the MASTER CLOCK FMCLK output at pin 22 is the same frequency as the crystal oscillator. For slower tape speeds, e.g., 15 ips, strap 5 is used, connecting the divide-by-two counter IC18-12 between the oscillator and the output. This sets FMCLK at one-half the crystal frequency. FMCLK is supplied to a dividing network consisting of ICs 11, 16, 17, and 18, to provide the synchronous readout clock frequencies required for writing the various data densities. The master clock frequency is divided by 256 to supply the 200 cpi frequency MO200 at output pin Y and to NAND gate IC6-4, by 64 to supply the 800 cpi frequency to NAND gate IC9, and by 32 to supply the 1600 cpi frequency to NAND gate IC1-1. To derive the 556 cpi frequency, flip-flops IC11 are used in addition to the main dividing chain, in order to divide the master clock frequency by 92. The 556 cpi frequency is supplied to NAND gate IC6-1. To select the data density, two lines, TRANSPORT SELECT DENSITY TSDY1 and TSDY2, are supplied from the tape transport at input pins U and V. The two density select lines encode the selected density as tabulated below.

Selected Density (cpi)	TSDY1	TSDY2
200	high	high
556	high	low
800	low	high
1600	low	low

Whenever a particular density is selected, the two density select lines enable one of the gates which routes the corresponding master frequency through to NOR gate IC1-8 to be output as READOUT OSCILLATOR ROOSC at output pin X (test point F). ROOSC is supplied to the tape motion control module where it is used to generate the various readout time pulses. The 200 cpi frequency is also output at pin Y as MO200 to read control III module to be used as the READ OUT CONTINUOUSLY (ROC) clock whenever that option is used.

PUCLK AND $\overline{\text{PUCLK2}}$

The master clock frequency divided-by-two is supplied at pin Z (test point E) as the PUMP CLOCK PUCLK. PUCLK is supplied to the memory counter module to be used as the memory clock during a segment of the write memory cycle, advancing the data record to the output of the memory. On this module PUCLK is also gated with READ OUT START 2 ROSRT2 through NAND gate 4-11 and is output as $\overline{\text{PUCLK2}}$ at output pin 6. $\overline{\text{PUCLK2}}$ is supplied to read control II module where it is incorporated in the INCREMENTAL READ CLOCK $\overline{\text{IRCLK}}$. $\overline{\text{PUCLK2}}$ is thus supplied only when one of the memories has received a complete record or is filled. $\overline{\text{PUCLK2}}$ is used as the pump clock during the read mode, advancing the read data to the output of the memory in the same manner as in the write mode.

MO2001

The 200 cpi master oscillator frequency is gated with the $\overline{\text{REST}}$ output of the program control counter on the tape timing control module and is output as MO2001 at pin 7 to the tape timing control module. MO2001 is supplied only when the tape is in motion ($\overline{\text{REST}}$ false), and effectively divides each inch of tape into 200 increments, regardless of the readout frequency. It is used to clock the delay counter on the tape timing control module and the blank tape detector on read control II.

WRITE COMMAND $\overline{\text{WCMD1}}$

The input asynchronous write clock WRITE STEP is supplied from the interface at input pin R, and is gated with ZTSEL to provide the proper polarity. It is then supplied to NAND gate IC10-10 and to inverter IC10-1. NAND gate IC10 is enabled by $\overline{\text{BUSY}}$ false at pin 9 and by WRITE SELECT 3 $\overline{\text{WSEL3}}$ true at input pin 13. IC10-8 is then activated following a delay of 0.5 μsec, due to capacitor C4 on the extender of the gate. The output signal of the gate is inverted by IC14-2 and is gated to NAND gate IC9-4. Inverter IC10-6 delays the write command by approximately 1.5 μsec; e.g., IC10-6 remains high for 1 μsec after IC14-2 has gone high. IC9-6 then generates the output WRITE COMMAND $\overline{\text{WCMD1}}$ of 1 μsec (test point C) regardless of the duration of the input WRITE STEP. $\overline{\text{WCMD1}}$, output at pin T, is supplied to the memory counter module to become the read-in clock during the write mode, strobing the write data into the memory.

CHANNEL P GENERATION

This module also includes the output segment of the parity tree used to generate the parity channel. The initial segments of the parity tree are located on the memory modules. The output data channel from the memories is supplied to the initial stages of the parity tree, which is then supplied to this module as PCHKB (P, 0, 1), PCHKB (3, 4, 5) and PCHKB (6, 7) at input pins E, F, and 12. These inputs are supplied to a pair of exclusive-OR gates IC5, which supply the parity channel DTA1(P) at output pin A. In recorders with the memory error check option, the parity channel is also generated during a write mode at the input of the memory, and is then cycled through the memory with the other write data channels. The initial segments of this parity tree are also located on the memory modules, and are supplied to this card as PCHKA (P, 0, 1), PCHKA (3-5), and PCHKA (6, 7) at input pins 1, 2, and 5. These inputs are supplied to a pair of IC5 exclusive-OR gates whose output is gated with WSEL2 to generate the output parity channel $\overline{\text{DTA1(P)}}$ at output pin H (test point A). This parity channel is supplied to the input of the P channel memory stage. During a read mode the parity channel read from the tape is cycled through the memory.

MEMORY INPUT CONTROL TYPE 3516

CIRCUIT DESCRIPTION

This module performs the following functions in controlling the operation of the buffer memories:

a. It determines which memory is available for read-in and which is available for readout, switching memories in response to an EOR command or when a memory is filled.

b. It generates $\overline{\text{BUSY}}$ output when both memories contain data available for readout, inhibiting any further input data until a memory becomes available.

c. It delays the writing of the EOF, if required, until both memories are empty, and generates an automatic EOR before the EOF is carried out.

READ IN AND READ OUT CONTROL

This module controls the data input and output of the memories, determining which memory is available for read-in, and which is available for readout. When the recorder is initially turned on, PRESET $\overline{\text{PST}}$ at input pin J clears the two readout available flip-flops IC10, setting both AROA, A MEMORY READOUT AVAILABLE, and BROA, B MEMORY READOUT AVAILABLE, low at test points C and D. Since both memories are empty at this time, it is irrelevant which memory receives data first, hence the read-in flip-flop IC14 is in an indeterminate state with either A MEMORY READ IN ARI or B MEMORY READ IN BRI high at output pins 14 and 15. BRI is supplied to the memory select and interface module. BRI high would enable a set of drivers which supply the data to memory B. Once the first memory has received a complete record, or it is full, the input data is switched to the other memory. In addition, the filled memory starts reading out the data onto the tape following the required start delay. The switching is controlled by this module, as described below.

Either an EOR command from the interface, or a memory counter pulse XCTR1, indicating that a record is at the output of the memory, is used to effect a memory switch. When an EOR command is given, it is gated through NOR gate IC1-6 to NAND gate IC7-1. NAND gate IC7-2 is enabled only if the data in memory flip-flop IC17/IC12 is set by a preceding write command $\overline{\text{WCMD1}}$ (input pin R, supplied from the memory select and interface module), indicating that the memory contains data; this prevents two successive memory switches from occurring without any data having been received between them. When the data in memory flip-flop is set, its $\overline{Q}$ output low is supplied to lamp driver IC19, turning on the DATA IN MEMORY lamp on the front panel of the recorder. The Q output of the data in memory flip-flop enables IC7-2, gating the EOR command through IC7-3 to fire the first of the two IC16 one-shots, provided that $\overline{\text{BUSY}}$ is false. If $\overline{\text{BUSY}}$ is true, the memory switch is delayed, as described in the $\overline{\text{BUSY}}$ paragraph below, until $\overline{\text{BUSY}}$ goes false. The first IC16 one-shot generates a 6.6 μsec pulse whose trailing edge triggers the second IC16 one-shot, generating a 1.5 μsec pulse. The first of the two one-shots delays the execution of the EOR to allow the EOR command to be given simultaneously with the last character of the record. The 1.5 μsec pulse generated by the second one-shot is gated through NOR gates IC10-13 and IC15-12; this pulse will set the readout available flip-flop of the memory in the read-in state (as determined by either ARI or BRI true), and trigger the memory switch one-shot IC8. IC8 supplies a 4.8 μsec pulse, the trailing edge of which toggles the memory read-in flip-flop IC14, switching the next incoming block to the available memory by changing from ARI true to BRI true, or vice versa. A memory switch is also effected without an EOR command when the memory is filled to capacity. The memory counter of the filled memory issues a counter pulse, ACTR1 or BCTR1, at input pin E or P of this module. The pulse is gated through an edge circuit which supplies a 2 μsec pulse to the set input of the respective memory available flip-flop, one of the two IC10/IC20 flip-flops. The pulses are also output at pins K and N as $\overline{\text{ACTRP}}$ and $\overline{\text{BCTRP}}$ and are supplied to the memory readout control module. If we assume that A memory was reading in and was filled, then ARI is true and enables NAND gate IC10-1, allowing ACTR1 pulse to be gated through IC10-3 to set the A readout available flip-flop, setting AROA true at test point C. In addition, the ACTR1 pulse is gated through NAND gate IC10-3, activates NOR gate IC13-8, and fires memory-switch one-shot IC8. The Q output of the one-shot generates a 4.8 μsec positive-going pulse which is inverted by IC3-3, test point B going low, and disables READ OUT START 2 ROSRT2 for the pulse duration. The trailing edge of the pulse toggles the read-in flip-flop IC14. Since at this time $\overline{\text{AROA}}$ is true while BROA is false, the flip-flop toggles to set its Q output low, $\overline{Q}$ high. A MEMORY READ IN ARI then goes low while BRI goes high, indicating that memory B is available for read-in; this routes the next record to memory B. When AROA flip-flop is set, AROA high (test point C) enables NAND gate IC18-3. At this point $\overline{\text{ROCOMP}}$ false (high) enables IC18-4. Since memory B has yet to receive any data, BROA is false, enabling IC18-5; consequently IC18-6 goes low, setting the readout flip-flop IC5 and activating NOR gate IC4-8, which generates READ OUT START 2 ROSRT2 true at output pin L. As described above, ROSRT2 is delayed for the duration of the read-in switching delay by one-shot IC8. The 1-output of IC5 goes high, generating ROA true (high) at output pin F. ROSRT2 true is supplied to the tape motion control module where it generates a PROGRAM ADVANCE PADV to advance the program counter from the stage $\overline{Q_0}$ to $\overline{Q_1}$, initiating the start delay. Following the start delay, when the tape ramps up to normal speed, PADV goes true again advancing the program from Q_1 to Q_2, the readout state, in which memory A is read onto the tape. ROA true is supplied to Memory Readout Control Type 3517 module where it is used to reset the memory clock flip-flop, as described for that module. When the A memory has completed its readout, and the tape has come to a stop following the stop delay, a READ OUT COMPLETE pulse $\overline{\text{ROCOMP}}$ is supplied from the Tape Timing Control Module Type 3633 and is input at pin 22. $\overline{\text{ROCOMP}}$ is inverted by IC17-6 and is supplied to the clearing gates of the readout available flip-flops. Since we assume that memory A was read out, ROA true enables NAND gate IC15-5. $\overline{\text{ROCOMP}}$ is gated through IC15-6 to clear the AROA flip-flop, setting AROA false at test point C.

$\overline{\text{BUSY}}$

When both memories contain data available for readout simultaneously, no further data can be received from the interface until one of the memories has read out its data completely. When the data input rate from the interface exceeds the allowable rate, or when an error sequence occurs, both AROA and BROA go high and activate NAND gate IC18-1, 2, provided the gate is enabled by WRITE SELECT WSEL2 true at input pin Y. IC18-12 then goes low (test point E), producing $\overline{\text{BUSY}}$ true at output pin 17. On this module $\overline{\text{BUSY}}$ true disables the EOR delay one-shot IC16-2, preventing any memory switch from occurring in response to an EOR command. The memory switch is delayed until $\overline{\text{BUSY}}$ goes false. $\overline{\text{BUSY}}$ is also supplied to the memory select and interface module where it inhibits any WRITE COMMAND WCMD1 when true, thus inhibiting any data from being read into the memories. When one of the memories has completed its readout sequence and the tape has come to a stop, READOUT COMPLETE $\overline{\text{ROCOMP}}$ pulse is gated through inverter IC17-6 and clears the readout available flip-flop of the memory that was reading out. Thus either AROA or BROA goes false, setting $\overline{\text{BUSY}}$ false. This enables the EOR delay flip-flop IC16-2, allowing the next EOR command or counter pulse (ACTR1 or BCTR1) to switch the memory input. $\overline{\text{BUSY}}$ going false generates a pulse through IC7-6 which is routed through NOR gate IC13-8 to trigger the memory switch one-shot IC8, causing a memory read-in switch. For example, if AROA is still true while BROA has gone false, indicating that memory B has completed readout, BRI will go true and the incoming block will be supplied to memory B.

$\overline{\text{BUSY}}$ from this module is wire-OR'd with $\overline{\text{BUSY}}$ from the tape timing control module, which holds $\overline{\text{BUSY}}$ true when load point is detected or when an EOF command is given until either the load sequence or the end of file sequence is completed.

$\overline{\text{BUSY}}$ is gated through exclusive-OR gate IC2-6 with ZERO TRUE SELECT $\overline{\text{ZTSEL}}$ to give it the proper polarity, and is then output by driver IC3-11 (test point A) as $\overline{\text{BSY2}}$ to the interface where it may be used to inhibit any incoming data when true.

EOF DELAY CIRCUITRY

The purpose of the EOF delay circuitry on this module is to insure that the memories are emptied before an EOF sequence is carried out. An EOF command, given by the EOF pushbutton (input pin P) or by the interface (input pin W) sets the EOF flip-flop IC21/IC11, the 0-output of the flip-flop going low. If at this time neither memory contains any data available for readout, $\overline{\text{AROA}}$ and $\overline{\text{BROA}}$ false enable NAND gate IC11-2, 5. The 0-output of the EOF flip-flop low is inverted by IC6-6 and generates a 2 μsec pulse through IC1-12; the pulse sets flip-flop IC7/IC18, but at the same time it is gated through NOR gate IC1-6, as though it were an EOR command. What happens now depends on the state of the data-in-memory flip-flop IC17/IC12. If a memory switch has occurred, and no further data has been supplied by the interface, the file mark sequence is executed directly. This is accomplished as follows: the last memory switch, caused by the firing of one-shot IC8, sets flip-flop IC12/IC17 at IC12-5. The 1-output of the flip-flop goes high and clears the data in memory flip-flop IC17/IC12. The 0-output of this flip-flop in turn enables NAND gate IC12-10, gating the file mark pulse directly through NOR gate IC1-6 to clear flip-flop IC7/IC18 immediately after it was set. A delay is provided on NAND gate IC12-8 by capacitor C8 to ensure that the clearing pulse arrives after the setting pulse. The 0-output of the EOF delay flip-flop (IC18-8) goes high and activates NAND gate IC21/IC11. The 0-output of the flip-flop goes high, and generates a 2 μsec pulse through IC1-8 to be output as $\overline{\text{EOF2}}$ at output pin X. $\overline{\text{EOF2}}$ initiates the tape motion and the writing of the EOF on the tape timing control and tape motion control modules.

A different condition exists when there is data in the memories at the time of the EOF command. In this case the EOF flip-flop is not cleared immediately after setting, and the $\overline{\text{EOF2}}$ pulse is delayed. When there is data in the available for readout, indicated by either $\overline{\text{AROA}}$ or $\overline{\text{BROA}}$ true, the clearing gate to the EOF flip-flop (IC11-6) is disabled. In addition, when the EOF flip-flop is set, the pulse generated through IC1-12 sets flip-flop IC7/IC18, but the same pulse does not clear the flip-flop as before. Since data has been received from the interface, WRITE COMMAND $\overline{\text{WCMD1}}$ at input pin R has set flip-flop IC17/IC12 at IC17-12. The 0-output of the flip-flop goes low and disables NAND gate IC12-10, preventing flip-flop IC7-IC18 from being cleared, which in turn prevents the EOF delay flip-flop from generating EOF2. EOF2 is delayed until readout data is no longer available, indicated by both $\overline{\text{AROA}}$ and $\overline{\text{BROA}}$ false, which enables NAND gate IC11-2, 5. When readout has been completed and tape motion has ceased, READ OUT COMPLETE $\overline{\text{ROCOMP}}$ clears flip-flop IC7/IC18, which in turn clears the EOF flip-flop IC21/IC11 generating $\overline{\text{EOF2}}$ to start the actual writing of the EOF.

TYPE 3607 MEMORY COUNTER

CIRCUIT DESCRIPTION

This module performs the following functions:

a. Generates the memory clocks ACLK and BCLK used to toggle the memory and the memory counters

b. Contains the memory and EOR counter stages for buffers A and B

c. Generates WRITE SELECT WSEL4

d. Supplies PRESET pulse $\overline{\text{PST2}}$

e. Supplies the memory error output to the interface in recorders with the memory check option

MEMORY CLOCKS ACLK and BCLK

The memory clocks, used to toggle the memories and the respective memory counters, combine three distinct clocks during the write mode and three other clocks for the read mode. The read and the write clocks are basically similar with the order reversed. During a write operation the asynchronous input clock WRITE COMMAND $\overline{\text{WCMD1}}$ is supplied first as XCLK (X standing for either A or B) to strobe the input write data from the interface into the available memory. The pump clock PUCLK is supplied next as XCLK, shifting the data record to the output of the memory. The synchronous readout clock ROCLK2 is finally supplied as XCLK to strobe the data out of the memory at the preselected density and send it to the CRC register and the write buffer, to be transmitted to the tape transport. During the read mode the synchronous READ DATA STROBE $\overline{\text{RDS3}}$ is first supplied as XCLK, strobing the data into the buffer. Next the pump clock, in this case included in the INCREMENTAL READ CLOCK $\overline{\text{IRCLK}}$, pumps the read data to the output of the memory. Finally, the asynchronous read clock supplied from the interface as READ OUT ONE CHARACTER ROOC (later also incorporated as $\overline{\text{IRCLK}}$) is used to strobe the data out of the memories to the interface. A more detailed description of the memory clock generation follows.

During the write mode WRITE COMMAND $\overline{\text{WCMD1}}$, input at pin 7 from the Time Pulse Generator Type 3640 module, is inverted by IC18-3 and is gated through one of the two IC18 NAND gates. Assuming BRI is false at this time, meaning that memory A is reading in, BRI low is inverted by IC18-6 and enables the upper of the two IC18 gates, gating $\overline{\text{WCMD1}}$ through NOR gate IC23-11 as A MEMORY CLOCK ACLK. BRI high, indicating the memory B is reading in, would enable the lower IC18 NAND gate, and $\overline{\text{WCMD1}}$ would be gated through IC18-8 and IC23-8 as B MEMORY CLOCK BCLK. Either ACLK or BCLK then strobes the data into the memory until the memory is full or an EOR command is received. In either case $\overline{\text{WCMD1}}$ is terminated and START DELAY SRTD2 true is supplied from read control III module at input pin S. SRTD2 sets flip-flop IC7, the Q output of the flip-flop going high and enabling NAND gate IC1-10. PUMP CLOCK PUCLK, a crystal controlled frequency supplied from the time pulse generator module, is then gated through IC1-8, provided that WRITE SELECT WSEL3 is true at this time. PUCLK is then routed through NOR gate IC6-8 to one of the IC13 NAND gates. If BRI is true at this time, meaning that memory B is reading in data, PUCLK is gated through IC23-3 and is supplied as ACLK at output pin W, since memory A is no longer reading in. If BRI is false, PUCLK would be supplied as BCLK. When the data is shifted to the output of the memories, either $\overline{\text{ACTRP}}$ or $\overline{\text{BCTRP}}$ is supplied from the memory input control module at inputs R and L, respectively. Either counter pulse clears flip-flop IC7, terminating the pump clock. At this time $\overline{\text{Q}}$ output of flip-flop IC7 enables NAND gate IC6-5, WSEL enables the gate at IC6-4, gating READOUT CLOCK ROCLK2 (supplied from read control III at input pin 15) through IC6-6, IC6-8, and one of the two IC23 NAND gates, whichever one is enabled by the respective memory not reading in. ROCLK2 serves as the memory clock until all the data is read out of the memory.

During a read operation the order of the memory clock is reversed. When the data is initially read into the memory, READ DATA STROBE $\overline{\text{RDS3}}$, the synchronous read clock input at pin 6, is gated through NOR gate IC18-3 and is supplied as either ACLK or BCLK, as determined by BRI true or false. Once a whole block has been read from the tape to the memory, $\overline{\text{RDS3}}$ is terminated, INCREMENTAL READ CLOCK $\overline{\text{IRCLK}}$, input at pin 19, which combines the pump clock as well as the readout clock, is gated through NOR gate IC6-8 and through one of the two IC23 NAND gates, the one enabled by the memory not reading in. At this time $\overline{\text{IRCLK}}$ consists of the pump clock PUCLK2, which shifts the data to the memory's output. Once the data is at the memory's output and is framed, read control II module switches $\overline{IRCLK}$ from the pump clock to the asynchronous readout clock READ OUT ONE CHARACTER ROOC, which then strobes the data from the memory to the interface.

MEMORY COUNTERS

This module contains four nearly identical counters— a memory stage and an EOR stage for each memory. Each counter consists of divide-by-sixteen counters in series, and each has a capacity equal to twice that of the memory size. Consequently a memory of 512 bit capacity has 1024 bit counters. The counters are advanced by the MEMORY CLOCK, either ACLK or BCLK, as are the memory stages. When the data is initially read into the memory during either a write or a read mode, only the memory counter stage of the memory reading in is enabled, while the EOR stage associated with that memory is kept disabled by READOUT AVAILABLE XROA false (where X is either memory A or B, depending on which memory is reading in). When the memory has received a complete data record of N_r characters and an EOR command is issued by the interface, the memory clock is switched from the read-in clock ($\overline{WCMD1}$ during a write mode, $\overline{RDS3}$ during a read mode) to the pump clock, which shifts the data to the memory's output. When the pump clock is supplied as the memory clock, the EOR counter stage is enabled as well, and counts $N_m - N_r = N_p$ pulses, where N_m is memory bit size, N_r is the record size, and N_p the number of pump clock pulses supplied. When the data is shifted to the memory's output, the memory counter has counted $N_r + N_p = N_m$ pulses while the EOR counter has counted only the N_p pulses of the pump clock. At this time the memory counter stage issues COUNTER PULSE XTR1 (at output pin 1 or 22). This pulse is supplied to the memory input control module, where it sets the readout data available flip-flop, initiating the readout sequence by setting ROSRT2 true. The differentiated COUNTER PULSE XCTRP is also supplied to the memory counter module where it switches the memory clocks from the pump clock to the readout clock.

When valid data is present at the output of the memory stage, the output of the last flip-flop on the memory counter stage is high, since it has already counted $N_p = N_r = N_m$ pulses. At this time the output of the last flip-flop of the EOR counter stage is low. The outputs of the two counter stages of each buffer are supplied to exclusive-OR gates IC13-8 and IC13-11. When valid data is output by one of the memories, one of the two exclusive-OR gates is activated, supplying RECORD FRAME RFRMA or RFRMB true. RFRMX is kept true until the whole data record has been read out, at which point the output of the EOR counter stage goes high, setting RFRMX false, and indicating that the data is no longer valid.

RFRMA and RFRMB are supplied to read control II module where READ DATA AVAILABLE is generated, initiating the readout of data to the interface.

WRITE SELECT WSEL4

WRITE SELECT WSEL4, true when a write mode is selected, is gated with RO, the readout output of the program control counter (on the tape timing control module) and with DEVICE ENABLE DEN2, true when the transport is on line. These functions activate NAND gate IC11-6; the output of the gate is inverted by IC1-12 and is supplied at pin 16 as WRITE SELECT WSEL4. WSEL4 is supplied to the memory module, where it enables the write data output gates.

PRESET $\overline{PST2}$

When the power is first turned on, NOR gate IC4-6 is activated, its output is inverted by IC3-11 which supplies PRESET pulse $\overline{PST2}$ at output pin N. Capacitor C1 then charges up and disables IC4-3, terminating the pulse. The PRESET pulse is also generated when the interface issues INITIALIZE $\overline{INIT}$, input at pin K. $\overline{INIT}$ is differentiated and supplies a PRESET pulse through IC4-6 and IC11. $\overline{PST2}$ is used throughout the formatter to precondition a variety of functions.

MEMORY ERROR OUTPUT (OPTION)

Whenever a memory error is detected, $\overline{MEMER}$ goes true (low) at input pin 5, setting the D input of the memory error flip-flop IC10-2 low. The memory clock, $\overline{IRCLK}$ during a read mode or ROCLK2 during a write mode, is gated through NOR gate IC6-8 to clock the memory error flip-flop. If a memory error is detected, the $\overline{Q}$ output of the flip-flop goes high, enabling both IC9 NAND gates. The gates are not enabled until the data is framed, so that the memory error output will be synchronized with the valid data. If a memory error is detected in buffer A, the error output will be delayed until BRI is true, indicating the memory A is <u>not</u> reading in, and RECORD FRAME A RFRMA is true, indicating that buffer A is reading out valid data. Thus when an error is indicated, and both BRI and RFRMA are true, IC9-6 will go low, activating NOR gate IC9-8, test point A going high. The output of IC9-8 is gated with GATED DEVICE ENABLE DEN2 through NAND gate IC8-8, supplying the memory error indication $\overline{MEMER2}$ to the interface at output pin 11.

TYPE 3660 READ CONTROL III

CIRCUIT DESCRIPTION

This module performs the following read control functions:

a. Generates READ OUT ONE CHARACTER 2 ROOC2 from the input asynchronous read clock, or optionally, from a preselected crystal frequency

b. Gates the following functions: DEN3, WSEL3, RSEL3, LDPT2, ROSRT3, ROCOMP2, SRTD2, ROEN2, and ROCLK2

READ OUT ONE CHARACTER 2

READ OUT ONE CHARACTER $\overline{\text{ROOC}}$, the asynchronous read clock supplied from the interface (input pin W), is gated with ZTSEL to provide the proper polarity and is supplied to NAND gate IC6-10. If the READ OUT CONTINUOUSLY option is not used, flip-flop IC1 is cleared, and its $\overline{\text{Q}}$ output high enables NAND gate IC6-9. Consequently the ROOC pulses are gated through to NOR gate IC6-11, to be output as ROOC2 at pin 21. ROOC2 is supplied to read control II module where it is used to generate the INCREMENTAL READ CLOCK $\overline{\text{IRCLK}}$. A continuous read option is provided on this module as well. READ OUT CONTINUOUSLY $\overline{\text{ROC}}$ true at input pin X (supplied from the interface) is gated with ZTSEL, is inverted twice by a pair of IC11 inverters and sets the D input of flip-flop IC1-12 high. The 200 cpi crystal frequency MO200 (any other frequency may be ordered) is supplied to the clock input of the flip-flop, and the first pulse triggers the flip-flop, causing its $\overline{\text{Q}}$ output to go low and disable NAND gate IC6-9, inhibiting ROOC from being gated through. The $\overline{\text{Q}}$ output of flip-flop K1-9 goes high and enables NAND gate IC6-2, gating MO200 through IC6-3 and IC6-11 to be output as ROOC2. The crystal generated pulses are then used as the readout command, and the data is read out automatically at the preselected frequency.

WRITE SELECT 3, READ SELECT 3, AND OTHER FUNCTIONS

DEVICE ENABLE DEN3 is generated by combining ON LINE $\overline{\text{ONL}}$ from the tape transport with FORMATTER ENABLE $\overline{\text{FEN}}$ supplied from the interface. $\overline{\text{ONL}}$ is supplied at input pin 14, is inverted by IC8-6 and enables NAND gate IC9-1 whenever the transport is on line. $\overline{\text{FEN}}$ is input at pin V and is gated with ZERO SELECT TRUE ZTSEL through exclusive-OR gate IC2-3 and activates NAND gate IC9-3, provided that $\overline{\text{ONL}}$ is true. The output of the gate is inverted by IC8-12 and is output as DEVICE ENABLE 3 DEN3 at output pin 12. DEN3 preconditions almost all functions performed by the formatter. On this module it enables the rewind, read select, and write select gates as described below. When FEN3 goes true it enables IC3-2. When the interface selects a write operation, WRITE SELECT $\overline{\text{WSEL}}$ goes true at input pin T and is gated with ZTSEL to achieve the right polarity. It then activates NAND gate IC3-3 supplying WRITE SELECT 3 WSEL3 true at output pin P and WSEL3 true at output pin N. WSEL3 is used on this module as well as throughout the formatter to precondition the write functions. The inverse of $\overline{\text{WSEL}}$, output by inverter IC8-2, activates NAND gate IC3-13 whenever $\overline{\text{WSEL}}$ is false, provided that DEN3 is true, generating READ SELECT RSEL3 true at output pin R and RSEL3 true at output pin S. Thus, whenever DEVICE ENABLE 3 is true either WSEL3 or RSEL3 must be true, and the transport is in either a read or a write mode. If the interface selects a write mode, WSEL3 goes true; otherwise RSEL3 is true. A variety of other functions are gated with the above three on this module. Thus GATED REWIND REW2, input at pin 13 from the memory input control module, is conditioned by DEN3 and is output as REW3 at output pin Z. LOAD POINT $\overline{\text{LDPT}}$ from the transport is inverted by IC10-12 and is then conditioned by WSEL3 to generate $\overline{\text{LDPT2}}$ at output pin A. $\overline{\text{ROSRT2}}$ is conditioned with WSEL3 to supply ROSRT3 during a write mode to the tape motion control module. $\overline{\text{ROSRT4}}$, supplied only during a read mode. is also gated through NOR gate IC9-6 and is output as ROSRT3 at output pin Y. READ OUT COMPLETE pulse ROCOMP supplied by the tape timing control module is gated with WSEL3 to generate $\overline{\text{ROCOMP2}}$ at output pin Y, which is then supplied to the tape motion control and the memory input control modules to generate the memory counter reset pulses and to clear the readout data available flip-flops. During a read mode $\overline{\text{ROCOMP}}$ is gated with RSEL3 and is gated through NOR gate IC4-8 to the output as SRTD2. SRTD2 is supplied to the memory counter module where it switches the memory clock to the pump clock during a write operation. WSEL3 is also used to condition READOUT ENABLE ROEN and READOUT CLOCK ROCLK, supplying ROCLK2 to the memory counter module and ROEN2 to the tape timing control module during a write mode.

TYPE 3618 READ CONTROL II

CIRCUIT DESCRIPTION

This module performs the following read control functions:

a. Generates INCREMENTAL READ CLOCK $\overline{\text{IRCLK}}$
b. Supplies READ OUT COMPLETE pulse ROCOMP2
c. Supplies READ END OF RECORD indication $\overline{\text{REOR3}}$ to the interface
d. Performs the HOLD function
e. Generates READOUT START 4, to keep the transport in forward motion
f. Supplies additional READ END OF RECORD REOR following end of tape, 25 feet of blank tape, and optionally every file mark
g. Generates FORMATTER RESET $\overline{\text{FREST}}$

INCREMENTAL READ CLOCK GENERATION

INCREMENTAL READ CLOCK $\overline{\text{IRCLK}}$, generated on this module, is used during the read mode as the memory clock ACLK or BCLK on the memory counter module. $\overline{\text{IRCLK}}$ combines two distinct clocks — PUMP CLOCK 2 $\overline{\text{PUCLK2}}$ and READOUT ONE CHARACTER 2 ROOC2. The pump clock is used to pump the read data to the output of the buffer before the data is read out, while ROOC2 is used to strobe the data asynchronously from the buffer to the interface.

$\overline{\text{PUCLK2}}$ input at pin 21 is supplied from the time pulse generator type 3640; it is generated by gating PUCLK with ROSRT2, supplying the pump clock whenever one of the memories has data available for readout. $\overline{\text{PUCLK2}}$ is supplied to pin 2 of NAND gate IC11. The counter consisting of the two IC12 flip-flops eliminates the first two pump pulses, allowing the clock to be synchronized with the data. NAND gate IC11-1 is kept enabled until the read data is pumped to the output of the memory and becomes valid. Until then the pump clock is gated through IC11-12, NOR gate IC16-6, and NAND gate IC11-8 to be output as $\overline{\text{IRCLK}}$ at pin 22 to the memory counter module. Once the data is shifted to the buffer's output, the pump clock is inhibited. If memory A contains the data, READ OUT DATA AVAILABLE AROA (from the memory input control module, input pin T) enables NAND gate IC3-4. At this time READ OUT MEMORY B ROB (also from the memory input control module, input pin R) must be false, enabling IC3-5. When the valid read data is at the output of the memory, RECORD FRAME A RFRMA goes true (input pin S, from the memory counter module) activating the gate, IC3-6 going low. NOR gate IC7-3 is then activated, its output is inverted by IC11-6, disabling NAND gate IC11-12 and inhibiting the pump clock. The same sequence occurs when memory B contains the readout data.

When either memory contains valid data available for readout, NOR gate IC7-3 is activated, its output enabling NAND gate IC5-2 and triggering one-shot IC17. READ SELECT 3 RSEL3 enables the gate at IC5-13. NAND gate IC5 is then activated; following a delay of approximately 13 μsec (provided to allow for memory switching) IC5-12 goes low, is inverted by the two IC1 inverters, and is output as READ DATA AVAILABLE RDVAL at pin U to the interface. Once RDAVL goes true, the interface can start supplying the readout clock. The readout clock is supplied to this module as READ OUT ONE CHARACTER 2 ROOC2 from read control III module at input pin W. ROOC2 is supplied to the first of the two IC6 one-shots, which is enabled at this time by RDAVL true. The Q output of the one-shot outputs a pulse, approximately 2 μsec in duration, which is gated with READ SELECT RSEL3 and is output as READ DATA STROBE to the interface. The pulse output by the $\overline{Q}$ output of IC6-4 is supplied to the next IC6 one-shot, triggering it on its trailing edge. The Q output of the second flip-flop then generates a 1 μsec pulse following each readout command. This pulse is gated with the output of NOR gate IC7-3 (which is high whenever there is valid data available for readout by either memory) and is gated through IC16-6 and IC11-8 to be output as $\overline{\text{IRCLK}}$ at pin 22. As mentioned above, $\overline{\text{IRCLK}}$ is used as the memory clock, strobing the data from the memory to the interface.

$\overline{\text{REOR3}}$ and $\overline{\text{ROCOMP2}}$

During a read operation when a complete block of data has been read out of the memories, one of the memory EOR counters issues either EORA or EORB, input at pin L or M of this module. EORX triggers one of two IC8 one-shots, which generates a 2 μsec pulse to one of the two IC13 NAND gates, whichever is enabled by either ROA or ROB true. The $\overline{Q}$ output of flip-flop IC12-8 is high, since counter IC12 has been cleared by IC11-6 low (RDAVL true). The 2 μsec pulse (generated by the EORX one-shot) is then gated through NAND gate IC2-8, provided that RSEL3 is true, and is supplied as READ END OF RECORD 3 REOR3 at pin 20 to the interface.

The EORX pulse is also gated through IC7-8, provided that HOLD is false, and is output as READ OUT COMPLETE pulse ROCOMP2. ROCOMP2 is supplied to the memory input control and the memory timing control modules; it is used to reset the data available flip-flops and to generate the memory counter reset pulses.

HOLD

This function may be especially useful in data communication applications where an error is detected during transmission and the block is to be retained in the memory. When HOLD goes true (from the interface input pin 12) it inhibits ROCOMP2 from being generated, preventing the memory counter reset pulses from being issued. This retains the data in the memory. When HOLD is returned to a false state it triggers one-shot IC9 which then generates a 2 μsec pulse through IC7-6 and IC2-11 to be used as ROCOMP2.

READOUT START 4

During a read mode, the transport continuously searches for data until one of the following conditions is met: 1) both buffers are filled; 2) end of tape is detected; 3) 25 feet of blank tape have been read; 4) a STOP command is issued; 5) optionally, an end-of-file tape mark has been detected. When none of the above conditions is true, NAND gate IC19-6 is kept activated, generating ROSRT4 true at output pin 1. ROSRT4 is supplied to the read control III module, which in turn supplies it to the tape motion control module, where it generates PADV true, preventing the main program control counter from returning to the REST state. When any of the above conditions is met, NAND gate IC19-6 is disabled, and ROSRT4 goes false. Thus when both buffers contain data available for readout, AROA and BROA true activate NAND gate IC20-6, disabling IC19-1. When end of tape is detected, EOT goes true (input pin 5, supplied from the transport) and sets flip-flop IC15. The 0 output of the flip-flop then activates NOR gate IC20-3, enabling NAND gate IC10-13. When the file mark is read after the EOT, RTM1 true at input pin E from read control I module is inverted by IC10-6 and activates IC10-11, disabling the ROSRT4 gate at IC19-4. When the STOP ON FILE MARK option is used, STPEOF true at input pin 2 (supplied from the interface) activates NOR gate IC20-13, enabling IC10-13; the gate is activated by READ TAPE MARK RTM1 true whenever a file mark is read, inhibiting ROSRT4. A counter consisting of divide-by-sixteen ICs 21, 22, 23, and 24 connected in series is used to detect 25 feet of blank tape. Whenever the transport is searching for data, SYNCHRONOUS FORWARD COMMAND SFC true at input pin Y enables NAND gate IC16-10. The counter is advanced by MASTER OSCILLATOR frequency MO2001 (supplied at pin Z from the time pulse generator module) which effectively divides each inch of tape into 200 increments, regardless of the data density or tape speed. When 25 feet of blank tape have been read, NAND gate IC19-8 is activated, clearing flip-flop IC18; the 1 output of the flip-flop goes low and disables IC19-5, inhibiting ROSRT4. When a STOP command is issued from the interface at input pin 6, flip-flop IC15-1 is set; the 0 output of the flip-flop goes low and disables IC19-2, again inhibiting ROSRT4.

READ END OF RECORD REOR

The REOR indication supplied from this module is wire-OR'd with the REOR2 output of the gap detector located on the tape timing control module. When READ GAP RGAP (input at pin B, supplied from the tape timing control module) is false, indicating that the gap detector has not detected an interrecord gap, it is inverted by IC10-3 and enables NAND gate IC5-10. The gate is also enabled by READ SELECT RSEL3. If END OF TAPE EOT is detected followed by a file mark RTM1, NAND gate IC10-11 is activated, as described above; this activates NOR gate IC14-10, activating NAND gate IC5-8, and issuing REOR true at output pin A. Similarly, if the STOP ON FILE MARK option is used, NAND gate IC10-11 is activated whenever a file mark RTM1 is detected, causing REOR to go true. In addition, after 25 feet of blank tape have been read, flip-flop IC18-1 is cleared, its 1 output goes low and activates NOR gate IC14-8, and an REOR indication is issued. Thus REOR is issued following end of tape, 25 feet of blank tape, and optionally after any file mark has been detected. REOR initiates the end-of-record sequence on the memory input control and read control I modules.

FORMATTER RESET FREST

The preset pulse PST2 is supplied from the memory counter module to NOR gate IC14-3, is inverted twice to generate FORMATTER RESET FREST. In addition, whenever load point is detected, LDPT goes true at input pin H and activates IC14-6, generating FREST true. One-shot IC9 holds FREST true for approximately 14 milliseconds after LDPT has gone false. Thus FREST is generated whenever the power is first turned on, whenever the INITIALIZE is used (both combined in PST2), and whenever load point is detected. FREST is used to preset the flip-flops on this module, as well as throughout the formatter.

TYPE 3817 READ CONTROL I

CIRCUIT DESCRIPTION

This module performs the following read control functions:

a. Detects the file mark

b. Generates PROGRAM ADVANCE PADV2

c. Generates the read stop delay

d. Generates the READ END OF RECORD indication to the interface following a good block and controls read backspace on error

e. Generates memory counter reset pulses $\overline{\text{ARST}}$ and $\overline{\text{BRST}}$ after an erroneous block has been read

f. Supplies the gated data strobe $\overline{\text{RDS3}}$

FILE MARK DETECTION

The deskewed read data channels $\overline{\text{RDTAP}}$ through $\overline{\text{RDTA7}}$, supplied from the Read Skew Delay Type 3641 module, are decoded by a gating system consisting of ICs 3, 4, 8, 9, and 14. When SEVEN TRACK TAPE UNIT TS7TR (input at pin 13 from the tape transport) is true, indicating that a seven-track unit is used, the decoding is adjusted to read the seven-track file mark. When a file mark character is read NAND gate IC9-8 is activated, its output going low. Since a file mark character may be a valid data character within the block, it is necessary to distinguish between the real file mark and a data character which happens to be identical to it. Thus when NAND gate IC9-8 is activated it disables NAND gate IC13-4. During a valid data block IC13-4 is enabled, gating READ DATA STROBE RDS1 through IC13-6 to set flip-flop IC6 at pin 10. If a block contains nothing but file mark characters, which should be true only for the real file mark, NAND gate IC13-4 is kept disabled throughout the block and flip-flop IC6-10 is <u>not</u> set. The $\overline{\text{Q}}$ output of the flip-flop then remains high, enabling NAND gate IC22-1 and setting the D input of flip-flop IC6-2 high. When DATA END DEND goes true at the beginning of the gap (as described in the read delay paragraph) it activates NAND gate IC22-3, supplying TAPE ERROR INHIBIT $\overline{\text{TERI}}$ at output pin Z. $\overline{\text{TERI}}$ is supplied to the tape timing control module and inhibits the error detection circuits while the file mark is being read. When a read gap is detected after a real file mark was read, RGAP goes true and toggles flip-flop IC6-3. The Q output of the flip-flop IC6-5 sets the D input of both IC11 flip-flops high while its $\overline{\text{Q}}$ output sets READ TAPE MARK $\overline{\text{RTM1}}$ true at output pin W. $\overline{\text{RTM1}}$ is the initial tape mark indication and is supplied to read control II to initiate the ramp down following the file mark. However, the second tape mark indication $\overline{\text{REOF}}$, supplied to the interface, is delayed until it is resynchronized with the data. Since the data stored in the memory is read asynchronously by the interface, the file mark indication must be delayed until the memory has been read out completely. The storing of the file mark is accomplished by the D type flip-flops IC6-5, IC11-12, and IC11-2, and two IC21 NAND gates. As described above, the file mark indication is first stored at the output of IC6-5, hence at the input of the IC11 flip-flops. It is not transferred to the output of the IC11 flip-flops until either ARI or BRI switch to a true state, which occurs when a memory is empty and available for read-in. The sequence may be explained as follows: When a file mark is detected, it is also supplied to one of the two memories, whichever is reading in, as determined by either ARI or BRI true. If the file mark is read into memory A, ARI has to be true at this time. Memory B may have data available for readout to the interface at this time. The data is then read out asynchronously from memory B until the memory is empty. If the data is correct, then ROCOMP is issued and memory B becomes available for read-in, BRI going true. This clocks flip-flop IC11-11, the Q output of the flip-flop going high. Recall, however, that memory A contains the file mark. When memory A is ready to be read out, meaning that the file mark is at the output of the memory, ROA goes true, and only then is NAND gate IC21-6 activated by ROA true, and issues READ END OF FILE $\overline{\text{REOF}}$ true (output pin 17) to the interface. $\overline{\text{REOF}}$ is then delayed until both memories are empty.

GENERATION OF READ STOP DELAY

During a read operation, RO true at input pin 6 from the tape timing control module enables NAND gate IC10-4. When no read data strobes are received by the read gap detector on the tape timing control module, $\overline{\text{REOR}}$ true (input pin K) is issued and sets the data end flip-flop IC13. The 1 output of the flip-flop goes high, generating DEND true and activating NAND gate IC10-4. This direct sets flip-flop IC18-10, enabling NAND gate IC15-13. Since this is a read operation, RSEL2 true enables IC15-10. On the tenth count of the interrecord gap, the gap detector on the tape timing control module issues RGAP true at input pin 8. This clears the data end flip-flop and, after being inverted, enables IC15-9, gating MO2001 clock to the read stop delay counter IC25. When the counter reaches the count of 8, equivalent to 0.04 inch of tape after the read gap has been detected, it activates NAND gate IC22-11, provided that both $\overline{REST}$ and $\overline{BSP}$ are false (indicating that this is an actual read operation). NAND gate IC22-11 then goes low, issuing $\overline{STPFD}$ true at output pin 11. This returns the program control counter to the $\overline{REST}$ state, initiating the tape rampdown.

READ ERROR BACKSPACE CONTROL

When a read error is detected, the recorder automatically backspaces over the erroneous block and rereads it. The number of times the block is reread can be determined by setting straps 1, 2, or 3 to be 2, 4, or 8 times, respectively. If the error is still detected after the last reading, a permanent error indication, READ BLOCK IN ERROR $\overline{RBIE}$, is issued. The read backspace control operates as follows: Each time an error is detected the tape timing control module causes the transport to backspace over the erroneous block. Each time the transport backspaces BSF true, input at pin A from the tape timing control module clocks the divide-by-sixteen counter IC24. Depending on the count for which the counter is strapped, after the final desired backspace operation one of the counter outputs enables NAND gates IC14-13 and IC22-5, while setting the D input of flip-flop IC18 high. At this time SRTD true has cleared flip-flop IC17, its $\overline{Q}$ output going high; this activates NAND gate IC22-6, causing TAPE ERROR INHIBIT $\overline{TERI}$ to go true. $\overline{TERI}$ is supplied to the tape timing control module to prevent any further error detection. After the read stop delay $\overline{STPDF}$ true activates NAND gate IC14-11, and after being gated through NOR gate IC14 and IC5-2 is output as $\overline{STPDF2}$ at output pin 7. $\overline{STPDF2}$ is supplied to the tape motion control module where it causes READ OUT COMPLETE PULSE ROCOMP to be generated, terminating the read sequence for the erroneous block. The permanent read error indication is delayed until it is resynchronized with the data. After the final rereading of the erroneous block the D input of flip-flop IC18-2 is set high by the reread counter. When the read gap is detected, RGAP true toggles the flip-flop, causing its Q output to go high. The actual error indication, however, has to be delayed until it coincides with the data as it is read out to the interface. This is accomplished by flip-flops IC16 and NAND gates IC21 in the same manner as the file mark is synchronized with the data, as described in the file mark detection paragraph. When the erroneous block is actually read out, $\overline{RBIE}$ goes true, indicating READ BLOCK IN ERROR to the interface.

PROGRAM ADVANCE 2

PROGRAM ADVANCE 2 is used to advance the program control counter on the tape timing control module from one operation state to the next. During the write operation PADV supplied from the tape motion control module at input pin X is gated with DEVICE ENABLE, and is gated through NOR gate IC1-8 to be output as PADV2. However, additional program advance commands for the read operation are generated on this module. BACKSPACE FLIP-FLOP $\overline{BSF}$ is supplied from the tape timing control module at input pin A, and is gated with PADV to set flip-flop IC19-13. The 0 output of the flip-flop goes low and activates NOR gates IC19-6 and IC19-3. These in turn activate NAND gate IC23-6, provided that RSEL2 is true, and hold PADV2 true until flip-flop IC19-9 is cleared by the $\overline{REST}$ state. This causes the program control counter on the tape timing control module to jump over state Q7, which is used during the write operation, and to go directly to the $\overline{REST}$ state following a read backspace. An additional program advance is generated by gating DATA END DEND and READ OUT RO. After a block is read out, it provides an additional program advance command to keep the tape moving forward until the read stop delay is completed. When $\overline{STPDF}$ goes true on this module, the program control counter is direct cleared and returns to the $\overline{REST}$ state until the next block is read.

READ END OF RECORD AND MEMORY COUNTER RESET PULSES

On the tenth character space of the interrecord gap, the gap detector on the tape timing control module supplies $\overline{RGAP}$ true at input pin 8 of this module, clearing the DATA END flip-flop IC13. The 0 output of the flip-flop goes high and triggers one-shot IC20, which generates a 2 μsec pulse on its Q output (test point A). During a read operation, if the block just read was good, $\overline{ROSRT1}$ (input pin U, supplied from the tape timing control module) is false, enabling NAND gates IC23-13. READ SELECT RSEL2 enables IC23-2, and the pulse generated by IC20 is gated through to the interface as READ END OF RECORD $\overline{REOR2}$ at output pin 22. On the other hand, if the block just read is in error, $\overline{ROSRT1}$ is true and inhibits IC23-13. $\overline{ROSRT1}$ true is inverted by IC2-4 and enables the two IC12 NAND gates. These gates are also enabled by RSEL2. If the block just read was supplied to memory A, ARI true (input pin 9, supplied from the memory input control module) enables the upper of the two IC12 gates. If memory B has just received the block, ARI false is inverted by IC5-6, enabling the lower IC12 gate. In either case, the pulse generated by IC20 on the tenth character of the interrecord gap is gated through as either A MEMORY COUNTER RESET $\overline{ARST}$ or B MEMORY COUNTER RESET $\overline{BRST}$. $\overline{XRST}$ is supplied to the memory counter module where it resets the counter of the memory that contains the erroneous block, in effect erasing the data from that memory. The recorder then rereads the block until it is read correctly, or until a permanent read error indication is issued.

GATED READ DATA STROBE $\overline{RDS3}$

During a read mode, when a block is being read from tape to the memory, RSEL2 true enables IC15-5 and RO (the READ OUT state of the program control counter) enables IC15-1. During the actual data the DATA END flip-flop IC13 is in a cleared state, hence its 0 output enables IC15-4. The READ DATA STROBE $\overline{RDS}$, supplied from the tape transport, is then inverted by IC2-2 and gated through IC15-6 to output pin 10 as $\overline{RDS3}$. $\overline{RDS3}$ is supplied to the memory counter module where it is used as the read-in clock during the memory cycle, strobing the read data into the memory.

TAPE TIMING CONTROL TYPE 3633

CIRCUIT DESCRIPTION

This module performs the following format control and error check functions:

a. Controls the tape formatting using a main program control counter.

b. Generates the start, stop, erase, beginning of tape, and end of file delays.

c. Provides the write clock $\overline{WCLK}$ and readout clock ROCLK.

d. Contains read-after-write error check circuitry, including a read gap detector, an LRC register, and a parity tree.

PROGRAM CONTROL COUNTER

The program control counter consists of divide-by-sixteen counter IC29 in tandem with binary to octal decoder IC23. There are eight program states, $\overline{Q}_0$ through $\overline{Q}_7$, as tabulated below.

Initially the program control counter is in the $\overline{REST}$ state, in which no tape motion occurs. When one of the memories is filled and has data available for readout, the memory input control module supplies ROSRT2 true to the tape motion control module. That module in turn generates the first PROGRAM ADVANCE PADV true at input pin W. PADV true enables NAND gate IC21-1, gating ROTP1 (input pin X) through IC21-3 to the clock input of the program control counter, advancing it from $\overline{Q}_0$ to $\overline{Q}_1$. $\overline{Q}_1$ low is inverted by IC28-10 and enables the start delay gate IC24-1, direct clears the LRC register, and is also output as START DELAY SRTD at output pin H. SRTD is supplied to the memory readout control module to switch the memory clock. During this time, the tape motion control module supplies a SYNCHRONOUS FORWARD COMMAND SFC to the transport, initiating the tape ramp up. Following the start delay, the start delay gate is enabled (as described in the delay counter paragraph below) and issues $\overline{SRTDF}$ true at output pin 1. This causes the next PADV to be generated on the tape motion control module, advancing the program counter to $\overline{Q}_2$, the readout state. $\overline{Q}_2$ low is inverted by IC28-12, supplying RO true at output pin K and enabling NAND gate IC22-9. IC22-10 is enabled by READOUT ENABLE ROEN at input V from the memory readout control module, and READOUT TIME PULSE ROTP1 is gated through IC22-8 to set the readout flip-flop IC27. The 1-output of the readout flip-flop goes high and enables NAND gate IC3-13. DEVICE ENABLE DEN2 enables IC3-1, gating ROTP2 through IC3-12 to output pin S as the write clock $\overline{WCLK}$. $\overline{WCLK}$ is supplied to the CRC control module, from where it is supplied to the CRC

	Output of Program Counter	Function Performed	
	Q_0	REST	Tape is stationary
	Q_1	SRTD	Start delay, tape ramps up to speed
	Q_2	RO	Read out, one of the memories is read onto tape
	Q_3	CRC	The CRC character is written on tape
	Q_4	LRC	The LRC character is written on tape
	Q_5	STOP DELAY	The stop delay gate is enabled if no error is detected
only during error sequence	Q_6	BSP	Tape backspaces over erroneous block
	Q_7	ERASE DELAY	Erase delay gate is enabled, erroneous block is erased

register to toggle the register flip-flops and to the write amplifier modules. The 1-output of the readout flip-flop also enables NAND gate IC3-5, gating ROTP3 through to output pin R as READOUT CLOCK ROCLK. ROCLK is supplied to the memory readout control module to become the memory clock during the readout of the memories. When the memory has completed the readout of a block, the tape motion control module issues the next PROGRAM ADVANCE PADV, advancing the program control counter to $\overline{Q}_3$, the CRC state. $\overline{\text{CRC}}$ true is supplied to the tape motion control module, where the formatting of the CRC character is controlled. After the CRC character is written, PADV goes true and advances the program to $\overline{Q}_4$, the LRC state. LRC is supplied to the tape motion control where an additional PADV is generated, moving the program to $\overline{Q}_5$. $\overline{Q}_5$ is inverted by IC28-6 and enables the stop delay gate. The gate is activated following the stop delay, issuing $\overline{\text{STPDF}}$ true at output pin 12 to the motion control module in order to generate the next PADV. The output of the stop delay gate is also inverted by inverted IC21-10 and enables NAND gate IC21-10. If the data block is good and no error is detected, the output of the error flip-flop IC6-9, $\overline{\text{ROSRT1}}$, is false (high). In that case IC21-11 goes low and sets the readout complete flip-flop IC22/IC26. The 1-output of the flip-flop goes high and enables NAND gate IC16-5 while the 0-output of the flip-flop direct-clears the main program control counter at IC29-2, returning it to the $\overline{\text{REST}}$ state. This causes the tape to ramp down to a stop and completes the readout cycle. When the tape is stationary TAPE RUNNING $\overline{\text{TRNG}}$, supplied from the ramp generator module, goes false at input pin J and activates NAND gate IC16-6, supplying $\overline{\text{ROCOMP}}$ true at output pin 21 to the memory input control and tape motion control modules. $\overline{\text{TRNG}}$ also gates ROTP3 through NAND gate IC26-3 to clear the readout complete flip-flop, terminating $\overline{\text{ROCOMP}}$ after a short delay.

A different condition exists when an error is detected by the read-after-write circuits on this module. In that case the error flip-flop IC6-9 is set by either an LRC or a VRC error, READOUT START 1 $\overline{\text{ROSRT1}}$ going low. $\overline{\text{ROSRT1}}$ low disables NAND gate IC21-12, preventing the readout complete flip-flop from being set. $\overline{\text{ROSRT1}}$ is also supplied to the memory input control module where it generates ROSRT2; ROSRT2 in turn generates another PADV, advancing the program advance counter to $\overline{Q}_6$ $\overline{Q}_6$ low supplies $\overline{\text{BSP}}$ true at output pin E and to the read gap detection circuits. $\overline{\text{BSP}}$ is supplied to the tape motion control module to activate the SYNCHRONOUS REVERSE COMMAND gate, causing the tape to backspace over the erroneous block. It is also inverted by IC5-3 on this module and enables NAND gate IC5-4; IC5-6 is activated by the gap detect counter on the tenth count of the interrecord gap preceding the erroneous block. IC5-6 low sets the backspace flip-flop IC5, generating $\overline{\text{BSF}}$ true at output pin A. $\overline{\text{BSF}}$ is supplied to the tape motion control module to generate the next PADV, moving the program control counter from $\overline{Q}_6$ to $\overline{Q}_7$, terminating the backspace and initiating the erase delay. $\overline{Q}_7$ low clears the backspace flip-flop IC5; in addition, it is inverted by IC28-4 and enables the erase delay gate IC30-5. At this time the transport is erasing a length of tape equivalent to the longest block capacity of the memories. At the end of the erase delay, IC30-6 goes low, initiating another start delay SRTDF at output pin 1. The program control counter proceeds to state $\overline{Q}_1$ and starts rewriting the erroneous block. This process is repeated until the block is written correctly on tape.

DELAY COUNTER

The delay counter consists of three divide-by-sixteen counters in tandem: ICs 19, 20, and 25, in addition to four delay gates: start delay, stop delay, erase delay, and file mark and BOT delay gates. The counter is reset each time PADV is generated; thus it starts counting from 0 each time the program status changes. The delay counter is clocked by master oscillator frequency MO2001 at input pin 7. MO2001 is the 200 cpi frequency gated with $\overline{\text{REST}}$, and is supplied only when the tape is in motion. MO2001 effectively divides each inch of tape into 200 increments regardless of the data density and tape speed, so that the delays are equal for all densities and speeds. The start delay gate, IC24-6, is enabled when the main program control counter advances from the $\overline{\text{REST}}$ state to $\overline{Q}_1$; it is activated on the 84th count after the tape has advanced 0.2325 inch, supplying $\overline{\text{SRTDF}}$ true to advance the program counter to the RO state. The stop delay gate IC24-8 is enabled when the program control counter is in $\overline{Q}_5$; it is activated on the 40th count in nine-track recorders and on the 72nd count in seven-track recorders, during which the tape travels 0.200 inch and 0.360 inch respectively.

The stop delays vary in order to account for the difference in read-write head spacing in seven-track and nine-track recorders; in nine-track recorders the spacing is 0.15 inch while in seven-track it is 0.30 inch. The erase delay gate is enabled when the counter is in the $\overline{Q}_7$ state. The length of the erase delay varies according to the buffer size of each recorder so that the length of tape erased is equivalent to the longest block that can be accepted by the particular buffer. The erase delays for the various buffer sizes and the respective lengths of tape erased are tabulated below.

ERASE DELAY

Buffer Size	Delay Count	Length of Tape Erased (inches)
512	264	1.32
1024	520	2.60
2048	1032	5.16

The file mark and beginning of tape delays are both set by the same gate — IC30-8. When LOAD POINT $\overline{\text{LDPT}}$ goes true at input pin Y, indicating that load point was detected, flip-flop IC22/IC27 is set; the 1-output of the flip-flop is inverted by IC28-2 and holds $\overline{\text{BUSY}}$ true at output pin L, inhibiting any data from being received during the BOT sequence. The 1-output of the EOF-BOT flip-flop also enables the EOF-BOT delay gate IC30-12. The 0-output of the flip-flop direct sets the program control counter IC29, setting the counter at $\overline{Q}_7$ true. $\overline{Q}_7$ low is inverted by IC28-4 and enables the erase delay gate IC30-5, but the erase mode is prevented by the 0-output of the EOF-BOT flip-flop which inhibits IC30-2. Since $\overline{Q}_7$ is true, SFC is kept true on the tape motion control module, and the tape is advanced forward as required for the BOT gap. The 0-output of the EOF-BOT flip-flop also clears error flip-flop IC6, inhibiting any error detection. On the count of 768, after a gap of 3.84 inches, the EOF-BOT delay gate is activated, supplying $\overline{\text{SRTDF}}$ true at output pin 1 to the tape motion control module. PADV is then generated, which clears the EOF-BOT flip-flop through NOR gate IC26-11, inverter IC21-4. A similar sequence occurs when the EOF command $\overline{\text{EOF2}}$ is received at input pin 20 from the memory input control module. It also sets flip-flop IC22/IC27, and the EOF gap is generated in an identical manner to the BOT gap.

READ AFTER WRITE CIRCUITRY

The read after write circuits on this module include a read-gap detector, and VRC and LRC error detection circuits. The read-gap detector consists of divide-by-sixteen counter IC14 and associated gating. When a block of data is read, $\overline{\text{RGAP}}$ false enables NAND gate IC15-4 and ROTP1 is gated through to the clock input of the counter. However, READ DATA STROBE RDS, input at pin 16 from the read amplifier/skew delay module, is gated through IC10-3, since flip-flop IC10/IC15 is initially cleared. RDS then clears the gap counter during each data character. During the interrecord gap, RDS is no longer generated, and the gap counter keeps counting. On the count of three NAND gate IC15-12 is activated, provided that $\overline{\text{BSP}}$ is false; IC15-12 goes low and sets flip-flop IC10/IC15, inhibiting any succeeding RDS pulses (corresponding to the check characters) from clearing the gap counter. The counter keeps counting and on the count of 10 activates IC10-11, generating the LRC CHECK pulse. On the count of 12 IC10-8 is activated, generating READ GAP $\overline{\text{RGAP}}$ true at output pin F, disabling NAND gate IC15-4 and locking the counter. The gap detector is also used to detect the gaps when the tape backspaces during an error sequence. In that case BSP true inhibits IC15-2, and flip-flop IC10/IC15 is not cleared, so that any RDS pulses can clear the gap counter. On the tenth count of the interrecord gap <u>preceding</u> the erroneous block, IC10-11 is activated, and sets the backspace flip-flop IC5. $\overline{\text{BSF}}$ goes low and is output at pin A to the tape motion control module where it generates a PROGRAM ADVANCE PADV, terminating the backspace.

The read data channels $\overline{\text{RDTA0}}$ through $\overline{\text{RDTAP}}$, supplied from the read amplifier modules, are inverted by ICs 7 and 9 and supplied to parity check IC8. In seven-track recorders, odd or even parity can be selected by SELECT ODD PARITY PSELO. If PSELO is low, it is inverted by IC9-4 and enables the even input of the parity tree; otherwise odd parity is selected. In nine-track recorders only odd parity is used. If a vertical parity error is detected IC8-6 goes high and enables IC16-9, gating the gated read data strobe RDS2 through IC16-8 to set the error flip-flop IC6-10. $\overline{\text{ROSRT1}}$ then goes low and initiates the error sequence as described above.

The LRC error detection circuits consist of a data register including a set of nine J-K flip-flops IC6, IC11, IC12, IC13, and IC18. (In seven-track recorders IC13 is omitted.) The read data input $\overline{\text{RDTA0}}$ through $\overline{\text{RDTAP}}$ is inverted and supplied to the J-K inputs of the flip-flops, so that each flip-flop is toggled to the opposite state whenever a logic 1 is present on the associated input line. The register is shifted once for each data character by the READ DATA STROBE RDS from the read amplifier/skew delay card at input pin 16. The $\overline{Q}$ outputs of the nine flip-flops are connected to NOR gate IC17, which enables NAND gate IC16-12 whenever one or more of the $\overline{Q}$ outputs is low. When all data characters in a block, the CRC character, and the LRC character have been shifted through the LRC register, all flip-flops will be in clear condition (all zeros) if no error has occurred. If an error is present, LRC CHECK supplied by the gap detector will activate IC16-13 and an error indication will be output, setting the error flip-flop IC6-10 and initiating the error sequence.

TYPE 3638 MEMORY

CIRCUIT DESCRIPTION

This module includes six memory stages used to store three channels of data for each of the two buffers: memories A and B. A single card includes the memory stages for channels P, 0, 1; another is used to store channels 2, 3, and 4, and another stores channels 5, 6, and 7. During a write mode the three data channels supplied to the card from the interface are input at pins P, S, and T. At this time WRITE SELECT WSEL3 (input pin X, supplied from Read Control III module) and DEVICE ENABLE DEN2 true enable the two write input NAND gates IC1-3 and IC1-6. The write data is then supplied to NOR gates IC4-10, IC4-2, and IC4-5, which in turn supply the data to the multiplexer IC8. The multiplexer is enabled WRITE SELECT WSEL or $\overline{\text{WSEL}}$ for read. The memory write gates are enabled by A MEMORY READ IN ARI true, and ARI false. ARI true enables the gates that supply the data to the memory stages of buffer A, while ARI false (equivalent to BRI true) supplies the input data to memory B. For example, when memory A is available for read-in, ARI true, output by inverter IC5-12, enables AND gates IC7-8 and IC7-11. The clocks are then gated through the NAND gates IC2-8 and IC7-11 to the appropriate RAM module.

In a read mode, three read data channels $\overline{\text{RDTA}}$ are supplied from the tape transport at input pins M, 12, and 13. The read channels are inverted and supplied to the input multiplexer IC8 enabled by $\overline{\text{WSEL3}}$ true during the read mode. The read channels are supplied to the memory through the input multiplexer, IC8 pins 3, 6, and 10, to the memory stages of either buffer A or B, depending on whether ARI is true or false.

The memory stages themselves consist of a number of RAM memory chips. The number of the chips varies according to the buffer size, and the strapping is changed to accommodate the different number of chips. A typical memory chip consists of one 1024 bit RAM. The memory address register is clocked by the memory clock ACLK or BCLK (input pins V, W) supplied from the Type 3607 Memory Counter module. In read mode the data in memory is continuously available and may be read out by simply clocking the address register, hold option.

To be read out of the memory, the output data of each memory stage is gated with either ARI or BRI, depending upon whether that stage is a part of memory A or B; thus the output data of memory A is gated with BRI to insure that memory A is <u>not</u> reading data in while it is being read out; e.g., it is in the read-out state. The corresponding memory stages of each channel are OR'd through output multiplexer IC12 and supplied to a pair of drivers. One set of drivers is enabled by READ SELECT RSEL4 true; the other is enabled by WRITE SELECT WSEL4 true (input pin 11, from memory counter module). If the recorder is in a read mode, RSEL enables the read drivers, supplying the data as RD at output pins E, K, and H to the interface. If the recorder is in a write mode, the write drivers are enabled by WSEL4 true, supplying the data as WDTA1 at output pins F, L, and J to the CRC shift register module, which then supplies the data to the write amplifiers to be written on tape. The RAM address registers IC17, 22, 27, 13, 18, and 23 are advanced on the trailing edge of ACLK or BCLK.

The multiplexer, IC12 pins 4, 7, and 9, on the output of the memories also supplies the data to a pair of exclusive-OR gates IC2-3 and IC2-11.which constitute the initial stage of a parity tree. The output of this stage is supplied as PARITY CHECK B PCHKB at output pin 2 to the time pulse generator module, where the final stages of the parity tree are situated, combining the parity outputs of all three memory modules. The parity tree then supplies the parity channel DTA1P which is either written on tape during a write mode or is supplied to the interface during a read mode. In recorders with the memory error check option, the input data channels to the memory are gated from the input multiplexer IC8 to exclusive-OR gates IC2-8 and IC2-6. These gates constitute the initial stage of another parity tree. The output of this stage is supplied as PARITY CHECK A PCHKA at output pin B to the time pulse generator module, where the final stages of the parity tree are located. That parity tree supplies the parity channel to the input of an additional memory stage, used only with the memory check option. The parity channel is then cycled through the memory with the other data channels and is checked again at the output of the memory. Should any error be detected, the time generator module issues MEMORY ERROR $\overline{\text{MEMER}}$.

TAPE MOTION CONTROL TYPE 3616

CIRCUIT DESCRIPTION

This module performs the following functions in controlling the tape motion and writing format:

a. Supplies the SYNCHRONOUS FORWARD and SYNCHRONOUS REVERSE commands to the control section of the transport.

b. Generates PROGRAM ADVANCE PADV to the tape timing module.

c. Formats the writing of the CRC and LRC characters.

d. Writes the end-of-file tape mark.

e. Supplies the synchronous readout time pulses.

f. Generates the memory counter reset pulses XRST.

SYNCHRONOUS FORWARD and SYNCHRONOUS REVERSE COMMANDS

The SYNCHRONOUS FORWARD COMMAND (SFC) is generated by NAND gates IC14-6. $\overline{\text{REST}}$, the stationary state of the program control counter, is input at pin 19 and is gated through IC25-3 and IC20-8 to IC14-1. BACKSPACE $\overline{\text{BSP}}$ (from the tape timing control module, input at pin 8) is supplied to IC14-5. If the program control counter is not in the $\overline{\text{REST}}$ or BACKSPACE state, the SFC gate is activated provided that both WRITE SELECT WSEL (pin S) and DEVICE ENABLE DEN2 (pin R) are true. The SYNCHRONOUS REVERSE COMMAND SRC is generated by NAND gate IC9-11. The SRC gate is activated by $\overline{\text{BSP}}$ true, provided that WSEL and DEN2 are also true.

PADV GENERATION

PROGRAM ADVANCE PADV is generated on this module to advance the program control counter on the tape timing control module from one state to the next. Initially the program control counter is in the REST state, with the $\overline{Q}_0$ output true; in this state no tape motion occurs. In order to advance the program counter from $\overline{\text{REST}}$ to the START $\overline{\text{DELAY}}$ state NAND gate IC1-6 must be activated. $\overline{\text{REST}}$ true at input pin 19 (supplied from the tape timing control module) is inverted by IC25-3 and enables IC1-5. TAPE RUNNING $\overline{\text{TRNG}}$ input at pin 17 enables IC1-4, since there is no tape motion at this time. When the memory has data available for readout, the memory input control module generates READ OUT START ROSRT2 true at input pin 16, activating IC1-6, which in turn activates NOR gate IC2-6, supplying PADV true at output pin W. PADV true advances the program control counter to the start delay state, in which the tape ramps up to the normal running speed. Since $\overline{\text{REST}}$ goes false at this time SFC goes true, as described above, initiating the tape motion. When the start delay is complete the delay counter on the tape timing control module issues $\overline{\text{SRTDF}}$ true at input pin U; this activates IC2-6 and supplies the next PADV to the program control counter, advancing it to the READOUT state RO. The program counter remains in the RO state until readout of the block is complete. To generate the next PADV the end of the readout state is detected on this module. When the memory readout is complete the memory counter pulse XCTRP (at input pins 4 and F, supplied from the memory input control module) or the END OF RECORD EORX (supplied from the memory modules) activates NOR gates IC15-8 or IC10-6. If memory A was reading out, for example, IC15-8 would go high, activating NAND gate IC4-6, since READ OUT A (ROA, input pin B from the memory input control module) is true at this time. This sets flip-flop IC25, test point B going high and activating NAND gate IC11-10; IC11-9 is enabled by flip-flop IC11, since the flip-flop was set by ROCLK. IC11-8 then goes low and generates the next PADV at the extender of IC2-3. This causes the program counter to advance from the RO state to the $\overline{\text{CRC}}$ state. RO then goes low and clears flip-flops IC11 and IC25 on this module. $\overline{\text{CRC}}$ true enables the gap counter on this module, starting the writing of the CRC character as described below. When the second CRC pulse is generated (CRCB) it generates another PADV, advancing the program counter to the LRC state. Of course, in seven-track recorders, only the LRC character is written on tape. After the LRC character is written the fourth counter pulse activates NOR gate IC7-6, generating the PADV which advances the program counter to the stop delay state $\overline{Q}_5$. If no error is detected, the program control counter is then reset, returning to the $\overline{\text{REST}}$ state until the next block is available for readout. If an error is detected, the program counter advances to $\overline{Q}_6$, the backspace state. $\overline{\text{BSP}}$ then goes true, activating the SRC gate on this module, causing the tape to backspace over the erroneous block. When the gap preceding the erroneous block is detected by the gap detector located on the tape timing module, $\overline{BSF}$ goes true at input pin V, generating another PADV which terminates the backspace operation and advances the program control counter to the erase state $\overline{Q}_7$. Note that in seven-track recorders capacitor C13 is used on IC1-11 to delay the termination of the backspace operation, allowing for the greater space between the read and write heads; in nine-track recorders the spacing is 0.15 inch, while in seven-track recorders it is 0.30 inch. Following the erase delay during an error sequence the tape immediately ramps up to speed again, rewriting the block as described above.

FORMATTING THE CRC AND LRC CHARACTERS

After the readout of a block of data has been completed, the main program control counter on the tape timing control module advances from the readout state to the CRC state. $\overline{CRC}$ then goes low at input pin 7 of this module, activating NOR gate IC23-8, which in turn enables NAND gate IC19-13. IC19-11 then gates the data synchronized readout pulse ROTP2 to the clock input of the gap counter. The gap counter consists of a divide-by-sixteen counter IC18 in tandem with binary to octal decoder IC13. On the second count of the counter, equivalent to the third character space of the interrecord gap, IC13-2 goes high, issuing the first of two CRC pulses — CRCA. CRCA is supplied to the CRC control module, and is used to toggle the CRC register an additional time before the writing of the CRC character. On the next gap counter count, equivalent to the fourth character count of the gap, Q13-3 goes high and issues CRCB at output pin 14; this pulse is also supplied to the CRC control module and is used to enable the CRC gates on the CRC register module, writing the actual CRC character on tape four character spaces past the last data character of the block. CRCB is also gated through NOR gate IC7-6, NAND gate IC7-3 (provided that this is not a file mark sequence) and activates NOR gates IC2-3 and IC9-6. IC2-6 generates the next PADV while IC9-4 enables NAND gate IC2-8, gating ROTP2 through as the WRITE CLOCK $\overline{WCLK}$, provided that WSEL and DEN2 are both true. $\overline{WCLK}$, output at pin P, is wire-OR'd with $\overline{WCLK2}$ output by the CRC control module, and is used to toggle the write amplifier flip-flops during the writing of the CRC character and the file mark character. Following the writing of the CRC character the main program control counter on the tape timing control module moves from the $\overline{CRC}$ state to the $\overline{LRC}$ state. $\overline{LRC}$ true at input pin 7 keeps the gap counter enabled, and on the seventh count, equivalent to the eighth character space of the interrecord block, IC13-7 goes high and activates NOR gate IC7-11 through strap 2. IC7-11 goes high and enables NAND gate IC23-4, gating ROTP2 through as WRITE AMPLIFIER RESET WARS at output pin K. WARS is supplied to the write amplifiers where it returns the write amplifier flip-flops to a known state as required for the writing of the LRC character.

In seven-track recorders the strapping is changed so that the CRC pulses are not issued. Instead, strap 1 is used so that WARS is issued on the third gap counter count, writing the LRC character four character spaces following the last data bit of the block.

WRITING THE EOF TAPE MARK

The END OF FILE command $\overline{EOF2}$, issued by the memory input control module only when there is no data in the memories, is input at pin 10 and sets the first of three EOF flip-flops, IC19. IC19-3 goes high and enables the EOF one-shot IC8, but does not fire it. $\overline{EOF2}$ is also supplied to the tape timing control module where it enables the delay counter, timing the EOF gap. Following the EOF delay the delay counter supplies $\overline{SRTDF}$ true, setting flip-flop IC12/IC23 and firing the EOF one-shot IC8. The Q output of the one-shot generates a positive pulse, 46 msec in duration, which is inverted by IC6-11 and is output as TAPE ERROR INHIBIT $\overline{TERI}$ at output pin 20. $\overline{TERI}$ is supplied to the tape timing control module where it disables the error flip-flop, preventing the file mark from being recognized as an error. The $\overline{Q}$ output of the one-shot supplies a negative-going 46 msec pulse which activates NOR gate IC20-8; IC20-8 goes high and activates the SFC gate IC14-6. This retains the SYNCHRONOUS FORWARD COMMAND true in order to advance the tape while the file mark is being written. As mentioned above, $\overline{SRTDF}$ also sets the second of the three EOF flip-flops. The 0-output of that flip-flop, IC23-12, goes low and activates NOR gate IC9-4; in addition, it is inverted by IC9-3 and enables the file mark gates. IC9-4 goes high and enables NAND gate IC2-10; ROTP2 is then gated through IC2-8, provided WSEL and DEN2 are true, and is supplied as the file mark write clock $\overline{WCLK}$ at output pin P. The file mark gates, consisting of IC3-11, IC3-4, and IC3-3 for nine-track recorders, and additionally IC3-10 for seven-track recorders, are activated, provided that WSEL and DEN2 are true, and the file mark is written on tape. Returning to the second EOF flip-flop, note that the 1-output of the flip-flop goes high and enables NAND gate IC24-9, gating ROTP4 through IC24-8 to set the third flip-flop, IC24/IC25. The 1-output of the third flip-flop sets test point A high while the 0-output goes low and clears flip-flop IC12/IC23 a single character time after that flip-flop was set. Thus the file mark gates and write clock are enabled only for the file mark character. In addition the 0-output of flip-flop IC24/IC25 activates NOR gate IC23-9, enabling the gap counter. The 0-output of IC24/IC25 also disables NAND gate IC7-1, inhibiting the CRC clock. On the seventh gap-counter count, equivalent to eight character spaces following the file mark character, IC13-7 goes high and enables NAND gate IC23-4, issuing WARS to return the write amplifier flip-flops to a known state for the writing of the LRC character. In seven-track recorders the strapping is changed so that the LRC character is written on the fourth character space following the file mark.

SYNCHRONOUS READOUT TIME PULSES

READOUT OSCILLATOR frequency ROSSC, the data synchronized crystal controlled square wave, is supplied from the memory readout control II at input pin 22. ROOSC is supplied to a series of four edge circuits, consisting of ICs 16, 17, 21, and 22, which supply a train of data synchronized pulses ROTP1, ROTP2, ROTP3, and ROTP4. Each pulse's leading edge is slightly delayed after the trailing edge of the preceding pulse; thus ROTP2 is slightly delayed after ROTP1, and so forth. These pulses are used throughout the formatting and buffer electronics to synchronize all the readout functions.

MEMORY COUNTER RESET PULSES

When memory A or memory B has completed readout of a data block and no error is detected, READOUT COMPLETE PULSE ROCOMP is supplied from the tape timing control module at input pin A. $\overline{\text{ROCOMP}}$ is inverted by IC4-3 and is supplied to the input of NAND gates IC5-3 and IC5-4. One of these gates is enabled by either READOUT A ROA true or READOUT B ROB true, depending on which memory was reading out. Thus if memory A was reading out, ROA true enables IC5-2, gating $\overline{\text{ROCOMP}}$ out as A RESET $\overline{\text{ARST}}$ at output pin 1. $\overline{\text{ARST}}$ is supplied to the memory A module where it clears both the memory counter and the EOR counter, in effect erasing any data in that memory.

CRC CONTROL TYPE 3578

CIRCUIT DESCRIPTION

This module contains a set of drivers consisting of ICs 1, 3, and 4 which supply the data from the CRC register to the write amplifier modules as WDTA2. The drivers are enabled by READ OUT (RO) true for seven-track recorders, and WRITE SELECT (WSEL2) true for nine-track recorders.

In addition, this module supplies several status outputs to the interface. TAPE LOAD POINT $\overline{\text{TLDPT}}$, input at pin 9 from control B module, is gated with $\overline{\text{ZTSEL}}$ through exclusive-OR gate IC7 to select the output logic level, and is output by driver IC6-12 at pin 17 as BOT2; BOT2 is supplied to interface connector P3. END OF TAPE EOT is also gated with $\overline{\text{ZTSEL}}$ to provide the proper output polarity, and is then output to the interface as EOT2. READY RDY, input at pin E, is inverted and is gated with FILE PROTECT through NAND gate IC3-10. If file protect is true, the gate is disabled, outputting RDY2 false at output pin U. WRITE CLOCK $\overline{\text{WCLK}}$ is input at pin B and is gated with either RO or WSEL2, depending upon whether it is a seven-track or a nine-track machine, and is supplied at pin 11 as WRITE DATA STROBE WDS to the write amplifier modules.

CRCA, the first of two CRC pulses from the tape motion control module, is input at pin 2; it is inverted by IC5-3 and it enables, when true, NAND gate IC1-2, gating READ OUT TIME PULSE ROTP2 through IC1-2 to NOR gate IC2-8, and is output as CRC TIME PULSE CRCTP.

During the block, WRITE CLOCK WCLK from the tape timing control module is gated through as CRCTP and is used to toggle the CRC register on the CRC register module. During the interrecord gap, CRCA is generated on the third character count of the block and is used to gate ROTP2 to shift the CRC register an additional time as required for the writing of the CRC character. The second CRC pulse, CRCB, is inverted on this module and is also supplied to the CRC register to gate the actual writing of the CRC character on tape.

TYPE 3642 WRITE BUFFER

CIRCUIT DESCRIPTION

This module receives the output write data from the memories, WRITE DATA P through 7, and after being inverted, supplies them to the J-K inputs of a set of nine flip-flops, which constitute the data buffer itself. The data buffer flip-flops are toggled by the WRITE DATA STROBE $\overline{\text{WDS}}$ supplied from the CRC control module. The write data strobe is first supplied to a one-shot network consisting of ICs 4 and 9 which supplies a 1 μsec pulse for each $\overline{\text{WDS}}$ pulse. At the end of the write data WRITE AMPLIFIER RESET PULSE $\overline{\text{WARS}}$, supplied from the tape motion control module, resets the write buffer amplifiers to a known state. The write data channels FWDC P through 7 output from the write buffer are supplied to the tape transport, to be written on tape.

TYPE 3641 READ SKEW DELAY/GAP DETECT

CIRCUIT DESCRIPTION

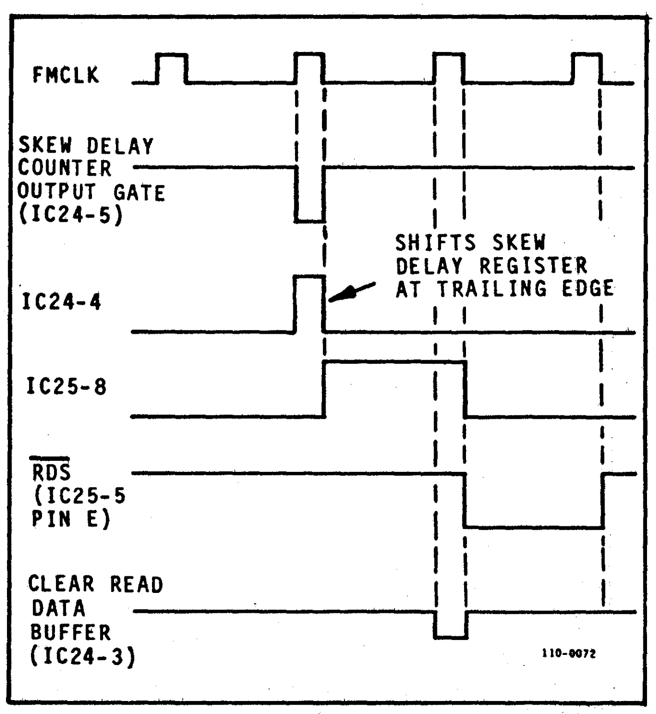
This module provides deskewing of the NRZ1 read data inputs from the tape transport. These inputs, designated FRDCP, FRDC0 through FRDC7, are connected to the toggles of a set of nine J-K flip-flops, comprising the read data buffer. The J inputs of these flip-flops can be cleared but cannot be set. The input signals consist of peak-detected pulses which have been deskewed in the tape transport to compensate for gap scatter and parallel, each pulse corresponding to a logic 1 in that data channel. The zero-transition on the negative-going leading edge of a data pulse toggles the associated data buffer flip-flop, causing the $\overline{Q}$ output to go high. The $\overline{Q}$ outputs from the nine buffer flip-flops are tied to the J inputs of the skew delay register flip-flops. The Q outputs are tied to the K inputs and to NOR gate IC17 which controls the skew delay counter. The first flip-flop in the buffer to be toggled during a given character space initiates the deskew function. After the data has been shifted through the skew delay register, the buffer flip-flops are reset (direct-set by an output from the read clock generator described below).

SKEW DELAY REGISTER

The skew delay register consists of a set of nine J-K flip-flops, ICs 1, 2, 4, 6, and 9, which receive data inputs from the read data buffer flip-flops. The data is transferred to the slave output section of each flip-flop by an output pulse from the skew delay counter which toggles all nine flip-flops simultaneously, at the approximate midpoint of the character space. The Q outputs of the flip-flops are the positive-true logic levels RDTAP and RDTA0 through RDTA7. These outputs are supplied to Tape Timing Control Type 3633 module for error check and gap detection, and to the memory modules for storage.

SKEW DELAY COUNTER AND READ CLOCK GENERATOR

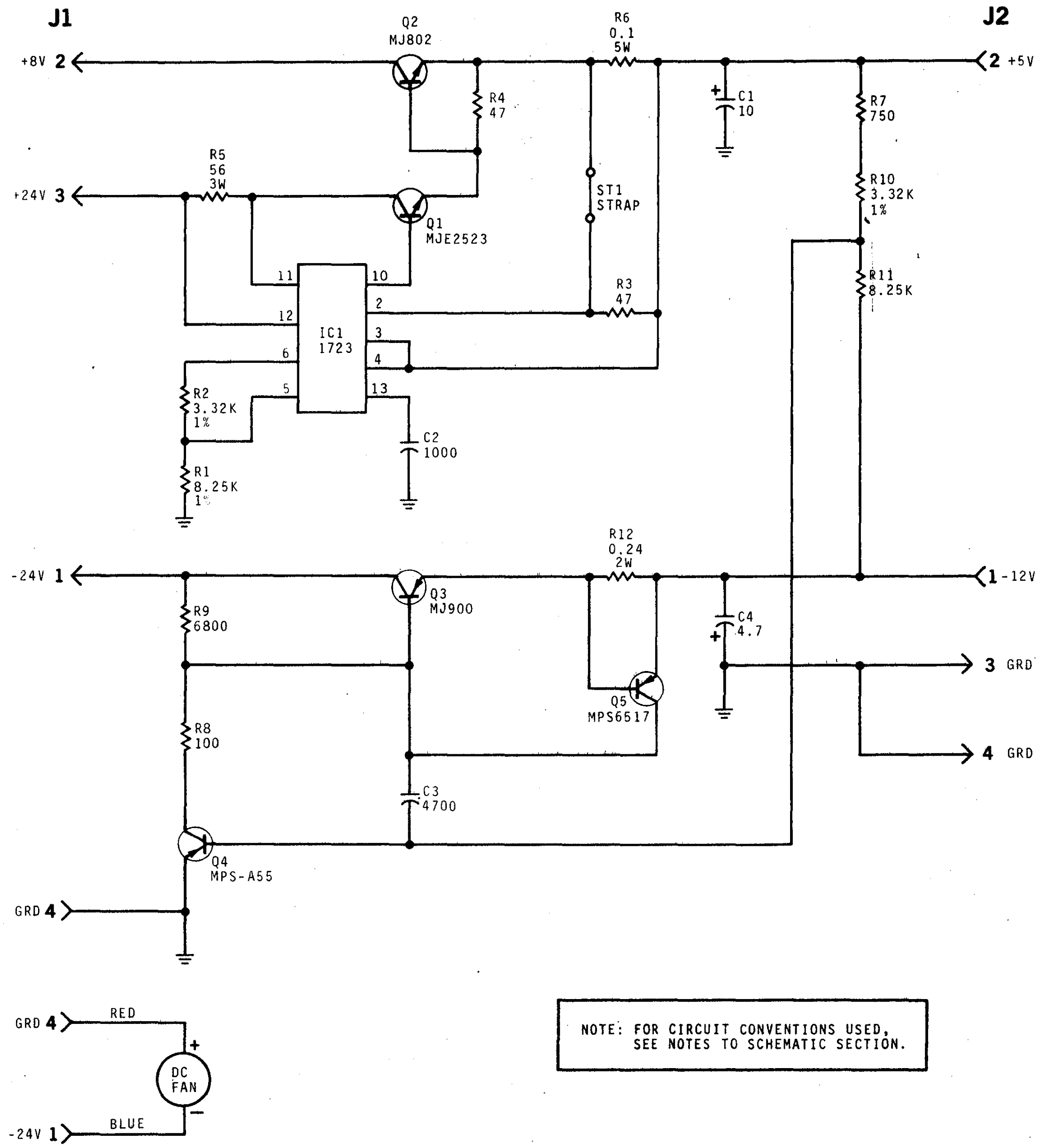
The Q outputs of the data buffer flip-flops are connected to NOR gate IC17. The first 1-bit on the data input lines during each character space causes IC17-8 to go high. If this is the first character in a data block, the change in level at IC17-8 is gated through inverter IC21-10, toggling flip-flop IC16 to a clear state; the $\overline{Q}$ output of the flip-flop goes high and enables NAND gate IC3-12, so that the next MASTER CLOCK PULSE FMCLK from the Time Pulse Generator Type 3640 module (input pin 12) is gated through IC3-11 to start the skew delay counter. The skew delay counter consists of divide-by-sixteen counters ICs 12 and 13, connected in series. Each subsequent FMCLK pulse advances the counter one count. The counter outputs are connected to a set of three gates: IC17-6, IC8-6, IC8-8. Each gate is enabled by a different data density, as selected by the DENSITY SELECT lines $\overline{TSDY1}$ and $\overline{TSDY2}$ (supplied from the transport, input at pins 11 and 13). The coded densities are tabulated on the schematic diagram. When 200 cpi density has been selected, IC8-9 is enabled. IC8-8 then goes low when the skew delay counter reaches the count of 120. Since FMCLK is 256 times the data rate for 200 cpi operation, this count occurs approximately 47 percent of the distance between two successive data characters. Similarly, for 556 cpi operation IC17-2 is enabled, and IC17-6 goes low at the count of 44. For 800 cpi operation IC8-6 is also enabled at the midpoint of the character. The timing diagram below shows the relationships of the timing functions controlled by the skew delay counter. The positive-going pulse output by IC24-4 toggles the skew delay register flip-flops, coincident with the



Skew Delay Timing Diagram

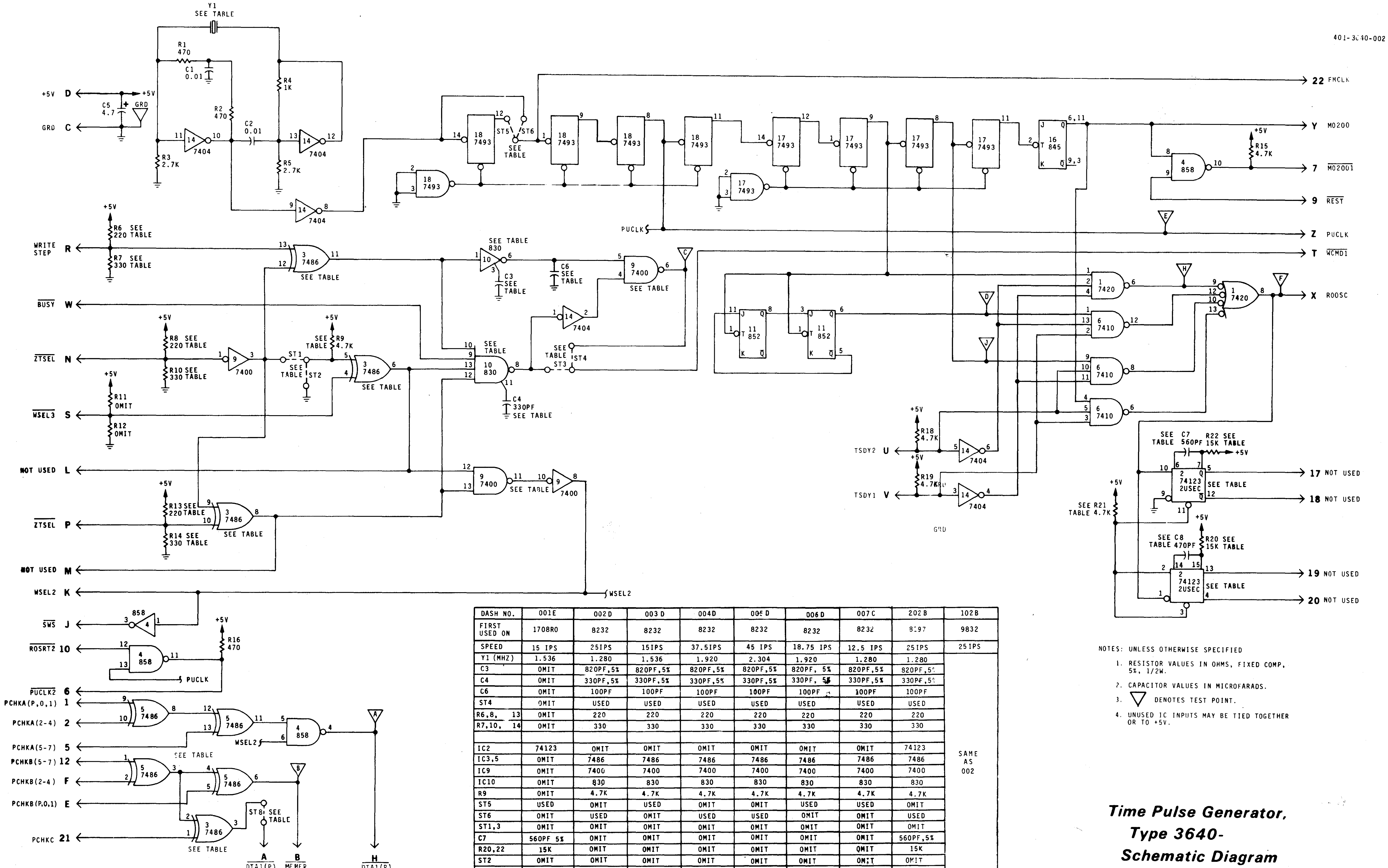
trailing edge of the pulse, shifting the data to the output signal lines, and to the memory and timing control modules. The counter output gate also sets the J input of flip-flop IC25 high and the K input low, so that the trailing edge of the FMCLK pulse sets the flip-flop, causing its Q output to go high and $\overline{Q}$ output to go low. This output generates the READ DATA STROBE $\overline{RDS}$ at pin E. $\overline{RDS}$ is the read clock used to strobe the read data into the memory; it is supplied to Read Control I Type 3817 module. The next FMCLK pulse after IC25-5 goes low toggles the second IC25 flip-flop back to clear condition and its $\overline{Q}$ output goes high. Thus, the read clock pulse width is equal to the time between two successive MASTER CLOCK FMCLK pulses, approximately 700 nanoseconds at a tape speed of 25 ips.

This completes the skew delay and read clock output sequence. The skew delay counter remains in clear status until the first 1-bit in the next data character toggles the data buffer flip-flop and starts a new count sequence.



Power Supply Regulator, Type 4480-002A, Schematic Diagram

401-3640-002 E

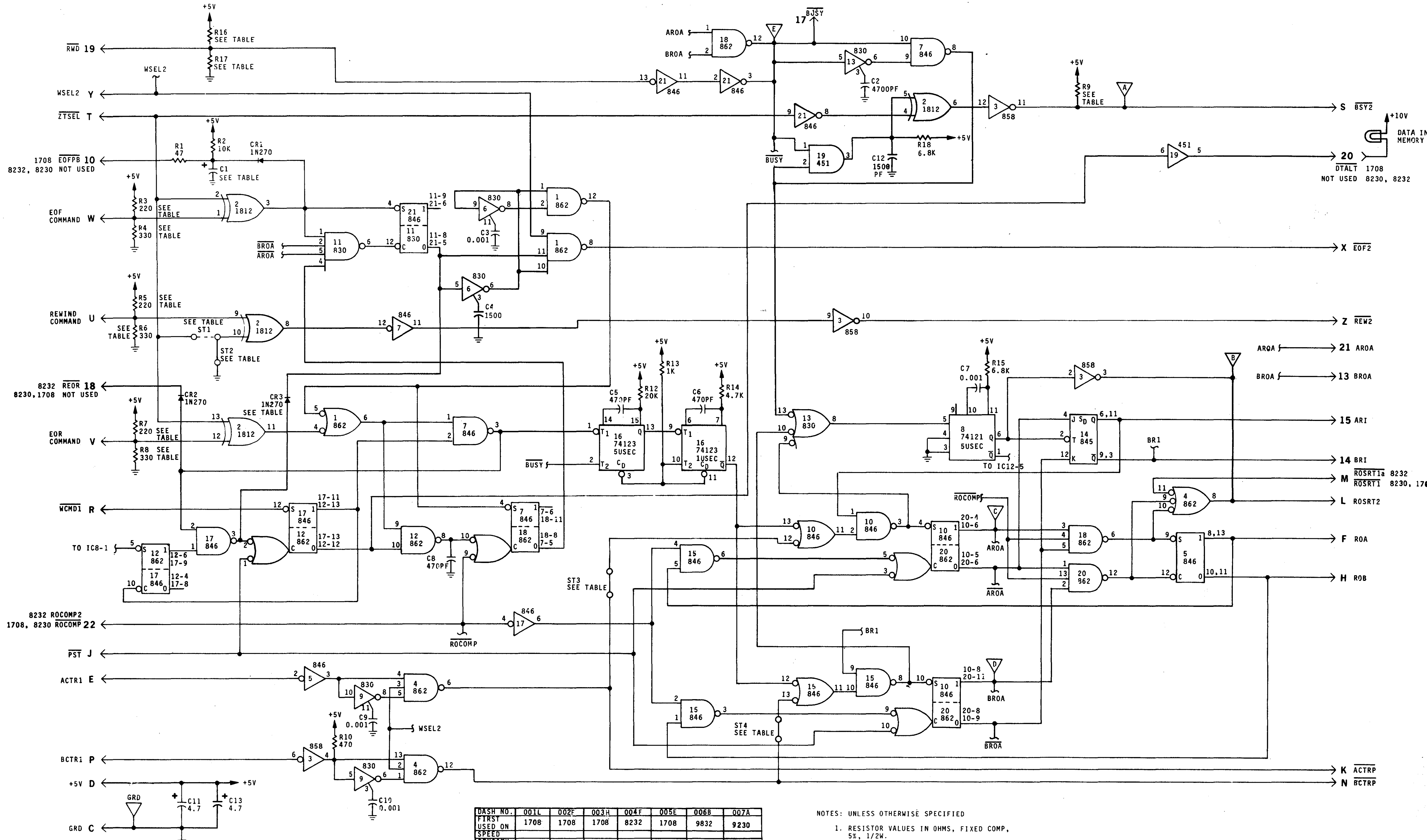


DASH NO.	001E	002D	003D	004D	005D	006D	007C	202B	102B
FIRST USED ON	1708R0	8232	8232	8232	8232	8232	8232	8197	9832
SPEED	15 IPS	25IPS	15IPS	37.5IPS	45 IPS	18.75 IPS	12.5 IPS	25IPS	25IPS
Y1 (MHZ)	1.536	1.280	1.536	1.920	2.304	1.920	1.280	1.280	SAME AS 002
C3	OMIT	820PF,5%	820PF,5%	820PF,5%	820PF,5%	820PF, 5%	820PF,5%	820PF,5%	
C4	OMIT	330PF,5%	330PF,5%	330PF,5%	330PF,5%	330PF, 5%	330PF,5%	330PF,5%	
C6	OMIT	100PF	100PF	100PF	100PF	100PF	100PF	100PF	
ST4	OMIT	USED	USED	USED	USED	USED	USED	USED	
R6,8, 13	OMIT	220	220	220	220	220	220	220	
R7,10, 14	OMIT	330	330	330	330	330	330	330	
IC2	74123	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	74123	
IC3,5	OMIT	7486	7486	7486	7486	7486	7486	7486	
IC9	OMIT	7400	7400	7400	7400	7400	7400	7400	
IC10	OMIT	830	830	830	830	830	830	830	
R9	OMIT	4.7K	4.7K	4.7K	4.7K	4.7K	4.7K	4.7K	
ST5	USED	OMIT	USED	OMIT	OMIT	USED	USED	OMIT	
ST6	OMIT	USED	OMIT	USED	USED	OMIT	OMIT	USED	
ST1,3	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	
C7	560PF 5%	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	560PF,5%	
R20,22	15K	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	15K	
ST2	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	
SCHEMATIC	001	002	002	002	002	002	002	002	
C8	470PF 5%	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	470PF,5%	
R21	4.7K	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	4.7K	
ST 8	OMIT	USED							

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.

Time Pulse Generator, Type 3640- Schematic Diagram



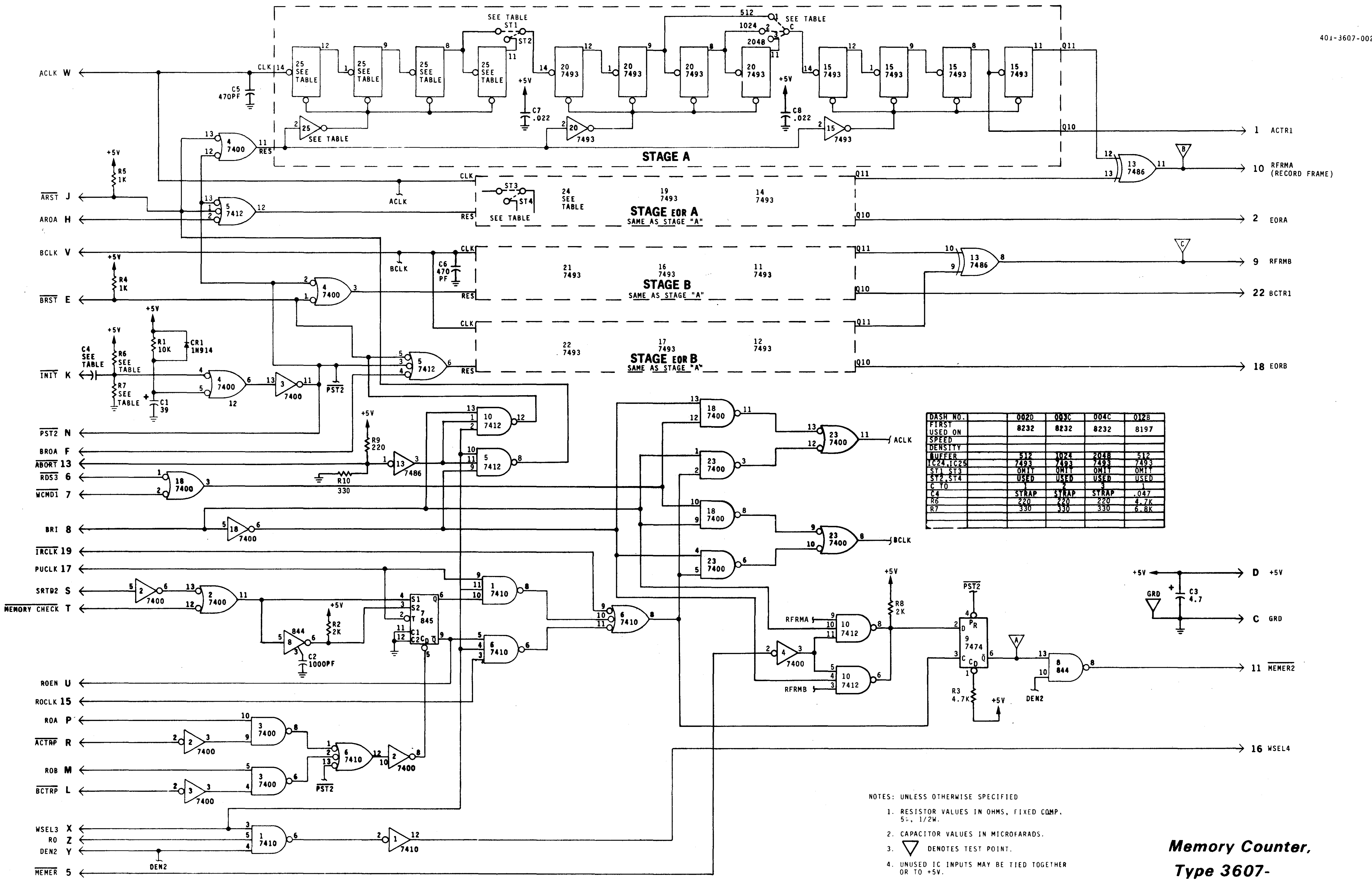
DASH NO.	001L	002F	003H	004F	005E	006B	007A
FIRST USED ON	1708	1708	1708	8232	1708	9832	9230
SPEED							
DENSITY							
R9	OMIT	OMIT	470	OMIT	OMIT	OMIT	OMIT
ST1	OMIT	USED	OMIT	USED	OMIT	USED	OMIT
ST2	USED	OMIT	USED	OMIT	USED	OMIT	USED
R3,R5,R7	AS	AS	3.3K	AS	AS	AS	AS
R4,R6,R8	AS	AS	220PF	AS	AS	AS	AS
R16	OMIT	OMIT	OMIT	220	OMIT	220	OMIT
R17	OMIT	OMIT	OMIT	330	OMIT	330	OMIT
ST3	USED	USED	USED	USED	OMIT	OMIT	OMIT
ST4	USED	USED	USED	USED	OMIT	OMIT	OMIT
CR3	OMIT	OMIT	OMIT	OMIT	AS	OMIT	OMIT
C1	0.047	0.047	0.047	4.7	0.047	4.7	0.047

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.
5. RESISTORS R4, R6 AND R8 ARE REPLACED BY 220PF CAPACITORS FOR -003 ONLY.

Memory Input Control
Type 3516
Schematic Diagram

401-3607-002D1

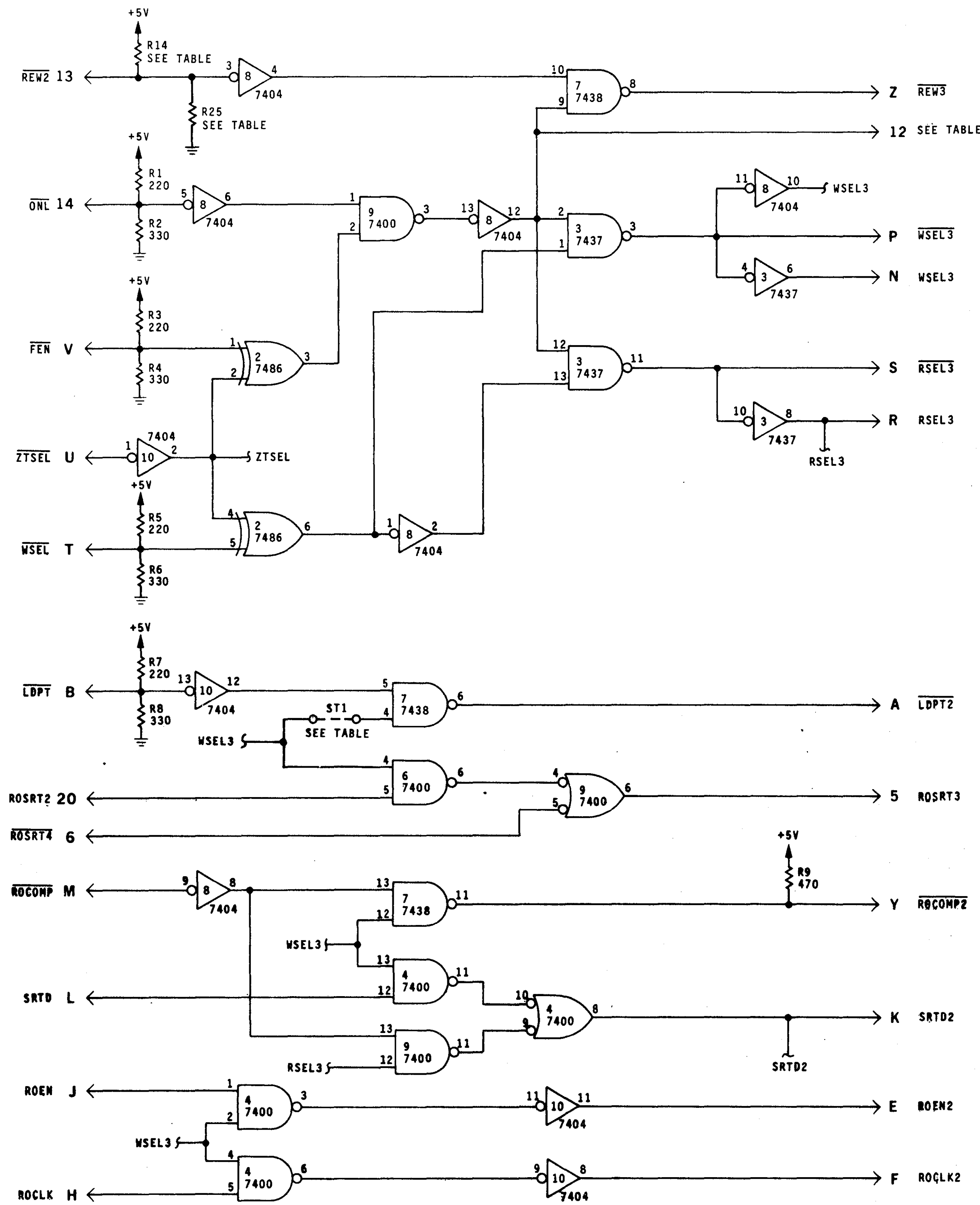


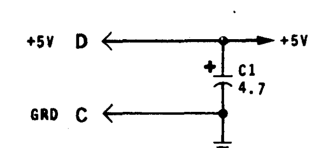
DASH NO.		002D	003C	004C	012B
FIRST USED ON		8232	8232	8232	8197
SPEED					
DENSITY					
BUFFER		512	1024	2048	512
IC24,IC25		7493	7493	7493	7493
ST1,ST3		OMIT	OMIT	OMIT	OMIT
ST2,ST4		USED	USED	USED	USED
C TO		1	2	3	1
C4		STRAP	STRAP	STRAP	.047
R6		220	220	220	4.7K
R7		330	330	330	6.8K

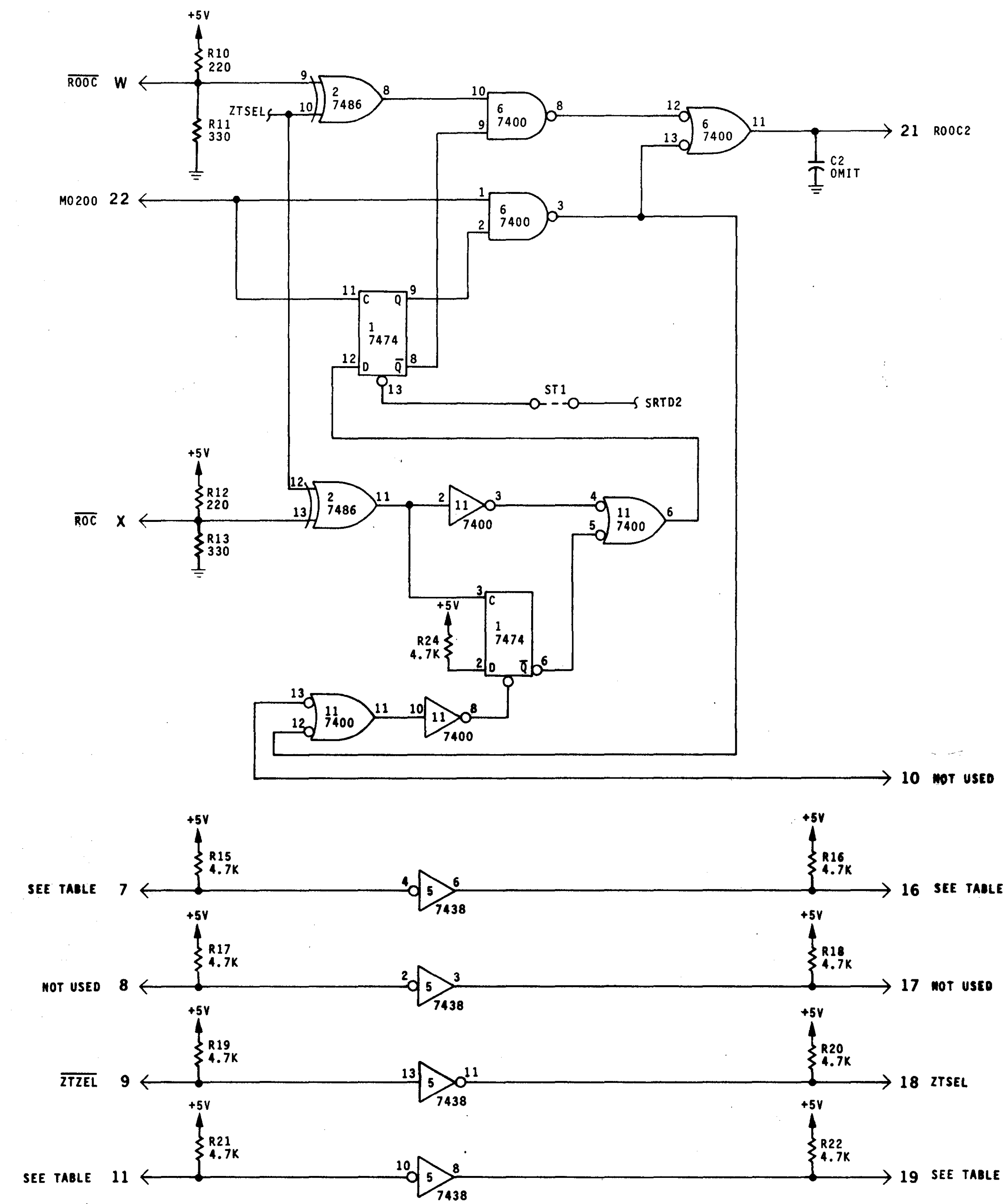
NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP. 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.

Memory Counter, Type 3607- Schematic Diagram







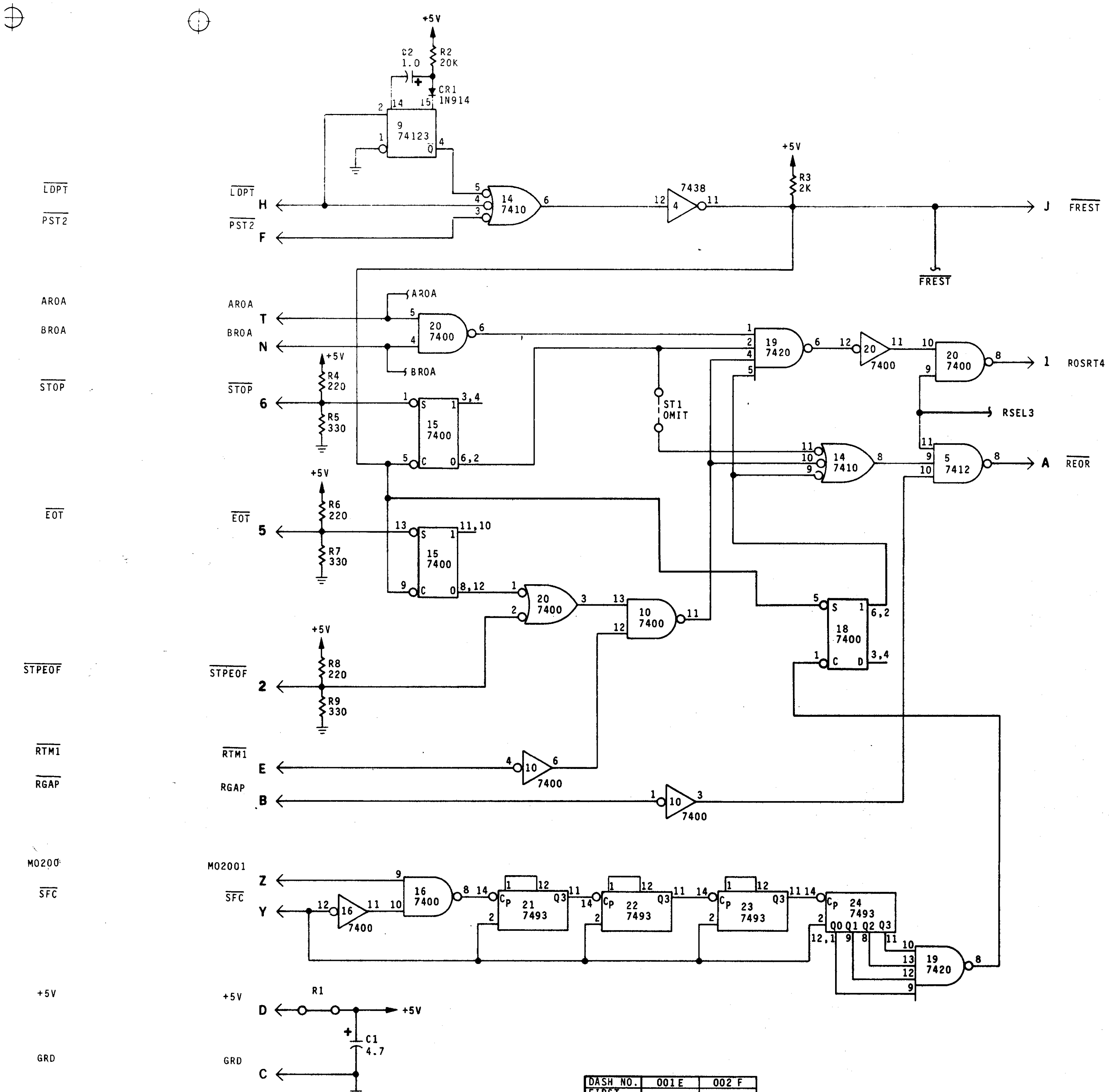
	-002 A	-011 A
R14	1K	220
R25	OMIT	330
7	NOT USED	EOT
11	NOT USED	EOT
16	NOT USED	EOT
19	NOT USED	EOT
12	DEN3	DEN
ST1	USED	OMIT

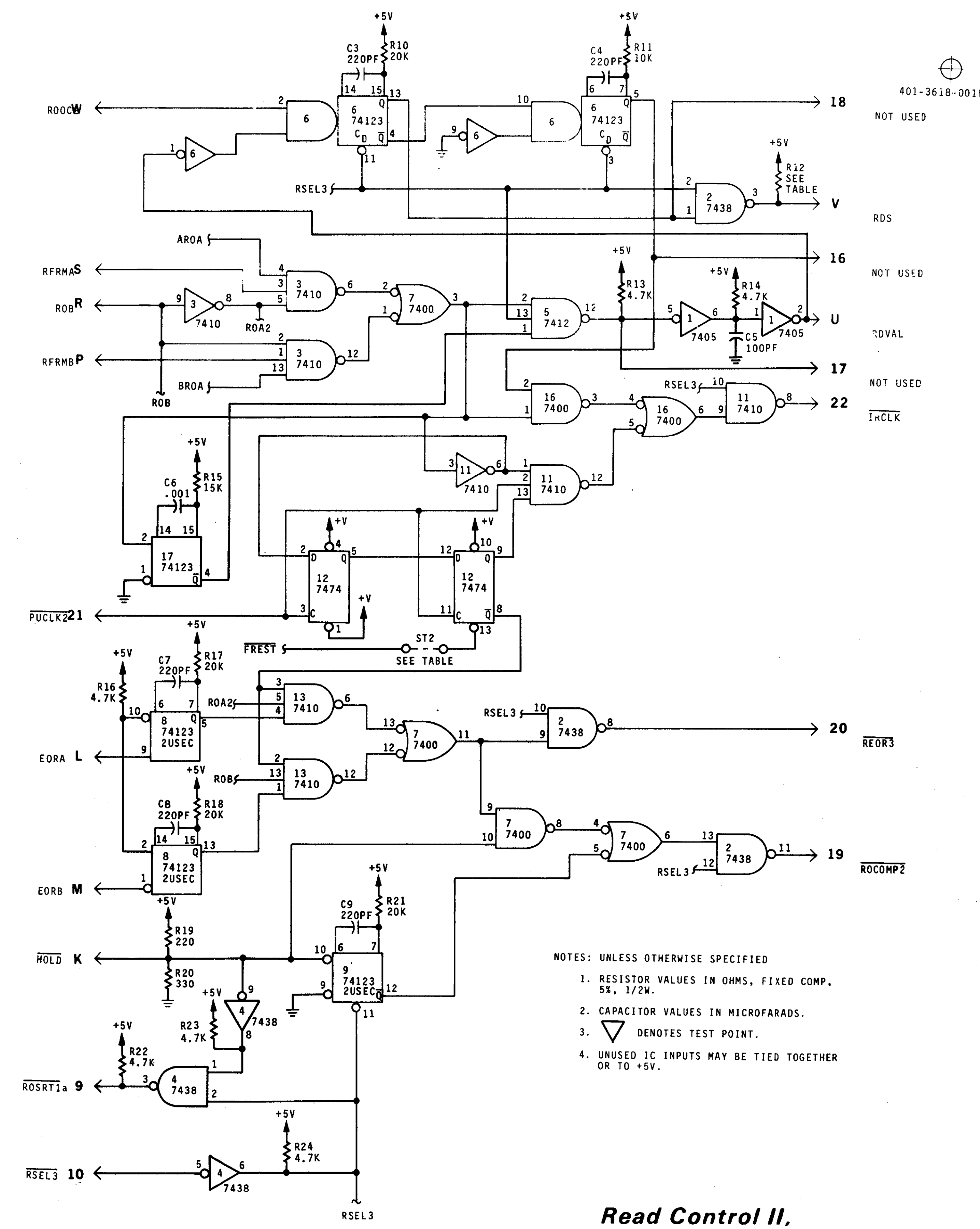
TABLE

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.

Read Control III, Type 3660 Schematic Diagram



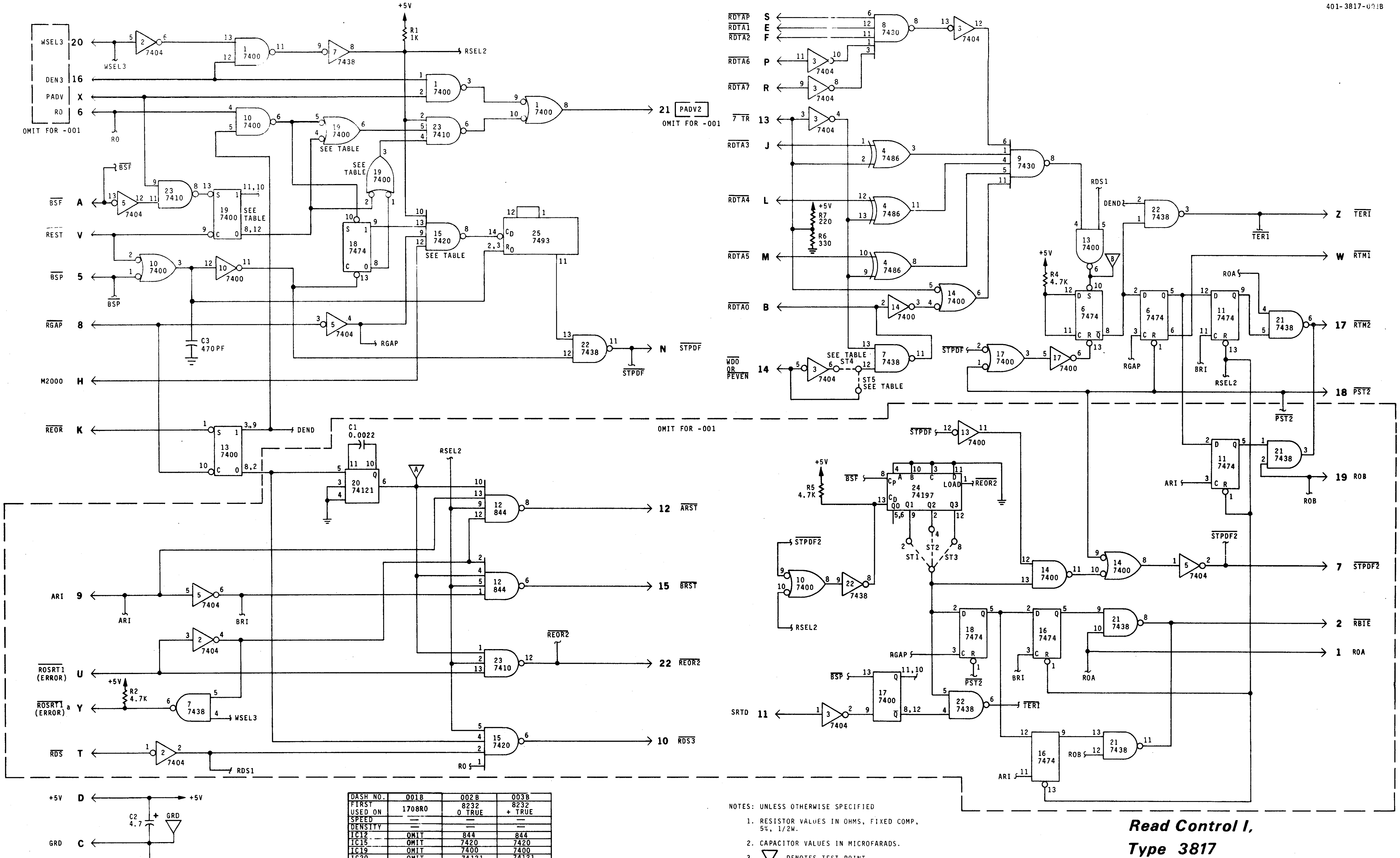


DASH NO.	001 E	002 F
FIRST USED ON	8237	1708R0
SPEED		
DENSITY		
SCHEMATIC	001	002
ST2	USED	OMIT
R12	OMIT	470

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.

Read Control II, Type 3618 Schematic Diagram

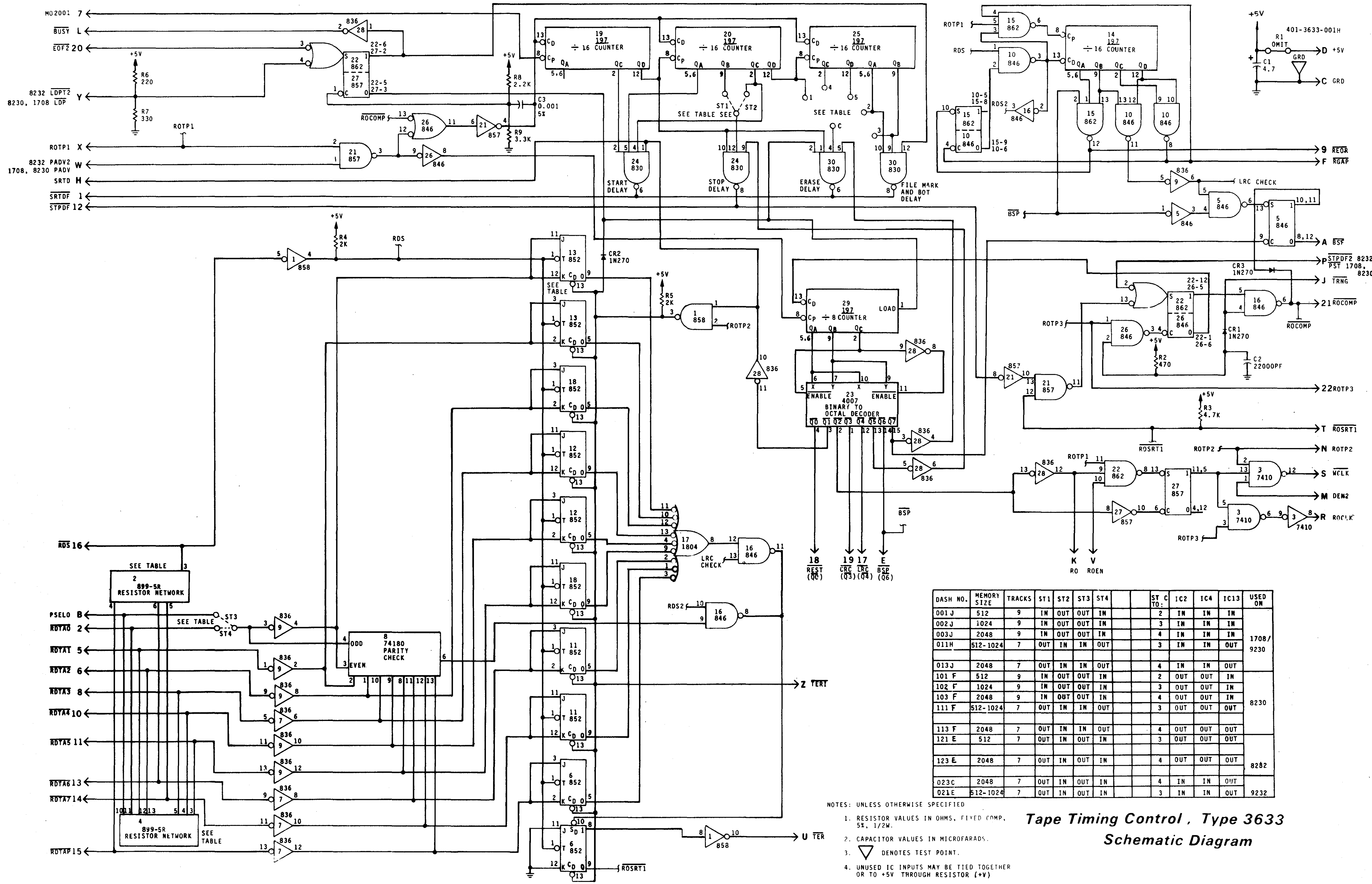


DASH NO.	001B	002B	003B
FIRST USED ON	1708R0	8232 O TRUE	8232 + TRUE
SPEED	—	—	—
DENSITY	—	—	—
IC12	OMIT	844	844
IC15	OMIT	7420	7420
IC19	OMIT	7400	7400
IC20	OMIT	74121	74121
ST1	OMIT	USED	USED
ST2	OMIT	OMIT	OMIT
ST3	OMIT	OMIT	OMIT
ST4	OMIT	USED	OMIT
ST5	USED	OMIT	USED
IC16	OMIT	7474	7474
IC24	OMIT	74197	74197
C1	OMIT	.0022	.0022
R2,R5	OMIT	4.7K	4.7K

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED INPUTS OF IC MAY BE TIED TOGETHER OR TO +5V THROUGH RESISTOR (+V)

Read Control I, Type 3817 Schematic Diagram



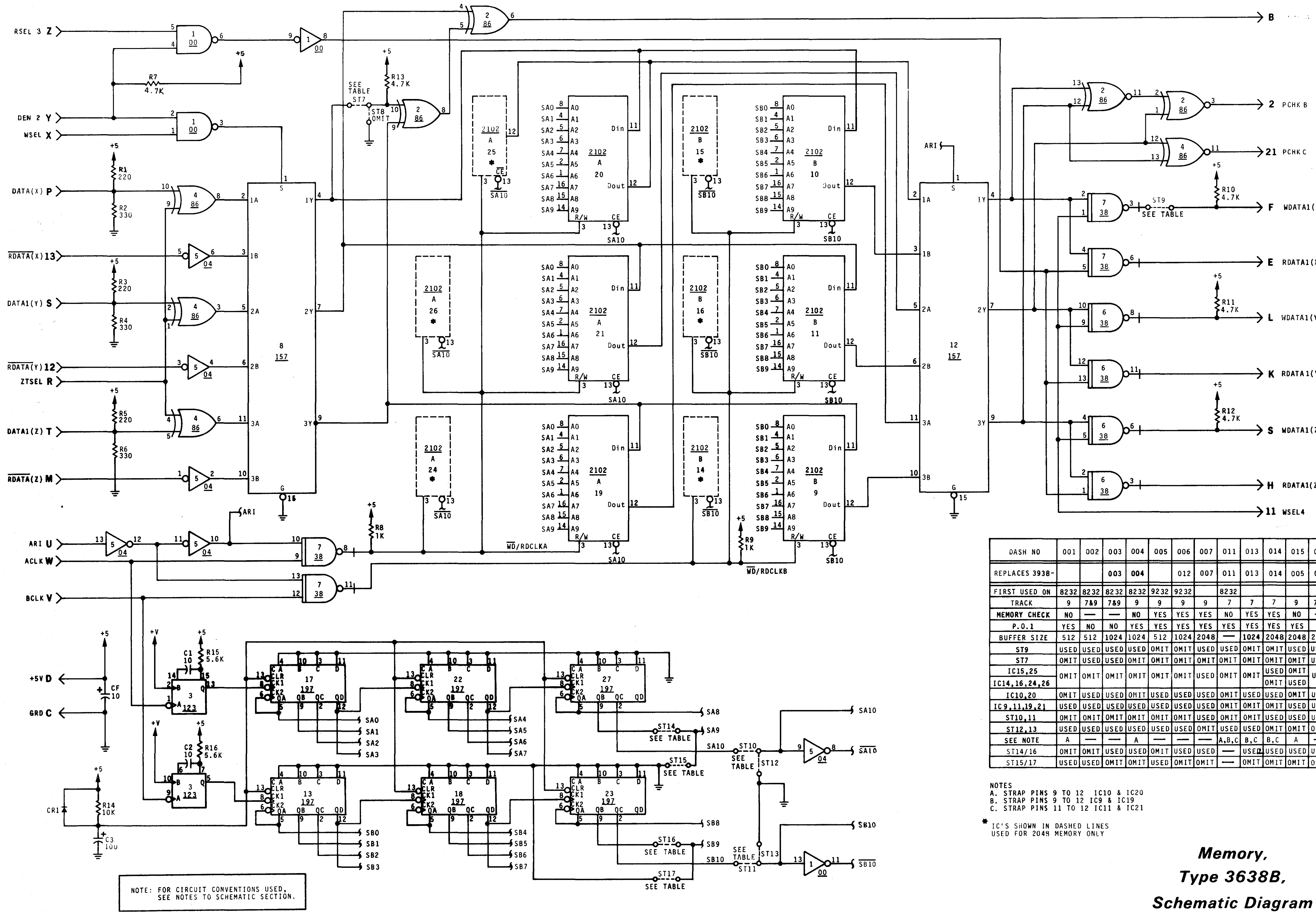
DASH NO.	MEMORY SIZE	TRACKS	ST1	ST2	ST3	ST4			ST C TO:	IC2	IC4	IC13	USED ON
001 J	512	9	IN	OUT	OUT	IN			2	IN	IN	IN	
002 J	1024	9	IN	OUT	OUT	IN			3	IN	IN	IN	
003J	2048	9	IN	OUT	OUT	IN			4	IN	IN	IN	
011H	512-1024	7	OUT	IN	IN	OUT			3	IN	IN	OUT	1708/ 9230
013J	2048	7	OUT	IN	IN	OUT			4	IN	IN	OUT	
101 F	512	9	IN	OUT	OUT	IN			2	OUT	OUT	IN	
102 F	1024	9	IN	OUT	OUT	IN			3	OUT	OUT	IN	
103 F	2048	9	IN	OUT	OUT	IN			4	OUT	OUT	IN	
111 F	512-1024	7	OUT	IN	IN	OUT			3	OUT	OUT	OUT	8230
113 F	2048	7	OUT	IN	IN	OUT			4	OUT	OUT	OUT	
121 E	512	7	OUT	IN	OUT	IN			3	OUT	OUT	OUT	
123 E	2048	7	OUT	IN	OUT	IN			4	OUT	OUT	OUT	8282
023C	2048	7	OUT	IN	OUT	IN			4	IN	IN	OUT	
021E	512-1024	7	OUT	IN	OUT	IN			3	IN	IN	OUT	9232

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V THROUGH RESISTOR (+V)

Tape Timing Control, Type 3633
Schematic Diagram

401-3638-001H1



DASH NO	001	002	003	004	005	006	007	011	013	014	015	016	017
REPLACES 3938-			003	004		012	007	011	013	014	005	006	
FIRST USED ON	8232	8232	8232	8232	9232	9232		8232					9232
TRACK	9	7&9	7&9	9	9	9	9	7	7	7	9	7&9	7
MEMORY CHECK	NO	—	—	NO	YES	YES	YES	NO	YES	YES	NO	—	YES
P.O.1	YES	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES	NO	YES
BUFFER SIZE	512	512	1024	1024	512	1024	2048	—	1024	2048	2048	2048	512
ST9	USED	USED	USED	USED	OMIT	OMIT	USED	USED	OMIT	OMIT	USED	USED	OMIT
ST7	OMIT	USED	USED	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	USED	OMIT
IC15,25	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	USED	OMIT	OMIT	USED	OMIT	USED	OMIT
IC14,16,24,26										OMIT	USED		
IC10,20	OMIT	USED	USED	OMIT	USED	USED	USED	OMIT	USED	USED	OMIT	USED	USED
IC9,11,19,21	USED	USED	USED	USED	USED	USED	USED	OMIT	OMIT	OMIT	USED	USED	OMIT
ST10,11	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	USED	OMIT	OMIT	USED	USED	USED	OMIT
ST12,13	USED	USED	USED	USED	USED	USED	OMIT	USED	USED	OMIT	OMIT	OMIT	USED
SEE NOTE	A	—	—	A	—	—	—	A,B,C	B,C	B,C	A	—	B,C
ST14/16	OMIT	OMIT	USED	USED	OMIT	USED	USED	—	USED	USED	USED	USED	OMIT
ST15/17	USED	USED	OMIT	OMIT	USED	OMIT	OMIT	—	OMIT	OMIT	OMIT	OMIT	USED

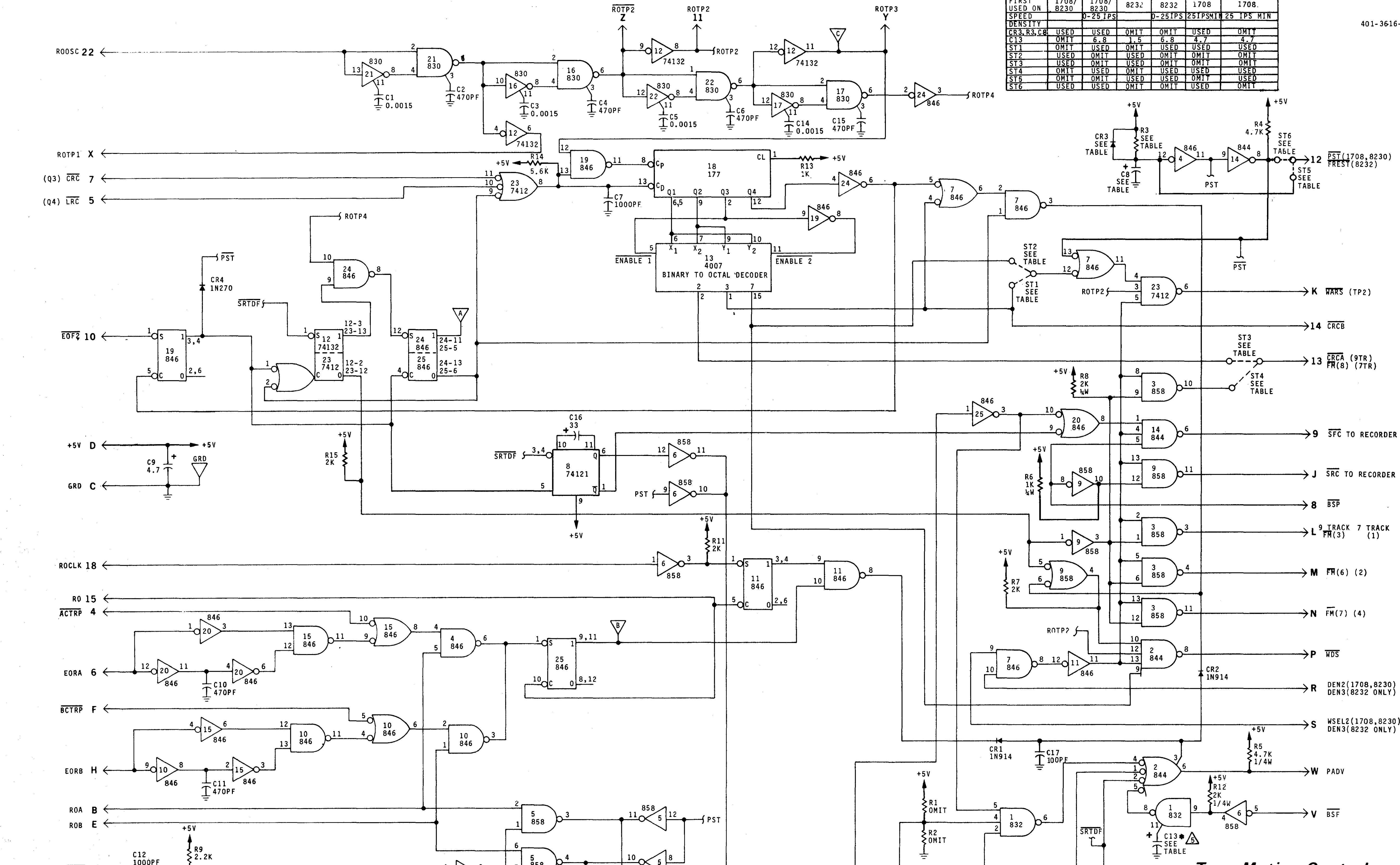
NOTES
A. STRAP PINS 9 TO 12 IC10 & IC20
B. STRAP PINS 9 TO 12 IC9 & IC19
C. STRAP PINS 11 TO 12 IC11 & IC21

* IC'S SHOWN IN DASHED LINES USED FOR 2048 MEMORY ONLY

Memory, Type 3638B, Schematic Diagram

401-3616-001- M

DASH NO.	001M	002L	003F	004H	012F	014 F
FIRST USED ON	1708/ 8230	1708/ 8230	8232	8232	1708	1708.
SPEED		0-25 IPS		0-25IPS	25IPSMIN	25 IPS MIN
DENSITY						
CR3,R3,C8	USED	USED	OMIT	OMIT	USED	OMIT
C13	OMIT	6.8	1.5	6.8	4.7	4.7
ST1	OMIT	USED	OMIT	USED	USED	USED
ST2	USED	OMIT	USED	OMIT	OMIT	OMIT
ST3	USED	OMIT	USED	OMIT	OMIT	OMIT
ST4	OMIT	USED	OMIT	USED	USED	USED
ST5	OMIT	OMIT	USED	USED	OMIT	USED
ST6	USED	USED	OMIT	OMIT	USED	OMIT



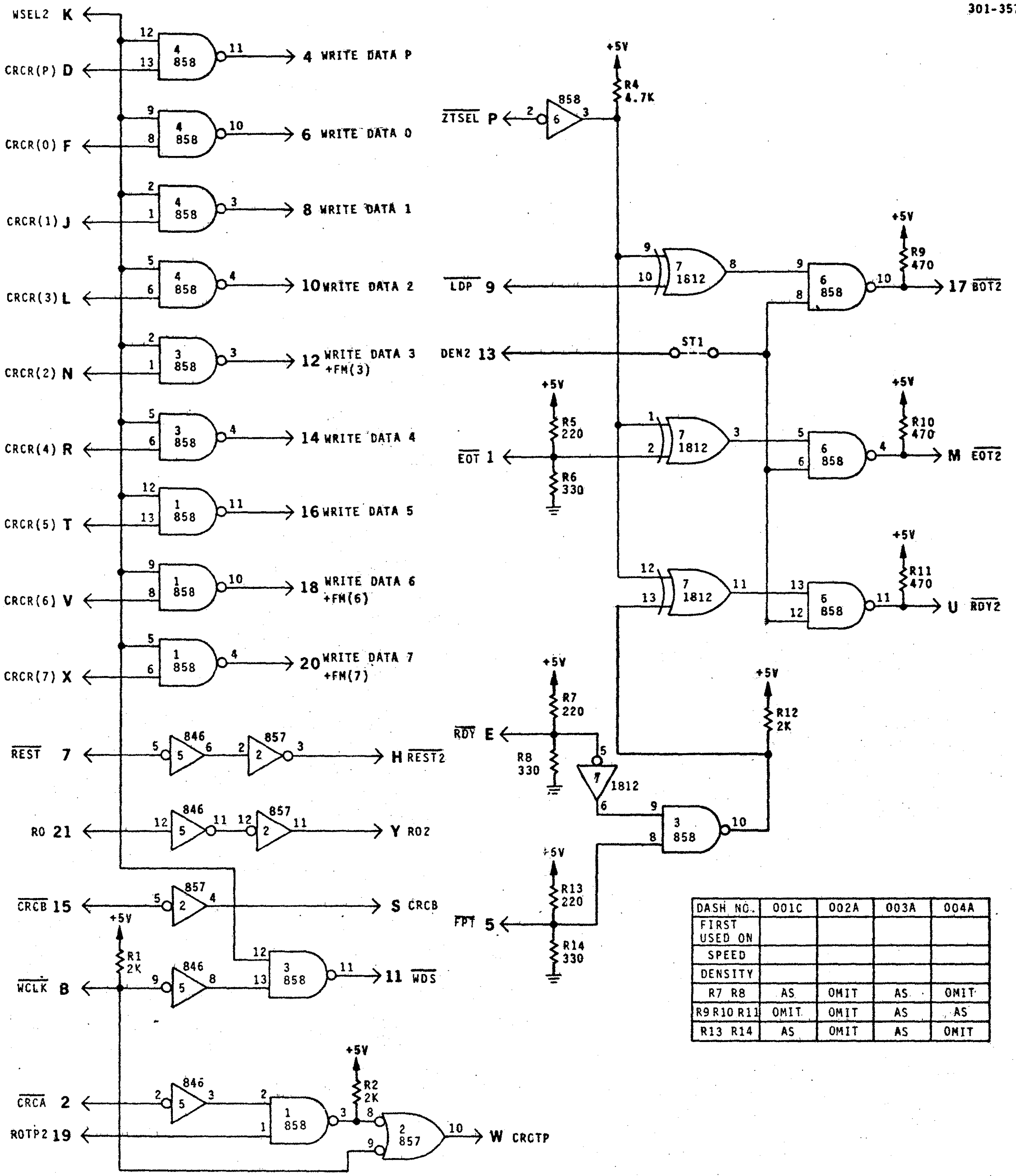
NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.

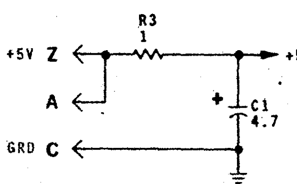
△5 ADJUST VALUE OF CAPACITOR C13 IF NECESSARY

Tape Motion Control Type 3616 Schematic Diagram

301-3578-001-D



DASH NO.	001C	002A	003A	004A
FIRST USED ON				
SPEED				
DENSITY				
R7 R8	AS	OMIT	AS	OMIT
R9 R10 R11	OMIT	OMIT	AS	AS
R13 R14	AS	OMIT	AS	OMIT

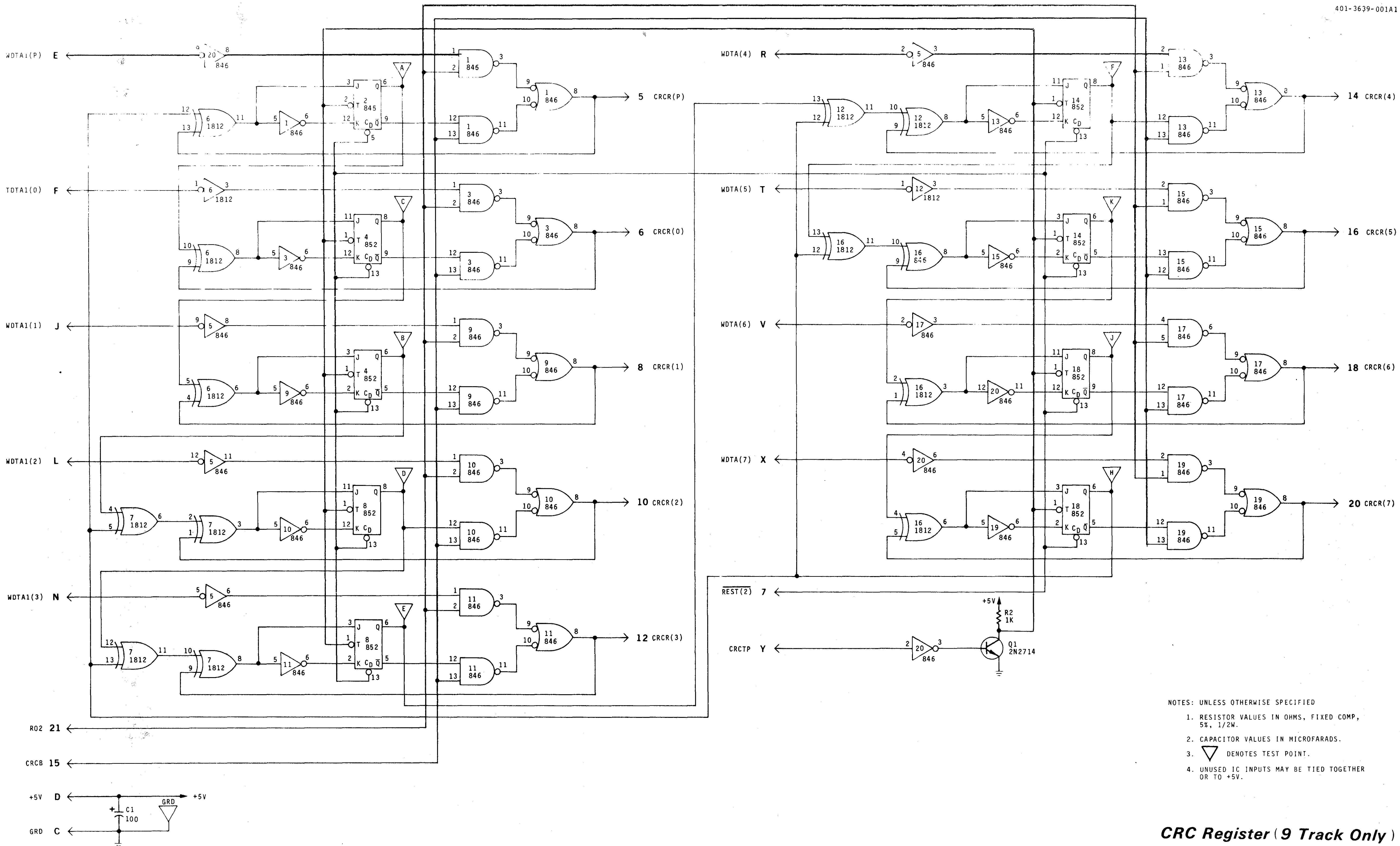


NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.

CRC Control
Type 3578
Schematic Diagram

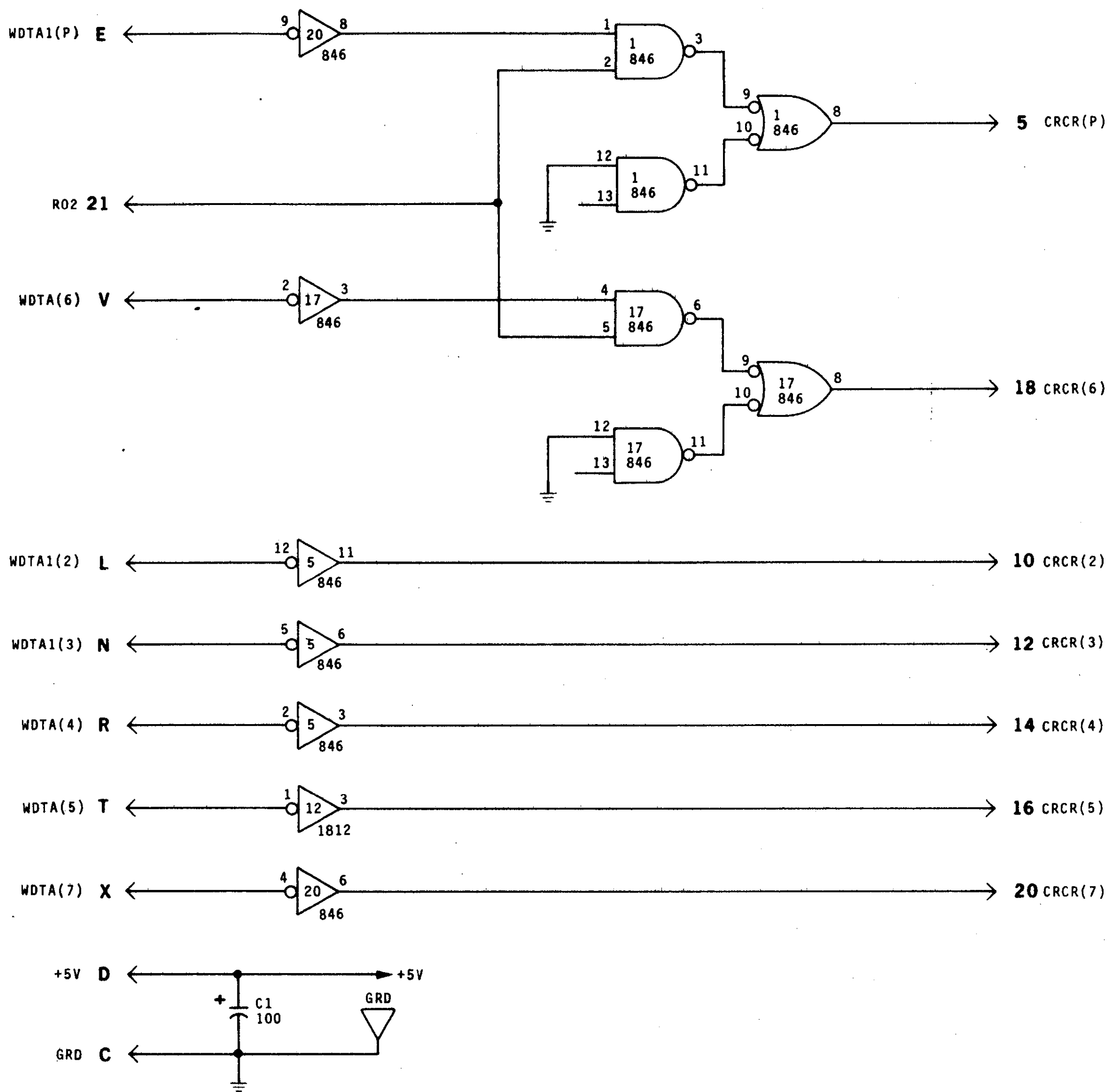
401-3639-001A1



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.

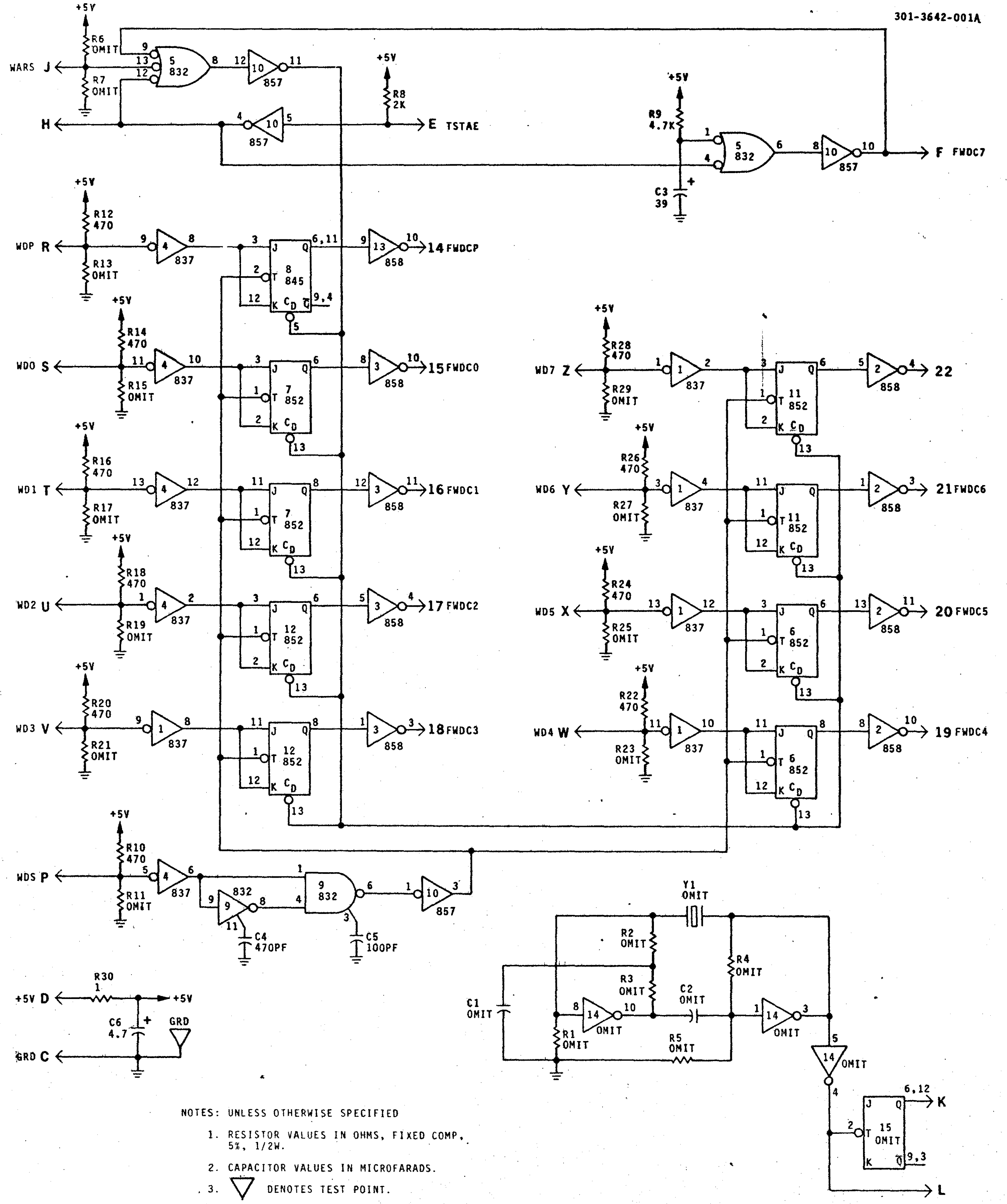
CRC Register (9 Track Only)
Type 3639-001A
Schematic Diagram



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.

CRC Register (7 Track Only)
Type 3639-002A
Schematic Diagram

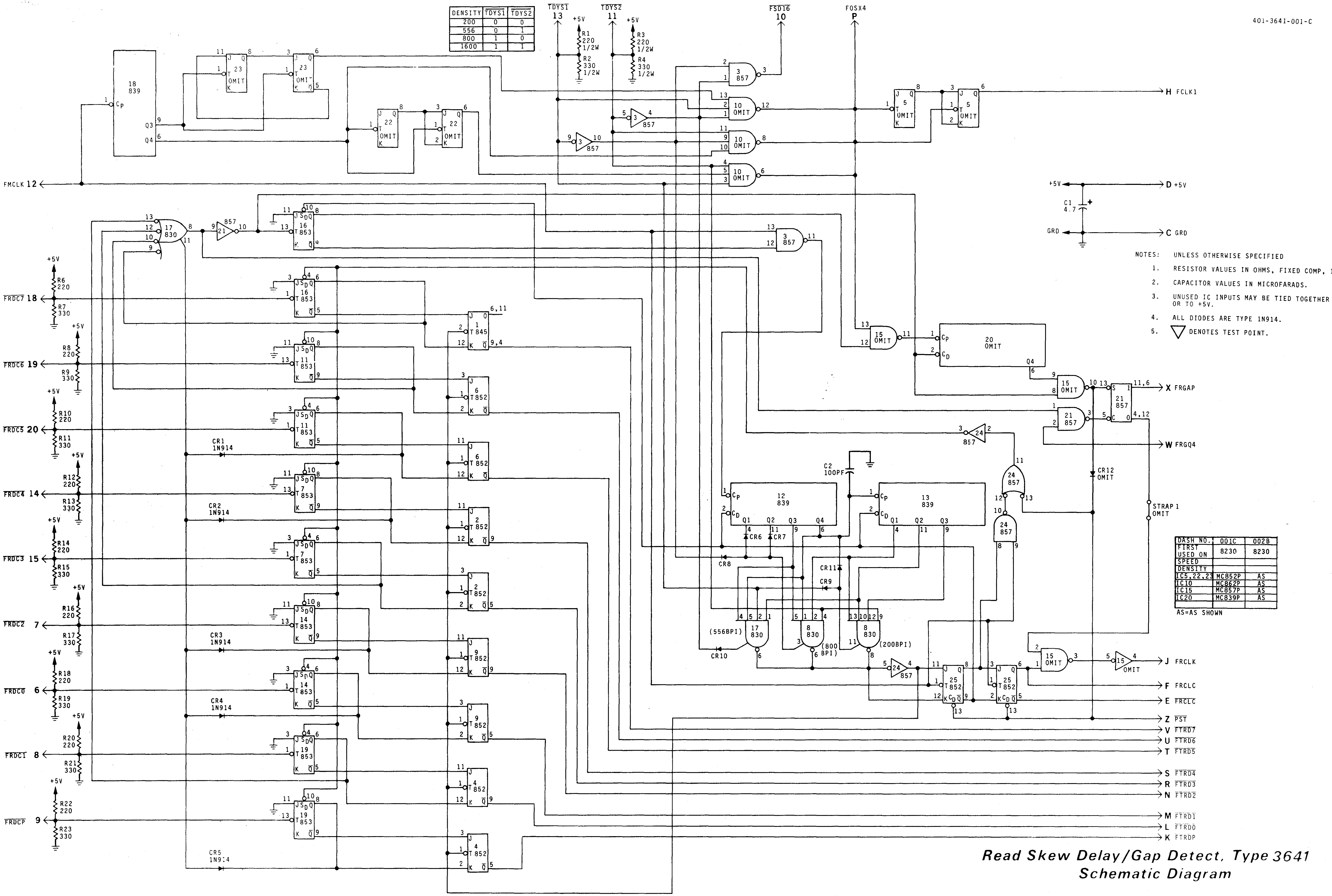


NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.

Write Buffer Type 3642-001A
Schematic Diagram

401-3641-001-C



DENSITY	$\overline{TDYS1}$	$\overline{TDYS2}$
200	0	0
556	0	1
800	1	0
1600	1	1

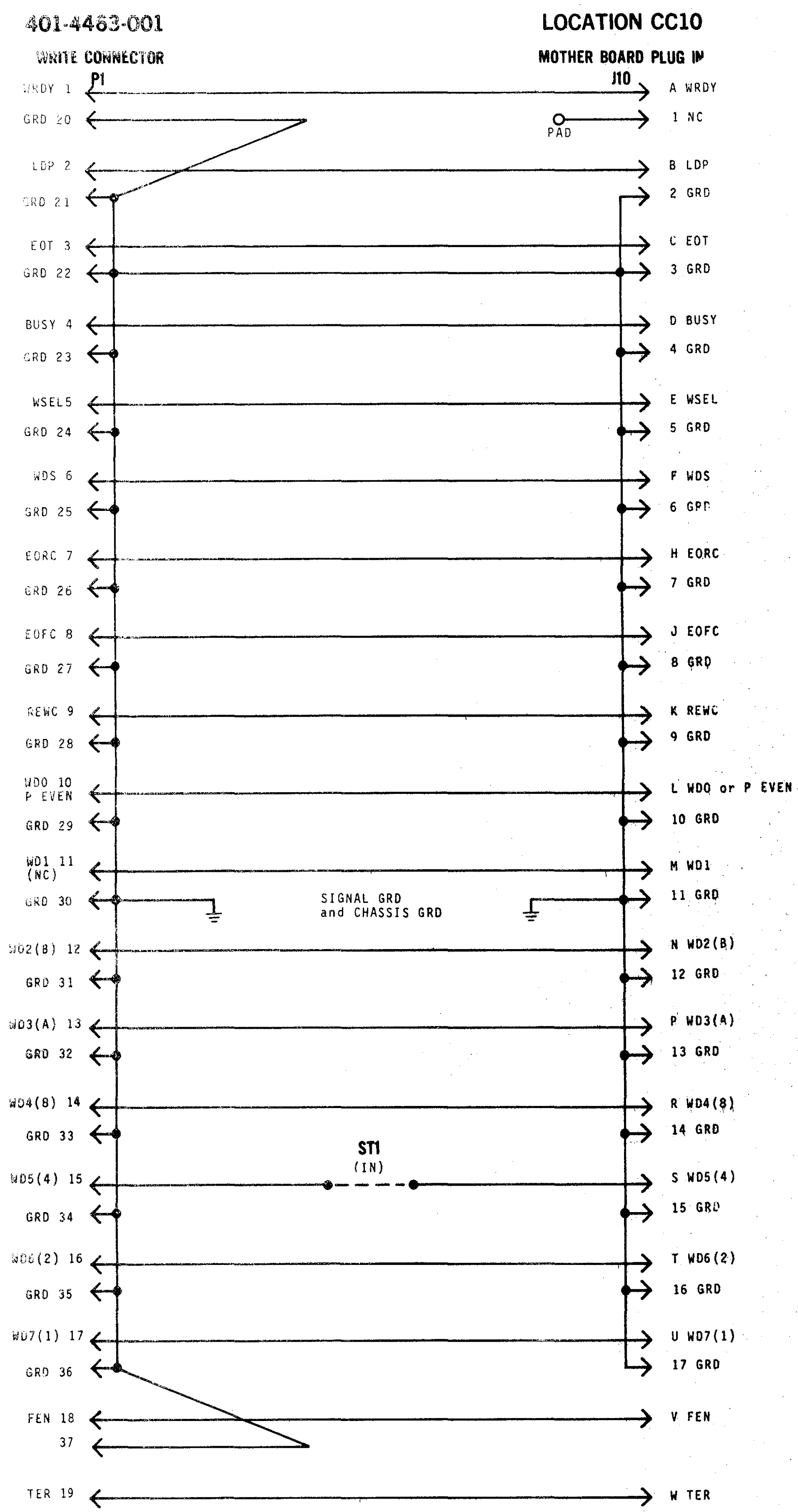
NOTES: UNLESS OTHERWISE SPECIFIED

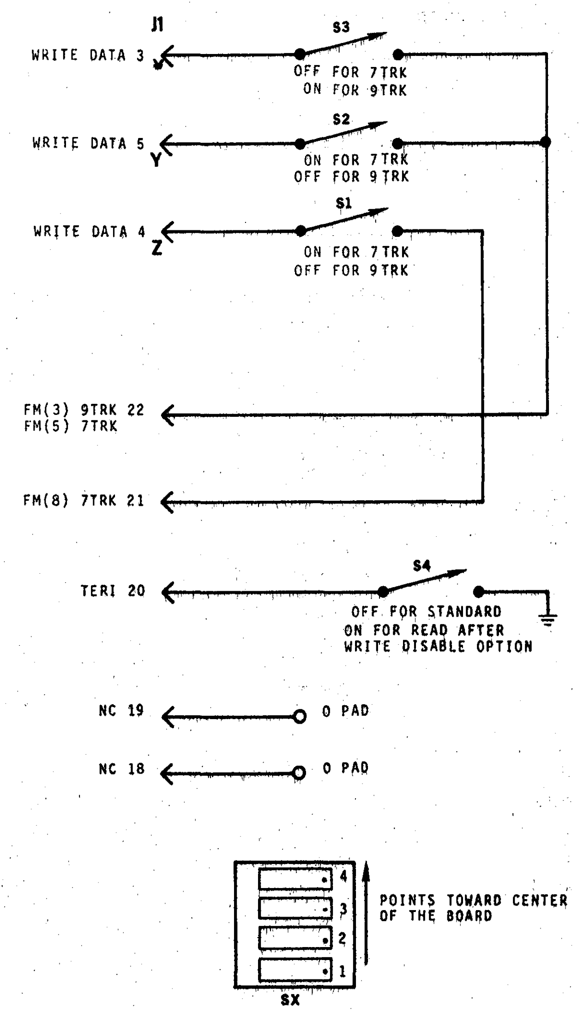
1. RESISTOR VALUES IN OHMS, FIXED COMP, 1/4W.
2. CAPACITOR VALUES IN MICROFARADS.
3. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.
4. ALL DIODES ARE TYPE 1N914.
5. ▽ DENOTES TEST POINT.

DASH NO.	001C	002B
FIRST USED ON	8230	8230
SPEED		
DENSITY		
IC5,22,23	MC852P	AS
IC10	MC862P	AS
IC15	MC857P	AS
IC20	MC839P	AS

AS=AS SHOWN

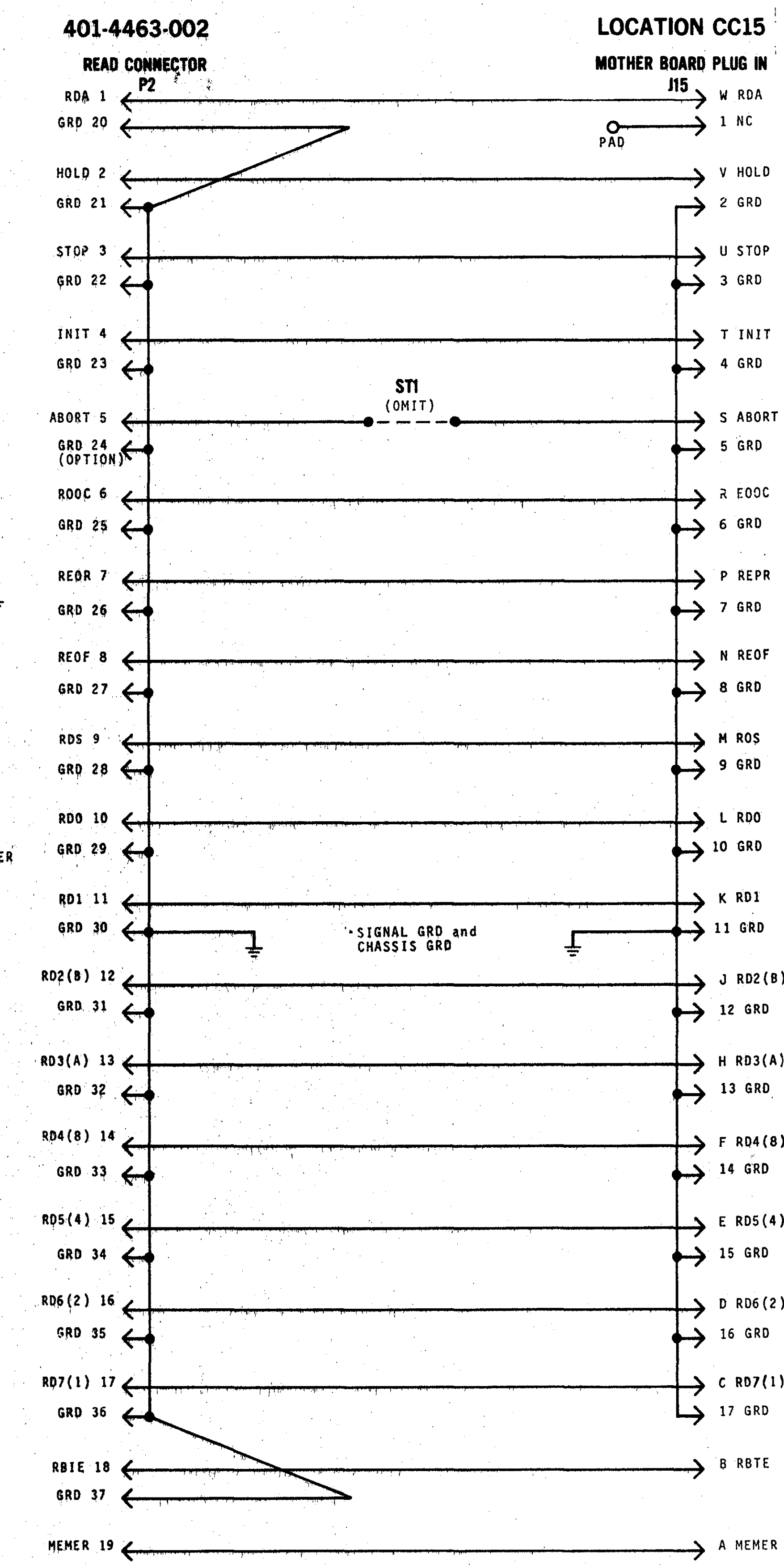
Read Skew Delay/Gap Detect, Type 3641
Schematic Diagram

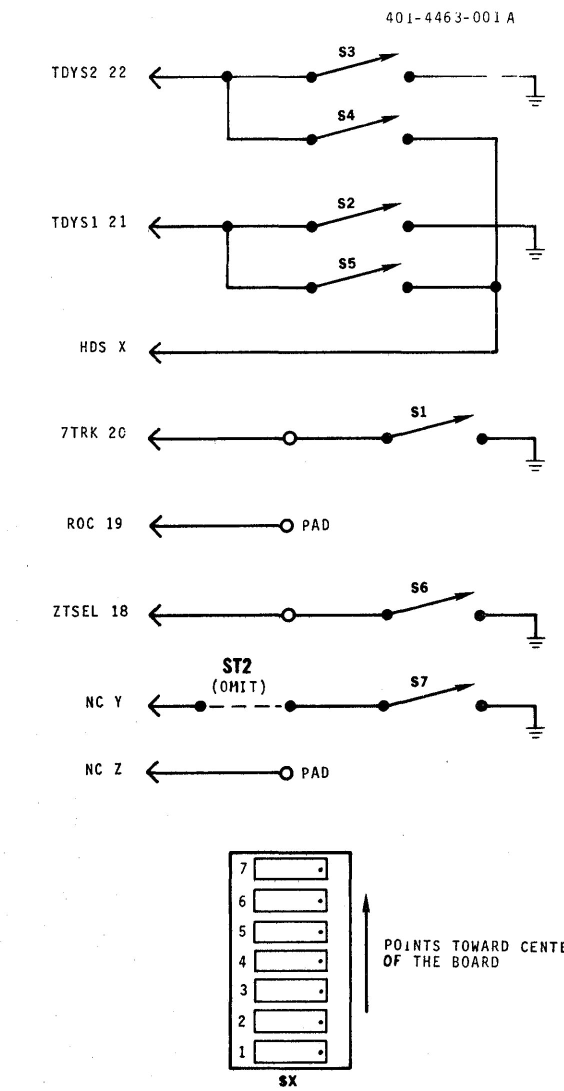




SX INSTALLED AS SHOWN ON SILK SCREEN

OPTION on SYNCHRONOUS DECK	S2	S3	S1	S4
9TRK	OFF	ON	OFF	
7TRK	ON	OFF	ON	
ERROR DISABLE				ON





SX INSTALLED AS SHOWN ON SILK SCREEN

FUNCTION	S1	S6
7TRK	ON	
9TRK	OFF	
ZTSEL		ON

TDYS1	TDYS2	DENSITY
H	H	200
H	L	556
L	H	800

DECK	DENSITY	S2	S3	S4	S5
200/556	200 556	OFF OFF	OFF ON	OFF ON	OFF OFF
556/800	556 800	OFF ON	ON OFF	OFF OFF	OFF ON
800(9TRK)	800	OFF	OFF	OFF	ON

Connector Board, Type 4463-001,2, Schematic Diagram

SECTION VII
GENERAL INFORMATION AND APPENDIX

SIGNAL	DEFINITION	SOURCE	DESTINATION
ACLK	A MEMORY CLOCK	3607	3638
ACTR1	A MEMORY COUNTER OUTPUT	3607	3516
ACTRP	A MEMORY COUNTER PULSE	3516	3616, 3607
ARI	A MEMORY READ IN	3516	3817, 3638
AROA	A MEMORY READOUT AVAILABLE	3516	3618, 3607
ARST	A MEMORY COUNTERS RESET	3616 + 3817	3607
BCLK	B MEMORY CLOCK	3607	3638
BCTR1	B MEMORY COUNTER OUTPUT	3607	3516
BCTRP	B MEMORY COUNTER PULSE	3516	3616, 3607
BOT2	GATED BEGINNING OF TAPE OUTPUT	3578	INTERFACE J1
BRI	B MEMORY READ IN	3516	3607
BROA	B MEMORY READOUT AVAILABLE	3516	3618, 3607
BRST	B MEMORY COUNTERS RESET	3616 + 3817	3607
BSF	BACKSPACE FLIP-FLOP	3633	3616, 3817
BSP	BACKSPACE COMMAND	3633	3616, 3817
BSY2	GATED BUSY OUTPUT	3516	INTERFACE J1
BUSY	MEMORY BUSY	3516 + 3633	3640
CRC	CRC STATUS	3633	3616
CRCA	CRC REGISTER TOGGLE PULSE	3616	3578
CRCB	CRC CLOCK PULSE	3616	3578
CRCB	CRC CLOCK PULSE	3578	3639
CRCR(P)	CRC REGISTER WRITE CHANNEL P	3639	3578
CRCR(0)	CRC REGISTER WRITE CHANNEL 0	3639	3578
CRCR(1)	CRC REGISTER WRITE CHANNEL 1	3639	3578
CRCR(2)	CRC REGISTER WRITE CHANNEL 2	3639	3578
CRCR(3)	CRC REGISTER WRITE CHANNEL 3	3639	3578
CRCR(4)	CRC REGISTER WRITE CHANNEL 4	3639	3578
CRCR(5)	CRC REGISTER WRITE CHANNEL 5	3639	3578
CRCR(6)	CRC REGISTER WRITE CHANNEL 6	3639	3578
CRCR(7)	CRC REGISTER WRITE CHANNEL 7	3639	3578
CRCTP	CRC TIME PULSE	3578	3639
DEN3	GATED DEVICE ENABLE	3660	3578, 3616, 3817, 3633, 3607, 3638
DTA1(0)	INPUT WRITE DATA CHANNEL 0	INTERFACE J1	3638
DTA1(1)	INPUT WRITE DATA CHANNEL 1	INTERFACE J1	3638
DTA1(2)	INPUT WRITE DATA CHANNEL 2	INTERFACE J1	3638
DTA1(3)	INPUT WRITE DATA CHANNEL 3	INTERFACE J1	3638
DTA1(4)	INPUT WRITE DATA CHANNEL 4	INTERFACE J1	3638
DTA1(5)	INPUT WRITE DATA CHANNEL 5	INTERFACE J1	3638
DTA1(6)	INPUT WRITE DATA CHANNEL 6	INTERFACE J1	3638
DTA1(7)	INPUT WRITE DATA CHANNEL 7	INTERFACE J1	3638
DTA1(P)	INPUT WRITE DATA CHANNEL P	3640	3638
EOF2	GATED END OF FILE COMMAND	3516	3616, 3633
EOF COMMAND	END OF FILE COMMAND	INTERFACE J1	3516
EORX	SEE EORA OR EORB		
EOT	END OF TAPE OUTPUT	TRANSPORT J3	3578
EOT2	GATED END OF TAPE OUTPUT	3578	INTERFACE, 3618
FEN	FORMATTER ENABLE	INTERFACE J1	3660
FM(3)(1)	WRITE FILE MARK CHANNEL (3-9TR)(1-7TR)	3616	3642
FM(6)(2)	WRITE FILE MARK CHANNEL (6-9TR)(2-7TR)	3616	3642
FM(7)(4)	WRITE FILE MARK CHANNEL (7-9TR)(4-7TR)	3616	3642
FM(8)	WRITE FILE MARK CHANNEL (8-7TR)	3616	3642
FMCLK	MASTER CLOCK	3640	3641
FREST	FORMATTER RESET	3817 + 3618	3616, 3641
FPT	FILE PROTECT	TRANSPORT J	3578
FWC0	OUTPUT WRITE DATA CHANNEL 0	3642	TRANSPORT
FWC1	OUTPUT WRITE DATA CHANNEL 1	3642	TRANSPORT
FWC2	OUTPUT WRITE DATA CHANNEL 2	3642	TRANSPORT
FWC3	OUTPUT WRITE DATA CHANNEL 3	3642	TRANSPORT

SIGNAL	DEFINITION	SOURCE	DESTINATION
RDY	READY STATUS	3002	3578
RDY2	GATED READY OUTPUT	3578	INTERFACE
REOF	READ END OF FILE	3817	INTERFACE J2
REOR2	READ END OF RECORD 2	3618 + 3633	3516, 3817
REOR2	READ END OF RECORD 2	3817	3516
REOR3	READ END OF RECORD 3	3618	INTERFACE J2
REST	REST STATE	3633	3578, 3640, 3616, 3817
REST2	GATED REST OUTPUT	3578	3639
REW2	GATED REWIND COMMAND	3516	3002, 3660 AS RWC
REW3	REWIND 3	3660	TRANSPORT J3
REWIND COMMAND	REWIND COMMAND	INTERFACE J1	3516
RFRMA	READ FRAME A	3607	3618
RFRMB	READ FRAME B	3607	3618
RGAP	READ GAP	3633	3817, 3618
RO	READ OUT STATE	3633	3616, 3607, 3578, 3817
RO2	GATED READ OUT STATUS	3578	3639
ROA	READ OUT MEMORY A	3516	3607, 3616, 3817
ROB	READ OUT MEMORY B	3516	3607, 3616, 3817, 3618
ROC	READ OUT MEMORY C	INTERFACE J2	3660
ROCLK	READ OUT CLOCK	3633	3616, 3660
ROCLK2	READ OUT CLOCK 2	3660	3607
ROCOMP	READ OUT COMPLETE PULSE	3633	3660
ROCOMP2	READ OUT COMPLETE PULSE 2	3618 + 3660	3516, 3616
ROEN	READ OUT ENABLE	3607	3660
ROEN2	READ OUT ENABLE 2	3660	3633
ROOC	READ OUT ONE CHARACTER	INTERFACE J2	3660
ROOC2	READ OUT ONE CHARACTER 2	3660	3618
ROOSC	READ OUT OSCILLATOR	3640	3616
ROSRT1	READ OUT START 1	3633	3817
ROSRT1A	READ OUT START 1A	3618	3516
ROSRT2	READ OUT START 2	3516	3640, 3660
ROSRT3	READ OUT START 3	3660	3616
ROSRT4	READ OUT START 4	3618	3660
ROTP1	READ OUT TIME PULSE 1	3616	3633/3531
ROTP2	READ OUT TIME PULSE 2	3616	3633/3531, 3578
ROTP2	READ OUT TIME PULSE 2	3616	NOT USED
ROTP3	READ OUT TIME PULSE 3	3616	3633/3531
RSEL3	READ SELECT 3	3660	3618
RSEL3	READ SELECT 3	3660	3638
RTM1	READ TAPE MARK 1	3817	3618
RWD	REWIND STATUS	3002	3516
SFC	SYNCHRONOUS FORWARD COMMAND	3616	3002, 3618
SRC	SYNCHRONOUS REVERSE COMMAND	3616	3002
SRTD	START DELAY	3633	3817, 3660
SRTD2	START DELAY 2	3660	3607
SRTDF	END START DELAY	3633	3616
STOP	STOP	INTERFACE J2	3618
STPDF	END STOP DELAY	3633 + 3817	3616
STPDF2	END STOP DELAY 2	3817	3633
STPEOF	STOP ON END OF FILE	OPTIONAL TO 0	3618
SWS	SET WRITE STATUS	3640	3002
TER	TAPE ERROR	3633	NOT USED
TERI	TAPE ERROR DETECTION INHIBIT	3616 + 3817	3633

UPDATES AND MODIFICATIONS

In the continuing effort to improve the performance and reliability of our product line, the Kennedy Company occasionally incorporates changes in existing models. The changes incorporated since the manual was printed are described in this section. Your particular model may or may not include these changes. Should you wish to incorporate these changes it is advisable to contact our Customer Engineering Department regarding available retrofit kits and application information.

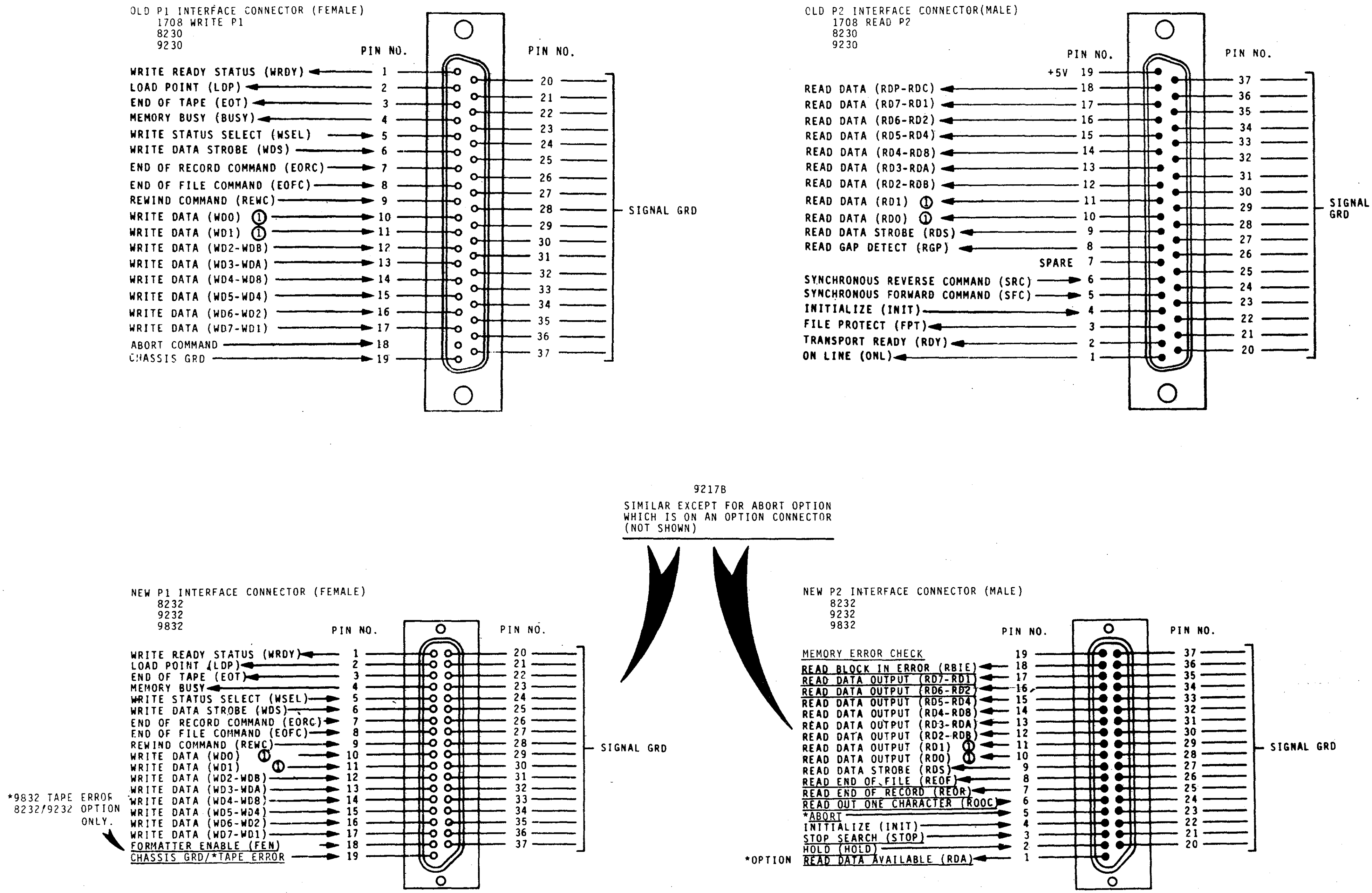
This section also describes any special features and modifications included in your model which distinguish it from the standard model described in the manual.

Model 8232/9232/9832 310-3023

This modification applies to systems where a Kennedy Model 8232, 9232, or 9832 tape transport is replacing a Kennedy Model 1708, 8230, or 9230 machine.

The old and new tape transport interface connectors are physically identical. However, the wiring has been changed to accommodate added or different signals. Therefore, the wiring from the interface to its connector must be changed to correspond to the new wiring pattern. Refer to the attached figure. The underlined signal functions are the ones that have changed.

NOTE:
WHEN SYSTEM UPDATE REQUIRES USE AND INSTALLATION OF THE FOLLOWING BUFFERED MODELS IN PLACE OF THE MODEL 1708 SERIES, NOTE THE CABLE DIFFERENCE AND INTERFACE ACCORDINGLY.



310-3023