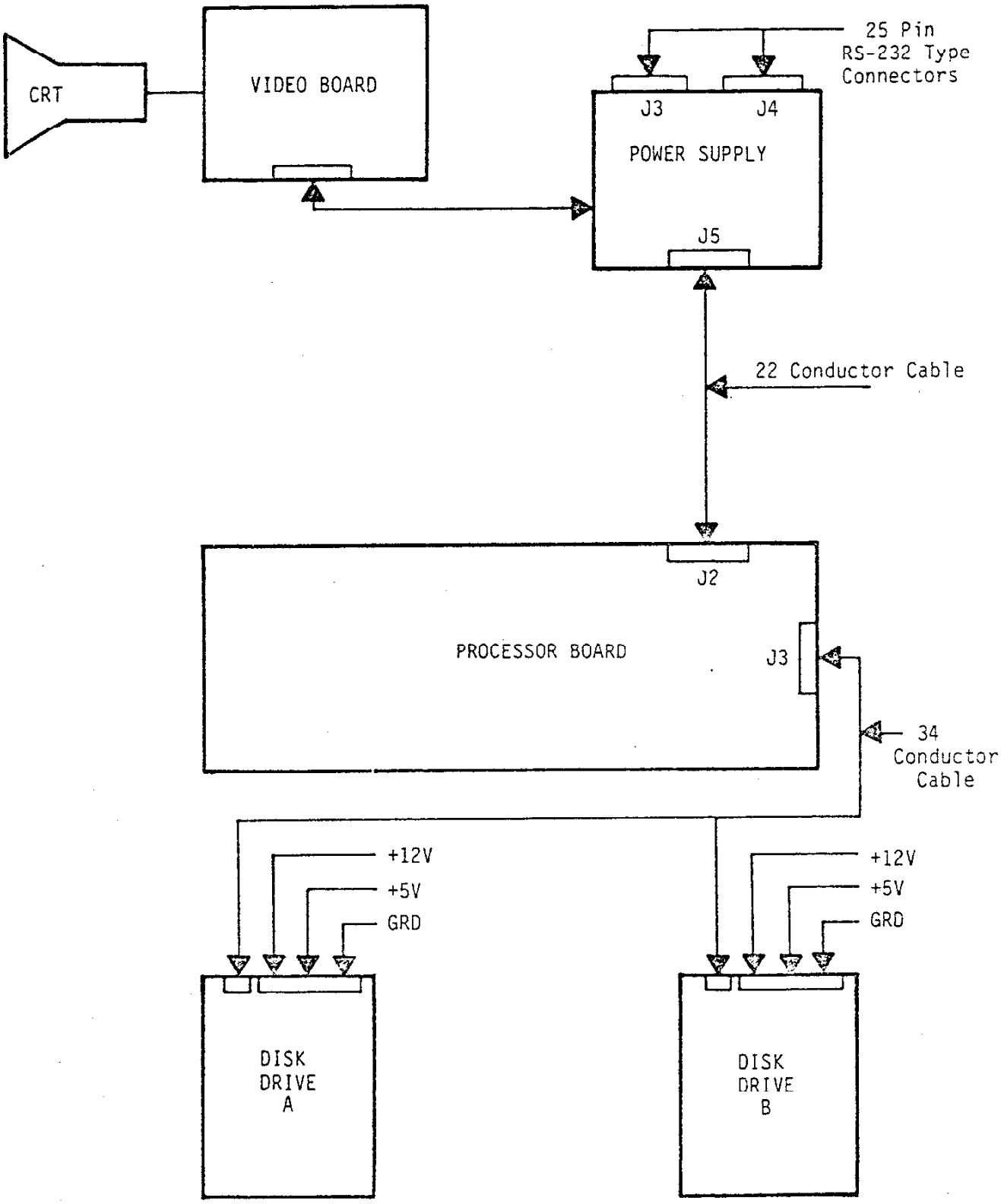
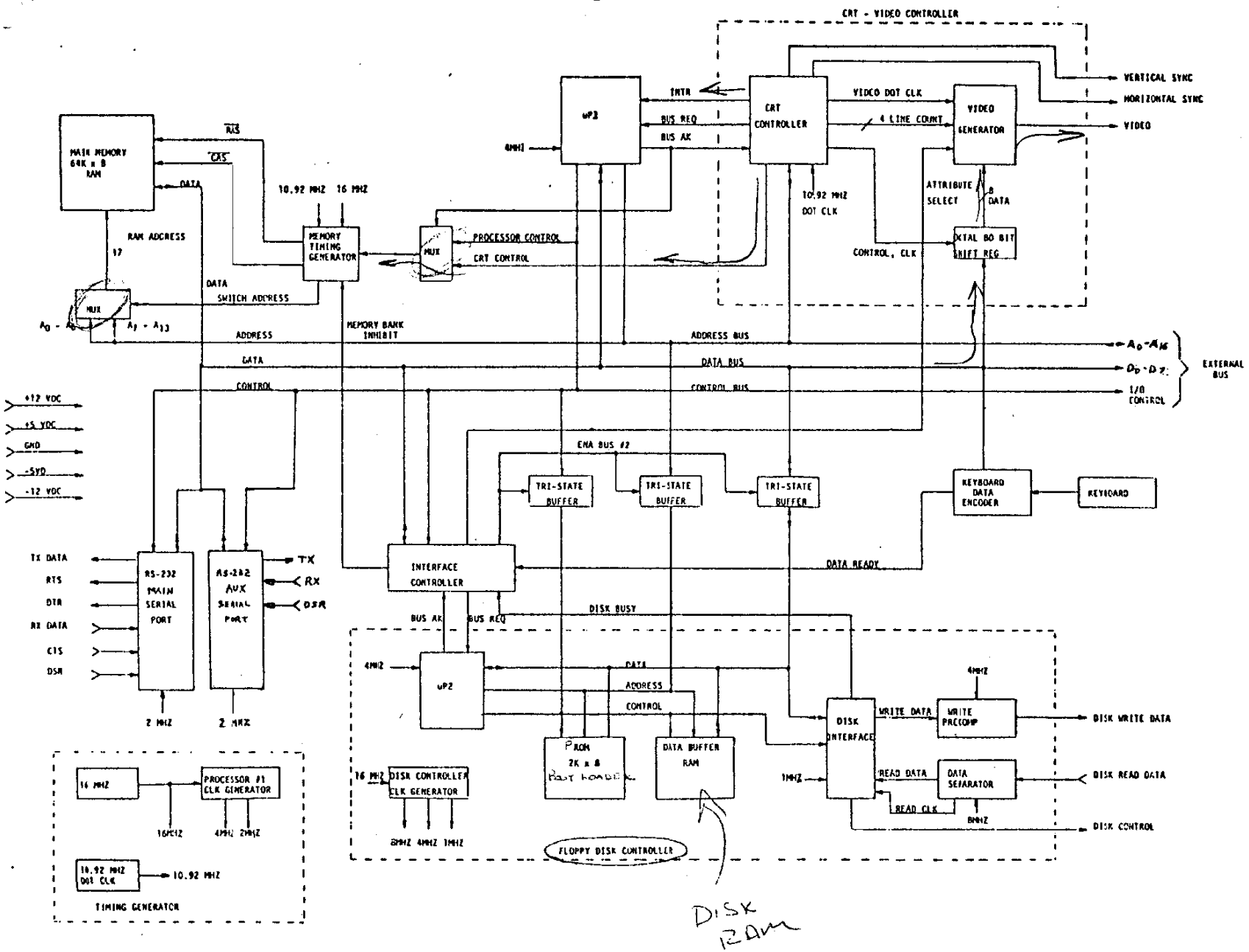
SUPERBRAIN GENERAL ARCHITECTURE





SUPERBRAIN KEYBOARD/CPU MODULE BLOCK DIAGRAM

CRT SCREEN ALIGNMENT PROCEDURES

1. ADJUST EXTERNAL BRIGHTNESS CONTROL FULLY CLOCKWISE.
2. ADJUST BRIGHTNESS POT. (R109) FOR A BACKGROUND RASTER.
3. ADJUST EXTERNAL CONTRAST COUNTER-CLOCKWISE UNTIL RASTER DISAPPEARS.
4. ADJUST CONTRAST POT. (R101) UNTIL THE DOT MATRIX OF CHARACTERS IS AS BRIGHT AS POSSIBLE WITHOUT DISTORTION.
5. ADJUST VERTICAL HEIGHT (R303) FOR ROUGHLY 1/2 INCH CLEARANCE TOP AND BOTTOM.
6. ADJUST VERTICAL LINIARITY (R307) UNTIL THE TOP, MIDDLE, AND BOTTOM ROW OF CHARACTERS ARE EQUAL IN HEIGHT.
7. ADJUST FOCUS POT. (R477) FOR A CLEAR, DISTINCT CHARACTER SET.
8. ADJUST HORIZONTAL WIDTH COIL (L403) FOR ROUGHLY 1/2 INCH CLEARANCE ON BOTH SIDES OF THE PICTURE.
9. ADJUST CENTERING RINGS LOCATED ON THE CRT YOKE TO ADJUST OVERALL PICTURE POSITION.
10. ADJUST HORIZONTAL CENTERING POT. (R410) FOR FINE ADJUSTMENT OF LEFT OR RIGHT POSITION.

Corporate Headquarters: 2300 Broad River Road, Columbia, South Carolina 29210 • 803/798-9100 • TWX: 810-666-2115

DATE OF THIS RELEASE May, 1981 PAGE 1 OF 15 BULLETIN # B051031

ASSEMBLY NAME/NUMBER DIAGNOSTIC DISKETTE DA1 PRODUCT CompuStar 20,30 (Stand-Alone) SuperBrain, SuperBrain QD

REFERENCE ECO # DISTRIBUTED TO B,C,D,F,G,I APPROVED TMO

DIAGNOSTIC DISKETTE

The Diagnostic Diskette is designed to aid in determining service problems with Intertec microcomputer systems. The diskette contains several programs which test various aspects of the computer's operation. These programs do not completely test everything on the computer, but allow quicker diagnosis of module failures. The programs contained on this diskette will test the following:

- Main Memory RAM
- MAIN and AUXILIARY Serial Ports
- Both Diskette Drives A and B
- Video Alignment

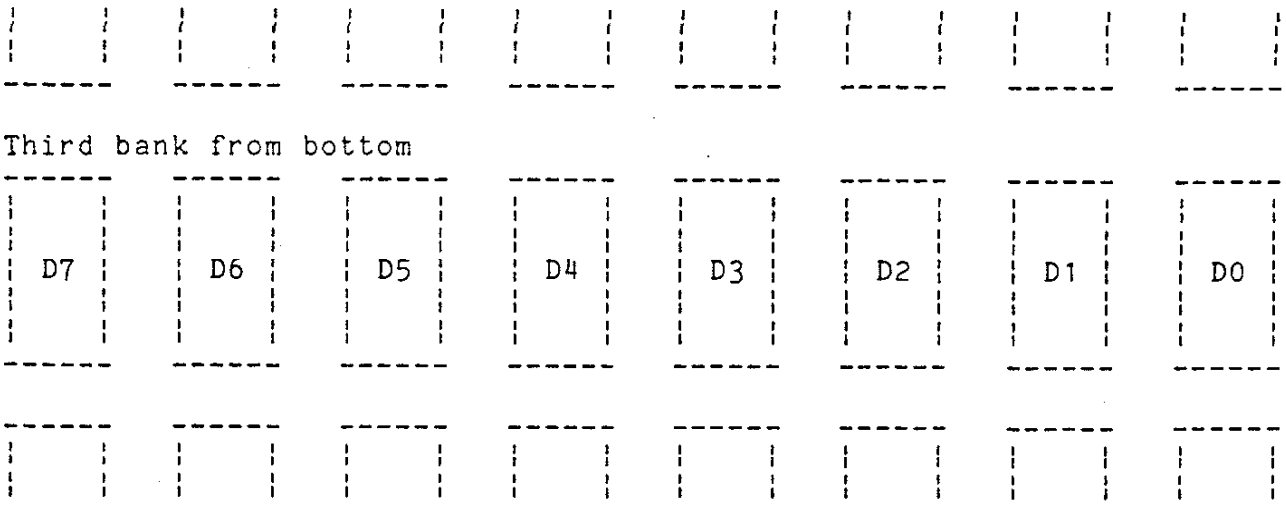
The testing procedures should be performed in conjunction with the flowchart included in this technical bulletin. This will insure that the modules are tested in the proper sequence and will eliminate unnecessary test time. Also included in this documentation are descriptions of the test programs and procedures. These should be read before attempting to use the test diskette.

You should test each module in the order given. After each module checks out satisfactorily, then proceed to the next module. If the test programs do not detect the malfunctioning module, then contact the Product Services Department at Intertec's Corporate Headquarters.

RAM TEST PROGRAM (Item #5 in the flowchart)

The purpose of the RAM test program is to insure that the random access memory is fully operational. The test will write and read binary patterns throughout the memory banks to verify the read/write operation . Failure by the test indicates that the RAM is defective and must be replaced by a factory-trained service technician.

There are four banks of memory on the processor board (only two banks for 32K systems). The lowest bank is addressed from 0000H to 3FFFH, the second bank from 4000H to 7FFFH, the third bank from 8000H to BFFFH, and the fourth bank from C000H to FFFFH. Upon failure, the test will display the address of the failure, the hexadecimal representation of the binary pattern that was written, and the pattern that was read back. The pattern must be converted to binary to locate the actual RAM chip that was defective. For example, the test indicates the following failure message: TESTING RAM BANKS 8000 0005 0004. 8000 is the failure address, so it is in the third bank from the bottom. The binary representation for 0005H is 0000 0101, and for 0004H it is 0000 0100. Therefore, the least significant bit was lost upon read back, and the chip corresponding to D0 is defective, and must be replaced.



PORT TEST PROGRAM (Item #6 in the flowchart)

This program is designed to test the send and receive functions of the MAIN and AUXILIARY ports. The program will perform a test of the ports by sending data from one port to the other. An error occcurs when the data sent does not match the data received.

To use the port test program, you must have the port test loop cable interconnecting the MAIN and AUX ports (see next sheet). After you have properly attached the loop cable, the port test is initiated by the following command :

PORTTEST (cr)

The following is a sample run of the port test program. Note that reference to switches means the small five-position dip switch on the upper right corner of the processor board.

A>PORTTEST (cr)

RS232 PORT TEST VER 3.0 FOR CP/M 2.2
TURN SWITCH POSITIONS 3,4 OFF
TURN SWITCH POSITIONS 1,2,5 ON (test of synchronous communication)
RETURN TO CONTINUE (cr)
RI OK
DSR OK
TESTING MAIN PORT TO AUX PORT
TESTING AUX PORT TO MAIN PORT

TURN SWITCH POSITIONS 1,2,5 OFF
TURN SWITCH POSITIONS 3,4 ON (test of asynchronous communication)
RETURN TO CONTINUE (cr)
TESTING MAIN PORT TO AUX PORT
TESTING AUX PORT TO MAIN PORT
PORT TEST COMPLETE
RETURN TO CONTINUE (cr)

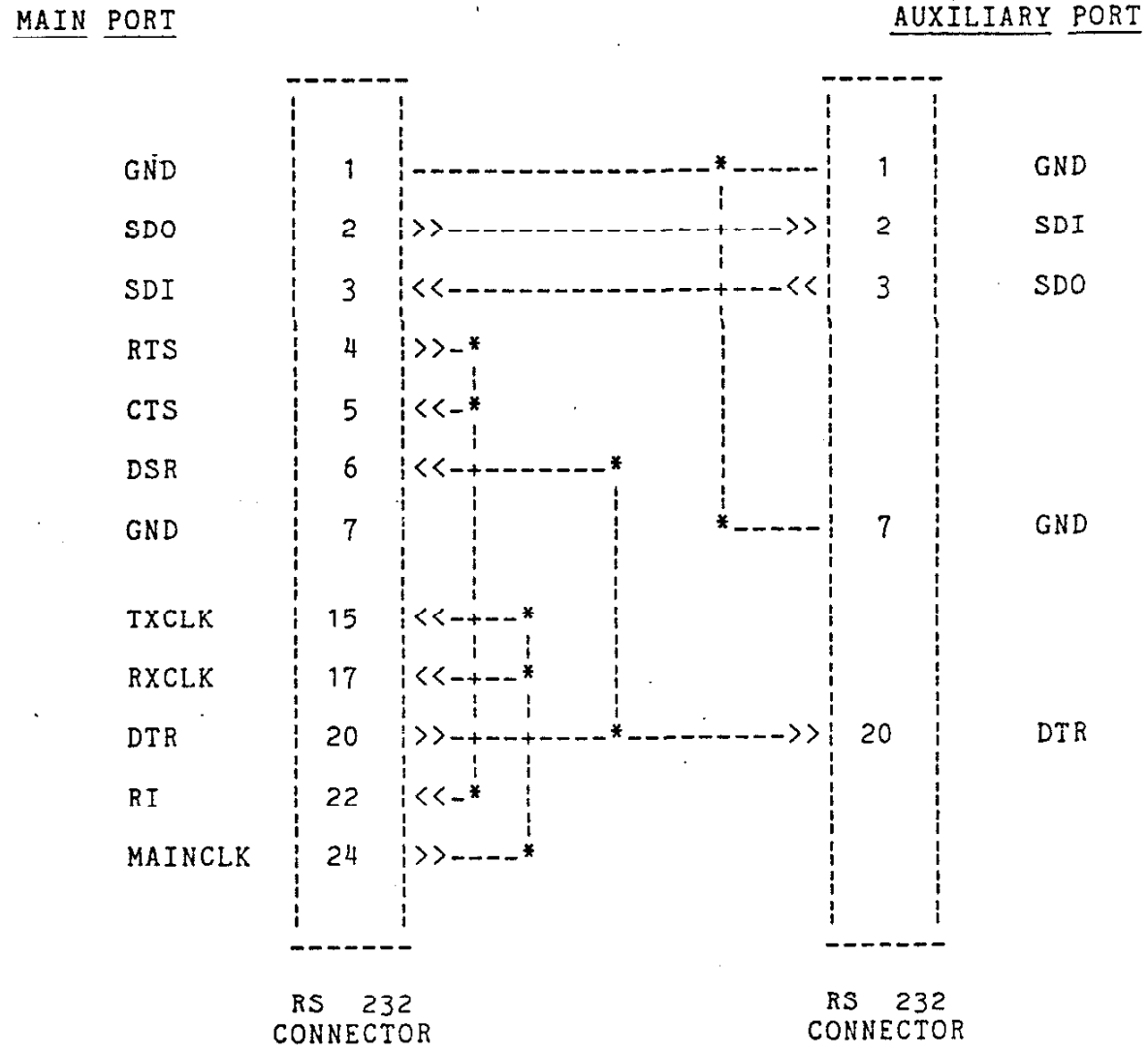
(E - INDICATES ERROR)
.....
.....

.....
.....

If an error occurs, the program will either lock up or will display an error indicator in the place of the dots. Refer to the flowchart for proper action.

PORT TEST INTERCONNECT CABLE

FOR SUPERBRAIN DOS 3.0 WITH CP/M 2.2



Note - * means lines are connected
+ means lines are not connected

DISK TEST PROGRAM (Item #7 in the flowchart)

The purpose of this program is to test the ability of each disk drive to read and write track and sector information. The program will test both drives and present a summary of test activity upon completion. The program will permit both double density and quad density disk drives to be tested. Requirements for the test are two diskettes of good quality that have been previously formatted. An error occurs when the disk drives are unable to write and verify any step of the test process. Error messages might be the following:

*** crc error ***

Bdos Err on A: (or B:)

*** disk not ready ***

Should excessive numbers of these errors occur and you are certain that the media is of good quality, replace the disk drive that indicates the error. Please note that some errors may occur because of minute media flaws. Therefore, if more than ten errors are detected, then drive replacement is necessary. A sample run of the disk format program follows.

A>DISKTEST (cr)

SuperBrain Disk Exerciser Program
(C) Copyright Intertec Data Systems 1981

Checking Single or Double Sided System ? (S/D): D
Double Sided Disk Exerciser

Start-of-test. Place formatted disks in drives A and B.
Hit RETURN when ready: (cr)

Testing drive A.
Track number : 0034
Testing drive B.
Track number : 0034

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ENGINEERING CHANGE ORDER
IDS - 8104

19

SUBJECT Addition of Data Terminal Ready (DTR) RS-232-C Signal to Pin 20 on Aux Port

PRODUCT SuperBrain DATE 02/22/80 ECO # E02008 PAGE 1 OF 1

ASSEMBLY NAME/NUMBER Keyboard/CPU Module Rev. 1

BACKGROUND AND IMPLEMENTATION INFORMATION:

In order to implement the Data Terminal Ready (DTR) input signal on the Auxiliary RS232C Port of the SuperBrain, the following modification should be implemented with all production effective February 25, 1980.

PRODUCTION:

1. Cut Z60-22 (8251)
2. Add wire (track side) Z60-22 (on IC) to Z67-11 (1489).
3. Add wire (track side) Z67-13 to J2-12.

PRODUCTION TEST:

Final QA:

Use updated port test to electrically verify this change (contact Engineering).

See reverse side for additional information

THIS ENGINEERING CHANGE ORDER AFFECTS:

IDS-913A

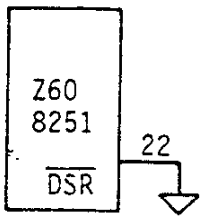
☐ MATERIAL(S)/COMPONENTS(S) USED ☐ PACKAGING/SHIPPING ☐ OTHER

☒ PRODUCTION PROCEDURES ☒ SERVICING/PROCEDURES

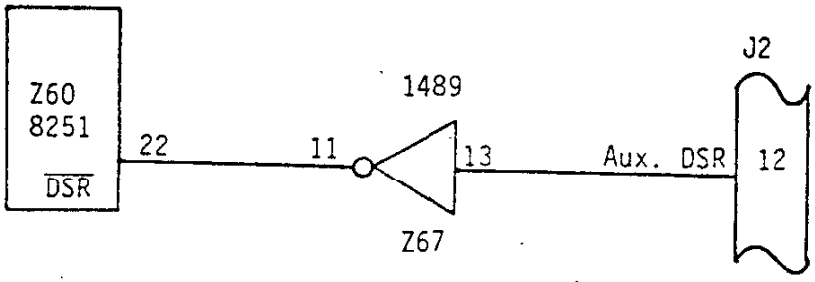
20

THIS CHANGE ~~AFFECTS~~: Allows use of Pin 20 on Aux. Port (DTR) to control data transmission from Aux. Port.

CHANGE FROM:



CHANGE TO:



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- ☒ FIELD SERVICE
- ☒ CUSTOMER LIST
- ☐ CUSTOMER AS REQUESTED

KIT AND ORDERING INFORMATION

KIT AVAILABLE? ☐ YES ☒ NO

KIT NUMBER

PRICING:

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Earlier Supplies

ENGINEERING CHANGE ORDER
IDS - 910A

21

SUBJECT Resistor Removal

PRODUCT SuperBrain DATE 2/27/80 ECO # E02009 PAGE 1 OF 1

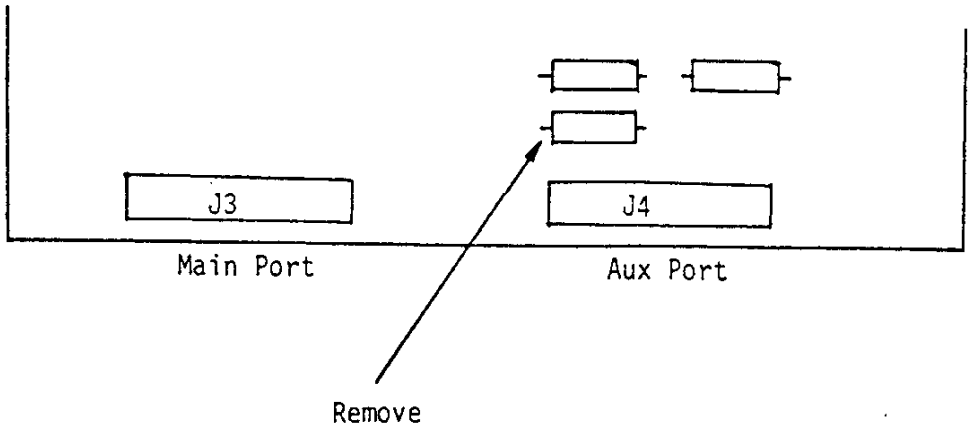
ASSEMBLY NAME/NUMBER Power Supply Rev. 4

BACKGROUND AND IMPLEMENTATION INFORMATION: RE: ECO E02008

PRODUCTION:

Implement on all SuperBrain assemblies using DOS Version 2.2 and up.

Remove 220 ½w resistor from J4-20 (AUX PORT) as shown below.



See reverse side for additional information

THIS ENGINEERING CHANGE ORDER AFFECTS:

IDS - 5104

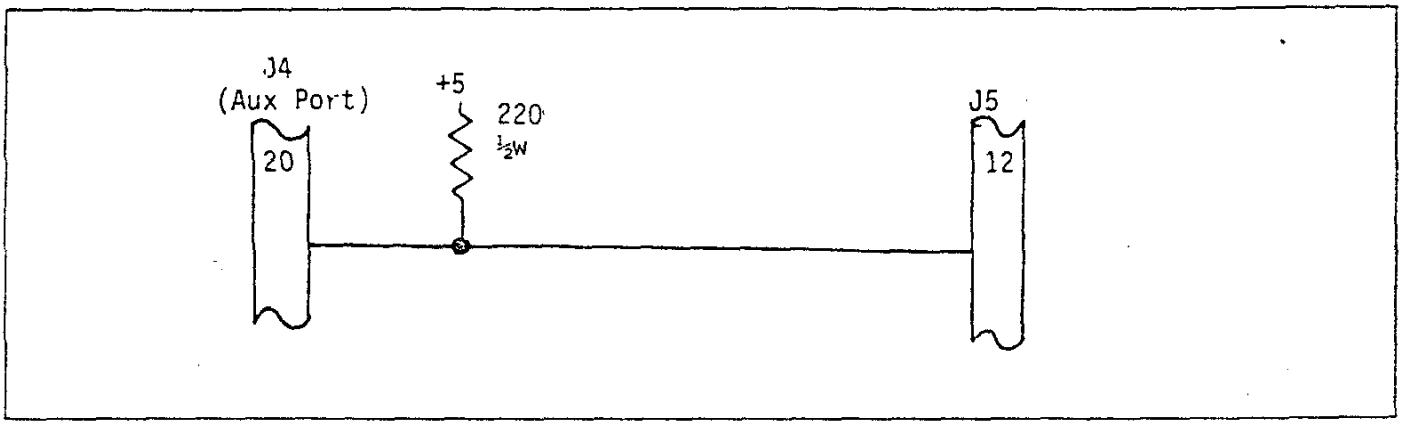
☐ MATERIAL(S)/COMPONENTS(S) USED ☐ PACKAGING/SHIPPING ☐ OTHER

☐ PRODUCTION PROCEDURES ☐ SERVICING/PROCEDURES

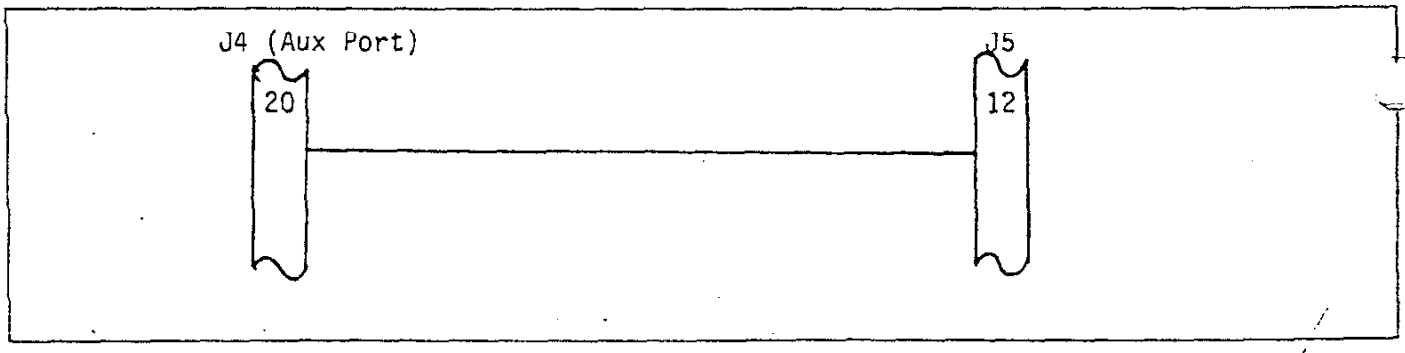
22

THIS CHANGE ~~XXXXXXXXX~~: Allows DSR signal to function properly

CHANGE FROM:



CHANGE TO:



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KIT AND ORDERING INFORMATION

KIT AVAILABLE? ☐ YES ☒ NO

KIT NUMBER

PRICING:

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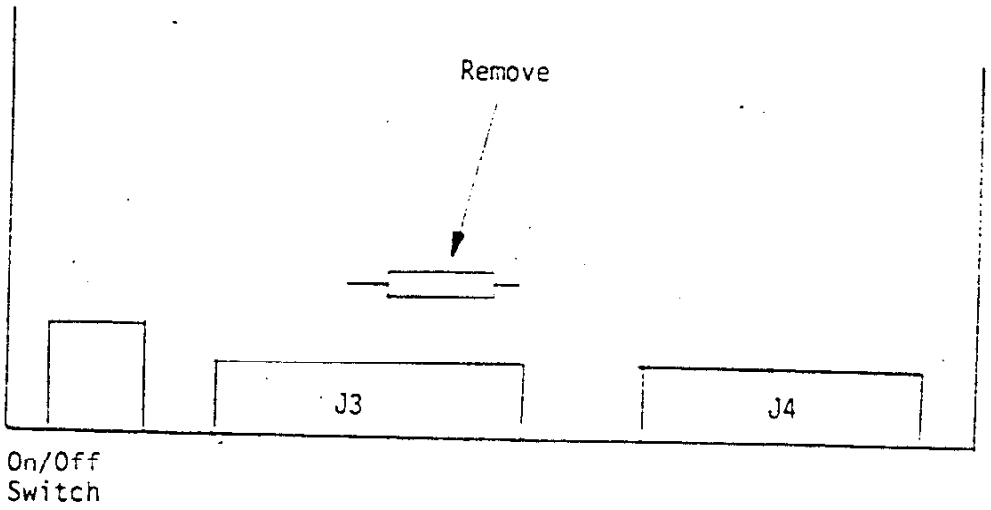
SUBJECT Resistor Removal

PRODUCT SuperBrain DATE 1/17/80 ECO # SB011780 PAGE 1 OF 1

ASSEMBLY NAME/NUMBER Power I/O Board 1424002-04 Rev. 04

BACKGROUND AND IMPLEMENTATION INFORMATION:

Remove 220Ω resistor from DTR signal (J3-20). This resistor should only be removed from power I/O boards used in SuperBrain assemblies.



Ful-Vu Pul-Pruf Protector RF3-11 Lightweight

DATA SYSTEMS
Corporate Headquarters. 2300 Broad River Road, Columbia, South Carolina 29210 • 803/798-9100 • TWX: 810-666-2115

REV 1

SUBJECT INTERMITTENT TRANSMISSION AND LOSS OF POWER AT THE AUXILIARY PORT

PRODUCT SUPERBRAIN DATE APRIL 25, 1980 ECO # E040010 PAGE 1 OF 2

ASSEMBLY NAME/NUMBER KEYBOARD/CPU MODULE #1532000

BACKGROUND AND IMPLEMENTATION INFORMATION:

On early models of the SuperBrain, lockout of data and intermittent transmission on the auxiliary port may occur. This problem can be corrected by grounding Z60, Pin 17 (clear-to-send on the USART).

PRODUCTION: Incorporate on Revisions -00 and -01.

1) On the back of the Keyboard/CPU Module, locate Z60, Pin 17 (see diagram).

2) Carefully remove the solder mask from the track immediately to the right of Pin 17.

3) Bend Pin 17 over to contact the track and solder.

PRODUCTION TEST:

With an ohmmeter, check the connection to ensure grounding of Pin 17.

See reverse side for additional information

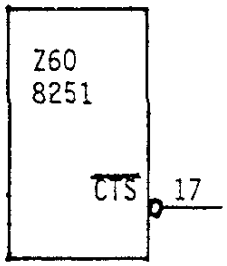
Ful-Vu Pul-Proof Protector RF3-11 Lightweight

☐ MATERIAL(S)/COMPONENTS(S) USED ☐ PACKAGING/SHIPPING ☐ OTHER

☒ PRODUCTION PROCEDURES ☐ SERVICING/PROCEDURES

THIS CHANGE PREVENTS: Intermittent transmission on the Auxiliary Port.

CHANGE FROM:



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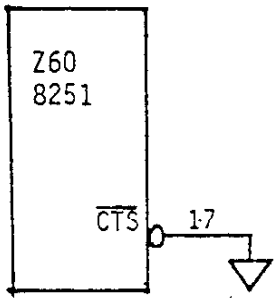

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- ☐ CUSTOMER AS REQUESTED

KIT AND ORDERING INFORMATION

KIT AVAILABLE? ☐ YES ☐ NO

KIT NUMBER N/A

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A. Programmable Peripheral Interface (IC8255)

Port A - Output - 68H
Port B - Input - 69H
Port C - Output - 6AH
Control Port - Output - 6BH
Mode - Ø

1. Control Port (PPICW)

Hex Address - 6BH
Control Word - 82H (1000$0011B)

8 Bit Breakdown

PCW Ø - Port C, Lower 4 bits
1 = Input; Ø = Output

PCW 1 - Port B
1 = Input; Ø = Output

PCW 2 - Mode Select
1 = Mode 1; Ø = Mode Ø

PCW 3 - Port C, Higher 4 bits
1 = Input; Ø = Output

PCW 4 - Port A
1 = Input; Ø = Output

PCW 5 & PCW 6 - Mode Select
ØØ = Mode Ø; Ø1 = Mode 1; 1X = Mode 2

PCW 7 - Mode Set
1 = Set; Ø = No Change

2. Port A (PPIA)

Hex Address - 68H
Program Word - 43H (0100$0011B)

8 Bit Breakdown

PAØ & PA1 - Mode Select
ØØ & Ø1 = Graphics; 1Ø = External; 11 = Alphanumeric

PA2 - Underline
1 = Set; Ø = Normal

PA3 & PA4 - Not used

PA5 - Strike through
1 = Set; Ø = Normal

PA6 - Operating Line Frequency
1 = 6ØHZ; Ø = 5ØHZ

PA7 - Reverse Video
1 = Reverse; Ø = Normal

3. Port B (PPIB)

Hex Address - 69H

8 Bit Breakdown

PBØ - Keyboard Encoder (Data Ready)
1 = Data Ready; Ø = No Character Present

PB1 - Keyboard Encoder (Any Key Out)
1 = AKO; Ø = No Key Hit

PB2 - CRT Controller (CRTC)
1 = Vertical Blank; Ø = Not Vertical Blank

PB3 - Not Used

PB4 - Capital Lock
1 = Normal; Ø = Set

PB5 - Disk Status
1 = Busy; Ø = Ready

PB6 - Main R. I.
1 = Normal; Ø = Set

PB7 - CPU2 $\overline{\text{BUSAK}}$
1 = Normal; Ø = Acknowledge

4. Port C (PPIC)

Hex Address - 6AH
Program Word - BØH (1011$0000)

8 Bit Breakdown

PCØ - Set CRT Controller
1 = Disable RAS for Bank Ø and Program CRTC
Ø = Normal RAM Addressing

PC1 - Character Blanking
1 = Set; Ø = Normal

PC2 - Tri-State Buffer Control (Address 0-8000H)
1 = Disable RAS for Bank Ø and Read EPROM
Ø = Disable EPROM and Enable RAM Bank Ø

PC3 - CPU2 Reset
1 = Reset; Ø = Normal

PC4 - Tri-State Buffer Control (Address 8000-FFFFH)
Ø = Enable Disk Buffer and Disable RAS for RAM Bank 2 (8000 TO BFFFH)
1 = Disable Disk Buffer and Enable RAS for Bank 2 (8000 TO BFFFH)

PC5 - CPU2 Bus Request
1 = Normal; Ø = Request

PC6 - Bell
1 = On; Ø = Off

PC7 - Keyboard Encoder (Data Ready)
1 = Normal; Ø = Reset

B. Other Ports of Interest

1. RS-232 Ports

Main In/Out Data - 58H
Main Status - 59H

Aux. In/Out Data - 40A
Aux. Status - 41A

2. BAUD Rate Port - 60H

a. Data Byte Example

EEH

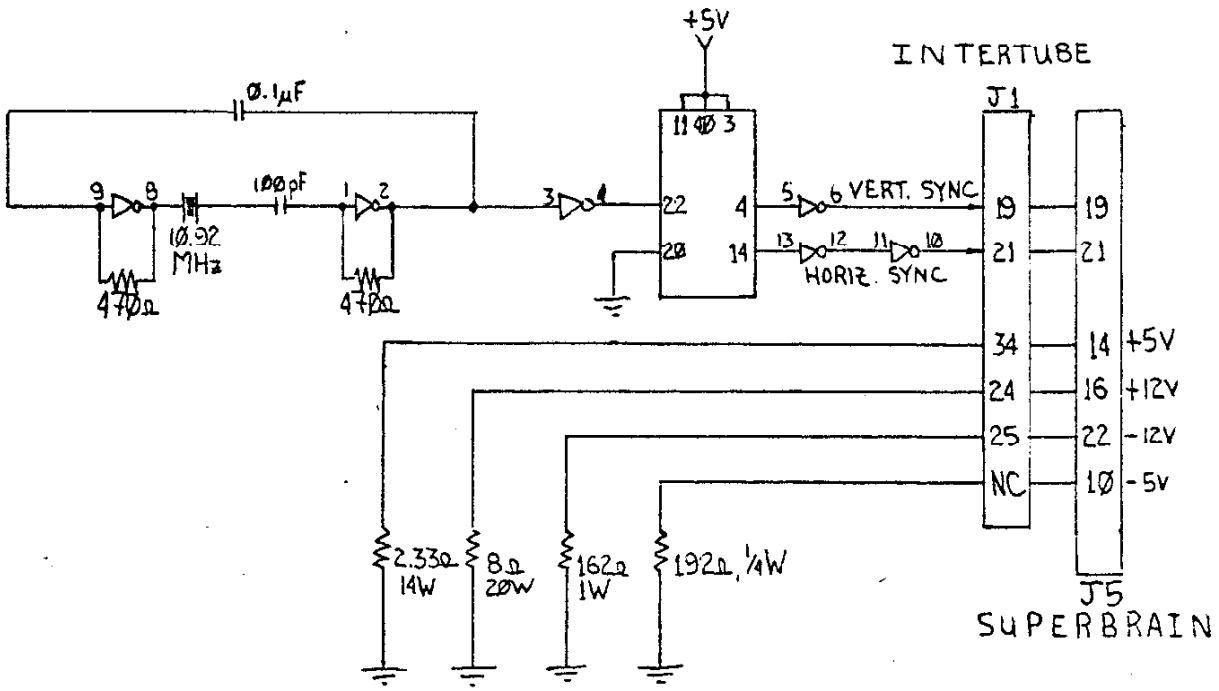
Least Significant Four Bits = Aux. BAUD Rate
Most Significant Four Bits = Main BAUD Rate

b. Four Bit Assignment versus BAUD Rate

ØH	=	50
5H	=	300
8H	=	1800
AH	=	2400
EH	=	9600

3. Character Ports

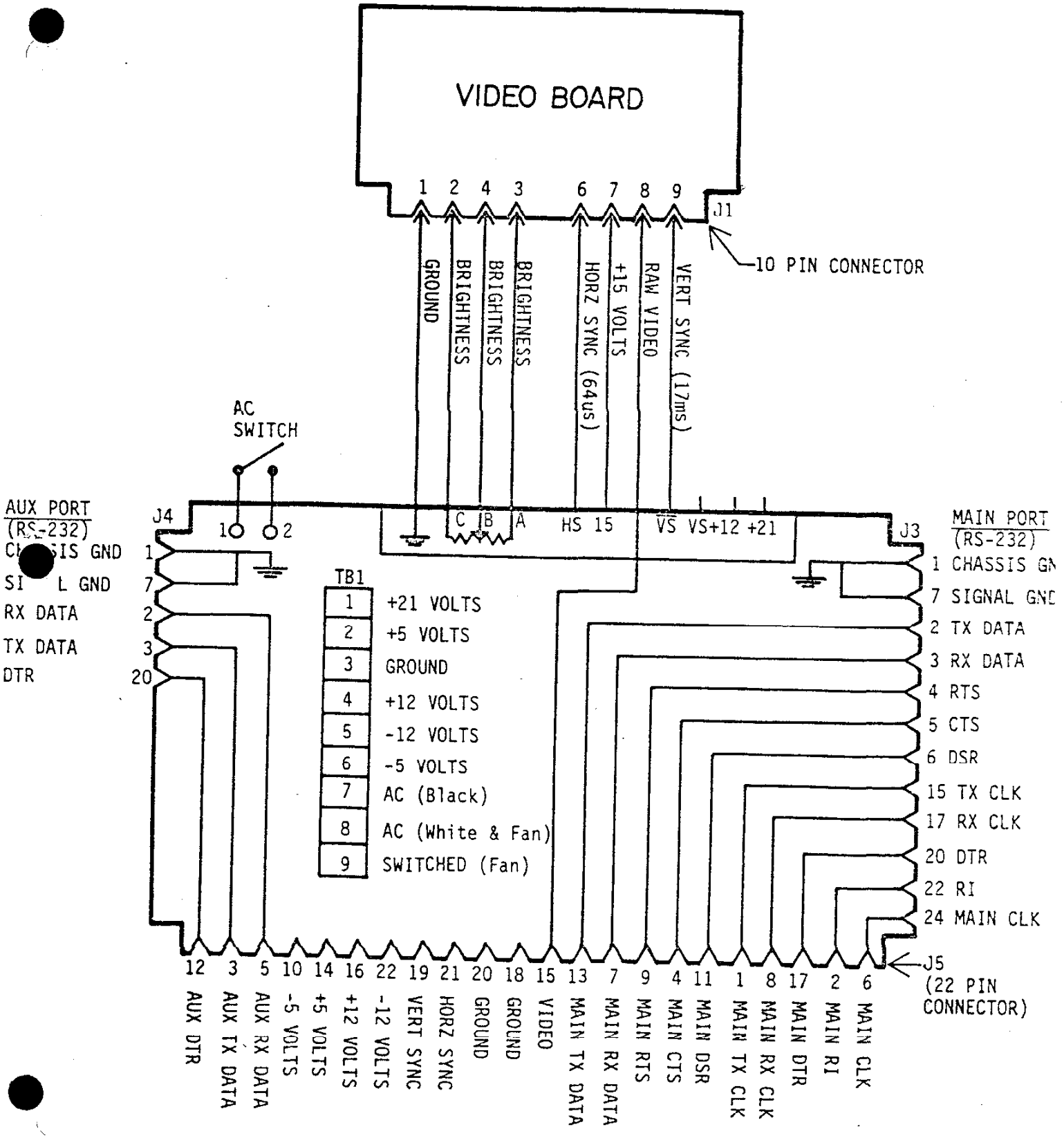
Character Interrupt Latch - 48H
Keyboard Character - 50H



1. ALL RESISTORS ARE ½ WATT UNLESS OTHERWISE SPECIFIED

2. LOAD RESISTORS ARE CALCULATED FOR MAXIMUM SUPERBRAIN LOAD (THE STANDARD INTERTUBE LOAD IS A LESSER VALUE)

INTERCONNECT DIAGRAM POWER SUPPLY/VIDEO BOARD



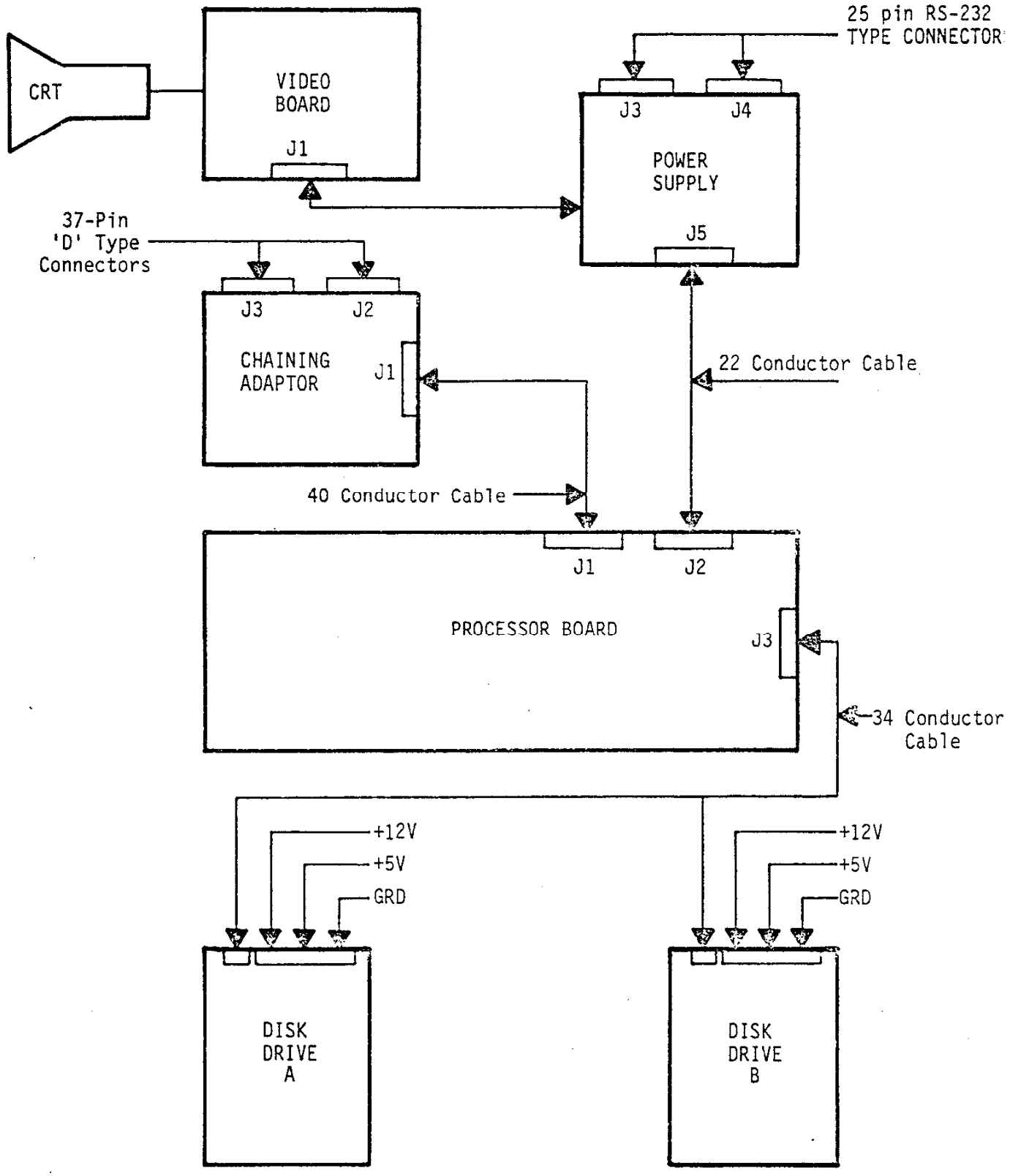
External ROM socket

The revision -01 and -01A CPU/Keyboard for the Superbrain contains a ROM socket which can be used in a variety of ways. Many customers that want to protect their software can program the ROM with specific serial numbers to be checked by the application software. The pin-out of the ROM is listed below:

pin of ROM	corresponding signal connection on the CPU
1	D4 of the Z-80
2	D5 of the Z-80
3	D6 of the Z-80
4	ground
5	D7 of the Z-80
6	A0 of the Z-80
7	A1 of the Z-80
8	A2 of the Z-80
9	A3 of the Z-80
10	A4 of the Z-80
11	chip select (I-O port 78 hex)
12	+ 5 volts
13	D0 of the Z-80
14	D1 of the Z-80
15	D2 of the Z-80
16	D3 of the Z-80

the organization of the ROM most likely is 32 x 8 .

VPU GENERAL ARCHITECTURE



Temp. Range
0°C to +70°C
0°C to +70°C
0°C to +70°C
0°C to +70°C
0°C to +70°C
0°C to +70°C
0°C to +70°C
0°C to +70°C
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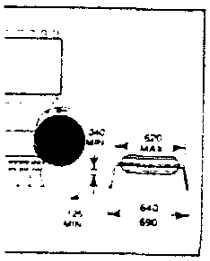
0°C to +70°C
0°C to +70°C
0°C to +70°C



PACKAGE

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TWX 910-595-1139

WESTERN DIGITAL
CORPORATION

BR1941 Dual Baud Rate Clock

FEBRUARY, 1981

FEATURES

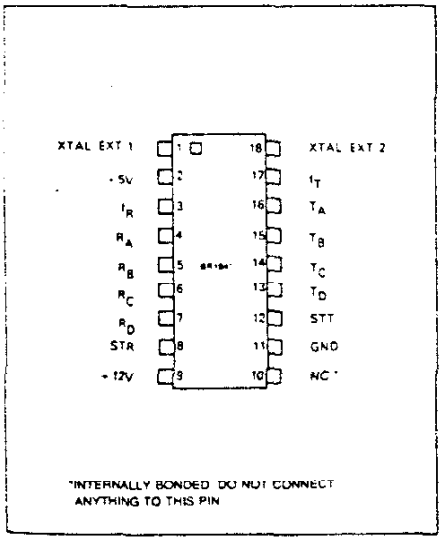
- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES
- DUAL SELECTABLE 16 X CLOCK OUTPUTS FOR FULL DUPLEX OPERATIONS
- OPERATES WITH CRYSTAL OSCILLATOR OR EXTERNALLY GENERATED FREQUENCY INPUT
- ROM MASKABLE FOR NON-STANDARD FREQUENCY SELECTIONS
- INTERFACES EASILY WITH MICRO-COMPUTERS
- OUTPUTS A 50% DUTY CYCLE CLOCK WITH 0.01% ACCURACY
- 18 PIN CERAMIC DIP PACKAGE
- 3 DIFFERENT FREQUENCY/DIVISOR PAIRS AVAILABLE

GENERAL DESCRIPTION

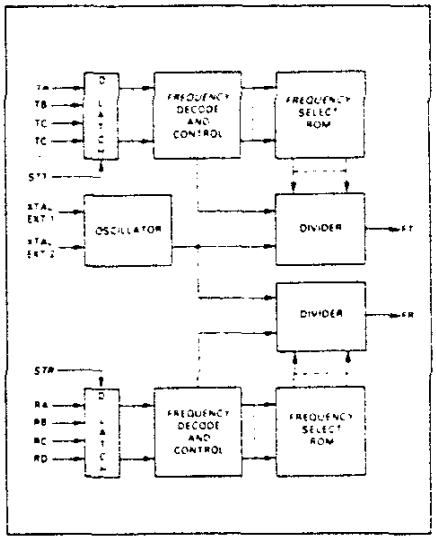
The BR1941 is a combination Baud Rate Clock Generator and Programmable Divider. It is manufactured in N-channel MOS using silicon gate technology. This device is capable of generating 16 externally selected clock rates whose frequency is determined by either a single crystal or an externally generated input clock. The BR1941 is a programmable counter capable of generating a division from 2 to $(2^{15}-1)$.

The BR1941 is available programmed with the most used frequencies in data communication. Each frequency is selectable by strobing or hard wiring each of the two sets of four Rate Select inputs. Other frequencies/division rates can be generated by reprogramming the internal ROM coding through a MOS mask change. Additionally, further clock division may be accomplished through cascading of devices. The frequency output is fed into the XTAL/EXT input on a subsequent device.

The BR1941 can be driven by an external crystal or by TTL logic.



PIN CONNECTIONS

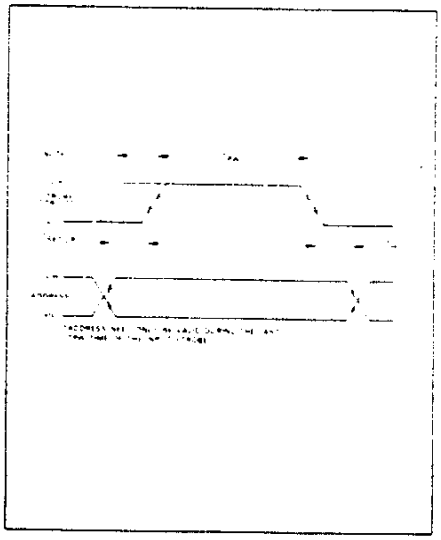


BR1941 BLOCK DIAGRAM

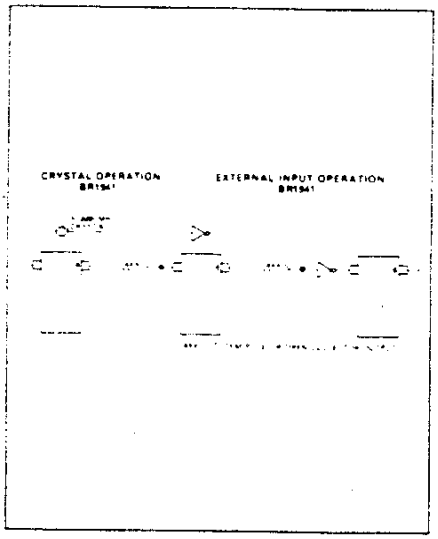
Band 1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	XTAL/EXT 1	Crystal or External Input 1	This input receives one pin of the crystal package or or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt Supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver Address inputs.
4-7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs as shown in Table 1, selects the receiver output frequency, f_R
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register. This input may be strobed or hard wired to +5V.
9	V_{DD}	Power Supply	+12 volt Supply
10	NC	No Connection	Internally bonded. Do not connect anything to this pin.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wired to +5V.
13-16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter Address inputs.
18	XTAL/EXT 2	Crystal or External Input 2	This input receives the other pin of the crystal package or the other polarity of the external input.



CONTROL TIMING



CRYSTAL/CLOCK OPTIONS

UNCTION

e pin of the crystal package or external input.

a frequency selected by the uts.

se inputs as shown in Table 1. utput frequency, f_R.

be loads the receiver address the receiver address register bed or hard wired to +5V

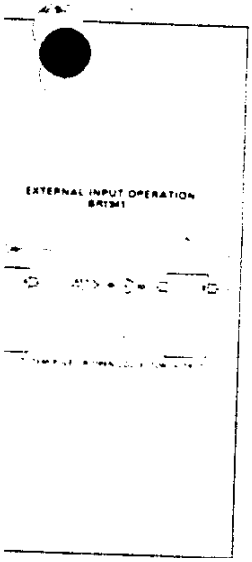
t connect anything to this pin.

e loads the transmitter address e transmitter address register. bed or hard wired to +5V.

inputs, as shown in Table 1, output frequency, f_T

frequency selected by the puts.

other pin of the crystal pack- y of the external input.



.OCK OPTIONS

ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin, with respect to ground	+20.0V
Negative Voltage on any Pin, with respect to ground	-0.3V
Storage Temperature	(plastic "M" package) - 65°C to + 125°C (ceramic "L" package) - 65°C to + 150°C
Lead Temperature (Soldering, 10 sec.)	+325°C

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and Functional Operation of the device at these or at any other condition above those indicated in the operational sections of this specification are not implied.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ± 5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding XTAL inputs
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 3.2 mA
High-level, V_{OH}	V_{CC}-1.5	4.0		V	I_{OH} = 100 µA
INPUT CURRENT					
Low-level, I_{IL}			0.3	mA	V_{IN} = GND, excluding XTAL inputs
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = GND excluding XTAL inputs
POWER SUPPLY CURRENT					
I_{CC}		20		mA	
I_{DD}		20		mA	
AC CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY		5.0688		MHz	XTAL/EXT inputs
PULSE WIDTH (T_{PW})					
Clock					50% Duty Cycle ± 10%
Receiver strobe	150		DC	ns	See Note 1
Transmitter strobe	150		DC	ns	See Note 1
INPUT SET-UP TIME (T_{SET-UP}) Address	50			ns	See Note 1
OUTPUT HOLD TIME(T_{HOLD}) Address	50			ns	

NOTE 1: Input set-up time can be decreased to >0 ns by increasing the minimum strobe width by 50 ns to a total of 200 ns.

All inputs except XTAL EXT have internal pull-up resistors

Board 3

OPERATION

Standard Frequencies

Choose a Transmitter and receiver frequency from the table below. Program the corresponding address into TA-TD and RA-RD respectively using strobe pulses or by hard wiring the strobe and address inputs.

Non-Standard Frequencies

To accomplish non-standard frequencies do one of the following:

1. Choose a crystal that when divided by the BR1941 generates the desired frequency.
2. Cascade devices by using the frequency outputs as an input to the XTAL EXT inputs of the subsequent BR1941.
3. Consult the factory for possible changes via ROM mask reprogramming.

FREQUENCY OPTIONS

TABLE 1 CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud	Theoretical Frequency	Actual Frequency	Percent	Duty Cycle	
D	C	B	A	Rate	16X Clock	16X Clock	Error	%	Divisor
0	0	0	0	50	0.8 KHz	0.8KHz	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.83	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

BR1941-00

TABLE 2 CRYSTAL FREQUENCY = 4.9152 MHZ

Transmit/Receive Address				Baud	Theoretical Frequency	Actual Frequency	Percent	Duty Cycle	
D	C	B	A	Rate	16X Clock	16X Clock	Error	%	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7598	-0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	-0.19	*	171
1	0	0	1	2000	32.0	31.9168	-0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8254	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	-0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

*When the duty cycle is not exactly 50% it is 50% ± 10%.

BR1941-05

TABLE 3. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 32X Clock	Actual Frequency 32X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	1.6 KHz	1.6 KHz	—	50:50	3168
0	0	0	1	75	2.4	2.4	—	50:50	2112
0	0	1	0	110	3.52	3.52	—	50:50	1440
0	0	1	1	134.5	4.304	4.303	.026	50:50	1178
0	1	0	0	150	4.8	4.8	—	50:50	1056
0	1	0	1	200	6.4	6.4	—	50:50	792
0	1	1	0	300	9.6	9.6	—	50:50	528
0	1	1	1	600	19.2	19.2	—	50:50	264
1	0	0	0	1200	38.4	38.4	—	50:50	132
1	0	0	1	1800	57.6	57.6	—	50:50	88
1	0	1	0	2400	76.8	76.8	—	50:50	66
1	0	1	1	3600	115.2	115.2	—	50:50	44
1	1	0	0	4800	153.6	153.6	—	-	33
1	1	0	1	7200	230.4	230.4	—	50:50	22
1	1	1	0	9600	307.2	298.16	2.941	-	17
1	1	1	1	19.200	614.4	633.6	3.125	50:50	8

*When the duty cycle is not exactly 50%, it is 50% ± 10%.

BR1941-06

Duty Cycle %	Divisor
50/50	8336
50/50	4224
50/50	2880
50/50	2355
5[illegible]	2112
5[illegible]	1056
50[illegible]	528
50/[illegible]	264
50/[illegible]	176
50/50	158
50/50	132
50/50	88
50/50	66
50/50	44
48/52	33
50/50	16

Duty Cycle %	Divisor
50/50	6144
50/50	4096
-	2793
50/50	2244
50/50	2048
50/50	1024
50/50	512
50/50	256
-	171
50/50	154
50/50	128
-	85
50/50	64
-	43
50/50	32
50/50	16

APPLICATIONS INFORMATION

OPERATION WITH A CRYSTAL

The BR1941 Baud Rate Generator may be driven by either a crystal or TTL level clock. When using a crystal, the waveform that appears at pins 1 (XTAL/EXT 1) and 18 (XTAL/EXT 2) does not conform to the normal TTL limits of $V_{IL} \leq 0.8V$ and $V_{IH} \geq 2.0V$. Figure 1 illustrates a typical crystal waveform.

Since the D.C. level of the waveform causes the least positive point to typically be greater than 0.8V, the BR1941 is designed to look for an edge, as opposed to a TTL level. The XTAL/EXT logic triggers on a rising edge of typically 1V in magnitude. This allows the use of a crystal without any additional components.

OPERATION WITH TTL LEVEL CLOCK

With clock frequencies in the area of 5 MHz, significant overshoot and undershoot can appear at pins 1 and/or 18. The BR1941 may, at times, trigger on a rising edge of an overshoot or undershoot waveform, causing the device to effectively "double-trigger". This phenomenon may result as a twice expected baud rate, or as an apparent device failure. Figure 2 shows a typical waveform that exhibits the "ringing" problem.

The design methods required to minimize ringing include the following.

1. Minimize the P.C. trace length. At 5 MHz, each inch of trace can add significantly to overshoot and undershoot.
2. Match impedances at both ends of the trace. For example, a series resistor near the BR1941 may be helpful.
3. A uniform impedance is important. This can be accomplished through the use of:
   a. parallel ground lines
   b. evenly spaced ground lines crossing the trace on the opposite side of PC board
   c. an inner plane of ground, e.g., as in a four layered PC board.

In the event that ringing exists on an already finished board, several techniques can be used to reduce it. These are:

1. Add a series resistor to match impedance as shown in Figure 3.
2. Add pull-up/pull-down resistor to match impedance, as shown in Figure 4.
3. Add a high speed diode to clamp undershoot, as shown in Figure 5.

The method that is easiest to implement in many systems is method 1, the series resistor. The series resistor will cause the D.C. level to shift up, but that does not cause a problem since the BR1941 is triggered by an edge, as opposed to a TTL level.

The BR1941 Baud Rate Generator can save both board space and cost in a communications system. By choosing either a crystal or a TTL level clock, the user can minimize the logic required to provide baud rate clocks in a given design.

Baud 5

CRYSTAL SPECIFICATIONS

User must specify termination (pin, wire, other)
Frequency—5.0688 MHz, or 4.9152 MHz
Temperature range 0°C to 70°C
Series resistance 50Ω
Series resonant
Overall tolerance ± .01%

CRYSTAL MANUFACTURERS (Partial List)

Northern Engineering Laboratories
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

Bulova Frequency Control Products
61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

CAL Crystal
1142 N. Gilbert Street
Anaheim, California 92801
(Available in HC-18 small can)
(714) 991-1580

CTS Knights Inc.
101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

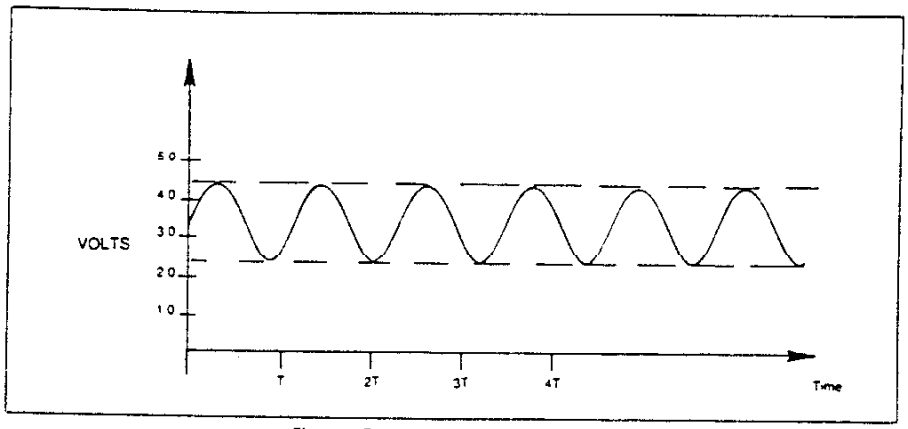


Figure 1 TYPICAL CRYSTAL WAVEFORM

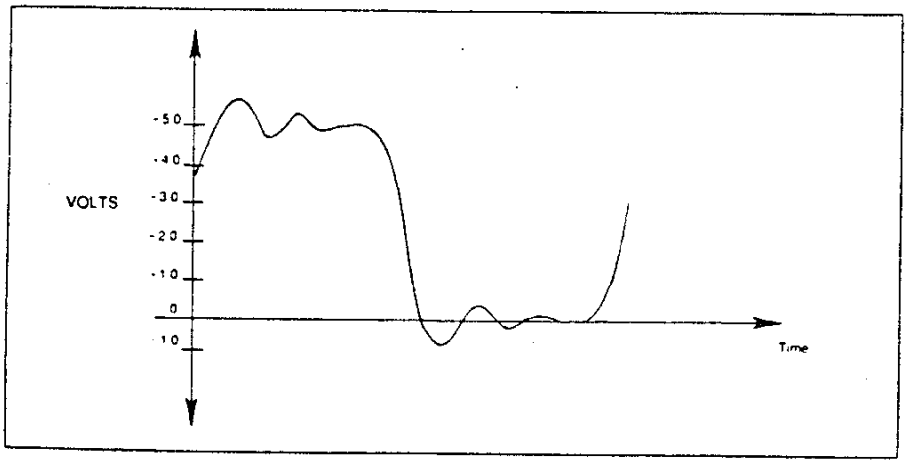
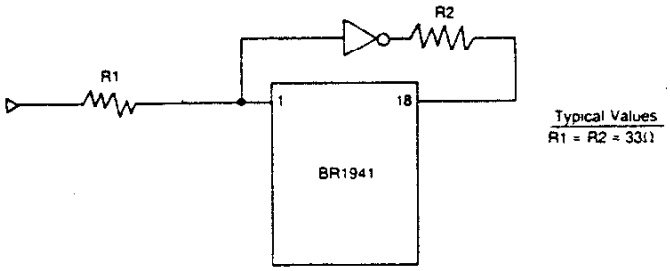
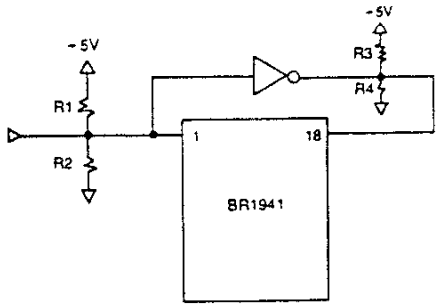


Figure 2 TYPICAL "RINGING" WAVEFORM



Typical Values
R1 = R2 = 33Ω

Figure 3 SERIES RESISTOR TO MATCH IMPEDANCE



Typical Values
R1 = R3 = 2.7K
R2 = R4 = 3.3K

Figure 4 PULL-UP/PULL-DOWN RESISTORS TO MATCH IMPEDANCE

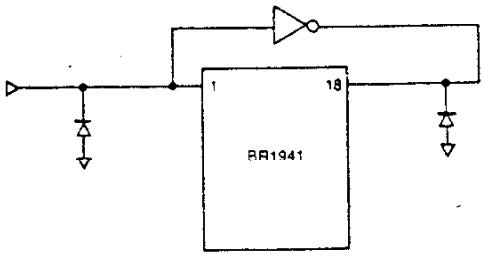
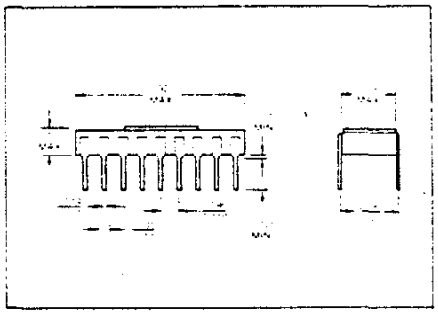
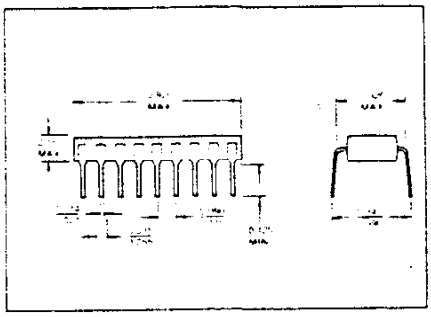


Figure 5 HIGH-SPEED DIODE TO CLAMP UNDERSHOOT



BR1941L CERAMIC PACKAGE



BR1941M PLASTIC PACKAGE

WESTERN DIGITAL CORPORATION | 3128 REDHILL AVENUE, BOX 2180
NEWPORT BEACH, CA 92663 (714) 557-3550,TWX 910-595-1139

Baud 5

BUS ORIE

FEATURES

ASYNCHRONOUS MOD

- FULL DUPLEX OPER
- SELECTABLE 5,6,7,
- LINE BREAK DETEC
- 1, 1½, or 2 STOP BI
- FALSE START BIT D
- OVERRUN AND FRA
- DC TO 35K BITS SE
- DC TO 600K BITS S
- 8251/9251A ASYNC
- REQUIRES NO AS
- 28 PIN PLASTIC DI
- −5 VOLT ONLY

SYSTEM COMPATIBL

- DOUBLE BUFFERI
- 8 BIT BI-DIRECTIO
  CONTROL WORDS
- ALL INPUTS AND O
- CHIP SELECT, RE
- ON-LINE DIAGNOS
- THREE STATE DAT

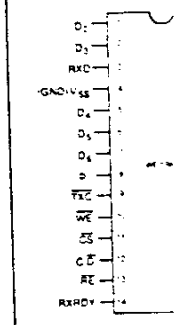


FIGURE 1 WD1

STANDARD MICROSYSTEMS CORPORATION

We keep ahead of our competition so you can keep ahead of yours.

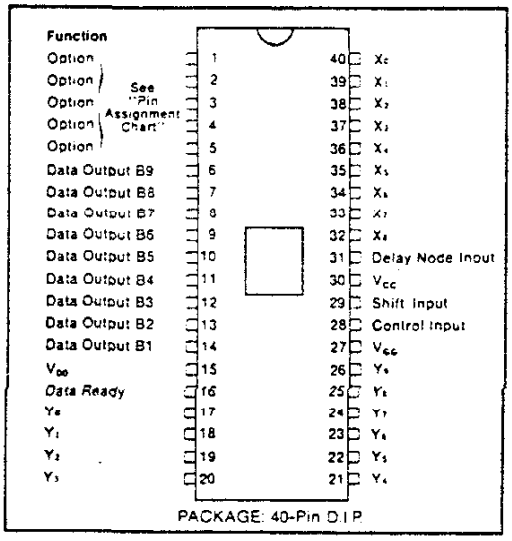
KR3600-XX
KR3600-ST
KR3600-STD
KR3600-PRO

Keyboard Encoder Read Only Memory

FEATURES

- Data output directly compatible with TTL
- N Key rollover or lockout operation
- Quad mode
- Lockout/rollover selection externally selected as option
- On chip-master/slave oscillator
- All 10 output bits available
- Fully buffered data outputs
- Output enable provided as option
- Data compliment control provided as option
- Pulse or level data ready output signal provided as an option
- Any key down output provided as an option
- Contact bounce circuit provided to eliminate contact bounce
- Static charge protection on all input/outputs
- Pin for Pin replacement for GI AY-5-3600

PIN CONFIGURATION



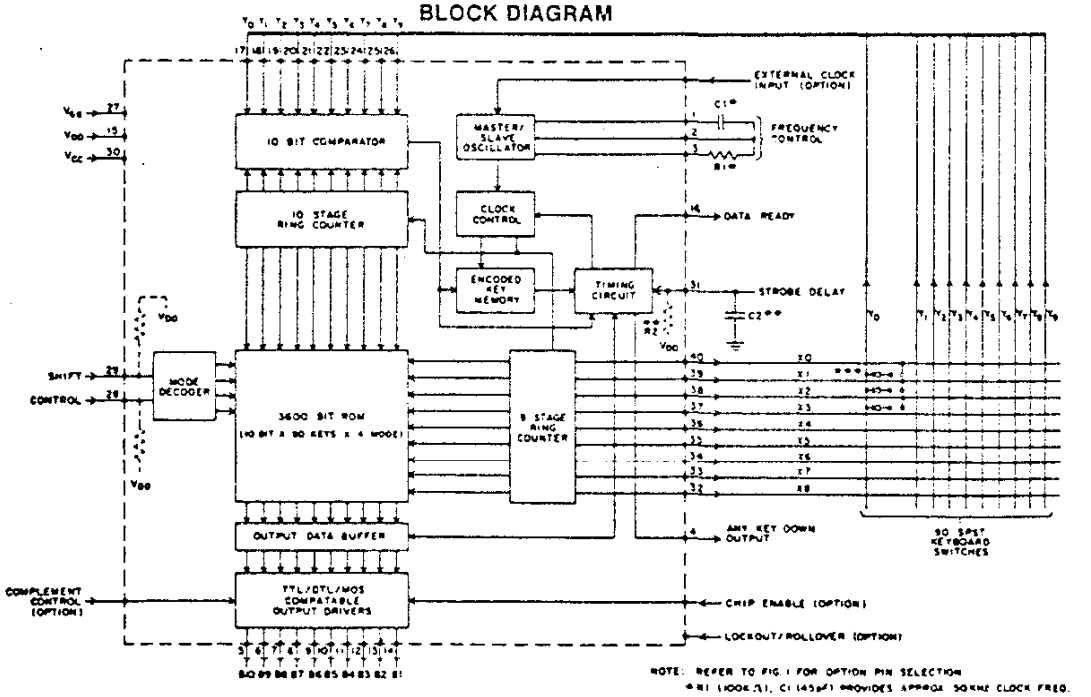
PACKAGE: 40-Pin D.I.P.

GENERAL DESCRIPTION

The SMC Microsystems KR3600-XX is a Keyboard Encoder containing a 3600 bit read only memory and all the logic necessary to encode single pole single throw keyboard closures into a 10 bit code.

The KR3600-XX is fabricated with a low voltage p channel technology and contains the equivalent of 5000 transistors on a monolithic chip in a 40 lead dip ceramic package.

BLOCK DIAGRAM



NOTE: REFER TO FIG. 1 FOR OPTION PIN SELECTION
* R1 (100K Ω), C1 (45pF) PROVIDES APPROX. 50KHz CLOCK FREQ.
** C2 (500pF DELAY/CPF) R2 SUPPLIED INTERNALLY
*** DIODES NECESSARY FOR COMPLETE N-KEY ROLLOVER OPERATION.

KR-1

DESCRIPTION OF OPERATION

The KR3600 contains a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby conditions, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y_0-Y_9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

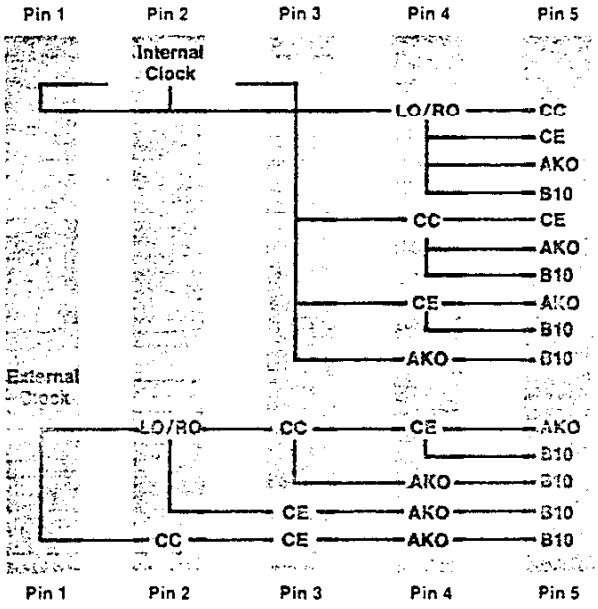
N KEY ROLLOVER – When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT – When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

SPECIAL PATTERNS – Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the KR3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes.

CUSTOM CODING INFORMATION
The custom coding information for SMC's 3600 Bit Keyboard Encoder ROM should be transmitted to SMC. The Truth Table should be completed on the format supplied.

LEGEND
CC = Complement Control
AKO = Any Key Down Output
B10 = B10 (Data) Output
LO/RO = Lockout/Rollover
CE = Chip Enable
Internal Clock = Self Contained Oscillator
External Clock = External Frequency Source



OPTION SELECTION/PIN ASSIGNMENT
FIGURE 1

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, V_{CC}	+0.3 V
Negative Voltage on any Pin, V_{CC}	−25 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{GG} = −12V ±1.0V, V_{DD} = GND, unless otherwise noted)

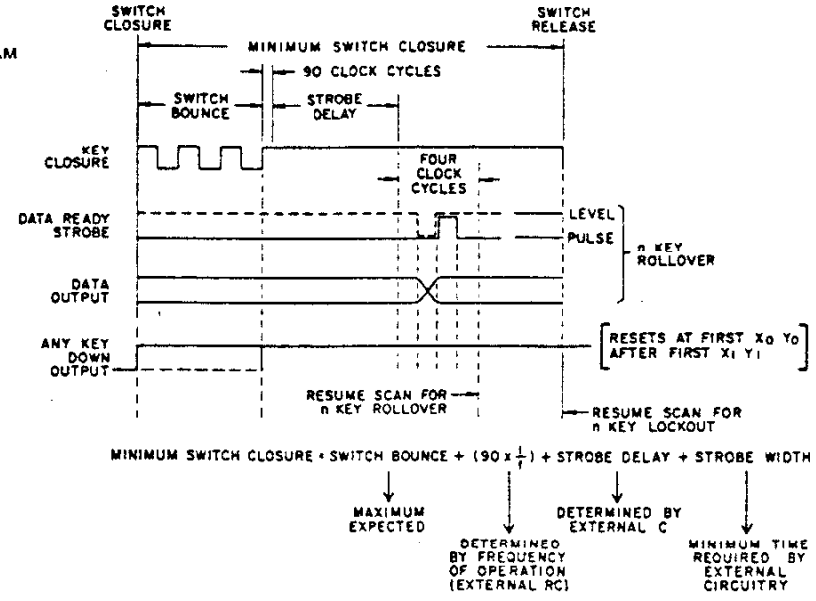
Characteristics	Min	Typ**	Max	Units	Conditions
Clock Frequency	10	50	100	KHz	See Block diagram footnote* for typical R-C values
External Clock Width	7	—	—	μs	
Data & Clock Input (Shift, Control, Compliment Control, Lockout/Rollover, Chip Enable & External Clock)					
Logic "0" Level	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{CC}−1.5	—	V_{CC}+0.3	V	
Shift & Control Input Current	75	150	220	μA	V_{IN} = +5V
X Output (X_0-X_9)					
Logic "1" Output Current	40	250	500	μA	V_{OUT} = V_{CC} (See Note 2)
	600	1300	4000	μA	V_{OUT} = V_{CC}−1.3V
	900	2000	6500	μA	V_{OUT} = V_{CC}−2.0V
	1500	2000	14,000	μA	V_{OUT} = V_{CC}−5V
	3000	10,000	23,000	μA	V_{OUT} = V_{CC}−10V
Logic "0" Output Current	8	30	60	μA	V_{OUT} = V_{CC}
	6	25	50	μA	V_{OUT} = V_{CC}−1.3V
	5	20	45	μA	V_{OUT} = V_{CC}−2.0V
	2	10	30	μA	V_{OUT} = V_{CC}−5V
	—	0.5	5	μA	V_{OUT} = V_{CC}−10V
Y Input (Y_0-Y_9)					
Trip Level	V_{CC}−5	V_{CC}−3	V_{CC}−2	V	Y Input Going Positive (See Note 2)
Hysteresis	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	18	100	170	μA	V_{IN} = V_{CC}
	14	80	150	μA	V_{IN} = V_{CC}−1.3V
	13	50	130	μA	V_{IN} = V_{CC}−2.0V
	5	40	110	μA	V_{IN} = V_{CC}−4.0V
Unselected Y Input Current	9	40	80	μA	V_{IN} = V_{CC}
	7	30	70	μA	V_{IN} = V_{CC}−1.3V
	6	25	60	μA	V_{IN} = V_{CC}−2.0V
	3	15	40	μA	V_{IN} = V_{CC}−5V
	—	0.5	20	μA	V_{IN} = V_{CC}−10V
Input Capacitance	—	3	10	pF	at 0V (All Inputs)
Switch Characteristics					
Minimum Switch Closure	—	—	—	—	See Timing Diagram
Contact Closure Resistance	—	—	300	Ω	Z_{CC}
	1 x 10^7	—	—	Ω	Z_{CO}
Strobe Delay					
Trip Level (Pin 31)	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)	−3	−5	−9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready					
Logic "0"	—	—	0.4	V	I_{OL} = 1.6m A
Logic "1"	V_{CC}−1	—	—	V	I_{OH} = 1.0m A
	V_{CC}−2	—	—	V	I_{OH} = 2.2m A
Power					
I_{CC}	—	12	22	mA	V_{CC} = +5V
I_{GG}	—	12	22	mA	V_{GG} = −12V

**Typical values are at +25°C and nominal voltages.

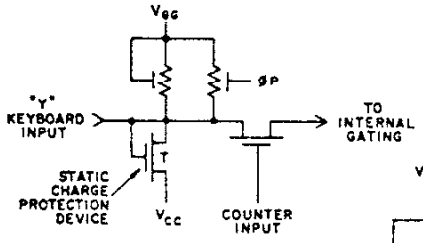
NOTE
1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.

KB3

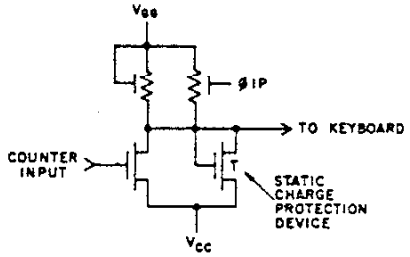
TIMING DIAGRAM



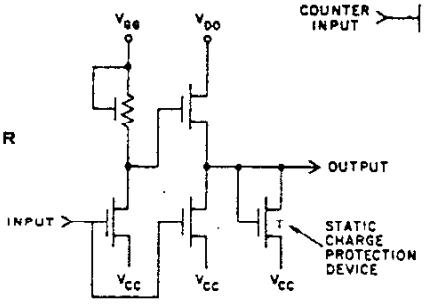
"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD

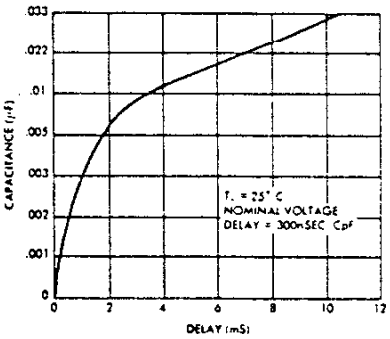


OUTPUT DRIVER

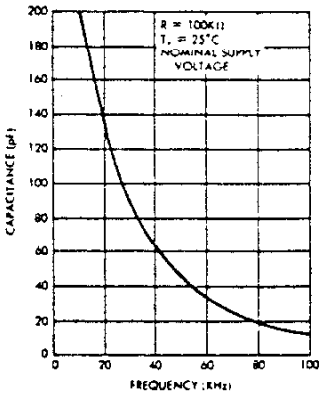


NOTE: Output driver capable of driving one TTL load with no external resistor. Capable of driving two TTL loads using an external 6.8KΩ resistor to V_{GG}

STROBE DELAY vs. C_2



OSCILLATOR FREQUENCY vs. C_1



KB4

KR3600-STD

XY	Normal B-12345678910	Shift B-12345678910	Control B-12345678910	Shift Control B-12345678910
00	1 1000111001	< 0011111001	1 1000111011	SUB 0101100001
01	q 1000110101	Q 1000100101	q 1000111111	DLE 0000100001
02	a 1000010101	A 1000000101	a 1000011111	@ 0000000101
03	z 0101110101	Z 0101100101	z 0101111111	P 0000100101
04	HT 1001000001	HT 1001000001	HT 1001000001	I 1001000101
05	H 0001000101	H 0001000101	H 0001000101	H 0001000111
06	+ 1101011001	+ 1101011001	+ 1101011001	+ 1101011011
07	SO 0111001001	> 0111111001	SO 0111000001	SO 0111000011
08	p 0000110101	@ 0000000101	NUL 0000000001	NUL 0000000001
09	1 1000111001	' 1000011001	SOH 1000000001	SOH 1000000001
10	2 0100111001	@ 0000000101	2 0100111011	ETB 1110100001
11	w 1110110101	W 1110100101	w 1110111111	A 0011100101
12	s 1100110101	S 1100100101	s 1100111111	A 1000000101
13	x 0001110101	X 0001100101	x 0001111111	Q 1000100101
14	RS 0111100001	RS 0111100001	RS 0111000001	FS 0011100001
15	% 1010011001	% 1010011001	% 1010011001	% 1010011011
16	m 1011010101	] 1011100101	CR 1011000001	CR 1011000001
17	SI 1111000001	SI 1111000001	SI 1111000001	SI 1111000011
18	n 0111010101	A 0111100101	SO 0111000001	SO 0111000001
19	2 0100111001	" 0100011001	STX 0100000001	STX 0100000001
20	3 1100111001	# 1100011001	3 1100111011	NAK 1010100001
21	e 1010010101	E 1010000101	e 1010011111	DC3 1100100001
22	d 0010010101	D 0010000101	d 0010011111	B 0100000101
23	c 1100010101	C 1100000101	c 1100011111	R 0100100101
24	— 1111100100	— 1111100100	— 1111100100	A 0111100100
25	$ 0010011001	$ 0010011001	$ 0010011001	$ 0010011011
26	L 0011000101	L 0011000101	L 0011000101	L 0011000111
27	US 1111100001	US 1111100001	US 1111100001	US 1111100011
28	6 0110111001	& 0110011001	ACK 0110000001	ACK 0110000001
29	k 1101010101	[1101100101	DEL 1111111101	DEL 1111111101
30	4 0010111001	$ 0010011001	4 0010111011	DC4 0010100001
31	r 0100110101	R 0100100101	r 0100111111	ENQ 0010000001
32	f 0110010101	F 0110000101	f 0110011111	C 1100000101
33	SP 0000011000	SP 0000011000	SP 0000011000	SP 0000011000
34	CAN 0001101000	(0001011000	CAN 0001100000	BS 0001000000
35	CR 1011000001	CR 1011000001	CR 1011000001	M 1011000101
36	[1101111101	[1101111101	[1101111111	K 1101000101
37	VT 1101000000	VT 1101000000	VT 1101000000	VT 1101000010
38	7 1110111001	' 1110011001	BEL 1110000001	BEL 1110000001
39	' 0100011001	" 0100011001	' 0100011001	' 0100011011
40	5 1010111001	% 1010011001	5 1010111011	STX 0100000001
41	t 0010110101	T 0010100101	t 0010111111	EOT 0010000001
42	g 1110010101	g 1110000101	G 1110011111	D 0010000101
43	v 0110110101	V 0110100101	v 0110111111	S 1100100101
44	ETX 1100000001	ETX 1100000001	ETX 1100000001	ETX 1100000001
45	} 1011111101	} 1011111101	} 1011111111	N 0111000101
46	? 1111111001	? 1111111001	? 1111111011	| 1101100101
47	— 1011011001	— 1011111001	— 1011011001	— 1011011011
48	) 1001011001	) 1001011001	) 1001011001	) 1001011011
49	SP 0000011001	SP 0000011001	SP 0000011001	SP 0000011011
50	6 0110111001	> 0111111001	6 0110111011	SOH 1000000001
51	y 1001110101	Y 1001100101	y 1001111111	DC1 1000100001
52	h 0001010101	H 0001000101	h 0001011111	E 1010000101
53	b 0100010101	B 0100000101	b 0100011111	T 0010100101
54	_ 0101111001	' 0101011001	_ 0101111011	SYN 0110100001
55	> 0111111001	> 0111111001	> 0111111011	Z 0101100101
56	. 1101111001	- 1101011001	. 1101111011	Y 1001100101
57	NUL 0000000001	NUL 0000000001	NUL 0000000001	NUL 0000000001
58	' 0101011001	' 0101011001	' 0101011001	' 0101011011
59	! 1000011001	! 1000011001	! 1000011001	! 1000011011
60	7 1110111001	& 0110011001	7 1110111011	ETX 1100000001
61	u 1010110101	U 1010100101	u 1010111111	BEL 1110000001
62	j 0101010101	J 0101000101	j 0101011111	F 0110000101
63	n 0111010101	N 0111000101	n 0111011111	U 1010100101
64	= 1011111000	= 1011111050	= 1011111010	~ 0111111100
65	< 0011111001	< 0011111001	< 0011111011	W 1110100101
66	p 0000110101	P 0000100101	p 0000111111	J 0101000101
67	0 0000111001	) 1001011001	0 0000111011	DC2 0100100001
68	& 0110011001	& 0110011001	& 0110011001	& 0110011011
69	# 1100011001	# 1100011001	# 1100011001	# 1100011011
70	8 0001111001	* 0101011001	8 0001111011	ESC 1101100001
71	i 1001010101	I 1001000101	i 1001011111	ACK 0110000001
72	k 1101010101	K 1101000101	k 1101011111	G 1110000101
73	m 1011010101	M 1011000101	m 1011011111	V 0110100101
74	/ 1111011001	? 1111111001	/ 1111011001	' 1110011001
75	' 1110011001	" 0100011001	' 1110011001	" 0100011001
76	LF 0101000000	LF 0101000000	LF 0101000000	GS 1011100000
77	= 1011111001	+ 1101011001	= 1011111001	~ 1101011001
78	FF 0011001001	< 0011111001	FF 0011000001	FF 0011000011
79	(0001011001	(0001011001	(0001011001	(0001011011
80	9 1001111001	(0001011001	9 1001111011	EM 1001100001
81	o 1111010101	O 1111000101	o 1111011111	] 1011100101
82	i 0011010101	L 0011000101	i 0011011111	X 0001100101
83	. 0011011001	. 0011011001	. 0011011001	. 0011011011
84	0111011001	0111011001	0111011001	0111011011
85	. 1101111001	. 0101111001	. 1101111001	0101111001
86	] 1011100101	{ 1101100101	] 1011100101	[1101100101
87	- 1011011001	— 1111100101	- 1011011001	— 1111100101
88	0 0000111001	0 0000111001	0 0000111001	0 0000111001
89	9 1001111001	) 1001011001	HT 1001000001	HT 1001000001

Options:

Internal oscillator (pins 1, 2, 3)
Any key down (pin 4) positive output
N key rollover only
Pulse data ready signal
Internal resistor to VDD on shift and control pins
KR3600-STD outputs provides ASCII bits 1-6 on B1-B6, and bit 7 on B8

KBT

KR 3600-ST

XY	Normal B-123456789	Shift B-123456789	Control B-123456789	Shift/Control B-123456789
00	\ 000001101	~ 011111101	NUL 000000001	RS 011110001
01	= 101111010	` 110101001	GS 101110001	VT 110100010
02	DC3 110010010	DC3 110010010	DC3 110010010	DC3 110010010
03	— 101101001	— 111110101	CR 101100010	US 111110010
04	BS 000100010	BS 000100010	BS 000100010	BS 000100010
05	0 000011001	0 000011001	0 000011001	0 000011001
06	• 011101001	• 011101001	• 011101001	• 011101001
07	000000000	000000000	000000000	000000000
08	000000000	000000000	000000000	000000000
09	000000000	000000000	000000000	000000000
10	√ 111101010	? 111111001	ST 111100001	US 111110010
11	• 011101001	> 011111010	SO 011100010	RS 011110001
12	? 001101010	< 001111001	FF 001100001	FS 001110010
13	m 101101110	M 101100101	CR 101100010	CR 101100010
14	n 011101110	N 011100101	SO 011100010	SO 011100010
15	b 010001110	B 010000101	STX 010000010	STX 010000010
16	v 011011110	V 011010101	SYN 011010010	SYN 011010010
17	c 110001101	C 110000110	ETX 110000001	ETX 110000001
18	x 000111101	X 000110110	CAN 000110001	CAN 000110001
19	z 010111101	Z 010110101	SUB 010110010	SUB 010110010
20	LF 010100001	LF 010100001	LF 010100001	LF 010100001
21	\ 001110101	: 001111110	FS 001110010	FS 001110010
22	DEL 111111110	DEL 111111110	DEL 111111110	DEL 111111110
23	[110110110	] 101110110	ESC 110110001	GS 101110001
24	7 111011010	7 111011010	7 111010010	7 111011010
25	8 000111010	8 000111010	8 000111010	8 000111010
26	9 100111001	9 100111001	9 100111001	9 100111001
27	000000000	000000000	000000000	000000000
28	000000000	000000000	000000000	000000000
29	000000000	000000000	000000000	000000000
30	110111010	010111001	ESC 110110001	SUB 010110010
31	l 001101101	L 001100110	FF 001100001	FF 001100001
32	k 110101110	K 110100101	VT 110100010	VT 110100010
33	j 010101101	J 010100110	LF 010100001	LF 010100001
34	h 000101110	H 000100101	BS 000100010	BS 000100010
35	g 111001110	G 111000101	BEL 111000010	BEL 111000010
36	f 011001101	F 011000110	ACK 011000001	ACK 011000001
37	d 001001110	D 001000101	EOT 001000010	EOT 001000010
38	s 110011110	S 110010101	DC3 110010010	DC3 110010010
39	a 100001110	A 100000101	SOH 100000010	SOH 100000010
40	000000000	000000000	000000000	000000000
41	! 110111101	! 101111101	ESC 110110001	GS 101110001
42	GR 101100010	GR 101100010	GR 101100010	GR 101100010
43	' 111001001	" 010001001	BEL 111000010	STX 010000010
44	4 001011010	4 001011010	4 001011010	4 001011010
45	5 101011001	5 101011001	5 101011001	5 101011001
46	6 011011001	6 011011001	6 011011001	6 011011001
47	000000000	000000000	000000000	000000000
48	000000000	000000000	000000000	000000000
49	000000000	000000000	000000000	000000000
50	p 000011110	P 000010101	DEL 000010010	DEL 000010010
51	o 111101101	O 111100110	SI 111100001	SI 111100001
52	i 100101101	I 100100110	HT 100100001	HT 100100001
53	u 101011110	U 101010101	NAK 101010010	NAK 101010010
54	y 100111110	Y 100110101	EM 100110010	EM 100110010
55	t 001011101	T 001010110	DC4 001010001	DC4 001010001
56	r 010011101	R 010010110	DC2 010010001	DC2 010010001
57	e 101001101	E 101000110	ENQ 101000001	ENQ 101000001
58	w 111011101	W 111010110	ETB 111010001	ETB 111010001
59	q 100011101	Q 100010110	DC1 100010001	DC1 100010001
60	000000000	000000000	000000000	000000000
61	000000000	000000000	000000000	000000000
62	DC2 010010001	DC2 010010001	DC2 010010001	DC2 010010001
63	000000000	000000000	000000000	000000000
64	1 100011010	1 100011010	1 100011010	1 100011010
65	2 010011010	2 010011010	2 010011010	2 010011010
66	3 110011001	3 110011001	3 110011001	3 110011001
67	000000000	000000000	000000000	000000000
68	000000000	000000000	000000000	000000000
69	000000000	000000000	000000000	000000000
70	0 000011001	) 100101010	DLE 000010010	HT 100100001
71	9 100111001	(001010001	EM 100110010	BS 000100010
72	8 000111010	* 010101010	CAN 000110001	LF 010100001
73	7 111011010	& 011001010	ETB 111010001	ACK 011000001
74	6 011011001	A 011110110	SYN 011010010	RS 011110001
75	5 101011001	% 101001010	NAK 101010010	ENQ 101000001
76	4 001011010	$ 001001001	DC4 001010001	EOT 001000010
77	3 110011001	# 110001010	DC3 110010010	ETX 110000001
78	2 010011010	@ 000000110	DC2 010010001	NUL 000000001
79	1 100011010	! 100001001	DC1 100010001	SOH 100000010
80	000000000	000000000	000000000	000000000
81	000000000	000000000	000000000	000000000
82	000000000	000000000	000000000	000000000
83	000000000	000000000	000000000	000000000
84	000000000	000000000	000000000	000000000
85	SP 000001010	SP 000001010	NUL 000000001	NUL 000000001
86	000000000	000000000	000000000	000000000
87	DC1 100010001	DC1 100010001	DC1 100010001	DC1 100010001
88	HT 100100001	HT 100100001	HT 100100001	HT 100100001
89	ESC 110110001	ESC 110110001	ESC 110110001	ESC 110110001

Options Pin 1, 2, 3—Internal oscillator
Pin 4—Lockout (logic 1), rollover (logic 0)
Pin 5—Any key down output

All outputs complemented

KR 3600-PRO

XY	Normal	Shift	Control	Shift/Control
00	000000000	001000000	010000000	011000000
01	000000001	001000001	010000001	011000001
02	000000010	001000010	010000010	011000010
03	000000011	001000011	010000011	011000011
04	000000100	001000100	010000100	011000100
05	000000101	001000101	010000101	011000101
06	000000110	001000110	010000110	011000110
07	000000111	001000111	010000111	011000111
08	000001000	001001000	010001000	011001000
09	000001001	001001001	010001001	011001001
10	000001010	001001010	010001010	011001010
11	000001011	001001011	010001011	011001011
12	000001100	001001100	010001100	011001100
13	000001101	001001101	010001101	011001101
14	000001110	001001110	010001110	011001110
15	000001111	001001111	010001111	011001111
16	000010000	001010000	010010000	011010000
17	000010001	001010001	010010001	011010001
18	000010010	001010010	010010010	011010010
19	000010011	001010011	010010011	011010011
20	000010100	001010100	010010100	011010100
21	000010101	001010101	010010101	011010101
22	000010110	001010110	010010110	011010110
23	000010111	001010111	010010111	011010111
24	000011000	001011000	010011000	011011000
25	000011001	001011001	010011001	011011001
26	000011010	001011010	010011010	011011010
27	000011011	001011011	010011011	011011011
28	000011100	001011100	010011100	011011100
29	000011101	001011101	010011101	011011101
30	000011110	001011110	010011110	011011110
31	000011111	001011111	010011111	011011111
32	000100000	001100000	010100000	011100000
33	000100001	001100001	010100001	011100001
34	000100010	001100010	010100010	011100010
35	000100011	001100011	010100011	011100011
36	000100100	001100100	010100100	011100100
37	000100101	001100101	010100101	011100101
38	000100110	001100110	010100110	011100110
39	000100111	001100111	010100111	011100111
40	000101000	001101000	010101000	011101000
41	000101001	001101001	010101001	011101001
42	000101010	001101010	010101010	011101010
43	000101011	001101011	010101011	011101011
44	000101100	001101100	010101100	011101100
45	000101101	001101101	010101101	011101101
46	000101110	001101110	010101110	011101110
47	000101111	001101111	010101111	011101111
48	000110000	001110000	010110000	011110000
49	000110001	001110001	010110001	011110001
50	000110010	001110010	010110010	011110010
51	000110011	001110011	010110011	011110011
52	000110100	001110100	010110100	011110100
53	000110101	001110101	010110101	011110101
54	000110110	001110110	010110110	011110110
55	000110111	001110111	010110111	011110111
56	000111000	001111000	010111000	011111000
57	000111001	001111001	010111001	011111001
58	000111010	001111010	010111010	011111010
59	000111011	001111011	010111011	011111011
60	000111100	001111100	010111100	011111100
61	000111101	001111101	010111101	011111101
62	000111110	001111110	010111110	011111110
63	000111111	001111111	010111111	011111111
64	100000000	101000000	110000000	111000000
65	100000001	101000001	110000001	111000001
66	100000010	101000010	110000010	111000010
67	100000011	101000011	110000011	111000011
68	100000100	101000100	110000100	111000100
69	100000101	101000101	110000101	111000101
70	100000110	101000110	110000110	111000110
71	100000111	101000111	110000111	111000111
72	100001000	101001000	110001000	111001000
73	100001001	101001001	110001001	111001001
74	100001010	101001010	110001010	111001010
75	100001011	101001011	110001011	111001011
76	100001100	101001100	110001100	111001100
77	100001101	101001101	110001101	111001101
78	100001110	101001110	110001110	111001110
79	100001111	101001111	110001111	111001111
80	100010000	101010000	110010000	111010000
81	100010001	101010001	110010001	111010001
82	100010010	101010010	110010010	111010010
83	100010011	101010011	110010011	111010011
84	100010100	101010100	110010100	111010100
85	100010101	101010101	110010101	111010101
86	100010110	101010110	110010110	111010110
87	100010111	101010111	110010111	111010111
88	100011000	101011000	110011000	111011000
89	100011001	101011001	110011001	111011001

Options
Internal oscillator (pins 1, 2, 3)
Lockout rollover (pin 4), with internal resistor to VDD
Lockout is logic 1

Any key down (pin 5), positive output
Pulse data ready
Internal resistor to VDD on shift & control pins

4P7

DESCRIPTION

The KR 3600 PRO is a MOS/LSI device intended to simplify the interface of a microprocessor to a keyboard matrix. Like the other KR 3600 parts, the KR 3600 PRO contains all of the logic to de-bounce and encode keyswitch closures, while providing either a 2-key or N-key rollover.

The output of the KR 3600 PRO is a simple binary code which may be converted to a standard information code by a PROM or directly by a microprocessor. This permits a user maximum flexibility of key layout with simple field programming.

The code in the KR 3600 is shown in Table I. The format is simple: output bits 9, 8, 7, 6, 5, 4 and 1 are a binary sequence. The count starts at X0, Y0 and increments through X0Y1, X0Y2...X8Y9. Bit 9 is the LSB; bit 1 is the MSB.

Bits 2 and 3 indicate the mode as follows:

Bit 2	Bit 3	
0	0	Normal
0	1	Shift
1	0	Control
1	1	Shift Control

For maximum ease of use and flexibility, an internal scanning oscillator is used, with pin selection of N-key lockout (also known as 2-key rollover) and N-key rollover. An "any-key-down" output is provided for such uses as repeat oscillator keying.

Figure 1 shows a PROM-encoded 64 key, 4 mode application, using a 256x8 PROM, and Figure 2 a full 90 key, 4 mode application, utilizing a 512x8 PROM.

If N-key rollover operation is desired, it is recommended that a diode be inserted in series with each switch as shown. This prevents "phantom" key closures from resulting if three or more keys are depressed simultaneously.

FIGURE 1
KR 3600 PRO TYPICAL APPLICATION
64 KEY, 4 MODE

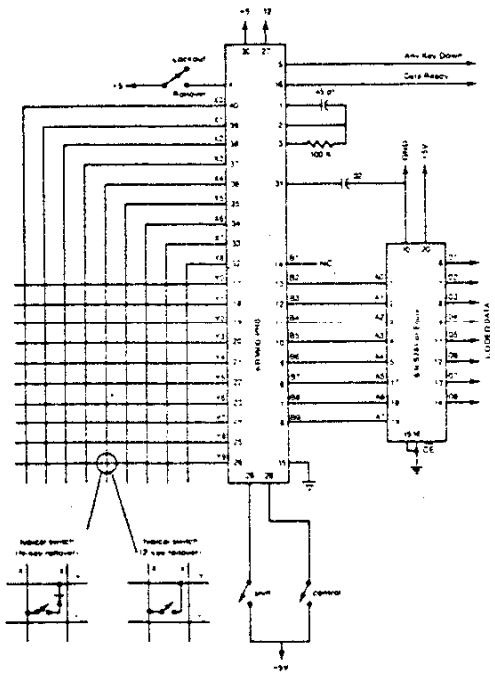
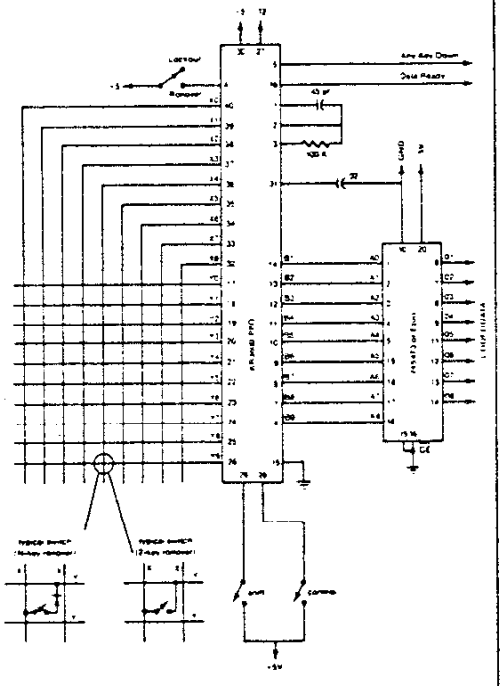


FIGURE 2
KR 3600 PRO TYPICAL APPLICATION
90 KEY, 4 MODE



National Semiconductor

Electronic Data Processing

MM5034, MM5035 Octal 80-Bit Static Shift Register

General Description

The MM5034 octal 80-bit shift register is a monolithic MOS integrated circuit utilizing N-channel low threshold enhancement mode and ion-implanted depletion mode devices.

The MM5034 is designed for use in computer display peripherals. All inputs and outputs are TTL compatible. The clocks and recirculate logic are internal to reduce system component count, and TRI-STATE® output buffers provide bus interface. Because of its N-channel characteristics, single 5V power supply operation is required.

Simple interface to the NSC CRT DP8350 controller and character generator to incorporate an entire CRT terminal is feasible with the MM5034.

The MM5034 is available in a 22-lead dual-in-line package.

The MM5035 is a 20-pin version of the MM5034 with the TRI-STATE output select feature omitted, for a simple data in/data out operation.

Features

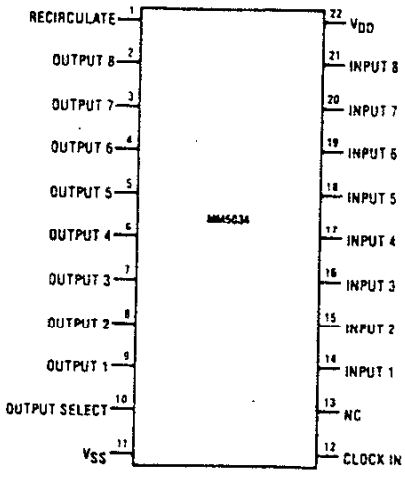
- Single 5V power supply
- Internal clocks
- High speed and static operation
- TRI-STATE output buffer
- Recirculate and output select independent
- TTL compatible

Applications

- CRT displays
- Computer peripherals

Connection Diagrams

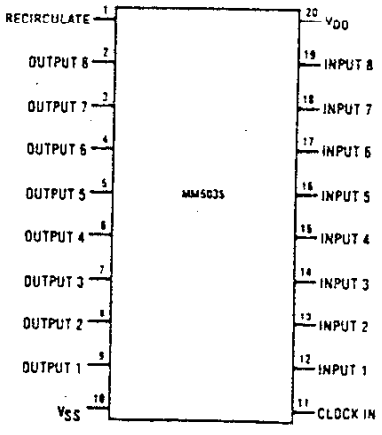
Dual-in-Line-Package



TOP VIEW

Order Number MM5034N
See Package 21

Dual-in-Line-Package



TOP VIEW

Order Number MM5035N
See Package 20A

5R 1

Absolute Maximum Ratings

Supply Voltage	7 V_{DC}
Input Voltage	7 V_{DC}
Power Dissipation	750 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics V_{DD} = 5V ±5%, T_A = 0°C to +70°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Input					
Logical "1" Input Voltage		2.2			V
Logical "0" Input Voltage				0.8	V
Data and Control Inputs					
Logical "1" Input Voltage		2.2			V
Logical "0" Input Voltage				0.8	V
Data, Clock and Control Inputs					
Logical "1" Input Current	V_{IN} = 5V			5.0	μA
Input Capacitance	V_{IN} = 2.5V		5.0	8.0	pF
Outputs					
Logical "1" Output Voltage	I_{OUT} = 100 μA	2.4	2.8		V
Logical "0" Output Voltage	I_{OUT} = 1.6 mA		0.25	0.4	V
TRI-STATE Output Current	V_{OUT} = 5V			−5.0	μA
	V_{OUT} = 0V			5.0	μA
Supply Current			60	90	mA
Timing					
Clock Frequency		0		3.0	MHz
Clock Pulse Width High	*(Figure 1)*	125		10,000	ns
Clock Pulse Width Low	(Note 1)	125		∞	ns
Output Rise and Fall Time (t_r, t_f)	*(Figure 1)*		40	50	ns
Set-Up Time	*(Figure 1)*	100			ns
Hold Time	*(Figure 1)*	0			ns
Output Enable Time	*(Figure 1)*			185	ns
Output Disable Time	*(Figure 1)*			185	ns
Clock Rise and Fall Time	*(Figure 1)*			5.0	μs
Output Delay, (t_{PD})			80	185	ns

Note 1: The clock input must be at a low level for DC storage. Minimum pulse width assumes 10 ns t_r and t_f.

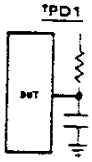
MM5034, MM5035 Recirculate and TRI-STATE Operation

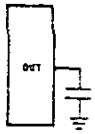
Recirculate is used to maintain data in the shift register after it has been loaded. While the shift register is being loaded, Recirculate must be at a logical "0". When the loading is completed, Recirculate should be brought to a logical "1". This disables the data input and feeds the output of the last shift cell back to the input of the first shift cell for each of the 8 registers.

For the output to be in the TRI-STATE mode output select should be at the logical "1" level.

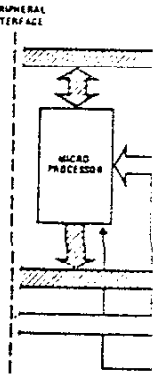
SR2

AC Test Circ





Typical Applic



FIGU

AC Test Circuits and Switching Time Waveforms

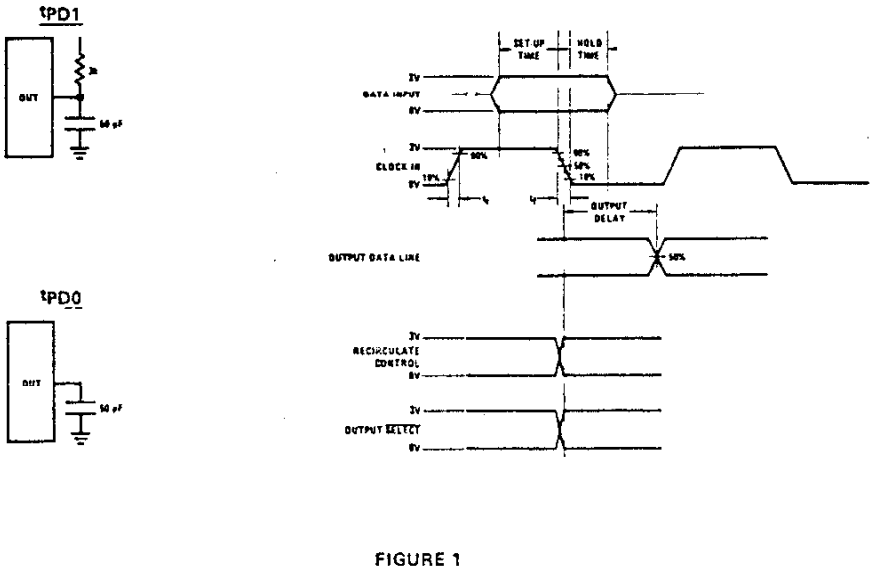


FIGURE 1

Typical Application

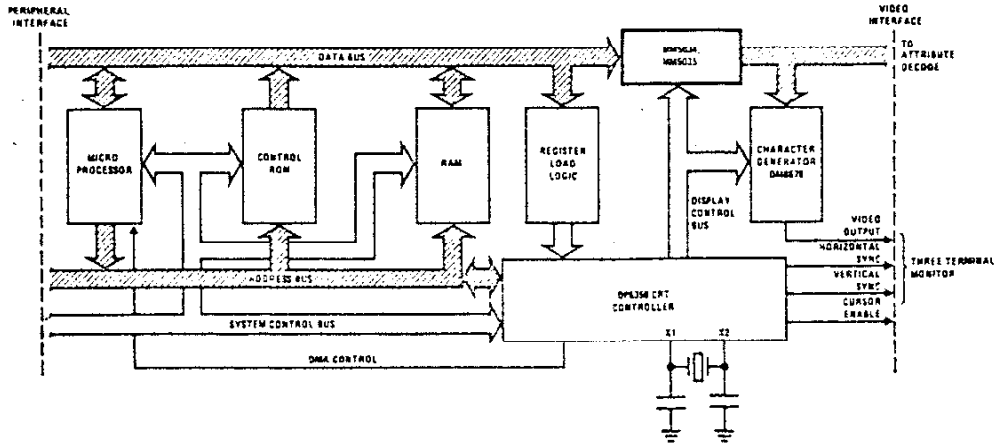


FIGURE 2. CRT System Diagram Using the MM5034, MM5035 as a Line Buffer with DMA

SR3

STANDARD MICROSYSTEMS CORPORATION

We keep ahead of our competition so you can keep ahead of yours.

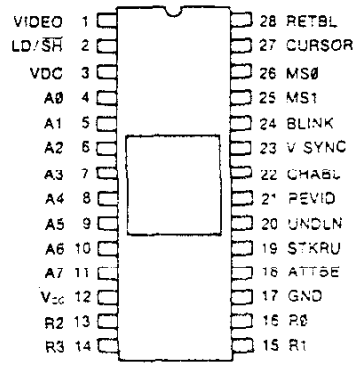
CRT 8002
μPC FAMILY

CRT Video Display Attributes Controller Video Generator VDAC™

FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters (alphanumeric and graphic)
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency
    - CRT 8002A 20MHz
    - CRT 8002B 15MHz
    - CRT 8002C 10MHz
  - Access time 400ns
- ☐ On chip horizontal and vertical retrace video blanking
- ☐ No descender circuitry required
- ☐ Four modes of operation (intermixable)
  - Internal character generator (ROM)
  - Wide graphics
  - Thin graphics
  - External inputs (fonts/dot graphics)
- ☐ On chip attribute logic—character, field
  - Reverse video
  - Character blank
  - Character blink
  - Underline
  - Strike-thru
- ☐ Four on chip cursor modes
  - Underline
  - Blinking underline
  - Reverse video
  - Blinking reverse video
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ Subscriptable
- ☐ Expandable character set
  - External fonts
  - Alphanumeric and graphic
  - RAM, ROM, and PROM
- ☐ On chip address buffer
- ☐ On chip attribute buffer
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ MOS N-channel silicon-gate COPLAMOS® process
- ☐ CLASP® technology—ROM and options
- ☐ Compatible with CRT 5027 VTAC®

PIN CONFIGURATION



General Description

The SMC CRT 8002 Video Display Attributes Controller (VDAC) is an N-channel COPLAMOS® MOS/LSI device which utilizes CLASP® technology. It contains a 7X11X128 character generator ROM, a wide graphics mode, a thin graphics mode, an external input mode, character address data latch, field and or character attribute logic, attribute latch, four cursor modes, two programmable blink rates, and a high speed video shift register. The CRT 8002 VDAC™ is a companion chip to SMC's CRT 5027 VTAC. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

The CRT 8002 video output may be connected directly to a CRT monitor video input. The CRT 5027 blanking output can be connected directly to the CRT 8002 retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

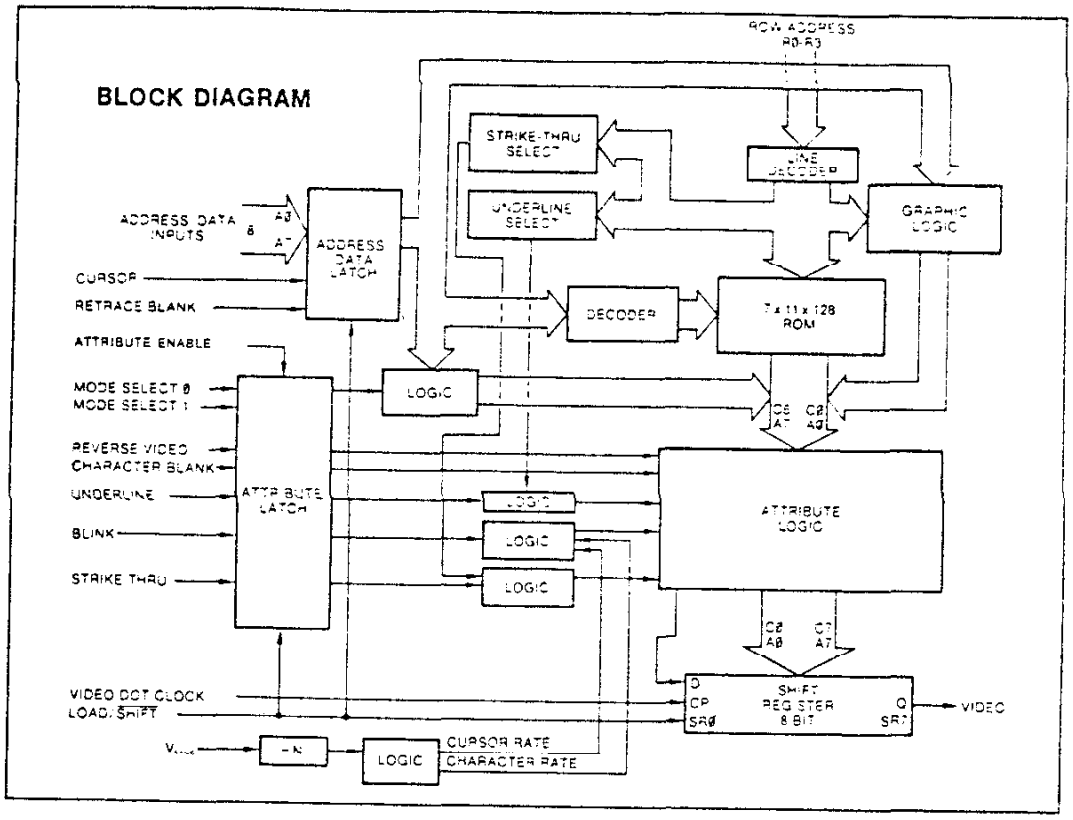
Four cursor modes are available on the CRT 8002. They are: underline, blinking underline, reverse video block, and blinking reverse video block. Any one of these can be mask programmed as the cursor function. There is a separate cursor blink rate which can be mask programmed to provide a 1.5Hz to 1Hz blink rate.

The CRT 8002 attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate is mask programmable from 7.5Hz to 0.5Hz and has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions and can be mask programmed to any number of raster lines at any position in the character block. These attributes are available in all modes.

In the wide graphic mode the CRT 8002 produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing for 256 unique graphic symbols. Thus, the CRT 8002 can produce either an alphanumeric symbol or a graphic entity depending on the mode selected. The mode can be changed on a per character basis.

The thin graphic mode enables the user to create single line drawings and forms.

The external mode enables the user to extend the on-chip ROM character set and/or the on-chip graphics capabilities by inserting external symbols. These external symbols can come from either RAM, ROM or PROM.



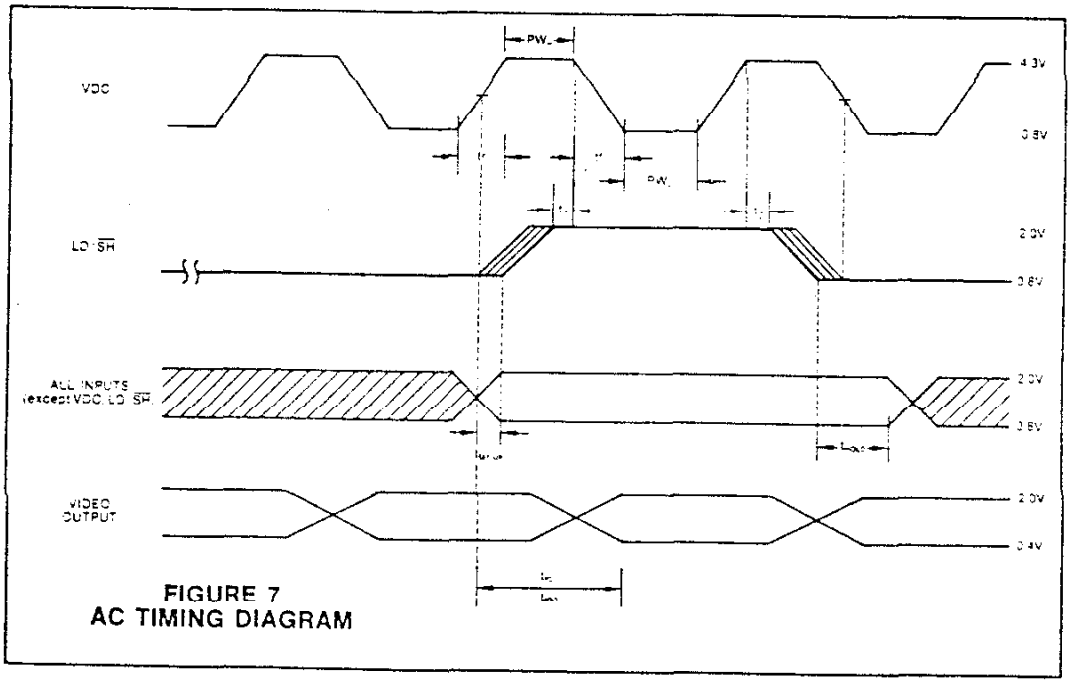


FIGURE 7
AC TIMING DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1	VIDEO	Video Output	O	The video output contains the dot stream for the selected row of the alphanumeric, wide graphic, thin graphic, or external character after processing by the attribute logic, and the retrace blank and cursor inputs. In the alphanumeric mode, the characters are ROM programmed into the 77 dots (7X11) allocated for each of the 128 characters. See figure 3. The top row (R0) and rows R12 to R15 are normally all zeros as is column C7. Thus, the character is defined in the box bounded by R1 to R11 and C0 to C6. When a row of the ROM, via the attribute logic, is parallel loaded into the 8-bit shift-register, the first bit serially shifted out is C7 (A zero, or a one in REVID). It is followed by C6, C5, through C0. The timing of the Load/Shift pulse will determine the number of additional (— —, zero to N) backfill zeros (or ones if in REVID) shifted out. See figure 4. When the next Load/Shift pulse appears the next character's row of the ROM, via the attribute logic, is parallel loaded into the shift register and the cycle repeats.
2	LD/SH	Load/Shift	I	The 8 bit shift register parallel-in load or serial-out shift modes are established by the Load/Shift input. When low, this input enables the shift register for serial shifting with each Video Dot Clock pulse. When high, the shift register parallel (broadside) data inputs are enabled and synchronous loading occurs on the next Video Dot Clock pulse. During parallel loading, serial data flow is inhibited. The Address/Data inputs (A0-A7) are latched on the negative transition of the Load/Shift input. See timing diagram, figure 7.
3	VDC	Video Dot Clock	I	Frequency at which video is shifted.
4-11	A0-A7	Address/Data	I	In the Alphanumeric Mode the 7 bits on inputs (A0-A6) are internally decoded to address one of the 128 available characters (A7 = X). In the External Mode, A0-A7 is used to insert an 8 bit word from a user defined external ROM, PROM or RAM into the on-chip Attribute logic. In the wide Graphic Modes A0-A7 is used to define one of 256 graphic entities. In the thin Graphic Mode A0-A2 is used to define the 3 line segments.
12	V_{cc}	Power Supply	PS	+5 volt power supply
13,14,15,16	R2,R3 R1,R0	Row Address	I	These 4 binary inputs define the row address in the current character block.
17	GND	Ground	GND	Ground
18	ATTBE	Attribute Enable	I	A positive level on this input enables data from the Reverse Video, Character Blank, Underline, Strike-Thru, Blink, Mode Select 0, and Mode Select 1 inputs to be strobed into the on-chip attribute latch at the negative transition of the Load/Shift pulse. The latch loading is disabled when this input is low. The latched attributes will remain fixed until this input becomes high again. To facilitate attribute latching on a character by character basis, tie ATTBE high. See timing diagram, figure 7.
19	STKRU	Strike-Thru	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SR0-SR7), providing a solid line segment throughout the character block. The operation of strike-thru is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which strike-thru is to be placed as well as to program the strike-thru to be 1 to N raster lines high. Actually, the strike-thru decoder (mask programmable) logic allows the strike-thru to be any number or arrangement of horizontal lines in the character block. The standard strike-thru will be a double line on rows R5 and R6.
20	UNDLN	Underline	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SR0-SR7), providing a solid line segment throughout the character block. The operation of underline is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which underline is to be placed as well as to program the underline to be 1 to N raster lines high. Actually, the underline decoder (mask programmable) logic allows the underline to be any number or arrangement of horizontal lines in the character block. The standard underline will be a single line on R11.
21	REVID	Reverse Video	I	When this input is low and RETBL = 0, data into the Attribute Logic is presented directly to the shift register parallel inputs. When reverse video is high data into the Attribute Logic is inverted and then presented to the shift register parallel inputs. This operation reverses the data and field video. See table 1.
22	CHABL	Character Blank	I	When this input is high, the parallel inputs to the shift register are all set low, providing a blank character line segment. Character blank will override blink. The operation of Character Blank is modified by the Reverse Video input. See table 1.
23	V SYNC	V SYNC	I	This input is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will be twice the character blink rate (75/25 duty cycle). The divisors can be programmed from ÷ 4 to ÷ 30 for the cursor (÷ 8 to ÷ 60 for the character).
24	BLINK	Blink	I	When this input is high and RETBL = 0 and CHABL = 0, the character will blink at the programmed character blink rate. Blinking is accomplished by blanking the character block with the internal Character Blink clock. The standard character blink rate is 1.875Hz.
25 26	MS1 MS0	Mode Select 1 Mode Select 0	I	These 2 inputs define the four modes of operation of the CRT 8002 as follows. Alphanumeric Mode – In this mode addresses A0-A6 (A7 = X) are internally decoded to address 1 of the 128 available ROM characters. The addressed character along with the decoded row will define a 7 bit output from the ROM to be loaded into the shift register via the attribute logic. Thin Graphics Mode – In this mode A0-A2 (A3-A7 = X) will be loaded into the thin graphic logic along with the row addresses. This logic will define the segments of a graphic entity as defined in figure 2. The top of the entity will begin on row 0000 and will end on a mask programmable row.

MS1	MS0	MODE
1	1	Alphanumeric
1	0	Thin Graphics
0	1	External Mode
0	0	Wide Graphics

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
25 26 (cont.)				External Mode – In this mode the inputs A0-A7 go directly from the character latch into the shift register via the attribute logic. Thus the user may define external character fonts or graphic entities in an external PROM, ROM or RAM. See figure 3. Wide Graphics Mode – In this mode the inputs A0-A7 will define a graphic entity as described in figure 1. Each line of the graphic entity is determined by the wide graphic logic in conjunction with the row inputs R0 to R3. In this mode each segment of the entity is defined by one of the bits of the 8 bit word. Therefore, the 8 bits can define any 1 of the 256 possible graphic entities. These entities can butt up against each other to form a contiguous pattern or can be interspaced with alphanumeric characters. Each of the entities occupies the space of 1 character block and thus requires 1 byte of memory. These 4 modes can be intermixed on a per character basis.
27	CURSOR	Cursor	I	When this input is enabled 1 of the 4 pre-programmed cursor modes will be activated. The cursor mode is on-chip mask programmable. The standard cursor will be a blinking (at 3.75 Hz) reverse video block. The 4 cursor modes are: Underline—In this mode an underline (1 to N raster lines) at the programmed underline position occurs. Blinking Underline—In this mode the underline blinks at the cursor rate. Reverse Video Block—In this mode the Character Block is set to reverse video. Blinking Reverse Video Block—In this mode the Character Block is set to reverse video at the cursor blink rate. The Character Block will alternate between normal video and reverse video. The cursor functions are listed in table 1.
28	RETBL	Retrace Blank	I	When this input is latched high, the shift register parallel inputs are unconditionally cleared to all zeros and loaded into the shift register on the next Load/Shift pulse. This blanks the video, independent of all attributes, during horizontal and vertical retrace time.

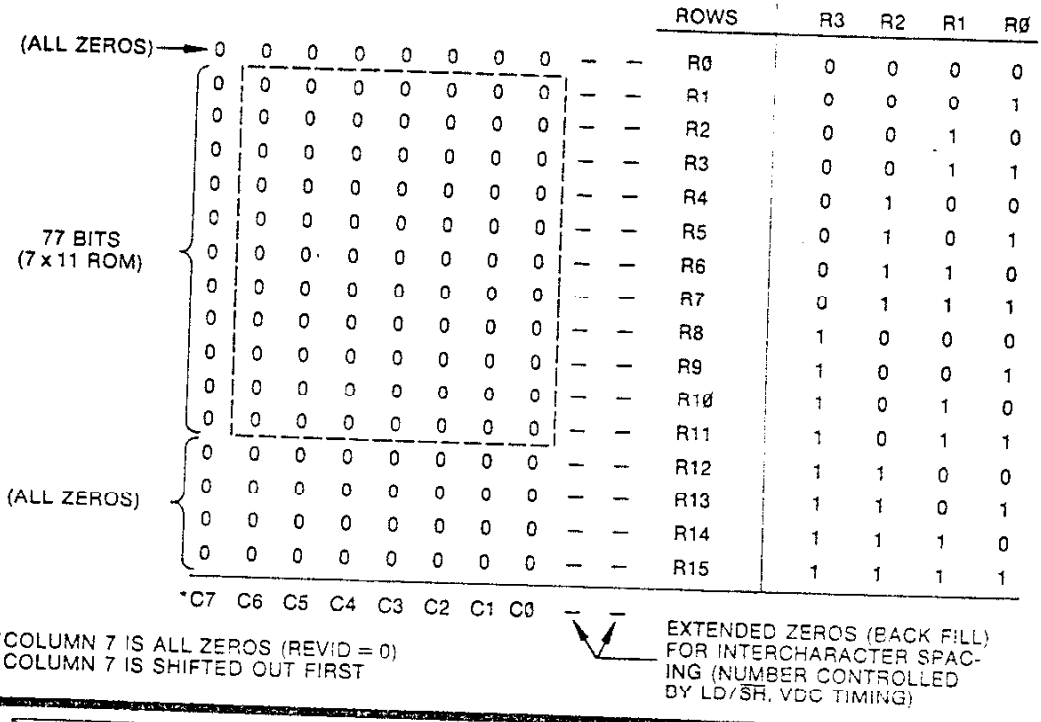
TABLE 1

CURSOR	RETBL	REVID	CHABL	UNDLN*	FUNCTION
X	1	X	X	X	"0" (S.R. All
0	0	0	0	0	D (S.R.) All
0	0	0	0	1	"1" (S.R.)*
					D (S.R.) All others
0	0	0	1	X	"0" (S.R.) All
0	0	1	0	0	D (S.R.) All
0	0	1	0	1	"0" (S.R.)*
					D (S.R.) All others
0	0	1	1	X	"1" (S.R.) All
Underline*	0	0	0	X	"1" (S.R.)*
					D (S.R.) All others
Underline*	0	0	1	X	"1" (S.R.)*
					"0" (S.R.) All others
Underline*	0	1	0	X	"0" (S.R.)*
					D (S.R.) All others
Underline*	0	1	1	X	"0" (S.R.)*
					"1" (S.R.) All others
Blinking** Underline*	0	0	0	X	"1" (S.R.)* Blinking
					D (S.R.) All others
Blinking** Underline*	0	0	1	X	"1" (S.R.)* Blinking
					"0" (S.R.) All others
Blinking** Underline*	0	1	0	X	"0" (S.R.)* Blinking
					D (S.R.) All others
Blinking** Underline*	0	1	1	X	"0" (S.R.)* Blinking
					"1" (S.R.) All others
REVID Block	0	0	0	0	D (S.R.) All
REVID Block	0	0	0	1	"0" (S.R.)*
					D (S.R.) All others
REVID Block	0	0	1	X	"1" (S.R.) All
REVID Block	0	0	0	1	"0" (S.R.)*
					D (S.R.) All others
REVID Block	0	1	0	0	D (S.R.) All
REVID Block	0	1	0	1	"1" (S.R.)*
					D (S.R.) All others
REVID Block	0	1	1	X	"0" (S.R.) All
Blink** REVID Block	0	0	0	0	Alternate Normal Video/REVID At Cursor Blink Rate
Blink** REVID Block	0	0	0	1	
Blink** REVID Block	0	0	1	X	
Blink** REVID Block	0	1	0	0	
Blink** REVID Block	0	1	0	1	
Blink** REVID Block	0	1	1	X	

*At Selected Row Decode **At Cursor Blink Rate

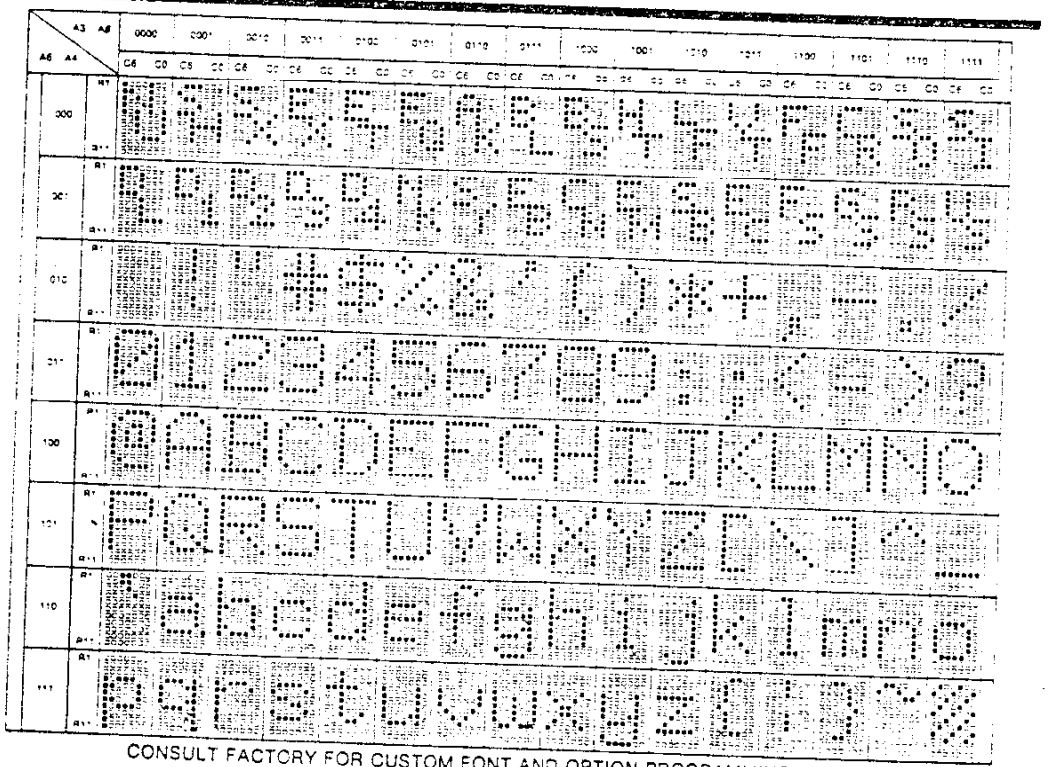
Note: If Character is Blinking at Character Rate, Cursor will change it to Cursor Blink Rate.

FIGURE 5
ROM CHARACTER BLOCK FORMAT



ROWS	R3	R2	R1	RØ
RØ	0	0	0	0
R1	0	0	0	1
R2	0	0	1	0
R3	0	0	1	1
R4	0	1	0	0
R5	0	1	0	1
R6	0	1	1	0
R7	0	1	1	1
R8	1	0	0	0
R9	1	0	0	1
R1Ø	1	0	1	0
R11	1	0	1	1
R12	1	1	0	0
R13	1	1	0	1
R14	1	1	1	0
R15	1	1	1	1

*COLUMN 7 IS ALL ZEROS (REVID = 0)
COLUMN 7 IS SHIFTED OUT FIRST



CONSULT FACTORY FOR CUSTOM FONT AND OPTION PROGRAMMING FORMS.

FIGURE 1
WIDE GRAPHICS MODE
MSØ=Ø MS1=Ø

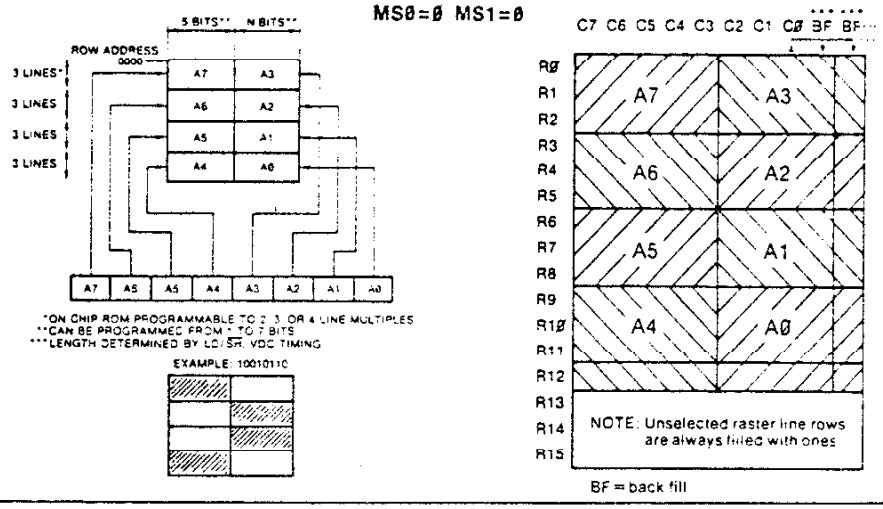


FIGURE 2
THIN GRAPHICS MODE
MSØ=Ø MS1=1

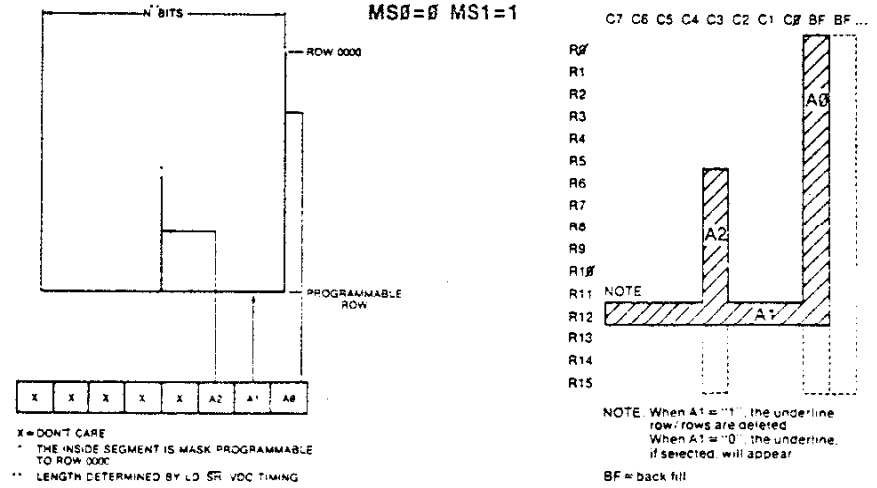
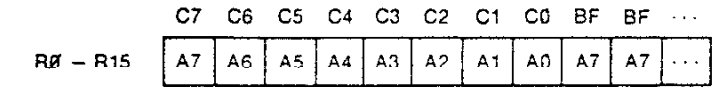
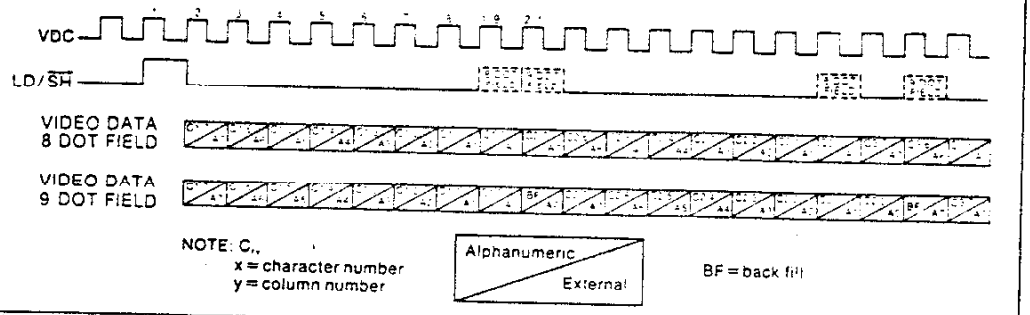


FIGURE 3
EXTERNAL MODE
MSØ=1 MS1=Ø



CRT 6

FIGURE 4 TYPICAL VIDEO OUTPUT



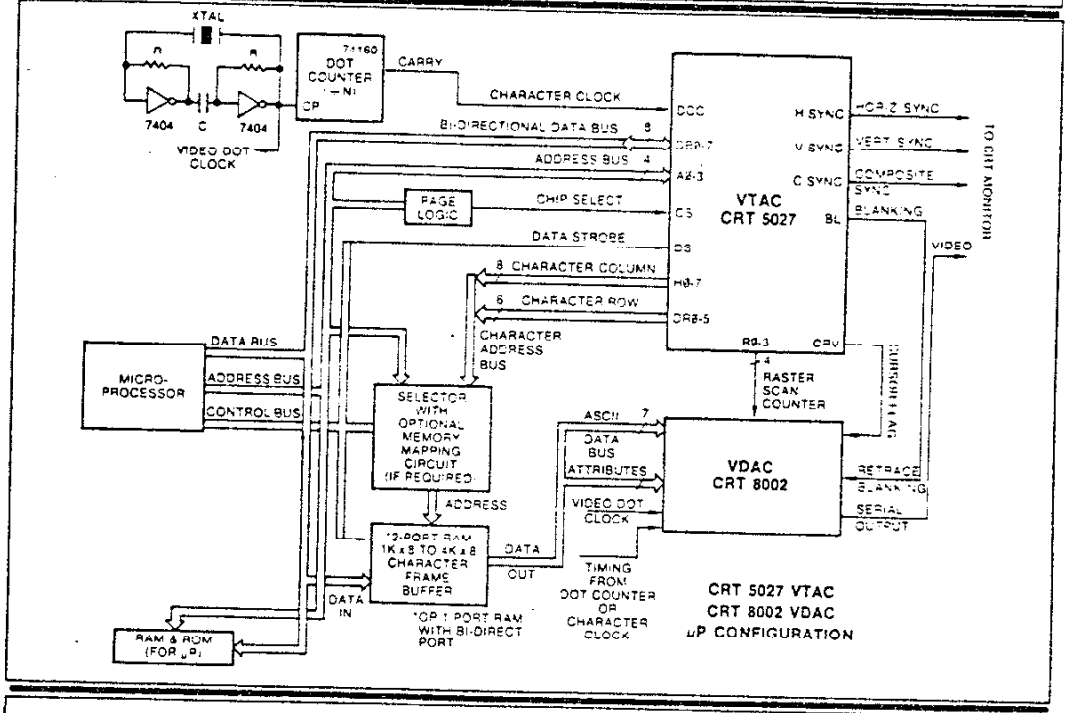
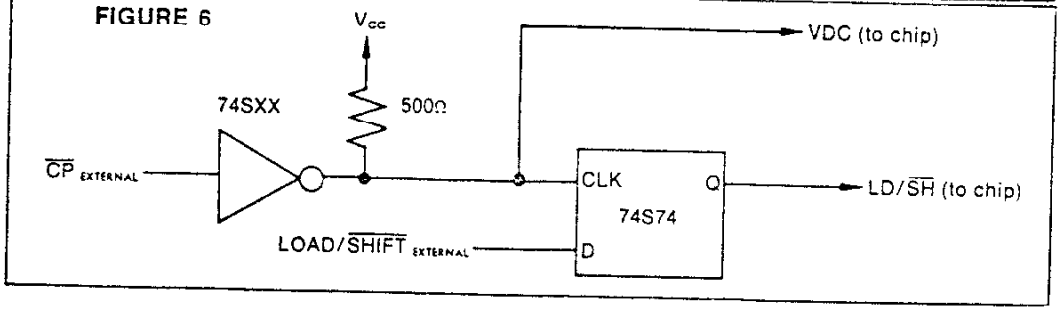


FIGURE 6



STANDARD MICROSYSTEMS CORPORATION

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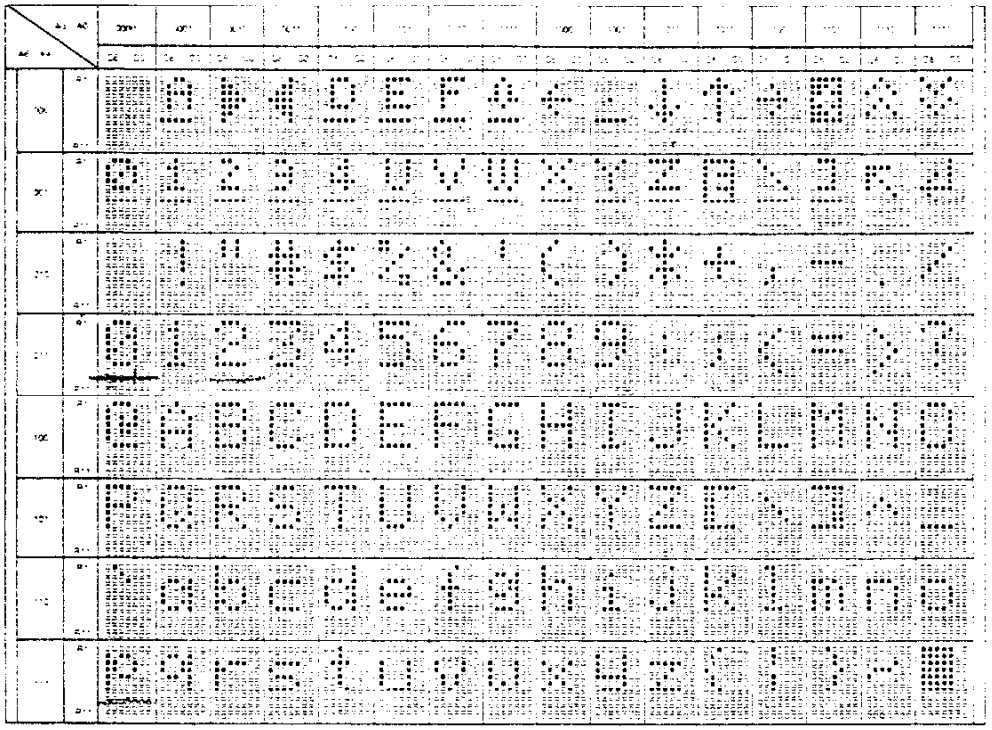
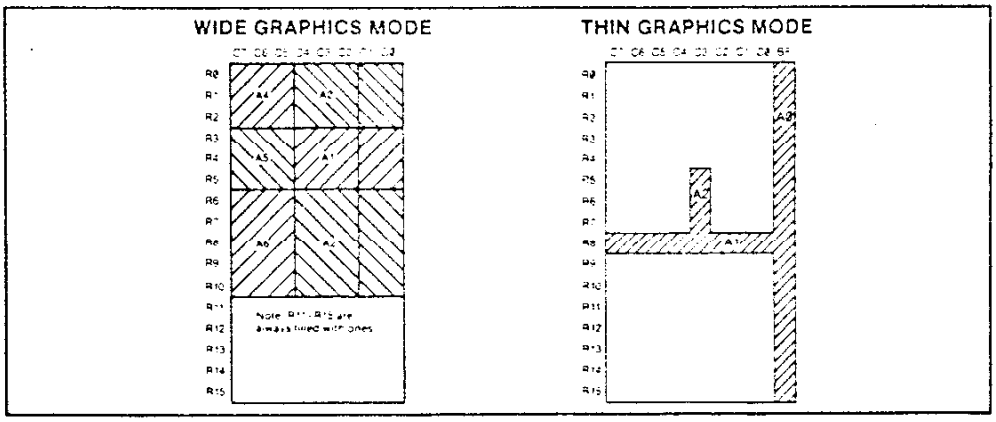
CRT 8002-003
(5 X 7 ASCII)
CODING INFORMATION

CRT Video Display-Controller Video Generator VDAC™





ATTRIBUTES

Underline
Underline will be a single horizontal line at R8

Cursor
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

Blink Rate
The character blink rate is 1.875 Hz

Strike-Thru
The strike-thru will be a single horizontal line at R4

National Semiconductor

AUGUST 1978

DP8350 Series Programmable CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock input may be used by the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMS, or DM8678-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, programmable vertical blanking, programmable horizontal sync, and programmable vertical sync.

The DP8350 Series CRTC provides for a wide range of programmability using internal mask programmable ROMs:

- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame

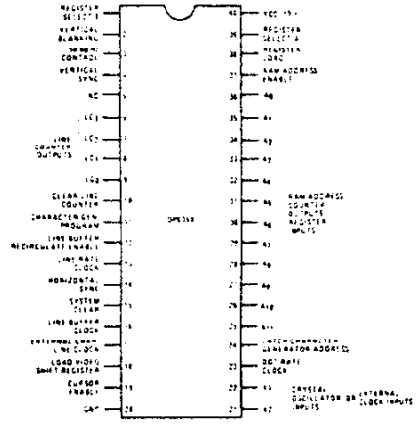
The CRTC also provides system sync and program inputs including 50/60 Hz control, system clear, external character/line rate clock, and character generator program.

The DP8350 Series operates on a single +5 V power supply. Outputs and inputs are TTL compatible.

Features

- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 50/60 Hz refresh rate
- Programmable characters/row (5 to 110)
- Programmable character field size (up to 16 dots x 16 scan line field size)
- Programmable character rows/frame (1 to 64)
- Single +5 V power supply
- Inputs and outputs TTL compatible
- Ease of system design application

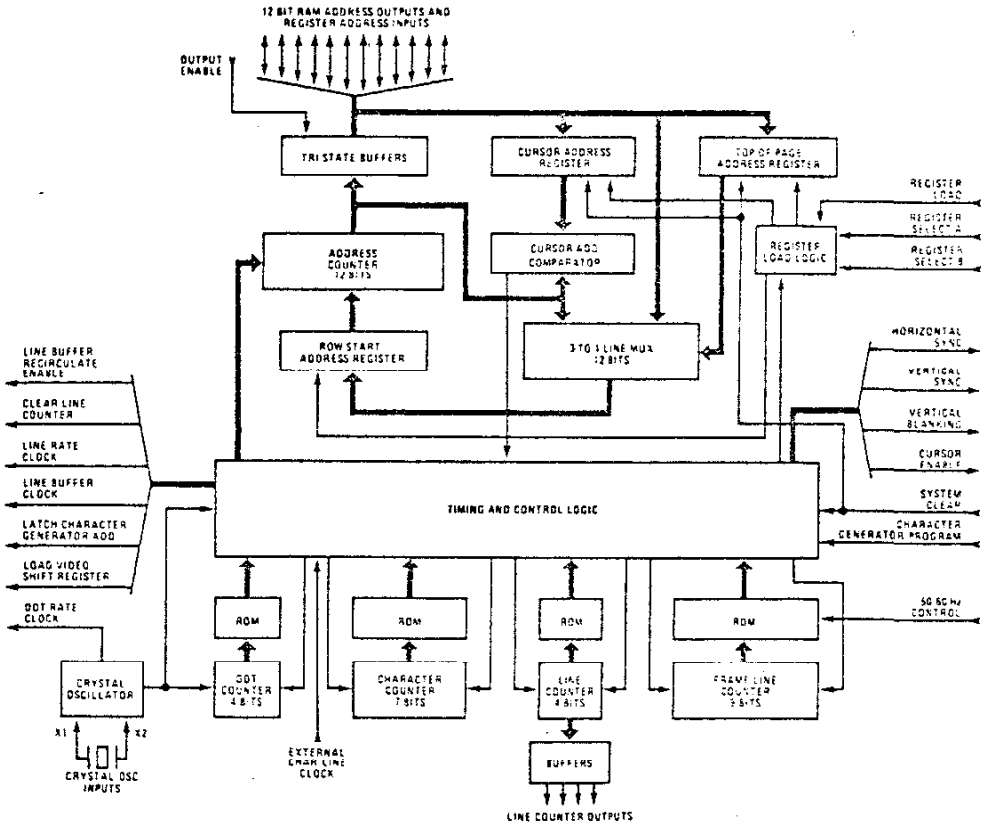
DP8350 Series Connnnection Diagram



8350-1

DA SIM88 Printed in U.S.A.

DP8350 Block Diagram



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DP8350 Functional Pin Description

CHARACTER GENERATION/TIMING OUTPUTS

The CRTC provides 11 interface timing outputs for line buffers, character generator ROM, DM8678-type latch/ROM/shift register combination character generators, and system status timing. All outputs are TTL compatible and directly interface to popular system circuits, including:

- DM8678 Series Character Generators
- MM52157, MM52179 Character ROMs
- DM74166 Dot Shift Register
- MK1007P, 33571/2, 2532 80-Bit Shift Registers (Line Buffers)

Dot Rate Clock: This output is buffered for use in system synchronization and interface to dot shift register. Positive edge clock at crystal oscillator frequency.

Load Video Shift Register: Buffered output at character rate frequency. Used for direct interface to dot shift register. This output is active only during video time and therefore performs both the horizontal and vertical blanking functions. Low level active.

Latch Character Generator Address: Buffered output at character rate frequency. Active at all times. Positive edge clock.

Line Buffer Clock: This output directly interfaces to line buffers. Output operates at character rate. Negative edge clock. Not active during horizontal blanking. The number of clocks per scan line is equivalent to the number of video characters per row.

Line Rate Clock: Line rate frequency output for use with DM8678-type character generator.

Line Counter Outputs (LC_0 to LC_3): Buffered outputs at line rate frequency for use with character ROMs without internal line counter. These outputs are also useful for system decode of present line position in character row. Outputs clock in sync with Line Rate Clock at start of horizontal blanking. Outputs are always active.

Clear Line Counter: Row rate clock – occurs in sync with Line Rate Clock during horizontal blanking between last line of any row and first line of a new row. This output is always active and is a negative edge clock – direct interface to the DM8678.

Line Buffer Recirculate Enable: This output interfaces to a line buffer and becomes inactive (logic "0" state) during the last line or the first line of a character row, depending on the state of the character generator program input. A low level on this output indicates (in line buffer applications) the time during which the line buffer is loaded with the next row of character codes.

Table 1. Character Generator Program Truth Table

Character Generator Program Input	Recirculate Enable Output Low Level and New Row Address at Address Outputs
"0"	Last line of character row
"1"	First line of character row

The pulse appears at the start of horizontal blanking prior to when the memory address bus must be transferred to the CRTC, then returns to the high state at the next horizontal blanking interval.

MEMORY ADDRESS OUTPUTS/INPUTS AND REGISTERS

CRT Character Address Outputs (TRI-STATE) – A_0 to A_{11}: 12 bits of bidirectional CRT character address counter outputs are provided by the CRTC. These outputs directly interface to the system RAM memory address bus.

Within a scan line the counter is pre-set to the address contained within the Row Start Register (RSR) three character times before the start of video time. The counter is then advanced sequentially at character rate to the max video character address plus 1 for the present scan line. This address is then held during the horizontal blanking interval up to three character times before video start for the next scan line. At this point the counter is again pre-set to the contents of the RSR and the above sequence is repeated. This sequence provides scan line address repetition for every scan line of a character location within a row. Row-to-row start address modifications are accomplished by updating the contents of the RSR.

During vertical blanking the address counter operation is modified by stopping the pre-set load of the contents of the RSR into the address counter, thereby allowing the address outputs to free run during vertical blanking. This allows minimum access time to the CRTC when the CRTC address counter outputs are being used for dynamic RAM refresh.

RAM Address Enable Input: At all times the status of the address counter outputs is controlled externally by the Enable Input. Logic "0" = TRI-STATE. Logic "1" = Active.

Internal Top-of-Page, Row Start, and Cursor Registers: Control pins are provided for loading the top-of-page, row start, and cursor address into three 12 bit CRTC registers from the bidirectional memory address pins.

The Top-of-Page Register (TOPR) holds the address of the first character of the first video row. This register allows display scroll with the CRTC without the use of external memory address adders. If the TOPR is not loaded after a system clear its contents will be zero and the address outputs will be sequential from zero at the top-of-page.

The Cursor Register (CR) holds the present address of the cursor and is cleared to zero after a system clear. Once the TOPR and CR registers have been loaded they need not be accessed again until modification of their contents is required. These registers may be loaded at any time, but to cause minimum display distortion it is recommended that they be loaded only during blanking intervals.

8350-3

The Row Start Register (RSR) is the working register for the CRTC address counter. It determines the first video character address on a scan line to scan line basis.

Modification of this register after the start of video in a scan line will modify the address counter outputs at the start of video on the next scan line. (See address output description.) If the RSR is never externally loaded, the CRTC address outputs will be sequential on a row-to-row basis from the TOPR contents at the start of the video page. With external loading, row-to-row non-sequential operation of the CRTC address outputs is possible, thus row-to-row edit capability. When used in this mode the RSR should be loaded after the start of video time of the last scan line of the previous row. A load to the RSR during vertical blanking will also load the TOPR.

Table 2. Register Load Truth Table

Register Select A	Register Select B	Register Load Input	Register Access
0	0	0	No Select
0	1	0	Top-of-Page
1	0	0	Row Start*
1	1	0	Cursor
X	X	1	No Select

*During vertical blanking a load to this register will also load the top-of-page register.

VIDEO RELATED OUTPUTS

Horizontal Sync: This output provides the necessary line (scan) rate sync to either three-terminal or composite sync monitors. The pulse is programmable in position and width at character time increments. This output may also be programmed to have RS-170 compatible serration pulses during the vertical sync interval. The active logic state of this output is also programmable.

Vertical Sync: This output provides the necessary frame rate sync consistent with either three-terminal or composite type monitors. The pulse is programmable in position and width at line (scan) time increments. The active logic state of this output is also programmable.

Cursor Enable: When a match with the CRTC cursor address register and address counter occurs a pulse will appear at this output at that video character time (character field width) for every line in that row. This output may also be programmed to appear on only one line of a character row. With the character generator program pin in a logic "0" position the cursor enable output will not be valid on the last line of a character row for that row. Like the Load Video Shift Register Output, this output is not active during horizontal or vertical blanking. High level active output.

CRT SYSTEM CONTROL FUNCTIONS

50/60 Hz Control Input: This input controls the CRT system refresh rate. The CRTC may also be programmed for refresh rates other than 50 and 60 Hz.

50/60 Hz Control	Refresh Rate
1	60 Hz (f_1)
0	50 Hz (f_0)

Vertical Blanking Output: This output becomes active (logic "1") at the start of vertical blanking and may be programmed to stop at the end of any line of the character row before the start of the first video row. This output is useful for flag applications to other elements in the CRT system. Its active level is also programmable.

System Clear Input: This input when low sets and holds the CRTC at the start of vertical blanking for system sync and test. It also clears to zero the cursor and top-of-page registers. The input has hysteresis and may be connected to a resistor to V_{CC} and a capacitor to ground to provide power-up system clear.

Character Generator Program Input: This input modifies both the position of the recirculate enable output low level and the time at which the address outputs change to a new row address. It is intended to provide optimum use of the CRTC with character generator/ROMs programmed with or without active video on the first or last line of a character row. (See Recirculate Enable for truth table.)

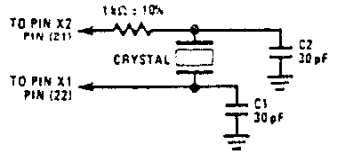
External Character/Line Rate Clock: This input is intended to aid testing of the CRTC and is not meant to be used as an active input in a CRT system. When this input is left open it is guaranteed not to interfere with normal operation.

Crystal Inputs X1 and X2: The oscillator is controlled by an external, parallel resonant crystal connected between the X1 and X2 pins. Normally, a fundamental mode crystal is used to determine the operating frequency of the oscillator; however, overtone mode crystals may be used.

Crystal Specifications (parallel resonant):

Type . . . . . AT-Cut Crystal
Tolerance . . . . . 0.005% at 25°C
Stability . . . . . 0.01% from 0°C to +70°C
Resonance . . . . . Fundamental (parallel)
Maximum Series Resistance . . . . . Dependent on frequency (for 10.92 MHz, 50 Ω)
Load Capacitance . . . . . 20 pF

Connection Diagram



If the DP8350 series is clocked at dot rate by a system clock, pin 22 (X1 input) should be clocked directly using a Schottky series circuit. Pin 21 (X2 input) may be left open.

8350-4

Timing Waveforms

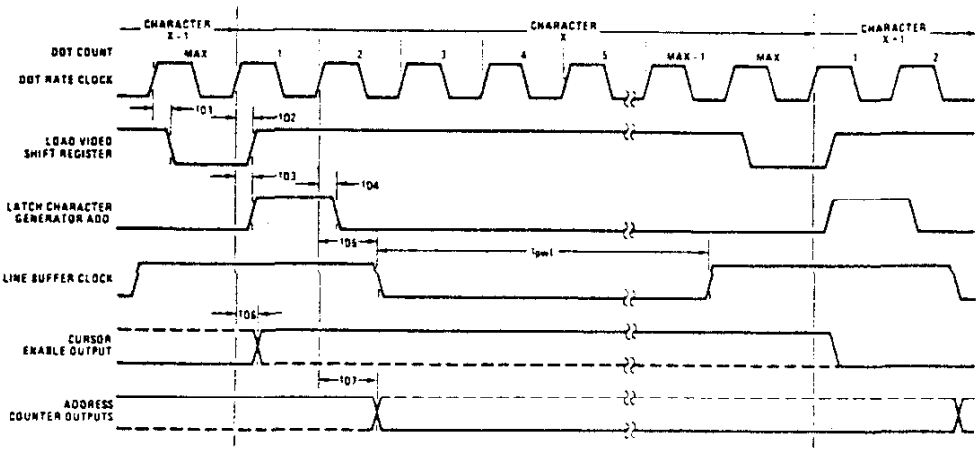
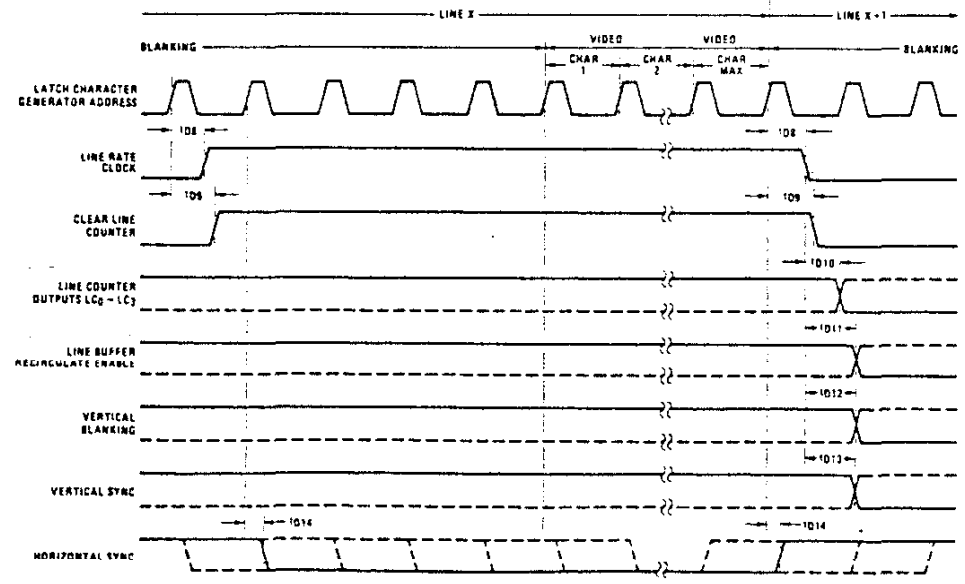


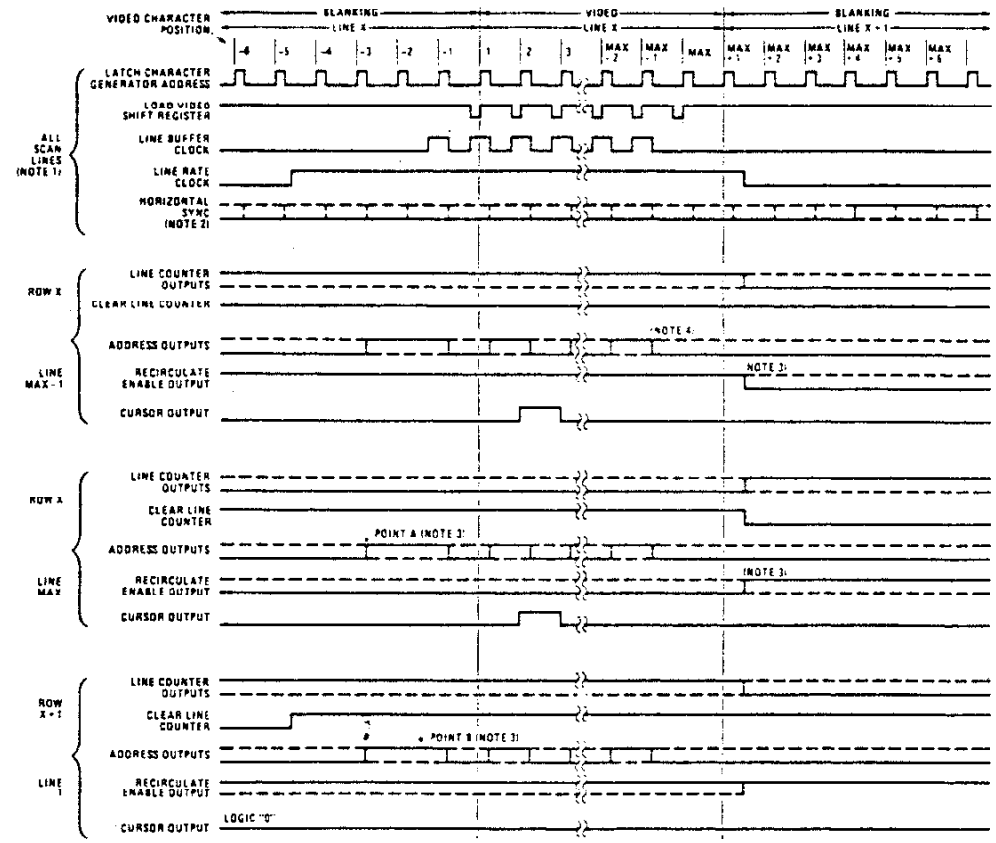
Figure 1. Dot/Character Rate Timing



*THE POSITION OF THE START AND STOP POINTS OF THE HORIZONTAL SYNC PULSE ARE PROGRAMMABLE BY CHARACTER TIME - WITHIN ONE CHARACTER TIME THE POINTS WILL HAVE THE t_{014} TIME RELATIONSHIP

Figure 2. Character/Line Rate Timing

Timing Waveforms (cont'd.)



Note 1: The load video shift register output is not active during vertical or horizontal blanking (remains in the logic "1" state during these intervals.

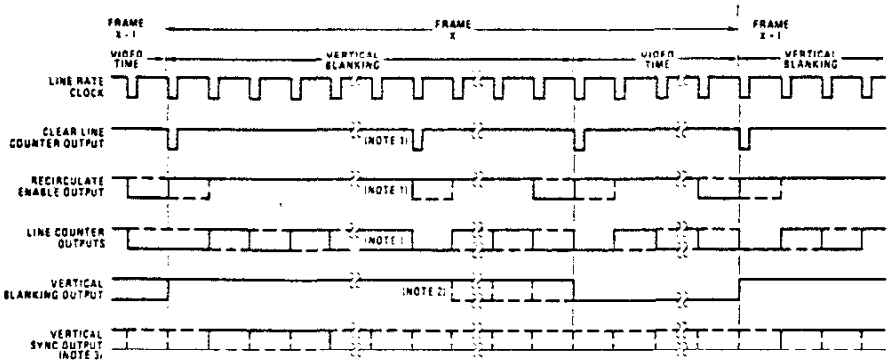
Note 2: The horizontal sync output start and stop point positions are user-programmable at character width intervals.

Note 3: The position of the recirculate enable output logic "0" level is dependent on the state of the character generator program input (CGPI). With CGPI = "0," recirculate enable occurs on the max line of a character row (solid line) and the address counter outputs roll over to the new row address at point A. With CGPI = "1," recirculate enable occurs on the first line of a character row (dashed line) and the address counter outputs roll over to the new row address at point B.

Note 4: The address counter outputs clock to the address of the last character of a video row plus 1. This address is then held during the horizontal blanking interval until video minus three character times. At this point the outputs are modified to the contents of the Row Start Register (RSR). With no external loading of the RSR the contents will be either the character address of the first character in the present row or the character address of the first character of the next video row (depending on the state of the Character Generator Program input) which will be sequential from the last character address of the last row. If the RSR was loaded, then the address outputs will be modified to the contents of the register.

Figure 3. Character/Line Rate Functional Diagram

Timing Waveforms (cont'd.)

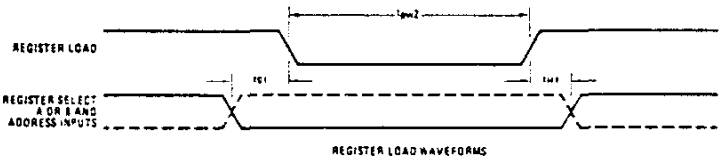


Note 1: One full row before start of video the line counter is set to zero state – this provides line counter synchronization in cases where the number of lines in vertical blanking are not even multiples of the number of lines per row.

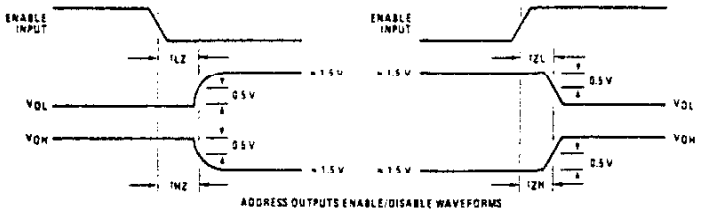
Note 2: The stop point of vertical blanking is programmable at line intervals within the last character row before start of video.

Note 3: The Vertical Sync Output start and stop points are programmable at line rate increments.

Figure 4. Line/Frame Rate Functional Diagram

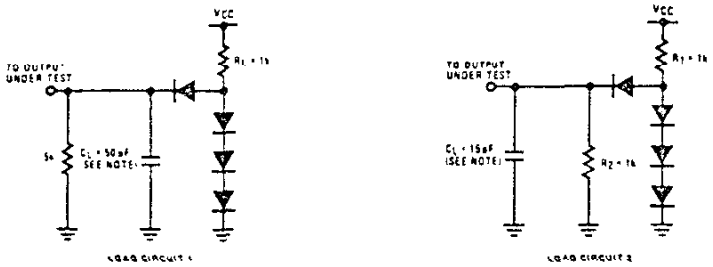


REGISTER LOAD WAVEFORMS



ADDRESS OUTPUTS ENABLE/DISABLE WAVEFORMS

Test Load Circuits



NOTE C_L INCLUDES PROBE AND JIG CAPACITANCE
ALL DIODES ARE 1N914 OR EQUIVALENT

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0 V
Input Voltage	−1 V to +5.5 V
Output Voltage	5.5 V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5 V ± 5%, T_A = 0°C to +70°C (Notes 2 and 3)

	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage					
	(System Clear)		2.6			V
	(All Other Inputs Except X1, X2)		2.0			V
V_{IL}	Logic "0" Input Voltage					
	(System Clear)				0.8	V
	(All Other Inputs Except X1, X2)				0.8	V
$V_{IH}-V_{IL}$	System Clear Input Hysteresis			0.4		V
V_{clamp}	Input Clamp Voltage (All Inputs Except X1, X2, & Char. Line Rate Clock)	I_{IN} = −12 mA		−0.8		V
I_{IH}	Logic "1" Input Current					
	(Address Outputs)	Enable Input = 0 V, V_{CC} = 5.25 V, V_R = 5.25 V		10		μA
	(All Other Inputs Except X1, X2)	V_{CC} = 5.25 V, V_R = 5.25 V		2		μA
I_{IL}	Input Current					
	(Address Outputs)	Enable Input = 0 V, V_{CC} = 5.25 V, V_{IN} = 0.5 V		−20		μA
	(All Other Inputs Except X1, X2)	V_{CC} = 5.25 V, V_{IN} = 0.5 V		−20		μA
V_{OH}	Logic "1" Output Voltage	I_{OH} = −100 μA	3.2	4.1		V
		I_{OH} = −1 mA	2.5	3.3		V
V_{OL}	Logic "0" Output Voltage	I_{OL} = 5 mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	V_{CC} = 5 V, V_{OUT} = 0 V, (Note 4)		−40		mA
I_{CC}	Power Supply Current	V_{CC} = 5.25 V		170		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min./max. limits apply across the 0°C to +70°C temperature range and the 4.75 V to 5.25 V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0 V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max. or min. are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

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Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C (Notes 1 and 2)

	Parameter	Conditions	Min	Typ	Max	Unit
t_{D1}	Dot Clock to Load Video Shift Register Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		5		ns
t_{D2}	Dot Clock to Load Video Shift Register Positive Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		11		ns
t_{D3}	Dot Clock to Latch Character Generator Positive Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		11		ns
t_{D4}	Dot Clock to Latch Character Generator Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		4		ns
t_{D5}	Dot Clock to Line Buffer Clock Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		20		ns
t_{PW1}	Line Buffer Clock Pulse Width	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		N(DT)*		ns
t_{D6}	Dot Clock to Cursor Enable Output Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		25		ns
t_{D7}	Dot Clock to Valid Address Output	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		20		ns
t_{D8}	Latch Character Generator to Line Rate Clock Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		300+2DT		ns
t_{D9}	Latch Character Generator to Clear Line Counter Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		400+2DT		ns
t_{D10}	Line Rate Clock to Line Counter Output Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		180		ns
t_{D11}	Line Rate Clock to Line Buffer Recirculate Enable Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D12}	Line Rate Clock to Vertical Blanking Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D13}	Line Rate Clock to Vertical Sync Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D14}	Latch Character Generator to Horizontal Sync Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		100		ns
t_{SI}	Register Select/Memory Address Setup Time Prior to Register Load Negative Edge			100		ns
t_{HI}	Register Select Memory Hold Time After Register Load Positive Edge			0		ns
t_{PW2}	Register Load Pulse Width			150		ns
f_{MAXdot}	Maximum Dot Rate Frequency			25		MHz
$f_{MAXchar}$	Maximum Character Rate Frequency			2.5		MHz
t_{LZ}, t_{HZ}	Delay from Enable Input to High Impedance State from Logic "0" and Logic "1"	C_L = 15 pF, Load Circuit 2		25		ns
t_{ZL}, t_{ZH}	Delay from Enable Input to Logic "0" and Logic "1" from High Impedance State	C_L = 15 pF, Load Circuit 2		25		ns

Note 1: Unless otherwise specified, all AC measurements are referenced to the 1.5 V level of the input to 1.5 V of the output.

Note 2: When external clock inputs are used, the input characteristics are Z_{OUT} = 50 Ω and t_R ≤ 10 ns, t_F ≤ 10 ns.

*"DT" is defined as the duration (in ns) of one full cycle of the Dot Rate Clock (Item 20 of the ROM Program Table). "N" denotes the number of DTs per definition in Item 24 of the ROM Program Table.

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DP8350 Series Option Program Table (Notes 1, 2, and 3)

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character		
2		Scan Lines per Character		
3	Character Field (Block Size)	Dots per Character		
4		Scan Lines per Character		
5	Number of Video Characters per Row			
6	Number of Video Character Rows per Frame			
7	Number of Video Scan Lines (Item 4 x Item 6)			
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 =	f0 =
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)			
10	Vertical Sync Width (Number of Scan Lines)			
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)			
12	Total Scan Lines per Frame (Item 7 + Item 11 = Item 13 ÷ Item 8)			
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)			
14	Number of Character Times per Scan Line			
15	Character Clock Rate (MHz) Item 13 x Item 14)			
16	Character Time (ns) (1 ÷ Item 15)			
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)			
18	Horizontal Sync Width (Character Times)			
19	Dot Frequency (MHz) (Item 3 x Item 15)			
20	Dot Time (ns) (1 ÷ Item 19)			
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)			
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?			
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)			
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)			
25	Serration Pulse Width, if used (Character Times)			
26	Horizontal Sync Pulse Active state logic level (1 or 0)			
27	Vertical Sync Pulse Active state logic level (1 or 0)			
28	Vertical Blanking Pulse Active state logic level (1 or 0)			

Note 1: If the Cursor Enable, Item 22, is active on only one line of a character row, then Item 21 must be either "1" or "0" unless it is the same as the line selected for Cursor Enable.

Note 2: Item 24 x Item 20 should be ~ 250 ns.

Note 3: Item 11 must be greater than Item 4 + 1

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DP8350 Series Option Program Table

DP8350 Option: 80 Characters x 24 Rows, 5 x 7 Character Font, 7 x 10 Character Field

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character	5	7
2		Scan Lines per Character	7	
3	Character Field (Block Size)	Dots per Character	7	
4		Scan Lines per Character	10	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		24	
7	Number of Video Scan Lines (Item 4 x Item 6)		240	
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 = 60 Hz	f0 = 50 Hz
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)		4	30
10	Vertical Sync Width (Number of Scan Lines)		10	10
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)		20	72
12	Total Scan Lines per Frame (Item 7 + Item 11 + Item 13 ÷ Item 8)		260	312
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)		15.6 kHz	19.2
14	Number of Character Times per Scan Line		100	102
15	Character Clock Rate (MHz) Item 13 x Item 14)		1.56 MHz	1.9584
16	Character Time (ns) (1 ÷ Item 15)		641 ns	510.6
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)		0	5
18	Horizontal Sync Width (Character Times)		43	9
19	Dot Frequency (MHz) (Item 3 x Item 15)		10.920 MHz	17.625
20	Dot Time (ns) (1 ÷ Item 19)		91.6 ns	56.7
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)		1	1
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?		Yes	YES
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	NO
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		4	5
25	Serration Pulse Width, if used (Character Times)		–	–
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	1
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	1
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	1

FULL/HALF ROW CONTROL (PIN 5)

Device pin 5 converts the DP8350 programmed display from 80 characters by 24 rows to 80 characters by 12 rows.

Full/Half Row (Pin 5) Logic State	Display Size
1	80 by 24
0	80 by 12

With pin 5 in logic "0" state, the 12 character rows are equally spaced vertically on the CRT. Each row is spaced by one full row of blanked video.

Also in this mode the address counter outputs address the same memory space for two rows – the video row and the blanked row. Thus one half of the CRT memory space is addressed with pin 5 in logic "0" state as compared to pin 5 in logic "1" state.

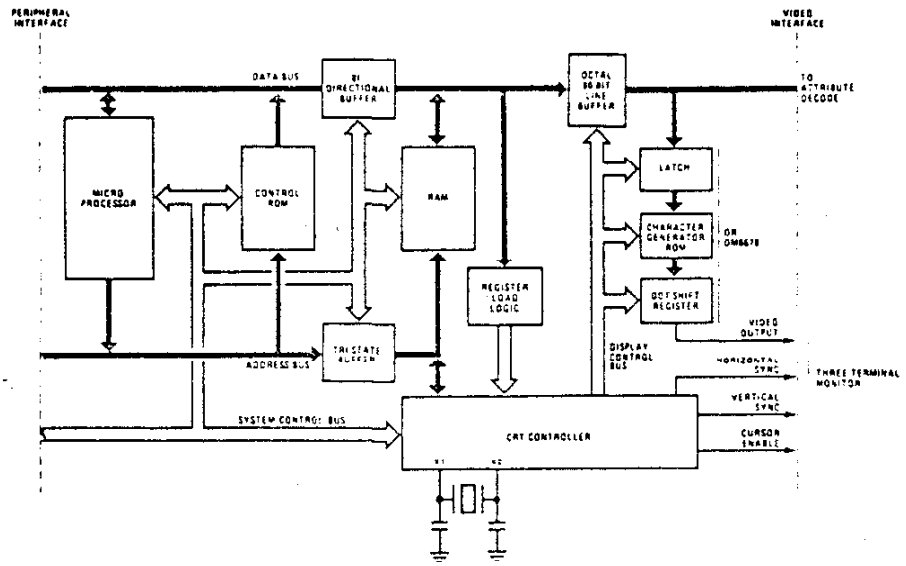

Figure 6. System Diagram Using a Line Buffer

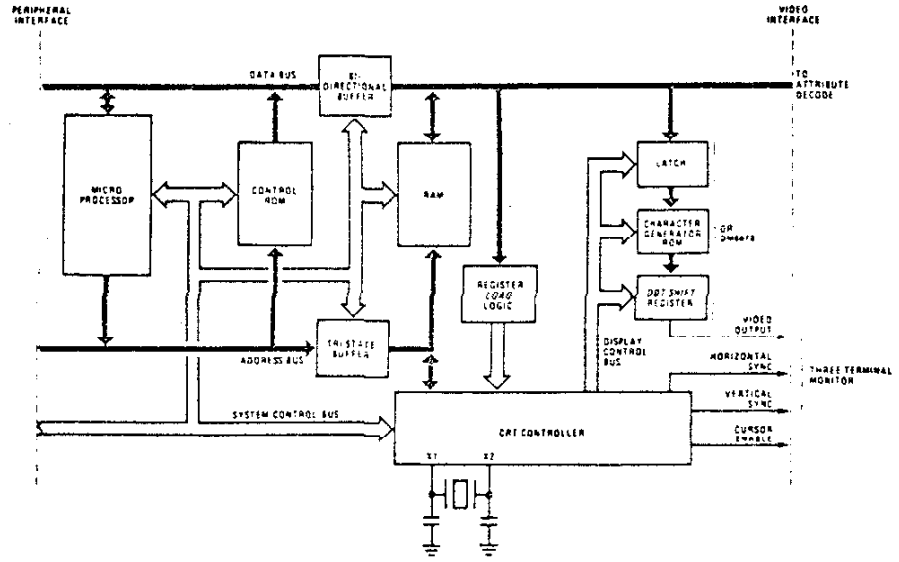

Figure 7. System Diagram with no Line Buffer

Note 1: If the Cursor Enable, Item 22, is active on only one line of a character row, then Item 21 must be either "1" or "0" unless it is the same as the line selected for Cursor Enable.

Note 2: Item 24 x Item 20 should be ≥ 250 ns.

Note 3: Item 11 must be greater than Item 4 + 1.

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