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METRIC

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MODELS 8/32C AND 8/32D PROCESSORS
CUSTOMER INSTALLATION MANUAL

PERKIN-ELMER

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PREFACE

This manual provides the customer with the information necessary to install a Model 8/32C or 8/32D processor. It includes information on unpacking, configurations, power supplies and testing. In addition, sections on the WCS, DFU, and Communication Instruction Package are included.

CAUTION

THE MODEL 8/32C USES 32KB MEMORY MODULES (32-206) EXPANDABLE UP TO EIGHT 128KB EXPANSIONS. THE MODEL 8/32D USES 64KB MEMORY MODULES (32-209) EXPANDABLE UP TO FOUR 256KB EXPANSIONS.

THE INTERMIXING OF 32KB MODULES WITH 64KB MODULES IS NOT PERMITTED AND IS NOT SUPPORTED BY INTERDATA. UNPREDICTABLE RESULTS MAY OCCUR.

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CHAPTER 1
MODELS 8/32C AND 8/32D
INSTALLATION

1.1 INTRODUCTION

This chapter provides installation information for INTERDATA Models 8/32C and 8/32D Digital Systems.

The INTERDATA Models 8/32C and 8/32D Digital Systems feature a highly modular structure which permits configuration to suit the user's exact needs. It provides the means for convenient expansion as the user's requirements increase. This chapter describes the Processor and Expansion chassis, Power Supply cabling and mounting, Filler and Display Panel mounting, cooling, and the interconnecting cables. Printed circuit board cabling and location are discussed. Circuit descriptions of these boards are provided in the appropriate maintenance or instruction manuals.

NOTE

It is assumed that the equipment is mounted in standard INTERDATA cabinets.

1.2 UNPACKING

Read the following procedures before starting an installation.

1. Carefully remove each component from its carton or crate, observing any special unpacking instructions included with the component.
2. Inspect all components for physical damage.
3. If the system is shipped from INTERDATA already rack mounted, insure that all terminals and connectors are secured properly.

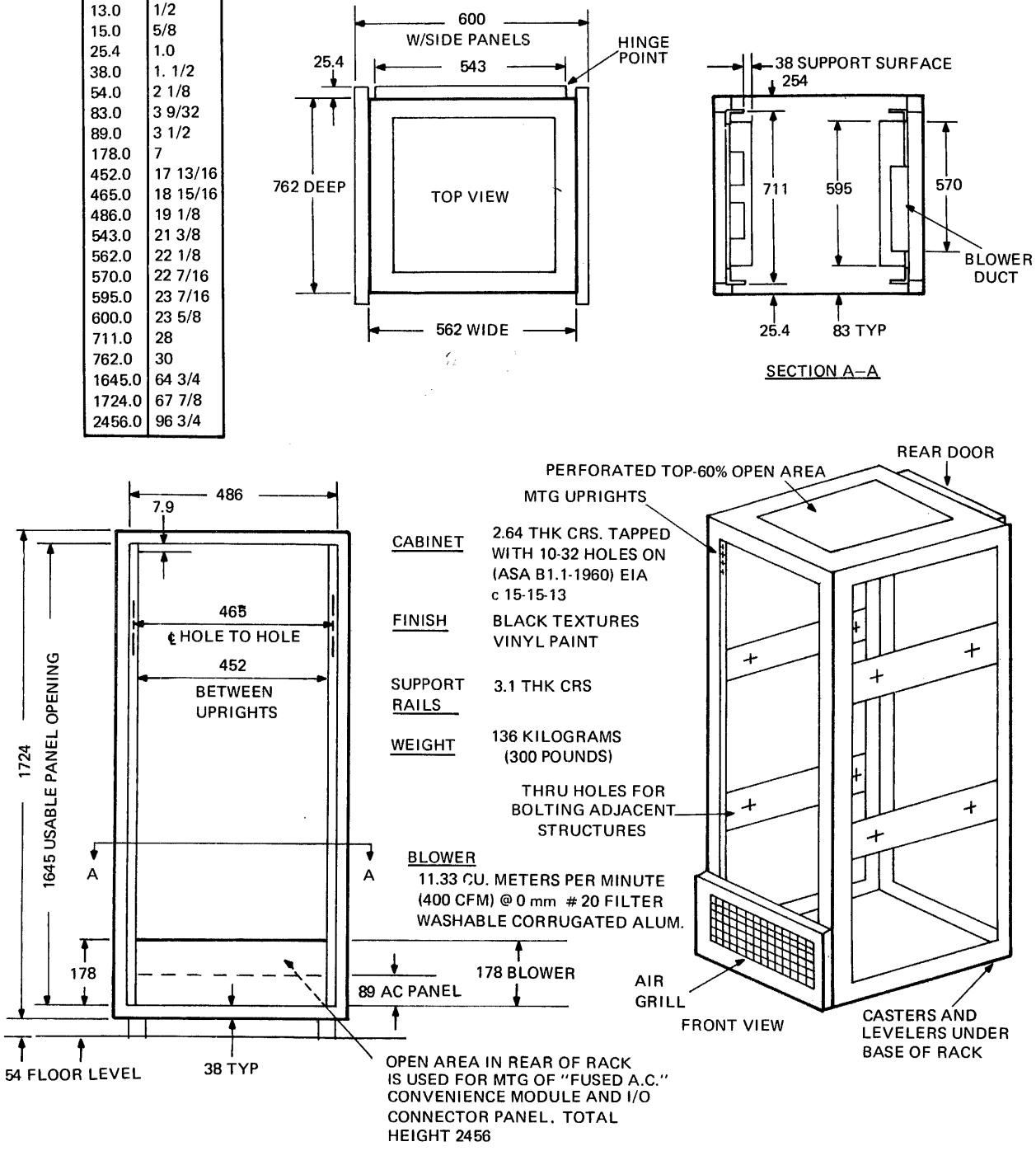
1.3 MECHANICAL CONFIGURATION

1.3.1 Mechanical Components

Figures 1-1 and 1-2 illustrate the mechanical components of a typical INTERDATA Digital System. Dimensions and mounting information are provided for the System Cabinet, Chassis Support Rails, Display and Filler Panels. Note in Figure 1-2 that, while the 133 mm (5¼"), 178 mm (7"), 222 mm (8¾"), 270 mm (10½") Filler Panels, and the Display Panel mount the same way (via retaining brackets), the smaller 44.5 mm (1¾") Filler Panel mounts with spring clips.

CONVERSION TABLE

MM	INCH
0.	0.
2.6	.104
3.1	1/8
13.0	1/2
15.0	5/8
25.4	1.0
38.0	1. 1/2
54.0	2 1/8
83.0	3 9/32
89.0	3 1/2
178.0	7
452.0	17 13/16
465.0	18 15/16
486.0	19 1/8
543.0	21 3/8
562.0	22 1/8
570.0	22 7/16
595.0	23 7/16
600.0	23 5/8
711.0	28
762.0	30
1645.0	64 3/4
1724.0	67 7/8
2456.0	96 3/4



NOTE: ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED. USE TABLE FOR CONVERSION TO ENGLISH UNITS.

Figure 1-1. System Cabinet Physical Dimensions

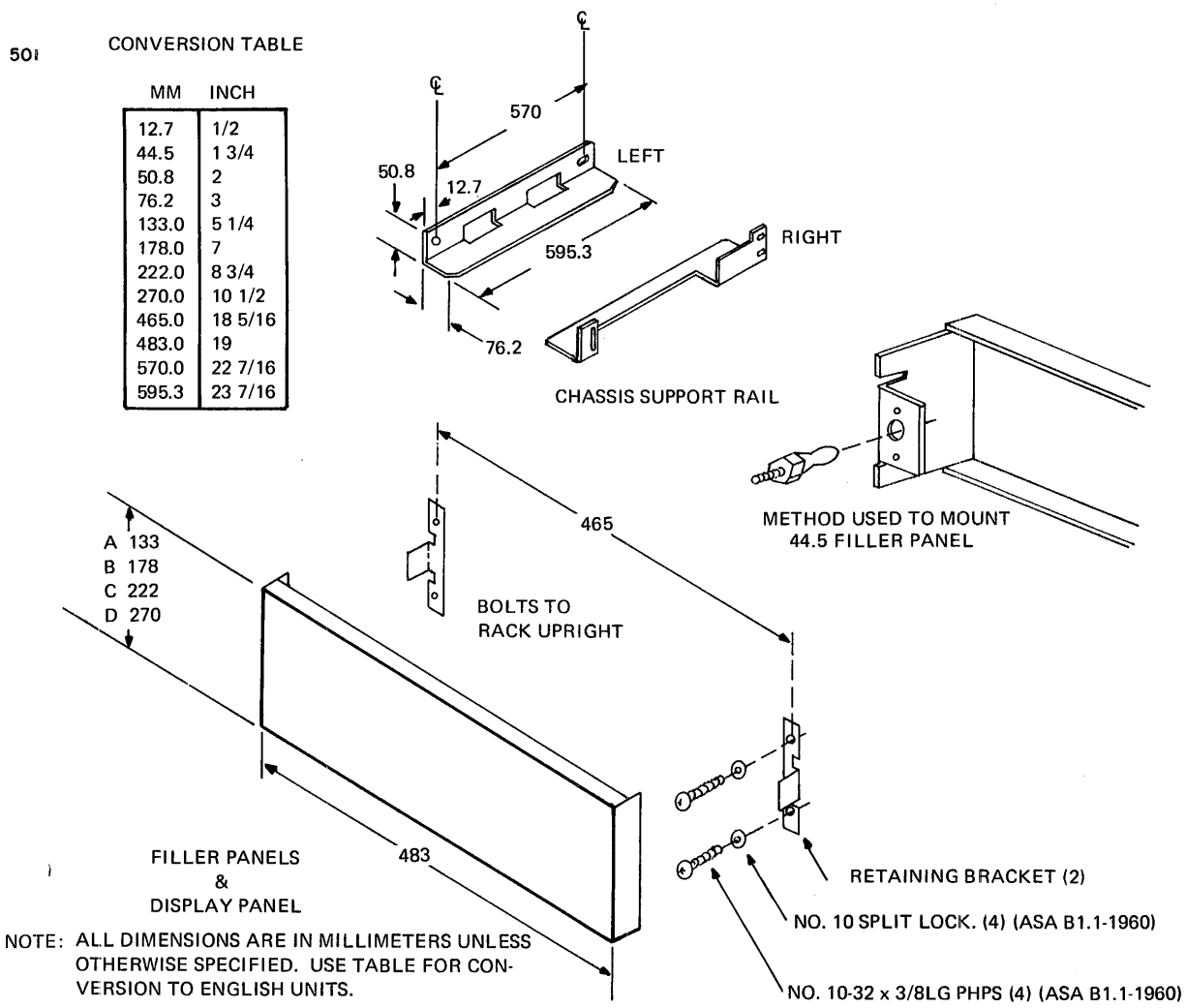


Figure 1-2. Typical Mounting Configuration for Display and Filler Panels

1.3.2 Cooling (See Figures 1-3 through 1-6.)

The cabinet is cooled by a packaged blower located at the bottom of the cabinet (see Figure 1-3), using forced air at ambient room temperature. The air is distributed by an internal plenum located along the right side of the cabinet opening (as viewed from the front). The air input to the blower enters directly into the bottom section of the plenum (Figure 1-4). The plenum contains seven removable covers located vertically in the appropriate spaces as illustrated by Figure 1-4.

The blower must be plugged into the AC panel at the rear of the cabinet, and the main circuit breaker on the AC panel must be in the ON position to power up the system.

The blower air switch, located on the side of the plenum system (Figure 1-4), is wired per Figure 1-7.

The blower must remain on for a minimum of five minutes after the Display Panel's LOCK-ON-OFF switch is turned OFF.

The blower is shut off by the main circuit breaker on the AC power panel.

A removable and washable filter is located behind the air intake grille.

Two types of covers are provided, solid and perforated (see Figures 1-5 and 1-6). Solid covers are snapped in place at locations where there are no chassis. Perforated covers are used in locations having an operating chassis.

For the Model 8/32C or 8/32D with no expansion, perforated covers are installed at Locations 4 and 5, and solid covers are installed in all other locations. If, at a later date, the first memory expansion is added, the solid covers at Locations 6 and 7 are replaced with perforated covers.

Two variations of blowers are available: 115VAC 50/60 Hz (36-025F01) and 220VAC 50 Hz (36-025F02).

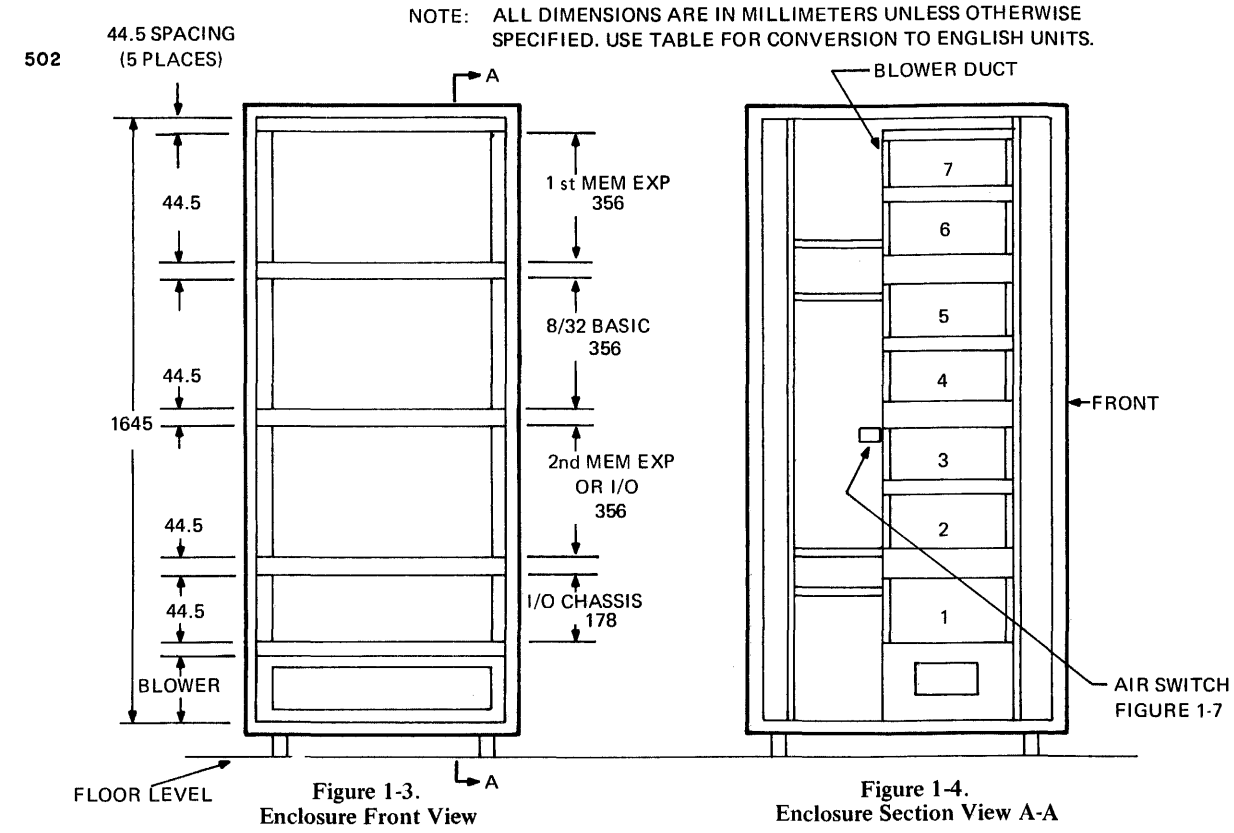


Figure 1-3.
Enclosure Front View

Figure 1-4.
Enclosure Section View A-A

CONVERSION TABLE

MM	INCH
44.5	1 3/4
178.	7
356.	14
1645.	64 3/4

Figure 1-5.
Blank Cover (Solid)

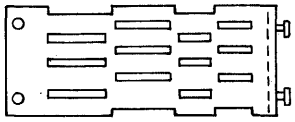


Figure 1-6.
Duct Outlet Cover
(Perforated)

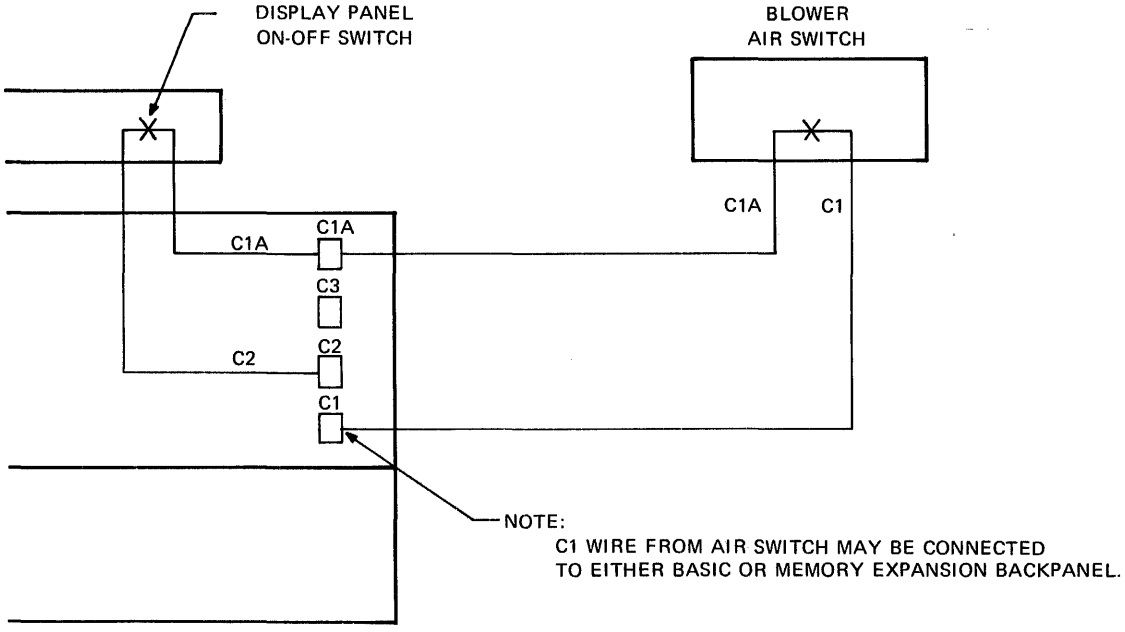


Figure 1-7. Wiring of the Blower Air Switch

1.4 POWER SUPPLY INSTALLATION

1.4.1 Introduction

This section describes the installation of the Model 8/32C or Model 8/32D Power Supply. Mounting information and cabling instructions are provided for the Power Supply in various configurations. Power Supply types 34-023 and 34-033 are currently available. Older supplies are referenced where appropriate.

1.4.2 Mounting

The power supplies mount directly behind the Processor and Expansion chassis (see Figure 1-8). They are attached to the right mounting upright (viewed from the rear). There is adequate slack in the power supply cable to allow the power supply to swing out. To prevent the cable from being pinched between the power supply and chassis support rails, a service loop is required. Power Supply 34-023 mounting varies slightly. Refer to Publication Number 29-452 for details.

WARNING

BEFORE SWINGING OUT THE POWER SUPPLIES, THE RACK LEVELING FEET SHOULD BE LOWERED. UP TO FIVE POWER SUPPLIES CAN BE SWUNG OUT AT ONE TIME AFTER THE LEVELERS ARE IN CONTACT WITH THE FLOOR SURFACE.

The power supplies may be swung in or out on their mounting pivots for easy access to the back plane. When they are in operating position, they are secured by two 10-32 screws (ASA B1.1-1960) which attach to the left mounting upright (viewed from the rear).

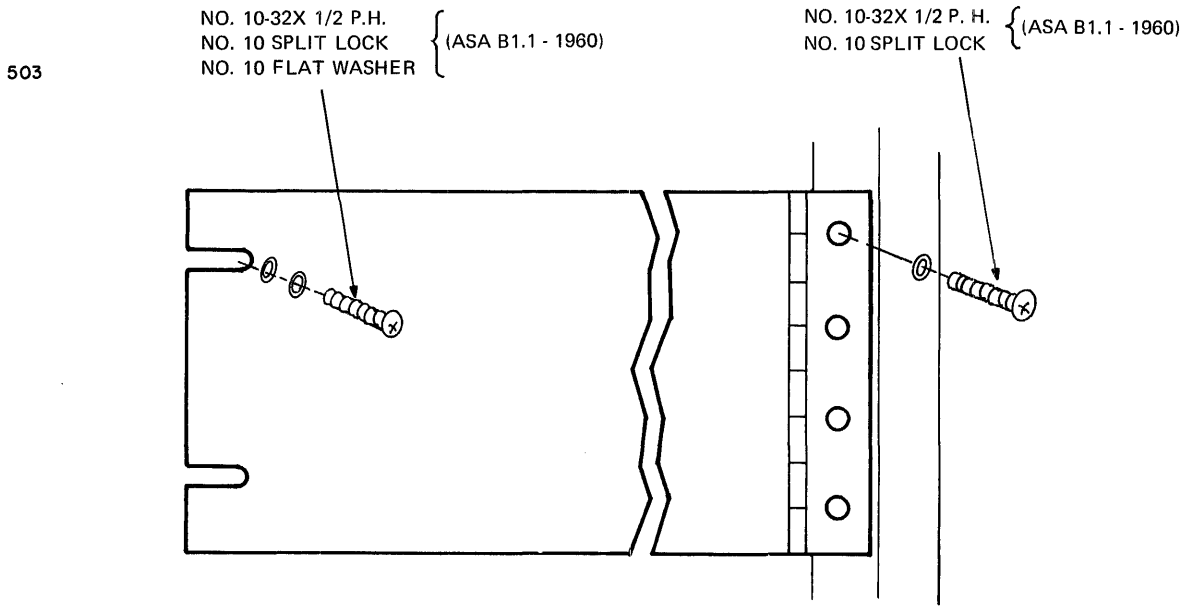


Figure 1-8. 34-033 Power Supply Mounting

1.4.3 Power Supply/Chassis Cabling

1.4.3.1 System Voltages.

The Model 8/32C or Model 8/32D Systems requires three system voltages:

Mnemonic	Voltage
P5	+5V
P15	+16.5V
N15	-16.5V

Any other voltages locally generated are not considered system voltages.

1.4.3.2 System Power Supply

This 34-023 or 34-033 INTERDATA Power Supply is used for all power requirements in the Model 8/32C or 8/32D Systems. All three outputs (P5, N15, and P15) are short circuit protected, and regulated to +1% when normally loaded. P15 and N15 are overvoltage protected. On the 34-033 supply the P5 output is also overvoltage protected.

Refer to the appropriate *Switching Regulated Power Supply Manual* for installation and operating details.

POWER SUPPLY	MANUAL NUMBER
34-026 34-027 34-029	29-437
34-023	29-452
34-033	29-595

NOTE: ALL OF THE ABOVE POWER SUPPLIES ARE FUNCTIONALLY EQUAL.

1.4.3.3 Power Control

The power control circuit diagram for the Model 8/32C is shown in Figure 1-9. Leads C1A and C2 are the remote ON/OFF switch leads in series with the Blower Air Switch. This switch shuts the system down if the blower fails.

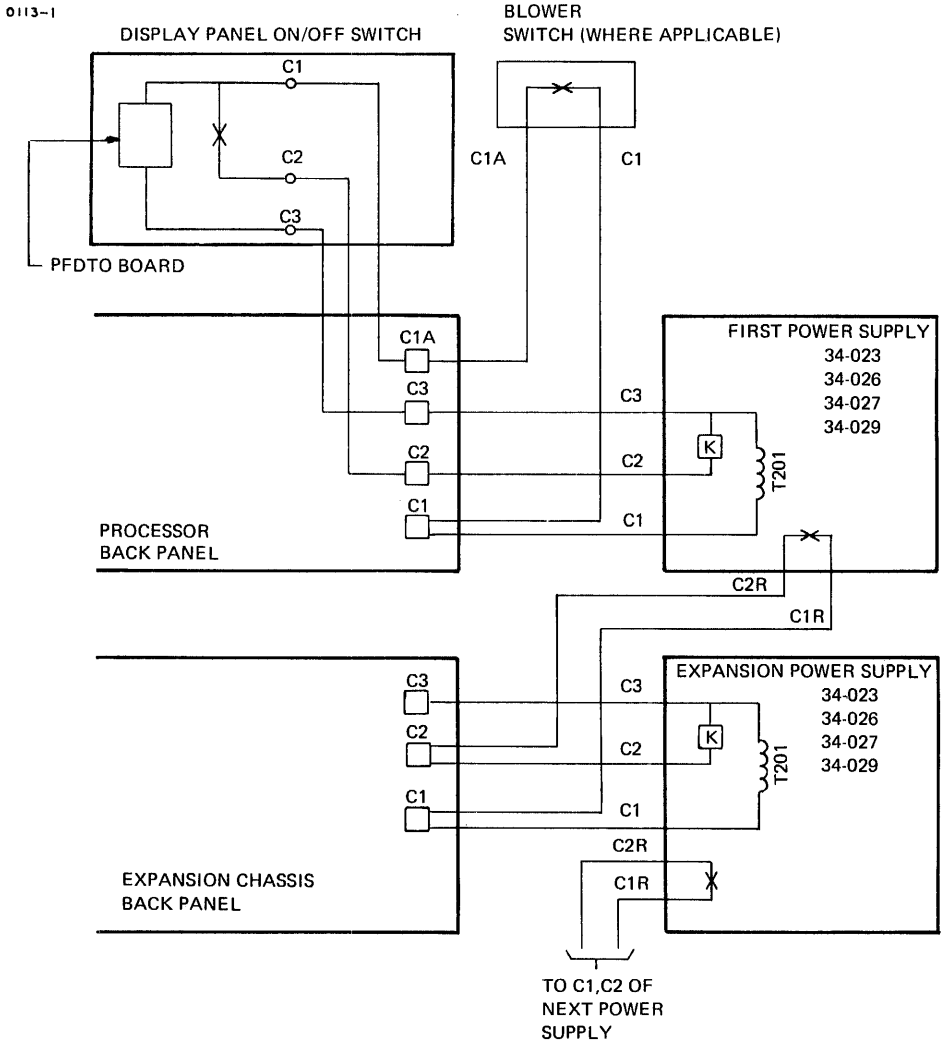


Figure 1-9. Set Up for Additional Power Supplies (34-023, 34-026, 34-027, 34-029)

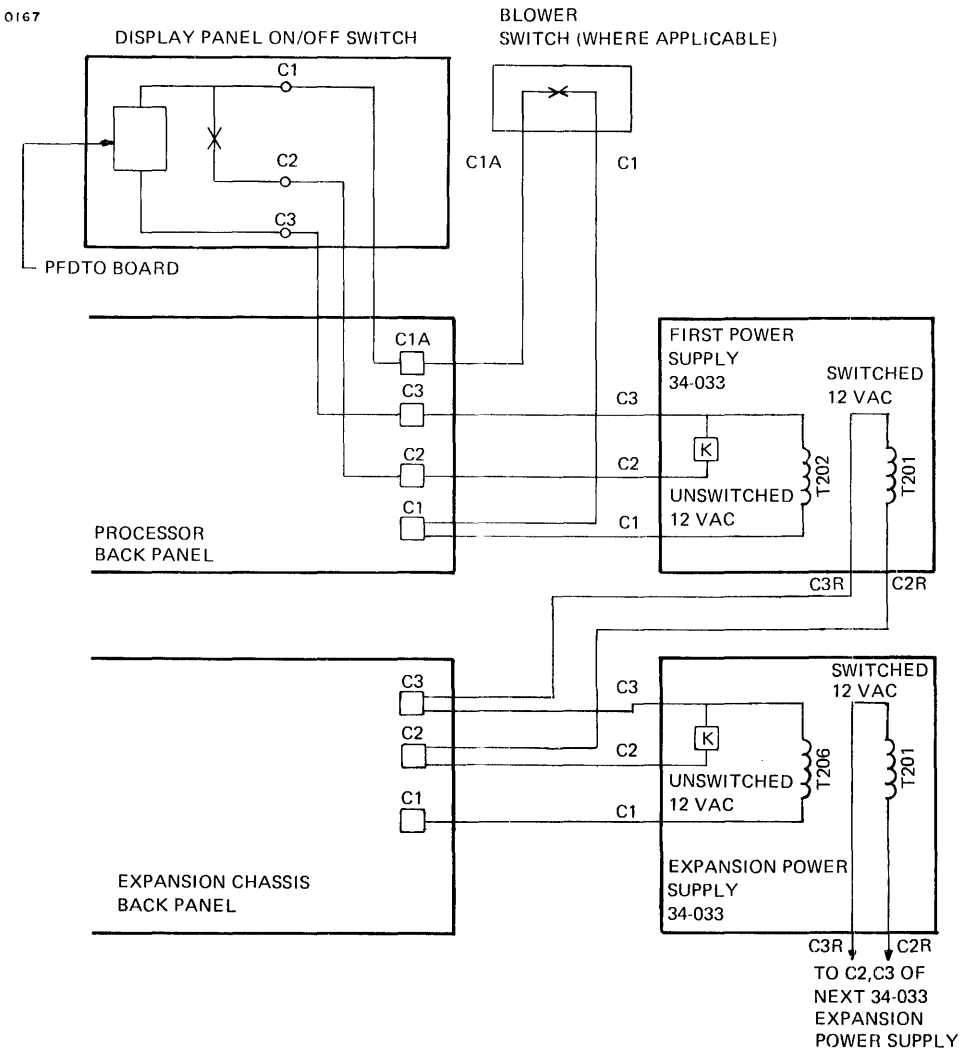


Figure 1-9A. Set Up for Additional Power Supplies (34-033)

1.4.3.4 Primary Power Requirements

The Power Supply is limited to operating at 115VAC or 230VAC + 10%, 47 to 63 Hz.

The maximum power requirements for each Power Supply are:

INPUT LINE	34-033	34-023
115 VAC 230 VAC	6.50 Amperes 3.25 Amperes	7.5 Amperes 3.75 Amperes

1.4.3.5 Conversion Procedure from 115 to 230 VAC Operation

Refer to the appropriate Power Supply manual for conversion procedure.

1.4.3.6 Adjustments

All power system adjustments are made at the factory and should not require readjustment in the field. If readjustment becomes necessary, the recommended settings are:

Mnemonic	Voltage Setting
P5	+ 5.1 Volts
P15	+16.5 Volts
N15	-16.5 Volts

Voltages should always be measured at the backpanel during adjustments. These adjustments are made after disconnecting the tracking thermistors and placing a 1 K ohm ±5% resistor across the thermistor terminals.

1.4.3.7 Configuration

In a Model 8/32C or 8/32D System, the minimum system configuration consists of one twin chassis and two standard INTERDATA Power Supplies. Figure 1-10 shows the power distribution of the basic system.

1.4.3.8 Installation

The installations for the various power systems are:

1. Connect the cables to the twin chassis; referring to Figures 1-10 through 1-16 depending upon the configuration.

   Note that the memory expansion backpanel contains two sets of +15 and -15 VDC power busses, and in some configurations it is necessary to connect the busses with jumper cables.

2. Cables from the front of the chassis may be routed through the 44.5 mm (1¾") space between chassis (see Figure 1-3). If there are any unused connectors, secure them to prevent shorting.

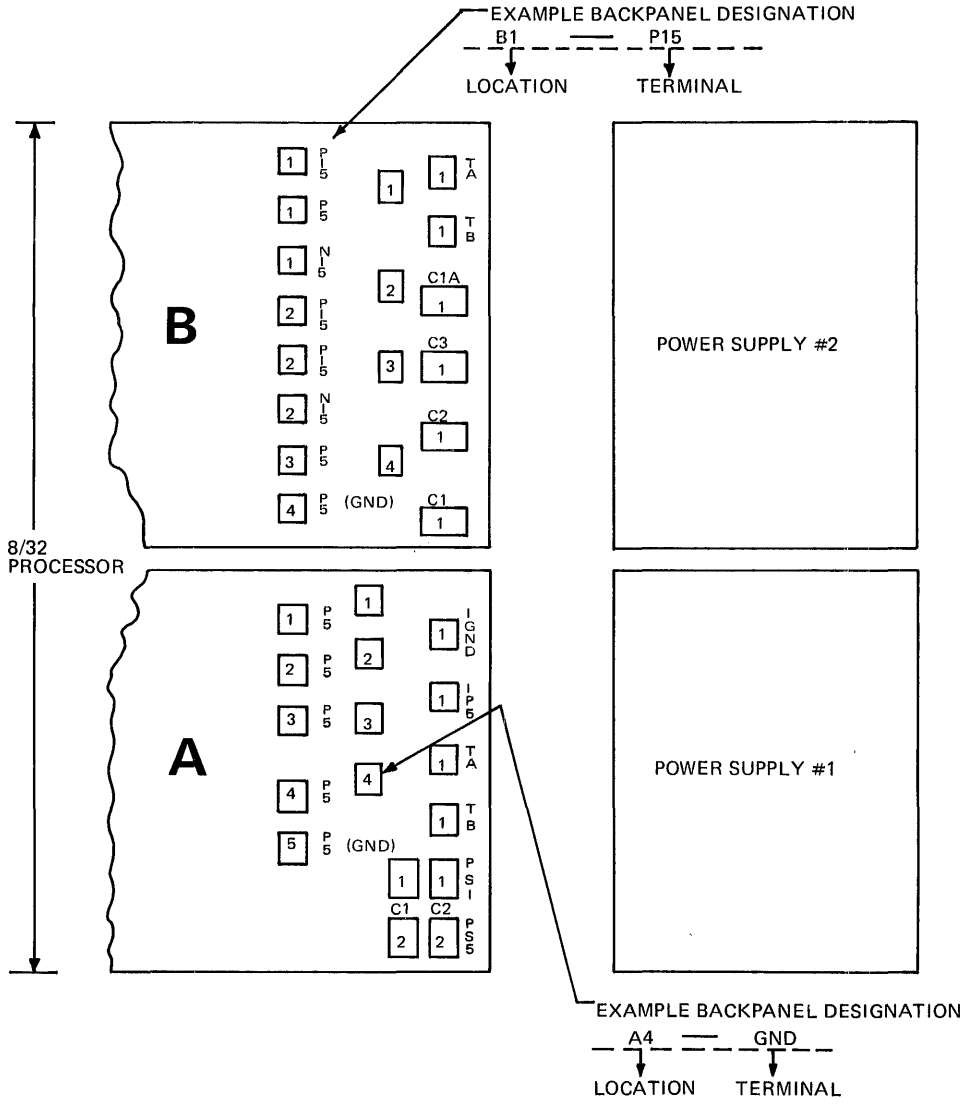


Figure 1-10. Wiring Diagram: 8/32C 128KB Memory, 8/32D 256KB Memory, No WCS, No DFU

	POWER SUPPLY LEADS	CHASSIS BACK PANEL DESIGNATION				
		PWR SUPPLY #1	PWR SUPPLY #2	PWR SUPPLY #3	PWR SUPPLY #4	PWR SUPPLY #5
CABLE BRANCH	N15	B2-N15	B1-N15			
	N15	B2-N15	B1-N15			
	P15	B2-P15	B1-P15			
	P15	B2-P15	B1-P15			
	TA	A1-TA	B1-TA			
	TB	A1-TB	B1-TB			
	GND	B4-GND	BI-GND			
CABLE BRANCH	P5	B3-P5	A4-P5			
	P5	B4-P5	A5-P5			
	GND	B3-GND	A3-GND			
	GND	B4-GND	A4-GND			
CABLE BRANCH	C3	T.B. (NOTE 3)	B1C3			
	C2	A1-C2	B1C2			
	C1	A1-C1	B1C1			
	P5	A1-P5	BI-P5			
	P5	A3-P5	B2-P5			
	GND	A1-GND	B1-GND			
	GND	A2-GND	B2-GND			
	L GND	A1-L GND	T.B. (NOTE 3)			
	+L	A1- +L	T.B. (NOTE 3)			
	C1R	T.B. (NOTE 3)	A1 C1			
	C2R	T.B.	A1-C2			
	FAN AC	T.B.	T.B. (NOTE 3)			

NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL POWER JUMPERS (P5, N15, P15) SHOULD BE REMOVED FROM THE BACKPANELS BEFORE POWER SUPPLY INSTALLATION.
2. ———
3. T.B. – TIE BACK WIRE.

Figure 1-10. Wiring Diagram: 8/32C 128KB Memory, 8/32D 256KB Memory, No WCS, No DFU (Continued)

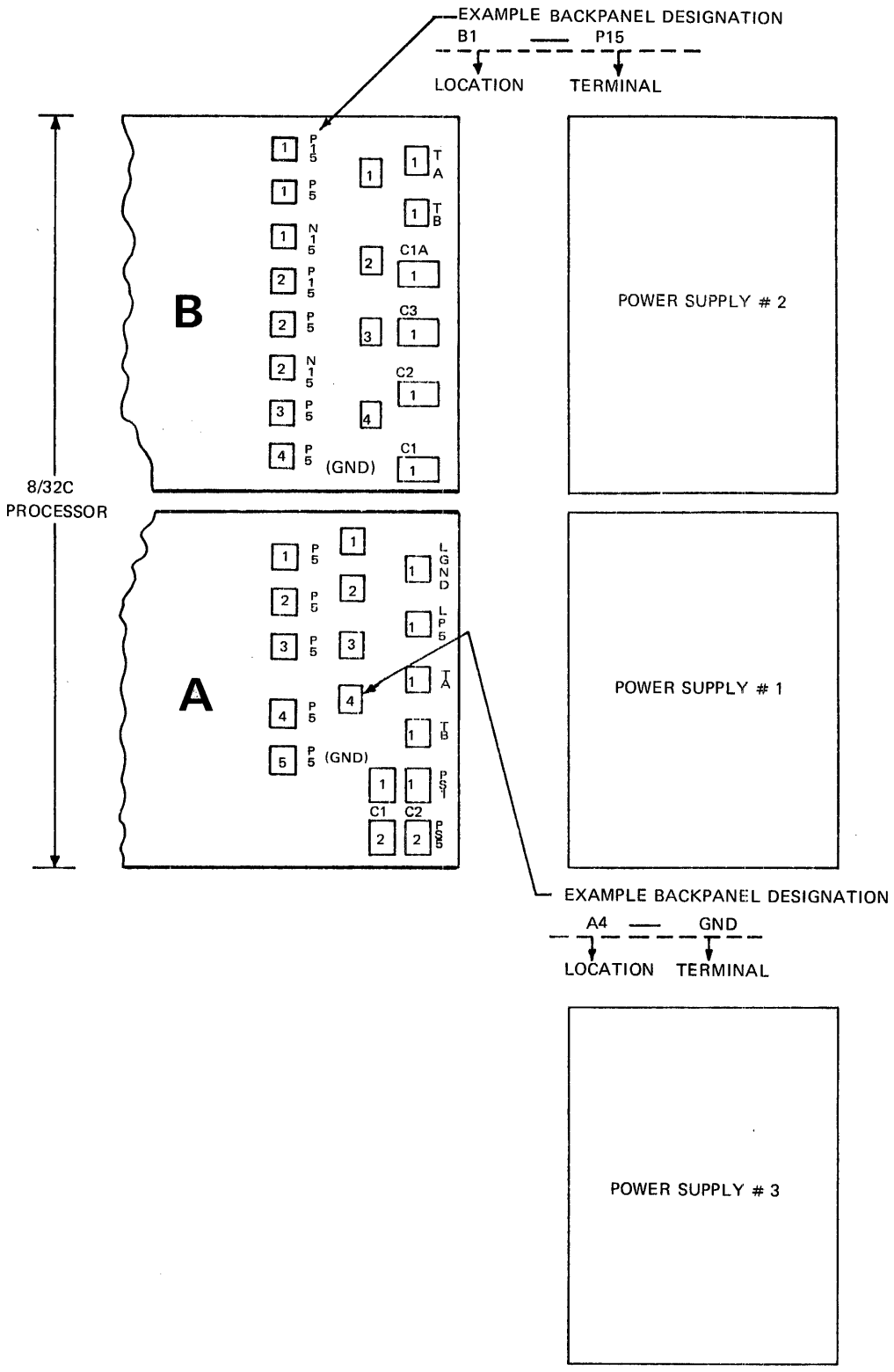


Figure 1-11. Wiring Diagram: 8/32C 128KB Memory, 8/32D 256KB Memory With WCS And/Or DFU

	POWER SUPPLY LEADS	CHASSIS BACK PANEL DESIGNATION				
		PWR SUPPLY #1	PWR SUPPLY #2	PWR SUPPLY #3	PWR SUPPLY #4	PWR SUPPLY #5
	N15	B2-N15	B1-N15	T.B. (NOTES 2&3		
	N15	B2-N15	B1-N15	↓		
CABLE BRANCH	P15	B2-P15	B1-P15	↓		
	P15	B2-P15	B1-P15	↓		
	TA	A1-TA	B1-TA	↓		
	TB	A1-TB	B1-TB	↓		
	GND	B4-GND	B1-GND	T.B. (NOTES 2&3)		
CABLE BRANCH	P5	A1-P5	B1-P5	B3-P5		
	P5	A1-P5	B1-P5	B4-P5		
	GND	A1-GND	B1-GND	B3-GND		
	GND	A2-GND	B2-GND	B4-GND		
	C3	T. B. (NOTE 3)	B1-C3	T.B. (NOTE 3)		
	C2	A1-C2	B1-C2	A2-C2		
	C1	A1-C1	B1-C1	A2-C1		
	P5	A2-P5	B2-P5	A4-P5		
	P5	A3-P5	B2-P5	A5-P5		
CABLE BRANCH	GND	A2-GND	B2-GND	A3-GND		
	GND	A3-GND	B3-GND	A4-GND		
	L GND	A1-L GND	T.B. (NOTE 3)	T.B. (NOTE 3)		
	+L	A1- +L	T.B. (NOTE 3)	↓		
	C1R	A2-C1	A1-C1	↓		
	C2R	A2-C2	A1-C2	↓		
	FAN AC	T.B. (NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)		

NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL POWER JUMPERS (P5, N15, P15) SHOULD BE REMOVED FROM THE BACKPANELS BEFORE POWER SUPPLY INSTALLATION.
2. ADJUST VOLTAGE OF P15 & N15 TO BELOW 17.0 VOLTS.
3. T.B. – TIE BACK WIRE.

Figure 1-11. Wiring Diagram: 8/32C 128KB Memory, 8/32D 256KB Memory, With WCS And/Or DFU (Continued)

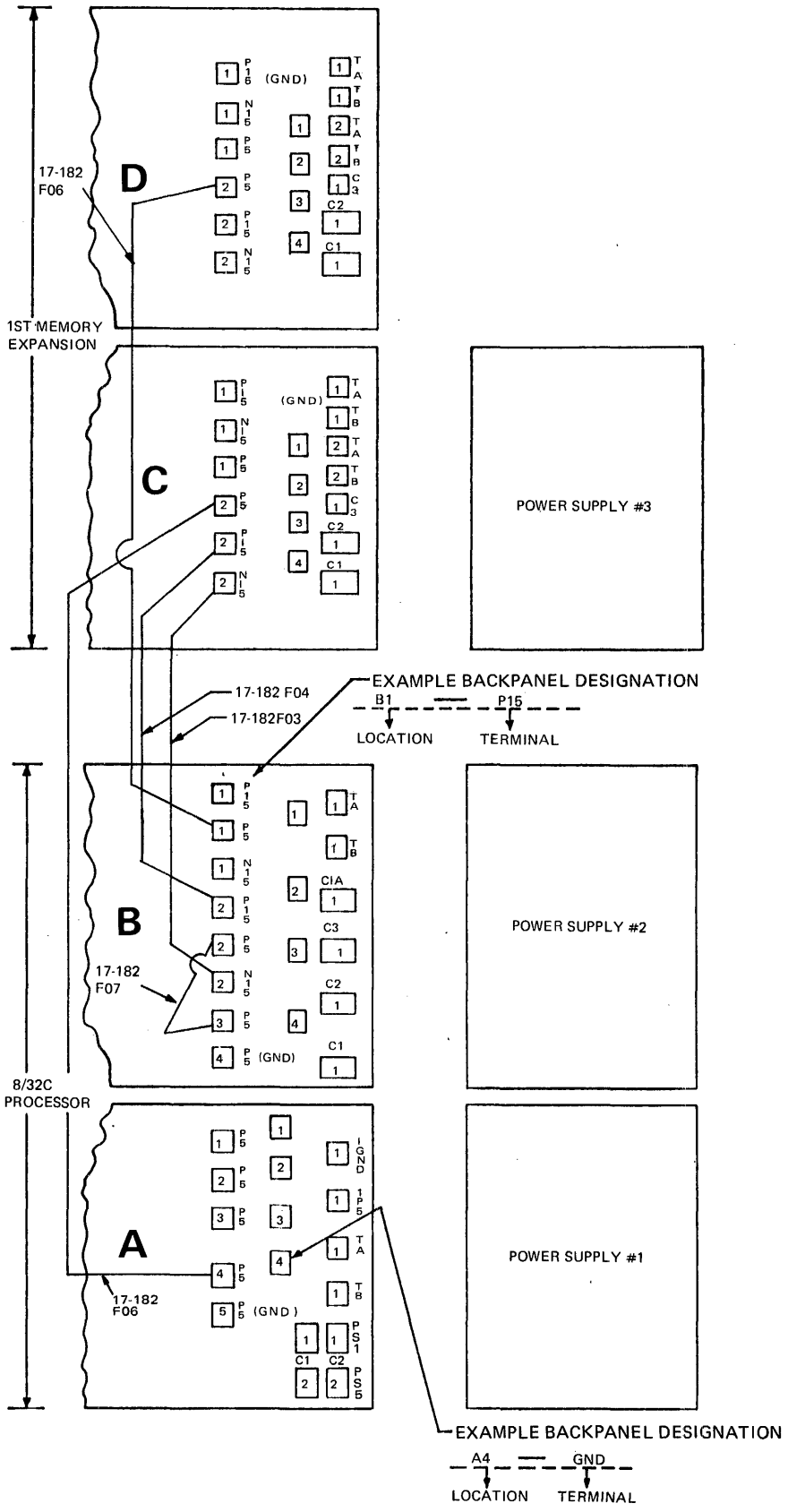


Figure 1-12. Wiring Diagram: 8/32C 256KB Memory, 8/32D 512KB Memory, With Or Without WCS And/Or DFU

	POWER SUPPLY LEADS	CHASSIS BACK PANEL DESIGNATION				
		PWR SUPPLY #1	PWR SUPPLY #2	PWR SUPPLY #3	PWR SUPPLY #4	PWR SUPPLY #5
CABLE BRANCH	N15	C1-N15	D1-N15	T.B. (NOTES 2&3)		
	N15	C2-N15	D2-N15			
	P15	C1-P15	D1-P15			
	P15	C2-P15	D2-P15			
	TA	C1-TA	D1-TA	(NOTE 3)		
	TB	C1-TB	D1-TB	(NOTE 3)		
	GND	C1-GND	D1-GND	T.B. (NOTE 3)		
CABLE BRANCH	P5	C1-P5	A2-P5	B2-P5		
	P5	C2-P5	A3-P5	B3-P5		
	GND	C2-GND	A3-GND	B3-GND		
	GND	C4-GND	A2-GND	B4-GND		
CABLE BRANCH	C3	T.B. (NOTE 3)	B1-C3	D1-C3		
	C2	A1-C2	B1-C2	D1-C2		
	C1	A1-C1	B1-C1	D1-C1		
	P5	A4-P5	A1-P5	D1-P5		
	P5	A5-P5	A2-P5	D2-P5		
	GND	A3-GND	A1-GND	D1-GND		
	GND	A4-GND	A2-GND	D3-GND		
	L GND	A1-L GND	T.B. (NOTE 3)	T.B.(NOTE 3)		
	+L	A1-+L	T.B. (NOTE 3)	T.B. (NOTE 3)		
	C1R	A2-C1	D1-C1	A1-C1		
	C2R	A2-C2	D1-C2	A1-C2		
	FAN AC	T.B. (NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)		

NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL POWER JUMPERS (P5, N15, P15) SHOULD BE REMOVED FROM THE BACKPANELS BEFORE POWER SUPPLY INSTALLATION.
2. ADJUST VOLTAGE OF P15 & N15 TO BELOW 17.0 VOLTS.
3. T.B. – TIE BACK WIRE.

Figure 1-12. Wiring Diagram: 8/32C 256KB Memory, 8/32D 512KB Memory With Or Without WCS And/Or DFU (Continued)

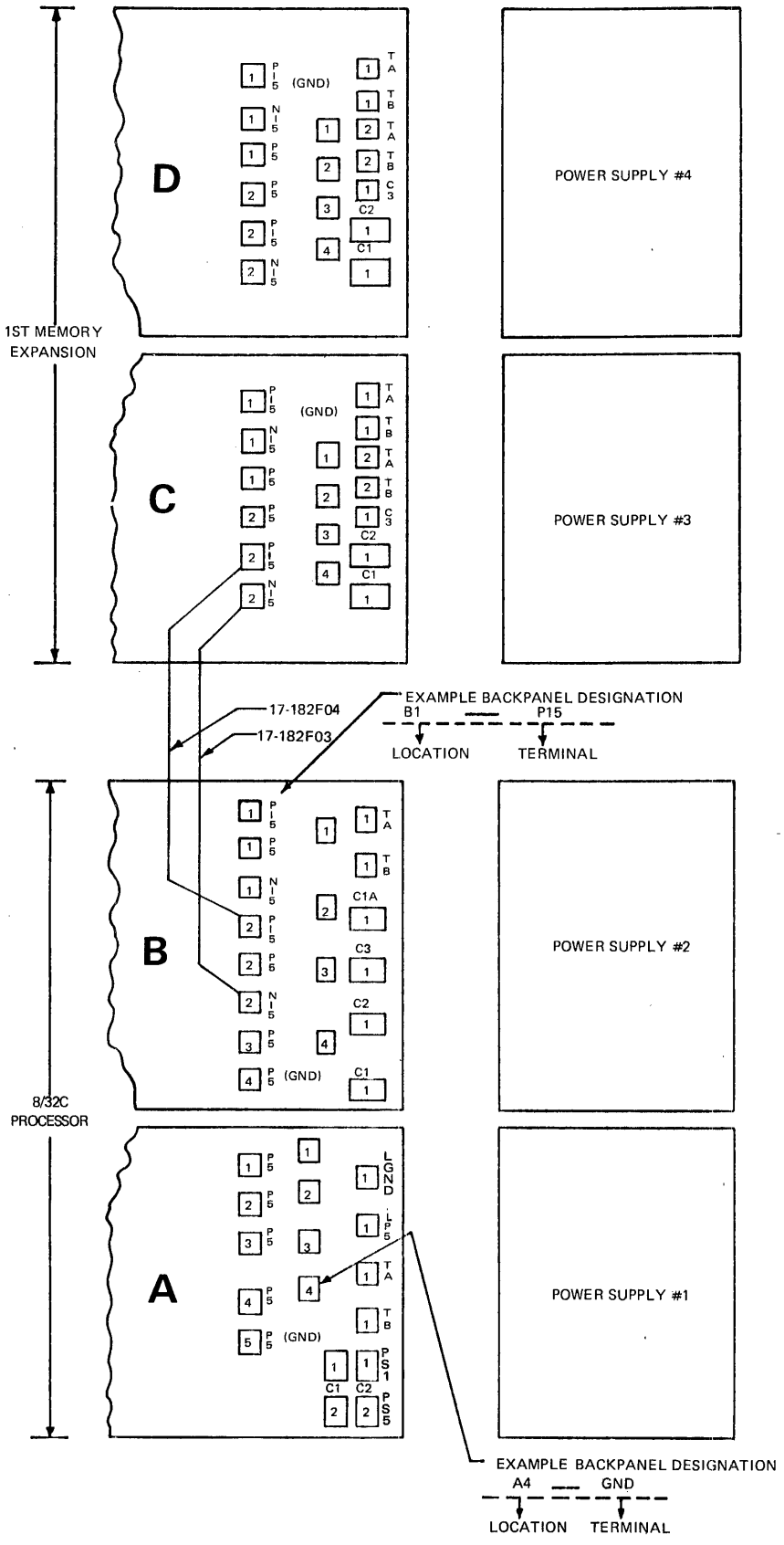


Figure 1-13. Wiring Diagram: 8/32C 384 Or 512KB Memory, 8/32D 768 Or 1024KB Memory With Or Without WCS And/Or DFU

	POWER SUPPLY LEADS	CHASSIS BACK PANEL DESIGNATION				
		PWR SUPPLY #1	PWR SUPPLY #2	PWR SUPPLY #3	PWR SUPPLY #4	PWR SUPPLY #5
CABLE BRANCH	N15	C2-N15	C1-N15	D2-N15	D1-N15	
	N15	C2-N15	C1-N15	D2-N15	D1-N15	
	P15	C2-P15	C1-P15	D2-P15	D1-P15	
	P15	C2-P15	C1-P15	D2-P15	D1-P15	
	TA	C2-TA	C1-TA	D2-TA	D1-TA	
	TB	C2-TB	C1-TB	D2-TB	D1-TB	
	GND	C4-GND	C1-GND	D4-GND	D1-GND	
CABLE BRANCH	P5	A1-P5	A4-P5	C1-P5	D1-P5	
	P5	B2-P5	A5-P5	C1-P5	D1-P5	
	GND	B1-GND	A3-GND	C1-GND	D1-GND	
	GND	B2-GND	A4-GND	C2-GND	D2-GND	
CABLE BRANCH	C3	T.B. (NOTE 3)	B1-C3	C1-C3	D1-C3	
	C2	A1-C2	B1-C2	C1-C2	D1-C2	
	C1	A1-C1	B1-C1	C1-C1	D1-C1	
	P5	A2-P5	B3-P5	C2-P5	D2-P5	
	P5	A3-P5	B4-P5	C2-P5	D2-P5	
	GND	A1-GND	B3-GND	C2-GND	D2-GND	
	GND	A3-GND	B4-GND	C3-GND	D3-GND	
	L GND	A1-L GND	T.B. (NOTE 3)	T.B.(NOTE 3)	T.B. (NOTE 3)	
	+L	A1-+L	T.B. (NOTE 3)	T.B.(NOTE 3)	T.B. (NOTE 3)	
	C1R	A2-C1	D1-C1	A1-C1	C1-C1	
	C2R	A2-C2	D1-C2	A1-C2	C1-C2	
	FAN AC	T.B.(NOTE 3)	T.B. (NOTE 3)	T.B(NOTE 3)	T.B. (NOTE 3)	

NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL POWER JUMPERS (P5, N15, P15) SHOULD BE REMOVED FROM THE BACKPANELS BEFORE POWER SUPPLY INSTALLATION.
2. ———
3. T.B.– TIE BACK WIRE.

Figure 1-13. Wiring Diagram: 8/32C 384 Or 512KB Memory, 8/32D 768 Or 1024KB Memory With Or Without WCS And/Or DFU (Continued)

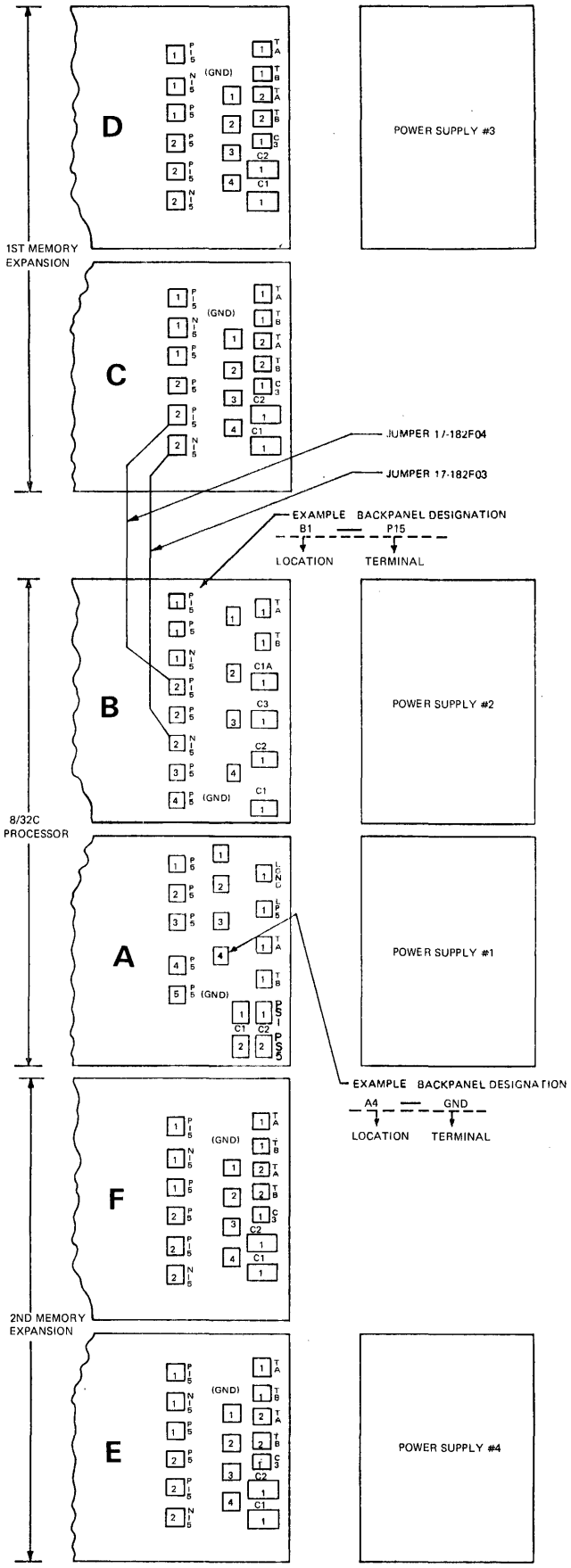


Figure 1-14. Wiring Diagram: 8/32C 640KB, 768KB Or 896KB Memory With Or Without WCS And/Or DFU

	POWER SUPPLY LEADS	CHASSIS BACK PANEL DESIGNATION				
		PWR SUPPLY #1	PWR SUPPLY #2	PWR SUPPLY #3	PWR SUPPLY #4	PWR SUPPLY #5
CABLE BRANCH	N15	F1-N15	C1-N15	D1-N15	E1-N15	
	N15	F2-N15	C2-N15	D2-N15	E2-N15	
	P15	F1-P15	C1-P15	D1-P15	E1-P15	
	P15	F2-P15	C2-P15	D2-P15	E2-P15	
	TA	F1-TA	C1-TA	D1-TA	E1-TA	
	TB	F1-TB	C1-TB	D1-TB	E1-TB	
	GND	F1-GND	C1-GND	D1-GND	E1-GND	
CABLE BRANCH	P5	B3-P5	A1-P5	C1-P5	F1-P5	
	P5	B4-P5	A2-P5	C2-P5	F2-P5	
	GND	B3-GND	A1-GND	C2-GND	F2-GND	
	GND	B4-GND	A2-GND	C4-GND	F4-GND	
CABLE BRANCH	C3	T.B. (NOTE 3)	B1-C3	D1-C3	E1-C3	
	C2	A1-C2	B1-C2	D1-C2	E1-C2	
	C1	A1-C1	B1-C1	D1-C1	E1-C1	
	P5	A4-P5	A1-P5	D1-P5	E1-P5	
	P5	A5-P5	B2-P5	D2-P5	E2-P5	
	GND	A3-GND	B1-GND	D2-GND	E2-GND	
	GND	A4-GND	B2-GND	D4-GND	E4-GND	
	L GND	A1-L GND	T.B. (NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)	
	+L	A1-+L	T.B. (NOTE 3)	T.B. (NOTE 3)		
	C1R	E1-C1	D1-C1	A1-C1		
	C2R	E1-C2	D2-C2	A1-C2		
	FAN AC	T.B. (NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)	

NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL POWER JUMPERS (P5, N15, P15) SHOULD BE REMOVED FROM THE BACKPANELS BEFORE POWER SUPPLY INSTALLATION.
2. ————
3. T.B. – TIE BACK WIRE

Figure 1-14. Wiring Diagram: 8/32C 640KB, 768KB Or 896KB Memory With Or Without WCS And/Or DFU (Continued)

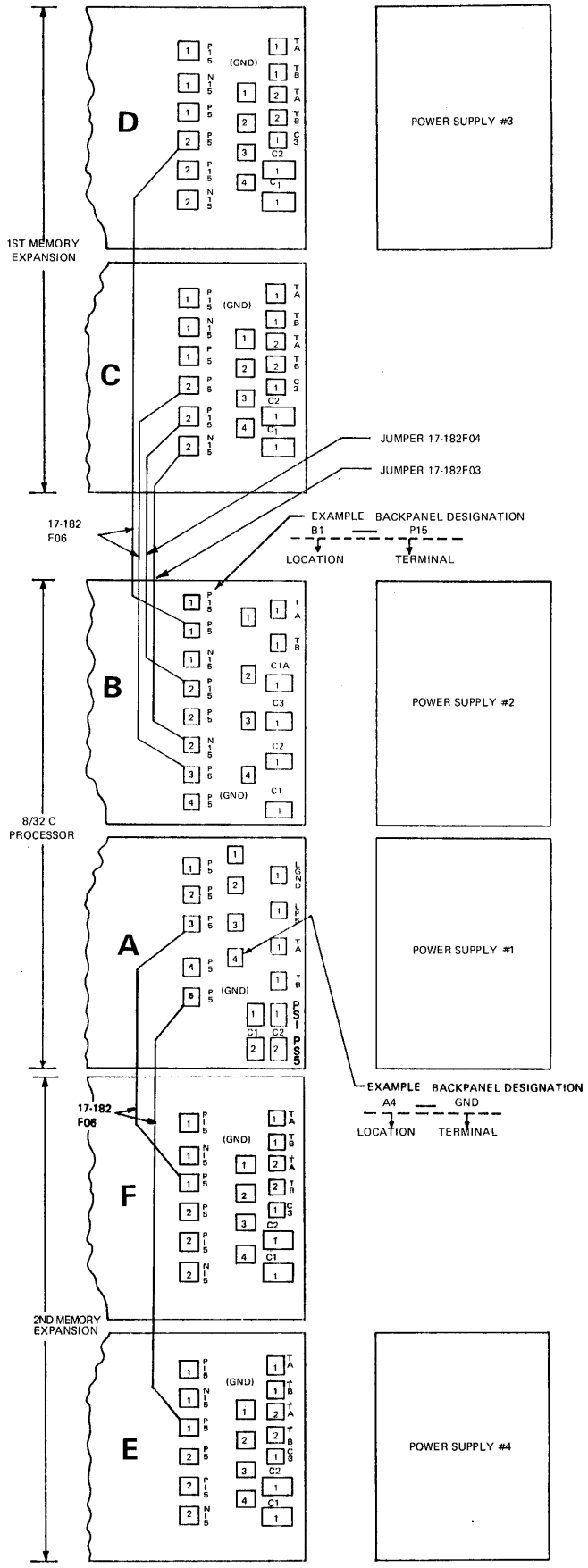


Figure 1-15. Wiring Diagram: 8/32C 1MB Memory Without WCS Or DFU

	POWER SUPPLY LEADS	CHASSIS BACK PANEL DESIGNATION				
		PWR SUPPLY #1	PWR SUPPLY #2	PWR SUPPLY #3	PWR SUPPLY #4	PWR SUPPLY #5
CABLE BRANCH	N15	F1-N15	C1-N15	D1-N15	E1-N15	
	N15	F2-N15	C2-N15	D2-N15	E2-N15	
	P15	F1-P15	C1-P15	D1-P15	E1-P15	
	P15	F2-P15	C2-P15	D2-P15	E2-P15	
	TA	F1-TA	C1-TA	D1-TA	E1-TA	
	TB	F1-TB	C1-TB	D1-TB	E1-TB	
	GND	F1-GND	C1-GND	D1-GND	E1-GND	
CABLE BRANCH	P5	F1-P5	C1-P5	B1-P5	A4-P5	
	P5	F2-P5	C2-P5	B2-P5	A5-P5	
	GND	F2-GND	C2-GND	B1-GND	A3-GND	
	GND	F4-GND	C4-GND	B2-GND	A4-GND	
CABLE BRANCH	C3	T.B.	B1-C3	D1-C3	E1-C3	
	C2	A1-C2	B1-C2	D1-C2	E1-C2	
	C1	A1-C1	B1-C1	D1-C1	E1-C1	
	P5	A1-P5	B3-P5	D1-P5	E1-P5	
	P5	A3-P5	B4-P5	D2-P5	E2-P5	
	GND	A1-GND	B3-GND	D2-GND	E2-GND	
	GND	A2-GND	B4-GND	D4-GND	E4-GND	
	L GND	A1-L GND	T.B. (NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)	
	+L	A1-+L	T.B. (NOTE 3)	T.B. (NOTE 3)		
	C1R	E1-C1	D1-C1	A1-C1		
	C2R	E1-C2	D1-C2	A1-C2		
	FAN AC	T.B. (NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)	

NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL POWER JUMPERS (P5, N15, P15 SHOULD BE REMOVED FROM THE BACKPANELS BEFORE POWER SUPPLY INSTALLATION.
2. ————
3. T.B.–TIE BACK WIRE.

Figure 1-15. Wiring Diagram: 8/32C 1MB Memory Without WCS Or DFU (Continued)

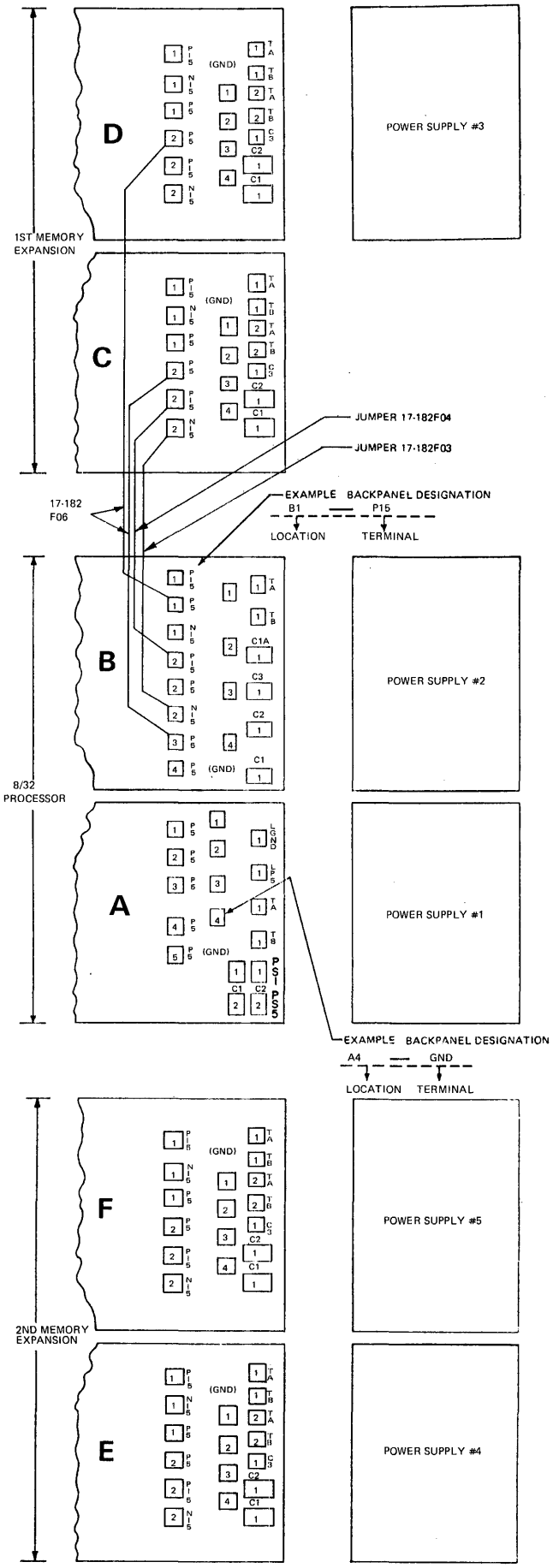


Figure 1-16. Wiring Diagram: 8/32C 1MB Memory With WCS Or DFU

	POWER SUPPLY LEADS	CHASSIS BACK PANEL DESIGNATION				
		PWR SUPPLY #1	PWR SUPPLY #2	PWR SUPPLY #3	PWR SUPPLY #4	PWR SUPPLY #5
CABLE BRANCH	N15	T.B. (NOTES 2&3)	C1-N15	D1-N15	E1-N15	F1-N15
	N15	↓	C2-N15	D2-N15	E2-N15	F2-N15
	P15	↓	C1-P15	D1-P15	E1-P15	F1-P15
	P15	(NOTES 2&3)	C2-P15	D2-P15	E2-P15	F2-P15
	TA	(NOTE 3)	C1-TA	D1-TA	E1-TA	F1-TA
	TB	↓ (NOTE 3)	C1-TB	D1-TB	E1-TB	F1-TB
	GND	T.B. (NOTE 3)	C1-GND	D1-GND	E1-GND	F1-GND
CABLE BRANCH	P5	A1-P5	C1-P5	B1-P5	E1-P5	A4-P5
	P5	A2-P5	C2-P5	B2-P5	E1-P5	A5-P5
	GND	A1-GND	C2-GND	B1-GND	E1-GND	A3-GND
	GND	A2-GND	C4-GND	B2-GND	E2-GND	A4-GND
CABLE BRANCH	C3	T.B. (NOTE 3)	B1-C3	D1-C3	E1-C3	F1-C3
	C2	A1-C2	B1-C2	D1-C2	E1-C2	F1-C2
	C1	A1-C1	B1-C1	D1-C1	E1-C1	F1-C1
	P5	A2-P5	B3-P5	D1-P5	E2-P5	F1-P5
	P5	A3-P5	B4-P5	D2-P5	E2-P5	F2-P5
	GND	A2-GND	B3-GND	D2-GND	E3-GND	F2-GND
	GND	A3-GND	B4-GND	D4-GND	E4-GND	F4-GND
	L GND	A1-L GND	T.B.(NOTE 3)	T.B.(NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)
	+L	A1-+L	T.B. (NOTE 3)	T.B.(NOTE 3)	↓	T.B. (NOTE 3)
	C1R	F1-C1	D1-C1	A1-C1	↓	E1-C1
	C2R	F1-C2	D1-C2	A1-C2	↓	E1-C2
	FAN AC	T.B. (NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)	T.B. (NOTE 3)

NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL POWER JUMPERS (P5, N15, P15) SHOULD BE REMOVED FROM THE BACKPANELS BEFORE POWER SUPPLY INSTALLATION.
2. ADJUST VOLTAGE OF P15 & N15 TO BELOW 17.0 VOLTS.
3. T.B. – TIE BACK WIRE

Figure 1-16. Wiring Diagram: 8/32C 1MB Memory With WCS Or DFU (Continued)

1.4.3.9 Number of Power Supplies

Tables 1-1 and 1-2 indicate the total number of power supplies needed for the various 8/32C and 8/32D configurations.

TABLE 1-1 8/32C POWER SUPPLIES

8/32C (M83-025) WITH DIFFERENT MEMORY OPTIONS		NUMBER OF M49-050 POWER SUPPLIES NEEDED	
MARKETING NUMBER	MEMORY SIZE	NO WCS OR HPFP OPTION	WITH WCS AND/OR HPFP OPTION
M83-025 w/wo M83-107	128KB	2	3
M83-310 or M83-311	256KB	3	3
M83-312 or M83-313	384KB	4	4
M83-314 or M83-315	512KB	4	4
M83-316 or M83-317	640KB	4	4
M83-318 or M83-319	768KB	4	4
M83-318 or M83-319	896KB	4	4
M83-318 or M83-319	1MB	4	5

TABLE 1-2 8/32D POWER SUPPLIES

8/32D (M83-030) WITH DIFFERENT MEMORY OPTIONS		NUMBER OF M49-050 POWER SUPPLIES NEEDED	
MARKETING NUMBER	MEMORY SIZE	NO WCS OR HPFP OPTION	WITH WCS AND/OR HPFP OPTION
M83-030 w/wo M83-107	256KB	2	3
M83-320 or M83-321	512KB	3	3
M83-324 or M83-325	768KB	4	4
M83-322 or M83-323	1MB	4	4

1.5 PROCESSOR AND EXPANSION CHASSIS INSTALLATION

1.5.1 Installation

For different memory expansions, it is possible to have from one to three twin chassis in the Model 8/32C System (located as shown in Figure 1-3), or from one to two twin chassis in the Model 8/32D System. Figures 1-10 through 1-16 show the three possible configurations.

Prior to mounting the chassis, replace the appropriate solid covers on the plenum with perforated covers (see Section 1.3.2).

The 8/32C or 8/32D System and its memory expansion chassis must always be mounted in a cabinet that is equipped with a blower and plenum. They must be configured as shown in Figure 1-3. These chassis do not have chassis fans. 178 mm (7") and 356 mm (14") chassis with fans are not to be used. When 178 mm (7") I/O chassis without fans are to be mounted in this cabinet, they must be installed in positions where duct covers are located (see Figure 1-3).

CAUTION

IF A CABINET OTHER THAN A 09-069 INTERDATA CABINET IS USED, THE USER MUST SUPPLY HIS OWN FORCED AIR COOLING SYSTEM.

To mount a chassis, slide the chassis into the rack on the chassis support rails from the front of the rack (see Figures 1-1 and 1-2).

CAUTION

NO CHASSIS SHOULD BE MOUNTED IN CANTILEVER FASHION. CHASSIS SUPPORT RAILS MUST BE USED. IF A NON INTERDATA RACK CABINET IS USED, CONSULT THE RACK MANUFACTURER FOR PROPER SUPPORT RAILS.

The chassis support rails are fastened to the mounting uprights at the front and rear of the rack. The Expansion and Processor chassis are screwed in place to the mounting uprights in front of the rack.

1.5.2 Basic Processor Configuration and Cabling

The basic Model 8/32C with 128KB of memory is comprised of:

1. 4 each or 32-206 32KB core modules	Upper Slots 2, 4, 5, and 7
2. 2 each 35-534 LMI	Upper Slots 3 and 6
3. 1 each 35-535 MBC	Upper Slot 1
4. 1 each 35-536 CPA	Upper Slot 0
5. 1 each 35-537 CPB	Lower Slot 7
6. 1 each 35-555 CPC	Lower Slot 6
7. 1 each 35-538 ALU	Lower Slot 3
8. 1 each 35-539 IOU	Lower Slot 0

The basic Model 8/32D with 256KB of memory is comprised of:

1. 4 each 32-209 64KB core modules	Upper Slots 3, 4, 6, and 7
2. 2 each 35-534 LMI	Upper Slots 2 and 5
3. 1 each 35-535 MBC	Upper Slot 1
4. 1 each 35-536 CPA	Upper Slot 0
5. 1 each 35-537 CPB	Lower Slot 7
6. 1 each 35-555 CPC	Lower Slot 6
7. 1 each 35-538 ALU	Lower Slot 3
8. 1 each 35-539 IOU	Lower Slot 0

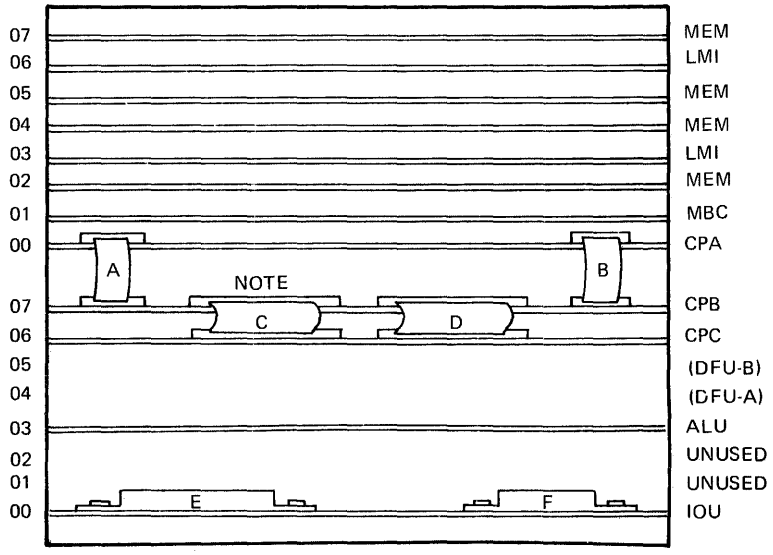
Lower Slots 4 and 5 are reserved for the optional Double/Precision Floating-Point Unit (DFU). Lower Slots 1 and 2 are not used.

CAUTION

BOARDS MUST BE PLUGGED INTO THEIR ASSIGNED LOCATIONS. SEVERE DAMAGE MAY OCCUR IF PLUGGED INTO WRONG SLOTS.

Figure 1-17 is a configuration of the basic 8/32C Processor chassis (see Figure 1-19 for the basic 8/32D Processor chassis) as viewed from the Display Panel side. It correlates applicable cables to the associated Processor connectors and Table 1-3 lists the function of each cable.

Figure 1-18 depicts the basic 8/32C Processor chassis (see Figure 1-20 for the basic 8/32D Processor chassis) as viewed from the back panel. Shown here are the 35-578 Local Memory Bus (LBM) Terminator, the 35-596 Control Address (CA) Terminator, the 17-385 Cable Assembly, and the 35-569 Processor Terminator. Note that P3 of the 17-385 cable assembly is installed on Upper Slot 1, Connector 1 side. P2 of the 17-385 cable assembly is installed on Lower Slot 0 on the Connector 0. P1 is installed on the first slot of the I/O expansion chassis. This chassis is a 12-016F00 if installed in an 8/32C or 8/32D cabinet or 12-012F01 if installed in an Expansion Cabinet.



NOTE
OPTIONAL ON WRITABLE CONTROL STORAGE (WCS)

Figure 1-17. 8/32C basic Processor – Front View

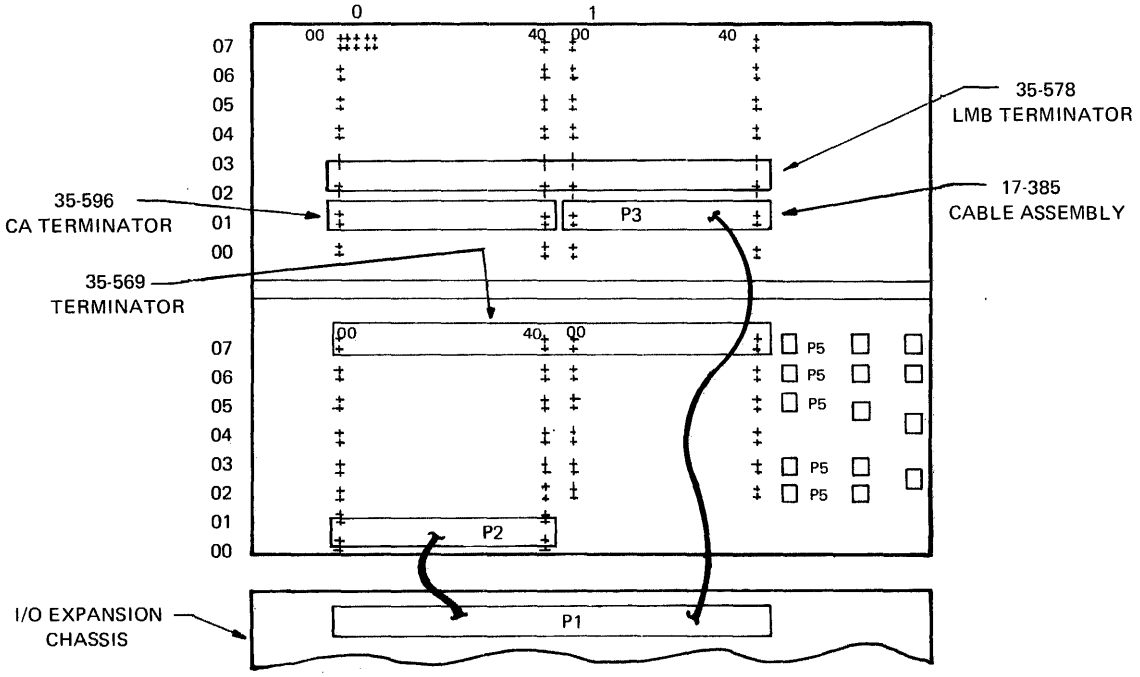
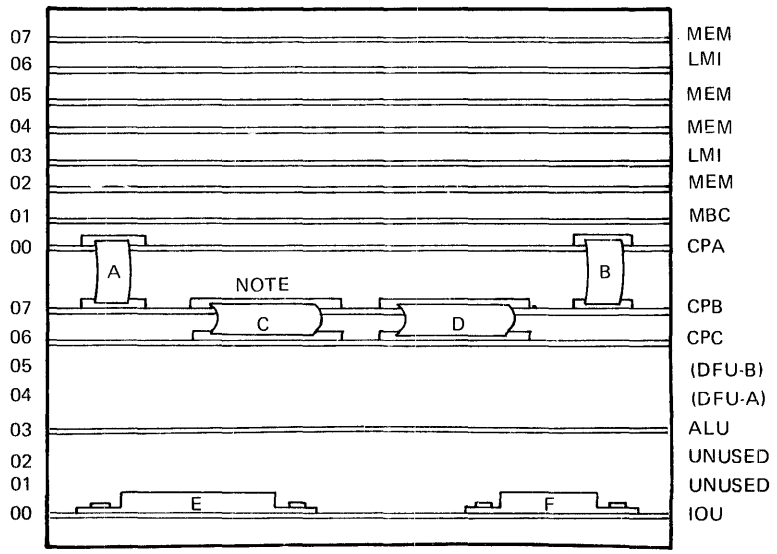


Figure 1-18. 8/32C basic Processor – Rear View

TABLE 1-3. PROCESSOR CABLES – REAR VIEW

LOC.	CONNECTOR #	CABLE	FUNCTION	TYPE
A	CPU5	17-361	USER SOURCE/DEST. REG. ADDR.	RIBBON
B	CPU2	17-361	B.S. REG. ADDR.: MC FIELD	RIBBON
C	CPU4	17-360	CONTROL STORE DATA	RIBBON
D	CPU3	17-360	CONTROL STORE ADDR.; A,B,S	RIBBON
E	IOU3	17-152 ASSY.	DISPLAY	BUNDLED WIRE
F	IOU2	17-180	TTY	BUNDLED WIRE



NOTE
OPTIONAL ON WRITABLE CONTROL STORAGE (WCS)

Figure 1-19 8/32D Basic Processor – Front View

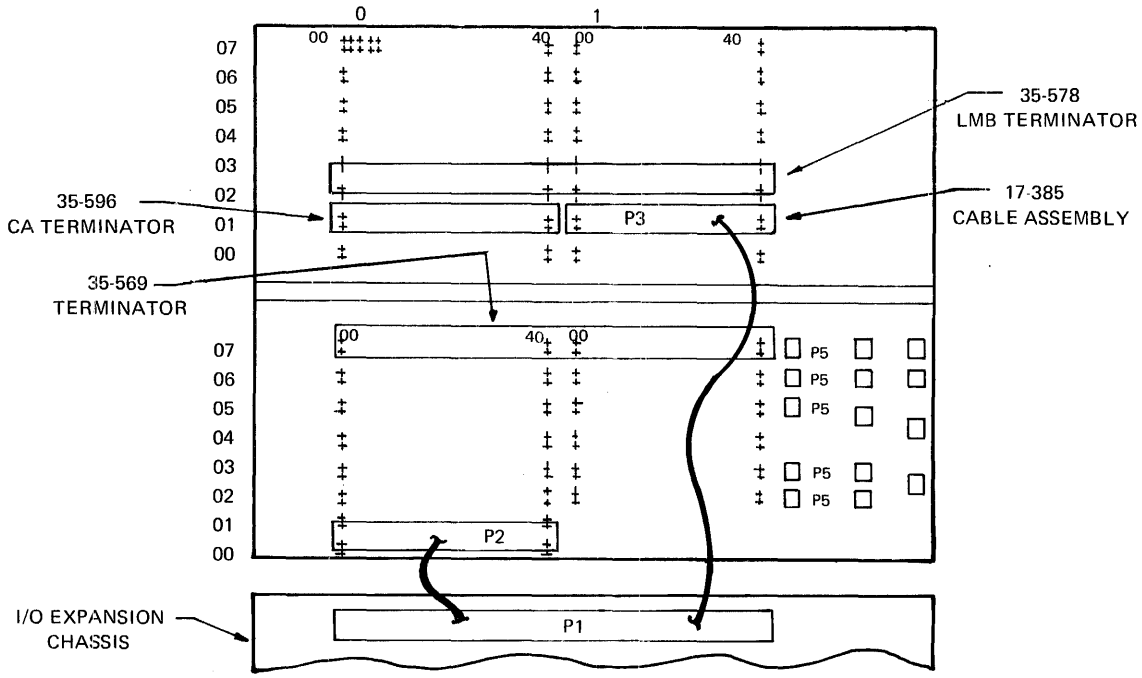


Figure 1-20 8/32D Basic Processor – Rear View

1.5.3 Processor Strap Options

Several Processor boards have strappable options which are described in the following paragraphs. Refer to Section 1.7 for information on memory system strap options.

1.5.3.1 35-536 CPA; Base Register Selection

The Base Register (BR) address is selected via three straps at IC location 05J on the CPA board. The following table indicates the starting locations and their respective strapping instructions. The standard address is X'300'.

STARTING LOCATION	05J11 TO	05J13 TO	05J15 TO
CRUX X'300'	05J06	05J03	05J01
X'500'	05J05	05J04	05J01
X'900'	05J05	05J03	05J02

1.5.3.2 35-537 CPB; Privileged/Illegal Straps

Depending upon system options, one of three straps must be included to properly service the illegal instruction interrupt. The straps are located at IC location 03D and the following table indicates the proper strap for each option. The standard strap is 03D02 to 03D14.

OPTION	03D02 TO
BASIC 8/32C	03D15
SGL.PREC.FLT.PT.	03D14
DBL.PREC.FLT.PT.	03D13

Clock Switches. The Processor runs with two clock speeds and CPB is equipped with an octal switch at IC location 15E to accommodate marginal testing, nominal or normal mode, and extender board testing. Switch Positions 1 through 4 are for the faster Processor clock and Positions 5 through 8 for the slower clock. The following table indicates the use of each switch position. Boards should normally have Position 3 and Position 6 closed.

SWITCH POSITION	USE
1	NOT USED
2	MARGINS
3	NOMINAL
4	EXTENDER BOARD
5	MARGINS
6	NOMINAL
7	EXTENDER BOARD
8	NOT USED

1.5.3.3 35-538 ALU Clock

There are four wire wrap stakes located at the front of the ALU board which provide for three ALU clock speeds. The following table indicates the location of the stakes and the approximate clock rates for each tap, respectively. The ALU should normally be strapped for nominal clocks (60 ± 2 nanoseconds). Clock is at 100-6.

STRAP	FOR	CLOCK SPEEDS
103-6 To 100-6	MRG	56 nanoseconds
103-6 To 101-6	NOM	60 nanoseconds
103-6 To 102-6	NOMA	62 nanoseconds

The TTY Address is normally strapped for X'02' and may be modified to X'82'. The following table correllates the strap position to the TTY address.

TTY ADDR	03J10 TO
X'02'	03J11
X'82'	03J09

1.6 DISPLAY PANEL INSTALLATION

The Model 8/32C or 8/32D Display Panel is electrically tied to the Processor via a connector and Faston lugs. The connector is installed on Connector 3 of the 35-539 IOU board and the terminal lugs mate into a terminal strip on the left side of the Processor chassis as viewed from the front. The terminal lugs are identified at the Faston connector and are mated to their corresponding terminal pin (C1, C2, etc.) on the strip. The Display Console is physically mounted to the brackets provided on the Processor chassis.

1.7 MEMORY INSTALLATION AND EXPANSION (Figures 1-21, 1-22, and 1-23)

1.7.1 First Memory Expansion (up to 512KB) Cabling on 8/32C (or 1024KB) on 8/32D

In 8/22C Systems, memory may be expanded beyond 128KB, in increments of 128KB, up to 512KB in one expansion chassis. Each 128KB increment requires the addition of four 32-206 32KB memory modules. If expansion beyond 512KB is desired, a second expansion chassis is required.

In 8/32D Systems, memory may be expanded beyond 256KB, in increments of 256KB, up to 1MB in one expansion chassis. Each 256KB increment requires the addition of four 32-209 64KB memory modules.

Refer to Figures 1-21 and 1-22. All memory modules up to a maximum of 512KB in the 8/32C (1MB in the 8/32D) are installed in the expansion chassis above the basic Processor chassis. The MBC is installed in upper Slot 1 of the Processor chassis and the two LMI modules are installed in upper Slots 2 and 5 of the Processor chassis. Upper Slots 3, 4, 6, and 7 remain blank. The first memory expansion chassis accommodates memory of 256KB, 384KB, and 512KB in the 8/32C, or 256KB, 512KB, 768KB, and 1MB in the 8/32D.

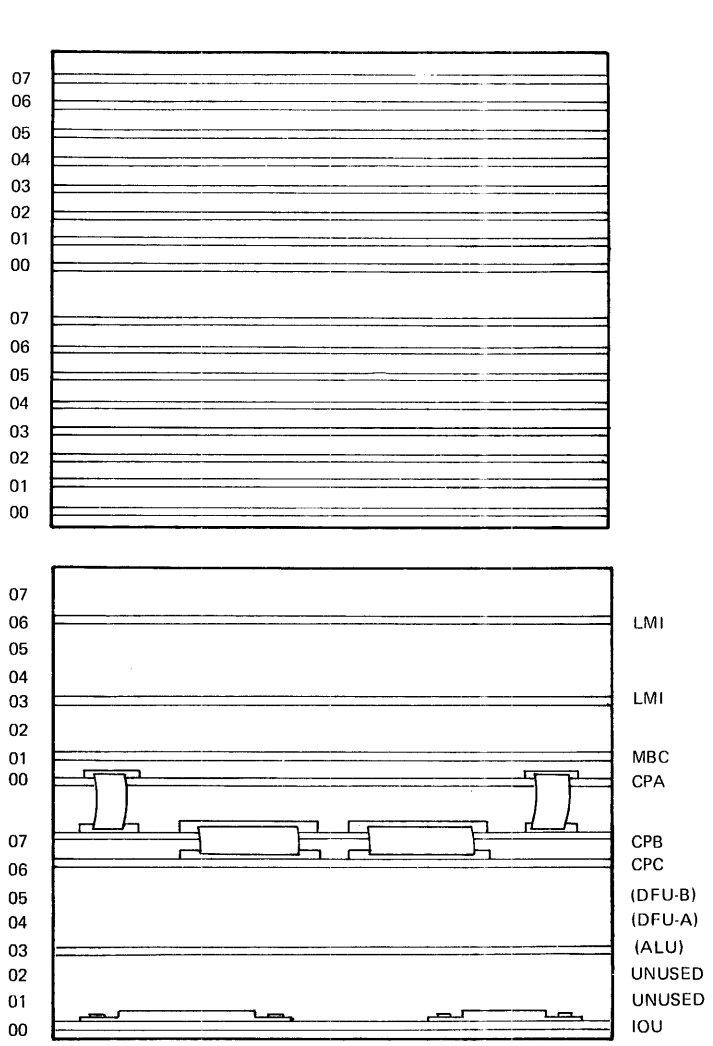


Figure 1-21. Front View of 8/32C Processor Configuration with First Memory Expansion

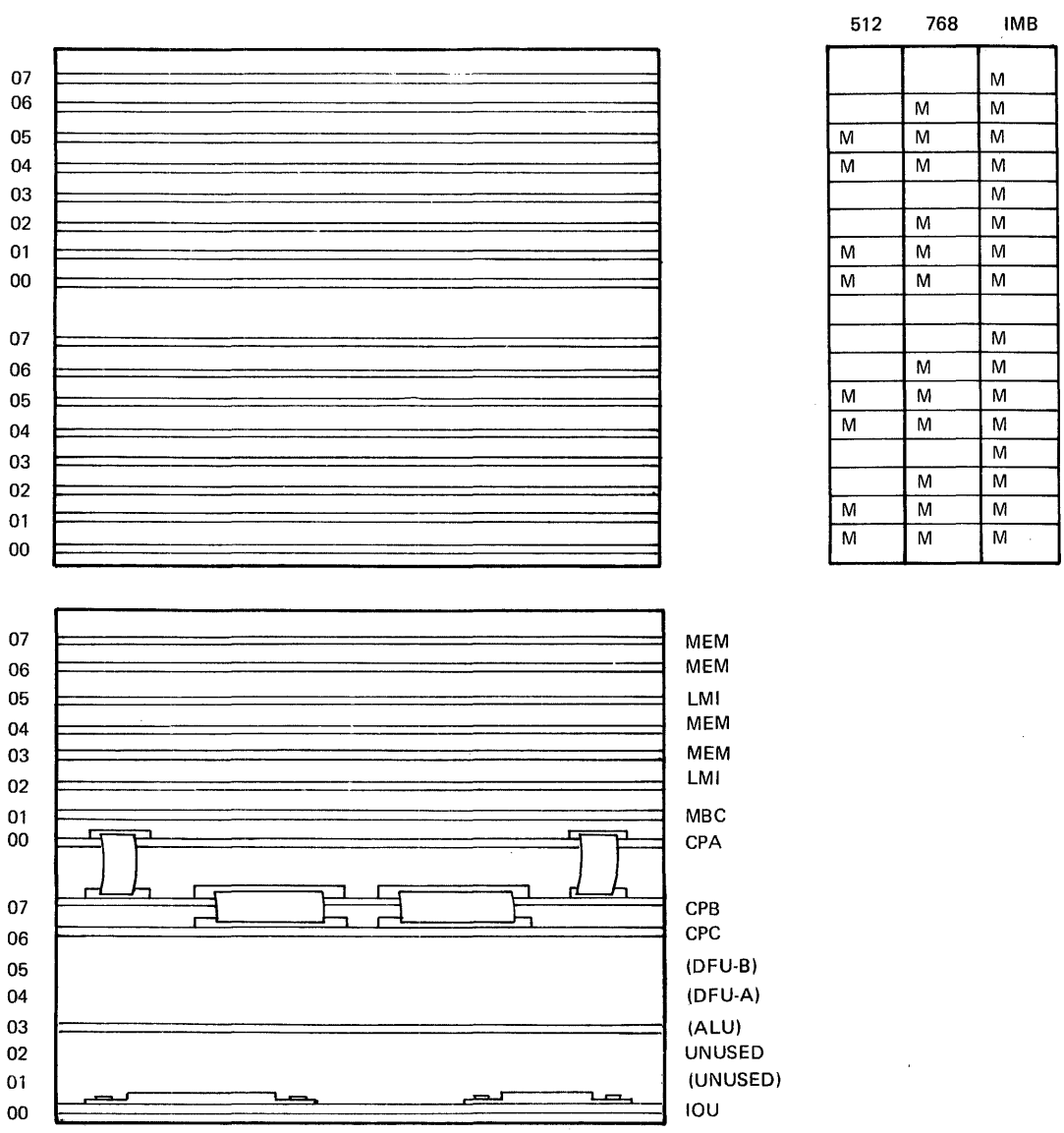


Figure 1-22 Front View of 8/32D Processor Configuration With First Memory Expansion

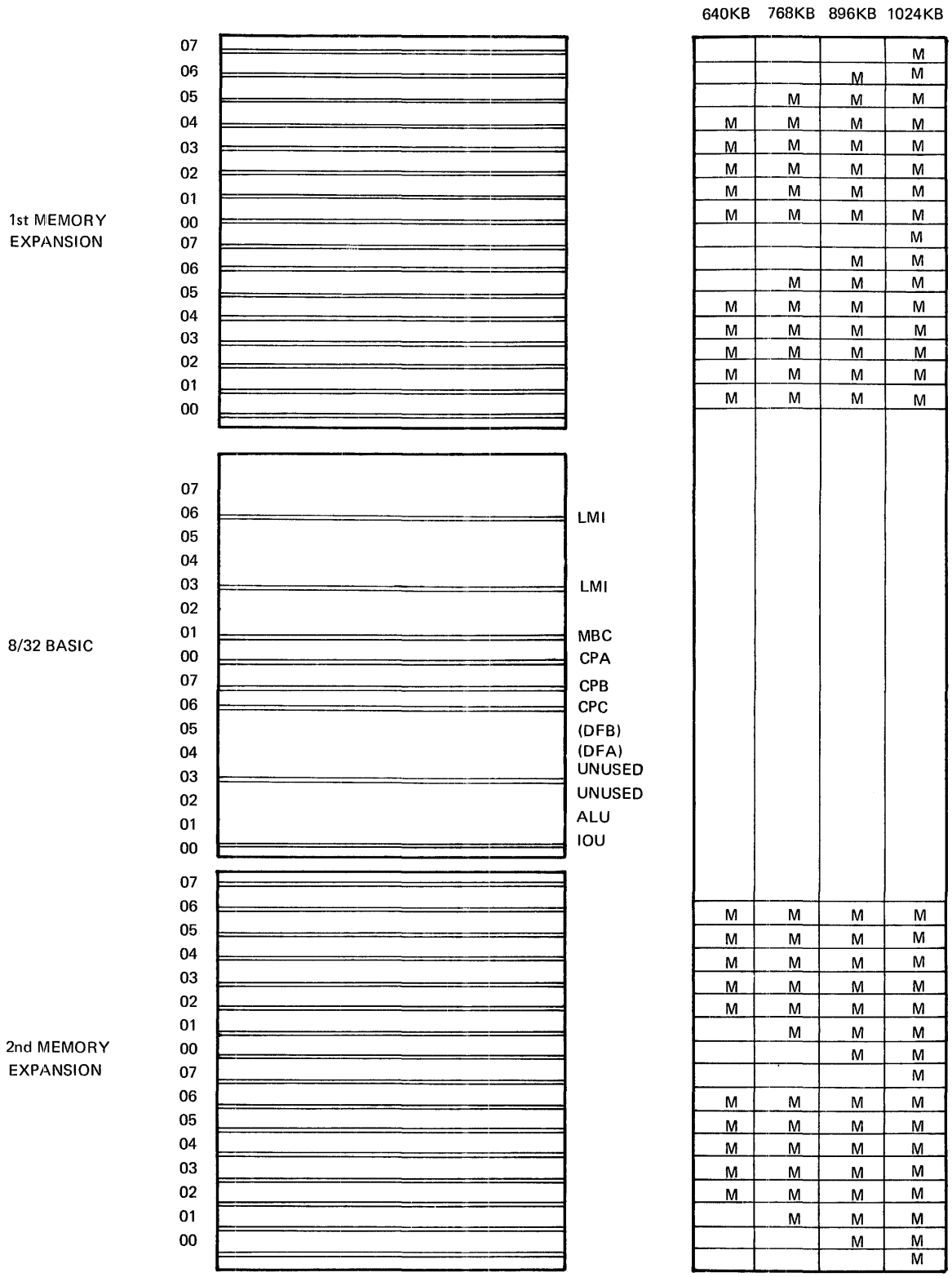


Figure 1-23. Front View of Processor Configuration with First and Second Memory Expansion (8/32C only)

1.7.2 Second Memory Expansion (8/32C only)

A second Memory Expansion chassis is required for memory size greater than 512KB. Up to 1MB of memory may be accommodated with two Expansion chassis.

All memory modules are installed in the two Memory Expansion chassis, the first located above and the second below the Basic Processor chassis. The MBC module is installed in upper Slot 1 of the Processor chassis and the two LMI modules are installed in upper Slots 3 and 6 of the Processor chassis. Upper Slots 2, 4, 5 and 7 remain blank.

NOTE

No Second Memory Expansion is required for 8/32D.

1.8 CONFIGURATION

1.8.1 Basic Chassis I/O

The Processor Multiplexor Bus is capable of driving 14 loads (not including the built-in Teletype and Display interfaces). The overall length of the bus is not to exceed a 914 mm (36") cable, plus 16 copper slots, plus a 17-183 or a 17-224 or a 127 mm (5") cable.

1.8.2 System Expansion Chassis

When configuring a multi-chassis system there are four rules:

1. The system Expansion chassis must be mounted below the basic Processor chassis, or in an adjacent rack.
2. All chassis must be contiguous.
3. All 356 mm (14") system Expansion chassis must be mounted above any 254 mm (10") system Expansion chassis.
4. Multiboard peripheral device controllers (on 254 mm (10") circuit boards) can only be used in the 254 mm (10") system Expansion chassis.

1.8.3 Circuit Board Distribution

Models 8/32C or 8/32D Digital Systems may be configured in a variety of ways. However, the following factors must be considered when determining circuit board distribution within the basic Processor and the system Expansion chassis.

1. The Extended Selector Channel can be placed in Slots 6, 4, 2, or 0 of the system Expansion chassis. Use only the 35-508M00R12 or the 35-508M01 (R00 or higher) ESELCH Card.
2. All slots on Connector 1 below the position where the ESELCH is inserted become ESELCH Bus slots. (This only applies within the back panel containing the ESELCH.) The ESELCH Bus extends down the right side connectors (rear view). Note that all device controllers on 381 mm (15") adapter boards connect the Multiplexor Bus from left side connectors (rear view). Therefore, these device controllers may be inserted in vacant ESELCH Bus slots, but are not on the ESELCH Bus. This also applies to all 178 mm (7") boards on adapters, installed on the left side.
3. The ESELCH Bus can be extended by cable to any even numbered slot in an I/O chassis. In this case, the I/O Multiplexor Bus must be cut between the even numbered slot and the slot above it.
4. All device addresses are hard-wired on the device controller boards, (device addresses may be changed at option) so that the distribution of I/O device controllers in the chassis normally need be considered as a matter of priority in the RACK0/TACK0 "daisy-chain" and convenience.
5. The 178 mm (7") system Expansion chassis may only be used for single board I/O device controllers unless the interconnection between boards takes place via cables on the outer edge of the board. For multi-board 254 mm (10") device controllers, the 254 mm (10") system Expansion chassis must be used.
6. The interrupt priority of a given device controller is determined by its physical location on the serial RACK0/TACK0 line. Refer to 1.8.4 Interrupt Priority Back Panel Wiring to determine which physical location has what priority. When deciding which devices should have a higher or lower priority, devices that must be serviced in a specific amount of time or loss of data access occurs, should be given a higher priority than a device with a high interrupt rate but no data loss if not serviced.

1.8.4 Interrupt Priority Back Panel Wiring

The Acknowledge Control line from the Processor carries the interrupt Acknowledge (ACK) signal. This line breaks up into a series of short lines to form the "daisy-chain" priority system. The ACK signal must pass through every controller that is equipped with interrupt control circuits. Back plane wiring for interrupt control at a given position is: The Received ACK (RACK0) at Pin 122-0 or 1 and the Transmitted ACK(TACK0) at Pin 222-1 or 0. The daisy-chain bus is formed by a series of isolated lines which connect Terminal 222-1 or 0 of a given position to Terminal 122-1 or 0 of the next position (lower priority). On unequipped positions, a jumper shorts 122-1 or 0 and 222-1 or 0 of the same connector to complete the bus. Back panels are wired with jumpers on all positions. Whenever a card chassis position is equipped with a controller that has an interrupt capability, the jumper from 122-1 or 0 and 222-1 or 0 must be removed from the back plane at that position. On the IOU board location in the Processor chassis, the daisy-chain starts at one of 127-0, 128-0, 129-0 or 130-0 terminals (Slot 0) and normally goes to the Console TTY RACK0, Terminal 137-1 of the same slot. The TTY TACK0 (237-1) is cabled with 17-385F01/F02 to Pin 134-0 of an expansion chassis.

Figure 1-24 shows the standard interrupt priority wiring to resolve conflicts in attention requests, queued on the same RACK0/TACK0 "daisy chain." The arrows indicate the direction of priority from the highest priority to the lowest. By changing the wires crossing from Side 0 to Side 1 of the Processor and/or Expansion panels, interrupt priorities may be rearranged. An example of this is shown in Figure 1-25, Modified Interrupt Priority. Slot 0 on Side 1 of the Processor panel has the highest priority. When Extended Selector Channels (ESELCHs) are installed, the standard interrupt priority must be modified. Refer to Figure 1-26 Interrupt Priority with ESELCH Installed. The Multiplexor Bus may be restored to the remaining slots on Side 1 that are not used for the private ESELCH Bus. This may be accomplished by using the 17-183 cable. To prevent this, install the ESELCH as low as possible in the chassis.

For controllers that occupy several positions, the jumper is removed only at the position where the controller board has ATN/ACK circuits. For details on the various devices, see the appropriate installation specification.

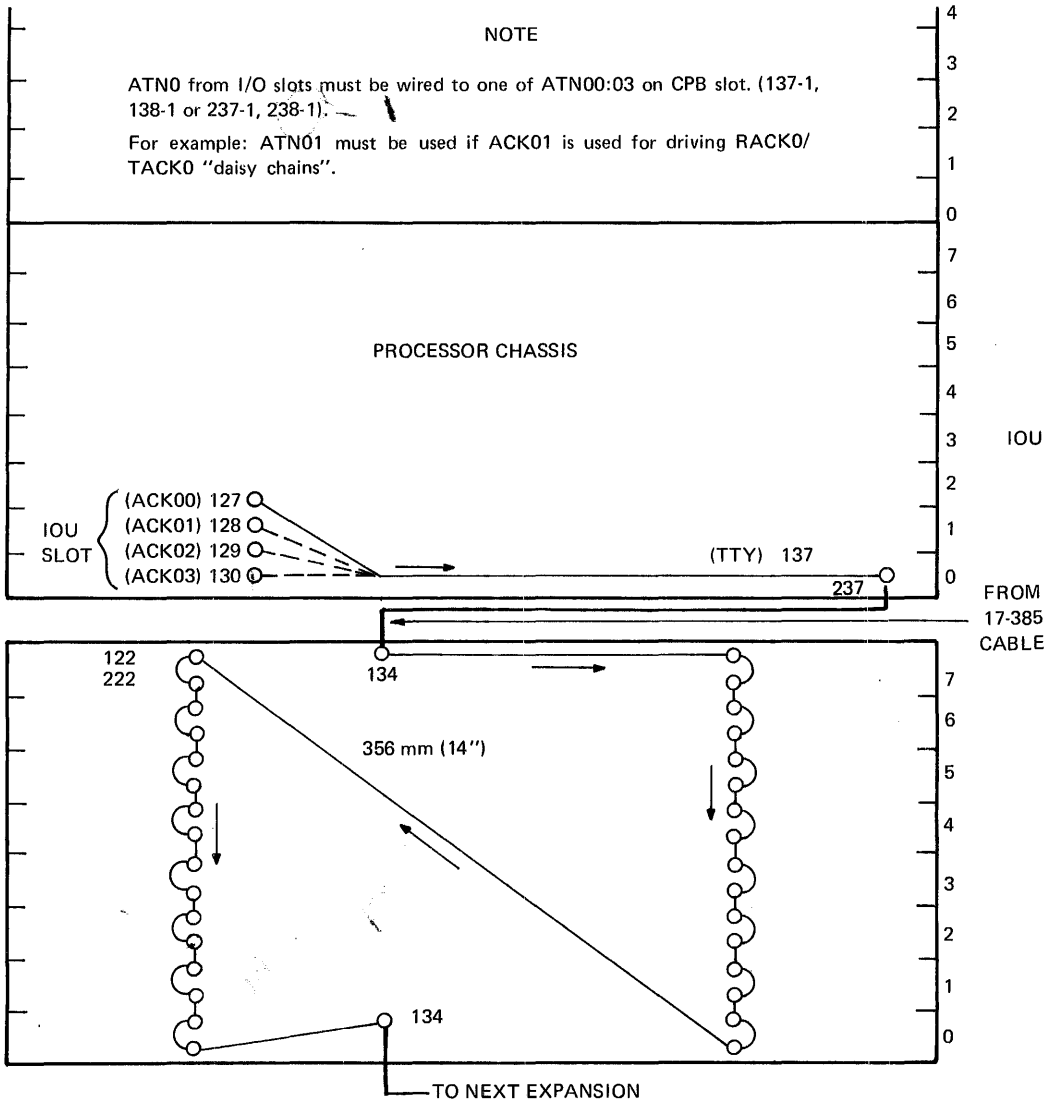


Figure 1-24. Standard Interrupt Priority

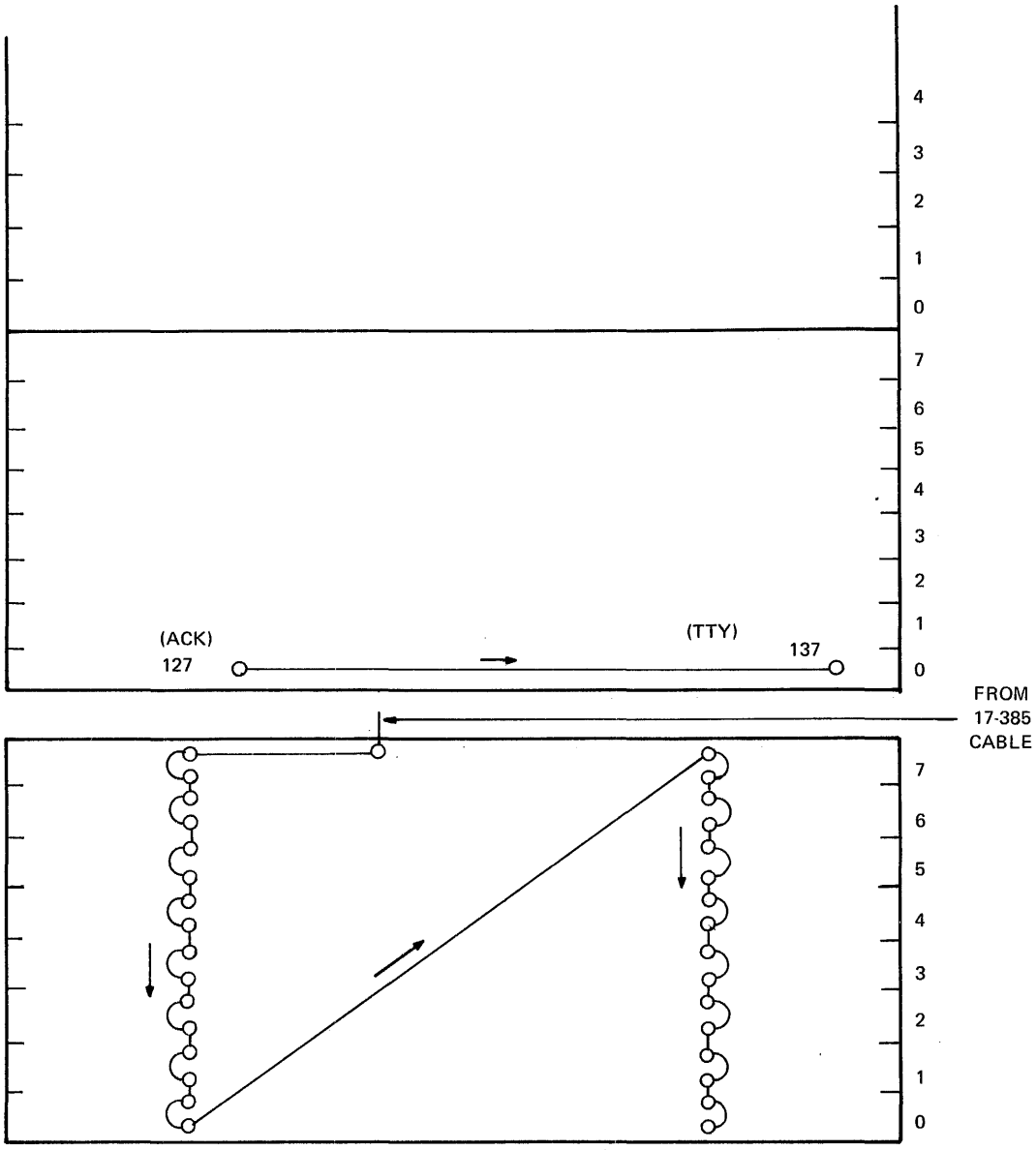


Figure 1-25. Modified Interrupt Priority

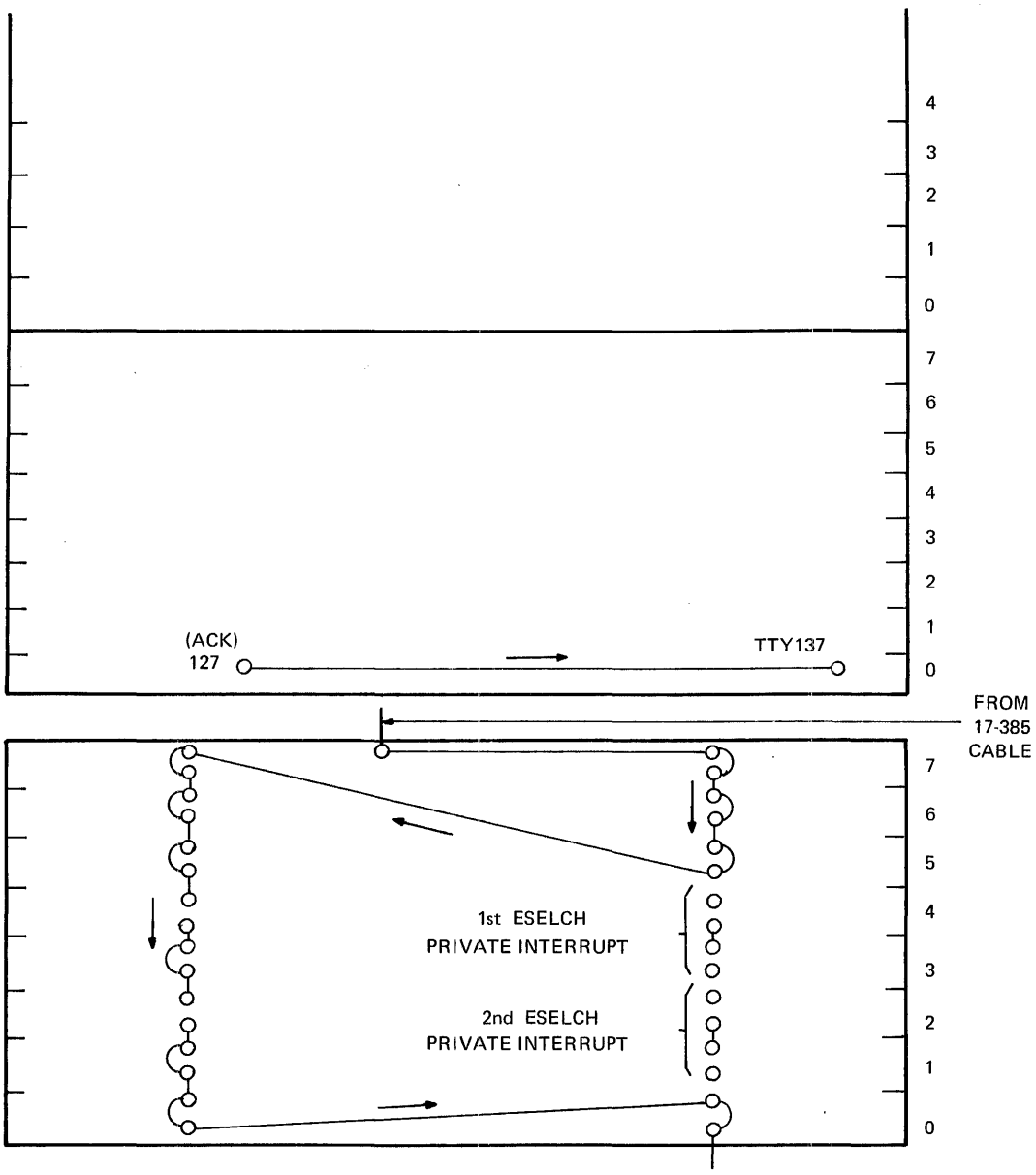


Figure 1-26. Interrupt Priority with ESELCH Installed

1.8.5 Terminators

35-433: I/O Bus Terminator. Install one at the end of the Mux Bus.
35-548: EDMA Bus Terminator, Connector 1. Install at the end of the EDMA Bus.
35-572: EDMA Bus Terminator, Connector 1. Install at the end of the EDMA Bus.

1.8.6 Multilevel External Interrupts

1. The 8/32C or 8/32D is capable of acknowledging four levels of external interrupts. Associated with each interrupt level is an Attention (ATN) line and priority chain (RACK0/TACK0).

2. The four Attention lines (ATN000:030) located on CPB (lower Slot 7) are wired to the OR-tied Attention lines of the device controllers (or external Processor).

3. The four Acknowledge lines (ACK000:030) located on the IOU (lower Slot 0) are the sources of the priority chain.

4. ATN/ACK levels must not be crossed. That is, ATN000 must be OR-tied to ATN line of those devices in the ACK000 priority chain. Similarly, ATN010 must be in the ACK010 priority chain, etc.

5. Standard 8/32C or 8/32D backplane wiring is as follows:

   – ATN000 on CPB is wired to ATN0 on IOU
   – ACK000 on IOU is wired to TTY RACK0 on IOU
   – TTY TACK0 comes out on 17-385 cable

1.9 CABLES

1.9.1 Power Cable

The standard INTERDATA cabinet is wired for 30 Ampere service. On the main power cable (part of the AC Distribution Panel), there is a three-wire, twist-lock, grounding, 125VAC, 30 Ampere, UL, (Hubbel #2610) plug. A three-wire grounding, 30 Ampere, 125 VAC receptacle (Hubbel #2611 or equivalent) is required to accept this plug.

1.9.2 System Expansion Cable

A number of standard cables are available for configuring systems made up of the INTERDATA Expansion chassis discussed in Section 1.4. The choice of cables is dependent upon system configuration. The following cables are always used in pairs:

1. 17-193: I/O Expansion Cable, Connector 0.

   This cable is used to connect the "0" connector field between two adjacent 356 mm (14") chassis.

2. 17-194: I/O Expansion Cable

   This cable is used to connect the "1" connector I/O fields between two adjacent 356 mm (14") chassis.

3. 17-216: I/O Expansion Cable, 914 mm (36") long

   This is a 914 mm (36") long cable. It can be used to connect two 356 mm (14") chassis that are not adjacent.

4. 17-214: 356 mm (14") to 254 mm (10") Expansion Cable

   This cable is used to connect the "0" connector field of a 356 mm (14") chassis to a lower adjacent 254 mm (10") chassis. It provides an 8-bit I/O bus to the 10 inch card file.

5. 17-166: 356 mm (14") to 254 mm (10") I/O Expansion Cable, 914 mm (36") long

   This cable is used to connect the "1" side of a 356 mm (15") expansion chassis to a 254 mm (10") expansion chassis. It provides an 8-bit I/O bus to a 254 mm (10") chassis. It must not be connected to the Basic Processor Multiplexor Bus. It may be driven either by an Extended Selector Channel or a bus buffer. It can be used on the older 254 mm (10") chassis (13 I/O slot).

6. 17-183: "0" to "1" Connector

   This cable issued to interconnect the I/O Multiplexor Bus of the "0" field and the "1" field within a 356 mm (14") chassis.

   There is no RACK0/TACK0 wire in this cable.

   It can also be used to connect a "0" side (Slot 0) of a file, to the "1" side (Slot 7) of the next adjacent file, or vice versa.

7. 17-215: 254 mm (10") to 254 mm (10") I/O Expansion Cable

   This cable is used to connect two adjacent 254 mm (10") chassis.

8. 17-326: EDMA/I/O Connector 0
9. 17-327: EDMA/I/O Connector 1
10. 17-328: EDMA only Connector 0, 914 mm (36")
11. 17-329: EDMA only Connector 1, 914 mm (36")
12. 17-336: EDMA Connector 1
13. 17-335: Memory Data/Memory Sense Cable
14. 17-334: Memory Address Expansion Cable
15. 17-359: EDMA/I/O Connector 1, 914 mm (36")
16. 17-360: Processor Connector 2/5
17. 17-361: Processor Connector 3/4
18. 17-374: I/O/EDMA, Connector 0, 914 mm (36")

1.9.3 Typical Configurations

Refer to Figure 1-27 for typical system configuration

1.10 TESTING

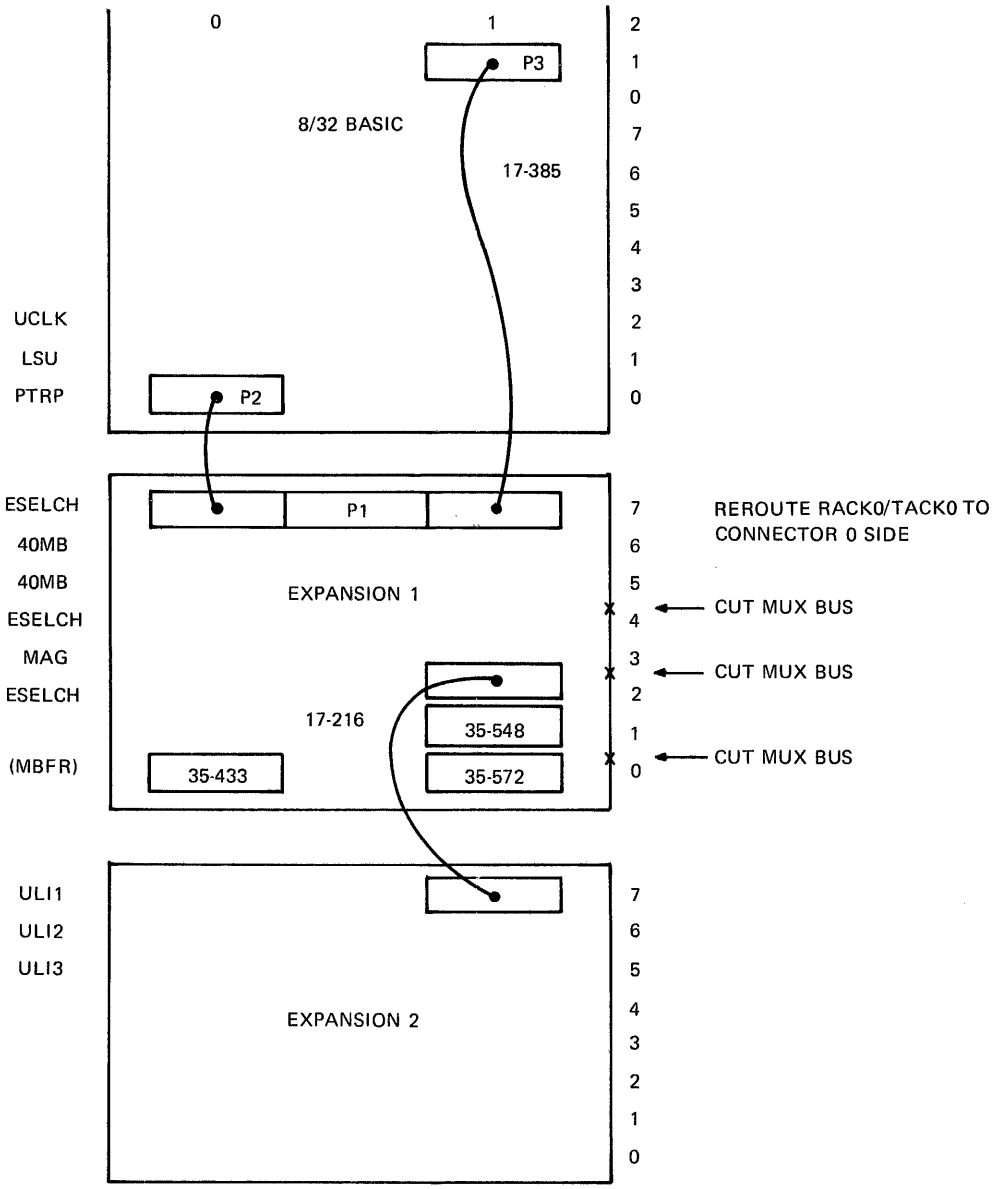
1.10.1 Standard Test Software

The following software is supplied with the basic Processor to insure that the system is operational:

1. Processor Test Programs	06-154, 155, 178
2. Memory Test Program	06-156 (F01, F02, F03)
3. Floating Point Test	DR320005
4. TTY Test Program	06-004
5. MAC Test Program	06-160 (F01 and F02)

1.10.2 Additional Software

In addition to the test software mentioned above, appropriate test software is supplied with each peripheral.



NOTES

1. THE MUX BUS TERMINATED AT THE END.
2. THE EXPANSION CHASSIS MAY BE MOUNTED WITHIN THE 8/32 CABINET OR IN AN ADJACENT CABINET.
3. THE EDMA BUS IS TERMINATED AT THE END OF THE BUS.
4. PROVISION HAS BEEN MADE FOR THE INSTALLATION OF A MBFR IF FUTURE EXPANSION IS NECESSARY.

Figure 1-27. Typical System Configuration (Back Panel)

CHAPTER 2
MODELS 8/32C AND 8/32D WRITABLE CONTROL STORE INSTALLATION

2.1 INTRODUCTION

The Writable Control Store (WCS) option extends the flexibility of the user level Processor to that of a micro-machine. The WCS can store and retrieve data within the control store and dynamically alter control store instructions. The micro-programmer has the full capability of the user level machine at micro-processor speeds.

The WCS has 2KB of control store, sufficient to contain 512 instructions or a combination of instructions and data. It is contained on the 8/32 CPC Processor board and requires typically 7 Amperes of 5VDC for power. This chapter provides information for the installation of the 8/32 Writable Control Store (WCS) option.

2.2 CHASSIS INSTALLATION

Slot 6 of the Processor lower chassis is used for the 8/32 WCS option. The WCS is mounted on the 35-555F01 board (the 8/32 Processor CPC board). Refer to Section 1.4.3.8 for correct power installation.

2.3 CABLING

The 17-360 cable connects Connector 4 on the CPB and CPC Processor boards.

2.4 STRAPPING

The Writable Control Store is factory strapped to respond to addresses in the X'800'-'9FF' range.

2.5 TESTING

Upon completion of installation, and before power is applied, all voltages should be checked for shorts between each other and ground. Operation of the WCS is tested by WCS Test Program, 06-192.

2.6 OTHER

Illegal instruction ROM, 19-195F13, on the 8/32 CPB board (35-537) at Location 00C must be replaced by 19-195F14.

CHAPTER 3
MODELS 8/32C AND 8/32D
DFU INSTRUCTION

3.1 INTRODUCTION

The DFU option is a module of the 8/32C and 8/32D architecture which handles the single and double precision floating point operations of the user instruction repertoire. The DFU contains single and double precision floating registers and performs the floating point operations with no firmware assist from the Central Processing Unit (CPU).

The unit is composed of two, standard size 381 mm (15") circuit boards, DFA (35-590) and (35-591) and uses high-speed Schottky TTL logic. The boards plug into the CPU lower back panel in two slots. Communication with the CPU is via the B Bus, S Bus, ASEL, and BSEL lines.

The DFU contains its own clock and control logic, therefore, while operating it releases the CPU. This allows the CPU to perform instructions using other modules concurrently with the DFU. It is conceptually possible to have two DFUs operating simultaneously under control of the microprogram.

3.2 INSTALLATION

3.2.1 Component and Power Requirements

The following components are required for installation of the 8/32C or 8/32D DFU:

1 ea DFA	35-590
1 ea DFB	35-591
2 ea Cables	17-317
1 ea Cable	17-191F01
1 ea Cable	17-191F02

The DFU requires 5V, 24 Amps maximum. When the DFU is installed in an 8/32C, refer to Figures 1-10 to 1-16 to see if P5, P15 and N15 power supply connections must be changed.

3.2.2 DFU

When the DFU is installed in the 8/32C, or 8/32D the following components must be at the indicated revision levels or higher.

CPB	– 35-537 R00	F01
IOU	– 35-539 R17	
CARD FILE	– 12-015	F04

3.2.3 Option Strapping

The CPB 35-537 privilege illegal ROM must be strapped to allow floating point operations. The straps shown in Table 3-1 must be installed.

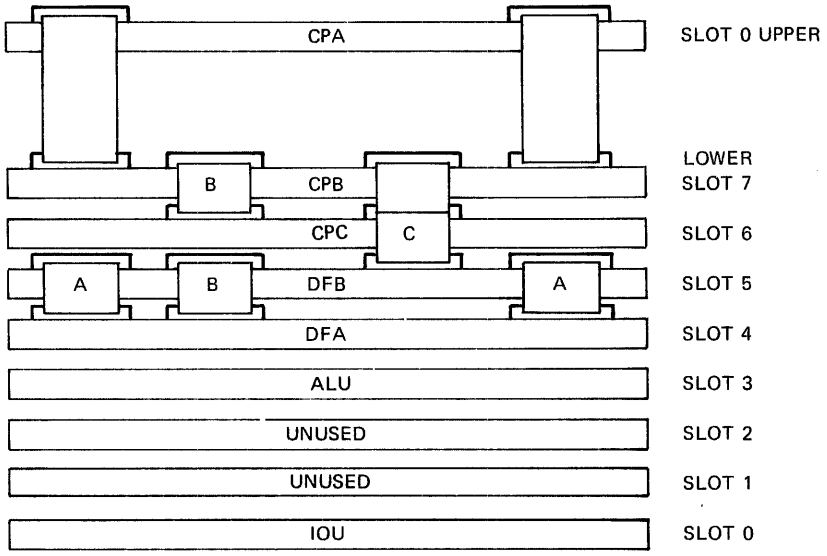
IOU 35-537 MCR Bit 4 strapping is accomplished to signal the DFU presence by strapping MCR bit 4 to GND.

The DFU may be strapped on DFA 35-590 as Module 4 or Module 6. The standard microcode uses Module 6. Strap 07T01 to 08T01 for Module 6, Strap 09T01 to 08T01 for Module 4.

The DFU must be plugged in slots 5 and 4 of the lower CPU backpanel. DFB plugs into Slot 5 and DFA into 4. Slots 1 and 2 are not used. The installation of boards is shown in Figure 3-1; cabling of the DFU is also shown in the figure. All cables are "Ribbon" type and connect to the front edge of the board (opposite backpanel).

TABLE 3-1. DFU PRIVILEGE ILLEGAL ROM STRAPPING

INSTRUCTION	STRAPPING
BASIC INSTRUCTION SET	03D02 TO 03D15
BASIC AND FLOATING POINT	03D02 TO 03D14
BASIC AND COMMUNICATION	03D02 TO 03D15 03D09 TO 03D08
BASIC, COMMUNICATION AND FLOATING POINT	03D02 TO 03D14 03D09 TO 03D08



A - 17-317
B - 17-191F01
C - 17-191F02

Figure 3-1. DFU Board Installation and Cabling

3.2.4 Testing

The following diagnostics are available to test the DFU.

06-193	Single and Double Floating Point Test
DR320005	Single Precision Random Number Test
DR320006	Double Precision Random Number Test

CHAPTER 4
MODELS 8/32C AND 8/32D
COMMUNICATION INSTRUCTION PACKAGE INSTALLATION

4.1 INTRODUCTION

The 8/32C and 8/32D Communication Instruction Package adds three instructions to the 8/32C instruction set. These instructions are: Process Byte (PB), Process Byte Register (PBR), and Move And Process Byte String Register (MPBSR). Also provided, through the Auto Driver Channel, is a redundancy checking feature in the Synchronous Data Link Control (SDLC) format. The 8/32C Communciation Instruction Package can be installed only on an 8/32C Processor that contains a CPB board stamped 35-537F01.

4.2 INSTALLATION

When installed at the factory, no unpacking instructions are provided for the 8/32C or 8/32D Communication Instruction Package because the system is ready for use. If the package is purchased separately, it should be immediately unpacked and inspected for any damage. The package consists of the following items:

Communication Hardware Assist Board (35-622)
Half-Board Adapter Kit (16-398)
8/32C And 8/32D Communication Instruction Package Maintenance Manual, Publication Number 29-520
Processor Test Part 4 Half-Board Kit (06-195)

4.2.1 Half-Board Kit

A Half-Board Adapter Kit, supplied with the 8/32C Communication Instruction Package, adapts a 178 mm (7") half-board to be used in a 381 mm (15") slot. The Communication Hardware Assist Board can be mounted on the Connector 0 side of the Half-Board Kit as shown in Figure 4-1. The unused Connector 1 side may be used to mount any other 178 mm (7") board or the blank metal plate.

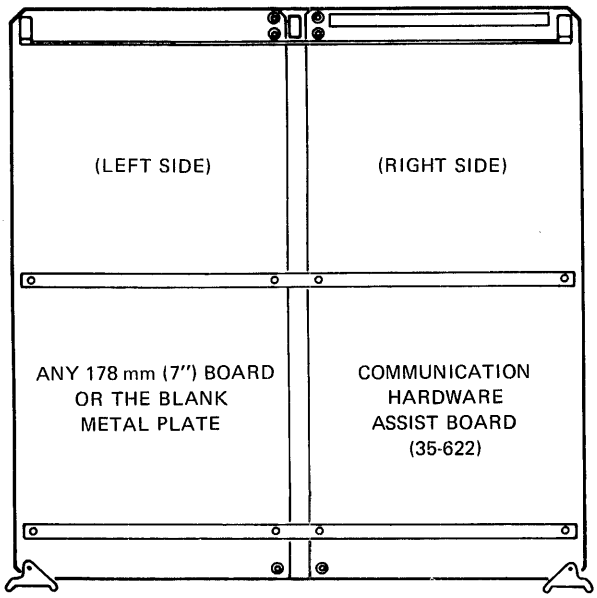


Figure 4-1. Half-Board Assembly

NOTE

The Communication Hardware Assist Board may be strapped for operation on the 8/32C or 8/32D Processor. The strapping is shown in Table 4-1. Insure strapping correct for the processor in use.

TABLE 4-1. PROCESSOR STRAPPING

8/32 C		
ACTION	FROM	TO
REMOVE	G	J
ADD	G	H
ADD	TP6	GND
REMOVE	TP4	GND
REMOVE	K	L
ADD	K	M

4.2.2 Physical Location

The Communications Hardware Assist Board may be located in any slot containing the I/O Multiplexer Bus, but must be located on Connector 0.

4.2.3 I/O Interrupt Priority

The I/O interrupt priority is not important since the Communication Hardware Assist Board can have any priority. The Communication Hardware Assist Board does not generate an interrupt, however, the looped jumper must be removed on Pins 122 and 222 of Connector 0 of the board's slot. The board does receive and transmit RACK0/TACK0.

4.2.4 Processor CPB Board (35-537F01)

The CPB board contains a Privileged/Illegal Instruction Decoder Read Only Memory (DROM). The Privileged Illegal DROM must be strapped to allow the execution of the PB, PBR, and MPBSR as legal instructions. See Table 4-2.

TABLE 4-2. PRIVILEGED/ILLEGAL DROM STRAPPING

INSTRUCTIONS EQUIPPED	DROM STRAPPING
BASIC INSTRUCTION SET	03D02 to 03D15
BASIC + FLOATING POINT	03D02 to 03D14
BASIC + COMMUNICATION	03D02 to 03D15, 03D09 to 03D08
BASIC + COMMUNICATION FLOATING POINT	03D02 to 03D14, 03D09 to 03D08

4.2.5 Processor IOU Board (35-539)

The Auto-Driver Channel micro-code detects the presence of the Communication Hardware Assist Board by testing Bit 5 of the Machine Control Register (MCR). If this bit is ZERO, the micro-code assumes that the Communication Hardware Assist is present. When installing the 8/32C or 8/32D Communication Instruction Package, MCR Bit 5 must be strapped to the ZERO state. To do this, strap 03J02 to 03J08 on the IOU Board (35-539).

4.2.6 Installation Checks

The following checks ensure proper installation of the 8/32C and 8/32D Communication Instruction Package:

1. Check that the Communication Hardware Assist Board is fully seated.
2. Insure that all wiring and strap options are properly installed.
3. Perform the final installation check by running the Processor Test Part 4 (06-195) according to the directions supplied.

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