Publication Number 29-266R01

MODEL 70
MAINTENANCE MANUAL

Consists of:

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MODEL 70
GENERAL DESCRIPTION

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MODEL 70
GENERAL DESCRIPTION

1. INTRODUCTION

The Model 70 combines advanced circuitry and packaging designs to give the user a price/performance optimized machine. The Model 70 is completely upward compatible with INTERDATA Model 3, 4 and 5 Processors user instructions, interrupt handling, input/output formats and control sequencing. Because of this compatability, the Model 70 can use the wide range of existing software and peripheral devices.

The Model 70 offers a comprehensive set of 113 instructions making the system both easy to program and efficient to operate. Through multi-function instructions and direct core addressing, coding and debugging time is reduced to a minimum.

Memory is addressable to the eight-bit byte level. Memory is expandable from the basic 8,192 bytes to 65,536 bytes. All memory is directly addressable with the primary instructions, no paging or indirect addressing is required. Sixteen 16-bit General Registers can be used as Accumulators, fifteen of which can also be used as Index Registers. Register-to-Register instructions permit operations between any of the sixteen General Registers, eliminating redundant loads and stores.

The Protect Mode of the Model 70 enables Memory Protect and detection of Privileged instructions, and can be activated under program control. This mode is invaluable in process control, data communication, and time-sharing operations to guarantee that a running program cannot interfere with the integrity of the system.

The Model 70 also provides a flexable Input/Output system in addition to conventional means of programmed I/O. In the Automatic I/O Service Mode, the Processor acknowledges all I/O interrupts and automatically performs much of the overhead prior to activating the Interrupt Service Routine. In conjunction with the Automatic I/O Service, an I/O Channel can perform data transfers and signal counting without interrupting the running program until the specified sequence is completed.

Up to four Direct Memory Access Channels can be added to a Model 70 Memory System. These channels operate over the common Memory Bus, on a cycle stealing basis, through a Direct Memory Access Port which is build into the Processor. Two types of Direct Memory Access Channels can be used with the Model 70 System: The Selector Channel, which permits direct data transfer between any standard oriented INTERDATA device controller and memory; and the Direct Memory Access Channel custom designed by the user for special applications.

2. SCOPE

This specification is intended to enable the digital technician to understand the INTERDATA documentation system. Number Notation, the Part Numbering System, and the Drawing System are described. Illustrations are provided to help understand these systems. Other publications which may be of interest to Model 70 users are shown in Table 1.

TABLE 1. RELATED PUBLICATIONS

Title	Publication Number
Universal Clock Instruction Manual	29-265
Model 70 Users Handbook	29-261
Model 70 Maintenance Manual	29-266*
Multiplexor Bus Buffer Instruction Manual	29-267
8 Line Interrupt Module Instruction Manual	29-268

*This General Description is a part of 29-266

3. BLOCK DIAGRAM

A Model 70 simplified block diagram is shown in Figure 1. The Model 70 is a 16-bit digital computer. The Processor logic is contained on four PC boards:

Part No.	Description	Card File Position
35-387	Memory Control	4
35-390	I/O Board	5
35-389	ALU Board	6
35-388	ROM Board	7

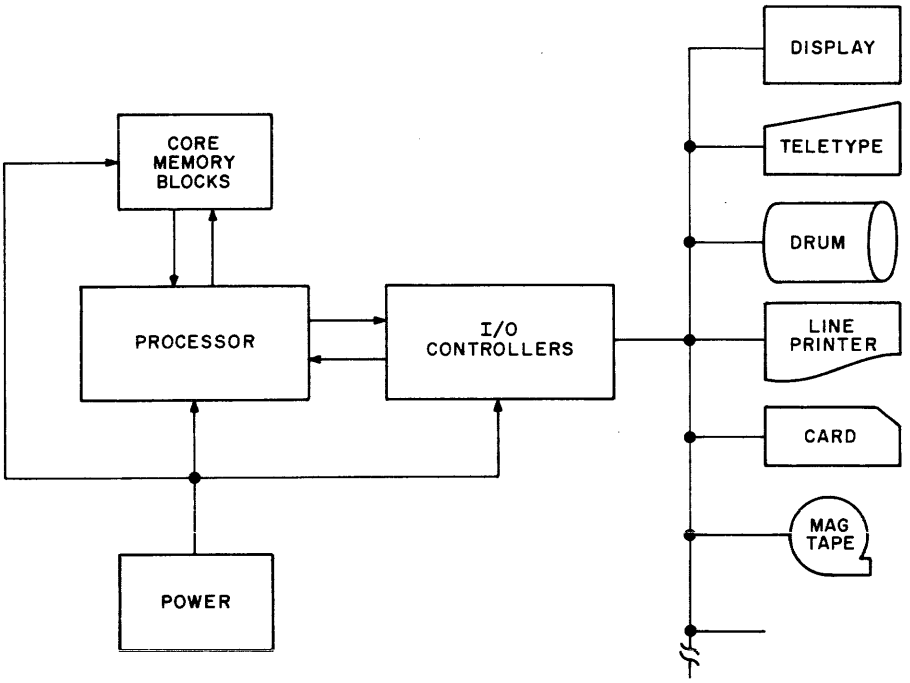

Figure 1. Model 70 Simplified Block Diagram

4. DOCUMENTATION

This section describes the style and conventions used with INTERDATA documentation.

4.1 Number Notation

The most common form of number notation used in INTERDATA documentation is hexadecimal notation. In this system, groups of four binary digits are represented by a single hexadecimal digit. Table 2 lists the hexadecimal characters employed.

TABLE 2. HEXADECIMAL NOTATION DATA

Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal
0000	0	0	0110	6	6	1100	12	C
0001	1	1	0111	7	7	1101	13	D
0010	2	2	1000	8	8	1110	14	E
0011	3	3	1001	9	9	1111	15	F
0100	4	4	1010	10	A			
0101	5	5	1011	11	B			

To differentiate between decimal and hexadecimal numbers, hexadecimal numbers are preceded by the letter "X", and the number is enclosed in single quotation marks. Examples of hexadecimal numbers are: X'1234', X'2EC6', X'A340, X'EEFA', and X'10B9'.

4.2 Part Numbering System

INTERDATA parts, drawings, and publications employ a common numbering system. The part number and drawing numbers for drawings which describe the part are related. The publication number is also often related to the part number of the device or program described. Figure 2 shows the format used for INTERDATA part numbers. The fields are described in the following paragraphs.

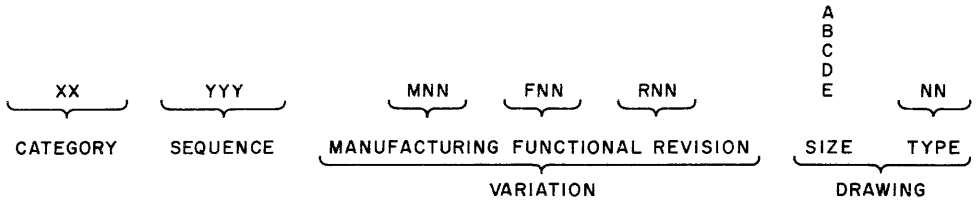

Figure 2. Part Number Format

4.2.1 Category Field. The two-digit Category number indicates the broad class or category to which a part belongs. Typical examples of category number assignments are:

01 - Basic Hardware Systems

02 - Basic Hardware Expansions

03 - Basic Software Systems

04 - Basic Software Expansions

05 - Major Application Programs

06 - Self-contained Utility Programs

07 - Subroutines of General Utility

10 - Spare Parts Packages

12 - Card File Assemblies

13 - Panels

17 - Wire and Cables

19 - Integrated Circuits

20 - Transistors

27 - Peripheral Equipment

29 - Manuals

34 - Power Supplies

35 - Assembled Printed Circuit Boards

36 - Electro-Mechanical Devices

4.2.2 Sequence Field. The Sequence number identifies a particular item within the category. Sequence numbers are assigned serially, and have no other significance.

NOTE

The Sequence Field, like all other part number fields, may be lengthened as required. The field lengths shown on Figure 2 are minimum lengths (insignificant zeros must be added to maintain these minimums).

4.2.3 Manufacturing Variation Field. The optional Manufacturing Variation Field consists of the letter "M" followed by two digits.

NOTE

A part number must contain a Category number and a Sequence number. All other fields are optional.

The M Field is used to distinguish between parts which are electrically and mechanically equivalent (interchangeable), but which vary in method of manufacture. For example, if leads are welded instead of soldered on an assembly, the M Field changes.

An important exception to the meaning of the M Field exists for categories related to software. Here the M Field number, when used, indicates the form in which a particular program is presented. For example, define a program as a set of machine instructions. These same identical instructions may be presented on punched cards, paper tape, or magnetic tape; and for any of these they could be in symbolic form. Thus, there are many ways to represent the same identical program. These ways are identified by the M Field numbers as follows:

M01 - Symbolic Punched Cards

M02 - Relative Binary Punched Cards

M03 - Absolute Binary Punched Cards

M04 - Symbolic Magnetic Tape

M05 - Relative Binary Magnetic Tape

M06 - Absolute Binary Magnetic Tape

M07 - Symbolic Punched Paper Tape

M08 - Relative Binary Punched Paper Tape

M09 - Absolute Binary Punched Paper Tape

M10 - Bootstrap Binary Object Punched Paper Tape

M11 - Read-Only-Memory (ROM) Absolute Binary Object Punched Paper Tape

M12 - ROM Wiring and Test Set (ROMWATS) Wiring Punched Paper Tape

M13 - ROMWATS Check Punched Paper Tape

M14 - Eight-bit Paper Tape

4.2.4 Functional Variation Field. The optional Functional Variation Field consists of the letter "F" followed by two digits. The F Field is used to distinguish between parts which are not necessarily electrically or mechanically equivalent, but which are described by the same set of drawings. For example, a power supply may be strapped internally to operate on either 110 vac or 220 vac. Except for this strap, all power supplies of this type are identical. The strapping option is easily described by a note on the assembly and test specification drawings. Therefore, this is a functional variation.

4.2.5 Revision Field. The optional Revision Field consists of the letter "R" followed by two digits. The R Field is used to indicate minor electrical or mechanical changes to a part which do not change the part's original character. R Field changes often reflect improvements. A part with a revision level HIGHER than the one specified will work. A part with a revision level LOWER than specified should not be used.

4.2.6 Drawing Field. The optional Drawing Field consists of a letter from "A" to "E" followed by two digits. The letter indicates the size of the original drawing. The sizes for each letter are:

A - $8\frac{1}{2}$" X 11"
B - 11" X 17"
C - 17" X 22"
D - 22" X 34"
E - 34" X 44"

The two digits indicate the drawing type as follows:

01 - Parts List
02 - Machine Details
03 - Assembly Details
05 - Art Details
06 - Wire Run List
08 - Schematic
09 - Test Specification
10 - Purchase Specification
11 - Bill of Material
12 - Information
13 - Program Listing
14 - Abstracts
15 - Program Description
16 - Operating Instructions
17 - Program Design Specification
18 - Flow Charts
19 - Product Specification
20 - Installation Specification
21 - Maintenance Specification
22 - Programming Specification

4.2.7 Examples. The following list provides some examples of the part numbering system. The numbers were arbitrarily selected, and in most cases are fictitious.

35-060 The 60th printed-circuit board assigned a part number under this system.

35-060M01 A printed circuit board electrically and mechanically interchangeable with the 35-060, but differing in method of manufacture.

35-060F01 A printed-circuit board not electrically and mechanically interchangeable with the 35-060, but described by the same set of drawings.

35-060P01 A revised 35-060 printed-circuit board. Probably supercedes the 35-060.

35-060A01 The $8\frac{1}{2}$ by 11 inch parts list for a 35-060.

35-060B08 The 11 by 17 inch schematic for a 35-060.

06-072 The 72nd utility program assigned a part number.

06-072A13 An $8\frac{1}{2}$ by 11 inch listing of the 06-072 program.

06-072M03 An absolute binary deck of punched cards for the 06-072 program.

06-072A12 An $8\frac{1}{2}$ by 11 inch information drawing on the 06-072 program. Probably a part of the program.

29-060 The 60th manual assigned a number under this system. Note that this number is not referenced in any way to the part number of equipment described in the manual.

4.3 Drawing System

This section describes the drawings provided with INTERDATA equipment. Note that drawings provided with peripheral devices and other purchased items may vary from the system described in this Section.

A digital system may be divided into a collection of functionally independent circuits such as core memory, Processor, and I/O device controllers. These circuits may or may not be saleable units in their own right, but in the electrical sense they are essentially self contained and capable of performing their function with minimum dependence on other functional circuits in the system. Hence a functional circuit is treated as a building block. Each functional circuit is described electrically by a detailed functional schematic. Each schematic contains a variety of information including type and location of discrete integrated circuits (IC's), pin connections, all interconnections within the schematic connector pin numbers and connections to other schematics. Further, the schematics are drawn to reflect, in an orderly fashion, all logical operations performed by the circuits. Generally, symbols used on schematics conform to MIL-STD-806B.

Registers are named according to the following rules:

1. The register mnemonic name has a maximum of three letters, excluding "I, O, Q, and Z'.
2. Each bit in the register is numbered, usually starting at 00 on the left, or most significant position, and continuing to N-1 on the right, where N is the number of bits in the register.
3. The 00 bit is the Most Significant Bit and the N-1 is the Least Significant Bit.

The IC's, mounted directly on the logic board, are represented on the schematic drawings by logic symbols. Each symbol contains the reference designation, device part number (category and sequence), and symbol mnemonic designation. Refer to Figure 3.

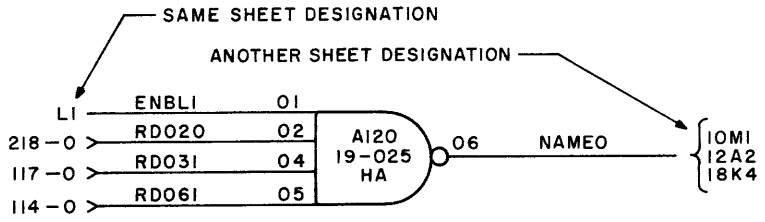

Figure 3. Example of a High Speed NAND Gate.

The designations, numbers, and references shown in Figure 3 are:

A120 - This indicates the component location on the logic board. Figure 4 illustrates the method generally used to determine component location on a logic board. With the logic board oriented so that the header connectors (Conn 0 and Conn 1) are on the right, the components are numbered from left to right starting in the upper left corner. That is, the first IC in the upper left corner is A01 and the first capacitor is C1. Test points are lettered bottom to top from A-Y (omitting I, O, L, E).

19-025- The number 19 is the category number of ICs, and the 025 is the sequence number of the component.

HA - Indicates this component is a high speed AND gate. Some other common designations used are:

P - Power Gate
HP - High Speed Power Gate
G - Gate
HG - High Speed Gate
HGOC - High Speed Gate, Open Collector
B - Buffer
HB - High Speed Buffer

L1 - This input lead is from area L1 on the same schematic sheet.

10M1, 12A2, 18K4 - Indicate outputs to another logic schematic sheet.

218-0, 117-0, 114-0 - Indicate inputs from Connector 0.

Note that the pin numbers (01, 02, 04, 05, and 06) correspond directly to the actual IC pin numbers.

Figure 4 also shows the locations of the header connectors (Conn 0 and Conn 1) and the cable connectors (Conn 2 and Conn 3). All logic boards always contain Header Connectors 0 and 1, however, any combination (either, both, or none) of cable connectors (Conn 2 and Conn 3) may be provided.

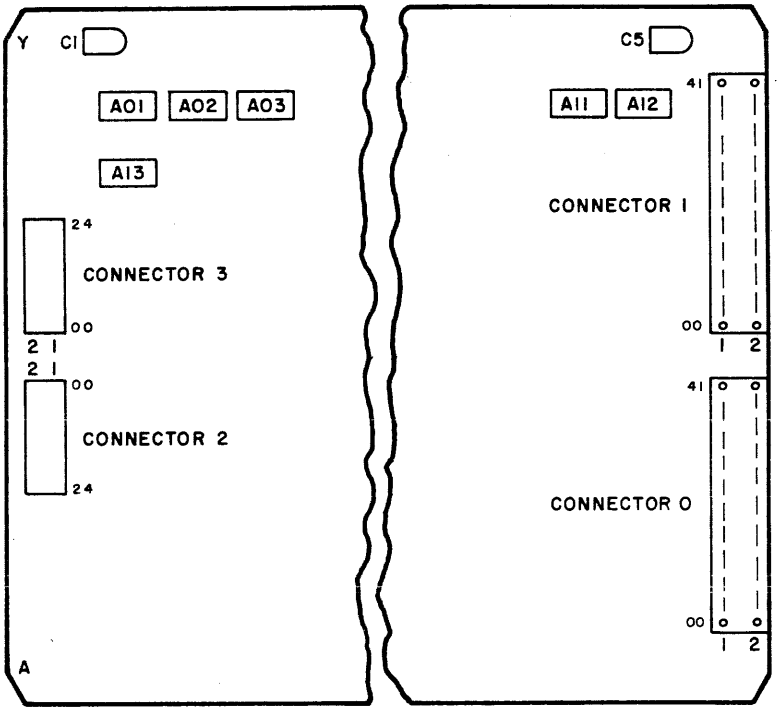

Figure 4. Example of a Logic Board Layout

Figure 5 provides the pin numbering scheme for the header and cable connectors. Header connectors always have 2 rows of pins and 12 positions. Cable connectors always have 2 rows of pins but may vary in the number of positions. The number of positions may only vary in increments of five positions (10 contacts). For instance, if 24 positions are desired, five blocks of five positions each (25 positions) must be used.

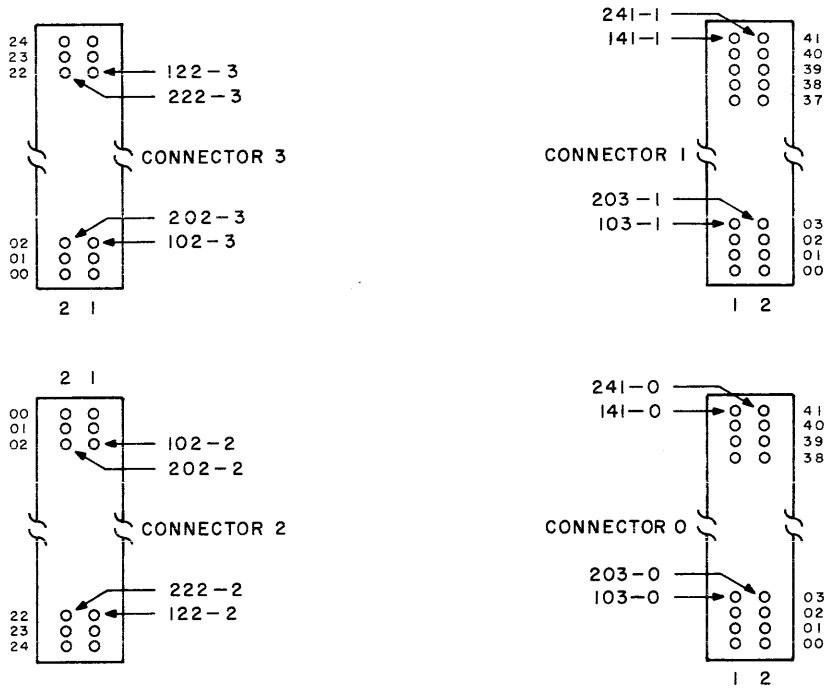

Figure 5. Connector Pin Numbering

A net is defined as an electrical connection between two or more points in a circuit. Ordinarily, a net has an originating end (usually a collector where the signal is generated) and one or more terminating ends. Often it is convenient to assign descriptive mnemonic names to nets as a way of identifying them on schematics. Whether a net is named or not is sometimes arbitrary. However, a net is always assigned a name if:

1. The net is contained on one drawing sheet but is not shown as a complete solid line on that sheet.
2. Part of the net appears on more than one sheet.
3. Part of the net connects with a different schematic.
4. Part of the net leaves a logic board.

If a net is named, the following rules are observed.

1. All mnemonic names are a maximum of six characters.
2. All decimal digits and upper case letters except the letters "I, O, Q, and Z" are permitted.
3. No other characters permitted.
4. Where possible, mnemonics are descriptive. However, it should be recognized that descriptive names are not always possible and a danger of misinterpreting a mnemonic exists.
5. Mnemonic names are not repeated within a schematic.
6. Every mnemonic is suffixed by a state indicator. This indicator consists of the digit "1" for the logically true state, or the digit "0" for the logically false state. For example, the set side of a flip-flop would have the "1" state indicator, while the reset side would have the "0" state indicator. The state indicator for a function changes each time that function is inverted. Thus, the state indicator permits assigning the same mnemonic to functions that are identical except for an inversion.
7. When a logical function is inverted, an inversion indicator is added after the state indicator. This allows for functionally equivalent, but electrically different nets to have the same mnemonic name. For example, assume a signal NAME1. NAME1 may be inverted to produce NAME0. If NAME0 is then inverted, NAME1A is produced. NAME1 and NAME1A are functionally equivalent, but physically different nets.

Sometimes a net fans-out to many sheets in a schematic. It is also possible for a net to fan-out to sheets in different schematics. In these situations, the net is assigned a mnemonic name. The net is also "zoned" from sheet to sheet to allow for properly identifying the originating and terminating ends of the net. The originating end of a net is defined as the collector at which a signal is generated. All other points to which the net connects are called terminating ends. When a lead leaves a sheet at the originating end, it is zoned to each and every sheet on which the net reappears, by indicating first the page number, followed by the schematic number that contains the page. For example, assume that the gate shown on Figure 3 is on a schematic, sheet 20. The output, NAME0, appears on sheets 10, 12 and 18 of the schematic. Note that the schematic number is implied. When a net enters a sheet from another sheet, it is labeled with the same mnemonic name, and is zoned back to the originating end of the net only. Thus, on Figure 3, the ENBL1 may, however, have many other terminations in addition to the one shown. Generally then, when a net leaves the sheet where it originates, it is zoned to every other sheet where the net terminates, while the terminating end is zoned only to the originating sheet. Note that in the Model 70 schematics, signals are co-ordinated between sheets only when the sheets are related to the same board. When a signal leaves a board, the Back Panel Map must be used.

When a lead leaves a logic board, it usually does so through a logic board back panel connector pin. These connector pins must be shown on the schematic even if the complete net is shown on one drawing sheet. Only the connector pin number need be indicated under the pin symbol, since the connector number itself is implied by the logic board location number in the logic symbol or in the footnote. Thus, on Figure 3, RD061 enters the logic board on Pin 114 of Header Connector 0.

Figure 6 is a typical schematic sheet with call-outs illustrating many of the conventions described in this section.

The schematic drawings for the basic Digital System and some of the more common expansions are commonly included in the rear of the appropriate Digital System Maintenance Manual. Schematic drawings for other expansions are included with the expansion or with the publications that describe the expansion.

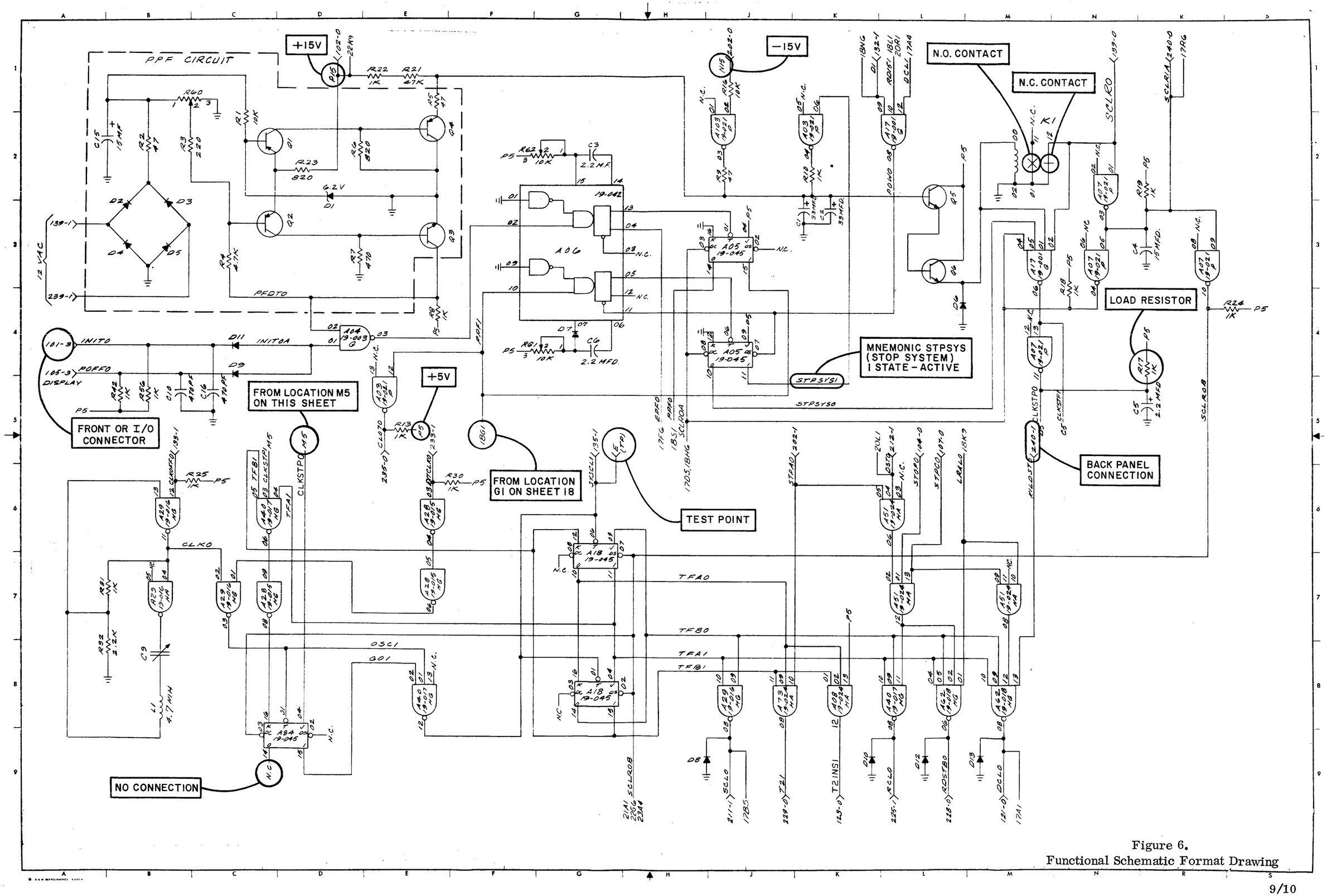

Figure 6.
Functional Schematic Format Drawing

MODEL 70 CHASSIS AND POWER SUPPLY EXPANSION INFORMATION SPECIFICATION

1. INTRODUCTION

The INTERDATA Model 70 Digital System features a highly modular structure which permits configurations to suit the user's exact needs. It provides the means for convenient expansion as the user's requirements grow. This document describes the Processor and System Expansion Chassis, Power Supply Mounting, Filler and Display Panel mounting, and the interconnecting cables. Integrated circuit boards are discussed with respect to cabling and location only. Circuit descriptions of these boards are provided in the appropriate maintenance or instruction manuals. Note that the following discussion assumes that the equipment is mounted in standard INTERDATA cabinets.

2. MECHANICAL COMPONENTS

This section is intended to familiarize the reader with the mechanical components that are discussed here (i.e. Cabinet Uprights, Chassis Support Rails, Filler Panels). Figures 1 through 4 provide the dimensions and mounting configurations for the Rack, Chassis Support Rails, and Filler/Display Panels. Note in Figure 4, that while 3 1/4", 7", and 10 1/2" Filler Panels and the Display Panel mount the same way (via retaining brackets), the smaller 1 3/4" Filler Panel mounts with spring clips.

3. POWER SUPPLY MOUNTING

The Power Supply mounts in the rear of the cabinet, immediately behind its respective Processor or Expansion Chassis. It is attached to the right mounting upright (looking from rear) via two mounting blocks and two nylon spacers. See Figures 1 and 5.

The mounting blocks mount to the upright via three number 10-32 Hex Socket Cap Screws. It may be necessary to drill clearance holes in the upright to accept the three number 10-32 screws.

The power supply may be swung in or out on its mounting pivot (see Figure 6) for easy access to the back plane.

WARNING

Before hinging out the power supplies, the rack levelling feet should be lowered. Only three power supplies can be hinged out at one time, after the levellers are in contact with the floor surface.

When the Power supply is in the installed operating position, it is secured by two 10-32 screws which attach to the left mounting upright (looking from rear). Care must be taken when installing the two mounting blocks to assure proper alignment of the screws. The power supply cable connects to a terminal board (35-382) at the right rear (looking from rear) of its respective Processor or Expansion Chassis via faston lugs and a connector for fan A.C. power. There is adequate slack provided in the cable to allow the Power Supply to hinge out freely. In order to prevent the cable from being pinched between the Power Supply and the Chassis Support Rails, a service loop is required. A maximum of four Power Supplies may be mounted in one rack.

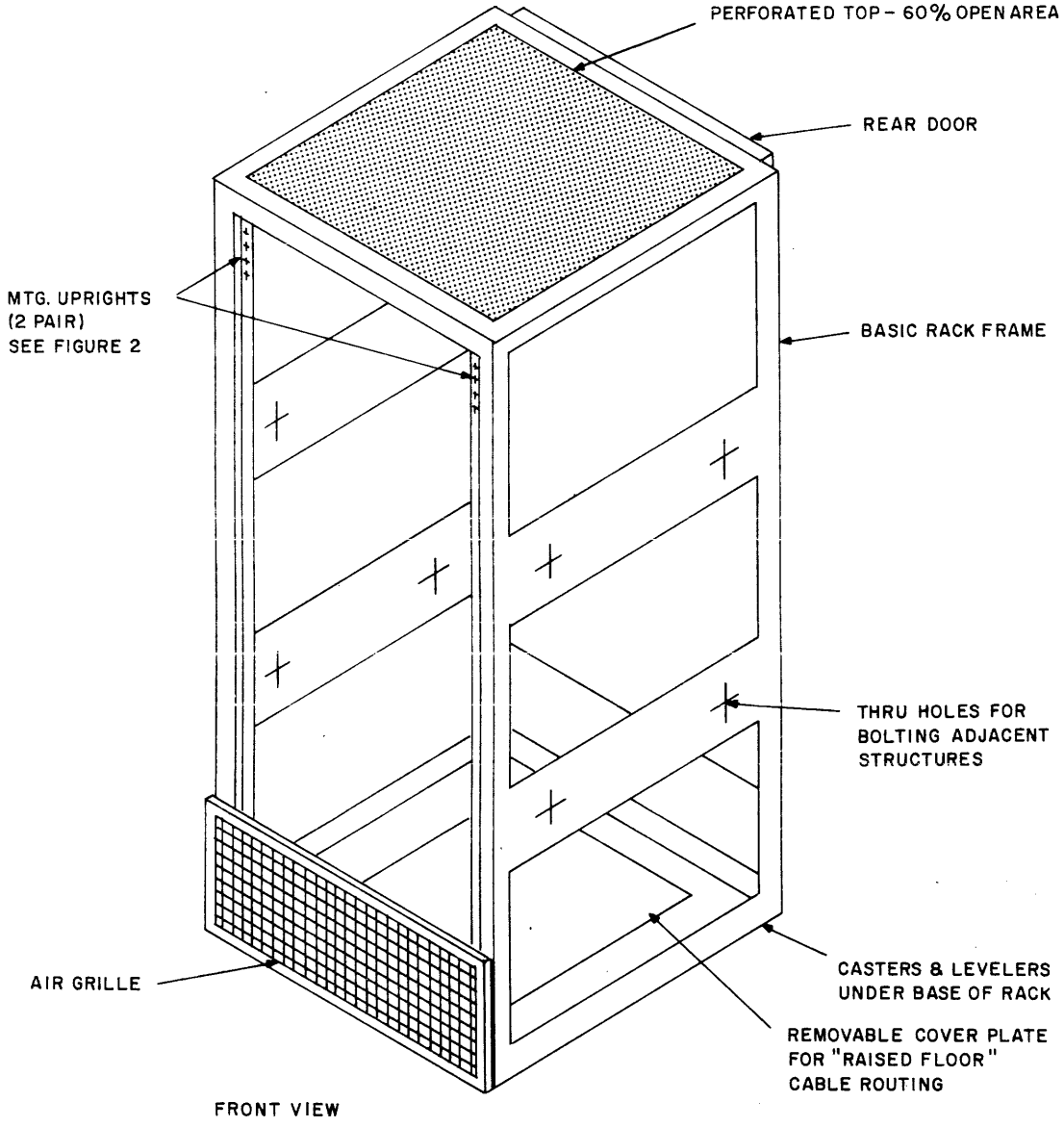

Figure 1. Basic Cabinet

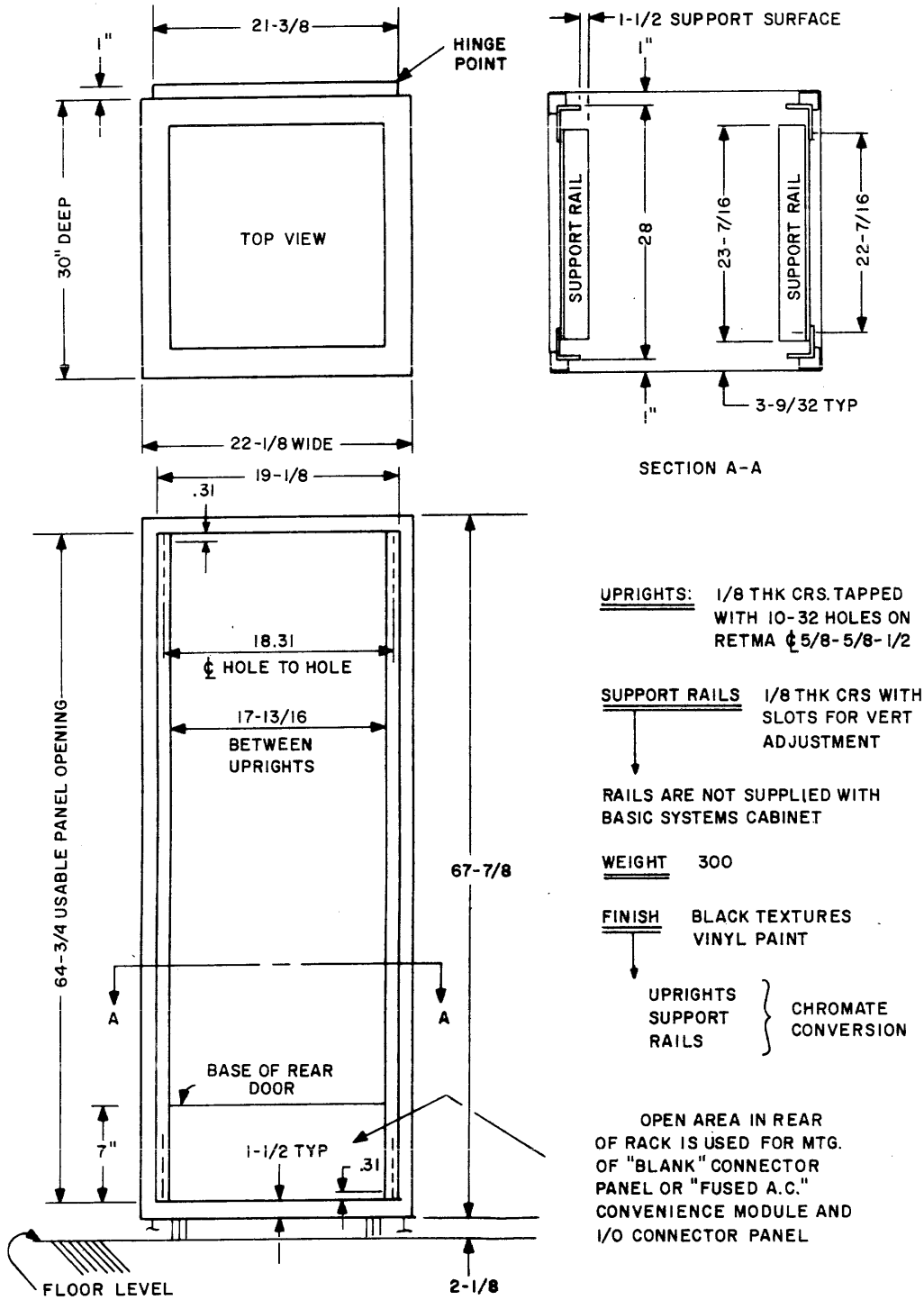

Figure 2. Basic Cabinet Physical Dimensions

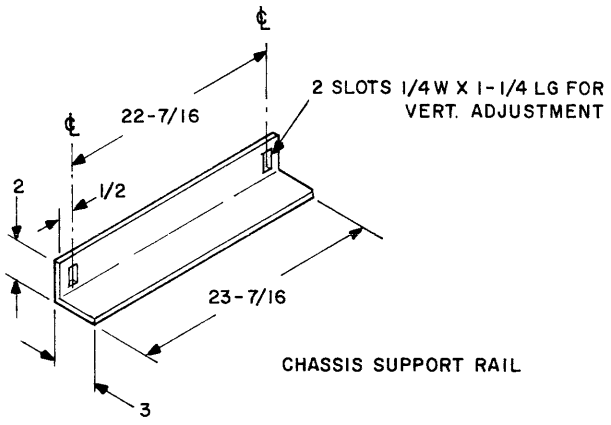

Figure 3. Chassis Support Rail

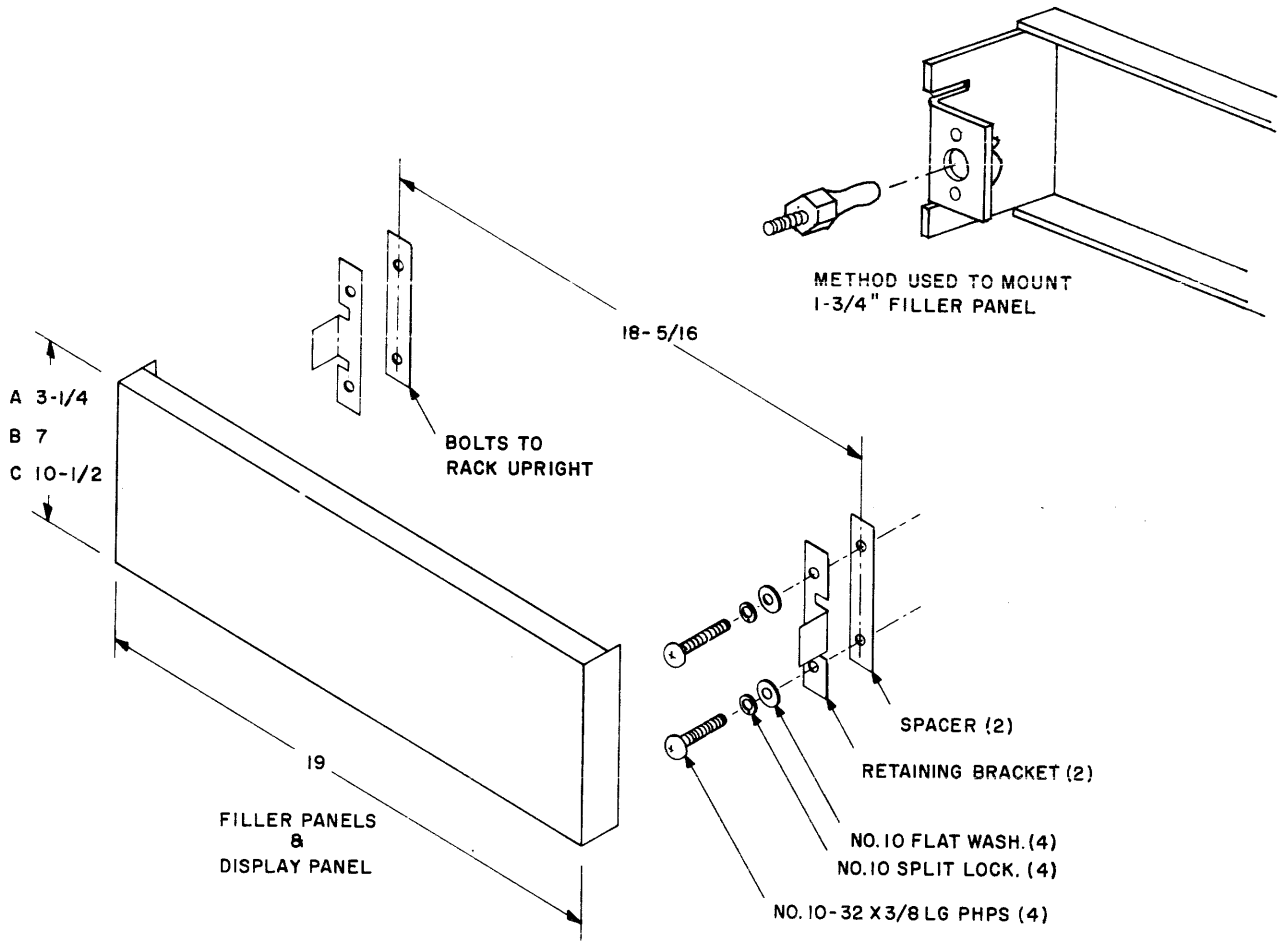

Figure 4. Typical Mounting Configuration for Display and Filler Panels

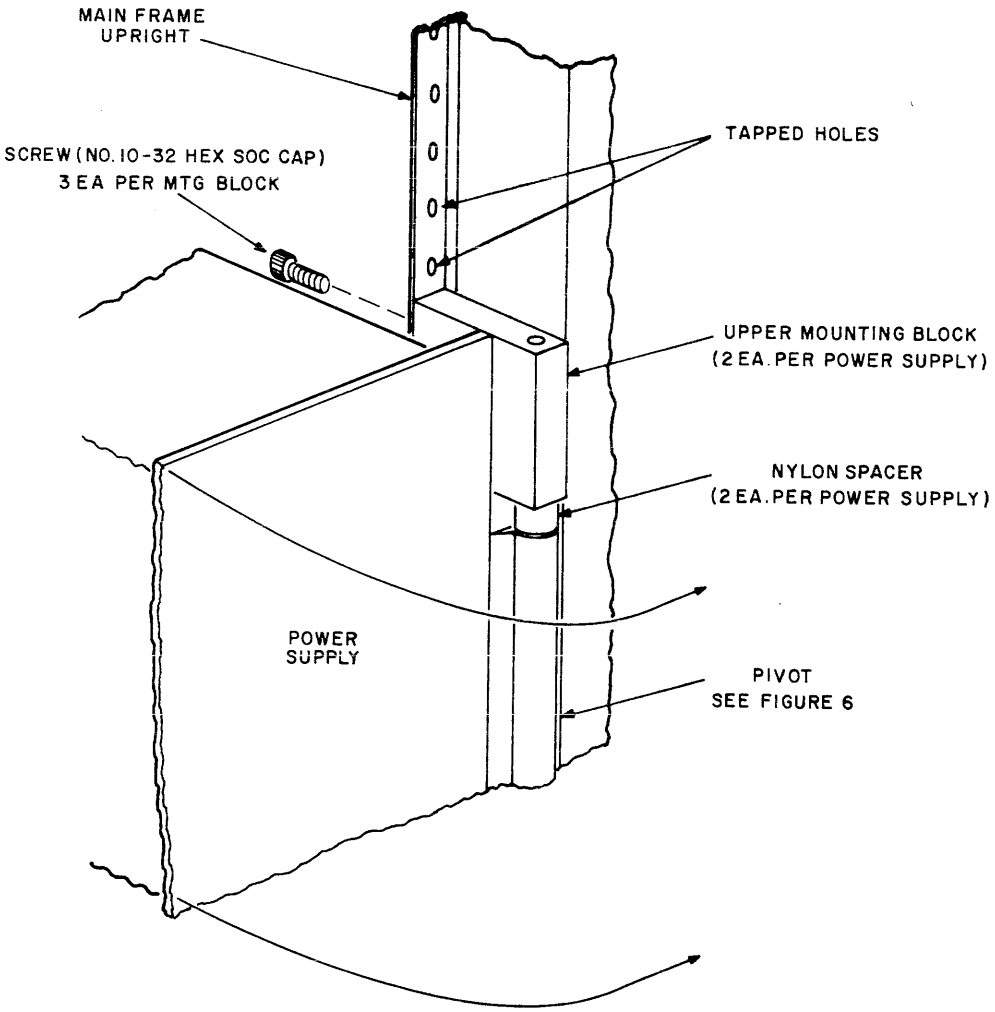

Figure 5. Power Supply Mounting

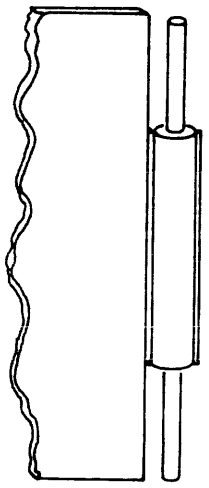

Figure 6. Power Supply Mounting Pivot

4. EXPANSION CHASSIS MOUNTING

Two Expansion Chassis (10 inch and 15 inch) are available for expanding the Model 70 Digital System. The Expansion Chassis have the same over-all dimensions as the Processor Chassis. See Section 5 on Configuration.

The Expansion Chassis slides into the rack on the two Chassis support rails (See Figures 2 and 3) from the front of the rack.

CAUTION

No chassis should be mounted in cantilever fashion. Chassis support rails MUST be used. If a rack cabinet other than an INTERDATA cabinet is used, consult rack manufacturer for proper support rails.

The chassis support rails are fastened to the mounting uprights at the front and rear of the rack. Slots are provided in the rails to allow vertical adjustment. The Expansion Chassis lock in place at the mounting uprights in front of the rack. The Expansion Chassis does not fasten in any way to the Chassis support rails. All Expansion Chassis mount below the Processor Chassis. Expansion Chassis cabling is discussed later in this document. Figure 7 shows Expansion Chassis location with respect to the filler panel and power supply.

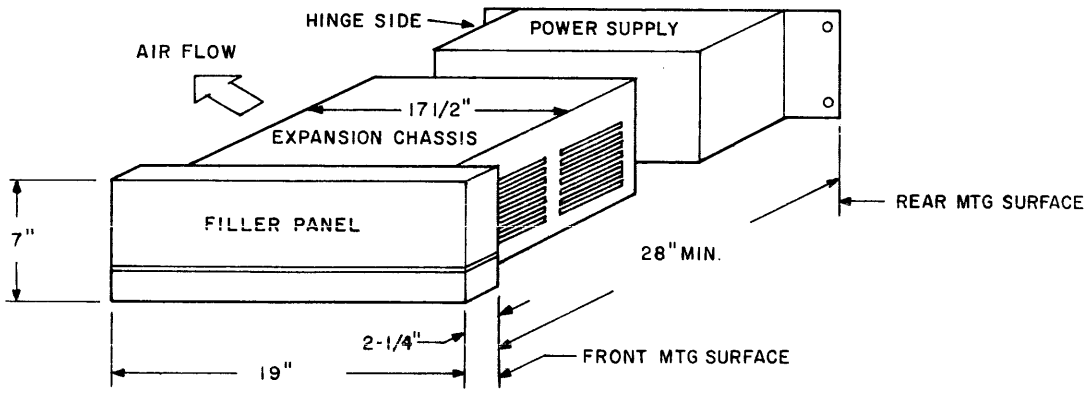

Figure 7. Expansion Chassis Location

4.1 15 Inch Expansion Chassis

The 15 inch Expansion Chassis contains eight universal expansion slots which can accept combinations of memory modules, single board peripheral controllers, system modules, selector channels, or user designed interfaces. Included with this chassis are the cooling fans and interconnecting cables. The chassis may be ordered with or without a power supply.

4.1.1 7 and 10 Inch Boards in a 15 Inch Chassis. A 10 inch I/O Controller (provided it does not use Connector 1) may be inserted in a 25 inch chassis via the 02-234 I/O Adapter Kit. (See Figure 8). One or two 7 inch boards (half boards) may be inserted into a 15" chassis via the 16-398 Half Board Adapter Kit (see Figure 9). The Half Board Adapter Kit may hold two active 7" boards or one active and one blank 7" board, depending on requirements. No wiring takes place between the boards and the adapters. The adapters are designed such that the connectors on the boards plug directly into the Expansion Chassis.

4.2 10 Inch Expansion Chassis

The 10 inch Expansion Chassis contains six 10 inch I/O expansion slots which can accept any combination of up to six wire-wrap or copper peripheral controllers, systems modules, or user designed interfaces. Included with the chassis are the cooling fan and system interconnecting cables. The Power Supply is separate. Power for this chassis is supplied by the system power supply.

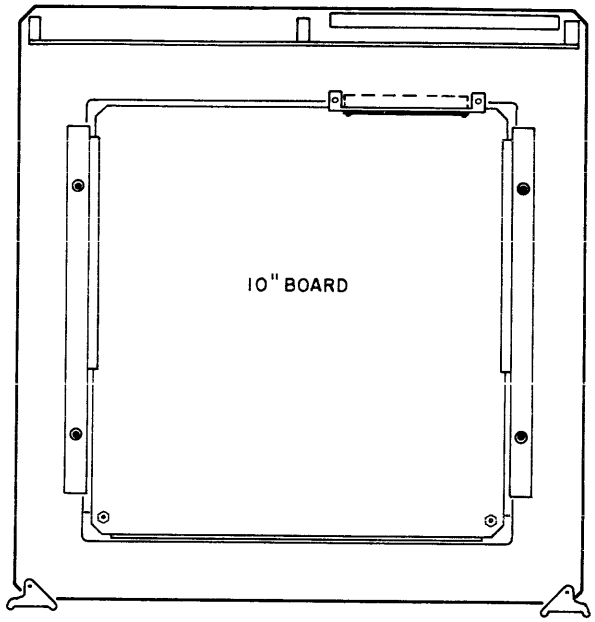

Figure 8. 02-234 I/O Adapter

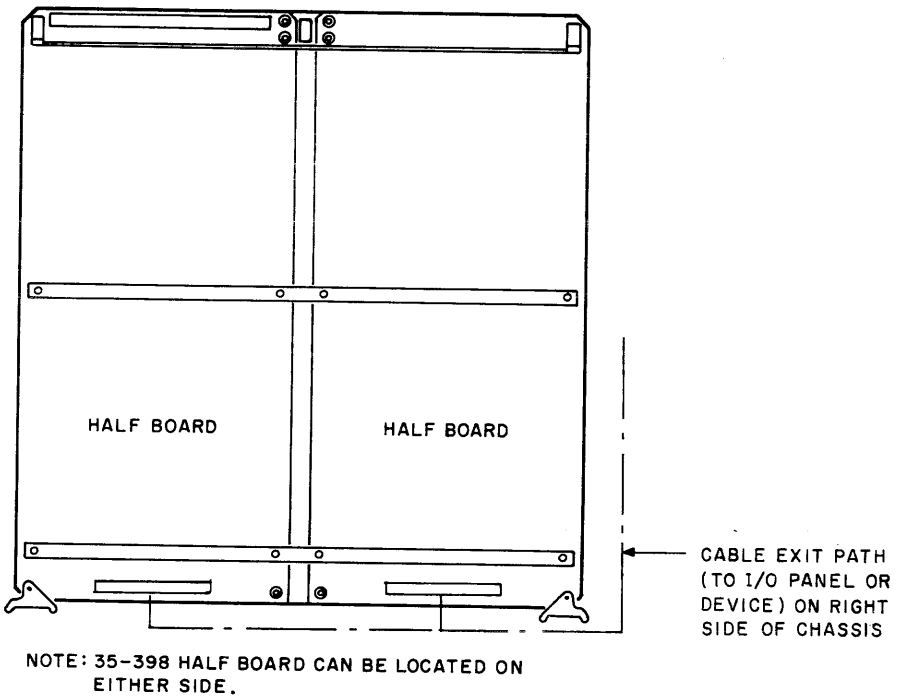

Figure 9. 16-398 Half Board Adapter

5. CONFIGURATION

5.1 System Expansion Chassis

When configuring a multi-chassis system there are four rules that must be followed:

1. The system expansion chassis must be mounted below the basic Processor chassis.
2. All chassis must be contiguous.
3. All 15 inch system expansion chassis must be mounted above the 10 inch system expansion chassis.
4. Multiboard peripheral device controllers (on 10 inch circuit boards) can only be used in the 10 inch system expansion chassis.

5.2 Circuit Board Distribution

Model 70 Digital System may be configured in a variety of ways. However, the following factors must be considered when determining circuit board distribution within the basic Processor and the system expansion chassis. See Figure 10.

1. The Selector Channel can only be placed in Slot 0 of the Processor Chassis (and Slot 2 if the system contains a maximum of 8KB core memory), or Slots 6, 4, 2, or 0 of the system expansion chassis.

2. All slots below the position where the SELCH is inserted become SELCH Bus slots. (This only applies within the chassis containing the SELCH.) The SELCH Bus extends down the left side connectors (front view). Note that all 7", and 10" with adapter, device controllers connect to the Multiplexor Bus from the right side connectors (front view). Therefore, these device controllers may be inserted in vacant SELCH Bus slots.

3. The SELCH Bus can be extended by cable to any even numbered slot in an I/O chassis adjacent to the chassis containing the SELCH controller.

4. The Universal Clock module (7" x 15") is always mounted on the right side (front view).

5. The Memory Protect module (7" x 15") is always mounted on the left side, and is normally mounted with the Universal Clock module.

6. All device addresses are hard-wired on the device controller cards, so that the distribution of I/O device controllers in the chassis normally need only be considered as a matter of convenience.

7. Slots 3, 2, 1, and 0 of the Processor chassis and all slots of the universal expansion chassis are prewired with memory module addresses for up to 64KB. It is mandatory that these slots be used for memory when, and if, required.

8. The 15 inch system expansion chassis, and the basic Processor chassis may only be used for single board I/O device controllers. For multi-board 10 inch device controllers, use the 10 inch system expansion chassis.

9. The Memory Protect module must be placed in the first available I/O slot.

NOTE

The Memory Protect Module must be placed ahead of all other I/O device controllers with respect to the device interrupt priority, including the SELCH.

10. Priority is established by the physical placement within a chassis. After the Memory Protect and the Universal Clock modules, priority for interrupt driven devices should normally be established in order of descending speed, i.e. , drum higher than magnetic tape, and card reader higher than a paper tape reader, etc.

INTERDATA Configuration Data Sheet B, Figure 10, shows an example of circuit board distribution in the basic Processor and System expansion chassis.

5.3 Back Panel Wiring

Control Line CL050 from the Processor carries the Interrupt Acknowledge (ACK) signal. This line breaks up into a series of short lines to form the "daisy-chain" priority system. The ACK signal must pass through every controller that is equipped with Interrupt Control circuits.

Back panel wiring for interrupt control at a given position is: the Received ACK (RACK0) at Pin 122-1 and the Transmitted ACK (TACK0) at Pin 222-1. The daisy-chain bus is formed by a series of isolated lines which connect Terminal 222-1 of a given position to Terminal 122-1 of the next position (lower priority). On unequipped positions, a jumper shorts 122-1 and 222-1 of the same connector to complete the bus. Back panels are wired with jumpers on all positions. Whenever a card chassis position is equipped with a controller, the jumper from 122-1 to 222-1 must be removed from the back panel at that position.

For controllers that occupy several positions, the jumper is removed only at the position where the controller board has ATN/ACK circuits. For details on the various devices (i.e. SELCH, Memory Protect Module, etc.), see the appropriate installation specification.

5.4 System Configuration

System configuration data is provided in the Model 70 User's Manual, Publication Number 29-261.

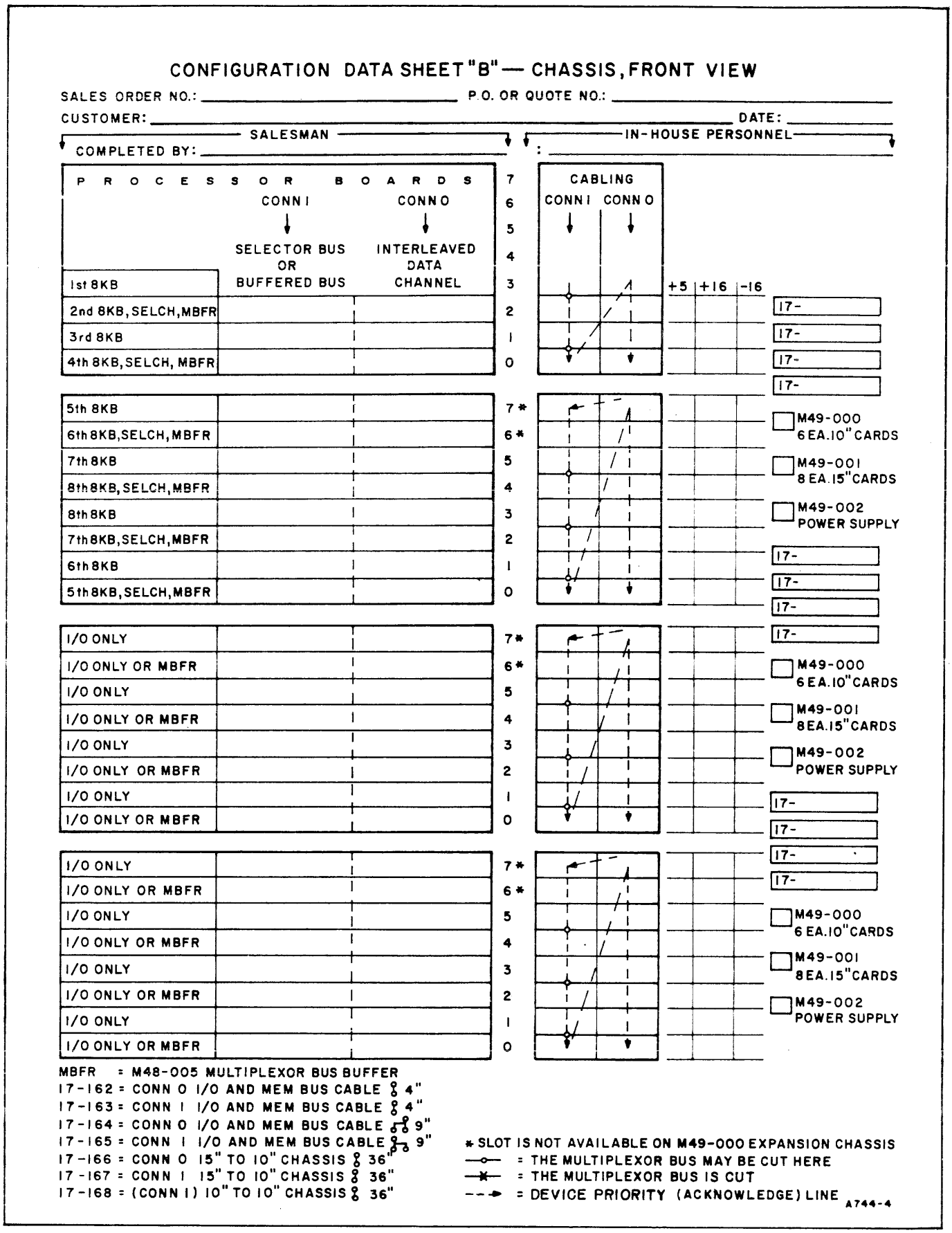

Figure 10. Configuration Data Sheet "B" (Chassis-Front View)

6. CABLES

6.1 Power Cable

The standard six foot rack is wired for 20 Amp service. On the main power cable (part of the AC Distribution Panel), the 20 Amp UL plug has one blade perpendicular to the other. A three wire, grounding, 20 Amp, 125 VAC receptacle (Hubbel #5362 or equivalent) is required to accept this plug.

6.2 Jumpers

Drawing 01-051 C12, provided in the Model 70 Maintenance Manual, Publication Number 29-266, provides the various jumper part numbers and configurations used between Power Supplies and Expansion Chassis in the Model 70. A detailed view of the terminal boards at the front and rear of the Expansion Chassis is shown in Figure 11.

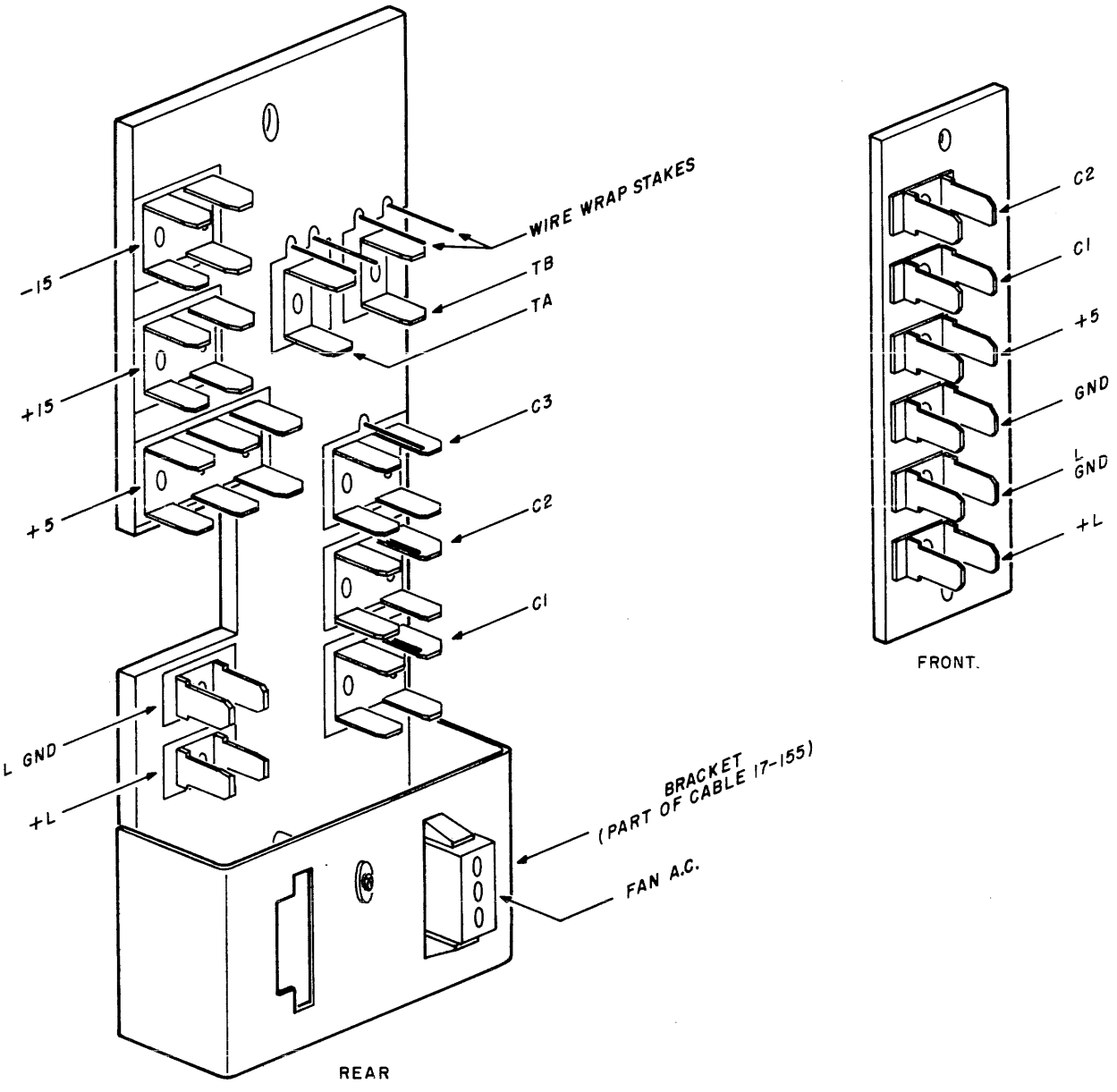

Figure 11. Terminal Boards

MODEL 70
MAINTENANCE SPECIFICATION

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MODEL 70
MAINTENANCE SPECIFICATION

1. INTRODUCTION

The INTERDATA Model 70 Digital System is a low cost, general purpose system, versatile enough to perform a wide range of industrial control, data processing, and scientific computation. The Model 70 is well suited to the real-time scanning of hundreds of instrument readings, process alarms, and pulse trains. It is particularly useful where larger amounts of main processor time are needed for computation.

This specification provides maintenance information for the Model 70 Processor. A block diagram analysis is followed by functional descriptions of major processor areas with reference to functional schematics.

2. BLOCK DIAGRAM ANALYSIS

Figure 1 is a block diagram of a Model 70 Digital System. Processor operation is controlled by the Read-Only-Memory (ROM). The micro-program in the ROM makes the Model 70 appear to have the capabilities of a much larger machine. When executing the instructions of the emulated computer, the micro-program directs the hardware to read the instruction from core memory. The hardware decodes the user's instruction and steers the micro-program to a micro-subroutine that performs the emulated instruction. When the subroutine is finished, the micro-program directs the hardware to read the next instruction from core memory, thus closing the loop.

The micro-program in the ROM consists of combinations of micro-instructions. Each micro-instruction performs a basic machine operation. Table 1 lists the 16 different micro-instructions.

TABLE 1. MICRO-INSTRUCTIONS

INSTRUCTION	OP-CODE
DO	0000
COMMAND	0001
TEST	0010
BRANCH	0011
LOAD	0100
LOAD IMMEDIATE	0101
OR	0110
OR IMMEDIATE	0111
AND	1000
AND IMMEDIATE	1001
EXCLUSIVE OR	1010
EXCLUSIVE OR IMMEDIATE	1011
ADD	1100
ADD IMMEDIATE	1101
SUBTRACT	1110
SUBTRACT IMMEDIATE	1111

The Read-Only-Memory (ROM) is a high speed, solid state, non-destructive memory used to contain the micro-program. The Model 70 micro-program occupies 1536 words of ROM. Space is provided for an additional 512 words. Micro-instruction cycle time is approximately 250 nanoseconds.

The ROM location of a micro-instruction is defined by the 12-bit address contained in the ROM Address Slave Register (RAS) and the ROM Address Lower Register (RAL). RAL is an eight-bit micro-instruction location counter. It is loaded from the S Bus during a Branch Micro-instruction, or when specified as a Destination Register. RAL increments, by one, between the execution of all other micro-instructions so that it holds the address of the next micro-instruction to be executed. RAS is a four-bit register that holds the ROM page number. It is loaded from the ROM Address Higher Register (RAH) whenever RAL is loaded from the S Bus. Neither the RAS nor the RAH is involved when the RAL is incremented.

To transfer from one page (256 ROM words) to another, the destination page number is first loaded into RAH from the S Bus. When the location address is loaded into RAL, RAS is loaded from RAH. This insures that all 12-bits of the new ROM address are sensed simultaneously.

The ROM Address Registers may also be loaded from the Decoder Read-Only-Memory (DROM). All 12-bits are loaded in parallel from the DROM read-out. RAH and RAS are loaded with the same page number.

Every micro-instruction read from ROM is placed in the ROM Data Register (RD) where it remains until the micro-instruction is executed and the next micro-instruction is read out. The output from the RD is input to the Processor control logic.

The control logic decodes the micro-instruction and activates the gating leads to the Arithmetic Logic Unit (ALU). The Source and Destination addresses are decoded, and the signals to unload registers to the B Bus and load registers from the S Bus are generated. Core memory activity and Input/Output operations are initiated in the control logic as well as the signals directing the clock system and initialize circuits.

The OP field (RD 0:3) is decoded as the operation code of the micro-instruction being executed. RD Bit-3 defines Immediate instructions. An Immediate instruction is one that has the data to be manipulated appended to the micro-instruction word itself. During the execution of an Immediate instruction or a Branch instruction RD Bits 8:15 are gated onto B Bus Bits 8:15, and treated as data.

The D Field (RD 4:7) specifies the destination of the micro-instruction result formed in the ALU. The result is placed on the S Bus by the ALU and then gated to the Destination Register specified by the D field.

The S field (RD 8:11) specifies the register to be gated to the B Bus. The selected register is the source of one operand to participate in arithmetic or logical operations. The other operand is in the A Register (AR).

The E field (RD 12:15) is an extended micro-operation modifier. This field provides control of flag actions, shifts, or I/O operations.

The Instruction Register (IR) is a 16-bit register used to hold the user instruction currently being executed. The OP field of IR (IR 0:7) holds the user's operation code. The meaning of the remaining bits depends on the type of instruction. Generally the following applies. The YD field (IR 8:11) specifies the Destination Register of the user's result. The S Bus data is gated into the General Register specified by this field. The YD field can also specify a Condition Code (CC) to match in the case of a user Branch instruction. The YS field (IR 12:15) selects the General Register to be gated to the B Bus as an operand. The IR is automatically loaded directly from core memory during the instruction fetch phase. The IR may also be loaded from the S Bus when specified as the destination in a micro-instruction. A provision is made to unload the entire IR to the B Bus or just the YD field (IR 8:11). The YD field (IR 8:11) is ANDed with the Condition Code field of PSW to assist the emulation of user's Branch instructions (MSK).

The outputs of the Instruction Register are input to Control. The user's instruction is interpreted and, through the Decoder Read-Only-Memory (DROM), the micro-program is steered to the subroutine designed to execute the user's instruction. The resulting 12-bit read-out is jammed into RAH/RAS and RAL.

The Flag Register (FLR) is a four-bit register containing the following flags: Carry (C), Overflow (V), Greater than zero (G), and Less than zero (L). These flags are modified at the conclusion of arithmetic and logical micro-operations to reflect the result of the operation. The FLR is tested by the Branch Micro-instruction. The FLR can be loaded from S Bus Bits 12:15 and unloaded to the Condition Code field of PSW.

The Program Status Word (PSW) is a 16-bit register used to define the system status relative to the user program being executed. Bits 0:11, the Status field, may be loaded from S Bus Bits 0:11. Some of the status bits have hardware significance, while others are of significance only to the emulator. Bits 12:15, the Condition Code field (CC), may be loaded from the micro Flag Register (FLR). When PSW is loaded from the S Bus, Bits 12:15 of the S Bus are captured in the FLR. PSW (12:15) remains unchanged.

The Alarm Register (ALRM) is a three-bit register containing the following flags: Parity Fail on Data Read (PFD), Parity Fail on Instruction Read (PFI), and Early Power Fail detect (EPF). The alarm bits can also be loaded into the Condition Code field of PSW.

The micro-register stack contains three general purpose registers (MR0, MR1, and MR2) and one special purpose register, the Location Counter (LOC). The Location Counter (LOC) is a 16-bit appendum to PSW holding the memory address of the next user instruction to be emulated.

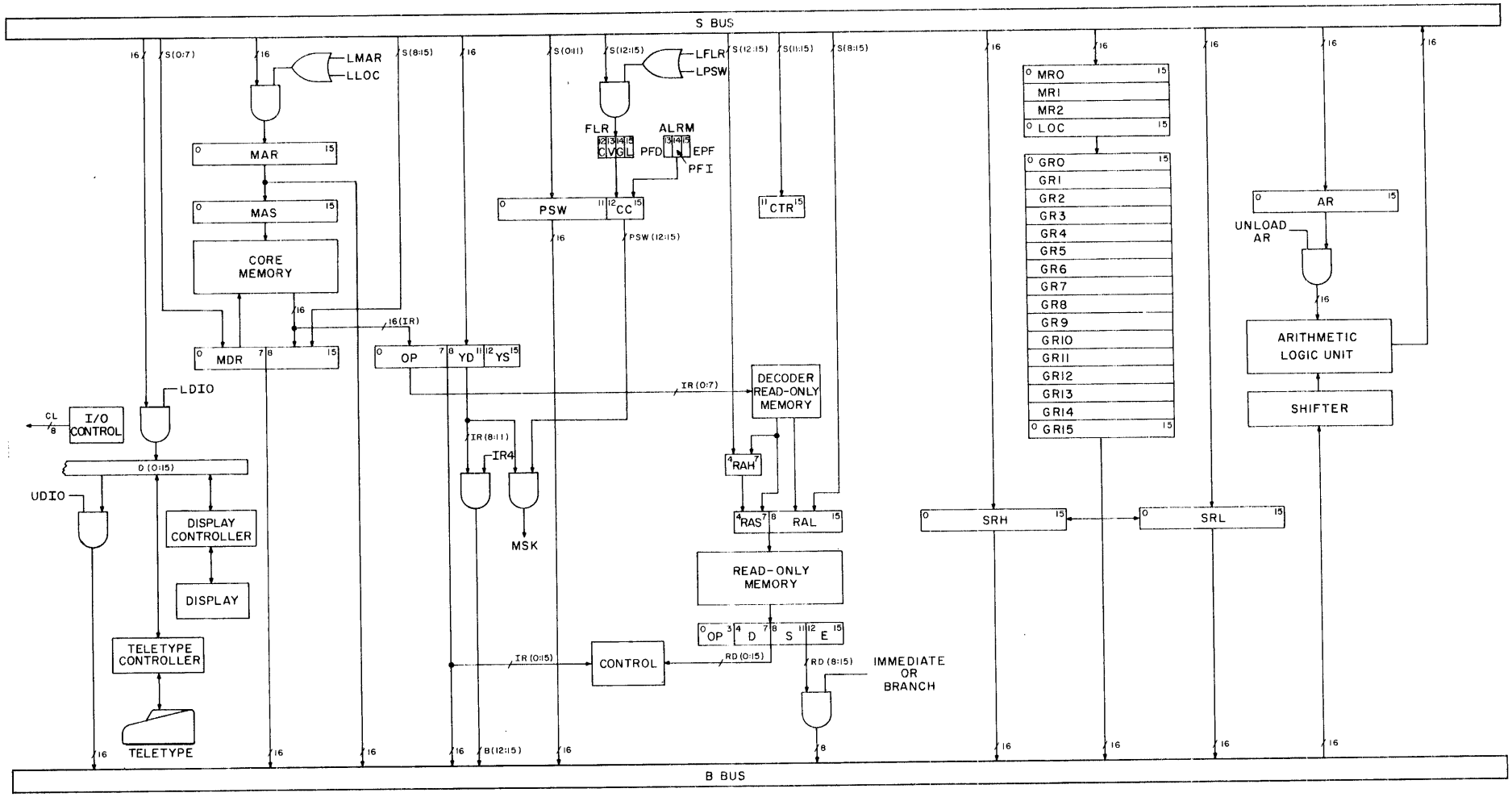


Figure 1. Model 70 Digital System

The user's register stack consists of 16 general purpose registers (GR0 through GR15). These registers are each 16-bits long and may be addressed only from the YD and YS fields of the IR. The micro-program accesses the General Register by specifying the field of IR - YD or YS - that contains the desired register address.

The Shift Registers High and Low (SRH and SRL) are two 16-bit general purpose micro-registers that can also be used in combination as a 32-bit shift register. The extended shift capability is used in multiply, divide, and other double precision operations.

The Arithmetic Logic Unit (ALU) performs the arithmetic or logical operation specified by RD. The operation executed is determined by the control lines activated when the control logic decodes the micro-instruction.

The B Bus, through the Shifter, provides one operand to the ALU. The Shifter performs Shift Left, Shift Right, Cross Shift, or direct gating of the B Bus data. The other operand is taken from the A Register (AR). The AR is a 16-bit register that can be loaded from the S Bus and input to the ALU as the second operand, if needed by the instruction being executed. The output from the ALU is the 16-bit S Bus.

The Counter (CTR) is a five-bit decrementing register used on multiply, divide, and repeat operations, and on the Branch on Counter Micro-instruction. The Counter is initialized to a count of 16; however, it may be pre-loaded with any value from 0 to 31 from the S Bus Bits 11:15.

The core memory is the source of user instructions and data constants. It contains 4K to 32K 16-bit locations. Memory operations are initiated by the control logic during a DO or Command Micro-instruction or by Direct Memory Access devices. For Processor initiated memory operations, the location selected in core memory is designated by the 16-bit Memory Address Slave Register (MAS). MAS is updated from the 16-bit outer-rank Memory Address Register (MAR) whenever a memory operation is not in progress. MAR may be loaded from the S Bus at any time and unloaded to the B Bus. Whenever the Location Counter (LOC) is loaded from the S Bus, MAR is also loaded with the same data. The 16-bits read-out or written into the addressed memory location are buffered in the Memory Data Register (MDR). MDR is separated into two eight-bit halves which may be loaded simultaneously or individually from the S Bus.

The memory timing signals are generated in the Processor. The Processor also resolves memory usage conflicts, handling external and internal requests for memory access. If the Processor attempts to unload MDR when memory data is not yet available, or load the MDR, or initiate another memory cycle when memory is still busy from the previous access, the Processor waits until memory data is available or the currect access is completed. Non-memory oriented operations may be interleaved with memory operations for maximum efficiency.

The Processor controls the multiplexed I/O Bus by directing device controllers to load data onto the D Bus or to accept data from the D Bus. The D Bus is a 16-bit bi-directional bus that can receive data from the S Bus or present data to the B Bus. The nature of the data on the D Bus is determined by the particular control line that has been activated.

The device controllers for the Control Console and the ASR 33 or 35 Teletype are built into the Model 70 Processor.

3. FUNCTIONAL DESCRIPTIONS

This section describes the major functional areas of the Processor. The descriptions reference both simplified drawings provided in this section, and the Processor Functional Schematic, 01-051D08.

3.1 Clock Control

The clock generator is shown on Sheet 19 and is located on the 35-390 I/O mother-board. The clock system employs a free-running 16MHz oscillator. The sinusiodal oscillator output (19C6) is ORed with the normally high External Clock (EXTCLK0)(19E6) producing OSC1 (19C7). The EXTCLK0 lead is provided so that an external clock may be used to run the system during troubleshooting. This is accomplished by grounding the CLKOFF0 lead to Pin 133-1 on the back panel to disable the internal oscillator, and then pulsing the EXTCLK0 lead. The external oscillator used should meet the following specifications:

1. Logic levels 0 to +0.45VDC for logic Zero.
   +2.6 to +5 VDC for logic One.

2. Square wave output, frequency up to 16 MHz.

3. Output drive = 7 milliamperes.

The Oscillator output (OSC1) is connected to the T input of the GO flip-flop (19C8). The K input to the GO flip-flop is tied to CLKSTP1 (19C5). When the system is initialized, CLKSTP1 goes high. The GO flip-flop toggles reset and SYSCL1 (19G5) is inhibited until the initialize sequence is terminated. At this time, CLKSTP1 goes low and shortly thereafter CLKSTP0 on the J input goes high. The GO flip-flop sets on the next negative going transition of OSC1, enabling SYSCL1.

The oscillator is adjustable (via the variable Capacitor, C9) over the range of 50 to 110 nanoseconds. The oscillator is nominally adjusted for a period of 62.5 nanoseconds, and may be monitored at Test Point E during troubleshooting.

The negative going transitions of SYSCL1 step the two-stage clock counter, TFA and TFB (19G7,8). The system clocks are produced by decoding particular states of the clock counter. The system clocks occur every 250 nanoseconds and have a fixed pulse width of 62.5 nanoseconds, the period of SYSCL1. Figure 2 shows the clock sequencing.

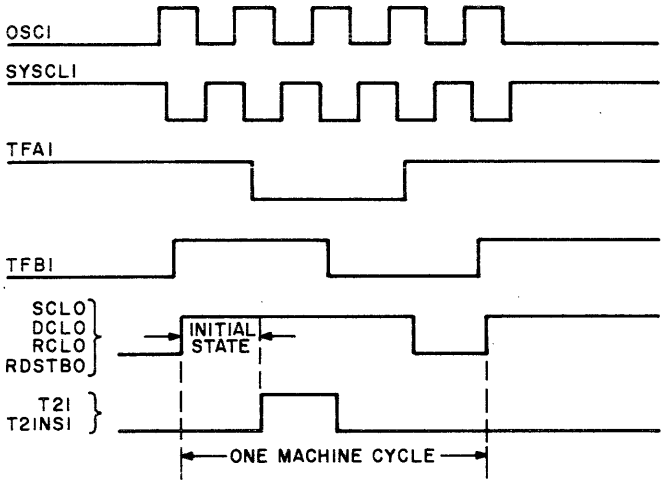


Figure 2. Clock Sequence

The initialize state of the clock counter is TFA and TFB set. This state is not decoded and no clocks are active. On the next negative transition of SYSCL1, TFA resets. This state (TFA reset, TFB set) is decoded to produce T21 and T21NS1 (19K9). T21 is inhibited (skipped) when the signal STPA0 (19J5) is low; T21NS1 is never skipped. T21 and T21NS1 occur in the middle of a machine cycle. These clocks are used when multiple operations have to be completed within one machine cycle. On the next negative transition of SYSCL1, TFB resets. This state (TFA reset, TFB reset) is not decoded and no clocks are active. On the next negative transition of SYSCL1, TFA sets. This state (TFA set, TFB reset) is decoded to produce RDSTB0, RCL0, DCL0, and SCL0.

ROM Data Strobe (RDSTB0)(19L9) is used to strobe data from the ROM into RD. RDSTB0 is skipped whenever any of the following signals are active: STPA0, DST0, STOP0, STPC0, or LRAL0.

ROM Clock (RCL0)(19L9) is used to load the ROM address registers and increment RAL. RCL0 is skipped whenever any of the following signals are active: STPA0, DST0, STOP0, or STPC0.

Destination Clock (DCL0)(19M9) is used primarily to gate data into the Processor registers. DCL0 is skipped whenever any of the following signals are active: STPA0, DST0, LRAL0, or KILDST0.

System Clock (SCL0)(19J9) is an uninhibited clock. The basic machine cycle is defined as the interval between the trailing edges of two consecutive System Clocks (SCL0).

After SCL0, the clock counter returns to the initial state, TFA and TFB set.

It is necessary to prevent the generation of certain timing functions at specific times. To achieve this, a hierarchy of clock inhibits is implemented. This network of clock stops can be divided into three categories:

1. Initialize - All clocks are stopped.

2. Asynchronous to synchronous timing conflicts - This category includes memory oriented operations and Input/Output operations.

3. Extended cycle operations - This category includes Branches and Loads to the RAL which require an extra clock period to allow the new ROM address to be accessed; the Commands Multiply, Divide, and Repeat, and the user instruction access activities carried on in a DO Micro-instruction.

When a memory oriented operation is attempted and memory is not ready, STPA0 goes low, disabling RDSTB0, RCL0, DCL0, and T21.

STPA0 is generated at 4K4 and is located on the 35-388 ROM mother-board. If an attempt is made to unload the MDR (UMDR1)(18C4) when memory data is not available (FMDUA1)(30J4), STPA0 goes low, stopping the Processor until memory data is available. If an attempt is made to load the MDR (LMDR1)(8F8) when the Memory Data Register is being used for the re-write cycle of memory (FMDBY0)(30R4), STPA0 goes low until the memory has finished with the MDR. If an attempt is made to start memory while memory is busy (FPMBY1)(30S8), MSST0 (4K2) goes low, generating STPA0 to stop the Processor until memory becomes un-busy. Note that MSST0 is not active if the Processor is in Phase Zero (P00)(4L1).

When an I/O Load Micro-instruction is performed, DST0 (4A4) goes low, disabling RDSTB0, RCL0, and DCL0. DST0 is generated at 4A4 and is located on the ROM mother-board.

The DST flip-flop (4A4) toggles set on the trailing edge of the first T21 in the Load Micro-instruction (GIO1 true), producing DST0. The DST flip-flop remains set until a Sync is returned from the device (SYNCH1)(4E3) or a false Sync time-out is generated. An I/O Load Micro-instruction takes a minimum of two system clocks.

The Skip flip-flop (18J8) provides the capability of skipping one clock period while performing a Branch or Load RAL Micro-instruction. The J input to the Skip flip-flop is normally low and goes high when clock cycles are to be skipped. The J input is fed by two NAND gates whose outputs are tied together. During a Branch instruction, if the branch is to be taken, GOBRA0 (18H8) is low, forcing both NAND gate outputs high. During a Load RAL instruction, LD10 (18F9) is low, forcing one NAND gate output high (18J7). On a DO Micro-instruction, if the Processor is in Phase Zero of a non-RR instruction, SSKIP0 (18K6) is low, forcing the outputs from both NAND gates high. SSKIP0 is generated at 9B8. The high present on the J input to the Skip flip-flop is ANDed with its reset output (18K9) and SSKIP0 to produce LRAL0 (18K9). (LRAL0 is not active if Skip is being used by the Phase Zero DO.)

LRAL0 inhibits RDSTB0 and DCL0 (19L5) for one clock interval, until the Skip flip-flop toggles set. Note that RCL0 has not been inhibited. The S Bus data is toggled into the RAL on the trailing edge of RCL0. At the same time, the Skip flip-flop toggles set and LRAL0 goes false. RDSTB0 and DCL0 are re-enabled. On the next system clock, the Skip flip-flop will toggle reset because of LD10 or GOBRA0. If Skip is being used by the Phase Zero DO, KSKIP0 (18J5) goes low when memory becomes un-busy. KSKIP0 is generated at 9F9. The DO Micro-instruction will be described later.

Referring again to Sheet 19, STOP0 (19L5) is active during Phase Zero of a DO Micro-instruction. STOP0 low inhibits RDSTB0 and RCL0.

STOP0 is generated at 9B4. STOP0 is low, if the micro-program is executing a DO Micro-instruction with phase change specified (DRD081) and is currently in Phase Two or Three (PC01) with no interrupts pending (DTEST0), or if in Phase Zero (P01A) and memory data is not yet available (FMDUA1), or if in Phase Zero (P01A) of a non-RR user instruction (RR0) and memory is still busy (FPMBY1). STOP0 prevents the strobing of a new ROM word (RDSTB0 false) or the incrementing of the RAL (RCL0 false) until the Processor is ready to leave Phase Zero.

The KILDST0 signal (19M5) is active if a Command Repeat is attempted when the Counter Register is equal to zero. KILDST0 stops DCL0 so that no Destination Register is loaded and the FLR is not changed. The attempted instruction is effectively skipped. KILDST0 is also low during a Phase Two Abort. See 3.9.2.

The STPC0 signal (19L5) is active during the Commands Multiply, Divide, and Repeat until the Counter Register decrements to one or zero. STPC0 inhibits RCL0 and RDSTB0 so that the same micro-instruction remains in RD for as many machine cycles as required to complete it.

3.2 Initialize Control

The Initialize Control logic is shown on Sheet 19. This logic provides an orderly system shutdown when Initialize occurs. The following actions take place on initialization:

1. Stop clocks
2. Preset Clock Counter (TFA, TFB)
3. Clear RAH, RAS, RAL
4. Clear RD
5. Clear FLR
6. Clear ALRM
7. Preset CNTR to 16
8. Set Phase Counter to Phase Three
9. Clear BANK and UTILITY flip-flops
10. Clear RUN, CMODE, and RPT flip-flops
11. Reset I/O Control (DST, LINE)
12. Reset Memory Control
13. Provide reset signal to Multiplexor Bus.

The system is initialized as a result of one of the following conditions:

1. Command Power Down (POW)
2. AC input (with optional power fail detector) falls below minimum operating level.

The master reset signal (SCLR0)(19N1) is active when the Initialize Relay K1 (19M2) is de-energized. This happens when the POWDN0 signal (19F1) is active. During normal operating conditions, POWDN0 is high, allowing the Darlington circuit to conduct (Q5 and Q6). As long as the Darlington circuit conducts, the Initialize Relay K1 remains energized.

POWDN0 goes low if the STPSYS flip-flop sets (19J4), or if one of the voltages; +5 volts, +15 volts, -15 volts, or the AC input is lost.

The STPSYS flip-flop (19J4) is direct set if a Command Power Down (POW) is executed, or it toggles set one millisecond after Primary Power Fail (PPF) is detected. PPF0 (19H5) is true one millisecond after the key-operated power switch is turned off (POFF0)(19A4), if the Control Console Initialize switch is depressed (INIT0)(19A4), or if the optional Primary Power Fail Detector determines that the AC voltage is too low (PFDT0)(19C3).

If one of the three above mentioned items occur, the one millisecond delay at 19G2 is set. The negative transition of the zero (0) side toggles the Early Power Fail flip-flop set (EPF)(17S7). If PSW02 is set, Alarm Register Bit-15 sets, generating a Machine Malfunction Interrupt (MALF1). As soon as ALRM15 flip-flop sets, the EPF flip-flop is cleared. The Processor tests for MALF between the execution of each user instruction. In response to the Machine Malfunction Interrupt, the user has an opportunity to do any necessary system resetting.

After the initial one millisecond delay, the negative transition of the one (1) side of the EPF delay toggles the Primary Power Fail flip-flop set (PPF)(19J3). This starts the other one millisecond delay at 19G4. If this delay times out before the micro-program executes a Command Power Down, the STPSYS flip-flop toggles set (19J4). The Processor tests for PPF between the execution of each user instruction. When PPF is detected, the micro-program stores the PSW, LOC, and General Registers in core and executes a Command Power Down (POW), setting the STPSYS flip-flop and clearing the second one-millisecond delay. When STPSYS1 goes high, the POWDN0 lead goes low, de-energizing the Initialize Relay K1. STPSYS0 active causes CLKSTP1 (19N5) to go high. The GO flip-flop toggles reset (19D9), stopping the system clocks.

The second instance when POWDN0 goes low is when one of the voltages is lost. If the N15 (-15VDC) supply voltage is lost (19J1), the output from the NAND gate at 19J1 goes low. If the P15 (+15VDC) supply voltage is lost (19D1), the POWDN0 lead becomes effectively open as Transistor Q4 is normally off. If the P5 (+5VDC) is lost, the collector supply for the Darlington circuit is removed (19L2), causing the Initialize Relay K1 to de-energize. If the AC input is lost, the POWDN0 lead is also forced low. The AC input is sampled from the secondary of a 12VAC transformer and rectified. The pulsating DC voltage is applied to Potentiometer R60 (19B1). The potential selected by the potentiometer is applied to the optional Power Fail Detector.

Initially, Transistors Q2, Q3, and Q4 are off and Transistor Q1 is conducting. With Transistor Q1 conducting, a high enough potential on the base of Q4 keeps Q4 cut off, and applies about +6 volts to the emitter of Q2. The potential from Potentiometer R60 (approximately 8 volts) is felt on the base of Q2. If the AC input is lost, or fluctuates enough, the potential on the base of Q2 becomes more negative and Q2 conducts.

When Q2 conducts, it places a positive potential on the base of Q3, turning Q3 on. This causes the potential on the emitter of Q1 (by way of Q2) to become less positive, turning Q1 off. When Q3 conducts, its collector goes to ground, generating the low signal, PFDT0 (19D3).

When Transistor Q1 turns off, the positive potential is removed from the base of Q4. Transistor Q4 conducts, grounding the POWDN0 lead, turning the Darlington circuit off, and de-energizing the Initialize Relay K1. (The Initialize Relay K1, which is a dry reed relay with Single Pole Double Throw contacts, is shown de-energized.) When the relay de-energizes, the SCLR0 contact is grounded. This metallic ground is distributed to the memory and I/O boards for initialize control. SCLR0 also holds CLKSTP1 active, keeping the clocks off.

SCLR0 is inverted through the gate at 19N2. The output SCLR1A rises to +5 volts and generates SCLR0A (19H5) and SCLR0B (19R5) for use on the I/O board. SCLR1A (19R1) is also distributed on the back panel for use by the other Processor boards.

SCLR0A holds CLKSTP1 active and also clears the STPSYS flip-flop. Resetting the STPSYS flip-flop removes the ground from the POWDN0 line. The two 33mfd capacitors (C1 and C2) charge slowly (19K3). When the threshold of the input Transistor Q5 of the Darlington circuit is reached, the circuit conducts and the Initialize Relay K1 is energized.

The SCLR0 contact opens and SCLR1A goes to ground. SCLR0B goes high, removing the direct set signal on the Timer flip-flops (TFA and TFB) and the direct clear signal on the GO flip-flop. SCLR0A goes high allowing CLKSTP1 and the K input to the GO flip-flop to go low. The J input (CLKSTP0) is delayed by the 2.2mfd capacitor (19R5) to ensure that the clocks do not start until all initialize activity is completed.

In the case where Initialize is caused by a failure of P5, N15, P15, or the AC supply, the Initialize Relay K1 de-energizes and remains in that state until the fault is corrected.

3.3 Read-Only-Memory

The Read-Only-Memory (ROM) is a high-speed, solid-state, non-destructive memory used to hold the micro-program. The ROM is organized into pages of 256 16-bit words. Each page of ROM contains four integrated circuit (IC) packages arranged such that each integrated circuit holds four-bits of every word on the associated page.

The Model 70 micro-program is complete in six ROM pages, 24 ROM integrated circuits. Three additional ROM integrated circuits comprise the Decoder ROM (DROM). Space is provided on the ROM mother-board for an additional two pages of ROM.

Each ROM integrated circuit has two enable leads. Both enables have to be low before a read-out is obtained. If the enables are false, the four data output leads are high. Address decoding is done internal to the IC.

3.3.1 ROM Address Lower (RAL). The ROM Address Lower Register (RAL) is an eight-bit register that selects one of 256 addresses in a Read-Only-Memory page. RAL is shown of sheet 5.

During the performance of the major portion of the micro-program, micro-instructions are selected from successive locations in the ROM. RAL is consequentially designed as a standard up-counter. The RAL is incremented as each new micro-instruction is read from ROM. During a Branch Micro-instruction with the specified condition true, or if the RAL is specified as the Destination Register, the RAL increment signal is disabled and the new address is loaded from the S Bus.

RAL is direct cleared by System Clear (SCLR0)(5A1) when the system is initialized, or conditionally on a DO Micro-instruction by RACLR0 (5A1). The ROM Clock (RCL0)(5K1) is used to increment RAL or to gate the S Bus data into the RAL. If a Branch or a Load RAL instruction is performed, LRAL0 (5R2) is low and LRAL1 (5N4) is high. LRAL1 is NANDed with each bit of the S Bus (8:15) to set up the J and K inputs to each RAL flip-flop. LRAL0 low causes the two 19-040 four-bit carry networks to pass RCL1 to the toggles of RAL 09 through 14. RCL1 is always present on RAL15 and is gated to RAL08 by LRAL1. On the trailing edge of RCL0, the S Bus data is copied into RAL.

When the Processor is not executing a Branch or a Load RAL, LRAL0 is high and LRAL1 is low. LRAL1 low causes both the J and K inputs to each RAL flip-flop to be high. If a flip-flop receives a toggle, it will complement. A flip-flop is given a toggle pulse if all previous flip-flops are set. RAL15 will complement on the trailing edge of every RCL0. The 19-040 four-bit carry network (A66)(5R7) toggles RAL14 if RAL15 is set. RAL13 toggles if RAL14 and RAL15 are both set, etc. The signal PF0, low if RAL 12 through 15 are set, enables the second 19-040 four-bit carry network (A47)(5M7) which supplies the toggles for RAL09, RAL10, and RAL11. The toggle for RAL08 is generated separately if the PF0 lead from the 19-040 four-bit carry network (A47)(5M7) is low, indicating that RAL09 through 15 are all set.

When the DO Micro-instruction generates a new ROM address, the ROM Address Registers are first cleared, then the new address is loaded. The DO instruction generates RACLR0 (9B9), a 30 nanosecond pulse occurring during T2. RACLR0 clears RAH, RAS, and RAL. During the same T2, a 60 nanosecond pulse is applied to the direct set input of the appropriate ROM Address Register bits. The set pulse remains active for a short time after the clear pulse has passed.

3.3.2 ROM Address Higher (RAH). The ROM Address Higher Register (RAH) is shown on Sheet 5. RAH is a four-bit extension of the RAL which increases the ROM addressing capability to 4096 locations. RAH is independent of the RAL from both the programming and hardware viewpoint. When RAL is incremented from its highest value (hexadecimal 'FF'), it recycles to zero, but no carry is propagated into RAH. Consequently, the RAH must be loaded independently each time a Branch or Load RAL selects a different page.

A new page address is loaded into RAH at the trailing edge of RCL0 when the RAH is specified as the Destination Register (LRAH0 low)(5K1). RAH is cleared by SCLR0 (5A1) on Initialize or by RACLR0 on a DO Micro-instruction. Both the RAH and RAS receive the same page number when the DO instruction generates a new ROM address.

3.3.3 ROM Address Slave (RAS). The ROM Address Slave Register (RAS) is slaved to the four-bit RAH. The outputs from RAS select the page of ROM to be accessed.

The contents of RAH are loaded into RAS every time RAL is loaded from the S Bus. This allows the proper page number to be established in RAH in advance of a Branch or Load RAL.

The RAS is cleared by SCLR0 on Initialize or by the RACLR0 signal on a DO instruction. Note that RAH04 and RAS04 are cleared separately from the remaining bits of RAH, RAS, and RAL. Bit-4 of RAH and RAS is unconditionally held clear when PSW Bit-7 is reset. The only time that ROM Pages 8 and above can be specified is when PSW Bit-7 is set. Since Pages 8 and above physically do not exist, the illegal condition will be forced upon access. The connection between ROM address Bit-4 and PSW07 will be explained later in Section 3.4.

3.3.4 ROM Addressing Logic. Pages 0 through 3 of the ROM are shown on Sheet 6 and Pages 4 through 7 are shown on Sheet 7. One enable lead to the 16 ROM integrated circuits on Sheet 6 is RAH051. If RAH specifies Page 0, 1, 2, or 3, RAH051 is low, enabling the 16 devices on Sheet 6. If RAH specifies Page 4, 5, or 7, RAH050 is low, enabling the 16 devices on Sheet 7. One ROM page (four devices) out of the four pages enabled by RAH05 is selected by decoding RAH06 and RAH07. The signal EN000 is low if Page 0 or 4 is selected. EN010 is low if Page 1 or 5 is selected. Page 2 or 6 selected causes EN100 to go low. Page 3 or 7 causes EN110 to go low. The combination of an ENXX0 lead and RAH05X causes 4 ROM integrated circuits, out of 32 possible, to be enabled. The enabled devices each gate four-bits of data onto the high active SRDXX1 leads.

The address decoding of a word within a page is done internal to the ROM integrated circuits. The address selected is specified in RAL. Page 0, 1, 2, and 3 devices are addressed by the one (1) side of the RAL flip-flops and Page 4, 5, 6, and 7 devices are addressed by the zero (0) side of the RAL flip-flops. This is done for fan-out reasons.

The SRDXX1 leads are tied to the J inputs of the ROM Data Register (RD) flip-flops and inverted onto the K inputs (Sheet 8). At clock time, the ROM data is toggled into RD.

3.3.5 ROM Data Register (RD). The ROM Data Register (RD) is a 16-bit register shown on Sheet 8. The RD can be thought of as the micro instruction register. Each bit of the RD has a single-rail input from the ROM array. Each micro-instruction read from ROM is clocked into RD, where it remains while the instruction is executed.

Bits 0:3 of RD hold the Op-Code of the micro-instruction being executed. If the instruction is not a command, RD Bit-3 set means the instruction is Immediate. The data to be used as the first operand is contained in Bits 8 through 15 of the instruction. During an Immediate instruction, RD 8:15 are gated onto the B Bus Bits 8:15.

Bits 4:7 of RD are decoded as the Destination Register address for all micro-instructions except DO, Command, Test, and Branch. This identifies the register that will contain the result upon completion of the micro-instruction. If the micro-instruction is a DO, Command, or Test, Bits 4:15 of RD are the function code. If the instruction is a Branch, RD 4:7 defines the condition that the Processor will branch on.

Bits 8:11 of RD are decoded as the Source Register address for micro-instructions in the Register-to-Register format. The Source Register contains the first operand for the micro-operation.

Bits 12:15 of RD make up the Extended operation field for Register-to-Register Micro-instructions. The Extended field controls shifting, flags, I/O operations, or whether to enable the A Register input to the ALU.

The RD is cleared by SCLR0 on Initialize or when a Privileged instruction is addressed and the Processor has PSW Bit-7 enabled.

3.4 Decoder Read-Only-Memory

The Decoder Read-Only-Memory (DROM) consists of the three ROM integrated circuits shown on Sheet 4. Each IC contains 256 four-bit words. The Read-Only-Memories are addressed in parallel by Bits 0:7 from the Instruction Register (IR). The high active DROM read-out is gated onto the SRAXX0 leads by the GDROM0 signal (4A5) that occurs at T21 before the Processor enters Phase Two. The ROM Address Registers are direct cleared prior to or at the same T21. The DROM data is the starting address in ROM of a Phase Two micro-subroutine.

DROM read-out Bit-4 is active only on the privileged user instructions. A Privileged instruction may only be executed if PSW Bit-7 is reset. PSW071 (5A1) on the DC clear input to RAH04 (5C3) keeps RAH04 from setting if PSW07 is reset. If PSW07 is set, RAH04 is allowed to set from the DROM output. If a Privileged instruction is in the IR, RAH04 sets and the illegal address condition exists. The gates at 8A2 will cause the RD to clear on the next RDSTB0 and the illegal condition will occur. Privileged instructions that are attempted when PSW07 is set, are treated as illegal.

3.5 Processor Registers

The Processor executes micro-instructions received from the ROM. The majority of micro-instructions move data from one register to another and modify it in the ALU. Most of the Processor registers are 16-bit registers. Some of these registers perform special functions, but the majority are general purpose. Data is transferred between registers and other system elements by way of the 16-bit B and S Buses in the Processor. Each register is described in the following paragraphs.

3.5.1 Flag Register (FLR). The Flag Register (FLR)(Sheet 17) is a four-bit register located on the 35-390 I/O mother-board. The FLR is direct cleared by the SCLR0A signal (17D5). The FLR is loaded from the S bus when the FLR (address '4') or the PSW (address '2') is specified as the destination. Destination address '4' causes LFLR0 (17S1) to be active. Destination address '2' causes LPSW1 to be active (17S1). LFLR0 is generated on the 35-388 ROM mother-board at 8D9. LPSW1 is inverted and NANDed with LFLR0, producing LDFLR1 (17K2). LDFLR1 is NANDed with S Bus Bits 12 through 15. If any bit of the S Bus is true, SFLRXX0 on the K input to the corresponding bit in the FLR goes low and the J input goes high, allowing the corresponding flip-flop to toggle set on the trailing edge of the next Destination Clock (DCL0)(17A1). If the S Bus bit is false, the K input is high and the J input is low, and the flip-flop toggles reset.

Since the FLR is used to hold flags indicative of the result of micro-instructions, there are instances when individual bits will be changed independently. To facilitate this, different toggle leads are developed for the different bits.

LDFLR0 is inverted and ANDed with the CLR0 signal (17R1) producing LDCLR0 (17M4). CLR0 is active, when specified, during a DO Micro-instruction. CLR0 is generated on the ROM board at 9N4. If the Processor is executing a DO Micro-instruction, D1 is high (8D5). If the Processor is not in Phase Zero (P00) and no memory clock stop is in effect (MSST0), CLR0 is allowed to go low. MSST0 assures that CLR0 only occurs during the last clock interval of a DO Micro-instruction. CLR0 is forced low when the new phase is to be Phase Three (GTP30). LDCLR0 allows all the FLR bits to change.

The toggle lead for FLR Bits 14 and 15 is developed by the two NAND gates collector AND tied at 17R4. The input to one gate is the Destination Clock (DCL0) and one input to the other gate is LDCLR0. The toggle for Bits 12 and 13 is the ungated DCL1. The gating for these bits is done individually on the J and K inputs.

FLR Bit-12 is used as the Carry Save flip-flop (C)(17E5). FLR12 is set or reset to reflect whether or not a carry or borrow resulted from an Add or Subtract Micro-instruction, or to reflect the state of the bit shifted out during a Load Micro-instruction. FLR12 is allowed to change state when LDCLR0, SVSC0, or SVAC0 is active. If none of the gating leads are active, the J and K inputs are held at ground.

SVSC0 is generated in two places with an OR tie across the back panel. The first source is on the ROM board at 8S9. SVSC0 goes low if the Processor is executing a Load Micro-instruction (LOAD1) other than I/O (LDIO0·UDIO0) and RD Bit-15 is set (RD151), specifying Carry Out. The second source of SVSC0 is on the ALU board at 13A4. SVSC0 is active during a Command Shift Left (CSL0) or a Command Shift Right (CSR0) other than during a Multiply (MPY0) if RD Bit-15 is set (RD151), specifying Carry Out.

SVAC0 is also generated in two places with an OR tie across the back panel. The first source is on the ROM board at 8S9. SVAC0 is active during a non-immediate (RD030) AND, OR, Exclusive OR, Add, or Subtract Micro-instruction (RD001+RD011·RD021) if RD Bit-15 is set (RD151), specifying Carry Out. The second source of SVAC0 is on the ALU board at 13B4. SVAC0 is low during a Command Multiply Micro-instruction (MPY1) if RD15 is set (RD151), specifying Carry Out.

FLR12 is set when SFLR120 is low. SFLR120 is generated by four NAND gates collector OR tied. The input to the first NAND gate is SHOT1 (17C1), generated on the ALU board (13C9). SHOT1 goes high when the Processor is executing a Shift Right (SHR1) and B Bus Bit-15 is active (B150), or a Shift Left (SHL1) and B Bus Bit-0 is active (B000), or a Command Shift Right (CSR1) other than on Multiply (MPY0) and Shift Register Lower Bit-15 is set (SRL151), or Command Shift Left (CSL1) and Shift Register Higher Bit-0 is set (SRH001).

The second NAND gate is enabled by SVAC1 (17D3). The Carry Output from the ALU (CSV1) is Exclusive ORed with Subtract (SUB1) and applied as the second input. The third input to the NAND gate at 17D3 is the Exclusive-NOR of RD000 and RD010 and is high when RD000 and RD010 are alike. The only time that RD000 and RD010 are alike when SVAC1 is high, is during an Add, Subtract, or Command Micro-instruction. The meaning of CSV1 from the ALU differs depending on whether an Add or Subtract Micro-instruction is performed. The Exclusive OR of CSV1 and SUB1 inverts the ALU Carry on a Subtract Micro-instruction.

The third NAND gate (17C2), enabled by LDFLR1, has a low output when S Bus Bit-12 (S121) is active. The fourth NAND gate is the master enable for the K input to FLR12. SFLR120 is inverted and the J input is allowed to go high. FLR12 toggles set on the trailing edge of the next Destination Clock (DCL1).

FLR Bit-13 serves as the Overflow flag (V) for Add and Subtract operations. FLR13 is allowed to change state when LDCLR0 or STFL0 is active. If neither of the gating leads are active, the J and K inputs are held at ground.

STFL0 (17F1) is generated on the ROM board at 8R9. STFL0 goes low if the Processor is doing a non-immediate (RD030) Add or Subtract Micro-instruction (RD001·RD011) and RD Bit-13 is set (RD131), specifying set flags.

FLR13 is set when SFLR130 is low. SFLR130 is generated by three NAND gates collector OR tied. The first NAND gate (17H3) is enabled by LDCLR0. The second input is the Exclusive OR of S000 and GB000. The third input is DIFF1, the Exclusive OR of GB000 and, the Exclusive OR of GA001 and SUB1. The NAND gate at 17H3 is low when the overflow condition exists. The overflow indication is created after the ALU has produced the Sum or Difference. Overflow occurs on an Add with like signs or a Subtract with different signs when the resulting sign is different from the sign of the first operand on the B Bus.

The second NAND gate at 17H2, enabled by LDFLR1, has a low output when S Bus Bit-13 (S131) is active. The third NAND gate (17F3) is the master enable for the K input to FLR13. SFLR130 is inverted and the J input is allowed to go high. FLR13 toggles set on the trailing edge of the next DCL1.

FLR13 can also be direct set by SV0. SV0 goes low when the False Sync flip-flop is set (4E3). The False Sync flip-flop is set if the Processor does not receive a return Sync from a device controller within 13 to 15 microseconds from the time the I/O control line is activated to start an I/O operation.

FLR14 and FLR15 serve as the Greater than and Less than flags respectively. FLR14 is set by SFLR140 if the data manipulated on the S Bus is greater than zero or the result of a Test Micro-instruction is true. FLR15 is set by SFLR150 if the data manipulated on the S Bus is less than zero or if the result of a Test Micro-instruction is false.

SFLR140 is generated by three NAND gates collector OR tied. The first NAND gate (17J2) is used to load FLR14 from S Bus Bit-14. The second NAND gate (17J2) is enabled by STF1. The second input is CTF1 and the third input, S000, is high when the S Bus is not negative.

The gating leads STF0 and STF1 are active during a non-immediate AND, OR, Exclusive OR, Add, or Subtract Micro-instruction if RD Bit-13 is set, specifying set flags (8R9).

The Change Test Flags signal (CTF1)(17J1) is active if any bit of the S Bus is active, or if the G or L flag is set. If either the G or L flag is set, FRNS1 is low (17N5). This signal is NANDed, on the ALU board, with the zero indicating outputs from the four 4-bit ALUs at 14S8. If S Bus Bits 0:3 are zero, S0031 is high. If S Bus Bits 4:7 are zero, S0471 is high. If S Bus Bits 8:11 are zero, S8111 is high. If S Bus Bits 12:15 are zero, S1251 is high. The output from the NAND gate at 14S9 (CTF1) returns to the I/O board to enable changing the G and L flags.

The third NAND gate (17K2) is active during a Test Micro-instruction (CTEST1) if the result of the test is true (TTEST1).

The TTEST0 signal (17K1) is generated on Sheet 18 as the collector OR tie of the inverted outputs of the three 19-026 four-to-one multiplexors. TTEST0 (18H5) is low if a testable function is true and the corresponding mask bit in the RD is set. The testable functions and the associated RD bits are listed below.

TESTABLE FUNCTION		
RD BIT	MNEMONIC	MEANING
4	FST1	Fast I/O Interrupt
5	ATN1 · PSW011	I/O Attention and PSW Bit-1 set
6	ARST1	Automatic Restart
7	CATN1	Console Attention
8	SNGL1	Console Single Mode
9	UT1	Utility flip-flop set
10	MALF1	Machine Malfunction
11	PPF1	Primary Power Fail
12	DC1	Data Channel Request
13	DRD1	Data Channel Read
14	MSK1	Mask
15	OP1	Operation Length

The logic to generate SFLR150 is similar to that that generates SFLR140. Except when the FLR is being loaded from the S Bus or cleared on a DO Micro-instruction (CLR0), SFLR140 and SFLR150 are complementary.

The toggle for FLR14 and 15 is generated at 17N4 as the collector AND tie of DCL0 and LDCLR0, STF0, or CTEST0.

3.5.2 Program Status Word (PSW). The Program Status Word (PSW) is a 16-bit register used to define the system status relative to the user program being executed. The Status field (PSW 0:11) is located on the 35-387 Memory Control mother-board and is shown on Sheet 19. The Condition Code field (PSW 12:15) is located on the 35-390 I/O mother-board and is shown on Sheet 17.

PSW 0:11 is loaded from S Bus Bits 0:11 when the PSW is specified as the destination (LPSW1)(29C1). LPSW1 is ANDed with the Destination Clock (DCL1)(29C1) at the gate (29C2) and applied to the clock input of the three 19-030 four-bit shift registers (A48-A50). Pin 06 of each 19-030 shift register is tied to P5 to establish the Load Mode rather than Shift Right Mode.

PSW Bits 12:15 are contained in the 19-017 quad latch (17B-G9). The Condition Code Register may be loaded from the Flag Register or from the Alarm Register. The clock input to the Condition Code latch is high at System Clock time (SCL0)(17B5) when either LCC0 or JACC0 is active (17C5). LCC0 is generated at 9M4 and is low on a DO Micro-instruction (D1) if the Processor is in Phase Three (P31) and RD Bit-12 is set, specifying copy alarm flags to the Condition Code. The data inputs to the quad latch are LCC1 and FLR 12:15, or JACC1 and ALRM 13:15.

All 16 PSW bits are applied to the eight 19-038 dual four-to-one line multiplexors on Sheet 29 for gating onto the B Bus. When the PSW is specified as the Source Register (address '4'), the signal USTRB0 (29A4) goes low enabling all the 19-038 multiplexors. USTRB0 is generated at 18C5 and is active when the Source Register address is hexadecimal 4, 5, 9, or A. RD Bits 9 and 11 are decoded internal to the multiplexors to select which of the four input registers are gated out to the B Bus.

PSW Bit-1 is the I/O interrupt enable. PSW011 is ANDed with ATN1 at 18J3 for the Test Micro-instruction and at 18N3 for generating an interrupt. PSW Bit-2 set allows the Alarm Register Bits 13:15 to be set (17K6). PSW Bit-4 is available at Pin 226-0 on the I/O board back panel to enable detection of the Fast I/O interrupt. (For the regular Model 70, this pin is tied to ground instead of PSW041.) PSW Bit-7 controls the supervisor/user mode of the Model 70 Processor. If PSW07 is set, detection of Privileged instructions is allowed and the optional Memory Protect feature is enabled. PSW07 set allows RAH04 to be set from the DROM (5C2). Privileged instructions are flagged in the DROM by having Bit-4 set. If RAH04 sets, the non-existent ROM address forces the Illegal instruction trap. No hardware significance is attached to the remaining PSW bits.

3.5.3 Alarm Register (ALRM). The three-bit Alarm Register is located on the 35-390 I/O mother-board and is shown on Sheet 17. PSW Bit-2 (17K6) enables setting any bit in the Alarm Register.

ALRM15 is set on the occurrence of Early Power Fail (EPF)(17S6). Refer to 3.2. ALRM14 is set if a Memory Parity Failure occurs (PFF1)(17M6) during Phase Zero or Phase One (PC00). ALRM13 is set if a parity failure occurs during Phase Two or Phase Three (PC01)(17K6). If any bit in the Alarm Register sets, Machine Malfunction goes high (MALF1)(17S9).

The Alarm Register bits can be copied into the Condition Code of the PSW on a DO Micro-instruction, JACC1 high. This is done during the PSW swap routine for Machine Malfunction Interrupt so that the user is informed of the nature of the interrupt.

The Alarm Register is cleared by SCLR0 on Initialize or it toggles clear at SCL1 time when JACC1 is high.

3.5.4 Counter Register (CTR). The Counter Register (CTR) is shown on Sheet 27. It is used to count the number of repetitions of a single micro-instruction when the Processor is executing a Command Repeat, Multiply, or Divide. The Counter is also a testable item for the Branch Micro-instruction.

The five-bit decrementing CTR is loaded from S Bus Bits 11:15 by LDCTR0 (27B1). LDCTR0 is generated at 8C9 and is low when the Destination address is hexadecimal 'C'. LDCTR0 is inverted and NANDed with DCL1 (27E3), producing the low active load pulse for the 19-035 four-bit counter at 27F5. The S Bus Bits 12:15 are toggled into CTR 12:15 at the trailing edge of the load pulse. CTR Bit-11 is maintained in a separate JK flip-flop (27B5) and is toggled by the AND of LDCTR1 and DCL1 (17A3). The J and K inputs to CTR11 track S Bus Bit-11 when DECTR0 is false (27C1).

The DECTR0 lead goes low to allow the CTR to decrement on the trailing edge of DCL1. DECTR0 is generated in two places with an OR tie across the back panel. The first place is on the 35-390 I/O board at 18E9. DECTR0 goes low if the Processor is executing a Branch on Counter Micro-instruction. Op-Code '3' causes BRA1 (18H8) to go high. If the CTR is the specified condition, RD 04:07 are reset and LD01 (18D7) is high. The second place DECTR0 is generated, is on the ALU board at 13F9. DECTR0 is low if the CTR is not zero (CEMT0 false)(13F7) and the Processor is executing a Command Multiply (MPY0), or a Divide (DIV0) Micro-instruction, or if the Counter Mode flip-flop (CMODE) is set after a Command Repeat (13G8). For these instructions, DECTR0 remains active until the counter decrements to zero.

DECTR0 is inverted and ANDed with DCL1 (27A1) to produce the low active decrement pulse to the 19-035 four-bit counter. If the low four-bits are zero when the decrement pulse occurs, a carry pulse is produced on Pin 13 of the I.C. and the CTR 12:15 wraps to a count of 'F'. The carry pulse complements CTR Bit-11.

Two states of the CTR are decoded. Counter equal to zero causes CEMT0 at 27C9 to go low. Counter equal to one causes CTONE0 at 27C9 to go low. These signals are used by the Branch on Counter and the Counter mode logic.

The Counter is preset to a count of 16 by SCLR0 (27C1) on initialize, or CLR1 and SCL1 (27D2) on a DO Micro-instruction.

3.5.5 Register Stack. The register stack shown on Sheet 11 is located on the 35-389 ALU mother-board. The register stack consists of 20, general purpose, 16-bit registers which can be specified as Source and Destination Registers for micro-instructions. These registers can be loaded from the S Bus and unloaded to the B Bus.

The register stack consists of 20, 19-041 four-bit by four-word register files. Each IC has a read enable and two read select lines, and a write enable and two write select lines. This allows a stack register to be both the source and destination in the same micro-instruction. The read enable level selects one of five sets of four ICs. The micro-register stack (MR0, MR1, MR2 and LOC) is selected by RMS0 (11A2). The RMS0 signal is generated at 10D4 and is active when the Source Register address is hexadecimal 0, 1, 2, or 3, or when the DO Micro-instruction forces the LOC to be both the source and destination (FRCLOC0)(9J4).

General Registers 0 through 3 are selected by the signal GR00 (11C1). General Registers 4 through 7 are selected by GR10 (11G1). General Registers 8 through 11 by GR20 (11J1) and General Registers 12 through 15 by GR30 (11M1). The General Registers are addressed by the YD or YS field of the Instruction Register (IR). The micro-program accesses a General Register by specifying the field of the IR that contains the register's address. If the Source Register is YS (hexadecimal D), or if a DO Micro-instruction in Phase Zero has generated Load AR from YS (LARYS0)(9C4), RYS1 is high (10B6). RYS1 is NANDed with the four decoded states of IR Bits 12 and 13 (10M1) to activate the appropriate GRX0 lead on Sheet 10. If the Source Register is YD or YDP1 (hexadecimal E or F), RYD1 is high (10A6). RYD1 is NANDed with the four decoded states of IR08 and 09 (10L1) to activate the GRX0 leads.

Given that RMS0 or one of the GRX0 leads is active, selection of the particular register is done internal to the 19-041 by decoding the state of the two read select lines.

The micro-registers are selected by the leads RMA1 and RMB1 (10F3). These lines track RD Bits 10 and 11 respectively. Both lines are forced high by FRCLOC0 (10F1).

The General Registers are selected by the leads RA1 (10H9) and RB1 (10F9). RB1 tracks IR Bits 10 or 14 depending on whether YD or YS is the source. If YDP1 is the source, RA1 is forced high so that an odd address register is selected (11C1).

The logic for writing into the register stack is similar to that for reading. The significant difference is that the write enable line is a pulse rather than a level. This pulse occurs at SYSCL1 time during DCL1 (10H3). The write pulse is about 30 nanoseconds wide. The minimum pulse width necessary to satisy the 19-041 is 25 nanoseconds. The maximum pulse width depends on the delay through the ALU and is approximately 50 nanoseconds. A wider write pulse mutilates data in a register if the same register is specified as the source and destination.

3.5.6 Shift Registers (SRH and SRL). The two 16-bit Shift Registers, SRH and SRL, are located on the 35-389 ALU mother-board and are shown on Sheet 15. Either shift register may be loaded from the S Bus and unloaded to the B Bus. The SRH and SRL consist of four 19-048, eight-bit, shift register packs, that function as a single 32-bit register when used by the Command Shift Left, Shift Right, Multiply, or Divide Micro-instructions.

The shift register devices can load, shift left, or shift right, depending on the state of the two mode control leads on Pins 01 and 23 of the devices. The logic that generates the mode control leads is shown on Sheet 15.

SRH is loaded from the S Bus when the Destination address is hexadecimal 6. SRH is forced to be a destination during a Command Multiply or during a Command Divide Micro-instruction when the ALU Carry is active (CSV1)(15R1). When SRH is the destination, HDEST0 is low (15L1). HDEST0 causes both SRH mode control leads, SRHM01 and SRHM11 (15J4), to go high, establishing the load function. On the trailing edge of DCL0 (15S1), the S Bus data is copied into SRH. When the Processor is executing a Command Multiply Micro-instruction, MPY0 is low (15L1), forcing SRHM01 and SRHM11 high. During a Command Divide Micro-instruction (15L1), DIV0 is low, forcing SRHM11 high. If CSV1 is high (15R1), SRHM01 is also forced high, establishing the Load Mode. If CSV1 is false, SRHM01 is low and SRH is in the Shift Left Mode.

The data in SRH is shifted left one bit position when SRHM01 is high and SRHM11 is low. This condition is established as mentioned previously for the Divide Micro-instruction, or by CSL0 (15L1) during a Command Shift Left. Anytime SRH is shifted left, SRL Bit-0 shifts into SRH Bit-15. Bits shifted out of SRH00 may be saved in the Carry flag (FLR12) if RD Bit-15 is set, specifying Carry Out (15A3).

The data in SRH is shifted right one bit position when SRHM01 is low and SRHM11 is high. This condition occurs only during a Command Shift Right Micro-instruction (CSR0)(15M1). If RD Bit-14 is set, specifying Carry In, the state of the Carry flag (FLR12) is shifted into SRH00 (15A3).

SRL is loaded from the S Bus when the Destination address is hexadecimal 7. LSRL0 (15N1) goes low forcing SRLM01 and SRLM11 high, establishing the Load Mode.

The data in SRL is shifted left one bit position when SRLM01 is high and SRLM11 is low. This condition occurs during a Command Shift Left (CSL0) or a Command Divide Micro-instruction (DIV0). If RD Bit-14 is set, the state of the Carry flag (FLR12) or, if Divide, the static ALU Carry (CSV1), is shifted into SRL15 (15S9).

The data is SRL is shifted right when SRLM01 is low and SRLM11 is high. This condition occurs during a Command Shift Right (CSR0) or a Command Multiply Micro-instruction (MPY0). The state of SRH15 is shifted into SRL00. If RD Bit-15 is set, specifying Carry Out, the bit shifted from SRL15 is saved in FLR12 (15A3) except during Multiply (MPY0).

The gates that unload SRH and SRL to the B Bus are shown on Sheet 16. The SRH is unloaded when the Source address is hexadecimal 6 (USRH0)(16A1) or when the Processor is executing a Command Multiply or Divide (MD0)(16A1). The SRL is unloaded when the Source address is hexadecimal 7 (USRL1)(16A3).

3.5.7 Instruction Register (IR). The Instruction Register (IR) is located on the 35-387 Memory Control mother-board and is shown on Sheet 18. The IR holds the user's instruction word during emulated execution. The IR may be loaded from the S Bus when it is specified as the Destination. It is also loaded directly from memory upon instruction access Phase Zero. The IR may be unloaded to the B Bus.

During Phase Zero (P01), the Memory Strobe Bus (MS 0:15) is gated to the direct set inputs of the IR flip-flops by GMSIR1 (28B3). IR was previously direct cleared when Phase Zero was entered, CLRIR0 from 28A1.

When the IR is specified as the Destination (hexadecimal 9), LIR0 goes low (28S1). LIR0 is used to develop the toggle inputs (TIR0)(28S3) to the IR flip-flops (Sheet 28).

Bits 0:7 of the IR are applied, as the address, to the Decoder Read-Only-Memory and to the instruction class decoders on Sheet 4. IR Bits 8:15 are used to select the General Registers (Sheet 10). In addition, IR Bits 8:11 are ANDed with PSW Bits 12:15 at 29S7 to generate the testable MSK function.

All 16 IR bits are applied to the eight 19-038 dual four-to-one line multiplexors (Sheet 29) for gating onto the B Bus. When the IR is specified as the Source Register (address '9'), USTRB0 goes low (29A4). RD Bits 9 and 11 are decoded internal to the multiplexors to select the IR. When the Source Register address is 'C', UIR40 goes low (18E5). UIR0 is inverted and ANDed with IR Bits 8:11 (Sheet 28) to develop the B Bus Bits 12:15. The remaining B Bus bits stay false.

3.5.8 Arithmetic Register (AR). The Arithmetic Register (AR), located on the 35-389 ALU mother-board, is shown on Sheet 12. The AR is used to hold the second operand of the Add, Subtract, OR, AND, or Exclusive OR Micro-instruction. The AR may be loaded from the S Bus and unloaded to the Arithmetic Logic Unit (ALU).

When the AR is specified as the Destination (hexadecimal 8), LAR1 goes high (12A1). LAR1 is used to develop the toggle inputs to the AR flip-flops.

The set outputs from the AR are NANDed with the ULAR1 signal to develop the GA leads (GA000:150) as gated inputs to the ALU. ULAR1 is generated at 13N5. For fan-out reasons, it is developed twice. One input to each AND gate at 13N5 is NA0 (13R4). The other input comes from the 19-026 four-wide AND/OR pack A121 at 13N3.

NA0 is only low during a non-immediate (RD030) Micro-instruction that has Bit-12 set, specifying the No AR option. The 19-026 pack produces a high output whenever one of the following conditions is met:

1. The Processor is executing an AND, Exclusive OR, Add or Subtract Micro-instruction (RD001).
2. The Processor is executing an OR Micro-instruction (RD011·RD021).
3. The Processor is executing a Command Divide Micro-instruction (RD010·RD020·RD031·RD061·RD081)
4. The Processor is executing a Command Multiply Micro-instruction (RD010·RD020·RD031·RD061·RD071) and SRL Bit 15 is set (SRL151).

3.6 B Bus Shifter

The GA leads provide the second operand input to the ALU (Sheet 14). The other input is the GB output from the B Bus Shifter (Sheet 14). The B Bus Shifter can load, shift left, shift right, or cross shift the B Bus data prior to presenting it to the ALU. The function performed is determined by the state of the SHCA1 and SHCB1 control leads applied to the eight 19-038 dual four-to-one multiplexors.

3.6.1 Load. The quiescent state of the B Bus Shifter is the Load Mode. This mode exists when both B Bus Shifter control leads are low. SHCA1 is low (12B9) when the Processor is not doing a Command Divide (DIV0)(12B6) or a Load specifying Shift Left or Cross Shift. SHCB1 is low (12C9) when the Processor is not doing a Command Multiply (MPY0)(12C6) or a Load specifying Shift Right or Cross Shift. SHCA1 and SHCB1 are decoded internal to the 19-038 packs to gate each bit from the B Bus to the corresponding GB lead.

3.6.2 Shift Left. The B Bus Shifter is conditioned to shift the B Bus data left one position when SHCA1 is high and SHCB1 is low. This occurs on a Command Divide or on a Load specifying Shift Left (LOAD1·RD121)(12B6). Each bit from the B Bus is gated onto the next more significant GB line. If Carry In is specified on the Load (RD141·DIV0) (15A3), the state of the Carry flag (FLR12) is applied to GB150.

3.6.3 Shift Right. When SHCA1 is low and SHCB1 is high, the B Bus Shifter shifts the B Bus data right one position. This occurs on a Command Multiply (MPY0) or on a Load specifying Shift Right (LOAD1·RD131). Each bit from the B Bus is gated to the next lower position of the GB Bus. If Carry In is specified (DIV0·RD141)(15A3), the state of the Carry flag (FLR12) is gated onto GB000.

3.6.4 Cross Shift. The B Bus data is byte swapped by the B Bus Shifter when SHCA1 and SHCB1 are both high. This condition exists only during a Load Micro-instruction (LOAD1)(12B6), if Cross Shift is specified (RD121·RD131) and not suppressed by the X0 lead (12A6). A Cross Shift becomes conditional if the Memory Data Register (MDR) is specified as either the Source or Destination, or if on an I/O data read or data write, the Halfword test line is active. If the Processor is executing a Data Available or Data Request I/O operation, NOCS0 goes low (9K4) if the Halfword line is low (HW0)(9K1). NOCS0 suppresses Cross Shift (CS1) and jam sets RAL14. If the Cross Shift is not suppressed by NOCS0, and MDR is involved, the Cross Shift is allowed if the Memory Address Register is even (MAR150 high). If MAR is odd (MAR150 low), the Cross Shift is not performed. When the Cross Shift occurs, Bits 00:07 from the B Bus are gated to GB 08:15 and B 08:15 are gated to GB 00:07.

3.7 Arithmetic Logic Unit (ALU). The Arithmetic Logic Unit (ALU) consists of four 19-039 four-bit ALU packs and one 19-040 carry look-ahead pack. The ALU is shown on Sheet 14. The ALU receives five control lines defining the function it is to perform. These control lines are summarized on Table 2.

TABLE 2. ALU CONTROL LINES.

OP	M	S0	S1	S2	SUB
D	0	1	0	0	0
C	0	1	0	0	0
T	1	1	1	1	0
B	1	1	1	1	0
L	1	1	1	1	0
O	1	1	1	0	0
N	1	0	1	1	0
X	1	1	0	0	0
A	0	1	0	0	0
S	0	0	1	1	1

Each 19-039 ALU pack develops four-bits of the low active S Bus. The four S Bus bits are internally NANDed to produce the SXXX1 zero indicating signal. When the signals S1251, S8111, S0471, and S0031 are all high, the S Bus data is zero. Each ALU produces an output carry on Pin 16. Only the carry output of the most significant ALU is used (CSV1)(14D9). The internal Carry Propagated (CP) to the most significant stage of each ALU pack is available on Pin 15, and the Carry Generated (CG) for the most significant stage is available on Pin 17. These signals, CPXX1 and CGXX1 are applied to the 19-040 carry look-ahead pack to develop the Carry In to the next more significant ALU pack (CNXX1).

Each function of the ALU is described in the following paragraphs. Unless otherwise noted, all gate references are to the arbitrary labels on Figure 3.

3.7.1 Load. The ALU is conditioned to the Load Mode on a Test, Branch, or Load Micro-instruction. In this mode, Gates 1, 2, 3, and 4 are enabled by S01, S11, S21 and SUB0 respectively, and Gate 8 is disabled by M1. The AR is not unloaded, so the false GAXX0 Bus disables Gates 2 and 3. Gate 1 produces a high output causing the output from Gate 5 to go low. The state of the GBXX0 Bus is passed to the SXX0 Bus from Gates 4, 6, 7 and 9.

3.7.2 AND. In this mode, conditioned by the AND Micro-instruction, each bit from the B Bus is logically ANDed with the corresponding bit from the GA Bus. The output equation for Gate 5 becomes $\overline{A}\cdot B$. The output equation for Gate 6 is simply B. Consequently, Gate 7 yields the function $A\cdot B$ which is inverted by Gate 9, forming the S Bus.

3.7.3 OR. The OR Micro-instruction causes each bit from the B Bus to be logically ORed with the corresponding bit from the GA Bus. Gate 5 produces a low output because of the complimentary GA inputs. The OR function is realized entirely by Gate 4. Gate 4 produces a low output whenever either the GA or GB input is active (low). The logical sum is double inverted by Gates 6 and 9, forming the S Bus.

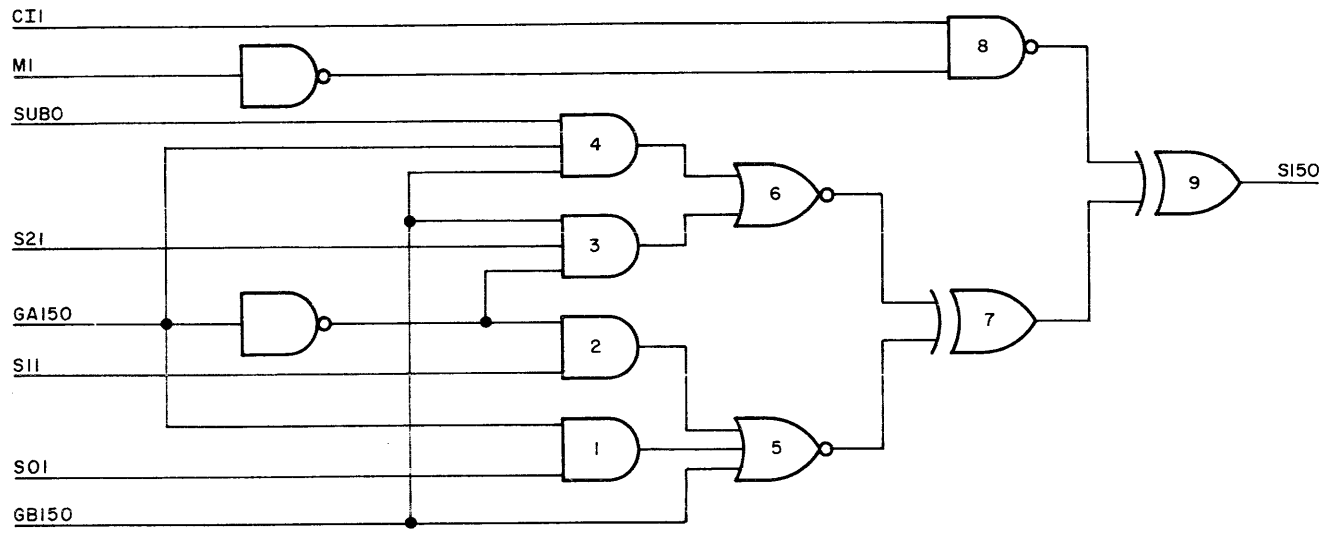


Figure 3. Least Significant ALU Stage

3.7.4 Exclusive OR. The Exclusive OR Micro-instruction produces the logical difference of the data on the GA and GB Busses. Gate 5 produces a high output when the A·B condition is met. Gate 6 produces a high output when the A+B condition is met. When combined by Gate 7, the Exclusive OR function ($A\cdot\overline{B} + \overline{A}\cdot B$) is realized.

3.7.5 Add. The ALU is conditioned to the Add Mode on a DO, Command, or Add Micro-instruction. Note that with the exception of the M control line, Add is the same as Exclusive OR. The M control line enables the carry networks internal to the ALU device so that the output from Gate 8 is $(\overline{A}B+A\overline{B})\cdot\overline{C} + (AB+\overline{A}\overline{B})C$. Figure 3 shows only the least significant stage of the 19-039 four-bit ALU. The next three stages are identical with the exception of the internally propagated carry.

3.7.6 Subtract. The Subtract function produced by the 19-039 four-bit device is A-B-1. For this reason, the Carry In to the least significant state is inverted on the Subtract Micro-instruction. The output equation for Gate 5 is $\overline{A}B$ and the equation for Gate 6 is $\overline{A}+B$. Gate 7 produces a high output when the equation $\overline{A}\overline{B}+AB$ is satisfied. If no Carry In is specified, the CI1 (14A5) lead is high and the output from Gate 9 is high. If Carry In is specified, the output from Gate 7 is inverted by Gate 9, producing the S Bus.

3.8 Counter Dependent Operations

A Command Micro-instruction with RD Bit-6 set implies a counter dependent mode of operation that is maintained until the Counter Register (CTR) is zero. Command Repeat causes the next micro-instruction to be repeated the number of times specified in the CTR. Command Multiply and Command Divide cause the Command itself to be repeated with SRH forced to be the Source and Destination Register. These modes are implemented by the circuit shown on Sheet 13.

3.8.1 Repeat. When a Command Repeat Micro-instruction is executed, CMD1 goes high (13K7). The Repeat flip-flop (RPT)(13K8) toggles set on SCL1 (CMND1·RD091). On the same SCL1, the Counter Mode flip-flop (CMODE) will toggle set if the CTR is not zero (CEMT0)(13N6). If the CTR is zero, the next micro-instruction should not be executed. Since, at the same time RPT flip-flop toggles set, the next micro-instruction toggles into RD, the Processor has to execute the instruction. However, KILDST0 goes active (13N9) stopping the Destination Clock, DCL0 (19M9). No register will be modified, nor will the FLR change. RPT will toggle reset on the next SCL1.

If the CTR is not zero, CMODE and RPT both toggle set. Now the target micro-instruction is in RD. Because CMODE is set, DECTR0 (13F9) goes low until the CTR is zero. The CTR will decrement on each Destination Clock. As long as CMODE is set and the CTR does not equal zero or one (CTLT21)(13M8), STPC0 is low (13R9), disabling RCL0 and RDSTB0 (19L9). The RAL will not increment nor will another micro-instruction be strobed into RD until the Counter decrements from one to zero. As soon as the CTR decrements from one to zero, CMODE and RPT both toggle reset. STPC0 is high and the next sequential micro-instruction is executed.

3.8.2 Multiply. Prior to executing the Command Multiply Micro-instruction, the following preliminary conditions are assumed: The multiplier is in SRL, SRH contains zero, the AR holds the multiplicand, the Carry flag is cleared, and the Counter contains 16. The Command Multiply is executed in 16 machine cycles. On each Destination Clock; the CTR is decremented, SRL is shifted right one place, FLR12 is updated from the ALU Carry (CSV1)(14D9), and SRH is loaded from the S Bus. Refer to Figure 4.

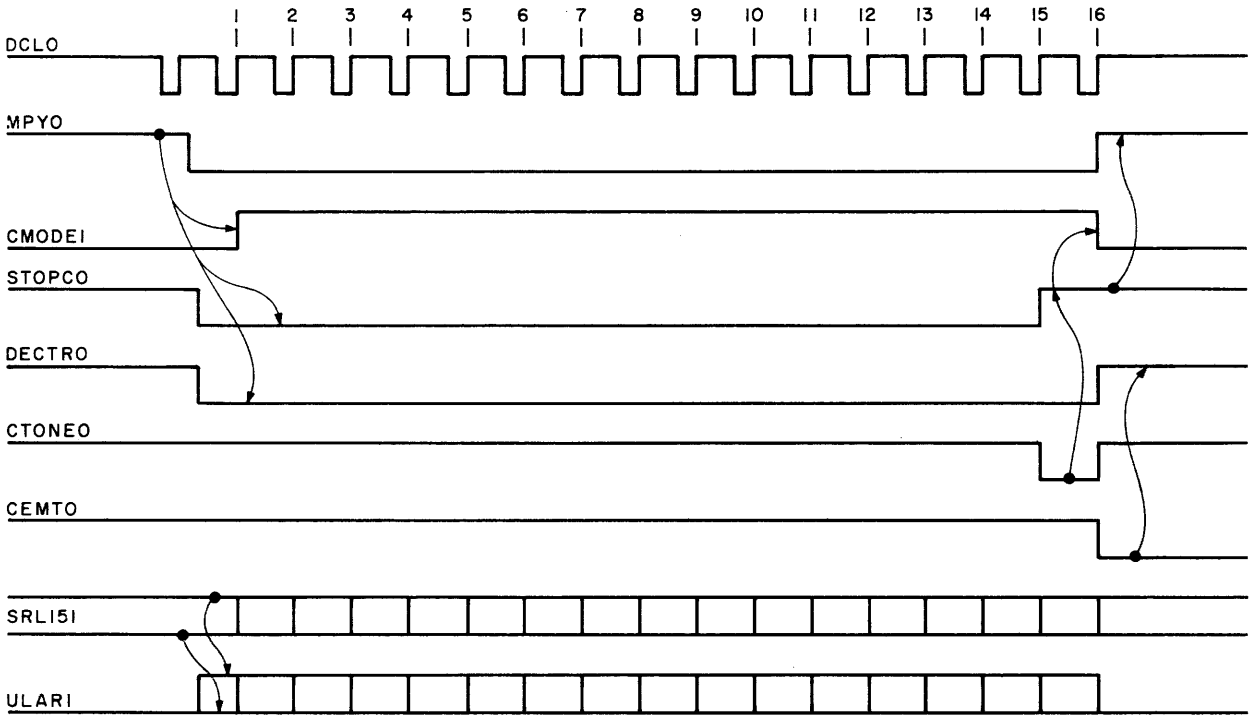


Figure 4. Command Multiply Timing Diagram

As soon as the Command Multiply Micro-instruction is decoded, the signal MPY0 goes low (13H7). As long as the CTR is not zero (CEMT0 false), DECTR0 is low (13F9) and the Counter decrements on the trailing edge of each Destination Clock. Shift Register Lower (SRL) is also conditioned to the Shift Right Mode, SRLM01 low and SRLM11 high, by the MPY0 signal. Similarly, Shift Register High (SRH) is conditioned to the Load Mode, SRHM01 and SRHM11 high. At the trailing edge of each DCL0, SRL shifts right one position and SRH is loaded from the S Bus.

The data loaded into SRH constitutes the sum of the accumulated partial products. The signal MPY0 is ORed with DIV0 to produce MD0 (13H9). MD0 forces the contents from SRH to be gated onto the B Bus (16A1). The B Bus Shifter is forced to the Shift Right Mode by MPY0. Now, depending on the state of the least significant bit from the multiplier (SRL15), the multiplicand in AR is either gated to the ALU or not. If SRL151 is high, ULAR1 (13N5) is high. The AR is gated to the ALU and the sum from AR and the shifted SRH is gated back into SRH. If SRL151 is low, the AR is not gated to the ALU and zeros are added to the shifted SRH. The result of the latter case is a 32-bit shift right.

Carries resulting from the additions that occur are saved in the Carry flag (FLR12) which is shifted back into the high end of the B Bus Shifter for the next cycle so no data is lost.

After the Command Multiply, the product in SRH and SRL must be shifted right one more position.

3.8.3 Divide. Prior to executing the Command Divide Micro-instruction, the following preliminary conditions are assumed: The 32-bit positive dividend is in SRH and SRL, the divisor is in two's complement negative form in the AR, the Carry flag is reset, and the CTR contains 16. The Command Divide executes in 16 machine cycles. On each DCL0; the CTR is decremented, SRL is shifted left one position, FLR12 is updated from the ALU Carry, and SRH is either shifted left one position or loaded from the S Bus. Refer to Figure 5.

The signal DIV0 is low during the Command Divide. DIV0 causes DECTR0 to go low until the Counter decrements to zero. SRL is conditioned to the Shift Left Mode, and SRH assumes the Load Mode or the Shift Left Mode depending upon the state of the ALU Carry (CSV1).

The most significant 16-bits of the dividend in the SRH are present on the B Bus. The data is shifted left one position by the B Bus Shifter and presented to the ALU. Note that SRL00 is carried into GB15 (14R1). The AR is unloaded to the ALU and an 'Add' is performed.

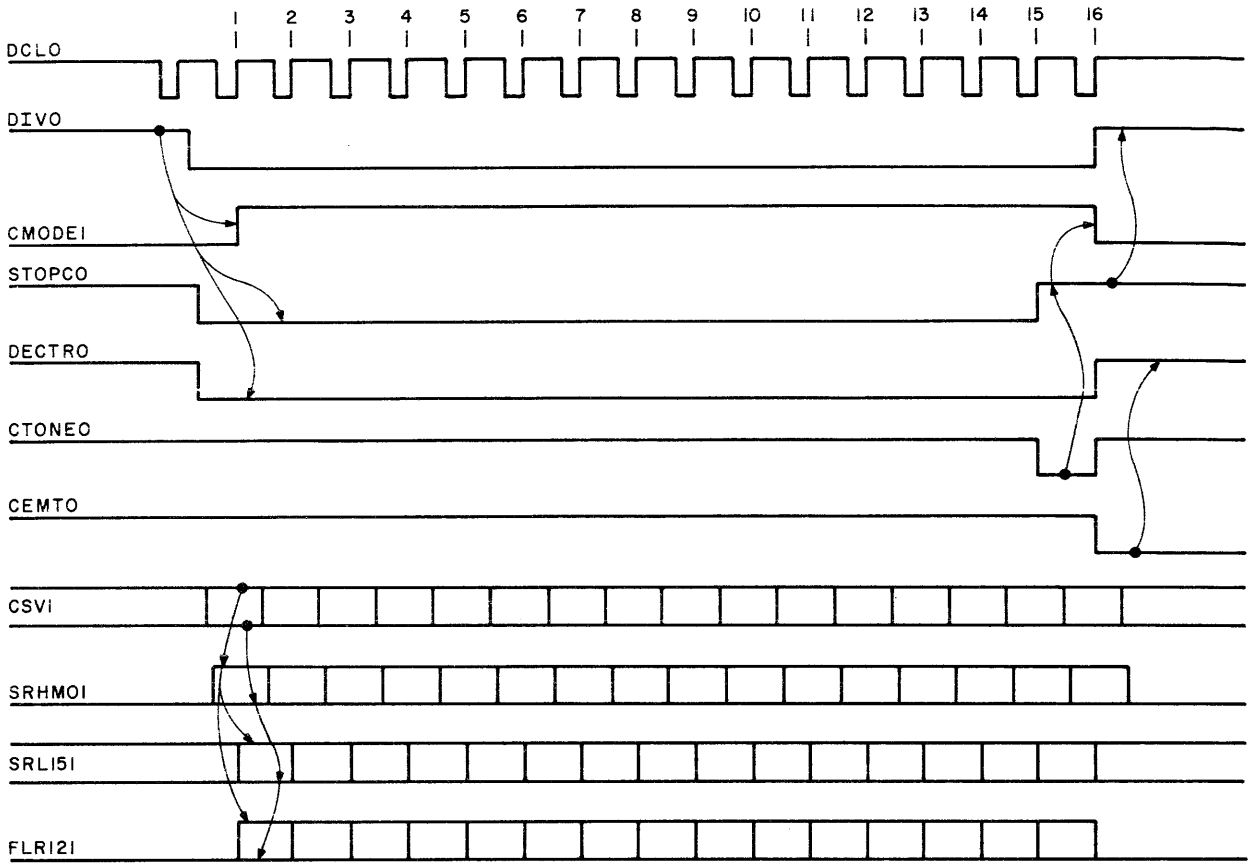


Figure 5. Command Divide Timing Diagram

By adding the two's complement from the divisor in the AR to the most significant half of the dividend in the SRH, the result on the S Bus is actually the difference between the two. If this 'trial subtraction' is successful, the ALU produces a Carry (CSV1 high), and the partial remainder on the S Bus is gated into the SRH. If the 'subtraction' is unsuccessful, CSV1 is low, and the SRH is shifted left one position; the S Bus data is ignored. The CSV1 signal is shifted into SRL15 to form the quotient bits. CSV1 is also saved in FLR12. After the Command Divide, the remainder is in the SRH and the quotient is in the SRL.

3.9 Phase Control

3.9.1 General Description. The Phase Control logic, contained on the 35-388 ROM board, is shown on Sheet 9 and in block diagram form on Figure 6. Phase is a hardware condition that is affected by the DO Micro-instruction and user program activity. Phase, in turn, affects actions resulting from the DO Micro-instruction.

The two stage Phase Counter defines the four hardware phases. Referring to Figure 6, from a count of 00 (Phase Zero), the Phase Counter can go to a count of 01 (Phase One) or 10 (Phase Two). From Phase One, the Phase Counter can only go to Phase Two. From Phase Two, the Phase Counter can go to a count of 00 (Phase Zero) or 11 (Phase Three). From Phase Three, the Phase Counter can only go to Phase Zero. A phase change usually occurs on a DO Micro-instruction. Initialize unconditionally forces the Phase Counter to Phase Three, as does a Phase Two abort.

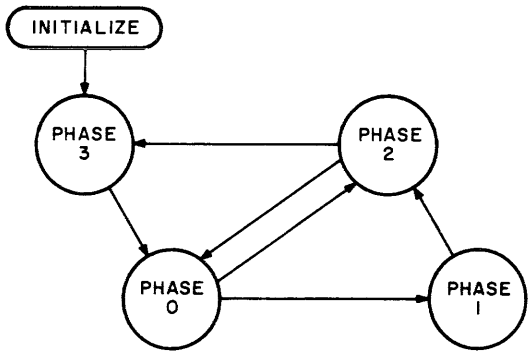


Figure 6. Phase Control Flow Diagram

Each phase, other than Phase Zero, has corresponding sets of micro-code routines. The phase control hardware generates the starting addresses of these routines.

Phase Zero is dedicated to user's instruction decoding. Phase Zero is a purely hardware state, lasting for two or four system clocks. During Phase Zero, the user's instruction is automatically loaded into the Instruction Register (IR), and the A Register (AR) is automatically loaded from the User's second operand register (YS). If the user's instruction is of the RR format (Op-Codes 0n, 1n, 2n, 3n, 8n, or 9n), Phase Zero is exited and Phase Two is entered. If the user's instruction is not RR, a second memory read is generated to fetch the second half of the fullword instruction, the Location Counter (LOC) is incremented by two and Phase Zero is exited.

If the user's instruction is RS (Op Codes Cn or En), Phase One is entered if the instruction is indexed - IR Bits 8:11 not zero - and the ROM Address Registers are forced to '002'. If the instruction is not indexed, Phase Two is entered.

If the user's instruction is RX (Op Codes 4n, 5n, 6n, 7n, An, Bn, Dn, or Fn), Phase One is entered. The ROM Address Registers are forced to '006' if the instruction is indexed or to '004' if the instruction is not indexed.

The Phase One micro-code routines perform the second operand address arithmetic.

The Phase Two entry point for a particular user instruction is derived from the Decoder Read-Only-Memory (DROM). Words in the DROM are addressed by the Operation Code field of the user's instruction, IR 0:7. The DROM contains 256, 12-bit words. The Model 70 user's instruction repertoire uses 113 words. The words not used contain zeros and correspond to illegal user's instructions.

As Phase Two is entered, the DROM read-out is jammed into the ROM Address Registers. The next micro-instruction executed will be that at the specified location.

The Model 70 instruction repertoire includes 22 Privileged instructions. Privileged instructions (all I/O instructions plus LPSW and EPSR) may only be executed if PSW Bit-7 is reset. If PSW07 is set and an attempt is made to execute a Privileged instruction, the Illegal instruction interrupt is forced.

The Privileged instructions are identified in the DROM by having Bit-4 of the read-out set. When Phase Two is entered, the ROM Address Registers are allowed to be jammed from the DROM. Then, when the non-existant location is read-out, the ROM Data Register (RD) is direct cleared.

When Phase Two is entered, the abort Enable flip-flop (EBL) is set. As long as EBL is set, the Processor can be interrupted by the occurrence of an I/O Attention (ATN), a Data Channel request, or a Machine Malfunction which includes parity failure and Early Power Fail (EPF) detection. This abort condition forces the Processor to Phase Three and jams the ROM Address Registers to '00A', the starting address of the abort micro-routine. The EBL flip-flop automatically resets whenever the micro-program does a Memory Write (MW or PW), an I/O operation, or changes a user General Register or the PSW or the LOC. When Phase Two is exited, the DO Micro-instruction automatically tests for interrupts, regardless of the state of EBL. The interrupts tested for are I/O Interrupt (ATN), Console Interrupt (CATN), Console Single Mode (SNGL), Machine Malfunction (MALF), Primary Power Fail (PPF), Data Channel request (DC), and Fast I/O Interrupt (FAST). If any interrupt is true, Phase Three is entered and the ROM Address Registers are jammed to '010'. If no interrupts are pending, Phase Zero is entered.

The Phase Three firmware sets (entry points '000', '00A', '010', and '100') are dedicated to display and interrupt support. When Phase Three is exited, Phase Zero is entered.

3.9.2 Functional Description. When RD 00:03 are zero, D1 goes high (8K4). This may occur on the DO Micro-instruction or an Illegal instruction. The illegal condition exists if the Run flip-flop is set (8J6) and the RD14 flip-flop is reset (8R3). (A DO Micro-instruction always has RD Bit-14 set.)

When the Processor is initialized, the signal SCLR1A (8A6) is active. Initialize clears the ROM Address Registers and the ROM Data Register, and the Run flip-flop at 8J6 is reset. D1 is ANDed with RD140 and RUN1. If the Run flip-flop is not reset at this time, ILEG0 goes low, forcing the Processor to Phase Three and the ROM address to '100'. As soon as a word whose Op-Code is not zero is read from the ROM, $\overline{D0}$ on the J input to Run goes high and the flip-flop toggles set.

The DO Micro-instruction may specify one or more functions to be performed. Bits 4 and 5 specify a Memory Read, Memory Write, or Privileged Write. DDC1 (8B9) is high if the Processor is executing a DO or Command Micro-instruction. DDC1 at 30R9 generates a memory start (PSTART0). See Section 4.

Bit-6 set causes the Location Counter (LOC) to be incremented by two. If the Processor is not going to Phase Three (GTP30) or is not in Phase Zero with Memory Busy (P01·FPMBY1), FRCLOC0 goes low (9J5). FRCLOC0 forces the LOC to be both the Source and Destination (25B1) and forces GA140 to be active (12S3). The AR is not unloaded, so the GAXX0 Bus equals 2. The ALU is conditioned to do an Add operation and, at DCL0, LOC is loaded with the value (LOC)+2.

Bit-7 set causes the contents of the Flag Register to be copied into the Condition Code Register. LCC0 at 9N4 goes low during the last machine cycle of a DO Micro-instruction. A DO Micro-instruction is normally executed in one machine cycle (250 nanoseconds). It takes more than one cycle if a memory operation is specified and memory is busy, or if a phase change is specified and the new phase is Phase Zero.

The phase change is specified by RD Bit-8. The signal DRD081 goes high (8J9) to indirectly enable the Phase Counter. The Phase Counter is initialized to Phase Three. From Phase Three, the Phase Counter can only step to Phase Zero. The K input to the PC1 flip-flop (9G2) goes high with DRD081. The K input to the PC0 flip-flop (9F2) goes high because DTEST0 and GTP30 are false. DTEST0 can only be active during Phase Two and, GTP30 can only be active during Phase Two or on Illegal. The NAND gate at 9F7 produces a low output on DRD081 if memory is not busy (FPMBY0). The Phase Enable lead (PHEN1) at 9F9, goes high. This lead is ANDed with MSST0 and SCL1 to develop the toggle input to the Phase Counter flip-flops (9F2). MSST0 (9E1) is low if an attempt is made to start memory when the memory is busy. On the trailing edge of SCL1, Phase Zero is entered.

The DO Micro-instruction that causes Phase Zero to be entered must specify a Memory Read. The word read from memory will be taken as the next user instruction to perform. Phase Zero lasts for two or four machine cycles (assuming one microsecond core memory). For the duration of Phase Zero, the DO Micro-instruction remains in RD. The signal STOP0 goes low for the cycle before Phase Zero was entered by DRD081·DTEST0·PC01 (9B1). As soon as Phase Zero is entered, P01A·FMDUA1 (9D1) holds STOP0 down until memory data is available. STOP0 disables RDSTB0 and RCL0 (19L6) so that another micro-instruction is not strobed into RD, and RAL does not increment.

On the machine cycle before Phase Zero is entered, the ROM Address Registers are cleared (PHEN1·P00·T21·SYSCL1 = RACLR0) (9B9). At the same time, the Instruction Register is direct cleared by CRLIR0 (9A9).

When the memory data is strobed into MDR, the IR receives the same information. GMSIR1 goes high (28C2) to gate the Memory Strobe Bus (MS) to the direct set inputs of the IR flip-flops. Shortly after the Memory Strobe (MS), and one machine cycle into Phase Zero, the data unavailable signal FMDUA1 goes low. See Figure 7.

If the instruction in IR is of the RR type, RR1 (9D5) goes high. Phase Zero and RR generate GTP21 (9D9) and PHEN1 (9F9). GTP21 allows the J input to the PC1 flip-flop to go high (9G2). The Phase Counter steps to Phase Two on the SCL1. GTP21 also generates GDROM0 at T21 time (9H9). The GDROM0 signal strobes the DROM read-out into the ROM Address Registers on Sheet 5. On the clock that steps the Phase Counter to Phase Two, the AR is loaded from the user's second operand register, specified by YS. LARYS0 at 9C4 goes low when memory data becomes available. LARYS0 forces YS to be the source and the AR to be the destination. The contents of YS are added to zero and placed into the AR.

If the user's instruction is not RR, the signal STOP0 is held low until memory becomes un-busy (9D3). Phase Zero will last for four machine cycles. After memory data becomes available, the AR is loaded from YS and, at the same time, the Skip flip-flop (Sheet 18) is toggled set by SSKIP0 (9B9).

The Skip flip-flop resets, on the clock, after memory goes un-busy (KSKIP0)(9F9). The Skip flip-flop keeps YS off the B Bus for the remainder of Phase Zero by disabling the LARYS0 signal at 9C4.

The B Bus must be kept clear so that when memory does go un-busy, the LOC can be incremented again (FRCLOC)(9J5). As soon as memory goes un-busy, another Memory Read is started. This occurs because the DO Micro-instruction is still in RD. This Memory Read will fetch the second half of the user's instruction. If the instruction in IR is RS with no indexing (AMOD0), the new phase is Phase Two (GTP21 = 1)(9D9). When memory goes un-busy, PHEN1 goes active to step the Phase Counter to Phase Two. See Figure 8.

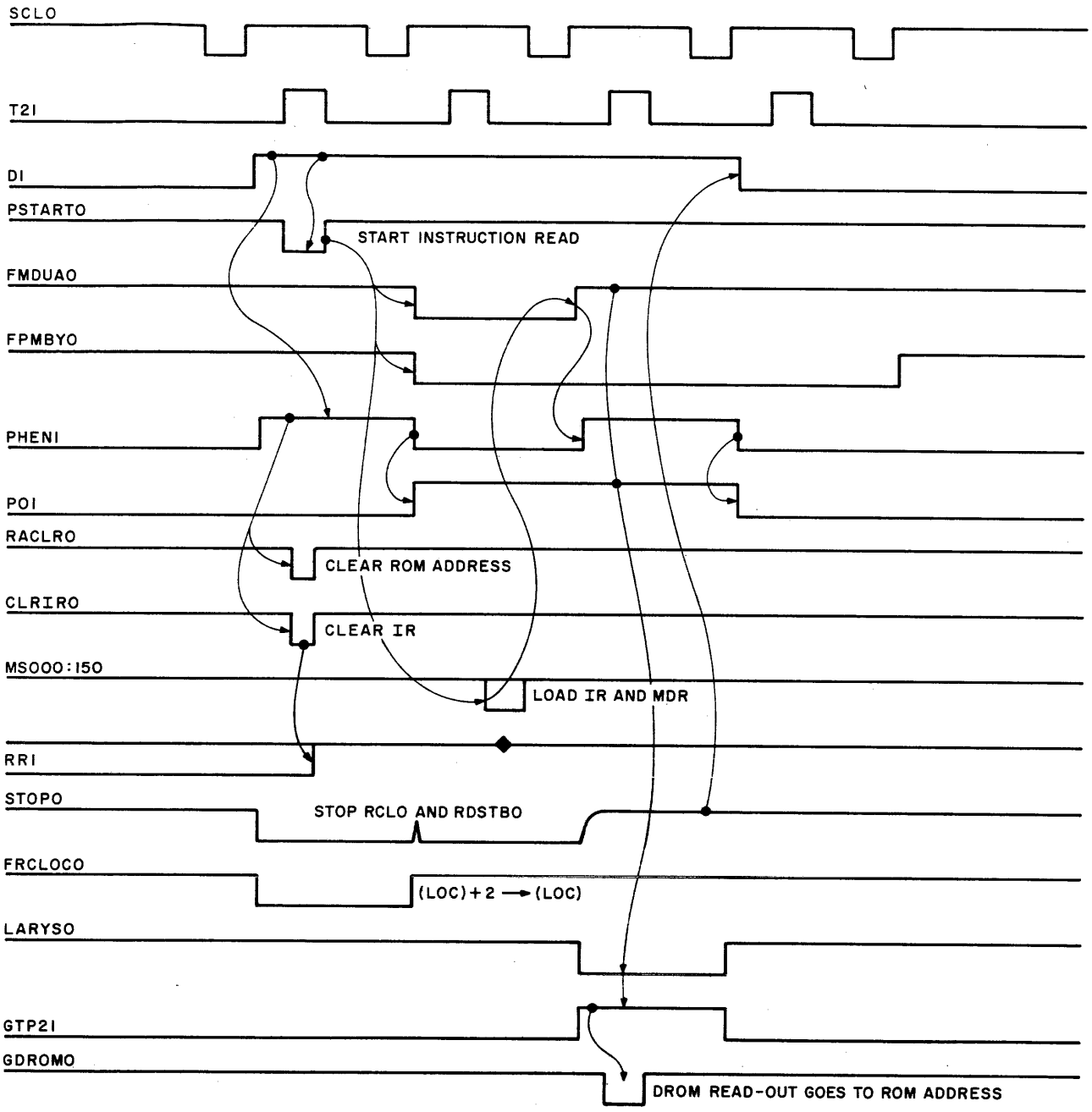


Figure 7. Phase Zero Timing (RR)

If the instruction in IR is RS with indexing or is RX, the new phase will be Phase One. The J input to PC1 goes high (P01·GTP10). On T21, the Phase One entry point is generated by the gates in area 9G3 and at SCL1, Phase One is entered.

The DO Micro-instruction exiting Phase One always causes Phase Two to be entered. GTP21 is active during all of Phase One. The DO Micro-instruction that exits the two RX Phase One routines ('004', '006') specifies a Memory Read. Normally, execution of the DO Micro-instruction is delayed because memory is still busy from the Memory Read generated in Phase Zero.

If IR holds a STH, BAL, BTC, or BFC user instruction (Op-Codes '40', '41', '42', or '43'), the signal STBR1 at 9E6 goes high. STBR1 generates DISB0 at 9C9 which in turn causes PHEN1 to go high and NOMEM0 to go low. This Phase One DO Micro-instruction will execute in only one machine cycle. NOMEM0 keeps the memory from starting (8A9) and DISB0 keeps the clocks from stopping (4L1). See Figure 9.

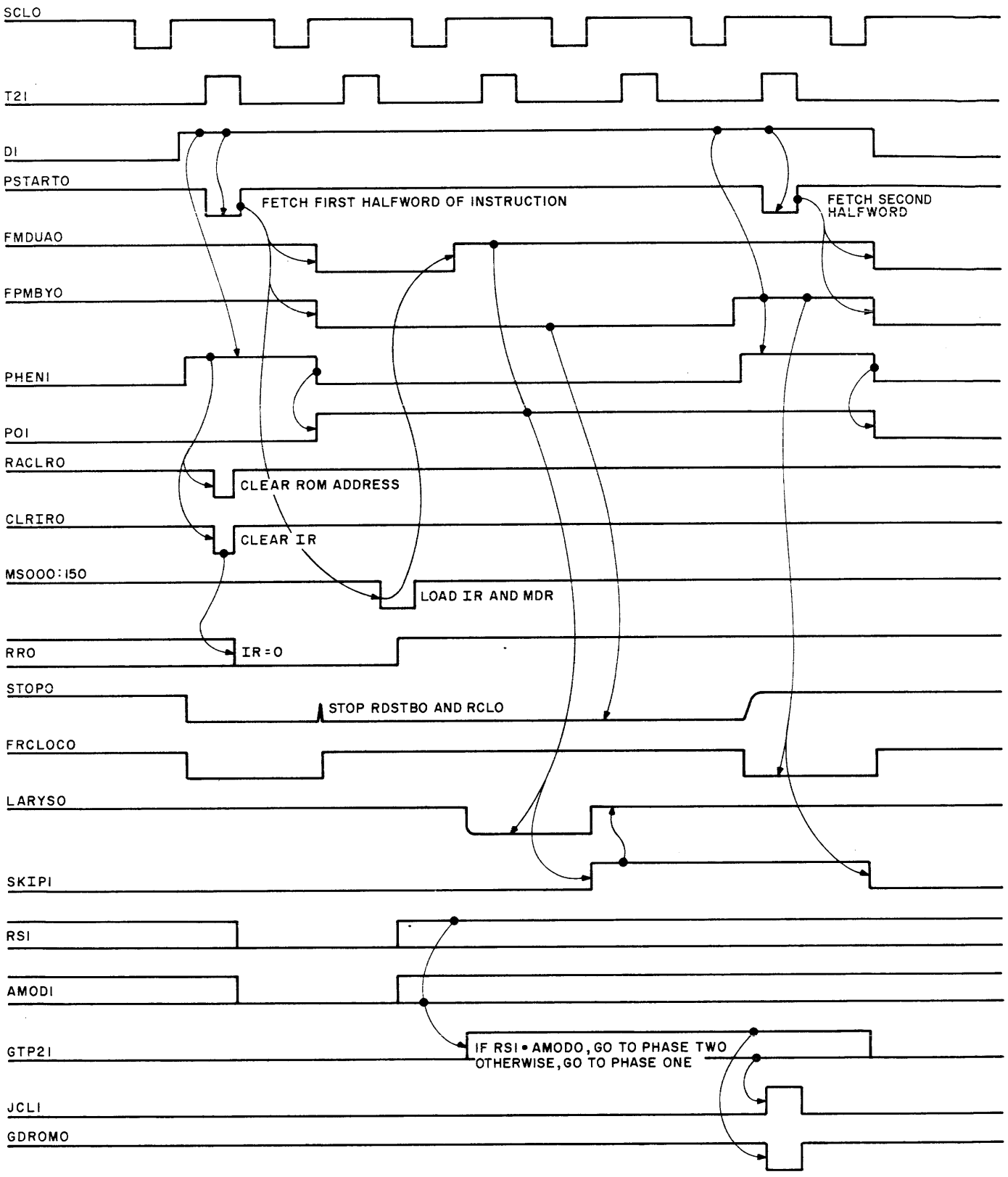


Figure 8. Phase Zero Timing Non-RR.

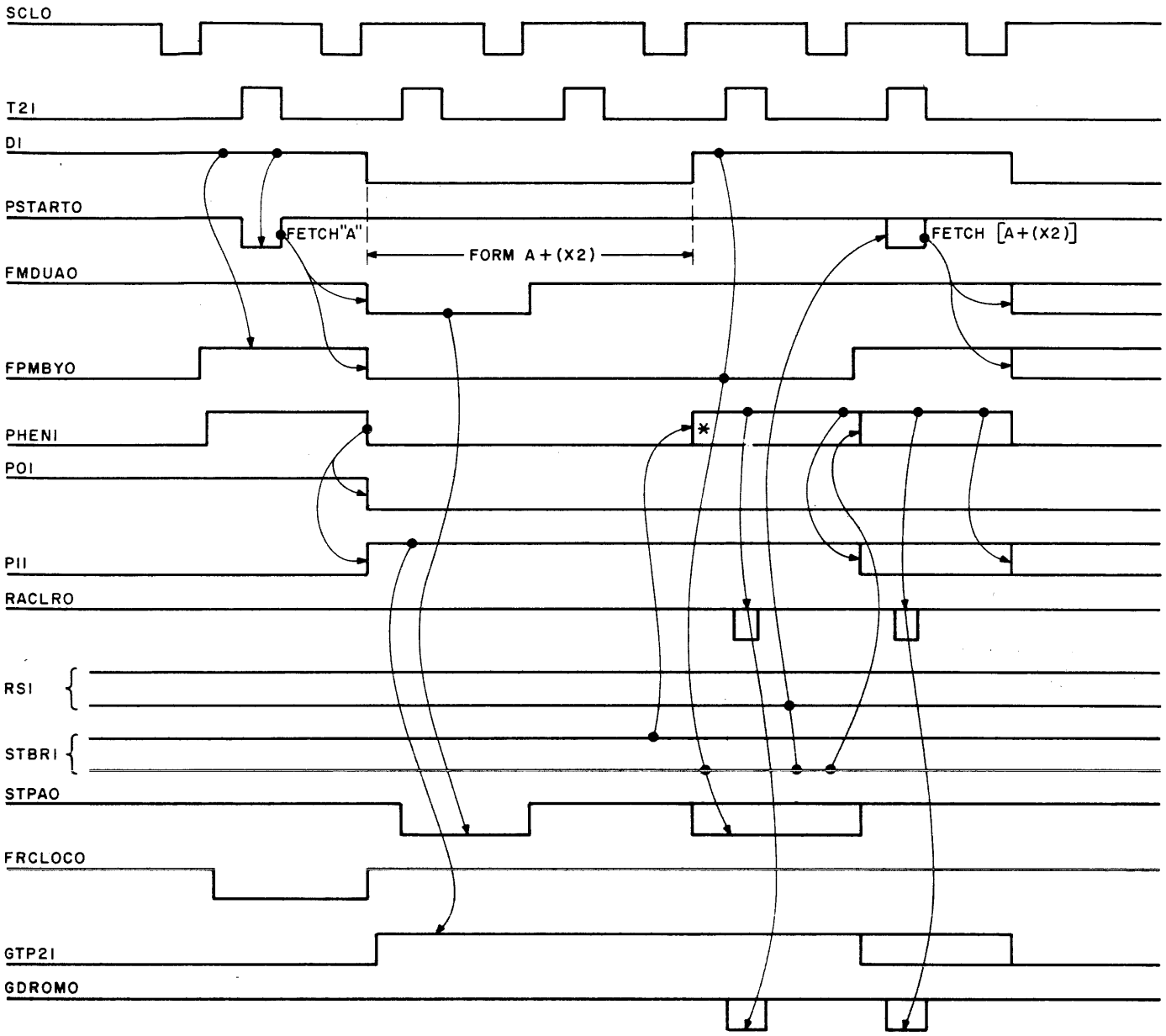


Figure 9. Phase One Timing

If the instruction in IR is illegal, the associated DROM read-out is zero. The Processor enters Phase Two and reads the contents of ROM location '000' into RD. ROM location '000' contains zeros so the illegal condition occurs. ILEG0 goes low (9G5). PHEN1 goes high due to the GTP30 signal. On the next SCL1, the Phase Counter steps to Phase Three. The ROM Address Registers clear at T21 (RACLR0), and RAH07 is forced set (SRAH070)(9H9). If the instruction in IR is privileged (DROM Bit-4 set) and if PSW07 is set, RAH04 is allowed to set. The illegal ROM address causes RD to be direct cleared on RDSTB0 and the illegal condition occurs. See Figure 10.

As soon as Phase Two is entered, the abort Enable flip-flop (EBL)(4S3) is allowed to set. EBL resets when a Memory Write or Privileged Write is performed (MWPW0), an I/O operation is performed (UD100, LD100), a General Register is loaded (LGR0), PSW is loaded (LPSW0), or the LOC is loaded (LLOC0, FRCLOC0). If one of these conditions occurs on the first micro-instruction in Phase Two, EBL resets immediately. As long as EBL remains set, if an I/O Interrupt (ATN1·PSW01), Data Channel Interrupt (DC0), or Machine Malfunction (MALF1) occurs, the TESTA flip-flop is allowed to set. If TESTA sets during Phase Two, ABRT0 goes low. ABRT0 causes GTP30 to go low (9G6). On the next SCL1, the Processor enters Phase Three at ROM address '00A'. See Figure 11.

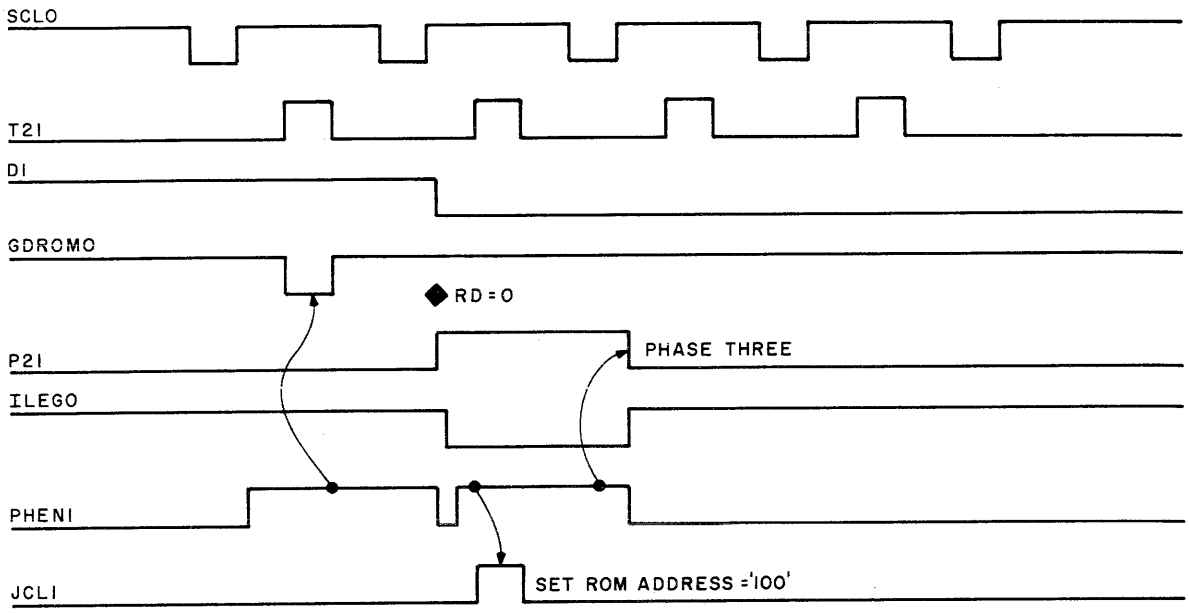


Figure 10. Phase Two Timing (Illegal)

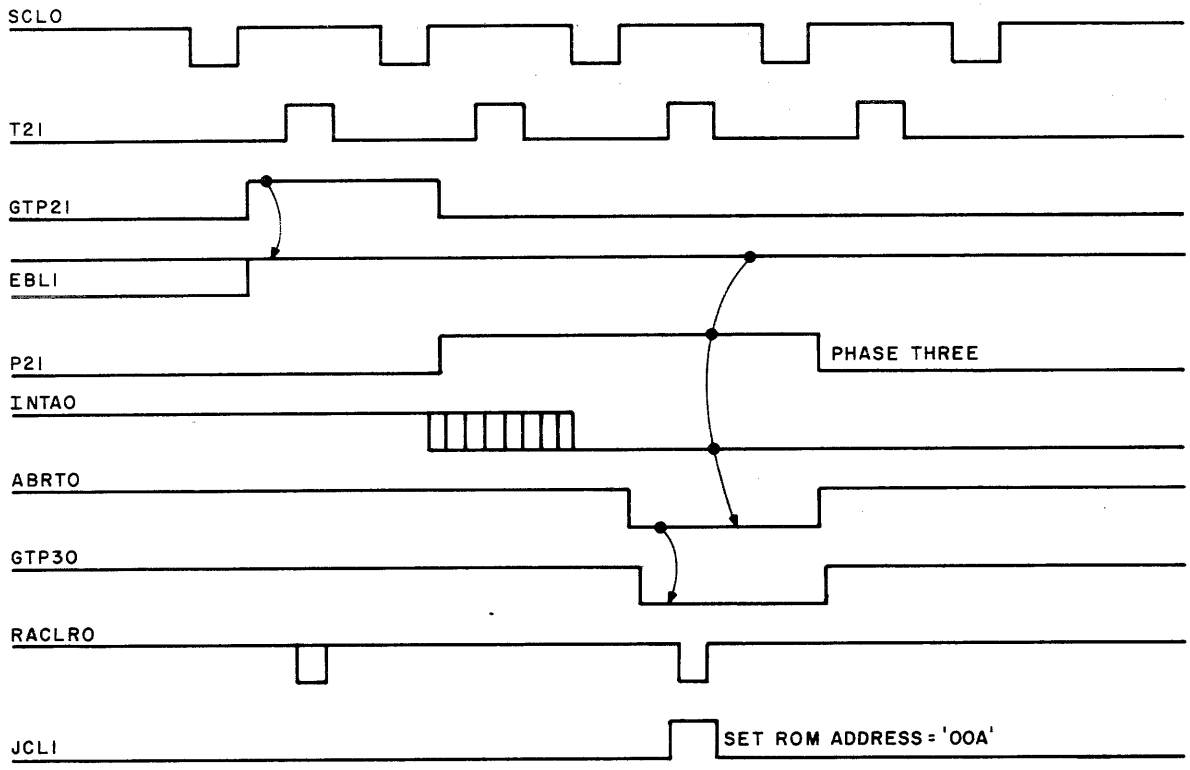


Figure 11. Phase Two Timing (Abort)

If an abort has not occurred, the DO Micro-instruction that exits Phase Two automatically tests for interrupts. See Sheet 18. The interrupts tested for are ATN1·PSW011, DC0, and MALF1 which form INTA0; and CATN0, SNGL0, or PPF0 which form INTB0. The occurrence of any interrupt is synchronized by the Test flip-flop. If Test is set when the DO Micro-instruction that exits Phase Two is executed, D1·RD081A·TEST1 generates DTEST0. DTEST0 (18N9) causes GTP30 to go low. The Processor enters Phase Three at ROM address '010'. See Figure 12.

If no interrupts are pending, DTEST0 remains high and the Processor goes to Phase Zero instead of Phase Three, as shown in Figures 7 and 8.

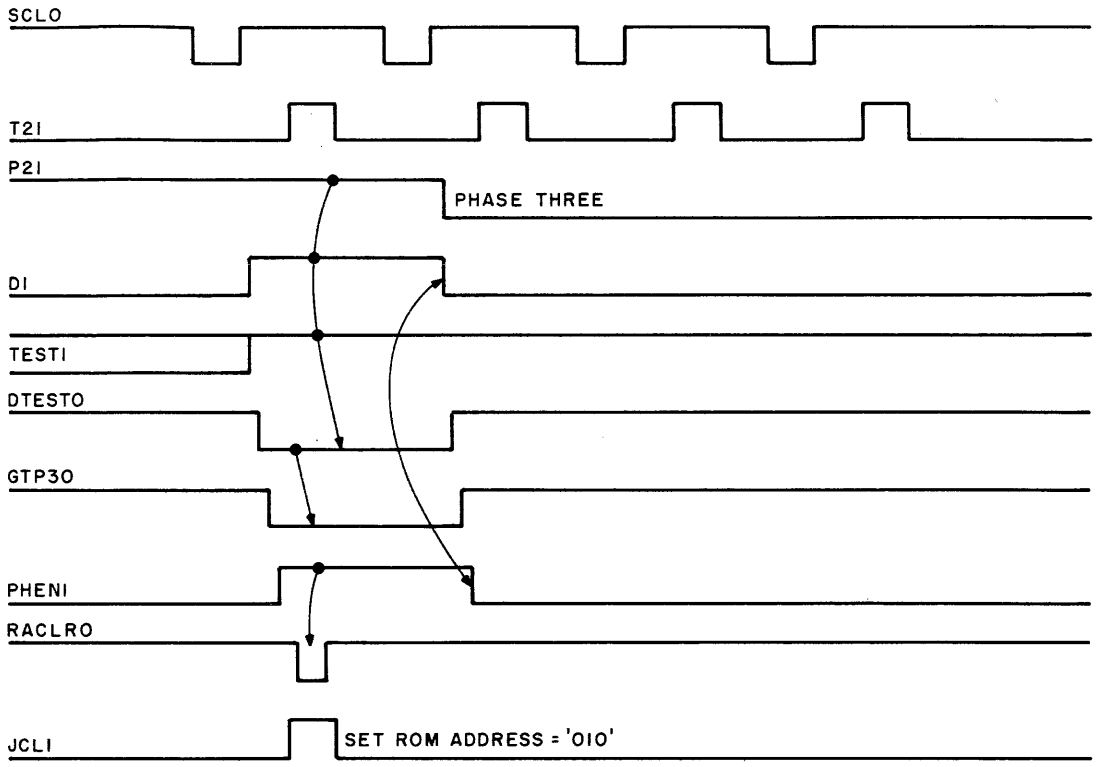


Figure 12. Phase Two Timing (Interrupt)

Bit-9 set causes CLR0 to go low during the last machine cycle of a DO Micro-instruction. CLR0, also low on GTP30, resets the Bank flip-flop (12M8), the Utility flip-flop (12M8), the CMODE flip-flop (13M8), the RPT flip-flop (13K8), the Flag Register (Sheet 17), and the Counter (27F5). For the case where CLR0 and LCC0 are both active, the Condition Code of PSW is updated from the FLR before the FLR is reset.

If RD Bit-10 is set, the Wait indicator on the Control Panel is set. The Wait lamp is driven by the RS flip-flop shown on Sheet 8. RD Bit-11 set causes the Wait flip-flop to reset.

If RD Bit-12 is set, Bits 13, 14 and 15 of the ALRM Register are loaded into Bits 13:15 of the Condition Code. The signal JACC0 (9L4) goes low only if the Processor is in Phase Three. On Sheet 17, if LCC0 is also active, the ALRM bits are ORed with the FLR bits and loaded into the Condition Code.

If RD Bit-15 is set, a Power Down is generated (POW0)(19L2) to set the STPSYS flip-flop.

3.10 I/O Control

An I/O operation is initiated if IO is the Source or Destination of a Load Micro-instruction. The I/O Control logic is shown on Sheet 4. The control line gating is shown on Sheet 20 and the data line gating is shown on Sheets 16 and 20. If RD contains a Load Micro-instruction, LOAD1 at 4B1 is high. If IO is the Source, UDIO0 is low. If IO is the Destination, LDIO0 is low. LOAD1 (LDIO1+UDIO1) produces G101 (4B2) which starts the I/O sequence. I/O timing is discussed separately for input and output.

3.10.1 Input. The initialized state of the I/O sequencer is Line, DST, and DIO flip-flops reset. On input, UDIO0 is low and LDIO0 is high. The gate at 4C3 produces a low output at T21 time, direct setting the Line flip-flop. On the trailing edge of T21, the DST flip-flop toggles set. This disables the clocks DCL0, RDSTB0 and RCL0 until a Sync returns to reset the DST flip-flop. Because the Line flip-flop sets, a control line, selected by RD 14 and 15 is gated out (Sheet 20). The addressed device controller should respond to the control line with data on Data Lines D00:15 and a Sync.

When the Line flip-flop sets, the 13-15 microsecond delay at 4H2 starts. This delay generates a False Sync if a device fails to respond within the delay period, assuring that the Processor does not hang up. The RS flip-flop (DIO)(4E3) latches the occurrence of a False Sync and locks out the other. SYNCH1 goes high allowing DST to toggle reset on the next T21, and the Line flip-flop to toggle reset on the following DCL1 which resets the RS flip-flop had Sync time out occurred. The False Sync delay is also direct cleared.

When the Line flip-flop resets, the control line drops and the device controller drops SYN0. SYNCH0 is used to keep an I/O operation from starting until SYN0 from the previous operation has been dropped.

In the case of a False Sync, the Overflow flag (FLR13) is direct set at SCL1 time by the SV0 lead (4F4). If the I/O operation was a Status Request, B Bus Bit-13 is forced active (B130)(4G4) to simulate the Examine Status condition.

At the end of an Input type I/O operation, the DCL1 that toggles the Line flip-flop reset also loads the specified Destination Register from the S Bus. See Figure 13.

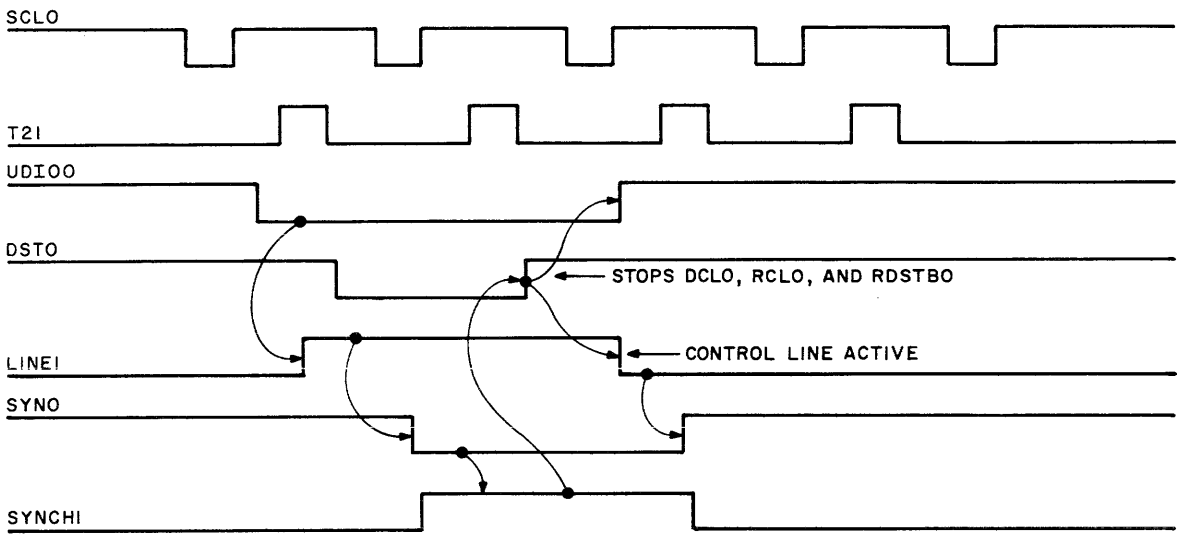


Figure 13. I/O Timing (Input)

3.10.2 Output. With LDIO0 active, DST toggles set at T21 time and 100 nanoseconds later, the Line flip-flop is direct set by the gate at 4C4. The delay is to guarantee that the data to be output is present on Data Lines D00:15 at least 100 nanoseconds before the control line is switched on. The control line, selected by RD Bits 14 and 15, is active from the time the Line flip-flop sets until DST resets. The control line is dropped early so that the data lines remain active for at least 100 nanoseconds after the control line. When the Line flip-flop sets, the False Sync delay starts. When a Sync returns (SYN0) or a False Sync is generated, the DST flip-flop toggles reset followed at DCL1 by the Line flip-flop. The DIO flip-flop latches the occurrence of a False Sync until the Line flip-flop resets. See Figure 14.

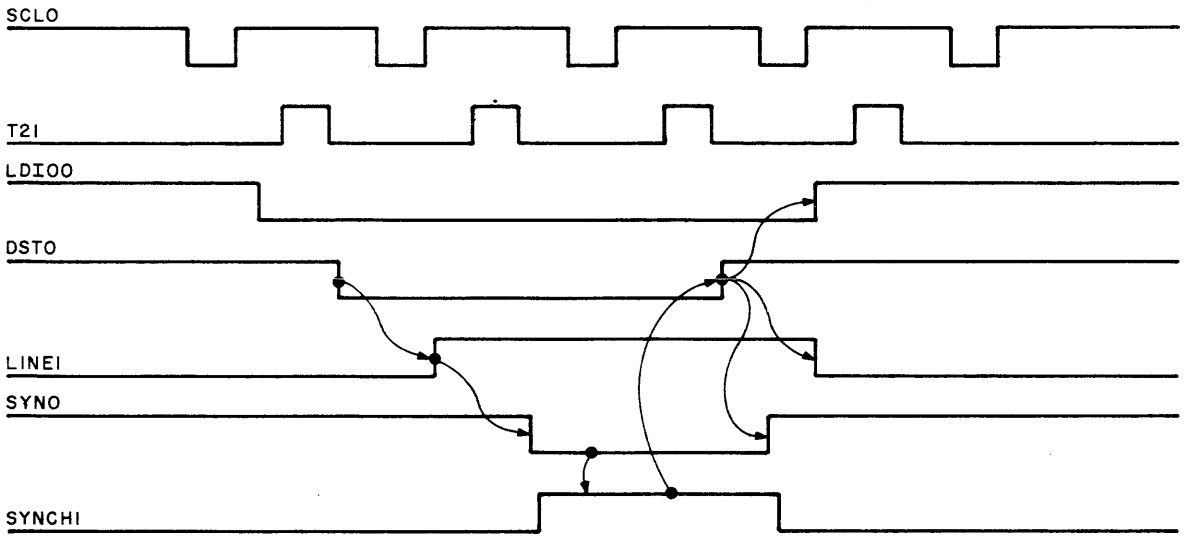


Figure 14. I/O Timing (Output)

3.10.3 Halfword I/O. Special device controllers that make use of the 16-bit I/O data bus activate the Halfword (HW0) test line while they are addressed.

NOTE

Data Channel devices must not activate the Halfword test line (HW0).

The HW0 line has no affect on the Input/Output sequencing described above. NOCS0 forces Cross Shift (CS1)(8M9) to be false so that X0 is high and no Cross Shift can occur. Also, RAL Bit-14 is forced set by SRAL140 at 5H5. This results in a skip of two micro-instructions, unless RAL14 is already set.

Data should only be exchanged with halfword devices with the RH, RHR, WH and WHR user instructions. Only on these instructions has the firmware been purposely aligned to take advantage of the skip on Halfword I/O.

4. MEMORY INTERFACE

4.1 General Description

The memory interface consists of data, address, timing, and control lines which provide the communication path between the memory modules, the Processor, and the Direct Memory Access (DMA) ports. Up to four Direct Memory Access devices plus the Processor may be connected to the memory via the memory interface.

The timing and control circuits for the memory are contained on the Memory Control mother-board. The logic for controlling the memory parity and the Memory Protect controller is also included on this board; although these features are optional, the basic circuits are always provided. The memory may be expanded up to 32K 16-bit words with no modification to the existing control circuits.

The Data and Address Registers are OR tied to the Memory Bus. They are contained on the Memory Control mother-board and are dedicated for Processor memory operations. The timing and control logic is shared by all the devices using the memory. All busses are of the false type (low active). That is; an active bit is 0 to .4 VDC and an inactive bit is 2.4 to 5.0 VDC.

4.2 Functional Analysis

4.2.1 Memory Address Registers. The Memory Address Register (MAR) shown on Sheet 25, is a double rank register consisting of four 19-030 four-bit shift registers (MAR), and four 19-027 quad latch circuits, the Memory Address Slave Register (MAS). The shift registers are permanently tied in the parallel load mode. These registers are loaded on the trailing edge of DCL0 when LMAR0 is present. MAR may be unloaded to the B Bus via the eight 19-038 multiplexors shown on Sheet 29. The MAS Register follows the MAR whenever the memory is not in use. This is accomplished by holding the clock on the MAS latch circuits high except when MB1 or FPMBY1 are active (25A1). MB1 and/or FPMBY1 are active throughout the memory cycle. See Figure 15. It is therefore possible that the MAR holds information different from that in the MAS Register. The outputs from the MAS Register (MA000:140) are gated to the Memory Address Bus any time PSEL1 and PSEL1A are active (25H7). When a Direct Memory Access device captures a memory cycle, PSEL1 and PSEL1A are inactive, inhibiting the MAS Register outputs to the Memory Address Bus.

Memory Address Bits MA000, MA010, and MA020 are inverted and assigned to back panel pins. The true and false sides of these memory address bits are used to define the active memory module. The memory positions on the back panel have pre-wired slots to accept eight memory modules.

In addition to the Memory Address Bus, the seven most significant bits of the MAS Register (25A-G6) are brought out via connector three, where they are available for the Memory Protect controller option.

4.2.2 Memory Data Register. The Memory Data Register shown on Sheet 26 is a 16-bit register which can be loaded from the S Bus or the Memory Bus. Its outputs can be unloaded to the B Bus or the Memory Data Bus. When the MDR is loaded from the S Bus, data is toggled in on the falling edge of DCL1. The gating provided allows three different modes to load the MDR. If the micro-code specifies no Cross Shift operation, the entire 16-bits on the S Bus are loaded into the MDR. This is accomplished by the inactive Cross Shift (CS1)(26A1) which allows the clock DCL1 to appear at all toggle inputs. If a Cross Shift operation is specified, either the least or the most significant byte is loaded without changing the remaining byte. The state of X1 (26A1) determines which byte is loaded. X1 is generated on Sheet 9 and is active if Memory Address Register Bit-15 is inactive. An active X1 loads the cross shifted S Bus Bits 8:15 (on S Bus 0:7) into the MDR 0:7, thus only the left-most byte at the specified 16 bit memory location is changed. If X1 is inactive (MAR15 active), the cross shifted S Bus Bits 0:7 (on S Bus 8:15) are loaded into the MDR 8:15, thus only the odd or right-most byte is changed.

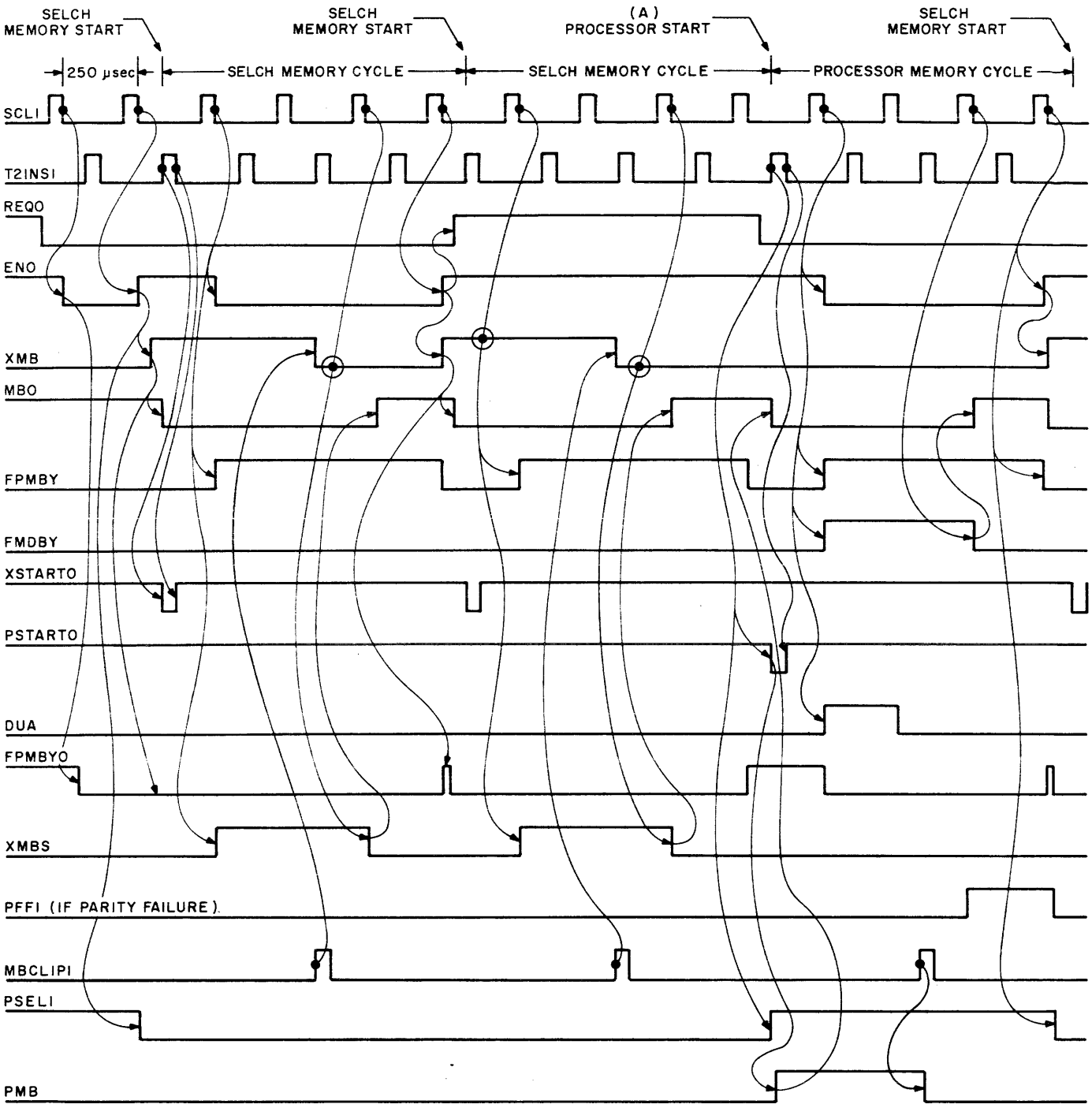


Figure 15. Memory Interface Timing Diagram

When a Memory Read operation is specified by the micro-code, the MDR is loaded directly from the Memory Bus (MS). In this case, READ1 (26A1) and PSEL1A (26B1) are true and the single rail MS Bus is gated to the direct set inputs of the MDR. MDR is cleared prior to memory data being strobed to the MS Bus by the gate at 26A2. Data Unavailable (DUA1) and READ1 (26A1) are both true during the Clock pulse (SCL1) that follows a Processor initiated Memory Read operation. MDRCLR0 goes active clearing the MDR. The memory access time is approximately 300 nanoseconds thus memory data appears on the MS Bus between the two Clocks pulses (SCL1) following a Processor memory start.

4.2.3 Memory Control Circuit. The memory control circuit shown on Sheet 30 consists of two sets of control flip-flops, one set is used when a DMA device captures memory, the other is used when the Processor captures memory. Figure 15 indicates the control sequence.

Assume that a Selector Channel requests a memory cycle. REQ0 (30L1) is activated and on the falling edge of the Clock pulse (SCL1), the EN flip-flop toggles set and EN0 to the channel drops. The EN flip-flop also prevents the Processor from starting memory, by holding PSTART0 high and FPMBY0 low. FPMBY0 is used primarily to stop the clocks.

When the EN flip-flop is set, the SELCH is guaranteed the next memory cycle. If memory is not busy, the EN flip-flop is cleared on the next SCL1. This causes the XMB and PSEL flip-flops to toggle set, allowing the memory to be started on the next occurrence of T21NS1 and deselecting the Processor registers. The Selector Channel may continue requesting memory and capture succeeding cycles under control of the EN flip-flop. On the Clock pulse following the start of the memory cycle, the FPMBY and XMBS flip-flops toggle set assuring FPMBY0 to the Processor and setting up conditions for a graceful completion of the memory cycle. The next action is initiated by the 100 nanosecond MBCLIP pulse, generated by a variable delay at 30C6. This delay is set such that MBCLIP occurs between the second and third SCL1 following the memory cycle start (500-600 nanoseconds after memory start). This pulse (MBCLIP) clears the XMB flip-flop which allows the XMBS flip-flop to clear on the following SCL1. The result is MB0 becomes inactive (30R1) allowing the EN and the FPMBY flip-flops to be cleared on the next SCL1. As seen from the timing chart, four Clock pulses (one microsecond) have occurred and the control circuit is initialized to start another Selector Channel cycle.

If the Selector Channel did not request a second cycle (point A in Figure 15), the EN flip-flop remains cleared. The PSEL flip-flop is cleared on the following T21NS1 and the Processor is free to start a memory cycle via PSTART0. The sequence of events is similiar to the Selector Channel cycle except that the DUA delay is triggered when memory is started. This delay is adjusted such that the DUA flip-flop is set for one SCL1 clock period (250 nanoseconds) following memory start. The DUA flip-flop prevents the unloading of the Memory Data Register prior to memory readout which is in the order of 300 nanoseconds from memory start.

The PSTART0 pulse, in addition to starting a memory cycle, toggles the PMB flip-flop set which allows FMDBY to set on the next SCL1. The sequence of operations is the same as a Selector Channel cycle except that the PMB and FMDBY flip-flops are used in place of the XMB and XMBS flip-flops. FMDBY1 is used to prevent changing the Memory Data Register when a memory cycle is in operation.

4.3 Memory Timing Pulses

The memory timing pulses, ER0, LR0, INH0, and W0 are generated on the Memory Control mother-board and are used to drive the memory modules. Figure 16 indicates their relationships. The chain is initiated by a START1 pulse which is generated whenever PSTART0 or XSTART0 occurs. This activates the delay at 30G3 which generates the ER0 pulse. A second pulse, DLAYA0, is also generated which prevents the LR0 pulse from occurring until 60 nanoseconds following the beginning of ER0. When ER0 and LR0 end, DLAYB1 and DLAYC1, at location 30G7, occur which define the start of INH0 and W0. The width of both these pulses is controlled by the delays at 30B8.

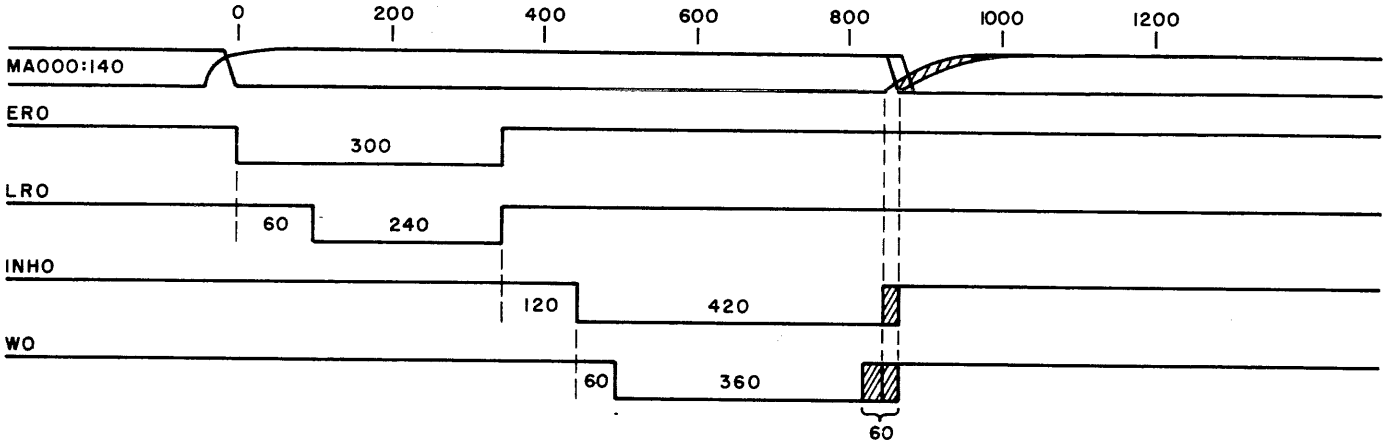


Figure 16. Typical Memory Cycle.

4.4 Parity Check Circuit

The parity control circuit is shown on Sheet 27. Parity is generated on each Write operation and is checked on each Processor initiated read cycle. The Exclusive OR circuits at locations 27R1-5, are tied directly to the Memory Data Bus and statically generate GMD160 which is low if the bus contains an even number of active bits. If a memory read cycle is initiated by the Processor, the Read flip-flop at 27R9 is set. This allows the MS Bus, including the parity bit, to be gated to the Memory Data Register. Bit-16, the parity bit, is loaded into the flip-flop at 27J1. The register is cleared on the start of each cycle by DLAYA1. If the generated parity bit (GMD160) is the same as the received parity bit (MS160), the Parity Fail signal (PFF1) at 27J9 remains inactive. The signal PFF1 will be active on a failure for oen clock period during the memoey cycle. See Figure 15. Note that non-parity memory modules, when accessed, hold PAR0 high which disables the parity fail gate.

The parity bit written to memory during the restore portion of the memory cycle is generated by the check circuit on a write cycle. On a read cycle, the received parity bit is returned to memory. The circuits at 27B3 control this operation. The signal WRT0A presented by a Selector Channel, is active when the Selector Channel is writing.

4.5 Memory Protect

Memory Address Bits 00:06 from the Processor Address Register, are presented to the optional Memory Protect Controller. Note that this provides for protection only on Processor initiated Write operations. If PSW Bit-7 is set, indicating the protect mode, the signal, PRTECT0, is sent to the controller. The controller, if it recognizes a protected address, returns with the Change Write to Read signal (CWR0) which sets the Read flip-flop and allows the MS Bus to be gated to the Memory Data Register, thus creating a read cycle.

5. DISPLAY SYSTEM

The Display System provides a means for reading the contents of all the system registers and any core memory location, together with the capability of manually entering data and programs. Figure 17 shows the Control Console layout. Two register displays are provided. Sixteen switches provide a means for entering memory data and addresses into the machine. The momentary EXEcute control switch requests that any operation, selected by the 12 position rotary Function switch and the SGL and RUN function switches, be executed. The Initialize (INT) control switch resets the system and peripherals. The LOCK-ON-OFF key operated security lock switch, controls power to the system and permits locking the controls. The Control Console is an input/output device interfaced with the Multiplexor Bus. The Display System is supported by a special micro-program sequence in the Read-Only-Memory. The Control Console operating procedures may be found in the Model 70 User's Manual, Publication Number 29-261.

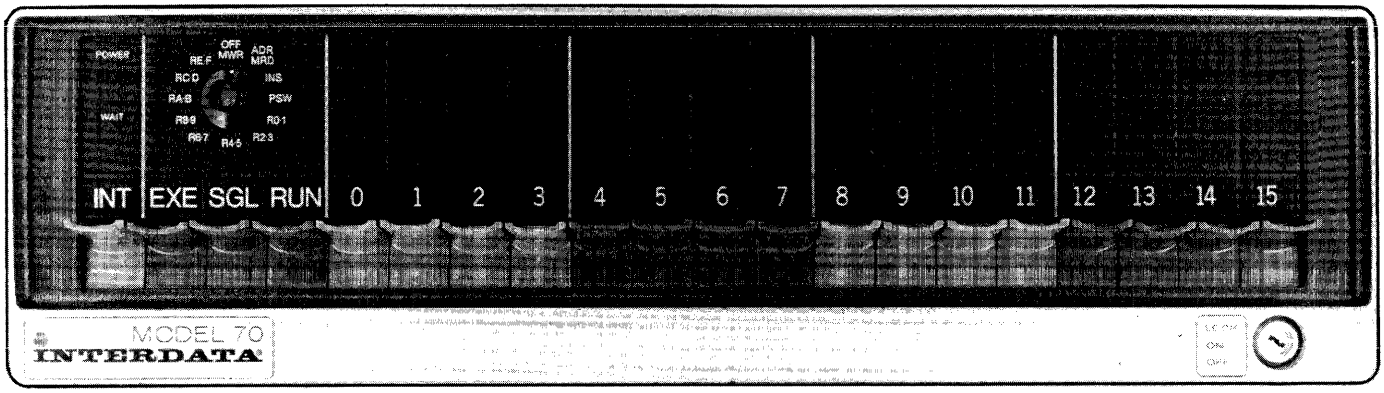


Figure 17. Control Console

5.1 Block Diagram Analysis

Refer to the block diagram on Figure 18. The Processor Multiplexor Bus is shown on the left, the Display System device controller is shown in the center, and the Control Console is shown on the right side.

The address logic is shown in the upper left area of the block diagram. On receiving a request for service via the EXEcute switch and the CATN signal, the Processor outputs the eight-bit display address (X'01') on Data Lines D08:15. This is followed by the ADRS control line which causes the decoded address to be strobed into the Address Storage flip-flop. The set output from this flip-flop enables all other I/O commands into the display controller logic.

Data to the Control Console is transmitted one byte at a time. The first byte is output on Data Lines D08:15, and the Data Available (DA) control line is raised. This command causes the first byte of data to be strobed into Bits 8 through 15 of Display Register Two. The DA line is then dropped, and the two-stage byte counter is incremented. The second byte of data is then placed on Data Lines D08:15, and the DA activated again. This process is repeated four times. Each time the display is addressed, the byte counter is automatically reset to zero for the first byte of data.

Data from the Input Register data switches is read into the system one byte at a time via Data Lines D08:15. On raising the Data Request (DR) control line, Bits 8 through 15 of the data switches are read into the system. The DR command is then dropped and the one-stage byte counter is toggled, enabling the second byte of data. The DR control line is again activated and Bits 0 through 7 of the data switches are read. The one-stage byte counter is automatically reset when the display is addressed.

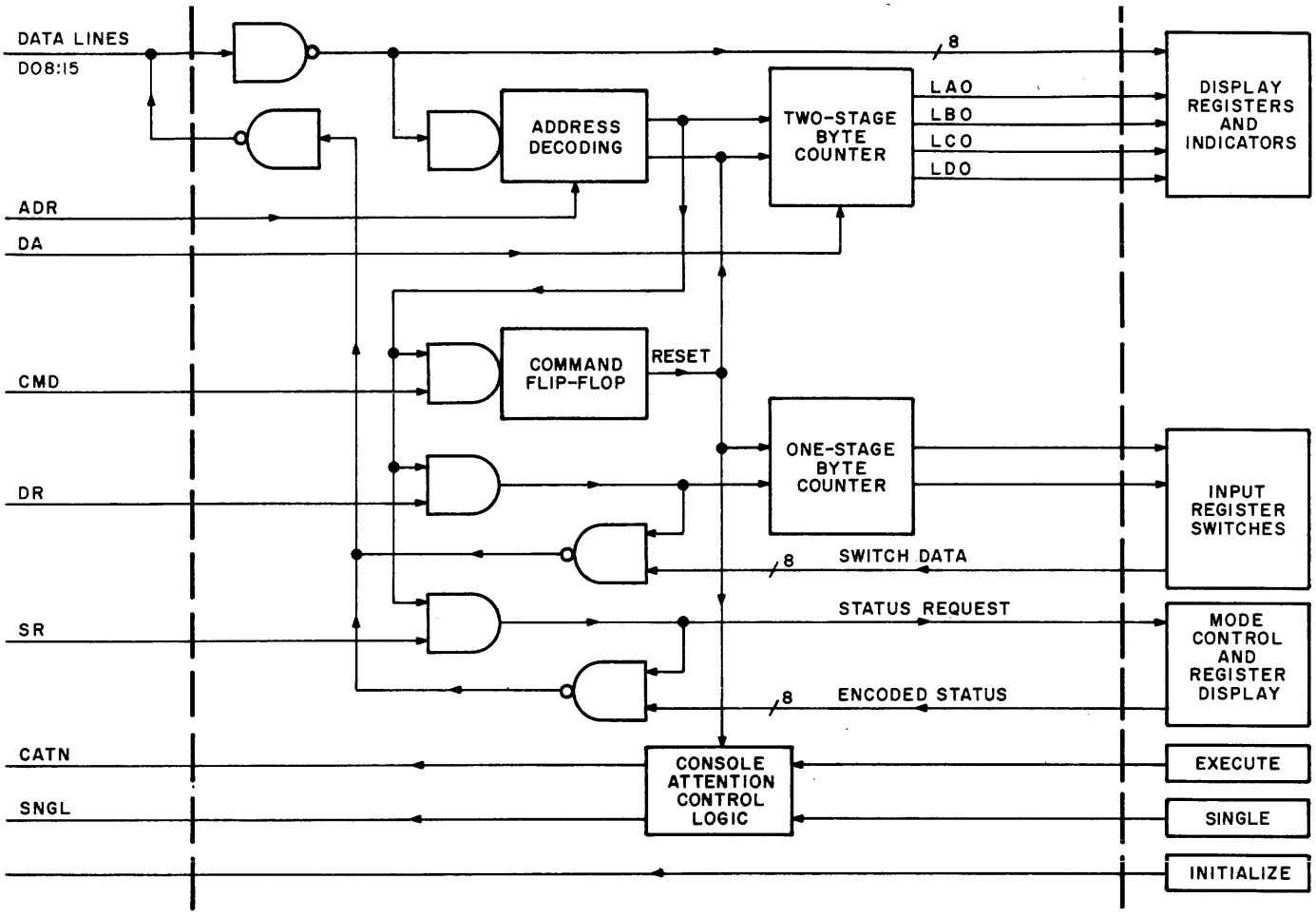


Figure 18. Display Controller Block Diagram

The status of the control and register switches is read into the system as a single byte of encoded data by raising the Status Request (SR) control line. The twelve positions of the register display rotary Function switch are encoded into Bits 4:7 of the status byte and the Control switches are encoded into Bits 0:7. The status byte is read into the system on Data Lines D08:15. The 32 register display lamps and the 16 data switches may be I/O programmed by the user. An Output Command (OC) instruction causes the CMD control line to set a flip-flop that disables the byte counters from being reset when the device is addressed.

The control logic is shown on the bottom of the block diagram. Depressing the EXEcute switch sets a flip-flop in the console attention control logic (21N7). This generates a CATN signal to the Processor. On receiving CATN, the Processor addresses the display, which in turn resets the flip-flop.

The Single switch (SGL) causes the Single control line (SNGL) to go active after the EXEcute switch is depressed to signify the Single Step Mode of operation to the Processor. A user instruction is executed each time the EXEcute switch is depressed. The Initialize (INT) switch causes the resetting of the Processor, Display Panel and all I/O devices.

5.2 Addressing Logic

Refer to Sheet 21. The Control Console's device number is decoded from Data Lines D08:15 by the eight-input NAND gate at 21L3. The Address flip-flop (ADR)(21L5) toggles set on the falling edge of ADRS1. When the display is addressed, ASYN0 goes low (21B4). ASYN0 generates a return Sync, SYN0 on 23G8.

If the Command flip-flop at 21A2 is reset, SCLR0F goes low to reset the two-stage byte counter at 21D3 and the one-stage byte counter at 21A6.

5.3 Data Output

The two-stage byte counter at 21D3 is set to zero on Initialize (SCLR0), on an Output Command to the display (21D8), or when the display is addressed in the Normal Mode. The state of the two-stage byte counter, the Data Available lead (DA1), and the set output from ADRS are input to the 19-032 one-of-ten decoder. The outputs LA0, LB0, LC0, and LD0 correspond to the four states of the byte counter and enable the four bytes of the two display registers. The display registers are shown on 09-051D08, Sheet 2.

The DA0 control line causes Data Lines D08:15 to be gated onto the bi-directional SD00:07 Bus (GSD1A)(21K6). On 09-051D08, Sheet 2, LA0 gates SD00:07 into Display Register 2, Bits 08:15. LB0 gates the SD Bus into Display Register 2, Bits 00:07. LC0 gates into Display Register 1, Bits 08:15. LD0 gates into Display Register 1, Bits 00:07.

The GSD1A lead is delayed from the DA0 line so that the LX0 line will drop before the SD Bus drops. The trailing edge of the gated Data Available (DAG1 at 21C9) increments the two-stage byte counter.

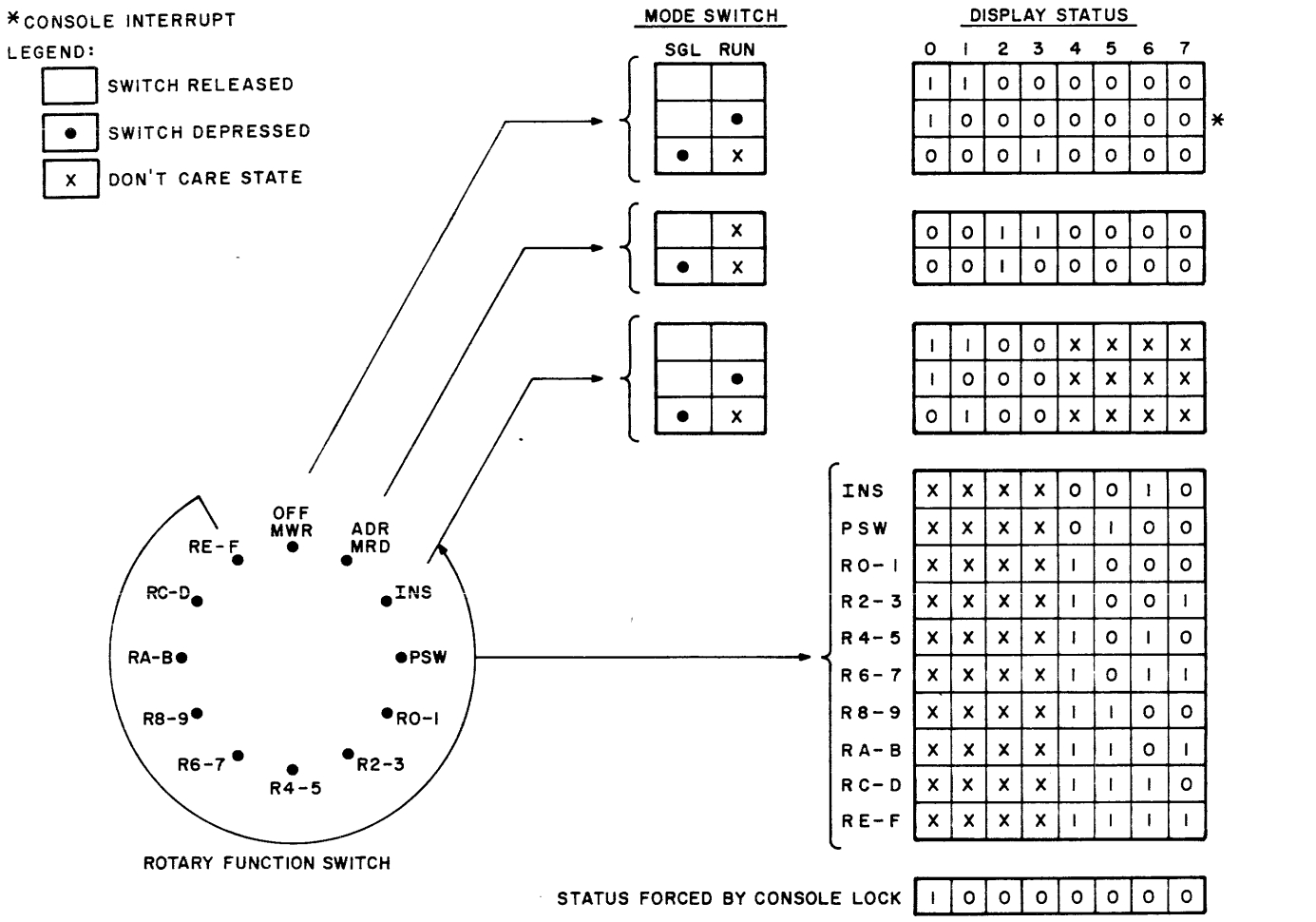
5.4 Data Input

The one-stage byte counter at 21A6 is cleared by SCLR0F on Initialize, Output Command, or when the display is addressed while in the Normal Mode. When the Data Request control line (DRG1) goes high, the least significant byte enable goes high to gate Bits 8:15 of the data switches onto the SD 00:07 lines. (The switches are shown on Sheet 2 of 09-051D08.) When the DRG1 line goes low, the flip-flop at 21A6 toggles set. The next time DRG1 goes high, Bits 0:7 of the data switches are gated onto the SD00:07 lines. DRG0 generates STRB0 (24G5) which gates the SD00:07 lines through the 19-038 dual four-to-one line multiplexors onto Bits 8:15 of the D Bus.

5.5 Status Input

The status byte encoding is shown on Sheet 1 of 09-051D08. The register display rotary Function switch is encoded into the least significant four bits of the status byte. The Control switches, SGL and RUN, in conjunction with the first two positions of the rotary Function switch, OFF/MWR and ADR/MRD, form the most significant four bits of the status byte. The status byte is gated onto the SD00:07 lines by the SRG0 lead. SRG0 generates STRB0 to gate the SD00:07 lines onto Bits 08:15 of the D Bus. Table 3 lists the status codes for the switch positions.

TABLE 3. DISPLAY STATUS BYTE ENCODING.



5.6 Control Logic

The EXEcute switch outputs, ESNO0 and ESNC0, are latched in the RS flip-flop at 21N4. The differentiated output sets the Console Attention flip-flop (CATN) at 21N7. This flip-flop is reset by ADSY0 when the Processor addresses the display.

When the SGL Control switch is latched and the rotary Function switch is in a position other than OFF/MWR or ADR/MRD, the SSGL1 lead is high. When EXEcute is depressed, the SNGL flip-flop toggles set. SNGL resets when SSGL1 is low and EXEcute is depressed.

6. TELETYPE CONTROLLER

The built-in Teletype device controller is used to interface an ASR/KSR 33 or 35 Teletype to the Processor. It converts serial eight level ASCII code (see Figure 19) to a parallel form for processing by the computer.

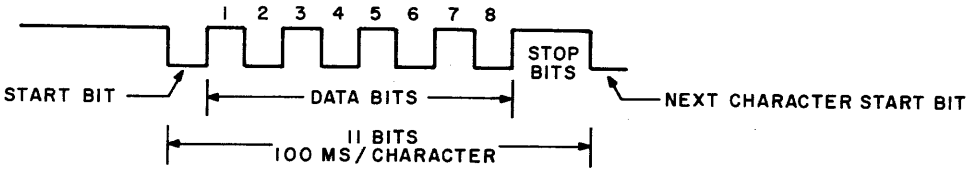


Figure 19. Serial ASCII Code U (Even Parity)

6.1 Block Diagram Analysis

Figure 20 is a block diagram of the Teletype controller. The control circuits consist of Command flip-flops (Read or Write, etc), circuits to direct the flow of information (Teletype Terminal to/from Processor), and the circuits to control the timer when transmitting/receiving to/from the Teletype Terminal.

The serial information received from the terminal, is sampled by the timer and strobed into the Shift Register. When the entire character has been shifted in, the data is placed in a byte Buffer Register from which the Processor takes the parallel data. When transmitting to the terminal, the information is placed directly in the Shift Register and then shifted out (serially) to the terminal.

6.2 Multiplexor Bus Communication

Communication between the Processor and the Teletype controller is via the low order eight bits of the D Bus. The bus receivers are shown on Sheet 22. The Data Lines D08:15 are buffered to form the DAL 00:07 leads. The device address, X'02', is detected by the gate at 22G1. On the trailing edge of ADRS1, the Address flip-flop toggles set, enabling the other control lines.

6.3 Data Output

The interface is conditioned to the Write Mode by an Output Command with D Bus Bit-12 set. The Read flip-flop at 22R5 resets. When the Data Available line (DA0) goes low, DAG0A (23B6) and TDAG0 (23B6) go low. DAG0A causes the 19-035 four-bit counter at 23M7 to be loaded with a '5'. TDAG0 resets the RDY flip-flop at 23E3. The two Stop Bit flip-flops (STP)(24D4) are set, the Start Bit flip-flop (STRT)(24E3) is reset and the data to be output (on DAL 00:07) is loaded into the two 19-030 four-bit shift registers (Sheet 24). When the DA0 control line is removed, the TMG flip-flop (23G4) toggles set. As soon as TMG sets, the oscillator at 23K1 starts. The CLK1 output (23M1) is a 300 nanosecond pulse occurring every 2.27 milliseconds or 440 Hz. CLK1 steps the two-stage counter (C1 and C2) to divide the frequency by four. Thus, the TDR0 signal at 23L5 is a 300 nanosecond pulse occurring every 9.09 milliseconds. Each pulse increments the four-bit counter at 23M7 and, as long as the counter does not equal all ones, shifts the 11 bit Shift Register (Sheet 24) left one position. The Counter counts up from 5 so that by the time it equals 15, the Shift Register has shifted ten places.

The DRS0 lead from the least significant bit of the Shift Register is gated with READ0 and TMG1 at 22C7 forming the TRNS0 lead to the Teletype.

When the Counter increments from all ones to all zeros, the Carry Output (EOC0) goes low. EOC0 clears the TMG flip-flop stopping the oscillator.

While TMG is set, BSY1 is high (23S9) indicating that the interface is busy serializing the eight bit character sent to it. See Figure 21.

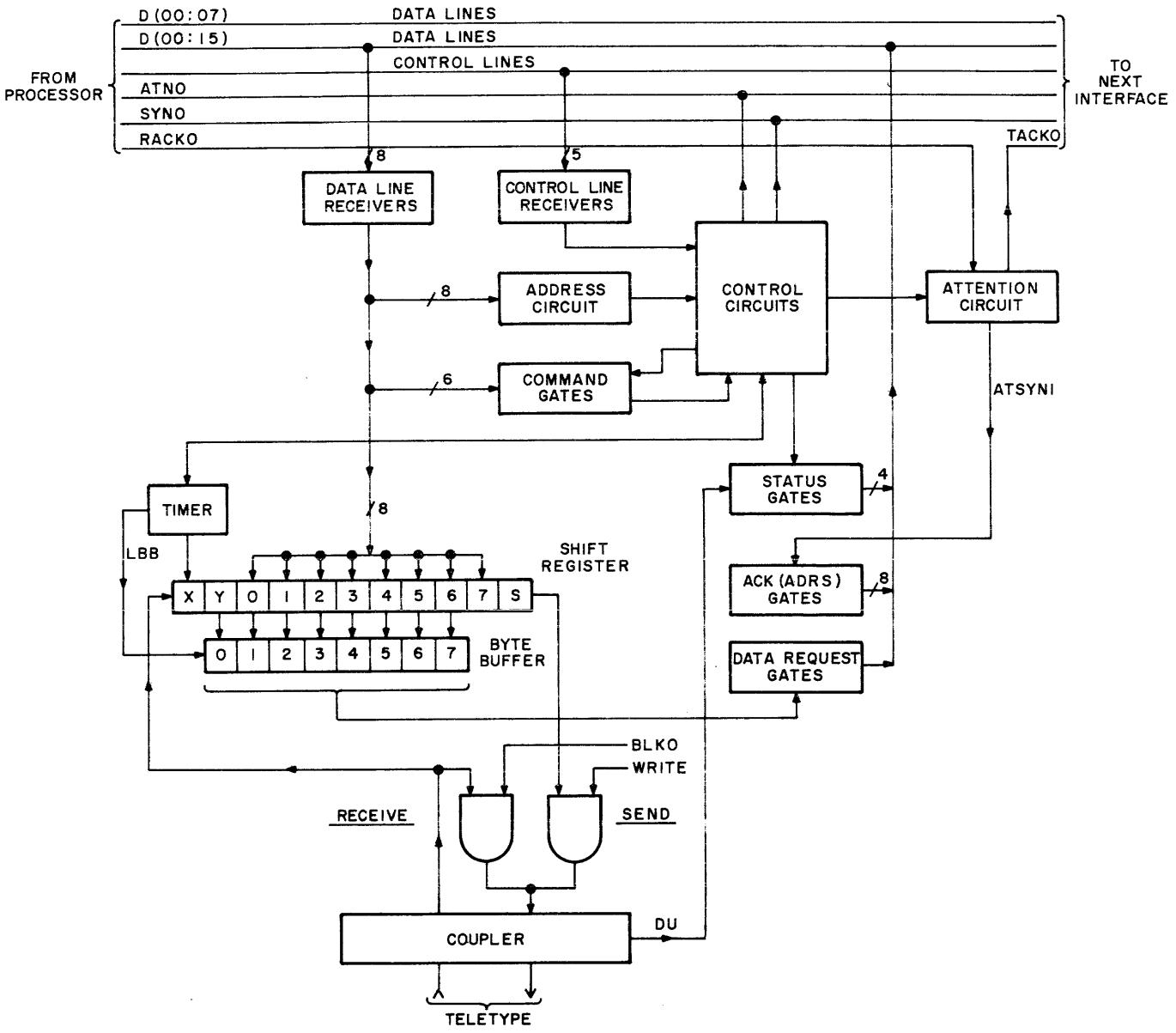


Figure 20. Teletype Controller Block Diagram

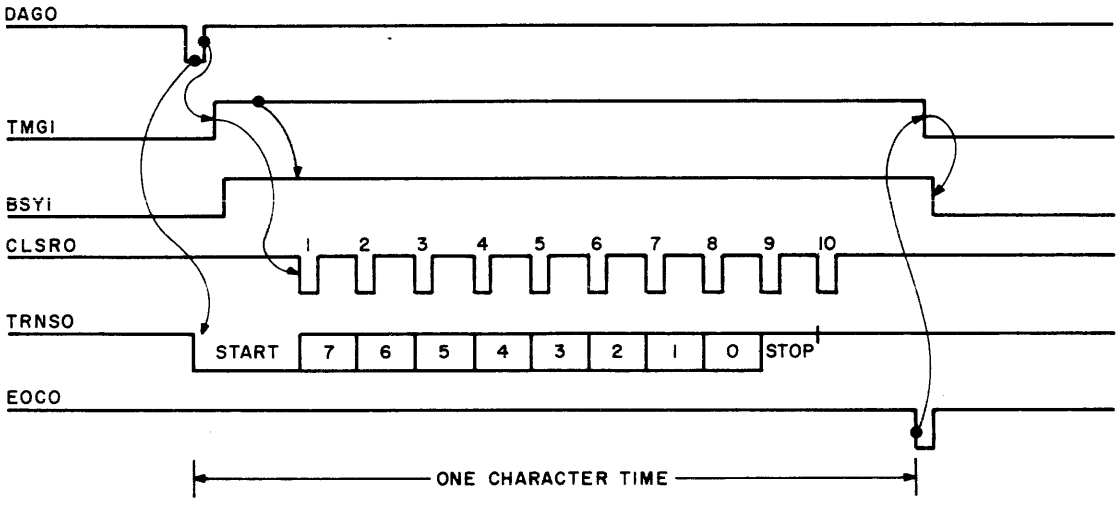


Figure 21. Write Timing

6.4 Data Input

The interface is conditioned to the Read Mode by Initialize or by an explicit Output Command with D Bus Bit-13 set. The Read flip-flop (22R5) is set. In the Read Mode, the interface remains busy (BSY1=1) until a complete character is received from the Teletype. The data input line (DD0)(22F8) is quiescently high. When the Teletype starts to transmit a character, the DD0 line goes low for one bit period, 9.09 milliseconds, to signify the start of a character. Following this start bit are eight data bits and at least two Stop bits. See Figure 22.

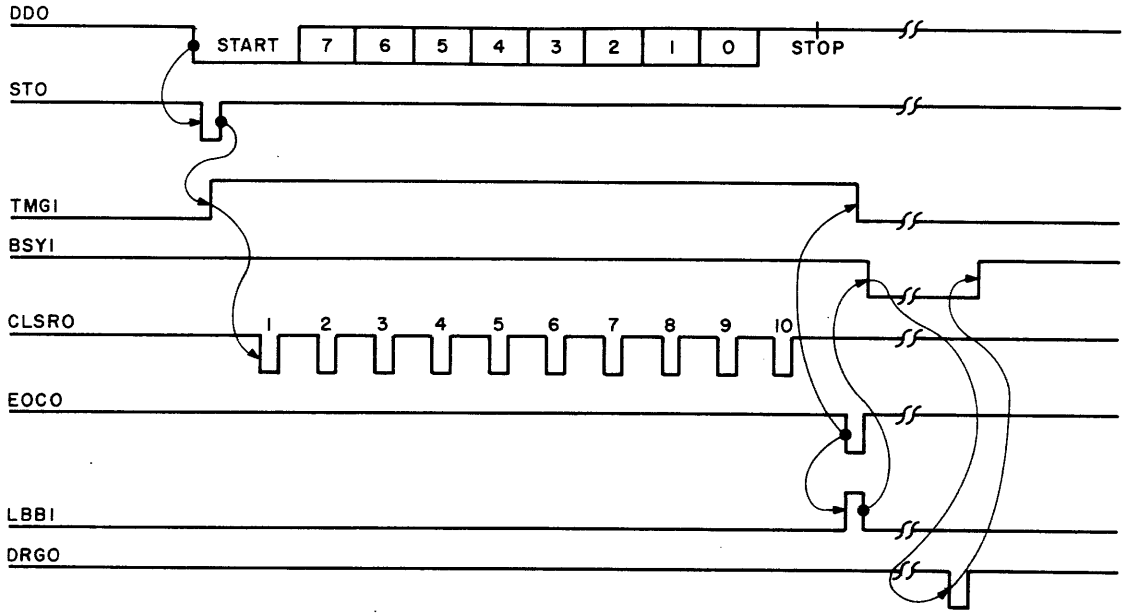


Figure 22. Read Timing

DD0 causes the RDY flip-flop at 23E3 to momentarily set. This transition is differentiated to produce the ST0 pulse (23G4). ST0 sets TMG, clears RDY, and loads the four-bit counter at 23M7 with '5'. When TMG sets, the oscillator at 23K1 starts. After 4.5 millisecond, the first TDR0 pulse occurs. TDR0 produces CLSR0 which shifts the state of the DD1 line into the 11-bit Shift Register (24D1). The first bit that shifts in is the start bit that started the timer. After ten shifts, the start bit will be in Bit-7 of the Data Register. The EOC0 pulse generates LBB1 (23R6) to clock the eight bits from the Shift Register into the byte buffer (24G1).

The signal BSY1 is high until the LBB1 pulse toggles the BSY flip-flop at 22L2 set. When the Processor takes the data from the byte buffer, the signal DRG0A clears the BSY flip-flop at 22L2 and BSY1 again goes active.

6.5 Status and Commands

The interface is initialized to the Read Mode and is consequently busy until a character is processed. If another character is processed before a Data Request is received, the ERR flip-flop (22M2) toggles set to indicate the overflow condition.

The Block Command sets the BLK flip-flop (22L4). In Block Mode, serial data received from the Teletype is not echoed back. In the Unblock Mode, serial data received is turned around by the gate at 22C8 and transmitted back to the Teletype.

In the Write Mode, the interface is busy only for the time that TMG is set.

The Device Unavailable status bit (DU) is active when the Teletype is off-line or powered down. The DU network on Sheet 22 senses the open circuit condition from Pin 10 of the stub cable and raises the DU1 lead.

The Break status occurs when a Stop Bit is not received from the Teletype. When the EOC0 pulse occurs, the input data line should be high to set the RDY flip-flop (23E3). If TMG resets, and RDY did not get set, the BRK1 signal at 22D9 goes high.

Teletype status is gated onto Data Lines D08:15 by the 19-038 Dual four-to-one line multiplexors on Sheet 24, when the ADRSA1 and ADRSB1 gating leads are both low. These leads are generated at 23F6 as follows:

	ADRSA1	ADRSB1
TTY Status Request	0	0
TTY Interrupt Acknowledge	0	1
TTY Data Request	1	0
Display Data Request	1	1
Display Status Request	1	1

TABLE 4. TELETYPE STATUS AND COMMAND BYTE

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE	ERR		BRK		BSY	EX		DU
COMMAND BYTE	DISABLE	ENABLE	UNBLOCK	BLOCK	WRITE	READ		

ERR The Error bit is set when a character is not taken from the controller buffer before another character is assembled.

BRK The Break bit is set at the end of one character time when the line is held in the space condition for a period greater than a character period.

BSY Read Mode - The Busy bit is normally set and is reset when data is available for transfer to the Processor. Write Mode - The Busy bit is normally reset and is set when data is being transferred to the terminal.

EX The Examine bit is set when BRK or ERR is set.

DU The Device Unavailable bit is set when the terminal is powered down or in Local Mode.

DISABLE Disables device interrupts; allows queuing of interrupts.

ENABLE Enables device interrupts.
Note: A command byte with both Bits 0 and 1 set Disarms the interface (no interrupt queuing).

UNBLOCK Allows Printer to print data entered via keyboard or tape reader.

BLOCK Disables the Unblock feature.

WRITE The interface is placed in the Write Mode.

READ The interface is placed in the Read Mode.

6.6 Interrupt Circuit

The Teletype controller is prevented from queuing interrupts when the Arm flip-flop is reset (24B3). The interface is disarmed by SCLR0 or by the Disarm Output Command. The Arm flip-flop sets whenever an Output Command Enable or Disable is received. If armed, the ATN flip-flop sets whenever an Output Command Enable or Disable is received. If armed, the ATN flip-flop (24B7) also sets on the negative going transition of BSY1. If EBL is also set (24B8), the ATN0 lead at 24C9 goes low.

The Processor responds to an ATN by executing an Acknowledge Interrupt. The ACKA000 lead (20N6) goes low. This lead is connected to the RACK0 input (24A1) to the Teletype controller if the Teletype is to be first in priority. When RACK0 goes low, if ATN and EBL are set, the signal ATSYN0 goes low. If either ATN or EBL is reset, the TACK0 lead to the next device controller in the daisy chain goes low.

ATSYN0 toggles the ATN flip-flop reset and gates the Teletype's device number onto Data Lines D08:15, by way of the DAL 00:07 inputs to the 19-038 multiplexors on Sheet 24.

7. MAINTENANCE

This section describes maintenance procedures which may be used to check and, if necessary, adjust the Processor.

7.1 Clock Timing

There is only one adjustment associated with the system clocks. The variable Capacitor C9 on the I/O mother-board is very stable and should not require field adjustment. The adjustment should only be changed after the test indicates that it is out of tolerance and there are no faulty components in the system.

1. Force the RD Register to all ones by grounding the DISR0 signal at Pin 217-1 on the ROM board and depress the Initialize switch.

NOTE

Exercise care in grounding points in the digital system as some components may be damaged if the wrong pins are grounded.

2. Use an oscilloscope to check that the period of the SCL0 at Pin 211-1 on the I/O mother board is 250 nanoseconds. Adjust Capacitor C9 to get the 250 nanosecond period. The pulse width is dependent on a decoded state of the clock counter. Check the associated logic if there is a discrepancy.

3. Check that the following system clocks occur at the same time as SCL0:

DCL0	121-0
RCL0	225-1
RDSTB0	228-0

If a discrepancy occurs, check the associated logic.

4. Check that T21 and T21NS1 occur approximately 80 nanoseconds after the rising edge of SCL0 and last for approximately 50 nanoseconds. These clocks are available on the I/O mother-board at Pins 229-0 and 123-0 respectively. These clocks are also decoded states of the clock counter.

5. Check that T2SYS1 on the ROM mother board (12-087) is a 30 nanosecond pulse occurring during T21 and about 20 nanoseconds after the rising edge of T21.

6. Check that STCLK1 is a 30 nanosecond pulse occurring during DCL0 and approximately 25 nanoseconds after the falling edge of DCL0 (06-107 on the ALU mother-board).

7. Remove the ground from Pin 217-1 on the ROM back panel.

7.2 Memory Timing Adjustments

Refer to Figures 15 and 16. Timing adjustments are checked by grounding Console Attention (CATN0), Pin 238-1 on the I/O Control Board at Position 05 in the Processor chassis. The Control Console rotary Function switch should be placed in the Memory Read (MRD) position with the Single (SNG) switch depressed. Sync may be obtained from the START1 Test Point on the Memory Control board at Position 04 of the Processor chassis.

Timing for the Memory Control is generated by the 19-042 delays at 30C3 (A102) and 30C5 (A101). These delays adjust the set time of the DUA and the XMB or PMB flip-flops.

The output at Pin 04 of A102, a high going pulse, should be approximately 200 nanoseconds such that the DUA flip-flop is set for one clock period (250 nanoseconds) following the first SCL1 pulse after memory start.

The output at Pin 12 of A102, a low going pulse, should be approximately 400 nanoseconds such that a 70-100 nanosecond Memory Busy Clear Pulse (MBCLIP) occurs at Pin 13 of A101, approximately 450 nanoseconds after memory start. The MBCLIP should occur between the second and third SCL1 following memory start. Its function is to clear the XMB or PMB flip-flops depending on whether the Selector Channel or the Processor started memory.

Timing for memory modules (ER0, LR0, INH0, and W0) is indicated in Figure 16. These pulses are generated by the 19-042 delays at 30G3 (A103), 30G7 (A104), and 30C7 (A105). All signals are initiated by the START1 pulse.

ER0, generated by the A103 delay, should be 300 nanoseconds at 204-0. Pin 12 of A103 should be a 60 nanosecond pulse which determines the time between the falling edges of the ER0 and LR0 pulses.

The output of the A104 delay, DLAYB (Pin 13) and DLAYC (Pin 05), determine the start of the INH0 and W0 pulses respectively from the rising edge of the ER0 pulse. They should be 120 and 180 nanoseconds respectively.

Finally, the width of the INH0 and W0 pulses is determined by the delays at A105, Pins 13 and 12 respectively.

All delays are factory adjusted and should not require field adjustment.

7.3 Teletype Controller

Refer to the vendor operating and service manuals for maintenance information on the terminal being used. The overall operation of the terminal and interface can be checked by running the 06-004 test program.

The only adjustment on the Teletype controller is the potentiometer (R63) on the oscillator. A check of the timing can be made as follows:

1. Initialize the interface.

2. Connect an oscilloscope to C21, Pin 6 of IC 14
   Vertical scale: 2 volts/centimeter
   Horizontal scale: 10ms/centimeter

3. Generate a continuous stream of data from the terminal by tape or by the REPEAT key function of the keyboard.

4. Adjust the oscillator for the waveform shown on Figure 23.

7.4 Overall Processor Test

Use the 06-106 Model 5 Test Program to perform a comprehensive test of the Processor.

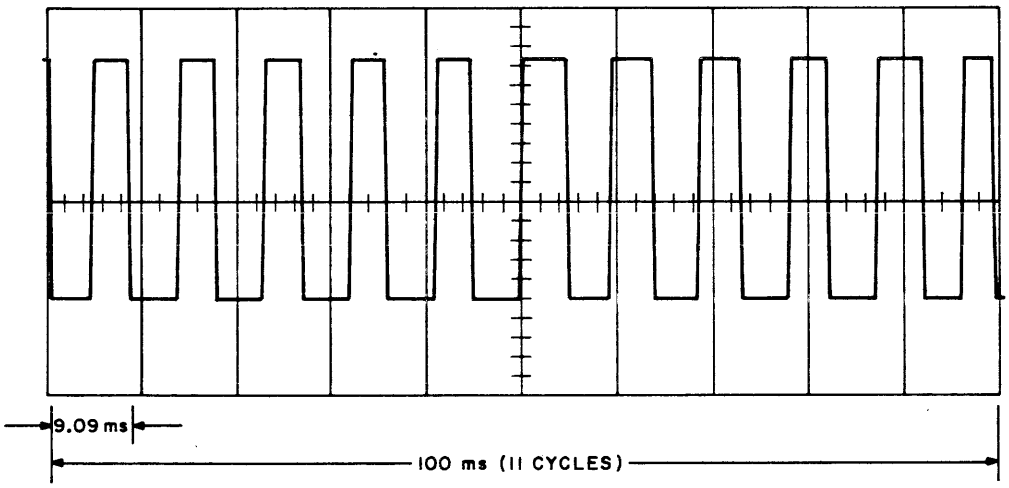


Figure 23. Character Timer Adjustment

8. MNEMONICS

The following list provides a brief description of each mnemonic found in the Model 70 Processor. The source of each signal on Schematic Drawing 01-051D08, is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
ABRT0	Abort Phase Two sequence	4N4
ACKA00	Acknowledge Interrupt Control Line	20N5
AD	TTY Address flip-flop	22J1
ADMH1	TTY Address Select	22H1
ADR	Display Address flip-flop	21L5
ADRS0	Address Control Line	20L5
ADRSA1	Display/TTY D Bus gating lead	23E6
ADRSB1	Display/TTY D Bus gating lead	23E5
ALRM131	Data Parity Fail Alarm	17K7
ALRM141	Instruction Parity Fail Alarm	17L7
ARLM151	Early Power Fail Alarm	17N7
AMOD0	Address Modification	9A2
AR00:15	Arithmetic Register	Sheet 12
ARST1	Automatic Restart	18J1
AST0	TTY Timer Start	23G3
ASYN0	Display Address Sync	21B4
ASYN0A	TTY Address Sync	23B5
ATN0	I/O Attention Test Line	18N1, 24C8
ATSYN0	TTY Interrupt Acknowledge Sync	24B5
B	B Bus	Sheets 11,13, 16,20,29
B130	B Bus Bit-13	4F4
BANK	Bank flip-flop	12M9
BLKDT0	Block Serial Data Transfer	22N4
BRA1	Branch	18H8
BRK1	Line Break	22D9
BSY	Busy flip-flop	22L2
BSY1	Busy	23M9
C1, C2	TTY Time Counter flip-flops	23J4, 23J5
CATN0	Console Attention	21N9

MNEMONIC	MEANING	SCHEMATIC LOCATION
CC121:151	Condition Code Bits 12:15	Sheet 17
CEMT0	Counter Empty	27C9
CG	Gated ALU Carry	Sheet 14
GI1	Carry In	14A5
CL070	Control Line 7	19D5
CLK0	System Clock Oscillator Output	19B6
CLK1	TTY Timer Clock	23M1
CLKOFF0	Clock Off	19B6
CLKSTP0	Clock Stop	19M4
CLMF	Clear Memory flip-flops	30H8
CLR0	Clear Function	9N4
CLRA0	Clear ROM Address Higher	5C3
CLRB0	Clear ROM Address Lower	5B3
CLRBK0	Clear Bank and Utility flip-flops	12K9
CLRIR0	Clear Instruction Register	9A7
CLRST0	Clear Memory Timer	30J3
CLSR0	Data Register Clock	23R6
CMD0	Command Control Line	20M5
CMDG0	Gated Command Line (Display)	21D9
CMDG0A	Gated Command Line (TTY)	23B8
CMND1	Command	13G7
CMODE	Counter Mode flip-flop	13M8
CP	Propogated ALU Carry	Sheet 14
CRY0	Carry	15A5
CS1	Cross Shift	8M6
CSL0	Command Shift Left	13J8
CSR0	Command Shift Right	13G8
CSV1	Carry Save	14D7
CTEST1	Command Test	17M3
CTF1	Change Test Flags	14S9
CTLT21	Counter is Less than Two	13K7

MNEMONIC	MEANING	SCHEMATIC LOCATION
CTONE1	Counter Equals One	27C9
CTR121:151	Counter Bits 12:15	Sheet 27
CWR0	Change Write to Read	27R9
D	D Bus Bits	Sheets 16,20,24
D1	DO Micro-Instruction	8C5
DA0	Data Available Control Line	20M5
DAG0	Gated Data Available (Display)	21C8
DAG0A	Gated Data Available (TTY)	23B6
DAL	Data Available Lines	Sheet 22
DC0	Data Channel Request	18R1
DCAK0	Data Channel Acknowledge	20K5
DCL0	Destination Clock	19M9
DD0	Device Data (TTY)	22F8
DDC1	DO or Command	8B5
DECTR0	Decrement the Counter	13F8,18E9
DIFF1	Different Signs	17G3
DISB0	Disable Memory Start	9E8
DISR0	Disable ROM	6A7
DIV0	Command Divide	13J8
DLAYA0	ER0/LR0 Delay	30F4
DLAYB1	ER0/INH0 Delay	30G8
DLAYC1	ER0/W0 Delay	30F8
DR0	Data Request Control Line	20N5
DR001B:071B	TTY Data Buffer Register	Sheet 24
DRD0	Data Channel Read/Write Test Line	18M1
DRD081	DO and RD Bit-8	8J9
DRG1	Gated Data Request (Display)	21C8
DRG0A	Gated Data Request (TTY)	23B7
DRS0	Data Register Start Bit	24E4
DST0	I/O Device Clock Stop	4A4
DTEST0	True Interrupt Test on Phase 2 DO	18M9

MNEMONIC	MEANING	SCHEMATIC LOCATION
DUA0	Device Unavailable	30D4
EBL	Abort Enable flip-flop	4S3
EN	ROM Page Enable	Sheet 6
EN0	External Memory Request Enable	30L4
ENABL1	TTY Interrupt Enable	24E8
EOC0	TTY End Of Character Detect	23M7
EPF0	Early Power Fail	19G3
ER0A	Early Read, memory timing lead	30G4
ER1	Early Read, memory timing lead	30E6
ERR1	TTY Interface Overflow Error	22M2
ESNC0	Execute Switch Normally Closed Contact	21N3
ESNO0	Execute Switch Normally Open Contact	21M3
EX1	Examine Status	22N1
EXES1	Execute Switch Depressed	21N5
EXTCLK0	External Clock Input	19E6
FAST0	Fast External Interrupt Test Line	18B5
FLR	Flag Register	Sheet 17
FMDBY	Memory Data Register Busy flip-flop	30N4
FMDUA	Memory Data Unavailable flip-flop	30J4
FPMBY	Processor Memory Busy flip-flop	30M4
FRCLOC0	Force Location Counter to be Source and Destination	9J4
FRNS1	Flag Register Bits 14 and 15 Not Set	17N5
FST1	Fast External Interrupt Test Line	18B8
FSYN0	False Sync	4F2
GA	Gated AR Input to ALU	Sheet 12
GB	Gated B Bus Input to ALU	Sheet 14
GCMND1	Clocked Command Micro-Instruction	13L7
GDEST1	Gated Destination Enable	10D3
GDEST1A	Gated Destination Enable	18D2
GDRL0	Gated Data Request Lines (Display)	23B5

MNEMONIC	MEANING	SCHEMATIC LOCATION
GDROM0	Gate DROM Output	9H7
GIO1	Gated I/O Control Line	4A2
GMD160	Gated MD Bit-16	27R5
GMSIR1	Gate MS Bus to IR	28A3
GMSMD1	Gate MS Bus to MDR	26B2
GO	GO flip-flop	19D9
GOBRA0	GO Branch	18H9
GR	Gate Read Register Stack Enable	Sheet 10
GTP20	Go to Phase 2	9D8
GTP30	Go to Phase 3	9G7
GW	Gate Write Register Stack Enable	Sheet 10
HDEST0	Load SRH	8D7
HIDU0	ROM Read Inhibit	8A1
HW0	Halfword I/O Test Line	9K1
ILEG0	Illegal Instruction Detect	8K8
INH0	Inhibit, memory timing lead	30C9
INHINC0	Inhibit RAL Increment	5R2
INIT0	Initialize Switch	19A4
INTA0	Interrupt Set A	17R9, 18N3
INTB0	Interrupt Set B	18R4
IR	Instruction Register	Sheet 28
IRA1	Clear, Jam, and Alarm DO Option Timing Lead	9M3
JACC0	Jam Alarms to Condition Code	9L4
JCL1	ROM Address Jam Clock	9H7
KILDST0	Kill Destinations	4N4, 13N9
KSKIP0	Reset Skip flip-flop	9F7
LA0	Load Display Byte A	21F9
LARCLK1	AR Loading Clock	12A2
LAR1	Load AR	8F9
LARYS0	Load AR from YS	9C3
LB0	Load Display Byte B	21F9

MNEMONIC	MEANING	SCHEMATIC LOCATION
LBB1	Load TTY Byte Buffer	23N6
LC0	Load Display Byte C	21F9
LCC0	Load Condition Code from FLR	9M4
LD0	Load Display Byte D	21F9
LD01	Load Destination Address 0 (RAH)	18D8
LD10	Load Destination Address 1 (RAL)	18E8
LDIO1	Load I/O	20K3
LDCTR0	Load CTR	8C7
LDCLR0	Load FLR or CLR	17R4
LDFLR0	Load FLR	17S3
LFLR0	Load FLR	8D7
LINE	I/O Control Line flip-flop	4C4
LIR0	Load IR	8D7
LLOC0	Load LOC	8G8
LMAR0	Load MAR	8G9
LMAS1	Load MAS	25A3
LMDH1	Load MDR High 0:7	26A5
LMDL1	Load MDR Low 8:15	26A7
LMDR1	Load MDR	8F8
LOAD1	Load Micro-Instruction	8D5
LPSW0	Load PSW	8H8
LR0	Late Read, memory timing lead	30E6
LRAH0	Load RAH	18C8
LRAL0	Load RAL	18K9
LSRL0	Load SRL	8D7
LYD0	Load YS, YD or YDP1	8C7
M1	ALU Control Line	13J5
MA	Memory Address Bus	Sheet 25
MALF1	Machine Malfunction	17R9
MAR	Memory Address Register	Sheet 25
MB0	Memory Busy	30M3

MNEMONIC	MEANING	SCHEMATIC LOCATION
MBCL0	Memory Busy Clear	30C4
MBCLIP	Memory Busy Clear Pulse	30C6
MCLR1	Memory Clear Input	30A1
MD	Memory Data Bus	Sheet 26
MD0	Multiply or Divide	13H9
MDR	Memory Data Register	Sheet 26
MDRCLR0	MDR Clear	26A2
MNB1	Memory Enable	30M7
MPY0	Multiply	13H7
MS	Memory Strobe Bus	Sheet 26
MSK1	Mask IR4 and CC Test Line	29R8
MSST0	Memory Contention Clock Stop	4L2
MST0	Memory Contention Clock Stop	4J2
MWPW0	Memory Write or Priviliged Write	8B9
NA0	No AR to ALU	13R4
NOCS0	No Cross Shift	9K3
NOMEM0	Surpress Memory Read	9E9
OP	Operation Length flip-flop	4L9
OSC1	Oscillator Output	19C8
P00	Phase Zero	9K4
P10	Phase One	9D7
P21	Phase Two	9F4
P30	Phase Three	9G5
PC0	Phase Counter Bit-0	9F3
PC1	Phase Counter Bit-1	9F3
PERR1	Parity Error Detect	27J6
PF0	RAL Increment Internal Carry	5R8
PFDT0	Power Fail Detect	19D4
PFF1	Parity Fail	27J9
PHEN1	Phase Change Enable	9F9
PMB	Processor Memory Busy flip-flop	30R5

MNEMONIC	MEANING	SCHEMATIC LOCATION
POFF0	Power Off (Switch Contact)	19A4
POW0	Command Power Down	19L2
POWDN0	Power Down	19J2
PPF0	Primary Power Fail	19J3
PR5	Pullup Resistor	12N9
PRTECT0	Memory Protect Test	27N9
PSEL0	Processor Selected	30L8
PSTART0	Processor Memory Start	30N7
PSW	Program Status Word	Sheet 29
RA1	User's Stack Read Enable	10H8
RACK0	Receive Acknowledge Control Line	24A1
RACLR0	ROM Address Register Clear	9B7
RAH	ROM Address Higher	Sheet 5
RAL	ROM Address Lower	Sheet 5
RB1	User's Stack Read Enable	10F8
RCL0	ROM Address Clock	19L9
RD	ROM Data Register	Sheet 8
RDSTB0	RD Strobe	19L9
RDY0	TTY Ready	23E3
READ	TTY Read flip-flop	22R5
READ	Memory Read flip-flop	27N9
REQ0	External Memory Request	30L1
RMA1	Micro Stack Read Enable	10F4
RMB1	Micro Stack Read Enable	10F4
RMS0	Read Micro Stack	10D5
RR0	RR User Instruction	4M8
RS0	RS User Instruction	4M8
RUN	Run flip-flop	8J7
RYD1	Read YD	10A5
RYS1	Read YS	10C5
S	S Bus	Sheet 14

MNEMONIC	MEANING	SCHEMATIC LOCATION
S01,S11,S12	ALU Control Lines	Sheet 13
SCL0	System Clock	13G1,19J9
SCLR0	System Clear	19N1
SD	Display Status and Data Bus	Sheet 21
SFLR120	Set FLR12 (C)	17D4
SFLR130	Set FLR13 (V)	17G4
SFLR140	Set FLR14 (G)	17J3
SFLR150	Set FLR15 (L)	17L4
SHI0	Input High Data Switches	21A9
SHCA1	Shifter Control Line	12B9
SHCB1	Shifter Control Line	12C9
SHL1	Shift Left	8N6
SHOT1	Bit Shifted Out	13C9
SHR1	Shift Right	8N6
SLO0	Input Low Data Switches	21A9
SNGL0	Single Mode	21H8
SR0	Status Request Control Line	20R5
SRAH	Set RAH	Sheet 4
SRAL	Set RAL	Sheets 4,9
SRD	Set RD	Sheets 6,7,8
SRDY0	TTY Set Ready	23D3
SRG0	Gated Status Request (Display)	21B7
SRG0A	Gated Status Request (TTY)	23B7
SRH	Shift Register Higher	Sheet 15
SRHM01	SRH Mode Control Lead	15L4
SRHM11	SRH Mode Control Lead	15M4
SRL	Shift Register Lower	Sheet 15
SRLCI1	SRL Carry In	15S4
SRLM01	SRL Mode Control Lead	15R4
SRLM11	SRL Mode Control Lead	15N4
SSGL1	Set SNGL flip-flop	21H7

MNEMONIC	MEANING	SCHEMATIC LOCATION
SSKIP0	Set Skip	9B7
SSMEM1	Solid State Memory Control Line	30J1
ST0	TTY Data Start	23J3
START1	Memory Start	30G2
STBR1	Store or Branch	4N8
STF0	Set Test Flags	8R7
STFL0	Set Test Flags	8R9
STOP0	Clock Stop (Phase Zero)	9C4
STPA0	Memory Contention Clock Stop	4J4
STPC0	MPY, DIV, and RPT Clock Stop	13R9
STPSYS	Stop System flip-flop	19J4
STRB1	Display/TTY D Bus Strobe	23E6
SUB0	Subtract	13K5
SV0	Set V Flag	4F4
SVAC0	Save Adder Carry	8S7,13B4
SVSC0	Save Shifted Carry	8S6,13A4
SYD	Decoded YD Field Bits	Sheet 10
SYN0	System Synchronize	4E1, 23G7
SYNCH0	Receive Synchronize	4D4
SYS	Decoded YS Field Bits	Sheet 10
SYSCL1	System Clock	19E8
T21	Time 2 (Clock)	19J9
T21NS1	Unskipped T21	19K9
T21SY1	T21 and SYSCL1	9A6
TACK0	Transmit Acknowledge	24A9
TDAG0	TTY Gated Data Available	23B6
TDR0	Toggle TTY Data Register	23L5
TEST1	Test Micro-Instruction	18M8
TESTA	Abort Test flip-flop	4M3
TFA	Clock Timer flip-flop A	19G7
TFB	Clock Timer flip-flop B	19G8

MNEMONIC	MEANING	SCHEMATIC LOCATION
TIR0	Toggle IR	28S3
TMG0	TTY Timing Gate	23G4
TP1	Toggle TTY Data Register	23H1
TRA	RAL	Sheet 5
TRNS1	TTY Data Transmit	22C8
TTEST0	True Testable Function	18H5
UDIO0	Unload I/O	18D5
UIR41	Unload IR 08:11	18F3
ULAR1	Unload AR 00:07	13N5
ULAR1A	Unload AR 08:15	13N5
UMDR1	Unload MDR	18C4
USRH0	Unload SRH	18E5
USRL0	Unload SRL	18D5
USTRB0	Unload Register to B Bus	18C5
UT	Utility flip-flop	12L9
W0	Write, memory timing lead	30B9
WA1	Write User Stack Enable	10S8
WAIT0	Wait flip-flop	8L7
WAIT1	Wait flip-flop	21R4
WB1	Write User Stack Enable	10R8
WMA1	Write Micro Stack Enable	10G4
WMB1	Write Micro Stack Enable	10G4
WMS0	Write Micro Stack	10J5
WRT0A	Memory Write Control Line	27L2
WYD1	Write YD	10H5
WYS1	Write YS	10J5
X0	Conditional Cross Shift	9R9
XMBS0	External Memory Busy (Slave)	30M5
XMBY0	External Memory Busy	30L5
XSTART0	External Memory Start	30L6

SERIES 5 MEMORY MAINTENANCE SPECIFICATION

1. INTRODUCTION

This specification applies to the INTERDATA Series 5 Memories listed in Table 1.

TABLE 1. SERIES 5 MEMORIES

INTERDATA PART NUMBER	SPEED	SIZE	CONFIGURATION
02-211F01	1.0 us	4KB	4K X 17*
02-211F02	1.0 us	4KB	4K X 16

*The seventeenth bit is a parity bit.

2. SCOPE

This specification describes the operation of the Series 5 Memory. It does not include Processor to Memory Interface information, except the inputs necessary to operate the Memory and the resultant outputs provided by the Memory. A brief review of core memory theory precedes the detailed circuit description. This specification also provides a block diagram analysis, timing information, troubleshooting and maintenance information, and a mnemonics list.

3. PHYSICAL DESCRIPTION

The Series 5 Memory consists of one mother-board (approximately 15" x 15") that can be installed in a card file on 0.75 inch centers. Figure 1 shows the physical location on the mother-board of the major circuit blocks comprising the Series 5 Memory. A back panel Map is shown in Functional Schematic 02-211D08, Sheet 6.

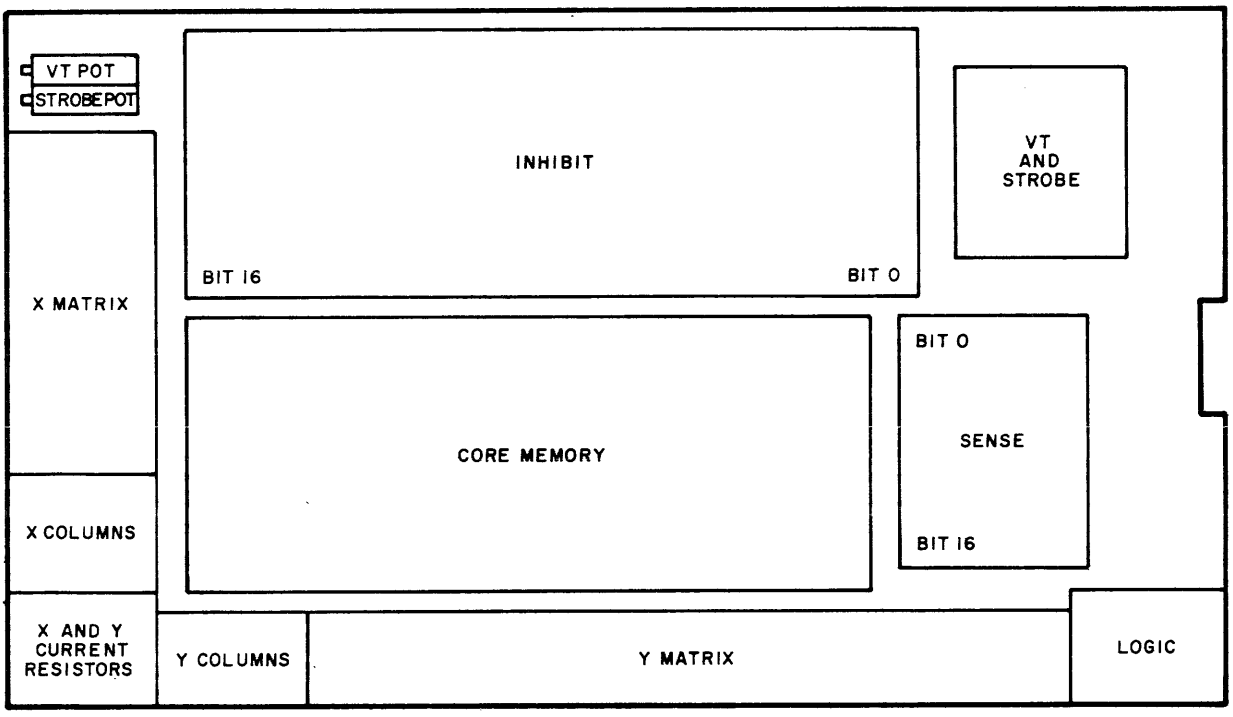
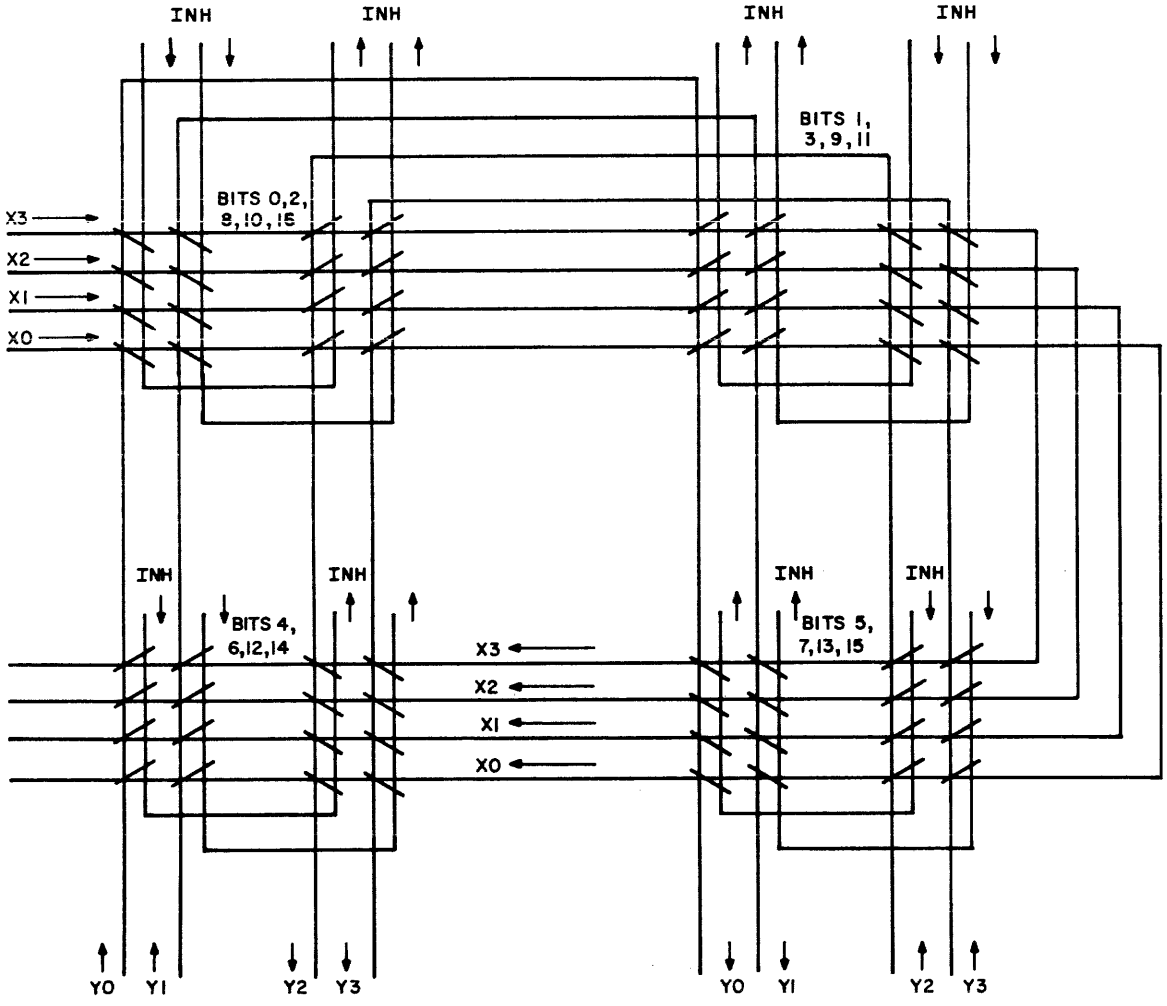


Figure 1. Series 5 Memory Basic Layout of Major Circuit Sections

This memory is wired in a coincident current, 3D, 3 wire configuration. As an aid in describing basic core switching techniques, a portion of the core plane in the Series 5 Memory is illustrated in Figure 2, where the core orientation and wiring configuration of four typical bit planes are shown. Although there are numerous core and wiring configurations existing in various types of memories, the basic core theory still holds for any version.

A core is switched by applying one-half the current, necessary to switch the core, to the appropriate X and Y drive lines. One core in each plane is thereby addressed. During a Read operation, current flow in the drive lines is such as to force the cores to the ZERO state. Nothing occurs in any core which is already in the ZERO state. However, if a core is in the ONE state, the core switches. When the core changes state, a signal is induced in the sense winding for that bit plane. The induced signal is used to generate a ONE indication for that bit position. During a Write operation, current flow is in the opposite direction in the drive lines, and tends to force the cores to the ONE state. An opposing current is applied to the inhibit winding for each bit plane which is to remain at ZERO.

The arrows corresponding to current direction in Figure 2 indicate the current direction necessary through all cores for a Write operation. A half current on XO and YO will switch the cores at the intersection of XO/YO to the ONE state; if an XO/YO core in a particular bit plane is to remain in its present (ZERO) state, an inhibit current in the appropriate bit plane is also applied to cancel one of the X or Y half currents. During Read, the inhibit current is never applied and the current direction for the X and Y wires is reversed.



NOTE: CURRENT DIRECTION SHOWN FOR "WRITE" PORTION OF MEMORY CYCLE.

Figure 2. Basic Three Wire, 3 D Memory

5. SERIES 5 MEMORY CORE PLANE CONFIGURATION

For clarity, the core plane wiring is shown in two parts. Figure 3 depicts the X and Y wires and Figure 4 depicts the Sense-Inhibit wires.

Each bit plane contains 64 rows of cores in the horizontal direction (64Y), with each row containing 64 cores (64X), for a total of 4096 cores (Figure 3). The X and Y wires are common to all bit planes. For a non-parity memory, the cores in Bit 17 are omitted and the X wires terminate as shown. Each bit plane has a pair of Sense-Inhibit windings (Figure 4). These serve a dual purpose: during a Read operation they are used to sense the readout of the cores; during a Write operation, they are used to carry inhibit current. The operation of the core plane is described in greater detail later in this specification.

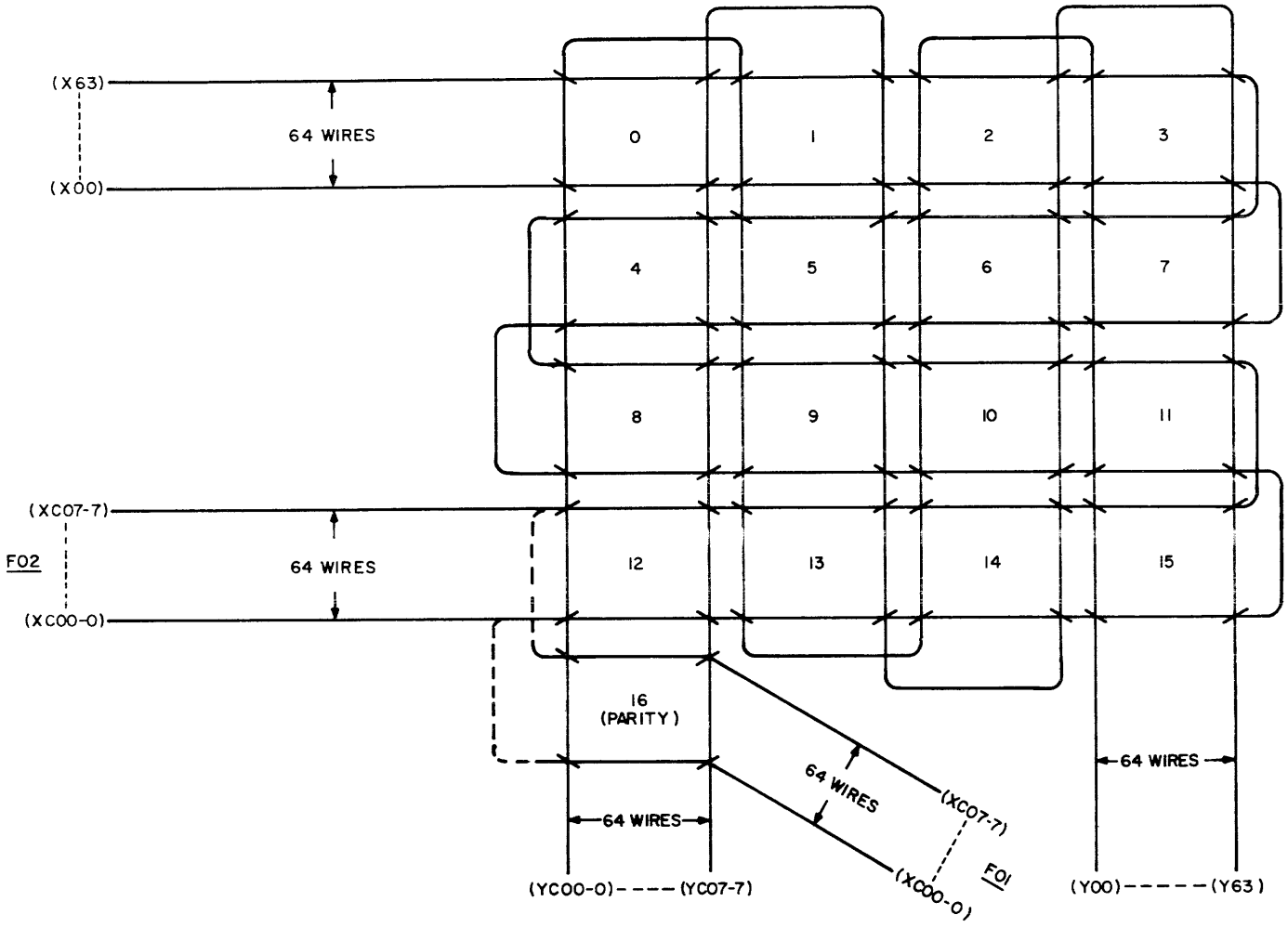
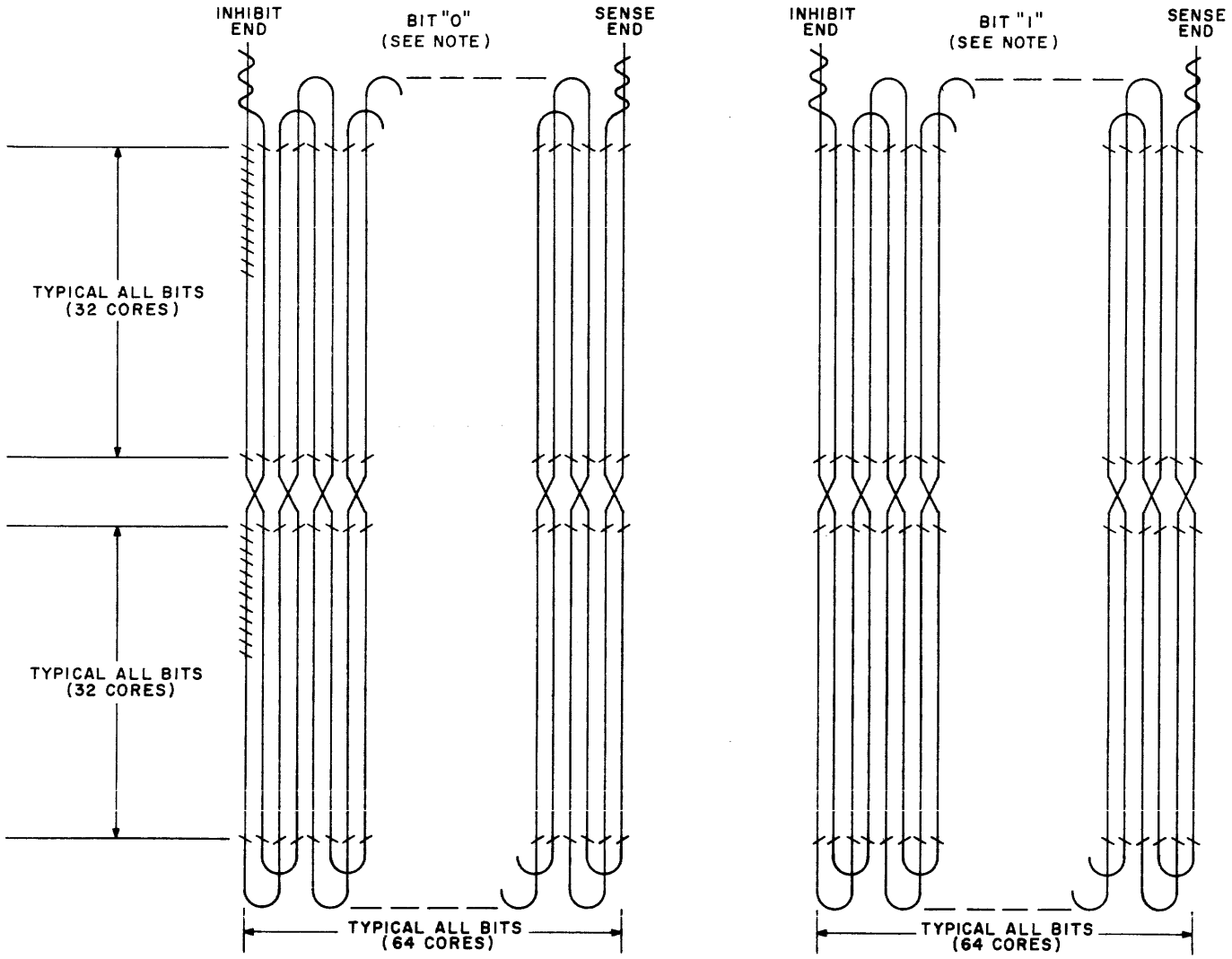


Figure 3. X and Y Core Plane Wiring

Note that the cores are oriented in opposite alignments for specific bit planes. The inhibit current direction alternates in every other bit plane. Inhibit current for bits 0, 2, 4, 6, 8, 10, 12, 14, and 16 flows from + 16.5 volts (at the inhibit end) to ground (at the sense end). Inhibit current for bits 1, 3, 5, 7, 9, 11, 13, and 15 flows from ground (at the sense end) to - 16.5 volts (at the inhibit end). As shown in Figure 4, the inhibit current direction (in any bit plane) in the first two rows of cores (and subsequent alternate pairs of rows) is in the opposite direction from the second two rows of cores (and subsequent alternate second pairs of rows).

Since the Y write current must be such as to always oppose the direction of inhibit current (see Figure 2), the Sense-Inhibit wiring pattern dictates that the Y write current of a pair of Y wires be in a direction opposite to the next adjacent pair of Y wires. This is described in greater detail later in this specification.

The Sense-Inhibit wiring pattern used in the Series 5 Memory minimizes noise, thereby maximizing readout ZERO-ONE separation.



NOTE: CORE ORIENTATION SHOWN FOR BIT "0" IS TYPICAL FOR BITS 0,2,5,7,8,10,13,15, AND 16.
CORE ORIENTATION SHOWN FOR BIT "1" IS TYPICAL FOR BITS 1,3,4,6,9,11,12, AND 14.

Figure 4. Sense-Inhibit Core Plane Wiring

6. BLOCK DIAGRAM ANALYSIS

The Block Diagram for the Series 5 Memory is on Sheet 6 of Functional Schematic 02-211D08. It consists of five basic blocks. The Logic Block receives the four main timing pulses, LRO, WO, ERO, and INHO, and sends a parity indicating signal (PARO) signifying whether or not the memory has a parity bit. The logic contains double inverting gates for fan-out, and a decoder that generates other timing pulses used in the Y access.

The Y and X Access Blocks receive external memory addresses and timing pulses from the input logic. Each block contains decoders, current switches and drivers, and a diode matrix. Sixty-four wires from the Y Diode Matrix and 64 wires from the X Diode Matrix are threaded through the core plane.

The Inhibit and Sense Block receives memory data and sends memory sense pulses. Each pair of the 17 pairs of dual purpose sense-inhibit wires is threaded through its corresponding bit core plane. The Inhibit and Sense Block also contains the inhibit current drivers, sense amplifiers, strobe circuit, and bus sending and receiving gates.

7. TIMING

The timing for the Series 5 Memory is shown in Figure 5. The pulse widths and pulse timing must be maintained within ± 9 nanoseconds.

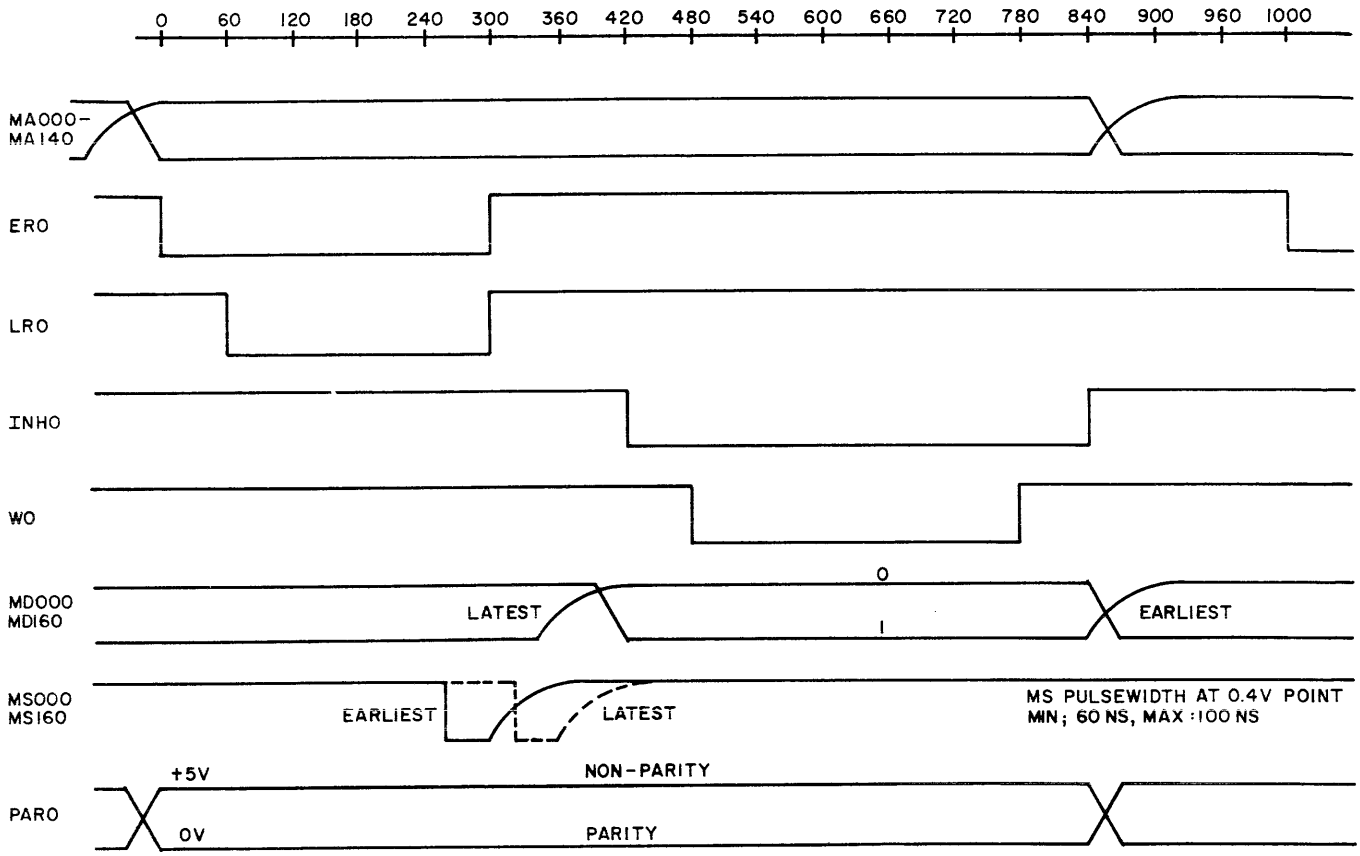


Figure 5. Series 5 Memory Timing

For a Write (Erase and Write) operation, ERO (Early Read) which controls Y drive current, is lowered at T_0 after the address (MA000 - MA140) has settled. LRO (Late Read) which controls X drive current, is lowered 60 nanoseconds after ERO is lowered. Both ERO and LRO are raised at the same time, at 300 nanoseconds. The addressed word is read and switched to ZERO, and gated onto the MS Bus. The Read data is not written back into the same address location. The net effect is an erase of data in the addressed location.

INHO (Inhibit Current Control) is lowered 120 nanoseconds after ERO and LRO are raised, followed 60 nanoseconds later by the lowering of WO (Write), which controls the X and Y drive current. WO is raised 60 nanoseconds before INHO. New data is written into this addressed location depending on MD000 - MD160. Raising the MD line signifies a ZERO; lowering the MD line signifies a ONE.

The Read (Read-Restore) operation timing functions in the same manner as in the Write operation, except that data read out is written back into the same address location.

Output PARO is a DC level. When the Series 5 Memory is addressed, PARO is high if the memory does not have a parity bit and low if it does have a parity bit. This allows Parity Core Memories and Non-Parity Core Memories to be intermixed in the same system.

8. ADDRESSING

Addressing in the Series 5 Memory requires the selection of two core plane wires. Figure 6 tabulates the memory address assignments. MA000, MA010, and MA020 are used in selecting up to one-out-of-eight memory boards. This is accomplished on the back panel pins of memory slots in the Processor card file and expansion card file, where each memory slot is uniquely preconnected so that each memory responds to its one-out-of-eight address code. Memory boards can easily be interchanged without necessitating any wiring changes on the memory board itself. Refer to Schematic 02-211D08, Sheet 6, for the memory back panel map and the address decoding table.

The X access contains an 8 x 8 diode matrix to drive current in the 64 X wires. MA030, MA040, and MA050 are used for the X column selection, while MA060, MA070, and MA080 select the X lines. The 64 Y wires are driven by an 8 x 8 diode matrix in the Y access. MA090, MA100, and MA110 select the Y columns and MA120, MA130, and MA140 are used in the selection of the Y lines.

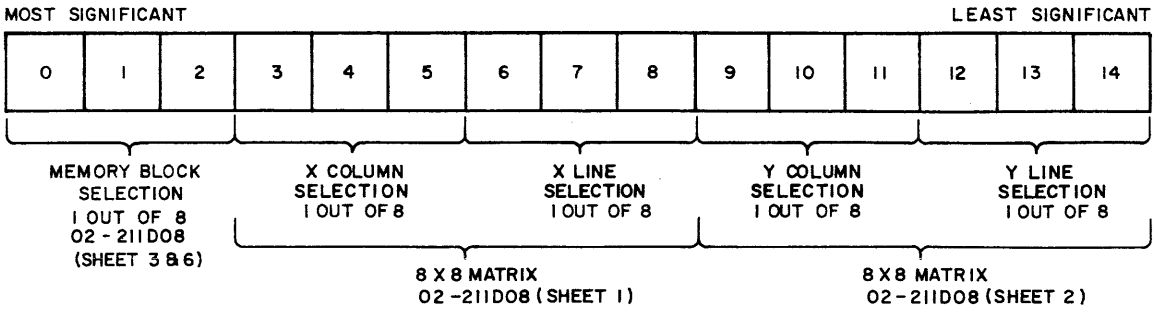


Figure 6. Memory Address Assignments

Figure 7 shows a simplified schematic of the Series 5 Memory with Bits 0 and 15 used for illustrative purposes. The sense-inhibit wiring pattern for Bits 0 and 15 is shortened and simplified. The sense amp ends, exit the bit planes in the Y62 an Y63 rows (see Figure 4 for the precise wiring pattern). The direction of inhibit current is shown for each bit plane. Note that in order for the Y current to be opposition to the inhibit current at each core location, appropriate switches must be closed. The currents in YL00 and YL01 must be opposite to those in YL02 and YL03. This current direction alternates throughout successive pairs of Y lines. See Section 9 and Functional Schematic 02-211D08, Sheet 2, for more detailed information on the Y access.

Examples of core switching are tabulated in Table 2, referencing Figure 7. S1 through S16 represent switching circuits.

TABLE 2. CORE SWITCHING EXAMPLES

OPERATION	SWITCHES CLOSED		
	X	Y	Inhibit
Read Core AO and A1*	S2, S3	S5, S14	---
Read Core CO and C1*	S2, S3	S10, S13	---
Write One in AO and Zero in A1	S1, S4	S6, S13	S16
Write Zero in AO and One in A1	S1, S4	S6, S13	S15
Write One in CO and Zero in C1	S1, S4	S9, S14	S16
Write Zero in CO and One in C1	S1, S4	S9, S14	S15

*Cores BO/B1 operate in same fashion as the AO/A1 cores; DO/D1 operate the same as CO/C1.

9. CIRCUIT DESCRIPTION

9.1 Introduction

This section describes the Series 5 Memory circuits shown on Functional Schematic 02-211D08. The decoders referenced in the logic and Y and X access sections, are one-out-of-ten decoders in which only eight, or fewer, outputs are used for one-out-of-eight decoding. A high on the D input (pin 12) of any decoder enables the last two outputs that are not used, and disables the first eight outputs. Therefore, the D inputs to the decoders are driven by timing pulses which either enable or disable a decoder. The access decoder outputs are activated, in order, by the memory addresses, with input A being the least significant and the timing pulse on input D being the most significant.

The zone location in the schematics of components referenced or which generates signals referenced during the course of the following descriptions are provided in parenthesis after the circuit designation or signal mnemonic.

9.2 Logic

Refer to Schematic 02-211D08, Sheet 3. The Logic consists of an enabling gate, input buffer gates, inverting gates, a timing decoder, and a parity indicating gate. The three back panel decoded addresses, MA00, MA01, and MA02, are the three inputs to the enabling gate, A3(3B3). The Address Connection Table on Sheet 6 of Functional Schematic 02-211D08 tabulates the eight strap configurations to obtain one-out-of-eight address decoding. Whenever the three inputs to the AND gate A3 are high, the output is high. This enables certain gates in A4, A5, and decoder A2. If any input to AND gate A3 is low, all the above-mentioned gates are disabled to prevent any timing pulses from reaching their destinations in the memory circuits.

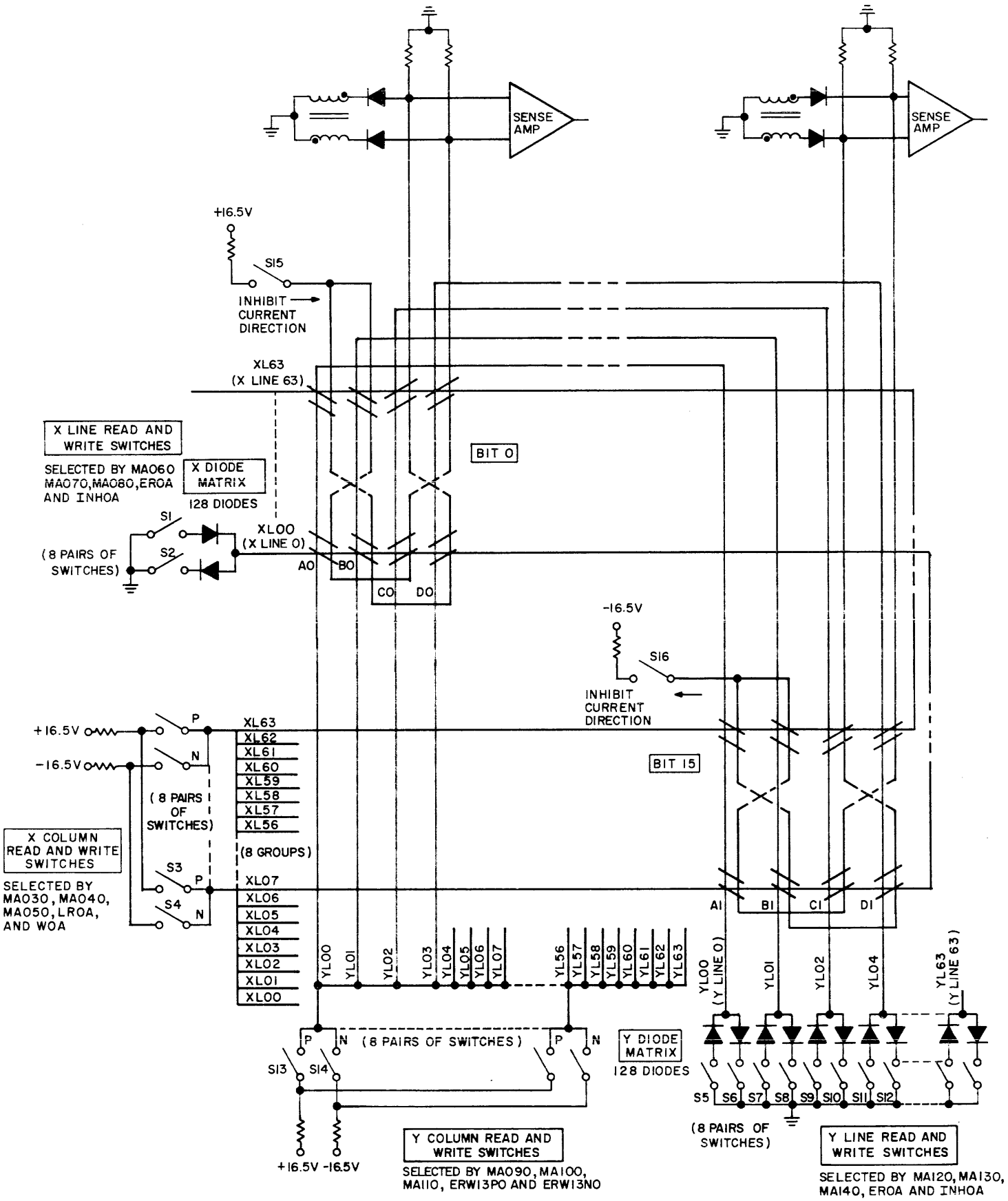


Figure 7. Memory Addressing, Simplified Schematic

The input to gate A1A (3B4) is strapped to the enable line of A3 (B) when the board contains a parity core plane. Whenever the memory board is addressed, PARO goes low. This is used to enable a parity-checking circuit external to the Series 5 Memory. By strapping the input to A1 (A) to ground (C), a high PARO defines a non-parity memory.

Gates A5 (3E2) buffer and invert the four major timing inputs (LRO, WO, ERO, INHO), and the A4 gates (3E3) then invert these pulses to their correct negative-going levels (LROA, WOA, EROA, INHOA) to enable the X and Y access decoders. INH1A (3H2), however, is positive-going to enable the memory data input gates on Sheets 4 and 5. LR1A and W1A are positive-going to turn on the positive and negative current generating switches in the X Access.

Decoder A2 (3E4) decodes EROA, WOA, and MA130. Two pairs of outputs are OR tied to obtain ERW13P0 and ERW13N0. The ERW13P0 and ERW13N0 signals are used to enable Column Decoders in the Y Access, which effectively reverses the direction of Y drive current (during Read and Write) in successive pairs of Y wires, depending on the state of MA130. ERW13P1 and ERW13N1 are positive-going to turn on the positive and negative current generating switches in the Y access.

9.3 Y Access

Refer to Schematic 02-211D08, Sheet 2. Memory addresses MA120 through MA140 (2A2) are three inputs to one-out-of-eight Read/Write line decoders, A12 and A7. MA090 through MA110 (2S2) are three inputs to the one-out-of-eight Read/Write column decoders, A18 and A13. The Y Access is an eight-by-eight matrix. One-out-of-eight decoder, A12 (2B4) turns on one of the eight line Read switches, Q9-Q16, during Read time when it is enabled by EROA. Another one-out-of-eight decoder, A7 (2B7) turns on one of the eight Write switches, Q1-Q8, during Write time when it is enabled by INHOA. The decoder A18 (2H2) and the eight positive column switches Q25-Q32 are enabled by ERW13P0, and decoder A13 and the eight negative column switches Q17-Q24 are enabled by ERW13N0. A column is turned on after one of the Write lines has been turned on by INHOA during Write time. For Read, one line and one column are turned on simultaneously. The positive (2D1) and negative (2L1) currents are turned on when gates A20 are enabled by ERW13P1 and ERW13N1 respectively. SCLROA connects to the second inputs of the current switching gates at 2B1 and 2J1. This input is low during power on power off sequences; the currents are thereby inhibited and memory contents are preserved.

Note that the polarity of alternate line switch transistor pairs (Q9-Q10; Q11-Q12) is reversed in order to drive current into alternate Y line pairs in an opposite direction. The Y Column Decoders correspondingly turn on appropriate positive or negative column switches. The decision of whether to turn on a positive or negative switch is controlled by ERW13P0 and ERW13N0, an OR function of EROA, WOA, and MA130. MA130 (second least significant) is also a control input to the line decoders, where it turns on pairs of Read or Write switches (each of which is in turn selected by MA140, the least significant). When a Line switch with its collector grounded (Q9, Q10, Q13, Q14, Q3, Q4, Q7, Q8) is turned on, a negative column switch is turned on (Q17 through Q24); conversely, when a Line switch with its emitter grounded (Q11, 12, 15, 16, 1, 2, 5, 6) is turned on, a positive column switch is turned on (Q25 through Q32) to allow current to flow in the Y line which is opposite to that of the current generated by the first example. Also note that the Y Access current is turned on before the X Access current during Read time. This is to minimize the effect of noise on the sense wire which occurs when currents are turned on. Two test points (2G1, 2R1) are available to observe voltages. For a basic example of access operation, see Section 8, Addressing.

The Y Access line and column switches are selected according to the truth table in Table 3. An active decoder output turns on the transistor switch connected to it.

9.4 X Access

The X Access circuit is shown on Sheet 1 of Functional Schematic 02-211D08. Memory addresses MA060, MA070, and MA080 (1A2) are used to drive the one-out-of-eight Read/Write line decoders, A27 and A32. MA030, MA040, and MA050 are used for driving the one-out-of-eight Read/Write column decoders A20 and A21. The X Access is an eight-by-eight matrix. The one-out-of-eight decoder, A27, turns on one of the eight line Read switches (Q53-Q60) during Read time when it is enabled by EROA. The one-out-of-eight decoder A32 turns on one of the eight line Write switches (Q61-Q68) during Write time, when it is enabled by INHOA. The eight column Read and Write switches (Q37-Q52), when activated by decoders A26 and A21, function in the same fashion. EROA and INHOA enable the line decoders and switches first; LROA and WOA enable the column decoders and switches after the line switches have been turned on. The positive (1D1) and negative (1L1) currents are turned on when gates A20 are enabled by LR1A and W1A respectively. SCLROA connects to the second inputs of the current switching gates at 1B1 and 1J1. This input is low during power on/power off sequences; the currents are thereby inhibited and the memory contents are preserved. Two test points (161, IR1) are available for observing voltages. For a basic example of access operation, see Section 8, Addressing. The X Access line and column switches are selected according to the truth table in Table 4. An active decoder output turns on the transistor switch connected to it.

TABLE 3. Y SELECTION DATA

Y LINE SELECTION DATA						
EROA	INHOA	MA120	MA130	MA140	Decoder Output	Mnemonic
0		1	1	1	A12-09	YL00P0
0		1	1	0	07	YL01P0
0		1	0	1	06	YL02N0
0		1	0	0	05	YL03N0
0		0	1	1	04	YL04P0
0		0	1	0	03	YL05P0
0		0	0	1	02	YL06N0
0		0	0	0	01	YL07N0
	0	1	1	1	A7-09	YL00N0
	0	1	1	0	07	YL01N0
	0	1	0	1	06	YL02P0
	0	1	0	0	05	YL03P0
	0	0	1	1	04	YL04N0
	0	0	1	0	03	YL05N0
	0	0	0	1	02	YL06P0
	0	0	0	0	01	YL07P0

Y COLUMN SELECTION DATA						
ERW13P0	ERW13N0	MA090	MA100	MA110	Decoder Output	Mnemonic
0		1	1	1	A18-09	YC00
0		1	1	0	07	YC01
0		1	0	1	06	YC02
0		1	0	0	05	YC03
0		0	1	1	04	YC04
0		0	1	0	03	YC05
0		0	0	1	02	YC06
0		0	0	0	01	YC07
	0	1	1	1	A13-09	YC00
	0	1	1	0	07	YC01
	0	1	0	1	06	YC02
	0	1	0	0	05	YC03
	0	0	1	1	04	YC04
	0	0	1	0	03	YC05
	0	0	0	1	02	YC06
	0	0	0	0	01	YC07

9.5 Sense-Inhibit Circuits

The Sense-Inhibit Circuits are shown in 02-211D08, Sheets 4 and 5. Since the circuits in Sheets 4 and 5 are similar, only Sheet 5 will be used in the description. Nine MD gates, A38, A40, and A45 (5A2-5R2), are used to turn on the nine Inhibit switches, Q77-Q85 (5A3-5R3). During Write time, INHIA (5A1) is high enabling the nine MD gates. The state of the MD lines determines if a ONE or a ZERO is to be written at a particular address. A high MD (Write Zero) line turns on the Inhibit switch causing current to flow in the Sense-Inhibit wires. This current cancels the X or Y current with the result that the core remains in the ZERO state (not switched). A low MD (Write One) will not turn on the Inhibit switch. The coincident X and Y current causes the core to switch to the ONE state.

Bit 0, 2, 4, 6, and 8 currents flow from +16.5 volts, through switches, to ground. Bit 1, 3, 5, and 7 currents flow from ground, at the balun network (5A5-5R5), to -16.5 volts through switches. The inhibit current is divided through a pair of Sense-Inhibit wires (5A4-5R4) unique to each bit. The balun network at the sense end equalizes the current in each pair of Sense-Inhibit wires. Note, therefore, that the Inhibit switch carries approximately 600 milliamps with 300 milliamps flowing in each leg of the Sense-Inhibit pair.

During Read time, bipolar readouts are sensed by the sense amplifiers, A44, A48, A49, A55, and A56 (5A6-5R6). The positive-going sense amplifier output is enabled by the positive-going strobe pulse STBB1. The VT (threshold voltage) of the sense amplifiers is adjusted to provide maximum ZERO/ONE margins. The voltage division at the reference input to the sense amplifier is approximately 100 to 1.

TABLE 4. X SELECTION DATA

X LINE SELECTION DATA						
EROA	INHOA	MA060	MA070	MA080	Decoder-Output	Mnemonic
0		1	1	1	A27-09	XL00N0
0		1	1	0	07	XL01N0
0		1	0	1	06	XL02N0
0		1	0	0	05	XL03N0
0		0	1	1	04	XL04N0
0		0	1	0	03	XL05N0
0		0	0	1	02	XL06N0
0		0	0	0	01	XL07N0
	0	1	1	1	A32-09	XL00P0
	0	1	1	0	07	XL01P0
	0	1	0	1	06	XL02P0
	0	1	0	0	05	XL03P0
	0	0	1	1	04	XL04P0
	0	0	1	0	03	XL05P0
	0	0	0	1	02	XL06P0
	0	0	0	0	01	XL07P0

X COLUMN SELECTION DATA						
LROA	WOA	MA030	MA040	MA050	Decoder-Output	Mnemonic
0		1	1	1	A26-09	XC00
0		1	1	0	07	XC01
0		1	0	1	06	XC02
0		1	0	0	05	XC03
0		0	1	1	04	XC04
0		0	1	0	03	XC05
0		0	0	1	02	XC06
0		0	0	0	01	XC07
	0	1	1	1	A21-09	XC00
	0	1	1	0	07	XC01
	0	1	0	1	06	XC02
	0	1	0	0	05	XC03
	0	0	1	1	04	XC04
	0	0	1	0	03	XC05
	0	0	0	1	02	XC06
	0	0	0	0	01	XC07

The flip-flop circuit at location 5A8, which is typical of all the sense amp flip-flops, is used in the following description: The set input (Pin 5 of A60) goes high when a Strobe pulse (STBD1) is generated. The positive-going sense amp output (when a ONE is read out) is inverted by gate A57, whose output connects to the ONE side of the flip-flop (Pin 6 of A60). If a ONE is read out, the flip-flop is reset. The ZERO side of the flip-flop (Pin 3 of A60) is inverted by A58 and the negative-going pulse is placed on the MS Bus. When the Strobe pulse (STBD1) goes low, the flip-flop is set again. If a ZERO is read out, the flip-flop is never reset and the MS Bus stays high.

9.6 Sense Auxiliary Circuits and Decoupling

Refer to Schematic 02-211D08 Sheet 3 during the following descriptions.

9.6.1 Strobe. The Strobe pulse (STB0) is derived from a dual single shot monostable, A42 (3N2). The negative-going edge of LROA triggers the first monostable. The negative-going output from the second monostable is connected to fan-out and inverting gates, A41. STBA1 and STBB1 enable the sense amplifiers; STBC1 and STBD1 are used to set the MS flip-flops. Potentiometer P2 (3N1) and Capacitor C85 (3N2) are timing components used to vary the Strobe pulse delay. C114 and R251 determine the width of the Strobe pulse. A test point, STB, is provided to observe the strobe.

9.6.2 VT. The VT circuit (3M5) provides a regulated threshold voltage for the sense amplifiers. This VT can be varied by P1. Terminals 129-1 and 228-1 allow connection to an external test circuit to override the VT circuit for factory test purposes. A test point is provided to measure VT.

9.6.3 -6.2 Volts. The network at 3N7 derives -6.2 volts from the -16.5 volt source. The -6.2 volts is one of the supply voltages required by the sense amplifiers.

9.6.4 Thermistor. The thermistor connections to the back panel are shown at 3S7. The thermistor is a temperature sensitive device which connects to the ± 16.5 volt power supply. The ± 16.5V will vary as the temperature varies. At 0°C the supply voltages are approximately 18.00 volts; at 50°C the supply voltages are approximately 15.00 volts. (See Section 11.2, Voltage Adjustment, and Figure 8.) This temperature/voltage tracking is necessary since the memory drive current requirements vary with temperature; at 0°C more drive current is required, while at 50°C less drive current is required to realize optimum memory performance.

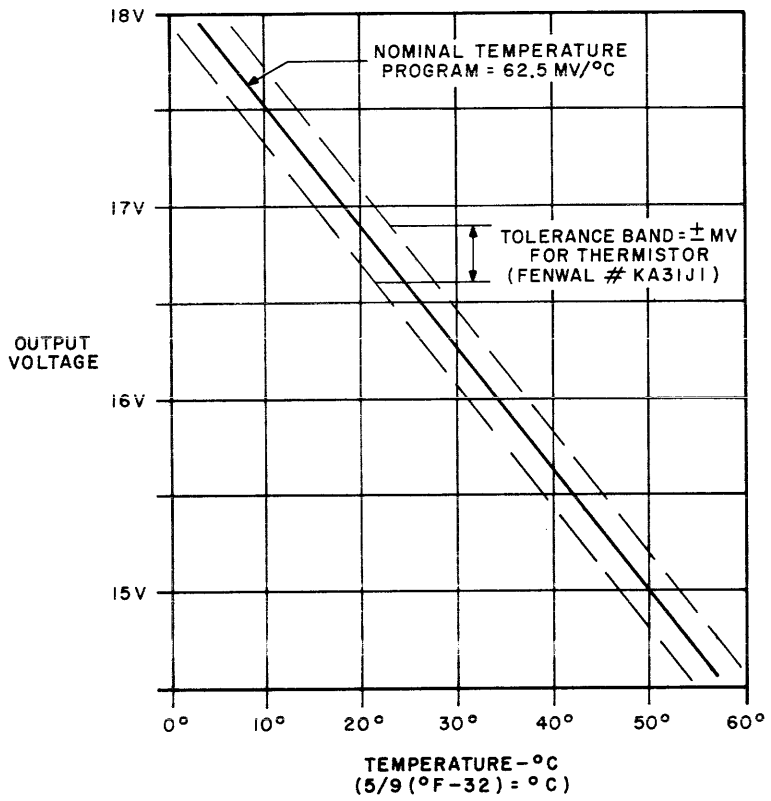


Figure 8. Thermistor Temperature Program

9.6.5 Decoupling. Various capacitors are used throughout the board for voltage decoupling. Their values and their approximate physical location in the vicinity of IC's are referenced at 3B7 through 3K7.

10. TESTPOINTS

Figure 9 illustrates the approximate physical locations of test points. These are tabulated in Table 5 with their corresponding location in Functional Schematic 02-211D08.

TABLE 5. TEST POINT LOCATIONS

Test Point	Function	Schematic Location
VT	Sense Amplifier Threshold Voltage	3S5
STB	Strobe	3M3
LROA	X Column Read Timing and Strobe Generation	1G2
GRD	Ground	
PYC	Positive Y Column Voltage	2G1
NYC	Negative Y Column Voltage	2R1
PXC	Positive X Column Voltage	1G1
NXC	Negative X Column Voltage	1R1

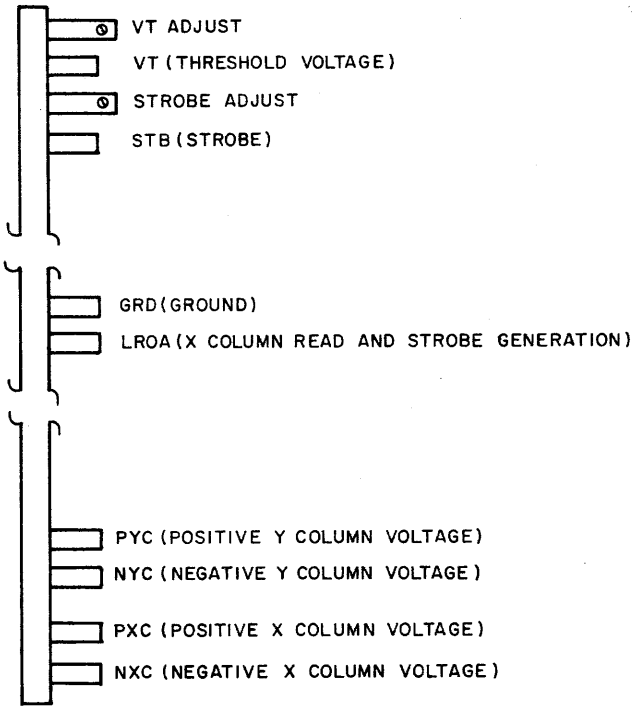


Figure 9. Series 5 Memory Test Points

11. TESTS AND ADJUSTMENTS

11.1 Introduction

This section describes tests and adjustments which should be used periodically as a check of memory system operation, and as an aid in troubleshooting when a memory problem exists. Perform the checks in the order that they are listed in this section.

NOTE

The power supply adjustments listed in the appropriate Power System Manual, and the system clock adjustments listed in the appropriate digital system maintenance manual, should be performed prior to the memory adjustments.

11.2 Voltage Adjustment

The nominal ± 16.5 volt input to the memory system should be checked prior to any other memory checks. The 16.5 volt regulator on the power supply has a control input from a thermistor mounted on the memory board. It is therefore important to consider the ambient temperature when adjusting the 16.5 volt regulator. The following test equipment is required for this adjustment.

1. A laboratory thermometer accurate to ± 1%.
2. A digital voltmeter capable of reading 15 to 18 volts ± 1%.

Use the following procedure to check, and adjust if necessary, the 16.5 volt regulator.

1. Measure the ambient temperature. Refer to Figure 8 and determine the voltage setting for the temperature measured.
2. Compare the voltage of -16.5 and +16.5 at the back panel terminals to assure that the voltages are equal. If the voltages are not equal, adjust the trimpot on the power supply to obtain equal readings.
3. Measure the voltage at the +16.5 back panel terminal.
4. Adjust the trimpot on the power supply to obtain the reading calculated in Step 1.

11.3 Strobe Timing Adjustment

There is a single timing adjustment on the Series 5 Memory.

CAUTION

The adjustment described in this section is carefully set at the factory using sophisticated test equipment not normally available in the field. The adjustment is very stable and should not require field adjustment. The adjustment should be changed only after the check provided indicates that it is out of tolerance and there are no faulty components in the system.

A dual trace oscilloscope with a calibrated time base is required for this check. Use the following procedure to check strobe timing.

1. Load and run the appropriate Memory Test Program.
2. Synchronize the oscilloscope to the negative-going edge of LROA on TP "LROA". (See Figure 9). Observe this pulse.
3. On the second trace, observe the strobe pulse on TP "STB" (see Figure 9). The relationship should be as shown in Figure 10.
4. If the relationship is not as shown in Figure 10 and all components are found to be operating correctly, adjust the Strobe trimpot shown on Figure 9.

The above is a rough adjustment that places the strobe in the general correct area. The VT trimpot is increased to 2.0 volts (see Section 11.5, Marginal Test, for proper procedure). If there are memory errors, the Strobe trimpot is fine adjusted until there are no errors. Then verify that there are no errors with VT at 1.0 volt. When memory is operating properly, adjust the VT trimpot back to its nominal 1.5V ± 0.1V.

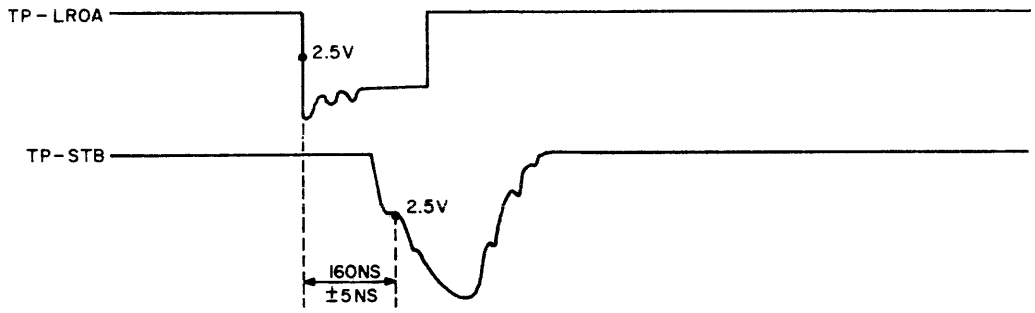


Figure 10. LR0A - STB Relationship

11.4 Memory Test

Run the appropriate Memory Test Program.

11.5 Marginal Test

The following Marginal Test may be performed periodically to locate memory areas which may cause future problems. Test equipment required for this test is:

1. A voltmeter capable of measuring 5 volts ± 2%.

Use the following procedure:

1. Connect the voltmeter to test-points VT and GRD.
2. Run the Memory Test referenced in Section 11.3.
3. Vary the VT trimpot to 1.0 volt and then to 2.0 volts. The test program should continue to run normally within these VT voltages. Return VT to its nominal 1.5 volts ± 1.0V setting after tests are completed.

11.6 Trouble Shooting Aid

Sheets 7 and 8 of Drawing 02-211D08 are provided as an aid in trouble-shooting circuits and locating components. They are used in conjunction with Functional Schematic 02-211D08, Sheets 1 through 6.

12. MEMORY MNEMONICS

The following list provides a brief description of each mnemonic in the Series 5 Memory. The 02-211D08 source of each signal is also provided.

MNEMONIC	MEANING	LOCATION
ENABLE1	Enables logic and access circuits	3C3
ERO	Early Read; X and Y lines read timing pulse	3E1
ERW13N0 ERW13P0 ERW13N1 ERW13P1	Early Read or Write; Y column read and write current direction control timing pulses	3H5
INHO	Inhibit; X and Y lines write, and inhibit drivers timing pulse	3E1
LRO	Late Read; X column read timing pulse and strobe generation	3E1
MA00-MA02	Decoded Memory block selection address	3B1
MA030-MA140	Memory Address Bus	2A2, 2S2, 3A2, 3S2
MD000-MD160	Memory Data Bus	4A1-4N1, 5A1-5R1
MS000-MS160	Memory Sense Bus	4B9-4S9, 5B9-5S9
NXC	Negative X column voltage	1R1
NYC	Negative Y column voltage	2R1
PARO	Parity indicating signal	3A5
PXC	Positive X column voltage	1G1
PYC	Positive Y column voltage	2G1
SCLROA	System Clear	1A1
STB0	Strobe Pulse	3N3
STBA1 and STBB1	Enables sense amplifiers	3S3
STBC1 and STBD1	Sets MS flip-flops	3S5
TEMPA	Connection to thermistor	3S7
TEMPB	Connection to thermistor	3S7
VT	Sense amplifiers threshold voltage	3S6
WO	Write; X and Y column write timing pulse	3E1
XC00-XC07	X column wires (common)	1J6-1S6

MNEMONIC	MEANING	LOCATION
XC00-0 through XC07-7	X wire; Column 0, Wire 0 through Column 7, Wire 7	1J5-1S5
XL00N0-XL07N0	X Line Cathodes	1F6-1F9
XL00P0-XL07P0	X Line Anodes	1F6-1F9
YC00-YC07	Y column wires (common)	2J6-2S6
YC00-0 through YC07-7	Y Wire; Column 0, Wire 0 through Column 7, Wire 7	2J5-2S5
YL00N0-YL07N0	Y Line Cathodes	2F6-2F9
YL00P0-YL07P0	Y Line Anodes	2F6-2F9

MODEL 70 SELECTOR CHANNEL INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-232 Selector Channel (SELCH) in a Model 70 Processor System. The Model 70 Selector Channel is complete on one 35-391 printed circuit board.

2. PHYSICAL CHARACTERISTICS

2.1 Dimensions 15 3/8 x 14 7/8"

2.2 Weight $2\frac{1}{2}$ pounds maximum

3. INSTALLATION

The Model 70 SELCH may be installed in any even numbered universal expansion slot (i.e. 0,2,4, or 6) in the Central Processor Unit (CPU) or in the first Memory or I/O expansion chassis. See Figure 1.

NOTE

If a Memory-I/O chassis is used in the system, any Selector Channel must be installed in that chassis.

3.1 Back Panel Wiring

3.1.1 Multiplexor Channel Bus. At the time of installation it is necessary to cut the Multiplexor Bus wiring between the even numbered slot accepting the SELCH and the next higher numbered slot on the One (1) connector only. The RACK0/TACK0 daisy chain wiring on the back panel is rerouted according to Figure 1. The lower numbered card slots in the chassis become part of the private SELCH Bus on the One (1) connector only.

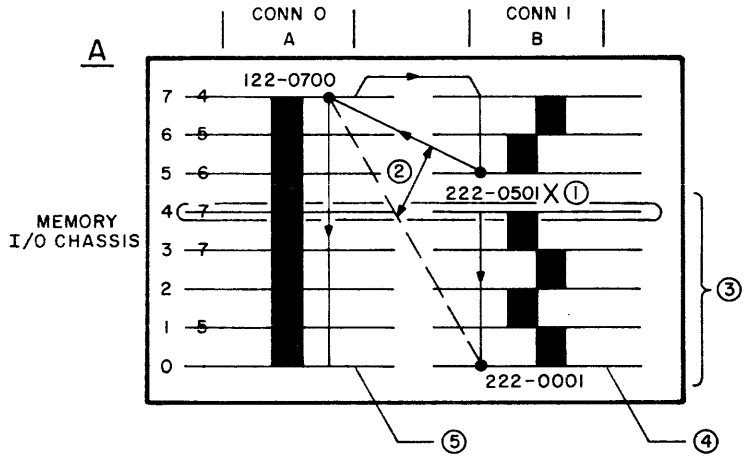
For the convenience of cutting the Multiplexor Bus, the connections between every other slot are made using "top" wire wraps. This allows the cutting of the bus by simply lifting the top wraps when the SELCH is installed in an even numbered slot. Refer to Figure 1 (A) during the following example.

To install a SELCH in Slot 4:

1. Remove all wires on Connector One (1), between Slots 4 and 5, on Pins 11 through 26, Rows 1 and 2. (See backpanel map in 02-232D08 Sheet 7).
2. Remove the wire between 222-0001 and 122-0700.
3. Remove the RACK0/TACK0 jumper between Pins 122 and 222 on both the Zero (0) and One (1) connectors of Slot 4.
4. Connect 122-0700 to 222-0501.
5. Install the SELCH into Slot 4 of the chassis. The private SELCH Bus now appears on the Connector One (1) side of Slots 4,3,2,1, and 0. All slots on the Connector Zero (0) side and Slots 7,6, and 5 on Connector One (1) side remain as standard Multiplexor Bus slots.

To install a SELCH in any other even numbered slot of a CPU chassis or a Memory-I/O chassis, a similar procedure is followed. Refer to Figure 1 B and C.

3.1.2 ACT0/TAC0. The ACT0/TAC0 jumper between Pins 137-0 and 237-0 must be removed from the slot used by the SELCH controller. If the Selector Channel is not the first Direct Memory Access (DMA) channel on the Memory Bus, jumper "K" on the SELCH controller must be removed.



NOTE: THE CIRCLED NUMBERS ON ILLUSTRATIONS A, B, AND C REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING INSTALLATION PROCEDURES.

TO INSTALL A SELECTOR CHANNEL IN SLOT 4 OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

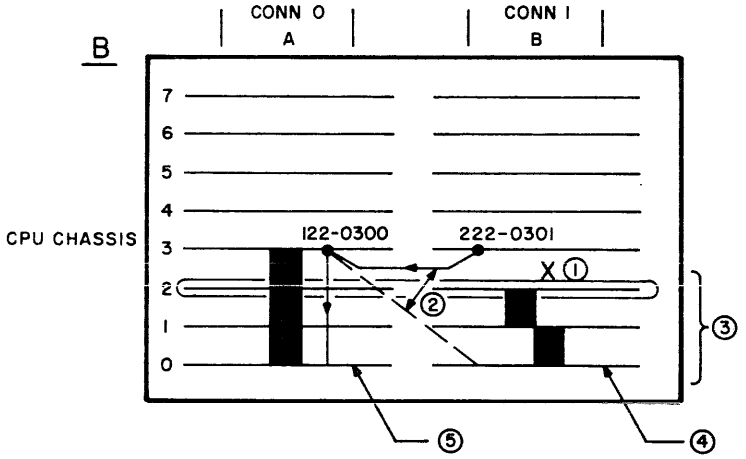
② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE, AND SLOTS 7, 6 AND 5 ON CONNECTOR ONE SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ MEMORY MODULE 7, IF IT EXISTS, MUST BE LOCATED IN SLOT 3.



TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE CPU CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

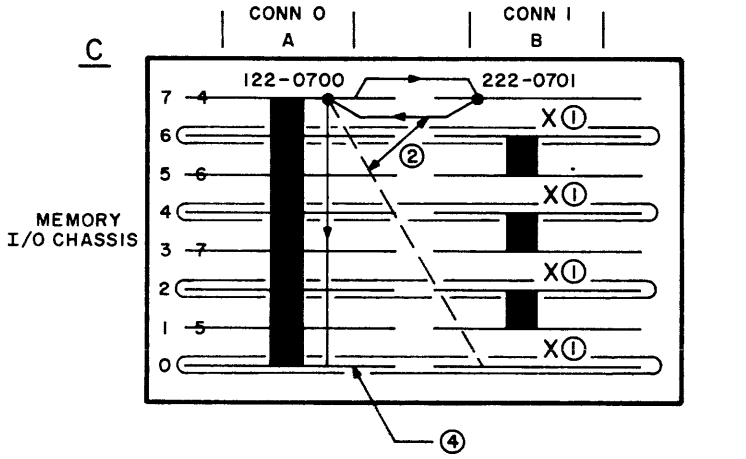
② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

NOTE:
IF A MEMORY I/O CHASSIS IS USED IN THE SYSTEM, ANY SELECTOR CHANNELS MUST BE INSTALLED IN THAT CHASSIS.



TO INSTALL 4 SELECTOR CHANNELS (IN SLOTS 6, 4, 2 AND 0) OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS IN FOUR PLACES.

② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ EACH SELCH, EXCEPT THE ONE IN SLOT 0, HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 0, 1, 3 AND 5 ON CONNECTOR ONE (CONN. 1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

⑤ MEMORY MODULES 5 AND 7, IF THEY EXIST, MUST BE LOCATED IN SLOTS 1 AND 3.

Figure 1. Backpanel Modifications

3.3 Cabling

The cabling necessary for the SELCH depends on the system's physical configuration. When the SELCH Bus does not extend outside the chassis, no cabling is required. When the SELCH Bus must be extended to another chassis, a number of cable configurations can be used. See Figure 2.

See Figure 2 for a summary of all cables. Refer also to Chapter 8, Model 70 User's Manual, Publication Number 29-261, for further details on system configurations.

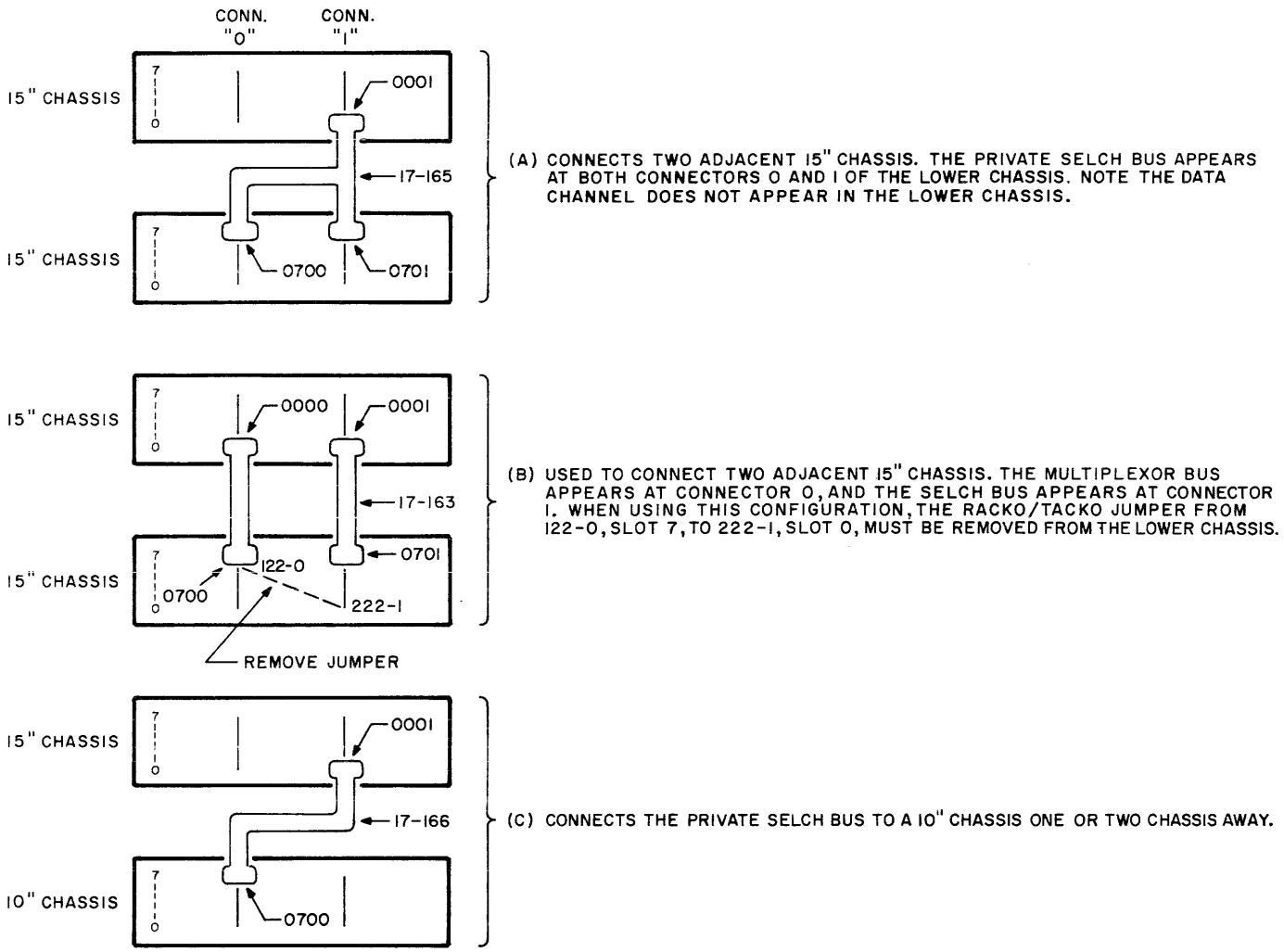


Figure 2. Cabling

4. ADDRESS STRAPPING

The preferred address of the Model 70 Selector Channel is X'F0'. The controller is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-232D08. The number and letter designations shown on the schematic refer to the designations on the apparatus side of the SELCH controller board.

5. INSTALLATION CHECKS

The Model 70 SELCH is factory tested using a special high speed device. Therefore, field checks are contingent upon the user having appropriate hardware and software available with which to exercise the Selector Channel.

MODEL 70 SELECTOR CHANNEL MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-232 Model 70 Selector Channel (SELCH) is a Direct Memory Access port (DMA) which provides block data transfer between a device controller and memory. Once initiated, the transfer is independent of the Processor. The Processor sets up the device controller, loads the SELCH with the starting and final addresses of the memory block, specifies the type of operation (Read or Write), and issues a GO Command. The SELCH then handles the transfer without further direction by the Processor.

The Model 70 Selector Channel is complete on one printed circuit board and occupies one slot in a system chassis. The SELCH provides the drivers, receivers and termination resistors for the private SELCH Bus. This bus originates at Connector One (1) of the SELCH slot and extends to each lower numbered slot in the system chassis on the Connector One (1) side only. The private SELCH Bus can be extended to other chassis, as required. For installation information, refer to Installation Specification 02-232A20.

2. SCOPE

This specification describes the operation of the SELCH in its various modes; Setup, Memory Read, Memory Write, and Termination. Where necessary, this specification references the Multiplexor Channel Bus and Memory Bus operations. These buses are described in detail in the Model 70 User's Manual, Publication Number 29-261.

3. BLOCK DIAGRAM ANALYSIS

Refer to the SELCH block diagram on Sheet 7 of Functional Schematic 02-232D08, and the SELCH Flow Chart, Figure 1, during the following analysis. Before initiating a data transfer via the SELCH, the device controller and the SELCH must be set up. The setup procedure is implemented by the Processor via the Multiplexor Bus (MPX-Bus). When the SELCH is in the Idle Mode, the MPX-Bus is tied directly to the private SELCH Bus through the SELCH. This allows the Processor to communicate directly with any device on the private SELCH Bus.

To prepare the SELCH for data transfer, the Address Register (AR) and Auxiliary Address Register (AAR) must be loaded with the starting address in memory where the transfer is to begin, and the Final Address Register (FAR) must be loaded with the address of the last memory location to be accessed. These registers are loaded from the eight least significant Data Lines D080:150 by four consecutive Data Availables (DAs) from the Processor. The first two Data Availables simultaneously load the AR and AAR, which are 16-bit incrementing registers. The AR is incremented, by two, after each halfword is transferred to/from memory, and the AAR is incremented, by one, with each byte transferred to/from the device. Data transfer is terminated when the AAR is equal to the FAR or when the AAR increments past its maximum value, X'FFFF'.

Data transfer is begun by the Processor issuing a GO Command to the SELCH. Transfer to/from the device is now independent of the Processor. The GO Command also prevents communication between the Processor and any device on the private SELCH Bus until the transfer is terminated and the SELCH is addressed.

Data transfer is controlled in the Move Data circuit by inspection of the four least significant bits of the Status Byte presented by the active device on the private SELCH Bus. When any one of the three least significant bits are set, (EX, EOM, or DU), the transfer is terminated. Bit-12 (Busy) regulates the rate of data transfer. In the Memory Read Mode, the actual data transfer begins with a memory request, REQ0 active, as soon as a GO Command is issued. When the memory request is serviced by the Processor, the SELCH Memory Bus Control circuit activates Select (SEL), which gates the contents of the Address Register (AR) onto the Memory Address Bus, and gates a halfword of data from memory into the Data Register (DR). At the termination of the memory transfer, the data is loaded from the DR to the Data Buffer (DB) and the AR is incremented.

NOTE

Unless the SELCH has dropped REQ0 in time to remain selected during the next memory cycle, the SELCH will be deselected by the rising edge of Inhibit (INH0) after the halfword has been transferred.

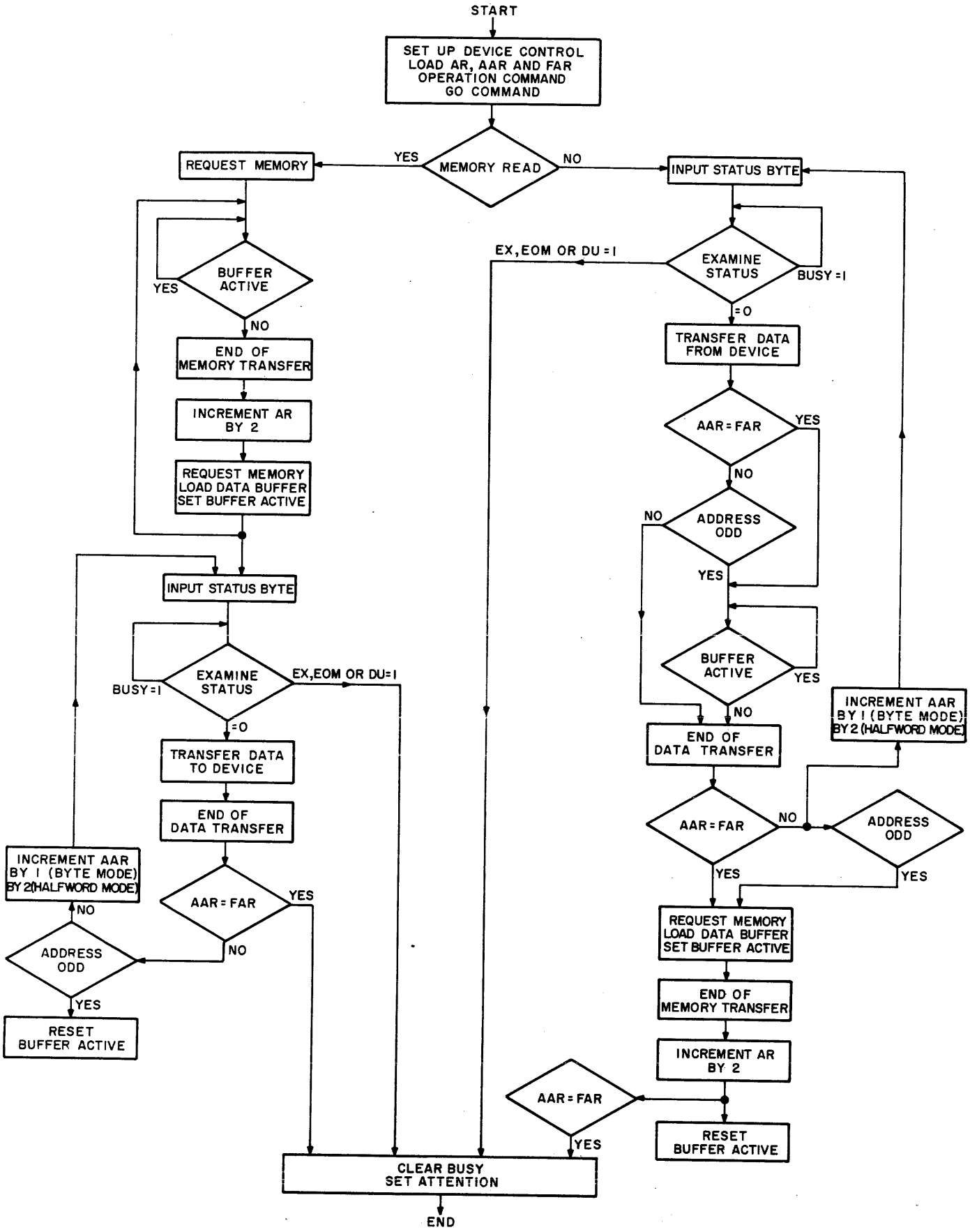


Figure 1. Flow Chart

Once the DB is loaded, data transfer to the device over Private Data Lines PD000:150 is initiated and, when applicable, a request is made to fetch the next halfword from memory. This cycle continues until either a match is detected between the contents of the Auxiliary Address Register and contents of the Final Address Register, or until the transfer is aborted due to an error condition.

In the Memory Write Mode, the data transfer sequence described previously for Memory Read Mode is reversed. That is, two bytes of data are loaded into the DR from the device prior to a memory request and the data flow is from the device to the DR, DR to the DB, and finally into memory.

The Branch Gate circuit and the Move Data circuit control the flow of data between memory and the device. The Branch Gate supervises the overall data flow, while the Move Data circuit performs the handshaking between the SELCH and the active device on the private SELCH Bus.

Upon termination of the data transfer, the program is notified via an interrupt and by the inactive state of the SELCH Busy flip-flop which is presented to the program as Bit-12 of the SELCH Status Byte.

Selector Channel Status and Command Byte Data is shown on Table 1.

TABLE 1. SELECTOR CHANNEL STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE					BSY			
COMMAND BYTE			READ	GO	STOP			

BSY — When this bit is set, an RC circuit generates the EBS1 pulse to start the appropriate SELCH operation. When this bit is cleared an interrupt is generated.

READ — This command, Bit-2, sets the Memory Write (WT) flip-flop. The controller on the SELCH Bus is setup for a device Read operation.

GO — This command, Bit-3, clears the MSC flip-flop and sets the BSY flip-flop to initiate the Data Transfer Mode.

STOP — This command, Bit-4, from the Processor clears the BSY flip-flop and initializes the Load/Unload Sequencer. During the Data Transfer Mode, execution of the command is delayed until the end of a memory cycle, if one is in progress.

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

This section relates to Functional Schematic 02-232D08, Sheets 1 through 6. Note that in INTERDATA functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D080 is Data Line Number 8 (D08). The last character (0) indicates that when D080 is active, the line is at a logical Zero level.

4.2 SELCH Control Circuit

In the Idle Mode, the SELCH Address (2M8), Busy (3F3), and Multiplexor-SELCH (MSC) (3FA) flip-flops are reset and the private SELCH Bus is tied directly to the Multiplexor Bus. This allows the Processor to communicate, via the Multiplexor Bus, with any device on the private SELCH Bus.

To communicate with the SELCH, it must first be addressed. The SELCH Address (X'F0' preferred) is placed on Data Lines D080:150 (1A3-8) and the Address control line is activated (ADRS0)(4B8). The SELCH Address is decoded by the four input NAND gate (1F4) and the Address flip-flop is set (2M8). The set output from the Address flip-flop (AD1)(2J7), when active, prevents the control signals on the MPX-Bus from passing onto the private SELCH Bus by holding the Control Line Gate inactive (CLG1)(1B2). The Capacitors C33 and C34 (4D8) delay the propagation of the Private Address control line (PADRS0)(4F9) to the SELCH Bus so that when the SELCH is being addressed, PADRS0 will not become active. This delay allows the SELCH to be addressed without resetting the Address flip-flop of the active device on the private SELCH Bus.

The simultaneous loading of the Address Register (AR) and Auxiliary Address Register (AAR), and the loading of the Final Address Register (FAR) is accomplished by four consecutive Data Availables (DAs) from the Processor. The Load/Unload Sequencer (2L2) controls the loading of these registers (AR, AAR, and FAR) and the unloading of the AAR. The sequencer is set to its initial state by the termination of the last data transfer, a Stop Command, or a System Clear (SCLR0)(4MS) so that the first DA, through Data Available Gate (DAG0)(2L4), will activate Load Address Register High (LARH0)(2S2).

LARH0 gates Data Lines DA081:151 (1D3-8) into the eight most significant bits of the AR and AAR. The rising edge of the first and each successive Data Available Gate (DAG0)(2L4) increments the sequencer and allows the next DA to activate the next load line. The second DA loads the eight least significant bits of these registers. The third and fourth DAs will then load the Final Address Register in the same order. The contents of the AAR may be inspected, via the program, by issuing two Data Requests (DR) to the SELCH whenever the Load/Unload Sequencer is in its initial state. (e.g. Upon termination of a SELCH transfer, sequencer initialized, the FAR may be inspected to determine if the entire block of data had been transferred.)

If a Memory Write operation is desired, an Output Command with Bit-10 set must be issued to set the Write flip-flop (3F5). Since the Write flip-flop is reset by the Data Available/Request Gate (DARG1)(2L5) whenever a DA or DR is sent to the SELCH (setup procedure), no command is necessary to initiate a Memory Read operation.

Data transfer commences with a GO Command from the Processor, which is an Output Command with Bit-11 set. The GO Command sets both the Busy (3F3) and MSC (3F4) flip-flops. The setting of the Busy flip-flop causes an End of Busy Set pulse (EBS1)(3H4) to be generated. This pulse is generated by differentiating the falling edge of BSY0 (3F3), and is used by the Branch Gate circuit to initiate the transfer cycle. The Busy latch circuit remains set until the Selector Channel detects the termination of transfer and its state is presented to the program via Bit-12 of the Sense Status Byte.

The MSC flip-flop is reset by SCLR0A or by addressing the SELCH, Set Gate active (SGAD1)(2L9), when the Busy flip-flop is reset. The resetting of the MSC flip-flop, MSC0 active, clears any pending interrupt in the Selector Channel.

Information is steered from the SELCH to both the Data Lines (D080:150)(1B4-9) and the Private Data Lines (PD080:150) (1S4-9) by the proper gating of four each, four-to-one line multiplexors (Sheet 1). For example; with the SELCH idle, Busy reset, all Data Lines are tied directly to the Private Data Lines in both directions.

4.3 Memory Bus Control Circuit

Memory Bus Control timing relationships are shown in Figure 2. A SELCH request for memory is started by activating Set Request (SREQ0)(3S4). SREQ0 is activated by the Branch Gate circuit (3M8) when either the SELCH has received a halfword of data from the device or, in the Memory Read Mode, whenever the Memory Data Register is available to accept the next halfword.

SREQ0 is applied to the direct set input of the Request flip-flop (REQ)(4L5) which sets the flip-flop and sends REQ0 to the Processor. When REQ0 is received, the Processor generates Enable (EN0). EN0, on the first DMA device, is jumpered to Accept (ACT0) which generates the daisy chain priority loop through all DMAs in the system. The daisy chain begins at the highest priority DMA as EN0, and propagates to the lower priority DMAs as Transmit Accept (TAC0) until it is captured by the first DMA requesting a memory cycle. When the REQ flip-flop is set and ACT0 (EN0) is active, the ACT0/TAC0 contention circuit (4H2) will block the propagation of TAC0, and provide highs on the J input to the SEL flip-flop and the K input to the REQ flip-flop. Thus, on the rising edge of EN0, the Select flip-flop will become set and the Request flip-flop will be reset. When the SELCH REQ flip-flop is reset and ACT0 (EN0) is active, the ACT0 signal is propagated as TAC0 to the DMA with a lower priority.

The trailing edge of Inhibit (INH0)(4H5), from the Processor, indicates the end of the memory cycle. This edge, unless the SELCH has dropped REQ0 in time to remain selected during the next cycle, will cause the SEL flip-flop to reset. Two pulses, End of Memory Transfer (EMX0)(4M7) and Inhibit (INH0P)(4M2), are generated by the leading and trailing edges of INH0 respectively. EMX0 is used by the Branch Gate circuit to indicate the end of the memory transfer, and is also used together with INH0P to generate Toggle AR (TAR0) which increments the Address Register.

In the Memory Read Mode, the Memory Data Register (MDR) is cleared by Clear Data Register (CDR0)(4R2) which is generated by the trailing edge of REQ1. Write Not (WT0A)(3F5) is ANDed with SEL1 to form Enable Memory Data Read (ENMDR1)(4R6), which gates the contents of the MDR onto the Memory Data Lines for the restore portion of the memory cycle. (This function is disabled when using solid state memory.) The contents of the memory location accessed is gated to the direct set inputs of the MDR by Enable Memory Strobe (ENMS1)(4R4). This function is $\overline{WT} \cdot SEL \cdot \overline{INH}$ for use with core memory and $WT \cdot SEL \cdot INH$ when using solid state memory (4R4).

When writing to memory, the contents of the Data Buffer is gated onto Memory Data Lines MD000:150 (Sheet 6) by Enable Memory Data Write (ENMDW1)(4R3), when selected. A Memory Write operation is indicated to the Processor by activating WRT0A (4S3).

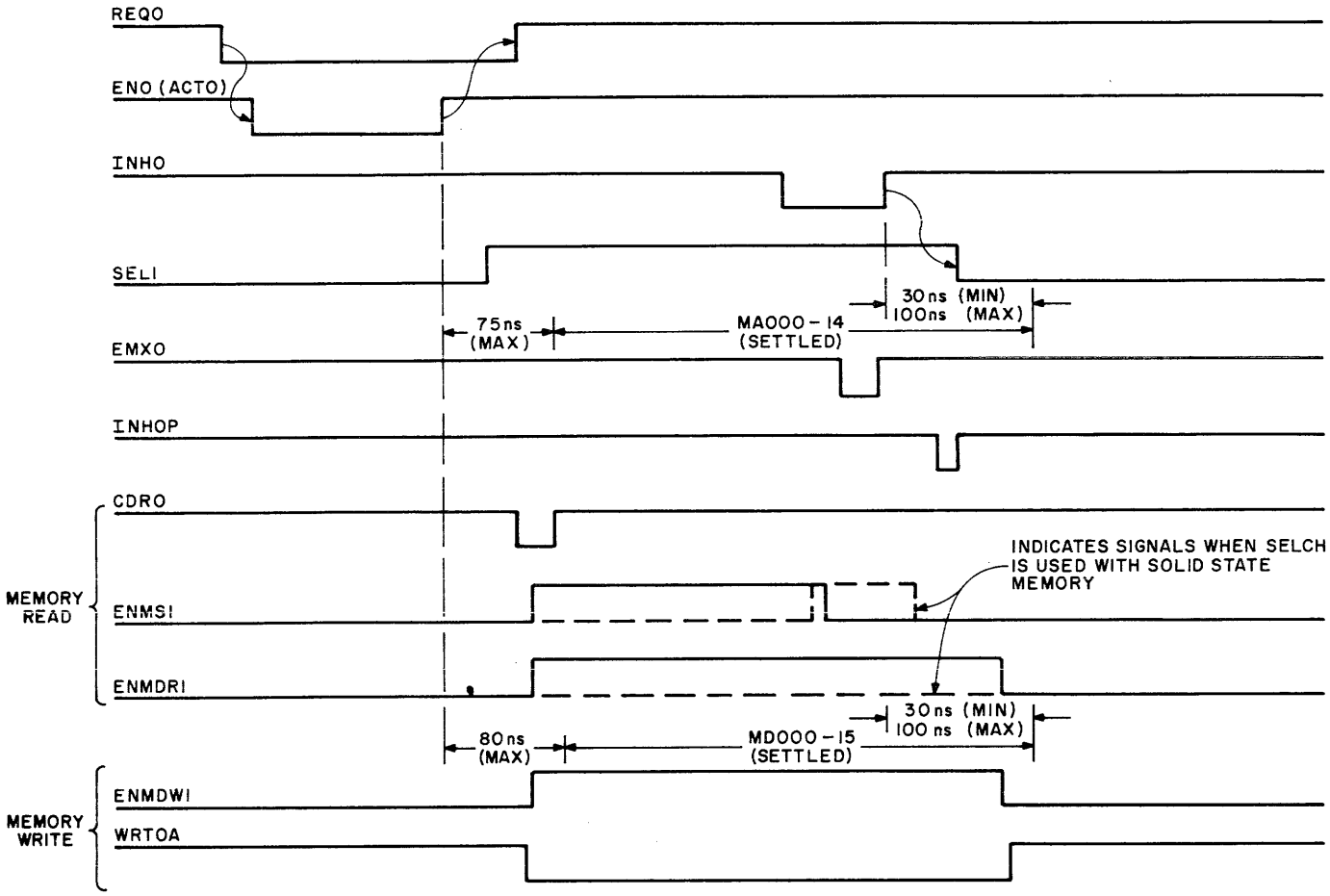


Figure 2. Memory Bus Control Timing Diagram

4.4 Address Register and Auxiliary Address Register.

The Address Register (AR) and Auxiliary Address Register (AAR) (Sheet 5) each consist of four, four-bit counters. These registers are loaded simultaneously by the Processor from Data Lines D080:150 (1A3-8), under control of the Load/Unload Sequencer (as discussed in Section 4.2), with the starting address from which the block transfer is to begin. The contents of the AR (Sheet 5) is gated onto Memory Address Lines MA000:140 (5R1-8) whenever the SELCH is selected, SEL flip-flop set. The AR is incremented, by two, with each memory transfer by Toggle Address Register (TAR0)(4R7). The AAR (Sheet 5) keeps track of the transfer between the SELCH and the device. This register is incremented, by one, for each byte of data transferred by Toggle Auxiliary Address Register (TAAR0)(3M1). When the transfer is in the Halfword Mode, TAAR0 is generated twice for each transfer. The outputs of the AAR are used by the Match circuit to determine the end of the data block. Its contents may be examined, via the program, by issuing two consecutive DRs to the SELCH when the sequencer is initialized. In addition, AAR151 is used in the Byte Transfer Mode to determine whether the byte being transferred is odd or even, for byte steering. Carry Out from the most significant stage of the AAR (CO0)(541) will terminate the transfer, clear Busy, when a transfer is attempted past the maximum memory address. This feature prevents 'wrap-around' in memory.

4.5 Final Address Register

The Final Address Register (FAR) is implemented by four quad latches (Sheet 5). This register, like AR and AAR, is loaded by the Processor under control of the Load/Unload Sequencer. The outputs of this register are used exclusively by the Match circuit to determine when the final address of the transfer is reached.

4.6 Memory Data Register and Data Buffer

The Memory Data Register (MDR)(Sheet 6) is a16-bit register composed of 16 edge triggered JK flip-flops. In the Memory Read Mode, the MDR is first cleared by Clear Data Register (CDR0)(4R2) and then direct set by each active bit on Memory Strobed Data Lines MS000:150 (Sheet 6). During a Memory Write, the data, in double rail format, present at the J and K inputs to the MDR, is toggled into the flip-flops on the trailing edge of either Load Data Register High (LDRH0)(649) or Load Data Register Low (LDRL0)(6J9).

As soon as the MDR is loaded, if the Data Buffer (DB) is empty (as determined by the inactive state of the Buffer Active flip-flop)(3H1), the MDR contents are loaded into the DB (Sheet 6) by Load Data Buffer (LDB1)(357). Information present in the DB is, in turn, either written into memory via Memory Data Lines MD000:150 or sent to the device on Private Data Lines PD000:150.

4.7 Data Transfer Circuit

Refer to Figure 3 for Memory Read timing diagrams and Figure 4 for Memory Write timing diagrams. The Memory Read timing diagram shows the timing of a three byte transfer, in the Byte Mode, of 2,000,000 Bytes/second. Figure 4 shows a transfer of two halfwords, in the Halfword Mode, to a slower device.

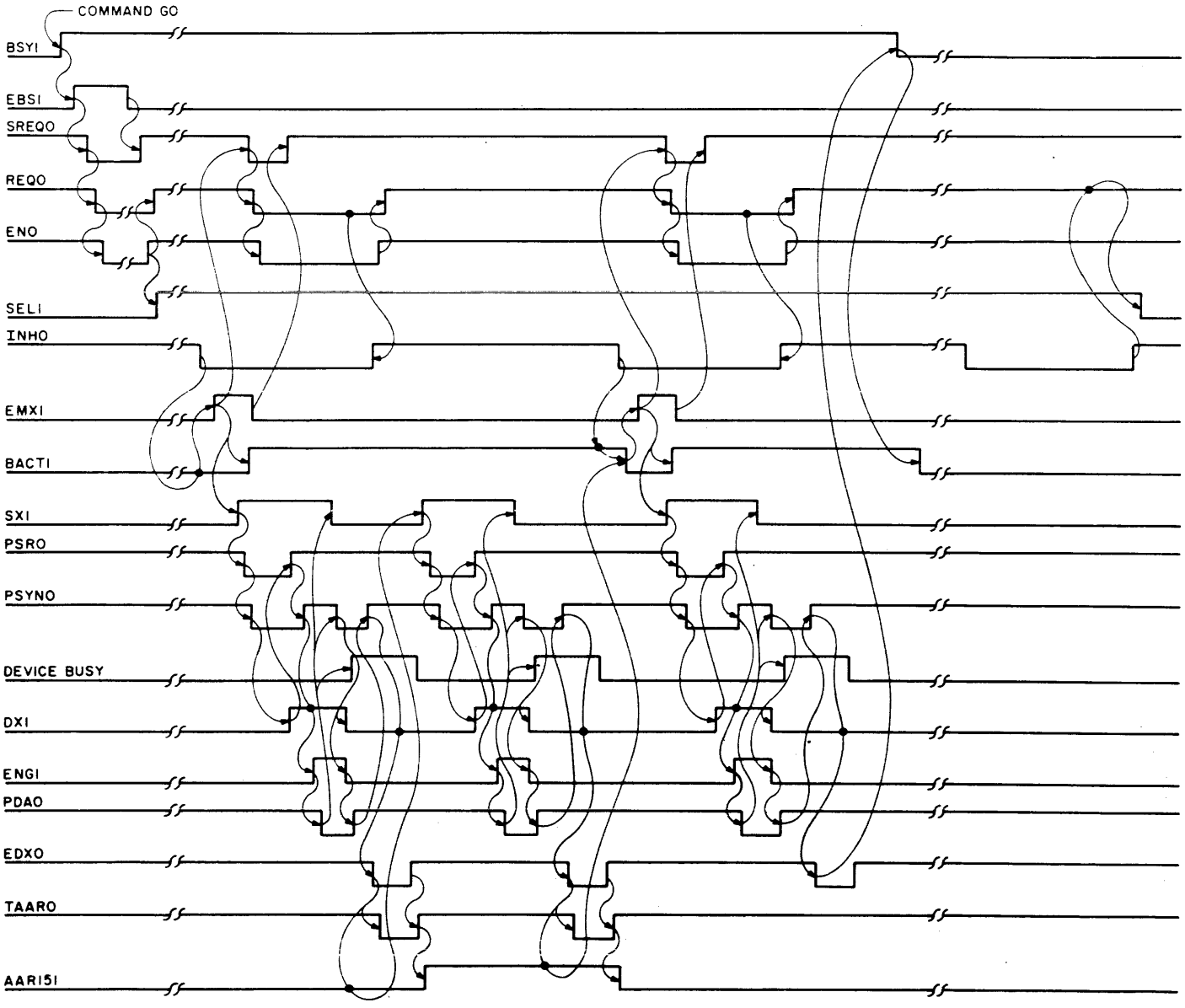


Figure 3. Memory Read (Byte Mode)

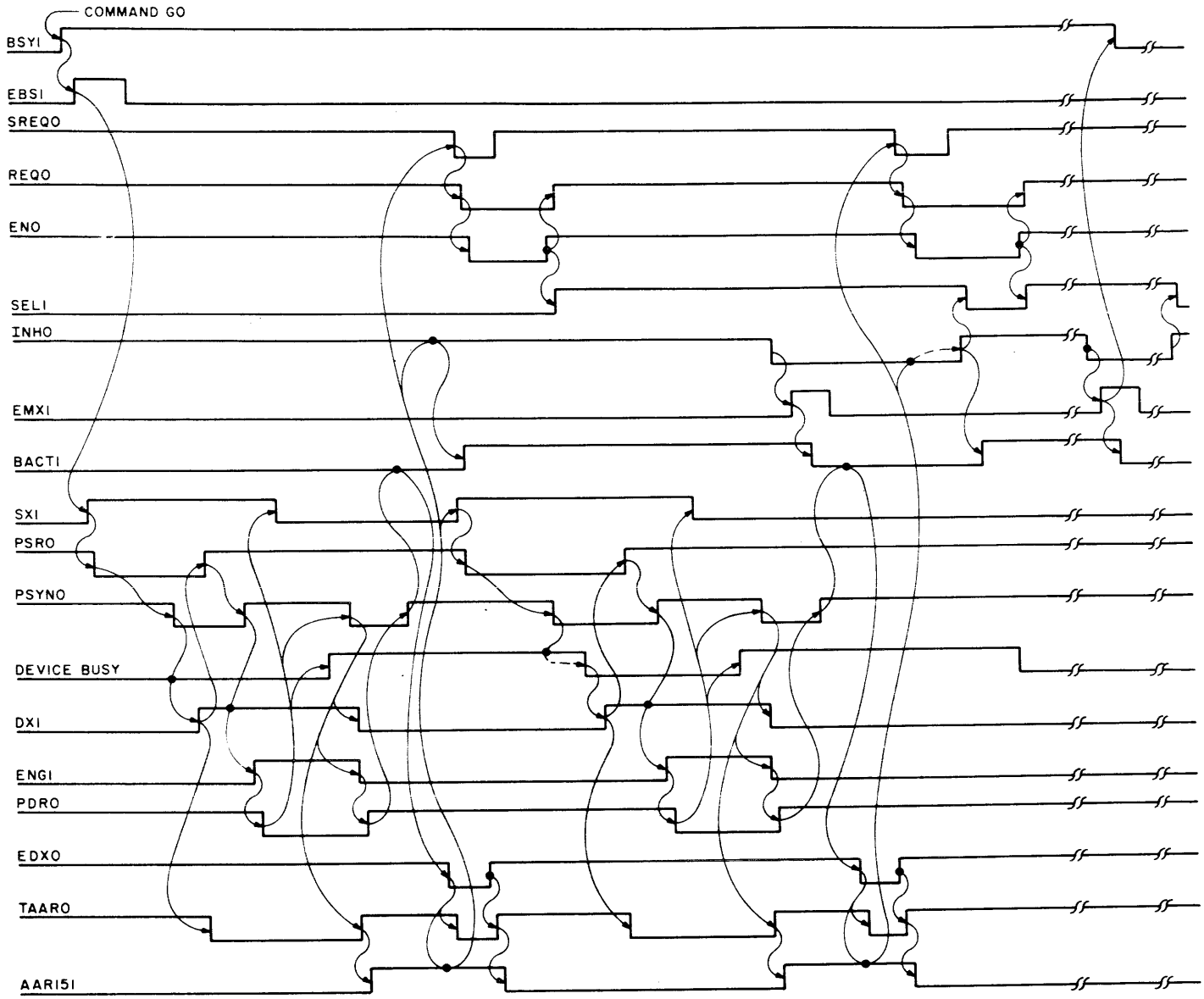


Figure 4. Memory Write (Halfword I/O Mode)

A GO Command to the Selector Channel sets the Busy flip-flop which generates the End of Busy Set pulse (EBS1)(3K8).

In the Memory Read Mode, EBS1 is decoded by the Branch Gate circuit and SREQ0 is generated. Thus, a request for memory is initiated. When the halfword of data is present in the MDR, the End of Memory Transfer pulse (EMX1)(4R6) becomes active and the Branch Gate circuit once again requests memory and generates Set Status Transfer (SSX0)(3S5) and Load Data Buffer (LDB1)(3S7). These signals initiate the transfer to the device and load the Data Buffer respectively.

SSX0 sets the Status Request flip-flop (3F6) which activates the Private Status Request control line (PSR0)(3G6) to the active device on the private SELCH Bus. This Status Request examines the four least significant bits of the Status Byte. If any of the three least significant bits (EX, EOM, or DU) are set, the transfer is terminated by resetting the Busy flip-flop (3F3). The assumption is made that each of these status bits remain reset for the remainder of this discussion. With Bit-12 (Busy) of the Status Byte reset, the Data Transfer flip-flop becomes set (3F7). Data Transfer (DX0)(3E1) inhibits the generation of PSR0, which causes Private Sync (PSYN1)(4B4) from the device to become inactive. This enables Engage to go high (ENG1)(3D8), which allows the Private Data Available control line (PDA0)(3H5) to become active. The Private Data Available/Request signal (PDAR1)(3H5), generated whenever a Private Data Available (PAD0) or Private Data Request (PDR0) signal is active, will then clear the Status Request flip-flop. Upon receipt of Sync from the device, PSYN1 active, the Data Transfer flip-flop becomes reset and ENG1 goes low, disabling PAD0. When the Sync is removed by the device, a 100 millisecond End of Data Transfer pulse is generated (EDX0)(3J8) which increments the Auxiliary Address Register and is used by the Branch Gate circuit to generate a function in accordance with the truth table for EDX on Sheet 3. This cycle continues until termination of the transfer is detected.

In the Memory Write Mode, WT1 active (3F5), EBS1 is used to generate SSX0, and the Branch Gate circuit directs the loading of a halfword of data into the DB before a memory request is made. The transfer of data from the device is the same as described in the Memory Read Mode, except that ENG1 is used to generate the Private Data Request control line (PDR0)(3H5) rather than PDA0. Data from the device is loaded into the MDR on the trailing edge of either Load Data Register High (LDRH0)(2R2) or Load Data Register Low (LDRL0)(2R2), depending on which eight bits are being loaded. In the Halfword Transfer Mode, both LDRH0 and LDRL0 are generated simultaneously. With WT1 active, the generation of EDX1 is delayed by activating the clear input to the one-shot (3H8) when the Buffer Active flip-flop is set (BACT1)(3H1), if either the transfer to the device is on an odd boundary or when a Match is detected (MCH0)(5J2). This prevents the reloading of the Data Buffer before the last halfword has been written into memory.

4.8 RACK0/TACK0 Contention Circuit

The Selector Channel directs the propagation of the Acknowledge signal to lower priority devices on the Multiplexor Channel Bus as well as devices on the private SELCH Bus. If the Selector Channel Attention flip-flop (4B4) is set, the SELCH will capture the Receive Acknowledge signal (RACK0)(4B3), place its device address on the Data Lines and return Sync to the Processor, Attention Sync (ATSYN0)(4F4) active. If the Attention flip-flop is reset, RACK0 is propagated as either Private Transmit Acknowledge (PTACK0)(4F2) or Transmit Acknowledge (TACK0)(4F3). Since devices on the private SELCH Bus have a higher interrupt priority than devices below the SELCH on the MPX Bus; if the Private Attention Test line is active (PATN0)(4B1), PTACK0 will be generated rather than TACK0. Note that when MSC0 is high (3F4), PATN0 is disabled so that a device on the private SELCH Bus may not interrupt the Processor while the SELCH is active.

5. MAINTENANCE, TROUBLE SHOOTING, AND TEST

Before attempting any maintenance or testing, insure that the necessary back panel modifications have been made in accordance with the Model 70 Selector Channel Installation Specification 02-232A20.

To insure a 2,000,000 Byte/second transfer rate in the Byte Transfer Mode, it is necessary to limit the maximum delay between PDA0, PDR0, and PSR0 and the return of Sync from the device (PSYN0), to 30 nanoseconds. In addition, the device must be ready for the next byte of data, Busy Status Bit reset, whenever a Status Request is made. Field testing of this device is contingent upon the user having appropriate software and hardware available with which to exercise the Selector Channel. There are no adjustments associated with this device.

6. MNEMONICS

The following list provides a brief description of each mnemonic found in the SELCH. The source of each signal on Schematic Drawing, 02-232D08, is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AAR001:151	Outputs of the Auxiliary Address Register	5F1-5F9
ACT0	Accept - Request for memory accepted by Processor	4H1
AD1	Address - Active when SELCH is addressed	2K7
ADRS0	Address control line from MPX-Bus	4B8
AG081:151	Address Gated Lines - Output of Address Strap	1E3 - 1E8
ATN0	Attention - Attention to Processor	4F1
ATSYN	Attention Sync - Generated by an Acknowledge Attention from Processor	4F4
BACT1	Buffer Active - Indicates that valid data is present in the DB	3H1
BSY	Busy - Indicates a data transfer is in progress	3F3
CDR0	Clear Data Register - Clears MDR prior to loading from MS000:150	4R2
CBSY0	Clear Busy - Terminates transfer when a match is detected	3M3
CL070	Control Line 7 - Control Line from MPX-Bus	4B6
CLG1	Control Line Gate - Gates Private Control Lines	1C2

MNEMONIC	MEANING	SCHEMATIC LOCATION
CLUS0	Clear Load/Unload Sequencer - Clears Sequencer	3S2
CMD0	Command Control Line from MPX-Bus	4B8
CMG	Command Gated by AD1	2S7
CO0	Carry Out of the AAR - Prevents Memory 'Wrap-around'	5A1
D000:150	Data Lines from MPX-Bus	1A3 - 1A8 2A1 - 2A8
DA0	Data Available Control Line from MPX-Bus	4B7
DLG0	Data Line Gate - Gates Data Lines and Private Data Lines	1R2 - 1D3
DB001:151	Outputs of Data Buffer	6G2 - 6G9 6R2 - 6R9
DR0	Data Request Control Line from MPX-Bus	4B7
DRG0	Data Request Gated by AD1	2L5
DX	Data Transfer flip-flop	3F8
EBS1	End of Busy Set - Signals the start of a SELCH transfer	3J4
EDX1	End of Data Transfer - Signals the end of a device transfer	3J8
EMX1	End of Memory Transfer - Signals the end of a memory transfer	4R7
EN0	Enable from Memory Bus	4H2
ENG1	Engage - Gates either PDS0 or PDR0	3D8
ENMDR1	Enable Memory Data Register Read - Gates contents of MDR to MD000:150	4R6
ENMDW1	Enable Memory Data Register Write - Gates contents of DB to MD000:150	4R3
ENMS1	Enable Memory Strobe - Gates contents of MS000:150 to MDR	4R4
HW0	Halfword Control Line from MPX-Bus	1D2
INH0	Inhibit from Memory Bus	4H5
LARH0	Load Address Register High - Loads AAR and AR, Bits 00:07	2R2
LARL0	Load Address Register Low - Lards AAR and AR, Bits 08:15	2R2
LDB1	Load Data Buffer - Load contents of MDR to DB	3S2
LDRH0	Load Data Register High - Loads MDR Bits 00:07	3F8
LDRL0	Load Data Register Low - Loads MDR Bits 08:15	3H9
LFRH0	Load Final Address Register High - Loads FAR Bits 00:07	2S3
LFRL0	Load Final Address Register Low - Loads FAR Bits 08:15	2S3
MA000:140	Memory Address Lines to Memory Bus	5R1 - 5R8
MCH1	Match - Indicates a match between AAR and FAR	5J6

MNEMONIC	MEANING	SCHEMATIC LOCATION
MD000:150	Memory Data Lines to Memory Bus	6G1 - 6G8 6R1 - 6R8
MS000:150	Memory Strobed Data Lines from Memory Bus	6A1 - 6A8 6H1 - 6H8
MSC0	Multiplexor SELCH Control flip-flop	3F4
PADRS0	Private Address Control Line to SELCH Bus	4F8
PATN0	Private Attention from SELCH Bus	4B1
PCL070	Private Control Line 7 to SELCH Bus	4R6
PCMD0	Private Command Control Line to SELCH Bus	4F8
PD000:150	Private Data Lines - SELCH Bus	2F1 - 2F8 1S3 - 1S9
PDA0	Private Data Available Control Line to SELCH Bus	3H5
PHW0	Private Halfword Control Line from SELCH Bus	1A1
PSR0	Private Status Request Control Line to SELCH Bus	3H6
PSYN0	Private Sync from SELCH Bus	4B5
PTACK0	Private Transmit Acknowledge to SELCH Bus	4F2
RACK0	Receive Acknowledge from MPX-Bus	4B5
RBA0	Reset Buffer Active - Resets Buffer Active flip-flop	3M2
REQ0	Request - Request for memory cycle to Memory Bus	4R5
SCLR0	System Clear - Initialize Signal	4H4
SGAD1	Set Gate - Sets Address flip-flop	2LR
SR0	Status Request Control line from MPX-Bus	4B6
SREQ0	Set Request - Initiates a request for memory	3S4
SSX0	Set Status Transfer - Sets the Status Request flip-flop	3S5
SX	Status Transfer - Status Request flip-flop	3F6
SYN0	Sync to MPX-Bus	2S5
TAC0	Transmit Accept - To lower priority DMAs	4R1
TACK0	Transmit Acknowledge - To lower priority devices on MPX Bus	4F3
TAAR0	Toggle Auxiliary Address Register - Increments AAR	3M1
TAR0	Toggle Address Register - Increments AR	4S7
UAAH0	Unload Auxiliary Address Register High - Unloads AAR Bits 00:07	2R4
UAARL0	Unload Auxiliary Address Register Low - Unloads AAR Bits 08:15	2R4
WT	Write flip-flop	3F5
WRT0A	Write to Memory Bus, when selected	4R3

02-232 SELECTOR CHANNEL PROGRAMMING SPECIFICATION

1. INTRODUCTION

The 02-232 Selector Channel (SELCH) controls the transfer of data between I/O devices and memory at rates of up to 2,000,000 bytes per second. Up to 16 I/O devices can be connected to the Selector Channel, but only one device can transfer data at a time. The advantage in using the Selector Channel is that other program processing can occur simultaneously with the transfer of data between the I/O device and memory. This is accomplished by allowing the Selector Channel and the Processor to access memory on a cycle-stealing basis. In some instances, the execution times of the program in progress are affected, while in others, the effect is negligible. This depends upon the rate at which the Selector Channel and Processor both compete for access to memory. Data transfer to the device may be made in either the Byte or Halfword Mode. Figure 1 is a block diagram which shows the incorporation of the Selector Channel into the INTERDATA peripheral system.

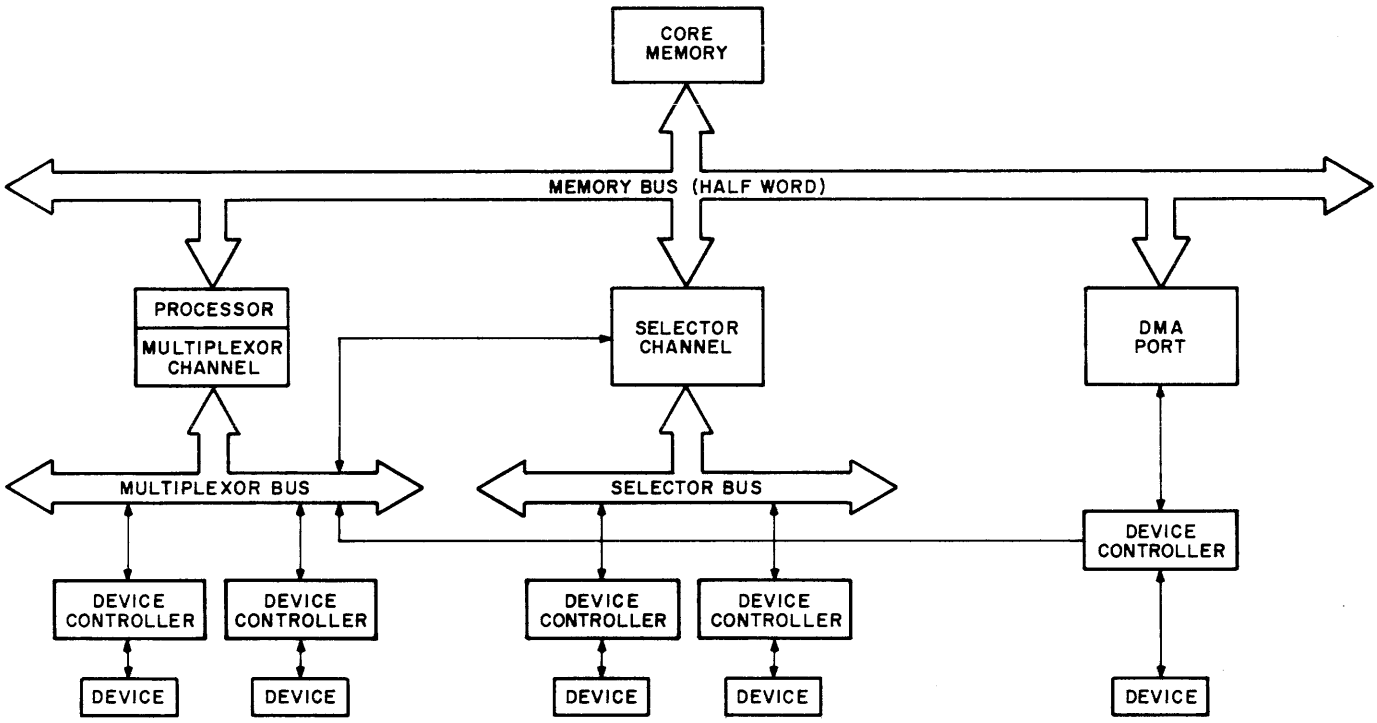


Figure 1. Systems Interface Block Diagram

2. CONFIGURATION

The 02-232 Selector Channel is used with Model 70, Model 80, or other compatible Processors. The Selector Channel requires one 15 inch board, and one slot in a 15" chassis.

The priority of the Selector Channel is determined by its position on the Multiplexor Bus. Devices on the Selector Channel Private Bus have higher priority then devices which appear after the Selector Channel in the daisy chain of the Multiplexor Bus. Refer to 02-232A20 for installation information.

3. OPERATING PROCEDURES

The 02-232 Selector Channel is controlled solely by programmed I/O sequences over the Multiplexor Bus.

4. DATA FORMAT

Not applicable to the 02-232 Selector Channel.

5. PROGRAMMING INSTRUCTIONS

Table 1 illustrates the Selector Channel Status and Command Byte coding. A Sense Status instruction (SS or SSR) is used to transfer the status byte from the Selector Channel Device Controller to the Processor. The least significant four bits (4:7) of the status byte are copied into the Condition Code during the Sense Status operation. Branch instructions can test these four bits directly.

The Output Command instruction (OC or OCR) causes a command byte to be sent to the Selector Channel Controller.

TABLE 1. SELECTOR CHANNEL STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE					BSY			
COMMAND BYTE			READ	GO	STOP			

STATUS

BSY — This bit is set when the Selector Channel is in the process of transferring data.

COMMAND

READ — This command changes the mode of the Selector Channel from Write to Read. In the Read Mode, data is transmitted from the active device on the Selector Channel and written into memory. Whenever a data transmission has been completed, the Selector Channel is placed in the Write Mode. Each time a Read operation is required, a Read Command must be issued.

GO — This command initiates a data transmission. This command can be issued at the same time the Read/Write Mode is established.

STOP — This command halts any data transmission in progress, and initializes the Selector Channel for starting a new operation. It should be given when the Selector Channel terminates.

The Write Data (WD or WDR) or Write Halfword (WH or WHR) instructions may be used to send the starting and final addresses to the Selector Channel Controller.

The Read Data (RD or RDR) or Read Halfword (RH or RHR) instructions may be used to obtain the last Processor memory location either written into or read from memory.

The Read Block (RB or RBR) or Write Block (WB or WBR) instructions should not be used since the status byte produced by an idle SELCH is the status of any active device on the SELCH Bus with Bit-4 (BSY) forced to zero. Depending on the device status, the Read Block or Write Block instructions may terminate.

NOTE

The user should be aware that programs using Block I/O instructions to control the SELCH may not work when using the 02-232 Selector Channel.

If an interrupt is pending, an Immediate Interrupt or Acknowledge Interrupt instruction (AI or AIR) clears the interrupt and causes the device number of the Selector Channel to be sent to the Processor. If the Acknowledge Interrupt instruction is used, the SELCH status is also sensed by the Processor. The SELCH status is the status of the peripheral device in use with BSY forced to a zero.

6. PROGRAMMING SEQUENCES

Programming a device on the Selector Channel consists of setting up the device, setting up the Selector Channel, and sending a GO command to the Selector Channel. When all devices on the Selector Channel are idle, the Selector Bus becomes a part of the Multiplexor Bus. This provides the path to set up the device and the Selector Channel.

The last device addressed prior to sending the GO command is the device the Selector Channel controls, assuming that the device is connected to the Selector Channel. The program must, therefore, send the GO command before addressing any other device. Note that when the SELCH device is being addressed, prior to the GO command, the Single Mode may not be used since the Display Panel is addressed in this mode.

During data transfer, the Selector Channel provides a direct data path between the device and memory. Until the transfer is complete, no I/O instruction can be issued to any device on the Selector Channel Bus, including the device transferring data. If devices on the Selector Channel Bus are referenced while the Selector Channel is busy, the False Sync bit is set (V Condition Code).

The initialization of a device on the Selector Channel Bus is accomplished by executing an Output Command (OC or OCR) instruction. Refer to the device Programming Manual for the bit configuration of the Output Command. Note that the Selector Channel has a unique device number just like all other I/O devices. Output Commands, as with all Input/Output instructions, affect only the device addressed.

The Selector Channel has a 16-bit incrementing Address Register and a 16-bit Final Address Register. The user program loads the starting address into the incrementing Address Register and the final address into the Final Address Register. Transfer is completed when the incrementing Address Register matches the Final Address Register. The address limits are expressed inclusively; transfers begin and end on the addresses placed in the starting and final address registers.

The memory is addressed on halfword boundaries; that is, each time memory is accessed, two bytes or a halfword are obtained. 16-bit addressing is used, with the least significant bit, Bit-15, determining the byte desired. See Figure 2.

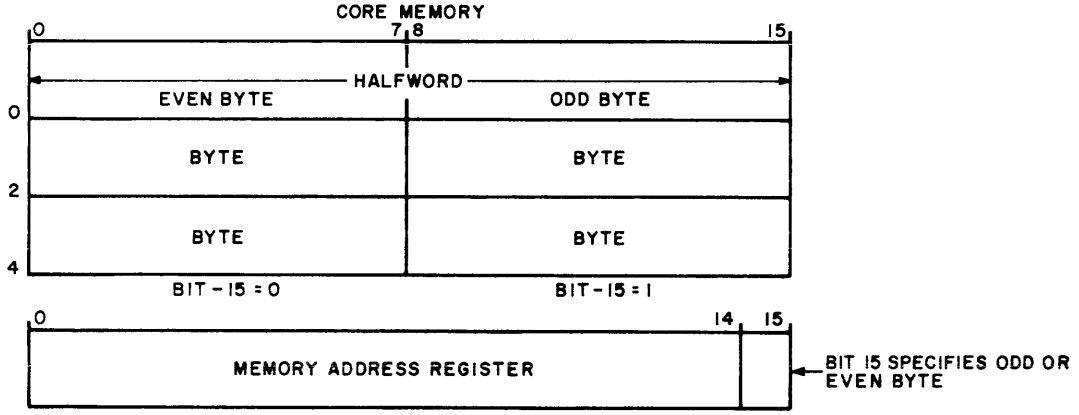


Figure 2. Memory Addressing

Each time the Selector Channel accesses memory, two bytes (halfword) are transferred. It is mandatory that data transfers begin on a halfword boundary. The following results if data transfers are ended on byte boundaries:

1. Write Mode (memory to device) - End on byte boundary (Bit-15 = 0) - No effect.
2. Read Mode (device to memory) - End on byte boundary (Bit-15 = 0) - The previous contents of the last odd byte in memory is written into the current odd byte in memory. See Figure 3.

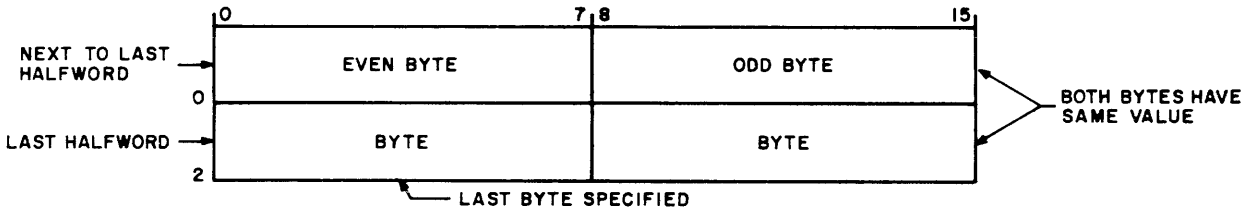
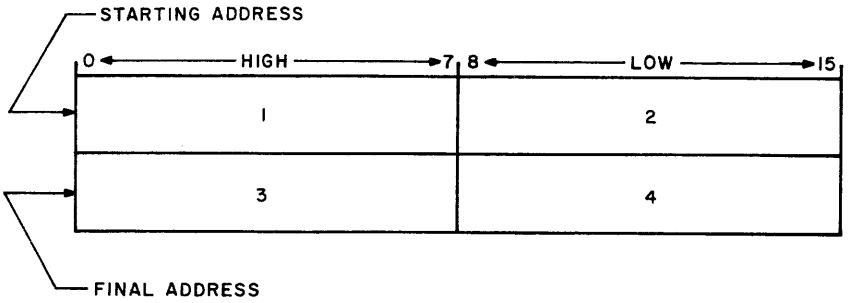


Figure 3. Memory Configuration, End on Byte Boundary

The user program specifies the mode, either Read or Write, and gives the GO command. The following sections provide details for programming the Selector Channel.

6.1 Starting and Final Addresses

An Output Command with the Stop bit set should be issued prior to starting any operation on the Selector Channel to clear any preceding conditions. Four successive bytes are required to specify the starting and final addresses of the user's buffer area. Either the Write Data (WD or WDR) or Write Halfword (WH or WHR) instructions may be used to send the starting and final addresses to the Selector Channel Controller. Figure 4 defines the four bytes used for addressing.



1. Starting Address High (Bits 0:7)
2. Starting Address Low (Bits 8:15)
3. Final Address High (Bits 0:7)
4. Final Address Low (Bits 8:15)

Figure 4. Starting and Final Address Data Bytes

6.2 Status and Commands

A Sense Status instruction (SS or SSR) is used to transfer the status byte from the Selector Channel Device Controller to the Processor. The least significant four bits (4:7) of the status byte are copied into the Condition Code during the Sense Status operation. Branch instructions can test these four bits directly. The status byte returned by the SELCH when idle, is the status of any device on the SELCH Bus with Bit-4 (BSY) forced to a zero. The Output Command instruction (OC or OCR) is used for transmitting the command byte to the Selector Channel Controller.

6.3 Termination

Data transmission between the Selector Channel and the device presently connected to it is halted if any of the following conditions occur:

1. The starting address matches the final address. This denotes a normal termination.
2. The starting (incrementing) address goes from all Ones to all Zeros (maximum count). In this case, a match has not occurred and is considered an abnormal termination.
3. Any of the DU, EOM, or EX status bits of the device presently connected to the Selector Channel changes to a One. This is also an abnormal termination.
4. A Stop command is sent to the Selector Channel via a user program.

The termination condition is determined in one of two ways: by a status scan, or by the interrupt method. These methods are described in the following paragraphs. An Output Command Stop should be issued to the Selector Channel following its termination.

NOTE

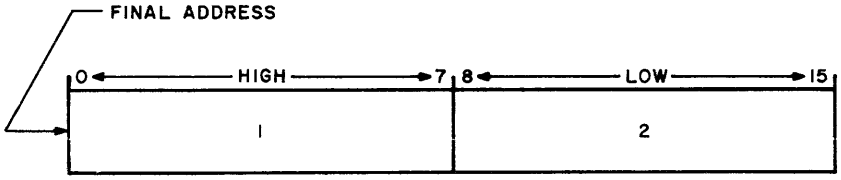
In the status scan method of programming, it is possible for the Busy Bit to change from One to Zero during a Sense Status instruction without returning the SELCH to Idle. To guarantee the Idle Mode after Busy = 0 on the Sense Status instruction, a Stop command should be sent to the SELCH.

Status Scan. The status of the Selector Channel Controller may be examined by issuing a Sense Status instruction (SS or SSR). The Busy Bit (Bit-4) is a One while transmission is in progress, and Zero when transmission is terminated. One method of testing for termination would be to continually or periodically test the Busy Bit of the Selector Channel Controller. The change from One to Zero would then indicate the termination of a data transfer. When the Selector Channel is busy, only the Busy Bit (Bit-4) is present in the status byte and all other bits are Zero. At termination, the status of the device is presented in the status byte, except for the Busy Bit which is Zero.

Interrupt Method. When data transmission is initiated on the Selector Channel, the interrupts are always enabled. If external device interrupts are enabled (PSW Bit-1 set), the Processor is interrupted when the Selector Channel terminates. The interrupt can be serviced via Immediate Interrupt or Acknowledge Interrupt instruction (AI or AIR), which clears the interrupt and causes the device number of the Selector Channel (X'F0' preferred) and status of the peripheral device to be sent to the Processor. The Busy Bit is treated in the manner described previously for Status Scan.

6.4 Reading the Final Address

The last Processor memory location either written into or read from may be obtained by executing a pair of Read Data instructions (RD or RDR) or a Read Halfword instruction (RH or RHR). The Read Block instruction (RB or RBR) should not be used. This information permits a user program to verify a successful data transmission or determine at what address termination occurred. Figure 5 illustrates the order in which the data is read into the Processor.



1. Final Address High (Bits 0:7)
2. Final Address Low (Bits 8:15)

Figure 5. Read Data Instructions

7. INTERRUPTS

Refer to Section 6.3 Termination, Interrupt Method.

8. INITIALIZATION

Whenever the Initialize switch (INT) on the Display Panel is depressed, or a Stop command is issued, the following actions occur:

1. Any data transmission in process is halted and the Stop Mode is effected.
2. The Selector Channel is placed in the Write Mode.
3. The Selector Channel is placed in the Idle Mode.
4. The Selector Channel interrupt is reset.

9. DEVICE NUMBER

The Selector Channel is normally assigned device number X'F0', but may easily be changed by a minor wiring modification on the Selector Channel Device Controller board. Refer to the Installation Specification, 02-232A20, for specific details.

10. SAMPLE PROGRAM

Appendix 1 presents a sample driver program for a magnetic tape unit connected to the Selector Channel. The purpose of this sample program is to show the program instructions used to control the Selector Channel and the order in which they may be executed.

The function of Subroutine 1 is to prepare the Selector Channel and device for a data transfer. Upon entry to Subroutine 1, Steps 1, 2, and 3 load the device number of the Selector Channel into a register and tests the Selector Channel's Busy Bit. If the Busy Bit is set, return is made to the calling program via the Busy Exit. If the Selector Channel is idle, Steps 5 and 6 test the status of the tape unit. If the tape unit status reveals it is available, Step 7 sends a command to the tape unit. If the tape unit is not available, return is made to the calling program via the error return exit. Steps 8 through 11 load the Selector Channel's Address Register. Step 12 then gives the GO command to the Selector Channel initiating the data transfer.

The function of Subroutine 2 is to service the interrupt caused by the Selector Channel. Step 14 acknowledges the interrupt, and at the same time loads the status of the device into register Status. Steps 15 and 16 read the incrementing (start) register of the Selector Channel and load the results into memory locations, LFINLH and LFIXLL. Steps 17 through 19 compare the actual ending address to that loaded into the Final Address Register. If not equal, return is made to the call program via the error return exit; if equal, return is made to the normal return.

APPENDIX 1
SAMPLE PROGRAM

```
                        *
                        * SAMPLE DRIVER PROGRAM FOR A MAGNETIC
                        * TAPE UNIT UNDER CONTROL OF SELECTOR
                        * CHANNEL INTERFACE
                        *
                        * NORMAL RETURN -REGISTER 15
                        * BUSY RETURN - REGISTER 15+4
                        * ERROR RETURN - REGISTER 15+8
                        *
                        * SUBROUTINE 1 INITIALIZES DEVICE AND SELECTOR CHANNEL
                        *
0000R C8A0      SUBR1   LHI     SCDVNU,X'F0'    (1) LOADS DEVICE NUMBER OF
        00F0
                        *                               SEL CHAN IN REGISTER
0004R 9DAC              SSR     SCDVNU,STATUS   (2) TEST SEL CHAN AVAIL-
0006R 428F              BTC     8,4(RETURN)     (3) BUSY RETURN
        0004
000AR C8B0              LHI     TPDVNU,X'20'    (4) LOADS DEVICE NUMBER OF
        0020
                        *                               TAPE UNIT IN REGISTER
000ER 9DBC              SSR     TPDVNU,STATUS   (5) TEST TAPE UNIT AVAIL-
                        *                               ABLE FOR COMDS
0010R 45C0              CLH     STATUS,COMSAT   (6) TST  STATUS OF TPE UNIT
        005AR
0014R 423F              BNE     8(RETURN)       ERROR RETURN
        0008
0018R DEB0              OC      TPDVNU,CMDMOD   (7 ) COMMANDS TAPE UNIT TO
        0052R
                        *                               READ  MODE
001CR DEA0              OC      SCDVNU,RESET    RESET SC REGISTERS
        0054R
                        *
0020R DAA0              WD      SCDVNU,STARTH   (8 ) SENDS BITS 0-7 OF
        0056R
                        *                           START ADDR TO SEL CHAN
0024R DAA0              WD      SCDVNU,STARTL   (9 ) SENDS BITS 8-15 OF
        0057R
                        *                           START ADDR TO SEL CHAN
0028R DAA0              WD      SCDVNU,FINALH   (10) SENDS BITS 0-7 OF
        0058R
                        *                         END ADDR TO SEL CHAN
002CR DAA0              WD      SCDVNU,FINALL   (11)SENDS BITS 8-15 OF
        0059R
                        *                           END ADDR TO SEL CHAN
0030R DEA0              OC      SCDVNU,GORD     (12) STARTS DATA TRANSFER
        0053R
                        *                                   BETWEEN TAPE AND CORE
0034R 030F              BR      RETURN          (13) RETURN TO CALLING ROUTINE
                        *
                        ********************************************************
                        * SUBROUTINE 2 SERVICES INTERRUPT RETURN
                        *
0036R 9F9C      SBUR2   AIR     DEVICE,STATUS   (14) ACKNOWLEDGE INTERRUPT
                        *                               AND OBTAIN STATUS
0038R DEA0              OC      SCDVNU,RESET    SEND STOP TO SELECTOR
        0054R
```

```
                        *                                       CHANNEL FOLLOWING TERM.
003CR DBA0                      RD      SCDVNU,LFINLH   (15) READ SEL CHAN BITS
      005CR
                        *                                       0-7 FOR ENDING ADDR
0040R DBA0                      RD      SCDVNU,LFINLL   (16) READ SEL CHAN BITS
      005DR
                        *                                       8-15 FOR ENDING ADDR
0044R 48E0                      LH      TEST,LFINLH     (17) LOADS ACTUAL ENDING ADDR
      005CR
0048R 45E0                      CLH     TEST,FINALH     (18) TO COMPARE WITH SPECIFIED
      0058R
004CR 423F                      BNE     8(RETURN)       (19) ERROR RETURN
      0008
0050R 030F                      BR      RETURN          (20) RETURN TO CALLING ROUTINE
0052R 9930      CMDMOD  DC      X'9930'
0053R           GORD    EQU     CMDMOD+1
0054R 0808      RESET   DC      X'0808'
0056R           STARTH  DS      2
0057R           STARTL  EQU     STARTH+1
0058R           FINALH  DS      2
0059R           FINALL  EQU     FINALH+1
0009            DEVICE  EQU     9
000A            SCDVNU  EQU     10
000B            TPDVNU  EQU     11
000C            STATUS  EQU     12
000D            ADDR    EQU     13
000E            TEST    EQU     14
000F            RETURN  EQU     15
005AR           COMSAT  DS      2               CONTAINS EXPECTED STATUS
005CR           LFINLH  DS      2
005DR           LFINLL  EQU     LFINLH+1
005FR                   END
ADDR    000D
CMDMOD  0052R
COMSAT  005AR
DEVICE  0009
FINALH  0058R
FINALL  0059R
GORD    0053R
LFINLH  005CR
LFINLL  005DR
RESET   0054R
RETURN  000F
SBUR2   0036R
SCDVNU  000A
STARTH  0056R
STARTL  0057R
STATUS  000C
SUBR1   0000R
TEST    000E
TPDVNU  000B
```

MODEL 70 MEMORY PROTECT INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-236 Memory Protect Module in a Model 70 Processor System. The module assembly consists of one 35-396 7" board and one 17-169 cable. The 35-396 7" board must be strapped to a blank 7" board or an active 7" board (e.g. Universal Clock Module) by an INTERDATA 16-398 Half Board Kit, so that it may be installed in a chassis designed for standard 15" boards. The Memory Protect Module may be installed in either the right or left half position, depending on the system configuration. See Figure 1.

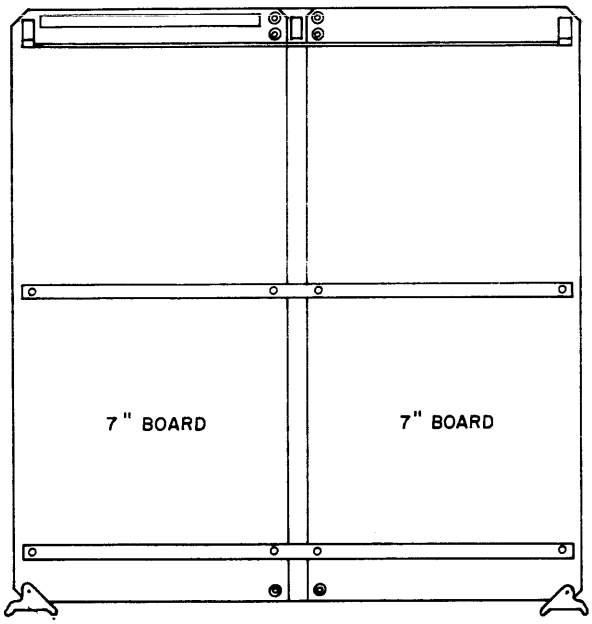


Figure 1. 7" Board Assembly

2. UNPACKING

When the Memory Protect Module is shipped with a system, it is installed at the factory so there is no special unpacking procedure. If the module assembly is purchased separately, it should be inspected for damage prior to installation.

3. LOCATION

The 35-396 Memory Protect Module 7" board, once assembled using a half board kit, may be installed in any available I/O slot of a standard 15" chassis which is located no more than one chassis from the Processor.

NOTE

Normally it is required that the Memory Protect Module be installed as the highest priority device controller (with respect to interrupts) on the Multiplexor Bus to insure proper recognition and response to Memory Protect violation interrupts that may occur in the system. This is accomplished by installing the Memory Protect Module in the first available I/O slot with respect to the daisy chain priority line, and rerouting the RACK0/TACK0 line which is ordinarily connected first to the built-in Teletypewriter controller. See Section 4.

4. BACK PANEL WIRING

To insure that the Memory Protect has the highest priority on the Multiplexor Bus, the RACK0/TACK0 line on the Processor chassis back panel must be rerouted. Refer to Figure 2 during the following rerouting procedure.

1. Remove the RACK0/TACK0 jumper from the slot occupied by the Memory Protect Module. The jumper is located between Terminals 122 and 222 on the selected slot.

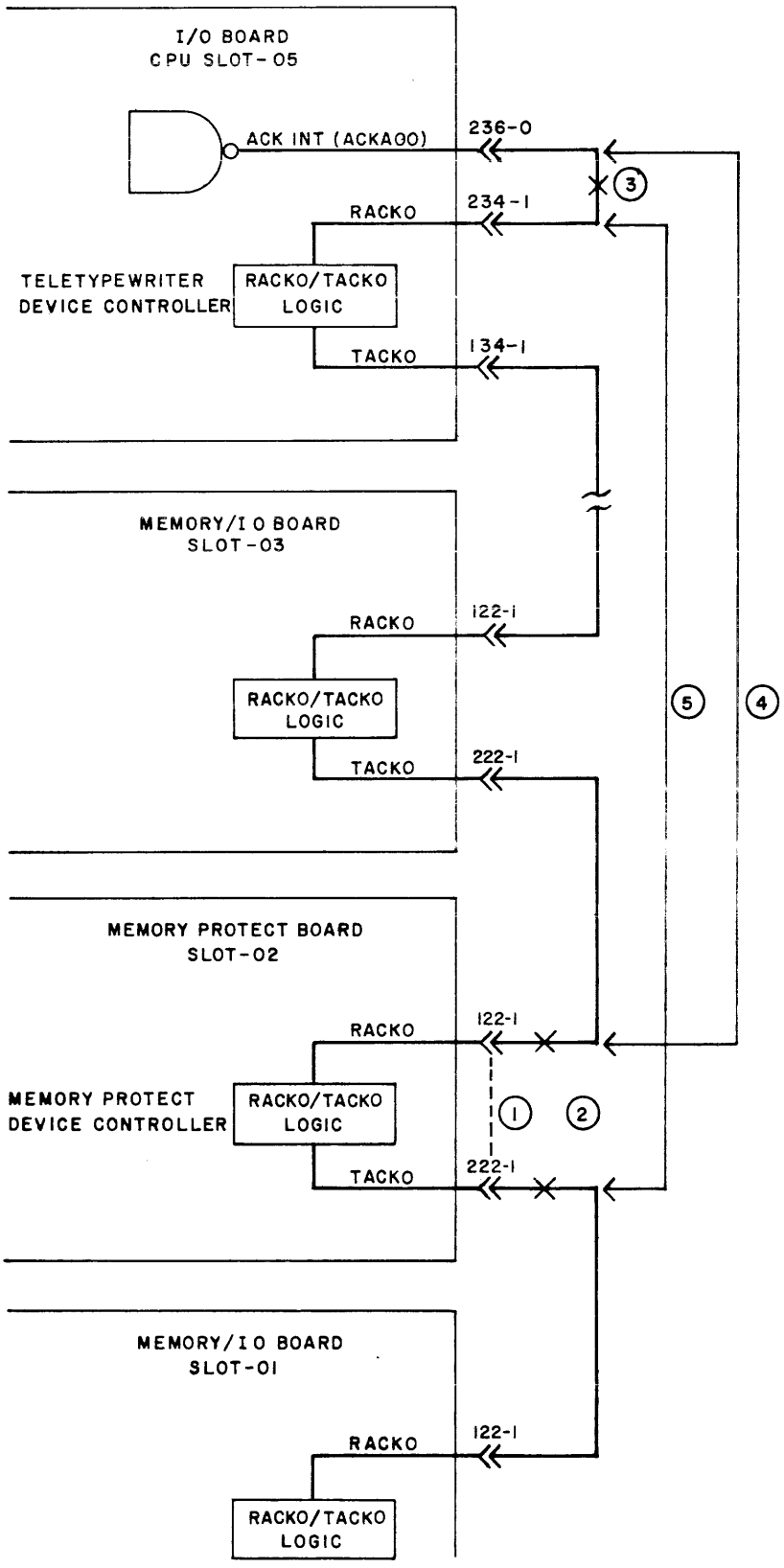
2. Break the daisy chain line from the next higher priority device controller and to the next lower priority device controller, at Terminals 122-1 and 222-1 on the Memory Protect Module's selected slot. Connect the TACK0 Terminal 222-1 from the next higher priority device to the RACK0 Terminal 122-1 on the next lower priority device controller on the Multiplexor Bus. This removes the Memory Protect Module from the daisy chain priority sequence, and re-establishes the daisy chain to lower priority device controllers.

3. Break the connection between Acknowledge Interrupt (ACKA00) Terminal 236-0 and Teletypewriter Receive Acknowledge (RACK0) Terminal 234-1 on the I/O Board, Slot 5. This disconnects the Teletypewriter device controller from the Acknowledge Interrupt (ACKA00) line.

4. Connect a jumper between Memory Protect Module RACK0 Terminal 122-1 and I/O Board ACKA00 Terminal 236-0. This connects the Memory Protect Module as the first device controller in the RACK0/TACK0 line.

5. Connect a jumper between Memory Protect Module TACK0 Terminal 222-1 and I/O Board Teletypewriter RACK0 Terminal 234-1. This connects the Teletypewriter as the second device controller in the RACK0/TACK0 line.

The Memory Protect Module is now the highest priority device controller in the daisy chain. The built-in Teletypewriter device controller is second in priority and the remaining device controllers are as before in their required sequence.



NOTE: THE CIRCLED NUMBERS REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING RACKO/TACKO LINE REROUTING PROCEDURE

(1) REMOVE RACKO/TACKO JUMPER ON THE SELECTED SLOT

(2) BREAK DAISY CHAIN LINE AT TERMINALS 122-1 AND 222-1 ON THE SELECTED SLOT. CONNECT NEXT HIGHER PRIORITY DEVICE TERMINAL 222-1 TO NEXT LOWER PRIORITY DEVICE TERMINAL 122-1

(3) BREAK CONNECTION BETWEEN THE I/O BOARD TERMINAL 236-0 AND THE TELETYPEWRITER DEVICE CONTROLLER TERMINAL 234-1

(4) CONNECT JUMPER BETWEEN MEMORY PROTECT MODULE TERMINAL 122-1 AND I/O BOARD TERMINAL 236-0

(5) CONNECT JUMPER BETWEEN MEMORY PROTECT MODULE TERMINAL 222-1 AND I/O BOARD TELETYPEWRITER DEVICE CONTROLLER TERMINAL 234-1

Figure 2. RACK0/TACK0 Rerouting with Memory Protect Module

5. CABLE CONNECTION

Install the 17-169 cable between the 35-396 Memory Protect board and the 35-387 Memory Control board. See Figure 3. The Memory Control board is located in Slot 4 of the Central Processor Unit (CPU) chassis.

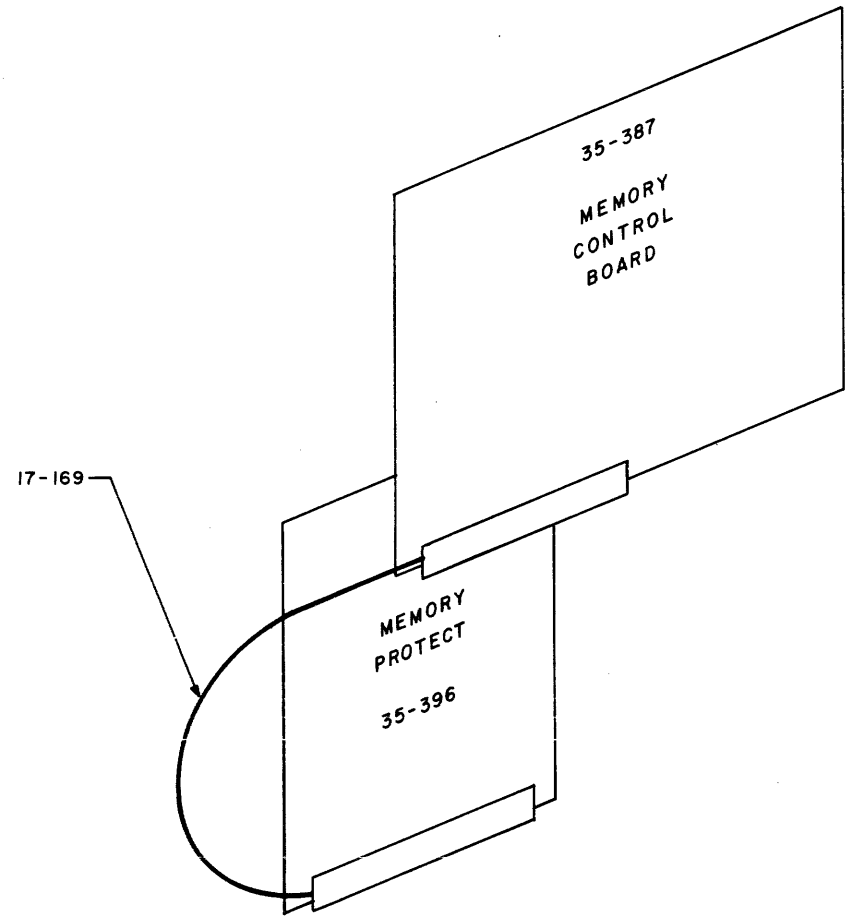


Figure 3. Cable Connection

6. STRAP OPTIONS

6.1 Address Strapping

The preferred address of the Memory Protect Controller is X'AE'. The module is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-236D08, Sheet 1.

6.2 Block Size Option

The Memory Protect Controller is strapped for 1,024 Byte blocks at the factory. To change the block size, refer to the Block Size Table on Sheet 2 of Functional Schematic 02-236D08.

NOTE

The alpha-numeric designations referred to on the functional schematic, indicate similar designations on the apparatus side of the printed circuit board.

7. INSTALLATION CHECKS

To insure proper operation of the Model 70 Memory Protect, Test Program 06-123F04 should be executed in accordance with its test program description.

MODEL 70 MEMORY PROTECT MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-236 Model 70 Memory Protect provides a means of allocating selected blocks of memory to be protected. The Memory Protect Controller (MPC) converts a Write operation to any location in a protected block to a Read operation, notifies the Processor via an interrupt, and sets a status bit in the controller. The memory may be partitioned into a maximum of 64 blocks with individual protect control for each block. An overall protection override provides a means of loading any area in memory.

The Model 70 Memory Protect consists of one Memory Control mother-board and one cable. The cable interconnects the Memory Protect Controller with the Memory Control board of the Central Processor Unit (CPU). Refer to the Installation Specification, 02-236A20, for necessary installation information.

2. SCOPE

This specification describes the functional operation of the Memory Protect Controller and its associated circuits in the Processor. This specification contains a block diagram analysis, a functional diagram analysis, timing information, and a mnemonic list for the Memory Protect Controller. Strapping information for block size selection is found on Sheet 2 of Functional Schematic 02-236D08.

3. BLOCK DIAGRAM ANALYSIS

Refer to the block diagram of the Memory Protect Controller (MPC) on Sheet 3 of Functional Schematic 02-236D08.

Prior to installation, the Memory Protect should be strapped for the desired block size. The following block sizes may be selected; 512 bytes, 1,024 bytes, or 2,048 bytes. Refer to the table on Sheet 2 of Functional Schematics 02-236D08 for strapping information.

Having selected the desired block size, the MPC is setup by the Processor via the Multiplexor Channel Bus. This setup includes the loading of the 64-bit Mask Register with the block or blocks to be protected, either selecting or overriding the protect function, and either arming or disarming the I/O interrupts at the controller. The loading of the 64 bit Mask Register is accomplished by steering up to eight Data Availables (DAs), by the Control Circuit, to the Mask Register. The most significant bit of the first DA corresponds to block one, the next less significant bit of the first DA corresponds to block two, etc.

The Memory Protect Controller constantly monitors the true outputs from the Memory Address Register in the Processor (MA001A:MA061A) and generates Protected Address (PRTAD1) whenever a protected memory address, as defined by the 64-bit Mask Register, is accessed. Meanwhile, if protect is enabled at the Processor, and a Write operation is attempted, Protect (PRTECT0) is generated on the Memory Control board and sent to the MPC. PRTECT0 is ANDed with Protected Address (PRTAD1) and Override Protect (ORP1), by the MPC Control Circuit, to generate CWR0. CWR0 is in turn sent to the Read flip-flop on the Memory Control board. It sets the Read flip-flop which disables the Write attempt and causes a normal Read operation to be performed.

CWR0 also sets a status bit in the controller and generates an interrupt, when enabled, to indicate to the program that an attempt was made to Write to a protected area in memory.

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

To understand INTERDATA functional schematics, it must be noted that the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D080 is Data Line Number 8 and the last character 0 means that when D080 is active, the line is at a logical Zero level.

This section relates to Functional Schematic 02-236D08.

4.2 Multiplexor Bus Communication

When the Memory Protect Controller is addressed by the Processor, all highs are presented to the inputs of the NAND gate at 1G3. The output from this gate is inverted and applied to the J input of the Address flip-flop (AD)(1L3) while the non-inverted signal is applied to the K input of the Address flip-flop. The trailing edge of ADRS0 toggles the Address flip-flop set producing AD1.

The Processor is notified that the address was recognized by a device controller by activating SYN0 (1H7). SYN0 is generated by ADSYN0 (1D6), which is the ANDed output of ADRS1 and the recognition of the address. SYN0 is generated for each of the other control signals (CMD, DR, DA, and SR) by gating them with an active AD1 and applying the gated output to the NAND gate at 1E7.

If an interrupt is generated by this controller, the Attention flip-flop (1J9) is set, and Attention (ATN0) is sent to the Processor. When the Processor acknowledges this interrupt, Receive Acknowledge (RACK0)(1L8) becomes active. RACK0 is inverted and applied to the contention circuit (1R5) which generates either Attention Sync (ATSYN0), when ATN1 is active or Transmit Acknowledge (TACK0), when ATN1 is inactive. ATSYN1 (1H8) gates the address onto Data Lines 8:15, and its falling edge resets both the ATN and the Write Attempt (WATT) flip-flops. Interrupts may be enabled and disabled, via program control, by the setting or clearing of the ARM/DISARM flip-flop (1M7). Initialize (SCLR0 active) or an Output Command with Bit-8 active and Bit-9 inactive, sets this flip-flop to the Disarm state, and an Output Command with Bit-8 inactive and Bit-9 active, places it in the Arm state. In the Disarm state, a low is presented to the direct clear input of the ATN flip-flop, preventing it from becoming set.

4.3 Status and Command

The Status and Command Byte data is shown in Table 1.

TABLE 1. MEMORY PROTECT STATUS AND COMMAND BYTE DATA.

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE			PON	PWF		EX		
COMMAND BYTE	DISARM	ARM	PON	POFF				

PON	Indicates that protect is enabled.
PWF	Indicates that an attempt was made to Write into a protected memory area. This bit is reset by an Output Command, or an Acknowledge Interrupt instruction.
EX	Examine is set when PWF is set.
DISARM	Disables interrupts. They will not be queued.
ARM	Enables interrupts.
PON	Enables the protect function on the controller.
POFF	Disables the protect function on the controller.

4.4 Load Mask Sequencer

The load mask sequencer steers up to eight Data Availables (DAs) to load the 64-bit Mask Register with the desired protect pattern. The four-bit counter (2L7) is initialized by CLl which is the OR output from SCLR0 and CMG0 (1H9). When initialized, all outputs from the counter are at a logical Zero level. This causes the first DA to activate BADG20 which enables the loading of the two 4 x 4 register stacks located at 2G2 and 2G6. Since BAD01 and BAD11 are both low, the first DA loads Word '0' into the two registers. The trailing edge of DAG0 increments the counter, allowing the next DA to load Word '1' into the same two registers (BAD0l active). For the last four DA outputs, output C from the counter is high causing these DAs to activate BADG30 which enables the loading of the remaining two register stacks. If more than eight DAs are issued, wrap-around occurs (i.e., the ninth DA will once again load Word '0' into the first pair of registers).

4.5 Protect Pattern Recognition

The Memory Protect Controller constantly monitors the true outputs from the Memory Address Register (MAR) in the Processor (MA001A:MA061A). The MAR outputs are strapped in accordance with the table on Sheet 2 of Functional Schematic 02-236D08 for the desired block size, to generate Memory Address Lines MA01 to MA051 (2C3-267). The four most significant signals, MA01:MA031, are decoded by the four-to-four line decoder (2D2-2D9) to enable one of the four register stacks and to select one of the four-bit words of that register for a particular group of memory addresses.

Each of the four outputs from the four-bit register stacks is OR tied with the corresponding output from the other register stacks (i.e., the 1 output from register 35 is OR tied with the 1 output from register stacks 34, 33, and 32), but only the selected stack may be active. The two least significant memory address bits monitored by the Memory Protect Module for any given block size, MA41 and MA51, are used to select one of the four outputs of the selected register stack (2L3). This selection is accomplished by the four-to-one line multiplexor (2M8). If the selected data input to the multiplexor is high, the Protected Address signal (PRTAD1) is active.

Each time a Memory Write function is decoded by the Processor with Program Status Word (PSW) Bit-7 set, PRTECT0 is generated unless the Write function is a privileged write. The one-shot at 2K5 generates a pulse approximately 60 nanoseconds in duration on the trailing edge of PRTECT0. This pulse, when the protect function is enabled in the module, ORP1 and PRTAD1 active, generates CWR0 and ASATN0. These signals (CWR0 and ASATN0) cause the Write attempt by the Processor to be converted into a Read operation, and the Attention flip-flop in the Memory Protect Module to be set respectively.

5. TIMING

Refer to Figure 1. Worst case delays are indicated.

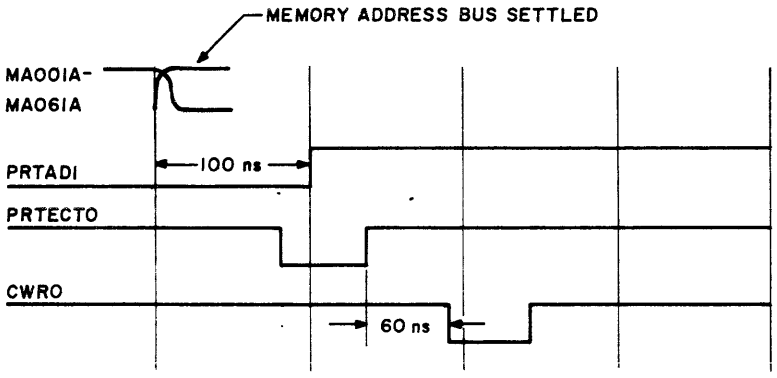


Figure 1. Memory Protect Timing

6. MAINTENANCE AND TESTS

The Memory Protect Module requires no adjustments. Before attempting any maintenance or testing, insure that the cable and the controller are installed properly. Refer to the Installation Specification, 02-236A20, for necessary installation information.

To test the Memory Protect Module, run the Memory Protect Test 06-123F04 in accordance with its test program description.

7. MNEMONICS

The following list provides a brief description of each mnemonic in the Memory Protect Module. The source of each signal on Schematic Drawing 02-236D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AD	Address flip-flop	1M3
ADRS0	Address control line from CPU	1J4
ADSYN0	Address Sync - Causes Sync to be returned on an ADRS0	1M4
ASATN0	Set Attention - Sets the Attention flip-flop on a protect violation	2R4
ATN	Attention flip-flop	1J8
ATSYN0	Attention Sync - Causes Sync to be returned on an Acknowledge Interrupt	1S5
BAD01-11	Block Address - Selects the indicated word in the 64-bit Mask Register	2M6
BADG20-30	Block Address Gated - Enables the indicated pair of registers in the 64-bit Mask Register	2S6
CL1	Clear - Initialize the load mask sequencer on a Command or System Clear	1K9
CMD0	Command control line from the CPU	1A6
CWR0	Convert Write to Read - To CPU to change the Write operation into a Read operation	2S4
D080:D150	Data Lines from the CPU	1A1 - 1A5
DA0	Data Available control line from the CPU	1A7
DR0	Data Request control line from the CPU	1A7
MA001A:061A	Ungated Memory Address from the Memory Address Register	2A3 - 2A9
MA01:051	Memory Address lines selected by the Block Size strapping	2C4 - 2C7
ORP1	Override Protect - Overrides the protect function of the Memory Protect Module	1L1
PRTAD1	Protected Address - Indicates that the Memory Address Register in the CPU contains a protected address when active.	2N3
PRTECT0	Protect - Generated by the Processor when a non-privileged Write attempt is made	2J5
RACK0	Receive Acknowledge - Acknowledge from the lower priority device in the RACK0/TACK0 daisy chain	1L8
SCLR0	System Clear from the CPU	1A8
SR0	Status Request control line from the CPU	1A8
SYN0	Sync - Composite Sync signal to the CPU	1G7
TACK0	Transmit Acknowledge - Acknowledge to the higher priority device in the RACK0/TACK0 daisy chain	1S6

MODEL 70 MEMORY PROTECT PROGRAMMING SPECIFICATION

1. INTRODUCTION

The 02-236 Model 70 Memory Protect provides a means of allocating selected blocks of memory to be protected from user writing. The Memory Protect Controller (MPC) converts a Write operation to any location in a protected block to a Read operation, notifies the Processor via an interrupt, and sets a status bit in the controller. The memory may be partitioned into a maximum of 64 blocks with individual protect control for each block. Block sizes of 512 bytes, 1,024 bytes, or 2,048 bytes may be selected by strap options on the controller. Refer to Installation Specification 02-236A20, for block size strapping information. An overall protection override provides a means of disabling the protect function at the controller. Note that the protect function is enabled at the Processor only when Bit-7 of the current Program Status Word is set. When Bit-7 is reset, all Writes are treated the same as Privileged Writes (i.e. protect disabled).

2. CONFIGURATION

The Model 70 Memory Protect consists of one Memory Control mother-board and one cable. The cable interconnects the Memory Protect Controller with the Memory Control Board in the Central Processor Unit (CPU). The priority of the Memory Protect Controller on the Multiplexor Bus is determined by its installation in the systems chassis. Refer to 02-236A20 for installation information.

> NOTE
>
> It is imperative that the Memory Protect Controller have the highest priority on the Multiplexor Bus, to avoid ambiguity in identifying the source of a protect violation when executing interrupt routines with I/O interrupts enabled.

3. OPERATING PROCEDURES

The Model 70 Memory Protect is controlled by programmed I/O sequences using the Multiplexor Bus. See Sections 5 and 6.

4. DATA FORMAT

Refer to Appendix 1 for the definition of the Load Mask Bytes.

5. PROGRAMMING INSTRUCTIONS

The Output Command instruction (OC or OCR) causes a command byte, as defined in Table 1, to be sent to the controller. Any command causes all status except Protect On (PON) to be reset, and the Load Mask Sequencer to be initialized. The Sense Status instruction (SS or SSR) is used to read the status byte, as defined in Table 1, from the Memory Protect Controller. The status byte reflects the operational state of the controller. The least significant four bits (4:7) of the status byte are copied into the Condition Code of the current Program Status Word so they can be tested directly by the use of Branch instructions.

The Write Data (WD or WDR), Write Halfword (WH or WHR), or the Write Block (WB or WBR) instructions may be used to load the protect pattern into the controller.

TABLE 1. MEMORY PROTECT STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE			PON	PWF		EX		
COMMAND BYTE	DISARM	ARM	PON	POFF				

STATUS

PON	Indicates that protect is enabled.
PWF	Indicates that an attempt was made to Write into a protected memory area. This bit is reset by an Output Command, or an Acknowledge Interrupt instruction.
EX	Examine is set when PWF is set.

COMMAND

DISARM	Disables interrupts. They will not be queued.
ARM	Enables interrupts.
PON	Enables the protect function at the controller.
POFF	Disables the protect function at the controller.

If an interrupt is pending, the Acknowledge Interrupt instruction (AI or AIR) clears the interrupt and causes the interrupting device address and status to be read into the Processor. Executing an Acknowledge Interrupt instruction when no interrupt is pending, results in a device address of zero and a status of X'04'.

6. PROGRAMMING SEQUENCE

The setting up of the Memory Protect Controller consists of loading the desired protect pattern into the controller, enabling the protect function, and either Arming or Disarming the interrupts. Any Output Command initializes the load sequencer in the controller so that the first byte to the protect module, following the Output Command, will load the Mask Register, Blocks 0:7. Refer to Appendix 1 for the correspondence between the load mask bytes, block size, and memory addresses protected. An active bit in the load mask byte masks (protects) the selected addresses. If more than eight bytes are used to load the Mask Register, wrap-around occurs (i.e. the ninth byte once again loads blocks 0:7). For the 2K byte block size option only four bytes are required to protect maximum memory, 64K. If more than four bytes are issued, bytes 4:7 load the Mask Register but are not used. The Protect Enable Command and Arm or Disarm Command may be issued simultaneously.

After setting up the Protect Controller, Bit-7 of the Program Status Word must be set to enable the protect function at the Processor.

7. INTERRUPTS

An interrupt can be used to signal the Processor that an attempt was made to Write into a protected area in memory. In the Arm state, interrupts are armed and enabled. In the Disarm state, interrupts are neither enabled not queued.

When an interrupt is acknowledged by an Acknowledge Interrupt instruction (AI or AIR) the interrupt is cleared and all status bits except PON are reset. The normal status returned by an Acknowledge Interrupt is X'20'.

8. INITIALIZATION

During power up, power down, or whenever the Initialize (INT) switch on the Display Panel is depressed, the Memory Protect Controller is placed in the Disarm state with all status conditions reset. The Load Mask Sequencer is initialized and the protect function is disabled at the controller.

9. DEVICE NUMBER

The Model 70 Memory Protect is normally assigned device address X'AE'. This address can be changed by the modification of straps on the controller. Refer to the Installation Specification 02-236A20, for details about the wiring alteration.

10. SAMPLE PROGRAM(S)

Not applicable to the Model 70 Memory Protect.

MODEL 70 MEMORY PROTECT PROGRAMMING SPECIFICATION

1. INTRODUCTION

The 02-236 Model 70 Memory Protect provides a means of allocating selected blocks of memory to be protected from user writing. The Memory Protect Controller (MPC) converts a Write operation to any location in a protected block to a Read operation, notifies the Processor via an interrupt, and sets a status bit in the controller. The memory may be partitioned into a maximum of 64 blocks with individual protect control for each block. Block sizes of 512 bytes, 1,024 bytes, or 2,048 bytes may be selected by strap options on the controller. Refer to Installation Specification 02-236A20, for block size strapping information. An overall protection override provides a means of disabling the protect function at the controller. Note that the protect function is enabled at the Processor only when Bit-7 of the current Program Status Word is set. When Bit-7 is reset, all Writes are treated the same as Privileged Writes (i.e. protect disabled).

2. CONFIGURATION

The Model 70 Memory Protect consists of one Memory Control mother-board and one cable. The cable interconnects the Memory Protect Controller with the Memory Control Board in the Central Processor Unit (CPU). The priority of the Memory Protect Controller on the Multiplexor Bus is determined by its installation in the systems chassis. Refer to 02-236A20 for installation information.

> NOTE
>
> It is imperative that the Memory Protect Controller have the highest priority on the Multiplexor Bus, to avoid ambiguity in identifying the source of a protect violation when executing interrupt routines with I/O interrupts enabled.

3. OPERATING PROCEDURES

The Model 70 Memory Protect is controlled by programmed I/O sequences using the Multiplexor Bus. See Sections 5 and 6.

4. DATA FORMAT

Refer to Appendix 1 for the definition of the Load Mask Bytes.

5. PROGRAMMING INSTRUCTIONS

The Output Command instruction (OC or OCR) causes a command byte, as defined in Table 1, to be sent to the controller. Any command causes all status except Protect On (PON) to be reset, and the Load Mask Sequencer to be initialized. The Sense Status instruction (SS or SSR) is used to read the status byte, as defined in Table 1, from the Memory Protect Controller. The status byte reflects the operational state of the controller. The least significant four bits (4:7) of the status byte are copied into the Condition Code of the current Program Status Word so they can be tested directly by the use of Branch instructions.

The Write Data (WD or WDR), Write Halfword (WH or WHR), or the Write Block (WB or WBR) instructions may be used to load the protect pattern into the controller.

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STATUS BYTE			PON	PWF		EX		
COMMAND BYTE	DISARM	ARM	PON	POFF				

STATUS

PON	Indicates that protect is enabled.
PWF	Indicates that an attempt was made to Write into a protected memory area. This bit is reset by an Output Command, or an Acknowledge Interrupt instruction.
EX	Examine is set when PWF is set.

COMMAND

DISARM	Disables interrupts. They will not be queued.
ARM	Enables interrupts.
PON	Enables the protect function at the controller.
POFF	Disables the protect function at the controller.

If an interrupt is pending, the Acknowledge Interrupt instruction (AI or AIR) clears the interrupt and causes the interrupting device address and status to be read into the Processor. Executing an Acknowledge Interrupt instruction when no interrupt is pending, results in a device address of zero and a status of X'04'.

6. PROGRAMMING SEQUENCE

The setting up of the Memory Protect Controller consists of loading the desired protect pattern into the controller, enabling the protect function, and either Arming or Disarming the interrupts. Any Output Command initializes the load sequencer in the controller so that the first byte to the protect module, following the Output Command, will load the Mask Register, Blocks 0:7. Refer to Appendix 1 for the correspondence between the load mask bytes, block size, and memory addresses protected. An active bit in the load mask byte masks (protects) the selected addresses. If more than eight bytes are used to load the Mask Register, wrap-around occurs (i.e. the ninth byte once again loads blocks 0:7). For the 2K byte block size option only four bytes are required to protect maximum memory, 64K. If more than four bytes are issued, bytes 4:7 load the Mask Register but are not used. The Protect Enable Command and Arm or Disarm Command may be issued simultaneously.

After setting up the Protect Controller, Bit-7 of the Program Status Word must be set to enable the protect function at the Processor.

7. INTERRUPTS

An interrupt can be used to signal the Processor that an attempt was made to Write into a protected area in memory. In the Arm state, interrupts are armed and enabled. In the Disarm state, interrupts are neither enabled not queued.

When an interrupt is acknowledged by an Acknowledge Interrupt instruction (AI or AIR) the interrupt is cleared and all status bits except PON are reset. The normal status returned by an Acknowledge Interrupt is X'20'.

8. INITIALIZATION

During power up, power down, or whenever the Initialize (INT) switch on the Display Panel is depressed, the Memory Protect Controller is placed in the Disarm state with all status conditions reset. The Load Mask Sequencer is initialized and the protect function is disabled at the controller.

9. DEVICE NUMBER

The Model 70 Memory Protect is normally assigned device address X'AE'. This address can be changed by the modification of straps on the controller. Refer to the Installation Specification 02-236A20, for details about the wiring alteration.

10. SAMPLE PROGRAM(S)

Not applicable to the Model 70 Memory Protect.

APPENDIX 1

TABLE OF MEMORY ADDRESSES VS. BLOCKS

BLOCK	LOAD MASK DATA		MEMORY ADDRESSES (HEX)		
	BYTE	BIT	.5K BYTE	1K BYTE	2K BYTE
1	0	0	0000-01FF	0000-03FF	0000-07FF
2	0	1	0200-03FF	0400-07FF	0800-0FFF
3	0	2	0400-05FF	0800-0BFF	1000-17FF
4	0	3	0600-07FF	0C00-0FFF	1800-1FFF
5	0	4	0800-09FF	1000-13FF	2000-27FF
6	0	5	0A00-0BFF	1400-17FF	2800-2FFF
7	0	6	0C00-0DFF	1800-1BFF	3000-37FF
8	0	7	0E00-0FFF	1C00-1FFF	3800-3FFF
9	1	0	1000-11FF	2000-23FF	4000-47FF
10	1	1	1200-13FF	2400-27FF	4800-4FFF
11	1	2	1400-15FF	2800-2BFF	5000-57FF
12	1	3	1600-17FF	2C00-2FFF	5800-5FFF
13	1	4	1800-19FF	3000-33FF	6000-67FF
14	1	5	1A00-1BFF	3400-37FF	6800-6FFF
15	1	6	1C00-1DFF	3800-3BFF	7000-77FF
16	1	7	1E00-1FFF	3C00-3FFF	7800-7FFF
17	2	0	2000-21FF	4000-43FF	8000-87FF
18	2	1	2200-23FF	4400-47FF	8800-8FFF
19	2	2	2400-25FF	4800-4BFF	9000-97FF
20	2	3	2600-27FF	4C00-4FFF	9800-9FFF
21	2	4	2800-29FF	5000-53FF	A000-A7FF
22	2	5	2A00-2BFF	5400-57FF	A800-AFFF
23	2	6	2C00-2DFF	5800-5BFF	B000-B7FF
24	2	7	2E00-2FFF	5C00-5FFF	B800-BFFF
25	3	0	3000-31FF	6000-63FF	C000-C7FF
26	3	1	3200-33FF	6400-67FF	C800-CFFF
27	3	2	3400-35FF	6800-6BFF	D000-D7FF
28	3	3	3600-37FF	6C00-6FFF	D800-DFFF
29	3	4	3800-39FF	7000-73FF	E000-E7FF
30	3	5	3A00-3BFF	7400-77FF	E800-EFFF
31	3	6	3C00-3DFF	7800-7BFF	F000-F7FF
32	3	7	3E00-3FFF	7C00-7FFF	F800-FFFF
33	4	0	*	8000-83FF	
34	4	1		8400-87FF	
35	4	2		8800-8BFF	
36	4	3		8C00-8FFF	
37	4	4		9000-93FF	
38	4	5		9400-97FF	
39	4	6		9800-9BFF	
40	4	7		9C00-9FFF	N/A
41	5	0		A000-A3FF	
42	5	1		A400-A7FF	
43	5	2		A800-ABFF	
44	5	3		AC00-AFFF	
45	5	4		B000-B3FF	
46	5	5		B400-B7FF	
47	5	6		B800-BBFF	
48	5	7		BC00-BFFF	

* If more than 32K Bytes of memory exists, and the 512 Byte Block option is used, the pattern defined for the first 32K repeats itself for the second 32K.

APPENDIX 1
TABLE OF MEMORY ADDRESSES VS. BLOCKS (Continued)

BLOCK	LOAD MASK DATA		MEMORY ADDRESSES (HEX)		
	BYTE	BIT	.5K BYTE	1K BYTE	2K BYTE
49	6	0		C000-C3FF	N/A
50	6	1		C400-C7FF	
51	6	2		C800-CBFF	
52	6	3		CC00-CFFF	
53	6	4		D000-D3FF	
54	6	5		D400-D7FF	
55	6	6		D800-DBFF	
56	6	7		DC00-DFFF	
57	7	0		E000-E3FF	
58	7	1		E400-E7FF	
59	7	2		E800-EBFF	
60	7	3		EC00-EFFF	
61	7	4		F000-F3FF	
62	7	5		F400-F7FF	
63	7	6		F800-FBFF	
64	7	7		FC00-FFFF	

Publication Number 29-267R01

MULTIPLEXOR BUS BUFFER INSTRUCTION MANUAL

Consists of:

Installation and Maintenance Specification	02-239A21
Schematic	02-239R01D08

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January 1972

MULTIPLEXOR BUS BUFFER INSTALLATION AND MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-239 Multiplexor Bus Buffer (MBB) is a Processor option which regenerates the Multiplexor Bus (MB) providing a drive capability for up to 16 additional device controllers on the buffered Multiplexor Bus. The MBB itself presents one standard load to the unbuffered bus. The MBB is complete on one standard 15 inch circuit board. The unbuffered bus input is received on the MBB Zero (0) level connector. The regenerated (buffered) bus output appears on the MBB One (1) level connector. The MBB buffers all lines in the Multiplexor Bus except the three lines uniquely associated with the Interleaved Data Channel (i.e. DC, DCR, and RDACK).

2. INSTALLATION

See Figure 1. The MBB is installed in any even numbered card slot (i.e. 0, 2, 4, or 6) of a 15 inch expansion chassis. At the time of installation it is necessary to cut the Multiplexor Bus wiring between the even numbered slot accepting the MBB and the next higher numbered slot on the One (1) level connector only. The RACK0/TACK0 daisy chain wiring on the back panel is rerouted according to Figure 1. The lower numbered card slots in the chassis become buffered on the One (1) level connector only.

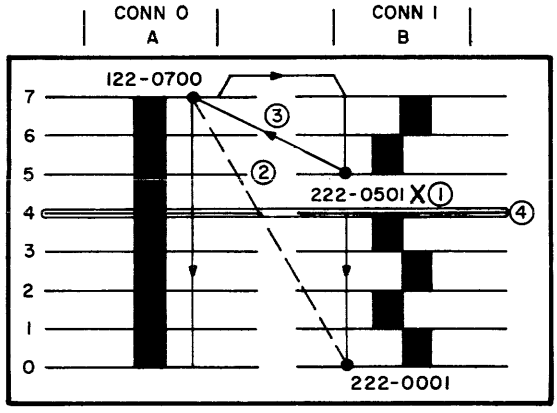
For the convenience of cutting the Multiplexor Bus, the connections between every other slot are made using "top" wire wraps. This allows the cutting of the bus by simply lifting the top wraps when the MBB in installed in an even numbered slot. Refer to Figure 1 during the following example.

To install a MBB in Slot 4:

1. Remove all wires on Connector One (1), between Slots 4 and 5, on Pins 11 through 26, Rows 1 and 2. (See backpanel map in 02-239D08, Sheet 2.)
2. Remove the wire between 222-0001 and 122-0700.

   Remove the RACK0/TACK0 jumper between Pins 122 and 222 on both the Zero (0) and One (1) level connectors.
3. Connect 122-0700 to 222-0501.
4. Install the MBB into Slot 4 of the chassis.

The buffered Multiplexor Bus now appears on the Connector One (1) side of Slots 4, 3, 2, 1, and 0. All other connectors in the chassis receive the unbuffered bus. To install a MBB in any other even numbered slot a similar procedure is followed.



NOTE: THE CIRCLED NUMBERS ON THE FIGURE REFER TO THE STEPS IN THE INSTALLATION SEQUENCE.

Figure 1. Rear (Wiring) View, 15 Inch Expansion Chassis

The cabling necessary for the MBB depends on the system's physical configuration. In cases where the buffered bus does not extend outside the chassis, no cabling is required. When the buffered bus extends to another chassis, a number of cables can be used. See Figure 2 for a summary of all cables. Refer also to Chapter 8, Model 70 User's Manual, Publication Number 29-261, for further details on system configurations.

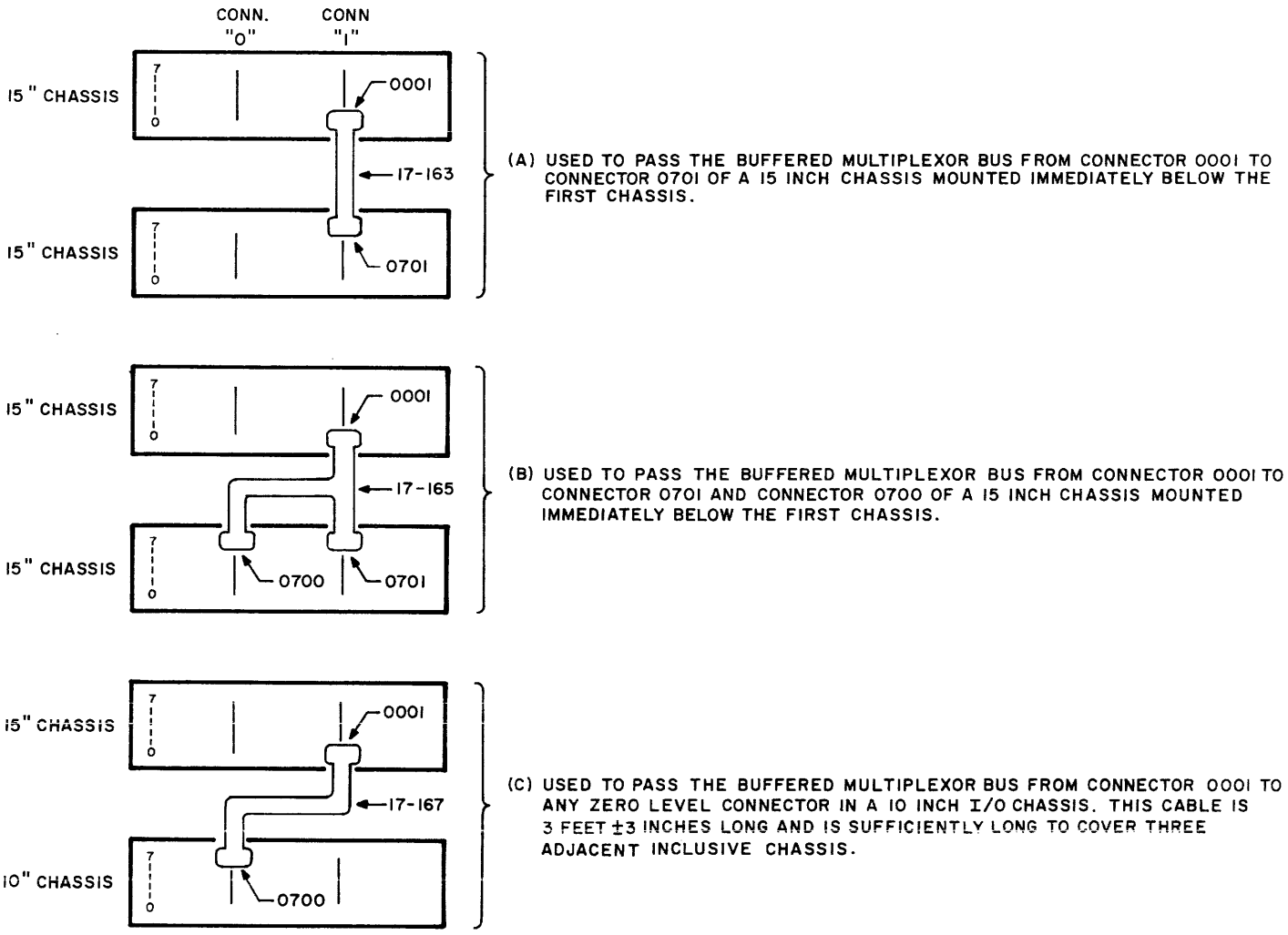


Figure 2. MBB Extended Configurations and Associated Cables

3. MULTIPLEXOR BUS BUFFER MAINTENANCE

3.1 MBB Block Diagram Analysis

Refer to Figure 3. The MBB provides the buffering necessary to regenerate the MB between the unbuffered MB and the buffered Multiplexor Bus which can drive up to 16 device controllers.

The MBB operates on the following 27 lines:

16 - bidirectional Data Lines (D000:150)

6 - unidirectional Control Lines (ADRS, CMD, DA, CL070, SR and DR)

3 - unidirectional Test Lines (HW, ATN and SYN)

1 - unidirectional Initialize Line (SCLR)

1 - daisy chain acknowledge Control Line (RACK/TACK)

NOTE

The MBB does not regenerate any of the MB lines uniquely associated with the Interleaved Data Channel (i.e. DC, DCR, and RDACK).

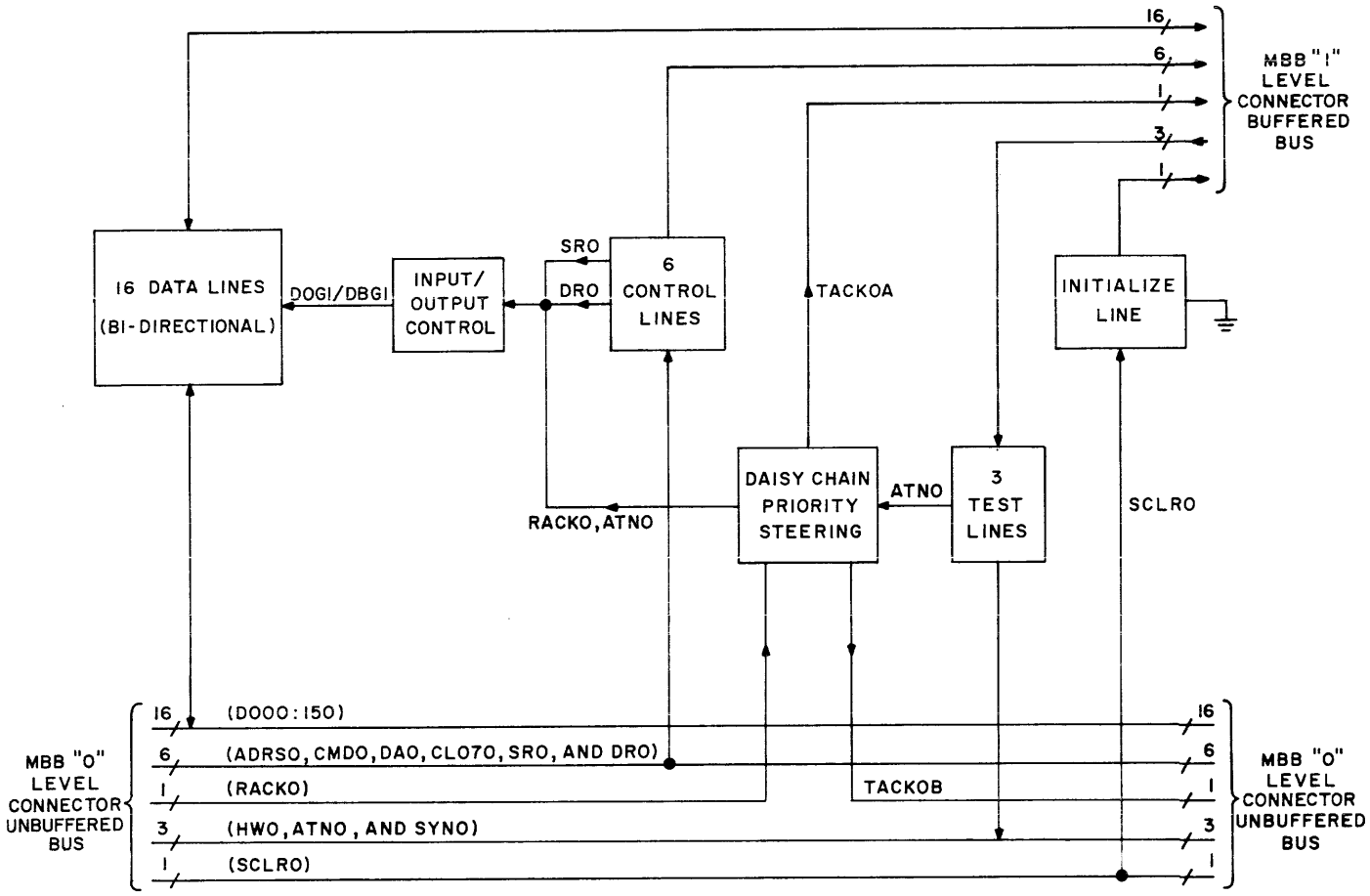


Figure 3. Multiplexor Bus Buffer, Block Diagram

3.2 Operation

All buses are the false type, i.e. low level active, high level inactive. The unbuffered MB connects to the MBB on the Zero (0) level connector. The buffered MB appears on the One (1) level connector on the MBB. Refer to Schematic 02-233D08, Sheets 1 and 2.

3.3 Functional Description

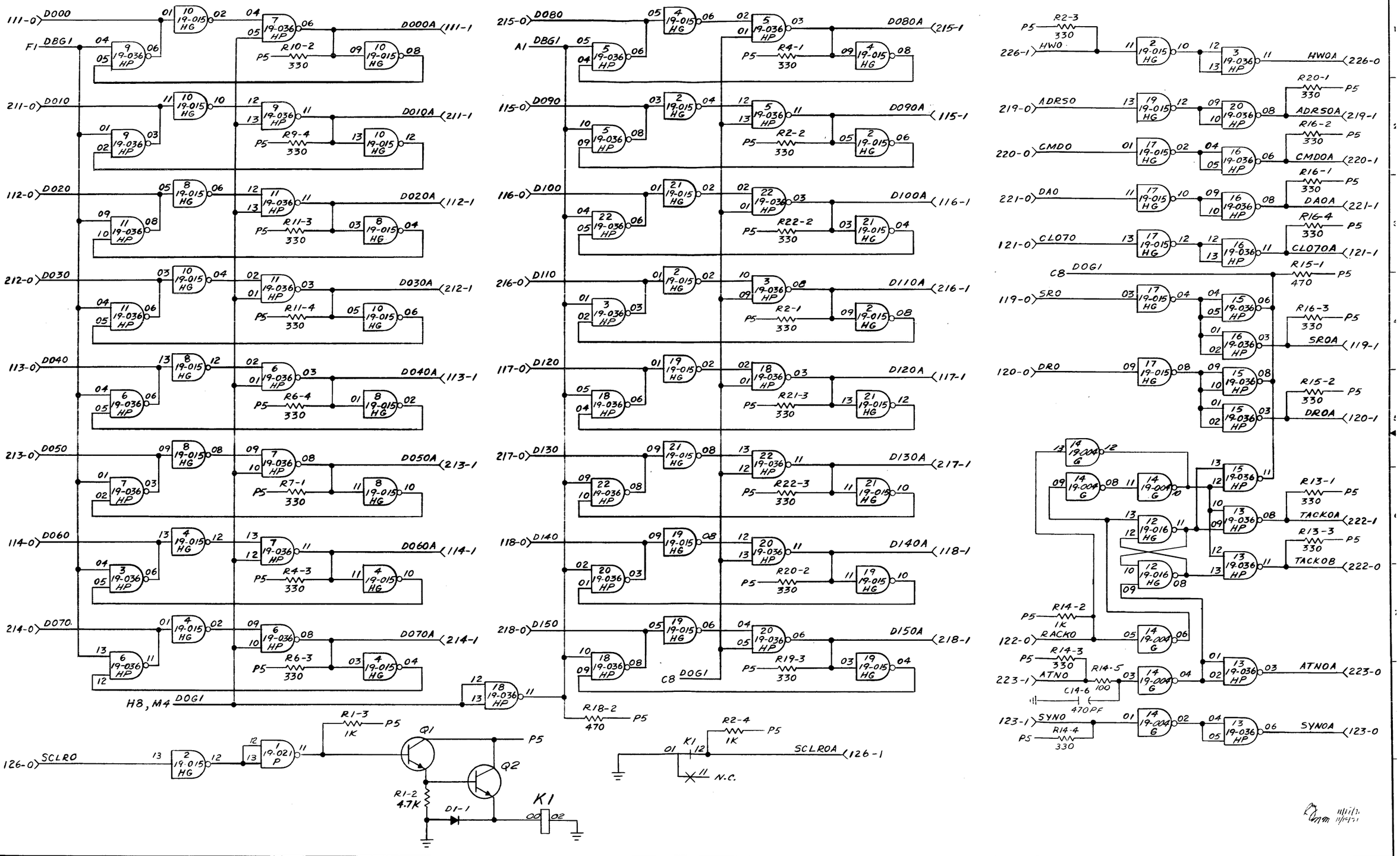
The operation of the Multiplexor I/O System is the same regardless of whether or not a MBB is used in the system. Referring to Schematic 02-239D08, observe that the 16 bidirectional Data Lines (D000:150) connect the unbuffered Multiplexor Bus on Connector Zero (0) to the buffered Multiplexor Bus on Connector One (1). The direction data passes between the two busses is defined by the two lines DOG1 and DBG1 which are inverse functions. With all Multiplexor Bus Control Lines inactive, or when any of the following control lines ADRS0, CMD0, DA0, or CL070 are active the DOG1 line is high and data flows from Connector Zero (0) to Connector One (1). With either of the Multiplexor Control Lines SR0 or DR0 active, or RACK0 active with a low on ATN0 at Pin 223-1, the DBG1 line is high and data flows from Connector One (1) to Connector Zero (0).

Note that the daisy chain contention circuit can pass RACK0/TACK0 to either the unbuffered bus (222-0, TACK0B) if the ATN signal from the buffered bus is not active, or it can pass RACK0/TACK0 to the buffered bus (222-1, TACK0A) if the ATN signal from the buffered bus is active. Note also that the Multiplexor Bus Control Lines ADRS, CMD0, DA0, CL070, SR0, and DR0 are mutually exclusive only one or none being active at a time.

4. MNEMONICS LIST

This section provides an alphabetical list of the mnemonics used in the Multiplexor Bus Buffer (MBB). A brief description of each mnemonic and a reference to its source on Schematic 02-239D08, is also provided.

MNEMONIC	MEANING	LOCATION
ADRS	Address Control Line, the Processor presents an Address Byte on Data Lines D080:150, the device controller accepts the Address Byte and responds with a SYN.	1M2, 1S2
ATN	Attention Test Line, any device controller desiring to interrupt the Processor will activate the ATN line in its MBB and hold this line until an acknowledge signal is received from the Processor.	1M8, 1S8
CL070	Power Fail Control Line, this control line is activated by the Processor when a Power Fail condition is detected by the Processor, if the Power Fail option is equipped. This line is held active until the SCLR0 signal occurs.	1M3
D000:150	The 16 bidirectional data lines used to transfer one 8-bit byte or one 16-bit halfword of data between the Processor and the device controllers.	1A1-8, 1E1-8 1F1-8, 1L1-8
DA	Data Available Control Line, the Processor presents data on Data Lines D000:150 for transfer to the device controller. The device controller accepts the low byte or the entire halfword and responds with a SYN.	1M3
DBG1	Enables data transfer from the device controller. A high DBG1 ANDed with the data output from the device controller, gates data (8-bit byte or 16-bit halfword) to the MB.	1F1
DOG1	Enables data transfer to the device controller. A high DOG1, ANDed with the data output from the MB, gates data (8-bit byte or 16-bit halfword) to the device controllers.	1M4
DR	Data Request Control Line, the device controller presents data to Data Lines D080:150, followed by a SYN. If a Halfword (HW) is present, the HW test line is also active.	1M5
HW	Halfword Test Line, the HW line is activated by a halfword oriented device controller whenever it is communicating with the Processor.	1M1
RACK	Receive Acknowledge Control Line, this control line is activated by the Processor in response to an interrupt.	1M7
SCLR	System Clear (Initialize) Control Line, this is a metallic contact to ground that occurs during Power Fail, Power Up, or Initialize.	1A9, 1K9
SR	Status Request Control Line, the device controller must present status to Data Lines D080:150, followed by a SYN.	1M4
SYN	Synchronize Test Line, this signal is generated by the device controller to inform the Processor that it has properly responded.	1M8, 1S8
TACK0A	Transmit Acknowledge Control Line. This is the MBB daisy chain control line to its associated device controllers.	1S6
TACK0B	Transmit Acknowledge Control Line. This is the MB daisy chain control line to the I/O System.	1S7



NOTES

REVISIONS

LOC M8 ADDED 100Ω RES & 470PF CAP

BG	DJF			1-21-72	R01

NAME	TITLE	DATE
L. VALENTY	DRAFT	8-10-71
G. J. HOMEFIELD	CHK	9-8-71
R. E. JONES	ENGR	
D. W. YOUNG	SYS TST	
R. E. JONES	DIR ENG	

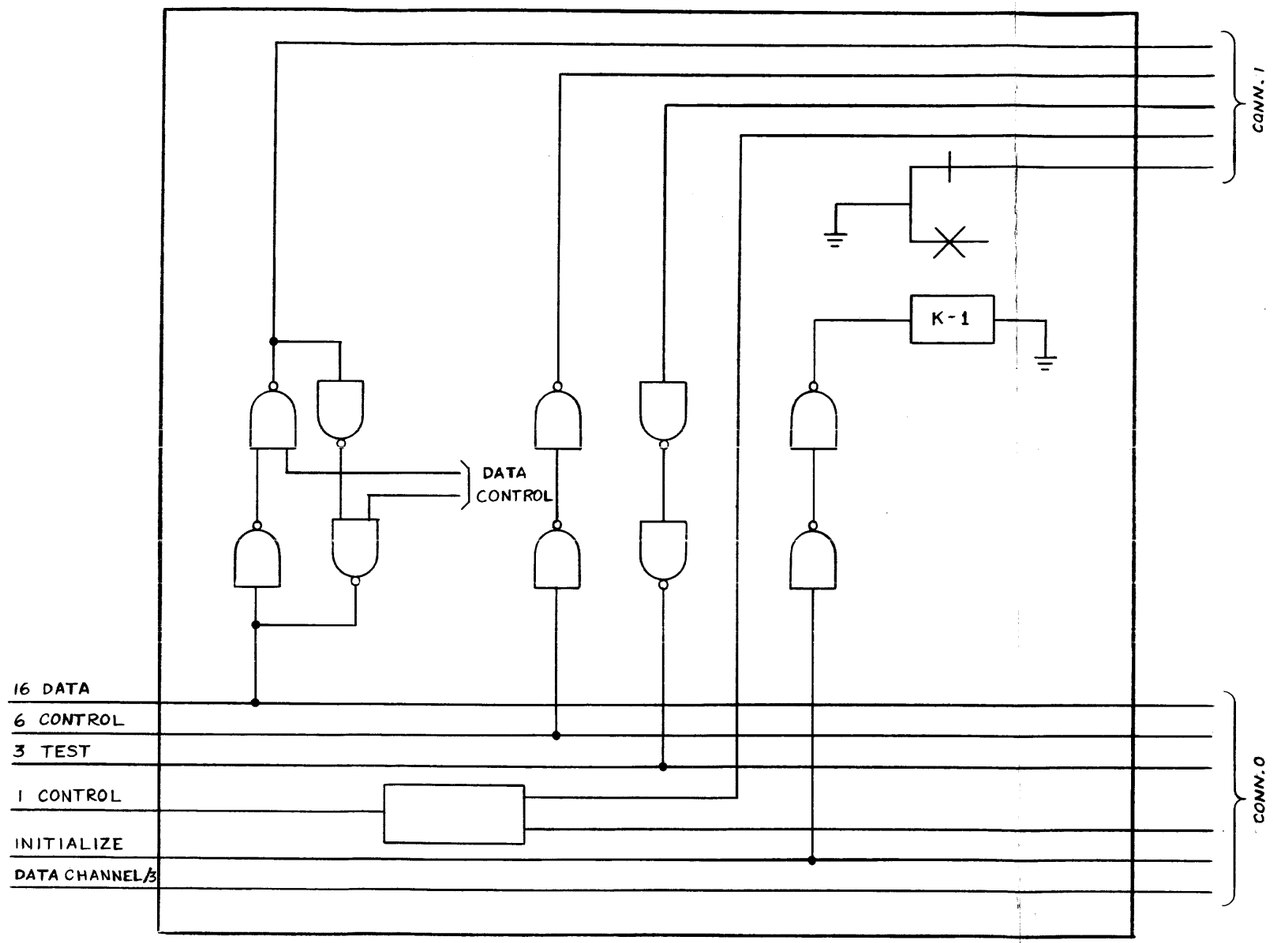
TITLE: FUNCTIONAL SCHEMATIC NS-BUS BUFFER

TASK NO. 03117

DWG NO. 02-239 R01D08

SHEET 1 OF 2

BRUNING 44231 15043



BLOCK DIAGRAM — NS BUS BUFFER

CONN POS	I/O SLOT	
MOTH. BD.	NS-BUS BUFFER	
VERT. POS.	HORIZON. POS.	
	1	2
41	P5	GND
40	GND	GND
39	P15	REQO
38	N15	ENO
37	ACTO	TACO
36		
35		
34	RACKO	
33	MA130	MA140
32	MA110	MA120
31	MA090	MA100
30	MA070	MA080
29	MA050	MA060
28	RDACKO	TDACKO
27	DCO	DCRO
26	SCLRO	HWOA
25		
24		
23	SYNOA	ATNOA
22	RACKO	TACKOB
21	CLO7O	DAO
20	DRO	CMDO
19	SRO	ADRSO
18	D140	D150
17	D120	D130
16	D100	D110
15	D080	D090
14	D060	D070
13	D040	D050
12	D020	D030
11	D000	D010
10	MA030	MA040
09	MA020	MA021
08	MA01	MA02
07	MA010	MA011
06	MA000	MA001
05	PARO	MA00
04	INHO	ERO
03	WO	LRO
02	P15	N15
01	GND	GND
00	P5	GND

0

CONN POS	I/O SLOT	
MOTH. BD.	NS-BUS BUFFER	
VERT. POS.	HORIZON. POS.	
	1	2
41	P5	GND
40	GND	GND
39	P15	P15
38	N15	N15
37	MD150	MD160
36	MD130	MD140
35	MD110	MD120
34	MD090	MD100
33	MD070	MD080
32	MD050	MD060
31	MD030	MD040
30	MD010	MD020
29	EXVT	MD000
28	TEMPA	VT
27	WRTO	TEMPB
26	SCLROA	HWO
25		
24		
23	SYNO	ATNO
22	RACKOA	TACKOA
21	CLO7OA	DAOA
20	DROA	CMDOA
19	SROA	ADRSOA
18	D140A	D150A
17	D120A	D130A
16	D100A	D110A
15	D080A	D090A
14	D060A	D070A
13	D040A	D050A
12	D020A	D030A
11	D000A	D010A
10		MS000
09	MS010	MS020
08	MS030	MS040
07	MS050	MS060
06	MS070	MS080
05	MS090	MS100
04	MS110	MS120
03	MS130	MS140
02	MS150	MS160
01	GND	GND
00	P5	GND

1

NOTES

NAME	TITLE	DATE
L.VALENTY	DRAFT	8-11-71
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TITLE: FUNCTIONAL SCHEMATIC NS-BUS BUFFER

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EXPANSION CHASSIS INSTALLATION AND INTERCONNECTION INSTRUCTIONS

Consists of:	Installation and Interconnection Instructions	29-118A12
	48KB Expansion Chassis Installation Specification	02-221A20
	Installation Drawing	3-109R02B20 (Sheets 2 and 3)
	Wiring Diagram	17-039R01B06

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July 1971

EXPANSION CHASSIS INSTALLATION AND INTERCONNECTION INSTRUCTIONS

1. INTRODUCTION

Four standard expansion chassis are available for use in INTERDATA Digital Systems. Each expansion chassis is wired to accept some combination of standard INTERDATA core memory modules and standard INTERDATA peripheral device controller cards as follows:

Sales Number	Part Number	Description
7-990	12-001F03	Will accept up to 8K Bytes of core memory (one module) plus 10 wire wrapped or 10 printed I/O controller cards.
7-991	12-001F04	Will accept 24K Bytes of core memory (three modules) plus 5 wire wrapped or 5 printed I/O controller cards.
7-992	12-001F08	Will accept 40K Bytes of core memory (five modules) only.
7-993	12-001F10	Will accept 13 wire wrapped or 13 printed I/O controller cards only.

The I/O section of each expansion chassis is wired according to the standard wiring pattern described in the Systems Interface Manual, 29-003. The memory section of each expansion chassis is wired in the same manner as the memory section in the Processor's chassis. The expansion chassis is connected to other chassis in the system via standard cables which are supplied with the expansion chassis.

2. DIMENSIONS

All INTERDATA chassis have RETMA Standard dimensions as indicated in Figure 1.

3. INSTALLATION, MECHANICAL

All INTERDATA chassis can be installed in any standard 19 inch rack. (Up to five chassis fit in the INTERDATA Systems Cabinet, Sales Number 7-989.) Chassis interconnect cables, supplied with each expansion chassis, require that all chassis are mounted immediately above or immediately below other chassis in the system. Any other installation may require special cabling and is subject to special bidding.

Table 1 identifies the kinds of circuit boards which may be installed in the 26 locations of the expansion chassis. The four board sets (MCD, ME1, ME0, and MSW) correspond to one standard 4K Byte or 8K Byte memory module. The wiring pattern between these boards is identical to that between the corresponding boards in the basic Processor's chassis.

The slots designated I/O accept any set of standard I/O controller boards (either double spaced boards or printed copper boards) or any other board designed specifically to be installed in a standard I/O controller slot.

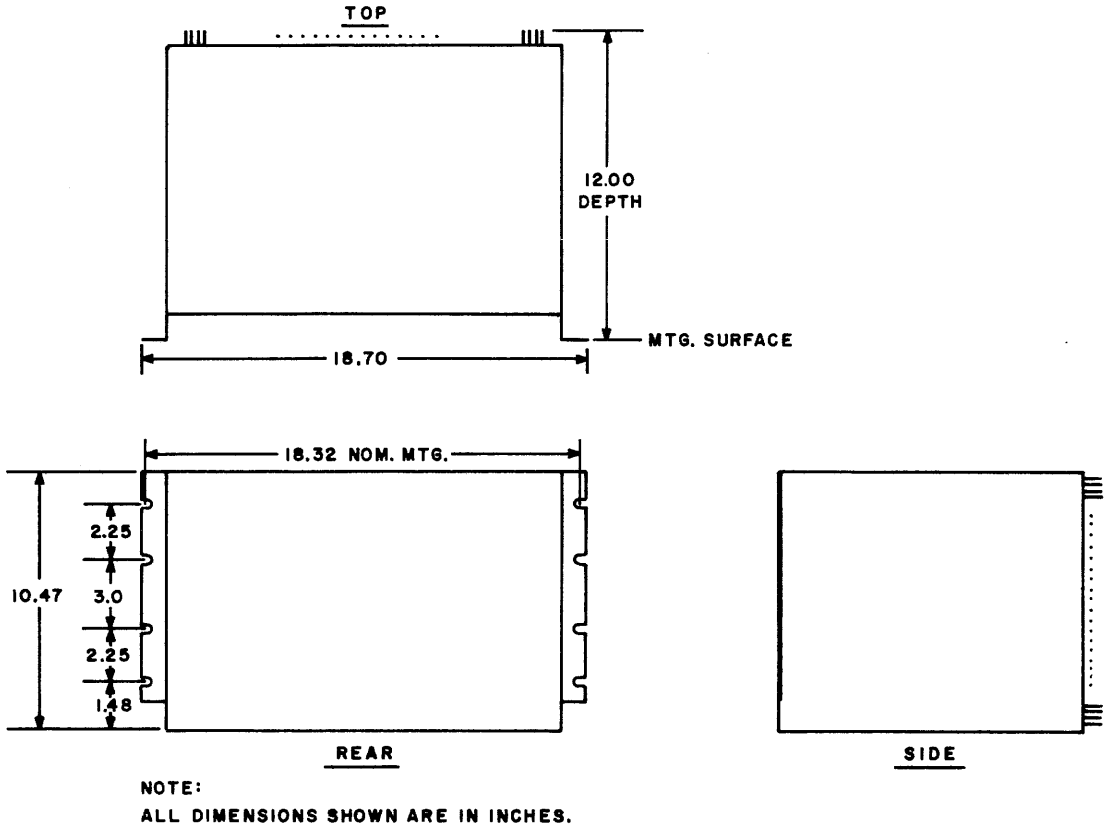


Figure 1. Dimensions

The wiring pattern between I/O slots is defined in the Systems Interface Manual, 29-003. Note, for certain controllers, the I/O section of expansion back panels requires removal of some wires. Refer to 29-003 or to the installation instructions for each specific device controller for details.

Once the cards are inserted, install the retaining bar to assure reliable contact between the connectors and mother-boards.

Six FAST-ON tabs are provided across the top and bottom at the rear of the back panel. Six ground jumpers, Part Number 17-076, are provided with each chassis to jumper between corresponding tabs on adjacent chassis.

4. INSTALLATION, ELECTRICAL

4.1 Power

A standard INTERDATA power supply can normally drive two fully loaded chassis (the basic Processor's chassis plus one expansion chassis.) Each additional expansion chassis, or pair of expansion chassis', requires an additional power supply, Sales Number 7-985. (Exception: 7-992 requires in most cases, a dedicated power supply.)

The 17-039 cable is used for connecting the power supplies to the Digital System Chassis. As supplied, the cable is used to connect one supply to one chassis. To connect one supply to two chassis, simply remove the shrink tubing from the second set of connectors and make the additional connections on the second chassis.

NOTE

The dimensions of the cable requires that the power supply be installed immediately above, immediately below, or behind one of the two chassis.

TABLE 1. PERMISSIBLE LOCATIONS

Location	7-990	7-991	7-992	7-993
0	HSMBC	HSMBC	HSMBC	----
1	-------	-------	MCD	I/O
2	MCD	MCD	MEM1	----
3	MEM1	MEM1	MEM0	I/O
4	MEM0	MEM0	-------	----
5	-------	-------	MSW	I/O
6	MSW	MSW	MCD	----
7	I/O	MCD	MEM1	I/O
8	-------	MEM1	MEM0	----
9	I/O	MEM0	-------	I/O
10	-------	-------	MSW	----
11	I/O	MSW	MCD	I/O
12	-------	MCD	1	----
13	I/O	MEM1	0	I/O
14	-------	MEM0	-	----
15	I/O	-------	MSW	I/O
16	-------	MSW	MCD	----
17	I/O	I/O	1	I/O
18	-------	-------	0	----
19	I/O	I/O	-	I/O
20	-------	-------	MSW	----
21	I/O	I/O	MCD	I/O
22	-------	-------	MEM1	----
23	I/O	I/O	MEM0	I/O
24	-------	-------	-------	----
25	I/O	I/O	MSW	I/O

The bracketed groups correspond to one standard INTERDATA memory module, either 4K or 8K Bytes.

The bulk of the power cable connections are made to the terminal block on the basic Processor's chassis. See Section 4.3.3.

When a second power supply is required, a second 17-039 power cable is supplied with it. This power cable is connected similarly to the first. Also cable 17-074 is installed between terminal blocks to control power on/off from the main power control switch on the Processor's control panel. See Section 4.3.3.

4.2 General Rules

1. Memory modules must be located within three adjacent chassis.
2. The first memory module in an expansion chassis must be located in the lowest numbered slots that are available for memory.
3. The 1K resistor between pins 7 and 8 on the TB is removed when a memory module is installed.

4.3 Chassis Interconnect Cable

Expansion chassis are interconnected to other chassis in the digital system via some combination of cables which slip onto the wire wrap pins on the back panel. Three classes of interconnections are required.

1. Memory module interconnections.
2. Multiplexor Bus Interconnections.
3. Power and power control interconnections.

4.3.1 Memory. Memory modules must be located in no more than three adjacent system chassis. Systems configured with three chassis which can contain memory (the Processor qualifies as one of these) will be provided with two each 17-015 cables. These are installed on connector 000 and 0001 of the three chassis (rows 1 and 2). Systems configured with two chassis which can contain memory modules will be provided with two each 17-012 cables. These also are installed between connector 0000 and 0001 (rows 1 and 2) of the two chassis. See Figure 2.

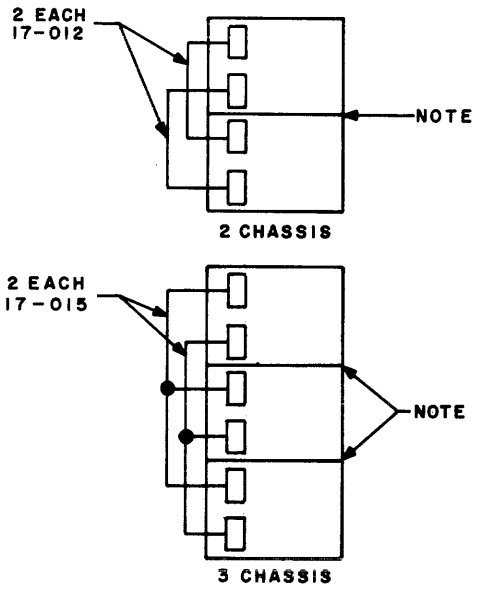


Figure 2. Memory Interconnections

4.3.2 Multiplexor Bus. The multiplexor bus is extended to expansion chassis via a single 17-014F01 (20 inch) or a single 17-014F02 (30 inch) cable, identical except for length. This cable is installed from the highest numbered I/O slot in the first chassis to the lowest numbered I/O slot in the expansion chassis. (The cable connects to the bottom connector, columns 1 and 2 of each slot. The corresponding top connector is not connected to the expansion chassis).

The first expansion chassis is provided with one each 17-014F01. The second expansion chassis is provided with one each 17-014F02. All additional expansion chassis are supplied with one each 17-014F01. This permits cabling as indicated in Figure 3. In this case, I/O controllers in the Processor are highest in priority, followed by those in Card File 4, followed by Card File 2, followed by Card File 1.

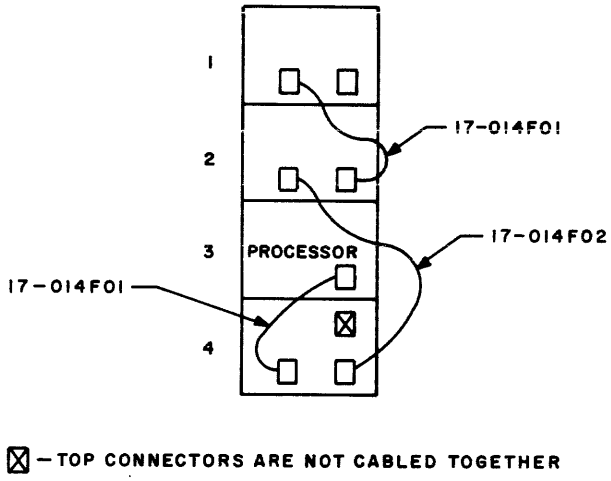


Figure 3. Multiplexor Bus Interconnections

Certain controllers that locate in I/O slots (i.e., SELCH) provide additional cables for extending the I/O bus. Refer to the Installation Specification for SELCH and to 29-003.

Also, all multicard I/O controllers, that is all products which require more than one mother-board and which are designed to plug into I/O slots, must be installed in adjacent slots of the same chassis.

4.3.3 Power. In general, one standard INTERDATA power supply is sufficient to drive two system chassis (i.e., the basic Processor plus one expansion chassis or two expansion chassis). If more than two chassis are included in a system, at least two power supplies are required; if more than four chassis are involved, at least three supplies, etc. Each power supply in the system is equipped with one 17-039. (A supply common to two chassis requires that those chassis be mounted adjacent to each other.) The power cable connects to the power bus strips on both systems chassis and to the terminal block on one chassis designated here as Chassis A. If one of the two chassis is a Processor, it must be Chassis A. Or if one chassis in a pair contains memory and the other does not, it must be Chassis A. Otherwise, there are no restrictions.

The 17-039 cable is installed as indicated in Drawings 3-109R01B12 and 17-039B06. (The cable lugs are marked as indicated.)

When more than one power supply is involved in a system, cable 17-074 is connected between pins 3, 4, and 5 of the terminal block A. This permits common power on/off control from the power switch on the Processor's control panel.

02-221 48 KB EXPANSION CHASSIS INSTALLATION SPECIFICATION

1. INTRODUCTION

The 48KB Expansion Chassis is designed for use with 02-205 Series 1 Memory Modules only. It is wired to accept up to six (6) 02 205 Series 1 Memory Modules (consisting of four boards each), with or without parity. See Figure 1 for slot assignments.

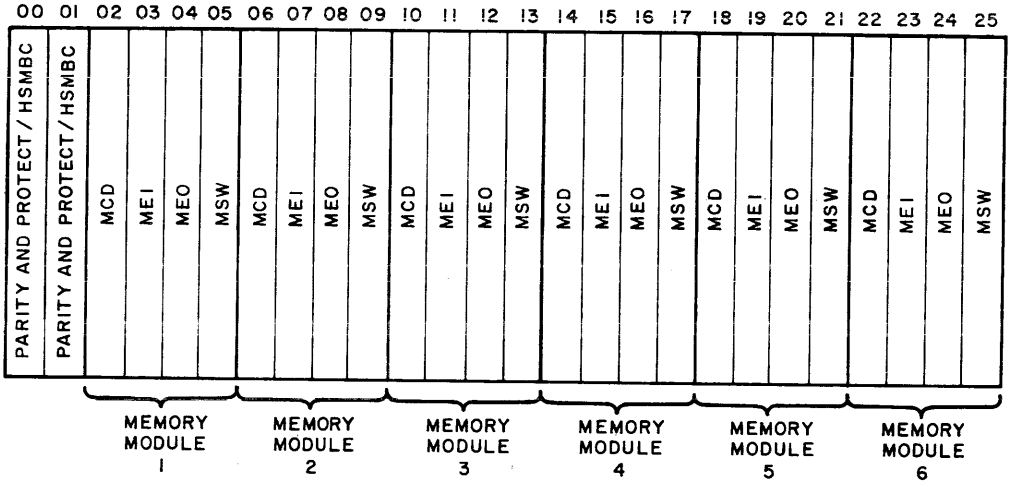


Figure 1. Slot Assignments

2. DIMENSIONS

The 48KB Expansion Chassis has standard RETMA dimensions as indicated in Figure 2.

3. INSTALLATION, MECHANICAL

An INTERDATA System Cabinet, Sales Number 7-989, can have as many as five chassis. However, the chassis interconnect cables (17-012), supplied with each 48KB Expansion Chassis, require that the 48KB Expansion Chassis be mounted either immediately above, or immediately below the CPU chassis.

Figure 1 identifies the slot assignments for the Memory Module Boards that may be installed in the twenty-six slots of the 48KB Expansion Chassis. Each Memory Module consists of four boards, (MCD, ME1, ME0, and MSW). The 48KB Expansion Chassis is expandable from one to a maximum of six Memory Modules.

Once the boards are inserted and properly seated in the chassis, the retaining bar, 11-024, is installed to assure that contact is made between the back panel connectors and the mother-boards.

Six Fast-On tabs are provided across the top and bottom at the rear of the back panel. Six ground jumpers are provided between the corresponding Fast-On tabs on adjacent chassis.

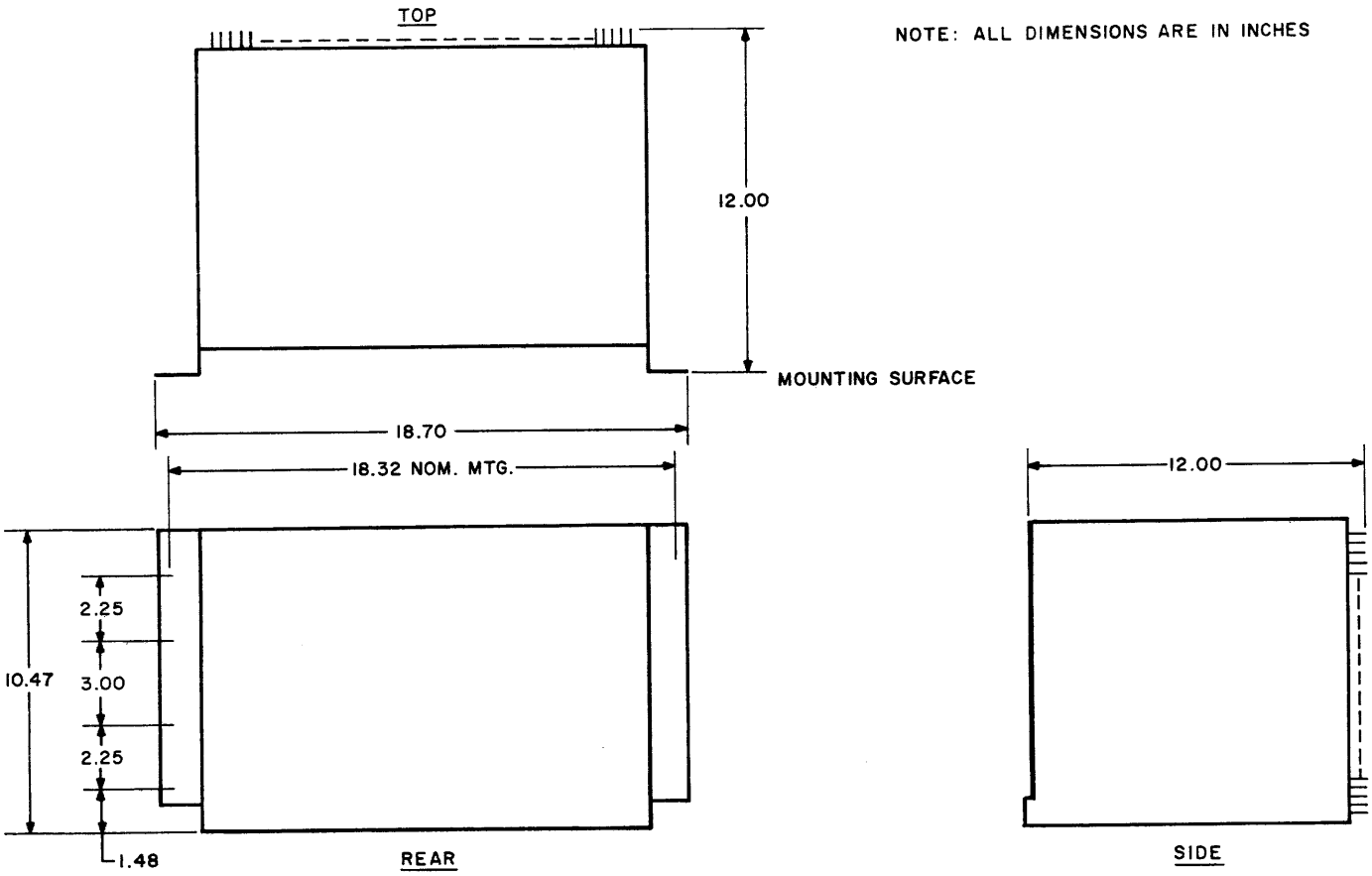


Figure 2. 48KB Expansion Chassis Dimensions

4. INSTALLATION, ELECTRICAL

4.1 Power

The 02-221 48KB Expansion Chassis power requirements are such that a separate 34-007 Power Supply is required for each chassis. Therefore, each 48KB Expansion Chassis is supplied with a 34-007 Power Supply. See Figure 3 for the interconnection between the 34-007 Power Supply and the 02-221 48KB Expansion Chassis.

Interconnect the 34-007 Power Supply and 48KB Expansion Chassis (Back Panel) as indicated by the terminal board and pin number marked on the two protective sleeves of each wire in the 17-039 cable. For example, a wire with one end marked 26-5 connects to Terminal Board 26, Pin 5, on the 48KB Expansion Chassis Back Panel, and the other end, marked 1-6, connects to Terminal Board 1, Pin 6, of the 34-007 Power Supply. Refer to 34-007 Power System Instruction Manual, Publication Number 29-157 for further information.

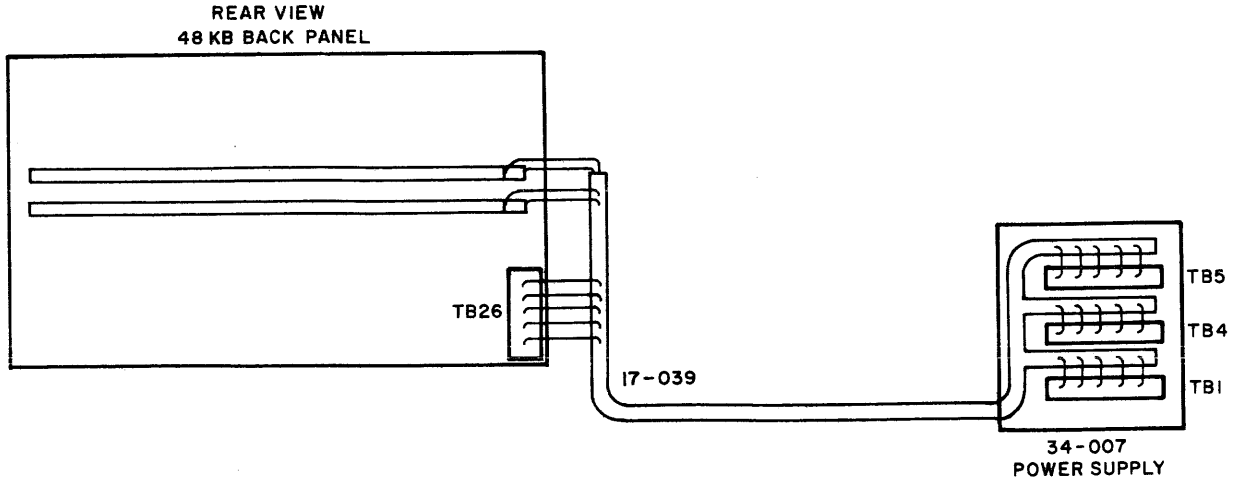


Figure 3. Power Supply/48KB Expansion Chassis Interconnection

4.2 Chassis Interconnect Cables

The 48KB Expansion Chassis is interconnected to the CPU via two cables, Part Number 17-012, which slip onto the wire wrap pins on the back panel. They are installed on connectors 0000 and 0001, Rows 1 and 2 of each chassis. See Figure 4.

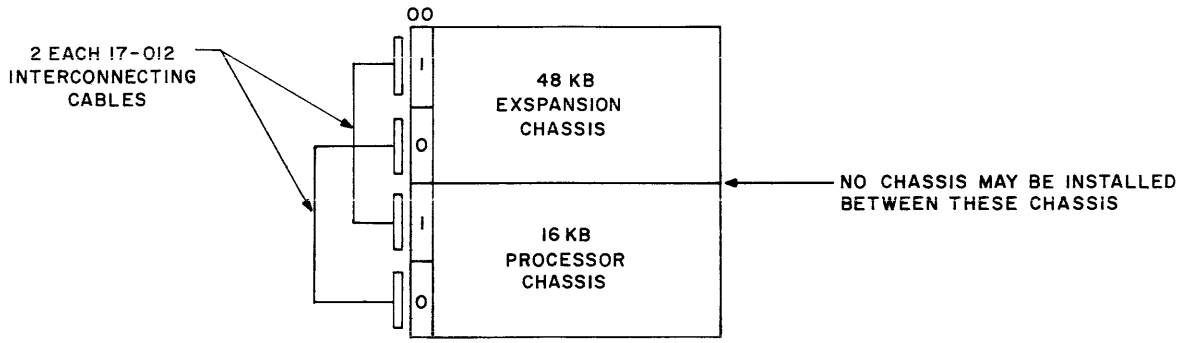


Figure 4. 48KB Expansion Chassis Memory Interconnections

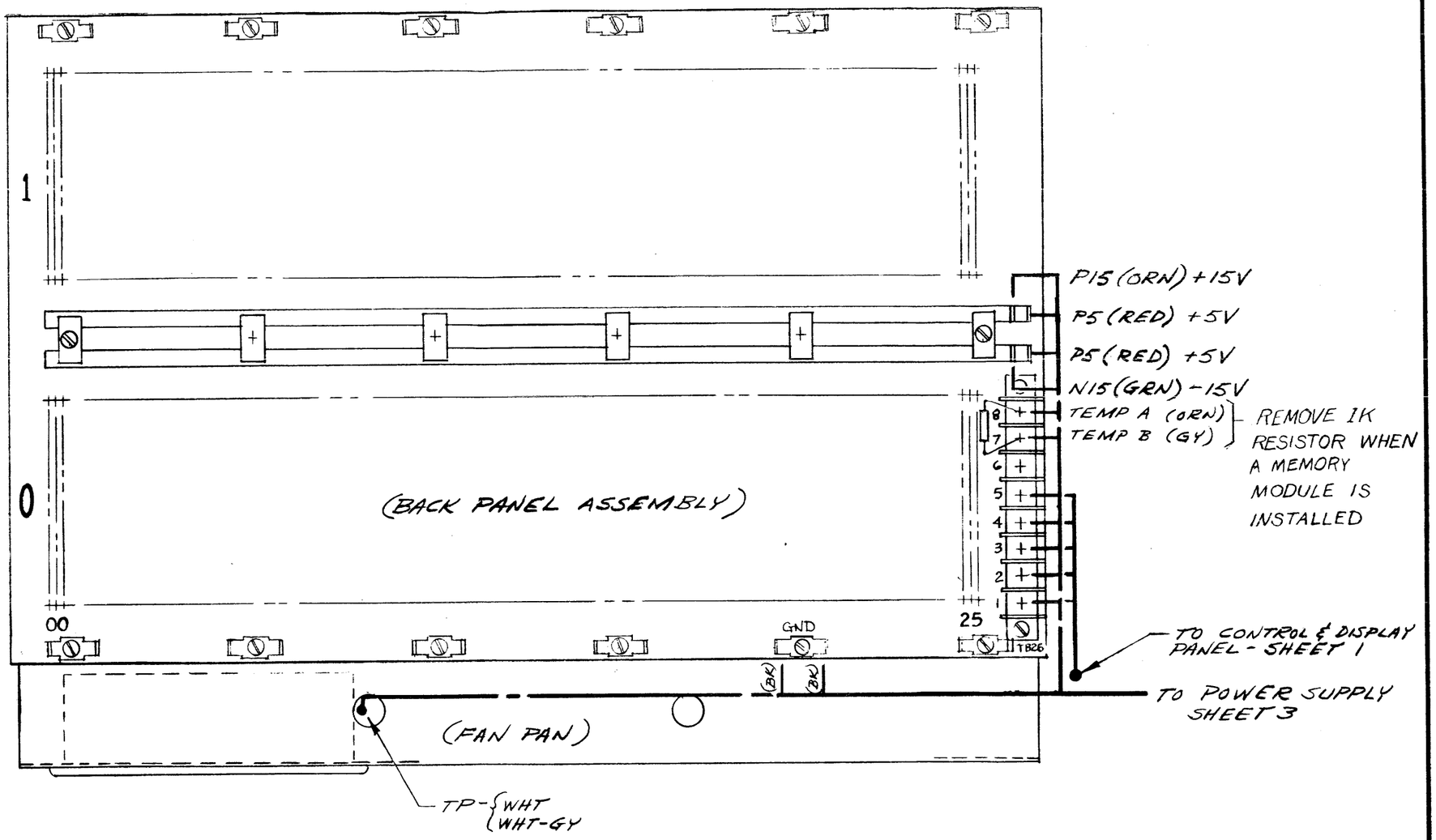
5. GENERAL RULES

1. The Memory Modules must be located in two adjacent chassis.

2. The first Memory Module (four boards) in the 48KB Expansion Chassis must be located in the lowest numbered slots that are available for a Memory Module.

3. The 48KB Expansion Chassis, 02-221, is designed for use with the 02-205 Memory Modules only, and will not function with any other.

4. The terminating board, 35-378, must be installed in Slot 22, Connector 0, Rows 1 and 2 for proper operation of the memory system.



REAR VIEW

CABLE PATH SHOWN FOR PROCESSOR CARD FILE

NOTES

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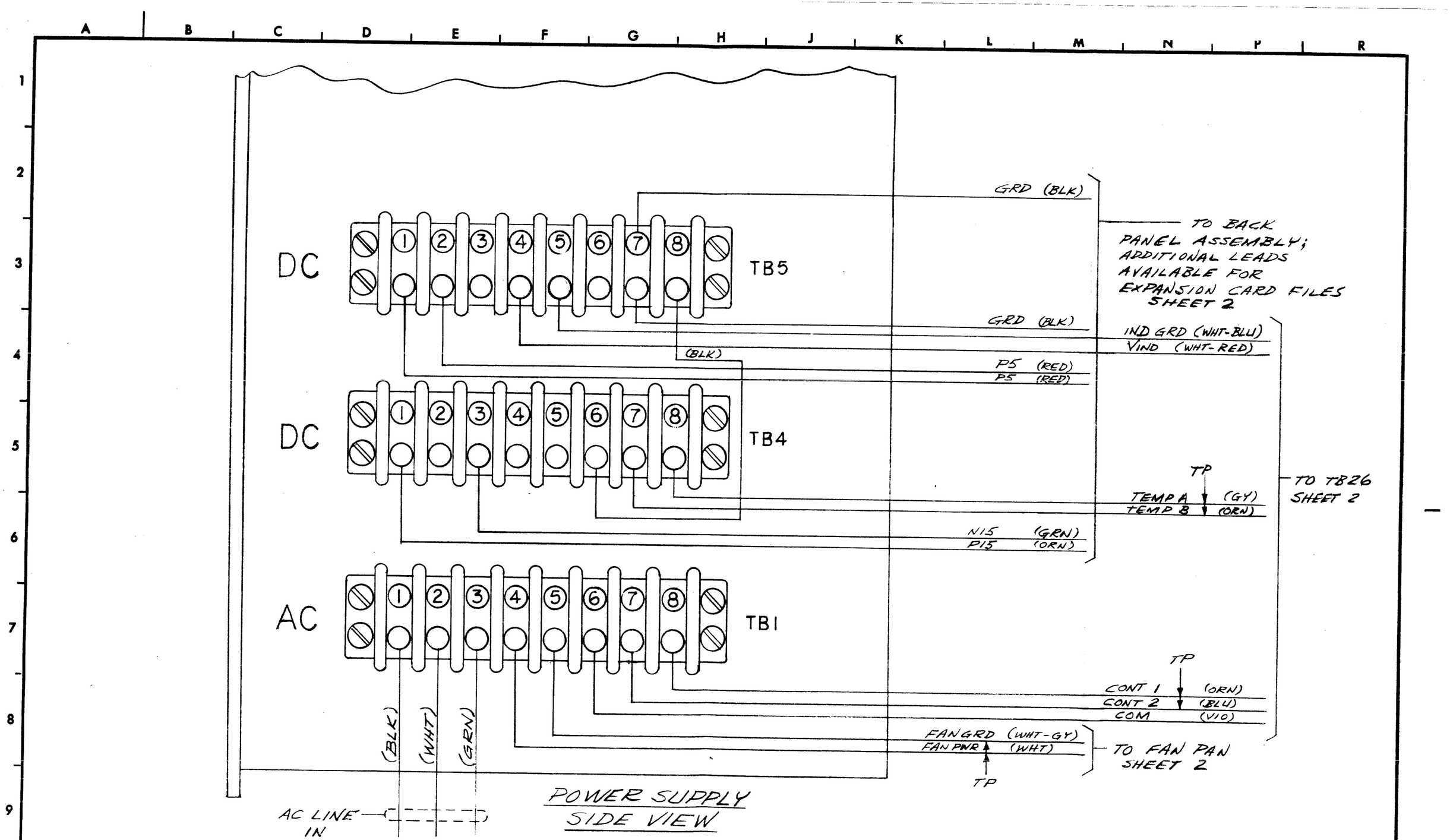
TITLE: GENERAL PURPOSE INSTALLATION SPECIFICATION

TASK NO. 3-109 | SHEET OF 2-3

DWG. NO. 3-109 R02 B20



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TASK NO. 3-109 | SHEET OF 3 - 3

DWG. NO. 3-10? RUC 320

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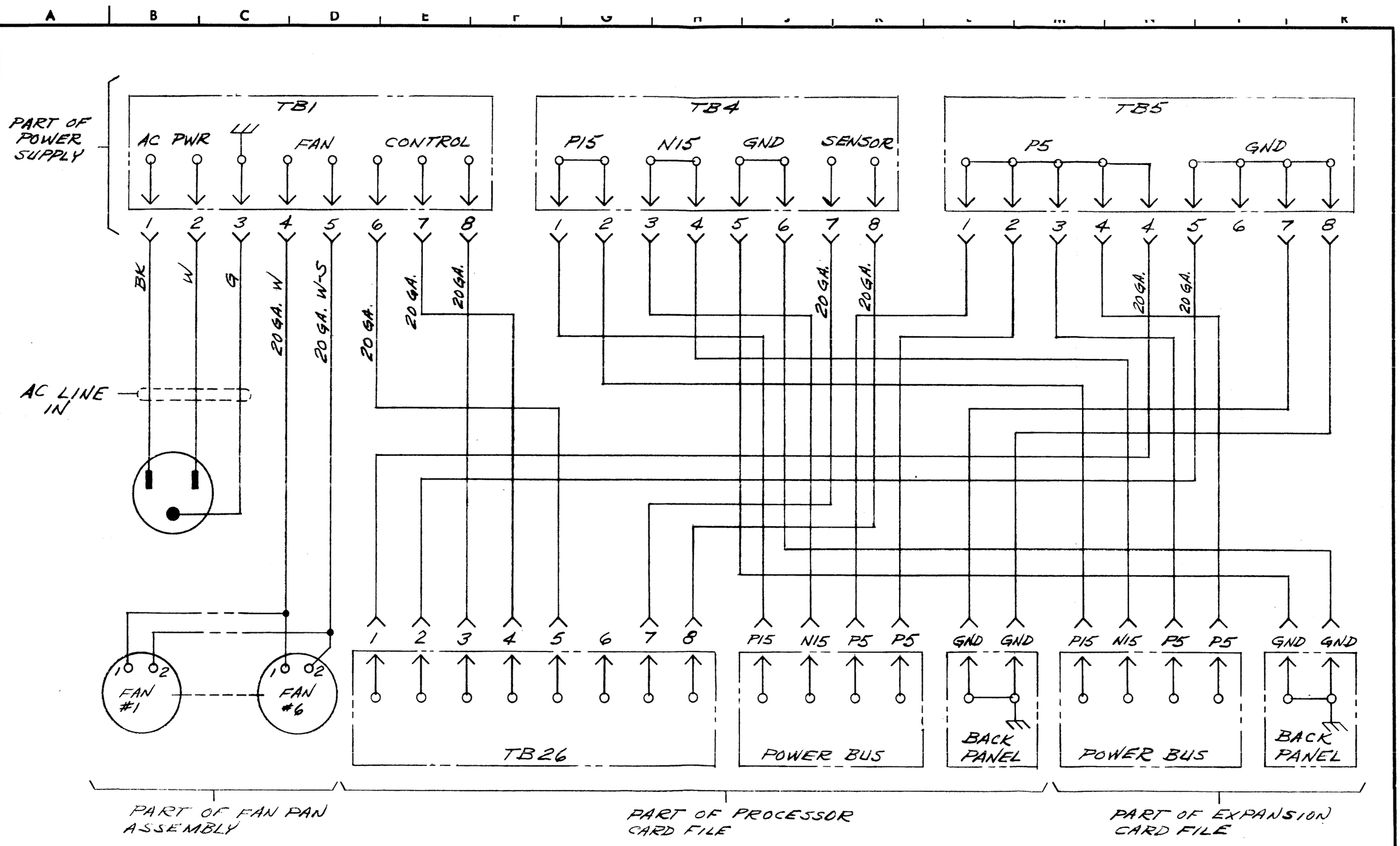

NOTES 1. UNLESS OTHERWISE SPECIFIED, ALL LEADS SHALL BE 14 GA. STRANDED WIRE. ALL WIRE IS WHITE

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B.W.SATHMARY	ENGR	6-19-68
A.G.ALESSI	PROD	6-19-68
A.R.FURMAN	DIR.ENG.	6-15-68

TITLE: CABLE WIRING DIAGRAM, POWER - SYSTEM CABINET

TASK NO. 30-113

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MODEL 70
SYSTEM TEST SET
INSTRUCTION MANUAL

Consists Of:	Operating Instructions	28-010A16
	Schematics	28-010B08

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April 1972

MODEL 70 SYSTEM TEST SET OPERATING INSTRUCTIONS

1. INTRODUCTION

The Model 28-010 System Test Set (often referred to as a Mots Box) is a maintenance test device which permits manual control of an INTERDATA Digital System. Indicators on the test set display the contents of several pertinent registers and the Sum Bus within the system. The system test set is compatible with all INTERDATA Digital Systems except the Model 1.

2. SET UP PROCEDURE

Use the following procedure to connect the system test set to the digital system.

CAUTION

Remove power from the digital system
and disconnect it from its power source
before proceeding.

1. Carefully remove the cable assembly from its storage compartment in the system test set.

2. Connect the four 35-103 PC board/cable connectors P1 through P4 to their corresponding test set connectors, J1 through J4, on the rear of the system test set. Refer to Figure 1.

3. Connect the three PC board/cable connectors (i.e., 35-419 ROM-0, 35-420 ROM-1, and 35-421 ALU-1) on the other end of the cable bundle to their corresponding board slots on the back panel of the Processor chassis.

4. The system test set derives its power from the digital system. Connect the power cable as follows:

   Red wire probe to power supply socket labeled P5
   Black wire probe to power supply socket labeled GND

5. Check that all connectors are mated properly and apply power to the system.

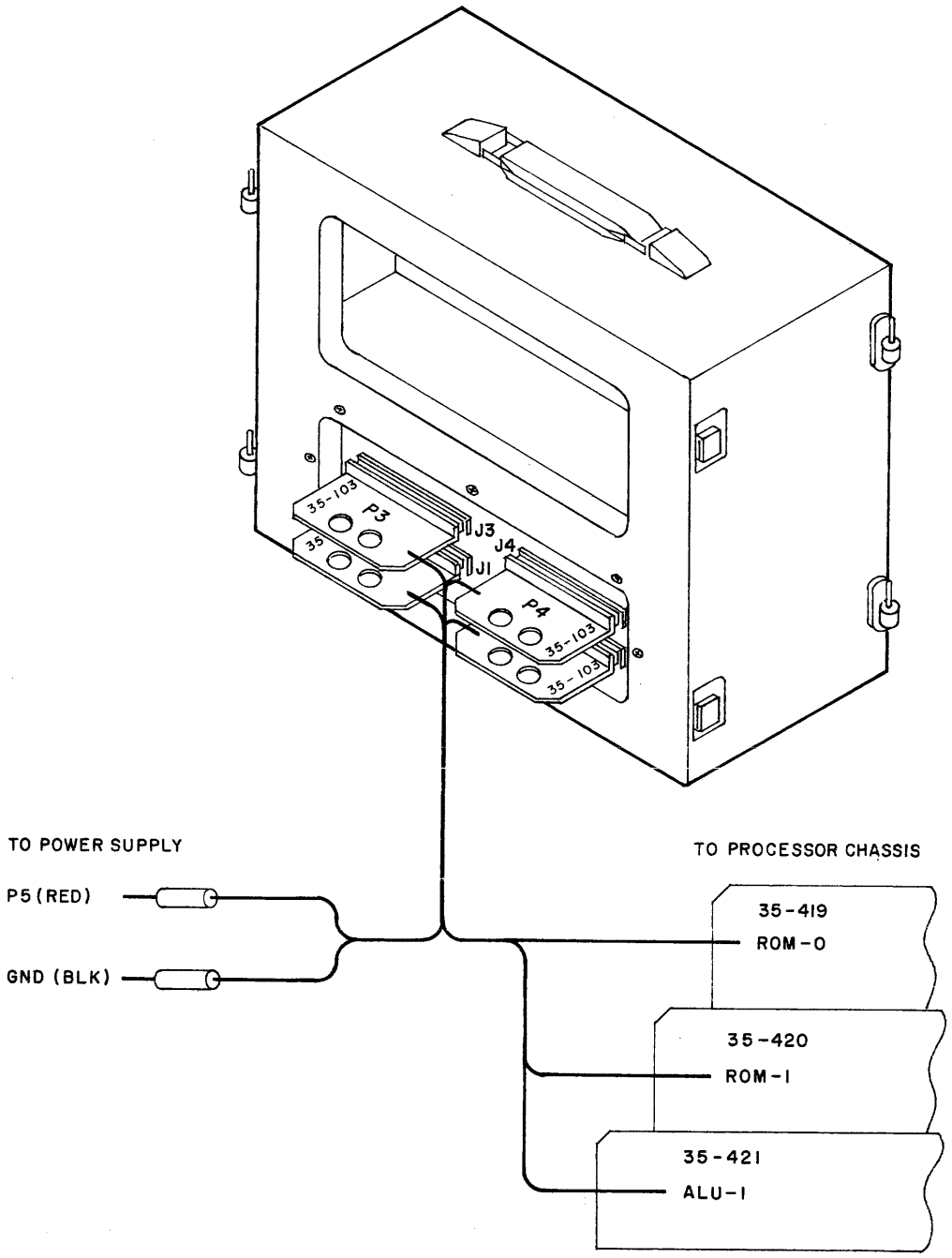


Figure 1. System Test Set Cabling

3. CONTROLS AND INDICATORS

Each of the controls and indicators on the system test set that are used with the Model 70 are described in the following paragraphs. Refer to Figure 2. For information on the remaining controls and indicators which may be used with other INTERDATA Digital Systems, refer to System Test Set Manual, Publication Number 29-012.

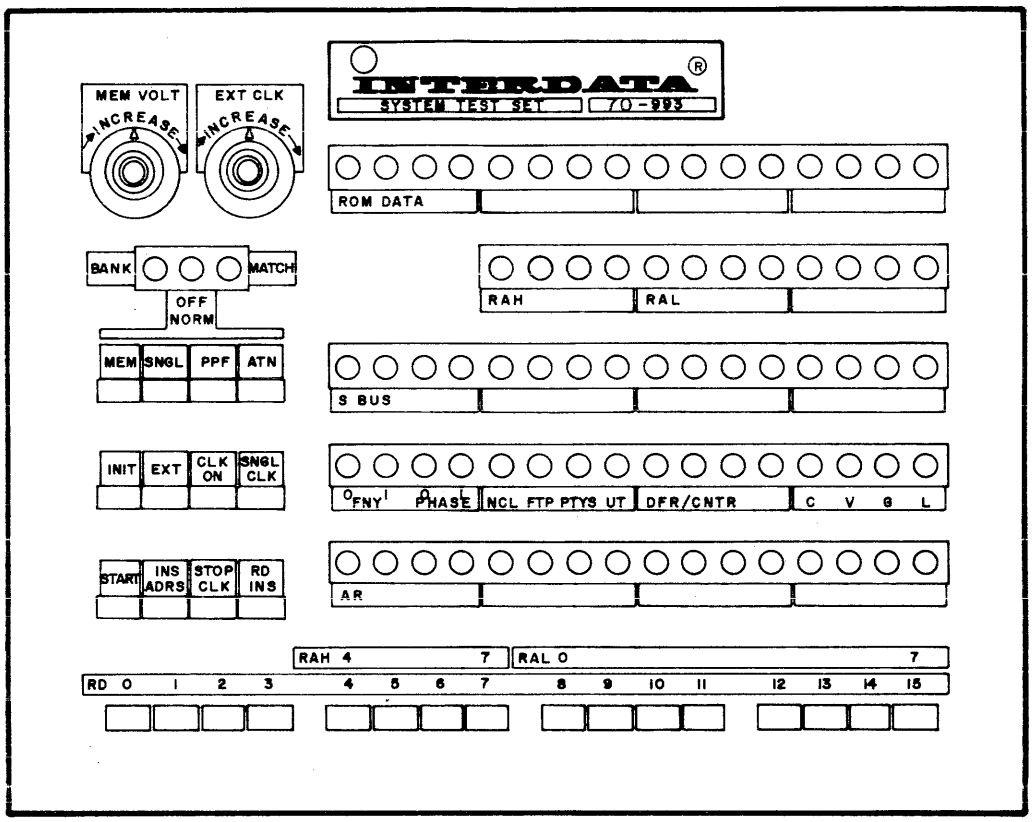


Figure 2. Control Panel Layout

3.1 Controls

INIT - Depressing the Initialize switch (INIT) performs the same function as the Initialize switch on the Processor Control Panel, that is, the initialize relay in the Processor is released. This stops the clock momentarily, and clears the ROM Address Register and other flip-flops in the system.

CLK ON - Depressing the Clock On switch (CLK ON), followed by depressing the Start switch (START), causes the system clock to run. The clock may be stopped by releasing the Clock On switch.

SNGL CLK - If the system clock is off, depressing the Single Clock switch (SNGL CLK) generates a single clock pulse to execute one micro-instruction at a time.

START - Depressing the START switch permits the system clock to start running if the CLK ON switch is depressed. The first micro-instruction to be executed is the instruction currently in the ROM Data Register.

INH ADRS - Depressing the Inhibit Address switch (INH ADRS) stops the ROM Address Register clock when the data switches match the ROM address. Note that the Processor clock is still running and ROM readouts are still strobed into the ROM Data Register even though the ROM Address Register clock is stopped. This micro-instruction will be executed repeatedly.

RD INS - The Read Instruction switch (RD INS) is normally a momentary action switch when used with other INTERDATA digital computer systems. In the Model 70 it is desireable to have the RD INS switch latching (e.g. CLK ON). To modify the RD INS switch, remove the latch retaining clip and pin from the STOP CLK latch switch, which is not used with the Model 70, and insert them in the RD INS switch assembly. Refer to Figure 3 for an example of RD INS modification.

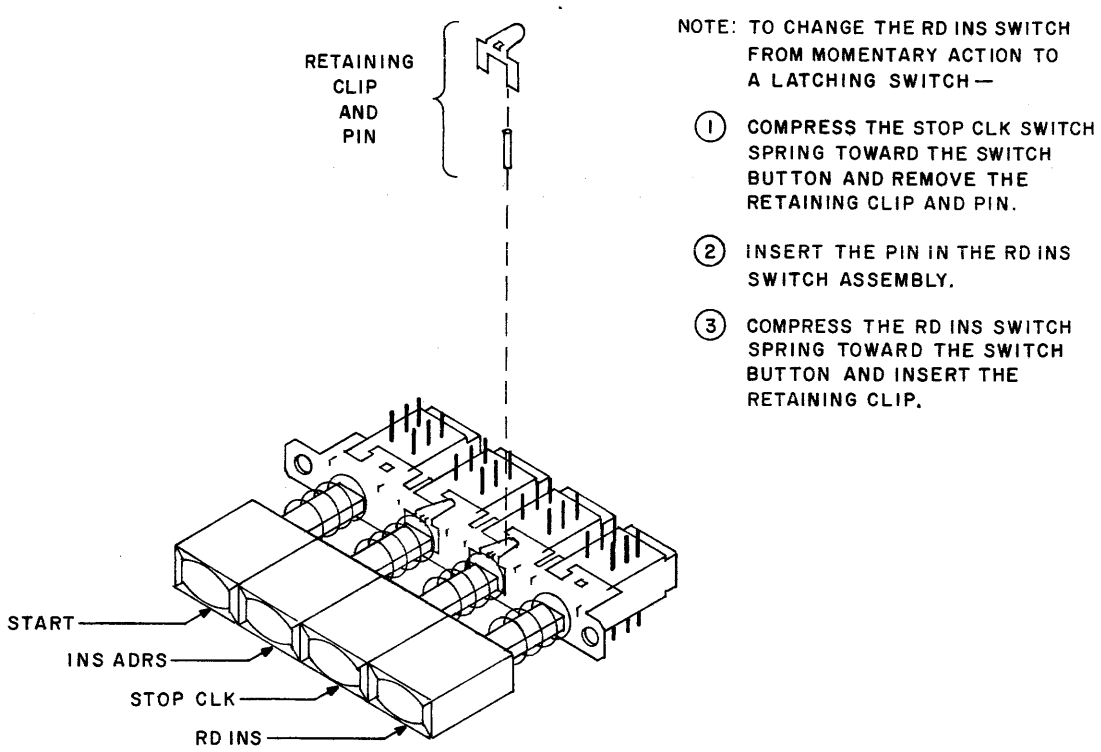


Figure 3. Control Panel Switch Modification

This modification is performed at the INTERDATA factory at Oceanport, New Jersey, when a customer initially purchases a system test set for use with a Model 70 system. If the customer is presently using a system test set, he must modify his test set to function properly on the Model 70.

Depressing the Read Instruction switch (RD INS) causes the contents of the data switches to be loaded into the ROM Data Register. This may be observed on the ROM data lamps. The RD INS switch must be used in conjunction with the ATN switch and either the SNGL CLK or PPF switch.

To load the ROM Data Register with the contents of the data switches:

1. Depress the ATN switch. This causes the disabling of all ROM readouts.

2. Depress the RD INS switch. This causes the contents of the data switches to be presented to the ROM Data Register, awaiting a clock.

3. Depress the SNGL CLK switch. This causes data on the data switches to be clocked into the ROM Data Register and the ROM Address Register to be incremented by one. As an option the PPF switch is offered as a clock to load the contents of the data switches into the ROM Data Register. This action does not increment the ROM Address Register.

ATN - The ATN switch is only used for inserting the contents of the data switches into the ROM Data Register during a RD INS. When this switch is depressed the ROM readouts are disabled. This switch must be used in conjunction with the RD INS switch and either the SNGL CLK or PPF switch.

DATA SWITCHES - The 16 data switches, at the bottom of the system test set Control Panel, are used to perform a dual function:

1. The data set into these switches is loaded into the ROM Data Register when the RD INS switch is depressed, with the ATN switch depressed, and the clock stopped.

2. The right-most 12 switches may be used as a constant to match against the ROM Address Register.

3.2 Indicators

The indicators light when the associated bit or flip-flop is set.

ROM DATA - The 16 ROM data lamps indicate the contents of the last address read from the Read-Only-Memory.

BANK - This indicator lights when the Bank flip-flop is set.

OFF NORMAL - Indicates that at least one of the following switches is depressed: MEM, SNGL, PPF, or ATN.

MATCH - Indicates a match condition between the 12-bit ROM Address Register and the data switches at the bottom of the system test set Control Panel.

RAH - These lamps monitor the four most significant bits of the second rank of the ROM Address Register.

RAL - These lamps monitor the eight least significant bits of the ROM Address Register. Ordinarily, these lamps display the address of the next instruction to be executed.

S BUS - These 16 indicators monitor the contents of the 16-bit S Bus (Sum Bus), the result of all arithmetic and logical operations will be displayed on the S Bus.

4. OPERATING PROCEDURES

The following procedure assumes that the system test set has been properly connected to a normally functioning Model 70.

4.1 Initial Start-Up

1. Connect the system test set as outlined in Section 2.
2. Release all switches on the test set except the CLK ON switch. (Depress the CLK ON switch if it is not already depressed.)
3. Turn the digital system power on.
4. Depress the momentary action START switch. This starts the system clocks. The system is now in the normal users mode.
5. At this point the system may be investigated by the system test set. Perform any of the desired functions to examine results. That is, clock stopping, ROM address matching, single stepping each ROM address, or inserting any desired data into the ROM Data Register by the RD INS switch.

5. FUNCTIONAL DESCRIPTION

The following description refers to the seven sheet Model 70 System Test Set Functional Schematic 28-010B08. Sheet 1 of the schematic shows the A section of each of the Data/Address switches on the bottom of the system test set Control Panel, and the interconnection of the switches to the Processor back panel. As shown in Figure 1, J1 and J2 are on the rear of the system test set and connections P1 and P2 are on the cable assembly. Note the latching Read Instruction switch (RD INS) contacts shown in the lower left area of Sheet 1. When the RD INS switch is depressed, the condition of switches S00 through S15 are gated into the ROM Data Register.

Sheet 2 of the schematic shows the ROM data lamps on the system test set Control Panel, and the gates which drive them. Note that there is no gating involved. Thus, the ROM data lamps continuously display the contents of the RD Register in the digital system.

Sheet 3 shows the 16 bits of the S Bus display.

The left half of Sheet 4 shows the RAH display logic. The four outputs to Sheet 6 are high when the RAH bit matches the corresponding S4 through S7 switch condition. For example, if S4 is depressed and RAH04 is set, the MRAH041 signal is high. The right half of Sheet 4 shows the P5 lamp power and P5 logic power connections to the system test set.

Sheet 5 shows the RAL display logic. Note that outputs to the address match logic on Sheet 6 are similar to those shown on Sheet 4 and described earlier in this section.

The ROM address match logic is shown on the left side of Sheet 6. When the ROM address matches the configuration set in Switches 4 through 15, the output from the gate shown in area C5 goes high. This output is applied to two gates shown in area D6 and D7. Going from the top to bottom, the first gate lights the MATCH indicator on the Control Panel. If the INH ADRS switch on the Control Panel is set, the next gate sends a signal to the Processor to inhibit incrementing the ROM address.

The PPF and ATN switches in areas L6 and M6 supply signals to the Processor and are OR-tied to light the OFF NORMAL indicator. The final circuit on Sheet 6 lights the BANK indicator when the Bank flip-flop in the Processor is set.

Sheet 7 of the schematic shows the system test set clock and control logic. When the CLK ON switch (L6) is depressed, ground is removed from the gate at E7. Depressing the START switch (F7) enables the gate at C7 which applies a high to the J input and a low to the K input of the flip-flop at L2. The CLKOFF0 signal to the Processor is high. The Processor clock runs normally until the CLK ON switch is released.

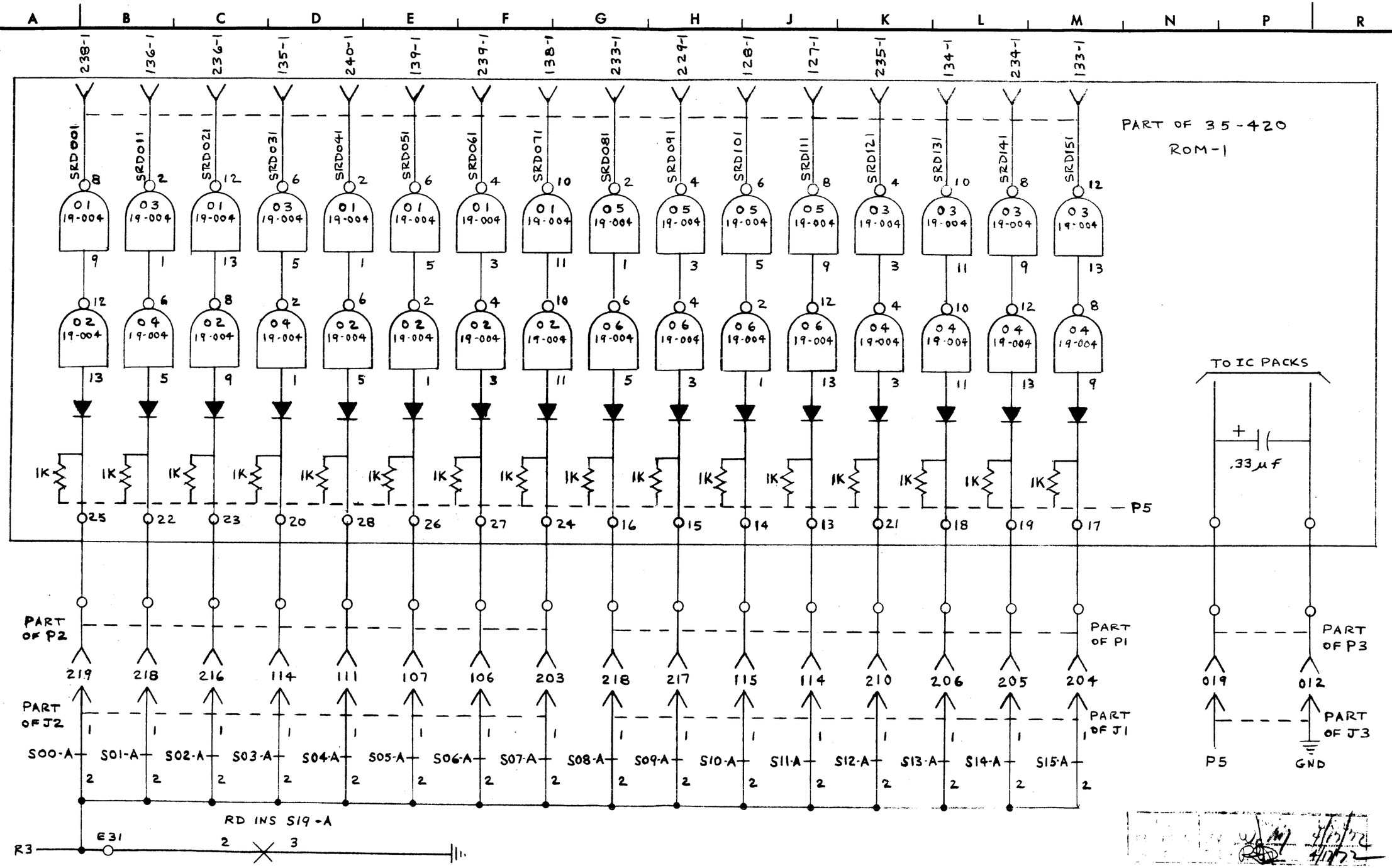
The SNGL CLK switch is shown in area N7. If the CLK ON switch is released, each time the SNGL CLK switch is depressed the flip-flop in area M8 is set. The flip-flop set output direct sets the flip-flop at L2 via the gates in area J3 and K3 and the 19-034 One Shot Multivibrator. The flip-flop at L2 is reset by the System Clock signal (SYSCL) from the Processor clock.

The Initialize switch (INIT), shown in area N6, produces a POW0 signal to the Processor each time it is depressed.

6. MAINTENANCE

Maintenance on the system test set itself is normally restricted to the periodic replacement of indicator lamps. The lamps slip straight out from the front. It is normally possible to remove the lamp by hand. The replacement lamp, INTERDATA Part Number 33-011 or Sylvania Part Number 12ESB, is pushed into place by hand.

If a trouble is encountered in the system test set, use the functional description provided in Section 5 and Functional Schematic 28-010B08 to locate the malfunction.



NOTES	REVISED SHEET 6	NAME	TITLE	DATE	TITLE
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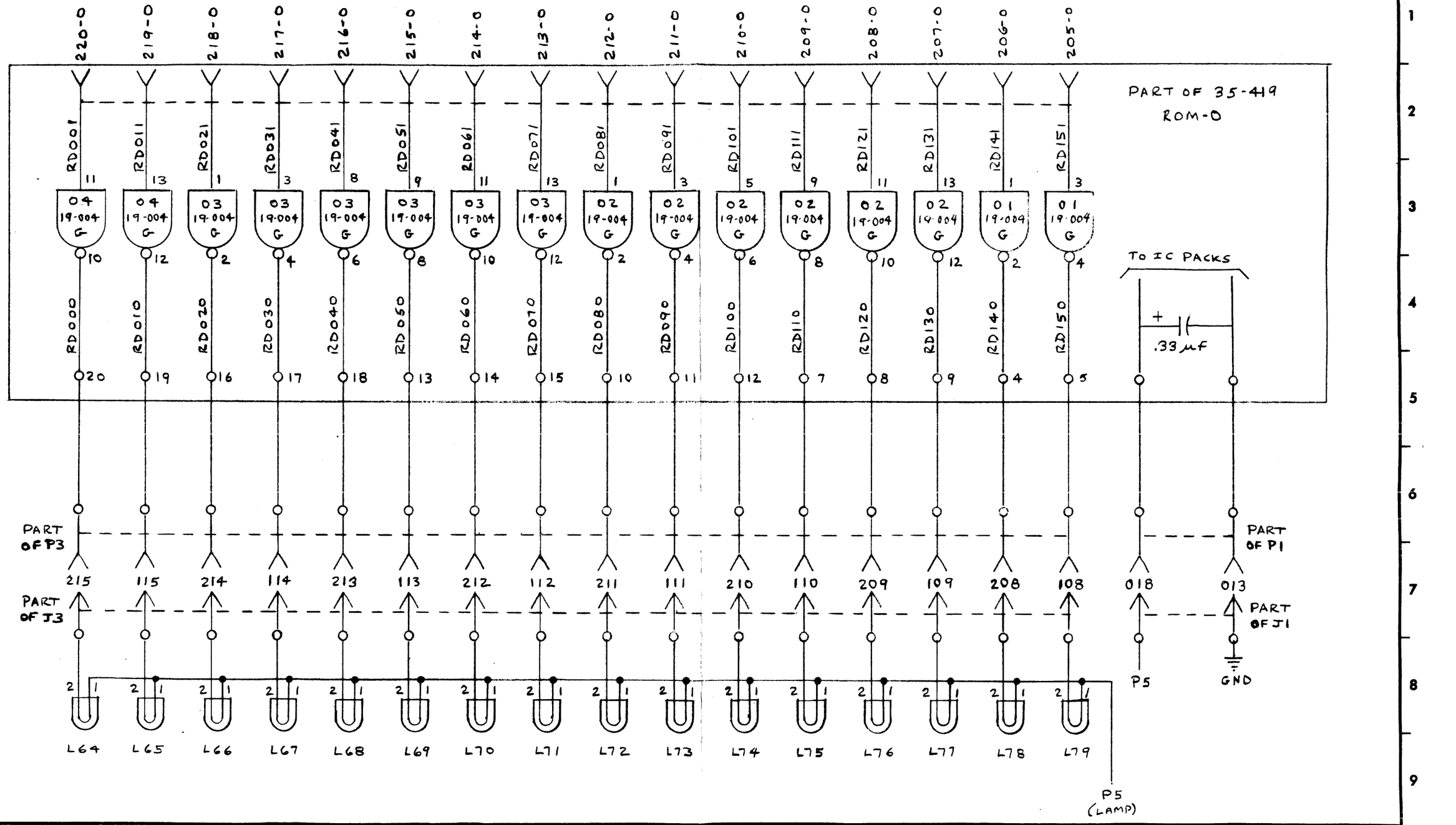
					TASK NO. 03116
					DWG. NO. 28-010R01808
					SHEET OF 1-7



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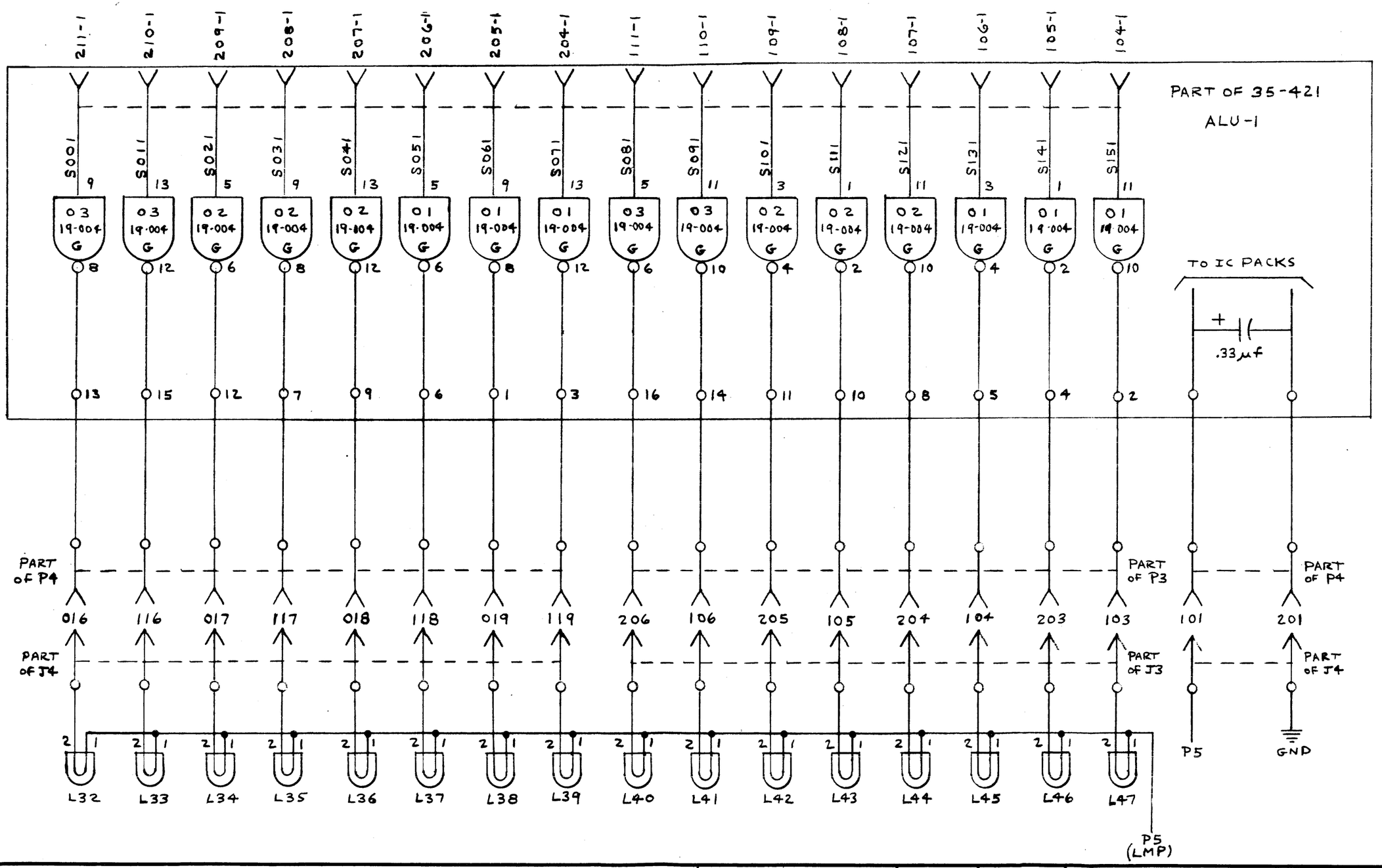
				DWG. NO. 28-010R01B08



NOTES

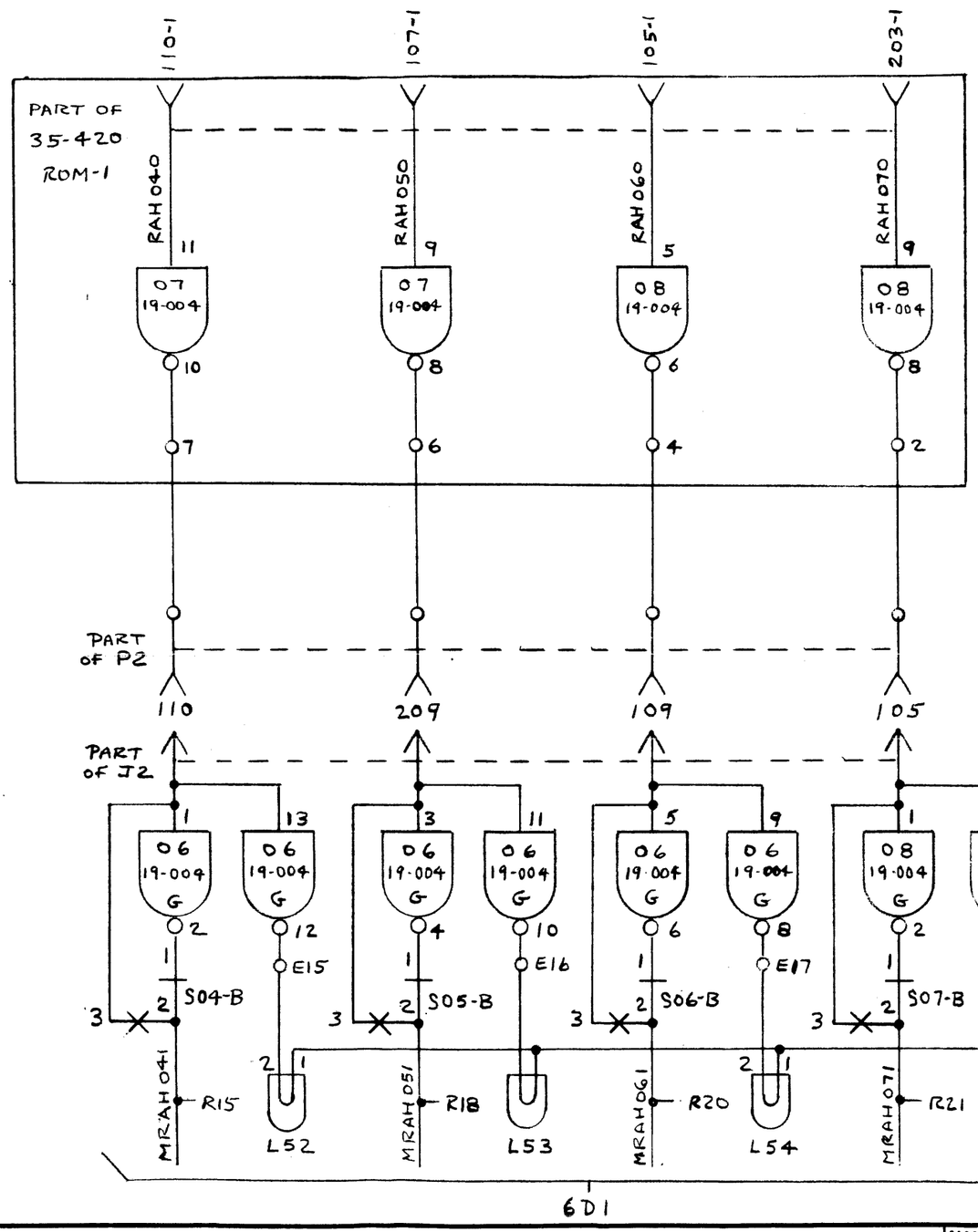
NAME	TITLE	DATE

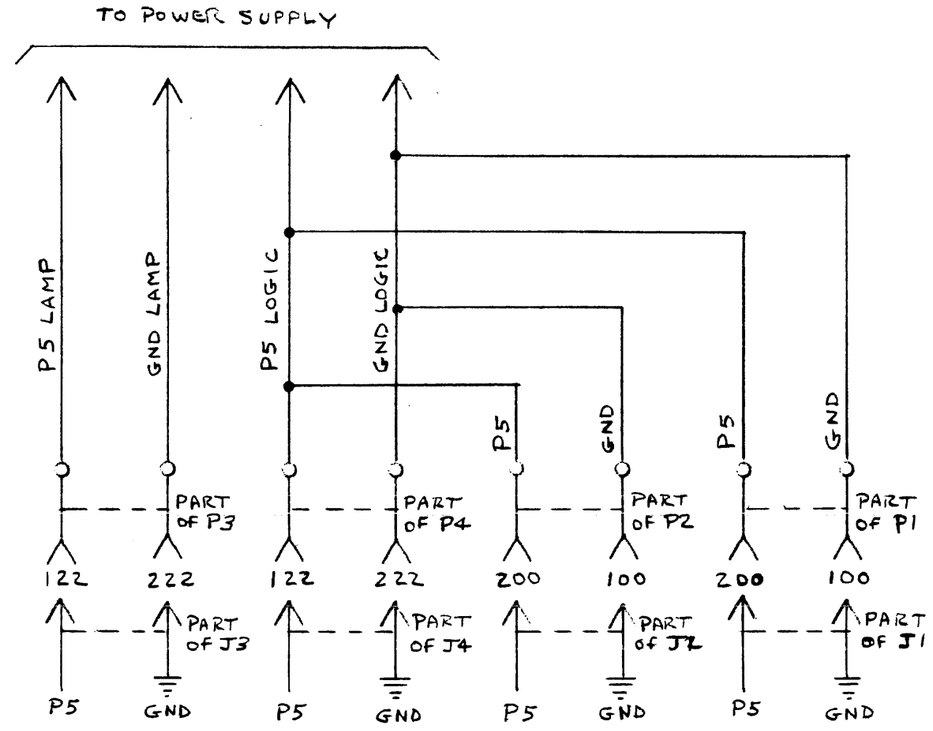
TITLE: MODEL 70 SYSTEM TEST SET

TASK NO. 03116

DWG. NO. 28-010R01B08

SHEET OF 3 - 7





NOTES

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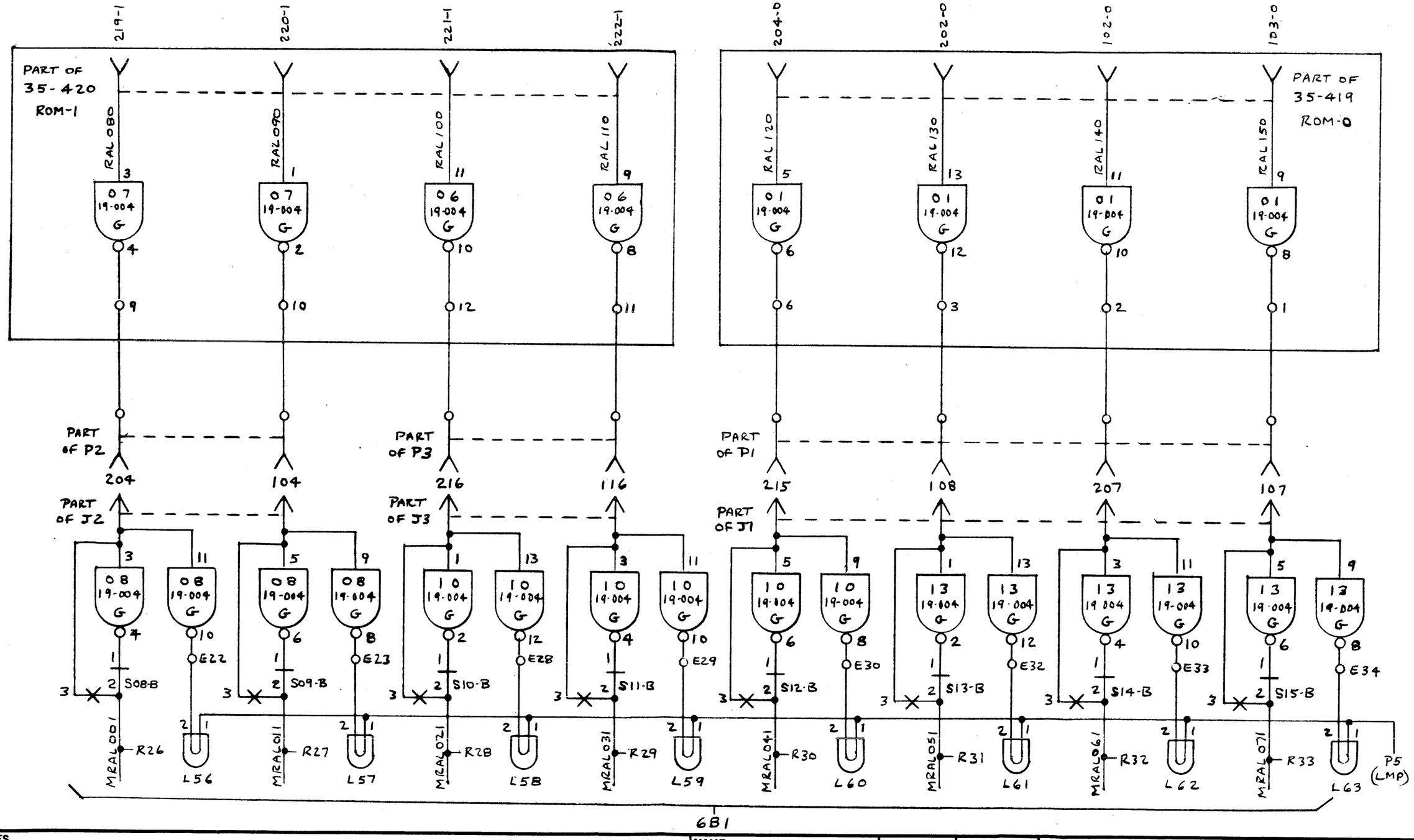
TITLE: MODEL 70 SYSTEM TEST SET

TASK NO. 03116

DWG. NO. 28-010R01B08

SHEET OF 4-7



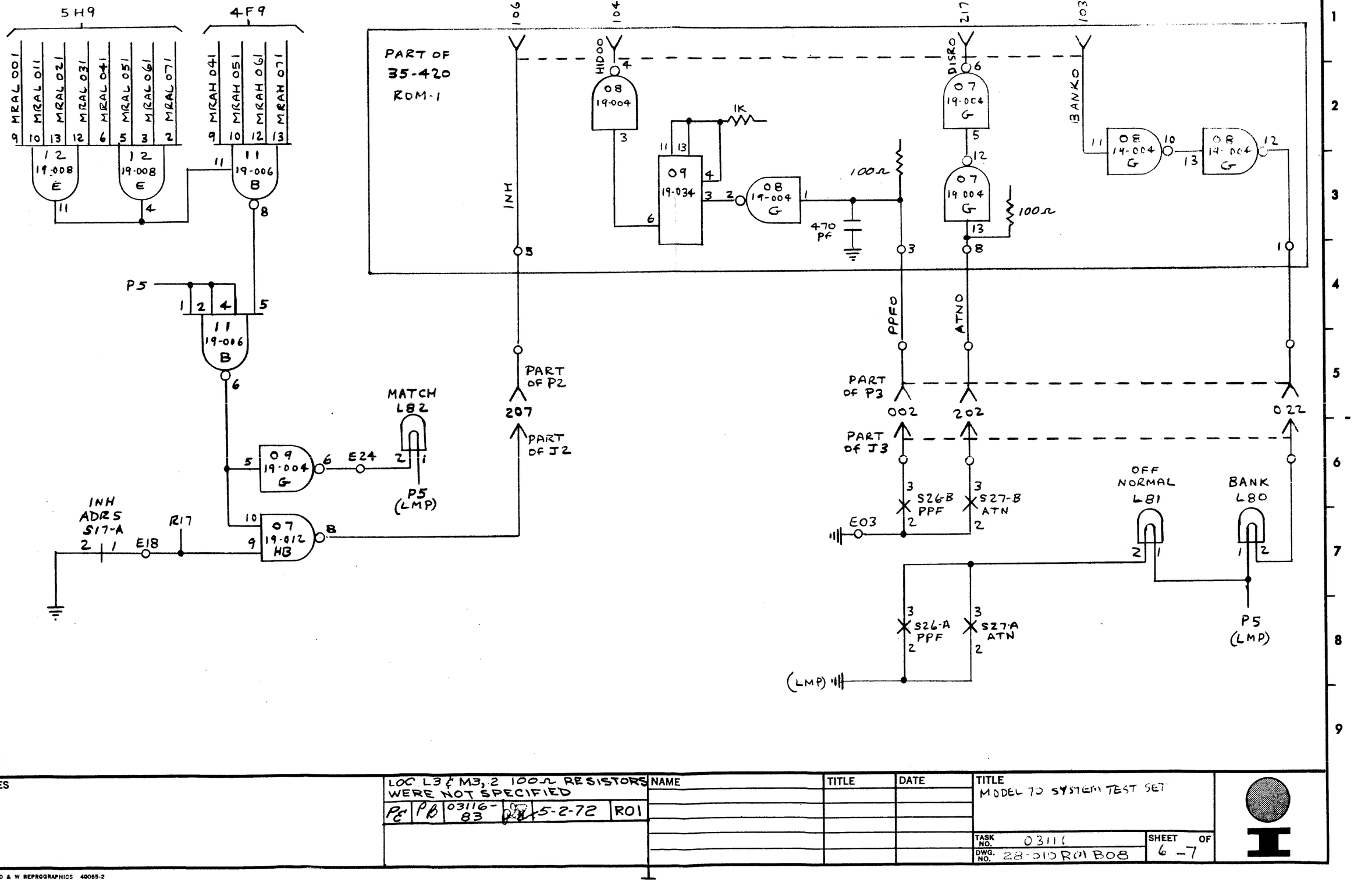
NOTES

NAME	TITLE	DATE

TITLE: MODEL 70 SYSTEM TEST SET

TASK NO. 03116 | SHEET OF 5 - 7

DWG. NO. 28-010R01B08



NOTES

LOC L3 & M3, 2 100Ω RESISTORS WERE NOT SPECIFIED

PC	PB	03116-83	5-2-72	R01

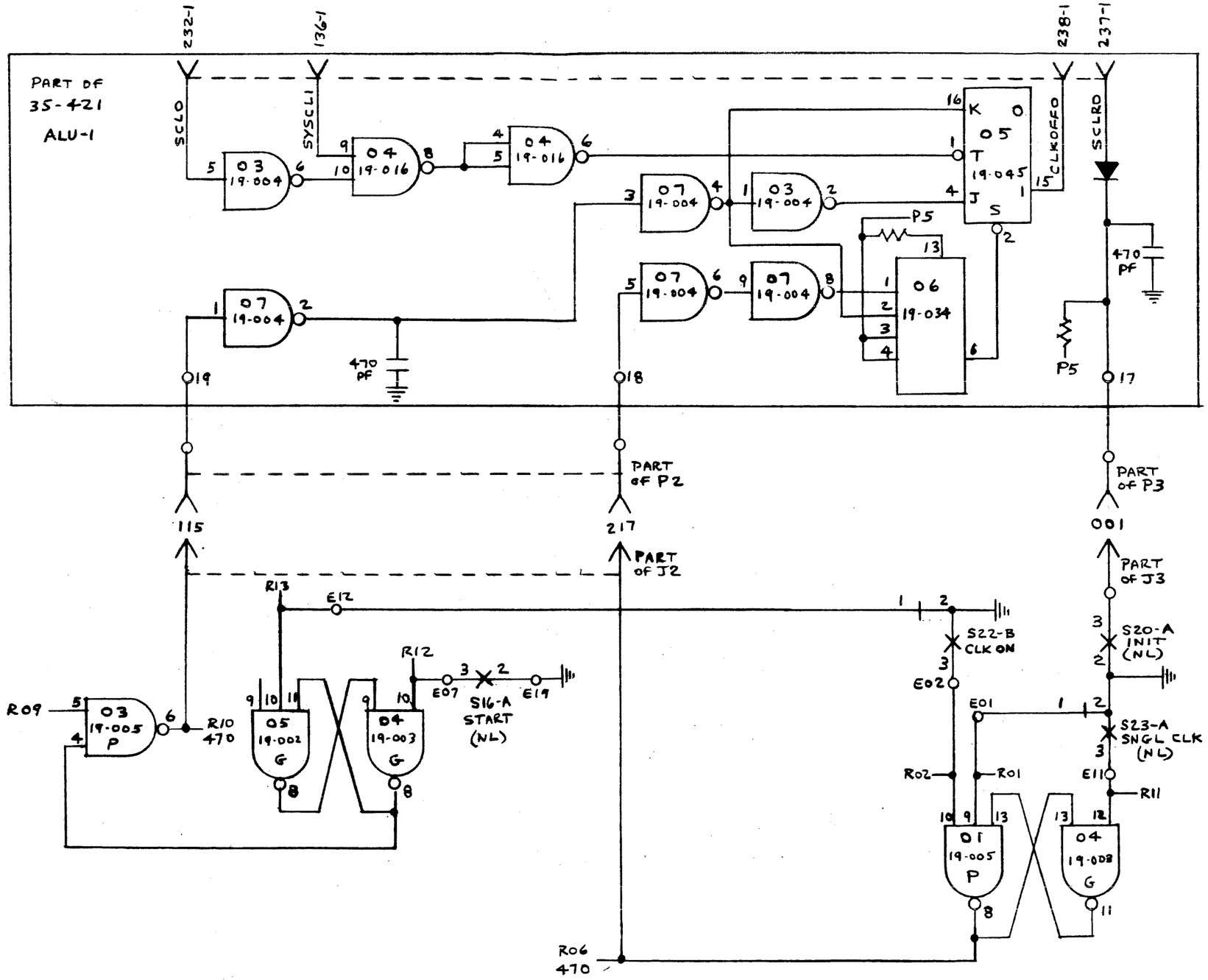
NAME	TITLE	DATE

TITLE: MODEL 70 SYSTEM TEST SET

TASK NO. 03116

DWG. NO. 28-210 R01 B08

SHEET 6 OF 7



NOTES	NAME	TITLE	DATE	TITLE
				MODEL 70 SYSTEM TEST SET
				TASK NO. 03116
				DWG. NO. 28-010R01B08
				SHEET 7 OF 7

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SYSTEM TEST SET
INSTRUCTION MANUAL

Consists Of:	Operating Instructions	28-001R01A16
	Schematics	28-001R07B08

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August 1970

SYSTEM TEST SET OPERATING INSTRUCTIONS

TABLE OF CONTENTS

ILLUSTRATIONS

SYSTEM TEST SET OPERATING INSTRUCTIONS

1. INTRODUCTION

The Model 28-001 System Test Set (often referred to as a MOTS Box) is a maintenance test device which permits manual control of an INTERDATA Digital System. Indicators on the Test Set display the contents of all pertinent registers and buses within the system. The System Test Set may be used in maintaining systems with standard Read-Only-Memories (ROMs), and is required if a special maintenance ROM (X-Ray ROM) is used. The plug-in X-Ray ROM is substituted for the normal ROM in the system under test. X-Ray ROM details are provided in separate publications. The System Test Set or System Test Set/X-Ray ROM combination permits rapid check-out and/or trouble analysis of an INTERDATA Digital System. The System Test Set is compatible with all INTERDATA Digital Systems, except Model 1. Unless otherwise noted, all comments in this manual apply equally to all Digital System Models.

2. SET-UP PROCEDURE

Use the following procedure to connect the System Test Set to the Digital System.

CAUTION

Remove power from the Digital System and disconnect it from its power source before proceeding.

1. Carefully remove the cable assemblies from their storage compartment in the System Test Set.

2. Connect the P1 through P3 cable connectors to the J1 through J3 connectors on the rear of the Test Set. Refer to Figure 1.

3. Connect the other end of the cables to the back panel of the Digital System. Refer to Figure 1.

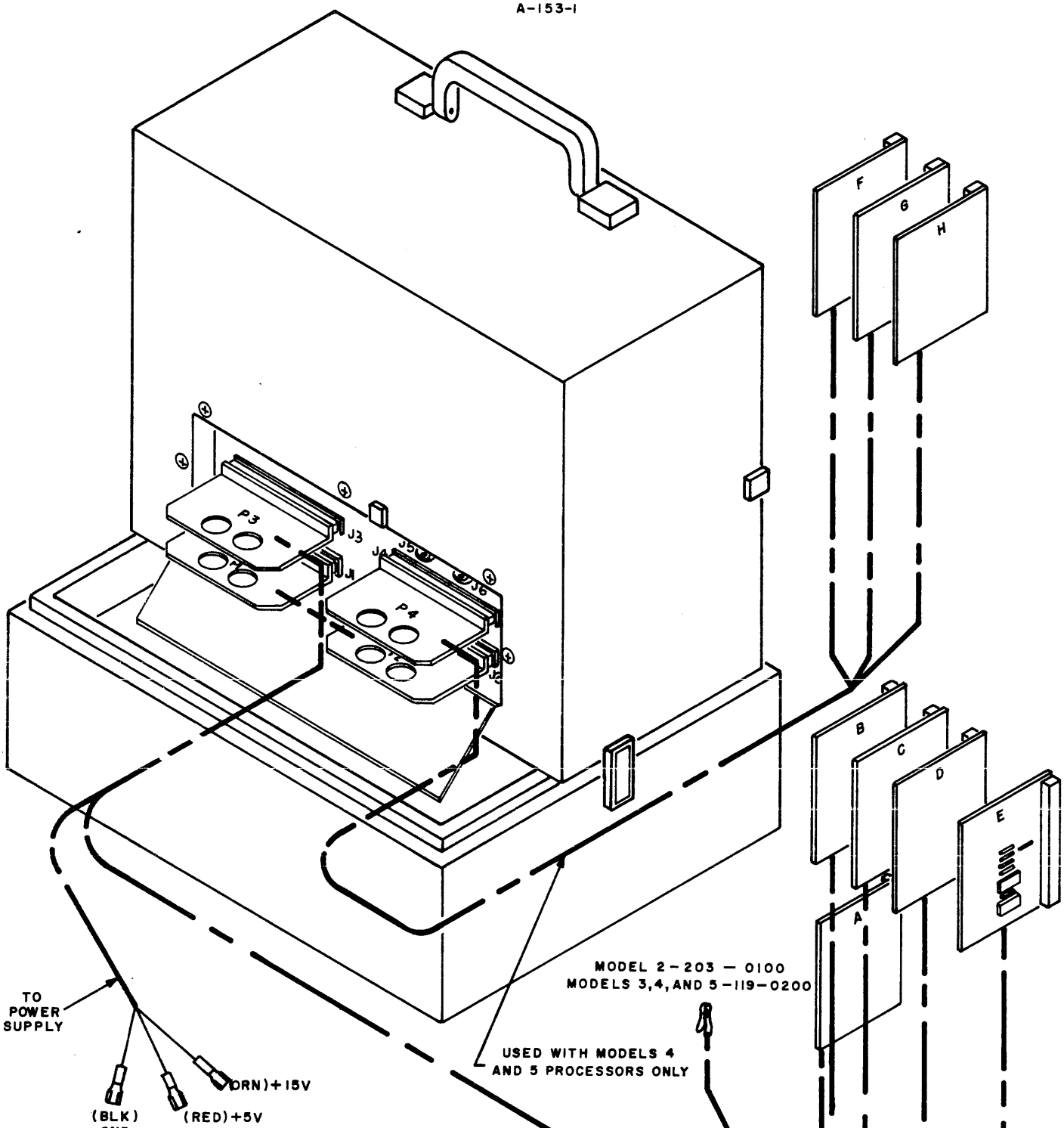
4. The System Test Set derives its power from the Digital System. Connect the power cable as follows:

Voltage	Wire Color	Location	Use
+15	Orange	TB4-2	Memory Voltage Reference
+ 5	Red	TB5-3	Lamp Supply
GRD	Black	TB5-6	Lamp Ground

5. Clip the final lead (used for the memory threshold adjustment) to the back panel as follows:

   Model 2 - 203-0100
   Models 3, 4, and 5 - 119-0200

6. Check that all connectors are mated properly and apply power to the system.



MODEL	CONNECTOR A	B	C	D	E	F	G	H
MODEL 2 01-002	RMI-0 ROWS 1,2	RMI-1 ROWS 1,2	BS1-1 ROWS 1,2	BS2-1 ROWS 1,2	CO2-1 ROWS 0,1	NA	NA	NA
MODEL 3 01-003	RMI-0 ROWS 1,2	RMI-1 ROWS 1,2	BS1-1 ROWS 1,2	BS2-1 ROWS 1,2	CO2-1 ROWS 0,1	NA	NA	NA
MODEL 4 WW01-004	RMI-0 ROWS 1,2	RMI-1 ROWS 1,2	BS3-1 ROWS 1,2	BS2-1 ROWS 1,2	CO1-1 ROWS 0,1	CO2-1 ROWS 1,2	BS1-1 ROWS 1,2	BS0-1 ROWS 1,2
MODEL 4CU 01-013 AND MODEL 5 01-015	RMI-0 ROWS 1,2	RMI-1 ROWS 1,2	BS3-1 ROWS 1,2	BS2-1 ROWS 1,2	CO0-1 ROWS 1,2	CO1-1 ROWS 1,2	BS1-1 ROWS 1,2	BS0-1 ROWS 1,2

Figure 1. System Test Set Cabling

3. CONTROLS AND INDICATORS

Each of the controls and indicators on the System Test Set control panel is described in the following paragraphs. Refer to Figure 2.

3:1 Controls

MEM VOLT — The MEMory VOLTage potentiometer is used to vary the bias in the core memory. The potentiometer is connected only when the MEM Switch is depressed.

EXT CLK — The EXTernal CLocK potentiometer is used to vary the frequency of a test clock which may be substituted for the system clock. The potentiometer is connected only when the EXT Switch is depressed.

MEM — When depressed, the MEMory Switch enables the MEM VOLT potentiometer which is used to test the bias margins in the core memory. This switch should normally be released - if not, marginal core memory operation may result.

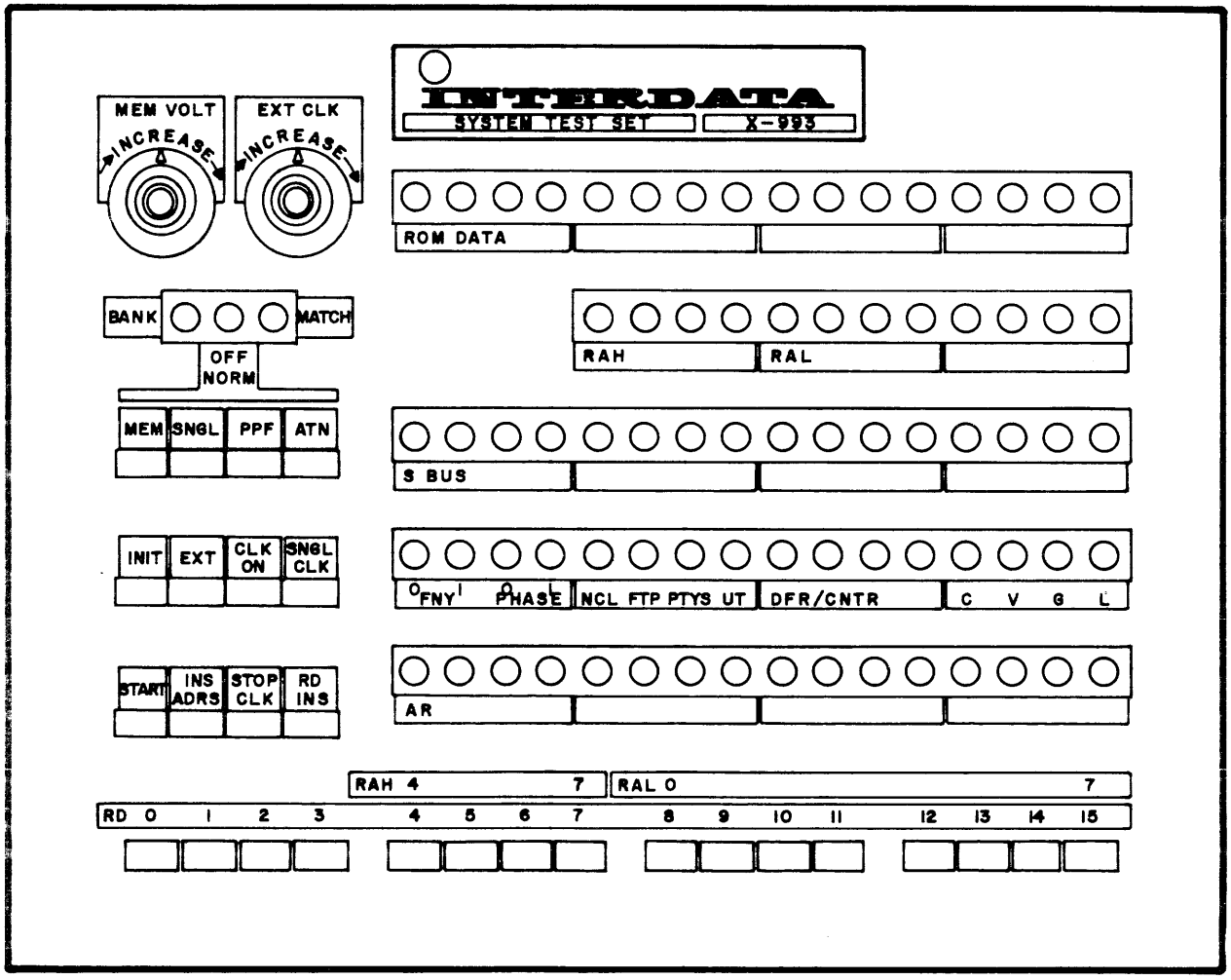


Figure 2. Control Panel Layout

ATN, PPF, and SNGL — These switches are used as sense switches for the X-Ray. (See Section 4.) If an X-Ray ROM is not in place in the computer, these switches should all be released. The OFF NORMal lamp lights if any are depressed.

INIT — The INITialize Switch performs the same function as the INITIALIZE Switch on the front panel, the Initialize relay in the Processor is released. This stops the clock momentarily, and clears the ROM address register and other flip-flops in the system.

EXT — When depressed, the EXTernal Switch enables the clock frequency to be controlled by the EXT CLK potentiometer. If the switch is released, the crystal-controlled clock in the Processor is enabled. This switch should not be operated while the clock is running.

CLK ON — Depressing the CLocK ON Switch, followed by depressing START, causes the system clock to run. The clock may be stopped by releasing the CLocK ON Switch, or on an address match when STOP CLocK is depressed.

SNGL CLK — If the clock is off, depressing the SiNGLe CLocK Switch generates a single clock pulse, to execute one micro-instruction at a time.

START — Depressing the START Switch permits the clock to start running if CLK ON is depressed. The first micro-instruction to be executed is the instruction currently in the ROM data register.

INH ADRS — Depressing the INHibit ADdReSs Switch stops the ROM address register clock when the Data Switches match the ROM address. Note that the Processor clock is still running and ROM readouts are still strobed into the ROM DATA register even though the ROM address register clock is stopped. This micro-instruction will be executed repeatedly.

STOP CLK — Depressing the STOP CLocK Switch enables a continuous match between the ROM address register and the 12 least significant bits of the Data Switches. The Processor clock is stopped when a match is detected.

RD INS — Operation of the ReaD INStruction momentary Switch causes the contents of the Data Switches to be loaded into the ROM DATA Register. This may be observed on the ROM DATA lamps. The switch is disabled when the clock is running, i.e. CLK ON depressed.

Data Switches — These 16 Data Switches, across the bottom of the panel, are used to perform a dual function:

1. The data set into these switches is inserted into the ROM DATA Register when RD INS is depressed with the clock stopped.

- or -

2. The right-most 12 bits may be used as a constant to match against the ROM address register.

3.2 Indicators

The indicators light when the associated bit or flip-flop is set.

ROM DATA — The 16 ROM DATA lamps indicate the contents of the last address read from the ROM.

BANK — Indicates the state of the Bank flip-flop in Models 3, 4, or 5 Digital Systems. Not used with the Model 2.

OFF NORMAL — Indicates that at least one of the following switches are depressed: MEM, SNGL, PPF, or ATN.

MATCH — Indicates a match condition between the 12-bit ROM Address Register and Data Switches.

RAH — These lamps monitor the 4 most significant bits of the second rank of the ROM Address Register.

RAL — These lamps monitor the 8 least significant bits of ROM Address Register. Ordinarily, these lamps display the address of the next instruction to be executed.

S BUS — Indicates the contents of the S Bus. For the Models 2 and 3, only the right-most 8 bits are applicable. For Models 4 and 5, all bits are used.

DFR/IR — For the Models 2 and 3, the right-most 8 bits display the contents of DFR. For the Models 4 and 5, the right-most 4 bits display the contents of the Flag Register; C, V, G, and L. The next 4 bits display the state of the Counter Register.

The remaining 8 bits in this row of lamps are used for Models 4 and 5 Systems only. Eight flip-flops are displayed as indicated on the display panel.

AR — Indicates the contents of the AR. For the Model 2 and 3, only the right-most 8 bits are applicable. For the Models 4 and 5, all 16 bits are used.

4. OPERATING PROCEDURES

The following procedures assume that an X-Ray ROM is used in conjunction with the Test Set.

4.1 Initial Start-Up

1. Connect the Systems Test Set as outlined in Section 2.
2. Before power is applied to the system, carefully remove the ROM mother-board and substitute the X-Ray ROM.
3. Slide the Display Controller mother-board out of the card file far enough to disconnect the back panel connectors. It is not necessary to remove the cables from the front of the Display Controller.
4. Release all switches on the Test Set except CLK ON. Depress CLK ON.

5. Turn the Digital System power on.

6. Depress the momentary START Switch. This starts the X-Ray running.

4.2 ROM Program Execution

The ROM program may be started at any address by using the following procedure to load the starting address of the ROM subroutine into the ROM Address Register.

1. Release the CLK ON Switch to stop the system clock.

2. Depress INIT to initialize the system.

3. Insert X'5D' (Load RAH) on Data Switches 0 through 7.

4. Set Data Switches 8 through 15 to the desired RAH address.

5. Depress the RD INS pushbutton and the SNGL CLK pushbutton to load the RAH Master Register.

6. Insert X'5E' (Load RAL) on Data Switches 0 through 7.

7. Set Data Switches 8 through 15 to the desired RAL address.

8. Depress the RD INS pushbutton and the SNGL CLK pushbutton to load the RAL Register and the RAH Slave Register. The starting address is now displayed on the RAH and RAL indicators.

9. Depress SNGL CLK. The system fetches the micro-instruction at the selected address and executes that instruction.

The system may be stepped through each micro-instruction by continuing to depress SNGL CLK, or CLK ON may be depressed to run the micro-program at normal speed.

4.3 Address Match

The System Test Set permits halting the system in either of two modes when the micro-program reaches a designated address. If an address is selected and STOP CLK is depressed, the system executes the instruction at the selected address, and then fetches the next instruction, but does not execute it. If, instead of STOP CLK, INH ADRS is depressed, the ROM Address Register is frozen at the selected address and the instruction at that address is executed repeatedly. Use the following procedure for address matching:

1. Set the desired match address on the Data Switches.

   NOTE

   Do not select an address at which the ROM micro-instruction is a Load RAL or an executed Branch.

2. Depress STOP CLK or INH ADRS depending upon the mode of the operation desired.

3. Resume operation after a match by simply releasing INH ADRS, or by releasing STOP CLK and depressing START.

4.4 X-Ray Control

When running the X-Ray ROM program, it is often desirable to have the program continuously loop through certain tests, or to loop through all X-Rays and only stop on errors. This is accomplished by using the PPF, ATN, and SNGL Switches as sense switches which are interrogated by the X-Ray program after a set of tests. The function of each switch is:

1. SNGL - When SNGL is released, the X-Ray continuously loops through the Processor X-Rays and the Memory X-Ray.

When SNGL is depressed, the X-Ray ROM loops in the Wait loop after each set of tests.

2. ATN - When ATN is depressed, the X-Ray loops in one set of tests. The operator selects the particular set of tests by stepping the system through the X-Rays with the EXECUTE pushbutton. Just prior to executing the test to be repeated, the ATN pushbutton is depressed.

3. PPF - If the PPF Switch is depressed, the micro-program loops in the Wait loop if the X-Ray detects an error. The AR indicators also display an error pointer code at this time. An error pointer code dictionary is provided in the Model 4 X-Ray ROM Instruction Manual, Publication Number 29-058.

If the program is looping in the Wait loop as a result of the PPF and/or SNGL Switches, the program may be continued by depressing the EXECUTE pushbutton on the Display Panel twice.

The previous descriptions of the SNGL, ATN, and PPF Switch operation are applicable for the Model 3 X-Rays (START 0 through START 6), and for the Memory X-Ray (START 10). The START 7 X-Ray tests the Primary Power Fail circuit and the False Sync logic. During START 7, the SNGL, ATN, and PPF Switches have a different significance. To begin execution of the START 7 X-Ray, depress PPF and then INIT. If the SNGL Switch is depressed, the program loops at the end of the test (though not in the Wait loop). If the SNGL Switch is released, the micro-program continuously repeats START 7.

4.5 Core Memory Marginal Test

Use the following procedure to determine the core memory threshold margins:

1. Continuously loop through the START 10 X-Ray with the PPF Switch depressed to assure that no errors are detected.

2. Connect a voltmeter between ground and the VT testpoint on the Digital System back panel (pin 211-1 of MEM0 or MEM1).

3. Set the MEM VOLT potentiometer to its mid position and depress the MEM Switch.

4. Vary the MEM VOLT potentiometer to obtain readings from 3 volts to 5 volts. If the Memory X-Ray fails between these limits, the memory requires adjustment or repair. Refer to the Memory Section of the Digital System Maintenance Manual.

4.6 System Clock Marginal Test

If a trouble exists in the system, and it is suspected that the problem is related to speed, the variable clock on the System Test Set may be used as an aid to isolate the problem.

Use the following procedure to employ this feature.

1. Monitor the CD0 test point on the Digital System back panel with an oscilloscope.

2. Start the X-Ray running through all Processor tests, SNGL and ATN Switches released, PPF Switch depressed.

3. Release CLK ON, and PPF.

4. Turn the EXT CLK potentiometer fully counter-clockwise.

5. Operate the EXT, CLK ON, INIT, and PPF Switches.

When START is operated, the X-Ray program runs with the EXT clock at its slowest speed. If the program runs at this speed, increase the clock speed in discrete steps until a failure occurs. Five or ten seconds should be allowed between each setting to insure that the X-Ray completes at least one cycle.

NOTE

The clock in the Test Set is variable over a wide range and can be adjusted to be much faster than the computer crystal frequency. The crystal frequency should not be exceeded by more than 10% when running this test. The X-Rays should normally be run with the EXT Switch released.

5. FUNCTIONAL DESCRIPTION

The following description refers to the ten sheet System Test Set schematic provided at the rear of this manual.

Sheet 1 of the schematic shows the A Section of each of the Data/Address switches on the bottom of the System Test Set panel, and the interconnection of the switches to the Processor back panel. As shown on Figure 1 earlier in this manual, J1 and J2 are on the rear of the System Test Set. Connections P1 and P2 are on the cable assemblies, while the diodes shown enclosed within dotted lines are mounted on the connectors which mate with the back panel (RMI-0 and RMI-1). Note the momentary (non-latching) Read Instruction switch contacts shown in the lower left area of Sheet 1. When RD INS Switch is depressed, the condition of switches S00 through S15 is gated into the ROM Data Register.

Sheet 2 of the schematic shows the ROM DATA lamps on the System Test Set Control Panel, and the gates which drive them. Note that there is not gating envolved. Thus, the ROM DATA lamps continuously display the contents of the RD Register in the Digital System.

Sheet 3 shows the least significant 8 bits of the AR display and the S Bus display. Sheet 4 shows the most significant 8 bits of these displays, which are required only with Model 4 and 5 Digital Systems.

Sheet 5 shows part of the cable which is used with the Models 4 and 5. The sheet provides the Instruction Register display in such systems. Note the output from area R9 of this sheet to 6R9. This ground inhibits the inputs shown on the top right of Sheet 6.

The left half of Sheet 6 shows the RAH display logic. The four outputs to Sheet 8 are high when the RAH bit matches the corresponding S4 through S7 switch condition. For example, if S4 is depressed and RAH04 is set, the MRAH041 signal is high. The right half of Sheet 6 shows the DFR display logic if the Digital System is a Model 2 or a Model 3 (see the preceding paragraph if the Digital System is a Model 4 or 5).

Sheet 7 shows the RAL display logic. Note that outputs to the address match logic on Sheet 8 are similar to those shown on Sheet 6 and described earlier in this Section.

The ROM address match logic is shown on the left side of Sheet 8. When the ROM address matches the configuration set in Switches 4 through 15, the output from the gate shown in area C5 goes high. This output is applied to four gates shown in area C6 through C9. Going from the top to bottom, the first gate lights the MATCH indicator on the Control Panel. If the INH ADRS Switch on the Control Panel is set, the next gate sends a signal to the Processor to inhibit incrementing the ROM address. If the STOP CLK Switch on the Control Panel is set, the output from the next gate stops the System Test Set clock (Sheet 9). The last gate provides an output to the ADD MATCH jack on the rear of the System Test Set. This output is typically used to trigger an oscilloscope at a selected ROM address.

The logic shown in the H and J area of Sheet 8 provides the Digital System clock to the CLOCK jack on the rear of the System Test Set, and to the Stop Clock gate discussed in the preceding paragraph. The PPF, ATN, and SNGL Switches are shown in areas L6 and M6. Note that in addition to supplying signals to the Processor, these three switches and the MEM Switch are ORed to light the OFF NORMAL indicator. The final circuit on Sheet 8 lights the BANK indicator when the Bank flip-flop in the Model 3, 4, or 5 Processor is set.

Sheet 9 of the schematic shows the System Test Set clock and control logic. Assume first that the normal Processor internal clock is being used. In this case, the CLK ON Switch,shown in area G6, is depressed to remove the ground from IC05-10 (area C7). The CLKOFF0 signal is then forced high via gates at B7 and C2 when the START Switch at E7 is depressed. The Processor clock runs normally until a STP0 signal is received on an ROM address match, or until the CLK ON Switch is released.

If the External (System Test Set) clock is used, the EXT Switch,shown in area A8, is depressed. The normally-open contacts close to generate a CLKOFF0 signal which stops the Processor clock until EXT is released. The normally-closed contacts release the flip-flop shown in area C9. When CLK ON is depressed, followed by START, the flip-flop is set. The high output from the flip-flop enables the gate shown in area F9. The other input to the gate is the output from the external clock multivibrator circuit which is shown in the lower right area of Sheet 9. The output from the gate in area F9 generates the EXTCLK0 signal to the Processor via gates shown in areas G2 and H2. The clock continues to run at the frequency selected by the EXT CLK potentiometer shown in area M6, until the flip-flop shown in area C9 is reset. The flip-flop may be reset one of three ways: by SCLR1 from the Processor, by STP0 from Sheet 8, or by the CLK ON Switch (shown in area E6) being released. Note the SNGL CLK Switch shown in area H7. If the CLK ON Switch is released, the flip-flop shown in areas G8 and H8 is set each time the SNGL CLK Switch is depressed. The flip-flop output produces a clock pulse each time SNGL CLK is depressed.

The Initialize Switch, shown in area H6, produces a POW0 signal to the Processor each time it is depressed. The MEM VOLT potentiometer selects a memory threshold voltage which is applied to the Processor if the MEM Switch is depressed and the clip lead is installed.

6. MAINTENANCE

Maintenance on the System Test Set itself is normally restricted to the periodic replacement of indicator lamps. The lamps slip straight out from the front. It is normally possible to remove the lamp by hand. The replacement lamp, INTERDATA Part Number 33-011 or Sylvania Part Number 12ESB, is simply pushed into place by hand.

If a trouble is encountered in the System Test Set, use the Functional Description provided in Section 5 and Functional Schematic 28-001B08 to locate the malfunction.

INTERDATA

SHEET INDEX

CONTENTS	SHEET NO.	SHEET REVISION 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A			—	4	5	6	7													
SYSTEM TEST SET	1			3	3	3	3	3													
	2			3	3	5	5	5													
	3			3	3	3	3	3													
	4			3	3	3	3	3													
	5			3	3	3	3	3													
	6			3	3	3	3	3													
	7			3	3	3	3	3													
	8			3	3	3	6	6													
	9			3	3	3	6	6													
CONNECTOR ASSIGNMENT	10			3	4	4	4	7													
REVISION DATE				3-19-69	10-3-69	10-21-69	12-10-69	2-27-70	9-21-70												

SUPPORTING INFORMATION

CATEGORY	PART NO.
SYSTEM TEST SET	28-001 R10 B01 28-001 R01 B01 28-002 R02 B01

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REVISION OF SHEETS AFFECTED.

2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST REVISION OF THIS DRAWING.

NOTES

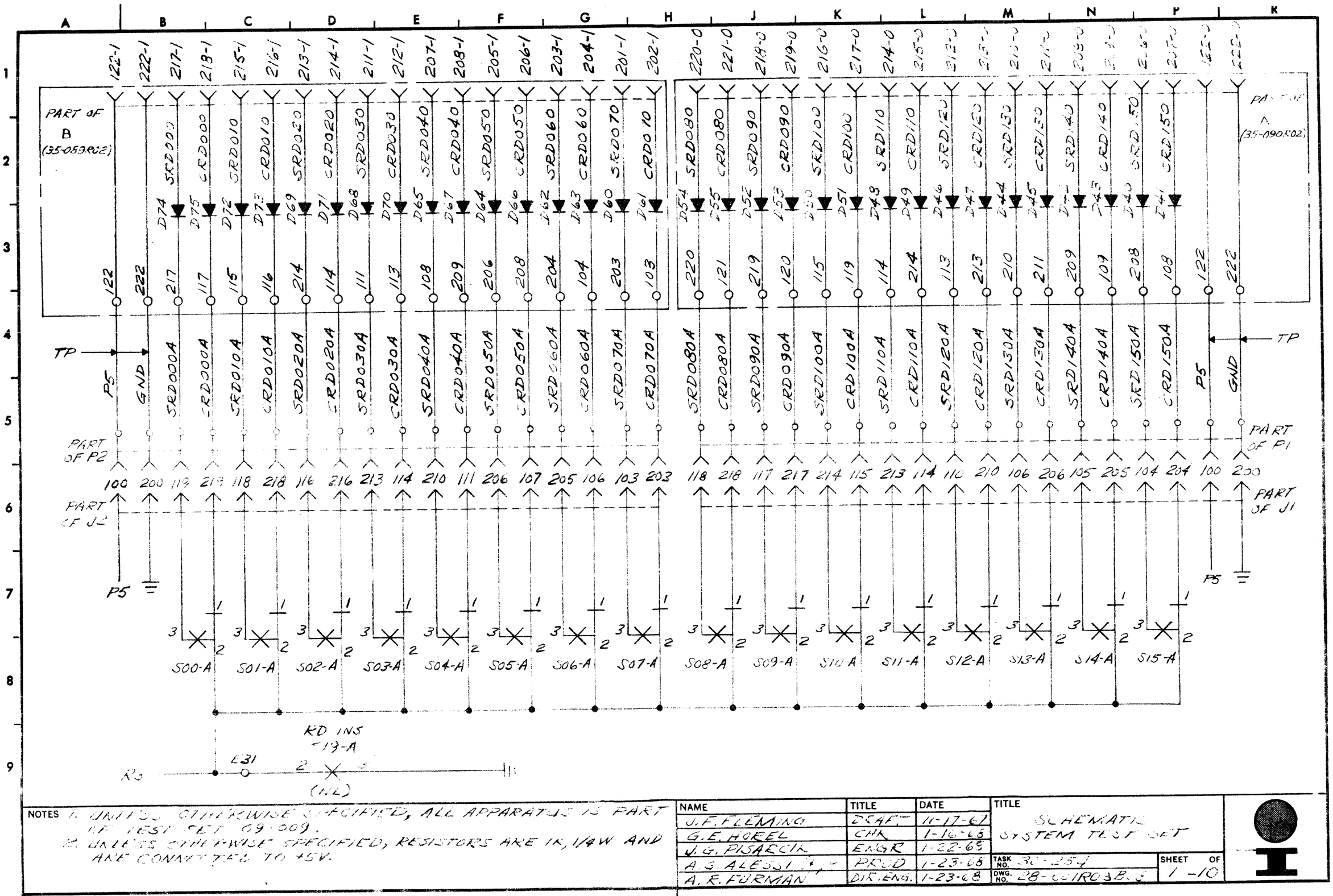
NAME	TITLE	DATE
J. F. FLEMING	DRAFT	11-17-67
G. E. HOREL	CHECK	1-16-68
J. G. PISARCIK	ENGR	1-22-68
A. G. ALESSI	PROD	1-23-68
A. R. FURMAN	DIR. ENGR.	1-23-68

TITLE FUNCTIONAL SCHEMATIC
SYSTEM TEST SET

TASK NO

DWG NO 28-001 R07 B08

SHEET CA-11 OF



NOTES
1. UNLESS OTHERWISE SPECIFIED, ALL APPARATUS IS PART OF TEST SET 09-009.
2. UNLESS OTHERWISE SPECIFIED, RESISTORS ARE 1K, 1/4W AND ARE CONNECTED TO +5V.

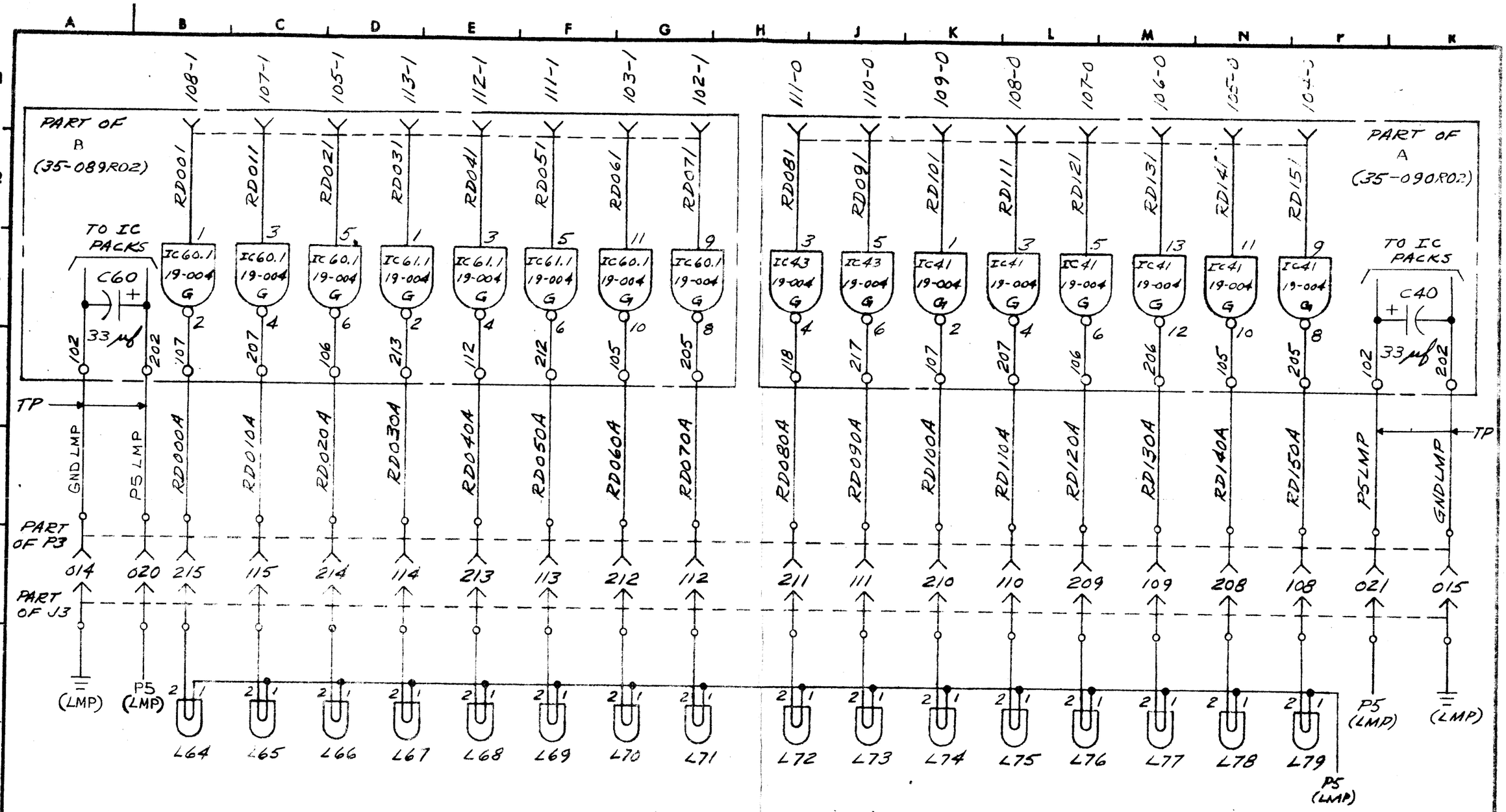
NAME	TITLE	DATE
J.F. FLEMING	DRAFT	11-17-67
G.E. HOREL	CHK	1-16-68
J.G. PISARCIK	ENGR	1-22-68
A.G. ALESSI	PROD	1-23-68
A.R. FURMAN	DIR. ENG.	1-23-68

TITLE: SCHEMATIC SYSTEM TEST SET

TASK NO. [illegible]-254 | SHEET OF 1-10

DWG. NO. 28-C0IR03B.S

EUGENE DIETZGEN CO. 196-H 20003



NOTES

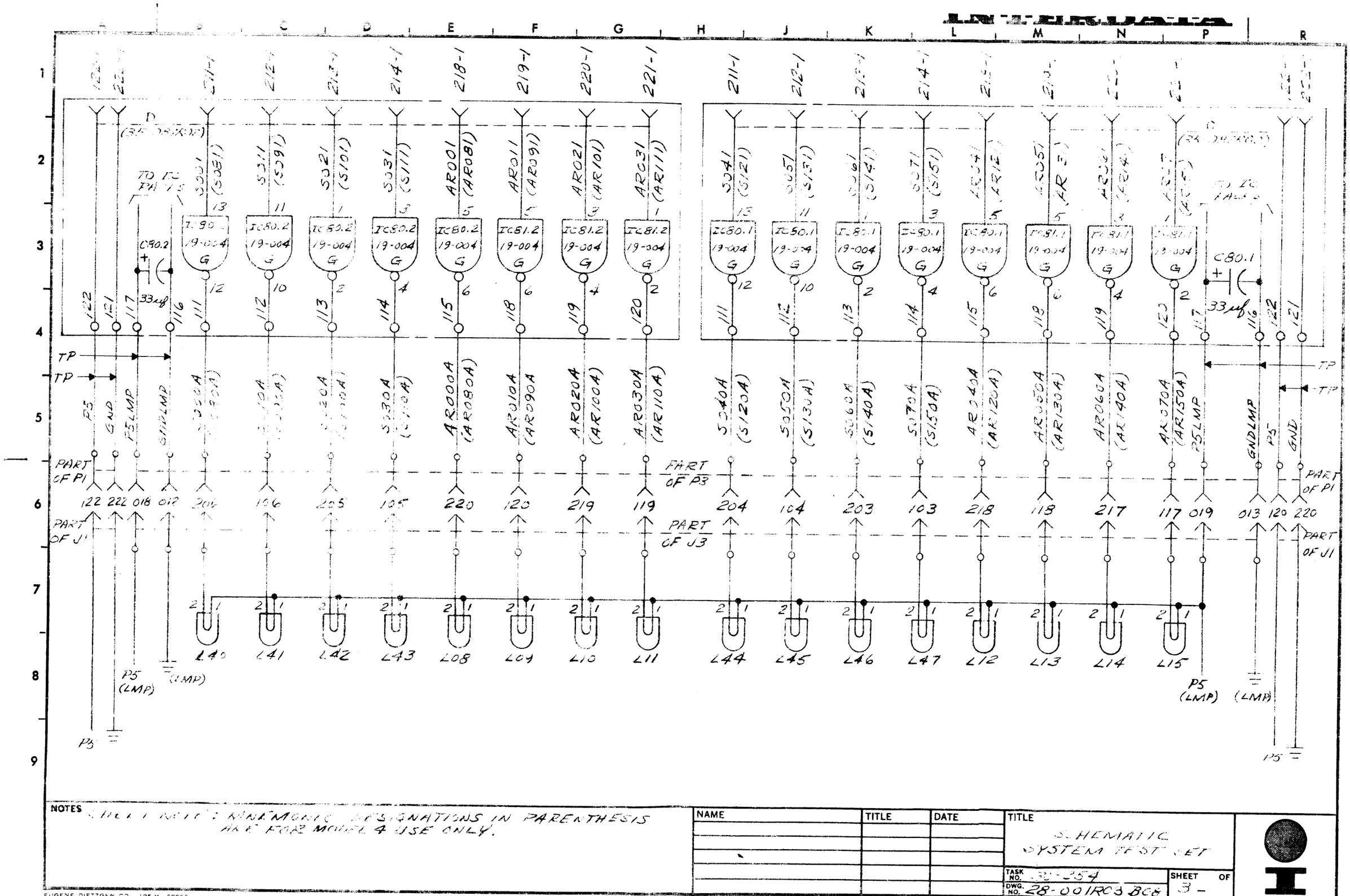
NAME	TITLE	DATE

TITLE: SCHEMATIC SYSTEM TEST SET

TASK NO. 30-254

DWG. NO. 29-001R05 B08

SHEET OF 2-



NOTES: SIGNAL NAME MNEMONIC DESIGNATIONS IN PARENTHESIS ARE FOR MODEL 4 USE ONLY.

NAME	TITLE	DATE

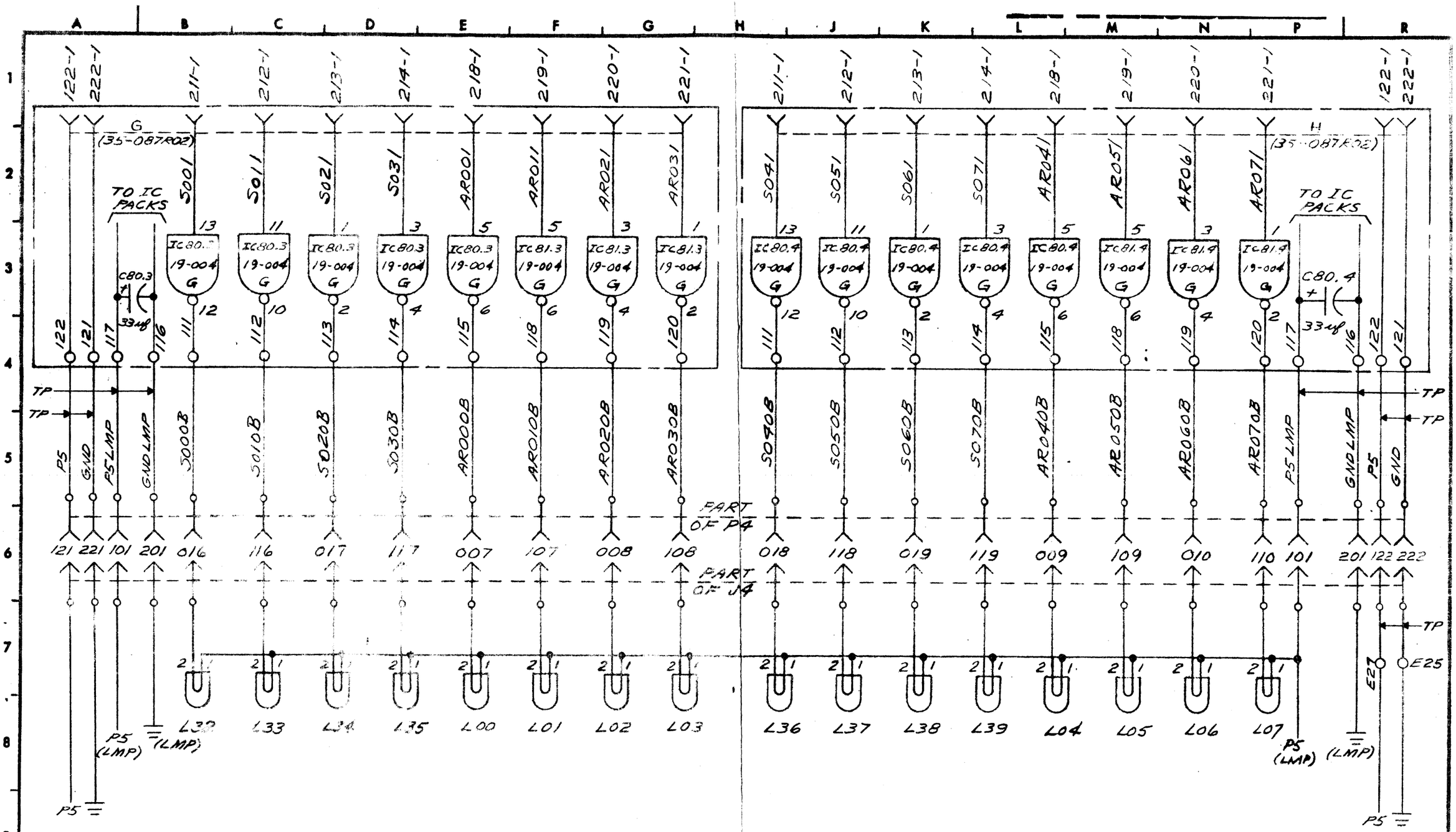
TITLE: SCHEMATIC SYSTEM TEST SET

TASK NO. 32-254

DWG. NO. 28-001RC3 BCE

SHEET 3 OF

EUGENE DIETZGEN CO 196-H 20003



NOTES SHEET NOTE: ALL APPARATUS IS FOR MODEL 4 USE ONLY.

NAME	TITLE	DATE

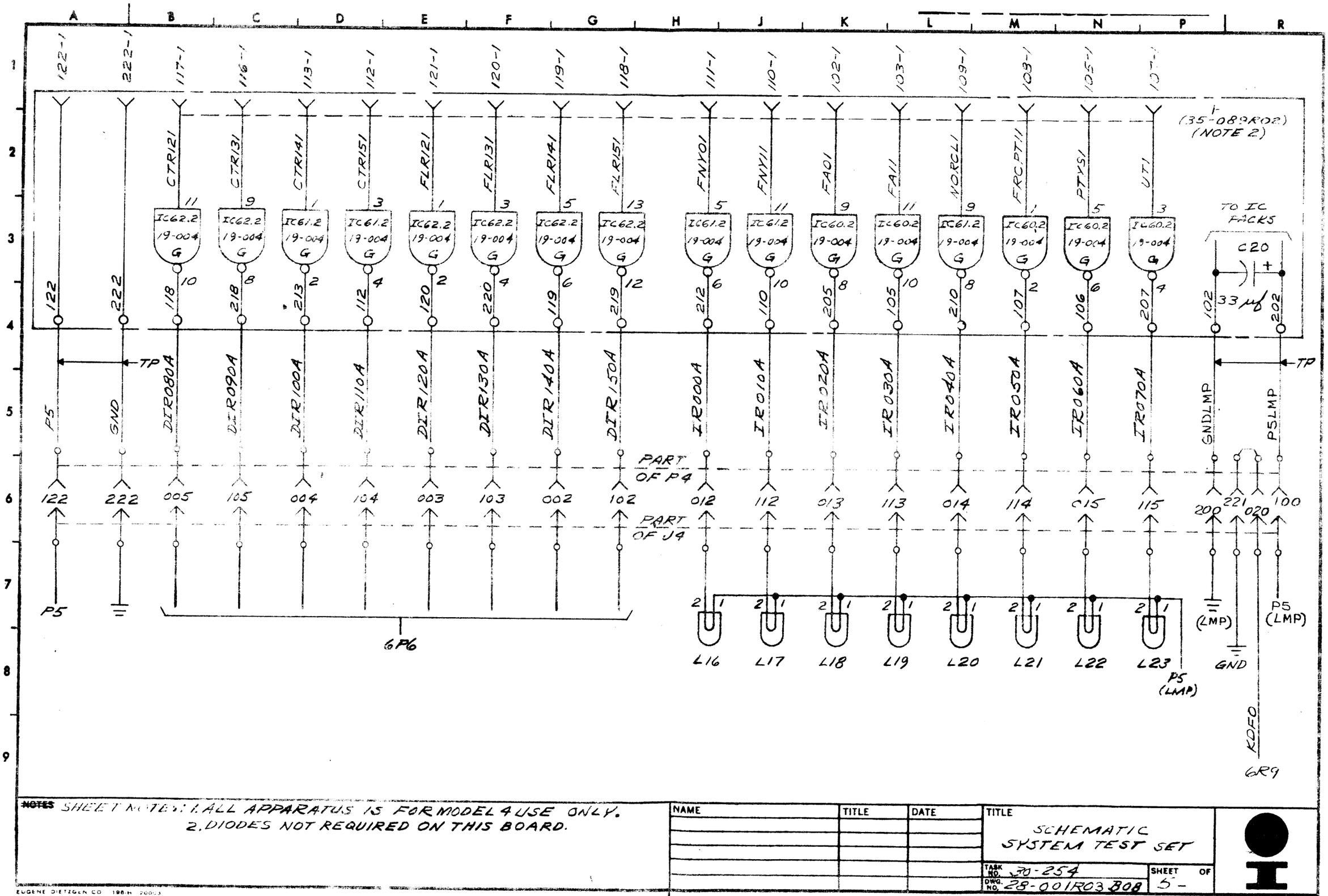
TITLE: SCHEMATIC SYSTEM TEST SET

TASK NO. JU-254

DWG. NO. 28-001R03308

SHEET 4 OF -

EUGENE DIETZGEN CO 196-H 20003



NOTES SHEET NOTES: 1. ALL APPARATUS IS FOR MODEL 4 USE ONLY.
2. DIODES NOT REQUIRED ON THIS BOARD.

NAME	TITLE	DATE

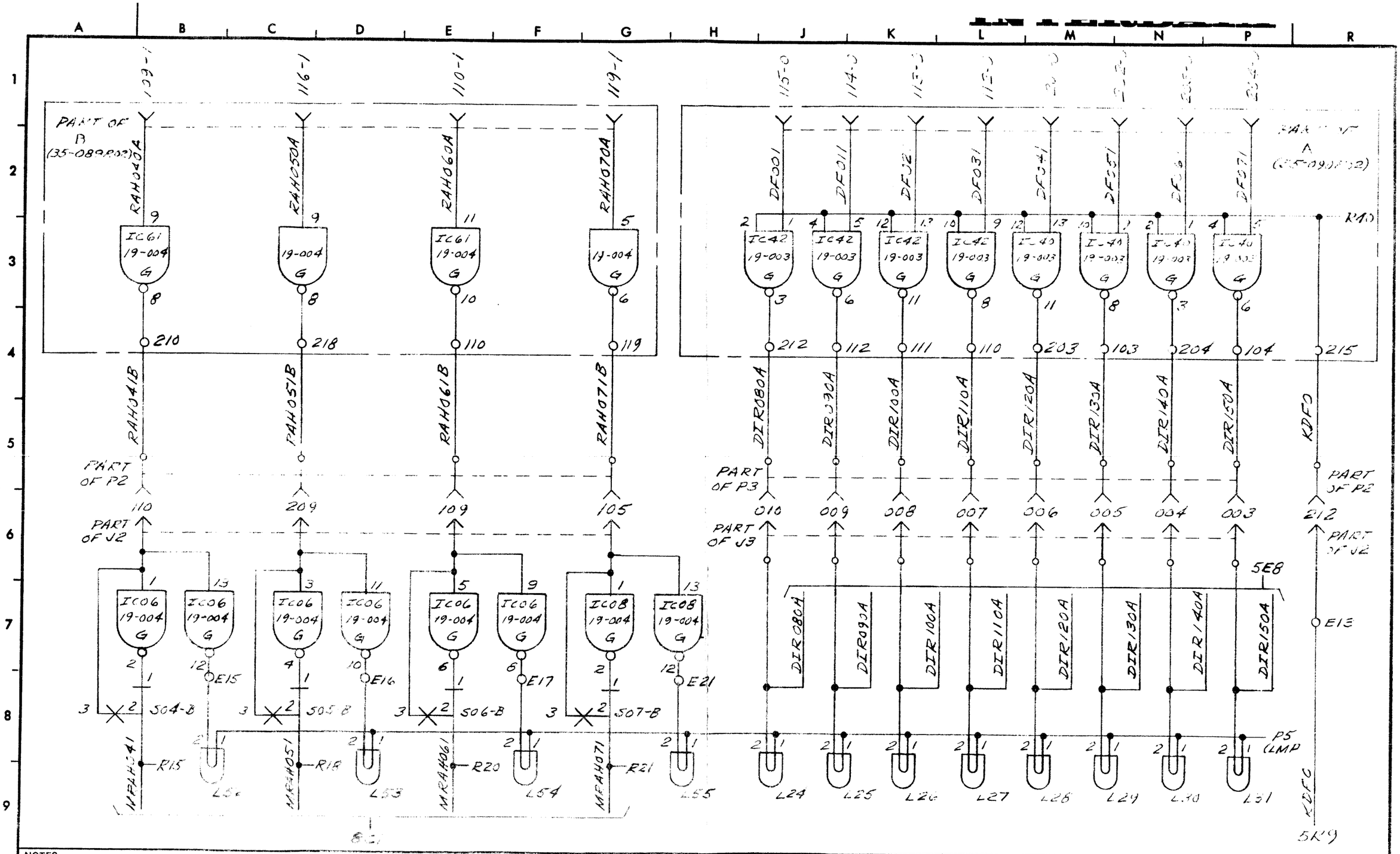
TITLE: SCHEMATIC SYSTEM TEST SET

TASK NO. 70-254

DWG. NO. 28-001R03 B08

SHEET 5 OF

EUGENE DIETZGEN CO. 186-H 20003



NOTES

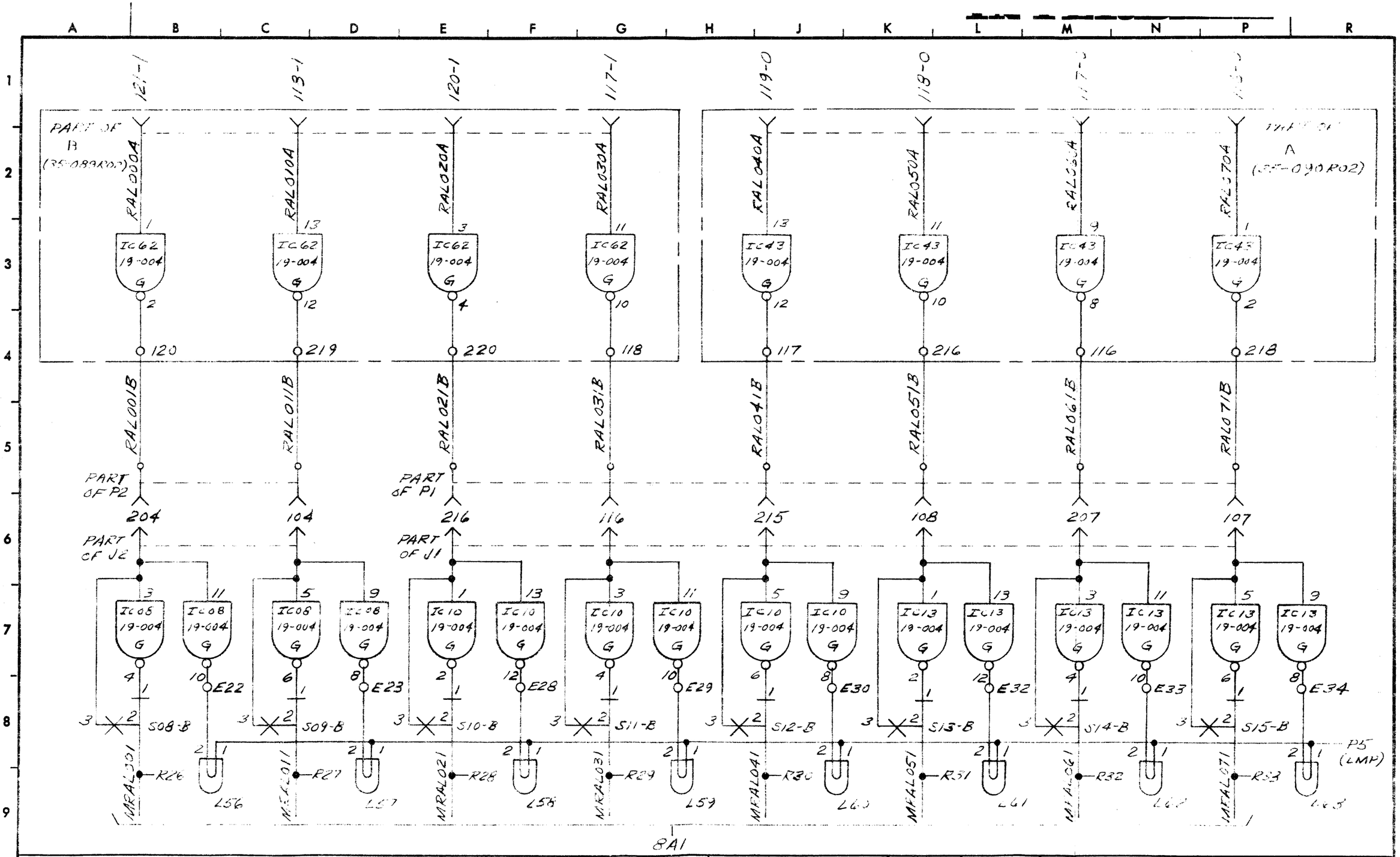
NAME	TITLE	DATE

TITLE: SCHEMATIC SYSTEM TEST SET

TASK NO. 30-254

DWG. NO. 25-001R03 Rev B

SHEET 6 OF -



NOTES

NAME	TITLE	DATE

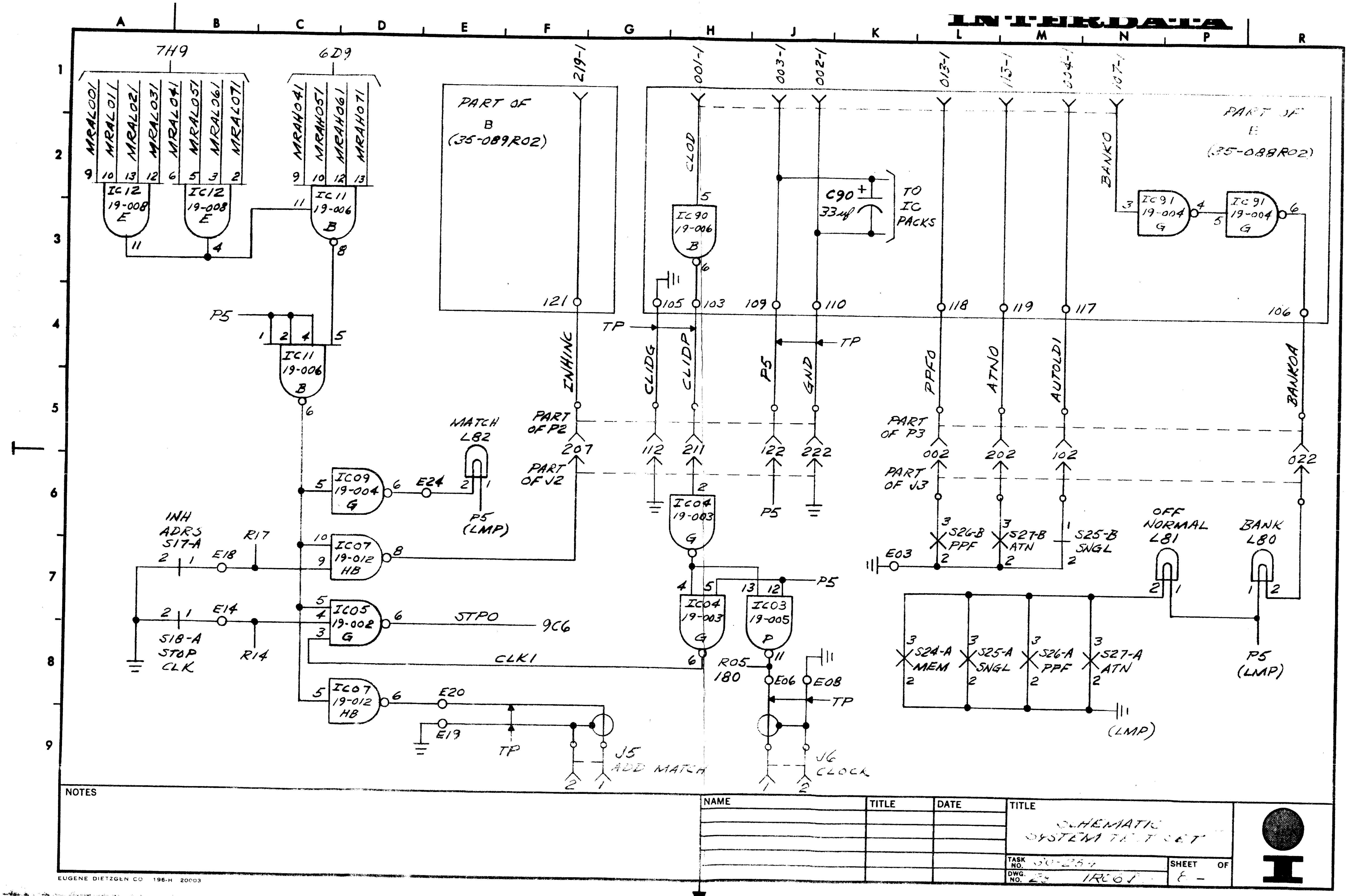
TITLE

TASK NO.

DWG. NO.

SHEET OF

EUGENE DIETZGEN CO 196-H 20003


INTERDATA
PART OF B (35-089R02)
PART OF B (35-088R02)
7H9
6D9
MRAL001 MRAL011 MRAL021 MRAL031 MRAL041 MRAL051 MRAL061 MRAL071
MRAH041 MRAH051 MRAH061 MRAH071
IC12 19-008 E
IC11 19-006 B
IC90 19-006 B
IC91 19-004 G
C90 33µf
TO IC PACKS
CLOD
BANKO
INHINC
CLIDG
CLIDP
P5
GND
PPFO
ATNO
AUTOLDI
BANKOA
TP
PART OF P2
PART OF J2
PART OF P3
PART OF J3
MATCH L82
P5 (LMP)
IC09 19-004 G
IC07 19-012 HB
IC05 19-002 G
IC04 19-003 G
IC03 19-005 P
INH ADRS S17-A
STOP CLK S18-A
R17
R14
E18
E14
E24
E20
E19
E03
E06
E08
R05 180
STPO
9C6
CLK1
S26-B PPF
S27-B ATN
S25-B SNGL
OFF NORMAL L81
BANK L80
S24-A MEM
S25-A SNGL
S26-A PPF
S27-A ATN
(LMP)
J5 ADD MATCH
J6 CLOCK
NOTES
NAME
TITLE
DATE
TITLE
SCHEMATIC SYSTEM TEST SET
TASK NO.
DWG. NO.
SHEET
OF
EUGENE DIETZGEN CO 196-H 20003

INTERDATA

A B C D E F G H J K L M N P R

120-0 110-1 109-1 014-1

PART OF A (35-090R02)

PART OF E (35-088R02)

CLKOFFO

EXTCLKO

POWO

IC91 19-004 G

IC91 19-004 G

IC91 19-004 G

R90 470

D90

C91 470pf

R92

221 108 110 105 107 116

TP TP

SCLRI CLKOFIP CLKOFIG EXCLKOG EXCLKOP POWOA

PART OF P2

PART OF P3

214 115 215 112 217 001

PART OF J2

PART OF J3

POWER SUPPLY

119-0200 TB4-2 TB5-3 TB5-6

CLIP LEAD TO MEM

VT P15 P5LMP GNDLMP TP

000 101 122 222

8F7

STPO

R13 R12

S16-A START (NL)

S22-B CLK ON

S20-A INIT (NL)

S23-A SNGL CLK (NL)

S21-A EXT

IC09 19-004 G

IC03 19-005 P

IC05 19-002 G

IC04 19-003 G

IC02 19-007

IC01 19-005 P

IC01 19-005 P

IC04 19-003 G

IC09 19-004 G

R09 R10 470 R07 R06 470

E09 E10 E08 E12 E17 E19 E02 E01 E11 R02 R01 R11

EXTCLKG EXTCLKP

E25 E26 E27

R25 1K C4 100pf C6 100pf R24 220

C5 100pf R22 470 R23 1K

Q1 2N3646 Q2 2N3646

R39 20K CW EXT CLK

R38 1K CW MEM VOLT MT2 MT1

S24-B MEM

E05 E04

R04 220

C2 2.2μf C7 2.2μf

D1 6.2V D2 6.2V

P5 P5 (LMP) (LMP)

NOTES

NAME	TITLE	DATE

TITLE: SCHEMATIC SYSTEM TEST SET

TASK NO. 30-254

DWG. NO. 28-001R06 E08

SHEET 9 OF -

EUGENE DIETZGEN CO. 196-H 20003

CONNECTOR ASSIGNMENT FOR SYSTEM TEST SET

CABLE	CONNECTOR BOARD		COMPUTER LOCATION								
	TYPE	DESIG.	MODEL 2	MODEL 3 (WIREWRAP)	MODEL 3 (COPPER)	MODEL 4	MODEL 4 (COPPER)	MODEL 5 (COPPER)	MODEL 5 16KB	MODEL 3M	MODEL 4M -MODEL 5M
17-035	35-089	B	09-1	11-1	10-1	10-1	10-1	10-1	16-1	11-1	11-1
	35-090	A	09-0	11-0	10-0	10-0	10-0	10-0	16-0	11-0	11-0
	35-087	C	10-1	13-1	11-1	18-1	15-1	15-1	21-1	13-1	16-1
	35-087	D	11-1	15-1	12-1	17-1	14-1	14-1	20-1	12-1	15-1
	35-088	E	13-1	19-1	14-1	13-1	11-1	11-1	17-1	15-1	12-1
17-038	35-087	G	—	—	—	15-1	12-1	12-1	19-1	—	14-1
	35-087	H	—	—	—	16-1	13-1	13-1	18-1	—	13-1
	35-089	F	—	—	—	19-1	16-1	16-1	22-1	—	17-1

NOTES

NAME	TITLE	DATE	TITLE
J. RANDOLPH	DRAFT	9-21-70	SCHEMATIC SYSTEM TEST SET
			TASK NO. 30254
			DWG. NO. [illegible]
			SHEET OF 16

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BACK PANEL PIN INDEX

MNEM.	SCHEMATIC LOCATION ROM	ALU	MEM CONT.	I/O
ACKA00	—	—	—	20N6
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B020	—	11S2	29M4	—
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B060	—	11S4	29D8	—
B070	—	11S4	29E8	—
B080	—	11S6	29F8	20B6
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D010	—	16C6	—	—
D020	—	16C6	—	—
D030	—	16D6	—	—
D040	—	16E6	—	—
D050	—	16F6	—	—
D060	—	16G6	—	—
D070	—	16H6	—	—
D080	—	—	—	20B6
D090	—	—	—	20C6
D100	—	—	—	20D6
D110	—	—	—	20E6
D120	—	—	—	20F6
D130	—	—	—	20G6
D140	—	—	—	20H6
D150	—	—	—	20H6
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DA0	—	—	—	20M6
DCAK0	—	—	—	20L6
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FMDUA1	9D1	—	30K1	—
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FRNS1	—	14S7	—	17R5
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GB000	—	14A4	—	17G1
GDEST1	8H4	10J1	—	—
GTP20	9F1	—	—	—
HIDUA0	8A1	—	—	—
HDEST0	8D9	15L1	—	—
HW0	9K1	—	—	—

MNEM.	SCHEMATIC LOCATION ROM	ALU	MEM CONT	I/O
INH0	—	—	30C9	—
INHINC0	5R2	—	—	—
INTA0	4N1	—	—	17S9
IR001	4A5	—	28B5	—
IR011	4B5	—	28D5	—
IR021	4B5	—	28F5	—
IR031	4B5	—	28G5	—
IR041	4B5	—	28J5	—
IR051	4C5	—	28L5	—
IR061	4C5	—	28M5	—
IR071	4C5	—	28R5	—
IR080	—	10L1	28B9	—
IR090	—	10M1	28D9	—
IR100	—	10E4	28E9	—
IR110	—	10R4	28G9	—
IR120	—	10L1	28J9	—
IR130	—	10M1	28K9	—
IR140	—	10F4	28M9	—
IR150	—	10S4	28R9	—
JACC0	9L4	—	—	17C5
KILDST0	4N5	13N9	—	19M5
KSKIP0	9F9	—	—	18J5
LAR1	8F9	12A1	—	—
LARYS0	9C4	10B1	—	—
LCC0	9M4	—	—	17C5
LD100	8S4	—	—	20L1
LD101	—	16B6	—	20K6
LDCTR0	8C9	—	27B1	—
LFLR0	8D9	—	—	17S1
LINE1	4C5	—	—	20R1
LIR0	8D9	—	28S1	—
LMAR0	8G9	—	25B1	—
LMDR1	4J1	—	26B1	—
LOAD1	8N4	12B6	—	—
LPSW1	8H9	—	29C1	17S1
LRAH0	5K1	—	—	18C9
LRAL0	5R2	—	—	18K9
LR0	—	—	30E9	—
LSRL0	8D9	15N1	—	—
MA000	—	—	25A9	—
MA001	—	—	25A9	—
MA010	—	—	25B9	—
MA011	—	—	25B9	—
MA020	—	—	25C9	—
MA021	—	—	25C9	—
MA030	—	—	25D9	—
MA040	—	—	25E9	—
MA050	—	—	25F9	—
MA060	—	—	25F9	—
MA070	—	—	25H9	—
MA080	—	—	25H9	—
MA090	—	—	25J9	—
MA100	—	—	25K9	—
MA110	—	—	25L9	—
MA120	—	—	25M9	—
MA130	—	—	25N9	—
MA140	—	—	25R9	—
MAR150	9S5	—	25S9	—
MCLR1	—	—	30A1	—
MD000	—	—	26C5	—
MD010	—	—	26E5	—
MD020	—	—	26F5	—
MD030	—	—	26H5	—
MD040	—	—	26K5	—
MD050	—	—	26L5	—
MD060	—	—	26N5	—
MD070	—	—	26S5	—
MD080	—	—	26D9	—
MD090	—	—	26E9	—
MD100	—	—	26F9	—
MD110	—	—	26H9	—
MD120	—	—	26K9	—
MD130	—	—	26L9	—
MD140	—	—	26N9	—
MD150	—	—	26S9	—
MD160	—	—	27K4	—
MS000	—	—	26D1	—
MS010	—	—	26E1	—
MS020	—	—	26G1	—
MS030	—	—	26J1	—
JOE 1	9G5	—	27L9	—

MNEM	SCHEMATIC LOCATION ROM	ALU	MEM CONT	I/O
MS040	—	—	26K1	—
MS050	—	—	26M1	—
MS060	—	—	26R1	—
MS070	—	—	26S1	—
MS080	—	—	26D5	—
MS090	—	—	26E5	—
MS100	—	—	26G5	—
MS110	—	—	26J5	—
MS120	—	—	26K5	—
MS130	—	—	26M5	—
MS140	—	—	26N5	—
MS150	—	—	26S5	—
MS160	—	—	27J1	—
MSK1	—	—	29R8	18L1
NOMEM0	8A9	—	30R9	—
OP1	4L9	—	—	18L1
P00	9K4	—	30S1	—
P21	9F4	—	—	18N6
PAR0	—	—	27J5	—
PC00	9E4	—	—	17M6
PC10	9F4	—	—	—
PFF1	—	—	27H9	17L6
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PSW021	—	—	29M1	17K6
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PSW071	—	—	29E4	—
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RAH050	5E4	—	—	—
RAH060	5F4	—	—	—
RAH070	5G4	—	—	—
RAL080	5A9	—	—	—
RAL090	5B9	—	—	—
RAL100	5C9	—	—	—
RAL110	5D9	—	—	—
RAL120	5E9	—	—	—
RAL130	5F9	—	—	—
RAL140	5G9	—	—	—
RAL150	5H9	—	—	—
RCL0	5K1	—	—	19L9
RD000	8A4	10A1	—	17M1
RD001	8B4	13M1	—	17B1
RD010	8B4	10A1	—	17M1
RD011	8B4	13M1	—	17B1
RD020	8C4	13N1	—	—
RD021	8C4	13N1	—	17M1
RD030	8D4	10A1	—	17N1
RD031	8D4	13N1	—	18C1
RD040	8E4	—	30S9	18D6
RD041	8E4	10J1	—	18L1
RD050	8F4	—	30S9	18D6
RD051	8F4	10J1	—	18K1
RD060	8G4	10G1	—	18D6
RD061	8G4	13N1	—	18K1
RD070	8H4	10G1	—	18D6
RD071	8H4	13R1	—	18J1
RD080	8H4	10C1	—	18B1
RD081	8J4	10A1	—	18F1
RD090	8K4	10C1	29D4	18B1
RD091	8K4	10B1	—	18B1
RD100	8K4	10B1	—	18B1
RD101	8L4	10B1	—	18C1
RD110	8L4	10F1	29C4	18E1
RD111	8L4	10B1	—	18G1
RD120	8M4	—	—	—
RD121	8M4	12B6	—	18M1
RD130	8N4		—	—
RD131	8N4	12C6	—	18N1
RD140	8R4		—	20N1
RD141	8R4	15A2	—	18M1
RD150	8S4		—	20N1
RD151	8S4	13G1	—	18L1
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REQ0	—	—	30L1	—
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S001	—	12E1		17L1
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S011	—	12E1		—
S020	—	11S3	26F1	—
S021	—	12C1	—	—

MNEM.	SCHEMATIC LOCATION ROM	ALU	MEM CONT	I/O
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S031	—	12D1	—	—
S040	—	11S5	26J1	—
S041	—	12E1	—	—
S050	—	11S5	26L1	—
S051	—	12F1	—	—
S060	—	11S5	26N1	—
S061	—	12G1	—	—
S070	—	11S5	26R1	—
S071	—	12H1	—	—
S080	—	11S7	26C5	—
S081	5A5	12J1	—	20B1
S090	—	11S7	26D5	—
S091	5B5	12K1	—	20C1
S100	—	11S7	26F5	—
S101	5C5	12K1	—	20D1
S110	—	11S7	28G5	—
S111	5D5	12L1	—	20E1
S120	—	11S9	28J5	—
S121	5D1	12M1	—	20F1
S130	—	11S9	28K5	—
S131	5E1	12N1	—	20G1
S140	—	11S9	28M5	—
S141	5F1	12R1	—	20H1
S150	—	11S9	28R5	—
S151	5H1	12S1	—	20J1
SCL0	—	13G1	27D1	19J9
SCLR0	—	—	—	19N1
SCLR1A	5C1	12J5	30J9	19R1
SDUAD0	—	—	30K1	—
SHL1	8N9	13C5	—	—
SHOT1	—	13C9	—	17C1
SHR1	8N9	13B5	—	—
SKIP0	9C1	—	—	18J9
SNGL0	—	—	—	18R1
SRD001	8A1	—	—	—
SRD011	8B1	—	—	—
SRD021	8C1	—	—	—
SRD031	8D1	—	—	—
SRD041	8E1	—	—	—
SRD051	8F1	—	—	—
SRD061	8G1	—	—	—
SRD071	8H1	—	—	—
SRD081	8J1	—	—	—
SRD091	8K1	—	—	—
SRD101	8K1	—	—	—
SRD111	8L1	—	—	—
SRD121	8M1	—	—	—
SRD131	8N1	—	—	—
SRD141	8R1	—	—	—
SRD151	8S1	—	—	—
SR0	—	—	—	20R6
SSKIP0	9E9	—	—	18K6
SSMEM1	—	—	30J1	—
STFL0	8R9	—	—	17F1
STF0	8R9	—	—	17N1
STOP0	9B4	—	—	19L5
STFA0	4J5	—	—	19J5
STPC0	—	13R9	—	19L5
SUB1	—	13L4	—	17E1
SVAC0	8S9	13B4	—	17D1
SV0	4F5	—	—	17H1
SYSC0	8S9	13A4	—	17E1
SWTAL0	8L9	—	—	21M5
SYN0	4E1	—	—	23H7
SYSCL1	9A5	10H1	—	19G5
T21	9N5	13L6	—	19K9
T2INS1	—	—	30N9	19K9
TACK0	—	—	—	24A9
UD100	8S4	16A6	—	18C5
UIR41	—	—	28C5	18F5
UMDR1	9R5	—	—	18C5
USRH0	—	16A1	—	18E5
USRL0	—	16A1	—	18D5
USTRB0	—	—	29A4	18C5
UT1	—	12L9	—	18H1
WAIT0	8L9	—	—	21R1
W0	—	—	30B9	—
WRTOA	—	—	27L1	—
X0	9F9	12A6	—	—

F01	AS SHOWN WITH POWER FAIL DETECT CIRCUIT LOCATED ON SHEET 19
F02	AS SHOWN LESS POWER FAIL DETECT CIRCUIT LOCATED ON SHEET 19

MNEM	SCHEMATIC LOCATION ROM	ALU	MEM CONT	I/O
X1	9S9	—	26A1	—
+15	—	—	—	19D1
-15	—	—	—	19J1
12VAC	—	—	—	19A3
12VAC	—	—	—	19A4

CONNECTOR 3 PIN INDEX

MNEM.	SCHEMATIC LOCATION ROM	ALU	MEM CONT	I/O
CWR0	—	—	27R9	—
ESN00	—	—	—	21M2
INIT0	—	—	—	19A4
LA0	—	—	—	21F9
LB0	—	—	—	21F9
LC0	—	—	—	21F9
LD0	—	—	—	21F9
MA001A	—	—	25A7	—
MA011A	—	—	25B7	—
MA021A	—	—	25C7	—
MA031A	—	—	25D7	—
MA041A	—	—	25E7	—
MA051A	—	—	25F7	—
MA061A	—	—	25G7	—
POFF0	—	—	—	19A4
PRTECT0	—	—	27N9	—
SD001	—	—	—	21E6
SD011	—	—	—	21F6
SD021	—	—	—	21F6
SD031	—	—	—	21F6
SD041	—	—	—	21G6
SD051	—	—	—	21H6
SD061	—	—	—	21H6
SD071	—	—	—	21J6
SHI0	—	—	—	21A9
SLO0	—	—	—	21A9
SRG0	—	—	—	21B9
SSGL1	—	—	—	21H7
SSNC0	—	—	—	21N2
WAIT1	—	—	—	21R9
GND	—	—	—	21J6

TTY STUB CABLE INDEX

PIN NO.	I/O LOC
103-2	22N7
102-2	22N8
204-2	22N8
203-2	22N8
104-2	22N9
202-2	22N9

TEST POINT INDEX

DESIG	MNEM	LOC.	BOARD
A	TMG1A	22S6	I/O
B	ENABL1	24D9	I/O
C	ATN1	24B9	I/O
D	READ1	22S6	I/O
E	SYSCL1	19G5	I/O
F	AD1	22K2	I/O
G	ARM0	24F9	I/O
	MB0	30R1	MEM
	READ1	27N9	MEM
	START1	30C1	MEM

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION	
ROM	35-388R08
ALU	35-389R08
MEM.CONT	35-387R13
I/O	35-390R15
ROM	35-388 M01 R04
I/O	35-390 M01 R10

NOTE:
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

REVISIONS

MNEM B140 & B150 ADD LOC 20G6 & 20H6. MNEM DDC1 ADD LOC 30R9. MNEM DECTR0 LOC WAS 30R9 ON MEM CONT. MNEM GDEST1 DELETE 10D3 LOCATION ON ALU. MNEM LSRL0 ADD LOC 15N1. AREA N8 REV LEVEL OF ROM, ALU, MEM CONT & I/O WERE R00, R00, R01 & R00 RESP. REV LEVEL OF SHTS 1,2,4,5,8,9,10,12,13,15,16,17,19, 20, 21, 22, 24, 25, 26, 27, 28, 29 & 30 WERE REV 0 RESP. MNEM DISR0 DELETED LOC 27C1 ON MEM. CONT.

RC	WH	03116-12	WH	29 NOV 71	R01

REV LEVEL OF ROM, ALU, MEM CONT & I/O WERE R04, R05, R03 & R08 RESP. 35-388 & 390 M01 WERE NOT SPEC'D. MNEM GDEST1 WAS NOT SPEC'D ON ALU. MNEM UBE1 WAS NOT SPEC'D. REV LEVEL OF SHTS 1, 2, 4, 5, 9, 10, 12, 19, 25, 26, 27, 29 & 30 WERE REV 1 RESP. REV LEVEL OF SHT 18 & SHT 23 WAS REV 0.

RC	WH	03116-32	WH	28 DEC 71	R02

REVISED SHTS 9, 10, 13, 16-19, 21, 23, 27, 30. REV LEVEL OF ROM, ALU, MEM CONT, I/O WERE R07, R07, R08, R08 RESP. 35-388 M01 WAS R03 35-390 M01 WAS R03.

WM	PB	03116-63	PB	8 MAR 72	R03

INIT. PB 3/23/72
DATE PBB 3/28/72

SHEET INDEX																														
REV. LEVEL	2	2		2	2			1	3	3		2	2		1	2	2	2	3	1	2	1	2	1	2	2	3	1	2	3
SHEET NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

NOTES

NAME	TITLE	DATE
P EDWARDS	DRAFT	10-15-71
R CERO	CHK	10-15-71
H HIDU	ENGR	
M FUCHS	Q.C.	
RE JONES	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR
TASK NO 03116
DWG NO. 01-051R03D08
SHEET 1 OF 30

INTERDATA®

BACK PANEL MAP

CONN.	TITLE	ROM 07		ALU 06		I/O CTRL 05		MEM CTRL 04	
	BD. LOC.	ROW		ROW		ROW		ROW	
	TERM. NO.	1	2	1	2	1	2	1	2
1	41	P5	GND	P5	GND	P5	GND	P5	GND
	40	GND	SRD041	GND	KILDSTO	GND	KILDSTO	GND	
	39	SRD051	SRD061			+12V	12VAC		
	38	SRD071	SRD001		CLKOFFO	LDI00	CATNO	WRTOA	
	37	LOADI	KSKIPO		SCLRO		SNGLO	MDI50	MDI60
	36	SRD011	SRD021	SYSCLI		FASTO	KSKIPO	MDI30	MDI40
	35	SRD031	SRD121	LOADI		SYSCLI	AASTI	MDI10	MDI20
	34	SRDI31	SRDI41			TACKO	RACKO	MD090	MD100
	33	SRDI51	SRD081			CLKOFFO	EXTCLKO	MD070	MD080
	32	DI	SKIPO		SCLO	DI	SKIPO	MD050	MD060
	31	DTESTO	GDESTI	GDESTI	USRLO	USRLO	DTESTO	MD030	MD040
	30	UDI00	LDI00	UDI00	USRHO	USRHO	UDI00	MD010	MD020
	29	UMDRI	SRD091		SHOTI	SHOTI	PFFI	MD000	
	28	SRDI01	DDCI	DDCI	CSVI	CSVI	UMDRI	DDCI	SSMEMI
	27	SRDI11	KILDSTO	SOOO	BOOO	BO80	SOOO	SOOO	BOOO
	26	P2I	SWTALO	SOI0	BOI0	BO90		SOI0	BOI0
	25	PCOO	SVSCO	SO20	BO20	BI00	RCLO	SO20	BO20
	24	RCLO	LRAHO	SO30	BO30	BI10	LRAHO	SO30	BO30
	23	JACCO	SVO	SO40	BO40	BI20	JACCO	SO40	BO40
	22	LCCO	RALI10	SO50	BO50	BI30	LCCO	SO50	BO50
	21	LINEI	RALI00	SO60	BO60	BI40	LINEI	SO60	BO60
	20	LFLRO	RAL090	SO70	BO70	BI50	LFLRO	SO70	BO70
	19		RAL080	SO80	BO80			SO80	BO80
	18		LRALO	SO90	BO90		LRALO	SO90	BO90
	17	GTP20	DISRO	SI00	BI00	SVO		SI00	BI00
	16	OPI		SI10	BI10	SVSCO	OPI	SI10	BI10
	15		SVACO	SI20	BI20	PCOO	SVACO	SI20	BI20
	14	BI30		SI30	BI30	SWTALO	WAITO	SI30	BI30
	13		WAITO	SI40	BI40	P2I	DCAKO	SI40	BI40
	12	DSTO	LDCTRO	SI50	BI50		DSTO	SI50	BI50
	11	SCLO	SO81	SO81	SO01	SO01	SCLO	SCLO	LDCTRO
	10	RAH040	SO91	SO91	SO11	SO81	USTRBO	USTRBO	MSOOO
	09	STFO	SI01	SI01	SO21	SO91	STFO	MSO10	MSO20
	08	STFLO	SI11	SI11	SO31	SI01	STFLO	MSO30	MSO40
	07	RAH050	SI21	SI21	SO41	SI11	SI21	MSO50	MSO60
	06	INHINCO	SI31	SI31	SO51		SI31	MSO70	MSO80
	05	RAH060	SI41	SI41	SO61		SI41	MSO90	MSI00
	04	HIDJAO	SI51	SI51	SO71		SI51	MSI10	MSI20
	03	BANKO	RAH070	CTFI	BANKO	BANKO	CTFI	MSI30	MSI40
	02	STPAO	FRCLOCO	FRCLOCO	FRNSI	FRNSI	STPAO	MSI50	MSI60
	01	GND	CLRO	GND	CLRO	GND	CLRO	GND	CLRO
	00	P5	GND	P5	GND	P5	GND	P5	GND
		1	2	1	2	1	2	1	2
0	41	P5	GND	P5	GND	P5	GND	P5	GND
	40	GND	SCLRIA	GND	SCLRIA	GND	SCLRIA	GND	SCLRIA
	39	FPMBYO	IR001		LARI	SCLRO	RD001	IR001	FPMBYO
	38	CSI	IR011	CSI	GA000	GA000	RD011	IR011	CSI
	37	FMDBYI	IR021		GB000	GB000	ATNO	IR021	FMDBYI
	36	FMDUAI	IR031			LDI01	ACKA00	IR031	FMDUAI
	35	LIRO	IR041			SRO	CLO70	IR041	LIRO
	34	LPSWI	IR051	LDI01		DRO	DCO	IR051	LPSWI
	33	LMARO	IR061	SVSCO	SVACO	DAO	DRDO	IR061	LMARO
	32	LMDRI	IR071	AMODI	T2I	ADRSO	CMDO	IR071	LMDRI
	31	MARI50	HWO	DO70	IR080	DI50	LPSWI	IR080	MARI50
	30	JOEI	SYNO	DO60	IR090	DI40	SYNO	IR090	JOEI
	29	NOMEMO	AMODI	DO50	IRI00	DI30	T2I	IRI00	NOMEMO
	28	P00	T2I	DO40	IRI10	DI20	RDSTBO	IRI10	P00
	27	PSW07I	RDSTBO	DO30	IRI20	DMO	INTAO	IRI20	PSW07I
	26	XO	CLRIRO	DO20	IRI30	DI00	PSW04I	IRI30	PSW04I
	25	SHRI	HDESTO	DO10	IRI40	DO90	PSW02I	IRI40	PSW02I
	24	SHLI	LARI	DO00	IRI50	DO80	PSW01I	IRI50	PSW01I
	23	SYSCLI	LARYSO	LARYSO	XO	T2INSI	CCI2I	CCI2I	T2INSI
	22	INTAO	LSRLO	LSRLO	DECTRO	DECTRO	CCI3I	CCI3I	DECTRO
	21	XI	DCLO	CTONEO	DCLO	DCLO	CCI4I	CCI4I	DCLO
	20	RDOOO	RDOO1	RDOO1	RDOOO	RDOOO	CCI5I	CCI5I	XI
	19	RDO10	RDO11	RDO11	RDO10	RDO10	CTONEO	CTONEO	CLRIRO
	18	RDO20	RDO21	RDO21	RDO20	UIR41	RDO21	MCLRI	UIR41
	17	RDO30	RDO31	RDO31	RDO30	RDO30	RDO31	RDO40	REQO
	16	RDO40	RDO41	RDO41	SHRI	RDO40	RDO41	RDO50	ENO
	15	RDO50	RDO51	RDO51	SHLI	RDO50	RDO51	MAI30	MAI40
	14	RDO60	RDO61	RDO61	RDO60	RDO60	RDO61	MAI10	MAI20
	13	RDO70	RDO71	RDO71	RDO70	RDO70	RDO71	MA090	MAI00
	12	RDO80	RDO81	RDO81	RDO80	RDO80	RDO81	MA070	MA080
	11	RDO90	RDO91	RDO91	RDO90	RDO90	RDO91	MA050	MA060
	10	RDI00	RDI01	RDI01	RDI00	RDI00	RDI01	MA030	MA040
	09	RDI10	RDI11	RDI11	RDI10	RDI10	RDI11	MA020	MA021
	08	RDI20	RDI21	RDI21	FLRI21	FLRI21	RDI21	RDO90	RDI10
	07	RDI30	RDI31	RDI31	STPCO	STPCO	RDI31	MAOI0	MAOII
	06	RDI40	RDI41	RDI41		RDI40	RDI41	MAOOO	MAOOI
	05	RDI50	RDI51	RDI51	UTI	RDI50	RDI51	PARO	CEMTO
	04	STOPO	RALI20	SUBI	CEMTO	STOPO	SUBI	INHO	ERO
	03	RALI50	SSKIPO		HDESTO	UTI	SSKIPO	WO	LRO
	02	RALI40	RALI30			+15V	-15V		SDUAO
	01	GND	PCIO	GND		GND	MSKI	GND	MSKI
	00	P5	GND	P5	GND	P5	GND	P5	GND
		1	2	1	2	1	2	1	2

CONN.	TITLE	MEM/IO 03		MEM/IO 02		MEM/IO 01		MEM/IO 00		TITLE	CONN.
	BD. LOC.	ROW		ROW		ROW		ROW		BD. LOC.	
	TERM. NO.	1	2	1	2	1	2	1	2	TERM NO.	
1	41	P5	GND					P5	GND	41	
	40	GND	GND					GND	GND	40	
	39	PI5	PI5					PI5	PI5	39	
	38	NI5	NI5					NI5	NI5	38	
	37	MDI50	MDI60					MDI50	MDI60	37	
	36	MDI30	MDI40					MDI30	MDI40	36	
	35	MDI10	MDI20					MDI10	MDI20	35	
	34	MD090	MDI00					MD090	MDI00	34	
	33	MD070	MD080					MD070	MD080	33	
	32	MD050	MD060					MD050	MD060	32	
	31	MD030	MD040					MD030	MD040	31	
	30	MD010	MD020					MD010	MD020	30	
	29	EXVT	MD000					EXVT	MD000	29	
	28	TEMPA	VT					TEMPA	VT	28	
	27	WRTO	TEMPB					WRTO	TEMPB	27	
	26	SCLRO	HWO					SCLRO	HWO	26	
	25									25	
	24									24	
	23	SYNO	ATNO					SYNO	ATNO	23	
	22	RACKO	TACKO					RACKO	TACKO	22	
	21	CL070	DAO					CL070	DAO	21	
	20	DRO	CMDO					DRO	CMDO	20	
	19	SRO	ADRSO					SRO	ADRSO	19	
	18	DI40	DI50					DI40	DI50	18	
	17	DI20	DI30					DI20	DI30	17	
	16	DI00	DI10					DI00	DI10	16	
	15	DO80	DO90					DO80	DO90	15	
	14	DO60	DO70					DO60	DO70	14	
	13	DO40	DO50					DO40	DO50	13	
	12	DO20	DO30					DO20	DO30	12	
	11	DO00	DO10					DO00	DO10	11	
	10	WRTOA	MSOOO					WRTOA	MSOOO	10	
	09	MSO10	MSO20					MSO10	MSO20	09	
	08	MSO30	MSO40					MSO30	MSO40	08	
	07	MSO50	MSO60					MSO50	MSO60	07	
	06	MSO70	MSO80					MSO70	MSO80	06	
	05	MSO90	MSI00					MSO90	MSI00	05	
	04	MSI10	MSI20					MSI10	MSI20	04	
	03	MSI30	MSI40					MSI30	MSI40	03	
	02	MSI50	MSI60					MSI50	MSI60	02	
	01	GND	GND					GND	GND	01	
	00	P5	GND					P5	GND	00	
		1	2	1	2	1	2	1	2		
0	41	P5	GND					P5	GND	41	
	40	GND	GND					GND	GND	40	
	39	PI5	REQO					PI5	REQO	39	
	38	NI5	ENO					NI5	ENO	38	
	37	ACTO	TACO					ACTO	TACO	37	
	36									36	
	35									35	
	34							XRACKO		34	
	33	MAI30	MAI40					MAI30	MAI40	33	
	32	MAI10	MAI20					MAI10	MAI20	32	
	31	MA090	MAI00					MA090	MAI00	31	
	30	MA070	MA080					MA070	MA080	30	
	29	MA050	MA060					MA050	MA060	29	
	28	RDACKO	TDACKO					RDACKO	TDACKO	28	
	27	DCO	DCRO					DCO	DCRO	27	
	26	SCLRO	HWO					SCLRO	HWO	26	
	25									25	
	24									24	
	23	SYNO	ATNO					SYNO	ATNO	23	
	22	RACKO	TACKO					RACKO	TACKO	22	
	21	CL070	DAO					CL070	DAO	21	
	20	DRO	CMDO					DRO	CMDO	20	
	19	SRO	ADRSO					SRO	ADRSO	19	
	18	DI40	DI50					DI40	DI50	18	
	17	DI20	DI30					DI20	DI30	17	
	16	DI00	DI10					DI00	DI10	16	
	15	DO80	DO90					DO80	DO90	15	
	14	DO60	DO70					DO60	DO70	14	
	13	DO40	DO50					DO40	DO50	13	
	12	DO20	DO30					DO20	DO30	12	
	11	DO00	DO10					DO00	DO10	11	
	10	MA030	MA040					MA030	MA040	10	
	09	MA020	MA021					MA020	MA021	09	
	08	MA01	MA02					MA01	MA02	08	
	07	MA010	MA011					MA010	MA011	07	
	06	MA000	MA001					MA000	MA001	06	
	05	PARO	MA00					PARO	MA00	05	
	04	INHO	ERO					INHO	ERO	04	
	03	WO	LRO					WO	LRO	03	
	02	PI5	NI5					PI5	NI5	02	
	01	GND	GND					GND	GND	01	
	00	P5	GND					P5	GND	00	
		1	2	1	2	1	2	1	2		

NOTES

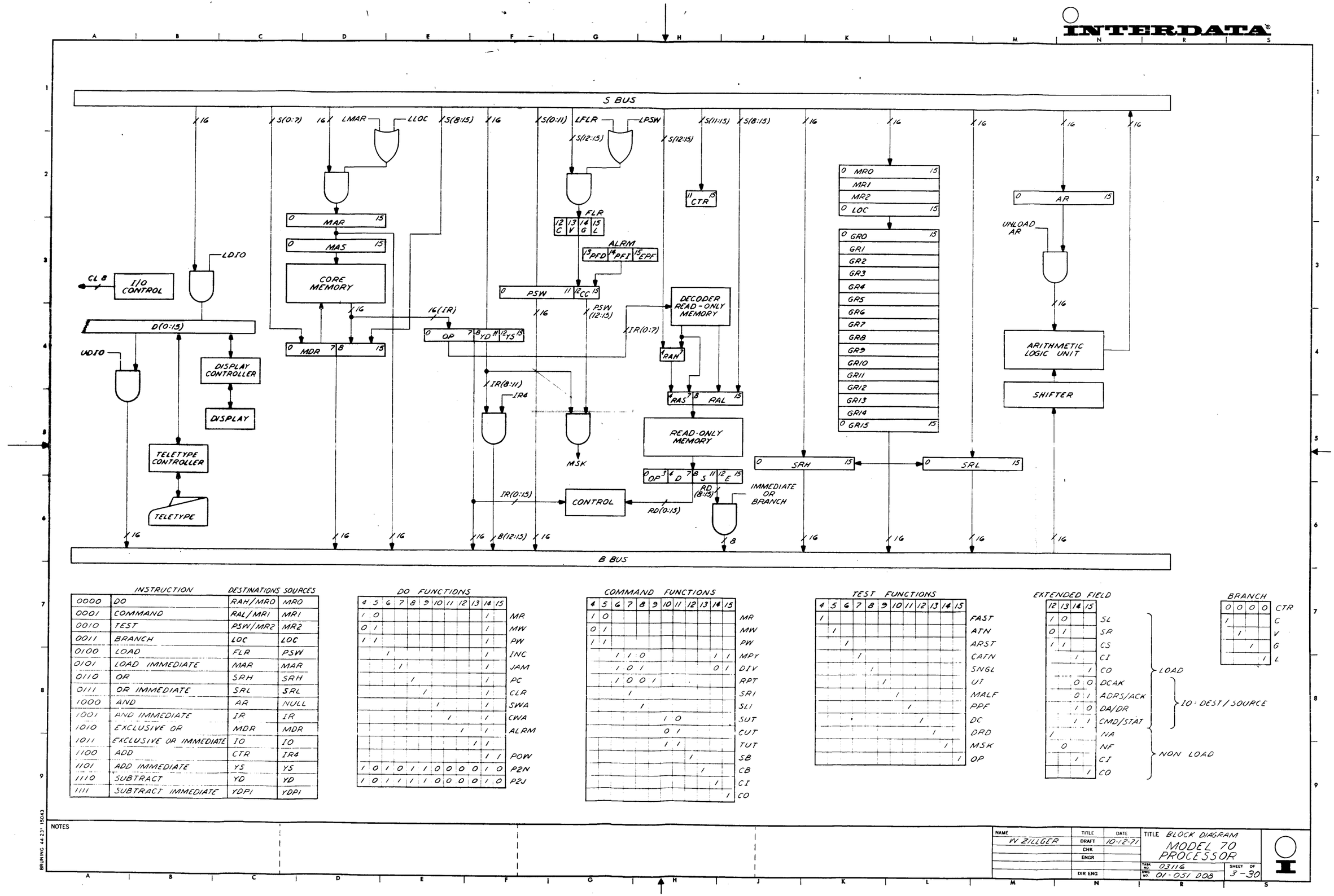
SIGNALS ON PIN 130-0 ROM, 131-1 ALU & 230-0 MEM. CTRL WERE NOT SPECD.
RC | 03116-32 | 28 DEC 71 | R02

DELETED SIG GDESTI FROM PIN NUMBER 131-1 ALU. ADD SIG TO PIN 227-1 ROM & PIN 139-0 PAS 00 MEM. I/O.
RC | 03116-12 | 24 NOV 71 | E01

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	OCT 13, '71
	CHK	
	ENGR	
	DIR ENG	

TITLE BACK PANEL MAP
MODEL 70
PROCESSOR (CPU)

DRAW NO. 03116
DWG NO. 01-051R02D08
SHEET OF 2-30



	INSTRUCTION	DESTINATIONS SOURCES	
0000	DO	RAH/MR0	MR0
0001	COMMAND	RAL/MR1	MR1
0010	TEST	PSW/MR2	MR2
0011	BRANCH	LOC	LOC
0100	LOAD	FLR	PSW
0101	LOAD IMMEDIATE	MAR	MAR
0110	OR	SRH	SRH
0111	OR IMMEDIATE	SRL	SRL
1000	AND	AR	NULL
1001	AND IMMEDIATE	IR	IR
1010	EXCLUSIVE OR	MDR	MDR
1011	EXCLUSIVE OR IMMEDIATE	IO	IO
1100	ADD	CTR	IR4
1101	ADD IMMEDIATE	YS	YS
1110	SUBTRACT	YD	YD
1111	SUBTRACT IMMEDIATE	YDPI	YDPI

DO FUNCTIONS

4	5	6	7	8	9	10	11	12	13	14	15	
1	0										1	MR
0	1										1	MW
1	1										1	PW
			1								1	INC
				1							1	JAM
					1						1	PC
						1					1	CLR
							1				1	SWA
								1			1	CWA
									1		1	ALRM
										1	1	
										1	1	POW
1	0	1	0	1	1	0	0	0	0	1	0	P2N
1	0	1	1	1	1	0	0	0	0	1	0	P2J

COMMAND FUNCTIONS

4	5	6	7	8	9	10	11	12	13	14	15	
1	0											MR
0	1											MW
1	1											PW
		1	1	0						1	1	MPY
		1	0	1						0	1	DIV
		1	0	0	1							RPT
			1									SRI
				1								SLI
						1	0					SUT
						0	1					CUT
						1	1					TUT
								1				SB
									1			CB
										1		CI
											1	CO

TEST FUNCTIONS

4	5	6	7	8	9	10	11	12	13	14	15	
1												FAST
	1											ATN
		1										ARST
			1									CATN
				1								SNGL
					1							UT
						1						MALF
							1					PPF
								1				DC
									1			DRD
										1		MSK
											1	OP

EXTENDED FIELD

12	13	14	15		
1	0			SL	LOAD
0	1			SR	
1	1			CS	
		1		CI	
			1	CO	
		0	0	DCAK	IO: DEST/SOURCE
		0	1	ADRS/ACK	
		1	0	DA/DR	
		1	1	CMD/STAT	
1				NA	NON LOAD
	0			NF	
		1		CI	
			1	CO	

BRANCH

0	0	0	0	
1				CTR
	1			C
		1		V
			1	G
			1	L

NOTES

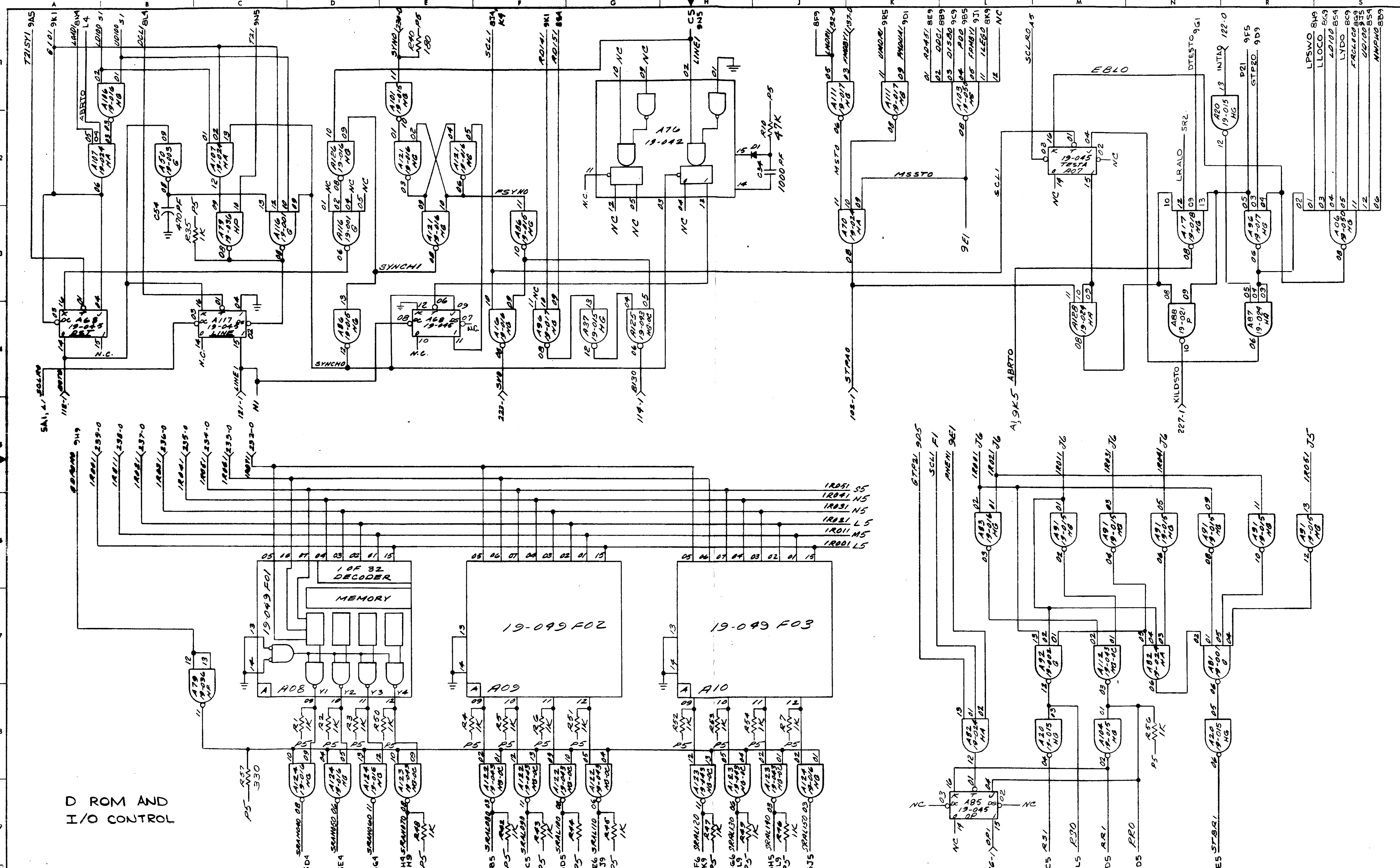
NAME	TITLE	DATE
W ZILLGER	DRAFT	10-12-71
	CHK	
	ENGR	
	DIR ENG	

TITLE BLOCK DIAGRAM
MODEL 70
PROCESSOR

TASK NO. 03116
DWG NO. 01-051 D08
SHEET 3 OF 30

BRUNING 44231 15043

INTERDATA®



NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-388 ROM BOARD.

AREA M4 IC A128 WAS NOT SPEC'D. REVISED CIRCUITRY	PIN 9 WAS N.C. AREA A2, A107 PIN 04 WAS N.C. AREA N3, A17 PIN 12 WAS CONNECTED TO A17 PIN 10.	AREA D2 & 3 & AREA G4. ICs A126, A116, A37 & A125 WERE NOT SPEC'D. R35 WAS NOT SPEC'D. VALUE OF C54 WAS 1CONF VALUE OF R57 WAS 1K. REVISED CIRCUITRY AREA J7 19-049F03 WA 19-042F03. AREA E4, A68
RC 03116-32 R02	PE 03116-12 24NOV71 R01	

NAME	TITLE	DATE
E. ROE	DRAFT	12 OCT 71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TASK NO. 03116

DWG NO. 01-051R02D08

SHEET 4-30

BRUNING 44 231 15043

INTERDATA®

ROM ADDRESS REGISTER

NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-388 ROM BOARD.

AREA C1: IC #21 "NC" WAS SPECD AS "G".

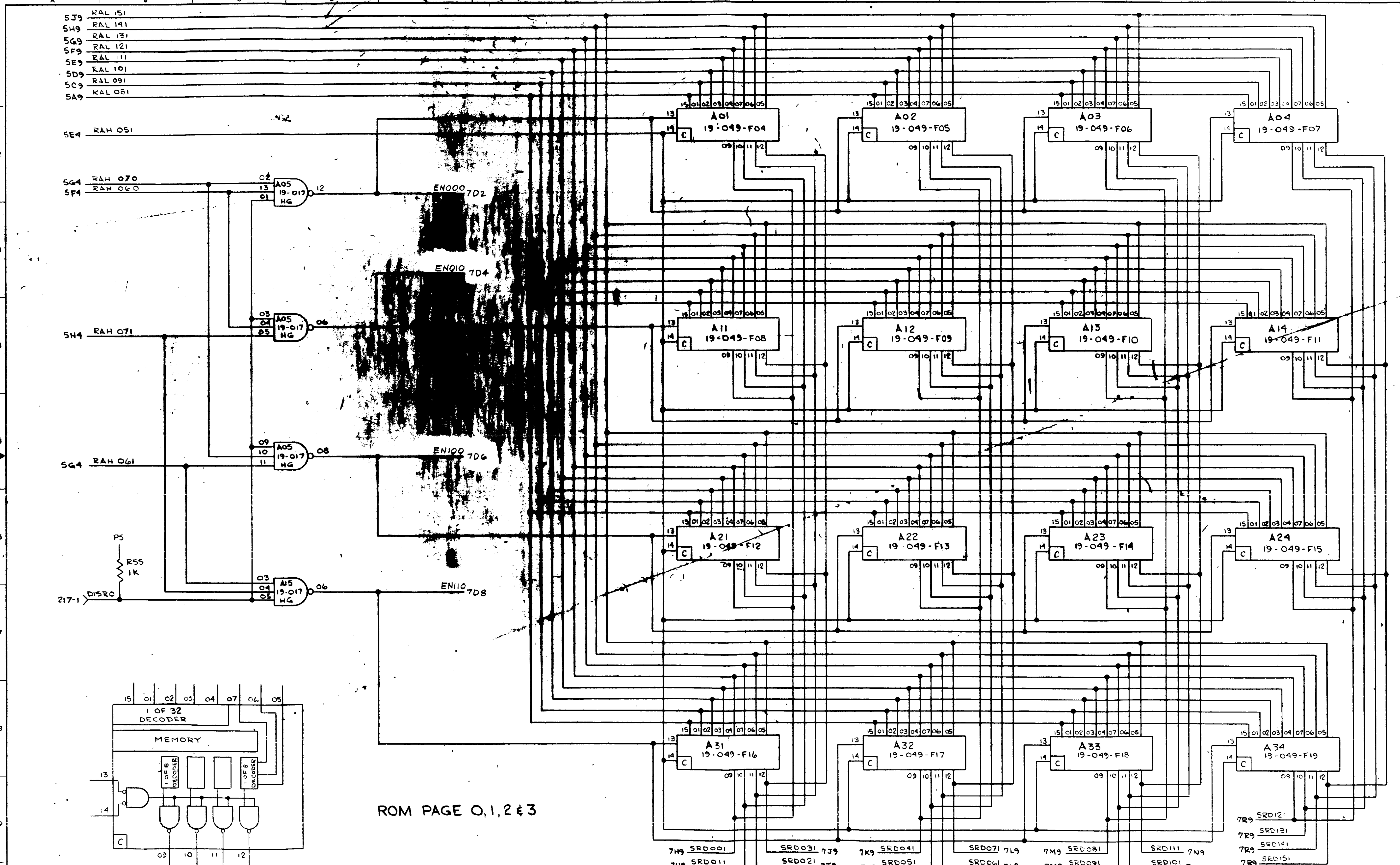
AREA J2: VALUE OF R8 & 9 WAS 1K. AREA R1: CONNECTED A67 PIN 03 TO A11 PIN 12

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	10-13-71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO 03116 SHEET OF 5-30
DRG NO 01-051REC2 D08

BRUNING 44 2 11 15043



NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-388 ROM BOARD.

NAME	CHRIS JENSEN
DRAFT	10-5-71
TITLE	FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR
No.	03116 01-051 D08
SHEET 6 OF 30	

INTERDATA®

5H9 RAL 150
5G9 RAL 140
5F9 RAL 130
5E9 RAL 120
5D9 RAL 110
5C9 RAL 100
5B9 RAL 090
5A9 RAL 080

6E2 EN000
5D4 RAH 050

6E3 EN010
8A4

6E5 EN100
8A4

6E7 EN110
8A4

A41 19-049-F20
A42 19-049-F21
A43 19-049-F22
A44 19-049-F23
A51 19-049-F24
A52 19-049-F25
A53 19-049-F26
A54 19-049-F27
A61 SEE NOTE 2
A62 SEE NOTE 2
A63 SEE NOTE 2
A64 SEE NOTE 2
A71 SEE NOTE 2
A72 SEE NOTE 2
A73 SEE NOTE 2
A74 SEE NOTE 2

P5
R18 470
R19 470
R20 470
R21 470
R22 470
R23 470
R24 470
R25 470
R26 470
R27 470
R28 470
R29 470
R30 470
R31 470
R32 470
R33 470

8B1, 6H9 SRD001
8C1, 6H9 SRD011
SRD021 6J9, 8D1
SRD031 6J9, 8D1
8E1, 6K9 SRD041
6K9, 8F1 SRD051
SRD061 6L9, 8G1
SRD071 6L9, 8H1
8J1, 6M9 SRD081
6M9, 8K1 SRD091
SRD101 6N9, 8L1
SRD111 8M1, 6N9
8N1, 6R9 SRD121
8N1, 6R9 SRD131
8R1, 6R9 SRD141
8S1, 6R9 SRD151

1 OF 32 DECODER
MEMORY
1 OF 8 DECODER
1 OF 8 DECODER

ROM PAGE 4, 5, 6 & 7

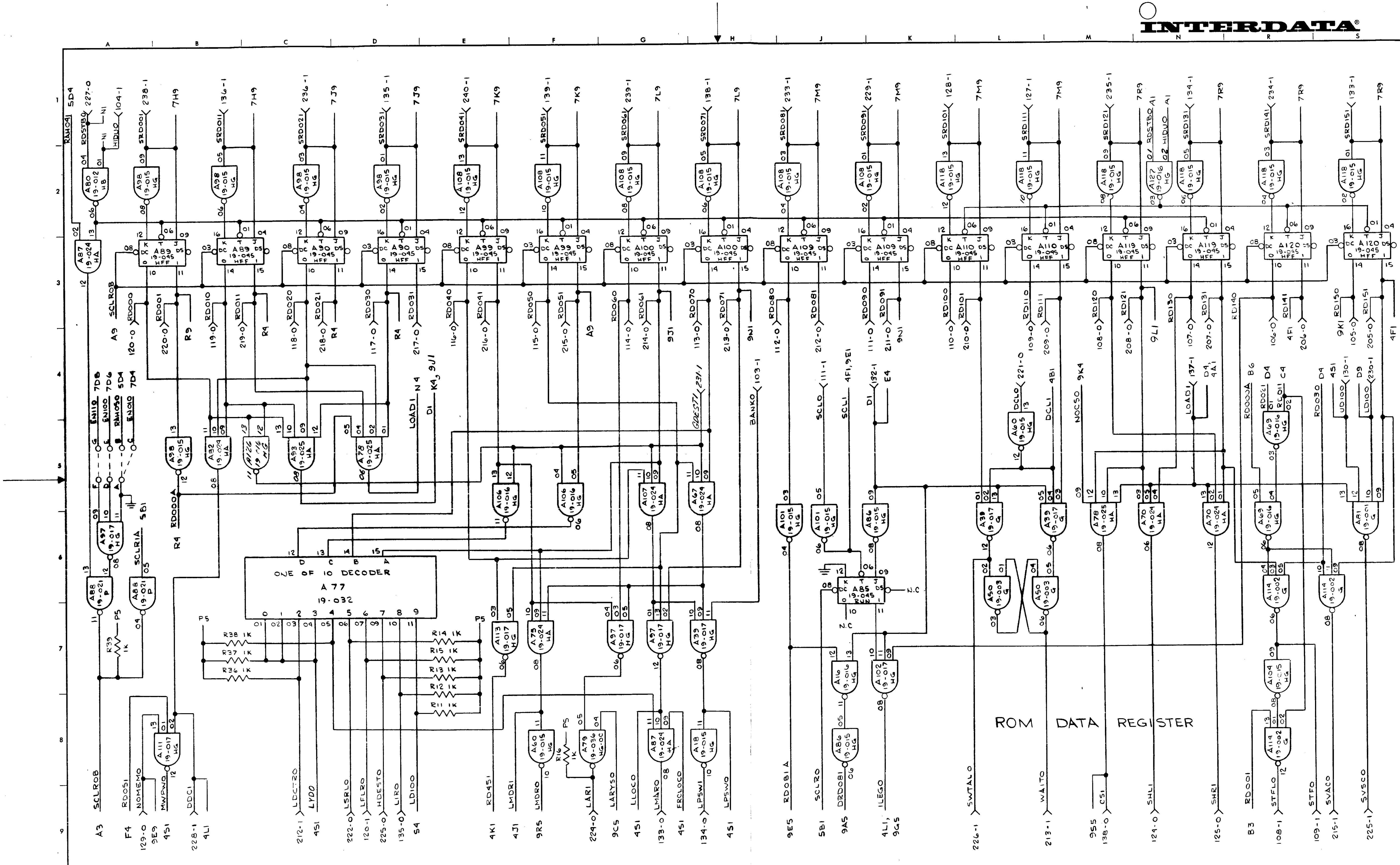
NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-388 ROM BOARD.
2. COMPONENTS ARE SHOWN FOR REFERENCE ONLY AND ARE NOT PART OF THE ASSEMBLY.

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO. 03116
DRC NO. 01-051 D08
SHEET OF 7-30

BRUNING 44 231 15043

INTERDATA



NOTES

1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-388 ROM BOARD.

AREA J4, A109 PIN 10 WAS CONNECTED TO (AREA 9N1) A40 PIN 1.

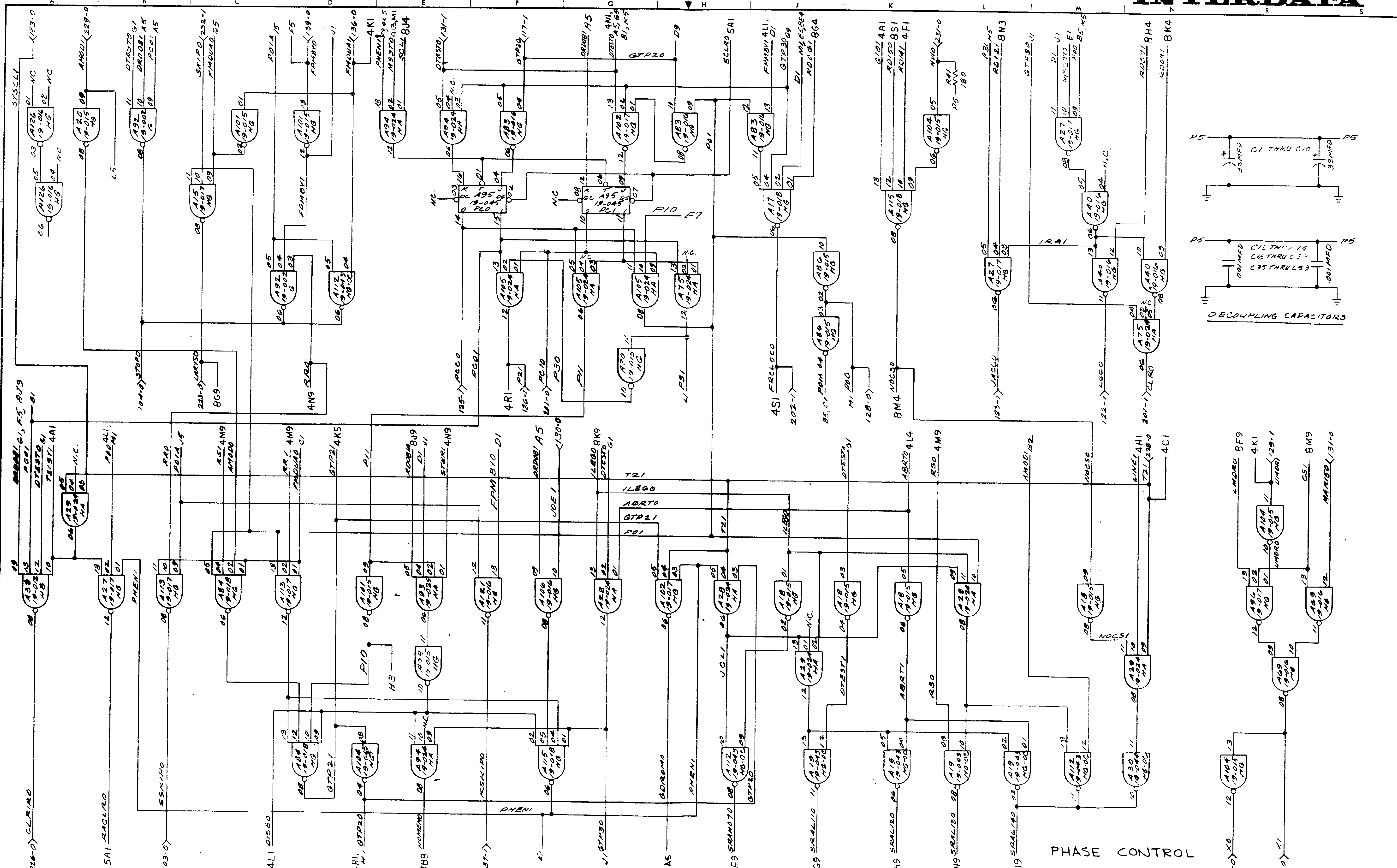
PC	14.	03116-12		29 NOV 71	R01

NAME		TITLE	DATE
CHRIS JENSEN		DRAFT	10-8-71
		CHK	
		ENGR	
		DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO 03116
DWG NO 01-051 R01 D08
SHEET OF 8-30

INTERDATA®



NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-388 ROM BOARD.

BACKPANEL PIN 130-1 WAS NOT SPEC'D.	AREA M1, A27 PIN 11 WAS DRDO81, A27 PIN 10 WAS PHEN1	AREA H2 IC A126 (2 PLACES) WAS NOT SPEC'D. AREA E-7 A95 WAS SPEC'D AS A.C. AREA M2, DELETED A40 PIN 3 TO A40 PIN 4. DELETED A40 PIN 2 TO A117 PIN 2
RC 03116-32 28 DEC 71 R02	PC 03116-12 24 NOV 71 R01	
DELETED 123-0 TO A126-01. DELETED A126-06 TO A29-03	AREA F6. A121 PIN 13 & A106 PIN 10 WERE TIED TOGETHER.	
PB 03116-63 PB 6 MAR 72 R03		

NAME	TITLE	DATE
E. ROE	DRAFT	14 OCT 71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TASK NO. 03116

DWG NO. 01-051R03D08

SHEET 9-30

BRUNING 44 231 15043

INTERDATA®

REGISTER STACK ADDRESS DECODING

NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-389 ALU BOARD.

CROSS REF 13L4, AREA H-1, WAS NOT SPEC.

AREA J2. A95 PIN 10 & A53 PIN 10 WERE TIED TOGETHER. BOLD PRINT PIN 131-1 WAS NOT SPEC'D.

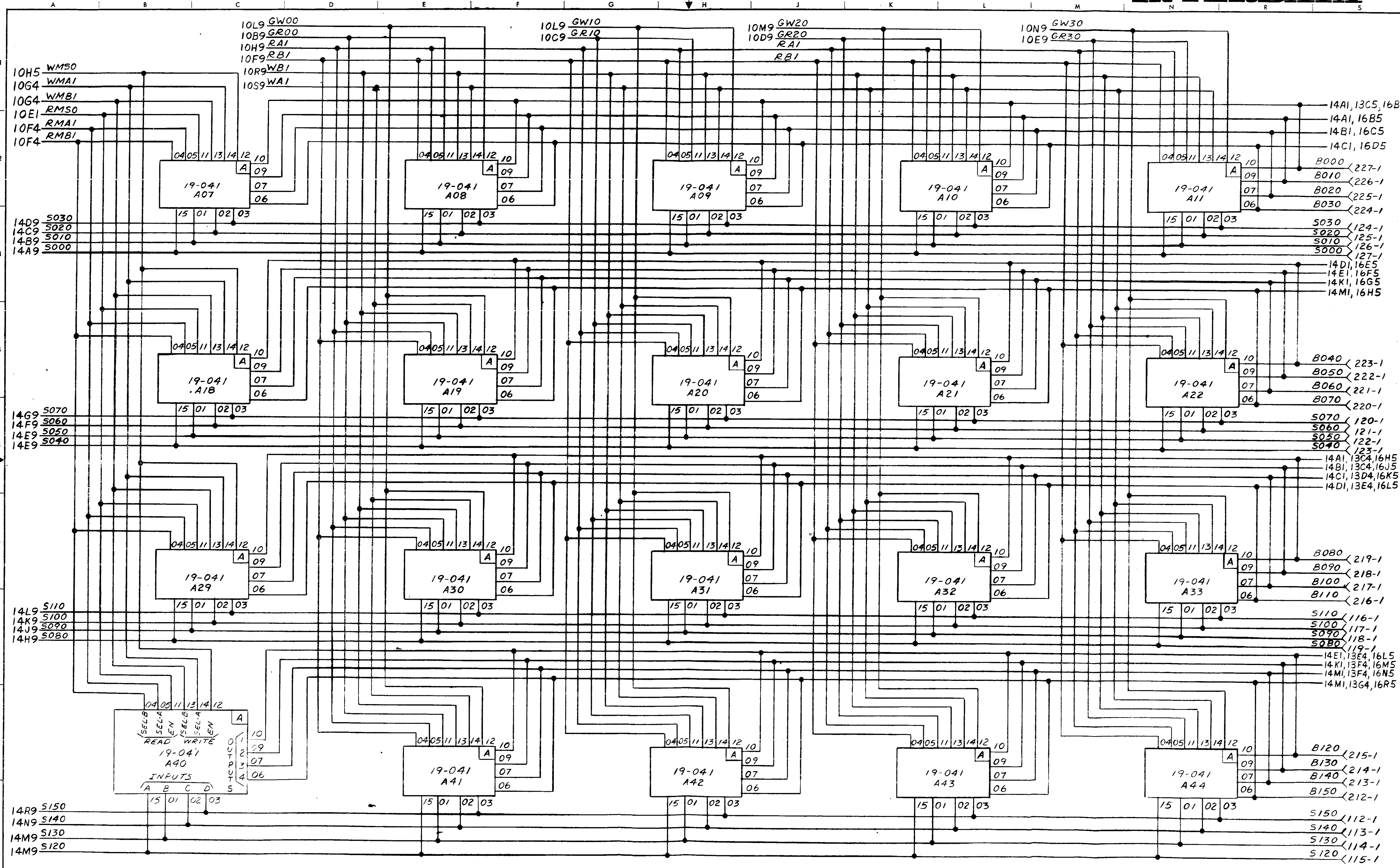
AREA D2. DELETE IC A62, 19-016, PIN 4 & 5 WHAT TO A95 PINS 11 & 13 RESP. ALSO PINS WHAT TO GND. 11IN6L PIN 131-1.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO. 03116
DWG NO. 01 01R03D05
SHEET OF 10-30

BRUNING 44-231 15043

INTERDATA®



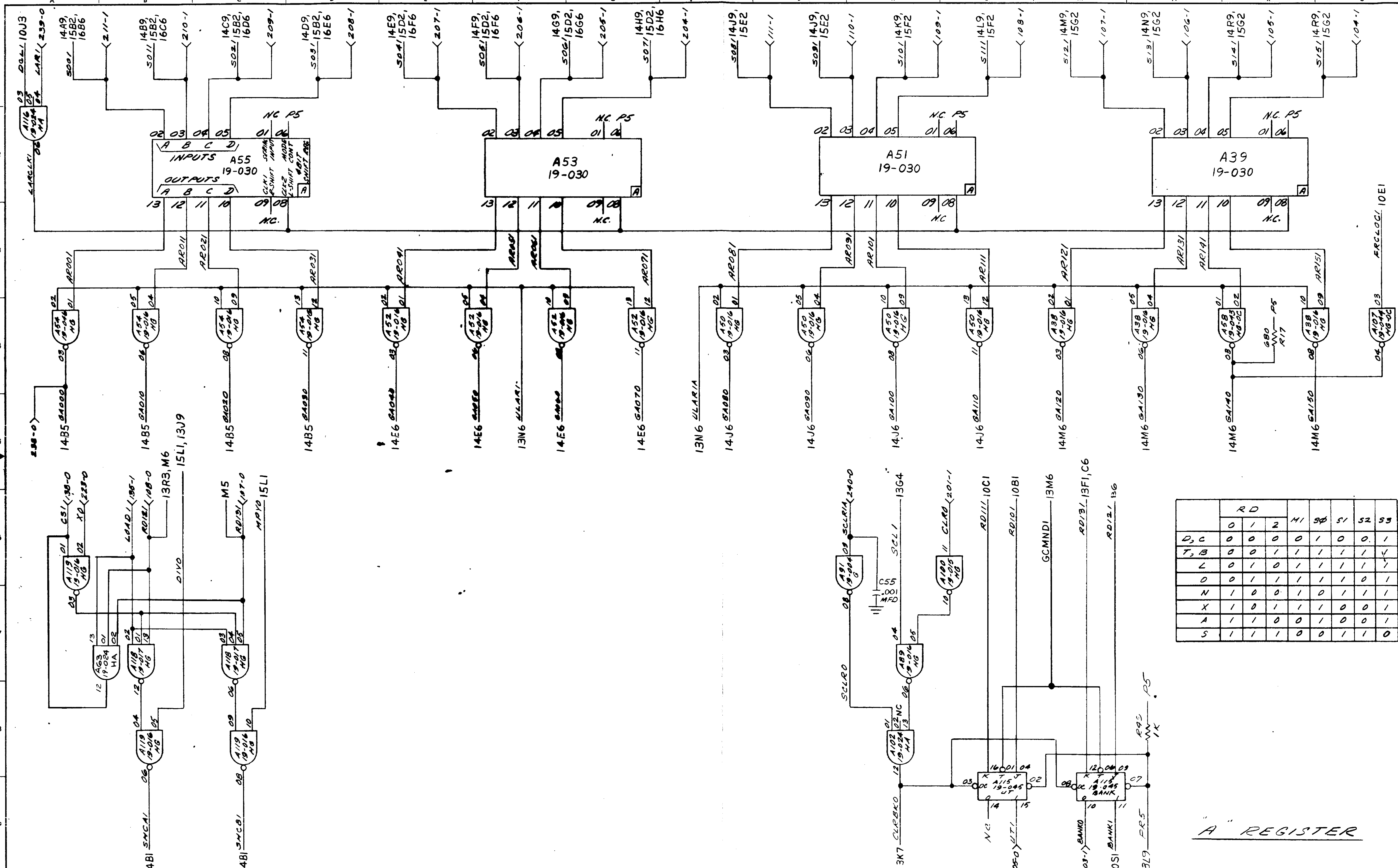
NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-389 ALU BOARD.

REGISTER STACK

NAME L VALENTY	DRAFT 8-31-71	TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR
	CHK	
	ENGR	TASK NO 03116
	DIR ENG	DWG NO 01-051 D05 SHEET 11 OF 39

BRUNING 44 231 15043

INTERDATA



	RD			M1	S⌀	S1	S2	S3
	0	1	2					
D, C	0	0	0	0	1	0	0	1
T, B	0	0	1	1	1	1	1	1
L	0	1	0	1	1	1	1	1
O	0	1	1	1	1	1	0	1
N	1	0	0	1	0	1	1	1
X	1	0	1	1	1	0	0	1
A	1	1	0	0	1	0	0	1
S	1	1	1	0	0	1	1	0

"A" REGISTER

NOTES 1. ALL APPARATUS ON THIS SHEET LOCATED ON 35-389 ALU BOARD.

IN AREA K-6 C55 WAS NOT SPEC. | U.P. | RG | 03116-32 | KG | 12-28-71 | R02

AREA B-5 DELETE COORDINATION 15A2 FRONT RIV... AREA A7 ADDED A63 AREA M9, A115 WAS CONNECTED TO A66 PIN 1 (13E1) | PC | 03116-12 | 24 NOV 71 | R01

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

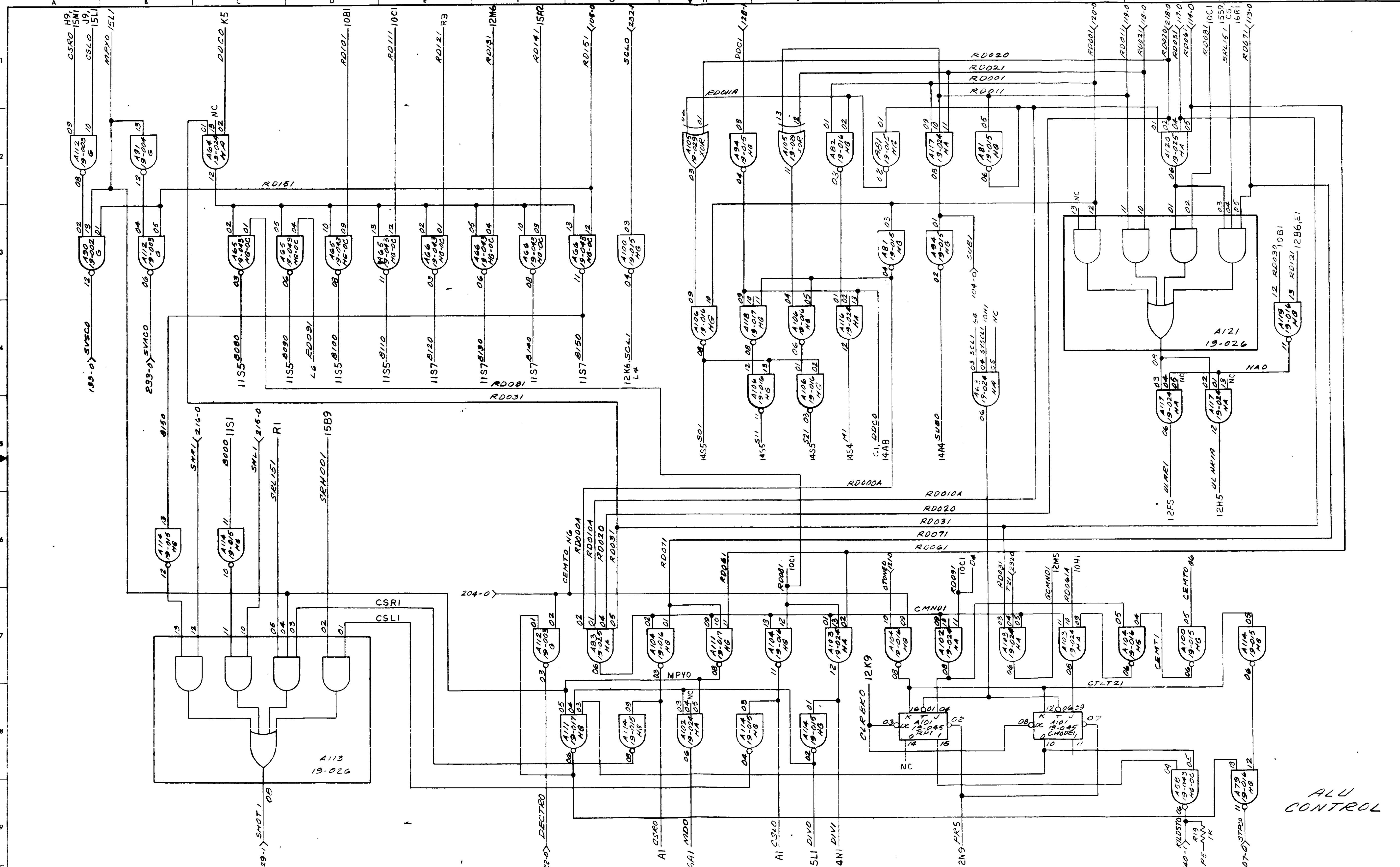
TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TASK NO. 03116

DWG NO. 01-051R02D08

SHEET 12 OF 30

INTERDATA®



NOTES 1. ALL APPARATUS IN THIS SHEET IS LOCATED ON 35-389 ALU BOARD.

AREA H1, A94 PIN 3 WAS CONNETED TO (AREA J) A103 PIN 5. CONNECTED A103 PIN 5 TO CMND1.

ADDED A63, AREA L-6

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

03116

01-051 R02 D08

SHEET 13 OF 30

INTERDATA®

SHIFTER & ALU

A28 19-038 · A27 DUAL 4 LINE TO 1 LINE DATA SELECTOR 19-038 · A26 19-038 · A25 19-038 · A24 19-038 · A35 19-038 · A36 19-038 · A37 19-038

A23 4 BIT ALU 19-039 · A34 19-039 · A45 19-039 · A56 19-039

A57 19-040 · A82 19-016 HG · A79 19-016 HG · A100 19-015 HG · A99 19-018 HG · A49 19-015 HG · A48 19-015 HG · A47 19-015 HG · A46 19-050 HG

NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-389 ALU BOARD.

NAME	TITLE	DATE
L VALENTY	DRAFT	8-30-71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TASK NO 03116 · DWG NO 01-051 D08 · SHEET OF 14-30

BRUNING 44.231.15043

ALU

INTERDATA

SHIFT REGISTERS

NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-389 ALU BOARD.

AREA A3 ADD COORDINATION
L1 TO DIVO SIGNAL.
AREA L1 ADD COORDINATION
A2 TO DIVO SIGNAL.

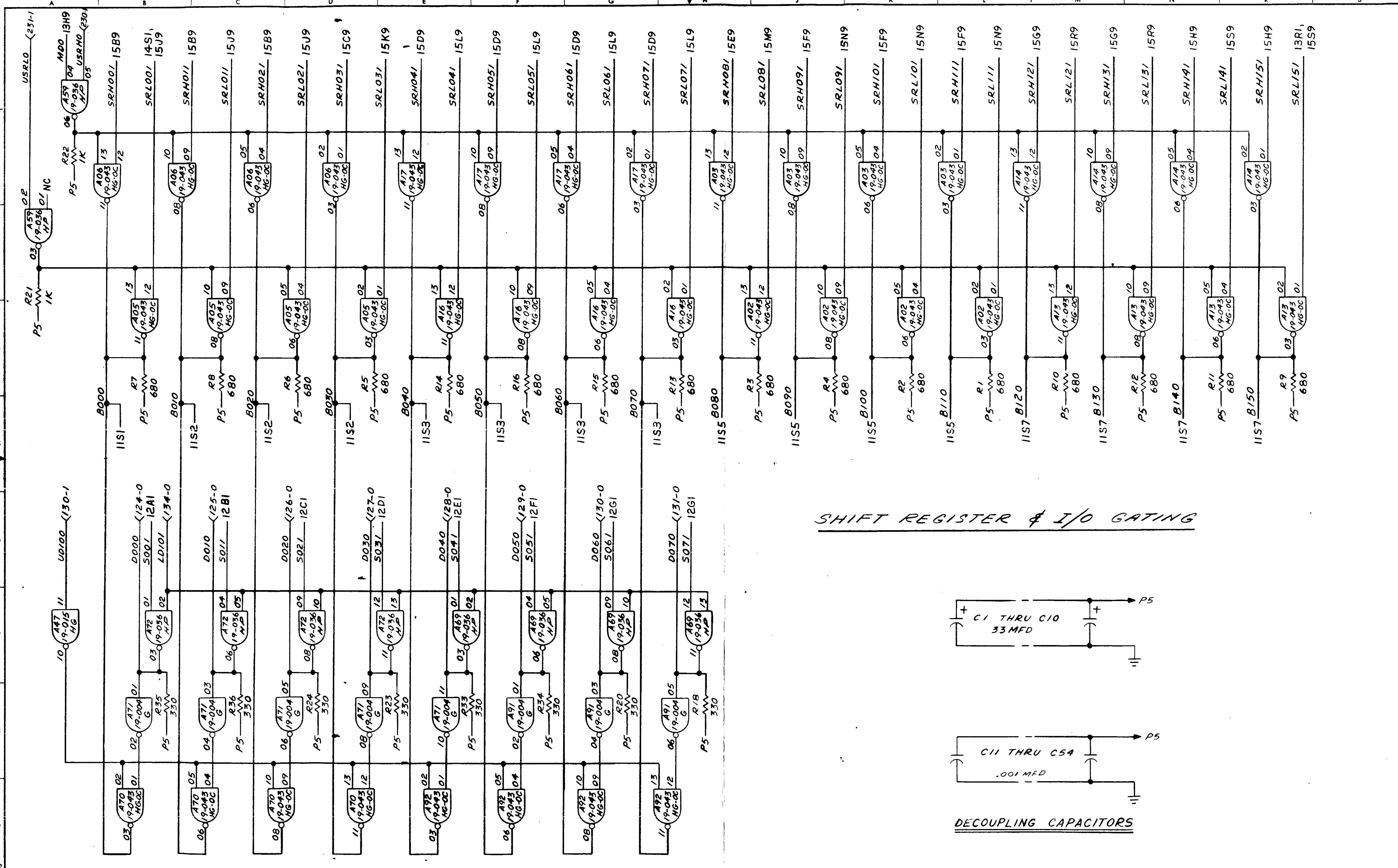
RC	NUM	03116-12		29NOV 71	R01

	NAME	TITLE	DATE
	M WILLIS	DRAFT	
		CHK	
		ENGR	
		DIR ENG.	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116
DRG NO. 01-051,R01 D08

SHEET OF 15-30



NOTES 1 ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-383 ALU BOARD.

AREA L9, C11 THRU C54 WERE DISC CAPS.

AREA L8, C56-C61 WERE NOT SPEC.

NAME		TITLE	DATE
L VALENTY	DRAFT		8-26-71
	CHK		
	ENGR		
	DIR ENG		

TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TAB. NO. 03116

DWG NO. 01-051 R02 D08

SHEET 16 OF 30

INTERDATA

FLAGS AND ALARM REGISTERS

NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD

NAME	TITLE	DATE
N. WILLIS	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TASK 03116 SHEET OF

DWG NO 01-051B02 DOG 17-30

BRUNING 44231 15043

INTERDATA®

TEST AND BRANCH

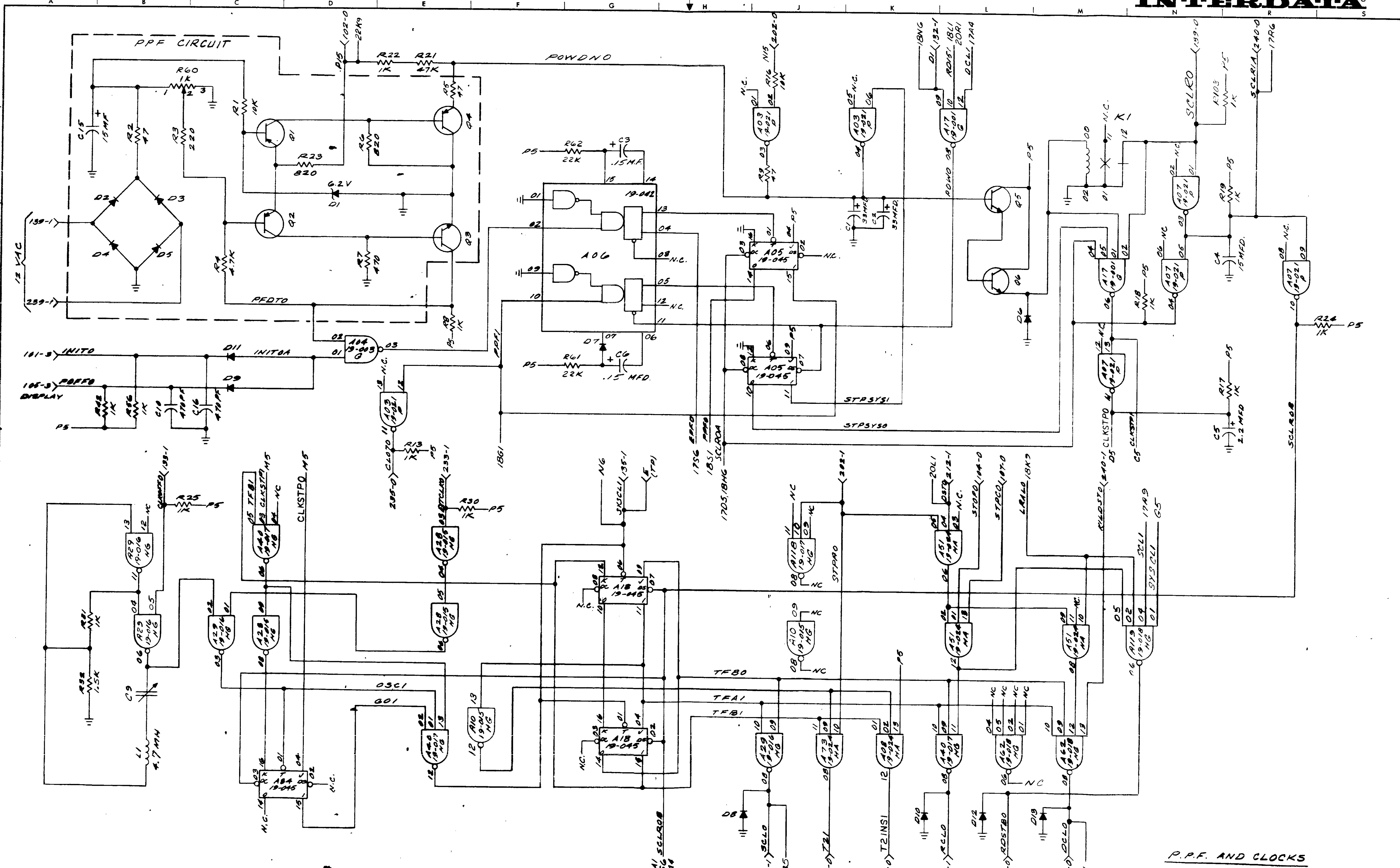
NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD.

AREA N2: RD131 WAS SPECD AS RD031.	RC	03116-32	28620-01	R01	NAME E. ROE	TITLE	DATE 4 OCT 71
AREA K5: 203-0 WAS 203-1. AREA N8: ADDED RIO5 & C77	MM	PL	03116-63	PL	7 MAR 72	R02	CHK
							ENGR
							DIR ENG

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO. 03116 SHEET OF
DWG NO. 01-051 R02 D08 18-30

BRUNING 44 231 15043

INTERDATA®



P.P.F. AND CLOCKS

NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD.

DELETED A10-08 TO 229-0. DELETED A118-08 TO A10-09 DELETED A10-13 TO A40-04. DELETED A62-01, 02, 04, 05. ADDED A40-13 TO A40-06 A29-02. D10 GO TO A29-04 EXCHANGED A29-05 WITH A29-12	AREA K2. DELETE R10, 1K RES IN SERIES WITH PIN 9 OF A03. R61 & 62 WERE VARI RES. C3 & 6 WERE 2.2MF	AREA J6 & 7 ADDED A10 & A118. AREA N7 ADDED A119. AREA F8 ADDED A10. AREA N1 ADDED R103. AREA J2 A103 WAS SPEC'D AS A103
03116-23 · 8 MAR 72 · R03	RC · 03116-32 · 28 DEC 71 · R02 — R32 WAS 2.2K. DELETED A118-09 TO A73-08	RC · 03116-12 · 29 NOV 71 · R01

NAME	TITLE	DATE
E. ROE	DRAFT	5 OCT 71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TASK NO. 03116 · DWG NO. 01-051R03008 · SHEET 19 OF 30

INTERDATA®

I/O GATING

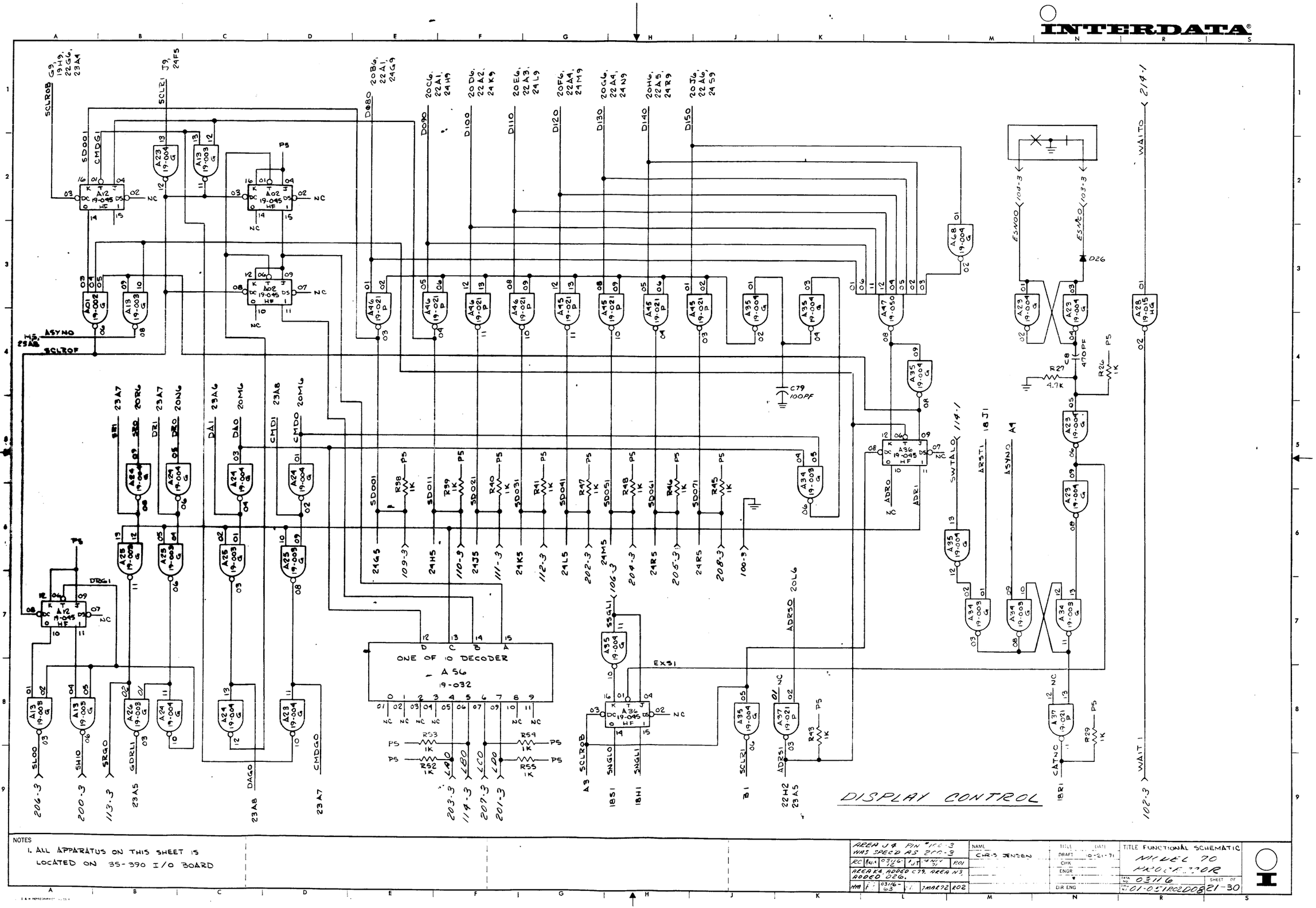
NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD.

AREA J2. NIC PINS 3 & 9 WERE REVERSED. AREA E9 C79, 75 & 76 WERE NOT SPEC'D.

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	10-9-71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO 03116
DWG NO 01-05RAD08
SHEET 20 OF 30

BRUNING 44-231 15043



NOTES

1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD

AREA J & PIN "17C-3 WAS SPECD AS 200-3

AREA K4 ADDED C79, AREA N3 ADDED D26.

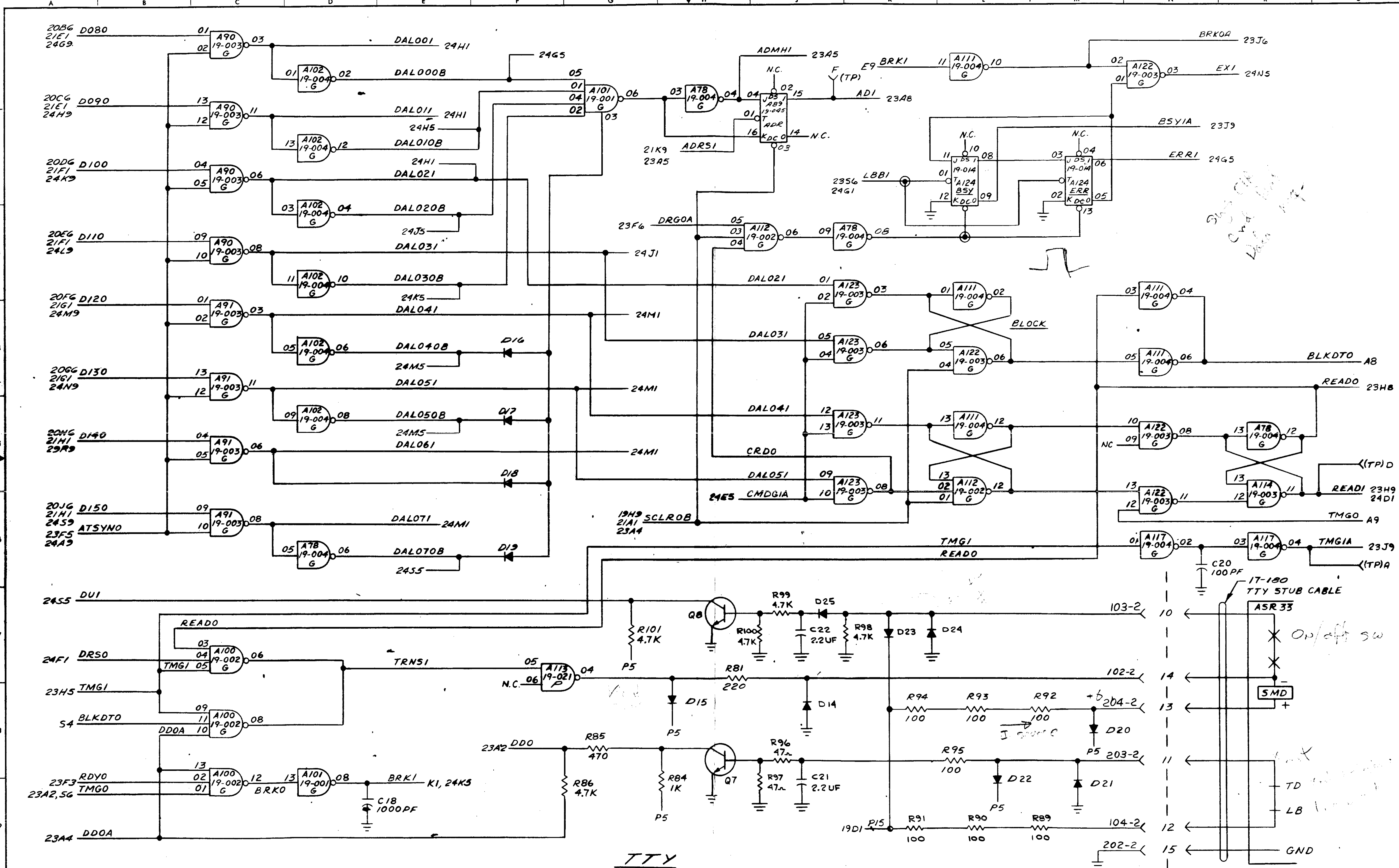
RC	03/16-15	J.T.	7MAR72	R01		
HM	03/16-03		7MAR72	R02		

	NAME	DATE
DRAFT	CHR.S JENSEN	10-21-71
CHK		
ENGR		
DIR ENG		

TITLE FUNCTIONAL SCHEMATIC
MICRO 70
MODEL 70R

TASK NO. 03116
ITEM NO. 01-05112CE005
SHEET 21 OF 30

INTERDATA



NOTES

1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD

AREA E7 CABLE NO. WAS 17-003. AREA H7 VALUE OF R81 WAS 100. AREA F4 ADDED DESIGNATION D16 TO DIODE.

NAME	L VALENTY	TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR
		DRAFT	9-22-71	
		CHK		
		ENGR		
		DIR ENG		DWG NO. 01-051R01D08 SHEET 22 OF 30

INTERDATA®

NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD

IN AREA J-4 REVERSED CONNECTIONS OF PINS 4 & 10 OF I.C. A14.

U.R.	P.O.	ECR			
		03116-32	KT	028-71	R01

AREA D4, MOVED C78, AREA B6, REVERSED PINS 9 & 10 ON A67.

WM	P/O	03116-33	J/C	8 MAR 72	R02

NAME	TITLE	DATE
L VALENTY	DRAFT	9-23-71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116 | SHEET OF 23-30
DRG NO. 01-051R02D08

INTERDATA®

TTY

A116 19-030 4 BIT SHIFT REG. (-2 OUTS, SERIAL INPUT, MODE CONT, CLK1 R-SHIFT, CLK2 L-SHIFT)

A126 19-030 4 BIT SHIFT REG.

A93 19-038 DUAL 4/1 MUX

A104 19-038 DUAL 4/1 MUX

A92 19-038 DUAL 4/1 MUX

A103 19-038 DUAL 4/1 MUX

C17 100PF

C19 470PF

R82 1K

R83 3.3K

C23 THRU C30 33MFD

C31 THRU C72 .001 MFD

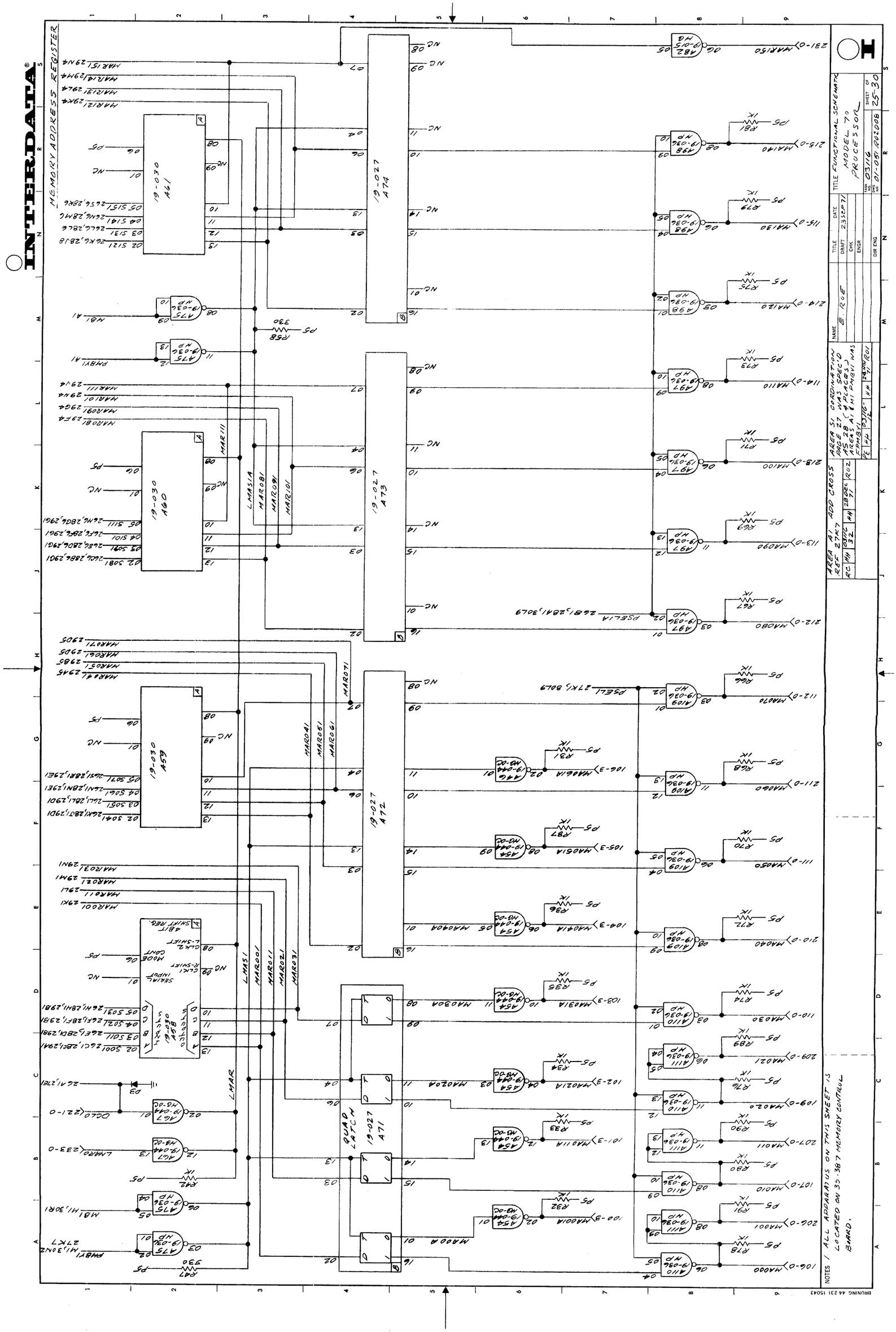
DECOUPLING CAPACITORS

NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-390 I/O BOARD

AREA C4 R10 4 WAS NOT SPECD.

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	10-1-71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR
TASK NO. 03116
DWG NO. 01-051R01 D08
SHEET 29 OF 30


INTERDATA
MEMORY ADDRESS REGISTER
TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR
SHEET OF 25-30
03/16
01-05-2006
AREA A1 ADD CROSS REF 2747
AREA S1 CARDINATION PAGE 27 WAS SPECIFIED AS 28 (4 PLACES) AREA S1 & A1 PAGE 31
NOTES / ALL APPARATUS ON THIS SHEET IS LOCATED ON 30-387 MEMORY CONTROL BOARD.
BRUNING 44 231 15043

INTERDATA®

NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-387 MEMORY CONTROL BOARD

R24 THRU R39 WERE SPEC'D AS 1K. AREA 01 PIN 210-1 WAS SPEC'D AS 210-0.

EC [illegible] 03176-35 [illegible] 28 DEC 71 E02

AREA A1 COORDINATION 27E1 WAS NOT SPEC'D.

EC [illegible] 03176-12 [illegible] 29 NOV 71 E01

NAME	TITLE	DATE
L VALENTY	DRAFT	9-7-71
	CHK	
	ENGR	
	DIR ENG	

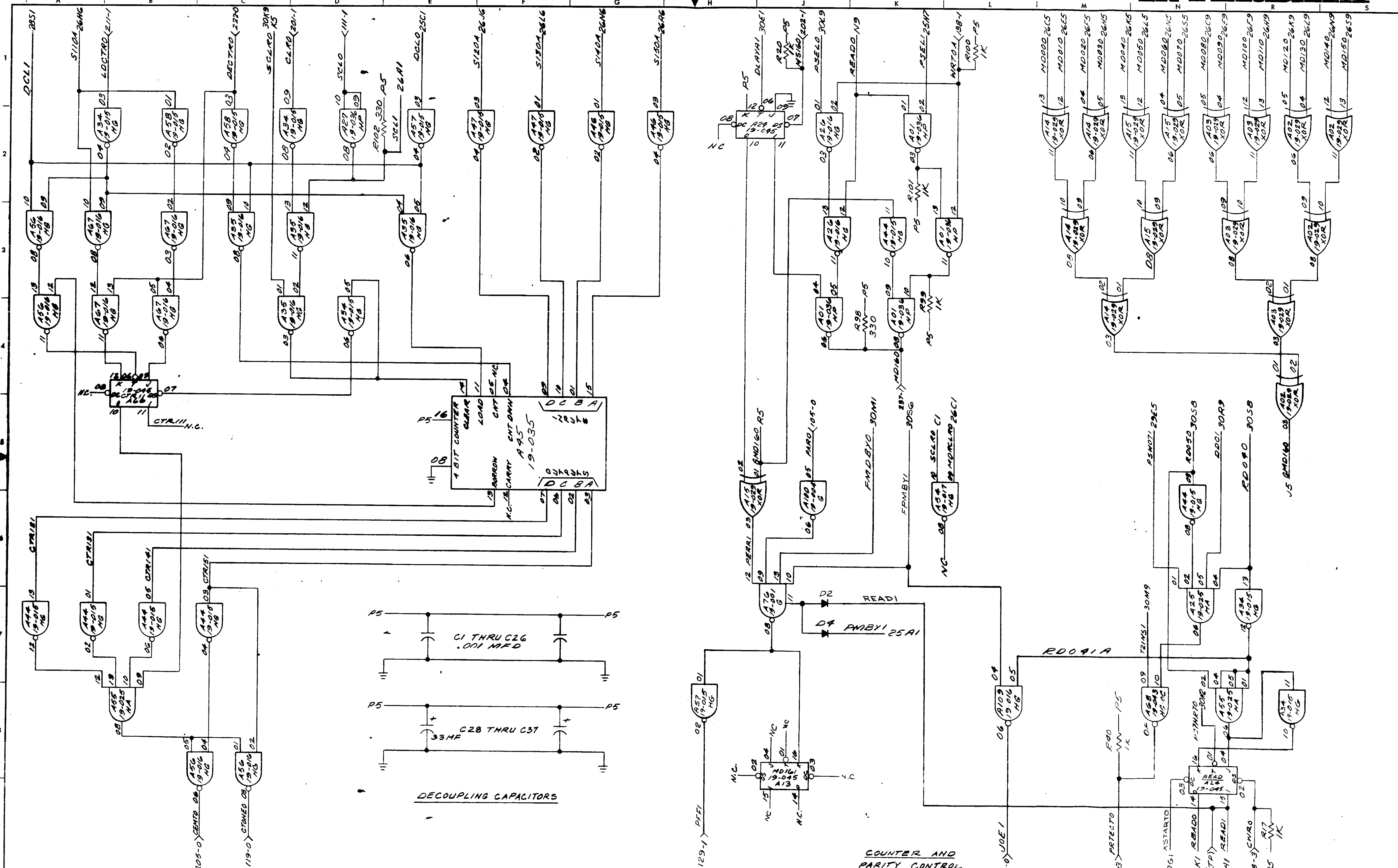
TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116
W.O. NO. 01-0051 RC2008
SHEET OF 26-30

MEMORY DATA REGISTER

BRUNING 44 231 15043

INTERDATA



NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-387 MEMORY CONTROL BOARD

AREA N8, A68-09 WAS NOT SPEC. | 03116-63 | 8 MAR 72 | R03

AREA K & L7. IC A109 & D9 WERE NOT SPEC'D. DELETED C27 DECOUPLING CAP. | RC | 03116-32 | 28 DEC 71 | R02

PIN 16 WAS GND. PIN 04 WAS TO A55 PIN 06. AREA J7, A76 PIN 10 WAS FMDUAO | PC | 03116-12 | 24 NOV 71 | R01 | R98 & R102 WERE SPEC'D AS 1K.

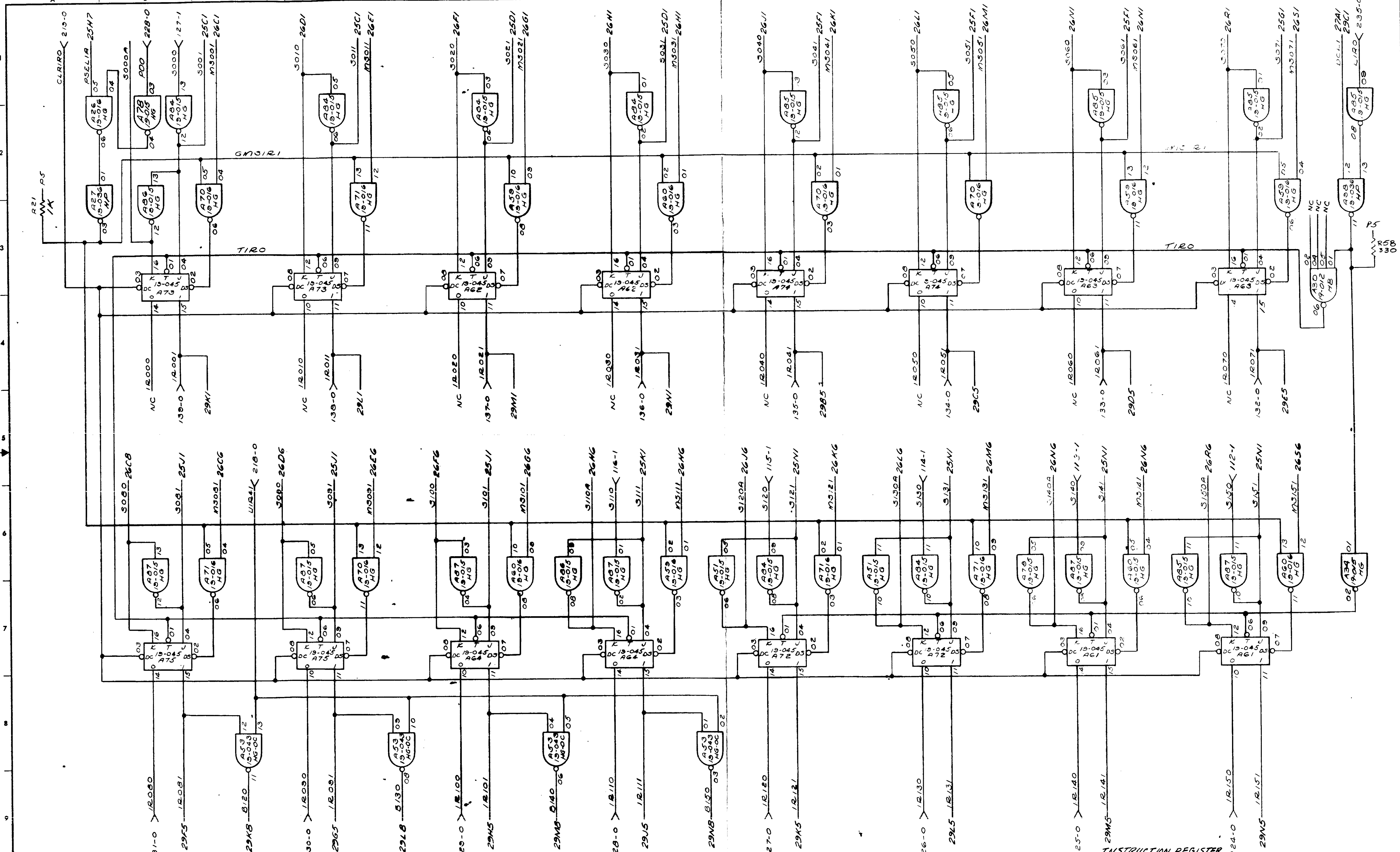
AREA L6, DELETED A34 PINS 02 & 01 BETWEEN A13 PIN 03 & A54 PIN 8. AREA J9, A13 PIN 15 WAS PFF1 (TO 129-1) PIN 04 WAS TO A57 PIN 02. PIN 01 WAS MBCLIP. AREA R8, A24 PIN 03 WAS CLMFO.

AREA F2. A97 PINS 1 & 2 WERE SPEC'D AS 3 & 4 RESP. AREA E7, C1 THRU C27 WERE DISC CAPS. AREA K6, DELETED A100 PINS 12 & 13 BETWEEN A76 PIN 13 & A77 PIN 10 (30M1).

NAME	TITLE	DATE
E. ROE	DRAFT	29 SEP 71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 70 PROCESSOR

TASK NO. 03116 — DWG NO. 01-051 R03 D08 — SHEET 27 OF 30



NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-387 MEMORY CONTROL BOARD.

ADDED A30 & A34, R58 WAS 1K

AREA S8 ADD PIN #5 TO I.C. AREA H7, ADD PIN #3 ... AREA H7, A64 PIN 01 WAS TO A72 PIN 01. AREA S3, A63 PIN 01 WAS TO A58 PIN 11. AREA S3 & S6,

NAME	TITLE	DATE
C. SCOTT	DRAFT	2 SEP 71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR

03116
01-051 R01 D08
SHEET 28 OF 30

INTERDATA®

A 50
19-030
4 BIT SHIFT REGISTER
INPUTS A B C D
OUTPUTS A B C D
MODE CONT
SERIAL INPUT
CLK 1 R SHIFT
CLK 2 L SHIFT

A 49
19-030

A 48
19-030

A 41
19-038

A 40
19-038

A 39
19-038
DUAL 4 LINE TO 1 LINE DATA SELECTOR

A 38
19-038

A 37
19-038

A 36
19-038

A 43
19-038

A 42
19-038

A 52
19-026

PSW031
PSW021
PSW011
PSW001

PSW AND B BUS GATING

NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-387 MEMORY CONTROL BOARD.

SPECD AS 19-033.
RC 03116-32 28 DEC 71 R02

AREA N3 A31 WAS
SPECD AS A32 IN ERROR.
RC 03116-12 28 NOV 71 R01

AREA G7. A32 WAS
SPECD AS 19-032.
AREA K7. A33 WAS

NAME CHRIS JENSEN
DRAFT 9-22-71
CHK
ENGR
DIR ENG

TITLE FUNCTIONAL SCHEMATIC
MODEL 70
PROCESSOR

TASK NO. 03116
DWG NO. 01-051 R02 D08
SHEET OF 29-30

D D & W REPROGRAPHICS 40CSS 4

INTERDATA®

MEMORY CONTROL AND TIMING

A102 19-042 DUA

A103 19-042

A101 19-042

A105 19-042

A104 19-042

NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-387 MEMORY CONTROL BOARD.

AREA M8, A69-04,05 DIO GO TO A57-06.

C39 WAS SPEC'D AS 470 PF.

AREA M9, ADDED T3INS1. AREA J8, ADDED C96. A68-13 DIO GO TO 223-0.

WERE NOT SPEC'D. R67 WAS 6.8K. DELETED R86 VARI POT IN PARALLEL WITH R67. R87, 92, 91, 90 & 85 WERE SHOWN IN PARALLEL WITH R66, 71, 70, 69 & 68 RESP. C93 WAS SPEC'D AS 68 PF.

ADDED CONNECTION TO A76 PIN 10 AREA H5 ADDED A100

DELETED R88 & 89 VARI POTS IN PARALLEL WITH R65 & 64 RESP. R65 THRU 66, 68, 63, 70 & C91

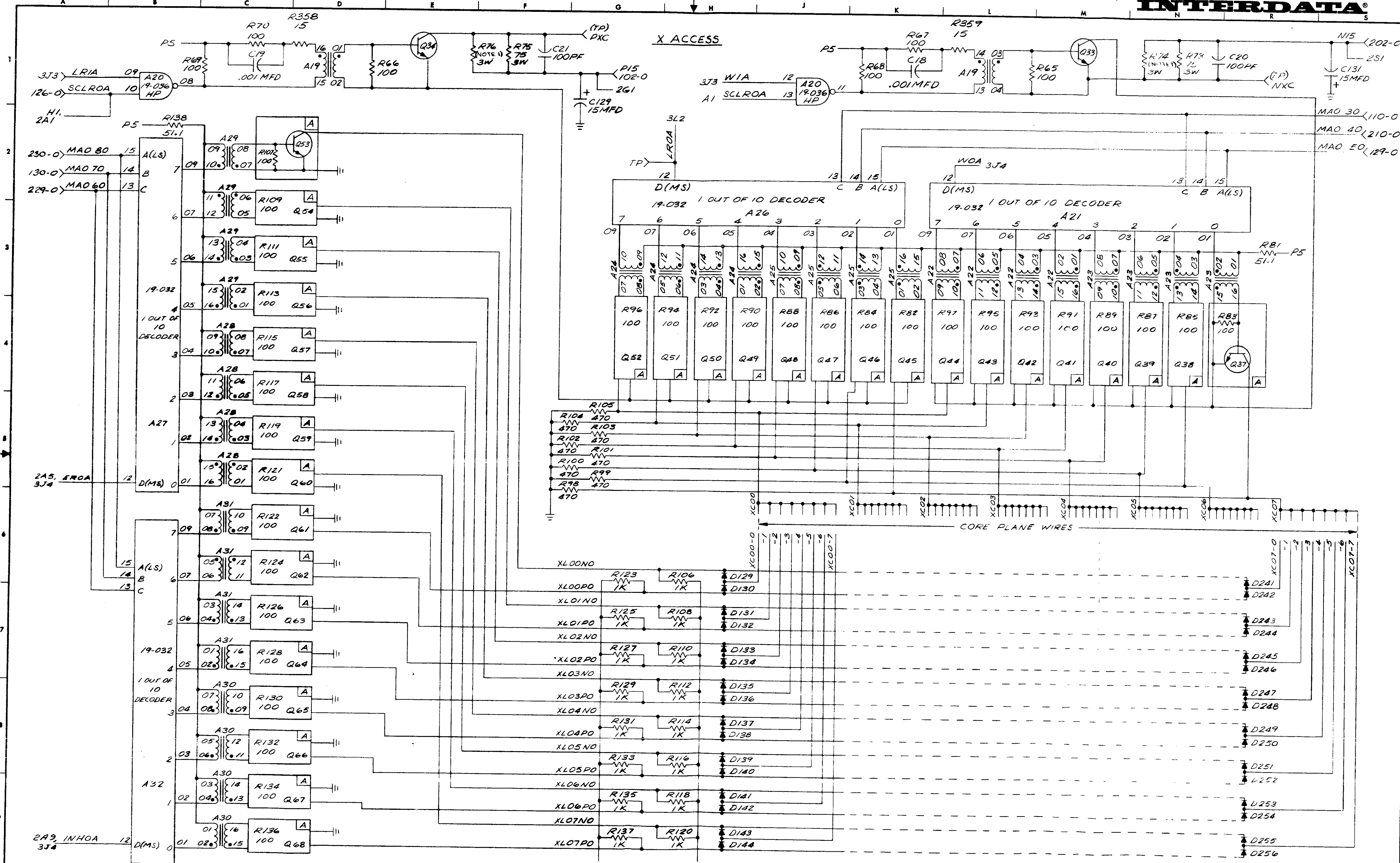
C38 WAS 22 PF. C95 WAS 47 PF. C99 WAS 68 PF. AREA N8 ARE (PRINTED) WERE NOT SPEC'D. REVISED "MBCLIP" CIRCUIT AREA N2 PMBY1 WAS FPMBY1. AREA S7

NAME	TITLE	DATE
CHRIS JENSEN	DRAFT	9-28-71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 70 PROCESSOR

TASK NO. 03116
DWG NO. 01-051 R03 D08
SHEET OF 30-30

INTERDATA®



NOTES
1. VALUE TO BE DETERMINED AT TIME OF MANUFACTURE.

PE	BA	1236	11/23/71	R02
ON SHT. 6KB-DELETED BACK PANEL ADDRESS CONNECTION TABLE. (SEE USERS MANUAL)				
PE	BA	1272	1/19/72	R03

REVISIONS:
ON SH 3R3, R251 WAS 2.2K; C114 WAS 68 PF.
BA | 10-5-71 | R01
ON SHT. 1&2 DELETED VALUE OF R74, R76, R78, & R80. ADDED NOTE 1. ON SHT 3R3, R251 WAS 6.8K

NAME	TITLE	DATE
D. DWORZAK	DRAFT	10 FEB 71
R. F. ZERO	CHK	1 JULY 71
B. MCKERNAN	ENGR	6 JULY 71
M. FUHS	QC	6 JULY 71
R. E. JONES	DIR ENG	6 JULY 71

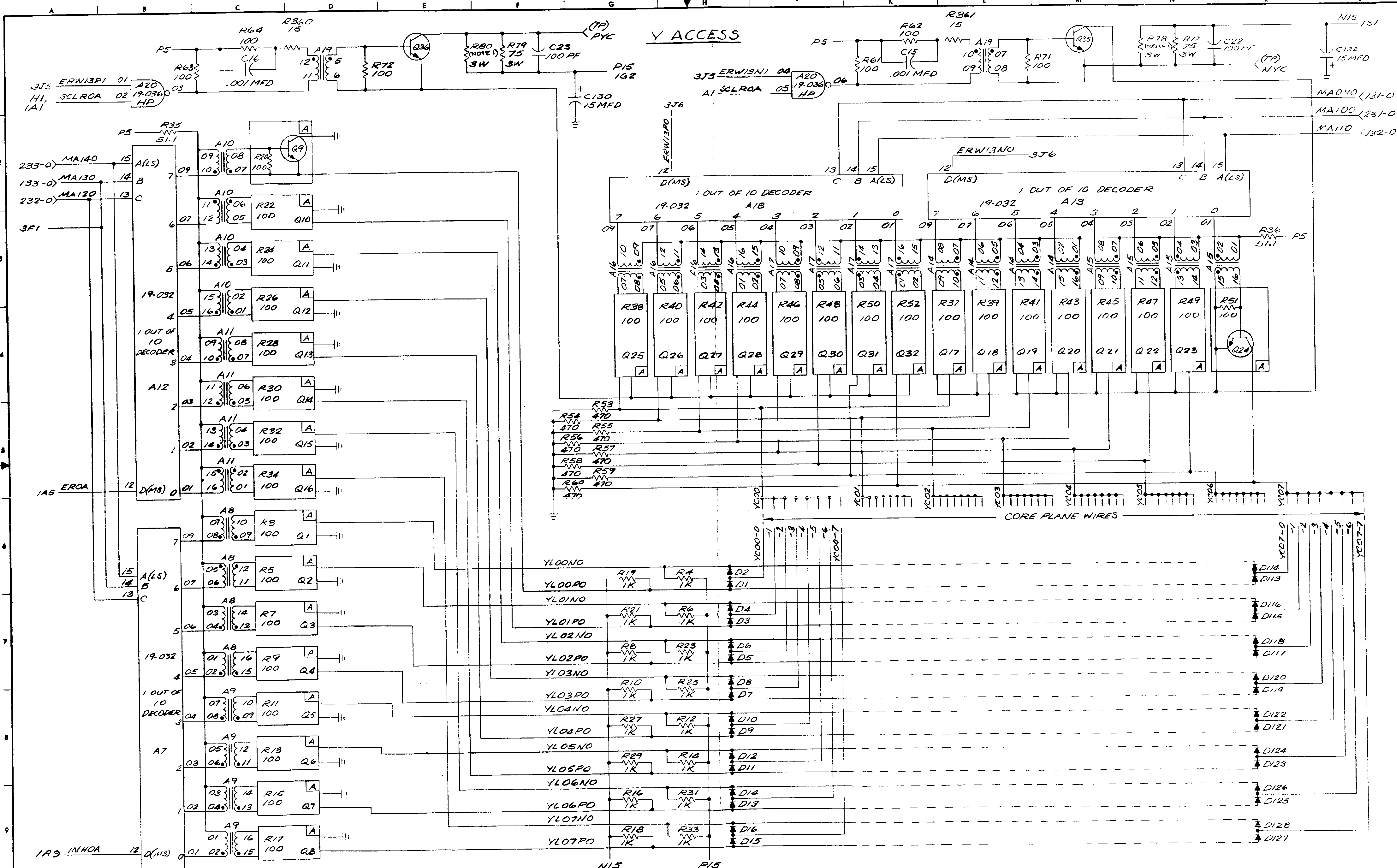
TITLE FUNCTIONAL SCHEMATIC SERIES 5 MEMORY

TASK NO. 03070

DWG NO. 02-211R03 D08

SHEET 1 OF 8

INTERDATA



NOTES
1. VALUE TO BE DETERMINED AT TIME OF MANUFACTURE.

REV.	DESCRIPTION	APPV'D
ISS. 1	REVISED PER LAB PROTOTYPE D. DWORZAK 3MAY 71	

NAME: D. DWORZAK

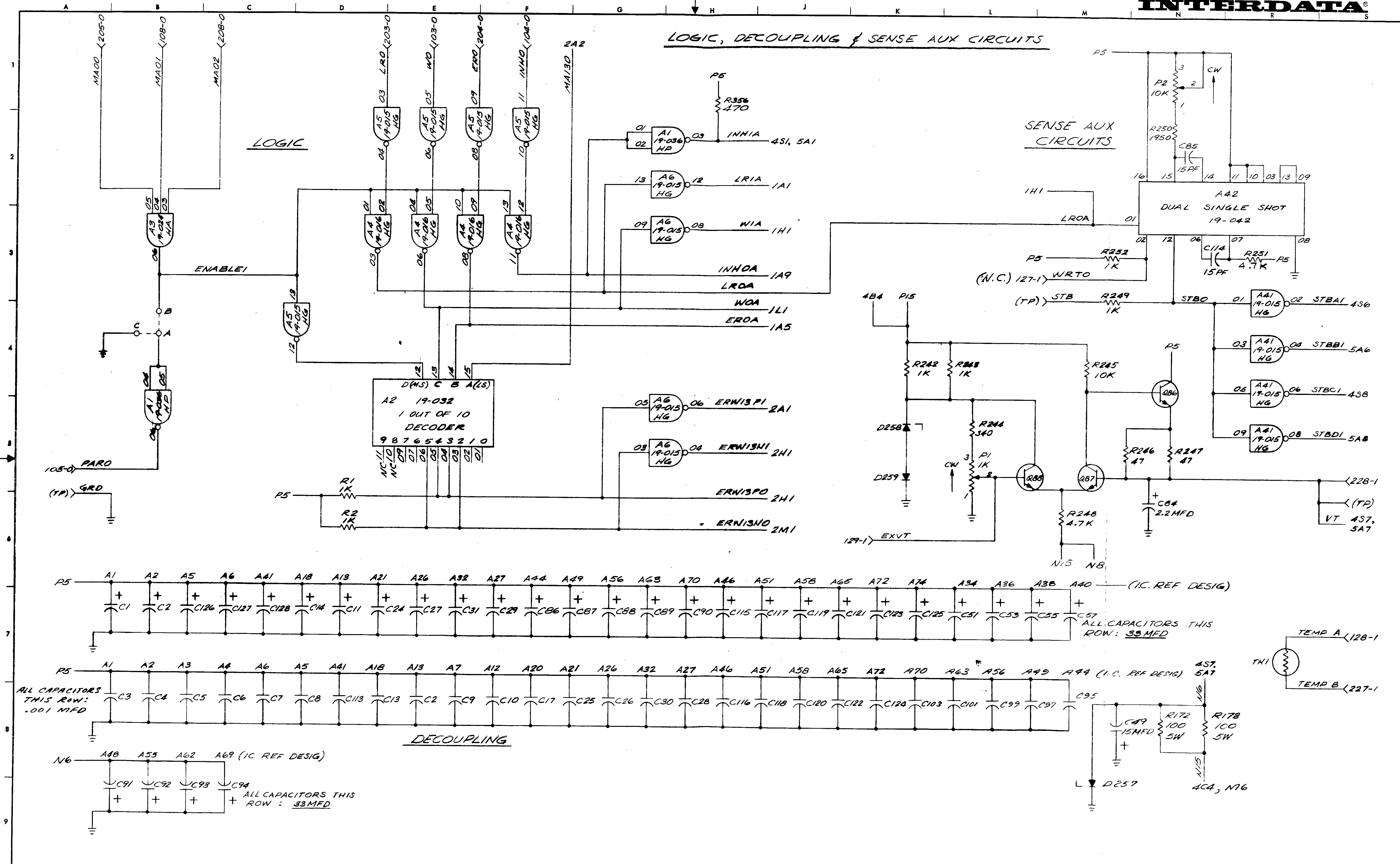
TITLE: FUNCTIONAL SCHEMATIC SERIES 5 MEMORY

03070

02-211R03 D08

SHEET 2-8

INTERDATA


LOGIC, DECOUPLING & SENSE AUX CIRCUITS
LOGIC
SENSE AUX CIRCUITS
DECOUPLING
MA00 205-0
MA01 108-0
MA02 208-0
LR0 203-0
W0 103-0
ER0 204-0
INH0 104-0
MA130 2A2
ENABLE1
PARO 105-0
(TP) GRD
A2 19-032 1 OUT OF 10 DECODER
R356 470
INHIA 4S1, 5A1
LR1A 1A1
W1A 1H1
INH0A 1A9
LR0A
W0A 1L1
ER0A 1A5
ERW13P1 2A1
ERW13N1 2H1
ERW13P0 2H1
ERW13N0 2M1
A42 DUAL SINGLE SHOT 19-042
P2 10K
R250 1950
C85 15PF
C114 15PF
R251 4.7K
R252 1K
(N.C.) 127-1 WRT0
(TP) STB
R249 1K
STB0
STBA1 4S6
STBB1 5A6
STBC1 4S8
STBD1 5A8
R242 1K
R243 1K
R245 10K
R244 340
P1 1K
R246 47
R247 47
R248 4.7K
C84 2.2MFD
D258
D259
Q86
Q87
Q88
228-1
(TP)
VT 4S7, 5A7
129-1 EXVT
N15 N8
(I.C. REF DESIG)
ALL CAPACITORS THIS ROW: 33 MFD
ALL CAPACITORS THIS ROW: .001 MFD
ALL CAPACITORS THIS ROW: 33MFD
TEMP A 128-1
TEMP B 227-1
TH1
C49 15MFD
R172 100 5W
R178 100 5W
D257
4C4, N16

NOTES

REV.	DESCRIPTION
ISS. 1	REVISED PER LAB PROTOTYPE D DWORZAK 3MAY '71

NAME: D. DWORZAK

TITLE: FUNCTIONAL SCHEMATIC SERIES 5 MEMORY

03070

DWG NO. 02-211 R03 D08

SHEET 3-8

INTERDATA®

SENSE-INHIBIT BIT 39-16

INHIA 3J2

STBA1 3S3

VT 3S6

N6 3N8

STBC1 3S4

REV	DESCRIPTION	APPVD
ISS. 1	REVISED PER LAB PROTOTYPE. D.DWORZAK 4MAY71	

NOTES

NAME	TITLE	DATE
R. F. CERO	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC SERIES 5 MEMORY

TASK NO. 03070

DWG NO. 02-211RC3 D08

SHEET OF 9-8

INTERDATA®

SENSE-INHIBIT BITS 0-8

INHIA

STBB1

STBD1

VT

N6

REV.	DESCRIPTION	APPVD
ISS. 1	REVISED PER LAB PROTOTYPE. D DWORZAK 4 MAY 71	

NOTES

NAME	TITLE	DATE
R. F. CERO	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

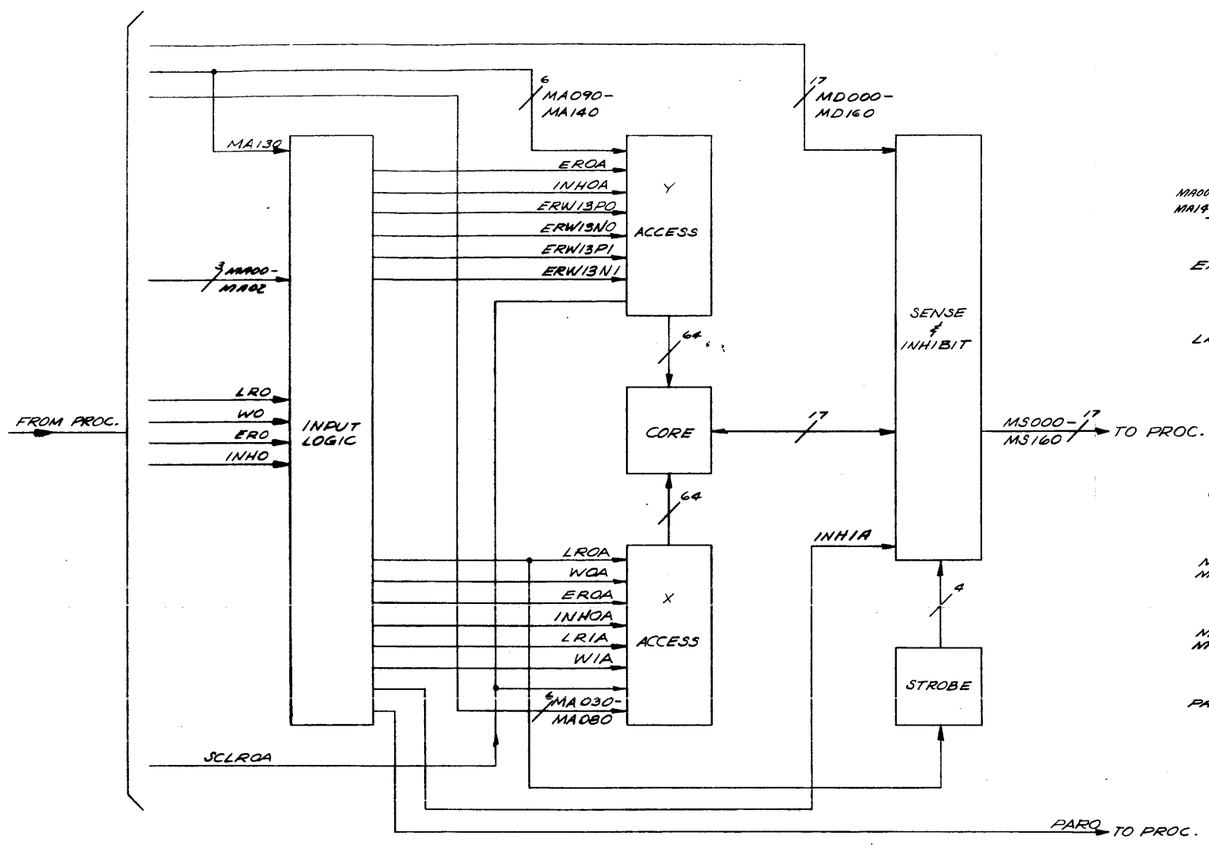
TITLE FUNCTIONAL SCHEMATIC SERIES 5 MEMORY

TASK NO. 03070

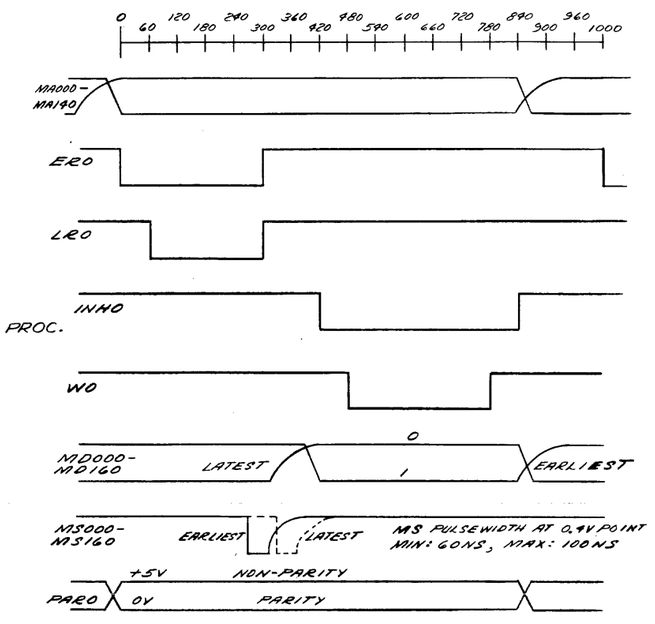
DRG NO. 02-211R0- D06

SHEET OF 5-8

BLOCK DIAGRAM



TIMING



TEST POINTS	LOCATION
NXC	1R1
PXC	1G1
NYC	2R1
PYC	2G1
GRD	3A6
LROA	1G2
STB	3L3
VT	3S6

BACK PANEL MAP

CONN. POS.:
MOTHER BD.: SERIES 5 MEMORY
VERT. POS.: HORIZONTAL POS.

CONN		1	2
1	41	P5	GND
	40	GND	GND
	39	P15	P15
	38	N15	N15
	37	MD150	MD160
	36	MD130	MD140
	35	MD110	MD120
	34	MD090	MD100
	33	MD070	MD080
	32	MD050	MD060
	31	MD030	MD040
	30	MD010	MD020
	29	EXVT	MD000
	28	TEMP A	VT
	27	WRTO	TEMP B
	26		
	25		
	24		
	23		
	22		
	21		
	20		
	19		
	18		
	17		
	16		
	15		
	14		
	13		
	12		
	11		
	10		MS000
	09	MS010	MS020
	08	MS030	MS040
	07	MS050	MS060
	06	MS070	MS080
	05	MS090	MS100
	04	MS110	MS120
	03	MS130	MS140
	02	MS150	MS160
	01	GND	GND
	00	P5	GND
0	41	P5	GND
	40	GND	GND
	39		
	38		
	37		
	36		
	35		
	34		
	33	MA130	MA140
	32	MA110	MA120
	31	MA090	MA100
	30	MA070	MA080
	29	MA050	MA060
	28		
	27	SCLROA	
	26		
	25		
	24		
	23		
	22		
	21		
	20		
	19		
	18		
	17		
	16		
	15		
	14		
	13		
	12		
	11		
	10	MA030	MA040
	09	MA020	MA021
	08	MA01	MA02
	07	MA010	MA011
	06	MA000	MA001
	05	PARO	MA00
	04	INHO	ERO
	03	WO	LRO
	02	P15	N15
	01	GND	GND
	00	P5	GND

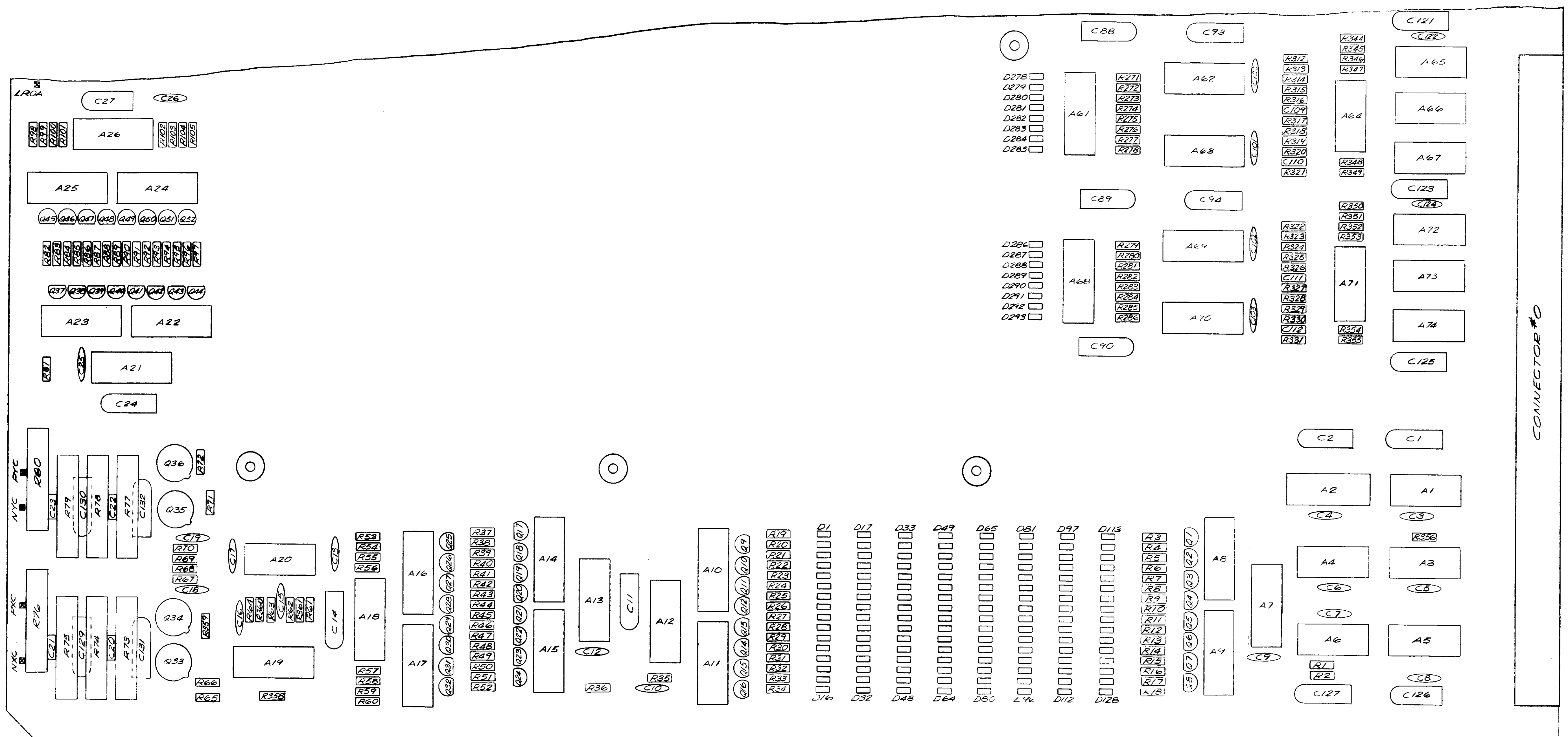
NOTES

REV.	DESCRIPTION	APPVD
ISS. 1	REVISED PER LAB PROTOTYPE. D. DWORZAK 2 MAY 71	

NAME: L. DWORZAK
TITLE / DATE: DRAFT; CHK; ENGR; DIR ENG

TITLE: FUNCTIONAL SCHEMATIC SERIES 5 MEMORY
DATA NO.: C3070
DWG NO.: 02-211RC3 D08
SHEET OF: 6-8

INTERDATA



COMPONENT	REFERENCE DESIGNATION
THERMISTOR	TH1
I.C.	A1 THRU A74
CAP.	C1 THRU 58, 60, 62, 64, 66, 68, 70, 72, 74, 76, 78, 80, 82, 84 THRU 132
RES	R1 THRU R361
TRANS	Q1 THRU Q88
DIODE	D1 THRU D293
POT.	P1 & P2

NOTES

REV.	DESCRIPTION	APPV'D
ISS. 1	REVISED PER LAB PROTOTYPE. R358 THRU R361 WERE NOT SPECIFIED. D. DWORZAK 4 MAY 71	

NAME	TITLE	DATE
D. DWORZAK	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

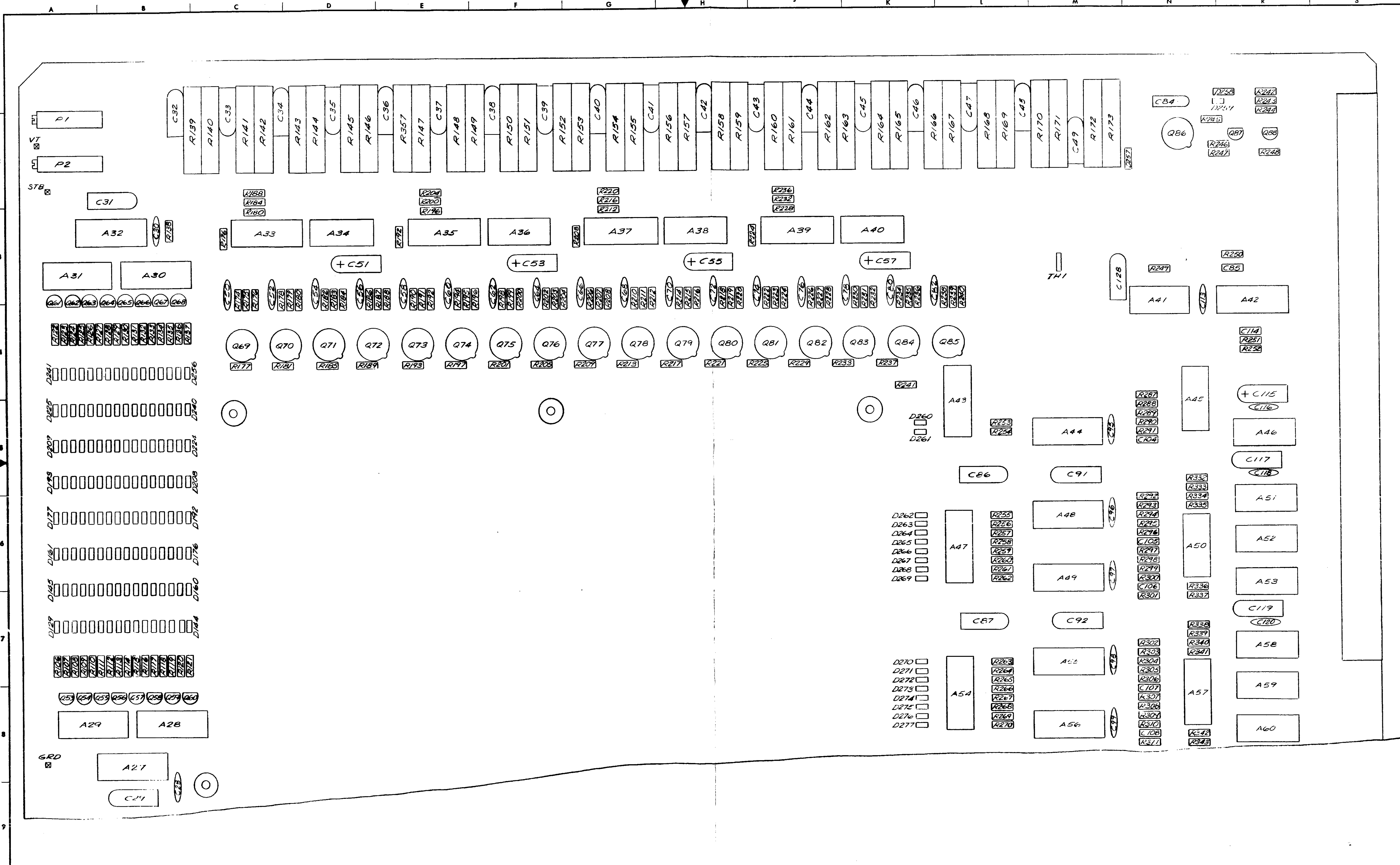
TITLE FUNCTIONAL SCHEMATIC SERIES 5 MEMORY

TASK NO. 03070

DWG NO. 02-211 RC3 D08

SHEET 7 OF 8

INTERDATA®



NOTES

REV.	DESCRIPTION	APPV'D
ISS. 1	REVISED PER LAB PROTOTYPE, D. DWORZAK 4 MAY 71	

NAME: D. DWORZAK
TITLE / DATE: DRAFT / CHK / ENGR / DIR ENG

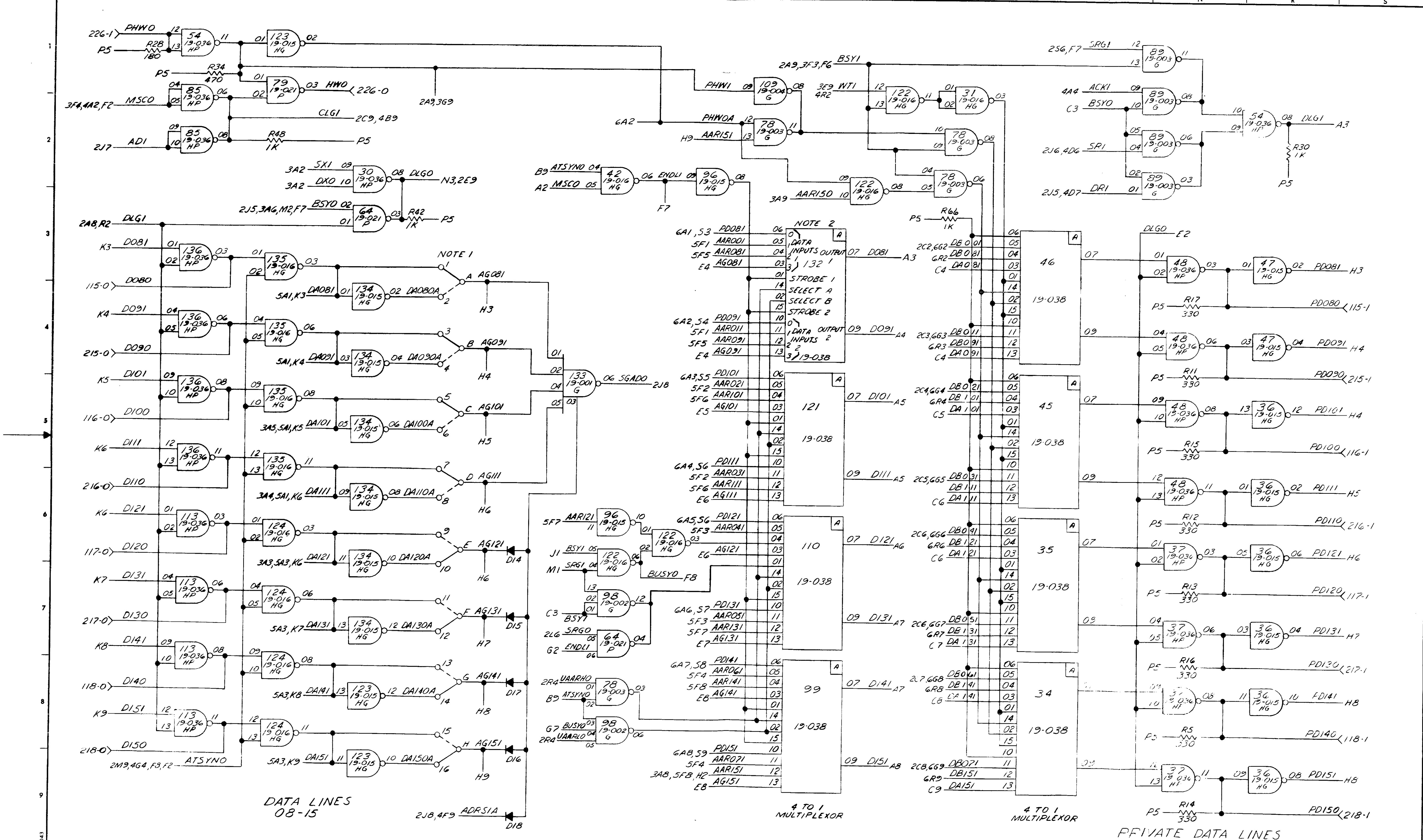
TITLE: FUNCTIONAL SCHEMATIC SERIES 5 MEMORY

03070

02-211R03 D05

SHEET 8 OF 8

INTERDATA®



NOTES 1. PREFERRED ADDRESS X'F0'

REVISIONS:			
AREA L3 A45 46, 34 & 35 PINS 6 & ? WERE N.C. CHANGED SHEETS 2,3,4 & 5			
C. J.	03124-01	18 JAN 72	R01
CHANGED SHEET 4			
C. J.	03124-02	18 JAN 72	R02

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
C J	CHK	10-?-71
	ENGR	
	SYS	
	DIR ENG	

TITLE NS SELECTOR CHANNEL

TASK NO. 03116

DWG NO. 02-232 R02D08

SHEET 1 OF 7

BRUNING 44 231 15043

INTERDATA®

DATA LINES 00-07

PRIVATE DATA LINES 00-07

LOAD/UNLOAD SEQUENCER

ADDRESS FF

NOTES

REVISIONS:
AREA K1, R65 WAS NOT SPEC.
C.J. | 03124-01 | 18 JAN 72 | R01

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: NS SELECTOR CHANNEL

TASK NO. 03116 | DWG NO. 02-232 R02 D08 | SHEET OF 2-7

INTERDATA®

CIRCUIT NOTES

MAP FOR EDX (END OF DATA XFER)

	WTO	WTI	
MCHO	000 SSX	100 SSX	(EVEN) AAR15O
MCHO	001 RBA	101 SREQ, SSX, LDB	(ODD) AAR15I
MCHI	011 CBSY	111 SREQ, LDB	(ODD) AAR15I
MCHI	010 CBSY	110 SREQ, LDB	(EVEN) AR15O

MAP FOR EMX (END MEM. XFER)

	WTO	WTI
MCHO	SREQ, SSX, LDB	RBA
MCHI	SREQ, SSX, LDB	CBSY

MAP FOR EBS (END BSY SET)

WTO	WTI
SREQ	SSX

BUFFER ACTIVE FF

BUSY FF

MUX/SELCH FF

WRITE FF

STATUS REQ FF

DATA XFER FF

BRANCH GATES

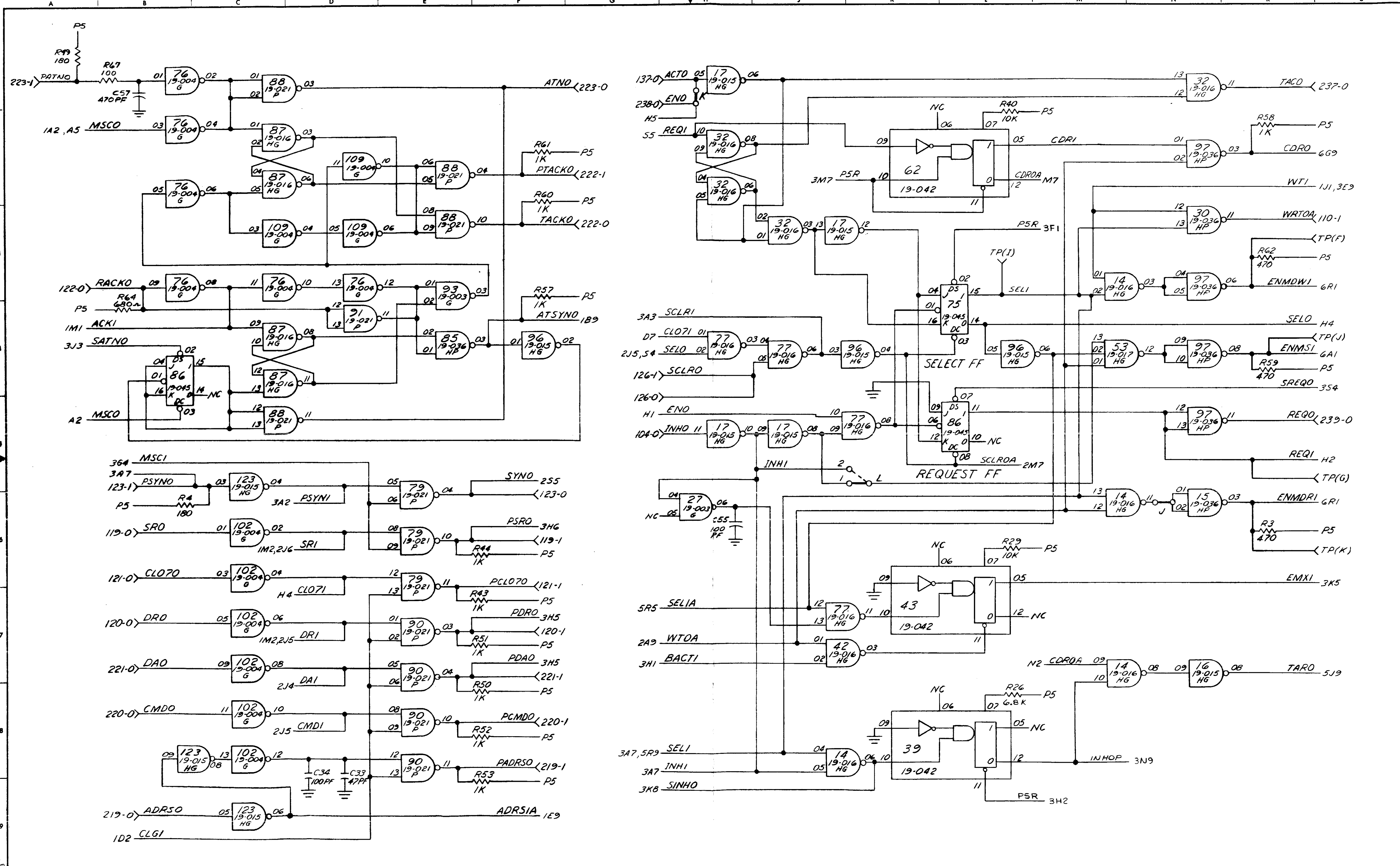
19-032 2 OF 10 DECODER

NOTES	REVISIONS: AREA F3 BSY1 WAS NOT SPEC TO A39 PIN3 OR 4L9, AREA A8 ALDBI WAS SPEC TO 57, AREA 56 A62 PIN 13 WAS ALDBI, AREA L THRU S9 A3, A27 & C56 WERE NOT SPEC. C.J. 03129-01 18 JAN 72 R01	NAME	TITLE	DATE
		W ZILLGER	DRAFT	10-5-71
			CHK	
			ENGR	
			DIR ENG	

TITLE: NS SELECTOR CHANNEL

TASK NO. 03116 DWG NO. 02-232R02D08 SHEET OF 3-7

INTERDATA®



NOTES

AREA A,B1 R67 & C57 WERE NOT SPEC.

C. J.		03124-02		18 JAN 72	R02

REVISIONS:
AREA B4, R64 WAS NOT SPEC; AREA L8,9 R26 WAS 10K
A39 PIN 11 WAS N.C., PIN 12 TO 3N9 WAS NOT SPEC;
AREA L3, A62 PIN 11 & A75 PIN2 WERE N.C.

C. J.		03124-01		18 JAN 72	R01

NAME	TITLE	DATE
N ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE NS SELECTOR CHANNEL

TASK NO. 03116

DWG NO. 02-232 R02D08

SHEET OF 4-7

INTERDATA®

AUXILIARY ADDRESS REGISTER FINAL ADDRESS REGISTER MATCH CIRCUIT

ADDRESS REGISTER

NOTES

REVISIONS:
A115, 116, 117, 118, 119, 120 & 130 PIN 13 WAS N.C., A131 PINS 12 & 13 WERE N.C.

C.J.	03124-01	18 JAN 72	R01

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: SELECTOR CHANNEL

TASK NO. 03116 | DWG NO. 02-2332 R02D08 | SHEET OF 5-7

BRUNING 44-231-15043

INTERDATA®

DATA REG HIGH

DATA BUFFER

DATA REG LOW

DATA BUFFER

4R4,H1 ENMS1

210-1 MS000 — 1H3,H2 PD081 — 1H2 PHWDA — 2H1 PDR000

109-1 MS010 — 1H4,H3 PD091 — 2H2 PDR010

209-1 MS020 — 1H4,H4 PD101 — 2H3 PDR020

108-1 MS030 — 1H5,H5 PD111 — 2H4 PDR030

208-1 MS040 — 1HG,HG PD121 — 2H5 PDR040

107-1 MS050 — 1H7,H7 PD131 — 2H6 PDR050

207-1 MS060 — 1H7,H8 PD141 — 2H7 PDR060

106-1 MS070 — 1H8,H9 PD151 — 2H8 PDR070

3G8 LDRH0

3G9 LDRH1

R7 470Ω — P5

MD000 (229-1) — DB001 1K3

MD010 (130-1) — DB011 1K4

MD020 (230-1) — DB021 1K5

MD030 (131-1) — DB031 1K5

MD040 (231-1) — DB041 1K6

MD050 (132-1) — DB051 1K7

MD060 (232-1) — DB061 1K8

MD070 (133-1) — DB071 1K9

LDB1 R9,3S7

CDR0 R9,4R2

A1 ENMS1

206-1 MS080 — A1 PD081

105-1 MS090 — A2 PD091

205-1 MS100 — A3 PD101

104-1 MS110 — A4 PD111

204-1 MS120 — A5 PD121 — 3A1 PDR120

103-1 MS130 — AG PD131 — 3A1 PDR130

203-1 MS140 — A7 PD141 — 3A1 PDR140

102-1 MS150 — AB PD151 — 3A1 PDR150

3J9 LDRL0

R35 470Ω — P5

ENMDR1 4RG

ENMDW1 4R3

MD080 (233-1) — DB081 1K3

MD090 (134-1) — DB091 1K4

MD100 (234-1) — DB101 1K5

MD110 (135-1) — DB111 1K6

MD120 (235-1) — DB121 1K6

MD130 (136-1) — DB131 1K7

MD140 (236-0) — DB141 1K8

MD150 (137-1) — DB151 1K9

LDB1 G9

CDR0 G9

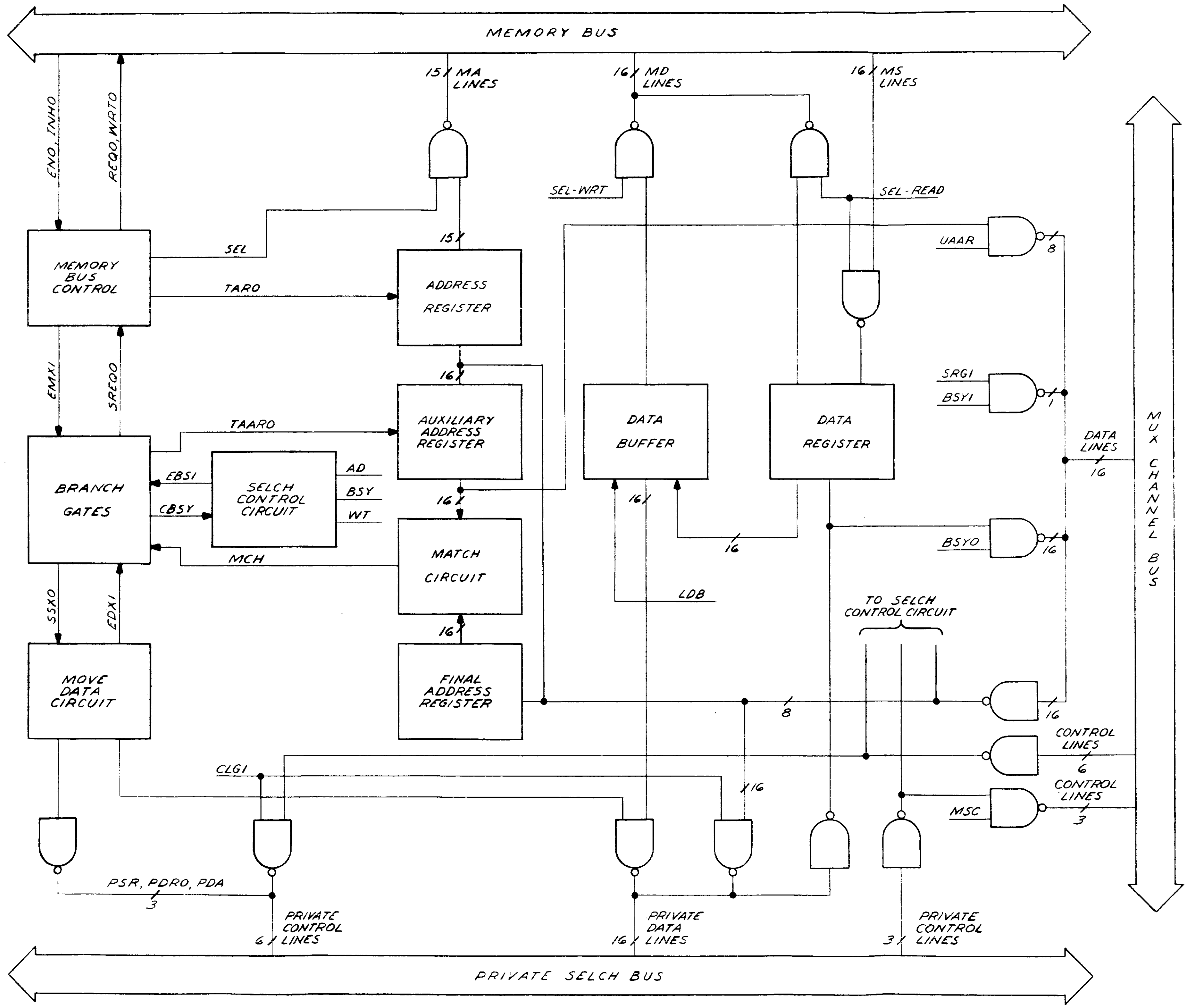
NOTES

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: NS SELECTOR CHANNEL

YASK NO. 03116 — ENG NO. 02-232 R02D08 — SHEET OF 6-7

BRUNING 44231 15043



BACK PANEL PIN INDEX

MNEM.	LOC.	MNEM.	LOC.
ACTO	4H1	MD130	6R6
ADRSO	4B8	MD140	6R7
ATNO	4F1	MD150	6R8
CLO70	4B6	MS000	6A1
CMDO	4B8	MS010	6A2
D000	2A1	MS020	6A3
D010	2A2	MS030	6A4
D020	2A3	MS040	6A5
D030	2A4	MS050	6A6
D040	2A5	MS060	6A7
D050	2A6	MS070	6A8
D060	2A7	MS080	6H1
D070	2A8	MS090	6H2
D080	1A3	MS100	6H3
D090	1A4	MS110	6H4
D100	1A5	MS120	6H5
D110	1A6	MS130	6H6
D120	1A6	MS140	6H7
D130	1A7	MS150	6H8
D140	1A8	PADRSO	4F8
D150	1A8	PATNO	4B1
DAO	4B7	PCLO70	4F6
DRO	4B7	PCMDO	4F8
ENO	4H1	PD000	2F1
HWO	1D1	PD010	2F2
INHO	4H5	PD020	2F3
MA000	5R1	PD030	2F4
MA010	5R1	PD040	2F5
MA020	5R2	PD050	2F6
MA030	5R2	PD060	2F7
MA040	5R3	PD070	2F8
MA050	5R3	PD080	1R4
MA060	5R4	PD090	1R4
MA070	5R4	PD100	1R5
MA080	5R5	PD110	1R6
MA090	5R6	PD120	1R7
MA100	5R6	PD130	1R7
MA110	5R7	PD140	1R8
MA120	5R7	PD150	1R9
MA130	5R8	PDAO	4F7
MA140	5R8	PDRO	4F8
MD000	6G1	PHWO	1A1
MD010	6G2	PSRO	4F6
MD020	6G3	PSYNO	4B5
MD030	6G4	PTACKO	4F2
MD040	6G5	RACKO	4B3
MD050	6G6	REQO	4R5
MD060	6G7	SCLRO	4H4
MD070	6G8	SRO	4B6
MD080	6R1	SYNO	4F5
MD090	6R2	TACKO	4H3
MD100	6R3	TACO	4R1
MD110	6R4	WRTOA	4R3
MD120	6R5		

BACK PANEL MAP

ROW 1	ROW 2	TERM NO.	CONN
P5	GND	41	
GND	GND	40	
		39	
		38	
MD150		37	
MD130	MD140	36	
MD110	M120	35	
MD090	MD100	34	
MD070	MD080	33	
MD050	MD060	32	
MD030	MD040	31	
MD010	MD020	30	
	MD000	29	
		28	
		27	
SCLRO	PHWO	26	
		25	
		24	
PSYNO	PATNO	23	
	PTACKO	22	
PCLO70	PDAO	21	1
PDRO	PCMDO	20	
PSRO	PADRSO	19	
PD140	PD150	18	
PD120	PD130	17	
PD100	PD110	16	
PD080	PD090	15	
PD060	PD070	14	
PD040	PD050	13	
PD020	PD030	12	
PD000	PD010	11	
WRTOA	MS000	10	
MS010	MS020	09	
MS030	MS040	08	
MS050	MS060	07	
MS070	MS080	06	
MS090	MS100	05	
MS110	MS120	04	
MS130	MS140	03	
MS150		02	
GND	GND	01	
P5	GND	00	
P5	GND	41	
GND	GND	40	
	REQO	39	
	ENO	38	
ATCO	TACO	37	
		36	
		35	
		34	
MA130	MA140	33	
MA110	MA120	32	
MA090	MA100	31	
MA070	MA080	30	
MA050	MA060	29	
		28	
		27	
SCLRO	HWO	26	
		25	
		24	
SYNO	ATNO	23	
RACKO	TACKO	22	
CLO70	DAO	21	
DRO	CMDO	20	0
SRO	ADRSO	19	
D140	D150	18	
D120	D130	17	
D100	D110	16	
D080	D090	15	
D060	D070	14	
D040	D050	13	
D020	D030	12	
D000	D010	11	
MA030	MA040	10	
MA020		09	
		08	
MA010		07	
MA000		06	
		05	
INHO		04	
		03	
		02	
GND	GND	01	
P5	P5	00	

TEST POINT INDEX

DESIG	MNEM	LOC.
A	ADI	2L6
B	WTI	3G5
C	SXI	3G6
D	MSCO	3G4
E	BSYO	3G3
F	ENMDWI	4S3
G	REQI	4S5
H	DXI	3G7
I	SELI	4L3
J	ENMSI	4S4
K	ENMDRI	4S6

SUPPORT INFORMATION

TITLE	BOARD NO.
NS SELCH	35-283

NOTES

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-13-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: NS SELECTOR CHANNEL

TASK NO. 03116

DWG NO. 02-232 R02D08

SHEET 7 OF 7

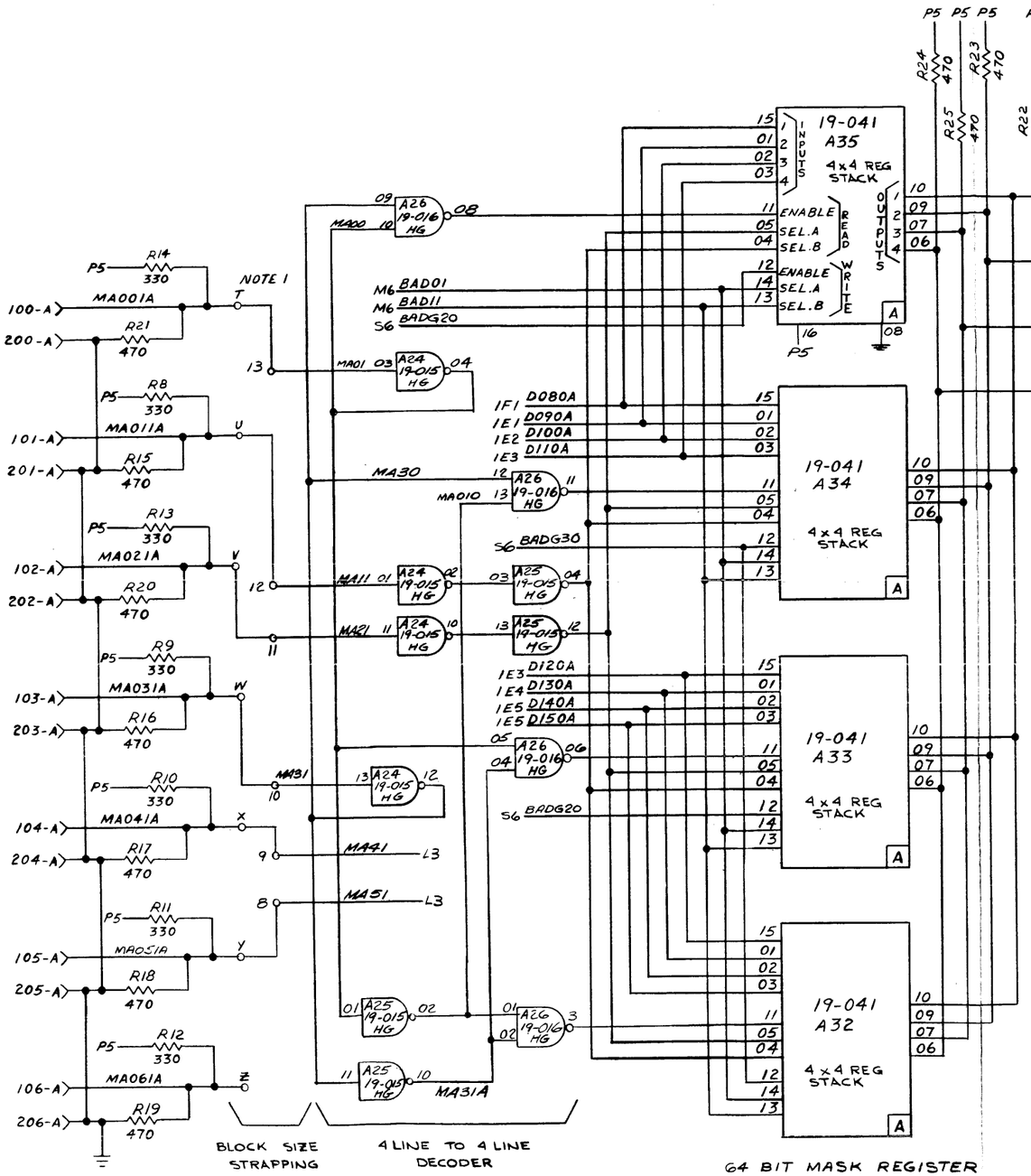
INTERDATA®

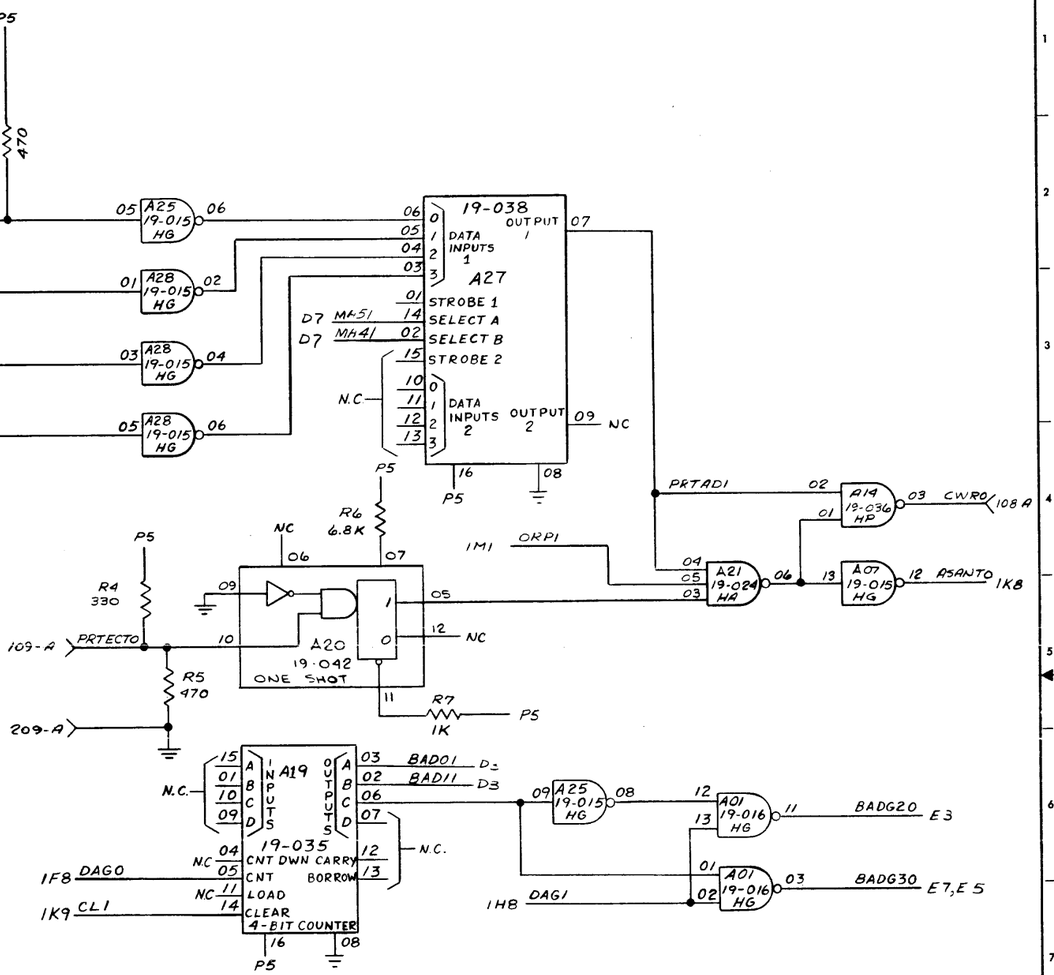
NOTES:
1. PREFERRED ADDRESS X'AE'

NAME	TITLE	DATE
L. VALENTY	DRAFT	9-10-71
G.J. HOMEFIELD	CHK	1-7-72
D.F. RANKENBERGER	ENGR	1-14-72
D.W. YOUNG	SYS	1-14-72
R.E. JONES	DIR ENG	1-17-72

TITLE FUNCTIONAL SCHEMATIC
NS -MEMORY PROTECT
TASK NO. 03123
DWG NO. 02-236 D08
SHEET OF 1-3

INTERDATA®





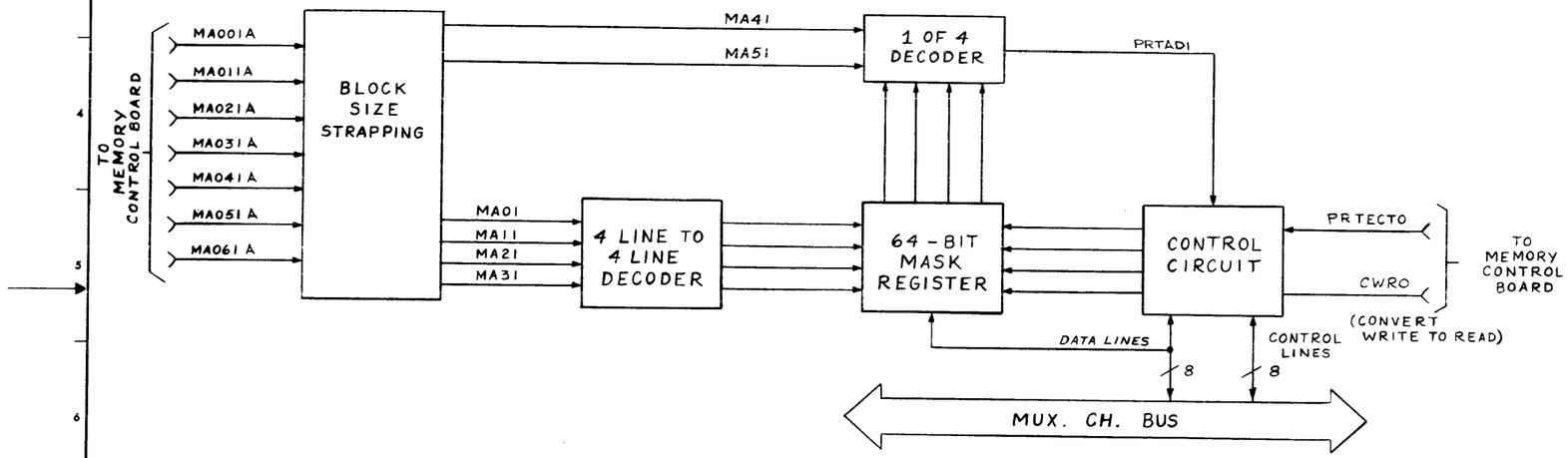
BLOCK SIZE	MA01 (13)	MA11 (12)	MA021 (11)	MA031 (10)	MA041 (9)	MA051 (8)
512 BYTES	MA011A (U)	MA021A (V)	MA031A (W)	MA041A (X)	MA051 (Y)	MA061A (Z)
1,024 BYTES	MA001A (T)	MA011A (U)	MA021A (V)	MA031A (W)	MA041A (X)	MA051A (Y)
2,048 BYTES	SEE NOTE 2	MA001A (T)	MA011A (U)	MA021A (V)	MA031A (W)	MA041A (X)

TABLE 1. BLOCK SIZE STRAPPING

NOTES:
1. STRAPPED FOR 1K BYTE BLOCKS
2. FOR THE 2K BYTE OPTION MA01 (13) MUST BE TIED TO GROUND

NAME	TITLE	DATE
L VALENTY	DRAFT	9-14-71
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
NS - MEMORY PROTECT
TASK NO. 03123
DWG NO. 02-236 D08
SHEET 2-3



BLOCK DIAGRAM

HORIZ. POS	VERTICAL POSITION 1	2
00	MA001A	GND
01	MA011A	GND
02	MA021A	GND
03	MA031A	GND
04	MA041A	GND
05	MA051A	GND
06	MA061A	GND
07		GND
08	CWRO	GND
09	PROTECTO	GND

CABLE MAP

HORIZ. POS	VERTICAL POSITION 1	2
00	P5	GND
01	GND	GND
02		
03		
04		
05		
06		
07		
08		
09		
10		
11		
12		
13		
14		
15	D080	D090
16	D100	D110
17	D120	D130
18	D140	D150
19	SRO	ADRSO
20	DX20	CMDO
21	CLO70	DAO
22	RACKO	TACKO
23	SYNO	ATNO
24		
25		
26	SCLRO	HWO
27		
28		
29		
30		
31		
32		
33		
34		
35		
36		
37		
38		
39		GND
40	GND	GND
41	P5	GND

BACK PANEL MAP

NOTES

NAME	TITLE	DATE
L.VALENTY	DRAFT	9-14-71
	CHK	
	ENGR	
	DIR ENG	

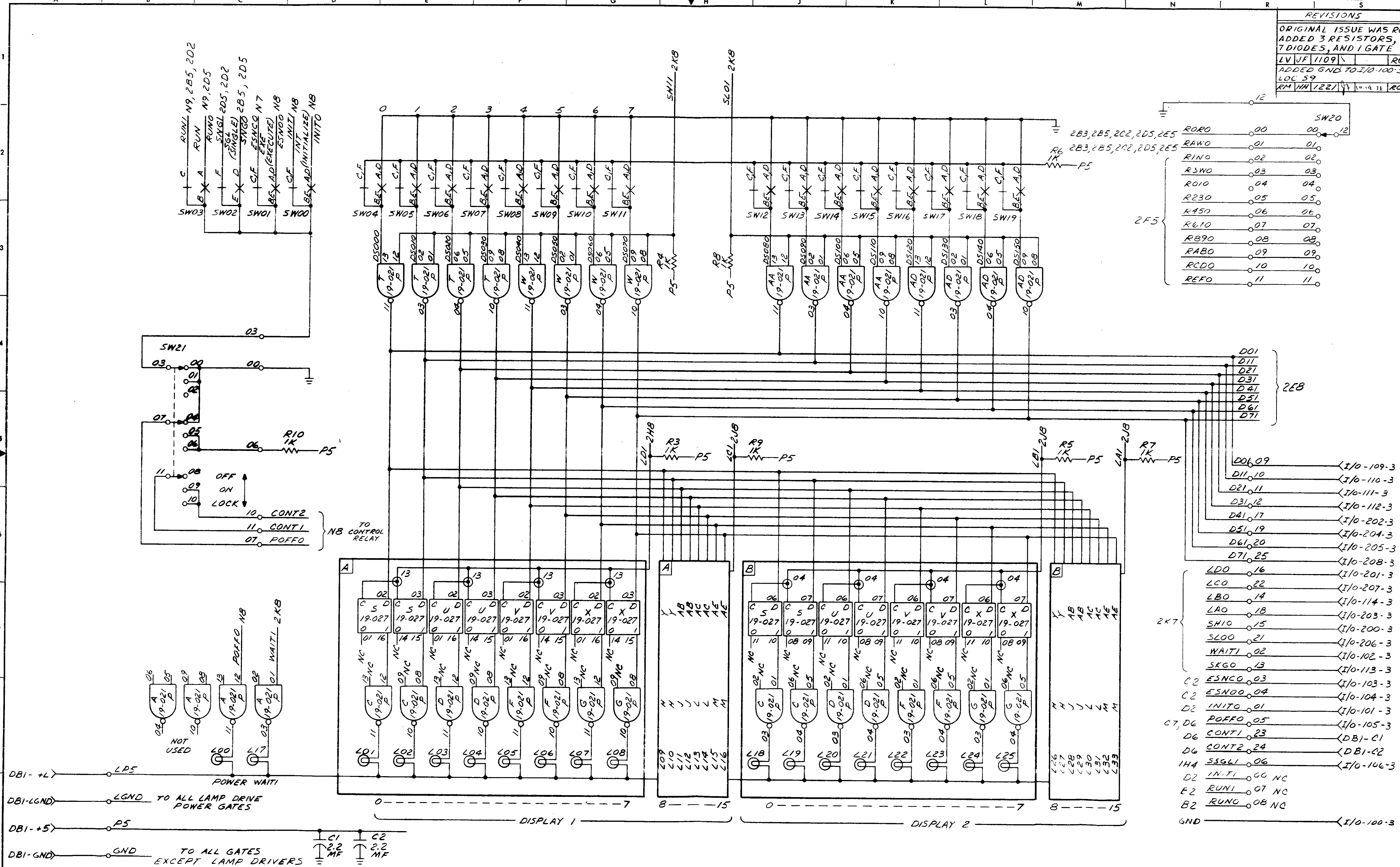
TITLE FUNCTIONAL SCHEMATIC
NS - MEMORY PROTECT

TASK NO. 03123
DRG NO. 02-236 DOB

SHEET OF 3 - 3

INTERDATA®

REVISIONS			
ORIGINAL ISSUE WAS R01 ADDED 3 RESISTORS, 7 DIODES, AND 1 GATE			
LV	JF	1109	R02
ADDED GND TO I/O-100-3 LOC S9			
RM	HH	1221	R03



NOTES

NAME	TITLE	DATE
B. W. SATHMARY	ENGR	
M. FUCHS		
R. E. JONES	DIR ENG	

TITLE SCHEMATIC DISPLAY PANEL (NS1)

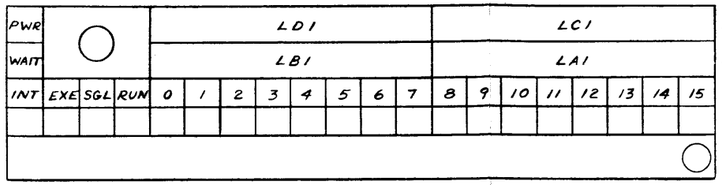
TASA NO. 03116

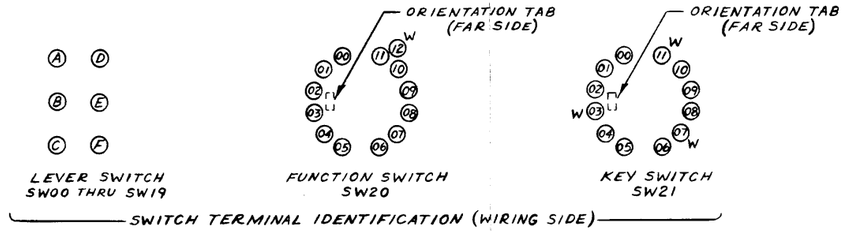
DWG NO. 09-051R03D08

SHEET 1 OF 2

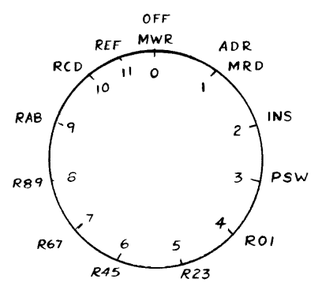
INTERDATA®

FRONT PANEL LAYOUT





STATUS													
RUN	OFF WRT RORO	ADRS RD RAWO	SINGLE	MODE	0	1	2	3	4	5	6	7
0	0	0	0	HALT	1	1	0	0	X	X	X	X
0	0	0	1	HALT	1	1	0	0	X	X	X	X
0	0	1	0	ADR	0	0	1	1	0	0	0	0
0	0	1	1	MRD	0	0	1	0	0	0	0	0
0	1	0	0	HALT	1	1	0	0	0	0	0	0
0	1	0	1	MWR	0	0	0	1	0	0	0	0
0	1	1	0									
0	1	1	1									
1	0	0	0	RUN	1	0	0	0	X	X	X	X
1	0	0	1	VAR	0	1	0	0	X	X	X	X
1	0	1	0	ADR	0	0	1	1	0	0	0	0
1	0	1	1	MRD	0	0	1	0	0	0	0	0
1	1	0	0	RUN	1	0	0	0	0	0	0	0
1	1	0	1	MWR	0	0	0	1	0	0	0	0
1	1	1	0									
1	1	1	1									
				OFF					0	0	0	0
				INS					0	0	1	0
				PSW					0	1	0	0
				0/1					1	0	0	0
				2/3					1	0	0	1
				4/5					1	0	1	0
				6/7					1	0	1	1
				8/9					1	1	0	0
				A/B					1	1	0	1
				C/D					1	1	1	0
				E/F					1	1	1	1



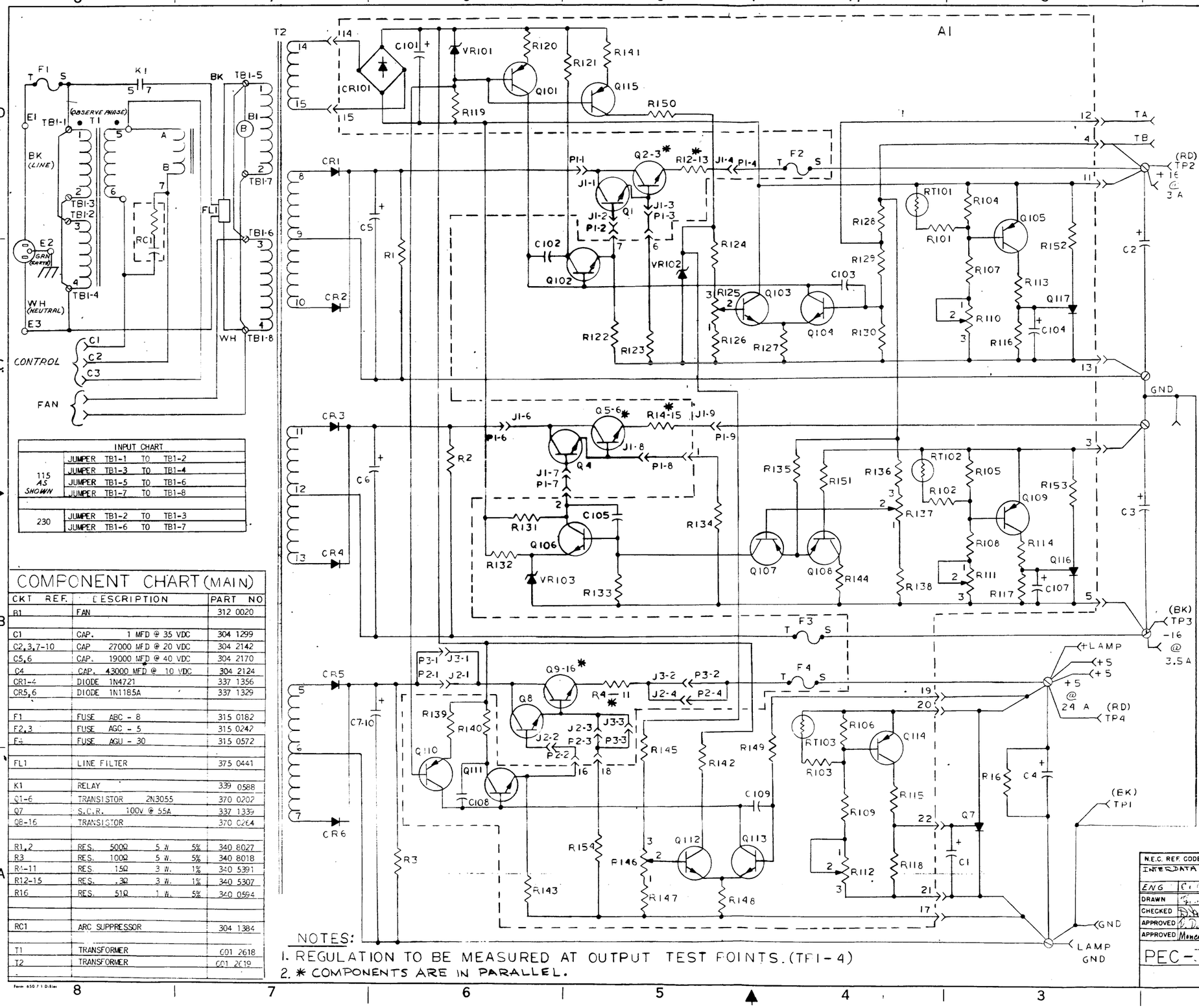
FRONT VIEW ROTARY

NOTES

NAME	TITLE	DATE
L VALENTY	DRAFT	28JUL71
	CHK	
	ENGR	
	DIR ENG	

TITLE SCHEMATIC
DISPLAY PANEL (NS1)
TASK NO. 03116
DWG NO. 09-051R03D08
SHEET OF 2-2

BRUNING 44231 15043



INPUT CHART			
115 AS SHOWN	JUMPER	TB1-1	TO TB1-2
	JUMPER	TB1-3	TO TB1-4
	JUMPER	TB1-5	TO TB1-6
	JUMPER	TB1-7	TO TB1-8
230	JUMPER	TB1-2	TO TB1-3
	JUMPER	TB1-6	TO TB1-7

COMPONENT CHART (MAIN)

CKT REF.	DESCRIPTION	PART NO
B1	FAN	312 0020
C1	CAP. 1 MFD @ 35 VDC	304 1299
C2,3,7-10	CAP 27000 MFD @ 20 VDC	304 2142
C5,6	CAP. 19000 MFD @ 40 VDC	304 2170
C4	CAP. 43000 MFD @ 10 VDC	304 2124
CR1-4	DIODE 1N4721	337 1356
CR5,6	DIODE 1N1185A	337 1329
F1	FUSE ABC - 8	315 0182
F2,3	FUSE AGC - 5	315 0242
F4	FUSE AGU - 30	315 0572
FL1	LINE FILTER	375 0441
K1	RELAY	339 0588
Q1-6	TRANSISTOR 2N3055	370 0202
Q7	S.C.R. 100V @ 55A	337 1339
Q8-16	TRANSISTOR	370 0264
R1,2	RES. 500Ω 5 W. 5%	340 8027
R3	RES. 100Ω 5 W. 5%	340 8018
R4-11	RES. 15Ω 3 W. 1%	340 5391
R12-15	RES. .3Ω 3 W. 1%	340 5307
R16	RES. 51Ω 1 W. 5%	340 0594
RC1	ARC SUPPRESSOR	304 1384
T1	TRANSFORMER	C01 2618
T2	TRANSFORMER	C01 2619

COMPONENT CHART - A1

CKT. REF.	DESCRIPTION	PART NO.
C101	CAP. 1500 MFD @ 25 VDC	304 1511
C102,103,108,109	CAP. .0022 MFD @ 100 VDC	304 1048
C104,107	CAP. 1 MFD @ 35 VDC	304 1299
C105	CAP. .015 MFD @ 100 VDC	304 0977
CR101	DIODE BRIDGE 100V @ 1.5A	337 1675
Q101,110,115	TRANSISTOR 2N4036	370 0163
Q102-104,106,111,	TRANSISTOR 2N1613 SPL	370 0072
Q112,113	TRANSISTOR 2N1613 SPL	370 0072
Q105,107-109,114	TRANSISTOR 2N3133	370 0144
Q116,117	S.C.R. 7A @ 150V	337 1154
R101-103	RES. 425Ω 1/2 W. 1%	340 5907
R104-106	RES. 225Ω 1/2 W. 1%	340 5921
R107,108	RES. 1.8KΩ 1/2 W. 1%	340 5920
R109	RES. 700Ω 1/2 W. 1%	340 5992
R110,111	POT. 5KΩ 3/4 W. 10%	341 0686
R112	POT. 2KΩ 3/4 W. 10%	341 0685
R113,114	RES. 43Ω 1/2 W. 5%	340 0120
R115	RES. 20Ω 1/2 W. 5%	340 0107
R116-118,127,139	RES. 510Ω 1/2 W. 5%	340 0146
R119	RES. 510Ω 2 W. 5%	340 0841
R120	RES. 750Ω 1/2 W. 5%	340 0150
R121	RES. 390Ω 1/2 W. 5%	340 0143
R122	RES. 3900Ω 1/2 W. 5%	340 0167
R123,132,151	RES. 1800Ω 1/2 W. 5%	340 0159
R124	RES. 562Ω 1/2 W. 1%	340 6229
R125	POT. 500Ω 3/4 W. 10%	341 0656
R126	RES. 1250Ω 1/2 W. 1%	340 5915
R128	RES. 550Ω 1/2 W. 1%	340 5913
R129	RES. 560Ω 1/2 W. 1%	340 5923
R130	RES. 511Ω 1/2 W. 1%	340 5975
R131	RES. 910Ω 1/2 W. 5%	340 0152
R133,144	RES. 2400Ω 1/2 W. 5%	340 0162
R134	RES. 1KΩ 1/2 W. 5%	340 0153
R136,138	RES. 2.5KΩ 1/2 W. 1%	340 0474
R137	POT. 1KΩ 3/4 W. 10%	341 0660
R140	RES. 240Ω 3 W. 1%	340 5101
R141	RES. 160Ω 1/2 W. 5%	340 0134
R142	RES. 3.9KΩ 1 W. 5%	340 0639
R143	RES. 1.6KΩ 1/2 W. 5%	340 0158
R145	RES. 301Ω 1/2 W. 1%	340 5970
R146	POT. 200Ω 3/4 W. 10%	341 0658
R147	RES. 402Ω 1/2 W. 1%	340 5972
R148	RES. 30Ω 1/2 W. 5%	340 0144
R149	RES. 270Ω 1/2 W. 5%	340 0137
R150	RES. 70Ω 1 W. 5%	340 0617
R152,153	RES. .5Ω 3W 1%	340 5087
R154	RES. 620Ω 1/2 W 5%	340 0148
RT101-103	THERMISTOR 1000Ω @ 25° C	369 0014
R135	RES. 3.3Ω 1/2 W 5%	340 0165
VR101,103	ZENER 1N751A 5.1V 5%	337 1072
VR102	ZENER 1N937A 9.0V 5%	337 1018

NOTES:
1. REGULATION TO BE MEASURED AT OUTPUT TEST POINTS. (TP1-4)
2. * COMPONENTS ARE IN PARALLEL.

	850 0050	8-10-71 JQ
	ENG. LEVEL	DATE JST

N.E.C. REF. CODE
INTERDATA APPROVAL:

ENG		
DRAWN		7-6-71
CHECKED		7-26-71
APPROVED		8-9-71
APPROVED	Moneysmith	8-9-71

PEC-3560

NORTH ELECTRIC COMPANY
POWER EQUIPMENT DIV. GALION, OHIO USA

NS POWER SUPPLY
SCHEMATIC
NORTH ELECTRIC #4391966

CODE IDENT. NO.	SIZE	
	D	34-012R01D08
SCALE NONE	UNIT WEIGHT	SHEET / OF

[4391966]

AREA G & K4. JUMPERS SHOWN ON TERM C2 WAS ON C3. SHT 2 AREA F3 17-166 WAS 17-167. AREA L12 DELETED MATE FOR CABLE B.

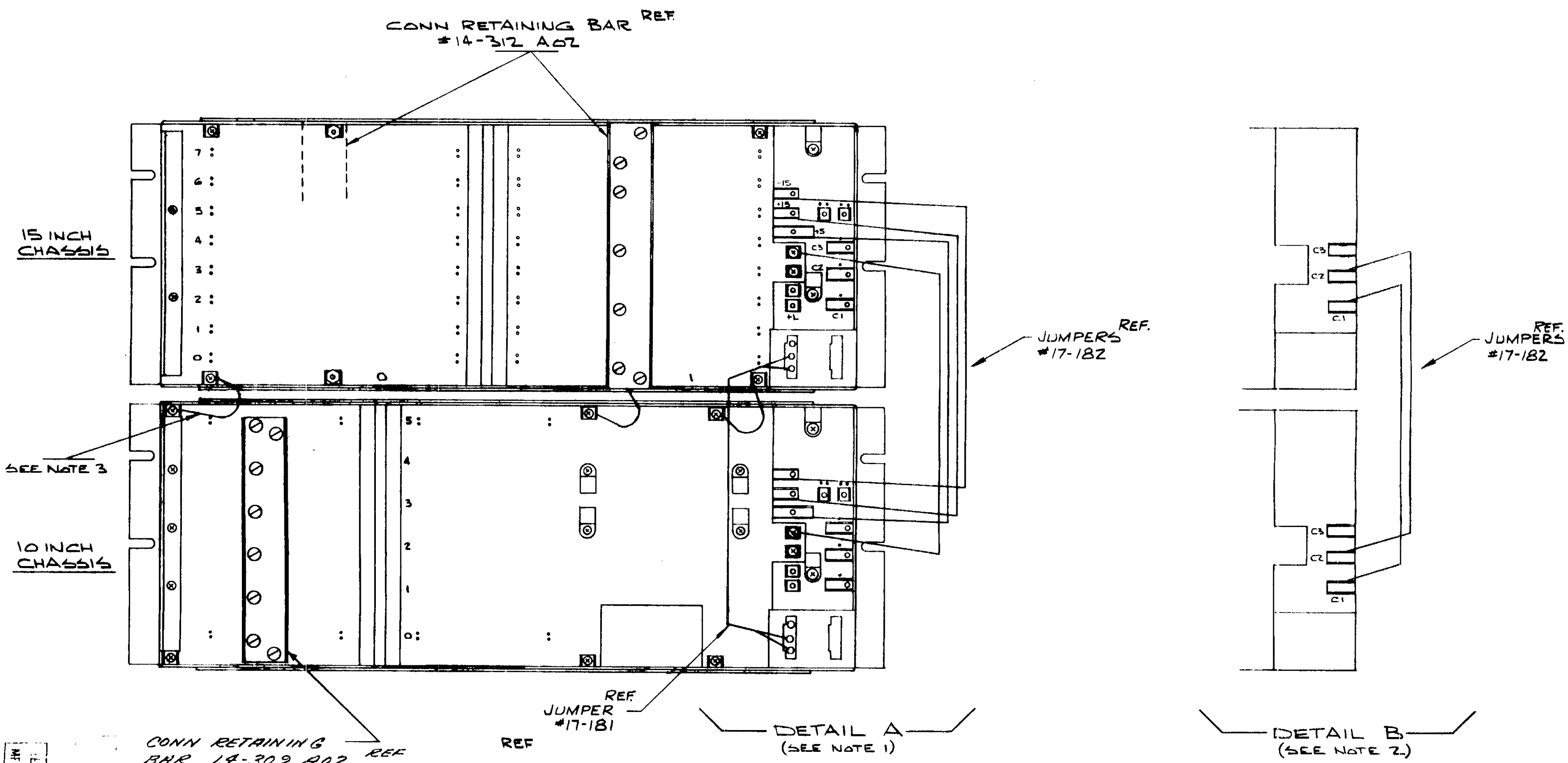
BW	RW	03116-45		11/31/72	ISS.

AREA J THRU M-14. DELETED RETAINING BAR 14-309 A02

RC	BW	03116-67			R01

NOTES:

1. WHEN POWERING TWO CHASSIS FROM ONE POWER SUPPLY USE JUMPER #17-182 4 REQ'D & FAN JUMPER #17-181 1 REQ'D PER DETAIL A
2. WHEN CONNECTING POWER SUPPLIES IN PARALLEL USE JUMPER #17-182 PER DETAIL B
3. ADJACENT CHASSIS MUST USE GROUND JUMPERS #17-076 F00 AS STATED BELOW
   a. ADJACENT 15 IN CHASSIS TO USE 4 JUMPERS
   b. CHASSIS ADJACENT TO 10 IN CHASSIS TO USE 3 JUMPERS.

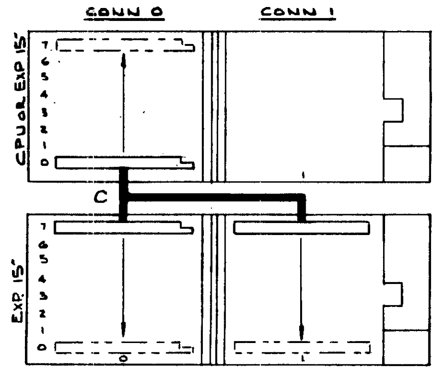


REAR VIEW

CABLE INFORMATION 4S

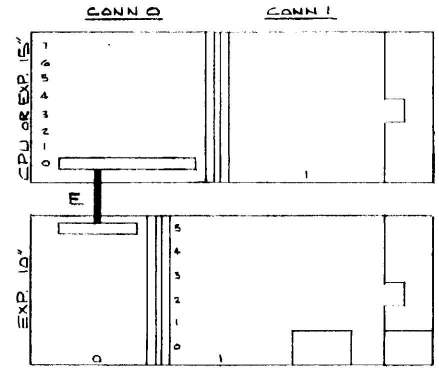
DWG. NO. 01-051R01C12 SHEET 1 OF 2

INTERDATA



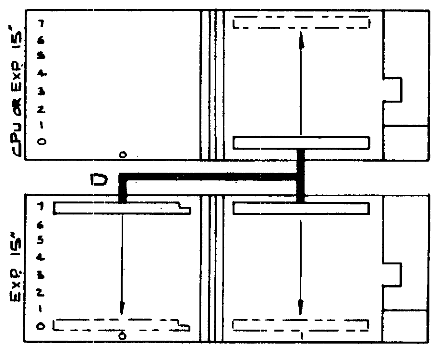
CABLE C : 17-164

USED TO CONNECT TWO ADJACENT 15 IN. CHASSIS IN AN ENTIRELY NORMAL WAY. THE LOWER CHASSIS BUS APPEARS EXACTLY AS ON THE TOP CHASSIS.



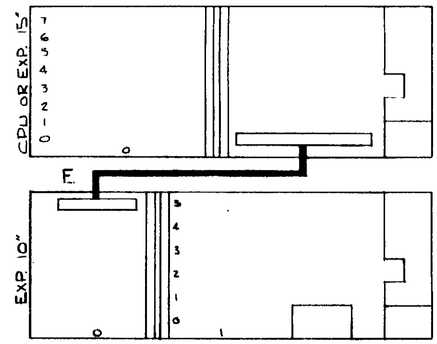
CABLE E : 17-166

USED TO CONNECT A 15 IN CHASSIS FROM CONN 00 TO A 10 IN CHASSIS ONE OR TWO CHASSIS POSITIONS BELOW. (TWISTED PAIR)



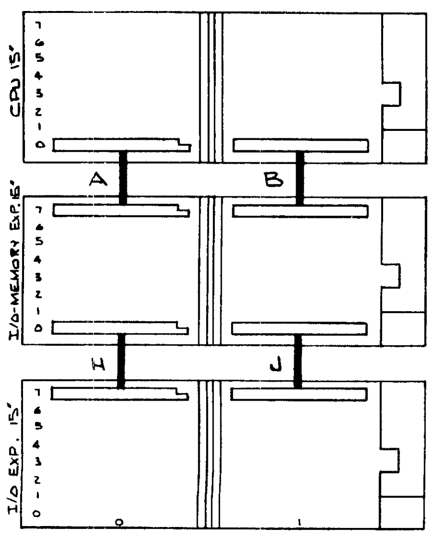
CABLE D : 17-165

USED TO CONNECT TWO ADJACENT 15 IN. CHASSIS. THIS CABLE IS USEFULL WITH EITHER A SELCH OR BUS BUFFER IN THE TOP CHASSIS. THE LOWER CHASSIS BUS APPEARS EXACTLY AS ON THE TOP CHASSIS. NOTE THAT THE DATA CHANNEL DOES NOT APPEAR IN THE LOWER CHASSIS.



CABLE F : 17-166

USED TO CONNECT A 15 IN. CHASSIS FROM ANY CONN ON ONE SIDE (WHERE THE BUS HAS BEEN CUT) TO A 10 IN. CHASSIS ONE OR TWO CHASSIS POSITIONS BELOW. (TWISTED PAIR)

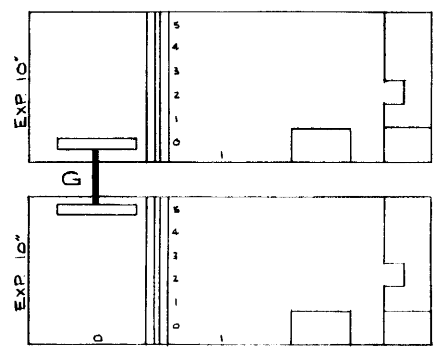


CABLE A : 17-162 & B : 17-163

CABLES A & B ARE USED TO CONNECT TWO ADJACENT 15 IN. CHASSIS. THESE ARE USEFULL TO EXTEND BOTH THE MUX BUS PRIVATE MUX BUS (OR BUFFERED BUS) & MEMORY BUS TO THE LOWER CHASSIS WHICH MUST BE A 15 IN I/O CHASSIS.

CABLE H : 17-193 & J : 17-194

SAME AS CABLE A & B LESS MEMORY BUS WIRING



CABLE G : 17-168

USED TO CONNECT TWO 10 IN. CHASSIS LOCATED ONE OR TWO POSITIONS BELOW. (TWISTED PAIR)

NOTES

NAME	DATE

TITLE: CABLE INFORMATION N S

TASK NO. 0316 — DWG. NO. 01-051R01C12 — SHEET 2 OF 2

INTERDATA

CUT ALONG LINE

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