Publication Number 29-573R06

M81-SERIES
MODEL 8/16
MAINTENANCE MANUAL

Consists of:

M71-Series Model 6/16 Processor General Description	29-470A12
M71-Series Model 6/16 Processor Installation Specification	01-094R02A20
M71-Series Model 6/16 Processor Maintenance Specification	01-094A21
M71-094 Multiply/Divide Card Information Specification	02-403A12
Selector Channel Installation Specification	02-232M01R04A20
Selector Channel Maintenance Specification	02-232M01R01A21
Test Aid Information Specification	02-276R03A12
Hexadecimal Display Information Specification	09-065R01A12
Model 8/16 Micro-Program Listing	05-068A13
Model 8/16 DROM BASIC	05-069F01A13
Model 8/16 DROM BASIC + MPY-DIV	05-069F02A13
Model 8/16 DROM BASIC, M/D + SPFP	05-069F03A13
Model 8/16 DROM BASIC, M/D + DPFP	05-069F04A13
Parity Option Board Schematic Drawing	02-368R01C08
Hexadecimal Display Panel Schematic Drawing	09-065R02D08
Functional Schematic Drawing	02-232M01R05D08
Functional Schematic Drawing	35-448C03
Functional Schematic Drawing	01-094R08D08
Functional Schematic Drawing	02-403R01D08
Functional Schematic Drawing	02-405R02D08
Assembly Drawing	35-391M02R04E03
Assembly Drawing	35-605R01D03
Assembly Drawing	35-604R08E03
Assembly Drawing	35-601R01D03
Assembly Drawing	35-602R01D03
Assembly Drawing	35-603R02D03
Assembly Drawing	02-351R01B08

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M71-SERIES
MODEL 6/16
GENERAL DESCRIPTION

INTRODUCTION

The Model 6/16 combines advanced circuits and packaging designs to give the user a price/performance optimized machine. The Model 6/16 is completely upward compatible with INTERDATA Models 3, 4, 74, 7/16 Basic Processor user instruction, interrupt handling, input-output formats and control sequencing. In addition, many of the powerful features of the INTERDATA Models 5, 70 and 80 are included. Because of this compatibility, the Model 6/16 can use the wide range of existing software and peripheral devices.

The Model 6/16 offers a comprehensive set of 96 instructions making the system both easy to program and efficient to operate. Through multi-function instructions and direct core addressing, coding and debugging time is reduced to a minimum.

Memory is addressable to the eight-bit byte level. Memory is expandable from the basic 8,192 bytes to 65,536 bytes. All memory is directly addressable with the primary instructions, no paging or indirect addressing is required. Sixteen 16-Bit General Registers can be used as Accumulators, fifteen of which can also be used as Index Registers. Register-to-Register instructions permit operations between any of the sixteen General Registers, eliminating redundant loads and stores.

The Model 6/16 also provides a flexible Input/Output system in addition to conventional means of programmed I/O. In the Automatic I/O Service Mode, the Processor acknowledges all I/O interrupts and automatically performs much of the overhead prior to activating the Interrupt Service Routine.

Up to four Direct Memory Access Devices can be added to a Model 6/16 Memory System. This channel operates over the common Memory Bus, on a cycle stealing basis, through a Direct Memory Access Port which is built into the Processor. Two types of Direct Memory Access Channels can be used with the Model 6/16 System: The Selector Channel, which permits direct data transfer between any standard oriented INTERDATA device controller and memory; and the Direct Memory Access Channel custom designed by the user for special applications. In addition, an Instruction Steal DMA is supported which allows high speed burst transfer over the I/O Bus.

SCOPE

This document is intended to enable the digital technician to understand the INTERDATA documentation system. Number Notation, the Part Numbering System, and the Drawing System are described. Illustrations are provided to help understand these systems. Other publications which may be of interest to Model 6/16 users are shown in Table 1.

A cross reference between INTERDATA part numbers and standard industry part numbers for the ICs and transitors found in the Model 6/16 may be found in Appendix 1.

TABLE 1. RELATED PUBLICATIONS

TITLE	PUBLICATION NUMBER
16-Bit Reference Manual	29-398
Model 6/16 Maintenance Manual	29-470
Multiplexor Bus Buffer Instruction Manual	29-267

BLOCK DIAGRAM

A block diagram of the Model 6/16 is shown in Figure 1. The Model 6/16 is a 16-Bit digital computer.

Part No.	Description	Card File Position
35-604	CPU	7
	MEMORY	6

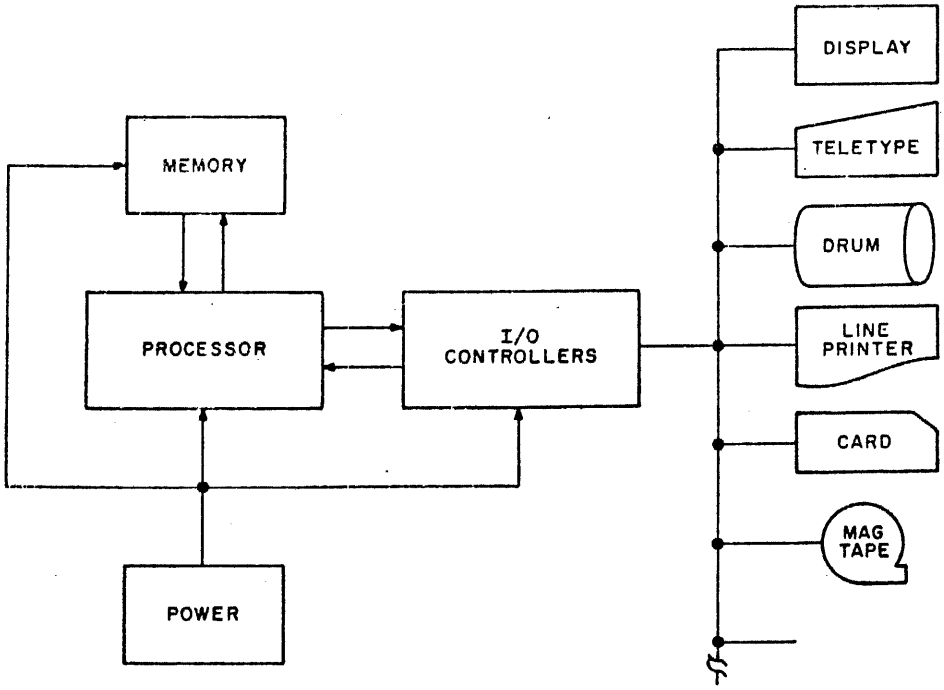


Figure 1. Model 6/16 Simplified Block Diagram

DOCUMENTATION

This section describes the style and conventions used with INTERDATA documentation.

Number Notation

The most common form of number notation used in INTERDATA documentation is hexadecimal notation. In this system, groups of four binary digits are represented by a single hexadecimal digit. Table 2 lists the hexadecimal characters employed.

TABLE 2. HEXADECIMAL NOTATION DATA

Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal
0000	0	0	0110	6	6	1100	12	C
0001	1	1	0111	7	7	1101	13	D
0010	2	2	1000	8	8	1110	14	E
0011	3	3	1001	9	9	1111	15	F
0100	4	4	1010	A	A			
0101	5	5	1011	B	B			

To differentiate between decimal and hexadecimal numbers, hexadecimal numbers are preceded by the letter "X", and the number is enclosed in single quotation marks. Examples of hexadecimal numbers are X'1234', X'2EC6', X'A340', X'EEFA', and X'10B9'.

Part Numbering System

INTERDATA parts, drawings, and publications use a common numbering system. The part number and drawing numbers for drawings which describe the part are related. The publication number is often related to the part number of the device or program described. Figure 2 shows the format used for INTERDATA part numbers. The fields are described in the following paragraphs.

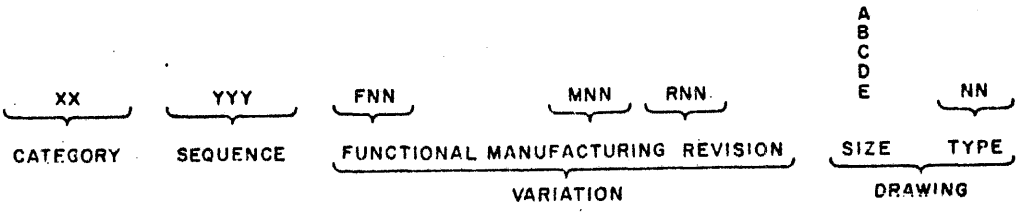


Figure 2. Part Number Format

Category Field

The two-digit Category Number indicates the board class or category to which a part belongs. Typical examples of category number assignments are:

01 – Basic Hardware Systems
02 – Basic Hardware Expansions
03 – Basic Software Systems
04 – Software Packages
05 – Micro-programs
06 – Test Programs
07 – Subroutines of General Utility
10 – Spare Parts Packages
12 – Card File Assemblies
13 – Panels
17 – Wire and Cables
19 – Integrated Circuits
20 – Transistors
27 – Peripheral Equipment
29 – Manuals
34 – Power Supplies
35 – Assembled Printed Circuit Boards
36 – Electro-Mechanical Devices

Sequence Field

The Sequence number identifies a particular item within the category. Sequence numbers are assigned serially, and have no other significance.

NOTE

The Sequence Field, like all other part number fields, may be lengthened as required. The field lengths shown on Figure 2 are minimum lengths (insignificant zeros must be added to maintain these minimums).

Functional Variation Field

The optional Functional Variation Field consists of the letter "F" followed by two digits. The F field is used to distinguish between parts which are not necessarily electrically or mechanically equivalent, but which are described by the same set of drawings. For example, a power supply may be strapped internally to operate on either 110 VAC or 220 VAC. Except for this strap, all power supplies of this type are identical. The strapping option is easily described by a note on the assembly and test specification drawings. Therefore, this is a functional variation.

Manufacturing Variation Field

The optional Manufacturing Variation Field consists of the letter "M" followed by two digits.

The M Field is used to distinguish between parts which are electrically and mechanically equivalent (interchangeable), but which vary in method of manufacture. For example, if leads are welded instead of soldered on an assembly, the M Field changes.

An important exception to the meaning of the M Field exists for categories related to software. In software, the M Field number, when used, indicates the form in which a particular program is presented. For example, define a program as a set of machine instructions. These same identical instructions may be presented on punched cards, paper tape, or magnetic tape; and for any of these they can be in symbolic form or in relative or absolute binary form. Thus, there are many ways to present the same identical program.

The format for the M Field and its meaning for software is:

Mxy

where x identifies the media selection (i.e., Paper Tape, Magnetic Tape, Cassette, etc.) and y identifies object or source and the format.

Meaning of x		Meaning of y	
Conceptual	0	1	Object program standard format 32-Bit Processor
Paper Tape	1		
Cassette	2	4	Memory image
Magnetic Tape (800 BPI)	3	6	Object Program standard format 16-Bit Processor
Cards	4	7	Object non-standard format
Disc (2.5 MB)	5	8	Object established task
Disc (10 MB)	6	9	Source program
Magnetic Tape (1600 BPI)	7		

These numbers refer to the physical program placed on an approved media for INTERDATA Software. A Paper Tape Object program is standard format and for a 16-Bit Processor has an M16 identifier. A Magnetic Tape Object program is standard format and for a 32-Bit Processor has an M31 identifier.

In addition to the foregoing, there are three unique M numbers which have special meaning:

00	Conceptual Object
91	32 Bit Object Listing
92	Programming Specifications
95	Program Description
96	16 Bit Object Listing
98	Operating Procedures
99	Documentation and Manuals

Revision Field

The optional Revision Field consists of the letter "R" followed by two digits. The R Field is used to indicate minor electrical or mechanical changes to a part which do not change the part's original character. The R field changes often reflect improvements. A part with a revisions level *HIGHER* than the one specified can be used; however, a part with a revision level *LOWER* than specified should not be used.

NOTE

A part number must contain a Category number and a Sequence number. All other fields are optional.

Drawing Field

The optional Drawing Field consists of a letter from "A" to "E" followed by two digits. The letter indicates the size of the original drawing. The sizes for each letter are:

A – 8½" x 11"
B – 11" x 17"
C – 17" x 22"
D – 22" x 34"
E – 34" x 44"

The two digits indicate the drawing type as follows:

01 – Parts List
02 – Machine Details
03 – Assembly Details
05 – Art Details
06 – Wire Run List
08 – Schematic
09 – Test Specification
10 – Purchase Specification
11 – Bill of Material
12 – Information
13 – Program Listing
14 – Abstracts
15 – Program Description
16 – Operating Instructions
17 – Program Design Specifications
18 – Flow Charts
19 – Product Specification
20 – Installation Specification
21 – Maintenance Specification
22 – Programming Specification
23 – Replaceable Parts List
24 – Application Information
25 – Functional Specifications

Examples

The following list provides some examples of the part numbering system. The numbers were arbitrarily selected, and in most cases are fictitious.

35-060	The 60th printed circuit board assigned a part number under this system.
35-060M01	A printed circuit board electrically and mechanically interchangeable with the 35-060, but differing in method of manufacture.
35-060F01	A printed circuit board not electrically and mechanically interchangeable with the 35-060, but described by the same set of drawings.
35-060-R01	A revised 35-060 printed circuit board which probably supercedes the 35-060.
35-060A01	The 8½ by 11 inch parts list for a 35-060.
35-060B08	The 11 by 17 inch schematic for a 35-060.
06-072	An 8½ by 11 inch listing of the 06-072 program.
06-072A12	An 8½ by 11 inch information drawing on the 06-072 program. Probably a part of the program.
29-060	The 60th manual assigned a number under this system. Note that this number is not referenced in any way to the part number of equipment described in the manual.

Drawing System

This section describes the drawings provided with INTERDATA equipment. Drawings provided with peripheral devices and other purchased items may vary from the system described in this section.

A digital system may be divided into a collection of functionally independent circuits such as Memory, Processor, and I/O Device Controllers. These circuits may or may not be saleable units in their own right, but in the electrical sense they are essentially self contained and capable of performing their function with minimum dependence on other functional circuits in the system. Hence a functional circuit is treated as a building block. Each schematic contains a variety of information including type and location of discreet Integrated Circuits (IC's), pin connections, all interconnections within the schematic, connector pin numbers and connections to other schematics. Further, the schematics are drawn to reflect, in an orderly fashion, all logical operations performed by the circuits. Generally, symbols used on schematics conform to MIL-STD-806B.

Registers are named according to the following rules:

1. The register mnemonic name has a maximum of three letters, excluding "I, O, Q, and Z".
2. Each bit in the register is numbered, usually starting at 00 on the left, or most significant positions, and continuing to N-1 on the right, where N is the number of bits in the register.
3. The 00 bit is the Most Significant Bit and the N-1 is the Least Significant Bit.

The IC's mounted directly on the logic board are represented on the schematic drawings by logic symbols. Each symbol contains the reference designation, device part number (category and sequence), and symbol mnemonic designation. Refer to Figure 3.

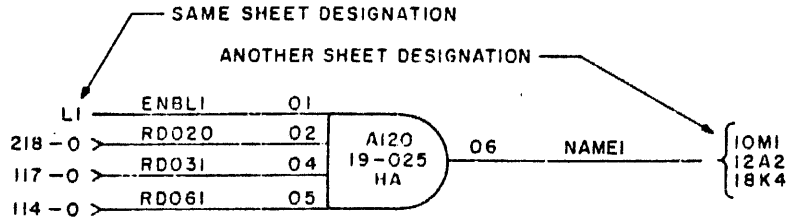


Figure 3. Example of a High Speed AND Gate

The designations, numbers, and references shown in Figure 3 are:

A20 – This shows the components location on the logic board. Figure 4 illustrates the method generally used to determine component location on a logic board. With the logic board oriented so that the header connnectors (Conn 0 and Conn 1) are on the right, the components are numbered from left to right starting in the upper left corner. That is, the first IC in the upper left corner is 01 and the first capacitor is C1.

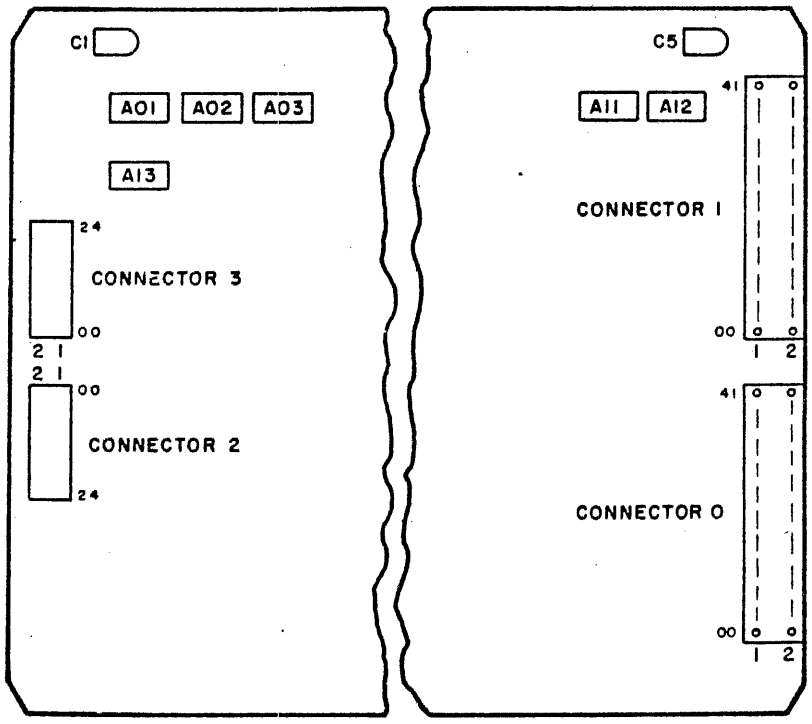


Figure 4. Example of a Logic Board Layout

19-025 – The number 19 is the category number of ICs, and the 025 is the sequence number of the component.

HA – Designates that this component is a high speed AND gate. Some other common designators used are:

P	–	Power Gate
SB	–	Schottky High Speed Power Gate
SG	–	Schottky Gate
SGO	–	Schottky High Speed Gate, Open Collector
SO	–	Schottky High Speed Gate, Open Collector
B	–	Buffer
SB	–	Schottky High Speed Buffer
LOR	--	Low Power Schottky OR
LN	–	Low Power Schottky NOR

L1 – This input lead is from area L1 on the same schematic sheet.
10M1, 1242, 18K4 – Designate outputs to another logic schematic sheet.
218-0,117-0, 114-0 – Designate inputs from Connector 0.
Pin numbers (01, 02, 04, 05 and 06) correspond directly to the actual IC pin numbers.

Figure 4 also shows the locations of the header connectors (Conn 0 and Conn 1) and the cable connectors (Conn 2 and Conn 3). All logic boards always contain Header Connectors 0 and 1, however, any combination (either, both, or none) of cable connectors (Conn 2 and Conn 3) may be provided.

Whenever possible, the immediate output from a flip-flop (1 or 0 side) has a mnemonic name preceded by an F. A flip-flop whose name is PSEL (Processor selected) has an output mnemonic, on the 0 side, FPSEL0 (see Figure 5). This provides the digital technician with an indication, when observing a mnemonic at the terminal end of a net, that the signal is the output of a flip-flop rather than a decoded function.

Clocked devices, flip-flops, and counters in particular, are drawn in a manner which indicates information concerning their inputs. An input which has a circle adjacent to the pin designation implies a low active signal is required to perform the specified operation. In addition, an inverted V at the clock input shows that the device changes state on an edge. Thus, if no circle is present the chip is positive edge triggered. Refer to Figure 5 for examples.

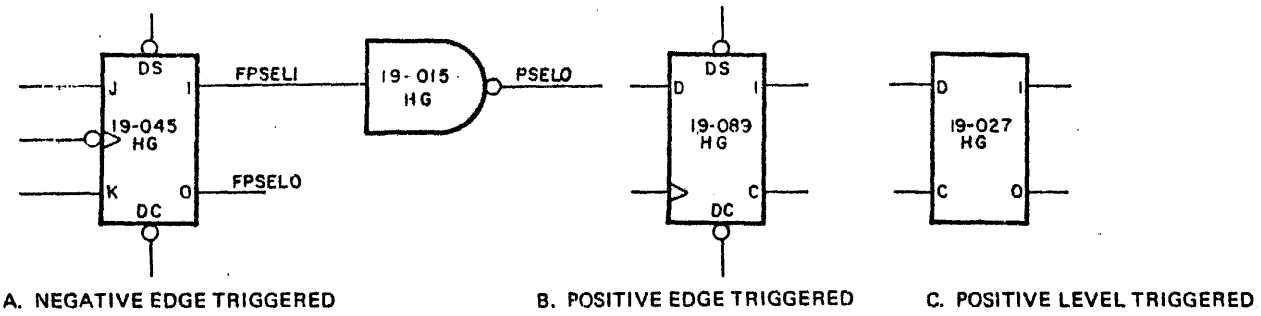


Figure 5. Examples of Clocked Devices

Figure 6 shows the pin numbering scheme for the header and cable connectors. Header connectors always have 2 rows of pins and 42 positions. Cable connectors always have 2 rows of pins but may vary in the number of positions. The number of positions may only vary in increments of five positions (10 contacts). For instance, if 24 positions are desired, five blocks of five positions each (25 positions) must be used.

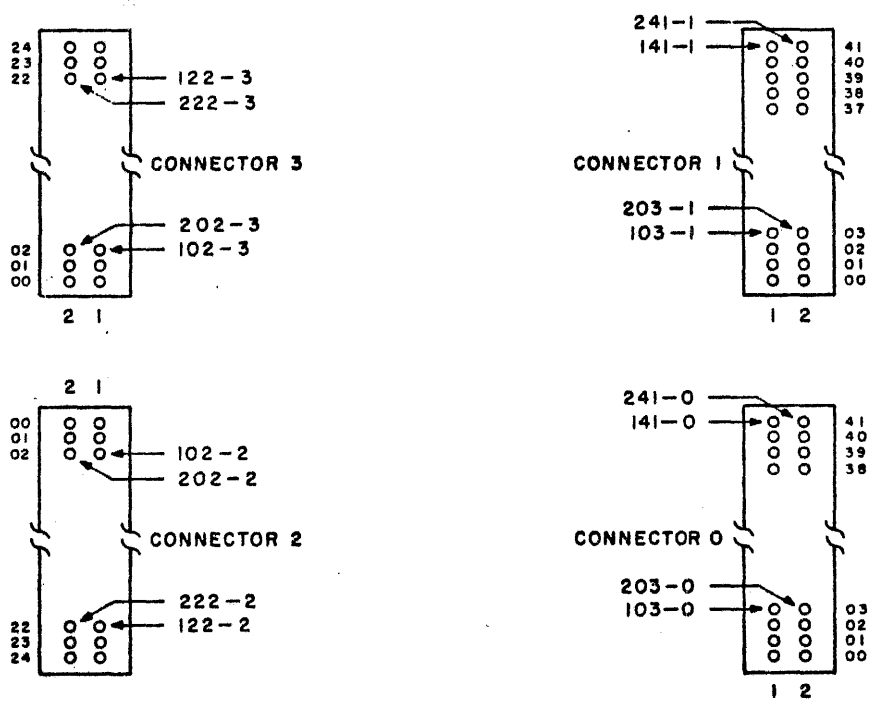


Figure 6. Connector Pin Numbering

A net is defined as an electrical connection between two or more points in a circuit. Ordinarily, a net has an originating end (usually a collector where the signal is generated) and one or more terminating ends. Often it is convenient to assign descriptive mnemonic names to nets as a way of identifying them on schematics. Whether a net is named or not is sometimes arbitrary. However, a net is always assigned a name if:

1. The net is contained on one drawing sheet but is not shown as a complete solid line on that sheet.
2. Part of the net appears on more than one sheet.
3. Part of the net connects with a different schematic.
4. Part of the net leaves a logic board.

If a net is named, the following rules are observed.

1. All mnemonic names are a maximum of six characters.

2. All decimal digits and upper case letters except the letters "I, O, Q, and Z" are permitted.

3. No other characters are permitted.

4. Where possible, mnemonics are descriptive. However, it should be recognized that descriptive names are not always possible and a danger of misinterpreting a mnemonic exists.

5. Mnemonic names are not repeated within a schematic.

6. Every mnemonic is suffixed by a state indicator. This indicator consists of the digit "1" for the logically true state, or the digit "0" for the logically false state. For example, the set side of a flip-flop has the "1" state indicator, while the reset side has the "0" state indicator. The state indicator for a function changes each time that function is inverted. Thus, the state indicator permits assigning the same mnemonic to functions that are identical except for an inversion. Logic 0 = .4VDC or less, Logic 1 - 2.4VDC or more.

7. When a logical function is inverted, an inversion indicator is added after the state indicator. This allows for functionally equivalent, but electrically different nets to have the same mnemonic name. For example, assume a signal NAME1 which may be inverted to produce NAME0. If NAME0 is then inverted, NAME1A is produced. NAME1 and NAME1A are functionally equivalent, but physically different nets.

There are times when a net fans-out to many sheets of a schematic. It is also possible for a net to fan-out to sheets on different schematics. In such situations, the net is assigned a mnemonic name. The net is also "zoned" from sheet to sheet to allow for properly identifying the originating and terminating ends of the net. The originating end of a net is defined as the collector at which a signal is generated. All other points to which the net connects are called terminating ends. When a lead leaves a sheet at the originating end, it is zoned to each and every sheet on which the net reappears, by indicating first the page number, followed by the schematic number that contains the page. For example, assume that the gate shown on Figure 3 is on a schematic, Sheet 20. The output NAME0, appears on Sheets 10, 12 and 18 of the schematic. Note that the schematic number is implied. When a net enters a sheet from another sheet, it is labeled with the same mnemonic name, and is zoned back to the originating end of the net only. Thus, on Figure 3, the ENABL1 may have many other terminations in addition to the one shown. Generally, when a net leaves the sheet where it originates, it is zoned to every other sheet where the net terminates, while the terminating end is zoned only to the originating sheet. Note that on schematics, signals are coordinated between sheets only when the sheets are related to the same board. When a signal leaves a board, the Back Panel Map must be used.

When a lead leaves a logic board, it usually does so through a logic board back panel connector pin. These connector pins must be shown on the schematic even if the complete net is shown on one drawing sheet. Only the connector pin number need be indicated under the pin symbol, since the connector number itself is implied by the logic board location number in the logic symbol or in the footnote. Thus, on Figure 3, RD061 enters the logic board on Pin 114 of Header Connector 0.

Figure 7 is a typical schematic sheet with call-outs illustrating many of the conventions described in this section.

The schematic drawings for the basic Digital System and some of the more common expansions are commonly included in the rear of the appropriate Digital System Maintenance Manual. Schematic drawings for other expansions are included with the expansion or with the publications that describe the expansion.

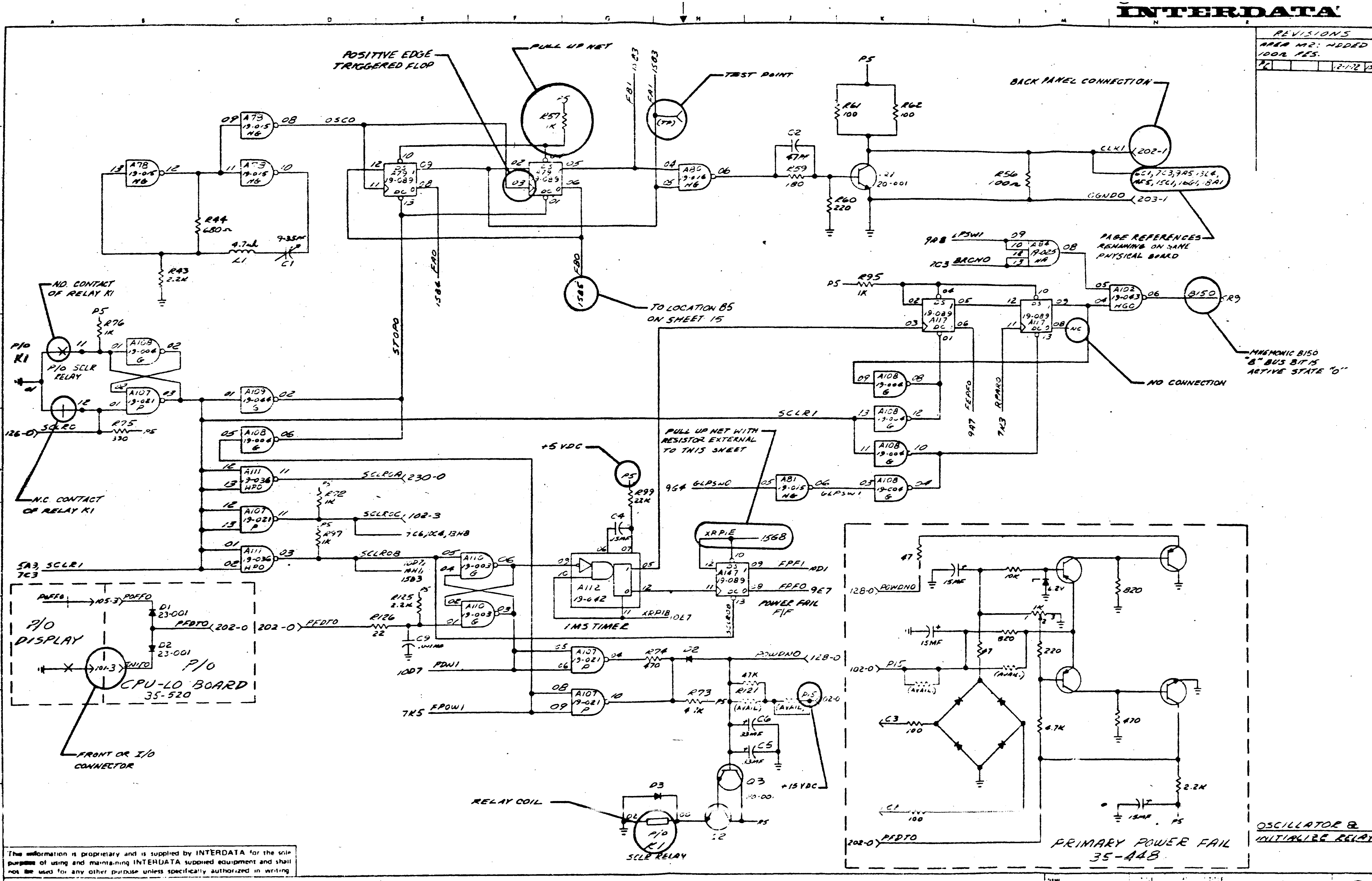


Figure 7. Functional Schematic Format Drawing

M71-SERIES
MODEL 6/16
INSTALLATION SPECIFICATION

INTRODUCTION

The INTERDATA Model 6/16 Digital System features a highly modular structure which permits configurations to suit the user's exact needs. The Model 6/16 provides the means for convenient expansion as the user's requirements grow. This document describes the Processor and System Expansion Chassis, Power Supply Mounting, Filler and Display Panel Mounting, and the interconnecting cables. Printed circuit boards are discussed with respect to cabling and location only. Circuit descriptions of these boards are provided in the appropriate maintenance or instruction manuals. The following descriptions assume that the equipment is mounted in standard INTERDATA cabinets.

MECHANICAL COMPONENTS

This section is intended to familiarize the reader with the mechanical components that are discussed in this document (i.e., Cabinet, Chassis Support Rails, and Filler Panels). Figures 1 through 4 provide the dimensions and mounting configurations for the Cabinet, Chassis Support Rails, and Filler/Display Panels. It is shown in Figure 4, that while 5¼ inch, 7 inch, 8¾ inch and 10½ inch Filler Panels and the Display Panel mount in the same way (via retaining brackets), the smaller 1¾ inch Filler Panel mounts with spring clips.

PROCESSOR AND EXPANSION CHASSIS MOUNTING

Two Processor Chassis (7 inch and Twin Versions) are available. In addition, a 7 inch Expansion Chassis is available for expanding the Model 6/16 Digital System. Two different Expansion chassis are available, one for mounting either 7 inch or 15 inch controllers and one for mounting 10 inch controllers. The Expansion Chassis has the same over-all dimensions as the 7 inch Processor Chassis (refer to Figure 12).

The Expansion or Processor Chassis slides into the rack on two Chassis support rails (refer to Figures 2 and 3) from the front of the rack.

CAUTION

NO CHASSIS SHOULD BE MOUNTED IN CANTILEVER FASHION. CHASSIS SUPPORT RAILS MUST BE USED. IF A RACK CABINET OTHER THAN AN INTERDATA CABINET IS USED, CONSULT THE RACK MANUFACTURER FOR PROPER SUPPORT RAILS.

The Chassis support rails are fastened to the mounting uprights at the front and rear of the rack. The Expansion or Processor Chassis are fastened in place, with screws, to the mounting uprights in front of the rack. All Expansion Chassis mount below the Processor Chassis. Expansion Chassis cabling is discussed later in this document. Expansion Chassis location with respect to the Filler Panel and Power Supply is shown in Figure 14.

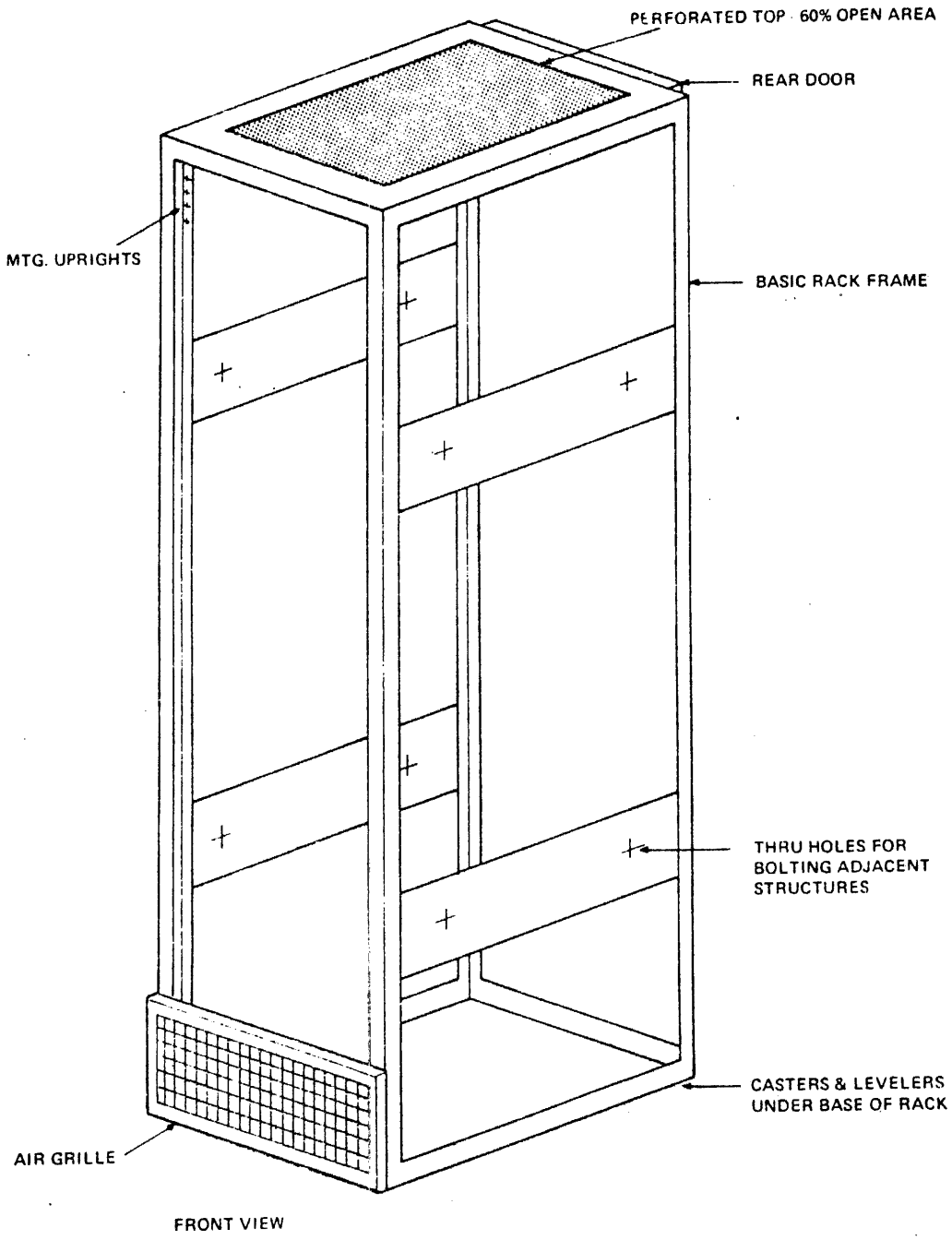


Figure 1. Basic Cabinet

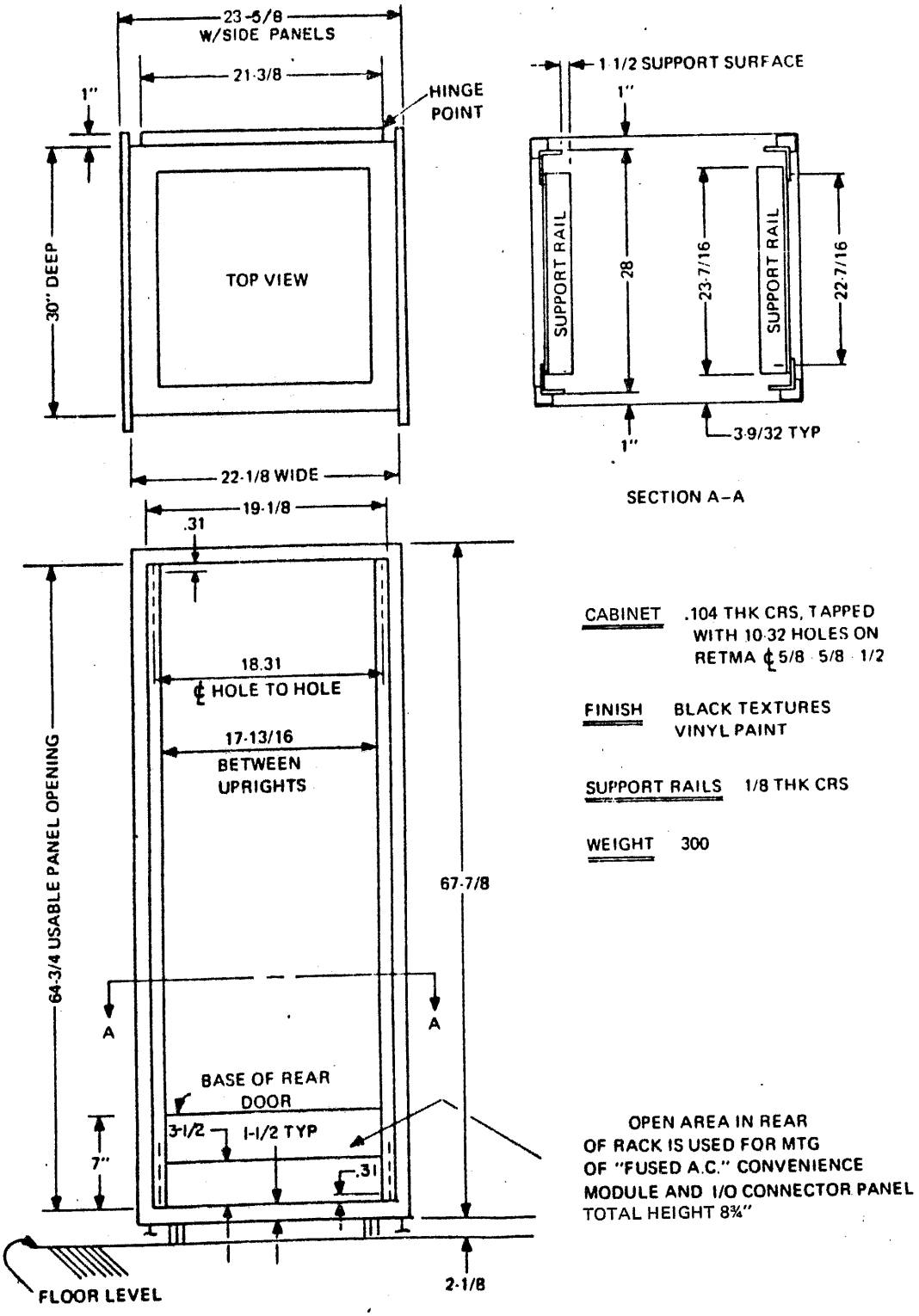


Figure 2. Basic Cabinet Physical Dimensions

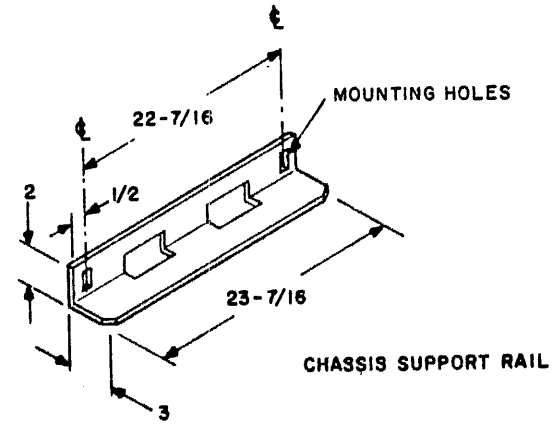


Figure 3. Chassis Support Rail

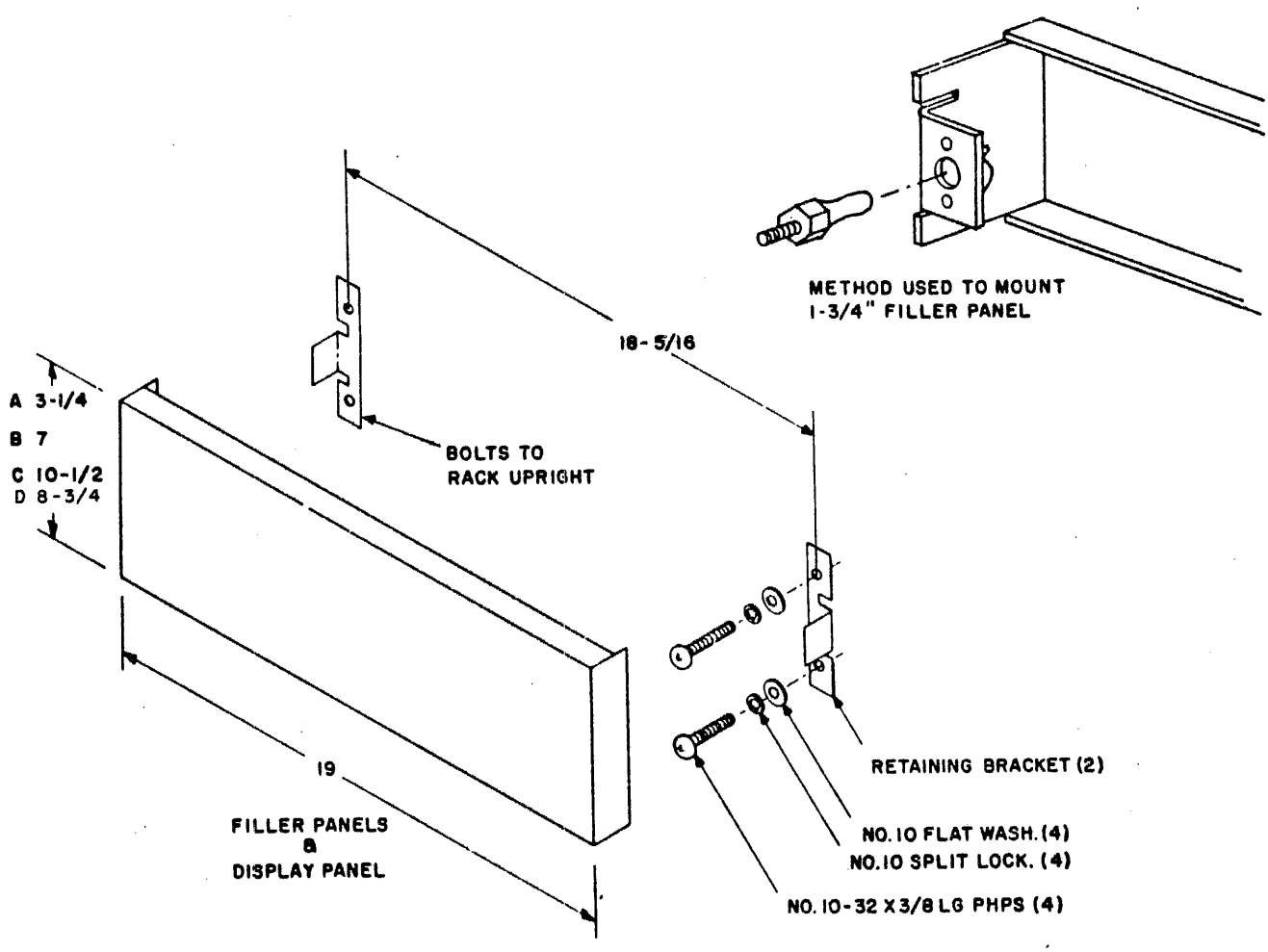


Figure 4. Typical Mounting Configuration for Display and Filler Panels

Expansion Chassis

The Expansion Chassis for 7 inch and 15 inch controllers contains eight universal expansion slots which can accept combinations of single board peripheral controllers, system modules, Selector Channel, or user designed interfaces. Included with this 7 inch Chassis are the cooling fans and interconnecting cables. The chassis may be ordered with or without a power supply.

A 10 inch I/O controller (provided it does not use Connector 1) may be inserted in this chassis via the 02-234 I/O Adapter Kit (see Figure 5).

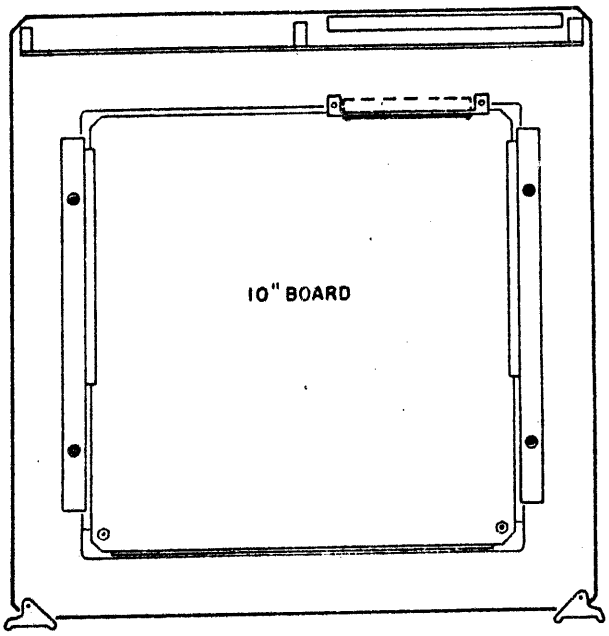


Figure 5. 02-234 I/O Adapter (Top View)

One or two 7 inch boards (half-boards) may be inserted into this Chassis via the 16-398 Half-Board Adapter Kit (see Figure 6). The Half-Board Adapter Kit may hold two active 7 inch boards or one active and one blank 7 inch board, depending on requirements.

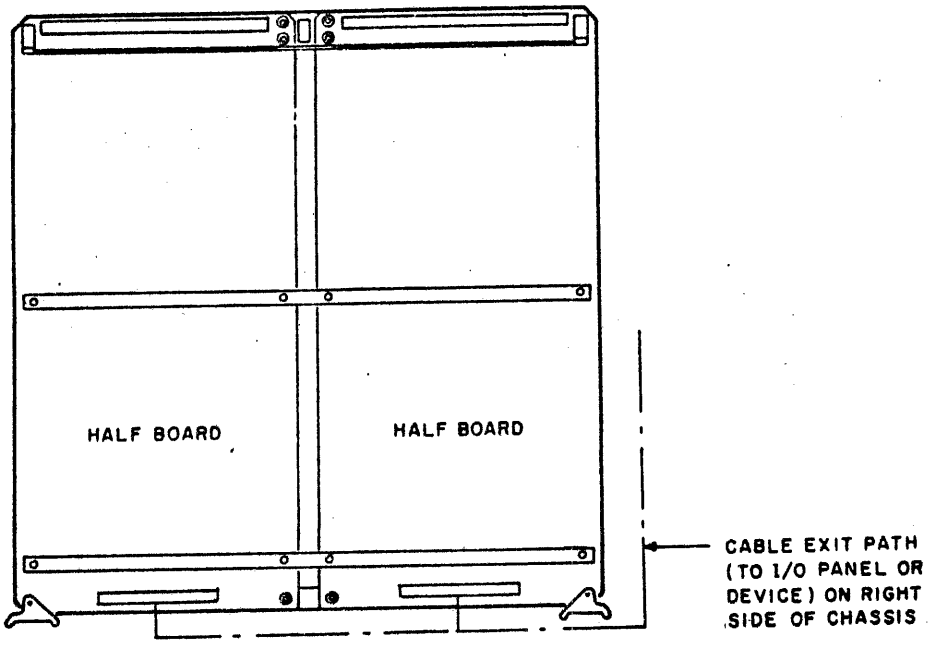


Figure 6. 16-398 Half Board Adapter

No wiring takes place between the boards and the adapters. The adapters are designed such that the connectors on the board plug directly into the Expansion Chassis.

The Expansion Chassis for 10 inch controllers contains six 10 inch I/O expansion slots which can accept any combination of up to six 10 inch wire-wrap or copper peripheral controllers, systems, modules, or user designed interfaces. Included with the Chassis are the cooling fans and system interconnecting cables. The Power Supply is separate.

POWER SUPPLY MOUNTING

The Power Supply mounts in the rear of the cabinet, behind the Processor or Expansion Chassis. It is attached to the right mounting upright (looking from the rear). One of three Power Supplies may be supplied with the Model 6/16 System.

These Power Supplies attach to the mounting upright via four 10-32 x ½ lg PHPS screws (refer to Figure 7).

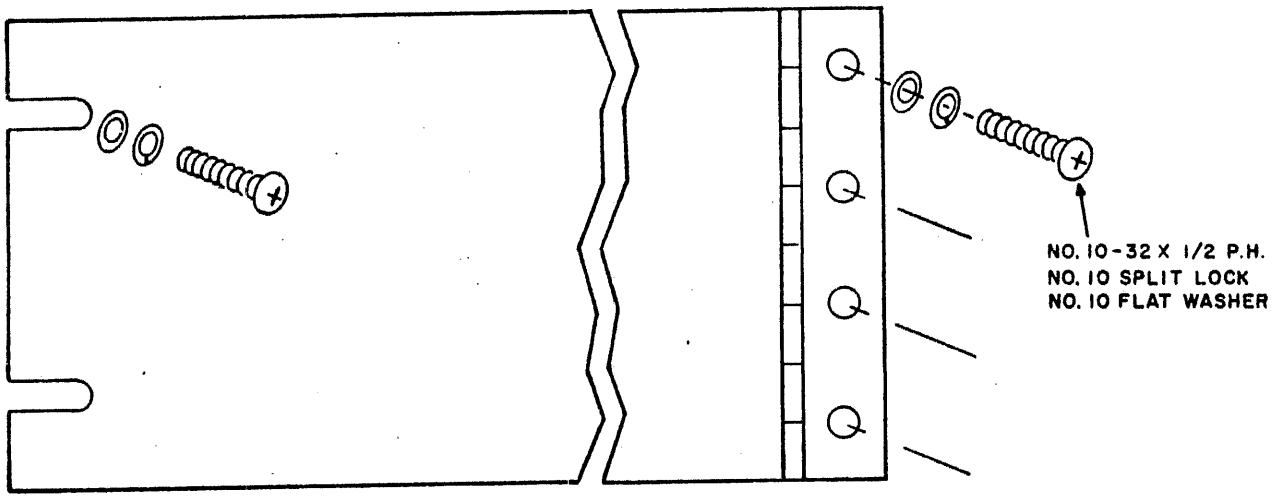


Figure 7. Power Supply Mounting

WARNING

BEFORE HINGING OUT THE POWER SUPPLIES, THE RACK LEVELLING FEET SHOULD BE LOWERED. AFTER THE LEVELLERS ARE IN CONTACT WITH THE FLOOR SURFACE, UP TO THREE POWER SUPPLIES MAY BE HINGED OUT AT ONE TIME. IF THE LEVELLERS ARE NOT DOWN, AND THREE POWER SUPPLIES ARE HINGED OUT, THE RACK MAY TIP DUE TO THE WEIGHT OF THE POWER SUPPLIES.

When any Power Supply is in the installed operating position, it is secured to the left rear upright by two 10-32 screws. The power supply cable connects to terminal lugs at the right rear (looking from the rear) of its respective Processor or Expansion Chassis via Faston lugs and a connector for AC fan power (refer to Figure 8).

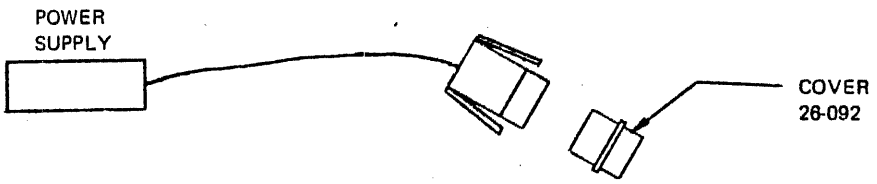


Figure 8. Fan Connector Caps

There is adequate slack provided in the cable to allow the Power Supply to hinge out freely. In order to prevent the cable from being pinched between the Power Supply and Chassis Support Rails, a service loop is required. A maximum of five Power Supplies may be mounted in one rack.

WARNING

ALL AC FAN CONNECTORS ON POWER SUPPLIES WHICH ARE NOT CONNECTED TO MATING RECEPTACLES MUST REMAIN COVERED OR SHORTING MAY OCCUR. SEE FIGURE 8.

The 115/230 volt fan switch on the chassis must be matched with the 115 volt or 230 volt strapping on the Power Supply (refer to Figure 9).

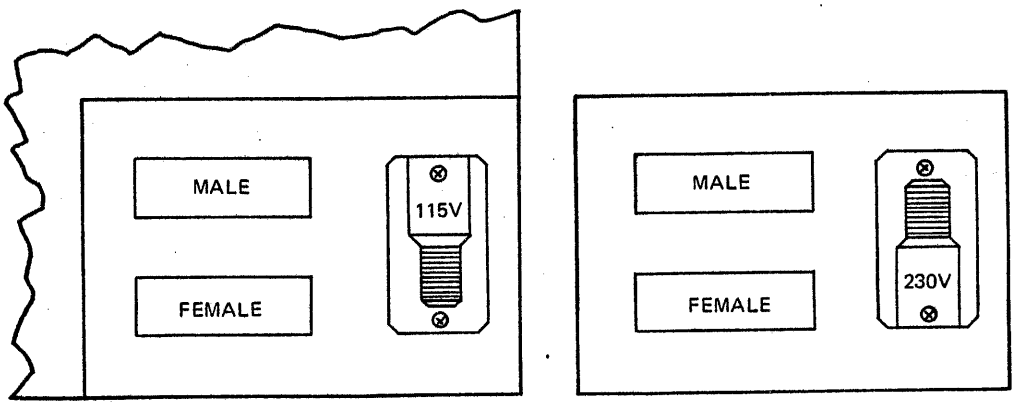


Figure 9. Fan Power Switch Match

Exhaust fan plates are equipped with a switch to provide either 115 volt or 230 volt AC operation as shown in Figure 10.

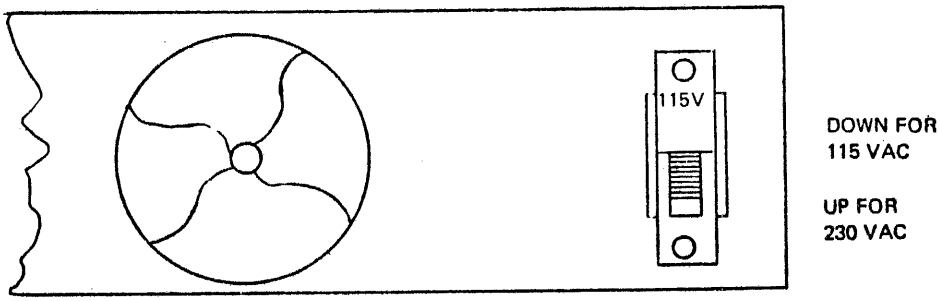


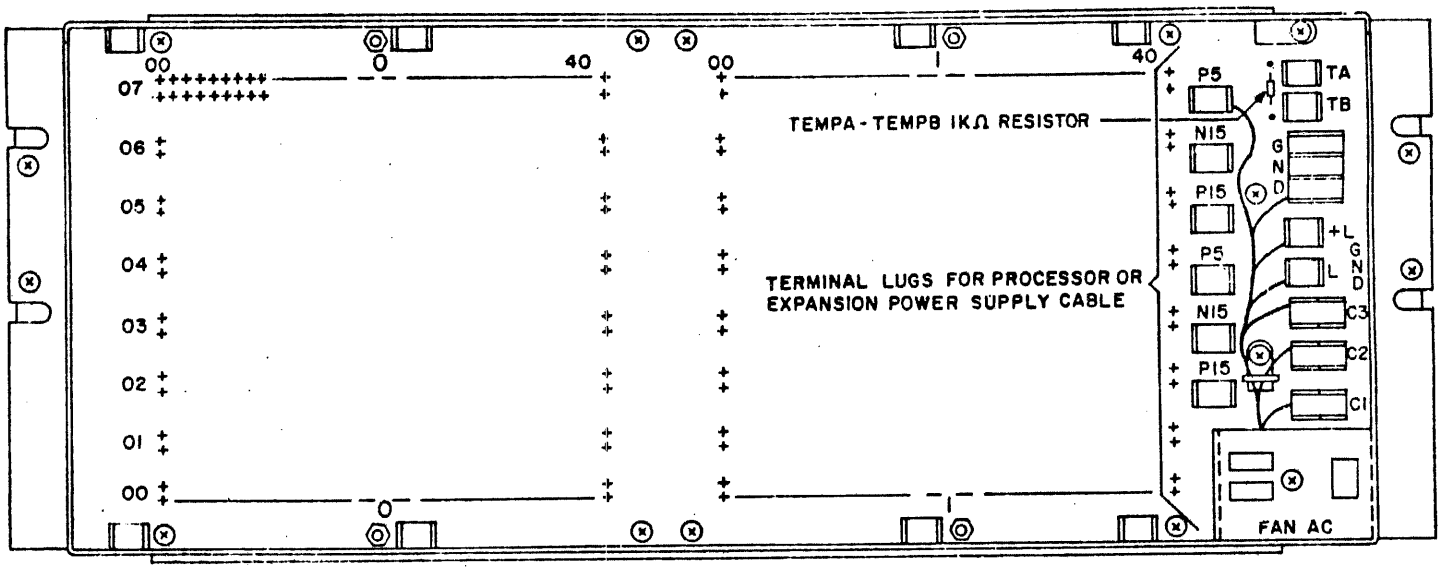
Figure 10. Exhaust Fan Switch Setting

A third supply (34-023) designed to meet VDE specifications required by some International installations, is also available. The mounting procedure for this power supply is different than the procedure for the standard supplies. Refer to *Power Supply Maintenance Manual,* Publication Number 29-452, for installation information.

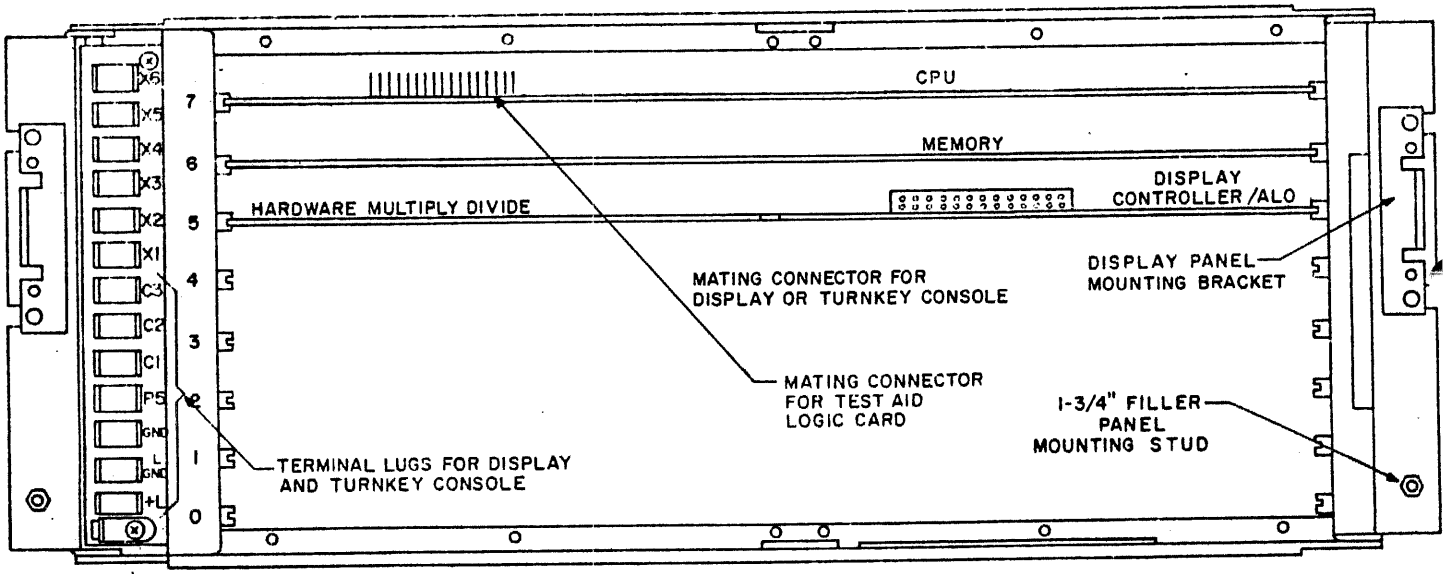
DISPLAY PANEL INSTALLATION

The optional Model 6/16 Hexadecimal or Binary Display Panel is electrically tied to the system via one connector and seven Faston lugs. The connector is installed on Connector A of the 35-601 or 35-602 Display Controller Board and the seven terminal lugs mate into a terminal strip on the left side of the Processor Chassis. The terminal lugs are identified at the Faston Connector and are mated to their corresponding terminal pin (C1, C2, etc.) on the Chassis, see Figure 11.

The Hexadecimal Display Panel is physically mounted to the brackets provided on the Processor Chassis. The 1¾ inch Filler Panel is mounted directly below the Hexadecimal Display Panel on this same Chassis.(see Figure 12.)



Rear View



Front View

Figure 11. View of the Processor and 15 Inch Expansion Chassis

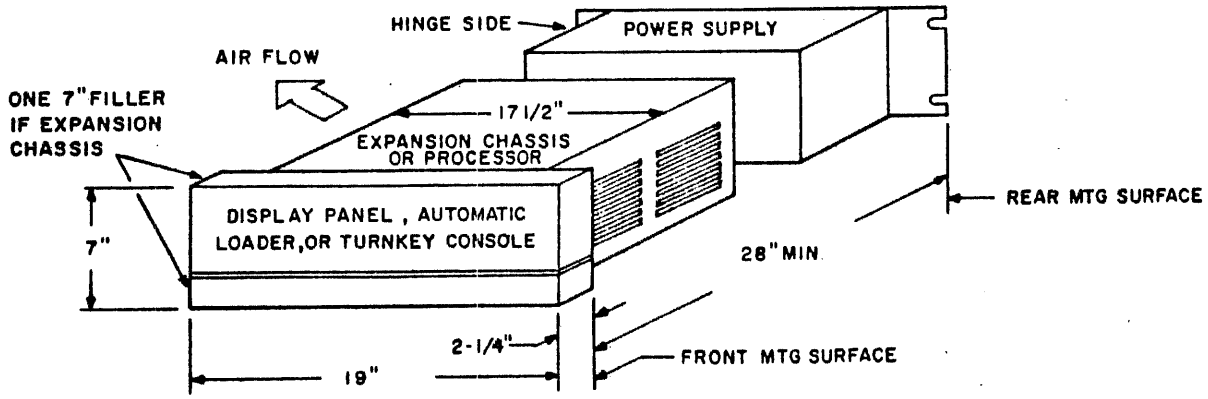


Figure 12. Processor or Expansion Chassis

TURNKEY CONSOLE PANEL INSTALLATION

The Turnkey Console is connected to the Processor in the same manner as the Hexadecimal Display Panel discussed previously (see Figure 13). Only three Faston connectors are provided with the Turnkey Console assembly and in the semi-conductor memory version of the 6/16. They are connected to the terminals on the backpanel indicated on the lugs (i.e. C1R-C1R, C2R-C2R, and CNTL 4-C4).

On the core memory version of the 6/16, the three Faston lugs are connected to a terminal strip on the left side of the Processor Chassis (Figure 11) and are connected as follows: Faston lug C1R to Terminal Pin C1, lug C2R to Terminal Pin C2 and lug CNTL4 to Terminal Pin X1.

Either the Hexadecimal Display Panel option or the Turnkey Console option (but not both) may be installed in a system.

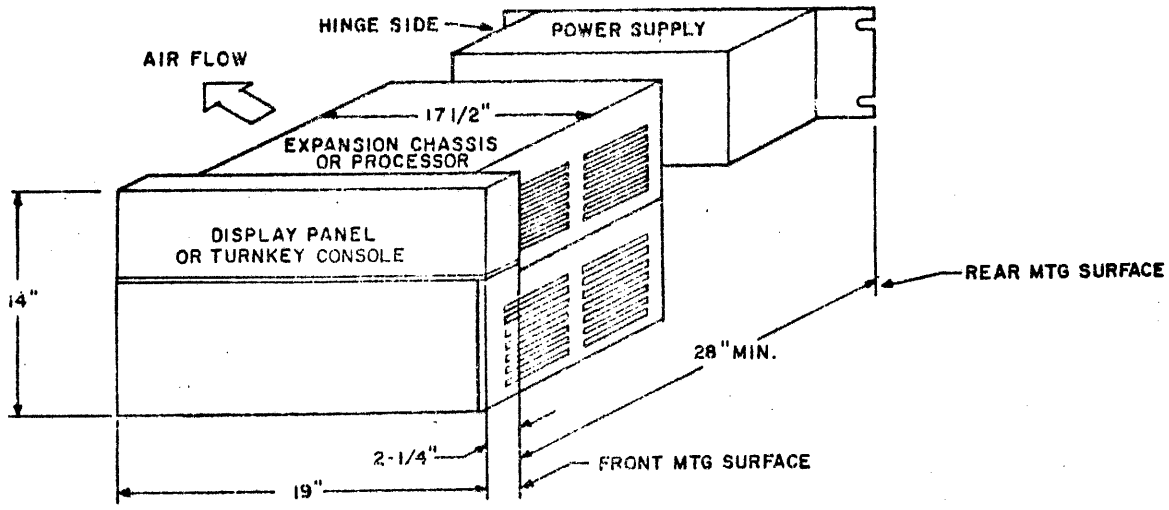


Figure 13. Twin Chassis Processor

MEMORY INSTALLATION

A single slot is allocated to Memory on the Model 6/16. Memory must be installed in Slot 6 of the Processor Backpanel.

NOTE

When installing either an 8KB or 16KB Memory Module on the Model 6/16 the Memory Adapter Card, 35-608, must be installed at the Processor Backpanel on Slot 6. In addition jumpers must be added between 135-0007 and 235-0006, between 128-0106 and TEMPA, and between 227-0106 and TEMPB on this same Backpanel. Remove the 1K OHM Resister between TEMPA and TEMPB. The 16KB Memory Module must be at revision M02R02 or higher.

INSTALLATION OF CPU OPTIONS

Display Controller/Automatic Load Option

Install the Display Controller, 35-601, the Display Controller with Automatic Load Option, 35-602, or Automatic Load Option, 35-603, in Slot 5 Connector "0" of the Processor Backpanel. A Half-Board Adapter 16-398, must be used to mount this board (see discussion on Expansion Chassis).

The Hexadecimal or Binary Display cable or the Turnkey Console cable mounts to the connector on the outer edge of the Display Controller PC board.

Hardware Multiply/Divide Option

Install the Hardware Multiply/Divide PC board, 35-605, in Slot 5 Connector "1" of the Processor Backpanel. A Half-Board Adapter, 16-398, must be used to mount this board (see the discussion on the Expansion Chassis).

NOTE

The Multiply/Divide Option may only be used on Processors equipped to support this option. The Processor PC board must be stamped 35-604F02.

Primary Power Fail/Auto-Restart Option

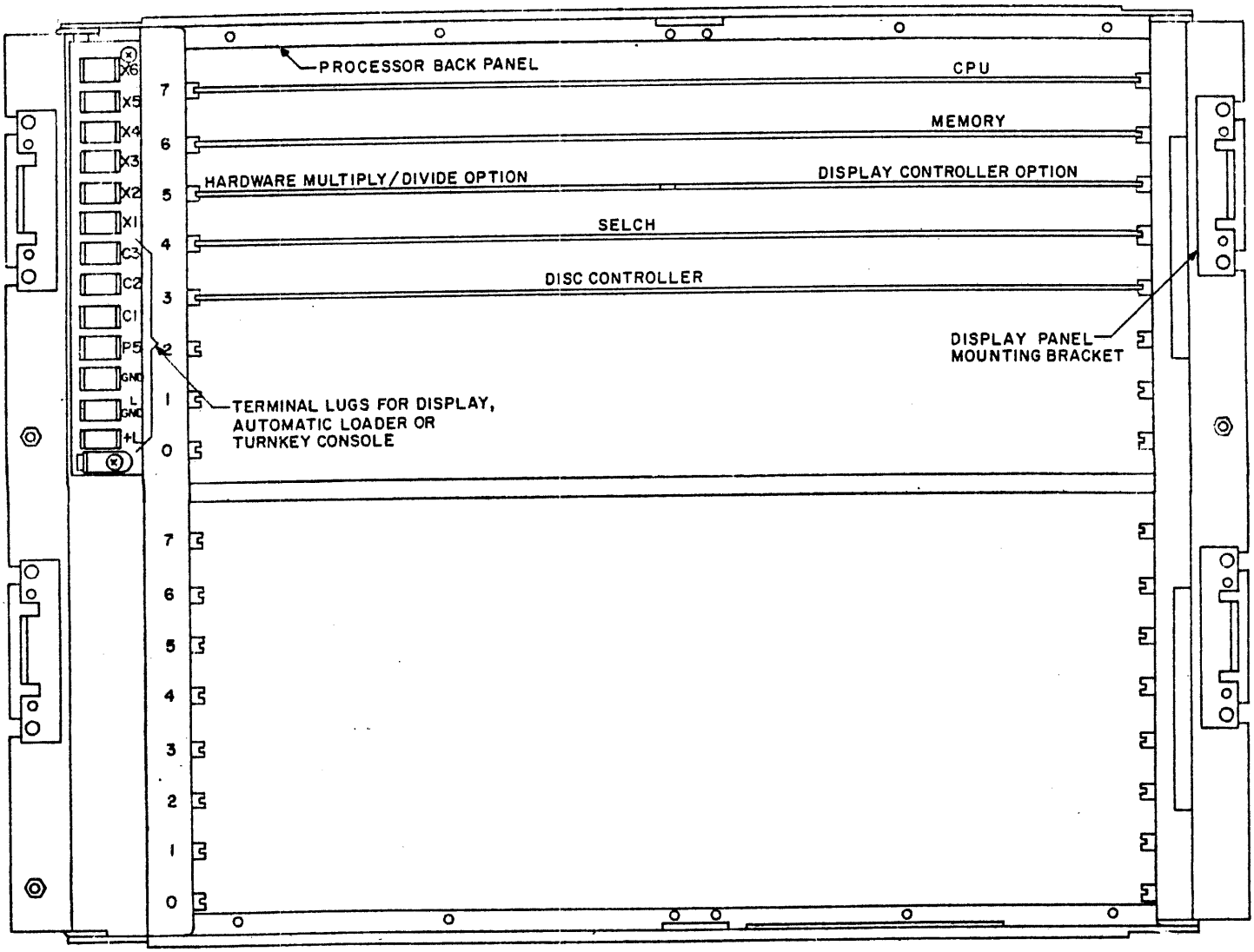
Install the 35-448 logic card for the Primary Power Fail/Auto-Restart option on the wire wrap side of the Processor Backpanel at Slot 7, Connector 0 with the apparatus side up. The 17-182F01 and 17-182F02 cables which supply 12 VAC to the logic card, connect between C1 on the logic card and C1 on the backpanel and C3 on the logic card and C3 on the backpanel as indicated on the cables (see Figures 14 and 15). Remove wire-wrap jumper (P to R) on Processor board for auto-restart (see Processor Functional Schematic Sheet 14). The Primary Power Fail option card is adjusted at the factory.

Memory Parity Option Card

The 35-533 Memory Parity Option card is used with parity memory modules only. The Memory Parity option card mounts on the wire wrap side of the Processor Backpanel, Slot 7, Connector 1 (see Figure 15).

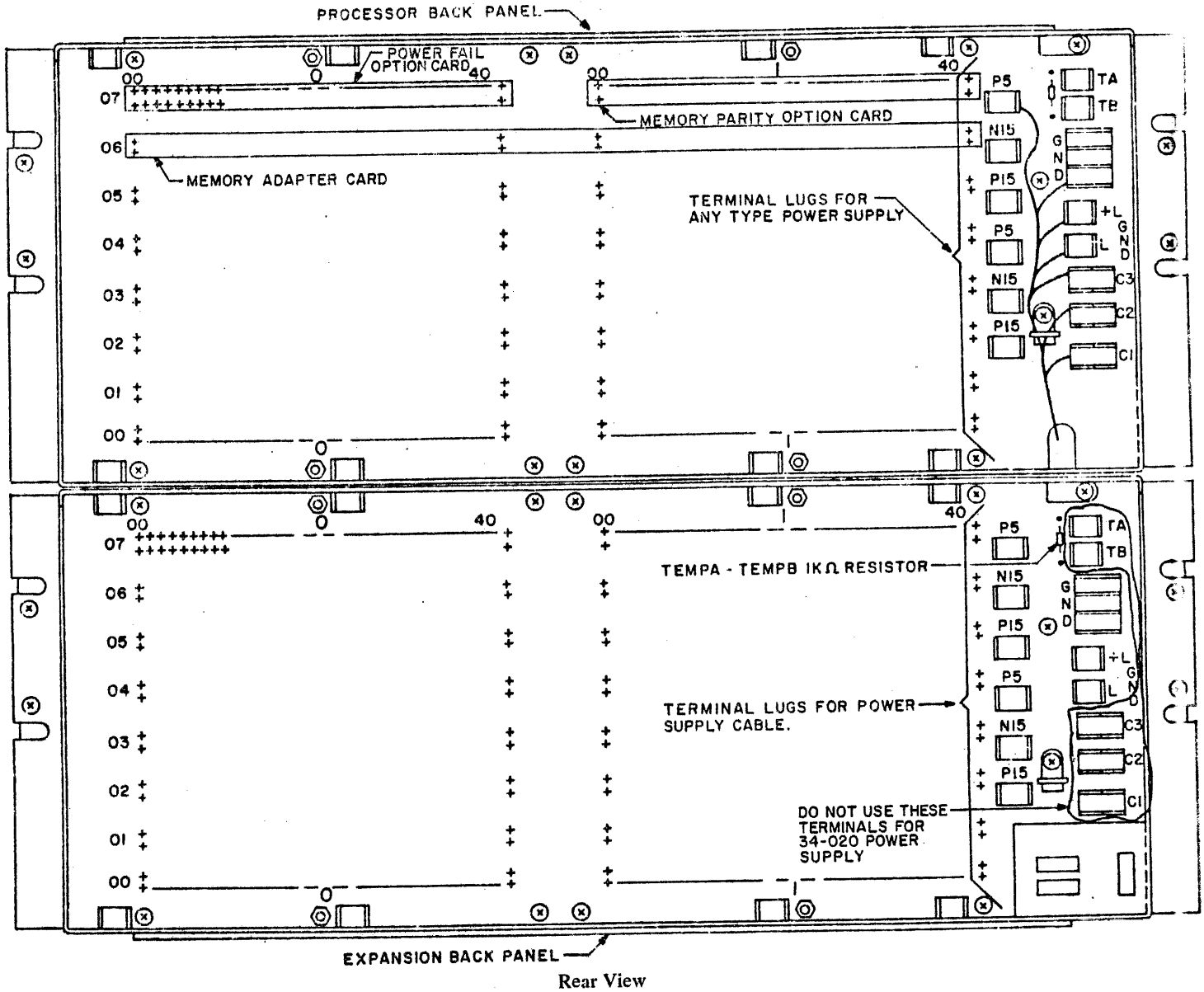
Selector Channel (SELCH) Installation

The 35-391 Selector Channel may be installed in Slot 4, 2, or 0 of the Processor Backpanel or in Slot 6 or Slot 4 of the Expansion Backpanel on a Twin Chassis version of the Processor. The maximum number of Selector Channels in a system is 4 for a Twin Chassis Processor or 3 for a 7 inch Chassis (refer to Figure 16). Also see the Selector Channel Installation Specification 02-232M01A20, for further information on installing SELCHs.



Front View

Figure 14. Front View of the 6/16 Twin Chassis



Rear View

Figure 15. Rear View Model 6/16 Twin Chassis

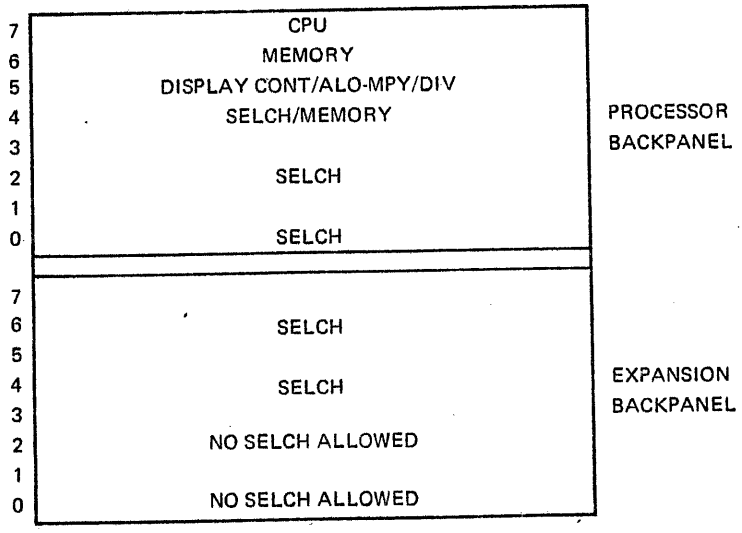


Figure 16. System Configuration (Front View)

Basic Switch Panel Option

For systems not equipped with either the Hexadecimal or Binary Display or Turnkey Console the Basic Switch Panel is used to start the system. The Installation Procedure for this Option is as follows:

1. Connect the four Faston lugs to the terminal strip located on the left side of the Processor Chassis. The terminal lugs are identified at the Faston connector and are mated to their corresponding terminal pin (C1, C2, etc.) on the chassis. (see Figure 11).

2. Remove the Faston connection on the Rear of the Processor Chassis labeled L-GND which comes from the Power Supply and connect this lug to a spare GND lug. Install a wire between the L-GND male receptacle, just vacated, and Back Panel pin INITO (136-0501). The panel on which the switch is installed may be mounted to the chassis uprights with standard 10-32 hardware. This panel is intended to mount behind a door or filler panel to prevent easy accessibility when the system is running. This option may not be used on a system on which a Display Panel is installed.

CONFIGURATION

System Expansion Chassis

When configuring a multi-chassis system there are four rules that must be followed:

1. The system Expansion Chassis must be mounted below the basic Processor Chassis.

2. All Chassis must be Contiguous.

3. All 15 inch system Expansion Chassis must be mounted above any 10 inch system Expansion Chassis.

4. Multiboard peripheral device Controllers (on 10 inch circuit boards) can only be used in the 10 inch system Expansion Chassis.

Circuit Board Distribution

The Model 6/16 Digital System may be configured in a variety of ways. However, the following factors must be considered when determining circuit board distribution within the basic Processor and system Expansion Chassis (see Figure 16).

1. The Selector Channel or Selector Channels must be installed in the slots described under SELCH Installation.

2. All device addresses are hard-wired on the device controller cards (device addresses may be changed at option), so that the distribution of I/O device controllers in the chassis normally need be considered as a matter of priority in the RACK0/TACK0 "daisy-chain".

3. The 15 inch system Expansion Chassis, and the basic Processor Chassis may only be used for single board I/O device controllers unless the interconnection between boards takes place via cables installed on the outer edge of the board. For multi-board 10 inch device controllers, the 10 inch system Expansion Chassis must be used.

4. The interrupt priority of a given device controller is determined by its physical location on the serial RACK0/TACK0 line. Refer to Interrupt Priority Back Panel Wiring to determine which physically located controller has what priority. When deciding which devices should have a higher or lower priority, devices that must be serviced in a certain amount of time or loss of data access should be given a higher priority than a device with a high interrupt rate and no data loss if not serviced.

Interrupt Priority Backpanel Wiring

The Acknowledge Control line from the Processor carries the Interrupt Acknowledge (ACK) signal. This line breaks up into a series of short lines to form the "daisy-chain" priority system. The ACK signal must pass through every controller that is equipped with Interrupt Control circuits. Refer to Figure 17 to determine order of priority.

Back panel wiring for interrupt control at a given position is: The Received ACK (RACK0) at Pin 122-0 or 1 and the Transmitted ACK (TACK0) at Pin 222-1 or 0. The daisy-chain bus is formed by a series of isolated lines which connect Terminal 222-1 or 0 of a given position to Terminal 122-1 or 0 of the next position (lower priority). On unequipped positions, a jumper shorts 122-1 or 0 and 222-1 or 0 of the same connector to complete the bus. Back panels are wired with jumpers on all positions. Whenever a card chassis position is equipped with a controller that has an interrupt capability, the jumper from 122-1 or 0 and 222-1 or 0 must be removed from the back panel at that position.

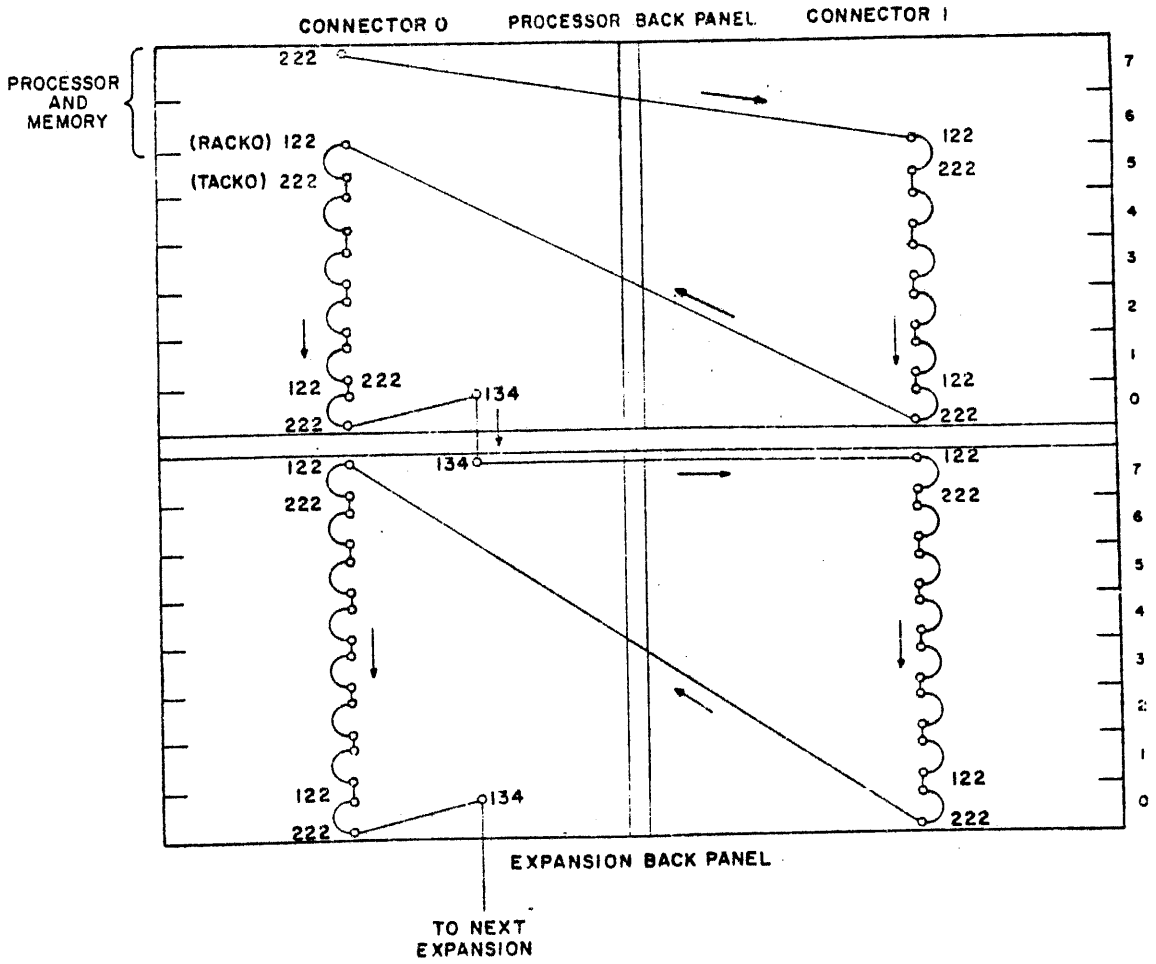


Figure 17. Standard Interrupt Priority

Figure 17, showing the standard interrupt priority wiring, assumes a Model 6/16 Processor and memory. The arrows indicate the direction of priority from the highest priority to the lowest. By changing the wires crossing from Side 0 to Side 1 of the PROC and/or Expansion Panels, interrupt priorities may be rearranged. An example of this is shown in Figure 18, Modified Interrupt Priority. Slot 5 on Side 1 of the Processor panel has the highest priority. When Selector Channels (SELCHs) or Bus Buffers are installed, the standard interrupt priority must be modified. Refer to Figure 19, Interrupt Priority with SELCH Installed.

For controllers that occupy several positions, the jumper is removed only at the position where the controller board has ATN/ACK circuits. For details on the various devices, see the appropriate installation specification.

Terminators

The termination end of both legs, Connector 0 and 1, of the Multiplexor Bus must have a standard INTERDATA termination card (35-433) installed if the bus is extended beyond a single 7 inch chassis or backpanel. These cards are installed on the back panel at the lowest numbered slot of both connectors on the Multiplexor Bus that exists; e.g., if a Selector Channel or bus buffer is installed in Slot 4 on the first expansion chassis and only the Processor Chassis and one Expansion Chassis is used in the system, the Multiplexor Bus must be terminated at Slot 0, Connector 0, and Slot 5, Connector 1 of the Expansion Chassis. In addition, the buffered bus or the SELCH Bus should be terminated at Slot 0, Connector 1 of this chassis.

Depending upon system configuration, any SELCH Bus or Buffered Bus may be terminated by a 15 inch Terminator (35-433) or a 10 inch Terminator (35-434). The choice of terminators depends on the type of chassis in which the last slot of the bus is present.

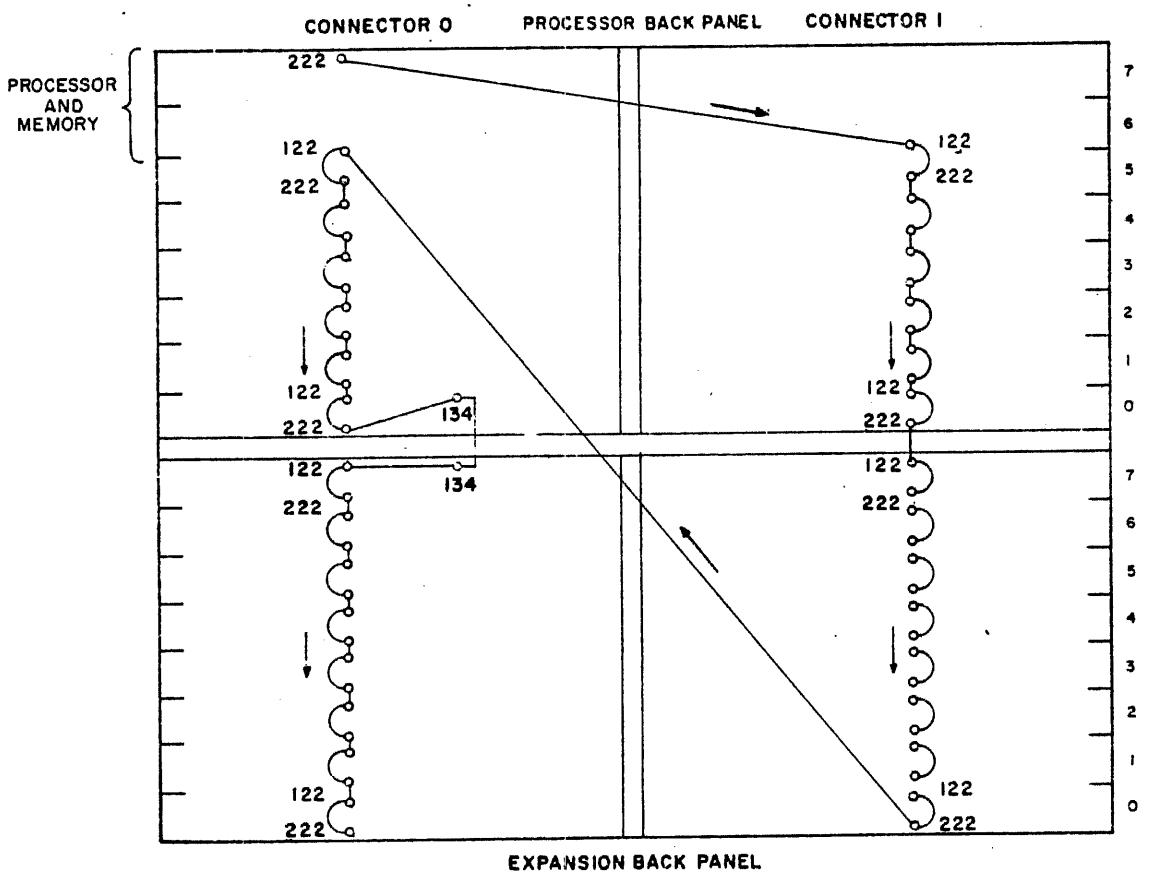


Figure 18. Modified Interrupt Priority

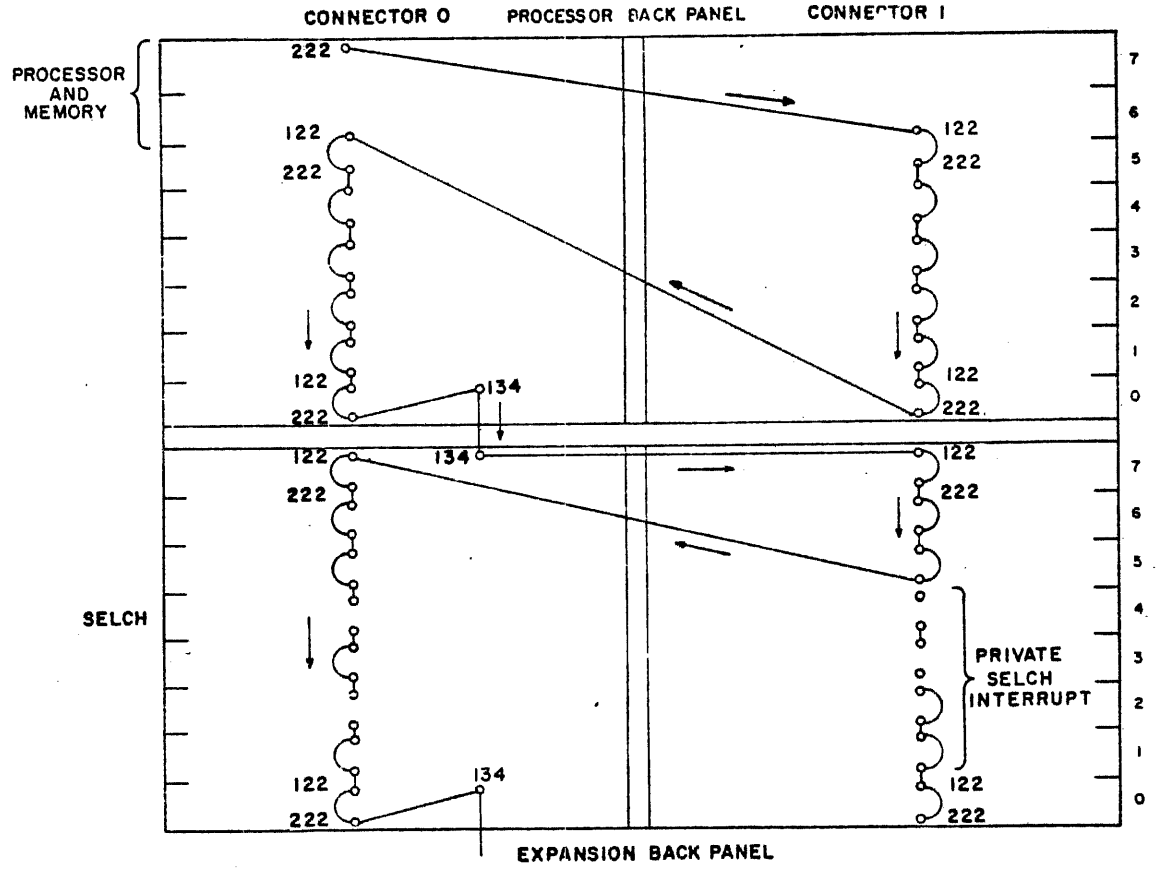


Figure 19. Interrupt Priority with SELCH Installed

CABLES

Power Cable

The standard INTERDATA Cabinet is wired for 30 Ampere service. On the main power cable (part of the AC Distribution Panel), there is a three wire, twist lock, grounding, 125VAC, 30 Ampere, UL, (Hubbel No. 2610) plug. A three wire grounding, 30 Ampere, 125 VAC receptacle (Hubbel No. 2611 or equivalent) is required to accept this plug.

System Expansion Cable

A number of standard cables are available for configuring systems made up of an INTERDATA Expansion Chassis. The choice of cables is dependent upon system configuration. The following cables are available:

1. 17-193: I/O Expansion Cable, Connector "0"

This cable is used to connect the "0" connector field between two adjacent 15 inch card files.

2. 7-194: I/O Expansion Cable (see note)

This cable is used to connect the "1" connector I/O fields between two adjacent 15 inch card files.

3. 17-216: I/O Expansion Cable, 36 Inch Long

This cable is used to connect two 15 inch files that are not adjacent. It must not be used to extend the basic Processor Multiplexor Bus.

It can be used to extend a buffered bus or a SELCH Bus. It plugs into a "1" side connector. The "receiving" end can plug into the "0" or "1" side of the expansion file.

4. 17-214: 15 inch to 10 inch Expansion Cable

This cable is used to connect the "0" connector field of a 15 inch card file to a lower adjacent 10 inch card file. It provides an 8 bit I/O bus to the 10 inch card file.

5. 17-166: 15 inch to 10 inch I/O Expansion Cable, 36 Inches Long

This cable is used to connect the "1" side of a 15 inch expansion file to a 10 inch expansion file. It provides an 8 bit I/O bus to a 10 inch card file.

It must not be connected to the basic Processor Multiplexor Bus.

It may be driven either by an Extended Selector Channel or a bus buffer.

It can be used on the older 10 inch card file (13 I/O slot).

6. 17-183: "0" to "1" Connector

This cable can be used to interconnect the I/O Multiplexor Bus of the "0" field and the "1" field within a 15 inch card file.

There is no RACK0/TACK0 wire in this cable.

It can also be used to connect a "0" side (Slot 0) of a file, to the "1" side (Slot 7) of the next adjacent file, or vice versa.

7. 17-215: 10 inch to 10 inch I/O Expansion Cable

This cable is used to connect two adjacent 10 inch card files.

NOTE

A strap is installed at the factory on the receive end of either a 17-327 or 17-194 cable. This strap must be removed unless the cable is being used to jumper a private I/O Bus (ESELCH or Bus Buffer). This strap jumpers Pin 222-0001 of the upper chassis to Pin 122-0701 of the first expansion chassis. If these cables are used to extend a SELCH or Bus Buffer the following wiring changes are required on the lower chassis:

Remove the strap from Pin 134-0700 to Pin 122-0701

Add a strap from Pin 134-0700 to Pin 122-0700

CONFIGURATION RULES

1. A maximum of 16 device controllers may be installed on the Multiplexor Bus of the Model 6/16. This assumes all drivers in the system are capable of sinking 48 milliamps or more and no more than one TTL load (2 milliamps max.) on any Control Line or Data Line on the device controllers. The Display Controller and Multiply/Divide option are considered one load each.

2. The Multiplexor Bus must be contained within the Processor Chassis and three adjacent 7 inch Expansion Chassis (two adjacent chassis if the Processor Chassis is a Twin Chassis). The Multiplexor Bus must be buffered by a Bus Buffer or the equivalent for systems which require the Multiplexor Bus to be extended beyond these limits or in the case where the Bus must be extended by any 36 inch cable.

01-094A21
September 1975

M71-SERIES
MODEL 6/16
MAINTENANCE SPECIFICATION

INTRODUCTION

The Model 6/16 Processor is a low cost, 16-Bit general purpose minicomputer. The latest MSI and LSI Integrated Circuit technology is used to construct a processor suitable for use in data communications, process control, or stand-alone scientific computer applications. The Model 6/16 Processor is modularly constructed for ease of maintenance and is compatible with all building blocks in the INTERDATA product line.

SCOPE

This specification describes the functional operation of the Model 6/16 Processor and provides maintenance information useful to digital technicians maintaining this processor. A block diagram analysis, a micro-program description, and a functional analysis of major processor areas are included.

BLOCK DIAGRAM ANALYSIS

The following sections make reference to Figure 1.

System Organization

The Model 6/16 is organized between two 16-bit buses. The B Bus is used to present data to the Arithmetic Logic Unit (ALU). The S Bus then transfers the ALU output to the appropriate destination. The source and destination of data on the B Bus and S Bus as well as the functions performed by the ALU are controlled by micro-instructions contained in the Read-Only-Memory (ROM).

Read Only Memory (ROM)

The Read-Only-Memory is a high speed, solid state, non-destructive memory organized into one page of 512 words. An additional page of 512 words is available for expansion (e.g., Multiply/Divide option). Each word in ROM is 24 bits long and represents one micro-instruction. Each micro-instruction read out of ROM is latched at the ROM output by latches internal to the ROM. Most micro-instructions are executed in one machine cycle. The ROM bits are decoded to select a Source to be statically unloaded to the B Bus as well as a second Source to be directed to the ALU (see Figure 1). The ALU then forms a result on the S Bus. This result becomes available some time before the end of the machine cycle and is deposited in the appropriate destination register at the start of the next machine cycle as the next micro-instruction is fetched. The meaning of the micro-instruction word bits is explained later.

Locations in the ROM are addressed by the 10-bit ROM Address Register (RAR). Micro-instructions are normally located at sequential addresses in the ROM. The RAR is an up-counter which increments by one before each new micro-instruction is fetched. The RAR therefore holds the address of the micro-instruction presently being executed. When it becomes necessary to jump out of sequence, the RAR can be loaded with a new address from the ROM, from the Decoder ROM (DROM), or it can be preset by hardware.

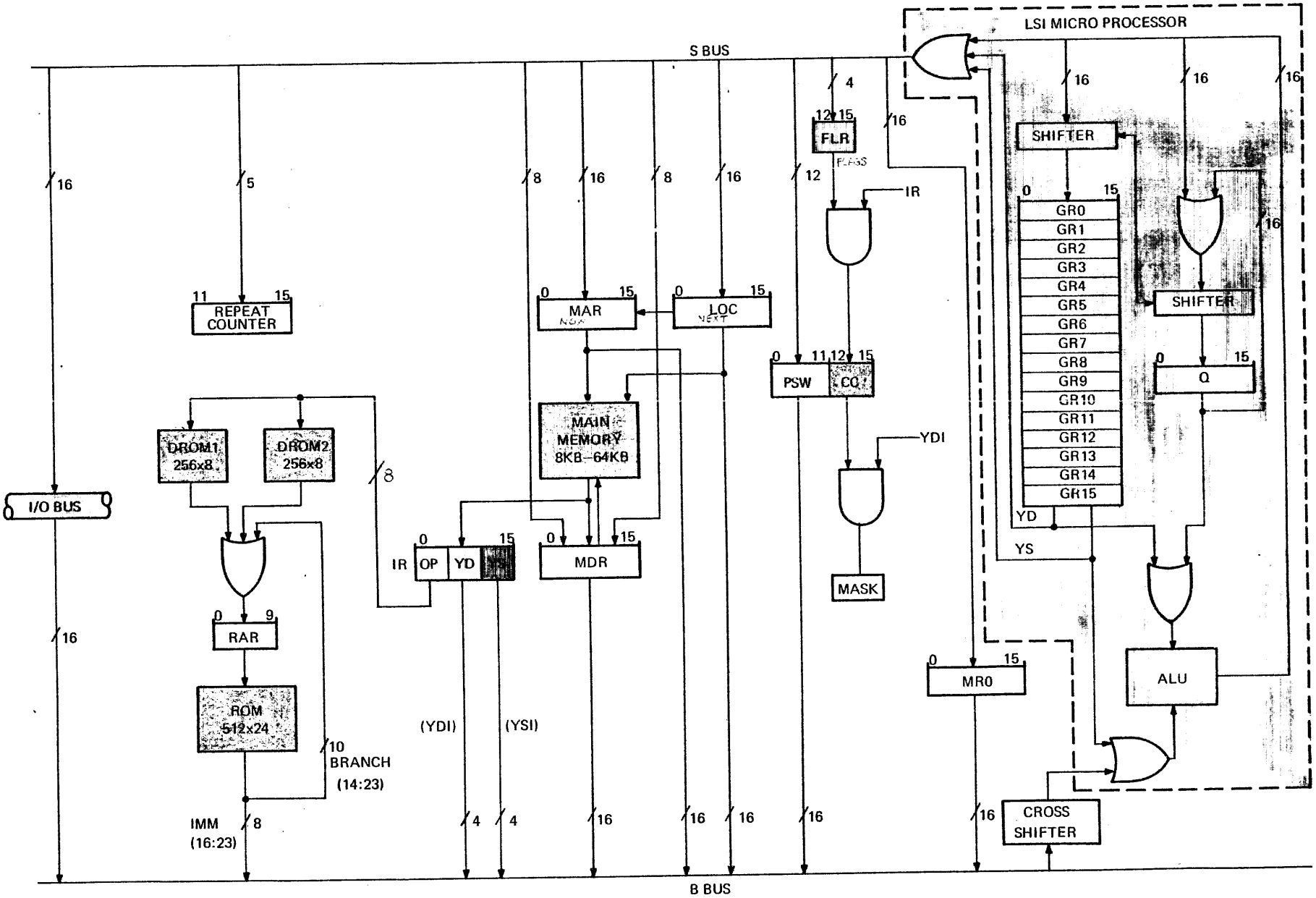


Figure 1. Block Diagram 6/16 IWLM

Repeat Counter

The Repeat Counter is a 5-bit counter which can be loaded from the S Bus. The purpose of this counter is to allow a micro-instruction to be executed n number of times (where $n \leq 31$) before the next micro-instruction is fetched. The next micro-instruction in sequence following the micro-instruction which loads the Repeat Counter is the one which is automatically repeated n-times.

Flag Register (FLR)

The Flag Register (FLR) is a four-bit register containing the following flags: Carry (C), Overflow (V), Greater Than Zero (G), and Less Than Zero (L). These flags are modified at the conclusion of arithmetic and logical micro-operations to reflect the result of the operation. The FLR is loaded from Bits 12 through 15 of the S Bus when either the FLR or the Program Status Word (PSW) is the specified Destination Register.

Program Status Word (PSW)

The Program Status Word (PSW) is a 16-Bit register used to indicate the system status relative to the user program being executed. Bits-0 through 6 of the PSW define enabled interrupts and the operational status or mode of the user level processor. PSW Bits-7 through 11 are not defined. Some of the PSW bits have hardware significance while others are of significance only to the micro-program. Bits-12 through 15 of the PSW make up the Condition Code field (CC) which reflects the result of the most recent user instruction. Bits-8 through 11 are not provided.

The Condition Code may only be updated from the FLR. When PSW is the Specified Destination Register Bits-0 through 7 of the S Bus are loaded into Bits-0 through 7 of the PSW and S Bus Bits-12 through 15 are captured in the FLR. The Condition Code field is then updated from the FLR on the next Processor clock. Instruction Read operations also copy the contents of the FLR into the Condition Code.

Location Counter

The Location Counter (LOC) is a 16-bit appendum to the PSW which holds the main memory address of the next user instruction to be performed. The Location Counter is an up-counter which automatically increments by 2 following each Instruction Read micro-instruction or D1 option in the micro-instruction (unless the op-code indicates an RR or SF format instruction). Bit-15 of this register is not implemented.

Memory Address Register (MAR)

The Memory Address Register (MAR) is a 16-bit register which is loaded with the address of main memory locations. It is automatically loaded from the Location Counter each time LOC is incremented. It can also be loaded from the S Bus whenever LOC or MAR is the specified Destination Register.

Main Memory

The Main Memory consists of random access memory providing storage for user instructions and data. Memory is addressed through the Memory Address Buffer (MAB). The MAB is constructed using 2:1 Multiplexors. On Instruction Reads the contents of the Location Counter is presented as the address to Main Memory. On all other memory operations the contents of the MAR is presented as the address for Main Memory. Data read from or written into memory is buffered in the Memory Data Register (MDR). The micro-program initiates a main memory cycle by using a Memory Read, Memory Write, or Instruction Read command. After issuing a memory command, the micro-program is free to perform other instruction. The memory cycle is accomplished asynchronous of other processor activity. If the micro-program, however, attempts to use the contents of MDR after a Memory Read or Instruction Read operation, before memory data become available, or attempts to load MDR or issue another Memory command before the current memory cycle is complete, the processor stops until the desired function can be performed.

Instruction Register (IR)

On Instruction Read operations data on the Memory Register Receive Bus (MRR), MRR Bits-0 through 7 are placed in the register labeled OP, Bits -8 through 11 are placed in the register labeled YD, and Bits-12 through 15 are placed in the register labeled YS. These three registers (OP, Yd, and YS) comprise the user's Instruction Register.

Decoder Read-Only Memory (DROM)

The OP register is used to address locations in the Decoder Read-Only-Memory (DROM). The DROM consists of two halves: DROM 1 and DROM 2. Each half contains 256 8-bit words. The micro-program interrogates either DROM 1 or DROM 2 at appropriate times and the 8 bits of the resulting read-out are jammed into the RAR, resulting in an automatic branch to an address that is related to the user's operation code. The most significant bit of DROM 1 is used to suppress unnecessary memory reads and Location Counter increments. The DROM also decodes all illegal user instructions.

Micro Register (MR)

A 16-bit register labeled MR0 is available to the micro-program for general purpose use.

Input/Output (I/O)

Input/Output operations are achieved by gating S Bus data onto the I/O Bus and activating an I/O Control Line, or by activating an I/O Control Line and gating the I/O Bus data onto the B Bus.

LSI Micro-processor

The LSI Micro-processor is comprised of four Large Scale Integrated (LSI) Circuits, each of which is a 4-bit wide slice of the Central Processing Unit (CPU). Four of these CPU slices make up the 16-bit wide CPU. The combined slices contain a 16-bit Arithmetic Logic Unit (ALU), a two port Random Access Memory (RAM) Stack forming sixteen 16-bit General Registers, a 16-bit temporary storage register Q, shift circuits for right, left, and no shift for the RAM stack and Q register. By external circuits connecting the Q shift and RAM shift circuits 32-bit shifts and rotates are made possible with Q as one of the registers and one of the sixteen general registers as the second register.

It is most often the case that the micro-program accesses the User's General Register without caring which of the 16 General Registers is accessed. Consequently, no provision has been made in the Model 6/16 for the micro-program to randomly access an explicit General Register. Since after Instruction Read, one or more register addresses specified by the user instruction, are in the YD and YS register, the micro-program can access the appropriate General Register by specifying the YD or YS Register. The hardware then selects the General Register whose number is in the YD or YS Register.

The YD Register is an up/down-counter so that sequential General Registers can be accessed. The micro-program can also clear the YD Register when it needs to access a specific General Register.

MICRO-PROGRAM DESCRIPTION

Introduction

Micro-programming is a means for implementing the control logic of a digital processor. At INTERDATA, micro-programming has been effectively used to maintain upward program compatibility in a family of processors whose internal hardware varies from one member to the next.

The Model 6/16 Processor is designed to execute micro-instructions stored in a Control Store or Read-Only Memory (ROM). A micro-instruction is an elemental step or instruction to the actual hardware of the machine. Each micro-instruction causes one or more hardware functions to be performed, such as transferring the contents of one register to another, arithmetic or logical operations between two specified operands, controlling input/output operations or performing memory functions.

A series of micro-instructions is called a micro-program. The complete Model 6/16 micro-program is, by definition, an emulator, causing the Model 6/16 to react to a user program in main memory and to external events as does the Model 7/16 Processor, described in the *INTERDATA 16-Bit Reference Manual,* Publication Number 29-398. Every user level instruction, interrupt handling feature, etc. is simulated by some portion of the Model 6/16 Processor micro-program.

The following pages outline the Model 6/16 hardware from a micro-programmer's point of view, data and instruction formats, instruction repertoire and interrupt system.

DATA AND INSTRUCTION FORMATS

Data Formats

All internal data paths are 16-bits wide. Hence the basic machine operand is a 16-bit halfword. In arithmetic operations, the most significant bit is interpreted as the sign bit of the number in the least significant 15 bits of a halfword: Positive fixed-point data is expressed in true binary form with a sign bit of Zero. Negative fixed-point data is expressed in twos complement notation with a sign bit of One.

Binary information is represented in hexadecimal notation, base 16, for simplicity.

Instruction Formats

Model 6/16 Processor micro-instructions can be one of five formats designated Register-to-Register, Register-to-Immediate, Input/Output, Branch and Exchange Byte. The Instruction word formats are shown in Table 1 and Figure 2. Instruction word fields are explained in the following sections. (Refer to Table 2.)

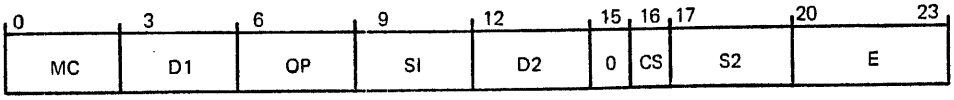
TABLE 1. INSTRUCTION WORD CHART

INSTRUCTION WORD BITS										
	MC	D1	ALU OP	S1	D2	IMMEDIATE	S2	E FIELD		
	0 1	3 4 5	6 7 8	9 10 11	12 13 14	15 16	17 18 19	20 21 22 23		
NOP	0 0 0							0 0 0 0	NULL	
D2	0 0 1							0 0 0 1	ADR/ACK	I/O-$\overline{BR}$-$\overline{IMM}$
MR	0 1 0							0 0 1 0	CMD/STAT	
MW	0 1 1							0 1 0 0	DA/DR	
BT	1 0 0									
BF	1 0 1							0 0 0 1	CLEAR YD AND SET WAIT	$\overline{I/O}$-$\overline{BR}$-$\overline{IMM}$
JAM CC+IR	1 1 0									
D1	1 1 1							0 0 1 0	YDP1	
								0 0 1 1	YDM1	
LOAD Q; ALU OUTPUT		0 0 0								
NULL; ALU		0 0 1						0 1 0 0	POW	
LOAD YD AND Q; FA OUTPUT		0 1 0						0 1 0 1	JAM CI 4C0	FOR INC, DEC ONLY
LOAD YD; ALU OUTPUT		0 1 1			0 0 0			0 1 1 0	M/D	
LOAD YD AND Q;SR;ALU OUTPUT		1 0 0						0 1 1 1	FLT PT	
LOAD YD; SR; ALU OUTPUT		1 0 1								
LOAD YD AND Q; SL; ALU OUTPUT		1 1 0						1 0 0 1	CI	
LOAD YD; SL; ALU OUTPUT		1 1 1						1 0 1 0	CO	$\overline{I/O}$-$\overline{BR}$-$\overline{IMM}$
LOAD YS; ALU OUTPUT		0 1 1			0 0 1			1 1 0 0	F	
							1 1 1	1 0 0 0	UNLOAD M/D BOX ON I/O BUS	
	R+S		0 0 0							
	S-R		0 0 1							
	R-S		0 1 0							
	R OR S		0 1 1							
	R AND S		1 0 0							
UNUSED	$\overline{R}$ AND S		1 0 1							
	R XOR S		1 1 0							
	R XNERS		1 1 1							
		R	S							
		YS	Q	0 0 0						
		YS	YD	0 0 1						
		0	Q	0 1 0						
		0	YD	0 1 1						M/D: DIFFERENTIATED BY# SOURCE HALFWORDS FLTPT: DIFFERENTIATED BY IR00:07
		0	YS	1 0 0						
EXTERNAL SOURCE		D	YD	1 0 1						
		D	Q	1 1 0						
		D	0	1 1 1						
		0 0 1		PSW	0 0 0		0 0 0	PSW		
				LOC	0 0 1		0 0 1	LOC		
				MR0	0 1 0		0 1 0	MR0		
		0 0 0		CNTR	0 1 1		0 1 1	YSI		
		OR		MDR	1 0 0		1 0 0	MDR		EXT-SOURCE-$\overline{BR}$-$\overline{IMM}$
		0 0 1		MAR	1 0 1		1 0 1	MAR		
				FLR	1 1 0		1 1 0	YDI		
				IO	1 1 1		1 1 1	IO		
					NULL	0 0				
					IMM	1 X				
					CS	0 1				

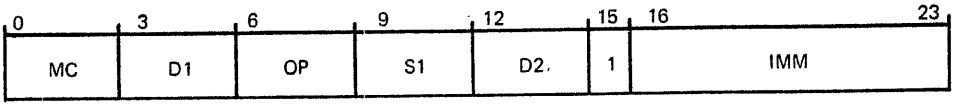
BRANCH	8 CONDITION 13, 14	23 ADDRESS
C	0 0 0 1 1 1	
V	0 0 1 0 1 1	
G	0 0 1 1 0 1	
L	0 0 1 1 1 0	
MSK	0 1 0 1 1 1	
ARST	0 1 1 0 1 1	
DATN	0 1 1 1 0 1	
	0 1 1 1 1 0	
ATN	1 0 0 1 1 1	
CATN	1 0 1 0 1 1	
SNGL	1 0 1 1 0 1	
MALF	1 0 1 1 1 0	
AMOD	1 1 0 1 1 1	
ALO/HW	1 1 1 0 1 1	
PPF	1 1 1 1 0 1	
MPE	1 1 1 1 1 0	
UNCOND	0 0 1 1 1 1	

ALO: ADDRESSED ON POWER UP
KNOCKED DOWN WHEN
OTHER DEV. ADDRESSED

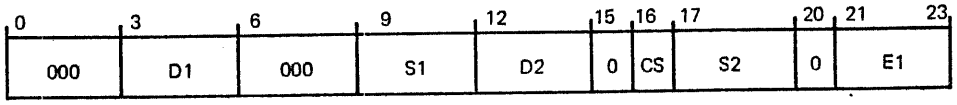
REGISTER TO REGISTER



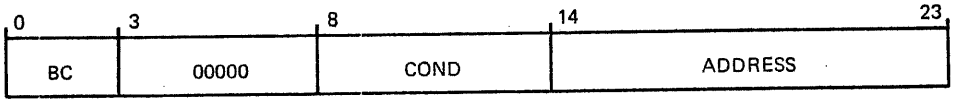
REGISTER TO IMMEDIATE



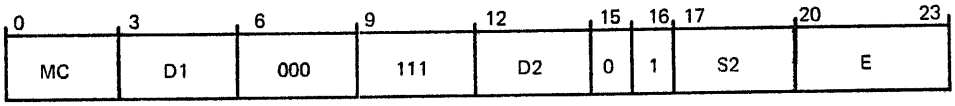
INPUT/OUTPUT



BRANCH



EXCHANGE BYTE



INSTRUCTION WORD FIELDS

FIELD	MEANING
MC/BC	MAIN MEMORY CONTROL/BRANCH CONTROL
D1	SHIFT LEFT/SHIFT RIGHT OPERATION
D1 AND D2	DESTINATION FIELD
OP	ALU OPERATION
S1	SELECTS TWO SOURCES FOR ALU
S2	SELECT EXTERNAL (TO ALU) SOURCE
E	EXTENSION FIELD
E1	SPECIFIED TYPE OF I/O OPERATION
COND	BRANCH CONDITION(S)
ADDRESS	BRANCH ADDRESS
CS	SPECIFIES CROSS-SHIFT

Figure 2. Instruction Word Formats

Memory Control (MC)

The processor's main memory is the source of user's instructions and data. The Register-to-Register and Register-to-Immediate micro-instructions can specify one of the following options to perform main memory operations or to use the Decoder Read-Only-Memory (DROM).

TABLE 2. MC/BC FIELD

Instruction Word Bits 0 1 2	Meaning
000	No operation
001	D2—Vector through DROM2
010	MR—Data Read Halfword
011	MW—Data Write Halfword
100	BT—Branch on True Condition
101	BF—Branch on False Condition
110	IR—Instruction Read and Jam CC
111	D1—Vector through DROM1

D2: The user's instruction op-code, IR (0:7), is used to vector through DROM2. The unique word from DROM2 is jammed into RAR, causing a branch in the micro-program sequence.

MR: A main memory read operation is started using the contents of MAR as the memory address. Then the micro-instruction execution starts. The halfword is read from memory and is loaded into this MDR for use by the micro-program when the data is available.

MW: A Main Memory Write operation is started. The current content of MDR is written into the halfword of memory currently addressed by the content of MAR.

BT: If any of the specified conditions are true, a branch is taken to the address specified in the address field.

BF: If all of the specified conditions are false, a branch is taken to the address specified in the address field. An unconditional branch micro-instruction assembles as a branch on false micro-instruction with no conditions specified.

IR: An Instruction Read operation is started prior to execution of the current micro-instruction. The halfword addressed by the current contents of LOC is read and placed in both the MDR and the Instruction Register (IR). LOC is then incremented by two and the incremented LOC is jammed into the MAR. The current content of FLR is copied into the condition code field of PSW. (LOC must not be the destination register in the micro-instruction specifying the IR option.) The FLR is cleared and the micro-instruction at ROM location '000' is executed.

D1: The address of the next micro-instruction is extracted from DROM1 using the user's instructions op-code, IR (0:7), as an index.

Commands (E)

A Register-to-Register or Exchange Byte micro-instruction can specify one of the following six commands to perform the desired hardware function. These commands are executed at the end of the micro-instruction.

Word Word Bits				Meaning	
20	21	22	23		
0	0	0	1	CYD and SWA	Clear YD field and set Wait FF
0	0	1	0	YDP1	Increment YD field
0	0	1	1	YDM1	Decrement YD field
0	1	0	0	POW	Power down, Generate System Clear
0	1	1	0	M/D	Load data into M/D box
0	1	1	1	FLTPT	Specify Floating Point operation

Condition Code Options (E)

A Register to Register or Exchange Byte micro-instruction can specify up to three options in this category.

Instruction Word Bits				Meaning	
20	21	22	23		
1	0	0	1	CI	Carry In
1	0	1	0	CO	Carry Out
1	1	0	0	F	Set Test Flags in FLR

CI: In a Load micro-instruction specifying this option, the Carry Flag (P/O FLR) is shifted into the most significant bit of the result if Shift Right is also specified. If Shift Left is specified, the Carry Flag is shifted into the least significant bit of the result. While executing an Add micro-instruction, the Carry Flag is added to the least significant bit of the sum.

In a subtract micro-instruction, the Carry Flag represents a borrow situation from the least significant bit of the subtraction. This borrow participates in the subtraction operation.

CO: In a Load micro-instruction specifying this option, the Carry Flag in FLR stores the bit shifted out, if a Shift Right or Shift Left is also specified. If shift is not specified, the Carry Flag is reset.

In an Add micro-instruction, the Carry Flag is set if a carry is generated. In the subtraction, carry is reset if a borrow is not generated. If a micro-instruction specifying CO performs a logical operation, the Carry Flag in FLR is reset.

F: If a micro-instruction specifying this option performs addition or subtraction, V, G and L Flags in FLR are adjusted to reflect the result of the operation. The V Flag reflects the overflow condition and Flags G and L reflect the algebraic value of the result.

In an I/O instruction, the V Flag is set if the addressed device does not return a SYNC in approximately 14 microseconds. If a micro-instruction specifying this option performs a load or logical operation, the V Flag is reset and the G and L Flags are adjusted to reflect the algebraic value of the result.

The hardware provides a cumulative flag effect to facilitate multi-precision operations. The following table shows how the G and L Flags in FLR are adjusted to reflect the algebraic value of the result. Note that once the G or L Flag becomes set, the G and L Flags will never again both be Zero unless the FLR is explicitly cleared (e.g., an Instruction Read operation).

Result	Flags before Execution		Flags after Execution	
	G	L	G	L
Zero	0	0	0	0
	0	1	1	0
	1	0	1	0
Positive	0	0	1	0
	0	1	1	0
	1	0	1	0
Negative	0	0	0	1
	0	1	0	1
	1	0	0	1

Shift Options

A Register-to-Register or Register-to-Immediate micro-instruction can specify either the Shift Left or Shift Right option. There are no specific bits in the micro-instruction word for the SL or SR options. However, this information is included in Bits-3, 4 and 5. The micro-instruction must specify YD or YD&Q as the destination register or registers. Other desired options may be specified.

SL: The 16-Bit Arithmetic Logic Unit result is shifted left one bit position. If CI is also specified, the state of the Carry Flag in FLR is shifted into the least significant bit position, otherwise, the least significant bit is forced to Zero. If CO is also specified, the most significant bit of the ALU result, which is shifted out, is shifted into the Carry Flag of the FLR; otherwise, that bit is lost. The 16-bit result thus obtained is copied into the destination register or registers.

SR: The 16-bit ALU result is shifted right one bit position. If CI is also specified, the state of the Carry Flag in FLR is shifted into the most significant bit position; otherwise, the most significant bit is forced to Zero. If CO is specified, the least significant bit of the ALU result, which is shifted out, is shifted into the Carry Flag of FLR; otherwise, that bit is lost. The 16-bit result, thus obtained, is copied into the destination register or registers.

Branch Conditions

A Branch micro-instruction can specify up to four conditions from Group 0, Group 1, Group 2 or Group 3. Conditions from different groups cannot be mixed in the same instruction. The micro-instruction word bits, symbolic conditions and their meanings are shown below.

GROUP	WORD BITS 8 9 10 11 12 13	SYMBOLIC CONDITION	MEANING OF TRUE CONDITION
0	0 0 0 1 1 1	C	CARRY FLAG SET
	0 0 1 0 1 1	V	OVERFLOW FLAG SET
	0 0 1 1 0 1	G	GREATER THAN ZERO FLAG SET
	0 0 1 1 1 0	L	LESS THAN ZERO FLAG SET
	0 0 1 1 1 1		UNCONDITIONAL BRANCH
1	0 1 0 1 1 0	MSK	(YD) AND (CONDITION CODE FIELD) 0
	0 1 1 0 1 1	ARST	AUTO-RESTART PRESENT
	0 1 1 1 0 1	DATN	DMA ON I/O BUS IS REQUESTING ATTENTION
2	1 0 0 1 1 0	ATN	I/O ATTENTION AND PSW BIT 1 ARE SET OR DMA ON I/O BUS IS REQUESTING ATTENTION
	1 0 1 0 1 1	CATN	CONSOLE ATTENTION REQUESTED
	1 0 1 1 0 1	SNGL	CONSOLE IS IN SINGLE MODE
	1 0 1 1 1 0	MALF	MACHINE MALFUNCTION DETECTED
3	1 1 0 1 1 1	AMOD	ADDRESS MODIFICATION IS NECESSARY
	1 1 1 0 1 1	HW	HALFWORD I/O LINE IS ACTIVE/ALO PRESENT INDICATION ON POWER UP
	1 1 1 1 0 1	PPF	PRIMARY POWER FAIL DETECTED
	1 1 1 1 1 0	MPE	MEMORY PARITY ERROR DETECTED

THE MICRO-PROGRAM

The Model 6/16 Processor micro-program can be divided into three major functional areas. These are: user instruction fetch; user instruction execution; and interrupt support. Refer to Figure 3.

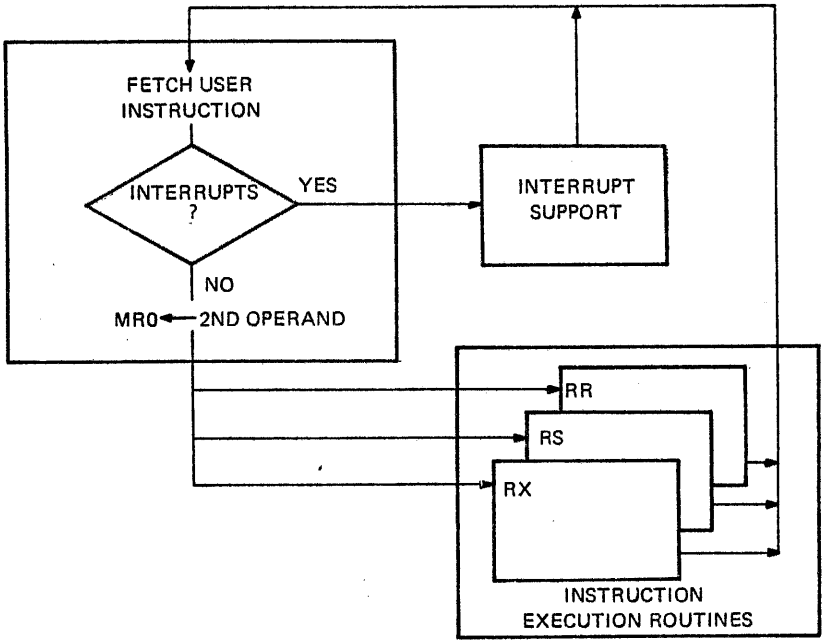


Figure 3. Micro-Program Functional Areas

System Initialization

On power up, or following initialize, when the System Clear signal (SCLR0) goes high, the Processor starts executing micro-instructions. SCLR0 presets the ROM Address Register (RD) to X'100'.

Referring to Figure 4, address X'100' corresponds to the symbolic label PWRUP on the flow chart.

The micro-program checks if Automatic Loader Option (ALO) is present. If the ALO exists, the HW line is active. The test for HW passes and routine ALO1 is entered. If the HW test fails, the micro-program continues the normal power-up sequence.

NOTE

The Automatic Loader Option (ALO) is a halfword oriented device but it does not have a specific device address. If it is present in the system and enabled then on power-up or initialize, the HW line is activated. The micro-program detects this and loads new PSW and LOC and up to 4K bytes of main memory from the ALO. Depending on the new PSW, the user level Processor goes into the Wait State or user instruction execution starts.

In the Auto Load Option route (AL01), the micro-program reads in a new PSW and LOC, a starting Memory Address and an ending Memory Address from the ALO. The micro-program then forms in YD the difference between the ending address and the starting address. If a carry is produced, the end address was less than the start address. Routine IDLE is entered. If the end address is not less than the start address, the data input loop, AL02, is entered. The data halfwords are read from the ALO and stored in consecutive halfword locations in main memory until the difference count in YD is decremented from X'000' to X'FFFF'. When this happens, all the data has been loaded into Main Memory. Then Bit-0 of the PSW (Wait Bit) is tested. If it is set WAIT routine is entered. Otherwise, user instruction fetch is started. (See Figure 5.)

In the normal power-up sequence, the PSW and LOC are restored from their power fail save locations, X'0024' and X'0026' in main memory, and the user's General Registers are restored from their main memory power fail save locations. The General Register save area is a 32-byte block of memory whose starting address is contained in memory location X'0022'.

After restoring the registers, Bits-13, 14, and 15 of location X'20' are examined to determine the last display panel status. If non-Zero, the Hexadecimal Display Panel was not in the Run mode when power went down. LOCDIS is entered. If Zero, the Hexadecimal Display Panel was in the Run mode. The Auto-Restart, ARST, option is tested. If set, routine MMF is entered to do the Machine Malfunction interrupt if PSW Bit-2 is set. If the ARST option is absent, routine LOCDIS is entered to display the present values of the location Counter. The IDLE loop is then entered.

Hexadecimal Display Panel Support

The Hexadecimal Display Panel is serviced by two major routines: CONSER and DISPLY. Routine CONSER is entered, if during user instruction execution, the micro-program determines that CATN is active; or if in the IDLE loop or the WAIT loop, CATN becomes active but SNGL is not active. See Figure 6.

In the CONSER routine, the Display Controller is addressed and its status is sensed. It is put into the normal mode and addressed to reset byte counter. The most significant four bits of the status byte are stored as the least significant four bits of location X'20'. If the SNGL signal is active, the LOC is incremented by two, the FLR is cleared and the micro-program returns to the user instruction fetch routine at START 1. If SNGL is not active, the Hexadecimal Display status is examined.

If status Bit-1 is set a function or a register has been selected. Routine FNREG is entered. If status Bits-0, 4, 5, 6 and 7 are all reset, Function 0 was selected. If PSW Bit-4 is also set, the micro-code simulates an interrupt from device number 1 (Hexadecimal Display Panel Interrupt). If PSW Bit 4 is reset, routine CLRWT is entered to fetch the next user instruction.

If status Bit-1 is reset, MDR gets data from memory location specified by LOC. If the Display status indicates Address or Memory Write, routine ADWRT is entered. The Switch Register is read into MDR and if the mode is Address, routine ADD is entered; where the data in MDR is copied to LOC and routine LOCDIS is entered. If the mode is Memory Write, routine RDKEY is entered, where the data in MDR is written to the memory location specified by LOC. LOC is then incremented by two and copied to MAR. The data written is copied into MR0 and MDR is set equal to X'80' to light the Memory Address/Memory Data lamp. Routine OUTDIS is entered.

If the mode is Memory Read, the RDKEY routine is entered.

Display status Bits-1, 2, and 3 being reset indicate Run mode. Routine CLRWT is entered to fetch the next user instruction.

Routine DISPLY is entered from routine CONSER if the status indicates that a function other than Function 0 or a Register was selected; or before the interruptable Wait loop is entered, if SNGL is active. See Figure 7.

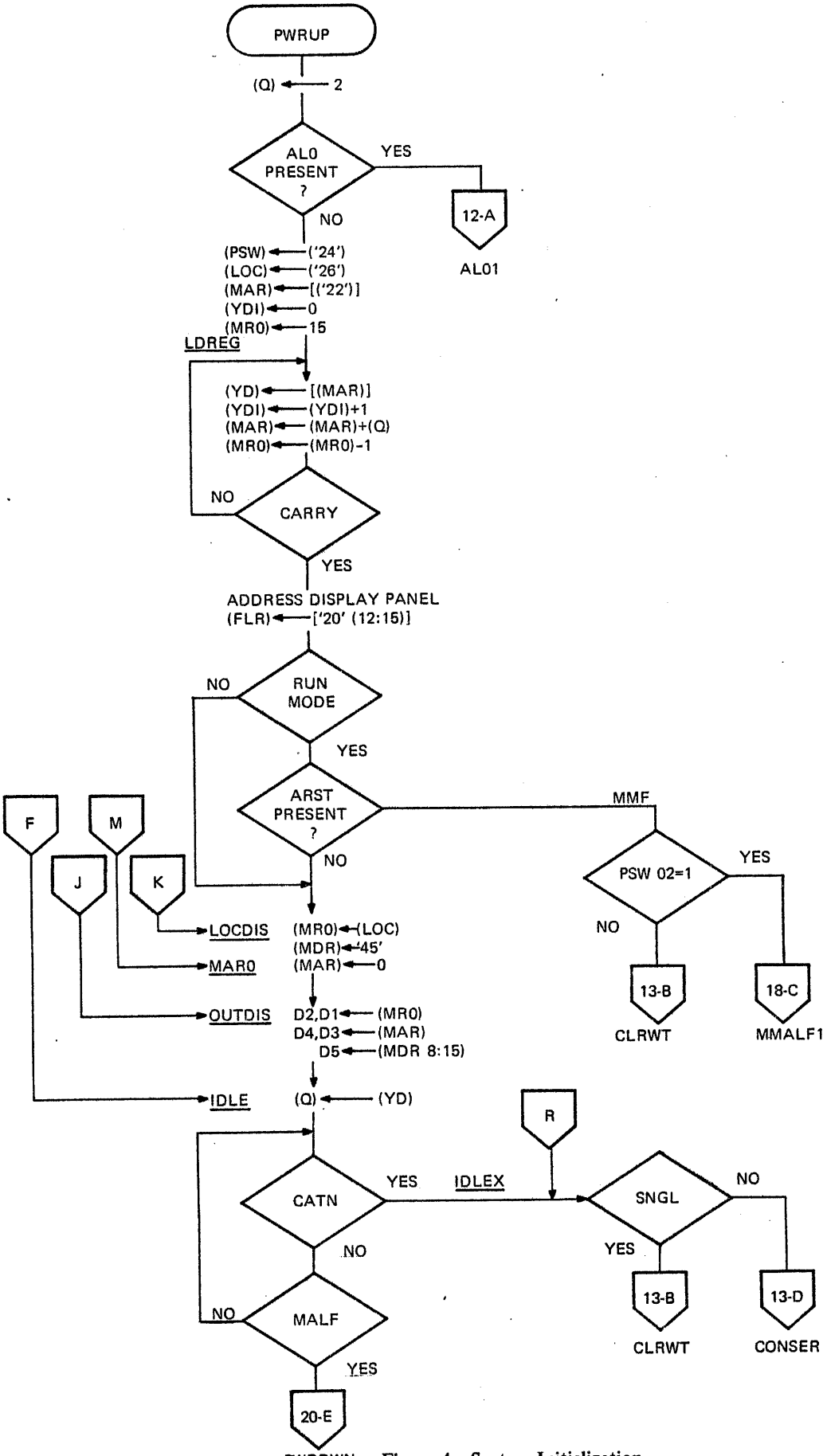


Figure 4. System Initialization

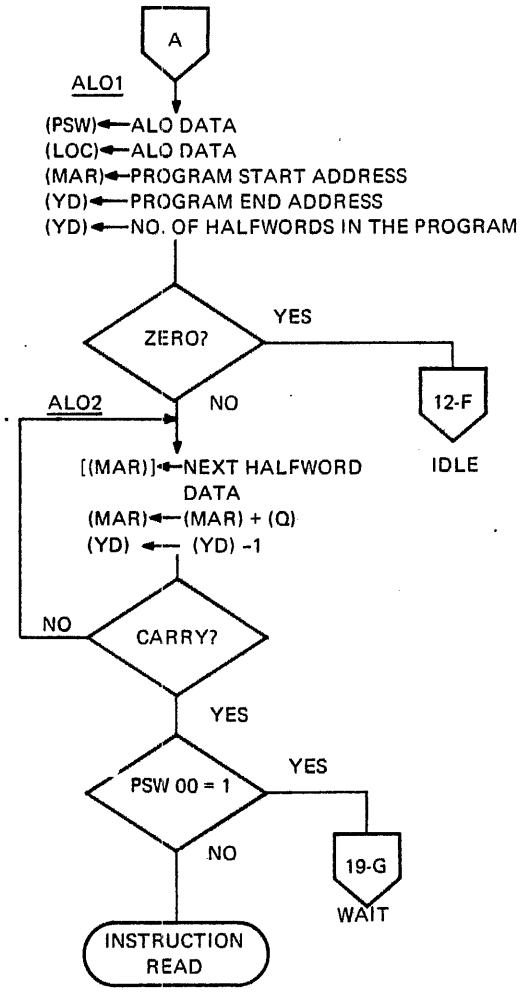


Figure 5. Auto Load Option

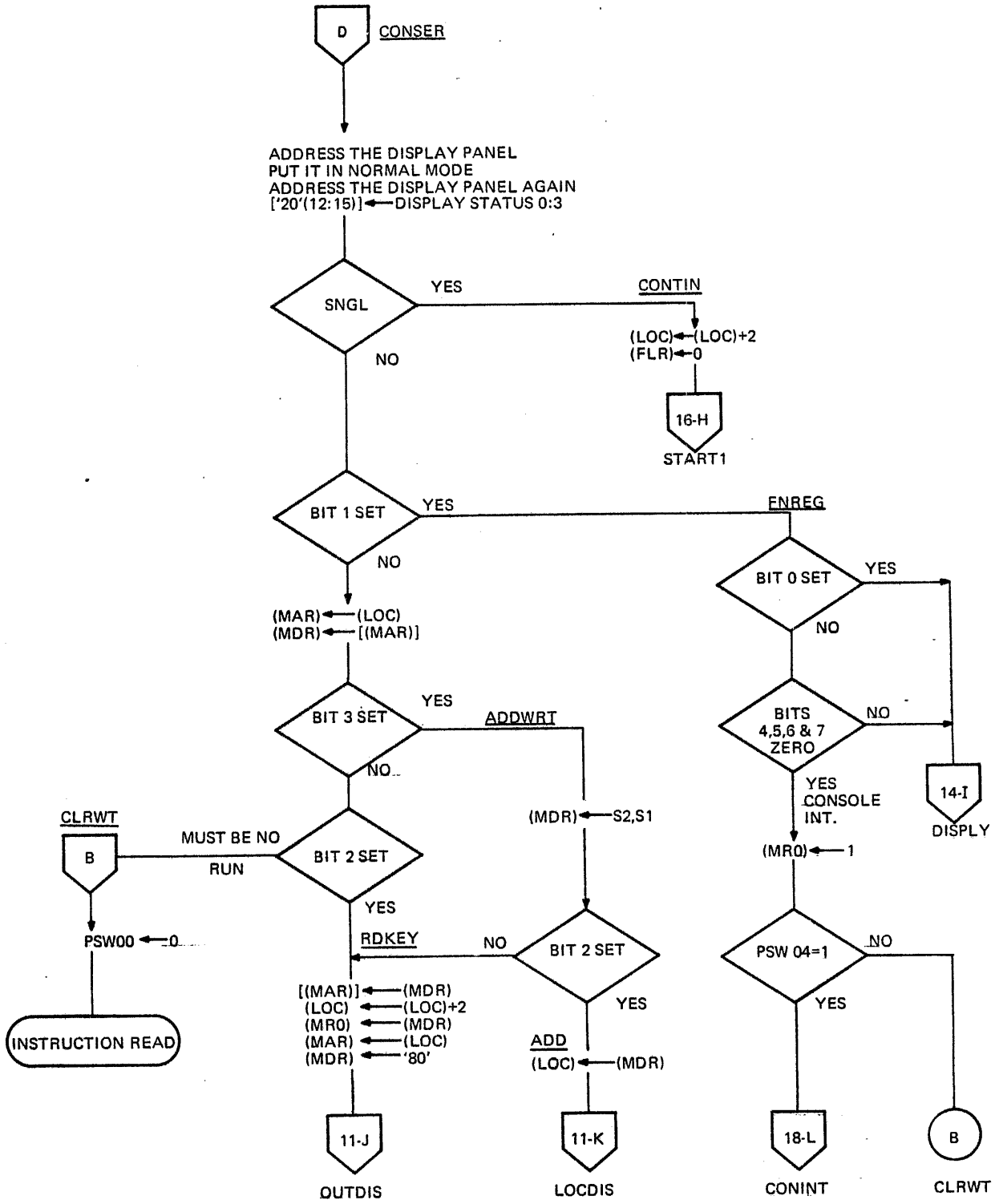


Figure 6. Routine CONSER

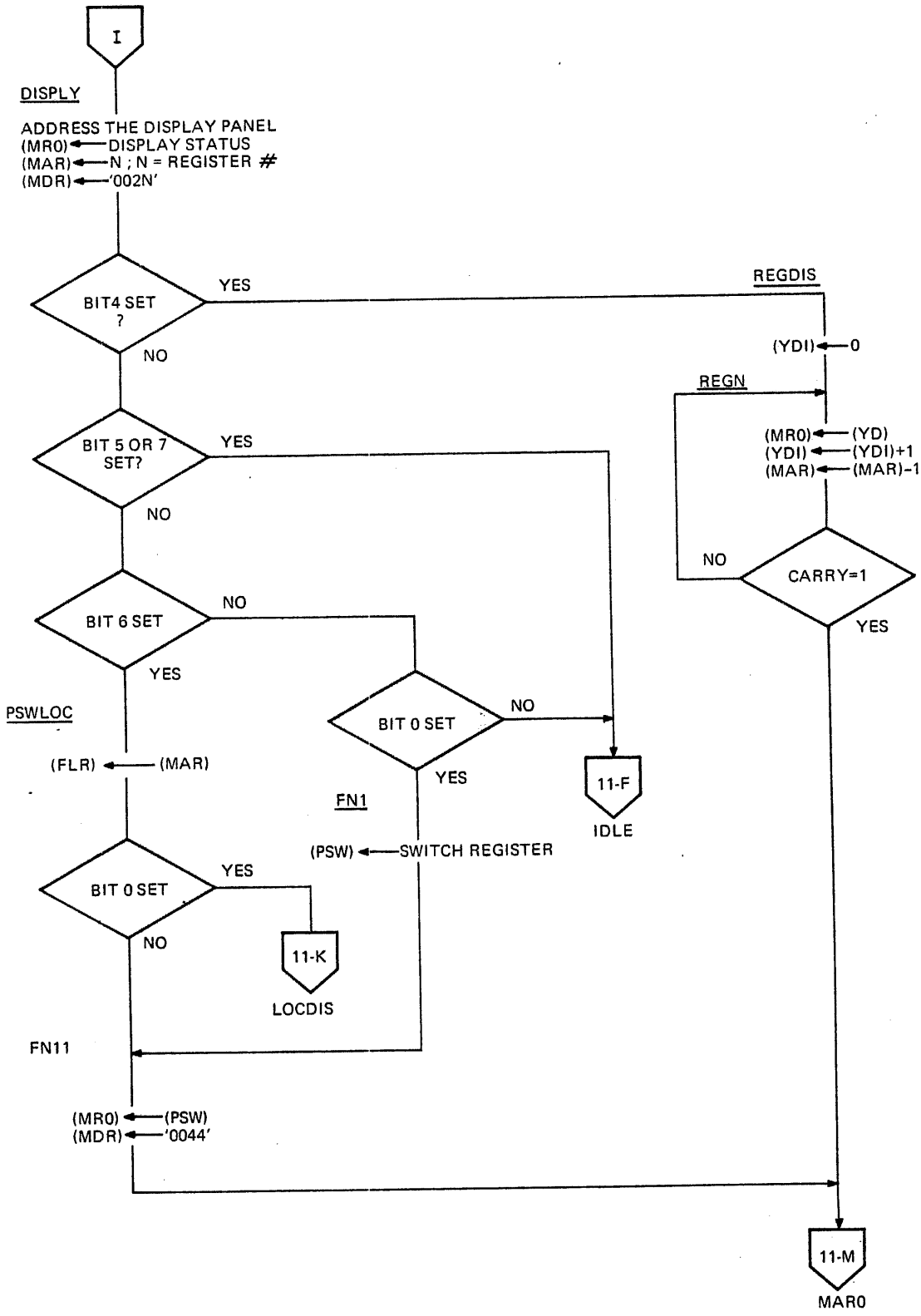


Figure 7. Display Routine

In the DISPLY routine, the Display Controller is addressed and its status is sensed. Then the register number n is obtained in MAR and MDR is set equal to X'2n'. If a General Register is selected, routine REGDIS is entered. If Function codes 4 or 5 are indicated, routine PSWLOC is entered. If Function code 1 is indicated, routine FN1 is entered. Otherwise, the uninterruptable IDLE loop is entered.

At REGDIS, the YD field is cleared and incremented until it equals the register number specified by MAR. The specified General Register is copied to MR0. Routine MAR0 is then entered.

At PSWLOC, status Bit-0 is examined to differentiate between Functions 4 and 5. If status Bit-0 is set, the Function 5 is indicated and routine LOCDIS is entered. Otherwise, the PSW is copied to MR0, and MDR is set equal to X'44', and the MAR0 routine is entered.

At FN1, the switch register data is copied into PSW and a branch is taken to FN11.

Routine LOCDIS copies LOC to MR0, sets MDR equal to X'45' and clears MAR. Routine OUTDIS is then entered.

Routine OUTDIS outputs the five bytes contained in MDR8:15, MAR and MR0 to the Display Controller. Then the uninterruptable IDLE loop is entered.

The IDLE loop is a high speed loop that can only be exited if a power failure occurs or a CATN is detected.

Instruction Fetch

A user's Instruction Fetch begins when a micro-instruction specifying Instruction Read is performed. The hardware sets the ROM Address Register to '000', which corresponds to the label START on the flowchart, see Figure 8. If any interrupts are pending, the micro-program branches to routine HELP. If no interrupts are pending, the LOC is incremented by two. The hardware copies the instruction word from MDR into the Instruction Register (OP, YD, and YS). The General Register specified by YS is loaded into MR0 and Q and DROM1 is interrogated. If the most significant bit of DROM1 is false, a memory read is initiated from the address specified by the new contents of LOC, and LOC is incremented by two. If this bit is active (RR type user instructions), no memory read occurs.

Depending on the user's operation code, DROM1 supplies an appropriate address to resume micro-code execution. If the user's operation code is not legal, the DROM1 sets the ROM Address Register to 082 causing a branch to routine ILEG. There, the LOC is decremented by two, the MAR is set to 0030 and routine GENSWP is entered.

User Instructions Emulation

The ROM address supplied by DROM1, in a way, categorizes the user instructions into those that require operand set-up and those that do not. Table 3 shows the legal instruction mnemonics and the corresponding symbolic ROM address for DROM1. For those instructions that do not require any operand set-up, the micro-program goes directly to the appropriate execution routine via DROM1 and DROM2 is not used. For those instructions that do require pre-processing, DROM 2 is interrogated to get the starting address of the execution routine. Table 4 shows the legal instruction mnemonics and the corresponding symbolic ROM addresses for DROM2.

Interrupt Support

During user Instruction Fetch, the micro-program tests for interrupts. If any of the tested interrupts (MALF, ATN, CATN, SNGL) are active, routine HELP is entered, and LOC is decremented by two. See Figure 9.

Machine Malfunction

If MALF is active, routine MMALF is entered. MALF can be caused by Memory Parity Error or Early Power Fail if PSW Bit-2 is set; or by Primary Power Fail. At routine MMALF, if the Primary Power Fail signal is active, Routine PWRDWN is entered. There, the PSW and LOC are stored in their core memory save locations and the user's General Registers are saved in the area of core whose starting address is contained in location X'0022'. The command Power down (POW) micro-instruction is then performed which stops the processor and deactivates the initialize (SCLR) relay.

If Primary Power Fail was not causing MALF, the micro-program checks for CATN. This test allows microprogram to exit from a continuous repetition of machine malfunction PSW swap because of repetitive memory parity error. If CATN test fails, the micro-program does a Machine Malfunction PSW swap with location X'0038'. Routine GENSWP, the common PSW swap routine, is discussed later.

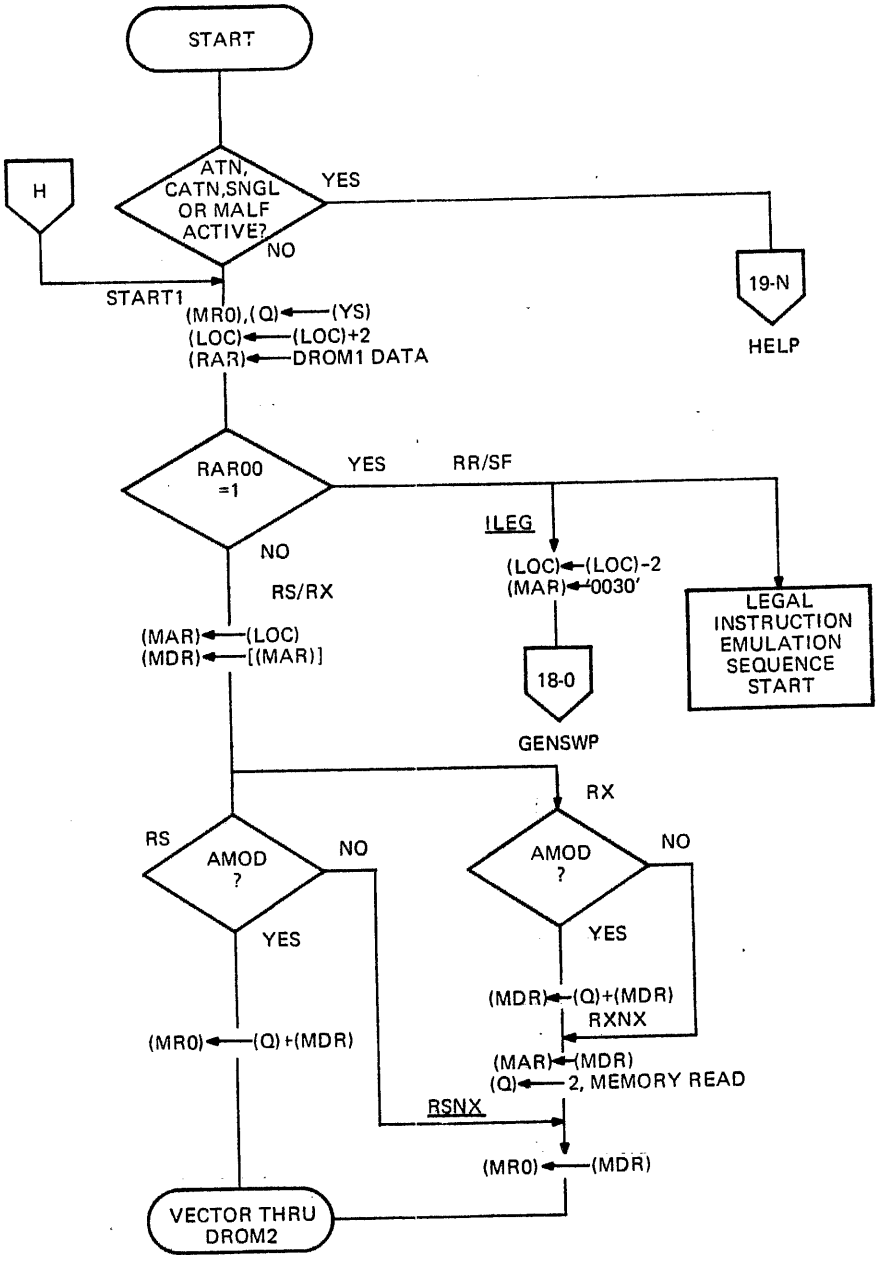


Figure 8. Instruction Fetch

TABLE 3. DROM–1 DATA

	00		20		40		60		80		A0	C0		E0	
0		ILEG	BTBS	BTS	STH	RS		ILEG		ILEG		BXH	BX		ILEG
1	BALR	BALR	BTFS		BAL		AHM	RX				BXLE	BX	SVC	RS
2	BTCR	BTCR	BFBS	BFS	BTC			ILEG				LPSW	RX	SINT	RS
3	BFCR	BFCR	BFFS		BFC							THI	RS		ILEG
4	NHR	NHR	LIS	IMM	NH	RX						NHI			
5	CLHR	CLHR	LCS	LCS	CLH							CLHI			
6	OHR	OHR	AIS	IMM	OH							OHI			
7	XHR	XHR	SIS		XH							XHI			
8	LHR	LHR		ILEG	LH							LHI			
9	CHR	CHR			CH							CHI			
A	AHR	AHR			AH							AHI		RRL	SLL
B	SHR	SHR			SH							SHI		RLL	
C	MHR	MHR*			MH	RX*						SRHL	SLHL	SRL	
D	DHR	DHR*			DH	RX*						SLHL		SLL	
E	ACHR	ACHR			ACH	RX						SRHA	SLHA	SRA	SLA
F	SCHR	SCH			SCH	RX						SLHA		SLA	
0		ILEG		ILEG		ILEG			SRLS	SLLS		STM	LMSTM		ILEG
1									SLLS			LM			
2									STBR	STBR		STB	RX		
3									LBR	LBR		LB			
4									EXBR	EXBR		CLB			
5									EPSR	EPSR		AL	AL		
6									WBR	RBRWBR		WB	RBWB		
7									RBR			RB			
8									WHR	IORR		WH	IORX		
9									RHR			RH			
A									WDR			WD			
B									RDR			RD			
C									MHUR	MHUR*		MHU	RX*		
D									SSR	IORR		SS	IORX		
E									OCR			OC			
F									AIR	AIR		AI	AI		

* FOR M/D OPTION ONLY, OTHERWISE IT IS ILEG

TABLE 4. DROM–2 DATA

	00		20		40		60		80		A0	C0		E0	
0		0	BTBS	BKWORD	STH	STH		0		0	0	BXH	BXH		0
1	BALR		BTFS	FRWORD	BAL	BALR	AHM	AHM				BXLE	BXLE	SVC	SVCD2
2	BTCR		BFBS	BKWORD	BTC	BTCR		0				LPSW	LPSW	SINT	SINT
3	BFCR		BFFS	FRWORD	BFC	BFCR						THI	THI		0
4	NHR		LIS	LHR	NH	NHR						NHI	NHR		
5	CLHR		LGS	0	CLH	CLHR						CLHI	CLHR		
6	OHR		AIS	AHR	OH	OHR						OHI	OHR		
7	XHR		SIS	SHR	XH	XHR						XHI	XHR		
8	LHR			0	LH	LHR						LHI	LHR		
9	CHR				CH	CHR						CHI	CHR		
A	AHR				AH	AHR						AHI	AHR	RRL	RRLD2
B	SHR				SH	SHR						SHI	SHR	RLL	RLLD2
C	MHR				MH	MHR*						SRHL	SRHLD2	SRL	SRLD2
D	DHR				DH	DHR*						SLHL	SLHLD2	SLL	SLLD2
E	ACHR				ACH	ACH						SRHA	SRHAD2	SRA	SRAD2
F	SCHR				SCH	SCH						SLHA	SLHAD2	SLA	SLAD2
0						0			SRLS	SRHLD2	0	STM	STM		0
1						0			SLLS	SLHLD2		LM	LM		
2						0			STBR	NOB		STB	STB		
3						0			LBR	0		LB	LB		
4						0			EXBR	NOB		CLB	CLB		
5						0			EPSR	0		AL	RBR		
6						0			WBR	WBR		WB	WBR		
7						0			RBR	RBR		RB	RBR		
8						0			WHR	WHR		WH	WHR		
9						0			RHR	RHR		RH	RH		
A						0			WDR	WDR		WD	WD		
B						0			RDR	RDR		RD	RD		
C						0			MHUR	0		MHU	MHUR*		
D						0			SSR	SSR		SS	SS		
E						0			OCR	OCR		OC	OC		
F						0			AIR	SSR		AI	SS		

* FOR M/D OPTION ONLY, OTHERWISE IT IS 0

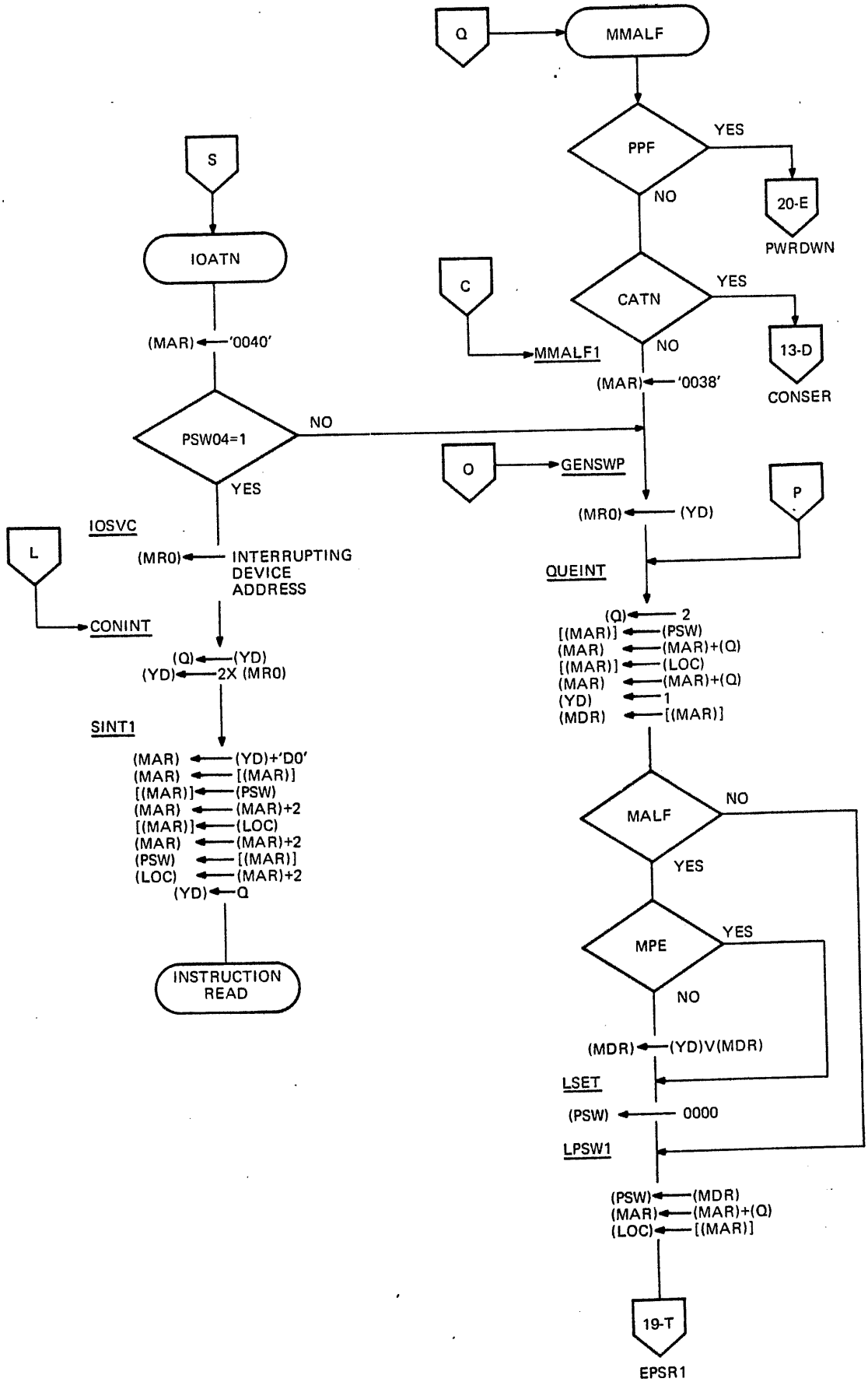


Figure 9A. Interrupt Support

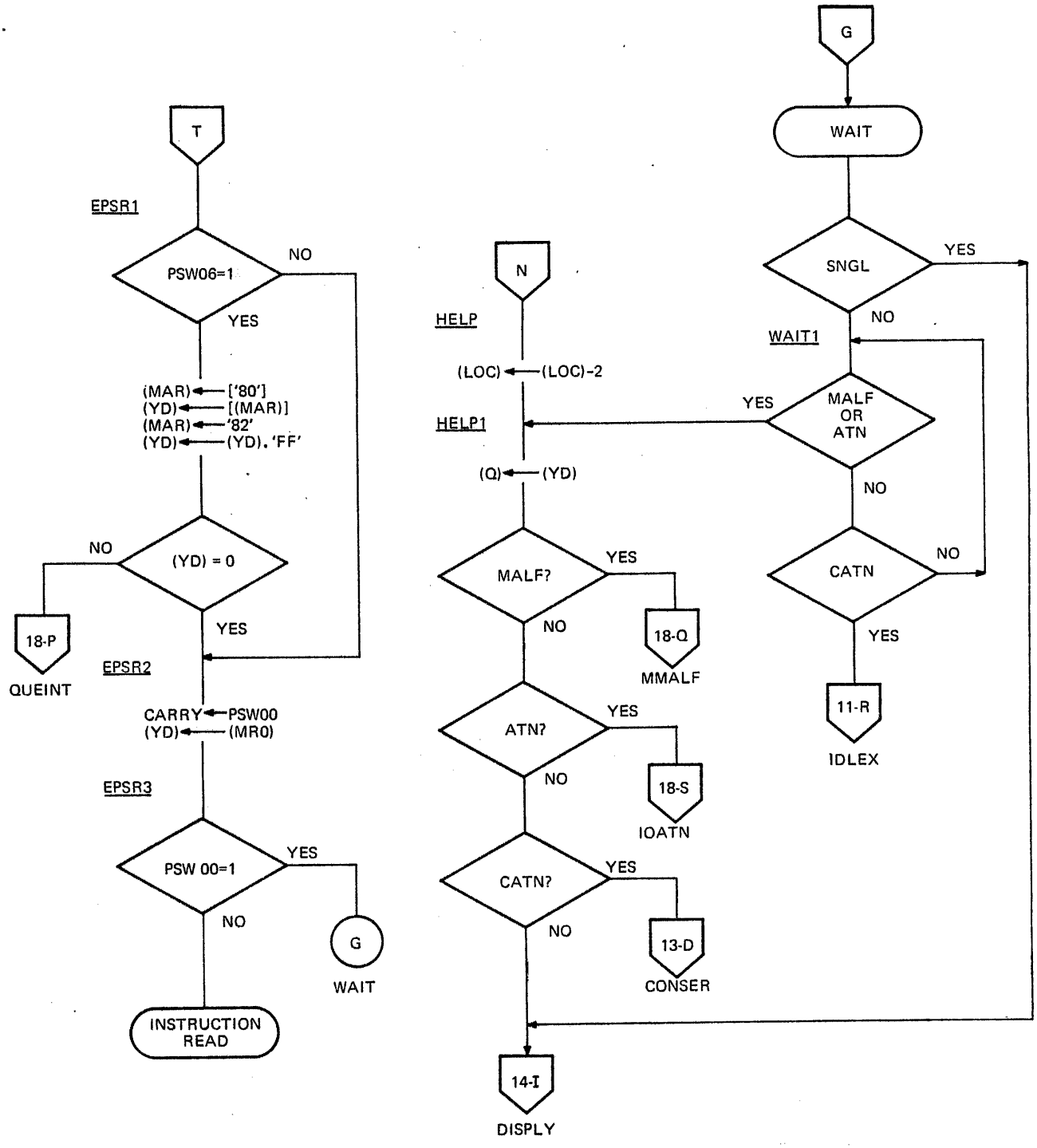


Figure 9A. (Continued) Interrupt Support

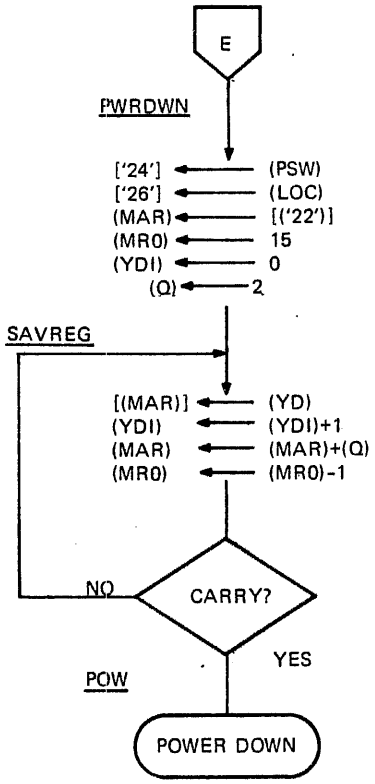


Figure 9B. Power Down Routine

I/O Attention

If MALF is not active, the micro-program tests for I/O attention (ATN). If ATN is active, the IOATN routine is entered. In IOATN routine, if DATN is active, IODMA routine is entered; otherwise, PSW bit 4 is tested. If PSW Bit-4 is set, routine IOSVC is entered; otherwise, a PSW swap is performed with location X'0040'.

In IODMA routine, device zero is addressed to knock down any addressed device. Then one halfword is read from the DMA on I/O Bus. This halfword is the start memory address for the requested data transfer. If memory address is odd, DMARD routine is entered, where halfwords are read from the DMA device and stored in consecutive memory halfwords. If memory address is even, DMAWRT routine is entered, where consecutive halfwords from the start memory address are written to the DMA device. A DMA device must be a halfword oriented device. The DMARD or the DMAWRT routine is exited when DATN is dropped. The next user instruction is then fetched.

Routine IOSVC acknowledges the I/O interrupt. The returned device number times two is used to index into the Service Pointer table beginning at core location X'00D0'. The halfword contained in the selected location is fetched and placed in MAR. The micro-program then stores the PSW in the location whose address is (MAR) and the LOC in the location whose address is (MAR)+2. The contents of the location whose address is (MAR)+4 is fetched and placed in the PSW, LOC is set equal to (MAR)+6, and the user instruction now pointed to is fetched and executed.

Console Attention

If neither MALF nor ATN is active, the micro-program tests for Console Attention (CATN). If not active, the interrupt must have been SNGL, and routine DISPLY is entered. There, the selected register or registers are output to the Display Console and the Idle loop is entered.

If CATN is active, routine CONSER is entered. There, the Display Console is addressed, which resets the CATN indication. If SNGL is also active, the micro-program continues the user instruction emulation. When the next user instruction fetch begins, CATN is inactive and SNGL is active, causing routine DISPLY to be entered.

Routine GENSWP

Routine GENSWP is the common PSW swap routine, entered with MAR containing the address of the swap area. The PSW is stored in the location whose address is (MAR). LOC is stored in the location whose address is (MAR)+2. The PSW is loaded with the contents of the location addressed by (MAR)+4. The L flag in the new PSW is set to 1 if the PSW swap is due to an Early Power Fail. LOC is then loaded from location (MAR)+6.

If Bit-6 of the new PSW is set, the micro-program examines Bits-8:15 of the halfword whose address is in location X'0080'. If this byte is non-Zero, another PSW swap is performed with location X'0082'. If Bit-6 of the new PSW is not set, the micro-program tests PSW Bit-0. If not set, user instruction execution begins with the instruction specified by LOC. If Bit-0 is set, the interruptable WAIT loop is entered. The WAIT loop tests for MALF, ATN, or CATN. If any interrupt occurs, routine HELP is re-entered.

Interrupt System

The interrupt structure provides rapid response to external and internal events that require special software attention. The descriptions that follow are oriented towards the emulator.

Internal Interrupts

Five different internal interrupts may be generated. Of these, the Illegal Instructions, Fixed-Point Divide Fault, Queue Service, and Supervisor Call Interrupts are created by the Emulator, and the Machine Malfunction Interrupt is generated in the hardware.

Illegal Instruction Interrupt

The illegal instruction interrupt occurs when an instruction not in the user's repertoire is fetched. Table 5 shows the Model 6/16 user's instruction repertoire. All 256 combinations of Op Codes are available in the DROM. For illegal Op-Codes, the data in DROM1 equals '082', starting address of Illegal Instruction interrupt micro-routine. In case of illegal op-codes, when DROM1 is interrogated, a branch to ILEG routine occurs where an Illegal Instruction PSW swap, location X 30 , is performed.

TABLE 5. USER'S INSTRUCTION REPERTOIRE

OP CODE	OP-CODE BITS 0:3							
BITS 4:7	0	2	4	6	9	C	D	E
0		BTBS	STH		SRLS	BXH	STM	
1	BALR	BTFS	BAL	AHM	SLIS	BXLE	LM	SVC
2	BTCR	BFBS	BTC		STBR	LPSW	STB	SINT
3	BFCR	BFFS	BFC		LBR	THI	LB	
4	NHR	LIS	NH		EXBR	NHI	CLB	
5	CLHR	LCS	CLH		EPSR	CLHI	AL	
6	OHR	AIS	OH		WBR	OHI	WB	
7	XHR	SIS	XH		RBR	XHI	RB	
8	LHR		LH		WHR	LHI	WH	
9	CHR		CH		RHR	CHI	RH	
A	AHR		AH		WDR	AHI	WD	RRL
B	SHR		SH		RDR	SHI	RD	RLL
C	MHR*		MH*		MHUR*	SRHL	MHU*	SRL
D	DHR*		DH*		SSR	SLHL	SS	SLL
E	ACHR		ACH		OCR	SRHA	OC	SRA
F	SCHR		SCH		AIR	SLHA	AI	SLA

*Available only with Multiply/Divide option.

Machine Malfunction Interrupt

The Machine Malfunction Interrupt occurs on a memory parity error or early power fail if PSW Bit-2 is set. The emulator also performs a Machine Malfunction PSW swap on Power-Up if PSW Bit-2 is set, Auto-Restart is present, and the Run mode is specified.

If the Memory Parity option is present, the parity bit of each halfword in main memory is set or reset to maintain odd parity. The parity bit is generated on every Memory Write and checked on every Memory Read or Instruction Read. If a Memory Parity Error (MPE) occurs, and PSW Bit-2 is set, the testable signal MALF goes active. During the user instruction fetch part of the micro-program, MALF, along with other interrupts, is tested. If any interrupt is pending, the micro-program branches to a routine to sort interrupts by priority.

The Early Power Fail condition (EPF) exists if the optional power fail detector determines that the line voltage is low. The condition also occurs when the Initialize key is depressed or when the Power switch is turned OFF. One millisecond after Early Power Fail, the testable Primary Power Fail signal (PPF) goes active. The testable signal MALF is active if EPF is active and PSW Bit-2 is set or if PPF is active. When the micro-program loads Zero into PSW, the MPE and EPF Flags are reset.

External Interrupts

If individually enabled by the user's program, a peripheral device controller is allowed to request Processor service when the device itself is ready to transfer data. If PSW Bit-1 is reset, I/O device interrupt signals are ignored but queued, the signal (ATN) remains pending. However, when PSW Bit-1 is set the interrupt is acknowledged.

The processor may service an I/O interrupt in one of two ways, depending on the state of PSW Bit-4. Refer to Figure 9.

FUNCTIONAL DIAGRAM ANALYSIS

Introduction

This section relates to Functional Schematic 01-094D08, Sheets 1 through 19. The last character of the mnemonic symbol on INTERDATA Functional Schematics designates the logic level at the time the signal is active. For example; D050 is data line number 5 (D05). The last character (0) indicates that when D05 is active, the line is at a logic level of ZERO. Refer to the General Description section of the *Model 6/16 Maintenance Manual,* Publication Number 29-470 for further information concerning the INTERDATA documentation system.

CLOCK CONTROL

The Clock Generator is shown on Sheet 12. The Clock System employs a free running 20MHz oscillator. The oscillator is adjusted by variable resistor R26. (For the semi conductor version of the machine the oscillator is adjusted for 1.66 MHZ to compensate for a memory cycle time which is not divisable by 250ns.)

Signal OSC0 is used as the clock input to three flip-flops arranged as a feedback delay counter. The delay counter generates three overlapping clocks, CLK1, DCLK1, and DDCLK1. All Processor Clocks are derived from CLK1, DCLK1, and DDCLK1. The counter is initialized and held in the initialized state by SCLR0A, on a Power-Down or Power-Up to inhibit clocks. A delayed system clear ACLR0 is generated for the processor to assure that the processor receives clocks in the proper sequence (refer to Figure 10 for clock timing).

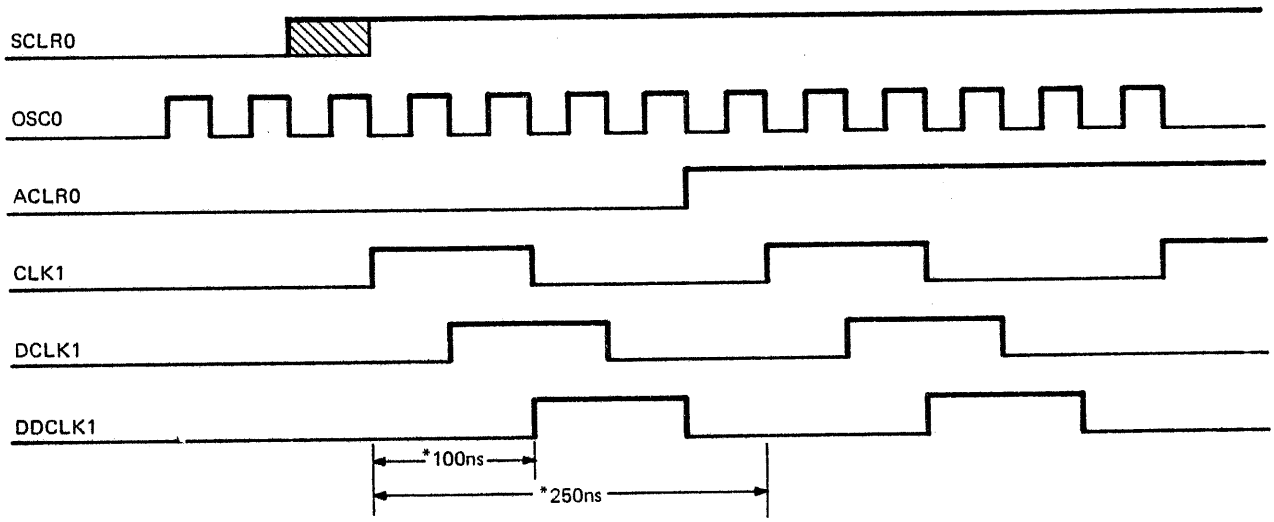


Figure 10. Clock Timing Nominal

The Clock Control Logic is also shown on Sheet 12. Two basic Processor Clocks are derived from CLK1. The first, the CPU clock (CPUCLK0), is the clock for the LSI micro-processor chips. It is disabled for I/O operations, and memory operations whenever MSTP0 is active.

The second Processor Clock generated is the ROM Data Clock (CKRDO, CKRD1). This clock is disabled by I/O operations (IOSTPO), memory operations (MSTPO), and RDSTPO which is a signal from the Repeat Counter which disables the ROM Data Clock for a fixed count n ($n < 31$), allowing a specific micro-instruction to be repeated n times. Refer to Figure 11 for a description of a clock cycle. The ROM Data Clock also serves as a destination clock. Clocks CLK1, DCLK1, and DDCLK1 are used to synchronize memory and I/O operations.

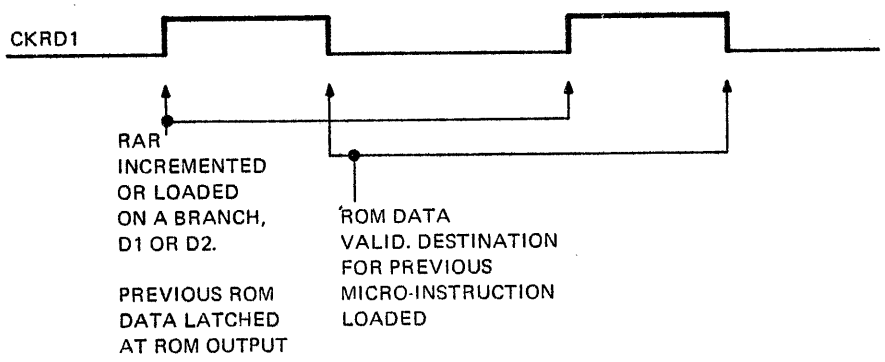


Figure 11. Specific Clock Functions

INITIALIZE CONTROL

System Initialize is performed by de-energizing the System Clear (SCLR) relay (19G7). This relay is de-energized as a result of the following:

1. Placing the processor in an OFF condition.
2. Operating the processor INIT (Initialize) switch.
3. Activating PFDTO by an external source.
4. Activating PFDTO from the optional Primary Power Fail detector if the input falls below the minimum operating level.
5. Loss of either +5VDC or (+12 OR 15VDC) from the processor power supply.

The SCLR function provides an orderly shut down of the processor as well as a reset signal to both the memory and the Multiplexor Bus. On a power up, the SCLR relay remains de-activated until all DC Voltages are within regulation. This assures predictable initial states of latched functions.

An early Power Fail indication is provided to the user program if Bit-2 of the Program Status Word (PSW) is set. This indication is provided by the micro-program by means of a machine malfunction interrupt swap.

Upon receipt of a Power-Down indication by the hardware, PFDTO (19F1) active, the one millisecond timer (19J4) is triggered. The leading edge of this pulse sets the Early-Power Fail flip-flop (19L5) which in turn enables, if PSW Bit-2 is set, a branch on Machine Malfunction to be taken by the micro-program. The micro-program tests to determine which condition caused the Machine Malfunction (MMALF) interrupt. If the Early Power Fail flip-flop (FEPF) is set, the micro-program signals the user program by means of a Machine Malfunction PSW swap. On the trailing edge of the pulse from the one millisecond timer, the Primary Power Fail flip-flop (19J6) is set, initiating a Power-Down sequence.

The optional Primary Power Fail detector monitors the AC input by sampling the secondaries of a 12 VAC transformer, C1 and C3 from the processor power supply. If the AC is lost or if the AC falls below a predetermined level PFDTO (19F1) and POWDNO (19D1) become active. Signal PFDTO initiates the Power-Down sequence and POWDN0 provides a fast discharge path for capacitors C-46 and C-47 which de-energizes the SCLR relay and holds the relay OFF in the event that the AC voltage is fluctuating about its preset Power-Down level.

NOTE

With a semi-conductor memory system the Primary Power Fail detector is built into the Power Supply.

READ ONLY MEMORY (ROM)

The Read Only Memory (ROM) is a high speed, solid state, non-destructive memory which holds the micro-program. The ROM is organized into a single page of 512 words and each word is 24 bits in length. An additional page of ROM can be added to support optional features. Each page of ROM contains 3 Integrated Circuit (IC) packages arranged such that each IC holds 8 bits of each word on the associated page. An additional ROM chip (512 x 8) comprises the Decoder ROM (DROM).

Each ROM IC contains two enable leads (CE1 and CE2), and a strobe lead (see Sheet 6). To enable the ROM chip CE1 must be Low and CE2 must be High. The strobe (CKRD0) is used to latch the data at the output of the ROM. The ROM contains internal latches which are used to hold the ROM Data (RD), refer to Figure 12 for ROM timing. The RD register is internal to the ROM ICs.

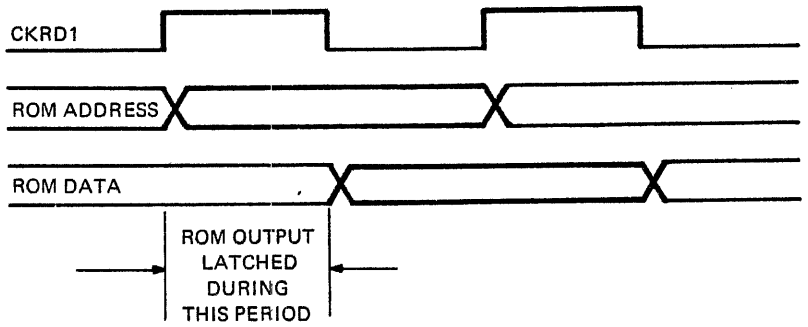


Figure 12. ROM Timing

Decoder ROM (DROM)

The Decoder ROM (DROM) is a single ROM Integrated circuit, refer to Sheet 5. It contains 512 eight bit words. The DROM is addressed by the most significant eight bits of the Instruction Register (OP Code Field). Each of the 256 possible combinations of this decoded function may address two locations in the DROM, depending on the state of D10 (5D1), a decoded function of RD0, RD1, and RD2. When D10 is low, one of the first 256 words of the DROM is selected, corresponding to a micro-code D1. Illegal instructions are decoded in the DROM.

ROM Address Register (RAR)

The ROM Address Register (RAR), sheets 5 and 6, is a 10 bit register which is loaded on the positive edge of CKRD1 from the DROM during a decode micro-operation or the ROM Data bits during a branch micro-operation. The eight least significant bits of this register are arranged as a counter to allow sequential ROM addresses in a given half page to be selected. The RAR is initialized on Power Up to address X'100' and the micro-program begins execution at this location. Address Clear (ACLR0) is used to hold the ROM Address at X'100' allowing the ROM to latch the RD information accessed from ROM Address X'100', refer to Figure 10 for ACLR0 timing.

PROCESSOR REGISTERS

The majority of the instructions contained in the micro-program are concerned with relocating data from one processor register to another. Most of the processor registers are general purpose registers, however, some do perform special functions. Each register is described in the following sections.

Location Counter, Memory Address Register, and Memory Address Buffer (Refer to Sheet 17).

The Location Counter is an up-counter which automatically increments by 2 on each Instruction Read or D1 (non-RR or SF referenced) micro-instruction. The Location Counter can also be loaded directly from the S Bus. Anytime the Location Counter is loaded from the S Bus, the Memory Address Register (MAR) is also loaded with the same data.

The Memory Address Register (MAR) is a two to one (2:1) multiplexer, with storage latches. The clock following an increment of the Location Counter causes the contents of the Location Counter to be copied into the Memory Address Register.

The Memory Address Buffer (MAB) is a two-to-one (2:1) multiplexer, the inputs of which are the Location Counter and the Memory Address Register. During an Instruction Read, the contents of the Location Counter is gated onto the Memory Address Bus. During all other memory operations the contents of the Memory Address Register are present on the Memory Address Bus. The Memory Address Buffer outputs are disabled (high impedance state) whenever the processor is not selected such as during DMA operations. The Memory Address Buffer is also disabled by EXMBSY0 (19) if a memory adapter card (35-608) is used.

The Location Counter is a 15-Bit register and the Memory Address Register is a 16-Bit register.

Memory Data Register (MDR)

The Memory Data Register (MDR) is shown on Sheet 16. The MDR is a two-to-one (2:1) multiplexer with storage latches and is 16 bits wide. The inputs to the multiplexer originate from the S Bus and the Memory Data Receive Bus. The storage latches are edge triggered which are loaded by signals LDMDRH and LDMDRL. When the MDR is to be loaded from the S Bus the LDMDRH and LDMDRL signals are a combination of the MDR being selected and CKRD. When a Memory Read Operation is specified the LDMDRH and LDMDRL signals are generated by a combination of FRD and the removal of the Data Unavailable (DUA) signal by the memory.

The MDR is divided into a High and Low half. The High half is loaded by the LDMDRH signal and the Low half is loaded by the LDMDRL signal. If Cross Shift is specified by the micro-code, only MDR High is loaded when Bit-15 of the MAR is set and only MDR Low is loaded when Bit-15 is reset.

The outputs of the MDR are presented to memory during the Write portion of a memory cycle.

Instruction Register (IR)

The Instruction Register (IR) is a 16-Bit register which stores the user instruction currently being executed. The IR is divided into three parts or fields; OP code field (Bits-0-7), YD field (Bits-8-11), and YS field (Bits-12-15). The IR is loaded directly from the Memory Data Receive Bus (MRR) during an Instruction Read Memory operation.

The OP code field (sheet 5), contains the encoded instruction to be performed. The OP code field outputs are presented as address to the Decoder Read Only Memory. Ninety-Six of the possible 256 combinations are defined as legal instructions (when Multiply, Divide option is included) and have unique entry points in the micro-program. The remaining 160 combinations are directed by Direct the Read-Only-Memory (DROM) to the illegal instruction entry point in the micro-program.

The YD field is defined as the User Destination field. The YD field selects one of the 16 general registers, located in the LSI micro-controller chips (sheet 4), in which the result of the user instruction is to be stored. This portion of the IR (sheet 11) is arranged as an up/down-counter. If YDP1 is specified in a micro-instruction the YD field of the IR is incremented by one at the end of the instruction. In the same manner, if YDM1 is specified, the YD field of the IR is decremented by one at the end of the instruction. The YD field is also set to ZERO when Clear YD is specified by the micro-program.

The YS field is the User Source field of the instruction being emulated. The second operand of the instruction is contained in the general register specified by YS for RR format instruction. This field also contains the number of the general register being used as the index register on an RX or RS instruction or data in SR instruction.

Flag Register (FLR) and Condition Code (CC)

The Flag Register (FLR) (sheet 13), is a four bit register which contains the Carry Flag (C), the Overflow Flag (V), the Greater Than Flag (G), and the Less Than Flag (L). The Flag Register outputs are copied into another four bit register, the Condition Code (Sheet 10), at the end of each user instruction being emulated. These flags represent results of instructions which are not otherwise indicated.

The FLR is loaded from the S Bus whenever either the FLR or Program Status Word (PSW) register is specified as a destination. The contents are copied into the Condition Code (CC) on an Instruction Read or after a Load PSW micro-instruction. The outputs from the FLR are also used by the Branch Circuit (sheet 14) for conditional branches. The contents of the CC are copied onto the B Bus (Bits-12-15) when the PSW is specified as the source register.

The FLR (the Carry Flag, Overflow Flag, and Greater/Less Than Flags) are also modifier as follows:

The Carry Flag (C) is affected by any Arithmetic, Boolean, Shift, or Load micro-instruction if Carry Out (CO) is specified. The Carry Flag sets on a Shift if the bit shifted from the appropriate port on the LSI micro-controller (sheet 4) is set, if Carry (Carry 1) from the LSI micro-controller (sheet 4) is set on an Add, or if Carry 1 is inactive on a Subtract. In all other cases the Carry Flag is reset.

The Overflow Flag (V) is directly set if false SYNC is detected on an I/O operation and is changed on any Add or Subtract micro-instruction if Flag (F1) is specified. Overflow (OVL1) is a direct output of the most significant slice of the Central Processing Unit (CPU) (sheet 4) and is valid only on an Add or Subtract micro-instruction.

The Greater Than (G) and Less Than (L) Flags change on any Load, Arithmetic, or Boolean micro-instruction providing Flag (F1) is specified. The G Flag is set if the result of the operation is positive or if the result is Zero and either the G or L Flag were set from a previous operation. The L Flag is set if the resulting sign is negative. Either flag is reset if these conditions are not met.

Shift Control

The LSI micro-controller components making up the processor (Sheet 4) have the capability of shifting 16 or 32-Bits of data right or left under micro-program control. The ports on these chips associated with this capability are SLOSRI (Shift Left Out, Shift Right In), and SROSLI (Shift Right Out, Shift Left In) for shifting the general purpose register left or right. Signals QLOQRI (Q Register Left Out, Q Register Right In) and QROQLI (Q Register Right Out, Q Register Left In) are associated with a 16-Bit internal extension register for double precision shifting capability. The controls for this are shown on sheet 13. For single and double precision shifts, Carry Out (CO) is specified to load the C flag. Carry In (CI) is used as a control to determine whether data is rotated or shifted by the control logic.

Table 6 shows the states of the shift ports of the processor.

TABLE 6. PROCESSOR SHIFT PORT STATUS.

FUNCTION	SLISRO1	QLOQRI1	SLOSRI1	QLIQRO1
Shift Left	0	Z	Z	0
Shift Right	Z	0	0	Z
Double Precision Shift Left	Z	Z	Z	0 or Z*
Double Precision Shift Right	Z	Z	0 or Z*	Z

Z = Open collector output state, equal to bits being shifted out of these ports.

* 0 or Z depends on the state of Carry In (CI).
CI = 1 for a rotate, and the port state is Z.
CI = 0 for a shift, and the port state is 0.

CPU, Data Multiplexer, and Cross Shift

The CPU (sheet 4) is comprised of four Large Scale Integration (LSI) chips forming a 16-Bit wide data path. Internal to these chips are an ALU (Arithmetic Logic Unit), a 16 x 16 general purpose register stack with dual port accessibility to the ALU, a 16-Bit extension register, and circuits to control shifts, both single and double precision.

Data is presented to the CPU through a Data Multiplexer (sheets 8 and 9). The Data Multiplexer, under ROM Control, selects one of 8 inputs (16-Bits wide), unless it is an Immediate function. An Immediate function disables the outputs of the Data Multiplexer (sheet 8), and passes the data from the Data Multiplexer through a second multiplexer network. The second multiplexer network either cross shifts the data or passes it through depending on the state of MAR 15 and whether or not Cross Shift is specified by the microcode.

On Immediate micro-instructions, the output of the Cross Shift Multiplexer is disabled (High Z state) and the output of the Immediate Multiplexer is enabled. The outputs of these Multiplexers are OR-tied and present data to the Data Inputs of the CPU chips.

The Data Outputs of the CPU chips form the S Bus.

I/O CONTROL

An I/O operation is initiated if I/O is the Source or Destination of a micro-instruction. The I/O control logic is shown on Sheet 15. If I/O is a source, then an Input operation is initiated or if I/O is a destination, an output operation is indicated. I/O Timing is discussed separately for input and output.

Input

Refer to Figure 13 for Timing information. When I/O is specified as a source, unload I/O (UIOO) (15G6) and IOSTOP0 goes active. On the trailing edge of the next clock (CLK1) The Control In flip-flop (15G8) sets. On receipt of SYN0 from the selected I/O device or the detection of False SYNC, the 14 millisecond Timer (15N7) timed out, the SYNC flip-flop (15L8) sets which deactivates IOSTOP0. On The Trailing edge of the next CLK1 the destination register is loaded and both the Control In flip-flop and the SYNC Flip-Flop resets completing the operation.

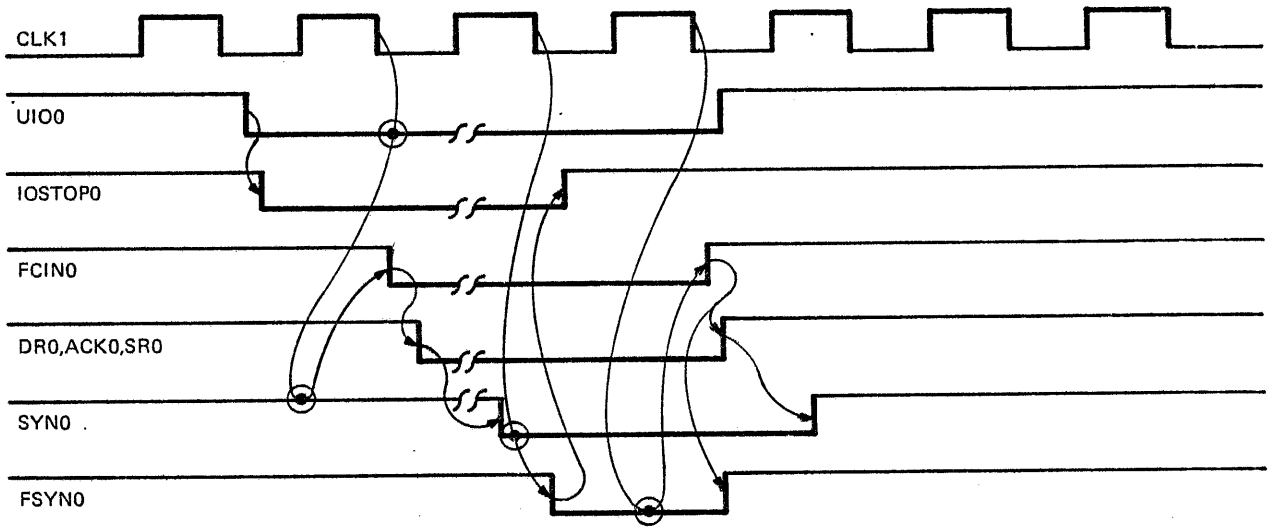


Figure 13. I/O Input

Output

Refer to Figure 14 for Output Timing information. An I/O out operation is very similar to the input operation. When Load I/O LDI00 (15J6) is detected, IOSTOPO goes active and on the leading edge of the next CLK1 the Data flip-flop (15K8) sets. The output of the Data flip-flop is used to gate data To The Data Bus, D000:160. On the trailing edge of the next DDCLK1 the Control Out flip-flop (15H8) is set which activates the specified output control line. The output operation now progresses in the same manner as the I/O Input operation discussed previously.

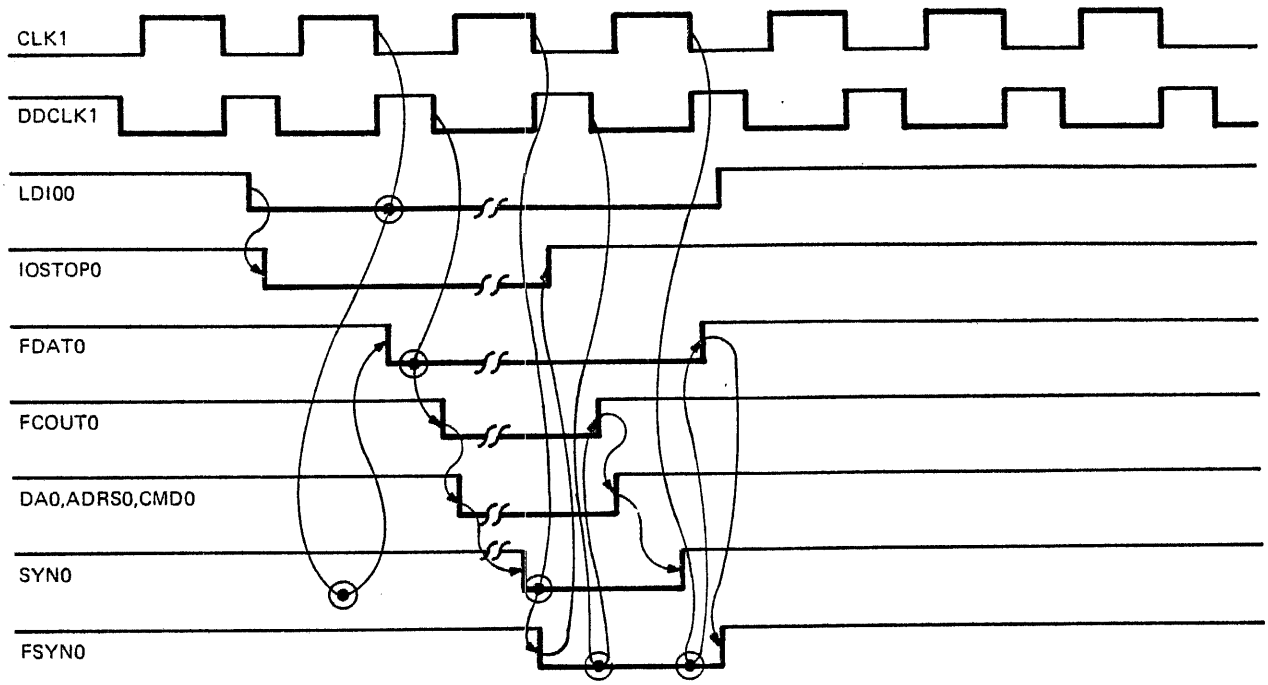
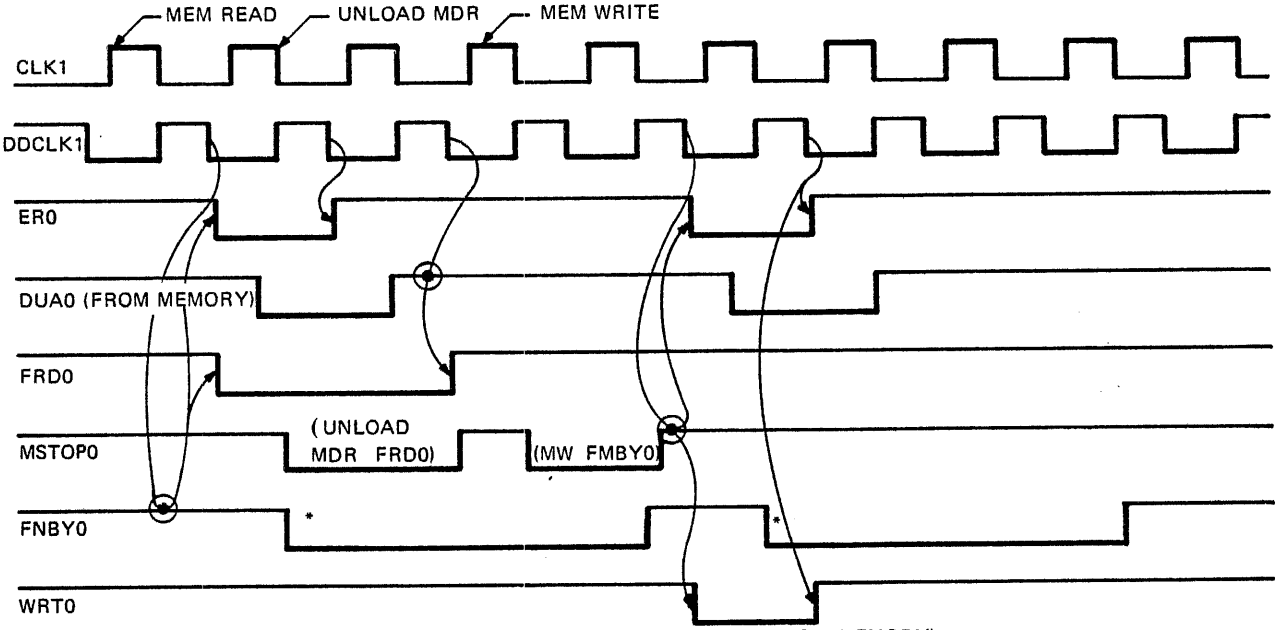


Figure 14. I/O Output

Memory Timing and Control

A memory operation can be initiated by the micro-program by specifying a Memory Read, Memory Write or an Instruction Read. An Instruction Read and a Memory Read Operation is identical except that an Instruction Read causes both the MDR and the Instruction Register to be loaded from the Memory Bus. In addition, a memory cycle can be commenced by a DMA Request, REQO (18F1) active. (The semi-conductor memory uses a DMA request in order to insure that the Processor does not attempt a memory operation during the time that an internal memory refresh operation is taking place.)

Figure 15 depicts the memory timing and control functions for Processor initiated cycles. MEMI (18F1) indicates a memory operation is requested by the Processor. If the memory is not busy, FMBY0 (18G1) inactive and a DMA request is not latched, FREQO (28F8) inactive, a processor memory operation is initiated, the Early Read flip-flop (18C5) is set on the trailing edge of Double Delayed Clock (DDCLKO). On this same edge, either the Write flip-flop (18D6) or the Read flip-flop (18J6) is set to differentiate between a memory read or a memory write operation. On the trailing edge of the next CLK1 the four bit counter (18M6) is loaded with a value, which is dependent on the memory cycle time of the memory being used. (Refer to the strap option Table on Sheet 18 of the Function Schematics for strapping information for specific memory cycle times.) The output of the FMBY1 counter is used for clock stops and memory timing control. The counter is incremented by one on each CLK1 until the count goes from X'F' to X'O'. This deactivates FMBY1.



* FMBY0 = 3 CLOCKS (1.0 us CYCLE), 2 CLOCKS (0.75 us CYCLE), OR 1 CLOCK (SEMI MEMORY)

Figure 15. Processor Memory Timing (1.0 usec)

DMA memory timing, Figure 16, is similar to Processor Timing except that the sequence is started by a DMA request, REQO active. This signal is synchronized to the Processor clocks by the request flip-flop (18F6). Once this request is latched the DMA device requesting memory gets the next avilable memory cycle. Prior to generating ERO to the memory the Processor generates an Enable command (ENO) (18H8) to the DMA Bus. This signal is used by DMA devices to resolve contention during the active period of this line and on its trailing edge the DMA with the highest priority which is requesting memory becomes selected.

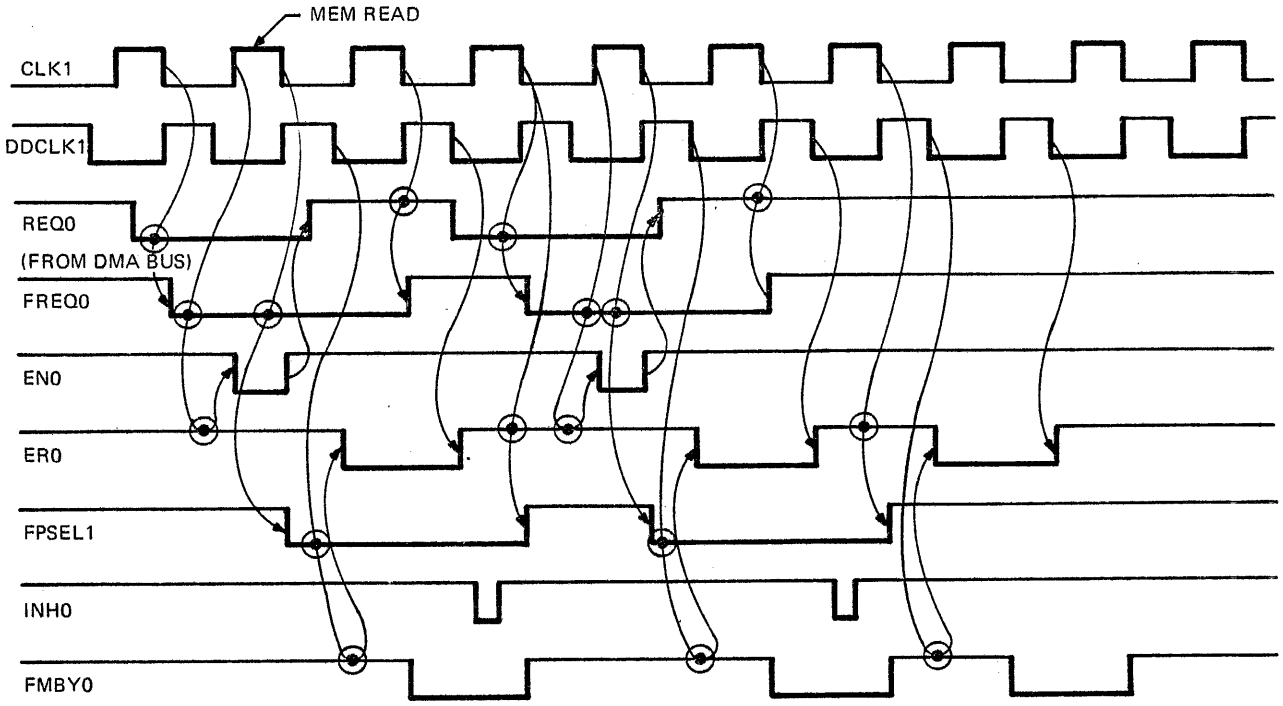


Figure 16. DMA Memory Timing

On the trailing edge of ENO the Processor Select flip-flop (18G6) becomes reset which causes the Memory Address and Memory Data Busses to be forced to a high impedence state by the Processor allowing the selected DMA device to present its address and data to the memory. The first half of the CLK1 following ERO generates INHO (18J6). INHO may be used by the DMA device to indicate that data is available and that the address and data information is latched in the memory. INHO, therefore, should be used to deselect the DMA device.

Figure 16 shows two DMA transfers to a semi-conductor memory at the maximum transfer rate. During the first DMA memory cycle a Processor memory request is queued. Since the Processor has a lower priority than any DMA device, its memory request is not honored until both DMA requests are honored.

Display System

The Display System provides, if the Hexadecimal Display Panel is present, a means for reading the contents of all the system registers and any core memory location, together with the capability of manually entering data and programs. Figure 17 shows the Hexadecimal Display Panel layout. Within the Hexadecimal Display Panel are five eight-bit byte Display Registers, D1 through D5, that hold data output from the Processor, and a 20-bit Switch Register which stores data input from the Hexadecimal Keyboard.

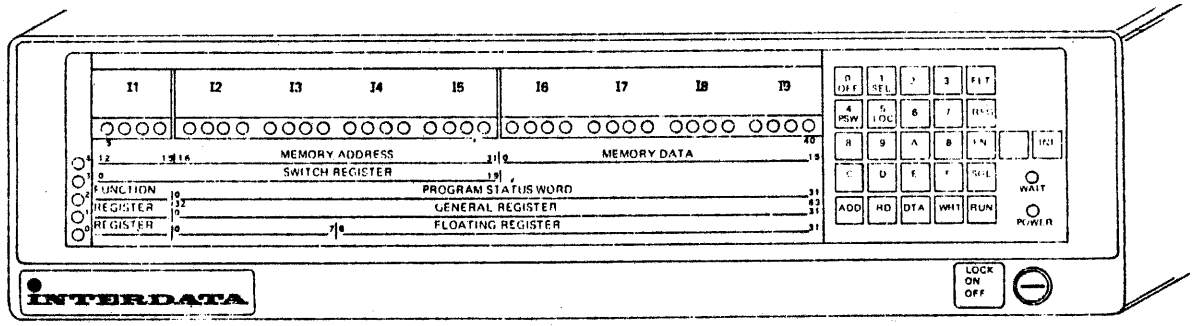


Figure 17. Hexadecimal Display Panel

Associated with each Display Register D1 through D4 are eight indicator lamps that provide a binary readout and two optional hexadecimal read-out indicators. Associated with Display Register 5 are four indicator lamps for binary display and one optional hexadecimal read-out indicator.

The most significant four bits of Display Register D5 (Bits 0:3) control four of the five indicator lamps along the left edge of the Hexadecimal Display Panel. The fifth indicator lamp is controlled by logic internal to the Hexadecimal Display Panel. To the right of each of these five lamps is a diagram that defines what is being displayed. In general, only one of the diagram lamps is on at a time. If none of the diagram lamps are on, a user program has written data to the display registers.

The most significant 20-bits of the display show the contents of Display Registers D3 and D4 and the least significant four bits of Display Register D5 (Bits 4:7) or the contents of the 20-bit Switch Register. When the Switch Register is being displayed, the lamp next to the Switch Register diagram is turned ON. Any other diagram lamp that may have been ON, remains ON. When the Switch Register is no longer displayed, its diagram lamp goes out and the most significant 20-bits of the display again shows the contents of Display Registers D3 and D4 and the least significant four bits of Display Register D4 (Bits 4:7) (refer to Table 7)

TABLE 7. DISPLAY STATUS AND COMMAND ENCODING

STATUS

	0	1	2	3	4	5	6	7
Run	X	0	0	0	X	X	X	X
Memory Write	X	0	0	1	X	X	X	X
Memory Read	X	0	1	0	X	X	X	X
Address	X	0	1	1	X	X	X	X
Fixed Register	X	1	0	0	X	X	X	X
Floating Register	X	1	0	0	X	X	X	X
Function	X	1	0	0	X	X	X	X

General Register	0	0	1	0	X	1	0	0	0
	1	1	1	0	X	1	0	0	0
	2	0	1	0	X	1	0	0	1
	3	1	1	0	X	1	0	0	1
	4	0	1	0	X	1	0	1	0
	5	1	1	0	X	1	0	1	0
	6	0	1	0	X	1	0	1	1
	7	1	1	0	X	1	0	1	1
	8	0	1	0	X	1	1	0	0
	9	1	1	0	X	1	1	0	0
	A	0	1	0	X	1	1	0	1
	B	1	1	0	X	1	1	0	1
	C	0	1	0	X	1	1	1	0
	D	1	1	0	X	1	1	1	0
	E	0	1	0	X	1	1	1	1
General Register	F	1	1	0	X	1	1	1	1

Floating Register 0, 2, 4, 6, 8, A, C, Floating Register E

Function	0	0	1	0	0	0	0	0	0
	1	1	1	0	0	0	0	0	0
	2	0	1	0	0	0	0	0	1
	3	1	1	0	0	0	0	0	1
	4	0	1	0	0	0	0	1	0
	5	1	1	0	0	0	0	1	0
	6	0	1	0	0	0	0	1	1
	7	1	1	0	0	0	0	1	1
	8	0	1	0	0	0	1	0	0
	9	1	1	0	0	0	1	0	0
	A	0	1	0	0	0	1	0	1
	B	1	1	0	0	0	1	0	1
	C	0	1	0	0	0	1	1	0
	D	1	1	0	0	0	1	1	0
	E	0	1	0	0	0	1	1	1
Function	F	1	1	0	0	0	1	1	1

Console Interrupt
PSW Select

PSW
LOC

COMMAND

Normal	1	0	0	0	0	0	0	0
Incremental	0	1	0	0	0	0	0	0

The Key Operated Security Lock is a three-position, OFF-ON-LOCK, key operated locking switch, which controls the primary power to the system. This switch can also disable the Hexadecimal Display Panel, thereby preventing any accidental manual input to the system. The power indicator lamp (PWR) associated with the key lock is located in the lower right corner of the Hexadecimal Display Panel. The PWR positions, primary power, the Control keys, and the Hexadecimal keys are (see Figure 18):

OFF	The primary power is OFF.
ON	The primary power is ON and the Control keys and Hexadecimal keys are enabled.
LOCK	The primary power is ON and the Control keys and Hexadecimal keys are disabled.

The Hexadecimal Display Panel operating procedures may be found in the appropriate User's Manual.

The Display Controller, 35-601, or the Display Controller with ALO, 35-602, must be used to support the Binary or Hexadecimal Display Console or the Turnkey Console. Refer to Display Contoller Functional Schematic 02-405D08 during the following desciption.

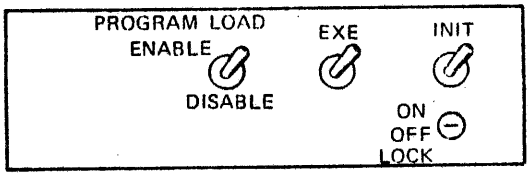


Figure 18. Turnkey Console

Data Transfer

When the display is in the Normal mode, all data outputs are directed into Display Register D1. Conditioning the controller to the incremental mode, via an Output command, causes the two bit counter (2M9) to be incremented at the trailing edge of DAG1. The output of this counter is decoded to activate LA0, in response to the first DAG1 and then LB0 for all subsequent DAG1's until the counter is initialized. In this mode, the first DA loads Display Register D1, the next DA loads Display Register D2. The next two DAs load Display Registers D3 and D4. This counter is initialized by SCLRO, by an Output command placing the controller in the incremental mode, or whenever the display is addressed and the Normal mode is selected.

Input data from the Switch Register to the Hexadecimal Display Panel is handled in a similar manner as output data. In the Normal mode or on the first Data Request (DR), if in the Incremental mode, Switch Register Bits 12:19 are read. The second DR, in the incremental mode, reads Switch Register Bits 4:11. The two bit counter (2M7) directs the DR to the appropriate group of Switch Registers. This counter is initialized by the same function as the four bit counter discussed previously and is incremented at the trailing edge of DRG1.

NOTE

Bits 0:3 of the Switch Register are gated out as part of the status byte when address is read.

Control Logic

When the display requires micro-program support, it generates two outputs, ESNO0 and ESNC0, which are latched in the RS flip-flop at 2K2. The output of this flip-flop sets the Console Attention flip-flop (CATN) at 2L2. This flip-flop is reset by GADR0 when the Processor addresses the display or by SCLRO.

When the SGL function switch is depressed, SSGL1 becomes active (2G4) and ESNCO AND ESNO0 are generated which cause the Single flip-flop (2L3) to become set. This flip-flop remains set until another execute is generated and the SGL function is not selected.

Status Input

The status byte encoding is shown in Table 8. The status byte is gated onto the SD00:07 lines by the SRG0 lead. SRG0 gates the SD00:07 lines onto Bits 08:15 of the D Bus.

TURNKEY CONSOLE

This panel provides a means of controlling the system power, initializing the system, and generating a Console Attention (FCATN) to start program execution, if the Primary Power Fail/Auto Restart option is not installed.

This option conditions the Processor to the Run mode by grounding SSGL1, SD011, SD021, and SD031 at the Control Console connector. The Display Controller, when addressed by the micro-program in the power up sequence, indicates the Run mode. With the Auto-Restart option present, program execution commences at the address specified in the Location Counter (LOC), when the system is turned on and without the Auto-Restart option the micro-program performs a normal power sequence and then goes to the un-interruptable idle Loop until the Execution (EXE) switch is operated.

BASIC SWITCH PANEL

The Basic Switch Panel provides a means of controlling system power if an optional Display Controller is not equipped. The switch on this option is a single throw double pole switch. One set of contacts is used to jumper C1 and C2, which turns on the power supply or supplies in the system, while the other set of contacts grounds PFDTO (19) going to the Processor to provide an early power fail indication which enables the controlled power down sequence.

Automatic Load Option (ALO)

Refer to Functional Schematics, 02-405 D08, Sheet 3 during this discussion. This option is present on 35-602, Display Controller with ALO, or 35-603, ALO.

The Automatic Load Option is used to store program information in non-destructive Read-Only-Memory (ROM) integrated circuits. A maximum of eight-4K-Bit ROM chips may be installed on a single option board. This provides a storage capability of up to 4K-bytes of information. The ALO is a halfword device which transfers data 16-Bits at a time. Eight-bits of data come from one 512x8-bit ROM while the other 8-bits come from another 512x8-bit ROM. Due to this, ROM chips must be used in pairs (i.e. ROMOA and ROMOB, ROM1A and ROM1B, etc.)

The ALO is enabled, ALEN1 (3F3), by SCLRO. Upon power up the micro-program tests the Halfword Control Line (HWO) (354), if active ALEN1 high and S1 in the Enable position, the micro-program loads the data contained in the ROM devices on the ALO. The data format is shown in Table 8.

TABLE 8. ALO DATA FORMAT

WORD	0	PSW
WORD	1	LOC
WORD	2	START ADDRESS
WORD	3	END ADDRESS
WORD	4	DATA
WORD	.	.
WORD	.	.
WORD	N	DATA

The eleven-bit counter (3D5-3H5) is initialized to X'000' by SCLRO and is incremented following each Data Request on the trailing edge of FDATO (3B5). The micro-program continues to read the ROM data until all data between the start and end addresses is loaded into memory.

The ALO is disabled, ALEN1 inactive, on the leading edge of the first Address Control Line (ADRS0), independently of the device address.

MAINTENANCE

This section describes maintenance procedures which may be used to check and, if necessary, adjust the Processor.

There is only one adjustment associated with the Processor. Check Basic Clock (BCLK0) found on connector 104-3, the Test Aid connector, for a clock period of 250, 300 nanoseconds for the semi-conductor memory version of the Processor. This adjustment is very stable and need only be made if a check indicates that it is out of tolerance. Adjust variable resistor, R26, to bring it into tolerance.

Use the 06-106 Processor Test to perform a comprehensive test of the 6/16 Processor.

MNEMONICS

The following list provides a brief description of each mnemonic found in the Model 6/16 Processor. The source of each signal on Schematic Drawing 01-094DO8, is also provided.

MNEMONIC	DESCRIPTION	LOCATION
ACK0	Acknowledge Control Line to MPX Bus	15D9
ACLR0	Delayed System Clear	12N3
ADD	Add	7J7
ADRS0	Address Control line to MPX Bus	15F9
AMOD1	YS Equals Zero	11H9
ATN0	Attention Request Line	14L2
B0	YD, YS Address Control	7L7
B000-B150	Data From B Bus	Sheet 8
BCLK0	Buffered Processor Clock	12N4
BRSEL0	Branch Select	14E9
CARRY1	Carry from CPU	4A5
CATN0	Console Attention Request Line	14M2
CBRSEL0	Clocked Branch Select	5K8
CI1	Carry In Enable	1356
CKRD1	ROM Data Clock	12N8
CLK0	Processor Clock	12N5
CLO70	Control Line 7 from MPX Bus	19G5
CLR0	Clear RAR	5N8
CLRFLR0	Clear Flag Register	11D9
CLRYD0	Clear YD Address Register	11C4
CMD0	Command Control Line To MPX Bus	15D9
DA0	Data Available Control Line to MPX Bus	15E9
DB000-DB151	Outputs of Data Buffer	15B1, C1, D1, E1, F1, G1, H1, J1, K1, L1, M1, N1
DBF0	Decoded Branch on False Condition	7D7
DBRCH0	Decoded Branch	7E7
DCLK0	Delayed Processor Clock	12N1
DDCCK0	Clock Delayed from DCLK0	12N1
DI000-DI151	Data in Bus to CPU	4F9, 4G9, 4H9,4J9, 4K9, 4L9
DIR0	Decode Instruction Read	7D7
DMR0	Decoded Memory Read	7D7
DMW0	Decoded Memory Write	7D7
DO001-DO151	Bus Outputs of the CPU Elements	4F3, 4G3, 4J3, 4K3, 4L3
DR0	Data Request Control Line to MPX Bus	15C9

MNEMONIC	DESCRIPTION	LOCATION
DR081	DROM Output Bit 8	SE9
DR081-DR151	DROM DATA	5E3, SE5, 5E6
D10	DROM Decode 1	7D7
D20	DROM Decode 2	7D7
EN0	Enable From Memory Bus	1848
ER0	Memory Read or Write Enable	18C8
EXBSY0	External Busy to Processor From Memory	18S2
EXDUA0	Data Unavailable From Memory	18H1
EXSTP0	External Clock Stop	12B7
FDAT0	Data Flip-Flop to MPX Bus	15K9
FINR0	Instruction Read Flip-Flop	11E1
FEPF0	Early Power Fail Flip-Flop	19L9
FLDREG0	Load External Register Flip-Flop	19C6
FLPT0	Floating Point Control	11B5
FLR121-FLR151	Flag Register Outputs	13G9, J9, L9, N9
FLRSEL0	Destination Select for Flag Register	7F7
FMBY1	Memory Busy Flip-Flop	18K8
FPAR1	Parity Error Flip-Flop	19M9
FPPF1	Power Fail Flip-Flop	19K9
FPSEL1	Processor Select Flip-Flop	18G8
FRD1	Read Flip-Flop	16A1
FREQ0	Request Flip-Flop	18F8
FTIT0	Clock Stop Test Point	12B7
FWAIT	Wait Flip-Flop	11C9
F1	Set Flags Enable	13Rg
HW0	Halfword Control Line from MPX Bus	14B1
INH0	Inhibit From Memory Bus	18J8
I01	Decoded I/O Operation	15J9
IODMA0	I/O DMA Request Line	14G2
IOSTP0	Clock Stop for I/O	15G9
IO001-IO151	I/O Inputs From MPX Bus	15B1, C1, D1, E1, F1, G1, H1, J1, K1, L1, M1, N1, R1
JAMCC0	Jam Condition Code	7C8
JCICO0	Jam Carry In and Carry Out	11B5

MNEMONIC	DESCRIPTION	LOCATION
LDCC0	Load Condition Code	11A1
LDCT0	Load Repeat Counter	7G7
LDDEST0	Decoded Load Function (Load Destination)	13C4
LDIO0	Load I/O	7F7
LDREG	Load External Registers	19B9
LMDRH1	Load High Order Byte of MDR	11D9
LMDRL1	Load Low Order Byte of MDR	11D9
LOC001-LOC151	Location Counter Outputs	17B8, E8, H8, L8
LOCSEL0	Destination Selector for LOC	7G7
MA000-MA150	Memory Address Bus	17C9, D9, F9, G9, J9, K9, M9, N9
MAR001-MAR151	MAR Outputs	17D6, 17G6, 17K6, 17N6
MARSEL0	Destination Select for MAR	7F7
MRR001-MRR151	Memory Register Receive Bus	16D1, 16E1, 16G1, 16K1
MSK1	Mask on Condition Code	ION1
MSTP0	Clock Stop For Memory	12J9
OVL0	Overflow	4A5
PERR0	Parity Fail Detected	19M2
PFDT0	Power Fail Detector	19F2
POW0	Power Down Command	11B5
POWDN0	Power Down Signal	19D2
PSW001-PSE151	PSW Outputs	10A6, B6, G6, S5
PSWSEL0	Destination Select for PSW	7G8
QLIQRO1	Shift Q Left In, Shift Q Right Out	4A7
QLOQRI1	Shift Q Left Out, Shift Q Right In	4A7
RAR061-RAR151	ROM ADDRESS Registers	5K1, 5N4, 5N6, 6C6
RD001-RD231	ROM Data Bus	8L3, 8L4, 8L5, 8L6, 8L7, 8L8
RDSP0	ROM Data Clock Stop	11N9
REQ0	DMA Request for Memory Cycle	18F2
SCLR	System Clear	19H9
SINGL0	Single Step Request Line	
SH1	Decoded Shift	13A9
SLISRO1	Shift Left In, Shift Right Out	4A7
SLOSRI1	Shift Left Out, Shift Right In	4A7
SR0	Status Request Control Line to MPX Bus	15B9
SUB0	Subtract	7J7

MNEMONIC	DESCRIPTION	LOCATION
SUPINC0	Suppress Location Counter Increment	7A7
SV0	Set Overflow on False SYNC	15N9
SYN0	SYNC to MPX Bus	15M9
UIO0	Unload I/O	7N7
UMDR0	Unload MDR	7R7
WT0	Write Signal to Memory	18D8
XIMM1	Immdiate Control Line	9A1
YD01-YD31	Outputs of the User Destination Register	11K9
YDI0	YD Immediate	7R7
YDMI0	Decrement YD	11D4
YDPI0	Increment YD	11D4
YS01-YS31	Outputs of the User Source Register	11F9
ZERO1	Zero Result on S Bus	4A5

M71-094
MULTIPLY/DIVIDE CARD
INFORMATION SPECIFICATION

INTRODUCTION

The Multiply/Divide card is a half-board which resides in the Model 6/16 Processor chassis. The Multiply/Divide card provides the means for executing Multiply or Divide instructions under micro-program control. The processor provides operands to the Multiply/Divide card which in turn processes the operands and returns an answer to the processor.

INSTALLATION

Refer to the appropriate processor installation specification for applicable installation information.

BLOCK DIAGRAM ANALYSIS

Refer to the block diagram of the Multiply/Divide option, Sheet 1 of the Multiply/Divide Functional Schematic 02-403D08.

Inputs to and outputs from the Multiply/Divide card are over the standard I/O Multiplexor Bus and are under micro-program control. Special signals to the card from the processor are: MDO, which selects the card for receiving data over the I/O Bus; LDREG0, which is data from the processor to the option card; EXSTP0, a signal from the card to the Processor to stop the clocks while the card is performing its operations.

CLOCK AND CONTROL

This portion of the card circuit controls the loading of registers from the I/O Bus, the unloading of registers to the I/O Bus, synchronizing the on-board clock stop, and controlling the data paths on the card.

B-REGISTER

The B-Register contains the positive operand for Multiply operations and the two's complement negative operand for Divide operations.

SRH and SRL

SRH and SRL is a 32-Bit register with Shift Left, Shift Right, and Load capability. For Multiply operations SRH is initialized to Zero and SRL contains the Multiplier. SRL is shifted left for Divide operations and shifted right for Multiply operations. SRH is either loaded and shifted left or just shifted left on Divide operations. The Divide Shift Network provides the load and shift function on Divide operations. The decision to just shift or to load and shift is made by the Control Section. SRH is either shifted right by direction of the Control Section on Multiply operations or the output of the adder is loaded. The Multiply Shift Network provides a pre-shift to the partial product contained in SRH so that the Multiply and Divide operations are completed in the same number of clocks (16).

At the completion of an operation, the results are stored in SRH and SRL. The 32-Bit result of a Multiply operation is stored in SRH and SRL or, in the case of a Divide, the quotient is stored in SRL and the remainder is stored in SRH.

FUNCTIONAL ANALYSIS

When reading this section, refer to Functional Schematic 02-403D08.

Loading SRH,SRL and B Registers

Data is placed on the common BD Bus (BD001-151) from the I/O Bus when the M/D0 signal from the processor is active. When the data to be transferred is valid on the I/O Bus, the LDREG0 control line from the processor is activated for one processor clock. Signals LDREG0 and BCLK0 provide a load clock for the B, SRL, and SRH registers according to a sequence determined by a counter at 4C2, 4D2, 4E2 and 4F2. The LDA0 signal (4H4) loads data from the BD Bus into the B-Register, and also clears SRH. The LDB0 signal load SRL from the DB Bus, and LDC0 loads SRH. If the LDC0 clock is not generated, the operation to be performed is assumed to be a Multiply and the Divide flip-flop (4H5) is not set.

CLOCK CONTROL

The removal of MD0 by the processor causes EXSTP0 to be activated stopping all processor clocks except the Basic Clock (BCLK0). On the BCLK, following the activation of EXSTP0, the local clock is started and 16 clock pulses are generated on the Multiply/Divide Option Board. At the end of the 16 clock period the Multiply or Divide operation is complete and EXSTP0 is deactivated. (This signal is synchronized to the Processor clocks by BCLKO.) For one processor clock period following the removal of EXSTP0, the contents of SRL is gated to the I/O Bus and, during the following processor clock period, the contents of SRH is gated to the I/O Bus.

MULTIPLY

Prior to the commencement of the Multiply operation, the B-Register has been loaded with the multiplicand, SRL has been loaded with the multiplier, and SRH is set to zero. All operands are positive in form. (If negative the micro-program two's complements the numbers prior to loading.) The control lines for SRL (SRLS01 and SRLS11) are set for shift right. The control line for SRH (SRH01 and SRHS11) will either be set for load SRH, if the least significant bit of SRL (SRL151) is a logical One, or will be set for a shift right, if SRL151 is a logical Zero. The Divide Shift Network is disabled and passes the sum of the addition between the content of the B-Register and shifted left partial product contained in the SRH directly to the BD Bus. SRL is shifted right 16 times so that all 16 bits of the multiplier are tested. At the end of this time, SRH contains the most significant 16 bits of the result and SRL contains the least significant 16 bits of the result.

DIVIDE

Prior to the start of the Divide operation SRH and SRL contain the dividend in positive form (if negative the two's complement of the dividend is loaded by the micro-program) and the divisor is loaded into the B-Register in two's complement form. The quotient bit is the carry formed by the addition of SRH and B. Whenever the carry is positive (logical one) the partial remainder at the outputs of the adder is gated into SRH shifted left. Signal SRL is also shifted left and the carry is shifted into the least significant bit of SRL (SRL151). If carry is a logical zero SRH and SRL are shifted left one position and the outputs of the adder are ignored. Carry is again shifted into SRL. SRL is shifted left 16 times at the end of which SRL contains the quotient and SRH contains the remainder of the division.

Figures 1 and 2 are timing diagrams representing the timing of the Multiply/Divide Option Board 35-605.

ADJUSTMENTS

The only adjustment on the M71-094 Multiply/Divide card is that of the on-board oscillator. The oscillator frequency is adjusted by means of potentiometer R2, which is adjusted for an 80 nanosecond period (12.5 megahertz) as measured at the test point on the outer edge of the Multiply/Divide Option card.

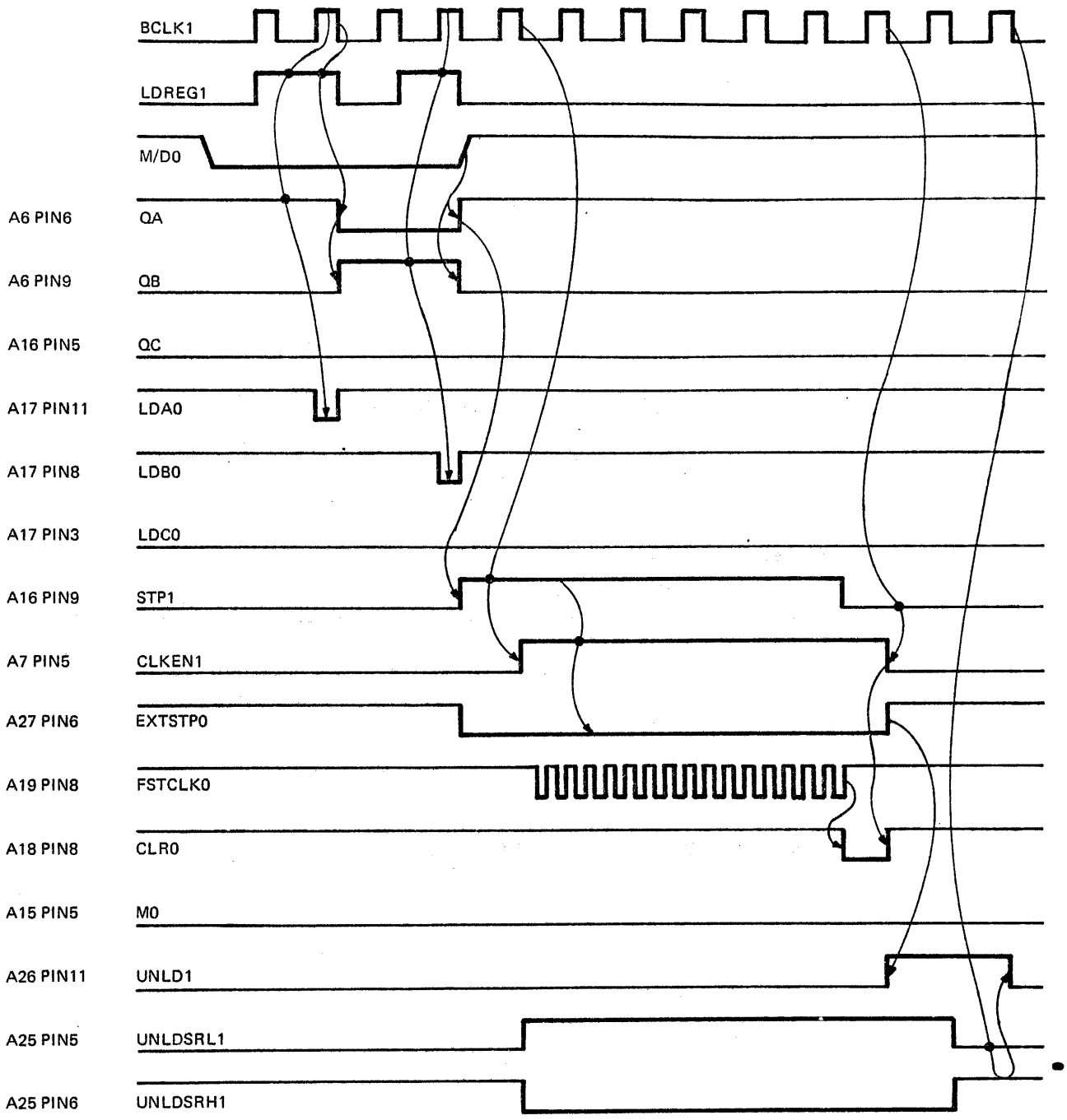


Figure 1. Multiply Timing

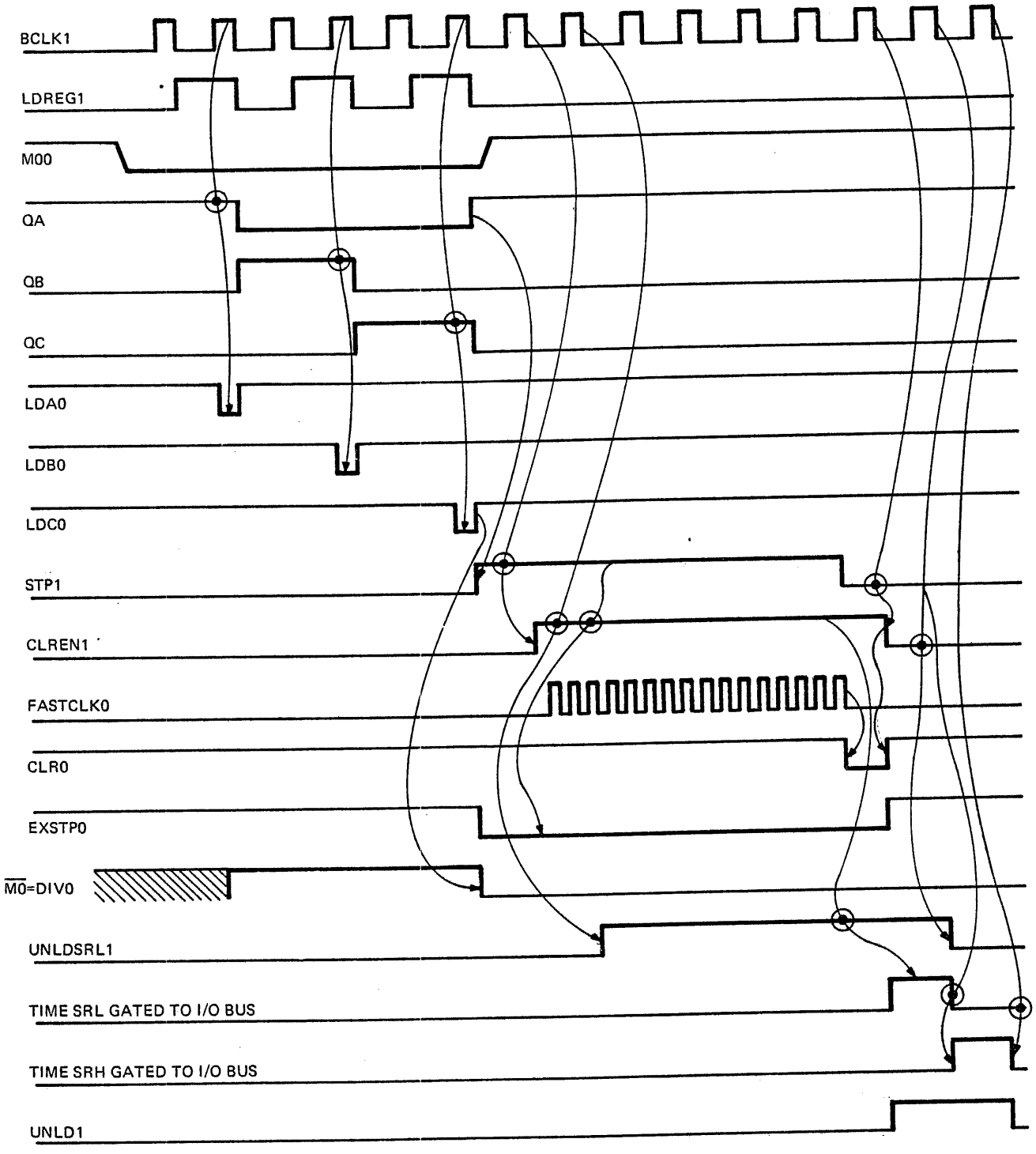


Figure 2. Divide Timing

MNEMONICS

The following list provides a brief description of each mnemonic found in the Multiply/Divide Option Board. The source of each signal on Functional Schematic 02-403D08, is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
B001:151	Outputs of B-Register	Sheet 3
BCLKO	Basic Clock From CPU	4A2
BD001:151	The Outputs of either the 2:1 MUX following the Adder or the Inverted D-Bus data	Sheets 2, 3
CARRY1	Carry out of the 16-Bit Adder	3B4
CLKEN0	Enables the Clock System of the M/D Board	4A5
CLR0	The OR of SCLR0 and MRESET0	4N8
D000:150	Processor's Bidirectional Data Bus	Sheet 2
DB00:150	Outputs of either SRH,OR SRL to the D-Bus	Sheet 2
DIVO	Divide output of the Multiply/Divide flip-flop	4H5
EXSTP0	External Stop to Processor Clock Stop Logic	4RZ
FSTCLK0	Fast Clock used to perform the Multiply or Divide Functions on the Option Board	4F5
LDA0	A Output of Load Sequencer loads the B-Reg and clears SRH	4H3
LDBO	B Output of Load Sequencer. Loads SRL	4H3
LDCO	C Output of Load Sequencer. Loads SRH	4H3
LDREG0	Load Register Signal from Processor. Indicates Data available.	4A2
MD0	Multiply/Divide select line from Processor	4A2
M0	Multiply output of Multiply/Divide flip-flop	4L4
MRESET0	Master Reset. Initialize function for M/D Option	4K8
SCLR0	System Clear from Processor	4K8
SRH001:151	Outputs of SRH	
SRHCLK0	Clock to SRH	4K3
SRHX1	Conditions SRH to either the Shift Right, Shift Left, or Load Mode.	4N4
SRI01	Shift Right into SRL	3L8
SRL001:151	Outputs of SRL	4K3
SRLX1	Conditions SRL to either the Shift Right, Shift Left or Load Mode.	4K4
STP1	Output of Stop flip-flop	4J2
UNLD1	Enables D-Bus drivers to unload results	4R6
UNLDSRL1	Selects the contents of either SRH or SRL to be gated onto the D-Bus.	4K6
Z001:Z151	Outputs of the 16-Bit Adder	Sheet 3

APPENDIX 1

EXAMPLE MULTIPLY/DIVIDE OPERATION

Appendix 1 shows an example of a multiply operation, Table A1-1, and a sample of a divide operation, Table A1-2.

TABLE A1-1. Sample Multiplication X'1111'*X'1111'=X'01234321'

B-Reg = 0001 0001 0001 0001

	SRH				SRL			
0	0000	0000	0000	0000	0001	0001	0001	0001
1	0000	1000	1000	1000	1000	1000	1000	1000
2	0000	0100	0100	0100	0100	0100	0100	0100
3	0000	0010	0010	0010	0010	0010	0010	0010
4	0000	0001	0001	0001	0001	0001	0001	0001
5	0000	1001	0001	0001	0000	1000	1000	1000
6	0000	0100	1000	1000	1000	0100	0100	0100
7	0000	0010	0100	0100	0100	0010	0010	0010
8	0000	0010	0010	0010	0010	0001	0001	0001
9	0000	1001	0001	1001	1001	0000	1000	1000
10	0000	0100	1000	1100	1100	1000	0100	0100
11	0000	0010	0100	0110	0110	0100	0010	0010
12	0000	0001	0010	0011	0011	0010	0001	0001
13	0000	1001	0001	1010	0001	1001	0000	1000
14	0000	0100	1000	1101	0000	1100	1000	0100
15	0000	0010	0100	0110	1000	0110	0100	0010
16	0000	0001	0010	0011	0100	0011	0010	0001

TABLE A1-2. Sample Divide X'3FFF7FFF'/X'7FFF' =X'7FFE'X'7FFF'

B = 1000 0000 0000 0001

	SRH				SRL				CARRY
0	0011	1111	1111	1111	0111	1111	1111	1111	0
1	0111	1111	1111	1110	1111	1111	1111	1110	1
2	0111	1111	1111	1110	1111	1111	1111	1101	1
3	0111	1111	1111	1110	1111	1111	1111	1011	1
4	0111	1111	1111	1110	1111	1111	1111	0111	1
5	0111	1111	1111	1110	1111	1111	1110	1111	1
6	0111	1111	1111	1110	1111	1111	1101	1111	1
7	0111	1111	1111	1110	1111	1111	1011	1111	1
8	0111	1111	1111	1110	1111	1111	0111	1111	1
9	0111	1111	1111	1110	1111	1110	1111	1111	1
10	0111	1111	1111	1110	1111	1101	1111	1111	1
11	0111	1111	1111	1110	1111	1011	1111	1111	1
12	0111	1111	1111	1110	1111	0111	1111	1111	1
13	0111	1111	1111	1110	1110	1111	1111	1111	1
14	0111	1111	1111	1110	1101	1111	1111	1111	1
15	0111	1111	1111	1110	1011	1111	1111	1111	1
16	0111	1111	1111	1110	0111	1111	1111	1111	X

M70-103
NS SELECTOR CHANNEL
INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-232 Selector Channel (SELCH) (Product Number M70-103) in a Model 70, 74, 80, 7/16 or 7/16 HSALU Processor System. The NS Selector Channel is complete on one 35-391M02 printed circuit board.

2. PHYSICAL CHARACTERISTICS

2.1 Dimensions 15 3/8 x 14 7/8"

2.2 Weight $2\frac{1}{2}$ pounds maximum

3. INSTALLATION

The NS SELCH may be installed in any even numbered universal expansion slot (i.e., 0, 2, 4, or 6) in the Central Processor Unit (CPU) or in the first memory-I/O expansion chassis. See Figure 1. On 7/16 HSALU the NS SELCH may only be installed in Slot 0 of the CPU back panel.

To install a NS Selector Channel on a Model 74 or a 7/16 BASIC, the Selector Channel must be a 35-391M02. To install a Selector Channel on a 7/16 HSALU the Selector Channel must be a 35-391M02, R02 or higher.

NOTE

A SELCH may be installed in slots 0, 1, or 2 of a Model 80/85 CPU chassis only. In this case cutting of the Multiplexor Bus is not necessary.

3.1 Back Panel Wiring

3.1.1 Multiplexor Channel Bus. At the time of installation it is necessary to cut the Multiplexor Bus wiring between the even numbered slot accepting the SELCH and the next higher numbered slot on the One (1) connector only. The RACK0/TACK0 daisy chain wiring on the back panel is rerouted according to Figure 1. The lower numbered card slots in the chassis become part of the private SELCH Bus on the One (1) connector only.

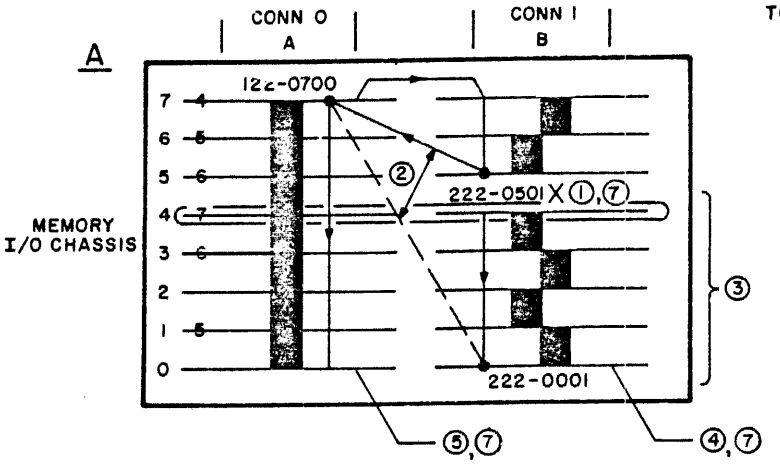
For the convenience of cutting the Multiplexor Bus, the connections between every other slot are made using "top" wire wraps. (This refers to wire wrap back panels only.) This allows the cutting of the bus by simply lifting the top wraps when the SELCH is installed in an even numbered slot. Refer to Figure 1 A during the following example.

To install a SELCH in Slot 4:

1. Remove all wires on Connector One (1), between Slots 4 and 5, on Pins 11 through 26, Rows 1 and 2. (See backpanel map in 02-232M01D08 Sheet 7.)
2. Remove the wire between 222-0001 and 122-0700.
3. Remove the RACK0/TACK0 jumper between Pins 122 and 222 on both the Zero (0) and One (1) connectors of Slot 4.
4. Connect 122-0700 to 222-0501.
5. Install the SELCH into Slot 4 of the chassis. The private SELCH Bus now appears on the Connector One (1) side of Slots 4,3,2,1, and 0. All slots on the Connector Zero (0) side and Slots 7,6, and 5 on Connector One (1) side remain as standard Multiplexor Bus slots.

To install a SELCH in any other even numbered slot of a CPU chassis or a Memory-I/O chassis, a similar procedure is followed. Refer to Figure 1 B, C, D, and E.

NOTE: THE CIRCLED NUMBERS ON ILLUSTRATIONS A, B, AND C REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING INSTALLATION PROCEDURES.



TO INSTALL A SELECTOR CHANNEL IN SLOT 4 OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

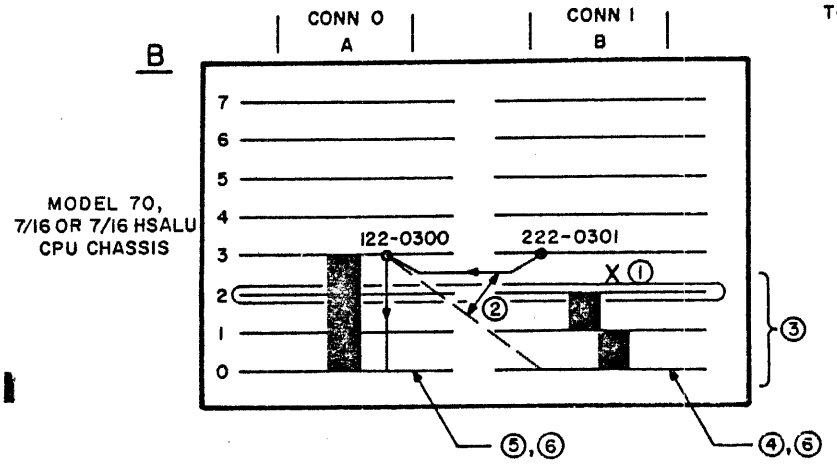
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE, AND SLOTS 7, 6 AND 5 ON CONNECTOR ONE SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ MEMORY MODULE 7, IF IT EXISTS, MUST BE LOCATED IN SLOT 3.

⑦ INSTALL I/O TERMINATORS 35-433 ROI HERE.



TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE CPU CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

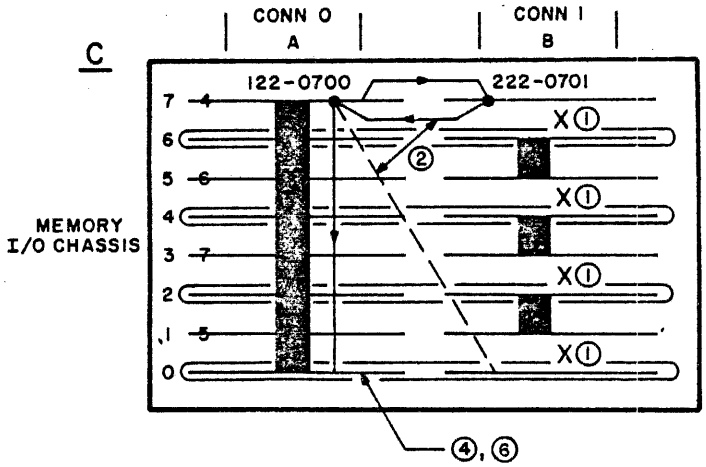
④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ INSTALL I/O TERMINATORS 35-433 ROI HERE.

NOTE 1:
IF A MEMORY I/O CHASSIS IS USED IN THE SYSTEM, ANY SELECTOR CHANNELS MUST BE INSTALLED IN THAT CHASSIS.

NOTE: 2
A SELECTOR CHANNEL MAY NOT BE INSTALLED IN SLOT 2 OF THE 7/16 HSALU. SLOT 0 IS THE ONLY SLOT IN WHICH A SELCH MAY BE INSTALLED.



TO INSTALL 4 SELECTOR CHANNELS (IN SLOTS 6, 4, 2 AND 0) OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS IN FOUR PLACES.

② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

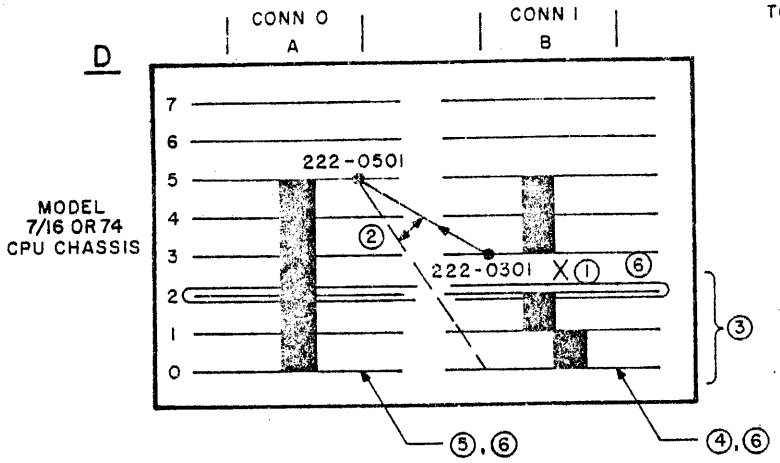
③ EACH SELCH, EXCEPT THE ONE IN SLOT 0, HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 0, 1, 3 AND 5 ON CONNECTOR ONE (CONN.1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

⑤ MEMORY MODULES 5 AND 7, IF THEY EXIST, MUST BE LOCATED IN SLOTS 1 AND 3.

⑥ INSTALL I/O TERMINATORS 35-433 ROI HERE.

Figure 1. Backpanel Modifications



TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE CPU CHASSIS——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

② JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPER.

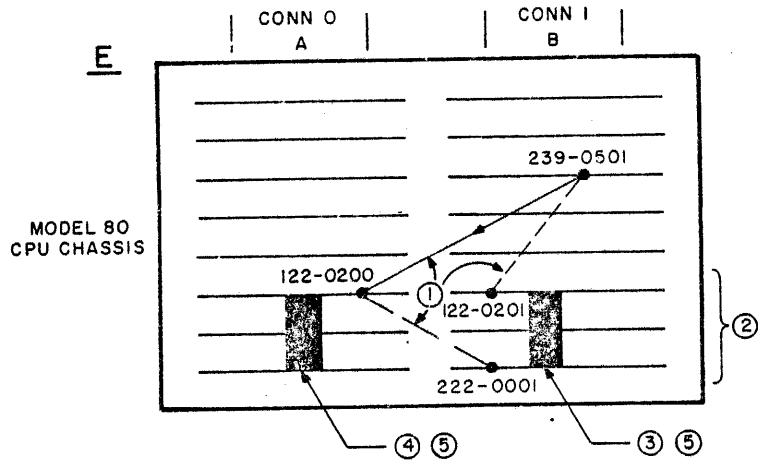
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHE CHASSIS BY INSTALLING A CABLE HERE.

⑥ INSTALL I/O TERMINATORS 35-433 ROI HERE.

NOTE:
IF A MEMORY I/O CHASSIS IS USED IN THE SYSTEM, THE SELECTOR CHANNEL MUST BE IN SLOT 0 OF THE CPU CHASSIS OR IN SOME SLOT OF THE EXPANSION.



TO INSTALL A SELECTOR CHANNEL IN SLOT 0, 1 OR 2 CHASSIS——

① JUMPER RACK0/TACK0 AS SHOWN, REMOVE DASHED JUMPERS.

② THIS SECTION BECOMES THE PRIVATE SELCH BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR SLOTS.

③ EXTEND THE SELCH BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

④ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ INSTALL I/O TERMINATORS 35-433 ROI HERE.

NOTES:
1. IF A 17-183 CABLE IS INSTALLED BETWEEN CONNECTORS ZERO AND ONE IN THE CPU CHASSIS, THIS CABLE MUST BE REMOVED PRIOR TO INSTALLING SELCH.
2. THE INSTALLATION OF A SELCTOR CHANNEL OR OTHER I/O DEVICE CONTROLLER IN THE M80 CPU CHASSIS REDUCES THE MAXIMUM MEMORY SIZE BY 16K BYTES (ONE MSU) FOR EACH SLOT USED!
3. ONLY ONE SELECTOR CHANNEL MAY BE CONFIGURED IN THE MODEL 80 PROCESSOR CHASSIS.

Figure 1. Backpanel Modifications
(Continued)

3.1.2 ACT0/TAC0. The ACT0/TAC0 jumper between Pins 137-0 and 237-0 must be removed from the slot used by the SELCH controller. If the Selector Channel is not the first Direct Memory Access (DMA) channel on the Memory Bus, jumper "K" on the SELCH controller must be removed. Note that on a Model 74 only one DMA device is permitted.

NOTE (Not Applicable on Model 74)

On installations with Multiple SELCH's, remove the "EN0" and the "INH0" filters on all but the last SELCH (Remove the following: R70, R72, C59 and C61).

3.2 Cabling

The cabling necessary for the SELCH depends on the system's physical configuration. When the SELCH Bus does not extend outside the chassis, no cabling is required. When the SELCH Bus must be extended to another chassis, a number of cable configurations can be used. See Figure 2. Care should be taken to minimize bus lengths.

See Figure 2 for a summary of cables.

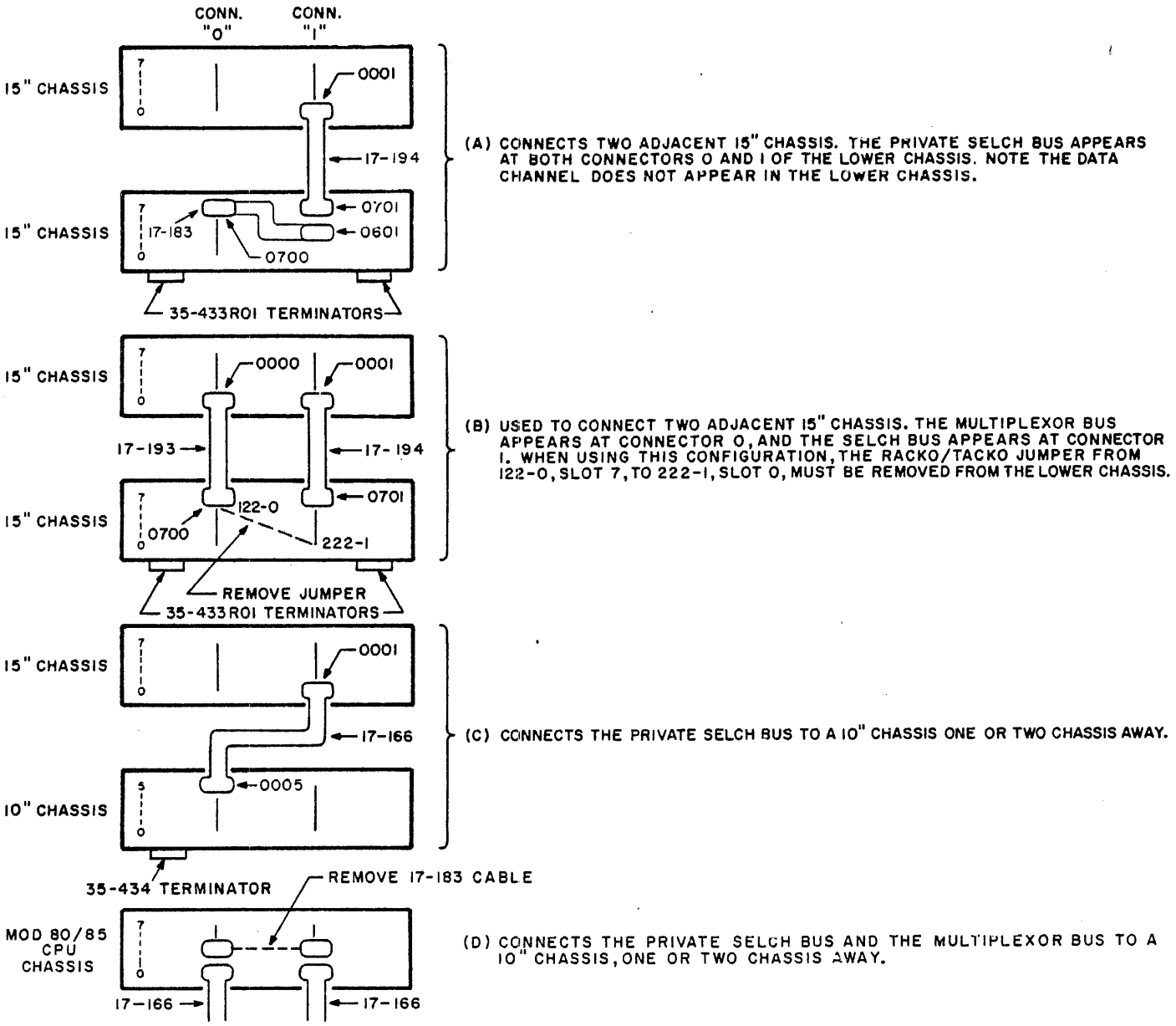


Figure 2. Cabling

4. ADDRESS STRAPPING

The preferred address of the NS Selector Channel is X'F0'. The controller is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-232M01D08. The number and letter designations shown on the schematic refer to the designations on the apparatus side of the SELCH controller board.

5. MODEL 80/85 STRAPPING

For use with the Model 80 or 85 the following options must be exercised:

1. Remove the jumper labled J located between IC 14 and 15.
2. Change the jumper, above IC 53, from (L to X) to (L to 2).

6. INSTALLATION CHECKS

The NS SELCH is factory tested using a special high speed device. Therefore, field checks are contingent upon the user having appropriate hardware and software available with which to exercise the Selector Channel. When the SELCH is used with Model 80 or 85, insure that the strap options on the SELCH have been made according to Section 5.

M70-103
NS SELECTOR CHANNEL
MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-232M01 NS Selector Channel (SELCH) (Product Number M70-103) is a Direct Memory Access port (DMA) which provides block data transfer between a device controller and memory. Once initiated, the transfer is independent of the Processor. The Processor sets up the device controller, loads the SELCH with the starting and final addresses of the memory block, specifies the type of operation (Read or Write), and issues a GO Command. The SELCH then handles the transfer without further direction by the Processor.

The NS Selector Channel is complete on one printed circuit board and occupies one slot in a system chassis. The SELCH provides the drivers, receivers and termination resistors for the private SELCH Bus. This bus originates at Connector One (1) of the SELCH slot and extends to each lower numbered slot in the system chassis on the Connector One (1) side only. The private SELCH Bus can be extended to other chassis, as required. For installation information, refer to Installation Specification 02-232M01A20.

2. SCOPE

This specification describes the operation of the SELCH in its various modes; Setup, Memory Read, Memory Write, and Termination. Where necessary, this specification references the Multiplexor Channel Bus and Memory Bus operations.

3. BLOCK DIAGRAM ANALYSIS

Refer to the SELCH block diagram on Sheet 7 of Functional Schematic 02-232M01D08, and the SELCH Flow Chart, Figure 1, during the following analysis. Before initiating a data transfer via the SELCH, the device controller and the SELCH must be set up. The setup procedure is implemented by the Processor via the Multiplexor Bus (MPX-Bus). When the SELCH is in the Idle mode, the MPX-Bus is tied directly to the private SELCH Bus through the SELCH. This allows the Processor to communicate directly with any device on the private SELCH Bus.

To prepare the SELCH for data transfer, the Address Register (AR) and Auxiliary Address Register (AAR) must be loaded with the starting address in memory where the transfer is to begin, and the Final Address Register (FAR) must be loaded with the address of the last memory location to be accessed. These registers are loaded from the eight least significant Data Lines D080:150 by four consecutive Data Availables (DAs) from the Processor. The first two Data Availables simultaneously load the AR and AAR, which are 16-bit incrementing registers. The AR is incremented, by two, after each halfword is transferred to/from memory, and the AAR is incremented, by one, with each byte transferred to/from the device. Data transfer is terminated when the AAR is equal to the FAR or when the AAR increments past its maximum value, X'FFFF'.

Data transfer is begun by the Processor issuing a GO Command to the SELCH. Transfer to/from the device is now independent of the Processor. The GO Command also prevents communication between the Processor and any device on the private SELCH Bus until the transfer is terminated and the SELCH is addressed.

Data transfer is controlled in the Move Data circuit by inspection of the four least significant bits of the Status Byte presented by the active device on the private SELCH Bus. When any one of the three least significant bits are set, (EX, EOM, or DU), the transfer is terminated. Bit-12 (Busy) regulates the rate of data transfer. In the Memory Read mode, the actual data transfer begins with a memory request, REQ0 active, as soon as a GO Command is issued. When the memory request is serviced by the Processor, the SELCH Memory Bus Control circuit activates Select (SEL), which gates the contents of the Address Register (AR) onto the Memory Address Bus, and gates a halfword of data from memory into the Data Register (DR). At the termination of the memory transfer, the data is loaded from the DR to the Data Buffer (DB) and the AR is incremented.

NOTE

Unless the SELCH has dropped REQ0 in time to remain selected during the next memory cycle, the SELCH is deselected by the rising edge of Inhibit (INH0) after the halfword has been transferred.

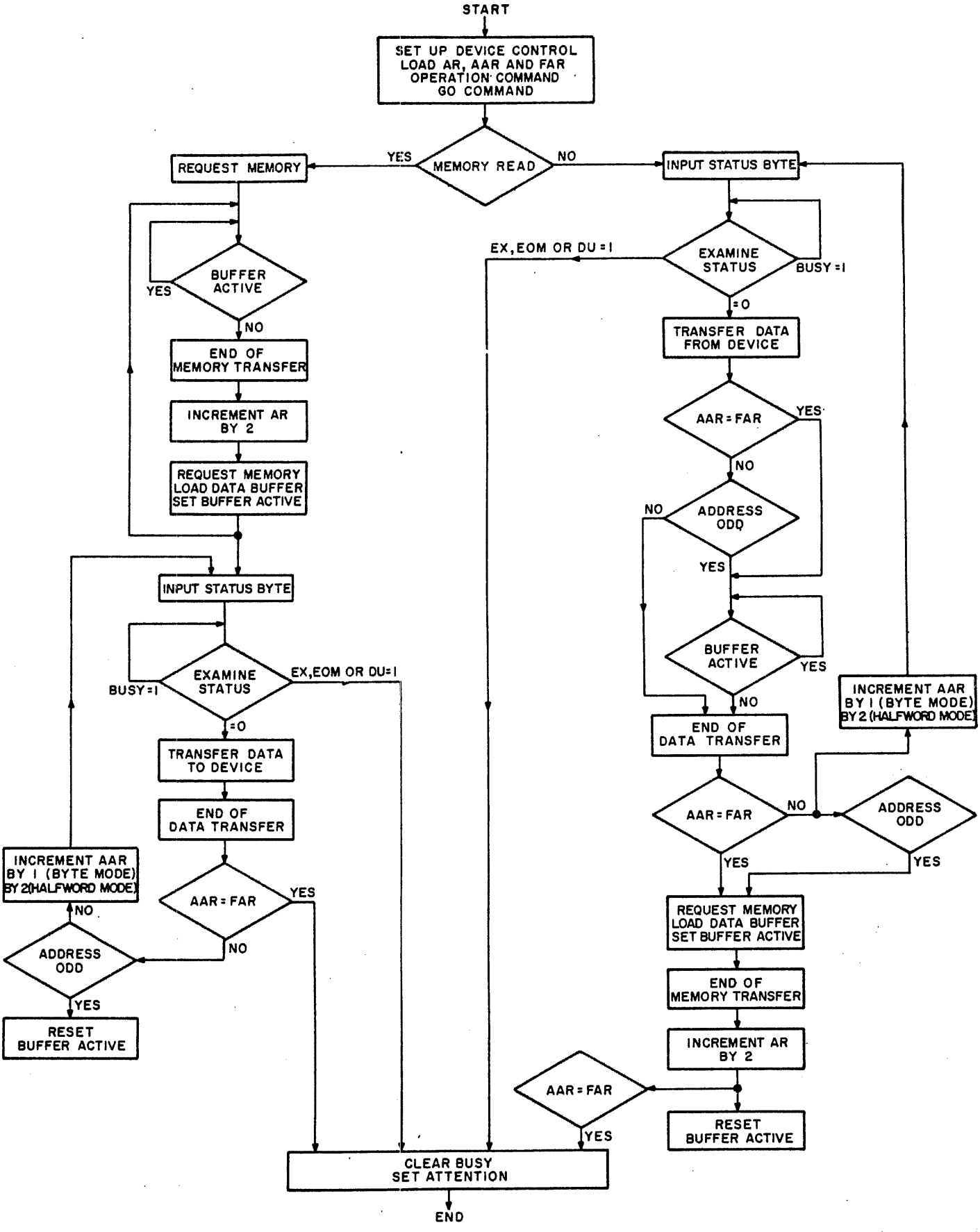


Figure 1. Flow Chart

Once the DB is loaded, data transfer to the device over Private Data Lines PD000:150 is initiated and, when applicable, a request is made to fetch the next halfword from memory. This cycle continues until either a match is detected between the contents of the Auxiliary Address Register and contents of the Final Address Register, or until the transfer is aborted due to an error condition.

In the Memory Write mode, the data transfer sequence described previously for Memory Read mode is reversed. That is, two bytes of data are loaded into the DR from the device prior to a memory request and the data flow is from the device to the DR, DR to the DB, and finally into memory.

The Branch Gate circuit and the Move Data circuit control the flow of data between memory and the device. The Branch Gate supervises the overall data flow, while the Move Data circuit performs the handshaking between the SELCH and the active device on the private SELCH Bus.

Upon termination of the data transfer, the program is notified via an interrupt and by the inactive state of the SELCH Busy flip-flop which is presented to the program as Bit-12 of the SELCH Status Byte.

Selector Channel Status and Command Byte Data is shown on Table 1.

TABLE 1. SELECTOR CHANNEL STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE					BSY			
COMMAND BYTE			READ	GO	STOP			

BSY — When this bit is set, a one shot generates the EBS1 pulse to start the appropriate SELCH operation. When this bit is cleared an interrupt is generated.

READ — This command, Bit-2, sets the Memory Write (WT) flip-flop. The controller on the SELCH Bus is setup for a device Read operation.

GO — This command, Bit-3, clears the MSC flip-flop and sets the BSY flip-flop to initiate the Data Transfer mode.

STOP — This command, Bit-4, from the Processor clears the BSY flip-flop and initializes the Load/Unload Sequencer. During the Data Transfer mode, execution of the command is delayed until the end of a memory cycle, if one is in progress.

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

This section relates to Functional Schematic 02-232M01D08, Sheets 1 through 6. Note that in INTERDATA functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D080 is Data Line Number 8 (D08). The last character (0) inidicates that when D080 is active, the line is at a logical Zero level.

4.2 SELCH Control Circuit

In the Idle mode, the SELCH Address (2M8), Busy (3F3), and Multiplexor-SELCH (MSC) (3FA) flip-flops are reset and the private SELCH Bus is tied directly to the Multiplexor Bus. This allows the Processor to communicate, via the Multiplexor Bus, with any device on the private SELCH Bus.

To communicate with the SELCH, it must first be addressed. The SELCH Address (X'F0' preferred) is placed on Data Lines D080:150 (1A3-8) and the Address control line is activated (ADRS0)(4B8). The SELCH Address is decoded by the four input NAND gate (1F4) and the Address flip-flop is set (2M8). The set output from the Address flip-flop (AD1)(2J[illegible]), when active, prevents the control signals on the MPX-Bus from passing onto the private SELCH Bus by holding the Control Line Gate inactive (CLG1) (1B2). Capacitors C33 and C34 (4D8) delay the propagation of the Private Address control line (PADRS0) (4F9) to the SELCH Bus, so that when the SELCH is being addressed PADRS0 does not become active. This delay allows the SELCH to be addressed without resetting the Address flip-flop of the active device on the private SELCH Bus.

The simultaneous loading of the Address Register (AR) and Auxiliary Address Register (AAR), and the loading of the Final Address Register (FAR) is accomplished by four consecutive Data Availables (DAs) from the Processor. The Load/Unload Sequencer (2L2) controls the loading of these registers (AR, AAR, and FAR) and the unloading of the AAR. The sequencer is set to its initial state by the termination of the last data transfer, a Stop Command, or a System Clear (SCLR0)(4MS) so that the first DA, through Data Available Gate (DAG0)(2L4), will activate Load Address Register High (LARH0)(2S2).

LARH0 gates Data Lines DA081:151 (1D3-8) into the eight most significant bits of the AR and AAR. The rising edge of the first and each successive Data Available Gate (DAG0)(2L4) increments the sequencer and allows the next DA to activate the next load line. The second DA loads the eight least significant bits of these registers. The third and fourth DAs will then load the Final Address Register in the same order. The contents of the AAR may be inspected, via the program, by issuing two Data Requests (DR) to the SELCH whenever the Load/Unload Sequencer is in its initial state. (e.g., Upon termination of a SELCH transfer, sequencer initialized, the FAR may be inspected to determine if the entire block of data had been transferred.)

If a Memory Write operation is desired, an Output Command with Bit-10 set must be issued to set the Write flip-flop (3F5). Since the Write flip-flop is reset by the Data Available/Request Gate (DARG1)(2L5) whenever a DA or DR is sent to the SELCH (setup procedure), no command is necessary to initiate a Memory Read operation.

Data transfer commences with a GO Command from the Processor, which is an Output Command with Bit-11 set. The GO Command sets both the Busy (3F3) and MSC (3F4) flip-flops. The setting of the Busy flip-flop causes an End of Busy Set pulse (EBS1) (3H4) to be generated. This pulse is generated from the falling edge of BSY0 (3F3), and is used by the Branch Gate circuit to initiate the transfer cycle. The Busy latch circuit remains set until the Selector Channel detects the termination of transfer and its state is presented to the program via Bit-12 of the Sense Status Byte.

The MSC flip-flop is reset by SCLR0A or by addressing the SELCH, Set Gate active (SGAD1)(2L9), when the Busy flip-flop is reset. The resetting of the MSC flip-flop, MSC0 active, clears any pending interrupt in the Selector Channel.

Information is steered from the SELCH to both the Data Lines D080:150 (1B4-9) and the Private Data Lines PD080:150 (1S4-9) by the proper gating of four each, four-to-one line multiplexors (Sheet 1). For example; with the SELCH idle, Busy reset, all Data Lines are tied directly to the Private Data Lines in both directions.

4.3 Memory Bus Control Circuit

Memory Bus Control timing relationships are shown in Figure 2. A SELCH request for memory is started by activating Set Request (SREQ0)(3S4). SREQ0 is activated by the Branch Gate circuit (3M8) when either the SELCH has received a halfword of data from the device or, in the Memory Read mode, whenever the Memory Data Register is available to accept the next halfword.

SREQ0 is applied to the direct set input of the Request flip-flop (REQ)(4L5) which sets the flip-flop and sends REQ0 to the Processor. When REQ0 is received, the Processor generates Enable (EN0). EN0, on the first DMA device, is jumpered to Accept (ACT0) which generates the daisy chain priority loop through all DMAs in the system. The daisy chain begins at the highest priority DMA as EN0, and propagates to the lower priority DMAs as Transmit Accept (TAC0) until it is captured by the first DMA requesting a memory cycle. When the REQ flip-flop is set and ACT0 (EN0) is active, the ACT0/TAC0 contention circuit (4H2) blocks the propagation of TAC0, and provide highs on the J input to the SEL flip-flop and the K input to the REQ flip-flop. Thus, on the rising edge of EN0, the Select flip-flop becomes set and the Request flip-flop is reset. When the SELCH REQ flip-flop is reset and ACT0 (EN0) is active, the ACT0 signal is propagated as TAC0 to the DMA with a lower priority.

The trailing edge of Inhibit (INH0) (4H5), from the Processor, indicates the end of the memory cycle. This edge, unless the SELCH has dropped REQ0 in time to remain selected during the next cycle, causes the SEL flip-flop to reset. Two pulses, End of Memory Transfer (EMX0) (4M7) and Inhibit (INH0P) (4M2), are generated by the leading and trailing edges of INH0 respectively. EMX0 is used by the Branch Gate circuit to indicate the end of the memory transfer. The Address Register is toggled by the AND function of SEU and INH1.

In the Memory Read mode, the Memory Data Register (MDR) is cleared by Clear Data Register (CDR0) (4R2) which is generated by the trailing edge of REQ1. Write Not (WT0A) (3F5) is ANDed with SEL1 to form Enable Memory Data Read (ENMDR1) (4R6), which gates the contents of the MDR onto the Memory Data Lines MD000:150 (Sheet 6) for the restore portion of the memory cycle. (This function is disabled when using solid state memory.) The contents of the memory location accessed is gated to the direct set inputs of the MDR by Enable Memory Strobe (ENMS1) (4R4). This function is WT•SEL•CDR0 for use with core memory and WT•SEL•INH when using solid state memory (4R4).

When writing to memory, the contents of the Data Buffer is gated onto Memory Data Lines MD000:150 (Sheet 6) by Enable Memory Data Write (ENMDW1)(4R3), when selected. A Memory Write operation is indicated to the Processor by activating WRT0A (4S3).

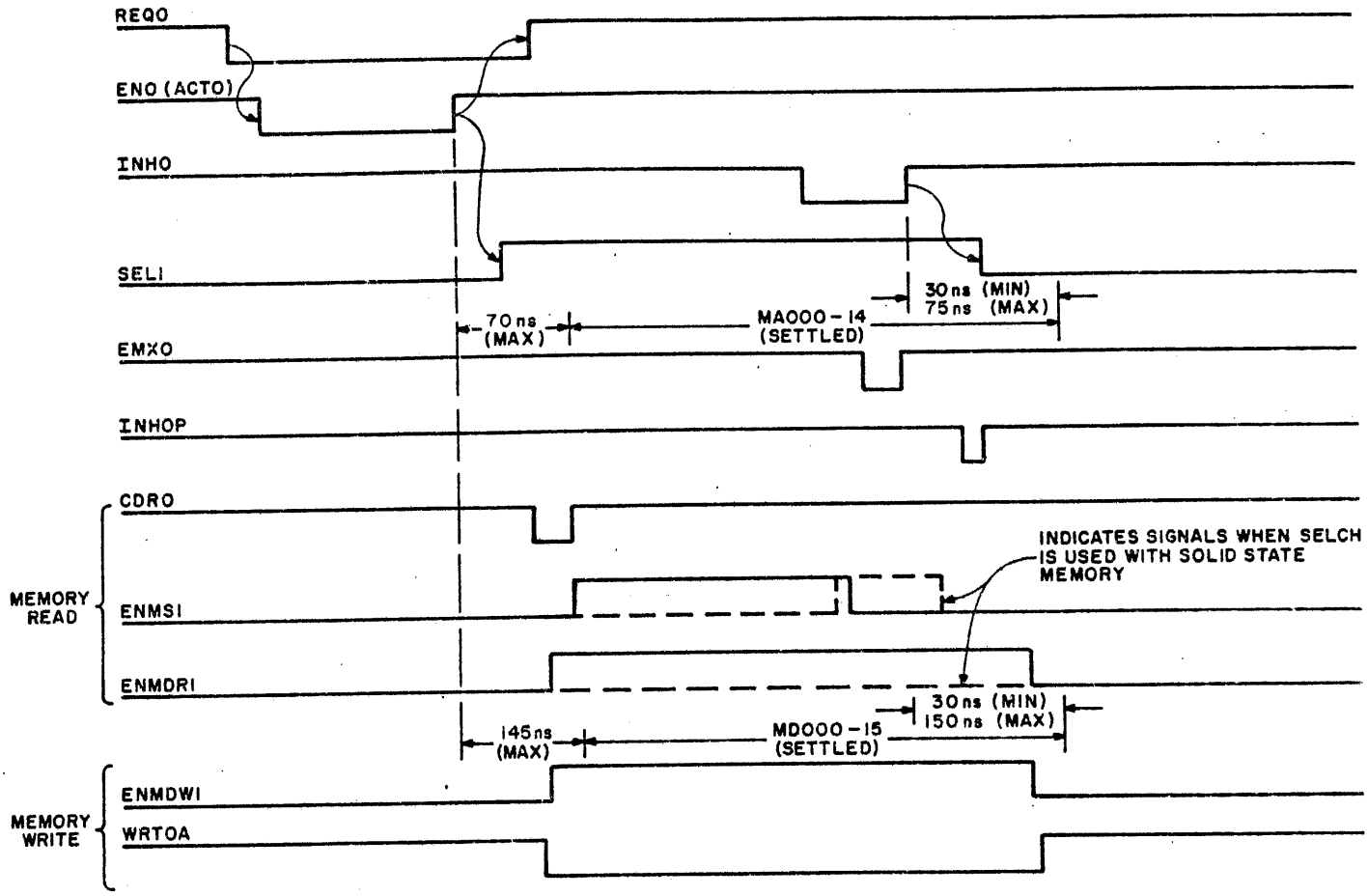


Figure 2. Memory Bus Control Timing Diagram

4.4 Address Register and Auxiliary Address Register.

The Address Register (AR) and Auxiliary Address Register (AAR) (Sheet 5) each consist of four, four-bit counters. These registers are loaded simultaneously by the Processor from Data Lines D080:150 (1A3-8), under control of the Load/Unload Sequencer (as discussed in Section 4.2), with the starting address from which the block transfer is to begin. The contents of the AR (Sheet 5) is gated onto Memory Address Lines MA000:140 (5R1-8) whenever the SELCH is selected, SEL flip-flop set. The AR is incremented with each memory transfer by Select Inhibit (SINH0) (4K8). The AAR (Sheet 5) keeps track of the transfer between the SELCH and the device. This register is incremented, by one, for each byte of data transferred by Toggle Auxiliary Address Register (TAAR0) (3M1). When the transfer is in the Halfword mode, TAAR0 is generated twice for each transfer. The outputs of the AAR are used by the Match circuit to determine the end of the data block. Its contents may be examined, via the program, by issuing two consecutive DRs to the SELCH when the sequencer is initialized. In addition, AAR151 is used in the Byte Transfer mode to determine whether the byte being transferred is odd or even, for byte steering. Carry Out from the most significant stage of the AAR (CO0) (541) terminates the transfer, clear Busy, when a transfer is attempted past the maximum memory address. This feature prevents 'wrap-around' in memory.

4.5 Final Address Register

The Final Address Register (FAR) is implemented by four quad latches (Sheet 5). This register, like AR and AAR, is loaded by the Processor under control of the Load/Unload Sequencer. The outputs of this register are used exclusively by the Match circuit to determine when the final address of the transfer is reached.

4.6 Memory Data Register and Data Buffer

The Memory Data Register (MDR)(Sheet 6) is a16-bit register composed of 16 edge triggered JK flip-flops. In the Memory Read mode, the MDR is first cleared by Clear Data Register (CDR0) (4R2) and then direct set by each active bit on Memory Strobed Data Lines MS000:150 (Sheet 6). During a Memory Write, the data, in double rail format, present at the J and K inputs to the MDR, is toggled into the flip-flops on the trailing edge of either Load Data Register High (LDRH0)(649) or Load Data Register Low (LDRL0)(6J9).

As soon as the MDR is loaded, if the Data Buffer (DB) is empty (as determined by the inactive state of the Buffer Active flip-flop)(3H1), the MDR contents are loaded into the DB (Sheet 6) by Load Data Buffer (LDB1)(357). Information present in the DB is, in turn, either written into memory via Memory Data Lines MD000:150 or sent to the device on Private Data Lines PD000:150.

4.7 Data Transfer Circuit

Refer to Figure 3 for Memory Read timing diagrams and Figure 4 for Memory Write timing diagrams. The Memory Read timing diagram shows the timing of a three byte transfer, in the Byte mode, of 2,000,000 bytes/second. Figure 4 shows a transfer of two halfwords, in the Halfword mode, to a slower device.

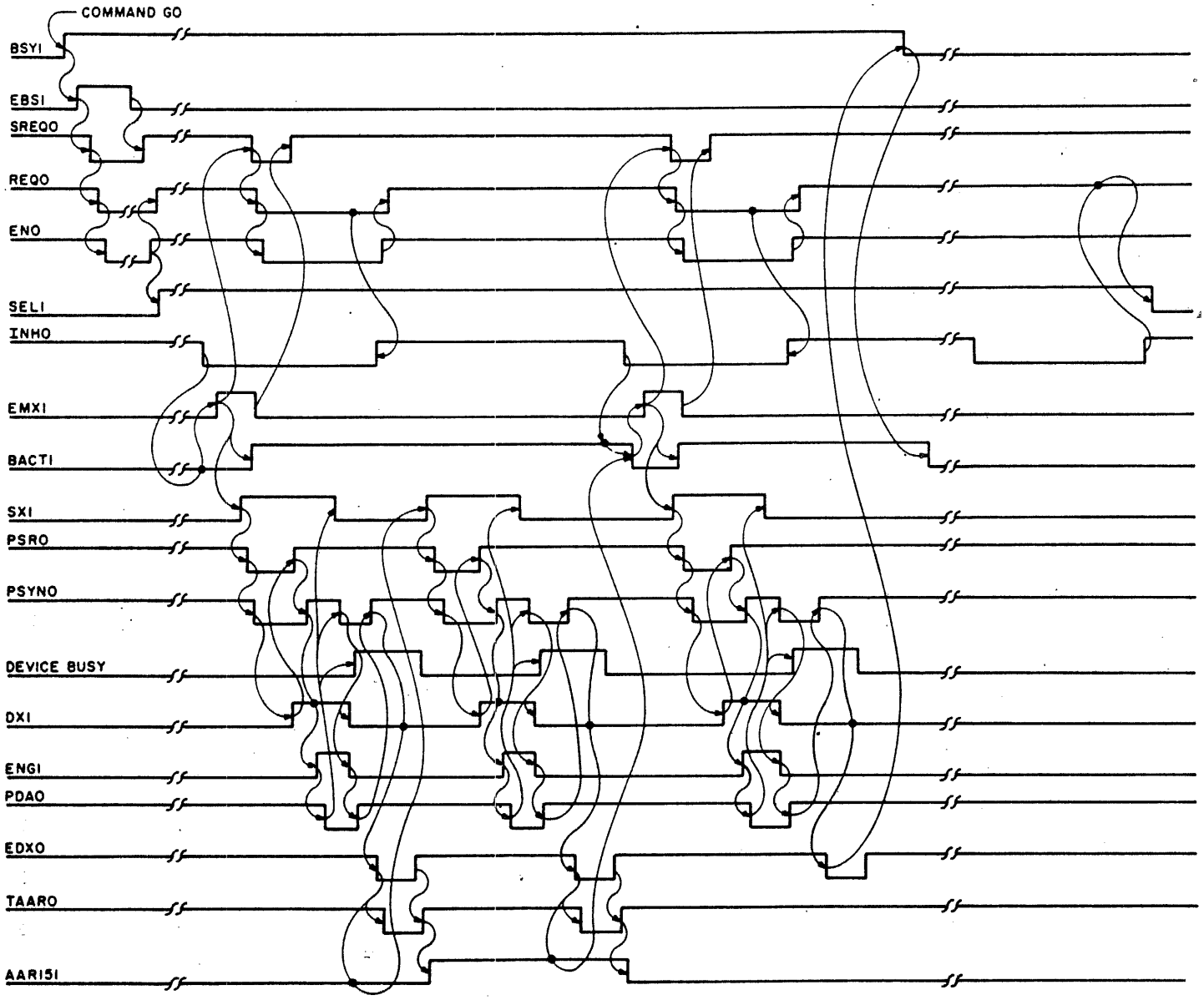


Figure 3. Memory Read (Byte Mode)

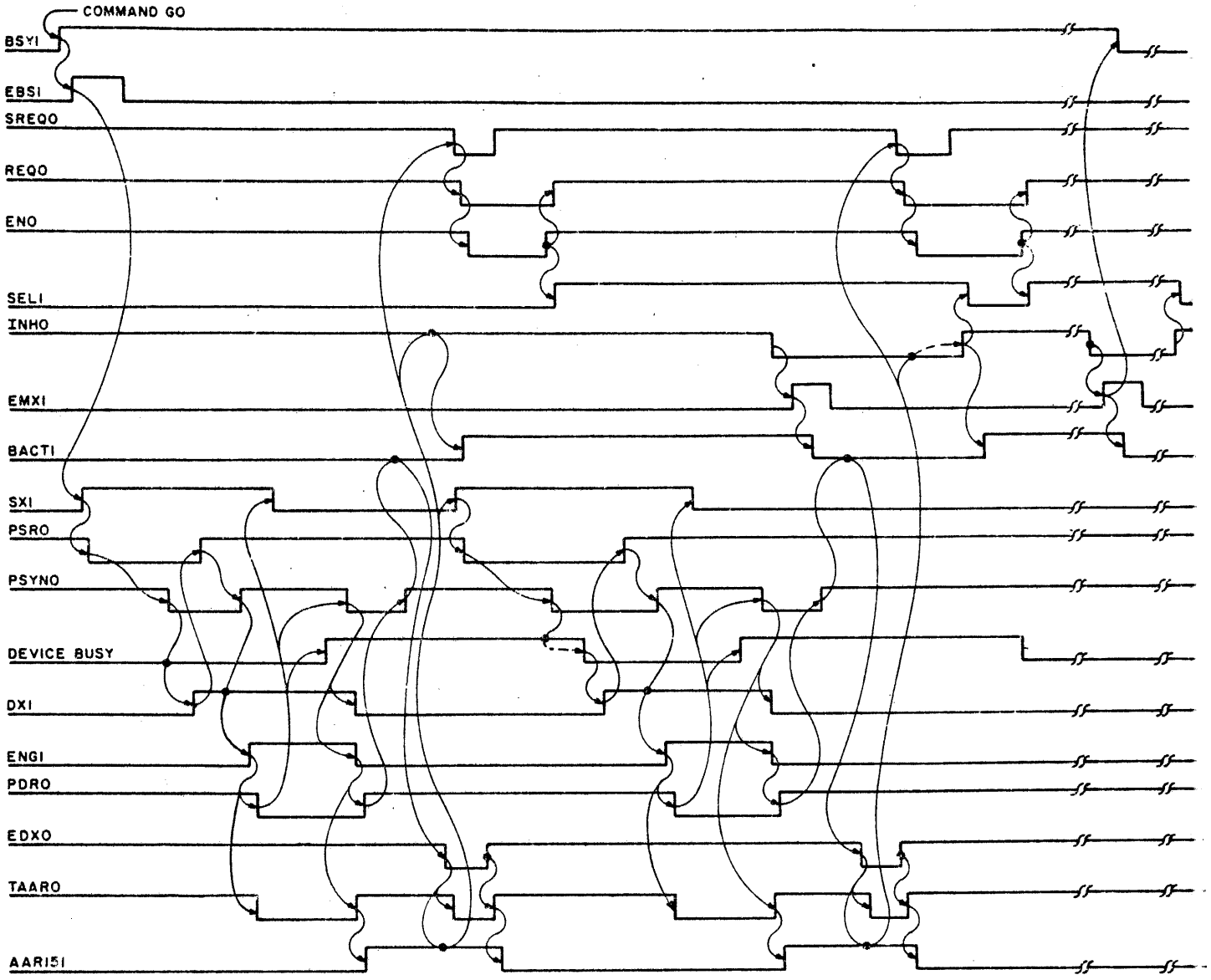


Figure 4. Memory Write (Halfword I/O Mode)

A GO Command to the Selector Channel sets the Busy flip-flop which generates the End of Busy Set pulse (EBS1)(3K8).

In the Memory Read mode, EBS1 is decoded by the Branch Gate circuit and SREQ0 is generated. Thus, a request for memory is initiated. When the halfword of data is present in the MDR, the End of Memory Transfer pulse (EMX1)(4R6) becomes active and the Branch Gate circuit once again requests memory and generates Set Status Transfer (SSX0)(3S5) and Load Data Buffer (LDB1) (3S7). These signals initiate the transfer to the device and load the Data Buffer (DB) respectively.

SSX0 sets the Status Request flip-flop (3F6) which activates the Private Status Request control line (PSR0)(3G6) to the active device on the private SELCH Bus. This Status Request examines the four least significant bits of the Status Byte. If any of the three least significant bits (EX, EOM, or DU) are set, the transfer is terminated by resetting the Busy flip-flop (3F3). The assumption is made that each of these status bits remain reset for the remainder of this discussion. With Bit-12 (Busy) of the Status Byte reset, the Data Transfer flip-flop becomes set (3F7). Data Transfer (DX0)(3E1) inhibits the generation of PSR0, which causes Private Sync (PSYN1)(4B4) from the device to become inactive. This enables Engage to go high (ENG1)(3D8), which allows the Private Data Available control line (PDA0)(3H5) to become active. The Private Data Available/Request signal (PDAR1)(3H5), generated whenever a Private Data Available (PAD0) or Private Data Request (PDR0) signal is active, will then clear the Status Request flip-flop. Upon receipt of Sync from the device, PSYN1 active, the Data Transfer flip-flop becomes reset and ENG1 goes low, disabling PAD0. When the Sync is removed by the device, an 80 nanosecond End of Data Transfer pulse is generated (EDX0) (3J8) which increments the Auxiliary Address Register and is used by the Branch Gate circuit to generate a function in accordance with the truth table for EDX on Sheet 3. This cycle continues until termination of the transfer is detected.

In the Memory Write mode, WT1 active (3F5), EBS1 is used to generate SSX0, and the Branch Gate circuit directs the loading of a halfword of data into the DB before a memory request is made. The transfer of data from the device is the same as described in the Memory Read mode, except that ENG1 is used to generate the Private Data Request control line (PDR0)(3H5) rather than PDA0. Data from the device is loaded into the MDR on the trailing edge of either Load Data Register High (LDRH0)(2R2) or Load Data Register Low (LDRL0)(2R2), depending on which eight bits are being loaded. In the Halfword Transfer mode, both LDRH0 and LDRL0 are generated simultaneously. With WT1 active, the generation of EDX1 is delayed by activating the clear input to the one-shot (3H8) when the Buffer Active flip-flop is set (BACT1)(3H1), if either the transfer to the device is on an odd boundary or when a Match is detected (MCH0)(5J2). This prevents the reloading of the Data Buffer (DB) before the last halfword has been written into memory.

4.8 RACK0/TACK0 Contention Circuit

The Selector Channel directs the propagation of the Acknowledge signal to lower priority devices on the Multiplexor Channel Bus as well as devices on the private SELCH Bus. If the Selector Channel Attention flip-flop (4B4) is set, the SELCH captures the Receive Acknowledge signal (RACK0) (4B3), place its device address on the Data Lines and return Sync to the Processor, Attention Sync (ATSYN0)(4F4) active. If the Attention flip-flop is reset, RACK0 is propagated as either Private Transmit Acknowledge (PTACK0)(4F2) or Transmit Acknowledge (TACK0)(4F3). Since devices on the private SELCH Bus have a higher interrupt priority than devices below the SELCH on the MPX Bus; if the Private Attention Test line is active (PATN0) (4B1), PTACK0 is generated rather than TACK0. Note that when MSC0 is high (3F4), PATN0 is disabled so that a device on the private SELCH Bus may not interrupt the Processor while the SELCH is active.

5. MAINTENANCE, TROUBLE SHOOTING, AND TEST

Before attempting any maintenance or testing, insure that the necessary back panel modifications and SELCH board option strapping have been made in accordance with the NS Selector Channel Installation Specification 02-232M01A20.

To insure a 2,000,000 Byte/second transfer rate in the Byte Transfer Mode, it is necessary to limit the maximum delay between PDA0, PDR0, and PSR0 and the return of Sync from the device (PSYN0), to 30 nanoseconds. In addition, the device must be ready for the next byte of data, Busy Status Bit reset, whenever a Status Request is made. Field testing of this device is contingent upon the user having appropriate software and hardware available with which to exercise the Selector Channel. There are no adjustments associated with this device. Do not install Terminator Boards 35-433 or 35-434 on the SELCH bus if a transfer rate of 2,000,000 Bytes/second is to be maintained in the Byte (8 Bit) Mode. The SELCH Bus should be contained on a single 15 inch chassis if no terminators are used.

6. MNEMONICS

The following list provides a brief description of each mnemonic found in the SELCH. The source of each signal on Functional Schematic 02-232M01D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AAR001:151	Outputs of the Auxiliary Address Register	5F1-5F9
ACT0	Accept - Request for memory accepted by Processor	4H1
AD1	Address - Active when SELCH is addressed	2K7
ADRS0	Address control line from MPX-Bus	4B8
AG081:151	Address Gated Lines - Output of Address Strap	1E3 - 1E8
ATN0	Attention - Attention to Processor	4F1
ATSYN	Attention Sync - Generated by an Acknowledge Attention from Processor	4F4
BACT1	Buffer Active - Indicates that valid data is present in the DB	3H1
BSY	Busy - Indicates a data transfer is in progress	3F3
CDR0	Clear Data Register - Clears MDR prior to loading from MS000:150	4R2
CBSY0	Clear Busy - Terminates transfer when a match is detected	3M3
CL070	Control Line 7 - Control Line from MPX-Bus	4B6
CLG1	Control Line Gate - Gates Private Control Lines	1C2

MNEMONIC	MEANING	SCHEMATIC LOCATION
CLUS0	Clear Load/Unload Sequencer - Clears Sequencer	3S2
CMD0	Command Control Line from MPX-Bus	4B8
CMG	Command Gated by AD1	2S7
CO0	Carry Out of the AAR - Prevents Memory 'Wrap-around'	5A1
D000:150	Data Lines from MPX-Bus	1A3 - 1A8 2A1 - 2A8
DA0	Data Available Control Line from MPX-Bus	4B7
DLG0	Data Line Gate - Gates Data Lines and Private Data Lines	1R2 - 1D3
DB001:151	Outputs of Data Buffer	6G2 - 6G9 6R2 - 6R9
DR0	Data Request Control Line from MPX-Bus	4B7
DRG0	Data Request Gated by AD1	2L5
DX	Data Transfer flip-flop	3F8
EBS1	End of Busy Set - Signals the start of a SELCH transfer	3J4
EDX1	End of Data Transfer - Signals the end of a device transfer	3J8
EMX1	End of Memory Transfer - Signals the end of a memory transfer	4R7
EN0	Enable from Memory Bus	4H2
ENG1	Engage - Gates either PDS0 or PDR0	3D8
ENMDR1	Enable Memory Data Register Read - Gates contents of MDR to MD000:150	4R6
ENMDW1	Enable Memory Data Register Write - Gates contents of DB to MD000:150	4R3
ENMS1	Enable Memory Strobe - Gates contents of MS000:150 to MDR	4R4
HW0	Halfword Control Line from MPX-Bus	1D2
INH0	Inhibit from Memory Bus	4H5
LARH0	Load Address Register High - Loads AAR and AR, Bits 00:07	2R2
LARL0	Load Address Register Low - Lards AAR and AR, Bits 08:15	2R2
LDB1	Load Data Buffer - Load contents of MDR to DB	3S2
LDRH0	Load Data Register High - Loads MDR Bits 00:07	3F8
LDRL0	Load Data Register Low - Loads MDR Bits 08:15	3H9
LFRH0	Load Final Address Register High - Loads FAR Bits 00:07	2S3
LFRL0	Load Final Address Register Low - Loads FAR Bits 08:15	2S3
MA000:140	Memory Address Lines to Memory Bus	5R1 - 5R8
MCH1	Match - Indicates a match between AAR and FAR	5J6

MNEMONIC	MEANING	SCHEMATIC LOCATION
MD000:150	Memory Data Lines to Memory Bus	6G1 - 6G8 6R1 - 6R8
MS000:150	Memory Strobed Data Lines from Memory Bus	6A1 - 6A8 6H1 - 6H8
MSC0	Multiplexor SELCH Control flip-flop	3F4
PADRS0	Private Address Control Line to SELCH Bus	4F8
PATN0	Private Attention from SELCH Bus	4B1
PCL070	Private Control Line 7 to SELCH Bus	4R6
PCMD0	Private Command Control Line to SELCH Bus	4F8
PD000:150	Private Data Lines - SELCH Bus	2F1 - 2F8 1S3 - 1S9
PDA0	Private Data Available Control Line to SELCH Bus	3H5
PHW0	Private Halfword Control Line from SELCH Bus	1A1
PSR0	Private Status Request Control Line to SELCH Bus	3H6
PSYN0	Private Sync from SELCH Bus	4B5
PTACK0	Private Transmit Acknowledge to SELCH Bus	4F2
RACK0	Receive Acknowledge from MPX-Bus	4B5
RBA0	Reset Buffer Active - Resets Buffer Active flip-flop	3M2
REQ0	Request - Request for memory cycle to Memory Bus	4R5
SCLR0	System Clear - Initialize Signal	4H4
SGAD1	Set Gate - Sets Address flip-flop	2LR
SR0	Status Request Control line from MPX-Bus	4B6
SREQ0	Set Request - Initiates a request for memory	3S4
SSX0	Set Status Transfer - Sets the Status Request flip-flop	3S5
SX	Status Transfer - Status Request flip-flop	3F6
SYN0	Sync to MPX-Bus	2S5
TAC0	Transmit Accept - To lower priority DMAs	4R1
TACK0	Transmit Acknowledge - To lower priority devices on MPX Bus	4F3
TAAR0	Toggle Auxiliary Address Register - Increments AAR	3M1
TAR0	Toggle Address Register - Increments AR	4S7
UAAH0	Unload Auxiliary Address Register High - Unloads AAR Bits 00:07	2R4
UAARL0	Unload Auxiliary Address Register Low - Unloads AAR Bits 08:15	2R4
WT	Write flip-flop	3F5
WRT0A	Write to Memory Bus, when selected	4R3

M49-410
TEST AID
INFORMATION SPECIFICATION

1. INTRODUCTION

This Information Specification covers installation, operation, and maintenance of the M49-410 Test Aid (02-276) and the associated logic in the Processor. Refer to 02-276D08 for schematics of the M49-410 Test Aid.

2. GENERAL DESCRIPTION

The Test Aid consists of a switch display panel and a 17-283 logic card which attaches to the following boards:

35-446 CPU-HI Model 74 Processor
35-446F01 and 35-446F02 CPU-HI 7/16 Basic Processor
35-524 CPU-B Model 7/16 HSALU Processor
35-523F01 and 35-523F02 CPU-B Model 7/32
35-624F01, F02, F03 CPU-B Model 7/32C Processor

The Test Aid provides the ability to examine the address of the micro-code and to stop Processor clocks at option.

3. INSTALLATION

This section provides the information necessary to install the Test Aid on the Processor. The 02-276R01 or higher revision level Test Aid may be used on the Model 74, 7/16 Basic, 7/16 HSALU, 7/32, and 7/32 C Processors. The 02-276R00 Test Aid may be used on the Model 74 and the Model 7/16 Basic. The installation procedure is:

1. Remove the display from the chassis.

2. Place Test Aid logic card over pins on CPU-HI board or CPU-B board (installed in Slot 6 of the Processor back panel, refer to Figure 1) and press down until Test Aid logic card rests on spacers on the Processor board. The switch/display panel assembly may be placed on a table or mounted on the chassis as shown in Figure 2.

3. On the 7/16 HSALU Processor, a jumper must be installed between TP1 on the 35-544 CPU-B board and TP2 on the 35-522 CPU-A board.

4. On the 7/32, a jumper must be installed between TP1 on the 35-523F01 or F02 CPU-B board and TP2 on the 35-522 CPU-A board.

5. On the 7/32 C Processor, a jumper must be installed between TP1 on the 35-625F01, F02, or F03 CPU-B board and TP2 on the 35-624 CPU-A board.

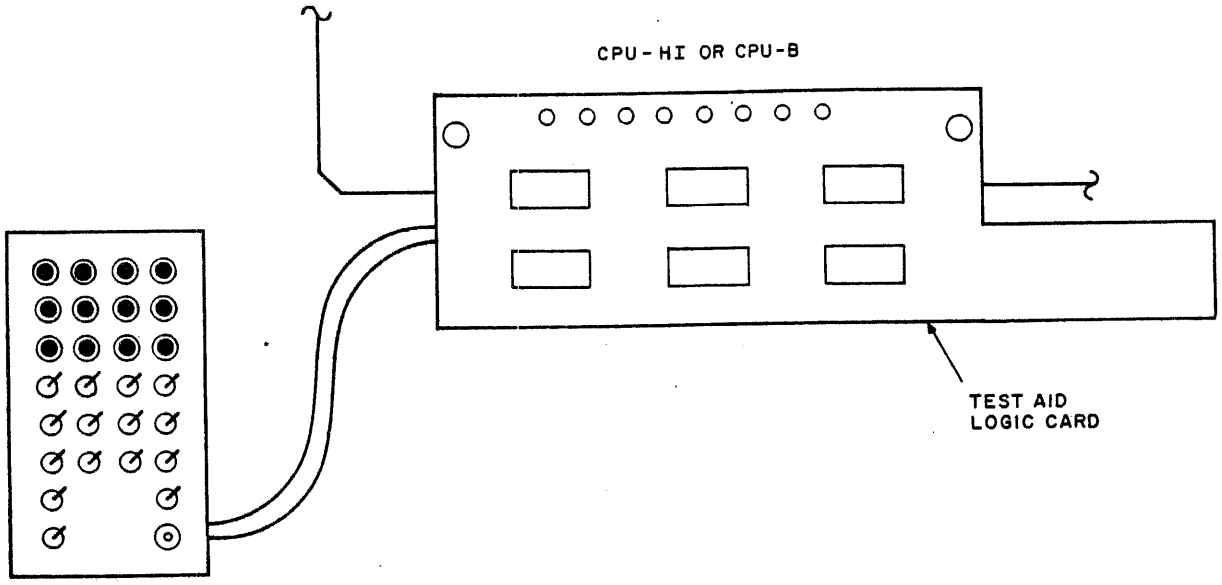


Figure 1. Test Aid Installation

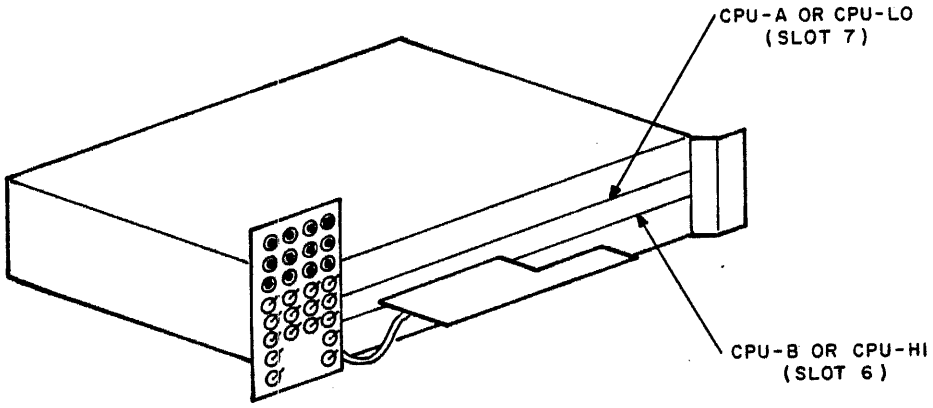


Figure 2. Switch Panel Mounting

4. POWER

Power and ground are supplied by the Processor board. There are no other power requirements.

5. OPERATION

Refer to Figure 3 during the operating description. The 12 Light-Emitting Diodes (LEDs) numbered 4:15 display the contents of the ROM Address Register. The numbers assigned to the LEDs correspond to the ROM Address Register bits. The 12 toggle switches labelled 4:15 provide the ability to set-up a match address. The Test Aid logic stops the Processor clocks when the selected "match address" is in the ROM Address Register and the Address Match switch is in the ON (up) position.

6. ADDRESS MATCH SWITCH

After selecting an address on the Address switches, place the Address Match switch in the ON (up) position. When the ROM Address Register of the Processor contains the "match address", the Processor clocks are stopped on the next clock. The Address Match switch feature can also be used to interrupt and continue micro-code loops. Follow the procedure for address matching. Select an address within a micro-code loop. Once the match has been found, depressing the Clock Advance (ADV) switch once allows the micro-code to go through the loop and match on the selected address again.

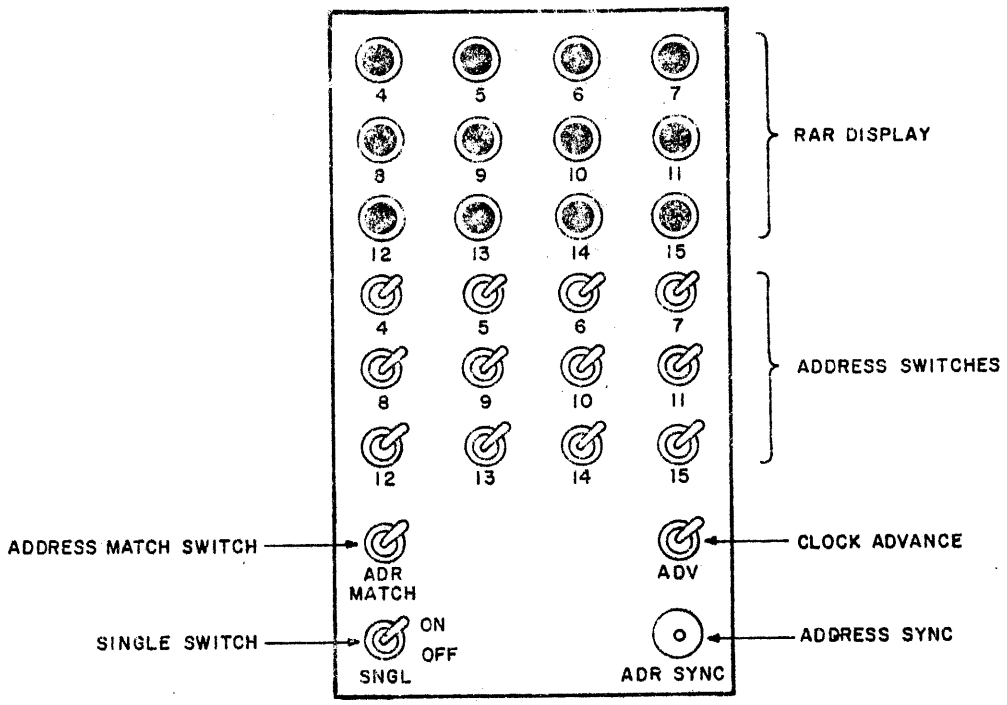


Figure 3. Switch Panel

NOTE

The LED display in most cases is one increment ahead of the match address. The micro-code instruction at the address selected has been executed or is one clock into execution when the match occurs and the Processor clocks stop.

7. CLOCK ADVANCE SWITCH

The Clock Advance switch allows the Processor to generate one clock each time it is depressed when the Address Match or Single switch is in the ON (up) position.

8. SINGLE SWITCH

When the Single switch is in the ON (up) position, the Processor clocks are stopped. With this switch ON, the micro-program may be executed one micro-instruction at a time by depressing the Clock Advance switch.

9. ADDRESS SYNC

Address Sync is a BNC connector whose output is a low going signal that becomes active when the Address switches and the contents of the ROM Address Register compare. The contents of the ROM (specified by the ROM Address Register) will not be loaded into the ROM Data Register until the next Clock which loads the ROM Data Register.

10. OPTION

Pins 'A' and 'B' are normally wired together. Pin 'A' is the output of a comparator that compares the ROM Address Register and the Address switches. When they compare, the signal on Pin A goes high (+5 VDC) causing Processor clocks to stop. Removing the wire between Pins 'A' and 'B' provides a means to bring in any high active signal on Pin 'B' to stop Processor clocks. To match on any high active signal, the Address Match switch must still be placed in the ON (up) position when a match is desired. Removing the wire between 'A' and 'B' will remove the capability to stop Processor clocks on address match. See Figure 4.

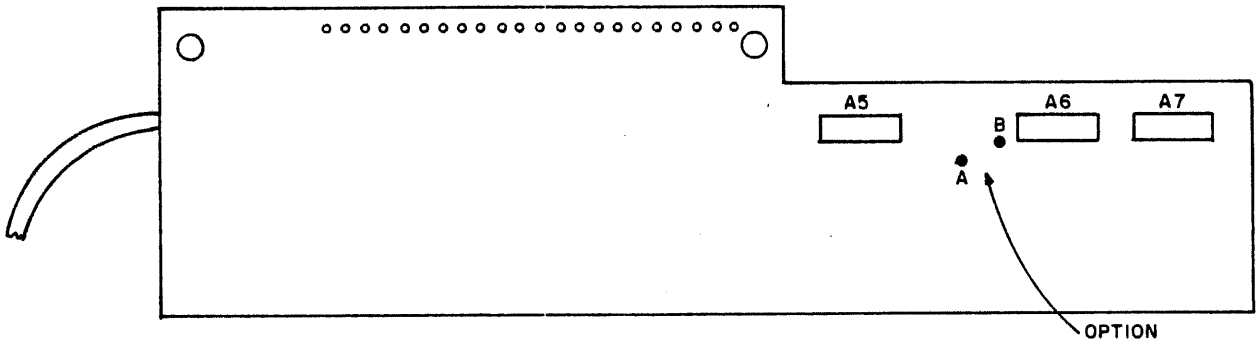
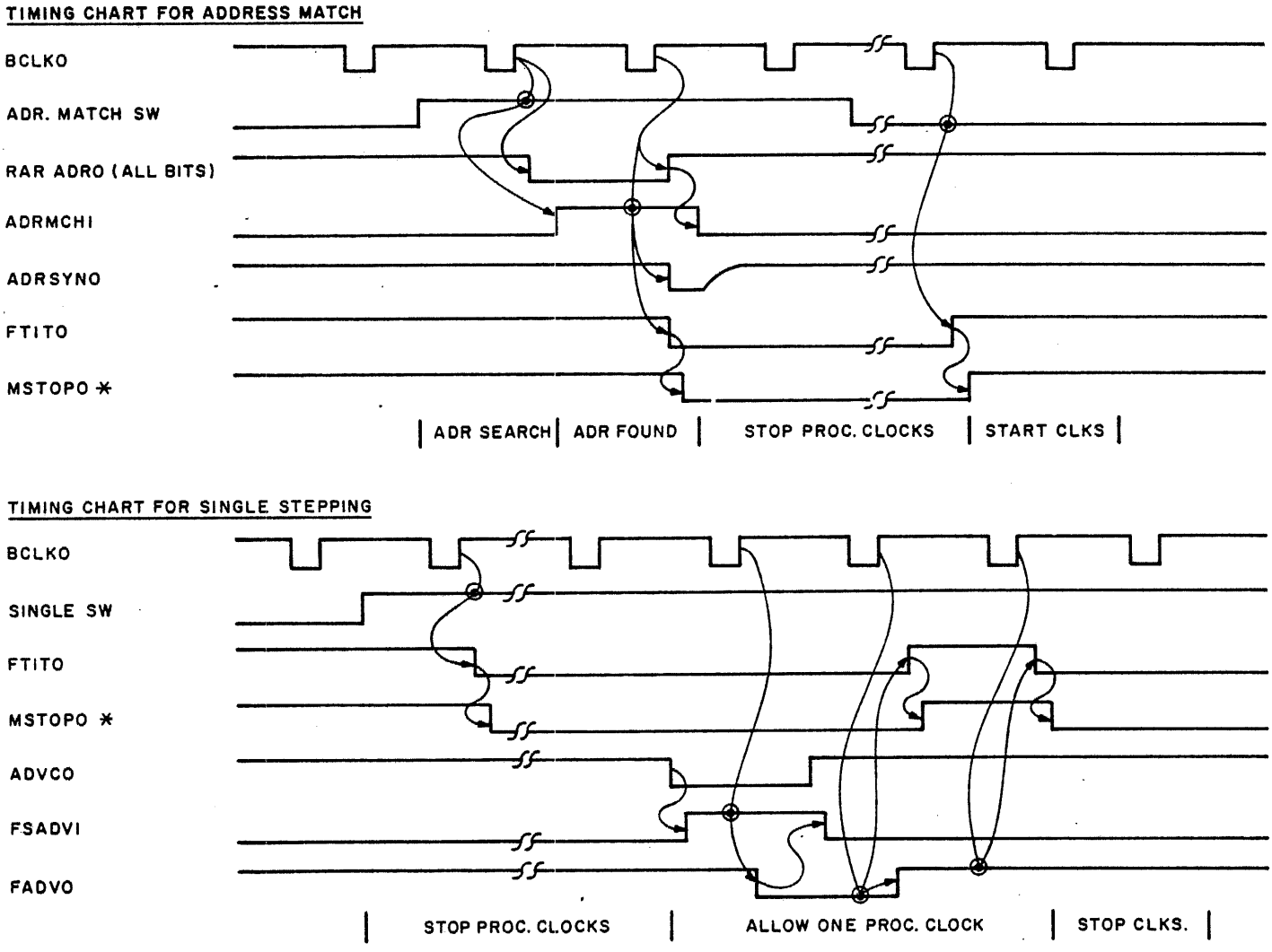


Figure 4. Option Connections

11. TEST AID MAINTENANCE

11.1 Timing

This section defines timing sequences (Figure 5) in the logic of the Test Aid and associated logic in the Processor. Refer to the Processor Functional Schematic, Clock Control sheet, for logic detail of the clock stop.



* MSTOPO IS A CLOCK STOPPING SIGNAL INTERNAL TO THE MODEL PROCESSOR. WHEN ACTIVE ALL PROCESSOR CLOCKS EXCEPT CLKI, BCLKI AND BCLKO ARE STOPPED.

Figure 5. Test Aid Timing

11.2 Mnemonic Definitions

ADRMCH1 - This signal is active when the contents of the ROM Address Register and the Address switches are equal.

ADVC0 - Flip-flop output which goes active when the ADV switch is depressed, inactive when the ADV switch is released.

BCLK0 - Derived from the Processor. This is a clock that cannot be stopped by any clock stop in the Processor. BCLK0 width is typically 60 nanoseconds and the period is typically 250 nanoseconds.

FADV0 - When active, allows FTIT0 to be inactive for one clock period. If ADVC0 and BCLK0 are active at the same time, the FADV0 flip-flop sets.

FTIT0 - This flip-flop is reset by Single switch ON, Address Match switch ON, and a match address.

MCH04-150 - When active, indicates that a particular address switch has been selected.

RAR04-150 - ROM Address Register outputs which indicates the address of the micro-instruction to be executed on the next clock.

12. USE OF MODEL 70 EXTENDER BOARD (11-103) ON THE PROCESSOR

12.1 Hazards

All Model 70 extender boards, below revision level 11-103R02, when used to extend Processor boards, present two hazards.

1. All stiffening metal on the extender board when being plugged in becomes +5VDC. This hazard exists with either Processor board on the extender.

2. When the Test Aid is installed and the CPU-LO or CPU-A is on the extender board, a stiffening bar located on the underside of the extender board rests on top of the Test Aid logic card and forces it down possibly causing a short.

12.2 Modification

The following information describes how to modify the 11-103R01 extender board:

1. Pins 200-0, 200-1, 241-0 and 241-1 are tied into the ground bus of the extender board. These pins in the Processor are +5VDC. Both ends of the extender board tie these pins to the extender board ground but via feedthrough holes causing the ground bus to become +5VDC. Cut the copper between these feedthrough holes and the extender board ground bus. Add a strap from the copper run of Pins 101-0, 101-1, 140-0 and 140-1 to the adjacent ground shield to restore the continuity of back panel ground to extender board ground.

2. Remove stiffening bar on underside of extender board. Three new clearance holes must be drilled so that the stiffening bar mounts horizontally rather than vertically. The original screws may bottom out; if so, use #4-40 x 5/8 screws. Refer to Figure 6.

   After this change is made, care should still be taken to insure that the Test Aid logic card is not shorting to the stiffening bar.

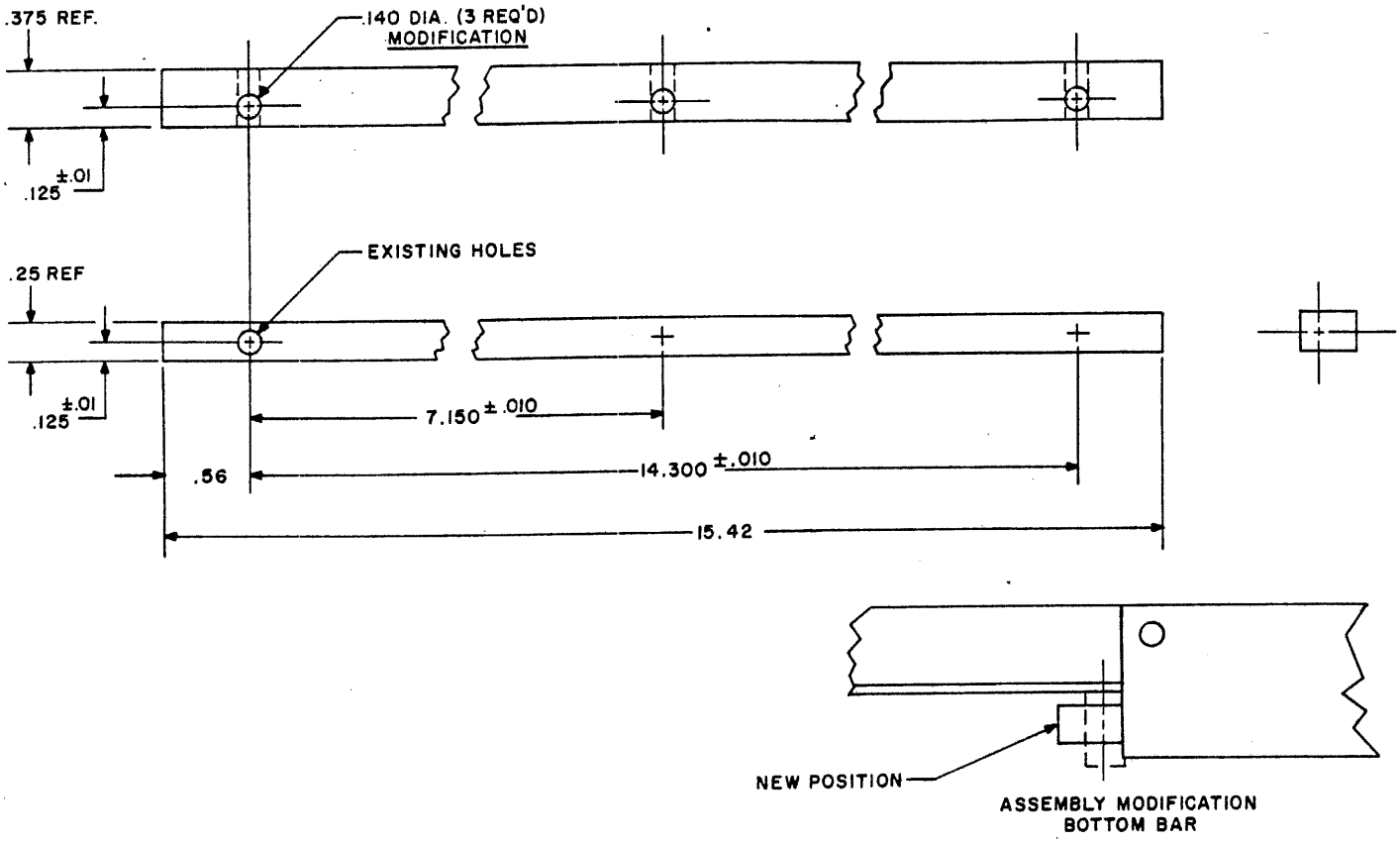


Figure 6. Stiffening Bar

M71-102
HEXADECIMAL DISPLAY
INFORMATION SPECIFICATION

1. INTRODUCTION

The optional Hexadecimal Display Panel provides a means to manually control the Processor, interrogate and display various Processor registers and machine status, set and display Processor memory locations, and may be programmed as an I/O device by the user.

This specification describes the 09-065F02 Hexadecimal Display Panel (Product Number M71-102). It is also applicable to the 09-065F01 Binary Display Panel (Product Number M71-101), which is identical to the Hexadecimal Display Panel except for the omission of the hexadecimal indicators. The Hexadecimal Display Panel provides the following functions:

Displays five bytes of programmable digital information.

Registers and displays five hexadecimal digits of manually entered keyboard data.

Displays the WAIT and Power (PWR) indicators for the Processor.

Provides a 26 key control keyboard for manual input to the display.

Provides two bytes of unbuffered Switch Register data to the Processor.

Provides one byte of status to the Processor.

Provides a three position OFF-ON-LOCK key type switch capable of switching three separate power supply control lines.

Provides a control signal to the Processor that the display requires micro-program support.

2. GENERAL DESCRIPTION

A complete description of the operation of the Hexadecimal Display Panel is provided in the appropriate User's Manual. This specification describes the display from a maintenance view point. Figure 1 shows the Hexadecimal Display Panel.

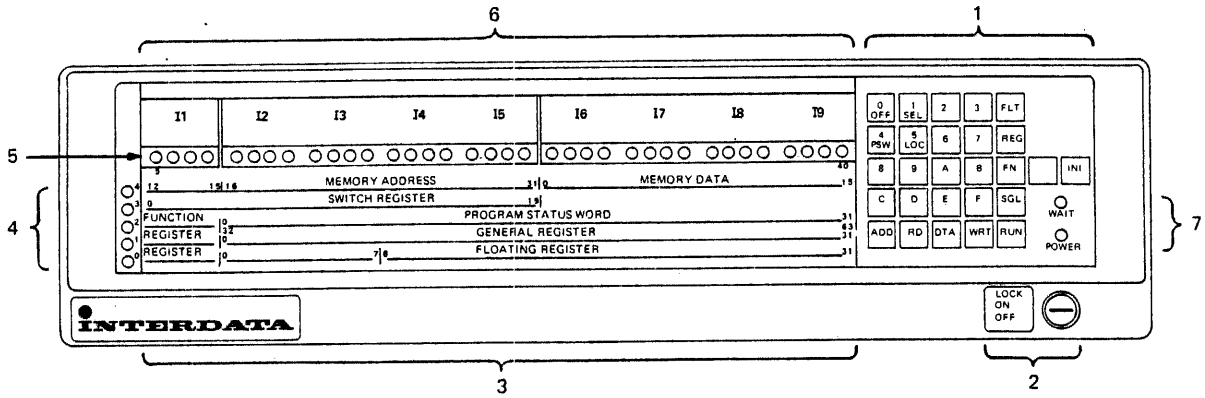


Figure 1. Hexadecimal Display Panel

Various parts of the Hexadecimal Display Panel in Figure 1 are numbered to correlate to the following descriptions.

1. Control Keyboard. The keyboard is the operators manual input to the Processor. The function of the specific keys are:

DTA — The function of the Data (DTA) key is to clear the Switch Register, connect the Switch Register to the display indicators, and enable hexadecimal data to be entered into the register. The Switch Register remains enabled and connected to the display indicators until any non-hexadecimal key other than DTA is depressed.

Hexadecimal Keys 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F supply data to the Switch Register when it is enabled, and the function number or register number for the Processor supported display (see Section 2. 2).

ADD — The Address (ADD) key causes the Processor to read the five hexadecimal characters of the Switch Register, store them in the address portion of the Program Status Word (PSW), and display PSW 32;63 on the indicators.

RD — The Read (RD) key causes the Processor to read the memory location specified by the PSW, increment the PSW address by two, and display on the indicators the new address and the data read from memory.

WRT — Depressing the Write (WRT) key causes the data contained in the Switch Register to be written into the address specified by the PSW, the PSW to be incremented by two, and the new address and the data written to be displayed on the indicators.

FLT — Depressing the Floating-Point Register (FLT) key, followed by any hexadecimal key n, causes Floating-Point Register n to be displayed on the indicators.

REG — Depressing the Register (REG) key, followed by any hexadecimal key n, causes general register n to be displayed.

FN — Depressing the Function (FN) key, followed by any hexadecimal key n, causes the Processor to perform "Function n" as described in the appropriate User's Manual.

SGL — Depressing the Single Step (SGL) key causes the Processor to execute one user instruction and display the last register or function selected.

RUN — Depressing the Run (RUN) key causes the Processor to enter the Run mode at the address specified by the PSW.

INI — Depressing the Initialize (INI) key initializes the Processor.

SEL — Depress DTA, then 0 or F, for selection of Register Set 0 or 1 respectively. Then depress the Function (FN) Key followed by SEL to enable the selected register set to be displayed.

NOTE

The display requires support from the micro-program for all functions other than entering or displaying Switch Register data.

2. OFF-ON-LOCK Key Operated Locking Switch. This switch controls the power to the Processor and allows the keyboard to be completely disabled in the LOCK position.

3. Indicator Formats. These formats aid the user in interpreting the display indicators.

4. Format Selectors L0:4. Light Emitting Diode (LED) indicators L0:4 determine the format to be used to interpret display indicators L5:40.

5. Display Indicators L5:40. These LED indicators are used to display the PSW, general registers, etc., as described by the indicator formats.

6. Display Indicators I1:9. These indicators display the corresponding values displayed on L5:40 in the hexadecimal format.

7. WAIT and PWR. These indicators are illuminated when Processor is in the Wait state and Power is supplied to the Processor.

2.1 Switch Register Entries

When the operator is manipulating the Switch Register, there is no interaction between the display and the Processor. Data is entered into this register by first depressing the DTA key. This operation clears the Switch Register; connects the Switch Register to L5:24 of the display, and allows subsequent hexadecimal keyboard entries to be left shifted into the least significant digit of the resigter. The register is disconnected from the display and disabled when any non-hexadecimal key other than DTA is depressed. The register can be momentarily examined when it is disabled without affecting the Processor operation by depressing any hexadecimal key.

2.2 Processor Intervention

Depressing the following single keys causes the signals ESNC0 and ESNO0 to be complimentarily pulsed (ESNC0 is a positive going pulse):

ADD
RD
WRT
SGL
RUN

Depressing one of the following sequences of two keys causes a similar action:

FLT n (n is any hexadecimal digit)
REG n
FN n

3. FUNCTIONAL DIAGRAM ANALYSIS AND CIRCUIT DESCRIPTION

Refer to Figure 2. Hexadecimal Display Panel Block Diagram and Functional Schematic 09-065D08.

3.1 OFF-ON-LOCK Switch

This switch (2K1) controls power to the Processor by completing the circuit between CONT2 and CONT1 in the ON and LOCK positions. The switch is factory wired to provide one set of closures. This switch also provides a hard ground to the Processor as POFF0 in the OFF position which may be used as an early power down indication. When the switch is in the ON position, LP5 (2L1) is provided to the keyboard to enable the sensing of these switch closures.

3.2 Keyboard

The keyboard (Sheet 2) has a 5 x 5 switch array which is used to enter information to the Hexadecimal Display Panel logic, plus an Initialize (INI) key used to transmit this condition to the Processor (2G1). The keyboard is a self-contained unit and connects to the 35-520 logic board by 27 stakes, 00-1 through 26-1. These normally open switches are encoded by diode logic (Sheet 2) to form HEX01:31 (2B8) and FUN00:30 (2C8), plus a few additional control signals mentioned later in this description. The switches are designed to be high active when a switch is depressed by biasing all receiving gates low with a 220 ohm input resistor. A switch being depressed causes an input gate to go high by supplying LP5 through a current limiting resistor from the common input, Pin 0, if the OFF-ON-LOCK switch is in the ON position. There is no keyboard rollover protection and if more than one key is simultaneously depressed, the result is unspecified.

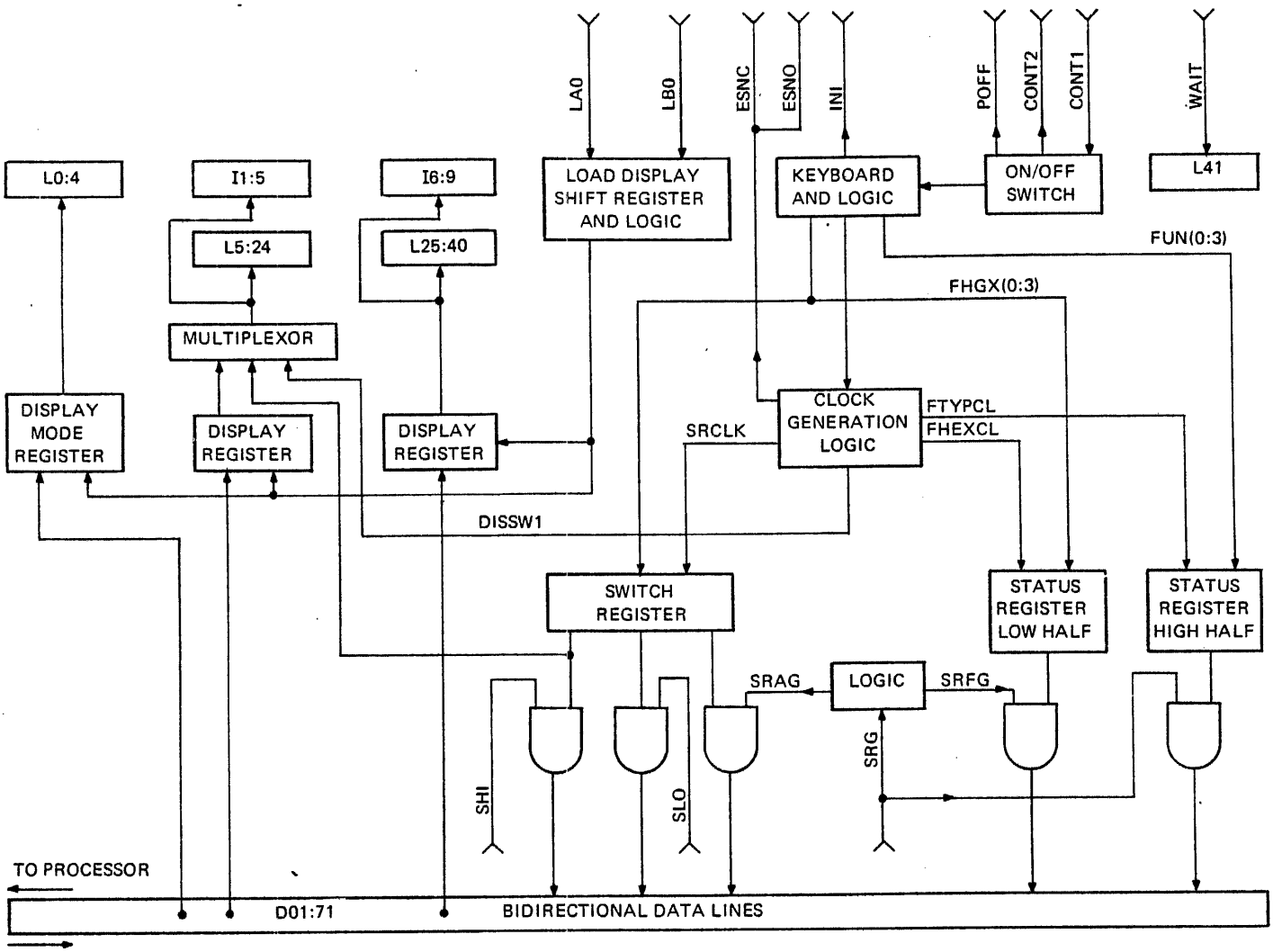


Figure 2. Hexadecimal Display Panel Block Diagram

3.3 Matrix Encoding

The diode matrix is encoded to drive signals HEX01:31 to the hexadecimal equivalent of the respective key 0:F (HEX31 is the LSB) when it is depressed. Depressing any function key other than DTA causes FUN00:30 to yield the codes specified by Table 1.

TABLE 1. FUNCTION KEY ENCODING (FUN00:30)

Key Depressed	FUN00	FUN10	FUN20	FUN30
SGL	0	1	1	1
RUN	1	1	1	1
WRT	1	1	0	1
RD	1	0	1	1
ADD	1	0	0	1
REG	0	1	1	0
FLT	0	1	0	0
FN	0	1	1	1

3.4 Clocking

Depressing any keyboard key other than DTA or INI generates one of three types of clocks used by the Hexadecimal Display Panel logic. This is accomplished by a positive transition of signal KEY1 (2F8) whenever one of these keys is depressed. The one shot triggered by this transition (2G8) is used to allow a one to two millisecond interval for switch bounce to subside before triggering the second one shot STRB1 (2K8) which is used to generate one of the three clocks. Since contact bounce is likely to retrigger these one shots when a key is released, the occurrence of signal KEY1 (any key depressed), HKEY1 (2F9 a hexadecimal key depressed), or FKEY1 (2H7 a function key depressed) being true in coincedence with the one shot is used to derive the clocks.

3.5 Switch Register Clocks

The Switch Register is enabled for clocking by depressing the DTA key. This is accomplished by direct clearing the Switch Register Enable flip-flop (SRENB) (2L5) when DTA is depressed and ANDing the zero output of the flip-flop plus HKEY1 and STRB1 to drive the Switch Register Clock (SRCLK0) (2M7). This clock is disabled by setting SRENB with the occurrence of FKEY1 when any function key is depressed.

3.6 Status Register Clocks

Two different clocks are used to load the status register. FTYPCL0 (2M8) is generated whenever any function key other than DTA is depressed and is used to load FUN00:30 into one half of the status register. The second clock FHEXCL0 (2N8) is generated whenever a hexadecimal key is depressed if the previously depressed key was FN, REG, or FLT. In this case, the hexadecimal input would be the register number or function number desired and FHEXCL0 is used to clock HEX01:31 into the second half of the status register.

3.7 Processor Intervention

The logic of the display signals the Processor that a response is necessary to a console function by signal ESNC0 (2R7) and its compliment ESNO0 (2R7). These signals are complimentarily pulsed whenever a function key other than DTA, FN, REG, or FLT is depressed, or whenever a hexadecimal key is depressed following FN, REG, or FLT (the occurrence of FHEXCL0).

3.8 Switch Register Loading

The Switch Register (4B1, 4D1, 4G1, 4J1, and 4M1) is loaded with a hexadecimal character with the occurrence of each SRCLK0 as mentioned previously. Data is entered into the least significant character (4B1) from the switches (HEX01:31) and left shifted through the register with each clock. The register is cleared whenever the DTA key is depressed.

3.9 Status Register

The status register is loaded in two parts as described previously. One half is loaded from FUN00:30 when a Function (FN) key is depressed by the occurrence of FTYPCL0. The least significant bit of this register is re-circulated on SGL or RUN and the second LSB is re-circulated on SSL to conform to the status codes indicated in Table 2. The second half of the register is loaded from HEX01:31 with the occurrence of FHEXCL0. These registers are initialized by SCL 0 from the Processor.

TABLE 2. STATUS CODES

KEY	DL1	DL2	DL3	DL4	DL5	DL6	DL7	DL0
SGL	1	U	X	X	X	X	X	X
INITIALIZE	U	U	U	U	U	U	O	U
RUN	0	0	0	X	X	X	X	X
WRT	0	0	1	U	U	U	U	U
RD	0	1	0	U	U	U	U	U
ADR	0	1	1	U	A_1	A_2	A_3	A_4
REG n	1	0	0	1	n_1	n_2	n_3	n_4
FLT n	1	0	1	1	n_1	n_2	n_3	n_4
FN n	1	0	0	0	n_1	n_2	n_3	n_4

A = Most significant hexadecimal digit of Switch Register
U = Unspecified
X = Unchanged
n = Hexadecimal digit associated with function (see Section 6)

The display status is presented to the Processor on the data lines (DL01:71) for the duration of time that control signal SRG0 is at a logical zero level. The data presented for status is in accordance with Table 2.

3.10 Display Register Loading

The Hexadecimal Display Panel registers and displays five bytes of data transmitted from the Processor. Two control signals are transmitted from the Processor to direct the loading of these registers. LA0 (2K5) is a low active pulse which signifies that data is available on bi-directional Data Lines D01:71 and it is to be loaded into the least significant byte of the display register. LA0 is used to initialize a four bit shift register (2M4) to 1000_2 which is used to load subsequent bytes, and generate a load pulse LA1 which is used to load the data into the LSB of the display register (2B6 and 3E6). Four subsequent LB0 pulses sent from the Processor gates data from D01:71 into successive bytes of the display register (3G6 and 3J6, 4C5 and 4E5, 4G5 and 4K5, 4N5 and 3N2). This is accomplished as each LB0 pulse is inverted and gated as LDB1, LDC1, LDD1 and LDE1 (2N4) respectively as controlled by the sequencing shift register (2M4) which is right shifted with each LB0 pulse.

3.11 Display Indicators

The two least significant bytes of the display register are gated directly to LEDs L25:40 and the hexadecimal indicators I6:9 (Sheet 3). LEDs L5:24 and hexadecimal indicators I1:5 are used to display either the most significant bytes of the display registers or the Switch Register. These sets of registers are selected through the 2:1 multiplexors (4C6, 4E6, 4H6, 4K6 and 4N6) as determined by the state of the DISSW1 (2N6). DISSW1 is high whenever the Switch Register is enabled (SRENB1) or a hexadecimal key is depressed (HKEY1).

3.12 Processor Inputs

Data is gated to the Processor in response to control signals SHI0, SLO0 or SRG0. SLO0 gates the two least significant digits of the Switch Register onto the bi-directional Data Lines D01:71 (4C3 and 4C4). SHI0 gates the next two Switch Register digits onto the bi-directional Data Lines D01:71 (4H3 and 4K3). SRG0 causes the status register bits to be gated (3D4) as per Table 2. Note that either the most significant Switch Register character is gated (4N3) if DL11 is low or the hexadecimal portion of the status register if DL11 is high (3H4).

4. PROCESSOR INTERFACING

4.1 Processor Connector

Signals from the display are terminated at a 26-080F06 type connector per the following list:

SIGNAL	PIN	SIGNAL	PIN	*X1-X4	PIN
D01	109	LA0	203	X1	207
D11	110	LB0	114	X2	211
D21	111	SHI0	200	X3	210
D31	112	SLO0	206	X4	209
D41	202	WAIT1	102		
D51	204	SRG0	113		
D61	205	ESNC0	103		
D71	208	ESNO0	104		
POFF0	105	INIT0	101		
CONT1	DB1-C1 & 214	SSGL1	106		
CONT2	DB1-C2	GND	100-3		
CONT3	DB-C3 & 213	GND	108		
SCLR0	107	GND	212	twisted with 114	
		GND	201	twisted with 203	

*X1-X4 A1-8 leads to front terminal strip of chassis.

4.2 Timing

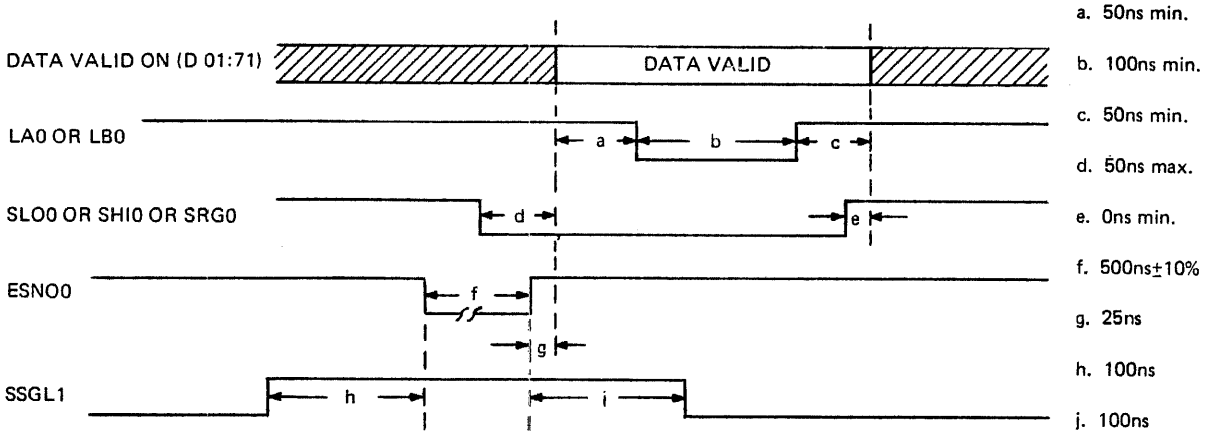


Figure 3. Hexadecimal Display Panel Timing

5. INSTALLATION PROCEDURE

The Hexadecimal Display Panel is connected to the Processor via a 17-305 cable. The 26-080F06 30-pin connector of the Hexadecimal Display Panel plugs into the mating connector as shown in Figures 4, 5 and 6.

CNTL1, CNTL2, P5, GND, LGND, +L jumpers go to corresponding lugs on the Processor chassis display terminal strip as shown in Figure 4.

6. POWER

The Hexadecimal Display Panel draws its power from the P5 and +L lugs on the Processor chassis display terminal strip. See Figure 4.

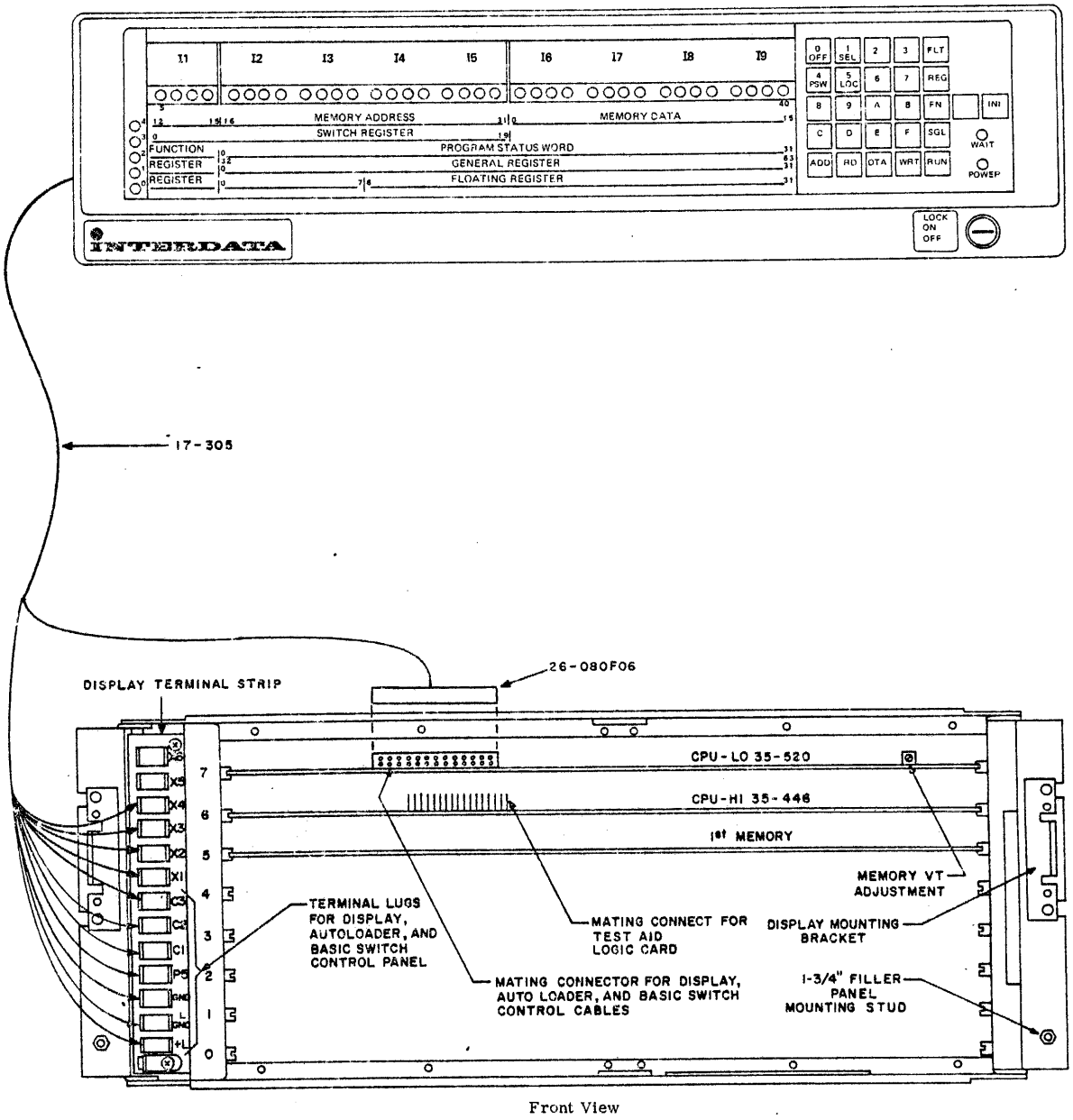
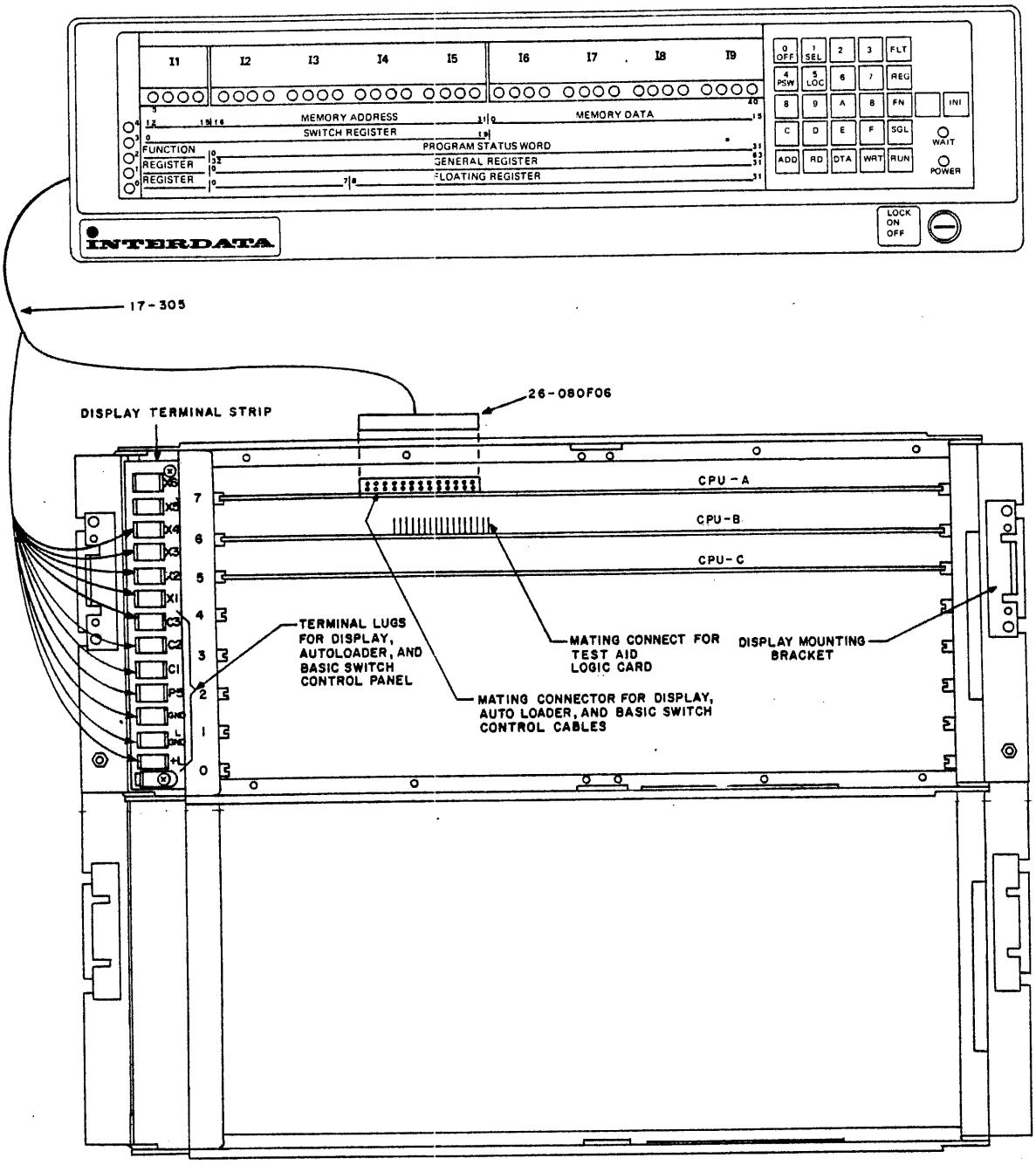
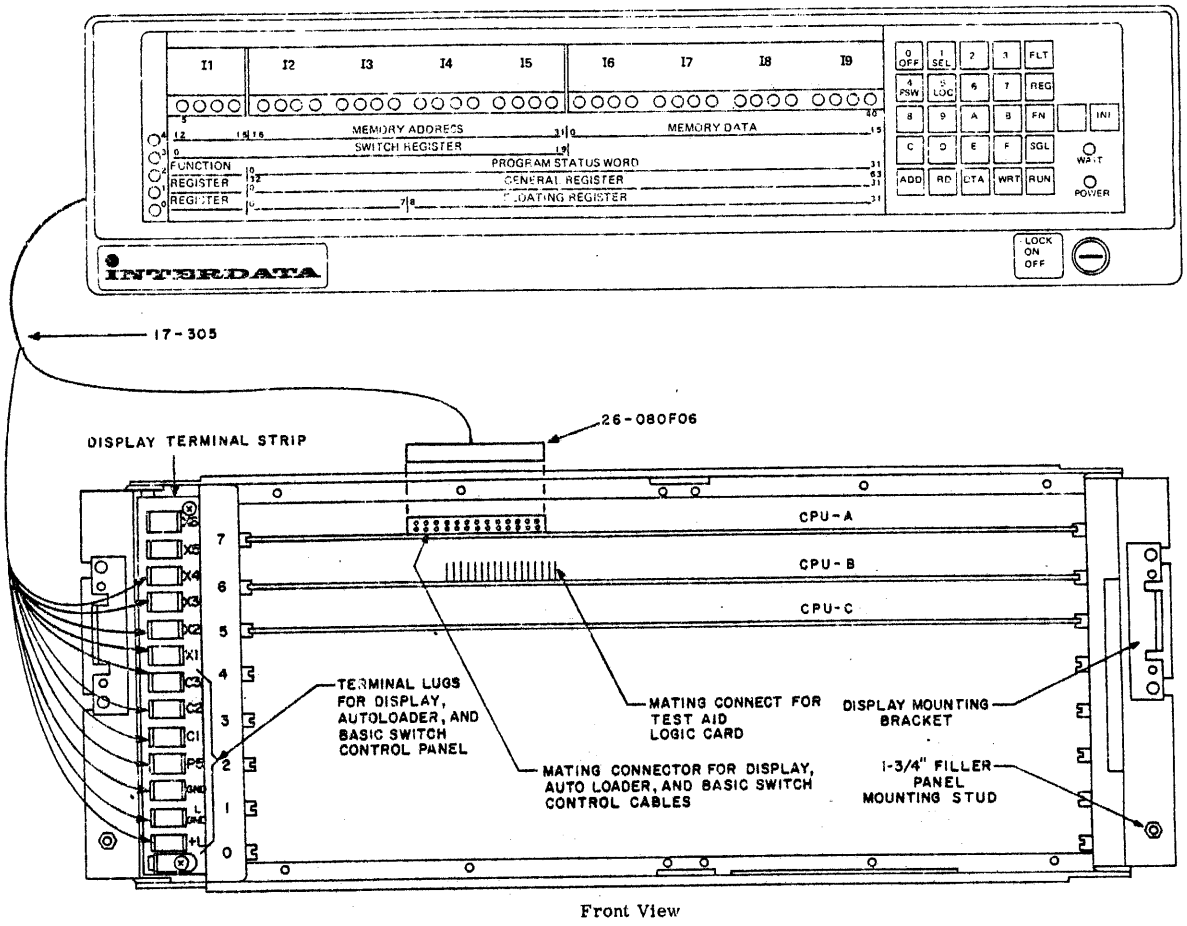


Figure 4. 7/16 Basic Display Installation



7/16 HSALU OR 7/32 TWIN CHASSIS INSTALLATION

Figure 5. Model 7/16 HSALU or 7/32 Installation



Front View

7/16 HSALU INSTALLATION

Figure 6. Model 7/16 HSALU Installation 7" Chassis

7. MNEMONICS

The following list provides a brief description of each mnemonic found in the Hexadecimal Display Panel. The source of each signal on Functional Schematic 09-065D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
CONT1	12 VAC to turn on power supply	2L1
CONT2	12 VAC to turn off power supply	2M1
DISSW1	Controls Display Multiplexors for L5:24	2R6
ESNC0	Execute switch normally open	2R7
ESNO0	Execute switch normally closed	2R7
FTYPCL0	Function type status register clock	2N7
FHEXCL0	Hexadecimal type status register clock	2N8
FUN00:30	Encoded functional keys	Sheet 2
HEX01:31	Encoded hexadecimal keys	Sheet 2
INIT0	Initialize Processor	2H2
LA0	Low active signal from Processor which initializes the loading sequence and loads the least significant byte of the Hexadecimal Display Panel	2K5
LB0	Low active signal from Processor used to control loading of display registers by generating LDB1, LDC1, LDD1, LDE1	2L5
LDB1	Load display registers	2R3
LDC1		2R4
LDD1		2R4
LDE1	Loads display mode register and most significant hexadecimal digit of the display	2R4
POFF0	Early power OFF failure	2K1
SCLR0	System Clear, initialize status registers	3J1
SDA0	DTA key depressed	2J2
SHI0	Switch Register high half gate command	2M2
SLO0	Switch Register low half gate command	2L3
SOR0	SGL or RUN keys depressed	2K2
SRAG1	Switch Register most significant hexadecimal digit gate command	2R2
SRCLK0	Switch Register clock	2M7
SRFG1	Status Register Function high half gate command	2R2
SRG1	Status Register low half gate command	2M2
SSL1	SGL key depressed	2J6
WAIT1	Wait light control	2M6

PROG= M8.16 ASSEMBLED BY MICROCAL II (32-BIT)

```
                                    1          SCRAT                                                                  8160003
                                    2          CROSS                                                                  8160004
                                    3          SQCHK                                                                  8160004
                                    4  * COPYRIGHT INTERDATA INC.  SEPTEMBER, 1976                                    8160005
                                    5  *                                                                              8160006
                                    6  * DHEMA MAHAJAN                                                               8160007
                                    7  *                                                                              8160008
                                    8  *                                                                              8160009
                                    9  * THE MICROCODE IS CONTAINED IN THE FOLLOWING 512 X 8 (4K) ROM CHIPS           8160010
                                   10  *                                                                              8160011
                                   11          PARTS 19-186R00F21,19-186R00F22,19-186R00F23                           8160012
                                   12          PARTS 19-186R00F24,19-186R00F25,19-186R00F26                           8160013
                                   13  *                                                                              8160014
                                   14  *                                                                              8160015
                                   15  *                                                                              8160016
                                   16  *                                                                              8160017
                                   17  *  LOCATION EQUATES                                                           8160018
                                   18  *                                                                              8160019
                                   19  *                                                                              8160020
0022                               20  PNTR     EQU   '22'                                                           8160021
0024                               21  APSW     EQU   '24'                                                           8160022
0026                               22  ALOC     EQU   '26'                                                           8160023
0030                               23  ILGPSW   EQU   '30'                                                           8160024
0038                               24  OMMPSW   EQU   '38'                                                           8160025
0040                               25  OIPSW    EQU   '40'                                                           8160026
                                   26  *                                                                              8160027
                                   27  *                                                                              8160028
                                   28  * INSTRUCTION READ IS IN PROGRESS                                             8160029
                                   29  * LOC IS INCREMENTED BY 2 & JAMMED IN MAR                                     8160030
                                   30  *                                                                              8160031
                                   31  *                                                                              8160032
000    84 8197                     32  START    BT    ATN+CATN+SNGL+MALF,HELP IF ANY INT., GO TO HELP                  8160033
001    E0 4400                     33  START1   L     MR0&Q,YS,D1          VECTOR THRU DROM1,                      8160034
                                   34  *                                   INITIATE MEMORY READ,                    8160035
                                   35  *                                   IF RR OR SF, SUPRESS MEMORY READ         8160036
                                   36  *                                                                            8160037
                                   37  *                                                                            8160038
                                   38  * COMMON RS                                                                  8160039
                                   39  *                                                                            8160040
                                   40  *                                                                            8160041
002    A4 DC0A                     41  RS       BF    AMOD,RSNX                                                     8160042
003    24 6440                     42           A     MR0,Q,MDR,D2         (MR0) = A+(X2)  VECTOR THRU DROM2        8160043
                                   43  *                                                                            8160044
                                   44  *                                                                            8160045
                                   45  * RX TYPE I/O INSTRUCTIONS                                                   8160046
                                   46  *                                                                            8160047
                                   47  *                                                                            8160048
                                   48  * COME HERE THRU DROM1                                                       8160049
                                   49  *                                                                            8160050
004    0C 7071                     50  AI       ACK   YD                   GET INTERRUPTING DEV ADR IN R1           8160051
                                   51  *                                                                            8160052
                                   52  * COME HERE THRU DROM1 FOR RD, WD, RH, WH, SS & OC                          8160053
                                   53  *                                                                            8160054
005    04 3E01                     54  IORX     ADR   YD                   ADDRESS THE DEVICE                       8160055
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                        55  *                                                                                  8160056
                        56  *                                                                                  8160057
                        57  *                                                                                  8160058
                        58  * COMMON RX                                                                        8160059
                        59  *                                                                                  8160060
                        60  *                                                                                  8160061
006     A4 DC08         61  RX        BF    AMOD,RXNX                                                        8160062
007     04 6840         62            A     MDR,Q,MDR                                                        8160063
008     04 7A40         63  RXNX      L     MAR,MDR                                                          8160064
009     40 7102         64            LI    Q,2,MR                                                           8160065
00A     24 7440         65  RSNX      L     MR0,MDR,D2          (MR0) = SECOND OPERAND                       8160066
                        66  *                                                                                  8160067
                        67  * COME HERE THRU DROM1 FOR AL                                                     8160068
                        68  *                                                                                  8160069
00B     A4 3F0E         69  AL        B     AL1                                                              8160070
                        70  *                                                                                  8160071
                        71  * COME HERE THRU DROM1 FOR  LM ,STM                                              8160072
                        72  *                           LME,STME                                             8160073
                        73  *                           LMD,STMD                                             8160074
                        74  *                                                                                  8160075
                        75  *                                                                                  8160076
                        76  *                                                                                  8160077
00C     A4 DC0E         77  LMSTM     BF    AMOD,LMNX                                                        8160078
00D     04 6840         78            A     MDR,Q,MDR                                                        8160079
00E     04 7A40         79  LMNX      L     MAR,MDR             (MAR) = EFFECTIVE 2ND OPERAND                8160080
                        80  *                                                                                  8160081
00F     00 710F         81            LI    Q,15                                                             8160082
010     04 E460         82            S     MR0,Q,YDI           (MR0) = COMPLEMENT OF YD FIELD               8160083
011     20 7102         83            LI    Q,2,D2                                                           8160084
                        84  *                                                                                  8160085
                        85  * COME HERE THRU DROM1 FOR BXH, BXLE                                             8160086
                        86  *                                                                                  8160087
012     A4 DC14         87  BX        BF    AMOD,BXNX                                                        8160088
013     04 6840         88            A     MDR,Q,MDR           (MDR) = A + (X2)                             8160089
014     04 3402         89  BXNX      L     MR0,YDP1            (MR0) = (R1) = START INDEX                   8160090
015     04 5423         90            A     MR0,YDM1,MR0        (MR0) = INCREMENTED OR                       8160091
                        91  *                                          DECREMENTED INDEX                     8160092
016     0C 7022         92            L     YDP1,MR0                                                         8160093
017     2C 3002         93            L     YDP1,YD,D2          BUMP YD FIELD                                8160094
                        94  *                                                                                  8160095
                        95  *                                                                                  8160096
                        96  * INPUT / OUTPUT INSTRUCTIONS                                                     8160097
                        97  *                                                                                  8160098
                        98  *                                                                                  8160099
                        99  * COME HERE THRU DROM2                                                           8160100
                       100  *                                                                                  8160101
018     04 78F4        101  RD        RD    MDR,CS              READ A BYTE                                  8160102
019     60 2000        102  RD2       L     Q,Q,MW              WRITE A BYTE/HW INTO MEMORY                  8160103
01A     C0 2000        103            L     Q,Q,IR                                                           8160104
                       104  *                                                                                  8160105
                       105  * COME HERE THRU DROM2                                                           8160106
                       106  *                                                                                  8160107
01B     00 7100        107  RH        LI    Q,0                                                              8160108
01C     84 EC1E        108            BT    HW,RHH              FOR HW DEVICE, GO TO RHH                     8160109
01D     00 70F4        109            RD    Q,CS                (Q 0:7)    = MS BYTE                         8160110
01E     04 7874        110  RHH       RD    MDR                 (MDR 8:15) = LS BYTE                         8160111
```

```
01F    04 6840                      A      MDR,Q,MDR
020    A4 3C19                      B      RD2
                       *
                       * COME HERE THRU DROM2
                       *
021    84 EC23         RHR          BT     HW,RDR                FOR HW DEVICE, GO TO RDR
022    00 70F4                      RD     Q,CS                  (Q 0:7) = MS BYTE
                       *
                       * COME HERE THRU DROM2 FOR RDR
                       *
023    04 7474         RDR          RD     MR0
024    CC 6220                      A      YS,Q,MR0,IR
                       *
                       * COME HERE THRU DROM2 FOR WH & WHR
                       *
025    84 EC27         WHR          BT     HW,WDR                FOR HW DEVICE, GO TO WDR
026    04 7EA4                      WD     MR0,CS
                       *
                       * COME HERE THRU DROM2 FOR WDR
                       *
027    04 7E24         WDR          WD     MR0                   WRITE A BYTE/HW TO DEVICE
028    C0 2000                      L      Q,Q,IR
                       *
                       * COME HERE THRU DROM2 FOR SS & AI
                       *
029    04 78F2         SS           SS     MDR,CS                SENSE STATUS INTO MDR
02A    04 7CC0                      L      FLR,MDR,CS
02B    A4 3C19                      B      RD2
                       *
                       * COME HERE THRU DROM2 FOR SSR & AIR
                       *
02C    0C 7272         SSR          SS     YS                    SENSE STATUS INTO R2
02D    C4 4C00                      L      FLR,YS,IR
                       *
                       * COME HERE THRU DROM2
                       *
02E    04 74C0         OC           L      MR0,MDR,CS            (MR0 7:15) = COMMAND BYTE
                       *
                       * COME HERE THRU DROM2 FOR OCR
                       *
02F    04 7E22         OCR          OC     MR0                   (MR0 7:15) = COMMAND
030    00 2000                      L      Q,Q                   DELAY
031    00 2000                      L      Q,Q
032    00 2000                      L      Q,Q
033    C0 2000                      L      Q,Q,IR
                       *
                       *
                       * COME HERE THRU DROM1 FOR RB & WB
                       *
                       *
034    04 3E01         RBWB         ADR    YD
035    04 7A40                      L      MAR,MDR               (MAR) = A
036    A4 DC68                      BF     AMOD,RBWBNX
037    04 6A40                      A      MAR,Q,MDR             (MAR) = A + (X2)
038    44 7A55         RBWBNX       INC    MAR,MAR,MR
039    04 7A55                      INC    MAR,MAR
```

```
03A  00 7040  167          L     Q,MDR              (Q) = BLOCK START ADDRESS          8160168
03B  44 2A00  168          L     MAR,Q,MR           (MAR) = BLOCK START ADDRESS        8160169
              169  *                                (MDR) = BLOCK END ADDRESS          8160170
03C  A4 3EE5  170          B     BLKIO1                                                8160171
              171  *                                                                   8160172
              172  *                                                                   8160173
              173  *                                                                   8160174
              174  * SHIFT / ROTATE INSTRUCTIONS                                       8160175
              175  *                                                                   8160176
              176  *                                                                   8160177
              177  * COME HERE FROM D1 FOR SRHL, SLHL                                  8160178
              178  *                                                                   8160179
03D  04 7B0F  179  SLHL  LI    MAR,15                                                 8160180
03E  04 7500  180  SLHL2 LI    MR0,0              (MR0) = 0 FOR LOGICAL SHIFTS/ROTATES 8160181
03F  04 7D00  181  SLHL3 LI    FLR,0                                                  8160182
              182  *                                                                   8160183
040  A4 0C42  183          BF    AMOD,SLHLNX                                           8160184
041  04 6840  184          A     MDR,Q,MDR                                             8160185
042  00 7052  185  SLHLNX L     Q,MAR,YDP1         (Q) = SHIFT / ROTATE MASK          8160186
              186  *                                BUMP YD FIELD                      8160187
043  06 684C  187          N     MDR Q,MDR,F        (MDR) = SHIFT / ROTATE COUNT = 0&31 8160188
              188  *                                (YD) = (R1)                        8160189
044  00 3003  189          L     Q,YDM1             (Q) = (R1+1)                       8160190
045  A4 34E6  190          BF    6,SHIFT0           ABORT IF COUNT = 0                 8160191
046  24 7D00  191  THRUD2 LI    FLR,0,D2                                               8160192
              192  *                                                                   8160193
              193  * COME HERE FROM D1 FOR SRHA, SLHA                                 8160194
              194  *                                                                   8160195
047  04 7B0F  195  SLHA  LI    MAR,15                                                 8160196
048  0C 300C  196  SLHA1 L     YD,YD,F                                                8160197
049  A4 383E  197          BF    L,SLHL2                                               8160198
04A  04 7580  198          LI    MR0,'80'                                              8160199
04B  04 74A0  199          EXB   MR0,MR0            (MR000) = SIGN BIT                 8160200
04C  A4 3C3F  200          B     SLHL3                                                 8160201
              201  *                                                                   8160202
              202  * COME HERE FROM D1 FOR SRA, SLA                                   8160203
              203  *                                                                   8160204
04D  04 7B1F  204  SLA   LI    MAR,31                                                 8160205
04E  A4 3C48  205          B     SLHA1                                                 8160206
              206  *                                                                   8160207
              207  * COME HERE FROM D1 FOR RRL, RLL, SRL, SLL                         8160208
              208  *                                                                   8160209
04F  04 7B1F  209  SLL   LI    MAR,31                                                 8160210
050  A4 3C3E  210          B     SLHL2                                                 8160211
              211  *                                                                   8160212
              212  * COME HERE FROM D2 FOR SLLS, SLHL                                 8160213
              213  *                                                                   8160214
051  04 7640  214  SLHLD2 L     CNTR,MDR                                               8160215
052  1C 300A  215          L     YD,YD,SL+C0        SET C FLAG                         8160216
053  CC 300C  216          L     YD,YD,F+IR         SET CC                             8160217
              217  *                                                                   8160218
              218  *                                                                   8160219
              219  *                                                                   8160220
054  04 7640  220  SLLD2 L     CNTR,MDR                                               8160221
055  18 300A  221          L     YD&Q,YD,SL+C0                                         8160222
056  0C 3002  222  SLL1D2 L     YD,YDP1            TO INCREASE YD FIELD               8160223
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057  0C 200C  223                L     YD,Q,F                                          8160224
058  0C 3003  224                L     YDM1,YD                                         8160225
059  CD D02C  225                O     YD,YD,MR0,F+IR      OR IN SIGN BIT, SET CC      8160226
               226  *                                                                 8160227
               227  *                                                                 8160228
               228  *                                                                 8160229
05A  04 7640  229  RLLD2  L     CNTR,MDR                                              8160230
05B  16 3009  230          L     YD&Q,YD,SL+CI                                         8160231
05C  A4 3C56  231          B     SLL1D2                                                8160232
               232  *                                                                 8160233
               233  *                                                                 8160234
               234  *                                                                 8160235
05D  04 7645  235  SLHAD2  INC   CNTR,MDR        (MDR) = SHIFT COUNT                 8160236
05E  1C 300A  236          L     YD,YD,SL+CO     SET C                               8160237
05F  14 3000  237          L     YD,YD,SR                                            8160238
060  CD D02C  238          O     YD,YD,MR0,F+IR  SET CC                              8160239
               239  *                                                                 8160240
               240  * COME HERE THRU DROM2 FOR SRHA                                  8160241
               241  *                                                                 8160242
061  0C 300C  242  SRHAD2  L     YD,YD,F                                             8160243
062  03 F100  243          INVI  Q,0             (Q) = 'FFFF'                        8160244
063  84 3865  244          BT    L,SRHL1                                             8160245
               245  *                                                                 8160246
               246  * COME HERE THRU DROM2 FOR SRLS & SRHL                          8160247
               247  *                                                                 8160248
064  00 7D00  248  SRHLD2  LI    FLR&Q,0                                             8160249
065  04 7640  249  SRHL1   L     CNTR,MDR                                            8160250
066  14 300B  250          L     YD,YD,SR+CI+CO                                      8160251
067  CC 300C  251  NLONG   L     YD,YD,F+IR      SET CC                              8160252
               252  *                                                                 8160253
               253  *                                                                 8160254
               254  *                                                                 8160255
068  04 7640  255  SRLD2   L     CNTR,MDR                                            8160256
069  10 300A  256  SRL1D2  L     YD&Q,YD,SR+CO                                       8160257
06A  A4 3C56  257          B     SLL1D2                                              8160258
               258  *                                                                 8160259
               259  *                                                                 8160260
               260  *                                                                 8160261
06B  04 7640  261  RRLD2   L     CNTR,MDR                                            8160262
06C  10 3009  262          L     YD&Q,YD,SR+CI                                       8160263
06D  A4 3C56  263          B     SLL1D2                                              8160264
               264  *                                                                 8160265
               265  * COME HERE THRU DROM2 FOR SRA                                   8160266
               266  *                                                                 8160267
06F  05 7845  267  SRAD2   DEC   MDR,MDR           (MDR) = SHIFT COUNT - 1 (0:30)    8160268
06F  04 784C  268          L     MDR,MDR,F                                           8160269
070  A4 3469  269          BF    6,SRL1D2          GO DO LAST SHIFT                  8160270
071  10 3000  270          L     YD&Q,YD,SR        SHIFT RIGHT R1 & R1+1 ONCE        8160271
072  0D D020  271          O     YD,YD,MR0         OR IN SIGN BIT                    8160272
073  24 7D00  272          LI    FLR,0,D2          LOOP THRU D2                      8160273
               273  *                                                                 8160274
               274  *                                                                 8160275
               275  *                                                                 8160276
074  04 7640  276  SLAD2   L     CNTR,MDR                                            8160277
075  18 3000  277          L     YD&Q,YD,SL                                          8160278
076  18 300A  278          L     YD&Q,YD,SL+CO   SET C                               8160279
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077  10 3000  279            L     YD&Q,YD,SR                                  8160280
078  A4 3C56  280            B     SLL1D2                                      8160281
               281  *                                                         8160282
               282  * COME HERE THRU DROM1 FOR : LE,CE,AE,SE,ME,DE            8160283
               283  *                          : LD,CD,AD,SD,MD,DD            8160284
               284  *                                                         8160285
079  A4 3EA5  285  FRX     B     FRXD1                                       8160286
               286  *                                                         8160287
               287  * COME HERE THRU DROM1 FOR : STE,STD                     8160288
               288  *                                                         8160289
07A  A4 0C7C  289  STE,STD  BF    AMOD,STENX                                  8160290
07B  04 6840  290            A     MDR,Q,MDR                                   8160291
07C  04 7A40  291  STENX    L     MAR,MDR       (MAR) = EFFECTIVE 2ND OPERAND 8160292
07D  20 7102  292            LI    Q,2,D2                                      8160293
               293  *                                                         8160294
               294  * COME HERE FOR ATL,ABL  (D1)                            8160295
               295  *                                                         8160296
07E  A4 3E51  296  ATLABL   B     ATLABLD1                                    8160297
               297  *                                                         8160298
               298  * COME HERE FOR RTL,RBL  (D1)                           8160299
               299  *                                                         8160300
07F  A4 3E6D  300  RTLRBL   B     RTLRBLD1                                    8160301
               301  *                                                         8160302
               302  * COME HERE THRU DROM2                                   8160303
               303  *                                                         8160304
080  00 3000  304  SINT     L     Q,YD          SAVE YD IN Q.                 8160305
081  0C 71FF  305            LI    YD,'FF'       (MR0) = 2ND OPERAND = DEV ADR 8160306
082  1E 5020  306            N     YD,YD,MR0,SL  (YD) = 2 X DEV ADR            8160307
083  A4 3DE0  307            B     SINT1                                       8160308
               308  *                                                         8160309
               309  * COME HERE THRU D2 FOR : STH                            8160310
               310  *                                                         8160311
084  04 7A20  311  STH      L     MAR,MR0       (MAR) = EFFCTIVE 2ND OPERAND  8160312
085  04 3800  312            L     MDR,YD        (MDR) = (R1)                  8160313
086  60 2000  313  STH2     L     Q,Q,MW        WRITE HW TO MEMORY            8160314
087  C4 7C00  314            L     FLR,PSW,IR                                  8160315
               315  *                                                         8160316
               316  *                                                         8160317
               317  *                                                         8160318
088  04 584E  318  AHM      A     MDR,YD,MDR,F+CO  SET FLAGS                  8160319
089  A4 3C19  319            B     RD2                                         8160320
               320  *                                                         8160321
               321  * COME HERE THRU DROM2                                   8160322
               322  *                                                         8160323
08A  C2 502C  323  THI      N     Q,YD,MR0,F+IR                               8160324
               324  *                                                         8160325
               325  *                                                         8160326
               326  * COME HERE THRU D2 FOR  :  LMD                          8160327
               327  *                                                         8160328
08B  A4 3E8B  328  LMD      B     LMDD2                                       8160329
               329  *                                                         8160330
               330  * COME THER THRU DROM1 FOR LIS, AIS & SIS                8160331
               331  *                                                         8160332
08C  24 7480  332  IMM      L     MR0,YSI,D2                                  8160333
               333  *                                                         8160334
               334  * COME HERE FOR ACHR (D1) & ACH (D2)                     8160335
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                        335     *                                                                       8160336
                        336     ACH     L       FLR,PSW                 GET OLD CC IN FLR               8160337
                        337     *                                                                       8160338
                        338     * COMMON AHR (D1) & AH, AHI, AIS (D2)                                  8160339
                        339     *                                                                       8160340
08E     CC 502F         340     AHR     A       YD,YD,MR0,CI+CO+F+IR                                    8160341
                        341     *                                                                       8160342
                        342     * COME HERE FOR SCHR (D1) & SCH (D2)                                   8160343
                        343     *                                                                       8160344
08F     04 7C00         344     SCH     L       FLR,PSW                 GET OLD CC IN FLR               8160345
                        345     *                                                                       8160346
                        346     * COMMON SHR (D1) & SH, SHI,SIS (D2)                                   8160347
                        347     *                                                                       8160348
090     CC D02F         348     SHR     S       YD,YD,MR0,CI+CO+F+IR                                    8160349
                        349     *                                                                       8160350
                        350     * COME HERE THRU D2 FOR .: LME                                         8160351
                        351     *                                                                       8160352
091     A4 3E91         352     LME     B       LMED2                                                   8160353
                        353     *                                                                       8160354
                        354     *  COMMON FOR NHR (D1) & NH, NHI (D2)                                   8160355
                        355     *                                                                       8160356
092     CE 502C         356     NHR     N       YD,YD,MR0,F+IR                                          8160357
                        357     *                                                                       8160358
                        358     * COMMON OHR (D1) & OH, OHI (D2)                                       8160359
                        359     *                                                                       8160360
093     CD D02C         360     OHR     O       YD,YD,MR0,F+IR                                          8160361
                        361     *                                                                       8160362
                        362     * COMMON XHR (D1) & XH, XHI (D2)                                       8160363
                        363     *                                                                       8160364
094     CF 502C         364     XHR     X       YD,YD,MR0,F+IR                                          8160365
                        365     *                                                                       8160366
                        366     * COMMON LHR (D1) & LH, LHI, LIS (D2)                                  8160367
                        367     *                                                                       8160368
095     CC 702C         368     LHR     L       YD,MR0,F+IR                                             8160369
                        369     *                                                                       8160370
                        370     *                                                                       8160371
                        371     *                                                                       8160372
096     CC F03C         372     LCS     TCMP    YD,YSI,F+IR                                             8160373
                        373     *                                                                       8160374
                        374     * COMMON CHR (D1) & CH, CHI (D2)                                       8160375
                        375     *                                                                       8160376
097 - 03 502C           376     CHR     X       Q,YD,MR0,F              COMPARE SIGNS OF BOTH OPERANDS  8160377
098     64 3ADC         377             BT      L,DIFFER                IF DIFFERENT, GO TO DIFFER      8160378
                        378     *                                                                       8160379
                        379     * COMMON CLHR (D1) & CLH, CLHI (D2)                                    8160380
                        380     *                                                                       8160381
099     C0 D02E         381     CLHR    S       Q,YD,MR0,CO+F+IR                                        8160382
                        382     *                                                                       8160383
                        383     * COME HERE THRU D2 FOR  : STMD                                        8160384
                        384     *                                                                       8160385
09A     A4 3E9A         385     STMD    B       STMDD2                                                  8160386
                        386     *                                                                       8160387
                        387     *                                                                       8160388
                        388     *                                                                       8160389
                        389     *                                                                       8160390
                        390     * ILLEGAL INSTRUCTION OP-CODE DETECTED                                  8160391
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                        391   *
098  05 7215            392   ILEG    DEC   LOC,LOC          DECREMENT LOC BY 2          8160392
09C  04 7B30            393           LI    MAR,ILGPSW                                  8160393
09D  A4 3F21            394           B     GENSWP           SWAP PSW                   8160394
                        395   *                                                         8160395
                        396   * COME HERE THRU D2 FOR  :  STME                          8160396
                        397   *                                                         8160397
09E  A4 3E9E            398   STME    B     STMED2                                      8160398
                        399   *                                                         8160399
                        400   *                                                         8160400
                        401   *                                                         8160401
                        402   *  RR & RS BRANCHES                                       8160402
                        403   *                                                         8160403
                        404   *                                                         8160404
                        405   * COMMON BALR (D1) & BAL (D2)                            8160405
                        406   *                                                         8160406
09F  0C 7010            407   BALR    L     YD,LOC           (YD) = INCREMENTED LOC     8160407
0A0  04 7220            408   BRANCH  L     LOC,MR0                                     8160408
0A1  C4 7C00            409   NOB     L     FLR,PSW,IR                                  8160409
                        410   *                                                         8160410
                        411   * COMMON BTCR (D1) & BTC (D2)                            8160411
                        412   *                                                         8160412
0A2  84 5CA0            413   BTCR    BT    MSK,BRANCH                                  8160413
0A3  C4 7C00            414           L     FLR,PSW,IR                                  8160414
                        415   *                                                         8160415
                        416   * COMMON BFCR (D1) & BFC (D2)                            8160416
                        417   *                                                         8160417
0A4  A4 5CA0            418   BFCR    BF    MSK,BRANCH                                  8160418
0A5  C4 7C00            419           L     FLR,PSW,IR                                  8160419
                        420   *                                                         8160420
                        421   *                                                         8160421
                        422   * SHORT BRANCHES                                         8160422
                        423   *                                                         8160423
                        424   *                                                         8160424
                        425   * COMMON FOR BTBS, BTFS (D1)                             8160425
                        426   *                                                         8160426
0A6  84 5CA9            427   BTS     BT    MSK,SHORTB       IF ANY CONDITION TRUE, BRANCH 8160427
0A7  C4 7C00            428           L     FLR,PSW,IR                                  8160428
                        429   *                                                         8160429
                        430   * COMMON FOR BFBS, BFFS (D1)                             8160430
                        431   *                                                         8160431
0A8  84 5CA1            432   BFS     BT    MSK,NOB          IF ANY CONDITION TRUE, DON'T BRANCH 8160432
0A9  05 7215            433   SHORTB  DEC   LOC,LOC          DECREMENT LOC BY 2          8160433
0AA  00 7030            434           L     Q,YSI                                       8160434
0AB  20 6030            435           A     Q,Q,YSI,D2       (Q) = DISPLACEMENT IN # OF BYTES 8160435
                        436   *                                                         8160436
                        437   * COME HERE THRU DROM2 FOR BTBS, BFBS                    8160437
                        438   *                                                         8160438
0AC  01 2000            439   BKWORD  TCMP  Q,Q              GET TWO'S COMPLEMENT        8160439
                        440   *                                                         8160440
                        441   * COME HERE THRU DROM2 FOR BTFS, BFFS                    8160441
                        442   *                                                         8160442
0AD  04 6210            443   FRWORD  A     LOC,Q,LOC        INCREMENT OR DECREMENT LOC 8160443
0AE  C4 7C00            444           L     FLR,PSW,IR                                  8160444
                        445   *                                                         8160445
                        446   *                                                         8160446
                                                                                        8160447
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                         447   *  BRANCH ON INDEX INSTRUCTIONS                                                    8160448
                         448   *                                                                                 8160449
                         449   *                                                                                 8160450
                         450   * COME HERE THRU DROM2                                                           8160451
                         451   *                                                                                 8160452
0AF     01 5025          452   BXH       S     Q,MR0,YD,JAMCI&CO   (Q) = DECREMENTED INDEX - LIMIT - 1         8160453
0B0     A4 3CB2          453             B     BX1                                                             8160454
                         454   *                                                                                 8160455
                         455   * COME HERE THRU DROM2                                                           8160456
                         456   *                                                                                 8160457
0B1     00 D02A          457   BXLE      S     Q,YD,MR0,CO         (Q) = LIMIT - INCREMENTED INDEX             8160458
                         458   *                                                                                 8160459
0B2     84 1CB4          459   BX1       BT    C,BXNOB                                                         8160460
0B3     04 7240          460             L     LOC,MDR                                                         8160461
0B4     C4 7C00          461   BXNOB     L     FLR,PSW,IR                                                      8160462
                         462   *                                                                                 8160463
                         463   *                                                                                 8160464
                         464   * BYTE HANDLING INSTRUCTIONS                                                     8160465
                         465   *                                                                                 8160466
                         466   *                                                                                 8160467
                         467   *                                                                                 8160468
                         468   * COME HERE THRU DROM2 FOR LB                                                     8160469
                         469   *                                                                                 8160470
0B5     04 74C0          470   LB        L     MR0,MDR,CS          (MR0 7:15) = BYTE TO BE LOADED              8160471
                         471   *                                                                                 8160472
                         472   * COME HERE THRU DROM1 FOR LBR                                                    8160473
                         473   *                                                                                 8160474
0B6     0C 7020          474   LBR       L     YD,MR0                                                          8160475
0B7     0E 51FF          475             NI    YD,YD,'FF'          ISOLATE BYTE                                8160476
0B8     C4 7C00          476             L     FLR,PSW,IR                                                      8160477
                         477   *                                                                                 8160478
                         478   * COME HERE THRU DROM2                                                           8160479
                         479   *                                                                                 8160480
0B9     06 55FF          480   CLB       NI    MR0,YD,'FF'         (MR0) = LS BYTE OF 1ST OPERAND              8160481
0BA     00 71FF          481             LI    Q,'FF'                                                          8160482
0BB     02 60C0          482             N     Q,Q,MDR,CS          (Q) = LS BYTE OF 2ND OPERAND                8160483
0BC     C5 642E          483             S     MR0,MR0,Q,F+CO+IR   SET CC                                      8160484
                         484   *                                                                                 8160485
                         485   * COME HERE THRU DROM2                                                           8160486
                         486   *                                                                                 8160487
0BD     04 3400          487   STB       L     MR0,YD                                                          8160488
0BE     04 78A0          488             EXB   MDR,MR0                                                         8160489
0BF     A4 3C86          489             B     STH2                                                            8160490
                         490   *                                                                                 8160491
                         491   *                                                                                 8160492
                         492   *                                                                                 8160493
0C0     04 7820          493   STBR      L     MDR,MR0             (MDR) = SECOND OPERAND                      8160494
0C1     04 7801          494             LI    MAR,1               (MAR) = ODD                                 8160495
0C2     04 3400          495             L     MR0,YD              (MR0) = 1ST OPERAND                         8160496
0C3     04 78A0          496             EXB   MDR,MR0             GET LS BYTE FROM 1ST OPERAND                8160497
0C4     2C 7240          497             L     YS,MDR,D2           INSTRUCTION READ THRU DROM2                 8160498
                         498   *                                                                                 8160499
                         499   *                                                                                 8160500
                         500   *                                                                                 8160501
0C6     2C 70A0          501   EXBR      EXB   YD,MR0,D2           IR THRU DROM2                               8160502
                         502   *                                                                                 8160503
```

```
                     *                                                              8160504
                     *                                                              8160505
                     *                                                              8160506
                     *                                                              8160507
                     * COME HERE THRU DROM2                                         8160508
                     *                                                              8160509
0C6     84 1CA1      LM       BT     C,NOB                                          8160510
0C7     45 7425               DEC    MR0,MR0,MR        DECREMENT COUNT              8160511
0C8     04 6A50               A      MAR,Q,MAR                                      8160512
0C9     2C 7042               L      YDP1,MDR,D2       LOAD GENERAL REGISTER        8160513
                     *                                                              8160514
                     * COME HERE THRU DROM2                                         8160515
                     *                                                              8160516
0CA     04 3802      STM      L      MDR,YDP1                                       8160517
0CB     65 7425               DEC    MR0,MR0,MW        STORE GENERAL REGISTER INTO MEMORY 8160518
0CC     84 1CA1               BT     C,NOB                                          8160519
0CD     24 6A50               A      MAR,Q,MAR,D2      INCREMENT MAR, LOOP THRU D2  8160520
                     *                                                              8160521
                     * COME HERE THRU DROM2 FOR LPSW                                8160522
                     *                                                              8160523
0CE     04 3400      LPSW     L      MR0,YD            SAVE YD IN MR0               8160524
0CF     A4 3F2C               B      LPSW1                                          8160525
                     *                                                              8160526
                     * COME HERE THRU DROM1 FOR EPSR                                8160527
                     *                                                              8160528
0D0     04 7400      EPSR     L      MR0,PSW                                        8160529
0D1     0C 7020               L      YD,MR0            (YD) = OLD PSW               8160530
0D2     04 4000               L      PSW,YS            NEW PSW                      8160531
0D3     A4 3F30               B      EPSR1                                          8160532
                     *                                                              8160533
                     *                                                              8160534
                     * SHORT SHIFTS                                                 8160535
                     *                                                              8160536
                     *                                                              8160537
                     *                                                              8160538
                     *                                                              8160539
                     * COMMON FOR SRLS, SLLS (D1)                                   8160540
                     *                                                              8160541
0D4     04 783C      SLLS     L      MDR,YSI,F         (MDR) = SHIFT COUNT          8160542
0D5     84 3446               BT     G,THRUD2                                       8160543
0D6     CC 300C               L      YD,YD,F+IR        ABORT IF COUNT IS ZERO       8160544
                     *                                                              8160545
                     *                                                              8160546
                     * RR TYPE I/O INSTRUCTIONS                                     8160547
                     *                                                              8160548
                     *                                                              8160549
                     * COME HERE THRU DROM1 FOR AIR                                 8160550
                     *                                                              8160551
0D7     0C 7071      AIR      ACK    YD                GET INTERRUPTING DEV ADR IN R1 8160552
                     *                                                              8160553
                     * COMMON FOR RDR, WDR, RHR, WHR, SSR, OCR                      8160554
                     *                                                              8160555
0D8     04 3E01      IORR     ADR    YD                ADDRESS THE DEVICE           8160556
0D9     20 7100               LI     Q,0,D2            (Q) = 0                      8160557
                     *                                                              8160558
                     *                                                              8160559
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                                559     *  BLOCK I/O                                                                  8160560
                                560     *                                                                             8160561
                                561     *                                                                             8160562
                                562     * COME HERE FOR RBR, WBR                                                     8160563
                                563     *                                                                             8160564
0DA     A4 3EDF                 564     RBRWBR  B       RBRWBRD1                                                    8160565
                                565     *                                                                             8160566
                                566     *                                                                             8160567
                                567     *                                                                             8160568
                                568     * COME HERE THRU DROM1 FOR DHR; THRU DROM2 FOR DH                            8160569
                                569     *                                                                             8160570
0DB     A4 3E00                 570     DHR     B       DHR1                                                        8160571
                                571     *                                                                             8160572
                                572     * COME HERE THRU DROM1 FOR MHR; THRU DROM2 FOR MH                            8160573
                                573     *                                                                             8160574
0DC     A4 3E32                 574     MHR     B       MHR1                                                        8160575
                                575     *                                                                             8160576
                                576     * COME HERE THRU DROM1 FOR MHUR; THRU DROM2 FOR MHU                          8160577
                                577     *                                                                             8160578
0DD     A4 3E48                 578     MHUR    B       MHUR1                                                       8160579
                                579     *                                                                             8160580
                                580     * COME HERE THRU D1 FOR : FXR,FXDR                                           8160581
                                581     *                                                                             8160582
0DE     A4 3EC9                 582     FXR     B       FXRD1                                                       8160583
                                583     *                                                                             8160584
                                584     * COME HERE THRU D1 FOR : FLR,FLDR                                           8160585
                                585     *                                                                             8160586
0DF     A4 3ECD                 586     FLR     B       FLRD1                                                       8160587
                                587     *                                                                             8160588
                                588     * COME HERE THRU D1 FOR : LER,AER,SER,MER,DER                                8160589
                                589     *                       : LDR,ADR,SDR,MDR,DDR                               8160590
                                590     *                                                                             8160591
0E0     A4 3EC6                 591     FRR     B       FRRD1                                                       8160592
                                592     *                                                                             8160593
                                593     * COME HERE THRU D1 FOR : CER,CDR                                            8160594
                                594     *                                                                             8160595
0E1     A4 3E8E                 595     CER     B       CERD1                                                       8160596
                                596     *                                                                             8160597
                                597     * COME HERE THRU DROM2 FOR STE                                              8160598
                                598     *                                                                             8160599
0E2     A4 3E83                 599     STE     B       STED2                                                       8160600
                                600     *                                                                             8160601
                                601     * COME HERE THRU DROM2 FOR STD                                              8160602
                                602     *                                                                             8160603
0E3     A4 3EAF                 603     STD     B       STDD2                                                       8160604
                                604     *                                                                             8160605
                                605     * COME HERE THRU DROM2                                                      8160606
                                606     *                                                                             8160607
0E4     04 7EC4                 607     WD      WD      MDR,CS                  WRITE A BYTE                        8160608
0E5     C0 2000                 608             L       Q,C,IR                                                      8160609
                                609     *                                                                             8160610
                                610     * SHIFT COUNT FOUND TO BE ZERO                                              8160611
                                611     *                                                                             8160612
0E6     04 3600                 612     SHIFT0  L       MDR,YD                  SAVE YD IN MDR                      8160613
0E7     0C 7110                 613             LI      YD,16                                                       8160614
0E8     0E 505C                 614             N       YD,YD,MAR,F             SEE IF LONG SHIFTS                  8160615
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0E9   0C 7040   615          L    YD,MDR          RESTORE YD                    8160616
0EA   A4 3467   616          BF   G,NLONG                                      8160617
0EB   04 7D00   617          LI   FLR,0           YES, CLEAR FLR                8160618
0EC   A4 3C56   618          B    SLL1D2          GO SET CC                     8160619
                619  *                                                         8160620
                620  * ROUTINE FOR SVC   (D2)                                 8160621
                621  *                                                         8160622
0ED   04 7820   622  SVCD2   L    MDR,MR0         (MDR) = SECOND OPERAND        8160623
0EE   04 7894   623          LI   MAR,'94'                                     8160624
0EF   64 7896   624          LI   MAR,'96',MW     WRITE IT @ X'94'              8160625
0F0   04 7800   625          L    MDR,PSW                                      8160626
0F1   64 7B98   626          LI   MAR,'98',MW     WRITE OLD PSW @ X'96'         8160627
0F2   04 7810   627          L    MDR,LOC                                      8160628
0F3   64 7B9A   628          LI   MAR,'9A',MW     WRITE OLD LOC @ X'98'         8160629
                629  *                                                         8160630
0F4   00 7460   630          L    MR0&Q,YDI                                    8160631
0F5   40 6020   631          A    Q,Q,MR0,MR      READ NEW PSW FROM X'9A'       8160632
0F6   04 6B9C   632          AI   MAR,Q,'9C'       (MAR) = '9C' + 2(YDI)         8160633
0F7   04 7040   633          L    PSW,MDR         NEW PSW                       8160634
0F8   40 2000   634          L    Q,Q,MR                                       8160635
0F9   04 7240   635          L    LOC,MDR         NEW LOC                       8160636
0FA   C4 7C00   636          L    FLR,PSW,IR                                   8160637
                637  *                                                         8160638
                638  *                                                         8160639
0FB   04 7D00   639  FINISH  LI   FLR,0                                        8160640
0FC   C0 2000   640  TERMIN  L    Q,Q,IR                                       8160641
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```
0FD                         ORG     '100'
                 *
                 *
                 * ON POWER UP, '100' IS JAMMED INTO RAR
                 *
                 *
100   00 7102    PWRUP      LI      Q,2                 'HW' ACTIVE ON POWER UP IF
101   84 EF00               BT      HW,ALO1             ALO IS IN THE SYSTEM
                 *
                 *
                 * ALO IS NOT HOOKED UP IN THE SYSTEM
                 *
102   04 7824               LI      MAR,APSW
103   44 7826               LI      MAR,ALOC,MR
104   04 7041               L       PSW,MDR,CYD&SWA     LOAD PSW, CLEAR YD FIELD
105   44 750F               LI      MRO,15,MR
106   04 7240               L       LOC,MDR             LOAD LOC
107   04 7B22               LI      MAR,PNTR
108   40 2000               L       Q,Q,MR
109   04 7A40               L       MAR,MDR
10A   45 7425    LDREG      DEC     MRO,MRO,MR
10B   0C 7042               L       YDP1,MDR            LOAD GENERAL REGISTER
10C   04 6A50               A       MAR,Q,MAR           INCREMENT MAR BY 2
10D   A4 1D0A               BF      C,LDREG             LOOP TILL ALL REGISTERS ARE LOADED
                 *
                 * LOAD DOUBLE PRECISION FLOATING POINT REGISTERS, IF EQUIPPED
                 *
10E   A4 7919               BF      DPFP,PWRUP2         BRANCH IF NOT EQUIPPED
10F   04 757F               LI      MRO,'7F'
110   04 74A7               EXB     MRO,MRO,FLTPT       SET UP OP-CODE FOR
111   04 7427               L       MRO,MRO,FLTPT       'LMD' IN FPP = '7F00'
112   04 753E               LI      MRO,62
113   44 6A50    LDDOUBLE   A       MAR,Q,MAR,MR
114   04 7847               L       MDR,MDR,FLTPT       SEND 16-BIT DATA TO FPP FOR DOUBLE
115   04 7847               L       MDR,MDR,FLTPT       PRECISION FLOATING POINT REGISTER
116   05 642A               S       MRO,MRO,Q,CO        DECREMENT COUNT BY 2
117   A4 1D13               BF      C,LDDOUBLE          LOOP TILL REG 14 IS SET UP
118   04 7471               ACK     MRO                 DUMMY ACKNOLEDGE FOR FPP TO IDLE
                 *
                 * LOAD SINGLE PRECISION FLOATING POINT REGISTERS, IF EQUIPPED
                 *
119   A4 7525    PWRUP2     BF      SPFP,PWRUP3         BRANCH IF NOT EQUIPPED
11A   04 7572               LI      MRO,'72'
11B   04 74A7               EXB     MRO,MRO,FLTPT       SET UP OP-CODE FOR
11C   04 7427               L       MRO,MRO,FLTPT       'LME' IN FPP = '7200'
11D   04 751E               LI      MRO,30
11E   04 7800               LI      MAR,0
11F   44 6A50    LDSINGLE   A       MAR,Q,MAR,MR
120   04 7847               L       MDR,MDR,FLTPT       SEND 16-BIT DATA TO FPP FOR SINGLE
121   04 7847               L       MDR,MDR,FLTPT       PRECISION FLOATING POINT REGISTER
122   05 642A               S       MRO,MRO,Q,CO
123   A4 1D1F               BF      C,LDSINGLE          LOOP TILL REG 14 IS SET UP
124   04 7471               ACK     MRO                 DUMMY ACKNOLEDGE FOR FPP TO IDLE
                 *
125   04 7501    PWRUP3     LI      MRO,1
126   04 7E21               ADR     MRO                 ADDRESS THE DISPLAY PANEL
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127  04 7B20   698            LI    MAR,'20'                                    8160699
128  40 3000   699            L     Q,YD,MR          SAVE YD IN Q FOR MMF       8160700
               700  *                                                          8160701
129  04 7C40   701            L     FLR,MDR          (FLR) = SAVED DISPLAY STATUS 0:3  8160702
12A  84 212C   702            BT    V+G+L,LOCDIS     IF WAS NOT IN RUN MODE, DISPLAY LOC  8160703
               703  *                                                          8160704
               704  * DISPLAY PANEL WAS IN RUN MODE                           8160705
               705  *                                                          8160706
12B  84 6D79   706            BT    ARST,MMF         IF PROCESSOR IS EQUIPPED WITH AN  8160707
               707  *                                AUTO-RESTANT OPTION, DO MMF PSW SWAP  8160708
12C  04 7410   708  LOCDIS    L     MR0,LOC          DISPLAY LOC IN D1 & D2     8160709
12D  04 7945   709            LI    MDR,'45'         INDICATE  FN 5             8160710
12E  04 7B00   710  MAR0      LI    MAR,0            DISPLAY 0   IN D3 & D4     8160711
               711  *                                                          8160712
12F  04 7E24   712  OUTDIS    WD    MR0              D1 = (MR0 8:15)            8160713
130  04 7EA4   713            WD    MR0,CS           D2 = (MR0 0:7)             8160714
131  04 7E54   714            WD    MAR              D3 = (MAR 8:15)            8160715
132  04 7ED4   715            WD    MAR,CS           D4 = (MAR 0:7)             8160716
133  04 7E44   716            WD    MDR              D5 = (MDR 8:15)            8160717
               717  *                                                          8160718
               718  *                                                          8160719
               719  * UN-INTERRUPTABLE IDLE LOOP                              8160720
               720  *                                                          8160721
134  00 2001   721  IDLE      L     Q,Q,CYD&SWA                                 8160722
135  00 3001   722            L     Q,YD,CYD&SWA     SAVE YD IN Q, WAIT LIGHT ON  8160723
136  84 AD5E   723  IDLE1     BT    CATN,IDLEX                                  8160724
137  A4 F536   724            BF    PPF,IDLE1                                   8160725
               725  *                                                          8160726
               726  *                                                          8160727
               727  *                                                          8160728
               728  * POWER IS GOING DOWN                                     8160729
               729  *                                                          8160730
138  04 7B24   730  PWRDWN    LI    MAR,APSW                                    8160731
139  04 7800   731            L     MDR,PSW                                     8160732
13A  64 7B26   732            LI    MAR,ALOC,MW      SAVE CURRENT PSW           8160733
13B  04 7810   733            L     MDR,LOC                                     8160734
13C  64 7B22   734            LI    MAR,PNTR,MW      SAVE CURRENT LOC           8160735
13D  44 750F   735            LI    MR0,15,MR                                   8160736
13E  04 7A41   736            L     MAR,MDR,CYD&SWA  (MAR) = REGISTER SAVE AREA START  8160737
13F  00 7102   737            LI    Q,2                                         8160738
140  04 3802   738  SAVREG    L     MDR,YDP1                                    8160739
141  65 7425   739            DEC   MR0,MR0,MW       SAVE GENERAL REGISTER      8160740
142  04 6A50   740            A     MAR,Q,MAR                                   8160741
143  A4 1D40   741            BF    C,SAVREG         LOOP TILL ALL REGISTERS ARE SAVED  8160742
               742  *                                                          8160743
               743  * SAVE DOUBLE PRECISION FLOATING POINT REGISTERS, IF EQUIPPED  8160744
               744  *                                                          8160745
144  A4 794D   745            BF    DPFP,PWRDWN2     BRANCH IF NOT EQUIPPED     8160746
145  04 757E   746            LI    MR0,'7E'                                    8160747
146  04 74A7   747            EXB   MR0,MR0,FLTPT    SET UP OP-CODE FOR         8160748
147  04 7427   748            L     MR0,MR0,FLTPT    'STMD' IN FPP = '7E00'     8160749
148  04 753E   749            LI    MR0,62                                      8160750
               750  *                                                          8160751
149  04 7871   751  STDOUBLE  ACK   MDR              GET 16-BIT DATA FROM FPP FOR DOUBLE  8160752
14A  64 6A50   752            A     MAR,Q,MAR,MW     PRECISION FLOATING POINT REGISTER  8160753
14B  05 642A   753            S     MR0,MR0,Q,CO                                8160754
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14C   A4 1D49            BF    C,STDOUBLE       LOOP TILL REG 14 IS SAVED
                   *
                   * SAVE SINGLE PRECISION FLOATING POINT REGISTERS, IF EQUIPPED
                   *
14D   A4 7557    PWRDWN2 BF    SPFP,POW         BRANCH IF NOT EQUIPPED
14E   04 7B00            LI    MAR,0
14F   04 7571            LI    MRO,'71'
150   04 74A7            EXB   MRO,MRO,FLTPT    SET UP OP-CODE FOR
151   04 7427            L     MRO,MRO,FLTPT    'STME' IN FPP = '7100'
152   04 751E            LI    MRO,30
                   *
153   04 7871    STSINGLE ACK  MDR              GET 16-BIT DATA FROM FPP FOR SINGLE
154   64 6A50            A     MAR,Q,MAR,MW     PRECISION FLOATING POINT REGISTER
155   05 642A            S     MRO,MRO,Q,CO
156   A4 1D53            BF    C,STSINGLE       LOOP TILL REG 14 IS SAVED
                   *
157   04 7844    POW     L     MDR,MDR,POW      WAIT FOR MEMORY WRITE COMPLETION
                   *                            SYSTEM CLEAR
158   A4 3D57            B     POW
                   *
                   *
                   *
                   * INTERRUPTABLE WAIT LOOP
                   *
159   00 2001    WAIT    L     Q,Q,CYD&SWA
15A   00 3001            L     Q,YD,CYD&SWA     SAVE YD IN Q, WAIT LIGHT ON
15B   84 B59D            BT    SNGL,DISPLY
15C   84 9998    WAIT1   BT    MALF+ATN,HELP1
15D   A4 AD5C            BF    CATN,WAIT1
15E   84 B575    IDLEX   BT    SNGL,CLRWT       IF SNGL, RESET WAIT BIT IN PSW THEN
                   *                            DO USER'S INSTRUCTIONS.
                   *
                   * CONSOLE SERVICE
                   *
                   * ADD, RD, WRT, RUN, REG N OR FN N KEY(S) DEPRESSED.
                   *
15F   04 7501    CONSER  LI    MRO,1
160   04 7E21            ADR   MRO              ADDRESS THE DISPLAY PANEL
                   *                            YD IS SAVED IN Q
161   0C 7180            LI    YD,'80'
162   04 3E02            OC    YD               NORMAL MODE
163   04 7E21            ADR   MRO
164   04 7472            SS    MRO              (MRO 8:15) = DISPLAY STATUS 0:7
165   04 7B20            LI    MAR,'20'         '20' = 0X0Y = SAVED DISPLAY STATUS
                   *                              X = DISPLAY STATUS BITS 5,6,7,0
                   *                              Y = DISPLAY STATUS BITS 0:3
166   40 2000            L     Q,Q,MR
167   0C 7040            L     YD,MDR           (YD) = (MDR) = 0X0Y
168   06 D9FF            N2I   MDR,YD,'FF'      (MDR) = 0X00
169   0C 7020            L     YD,MRO
16A   04 7704            LI    CNTR,4
16B   14 3000            L     YD,YD,SR         (YD12:15) = DISPLAY STATUS 0:3
16C   05 D840            O     MDR,YD,MDR       (MDR) = 0X0Y ; Y = UPDATED STATUS
16D   64 3C00            L     FLR,YD,MW        (FLR) = DISPLAY STATUS 0:3
16E   0C 2000            L     YD,Q             RESTORE YD
                   *
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 16F    84 857F   810            BT    SNGL,CONTIN          IF SNGL, GO TO CONTIN                  8160811
 170    84 2D83   811            BT    V,FNREG              FN N OR REG N KEYS DEPRESSED           8160812
 171    04 7A10   812            L     MAR,LOC                                                     8160813
 172    40 2000   813            L     Q,Q,MR               READ HW SPECIFIED BY LOC               8160814
 173    84 398B   814            BT    L,ADDWRT             ADD OR WRT KEY DEPRESSED               8160815
 174    84 358F   815            BT    G,RDKEY              RD KEY DEPRESSED                       8160816
                  816   *                                   IF NONE ABOVE, RUN KEY IS DEPRESSED.   8160817
                  817   *                                                                          8160818
 0175             818   CLRWT    EQU   *                    YD IS SAVED IN Q                       8160819
 175    0C F101   819            TCMPI YD,1                                                        8160820
 176    14 3000   820            L     YD,YD,SR             (YD) = '7FFF'                          8160821
 177    06 5000   821            N     PSW,YD,PSW           RESET WAIT BIT IN PSW                  8160822
 178    A4 3DF6   822            B     SINT2                                                       8160823
                  823   *                                                                          8160824
                  824   * SUPPORT ROUTINES                                                        8160825
                  825   *                                                                          8160826
                  826   * ON POWER UP, CONSOLE WAS IN RUN MODE & AUTO-RESTART PRESENT             8160827
                  827   *                                                                          8160828
 0179             828   MMF      EQU   *                    YD IS SAVED IN Q                       8160829
 179    1C 7000   829            L     YD,PSL,SL            LOOK @ PSW02                           8160830
 17A    1C 3000   830            L     YD,YD,SL                                                    8160831
 17B    1C 300A   831            L     YD,YD,SL+C0                                                 8160832
 17C    0C 2000   832            L     YD,Q                 RESTORE YD                             8160833
                  833   *                                                                          8160834
 17D    84 1F20   834            BT    C,MMALF1             DO MACHINE MALFUNCTION INT PSW SWAP    8160835
 17E    A4 3D75   835            B     CLRWT                                                       8160836
                  836   *                                                                          8160837
                  837   * SNGL IS SET                                                             8160838
                  838   *                                                                          8160839
 17F    00 7102   839   CONTIN   LI    Q,2                                                         8160840
 180    04 6210   840            A     LOC,Q,LOC            INCREMENT LOC BY 2                     8160841
 181    04 7D00   841            LI    FLR,0                                                       8160842
 182    A4 3C01   842            B     START1               DO USER'S INSTRUCTION                  8160843
                  843   *                                                                          8160844
                  844   * FN N , FLT N OR REG N KEYS DEPRESSED                                     8160845
                  845   *                                                                          8160846
 183    84 39C5   846   FNREG    BT    L,FLTDISP            STATUS = X1X1XXXX                      8160847
                  847   *                                           = DISPLAY SINGLE/DOUBLE FP R.  8160848
 184    84 1D9D   848            BT    C,DISPLY             STATUS = 11X0XXXX = NOT FN 0           8160849
 185    04 7C20   849            L     FLR,MR0                                                     8160850
 186    84 019D   850            BT    C+V+G+L,DISPLY                                              8160851
                  851   *                                                                          8160852
 187    04 7501   852            LI    MR0,1                CONSOLE INT.(FN 0)                     8160853
 188    04 7C80   853            EXB   FLR,PSW                                                     8160854
 189    84 1DEB   854            BT    C,CONINT             PSW04 = 1, SIMULATE CONSOLE INT.       8160855
 18A    A4 3D75   855            B     CLRWT                                                       8160856
                  856   *                                                                          8160857
                  857   *  ADD OR WRT KEY DEPRESSED                                              8160858
                  858   *                                                                          8160859
 18B    04 7874   859   ADDWRT   RD    MDR                  (MDR 8:15) = (S1 SWITCH REGISTER)      8160860
 18C    00 70F4   860            RD    Q,CS                 (Q 0:7 )   = (S2 SWITCH REGISTER)      8160861
 18D    04 6840   861            A     MDR,Q,MDR            (MDR) = S2,S1                          8160862
 18E    84 3595   862            BT    G,ADD                                                       8160863
                  863   *                                                                          8160864
                  864   * RD KEY DEPRESSED                                                        8160865
                  865   *                                                                          8160866
```

```
18F   60 7102   RDKEY    LI    Q,2,MW
190   04 6210            A     LOC,Q,LOC       INCREMENT LOC BY 2
191   04 7440            L     MR0,MDR         DISPLAY MDR IN D1 & D2
192   04 7A10            L     MAR,LOC         DISPLAY LOC IN D3 & D4
193   04 7980            LI    MDR,'80'        INDICATE MEMORY ADDRESS/DATA
194   A4 3D2F            B     OUTDIS
                *
                * ADD KEY DEPRESSED
                *
195   04 7240   ADD      L     LOC,MDR         (LOC) = S2,S1 SWITCH REG.
196   A4 3D2C            B     LOCDIS          DISPLAY SWITCH REG DATA
                *
                * TO HELP DISTINGUISH I/O ATN, CATN, SNGL & MACHINE MALFUNCTION
                *
197   05 7215   HELP     DEC   LOC,LOC         DECREMENT LOC BY 2
                *
198   00 3000   HELP1    L     Q,YD            SAVE YD IN Q
199   84 BB1E            BT    MALF,MMALF      MACHINE MALFUNCTION HAS OCCURED
19A   84 9DE7            BT    ATN,IOATN       REQUEST FOR ATTENTION FROM I/O BUS
19B   84 AD5F            BT    CATN,CONSER     CONSOLE SERVICE DESIRED
19C   A4 B4A1            BF    SNGL,NOB        NO INTERRUPT QUEUED. FETCH NEXT
                *                              USER INSTRUCTION.
                *                              USER PROGRAM BEING SINGLE-STEPPED.
                *                              DISPLAY REG N OR PSW OR LOC.
                *
                * TO DISPLAY REG N OR PSW OR LOC ETC.
                *
19D   04 7501   DISPLY   LI    MR0,1
19E   04 7E21            ADR   MR0             ADDRESS THE DISPLAY PANEL
19F   00 7472            SS    MR0&Q
                *
1A0   04 6A20            A     MAR,Q,MR0
1A1   00 7000            EXB   Q,MAR
1A2   04 6A50            A     MAR,Q,MAR
1A3   00 710F            LI    Q,15
1A4   02 6A50            N     MAR&Q,Q,MAR     (MAR)=(Q)= N = REGISTER NUMBER
                *
1A5   04 7C20            L     FLR,MR0         (FLR) = DISPLAY STATUS 4:7
1A6   84 1DBB            BT    C,LOOK20        BIT 4 SET (REG N OR FLT N)
1A7   04 2C00            L     FLR,Q           (FLR) = STATUS BITS 5,6,7,0
1A8   84 1D34            BT    C,IDLE
1A9   84 2D86            BT    V,PSWLOC        BIT 6 SET  (FN 4 OR FN 5)
1AA   84 3580            BT    G,FN2,FN3       BIT 7 SET  (FN 2 OR FN 3)
1AB   A4 3934            BF    L,IDLE          MUST BE FN 1
                *
                *
                * FN 1 KEYS DEPRESSED
                *
1AC   04 7874   FN1      RD    MDR
1AD   00 70F4            RD    Q,CS
1AE   04 6040            A     PSW,Q,MDR       (PSW) = SWITCH REGISTER
1AF   A4 3088            B     FN11
                *
                * FN 2 OR FN 3 KEYS DEPRESSED
                *
1B0   04 7820   FN2,FN3  LI    MAR,'20'
```

```
181  44 2400   922          L    MR0,Q,MR          '20' = 0X0Y = SAVED STATUS                8160923
               923  *                                 X = DISPLAY STATUS BITS 5,6,7,0         8160924
               924  *                                 Y = DISPLAY STATUS BITS 0:3             8160925
182  04 7840   925          L    MDR,MDR           WAIT FOR MEMORY                           8160926
183  04 78A0   926          L    MDR,MR0,CS        (MDR)= 0X0Y ; X = UPDATED STATUS          8160927
               927  *                             MS BYTE OF MDR ALTERED AS MAR EVEN        8160928
184  60 2000   928          L    Q,Q,MW            WRITE BACK                                8160929
185  A4 3D2C   929          B    LOCDIS                                                      8160930
               930  *                                                                       8160931
               931  * FN 4 OR FN 5 KEYS DEPRESSED                                          8160932
               932  *                                                                       8160933
186  84 3534   933  PSWLOC  BT   G,IDLE            TO IDLE FOR FN 6 OR FN 7                  8160934
187  84 392C   934          BT   L,LOCDIS                                                   8160935
188  04 7400   935  FN11   L    MR0,PSW           DISPLAY PSW IN D1 & D2                    8160936
               936  *                             DISPLAY 0      IN D3 & D4                 8160937
189  04 7944   937          LI   MDR,'44'          INDICATE FN 4                            8160938
18A  A4 3D2E   938          B    MAR0                                                       8160939
               939  *                                                                       8160940
               940  * TO DISTINGUISH BETWEEN GENERAL / FLOATING POINT REGISTER            8160941
               941  *                                                                       8160942
18B  04 7B20   942  LOOK20 LI   MAR='20'                                                   8160943
18C  44 2A00   943          L    MAR,Q,MR                                                   8160944
18D  04 7C40   944          L    FLR,MDR                                                    8160945
18E  84 39C5   945          BT   L,FLTDISP                                                  8160946
               946  *                                                                       8160947
               947  * REG N KEYS ARE DEPRESSED                                           8160948
               948  *                                                                       8160949
18F  00 2001   949  REGDIS L    Q,Q,CYD&SWA       CLEAR YD FIELD                            8160950
1C0  05 7A55   950  REGN   DEC  MAR,MAR                                                    8160951
1C1  04 3402   951          L    MR0,YDP1          DISPLAY REG N IN D1 & D2                  8160952
1C2  A4 1DC0   952          BF   C,REGN                                                     8160953
               953  *                             DISPLAY 0      IN D3 & D4                 8160954
1C3  05 E920   954          OI   MDR,Q,'20'        (MDR) = '2N'                             8160955
1C4  A4 3D2E   955          B    MAR0              MDR INDICATES REG N                       8160956
               956  *                                                                       8160957
               957  * FLT N KEYS ARE DEPRESSED                                           8160958
               958  *                                                                       8160959
1C5  A4 752C   959  FLTDISP BF   SPFP,LOCDIS       BRANCH IF FLOATING POINT ABSENT           8160960
1C6  00 3000   960          L    Q,YD              SAVE YD IN Q                              8160961
1C7  0C 7107   961          LI   YD,7                                                       8160962
1C8  1E 5020   962          N    YD,YD,MR0,SL      (YD 12:14) = STATUS BITS 5,6,7            8160963
1C9  A4 1DCB   963          BF   C,FLT1                                                     8160964
1CA  0D D101   964          OI   YD,YD,1           OR IN STATUS BIT 0                       8160965
1CB  04 7704   965  FLT1   LI   CNTR,4                                                     8160966
1CC  1C 3000   966          L    YD,YD,SL          (YD) = 00N0 ; N = REGISTER NUMBER         8160967
               967  *                                        = ODD/EVEN                     8160968
1CD  04 7B20   968          LI   MAR,'20'          '20' = 0X0Y = SAVED STATUS               8160969
               969  *                                 X = DISPLAY STATUS BITS 5,6,7,0         8160970
               970  *                                 Y = DISPLAY STATUS BITS 0:3             8160971
1CE  44 7570   971          LI   MR0,'70',MR                                                8160972
1CF  04 7CC0   972          L    FLR,MDR,CS        (FLR) = STATUS BITS 5,6,7,0               8160973
1D0  84 39D2   973          BT   L,FLT2            BRANCH IF DOUBLE PRECISION REG.          8160974
1D1  04 7560   974          LI   MR0,'60'                                                   8160975
1D2  04 74A0   975  FLT2   EXB  MR0,MR0                                                    8160976
1D3  05 D427   976          O    MR0,YD,MR0,FLTPT  SET UP OP-CODE IN FPP FOR                 8160977
1D4  05 D427   977          O    MR0,YD,MR0,FLTPT  'STE' = '60N0' OR 'STD' = '70N0'          8160978
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1D5   04 7A71   978          ACK   MAR      D3,D4 = MOST SIGNIFICANT 16 BITS      8160979
1D6   04 7471   979          ACK   MR0      D1,D2 = NEXT 16 BITS                  8160980
1D7   04 7704   980          LI    CNTR,4                                         8160981
1D8   14 3000   981          L     YD,YD,SR  (YD) = 000N = REGISTER #              8160982
1D9   A4 39DF   982          BF    L,FLT3    BRANCH IF SINGLE PRECISION REG.      8160983
1DA   A4 79E2   983          BF    DPFP,FLT4 BRANCH IF DOUBLE PRECISION ABSENT    8160984
1DB   04 3C00   984          L     FLR,YD                                         8160985
1DC   A4 39E4   985          BF    L,FLT5    BRANCH IF N IS EVEN                  8160986
1DD   04 7A71   986          ACK   MAR       D3,D4 = NEXT 16 BITS                 8160987
1DE   04 7471   987          ACK   MR0       D1,D2 = LEAST SIGNIFICANT 16 BITS    8160988
1DF   05 D910   988   FLT3   QI    MDR,YD,'10' (MDR) = '001N'                     8160989
1E0   0C 2000   989          L     YD,Q      RESTORE YD                           8160990
1E1   A4 3D2F   990          B     OUTDIS                                         8160991
                991   *                                                          8160992
1E2   0C 2000   992   FLT4   L     YD,Q      RESTORE YD                           8160993
1E3   A4 3D2C   993          B     LOCDIS                                         8160994
                994   *                                                          8160995
1E4   04 7871   995   FLT5   ACK   MDR       SEND REMAINING 2 ACK FOR             8160996
1E5   04 7871   996          ACK   MDR       FPP TO GO TO IDLE STATE.             8160997
1E6   A4 3DDF   997          B     FLT3                                           8160998
                998   *                                                          8160999
                999   *                                                          8161000
               1000   * I/O DEVICE REQUESTS ATTENTION                            8161001
               1001   *                                                          8161002
 01E7          1002   IOATN  EQU   *                                            8161003
1E7   04 7B40  1003          LI    MAR,'40'                                       8161004
1E8   04 7C80  1004          EXB   FLR,PSW   LOOK @ PSW04                       8161005
1E9   A4 1F21  1005          BF    C,GENSWP                                       8161006
               1006   *                                                          8161007
               1007   * AUTOMATIC I/O SERVICE                                    8161008
               1008   *                                                          8161009
1EA   04 7471  1009   IOSVC  ACK   MR0       (MR0) = INTERRUPTING DEV ADR       8161010
               1010   *                                                          8161011
               1011   *                                                          8161012
               1012   * CONSOLE INTERRUPT                                        8161013
               1013   *                                                          8161014
 01EB          1014   CONINT EQU   *                                            8161015
1EB   00 3000  1015          L     Q,YD      SAVE YD IN Q                         8161016
1EC   1C 7020  1016          L     YD,MR0,SL (YD) = 2 X DEVICE ADDRESS            8161017
 01ED          1017   SINT1  EQU   *         FROM SINT EMULATION ROUTINE          8161018
1ED   04 5BD0  1018          AI    MAR,YD,'D0'                                    8161019
1EE   4C 7102  1019          LI    YD,2,MR                                        8161020
1EF   04 7A40  1020          L     MAR,MDR   (MAR) = I/O SERVICE TABLE ENTRY      8161021
1F0   04 7800  1021          L     MDR,PSW                                        8161022
1F1   64 5A50  1022          A     MAR,YD,MAR,MW STORE OLD PSW                    8161023
1F2   04 7810  1023          L     MDR,LOC                                        8161024
1F3   64 5A50  1024          A     MAR,YD,MAR,MW STORE OLD LOC                    8161025
1F4   44 5250  1025          A     LOC,YD,MAR,MR NEW LOC                          8161026
1F5   04 7040  1026          L     PSW,MDR   NEW PSW                              8161027
1F6   0C 2000  1027   SINT2  L     YD,Q      RESTORE YD                           8161028
1F7   C4 7C00  1028          L     FLR,PSW,IR DO USER'S INSTRUCTION               8161029
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FIXED POINT MPY/DIV SUPPORT

```
 1F8                    *                                                                     8161031
                        *                                                                     8161032
                                 ORG    '200'                                                 8161033
                        *                                                                     8161034
                        * DIVIDE                                                              8161035
                        *                                                                     8161036
  0200                  DHR1     EQU    *                                                     8161037
 200     04 7B00                 LI     MAR,0          RESET REMAINDER FLAG ( +VE OR 0 )      8161038
 201     07 F900                 INVI   MDR,0          SET QUOTIENT FLAG    ( -VE )           8161039
 202     04 742C                 L      MR0,MR0,F      LOOK @ DIVISOR                         8161040
 203     84 3A07                 BT     L,MRONEG                                              8161041
 204     A4 362A                 BF     G,OV1          IT IS ZERO                             8161042
                        *                                                                     8161043
 205     04 F420        MROPOS   TCMP   MR0,MR0        MAKE DIVISOR NEGATIVE                  8161044
 206     04 7900                 LI     MDR,0          RESET QUOTIENT FLAG                    8161045
                        *                                                                     8161046
  0207                  MRONEG   EQU    *                                                     8161047
 207     0C 300C                 L      YD,YD,F        LOOK @ DIVIDEND                        8161048
 208     A4 3A0D                 BF     L,YDNNEG                                              8161049
                        *                              DIVIDEND IS NEGATIVE                   8161050
 209     07 FA52                 INV    MAR,MAR,YDP1   SET REMAINDER FLAG  ( -VE )            8161051
 20A     0D 300A                 TCMP   YD,YD,CO       COMPLEMENT LS PORTION OF  DIVIDEND     8161052
 20B     07 F843                 INV    MDR,MDR,YDM1   INVERT QUOTIENT FLAG                   8161053
 20C     0D 3009                 TCMP   YD,YD,CI       COMPLEMENT MS PORTION OF DIVIDEND      8161054
  020D                  YDNNEG   EQU    *                                                     8161055
 20D     00 502A                 A      Q,YD,MR0,CO                                           8161056
 20E     00 3002                 L      Q,YDP1         (Q) = MS PORTION OF DIVIDEND           8161057
                        *                              YD NOW POINTS TO  R1+1                 8161058
 20F     84 1E25                 BT     C,OV           QUOTIENT TOO LARGE FOR 16 BITS         8161059
                        *                                                                     8161060
 210     04 7426                 L      MR0,MR0,M/D    LOAD DIVISOR INTO M/D BOX              8161061
 211     04 7426                 L      MR0,MR0,M/D                                           8161062
 212     0C 3006                 L      YD,YD,M/D      LOAD LS PORTION OF DIVIDEND            8161063
 213     0C 3006                 L      YD,YD,M/D                                             8161064
 214     00 2006                 L      Q,Q,M/D        LOAD MS PORTION OF DIVIDEND            8161065
 215     00 2006                 L      Q,Q,M/D                                               8161066
                        *                                                                     8161067
                        * DIVISION IS DONE BY THE M/D BOX ON THE I/O BUS                      8161068
                        *                                                                     8161069
 216     00 7078                 L      Q,IO           GET QUOTIENT                           8161070
 217     04 7478                 L      MR0,IO         GET REMAINDER                          8161071
                        *                                                                     8161072
 218     04 7A5C                 L      MAR,MAR,F      REMAINDER EXPECTED TO BE NEGATIVE ?    8161073
 219     A4 3A1B                 BF     L,RNNEG                                               8161074
 21A     04 F420                 TCMP   MR0,MR0        YES, ADJUST REMAINDER                  8161075
  021B                  RNNEG    EQU    *                                                     8161076
 21B     04 784C                 L      MDR,MDR,F      QUOTIENT EXPECTED TO BE POSITIVE ?     8161077
 21C     84 3A22                 BT     L,QNEG                                                8161078
 21D     00 200C                 L      Q,Q,F          YES, NOW LOOK @ THE QUOTIENT           8161079
 21E     84 3A25                 BT     L,OV           QUOTIENT > +32767                      8161080
                        *                                                                     8161081
 21F     0C 2003        QOK      L      YDM1,Q         (R1+1) = QUOTIENT                      8161082
 220     0C 7020                 L      YD,MR0         (R1) = REMAINDER                       8161083
 221     C4 7C00                 L      FLR,PSW,IR                                            8161084
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FIXED POINT MPY/DIV SUPPORT

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                                1084    *
                                1085    QNEG    EQU     *                                                       8161085
                                1086            LI      FLR,0                                                   8161086
0222                                                                                                            8161087
222     04 7D00                 1087            TCMP    Q,Q,F           COMPLEMENT THE QUOTIENT & EXAMINE       8161088
223     01 200C                 1088            BF      G,QOK           QUOTIENT OK                             8161089
224     A4 361F                 1089                                    QUOTIENT < -32768                       8161090
                                1090    *                                                                       8161091
                                1091    OV      EQU     *               QUOTIENT OVERFLOW DETECTED              8161092
0225                                                                                                            8161093
225     04 7A5C                 1092            L       MAR,MAR,F                                               8161094
226     A4 3A2A                 1093            BF      L,OV1           DIVIDEND IS NOT ALTERED                 8161095
                                1094    *                                                                       8161096
                                1095    * RESTORE DIVIDEND TO ITS ORIGINAL VALUE. YD POINTS TO  R1+1           8161097
                                1096    *                                                                       8161098
227     0D 300A                 1097            TCMP    YD,YD,CO                                                8161099
228     0C 3003                 1098            L       YDM1,YD         POINT TO R1                             8161100
229     0D 3009                 1099            TCMP    YD,YD,CI                                                8161101
                                1100    *                                                                       8161102
22A     04 7848                 1101    OV1     LI      MAR,'48'                                                8161103
22B     04 3400                 1102            L       MR0,YD          SAVE YD IN MR0                          8161104
22C     1C 7000                 1103            L       YD,PSW,SL                                               8161105
22D     04 7703                 1104            LI      CNTR,3          LOOK @ PSW03                            8161106
22E     1C 300A                 1105            L       YD,YD,SL+CO                                             8161107
22F     84 1F22                 1106            BT      C,QUEINT        DO PSW SWAP IF SET                      8161108
                                1107    *                                                                       8161109
230     0C 7020                 1108            L       YD,MR0          RESTORE YD                              8161110
231     C4 7C00                 1109            L       FLR,PSW,IR                                              8161111
                                1110    *                                                                       8161112
                                1111    *                                                                       8161113
                                1112    * SIGNED MULTIPLY                                                      8161114
                                1113    *                                                                       8161115
0232                            1114    MHR1    EQU     *                                                       8161116
232     04 7800                 1115            LI      MAR,0           RESET FLAG                              8161117
233     0C 3002                 1116            L       YDP1,YD         BUMP YD FIELD                           8161118
234     0C 300C                 1117            L       YD,YD,F         LOOK @ MULTIPLICAND                     8161119
235     A4 3A38                 1118            BF      L,NNEG1                                                 8161120
236     0D 3000                 1119            TCMP    YD,YD           NEGATIVE. COMPLEMENT IT.                8161121
237     07 F800                 1120            INVI    MAR,0           SET FLAG                                8161122
238     04 742C                 1121    NNEG1   L       MR0,MR0,F       LOOK @ MLTIPLIER                        8161123
239     A4 3A3C                 1122            BF      L,NNEG2                                                 8161124
23A     04 F420                 1123            TCMP    MR0,MR0         NEGATIVE. COMPLEMENT IT.                8161125
23B     07 FA5C                 1124            INV     MAR,MAR         INVERT FLAG                             8161126
                                1125    *                                                                       8161127
23C     0C 3006                 1126    NNEG2   L       YD,YD,M/D       LOAD MULTIPLICAND INTO M/D BOX          8161128
23D     0C 3006                 1127            L       YD,YD,M/D                                               8161129
23E     04 7426                 1128            L       MR0,MR0,M/D     LOAD MULTIPLIER                         8161130
23F     04 7426                 1129            L       MR0,MR0,M/D                                             8161131
                                1130    *                                                                       8161132
                                1131    * MULTIPLICATION IS DONE BY THE M/D BOX ON THE I/O BUS                  8161133
                                1132    *                                                                       8161134
240     0C 7078                 1133            L       YD,IO           (R1+1) * LS PORTION OF THE RESULT       8161135
241     00 7078                 1134            L       Q,IO            GET MS PORTION OF RESULT                8161136
                                1135    *                                                                       8161137
242     04 7A5C                 1136            L       MAR,MAR,F       RESULT EXPECTED TO BE NEGATIVE ?        8161138
243     A4 3A9F                 1137            BF      L,OOK1          NO, GO SET UP (R1) = MS PORTION
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FIXED POINT MPY/DIV SUPPORT

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244   0D 300A   1138            TCMP  YD,YD,CO      YES, COMPLEMENT IT                  8161139
245   0C 3003   1139            L     YDM1,YD                                           8161140
246   0D 2009   1140            TCMP  YD,Q,CI        (R1) = MS PORTION OF THE RESULT   8161141
247   C4 7C00   1141            L     FLR,PSW,IR     FETCH NEXT USER INSTRUCTION        8161142
                1142  *                                                                8161143
                1143  * UNSIGNED MULTIPLY                                             8161144
                1144  *                                                                8161145
 0248           1145  MHUR1     EQU   *                                                8161146
248   00 3002   1146            L     Q,YDP1                                            8161147
249   0C 3006   1147            L     YD,YD,M/D      LOAD MULTIPLICAND INTO M/D BOX     8161148
24A   0C 3006   1148            L     YD,YD,M/D                                         8161149
24B   04 7426   1149            L     MR0,MR0,M/D    LOAD MULTIPLIER                    8161150
24C   04 7426   1150            L     MR0,MR0,M/D                                       8161151
                1151  *                                                                8161152
                1152  * MULTIPLICATION IS DONE BY THE M/D BOX ON THE I/O BUS           8161153
                1153  *                                                                8161154
24D   0C 7078   1154            L     YD,IO          (R1+1) = LS PORTION OF THE RESULT  8161155
24E   00 7078   1155            L     Q,IO           GET MS PORTION OF THE RESULT       8161156
24F   04 7C03   1156  QOK1      L     FLR PSW,YDM1                                      8161157
250   CC 2000   1157            L     YD,Q,IR                                           8161158
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LIST PROCESSING SUPPORT

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                                    1159  *                                                                                  8161160
                                    1160  * COME HERE FOR  :  ATL,ABL  (D1)                                                 8161161
                                    1161  *                                                                                  8161162
                                    1162  ATLABLD1 EQU   *                                                                  8161163
 0251                               1163          BF      AMOD,ATL1                                                         8161164
 251    A4 DE53                     1164          A       MDR,Q,MDR       ADD INDEX REGISTER                                8161165
 252    04 6840                     1165  ATL1    L       MAR,MDR         (MAR) = LIST ADDRESS                              8161166
 253    04 7A40                     1166          L       Q,Q,MR          (MDR) ='# OF SLOTS, # USED' HW                    8161167
 254    40 2000                     1167          L       Q,MDR,CS        (Q)   = # USED, # SLOTS                           8161168
 255    00 70C0                     1168          S       Q,Q,MDR,CO                                                        8161169
 256    00 E04A                     1169          BF      C,LIST,OV       LIST OVERFLOW                                     8161170
 257    A4 1E8A                     1170          INC     MDR,MDR         (MDR) = # SLOTS, # USED+1                         8161171
 258    04 7845                     1171          INC     MAR,MAR,MW      WRITE BACK '# SLOTS,# USED'  HW                   8161172
 259    64 7A55                     1172          INC     MAR,MAR         MAR POINTS TO 'CUR. TOP,NEXT BOTTOM'              8161173
 25A    04 7A55                     1173          DEC     MR0,MDR,CS      (MR0) = # USED+1, # SLOTS-1                       8161174
 25B    05 74C5                     1174          LI      Q,'FF',MR       (MDR) = 'TOP,BOTTOM'  HW                          8161175
 25C    40 71FF                     1175          N       MR0,Q,MR0,D2    (MR0) = 0, #SLOTS-1                               8161176
 25D    26 6420                     1176  *                                                                                  8161177
                                    1177  * COME HERE FOR  :  ATL  (D2)                                                    8161178
                                    1178  *                                                                                  8161179
 25E    05 6845                     1179  ATLD2   S       MDR,MDR,Q,JAMCI&CO  (MDR) = TOP-1,BOTTOM                          8161180
 25F    A4 1E61                     1180          BF      C,NOWRAP1                                                         8161181
 260    04 78A0                     1181          L       MDR,MR0,CS      (MDR) = # SLOTS-1,BOTTOM                          8161182
 261    02 60C0                     1182  NOWRAP1 N       Q,Q,MDR,CS      (Q) = 0,NEW TOP    (ATL)                          8161183
                                    1183  *                               (Q) = 0,OLD BOTTOM (ABL)                          8161184
 262    64 6A55                     1184  ATL2    A       MAR,Q,MAR,JAMCI&CO+MW DO (MAR+Q+1)                                8161185
                                    1185  *                               WRITE BACK 'TOP,BOTTOM'  HW                       8161186
 263    04 6A55                     1186          A       MAR,Q,MAR,JAMCI&CO  (MAR) = SLOT ADDRESS                          8161187
 264    04 3800                     1187          L       MDR,YD                                                            8161188
 265    64 7D00                     1188          LI      FLR,0,MW        WRITE ELEMENT INTO LIST SLOT                      8161189
 266    C0 2000                     1189          L       Q,Q,IR                                                            8161190
                                    1190  *                                                                                  8161191
                                    1191  * COME HERE FOR  :  ABL  (D2)                                                    8161192
                                    1192  *                                                                                  8161193
 267    02 6040                     1193  ABLD2   N       Q,Q,MDR         (Q)   = 0, BOTTOM                                8161194
 268    04 7845                     1194          INC     MDR,MDR         (MDR) = TOP,BOTTOM+1                              8161195
 269    05 6425                     1195          S       MR0,MR0,Q,JAMCI&CO  DO (#SLOTS-1) - BOTTOM - 1                    8161196
 26A    A4 1E62                     1196          BF      C,ATL2                                                            8161197
 26B    05 6845                     1197          S       MDR,MDR,Q,JAMCI&CO  (MDR) = TOP,0                                 8161198
 26C    A4 3E62                     1198          B       ATL2                                                              8161199
                                    1199  *                                                                                  8161200
                                    1200  * COME HERE FOR  :  RTL,RBL  (D1)                                                8161201
                                    1201  *                                                                                  8161202
 026D                               1202  RTLRBLD1 EQU   *                                                                  8161203
 26D    A4 DE6F                     1203          BF      AMOD,RTL1                                                         8161204
 26E    04 6840                     1204          A       MDR,Q,MDR       ADD INDEX REGISTER                                8161205
 26F    04 7A40                     1205  RTL1    L       MAR,MDR         (MAR) = LIST ADDRESS                              8161206
 270    40 71FF                     1206          LI      Q,'FF',MR       (MDR) = # OF SLOTS, # USED                        8161207
 271    05 64C5                     1207          S       MR0,MDR,Q,CS+JAMCI&CO (MR0) = # USED-1, # SLOTS                   8161208
 272    A4 1E8A                     1208          BT      C,WASEMPTY                                                        8161209
 273    05 7845                     1209          DEC     MDR,MDR         (MDR) = # SLOTS, # USED-1                         8161210
 274    64 7A55                     1210          INC     MAR,MAR,MW      WRITE BACK '#SLOTS,#USED'  HW                     8161211
 275    04 7A55                     1211          INC     MAR,MAR                                                           8161212
 276    4E 60AC                     1212          N       YD,Q,MR0,CS+F+MR  CY6L = 0000  (NOW EMPTY)                        8161213
```

LIST PROCESSING SUPPORT

```
                        1213  *                                    *    = 0010  (NOT YET EMPTY)          8161214
                        1214  *                                    (MDR) = 'TOP,BOTTOM'  HW          8161215
 277    26 6420         1215          N     MR0,Q,MR0,02           (MR0)= 0, # SLOTS                 8161216
                        1216  *                                                                        8161217
                        1217  * COME HERE FOR  :  RTL  (D2)                                          8161218
                        1218  *                                                                        8161219
 278    04 6845         1219  RTLD2   A     MDR,Q,MDR,JAMCI&CO     (MDR) = TOP+1,BOTTOM    (NO WRAP) 8161220
 279    02 60C0         1220          N     Q,Q,MDR,CS             (Q)   = 0,TOP+1                   8161221
 27A    05 6425         1221          S     MR0,MR0,Q,JAMCI&CO     DO (#SLOTS) - (TOP+1) = 1         8161222
 27B    00 E101         1222          SI    Q,Q,'01'               (Q) = 0,TOP                       8161223
 27C    A4 1E85         1223          BF    C,RTL2                                                   8161224
 27D    04 2880         1224          L     MDR,Q,CS               (MDR) = 0,BOTTOM  (WRAP)          8161225
 27E    A4 3E85         1225          B     RTL2                                                     8161226
                        1226  *                                                                        8161227
                        1227  * COME HERE FOR  :  RBL  (D2)                                          8161228
                        1228  *                                                                        8161229
 27F    02 6040         1229  RBLD2   N     Q,Q,MDR                (MDR) = 'TOP,BOTTOM'  HW          8161230
                        1230  *                                    (Q)   = 0,BOTTOM                  8161231
 280    07 6840         1231          X     MDR,Q,MDR              (MDR) = TOP,0                     8161232
 281    00 A005         1232          DEC   Q,Q                    (Q)   = 0,BOTTOM-1                8161233
 282    A4 1E84         1233          BF    C,NOWRAP4                                                8161234
 283    01 7025         1234          DEC   Q,MR0                  (Q)   = 0,#SLOTS-1                8161235
 284    05 E840         1235  NOWRAP4 O     MDR,Q,MDR              (MDR) = TOP,BOTTOM-1  (NO WRAP)   8161236
                        1236  *                                    *     = TOP,#SLOTS-1  (WRAP)      8161237
 0285                   1237  RTL2    EQU   *                      (Q)   = 0,OLD TOP     (RTL)       8161238
                        1238  *                                          = 0,NEW BOTTOM (RBL)       8161239
 285    64 6A55         1239          A     MAR,Q,MAR,JAMCI&CO+MW DO (MAR+Q+1)                       8161240
                        1240  *                                    WRITE BACK 'TOP,BOTTOM' HW        8161241
 286    04 6A55         1241          A     MAR,Q,MAR,JAMCI&CO     (MAR) = SLOT ADDRESS              8161242
 287    40 2000         1242          L     Q,Q,MR                                                   8161243
 288    0C 7040         1243          L     YD,MDR                 EXTRACT LIST ITEM INTO R1         8161244
 289    C0 2000         1244          L     Q,Q,IR                 CVGL = 0000 OR 0010               8161245
                        1245  *                                                                        8161246
                        1246  * COME HERE IF LIST OVERFLOWS / WAS EMPTY                               8161247
                        1247  *                                                                        8161248
 028A                   1248  WASEMPTY EQU  *                                                        8161249
 28A    C4 7D04         1249  LIST,OV LI    FLR,4,IR               CVGL = 0100                       8161250
```

```
                   *
                   * COME HERE THRU D2 FOR  :  LMD
                   *
28B   44 6A50      LMDD2   A     MAR,Q,MAR,MR        GET 16 BITS FROM MAIN MEMORY
28C   04 7847              L     MDR,MDR,FLTPT       SEND 16 BITS TO FPP
28D   04 7847              L     MDR,MDR,FLTPT
28E   44 6A50              A     MAR,Q,MAR,MR
28F   04 7847              L     MDR,MDR,FLTPT       16 BITS
290   04 7847              L     MDR,MDR,FLTPT
                   *
                   * COME HERE THRU D2 FOR  :  LME
                   *
291   44 6A50      LMED2   A     MAR,Q,MAR,MR
292   04 7847              L     MDR,MDR,FLTPT       SEND 16 BITS TO FPP
293   04 7847              L     MDR,MDR,FLTPT
294   44 6A50              A     MAR,Q,MAR,MR
295   04 7847              L     MDR,MDR,FLTPT       16 BITS
296   04 7847              L     MDR,MDR,FLTPT
                   *
297   05 642A              S     MR0,MR0,Q,CO        DECREAMENT COUNT
298   84 1F0C              BT    C,LMEDONE           EXIT IF DONE
299   20 2000              L     Q,Q,D2              OTHERWISE, LOOP THRU D2
                   *
                   * COME HERE THRU D2 FOR  :  STMD
                   *
29A   04 7871      STMDD2  ACK   MDR                 GET U6 BITS FROM FPP
29B   64 6A50              A     MAR,Q,MAR,MW        WRITE INTO MAIN MEMORY
29C   04 7871              ACK   MDR                 16 BITS
29D   64 6A50              A     MAR,Q,MAR,MW
                   *
                   * COME HERE THRU D2 FOR  :  STME
                   *
29E   04 7871      STMED2  ACK   MDR                 GET 16 BITS FROM FPP
29F   64 6A50              A     MAR,Q,MAR,MW
2A0   04 7871              ACK   MDR                 16 BITS
2A1   64 6A50              A     MAR,Q,MAR,MW
                   *
2A2   05 642A              S     MR0,MR0,Q,CO        DECREAMENT COUNT
2A3   84 1CA1              BT    C,NOB               EXIT IF DONE
2A4   20 2000              L     Q,Q,D2              OTHERWISE, LOOP THRU D2
                   *
                   * COME HERE FROM D1 FOR : LE,CE,AE,SE,ME,DE
                                             LD,CD,AD,SD,MD,DD
                   *
                   *
2A5   A4 DEA7      FRXD1   BF    AMOD,FRXNX
2A6   04 6840              A     MDR,Q,MDR
2A7   04 7A40      FRXNX   L     MAR,MDR             (MAR) = SECOND OP ADDRESS
2A8   40 7102              LI    Q,2,MR
2A9   04 6A50              A     MAR,Q,MAR
2AA   04 7847              L     MDR,MDR,FLTPT       16 BITS TO FPP
2AB   04 7847              L     MDR,MDR,FLTPT
2AC   44 6A50              A     MAR,Q,MAR,MR        BUMP MAR BY 2
2AD   04 7847              L     MDR,MDR,FLTPT       16 BITS
2AE   24 7847              L     MDR,MDR,FLTPT+D2
```

FLOATING POINT SUPPORT

```
                                1305    *                                                                       8161306
                                1306    * COME HERE FOR STD                                                    8161307
                                1307    *                                                                       8161308
 2AF    04 7871                 1308    STDD2   ACK   MDR              (MDR) = MS 16 BITS OF DPFP REGISTER     8161309
 2B0    64 6A50                 1309            A     MAR,Q,MAR,MW                                             8161310
 2B1    04 7871                 1310            ACK   MDR              *     = NEXT 16 BITS                    8161311
 2B2    64 6A50                 1311            A     MAR,Q,MAR,MW                                             8161312
                                1312    *                                                                       8161313
                                1313    * COME HERE FOR STE                                                    8161314
                                1314    *                                                                       8161315
 2B3    04 7871                 1315    STED2   ACK   MDR              (MDR) = MS 16 BITS OF SPFP REGISTER     8161316
 2B4    64 6A50                 1316            A     MAR,Q,MAR,MW                                             8161317
 2B5    04 7871                 1317            ACK   MDR              *     = LS 16 BITS                      8161318
 2B6    60 2000                 1318            L     Q,Q,MW           WRITE INTO MAIN MEMORY                  8161319
 2B7    C4 7C00                 1319            L     FLR,PSW,IR                                               8161320
                                1320    *                                                                       8161321
                                1321    * COME HERE THRU D2 FOR : CD                                           8161322
                                1322    *                                                                       8161323
 2B8    44 6A50                 1323    CDD2    A     MAR,Q,MAR,MR                                             8161324
 2B9    04 7847                 1324            L     MDR,MDR,FLTPT    16 BITS                                 8161325
 2BA    04 7847                 1325            L     MDR,MDR,FLTPT                                            8161326
 2BB    44 6A50                 1326            A     MAR,Q,MAR,MR                                             8161327
 2BC    04 7847                 1327            L     MDR,MDR,FLTPT    16 BITS                                 8161328
 2BD    04 7847                 1328            L     MDR,MDR,FLTPT                                            8161329
                                1329    *                                                                       8161330
                                1330    * COME HERE FOR : CER,CDR      (D1)                                    8161331
                                1331    *               : CE           (D2)                                    8161332
 02BE                           1332    CERD1   EQU   *                                                        8161333
 2BE    04 7C71                 1333            ACK   FLR              GET CC FROM FPP                         8161334
 2BF    C0 2000                 1334            L     Q,Q,IR           UPDATE CC,                              8161335
                                1335    *                                                                       8161336
                                1336    * COME HERE THRU D2 FOR : LD,AD,SD,MD,DD                               8161337
                                1337    *                                                                       8161338
 2C0    44 6A50                 1338    FDRXD2  A     MAR,Q,MAR,MR                                             8161339
 2C1    04 7847                 1339            L     MDR,MDR,FLTPT    16 BITS                                 8161340
 2C2    04 7847                 1340            L     MDR,MDR,FLTPT                                            8161341
 2C3    44 6A50                 1341            A     MAR,Q,MAR,MR                                             8161342
 2C4    04 7847                 1342            L     MDR,MDR,FLTPT    16 BITS                                 8161343
 2C5    04 7847                 1343            L     MDR,MDR,FLTPT                                            8161344
                                1344    *                                                                       8161345
                                1345    * COME HERE FOR : LER,AER,SER,MER,DER    (D1)                          8161346
                                1346    *               : LDR,ADR,SDR,MDR,DDR    (D1)                          8161347
                                1347    *               : LE ,AE ,SE ,ME ,DE     (D2)                          8161348
 02C6                           1348    FRRD1   EQU   *                                                        8161349
 2C6    00 7C71                 1349            ACK   FLR&Q            WAIT HERE TILL FLOATING POINT           8161350
                                1350    *                              PROCESSOR SENDS CONDITION CODE          8161351
                                1351    *                                                                       8161352
 2C7    84 2ED4                 1352            BT    V,FL,OV          EXPONENT OVERFLOW/UNDERFLOW OCCURED     8161353
 2C8    C4 2C00                 1353    F,CC    L     FLR,Q,IR         UPDATE CC, FETCH NEXT INSTRUCTION       8161354
                                1354    *                                                                       8161355
                                1355    * COME HERE FOR : FXR,FXDR                                             8161356
                                1356    *                                                                       8161357
 02C9                           1357    FXRD1   EQU   *                                                        8161358
 2C9    0C 7071                 1358            ACK   YD               (R1) = FIX POINT NUMBER FROM FPP        8161359
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FLOATING POINT SUPPORT

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                                1359            ACK   MR0          DUMMY READ FOR FPP TO IDLE          8161360
 2CA    04 7471                 1360   FXR2     ACK   FLR          GET CC                              8161361
 2CB    04 7C71                 1361            L     Q,Q,IR       UPDATE CC & FETCH INSTRUCTION       8161362
 2CC    C0 2000                 1362   *                                                               8161363
                                1363   * COME HERE FOR : FLR,FLDR                                      8161364
                                1364   *                                                               8161365
                                1365   FLRD1    EQU   *                                               8161366
 02CD                           1366            B     FLRD11       DUMMY BRANCH FOR FPP TO SETTLE      8161367
 2CD    A4 3ECE                 1367   FLRD11   L     YS,YS,FLTPT  SEND (R2) TO FPP                    8161368
 2CE    0C 4207                 1368            L     YS,YS,FLTPT                                      8161369
 2CF    0C 4207                 1369            LI    Q,0                                              8161370
 2D0    00 7100                 1370            L     Q,Q,FLTPT    SEND DUMMY HALFWORD TO FPP          8161371
 2D1    00 2007                 1371            L     Q,Q,FLTPT                                        8161372
 2D2    00 2007                 1372            B     FXR2                                             8161373
 2D3    A4 3ECB                 1373   *                                                               8161374
                                1374   * FLOATING-POINT ARITHMATIC INTERRUPT                           8161375
                                1375   *                                                               8161376
                                1376   FL.OV    EQU   *                                               8161377
 02D4                           1377            L     FLR,PSW,CS   (FLR) = PSW 4:7                     8161378
 2D4    04 7C80                 1378            BF    V,F,CC       IF BIT 5 IS DISABLED,IGNORE INT.    8161379
 2D5    A4 2EC8                 1379            NI    MR0,Q,'0F'   HOLD CC IN MR0                      8161380
 2D6    06 650F                 1380            L     Q,PSW        GET PSW                             8161381
 2D7    00 7000                 1381            N2I   Q,Q,'0F'     ZERO OUT CONDITION CODE             8161382
 2D8    02 E10F                 1382            O     PSW,Q,MR0    OR IN CURRENT CC                    8161383
 2D9    05 E020                 1383            LI    MAR,'28'                                         8161384
 2DA    04 7B28                 1384            B     GENSWP                                           8161385
 2DB    A4 3F21
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BLOCK I/O, AUTO LOAD & PSW SWAP SERVICE

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                        1386  *                                                                    8161387
                        1387  *                                                                    8161388
                        1388  * COME HERE IF SIGNS DIFFER FOR CH, CHI & CHR                        8161389
                        1389  *                                                                    8161390
 2DC    00 300C         1390  DIFFER   L     Q,YD,F          SAVE YD IN Q, SET G,L FLAGS           8161391
 2DD    1C 300A         1391           L     YD,YD,SL+CO     SET/RESET CARRY                       8161392
 2DE    CC 2000         1392           L     YD,Q,IR         SET CC.                               8161393
                        1393  *                                                                    8161394
                        1394  *  BLOCK I/O                                                         8161395
                        1395  *                                                                    8161396
                        1396  * COME HERE THRU D1 FOR  :  RBR,WBR                                  8161397
                        1397  *                                                                    8161398
 2DF    04 3E01         1398  RBRWBRD1 ADR   YD             ADDRESS THE DEVICE                    8161399
 2E0    04 7431         1399           L     MR0,YSI,CYD&SWA                                       8161400
 2E1    00 3A02         1400  BLKRR1   L     MAR&Q,YDP1      (MAR) = BLOCK START ADDRESS           8161401
 2E2    05 7425         1401           DEC   MR0,MR0                                               8161402
 2E3    A4 1EE1         1402           BF    C,BLKRR1                                              8161403
 2E4    04 3800         1403           L     MDR,YI          (MDR) = BLOCK END ADDRESS             8161404
                        1404  *                                                                    8161405
                        1405  * COMMON TO WB,RB,WBR,RBR                                           8161406
                        1406  *                                                                    8161407
 02E5                   1407  BLKIO1   EQU   *              (MAR) = BLOCK START ADDRESS           8161408
 2E5    01 6040         1408           S     Q,MDR,Q         (Q) = # OF BYTES TO BE TRANSFERRED    8161409
 2E6    00 200C         1409  BLKIO2   L     Q,Q,F           SET FLAGS HERE                        8161410
 2E7    84 38FB         1410           BT    L,FINISH                                              8161411
 2E8    40 2000         1411           L     Q,Q,MR                                                8161412
 2E9    04 7C72         1412  BLKIO3   SS    FLR                                                   8161413
 2EA    84 20FC         1413           BT    V+G+L,TERMIN    IF BAD STATUS / TIME-OUT, TERMINATE   8161414
 2EB    84 1EE9         1414           BT    C,BLKIO3        LOOP TILL BSY DROPS                   8161415
 2EC    20 2000         1415           L     Q,Q,D2          GO TRANSFER THE BYTE                  8161416
                        1416  *                                                                    8161417
                        1417  * COME HERE THRU OROM2 FOR WB & WBR                                  8161418
                        1418  *                                                                    8161419
 2ED    04 7EC4         1419  WBR      WD    MDR,CS          WRITE A BYTE TO THE DEVICE            8161420
 2EE    00 A005         1420           DEC   Q,Q             DECREMENT BYTE COUNT                  8161421
 2EF    A4 3EF3         1421           B     RB1                                                   8161422
                        1422  *                                                                    8161423
                        1423  * COME HERE THRU D2 FOR  :  RB,RBR,AL                               8161424
                        1424  *                                                                    8161425
 2F0    04 7474         1425  RBR      RD    MR0             READ A BYTE FROM DEVICE               8161426
                        1426  *                                                                    8161427
                        1427  * COME HERE FROM EMULATION SEQUENCE FOR AL                           8161428
                        1428  *                                                                    8161429
 2F1    04 78A0         1429  FROMAL   EXB   MDR,MR0                                               8161430
 2F2    60 A005         1430           DEC   Q,Q,MW          WRITE THE BYTE INTO MEMORY            8161431
 2F3    04 7A55         1431  RB1      INC   MAR,MAR                                               8161432
 2F4    A4 3EE6         1432           B     BLKIO2                                                8161433
                        1433  *                                                                    8161434
                        1434  *                                                                    8161435
 2F5                    1435           ORG   '300'                                                 8161436
                        1436  *                                                                    8161437
                        1437  *                                                                    8161438
                        1438  * ALO SUPPORT : LOAD PROGRAM FROM ALO INTO MEMORY, START EXECUTION.  8161439
                        1439  *                                                                    8161440
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BLOCK I/O, AUTO LOAD & PSW SWAP SERVICE

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                                1440  ALO1    EQU   *          THE ALO (HW DEVICE) IS ADDRESSED   8161441
                                1441  *                        ON POWER UP.                       8161442
0300                            1442        RD    PSW        GET PSW                            8161443
0301  04 7074                   1443        RD    LOC        GET LOC                            8161444
0302  04 7274                   1444        RD    MAR        (MAR) = PROGRAM START ADDRESS      8161445
0303  04 7A74                   1445        RD    YD         (YD) = PROGRAM FINAL ADDRESS       8161446
0304  0C 7074                   1446        S     YD,YD,MAR,SR+F  ((YD)) = # OF HALFWORDS IN PROGRAM 8161447
0305  14 005C                   1447        BF    G,IDLE     IF NON-POSITIVE, ABORT UNLOADING ALO 8161448
      A4 3534                   1448  *                                                         8161449
0306  04 7874                   1449  ALO2    RD    MDR        (MDR) = NEXT HW OF PROGRAM         8161450
0307  6C B005                   1450        DEC   YD,YD,MW     WRITE THAT HW INTO MEMORY          8161451
0308  04 6A50                   1451        A     MAR,Q,MAR    INCREMENT MAR BY 2                 8161452
0309  A4 1F06                   1452        BF    C,ALO2                                          8161453
                                1453  *                                                         8161454
030A  1C 700A                   1454        L     YD,PSW,SL+CO  LOOK @ PSW WAIT BIT               8161455
030B  A4 3F3C                   1455        B     EPSR3                                           8161456
                                1456  *                                                         8161457
                                1457  *                                                         8161458
                                1458  *                                                         8161459
030C  04 7471                   1459  LMEDONE ACK   MR0         DUMMY ACKNOLEDGE FOR FPP TO IDLE   8161460
030D  C4 7C00                   1460        L     FLR,PSW,IR                                      8161461
                                1461  *                                                         8161462
                                1462  * ROUTINE FOR AL                                         8161463
                                1463  *                                                         8161464
030E  84 0F10                   1464  AL1     BT    AMOD,ALX                                    8161465
030F  00 7100                   1465        LI    Q,0                                           8161466
0310  00 6040                   1466  ALX     A     Q,Q,MDR      AL TO (Q) ADDRESS              8161467
0311  04 7B78                   1467        LI    MAR,'78'                                      8161468
0312  44 7B80                   1468        LI    MAR,'80',MR  READ BINDV ENTRY @ X'78'          8161469
0313  00 E05A                   1469        S     Q,Q,MAR,CO   (Q) = # OF BYTES TO BE TRANSFERRED. 8161470
0314  84 1CFB                   1470        BT    C,FINISH     ABORT IF LESS THAN ZERO           8161471
0315  04 7EC1                   1471        ADR   MDR,CS       ADDRESS THE DEVICE                8161472
0316  04 7E42                   1472        OC    MDR          SET UP THE DEVICE                 8161473
                                1473  *                                                         8161474
0317  04 7C72                   1474  LEADER  SS    FLR                                         8161475
0318  84 20FC                   1475        BT    V+G+L,TERMIN TERMINATE IF BAD STATUS/TIME-OUT   8161476
0319  84 1F17                   1476        BT    C,LEADER     LOOP TILL BSY DROPS               8161477
031A  04 7474                   1477        RD    MR0                                           8161478
031B  44 742C                   1478        L     MR0,MR0,F+MR                                  8161479
031C  84 36F1                   1479        BT    G,FROMAL     NON-ZERO BYTE IS READ             8161480
031D  A4 3F17                   1480        B     LEADER       LOOP                              8161481
                                1481  *                                                         8161482
                                1482  * MACHINE MALFUNCTION DETECTED                           8161483
                                1483  *                                                         8161484
031E                            1484  MMALF   EQU   *                                           8161485
031E  84 F538                   1485        BT    PPF,PWRDWN   PRIMARY POWER FAIL                8161486
031F  84 AD5F                   1486        BT    CATN,CONSER  TO EXIT IF MICROPROGRAM HANGS UP  8161487
                                1487  *                        IN MACHINE MALFUNCTION PSW SWAPS  8161488
0320  04 7B38                   1488  MMALF1  LI    MAR,OMMPSW                                  8161489
                                1489  *                                                         8161490
                                1490  * COMMON PSW SWAP ROUTINE                                 8161491
                                1491  *                                                         8161492
0321  04 3400                   1492  GENSWP  L     MR0,YD       SAVE YD IN MR0                 8161493
                                1493  *                                                         8161494
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BLOCK I/O, AUTO LOAD & PSW SWAP SERVICE

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 322   04 7800   1494  QUEINT  L    MDR,PSW                          8161495
 323   00 7102   1495          LI   Q,2                              8161496
 324   64 6A50   1496          A    MAR,Q,MAR,MW   SAVE OLD PSW      8161497
 325   04 7810   1497          L    MDR,LOC                          8161498
 326   64 6A50   1498          A    MAR,Q,MAR,MW   SAVE OLD LOC      8161499
 327   4C 7101   1499          LI   YD,1,MR                          8161500
 328   A4 BB2C   1500          BF   MALF,LPSW1                       8161501
                 1501  *                                            8161502
 329   84 FB2B   1502          BT   MPE,LSET                         8161503
 32A   05 0840   1503          O    MDR,YD,MDR     OR IN L FLAG      8161504
 32B   04 7100   1504  LSET    LI   PSW,0          RESET MPE & EPF   8161505
                 1505  *                                            8161506
 032C            1506  LPSW1   EQU  *              FROM LPSW         8161507
 32C   04 7040   1507          L    PSW,MDR        NEW PSW           8161508
 32D   04 6A50   1508          A    MAR,Q,MAR                        8161509
 32E   40 2000   1509          L    Q,Q,MR                           8161510
 32F   04 7240   1510          L    LOC,MDR        NEW LOC           8161511
 0330            1511  EPSR1   EQU  *              FROM EPSR         8161512
 330   04 7C80   1512          L    FLR,PSW,CS     LOOK @ PSW06      8161513
 331   A4 373A   1513          BF   G,EPSR2                          8161514
                 1514  *                                            8161515
 0332            1515  QUENBL  EQU  *                               8161516
 332   84 AF3A   1516          BT   CATN,EPSR2     TO EXIT IF MICROPROGRAM HANGS UP 8161517
                 1517  *                          IN QUEUE SERVICE PSW SWAPS       8161518
 333   04 7B80   1518          LI   MAR,'80'                         8161519
 334   44 7D00   1519          LI   FLR,0,MR                         8161520
 335   04 7A40   1520          L    MAR,MDR        (MAR) = QUEUE ADDRESS 8161521
 336   44 7B82   1521          LI   MAR,'82',MR                      8161522
 337   0C 71FF   1522          LI   YD,'FF'                          8161523
 338   0E 504C   1523          N    YD,YD,MDR,F    SEE IF LIST IS EMPTY 8161524
 339   84 3722   1524          BT   G,QUEINT       TAKE QUEUE SERVICE INTERRUPT 8161525
                 1525  *                                            8161526
 33A   1C 700A   1526  EPSR2   L    YD,PSW,SL+CO   CARRY = PSW00     8161527
 33B   0C 7020   1527          L    YD,MR0         RESTORE YD        8161528
                 1528  *                                            8161529
 33C   84 1059   1529  EPSR3   BT   C,WAIT                          8161530
 33D   C4 7C00   1530          L    FLR,PSW,IR     DO USER'S INSTRUCTION 8161531
 33E             1531          END                                  8161532
```

BLOCK I/O, AUTO LOAD & PSW SWAP SERVICE

NO ERRORS

ABLD2	0267				
ACH	008D				
ADD	0195	862			
ADDWRT	018B	814			
AHM	0088				
AHR	008E				
AI	0004				
AIR	00D7				
AL	000B				
AL1	030E	69			
ALO1	0300	649			
ALO2	0306	1452			
ALOC	0026	655	732		
ALX	0310	1464			
APSW	0024	654	730		
ATL1	0253	1163			
ATL2	0262	1196	1198		
ATLABLI	007E				
ATLABLD1	0251	296			
ATLD2	025E				
BALR	009F				
BECR	00A4				
BFS	00A8				
BKWORD	00AC				
BLKIO1	02E5	170			
BLKIO2	02E6	1432			
BLKIO3	02E9	1414			
BLKRR1	02E1	1402			
BRANCH	00A0	413	418		
BTCR	00A2				
BTS	00A6				
BX	0012				
BX1	00B2	453			
BXH	00AF				
BXLE	00B1				
BXNOB	00B4	459			
BXNX	0014	87			
CDD2	02B8				
CER	00E1				
CERD1	02BE	595			
CHR	0097				
CLB	00B9				
CLHR	0099				
CLRWT	0175	783	835	855	
CONINT	01EB	854			
CONSER	015F	885	1486		
CONTIN	017F	810			
DHR	00DB				
DHR1	0200	570			
DIFFER	02DC	377			
DISPLY	019D	780	848	850	
EPSR	00D0				
EPSR1	0330	531			

BLOCK I/O, AUTO LOAD & PSW SWAP SERVICE

LMDD2	028B	328						
LME	0091							
LMED2	0291	352						
LMEDONE	030C	1271						
LMNX	000E	77						
LMST*	000C							
LOCDIS	012C	702	876	929	934	959	993	
LOOK20	01BB	904						
LPSW	00CE							
LPSW1	032C	524	1500					
LSET	032B	1502						
MAR0	012E	938	955					
MHR	00DC							
MHR1	0232	574						
MHUR	00DD							
MHUR1	0248	578						
MMALF	031E	883						
MMALF1	0320	834						
MMF	0179	706						
MRONES	0207	1040						
MROPOS	0205							
NHR	0092							
NLONG	0067	616						
NNEG1	0238	1118						
NNEG2	023C	1122						
NOB	00A1	432	509	518	886	1289		
NOWRAP1	0261	1180						
NOWRAP4	0284	1233						
OC	002E							
OCR	002F							
OHR	0093							
OIPSW	0040							
OMMPSW	0038	1488						
OUTOIS	012F	871	990					
OV	0225	1058	1079					
OV1	022A	1041	1093					
PNTR	0022	659	734					
POW	0157	758	772					
PSWLOC	0186	907						
PWRDWN	0138	1485						
PWRDWN2	014D	745						
PWRUP	0100							
PWRUP2	0119	669						
PWRUP3	0125	683						
QNEG	0222	1077						
QOK	021F	1088						
QOK1	024F	1137						
QUEINT	0322	1106	1524					
QUENBL	0332							
RB1	02F3	1421						
RDLO2	027F							
RBR	02F0							
RBRWBR	00DA							
RBRWBRD1	02DF	564						

RBWB	0034						
RBWBNX	0038	163					
RD	0018						
RD2	0019	112	138	319			
RDKEY	018F	815					
RDR	0023	116					
REGDIS	C1BF						
REGN	C1C0	952					
RH	001B						
RHH	001E	108					
RHR	0021						
RLLD2	005A						
RNNEG	021B	1073					
RRLD2	006B						
RS	0002						
RSNX	000A	41					
RTL1	026F	1203					
RTL2	0285	1223	1225				
RTLD2	0278						
RTLRBL	007F						
RTLRBLD1	026D	300					
RX	0006						
RXNX	0008	61					
SAVREG	0140	741					
SCH	008F						
SHIFTD	00E6	190					
SHORTB	00A9	427					
SHR	0090						
SINT	0080						
SINT1	01ED	307					
SINT2	01F6	822					
SLA	004D						
SLAD2	0074						
SLHA	0047						
SLHA1	0048	205					
SLHAD2	005D						
SLHL	003D						
SLHL2	003E	197	210				
SLHL8	003F	200					
SLHLD2	0051						
SLHLNX	0042	183					
SLL	004F						
SLL1D2	0056	231	257	263	280	618	
SLLD2	0054						
SLLS	00D4						
SRAD2	006E						
SRHAD2	0061						
SRHL1	0065	244					
SRHLD2	0064						
SRL1D2	0069	269					
SRLD2	0068						
SS	0029						
SSR	002C						
START	0000						

PROG= M816DF01 ASSEMBLED BY MICROCAL II (32-BIT)

```
0001                    2    F.VARI   EQU   1                    F01 : BASIC
                        3    *
                        4             NLSTC
                        5    *
                        6             SQCHK
                        7    *
                        8    *
                        9    * SET UP SYSGEN PARAMETERS
                       10    *
                       13             ELSE
0000                   14    MPY.DIV  EQU   0
                       15             ENDC
                       18             ELSE
0000                   19    SPFP     EQU   0
                       20             ENDC
                       23             ELSE
0000                   24    DPFP     EQU   0
                       25             ENDC
                       26    *
                       27    *
                       28    *
                       29    *
                       30    * COPYRIGHT INTERDATA INC.   SEPTEMBER  1976
                       31    *
                       32    *
                       33    * DHEMA MAHAJAN
                       34    *
                       35    *
                       36    * DROM SOURCE IS ASSEMBLED IN CONJUNCTION WITH THE MICROPROGRAM SOURCE
                       37    * OPERAND FIELD IS THE SYMBOLIC ROM ENTRY POINT FOR D1
                       38    * COMMENT FIELD SHOWS OP-CODE AND VALID INSTRUCTION MNEMONIC
                       39    * ONLY THE LEAST SIGNIFICANT BYTE OF THE CODE GENERATED IS USED
                       40             PARTS 19-186R00F00        DUMMY PART #
                       41             PARTS 19-186R00F00        DUMMY PART #
                       42    * THE DROM DATA IS CONTAINED IN THE FOLLOWING 512 X 8 (4K) ROM CHIP
                       43    *
000                    44             IFZ   F.VARI-1
                       45             PARTS 19-186R00F27
                       46             ENDC
                       49             ENDC
                       52             ENDC
                       55             ENDC
                       56    *
000    00 009B         57             DC    ILEG              00
001    00 009F         58             DC    BALR              01  BALR
002    00 00A2         59             DC    BTCR              02  BTCR
003    00 00A4         60             DC    BFCR              03  BFCR
004    00 0092         61             DC    NHR               04  NHR
005    00 0099         62             DC    CLHR              05  CLHR
006    00 0093         63             DC    OHR               06  OHR
007    00 0094         64             DC    XHR               07  XHR
008    00 0095         65             DC    LHR               08  LHR
009    00 0097         66             DC    CHR               09  CHR
00A    00 008E         67             DC    AHR               0A  AHR
```

```
00B     00 0090          68          DC    SHR                 0B  SHR      0816067
00C                      69          IFZ   MPY,DIV                        0816068
00C     00 009B          70          DC    ILEG                0C           0816069
00D     00 009B          71          DC    ILEG                0D           0816070
                         72          ENDC                                   0816071
                         74          ENDC                                   0816075
00E     00 008D          77          DC    ACH                 0E  ACHR     0816076
00F     00 008F          78          DC    SCH                 0F  SCHR     0816077
                         79    *                                            0816078
                         80    * OP-CODES  10 - 1F  ARE ILLEGAL             0816079
                         81    *                                            0816080
010     00 009B          82          DC    ILEG                             0816081
011     00 009B          83          DC    ILEG                             0816082
012     00 009B          84          DC    ILEG                             0816083
013     00 009B          85          DC    ILEG                             0816084
014     00 009B          86          DC    ILEG                             0816085
015     00 009B          87          DC    ILEG                             0816086
016     00 009B          88          DC    ILEG                             0816087
017     00 009B          89          DC    ILEG                             0816088
018     00 009B          90          DC    ILEG                             0816089
019     00 009B          91          DC    ILEG                             0816090
01A     00 009B          92          DC    ILEG                             0816091
01B     00 009B          93          DC    ILEG                             0816092
01C     00 009B          94          DC    ILEG                             0816093
01D     00 009B          95          DC    ILEG                             0816094
01E     00 009B          96          DC    ILEG                             0816095
01F     00 009B          97          DC    ILEG                             0816096
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020  00 00A6   99          DC   BTS    20  BTBS   0816098
021  00 00A6  100          DC   BTS    21  BTFS   0816099
022  00 00A8  101          DC   BFS    22  BFBS   0816100
023  00 00A8  102          DC   BFS    23  BFFS   0816101
024  00 008C  103          DC   IMM    24  LIS    0816102
025  00 0096  104          DC   LCS    25  LCS    0816103
026  00 008C  105          DC   IMM    26  AIS    0816104
027  00 008C  106          DC   IMM    27  SIS    0816105
028           107          IFZ  SPFP               0816106
028  00 009B  108          DC   ILEG   28         0816107
029  00 009B  109          DC   ILEG   29         0816108
02A  00 009B  110          DC   ILEG   2A         0816109
02B  00 009B  111          DC   ILEG   2B         0816110
02C  00 009B  112          DC   ILEG   2C         0816111
02D  00 009B  113          DC   ILEG   2D         0816112
02E  00 009B  114          DC   ILEG   2E         0816113
02F  00 009B  115          DC   ILEG   2F         0816114
              116          ENDC                    0816115
              126          ENDC                    0816125
              127          IFZ  DPFP               0816126
030           128  *                               0816127
              129  * OP-CODES  30 - 3F  ARE ILLEGAL 0816128
              130  *                               0816129
030  00 009B  131          DC   ILEG               0816130
031  00 009B  132          DC   ILEG               0816131
032  00 009B  133          DC   ILEG               0816132
033  00 009B  134          DC   ILEG               0816133
034  00 009B  135          DC   ILEG               0816134
035  00 009B  136          DC   ILEG               0816135
036  00 009B  137          DC   ILEG               0816136
037  00 009B  138          DC   ILEG               0816137
038  00 009B  139          DC   ILEG               0816138
039  00 009B  140          DC   ILEG               0816139
03A  00 009B  141          DC   ILEG               0816140
03B  00 009B  142          DC   ILEG               0816141
03C  00 009B  143          DC   ILEG               0816142
03D  00 009B  144          DC   ILEG               0816143
03E  00 009B  145          DC   ILEG               0816144
03F  00 009B  146          DC   ILEG               0816145
              147          ENDC                    0816146
              165          ENDC                    0816164
```

```
040  00 0002  167          DC   RS          40  STH  0816166
041  00 0002  168          DC   RS          41  BAL  0816167
042  00 0002  169          DC   RS          42  BTC  0816168
043  00 0002  170          DC   RS          43  BFC  0816169
044  00 0006  171          DC   RX          44  NH   0816170
045  00 0006  172          DC   RX          45  CLH  0816171
046  00 0006  173          DC   RX          46  OH   0816172
047  00 0006  174          DC   RX          47  XH   0816173
048  00 0006  175          DC   RX          48  LH   0816174
049  00 0006  176          DC   RX          49  CH   0816175
04A  00 0006  177          DC   RX          4A  AH   0816176
04B  00 0006  178          DC   RX          4B  SH   0816177
04C           179          IFZ  MPY,DIV              0816178
04C  00 009B  180          DC   ILEG        4C        0816179
04D  00 009B  181          DC   ILEG.       4D        0816180
              182          ENDC                       0816181
              186          ENDC                       0816185
04E  00 0006  187          DC   RX          4E  ACH  0816186
04F  00 0006  188          DC   RX          4F  SCH  0816187
              189    *                               0816188
              190    * OP-CODES  50 - 5F  ARE ILLEGAL 0816189
              191    *                               0816190
050  00 009B  192          DC   ILEG                  0816191
051  00 009B  193          DC   ILEG                  0816192
052  00 009B  194          DC   ILEG                  0816193
053  00 009B  195          DC   ILEG                  0816194
054  00 009B  196          DC   ILEG                  0816195
055  00 009B  197          DC   ILEG                  0816196
056  00 009B  198          DC   ILEG                  0816197
057  00 009B  199          DC   ILEG                  0816198
058  00 009B  200          DC   ILEG                  0816199
059  00 009B  201          DC   ILEG                  0816200
05A  00 009B  202          DC   ILEG                  0816201
05B  00 009B  203          DC   ILEG                  0816202
05C  00 009B  204          DC   ILEG                  0816203
05D  00 009B  205          DC   ILEG                  0816204
05E  00 009B  206          DC   ILEG                  0816205
05F  00 009B  207          DC   ILEG                  0816206
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 060                   209          IFZ  SPFP                               D816208
 060       00 009B     210          DC   ILEG       60                      D816209
                       211          ENDC                                    D816210
                       214          ENDC                                    D816213
 061       00 0006     215          DC   RX         61  AHM                 D816214
 062       00 009B     216          DC   ILEG       62                      D816215
 063       00 009B     217          DC   ILEG       63                      D816216
 064       00 007E     218          DC   ATLABL     64  ATL                 D816217
 065       00 007E     219          DC   ATLABL     65  ABL                 D816218
 066       00 007F     220          DC   RTLRBL     66  RTL                 D816219
 067       00 007F     221          DC   RTLRBL     67  RBL                 D816220
 068                   222          IFZ  SPFP                               D816221
 068       00 009B     223          DC   ILEG       68                      D816222
 069       00 009B     224          DC   ILEG       69                      D816223
 06A       00 009B     225          DC   ILEG       6A                      D816224
 06B       00 009B     226          DC   ILEG       6B                      D816225
 06C       00 009B     227          DC   ILEG       6C                      D816226
 06D       00 009B     228          DC   ILEG       6D                      D816227
                       229          ENDC                                    D816228
                       237          ENDC                                    D816236
 06E       00 009B     238          DC   ILEG       6E                      D816237
 06F       00 009B     239          DC   ILEG       6F                      D816238
                       240     *                                            D816239
                       241     *                                            D816240
 070                   242          IFZ  DPFP                               D816241
 070       00 009B     243          DC   ILEG       70                      D816242
                       244          ENDC                                    D816243
                       247          ENDC                                    D816246
 071                   248          IFZ  SPFP                               D816247
 071       00 009B     249          DC   ILEG       71                      D816248
 072       00 009B     250          DC   ILEG       72                      D816249
                       251          ENDC                                    D816250
                       255          ENDC                                    D816254
 073       00 009B     256          DC   ILEG       73                      D816255
 074       00 009B     257          DC   ILEG       74                      D816256
 075       00 009B     258          DC   ILEG       75                      D816257
 076       00 009B     259          DC   ILEG       76                      D816258
 077       00 009B     260          DC   ILEG       77                      D816259
 078                   261          IFZ  DPFP                               D816260
 078       00 009B     262          DC   ILEG       78                      D816261
 079       00 009B     263          DC   ILEG       79                      D816262
 07A       00 009B     264          DC   ILEG       7A                      D816263
 07B       00 009B     265          DC   ILEG       7B                      D816264
 07C       00 009B     266          DC   ILEG       7C                      D816265
 07D       00 009B     267          DC   ILEG       7D                      D816266
 07E       00 009B     268          DC   ILEG       7E                      D816267
 07F       00 009B     269          DC   ILEG       7F                      D816268
                       270          ENDC                                    D816269
                       280          ENDC                                    D816279
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```
                                  282  *
                                  283  * OP-CODES  80 - 8F  ARE ILLEGAL
                                  284  *
080     00 009B                   285          DC    ILEG
081     00 009B                   286          DC    ILEG
082     00 009B                   287          DC    ILEG
083     00 009B                   288          DC    ILEG
084     00 009B                   289          DC    ILEG
085     00 009B                   290          DC    ILEG
086     00 009B                   291          DC    ILEG
087     00 009B                   292          DC    ILEG
088     00 009B                   293          DC    ILEG
089     00 009B                   294          DC    ILEG
08A     00 009B                   295          DC    ILEG
08B     00 009B                   296          DC    ILEG
08C     00 009B                   297          DC    ILEG
08D     00 009B                   298          DC    ILEG
08E     00 009B                   299          DC    ILEG
08F     00 009B                   300          DC    ILEG
                                  301  *
                                  302  *
090     00 00D4                   303          DC    SLLS          90  SRLS
091     00 00D4                   304          DC    SLLS          91  SLLS
092     00 00C0                   305          DC    STBR          92  STBR
093     00 00B6                   306          DC    LBR           93  LBR
094     00 00C5                   307          DC    EXBR          94  EXBR
095     00 00D0                   308          DC    EPSR          95  EPSR
096     00 00DA                   309          DC    RBRWBR        96  WBR
097     00 00DA                   310          DC    RBRWBR        97  RBR
098     00 00D8                   311          DC    IORR          98  WHR
099     00 00D8                   312          DC    IORR          99  RHR
09A     00 00D8                   313          DC    IORR          9A  WDR
09B     00 00D8                   314          DC    IORR          9B  RDR
09C                               315          IFZ   MPY.DIV
09C     00 009B                   316          DC    ILEG          9C
                                  317          ENDC
                                  320          ENDC
09D     00 00D8                   321          DC    IORR          9D  SSR
09E     00 00D8                   322          DC    IORR          9E  OCR
09F     00 00D7                   323          DC    AIR           9F  AIR
```

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0816281
0816282
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0816307
0816308
0816309
0816310
0816311
0816312
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0816315
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0816319
0816320
0816321
0816322
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                                  325     *
                                  326     * OP-CODES  A0 - AF  ARE ILLEGAL
                                  327     *
0A0     00 009B                   328             DC    ILEG
0A1     00 009B                   329             DC    ILEG
0A2     00 009B                   330             DC    ILEG
0A3     00 009B                   331             DC    ILEG
0A4     00 009B                   332             DC    ILEG
0A5     00 009B                   333             DC    ILEG
0A6     00 009B                   334             DC    ILEG
0A7     00 009B                   335             DC    ILEG
0A8     00 009B                   336             DC    ILEG
0A9     00 009B                   337             DC    ILEG
0AA     00 009B                   338             DC    ILEG
0AB     00 009B                   339             DC    ILEG
0AC     00 009B                   340             DC    ILEG
0AD     00 009B                   341             DC    ILEG
0AE     00 009B                   342             DC    ILEG
0AF     00 009B                   343             DC    ILEG
                                  344     *
                                  345     * OP-CODES  B0 - BF  ARE ILLEGAL
                                  346     *
0B0     00 009B                   347             DC    ILEG
0B1     00 009B                   348             DC    ILEG
0B2     00 009B                   349             DC    ILEG
0B3     00 009B                   350             DC    ILEG
0B4     00 009B                   351             DC    ILEG
0B5     00 009B                   352             DC    ILEG
0B6     00 009B                   353             DC    ILEG
0B7     00 009B                   354             DC    ILEG
0B8     00 009B                   355             DC    ILEG
0B9     00 009B                   356             DC    ILEG
0BA     00 009B                   357             DC    ILEG
0BB     00 009B                   358             DC    ILEG
0BC     00 009B                   359             DC    ILEG
0BD     00 009B                   360             DC    ILEG
0BE     00 009B                   361             DC    ILEG
0BF     00 009B                   362             DC    ILEG
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D816324
D816325
D816326
D816327
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0C0   00 0012    364          DC   BX          C0  EXH    0816363
0C1   00 0012    365          DC   BX          C1  BXLE   0816364
0C2   00 0006    366          DC   RX          C2  LPSW   0816365
0C3   00 0002    367          DC   RS          C3  THI    0816366
0C4   00 0002    368          DC   RS          C4  NHI    0816367
0C5   00 0002    369          DC   RS          C5  CLHI   0816368
0C6   00 0002    370          DC   RS          C6  OHI    0816369
0C7   00 0002    371          DC   RS          C7  XHI    0816370
0C8   00 0002    372          DC   RS          C8  LHI    0816371
0C9   00 0002    373          DC   RS          C9  CHI    0816372
0CA   00 0002    374          DC   RS          CA  AHI    0816373
0CB   00 0002    375          DC   RS          CB  SHI    0816374
0CC   00 003D    376          DC   SLHL        CC  SRHL   0816375
0CD   00 004D    377          DC   SLHL        CD  SLHL   0816376
0CE   00 0047    378          DC   SLHA        CE  SRHA   0816377
0CF   00 0047    379          DC   SLHA        CF  SLHA   0816378
                 380    *                                 0816379
                 381    *                                 0816380
0D0   00 000C    382          DC   LMSTM       D0  STM    0816381
0D1   00 000C    383          DC   LMSTM       D1  LM     0816382
0D2   00 0006    384          DC   RX          D2  STB    0816383
0D3   00 0006    385          DC   RX          D3  LB     0816384
0D4   00 0006    386          DC   RX          D4  CLB    0816385
0D5   00 000B    387          DC   AL          D5  AL     0816386
0D6   00 0034    388          DC   RBWB        D6  WB     0816387
0D7   00 0034    389          DC   RBWB        D7  RB     0816388
0D8   00 0005    390          DC   IORX        D8  WH     0816389
0D9   00 0005    391          DC   IORX        D9  RH     0816390
0DA   00 0005    392          DC   IORX        DA  WD     0816391
0DB   00 0005    393          DC   IORX        DB  RD     0816392
0DC              394          IFZ  MPY.DIV                0816393
0DC   00 009B    395          DC   ILEG        DC         0816394
                 396          ENDC                        0816395
                 399          ENDC                        0816398
0DD   00 0005    400          DC   IORX        DD  SS     0816399
0DE   00 0005    401          DC   IORX        DE  OC     0816400
0DF   00 0004    402          DC   AI          DF  AI     0816401
```

```
0E0   00 009B   404          DC   ILEG        E0          0816403
0E1   00 0002   405          DC   RS          E1  SVC     0816404
0E2   00 0002   406          DC   RS          E2  SINT    0816405
0E3   00 009B   407          DC   ILEG        E3          0816406
0E4   00 009B   408          DC   ILEG        E4          0816407
0E5   00 009B   409          DC   ILEG        E5          0816408
0E6   00 009B   410          DC   ILEG        E6          0816409
0E7   00 009B   411          DC   ILEG        E7          0816410
0E8   00 009B   412          DC   ILEG        E8          0816411
0E9   00 009B   413          DC   ILEG        E9          0816412
0EA   00 004F   414          DC   SLL         EA  RRL     0816413
0EB   00 004F   415          DC   SLL         EB  RLL     0816414
0EC   00 004F   416          DC   SLL         EC  SRL     0816415
0ED   00 004F   417          DC   SLL         ED  SLL     0816416
0EE   00 004D   418          DC   SLA         EE  SRA     0816417
0EF   00 004D   419          DC   SLA         EF  SLA     0816418
                420     *                                 0816419
                421     * OP-CODES  F0 - FF  ARE ILLEGAL   0816420
                422     *                                 0816421
0F0   00 009B   423          DC   ILEG                    0816422
0F1   00 009B   424          DC   ILEG                    0816423
0F2   00 009B   425          DC   ILEG                    0816424
0F3   00 009B   426          DC   ILEG                    0816425
0F4   00 009B   427          DC   ILEG                    0816426
0F5   00 009B   428          DC   ILEG                    0816427
0F6   00 009B   429          DC   ILEG                    0816428
0F7   00 009B   430          DC   ILEG                    0816429
0F8   00 009B   431          DC   ILEG                    0816430
0F9   00 009B   432          DC   ILEG                    0816431
0FA   00 009B   433          DC   ILEG                    0816432
0FB   00 009B   434          DC   ILEG                    0816433
0FC   00 009B   435          DC   ILEG                    0816434
0FD   00 009B   436          DC   ILEG                    0816435
0FE   00 009B   437          DC   ILEG                    0816436
0FF   00 009B   438          DC   ILEG                    0816437
```

MODEL 8/16 DROM2 DATA

```
                      440   *                                                    0816439
                      441   *                                                    0816440
 100    00 0000       442            DC     0             00                     0816441
 101    00 0000       443            DC     0             01  BALR               0816442
 102    00 0000       444            DC     0             02  STCR               0816443
 103    00 0000       445            DC     0             03  BFCR               0816444
 104    00 0000       446            DC     0             04  NHR                0816445
 105    00 0000       447            DC     0             05  CLHR               0816446
 106    00 0000       448            DC     0             06  OHR                0816447
 107    00 0000       449            DC     0             07  XHR                0816448
 108    00 0000       450            DC     0             08  LHR                0816449
 109    00 0000       451            DC     0             09  CHR                0816450
 10A    00 0000       452            DC     0             0A  AHR                0816451
 10B    00 0000       453            DC     0             0B  SHR                0816452
 10C                  454            IFZ    MPY.DIV                              0816453
 10C    00 0000       455            DC     0             0C                     0816454
 10D    00 0000       456            DC     0             0D                     0816455
                      457            ENDC                                        0816456
                      461            ENDC                                        0816460
 10E    00 0000       462            DC     0             0E  ACHR               0816461
 10F    00 0000       463            DC     0             0F  SCHR               0816462
                      464   *                                                    0816463
                      465   * OP-CODES  10 - 1F  ARE ILLEGAL                     0816464
                      466   *                                                    0816465
 110    00 0000       467            DC     0                                    0816466
 111    00 0000       468            DC     0                                    0816467
 112    00 0000       469            DC     0                                    0816468
 113    00 0000       470            DC     0                                    0816469
 114    00 0000       471            DC     0                                    0816470
 115    00 0000       472            DC     0                                    0816471
 116    00 0000       473            DC     0                                    0816472
 117    00 0000       474            DC     0                                    0816473
 118    00 0000       475            DC     0                                    0816474
 119    00 0000       476            DC     0                                    0816475
 11A    00 0000       477            DC     0                                    0816476
 11B    00 0000       478            DC     0                                    0816477
 11C    00 0000       479            DC     0                                    0816478
 11D    00 0000       480            DC     0                                    0816479
 11E    00 0000       481            DC     0                                    0816480
 11F    00 0000       482            DC     0                                    0816481
```

MODEL 8/16 DROM2 DATA

```
0120 00 00AC  484          DC    BKWORD      20  BTBS    0816483
0121 00 00AD  485          DC    FRWORD      21  FTFS    0816484
0122 00 00AC  486          DC    BKWORD      22  BFBS    0816485
0123 00 00AD  487          DC    FRWORD      23  FFFS    0816486
0124 00 0095  488          DC    LHP         24  LIS     0816487
0125 00 0000  489          DC    0           25  LCS     0816488
0126 00 006E  490          DC    AHR         26  AIS     0816489
0127 00 0090  491          DC    SHR         27  SIS     0816490
0128          492          IFZ   SPFP                    0816491
0128 00 0000  493          DC    0           28          0816492
0129 00 0000  494          DC    0           29          0816493
012A 00 0000  495          DC    0           2A          0816494
012B 00 0000  496          DC    0           2B          0816495
012C 00 0000  497          DC    0           3C          0816496
012D 00 0000  498          DC    0           2D          0816497
012E 00 0000  499          DC    0           3E          0816498
012F 00 0000  500          DC    0           2F          0816499
              501          ENDC                          0816500
              511          ENDC                          0816510
0130          512          IFZ   DPFP                    0816511
              513    *                                    0816512
              514    * OP-CODES  30 - 3F  ARE ILLEGAL     0816513
              515    *                                    0816514
0130 00 0000  516          DC    0                       0816515
0131 00 0000  517          DC    0                       0816516
0132 00 0000  518          DC    0                       0816517
0133 00 0000  519          DC    0                       0816518
0134 00 0000  520          DC    0                       0816519
0135 00 0000  521          DC    0                       0816520
0136 00 0000  522          DC    0                       0816521
0137 00 0000  523          DC    0                       0816522
0138 00 0000  524          DC    0                       0816523
0139 00 0000  525          DC    0                       0816524
013A 00 0000  526          DC    0                       0816525
013B 00 0000  527          DC    0                       0816526
013C 00 0000  528          DC    0                       0816527
013D 00 0000  529          DC    0                       0816528
013E 00 0000  530          DC    0                       0816529
013F 00 0000  531          DC    0                       0816530
              532          ENDC                          0816531
              550          ENDC                          0816549
```

MODEL 8/16 DROM2 DATA

```
140   00 0084   552          DC    STH          40  STH     0816551
141   00 009F   553          DC    BALR         41  BALR    0816552
142   00 00A2   554          DC    BTCR         42  BTCR    0816553
143   00 00A4   555          DC    BFCR         43  BFCR    0816554
144   00 0092   556          DC    NHR          44  NH      0816555
145   00 0099   557          DC    CLHR         45  CLH     0816556
146   00 0093   558          DC    OHR          46  OH      0816557
147   00 0094   559          DC    XHR          47  XH      0816558
148   00 0095   560          DC    LHR          48  LH      0816559
149   00 0097   561          DC    CHR          49  CH      0816560
14A   00 008E   562          DC    AHR          4A  AH      0816561
14B   00 0090   563          DC    SHR          4B  SH      0816562
14C             564          IFZ   MPY.DIV                  0816563
14C   00 0000   565          DC    0            4C          0816564
14D   00 0000   566          DC    0            4D          0816565
                567          ENDC                           0816566
                571          ENDC                           0816570
14E   00 008D   572          DC    ACH          4E  ACH     0816571
14F   00 008F   573          DC    SCH          4F  SCH     0816572
                574    *                                    0816573
                575    * OP-CODES  50 - 5F  ARE ILLEGAL     0816574
                576    *                                    0816575
150   00 0000   577          DC    0                        0816576
151   00 0000   578          DC    0                        0816577
152   00 0000   579          DC    0                        0816578
153   00 0000   580          DC    0                        0816579
154   00 0000   581          DC    0                        0816580
155   00 0000   582          DC    0                        0816581
156   00 0000   583          DC    0                        0816582
157   00 0000   584          DC    0                        0816583
158   00 0000   585          DC    0                        0816584
159   00 0000   586          DC    0                        0816585
15A   00 0000   587          DC    0                        0816586
15B   00 0000   588          DC    0                        0816587
15C   00 0000   589          DC    0                        0816588
15D   00 0000   590          DC    0                        0816589
15E   00 0000   591          DC    0                        0816590
15F   00 0000   592          DC    0                        0816591
```

MODEL 8/16 DROM2 DATA

```
160              594        IFZ   SPFP                        D816593
160   00 0000    595        DC    0         60                D816594
                 596        ENDC                              D816595
                 599        ENDC                              D816598
161   00 0088    600        DC    AHM       61   AHM          D816599
162   00 0000    601        DC    0         62                D816600
163   00 0000    602        DC    0         63                D816601
164   00 025E    603        DC    ATLD2     64   ATL          D816602
165   00 0267    604        DC    ABLD2     65   ABL          D816603
166   00 0278    605        DC    RTLD2     66   RTL          D816604
167   00 027F    606        DC    RBLD2     67   RBL          D816605
168              607        IFZ   SPFP                        D816606
168   00 0000    608        DC    0         68                D816607
169   00 0000    609        DC    0         69                D816608
16A   00 0000    610        DC    0         6A                D816609
16B   00 0000    611        DC    0         6B                D816610
16C   00 0000    612        DC    0         6C                D816611
16D   00 0000    613        DC    0         6D                D816612
                 614        ENDC                              D816613
                 622        ENDC                              D816621
16E   00 0000    623        DC    0         6E                D816622
16F   00 0000    624        DC    0         6F                D816623
                 625   *                                      D816624
                 626   *                                      D816625
170              627        IFZ   DPFP                        D816626
170   00 0000    628        DC    0                           D816627
                 629        ENDC                              D816628
                 632        ENDC                              D816631
171              633        IFZ   SPFP                        D816632
171   00 0000    634        DC    0                           D816633
172   00 0000    635        DC    0                           D816634
                 636        ENDC                              D816635
                 640        ENDC                              D816639
173   00 0000    641        DC    0                           D816640
174   00 0000    642        DC    0                           D816641
175   00 0000    643        DC    0                           D816642
176   00 0000    644        DC    0                           D816643
177   00 0000    645        DC    0                           D816644
178              646        IFZ   DPFP                        D816645
178   00 0000    647        DC    0                           D816646
179   00 0000    648        DC    0                           D816647
17A   00 0000    649        DC    0                           D816648
17B   00 0000    650        DC    0                           D816649
17C   00 0000    651        DC    0                           D816650
17D   00 0000    652        DC    0                           D816651
17E   00 0000    653        DC    0                           D816652
17F   00 0000    654        DC    0                           D816653
                 655        ENDC                              D816654
                 665        ENDC                              D816664
```

MODEL 8/16 DROM2 DATA

```
                                  667  *                                                                    0816666
                                  668  * OP-CODES  80 - 8F  ARE ILLEGAL                                     0816667
                                  669  *                                                                    0816668
180      00 0000                  670          DC     0                                                    0816669
181      00 0000                  671          DC     0                                                    0816670
182      00 0000                  672          DC     0                                                    0816671
183      00 0000                  673          DC     0                                                    0816672
184      00 0000                  674          DC     0                                                    0816673
185      00 0000                  675          DC     0                                                    0816674
186      00 0000                  676          DC     0                                                    0816675
187      00 0000                  677          DC     0                                                    0816676
188      00 0000                  678          DC     0                                                    0816677
189      00 0000                  679          DC     0                                                    0816678
18A      00 0000                  680          DC     0                                                    0816679
18B      00 0000                  681          DC     0                                                    0816680
18C      00 0000                  682          DC     0                                                    0816681
18D      00 0000                  683          DC     0                                                    0816682
18E      00 0000                  684          DC     0                                                    0816683
18F      00 0000                  685          DC     0                                                    0816684
                                  686  *                                                                    0816685
                                  687  *                                                                    0816686
190      00 0064                  688          DC     SRHLD2          90  SRLS                             0816687
191      00 0051                  689          DC     SLHLD2          91  SLLS                             0816688
192      00 00A1                  690          DC     NOB             92  STBR                             0816689
193      00 0000                  691          DC     0               93  LBR                              0816690
194      00 00A1                  692          DC     NOB             94  EXBR                             0816691
195      00 0000                  693          DC     0               95  EPSR                             0816692
196      00 02ED                  694          DC     WBR             96  WBR                              0816693
197      00 02F0                  695          DC     RBR             97  RBR                              0816694
198      00 0025                  696          DC     WHR             98  WHR                              0816695
199      00 0021                  697          DC     RHR             99  RHR                              0816696
19A      00 0027                  698          DC     WDR             9A  WDR                              0816697
19B      00 0023                  699          DC     RDR             9B  RDR                              0816698
19C                               700          IFZ    MPY.DIV                                              0816699
19C      00 0000                  701          DC     0               9C                                   0816700
                                  702          ENDC                                                        0816701
                                  705          ENDC                                                        0816704
19D      00 002C                  706          DC     SSR             9D  SSR                              0816705
19E      00 002F                  707          DC     OCR             9E  OCR                              0816706
19F      00 002C                  708          DC     SSR             9F  AIR                              0816707
```

MODEL 8/16 DROM2 DATA

```
                                  710    *                                                    0816709
                                  711    * OP-CODES  A0 - AF  ARE ILLEGAL                    0816710
                                  712    *                                                    0816711
1A0     00 0000                   713           DC     0                                     0816712
1A1     00 0000                   714           DC     0                                     0816713
1A2     00 0000                   715           DC     0                                     0816714
1A3     00 0000                   716           DC     0                                     0816715
1A4     00 0000                   717           DC     0                                     0816716
1A5     00 0000                   718           DC     0                                     0816717
1A6     00 0000                   719           DC     0                                     0816718
1A7     00 0000                   720           DC     0                                     0816719
1A8     00 0000                   721           DC     0                                     0816720
1A9     00 0000                   722           DC     0                                     0816721
1AA     00 0000                   723           DC     0                                     0816722
1AB     00 0000                   724           DC     0                                     0816723
1AC     00 0000                   725           DC     0                                     0816724
1AD     00 0000                   726           DC     0                                     0816725
1AE     00 0000                   727           DC     0                                     0816726
1AF     00 0000                   728           DC     0                                     0816727
                                  729    *                                                    0816728
                                  730    * OP-CODES  B0 - BF  ARE ILLEGAL                    0816729
                                  731    *                                                    0816730
1B0     00 0000                   732           DC     0                                     0816731
1B1     00 0000                   733           DC     0                                     0816732
1B2     00 0000                   734           DC     0                                     0816733
1B3     00 0000                   735           DC     0                                     0816734
1B4     00 0000                   736           DC     0                                     0816735
1B5     00 0000                   737           DC     0                                     0816736
1B6     00 0000                   738           DC     0                                     0816737
1B7     00 0000                   739           DC     0                                     0816738
1B8     00 0000                   740           DC     0                                     0816739
1B9     00 0000                   741           DC     0                                     0816740
1BA     00 0000                   742           DC     0                                     0816741
1BB     00 0000                   743           DC     0                                     0816742
1BC     00 0000                   744           DC     0                                     0816743
1BD     00 0000                   745           DC     0                                     0816744
1BE     00 0000                   746           DC     0                                     0816745
1BF     00 0000                   747           DC     0                                     0816746
```

MODEL 8/16 DROM2 DATA

```
1C0   00 00AF   749        DC   BXH        C0  BXH    0816748
1C1   00 00B1   750        DC   BXLE       C1  BXLE   0816749
1C2   00 00CE   751        DC   LPSW       C2  LPSW   0816750
1C3   00 008A   752        DC   THI        C3  THI    0816751
1C4   00 0092   753        DC   NHR        C4  NHI    0816752
1C5   00 0099   754        DC   CLHR       C5  CLHI   0816753
1C6   00 0093   755        DC   OHR        C6  OHI    0816754
1C7   00 0094   756        DC   XHR        C7  XHI    0816755
1C8   00 0095   757        DC   LHR        C8  LHI    0816756
1C9   00 0097   758        DC   CHR        C9  CHI    0816757
1CA   00 008E   759        DC   AHR        CA  AHI    0816758
1CB   00 0090   760        DC   SHR        CB  SHI    0816759
1CC   00 0064   761        DC   SRHLD2     CC  SRHL   0816760
1CD   00 0051   762        DC   SLHLD2     CD  SLHL   0816761
1CE   00 0061   763        DC   SRHAD2     CE  SRHA   0816762
1CF   00 005D   764        DC   SLHAD2     CF  SLHA   0816763
                765  *                               0816764
                766  *                               0816765
1D0   00 00CA   767        DC   STM        D0  STM    0816766
1D1   00 00C6   768        DC   LM         D1  LM     0816767
1D2   00 00BD   769        DC   STB        D2  STB    0816768
1D3   00 00B5   770        DC   LB         D3  LB     0816769
1D4   00 00B9   771        DC   CLB        D4  CLB    0816770
1D5   00 02F0   772        DC   RBR        D5  AL     0816771
1D6   00 02ED   773        DC   WBR        D6  WB     0816772
1D7   00 02F0   774        DC   RBR        D7  RB     0816773
1D8   00 0025   775        DC   WHR        D8  WH     0816774
1D9   00 001B   776        DC   RH         D9  RH     0816775
1DA   00 00E4   777        DC   WD         DA  WD     0816776
1DB   00 0018   778        DC   RD         DB  RD     0816777
1DC             779        IFZ  MPY.DIV               0816778
1DC   00 0000   780        DC   0          DC         0816779
                781        ENDC                       0816780
                784        ENDC                       0816783
1DD   00 0029   785        DC   SS         DD  SS     0816784
1DE   00 002E   786        DC   OC         DE  OC     0816785
1DF   00 0029   787        DC   SS         DF  AI     0816786
```

MODEL 8/16 DROM2 DATA

```
1E0     00 0000         789              DC     0                E0                  D816788
1E1     00 00ED         790              DC     SVCD2            E1   SVC            D816789
1E2     00 0080         791              DC     SINT             E2   SINT           D816790
1E3     00 0000         792              DC     0                E3                  D816791
1E4     00 0000         793              DC     0                E4                  D816792
1E5     00 0000         794              DC     0                E5                  D816793
1E6     00 0000         795              DC     0                E6                  D816794
1E7     00 0000         796              DC     0                E7                  D816795
1E8     00 0000         797              DC     0                E8                  D816796
1E9     00 0000         798              DC     0                E9                  D816797
1EA     00 006B         799              DC     RRLD2            EA   RRL            D816798
1EB     00 005A         800              DC     RLLD2            EB   RLL            D816799
1EC     00 0068         801              DC     SRLD2            EC   SRL            D816800
1ED     00 0054         802              DC     SLLD2            ED   SLL            D816801
1EE     00 006E         803              DC     SRAD2            EE   SRA            D816802
1EF     00 0074         804              DC     SLAD2            EF   SLA            D816803
                        805     *                                                    D816804
                        806     * OP-CODES  F0 - FF  ARE ILLEGAL                     D816805
                        807     *                                                    D816806
1F0     00 0000         808              DC     0                                    D816807
1F1     00 0000         809              DC     0                                    D816808
1F2     00 0000         810              DC     0                                    D816809
1F3     00 0000         811              DC     0                                    D816810
1F4     00 0000         812              DC     0                                    D816811
1F5     00 0000         813              DC     0                                    D816812
1F6     00 0000         814              DC     0                                    D816813
1F7     00 0000         815              DC     0                                    D816814
1F8     00 0000         816              DC     0                                    D816815
1F9     00 0000         817              DC     0                                    D816816
1FA     00 0000         818              DC     0                                    D816817
1FB     00 0000         819              DC     0                                    D816818
1FC     00 0000         820              DC     0                                    D816819
1FD     00 0000         821              DC     0                                    D816820
1FE     00 0000         822              DC     0                                    D816821
1FF     00 0000         823              DC     0                                    D816822
                        824     *                                                    D816823
200                     825              END                                         D816824
```

MODEL 8/16 DROM2 DATA

NO ERRORS

ABLO2	0267
ACH	008D
ADD	0195
ADDWRT	0188
AHM	0088
AHR	008E
AI	0004
AIR	00D7
AL	000B
AL1	030E
ALO1	0300
ALO2	0306
ALOC	0026
ALX	0310
APSW	0024
ATL1	0253
ATL2	0262
ATLABL	007E
ATLABLD1	0251
ATLO2	025E
BALR	009F
BFCR	00A4
BFS	00A8
BKWORD	00AC
BLKIO1	02E5
BLKIO2	02E6
BLKIO3	02E9
BLKRR1	02E1
BRANCH	00A0
BTCR	00A2
BTS	00A6
BX	0012
BX1	00B2
BXH	00AF
BXLE	00B1
BXNOB	00B4
BXNX	0014
COD2	02B8
CER	00E1
CERD1	02BE
CHR	0097
CLB	00B9
CLHR	0099
CLRWT	0175
CONINT	01EB
CONSER	015F
CONTIN	017F
DHR	00DB
DHR1	0200
DIFFER	02DC
DISPLY	019D
DPFP	0000
EPSR	00D0

MODEL 8/16 DROM2 DATA

EPSR1	0330
EPSR2	033A
EPSR3	033C
EXBR	00C5
F.CC	02C8
F.VARI	0001
FDRXD2	02C0
FINISH	00FB
FL.OV	02D4
FLR	00DF
FLRD1	02CD
FLRD11	02CE
FLT1	01CB
FLT2	01D2
FLT3	01DF
FLT4	01E2
FLT5	01E4
FLTDISP	01C5
FN1	01AC
FN11	01B8
FN2.FN3	01B0
FNREG	0183
FROMAL	02F1
FRR	00E0
FRRD1	02C6
FRWORD	00AD
FRX	0079
FRXD1	02A5
FRXNX	02A7
FXR	00DE
FXR2	02C8
FXRD1	02C9
GENSWP	0321
HELP	0197
HELP1	0198
IDLE	0154
IDLE1	0136
IDLEX	015E
ILEG	009B
ILGPSW	0030
IMM	008C
IOAIN	01E7
IORR	00D8
IORX	0005
IOSVC	01EA
LB	00B5
LBR	00B6
LCS	0096
LDDOUBLE	0113
LDREG	010A
LDSINGLE	011F
LEADER	0317
LHR	0095
LIST.OV	028A

MODEL 8/16 DROM2 DATA

LM	00C6
LMD	008B
LMDD2	028B
LME	0091
LMED2	0291
LMEDONE	030C
LMNX	000E
LMSTM	000C
LOCDIS	012C
LOOK20	01BB
LPSW	00CE
LPSW1	032C
LSET	032B
MAR0	012E
MHR	00DC
MHR1	0232
MHUR	00DD
MHUR1	0248
MMALF	031E
MMALF1	0320
MME	0179
MPY.DIV	0000
MRONEG	0207
MROPOS	0205
NHR	0092
NLONG	0067
NNEG1	0238
NNEG2	023C
NOB	00A1
NOWRAP1	0261
NOWRAP4	0284
OC	002E
OCR	002F
OHR	0093
OIPSW	0040
OMMPSW	0038
OUTDIS	012F
OV	0225
OV1	022A
PNTR	0022
POW	0157
PSWLOC	01B6
PWRDWN	0138
PWRDWN2	014D
PWRUP	0100
PWRUP2	0119
PWRUP3	0125
QNEG	0222
QOK	021F
QOK1	024F
QUEINT	0322
QUENBL	0332
RB1	02F3
RBLD2	027F

MODEL 8/16 DROM2 DATA

RBR	02F0
RBRWBR	000A
RBRWBRD1	02DF
RBWB	0034
RBWBNX	0038
RD	0018
RD2	0019
RDKEY	018F
RDR	0023
REGDIS	01BF
REGN	01C0
RH	001B
RHH	001E
RHR	0021
RLLD2	005A
RNNEG	021B
RRLD2	006B
RS	0002
RSNX	000A
RTL1	026F
RTL2	0285
RTLD2	0278
RTLRBL	007F
RTLRBLD1	026D
RX	0006
RXNX	0008
SAVREG	0140
SCH	008F
SHIFTO	00E6
SHORTB	00A9
SHR	0090
SINT	00B0
SINT1	01ED
SINT2	01F6
SLA	004D
SLAD2	0074
SLHA	0047
SLHA1	0048
SLHAD2	005D
SLHL	003D
SLHL2	003E
SLHL3	003F
SLHLD2	0051
SLHLNX	0042
SLL	004F
SLL1D2	0056
SLLD2	0054
SLLS	0004
SPFP	0000
SRAD2	006E
SRHAD2	0061
SRHL1	0065
SRHLD2	0064
SRL1D2	0069

MODEL 8/16 DROM2 DATA

SRLD2	0068
SS	0029
SSR	002C
START	0000
START1	0001
STB	00BD
STBR	00C0
STD	00E3
STD02	02AF
STDOUBLE	0149
STE	00E2
STE.STD	007A
STE02	02B3
STENX	007C
STH	0084
STH2	0086
STM	00CA
STMD	009A
STMD02	029A
STME	009E
STMED2	029E
STSINGLE	0153
SVC02	00ED
TERMIN	00FC
THI	008A
THRUD2	0046
WAIT	0159
WAIT1	015C
WASEMPTY	028A
WBR	02ED
WD	00E4
WDR	0027
WHR	0025
XHR	0094
YDNNEG	020D

PROG= M816DF02   ASSEMBLED BY MICROCAL II (32-BIT)

```
0002                    F.VARI   EQU   2                  F02 : BASIC + M/D          D816001
                                                                                      D816002
                        *                                                             D816003
                                 NLSTC                                                D816004
                        *                                                             D816005
                                 SGCHK                                                D816006
                        *                                                             D816007
                        *                                                             D816008
                        * SET UP SYSGEN PARAMETERS                                    D816009
                        *                                                             D816010
000                              IFP   F.VARI-1                                       D816011
0001                    MPY.DIV  EQU   1                                              D816014
                                 ENDC                                                 D816017
                                 ELSE                                                 D816018
0000                    SPFP     EQU   0                                              D816019
                                 ENDC                                                 D816022
                                 ELSE                                                 D816023
0000                    DPFP     EQU   0                                              D816024
                                 ENDC                                                 D816025
                        *                                                             D816026
                        *                                                             D816027
                        *                                                             D816028
                        *                                                             D816029
                        * COPYRIGHT INTERDATA INC.   SEPTEMBER  1976                  D816030
                        *                                                             D816031
                        *                                                             D816032
                        * DHEMA MAHAJAN                                               D816033
                        *                                                             D816034
                        *                                                             D816035
                        * DROM SOURCE IS ASSEMBLED IN CONJUNCTION WITH THE MICROPROGRAM SOURCE D816036
                        * OPERAND FIELD IS THE SYMBOLIC ROM ENTRY POINT FOR D1        D816037
                        * COMMENT FIELD SHOWS OP-CODE AND VALID INSTRUCTION MNEMONIC  D816038
                        * ONLY THE LEAST SIGNIFICANT BYTE OF THE CODE GENERATED IS USED D816039
                                 PARTS 19-186R00F00       DUMMY PART #                D816040
                                 PARTS 19-186R00F00       DUMMY PART #                D816041
                        * THE DROM DATA IS CONTAINED IN THE FOLLOWING 512 X 8 (4K) ROM CHIP D816042
                        *                                                             D816045
                                 ENDC                                                 D816046
000                              IFZ   F.VARI-2                                       D816047
                                 PARTS 19-186R00F28                                   D816048
                                 ENDC                                                 D816051
                                 ENDC                                                 D816054
                                 ENDC                                                 D816055
                        *                                                             D816056
000    00 0098                   DC    ILEG               00                          D816057
001    00 009F                   DC    BALR               01  BALR                    D816058
002    00 00A2                   DC    BTCR               02  BTCR                    D816059
003    00 00A4                   DC    BFCR               03  BFCR                    D816060
004    00 0092                   DC    NHR                04  NHR                     D816061
005    00 0099                   DC    CLHR               05  CLHR                    D816062
006    00 0093                   DC    OHR                06  OHR                     D816063
007    00 0094                   DC    XHR                07  XHR                     D816064
008    00 0095                   DC    LHR                08  LHR                     D816065
009    00 0097                   DC    CHR                09  CHR                     D816066
00A    00 008E                   DC    AHR                0A  AHR
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00B     00 0090          68              DC    SHR              0B  SHR          D816067
                         72              ENDC                                    D816071
00C                      73              IFP   MPY,DIV                          D816072
00C     00 00DC          74              DC    MHR              0C  MHR          D816073
00D     00 00DB          75              DC    DHR              0D  DHR          D816074
                         76              ENDC                                    D816075
00E     00 008D          77              DC    ACH              0E  ACHR         D816076
00F     00 008F          78              DC    SCH              0F  SCHR         D816077
                         79    *                                                 D816078
                         80    * OP-CODES  10 - 1F  ARE ILLEGAL                  D816079
                         81    *                                                 D816080
010     00 009B          82              DC    ILEG                             D816081
011     00 009B          83              DC    ILEG                             D816082
012     00 009B          84              DC    ILEG                             D816083
013     00 009B          85              DC    ILEG                             D816084
014     00 009B          86              DC    ILEG                             D816085
015     00 009B          87              DC    ILEG                             D816086
016     00 009B          88              DC    ILEG                             D816087
017     00 009B          89              DC    ILEG                             D816088
018     00 009B          90              DC    ILEG                             D816089
019     00 009B          91              DC    ILEG                             D816090
01A     00 009B          92              DC    ILEG                             D816091
01B     00 009B          93              DC    ILEG                             D816092
01C     00 009B          94              DC    ILEG                             D816093
01D     00 009B          95              DC    ILEG                             D816094
01E     00 009B          96              DC    ILEG                             D816095
01F     00 009B          97              DC    ILEG                             D816096
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020   00 00A6    99          DC    BTS      20  BTBS    D816098
021   00 00A6   100          DC    BTS      21  BTFS    D816099
022   00 00A8   101          DC    BFS      22  BFBS    D816100
023   00 00A8   102          DC    BFS      23  BFFS    D816101
024   00 008C   103          DC    IMM      24  LIS     D816102
025   00 0096   104          DC    LCS      25  LCS     D816103
026   00 008C   105          DC    IMM      26  AIS     D816104
027   00 008C   106          DC    IMM      27  SIS     D816105
028             107          IFZ   SPFP                 D816106
028   00 009B   108          DC    ILEG     28          D816107
029   00 009B   109          DC    ILEG     29          D816108
02A   00 009B   110          DC    ILEG     2A          D816109
02B   00 009B   111          DC    ILEG     2B          D816110
02C   00 009B   112          DC    ILEG     2C          D816111
02D   00 009B   113          DC    ILEG     2D          D816112
02E   00 009B   114          DC    ILEG     2E          D816113
02F   00 009B   115          DC    ILEG     2F          D816114
              116          ENDC                       D816115
              126          ENDC                       D816125
030           127          IFZ   DPFP                 D816126
              128   *                                  D816127
              129   * OP-CODES  30 - 3F  ARE ILLEGAL    D816128
              130   *                                  D816129
030   00 009B    131          DC    ILEG               D816130
031   00 009B    132          DC    ILEG               D816131
032   00 009B    133          DC    ILEG               D816132
033   00 009B    134          DC    ILEG               D816133
034   00 009B    135          DC    ILEG               D816134
035   00 009B    136          DC    ILEG               D816135
036   00 009B    137          DC    ILEG               D816136
037   00 009B    138          DC    ILEG               D816137
038   00 009B    139          DC    ILEG               D816138
039   00 009B    140          DC    ILEG               D816139
03A   00 009B    141          DC    ILEG               D816140
03B   00 009B    142          DC    ILEG               D816141
03C   00 009B    143          DC    ILEG               D816142
03D   00 009B    144          DC    ILEG               D816143
03E   00 009B    145          DC    ILEG               D816144
03F   00 009B    146          DC    ILEG               D816145
              147          ENDC                       D816146
              165          ENDC                       D816164
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040  00 0002   167          DC    RS          40  STH   D816166
041  00 0002   168          DC    RS          41  BAL   D816167
042  00 0002   169          DC    RS          42  BTC   D816168
043  00 0002   170          DC    RS          43  BFC   D816169
044  00 0006   171          DC    RX          44  NH    D816170
045  00 0006   172          DC    RX          45  CLH   D816171
046  00 0006   173          DC    RX          46  OH    D816172
047  00 0006   174          DC    RX          47  XH    D816173
048  00 0006   175          DC    RX          48  LH    D816174
049  00 0006   176          DC    RX          49  CH    D816175
04A  00 0006   177          DC    RX          4A  AH    D816176
04B  00 0006   178          DC    RX          4B  SH    D816177
               182          ENDC                        D816181
04C            183          IFP   MPY.DIV               D816182
04C  00 0006   184          DC    RX          4C  MH    D816183
04D  00 0006   185          DC    RX          4D  DH    D816184
               186          ENDC                        D816185
04E  00 0006   187          DC    RX          4E  ACH   D816186
04F  00 0006   188          DC    RX          4F  SCH   D816187
               189     *                                D816188
               190     * OP-CODES  50 - 5F  ARE ILLEGAL D816189
               191     *                                D816190
050  00 009B   192          DC    ILEG                    D816191
051  00 009B   193          DC    ILEG                    D816192
052  00 009B   194          DC    ILEG                    D816193
053  00 009B   195          DC    ILEG                    D816194
054  00 009B   196          DC    ILEG                    D816195
055  00 009B   197          DC    ILEG                    D816196
056  00 009B   198          DC    ILEG                    D816197
057  00 009B   199          DC    ILEG                    D816198
058  00 009B   200          DC    ILEG                    D816199
059  00 009B   201          DC    ILEG                    D816200
05A  00 009B   202          DC    ILEG                    D816201
05B  00 009B   203          DC    ILEG                    D816202
05C  00 009B   204          DC    ILEG                    D816203
05D  00 009B   205          DC    ILEG                    D816204
05E  00 009B   206          DC    ILEG                    D816205
05F  00 009B   207          DC    ILEG                    D816206
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060                  209        IFZ   SPFP                     D816208
060   00 009B        210        DC    ILEG       60            D816209
                     211        ENDC                           D816210
                     214        ENDC                           D816213
061   00 0006        215        DC    RX         61  AHM       D816214
062   00 009B        216        DC    ILEG       62            D816215
063   00 009B        217        DC    ILEG       63            D816216
064   00 007E        218        DC    ATLABL     64  ATL       D816217
065   00 007E        219        DC    ATLABL     65  ABL       D816218
066   00 007F        220        DC    RTLRBL     66  RTL       D816219
067   00 007F        221        DC    RTLRBL     67  RBL       D816220
068                  222        IFZ   SPFP                     D816221
068   00 009B        223        DC    ILEG       68            D816222
069   00 009B        224        DC    ILEG       69            D816223
06A   00 009B        225        DC    ILEG       6A            D816224
06B   00 009B        226        DC    ILEG       6B            D816225
06C   00 009B        227        DC    ILEG       6C            D816226
06D   00 009B        228        DC    ILEG       6D            D816227
                     229        ENDC                           D816228
                     237        ENDC                           D816236
06E   00 009B        238        DC    ILEG       6E            D816237
06F   00 009B        239        DC    ILEG       6F            D816238
                     240   *                                   D816239
                     241   *                                   D816240
070                  242        IFZ   DPFP                     D816241
070   00 009B        243        DC    ILEG       70            D816242
                     244        ENDC                           D816243
                     247        ENDC                           D816246
071                  248        IFZ   SPFP                     D816247
071   00 009B        249        DC    ILEG       71            D816248
072   00 009B        250        DC    ILEG       72            D816249
                     251        ENDC                           D816250
                     255        ENDC                           D816254
073   00 009B        256        DC    ILEG       73            D816255
074   00 009B        257        DC    ILEG       74            D816256
075   00 009B        258        DC    ILEG       75            D816257
076   00 009B        259        DC    ILEG       76            D816258
077   00 009B        260        DC    ILEG       77            D816259
078                  261        IFZ   DPFP                     D816260
078   00 009B        262        DC    ILEG       78            D816261
079   00 009B        263        DC    ILEG       79            D816262
07A   00 009B        264        DC    ILEG       7A            D816263
07B   00 009B        265        DC    ILEG       7B            D816264
07C   00 009B        266        DC    ILEG       7C            D816265
07D   00 009B        267        DC    ILEG       7D            D816266
07E   00 009B        268        DC    ILEG       7E            D816267
07F   00 009B        269        DC    ILEG       7F            D816268
                     270        ENDC                           D816269
                     280        ENDC                           D816279
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                             282     *                                                        D816281
                             283     * OP-CODES  80 - 8F  ARE ILLEGAL                        D816282
                             284     *                                                        D816283
080     00 009B              285              DC     ILEG                                     D816284
081     00 009B              286              DC     ILEG                                     D816285
082     00 009B              287              DC     ILEG                                     D816286
083     00 009B              288              DC     ILEG                                     D816287
084     00 009B              289              DC     ILEG                                     D816288
085     00 009B              290              DC     ILEG                                     D816289
086     00 009B              291              DC     ILEG                                     D816290
087     00 009B              292              DC     ILEG                                     D816291
088     00 009B              293              DC     ILEG                                     D816292
089     00 009B              294              DC     ILEG                                     D816293
08A     00 009B              295              DC     ILEG                                     D816294
08B     00 009B              296              DC     ILEG                                     D816295
08C     00 009B              297              DC     ILEG                                     D816296
08D     00 009B              298              DC     ILEG                                     D816297
08E     00 009B              299              DC     ILEG                                     D816298
08F     00 009B              300              DC     ILEG                                     D816299
                             301     *                                                        D816300
                             302     *                                                        D816301
090     00 00D4              303              DC     SLLS            90   SRLS                D816302
091     00 00D4              304              DC     SLLS            91   SLLS                D816303
092     00 00C0              305              DC     STBR            92   STBR                D816304
093     00 00B6              306              DC     LBR             93   LBR                 D816305
094     00 00C5              307              DC     EXBR            94   EXBR                D816306
095     00 00D0              308              DC     EPSR            95   EPSR                D816307
096     00 00DA              309              DC     RBRWBR          96   WBR                 D816308
097     00 00DA              310              DC     RBRWBR          97   RBR                 D816309
098     00 00D8              311              DC     IORR            98   WHR                 D816310
099     00 00D8              312              DC     IORR            99   RHR                 D816311
09A     00 00D8              313              DC     IORR            9A   WDR                 D816312
09B     00 00D8              314              DC     IORR            9B   RDR                 D816313
                             317              ENDC                                            D816316
09C                          318              IFP    MPY.DIV                                  D816317
09C     00 00DD              319              DC     MHUR            9C   MHUR                D816318
                             320              ENDC                                            D816319
09D     00 00D8              321              DC     IORR            9D   SSR                 D816320
09E     00 00D8              322              DC     IORR            9E   OCR                 D816321
09F     00 00D7              323              DC     AIR             9F   AIR                 D816322
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                                  325     *
                                  326     * OP-CODES  A0 - AF  ARE ILLEGAL
                                  327     *
0A0     00 009B                   328             DC      ILEG
0A1     00 009B                   329             DC      ILEG
0A2     00 009B                   330             DC      ILEG
0A3     00 009B                   331             DC      ILEG
0A4     00 009B                   332             DC      ILEG
0A5     00 009B                   333             DC      ILEG
0A6     00 009B                   334             DC      ILEG
0A7     00 009B                   335             DC      ILEG
0A8     00 009B                   336             DC      ILEG
0A9     00 009B                   337             DC      ILEG
0AA     00 009B                   338             DC      ILEG
0AB     00 009B                   339             DC      ILEG
0AC     00 009B                   340             DC      ILEG
0AD     00 009B                   341             DC      ILEG
0AE     00 009B                   342             DC      ILEG
0AF     00 009B                   343             DC      ILEG
                                  344     *
                                  345     * OP-CODES  B0 - BF  ARE ILLEGAL
                                  346     *
0B0     00 009B                   347             DC      ILEG
0B1     00 009B                   348             DC      ILEG
0B2     00 009B                   349             DC      ILEG
0B3     00 009B                   350             DC      ILEG
0B4     00 009B                   351             DC      ILEG
0B5     00 009B                   352             DC      ILEG
0B6     00 009B                   353             DC      ILEG
0B7     00 009B                   354             DC      ILEG
0B8     00 009B                   355             DC      ILEG
0B9     00 009B                   356             DC      ILEG
0BA     00 009B                   357             DC      ILEG
0BB     00 009B                   358             DC      ILEG
0BC     00 009B                   359             DC      ILEG
0BD     00 009B                   360             DC      ILEG
0BE     00 009B                   361             DC      ILEG
0BF     00 009B                   362             DC      ILEG
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D816324
D816325
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D816361

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0C0     00 0012     364          DC    SX          C0  BXH     D816363
0C1     00 0012     365          DC    BX          C1  BXLE    D816364
0C2     00 0006     366          DC    RX          C2  LPSW    D816365
0C3     00 0002     367          DC    RS          C3  THI     D816366
0C4     00 0002     368          DC    RS          C4  NHI     D816367
0C5     00 0002     369          DC    RS          C5  CLHI    D816368
0C6     00 0002     370          DC    RS          C6  OHI     D816369
0C7     00 0002     371          DC    RS          C7  XHI     D816370
0C8     00 0002     372          DC    RS          C8  LHI     D816371
0C9     00 0002     373          DC    RS          C9  CHI     D816372
0CA     00 0002     374          DC    RS          CA  AHI     D816373
0CB     00 0002     375          DC    RS          CB  SHI     D816374
0CC     00 003D     376          DC    SLHL        CC  SRHL    D816375
0CD     00 003D     377          DC    SLHL        CD  SLHL    D816376
0CE     00 0047     378          DC    SLHA        CE  SRHA    D816377
0CF     00 0047     379          DC    SLHA        CF  SLHA    D816378
                    380  *                                     D816379
                    381  *                                     D816380
0D0     00 000C     382          DC    LMSTM       D0  STM     D816381
0D1     00 000C     383          DC    LMSTM       D1  LM      D816382
0D2     00 0006     384          DC    RX          D2  STB     D816383
0D3     00 0006     385          DC    RX          D3  LB      D816384
0D4     00 0006     386          DC    RX          D4  CLB     D816385
0D5     00 0008     387          DC    AL          D5  AL      D816386
0D6     00 0034     388          DC    RBWB        D6  WB      D816387
0D7     00 0034     389          DC    RBWB        D7  RB      D816388
0D8     00 0005     390          DC    IORX        D8  WH      D816389
0D9     00 0005     391          DC    IORX        D9  RH      D816390
0DA     00 0005     392          DC    IORX        DA  WD      D816391
0DB     00 0005     393          DC    IORX        DB  RD      D816392
                    396          ENDC                          D816395
0DC                 397          IFP   MPY.DIV                 D816396
0DC     00 0006     398          DC    RX          DC  MHU     D816397
                    399          ENDC                          D816398
0DD     00 0005     400          DC    IORX        DD  SS      D816399
0DE     00 0005     401          DC    IORX        DE  OC      D816400
0DF     00 0004     402          DC    AI          DF  AI      D816401
```

```
0E0   00 009B   404          DC   ILEG        E0                  D816403
0E1   00 0002   405          DC   RS          E1  SVC             D816404
0E2   00 0002   406          DC   RS          E2  SINT            D816405
0E3   00 009B   407          DC   ILEG        E3                  D816406
0E4   00 009B   408          DC   ILEG        E4                  D816407
0E5   00 009B   409          DC   ILEG        E5                  D816408
0E6   00 009B   410          DC   ILEG        E6                  D816409
0E7   00 009B   411          DC   ILEG        E7                  D816410
0E8   00 009B   412          DC   ILEG        E8                  D816411
0E9   00 009B   413          DC   ILEG        E9                  D816412
0EA   00 004F   414          DC   SLL         EA  RRL             D816413
0EB   00 004F   415          DC   SLL         EB  RLL             D816414
0EC   00 004F   416          DC   SLL         EC  SRL             D816415
0ED   00 004F   417          DC   SLL         ED  SLL             D816416
0EE   00 004D   418          DC   SLA         EE  SRA             D816417
0EF   00 004D   419          DC   SLA         EF  SLA             D816418
                420  *                                            D816419
                421  * OP-CODES  F0 - FF  ARE ILLEGAL             D816420
                422  *                                            D816421
                                                                  D816422
0F0   00 009B   423          DC   ILEG                           D816423
0F1   00 009B   424          DC   ILEG                           D816424
0F2   00 009B   425          DC   ILEG                           D816425
0F3   00 009B   426          DC   ILEG                           D816426
0F4   00 009B   427          DC   ILEG                           D816427
0F5   00 009B   428          DC   ILEG                           D816428
0F6   00 009B   429          DC   ILEG                           D816429
0F7   00 009B   430          DC   ILEG                           D816430
0F8   00 009B   431          DC   ILEG                           D816431
0F9   00 009B   432          DC   ILEG                           D816432
0FA   00 009B   433          DC   ILEG                           D816433
0FB   00 009B   434          DC   ILEG                           D816434
0FC   00 009B   435          DC   ILEG                           D816435
0FD   00 009B   436          DC   ILEG                           D816436
0FE   00 009B   437          DC   ILEG                           D816437
0FF   00 009B   438          DC   ILEG
```

MODEL 8/16 DROM2 DATA

```
                          440   *                                                    D816439
                          441   *                                                    D816440
100   00 0000             442         DC    0          00                          D816441
101   00 0000             443         DC    0          01  BALR                    D816442
102   00 0000             444         DC    0          02  BTCR                    D816443
103   00 0000             445         DC    0          03  BFCR                    D816444
104   00 0000             446         DC    0          04  NHR                     D816445
105   00 0000             447         DC    0          05  CLHR                    D816446
106   00 0000             448         DC    0          06  OHR                     D816447
107   00 0000             449         DC    0          07  XHR                     D816448
108   00 0000             450         DC    0          08  LHR                     D816449
109   00 0000             451         DC    0          09  CHR                     D816450
10A   00 0000             452         DC    0          0A  AHR                     D816451
10B   00 0000             453         DC    0          0B  SHR                     D816452
                          457         ENDC                                         D816456
10C                       458         IFP   MPY.DIV                              D816457
10C   00 0000             459         DC    0          0C  MHR                     D816458
10D   00 0000             460         DC    0          0D  DHR                     D816459
                          461         ENDC                                         D816460
10E   00 0000             462         DC    0          0E  ACHR                    D816461
10F   00 0000             463         DC    0          0F  SCHR                    D816462
                          464   *                                                    D816463
                          465   * OP-CODES  10 = 1F  ARE ILLEGAL                    D816464
                          466   *                                                    D816465
110   00 0000             467         DC    0                                      D816466
111   00 0000             468         DC    0                                      D816467
112   00 0000             469         DC    0                                      D816468
113   00 0000             470         DC    0                                      D816469
114   00 0000             471         DC    0                                      D816470
115   00 0000             472         DC    0                                      D816471
116   00 0000             473         DC    0                                      D816472
117   00 0000             474         DC    0                                      D816473
118   00 0000             475         DC    0                                      D816474
119   00 0000             476         DC    0                                      D816475
11A   00 0000             477         DC    0                                      D816476
11B   00 0000             478         DC    0                                      D816477
11C   00 0000             479         DC    0                                      D816478
11D   00 0000             480         DC    0                                      D816479
11E   00 0000             481         DC    0                                      D816480
11F   00 0000             482         DC    0                                      D816481
```

MODEL 8/16 DROM2 DATA

```
120  00 00AC   484          DC   BKWORD   20  BTBS   D816483
121  00 00AD   485          DC   FRWORD   21  BTFS   D816484
122  00 00AC   486          DC   BKWORD   22  BFBS   D816485
123  00 00AD   487          DC   FRWORD   23  BFFS   D816486
124  00 0095   488          DC   LHR      24  LIS    D816487
125  00 0000   489          DC   0        25  LCS    D816488
126  00 008E   490          DC   AHR      26  AIS    D816489
127  00 0090   491          DC   SHR      27  SIS    D816490
128            492          IFZ  SPFP                D816491
128  00 0000   493          DC   0        28         D816492
129  00 0000   494          DC   0        29         D816493
12A  00 0000   495          DC   0        2A         D816494
12B  00 0000   496          DC   0        2B         D816495
12C  00 0000   497          DC   0        2C         D816496
12D  00 0000   498          DC   0        2D         D816497
12E  00 0000   499          DC   0        2E         D816498
12F  00 0000   500          DC   0        2F         D816499
               501          ENDC                     D816500
               511          ENDC                     D816510
130            512          IFZ  DPFP                D816511
               513     *                             D816512
               514     * OP-CODES  30 - 3F  ARE ILLEGAL D816513
               515     *                             D816514
130  00 0000   516          DC   0                   D816515
131  00 0000   517          DC   0                   D816516
132  00 0000   518          DC   0                   D816517
133  00 0000   519          DC   0                   D816518
134  00 0000   520          DC   0                   D816519
135  00 0000   521          DC   0                   D816520
136  00 0000   522          DC   0                   D816521
137  00 0000   523          DC   0                   D816522
138  00 0000   524          DC   0                   D816523
139  00 0000   525          DC   0                   D816524
13A  00 0000   526          DC   0                   D816525
13B  00 0000   527          DC   0                   D816526
13C  00 0000   528          DC   0                   D816527
13D  00 0000   529          DC   0                   D816528
13E  00 0000   530          DC   0                   D816529
13F  00 0000   531          DC   0                   D816530
               532          ENDC                     D816531
               550          ENDC                     D816549
```

MODEL 8/16 DROM2 DATA

```
140  00 0084   552          DC    STH          40  STH   D816551
141  00 009F   553          DC    BALR         41  BALR  D816552
142  00 00A2   554          DC    BTCR         42  BTCR  D816553
143  00 00A4   555          DC    BFCR         43  BFCR  D816554
144  00 0092   556          DC    NHR          44  NH    D816555
145  00 0099   557          DC    CLHR         45  CLH   D816556
146  00 0093   558          DC    OHR          46  OH    D816557
147  00 0094   559          DC    XHR          47  XH    D816558
148  00 0095   560          DC    LHR          48  LH    D816559
149  00 0097   561          DC    CHR          49  CH    D816560
14A  00 008E   562          DC    AHR          4A  AH    D816561
14B  00 0090   563          DC    SHR          4B  SH    D816562
               567          ENDC                        D816566
14C            568          IFP   MPY,DIV               D816567
14C  00 00DC   569          DC    MHR          4C  MH    D816568
14D  00 00DB   570          DC    DHR          4D  DH    D816569
               571          ENDC                        D816570
14E  00 008D   572          DC    ACH          4E  ACH   D816571
14F  00 008F   573          DC    SCH          4F  SCH   D816572
               574  *                                    D816573
               575  * OP-CODES  50 - 5F  ARE ILLEGAL     D816574
               576  *                                    D816575
150  00 0000   577          DC    0                      D816576
151  00 0000   578          DC    0                      D816577
152  00 0000   579          DC    0                      D816578
153  00 0000   580          DC    0                      D816579
154  00 0000   581          DC    0                      D816580
155  00 0000   582          DC    0                      D816581
156  00 0000   583          DC    0                      D816582
157  00 0000   584          DC    0                      D816583
158  00 0000   585          DC    0                      D816584
159  00 0000   586          DC    0                      D816585
15A  00 0000   587          DC    0                      D816586
15B  00 0000   588          DC    0                      D816587
15C  00 0000   589          DC    0                      D816588
15D  00 0000   590          DC    0                      D816589
15E  00 0000   591          DC    0                      D816590
15F  00 0000   592          DC    0                      D816691
```

MODEL 8/16 DROM2 DATA

```
160                594     IFZ    SPFP                          D816593
160   00 0000      595     DC     0              60             D816594
                   596     ENDC                                 D816595
                   599     ENDC                                 D816598
161   00 0086      600     DC     AHM            61  AHM        D816599
162   00 0000      601     DC     0              62             D816600
163   00 0000      602     DC     0              63             D816601
164   00 025E      603     DC     ATLD2          64  ATL        D816602
165   00 0267      604     DC     ABLD2          65  ABL        D816603
166   00 0278      605     DC     RTLD2          66  RTL        D816604
167   00 027F      606     DC     RBLD2          67  RBL        D816605
168                607     IFZ    SPFP                          D816606
168   00 0000      608     DC     0              68             D816607
169   00 0000      609     DC     0              69             D816608
16A   00 0000      610     DC     0              6A             D816609
16B   00 0000      611     DC     0              6B             D816610
16C   00 0000      612     DC     0              6C             D816611
16D   00 0000      613     DC     0              6D             D816612
                   614     ENDC                                 D816613
                   622     ENDC                                 D816621
16E   00 0000      623     DC     0              6E             D816622
16F   00 0000      624     DC     0              6F             D816623
                   625  *                                       D816624
                   626  *                                       D816625
170                627     IFZ    DPFP                          D816626
170   00 0000      628     DC     0                             D816627
                   629     ENDC                                 D816628
                   632     ENDC                                 D816631
171                633     IFZ    SPFP                          D816632
171   00 0000      634     DC     0                             D816633
172   00 0000      635     DC     0                             D816634
                   636     ENDC                                 D816635
                   640     ENDC                                 D816639
173   00 0000      641     DC     0                             D816640
174   00 0000      642     DC     0                             D816641
175   00 0000      643     DC     0                             D816642
176   00 0000      644     DC     0                             D816643
177   00 0000      645     DC     0                             D816644
178                646     IFZ    DPFP                          D816645
178   00 0000      647     DC     0                             D816646
179   00 0000      648     DC     0                             D816647
17A   00 0000      649     DC     0                             D816648
17B   00 0000      650     DC     0                             D816649
17C   00 0000      651     DC     0                             D816650
17D   00 0000      652     DC     0                             D816651
17E   00 0000      653     DC     0                             D816652
17F   00 0000      654     DC     0                             D816653
                   655     ENDC                                 D816654
                   665     ENDC                                 D816664
```

MODEL 8/16 DROM2 DATA

```
                                667     *                                                                   D816666
                                668     * OP-CODES  80 - 8F  ARE ILLEGAL                                   D816667
                                669     *                                                                   D816668
180     00 0000                 670             DC      0                                                   D816669
181     00 0000                 671             DC      0                                                   D816670
182     00 0000                 672             DC      0                                                   D816671
183     00 0000                 673             DC      0                                                   D816672
184     00 0000                 674             DC      0                                                   D816673
185     00 0000                 675             DC      0                                                   D816674
186     00 0000                 676             DC      0                                                   D816675
187     00 0000                 677             DC      0                                                   D816676
188     00 0000                 678             DC      0                                                   D816677
189     00 0000                 679             DC      0                                                   D816678
18A     00 0000                 680             DC      0                                                   D816679
18B     00 0000                 681             DC      0                                                   D816680
18C     00 0000                 682             DC      0                                                   D816681
18D     00 0000                 683             DC      0                                                   D816682
18E     00 0000                 684             DC      0                                                   D816683
18F     00 0000                 685             DC      0                                                   D816684
                                686     *                                                                   D816685
                                687     *                                                                   D816686
190     00 0064                 688             DC      SRHLD2          90  SRLS                            D816687
191     00 0051                 689             DC      SLHLD2          91  SLLS                            D816688
192     00 00A1                 690             DC      NOB             92  STBR                            D816689
193     00 0000                 691             DC      0               93  LBR                             D816690
194     00 00A1                 692             DC      NOB             94  EXBR                            D816691
195     00 0000                 693             DC      0               95  EPSR                            D816692
196     00 02ED                 694             DC      WBR             96  WBR                             D816693
197     00 02F0                 695             DC      RBR             97  RBR                             D816694
198     00 0025                 696             DC      WHR             98  WHR                             D816695
199     00 0021                 697             DC      RHR             99  RHR                             D816696
19A     00 0027                 698             DC      WDR             9A  WDR                             D816697
19B     00 0023                 699             DC      RDR             9B  RDR                             D816698
                                702             ENDC                                                        D816701
19C                             703             IFP     MPY,DIV                                             D816702
19C     00 0000                 704             DC      0               9C  MHUR                            D816703
                                705             ENDC                                                        D816704
19D     00 002C                 706             DC      SSR             9D  SSR                             D816705
19E     00 002F                 707             DC      OCR             9E  OCR                             D816706
19F     00 002C                 708             DC      SSR             9F  AIR                             D816707
```

MODEL 8/16 DROM2 DATA

```
                      710    *                                            D816709
                      711    * OP-CODES  A0 - AF  ARE ILLEGAL             D816710
                      712    *                                            D816711
1A0      00 0000      713             DC     0                            D816712
1A1      00 0000      714             DC     0                            D816713
1A2      00 0000      715             DC     0                            D816714
1A3      00 0000      716             DC     0                            D816715
1A4      00 0000      717             DC     0                            D816716
1A5      00 0000      718             DC     0                            D816717
1A6      00 0000      719             DC     0                            D816718
1A7      00 0000      720             DC     0                            D816719
1A8      00 0000      721             DC     0                            D816720
1A9      00 0000      722             DC     0                            D816721
1AA      00 0000      723             DC     0                            D816722
1AB      00 0000      724             DC     0                            D816723
1AC      00 0000      725             DC     0                            D816724
1AD      00 0000      726             DC     0                            D816725
1AE      00 0000      727             DC     0                            D816726
1AF      00 0000      728             DC     0                            D816727
                      729    *                                            D816728
                      730    * OP-CODES  B0 - BF  ARE ILLEGAL             D816729
                      731    *                                            D816730
1B0      00 0000      732             DC     0                            D816731
1B1      00 0000      733             DC     0                            D816732
1B2      00 0000      734             DC     0                            D816733
1B3      00 0000      735             DC     0                            D816734
1B4      00 0000      736             DC     0                            D816735
1B5      00 0000      737             DC     0                            D816736
1B6      00 0000      738             DC     0                            D816737
1B7      00 0000      739             DC     0                            D816738
1B8      00 0000      740             DC     0                            D816739
1B9      00 0000      741             DC     0                            D816740
1BA      00 0000      742             DC     0                            D816741
1BB      00 0000      743             DC     0                            D816742
1BC      00 0000      744             DC     0                            D816743
1BD      00 0000      745             DC     0                            D816744
1BE      00 0000      746             DC     0                            D816745
1BF      00 0000      747             DC     0                            D816746
```

MODEL 8/16 DROM2 DATA

```
1C0   00 00AF   749          DC   BXH      C0  BXH      D816748
1C1   00 00B1   750          DC   BXLE     C1  BXLE     D816749
1C2   00 00CE   751          DC   LPSW     C2  LPSW     D816750
1C3   00 008A   752          DC   THI      C3  THI      D816751
1C4   00 0092   753          DC   NHR      C4  NHI      D816752
1C5   00 0099   754          DC   CLHR     C5  CLHI     D816753
1C6   00 0093   755          DC   OHR      C6  OHI      D816754
1C7   00 0094   756          DC   XHR      C7  XHI      D816755
1C8   00 0095   757          DC   LHR      C8  LHI      D816756
1C9   00 0097   758          DC   CHR      C9  CHI      D816757
1CA   00 008E   759          DC   AHR      CA  AHI      D816758
1CB   00 0090   760          DC   SHR      CB  SHI      D816759
1CC   00 0064   761          DC   SRHLD2   CC  SRHL     D816760
1CD   00 0051   762          DC   SLHLD2   CD  SLHL     D816761
1CE   00 0061   763          DC   SRHAD2   CE  SRHA     D816762
1CF   00 005D   764          DC   SLHAD2   CF  SLHA     D816763
                765  *                                  D816764
                766  *                                  D816765
1D0   00 00CA   767          DC   STM      D0  STM      D816766
1D1   00 00C6   768          DC   LM       D1  LM       D816767
1D2   00 00BD   769          DC   STB      D2  STB      D816768
1D3   00 0085   770          DC   LB       D3  LB       D816769
1D4   00 0089   771          DC   CLB      D4  CLB      D816770
1D5   00 02F0   772          DC   RBR      D5  AL       D816771
1D6   00 02ED   773          DC   WBR      D6  WB       D816772
1D7   00 02F0   774          DC   RBR      D7  RB       D816773
1D8   00 0025   775          DC   WHR      D8  WH       D816774
1D9   00 001B   776          DC   RH       D9  RH       D816775
1DA   00 00E4   777          DC   WD       DA  WD       D816776
1DB   00 0018   778          DC   RD       DB  RD       D816777
                781          ENDC                      D816780
1DC             782          IFP  MPY,DIV              D816781
1DC   00 00DD   783          DC   MHUR     DC  MHU      D816782
                784          ENDC                      D816783
1DD   00 0029   785          DC   SS       DD  SS       D816784
1DE   00 002E   786          DC   OC       DE  OC       D816785
1DF   00 0029   787          DC   SS       DF  AI       D816786
```

MODEL 8/16 DROM2 DATA

```
1E0  00 0000   789          DC   0          E0                 D816788
1E1  00 00ED   790          DC   SVCD2      E1  SVC            D816789
1E2  00 0080   791          DC   SINT       E2  SINT           D816790
1E3  00 0000   792          DC   0          E3                 D816791
1E4  00 0000   793          DC   0          E4                 D816792
1E5  00 0000   794          DC   0          E5                 D816793
1E6  00 0000   795          DC   0          E6                 D816794
1E7  00 0000   796          DC   0          E7                 D816795
1E8  00 0000   797          DC   0          E8                 D816796
1E9  00 0000   798          DC   0          E9                 D816797
1EA  00 006B   799          DC   RRLD2      EA  RRL            D816798
1EB  00 005A   800          DC   RLLD2      EB  RLL            D816799
1EC  00 0068   801          DC   SRLD2      EC  SRL            D816800
1ED  00 0054   802          DC   SLLD2      ED  SLL            D816801
1EE  00 006E   803          DC   SRAD2      EE  SRA            D816802
1EF  00 0074   804          DC   SLAD2      EF  SLA            D816803
               805  *                                          D816804
               806  * OP-CODES  F0 - FF  ARE ILLEGAL           D816805
               807  *                                          D816806
1F0  00 0000   808          DC   0                             D816807
1F1  00 0000   809          DC   0                             D816808
1F2  00 0000   810          DC   0                             D816809
1F3  00 0000   811          DC   0                             D816810
1F4  00 0000   812          DC   0                             D816811
1F5  00 0000   813          DC   0                             D816812
1F6  00 0000   814          DC   0                             D816813
1F7  00 0000   815          DC   0                             D816814
1F8  00 0000   816          DC   0                             D816815
1F9  00 0000   817          DC   0                             D816816
1FA  00 0000   818          DC   0                             D816817
1FB  00 0000   819          DC   0                             D816818
1FC  00 0000   820          DC   0                             D816819
1FD  00 0000   821          DC   0                             D816820
1FE  00 0000   822          DC   0                             D816821
1FF  00 0000   823          DC   0                             D816822
               824  *                                          D816823
200            825          END                                D816824
```

MODEL 8/16 DROM2 DATA

NO ERRORS

ABLD2	0267
ACH	008D
ADD	0195
ADDWRT	018B
AHM	0088
AHR	008E
AI	0004
AIR	00D7
AL	000B
AL1	030E
ALO1	0300
ALO2	0306
ALOC	0026
ALX	0310
APSW	0024
ATL1	0253
ATL2	0262
ATLABL!	007E
ATLABLD1	0251
ATLD?	025E
BALR	009F
BECR	00A4
BFS	00A8
BKWORD	00AC
BLKIO1	02E5
BLKIO2	02E6
BLKIO3	02E9
BLKRR1	02E1
BRANCH	00A0
BTCR	00A2
BTS	00A6
BX	0012
BX1	00B2
BXH	00AF
BXLE	00B1
BXNOB	00B4
BXNX	0014
CDD2	02B8
CER	00E1
CERD1	02BE
CHR	0097
CLB	00B9
CLHR	0099
CLRWT	0175
CONINT	01EB
CONSER	015F
CONTIN	017F
DHR	00DB
DHR1	0200
DIFFER	02DC
DISPLY	019D
DPFP	0000
EPSR	00D0

MODEL 8/16 DROM2 DATA

EPSR1	0330
EPSR2	033A
EPSR3	033C
EXBR	00C5
F.CC	02C8
F.VARI	0002
FDRXD2	02C0
FINISH	00FB
FL.OV	02D4
FLR	00DF
FLRD1	02CD
FLRD11	02CE
FLT1	01CB
FLT2	01D2
FLT3	01DF
FLT4	01E2
FLT5	01E4
FLTDISP	01C5
FN1	01AC
FN11	01B8
FN2.FN3	01B0
FNREG	0183
FROMAL	02F1
FRR	00E0
FRRD1	02C6
FRWORD	00AD
FRX	0079
FRXD1	02A5
FRXNX	02A7
FXR	00DE
FXR2	02C8
FXRD1	02C9
GENSWP	0321
HELP	0197
HELP1	0198
IDLE	0134
IDLE1	0136
IDLEX	015E
ILEG	009B
ILGPSW	0030
IMM	008C
IOATN	01E7
IORR	00D8
IORX	0005
IOSVC	01EA
LB	00B5
LBR	00B6
LCS	0096
LDDOUBLE	0113
LDREG	010A
LDSINGLE	011F
LEADER	0317
LHR	0095
LIST.OV	028A

MODEL 8/16 DROM2 DATA

LM	00C6
LMD	008B
LMDD2	028B
LME	0091
LMED2	0291
LMEDONE	030C
LMNX	000E
LMSTM	000C
LOCOIS	012C
LOOK20	018B
LPSW	00CE
LPSW1	032C
LSET	032B
MAR0	012E
MHR	00DC
MHR1	0232
MHUR	00DD
MHUR1	0248
MMALF	031E
MMALF1	0320
MME	0179
MPY.DIV	0001
MRONEG	0207
MROPOS	0205
NHR	0092
NLONG	0067
NNEG1	0238
NNEG2	023C
NOB	00A1
NOWRAP1	0261
NOWRAP4	0284
OC	002E
OCR	002F
OHR	0093
OIPSW	0040
OMMPSW	0038
OUTDIS	012F
OV	0225
OV1	022A
PNTR	0022
POW	0157
PSWLOC	01B6
PWRDWN	0138
PWRDWN2	014D
PWRUP	0100
PWRUP2	0119
PWRUP3	0125
QNEG	0222
QOK	021F
QOK1	024F
QUEINT	0322
QUENBLI	0332
RB1	02F3
RBLD2	027F

MODEL 8/16 DROM2 DATA

RBR	02F0
RBRWBR	00DA
RBRWBRD1	02DF
RBWB	0034
RBWBNX	0038
RD	0018
RD2	0019
RDKEY	018F
RDR	0023
REGDIS	01BF
REGN	01C0
RH	001B
RHH	001E
RHR	0021
RLLD2	005A
RNNEG	021B
RRLD2	006B
RS	0002
RSNX	000A
RTL1	026F
RTL2	0285
RTLD2	0278
RTLRBL	007F
RTLRBLD1	026D
RX	0006
RXNX	0008
SAVREG	0140
SCH	008F
SHIFTO	00E6
SHORTB	00A9
SHR	0090
SINT	0080
SINT1	01ED
SINT2	01F6
SLA	004D
SLAD2	0074
SLHA	0047
SLHA1	0048
SLHAD2	005D
SLHL	003D
SLHL2	003E
SLHL3	003F
SLHLD2	0051
SLHLNX	0042
SLL	004F
SLL1D2	0056
SLLD2	0054
SLLS	00D4
SPFP	0000
SRAD2	006E
SRHAD2	0061
SRHL1	0065
SRHLD2	0064
SRL1D2	0069

MODEL 8/16 DROM2 DATA

SRLD2	0068
SS	0029
SSR	002C
START	0000
START1	0001
STB	00BD
STBR	00C0
STD	00E3
STDD2	02AF
STDOUBLE	0149
STE	00E2
STE.STD	007A
STED2	0283
STENX	007C
STH	0084
STH2	0086
STM	00CA
STMD	009A
STMOD2	029A
STME	009E
STMED2	029E
STSINGLE	0153
SVCD2	00ED
TERMIN	00FC
THI	008A
THRUD2	0046
WAIT	0159
WAIT1	015C
WASEMPTY	028A
WBR	02ED
WD	00E4
WDR	0027
WHR	0025
XHR	0094
YDNNEG	020D

PROG= M816DF03 ASSEMBLED BY MICROCAL II (32-BIT)

```
0003                    2   F.VARI   EQU   3                    F03 : BASIC + M/D + SPFP
                        3   *
                        4            NLSTC
                        5   *
                        6            SQCHK
                        7   *
                        8   *
                        9   * SET UP SYSGEN PARAMETERS
                       10   *
                       11            IFP   F.VARI-1
0000
 0001                  12   MPY.DIV  EQU   1
                       15            ENDC
                       16            IFP   F.VARI-2
0000
 0001                  17   SPFP     EQU   1
                       20            ENDC
                       23            ELSE
0000                   24   DPFP     EQU   0
                       25            ENDC
                       26   *
                       27   *
                       28   *
                       29   *
                       30   * COPYRIGHT INTERDATA INC.   SEPTEMBER  1976
                       31   *
                       32   *
                       33   * DHEMA MAHAJAN
                       34   *
                       35   *
                       36   * DROM SOURCE IS ASSEMBLED IN CONJUNCTION WITH THE MICROPROGRAM SOURCE
                       37   * OPERAND FIELD IS THE SYMBOLIC ROM ENTRY POINT FOR D1
                       38   * COMMENT FIELD SHOWS OP-CODE AND VALID INSTRUCTION MNEMONIC
                       39   * ONLY THE LEAST SIGNIFICANT BYTE OF THE CODE GENERATED IS USED
                       40            PARTS 19-186R00F00        DUMMY PART #
                       41            PARTS 19-186R00F00        DUMMY PART #
                       42   * THE DROM DATA IS CONTAINED IN THE FOLLOWING 512 X 8 (4K) ROM CHIP
                       43   *
                       46            ENDC
                       49            ENDC
000                    50            IFZ   F.VARI-3
                       51            PARTS 19-186R00F29
                       52            ENDC
                       55            ENDC
                       56   *
000    00 009B         57            DC    ILEG          00
001    00 009F         58            DC    BALR          01  BALR
002    00 00A2         59            DC    BTCR          02  BTCR
003    00 00A4         60            DC    BFCR          03  BFCR
004    00 0092         61            DC    NHR           04  NHR
005    00 0099         62            DC    CLHR          05  CLHR
006    00 0093         63            DC    OHR           06  OHR
007    00 0094         64            DC    XHR           07  XHR
008    00 0095         65            DC    LHR           08  LHR
009    00 0097         66            DC    CHR           09  CHR
00A    00 008E         67            DC    AHR           0A  AHR
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D816001 D816002 D816003 D816004 D816005 D816006 D816007 D816008 D816009 D816010 D816011 D816014 D816015 D816016 D816019 D816022 D816023 D816024 D816025 D816026 D816027 D816028 D816029 D816030 D816031 D816032 D816033 D816034 D816035 D816036 D816037 D816038 D816039 D816040 D816041 D816042 D816045 D816048 D816049 D816050 D816051 D816054 D816055 D816056 D816057 D816058 D816059 D816060 D816061 D816062 D816063 D816064 D816065 D816066

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00B     00 0090          68          DC    SHR                 0B  SHR          D816067
                         72          ENDC                                       D816071
00C                      73          IFP   MPY.DIV                             D816072
00C     00 00DC          74          DC    MHR                 0C  MHR          D816073
00D     00 00DB          75          DC    DHR                 0D  DHR          D816074
                         76          ENDC                                       D816075
00E     00 008D          77          DC    ACH                 0E  ACHR         D816076
00F     00 008F          78          DC    SCH                 0F  SCHR         D816077
                         79    *                                                D816078
                         80    * OP-CODES  10 - 1F  ARE ILLEGAL                 D816079
                         81    *                                                D816080
010     00 009B          82          DC    ILEG                                 D816081
011     00 009B          83          DC    ILEG                                 D816082
012     00 009B          84          DC    ILEG                                 D816083
013     00 009B          85          DC    ILEG                                 D816084
014     00 009B          86          DC    ILEG                                 D816085
015     00 009B          87          DC    ILEG                                 D816086
016     00 009B          88          DC    ILEG                                 D816087
017     00 009B          89          DC    ILEG                                 D816088
018     00 009B          90          DC    ILEG                                 D816089
019     00 009B          91          DC    ILEG                                 D816090
01A     00 009B          92          DC    ILEG                                 D816091
01B     00 009B          93          DC    ILEG                                 D816092
01C     00 009B          94          DC    ILEG                                 D816093
01D     00 009B          95          DC    ILEG                                 D816094
01E     00 009B          96          DC    ILEG                                 D816095
01F     00 009B          97          DC    ILEG                                 D816096
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020  00 00A6   99          DC    BTS     20  BTBS   D816098
021  00 00A6  100          DC    BTS     21  BTFS   D816099
022  00 00A8  101          DC    BFS     22  BFBS   D816100
023  00 00A8  102          DC    BFS     23  BFFS   D816101
024  00 008C  103          DC    IMM     24  LIS    D816102
025  00 0096  104          DC    LCS     25  LCS    D816103
026  00 008C  105          DC    IMM     26  AIS    D816104
027  00 008C  106          DC    IMM     27  SIS    D816105
             116          ENDC                       D816115
             117          IFP   SPFP                 D816116
028                                                   D816117
028  00 00E0  118          DC    FRR     28  LER    D816118
029  00 00E1  119          DC    CER     29  CER    D816119
02A  00 00E0  120          DC    FRR     2A  AER    D816120
02B  00 00E0  121          DC    FRR     2B  SER    D816121
02C  00 00E0  122          DC    FRR     2C  MER    D816122
02D  00 00E0  123          DC    FRR     2D  DER    D816123
02E  00 00DE  124          DC    FXR     2E  FXR    D816124
02F  00 00DF  125          DC    FLR     2F  FLR    D816125
             126          ENDC                       D816126
030          127          IFZ   DPFP                 D816127
             128  *                                   D816126
             129  * OP-CODES  30 - 3F  ARE ILLEGAL    D816129
             130  *                                   D816130
030  00 009B  131          DC    ILEG                 D816131
031  00 009B  132          DC    ILEG                 D816132
032  00 009B  133          DC    ILEG                 D816133
033  00 009B  134          DC    ILEG                 D816134
034  00 009B  135          DC    ILEG                 D816135
035  00 009B  136          DC    ILEG                 D816136
036  00 009B  137          DC    ILEG                 D816137
037  00 009B  138          DC    ILEG                 D816138
038  00 009B  139          DC    ILEG                 D816139
039  00 009B  140          DC    ILEG                 D816140
03A  00 009B  141          DC    ILEG                 D816141
03B  00 009B  142          DC    ILEG                 D816142
03C  00 009B  143          DC    ILEG                 D816143
03D  00 009B  144          DC    ILEG                 D816144
03E  00 009B  145          DC    ILEG                 D816145
03F  00 009B  146          DC    ILEG                 D816146
             147          ENDC                       D816164
             165          ENDC
```

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040   00 0002   167          DC    RS          40  STH    D816166
041   00 0002   168          DC    RS          41  BAL    D816167
042   00 0002   169          DC    RS          42  BTC    D816168
043   00 0002   170          DC    RS          43  BFC    D816169
044   00 0006   171          DC    RX          44  NH     D816170
045   00 0006   172          DC    RX          45  CLH    D816171
046   00 0006   173          DC    RX          46  OH     D816172
047   00 0006   174          DC    RX          47  XH     D816173
048   00 0006   175          DC    RX          48  LH     D816174
049   00 0006   176          DC    RX          49  CH     D816175
04A   00 0006   177          DC    RX          4A  AH     D816176
04B   00 0006   178          DC    RX          4B  SH     D816177
                182          ENDC                         D816181
04C               183          IFP   MPY.DIV               D816182
04C   00 0006   184          DC    RX          4C  MH     D816183
04D   00 0006   185          DC    RX          4D  OH     D816184
                186          ENDC                         D816185
04E   00 0006   187          DC    RX          4E  ACH    D816186
04F   00 0006   188          DC    RX          4F  SCH    D816187
                189     *                                 D816188
                190     * OP-CODES  50 - 5F  ARE ILLEGAL   D816189
                191     *                                 D816190
050   00 009B   192          DC    ILEG                     D816191
051   00 009B   193          DC    ILEG                     D816192
052   00 009B   194          DC    ILEG                     D816193
053   00 009B   195          DC    ILEG                     D816194
054   00 009B   196          DC    ILEG                     D816195
055   00 009B   197          DC    ILEG                     D816196
056   00 009B   198          DC    ILEG                     D816197
057   00 009B   199          DC    ILEG                     D816198
058   00 009B   200          DC    ILEG                     D816199
059   00 009B   201          DC    ILEG                     D816200
05A   00 009B   202          DC    ILEG                     D816201
05B   00 009B   203          DC    ILEG                     D816202
05C   00 009B   204          DC    ILEG                     D816203
05D   00 009B   205          DC    ILEG                     D816204
05E   00 009B   206          DC    ILEG                     D816205
05F   00 009B   207          DC    ILEG                     D816206
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                        211          ENDC                                                    D816210
                        212          IFP    SPFP                                             D816211
060                     213          DC     STE,STD          60  STE                         D816212
060     00 007A         214          ENDC                                                    D816213
                        215          DC     RX               61  AHM                         D816214
061     00 0006         216          DC     ILEG             62                              D816215
062     00 009B         217          DC     ILEG             63                              D816216
063     00 009B         218          DC     ATLABL           64  ATL                         D816217
064     00 007E         219          DC     ATLABL           65  ABL                         D816218
065     00 007E         220          DC     RTLRBL           66  RTL                         D816219
066     00 007F         221          DC     RTLRBL           67  RBL                         D816220
067     00 007F         225          ENDC                                                    D816228
                        230          IFP    SFFP                                             D816229
068                     231          DC     FRX              68  LE                          D816230
06A     00 0079         232          DC     FRX              69  CE                          D816231
069     00 0079         233          DC     FRX              6A  AE                          D816232
06A     00 0079         234          DC     FRX              6B  SE                          D816233
06B     00 0079         235          DC     FRX              6C  ME                          D816234
06C     00 0079         236          DC     FRX              6D  DE                          D816235
06D     00 0079         237          ENDC                                                    D816236
                        238          DC     ILEG             6E                              D816237
06E     00 009B         239          DC     ILEG             6F                              D816238
06F     00 009B         240  *                                                               D816239
                        241  *                                                               D816240
                        242          IFZ    DPFP                                             D816241
070                     243          DC     ILEG             70                              D816242
070     00 009B         244          ENDC                                                    D816243
                        247          ENDC                                                    D816246
                        251          ENDC                                                    D816250
                        252          IFP    SFFP                                             D816251
071                     253          DC     LMSTM            71  STME                        D816252
071     00 000C         254          DC     LMSTM            72  LME                         D816253
072     00 000C         255          ENDC                                                    D816254
                        256          DC     ILEG             73                              D816255
073     00 009B         257          DC     ILEG             74                              D816256
074     00 009B         258          DC     ILEG             75                              D816257
075     00 009B         259          DC     ILEG             76                              D816258
076     00 009B         260          DC     ILEG             77                              D816259
077     00 009B         261          IFZ    DPFP                                             D816260
078                     262          DC     ILEG             78                              D816261
078     00 009B         263          DC     ILEG             79                              D816262
079     00 009B         264          DC     ILEG             7A                              D816263
07A     00 009B         265          DC     ILEG             7B                              D816264
07B     00 009B         266          DC     ILEG             7C                              D816265
07C     00 009B         267          DC     ILEG             7D                              D816266
07D     00 009B         268          DC     ILEG             7E                              D816267
07E     00 009B         269          DC     ILEG             7F                              D816268
07F     00 009B         270          ENDC                                                    D816269
                        280          ENDC                                                    D816279
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```
                                282     *                                                                   D816281
                                283     * OP-CODES  80 - 8F  ARE ILLEGAL                                   D816282
                                284     *                                                                   D816283
080     00 009B                 285             DC      ILEG                                                D816284
081     00 009B                 286             DC      ILEG                                                D816285
082     00 009B                 287             DC      ILEG                                                D816286
083     00 009B                 288             DC      ILEG                                                D816287
084     00 009B                 289             DC      ILEG                                                D816288
085     00 009B                 290             DC      ILEG                                                D816289
086     00 009B                 291             DC      ILEG                                                D816290
087     00 009B                 292             DC      ILEG                                                D816291
088     00 009B                 293             DC      ILEG                                                D816292
089     00 009B                 294             DC      ILEG                                                D816293
08A     00 009B                 295             DC      ILEG                                                D816294
08B     00 009B                 296             DC      ILEG                                                D816295
08C     00 009B                 297             DC      ILEG                                                D816296
08D     00 009B                 298             DC      ILEG                                                D816297
08E     00 009B                 299             DC      ILEG                                                D816298
08F     00 009B                 300             DC      ILEG                                                D816299
                                301     *                                                                   D816300
                                302     *                                                                   D816301
090     00 00D4                 303             DC      SLLS            90  SRLS                            D816302
091     00 00D4                 304             DC      SLLS            91  SLLS                            D816303
092     00 00C0                 305             DC      STBR            92  STBR                            D816304
093     00 00B6                 306             DC      LBR             93  LBR                             D816305
094     00 00C5                 307             DC      EXBR            94  EXBR                            D816306
095     00 00D0                 308             DC      EPSR            95  EPSR                            D816307
096     00 00DA                 309             DC      RBRWBR          96  WBR                             D816308
097     00 00DA                 310             DC      RBRWBR          97  RBR                             D816309
098     00 00D8                 311             DC      IORR            98  WHR                             D816310
099     00 00D8                 312             DC      IORR            99  RHR                             D816311
09A     00 00D8                 313             DC      IORR            9A  WDR                             D816312
09B     00 00D8                 314             DC      IORR            9B  RDR                             D816313
                                317             ENDC                                                        D816316
09C                             318             IFP     MPY.DIV                                             D816317
09C     00 00DD                 319             DC      MHUR            9C  MHUR                            D816318
                                320             ENDC                                                        D816319
09D     00 00D8                 321             DC      IORR            9D  SSR                             D816320
09E     00 00D8                 322             DC      IORR            9E  OCR                             D816321
09F     00 00D7                 323             DC      AIR             9F  AIR                             D816322
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```
                                325  *
                                326  * OP-CODES  A0 - AF  ARE ILLEGAL
                                327  *
0A0     00 009B                 328          DC    ILEG
0A1     00 009B                 329          DC    ILEG
0A2     00 009B                 330          DC    ILEG
0A3     00 009B                 331          DC    ILEG
0A4     00 009B                 332          DC    ILEG
0A5     00 009B                 333          DC    ILEG
0A6     00 009B                 334          DC    ILEG
0A7     00 009B                 335          DC    ILEG
0A8     00 009B                 336          DC    ILEG
0A9     00 009B                 337          DC    ILEG
0AA     00 009B                 338          DC    ILEG
0AB     00 009B                 339          DC    ILEG
0AC     00 009B                 340          DC    ILEG
0AD     00 009B                 341          DC    ILEG
0AE     00 009B                 342          DC    ILEG
0AF     00 009B                 343          DC    ILEG
                                344  *
                                345  * OP-CODES  B0 - BF  ARE ILLEGAL
                                346  *
0B0     00 009B                 347          DC    ILEG
0B1     00 009B                 348          DC    ILEG
0B2     00 009B                 349          DC    ILEG
0B3     00 009B                 350          DC    ILEG
0B4     00 009B                 351          DC    ILEG
0B5     00 009B                 352          DC    ILEG
0B6     00 009B                 353          DC    ILEG
0B7     00 009B                 354          DC    ILEG
0B8     00 009B                 355          DC    ILEG
0B9     00 009B                 356          DC    ILEG
0BA     00 009B                 357          DC    ILEG
0BB     00 009B                 358          DC    ILEG
0BC     00 009B                 359          DC    ILEG
0BD     00 009B                 360          DC    ILEG
0BE     00 009B                 361          DC    ILEG
0BF     00 009B                 362          DC    ILEG
```

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D816324
D816325
D816326
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D816361
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0C0   00 0012   364          DC   BX      C0  BXH     D816363
0C1   00 0012   365          DC   BX      C1  BXLE    D816364
0C2   00 0006   366          DC   RX      C2  LPSW    D816365
0C3   00 0002   367          DC   RS      C3  THI     D816366
0C4   00 0002   368          DC   RS      C4  NHI     D816367
0C5   00 0002   369          DC   RS      C5  CLHI    D816368
0C6   00 0002   370          DC   RS      C6  OHI     D816369
0C7   00 0002   371          DC   RS      C7  XHI     D816370
0C8   00 0002   372          DC   RS      C8  LHI     D816371
0C9   00 0002   373          DC   RS      C9  CHI     D816372
0CA   00 0002   374          DC   RS      CA  AHI     D816373
0CB   00 0002   375          DC   RS      CB  SHI     D816374
0CC   00 003D   376          DC   SLHL    CC  SRHL    D816375
0CD   00 003D   377          DC   SLHL    CD  SLHL    D816376
0CE   00 0047   378          DC   SLHA    CE  SRHA    D816377
0CF   00 0047   379          DC   SLHA    CF  SLHA    D816378
                380  *                                D816379
                381  *                                D816380
0D0   00 000C   382          DC   LMSTM   D0  STM     D816381
0D1   00 000C   383          DC   LMSTM   D1  LM      D816382
0D2   00 0006   384          DC   RX      D2  STB     D816383
0D3   00 0006   385          DC   RX      D3  LB      D816384
0D4   00 0006   386          DC   RX      D4  CLB     D816385
0D5   00 0008   387          DC   AL      D5  AL      D816386
0D6   00 0034   388          DC   RBWB    D6  WB      D816387
0D7   00 0034   389          DC   RBWB    D7  RB      D816388
0D8   00 0005   390          DC   IORX    D8  WH      D816389
0D9   00 0005   391          DC   IORX    D9  RH      D816390
0DA   00 0005   392          DC   IORX    DA  WD      D816391
0DB   00 0005   393          DC   IORX    DB  RD      D816392
                396          ENDC                    D816395
0DC             397          IFP  MPY.DIV            D816396
0DC   00 0006   398          DC   RX      DC  MHU     D816397
                399          ENDC                    D816398
0DD   00 0005   400          DC   IORX    DD  SS      D816399
0DE   00 0005   401          DC   IORX    DE  OC      D816400
0DF   00 0004   402          DC   AI      DF  AI      D816401
```

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0E0  00 009B  404          DC   ILEG        E0                D816403
0E1  00 0002  405          DC   RS          E1  SVC           D816404
0E2  00 0002  406          DC   RS          E2  SINT          D816405
0E3  00 009B  407          DC   ILEG        E3                D816406
0E4  00 009B  408          DC   ILEG        E4                D816407
0E5  00 009B  409          DC   ILEG        E5                D816408
0E6  00 009B  410          DC   ILEG        E6                D816409
0E7  00 009B  411          DC   ILEG        E7                D816410
0E8  00 009B  412          DC   ILEG        E8                D816411
0E9  00 009B  413          DC   ILEG        E9                D816412
0EA  00 004F  414          DC   SLL         EA  RRL           D816413
0EB  00 004F  415          DC   SLL         EB  RLL           D816414
0EC  00 004F  416          DC   SLL         EC  SRL           D816415
0ED  00 004F  417          DC   SLL         ED  SLL           D816416
0EE  00 004D  418          DC   SLA         EE  SRA           D816417
0EF  00 004D  419          DC   SLA         EF  SLA           D816418
              420  *                                          D816419
              421  * OP-CODES  F0 - FF  ARE ILLEGAL           D816420
              422  *                                          D816421
                                                              D816422
0F0  00 009B  423          DC   ILEG                          D816423
0F1  00 009B  424          DC   ILEG                          D816424
0F2  00 009B  425          DC   ILEG                          D816425
0F3  00 009B  426          DC   ILEG                          D816426
0F4  00 009B  427          DC   ILEG                          D816427
0F5  00 009B  428          DC   ILEG                          D816428
0F6  00 009B  429          DC   ILEG                          D816429
0F7  00 009B  430          DC   ILEG                          D816430
0F8  00 009B  431          DC   ILEG                          D816431
0F9  00 009B  432          DC   ILEG                          D816432
0FA  00 009B  433          DC   ILEG                          D816433
0FB  00 009B  434          DC   ILEG                          D816434
0FC  00 009B  435          DC   ILEG                          D816435
0FD  00 009B  436          DC   ILEG                          D816436
0FE  00 009B  437          DC   ILEG                          D816437
0FF  00 009B  438          DC   ILEG
```

MODEL 8/16 DROM2 DATA

```
                          440    *                                                    D816439
                          441    *                                                    D816440
100     00 0000           442           DC    0          00                          D816441
101     00 0000           443           DC    0          01  BALR                    D816442
102     00 0000           444           DC    0          02  BTCR                    D816443
103     00 0000           445           DC    0          03  BFCR                    D816444
104     00 0000           446           DC    0          04  NHR                     D816445
105     00 0000           447           DC    0          05  CLHR                    D816446
106     00 0000           448           DC    0          06  OHR                     D816447
107     00 0000           449           DC    0          07  XHR                     D816448
108     00 0000           450           DC    0          08  LHR                     D816449
109     00 0000           451           DC    0          09  CHR                     D816450
10A     00 0000           452           DC    0          0A  AHR                     D816451
10B     00 0000           453           DC    0          0B  SHR                     D816452
                          457           ENDC                                         D816456
10C                       458           IFP   MPY,DIV                              D816457
10C     00 0000           459           DC    0          0C  MHR                     D816458
10D     00 0000           460           DC    0          0D  DHR                     D816459
                          461           ENDC                                         D816460
10E     00 0000           462           DC    0          0E  ACHR                    D816461
10F     00 0000           463           DC    0          0F  SCHR                    D816462
                          464    *                                                    D816463
                          465    * OP=CODES  10 - 1F  ARE ILLEGAL                    D816464
                          466    *                                                    D816465
110     00 0000           467           DC    0                                      D816466
111     00 0000           468           DC    0                                      D816467
112     00 0000           469           DC    0                                      D816468
113     00 0000           470           DC    0                                      D816469
114     00 0000           471           DC    0                                      D816470
115     00 0000           472           DC    0                                      D816471
116     00 0000           473           DC    0                                      D816472
117     00 0000           474           DC    0                                      D816473
118     00 0000           475           DC    0                                      D816474
119     00 0000           476           DC    0                                      D816475
11A     00 0000           477           DC    0                                      D816476
11B     00 0000           478           DC    0                                      D816477
11C     00 0000           479           DC    0                                      D816478
11D     00 0000           480           DC    0                                      D816479
11E     00 0000           481           DC    0                                      D816480
11F     00 0000           482           DC    0                                      D816481
```

MODEL 8/16 DROM2 DATA

```
120  00 00AC   484          DC    BKWORD      20  BTBS    D816483
121  00 00AD   485          DC    FRWORD      21  BTFS    D816484
122  00 00AC   486          DC    BKWORD      22  BFBS    D816485
123  00 00AD   487          DC    FRWORD      23  BFFS    D816486
124  00 0095   488          DC    LHR         24  LIS     D816487
125  00 0000   489          DC    0           25  LCS     D816488
126  00 008E   490          DC    AHR         26  AIS     D816489
127  00 0090   491          DC    SHR         27  SIS     D816490
               501          ENDC                          D816500
128            502          IFP   SPFP                    D816501
128  00 0000   503          DC    0           28  LER     D816502
129  00 0000   504          DC    0           29  CER     D816503
12A  00 0000   505          DC    0           2A  AER     D816504
12B  00 0000   506          DC    0           2B  SER     D816505
12C  00 0000   507          DC    0           2C  MER     D816506
12D  00 0000   508          DC    0           2D  DER     D816507
12E  00 0000   509          DC    0           2E  FXR     D816508
12F  00 0000   510          DC    0           2F  FLR     D816509
               511          ENDC                          D816510
130            512          IFZ   DPFP                    D816511
               513    *                                   D816512
               514    * OP-CODES  30 - 3F  ARE ILLEGAL    D816513
               515    *                                   D816514
130  00 0000   516          DC    0                       D816515
131  00 0000   517          DC    0                       D816516
132  00 0000   518          DC    0                       D816517
133  00 0000   519          DC    0                       D816518
134  00 0000   520          DC    0                       D816519
135  00 0000   521          DC    0                       D816520
136  00 0000   522          DC    0                       D816521
137  00 0000   523          DC    0                       D816522
138  00 0000   524          DC    0                       D816523
139  00 0000   525          DC    0                       D816524
13A  00 0000   526          DC    0                       D816525
13B  00 0000   527          DC    0                       D816526
13C  00 0000   528          DC    0                       D816527
13D  00 0000   529          DC    0                       D816528
13E  00 0000   530          DC    0                       D816529
13F  00 0000   531          DC    0                       D816530
               532          ENDC                          D816531
               550          ENDC                          D816549
```

MODEL 8/16 DROM2 DATA

```
140  00 0084   552          DC    STH          40  STH    D816551
141  00 009F   553          DC    BALR         41  BALR   D816552
142  00 00A2   554          DC    BTCR         42  BTCR   D816553
143  00 00A4   555          DC    BFCR         43  BFCR   D816554
144  00 0092   556          DC    NHR          44  NH     D816555
145  00 0099   557          DC    CLHR         45  CLH    D816556
146  00 0093   558          DC    OHR          46  OH     D816557
147  00 0094   559          DC    XHR          47  XH     D816558
148  00 0095   560          DC    LHR          48  LH     D816559
149  00 0097   561          DC    CHR          49  CH     D816560
14A  00 008E   562          DC    AHR          4A  AH     D816561
14B  00 0090   563          DC    SHR          4B  SH     D816562
               567          ENDC                         D816566
14C            568          IFP   MPY,DIV                D816567
14C  00 00DC   569          DC    MHR          4C  MH     D816568
14D  00 00DB   570          DC    DHR          4D  DH     D816569
               571          ENDC                         D816570
14E  00 008D   572          DC    ACH          4E  ACH    D816571
14F  00 008F   573          DC    SCH          4F  SCH    D816572
               574     *                                  D816573
               575     * OP-CODES  50 - 5F  ARE ILLEGAL   D816574
               576     *                                  D816575
150  00 0000   577          DC    0                       D816576
151  00 0000   578          DC    0                       D816577
152  00 0000   579          DC    0                       D816578
153  00 0000   580          DC    0                       D816579
154  00 0000   581          DC    0                       D816580
155  00 0000   582          DC    0                       D816581
156  00 0000   583          DC    0                       D816582
157  00 0000   584          DC    0                       D816583
158  00 0000   585          DC    0                       D816584
159  00 0000   586          DC    0                       D816585
15A  00 0000   587          DC    0                       D816586
15B  00 0000   588          DC    0                       D816587
15C  00 0000   589          DC    0                       D816588
15D  00 0000   590          DC    0                       D816589
15E  00 0000   591          DC    0                       D816590
15F  00 0000   592          DC    0                       D816591
```

MODEL 8/16 DROM2 DATA

```
                        596             ENDC                                    D816595
    160                 597             IFP     SPFP                            D816596
    160     00 00E2     598             DC      STE             60  STE         D816597
                        599             ENDC                                    D816598
    161     00 0088     600             DC      AHM             61  AHM         D816599
    162     00 0000     601             DC      0               62              D816600
    163     00 0000     602             DC      0               63              D816601
    164     00 025E     603             DC      ATLD2           64  ATL         D816602
    165     00 0267     604             DC      ABLD2           65  ABL         D816603
    166     00 0278     605             DC      RTLD2           66  RTL         D816604
    167     00 027F     606             DC      RBLD2           67  RBL         D816605
                        614             ENDC                                    D816613
    168                 615             IFP     SPFP                            D816614
    168     00 02C6     616             DC      FRRD1           68  LE          D816615
    169     00 02BE     617             DC      CERD1           69  CE          D816616
    16A     00 02C6     618             DC      FRRD1           6A  AE          D816617
    16B     00 02C6     619             DC      FRRD1           6B  SE          D816618
    16C     00 02C6     620             DC      FRRD1           6C  ME          D816619
    16D     00 02C6     621             DC      FRRD1           6D  DE          D816620
                        622             ENDC                                    D816621
    16E     00 0000     623             DC      0               6E              D816622
    16F     00 0000     624             DC      0               6F              D816623
                        625     *                                               D816624
                        626     *                                               D816625
    170                 627             IFZ     DPFP                            D816626
    170     00 0000     628             DC      0                               D816627
                        629             ENDC                                    D816628
                        632             ENDC                                    D816631
                        636             ENDC                                    D816635
    171                 637             IFP     SPFP                            D816636
    171     00 009E     638             DC      STME            71  STME        D816637
    172     00 0091     639             DC      LME             72  LME         D816638
                        640             ENDC                                    D816639
    173     00 0000     641             DC      0                               D816640
    174     00 0000     642             DC      0                               D816641
    175     00 0000     643             DC      0                               D816642
    176     00 0000     644             DC      0                               D816643
    177     00 0000     645             DC      0                               D816644
    178                 646             IFZ     DPFP                            D816645
    178     00 0000     647             DC      0                               D816646
    179     00 0000     648             DC      0                               D816647
    17A     00 0000     649             DC      0                               D816648
    17B     00 0000     650             DC      0                               D816649
    17C     00 0000     651             DC      0                               D816650
    17D     00 0000     652             DC      0                               D816651
    17E     00 0000     653             DC      0                               D816652
    17F     00 0000     654             DC      0                               D816653
                        655             ENDC                                    D816654
                        665             ENDC                                    D816664
```

MODEL 8/16 DROM2 DATA

```
                                667     *                                                                   D816666
                                668     * OP-CODES  80 - 8F  ARE ILLEGAL                                   D816667
                                669     *                                                                   D816668
180     00 0000                 670             DC      0                                                   D816669
181     00 0000                 671             DC      0                                                   D816670
182     00 0000                 672             DC      0                                                   D816671
183     00 0000                 673             DC      0                                                   D816672
184     00 0000                 674             DC      0                                                   D816673
185     00 0000                 675             DC      0                                                   D816674
186     00 0000                 676             DC      0                                                   D816675
187     00 0000                 677             DC      0                                                   D816676
188     00 0000                 678             DC      0                                                   D816677
189     00 0000                 679             DC      0                                                   D816678
18A     00 0000                 680             DC      0                                                   D816679
18B     00 0000                 681             DC      0                                                   D816680
18C     00 0000                 682             DC      0                                                   D816681
18D     00 0000                 683             DC      0                                                   D816682
18E     00 0000                 684             DC      0                                                   D816683
18F     00 0000                 685             DC      0                                                   D816684
                                686     *                                                                   D816685
                                687     *                                                                   D816686
190     00 0064                 688             DC      SRHLD2          90      SRLS                        D816687
191     00 0051                 689             DC      SLHLD2          91      SLLS                        D816688
192     00 00A1                 690             DC      NOB             92      STBR                        D816689
193     00 0000                 691             DC      0               93      LBR                         D816690
194     00 00A1                 692             DC      NOB             94      EXBR                        D816691
195     00 0000                 693             DC      0               95      EPSR                        D816692
196     00 02ED                 694             DC      WBR             96      WBR                         D816693
197     00 02F0                 695             DC      RBR             97      RBR                         D816694
198     00 0025                 696             DC      WHR             98      WHR                         D816695
199     00 0021                 697             DC      RHR             99      RHR                         D816696
19A     00 0027                 698             DC      WDR             9A      WDR                         D816697
19B     00 0023                 699             DC      RDR             9B      RDR                         D816698
                                702             ENDC                                                        D816701
19C                             703             IFP     MPY.DIV                                             D816702
19C     00 0000                 704             DC      0               9C      MHUR                        D816703
                                705             ENDC                                                        D816704
19D     00 002C                 706             DC      SSR             9D      SSR                         D816705
19E     00 002F                 707             DC      OCR             9E      OCR                         D816706
19F     00 002C                 708             DC      SSR             9F      AIR                         D816707
```

MODEL 8/16 DROM2 DATA

```
                                  710  *                                                    D816709
                                  711  * OP-CODES  A0 - AF  ARE ILLEGAL                     D816710
                                  712  *                                                    D816711
1A0     00 0000                   713          DC    0                                     D816712
1A1     00 0000                   714          DC    0                                     D816713
1A2     00 0000                   715          DC    0                                     D816714
1A3     00 0000                   716          DC    0                                     D816715
1A4     00 0000                   717          DC    0                                     D816716
1A5     00 0000                   718          DC    0                                     D816717
1A6     00 0000                   719          DC    0                                     D816718
1A7     00 0000                   720          DC    0                                     D816719
1A8     00 0000                   721          DC    0                                     D816720
1A9     00 0000                   722          DC    0                                     D816721
1AA     00 0000                   723          DC    0                                     D816722
1AB     00 0000                   724          DC    0                                     D816723
1AC     00 0000                   725          DC    0                                     D816724
1AD     00 0000                   726          DC    0                                     D816725
1AE     00 0000                   727          DC    0                                     D816726
1AF     00 0000                   728          DC    0                                     D816727
                                  729  *                                                    D816728
                                  730  * OP-CODES  B0 - BF  ARE ILLEGAL                     D816729
                                  731  *                                                    D816730
1B0     00 0000                   732          DC    0                                     D816731
1B1     00 0000                   733          DC    0                                     D816732
1B2     00 0000                   734          DC    0                                     D816733
1B3     00 0000                   735          DC    0                                     D816734
1B4     00 0000                   736          DC    0                                     D816735
1B5     00 0000                   737          DC    0                                     D816736
1B6     00 0000                   738          DC    0                                     D816737
1B7     00 0000                   739          DC    0                                     D816738
1B8     00 0000                   740          DC    0                                     D816739
1B9     00 0000                   741          DC    0                                     D816740
1BA     00 0000                   742          DC    0                                     D816741
1BB     00 0000                   743          DC    0                                     D816742
1BC     00 0000                   744          DC    0                                     D816743
1BD     00 0000                   745          DC    0                                     D816744
1BE     00 0000                   746          DC    0                                     D816745
1BF     00 0000                   747          DC    0                                     D816746
```

MODEL 8/16 DROM2 DATA

```
1C0  00 00AF   749        DC   BXH          C0  BXH     D816748
1C1  00 00B1   750        DC   BXLE         C1  BXLE    D816749
1C2  00 00CE   751        DC   LPSW         C2  LPSW    D816750
1C3  00 008A   752        DC   THI          C3  THI     D816751
1C4  00 0092   753        DC   NHR          C4  NHI     D816752
1C5  00 0099   754        DC   CLHR         C5  CLHI    D816753
1C6  00 0093   755        DC   OHR          C6  OHI     D816754
1C7  00 0094   756        DC   XHR          C7  XHI     D816755
1C8  00 0095   757        DC   LHR          C8  LHI     D816756
1C9  00 0097   758        DC   CHR          C9  CHI     D816757
1CA  00 008E   759        DC   AHR          CA  AHI     D816758
1CB  00 0090   760        DC   SHR          CB  SHI     D816759
1CC  00 0064   761        DC   SRHLD2       CC  SRHL    D816760
1CD  00 0051   762        DC   SLHLD2       CD  SLHL    D816761
1CE  00 0061   763        DC   SRHAD2       CE  SRHA    D816762
1CF  00 005D   764        DC   SLHAD2       CF  SLHA    D816763
               765   *                                  D816764
               766   *                                  D816765
1D0  00 00CA   767        DC   STM          D0  STM     D816766
1D1  00 00C6   768        DC   LM           D1  LM      D816767
1D2  00 00BD   769        DC   STB          D2  STB     D816768
1D3  00 00B5   770        DC   LB           D3  LB      D816769
1D4  00 00B9   771        DC   CLR          D4  CLB     D816770
1D5  00 02F0   772        DC   RBR          D5  AL      D816771
1D6  00 02ED   773        DC   WBR          D6  WB      D816772
1D7  00 02F0   774        DC   RBR          D7  RB      D816773
1D8  00 0025   775        DC   WHR          D8  WH      D816774
1D9  00 0018   776        DC   RH           D9  RH      D816775
1DA  00 00E4   777        DC   WD           DA  WD      D816776
1DB  00 0018   778        DC   RD           DB  RD      D816777
               781        ENDC                         D816780
1DC            782        IFP  MPY,DIV                 D816781
1DC  00 00DD   783        DC   MHUR         DC  MHU     D816782
               784        ENDC                         D816783
1DD  00 0029   785        DC   SS           DD  SS      D816784
1DE  00 002E   786        DC   OC           DE  OC      D816785
1DF  00 0029   787        DC   SS           DF  AI      D816786
```

MODEL 8/16 DROM2 DATA

```
1E0  00 0000   789          DC   0          E0          D816788
1E1  00 00ED   790          DC   SVCD2      E1  SVC     D816789
1E2  00 0080   791          DC   SINT       E2  SINT    D816790
1E3  00 0000   792          DC   0          E3          D816791
1E4  00 0000   793          DC   0          E4          D816792
1E5  00 0000   794          DC   0          E5          D816793
1E6  00 0000   795          DC   0          E6          D816794
1E7  00 0000   796          DC   0          E7          D816795
1E8  00 0000   797          DC   0          E8          D816796
1E9  00 0000   798          DC   0          E9          D816797
1EA  00 006B   799          DC   RRLD2      EA  RRL     D816798
1EB  00 005A   800          DC   RLLD2      EB  RLL     D816799
1EC  00 0068   801          DC   SRLD2      EC  SRL     D816800
1ED  00 0054   802          DC   SLLD2      ED  SLL     D816801
1EE  00 006E   803          DC   SRAD2      EE  SRA     D816802
1EF  00 0074   804          DC   SLAD2      EF  SLA     D816803
               805  *                                   D816804
               806  * OP-CODES  F0 - FF  ARE ILLEGAL     D816805
               807  *                                   D816806
1F0  00 0000   808          DC   0                      D816807
1F1  00 0000   809          DC   0                      D816808
1F2  00 0000   810          DC   0                      D816809
1F3  00 0000   811          DC   0                      D816810
1F4  00 0000   812          DC   0                      D816811
1F5  00 0000   813          DC   0                      D816812
1F6  00 0000   814          DC   0                      D816813
1F7  00 0000   815          DC   0                      D816814
1F8  00 0000   816          DC   0                      D816815
1F9  00 0000   817          DC   0                      D816816
1FA  00 0000   818          DC   0                      D816817
1FB  00 0000   819          DC   0                      D816818
1FC  00 0000   820          DC   0                      D816819
1FD  00 0000   821          DC   0                      D816820
1FE  00 0000   822          DC   0                      D816821
1FF  00 0000   823          DC   0                      D816822
               824  *                                   D816823
200            825          END                         D816824
```

MODEL 8/16 DROM2 DATA

NO ERRORS

ABLO2	0267
ACH	008D
ADD	0195
ADDWRT	018B
AHM	0088
AHR	008E
AI	0004
AIR	00D7
AL	000B
AL1	030E
ALO1	0300
ALO2	0306
ALOC	0026
ALX	0310
APSW	0024
ATL1	0253
ATL2	0262
ATLABL	007E
ATLABLD1	0251
ATLO2	025E
BALR	009F
BFCR	00A4
BFS	00A8
BKWORD	00AC
BLKIO1	02E5
BLKIO2	02E6
BLKIO3	02E9
BLKRR1	02E1
BRANCH	00A0
BTCR	00A2
BTS	00A6
BX	0012
BX1	00B2
BXH	00AF
BXLE	00B1
BXNOB	00B4
BXNX	0014
CDD2	02B8
CER	00E1
CERD1	028E
CHR	0097
CLB	00B9
CLHR	0099
CLRWT	0175
CONINT	01EB
CONSER	015F
CONTIN	017F
DHR	00DB
DHR1	0200
DIFFER	02DC
DISPLY	019D
DPFP	C000
EPSR	00D0

MODEL 8/16 DROM2 DATA

EPSR1	0330
EPSR2	033A
EPSR3	033C
EXBR	00C5
F.CC	02C8
F.VARI	0003
FDRXD2	02C0
FINISH	00FB
FL.OV	02D4
FLR	00DF
FLRD1	02CD
FLRD11	02CE
FLT1	01CB
FLT2	01D2
FLT3	01DF
FLT4	01E2
FLT5	01E4
FLTDISP	01C5
FN1	01AC
FN11	01B8
FN2,FN3	01B0
FNREG	0183
FROMALI	02F1
FRR	00E0
FRRD1	02C6
FRWORD	00AD
FRX	0079
FRXD1	02A5
FRXNX	02A7
FXR	00DE
FXR2	02CB
FXRD1	02C9
GENSWPL	0321
HELP	0197
HELP1	0198
IDLE	0134
IDLE1	0136
IDLEX	015E
ILEG	009B
ILGPSW	0030
IMM	008C
IOATN	01E7
IORR	00D8
IORX	0005
IOSVC	01EA
LB	00B5
LBR	00B6
LCS	0096
LDDOUBLE	0113
LDRES	010A
LDSINGLE	011F
LEADER	0317
LHR	0095
LIST.OV	028A

MODEL 8/16 DROM2 DATA

LM	00C6
LMD	008B
LMDD2	028B
LME	0091
LMED2	0291
LMEDONE	030C
LMNX	000E
LMSTM	000C
LOCDIS	012C
LOOK20	018B
LPSW	00CE
LPSW1	032C
LSET	032B
MAR0	012E
MHR	00DC
MHR1	0232
MHUR	00DD
MHUR1	0248
MMALF	031E
MMALF1	0320
MME	0179
MPY.DIV	0001
MRONEG	0207
MROPOS	0205
NHR	0092
NLONG	0067
NNEG1	0238
NNEG2	023C
NOB	00A1
NOWRAP1	0261
NOWRAP4	0284
OC	002E
OCR	002F
OHR	0093
OIPSW	0040
OMMPSW	0038
OUTDIS	012F
OV	0225
OV1	022A
PNTR	0022
POW	0157
PSWLOC	01B6
PWRDWN	0138
PWRDWN2	014D
PWRUP	0100
PWRUP2	0119
PWRUP3	0125
QNEG	0222
QOK	021F
QOK1	024F
QUEINT	0322
QUENBL	0332
RB1	02F3
RBLD2	027F

MODEL 8/16 DROM2 DATA

RBR	02F0
RBRWBR	00DA
RBRWBRD1	02DF
RBWB	0034
RBWBNX	0038
RD	0018
RD2	0019
RDKEY	018F
RDR	0023
REGDIS	01BF
REGN	01C0
RH	001B
RHH	001E
RHR	0021
RLLD2	005A
RNNEG	021B
RRLD2	006B
RS	0002
RSNX	000A
RTL1	026F
RTL2	0285
RTLD2	0278
RTLRBLI	007F
RTLRBLD1	026D
RX	0006
RXNX	0008
SAVREG	0140
SCH	008F
SHIFTD	00E6
SHORTBI	00A9
SNR	0090
SINT	0080
SINT1	01ED
SINT2	01F6
SLA	004D
SLAD2	0074
SLHA	0047
SLHA1	0048
SLHAD2	005D
SLHL	003D
SLHL2	003E
SLHL3	003F
SLHLD2	0051
SLHLNX	0042
SLL	004F
SLL1D2	0056
SLLD2	0054
SLLS	00D4
SPFP	0001
SRAD2	006E
SRHAD2	0061
SRHL1	0065
SRHLD2	0064
SRL1D2	0069

MODEL 8/16 DROM2 DATA

SRLD2	0068
SS	0029
SSR	002C
START	0000
START1	0001
STB	00BD
STBR	00C0
STD	00E3
STDD2	02AF
STDOUBLE	0149
STE	00E2
STE,STD	007A
STED2	02B3
STENX	007C
STH	0084
STH2	0086
STM	00CA
STMD	009A
STMOD2	029A
STME	009E
STMED2	029E
STSINGLE	0153
SVCD2	00ED
TERMIN	00FC
THI	008A
THRUD2	0046
WAIT	0159
WAIT1	015C
WASEMPTY	028A
WBR	02ED
WD	00E4
WDR	0027
WHR	0025
XHR	0094
YONNEG	020D

PROG= M816DF04 ASSEMBLED BY MICROCAL II (32-BIT)

```
0004                                    2   F.VARI  EQU  4                  F04 : BASIC + M/D + SPFP + DPFP   D816001
                                        3   *                                                                 D816002
                                        4           NLSTC                                                     D816003
                                        5   *                                                                 D816004
                                        6           SQCHK                                                     D816005
                                        7   *                                                                 D816006
                                        8   *                                                                 D816007
                                        9   * SET UP SYSGEN PARAMETERS                                        D816008
                                       10   *                                                                 D816009
000                                    11           IFP   F.VARI-1                                            D816010
 0001                                  12   MPY.DIV EQU  1                                                    D816011
                                       15           ENDC                                                      D816014
000                                    16           IFP   F.VARI-2                                            D816015
 0001                                  17   SPFP    EQU  1                                                    D816016
                                       20           ENDC                                                      D816019
000                                    21           IFP   F.VARI-3                                            D816020
 0001                                  22   DPFP    EQU  1                                                    D816021
                                       25           ENDC                                                      D816024
                                       26   *                                                                 D816025
                                       27   *                                                                 D816026
                                       28   *                                                                 D816027
                                       29   *                                                                 D816028
                                       30   * COPYRIGHT INTERDATA INC.  SEPTEMBER 1976                        D816029
                                       31   *                                                                 D816030
                                       32   *                                                                 D816031
                                       33   * DHEMA MAHAJAN                                                  D816032
                                       34   *                                                                 D816033
                                       35   *                                                                 D816034
                                       36   * DROM SOURCE IS ASSEMBLED IN CONJUNCTION WITH THE MICROPROGRAM SOURCE  D816035
                                       37   * OPERAND FIELD IS THE SYMBOLIC ROM ENTRY POINT FOR D1            D816036
                                       38   * COMMENT FIELD SHOWS OP-CODE AND VALID INSTRUCTION MNEMONIC      D816037
                                       39   * ONLY THE LEAST SIGNIFICANT BYTE OF THE CODE GENERATED IS USED   D816038
                                       40           PARTS 19-186R00F00      DUMMY PART #                     D816039
                                       41           PARTS 19-186R00F00      DUMMY PART #                     D816040
                                       42   * THE DROM DATA IS CONTAINED IN THE FOLLOWING 512 X 8 (4K) ROM CHIP  D816041
                                       43   *                                                                 D816042
                                       46           ENDC                                                      D816045
                                       49           ENDC                                                      D816048
                                       52           ENDC                                                      D816051
000                                    53           IFZ   F.VARI-4                                            D816052
                                       54           PARTS 19-186R00F30                                        D816053
                                       55           ENDC                                                      D816054
                                       56   *                                                                 D816055
000     00 009B                        57           DC    ILEG          00                                    D816056
001     00 009F                        58           DC    BALR          01  BALR                              D816057
002     00 00A2                        59           DC    BTCR          02  BTCR                              D816058
003     00 00A4                        60           DC    BFCR          03  BFCR                              D816059
004     00 0092                        61           DC    NHR           04  NHR                               D816060
005     00 0099                        62           DC    CLHR          05  CLHR                              D816061
006     00 0093                        63           DC    OHR           06  OHR                               D816062
007     00 0094                        64           DC    XHR           07  XHR                               D816063
008     00 0095                        65           DC    LHR           08  LHR                               D816064
009     00 0097                        66           DC    CHR           09  CHR                               D816065
00A     00 008E                        67           DC    AHR           0A  AHR                               D816066
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008     00 0090          68          DC    SHR                 08  SHR          D816067
                         72          ENDC                                       D816071
00C                      73          IFP   MPY,DIV                            D816072
00C     00 00DC          74          DC    MHR                 0C  MHR          D816073
00D     00 00DB          75          DC    DHR                 0D  DHR          D816074
                         76          ENDC                                       D816075
00E     00 008D          77          DC    ACH                 0E  ACHR         D816076
00F     00 008F          78          DC    SCH                 0F  SCHR         D816077
                         79    *                                                D816078
                         80    * OP-CODES  10 - 1F  ARE ILLEGAL                 D816079
                         81    *                                                D816080
010     00 009B          82          DC    ILEG                                 D816081
011     00 009B          83          DC    ILEG                                 D816082
012     00 009B          84          DC    ILEG                                 D816083
013     00 009B          85          DC    ILEG                                 D816084
014     00 009B          86          DC    ILEG                                 D816085
015     00 009B          87          DC    ILEG                                 D816086
016     00 009B          88          DC    ILEG                                 D816087
017     00 009B          89          DC    ILEG                                 D816088
018     00 009B          90          DC    ILEG                                 D816089
019     00 009B          91          DC    ILEG                                 D816090
01A     00 009B          92          DC    ILEG                                 D816091
01B     00 009B          93          DC    ILEG                                 D816092
01C     00 009B          94          DC    ILEG                                 D816093
01D     00 009B          95          DC    ILEG                                 D816094
01E     00 009B          96          DC    ILEG                                 D816095
01F     00 009B          97          DC    ILEG                                 D816096
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020   00 00A6    99    DC   BTS     20  BTBS    D816098
021   00 00A6   100    DC   BTS     21  BTFS    D816099
022   00 00A8   101    DC   BFS     22  BFBS    D816100
023   00 00A8   102    DC   BFS     23  BFFS    D816101
024   00 008C   103    DC   IMM     24  LIS     D816102
025   00 0096   104    DC   LCS     25  LCS     D816103
026   00 008C   105    DC   IMM     26  AIS     D816104
027   00 008C   106    DC   IMM     27  SIS     D816105
                116    ENDC                    D816115
                117    IFP  SPFP               D816116
028                                             D816117
028   00 00E0   118    DC   FRR     28  LER     D816118
029   00 00E1   119    DC   CER     29  CER     D816119
02A   00 00E0   120    DC   FRR     2A  AER     D816120
02B   00 00E0   121    DC   FRR     2B  SER     D816121
02C   00 00E0   122    DC   FRR     2C  MER     D816122
02D   00 00E0   123    DC   FRR     2D  DER     D816123
02E   00 00DE   124    DC   FXR     2E  FXR     D816124
02F   00 00DF   125    DC   FLR     2F  FLR     D816125
                126    ENDC                    D816146
                147    ENDC                    D816147
                148    IFP  DPFP               D816148
030                                             D816149
030   00 009B   149    DC   ILEG    30          D816150
031   00 009B   150    DC   ILEG    31          D816151
032   00 009B   151    DC   ILEG    32          D816152
033   00 009B   152    DC   ILEG    33          D816153
034   00 009B   153    DC   ILEG    34          D816154
035   00 009B   154    DC   ILEG    35          D816155
036   00 009B   155    DC   ILEG    36          D816156
037   00 009B   156    DC   ILEG    37          D816157
038   00 00E0   157    DC   FRR     38  LDR     D816158
039   00 00E1   158    DC   CER     39  CDR     D816159
03A   00 00E0   159    DC   FRR     3A  ADR     D816160
03B   00 00E0   160    DC   FRR     3B  SDR     D816161
03C   00 00E0   161    DC   FRR     3C  MDR     D816162
03D   00 00E0   162    DC   FRR     3D  DDR     D816163
03E   00 00DE   163    DC   FXR     3E  FXDR    D816164
03F   00 00DF   164    DC   FLR     3F  FLDR
                165    ENDC
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040  00 0002  167          DC   RS          40  STH   D816166
041  00 0002  168          DC   RS          41  BAL   D816167
042  00 0002  169          DC   RS          42  BTC   D816168
043  00 0002  170          DC   RS          43  BFC   D816169
044  00 0006  171          DC   RX          44  NH    D816170
045  00 0006  172          DC   RX          45  CLH   D816171
046  00 0006  173          DC   RX          46  OH    D816172
047  00 0006  174          DC   RX          47  XH    D816173
048  00 0006  175          DC   RX          48  LH    D816174
049  00 0006  176          DC   RX          49  CH    D816175
04A  00 0006  177          DC   RX          4A  AH    D816176
04B  00 0006  178          DC   RX          4B  SH    D816177
              182          ENDC                       D816181
04C           183          IFP  MPY,DIV               D816182
04C  00 0006  184          DC   RX          4C  MH    D816183
04D  00 0006  185          DC   RX          4D  OH    D816184
              186          ENDC                       D816185
04E  00 0006  187          DC   RX          4E  ACH   D816186
04F  00 0006  188          DC   RX          4F  SCH   D816187
              189     *                               D816188
              190     * OP-CODES  50 - 5F  ARE ILLEGAL D816189
              191     *                               D816190
050  00 009B  192          DC   ILEG                  D816191
051  00 009B  193          DC   ILEG                  D816192
052  00 009B  194          DC   ILEG                  D816193
053  00 009B  195          DC   ILEG                  D816194
054  00 009B  196          DC   ILEG                  D816195
055  00 009B  197          DC   ILEG                  D816196
056  00 009B  198          DC   ILEG                  D816197
057  00 009B  199          DC   ILEG                  D816198
058  00 009B  200          DC   ILEG                  D816199
059  00 009B  201          DC   ILEG                  D816200
05A  00 009B  202          DC   ILEG                  D816201
05B  00 009B  203          DC   ILEG                  D816202
05C  00 009B  204          DC   ILEG                  D816203
05D  00 009B  205          DC   ILEG                  D816204
05F  00 009B  206          DC   ILEG                  D816205
05F  00 009B  207          DC   ILEG                  D816206
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                        211          ENDC                                                    D816210
                        212          IFP    SPFP                                             D816211
060                     213          DC     STE,STD          60  STE                         D816212
060     00 007A         214          ENDC                                                    D816213
061     00 0006         215          DC     RX               61  AHM                         D816214
062     00 009B         216          DC     ILEG             62                              D816215
063     00 009B         217          DC     ILEG             63                              D816216
064     00 007E         218          DC     ATLABL           64  ATL                         D816217
065     00 007E         219          DC     ATLABL           65  ABL                         D816218
066     00 007F         220          DC     RTLRBL           66  RTL                         D816219
067     00 007F         221          DC     RTLRBL           67  RBL                         D816220
                        229          ENDC                                                    D816228
068                     230          IFP    SPFP                                             D816229
068     00 0079         231          DC     FRX              68  LE                          D816230
069     00 0079         232          DC     FRX              69  CE                          D816231
06A     00 0079         233          DC     FRX              6A  AE                          D816232
06B     00 0079         234          DC     FRX              6B  SE                          D816233
06C     00 0079         235          DC     FRX              6C  ME                          D816234
06D     00 0079         236          DC     FRX              6D  DE                          D816235
                        237          ENDC                                                    D816236
06E     00 009B         238          DC     ILEG             6E                              D816237
06F     00 009B         239          DC     ILEG             6F                              D816238
                        240  *                                                               D816239
                        241  *                                                               D816240
                        244          ENDC                                                    D816243
                        245          IFP    DPFP                                             D816244
070                     246          DC     STE,STD          70  STD                         D816245
070     00 007A         247          ENDC                                                    D816246
                        251          ENDC                                                    D816250
                        252          IFP    SPFP                                             D816251
071                     253          DC     LMSTM            71  STME                        D816252
071     00 000C         254          DC     LMSTM            72  LME                         D816253
072     00 000C         255          ENDC                                                    D816254
073     00 009B         256          DC     ILEG             73                              D816255
074     00 009B         257          DC     ILEG             74                              D816256
075     00 009B         258          DC     ILEG             75                              D816257
076     00 009B         259          DC     ILEG             76                              D816258
077     00 009B         260          DC     ILEG             77                              D816259
                        270          ENDC                                                    D816269
                        271          IFP    DPFP                                             D816270
078                     272          DC     FRX              78  LD                          D816271
078     00 0079         273          DC     FRX              79  CD                          D816272
079     00 0079         274          DC     FRX              7A  AD                          D816273
07A     00 0079         275          DC     FRX              7B  SD                          D816274
07B     00 0079         276          DC     FRX              7C  MD                          D816275
07C     00 0079         277          DC     FRX              7D  DD                          D816276
07D     00 0079         278          DC     LMSTM            7E  STMD                        D816277
07E     00 000C         279          DC     LMSTM            7F  LMD                         D816278
07F     00 000C         280          ENDC                                                    D816279
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                                282     *                                                                   D816281
                                283     * OP-CODES  80 - 8F  ARE ILLEGAL                                   D816282
                                284     *                                                                   D816283
080     00 009B                 285             DC      ILEG                                                D816284
081     00 009B                 286             DC      ILEG                                                D816285
082     00 009B                 287             DC      ILEG                                                D816286
083     00 009B                 288             DC      ILEG                                                D816287
084     00 009B                 289             DC      ILEG                                                D816288
085     00 009B                 290             DC      ILEG                                                D816289
086     00 009B                 291             DC      ILEG                                                D816290
087     00 009B                 292             DC      ILEG                                                D816291
088     00 009B                 293             DC      ILEG                                                D816292
089     00 009B                 294             DC      ILEG                                                D816293
08A     00 009B                 295             DC      ILEG                                                D816294
08B     00 009B                 296             DC      ILEG                                                D816295
08C     00 009B                 297             DC      ILEG                                                D816296
08D     00 009B                 298             DC      ILEG                                                D816297
08E     00 009B                 299             DC      ILEG                                                D816298
08F     00 009B                 300             DC      ILEG                                                D816299
                                301     *                                                                   D816300
                                302     *                                                                   D816301
090     00 00D4                 303             DC      SLLS            90  SRLS                            D816302
091     00 00D4                 304             DC      SLLS            91  SLLS                            D816303
092     00 00C0                 305             DC      STBR            92  STBR                            D816304
093     00 00B6                 306             DC      LBR             93  LBR                             D816305
094     00 00C5                 307             DC      EXBR            94  EXBR                            D816306
095     00 00D0                 308             DC      EPSR            95  EPSR                            D816307
096     00 00DA                 309             DC      RBRWBR          96  WBR                             D816308
097     00 00DA                 310             DC      RBRWBR          97  RBR                             D816309
098     00 00D8                 311             DC      IORR            98  WHR                             D816310
099     00 00D8                 312             DC      IORR            99  RHR                             D816311
09A     00 00D8                 313             DC      IORR            9A  WDR                             D816312
09B     00 00D8                 314             DC      IORR            9B  RDR                             D816313
                                317             ENDC                                                        D816316
09C                             318             IFP     MPY.DIV                                             D816317
09C     00 00DD                 319             DC      MHUR            9C  MHUR                            D816318
                                320             ENDC                                                        D816319
09D     00 00D8                 321             DC      IORR            9D  SSR                             D816320
09E     00 00D8                 322             DC      IORR            9E  OCR                             D816321
09F     00 00D7                 323             DC      AIR             9F  AIR                             D816322
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                                  325     *
                                  326     * OP-CODES  A0 - AF  ARE ILLEGAL
                                  327     *
0A0     00 009B                   328             DC    ILEG
0A1     00 009B                   329             DC    ILEG
0A2     00 009B                   330             DC    ILEG
0A3     00 009B                   331             DC    ILEG
0A4     00 009B                   332             DC    ILEG
0A5     00 009B                   333             DC    ILEG
0A6     00 009B                   334             DC    ILEG
0A7     00 009B                   335             DC    ILEG
0A8     00 009B                   336             DC    ILEG
0A9     00 009B                   337             DC    ILEG
0AA     00 009B                   338             DC    ILEG
0AB     00 009B                   339             DC    ILEG
0AC     00 009B                   340             DC    ILEG
0AD     00 009B                   341             DC    ILEG
0AE     00 009B                   342             DC    ILEG
0AF     00 009B                   343             DC    ILEG
                                  344     *
                                  345     * OP-CODES  B0 - BF  ARE ILLEGAL
                                  346     *
0B0     00 009B                   347             DC    ILEG
0B1     00 009B                   348             DC    ILEG
0B2     00 009B                   349             DC    ILEG
0B3     00 009B                   350             DC    ILEG
0B4     00 009B                   351             DC    ILEG
0B5     00 009B                   352             DC    ILEG
0B6     00 009B                   353             DC    ILEG
0B7     00 009B                   354             DC    ILEG
0B8     00 009B                   355             DC    ILEG
0B9     00 009B                   356             DC    ILEG
0BA     00 009B                   357             DC    ILEG
0BB     00 009B                   358             DC    ILEG
0BC     00 009B                   359             DC    ILEG
0BD     00 009B                   360             DC    ILEG
0BE     00 009B                   361             DC    ILEG
0BF     00 009B                   362             DC    ILEG

D816324
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0C0   00 0012   364        DC   BX      C0  BXH    D816363
0C1   00 0012   365        DC   BX      C1  BXLE   D816364
0C2   00 0006   366        DC   RX      C2  LPSW   D816365
0C3   00 0002   367        DC   RS      C3  THI    D816366
0C4   00 0002   368        DC   RS      C4  NHI    D816367
0C5   00 0002   369        DC   RS      C5  CLHI   D816368
0C6   00 0002   370        DC   RS      C6  OHI    D816369
0C7   00 0002   371        DC   RS      C7  XHI    D816370
0C8   00 0002   372        DC   RS      C8  LHI    D816371
0C9   00 0002   373        DC   RS      C9  CHI    D816372
0CA   00 0002   374        DC   RS      CA  AHI    D816373
0CB   00 0002   375        DC   RS      CB  SHI    D816374
0CC   00 003D   376        DC   SLHL    CC  SRHL   D816375
0CD   00 003D   377        DC   SLHL    CD  SLHL   D816376
0CE   00 0047   378        DC   SLHA    CE  SRHA   D816377
0CF   00 0047   379        DC   SLHA    CF  SLHA   D816378
                380   *                            D816379
                381   *                            D816380
0D0   00 000C   382        DC   LMSTM   D0  STM    D816381
0D1   00 000C   383        DC   LMSTM   D1  LM     D816382
0D2   00 0006   384        DC   RX      D2  STB    D816383
0D3   00 0006   385        DC   RX      D3  LB     D816384
0D4   00 0006   386        DC   RX      D4  CLB    D816385
0D5   00 000B   387        DC   AL      D5  AL     D816386
0D6   00 0034   388        DC   RBWB    D6  WB     D816387
0D7   00 0034   389        DC   RBWB    D7  RB     D816388
0D8   00 0005   390        DC   IORX    D8  WH     D816389
0D9   00 0005   391        DC   IORX    D9  RH     D816390
0DA   00 0005   392        DC   IORX    DA  WD     D816391
0DB   00 0005   393        DC   IORX    DB  RD     D816392
                396        ENDC                   D816395
0DC             397        IFP  MPY.DIV           D816396
0DC   00 0006   398        DC   RX      DC  MHU    D816397
                399        ENDC                   D816398
0DD   00 0005   400        DC   IORX    DD  SS     D816399
0DE   00 0005   401        DC   IORX    DE  OC     D816400
0DF   00 0004   402        DC   AI      DF  AI     D816401
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0E0  00 009B   404          DC   ILEG        E0          D816403
0E1  00 0002   405          DC   RS          E1  SVC     D816404
0E2  00 0002   406          DC   RS          E2  SINT    D816405
0E3  00 009B   407          DC   ILEG        E3          D816406
0E4  00 009B   408          DC   ILEG        E4          D816407
0E5  00 009B   409          DC   ILEG        E5          D816408
0E6  00 009B   410          DC   ILEG        E6          D816409
0E7  00 009B   411          DC   ILEG        E7          D816410
0E8  00 009B   412          DC   ILEG        E8          D816411
0E9  00 009B   413          DC   ILEG        E9          D816412
0EA  00 004F   414          DC   SLL         EA  RRL     D816413
0EB  00 004F   415          DC   SLL         EB  RLL     D816414
0EC  00 004F   416          DC   SLL         EC  SRL     D816415
0ED  00 004F   417          DC   SLL         ED  SLL     D816416
0EE  00 004D   418          DC   SLA         EE  SRA     D816417
0EF  00 004D   419          DC   SLA         EF  SLA     D816418
               420  *                                    D816419
               421  * OP-CODES  F0 - FF  ARE ILLEGAL      D816420
               422  *                                    D816421
0F0  00 009B   423          DC   ILEG                    D816422
0F1  00 009B   424          DC   ILEG                    D816423
0F2  00 009B   425          DC   ILEG                    D816424
0F3  00 009B   426          DC   ILEG                    D816425
0F4  00 009B   427          DC   ILEG                    D816426
0F5  00 009B   428          DC   ILEG                    D816427
0F6  00 009B   429          DC   ILEG                    D816428
0F7  00 009B   430          DC   ILEG                    D816429
0F8  00 009B   431          DC   ILEG                    D816430
0F9  00 009B   432          DC   ILEG                    D816431
0FA  00 009B   433          DC   ILEG                    D816432
0FB  00 009B   434          DC   ILEG                    D816433
0FC  00 009B   435          DC   ILEG                    D816434
0FD  00 009B   436          DC   ILEG                    D816435
0FE  00 009B   437          DC   ILEG                    D816436
0FF  00 009B   438          DC   ILEG                    D816437
```

MODEL 8/16 DROM2 DATA

```
                                440   *                                                                    D816439
                                441   *                                                                    D816440
100     00 0000                 442           DC    0                    00                              D816441
101     00 0000                 443           DC    0                    01  BALR                        D816442
102     00 0000                 444           DC    0                    02  BTCR                        D816443
103     00 0000                 445           DC    0                    03  BFCR                        D816444
104     00 0000                 446           DC    0                    04  NHR                         D816445
105     00 0000                 447           DC    0                    05  CLHR                        D816446
106     00 0000                 448           DC    0                    06  OHR                         D816447
107     00 0000                 449           DC    0                    07  XHR                         D816448
108     00 0000                 450           DC    0                    08  LHR                         D816449
109     00 0000                 451           DC    0                    09  CHR                         D816450
10A     00 0000                 452           DC    0                    0A  AHR                         D816451
10B     00 0000                 453           DC    0                    0B  SHR                         D816452
                                457           ENDC                                                       D816456
10C                             458           IFP   MPY.DIV                                              D816457
10C     00 0000                 459           DC    0                    0C  MHR                         D816458
10D     00 0000                 460           DC    0                    0D  DHR                         D816459
                                461           ENDC                                                       D816460
10E     00 0000                 462           DC    0                    0E  ACHR                        D816461
10F     00 0000                 463           DC    0                    0F  SCHR                        D816462
                                464   *                                                                    D816463
                                465   * OP-CODES  10 - 1F  ARE ILLEGAL                                     D816464
                                466   *                                                                    D816465
110     00 0000                 467           DC    0                                                    D816466
111     00 0000                 468           DC    0                                                    D816467
112     00 0000                 469           DC    0                                                    D816468
113     00 0000                 470           DC    0                                                    D816469
114     00 0000                 471           DC    0                                                    D816470
115     00 0000                 472           DC    0                                                    D816471
116     00 0000                 473           DC    0                                                    D816472
117     00 0000                 474           DC    0                                                    D816473
118     00 0000                 475           DC    0                                                    D816474
119     00 0000                 476           DC    0                                                    D816475
11A     00 0000                 477           DC    0                                                    D816476
11B     00 0000                 478           DC    0                                                    D816477
11C     00 0000                 479           DC    0                                                    D816478
11D     00 0000                 480           DC    0                                                    D816479
11E     00 0000                 481           DC    0                                                    D816480
11F     00 0000                 482           DC    0                                                    D816481
```

MODEL 8/16 DROM2 DATA

```
120  00 00AC   484          DC   BKWORD      20  BTBS     D816483
121  00 00AD   485          DC   FRWORD      21  BTFS     D816484
122  00 00AC   486          DC   BKWORD      22  BFBS     D816485
123  00 00AD   487          DC   FRWORD      23  BFFS     D816486
124  00 0095   488          DC   LHR         24  LIS      D816487
125  00 0000   489          DC   0           25  LCS      D816488
126  00 008E   490          DC   AHR         26  AIS      D816489
127  00 0090   491          DC   SHR         27  SIS      D816490
               501          ENDC                         D816500
                                                          D816501
128            502          IFP  SPFP                    D816502
128  00 0000   503          DC   0           28  LER      D816503
129  00 0000   504          DC   0           29  CER      D816504
12A  00 0000   505          DC   0           2A  AER      D816505
12B  00 0000   506          DC   0           2B  SER      D816506
12C  00 0000   507          DC   0           2C  MER      D816507
12D  00 0000   508          DC   0           2D  DER      D816508
12E  00 0000   509          DC   0           2E  FXR      D816509
12F  00 0000   510          DC   0           2F  FLR      D816510
               511          ENDC                         D816531
               532          ENDC                         D816532
130            533          IFP  DPFP                    D816533
130  00 0000   534          DC   0           30           D816534
131  00 0000   535          DC   0           31           D816535
132  00 0000   536          DC   0           32           D816536
133  00 0000   537          DC   0           33           D816537
134  00 0000   538          DC   0           34           D816538
135  00 0000   539          DC   0           35           D816539
136  00 0000   540          DC   0           36           D816540
137  00 0000   541          DC   0           37           D816541
138  00 0000   542          DC   0           38  LDR      D816542
139  00 0000   543          DC   0           39  CDR      D816543
13A  00 0000   544          DC   0           3A  ADR      D816544
13B  00 0000   545          DC   0           3B  SDR      D816545
13C  00 0000   546          DC   0           3C  MDR      D816546
13D  00 0000   547          DC   0           3D  DDR      D816547
13E  00 0000   548          DC   0           3E  FXDR     D816548
13F  00 0000   549          DC   0           3F  FLDR     D816549
               550          ENDC
```

MODEL 8/16 DROM2 DATA

```
140  00 0084   552          DC   STH          40 STH   D816551
141  00 009F   553          DC   BALR         41 BALR  D816552
142  00 00A2   554          DC   BTCR         42 BTCR  D816553
143  00 00A4   555          DC   BFCR         43 BFCR  D816554
144  00 0092   556          DC   NHR          44 NH    D816555
145  00 0099   557          DC   CLHR         45 CLH   D816556
146  00 0093   558          DC   OHR          46 OH    D816557
147  00 0094   559          DC   XHR          47 XH    D816558
148  00 0095   560          DC   LHR          48 LH    D816559
149  00 0097   561          DC   CHR          49 CH    D816560
14A  00 008E   562          DC   AHR          4A AH    D816561
14B  00 0090   563          DC   SHR          4B SH    D816562
               567          ENDC              D816566
14C            568          IFP  MPY.DIV      D816567
14C  00 00DC   569          DC   MHR          4C MH    D816568
14D  00 000B   570          DC   DHR          4D DH    D816569
               571          ENDC              D816570
14E  00 008D   572          DC   ACH          4E ACH   D816571
14F  00 008F   573          DC   SCH          4F SCH   D816572
               574     *                      D816573
               575     * OP-CODES  50 - 5F  ARE ILLEGAL  D816574
               576     *                      D816575
150  00 0000   577          DC   0            D816576
151  00 0000   578          DC   0            D816577
152  00 0000   579          DC   0            D816578
153  00 0000   580          DC   0            D816579
154  00 0000   581          DC   0            D816580
155  00 0000   582          DC   0            D816581
156  00 0000   583          DC   0            D816582
157  00 0000   584          DC   0            D816583
158  00 0000   585          DC   0            D816584
159  00 0000   586          DC   0            D816585
15A  00 0000   587          DC   0            D816586
15B  00 0000   588          DC   0            D816587
15C  00 0000   589          DC   0            D816588
15D  00 0000   590          DC   0            D816589
15E  00 0000   591          DC   0            D816590
15F  00 0000   592          DC   0            D816591
```

MODEL 8/16 DROM2 DATA

```
                        596          ENDC                                                    D816595
                        597          IFP    SPFP                                             D816596
160                     598          DC     STE          60  STE                         D816597
160     00 00E2         599          ENDC                                                    D816598
                        600          DC     AHM          61  AHM                         D816599
161     00 0088         601          DC     0            62                              D816600
162     00 0000         602          DC     0            63                              D816601
163     00 0000         603          DC     ATLD2        64  ATL                         D816602
164     00 025E         604          DC     ABLD2        65  ABL                         D816603
165     00 0267         605          DC     RTLD2        66  RTL                         D816604
166     00 0278         606          DC     RBLD2        67  RBL                         D816605
167     00 027F         614          ENDC                                                    D816613
                        615          IFP    SPFP                                             D816614
168                     616          DC     FRRD1        68  LE                          D816615
168     00 02C6         617          DC     CERD1        69  CE                          D816616
169     00 028E         618          DC     FRRD1        6A  AE                          D816617
16A     00 02C6         619          DC     FRRD1        6B  SE                          D816618
16B     00 02C6         620          DC     FRRD1        6C  ME                          D816619
16C     00 02C6         621          DC     FRRD1        6D  DE                          D816620
16D     00 02C6         622          ENDC                                                    D816621
                        623          DC     0            6E                              D816622
16E     00 0000         624          DC     0            6F                              D816623
16F     00 0000         625  *                                                           D816624
                        626  *                                                           D816625
                        629          ENDC                                                    D816628
                        630          IFP    DPFP                                             D816629
170                     631          DC     STD          70  STD                         D816630
170     00 00E3         632          ENDC                                                    D816631
                        636          ENDC                                                    D816635
                        637          IFP    SPFP                                             D816636
171                     638          DC     STME         71  STME                        D816637
171     00 009E         639          DC     LME          72  LME                         D816638
172     00 0091         640          ENDC                                                    D816639
                        641          DC     0                                            D816640
173     00 0000         642          DC     0                                            D816641
174     00 0000         643          DC     0                                            D816642
175     00 0000         644          DC     0                                            D816643
176     00 0000         645          DC     0                                            D816644
177     00 0000         655          ENDC                                                    D816654
                        656          IFP    DPFP                                             D816655
178                     657          DC     FDRXD2       78  LD                          D816656
178     00 02C0         658          DC     CDD2         79  CD                          D816657
179     00 0288         659          DC     FDRXD2       7A  AD                          D816658
17A     00 02C0         660          DC     FDRXD2       7B  SD                          D816659
17B     00 02C0         661          DC     FDRXD2       7C  MD                          D816660
17C     00 02C0         662          DC     FDRXD2       7D  DD                          D816661
17D     00 02C0         663          DC     STMD         7E  STMD                        D816662
17E     00 009A         664          DC     LMD          7F  LMD                         D816663
17F     00 008B         665          ENDC                                                    D816664
```

MODEL 8/16 DROM2 DATA

```
                                667     *                                                                   D816666
                                668     * OP-CODES  80 - 8F  ARE ILLEGAL                                   D816667
                                669     *                                                                   D816668
180     00 0000                 670             DC      0                                                   D816669
181     00 0000                 671             DC      0                                                   D816670
182     00 0000                 672             DC      0                                                   D816671
183     00 0000                 673             DC      0                                                   D816672
184     00 0000                 674             DC      0                                                   D816673
185     00 0000                 675             DC      0                                                   D816674
186     00 0000                 676             DC      0                                                   D816675
187     00 0000                 677             DC      0                                                   D816676
188     00 0000                 678             DC      0                                                   D816677
189     00 0000                 679             DC      0                                                   D816678
18A     00 0000                 680             DC      0                                                   D816679
18B     00 0000                 681             DC      0                                                   D816680
18C     00 0000                 682             DC      0                                                   D816681
18D     00 0000                 683             DC      0                                                   D816682
18E     ** ****                 684             DC      *                                                   D816683
18F     00 0000                 685             DC      0                                                   D816684
                                686     *                                                                   D816685
                                687     *                                                                   D816686
190     00 0064                 688             DC      SRHLD2          90      SRLS                        D816687
191     00 0051                 689             DC      SLHLD2          91      SLLS                        D816688
192     00 00A1                 690             DC      NOB             92      STBR                        D816689
193     00 0000                 691             DC      0               93      LBR                         D816690
194     00 00A1                 692             DC      NOB             94      EXBR                        D816691
195     00 0000                 693             DC      0               95      EPSR                        D816692
196     00 02ED                 694             DC      WBR             96      WBR                         D816693
197     00 02F0                 695             DC      RBR             97      RBR                         D816694
198     00 0025                 696             DC      WHR             98      WHR                         D816695
199     00 0021                 697             DC      RHR             99      RHR                         D816696
19A     00 0027                 698             DC      WDR             9A      WDR                         D816697
19B     00 0023                 699             DC      RDR             9B      RDR                         D816698
                                702             ENDC                                                        D816701
19C                             703             IFP     MPY.DIV                                             D816702
19C     00 0000                 704             DC      0               9C      MHUR                        D816703
                                705             ENDC                                                        D816704
19D     00 002C                 706             DC      SSR             9D      SSR                         D816705
19E     00 002F                 707             DC      QCR             9E      QCR                         D816706
19F     00 002C                 708             DC      SSR             9F      AIR                         D816707
```

MODEL 8/16 DROM2 DATA

```
                                  710    *                                                    D816709
                                  711    * OP-CODES  A0 - AF  ARE ILLEGAL                    D816710
                                  712    *                                                    D816711
1A0     00 0000                   713           DC    0                                      D816712
1A1     00 0000                   714           DC    0                                      D816713
1A2     00 0000                   715           DC    0                                      D816714
1A3     00 0000                   716           DC    0                                      D816715
1A4     00 0000                   717           DC    0                                      D816716
1A5     00 0000                   718           DC    0                                      D816717
1A6     00 0000                   719           DC    0                                      D816718
1A7     00 0000                   720           DC    0                                      D816719
1A8     00 0000                   721           DC    0                                      D816720
1A9     00 0000                   722           DC    0                                      D816721
1AA     00 0000                   723           DC    0                                      D816722
1AB     00 0000                   724           DC    0                                      D816723
1AC     00 0000                   725           DC    0                                      D816724
1AD     00 0000                   726           DC    0                                      D816725
1AE     00 0000                   727           DC    0                                      D816726
1AF     00 0000                   728           DC    0                                      D816727
                                  729    *                                                    D816728
                                  730    * OP-CODES  B0 - BF  ARE ILLEGAL                    D816729
                                  731    *                                                    D816730
1B0     00 0000                   732           DC    0                                      D816731
1B1     00 0000                   733           DC    0                                      D816732
1B2     00 0000                   734           DC    0                                      D816733
1B3     00 0000                   735           DC    0                                      D816734
1B4     00 0000                   736           DC    0                                      D816735
1B5     00 0000                   737           DC    0                                      D816736
1B6     00 0000                   738           DC    0                                      D816737
1B7     00 0000                   739           DC    0                                      D816738
1B8     00 0000                   740           DC    0                                      D816739
1B9     00 0000                   741           DC    0                                      D816740
1BA     00 0000                   742           DC    0                                      D816741
1BB     00 0000                   743           DC    0                                      D816742
1BC     00 0000                   744           DC    0                                      D816743
1BD     00 0000                   745           DC    0                                      D816744
1BE     00 0000                   746           DC    0                                      D816745
1BF     00 0000                   747           DC    0                                      D816746
```

MODEL 8/16 DROM2 DATA

```
1C0     00 00AF     749          DC    BXH          C0  BXH     D816748
1C1     00 00B1     750          DC    BXLE         C1  BXLE    D816749
1C2     00 00CE     751          DC    LPSW         C2  LPSW    D816750
1C3     00 008A     752          DC    THI          C3  THI     D816751
1C4     00 0092     753          DC    NHR          C4  NHI     D816752
1C5     00 0099     754          DC    CLHR         C5  CLHI    D816753
1C6     00 0093     755          DC    OHR          C6  OHI     D816754
1C7     00 0094     756          DC    XHR          C7  XHI     D816755
1C8     00 0095     757          DC    LHR          C8  LHI     D816756
1C9     00 0097     758          DC    CHR          C9  CHI     D816757
1CA     00 008E     759          DC    AHR          CA  AHI     D816758
1CB     00 0090     760          DC    SHR          CB  SHI     D816759
1CC     00 0064     761          DC    SRHLD2       CC  SRHL    D816760
1CD     00 0051     762          DC    SLHLD2       CD  SLHL    D816761
1CE     00 0061     763          DC    SRHAD2       CE  SRHA    D816762
1CF     00 005D     764          DC    SLHAD2       CF  SLHA    D816763
                    765  *                                      D816764
                    766  *                                      D816765
1D0     00 00CA     767          DC    STM          D0  STM     D816766
1D1     00 00C6     768          DC    LM           D1  LM      D816767
1D2     00 00BD     769          DC    STB          D2  STB     D816768
1D3     00 00B5     770          DC    LB           D3  LB      D816769
1D4     00 00B9     771          DC    CLB          D4  CLB     D816770
1D5     00 02F0     772          DC    RBR          D5  AL      D816771
1D6     00 02ED     773          DC    WBR          D6  WB      D816772
1D7     00 02F0     774          DC    RBR          D7  RB      D816773
1D8     00 0025     775          DC    WHR          D8  WH      D816774
1D9     00 001B     776          DC    RH           D9  RH      D816775
1DA     00 00E4     777          DC    WD           DA  WD      D816776
1DB     00 0018     778          DC    RD           DB  RD      D816777
                    781          ENDC                          D816780
1DC                 782          IFP   MPY,DIV                D816781
1DC     00 00DD     783          DC    MHUR         DC  MHU     D816782
                    784          ENDC                          D816783
1DD     00 0029     785          DC    SS           DD  SS      D816784
1DE     00 002E     786          DC    OC           DE  OC      D816785
1DF     00 0029     787          DC    SS           DF  AI      D816786
```

MODEL 8/16 DROM2 DATA

```
1E0  00 0000   789          DC   0          E0                D816788
1E1  00 00ED   790          DC   SVCD2      E1  SVC           D816789
1E2  00 0080   791          DC   SINT       E2  SINT          D816790
1E3  00 0000   792          DC   0          E3                D816791
1E4  00 0000   793          DC   0          E4                D816792
1E5  00 0000   794          DC   0          E5                D816793
1E6  00 0000   795          DC   0          E6                D816794
1E7  00 0000   796          DC   0          E7                D816795
1E8  00 0000   797          DC   0          E8                D816796
1E9  00 0000   798          DC   0          E9                D816797
1EA  00 006B   799          DC   RRLD2      EA  RRL           D816798
1EB  00 005A   800          DC   RLLD2      EB  RLL           D816799
1EC  00 0068   801          DC   SRLD2      EC  SRL           D816800
1ED  00 0054   802          DC   SLLD2      ED  SLL           D816801
1EE  00 006E   803          DC   SRAD2      EE  SRA           D816802
1EF  00 0074   804          DC   SLAD2      EF  SLA           D816803
               805  *                                         D816804
               806  * OP-CODES  F0 - FF  ARE ILLEGAL          D816805
               807  *                                         D816806
1F0  00 0000   808          DC   0                            D816807
1F1  00 0000   809          DC   0                            D816808
1F2  00 0000   810          DC   0                            D816809
1F3  00 0000   811          DC   0                            D816810
1F4  00 0000   812          DC   0                            D816811
1F5  00 0000   813          DC   0                            D816812
1F6  00 0000   814          DC   0                            D816813
1F7  00 0000   815          DC   0                            D816814
1F8  00 0000   816          DC   0                            D816815
1F9  00 0000   817          DC   0                            D816816
1FA  00 0000   818          DC   0                            D816817
1FB  00 0000   819          DC   0                            D816818
1FC  00 0000   820          DC   0                            D816819
1FD  00 0000   821          DC   0                            D816820
1FE  00 0000   822          DC   0                            D816821
1FF  00 0000   823          DC   0                            D816822
               824  *                                         D816823
200            825          END                               D816824
```

MODEL 8/16 DROM2 DATA

NO ERRORS

ABLO2	0267
ACH	008D
ADD	0195
ADDWRT	0188
AHM	0088
AHR	008E
AI	0004
AIR	00D7
AL	0008
AL1	030E
ALO1	0300
ALO2	0306
ALOC	0026
ALX	0310
APSW	0024
ATL1	0253
ATL2	0262
ATLABL	007E
ATLABLD1	0251
ATLO2	025E
BALR	009F
BFCR	00A4
BFS	00A8
BKWORD	00AC
BLKIO1	02E5
BLKIO2	02E6
BLKIO3	02E9
BLKRR1	02E1
BRANCH	00A0
BTCR	00A2
BTS	00A6
BX	0012
BX1	00B2
BXH	00AF
BXLE	00B1
BXNOB	00B4
BXNX	0014
CDD2	02B8
CER	00E1
CERO1	02BE
CHR	0097
CLB	0089
CLHR	0099
CLRWT	0175
CONINT	01EB
CONSER	015F
CONTIN	017F
DHR	00DB
DHR1	0200
DIFFER	02DC
DISPLY	019D
DPFP	0001
EPSR	00D0

MODEL 8/16 DROM2 DATA

EPSR1	0330
EPSR2	033A
EPSR3	033C
EXBR	00C5
F.CC	02C8
F.VARI	0004
FDRXD2	02C0
FINISH	00FB
FL.OV	02D4
FLR	00DF
FLRD1	02CD
FLRD11	02CE
FLT1	01CB
FLT2	01D2
FLT3	01DF
FLT4	01E2
FLT5	01E4
FLTDISP	01C5
FN1	01AC
FN11	01B8
FN2.FN3	01B0
FNREG	0183
FROMAL'	02F1
FRR	00E0
FRRD1	02C6
FRWORD	00AD
FRX	0079
FRXD1	02A5
FRXNX	02A7
FXR	00DE
FXR2	02CB
FXRD1	02C9
GENSWP'	0321
HELP	0197
HELP1	0198
IDLE	0134
IDLE1	0136
IDLEX	015E
ILEG	0098
ILGPSW	0030
IMM	008C
IOAIN	01E7
IORR	0008
IORX	0005
IOSVC	01EA
LB	00B5
LBR	00B6
LCS	0096
LDDOUBLE	0113
LDREG	010A
LDSINGLE	011F
LEADER	0317
LHR	0095
LIST.OV	028A

MODEL 8/16 DROM2 DATA

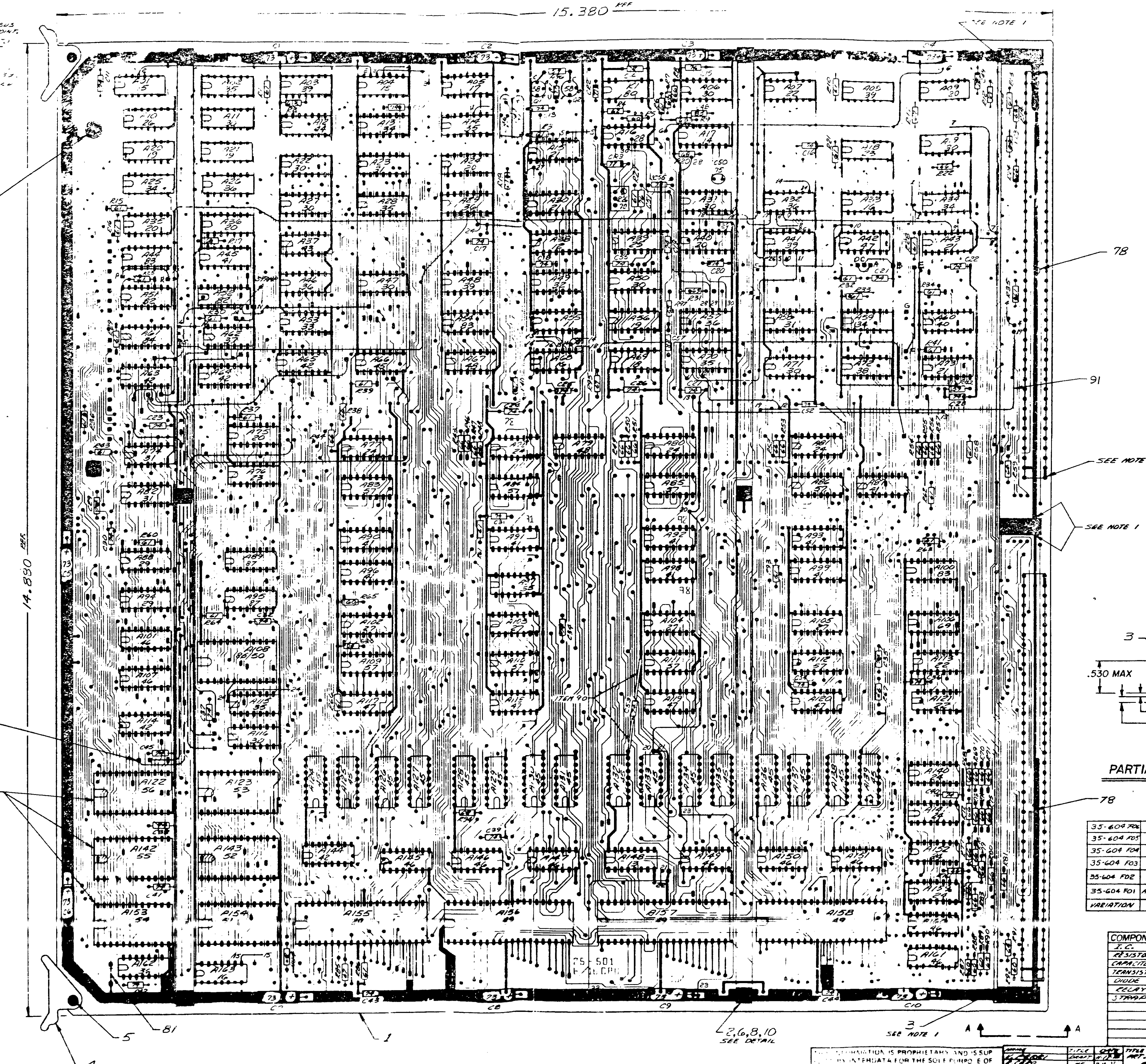
LM	00C6
LMD	008B
LMDD2	028B
LME	0091
LMED2	0291
LMEDONE	030C
LMNX	000E
LMSTM	00UC
LOCDIS	012C
LOOK20	01BB
LPSW	00CE
LPSW1	032C
LSET	032B
MAR0	012E
MHR	00DC
MHR1	0232
MHUR	00DD
MHUR1	0248
MMALF	031E
MMALF1	0320
MME	0179
MPY.DIV	0001
MRONEG	0207
MROPOS	0205
NHR	0092
NLONG	0067
NNEG1	0238
NNEG2	025C
NOB	00A1
NOWRAP1	0261
NOWRAP4	0284
OC	002E
OCR	002F
OHR	0093
OIPSW	0040
OMMPSW	0038
OUTDIS	012F
OV	0225
OV1	022A
PNTR	0022
POW	0157
PSWLOC	01B6
PWRDWN	0138
PWRDWN2	014D
PWRUP	0100
PWRUP2	0119
PWRUP3	0125
QNEG	0222
QOK	021F
QOK1	024F
QUEINT	0322
QUENBL	0332
RB1	02F3
RBLD2	027F

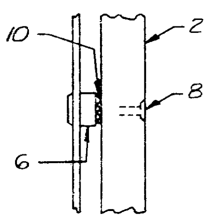
MODEL 8/16 DROM2 DATA

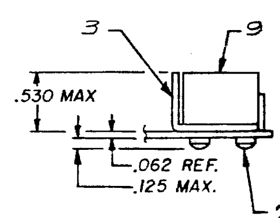
RBR	02F0
RBRWBR	00DA
RBRWBRD1	020F
RBWB	0034
RBWBNX	0038
RD	0018
RD2	0019
RDKEY	018F
RDR	0023
REGDIS	01BF
REGN	01C0
RH	001B
RHH	001E
RHR	0021
RLLD2	005A
RNNEG	021B
RRLD2	0068
RS	0002
RSNX	000A
RTL1	026F
RTL2	0285
RTLD2	0278
RTLRBL	007F
RTLRBLD1	026D
RX	0006
RXNX	0008
SAVREG	0140
SCH	008F
SHIFTO	00E6
SHORTB	00A9
SHR	0090
SINT	0080
SINT1	01ED
SINT2	01F6
SLA	004D
SLAD2	0074
SLHA	0047
SLHA1	0048
SLHAD2	005D
SLHL	003D
SLHL2	003E
SLHL3	003F
SLHLD2	0051
SLHLNX	0042
SLL	004F
SLL1D2	0056
SLLD2	0054
SLLS	00D4
SPFP	0001
SRAD2	006E
SRHAD2	0061
SRHL1	0065
SRHLD2	0064
SRL1D2	0069

MODEL 8/16 DROM2 DATA

SRLD2	0068
SS	0029
SSR	002C
START	0000
START1	0001
STB	00BD
STBR	00C0
STD	00E3
STD02	C2AF
STDOUBLE	0149
STE	00E2
STE.STD	007A
STED2	02B3
STENX	007C
STH	0084
STH2	0086
STM	00CA
STMD	009A
STMOD2	029A
STME	009E
STMED2	029E
STSINGLE	0153
SVC02	00ED
TERMIN	00FC
THI	008A
THRUD2	0046
WAIT	0159
WAIT1	015C
WASEMPTY	028A
WBR	02ED
WD	00E4
WDR	0027
WHR	0025
XHR	0094
YDNNEG	020D







PARTIAL VIEW A-A

REVISIONS

A16 WAS SPEC AS ITEM # 17. A97 WAS SPEC AS ITEM # 17. A16 WAS SPEC AS ITEM # 33. R95 WAS SPEC AS ITEM 61. C31 C33 C52 & R61 WERE NOT SPEC.

12-11-75

RELEASED FOR PRODUCTION

AREA A06, C48 ITEM NUMBER WAS 74.

2773 — 3-16-76

REVISED CIRCUITRY TO REFLECT NEW COPPER

— 3-22-76

AREA A15, R96 WAS NOT SPEC'D. REVISED CIRCUITRY TO REFLECT NEW COPPER.

2939 — 5-10-76

ADDED STRAP #1. A09 WAS ITEM #39, A12 WAS ITEM #61. REVISED CIRCUITRY TO REFLECT NEW COPPER

3032 — 1-20-77

ADDED STRAPS 2-27. A04 WAS ITEM 30, A WAS ITEM 39. ADDED WW STAKE & JUMPER BY A52. CR3 WAS A 470 Ω RES., ITEM 60. ADDED C53-C57. ADDED A97, A89 & A95 WERE ITEM 41. ADDED ITEM 86 TO A108. ADDED F03 TO F06 ON VAR. TABLE. ADDED ITEM 90 & 91. REVISED CIRCUITRY TO REFLECT NEW COPPER

3081 — 1-20-77

ADDED STRAPS 28-30. REVISED CIRCUITRY TO REFLECT NEW COPPER

3082 — 1-30-77

ADDED WW STAKES & JUMPER "PER" BY A44. R34 BY A60 WAS SPEC'D 66. R43 BY A74 WAS SPEC'D 66. ITEM 79 WAS 45 PLACES

3168 — 10-18-77

REVISED CIRCUITRY TO REFLECT NEW COPPER. ADDED STRAP 31. AREA A73

GP 3374 — 12-1-77

VARIATION	DESCRIPTION
35-604 F06	AS SHOWN
35-604 F05	AS SHOWN
35-604 F04	AS SHOWN
35-604 F03	AS SHOWN
35-604 F02	AS SHOWN LESS ITEM 86
35-604 F01	AS SHOWN LESS ITEMS 54,55 & 56

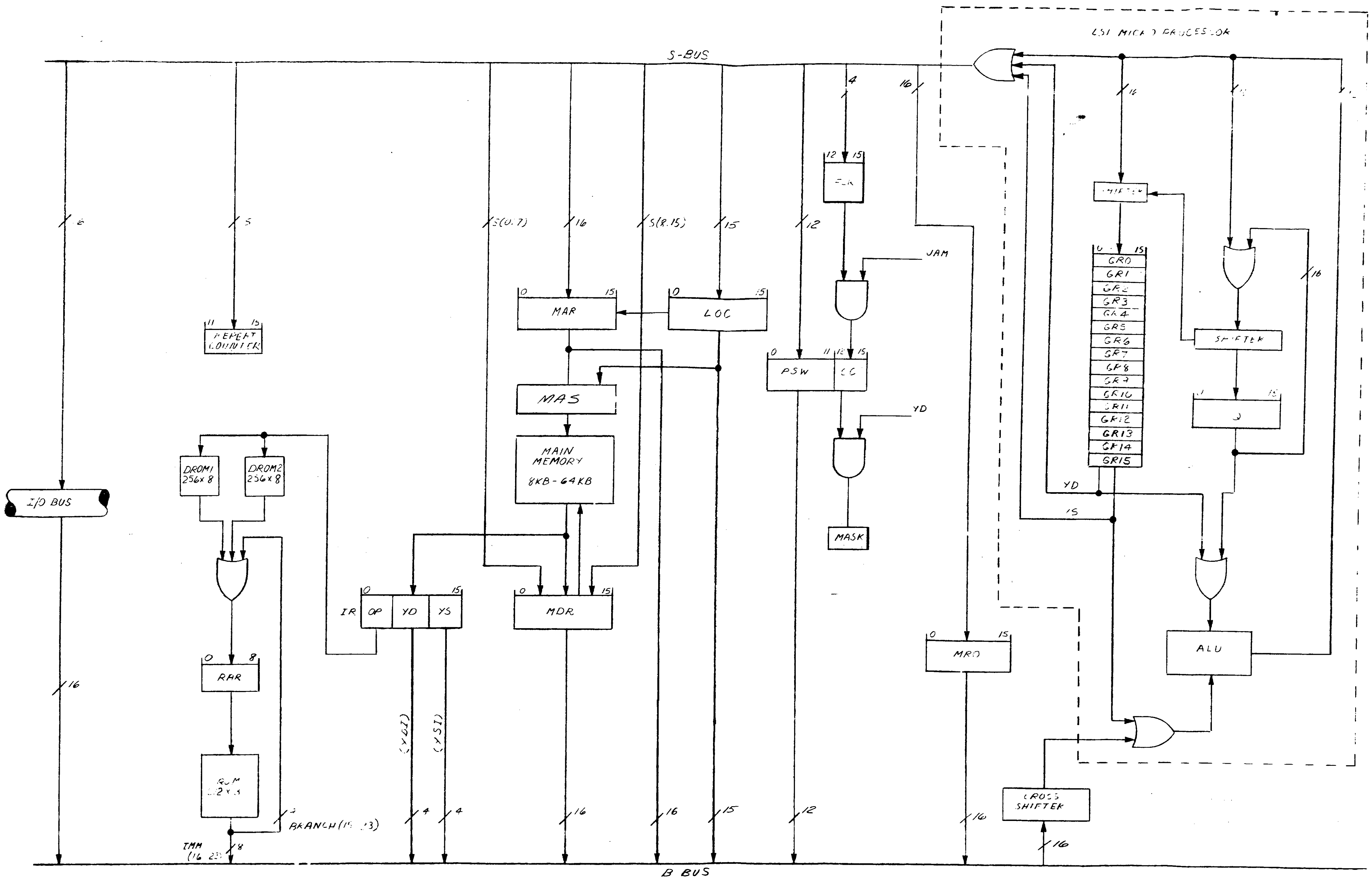
COMPONENT	REF DESIGNATION
I.C.	A01 THRU A163
RESISTOR	R1-R18, R20-R97
CAPACITOR	C1 THRU C57
TRANSISTOR	Q1 & Q2
DIODE	CR1 THRU CR3
RELAY	K1
STRAPS	1-31

TITLE: PRT. CKT ASSEMBLY 8/16 CPU

35-604 F01 — SHT 1 OF 1

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS					
PRE PRODUCTION APPROVAL	DEV	INIT	DATE		
SHTS 2,4,5,11,13 & 17 WERE SPEC AS REV LEVEL R00.					
		07145-3		12-11-75	R01
RELEASED FOR PRODUCTION ENG DATE					
REVISED SHT 1, 7, REV. LEV. OF BOTH BOARDS WERE R00 RESP.					
		2839	–	5-10-76	R02
REVISED SHTS 1 & 12. P.C. BOARDS 35-604 WERE R04.					
		2828	—	7-15-76	R03
REVISED SHTS 11, 18 & 19. PC BDS 35-604 WERE R05					
			–	12-23-76	R04
PC BDS 35-604 WERE R06					
WS		3081	–	1-10-76	R05
REVISED SHTS 1 & 18. PC BDS 35-604 F01 & F02 WERE R07. F03 - F06 WERE NOT SPEC					
WS		3082	–	1-20-77	R06
REVISED SHT 18.					
GS			–		R07
REVISED SHT 14. PC. BDS 35-604 F01 & F02 WERE R08. F03 & F04 WERE R03. F05 & F06 WERE R01.					
GS		3168		10-18-77	R08
REVISED SHT 15 P.C BOARDS F01-F02 WAS R09, F03-F04 WAS R04, F05-F06 WAS R02.					
GP		3374	–	12-2-77	R09



MODEL 6/16 BLOCK DIAGRAM

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION.	
6/16 CPU W/O M-D	35-604 F01 R10
6/16 CPU W/M-D	35-604 F02 R10
8/16 CPU BASIC	35-604 F03 R05
8/16 CPU W/M-D	35-604 F04 R05
8/16 CPU W/SPFP	35-604 F05 R03
9/16 CPU W/DPFP	35-604 F06 R03

NOTE:
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

SHEET INDEX	REV LEVEL	09	02	01	02	02	01	01				03	02	01	02	02		01	–	03
	SHEET NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

NOTE:
ALL COMPONENTS IN THIS SCHEMATIC LOCATED ON 35-604.

SCALE–	NAME	TITLE	DATE
TOLERANCE UNLESS OTHERWISE SPECIFIED	S. SCHAIBLE	DRAFT	11-4-75
	R CERO	CHK	
		ENGR	
			12-16-75
			12-16-75

TITLE FUNCTIONAL SCHEMATIC 6/16 CPU PROCESSOR

TASK NO. 03145

DWG NO. 01-094 R09 D08

SHEET 1 OF 19

INTERDATA®

BACK PANEL MAP

CONN.	TITLE	CPU		MEM I/O		MPY-DIV I/O		I/O		CONN.
	BD. LOC.	07		06		05		04		
	TERM. NO.	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	
1	41	P5	GND	P5	GND	P5	GND	P5	GND	1
	40	GND	GND	GND	GND	GND	GND	GND	GND	
	39	P15/P12	P15/P12	P15/P12	P15/P12	P15/P12	P15/P12	P15/P12	P15/P12	
	38	N15	N15	N15	N15	N15	N15	N15	N15	
	37	MDS150	MDS160	MDS150	MDS160	MDS150	MDS160	MDS150	MDS160	
	36	MDS130	MDS140	MDS130	MDS140	MDS130	MDS140	MDS130	MDS140	
	35	MDS110	MDS120	MDS110	MDS120	MDS110	MDS120	MDS110	MDS120	
	34	MDS090	MDS100	MDS090	MDS100	MDS090	MDS100	MDS090	MDS100	
	33	MDS070	MDS080	MDS070	MDS080	MDS070	MDS080	MDS070	MDS080	
	32	MDS050	MDS060	MDS050	MDS060	MDS050	MDS060	MDS050	MDS060	
	31	MDS030	MDS040	MDS030	MDS040	MDS030	MDS040	MDS030	MDS040	
	30	MDS010	MDS020	MDS010	MDS020	MDS010	MDS020	MDS010	MDS020	
	29		MDS000		MDS000		MDS000		MDS000	
	28	LDREGO	MIDO	TEMPA		LOREGO	MIDO			
	27	WTO	BCLKO	WRTO	TEMPB		BCLKO			
	26	SCLROA	HWO	SCLROA	HWO	SCLRO	HWO	SCLRO	HWO	
	25	PERRO	SLRO	PERRO						
	24	GND	GND			EXSTPO				
	23	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	
	22	EXSTPO				RACKO	TACKO	RACKO	TACKO	
	21	GDATO	DAO	CLOTO	DAO	CLOTO	DAO	CLOTO	DAO	
	20	DISOSCO	CMDO	DRO	CMDO	DRO	CMDO	DRO	CMDO	1
	19	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO	
	18	FOECIO		DI40	DI50	DI40	DI50	DI40	DI50	
	17	LIRHI		DI20	DI30	DI20	DI30	DI20	DI30	
	16			DI00	DI10	DI00	DI10	DI00	DI10	
	15			DO80	DO90	DO80	DO90	DO80	DO90	
	14			DO60	DO70	DO60	DO70	DO60	DO70	
	13			DO40	DO50	DO40	DO50	DO40	DO50	
	12			DO20	DO30	DO20	DO30	DO20	DO30	
	11			DO00	DO10	DO00	DO10	DO00	DO10	
	10	WRTOA	MDS000	WRTOA	MDS000	WRTOA	MDS000	WRTOA	MDS000	
	09	MDS010	MDS020	MDS010	MDS020	MDS010	MDS020	MDS010	MDS020	
	08	MDS030	MDS040	MDS030	MDS040	MDS030	MDS040	MDS030	MDS040	
	07	MDS050	MDS060	MDS050	MDS060	MDS050	MDS060	MDS050	MDS060	
	06	MDS070	MDS080	MDS070	MDS080	MDS070	MDS080	MDS070	MDS080	
	05	MDS090	MDS100	MDS090	MDS100	MDS090	MDS100	MDS090	MDS100	
	04	MDS110	MDS120	MDS110	MDS120	MDS110	MDS120	MDS110	MDS120	
	03	MDS130	MDS140	MDS130	MDS140	MDS130	MDS140	MDS130	MDS140	
	02	MDS150	MDS160	MDS150	MDS160	MDS150	MDS160	MDS150	MDS160	
	01	GND	GND	GND	GND	GND	GND	GND	GND	
	00	P5	GND	P5	GND	P5	GND	P5	GND	
		1	2	1	2	1	2	1	2	
	41	P5	GND	P5	GND	P5	GND	P5	GND	
	40	GND	GND	GND	GND	GND	GND	GND	GND	
	39	P15/P12	REGO	P15/P12	REGO	P15/P12	REGO	P15/P12	REGO	
	38	N15	ENO	N15	ENO	N15	ENO	N15	ENO	
	37		TACO		TACO	ACTO	TACO	ACTO	TACO	
	36	SINGLO	CATNO			INITO				
	35	EXB930	EXDUAO	EXDUAO	EXB340	CATNO	SINGLO			
	34					FWAITI				
	33	MAI30	MAI40	MAI30	MAI40	MAI30	MAI40	MAI30	MAI40	
	32	MAI10	MAI20	MAI10	MAI20	MAI10	MAI20	MAI10	MAI20	
	31	MA090	MA100	MA090	MA100	MA090	MA100	MA090	MA100	
	30	MA070	MA080	MA070	MA080	MA070	MA080	MA070	MA080	
	29	MA050	MA060	MA050	MA060	MA050	MA060	MA050	MA060	
	28									
	27	OMATNO		OMATNO		OMATNO		OMATNO		
	26		HWO	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO	
	25									
	24									
	23	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	
	22		ACKO	RACKO	TACKO	RACKO	TACKO	RACKO	TACKO	
	21		DAO	CLOTO	DAO	CLOTO	DAO	CLOTO	DAO	
0	20	DRO	CMDO	DRO	CMDO	DRO	CMDO	DRO	CMDO	0
	19	SRO	ADRS	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO	
	18	DB140	DB150	DI40	DI50	DI40	DI50	DI40	DI50	
	17	DB120	DB130	DI20	DI30	DI20	DI30	DI20	DI30	
	16	DB100	DB110	DI00	DI10	DI00	DI10	DI00	DI10	
	15	DB080	DB090	DO80	DO90	DO80	DO90	DO80	DO90	
	14	DB060	DB070	DO60	DO70	DO60	DO70	DO60	DO70	
	13	DB040	DB050	DO40	DO50	DO40	DO50	DO40	DO50	
	12	DB020	DB030	DO20	DO30	DO20	DO30	DO20	DO30	
	11	DB000	DB010	DO00	DO10	DO00	DO10	DO00	DO10	
	10	MA030	MA040	MA030	MI040	MA030	MA040	MA030	MA040	
	09	MA020		MA020	MA021	MA020	MA021	MA020	MA021	
	08									
	07	MA010		MA010		MA010		MA010		
	06	MA000		MA000		MA000		MA000		
	05									
	04	INNO	ERO	INNO	ERO	INNO	ERO	INNO	ERO	
	03									
	02	P15/P12	REDTO	P15/P12	NI5	P15/P12	NI5	P15/P12	NI5	
	01	GND	GND	GND	GND	GND	GND	GND	GND	
	00	P5	GND	P5	GND	P5	GND	P5	GND	
		1	2	1	2	1	2	1	2	

CONN.	TITLE	I/O		I/O		I/O		I/O		TITLE	CONN.
	BD. LOC.	03		02		01		00		BD. LOC.	
	TERM. NO.	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	TERM. NO.	
	41							P5	GND	41	
	40							GND	GND	40	
	39							P15/P12	P15/P12	39	
	38							N15	ENO	38	
	37							ACTO	TACO	37	
	36									36	
	35									35	
	34							XRACKO		34	
	33							MAI30	MAI40	33	
	32							MAI10	MAI20	32	
	31							MA090	MA100	31	
	30							MA070	MA080	30	
	29							MA050	MA060	29	
	28									28	
	27							OMATNO		27	
	26							SCLRO	HWO	26	
	25									25	
	24									24	
	23							SYNO	ATNO	23	
	22							RACKO	TACKO	22	
	21							CLOTO	DAO	21	
0	20							DRO	CMDO	20	0
	19							SRO	ADRSO	19	
	18							DI40	DI50	18	
	17							DI20	DI30	17	
	16							DI00	DI10	16	
	15							DO80	DO90	15	
	14							DO60	DO70	14	
	13							DO40	DO50	13	
	12							DO20	DO30	12	
	11							DO00	DO10	11	
	10							MA030	MA040	10	
	09							MA020	MA021	09	
	08									08	
	07							MA010		07	
	06							MA000		06	
	05									05	
	04							INHO	ERO	04	
	03									03	
	02							P15/P12	NI5	02	
	01							GND	GND	01	
	00							P5	GND	00	
		1	2	1	2	1	2	1	2		

NOTES

UPD	03145-3	MB	12-15-75	R01
ADDED FOECIO TO 118-1				
ADDED LIRHI TO 117-1				
WS	3041	-	1-11-77	R02

REVISIONS

SLOT 05 122-1 WAS EXSTPO
124-1 WAS NOT SPECIFIED
SLOT 06 122-1 WAS RACKO.
222-1 WAS TACKO, SLOT 07
222-1 WAS TACKO

NAME	TITLE	DATE
V. PERRI	DRAFT	11-12-75
E. CERO	CHK	
— CENTAIR	ENGR	
R.A. BARKER	D.E.	
D. FRANKENBERGER	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
6/16 CPU
PROCESSOR

TASK NO. 03145 SHEET OF 2-19
DWG NO. 01-094 R02000

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS				
AREA M7: SPFP WAS SPEC'D AS DATN, DPFP WAS NOT SPEC'D				
WS	JV	3081	1-10-77	

	ALU							IMMEDIATE		
	0 1 2	DEST 3 4 5	OP 6 7 8	SOURCE 9 10 11	D 12 13 14	15	16	S 17 18 19	E FIELD 20 21 22 23	
NOP	0 0 0								0 0 0 0	NULL
O2	0 0 1								0 0 0 1	ADR/ACK } I/O · $\overline{BR}$ · $\overline{IMM}$
MR	0 1 0								0 0 1 0	CMD/STAT } I/O · $\overline{BR}$ · $\overline{IMM}$
MW	0 1 1								0 1 0 0	DA/DR } I/O · $\overline{BR}$ · $\overline{IMM}$
BT	1 0 0									
BF	1 0 1								0 0 0 1	CLR YD & SET WAIT } $\overline{I/O}$ · $\overline{BR}$ · $\overline{IMM}$
JAM CC + IR	1 1 0								0 0 1 0	YDP1 } $\overline{I/O}$ · $\overline{BR}$ · $\overline{IMM}$
D1	1 1 1								0 0 1 1	YDM1 } $\overline{I/O}$ · $\overline{BR}$ · $\overline{IMM}$
LOAD Q ALU OUTPUT		0 0 0								
NULL ALU OUTPUT		0 0 1							0 1 0 0	POW } $\overline{I/O}$ · $\overline{BR}$ · $\overline{IMM}$
LOAD YD & Q, A OUTPUT		0 1 0							0 1 0 1	JAM CI & CO (FOR INC, DEC ONLY) } $\overline{I/O}$ · $\overline{BR}$ · $\overline{IMM}$
LOAD YD, ALU OUTPUT		0 1 1			0 0 0				0 1 1 0	M/D } $\overline{I/O}$ · $\overline{BR}$ · $\overline{IMM}$
LOAD YD & Q, SR		1 0 0							0 1 1 1	FLT PT } $\overline{I/O}$ · $\overline{BR}$ · $\overline{IMM}$
LOAD YD, SR		1 0 1								
LOAD YD & Q, SL		1 1 0							1 0 0 1	CI } $\overline{I/O}$ · $\overline{BR}$ · $\overline{IMM}$
LOAD YD, SL		1 1 1							1 0 1 0	CO } $\overline{I/O}$ · $\overline{BR}$ · $\overline{IMM}$
LOAD YS		0 1 1			0 0 1				1 1 0 0	F } $\overline{I/O}$ · $\overline{BR}$ · $\overline{IMM}$

The arrow from LOAD YD, ALU OUTPUT runs down to LOAD YS.

ALU OP	6 7 8	S 17 18 19	E FIELD 20 21 22 23	
R + S	0 0 0	1 1 1	1 0 0 0	UNLOAD BOX ON I/O BUS
S − R	0 0 1			
R − S	0 1 0			
R OR S	0 1 1			
R AND S	1 0 0			
$\overline{R}$ AND S (UNUSED)	1 0 1			
R XOR S	1 1 0			
R XNOR S	1 1 1			

MD: DIFFERENTIATED BY # OF OPERANDS
FLTPT: DIFFERENTIATED BY IR00:07

	R	S	SOURCE 9 10 11
	YS	Q	0 0 0
	YS	YD	0 0 1
	Ø	Q	0 1 0
	Ø	YD	0 1 1
	Ø	YS	1 0 0
EXTERNAL SOURCE	D	YD	1 0 1
EXTERNAL SOURCE	D	Q	1 1 0
EXTERNAL SOURCE	D	Ø	1 1 1

DEST 3 4 5	D	12 13 14	S 17 18 19	S	
0 0 1	PSW	0 0 0	0 0 0	PSW	EXT SOURCE · $\overline{BR}$ · $\overline{IMM}$
	LOC	0 0 1	0 0 1	LOC	
	MRØ	0 1 0	0 1 0	MRØ	
0 0 0 OR 0 0 1	CNTR	0 1 1	0 1 1	YSI	
	MDR	1 0 0	1 0 0	MDR	
	MAR	1 0 1	1 0 1	MAR	
	FLR	1 1 0	1 1 0	YDI	
	IO	1 1 1	1 1 1	IO	

Bits 14 15	
NULL	0 0
IMM	1 X
CS	0 1

BRANCH

	CONDITION 8 … 13		14	ADDRESS 15 … 23
C	0 0	0 1 1 1	X	
V		1 0 1 1		
G		1 1 0 1		
L		1 1 1 0		
MSK	0 1	0 1 1 1		
ARST		1 0 1 1		
SPFP		1 1 0 1		
DPFP		1 1 1 0		
ATN	1 0	0 1 1 1		
CATN		1 0 1 1		
SNGL		1 1 0 1		
MALF		1 1 1 0		
AMOD	1 1	0 1 1 1		
LSU/HW		1 0 1 1		
PPF		1 1 0 1		
MPE		1 1 1 0		
UNCOND	0 0	1 1 1 1		

Arrows under 00, 01, 10 and 11 run down each group.

LSU: ADDRESSED ON POWER UP
KNOCKED DOWN WHEN OTHER
DEV. ADDRESSED.

SCALE–	NAME	TITLE	DATE	TITLE
		DRAFT		
		CHK		
		ENGR		

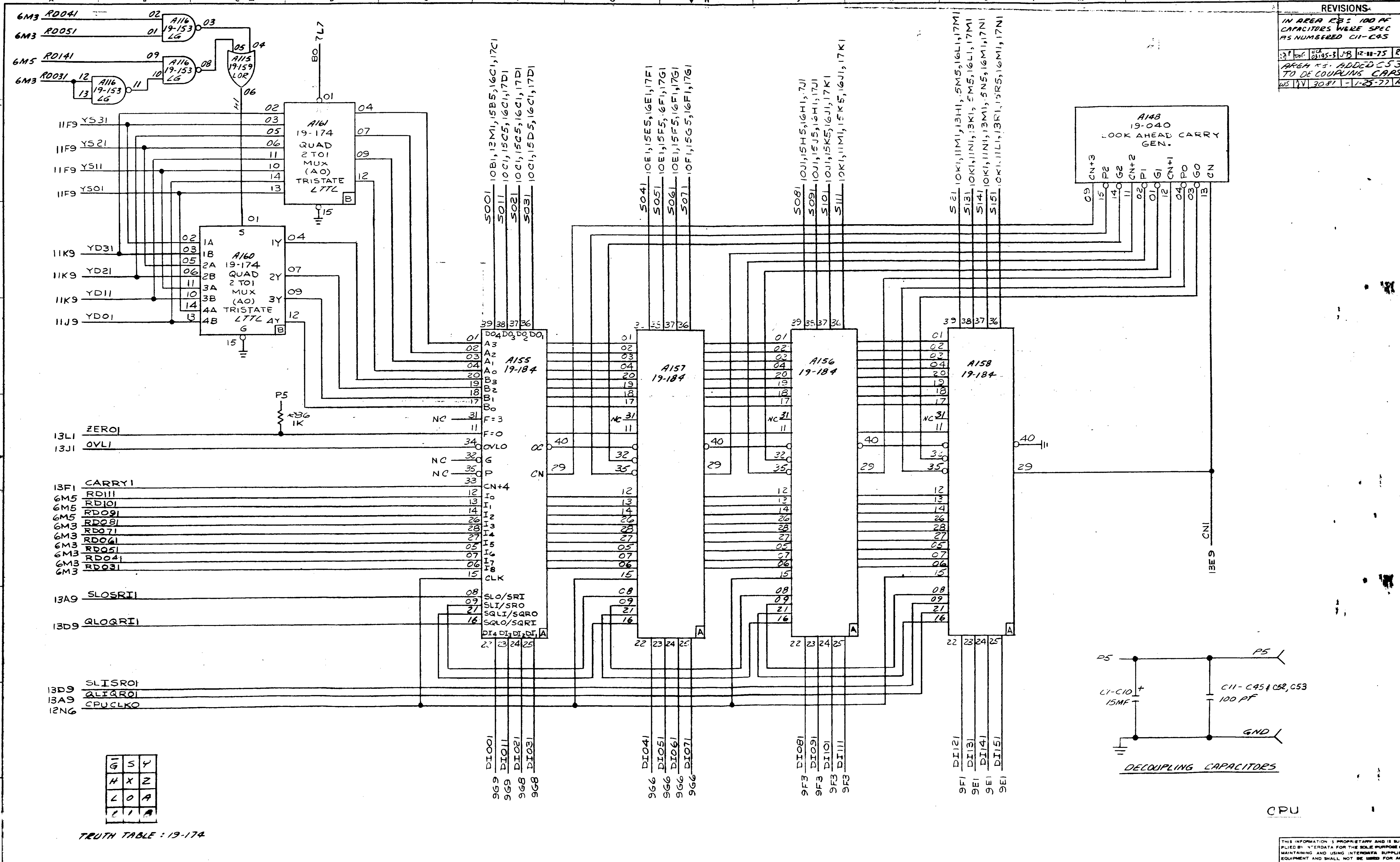
TASK NO 03145
DWG NO 01-094R01D08 SHEET 3 OF 19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

IN AREA R3: 100 PF CAPACITORS WERE SPEC AS NUMBERED C11-C45

AREA R3: ADDED C53 TO DECOUPLING CAPS.



CPU

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

SCALE	NAME	TITLE	DATE	TITLE
		DRAFT		
		CHK		
		ENGR		

03145

01-094R2D08

4-19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

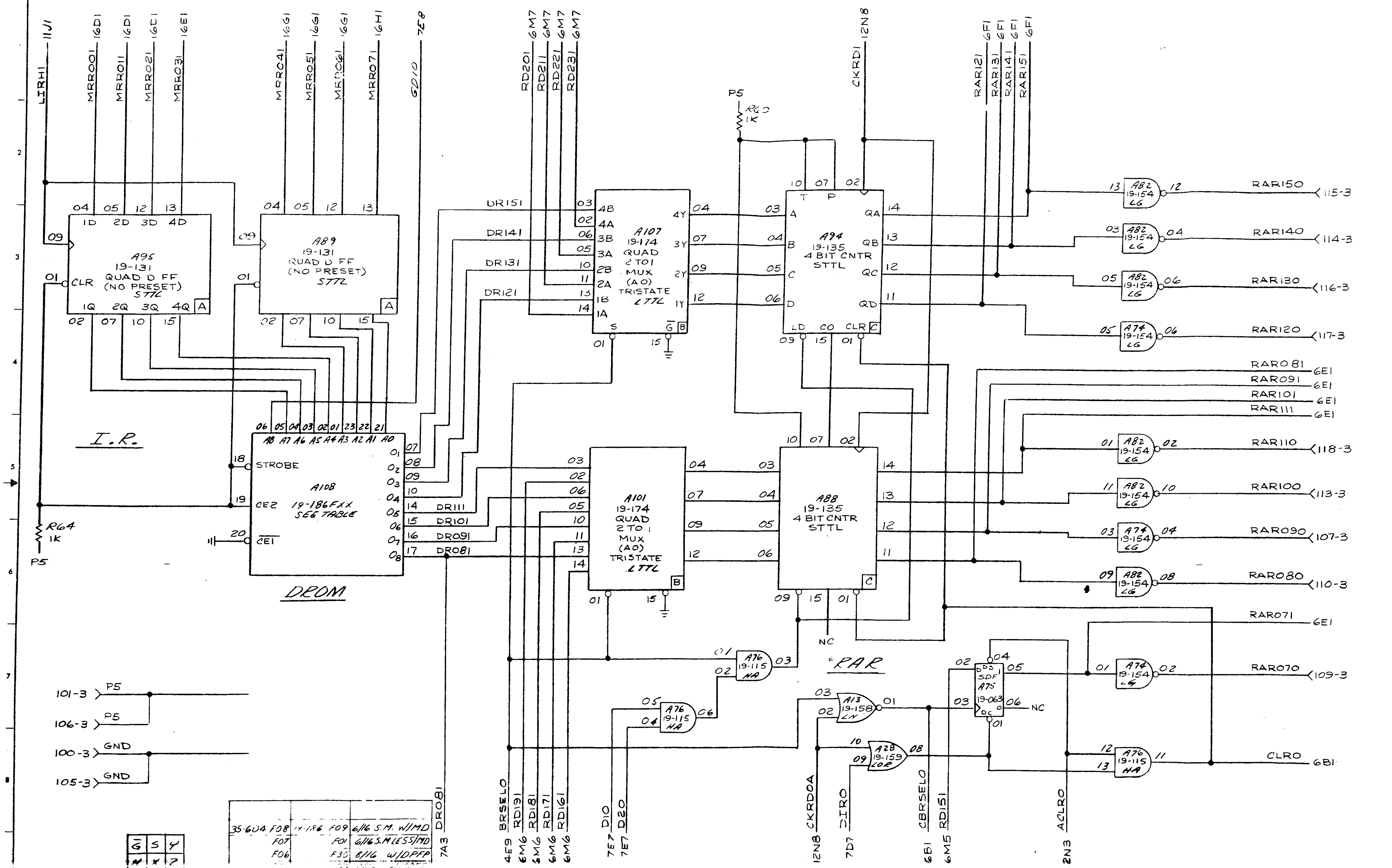
REVISIONS

ON A108 AREA C5; PIN 21 WAS SPEC AS MNEMONIC D10 AND REFERENCED TO F9 & 7F7. PIN 22 WAS CONNECTED TO A89-15. PIN 23 WAS CONNECTED TO A89-10. PIN 1 WAS CONNECTED TO A89-07. PIN 2 WAS CONNECTED TO A89-02. PIN 3 WAS CONNECTED TO A95-15. PIN 4 WAS CONNECTED TO A95-10. PIN 5 WAS CONNECTED TO A95-07 PIN 6 WAS CONNECTED

03'	LAF	ECR 03145-3	MB	12-11-75	R01

AREA C9: VARIATION TABLE WAS NOT SPEC'D. AREA A3 & C3: A95 & A89 WERE SPEC'D AS 19-167'S. AREA D1: A108-06 WAS TO MNE. D10, CROSS-REF. TO 7E7, & F9. AREA F9: MNE. D10 WAS CROSS-REF TO D1.

W	AV	3081	-	1-6-77	R02



G	S	Y
H	X	Z
L	0	A
L	1	B

TRUTH TABLE : 19-174

35-604 F08	19-186 F09	6/116 S.M. W/MD
F07	F01	6/116 S.M LESS/MD
F06	F30	8/116 W/DPFP
F05	F29	8/116 W/DPFP
F04	F28	8/116 W/M-D
F03	F27	6/116 BASIC
F02	F09	6/116 W/MD
35-604 F01	19-186 F01	6/116 LESS/M-D

VARIATION TABLE

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

SCALE —	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

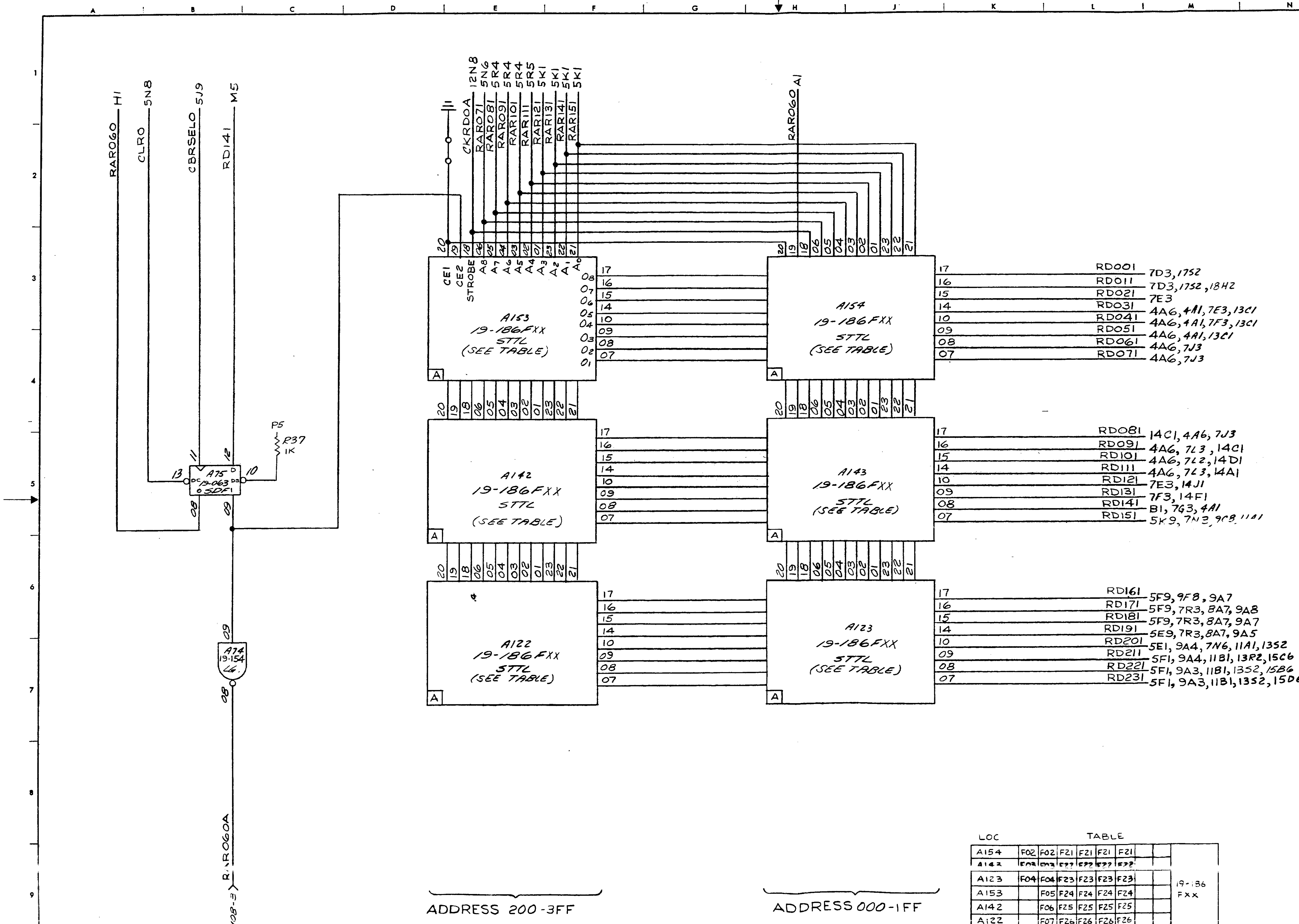
TITLE

03145
01-094 R02 D48 5-19

REVISIONS

AREA M3: ADDED SHT LOC 18H2 TO MNEMONIC RD011. AREA L9: ADDED TABLE

W.A. 121	3081	1-6-77	R01



TABLE

LOC									
A154	F02	F02	F21	F21	F21	F21			
A143	F03	F03	F22	F22	F22	F22			
A123	F04	F04	F23	F23	F23	F23			19-186 FXX
A153		F05	F24	F24	F24	F24			
A142		F06	F25	F25	F25	F25			
A122		F07	F26	F26	F26	F26			
35-604	F01	F02	F03	F04	F05	F06			

ROM

SCALE– NAME TITLE DATE TITLE
DRAFT CHK ENGR

03145
01-094 R01 D08 6–19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

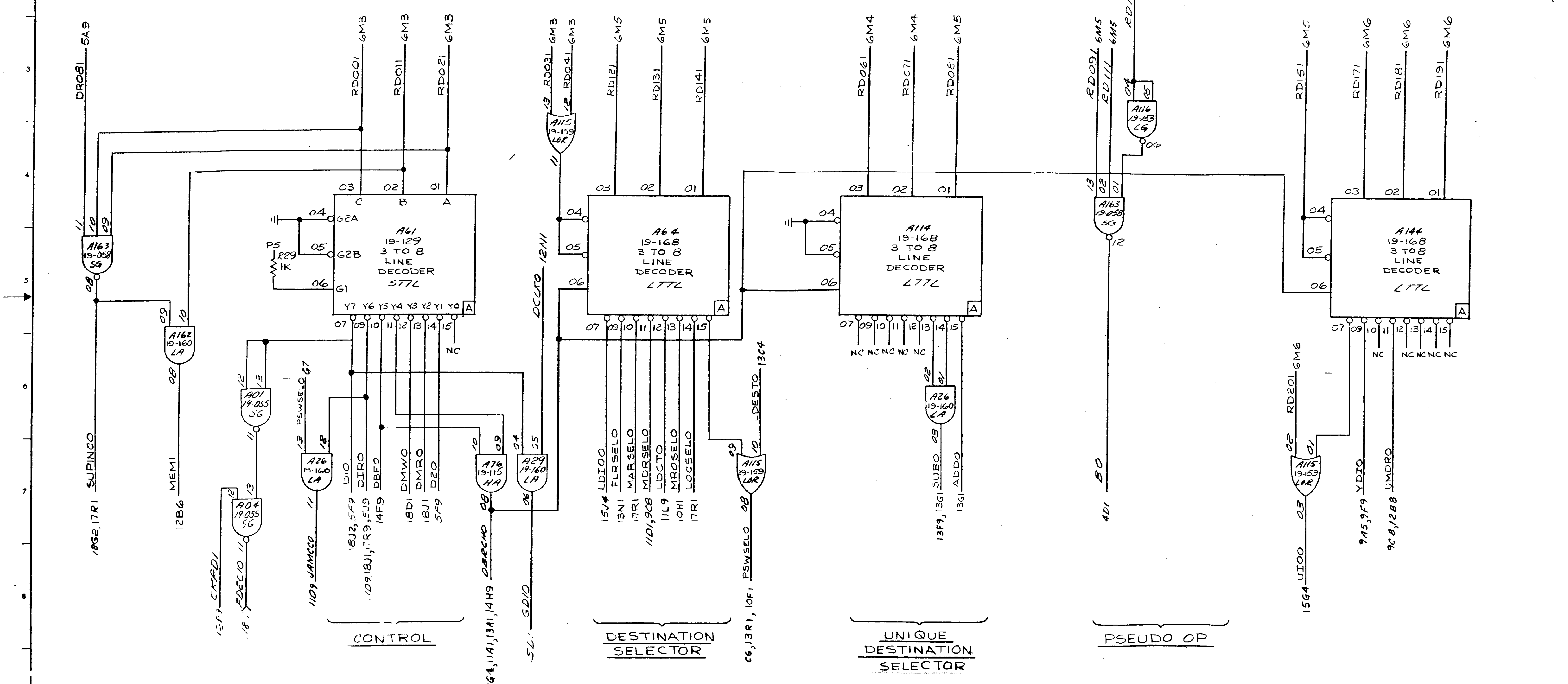
C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0	L	H	H	H	H	H	H	H
0	0	1	H	L						
0	1	0	H	H	L					
0	1	1	H	H		L				
1	0	0	H	H			L			
1	0	1	H	H				L		
1	1	0	H	H					L	
1	1	1	H	H						L

TRUTH TABLE : 19-129 & 19-168

REVISIONS

AREA A5: A163 WAS SPEC'D AS A 19-155. AREA C7, A01, A04 & RELATED CIRCUITRY WAS NOT SPEC'D. AREA E7: A29 & RELATED CIRCUITRY WAS NOT SPEC'D. AREA A7: ADDED CROSS-REF 18G2 TO MNE SUPINCO. AREA B7 DELETED CROSS-REF 5F? FROM MNE MEMI.

WS	JU	3081	-	1-7-77	R01



RD DECODING

SCALE–

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE

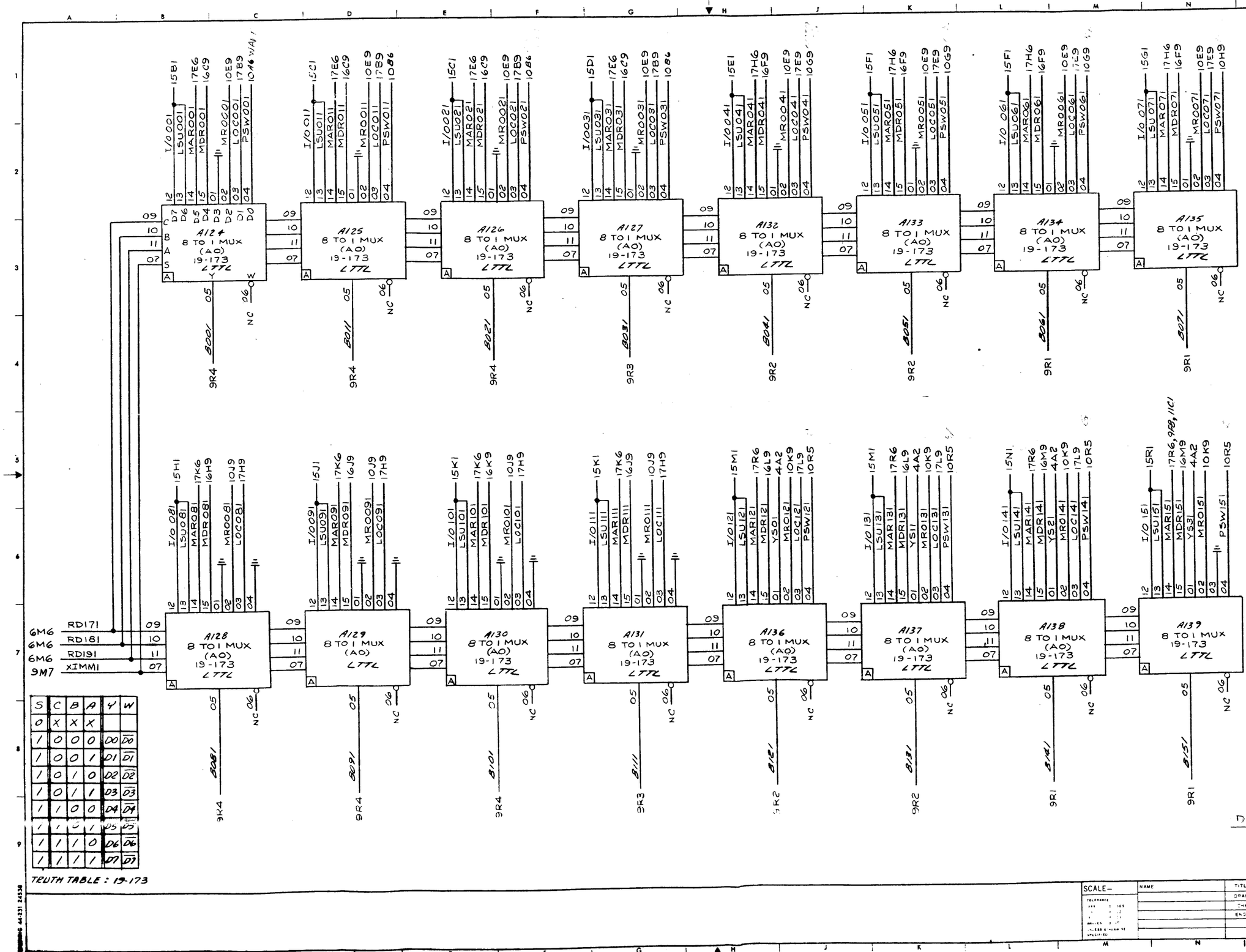
03145

01-094R01D08

SHEET 7-19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



S	C	B	A	Y	W
0	X	X	X		
1	0	0	0	D0	$\overline{D0}$
1	0	0	1	D1	$\overline{D1}$
1	0	1	0	D2	$\overline{D2}$
1	0	1	1	D3	$\overline{D3}$
1	1	0	0	D4	$\overline{D4}$
1	1	0	1	D5	$\overline{D5}$
1	1	1	0	D6	$\overline{D6}$
1	1	1	1	D7	$\overline{D7}$

TRUTH TABLE : 19-173

DATA MUX

SCALE—

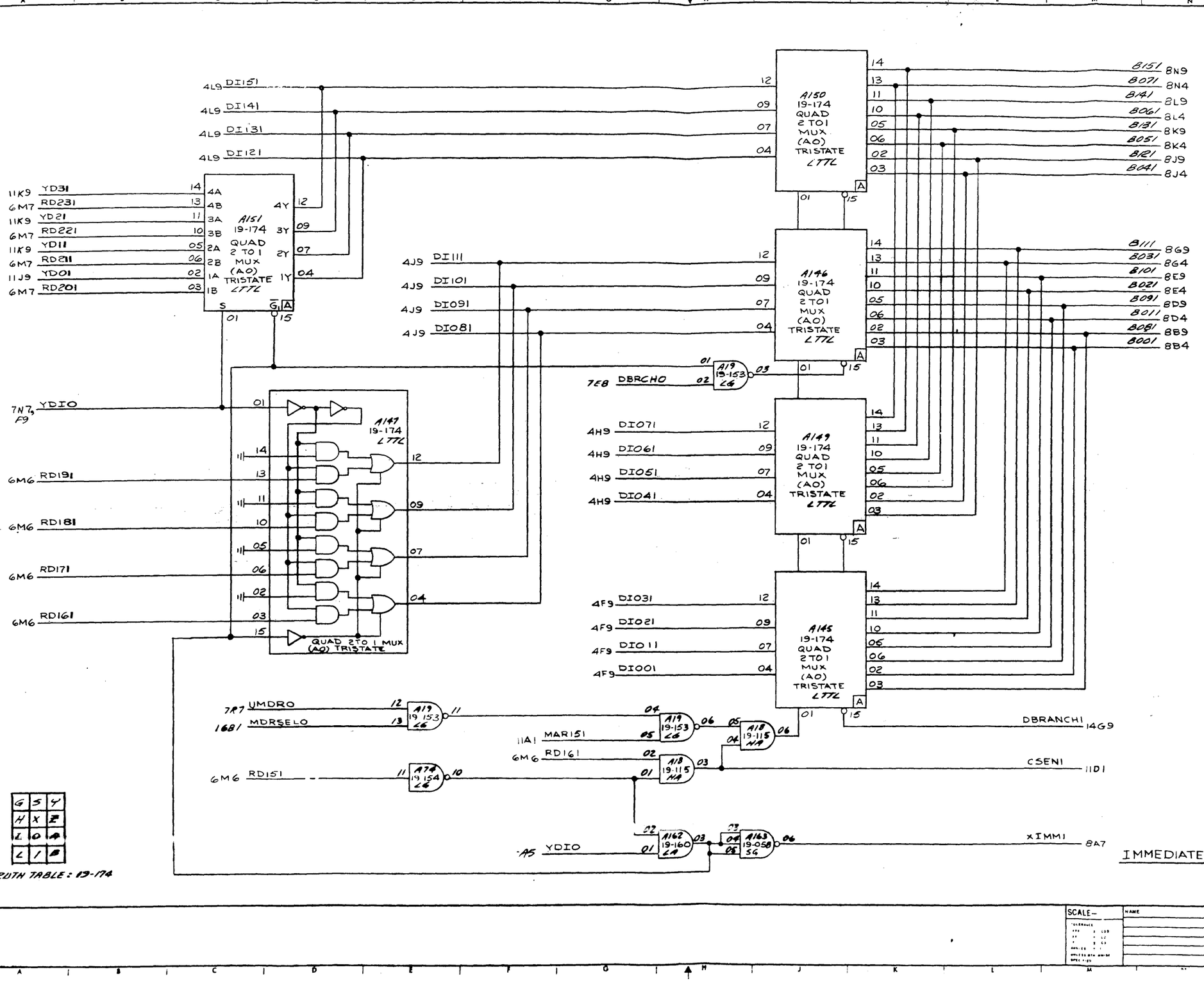
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE

DRAWING NO. 03145
SPEC NO. 01-094 D08
SHEET OF 8-19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



G	5	4
H	X	E
L	0	A
L	1	B

TRUTH TABLE: 19-174

IMMEDIATE & CROSS SHIFT

SCALE—

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE

DWG NO 09A03 SHEET 9 OF 19

ENG NO 01-094 008

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

A96 19-167 QUAD D FF (NO PRESET) TTL — CLR, 1D 2D 3D 4D, 1Q 2Q 3Q 4Q

A90 19-167 QUAD D FF (NO PRESET) LTTL

A92 19-167 QUAD D FF (NO PRESET) LTTL

A98 19-167 QUAD D FF (NO PRESET) LTTL

A91 19-167 QUAD D FF (NO PRESET) LTTL

A93 19-167 QUAD D FF (NO PRESET) LTTL

A97 19-159 LOR

A97 19-159 LOR

A58 19-154 LG

A100 19-179 LTTL

A99 19-167 QUAD D FF (NO PRESET) LTTL

R61 1K P5

R93 1K P5

5001 4F1, 5011 4F1, 5021 4F1, 5031 4F1

5041 4G1, 5051 4G1, 5061 4H1, 5071 4H1

PSWSELO 7G7

CKRDOB 12N8, MROSELO 7G7

5081 4J1, 5091 4J1, 5101 4J1, 5111 4J1

5121 4L1, 5131 4L1, 5141 4L1, 5151 4L1

YD31 11K9, YD21 11K9, YD11 11K9, YD01 11J9, MSK1 14D1

PSW121 8J5, PSW131 8K5, PSW141 8M5, PSW15 8N5

PSW001 8C1, PSW011 8D1, PSW021 19L1,8F1, PSW031 8G1, PSW010 14L1

MR0001 8C1, MR0011 8D1, MR0021 8F1, MR0031 8G1

MR0041 8J1, MR0051 8K1, MR0061 8M1, MR0071 8N1

PSW041 8J1, PSW051 8K1, PSW061 8M1, PSW071 8N1

MR0081 8C5, MR0091 8D5, MR0101 8F5, MR0111 8G5

MR0121 8J5, MR0131 8K5, MR0141 8M5, MR0151 8N5

LDCCO 11F9

FLR121 14D1,13G9, FLR131 14C1,13J9, FLR141 14J1,13L9, FLR151 14G1,13N9

PSW & MRO

SCALE— | NAME | TITLE | DATE | DRAFT | CHK | ENGR | TITLE | SIZE | SHEET OF 10 — 19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

IN AREA B7: A25 PW5 WAS SPEC AS N.C. A25 PIN 6 WAS SPEC AS TIED TO A58-01. IN AREA H6; A72 WAS SPEC WITH BALL ON OUTPUT, PIN 8.

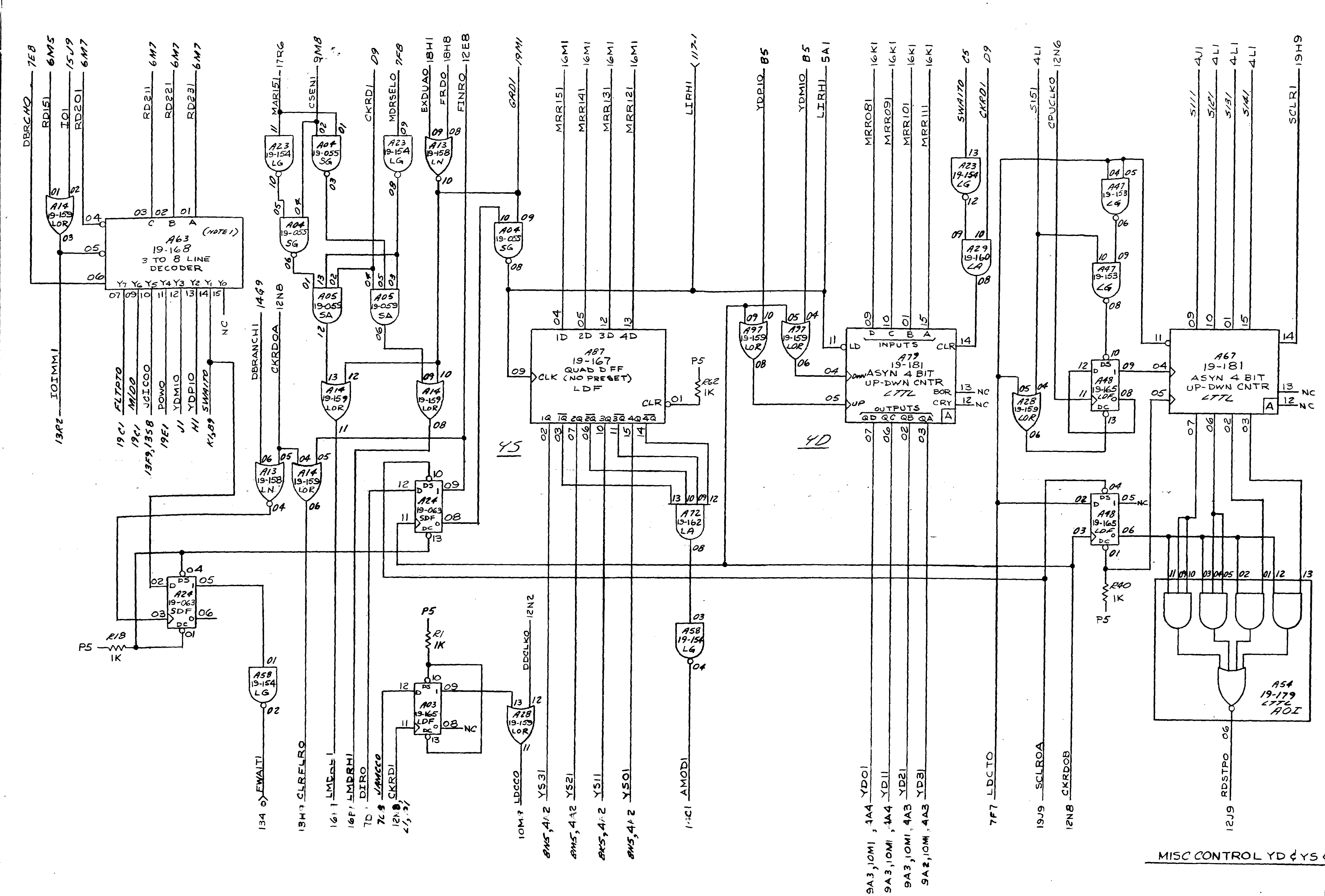
		03145-3	JB	12-11-75	R01

AREA F1: ADDED MNE. GRDI TO A04-09. CROSS-REF 19M1 WAS NOT SPEC'D.

WS	JU	3032	-	12-22-76	R02

AREAS D2, D3 & F3: A04 WAS SPEC'D AS A19-19-153. AREAS E6, B7: A24 WAS SPEC'D AS A19-165. ADDED CONN. TO 117-1 FROM MNE LIRHO AREA G1

WS	JU	3081	-	1-7-77	R03



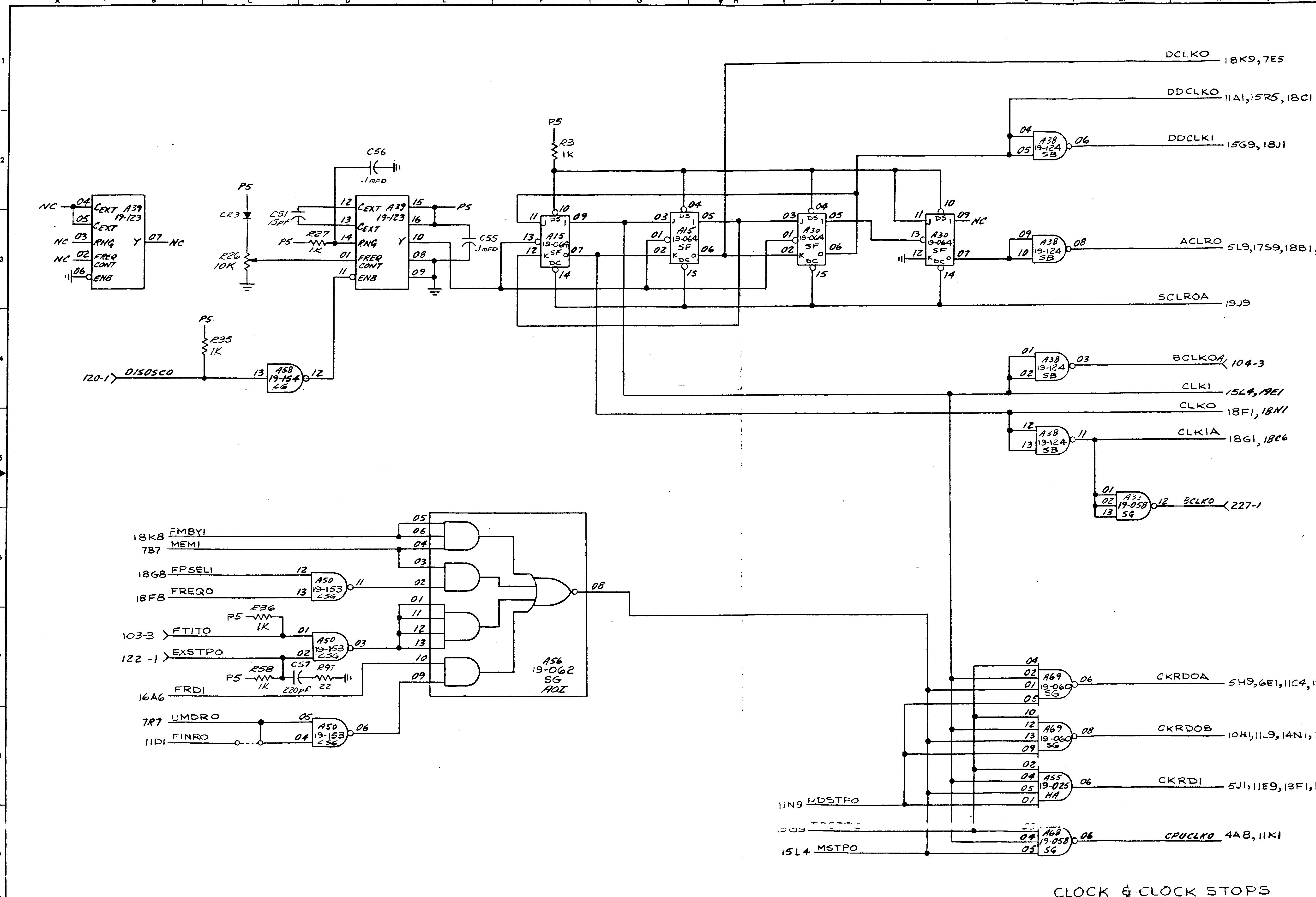
MISC CONTROL YD & YS & COUNTER

NOTES:
1. SEE TRUTH TABLE ON SHEET 7.

SCALE—	NAME	TITLE	DATE	TITLE
		DRAFT		
		CHK		
		ENGR		

03145
01-094R03D08
SHEET 11 OF 19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757



REVISIONS

AREA C3: R26 WAS 5K — 2828 — 7-15-76 R01

AREA C3: CR3 WAS SPEC'D AS R19 470Ω. AREA D2 & E3: ADDED C55 & C56. AREA D7: ADDED C57 & R97. AREA N1: ADDED SHT LOC. 7E5 TO MNEMONIC DCLKO. AREA N7: ADDED SHT ... 19B4 TO MNEMONIC CKRDOA. AREA N5: DELETED SHT LOC 19B3 FROM MNEMONIC BCLKO. AREA R8: ADDED 7B8 TO MNEMONIC CKRDI - WTA — 3081 — 1-6-77 R02

CLOCK & CLOCK STOPS

SCALE– | NAME | TITLE | DATE | DRAFT | CHK | ENGR

TITLE

03M5

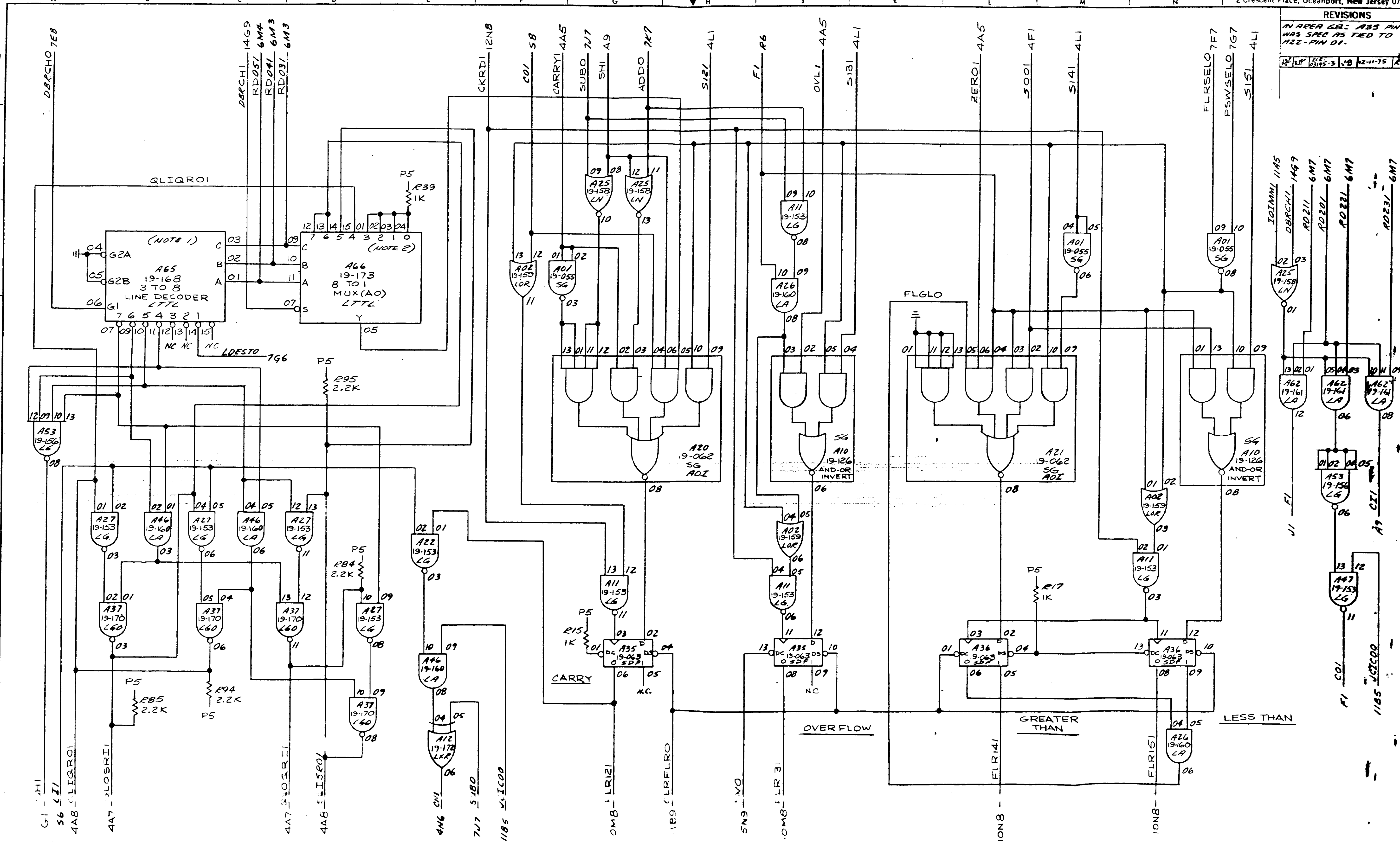
01-094R02D08

SHEET 12 OF 19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

IN AREA 6B: A35 PIN 5 WAS SPEC AS TIED TO A22-PIN 01.



FLAG REGISTER & SHIFT CONTROL

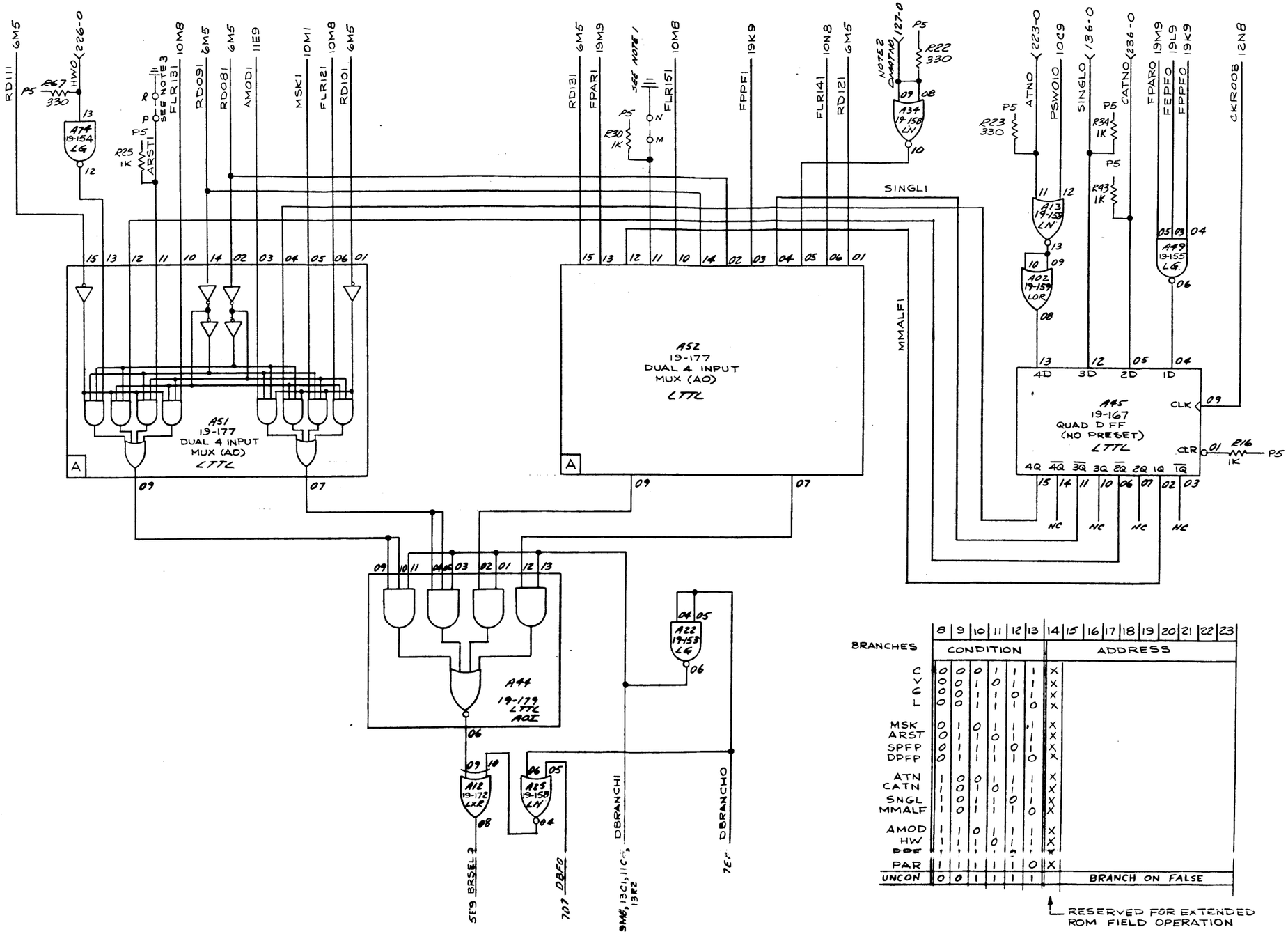
NOTES:
1. SEE TRUTH TABLE ON SHEET 7.
2. SEE TRUTH TABLE ON SHEET 8.

SCALE– | TITLE | DRAFT | CHK | ENGR

03145 01-094R01D08 13–19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
AREA G2: N,M WAS NOT SPEC'D AREA A9 & J2: NOTE 2 WAS NOT SPEC'D. AREA L3: A02-09 & 10 WAS NOT CONNECTED. A02-10 WAS CONNECTED TO A34-10 (AREA K2). AREA J8: ADDED SPFP. DPFP WAS SPEC'D AS IODMA. NOTE 1 WAS SPEC'D AS: RESISTOR & STAKES NOT EQUIPPED ON THIS ASSY.			
MFA	3081	1-6-77	R01
AREA B2: STRAP OPTIONS PER WERE NOT SPEC'D. "SEE NOTE 3" WAS "SEE NOTE 1". AREA A9: ADDED NOTE 3. AREA L2 & L3 R34 & R93 WERE 330Ω.			
GS	3168	10-18-77	R02



BRANCHES	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	CONDITION						ADDRESS									
C	0	0	0	1	1	1	X									
V	0	0	0	1	0	1	X									
Z	0	0	0	1	1	0	X									
L	0	0	0	1	1	1	X									
MSK	0	1	0	1	1	1	X									
ARST	0	1	1	1	0	1	X									
SPFP	0	1	1	1	1	0	X									
DPFP	0	1	1	1	1	1	X									
ATN	1	1	0	1	1	1	X									
CATN	1	1	1	0	1	1	X									
SNGL	1	1	0	1	0	1	X									
MMALF	1	1	1	1	1	0	X									
AMOD	1	1	0	1	1	1	X									
HW	1	1	1	0	1	1	X									
DPF	1	1	1	1	0	1	X									
PAR	1	1	1	1	1	0	X									
UNCON	0	0	1	1	1	1	BRANCH ON FALSE									

RESERVED FOR EXTENDED ROM FIELD OPERATION

BRANCH LOGIC

NOTES:
1. REMOVE JUMPER (M TO N) FOR DOUBLE PREC. FLOATING POINT OPTION.
2. JUMPER 127-0 TO GND ON BACK PANEL FOR SINGLE PROC. FLT. PT.
3. REMOVE JUMPER (PTO R) FOR AUTO-RESTART OPTION.

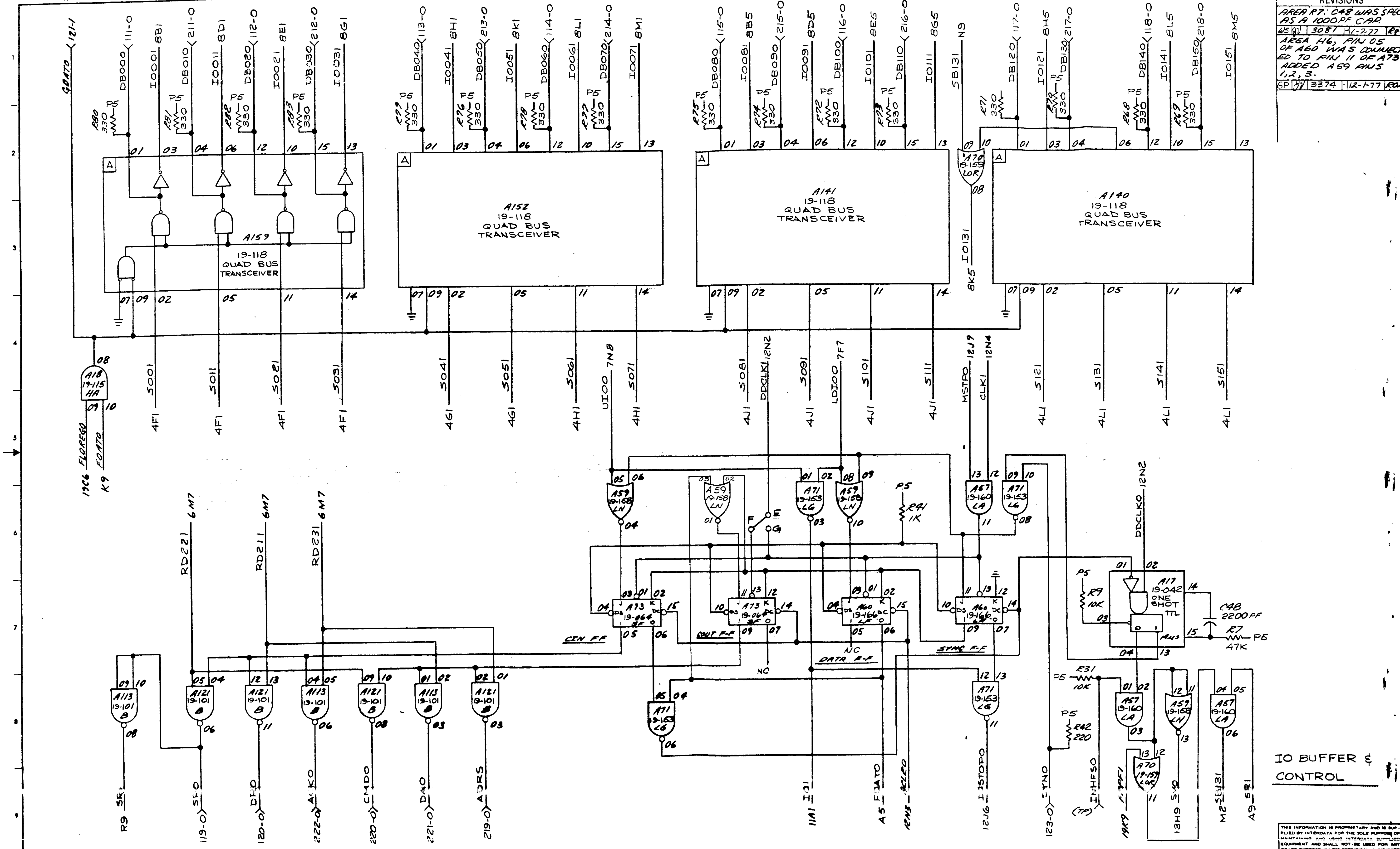
SCALE–	NAME	TITLE	DATE
TOLERANCES UNLESS OTHERWISE SPEC'FIED		DRAFT	
		CHK	
		ENGR	

TITLE

TASK NO. 03145
DWG NO. 01-094R02D08
SHEET 14 OF 19

REVISIONS

AREA R7: C48 WAS SPEC AS A 1000PF CAP.			
WS	3081	1-7-77	
AREA H6, PIN 05 OF A60 WAS CONNECTED TO PIN 11 OF A73 ADDED A69 PINS 1,2,3.			
GP	3374	12-1-77	

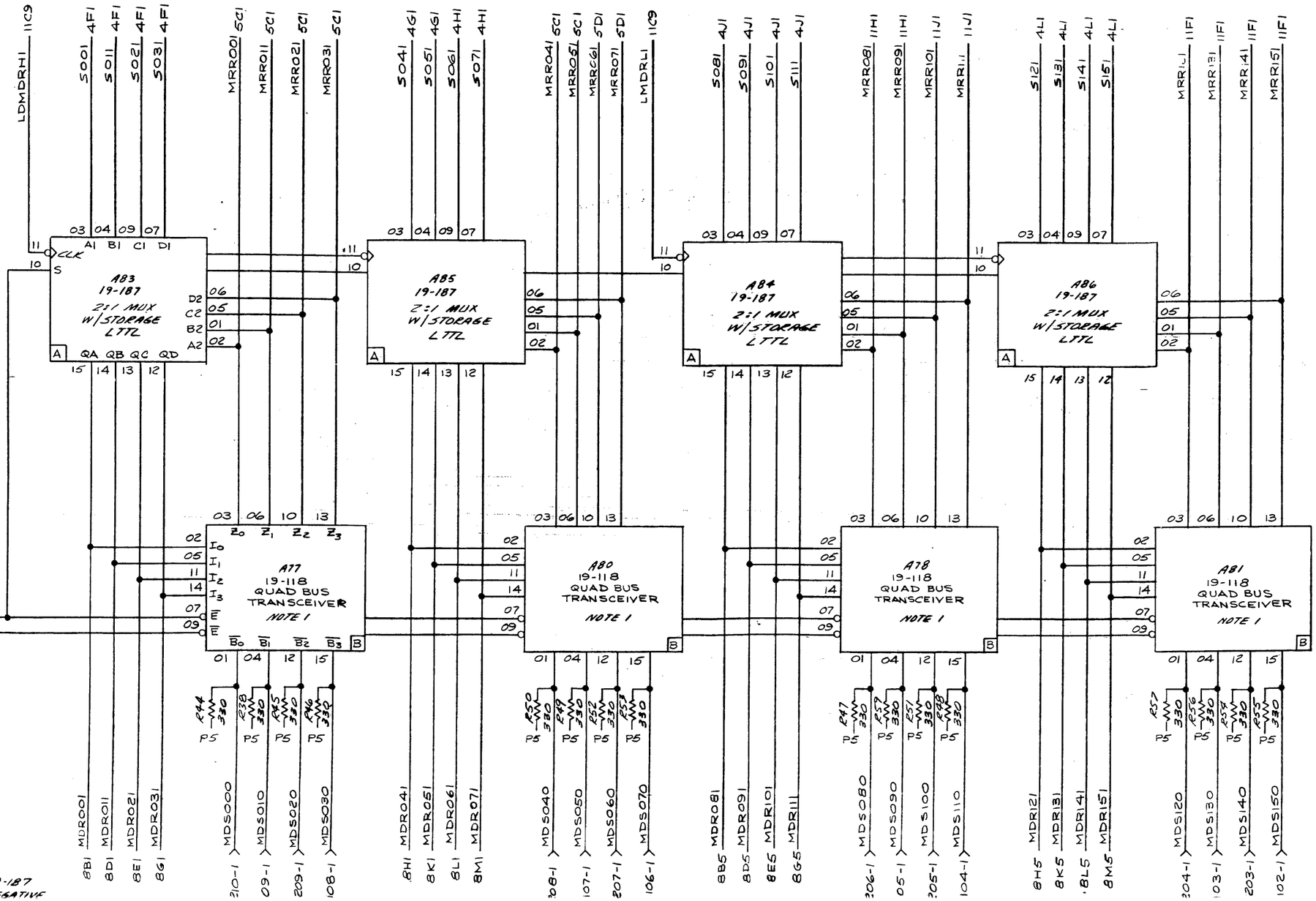


IO BUFFER & CONTROL

SCALE–	NAME	TITLE	DATE	TITLE
		DRAFT		
		CHK		
		ENGR		03145
				01-094 R02D08 15-19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



S	QA	QB	QC	QD
0	A1	B1	C1	D1
1	A2	B2	C2	D2

TRUTH TABLE : 19-187
LATCH LOADS ON NEGATIVE EDGE OF CLOCK

MDR & MEMORY BUS DRIVERS

NOTES:
1. SEE INTERNAL LOGIC SHEET 15.

SCALE—

	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE

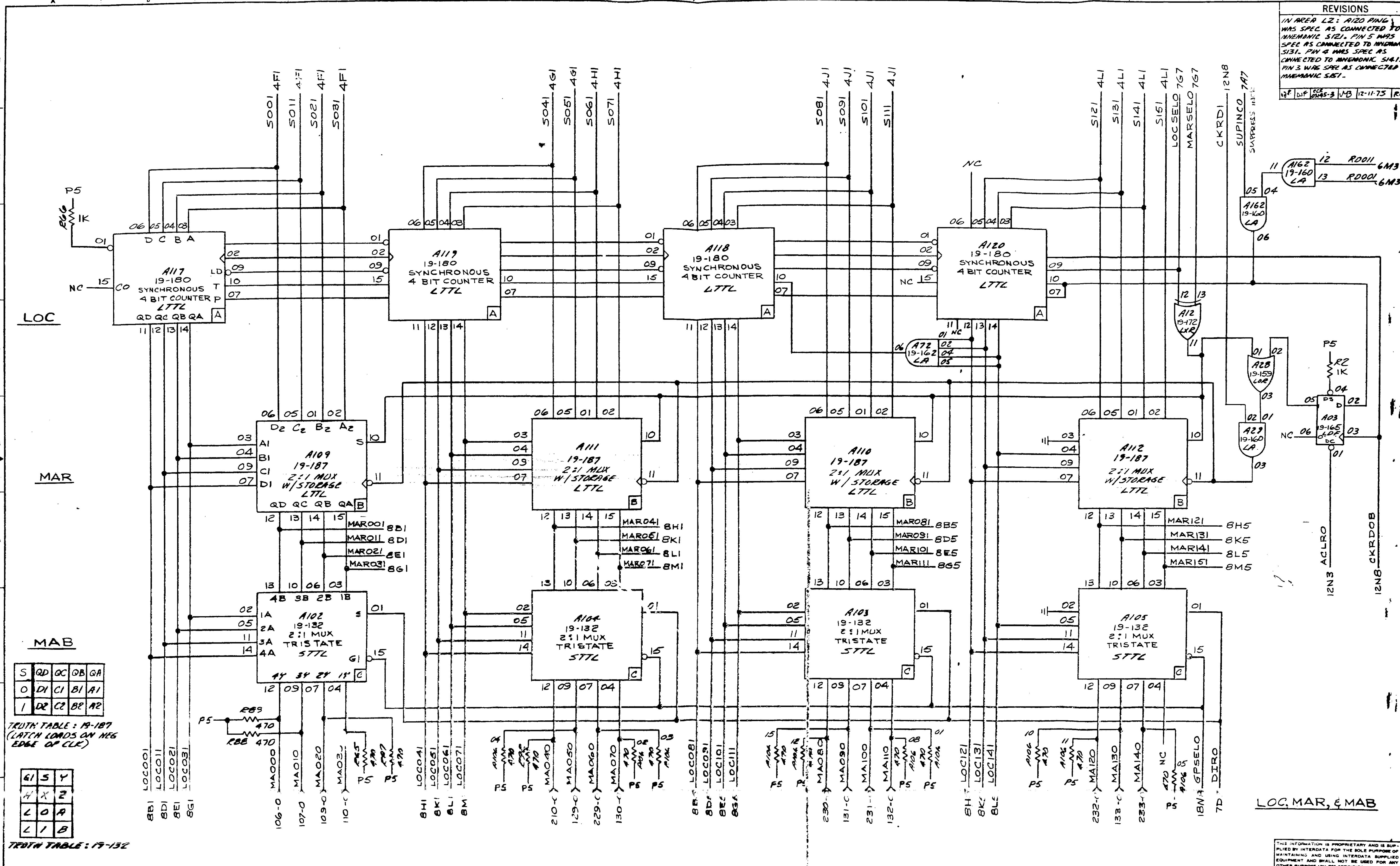
TASK NO 03145
DWG NO 01-094 005
SHEET OF 16-19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

IN AREA L2: A120 PIN 6 WAS SPEC AS CONNECTED TO MNEMONIC S121. PIN 5 WAS SPEC AS CONNECTED TO MNEMONIC S131. PIN 4 WAS SPEC AS CONNECTED TO MNEMONIC S141. PIN 3 WAS SPEC AS CONNECTED TO MNEMONIC S151.

12-11-75 R01



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SCALE– | NAME | TITLE | DATE

TITLE

08M5 01-094R11D08 17-19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

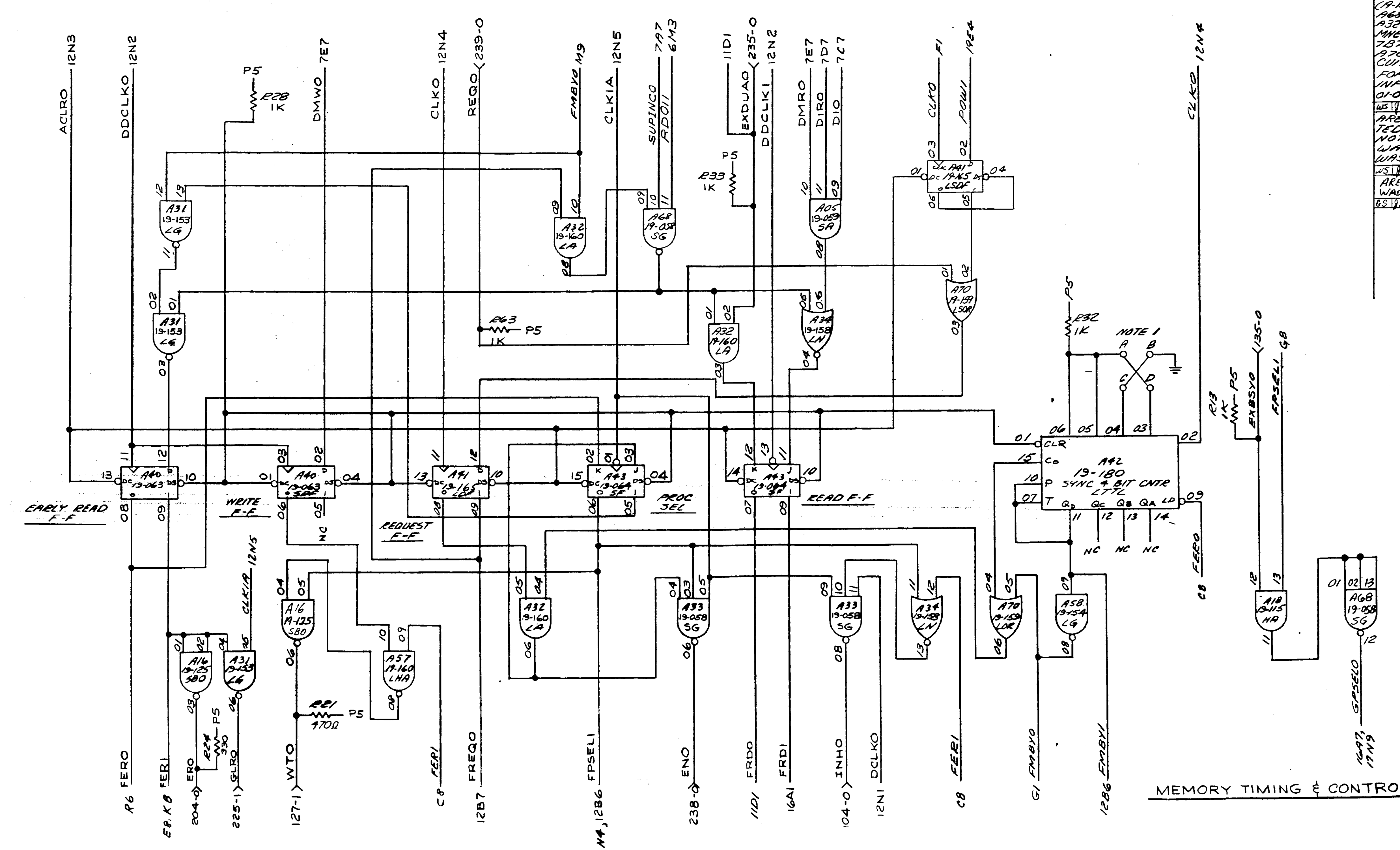
REVISIONS

AREA J9: DELETED CROSS-REF '9M1 FROM MNEMONIC FRD1
US | 3032 | 12-23-75 | R01

AREA F3: DELETED A31 (19-153). A31-08 WAS TO A68-08. A31-09 WAS TO A32-08. A31-10 WAS TO MNE. MEM1, CROSS-REF. TO 7B7. A32, A68, A41, A70 & RELATED CIRCUITRY WERE NOT SPEC'D. FOR PREVIOUS REV. INFO SEE VOIDED COPY 01-094, SHT 18, R01 D08
US | 3081 | 1-10-77 | R02

AREA E7: A57 & RELATED CIRCUITRY WAS NOT SPEC'D. A16-04 WAS TO A40-06. R21 WAS 1K.
US | 3082 | 1-10-76 | R03

AREA D7: A16 19-125 SBO WAS A16 19-036 HBO.
GS | 3214 | 6-28-77 | R04



MEMORY TIMING & CONTROL

NOTES:
1. THE FOLLOWING STRAPPING OPTIONS ARE MADE ACCORDING TO TYPE OF MEMORY TO BE INSTALLED IN PROCESSOR:

TYPE OF MEMORY	STRAPPING OPTION
SEMI	A-C-D
.75 μs CORE	A-C & B-D
1.0 μs CORE NORMALLY BUILT	A-D & B-C

SCALE— | NAME | TITLE | DATE
DRAFT
CHK
ENGR

TITLE

03145
01-094 | SHEET 18-19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
AREA F7: R96 WAS NOT SPEC'D. COLLECTOR OF Q2 WAS TO BE 20-001. WAS 20-001	WS	2839	5-10-76
AREA M2: A34-03 WAS TO MNE FRO1, CROSS-REF TO 18J9. AREA M5: R12 WAS 1K. AREA M6, B5: 1809 WAS SPEC'D AS 19-165	WS	3032	12-22-76
AREA B3: A09-03 WAS TO MNE BCLKO, CROSS-REF TO 12N5. AREA E3: ADDED MNE PDWX TO 19-13	WS	3081	1-10-77

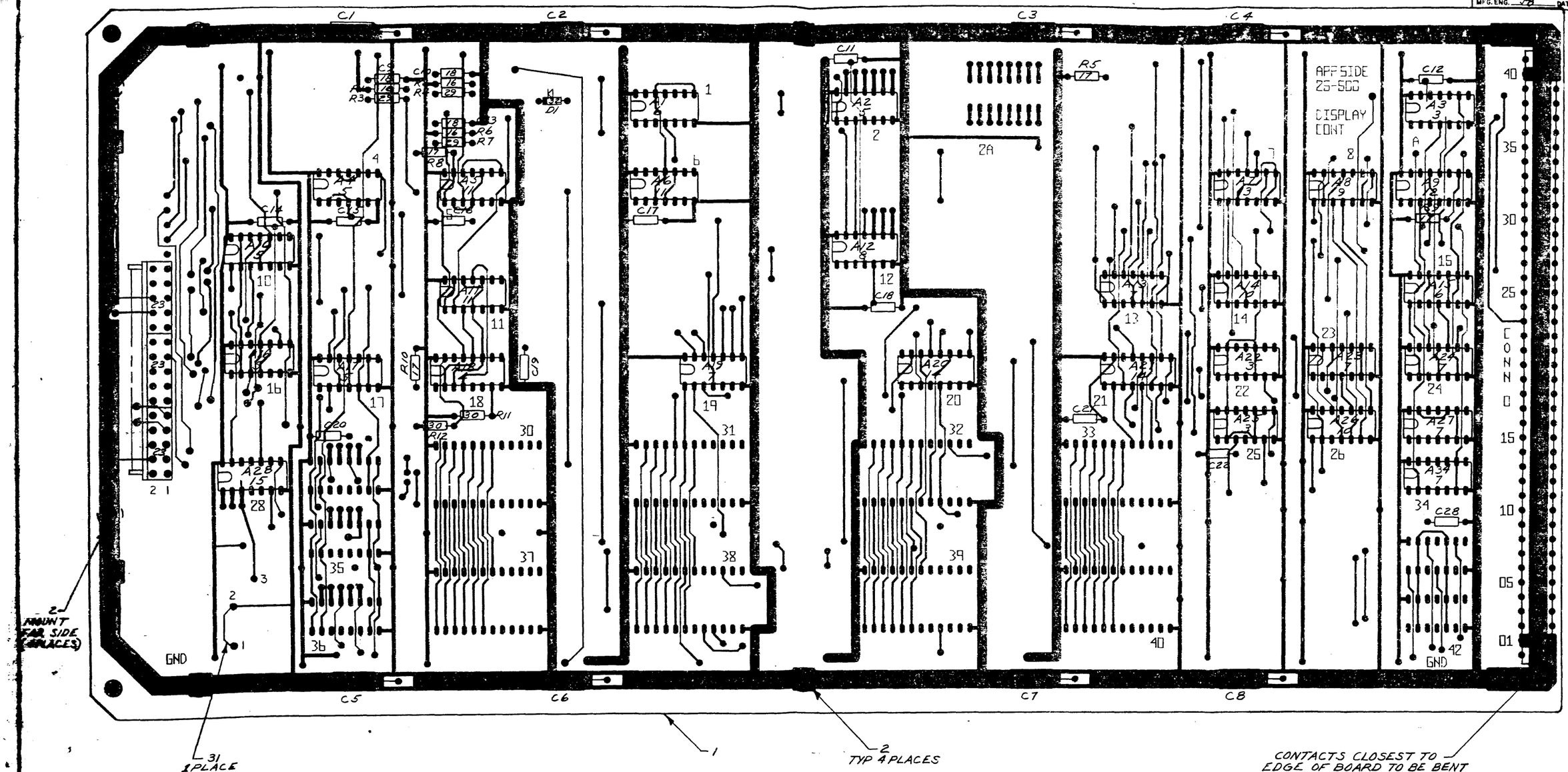
INITIALIZE & ALARM REGISTERS

SCALE–	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE

TASK NO 03165
SYS NO 01-009A0008
SHEET OF 19–19

PRE PRODUCTION APPROVAL	INIT	DATE
DEV PROD	MD	12-15-75
RELEASED FOR PRODUCTION		
MFG. ENG. JB	DATE 12-16-75	



(APP SIDE)

NOTE:
UNLESS OTHERWISE SPECIFIED ALL CAPACITORS ARE ITEM 20

REVISIONS			
REVISIED DRAWING TO REFLECT NEW COPPER, ADDED A28 ITEM 15			
GD	70345-5	MB	12-15-75	R01

COMPONENT	REF DESIGNATION
ICS	A1, A2, A3 THRU A27, A34
RESISTORS	R1 THRU R12
CAPACITORS	C1 THRU C22, C28
DIODE	D1
SWITCH	S1

B. GRAY	DRAFT	9-23-75	TITLE ASSEMBLED PRINTED CIRCUIT DISPLAY CONTROLLER LESS ALO
R. CERO	CHR	10-8-75	
D. FRANKENBERGER	ENG	12-16-75	
R. BARKER	QC	12-16-75	
S. MESSINA	MGR	12-16-75	

TASK NO. 03143 SHEET 1-1
35-601 R01 D03

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

PRE PRODUCTION APPROVAL	DEV	INIT	DATE
		DJF	11-NOV-75

REVISED SHT 3, 35-601 & 35-603 WERE R00, 35-602 WAS R01

G	DJF	03145-5	NB	12-7-75	R01

RELEASED FOR PRODUCTION
ENG. DJF DATE 12/16/75

REVISED SHTS 2&3. 35-603 WAS R01.

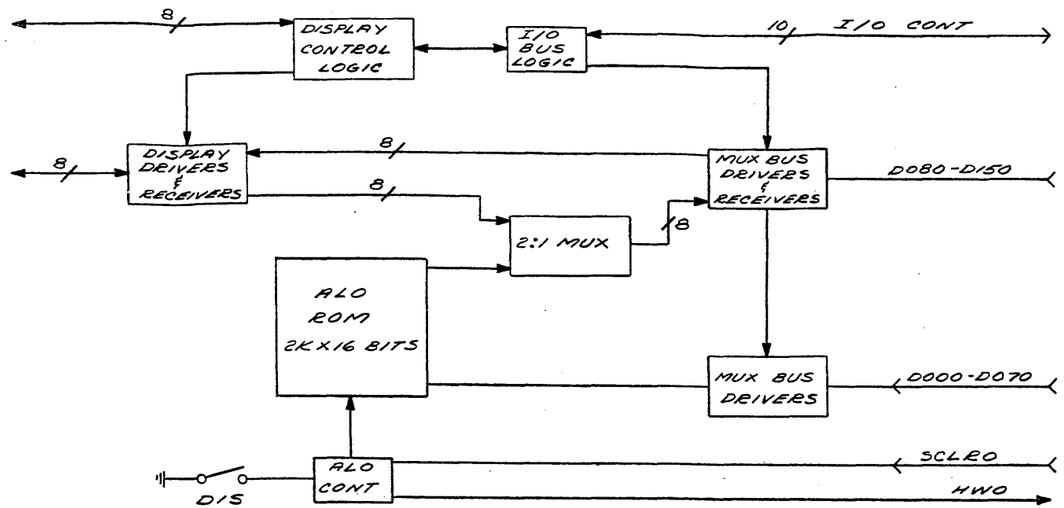
F	2774	—	3-17-76	R02	

BACK PANEL MAP

ROW 1	ROW 2	TERM NO.	CONN
		41	
		40	
		39	
		38	
		37	
INITO		36	
CATNO	SINGLO	35	
WAITI		34	
		33	
		32	
		31	
		30	
		29	
		28	
		27	
SCLRO	HWO	26	
		25	
		24	0
SYNO		23	
		22	
	DAO	21	
DRO	CMDO	20	
SRO	ADRSO	19	
D140	D130	18	
D120	D130	17	
D100	D110	16	
D080	D090	15	
D060	D070	14	
D040	D050	13	
D020	D030	12	
D000	D010	11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
		01	
		00	

ROW 2	ROW 1	TERM NO.	CONN
SHIO	GND	00	
GND	INITO	01	
D41	WAITI	02	
LAO	ESNCO	03	
DSI	ESNOO	04	
D61	POFFO	05	
SLOO	SSGLI	06	
	SCLROD	07	A
D71	GND	08	
	DOI	09	
	DII	10	
P5	D21	11	
GND	D31	12	
	SRGOA	13	
	LBO	14	
		15	
		16	

BLOCK DIAGRAM



PRINTED CIRCUIT BOARD AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

DISPLAY CONT LESS ALO	35-601 R01
DISPLAY CONT. W/ALO	35-602 R02
ALO LESS DISPLAY CONT	35-603 R02

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX					
	REV LEVEL	2	1	2	
	SHEET NO.	1	2	3	

SCALE—

NAME	TITLE	DATE
B. GRAY	DRAFT	9-4-75
R. LERO	CHK	12-16-75
D. FRANKENBERGER	ENGR	12-16-75
B. MULLER	VP TECH	12-16-75
S. MESSINA	MGR	12-16-75

TITLE: DISPLAY CONTROLLER

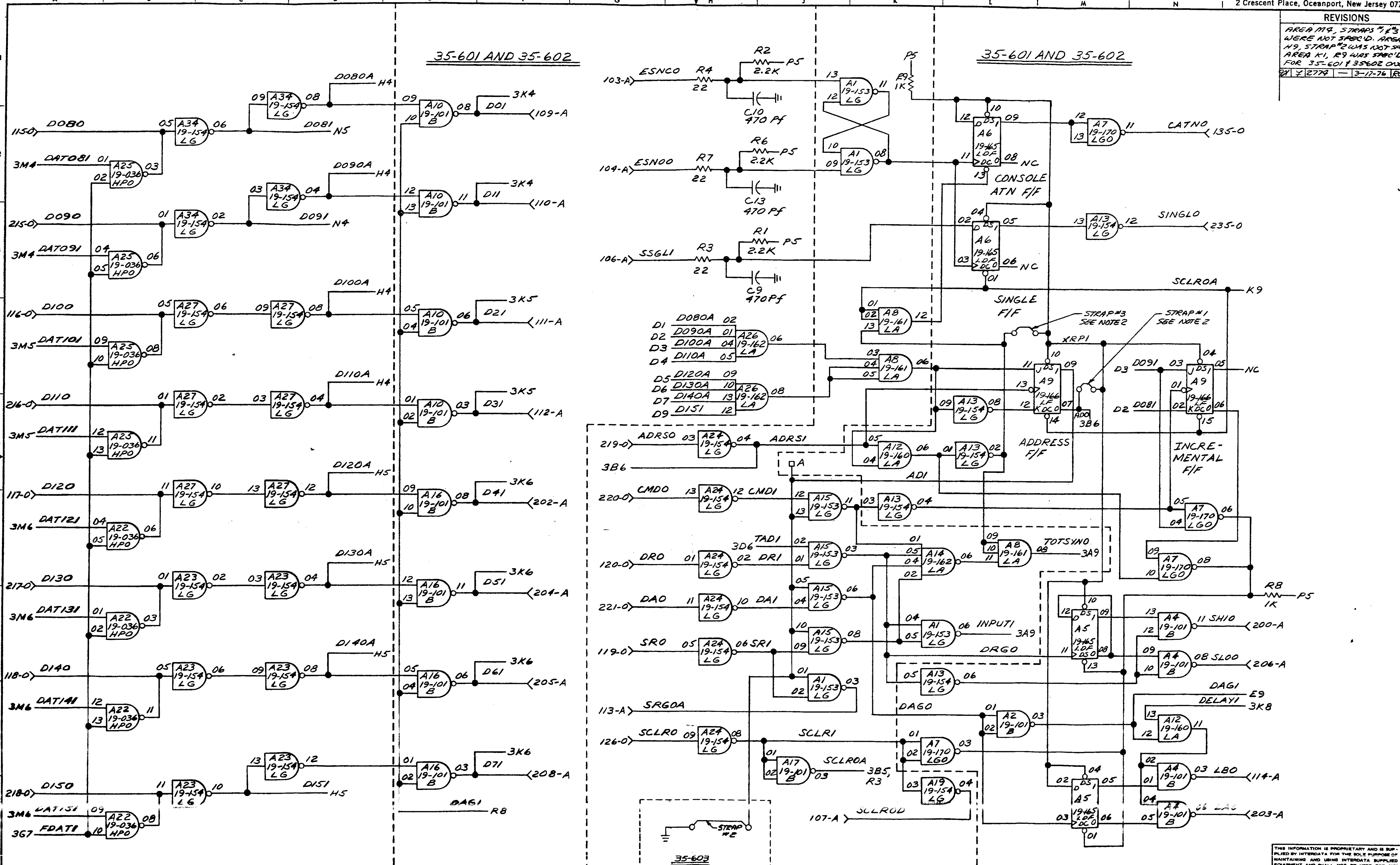
TDM No. 03145 SHEET OF 1—3
DWG. No. 02-405A02D08

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

AREA M4, STRAPS #1 & 3 WERE NOT SPEC'D. AREA H9, STRAP #2 WAS NOT SPEC'D. AREA K1, R9 WAS SPEC'D FOR 35-601 & 35-602 ONLY.

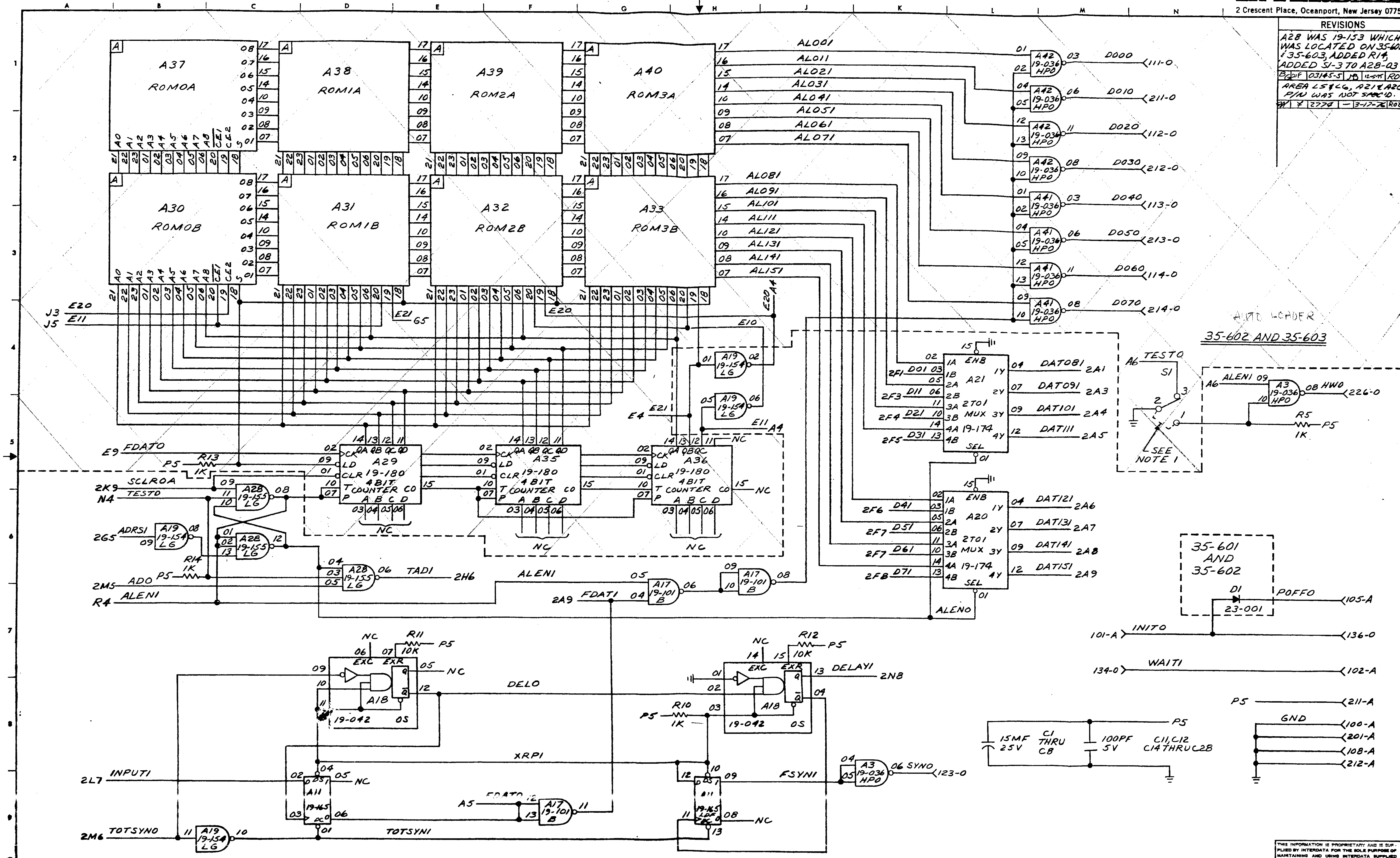
A	2774	—	3-17-76	R01



NOTE:
1. UNLESS OTHERWISE SPECIFIED ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-601, 35-602 & 35-603
2. ADD STRAPS 1 & 3 ON 35-603 ONLY. (SEE AREA M-4)

SCALE—
NAME: B GRAY
TITLE: DISPLAY CONTROLLER
DRAFT / CHK / ENGR
03/45
DWG NO. 02-405R01D08
SHEET 2 OF 3

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757



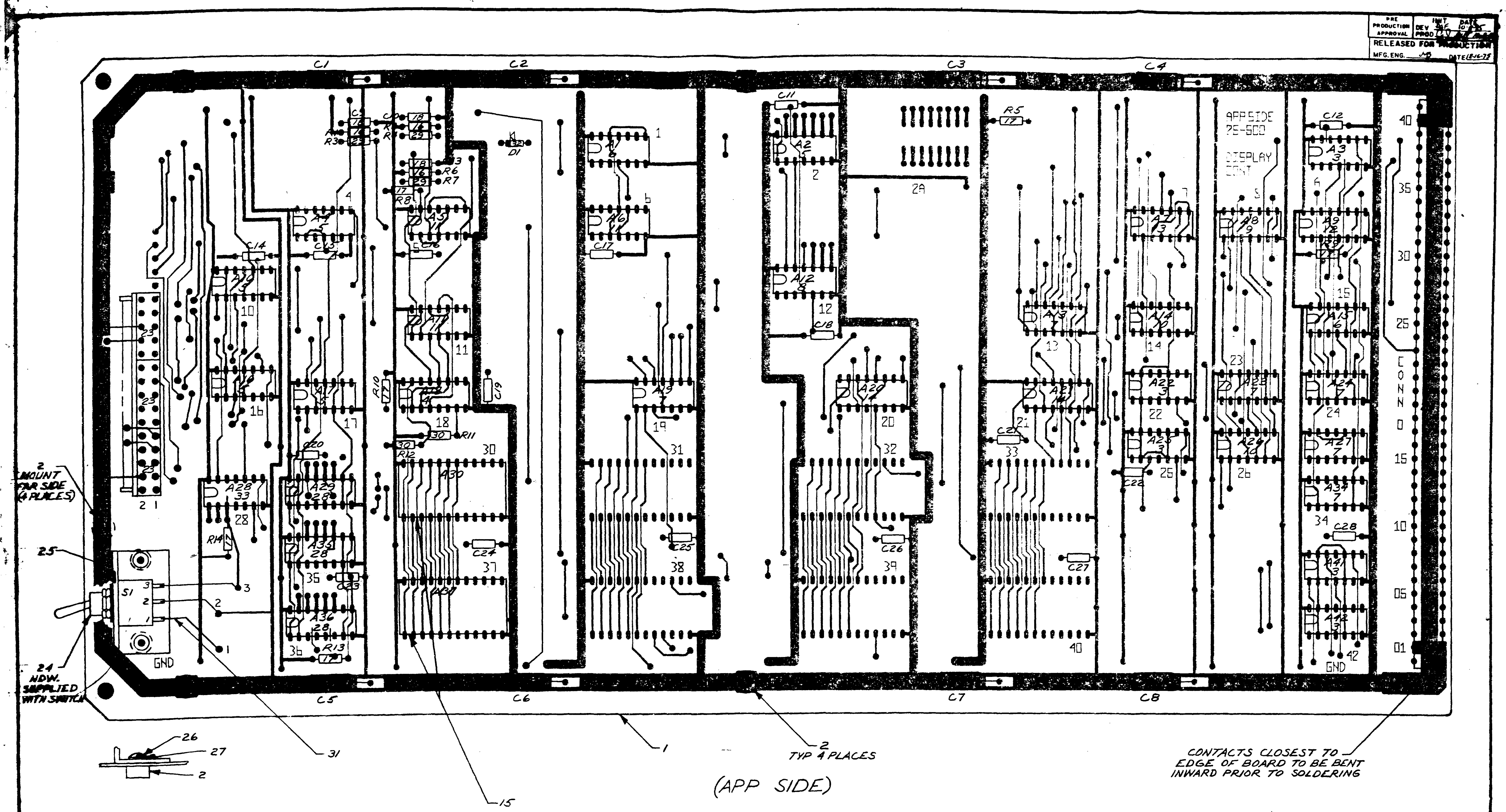
NOTES

1. STRAP CONNECTIONS S1-1 & 2 FOR 35-601 ONLY
2. ROMOA-ROM3A, ROMOB-ROM3B INDICATES LOCATIONS FOR CUSTOM WRITTEN PROM, THEY MAY OR MAY NOT BE EQUIPPED.
3. UNLESS OTHERWISE SPECIFIED ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-601, 35-602 & 35-603

SCALE—	NAME	TITLE	DATE
	B. GRAY	DRAFT	
		CHK	
		ENGR	

TITLE DISPLAY CONTROLLER

03145
02-405R02D08 SHEET 3 OF 3



(APP SIDE)

NOTE: UNLESS OTHERWISE SPECIFIED ALL CAPACITORS ARE ITEM 20

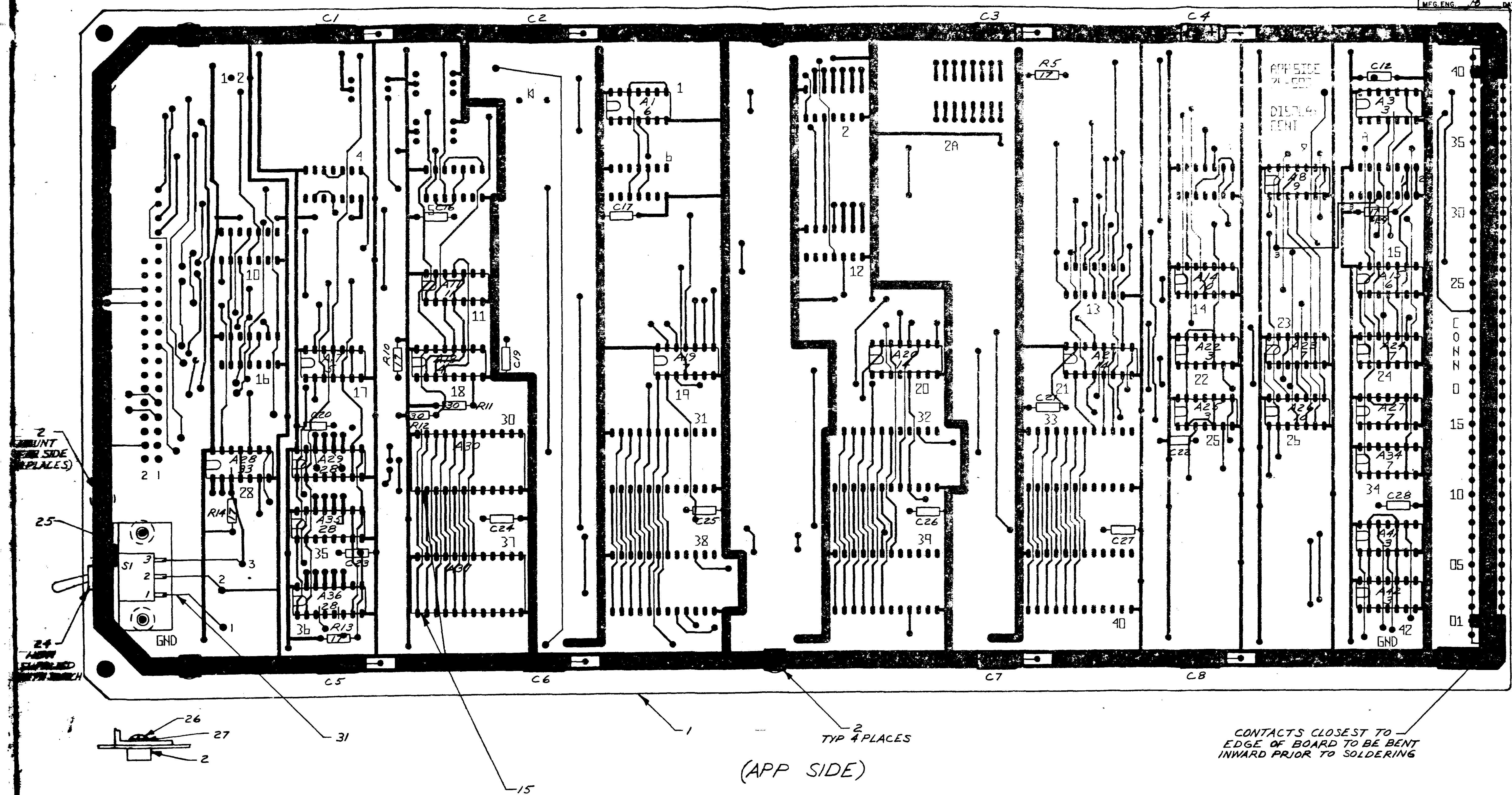
REVISIONS	COMPONENT	REF DESIGNATION
A28 WAS ITEM 6, ITEM 15 WAS 8 PLACES, ADDED R14 ITEM 17, REVISIED DRAWING TO REFLECT NEW COPPER	I.C.S	A1, A2, A3 THRU A29, A34, A35, A36, A41, A42
	RESISTORS	R1 THRU R14
	CAPACITORS	C1 THRU C28
	DIODE	D1
B G DIF 03145-S MB 12-15-75 R01	SWITCH	S1

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

B. GRAY	DRAFT	9-17-75	TITLE ASSEMBLED PRINTED CIRCUIT DISPLAY CONTROLLER W/ALD
R. CERO	CHK	10-8-75	
D. FRANKENBERGER	ENG	12-16-75	
R. BARKER	QC	12-16-75	PASR NO. 03145
S. MESSINA	MGR	12-16-75	35-602R01D03 SHEET 1-1

PRE PRODUCTION APPROVAL	INIT	DATE
DEV		10-?
PROD		

RELEASED FOR PRODUCTION
MFG ENG. | DATE



NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL CAPACITORS ARE ITEM 20
2. LAST STRAP IS #3.

AREA BELOW A3 ADDED STRAPS 1,2,3					
7	2774	—	3-16-76	RDE	

REVISIONS
A28 WAS ITEM 6, ITEM 15 WAS 8 PLACES, ADDED R14, ITEM 17, REVISED DRAWING TO REFLECT NEW COPPER
03145-5	JB	12-15-75	R01

COMPONENT	REF DESIGNATION
ICS	A1, A3 THRU A8, A11, A14, A15, A17 THRU A29, A34, A35, A36, A41, A42
RESISTORS	R5, R9 THRU R14
CAPACITORS	C1 THRU C8, C12, C16, C17, C19 THRU C28
SWITCH	S1

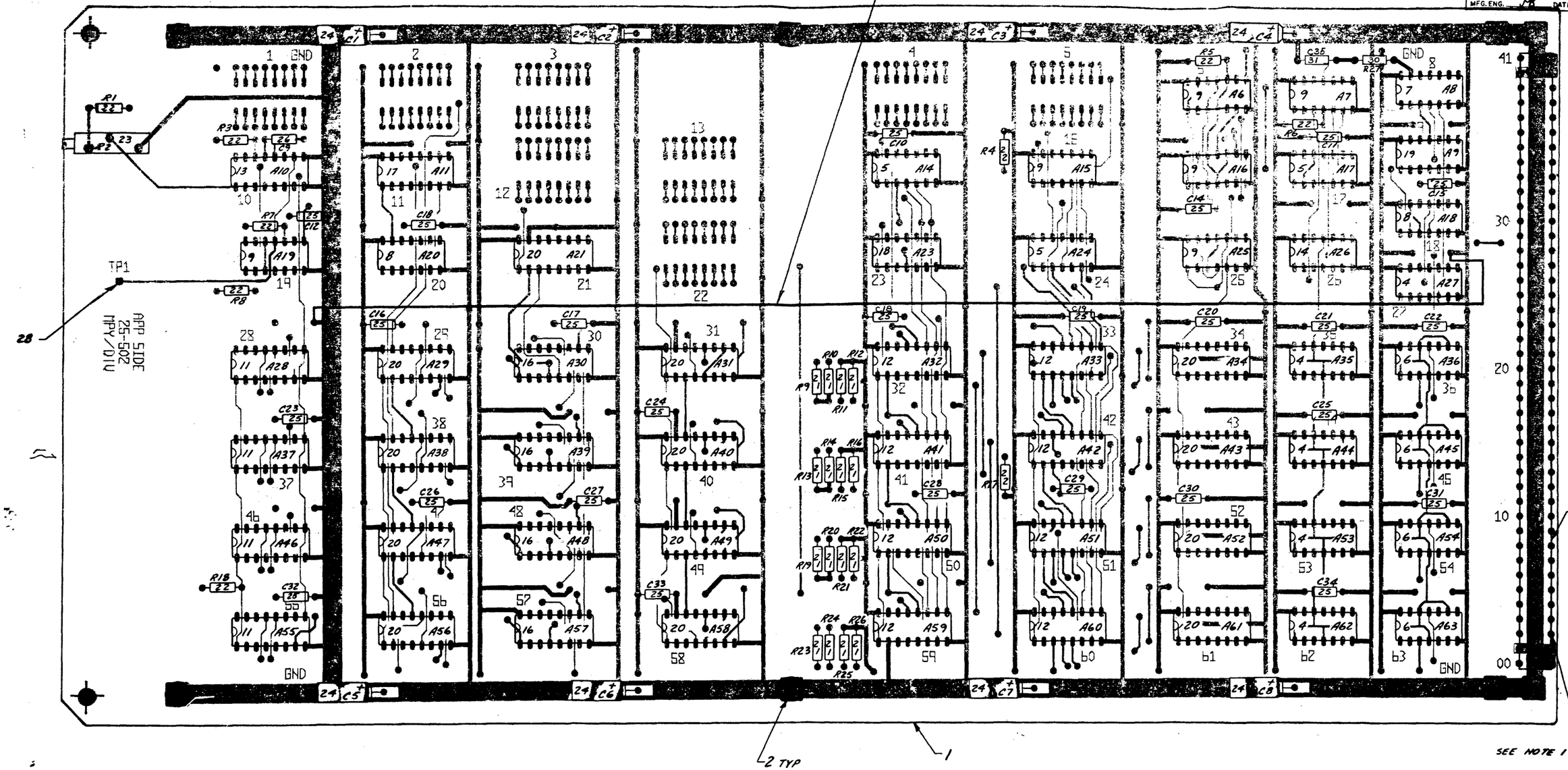
B. GRAY	DRAFT	9-24-75
R. CERO	CHK	10-8-75
D. FRANKENBERGER	ENG	12-16-75
R. BARKER	QC	12-16-75
S. MESSINA	MGR	12-16-75

TITLE
ASSEMBLED PRINTED CIRCUIT
ALO LESS
DISPLAY CONTROLLER

TASK No. 03145
35-603R02D03
SHEET 1-1

PRE PRODUCTION APPROVAL | INIT | DATE
DEV
PROD
RELEASED FOR PRODUCTION
MFG. ENG. | DATE 12-16-75

29 (THIS STRAP CONNECTS TWO (2) GRD POINTS.)



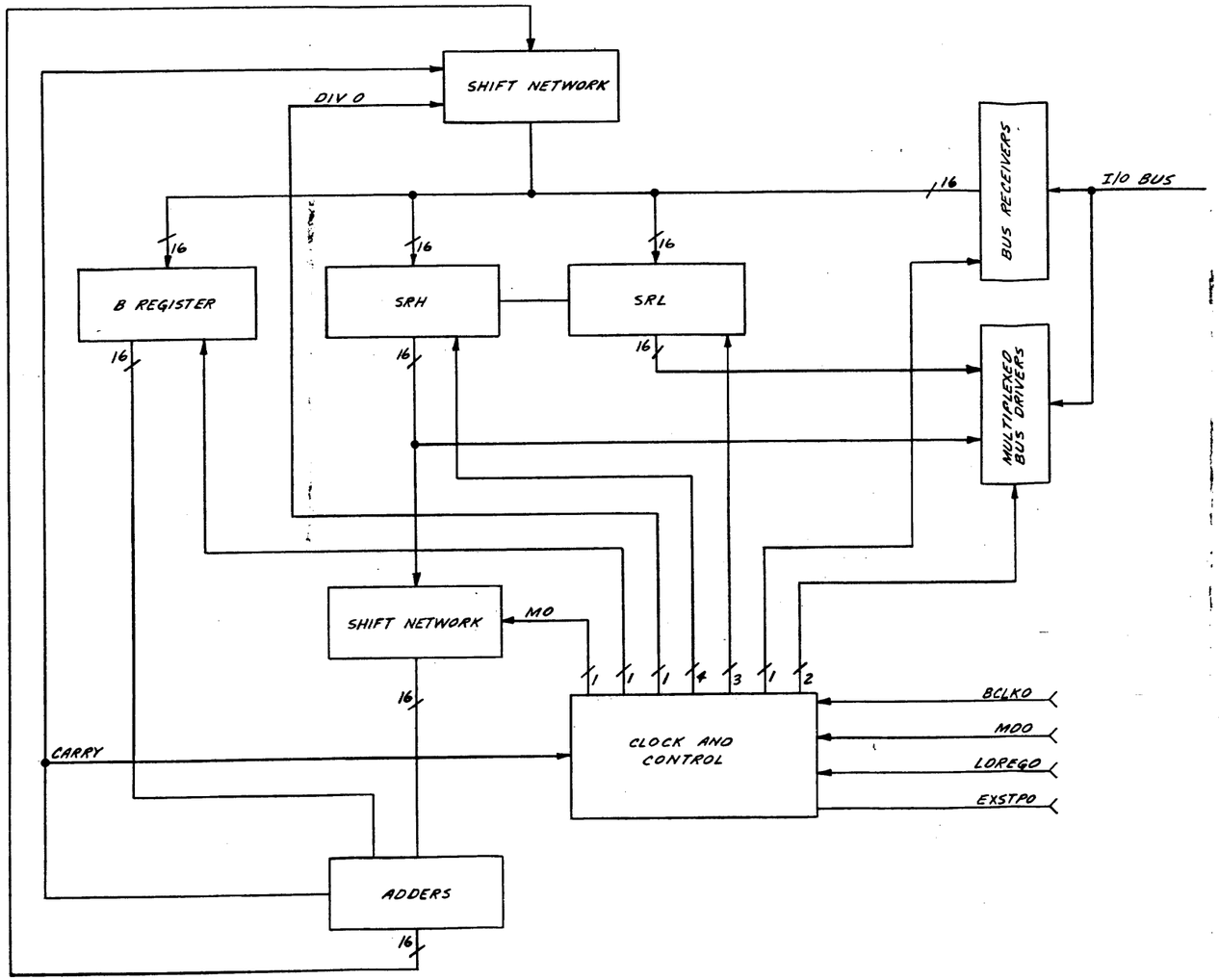
NOTES:
1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

REVISIONS	
STRAP FROM GND. PAD (ITEM 29) ABOVE A27 TO GND. PAD ABOVE A28 WAS NOT SPEC'D	
GSW 13401	V0-19-77 R01
REVISED CIRCUITRY TO REFLECT R03 COPPER, C33 (ITEM 31) & R23 (ITEM 30) ABOVE AT WERE NOT SPEC'D.	

RESISTORS	R1-R27
CAPACITORS	C1-C35
I.C.s	A6-A11, A14-A21, A23-A63

J.A. BIELSKIE	DRAFT.	9-16-76	ASSEMBLY MULTIPLY/DIVIDE 6/16A
H. MATTER	CHK.	11-16-75	
O. FRANKENBERGER	ENG.	12-16-75	
R. BARKER	Q.C.	12-16-75	03145 SH. OF 1-1
S. MESSINA	MGR.	12-16-75	35-605 R02 003

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757



TERM NO	ROW 1	ROW 2
41	P5	GND
40	GND	GND
39		
38		
37		
36		
35		
34		
33		
32		
31		
30		
29		
28	LOREGO	MIDO
27		BCLKO
26	SCLRO	
25		
24	EXSTPO	
23		
22		
21		
20		
19		
18	D140	D150
17	D120	D130
16	D100	D110
15	D080	D090
14	D060	D070
13	D040	D050
12	D020	D030
11	D000	D010
10		
09		
08		
07		
06		
05		
04		
03		
02		
01	GND	GND
00	P5	GND

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV DJF	10-7-75

REVISIED SHT. 4, 35-605 WAS R01, CONN TABLE EXTSTPO WAS PIN 122

B GSM	03145 A	VC	12-10-75	R01

RELEASED FOR PRODUCTION
ENG. DJF DATE 12-16-75

REVISED SHT 4. PC. BOARD 35-605 WAS R02.

GSM	3436	10-28-77	R02

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

MULT./DIV.	35-605 R04

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX						
REV. LEVEL	01			02		
SHEET NO.	1	2	3	4		

SCALE —

TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	9-25-75
E. CERO	CHK	10-3-75
D. FRANKENBERGER	ENGR	12-16-75
R. MULLER	SYS TEST	12-16-75
S. MESSINA	MGR.	12-16-75

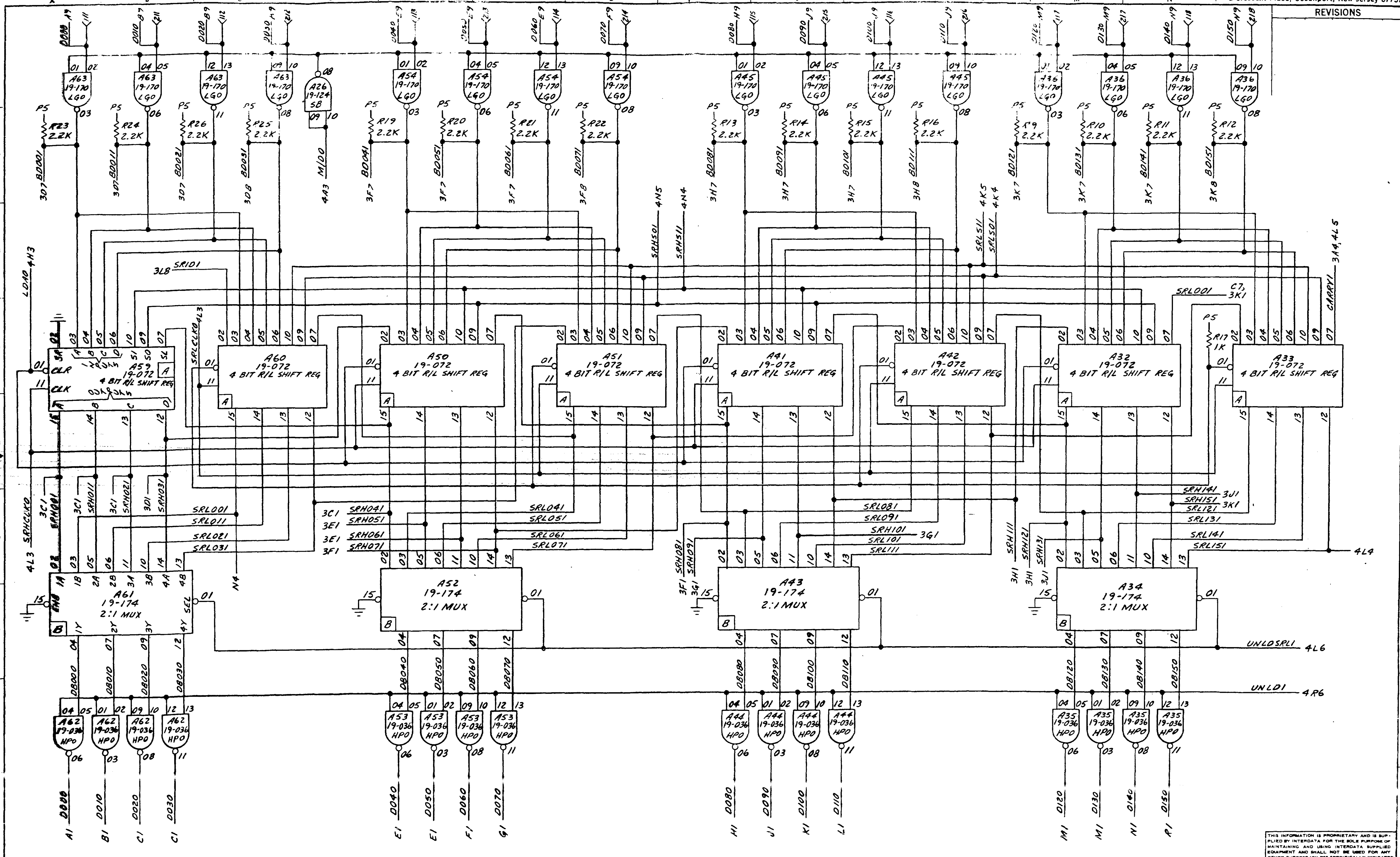
TITLE FUNCTIONAL SCHEMATIC
MULTIPLY/DIVIDE

TAPE NO. 03145
DWG NO. 02-403R02

SHEET 1 OF 4

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



SCALE–

NAME: J.R. BIELSKIE — DATE: 7-24-75

TITLE FUNCTIONAL SCHEMATIC MULTIPLY/DIVIDE

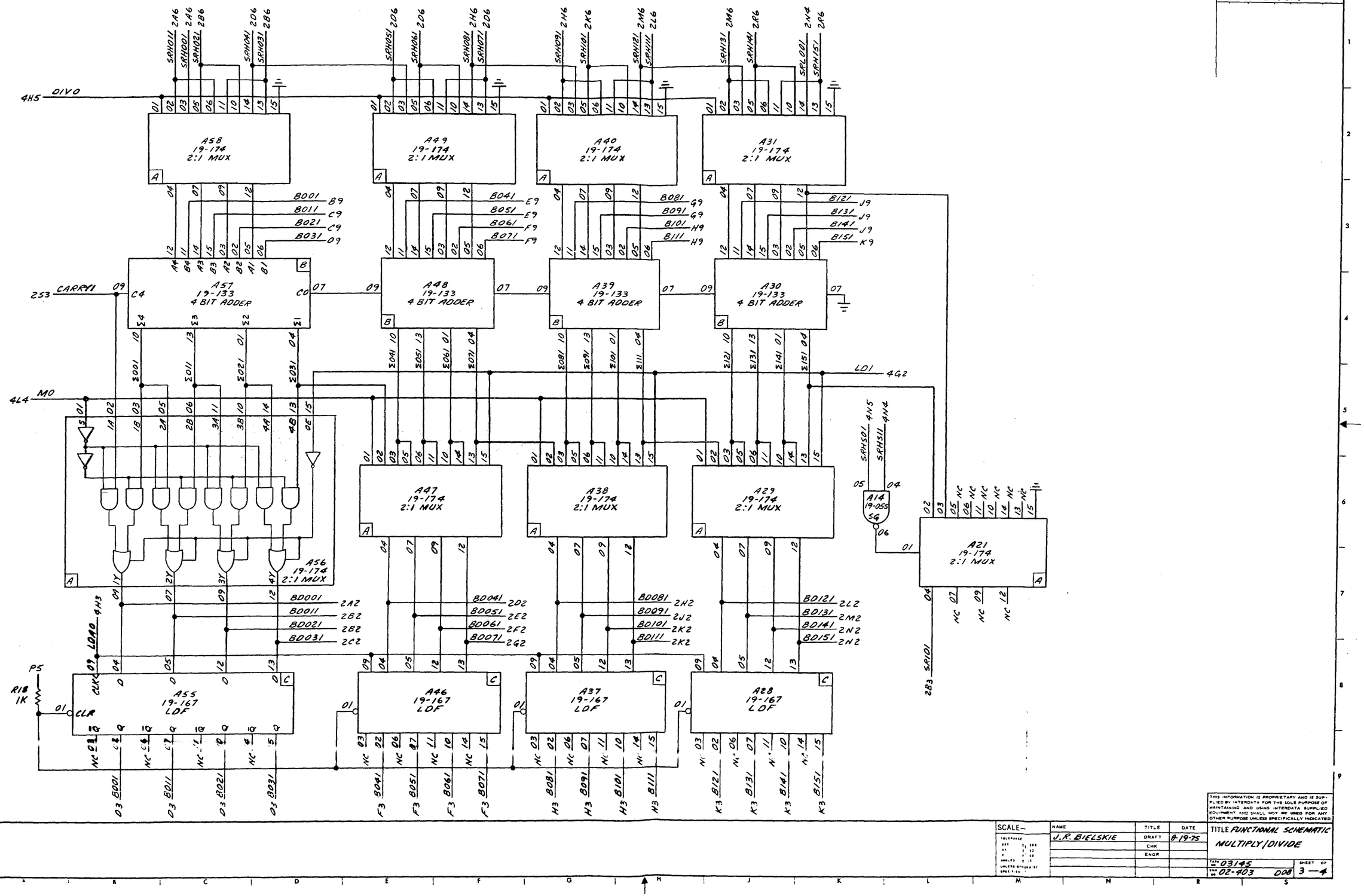
TASK NO 03145

DWG NO 02-403 D08

SHEET 2-4

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



SCALE—	NAME	TITLE	DATE
TOLERANCE	J.R. BIELSKIE	DRAFT	8-19-75
		CHK	
		ENGR	

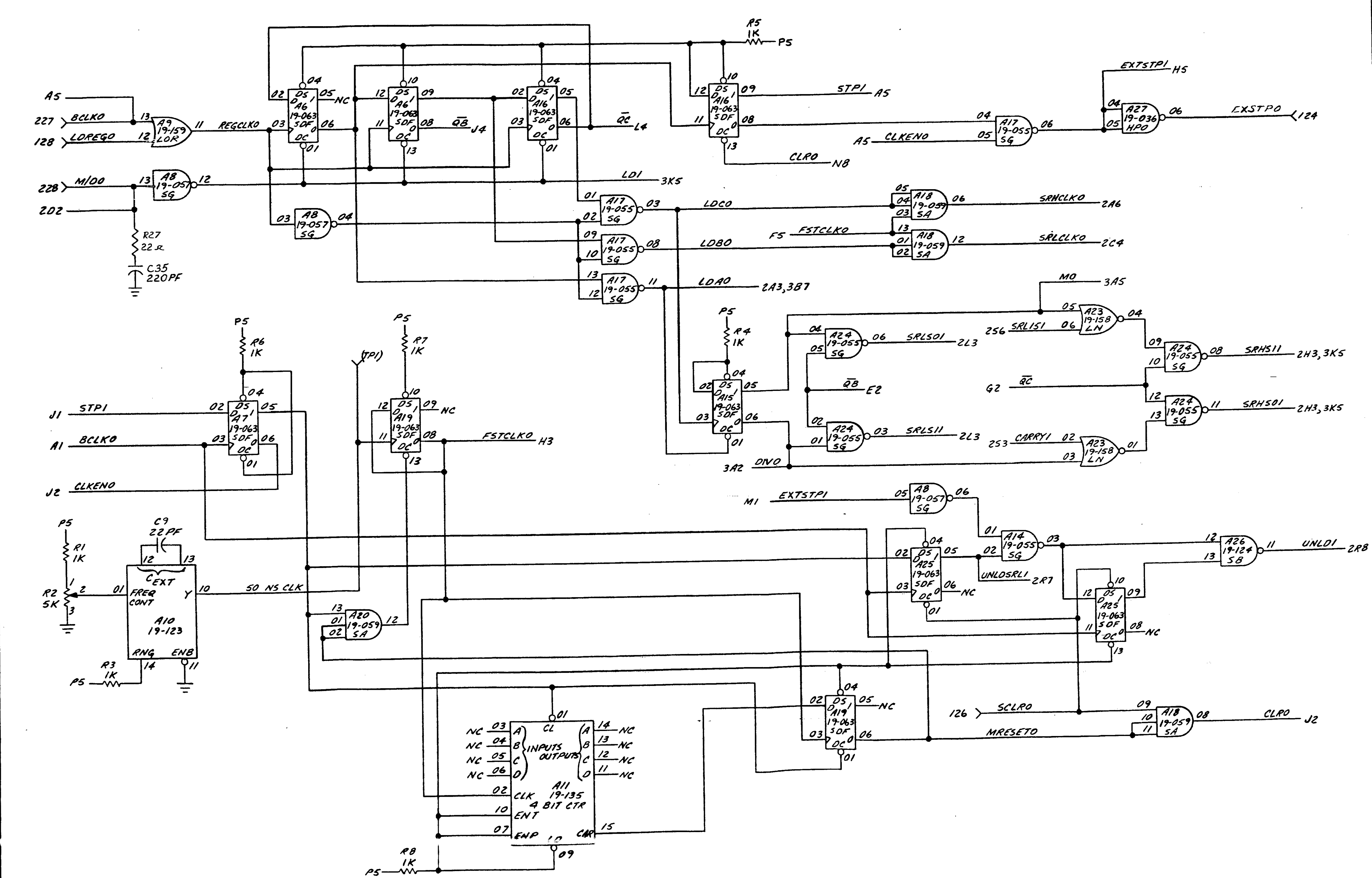
TITLE FUNCTIONAL SCHEMATIC
MULTIPLY/DIVIDE

TASK no. 03145
DWG no. 02-403 008
SHEET OF 3—4

DRAWING 44-231 24836

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS
LOC N2 PIN 124 WAS 122
B G 03145-4 R01
AREA B3: ADDED RESISTOR (R27), CAPACITOR (C35) & GND SYMBOL.
GS 3436 10-28-77 R02



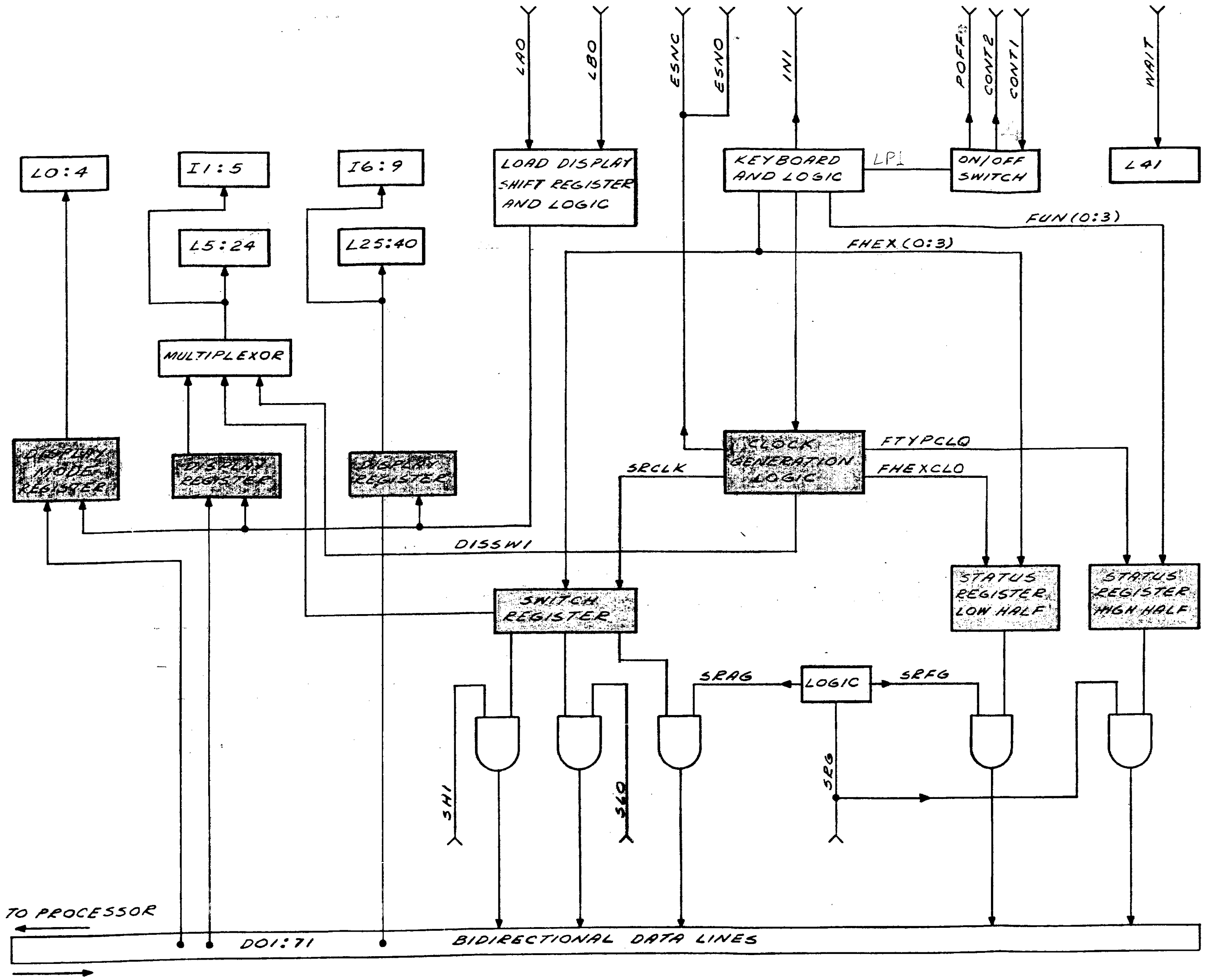
SCALE–	NAME	TITLE	DATE
	J.R. BIELSKIE	DRAFT	9-3-75
		CHK	
		ENGR	

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

TITLE FUNCTIONAL SCHEMATIC MULTIPLY/DIVIDE

03145
02-403 R02 D08
SHEET 4 OF 4

REVISIONS				
RELEASED FOR PRODUCTION MFG. ENG. [signature] DATE 2/1/74				
REVISED SHTS 2 & 3				
2323	-	1-31-75	R01	
REVISED SHTS 2 & 3				
7	2635	-	12-10-75	R02



BLOCK DIAGRAM

CONN-3		
TERM	ROW 1	ROW 2
00	GND	SHIO
01	INITO	GND
02	WAIT1	D41
03	ESNCO	LAO
04	ESNOO	D51
05	POFFO	D61
06	SSGL1	SLOO
07	SCLRO	
08	GND	D71
09	DO1	
10	D11	
11	D21	
12	D31	GND
13	SRGO	CONT3
14	LBO	

REVISION LEVEL OF THIS SHEET IS CONSIDERED THE REVISION LEVEL OF THE DOCUMENT

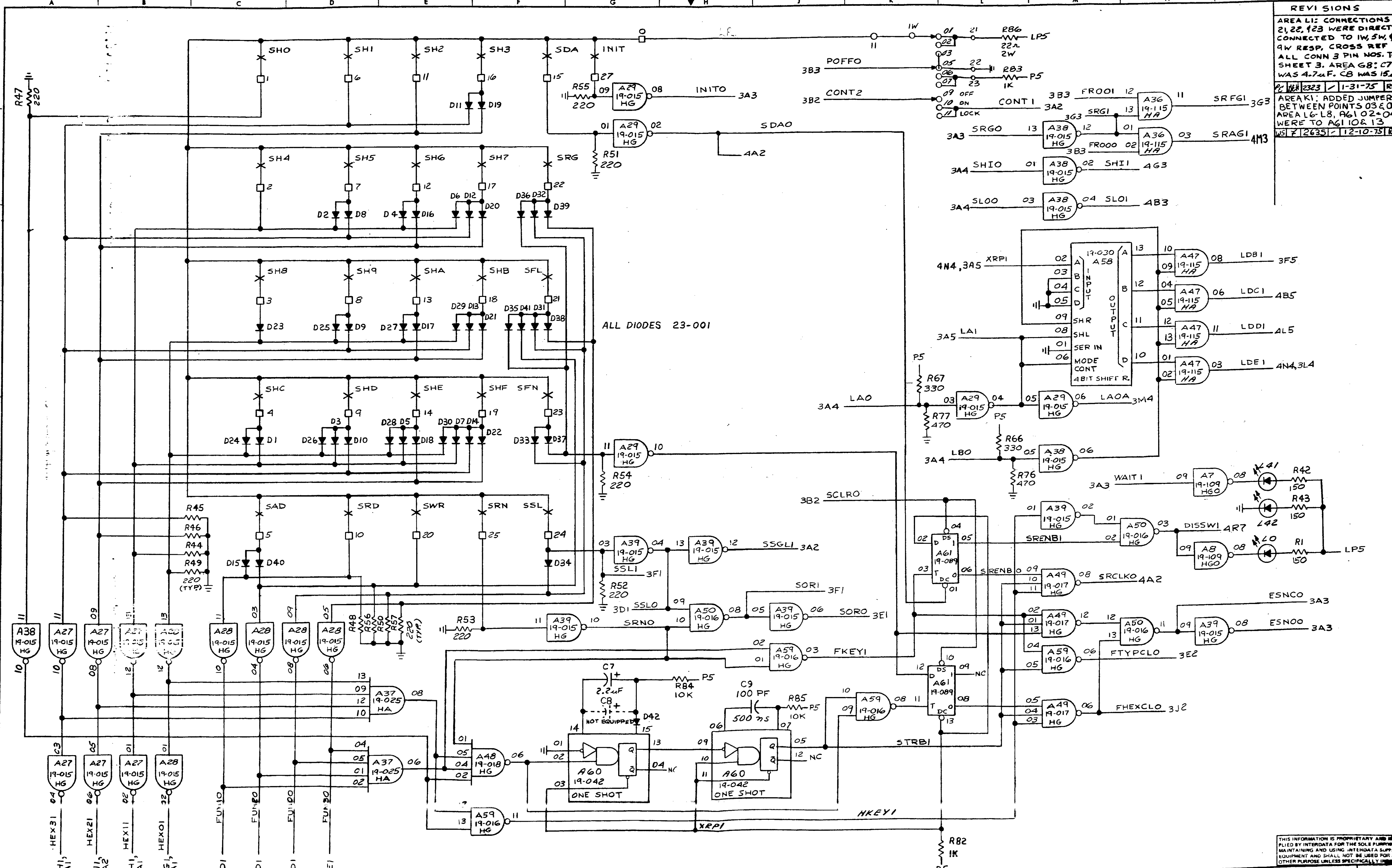
SHEET INDEX	REV	2	2	0
	SHT	2	3	4

NOTES

NAME	TITLE	DATE
H. MATTER	DRAFT	1-28-74
H. MATTER	CHK	1-28-74
S. MESSINA	ENGR	1-31-74
L. JOHMANN	TEST	1-31-74
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC HEXADECIMAL DISPLAY

TAB NO. 03081 DWG NO. 09-065R02 D08 SHEET 1 OF 4



REVISIONS

AREA L1: CONNECTIONS 21, 22, & 23 WERE DIRECTLY CONNECTED TO 1W, 5W, & 9W RESP. CROSS REF ALL CONN 3 PIN NOS. TO SHEET 3. AREA G8: C7 WAS 4.7uF. C8 WAS 15uF

PC	[illegible]	2323	1-31-75	R01

AREA K1: ADDED JUMPER BETWEEN POINTS 03 & 05 AREA L6-L8, A61 02+04 WERE TO A61 10 & 13

WS	7	2635	12-10-75	R02

NOTES
1. L0 THRU L42 ARE 33-027

NAME	TITLE	DATE	
P. EDWARDS	DRAFT	12-5-73	TITLE FUNCTIONAL SCHEMATIC HEXADECIMAL DISPLAY
	CHK		
	ENGR		TAB NO. 03081
	DIR ENG		DWG NO. 09-065R02 D08
			SHEET 2 OF 4

INTERDATA

REVISIONS			
AREA A1-A4, B1-B4: ADDED CROSS REF. FROM SHT. 2.			
PE	WAI	2323	—	1-31-75	R01
AREA B2. ADDED SCLRO REF. FROM SHT. 2			
WS	≠	2635	-	12-11-75	R02

DBI-C3 CONT3
213-3 TP
214-3 TP
DBI-C2 23 CONT2 2J1
DBI-C1 CONT1 2L2
106-3 14 SSGLI 2J6
107-3 9 SCLRO J1,2J6
105-3 22 POFFO 2J1
101-3 12 INITO 2H1
103-3 15 ESNCO 2S7
104-3 16 ESNOO 2S7
113-3 17 SRGO 2L2
102-3 10 WAITI 2M5
206-3 8 SLOO 2L3
208-3 20 SHIO 2L3
114-3 19 LBO 2L5
203-3 13 LAO 2K5
208-3 D71
205-3 D61
204-3 D51
202-3 D41
112-3 D31
111-3 D21
110-3 D11
109-3 D01
2L3 XRPI
2L4 LAI

FUN00 2D9
FUN10 2C9
SSLO 2G7
FUN20 2C9
SORO 2K7
FUN30 2D9
FTYPCLO 2N7
SCLRO J1
SORI 2J7
SSLI 2G7

A46 19-071
A57 19-043 HGO
R81 1K P5
R80 1K P5

2M2 FROO1
2M2 FROOO
2M2 SRGI
A35 19-036 HPO

HEX01 2B9
HEX11 2B9
HEX21 2A9
HEX31 2A9
FHEXCLO 2N8
SCLRO B2
R78 1K P5 E1
A56 19-071
2R2 SRFG1
A45 19-036 HPO

A1 19-071
A8 19-109 HGO
L1 R2 150 LP5
L2 R3 150
L3 R4 150
L4 R7 150
LAOA 2N5
LDE1 2R4

P5
R64 R63 R65 R62 R61 R60 R59 R58 330 (TYP.)
R68 R69 R70 R71 R72 R75 R73 R74 470 (TYP.)
D71 4A4
D61 4A4
D51 4A4
D41 4A4
D31 4A4
D21 4A4
D11 4A4
D01 4A4

2R4 LDBI
R79 1K P5

A26 19-030 4 BIT SHIFT REG.
A25 19-030 4 BIT SHIFT REG.
A24 19-030 4 BIT SHIFT REG.
A23 19-030 4 BIT SHIFT REG
SHR SHL SER IN MODE CONT

A7 19-109 HGO
A6 19-109 HGO
A5 19-109 HGO
L40 L39 L38 L37
L36 L35 L34 L33
L32 L31 L30 L29
L28 L27 L26 L25
R38 R39 R41 R40 150
R34 R35 R37 R36 150
R30 R31 R33 R32 150
R26 R27 R29 R28 150
LP5 4A8

A17 33-029 HEX DISPLAY
A16 33-029 HEX DISPLAY
A15 33-029 HEX DISPLAY
A14 33-029 HEX DISPLAY

LP5 — L GND
33MF, 10V
C1 & C2

P5 — GND
33MF, 10V
C3 TO C6

P5 — L GND
0.1MF, 30V
C10 TO C14

P5 — GND
0.1MF, 30V
C15 TO C39

DECOUPLING CAPACITORS

NOTES

NAME	TITLE	DATE	TITLE FUNTIONAL SCHEMATIC
P. EDWARDS	DRAFT	12-3-73	HEXADECIMAL DISPLAY
	CHK		
	ENGR		
	DWR ENG		TASK NO 03081
			DWG NO 09-065R02 D08 SHEET OF 3-4

DRAWING 64-231 10643

INTERDATA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

HEX01 2B9 · HEX11 2B9 · HEX21 2A9 · HEX31 2A9 · SRCLK0 2M7 · SDA0 2H2

SW161 SW171 SW181 SW191 SW121 SW131 SW141 SW151 SW081 SW091 SW101 SW111 SW041 SW051 SW061 SW071 SW001 SW011 SW021 SW031

A55 A54 A53 A52 A51 — 19-071

SL01 2N3 · SHI1 2N2 · SHAS1 2R2

A44 A43 A42 A41 A40 — 19-036 HPO

D71 3R4 · D61 3R4 · D51 3R5 · D41 3R5 · D31 3R5 · D21 3R5 · D11 3R5 · D01 3R5

LDC1 2R4 · LDD1 2R4 · LDE1 2R3 · XRP1 2L3

A34 A33 A32 A31 A30 — 19-030 4 BIT SHIFT REG

A22 A21 A20 A19 A18 — 19-053 2:1 MUX.

DISSWI 2N6

A5 A4 A3 A2 A8 — 19-109 HGO

L24 L23 L22 L21 L20 L19 L18 L17 L16 L15 L14 L13 L12 L11 L10 L9 L8 L7 L6 L5

R23 R24 R25 R22 R19 R18 R20 R21 R16 R15 R14 R17 R12 R11 R10 R13 R8 R9 R4 R5 — 150

LP5 3L8

A13 A12 A11 A10 A9 — 33-029 HEX DISPLAY

NOTES

NAME	TITLE	DATE
P EDWARDS	DRAFT	12-3-73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC HEXADECIMAL DISPLAY

TASK NO 03081 · DWG NO 09-065 · DOB · SHEET OF 4-4

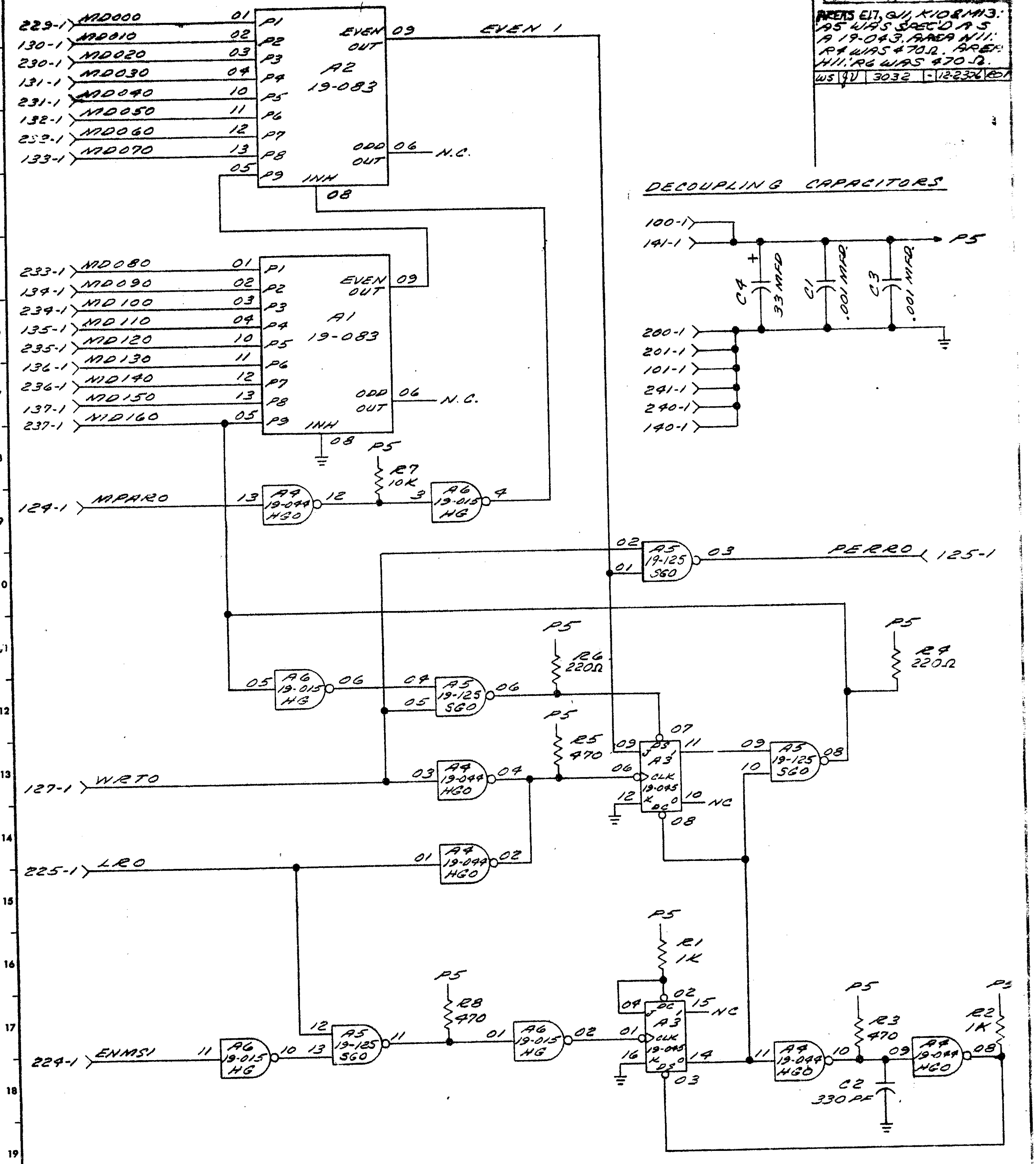
DRAWING 44 231 16042

INTERDATA

RELEASED FOR PRODUCTION
ENG. ENG. DATE

AREAS E17, G11, K10 & M13: A5 WAS SPEC'D AS A 19-043. AREA N11: R4 WAS 470Ω. AREA H11: R6 WAS 470Ω.

WS	GV	3032	-	12-23-76	



NOTES 1. UNLESS OTHERWISE SPECIFIED ALL APPARATUS THIS SHEET LOCATED ON 35-568.

2. THIS OPTION, WHEN EQUIPPED IS INSTALLED AT THE BACKPANEL ON SLOT 3, CONNECTOR 1.

NAME	TITLE	DATE
R F CERO	DRAFT	11-1-74
R F CERO	CHK	11-1-74
G JOYCE	ENGR	12-5-74
C MALUDA	QC	12-5-74
D FRANKENBERGER	MGR	12-5-74

TITLE SCHEMATIC PARITY OPTION BOARD 7/32

TASK NO. 03/32

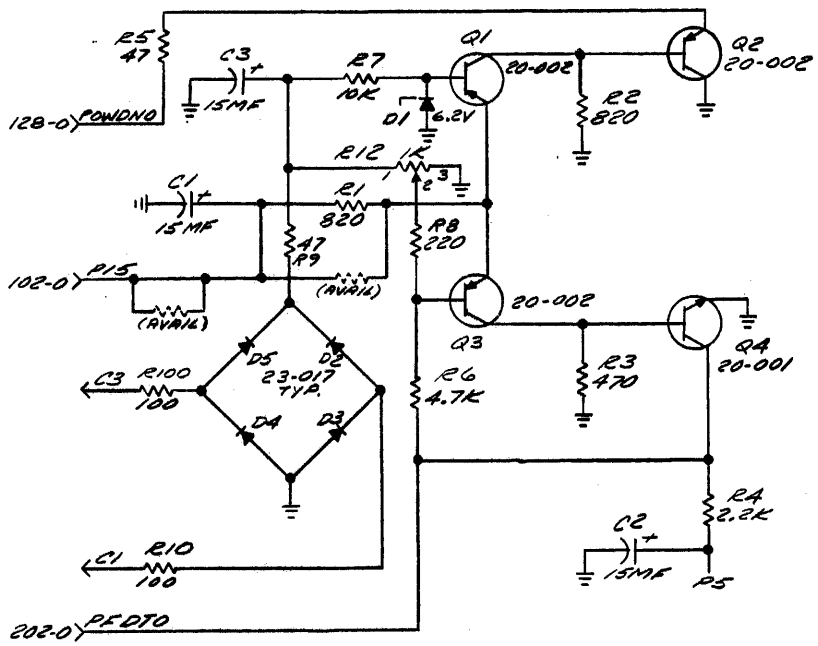
DWG. NO. 02-368R01D08

SHEET 1 OF 1

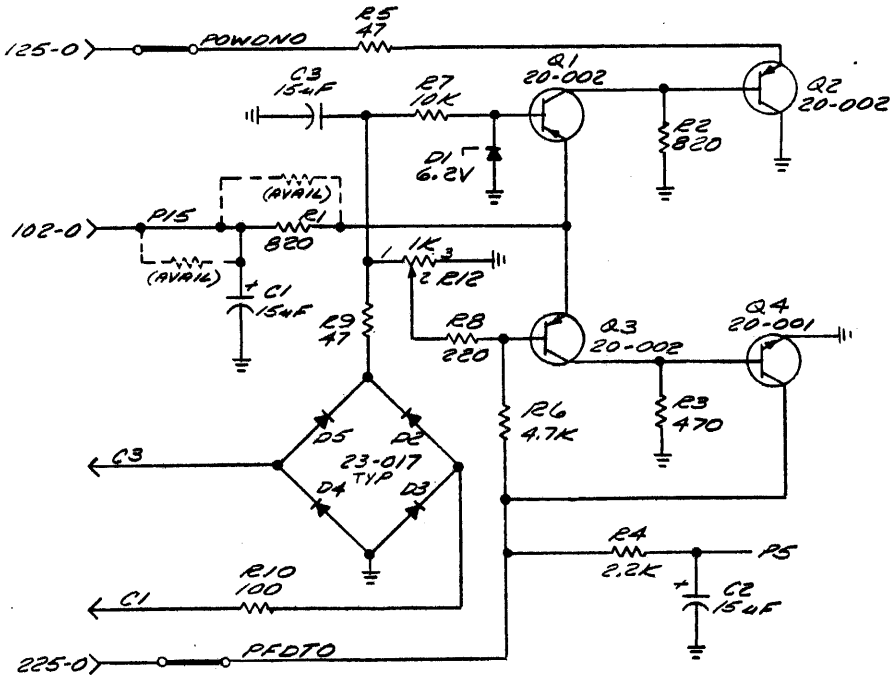
INTERDATA

REVISIONS

RELEASED FOR PRODUCTION
MFG. ENG. _____ DATE 5/6/76



F00



F01

SCALE—N	NAME	TITLE	DATE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .05, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	P.EDWARDS	DRAFT	1-19-75
	R.CERO	CHK	4-6-76
	D.FRANKENBERGER	ENGR	4-6-76
	R.BARKER	Q.C.	4-6-76
	S.MESSINA	MGR.	4-6-76

TITLE PRIMARY POWER FAIL

TAPE NO. 03175

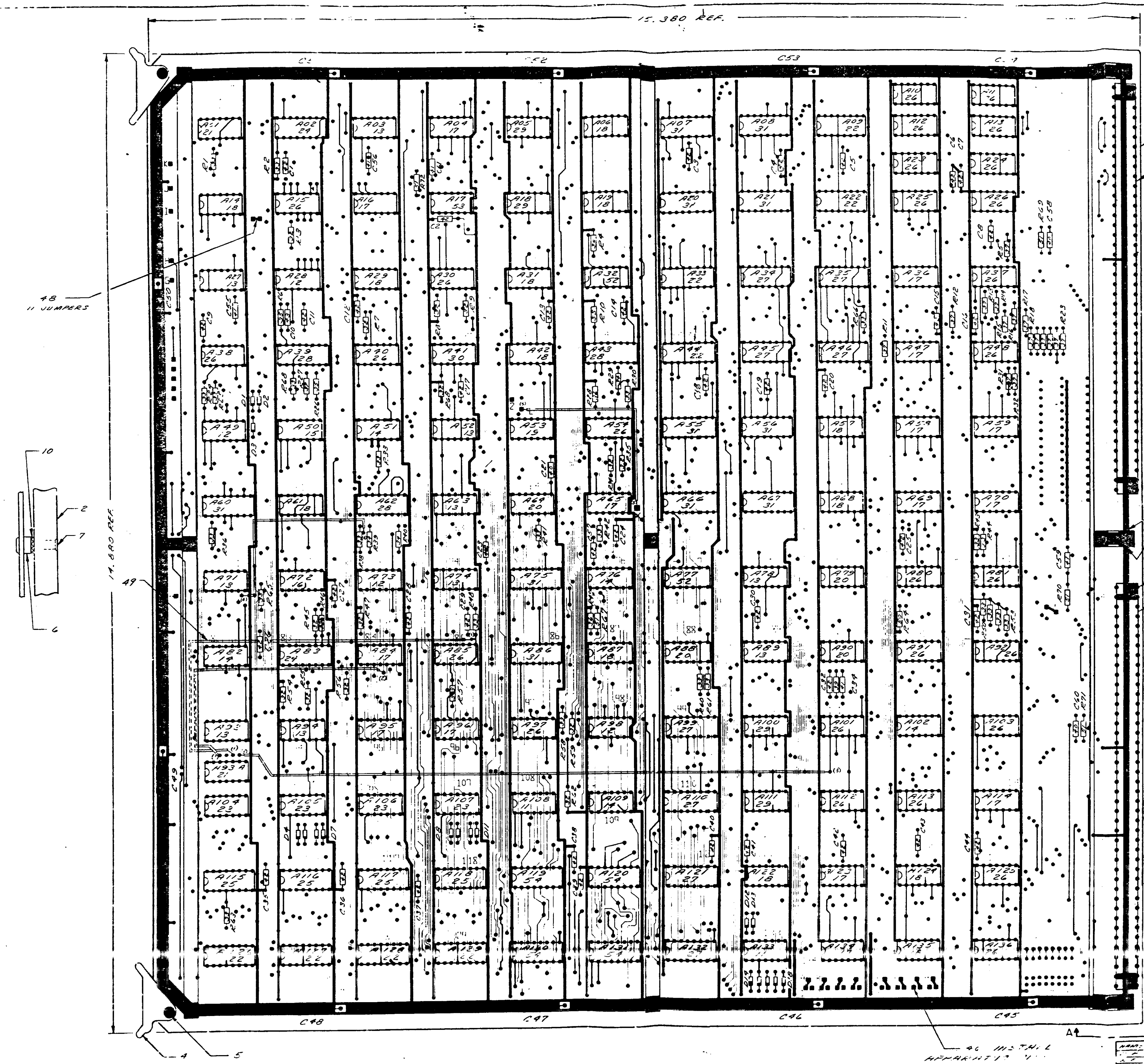
DWG. NO. 35-448 C08

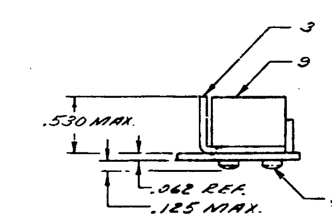
SHEET 1 OF 1

RELEASED FOR PRODUCTION

MFG. ENG. DATE

REVISIONS
ADDED R72 & C61
ADDED STRAPS 1 & 13. REVISE TO REFLECT ROE COPPER
ADDED: STRAPS 4 & 5
R10 WAS ITEM 34, R27 WAS ITEM 32





PARTIAL VIEW A-A

NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE ITEM 44.
2. STIFFENER BAR (ITEM 3) TO BE SOLDERED TO GROUND BUS AT 2 END POINTS AND CENTER POINT.
3. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

COMPONENT	REF. DESIGNATION
CAPACITOR	C1-21 & 23-60
RESISTOR	R1-36, 38-65 & 67-71
DIODE	D1 THRU D15
IC	A01 THRU A136 & 93A

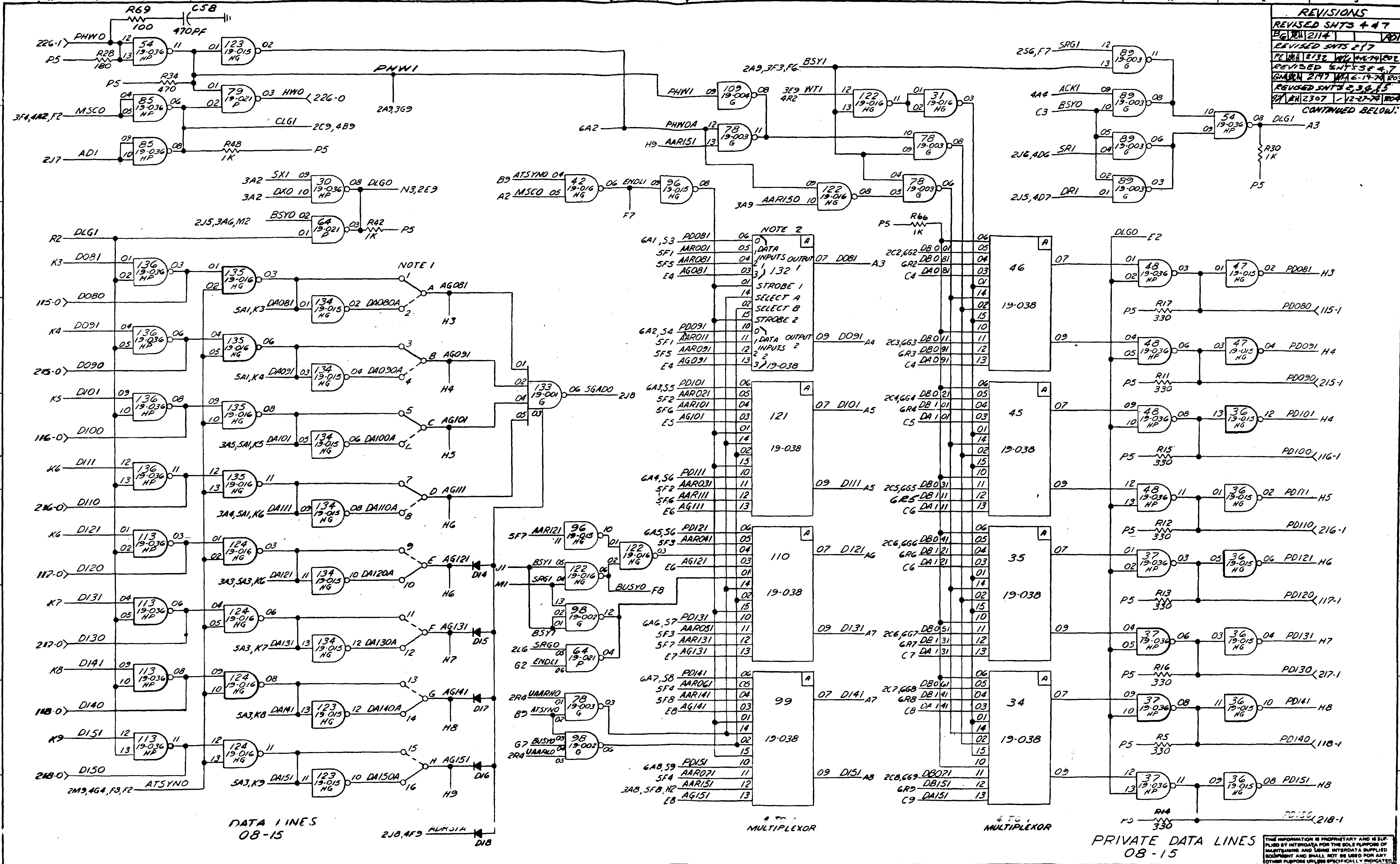
LAST STRAP NO. 15 (5)

SCALE 2:1

ASSEMBLY

CHANNEL

INTERDATA



REVISIONS
REVISED SHTS 4 & 7
2114
REVISED SHTS 2 & 7
2132
REVISED SHTS 3 & 4, 7
2197
REVISED SHTS 2, 3, 4, 5
2307
CONTINUED BELOW:

REVISED SHT. 3
2220 - 5-26-76

NOTES 1. PREFERRED ADDRESS X'F0'
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 M02 SELECTOR CHANNEL.

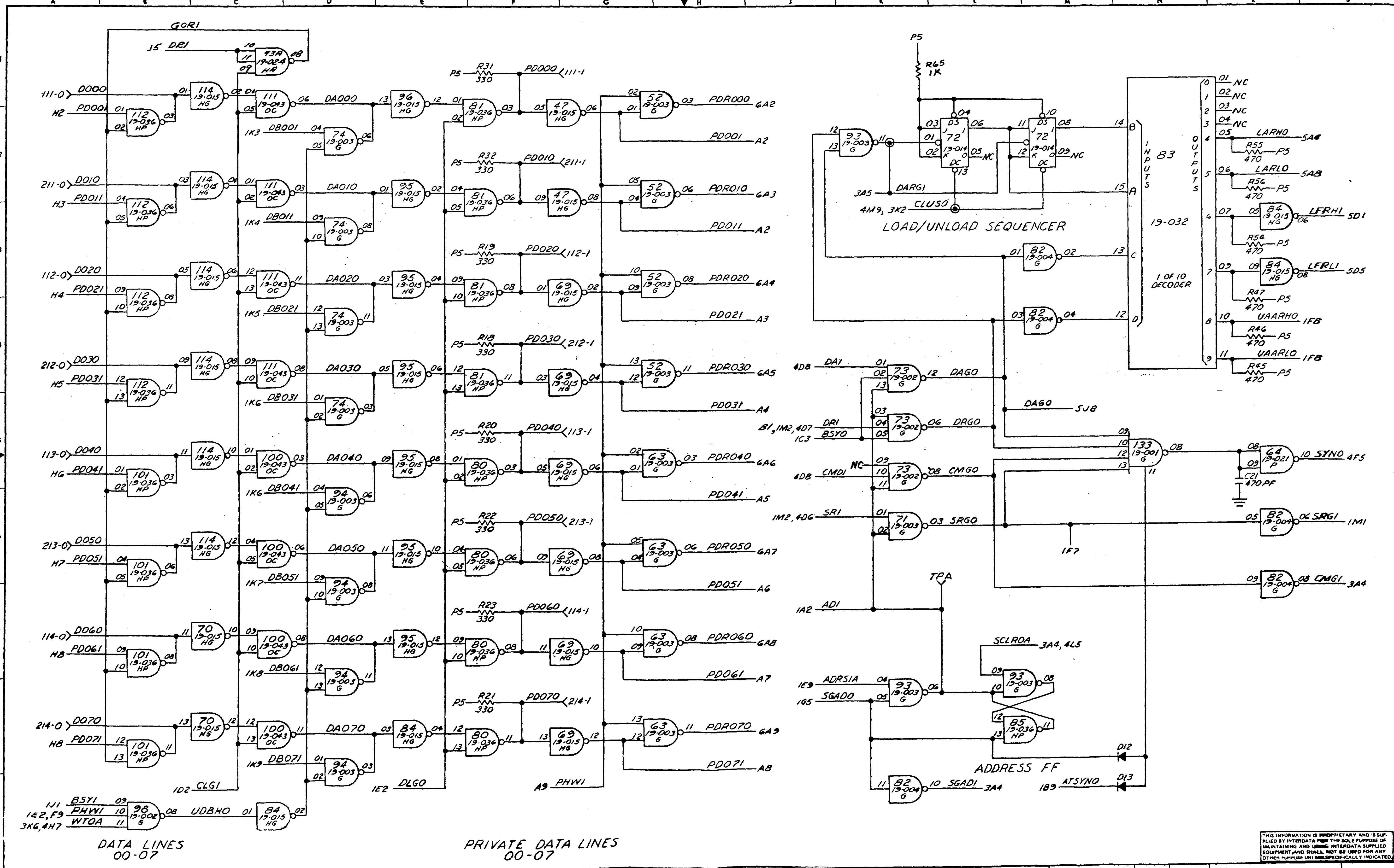
SHEET INDEX	SHEET	1	2	3	4	5	6	7
	REV NO.	5	3	4	3	2	1	8

REVISION LEVEL OF SHEET 1 IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

NAME	TITLE	DATE
W. ZILLGER	DRAFT	10-5-71
R. CERO	CHK	2-6-73
D. FRANKENBERGER	ENGR	2-7-73
N. MASI	SYS TST	2-7-73
R.E. JONES	DIR ENG	

TITLE: NS SELECTOR CHANNEL

03075 — 02-232M08D08 — SHEET 1 OF 7



NOTES

ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 MOZ SELECTOR CHANNEL.

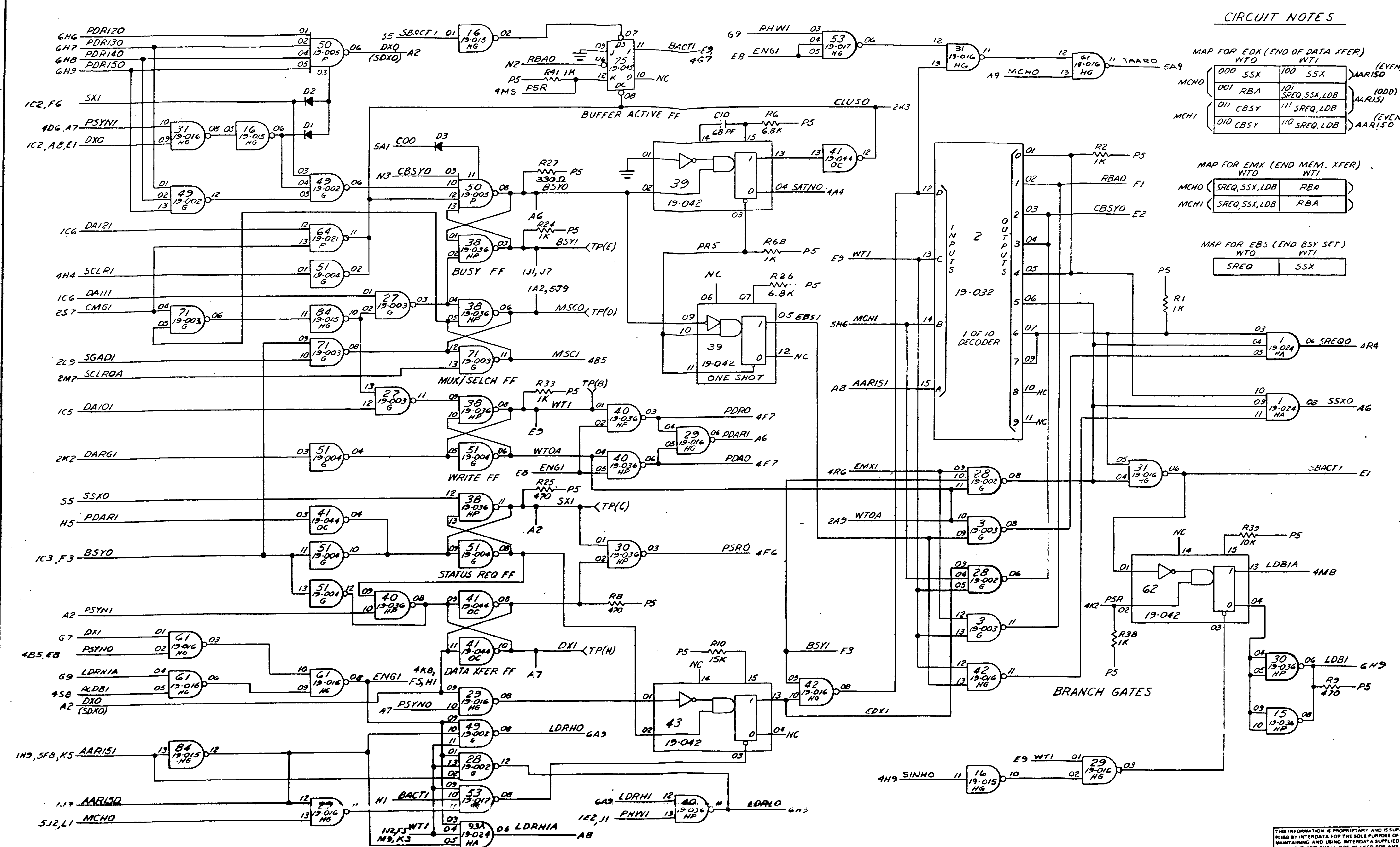
AREA K5 DELETED 'SELO'; TO A73-09	2307	2-27-79	R03
AREA B1: ADDED, 93A. AREA A8: A101-13, DLG1, WAS CONN TO DLG1 @ 1A3	2132	4-16-74	R02
AREAN2, A... WERE REVERSE			

NAME		TITLE	DATE
W ZILLGER		DRAFT	10-5-71
		CHK	
		ENGR	
		DIR ENG	

TITLE NS SELECTOR CHANNEL

03075 — 02-232M...D08 — SHEET 2-7

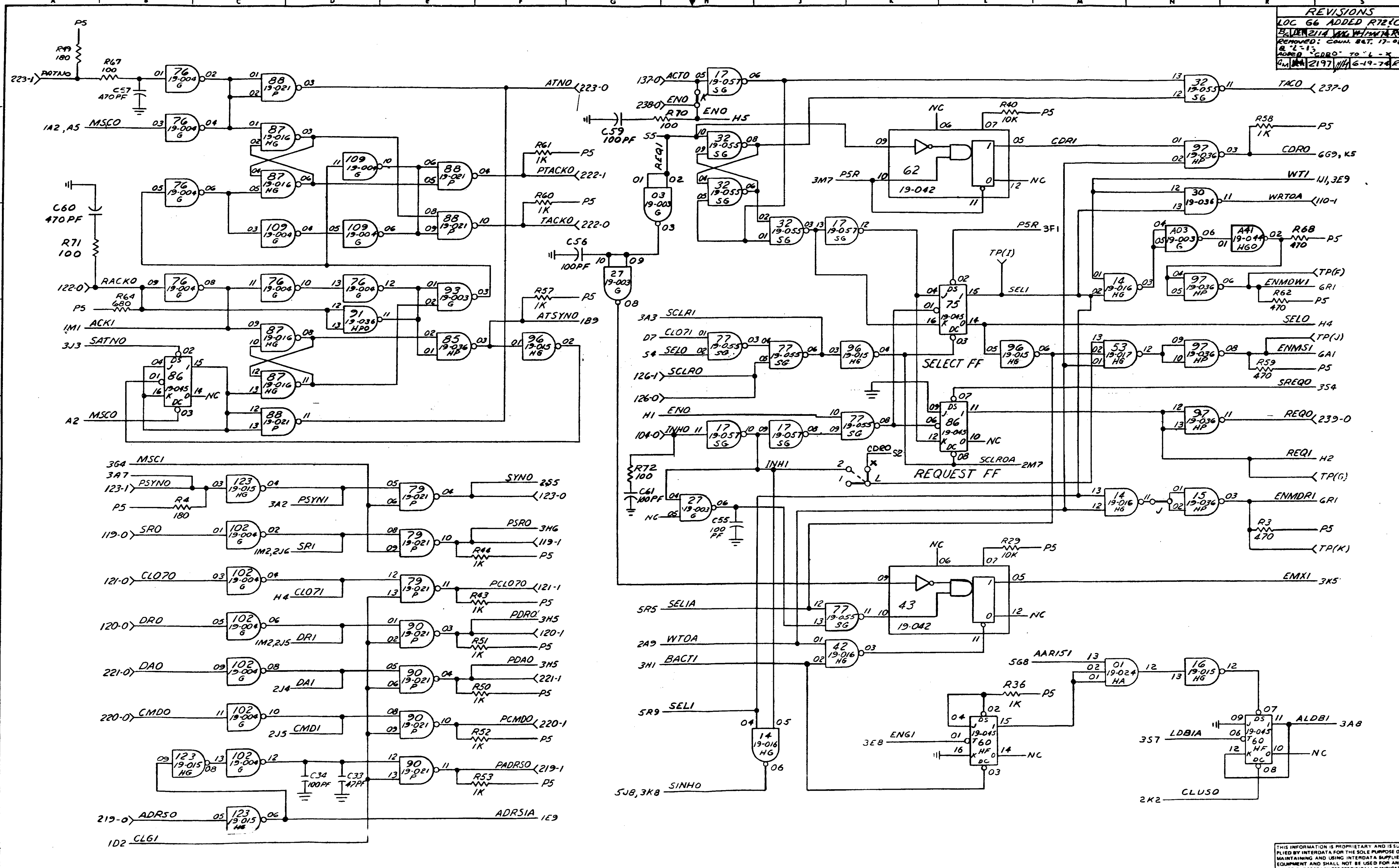
INTERDATA



NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 M02 SELECTOR CHANNEL.

REVISIONS
CHANGED: LEAD FROM 71-05 TO 71-11 WAS FROM 71-05 TO 71-09
AREA F3: VALUE OF R27 WAS 470Ω. AREA H7: VALUE OF R10 WAS 10K
AREA J9, EBS1 NOT ...
E307 12-27-79 R03
2197 6-19-74 R02
2224 5-26-76 R04

NAME	TITLE	DATE	TITLE
W ZILLGER	DRAFT		NS SELECTOR CHANNEL
	CHK		03075
	ENGR		02-232M08D08
	DIR ENG		SHEET 3-7



NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 M02 SELECTOR CHANNEL.

REVISIONS
AREA H4, DELETED CORR. 2J5 FROM SELO
2307 1-20-75

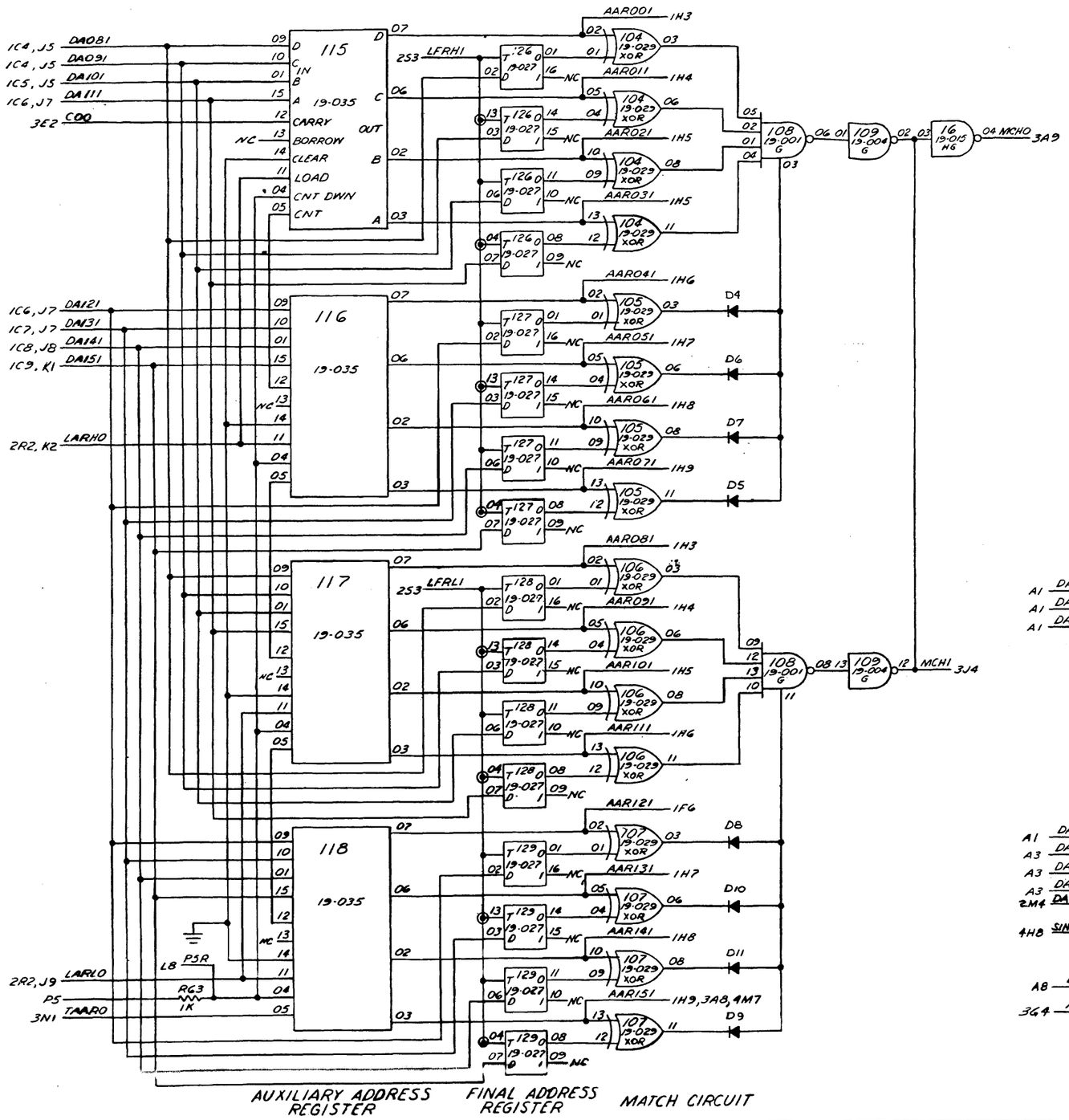
NAME	TITLE	DATE
W. ZIELGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: NS SELECTOR CHANNEL

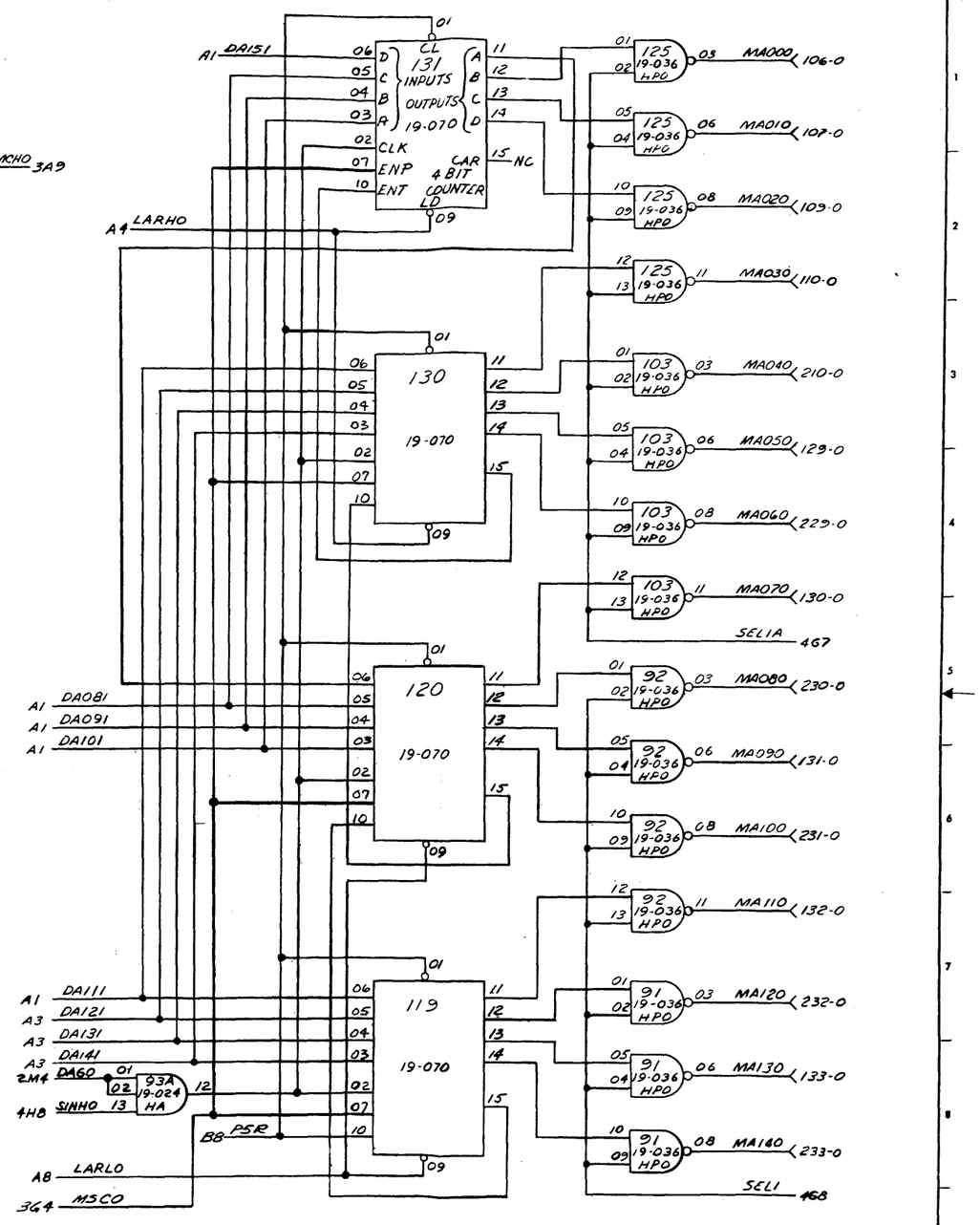
03075
02-232M01 D08

SHEET 4 OF 7

INTERDATA



AUXILIARY ADDRESS REGISTER FINAL ADDRESS REGISTER MATCH CIRCUIT



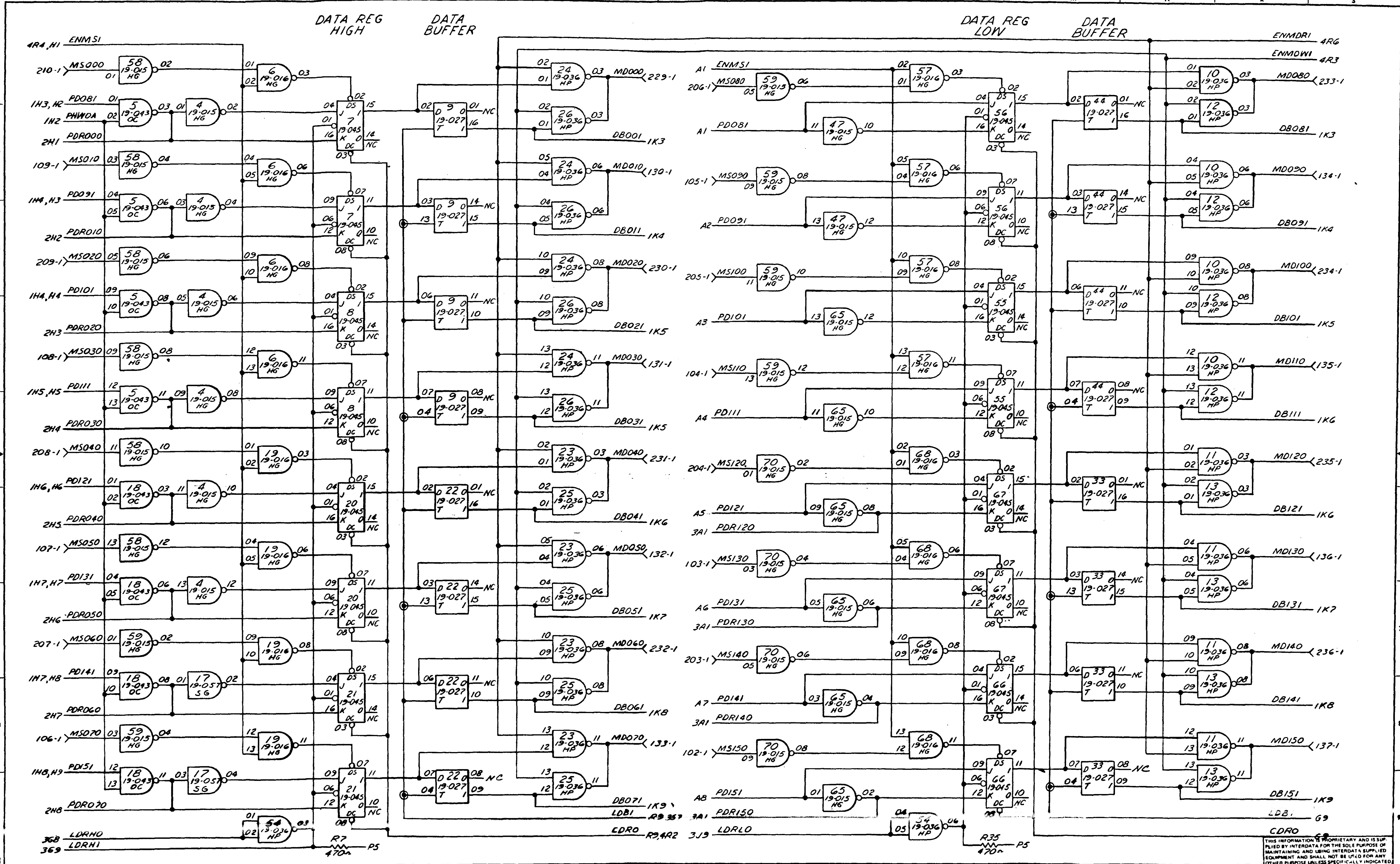
ADDRESS REGISTER

NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 MO2 SELECTOR CHANNEL.

REVISIONS
AREA MI, DESIG. WAS PNL TO R, PINS TO B, PIN 9 TO C, PINS TO D, PIN 7 TO ENT, 5 PIN 10 TO ENP.
MW 2307 L 12-27-74 E02

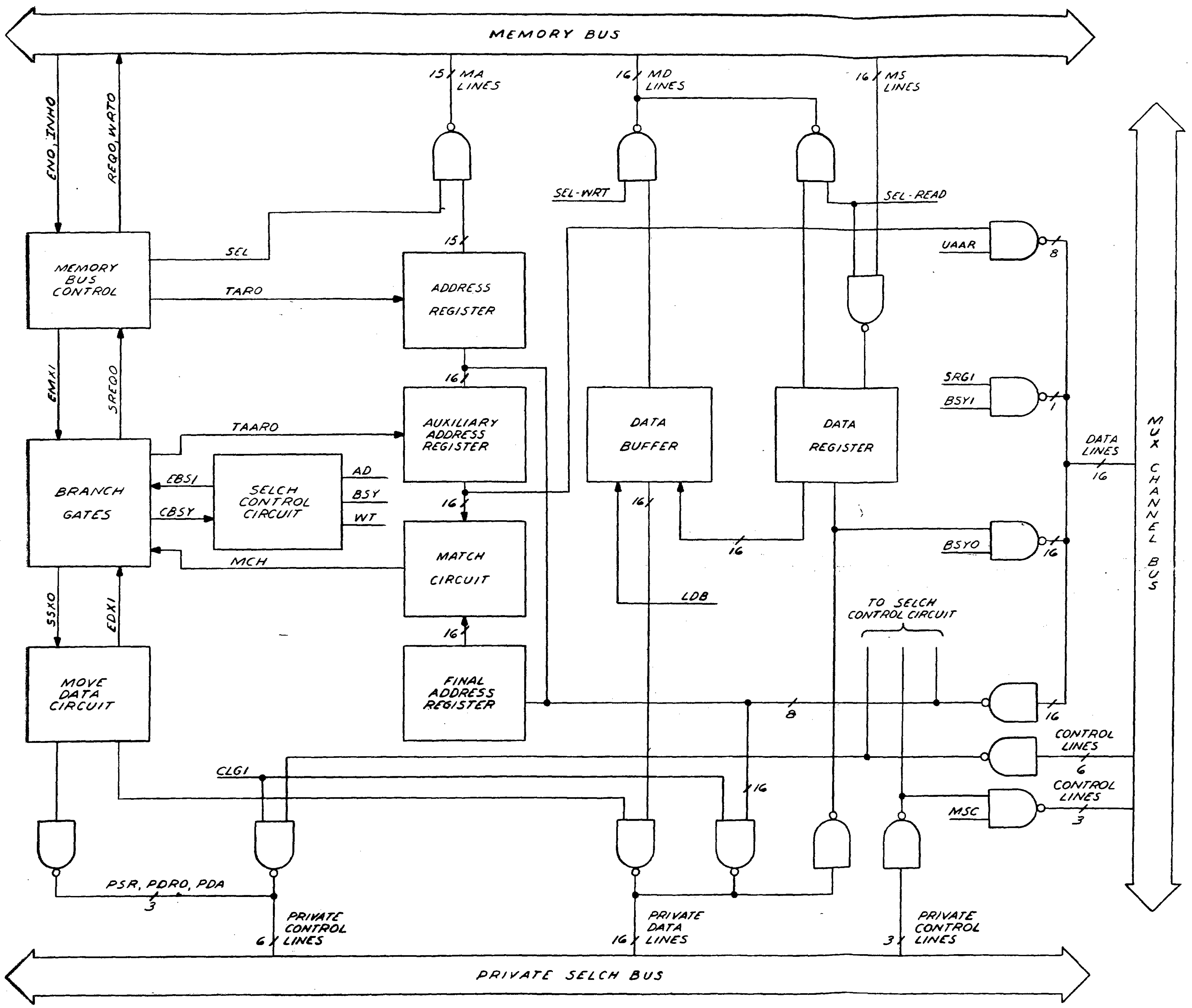
NAME	TITLE	DATE	TITLE
W. ZIELGER	DRAFT	10-5-71	SELECTOR CHANNEL
	CHK		
	ENGR		
	MR ENG		DWG NO 03095 SHT 5-7
			DWG NO 02-232MO1/R2008

INTERDATA®



NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 M02 SELECTOR CHANNEL.

NAME	TITLE	DATE	TITLE
W. ZIELGER	DRAFT.	10-5-71	NS SELECTOR CHANNEL
	CHK		03075
	ENGR		02-232M01R01D08
	DIR ENG		SHEET 6-7



BACK PANEL PIN INDEX			
MNEM	LOC.	MNEM.	LOC.
ACTO	4H1	MD130	6R6
ADRSO	4B8	MD140	6R7
ATNO	4F1	MD150	6R8
CLO70	4B6	MS000	6A1
CMDO	4B3	MS010	6A2
D000	2A1	MS020	6A3
D010	2A2	MS030	6A4
D020	2A3	MS040	6A5
D030	2A4	MS050	6A6
D040	2A5	MS060	6A7
D050	2A6	MS070	6A8
D060	2A7	MS080	6H1
D070	2A8	MS090	6H2
D080	1A3	MS100	6H3
D090	1A4	MS110	6H4
D100	1A5	MS120	6H5
D110	1A6	MS130	6H6
D120	1A6	MS140	6H7
D130	1A7	MS150	6H8
D140	1A8	PADRSO	4F8
D150	1A8	PATNO	4B1
DAO	4B7	PCLO70	4F6
DRO	4B7	PCMDO	4F8
ENO	4H1	PD000	2F1
HWO	1D1	PD010	2F2
INHO	4H5	PD020	2F3
MA000	5R1	PD030	2F4
MA010	5R1	PD040	2F5
MA020	5R2	PD050	2F6
MA030	5R2	PD060	2F7
MA040	5R3	PD070	2F8
MA050	5R3	PD080	1R4
MA060	5R4	PD090	1R4
MA070	5R4	PD100	1R5
MA080	5R5	PD110	1R6
MA090	5R6	PD120	1R7
MA100	5R6	PD130	1R7
MA110	5R7	PD140	1R8
MA120	5R7	PD150	1R9
MA130	5R8	PDAO	4F7
MA140	5R8	PDRO	4F8
MD000	6G1	PHWO	1A1
MD010	6G2	PSRO	4F6
MD020	6G3	PSYNO	4B5
MD030	6G4	PTACKO	4F2
MD040	6G5	RACKO	4B3
MD050	6G6	REQO	4R5
MD060	6G7	SCLRO	4H4
MD070	6G8	SRO	4B6
MD080	6R1	SYNO	4F5
MD090	6R2	TACKO	4H3
MD100	6R3	TACO	4R1
MD110	6R4	WRTOA	4R3
MD120	6R5		

BACK PANEL MAP			
ROW 1	ROW 2	TERM NO.	CONN
P5	GND	41	
GND	GND	40	
		39	
		38	
MD150		37	
MD130	MD140	36	
MD110	M120	35	
MD090	MD100	34	
MD070	MD080	33	
MD050	MD060	32	
MD030	MD040	31	
MD010	MD020	30	
	MD000	29	
		28	
		27	
SCLRO	PHWO	26	
		25	
		24	
PSYNO	PATNO	23	
	PTACK.)	22	
PCLO70	PDAO	21	
PDRO	PCMDO	20	1
PSRO	PADRSO	19	
PD140	PD150	18	
PD120	PD130	17	
PD100	PD110	16	
PD080	PD090	15	
PD060	PD070	14	
PD040	PD050	13	
PD020	PD030	12	
PD000	PD010	11	
WRTOA	MS000	10	
MS010	MS020	09	
MS030	MS040	08	
MS050	MS060	07	
MS070	MS080	06	
MS090	MS100	05	
MS110	MS120	04	
MS130	MS140	03	
MS150		02	
GND	GND.	01	
P5	GND	00	
P5	GND	41	
GND	GND	40	
	REQO	39	
	ENO	38	
ATCO	TACO	37	
		36	
		35	
		34	
MA130	MA140	33	
MA110	MA120	32	
MA090	MA100	31	
MA070	MA080	30	
MA050	MA060	29	
		28	
		27	
SCLRO	HWO	26	
		25	
		24	
SYNO	ATNO	23	
RACKO	TACKO	22	
CLO70	DAO	21	
DRO	CMDO	20	0
SRO	ADRSO	19	
D140	D150	18	
D120	D130	17	
D100	D110	16	
D080	D090	15	
D060	D070	14	
D040	D050	13	
D020	D030	12	
D000	D010	11	
MA030	MA040	10	
MA020		09	
		08	
MA010		07	
MA000		06	
		05	
INHO		04	
		03	
		02	
GND	GND	01	
P5	P5	00	

TEST POINT INDEX		
DESIG	MNEM	LOC.
A	ADI	2L6
B	WTI	3G5
C	SXI	3G6
D	MSCO	3G4
E	BSYO	3G3
F	ENMDWI	4S3
G	REQI	4S5
H	DXI	3G7
I	SELI	4L3
J	ENMSI	4S4
K	ENMDRI	4S6

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION	
NS SELCH	35-391M02R03

NOTES

REVISIONS
IN SUPP INFO 35-392 M02 WAS R00
- | REH | 2114 | | 3/14/74 | R01
IN SUPP INFO 35-392M02 WAS R01
R2 | | 2132 | | 4-16-74 | R02
NEW M9 = 281 LEV OF 35-391 M02 WAS R02
| | 2197 | | 6/22/74 | R03

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-13-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: NS SELECTOR CHANNEL

TASK NO. 03075
DWG NO. 02-232M01R03D08
SHEET OF 7 - 7

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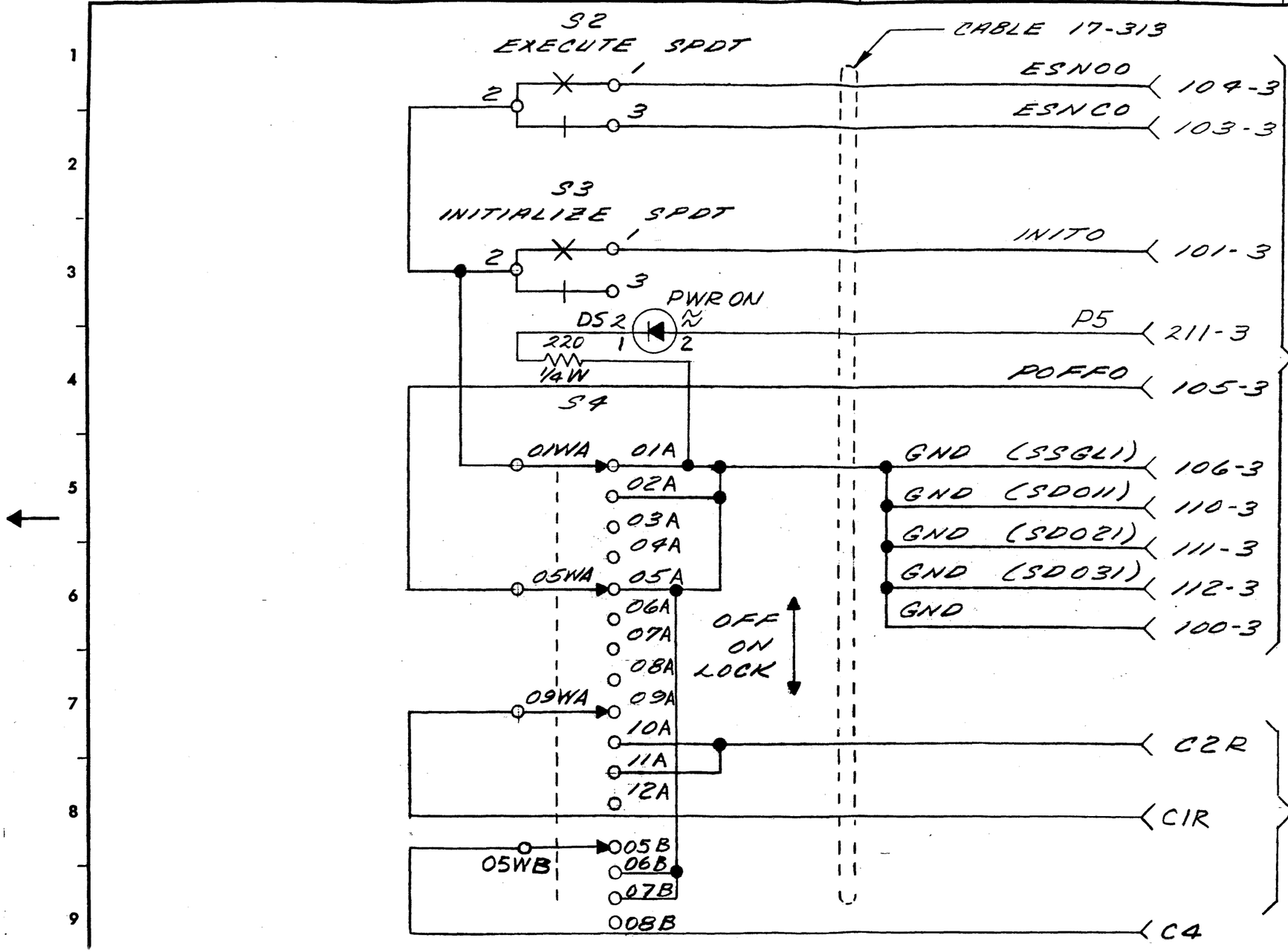
GP	80	3330	10-20-77	R01



NOTES

NAME	TITLE	DATE
R F CERO	DRAFT	3-15-74
R F CERO	CHK	3-29-74
G JOYCE	ENGR	4-5-74
D BOPP	Q.C	4-5-74
P ABITANTE	MGR	4-7-74

TITLE FUNCTIONAL SCHEMATIC
TURN KEY CONSOLE
(MODEL 7/16)

TASK NO. 03095
SHEET OF 1 - 1
DWG. NO. 02-351 R01 B08

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