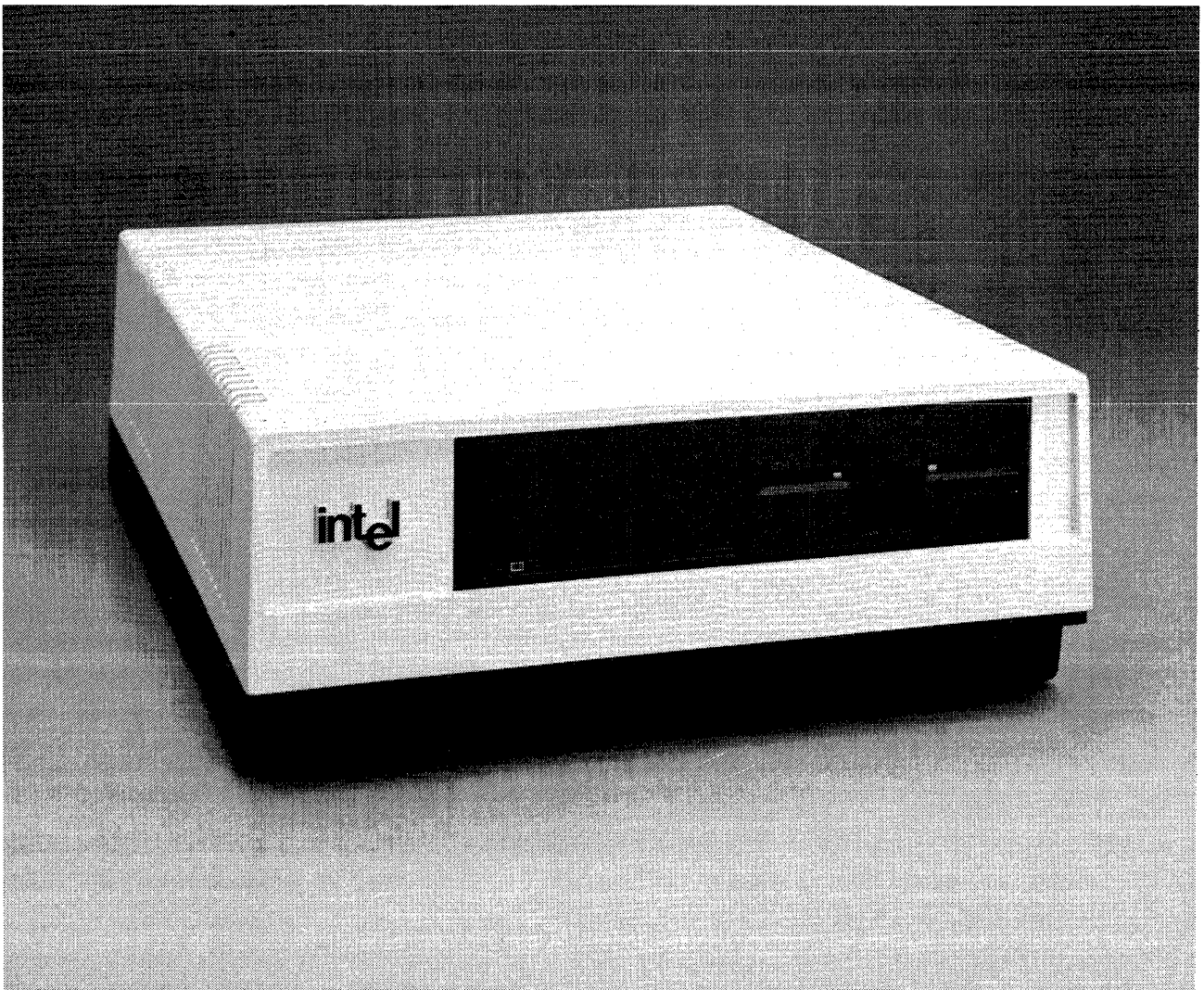




SYSTEM 310

PROCESSOR CONFIGURATION GUIDE:

iSBC® 86/30 SINGLE BOARD COMPUTER



SYSTEM 310
PROCESSOR CONFIGURATION GUIDE:
iSBC® 86/30 SINGLE BOARD COMPUTER

Order Number: 173205-001

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CAUTION

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class A Computing Device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Intel uses an iSBC[®] 86/30 Single Board Computer as the processor board in 86-based System 310's. While you can buy this board from Intel separately, it is not configured for the System 310. Intel makes certain component and jumper changes to this off-the-shelf board.

This manual explains the differences between the iSBC 86/30 Single Board Computer you buy off-the-shelf and the 86/30 processor board used in the System 310 so you can configure your own board or verify the configuration of the processor board in your preconfigured System 310.

Read this manual when you need to add or remove an expansion board, or change a jumper-controlled function on the processor board. Information is aimed at the both the hardware system designer and the technician. This manual explains not only why and when it is necessary to change a parameter on the processor board, but how to perform the change.

THE CHAPTERS AT A GLANCE

Chapter 1 - Features of the Processor Board

Lists the features provided by the processor board. Describes the expansion boards for each System 310 configuration and the features they add to the processor.

Chapter 2 - Components and Jumpers on the Processor Board

Illustrates and explains differences between the components and jumpers used on the off-the-shelf 86/30 processor board and those used on the System 310's 86/30 processor board.

Chapter 3 - Removing and Installing the Processor Board

Provides step-by-step instructions for removing and installing the iSBC 86/30 Single Board Computer in the System 310 chassis.

Chapter 4 - Adding the 304 RAM Board

Provides step-by-step instructions for mounting the iSBC 304 RAM Expansion MULTIMODULE™ board on the processor board.

Chapter 5 - Adding the 337 Math Board

Provides step-by-step instructions for mounting the iSBC 337 MULTIMODULE Numeric Data Processor on the processor board. Includes jumper changes to both boards.

Appendix A - Serial and Parallel Connector Pinouts

Describes the signal path between the processor board and the back panel for the parallel and serial I/O cables.

Appendix B - Uploading and Downloading

Provides step-by-step instructions for transferring files between an Intel development system running the ISIS-II operating system and an 86-based System 310 running the iRMX™ 86 operating system.

Appendix C - Operating Specifications

Lists the electrical, mechanical, and environmental requirements of the 86/30 processor board in the System 310.

RELATED PUBLICATIONS

The following manuals contain detailed information about the products discussed in this manual. You can order copies by contacting the Intel Literature Department at the address listed on page ii of this manual.

iSBC 86/14 and iSBC 86/30 Single Board Computer Hardware Reference Manual, Order Number 144044

System 310 Memory Configuration Guide: 86-Based Systems, Order Number 173206

System 310 Memory Configuration Guide: 286-Based Systems, Order Number 173443

System 310 Hardware Integration Guide, Order Number 173203

iSBC 337 MULTIMODULE Numeric Data Processor Hardware Reference Manual, Order Number 142887

iSXM™ 101 XENIX 86 Extension Module Installation Guide*, Order Number 173077

iSXM 951 Terminal Communications Installation Guide for System 310 Microcomputers, Order Number 173074

Guide to Installing and Using the iSBX™ 218A Flexible Diskette Controller Board, Order Number 145911

User's Guide for the iSBC 957B iAPX 86, 88 Interface and Execution Package, Order Number 143979

System 310 Disk Configuration Guide, Order Number 173207

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System 310 Publications Guide, Order Number 173441

*iRMX 86 Release 5 Operator's Manual for System 86/300 Series
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For information on running system confidence tests, refer to:

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CHAPTER 1 FEATURES OF THE PROCESSOR BOARD

This chapter explains how the System 310 uses the iSBC® 86/30 Single Board Computer (the processor board). It outlines the operating features of the board and explains which expansion boards you can add to the processor board. Expansion boards are either MULTIMODULE™ boards, boards with iSBX™ connectors (iSBX boards), or iSXM™ boards.

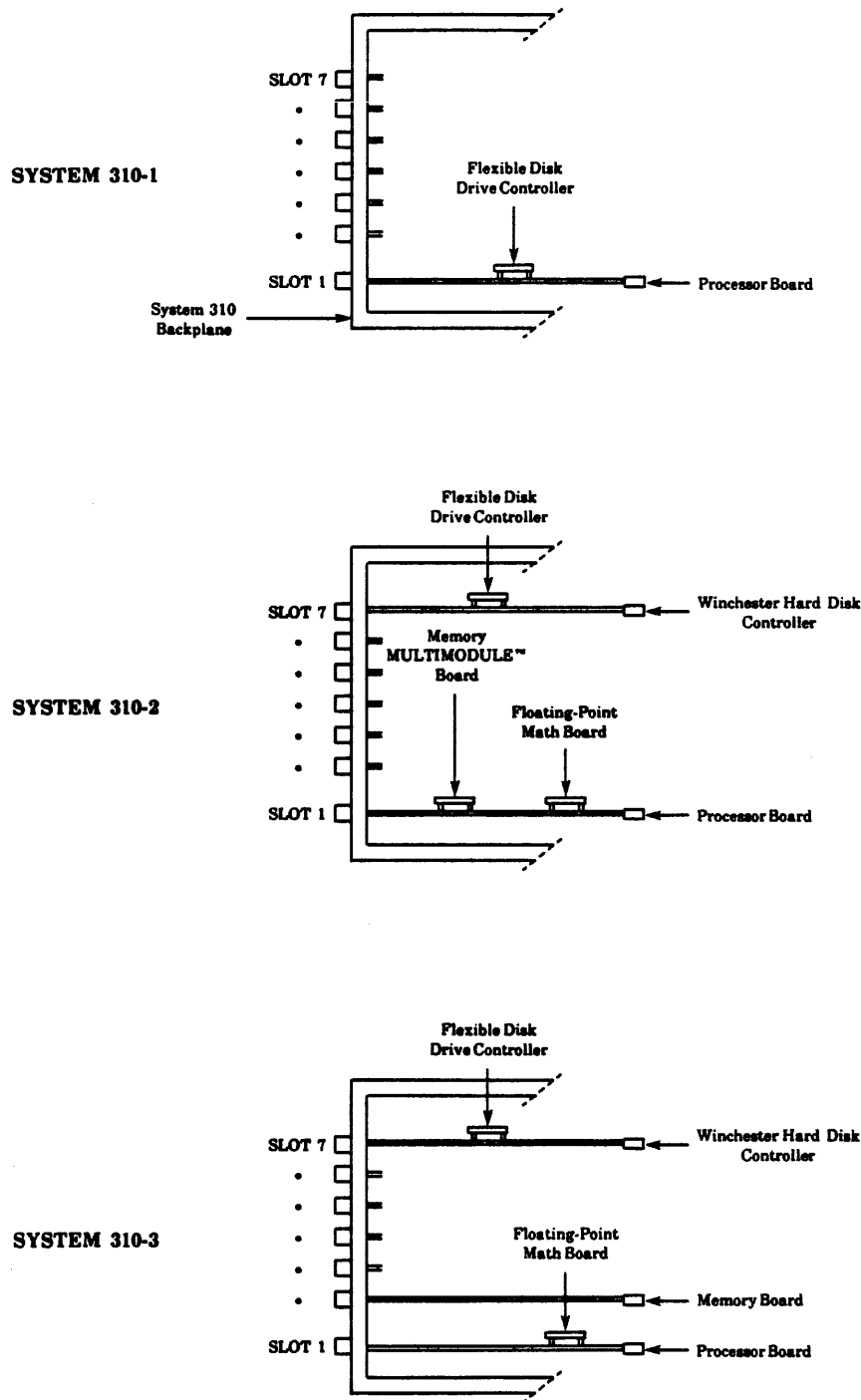
OVERVIEW OF PROCESSOR BOARD FEATURES

All 86-based System 310's use the iSBC 86/30 Single Board Computer as their processor board. This processor board, in turn, uses an 8086 microprocessor (CPU) to run software and to control communication between boards according to the MULTIBUS® (IEEE 796) interface standard. The major features of this processor board are listed below.

- Selectable clock rate
- Memory:
 - 128K bytes of on-board dual-port RAM (expandable)
 - Firmware for initializing and booting the system and various peripherals; also contains the system confidence test programs and monitor
 - Direct addressing for up to 1 megabyte of memory
- Input/Output:
 - 1 RS-232 serial I/O port for a video display terminal
 - 1 parallel port for a Centronics*-type printer
 - 2 system bus expansion (iSBX) connectors
 - Timers for controlling the time-of-day clock and baud rate
- Support for expansion boards that add:
 - On-board memory
 - Memory management
 - Diskette drive control
 - Floating-point math

Intel preconfigures three versions of the System 310 that use the 86/30 processor board: 310-1, 310-2, and 310-3. These three configurations contain the expansion boards shown in Figure 1-1. This figure shows a cross section of each cardcage with the expansion boards mounted piggyback on either the processor board or the Winchester hard disk controller board.

*Centronics is a trademark of Centronics Data Computer Corporation.



F-0086

Figure 1-1. Cross Section of Three Preconfigured Systems

CLOCK RATE

You can select one of two clock rates for the central processing unit (CPU) on the 86/30 processor Board Computer: either 5 or 8 MHz. The factory ships the 86-based System 310's with 5 MHz selected. This is to meet the requirements of the 8087 math coprocessor included in Systems 310-2 and 310-3. This coprocessor is found on several System 310-compatible boards such as the 337 math MULTIMODULE board and the iSXM 101 memory management board. You can select 8 MHz by changing the jumper setting listed in Chapter 2.

MEMORY ON THE PROCESSOR BOARD

The System 310 requires RAM at 00000H for the bootstrap loading program and the status/error register (containing the parity error flag). The factory sets up systems so that the processor board's memory is always located from 00000H through 1FFFFH.

Besides the on-board RAM, the processor board contains system firmware in PROMs. This firmware is located from F8000H through FFFFFH. The PROMs contain the iSDM 86 debug monitor program, the system confidence test programs (SCTs), and the bootstrap program for loading the operating system and booting the drives.

Intel produces two sets of PROMs for the System 310. One set boots the 5¼-inch flexible diskette drive found in the System 310-1. The other set boots both the 5¼-inch flexible diskette drive and the 5¼-inch Winchester hard disk drive found in the Systems 310-2 and 310-3. You will need a replacement set of PROMs if you change your system to or from the System 310-1 configuration.

INPUT/OUTPUT ON THE PROCESSOR BOARD

The processor board communicates with a number of peripherals and expansion boards. To do this, it provides a serial port, a parallel port, and two iSBX connectors. Table 1-1 lists the I/O port address assignments for these connectors. You may need these addresses when writing software routines such as drivers.

Serial Port

System 310 firmware, using the 8251A PCI (Programmable Communications Interface), determines the serial port operating characteristics such as baud rate and protocol. The 86-based preconfigured systems provide one RS-232 serial port for peripherals and presets its data transfer rate at 9600 baud.

Many customers use the serial port for a video display terminal and keyboard. Because many serial terminals use the RS-232 protocol, the factory connects two signal lines on the System 310's processor board, Clear To Send (CTS) and Request To Send (RTS), to provide the most common configuration for RS-232 video display terminals.

Refer to Chapter 2 in this manual for jumper information if your peripheral uses different signals. Appendix A lists the pinout for the serial port connector on the System 310 back panel.

Table 1-1. I/O Address Assignments

| Address | Function |
|---------------|--|
| 008(even)*H | MCS0 ¹ for iSBX connector J4†. Low byte of a 16-bit transfer. |
| 008(odd)H | MCS1 for iSBX connector J4. High byte of a 16-bit transfer. |
| 009(even)H | MCS1 for iSBX connector J4. 8-bit transfers. |
| 009(odd)H | Not used. |
| 00A(even)H | MCS0 for iSBX connector J3. Low byte of a 16-bit transfer. |
| 00A(odd)H | MCS1 for iSBX connector J3. High byte of a 16-bit transfer. |
| 00B(even)H | MCS1 for iSBX connector J3. 8-bit transfers. |
| 00B(odd)H | Not used. |
| 00C0 or 00C4H | Reads: Status and Polls the 8259A PIC ² . Writes: ICW1 ³ , OCW2 ⁴ , and OCW3 of the 8259A. |
| 00C2 or 00C6H | Reads: OCW1 for the 8259A. Writes: ICW2, ICW3, ICW4, and OCW1 of the 8259A. |
| 00C8H | Port A of the 8255A PPI ⁵ . |
| 00CAH | Port B of the 8255A. |
| 00CCH | Port C of the 8255A. |
| 00CEH | Control Word for the 8255A. |
| 00D0H | Counter 0 of the 8253 PIT ⁶ . |
| 00D2H | Counter 1 of the 8253. |
| 00D4H | Counter 2 of the 8253. |
| 00D6H | Control Word for the 8253. |
| 00D8 or 00DCH | Data Word for the 8251A PCI ⁷ . |
| 00DA or 00DEH | Command/Mode Status Word for the 8251A. Reads: Status. Writes: Mode and command. |

¹MCS0 and MCS1 are MULTIMODULE Chip Selects 0 and 1.

²Programmable Interrupt Controller (PIC)

³ICW stands for Initialize Command Word.

⁴OCW stands for Operational Command Word.

⁵Programmable Parallel Interface (PPI)

⁶Programmable Interval Timer (PIT)

⁷Programmable Communications Interface (PCI)

*The words (even) and (odd) represent an even- and odd-numbered hex digit.

†J4 and J3 are iSBX connectors on the processor board.

Parallel Port

The System 310 firmware also controls the parallel port using the 8255A PPI (Programmable Peripheral Interface). Parallel ports are preconfigured with a Centronics-type printer interface. This interface consists of several jumpers and the printer scrambler board mounted on the inside of the back panel. Refer to Chapter 2 in this manual when you need to change the parallel port protocol, and Appendix A for the pinout of the parallel connector on the System 310 back panel.

In addition, you can use the parallel port to transfer files between Intel development systems and the System 310. Refer to Appendix B, Uploading and Downloading, for operating instructions and a list of the necessary equipment and jumper changes.

iSBX™ Connectors

You can install iSBX expansion boards by plugging them into iSBX connectors (J3 and J4 on the 86/30 processor board) and changing the appropriate jumpers. For example, the iSBX 218A Flexible Diskette Controller plugs into J4 in the System 310-1. In fact, you can install iSBX boards into any host board containing iSBX connectors. Table 1-1 lists the connector names and functions on the processor board, and their corresponding port addresses so your software can communicate to the expansion boards.

Timers

The processor board provides an 8253 PIT (Peripheral Interface Timer). The iRMX™ 86 and XENIX* 86 operating systems use the timer for the time-of-day clock and baud rate generation. The manuals for these software products describe the ways you can use timers.

ADDING FEATURES WITH EXPANSION BOARDS

This section describes the expansion boards and the way they enhance the processor board. Expansion boards are either MULTIMODULE boards, iSXM boards, or iSBX boards. Refer back to Figure 1-1 for a diagram of each System 310 configuration and the expansion boards it uses.

ADDING MEMORY

The System 310-2 includes the iSBC 304 RAM Expansion MULTIMODULE Board for users who need more memory than the System 310-1 provides. Since the RAM board attaches to the processor board, over the existing RAM area, it does not consume an extra card slot in the chassis.

*XENIX is a trademark of Microsoft Corporation.

If you have a System 310-1 and want to upgrade memory to the size found in the 310-2, you can add this MULTIMODULE board yourself. Chapter 4 explains how to change jumper settings so no gaps occur in the address space between the processor and the expansion board. Chapter 4 also explains how to install the 304 board on the processor board.

Unlike the Systems 310-1 and 310-2, System 310-3 memory is constructed differently. It contains the iSBC 012B memory board instead of the 304 RAM MULTIMODULE board. Again, you can add the 012B memory board yourself. For more information about memory, refer to the *System 310 Memory Configuration Guide: 86-Based Systems*.

ADDING MEMORY MANAGEMENT FOR XENIX* SYSTEMS

The XENIX operating system needs memory management. While the preconfigured System 310's do not supply memory management boards, there are two System 310-compatible boards you can add: the iSXM 101 XENIX 86 Extension Module and the iSBC 309 Memory Management Board.

Both boards provide memory management and space for the 8087 math coprocessor. Each board attaches directly to the 86/30 processor board. For installation and jumpering information, refer to the reference manuals for these products (listed in the Preface).

ADDING DRIVE CONTROL

All preconfigured versions of the System 310 include a 5¼-inch, 318K-byte flexible diskette drive. The controller for this drive, the iSBX 218A Flexible Diskette Controller, is a MULTIMODULE board that fastens onto either the processor board (as in the 310-1) or onto the iSBC 215 Generic Winchester Disk Controller (as in the 310-2 and 310-3).

Refer to the *System 310 Disk Configuration Guide* for configuration and installation instructions.

ADDING FLOATING-POINT MATH

The System 310 performs floating-point math with the 8087 math coprocessor. Systems 310-2 and 310-3 include the iSBC 337 MULTIMODULE Numeric Data Processor (the math board) for this purpose. When jumpering and installing the 337 math board, refer to the instructions in Chapter 5 of this manual.

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If your System 310 uses the XENIX 86 operating system, you can install the 8087 coprocessor in the socket provided for that purpose on either of the memory management boards you are using. These boards were discussed earlier in the memory management section of this chapter. XENIX systems add floating-point math this way because a memory management board and a 337 math board will not fit on the processor board at the same time.



CHAPTER 2 COMPONENTS AND JUMPERS ON THE PROCESSOR BOARD

This chapter explains the differences between the components and jumpers on the standard (off-the-shelf) 86/30 processor board and the components and jumpers on the 86/30 processor board used in the System 310.

First, this chapter presents a drawing of the installation sites where components are added to System 310 processor boards. Then it presents a similar drawing showing location of the jumpers installed on all processor boards. The drawing is followed by a table listing the jumper numbers and a brief description of their functions.

The rest of the chapter explains effect these jumper changes have on the operation of the processor board. Later chapters discuss the component and jumper changes required when adding the 304 and 337 expansion boards.

ADDING COMPONENTS

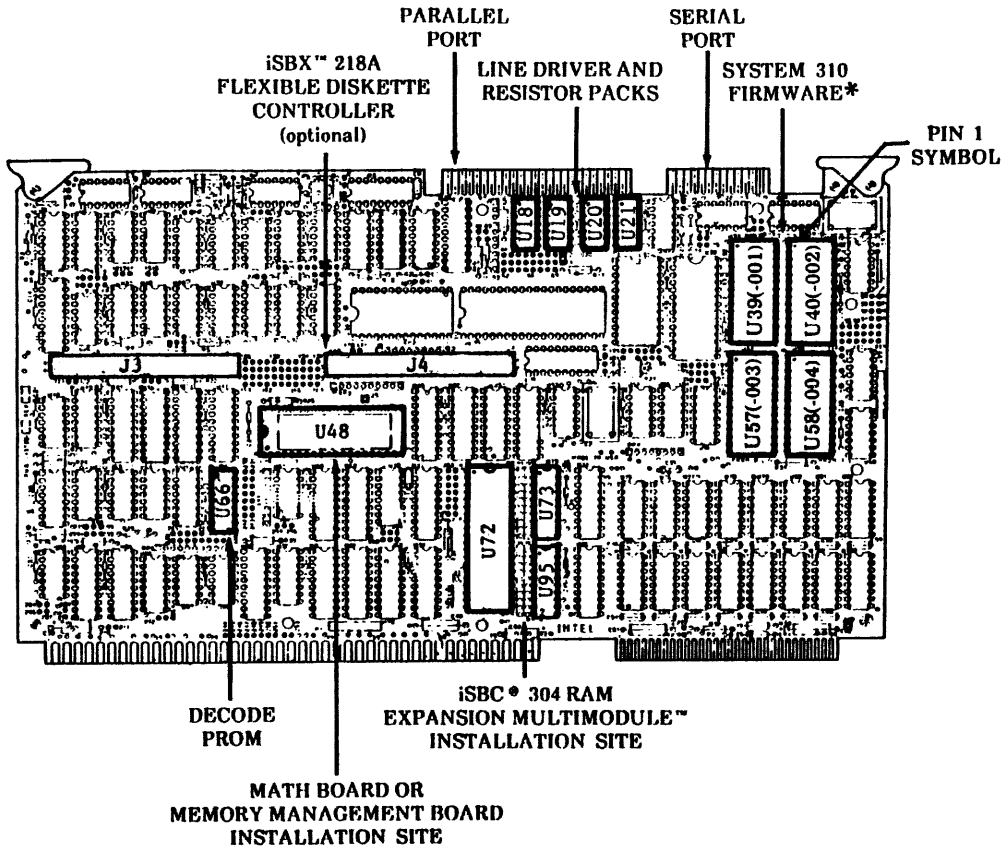
Intel adds several components to the 86/30 processor board so it will work in the 86-based System 310's. The placement of these components is shown in Figure 2-1.

- 3 1K-ohm resistor packs in locations U18, U20, and U21
- 1 line driver (7438) in location U19
- 4 PROMs containing system firmware in locations U39, U40, U57, and U58
- 1 decode PROM in location U66
- 1 8203 dynamic RAM controller in location U72
- 2 74LS373 octal D-type latches in locations U73 and U95

The first two items in the list, the resistors and line driver, help configure the parallel I/O port. The next five components are PROMs containing specific programs and addresses for booting, initializing, and operating the disk drives, and for decoding the addresses of expansion memory. The last two items, the dynamic RAM controller and the latches, are removed and reinstalled on the 304 RAM board in the System 310-2 (described in Chapter 4).

When altering a preconfigured system, be sure that you install the correct PROMs for your new configuration along with required components from the list above. You will need new PROMs in four cases:

1. When you attach the 218A diskette controller to the processor board, install the four PROMs labeled 172879. The System 310-1 is preconfigured with these PROMs. If you do not change PROMs, the software in your flexible diskette drive will not be automatically booted and the SCT will fail.



***NOTE:** Use either PROM set marked 172878-00x or 172879-00x in these locations as directed in text.

Figure 2-1. Location of Added Components

F-0082

2. When you attach the 218A diskette controller to the 215G Winchester hard disk controller, whether or not you are using a Winchester drive in your system, install the four PROMs labeled 172878. Preconfigured Systems 310-2 and 310-3 use these PROMs.
3. When you add a 304 RAM MULTIMODULE board, install the decode PROM labeled 144109-001 in U66, shown in Figure 2-1. System 310-2 is preconfigured with this PROM.
4. When you remove a 304 RAM MULTIMODULE board from the processor board, install the decode PROM labeled 144108-001 in U66. Preconfigured Systems 310-1 and 310-3 use this PROM.

SETTING THE JUMPERS FOR ALL CONFIGURATIONS

In addition to the component changes mentioned in the last section, there are several jumper changes necessary before you can use an off-the-shelf version of the 86/30 processor board in the System 310. These changes fall into two categories: 1) those that are made to all 86/30 processor boards (jumpers common to most boards), and 2) those that are required only when a specific expansion board is used.

Figure 2-2 shows the location of all the connected jumpers in category 1. There is one exception. The RAM size and RAM address jumper settings for the System 310-2 are different. Table 2-1 and the section on changing jumpers in Chapter 4 list these differences.

Table 2-1 lists both the jumpers shown in Figure 2-2 and the board-specific jumpers (category 2). Both kinds of jumper information are merged into a numerically ordered list for easy reference. Any jumper not listed in the table is not connected. Refer to the *iSBC 86/14 and iSBC 86/30 Single Board Computer Hardware Reference Manual* for a complete listing of all the jumpers on the processor board and their functions.

The three columns in Table 2-1 provide the location number of each jumper, the purpose of each jumper, and the system where each jumper is found. The "Jumper Connection" column lists the numbers identifying which pads or stake pins on the processor board are connected. An asterisk (*) following a number indicates that the connection is the default setting for off-the-shelf 86/30 processor boards. The "Purpose" column briefly states the function of each connection. If the connection is specific to an expansion board, it is also listed in the "Purpose" column. Entries in the "System 310 Configuration" column indicate which preconfigured system has that jumper connected.

The sections following the table talk about each of the System 310-specific jumpers in turn. Each section shows a blowup of the outlined jumper areas in Figure 2-2 along with an explanation of the purpose of each connection. Reading through these sections can help you decide if a jumper change is necessary and can help you understand more about your system.

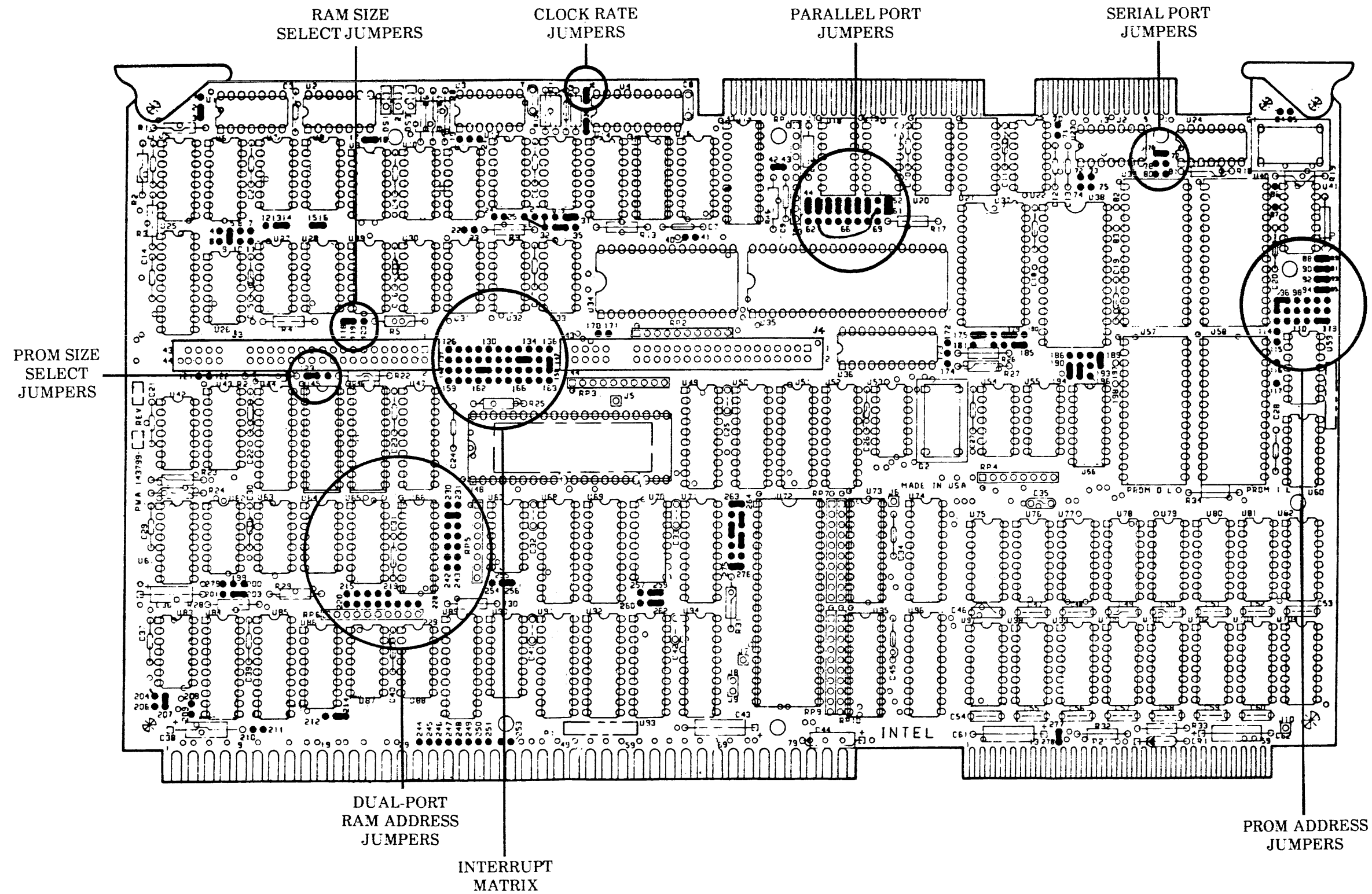


Figure 2-2. Jumpers Common to All Configurations

F-0101

Table 2-1. Common and Specific Jumpers

| Jumper Connection | Purpose | System 310 Configuration |
|-------------------|--|--------------------------|
| *2-3 1 | Connects 8284A to 8MHZ | -1,-2,-3 |
| *5-9 | Wait state | -1,-2,-3 |
| *13-14 | Wait state | -1,-2,-3 |
| *15-16 | Test | -1,-2,-3 |
| *17-18 | Test | -1,-2,-3 |
| *22-23 | Enables OVERRIDE/signal for locking the dual-port RAM | -1,-2,-3 |
| 26-32 | Allows NMI from status register to control NMI input to the 8086 | -1,-2,-3 |
| *28-32 | Continually enables the GATE input for Timer 0 | -1,-2,-3 |
| *30-31 | Continually enables the GATE input for Timer 1 | -1,-2,-3 |
| *33-34 | Selects bus vectored interrupts | -1,-2,-3 |
| *36-37 | Selects 5MHz clock rate for the 8086 CPU | -1,-2,-3 |
| *38-39 | Enables the failsafe timeout to the 8259A | -1,-2,-3 |
| *40-41 | Not user configurable | -1,-2,-3 |
| *42-43 | Disables latch and edge interrupts | -1,-2,-3 |
| *44-53 | " | -1,-2,-3 |
| *45-54 | " | -1,-2,-3 |
| *46-55 | " | -1,-2,-3 |
| *47-56 | " | -1,-2,-3 |
| *48-57 | " | -1,-2,-3 |
| *49-58 | " | -1,-2,-3 |
| *50-59 | " | -1,-2,-3 |
| *52-61 | Puts port A buffer of the 8255A in output mode | -1,-2,-3 |
| 60-63 | PA INTR signal from the parallel port | -1,-2,-3 |
| 76-77 | Allows serial port signal RTS to generate CTS | -1,-2,-3 |
| *84-85 | Test | -1,-2,-3 |
| *88-89 | PROM address selectors for range F8000H through FFFFFH | -1,-2,-3 |
| *90-91 | " | -1,-2,-3 |
| *92-93 | " | -1,-2,-3 |
| *94-95 | " | -1,-2,-3 |
| 96-97 | " | -1,-2,-3 |
| 96-102 | " | -1,-2,-3 |
| 112-113 | " | -1,-2,-3 |
| *114-115 | Connects +5V to battery backup | -1,-2,-3 |
| *118-119 | Indicates 128K of on-board RAM | -1, -3 |
| 118,119, & 120 | Indicates 256K of on-board RAM (used with 304 board) | -2 |

Table 2-1. Common and Specific Jumpers (Continued)

| Jumper Connection | Purpose | System 310 Configuration |
|-------------------|---|--------------------------|
| 123-124 | Indicates 64K PROMs are used | -1,-2,-3 |
| 127-154 | Connects OR5 to IR7 | -1,-2,-3 |
| 128-155 | Connects OR INTR2 to IR6 | -1,-2,-3 |
| 130-134 | Connects OR INTR1 to IR7 | -1,-2,-3 |
| 131-142 | Connects OR2 and OR3 | -1,-2,-3 |
| 132-157 | Connects PA INTR to IR4 | -1,-2,-3 |
| 136-159 | Connects IR3 to INT3 | -1,-2,-3 |
| 138-139 | Connects OR0 and OR4 | -1,-2,-3 |
| 139-145 | Connects NMI to OR0 | -1,-2,-3 |
| 140-153 | Connects RxRDY to interrupt matrix | -1,-2,-3 |
| 142-144 | Connects OR3 to ground | -1,-2,-3 |
| *144-145 | Disables NMI to the 8086 | -1,-2,-3 |
| *147-158 | Connects Timer INTO to IR2 | -1,-2,-3 |
| 149-164 | Connects INT1 (front panel) to IR1 | -1,-2,-3 |
| *151-152 | Connects INT5 from bus to IR5 | -2,-3 |
| 152-169 | Redirects INT5 to iSBX connector J4 (use when the 218A is installed on the 86/30 processor board) | -1 |
| 165-166 | Connects 8087 to INTO (for 337 math board only) | -2,-3 |
| *175-176 | Selects 1.23MHz for counter 0 | -1,-2,-3 |
| *178-179 | Selects 1.23MHz for counter 2 | -1,-2,-3 |
| *184-185 | Selects 156.3KHz for counter 1 | -1,-2,-3 |
| *189-193 | Connects DTR to DSR, 8251A | -1,-2,-3 |
| *190-194 | Selects TxC (counter 2), 8251A | -1,-2,-3 |
| *191-195 | Selects RxC (counter 2), 8251A | -1,-2,-3 |
| *202-203 | Bus arbitration | -1,-2,-3 |
| *205-207 | Provides BCLK/ to bus | -1,-2,-3 |
| *208-209 | Provides CCLK/ to bus | -1,-2,-3 |
| *213-214 | Connects CBRQ/ to bus | -1,-2,-3 |
| 232-233 | Selects ending RAM address 1FFFFH | -1, -3 |
| *254-255 | Not user configurable | -1,-2,-3 |
| *258-259 | " | -1,-2,-3 |
| *261-262 | " | -1,-2,-3 |
| *263-264 | " | -1,-2,-3 |
| *266-268 | " | -1,-2,-3 |
| *267-269 | " | -1,-2,-3 |
| *270-272 | " | -1,-2,-3 |
| *275-276 | " | -1,-2,-3 |
| *277-278 | Connects +5 volts to the battery backup circuit | -1,-2,-3 |

*Indicates the default jumper setting for off-the-shelf processor boards.

¹All jumper numbers are preceded with an E in the schematics.

CLOCK RATE JUMPER

Connecting jumper locations 36 to 37, as shown in Figure 2-3, selects a 5 MHz clock rate for the 8086 CPU. You must run the CPU at 5 MHz when using an 8087 math coprocessor in the system. For example, since the 8087 coprocessor is part of the the 337 math board, you must chose the 5 MHz clock rate when using this board. Removing the connection between 36 and 37 selects 8 MHz.

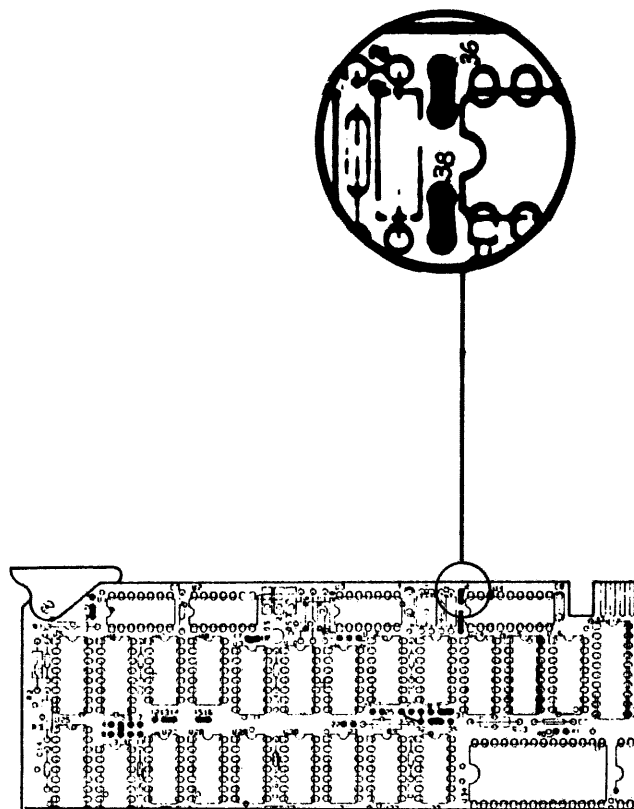
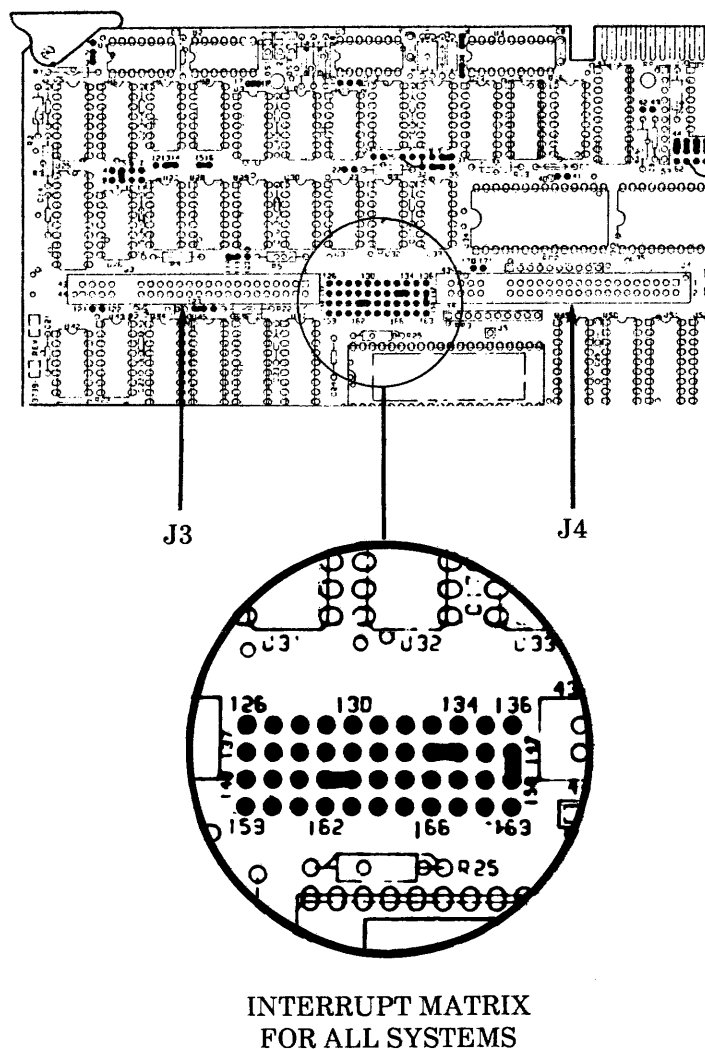
CLOCK RATE JUMPER
(Selects 5 MHz)

Figure 2-3. Clock Rate Jumper

F-0106

INTERRUPT MATRIX

The block shown between J3 and J4 in Figure 2-4 is a matrix of stake pins called the interrupt matrix. Connections between these pins determine which board functions, such as resetting the system, are connected to the interrupt structure of the CPU. Figure 2-4 shows four connections: 127 to 140, 144 to 145, 147 to 158, and 151 to 152. These connections disable the nonmaskable interrupt (NMI) and route interrupts to the MULTIBUS interface, as listed in Table 2-1.



INTERRUPT MATRIX
FOR ALL SYSTEMS

Figure 2-4. Interrupt Matrix Jumpers

F-0105

While there are eight interrupts defined by the MULTIBUS interface, the processor board uses seven interrupt levels for its operation leaving, effectively, only one available. The processor board saves INT3 for you to use. You might use INT3, for example, with terminal controller boards like the iSBC 544 Intelligent Communications Controller.

Table 2-2 lists the devices that can interrupt the system and each interrupt's priority level. So you will not be confused, notice that INT3 is also called IR3 on processor board schematics and in other hardware reference literature, and is shown this way in Table 2-2. Refer to the *iSBC 86/14 and iSBC 86/30 Hardware Reference Manual*, listed in the Preface, for more information about interrupts and what they do.

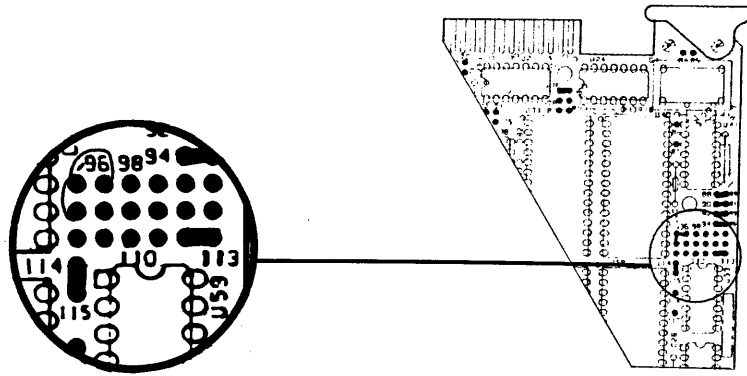
Table 2-2. Interrupt Priority Assignments

| Device Level | Description | Priority |
|--------------|------------------------------|----------|
| 8086 NMI | 309 memory manager interrupt | Highest |
| 8259A IR0 | Floating-point exception | . |
| " IR1 | Control panel interrupt | . |
| " IR2 | On-board timer | . |
| " IR3 | Available | . |
| " IR4 | Line printer | . |
| " IR5 | Disk interrupt | . |
| " IR6 | Serial I/O receive | . |
| " IR7 | Serial I/O transmit | Lowest |

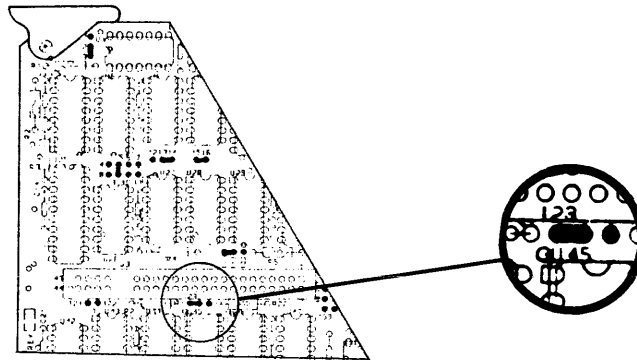
PROM SIZE AND PROM ADDRESS JUMPERS

The System 310 uses four 64K PROMs containing the system firmware. You have one of two sets of PROMs in your system depending on the location of the 218A controller board, as explained earlier in Chapter 1. Figure 2-1 shows the location of these PROMs.

Regardless of which set of PROMs you use, the capacity (size) and location of the PROMs are the same. Two sets of jumpers, shown in Figure 2-5, specify these PROMs to the processor board. The first set of connections, 123 to 124, tells the processor board you are using 64K PROMs. Figure 2-5 shows them on the left side of the processor board. On the right side, the second set of connections (96 to 97, 96 to 102, and 112 to 113) tells the processor board that the PROMs start at address F8000H and end at address FFFFFH.



PROM ADDRESS JUMPERS
(Selecting F8000H to FFFFFH)



PROM SIZE SELECT JUMPERS
(Selecting 64K Devices)

F-0104

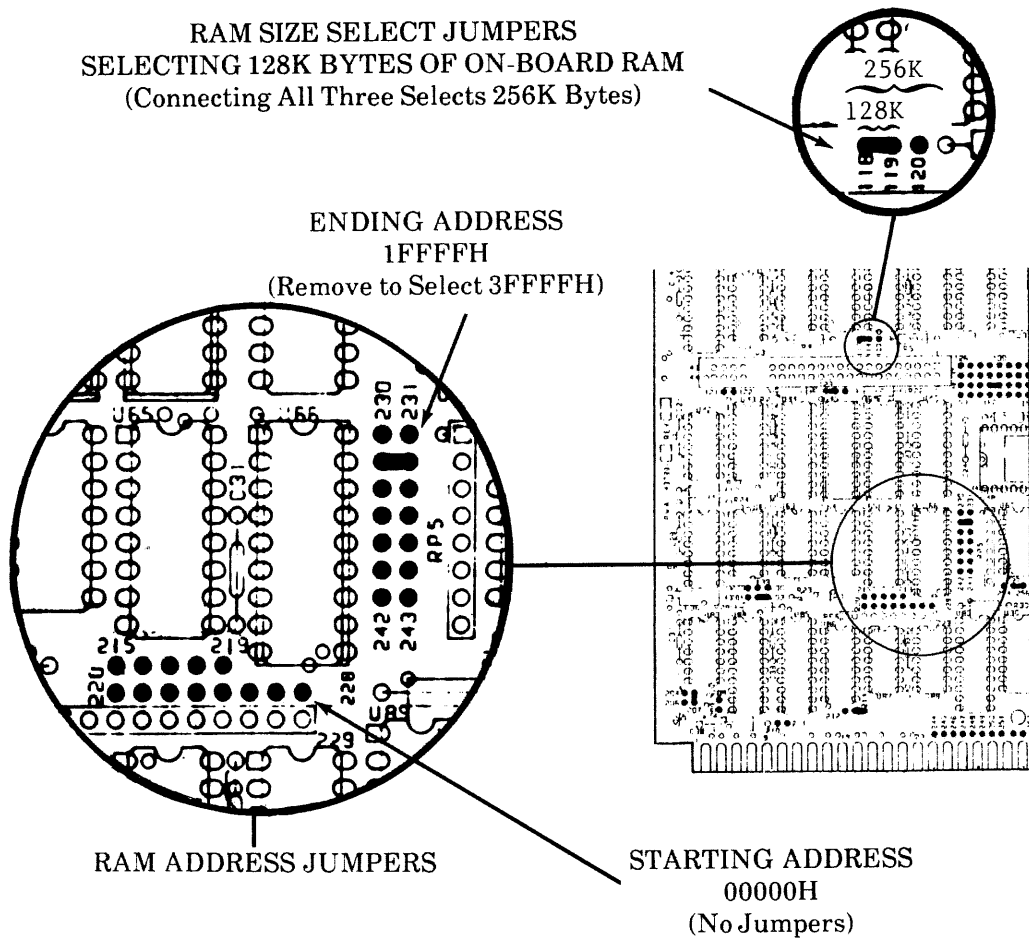
Figure 2-5. PROM Size and PROM Address Select Jumpers

RAM SIZE AND RAM ADDRESS JUMPERS

There are 128K bytes of dual-port RAM on the processor board. The same dual-port RAM space can be accessed with two different addresses, one originating from the processor board and one originating from the bus. The processor board finds this RAM at 00000H as determined by the system firmware residing in its PROMs. You access the dual-port RAM from the MULTIBUS interface.

To access dual-port RAM, you must describe its size and location to the processor board with three jumper connections, shown in Figure 2-6. The factory sets them for you in the preconfigured systems. For example, in the System 310-1 and System 310-3, the jumpers are set as follows:

The first connection, 118 to 119, tells the processor that there are 128K bytes of RAM on the board. The second connection, actually



F-0103

Figure 2-6. RAM Size and RAM Address Select Jumpers

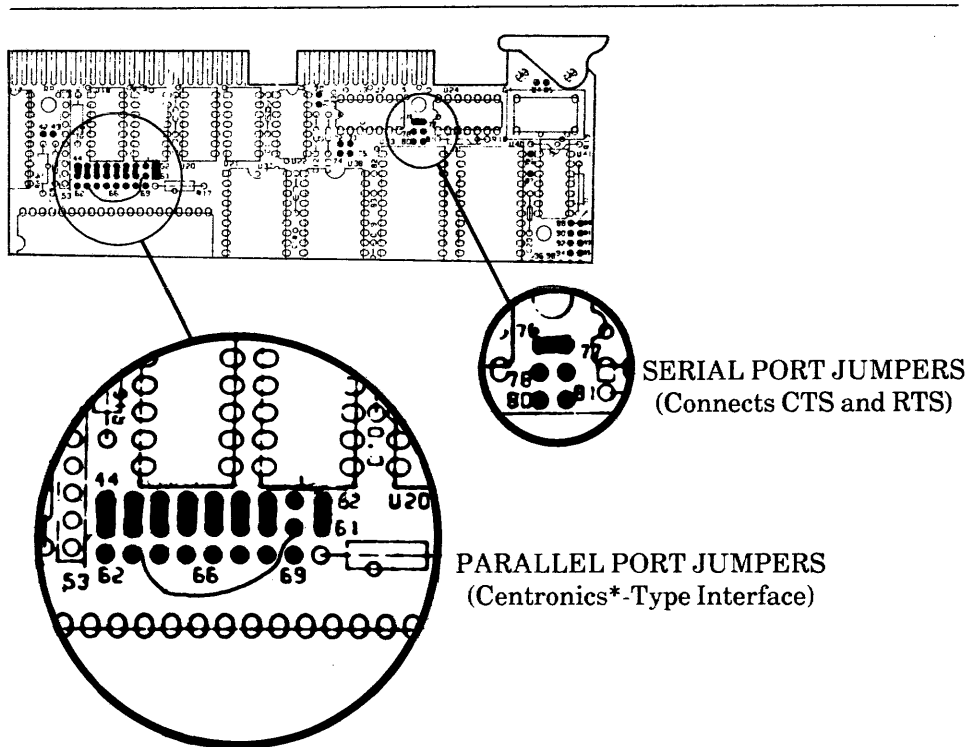
the absence of a connection between 219 and 225, selects starting address 0000H. The third connection, 232 to 233, selects ending address 1FFFFH.

If you add a 304 RAM MULTIMODULE board to your system, you must make the same two jumper changes that the factory makes to the processor board. First, select a new, higher ending address, 3FFFFH, by simply removing the connection between 232 and 233. Next, select a new, larger size, 256K bytes, by adding a connection from 119 to 120, thus connecting all three size selection jumper posts (118, 119, and 120).

For more information about dual-port RAM addressing, refer to the *iSBC 86/14 and iSBC 86/30 Single Board Computer Hardware Reference Manual* listed in the Preface. Also, Chapter 4 in this manual contains specific installation instructions for the 304 RAM board.

I/O PORT JUMPERS

The processor board provides two I/O ports for the System 310: an RS-232 serial port and a Centronics-type parallel port. Figure 2-7 shows the serial and parallel port jumpers.



* Centronics is a trademark of Centronics Data Computer Corporation.

Figure 2-7. Serial and Parallel Port Jumpers

F-0102

The serial port jumper, connecting 76 and 77, wires the CTS (clear to send) and RTS (request to send) signals together so that the System 310 accepts all standard RS-232-compatible terminals. This connection allows RTS to generate CTS.

The nine parallel port jumpers, also shown in Figure 2-7, provide a Centronics-type printer interface by connecting:

- 44 to 53
- 45 to 54
- 46 to 55
- 47 to 56
- 48 to 57
- 49 to 58
- 50 to 59
- 52 to 61
- 60 to 63



CHAPTER 3 REMOVING AND INSTALLING THE PROCESSOR BOARD

This chapter provides step-by-step instructions for removing and installing the processor board in the System 310 chassis. Once the processor board is removed, you can make modifications to it (such as adding or removing a MULTIMODULE board) before installing it again in the System 310. It takes 20 to 30 minutes to perform the instructions in this chapter.

WARNING

Unless you are a qualified service technician, do not attempt to service any parts in this system because of the risk of electrical shock. Only the boards and jumpers that can be reached by removing the back panel can be safely handled by users.

EQUIPMENT YOU WILL NEED

Phillips head screwdriver for #6 and #8 Phillips screws.

REMOVING THE PROCESSOR BOARD

The next three headings describe the major steps for removing the processor board from the System 310 chassis. Quite simply, you must open the chassis, disconnect the cables, and remove the board.

WARNING

To guard against a risk of fire, always disconnect the power cord before removing the chassis back panel.

OPENING THE CHASSIS

1. Turn off the power, then remove the AC power cord from the back of the System 310 chassis.
2. Turn the chassis so that the back panel faces you.
3. Remove the four Phillips screws holding the back panel. Save these screws and remember where they came from so you can reinsert them later.

4. Tilt the top of the back panel toward you and lift it out of the track at the bottom of the chassis. Be careful not to pull the back panel toward you so far that you disconnect the cables prematurely.

DISCONNECTING THE CABLES

Figure 3-1 shows the chassis with the back panel ajar and identifies the cables plugged into the processor board. The smaller one on the left is the serial port cable, and the larger one on the right is the parallel port cable. To remove the processor board, you must disconnect these cables as described in the next three steps.

1. With one hand, raise the back panel until you can reach under it, into the cardcage. In the bottom card slot, you will see the 86/30 processor board with two cables plugged into it.
2. With your other hand, disconnect these two cables. This frees the bottom of the back panel from the processor board. All other cables remain connected.

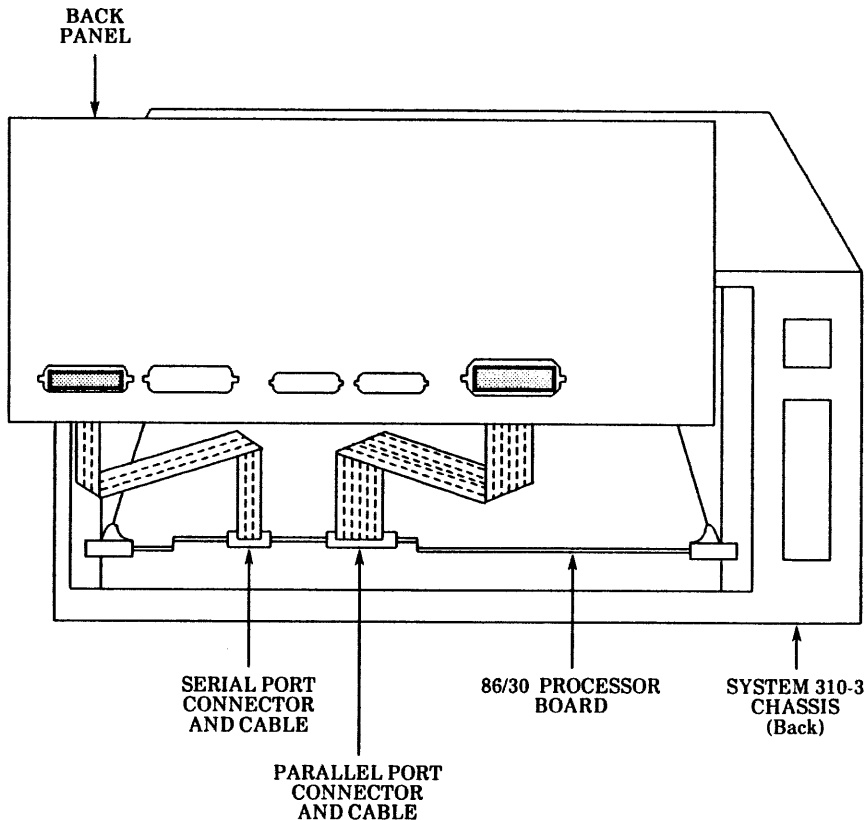


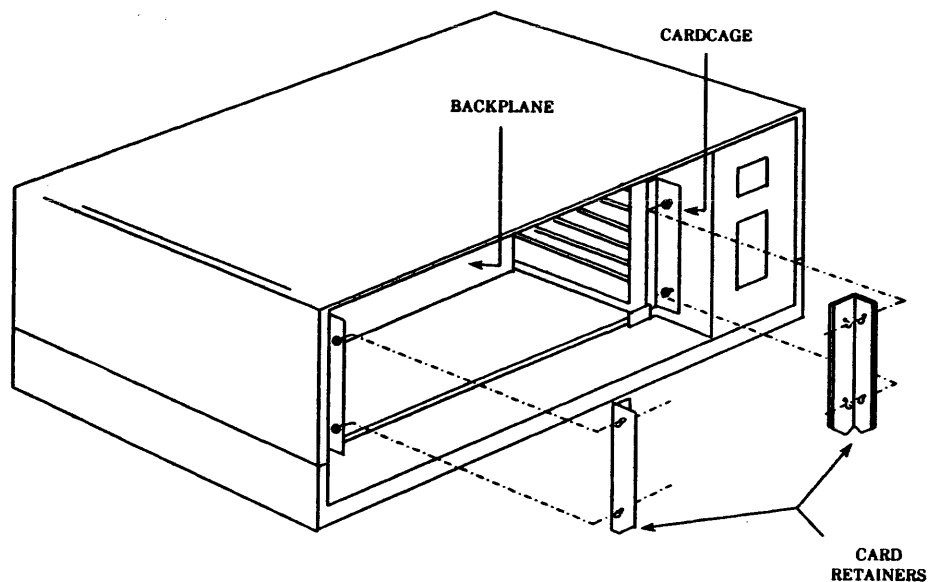
Figure 3-1. Installing the Serial and Parallel Port Cables F-0010

3. Lay the back panel on top of the chassis by flipping it over, connector side down. This keeps the back panel and any cables attached to it out of the way while you work inside the cardcage. Alternatively, you can remove all the cables and set the back panel aside. Be sure to mark or remember where the disconnected cables go so you can replace them.

WITHDRAWING THE BOARD FROM THE CARDCAGE

The next two steps describe how to remove the board from the edge connector at the back of the cardcage.

1. Loosen the screws that hold the two card retainers, shown in Figure 3-2. Lift each retainer up until it is free of the mounting screw and remove it. Save the retainers. These retainers prevent the cards from vibrating loose from the backplane during operation and transportation.



F-0087

Figure 3-2. Removing the Card Retainers

2. Find the processor board in the bottom slot (slot 1) of the cardcage. Use the two card ejectors as a lever to disconnect it from the backplane. When the board "pops" out, pull it free.

INSTALLING THE PROCESSOR BOARD

The four steps in this section explain how to install the processor board in the System 310 chassis.

1. Remove the back panel by following the steps listed earlier in this chapter in the section called "Opening the Chassis."
2. Once you have exposed the cardcage, insert the processor board in the bottom slot of the cardcage (slot 1). Be sure that the card edge connector of the processor board slides in first and that the component side is up. Push the processor board into the cardcage until it touches the edge connector.

NOTE

This recommended board placement conserves card slots although, with proper bus priority jumper settings, the board works in any position. The wider first and seventh slots in the cardcage are designed to accommodate cards with MULTIMODULE boards attached. For more information about board placement and priority, refer to the *System 310 Hardware Integration Guide*.

3. To seat the board firmly in the edge connector, place your thumbs on the flat part of the card ejectors, pushing firmly until the card stops. You may need to flex the middle of the board slightly, compensating for any warps, to get the board to seat properly.
4. Test the connection by gently trying to pull the board out again. If you feel resistance, the board is securely seated. Another test: when the board is properly seated, the card ejectors rest flat against the cardcage. If the board slides forward, or if the card ejectors are not flush against the cardcage, repeat step 3 above until these tests are met.

CLOSING THE CHASSIS

The seven steps in this section describe how to replace the back panel on the chassis. Essentially, it is the reverse of the removal process presented earlier in this chapter.

1. Install the card retainers.
2. Connect the serial and parallel cables. Although these ribbon cables are both marked P1, you can readily tell them apart by

the number of conductors they contain. The parallel cable has 34 conductors and the serial cable has 25 conductors.

Plug the P1 connector on the parallel cable into the port marked J1 on the processor board; likewise, plug the P1 connector on the serial cable into J2 on the processor board. To correctly align the cables, be sure the P1 labels are upright. J1 and J2 are silkscreened onto the processor board. Figure 3-1 shows this placement.

3. Connect any other loose cables. Refer to the individual System 310 manuals listed in the Preface for details on cable routing.
4. Insert the bottom of the back panel into the track at the bottom of the chassis.
5. Carefully push the excess cable into the space between the processor board and the back panel until the back panel fits flat against the chassis.
6. Align the screw holes in the back panel with the screw holes in the chassis, being sure not to pinch any cables, and replace the four screws you removed earlier.
7. Install the AC plug and turn the system on to run the system confidence tests (SCTs).



Intel adds more memory to the System 310-2 by combining an iSBC 304 RAM Expansion MULTIMODULE Board with the processor board. This RAM board expands the 128K bytes of memory already on the processor board to 256K bytes. Memory is expanded differently in other System 310 configurations. For more information, refer to the *System 310 Memory Configuration Guide: 86-Based Systems*.

This three-part chapter describes how to fasten the RAM MULTIMODULE board onto the iSBC 86/30 Single Board Computer. The first part tells you how to remove components from the processor board and how to change jumpers. The second part explains how to install the RAM board in the resulting empty sockets. The third part explains how to replace components on the RAM board.

EQUIPMENT YOU WILL NEED

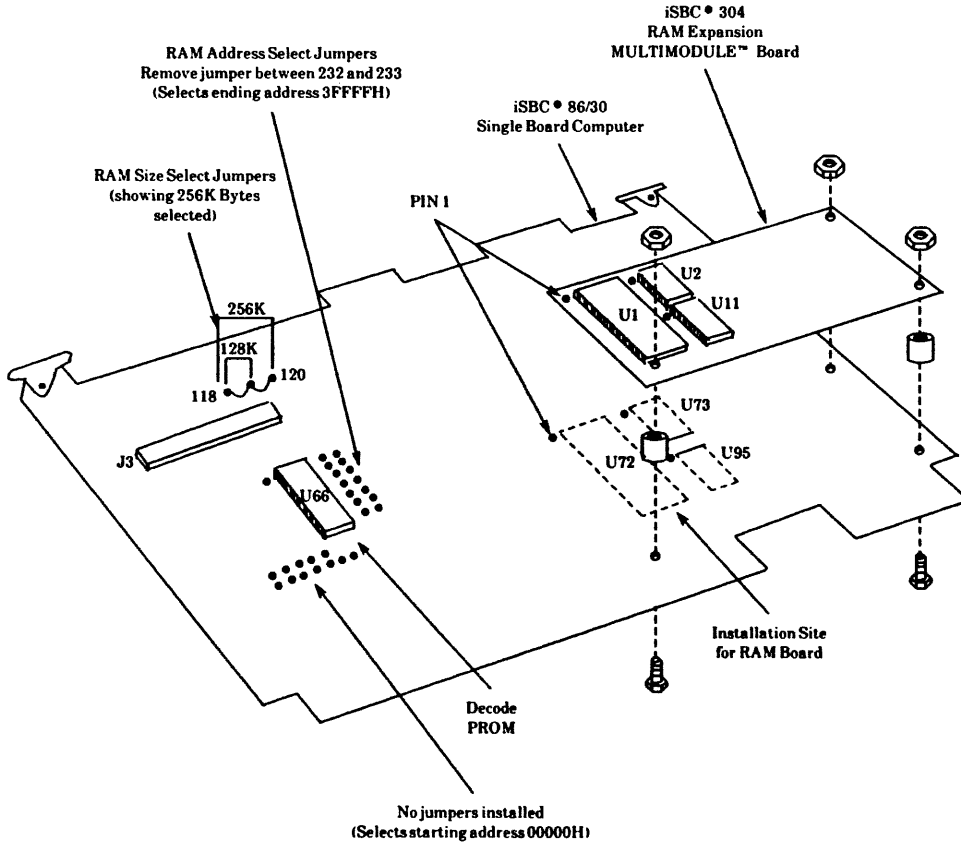
Flat-blade screwdriver for #6 screws
New decode PROM labeled 144109-001
Wire-wrap gun and 2 inches of 30-gauge Kynar wire

REMOVING COMPONENTS AND CHANGING JUMPERS

1. Remove the processor board from the System 310 cardcage by following the instructions in Chapter 3.
2. Set the processor board down on a static-free surface, component side up, and remove and save the following components.
 - 8203 in U72
 - 74LS373 in U73
 - 74LS373 in U95
 - Decode PROM in U66 labeled 144108-001

Figure 4-1 shows the locations of these components and the jumpers described next.

3. Remove the jumper connecting 232 and 233 to change the ending address of memory on the processor board from 1FFFFH to 3FFFFH.
4. To tell the processor board there are now 256K bytes of RAM instead of 128K, remove the jumper connecting 118 and 119, and wire wrap 118, 119, and 120 together.



F-0088

Figure 4-1. Installing the 304 RAM Board

INSTALLING THE RAM BOARD IN THE CARDCAGE

1. To connect the RAM board to the processor board, align the connector pins on the underside of the RAM board with socket U72 on the processor board, as shown in Figure 4-1. Be sure that pin 1 of the socket aligns with pin 1 of the connector.
2. When the pins are aligned, push down on the RAM board at U1 to seat the MULTIMODULE board in the socket on the processor board. Verify that no pins are bent.
3. Line up any pair of mounting holes, shown by the dashed lines in Figure 4-1. Insert a nylon spacer between these two holes.
4. From the solder side of the processor board, insert a screw all the way through the processor board, the spacer, and the RAM board. Attach the nut, tightening it with your fingers.
5. Finish installing the RAM board to the processor board by adding the other two screws, spacers, and nuts. (Repeat steps 3 and 4.)
6. Tighten all three screws with a screwdriver.

CAUTION

Overtightening the screws could damage the screws or the circuit board.

REPLACING THE COMPONENTS

1. Insert the 8302 component in U1 of the RAM board after aligning pin 1 of the 8203 with pin 1 of the socket, as shown in Figure 4-1.
2. After aligning pin 1's, insert the two components labeled 74LS373 in locations U2 and U11 on the RAM board.
3. After aligning pin 1's, insert the new decode PROM, labeled 144109-001, in U66 on the processor board. Save the removed PROM. Should you ever remove the 304 board, you will need to exchange PROMs.

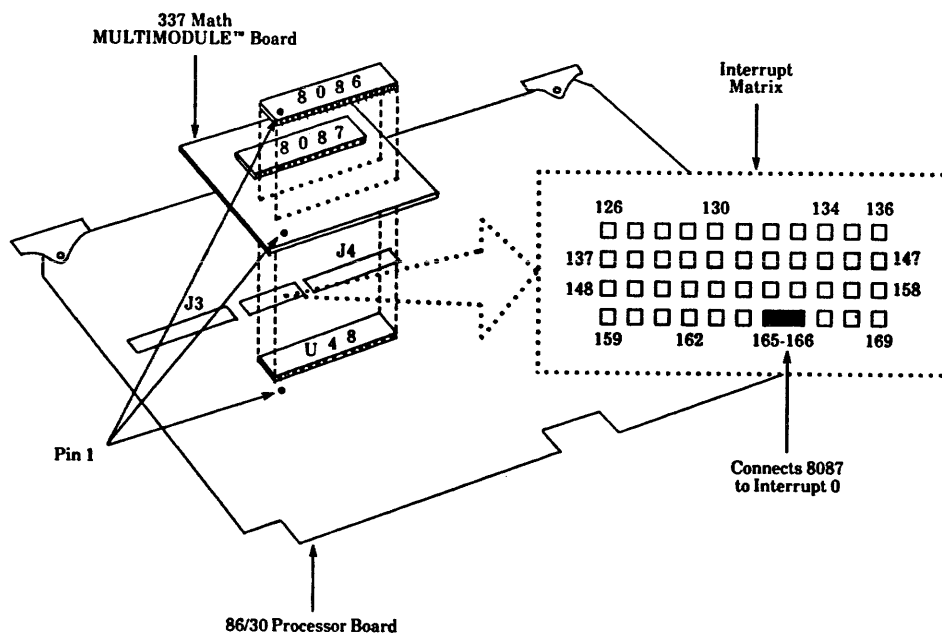
The processor board can now be installed in the chassis, as described in Chapter 3.



Intel adds floating-point math to both the System 310-2 and 310-3 by attaching the iSBC 337 MULTIMODULE Numeric Data Processor to the processor board. This MULTIMODULE board contains an 8087 math coprocessor and the 8086 CPU from the processor board.

INSTALLING THE MATH BOARD AND SETTING THE JUMPERS

The next five steps explain how to install the floating-point math board and set the jumpers. Figure 5-1 shows this installation and jumpering sequence.



F-0089

Figure 5-1. Installing the Math Board

1. Remove the processor board from the System 310 cardcage according to the instructions in Chapter 3.
2. Remove the 8086 CPU from U48 on the processor board. Save the CPU.
3. After aligning pin 1 of the connector on the solder side of the math board with pin 1 of U48, install the math board in the empty socket, as shown in Figure 5-1.
4. Align pin 1 of the CPU chip with pin 1 of the empty socket on the math board and install the CPU.
5. On the processor board, add a jumper between locations 165 and 166 in the interrupt matrix, as shown in Figure 5-1. This jumper connects the math board to the interrupt 0 level of the PIC (programmable interrupt controller--8259A).

The processor board can now be installed in the System 310 chassis according to the instructions in Chapter 3.



APPENDIX A SERIAL AND PARALLEL CONNECTOR PINOUTS

The two tables in this appendix, Tables A-1 and A-2, list the RS-232 serial and Centronics-type parallel connector pinouts, respectively. The pin number, described in the first column of both tables, refers to the 86/30 processor board's edge connector. The serial connector is labeled J2 and the parallel connector is labeled J1 on the board. The connector pin number columns describe the pin number of each cable as read from the outside of the back panel. These, then, are the signals your I/O cable plugs directly into. The description columns provide the names of the signals found in the schematics for the 86/30 processor board in the *iSBC 86/14 and iSBC 86/30 Single Board Computer Hardware Reference Manual*. Chapter 3 explains how to connect the cables.

Table A-1. RS-232 Serial Connector Pinouts

| 86/30 Board Pin Number | RS-232 Connector Pin Number | Description |
|---------------------------|--------------------------------|----------------------------------|
| 1 | 14 | No connection |
| 2 | 1 | Ground |
| 3 | 15 | No connection |
| 4 | 2 | Transmit Data |
| 5 | 16 | Secondary Receive |
| 6 | 3 | Receive Data |
| 7 | 17 | External Clock |
| 8 | 4 | Request To Send |
| 9 | 18 | No connection |
| 10 | 5 | Clear To Send |
| 11 | 19 | No connection |
| 12 | 6 | Data Set Ready |
| 13 | 20 | Data Terminal Ready |
| 14 | 7 | Ground |
| 15 | 21 | No connection |
| 16 | 8 | No connection |
| 17 | 22 | No connection |
| 18 | 9 | No connection |
| 19 | 23 | -12 VDC |
| 20 | 10 | No connection |
| 21 | 24 | Data Terminal Equipment Clock |
| 22 | 11 | +12 VDC |
| 23 | 25 | +5 VDC |
| 24 | 12 | No connection |
| 25 | No connection | Ground |
| 26 | 13 | Secondary CTS |

Table A-2. Centronics Parallel Connector Pinout

| 86/30 Board Pin Number | Parallel Connector Pin Number | Description |
|---------------------------|----------------------------------|-------------|
| 1 | No connection | - |
| 2 | No connection | - |
| 3 | No connection | - |
| 4 | No connection | - |
| 5 | No connection | - |
| 6 | No connection | - |
| 7 | No connection | - |
| 8 | No connection | - |
| 9 | No connection | - |
| 10 | No connection | - |
| 11 | No connection | - |
| 12 | No connection | - |
| 13 | No connection | - |
| 14 | No connection | - |
| 15 | No connection | - |
| 16 | No connection | - |
| 17 | No connection | - |
| 18 | No connection | - |
| 19 | No connection | - |
| 20 | No connection | - |
| 21 | No connection | - |
| 22 | No connection | - |
| 23 | 19 | Ground |
| 24 | 1 | STB |
| 25 | 29 | Ground |
| 26 | 13 | RDY |
| 27 | 29 | Ground |
| 28 | 12 | RDY/ |
| 29 | 28 | Ground |
| 30 | 10 | ACK |
| 31 | No connection | - |
| 32 | No connection | - |
| 33 | 27 | Ground |
| 34 | 9 | DATA7 |
| 35 | 26 | Ground |
| 36 | 8 | DATA6 |
| 37 | 25 | Ground |
| 38 | 7 | DATA5 |
| 39 | 24 | Ground |
| 40 | 6 | DATA4 |
| 41 | 23 | Ground |
| 42 | 5 | DATA3 |
| 43 | 22 | Ground |
| 44 | 4 | DATA2 |
| 45 | 21 | Ground |
| 46 | 3 | DATA1 |
| 47 | 20 | Ground |



APPENDIX B UPLOADING AND DOWNLOADING

The steps in this appendix describe how to transfer data files from an 86-based System 310 running the iRMX 86 Operating System to an Intel development system running the ISIS-II Operating System (downloading). It also describes how to transfer files to the System 310 from the development system (uploading). The Intel development systems covered by the instructions in this appendix are: the Series II, the Series III, and the 800.

To transfer files between the development system and the System 310, you must do three things to the hardware: 1) modify a parallel I/O cable; 2) alter the parallel port configuration on the System 310's processor board; and 3) change some jumpers. These changes prevent you from using the parallel port for a line printer or other parallel device. Therefore, be sure to return the System 310 to its original configuration before attempting to run them.

EQUIPMENT YOU WILL NEED

To transfer files, you will need an iRMX operating system diskette containing the UPCOPY and DOWNCOPY utility programs and an ISIS-II operating system diskette.

To configure the parallel port of the System 310's 86/30 processor board you will need:

- A wire-wrap gun
- A 1-foot length of 30-gauge Kynar wire
- A pair of 30-gauge wire strippers
- A pair of flush-cut wire cutters

To configure the System 310 hardware so it can transfer files, you will need the iSBC 957B iAPX 86, 88 Interface and Execution Package, part number 143974.

From this kit, you need only the following parts:

- The single-density diskette labeled iSBC 957B Interface and Execution Software, OR the double-density diskette labeled iSBC 957B Interface and Execution Software. The disk you use depends on the density rating of your drives.

- The 50-conductor parallel I/O ribbon cable.
- The status adapter board (approximately the size of a large component).

In addition, you will need to provide the following parts and equipment for modifying the parallel I/O cable:

- A 50-pin male delta-shaped ribbon cable connector. Two vendors who make this part are: Ansley, part number 609-50MA; and 3M, part number 3564-1001.
- A 50-pin female delta-shaped ribbon cable connector. The same two vendors also make this panel-mounting part: Ansley, part number 609-50F; and 3M, part number 3565-1000.
- A razor blade or utility knife for cutting ribbon cable.
- A cable clamp for installing connectors on the ribbon cable.
- Panel mounting hardware provided by the connector manufacturers and a screwdriver that fits it.

MODIFYING THE PARALLEL I/O CABLE

You must physically connect an Intel Series II, III, or 800 development system to the System 310 to transfer data between them. The parallel I/O cable, provided with the 957B package, serves this purpose. However, you must modify this cable to safely operate your System 310.

WARNING

To prevent fire hazards, do not operate the System 310 with the parallel I/O cable directly attached to the processor board.

The modification divides the cable and adds a male and female connector to the severed ends. The female connector then attaches to the back panel of the System 310 so you can plug the male connector directly into it.

Although the electrical connection between the 86/30 processor board and the connector labeled UPP on the back of the destination development system is direct and unscrambled, do not plug the cable directly into the parallel port of the processor board. Doing so would mean that the System 310 would have to operate with the back panel off or ajar, defeating the cooling system and creating a safety hazard. Take the time to modify the parallel cable so that you can conveniently plug the two systems together using the back panels.

Follow this four-step procedure to modify the parallel I/O cable. You should already be familiar with cable-making practices before following these steps.

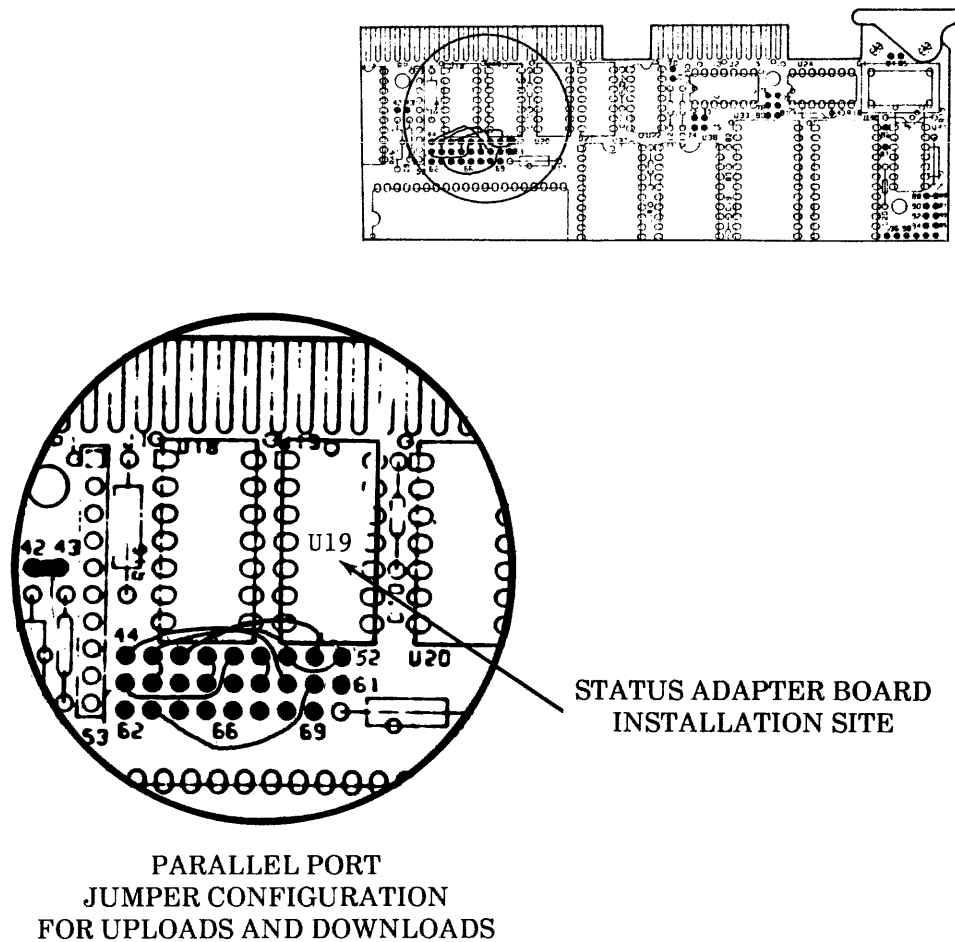
1. Lay the parallel I/O cable from the 957B package on a work surface. Measure along the cable 10 inches from the edge connector and cut it in two, across the conductors, with a razor or utility knife.
2. Clamp a 50-pin female connector onto the cable segment that has the edge connector attached. Be sure to align the red stripe that indicates pin 1 on the cable with pin 1 on the female connector. This cable connects the System 310's processor board to the inside of the back panel and is called the internal parallel I/O cable.
3. Clamp the 50-pin male connector onto the end of the other cable segment, aligning the red stripe with pin 1 on the connector. This cable will attach to the back panels of the two systems and is called the external parallel I/O cable.
4. Mount the internal parallel I/O cable by attaching the female connector to any 50-pin mounting hole in the System 310 back panel. Install this connector so the cable extends into the cardcage when the back panel is replaced. To mount the cable, you will probably need to remove a knockout. Use the mounting hardware and directions provided by the connector manufacturer.

CONFIGURING THE PROCESSOR BOARD

The eight steps in this section explain how to configure the processor board's parallel port and connect the cables. This configuration allows the System 310 to use the development system as an output device. You should know how to wire wrap before following these instructions.

1. Remove the System 310's processor board according to the instructions in Chapter 3.
2. Remove all the jumpers in the parallel port jumper area. (See Figure 2-7 in Chapter 2.)
3. Wire-wrap the following nine jumpers in the same area using a wire-wrap gun and 30-gauge Kynar wire. The resulting parallel port configuration is shown in Figure B-1.

| | |
|----------|----------|
| 44 to 59 | 49 to 58 |
| 45 to 50 | 50 to 52 |
| 45 to 54 | 60 to 63 |
| 46 to 51 | |
| 47 to 56 | |
| 48 to 53 | |



F-0107

Figure B-1. Parallel Port Configuration for Uploads and Downloads

4. Replace the 7438 component in location U19 with the Status Adapter Board. Be sure to align pin 1 of the Status Adapter Board with pin 1 of the socket.
5. Replace the processor board in the System 310 chassis according to the instructions in Chapter 3 of this manual. Do not replace the back panel.
6. Connect the edge connector side of the internal parallel I/O cable to the J1 parallel port of the System 310's processor board. The other end of this cable should already be attached to the inside of the System 310 back panel.

7. Push the excess cable into the space between the cardcage and the back panel and replace the back panel according to the instructions in Chapter 3.
8. Connect the external parallel I/O cable from the port labeled UPP on the back of the Intel development system to the female connector you installed on the System 310's back panel.

RUNNING THE FILE TRANSFER SOFTWARE

The seven steps in this section explain how to operate the file transfer software.

1. Turn on the System 310, the Intel development system, and the drives.
2. Insert an ISIS-II system diskette in drive 0 and insert the iSBC 957B Interface and Execution diskette in drive 1 of the development system.
3. Press the reset switch on the development system. This loads the ISIS-II operating system.
4. Type in this command on the Intel development system keyboard but *do not* follow it with a carriage return:

:F1:APXLOD

5. Press the reset switch on the front of the System 310. As soon as asterisks appear on the System 310's screen, press the carriage return on the development system to execute the APXLOD command. If you wait too long, the iRMX operating system will boot. Repeat steps 3 and 4 if this happens.

Executing the APXLOD command starts the ISIS loader program and stops the asterisk display. You should see the message listed below on the development system's console, followed by the system confidence test (SCT), then another message that says the iRMX operating system has been booted.

ISIS iAPX 86, 88 Loader, Vx.y

NOTE

The status of the PPI system confidence test is OFFLINE rather than GO in this new parallel port configuration. Refer to the *System 300 Series Diagnostic Software User's Guide* for more information about operating and understanding the system confidence tests.

If these messages do not appear, there may be an open or short in the parallel I/O cables you made. If you cannot determine and correct the problem, call the service number listed on the Service Information page of this manual.

Once you have successfully booted the iRMX 86 operating system on the development system's console, you are ready to transfer files. Step 6 describes an UPLOAD, and step 7 describes a DOWNLOAD.

6. To copy files from the Intel development system to the System 310, type in the following command at the System 310 terminal:

UPCOPY filename TO pathname

This copies the ISIS-II file *filename* to the iRMX 86 file *pathname*.

7. To copy files from the System 310 to the Intel development system, type in the following command at the System 310 terminal:

DOWNCOPY pathname TO filename

This copies the iRMX 86 file *pathname* to the ISIS-II file *filename*. For more information about pathnames, refer to the *iRMX 86 Release 5 Operator's Manual*.

RESTORING THE SYSTEM

To restore the System 310's console as the output device, rather than leave the development system as the output device, turn off the power to the development system. This breaks the program running on the System 310. Then reset the System 310 to boot the iRMX operating system software.

To restore the Centronics-type interface to the System 310's parallel port, remove any changes you made when following the instructions in the section on "Configuring the Processor Board" appearing earlier in this appendix. Restore the components and jumpers described in Chapters 2 and 3.



APPENDIX C OPERATING SPECIFICATIONS

WORD SIZE

Instruction 8, 16, 32, 40, or 48 bits
Data 8 or 16 bits

SYSTEM CLOCK SPEED 5 or 8 MHz (jumper-selectable)

INSTRUCTION CYCLE TIME

8 MHz 750 ns
250 ns (when an instruction is in the queue)
5 MHz 1.2 μ s
400 ns (when an instruction is in the queue)

MEMORY CYCLE TIME

RAM 750 ns
EPROM 500 to 875 ns (jumper-selectable)

I/O CAPABILITY

Serial 1 programmable RS-232C interface
(provided by the 8251A Programmable Interface Controller--PIC)
Parallel 24 programmable uni- or bi-directional parallel lines (provided by the 8255A Parallel I/O Port Interface--PPI)
Expansion 1 Centronics-type printer port
2 iSBX bus connectors for expansion boards

SERIAL COMMUNICATION

Synchronous 5- to 8-bit characters
Internal or external character synchronization
Automatic sync bit insertion
Asynchronous 5- to 8-bit characters
Break character generation
1, 1½, or 2 stop bits
False startup detection

DATA TRANSFER RATES

Synchronous Up to 38.4 kHz
Asynchronous Up to 9600 baud

TIMER

Input Frequencies 2.46 MHz \pm 0.1%
1.23 MHz \pm 0.1%
153.6 kHz \pm 0.1%

DIMENSIONS

| | |
|--------|----------------------|
| Width | 12.00 in. (30.48 cm) |
| Height | 6.75 in. (17.15 cm) |
| Depth | 0.70 in. (1.78 cm) |
| Weight | 14 oz. (388 g) |

ENVIRONMENT

| | |
|------------------------|-------------------------|
| Operating Temperatures | 0 to 55°C, ambient |
| Relative Humidity | 0 to 90%, noncondensing |

+5 VDC POWER REQUIREMENTS (75% of maximum)

| | |
|---|-----------|
| 86/30 processor board with 64K EPROM (firmware) and 128K on-board RAM | 5.27 amps |
| 304 MULTIMODULE board | 0.47 amps |
| 337 MULTIMODULE board | 0.45 amps |
| 218A diskette controller | 0.76 amps |

- 012B memory board. *See* Memory
- 215G Winchester Hard Disk Controller, 1-6, 2-3
- 310-1, 310-2, 310-3. *See* Preconfigured systems
- 544 Intelligent Communications Controller, 2-10
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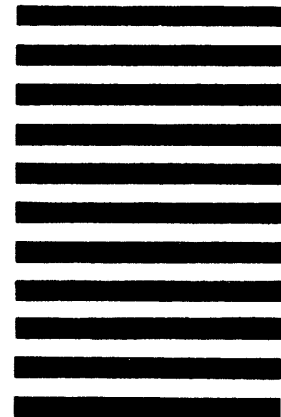
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