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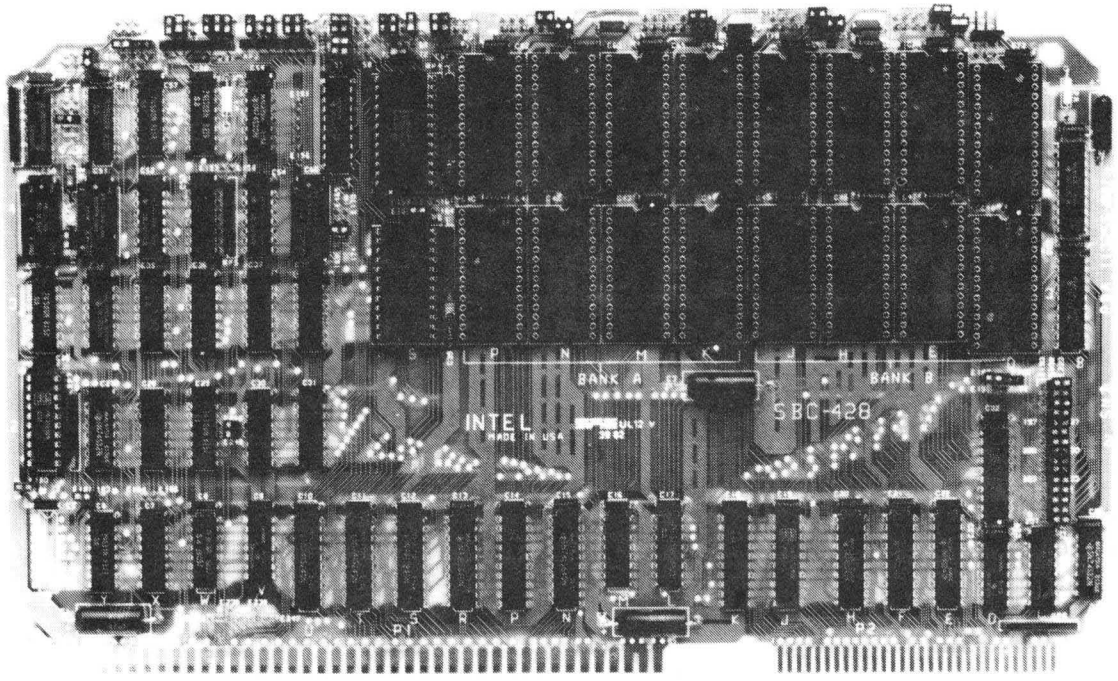
iSBC® 428 UNIVERSAL SITE MEMORY EXPANSION BOARD HARDWARE REFERENCE MANUAL



Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 145696-001

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PREFACE

The information within this manual was compiled by testing Intel manufactured memory devices. Memory devices that conform to the JEDEC byte-wide standard may be used, but may require different jumpers than those listed. Consult the data sheet of the memory devices used for the required information.

This manual provides general information, preparation for use, instructions for preparing your board for installation, and service information for the iSBC 428 Universal Site Memory Expansion Board. Related information is provided in the following publications:

- iSBC® Applications Manual, Order Number: 142687.
- Intel Multibus® Specification, Order Number: 9800683.
- Intel Multibus® Interfacing, Application Note AP-28A.
- Intel iLBX™ Bus Specification, Order Number: 145695.

CONTENTS

CONTENTS (continued)

PAGE

TABLES

CONTENTS (continued)

PAGE

FIGURES

CHAPTER 1. GENERAL INFORMATION

1.1 INTRODUCTION

The iSBC 428 Universal Site Memory Expansion Board adds memory capacity to the system environment. It is compatible with both the Multibus System Bus interface and the faster Intel Local Expansion bus called the iLBX Bus interface. However, you cannot use the iSBC 428 board for both interfaces at the same time. The iSBC 428 board contains sixteen 28-pin sockets which allow you to install memory devices arranged in two separately addressable banks. The actual memory capacity of the board is determined by the size and quantity of your memory devices. The iSBC 428 board supports the following five types of memory devices:

- EPROM - Ultraviolet Erasable Programmable Read Only Memory
- EEPROM - Electrically Erasable Programmable Read Only Memory
- SRAM - Static Random Access Memory
- iRAM - Integrated Random Access Memory
- NVRAM - Non-Volatile Random Access Memory

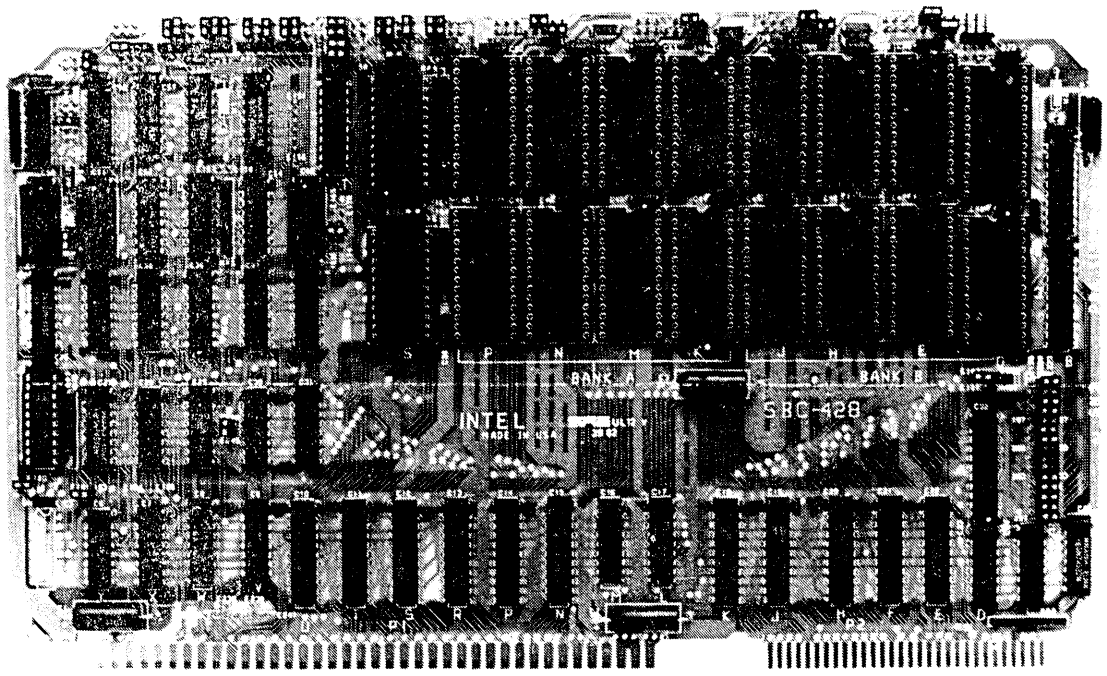

Figure 1-1. iSBC® 428 Universal Site Memory Expansion Board

1.2 DESCRIPTION

The iSBC 428 Universal Site Memory Expansion board is physically and electrically compatible with the Multibus System Bus interface standard as defined in the INTEL MULTIBUS SPECIFICATION. In addition, the board is physically and electrically compatible with the high-speed local bus expansion interface standard as defined in the INTEL iLBX BUS SPECIFICATION.

The iSBC 428 board memory partitioning for each bank is independent and is jumper selectable. These jumpers select one of sixty-four 256K byte pages. Each page is further partitioned by jumpers into blocks providing the starting and ending address within the selected page. It does not provide "dual-port" memory capability, but offers flexibility in that multiple memory device types supported may be installed at one time. This provides an added benefit in that customers may take advantage of memory components with the most density versus the least cost and yet be able to configure the board for a specific application. In addition, the board supports EEPROM and NVRAM devices which are non-volatile memory devices providing memory retention - without batteries.

The iSBC 428 board is jumper selectable for either 8-bit only or 8/16-bit data transfers.

Typical applications for the iSBC 428 board are:

- Additional EPROM/RAM storage for CPU EPROM/RAM based Operating Systems.
- Non-volatile or EEPROM storage of parameters for process control.
- Battery backup for CMOS SRAM to provide non-volatile Read/Write memory backup for data storage.

1.3 DOCUMENTATION SUPPLIED

Each iSBC 428 board is shipped with a corresponding schematic diagram. This diagram should be kept for future reference. The schematic diagram in Chapter 4 of this manual is for reference only.

1.4 SPECIFICATIONS

General specifications for the iSBC 428 board are listed in Table 1-1. Board AC and DC specifications are provided in Appendix A.

The installation of the memory devices adds to the current requirements of the iSBC 428 board. Table 1-2 lists the current requirements for the supported memory devices.

1.5 COMPLIANCE LEVEL: 796 BUS SPECIFICATION (IEEE STANDARD)

All Intel Multibus-compatible boards are designed around guidelines set forth in the 796 BUS SPECIFICATION (IEEE STANDARD - formerly the "Intel Multibus Specification"). The standard requires that certain board operating characteristics, such as data bus width and memory addressing paths, be clearly stated in the board's printed specifications (i.e., reference manual). Used properly, this information quickly summarizes the level of compliance the board bears to the published 796 BUS SPECIFICATION. It clearly states the board's level of compatibility to the Multibus structure. Refer to the 796 BUS SPECIFICATION or the INTEL MULTIBUS SPECIFICATION for additional information.

The following notation states the iSBC 428 board's level of compliance to the 796 BUS SPECIFICATION :

Slave D16 M24

This notation is decoded as follows:

D16 = data path is 8 and/or 16 bits
M24 = memory address path is up to 24 bits

1.6 COMPLIANCE LEVEL: INTEL iLBX™ BUS SPECIFICATION

All Intel iLBX Bus-compatible boards are designed around guidelines set forth in the Intel iLBX BUS SPECIFICATION. The standard requires that certain board operating characteristics, such as data bus width, address path width, and other characteristics, be clearly stated in the board's printed specifications (i.e., reference manual). Used properly, this information quickly summarizes the level of compliance the board bears to the published iLBX BUS SPECIFICATION. It clearly states the board's level of compatibility to the iLBX Bus structure. Refer to the iLBX BUS SPECIFICATION for additional information.

The following notation states the iSBC 428 board's level of compliance to the iLBX BUS SPECIFICATION:

SL D16

This notation is decoded as follows:

SL Slave device

D16 A 16-bit data path

Table 1-1. Board Specifications

ELECTRICAL REQUIREMENTS	
Standard Board, no RAM/EPROM	+5.0VDC ± 5% at 2.5A
CURRENT REQUIREMENTS	
Add for eight 8K x 8 iRAM devices	560mA*
Add for eight 2K x 8 SRAM devices	960mA*
Add for eight 8K x 8 EPROM device	800mA*
Add for eight 16K x 8 EPROM devices	1200mA*
Add for eight 2K x 8 EEPROM devices	1200mA*
Add for eight 512 x 8 NVRAM devices	800mA*
Maximum Total requirements	+5.0VDC ± 5% at 4.9A
PHYSICAL CHARACTERISTICS	
Width:	17.9cm (7.05 inches)
Length:	30.48cm (12 inches)
Thickness:	1.27cm (0.5 inches)
ENVIRONMENTAL CHARACTERISTICS	
Maximum Power Requirements:	25.73W
Standard Board, no RAM/EPROM:	13.13W
Maximum Heat Dissipation:	366.27 gcal/min or 1.4829 BTU/Min
Standard Board, no RAM/EPROM:	186.91 gcal/min or 0.7567 BTU/Min
Operating Temperature Range:	0° to 55° C (32° to 131° F)
Operating Humidity Range:	10% to 85%, non-condensing

* This information was compiled using Intel manufactured memory devices. Consult the data sheet of the memory device being installed for specific information concerning current requirements and access time.

Table 1-2. Memory Device Current Specifications

Device		MAXIMUM ICC (single)	MAXIMUM ICC (x 8)	MAXIMUM ICC (x 16)
2186	(8K x 8 iRAM)	70mA	560mA	1120mA
	(2K x 8 SRAM)*	120mA	960mA	1920mA
2764	(8K x 8 EPROM)	100mA	800mA	1600mA
27128	(16K x 8 EPROM)	150mA	1200mA	2400mA
2817A	(2K x 8 EEPROM)	150mA	1200mA	2400mA
2004X	(512 x 8 NVRAM)	100mA	800mA	1600mA

* This information was compiled using Intel manufactured memory devices. Consult the data sheet of the memory device being installed for specific information concerning current requirements and access time.

***

CHAPTER 2. PREPARATION FOR USE

2.1 INTRODUCTION

This chapter provides instructions for unpacking and inspection and installation considerations. Included in this chapter is information for you to consider before you install the iSBC 428 Universal Site Memory Expansion Board into your system. Using the information in this chapter, you can ascertain the configuration needed to operate this board in your particular application. To completely familiarize yourself with the flexibility of the iSBC 428 board, we recommend reading this chapter and chapter 3 before installation and use.

2.2 UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment contact the Intel Product Service Marketing Administration to obtain a return authorization number and further instructions (see Section 4-2). A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

2.3 INSTALLATION CONSIDERATIONS

There are several general requirements which should be considered prior to board installation and use. These requirements are discussed in the following sections.

2.3.1 MINIMUM OPERATING REQUIREMENTS

The iSBC 428 board standard configuration is described in Chapter 1. In order to operate the board you may need additional equipment. For most applications this will include a chassis with 5-Volt power supply, CPU software residing on ROM/PROM, and the interface connector and cables.

2.3.1.1 Power Requirements

The iSBC 428 board requires +5 VDC. Current requirements are a function of the memory device installed on the board. Table 1-1 provides current requirements for the different devices supported by the iSBC 428 board. Ensure that the power supply in your system has sufficient +5 VDC current capacity to provide the additional load.

2.3.1.2 Cooling Requirements

Operating temperature range for the iSBC 428 board is 0°C to 55°C. Ensure that cooling air is provided such that the ambient air temperature measured 1/16 to 1/4 inch from the component side of the board does not exceed 55°C. If the temperature exceeds 55°C, the expected reliability of the board may decrease.

2.4 SYSTEM CONSIDERATIONS

Before installing the iSBC 428 board, you need to consider the system environment in which the board is to operate. These considerations include the following:

Address allocation - Refer to 2.4.1
Page Select - Refer to 2.4.2
Starting and ending address within the 256K byte page - Refer to 2.4.3
Mode of operation (8-bit only or 8/16-bit transfers) - Refer to 2.4.4
Interface considerations - Refer to 2.4.5
Access time of user-installed devices
Inhibit Signals
Power Fail/Memory Protect - Refer to 2.4.7
Interrupt structure - Refer to 2.4.5

2.4.1 ADDRESS ALLOCATION CONSIDERATIONS

The iSBC 428 board is shipped from the factory with sixteen 28-pin sockets in which various memory devices can be installed. The sixteen sites on the iSBC 428 board are partitioned into two banks of eight sites each. Within each bank the eight sites are further partitioned into two groups of four sites each. Each group of four sites is configurable to each of the five device types via the configurator. This configurator is an arrangement of push-on jumpers which configures each of the four groups of four sites.

The jumper combinations of the iSBC 428 board allow various configurations for the two halves of the two banks. The size and the amount of memory devices installed determine the memory capacity and therefore the addressing range. You need to consider the memory capacity needed for your application. After memory capacity is determined, you need to configure your board for the page desired. Next, you need to configure the board to the starting and ending address within the selected 256K Byte page. Then, you need to configure the board for the type of memory device selected and the amount of memory to be installed on the board.

Within each bank, devices of the same density must reside. Within each group, devices of the same type must reside. If you wish to accept or generate inhibit signals, the iSBC 428 board may be configured for a variety of devices. The banks can contain all RAM, all ROM or a combination of RAM and ROM devices. The memory array can contain up to four different type memory devices, two per each bank. The factory default configuration is for 2K SRAM devices.

2.4.2 PAGE SELECT

The iSBC 428 board is configured at the factory to recognize 64 (0 to 63) separate on-board 256K byte pages as valid memory address ranges. One page per bank. These 64 256K byte pages are jumper selectable. Each of the two banks are independently addressable and can reside in any page. These pages are used to map memory. For example, one page (the top of memory) could be reserved for PROM and the other (bottom of memory) reserved for RAM. The memory portion reserved is jumper selectable. Because of the paging based memory addressing architecture, more than one iSBC 428 board can be placed in a system. Refer to section 3.3.1 for addressing memory jumper information.

2.4.3 STARTING AND ENDING ADDRESS WITHIN THE 256K BYTE PAGE

The starting and ending addresses within a page are a function of the device size and, as with the pages, are determined by jumpers.

You can partition memory from the top of a page down or from the bottom of a page up using the Size Select and Offset jumpers.

For example, suppose your system has 384K of memory beginning at 0 and you want to add 64K bytes of contiguous memory to the system by adding eight 8K devices. The Page Select jumpers can be configured to recognize a 256K byte page beginning at 256K and ending at 512K (referring to Table 3-1, this would be page 1). Because Page 1 begins at 256K (40000H) and you want it to begin at 384K (60000H), you want to offset the starting address by 128K (1FFFFH). (Referring to Table 3-5, configure the jumpers of the iSBC 428 board accordingly.) By configuring the appropriate Size Select and Offset jumpers, you cause the iSBC 428 board to respond to address 60000H (384K) and end with address 6FFFFH (448K).

2.4.4 MODE OF OPERATION

The iSBC 428 board can operate in one of two modes; the 8-bit only mode or the 8/16-bit mode. The iSBC 428 board is factory configured for operation in the 8/16-bit transfer mode. The 8/16-bit mode allows the iSBC 428 board to be compatible with systems employing 8- and 16-bit masters. The mode of operation is selectable by jumpers and is available for both Multibus and iLBX Bus interfaces. If you elect to operate in the 8-bit only mode you need to remove jumper E179 to E180 and reconfigure the address jumpers (E193 through E224) and the jumpers associated with the chip select multiplexers (E43 through E50 for Bank A and E51 through E58 for Bank B).

2.4.5 INTERFACE CONSIDERATIONS

The iSBC 428 board is designed to interface with either the Multibus System bus interface or the faster Intel Local Bus Extension called the iLBX Bus interface. The following sections present information to be considered when interfacing to the iSBC 428 board.

2.4.5.1 MULTIBUS® Interface

The Multibus connector P1 and auxiliary connector P2 interface the iSBC 428 board signals and power lines to the other boards in your system and the power supply. Where applicable, these signals conform to the Intel Multibus Interface standard. All of this interface information is available in the Multibus specification.

2.4.5.2 iLBX™ Interface

The iSBC 428 board can be configured via jumpers to communicate with the iLBX Bus interface. The iLBX Bus connector P2 interfaces the iLBX Master board signals to the iSBC 428 board in your system. Significant memory access time improvements can be realized over the iLBX Bus interface (versus the Multibus interface) due to its dedicated, unarbitrated architecture. The iLBX Bus interface allows selection of either the normal or optimized mode. Where applicable, these signals conform to the Intel iLBX Bus specification. Additional information on the iLBX Bus is available in the iLBX Bus Specification.

2.4.6 COMMAND DELAY

The amount of delay from receipt of a command to the start of the memory cycle is set at the factory for 60ns.

2.4.7 MEMORY ACCESS

The timing of memory access depends on the access time of the user-installed memory device (refer to the component data sheets for the access time of the memory device selected) and on the type of interface used: Multibus or iLBX. The iSBC 428 board has jumper selectable access times which allows the board to be tailored to the performance of the specific devices that are installed on the iSBC 428 board. The board can be configured via jumpers to accept devices with an access range of 50ns to 500ns with a granularity of 50ns. This results in board access times of from 217ns to 687ns. Refer to Table 2-19.

2.4.8 DEVICE CONFIGURATOR

The Device configurator allows the 28-pin sockets to be configured to accept a variety of byte-wide memory devices. This allows installation of two different types of memory devices within the same bank providing they are of the same capacity. For example, you may install 2K SRAM devices into one half of Bank A and 2K EEPROM devices in the other half of Bank A. However, you may not install 2K SRAM devices into one half of Bank A and 4K EEPROM devices in the other half of Bank A.

If it is desirable to mix device sizes in the same bank, you must reprogram the decode PROM device.

2.4.9 INTERRUPTS

The iSBC 428 board has the capability of generating interrupts to the Multibus System bus for the efficient support of EEPROM's. The interrupts can be configured in two ways; one, to signal completion of the EEPROM write cycle, or two, to allow polling by the system to determine the status of the EEPROM during the write programming time.

2.4.10 INHIBITS

Inhibits are provided on the iSBC 428 board to allow ROM to overlay RAM for bootstraping or diagnostic operations. Each bank of the iSBC 428 board can be overlayed using the appropriate jumpers provided on the board.

2.4.11 BATTERY BACKUP

The iSBC 428 board supports battery backup operation via a connector on the board. An auxiliary power bus is provided to allow separate power to the memory array for systems requiring battery backup. Selection of this auxiliary power bus in made via jumpers on the board.

An active-low TTL compatible Memory Protect signal is brought out on the auxiliary connector which, when asserted, disables access to the memory array. This input is provided for the protection of Memory contents during system power-down sequences.

The iSBC 428 board does not support battery backup of iRAM devices.

2.5 FACTORY DEFAULT CONFIGURATION

Table 2-1 lists the factory default jumpers. The iSBC 428 board is shipped from the factory in the following configuration:

1. 80000H Page Address for both banks
2. Bank A Offset from Page Address by 0H
3. Bank B Offset from Page Address by 4000H (16K)
4. 8/16-Bit Transfer Mode
5. 2K SRAM memory devices (32K total memory)
6. 60ns delay from receipt of command to cycle start
7. 250ns access time devices
8. No Inhibit generation or reception
9. No interrupt generation

2.6 JUMPER CONFIGURATIONS

Much of the flexibility of the iSBC 428 board is due to the use of jumper connections which may easily be altered from their factory configurations to suit a particular application. Table 2-2 lists the jumper connections in numerical order.

Table 2-1. Default Jumper List

Number	Description
E9 to E10	Install for any device except iRAM (2186) in Bank B.
E11 to E12	Install for any device except iRAM (2186) in Bank A.
E20 to E23 E24 to E21 E25 to E28 E26 to E29 E27 to E30	These jumpers enable Bank A to be accessed at Page 2 (80000H).

Table 2-1. Default Jumper List (continued)

Number	Description
E31 to E37 E33 to E39 E34 to E40 E35 to E41 E36 to E42	These jumpers enable Bank B to be accessed at Page 2 (80000H).
E43 to E44	This jumper enables the BHE signal to access the Bank A memory devices high order contents when in the 8/16-bit transfer mode.
E47 to E48	This jumper is installed when in the 8/16-bit transfer mode to allow BA0 signal to control the access to the Bank A memory devices low order contents.
E51 to E52	This jumper is installed when in the 8/16-bit transfer mode to allow HEN signal to control the access to the Bank B memory devices high order contents.
E55 to E56	This jumper is installed when in the 8/16-bit transfer mode to allow BA0 signal to control the access to the Bank B memory devices low order contents.
E62 to E66 and E63 to E59	These two jumpers specify that 2K devices are to be installed in Bank A.
E70 to E71	This jumper provides the starting address of 0 and an ending address of 16K (3FFFH) within the selected Page address indicating that the eight 2K devices installed in Bank A will respond to addresses within the range of 80000H to 83FFFH.
E73 to E77 and E74 to E78	These two jumpers specify that 2K devices are to be installed in Bank B.
E84 to E85 and E94 to E95	These jumpers configure the 28-pin sockets in Group 1 of Bank A for SRAM devices.
E99 to E100 and E110 to E109	These jumpers configure the 28-pin sockets in Group 2 of Bank A for SRAM devices.

Table 2-1. Default Jumper List (continued)

Number	Description
E114 to E115 and E124 to E125	These jumpers configure the 28-pin sockets in Group 1 of Bank B for SRAM devices.
E129 to E130 and E139 to E140	These jumpers configure the 28-pin sockets in Group 2 of Bank B for SRAM devices.
E142 to E147 and E143 to E148	Enables XACK/ACK after 3 counts of the counter (approximately 300ns plus command delay).
E163 to E164	This jumper provide the starting address of 16K (4000H) and an ending address of 32K (7FFFH) within the selected Page address indicating that the eight 2K devices installed in Bank B will respond to addresses within the range of 84000H to 87FFFH.
E167 to E172	Routes a clocking signal to the BRDSEL flip/flop after a 60ns delay from receipt of a command (either Multibus or iLBX).
E176 to E177	Routes the 50ns pulse train to the clock input of the counter. Clocks counter every 100ns.
E179 to E180	This enables or disables the appropriate gating signal to the data transceivers (either XHI/ or XLO/ for LBX data transceivers or MHI/ for the Multibus data transceivers for 8/16-bit mode or 8-bit only mode.
E181 to E182	Disables write enable (WE/) at the leading edge of the acknowledge signal (Multibus mode).
E188 to E191	Install to generate the Page B signal in the iLBX mode. (For Multibus mode, install E187 to E188.)
E189 to E192	Install to generate the Page A signal in the iLBX mode. (For Multibus mode, install E189 to E190.)
E209 to E225	Routes Multibus bit A10 from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E210 to E226	Routes Multibus bit AC from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.

Table 2-1. Default Jumper List (continued)

Number	Description
E211 to E227	Routes Multibus bit AA from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E212 to E228	Routes Multibus bit AB from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E213 to E229	Routes Multibus bit A9 from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E214 to E230	Routes Multibus bit AF from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E215 to E231	Routes Multibus bit AE from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E216 to E232	Routes Multibus bit AD from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E217 to E233	Routes Multibus bit A4 from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E218 to E234	Routes Multibus bit A3 from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E219 to E235	Routes Multibus bit A2 from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E220 to E236	Routes Multibus bit A1 from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E221 to E237	Routes Multibus bit A8 from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E222 to E259	Routes Multibus bit A7 from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E223 to E260	Routes Multibus bit A6 from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E224 to E261	Routes Multibus bit A5 from the Multibus Address Buffer to the Address Latch when in the 8/16-bit mode.
E248 to E249	Enables Multibus mode - disables iLBX mode.
E253 to E252	Reserved. Do not remove.
E255 to E256	Reserved. Do not remove.

Table 2-2. Numeric Jumper List

Number	Description
E1 to E5	Install to provide both Ready and not Ready signals from EEPROM devices installed in Bank B at the interrupt jumper matrix.
E2 to E6	Install to provide both Ready and not Ready signals from EEPROM devices installed in Bank A at the interrupt jumper matrix.
E3 to E7	Install to allow iRAM devices installed in Bank B to hold off ACK/XACK while device is in refresh mode.
E4 to E8	Install to allow iRAM devices installed in Bank A to hold off ACK/XACK while device is in refresh mode.
E9 to E10	Install for any device in Bank B except iRAM devices (2186).
E9 to E13	Install to delay the Bank B/ signal for iRAM devices installed in Bank B.
E11 to E12	Install for any device in Bank A except iRAM devices (2186).
E12 to E16	Install to delay the Bank A/ signal for iRAM devices installed in Bank A.
E14 to E17	Install to generate the INH1/ signal with access to devices installed in Bank B.
E15 to E18	Install to generate the INH1/ signal with access to devices installed in Bank A.
E19 through E30	These jumpers select the Page address for the memory devices installed in Bank A. Refer to section 3.3.1.1 and Table 3-1 for specific information.
E31 through E42	These jumpers select the Page address for the memory devices installed in Bank B. Refer to section 3.3.1.1 and Table 3-2 for specific information.
E43 to E44	This jumper is installed when in the 8/16-bit transfer mode to allow HEN signal to control the access to the high order memory devices in Bank A.
E45 to E46	This jumper is installed when in the 8-bit only transfer mode to allow the programmed PROM signals to control the access to the high order memory devices in Bank A .

Table 2-2. Numeric Jumper List (continued)

Number	Description
E49 to E50	This jumper is installed when in the 8-bit only transfer mode to allow the programmed PROM signals to control the access to the low order memory devices in Bank A.
E47 to E48	This jumper is installed when in the 8/16-bit transfer mode to allow BA0 signal to control the access to the low order memory devices in Bank A.
E51 to E52	This jumper is installed when in the 8/16-bit transfer mode to allow HEN signal to control the access to the high order memory devices in Bank B.
E53 to E54	This jumper is installed when in the 8-bit only transfer mode to allow the programmed PROM signals to control the access to the high order memory devices in Bank B.
E55 to E56	This jumper is installed when in the 8/16-bit transfer mode to allow BA0 signal to control the access to the low order memory devices in Bank B.
E57 to E58	This jumper is installed when in the 8-bit only transfer mode to allow the programmed PROM signals to control the access to the low order memory devices in Bank B.
E59 through E66	These jumpers select the size of the memory devices installed. Refer to section 3.3.1.2 and Tables 3-3 through 3-7.
E67 through E72	These jumpers select the offset address within the selected 256K byte page address of Bank A. Refer to section 3.3.1.2 and Tables 3-3 through 3-7.
E73 through E80	These jumpers select the size of the memory devices installed in Bank B. Refer to section 3.3.1.2 and Tables 3-8 through 3-12.
E81 through E95	These are the configurator jumpers for the memory device type installed in the Group 1 sites of Bank A.
E96 through E110	These are the configurator jumpers for the memory device type installed in the Group 2 sites of Bank A.
E111 through E125	These are the configurator jumpers for the memory device type installed in the Group 1 sites of Bank B.

Table 2-2. Numeric Jumper List (continued)

Number	Description
E126 through E140	These are the configurator jumpers for the memory device type installed in the Group 2 sites of Bank B.
E141 to E146	When generating INH1/, this jumper must be installed to ensure that XACK/ is not generated until after the inhibited slave would have generated its normal XACK/ signal.
E142 through E145 and E147 through E150	These jumpers select the delay time to generate the acknowledge signal in accordance with the access time of the devices installed.
E151 to E152	Install to prevent access to devices installed in Bank B when INH1/ is active.
E152 to E153	Install to prevent access to devices installed in Bank B when INH2/ is active.
E154 to E155	Install to prevent access to devices installed in Bank A when INH2/ is active.
E155 to E156	Install to prevent access to devices installed in Bank A when INH1/ is active.
E157 to E158	Install when iRAM devices are installed in either Bank and operating in the iLBX mode only.
E159 through E164	These jumpers select the offset address within the selected 256K byte page address of Bank B. Refer to section 3.3.1.2 and Tables 3-8 through 3-12.
E165 to E170	20 ns delay of command (either Multibus or iLBX). Do not install.
E166 to E171	40 ns delay of command (either Multibus or LBX).
E167 to E172	60ns delay of command (either Multibus or LBX).
E168 to E173	80ns delay of command (either Multibus or LBX).
E169 to E174	Install to delay Write Enable signal when iRAM devices are installed.
E175 to E176	Provides inverted clock edge to counter every 100ns in 50ns increments.
E176 to E177	Provides clock edge to counter every 100ns in 100ns increments.

Table 2-2. Numeric Jumper List (continued)

Number	Description
E179 to E180	Install for operation in the 8/16-bit transfer mode. This controls the appropriate enables to the data transceivers (either XHI/ or XLO/ for iLBX data transceivers or MHI/ for the Multibus data transceivers and swap byte buffer.
E181 to E182	Install to control the trailing edge of the Write Enable (WE/) signal for use in the Multibus Mode.
E182 to E183	Install to control the trailing edge of the Write Enable (WE/) signal for use in the iLBX Mode.
E184 to E185	Install to operate the iSBC 428 board in the iLBX optimized mode.
E185 to E186	Install to operate the iSBC 428 board in the iLBX normal mode.
E187 to E188	Install to generate the Page B signal in the Multibus mode.
E188 to E191	Install to generate the Page B signal in the iLBX mode.
E189 to E190	Install to generate the Page A signal in the Multibus mode.
E189 to E192	Install to generate the Page A signal in the iLBX mode.
E193 to E209	Routes Address bit AF to the Address Buffer when in the 8-bit only Mode.
E194 to E210	Routes Address bit AB to the Address Buffer when in the 8-bit only Mode.
E195 to E211	Routes Address bit A9 to the Address Buffer when in the 8-bit only Mode.
E196 to E212	Routes Address bit AA to the Address Buffer when in the 8-bit only Mode.
E197 to E213	Routes Address bit A8 to the Address Buffer when in the 8-bit only Mode.
E198 to E214	Routes Address bit AE to the Address Buffer when in the 8-bit only Mode.

Table 2-2. Numeric Jumper List (continued)

Number	Description
E199 to E215	Routes Address bit AD to the Address Buffer when in the 8-bit only Mode.
E200 to E216	Routes Address bit AC to the Address Buffer when in the 8-bit only Mode.
E201 to E217	Routes Address bit A3 to the Address Buffer when in the 8-bit only Mode.
E202 to E218	Routes Address bit A2 to the Address Buffer when in the 8-bit only Mode.
E203 to E219	Routes Address bit A1 to the Address Buffer when in the 8-bit only Mode.
E204 to E220	Routes Address bit A0 to the Address Buffer when in the 8-bit only Mode.
E205 to E221	Routes Address bit A7 to the Address Buffer when in the 8-bit only Mode.
E206 to E222	Routes Address bit A6 to the Address Buffer when in the 8-bit only Mode.
E207 to E223	Routes Address bit A5 to the Address Buffer when in the 8-bit only Mode.
E208 to E224	Routes Address bit A4 to the Address Buffer when in the 8-bit only Mode.
E209 to E225	Routes address bit A10 to the Address Buffer when in the 8/16-bit mode.
E210 to E226	Routes address bit AC to the Address Buffer when in the 8/16-bit mode.
E211 to E227	Routes address bit AA to the Address Buffer when in the 8/16-bit mode.
E212 to E228	Routes address bit AB to the Address Buffer when in the 8/16-bit mode.
E213 to E229	Routes address bit A9 to the Address Buffer when in the 8/16-bit mode.
E214 to E230	Routes address bit AF to the Address Buffer when in the 8/16-bit mode.

Table 2-2. Numeric Jumper List (continued)

Number	Description
E215 to E231	Routes address bit AE to the Address Buffer when in the 8/16-bit mode.
E216 to E232	Routes address bit AD to the Address Buffer when in the 8/16-bit mode.
E217 to E233	Routes address bit A4 to the Address Buffer when in the 8/16-bit mode.
E218 to E234	Routes address bit A3 to the Address Buffer when in the 8/16-bit mode.
E219 to E235	Routes address bit A2 to the Address Buffer when in the 8/16-bit mode.
E220 to E236	Routes address bit A1 to the Address Buffer when in the 8/16-bit mode.
E221 to E237	Routes address bit A8 to the Address Buffer when in the 8/16-bit mode.
E222 to E259	Routes address bit A7 to the Address Buffer when in the 8/16-bit mode.
E223 to E260	Routes address bit A6 to the Address Buffer when in the 8/16-bit mode.
E224 to E261	Routes address bit A5 to the Address Buffer when in the 8/16-bit mode.
E238	Provides ready signal for EEPROM devices to the interrupt jumper matrix (jumpers 240 through 247) for interrupt level 7 through 0, respectively.
E239	Provides a not ready signal for EEPROM devices to the interrupt jumper matrix (jumpers 240 through 247) for interrupt level 7 through 0, respectively.
E248 to E249	Enables Multibus mode - disables iLBX mode.
E253 to E252	Reserved. Do not remove.
E255 to E256	Reserved. Do not remove.

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CHAPTER 3. PREPARING YOUR BOARD FOR INSTALLATION

3.1 INTRODUCTION

This chapter provides a functional overview of the iSBC 428 Universal Site Memory Expansion Board and gives specific information enabling you to configure and install the iSBC 428 board into your system. The board's default or factory configuration and other variables are described, followed by information needed to alter the default configuration. Using the information in this chapter, you can configure this board for a variety of applications. To completely familiarize yourself with the flexibility of the iSBC 428 board, we recommend reading the entire chapter before installation and use.

3.2 OVERVIEW OF BOARD OPERATION

This section provides an overview of the operation of the iSBC 428 board. It is intended to familiarize you with the flexibility of the iSBC 428 board and the role of the different jumpers.

The processor board within your system communicates with the iSBC 428 Universal Site Memory Expansion Board by placing the address of the memory location on the address lines and issuing the appropriate command (either a read or write). The iSBC 428 board interfaces the processor board via either the Multibus System bus or the iLBX Bus. Thus, the iSBC 428 board includes two sets of address buffers. The Multibus Address Buffers accept addresses via the P1 connector. Appendix A contains the interface signal information. The iLBX Bus Address Buffers accept addresses via the P2 connector. With the appropriate Address Buffers enabled, the Address Latch receives the outputs from the selected Address buffers. (If the iLBX interface is used, the Address Strobe signal strobes the address lines.) Upon receipt of the command, the iSBC 428 board delays the start of the memory access cycle. This allows time to decode the address in order to determine the bank and the memory device to be accessed.

The memory location accessed depends on the selectable configuration of four sets of jumpers: the page select jumpers, the size select jumpers, the offset jumpers, and the configuration jumpers.

The Page Select Logic receives the six highest address bits (A12 through A17) where they are exclusively NOR*ed with the state of two sets of Page Select jumpers. Each Page Select jumper set consists of six jumpers which determine the address range of a particular Bank: Bank A or Bank B. The Page Select Logic defines one of 64 256K byte pages. If the address inputs match the jumper inputs, signals Page A and/or Page B are asserted.

Each bank has its own chip select logic to access a specific location within the memory array of the addressed bank. A decode PROM (one for each bank) receives address bits AB through A11 and the state of four Size Select jumpers. These four jumpers define the size of the installed memory devices (or the block size of the bank). In conjunction with the memory size jumpers, the state of four Offset jumpers (connected to the output of the decode PROM) define the offset address within the block or the starting and ending address within the selected 256K byte page. The memory map of the decode PROM is given in Appendix C.

The configurator jumpers select the memory device type (EPROM, EEPROM, SRAM, iRAM, or NVRAM) to be installed in four of the sixteen device sites. There are four configurator jumper sets - two sets per bank. Each set of configurator jumpers define one half of a bank (four memory devices). Appendix E list the jumpering required to install iRAM devices. Appendix F list the special jumpers required to install EEPROM devices.

When the address sent from the processor to the iSBC 428 board is within the range selected by the page and block jumpers, the decode PROM creates the appropriate output to enable the chip select signals to access the specific location within the memory array.

During a read operation, the iSBC 428 board's data transceivers transmit the data from the addressed memory location to the selected interface (either Multibus or iLBX Bus). A Programmable Array Logic (PAL) element controls the data transceivers to permit either the 8-bit only data transfers or the 8/16-bit data transfers. (The PAL equations are listed in Appendix D.) The transceivers provide the proper data flow paths including the required byte swapping.

During a write operation, the data transceivers transmit the write data from the selected interface (either Multibus or iLBX Bus) to the memory location specified. The Programmable Array Logic (PAL) element controls the direction of data transferred through the data transceivers. The transceivers provide the proper data flow paths including the required byte swapping for 8-bit only transfers as well as the 8/16-bit transfers.

The iSBC 428 board generates an acknowledge signal back to the system to indicate completion of the requested operation. The time delay in generating the acknowledge signal (XACK/ for the Multibus interface or the ACK/ signal for the iLBX interface) is jumper selectable to closely match the access time of the memory devices installed.

3.3 CONFIGURING YOUR BOARD

The following sections provide the jumpering information needed to configure the iSBC 428 board to suit your particular application.

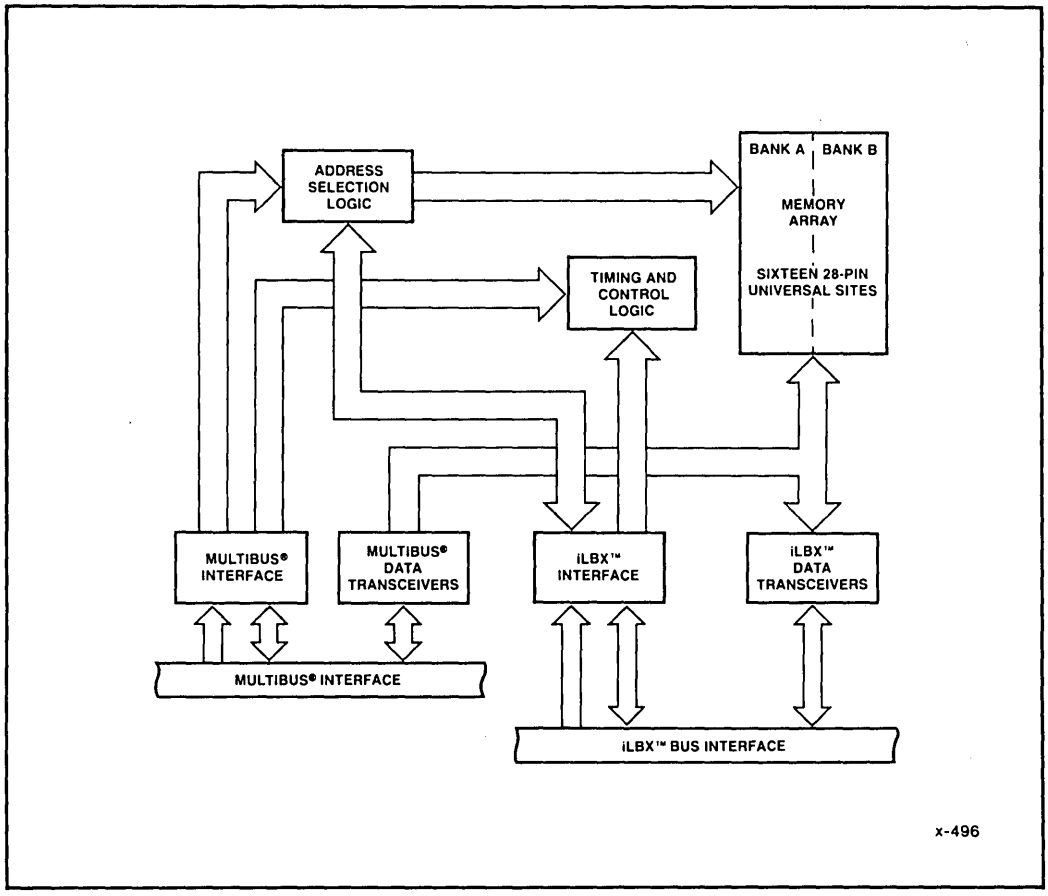


Figure 3-1. iSBC® 428 Board Functional Block Diagram

3.3.1 ADDRESSING

The iSBC 428 board is jumper selectable for a variety of addressing schemes. The size of the memory devices installed determine the address range. The size and offset within the selected range determine the memory location itself. Thus, the memory location accessed depends on the selectable configuration of four sets of jumpers; the Page Select jumpers, the Size Select jumpers, the Offset jumpers, and the Configurator jumpers.

The configurator jumpers select the memory device type (EPROM, EEPROM, SRAM, iRAM, or NVRAM) to be installed.

The page select jumpers select a particular 256K byte page within the full 16M byte address space.

The size select jumpers select the size of the memory devices to be installed (and the block size of the bank).

The offset jumpers select the starting address within the block of the selected 256K byte page.

First, determine the address range for each bank. This determines the Page Select jumper configurations within the 16M byte address range. Turn to section 3.3.1.1 to obtain the Page Select jumper information and jumper the board accordingly. Then, determine the size of the memory devices to be installed (2K, 4K, 8K etc.). Turn to section 3.3.1.2 to obtain the Size Select and Offset jumper information and configure the board accordingly. Next, determine the type of device to be installed. This determines the Configurator jumpers. Turn to section 3.3.1.3 to obtain the Configurator jumper information and configure the board accordingly.

3.3.1.1 Page Select Jumpers

This section provides the information needed to configure the Page Select jumpers for each bank of the iSBC 428 board.

The iSBC 428 board has two separately addressable memory banks; Bank A and Bank B. There are two sets (six jumpers per set) of Page Select jumpers that assign the address range of these two memory banks. The Bank A Page Select jumpers are E19 through E30; the Bank B Page Select jumpers are E31 through E42. Each set of Page Select jumpers defines one of 64 256K Byte pages. You can assign each bank a different page or assign the same page to both banks. First, determine the address range of each bank, go to the appropriate table for that bank, find the jumpers listed for the desired address range, and then, reconfigure your board. Table 3-1 lists the jumper configurations for the different pages of the memory devices installed in Bank A. Table 3-2 lists the jumper configurations for the different pages of the memory devices installed in Bank B.

Table 3-1. Bank A Page Addressing

Address Range	Page	E27-E30	E20-E23	E26-E29	E25-E28	E19-E22	E21-E24
000000-03FFFF	0	IN	IN	IN	IN	IN	IN
040000-07FFFF	1	IN	IN	IN	IN	IN	OUT
080000-0BFFFF	2	IN	IN	IN	IN	OUT	IN
0C0000-0FFFFF	3	IN	IN	IN	IN	OUT	OUT
100000-13FFFF	4	IN	IN	IN	OUT	IN	IN
140000-17FFFF	5	IN	IN	IN	OUT	IN	OUT
180000-1BFFFF	6	IN	IN	IN	OUT	OUT	IN
1C0000-1FFFFF	7	IN	IN	IN	OUT	OUT	OUT
200000-23FFFF	8	IN	IN	OUT	IN	IN	IN
240000-27FFFF	9	IN	IN	OUT	IN	IN	OUT
280000-2BFFFF	10	IN	IN	OUT	IN	OUT	IN
2C0000-2FFFFF	11	IN	IN	OUT	IN	OUT	OUT
300000-33FFFF	12	IN	IN	OUT	OUT	IN	IN
340000-37FFFF	13	IN	IN	OUT	OUT	IN	OUT
380000-3BFFFF	14	IN	IN	OUT	OUT	OUT	IN
3C0000-3FFFFF	15	IN	IN	OUT	OUT	OUT	OUT
400000-43FFFF	16	IN	OUT	IN	IN	IN	IN
440000-47FFFF	17	IN	OUT	IN	IN	IN	OUT
480000-4BFFFF	18	IN	OUT	IN	IN	OUT	IN
4C0000-4FFFFF	19	IN	OUT	IN	IN	OUT	OUT
500000-53FFFF	20	IN	OUT	IN	OUT	IN	IN
540000-57FFFF	21	IN	OUT	IN	OUT	IN	OUT
580000-5BFFFF	22	IN	OUT	IN	OUT	OUT	IN
5C0000-5FFFFF	23	IN	OUT	IN	OUT	OUT	OUT
600000-63FFFF	24	IN	OUT	OUT	IN	IN	IN
640000-67FFFF	25	IN	OUT	OUT	IN	IN	OUT
680000-6BFFFF	26	IN	OUT	OUT	IN	OUT	IN
6C0000-6FFFFF	27	IN	OUT	OUT	IN	OUT	OUT
700000-73FFFF	28	IN	OUT	OUT	OUT	IN	IN
740000-77FFFF	29	IN	OUT	OUT	OUT	IN	OUT
780000-7BFFFF	30	IN	OUT	OUT	OUT	OUT	IN
7C0000-7FFFFF	31	IN	OUT	OUT	OUT	OUT	OUT
800000-83FFFF	32	OUT	IN	IN	IN	IN	IN
840000-87FFFF	33	OUT	IN	IN	IN	IN	OUT
880000-8BFFFF	34	OUT	IN	IN	IN	OUT	IN
8C0000-8FFFFF	35	OUT	IN	IN	IN	OUT	OUT
900000-93FFFF	36	OUT	IN	IN	OUT	IN	IN
940000-97FFFF	37	OUT	IN	IN	OUT	IN	OUT
980000-9BFFFF	38	OUT	IN	IN	OUT	OUT	IN
9C0000-9FFFFF	39	OUT	IN	IN	OUT	OUT	OUT
A00000-A3FFFF	40	OUT	IN	OUT	IN	IN	IN
A40000-A7FFFF	41	OUT	IN	OUT	IN	IN	OUT
A80000-ABFFFF	42	OUT	IN	OUT	IN	OUT	IN
AC0000-AFFFFF	43	OUT	IN	OUT	IN	OUT	OUT
B00000-B3FFFF	44	OUT	IN	OUT	OUT	IN	IN
B40000-B7FFFF	45	OUT	IN	OUT	OUT	IN	OUT
B80000-BBFFFF	46	OUT	IN	OUT	OUT	OUT	IN

Table 3-1. Bank A Page Addressing (continued)

Address Range	Page	E27-E30	E20-E23	E26-E29	E25-E28	E19-E22	E21-E24
BC0000-BFFFFF	47	OUT	IN	OUT	OUT	OUT	OUT
C00000-C3FFFF	48	OUT	OUT	IN	IN	IN	IN
C40000-C7FFFF	49	OUT	OUT	IN	IN	IN	OUT
C80000-CBFFFF	50	OUT	OUT	IN	IN	OUT	IN
CC0000-CFFFFF	51	OUT	OUT	IN	IN	OUT	OUT
D00000-D3FFFF	52	OUT	OUT	IN	OUT	IN	IN
D40000-D7FFFF	53	OUT	OUT	IN	OUT	IN	OUT
D80000-DBFFFF	54	OUT	OUT	IN	OUT	OUT	IN
DC0000-DFFFFF	55	OUT	OUT	IN	OUT	OUT	OUT
E00000-E3FFFF	56	OUT	OUT	OUT	IN	IN	IN
E40000-E7FFFF	57	OUT	OUT	OUT	IN	IN	OUT
E80000-EBFFFF	58	OUT	OUT	OUT	IN	OUT	IN
EC0000-EFFFFF	59	OUT	OUT	OUT	IN	OUT	OUT
F00000-F3FFFF	60	OUT	OUT	OUT	OUT	IN	IN
F40000-F7FFFF	61	OUT	OUT	OUT	OUT	IN	OUT
F80000-FBFFFF	62	OUT	OUT	OUT	OUT	OUT	IN
FC0000-FFFFFF	63	OUT	OUT	OUT	OUT	OUT	OUT

Table 3-2. Bank B Page Addressing

Address Range	Page	E33-E39	E31-E37	E34-E40	E35-E41	E32-E38	E36-E42
000000-03FFFF	0	IN	IN	IN	IN	IN	IN
040000-07FFFF	1	IN	IN	IN	IN	IN	OUT
080000-0BFFFF	2	IN	IN	IN	IN	OUT	IN
0C0000-0FFFFF	3	IN	IN	IN	IN	OUT	OUT
100000-13FFFF	4	IN	IN	IN	OUT	IN	IN
140000-17FFFF	5	IN	IN	IN	OUT	IN	OUT
180000-1BFFFF	6	IN	IN	IN	OUT	OUT	IN
1C0000-1FFFFF	7	IN	IN	IN	OUT	OUT	OUT
200000-23FFFF	8	IN	IN	OUT	IN	IN	IN
240000-27FFFF	9	IN	IN	OUT	IN	IN	OUT
280000-2BFFFF	10	IN	IN	OUT	IN	OUT	IN
2C0000-2FFFFF	11	IN	IN	OUT	IN	OUT	OUT
300000-33FFFF	12	IN	IN	OUT	OUT	IN	IN
340000-37FFFF	13	IN	IN	OUT	OUT	IN	OUT
380000-3BFFFF	14	IN	IN	OUT	OUT	OUT	IN
3C0000-3FFFFF	15	IN	IN	OUT	OUT	OUT	OUT
400000-43FFFF	16	IN	OUT	IN	IN	IN	IN
440000-47FFFF	17	IN	OUT	IN	IN	IN	OUT
480000-4BFFFF	18	IN	OUT	IN	IN	OUT	IN
4C0000-4FFFFF	19	IN	OUT	IN	IN	OUT	OUT
500000-53FFFF	20	IN	OUT	IN	OUT	IN	IN
540000-57FFFF	21	IN	OUT	IN	OUT	IN	OUT
580000-5BFFFF	22	IN	OUT	IN	OUT	OUT	IN
5C0000-5FFFFF	23	IN	OUT	IN	OUT	OUT	OUT
600000-63FFFF	24	IN	OUT	OUT	IN	IN	IN
640000-67FFFF	25	IN	OUT	OUT	IN	IN	OUT
680000-6BFFFF	26	IN	OUT	OUT	IN	OUT	IN
6C0000-6FFFFF	27	IN	OUT	OUT	IN	OUT	OUT
700000-73FFFF	28	IN	OUT	OUT	OUT	IN	IN
740000-77FFFF	29	IN	OUT	OUT	OUT	IN	OUT
780000-7BFFFF	30	IN	OUT	OUT	OUT	OUT	IN
7C0000-7FFFFF	31	IN	OUT	OUT	OUT	OUT	OUT
800000-83FFFF	32	OUT	IN	IN	IN	IN	IN
840000-87FFFF	33	OUT	IN	IN	IN	IN	OUT
880000-8BFFFF	34	OUT	IN	IN	IN	OUT	IN
8C0000-8FFFFF	35	OUT	IN	IN	IN	OUT	OUT
900000-93FFFF	36	OUT	IN	IN	OUT	IN	IN
940000-97FFFF	37	OUT	IN	IN	OUT	IN	OUT
980000-9BFFFF	38	OUT	IN	IN	OUT	OUT	IN
9C0000-9FFFFF	39	OUT	IN	IN	OUT	OUT	OUT
A00000-A3FFFF	40	OUT	IN	OUT	IN	IN	IN
A40000-A7FFFF	41	OUT	IN	OUT	IN	IN	OUT
A80000-ABFFFF	42	OUT	IN	OUT	IN	OUT	IN
AC0000-AFFFFF	43	OUT	IN	OUT	IN	OUT	OUT
B00000-B3FFFF	44	OUT	IN	OUT	OUT	IN	IN
B40000-B7FFFF	45	OUT	IN	OUT	OUT	IN	OUT
B80000-BBFFFF	46	OUT	IN	OUT	OUT	OUT	IN
BC0000-BFFFFF	47	OUT	IN	OUT	OUT	OUT	OUT

Table 3-2. Bank B Page Addressing (continued)

Address Range	Page	E33-E39	E31-E37	E34-E40	E35-E41	E32-E38	E36-E42
C00000-C3FFFF	48	OUT	OUT	IN	IN	IN	IN
C40000-C7FFFF	49	OUT	OUT	IN	IN	IN	OUT
C80000-CBFFFF	50	OUT	OUT	IN	IN	OUT	IN
CC0000-CFFFFF	51	OUT	OUT	IN	IN	OUT	OUT
D00000-D3FFFF	52	OUT	OUT	IN	OUT	IN	IN
D40000-D7FFFF	53	OUT	OUT	IN	OUT	IN	OUT
D80000-DBFFFF	54	OUT	OUT	IN	OUT	OUT	IN
DC0000-DFFFFF	55	OUT	OUT	IN	OUT	OUT	OUT
E00000-E3FFFF	56	OUT	OUT	OUT	IN	IN	IN
E40000-E7FFFF	57	OUT	OUT	OUT	IN	IN	OUT
E80000-EBFFFF	58	OUT	OUT	OUT	IN	OUT	IN
EC0000-EFFFFF	59	OUT	OUT	OUT	IN	OUT	OUT
F00000-F3FFFF	60	OUT	OUT	OUT	OUT	IN	IN
F40000-F7FFFF	61	OUT	OUT	OUT	OUT	IN	OUT
F80000-FBFFFF	62	OUT	OUT	OUT	OUT	OUT	IN
FC0000-FFFFFF	63	OUT	OUT	OUT	OUT	OUT	OUT

3.3.1.2 Size Select And Offset Jumpers

This section provides the information needed to configure the Size Select and Offset jumpers for each bank of the iSBC 428 board.

Together, the Size Select and Offset jumpers define the starting and ending address within the selected 256K Byte page.

The Size Select jumpers (E59 through E66 for Bank A or E73 through E80 for Bank B) allow you to select the size of memory devices installed. The factory default is for 2K SRAM devices (E62 to E66 and E59 to E63 installed in Bank A and E73 to E77 and E74 to E78 installed in Bank B).

The Offset jumpers (E67 through E72 for Bank A and E159 through E164 for Bank B) allow you to select the specific offset block within the 256K Byte page you have selected.

Addressing within a particular bank is accomplished with the decode PROM. The inputs to this decode PROM include address bits AB through A11 and four Size Select jumpers. These four Size Select jumper inputs provide 16 different combinations of different size memory devices on a variety of address boundaries. The four Offset jumpers provide further configurability to offset the starting address by 0, 2, 4, or 8 times the device size. Refer to Table 3-3. For example, if the Size Select jumpers are set for 2K byte memory devices one possible range of offset addressing is as follows:

0 times 2K = 0 to 16K Offset from Page address
2 times 2K = 4K to 20K Offset from Page address
4 times 2K = 8K to 24K Offset from Page address
8 times 2K = 16K to 32K offset from Page address

This assumes that all sites within the addressed bank are fully populated with the appropriate device size (in this example - 2K devices).

Tables 3-3 and 3-8 list the jumpers involved in setting up the starting and ending offset addresses within the selected page for 2K memory devices installed in Banks A and B, respectively.

Tables 3-4 and 3-9 list the jumpers to configure the starting and ending offset addresses within the selected page for 4K memory devices for Banks A and B, respectively.

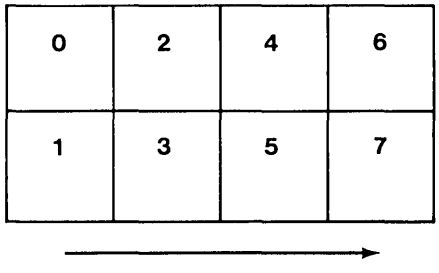
Tables 3-5 and 3-10 list the jumpers to configure the starting and ending offset addresses within the selected page for 8K memory devices for Banks A and B, respectively.

Tables 3-6 and 3-11 list the jumpers to configure the starting and ending offset addresses within the selected page for 16K memory devices for Banks A and B, respectively.

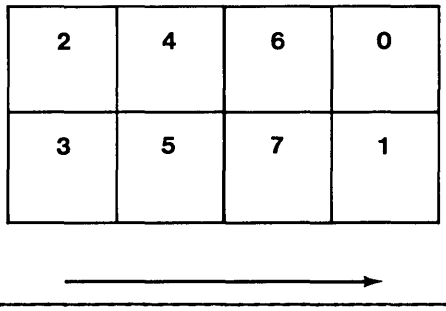
Tables 3-7 and 3-12 list the jumpers to configure the starting and ending offset addresses within the selected page for 32K memory devices for Banks A and B, respectively.

When using the offset jumpers to offset the starting and ending address within a selected block, remember to place your programmed PROM devices in the proper positions within the array. Refer to section 3.3.1.2.

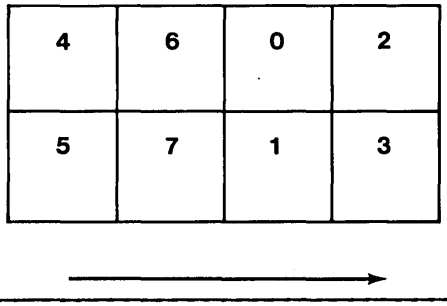
If you use the "0" offset jumper starting at a low address in memory and proceeding to a high address in memory, the access sequence to the addressed memory locations in the 8/16-bit mode start with chip selects 0 and 1, 2 and 3, 4 and 5, 6 and 7. In the 8-bit only mode, the chip select sequence is 0, 1, 2, 3, 4, 5, 6, and 7.



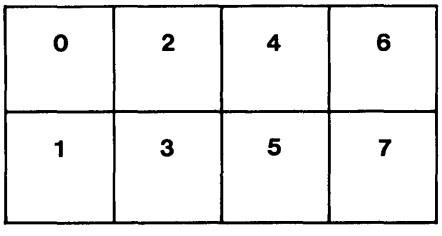
If you use the "2" offset jumper starting at a low address in memory and proceeding to a high address in memory, access to the memory locations in the 8/16-bit mode start with chip selects 2 and 3, followed by 4 and 5, 6 and 7 and 0 and 1. In the 8-bit only mode, the chip select sequence is 2, 3, 4, 5, 6, 7, 0 and 1.



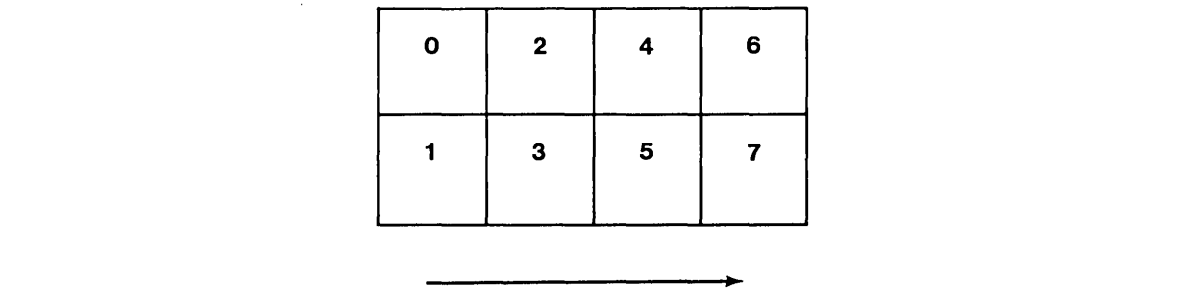
If you use the "4" offset jumper starting at a low address in memory and proceeding to a high address in memory, access to the memory locations in the 8/16-bit mode start with chip selects 4 and 5, followed by 6 and 7, 0 and 1, and 2 and 3. In the 8-bit only mode, the chip select sequence is 4, 5, 6, 7, 0, 1, 2 and 3.



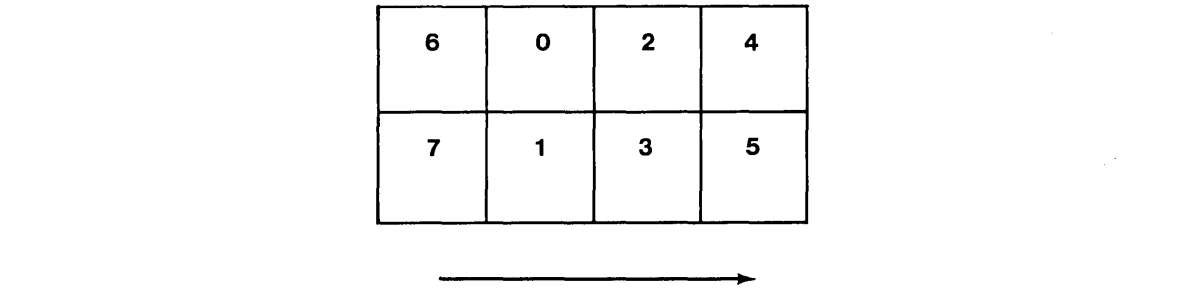
If you use the "8" offset jumper starting at a low address in memory and proceeding to a high address in memory, access to the memory locations in the 8/16-bit mode start with chip selects 0 and 1, followed by 2 and 3, 4 and 5, and 6 and 7. In the 8-bit only mode, the chip select sequence is 0, 1, 2, 3, 4, 5, 6 and 7.



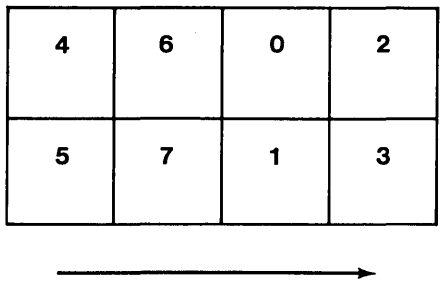
If you use the "0" offset jumper starting at a high address in memory and proceeding downward to a low address in memory, the access sequence to the addressed memory locations in the 8/16-bit mode start with chip selects 0 and 1, 2 and 3, 4 and 5, 6 and 7. In the 8-bit only mode, the chip select sequence is 0, 1, 2, 3, 4, 5, 6, and 7.



If you use "2" offset jumper starting at a high address in memory and proceeding downward to a low address in memory, access to the memory locations in the 8/16-bit mode start with chip selects 6 and 7, followed by 0 and 1, 2 and 3, and 4 and 5. In the 8-bit only mode, the chip select sequence is 6, 7, 0, 1, 2, 3, 4 and 5.



If you use "4" offset starting at a high address in memory and proceeding downward to a low address in memory, access to the memory locations in the 8/16-bit mode start with chip selects 4 and 5, followed by 6 and 7, 0 and 1, and 2 and 3. In the 8-bit only mode, the chip select sequence is 4, 5, 6, 7, 0, 1, 2 and 3.



If you use "8" offset starting at a high address in memory and proceeding downward to a low address in memory, access to the memory locations in the 8/16-bit mode start with chip selects 0 and 1, followed by 2 and 3, 4 and 5, and 6 and 7. In the 8-bit only mode, the chip select sequence is 0, 1, 2, 3, 4 and 5, 6 and 7.

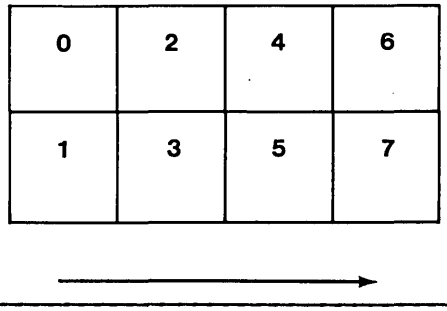


Table 3-3. 2K Devices In Bank A

Size Select Jumpers				Offset Jumpers				Address		Starting Address Socket Location
				0	2	4	8			
60 to 64	61 to 65	62 to 66	59 to 63	70 to 71	67 to 68	68 to 69	71 to 72	Starting	Ending	
0	0	I	I	I	0	0	0	0	16K	5P/3P
0	0	I	I	0	I	0	0	4K	20K	5N/3N
0	0	I	I	0	0	I	0	8K	24K	5M/3M
0	0	I	I	0	0	0	I	16K	32K	5P/3P
0	0	I	0	I	0	0	0	16K	32K	5P/3P
0	0	I	0	0	I	0	0	20K	36K	5N/3N
0	0	I	0	0	0	I	0	24K	40K	5M/3M
0	0	I	0	0	0	0	I	32K	48K	5P/3P
0	0	0	I	0	0	0	I	208K	224K	5P/3P
0	0	0	I	0	0	I	0	216K	232K	5M/3M
0	0	0	I	0	I	0	0	220K	236K	5K/3K
0	0	0	I	I	0	0	0	224K	240K	5P/3P
0	0	0	0	0	0	0	I	224K	240K	5P/3P
0	0	0	0	0	0	I	0	232K	248K	5M/3M
0	0	0	0	0	I	0	0	236K	252K	5K/3K
0	0	0	0	I	0	0	0	240K	256K	5P/3P

I - indicates jumper to be installed
0 - indicates jumper to be removed

Table 3-4. 4K Devices In Bank A

Size Select Jumpers				Offset Jumpers				Address		Starting Address Socket Location
				0	2	4	8			
60 to 64	61 to 65	62 to 66	59 to 63	70 to 71	67 to 68	68 to 69	71 to 72	Starting	Ending	
0	I	I	I	I	0	0	0	0	32K	5P/3P
0	I	I	I	0	I	0	0	8K	40K	5N/3N
0	I	I	I	0	0	I	0	16K	48K	5M/3M
0	I	I	I	0	0	0	I	32K	64K	5P/3P
0	I	I	0	I	0	0	0	32K	64K	5P/3P
0	I	I	0	0	I	0	0	40K	72K	5N/3N
0	I	I	0	0	0	I	0	48K	80K	5M/3M
0	I	I	0	0	0	0	I	64K	96K	5P/3P
0	I	0	I	0	0	0	I	160K	192K	5P/3P
0	I	0	I	0	0	I	0	176K	208K	5M/3M
0	I	0	I	0	I	0	0	184K	216K	5K/3K
0	I	0	I	I	0	0	0	192K	224K	5P/3P
0	I	0	0	0	0	0	I	192K	224K	5P/3P
0	I	0	0	0	0	I	0	208K	240K	5M/3M
0	I	0	0	0	I	0	0	216K	248K	5K/3K
0	I	0	0	I	0	0	0	224K	256K	5P/3P

I - indicates jumper to be installed
0 - indicates jumper to be removed

Table 3-5. 8K Devices In Bank A

Size Select Jumpers				Offset Jumpers				Address		Starting Address Socket Location
				0	2	4	8			
60 to 64	61 to 65	62 to 66	59 to 63	70 to 71	67 to 68	68 to 69	71 to 72	Starting	Ending	
I	0	I	I	I	0	0	0	0	64K	5P/3P
I	0	I	I	0	I	0	0	16K	80K	5N/3N
I	0	I	I	0	0	I	0	32K	96K	5M/3M
I	0	I	I	0	0	0	I	64K	128K	5P/3P
I	0	I	0	I	0	0	0	64K	128K	5P/3P
I	0	I	0	0	I	0	0	80K	144K	5N/3N
I	0	I	0	0	0	I	0	96K	160K	5M/3M
I	0	I	0	0	0	0	I	128K	192K	5P/3P
I	0	0	I	0	0	0	I	64K	128K	5P/3P
I	0	0	I	0	0	I	0	96K	160K	5M/3M
I	0	0	I	0	I	0	0	112K	176K	5K/3K
I	0	0	I	I	0	0	0	128K	192K	5P/3P
I	0	0	0	0	0	0	I	128K	192K	5P/3P
I	0	0	0	0	0	I	0	160K	224K	5M/3M
I	0	0	0	0	I	0	0	176K	240K	5K/3K
I	0	0	0	I	0	0	0	192K	256K	5P/3P

I - indicates jumper to be installed
0 - indicates jumper to be removed

Table 3-6. 16K Devices In Bank A

Size Select Jumpers				Offset Jumpers				Address		Starting Address Socket Location
				0	2	4	8			
60 to 64	61 to 65	62 to 66	59 to 63	70 to 71	67 to 68	68 to 69	71 to 72	Starting	Ending	
I	I	0	I	I	0	0	0	0	128K	5P/3P
I	I	0	I	0	I	0	0	32K	160K	5N/3N
I	I	0	I	0	0	I	0	64K	192K	5M/3M
I	I	0	I	0	0	0	I	128K	256K	5P/3P
I	I	0	0	0	0	0	I	0	128K	5P/3P
I	I	0	0	0	0	I	0	64K	192K	5M/3M
I	I	0	0	0	I	0	0	96K	224K	5K/3K
I	I	0	0	I	0	0	0	128K	256K	5P/3P

I - indicates jumper to be installed
0 - indicates jumper to be removed

Table 3-7. 32K Devices In Bank A

Size Select Jumpers				Offset Jumpers				Address		Starting Address Socket Location
				0	2	4	8			
60 to 64	61 to 65	62 to 66	59 to 63	70 to 71	67 to 68	68 to 69	71 to 72	Starting	Ending	
I	I	I	0	I	0	0	0	0	256K	5P/3P
I	I	I	0	0	I	0	0	0	256K	5P/3P
I	I	I	0	0	0	I	0	0	256K	5P/3P
I	I	I	0	0	0	0	I	0	256K	5P/3P

I - indicates jumper to be installed
0 - indicates jumper to be removed

Table 3-8. 2K Devices In Bank B

Size Select Jumpers				Offset Jumpers				Address		Starting Address Socket Location
				0	2	4	8			
76 to 80	75 to 79	74 to 78	73 to 77	162 to 163	159 to 160	160 to 161	163 to 164	Starting	Ending	
0	0	I	I	I	0	0	0	0	16K	5J/3J
0	0	I	I	0	I	0	0	4K	20K	5H/3H
0	0	I	I	0	0	I	0	8K	24K	5E/3E
0	0	I	I	0	0	0	I	16K	32K	5J/3J
0	0	I	0	I	0	0	0	16K	32K	5J/3J
0	0	I	0	0	I	0	0	20K	36K	5H/3H
0	0	I	0	0	0	I	0	24K	40K	5E/3E
0	0	I	0	0	0	0	I	32K	48K	5J/3J
0	0	0	I	0	0	0	I	208K	224K	5J/3J
0	0	0	I	0	0	I	0	216K	232K	5D/3D
0	0	0	I	0	I	0	0	220K	236K	5E/3E
0	0	0	I	I	0	0	0	224K	240K	5J/3J
0	0	0	0	0	0	0	I	224K	240K	5J/3J
0	0	0	0	0	0	I	0	232K	248K	5D/3D
0	0	0	0	0	I	0	0	236K	252K	5E/3E
0	0	0	0	I	0	0	0	240K	256K	5J/3J

I - indicates jumper to be installed
0 - indicates jumper to be removed

Table 3-9. 4K Devices In Bank B

Size Select Jumpers				Offset Jumpers				Address		Starting Address Socket Location
				0	2	4	8			
76 to 80	75 to 79	74 to 78	73 to 77	162 to 163	159 to 160	160 to 161	163 to 164	Starting	Ending	
0	I	I	I	I	0	0	0	0	32K	5J/3J
0	I	I	I	0	I	0	0	8K	40K	5H/3H
0	I	I	I	0	0	I	0	16K	48K	5E/3E
0	I	I	I	0	0	0	I	32K	64K	5J/3J
0	I	I	0	I	0	0	0	32K	64K	5J/3J
0	I	I	0	0	I	0	0	40K	72K	5H/3H
0	I	I	0	0	0	I	0	48K	80K	5E/3E
0	I	I	0	0	0	0	I	64K	96K	5J/3J
0	I	0	I	0	0	0	I	160K	192K	5J/3J
0	I	0	I	0	0	I	0	176K	208K	5D/3D
0	I	0	I	0	I	0	0	184K	216K	5E/3E
0	I	0	I	I	0	0	0	192K	224K	5J/3J
0	I	0	0	0	0	0	I	192K	224K	5J/3J
0	I	0	0	0	0	I	0	208K	240K	5D/3D
0	I	0	0	0	I	0	0	216K	248K	5E/3E
0	I	0	0	I	0	0	0	224K	256K	5J/3J

I - indicates jumper to be installed
0 - indicates jumper to be removed

Table 3-10. 8K Devices In Bank B

Size Select Jumpers				Offset Jumpers				Address		Starting Address Socket Location
				0	2	4	8			
76 to 80	75 to 79	74 to 78	73 to 77	162 to 163	159 to 160	160 to 161	163 to 164	Starting	Ending	
I	0	I	I	I	0	0	0	0	64K	5J/3J
I	0	I	I	0	I	0	0	16K	80K	5H/3H
I	0	I	I	0	0	I	0	32K	96K	5E/3E
I	0	I	I	0	0	0	I	64K	128K	5J/3J
I	0	I	0	I	0	0	0	64K	128K	5J/3J
I	0	I	0	0	I	0	0	80K	144K	5H/3H
I	0	I	0	0	0	I	0	96K	160K	5E/3E
I	0	I	0	0	0	0	I	128K	192K	5J/3J
I	0	0	I	0	0	0	I	64K	128K	5J/3J
I	0	0	I	0	0	I	0	96K	160K	5D/3D
I	0	0	I	0	I	0	0	112K	176K	5E/3E
I	0	0	I	I	0	0	0	128K	192K	5J/3J
I	0	0	0	0	0	0	I	128K	192K	5J/3J
I	0	0	0	0	0	I	0	160K	224K	5D/3D
I	0	0	0	0	I	0	0	176K	240K	5E/3E
I	0	0	0	I	0	0	0	192K	256K	5J/3J

I - indicates jumper to be installed
0 - indicates jumper to be removed

Table 3-11. 16K Devices In Bank B

Size Select Jumpers				Offset Jumpers				Address		Starting Address Socket Location
				0	2	4	8			
76 to 80	75 to 79	74 to 78	73 to 77	162 to 163	159 to 160	160 to 161	163 to 164	Starting	Ending	
I	I	0	I	I	0	0	0	0	128K	5J/3J
I	I	0	I	0	I	0	0	32K	160K	5H/3H
I	I	0	I	0	0	I	0	64K	192K	5E/3E
I	I	0	I	0	0	0	I	128K	256K	5J/3J
I	I	0	0	0	0	0	I	0	128K	5J/3J
I	I	0	0	0	0	I	0	64K	192K	5D/3D
I	I	0	0	0	I	0	0	96K	224K	5E/3E
I	I	0	0	I	0	0	0	128K	256K	5J/3J

I - indicates jumper to be installed
0 - indicates jumper to be removed

Table 3-12. 32K Devices In Bank B

Size Select Jumpers				Offset Jumpers				Address		Starting Address Socket Location
				0	2	4	8			
76 to 80	75 to 79	74 to 78	73 to 77	162 to 163	159 to 160	160 to 161	163 to 164	Starting	Ending	
I	I	I	0	I	0	0	0	0	256K	5J/3J
I	I	I	0	0	I	0	0	0	256K	5J/3J
I	I	I	0	0	0	I	0	0	256K	5J/3J
I	I	I	0	0	0	0	I	0	256K	5J/3J

I - indicates jumper to be installed
0 - indicates jumper to be removed

3.3.1.3 Configurator Jumpers

The Configurator block allows the 28-pin sockets to be configured to accept a variety of byte-wide memory devices. Two configurator blocks per bank permit you to install two different types of memory devices within the same bank providing they have the same capacity. For example, you may install 2K SRAM devices into one half of Bank A and 2K EEPROM devices in the other half of Bank A. However, you may not install 2K SRAM devices into one half of Bank A and 4K EEPROM devices in the other half of Bank A. That is unless you reprogram the decode PROM device.

The Configurator jumpers associated with Group 1 of Bank A (refer to Figure 3-7) are E81 through E95. The Configurator jumpers associated with Group 2 of Bank A are E96 through E110. The Configurator jumpers associated with Group 1 of Bank B are E111 through E125. The Configurator jumpers associated with Group 2 of Bank B are E126 through E140. Tables 3-13 and 3-14 lists the Configurator jumpers for the memory devices supported in Bank A and Bank B, respectively. Figure 3-2 through 3-6 show the layout of the configurator block and the jumper placement when installing SRAM, iRAM, EPROM, EEPROM and NVRAM devices.

Table 3-13. Device Configurator For Bank A

Device Type	Bank	Group	Jumper
EPROM 2K x 8 (2716)	A	1	E94 to E95 E93 to E85
		2	E110 to E109 E108 to E100
EPROM 4K x 8 (2732)	A	1	E94 to E95 E86 to E85
		2	E109 to E110 E100 to E101
EPROM 8K x 8 (2764)	A	1	E81 to EE88 E85 to E86 E92 to E93
		2	E96 to E103 E100 to E101 E107 to E108

Table 3-13. Device Configurator For Bank A (continued)

Device Type	Bank	Group	Jumper
EPROM 16K x 8 (27128)	A	1	E81 to E88 E85 to E86 E87 to E95 E92 to E93
		2	E96 to E103 E100 to E101 E102 to E110 E107 to E108
EPROM 32K x 8 (27256)	A	1	E81 to E88 E85 to E86 E87 to E95 E91 to E92
		2	E96 to E103 E100 to E101 E102 to E110 E106 to E107
EEPROM 2K x 8 (2817A)	A	1	E81 to E82 E84 to E92
		2	E96 to E97 E99 to E107
EEPROM 8K x 8	A	1	E81 to E82 E84 to E92 E85 to E86
		2	E96 to E97 E99 to E107 E100 to E101

Table 3-13. Device Configurator For Bank A (continued)

Device Type	Bank	Group	Jumper
SRAM 2K x 8	A	1	E84 to E85 E94 to E95
		2	E99 to E100 E109 to E110
SRAM 8K x 8	A	1	E89 to E92 E85 to E86
		2	E99 to E107 E100 to E101
SRAM 16K x 8	A	1	E84 to E92 E85 to E86 E87 to E95
		2	E99 to E107 E100 to E101 E102 to E110
SRAM 32K x 8	A	1	E84 to E92 E85 to E86 E87 to E95 E90 to E91
		2	E99 to E107 E100 to E101 E102 to E110 E105 to E106
iRAM 8K x 8* (2186)	A	1	E81 to E82 E84 to E92 E85 to E86
		2	E96 to E97 E99 to E107 E100 to E101

* Refer to Appendix E for additional information on iRAM configuration.

Table 3-13. Device Configurator For Bank A (continued)

Device Type	Bank	Group	Jumper
iRAM 16K x 8*	A	1	E81 to E82 E84 to E92 E85 to E86 E87 to E95
		2	E96 to E97 E99 to E107 E100 to E101 E102 to E110
NVRAM 512 x 8 (2004X), 1K x 8, 2K x 8	A	1	E84 to E92 E83 to E90
		2	E99 to E107 E98 to E105
NVRAM 4K x 8, 8K x 8,	A	1	E84 to E92 E83 to E90 E85 to E86
		2	E99 to E107 E98 to E105 E100 to E101
* Refer to Appendix E for additional information on iRAM configuration.			

Table 3-14. Device Configurator For Bank B

Device Type	Bank	Group	Jumper
EPROM 2K x 8 (2716)	B	1	E124 to E125 E115 to E123
		2	E139 to E140 E130 to E138
EPROM 4K x 8 (2732)	B	1	E124 to E125 E115 to E116
		2	E139 to E140 E130 to E131
EPROM 8K x 8 (2764)	B	1	E111 to E118 E115 to E116 E122 to E123
		2	E126 to E133 E130 to E131 E137 to E138
EPROM 8K x 8 (27128)	B	1	E111 to E118 E115 to E116 E117 to E125 E122 to E123
		2	E126 to E133 E130 to E131 E132 to E140 E137 to E138
EPROM 16K x 8 (27256)	B	1	E111 to E118 E115 to E116 E117 to E125 E121 to E122
		2	E126 to E133 E130 to E131 E132 to E140 E136 to E137

Table 3-14. Device Configurator For Bank B (continued)

Device Type	Bank	Group	Jumper
EEPROM 2K x 8 (2817A)	B	1	E111 to E112 E114 to E122
		2	E126 to E127 E129 to E137
EEPROM 8K x 8	B	1	E111 to E112 E114 to E122 E115 to E116
		2	E126 to E127 E129 to E137 E130 to E131
SRAM 2K x 8	B	1	E114 to E115 E124 to E125
		2	E129 to E130 E139 to E140
SRAM 8K x 8	B	1	E114 to E122 E115 to E116
		2	E129 to E137 E130 to E131
SRAM 16K x 8	B	1	E114 to E122 E115 to E116 E117 to E125
		2	E129 to E137 E130 to E131 E132 to E140
SRAM 32K x 8	B	1	E114 to E122 E115 to E116 E117 to E125 E120 to E121

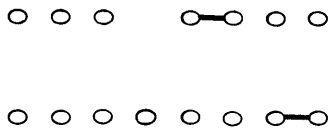
Table 3-14. Device Configurator For Bank B (continued)

Device Type	Bank	Group	Jumper
		2	E129 to E137 E130 to E131 E132 to E140 E135 to E136
iRAM 8K x 8* (2186)	B	1	E111 to E112 E114 to E122 E115 to E116
		2	E126 to E127 E129 to E137 E130 to E131
iRAM 16K x 8*	B	1	E111 to E112 E114 to E122 E115 to E116 E117 to E125
		2	E126 to E127 E129 to E137 E130 to E131 E132 to E140
NVRAM 512 x 8 (2004X), 1K x 8, 2K x 8	B	1	E114 to E122 E113 to E120
		2	E129 to E137 E128 to E135
NVRAM 4K x 8, 8K x 8	B	1	E114 to E122 E113 to E120 E115 to E116
		2	E129 to E137 E128 to E135 E130 to E131

* Refer to Appendix E for additional information on iRAM configuration.

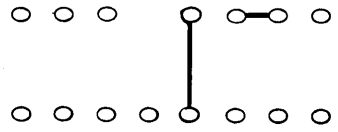
2k x 8 Static RAM — **Jumper Matrix Configuration**

Pin 1 n/c
Pin 27 n/c
Pin 26 Vcc
Pin 23 WE/



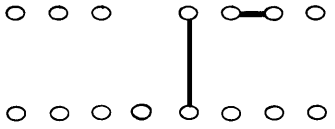
4k x 8 Static RAM — **Jumper Matrix Configuration**

Pin 1 n/c
Pin 27 WE/
Pin 26 n/c
Pin 23 A11



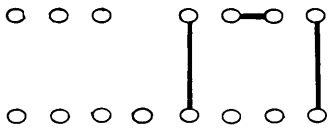
8k x 8 Static RAM — **Jumper Matrix Configuration**

Pin 1 n/c
Pin 27 WE/
Pin 26 n/c
Pin 23 A11



16k x 8 Static RAM — **Jumper Matrix Configuration**

Pin 1 n/c
Pin 27 WE/
Pin 26 A13
Pin 23 A11



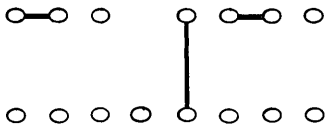
1381

Figure 3-2. Jumper Matrix Configurations For SRAM Devices

8k x 8 iRAM (example 2186)*

Jumper Matrix Configuration

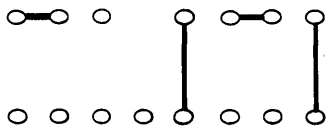
Pin 1 RDY
Pin 27 WE/
Pin 26 n/c
Pin 23 A11



16k x 8 iRAM*

Jumper Matrix Configuration

Pin 1 RDY
Pin 27 WE/
Pin 26 n/c
Pin 23 A11



1382

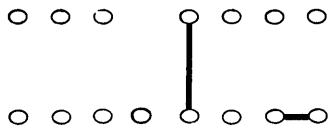
* Refer to Appendix E for additional information on iRAM configuration.

Figure 3-3. Jumper Matrix Configurations For iRAM Devices

2k x 8 EPROM (example 2716)

Jumper Matrix Configuration

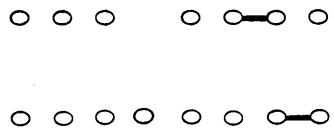
Pin 1 n/c
Pin 27 n/c
Pin 26 Vcc
Pin 23 Vcc/Vpp



4k x 8 EPROM (example 2732A)

Jumper Matrix Configuration

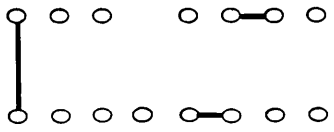
Pin 1 n/c
Pin 27 n/c
Pin 26 Vcc
Pin 23 A11



8k x 8 EPROM (example 2764)

Jumper Matrix Configuration

Pin 1 Vcc/Vpp
Pin 27 Vcc/PGM
Pin 26 n/c
Pin 23 A11



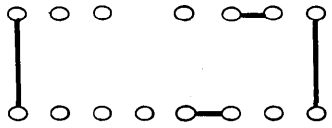
1383

Figure 3-4. Jumper Matrix Configurations For EPROM Devices

16k x 8 EPROM (example 27128)

Jumper Matrix Configuration

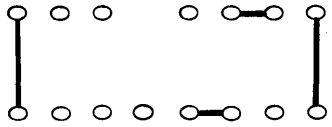
Pin 1 Vcc/Vpp
Pin 27 Vcc/PGM
Pin 26 A13
Pin 23 A11



32k x 8 EPROM (example 27256)

Jumper Matrix Configuration

Pin 1 Vcc/Vpp
Pin 27 A14
Pin 26 A13
Pin 23 A11

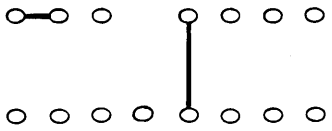


1383

Figure 3-4. Jumper Matrix Configurations For EPROM Devices (continued)

2k x 8 EEPROM

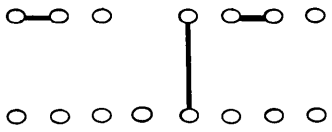
Jumper Matrix Configuration



Pin 1	**RDY**
Pin 27	**WE/**
Pin 26	**n/c**
Pin 23	**n/c**

8k x 8 EEPROM

Jumper Matrix Configuration



Pin 1	**RDY**
Pin 27	**WE/**
Pin 26	**n/c**
Pin 23	**A11**

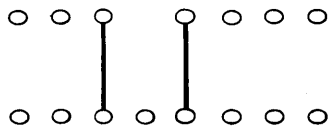
1384

Figure 3-5. Jumper Matrix Configurations For EEPROM Devices

512 x 8 NVRAM
1K x 8 NVRAM
2k x 8 NVRAM

Jumper Matrix Configuration

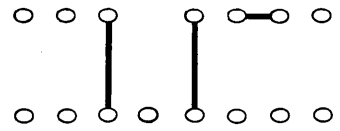
Pin 1	**NE/**
Pin 27	**WE/**
Pin 26	**n/c**
Pin 23	**n/c**



4k x 8 NVRAM

Jumper Matrix Configuration

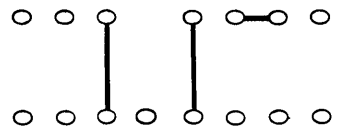
Pin 1	**NE/**
Pin 27	**WE/**
Pin 26	**n/c**
Pin 23	**A11**



8k x 8 NVRAM

Jumper Matrix Configuration

Pin 1	**NE/**
Pin 27	**WE/**
Pin 26	**n/c**
Pin 23	**A11**



1385

Figure 3-6. Jumper Matrix Configurations For NVRAM Devices

3.3.2 DATA TRANSFER MODE

This section provides the information needed to configure the Data Transfer mode of the iSBC 428 board. The iSBC 428 board is factory configured for operation in the 8/16-bit transfer mode.

The iSBC 428 board can operate in the 8-bit only transfer mode or the 8/16-bit transfer mode. The outputs from either of the Address Buffers (Multibus and iLBX) are jumper selectable to the Address Latch. The Address Latch receives address bits A0 through AF in the 8-bit only mode or address bits A1 through A10 in the 8/16-bit mode. The Address jumpers associated with the 8-bit Only transfer are E193 through E224. The jumpers associated with the 8/16-bit transfer mode are E209 through E237 and E259 through E261.

Two signals control the type of Data transfer. Byte High Enable (BHEN in the iLBX mode or BHEN/ in the Multibus mode) and address bit 0 (ABD0 in the iLBX mode or ADR0 in the Multibus mode). The four signal level combinations of these two lines specify the type of data transfer that takes place. These combinations are shown in Table 3-15. (Refer to Figure 4-3 sheets 5 and 6.)

Table 3-15. Data Transfer

iLBX™			MULTIBUS®		
BHEN	ABD0	Transfer	BHEN/	ADR0/	Transfer
1	1	High Byte	0	1	High Byte
0	0	Low Byte	0	0	Low Byte
1	0	Word	1	0	Word

Low byte transfers on the Multibus occur across Data lines DAT0/ through DAT7/.

High byte transfers on the Multibus are swapped from the high byte to Data lines DAT0/ through DAT7/.

Word transfers on the Multibus occur with the Low byte on DAT0/ through DAT7/ and high byte on DAT8/ through DAT15/.

Low byte transfers on the iLBX bus occur across Data lines DB0 through DB7.

High byte transfers on the iLBX bus occur across Data lines DB8 through DBF.

Word transfers on the iLBX bus occur with the Low byte on DB0 through DB7 and the high byte on Data lines DB8 through DBF.

3.3.2.1 8-Bit Only Mode

To operate in the 8-bit only mode, you need to remove jumper E179 to E180, reconfigure the address jumpers (E193 through E224), and reconfigure the jumpers associated with the chip select multiplexers (E43 through E50 for Bank A and E51 through E58 for Bank B). Table 3-16 lists the jumper configuration for the 8-bit only mode.

3.3.2.2 8/16-Bit Mode

Table 3-17 lists the jumpers required for the 8/16-bit transfer mode. For 16-bit (word) transfers, signal BHEN/ is active and signal BA0 is inactive. The low (even) byte is transferred across data lines DAT0/ through DAT7/ (Multibus mode) or DB0 through DB7 (iLBX mode) and the high (odd) byte is transferred across data lines DAT8/ through DATF/ (Multibus mode) or DB8 through DBF (iLBX mode).

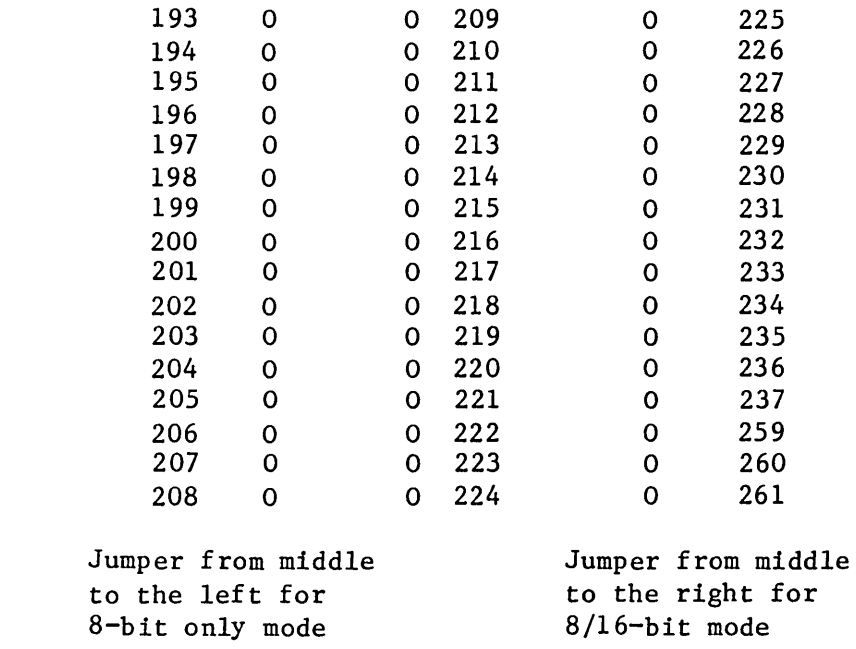


Figure 3-7. Address Mode

Table 3-16. 8-Bit Only Transfer Mode

Jumper	Function
E45 to E46	Allows the programmed PROM to control the access (generate the appropriate chip select signals) for the high order memory devices in Bank A.
E49 to E50	Allows the programmed PROM to control the access (generate the appropriate chip select signals) for the low order memory devices in Bank A.
E53 to E54	Allows the programmed PROM to control the access (generate the appropriate chip select signals) for the high order memory devices in Bank B.
E57 to E58	Allows the programmed PROM to control the access (generate the appropriate chip select signals) for the low order memory devices in Bank B.
E179 to E180	This jumper must be removed.
E193 to E209	Routes Address bit AF to the Address Buffer when in the 8-bit only Mode.
E194 to E210	Routes Address bit AB to the Address Buffer when in the 8-bit only Mode.
E195 to E211	Routes Address bit A9 to the Address Buffer when in the 8-bit only Mode.
E196 to E212	Routes Address bit AA to the Address Buffer when in the 8-bit only Mode.
E197 to E213	Routes Address bit A8 to the Address Buffer when in the 8-bit only Mode.
E198 to E214	Routes Address bit AE to the Address Buffer when in the 8-bit only Mode.
E199 to E215	Routes Address bit AD to the Address Buffer when in the 8-bit only Mode.
E200 to E216	Routes Address bit AC to the Address Buffer when in the 8-bit only Mode.
E201 to E217	Routes Address bit A3 to the Address Buffer when in the 8-bit only Mode.
E202 to E218	Routes Address bit A2 to the Address Buffer when in the 8-bit only Mode.

Table 3-16. 8-Bit Only Transfer Mode (continued)

Jumper	Function
E203 to E219	Routes Address bit A1 to the Address Buffer when in the 8-bit only Mode.
E204 to E220	Routes Address bit A0 to the Address Buffer when in the 8-bit only Mode.
E205 to E221	Routes Address bit A7 to the Address Buffer when in the 8-bit only Mode.
E206 to E222	Routes Address bit A6 to the Address Buffer when in the 8-bit only Mode.
E207 to E223	Routes Address bit A5 to the Address Buffer when in the 8-bit only Mode.
E208 to E224	Routes Address bit A4 to the Address Buffer when in the 8-bit only Mode.

Table 3-17. 8/16-Bit Transfer Mode

Jumper	Function
E43 to E44	This jumper enables the BHE signal to control access to the Bank A memory devices high order contents.
E47 to E48	This jumper enables the BA0 signal to control access to the Bank A memory devices low order contents.
E51 to E52	This jumper enables the HEN signal to control access to the Bank B memory devices high order contents.
E55 to E56	This jumper enables the BA0 signal to control access to the Bank B memory devices low order contents.
E179 to E180	Controls the 8/16-bit mode for the PAL. This jumper must be installed for the 8/16-bit mode.
E209 to E225	Routes Address bit A10 to the Address Buffer when in the 8-bit only Mode.
E210 to E226	Routes Address bit AC to the Address Buffer when in the 8-bit only Mode.

Table 3-17. 8/16-Bit Transfer Mode (continued)

Jumper	Function
E211 to E227	Routes Address bit AA to the Address Buffer when in the 8-bit only Mode.
E212 to E228	Routes Address bit AB to the Address Buffer when in the 8-bit only Mode.
E213 to E229	Routes Address bit A9 to the Address Buffer when in the 8-bit only Mode.
E214 to E230	Routes Address bit AF to the Address Buffer when in the 8-bit only Mode.
E215 to E231	Routes Address bit AE to the Address Buffer when in the 8-bit only Mode.
E216 to E232	Routes Address bit AD to the Address Buffer when in the 8-bit only Mode.
E217 to E233	Routes Address bit A4 to the Address Buffer when in the 8-bit only Mode.
E218 to E234	Routes Address bit A3 to the Address Buffer when in the 8-bit only Mode.
E219 to E235	Routes Address bit A2 to the Address Buffer when in the 8-bit only Mode.
E220 to E236	Routes Address bit A1 to the Address Buffer when in the 8-bit only Mode.
E221 to E237	Routes Address bit A8 to the Address Buffer when in the 8-bit only Mode.
E222 to E259	Routes Address bit A7 to the Address Buffer when in the 8-bit only Mode.
E223 to E260	Routes Address bit A6 to the Address Buffer when in the 8-bit only Mode.
E224 to E261	Routes Address bit A5 to the Address Buffer when in the 8-bit only Mode.

3.3.3 INTERFACE MODE

This section provides information needed to configure the interface mode of the iSBC 428 board. The iSBC 428 board is jumper selectable to operate in either the Multibus mode or the iLBX mode. The factory default configuration is the Multibus mode. Table 3-18 lists the jumpers required for each interface mode.

Table 3-18. Interface Mode Jumper Information

Jumper	MULTIBUS®	iLBX™
E248 to E249	IN	OUT
E181 to E182	IN	OUT
E182 to E183	OUT	IN
E189 to E190	IN	OUT
E187 to E188	IN	OUT
E189 to E192	OUT	IN
E188 to E191	OUT	IN
E184 to E185	OUT	IN*
E185 to E186	OUT	IN*
* Install E184 to E185 for Optimized Mode, E185 to E186 for Normal Mode.		

3.3.3.1 MULTIBUS® Mode

The default configuration of the iSBC 428 board is a mix of iLBX and Multibus modes as defined by four jumpers - E248 to E249, E181 to E182, E188 to E191 and E189 to E192. If you elect to operate the iSBC 428 board in the Multibus mode, you need to remove jumpers E188 to E191 amd E189 to E192 and install jumpers E187 to E188 and E189 to E190. However, if the board was configured for the iLBX mode and you decide to reconfigure the board to operate in the Multibus mode, you need to change the following jumpers. Install jumper E248 to E249 to enable the Multibus command receiver and the Multibus Address buffers. Removal of this jumper disables the Multibus command and Address buffers. (Refer to Figure 4-2 sheet 3.) Note that only one set of Address buffers can be enabled at a time. If the board operated in the normal iLBX mode, remove jumper E186 to E185. If the board operated in the optimized iLBX mode, remove jumper E184 to E185 instead of E184 to E185. Remove jumper E182 to E183 and install jumper E181 to E182.

3.3.3.2 iLBX™ Mode

If you elect to operate the iSBC 428 board in the iLBX mode, you need to reconfigure your board. Remove jumper E248 to E249 to enable the iLBX Address Buffers. Remove jumper E181 to E182 and install jumper E182 to E183 to control the trailing edge of WE/. Install jumper E185 to E186 to start the normal cycle from the Data Strobe. If you want the optimized mode of the iLBX, install jumper E184 to E185.

3.3.4 ACCESS TIME

This section provides the information needed to configure the access time of the iSBC 428 board. This access time is the delay encountered from receipt of the command from the processor board until the iSBC 428 board generates the acknowledge signal. This delay is the result of the type of memory devices installed and the interface mode. The access time includes the memory cycle delay and the acknowledge delay.

The iSBC 428 board generates the acknowledge signal back to the system processor board to indicate completion of the requested operation. Upon receipt of the command from the processor board, the iSBC 428 board delays the start of the memory cycle. The delayed command clocks the board select (BRDSEL) flip-flop. The output from the BRDSEL flip-flop initiates a series of 50ns pulses causing the counter to count. The counter output is jumper selectable to match the access time of the user-installed memory devices. The selected access time as defined by the jumpers are ANDed and routed to the acknowledge latch. The next edge of the clock after the selected count clocks the acknowledge flip-flop and generates the acknowledge signal back to the processor board. Therefore, the time delay in generating the acknowledge signal (XACK/ for the Multibus interface or the ACK/ signal for the iLBX interface) is jumper selectable to closely match the access time of the different memory devices.

3.3.4.1 Memory Cycle Delay

The Memory Cycle delay is required in order to compensate for address decode delays and is accomplished by a delay line. The installation of the default jumper E167 to E173 provides a 60ns delay time.

3.3.4.2 Acknowledge Delay

The Acknowledge delay time is jumper selectable and is directly related to the access time of the user-installed memory devices.

In the Multibus mode and the iLBX mode, the acknowledge signal (XACK/ for Multibus and ACK for iLBX mode) is generated on the following clock edge after the acknowledge counter reaches its jumpered count (factory configured for 200ns devices by installing jumpers E142 to E147 and E143 to E148 and E176 to E177).

In the Multibus mode, data must be valid on the bus when XACK/ is generated by the iSBC 428 board. In the iLBX optimized or normal mode, ACK/ can be asserted and driven onto the bus prior to valid data on the bus. In this case, the iSBC 428 board may be jumpered to generate a pre-acknowledge signal. If you wish to generate a pre-acknowledge signal, you must ensure that data is valid prior to the time that the data is sampled by the iLBX master. This time is given in the hardware reference manual of the particular LBX master board as ACK/ to Data Sample time.

To configure the iSBC 428 board acknowledge circuitry, first, find the access time required by consulting the data sheet for the memory devices to be installed. If in the Multibus mode, refer to Table 3-19 to determine the acknowledge delay time.

Table 3-19. MULTIBUS® XACK/

Memory Device T_{ACC}	Maximum ADDR/ to Data Valid*	Minimum time CMD to XACK/	Jumpers
50	200	217	E175 to E176, E143 to E148
100	250	262	E176 to E177, E143 to E148
120	270	311	E175 to E176, E142 to E147, E143 to E148
150	300	311	E175 to E176, E142 to E147, E143 to E148
200	350	356	E176 to E177, E142 to E147, E143 to E148
250	400	405	E175 to E176, E144 to E149
300	450	450	E176 to E177, E144 to E149
350	500	544	E176 to E177, E142 to E147, E144 to E149
400	550	593	E175 to E176, E143 to E148, E144 to E149
450	600	638	E176 to E177, E143 to E148, E144 to E149
500	650	687	E175 to E176, E142 to E147, E143 to E148, E144 to E149

*Assumes minimum Multibus specification T_{AS}.

In the iLBX normal mode, data valid time is a function of the delay between ASTB/ and DSTB/. With masters that separate ASTB/ and DSTB/ by some delay, calculate the maximum data valid time using the following equation:

$$T_{ADV} = 105 + T_{CE} + T_X*$$

Where: $T_X = T_{AD} + 156 + T_{OE} - (105 + T_{CE})$

T_{ADV} = ASTB/ to Data valid (maximum)
T_{AD} = ASTB/ to DSTB/ time of iLBX Master (maximum)
T_{OE} = memory device output enable to data valid time
T_{CE} = memory device chip enable to data valid time

* Disregard T_X in calculation if a negative number.

Example: A 200ns SRAM with the following specifications is used: T_{CE} = 200ns, T_{OE} = 75ns, T_{AD} = 85ns.

$T_X = 85 + 156 + 75 - (105 + 200) = 11ns.$

$T_{ADV} = 105 + T_{CE} + 11ns = 316ns.$

Once the maximum data valid time is found and no pre-acknowledge is desired, jumper the board to give an acknowledge time that is nearest to but greater than the calculated T_{ADV}. Thus, for the calculated time of 316ns in the above example, you should use ASTB/ to ACK/ time of 356 (as listed in Table 3-20) and configure the jumpers accordingly.

However, if you wish to pre-acknowledge you must know the minimum ACK/ to data sample time of the iLBX master being used. This number is subtracted from the maximum T_{ADV} calculated above to derive a minimum ASTB/ to ACK/ time. Jumper the iSBC 428 board to generate an acknowledge that is closest to but greater than the calculated minimum ASTB/ to ACK/ time. Referring to the above example and using an iLBX master with an ACK/ to data sample time of 80ns minimum gives:

316 - 80 = 236ns for minimum ASTB/ to ACK/.

Therefore, choosing the closest jumperable option from Table 3-20 that is greater than 236 means that the iSBC 428 board should be set for an ASTB/ to ACK/ time of 262ns (E176 to E177 and E143 to E148).

Table 3-20. Minimum ACK/ Options

Minimum Time ASTB/ or DSTB/ to ACK/	Jumpers
74	E176 to E177
123	E175 to E176, E142 to E147
168	E176 to E177, E142 to E147
217	E175 to E176, E143 to E148
262	E176 to E177, E143 to E148
311	E175 to E176, E142 to E147, E143 to E148
356	E176 to E177, E142 to E147, E143 to E148
405	E175 to E176, E144 to E149
450	E175 to E176, E144 to E149
499	E176 to E177, E142 to E147, E144 to E149
544	E176 to E177, E142 to E147, E144 to E149
593	E175 to E176, E143 to E148, E144 to E149
638	E176 to E177, E143 to E148, E144 to E149
687	E175 to E176, E142 to E147, E143 to E148, E144 to E149
732	E176 to E177, E142 to E147, E143 to E148, E144 to E149

If in the iLBX optimized mode, consult the data sheet for the memory devices being installed and then refer to Table 3-21 to determine the maximum data valid time. If you wish to pre-acknowledge and you know the acknowledge to data sample time for the master board being used, subtract that time from the ASTB/ to Data valid time listed in Table 3-21 and configure the jumpers on the board for the appropriate minimum ACK/ time as listed in Table 3-20.

Table 3-21. ASTB/ to Data Valid iLBX™ Optimized Mode

Memory Device T_{ACC}	100	120	150	200	250	300	400	450	500
ASTB/ to Data Valid (Maximum)	205	225	255	305	355	405	455	555	605

NOTE

The acknowledge delay must be jumpered for the slowest memory device installed in either bank.

3.3.4.3 Write Enable

The leading edge of the Write Enable (WE/) signal is generated after the BRDSEL signal becomes active on a write cycle.

When the iSBC 428 board is in the Multibus mode, the trailing edge of the WE/ signal is controlled by the acknowledge flip-flop which terminates the WE/ pulse upon the assertion of acknowledge. If you are operating the iSBC 428 board in the Multibus mode, install a jumper from E181 to E182.

When the iSBC 428 board is in the iLBX mode, the trailing edge of the WE/ signal is controlled directly by the rising edge of the DSTB/ signal. If your operating the iSBC 428 board in the iLBX mode, install a jumper from E182 to E183.

3.3.5 INTERRUPTS

The interrupt jumper matrix provides the capability of jumpering a buffered ARDY/BRDY signal to the Multibus interrupt request lines INT0/ through INT7/. Normally, this circuitry is used when programming EEPROMs that support a READY/BUSY pin. This READY signal from the EEPROM device is jumpered through the Configurator block to the interrupt matrix by installing jumper E2 to E6 (ARDY) or E1 to E5 (BRDY). Refer to Figure 4-3 sheet 2. Jumpering E239 to any of the interrupt request lines provide a means for a poll type of interrupt and reflects a direct buffered copy of the ARDY/BRDY signal. This signal is low for the entire write programming time (not ready) of the particular EEPROM device. Jumpering E238 to any of the interrupt request lines provide a ready interrupt that occurs when the particular EEPROM device completes its write cycle (refer to Table 3-22). Any subsequent read to the iSBC 428 board clears the interrupt. When 24-pin EEPROM devices are installed, special jumpering is required. Refer to Appendix F for 24-pin jumper information.

Table 3-22. Interrupt Jumper Information

Jumper	Function
E238	Ready Interrupt.
E239	Not Ready Interrupt.
E240	Interrupt INT 7/.
E241	Interrupt INT 6/.
E242	Interrupt INT 5/.
E243	Interrupt INT 4/.
E244	Interrupt INT 3/.
E245	Interrupt INT 2/.
E246	Interrupt INT 1/.
E247	Interrupt INT 0/.

3.3.6 INHIBIT SUPPORT

The iSBC 428 board supports both INH1/ and INH2/ as described in the Multibus specification. Bank A and Bank B both have the capability to listen to INH1/ or INH2/ and also to generate INH1/. However, you should not jumper the board to listen to INH1/ on one bank if you are going to generate INH1/ on the other bank. INH1/ is used to inhibit access to a bank that has RAM memory devices installed. If INH1/ is generated by either bank of the iSBC 428 board, then the acknowledge time delay must be extended to encompass the acknowledge that would have been generated by the inhibited slave. This is done by installing jumper E141 to E146. Table 3-23 lists the inhibit jumpers.

Table 3-23. Inhibit Jumpering

Jumper	Function
E14 to E17	Generate INH1/ from Bank B
E15 to E18	Generate INH1/ from Bank A
E154 to E155	Inhibit access to Bank A when INH2/ is generated
E152 to E153	Inhibit access to Bank B when INH2/ is generated
E155 to E156	Inhibit access to Bank A when INH1/ is generated
E151 to E152	Inhibit access to Bank B when INH1/ is generated

3.3.7 BATTERY BACKUP

A Battery backup provision is incorporated into the iSBC 428 board to preserve memory during an AC power failure. Install wire jumpers between W1 and W2 and connect a +5 Volt battery positive lead to auxiliary connector J1 pin 1 and negative lead to auxiliary connector J1 pin 2. In order for the battery backup scheme to function, the power supply used in your system must provide signal MPRO/. This signal must be asserted at least 50 microseconds before DC voltages are lost. When MPRO (Memory Protect) signal is asserted, all access to the memory devices are inhibited.

The iSBC 428 board does not support Battery backup of iRAM devices (2186).

3.4 INSTALLATION

Installation consists of installing the selected memory devices onto the board. Once all the jumpers and components have been installed and the connectors to implement your system requirements are determined, install the iSBC 428 board in place within your system chassis.

Instructions for installing these items are provided in the following sections. Before installing these items, the appropriate jumper connections must be made. Physical location of jumper posts on the board are shown in Figure 4-2. Jumper connections are also shown schematically in Figure 4-3.

3.4.1 MEMORY DEVICE INSTALLATION

Sockets 5P, 5N, 5M, 5K, 3P, 3N, 3M, 3K are reserved for memory devices installed in Bank A. (Refer to Figure 3-8.) Sockets 5J, 5H, 5E, 5D, 3J, 3H, 3E, and 3D are reserved for memory devices installed in Bank B. Each memory bank could contain two types of memory devices. If two different types of memory devices are used in a bank, they must be segregated; one type in one half of the bank (group) and the other type in the other half of the bank. Sockets 5P, 5N, 3P and 3N make up group 1 of Bank A; sockets 5M, 5K, 3M and 3K make up group 2 of Bank A. Sockets 5J, 5H, 3J and 3H make up group 1 of Bank B; sockets 5E, 5D, 3E and 3D make up group 2 of Bank B.

CAUTION

Never install any device onto a board when power is applied. Damage to the board, device or power supply could result.

CAUTION

The 28-pin sockets are used for both 24-pin and 28-pin devices. When inserting 28-pin devices, ensure that pin 1 of the device corresponds with pin 1 of the socket. When inserting 24-pin devices, ensure that pin 1 of the device corresponds with pin 3 of the socket. (Refer to Figure 3-9.)

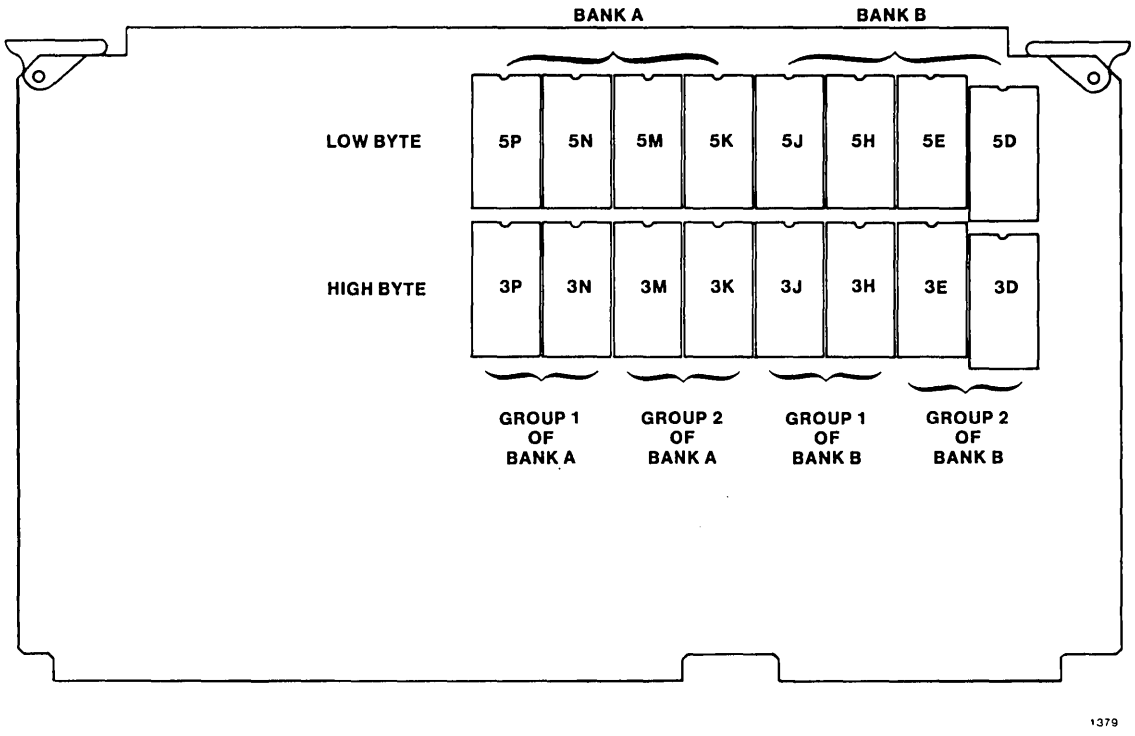


Figure 3-8. Memory Device Locations

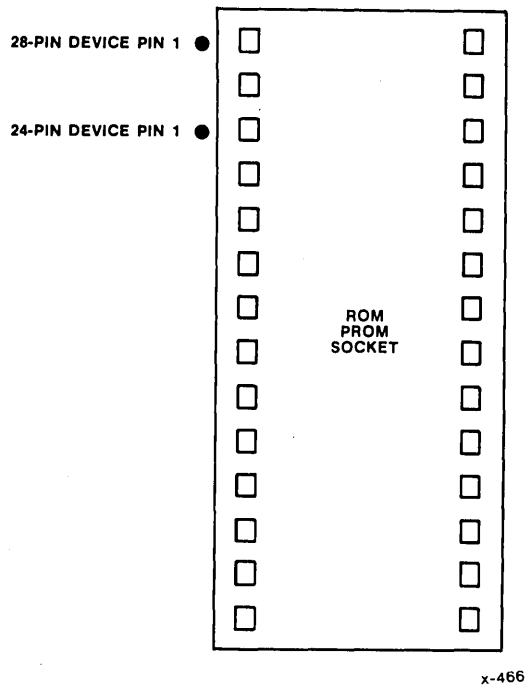


Figure 3-9. Device Insertion Diagram

3.4.2 FINAL INSTALLATION

In an iSBC single board computer based system, install the iSBC 428 board into any slot not wired for a dedicated function.

The iLBX bus interface requires an interconnect cable assembly. Ribbon cable and a mass terminated connector are required for this interconnect cable. Table 3-24 lists ribbon cables and Table 3-25 lists the connectors required for the interconnect cable. The iLBX interface scheme does not require that the iSBC 428 board be adjacent to iLBX compatible board slots.

CAUTION

If the Multibus interface environment is used, do not install the iSBC 428 board into a slot containing a P2 connector that is used for Multibus System Bus signals other than the high order address bits.

Table 3-24. Interface Cables

Vendor	Vendor Part Number	Conductors
T and B Ansley	171-60	60
T and B Ansley	173-60	60
3M	3365/60	60
3M	3306/60	60
Berg	76164-060	60
Belden	9L28060	60
Spectrastrip	455-240-60	60

Table 3-25. Interface Connectors

Vendor	Vendor Part No.	Conductors
KELAM	RF30-2803-5	60
T and B Ansley	A3020 (609-6025 modified)	60

***

CHAPTER 4. SERVICE INFORMATION

4.1 INTRODUCTION

This chapter contains the service and repair assistance instructions, replacement parts list and diagram, jumper post location diagram, and schematic diagrams.

4.2 SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance by contacting the Intel Product Service Marketing Administration in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Marketing Administration, you should have the following information available:

a. Date you received the product.
b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other MCSD products, it is usually stamped on a label.
c. Serial number of product. On boards, this number is usually stamped on the board. On other MCSD products, the serial number is usually stamped on a label.
d. Shipping and billing addresses.
e. Purchase order number for billing purposes if your Intel product warranty has expired.
f. Extended warranty agreement information, if applicable.

Use the following numbers for contacting the Intel Product Service Marketing Administration group:

Regional Telephone Numbers:

Western Region:	602-869-4951
Midwestern Region:	602-869-4392
Eastern Region:	602-869-4045
International:	602-869-4391

TWX Number:

910 - 951 - 1330
910 - 951 - 0687

Always contact the Product Service Marketing Administration group before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to Intel, use the original factory packing material, if possible. If this material is not available, wrap the product in cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service marketing Administration personnel.

4.3 REPLACEMENT PARTS

A complete list of replacement parts is provided in Table 4-1. This list provides the part number, manufacturer, description and quantity of the item. Notice that each item is referenced in the parts location diagram. Table 4-2 provides the full name of the manufacturer which is abbreviated in Table 4-1. Some of the parts are available from any normal commercial source, and should be ordered by their generic description. These items are called out as CML, rather than listing a specific part number. Figure 4-1 shows the location of each iSBC 428 referenced part in Table 4-1.

4.4 SERVICE DIAGRAMS

The following schematic diagram is included in this chapter:

Figure 4-3 iSBC 428 Board

Notice that a functional description of each jumper connection on a particular schematic sheet is referenced on the schematic.

Schematic diagrams are current when the manual is printed. However, minor revisions to the diagrams may occur between manual printings. Therefore, Intel provides photocopies of the current schematic diagrams with the board, when it is shipped from the factory. These diagrams should be inserted into this manual for future reference. In most instances, the diagrams shipped with the board will be identical to those printed in the manual.

4.5 INTERNAL SIGNALS

Internal board signals which traverse from one sheet to another in Figure 4-3 are identified by the signal mnemonic shown adjacent to a box along with the source or destination sheet number. Signals coming into the sheet are shown on the left side of the diagram. Conversely, signals leaving the sheet are shown on the right side.

To follow a signal from one sheet to another, read the signal mnemonic and the the sheet number next to the box, then look for the same signal mnemonic on the indicated sheet. For example, if you are going to trace the path of PAGE A when it exits sheet 4, the first step would be to turn to the indicated sheet. Since PAGE A will be entering sheet 3, as indicated on sheet 4 look for PAGE A on the left side of the sheet. Notice that the inputs on the sheet also list the source sheet number (sheet 4 in this example).

Each signal will keep the same mnemonic throughout Figure 4-3. This will enable you to trace the signal to any sheet with minimal effort.

The internal board signal mnemonics are listed and defined in Table 4-3. The signals are listed according to boxed code alphabetical order.

Signals which do not have boxes are either board inputs or outputs. These signals are described in Chapter 2.

4.6 JUMPER LOCATIONS

Jumper post locations are shown in Figure 4-2. This drawing is provided for use as a quick reference in locating the physical location of a jumper post on the iSBC 428 board. Jumper locations are also listed on each schematic sheet, with a brief description of the jumper's function.

Table 4-1. iSBC® 428 Replacement Parts List

Reference Designator	Description	Mfr Part No.	Mfr Code	Qty
	iSBC 428 Single Board Computer	113255	INTEL	1
C1,2,3	Capacitor ,47uF,20V,± 20%	OBD	COML	3
C4	Capacitor, 39uF, 10V, ± 20%	OBD	COML	1
C5,7,9,11,13 15,17,19-23 25-27,29, 31-33,35,37, 39-49,51,53, 57,9,60,62, 63,65,66,68, 69,71-73	Capacitor, 0.22uF, 50V, +80/-20%	OBD	COML	47
C6,8,10,12, 14,16,18,24 28,30,34,36, 38,50,52,54, 56,58,61,64, 67,70	Capacitor 0.1uF, 50V ±10%	OBD	COML	22
J1	Connector			1
R1	Resistor, 510, 1/4W, ±5%	COML	OBD	1
R2	Resistor, 10K, 1/4W, ±5%	COML	OBD	1
RP1-RP7	Resistor pack, 1K, 8-pin, SIP	COML	OBD	7
RP8	Resistor pack, 10K, 8-pin, SIP	COML	OBD	1
1A,2Y,3Y	IC, Quad, 2 input, positive NOR	74S32	TI	3
1C,3W	IC, Quad, 2 input, positive AND	74S08	TI	2
1D,1V	IC, Quad, 2 input, positive NAND	74S03	TI	2
1E,1F,1H	IC, Octal Buffers/Line Drivers	74S241	TI	3
1J,1K,1P	IC, Bus Transceiver	74LS245	TI	3
1N,1R	IC, Octal Bus Transceivers	74LS640	TI	3
1L,1M	IC, Decoder/Mux.	74LS155	TI	2
1S,1T,1U	IC, Octal Buffer	74LS240	TI	3
1W	IC, Hex Bus Drivers	74367	TI	1
1X,3X	IC, Dual D-Type Flip-flop	74S74	TI	2
1Y	IC, Tri, 3-input, positive AND	74S11	TI	1
2D,3B,4B,5T	IC, Octal D-Type Latches	74LS373	TI	4
2U,2V,3U,3V	IC, Quad exclusive NOR	74LS266	TI	4
2W,3Z,5X	IC, Quad, 2-input, positive NAND	74S00	TI	3
2X,4W	IC, Tri 3-input, positive NAND	74S10	TI	2
2Z	IC, Programmable Array Logic	PAL 16L8	MMI	1
3S,5S	IC, Bipolar PROM	3636B-1	Intel	2
4U,4Y	Delay Line, 100ns	DDU-7-100	DDD	2
4V,4X	IC, Hex Inverters	74S04	TI	2
4Z	Delay Line, 50ns	DDU-7-56	DDD	1

Table 4-1. iSBC® 428 Replacement Parts List (continued)

Reference Designator	Description	Mfr Part No.	Mfr Code	Qty
5V	IC, Dual 4-input, positive NAND	74S20	TI	1
5W	IC, Quad, 2-input, positive AND	74LS08	TI	1
5Y	IC, Sync. 4-bit counter	74LS161	TI	1
5Z	IC, 8-input, positive NAND	74S30	TI	1
X3D,X3E,X3H, X3J,X3K,X3M, X3N,X3P,X5D, X5E,X5H,X5J, X5K,X5M,X5N, X5P	Socket, 28-pin DIP	528-AG11D	AUGAT	16
X3S,X5S	Socket, 24-pin, DIP	524-AG11D	AUG	2
-	Plug, shorting, 2 position	530153-2	AMP	30

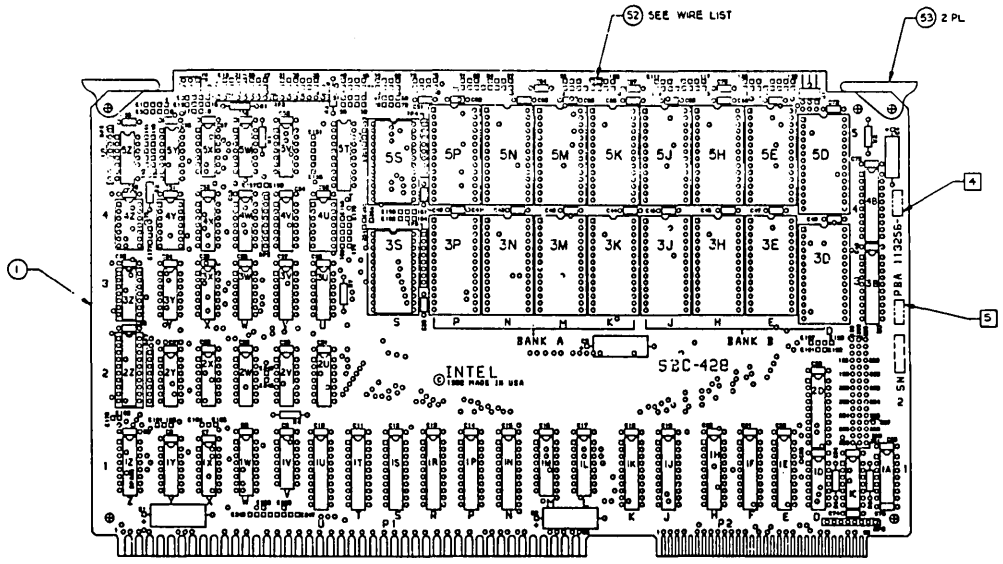
Table 4-2. Manufacturer's Names

Mfr. Code	Manufacturer
AMP	AMP Incorporated
AUGAT	Augat Incorporated
DDD	Data Delay Devices, Inc.
CRYSTEK	Crystek Crystals Corporation
Intel	Intel Corporation
MMI	Monolithic Memories
OBD	Order by description; any commercial (CML) source
TI	Texas Instruments Incorporated

Note: OBD = Order by description
CML = Any commercial source

Table 4-3. List of Internal Signal Mnemonics

Mnemonic	Description
ABD (0-17)	Address Bit iLBX Bus
ACE (0-7)/	Chip Enable (Bank A)
ACK/	Acknowledge
ADR (0-17)	Address Bit Multibus Mode
ARDY/	Bank A Ready
ASTB/	Address Strobe (LBX Mode)
BCE (0-7)	Chip Enable (Bank B)
BDSTB	Buffered Data Strobe
BHE	Byte High Enable (Internal to iSBC 428 board)
BHEN/	Byte High Enable
BINH	Buffered Inhibit
BINIT	Buffered Initialize
BRDSEL/	Board Select
BRDY/	Bank B Ready
CLR CYC	Clear Cycle
DIR	Direction
DSTB/	Data Strobe
HEN	High Byte Enable
iLBX	Local Bus Expansion
INH/	Inhibit
INIT	Initialize
INT (0-7)	Interrupt 0 -7
LATCH	Latch (for Address Latch and Page Select)
MPRO/	Memory Protect (Battery Back Up)
MRDC/	Memory Read Command
MWTC/	Memory Write Command
OE/	Output Enable
Page A	Page Select A
Page B	Page Select B
R/$\overline{W}$	Read/Write
SDC/	Swap Direction Control
SEL A/	Select Bank A
SEL B/	Select Bank B
SWAP/	Swap Enable
WE/	Write Enable
XACK/	Transfer Acknowledge
XHB/	iLBX High Byte Out
XHI/	iLBX High Byte Buffer Control
XLB/	iLBX Low Byte Out
XLO/	iLBX Low Byte Buffer Control
XLATCH	Latch (for Chip and Bank Select)



NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PART NUMBER IS 113256-002.
2. THIS DOCUMENT, PARTS LIST AND WIRE LIST ARE TRACKING DOCUMENTS.
3. WORKMANSHIP PER 99-0007-001.
4. MARK ASSEMBLY DASH NUMBER WITH CONTRASTING PERMANENT COLOR, NON-CONDUCTIVE, .12" HIGH, APPROXIMATELY WHERE SHOWN.
5. MARK VENDOR ID WITH CONTRASTING PERMANENT COLOR, NON-CONDUCTIVE, .12" HIGH, APPROXIMATELY WHERE SHOWN.
6. WIRE LIST WIRE NUMBERS 17 THRU 32 TO BE INSTALLED BY TEST.
7. INSTALL WIRE (ITEM 45) FROM 4X-9 TO RP3-2 ON SOLDER SIDE.
8. ON SOLDER SIDE CUT TRACE WHICH CONNECTS 3U-7 TO 5T-12.

Figure 4-1. iSBC® 428 Board Parts Location Drawing

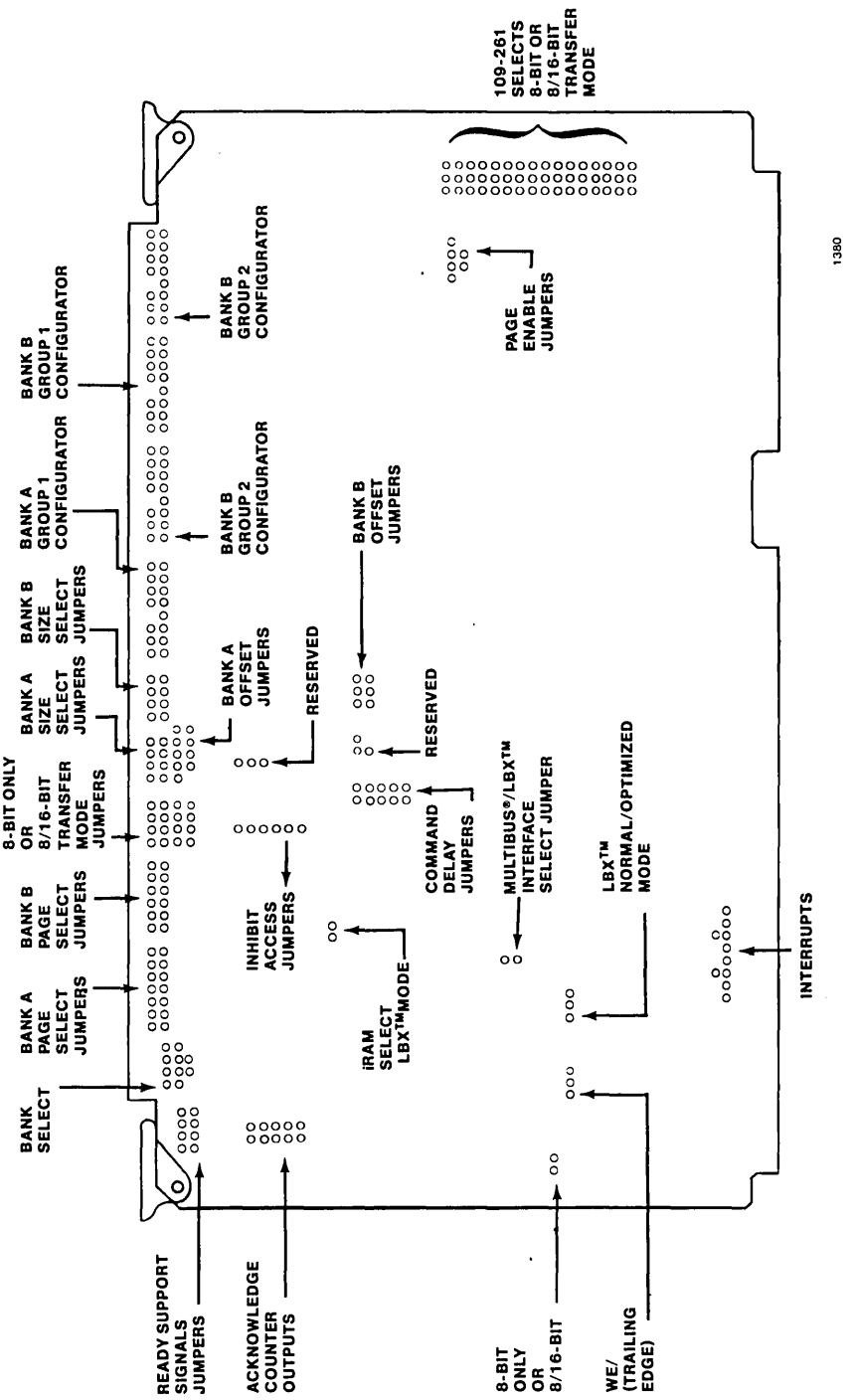


Figure 4-2. iSBC® 428 Board Jumper Post Location Drawing

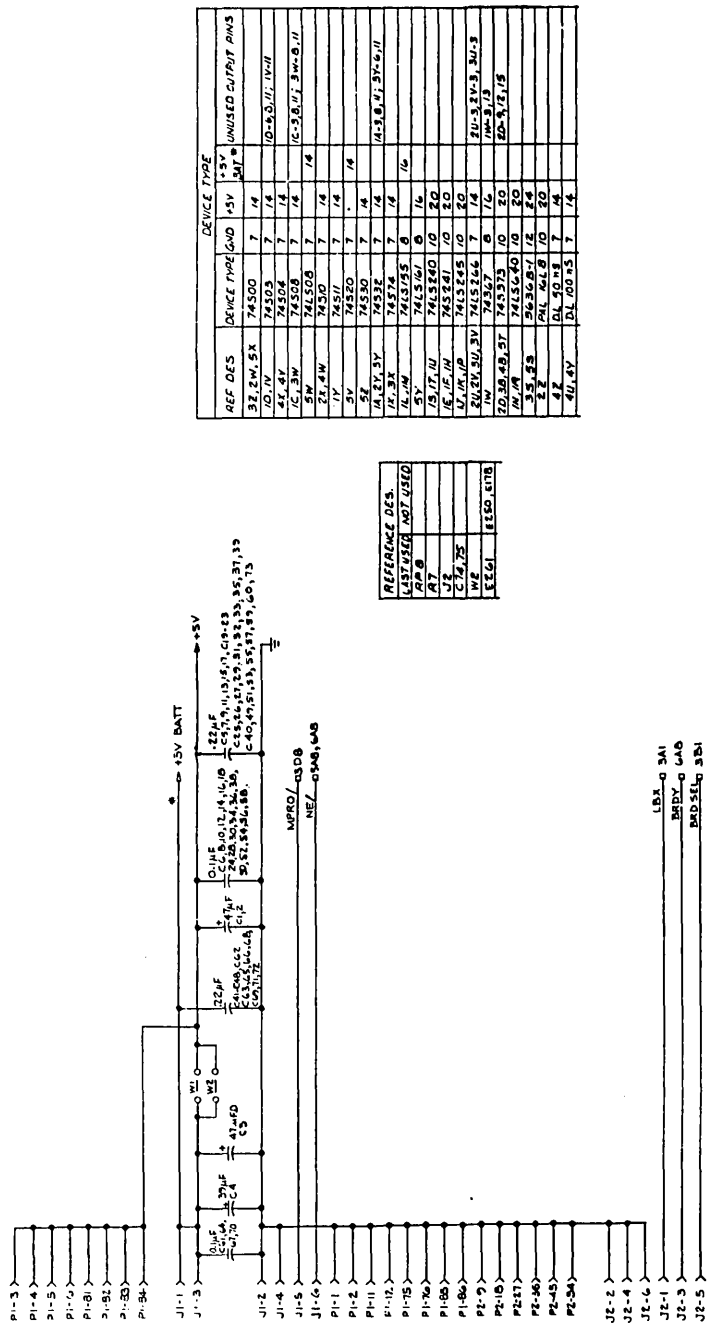


Figure 4-3. iSBC® 428 Board Schematic Diagram (Sheet 1 of 6)

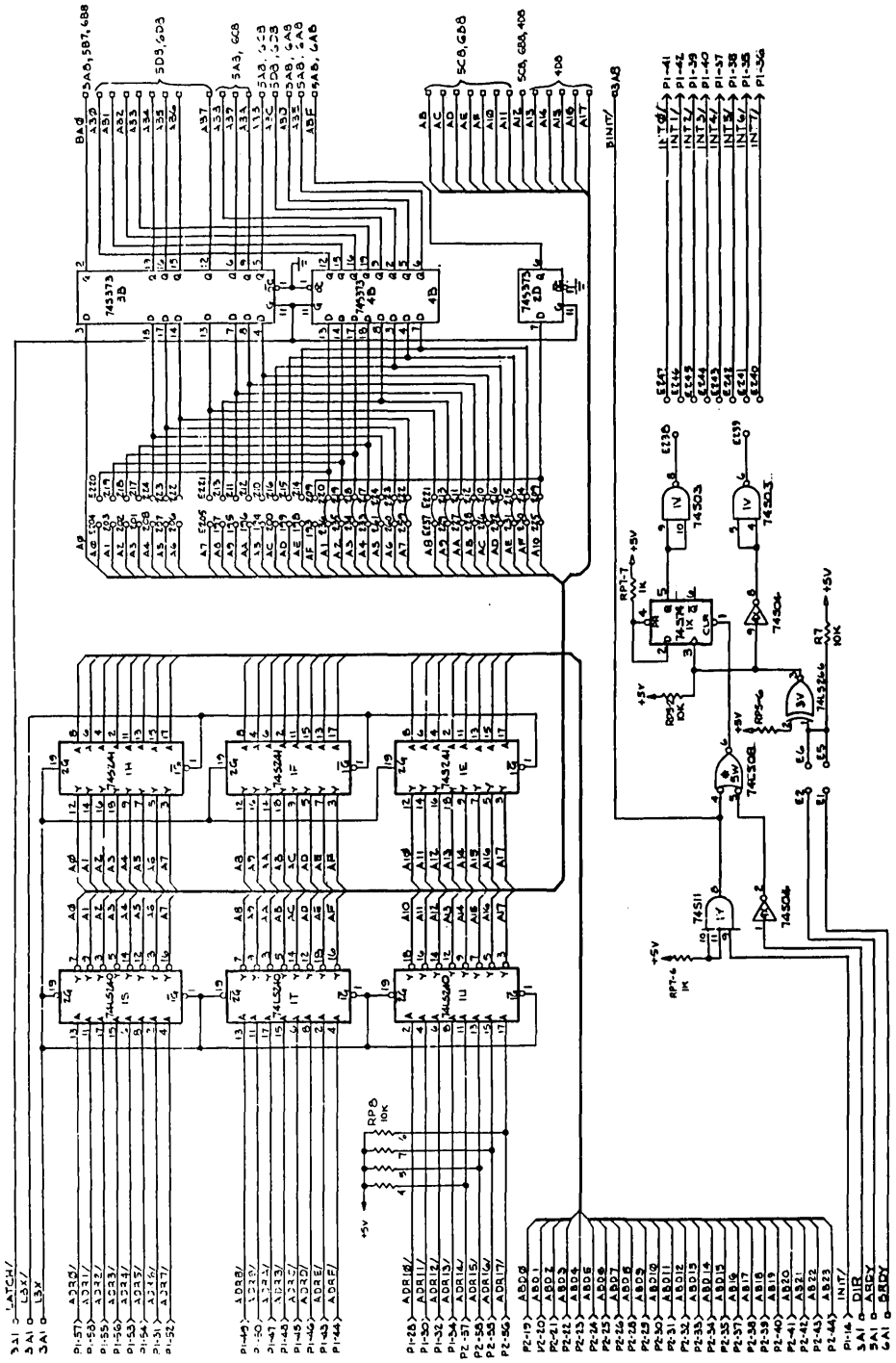


Figure 4-3. iSBC® 428 Board Schematic Diagram (Sheet 2 of 6)

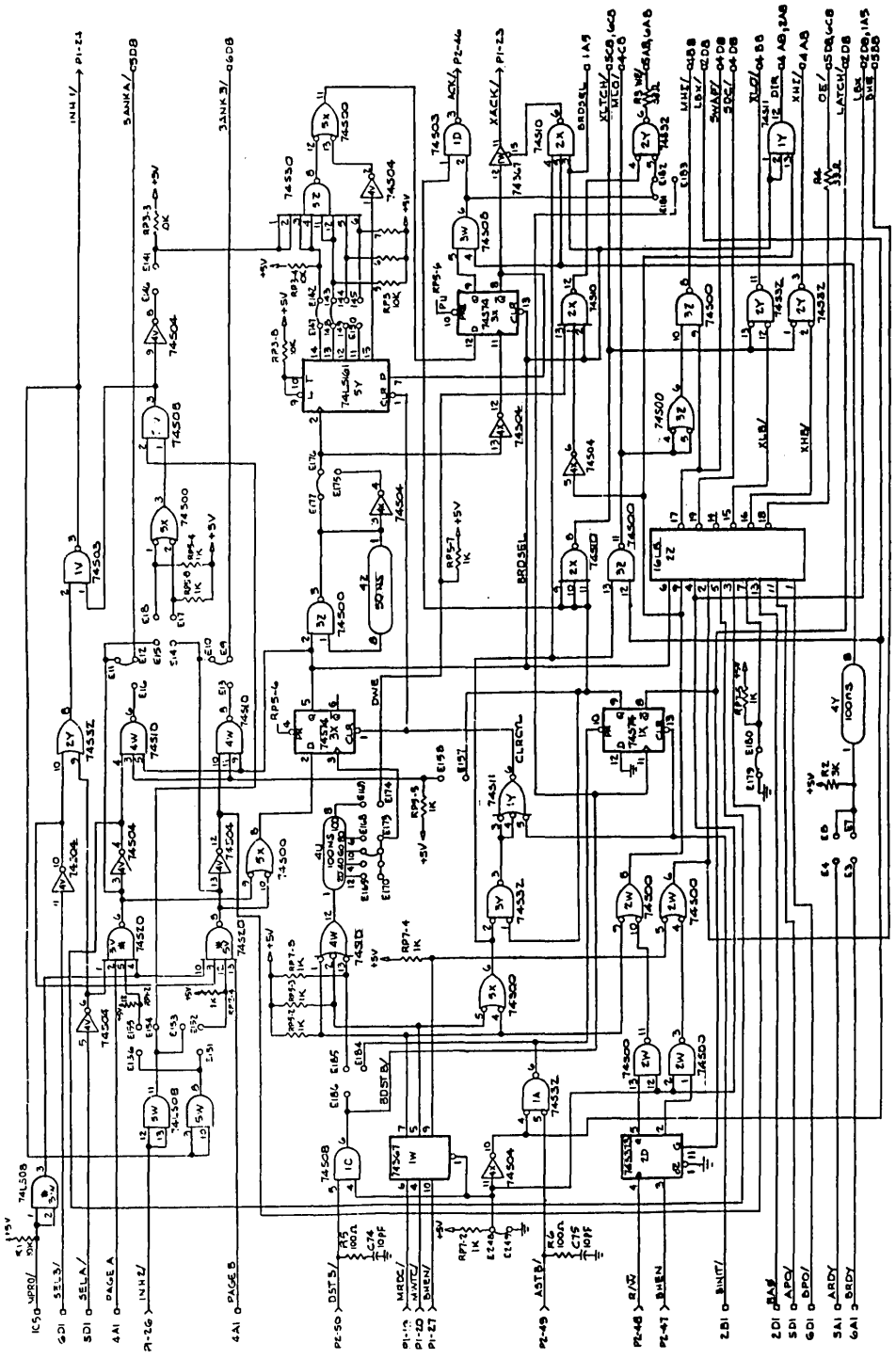


Figure 4-3. iSBC® 428 Board Schematic Diagram (Sheet 3 of 6)

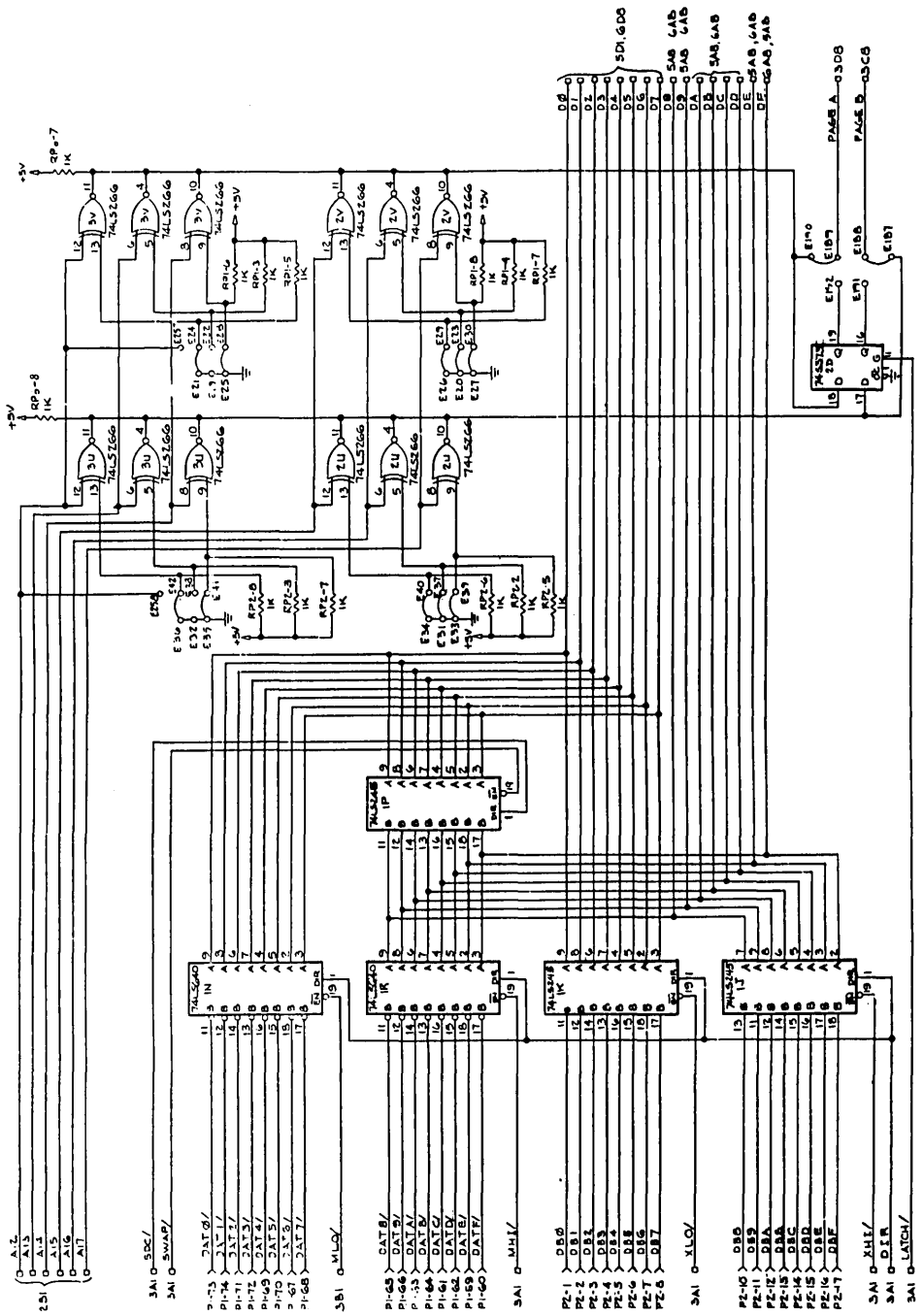


Figure 4-3. iSBC® 428 Board Schematic Diagram (Sheet 4 of 6)

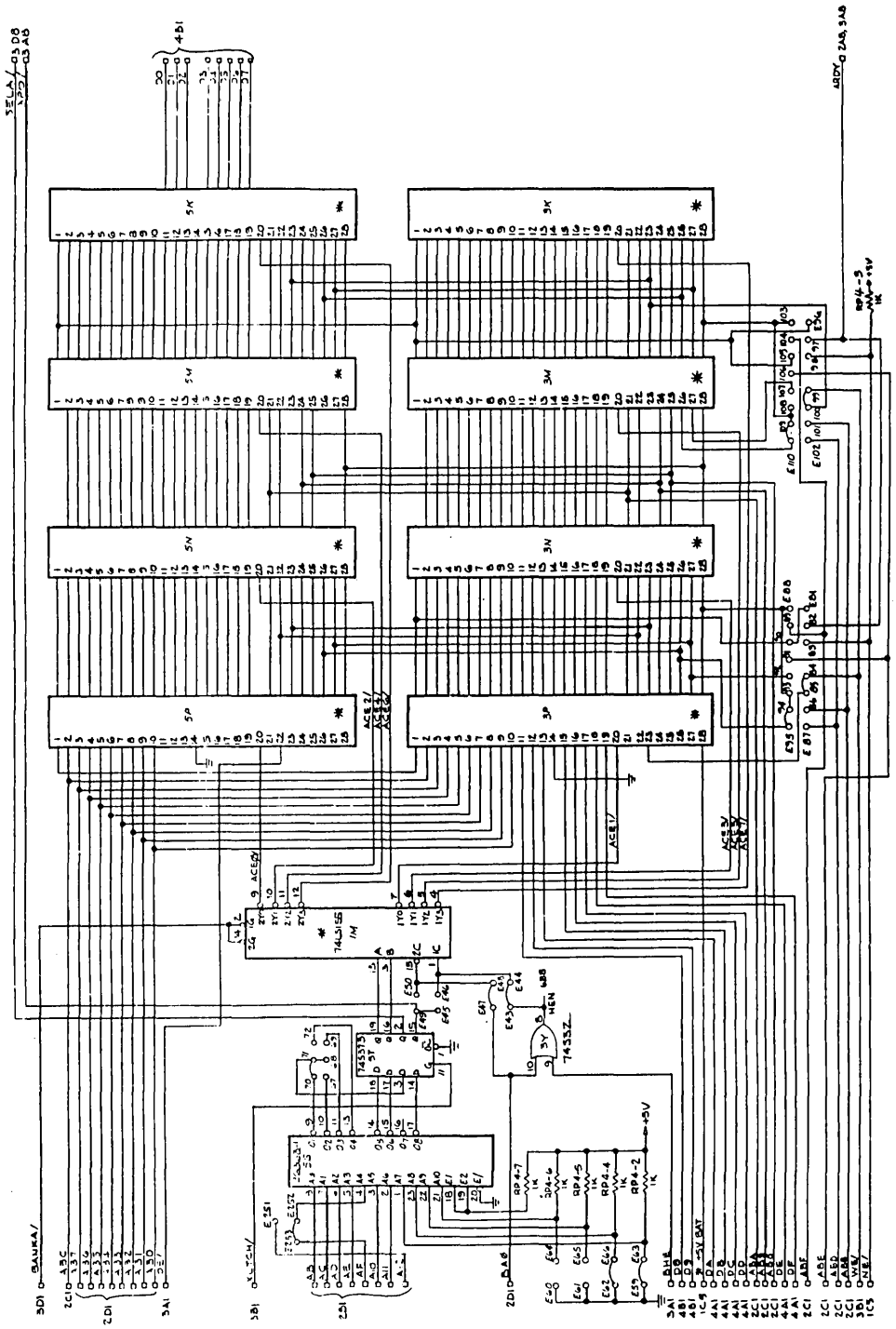


Figure 4-3. iSBC® 428 Board Schematic Diagram (Sheet 5 of 6)

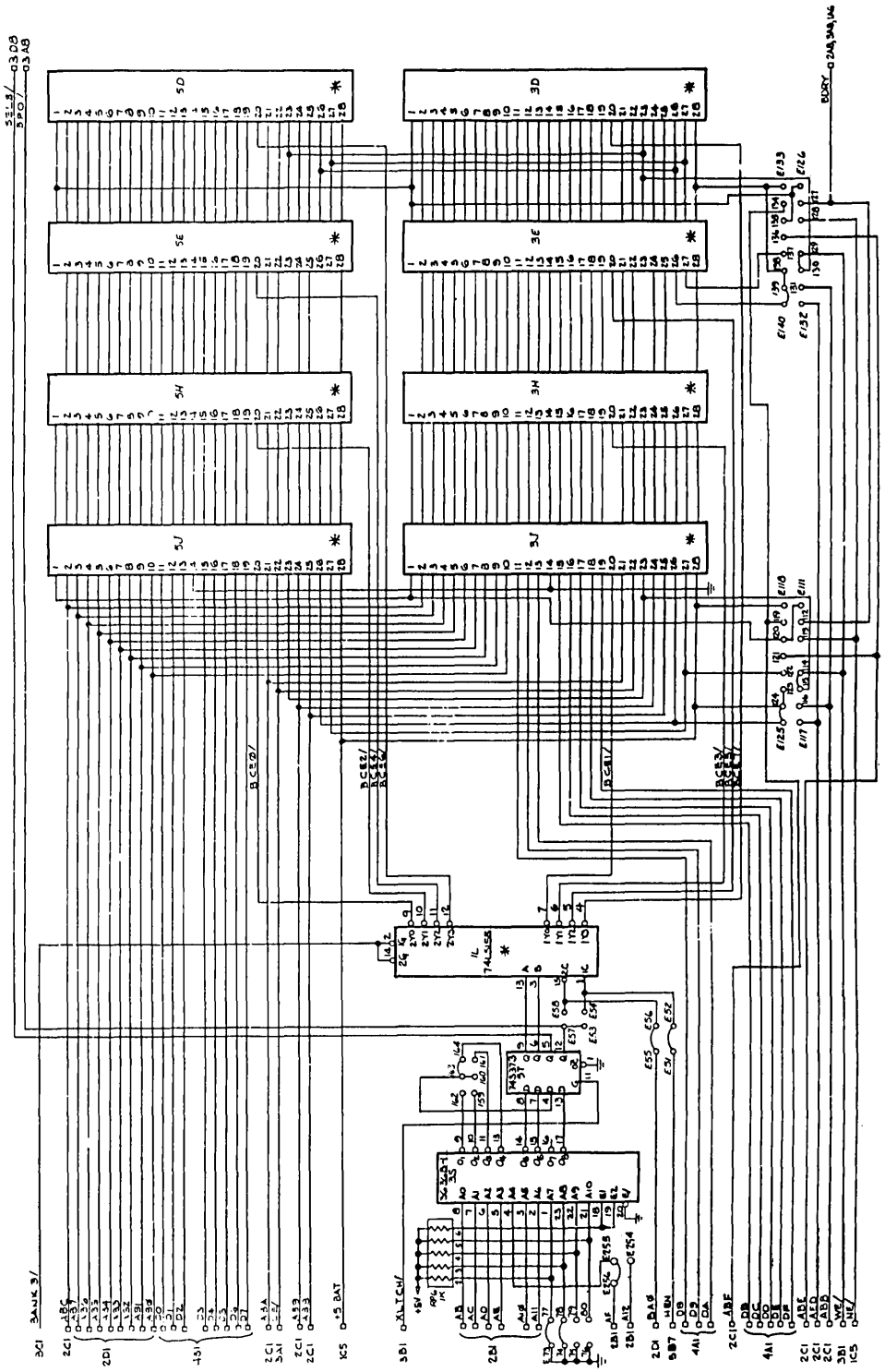


Figure 4-3. iSBC® 428 Board Schematic Diagram (Sheet 6 of 6)

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APPENDIX A. MULTIBUS® INTERFACE SIGNAL INFORMATION

Multibus connector P1 and auxiliary connector P2 interface the iSBC 428 board signals and power lines to the other boards in your system and the power supply. Where applicable, these signals conform to the Intel Multibus Interface standard. Multibus interface Pin assignments for the iSBC 428 board connectors P1 and P2 are provided in Table A-1 and A-3, respectively. Signal definitions are provided in Table A-2.

The signal names indicate whether or not the signal are active high or active low. If the signal name ends with a slash (/), then, the logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	L=TTL Low State	5.25V≥H≥2.0V	5.25V≥H≥2.4V
1	H=TTL High State	0.8V≥L≥−0.5V	0.5V≥L≥0V

If the signal name has no slash at the end, then the logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	L=TTL Low State	0.8V≥L≥−0.5V	0.5V≥L≥0V
1	H=TTL High State	5.25V≥H≥2.0V	5.25V≥H≥2.4V

These specifications are based on TTL where the power source is 5 volts ± 5%, referenced to ground (GND).

DC and AC characteristics of the P1 signals used on the iSBC 428 board are provided in Table A-4 and A-6, respectively. Refer to the board timing diagram (Figure A-1) for parameter identification.

Table A-1. MULTIBUS® Interface Connector P1

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	GND	Signal Ground	2	GND	Signal Ground
3	+5V	+5VDC	4	+5V	+5VDC
5	+5V	+5VDC	6	+5V	+5VDC
7	+12V**	+12VDC	8	+12V**	+12VDC
9	**	Reserved	10	**	Reserved
11	GND	Signal Ground	12	GND	Signal Ground
13	BCLK/**	Bus Clock	14	INIT/	Initialize
15	BPRN/**	Bus Priority In	16	BPRO/**	Bus Priority Out
17	BUSY/**	Bus Busy	18	BREQ/**	Bus Request
19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
21	IORC/**	I/O Read Cmd	22	IOWC/**	I/O Write Cmd
23	XACK/	Transf Ack	24	INH1/	Inhibit 1 RAM
25	LOCK/**	Lock	26		Reserved
27	BHEN/	Byte Hi Enable	28	AD10/	Address bit 10
29		Reserved	30	AD11/	Address bit 11
31		Reserved	32	AD12/	Address Bit 12
33		Reserved	34	AD13/	Address Bit 13
35	INT6/	Interrupt	36	INT7/	Interrupt
37	INT4/	Interrupt	38	INT5/	Interrupt
39	INT2/	Interrupt	40	INT3/	Interrupt
41	INT0/	Interrupt	42	INT1/	Interrupt
43	ADRE/	Address bit E	44	ADRF/	Address bit F
45	ADRC/	Address bit C	46	ADRD/	Address bit D
47	ADRA/	Address bit A	48	ADRB/	Address bit B
49	ADR8/	Address bit 8	50	ADR9/	Address bit 9
51	ADR6/	Address bit 6	52	ADR7/	Address bit 7
53	ADR4/	Address bit 4	54	ADR5/	Address bit 5
55	ADR2/	Address bit 2	56	ADR3/	Address bit 3
57	ADR0/	Address bit 0	58	ADR1/	Address bit 0
59	DATE/	Data bit E	60	DATF/	Data bit F
61	DATC/	Data bit C	62	DATD/	Data bit D
63	DATA/	Data bit A	64	DATB/	Data bit B
65	DAT8/	Data bit 8	66	DAT9/	Data bit 9
67	DAT6/	Data bit 6	68	DAT7/	Data bit 7
69	DAT4/	Data bit 4	70	DAT5/	Data bit 5
71	DAT2/	Data bit 2	72	DAT3/	Data bit 3
73	DAT0/	Data bit 0	74	DAT1/	Data bit 1
75	GND	Signal Ground	76	GND	Signal Ground
77		Reserved	78		Reserved
79		Reserved	80		Reserved
81	+5V	+5VDC	82	+5V	+5VDC
83	+5V	+5VDC	84	+5V	+5VDC
85	GND	Signal Ground	86	GND	Signal Ground

1. All odd-numbered pins (1, 3, 5...85) are on the component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top. All unassigned pins are reserved.

** Not used on the iSBC 428 board.

Table A-2. MULTIBUS® Interface Signal Functions

Signal	Functional Description
ADR0/ to ADRF/ ADR10/ to ADR17/	Address. These 24 lines transmit the address of the memory location to be accessed. All address bits are active low. ADR17/ is the most significant address bit.
BHEN/	Byte High Enable. When active low, enables the odd byte (DAT8/ through DATF/) onto the Multibus interface.
DAT0/ to DATF/	Data. 16-bits of data to be written into, or read from the memory array.
INIT/	Initialize. Resets the board logic to prepare the board for operation.
MPRO/	Memory Protect. Disables the board select circuits preventing memory operation during periods of uncertain AC power.
MRDC/	Memory Read Command. Initiates the read memory cycle.
MWTC/	Memory Write Command. Initiates the write memory cycle.
XACK/	Transfer Acknowledge. Indicates that the commanded read or write operation is complete and that data has been placed on the interface or accepted from the interface.
INH1/	Inhibit 1. The iSBC 428 board can receive or generate this signal. If received, this signal prevents access to the bank that is jumpered to listen for INH1/. If generated, this signal inhibits a slave board from accessing memory within the specified address range.
INH2/	Inhibit 2. If jumpered to listen for INH2/, this signal prevents access to the iSBC 428 board and will inhibit the board from generating INH1/ if so jumpered.

Table A-3. Connector P2 Pin Assignments

Pin	Signal Mnemonic	Description
1 to 54	Not used	Reserved
55	ADR 16/	Address bit
56	ADR 17/	Address bit
57	ADR 14/	Address bit
58	ADR 15/	Address bit
59, 60	Not used	Reserved.

Table A-4. DC Signal Characteristics

Pin	Signal	Drive Current	Load Current	Pin	Signal	Drive Current	Load Current
1	GND	-	-	2	GND	-	-
3	+5V	-	-	4	+5V	-	-
5	+5V	-	-	6	+5V	-	-
7	Not used	-	-	8	Not used	-	-
9	Reserved	-	-	10	Reserved	-	-
11	GND	-	-	12	GND	-	-
13	Not used	-	-	14	INIT/		0.4mA
15	Not used	-	-	16	Not used	-	-
17	Not used	-	-	18	Not used	-	-
19	MRDC/	-	1.6mA	20	MWTC/	-	1.6mA
21	Not used	-	-	22	Not used	-	-
23	XACK/	32mA	-	24	INH1/	20mA	0.8mA
25	Not used	-	-	26	INH2/	-	0.8mA
27	BHEN/	-	1.6mA	28	AD10/	-	0.2mA
29	Not used	-	-	30	AD11/	-	0.2mA
31	Not used	-	-	32	AD12/	-	0.2mA
33	INTA/	20mA	-	34	AD13/	-	0.2mA
35	INT6/	20mA	-	36	INT7/	20mA	-
37	INT4/	20mA	-	38	INT5/	20mA	-
39	INT2/	20mA	-	40	INT3/	20mA	-
41	INT0/	20mA	-	42	INT1/	20mA	-
43	ADRE/	-	0.2mA	44	ADRF/	-	0.2mA
45	ADRC/	-	0.2mA	46	ADRD/	-	0.2mA
47	ADRA/	-	0.2mA	48	ADRB/	-	0.2mA
49	ADR8/	-	0.2mA	50	ADR9/	-	0.2mA
51	ADR6/	-	0.2mA	52	ADR7/	-	0.2mA
53	ADR4/	-	0.2mA	54	ADR5/	-	0.2mA
55	ADR2/	-	0.2mA	56	ADR3/	-	0.2mA
57	ADR0/	-	0.2mA	58	ADR1/	-	0.2mA
59	DATE/	24mA	0.4mA	60	DATF/	24mA	0.4mA
61	DATC/	24mA	0.4mA	62	DATD/	24mA	0.4mA
63	DATA/	24mA	0.4mA	64	DATB/	24mA	0.4mA
65	DAT8/	24mA	0.4mA	66	DAT9/	24mA	0.4mA
67	DAT6/	24mA	0.4mA	68	DAT7/	24mA	0.4mA
69	DAT4/	24mA	0.4mA	70	DAT5/	24mA	0.4mA
71	DAT2/	24mA	0.4mA	72	DAT3/	24mA	0.4mA
73	DAT0/	24mA	0.4mA	74	DAT1/	24mA	0.4mA
75	GND	-	-	76	GND	-	-
77	Not used	-	-	78	Not used	-	-
79	Not used	-	-	80	Not used	-	-
81	+5V	-	-	82	+5V	-	-
83	+5V	-	-	84	+5V	-	-
85	GND	-	-	86	GND	-	-

Table A-5. AC Characteristics

Parameter	Description	Minimum	Maximum	Units
t_{BCY}	Bus Clock Period	100	D.C.	ns
t_{BW}	Bus Clock Width	0.35 t_{BCY}	0.65 t_{BCY} (not restricted)	
t_{SKEW}	BCLK/skew		3	ns
t_{PD}	Standard Bus Propagation Delay		3	
t_{AS}	Address Set-Up Time (at Slave Board)	50		ns
t_{DS}	Write Data Set Up Time	50		ns
t_{AH}	Address Hold Time	50		ns
t_{DHW}	Write Data Hold Time	50		ns
t_{DXL}	Read Data Set Up Time To XACK	0		ns
t_{DHR}	Read Data Hold Time	0	65	ns
t_{XAH}	Acknowledge Hold Time	0	65	ns
t_{XACK}	Acknowledge Time	0	8	μs
t_{CMD}	Command Pulse Width	100	9.5	μs
t_{INTA}	INTA/ Width	250		ns
t_{CSEP}	Command Separation	100		ns
t_{BREQL}	↑BCLK/ to BREQ/ Low Delay	0	35	ns
t_{BREQH}	↓BCLK/ to BREQ/ High Delay	0	35	ns
t_{BPRNS}	BPRN/ to ↓BCLK/ Setup Time	22		ns
t_{BUSY}	BUSY/ delay from ↓BCLK/	0	70	ns
t_{BUSYS}	BUSY/ to ↓BCLK/ Setup Time	25		ns
t_{BPRO}	↓BCLK/ to BPRO/ (CLK to Priority Out)	0	40	ns
t_{BPRNO}	BPRN/ to BPRO/ (Priority In to Out)	0	30	ns
t_{CBRO}	↓BCLK/ to CBRQ/ (CLK to Common Bus Request)	0	60	ns
t_{CBRQS}	CBRQ/ to ↓BCLK/ Setup Time	35		ns
t_{XCD}	XACK↓ to Command Delay	0	1500	ns
t_{BSYO}	CBRQ/↓ and BUSY/↓ to BUSY/↑	—	12	μs
t_{CCY}	C-clock Period	100	110	ns
t_{CW}	C-clock Width	0.35 t_{CCY}	0.65 t_{CCY}	ns
t_{INIT}	INIT/Width	5		ms
t_{INITS}	INIT/ to MPRO/ Setup Time	100		ns
t_{PBD}	Power Backup Logic Delay	0	200	ns
t_{PFINW}	PFIN/ Width	2.5		ms
t_{MPRO}	MPRO/ Delay	2.0	2.5	ms

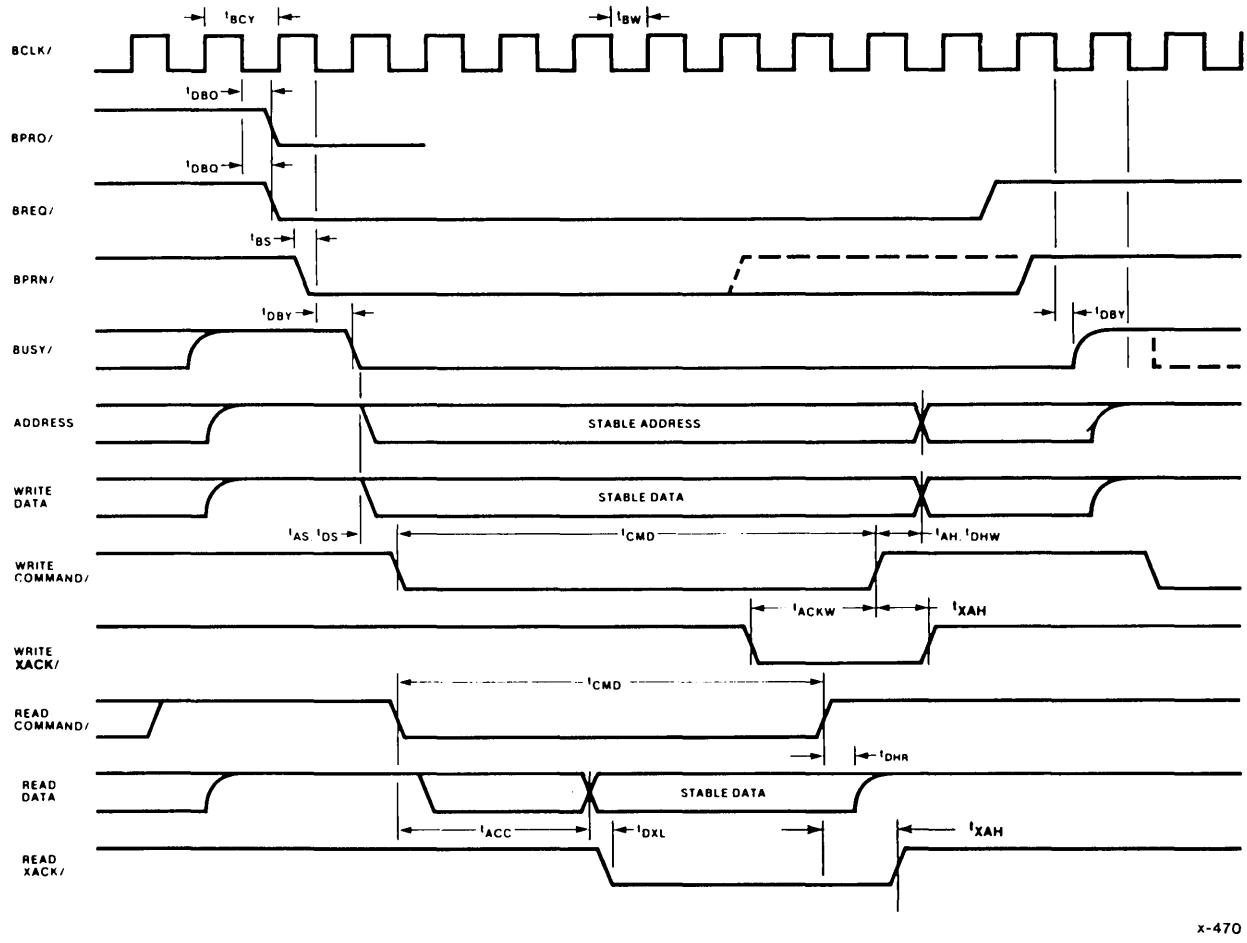

Figure A-1. AC Timing Diagram

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APPENDIX B. iLBX™ INTERFACE SIGNAL INFORMATION

The iLBX connector P2 interfaces the iSBC 428 board signals to other boards in your system. Where applicable, these signals conform to the Intel iLBX interface standard. Pin assignments for the P2 connector are listed in Table B-1.

The signal names indicate whether or not the signal; lines on the iLBX interface are active high or active low. If the signal name ends with a slash (/), then the logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	L=TTL Low State	5.25V≥H≥2.0V	5.25V≥H≥2.4V
1	H=TTL High State	0.8V≥L≥−0.5V	0.5V≥L≥0V

If the signal name has no slash, then the logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	L=TTL Low State	0.8V≥L≥−0.5V	0.5V≥L≥0V
1	H=TTL High State	5.25V≥H≥2.0V	5.25V≥H≥2.4V

These specifications are based on TTL where the power source is 5 Volts ±5% referenced to ground (GND).

Table B-1. iSBC® 428 Board iLBX™ Interface Connector Pin Assignments

Pin	Signal	Description	Pin	Signal	Description
1	DB0	Data Bus	2	DB1	Data Bus
3	DB2	Data Bus	4	DB3	Data Bus
5	DB4	Data Bus	6	DB5	Data Bus
7	DB6	Data Bus	8	DB7	Data Bus
9	GND	Signal Ground	10	DB8	Data Bus
11	DB9	Data Bus	12	DBA	Data Bus
13	DBB	Data Bus	14	DBC	Data Bus
15	DBD	Data Bus	16	DBE	Data Bus
17	DBF	Data Bus	18	GND	Signal Ground
19	ABD0	Address Bus	20	ABD1	Address Bus
21	ABD2	Address Bus	22	ABD3	Address Bus
23	ABD4	Address Bus	24	ABD5	Address Bus
25	ABD6	Address Bus	26	ABD7	Address Bus
27	GND	Signal Ground	28	ABD8	Address Bus
29	ABD9	Address Bus	30	ABD10	Address Bus
31	ABD11	Address Bus	32	ABD12	Address Bus
33	ABD13	Address Bus	34	ABD14	Address Bus
35	ABD15	Address Bus	36	GND	Signal Ground
37	AB16	Address Bus	38	AB17	Address Bus
39	AB18	Address Bus	40	AB19	Address Bus
41	AB20	Address Bus	42	AB21	Address Bus
43	AB22	Address Bus	44	AB23	Address Bus
45	GND	Signal Ground	46	ACK/	Acknowledge
47	BHEN	Byte High Enable	48	R/$\overline{W}$	Read/Write
49	ASTB/	Address Strobe	50	DSTB/	Data Strobe
51	Not used		52	Not used	
53	Not used		54	GND	Signal Ground
55	Not used		56	Not used	
57	Not used		58	Not used	
59	Not used		60	Not used	

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APPENDIX C. MEMORY MAP

Table C-1 lists the contents of the decode PROM Memory Map.

Table C-1. PROM Memory Map

8000	40	40	40	40	40	40	40	40	40	40	40	40	40	40	40	40
8010	60	60	60	60	60	60	60	60	60	60	60	60	60	60	60	60
8020	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0
8030	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0
8040	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50
8050	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70
8060	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0
8070	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0
8080	40	40	40	40	40	40	40	40	40	40	40	40	40	40	40	40
8090	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0
80A0	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50
80B0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0
80C0	60	60	60	60	60	60	60	60	60	60	60	60	60	60	60	60
80D0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0
80E0	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70
80F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0
8100	4E	4E	4E	4E	4E	4E	4E	4E	CE	CE	CE	CE	CE	CE	CE	CE
8110	5C	5C	5C	5C	5C	5C	5C	5C	DC	DC	DC	DC	DC	DC	DC	DC
8120	68	68	68	68	68	68	68	68	E8	E8	E8	E8	E8	E8	E8	E8
8130	78	78	78	78	78	78	78	78	F8	F8	F8	F8	F8	F8	F8	F8
8140	41	41	41	41	41	41	41	41	C1	C1	C1	C1	C1	C1	C1	C1
8150	53	53	53	53	53	53	53	53	D3	D3	D3	D3	D3	D3	D3	D3
8160	67	67	67	67	67	67	67	67	E7	E7	E7	E7	E7	E7	E7	E7
8170	77	77	77	77	77	77	77	77	F7	F7	F7	F7	F7	F7	F7	F7
8180	47	47	47	47	47	47	47	47	C7	C7	C7	C7	C7	C7	C7	C7
8190	57	57	57	57	57	57	57	57	D7	D7	D7	D7	D7	D7	D7	D7
81A0	63	63	63	63	63	63	63	63	E3	E3	E3	E3	E3	E3	E3	E3
81B0	71	71	71	71	71	71	71	71	F1	F1	F1	F1	F1	F1	F1	F1
81C0	48	48	48	48	48	48	48	48	C8	C8	C8	C8	C8	C8	C8	C8
81D0	58	58	58	58	58	58	58	58	D8	D8	D8	D8	D8	D8	D8	D8
81E0	6C	6C	6C	6C	6C	6C	6C	6C	EC	EC	EC	EC	EC	EC	EC	EC
81F0	7E	7E	7E	7E	7E	7E	7E	7E	FE	FE	FE	FE	FE	FE	FE	FE
8200	4E	4E	4E	4E	CE	CE	CE	CE	5C	5C	5C	5C	DC	DC	DC	DC
8210	68	68	68	68	E8	E8	E8	E8	78	78	78	78	F8	F8	F8	F8
8220	41	41	41	41	C1	C1	C1	C1	53	53	53	53	D3	D3	D3	D3
8230	67	67	67	67	E7	E7	E7	E7	77	77	77	77	F7	F7	F7	F7
8240	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8250	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8260	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

Table C-1. PROM Memory Map (continued)

8270	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8280	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8290	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
82A0	4E	4E	4E	4E	CE	CE	CE	CE	5C	5C	5C	5C	DC	DC	DC	DC
82B0	68	68	68	68	E8	E8	E8	E8	78	78	78	78	F8	F8	F8	F8
82C0	41	41	41	41	C1	C1	C1	C1	53	53	53	53	D3	D3	D3	D3
82D0	67	67	67	67	E7	E7	E7	E7	77	77	77	77	F7	F7	F7	F7
82E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
82F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8300	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8310	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8320	47	47	47	47	C7	C7	C7	C7	57	57	57	57	D7	D7	D7	D7
8330	63	63	63	63	E3	E3	E3	E3	71	71	71	71	F1	F1	F1	F1
8340	48	48	48	48	C8	C8	C8	C8	58	58	58	58	D8	D8	D8	D8
8350	6C	6C	6C	6C	EC	EC	EC	EC	7E	7E	7E	7E	FE	FE	FE	FE
8360	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8370	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8380	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8390	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
83A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
83B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
83C0	47	47	47	47	C7	C7	C7	C7	57	57	57	57	D7	D7	D7	D7
83D0	63	63	63	63	E3	E3	E3	E3	71	71	71	71	F1	F1	F1	F1
83E0	48	48	48	48	C8	C8	C8	C8	58	58	58	58	D8	D8	D8	D8
83F0	6C	6C	6C	6C	EC	EC	EC	EC	7E	7E	7E	7E	FE	FE	FE	FE
8400	4E	4E	CE	CE	5C	5C	DC	DC	68	68	E8	E8	78	78	F8	F8
8410	41	41	C1	C1	53	53	D3	D3	67	67	E7	E7	77	77	F7	F7
8420	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8430	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8440	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8450	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8460	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8470	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8480	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8490	4E	4E	CE	CE	5C	5C	DC	DC	68	68	E8	E8	78	78	F8	F8
84A0	41	41	C1	C1	53	53	D3	D3	67	67	E7	E7	77	77	F7	F7
84B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
84C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
84D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
84E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
84F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8500	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8510	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8520	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8530	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8540	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8550	47	47	C7	C7	57	57	D7	D7	63	63	E3	E3	71	71	F1	F1
8560	48	48	C8	C8	58	58	D8	D8	6C	6C	EC	EC	7E	7E	FE	FE

Table C-1. PROM Memory Map (continued)

8570	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8580	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8590	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
85A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
85B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
85C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
85D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
85E0	47	47	C7	C7	57	57	D7	D7	63	63	E3	E3	71	71	F1	F1
85F0	48	48	C8	C8	58	58	D8	D8	6C	6C	EC	EC	7E	7E	FE	FE
8600	4E	CE	5C	DC	68	E8	78	F8	41	C1	53	D3	67	E7	77	F7
8610	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8620	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8630	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8640	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8650	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8660	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8670	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8680	FF	FF	FF	FF	FF	FF	FF	FF	4E	CE	5C	DC	68	E8	78	F8
8690	41	C1	53	D3	67	E7	77	F7	FF	FF	FF	FF	FF	FF	FF	FF
86A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
86B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
86C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
86D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
86E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
86F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8700	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8710	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8720	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8730	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8740	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8750	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8760	FF	FF	FF	FF	FF	FF	FF	FF	47	C7	57	D7	63	E3	71	F1
8770	48	C8	58	D8	6C	EC	7E	FE	FF	FF	FF	FF	FF	FF	FF	FF
8780	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8790	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
87A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
87B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
87C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
87D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
87E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
87F0	47	C7	57	D7	63	E3	71	F1	48	C8	58	D8	6C	EC	7E	FE

***

APPENDIX D. PAL SWAP BYTE EQUATIONS

D-1. INTRODUCTION

Table D-1 presents the equations for the transceiver control PAL.

Table D-1. PAL Swap Byte Control Equations

```
BP H BNKB X BNKA B Y SP R GND AP SP A SP /XL /XH /SW /OE /SD VCC


IF (VCC) /SW  =  /X * Y * BNKA * AP
                 + /X * Y * BNKB * BP
                 + /X * /Y * /H * A
                 + X * Y * /A * BNKA * AP
                 + X * Y * /A * BNKB * BP
                 + X * Y * A * BNKA * /AP
                 + X * Y * A * BNKB * /BP


IF (VCC) /SD  =   X * Y * R * /A * BNKA * AP
                  + X * Y * R * /A * BNKB * BP
                  + X * Y * /R * A * BNKA * /AP
                  + X * Y * /R * A * BNKA * /BP
                  + /X * R * B


IF (VCC) /XL  =   X * /A * /R
                  + X * /A * R * B


IF (VCC) /XH  =   X * H * /R
                  + X * H * R * B

IF (VCC) /OE  =   /X * R * B
                  + X * R * B
```

DESCRIPTION:

A = Address 0 (odd Address)

/A = Even Address

B = BRDSEL

BNKA = Bank A Select

H = BHEN

BNKB = Bank B Select

R = Read

/R = Write

AP = Bank A chip Select - Hi = Odd Chip Select, Lo =Even Chip Select

BP = Bank B Chip Select - Hi = Odd Chip Select, Lo = Even Chip Select

Y = 8-bit Mode

/Y = 16-bit Mode

SP = Spare

X = iLBX mode

/X = Multibus Mode

/OE = Output Enable

/XH = iLBX Hi Byte Enable

/XL = iLBX Lo Byte Enable

/SD = Swap Direction Control

/SW = Swap Buffer Output Enable

***

APPENDIX E. SPECIAL JUMPERING FOR iRAM DEVICES

When installing iRAM devices in the iSBC 428 board there are special jumpers that need to be configured. One, you need to delay the leading edge of write Enable by installing a jumper E169 to E174. This guarantees that data is valid prior to the falling edge of WE/.

Second, you also need to provide clean chip select signals for iRAM devices. This is accomplished by removing the jumper from E11 to E12 and installing a jumper E12 to E16 for iRAM devices installed in Bank A or removing the jumper from E9 to E10 and installing a jumper E9 to E13 for iRAM devices installed in Bank B.

Third, the iRAM, being a dynamic device, periodically needs to refresh itself. When accessed and currently in a refresh cycle, the Ready signal (pin 1) is driven low. This signal must be connected to the XACK/ACK circuitry of the iSBC 428 board to hold off any acknowledge until the accessed device has valid output data. This is easily done with jumpers provided in the configurator jumper matrix of each bank. Therefore, follow pin 1 down to the configurator block (depending on the group and bank that the device is located) and install the jumper that connects to either the ARDY (reference sheet 5 of Figure 4-3) line or the BRDY (reference Sheet 6 of Figure 4-3) line (depending on the bank in which the device is installed). This brings the ready signal to either E4 or E3. The ARDY and BRDY signals are then connected to the acknowledge circuitry via jumpers E4 to E8 for Bank A or jumpers E3 to E7 for BAnk B. Install the appropriate jumper (E4 to E8 or E3 to E7) to delay the generation of the acknowledge signal (either XACK/ in the Multibus System Bus interface or ACK/ in the iLBX Bus interface).

In the iLBX mode only there is an additional jumper that must be installed. This jumper is E157 to E158. This jumper terminates the chip select signals to the iRAM and provides additional recovery time. If you have this jumper installed (in the iLBX mode) and decide to interface instead to the Multibus System Bus, this jumper must be removed.

NOTE

The iSBC 428 board does not support operation of iRAM devices in the iLBX optimized mode.

***

APPENDIX F. SPECIAL CASES EEPROM DEVICES

This Appendix provides jumper information to install EEPROM devices onto the iSBC 428 board. There are both 28-pin and 24-pin EEPROM devices available. When programming 28-pin EEPROM devices that support a READY/BUSY pin, the interrupt jumper matrix provides the capability of jumpering a buffered ARDY/BRDY signal to the Multibus interrupt request lines INT0/ through INT7/. This READY signal from the EEPROM device is jumpered through the Configurator block to the interrupt matrix by installing jumper E2 to E6 (ARDY) or E1 to E5 (BRDY). Refer to Figure 4-3 sheet 2. Jumpering E239 to any of the interrupt request lines provide a means for a poll type of interrupt and reflects a direct buffered copy of the ARDY/BRDY signal. This signal is low for the entire write programming time (not ready) of the particular EEPROM device. Jumpering E238 to any of the interrupt request lines provide a ready interrupt that occurs when the particular EEPROM device completes its write cycle (refer to Table 3-20). Any subsequent read to the iSBC 428 board clears the interrupt.

There are manufactures that produce 24-pin EEPROM devices. When 24-pin EEPROM devices are installed, special jumpering is required. These devices do not support a READY/BUSY signal. When using these 24-pin EEPROM devices on the iSBC 428 board, connect the Configurator block using the SRAM configuration for that particular device size. Also note that because the system master processor now has no direct feedback method to inform that the EEPROM write has completed, it must either poll the device for correct data written or set up a software or hardware timer that substitutes for the ready function.

Both 28-pin and 24-pin EEPROM devices require need to delay the leading edge of write Enable by installing a jumper E169 to E174. This guarantees that data is valid prior to the falling edge of WE/.

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INDEX

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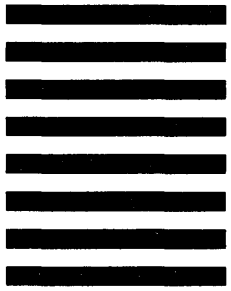

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