A MARKETING GUIDE TO INTEGRATED CIRCUITS

INTEGRATED CIRCUIT ENGINEERING CORPORATION © 466

FOREWORD

This Guide has been prepared to assist marketing organizations adapt to the new problems generated by integrated circuits. Most readers are already familiar with the changes wrought by integrated circuits – the loss of identity of individual components (transistors, resistors, coils and wire) within smaller structures. The scope of this technology's capabilities in application is as broad as engineering ingenuity. This remarkable new technology has usurped application after application of discrete components, modified design attitudes and revised marketing patterns.

The high volume use of integrated circuits has been a reality for some time. IBM is currently using in excess of 25,000,000 hybrid integrated circuits modules a year in its System 360 computer. Recently, Admiral Corporation announced their 1966 color television sets incorporating integrated circuits in the video-demodulator stage. Radio Corporation of America's entire 1966 television line will employ monolithic circuits in the sound channel. Computers the size of a high fidelity audio system are now in operation with the data processing capability of large commercial computers.... with improved reliability.

Firms presently fabricating modules, instruments, equipment, systems and components are feeling the impact of integrated circuits. Since an estimated 70% of conventionally constructed circuits are convertible, most firms must initiate or expand integrated circuit programs today in order to meet effectively tomorrow's competition. Even now, integrated circuits can reduce labor cost 70 to 80% and materials 25 to 35%.

The mechanics of marketing integrated circuits have begun to take definite form. The advent of MOS arrays has more solidly supported the fact that systems marketing concepts will prevail. Because this was foreseen with conventional monolithic structures, several companies are on the verge of offering complete computers on a single slice of silicon. Large Scale Integration (LSI) is becoming available. Thus, the marketing of integrated circuits must follow the precepts established by systems marketing in the past.

A major problem of systems marketing within the components industry will be accentuated by consideration of the customer's "contributed value". If the customer were accustomed to systems procurements, this problem would be minimal. However, in most situations, the vendor must sell on a systems basis to customers who are only accustomed to thinking in terms of discrete components. Perhaps this will produce the biggest change in the area of the new management interfaces. In systems procurement, these interfaces tend to occur at a much higher level. It is the duty of the marketing personnel to facilitate this educational process as much as possible.

Systems marketing must be conducted on a different basis than component marketing. Past purchasing negotiations have been characterized by a lower level of responsibility on the part of the vendor. All too often the marketing staff of discrete component manufacturers has been informed by their engineering "This is what we make – sell it". The marketing specialist has then taken the position of getting as much as he can for the product without taking responsibility for the performance of the end product. Where integrated circuits are involved, this attitude will no longer be adequate. While he may still try to get all he can for his product (and he should), he will be unable to avoid a significant part of the responsibility for the end product. This responsibility will extend through engineering and into the management of the vendor company. At the same time the customer will also have greater responsibility. He must reveal his design objectives to an extent not heretofore contemplated, and his approaches to specifications must be on a much more realistic basis. The purchaser-supplier relationship must thus be based on mutual trust and understanding of the other's problems.

This Guide is dedicated to the proposition that the marketing specialist who would excel in the vending of integrated circuits must know more than ever before, not only about his product, but how that product is used. Aside from technical innovations, the importance of which are diminishing, the battles for industry leadership will be fought primarily between marketing departments. (Reference here is to marketing in the broadest sense). The integrated circuit winners will be those who adapt most quickly to the concepts of systems marketing. This will require knowledge, a heightened sense of responsibility to the customer and increasing dedication to long-range planning. Traditionally, systems sales take a long time to mature. The marketing specialist must be in constant liaison with the customer. His services begin at the time the new product idea is conceived and continues until it is finally produced as finished pieces of equipment.

As used in this Guide, the term of "marketing" covers all functions related to getting the product from the end of the production line into the customer's hands and keeping it there. It is more complete, but fully includes the "sales" function. Included are such factors as pricing, application engineering, sales, market administration, long-range planning, product planning, order service and inventory control.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont)

TABLE OF CONTENTS (Cont)

TABLE OF CONTENTS (Cont)

SECTION 1 INTRODUCTION

1.0 General Considerations

Integrated circuits are changing the appearance, shape, size and modes of operation of electronic equipment. They also are changing the structure of the electronics industry from the methods of doing business to the supplier-user interface. They are causing the emergence of new products and the obsolescence of others. An entire company organization must soon adapt to this change. Unlike the evolutionary transition from tubes to transistors, the switch to integrated circuits is revolutionary. Specific direction must be provided for all parts of a company if this transition is to be accomplished effectively. This includes engineering, production, purchasing, quality control and marketing.

Marketing Specialist's Responsibilities

The marketing specialist must assume new responsibilities within the integrated circuit manufacturer's organization. These include greater interface with the integrated circuit user and systems engineer. He must have detailed knowledge of integrated circuit performance and fabrication to make optimum procurement compromises. He must face the questions, "Should the equipment manufacturer relinquish partial or complete control over the circuits to the integrated circuit supplier?", "What part should each play in their control?"

The marketing specialist will play a major role in resolving these questions. He will thus establish the extent to which a basically satisfactory vendor relationship with the customer is established. Whereas the customer must relinquish some design control to enable satisfactory procurement, at the same time he cannot relinquish all control. The consequences of doing so will soon be his undoing and the marketing specialist will be without a customer. This is a delicate balance. The establishment and preservation of this balance is the place where the successful marketing specialist will play his major role.

Reasons for Increasing Use of Integrated Circuits

The integrated circuit market projections (Figure 1-1) indicate an accelerating upward trend. These projections reflect increasing recognition of the advantages of integrated circuits in replacing discrete components. They are being designed into equipment and systems because of:

1. The lower systems costs with integrated circuits including parts complement, assembly, testing, etc.
2. The savings realized from improved reliability, decreased down-time and ease of maintenance.
3. The savings in size and weight
4. Improved performance capabilities
5. Decreased power requirements, increased battery life and reduced heat sink requirements.

Should Integrated Circuits be Used in a Specific Application

The question of whether or not to employ integrated circuits in specific applications will occur. To properly review the potential of integrated circuits, it is necessary to evaluate the costs of materials, assembly, engineering, tooling, the time differential required for the conversion, value of improved reliability (and warranty), value of improved portability and transportability, etc. Projections of those factors together with the design, production and life span of specific applications can be most revealing. Thus, by complete evaluation of specific situations, the overall integrated circuit impact may be projected. The trend toward Large Scale Integration (LSI) is promising further extention on the already extensive impact of integrated circuits on the electronics industry. (Figure 1-2).

THE TRANSISTOR AND INTEGRATED CIRCUIT GROWTH PATTERN

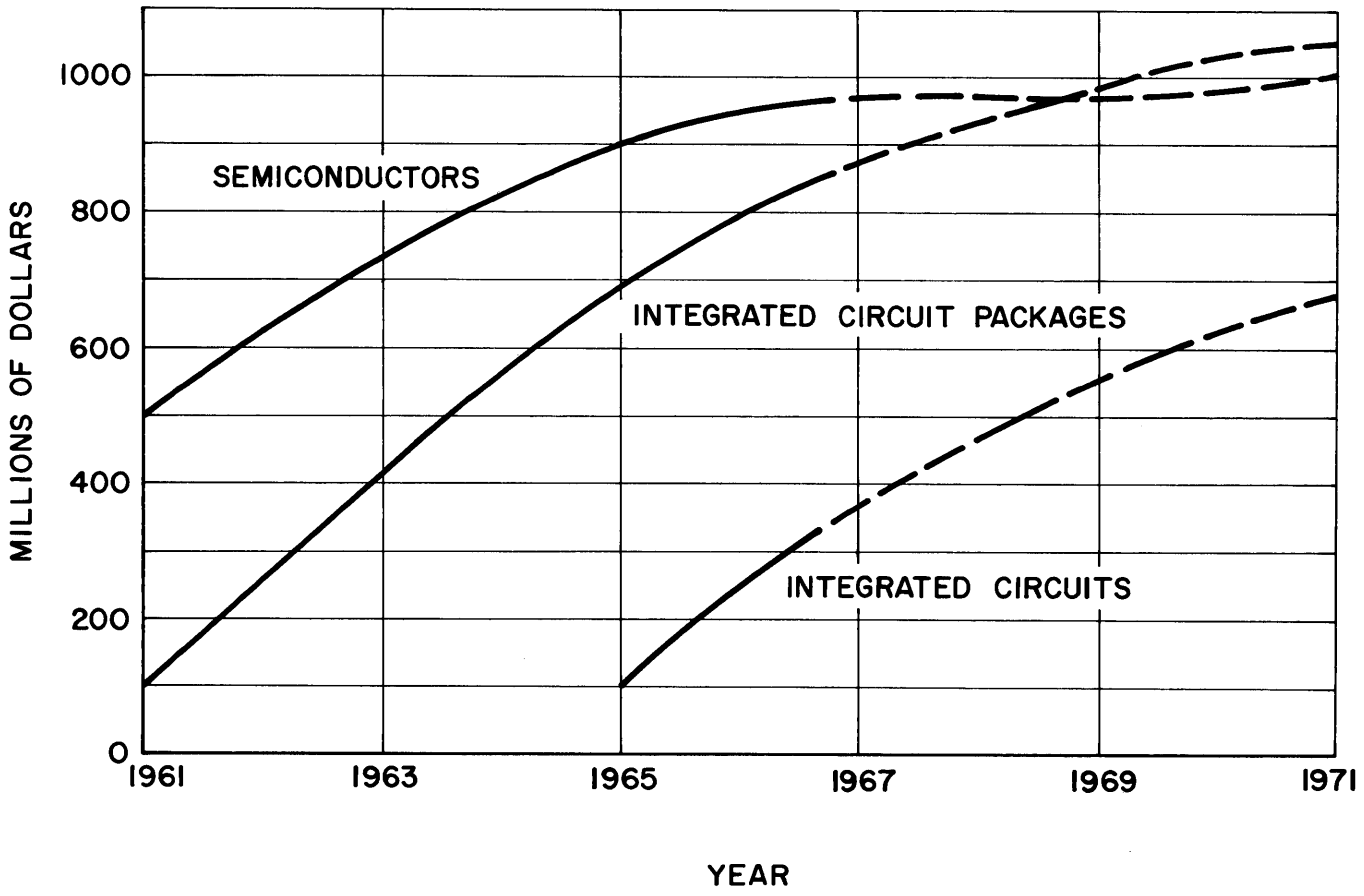


Figure 1-1

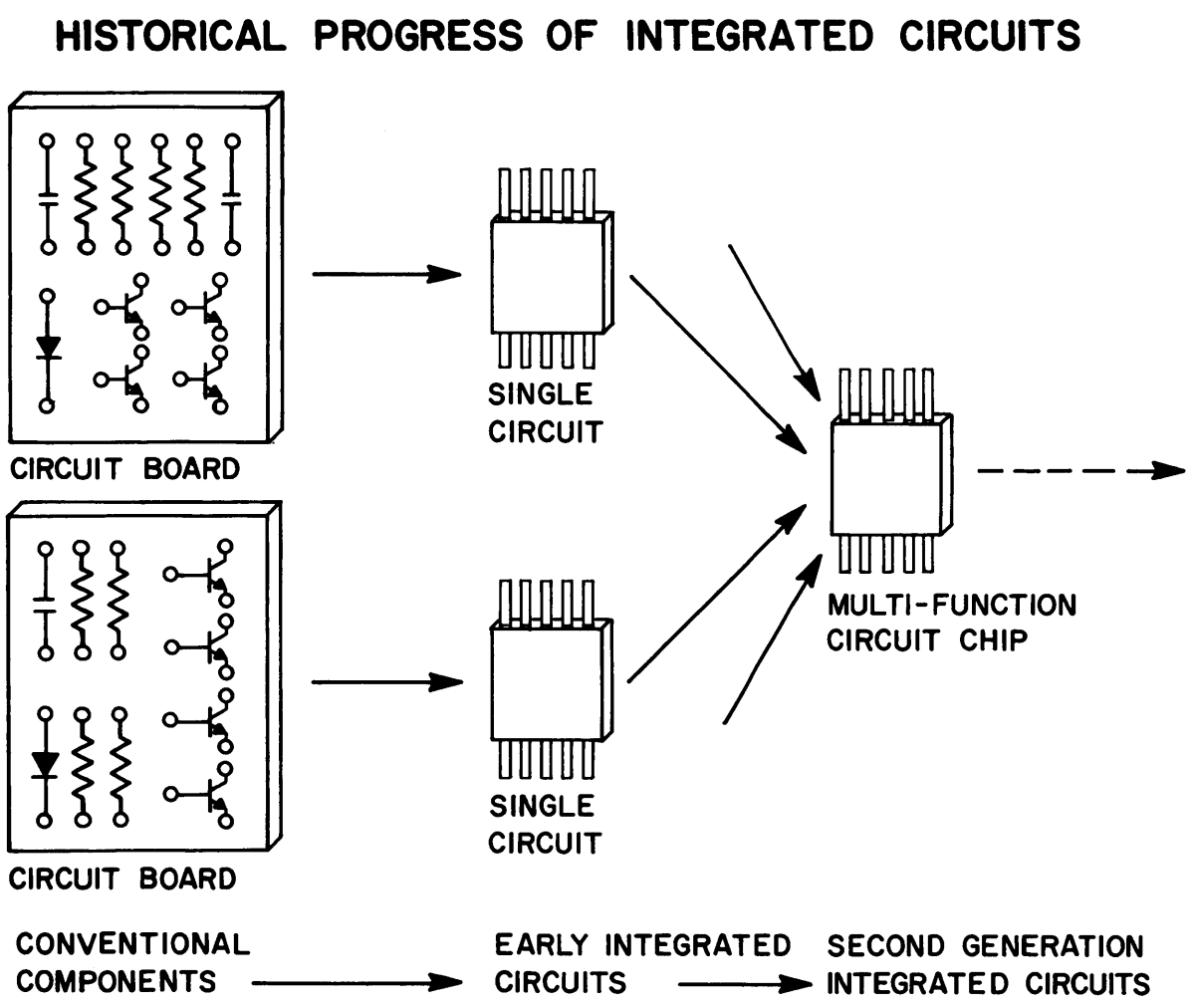

HISTORICAL PROGRESS OF INTEGRATED CIRCUITS
CIRCUIT BOARD
SINGLE CIRCUIT
MULTI-FUNCTION CIRCUIT CHIP
CIRCUIT BOARD
SINGLE CIRCUIT
CONVENTIONAL COMPONENTS
EARLY INTEGRATED CIRCUITS
SECOND GENERATION INTEGRATED CIRCUITS

Figure 1-2

1.0 (Continued)

Also to be considered is the profitability of equipment (using integrated circuits) with respect to sales volume and pricing. Clearly, in many areas, sales volume can be maintained and increased only by conversion to integrated circuits. The ultimate customers are coming to recognize the increased value factors integrated circuits offer and when warranted, are now more willing to accept a related price increase.

System Evaluation of the Use of Integrated Circuits

The supply logistics and marketing strategy to be faced at the onset of an equipment evaluation with respect to its integrated circuit complement include:

1. The desirability (or consequences) of using integrated circuits extensively
2. Integrated circuit supplier capacities
3. How to procure the needed integrated circuits most economically
4. Corporate profitability and future planning
5. Long and near term effects on the company's market position
6. Company organizational changes brought on by use of integrated circuits

To properly evaluate the economic effects of using integrated circuits, the following areas must be researched:

1. The present and future costs of producing integrated circuits and effects of these costs on selling price - (This question requires a basic understanding of the various fabrication processes and all costs associated with them). Each of basic monolithic, thin film and multichip processes must be compared
2. Design changes to permit lower-cost integrated circuits to be utilized without sacrificing performance
3. The economics of timing a changeover and scheduling for maximum profit
4. Enumeration of any differential in engineering and other conversion costs
5. Determining whether the complete system should be redesigned to use integrated circuits
6. The economics of important systems considerations affected by conversion to integrated circuits
7. Determination of the practical problems involved in selling integrated circuits to a commercial customer
8. Evaluation of any new problems in the user-supplier interface generated by the advent of integrated circuits.
9. An assessment of additional technical developments that may be expected and their timing.

1.1 Definition of the Problem

Team Procurement

As is evident, the function of the marketing specialist must be greatly broadened to meet this new and revolutionary integrated circuit technology. Currently, the team concept of procurement on the part of the customer is receiving considerable attention in the literature. It is probable, as the systems merchandising concept becomes more generally recognized and used, that team marketing concepts will be utilized. While difficult to forecast

1.1 (Continued)

exactly, it will certainly include in addition to marketing specialists, representatives from application engineering and perhaps production engineering. The marketing specialist will be expected to act as chairman and provide guidance for this group.

In terms of end products use, of course, the components marketing problem has not changed materially. There are home entertainment equipments, highly reliable military programs and industrial requirements. What has changed drastically are the simple mechanics of implementation.

Change orders, for example, have never been simple, but the complexity of carrying them out with integrated circuits has greatly increased. The problem of acceptance or rejection of given components has become an equally complicated problem. For these and many other reasons, the marketing specialist must have a more intimate and detailed knowledge of not only: a) what these components are; b) how they are made; c) how they actually operate in the circuit, and; d) how their presence affects the full range of systems considerations. This knowledge is requisite carrying out his responsibilities with the greatest effectiveness.

1.2 Marketing "Need-to-Know"

The real payoff for the marketing specialist in any field of endeavor results from being able to show the customer how he can do a job better or cheaper. It comes when he can intelligently discuss requirements with his prospective customer. The ability to do this can only come through detailed knowledge of both his product and the customer's objectives, goals and problems. With background knowledge in only one of these areas, he will have a major communications problem. Presently, many of the user's problems are resulting from this communication weakness. Obtaining the order and holding the customer will frequently depend upon the specialist's ability to get around this problem.

Systems Engineer

Successful marketing in the field of integrated circuits, compared to other components, requires more systems background. The competent marketing specialist for integrated circuits, in addition to other sales abilities, must be a good systems engineer. He must be conversant with integrated circuits and their systems application. Above all else, he must be able to think and talk of them in terms of systems.

Increasing numbers of equipment manufacturing companies are recognizing their need for comprehensive integrated circuit fabrication knowledge. They are either building in-house laboratory facilities or establishing relationships with someone who can build prototype circuits for them. In most cases, the larger electronic company either has access to such facilities or is able to obtain prototypes quickly. Frequently this involves a division or department within the corporate complex. When the customer obtains his prototypes elsewhere, the marketing specialist must be able to determine whether the indicated costs are realistic. The knowledge necessary to do this must be at his fingertips. He must be able to relate process technique to operational parameters and know the safety and yield factors involved. He can expect his opposite numbers on the procurement team to become more knowledgeable in their jobs, but he must be able to assess the accuracy of their representations. The marketing specialist must also screen special requests and frequently act as a restraining or encouraging influence on his own company. He must be able to assure that they are not too quick to agree to difficult specifications, or too slow to agree to more reasonable, easier ones.

1.3 Applications

When circuits were fabricated with discrete components, it was certainly desirable that the marketing specialist understand circuit design, but it was not mandatory. There are examples of discrete component salesmen who managed to survive and even prosper without knowing the difference between a transistor and a diode. This rare individual could not survive long in the marketing of integrated circuits. The systems concept requirement demands that he know circuit design thoroughly and also be familiar with how those circuits are applied. His knowledge must extend to the practical interrelationships and limits within a system.

Digital Circuits

In digital circuits, which are characterized by a deceptive appearance of simplicity, he must know the rudiments of logic design and how his products may be used to implement that design. To that end, an entire section of this Guide is devoted to the fundamentals of digital logic and design principles, together with a detailed discussion of the various families of circuits in current use. He must also handle seemingly enigmatic questions routinely, e.g., why can't a flip-flop capable of 10 MHz response be used at a 10 MHz rate? One steeped in applications realizes that the reset time of the flip-flop usually limits the speed of a 10 MHz device to a 1 MHz rate. In order to serve both his company and his client, the marketing specialist must be able to project himself into the position of the digital logic designer intelligently.

Linear Circuits

Unfortunately, linear (or analog) circuits are not as easily characterized as digital circuits. In absolute sense, a definition of a linear circuit is one which produces an output "analogous" to its input. Common examples of linear circuits include amplifiers, oscillators, detectors, etc. Standards useful for linear integrated circuits have been much slower in development than for digital circuits where nearly all modern computer systems are essentially the same logic building blocks. The variety of linear circuit requirements is virtually infinite. Hence, the development of linear circuitry has lagged behind that of digital circuits.

Large volume requirements for a number of given linear circuits are now appearing. These are primarily differential and operational amplifiers. The number can be expected to grow rapidly as the technology progresses. Up until now, most integrated linear circuits were intended to meet special customer requirements. This has made it difficult to delineate the uses of linear circuits in the same way as can be done with digital circuits. Recent announcements of extensive use of linear integrated circuits in television receivers should add strong impetus to extension of their usage.

A section of this Guide is devoted to linear integrated circuit applications. To cover the required material effectively, it has been necessary to assume that the reader has a basic knowledge of discrete component amplifier design.

So that he can perform the marketing function effectively, the marketing specialist must have a basic knowledge of the practicalities and limitations of integrated circuit linear design. To maintain liaison with the customer, particularly during the formulative stages, he must know the capabilities and limitations of all available integrated circuits and most particularly his own. He must also be able to evaluate new products of his competitors and relate such information to specific applications.

SECTION 2 IMPACT OF INTEGRATED CIRCUITS

2.0 Major Changes Initiated by the Integrated Circuit Concept

There are two major results from integrated circuit usage which will have long-range impacts on most electronics companies as presently constituted. In a sense it is difficult to separate the two. They are: (1) possible loss of "contributed value" in a given product or system; and (2) migration of design control toward the integrated circuit manufacturer.

Contributed Value

"Contributed value" may be defined as that value added to a product or system by the manufacturer; he procures parts and components and assembles them into a useful device or system. His contribution divides into the two major parts-mechanical assembly and design. Obviously, these are variables which differ widely both qualitatively and quantitatively dependent on product characteristics, the market served and ultimate use.

The immediate (and perhaps uninformed) use of integrated circuits on a direct substitution basis inevitably minimizes "contributed value" by an electronic equipment manufacturer. (See Figure 2-1). It is obvious that the integrated circuit represents considerable assembly work that has been done before hand.

One of the clearer examples of this problem is represented by the computer-module manufacturer. A company selling printed boards with discrete components assembled to perform a sequence of digital logic functions can now buy the entire function in one or more small integrated circuit packages. Subject to some justifiable over-simplification, this company can now dismiss almost all of its employees except the marketing staff. This, of course, will be a short-lived arrangement, for the ultimate consumer could as easily bypass this remaining marketing staff and go directly to the integrated circuit vendor.

A somewhat more complex version of this situation may be studied by consideration of the manufacturer of medium priced voltmeters. If he does not react quickly and correctly, one of the kit vendors may market an inexpensive package of integrated circuits and destroy his market within a short period of time – possibly a few months. While this is not nearly as straightforward as the computer-module manufacturer's dilemma, the same forces tend to threaten the voltmeter manufacturer's sales volume.

Design Control

Similarly and related to "contributed value", design control is migrating toward the integrated circuit maker. This happens for a host of obvious reasons as depicted in Figure 2-2.

Circuit Availability

Cost factors dictate that the buyer of integrated circuits uses a standard production item whenever possible. Since these are large volume products, they almost always will be items that the vendor can make at high yields. Hence, in effect, the vendor makes the decision as to many of the product's parameter limits. In a practical sense, many assemblers of hybrid and special circuit packages are finding that the integrated circuit manufacturers are actively resisting the fabrication of these circuits in low volume. This is tending to place major limitations on design freedom.

Basic Design Concepts

Proper utilization of integrated circuits in some systems requires modification of many established design principles. Obviously, the subsystem will be influenced by the previously listed considerations. (Ready availability of standards versus limitations on specials). Perhaps not so obviously, the fundamental design principles of any given system may be equally as affected, or perhaps more so. Frequently an entirely new approach should be undertaken and the entire system redesigned. This requirement may

SHIFT IN CONTRIBUTED VALUE
INTEGRATED CIRCUIT VS. DISCRETE

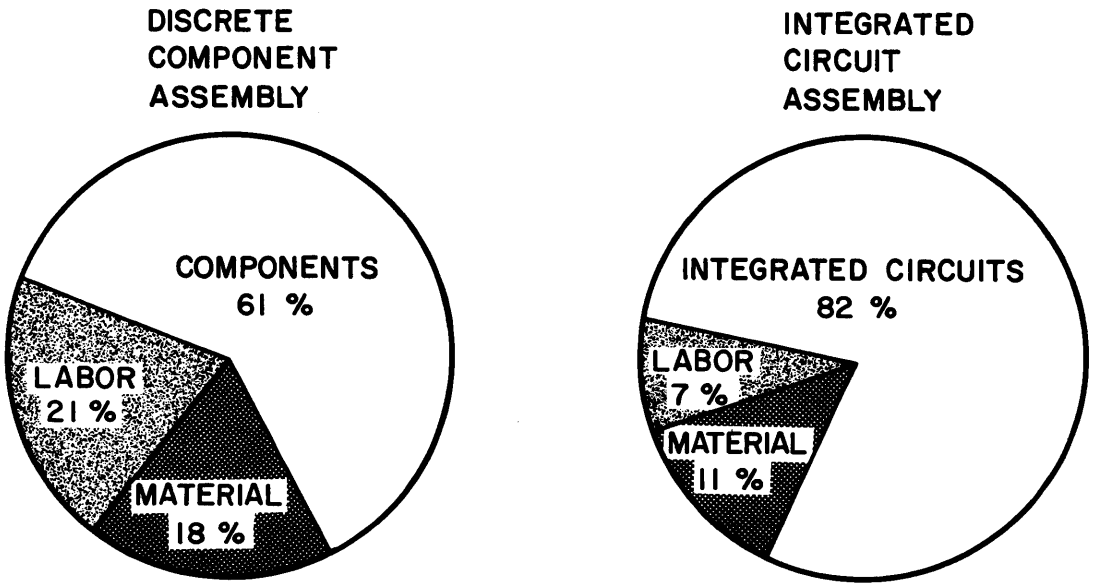


Figure 2-1

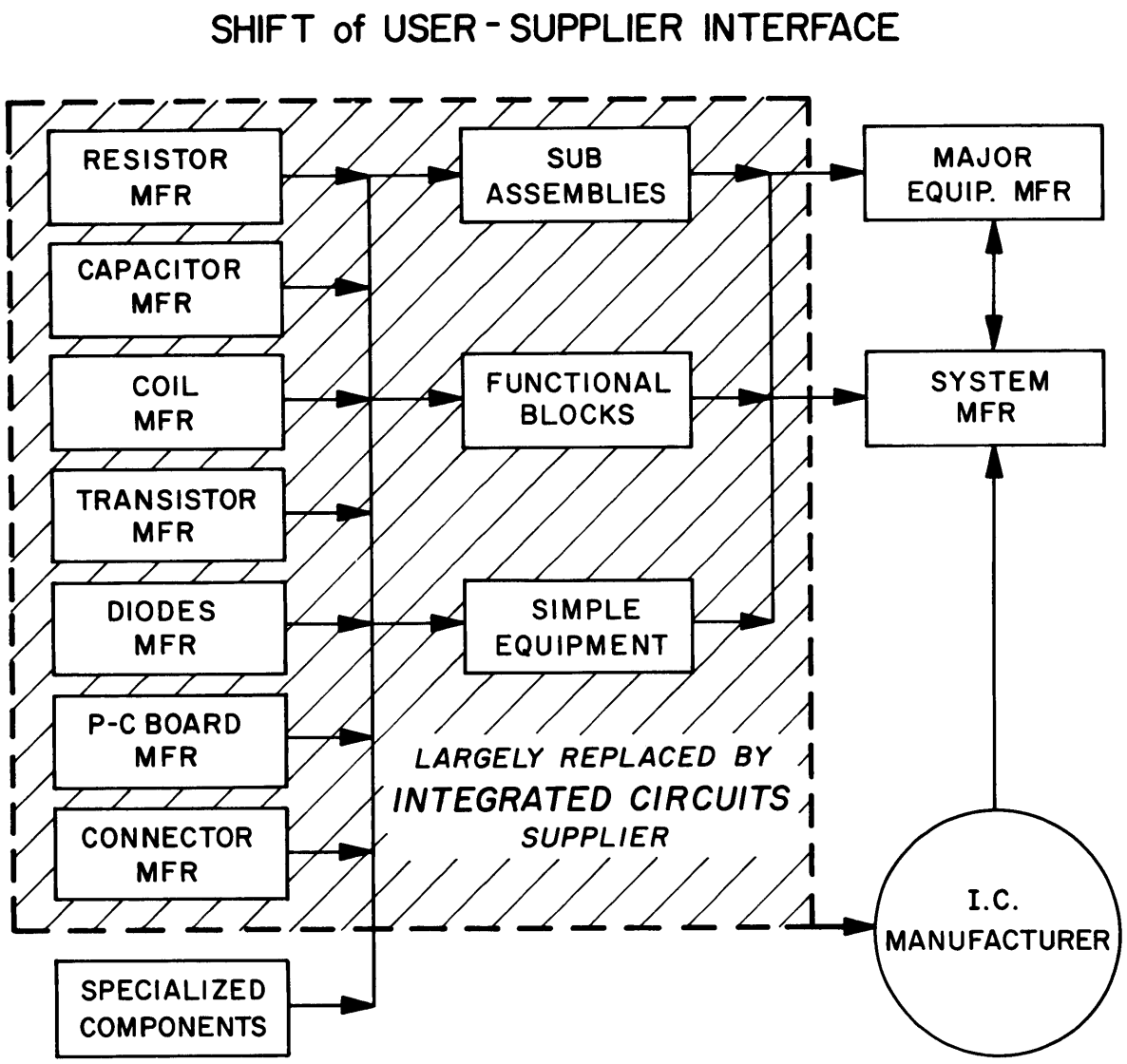

SHIFT of USER - SUPPLIER INTERFACE
RESISTOR MFR
CAPACITOR MFR
COIL MFR
TRANSISTOR MFR
DIODES MFR
P-C BOARD MFR
CONNECTOR MFR
SPECIALIZED COMPONENTS
SUB ASSEMBLIES
FUNCTIONAL BLOCKS
SIMPLE EQUIPMENT
LARGELY REPLACED BY
INTEGRATED CIRCUITS
SUPPLIER
MAJOR EQUIP. MFR
SYSTEM MFR
I.C. MANUFACTURER

Figure 2-2

2.0 (Continued)

extend to long established designs which are considered as standards.

New Design Approaches

To illustrate the desirability and some of the problems encountered in a major system redesign, consider the AM radio. Historically, the standard system design involves a superheterodyne with the IF portion operated at 455 KHz. This frequency was chosen for optimum image suppression in the broadcast band. When this standard first emerged, the technology had not progressed to the point of practical implementation of frequencies of the order of tens of megahertz's.

The 455 KHz IF strip could now be easily converted to integrated circuits, but little is accomplished from any point of view. Little space and weight savings could be realized because the inductors can't be integrated, hence, remain the same size. As externally connected components, they would limit assembly cost reductions. Since reliability is relatively unimportant, there would be little incentive to make this conversion.

Basic system's consideration reveals that 12 MHz is almost ideal in terms of integrated circuit capability. The inductors become quite small. The image problem disappears entirely. In addition, the oscillator tuning range is now only some 10 to 15% (12 to 13.5 MHz) versus the former 350% spread (455 KHz to 1600 KHz). The number of external components required becomes minimal so that major economies now offer the incentive to convert from discrete to integrated circuits. The foregoing example serves to illustrate the changes required in systems design. On this basis, full utilization of the advantages of integrated circuits can rapidly extend their usage.

2.1 Economics

Prices in mature industries are established by adding a reasonable profit to actual production costs. The resultant sales price must be competitive to obtain a sufficient share of the market and profitable to protect investment. The newness of the integrated circuit market precludes such price maturity. Reasonably accurate price projections based on past experience have been established. It is expected that the integrated circuits prices will follow the pattern of the transistor market.

Yield

Actual integrated circuit processing costs are reasonably well known. These cost factored by yield produce the unit cost. Yield is the ratio of the number of acceptable units to the total possible from material started through the process. The total processing cost divided by the number of acceptable units (or multiplied by yield) gives the desired unit cost figures. In the past, yield figures were considered highly proprietary by almost all semiconductor manufacturers. However, as the major integrated circuit manufacturers approach the 75% yield mark (and they must), this factor will become less important.

Integrated circuits must be produced in considerable quantities so that the supplier may realize profits. Currently, the supplier will lose money if he does not maintain a volume of production with rates in excess of 100,000 units per week. The average sale price of integrated circuits during 1965 was about $8. Bids for delivery from future production (one to three years) are typically about $2.50 for large quantities over the scheduled production period.

Position of Major Suppliers

Today's typical large manufacturer of integrated circuits employs about 1,000 people in the integrated circuit phase of his operation. A total annual business approximately $12,000,000 is required to

2.1 (Continued)

support this phase. A large operation can now produce 20,000 units weekly. With an annual volume of 1,000,000 units, the average price per unit, $12., is required for profitability. The same 1,000 employees would need to produce four million units annually to bring the profitable selling price down to $3. The total integrated circuit market in 1965 was slightly over 7,000,000 units. See Figure 2-3 for performance by major manufacturers.

Die Cost

For a volume (1,000 wafers/week) user of silicon, the epitaxial wafers cost about $5. each. The wafer is a slice of silicon about 1 inch in diameter and 0.007 inch thick. The various processes, i.e., diffusion, masking and metalization, cost about $15. per wafer in direct factory labor and overhead at the 1,000/week rate. The number of circuits possible per wafer varies from 20 to possibly 500.

Using 400 as an average, it now must be determined how many of the circuits are acceptable (yield). Thus, a whole wafer of 400 possible chips cost $5. + $15. = $20. A yield of only 1% would mean each chip costs $5. Consider Table 2-4 for a more complete review of this typical yield versus factory cost situation.

Cost vs Volume

Production economy as well as proportion reduction in overhead costs can be realized as production increases. This factor was implicit in the previous discussion of minimum profitable selling price. The curve of relative unit cost versus weekly production rate is shown in Figure 2-5. The optimum size for "production unit" has not been established.

2.2 Drives Toward Integrated Circuits

The economics of production and in-service reliability are presently providing the principal motivation for use of integrated circuits. Frequently, they are less costly to manufacture and assemble than the circuits which they are replacing. The reason for the gain in production economics is inherent in the "batch process" which is employed in making silicon integrated circuits. A single one inch wafer of silicon can contain several hundred circuits and constitutes a "batch". In parts of the process, numerous wafers (20 to 50) can be accommodated simultaneously – irrespective of the exact circuit configurations being produced.

Batch Process

The manufacturing costs of integrated circuits are substantially less than the equivalent in standard component form. A total system comparative cost analysis must include assembly, cost of research and development, servicing and warranty cost, out of service cost and values attributable to size and weight. The lower production cost is particularly enticing because it is coupled with improved reliability. The improved reliability, in turn, reduces the total operating cost. Figure 2-6 shows, graphically, several of these comparisons.

Reliability

Several Military organizations have made extensive studies of cost associated with reliability of electronic systems. They based these studies on the number of weapon systems immediately available for use. They included the cost of check out at regular intervals to insure immediate use, down-time and likelihood of failure during a mission. They made detailed analyses of times out-of-service due to electronic failure. These studies indicate that a savings of a minimum of several billion dollars in total defense system cost should result from employment of integrated circuits. This saving is providing the principal drive from all defense agencies for specification of integrated circuits in all future weapon systems. It is also the impetus to rapid conversion of existing systems.

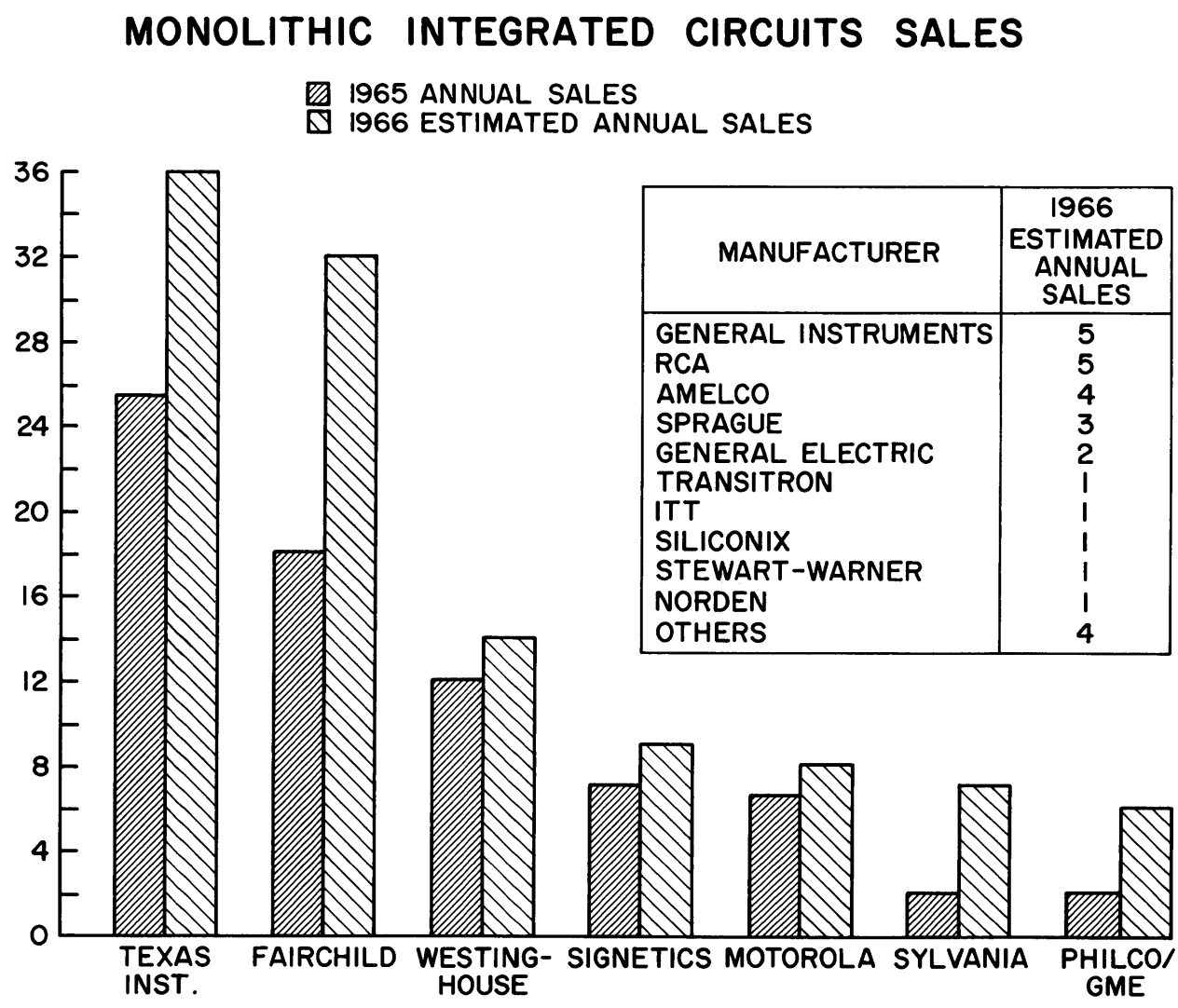

MONOLITHIC INTEGRATED CIRCUITS SALES
1965 ANNUAL SALES
1966 ESTIMATED ANNUAL SALES
36
32
28
24
20
16
12
8
4
0
TEXAS INST.
FAIRCHILD
WESTING-HOUSE
SIGNETICS
MOTOROLA
SYLVANIA
PHILCO/GME
MANUFACTURER
1966 ESTIMATED ANNUAL SALES
GENERAL INSTRUMENTS 5
RCA 5
AMELCO 4
SPRAGUE 3
GENERAL ELECTRIC 2
TRANSITRON 1
ITT 1
SILICONIX 1
STEWART-WARNER 1
NORDEN 1
OTHERS 4

Figure 2-3

INTEGRATED CIRCUIT FACTORY COST vs YIELD

YIELD	CIRCUIT CHIP COST	TESTING AND PACKAGING COST (TO-5)	FACTORY COST
1%	$ 5.00	$ 1.20	$ 6.20
2%	2.50	1.00	3.50
3%	1.67	0.85	2.52
4%	1.25	0.60	1.85
5%	1.00	0.50	1.50
10%	0.50	0.40	0.90
20%	0.25	0.35	0.60
30%	0.17	0.30	0.47
50%	0.10	0.30	0.40
60%	0.08	0.30	0.38
100%	0.05	0.30	0.35

Table 2-4

PRODUCTION COST vs VOLUME of I.C. PRODUCTION

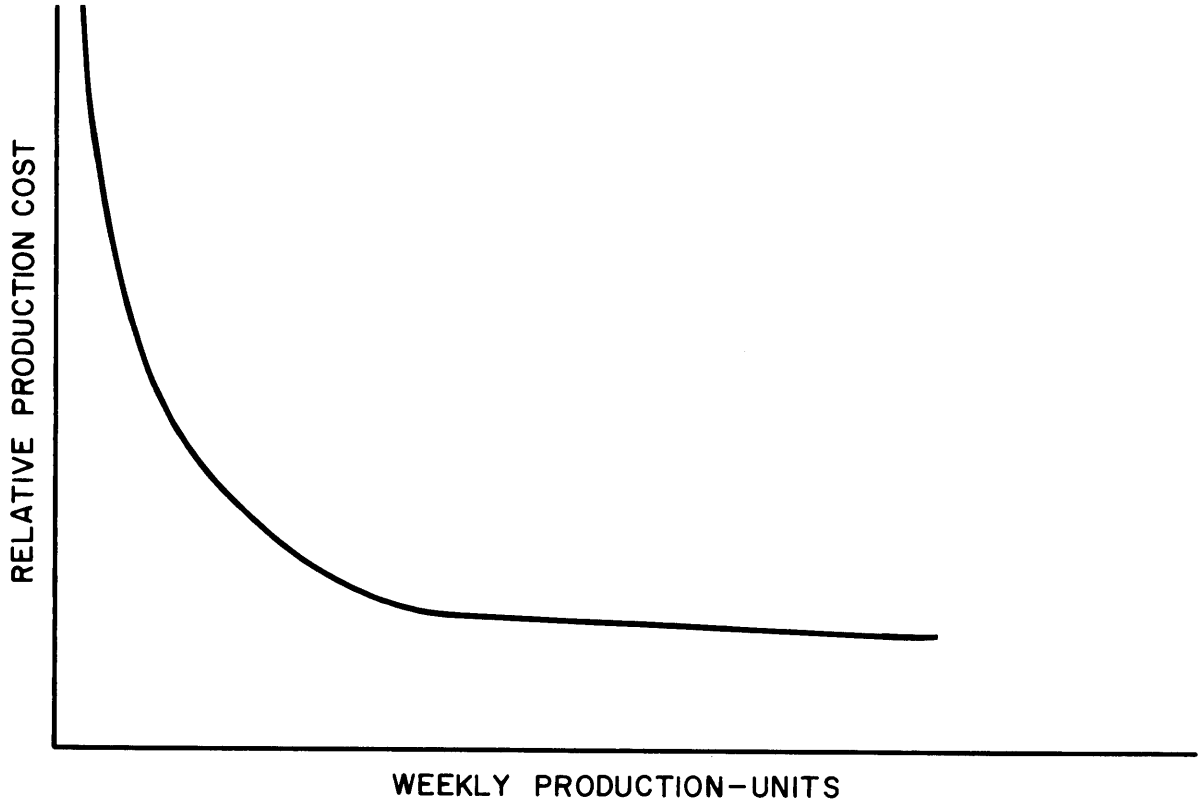


Figure 2-5

THE EFFECT OF INTEGRATED CIRCUITS ON EQUIPMENT DOWN TIME AND MAINTENANCE COST

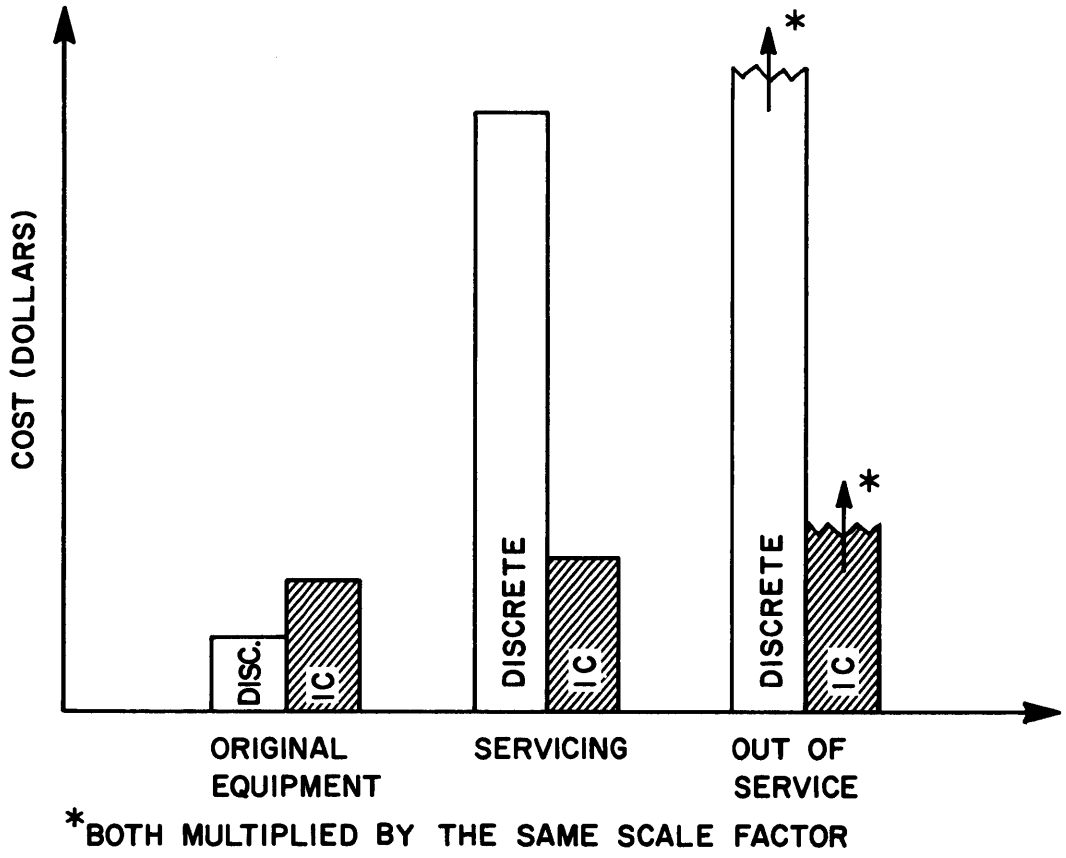


Figure 2-6

2.2 (Continued)

The commercial computer industry has changed to integrated circuits in almost all new designs because of the lower cost of integrated circuits as compared to conventional components, without sacrifice of reliability. Estimates place the cost of the type of integrated circuits in the IBM 360 computer at $0.40 each; monolithic circuits as used in the RCA SPECTRA 70 may be as low as $0.30 each. This estimate supposes that several circuit functions are placed in each integrated circuit package.

Profit Margins

Although the cost savings for the commercial electronic market may not be as great, the slim profit margins available in many areas of today's market amplify economic differences. A saving of 4% on the total sales dollars would double the profit margin for the entire electronics industry. Shrewd management is recognizing the value of savings through intelligent use of integrated circuits.

Most prognosticators predict that the consumer products industry will be the last to utilize integrated circuits. The fiercely competitive nature of this business is already accelerating the utilization of integrated circuits beyond expectations. At least one of the major manufacturers of consumer products is currently building an integrated circuit production facility to satisfy consumer goods requirements. One of the Japanese semiconductor suppliers is designing an integrated circuit 455KHz IF amplifier for use in broadcast radios.

Stewart Warner has recently announced a facility with large capacity for production of integrated circuits in chip form. This clearly implies their belief in a profitable market for chips which allow the equipment manufacturer to assemble the final microelectronic circuits. The major business leaders of the semi-conductor industry have placed the cost of producing circuit chips at less than ten cents. The lowest estimated has been $0.02 each.

2.3 Size of Integrated Circuit Market

The size of the integrated circuit market is limited only by the total number of electronic functions which they can perform economically. Of the entire electronics market, at present about 70% of the circuit functions are or shortly will be within the performance capability of integrated circuits. Gadgetry or new applications successfully appealing to the massive commercial market could increase the total market far beyond any existing projection. These might be based solely on integrated circuit capability.

The total electronics industry in 1965 totaled approximately 17.2 billion dollars and is estimated to be 20 billion dollars in 1968. Of these totals, all components comprise 4.4 billion dollars in 1965 and 5.3 billion dollars in 1968.

The integrated circuits market totaled 90 million dollars in 1965 and is estimated at 210 million dollars for 1968. This growth is particularly impressive when compared with that for all components of the entire electronics market. Their profound effect on the electronics industry is better appreciated when one considers both the integrated circuit production growth rate and share of the components market.

2.4 Reliability

When properly fabricated and applied, the reliability of integrated circuits is better than their equivalent in conventional components form. The typical system reliability improvement factor is estimated by most users at about four to one. Greater improvement claims await only the agonizingly slow aggregation of substantiating data. Leading authorities have stated that absolute proof of the reliability of these new devices will have to await the passing of several generations of mankind. Step-stress testing techniques

2.4 (Continued)

are being evaluated extensively as a possible answer to this problem.

Reliability Assurance

Purchasers of integrated circuits have the burden of verification of the vendor's reliability level, particularly with its effect on the specific end-use system reliability. Historically, duplication of a vendor's life test facility and reproduction of tests have been found to be prohibitively expensive. Two techniques are commonly used to avoid the necessity of duplication and to produce verification.

1. Extensive testing of all parameters to assure normal distribution of each

2. Detailed process certification with or without surveillance to gain assurance that no unapproved changes have taken place.

Military inspectors and specifications are widely employed for these purposes. The same techniques are widely used in non-military applications.

Good engineering judgement has generally prevailed with most users seeking a compromise between the two extremes of maximum protection and minimum cost.

Process Changes

Unfortunately, due to technological evolution with its associated process changes, the long term history established for some products may not apply to more recent purchases. Fortunately, new quality control techniques, such as step-stress testing and failure analysis, are providing a degree of reliability assurance. While not a complete substitute for life testing, these techniques effectively reduce the time required to obtain results in reliability investigations.

Accelerated Testing

Step-stress testing involves increasing the applied stress beyond ordinary limits, thus forcing the units to fail. By adjusting the stress in discrete steps and noting the failure rate of each stress level, extrapolation provides an acceleration factor which relates the test results to ordinary stress levels.

Control Patterns

Control pattern testing is another new technique developed specifically for integrated circuit use. While it has not been widely publicized, it is rapidly becoming popular. Control patterns are special areas on each slice where standard devices, circuits, or patterns are fabricated. By design and test, these relate to process control and show failure mechanisms.

The intelligent use of a control pattern concept can further reduce reliability costs for both user and supplier. The control pattern can also be used to correlate between different vendor's quality control methods, provided each uses the same pattern. This technique is particularly useful for comparing in-house with outside source of supply.

Interconnections

Interconnections have been recognized as the worst reliability problem to arise since transistors replaced vacuum tubes. The most reliable interconnection method is based upon an adherent thin metal film deposited by vacuum evaporation on a smooth compatible substrate. Such metallurgical interfaces are used for the interconnections within the integrated circuits. The leads between package posts and the circuit, and the lead seals providing the hermetic seal entering the package are also selected for compatibility. In the packaged integrated circuit, the closure provides

2.4 (Continued)

additional protection for the metalization and interconnections.

Reliability Through Redesign

Replacing passive resistor and capacitive components with transistors frequently enhances the circuit reliability. By the use of dynamic characteristics, transistors can either replace or multiply the effects of smaller resistors or capacitors, normally resulting in power and space savings. Except for their space allowance on the wafer, adding transistors presents no difficulty and is no more expensive to fabricate. Using these facts, improved reliability may be obtained through use of low power dissipation and redundancy. The same technique in discrete form usually results in offsetting reliability changes, accompanied by large increases in cost. Discrete transistors are far more expensive than most resistors and capacitors. The lower power operation would produce reliability improvement, which would be offset by the deterioration of reliability caused by the increased number of intermetallic interconnections.

2.5 Review of Present-Day Integrated Circuit Performance

Monolithic silicon, multichip hybrid and thin film (with silicon active elements added) are the three most common forms of integrated circuit. Integrated circuits of each type have been used in various types of equipment during the past several years. Many have been successful because of careful circuit design which has taken advantage of the strength and minimized the weakness of each approach.

Silicon Monolithic

The silicon monolithic approach has been favored principally for logic circuits. Two underlying factors have contributed heavily to this result.

1. The range of values and tolerances of components used in most logic circuits are compatible with monolithic construction; and,

2. Systems employing logic circuitry normally require large quantities of a small variety of types of circuit.

A recent tabulation showed that approximately 300 types of logic circuits, excluding custom designs, are available from about 20 different commercial suppliers. The circuit functions ranged in complexity from relatively simple gates to complete shift registers (using MOS technology).

Comparison of circuit performance of the various types of integrated logic circuits should consider specific application. One convenient method of summarizing them portrays propagation delay as a function of power dissipation (for one logic stage). This shown by the family of curves in Figure 2-7. The different curves apply to different types of logic.

Speed-Power

A further interesting correlation indicated in Figure 2-7 is the series of dates. They reflect the fact that the first available integrated circuits were inherently slow, with propagation delays of the order of 100 nanoseconds. As improvements were made in the technology, it has become possible to design and produce faster circuits. Propagation delays of less than one nanosecond are now commercially available. It should be noted that propagation delay and power dissipation may not be the most important considerations in a given system.

The variety of commercially available silicon monolithic integrated circuits for analog applications has been considerably smaller in number. This may be attributed both to the limited range of passive circuit elements available and to the smaller amount of standardization for such circuit applications. The most popular types of

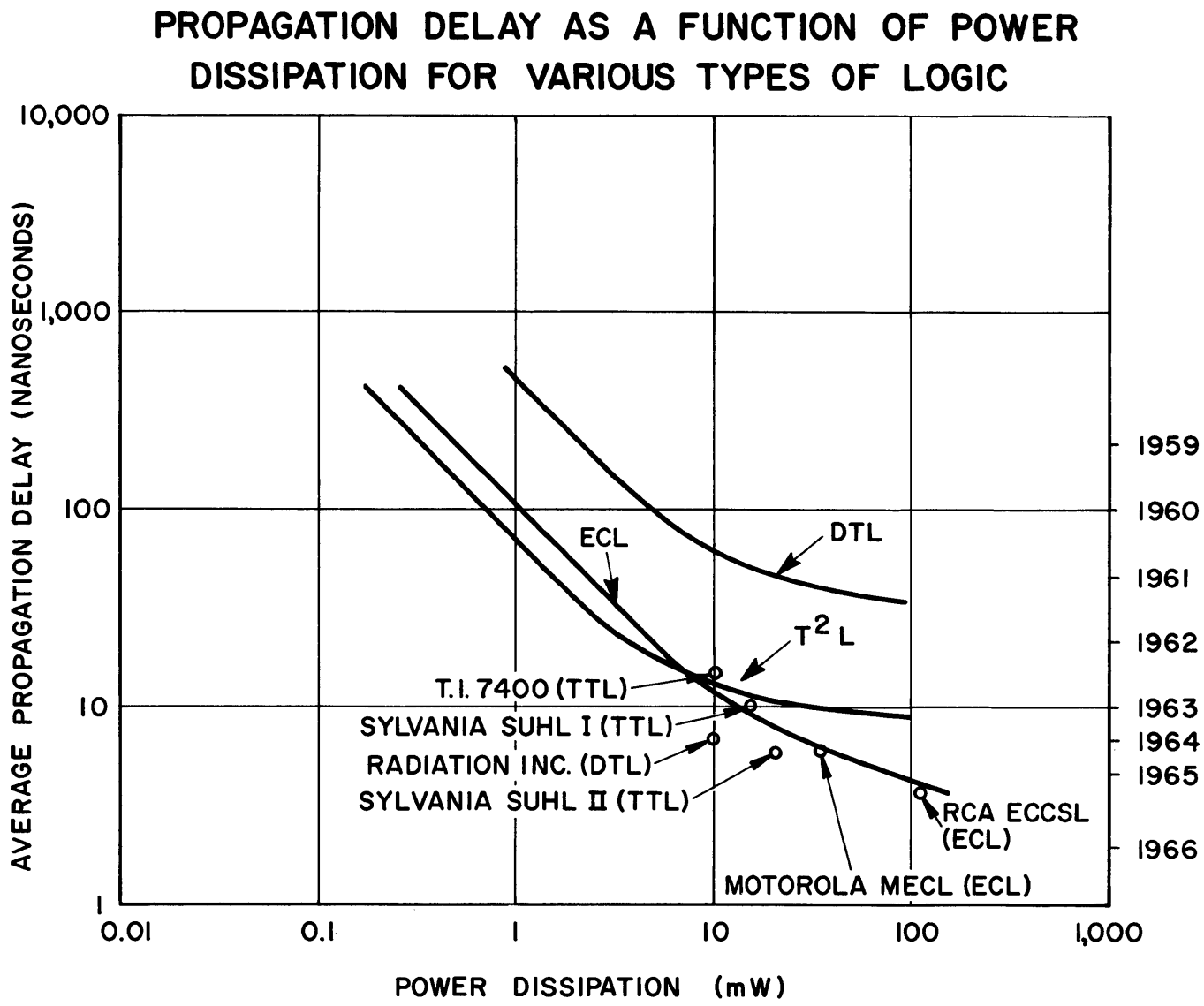

PROPAGATION DELAY AS A FUNCTION OF POWER DISSIPATION FOR VARIOUS TYPES OF LOGIC
AVERAGE PROPAGATION DELAY (NANOSECONDS)
10,000
1,000
100
10
1
0.01
0.1
1
10
100
1,000
POWER DISSIPATION (mW)
ECL
DTL
T²L
T.I. 7400 (TTL)
SYLVANIA SUHL I (TTL)
RADIATION INC. (DTL)
SYLVANIA SUHL II (TTL)
RCA ECCSL (ECL)
MOTOROLA MECL (ECL)
1959
1960
1961
1962
1963
1964
1965
1966

Figure 2-7

2.5 (Continued)

circuits within this broad classification are the differential and operational amplifiers. Recently growing in popularity has been a series of general purpose operational amplifiers. They are characterized by fairly large gain bandwidth products of the order of 1000 MHz. The user, by adding external shaping networks, may modify them to meet the needs of his particular application.

Multichip and Thin-Film

It is most difficult to catalog the various types of multichip hybrid and thin-film integrated circuits available today. There are many different types, and almost no standardization either for logic or analog applications. In addition, an even wider range of passive networks may be included within this group, classified as subcircuit modules. Typical of a few applications for this type of circuitry are the following:

1. 32 TRL (Transistor-Resistor-Logic) NOR gates fabricated on one panel, comprising 128 deposited resistors and interconnections;

2. A four-stage 70 MHz IF amplifier having an overall gain of 60 db and bandwidth of 40 MHz; and, of course,

3. The IBM 360 computer logic noted above.

2.6 MOS Integrated Circuits

The MOS (Metal-Oxide-Silicon) transistor has recently become practical and is now being used in integrated circuits. The basic operating principles of field effect devices have been know for many years. Some of the original patents have run out. They have only been practical to produce within the past few years. The principal production problem has been control of ionic contamination in and on the silicon dioxide. This is a most useful by-product of the planar process. Within the past year, understanding of ionic contamination has been increased. This technology has resulted in new fabrication techniques which produce practical and reliable MOST devices.

Yield Complexity

The yields of integrated circuits using MOS devices appear to be equivalent to that of other monolithic integrated circuits. Yields of typical configurations have been ranging from 10 to 50%. These yield figures may be somewhat misleading because the MOS integrated circuit may have the complexity of a 20 bit to 100 bit shift register, and the others the complexity of a JK flip-flop. This also means that the chip size with MOS devices is usually considerably larger. Typical bipolar integrated circuits are approximately 50 by 50 mils whereas an average size of 75 by 75 mils would be more appropriate for MOS fabrication.

Economics

More startling economic factors result from the higher component density involved with MOS technology. While these devices are limited to frequencies up to one or two megahertz's, they compensate by utilizing very low power levels. The power ratio between bipolar and MOS circuits may be 25 to 1 for a practical digital circuit system. In addition, MOS fabrication requires less wafer processing, hence costs are lower. This condition partially offsets their larger die size. A typical 50 by 50 mil bipolar JK flip-flop die may be obtained for as little as $0.08 each (factory cost). The equivalent MOS die, containing about 8 flip-flops, could be fabricated for approximately $0.20 each. If the MOS packaging cost was less than $2.40, and since the packaging cost for bipolar types is approximately $0.30 per circuit, a substantial saving in package cost would be apparent. A typical MOS integrated circuit requires a larger number of leads - possible 16 to 20 versus 12. The increased packaging cost is far less than the ratio of equivalent circuit functions. On an equivalent basis, therefore, a digital counter

2.6 (Continued)

might cost approximately $9.31 in bipolar form and about $2.99 in MOS form.

Tooling Costs

The impact of MOS technology on digital systems can be expected to be greater than previously experienced. Almost 80% of the available MOS circuit configurations are special designs. Each package must contain too large a part of the system for utilization in the form of simple repetitive flip-flops and gates. In practice, a considerably lower tooling cost should be developed for the MOS integrated circuits. One vendor presently is willing to tool a special MOS circuit and deliver a single wafer for $2,000. More startling is their willingness to fabricate the single wafer for $200, if the customer furnishes the mask.

Where the MOS technology is applicable, it appears to offer a substantial cost advantage. Integrated circuits without MOS devices may produce major cost reductions in electronic equipment by ratios of 2 or 3 compared with discrete components. MOS technology may provide an additional 2 to 3 (to 1) improvement for a total reduction ratio of as much as 10 to 1.

The trend is clear. The use of MOS integrated circuits may be expected to increase rapidly in the immediate future and become an important member of the broadening integrated circuit family.

SECTION 3 SYSTEMS CONSIDERATIONS

3.0 Introduction

The profitable utilization of integrated circuits is based upon reductions in material costs, assembly cost and improvements in performance factors, i.e., size, weight, reliability. Overhead cost reductions develop from the reduced number of suppliers, simplified QC and inspection procedures, and a more standardized parts inventory. Other factors which may result in indirect savings are simplified inventory control, reduced reaction time and increased production-volume capabilities from a given facility.

Integrated circuit systems considerations include the purely economic as well as other problems. Among these, the discussion in this section includes:

1. The portion of the equipment which can and should be converted from discrete components to integrated circuits
2. Timing the conversion to integrated circuits
3. Total systems cost, both qualitative and quantitative, for: cost of materials, assembly cost, repair and maintenance, out-of-service costs
4. Systems assembly problems
5. Gains in reliability
6. Power dissipation considerations
7. Reduction in size and weight
8. Specifications for systems.

3.1 Percentage of Integrated Circuits in Systems

The circuit functions which should be converted to integrated circuits in any particular electronic equipment are determined by two factors:

1. Technical feasibility and performance of the circuit function
2. The total economics of performing particular circuit functions in integrated form.

In addition to these two basic considerations, there may be other qualitative factors which may affect the decision, such as risk of nondelivery, loss of contributed value and revelation of proprietary information.

Circuits Capable of Integration

The percentage of circuit functions capable of being fabricated in integrated circuit form varies from almost 100% for digital functions to between 40 and 70% for radar and communications equipment. A forecast of the rate of conversion to integrated circuits for various areas of application is shown in Figure 3-1.

Conversion From Discrete to Integrated

Considerable experience is required to make the most favorable conversion from discrete to integrated circuits. An approach which attempts to convert directly on a function for function basis, with no system redesign, is usually doomed to failure. The entire system should usually be redesigned to most fully realize the advantages of integrated circuit construction. Such a system redesign may involve only simple changes, such as lower voltage power supplies, acceptance of broadened tolerances, different physical layout, etc. Major redesign may entail the use of entirely new concepts such as signal reconstruction within the system from linear to digital and back to linear.

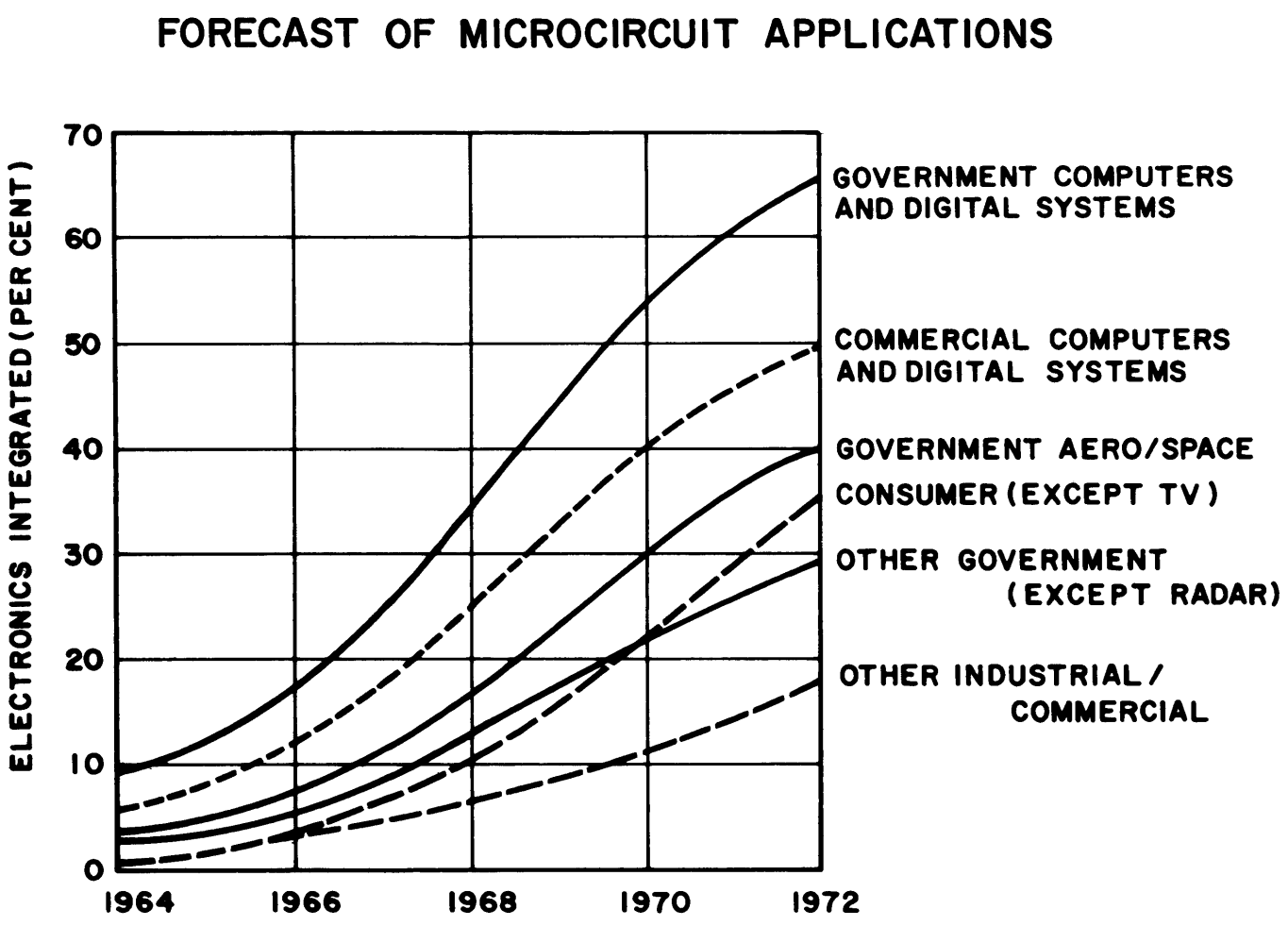

FORECAST OF MICROCIRCUIT APPLICATIONS
ELECTRONICS INTEGRATED (PER CENT)
70
60
50
40
30
20
10
0
1964
1966
1968
1970
1972
GOVERNMENT COMPUTERS AND DIGITAL SYSTEMS
COMMERCIAL COMPUTERS AND DIGITAL SYSTEMS
GOVERNMENT AERO/SPACE
CONSUMER (EXCEPT TV)
OTHER GOVERNMENT (EXCEPT RADAR)
OTHER INDUSTRIAL / COMMERCIAL

Figure 3-1

3.1 (Continued)

Rules for Conversion

The following rules for conversion are obviously general and may not hold for a specific requirement. They are presented as a guide:

1. Only standard packages should be used
2. Power dissipation should be maintained at less than 200 milliwatts per package
3. The propagation delay allowed for a function in a digital design should be at least two nanoseconds
4. Linear circuit functions should be limited to a maximum of 500 megahertz
5. Multiple sources of supply should be favored.

A mixture of integrated circuits supplemented by discrete components may frequently be the proper conversion decision. The economics of redesign for integrated circuits may dictate that some circuits be maintained in discrete form.

3.2 Timing

Profitability

Most engineering managers realize the important effect of timing on profitability. Almost every advanced engineering group is convinced that they will be designing with integrated circuits in the future. At present, the problem facing the industry is to establish the optimum switchover procedure. The costs of premature action can be as large or larger than losses in revenue due to the obsolescence of not changing.

Cost Projections

The average cost of transistors and other semiconductor components has been decreasing at the rate of about 27% per year while the price decreases in integrated circuits are averaging 50% per year (Figure 3-2). The equipment cost analysis must include the price projections of both transistors and integrated circuits. The projections shown are particularly interesting because integrated circuit prices (despite their greater complexity) are converging with those of transistors. The probable production rate of the equipment must also be included in these projections. Figure 3-3 shows a curve of typical production rate versus time of the equipment's production life.

The timing problem's solution becomes the selection of one of the three following options:

1. Continue with existing discrete component circuit designs
2. Change to integrated circuits at some time during the life production of the equipment
3. Begin production with a new equipment design utilizing integrated circuits.

Making the proper selection is not simple. Price projections, engineering and conversion costs, start-up delay and other cost variables must be determined and totaled over the useful life of the equipment. Figure 3-4 shows a typical summation of cost for the two basic approaches. The space between curves on the vertical scale represents the accrued net difference. Making the switch to integrated circuits represents a sizable investment which must be recovered over the production span of the equipment if reasonable profits are to be maintained.

3.3 Total System Cost

Total systems cost includes a variety of factors in addition to the purchase price of the components, and assembly and test. These additional factors range, primarily, throughout overhead cost areas, but also include the intangibles such as service and warranty costs.

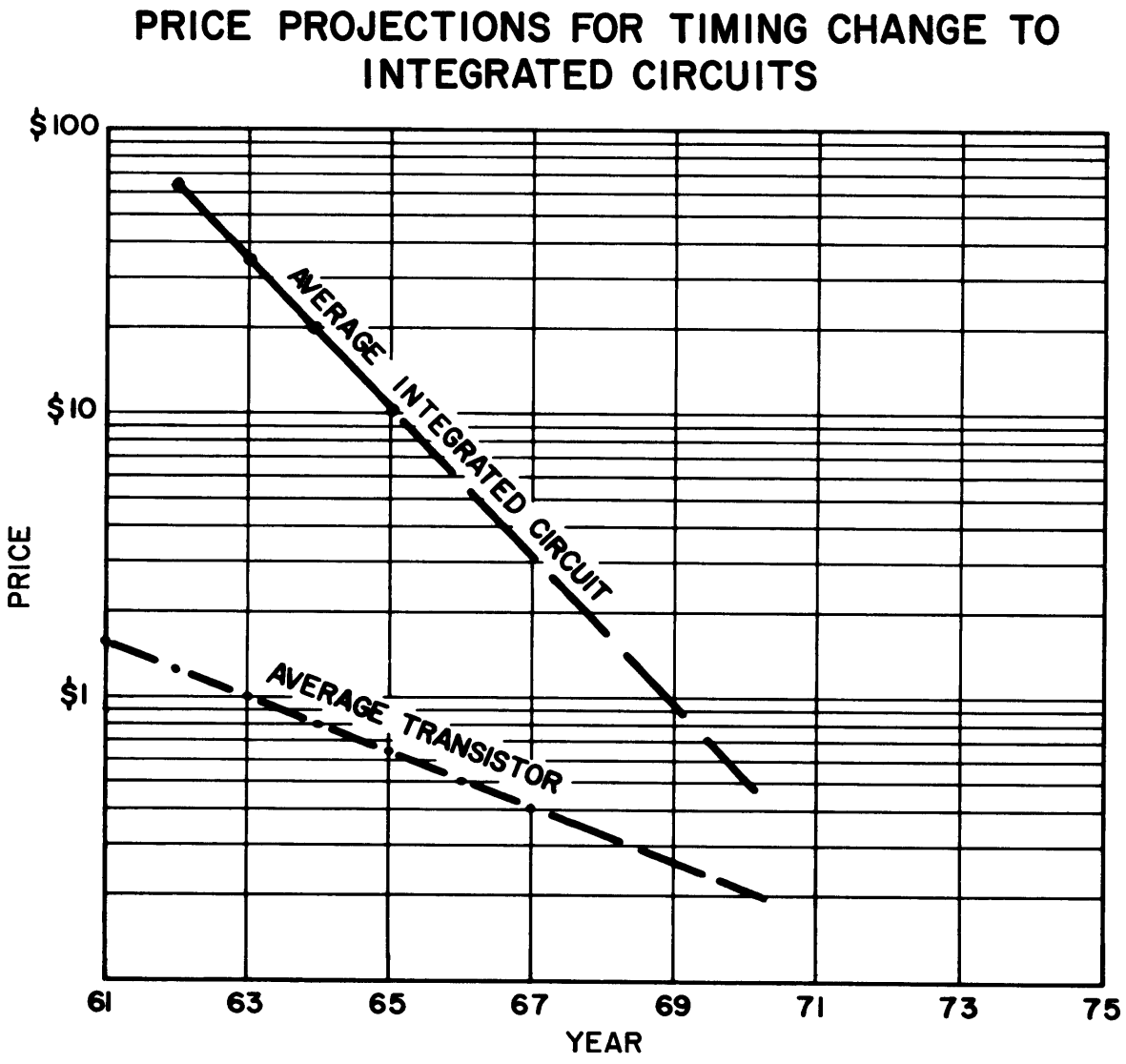

PRICE PROJECTIONS FOR TIMING CHANGE TO INTEGRATED CIRCUITS
$100
$10
$1
PRICE
AVERAGE INTEGRATED CIRCUIT
AVERAGE TRANSISTOR
61
63
65
67
69
71
73
75
YEAR

Figure 3-2

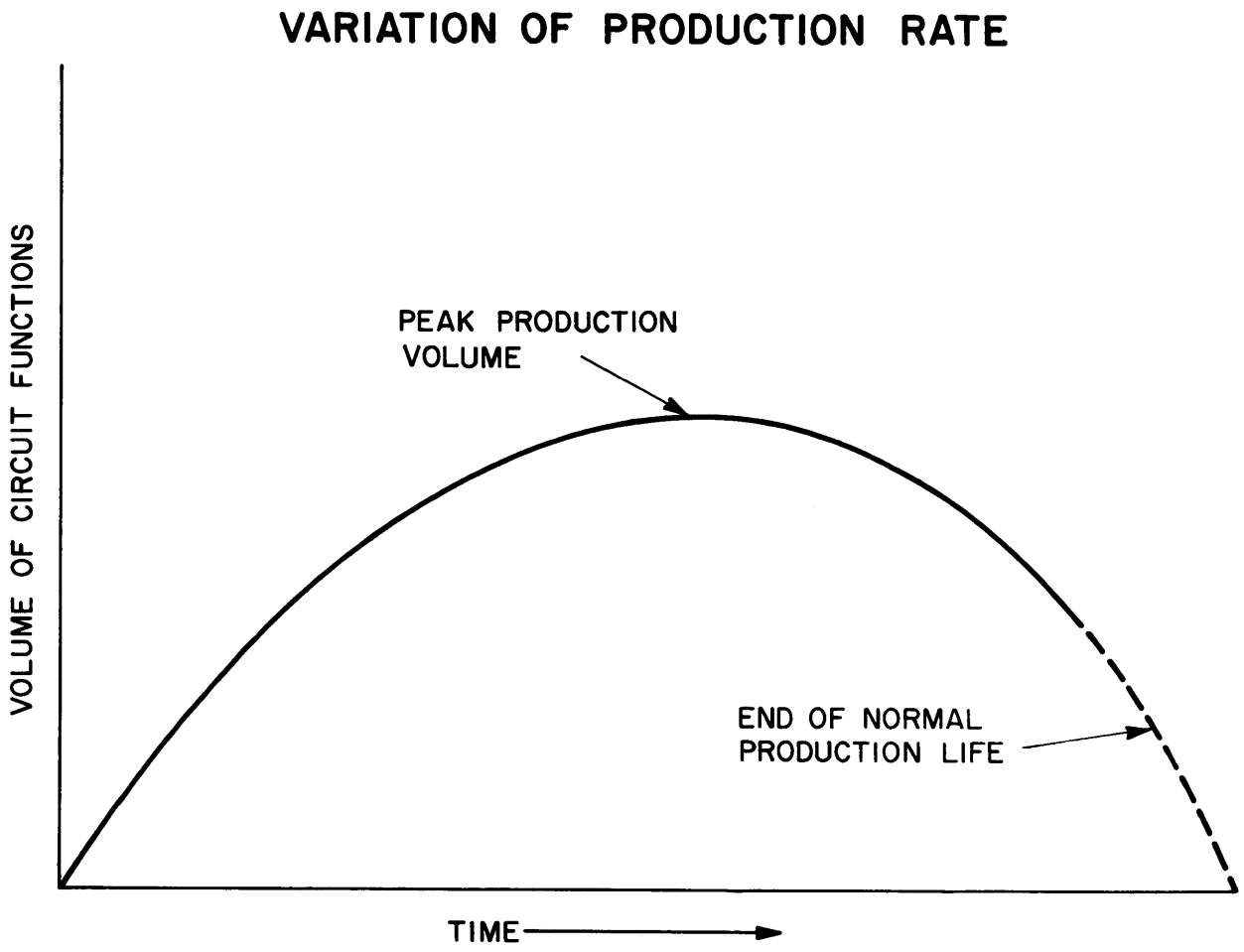

VARIATION OF PRODUCTION RATE
VOLUME OF CIRCUIT FUNCTIONS
PEAK PRODUCTION VOLUME
END OF NORMAL PRODUCTION LIFE
TIME

Figure 3-3

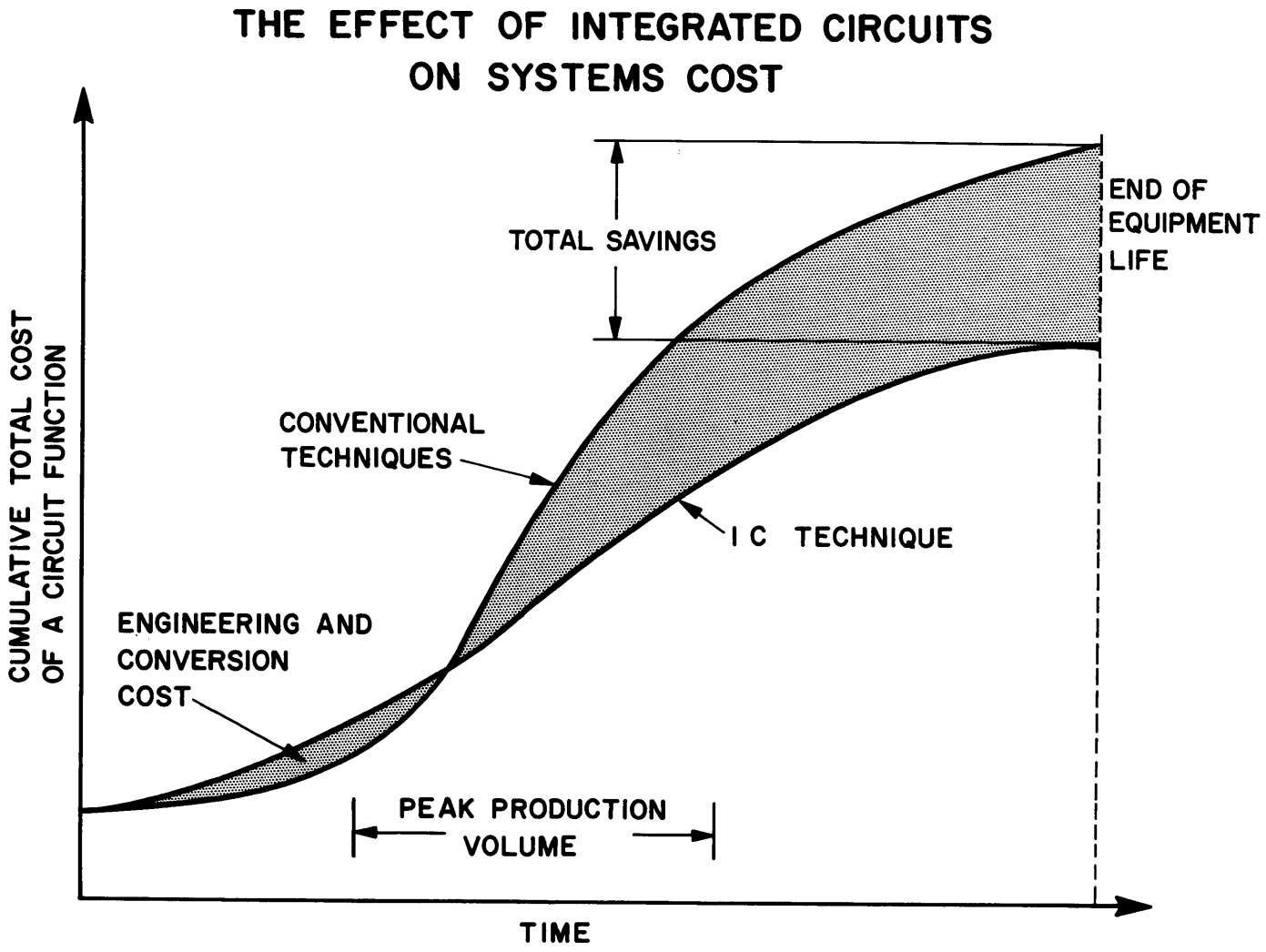

THE EFFECT OF INTEGRATED CIRCUITS
ON SYSTEMS COST
CUMULATIVE TOTAL COST
OF A CIRCUIT FUNCTION
TOTAL SAVINGS
END OF
EQUIPMENT
LIFE
CONVENTIONAL
TECHNIQUES
I C TECHNIQUE
ENGINEERING AND
CONVERSION
COST
PEAK PRODUCTION
VOLUME
TIME

Figure 3-4

3.3 (Continued)

R&D Overhead Procurement

The research and development costs for developing integrated circuit equipment, if substantially different, must be considered as part of the total systems cost. Other overhead costs include procurement with its associated paper work, vendor qualification and expediting. In these areas, integrated circuits offer substantial cost savings because of the smaller number of suppliers required for implementation of a given system. The quality assurance function also is included in this area.

Reliability

Some of the more intangible systems costs which are difficult to measure accurately are the service and warranty costs. These relate to customer satisfaction since he frequently must pay the out-of-service and equipment failure cost. Direct sales and marketing expenses can usually be determined. The value of market image must be balanced against the cost of retraining and obtaining market acceptance of a new product. Integrated circuit equipment has now been available long enough so that many of the pioneering problems have been dissipated. It is now becoming increasingly difficult to obtain older types of equipment since their integrated circuit replacements are becoming more widely available.

System Comparison Between Discrete Components and Integrated Circuits

The total cost differential of purchased components, between discrete and integrated circuits, should not be compared directly. In discrete form, adding to the basic parts cost are the cost of assembly (including parts shrinkage), additional inspection and capital requirements to support the greater amount of assembly. Reduction in direct labor and testing cost should be about 75% (in a typical system). Table 3-5 tabulates a comparison between integrated and discrete implementation of a specific system. Assembly labor and test are about 25% of the total direct system costs. Thus, 0.75 times 0.25, or about 20% should be added to discrete component cost to make equivalent microcircuit price comparison.

Trend Toward Complexity

The relationship of yield to silicon die area has been shown previously. A multifunction (two flip-flops or four to six gates per package) approach has had a pronounced effect on total system cost. The loss in yield is becoming smaller compared with the saving in packaging and assembly costs. The pricing of many manufacturers shows a definite saving on multifunction packages. Typically, the price of a dual-gate package is substantially less than twice that of a single gate. Figure 3-6 charts the trend toward greater complexity per package, whereas the most favorable costs resulted from 10 to 20 components in a single package in 1960 and 1962 respectively. The number is about 200 in 1966.

Figure 3-7 indicates how both process improvements and more complexity per package are both driving the production costs of complex integrated circuits downward.

3.3.1 Servicing Cost of Completed Equipment

The cost of servicing electronic equipment is directly associated with the total cost of ownership and factored into leasing charges. The integrated circuit package can be made directly replaceable in most systems assemblies now being used for commercial equipment. The inclusion of a number of packages in a module or subassembly is gaining in popularity. Modular construction tends to minimize the repair time, but only at the expense of more costly replacement parts. Isolating failures and their causes is generally easier with integrated circuits. Making equipment repairs usually requires package or modular replacement because integrated circuit repairing demands skills and equipment not found in the field.

Out-of-Service Cost

The electronics equipment user is greatly concerned with operating and down-time costs as it affects his business. The problem of

INTEGRATED CIRCUITS vs DISCRETE SYSTEMS

*COST COMPARISON

STANDARD TRANSISTOR CIRCUITS

COMPONENT	QUANTITY	UNIT COST	TOTAL COST
DIODES	1512	$ 0.25	$ 378.00
TRANSISTORS	336	1.05	352.80
CAPACITORS	420	0.05	21.00
RESISTORS	1428	0.044	62.83
PRINTED CIRCUIT BOARDS	28	5.00	140.00
CONNECTORS AND HARDWARE	29	2.75	79.75
DRIVER CARD	1	16.68	16.68
		SUBTOTAL	1051.06
LABOR			
ASSEMBLY			87.00
BACK PANEL WIRING			149.40
TESTING			43.50
		SUBTOTAL	279.90
		TOTAL	$1330.96

INDUSTRIAL INTEGRATED CIRCUITS

COMPONENT	QUANTITY	UNIT COST	TOTAL COST
DUAL INPUT NOR	84	$ 2.65	$ 222.60
DUAL 3-INPUT NOR	42	3.20	134.40
J-K FLIP-FLOP	42	6.35	266.70
BUFFER	14	2.55	35.70
PRINTED CIRCUIT BOARD	7	10.00	70.00
CONNECTORS	7	2.75	19.25
		SUBTOTAL	748.65
LABOR			
ASSEMBLY			21.00
BACK PANEL WIRING			29.40
TESTING			10.50
		SUBTOTAL	60.90
		TOTAL	$ 809.55

*FROM EDN - J. ROSE

Table 3-5

THE ECONOMICS OF INTEGRATED CIRCUIT COMPLEXITY

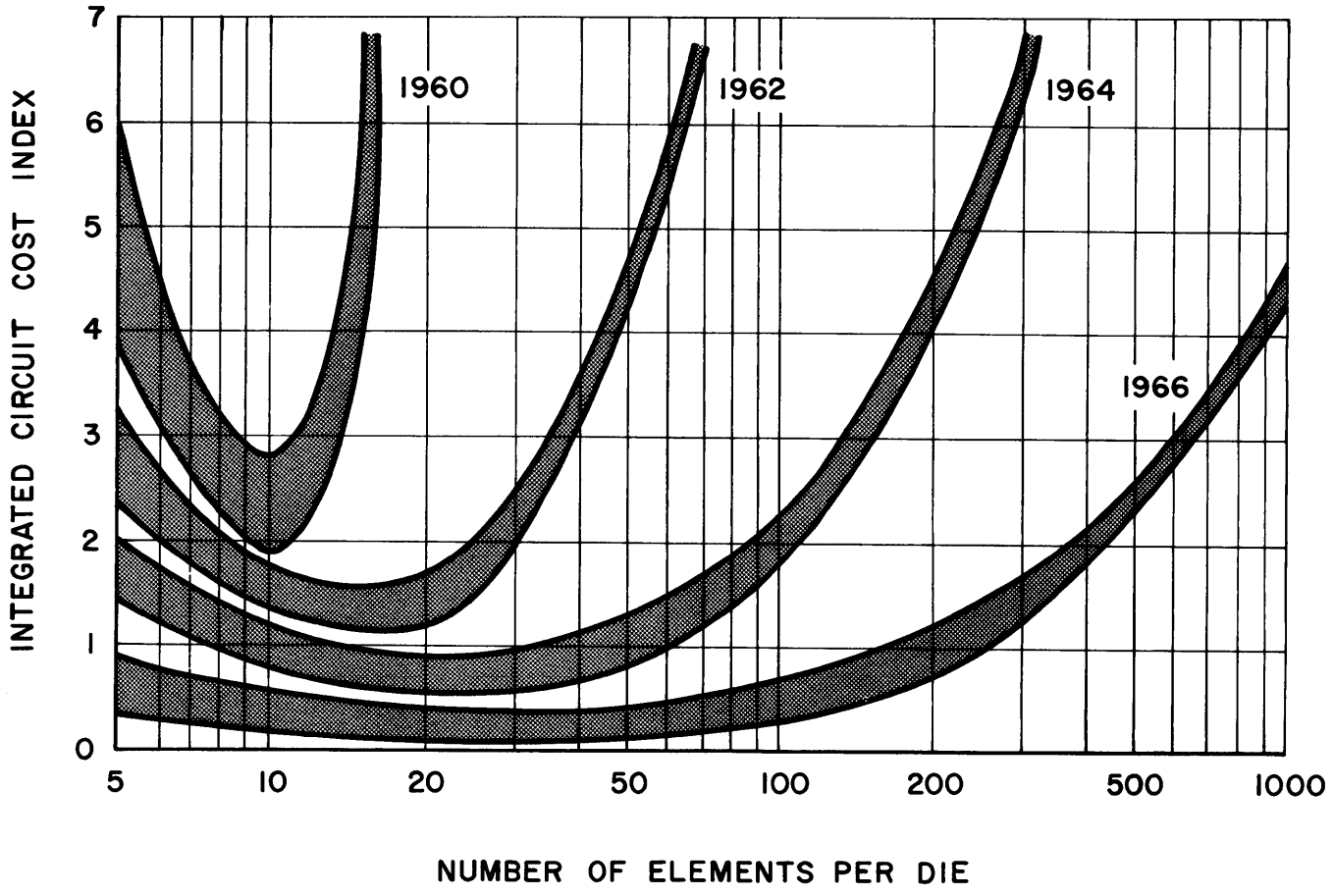


Figure 3-6

COST REDUCTION DUE TO IMPROVED PROCESSING AND NCREASED COMPLEXITY

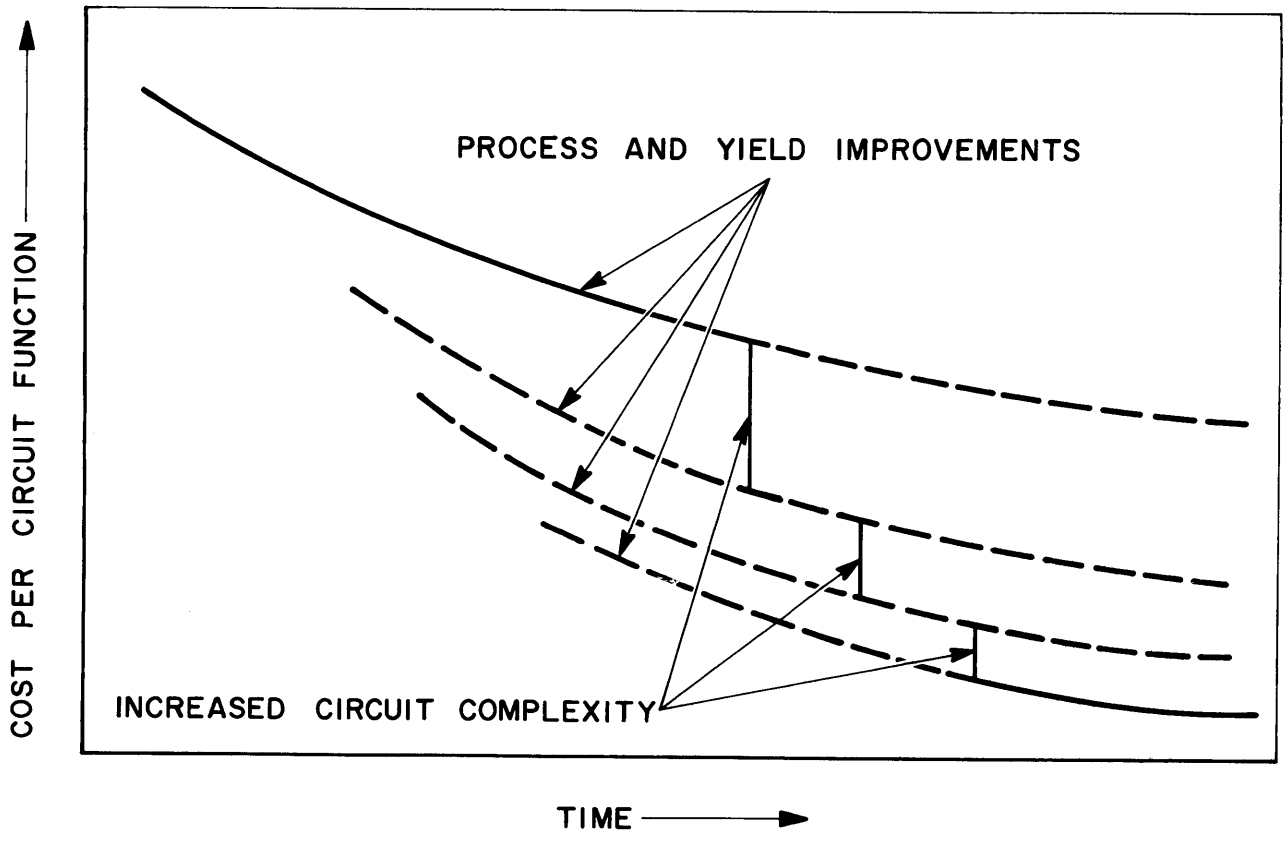


Figure 3-7

3.3.1 (Continued)

equating missile accuracy or human life to a specific dollar value is unsolvable. In comparison, the unavailability of a jet airliner or taxicab, because of communications failure, is equatable in terms of "dollars per hour". Rental of large computer systems places a large premium price on having every circuit functional for a high percentage of the time.

Assembly Costs

Assembly of systems employing integrated circuits generally requires a smaller number of more costly piece parts. Major savings accrue from the reduced amount of labor required. Care must, however, be exercised to avoid offsetting this gain by parts loss or breakage. The smaller overall size permits closer spacing, smaller cabinets and generally facilitates the use of more economical assembly parts and techniques. The use of miniature connectors and sockets to accomodate the numerous small pins are an exception. New techniques, such as multiconnector wires embedded in plastic, are being developed to further reduce microelectronic assembly costs.

3.4 Assembly Problems

The small package sizes and the desire for compact systems assemblies have generated numerous new problems. Some of these are readily solvable while others require considerable ingenuity. New techniques are being developed specifically to attain the advantages inherent with integrated circuit construction.

3.4.1 Mounting Integrated Circuit Packages

Circuit Boards

The single or double layer printed circuit (PC) board, fabricated by wave soldering techniques, has become reliable as well as economical for conventional component assembly. Unless the highest possible packaging density is required, PC's are also suggested for integrated circuit assembly. An advantage of this technique is that the tooling necessary to handle this form of circuit board is readily available. The limitations of present printed circuit board manufacturing techniques with the respect to spacing, art work, etc. are shown in Figure 3-8. The increasing use of integrated circuits will encourage more wide attainment of existing capability and continued effort to improve thereon.

Modified TO-5

One of the earliest and most popular integrated circuit packages is the modified TO-5 shown in Figure 3-9. This type of package configuration is in high volume production for use with transistors. It has been modified for integrated circuit use by the addition of a larger number of leads. Many standard components are made with a form factor which allows them to be packaged together with the multilead TO-5 package. All standard transistors, potentiometers, capacitors, small inductors and many other circuit items thus become immediately available for the integrated circuit system.

"Flat-Pack"

The flat package for integrated circuits is shown in Figure 3-10. This type of package although more expensive, permits higher packaging densities. As the volume use of the "flat-pack" increases, its price will undoubtedly be reduced, approaching that of the TO-5. Another package which may become an industry standard is the one developed for the IBM 360 (Figure 3-11).

External Components

An increasing variety of components capable of being included inside any of these small packages are becoming available. Their popularity is based on the space saving opportunities they offer. Table 3-12 summarizes the space requirements in mounting the various integrated circuit packages.

The individual circuit packages may be soldered or welded in place. Deciding between the use of welding versus soldering or the possibility of wire wrap involves several factors. Recent studies show that all three of these methods are quite reliable if properly done.

PRINTED CIRCUIT TOLERANCES OF LAND SEPARATION AND WIDTHS

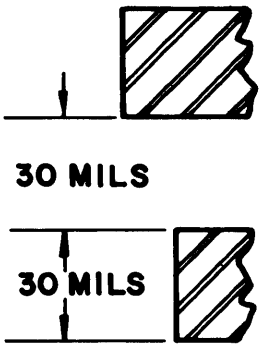
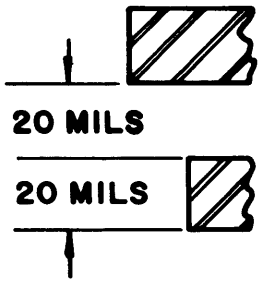
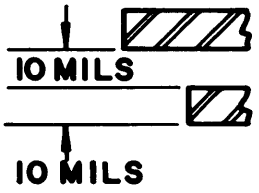
TITLE	GENERAL COMMERCIAL	AVAILABLE	CAPABILITY
			
RATIO OF ARTWORK TO FINAL PRODUCT	2:1	4:1	10:1
DISTANCE BETWEEN CENTERS	75 MILS	50 MILS	50 MILS
MINIMUM PAD DIAMETER	40 MILS	30 MILS	20 MILS

Figure 3-8

MODIFIED TO-5 PACKAGE

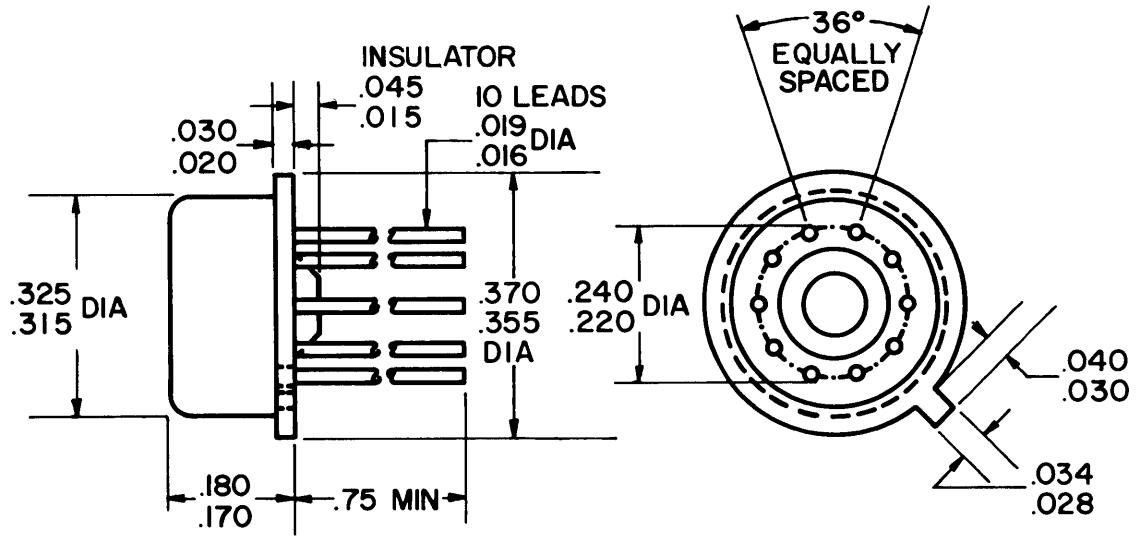


Figure 3-9

FLAT-PACK

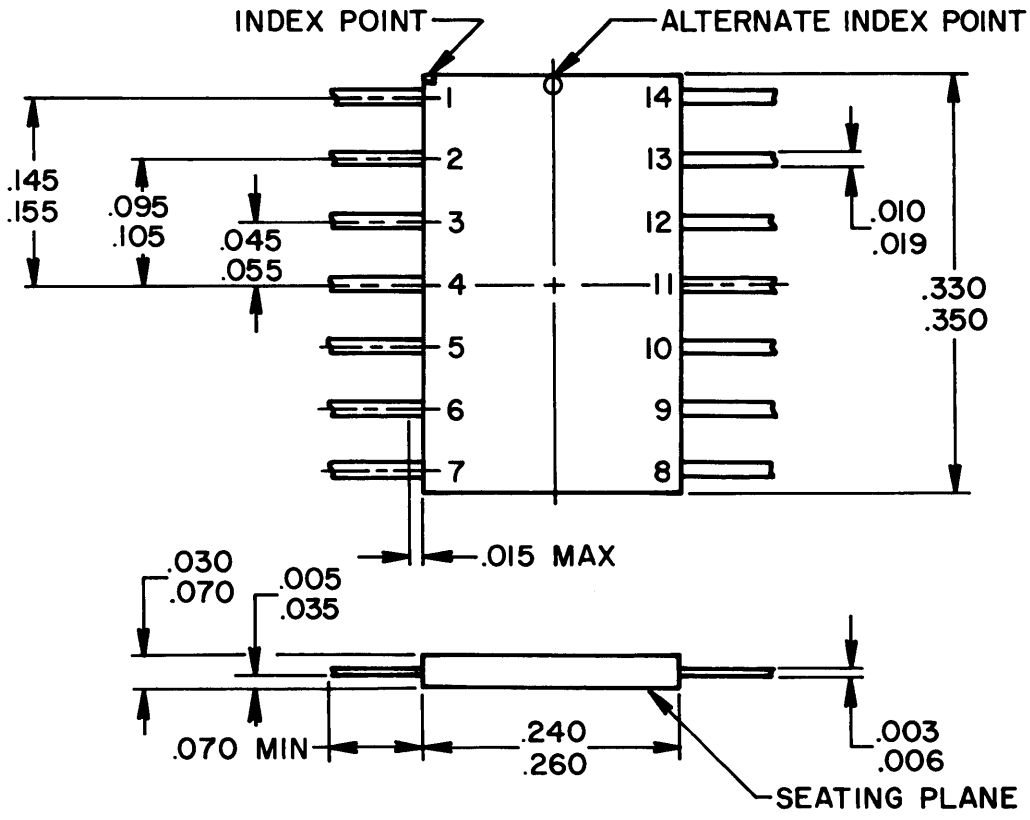


Figure 3-10

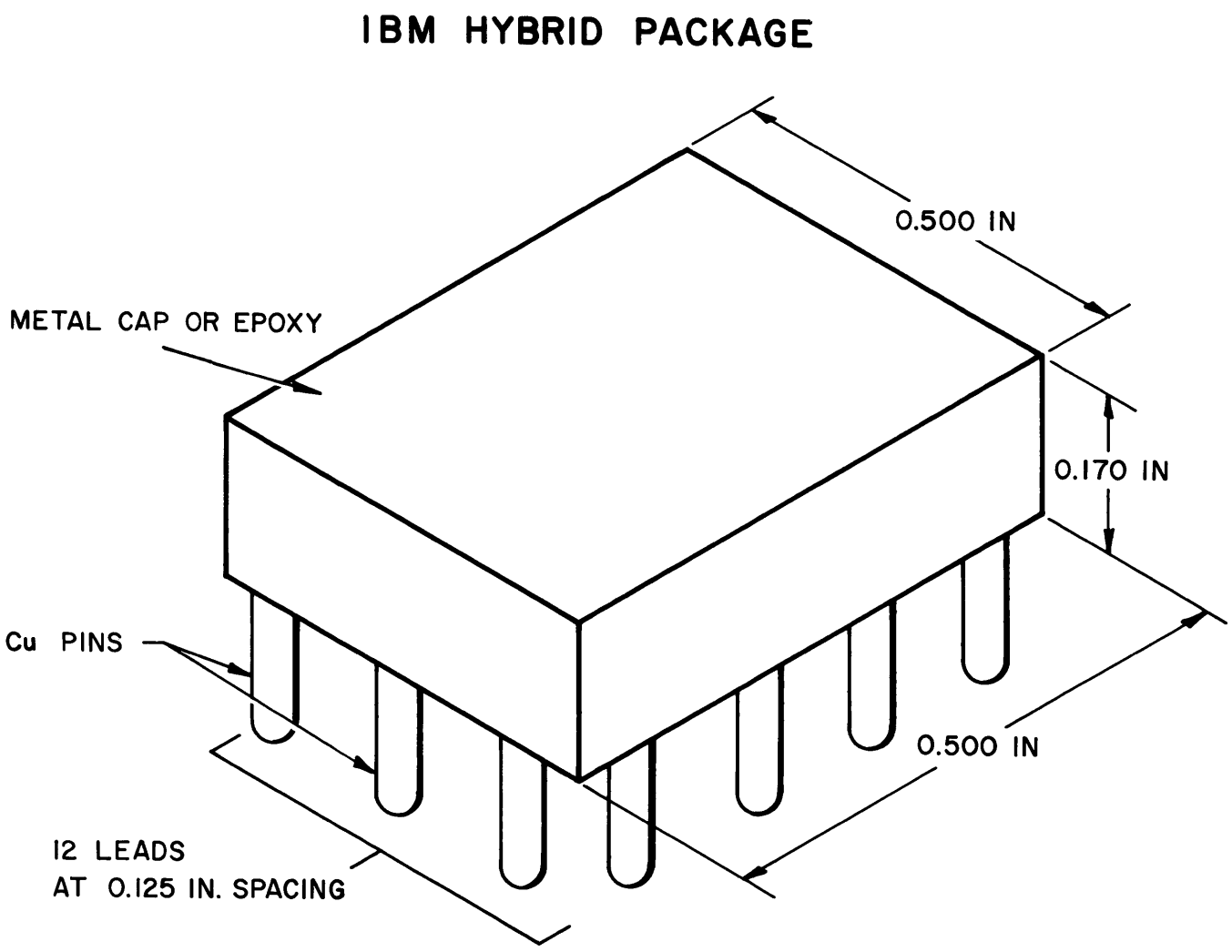

IBM HYBRID PACKAGE
0.500 IN
METAL CAP OR EPOXY
0.170 IN
Cu PINS
0.500 IN
12 LEADS
AT 0.125 IN. SPACING

Figure 3-11

COMPARISON OF SPACE REQUIREMENTS FOR VARIOUS PACKAGES

PACKAGE	MOUNTING	TOTAL * HEIGHT (IN.)	BOARD AREA ($IN.^2$)	TOTAL VOLUME ($IN.^3$)	NOTES
TO-5 (0.260 CAP)	PLUG-IN	0.345	0.16	0.055	
TO-5 (0.160 CAP)	PLUG-IN	0.245	0.16	0.039	
FLAT PACK 1/4 X 1/4	PLUG-IN	0.145	0.12	0.017	LEAD BENDING CAN EFFECT RELIABILITY
FLAT PACK 1/4 X 1/4	TOP MOUNTED	0.135	0.14	0.019	
INTELLUX HYBRID	PLUG-IN	0.370	0.19	0.070	
IBM HYBRID	PLUG-IN	0.250	0.30	0.075	LANDS MAY RUN BETWEEN PADS

*INCLUDES 0.075 P.C. BOARD

Table 3-12

3.4.1 (Continued)

Welding and Soldering

The flat-pack is more amenable to welding technology because of its flat ribbon lead and the ease with which welding heads can be positioned on the fifty mil spacing centers normally used. Wire wrap technology does not lend itself to integrated circuit systems because of the long leads normally required. The fragile foil leads of flat packages require careful handling. "Series gap welding" (Figure 3-13) has been developed for assembling flat-packs in high density electronic equipment. Laser beam welders are also used for this purpose. Figure 3-14 shows the plug-in solder mounting technique used with the modified TO-5 packages.

3.4.2 Connectors

The interconnection problem with integrated circuit assemblies is more acute than with conventional systems packaging. Their extremely small size, higher system reliability requirements and the desire to maintain economic advantages of integrated circuits place severe restrictions on microminiature connectors. An assembly of several integrated circuits may constitute a disposable package. Connectors printed or built on the edge of the PC board have been a partial answer. The printed circuit board with its associated connectors is a logical system building block.

The industry standard grid spacing of 0.100 inch has already changed to 0.050 inch to better accomodate integrated circuits.

All integrated circuit manufacturers supply leads which are both weldable and solderable. Gold-plated Kovar lead material has been satisfying both needs.

3.4.3 Multilayer Printed Circuit Boards

The high packaging densities possible with integrated circuits can often be solved using conventional two-sided printed circuit boards. Providing for the highest possible package density demands minimum spacing so that insufficient space is available on the normal printed circuit board for crossovers and interconnections. Multilayer printed circuit boards can satisfy these needs and provide additional volume advantages. Several methods used to connect the various layers of such boards are shown in Figure 3-15. By means of detents, the integrated circuit packages can actually be assembled within the structure. By using a sandwich of two double-sided printed circuit boards, an effective four layer system can be devised. Separate metalizations for the interconnections, signal lead, ground plane and the power supply distribution can be used to minimize noise in computer systems. It can also be used to facilitate the bypassing of individual circuit modules in systems.

3.5 Power Supply Considerations

The power supply requirements for integrated circuit systems are generally less demanding than those used for discrete circuit systems. It is easier to provide highly regulated current and voltage at the lower power levels required. Allowance must be made for variations in voltage between points in the system, particularly, if two or more power supplies are to be used. Supply voltage variation must also be limited. Most integrated circuits are specified with a range of allowable supply voltages. In most instances, these specifications refer to a single power supply. The power supply must provide the required voltage and have sufficient current carrying capacity for the entire system. The individual integrated circuits may be damaged more easily because of the low ratio of damaging current to normal current. This makes a large integrated system supply more difficult to fuse. The 0.001 inch wire, used to connect the silicon chip to the package leads, fuses rapidly at currents in excess of 300 mA. The use of zener diodes materially assists in obtaining voltage control for the system. Frequently, the needed zener diodes can be fabricated in the integrated circuit structures.

"SERIES GAP" WELDING

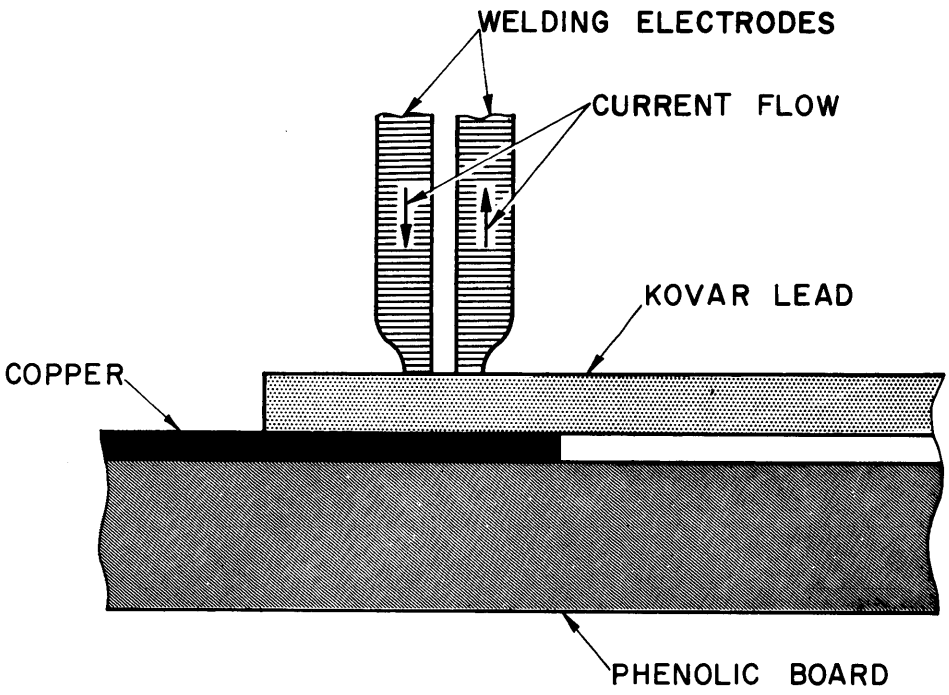


Figure 3-13

TO-5 PLUG-IN MOUNTING TECHNIQUE

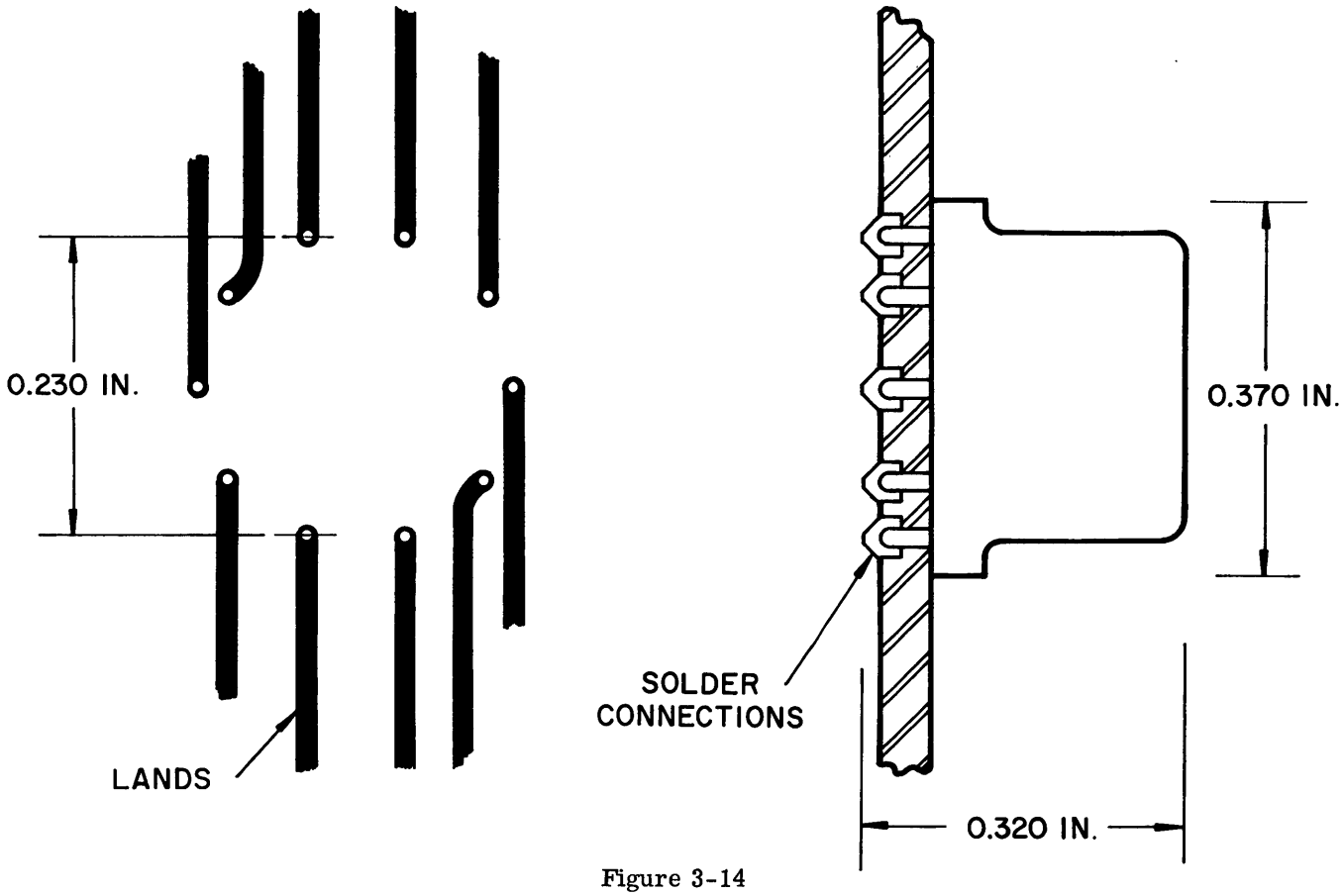


Figure 3-14

3.6 Size and Weight

The size and weight advantage of integrated circuits becomes appreciable for missile payloads. They are also important in aircraft and applications where portability is important (hearing aids, paging receivers, etc.). The approximate value of size and weight savings has been computed in Figure 3-16. Integrated circuits offer the possibility of large size and weight reduction as compared with conventionally fabricated discrete circuits. The small silicon circuit die size, typically, 0.050 by 0.050 by 0.005 = 0.0000125 cubic inches, may contain 10 to 200 components. To achieve the ultimate component density with such dice requires new ideas in packaging.

3.7 Thermal Considerations

Heat generation and dissipation becomes an extremely important design factor, particularly with high packing densities available with integrated circuits. Fortunately, miniaturization reduces the stray inductance and capacitance, thus permitting reduction in power level. Heat sinks may be incorporated with either multilayer or single layer circuit boards when used with either the flat-pack or TO-5 packages. Such thermal control elements as aluminum sheets or blocks may be incorporated as part of or between printed circuit boards. This becomes the thermal conductor needed to transfer the heat to the surrounding environment.

The maximum operating temperature of most available integrated circuit devices is 125°C. However, each circuit element should be operated at as low a temperature as possible to enhance reliability.

3.7.1 Thermal Calculation Problems

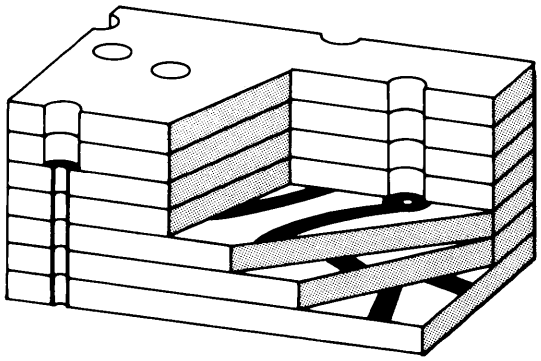
Calculations of thermal conditions are difficult to make because of the three dimensional structures involved and the wide variation in thermal conductivity of the materials used: e.g., air, 0.025 W/m-°C, silicon 148 W/m-°C. Experience has shown that one watt per cubic inch is a practical maximum; thus, the maximum for each of 100 flat-packs in a one cubic inch module is 10 milliwatts. Additional heat sinks or cooling equipment for heat removal quickly offsets the microminaturization advantages.

3.8 Systems Specification and Design Considerations: Conclusions

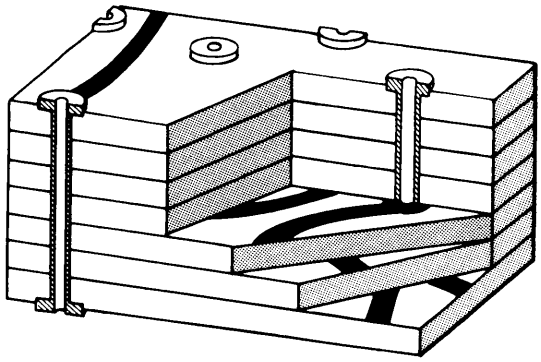
The following are presented as a summary of general systems specification and design considerations:

1. In most cases, it appears that no system specifications will need to be degraded to use integrated circuits
2. The most important requirement of any electronic system is that it perform correctly. Military reliability specifications are becoming more strict. Every effort continues to buy the most system with the least dollars
3. System size and weight may be established by the size and number of components employed. Their power dissipation may sharply limit the maximum packaging density
4. The high packaging densities available in microelectronics tends to reduce total stray inductance and capacity. However, the proximity of leads and the relatively fast switching speeds can induce objectionable coupling and circuit noise
5. The use of conductive ground planes for power distribution may be most useful. This is especially true in a multilayer, printed circuit board system
6. High frequency signal leads can be handled with "strip line" techniques over the useful range of present switching speeds and frequencies.

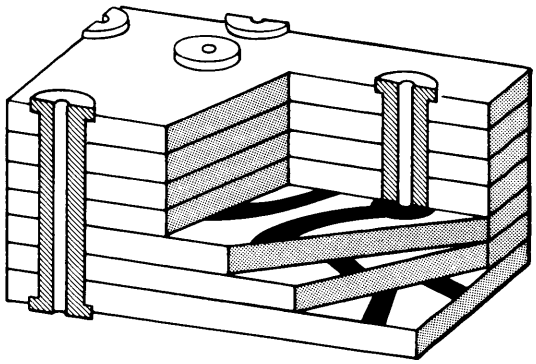
MULTILAYER WIRING PRINTED CIRCUIT



(A) UNPLATED CLEARANCE HOLES



(B) PLATED THROUGH-HOLES



(C) EYELETS THROUGH HOLES

Figure 3-15

VALUE OF WEIGHT SAVINGS

DEEP SPACE	$20,000/lb
NON-ORBIT	2,000/lb
PORTABLE	800/lb
AIRCRAFT	300/lb
VEHICULAR	7/lb
STATIONARY	0.05/lb

AN INTEGRATED CIRCUIT WEIGHS APPROX. 1gm (454 gm = 1lb).
(SOURCE – WALLMARK, 'MICROELECTRONICS'- McGRAW-HILL, 1963)

Figure 3-16

SECTION 4 INTEGRATED CIRCUIT FABRICATION HIGHLIGHTS

4.0 Introduction

To appreciate the performance capabilites and design contrasts involved with the use of integrated circuits, one should have an understanding of the fabrication techniques summarized in this section. Integrated circuits are produced in much the same manner as planar type transistors. The requirements for integrated circuits, however, are more exacting because selection and sorting is nearly impossible. To produce integrated circuits profitably, high production yields must be obtained. The earliest integrated circuits available five or six years ago were produced with very small yields (≈1%). Today, yields, in wafer form, of 60% are not uncommon. Further improvements in these yield figures are speeding the trend toward adoption of integrated circuits in place of discrete component circuits.

Yield

Batch

Integrated circuits are produced by a batch process. The individual wafer is the major increment of the batch. Figure 4-1 shows the effect of die size on the number of acceptable dice that may be obtained from a single wafer. Since many wafers can be processed simultaneously, large quantities of integrated circuits can be fabricated in a batch - and, as will be shown, they may include a number of different circuits. The economy of the batch process is the reason for the low cost of fabrication of silicon integrated circuits.

Packaging Advantages

The integrated circuit eliminates the excessive waste of packaging and structural support necessary when each individual component must be separately contained. The integrated circuit package, as each separate component package, must itself be structurally capable of withstanding the environmental conditions of use. In monolithic integrated circuits, the components are formed within a single substrate. In other types of integrated circuits, the components are packaged together in one container. In each instance, this minimizes the number of connections and eliminates many packaging supports.

4.1 Materials

Semiconductor

Semiconductor device technology depends upon solid state physics. The single crystal structure of materials of greatest interest are approximately midrange in resistivity between the conductors and the insulators. Hence, the name "semiconductor".

Single Crystal

Single crystal silicon, the most widely used semiconductor material, is used almost exclusively for monolithic integrated circuit structures. The development of dielectric isolation uses epitaxially deposited polycrystalline silicon to provide a substrate for supporting the integrated circuit. The electronic characteristics of such material can be made to afford unilateral current conduction. This is accomplished by introducing small, controlled amounts of impurities into specific regions. Proper positioning of these impurities within a piece of single crystalline semiconductor material makes possible the development of active devices, such as diodes and transistors. The transistor is the key component of integrated circuits. The same basic process may be employed to provide electrical isolation between components and to adjust the material resistivity for resistors and other passive components.

Silicon Purity

The silicon for integrated circuits is highly purified (about 1 impurity in 10^8), then grown into single crystals about 1 inch in diameter by 6 to 8 inches long. Wafers are then cut from the crystal and their surfaces lapped and polished. The wafers which constitute the starting material for integrated circuit processing are typically 6 to 8 mils thick with one mirror smooth surface.

Starting Wafer

4.1 (Continued)

The closeness with which the regions of controlled semiconductor material can be placed is the major determinant of the transistor's frequency and gain characteristics. In addition, the number of possible circuit elements per chip is related to this geometry control. Figure 4-2 reflects the increase in circuit complexity resulting from improved controls.

Substrate

The actual integrated circuit components are fabricated within a very shallow depth below the polished surface. For high frequency and high gain, the transistors' active regions are contained within a fraction of a mil of the wafer. The other components occupy even shallower depths. The remainder of the material, the substrate, is required to permit handling during production. If limited in thickness to that used to fabricate the circuit,it would be impossible to handle the material. Thermal requirements demand only that adequate provisions be made for removing the heat from the junctions.

4.2 Epitaxial Growth

The principle of epitaxial growth is depicted in Figure 4-3. It is a process by which crystalline material is grown on the surface of a suitable substrate. The most valuable application of this technique involves use of a single crystal silicon substrate upon which similarly oriented, higher resistivity silicon is epitaxially grown. The epitaxial growth procedure requires the introduction of a silicon gaseous compound ($SiCl_4$). This compound disassociates at high temperature leaving free silicon to deposit on the substrate. The silicon atoms will enter the crystal lattice in regular orientation if the temperature and growth rates are properly adjusted. In addition to the siliceous gas, other gases capable of imparting the impurities necessary to control the electronic characteristics are borne on a carrier gas into the system. Control of the rate of growth and orientation of the deposited material depends upon the temperature and rates of gas flow. The use of epitaxially grown semiconductor material permits improvement of certain integrated circuit characteristics. Epitaxial material is capable of being doped to provide junctions either at the growth interface or within the grown structure. The gaseous input flow must be regulated to contain the proper amounts of impurity materials.

Recent laboratory developments have demonstrated the ability to grow single crystal silicon epitaxially on materials other than single crystal silicon. These processes may eventually make possible the building of integrated circuits upon insulators to eliminate parasitics or metallic heat sinks to permit higher power operation without sacrifice of speed or gain.

4.3 Diffusion

The process of solid state diffusion is particularly useful in the formation of integrated circuits. Diffusion occurs increasingly rapidly as temperatures approach the melting point. Higher temperatures cause the crystal lattice to become more active and capable of absorbing foreign atoms into its structure. As used in integrated circuits, the solid material is single crystal silicon which is bombarded by impurities capable of producing the proper electronic characteristics. The impurities are mixed with a carrier to be absorbed into the silicon wafer surface in a diffusion chamber. Figure 4-4 shows some of the equipment necessary to perform these diffusions. To the right is the furnace or hot zone where the diffusion takes place. The gas flow equipment on the left is required to establish a clean ambient and conduct the dopants into the diffusion zone.

Diffusion System

Time and Temperature

The depth and extent of diffusion depends upon the time and temperature of the process. To cause the impurities to penetrate deeply into the material requires long periods of time and high

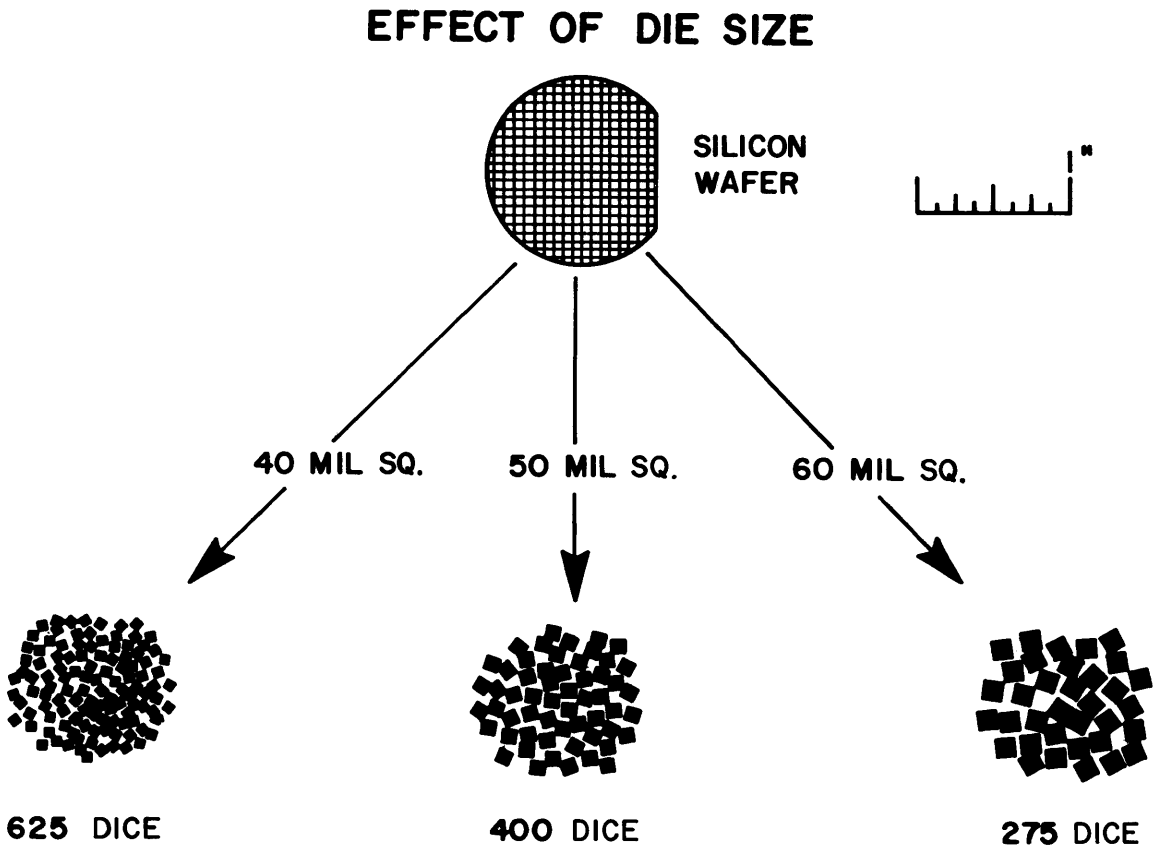


Figure 4-1

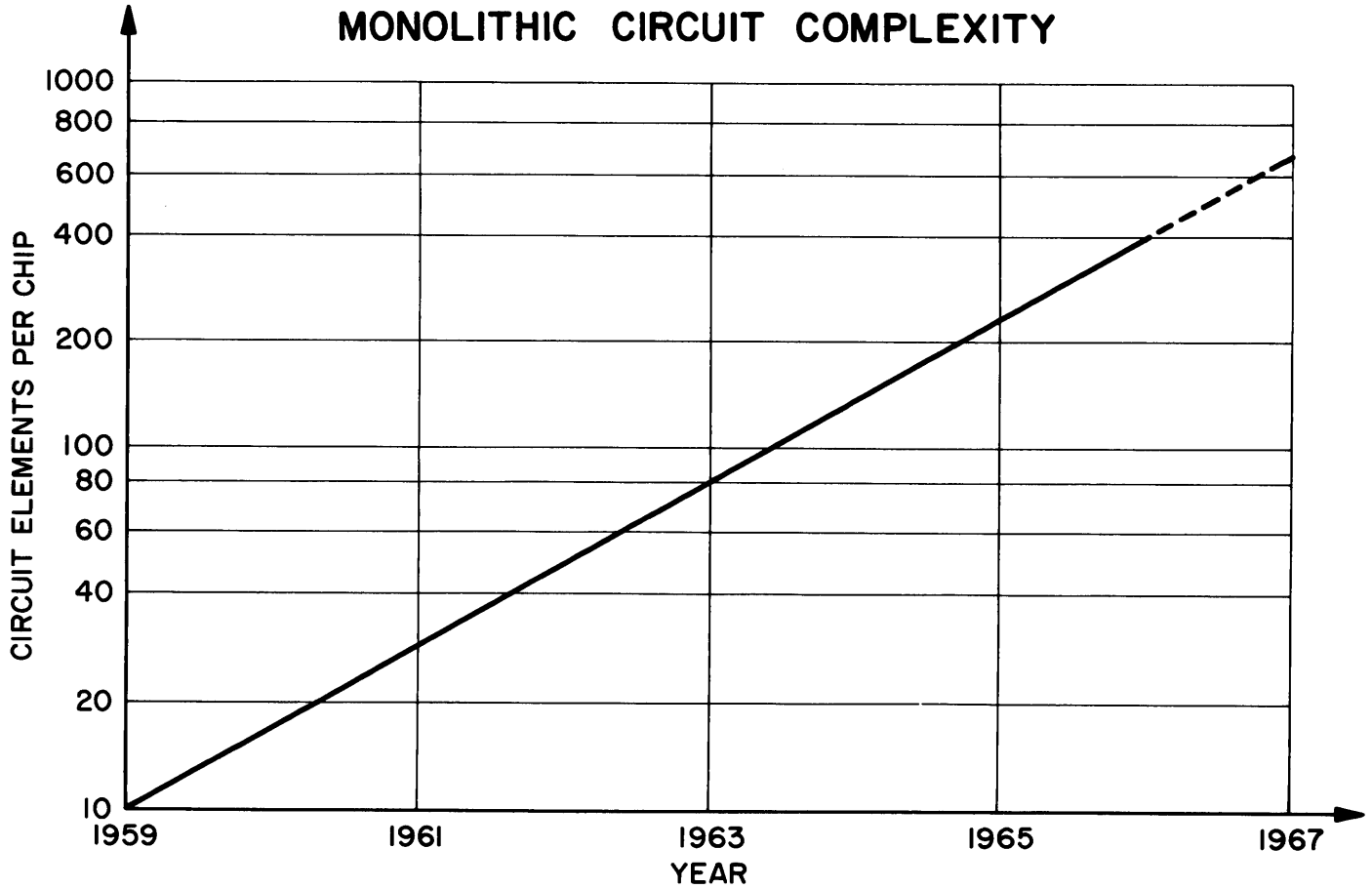


Figure 4-2

EPITAXIAL GROWTH

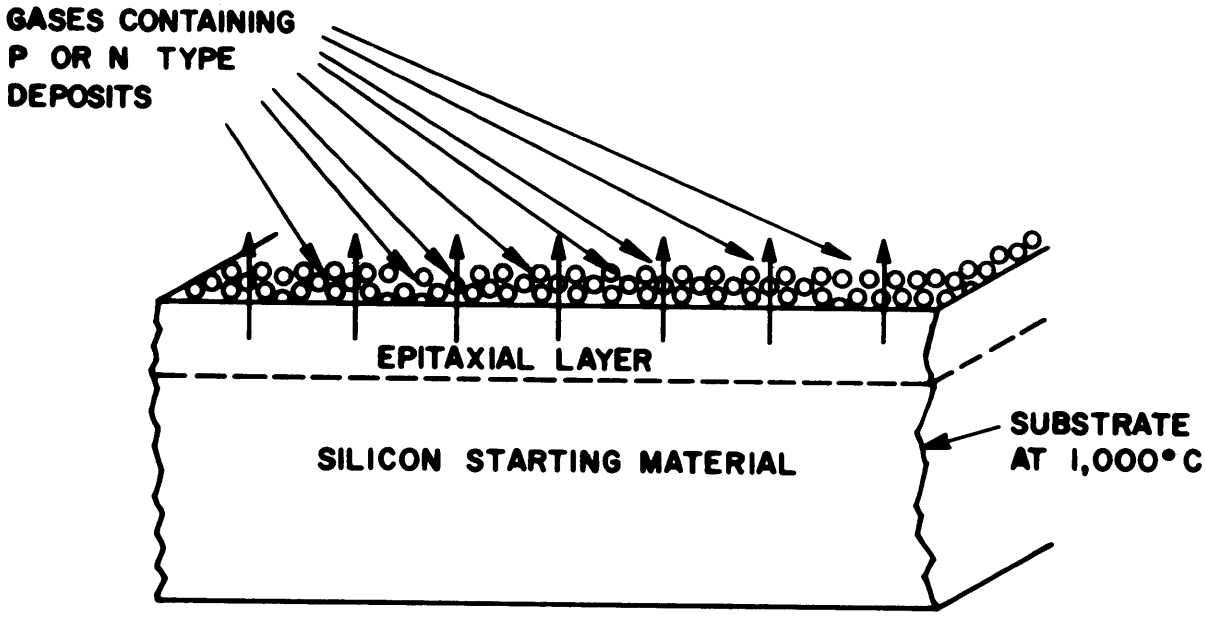


Figure 4-3

DIFFUSION SYSTEM

SHOWING FURNACE WITH PROFILE AND LIQUID DOPING SOURCE

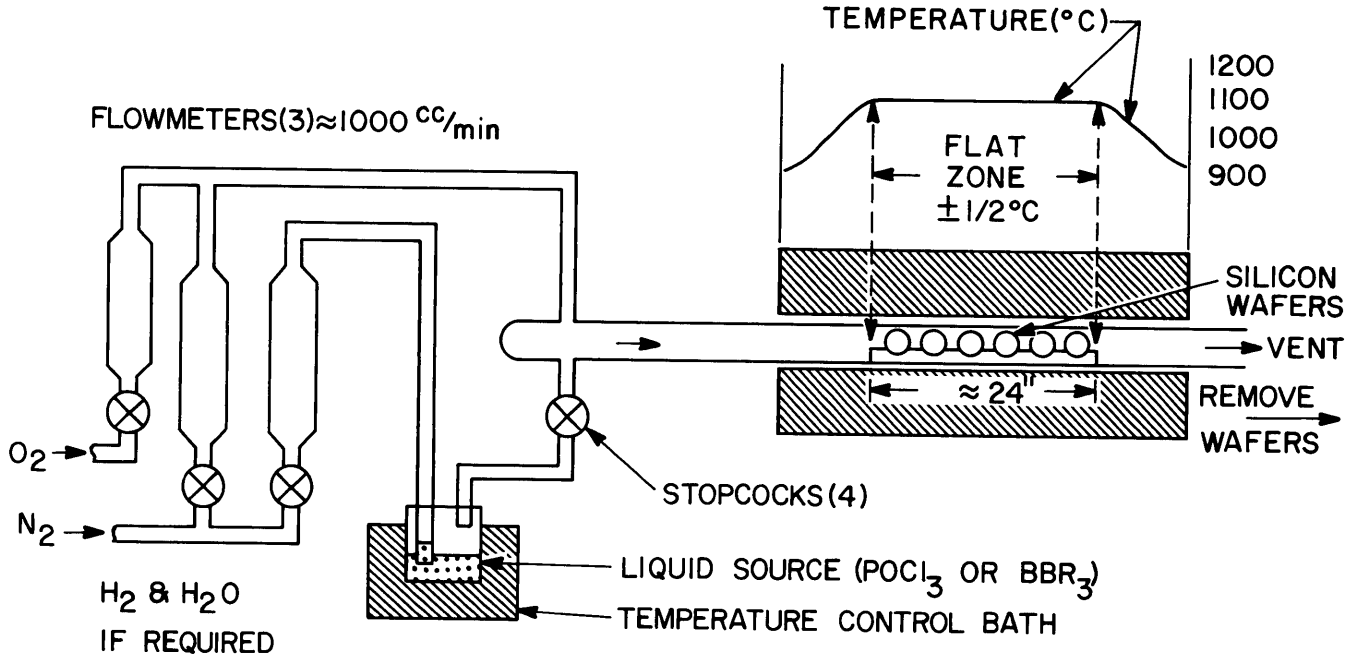


Figure 4-4

4.3 (Continued)

temperatures. Shallower diffusions may be accomplished more quickly at lower temperatures.

Diffused Junctions

The significance of the diffusion relates to formation of junctions and control of resistivity. Resistivity depends on the number of impurities among the semiconductor atoms, while junctions relate to the transition from P-to N-type. The P- or N-type characteristics relate to whether there is an excess of electrons or a shortage of electrons in the local lattice structure of the parent or substrate materials.

A junction will be formed where the number of P- and N-type impurities are equal if an excess of each type exists on either side. Boron and gallium diffusants are P-type dopants while arsenic, phosphorus and antimony produce an N-type characteristic.

The profile of the diffusion is dependent upon four factors; the diffusion time, the diffusant (impurity) used, diffusion temperature and the characteristic of the parent material into which the diffusion takes place. The characteristics of the parent material are important because, to form a junction by diffusion, it is necessary for the amount of diffusant to exceed the amount of impurity of the opposite type.

Single junction devices, useful for rectifiers and diodes, are somewhat simpler to fabricate than transistors, which rely on two proximate junctions. In each instance, however, careful control of the location and proximity of these junctions is required. In integrated circuits, this is accomplished by a series of different diffusions from one surface.

Isolation Diffusion

For integrated circuit fabrication, one of the first of the diffusion series is the isolation (or channel) diffusion. Its function is to isolate the various components from one another. Electrically, this is accomplished by reverse biasing each of the two junctions formed between components during the isolation diffusion.

Isolation generally requires a deep diffusion. Approximately one mil of penetration is required. The subsequent base and emitter diffusions are conducted at relatively lower temperatures. In contrast, the base diffusion reaches a depth of three or four microns, while the emitter diffusion is about two and one-half to three microns deep. The difference between the base and emitter diffusion depth is the base width, a most critical dimension in determining the transistor operation.

Base and Emitter Diffusions

In monolithic integrated circuits, the same diffusions used to form the base and emitter may be employed to fabricate resistors. The base diffusion forms moderately high resistances while the emitter diffusion more readily provides low values of resistors. Figure 4-5 illustrates a complete circuit composed of a capacitor, transistor and resistor formed primarily by diffusion. The regions are identifiable as follows:

1. P-type substrate - the starting wafer material

2. N-type collector material and all other material above the line of demarcation formed with the substrate is the epitaxially deposited layer

3. P-regions between components is epitaxial material converted to P-type by the isolation diffusion

4. P-regions of the transistor and resistor are regions of epitaxial areas converted to P-type by the base diffusion

4.3 (Continued)

5. N+ regions of the capacitor and transistor are formed during the emitter diffusion. The N+ in the capacitor forms the bottom plate, while the N+ in the N- collector region of the transistor is for making good contact. The N+ within the P-region of the transistor is the emitter itself, the P-base material having been reconverted to N+.

4.4 Photolithography

4.4.1 Principles of Photolithography as Applied to Integrated Circuits

Photolithographic techniques have been adapted to integrated circuit manufacturing. They are useful for the restriction of the various diffusions to defined areas. The actual restriction is accomplished by the masking effect of silicon oxide layers grown on the silicon surface. The oxide is first grown over the entire surface and then selectively removed from the areas where diffusion is desired. The oxide is permitted to remain in places where the diffusion is not desired. Photolithography is used to define and control the different areas as illustrated in Figure 4-6.

Each different diffusion process must be closely aligned with every other step in the process. Each integrated circuit on the wafer must maintain its individual resolution and alignment throughout each step in the entire process.

4.4.2 Geometry Control

The control of the geometry of each individual transistor in an integrated circuit has been a limiting factor in the performance of the resultant circuit.

The relationship between the surface geometry control and theoretical performance of a transistor is shown in Figure 4-7. The control of the surface geometry is largely dependent upon the ability to transfer a series of patterns from masks to the wafer surface. Highly refined photolithographic techniqes have been developed for this purpose.

4.4.3 Mask Making

When each unit on the wafer is identical, a single piece of art work may be photographed with a given reduction and repeated as many times as necessary to obtain the final pattern. The reduction employed in mask making permits the original image to be of a size in which standard drafting techniques may be employed. Thus, the master art work for photolithographic masks may be two to three hundred times as large as the final pattern on the wafer. The original art work, in addition to being reduced, is repeated iteratively.

4.4.4 The Photo Resist Process

In processing a wafer, it is first uniformly coated with a photo resist material that has a certain spectral light sensitivity. The photo resist material, spread over the wafer, closely resembles the undeveloped emulsion used in photography. The mask must be carefully aligned with the coated wafer to permit light to penetrate only in those places where it is desirable to have the photo resist film exposed. The pattern of each successive mask must be carefully aligned with that of its predecessors. After exposure, the photo resist is developed. This procedure removes the film from those areas which were unexposed, leaving the coating only where required as shown in Figure 4-6 (b).

4.4.5 Etching

The function of the developed photoresist is to protect the silicon oxide film on the substrate surface during etching. The exposed silicon oxide is dissolved when the entire wafer is immersed in an etching solution which is usually composed of some combination of hydrofluoric acid or fluoride compounds. The photo resist chemicals must be insoluble in the etch solution which, while

MONOLITHIC SILICON INTEGRATED CIRCUIT CONSTRUCTION

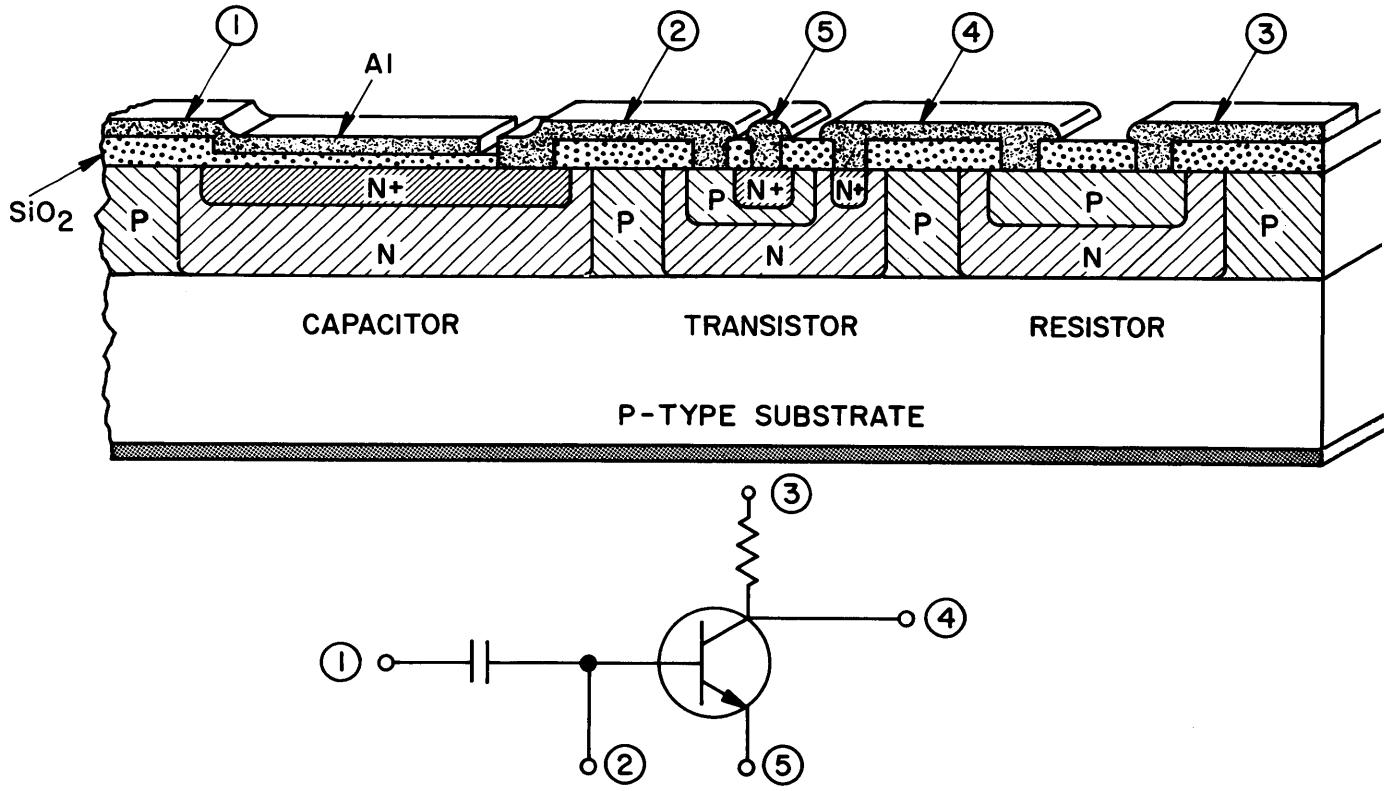


Figure 4-5

PHOTO RESIST OPERATION

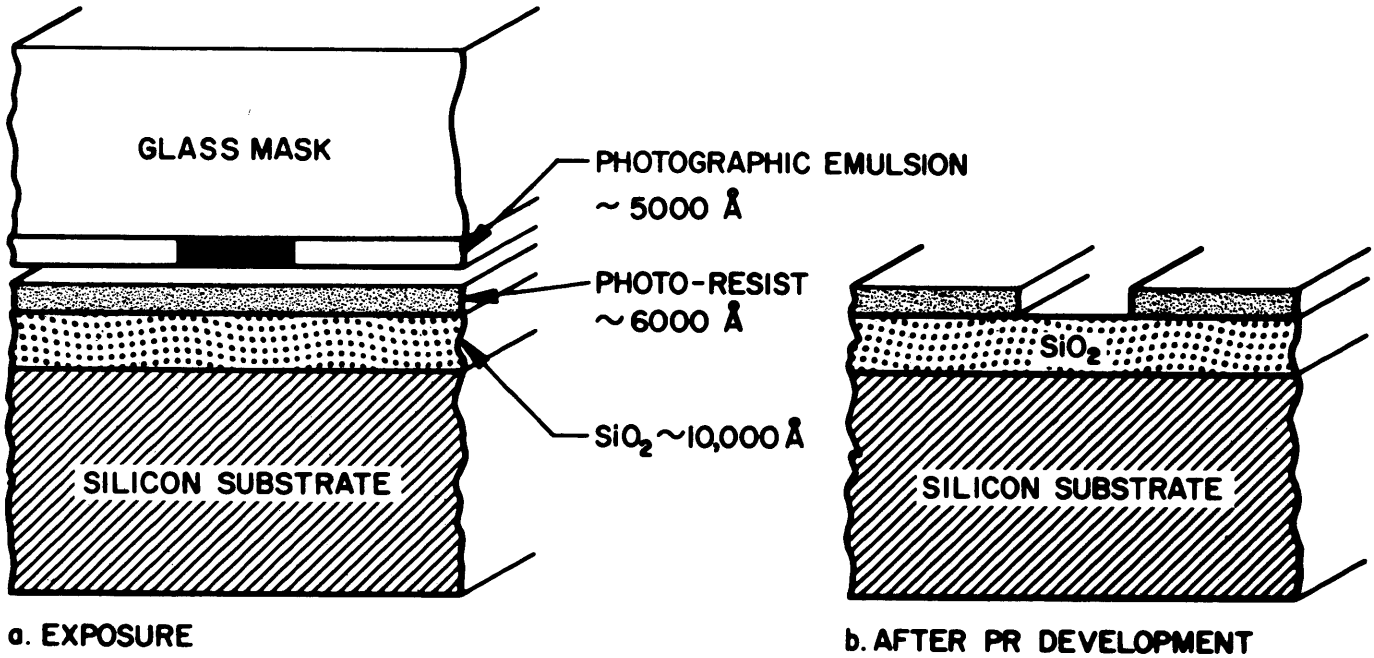


Figure 4-6

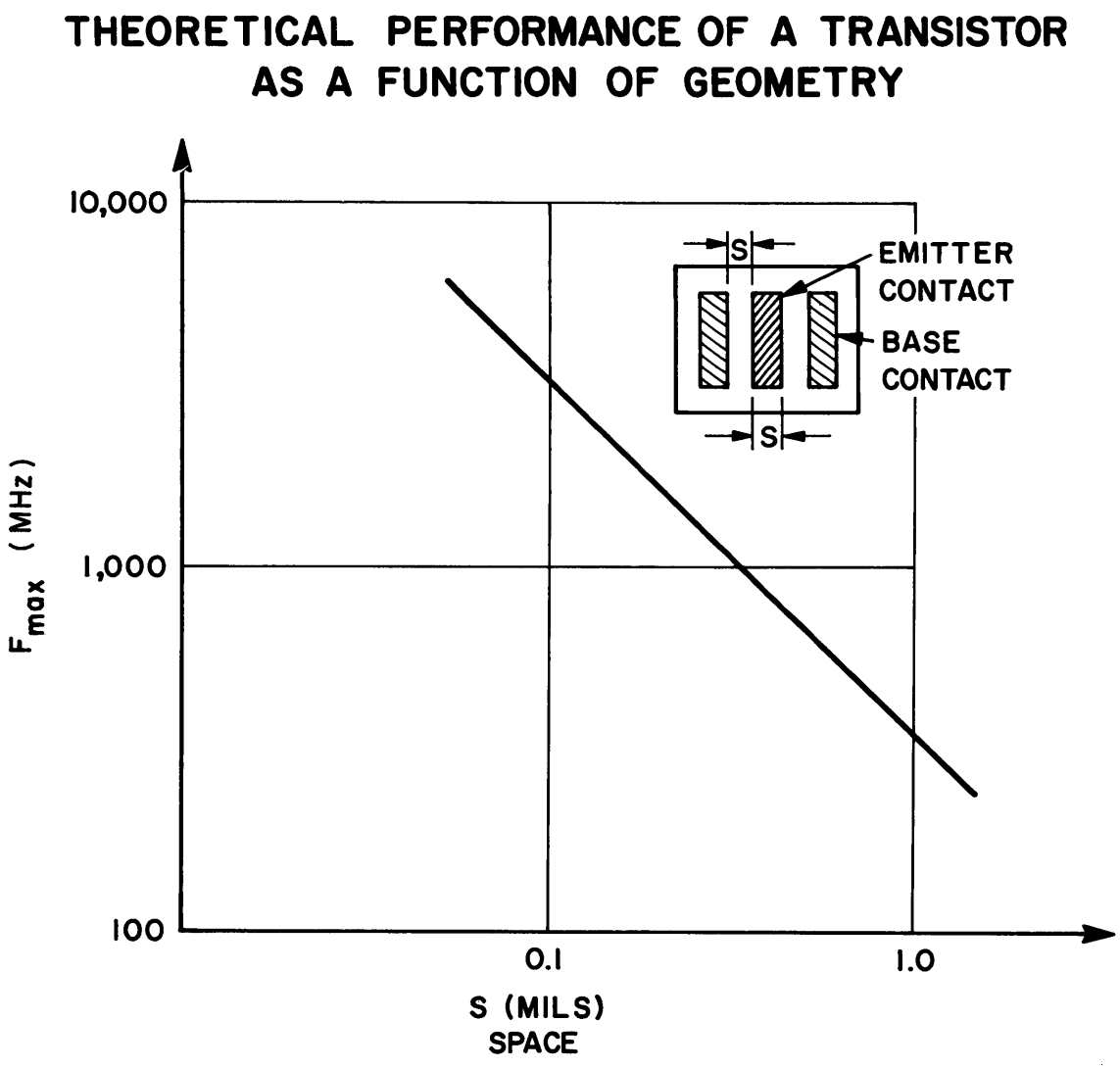

THEORETICAL PERFORMANCE OF A TRANSISTOR
AS A FUNCTION OF GEOMETRY
10,000
1,000
100
F_{max} (MHz)
0.1
1.0
S (MILS)
SPACE
S
S
EMITTER
CONTACT
BASE
CONTACT

Figure 4-7

4.4.5 (Continued)

attacking the oxide, must not react with the silicon itself. The oxide is thus removed only from the places where exposed to the etchant. After completing the etch, all photoresist is completely removed before proceeding. If the subsequent step is a diffusion, the oxide permitted to remain prevents the impurities from entering the silicon crystal structure.

Figure 4-8 shows the application of a minimum number of masks in a series to form a monolithic integrated structure. Whereas, in practice, each mask contains several hundred circuit patterns, only one is shown. It is shown large enough to indicate the appearance of a single pattern.

4.5 Thin Film Techniques

Thin films may be deposited either upon a passive substrate such as glass or ceramic or the surface of a monolithic silicon integrated circuit. Vacuum deposition or sputtering are the most commonly used methods of forming thin films. Vacuum deposition is widely used for gold and aluminum metalization and some metals useful for thin film resistors. Sputtering is used for depositing refractory metals and dielectric materials for thin film capacitors.

4.5.1 Thin Film Passive Components

Thin film techniques are capable of producing higher value resistors and capacitors within a given area. They are also capable of providing closer tolerance on the parameter values, and have less parasitic capacitance. Thin film resistors and capacitors generally have lower temperature coefficients than diffused components.

The thin film components are, however, much more expensive to fabricate on a monolithic structure because of the extra processing steps required. They also tend to be more expensive on passive substrates because of the additional expense of interconnecting the semiconductor active elements into the circuit. For some applications, the improved thin film component characteristics justify their higher processing cost because of the losses in yield accompanying such requirements on monolithic circuits.

4.5.2 Thin Film Active Devices

Active thin film devices have long been discussed and their principles are well understood. Commercial production of fully deposited devices, however, has not as yet been practical.

The field effect transistor (FET) and metal-oxide-silicon (MOST) devices are hybrid combinations of silicon diffusion techniques together with thin silicon oxide films and metalization. Recent developments indicate that these field effect devices are readily available in commercial quantities. Integrated circuits employing this type of active device are rapidly growing in popularity. The silicon diffusion employed to make the active devices is also used to form the resistors.

4.5.3 Thin Film Metalization

In a monolithic structure, many components may be fabricated in proximity to one another, isolated either by reverse bias junctions or dielectric materials. It is necessary to properly connect these elements within the circuit. One of the final steps in wafer processing is placing the interconnection pattern into position. These interconnections are accomplished by the vacuum deposition of a thin film of metal, usually aluminum or gold, over the entire surface. A photoresist-etch technique, similar to that employed to pattern silicon dioxide for controlled diffusions, is used.

Excess metal is thus removed from the surface of the integrated circuits while the metal interconnection pattern is permitted to remain. The interconnection patterns between components lie on the silicon oxide surface except where holes had been made to

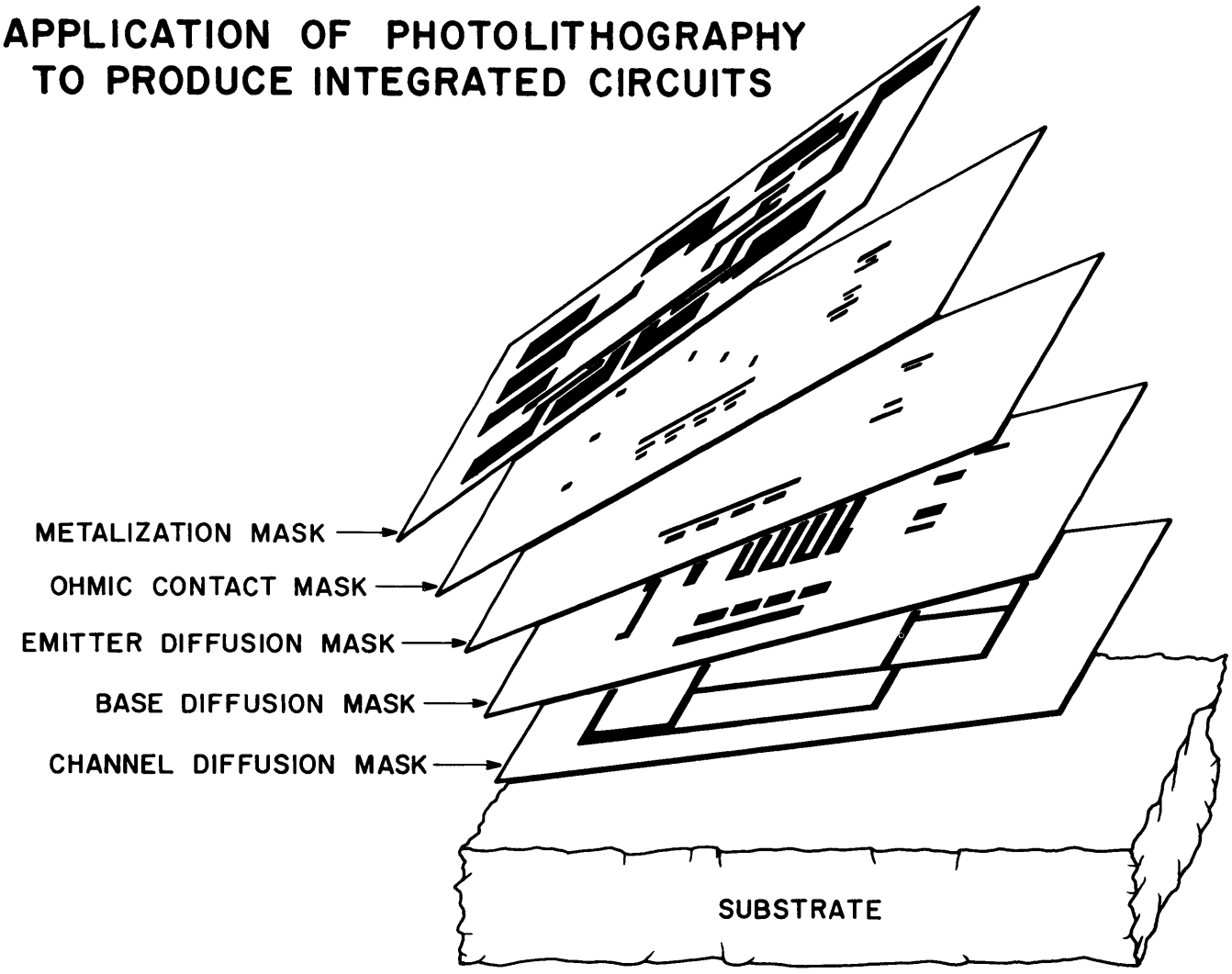

APPLICATION OF PHOTOLITHOGRAPHY
TO PRODUCE INTEGRATED CIRCUITS
METALIZATION MASK
OHMIC CONTACT MASK
EMITTER DIFFUSION MASK
BASE DIFFUSION MASK
CHANNEL DIFFUSION MASK
SUBSTRATE

Figure 4-8

4.5.3 (Continued) permit contact to the silicon. The oxide, as shown in Figure 4-5, thus prevents short circuiting.

4.6 Assembly

4.6.1 Dicing

After the wafer is fully processed, it is necessary to arrange the individual integrated circuits so as to facilitate their use in electronic systems. This usually requires the separation of the wafer into dice and placing each circuit into a package where its terminals must be connected to the package leads.

After testing the completed circuits, it is then necessary to divide the wafer into its individual dice or chips. The hard brittle nature of silicon makes it possible to break the wafer, relatively uniformly, along straight lines scribed on the surface. One mil blades are occasionally employed to divide the wafer into dice.

4.6.2 Die Bonding

Each die must be bonded to whatever package, header, or substrate is to be used. Bonding may be facilitated by gold plating the wafer and header so that solder may be used. High temperature solders are preferred. An alternate bonding method employs glass frit and is particularly useful for bonding to ceramic and glass substrates.

4.6.3 Wire Bonding

After bonding to the substrate, the necessary interconnections must be made between the die and package leads, or from one die to another die for hybrid assembly. Very small diameter gold or aluminum wires attached by thermal-compression bonding are most commonly used for this purpose. Bonding pad areas of metalization on the integrated circuit surface are designed to accept these connections. The pad sizes are typically two by three mils, which is large compared to many of the elements within the integrated circuit itself. Wire, from an extreme fineness of two-tenths mil to as large as five to seven mils, is used for making these connections. Figure 4-9 illustrates in cross section, a bonded circuit. The die bond and wire bonds to the circuit and package post are shown.

4.4.4 "Flip-Chip"

A method of mounting the integrated circuit bonding pads directly to interconnection metalization on the substrate is being developed. Called "Flip-Chip" mounting, the method eliminates the need for die bonding and bridging wires. The use of the "Flip-Chip" technique (Figure 4-10) may eliminate both the TO-5 and flat package from many future systems. This technique has been used in the IBM 360 computer system for transistor, diode and integrated circuit attachment. When all the interconnections have been completed, the package is sealed.

The first widely used package for integrated circuits was a modified TO-5. Whereas the TO-5 transistor header has only three leads - for integrated circuits 6, 8, 10, 12 and 14 lead packages are required. The TO-5 package has enjoyed wide popularity both for economic reasons and due to the wide availability of reliable equipment and techniques for using this package.

The newer flat package was designed primarily for integrated circuits. Its past economic disadvantage resulted from the use of TO-5 transistor packages in multimillion quantities whereas the demand for flat-packs has not been nearly that great. A number of other packages are being developed for integrated circuit use. Despite other possible advantages, the newer packages can be expected to reflect higher per unit cost because of lower production volumes and development costs.

SILICON MONOLITHIC ASSEMBLY

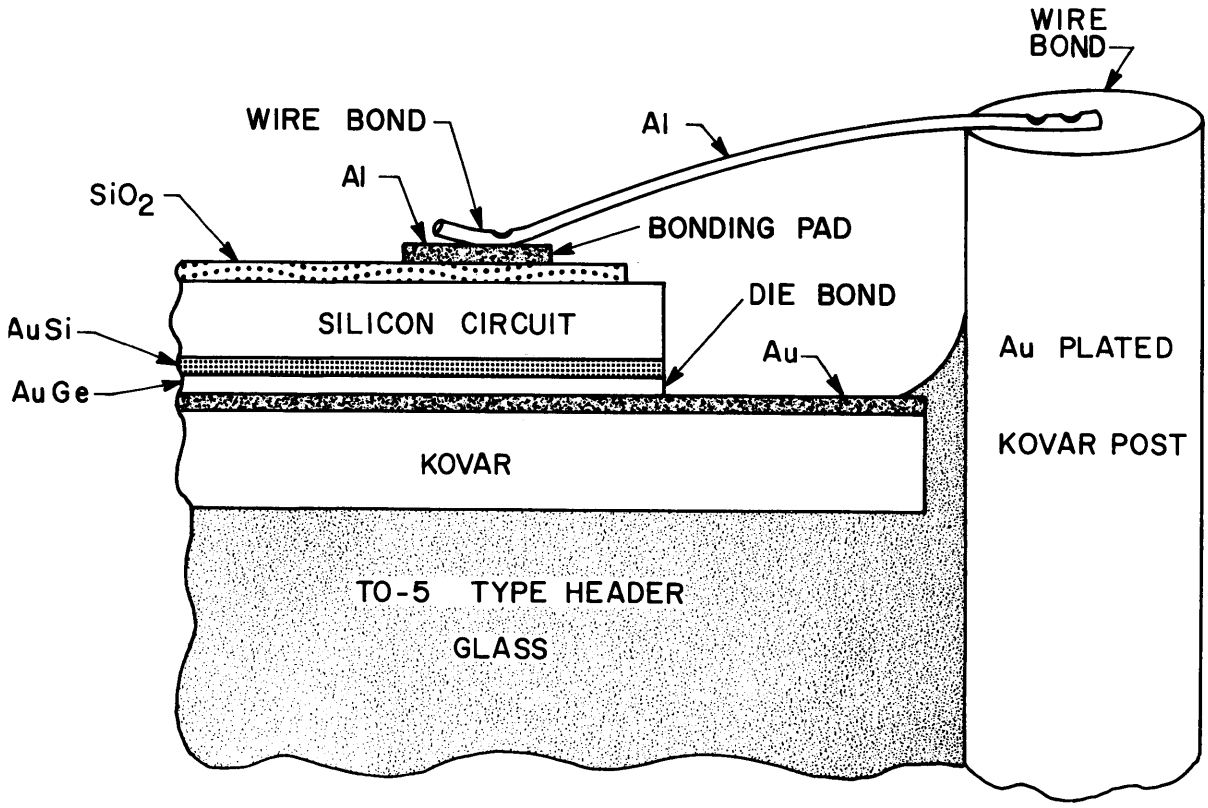


Figure 4-9

FLIP-CHIP SYSTEM ASSEMBLY TECHNIQUE

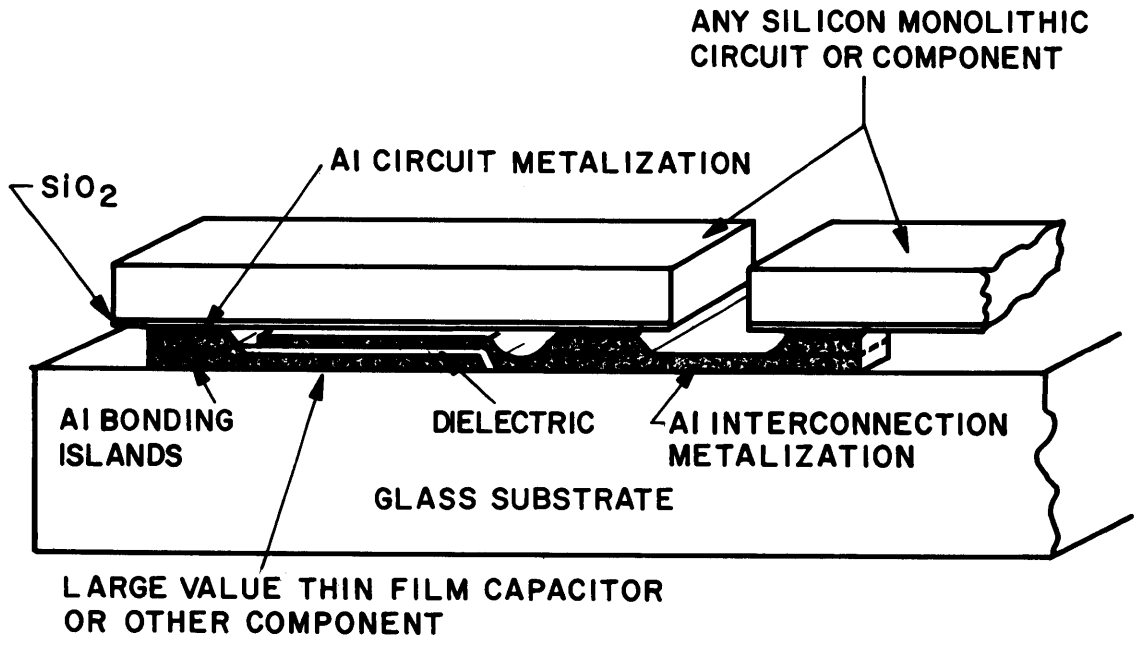


Figure 4-10

4.7 Probing or Quality Control

Dispersed throughout the process are numerous quality control tests and inspections. Visual inspections are made routinely as part of each process step. Electrical measurements via probing can only be accomplished when and where the silicon surface is exposed.

Electrical monitoring of the characteristics produced by various process steps poses unique problems in integrated circuits. The primary problems are mechanical, arising from the small dimensions of the parts that must be measured. A 40 mil square die may contain more than 20 individual components. Measurements made upon these components during processing must be made through the holes in the oxide developed by the etching process. Typically, these are 1/2 to 1 mil square. To fit easily into these openings, the probe points must taper to less than 1/2 mil diameter.

Probe Points

The probes are sharp needles, usually tungsten, fastened on a micromanipulator. Probe measurements are made during the process to monitor each diffusion.

Probing is also done on completed units in wafer form. A typical probe set-up is shown in Figure 4-11. Ten or more probes can be used on a die for functional positional testing before assembly. 100% probing is commonly done at this point to assure that only high quality units are assembled. Testing by probes usually must be restricted to low frequencies because of the long leads involved.

Yield is the measure of success or failure in the production of integrated circuits. To achieve high yields, close control, based upon probe information, must be maintained. Cleanliness is critical in most of the processes, hence marked emphasis must be placed in this area.

4.8 Testing the Completed Units

The advantage of probing is almost entirely restricted to the manufacturer. Even if equipped to make probe measurements, the user is unable to open the package without destroying the hermetic seal. He would also have extreme difficulty in replacing it as well as abrogating any supplier warranties. Hence, except for destructive evaluations, the user is forced to make measurements on the integrated circuit not as a discrete component, but rather a "black box". He can only make measurements between the external leads. If he understands how the integrated circuit has been fabricated, and has complete specifications knowledge, he may make meaningful measurements. This requires a degree of sophistication not previously required of the systems or circuit designer.

"Black Box"

Integrated circuits have necessitated "black box" specifications. Figure 4-12 shows the application of this type of testing in which output voltage is compared to input voltage. Those integrated circuits are accepted whose traces fall entirely within the shaded areas - the others are rejected. The Accept/Reject measurements which, while they indicate whether a circuit still operates properly under a given set of conditions, are not satisfactory for analytical evaluation. They are particularly limited in making reliability assurance determinations. For this reason, many users are adopting a series of tests which are not necessarily related to the actual circuit function. Observation of the leakage current and reverse breakdown of components and chips as they may be obtained from the external leads gives some insight into the quality. They also provide useful life test acceptance criteria. Measurements of leakage currents before and after high temperature storage or operating life tests may be employed to indicate reliability. In summary, integrated circuit testing presents frustrating problems to the user. Not only is "black box" testing

Black Box Testing

MONOLITHIC CIRCUIT FUNCTION TEST

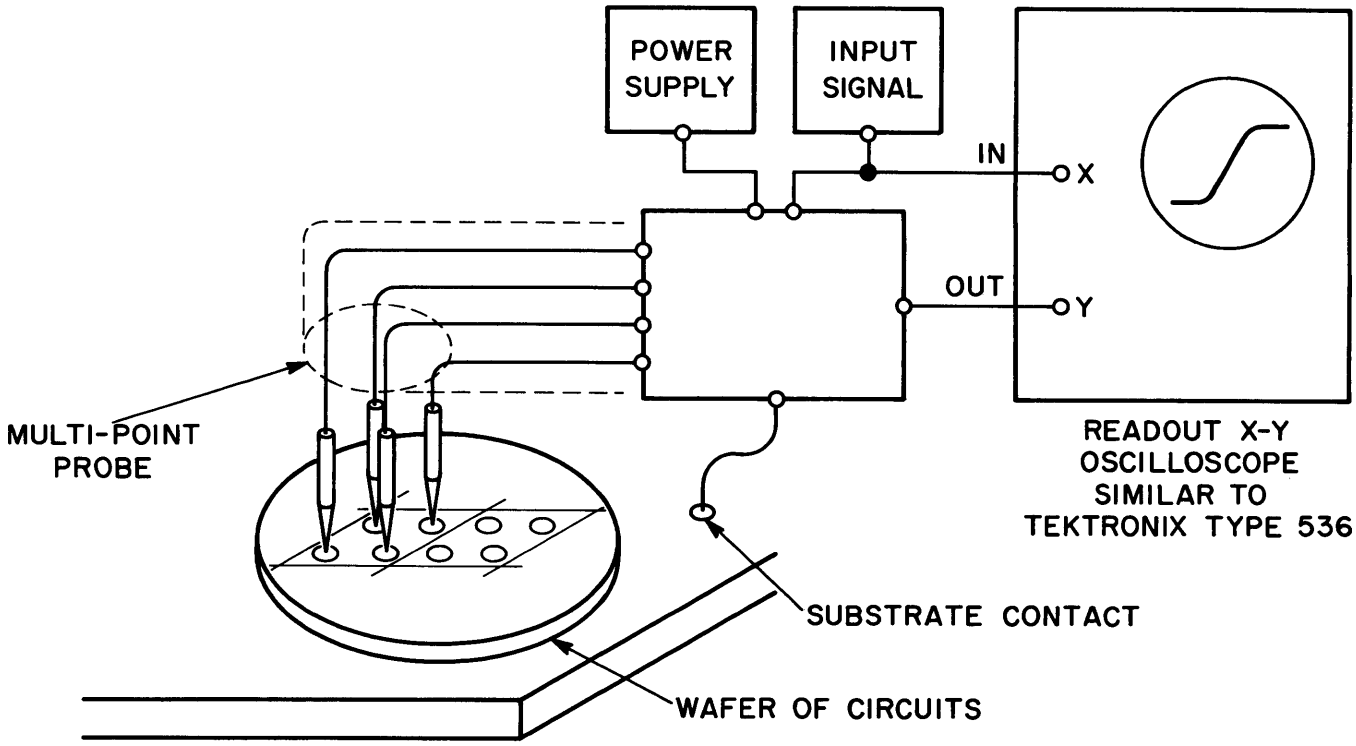


Figure 4-11

"BLACK BOX" LIMITS FOR TRANSFER CHARACTERISTICS

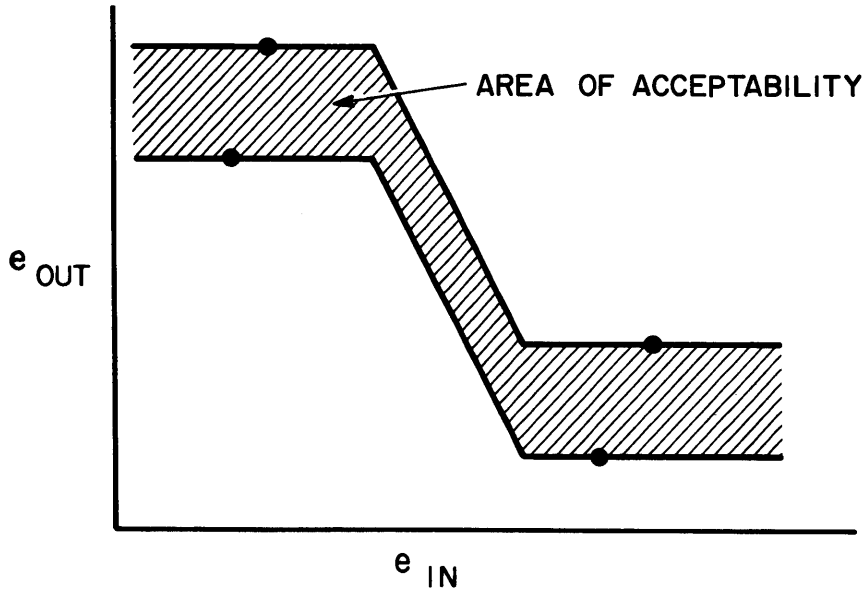


Figure 4-12

4.8 (Continued)

frequently inadequate, but also direct correlations for conditions other than those of the test are hardly ever available.

4.9 Total Cost

The total tooling cost ranging between $1000. and $5000. for a silicon monolithic circuit frequently make it unsatisfactory for low volume production quantities. Other assembly techniques, such as multichip or thin-film, may be used to fabricate small quantities (Figure 4-13). These assemblies may also be useful for prototype and breadboard analysis.

4.10 MOS Fabrication

Diffusion

MOS transistor fabrication requires fewer diffusions than the bipolar types described previously. Operating upon the principle of field effects induced through a thin dielectric, MOS integrated circuits would not need a separate isolation diffusion. This not only permits a simplified fabrication process, but also permits the inclusion of a larger number of components within a given area.

Ionic Contamination

The principle yield problem in earlier fabrication of MOST devices related to residual ionic contamination on or within the oxide. The contamination in the form of positive ions may be introduced during both the chemical etching or diffusion processes.

Several successful methods of either limiting or reducing the ionic contamination have been developed. One method prevents the ionic contamination from entering the oxide by employing special oxidation furnaces. Other techniques involve the removal of contaminated oxides and replacement with clean oxides or the use of getter materials which provide stabilization.

It appears that most commercial suppliers employ the oxide removal/replacement/gettering method while Bell Laboratories leans toward the use of contamination-free furnaces.

MOS Transistors

Available MOS transistors are stable with fixed gate voltages up to temperatures of approximately 200°C. This results in shifts of gate current or applied bias conditions of less than 10%.

MOS Circuits

Extension of the technique for fabrication of MOS devices is directly applicable for integrated circuits. Since this fabrication method requires fewer diffusions, large production savings are possible if yield levels can be maintained. Within a relatively short time, all major manufacturers can be expected to have MOS facilites. Present growth is retarded primarily by extremely large orders for the conventional diffused device.

TYPES OF INTEGRATED CIRCUIT CONSTRUCTION

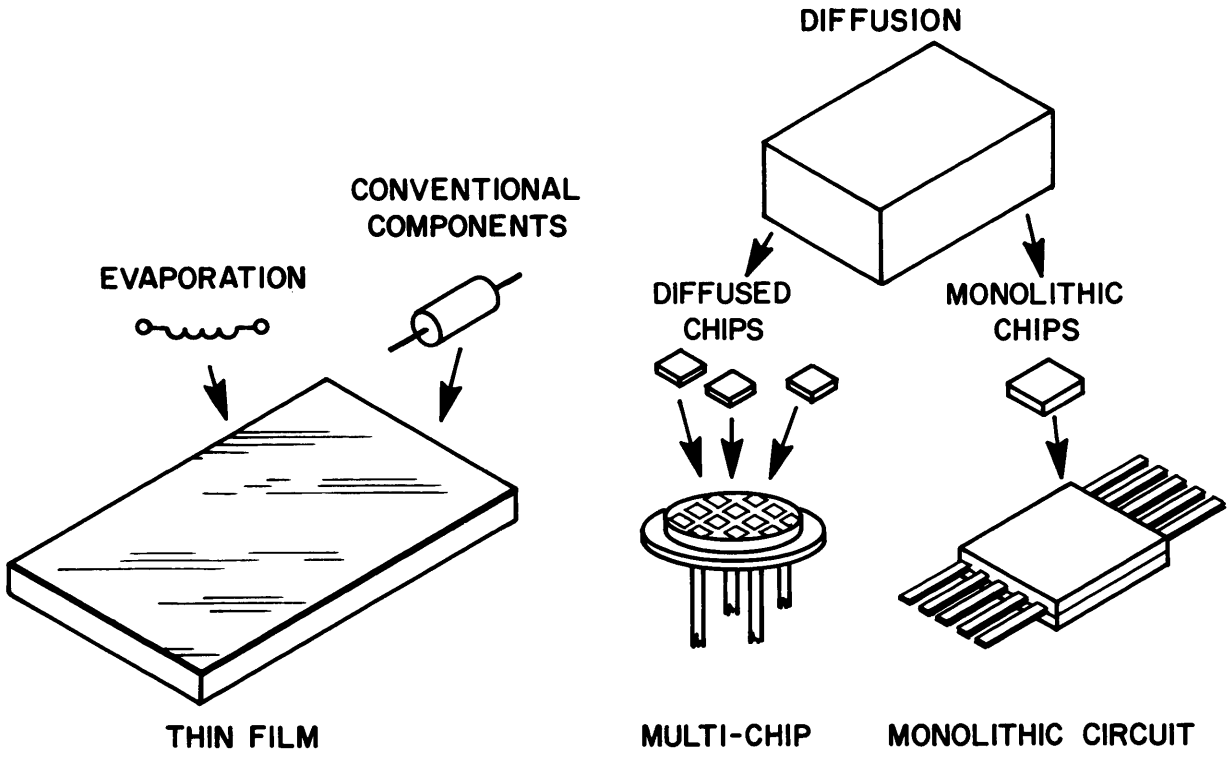


Figure 4-13

SECTION 5 DIGITAL INTEGRATED CIRCUIT APPLICATIONS

5.0 Introduction

This section has been prepared under the assumption that the reader as a competent marketing specialist concerned with digital applications is familar with binary arithmetic and Boolean algebra as well as basic logic elements. As a reference, a condensation of this material is included in Appendices A and B at the end of this book.

This section is divided into five general areas:

1. Significant parameters of logic circuits
2. Logic families
   a. Threshold type, (DTL, RTL, RCT, T^2L, etc.)
   b. Current Mode Logic (CML)
   c. Complementary Transistor Logic (CTL)
   d. MOS logic
3. Basic Logic Elements and Flip-Flops
4. Digital Systems Considerations: simple examples, counters, interfacing circuits, etc.
5. Comparisons of Currently Available Types of Logic in Integrated Circuit Form

Positive logic is used throughout this section. (See Appendix A).

5.1 Integrated Logic Circuits

A study of commercially available integrated logic circuits indicates that many have been designed to meet certain particular requirements. Frequently, to achieve advantages in one characteristic, other parameters must be compromised. Low power consumption circuits exhibit long propagation delays. Conversely, highest speed operation consumes the most power. Our discussion of the various types of logic circuits will bear heavily upon the design compromises employed which bear on their suitability for a given application.

To evaluate various circuits, those characteristics which must invariably be included will be considered first. These are:

1. Speed-power
2. Noise immunity
3. Fan-out and Capacitive drive capability
4. Circuit flexibility

5.1.1 Speed-Power

Speed and power must usually be considered together since, to date, most efforts to achieve higher speed logic operation have required greater power dissipation. Extremely low power dissipation logic systems such as MOS are characterized by low speed operation. The system's operating requirements usually dictate the logic speed or delays that can be tolerated. Satisfying the power and associated heat removal requirement then becomes a systems engineering problem. Frequently, the use of different logic circuitry can ease particularly difficult speed or power problems by exchanging one for the other. Alternately, simple rearrangements of the logic elements may avoid some of the delay associated with series operation to obtain greater speed without material increases in the power requirements. (Figure 5-1).

5.1.2 Noise Immunity

Industrial equipment almost always operates near such sources of wide band noise as relays, stepping switches, motors, etc. On large systems, engineering is demanded to control both the source and its effects. Moreover, with logic circuits, the relationship between noise immunity and circuit speed capability must not be

TWO METHODS OF IMPLEMENTING THE SAME LOGIC FUNCTION

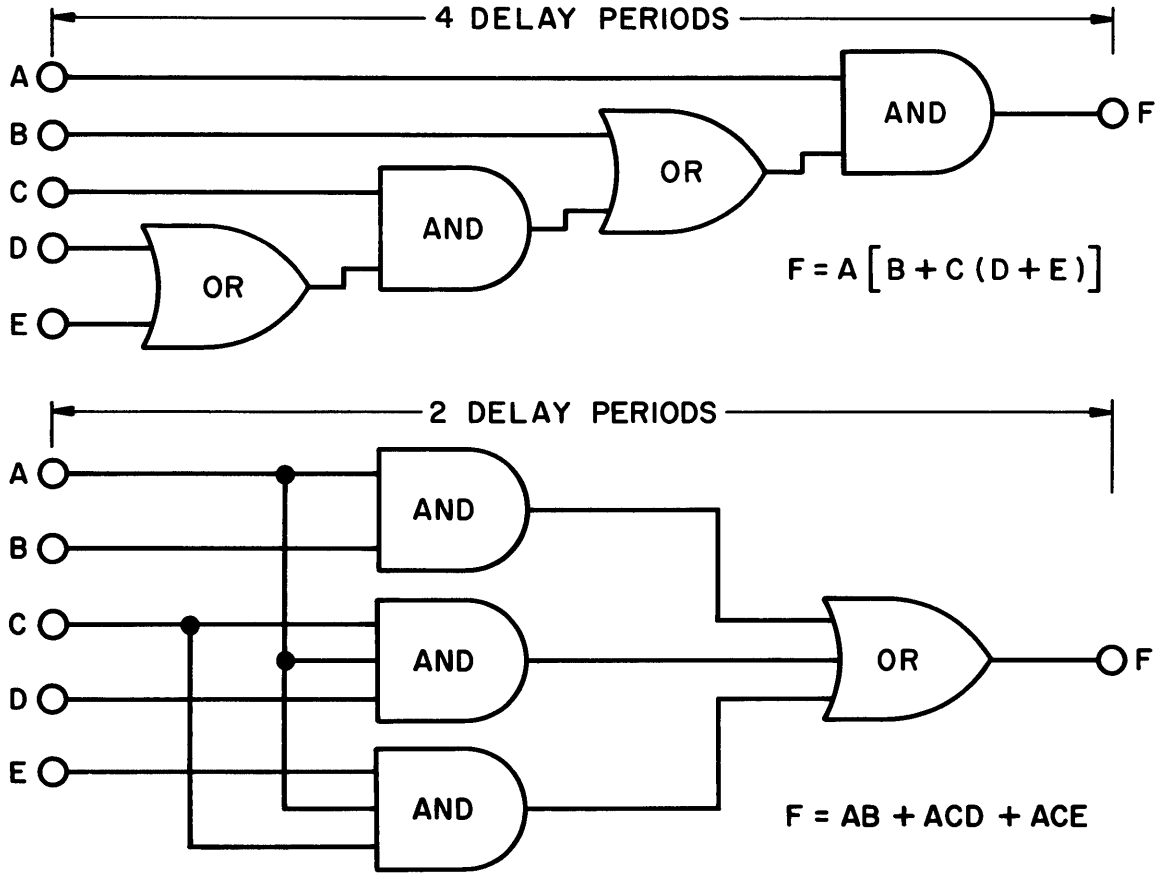


Figure 5-1

overlooked. The higher the speed capability, the narrower the pulse to which it will respond. Since the noise is most often in the form of spikes, noise problems increase with circuit speed.

5.1.3 Fan-Out

High fan-out offers obvious economies in driving reset lines of flip-flop registers, control signals and mass transfer gauge and mode control signals. Another advantage is related to systems speed. It often happens that the high speed requirement exists in only a small portion of the system and it is usual to organize that portion of the logic in parallel. To illustrate, consider the following function (F) which is expressed in two equivalent ways:

$$F = A\ [B + C\ (D + E)] \qquad F = AB + ACD + ACE$$

These logic arrangements are shown in Figure 5-1. If the function were implemented as in the first expression, it would consist of an OR-AND-OR-AND cascade requiring four gates having a series of four propagation delays. Since each term appears only once, each would constitute one load on the respective signal source. Implementing the function indicated in the second expression, four gates would still be required. However, the three AND combinations would be formed concurrently and then combined through an OR gate requiring only two propagation delays. The term A appears three times and C appears twice, indicating the higher fan-out requirement on those signal sources. In general, parallel organization requires higher fan-out and, to a lesser extend, higher fan-in. Higher fan-in is easily achieved with gate extenders, but higher fan-out is only achieved by circuit design or by duplication.

Fan-out is limited at the lower end of the temperature range by current drive capability, and at the upper end by the collector-emitter (V_{ce}) saturation voltage in the turn-off threshold. In general, minimum fan-out is guaranteed over the full specified temperature range, allowing for adequate DC margins.

As an example, the fan-out of the typical DTL gate at 25°C may be determined as follows: Assume a 0.5 volt DC margin. From Figure 5-2, it is apparent that for V_{in} equal to or less than one volt, V_{out} remains high and there is no leakage. Thus the V_{ce} saturation of the previous stage may become as high as 0.5 volt (1. - 0.5). Referring to Figure 5-3 for a V_{ce} saturation at 25°C, less than 0.5 volt, the output-collector drive may be as high 16.5 mA. Referring to Figure 5-4, it can be seen that each driven gate will supply 1.5 mA for the worst case, with the input grounded. Assuming an overdrive factor of 1.1, each will take 1.1 x 1.5 mA = 1.65 mA of current. Thus, 16.5/1.65 = fan-out of 10 for the given conditions.

In terms of AC, the fan-out of a unit is limited only by the effect of the RC time constants on the propagation delay of the circuits.

Capacitive Loads

The ability to drive high capacitive loads almost eliminates the need for extra buffers. This capability also makes it possible to design greater accessibility into system packaging by eliminating the need to minimize interconnection capacitance by close spacing. Signal tracing is easier when parts are more accessible. Available test points reduce the amount of unplugging and/or demounting.

Propagation delay is the time necessary to activate the circuit plus the time needed for the circuit to change from its existing state to the threshold level of the following circuit. The ability to drive capacitive loads without signal edge deterioration thus offers higher system speed capability.

OUTPUT VOLTAGE VS INPUT VOLTAGE OF A TYPICAL DTL GATE

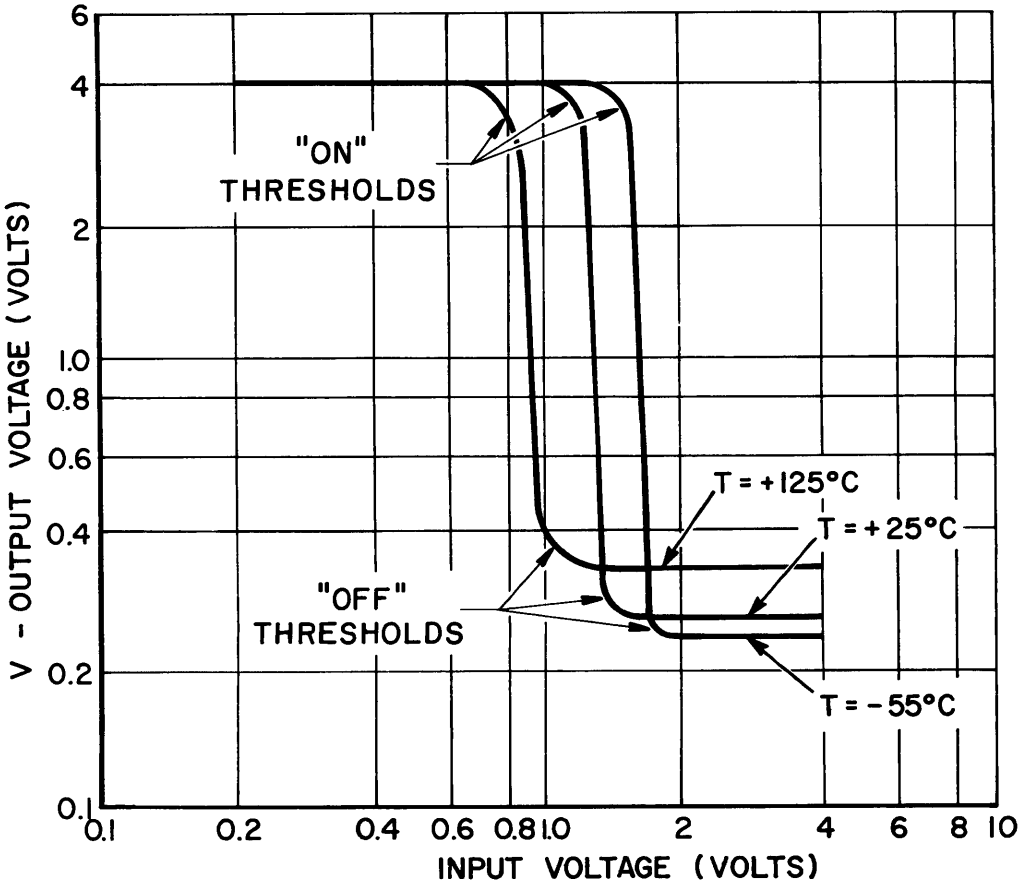


Figure 5-2

COLLECTOR SATURATION VOLTAGE AS A FUNCTION OF TEMPERATURE

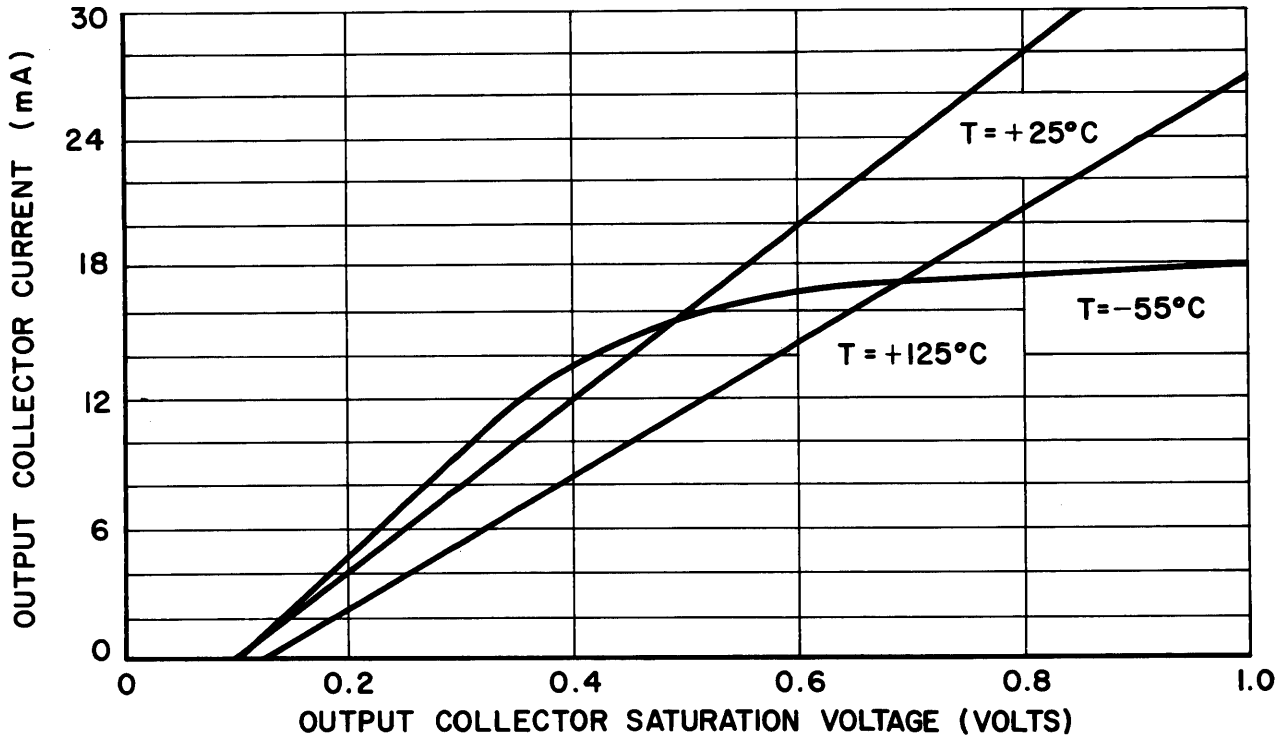


Figure 5-3

5.1.4 Circuit Flexibility

The characteristics of the flip-flop are extremely important in total system design. Clock problems are less severe if the flip-flop has internal protection against race conditions. Without this protection, dual rank registers and two-phase clocking may be required to protect data integrity. Multiple clock inputs with associated gating structures are also of significant benefit. The application for this type of flip-flop input arises when it is desired to load registers from more than one source. The input data is normally synchronized with its own clock while the inter-clock deviations may not be well defined. Therefore, even though external gating may suffice to combine data inputs to the flip-flop, the nature of the clock signals and their interrelationships make them difficult to combine with gating external to the flip-flop. This type of problem is most frequently encountered at the interface between major logic structures.

To a lesser extent, individual set and reset clock inputs find application where it is desired to set flip-flop from one source and reset it from another source. In nearly every application, there is a need to reset (clear) or set (preset) flip-flops without the need for clock signals. Initiating any digital system normally includes the use of a level signal to load all of the system registers to a predetermined state from which operation can commence. In most applications, it is advantageous for the flip-flops to have high fan-out. Registers provide the primary signal source for all logic structures. When the registers (flip-flop groupings) provide high fan-out, more freedom is available in the design of the logic structure.

5.2 Integrated Circuit Logic Forms

A wide variety of circuit configurations are available to perform the required logical functions. More important circuit configurations have been given names which generally describe the organization of circuit components. While each configuration may be designed to perform the same logical functions, differences in characteristics may make one more applicable in a particular system than another. The following section contains a comparison of the important electrical characteristics of the different basic logic configurations. Since DTL circuits represent the most widely used logic form, they will be studied in considerable detail and used as a basis for comparison. Much of this analysis will however apply to the other logic forms.

5.2.1 Diode Transistor Logic

Briefly, DTL implies the use of diodes in the inputs coupled to the base of a common-emitter transistor output amplifier. Although there are many arrangements possible within this definition, some with limited performance capability are not used. The circuits described herein will be confined for simplicity to those employing positive logic AND gates at the input and an NPN transistor at the output. Typically, this class of circuits contains the current source necessary to operate its input gate and transistor at the specified speed and load.

DTL popularity rests upon its being one of the better compromises of the many design factors which must be evaluated in implementing logic functions. Also, DTL is familiar because it has been widely used by discrete component circuit designers. These factors account for its wide and early acceptance in integrated form.

The fundamental DTL configuration is illustrated in Figure 5-5. This type of circuit affords the user several options:

1. The pull-up resistor, R_L, can be connected to the collector of the output transistor to charge line capacitance if desired

INPUT CHARACTERISTICS OF TYPICAL DTL GATE

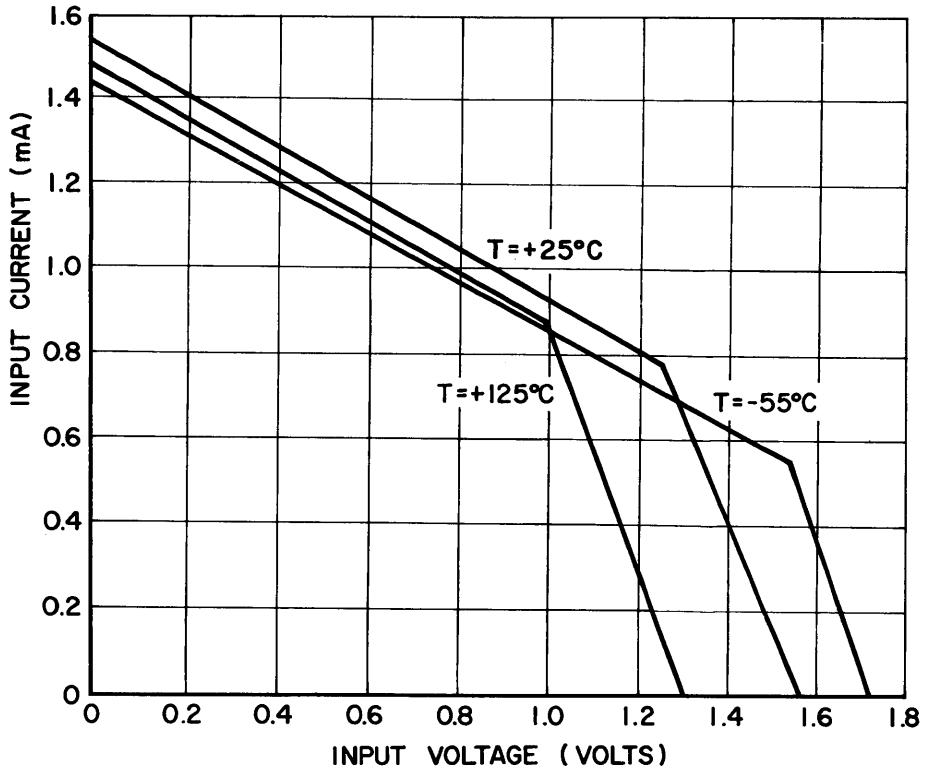


Figure 5-4

FUNDAMENTAL DTL CONFIGURATION

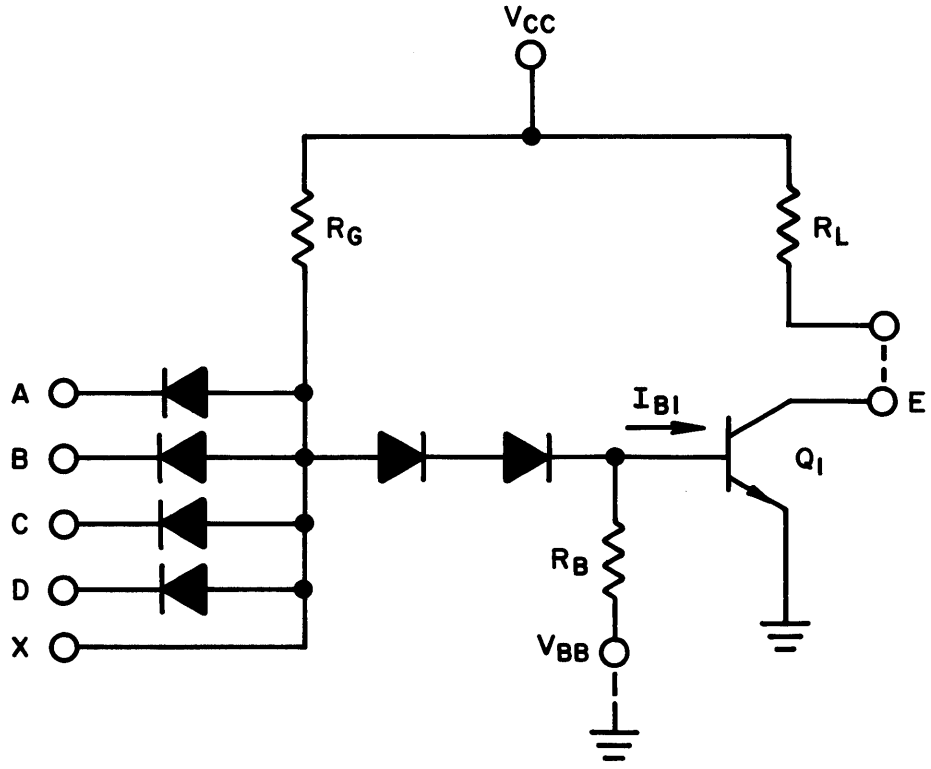


Figure 5-5

5.2.1 (Continued)

2. A gate extender such as that illustrated in Figure 5-6 can be connected to the gate node, X, to increase fan-in
3. For low power operations, the base resistor, R_B, can be returned directly to ground, eliminating the need for the additional negative supply (V_{BB}).

To determine the input threshold characteristics of a DTL circuit, consider the symmetric currents steering gate of Figure 5-7. The V-I characteristic of CR_2 can be drawn as a load-line intersecting the characteristic of CR_1 for various values of input voltage. This is illustrated in Figure 5-8 for the two values of V_{IN}, which cause 99% switching of I_G. These two V_{IN}, I_1 points are indicated on the curve of Figure 5-9, which is easily drawn by determining several intermediate load-line intersection points. The threshold characteristic shows that 90% switching occurs for an input voltage swing of less than 150 millivolts, and that a voltage swing of 300 millivolts can achieve 99% switching. This is the basis of the switching action of a DTL circuit.

The asymmetric gate of Figure 5-10 simulates a circuit of Figure 5-5 with CR1 representing the transistor emitter-base diode. The two intermediate diodes between CR2 and CR1 shift the threshold voltage. Compare Figure 5-11 to Figure 5-9. They not only raise the threshold voltage, but also provide immunity from noise on the input lines. Higher values of R_B will raise the threshold further by increasing the current level in the intermediate diodes before CR1 can begin to conduct. The shunting effect of R_B reduces the maximum value of I_1. From the bottom curve of Figure 5-11, it can be seen that the principal effect of a finite value of R_G is to reduce the maximum value of I_1. All three curves of Figure 5-11 indicate a significant DTL circuit characteristic - the value of I_1 (the base input curve) is independent of input voltage outside of the transition region. With all its components on the same chip, a monolithic integrated circuit is much more efficient than a multichip or discrete component design because all of its resistors have the same percentage shift from the design center values resulting from fabrication or operating temperature changes.

The gate of Figure 5-5 is shown in Figure 5-12 with only one input, typical resistor values and the pull-up resistor R_B(SK), connected to ground instead of a separate supply V_{BB}. The transistors have the gain characteristics shown in Figure 5-13. Using the lower curve of Figure 5-11 and assuming the driving inputs are from similar circuits, the resulting plot of output versus input voltage at several different temperatures is shown in Figure 5-14. From these curves, input noise margins can be determined. At 25°C (Figure 5-14B and Fan-Out of 8), an input noise signal of as much as 1.2 volts would not affect the output voltage, while an input signal voltage greater than 1.7 volts causes the output voltage to drop to 0.4 volts or less. Thus the DC turn-on noise margin with the input low:

$$\text{Noise margin} = \text{Minimum threshold voltage} - V_{CE}(\text{Sat})$$
$$\text{at } 25°C = 4.0 - 1.7 = 2.3 \text{ volts.}$$

At - 55°C, these noise margins become 1.0 and 2.1 volts respectively, while at 125°C they are 0.4 and 2.7. Thus, a full temperature range specification could guarantee a 400 mV noise margin. Optional connections to the circuit shown in Figure 5-5 permit performance compromises. In a lower power configuration, larger values of R_B, R_L and R_G charging current are available during turn-on and less current available through R_B to remove stored charge from Q1 during turn-off.

GATE EXPANDER

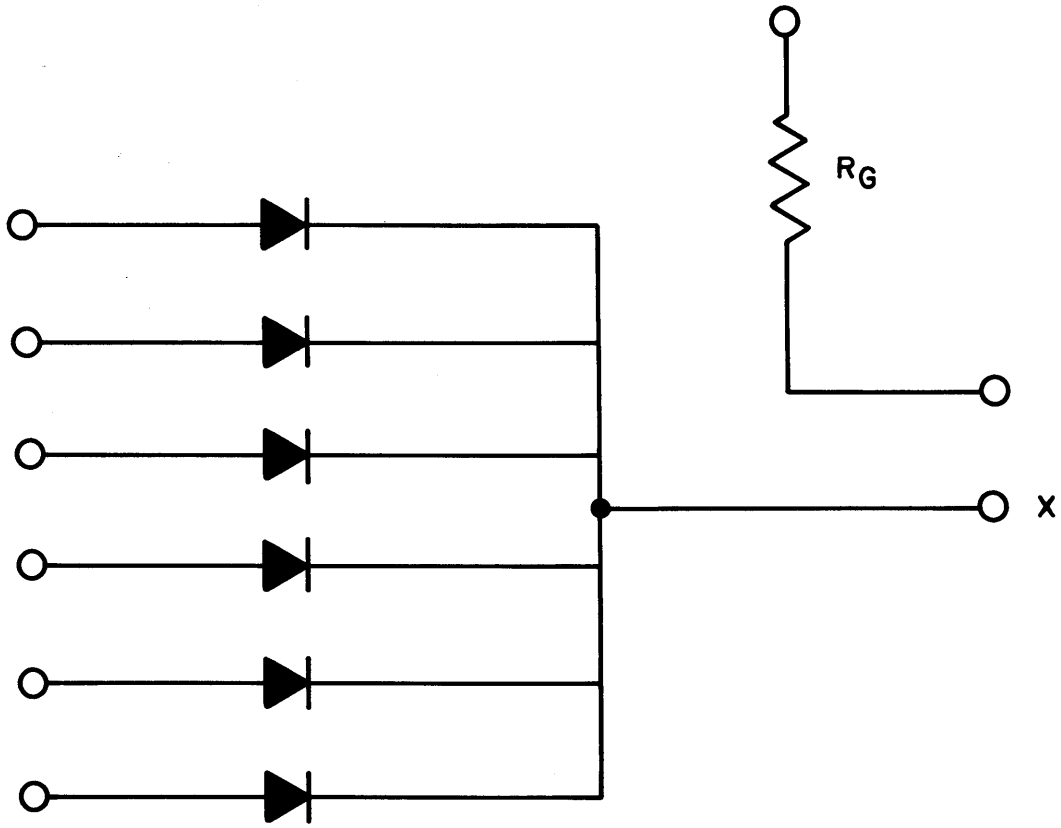
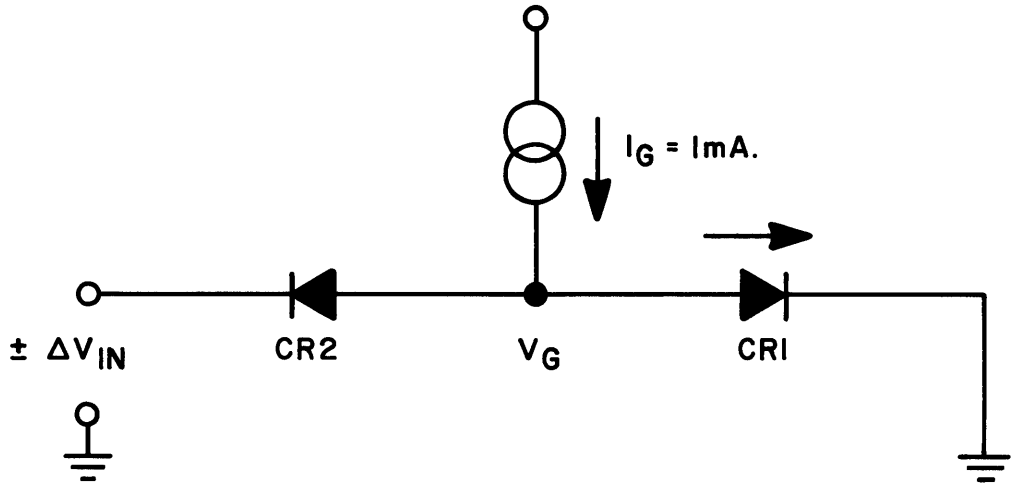


Figure 5-6

SYMMETRIC CURRENT STEERING GATE



DIODE CHARACTERISTIC

V	0.55	0.68	0.70	VOLTS
I	0.01	0.50	1.00	mA.

Figure 5-7

LOAD LINES FOR DIODE SWITCHING I_l FROM 1% TO 99% OF I_G

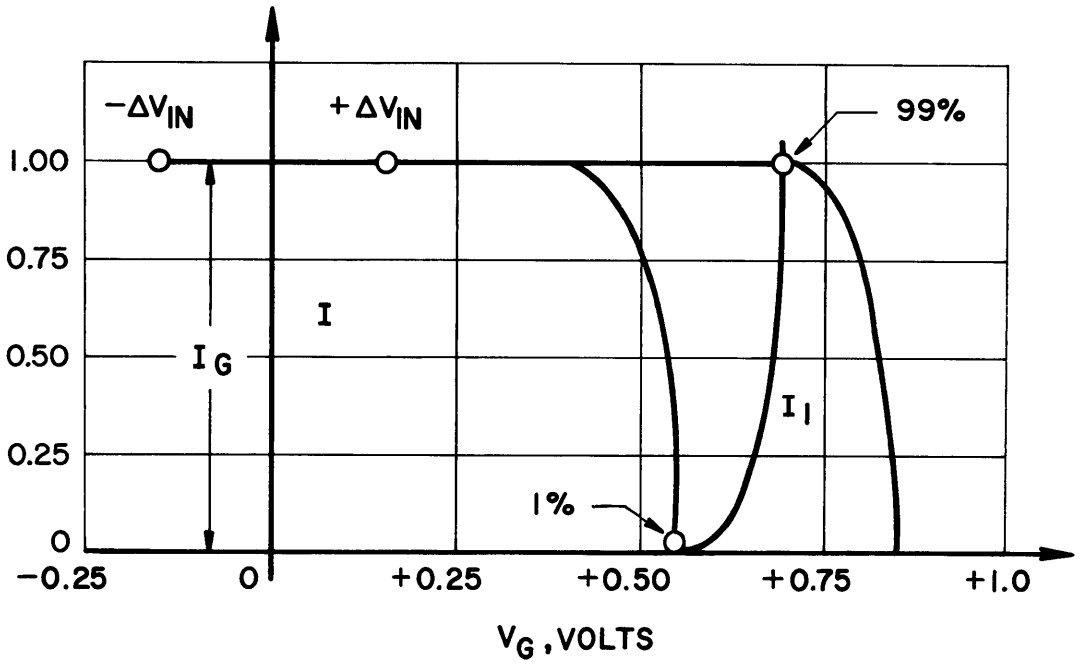


Figure 5-8

V_{IN}-I_l CHARACTERISTICS OF A DIODE GATE

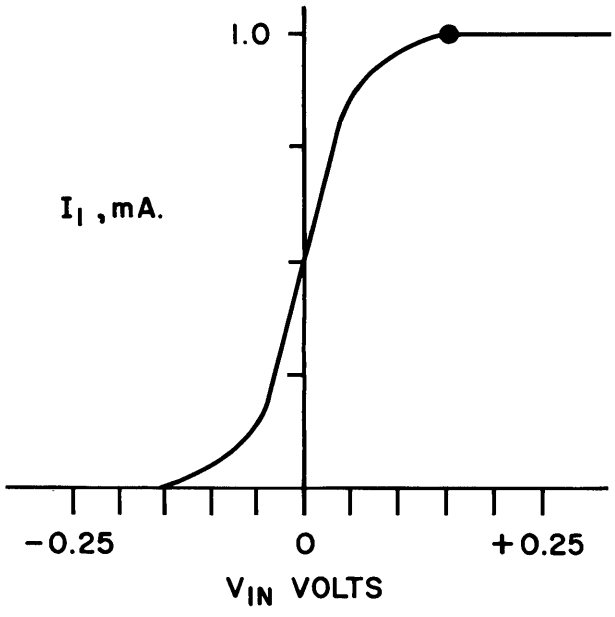


Figure 5-9

ASYMMETRIC CURRENT STEERING GATE

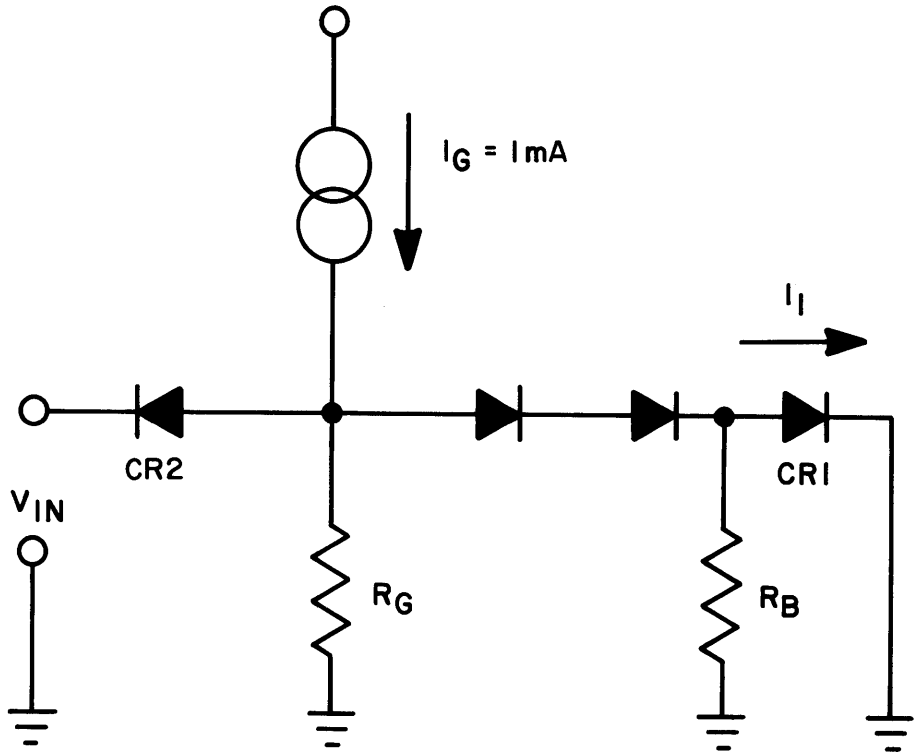


Figure 5-10

THRESHOLD SHIFT IN ASYMMETRIC GATE

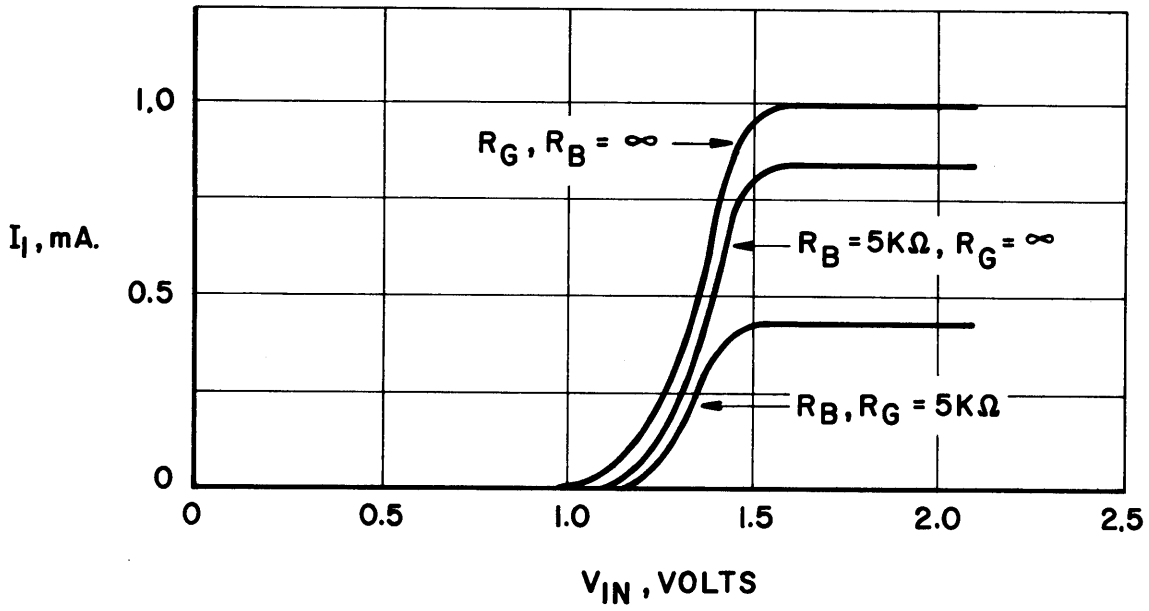


Figure 5-11

DTL GATE WITH LOADING

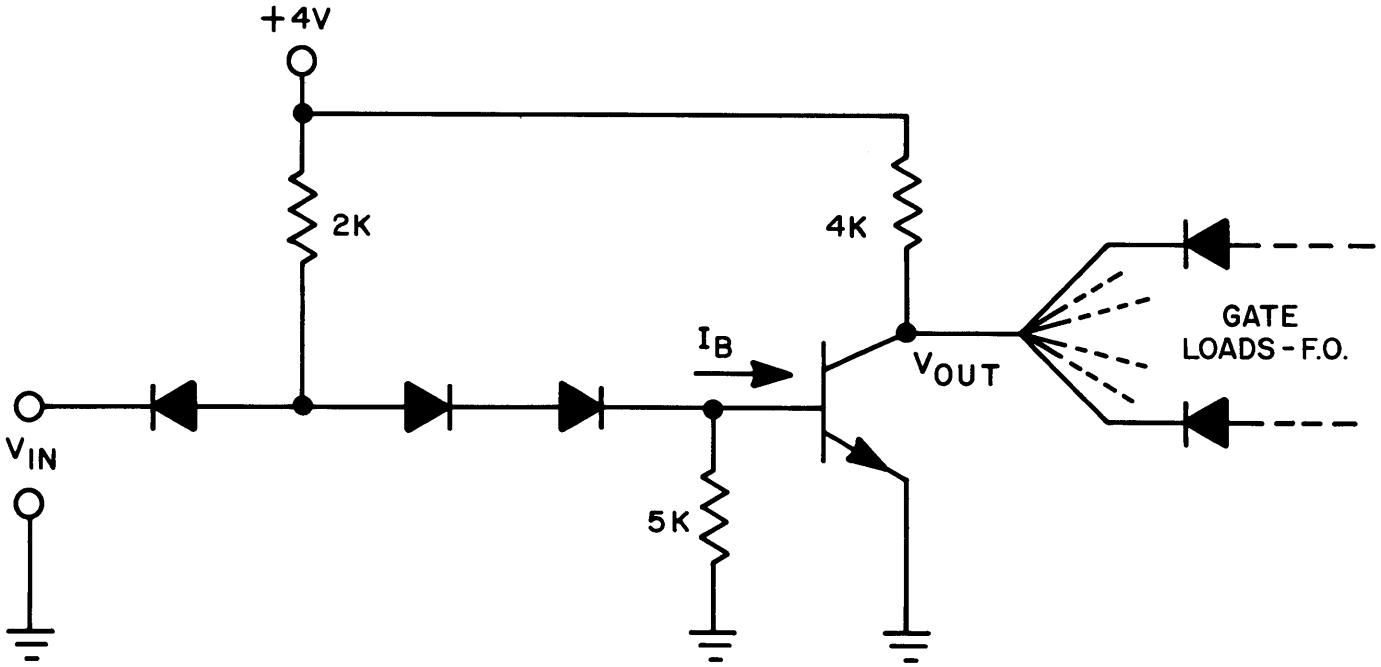


Figure 5-12

GAIN CHARACTERISTICS OF A DTL TRANSISTOR

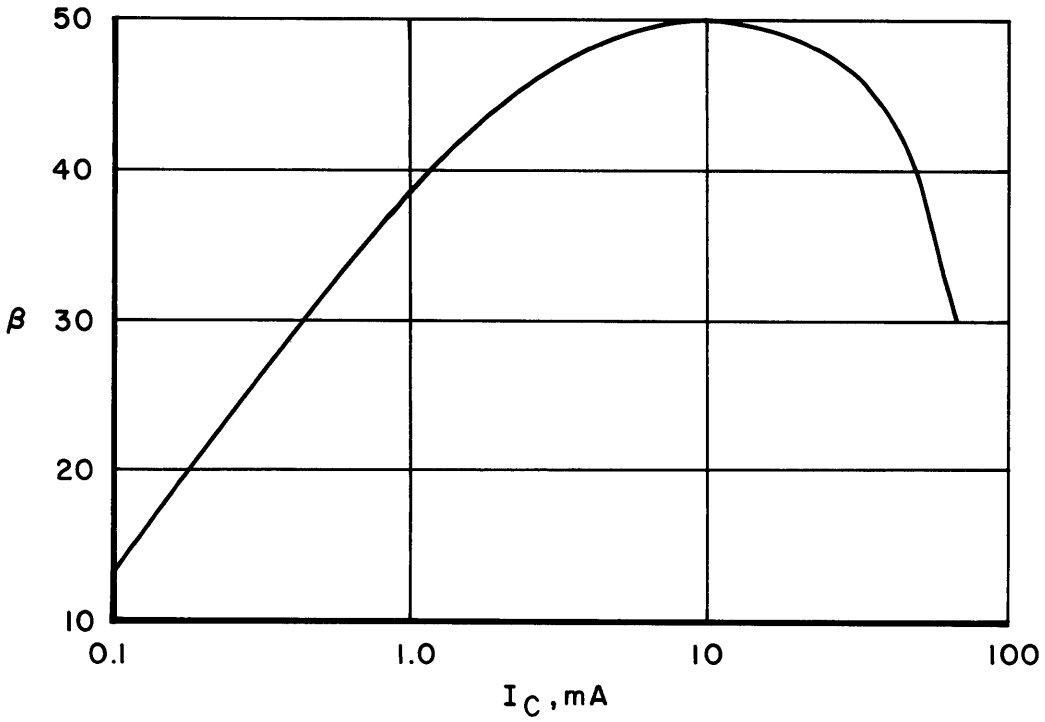


Figure 5-13

TRANSFER CHARACTERISTICS OF A SE 180 DTL GATE

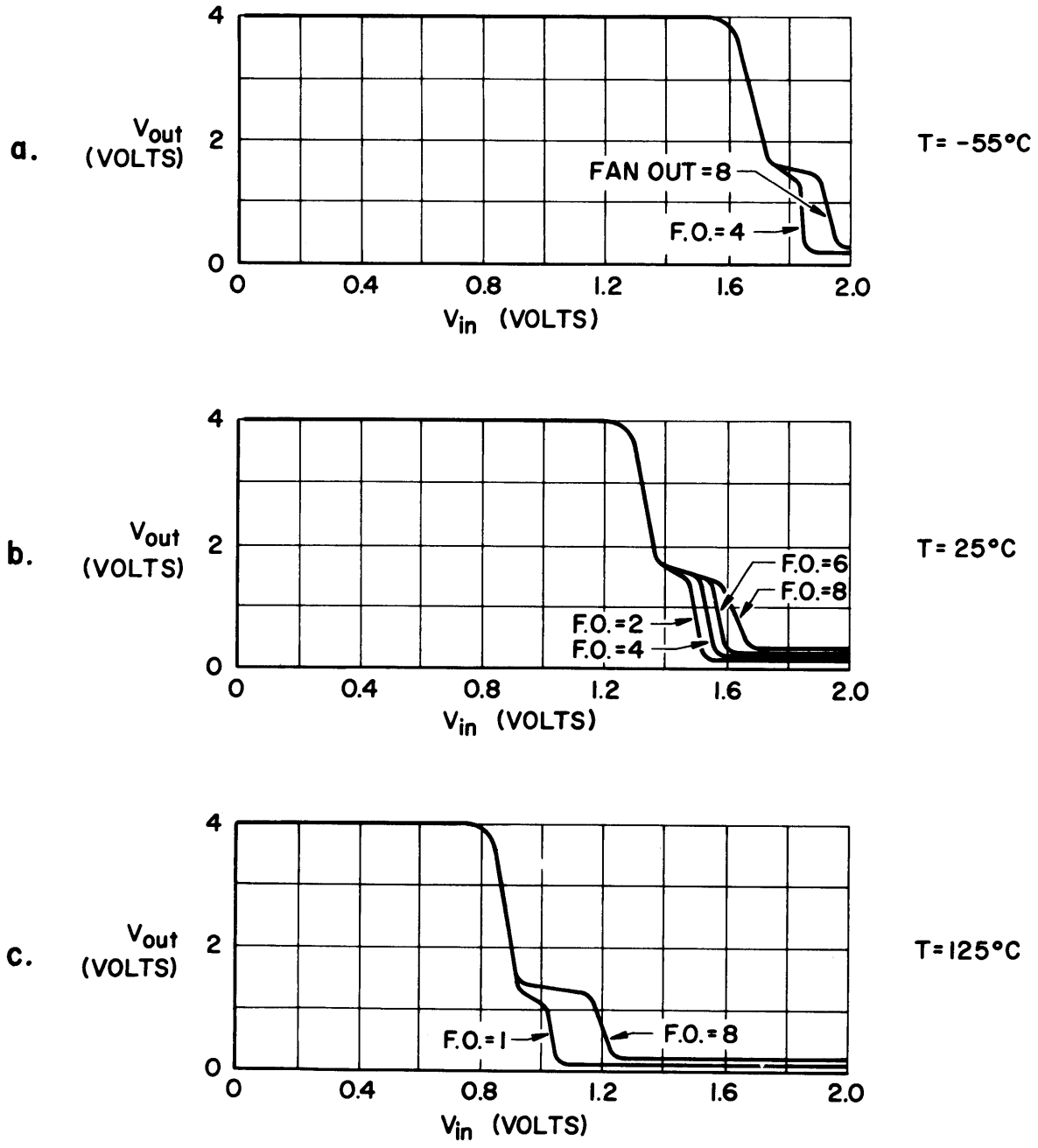


Figure 5-14

5.2.1 (Continued)

This sacrifices speed for lower power consumption. Use of the gate expander increases turn-on time, since the gate current must charge the capacitance between each additional diode and the grounded substrate. Thus, a fan-in-speed compromise is involved. Decreasing the load resistor R_L decreases output voltage rise time and increases power consumption, but reduces the fan-out. This is a speed-fan-out or power compromise. Use of an optional pull-up resistor permits extensive collector logic to be performed without sacrificing fan-out.

5.2.2 DTL Variations

Many variations of DTL circuits have been designed. Figure 5-15 illustrates a circuit employing an emitter followers between the AND gate and the base of the output transistor. This configuration provides increased circuit power gain because of the series transistors, and also a larger fan-out capability. Greater fan-out capability results from the lower output impedance which reduces the effects of loading without affecting the noise margins.

Other variations of DTL have been produced to take advantage of the unique features available through monolithic integrated circuit processing. These tend to emphasize high yield to obtain performance at low cost, and generous use of transistor gain (which is cheap) to relieve other component tolerances. AND gates are traditionally formed from diode arrays; however, the function can be produced at slightly lower cost and higher uniformity by using a multiple emitter transistor (Q1) as shown in Figure 5-16 (this is actually a form of TTL). An emitter output stage is employed to give the current gain required for high fan-out and low output impedance, and to provide a voltage drop to compensate for the voltage rise at the input. This compensation makes the maintenance of logic levels from stage to stage much easier. Diode (D1) connects the gate and the output transistor to assure good response to negative going waveforms.

The basic NOR gate for the family is shown in Figure 5-17. In this design, transistors are used to provide the input current gain, thus reducing some of the loading effects. Active pull-up/pull-down is employed to provide the ability to drive the large capacitances associated with long signal lines or high fan-outs, and to insure the low output impedances necessary for fast switching. The propagation delay with this output configuration is relatively insensitive to line capacitance. An increase in load capacitance from 100 pF to 200 pF will increase the propagation delay by less than 35%. With passive pull-up, the increase can be as large as 100%. This NOR uses emitter followers (Q1, Q2 and Q3) to permit low input currents consistent with high fan-in and higher internal currents to maintain high transistor gain and fast switching.

Input thresholds are largely determined by the resistor ratios, R_1 to R_2, and R_4 to R_6. These ratios may be adjusted to optimize the threshold with respect to the signal swing and to improve the noise immunity. The ratios may also be adjusted so that Q4 always turns on at a lower voltage than does Q6. This insures that both output transistors cannot be turned on simultaneously, thereby eliminating this as a cause of supply voltage noise. The threshold tends to be uniform since, in integrated circuits production, resistor ratios are easier to maintain than absolute values.

Noise generators within a typical DTL logic circuit are indicated in Figure 5-18. The diode gate provides good isolation for signal noise. When the input is high, the gate diode is back biased by a voltage determined by V_{CC} of the driving state of the forward drop of the series diodes, and $V_{BE}(SAT)$ of the output transistor. When the input is low, the bias diodes keep the output transistor off.

DTL CIRCUIT CONFIGURATION FOR HIGH FAN OUT

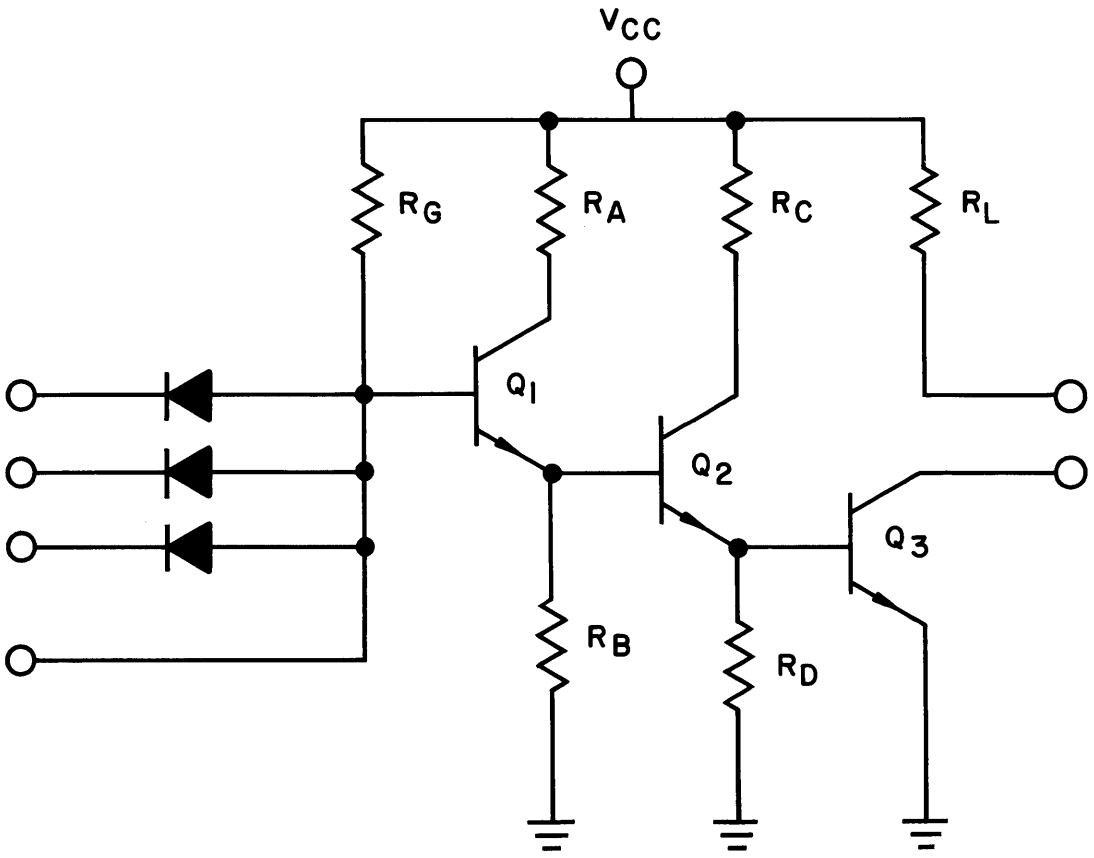


Figure 5-15

MODIFIED DTL AND GATE

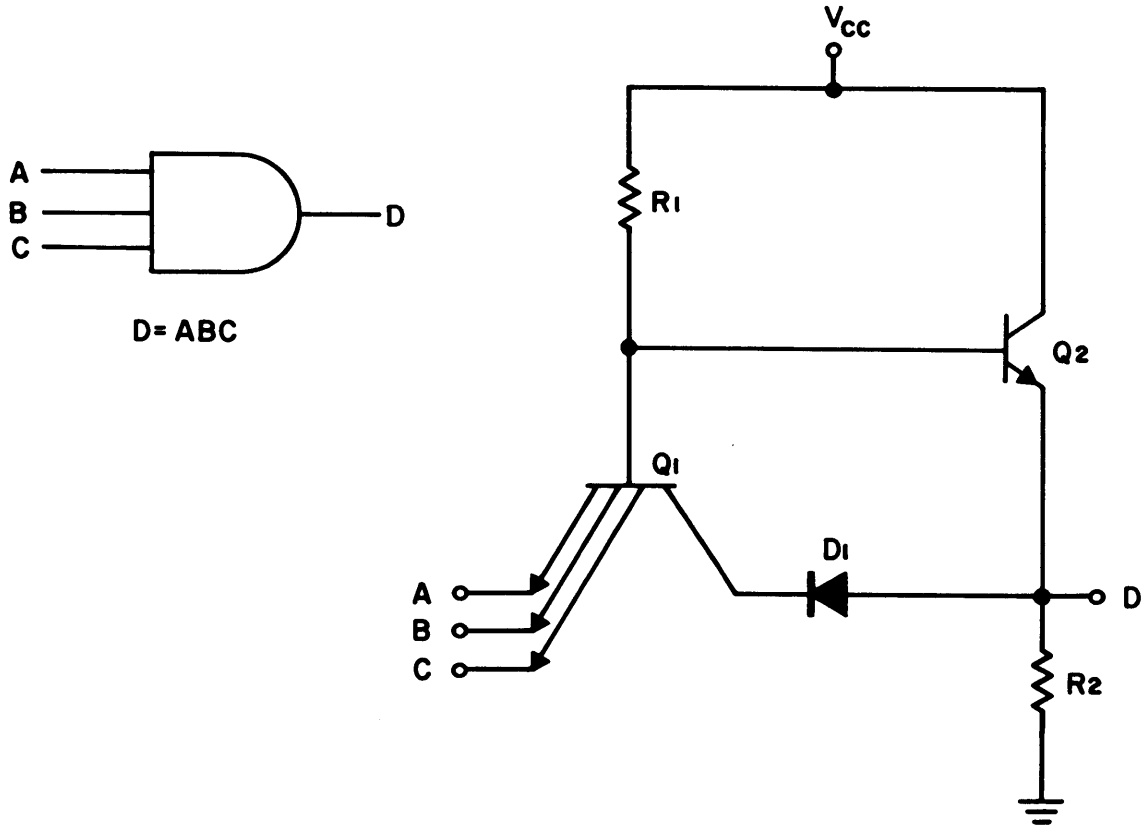


Figure 5-16

MODIFIED DTL NOR GATE

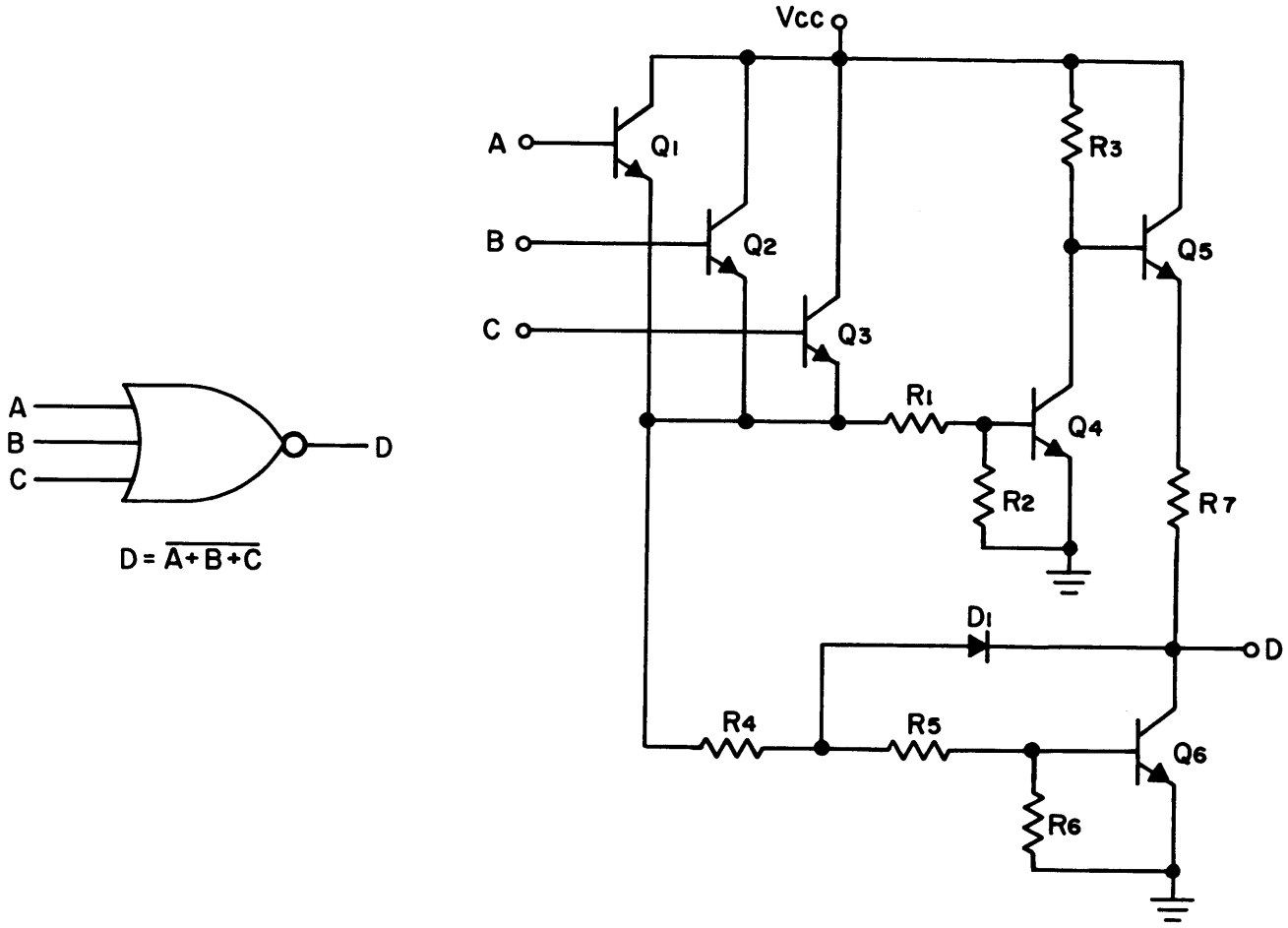
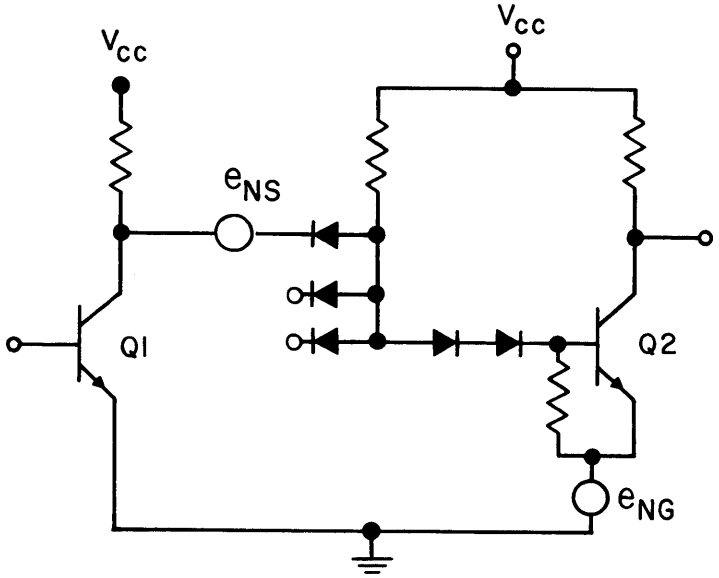


Figure 5-17

DTL NOISE IMMUNITY



WHEN INPUT IS PLUS, e_{NS} IS DISCONNECTED BY BACK BIAS ON GATE DIODE. e_{NG} DRIVES THE EMITTER DIRECTLY AND IS AMPLIFIED WHEN Q2 IS ON BORDER OF SATURATION.

Figure 5-18

5.2.2 (Continued)

At first, it appears that any desired noise immunity can be achieved with DTL by the choice of these biases. However, there is a separate ground noise problem. When the input is high, the AND gate output resistor supplies current to the transistor. Ground noise is in this signal loop. If the output load is heavy and a minimum gain transistor is in the circuit, it may be operating close to saturation. Under this condition, the ground noise will be amplified. Ground noise immunity may thus establish the net noise immunity of DTL circuits.

5.2.3 DCTL Logic Circuits

Direct-Coupled-Transistor-Logic represents the simplest form of useful logic circuits in terms of component count. (See Figure 5-19). Component counts, however, are less important in integrated circuits than in discrete component circuits.

DCTL circuits problems develop when several gates are driven from a single source. The slight unit-to-unit variations in base-to-emitter saturation voltages of the transistors generate most of this difficulty. If, among several different load transistors, one turns on first and saturates with low V_{BE}, it is possible that all the available source current may be taken by this transistor.

The remainder of the load transistors cannot turn fully on since the input voltage has been clamped by the low $V_{BE}(SAT)$ transistor to a value below their own base-to-emitter saturation voltage. Such a condition is referred to as "current-hogging". Even when all of the transistors are well matched as they might be when fabricated in an integrated circuit, the nonlinearity of the input characteristics makes hogging probable. DCTL circuits are also susceptible to noise because of their narrow signal voltage swings, as shown in Figure 5-20. DCTL, in integrated circuit form, has not seen widespread use because of the application problems.

5.2.4 Resistor Transistor Logic

By putting resistors in series with the base (as shown in Figure 5-19), the current hogging problem associated with DCTL may be minimized. This arrangement produces the RTL circuit family. Raising the gate input resistance allows the current to divide evenly among the driven transistors. The series base resistance, however, reduces the frequency response because the input capacity of the transistor must charge and discharge through this added resistance. To compensate, the turn-on drive voltage can be raised by increasing the supply voltage, V_{CC}. The turn-off margin is fixed, being dependent upon the voltage drop across the transistor in saturation. This presents a particularly serious frequency response problem with respect to turn-off since the capacitance must discharge through the resistor. To minimize the sacrifice in speed, a relatively low value resistor must be used. The improved frequency response is made at the expense of higher power levels.

The RTL noise immunity is better than DCTL, but still has significantly less than DTL. RTL noise margins are dependent on actual fan-out design. Consider the case of a heavily loaded gate driving a lightly loaded gate. When the source gate is low (output transistor saturated), a noise voltage (generated at the input to the load gate) would be developed across a low impedance load. With heavy loading, however, the base drive of the source gate may barely be holding the output transistor in saturation. At this point, the noise voltage impedance is increased. At the same time, the larger number of loads in parallel effectively reduce the impedance level again. Hence, by compromising parameters, the noise immunity can be controlled somewhat more than DCTL.

DIRECT COUPLED TRANSISTOR LOGIC

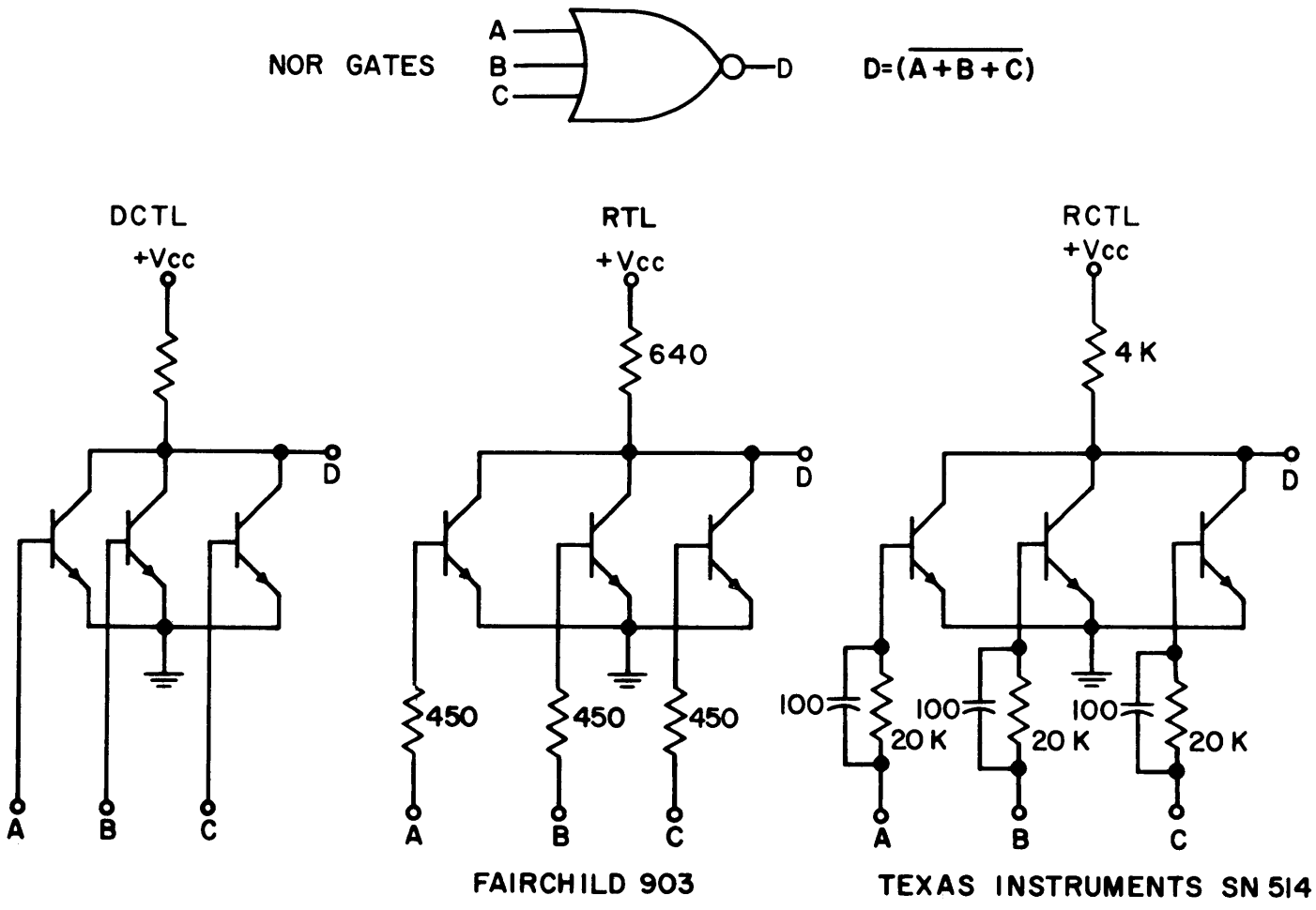


Figure 5-19

5.2.5 Resistor Capacitor Transistor Logic

A further modification to the basic DCTL configurations may be made by placing capacitors in parallel with the base input resistors of the RTL form to increase speed (see Figure 5-19). This improves the speed of operation, but makes the noise problem more serious because of capacitive coupling. This form of DCTL, called RCTL, is generally used where low power consumption is desired. It is not particularly amenable to monolithic integration because of the extensive use of capacitors.

5.2.6 Transistor-Transistor-Logic Forms

Transistor-Transistor-Logic (TTL) may be considered as a form of DTL with the input diode structure physically modified in integrated form. The AND gate in TTL employs a common base region for all of the input diode anodes. The basic TTL NAND circuit is shown in Figure 5-21.

This structure is particularly amenable to integrated circuit construction. TTL has the advantage of low parasitic capacity because of the isolation of the input diodes from the substrate and their smaller area requirements. TTL is also faster because of the active turn-on mechanism afforded by the transistor action. A potential disadvantage relating to lateral transistor action can develop if one emitter acts as a collector driven positive with respect to the base, while another emitter is held negative. Proper design can eliminate or at least minimize this difficulty by assuring that the resultant parasitic transistor gain is low.

Analytically, the operation of TTL is similar to DTL. Many specific design goals have generated a number of TTL variations, particularly with respect to internal coupling and output stage arrangements. It has been customized for speed, specific input impedance level, low power dissipation, high noise immunity, large fan-in and fan-out, etc. These usually require other tradeoffs. One form of TTL called high level TTL, for large fan-out capability, is shown in Figure 5-22.

5.2.7 Current Mode Logic Circuits

Current-Mode-Logic (CML) is another interesting and important circuit family developed to take advantage of monolithic integrated circuit fabrication capabilities. Figure 5-23 shows a version of the CML circuit. It is typified by small signal voltage swings and extremely short propagation time. The term "current steering" is sometimes applied to the circuit operation inasmuch as the input directs the current through one of the two legs of the differential amplifier input.

CML may be likened to a differential amplifier, whereas the logic types could be compared to single-ended amplifiers. The transition region in CML is sharply defined by a reference voltage (V_B). When the gate input transistor biases are below this reference, the current from the common emitter resistor flows through the reference transistor. The collector and emitter resistor ratios are chosen so that "On" transistors are not saturated. These values also assure that the output (D) of the emitter follower will swing symmetrically about the reference level (V_B). When any of the inputs move above the reference voltage, the current in the common emitter is transferred (steered) to the collector resistor in the input transistor circuit. This causes $\overline{D}$ to go negative and D to go positive.

The biases on the input transistors also may be selected so as to avoid saturation. As a result, the CML type is one of the fastest circuits available today in integrated circuit form, since the delays in storage times associated with saturation are avoided, as well as delays associated with transition to threshold levels.

DCTL NOISE IMMUNITY

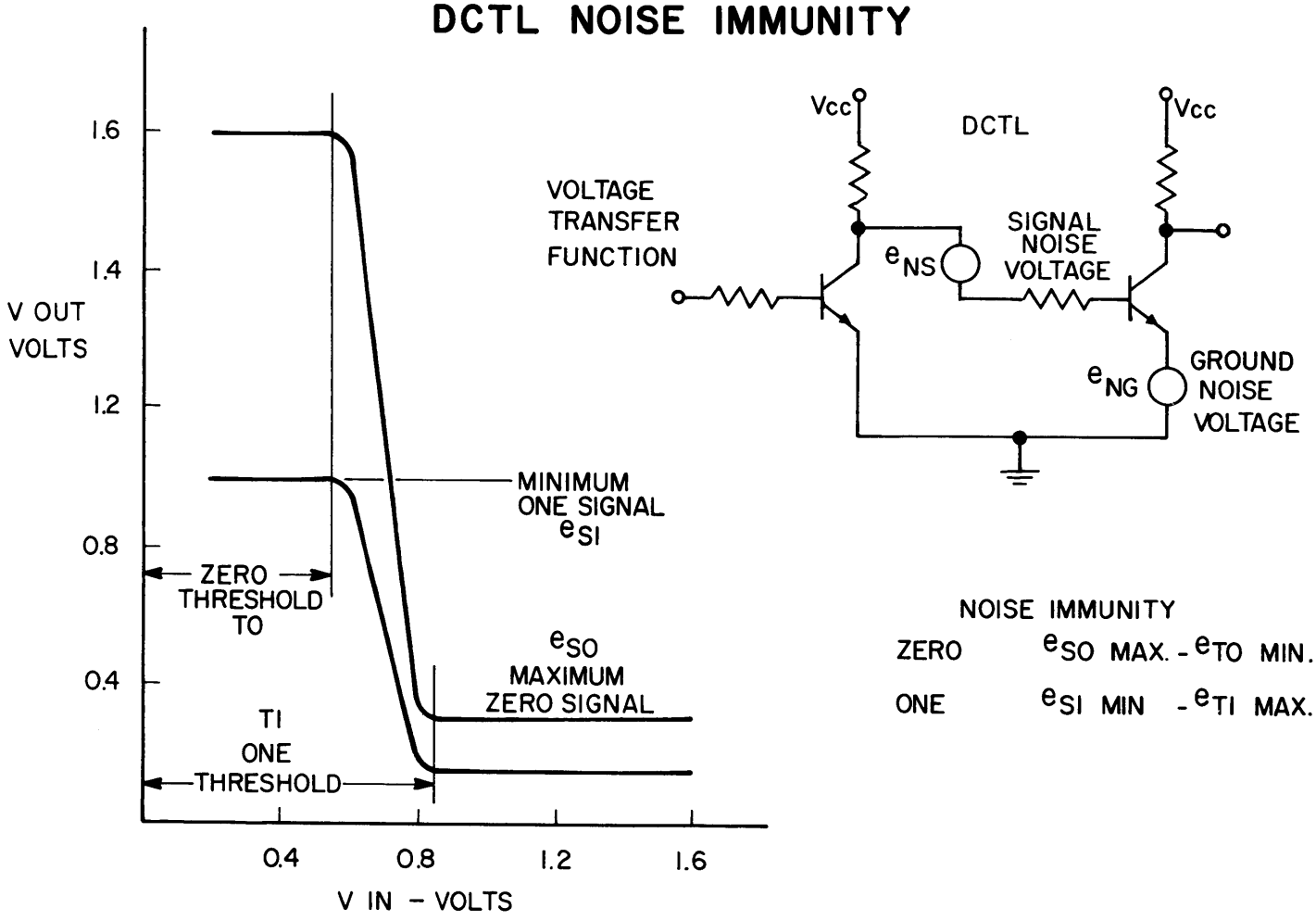


Figure 5-20

TRANSISTOR TRANSISTOR LOGIC (TTL)

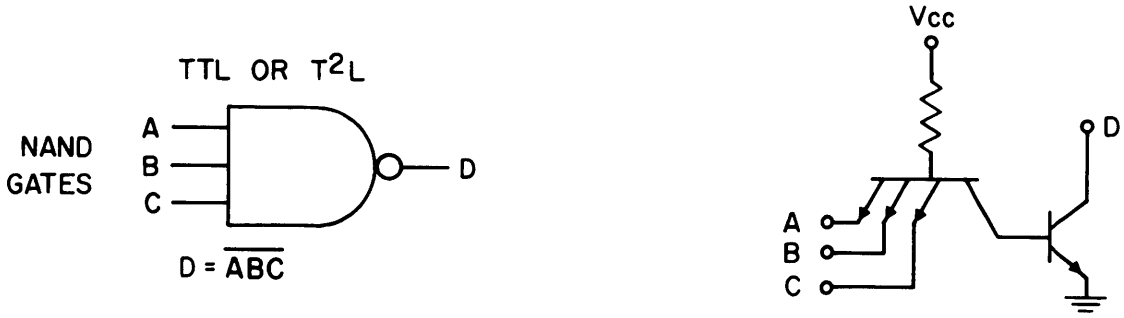


Figure 5-21

HIGH LEVEL TTL (HLT^{2}L)

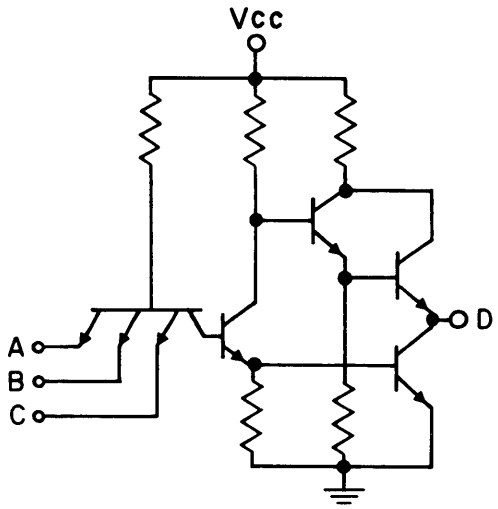
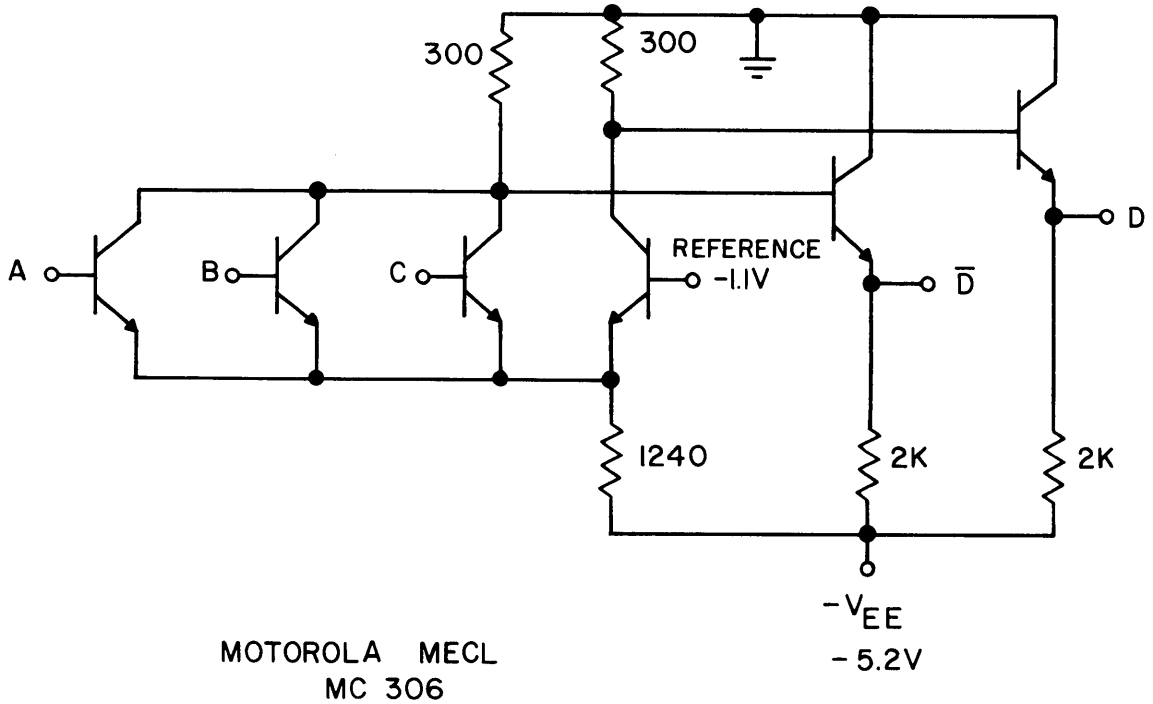


Figure 5-22

CURRENT MODE LOGIC (CML)

OR / NOR $D = A+B+C$ $\overline{D} = \overline{A}\,\overline{B}\,\overline{C}$



MOTOROLA MECL
MC 306

Figure 5-23

5.2.7 (Continued)

In addition to high speed, CML offers a high fan-out capability because of the emitter-follower output configuration. Its major disadvantages result from high power dissipation in the current source resistors and requirements for reference voltage supply which may be supplied by additional circuitry. Although closely matched transistor characteristics are necessary, this is not a major problem with monolithic integrated circuit construction.

At higher temperatures, the integrated transistors have increased saturation resistances which may cause problems. Operation in or near saturation will slow the circuit considerably.

5.2.8 Complementary Transistor Logic

The gates of the CTL circuit family consist of a complementary transistor emitter-coupled AND-OR gate and a NOR-OR gate with emitter-follower output, as shown in Figure 5-24 . The AND-OR gate employs complementary NPN and PNP transistors, to implement the AND function while a virtual "OR" may be obtained by connecting the output emitters together.

The input PNP transistors of the AND gate operate in the unsaturated mode. The output signal level is shifted according to the V_{BE} of the complementary transistors and less than unity gain is achieved. The NOR gate is used to perform this level restoration as well as to shape the rising and falling edges. (CTL circuits operate with several volts of signal swing so that signal edges as well as levels are important, and of course the emitter-follower AND gates have no edge setting capability). The NOR gate employs saturating NPN transistors at the input. In addition to their function of rereferencing and edge setting, the NOR gate serves the purpose of an inverter. Here again, the OR-INVERT function is performed by the gate, while the virtual OR is accomplished by connecting the emitters of the output transistors together. The AND gate has extremely short propagation delay. Hence, if several AND gate stages pressed the slower NOR, the net propagation delay is very small on the per-gate basis.

5.2.9 Future Digital Circuit Trends - MOS Logic

The use of MOS technology in fabricating NAND-NOR gates is expanding rapidly.

Presently there is no name to define this new logic, other than the usual term, MOS logic. Basic NAND and NOR gates are shown on Figure 5-25. The upper transistor, which acts as the load resistor, is simply another MOS transistor with the source shorted to the gate. This appears as an impedance of 50 Kohms to 100 Kohms and is adequate for relatively low speed logic. Many of these stages are directly coupled eliminating the need for resistors or capacitors on the chip. The inputs are high impedances with about 10 picofarads of capacity, effectively in parallel with the high MOST input resistance. The resulting time constants are thus large and produce upper limitations of the order of 100 KHz on devices presently being offered. Careful design may permit this speed to be increased to about 1 megahertz. Developmental work has been indicated that 10 MHz speeds may be feasible with complementary pairs.

Large voltage swings, of the order of 20 volts, result from the high impedance employed. These virtually eliminate the noise immunity problem. As a result, they are of great interest for use in business machines and other commercial equipments subject to large transient voltage spikes.

5.3.0 Flip-Flop Circuits

A flip-flop is a bistable element which can be set in either of its two stable states by proper input signals. The circuit will remain in this state until subsequent input signals cause the state to be

COMPLEMENTARY TRANSISTOR LOGIC (CTL)

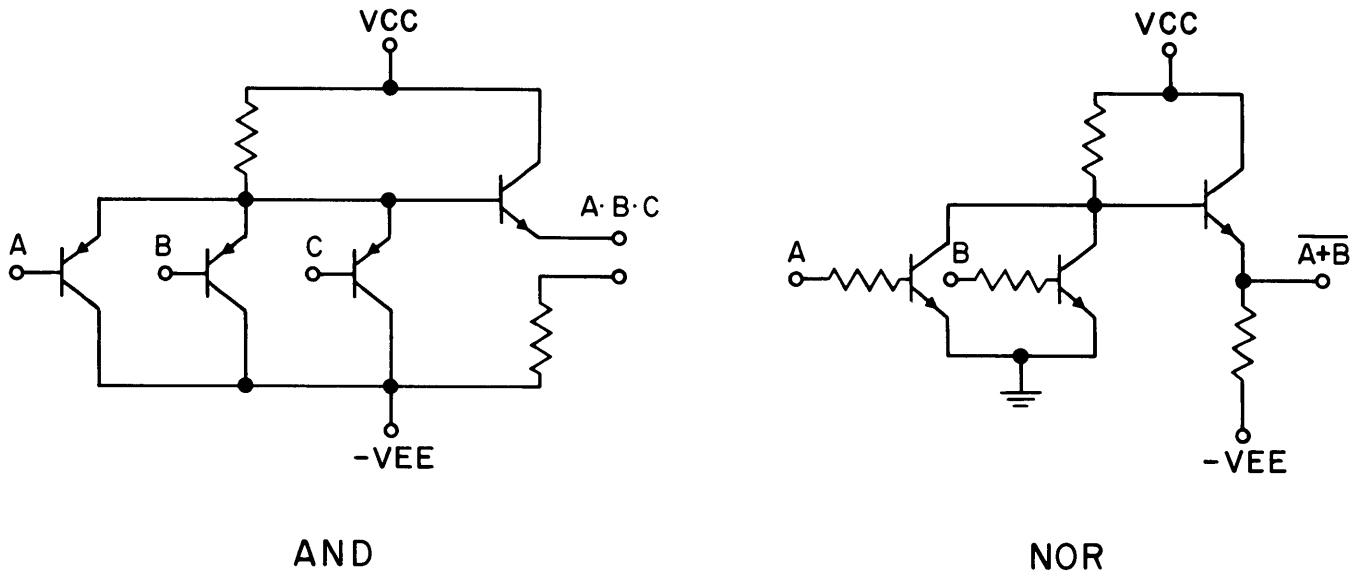


Figure 5-24

MOS GATES

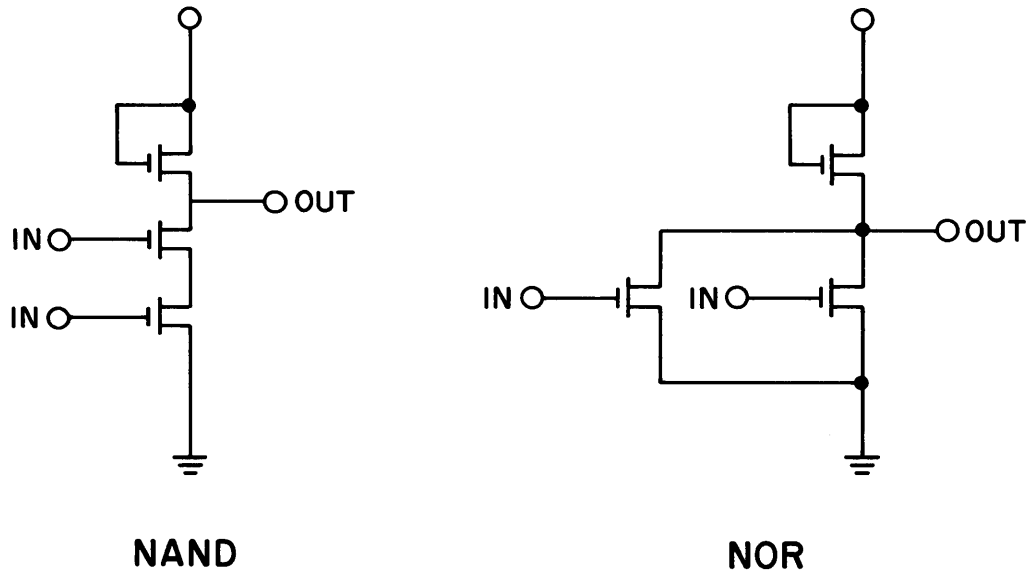


Figure 5-25

5.3.0 (Continued)

changed. The flip-flop thereby provides temporary storage of information. The many types of flip-flops in common use are delineated by the discipline of the input signals required to cause a state change.

Figure 5-26 shows a basic DTL flip-flop circuit. This flip-flop is simply two cross-connected NAND gates. It operates in such a way so that when one NAND gate is turned on, it turns the other NAND gate to the Off condition. The second NAND gate, in going off, holds the first NAND gate On. The gates will remain in this state until a signal reverses the conditions of Off and On. Only one input may be applied at any given time. Figure 5-27 shows in symbolic form the operation of an RS flip-flop, together with a Truth Table. It shows that when no input (R=S=0) is present, the state of the flip-flop is maintained. Either input can be used, initially, to set one or the other of the two possible states. Both inputs should not be applied at the same time since the resultant state of the circuit cannot be predicted, i.e., the resultant state is indeterminant.

If it was a common practice to build flip-flops out of combinations of NOR gates or NAND gates, then there would be no need for further discussion. It would only be necessary to apply the previously discussed logic circuits. However, as a result of refinements, a combination of logic functions is almost always grouped with a flip-flop. Hence, the flip-flop has become a basic circuit by itself.

5.3.1 RS Flip-Flops

One of the more complex forms of flip-flop circuits is an RS Binary Flip-Flop, as illustrated in Figure 5-28. This is called a binary element because it includes the function of sampling the input signal and storing the input temporarily while the setting action takes place. The binary element also blocks further input during the set period. The temporary storage is important because it holds the information being sent into the flip-flop while the other flip-flop circuits in the system are changing.

If temporary storage were not provided, the input signal, which originates in another flip-flop, would change during the setting period, thus causing the wrong value to be entered. In general, if simple flip-flops are used, it takes two flip-flops to store and handle one bit of information. One binary element alone can handle one bit of information. The Truth Table in Figure 5-29 shows that either input going to logic 0 sets the element to one of the two states, but both inputs must not go to logic 0 simultaneously. There are two sets of inputs in this binary element. One set is controlled by the clock. The direct inputs are generally used for clearing the flip-flop register or for entering some desired preset condition. Temporary storage is provided by the clock pulse capacitors. When the clock pulse goes positive, there will be 0 charge stored in these capacitors (if both S_c and R_c are positive). If either S_c or R_c is negative, the corresponding capacitor will be charged negatively through the resistor and charging diode. When the clock pulse goes negative, the signal input end of the capacitor will be driven more negative than the setting signal. This negative signal will be coupled to the flip-flop through the two biased diodes, delivering a negative signal which will turn off that side of the flip-flop.

The triggering action occurs during the fall time of the clock pulse. The charging diodes are back-biased when the capacitor drive is below the signal input level. Thus, any further input is shut off during the clock fall time. The energy to turn off the flip-flop is stored in the capacitor during the time when the input is blocked.

DTL RS FLIP-FLOP

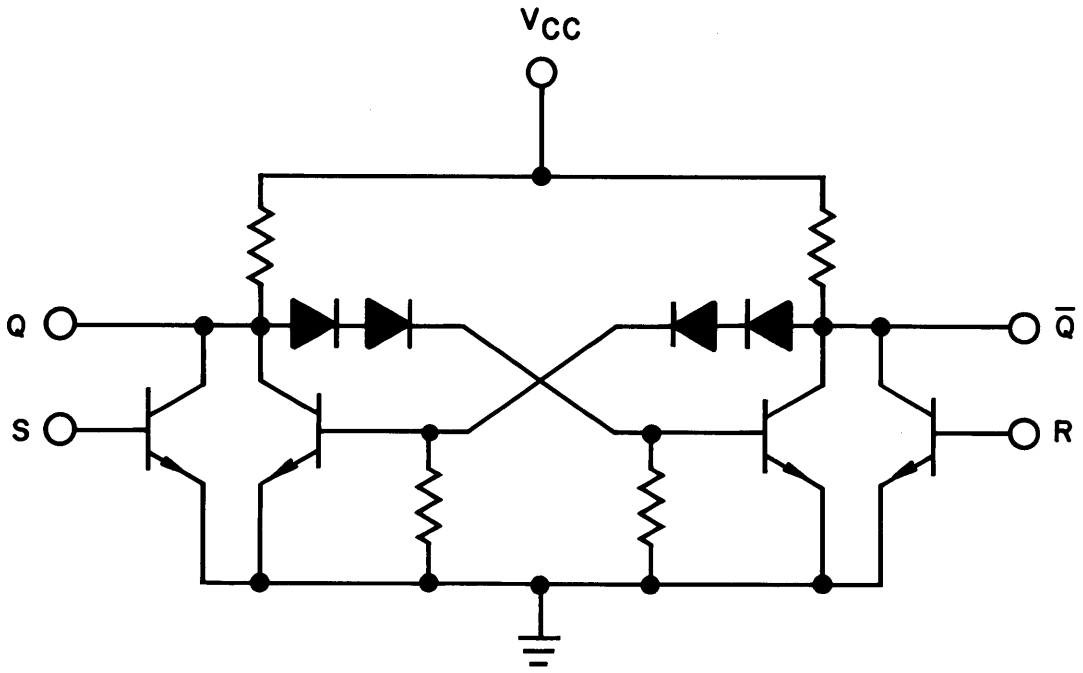
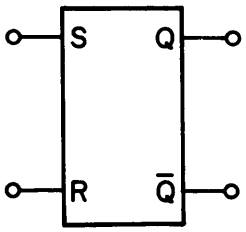


Figure 5-26

RS FLIP-FLOP

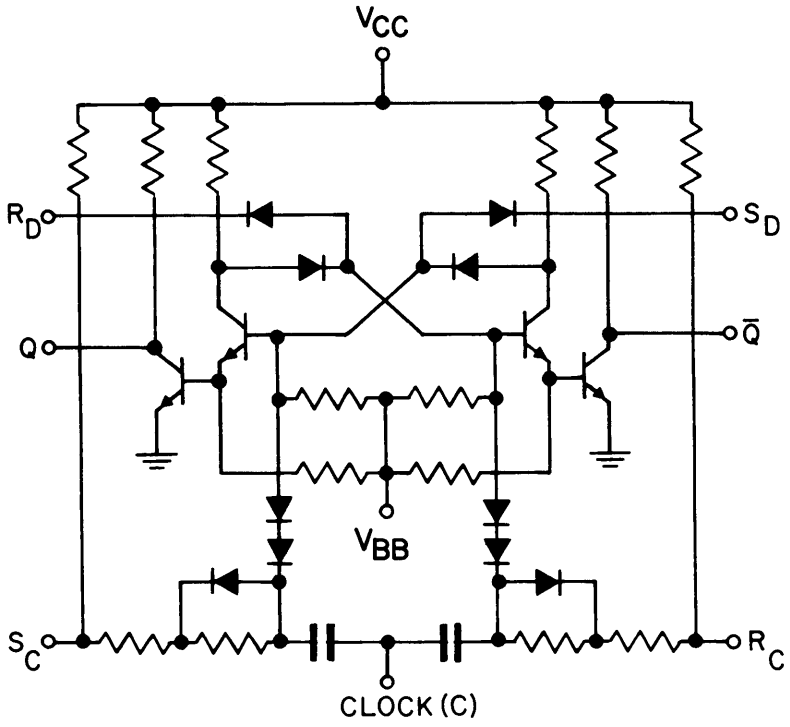


TRUTH TABLE

S	R	Q	$\bar{Q}$
0	0	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
1	1	INDETERMINATE	

Figure 5-27

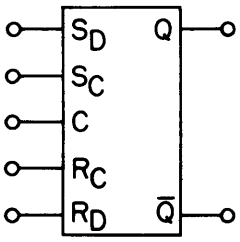
DTL RS BINARY ELEMENT



SIGNETICS SE 124

Figure 5-28

RS BINARY ELEMENT LOGIC SYMBOL



SINGLE-PHASE RS FLIP FLOP
WITH DIODE-CAPACITOR STEERED
CLOCK.

TRUTH TABLE

DIRECT SET-RESET			
S_D	R_D	Q	$\overline{Q}$
1	1	Qn	$\overline{Qn}$
0	1	1	0
1	0	0	1
0	0	IND.	

CLOCKED SET-RESET			
S_C	R_C	Q	$\overline{Q}$
1	1	Qn	$\overline{Qn}$
0	1	1	0
1	0	0	1
0	0	IND.	

IND. = INDETERMINATE

Figure 5-29

5.3.1 (Continued)

This action is called a "steered" circuit. It is a relatively simple circuit for the combination of functions it provides: Clocking, temporary storage and input blocking.

This type of circuit will accept a wide range of logic and trigger levels, while its complete buffering provides isolation between the input switching and outputs. It has the same margins as DTL, since the switching uses two DTL NAND gates. Input steering also provides 0 setting and Hold time. The capacitive triggering allows higher speeds impossible with DC techniques. However, clock pulse amplitude should be controlled to be high enough to provide a good signal, but not so high so that a low amplitude logic 1 input signal is exceeded by sufficient margin to charge the capacitor.

5.3.2 JK Flip-Flop

The JK flip-flop is shown in Figure 5-30. The JK flip-flop is a binary element with the additional feature of eliminating any forbidden or indeterminant conditions. The outputs are gated with the input so that when two logic 0 signals occur, one of the signals is blocked. Since the inverse is fed back into the input, the logic 1 signal which is not blocked changes the state of the flip-flop. This is illustrated in the Truth Table, Figure 5-31, which shows that two logic 0 signals cause the flip-flop to assume the inverse condition of two logic 1 signals.

Figure 5-32 illustrates the JK binary element in block diagram form which uses 5 NOR and 4 AND gates to form two flip-flops in the steering elements. The "master" flip-flop stores the input information when the clock voltage becomes sufficiently positive to turn on the AND gate. When the clock is turned off, the "master" flip-flop transfers the information to the output flip-flop.

5.4 Logic Subsystems

The various logic elements discussed, such as NAND/NOR gates and flip-flops, are actually building blocks which are interconnected to form more complex logic functions. These are sometimes called subsystems which, in integrated form, are often included within a single package. Some of the more commonly used subsystems are discussed here.

5.4.1 Binary Counters

A flip-flop element with gating differentation and delay may be connected directly to a second flip-flop for counting purposes. As illustrated in Figure 5-33, the state of flip-flop No. 1 changes whenever the input comes on. The input thus goes through 2 complete cycles for each one of the flip-flops. Thus flip-flop No. 2 and each succeeding flip-flop goes through one complete cycle for each two traversed by its input driving flip-flop. Figure 5-34, indicates the action of a series of four of these flip-flops connected to form a counter. The effect of each flip-flop changing from "OFF" to "ON" is indicated by the table which lists the state of the output. By giving each flip-flop a "weighted" value and noting their states, the total count will be indicated in binary form. Upon reaching the maximum number determined by the length of the chain, the count will return to zero in the next count to start the cycle again. This type of counter is called an up counter. By reversing the connections, the count readout in Figure 5-34 will proceed from 15 to 0. This type is called a down counter.

5.4.2 Gating

One repeated system requirement is the transfer of information from one place to another. The process, called gating, is illustrated in Figure 5-35. When the two AND gates are triggered by a signal at T, the logic levels of flip-flop No. 1 are fed into flip-flop No. 2 where the identical levels are produced. This gating action is useful for transferring numbers from one set of registers to another.

JK BINARY ELEMENT

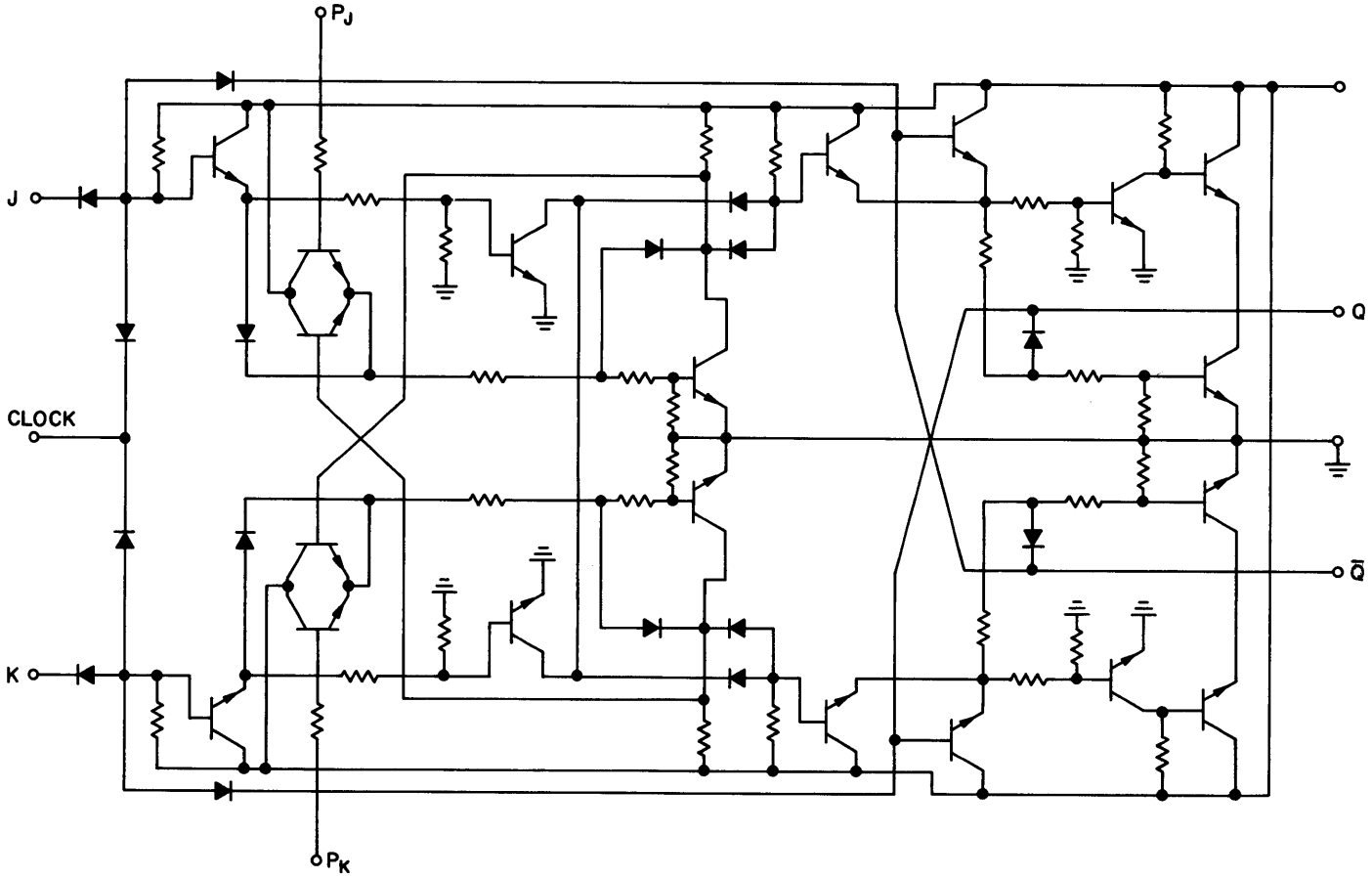
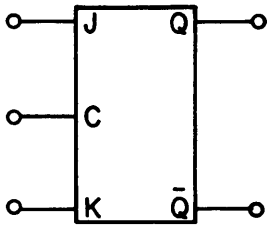


Figure 5-30

JK BINARY LOGIC



SINGLE-PHASE JK FLIP FLOP WITH TRANSISTOR CHARGE STORAGE.

TRUTH TABLE

J	K	Q	$\bar{Q}$
1	1	Qn	$\bar{Qn}$
1	0	1	0
0	1	0	1
0	0	$\bar{Qn}$	Qn

Figure 5-31

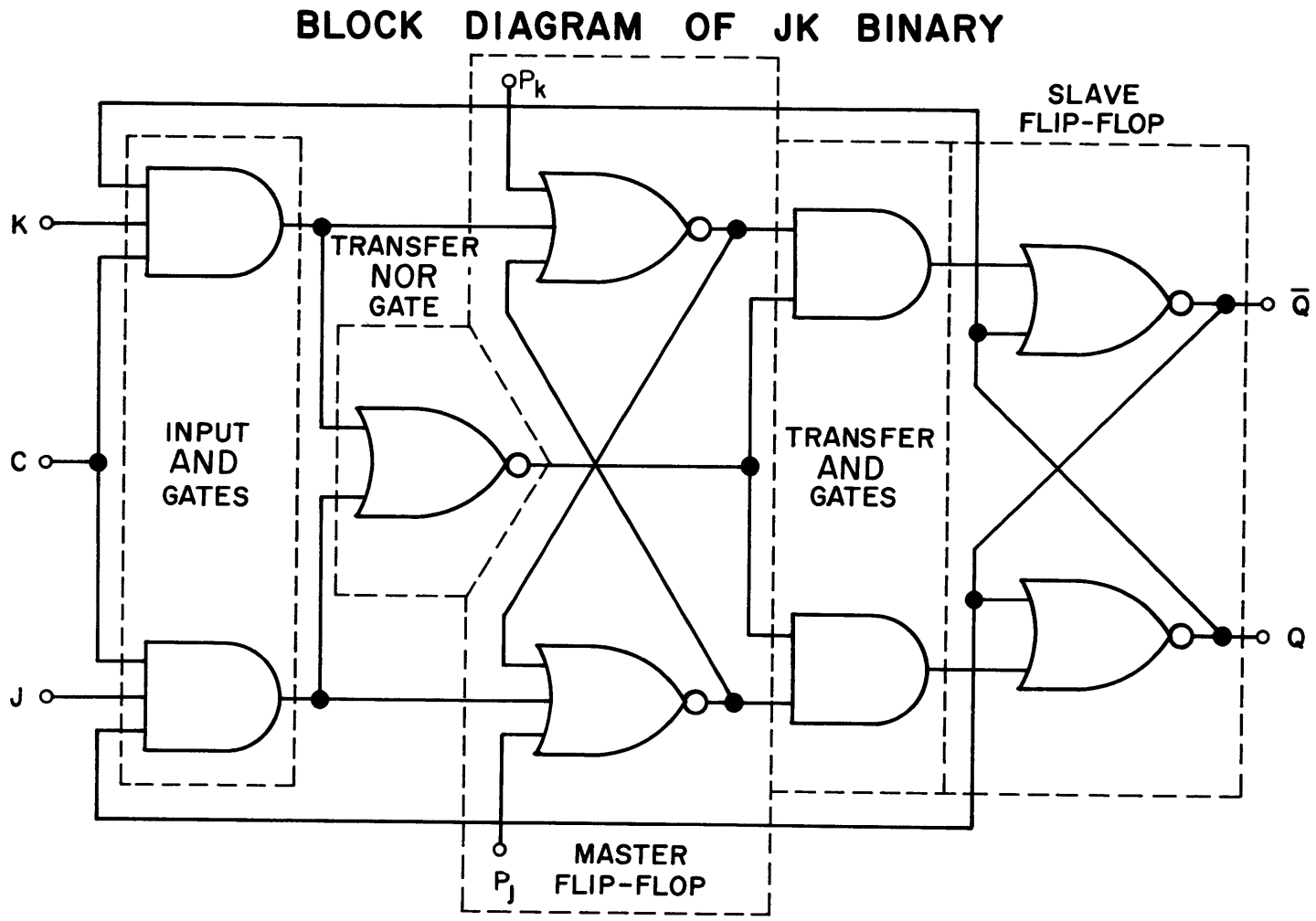


Figure 5-32

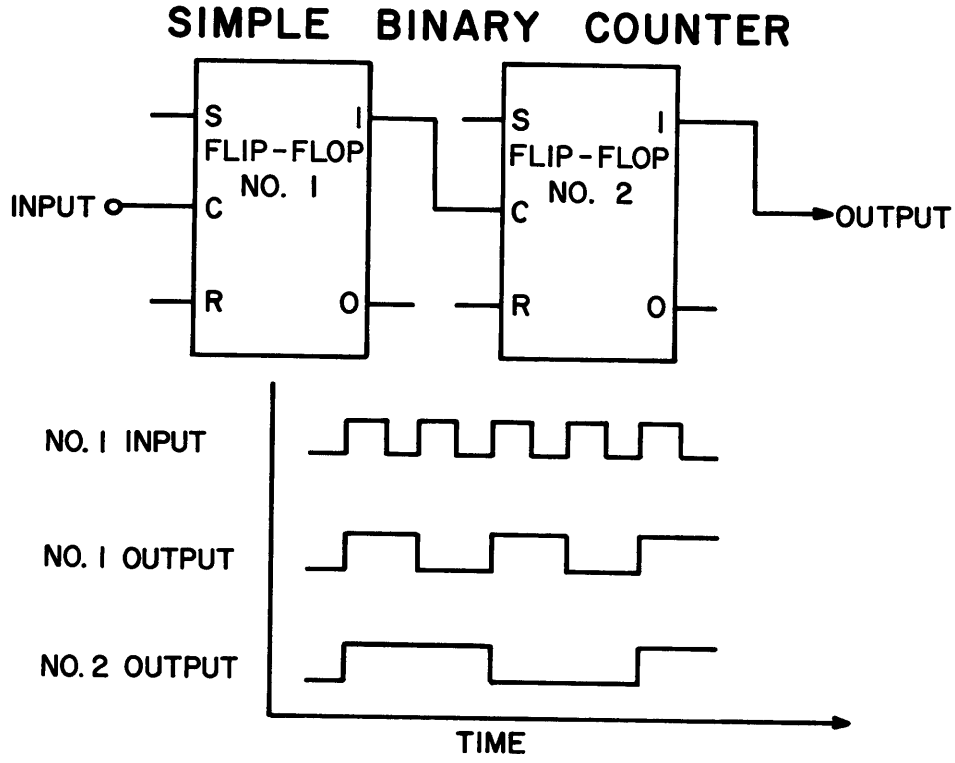


Figure 5-33

BINARY COUNTER

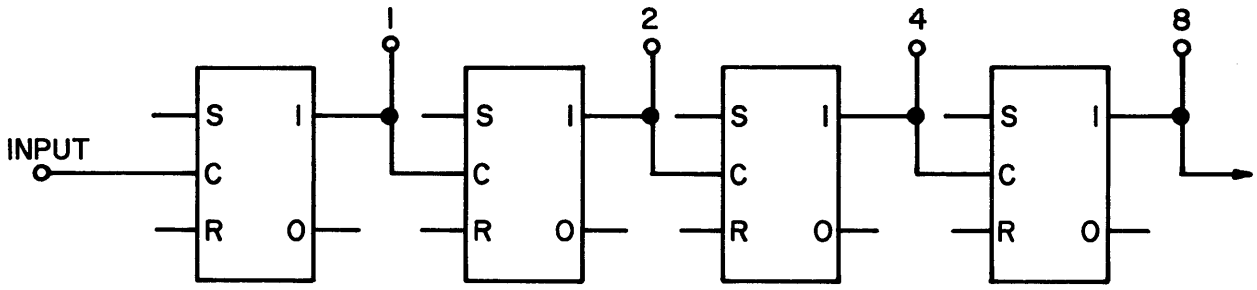


TABLE INDICATING STATE OF OUTPUT

0 = ON

1 = OFF

WEIGHT				COUNT	DECIMAL EQUIVALENT
8	4	2	1		
0	0	0	0		0
0	0	0	1		1
0	0	1	0		2
0	0	1	1		3
0	1	0	0		4
0	1	0	1		5
0	1	1	0		6
0	1	1	1		7
1	0	0	0		8
1	0	0	1		9
1	0	1	0		10
1	0	1	1		11
1	1	0	0		12
1	1	0	1		13
1	1	1	0		14
1	1	1	1		15

Figure 5-34

GATING FUNCTION

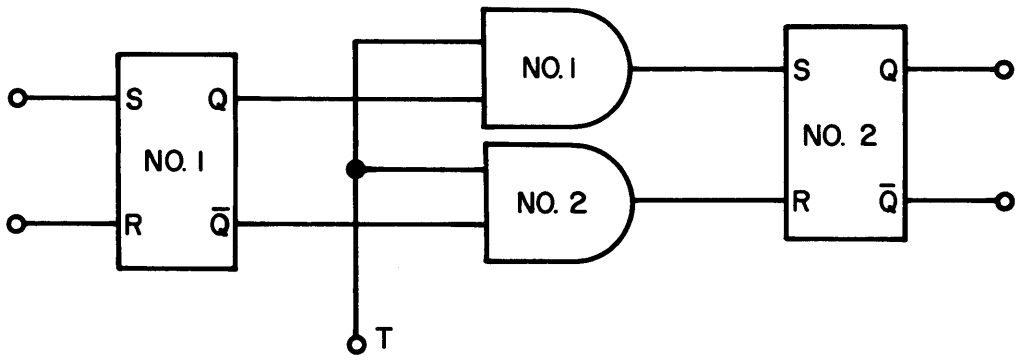


Figure 5-35

5.4.3 Comparators

Frequently, it is necessary to determine whether the digital information in one place is the same as in another. A simple comparator circuit used to determine whether two flip-flops are in the same state is shown in Figure 5-36. An output through the OR gate occurs only when both flip-flops are in the same state. In practice, comparators are used to compare two registers and, when this occurs, signal for additional operations.

5.4.4 Binary to Decimal Conversion

Since the decimal system is so widely used in our society, counters which indicate their output in decimal form are highly desirable. By adding control or steering circuitry to a combination of 4 flip-flops as shown in Figure 5-34, it can be caused to recycle on the tenth rather than the sixteenth count. This system, called Binary-Coded-Decimals (BCD), requires a set of 4 flip-flops and associated circuitry for each decade. Decade counters in a single integrated circuit package are now available.

5.4.5 Half-Adders

A "half-adder" is an example of a group of logic circuits which will add two binary bits, A and B, according to the rules given in Appendix A. Block diagrams of two half-adders are shown in Figure 5-37 with their truth table.

5.4.6 Parallel-Serial Conversion

When data must be transmitted between sections of a computer or two different computers, a method must be used to exchange the numerical information of the flip-flops. Two digital data transmission methods are parallel-to-serial conversion and serial-to-parallel conversion. An example of parallel-to-serial conversion is illustrated in Figure 5-38. The input timing signal A is only on during the first period and the time signal B is on during the second time period, etc. Thus, with the gating arrangement as illustrated, the parallel flip-flop information is transferred to a serial time arrangement to transmitting a single line. A similar arrangement exists for the conversion of the serial to parallel information. Shift registers, as discussed later, are widely used to simplify these conversions.

5.4.7 Shift Registers

A subsystem operation that is commonly required in digital systems is the shifting of data within a register to the right or to the left. Typical applications include: shift counters, timing pulse distributors and arithmetic operations. A shift register consists of the memory elements required to hold the multibit information and control circuitry to coordinate the actions of the memory elements.

The design includes three separate parts: the farthest left, farthest right and the intermediary stage which can be repeated as many times as necessary to fill out the register. Each stage consisting of two NOR Gates feeds a flip-flop. Figure 5-39 shows 2 two-phase shift registers together with the timing waveforms that show the shifts.

5.5 Interface Circuitry

In many digital systems, one of the major problems is interfacing between the various sections of the system. Interface circuits may be required between different logic families, between logic and memory units or between these and other peripheral sections. Some of the more common circuit requirements are line drivers, sense amplifiers, core drivers, etc. Circuits of this type are not always amenable to integration, requiring custom design and low volume production. However, several types are now available as standard items capable of meeting a number of these different requirements.

5.5.1 Logic Interfaces

To gain greater system flexibility or economy, it is frequently desirable to translate from one form of logic to another (saturated to

COMPARATOR FUNCTION

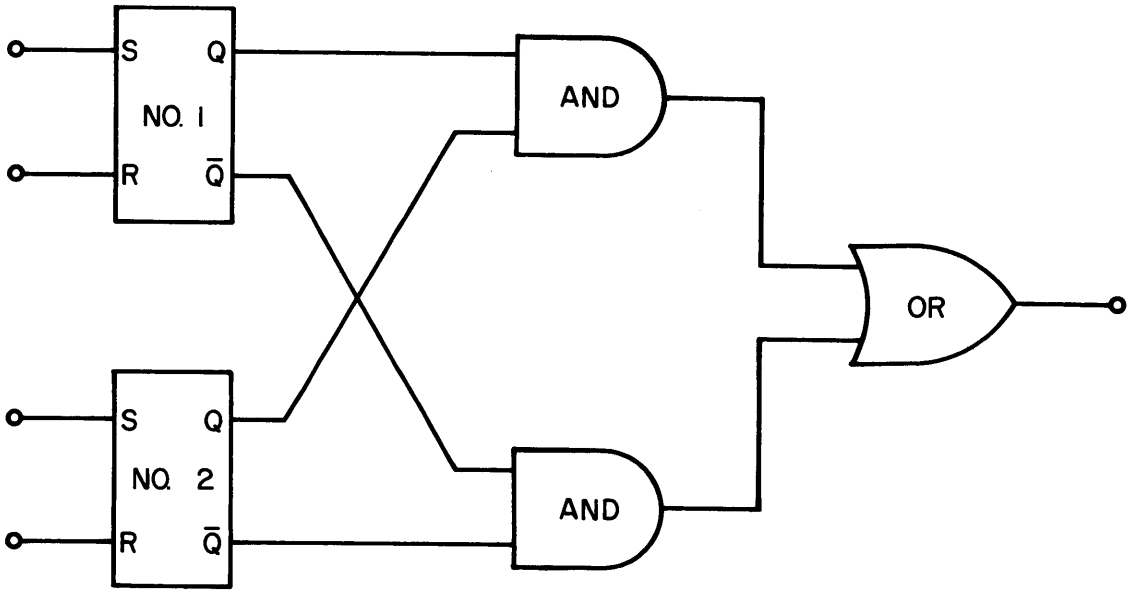
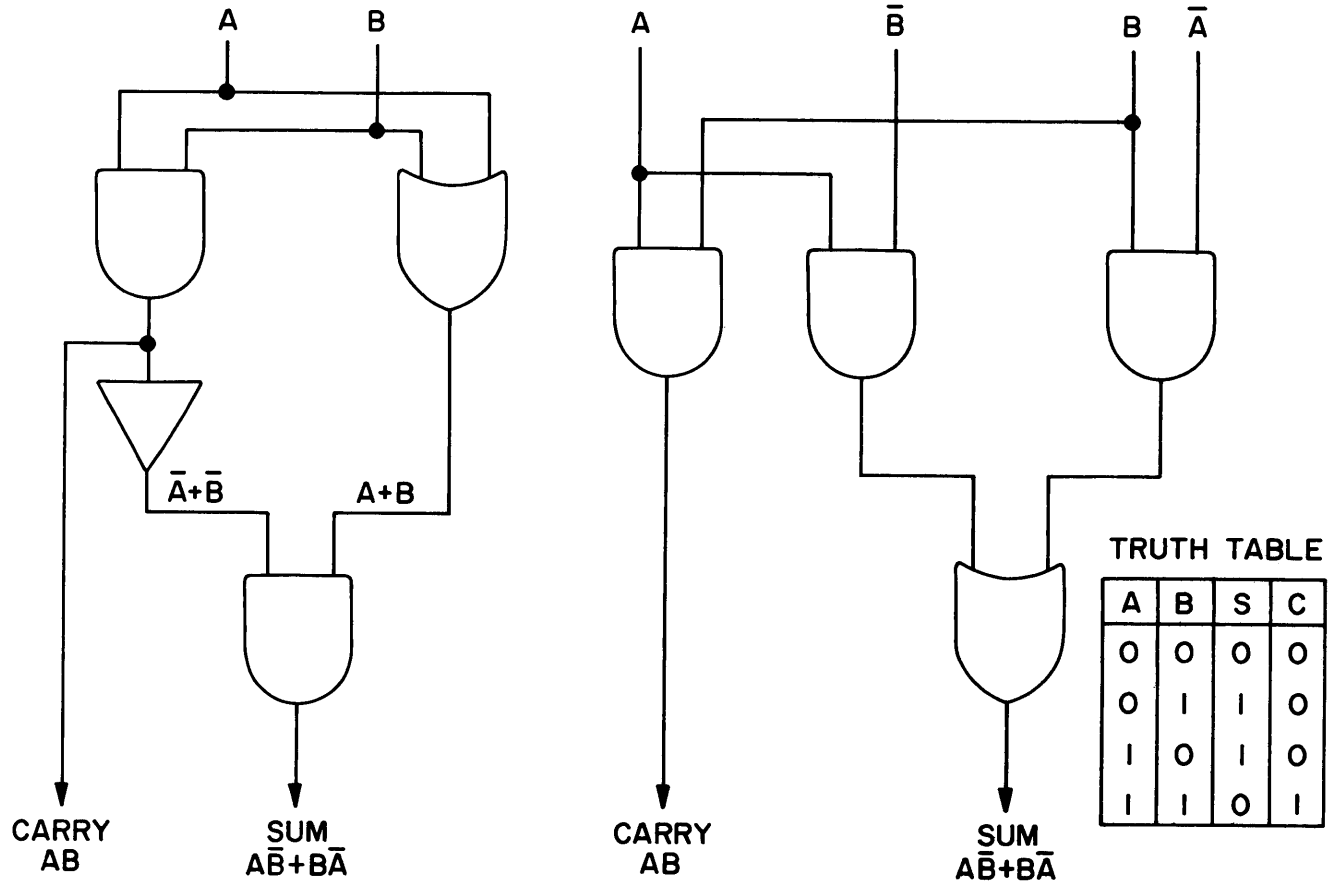


Figure 5-36

BASIC FORMS FOR HALF-ADDER DESIGNS



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 5-37

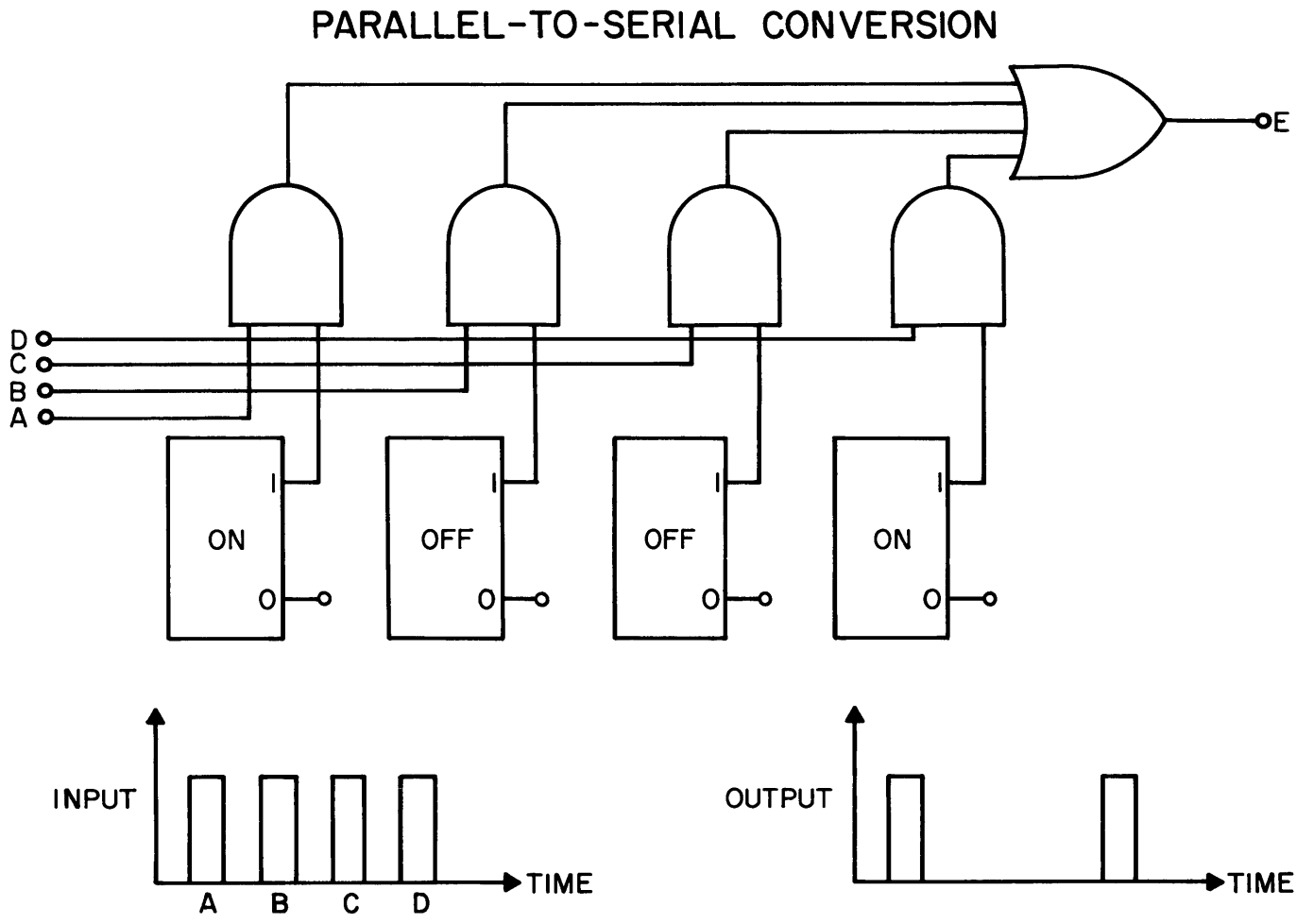

PARALLEL-TO-SERIAL CONVERSION
E
D
C
B
A
I
O
ON
OFF
OFF
ON
INPUT
A
B
C
D
TIME
OUTPUT
TIME

Figure 5-38

TWO-PHASE SHIFT REGISTER

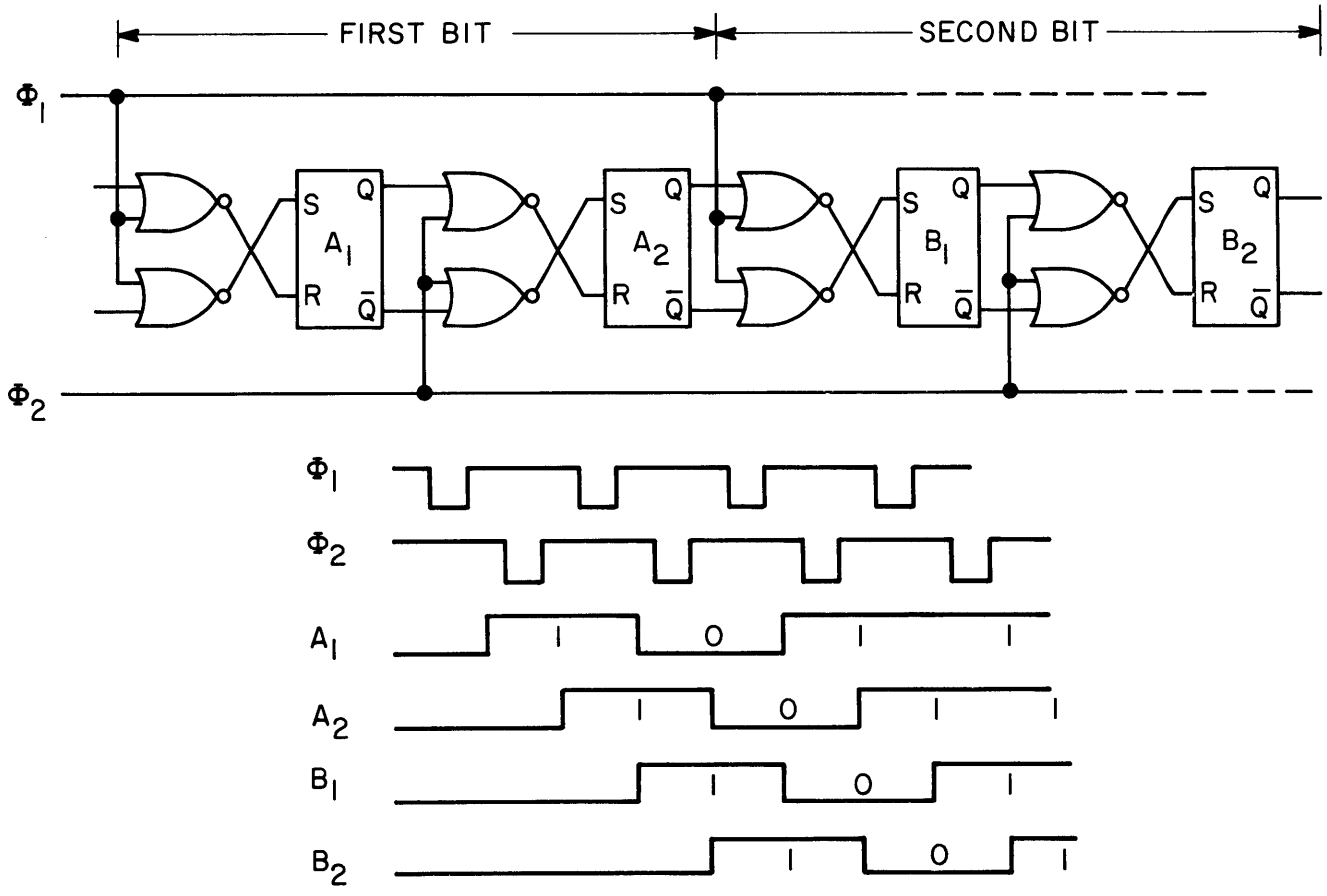


Figure 5-39

5.5.1 (Continued)

nonsaturated or vice versa). Generally, only a small percentage of a system might require the highest speed logic which is very expensive. Substantial economy can be achieved by using the different logic families and interfacing between them. Figure 5-40 illustrates an interface circuit which translates the voltage levels from a saturated transistor logic stage, such as RTL, DCTL, DTL, or T^2L, to the logic levels required by some forms of CML. Values of the individual resistors depend on the power supply voltages of the two logic systems to be connected.

5.5.2 Line Drivers

Another interface circuitry requirement is translation from logic switching to load impedance levels. Typical of this requirement is the high capacitive load driving capability required by transmission and clock lines. This type of circuit must be compatible with the input logic levels and be capable of driving the loads at their required levels. Frequently, only minor adjustment of some of the standard high fan-out logic circuitry can be used for this purpose.

5.5.3 Sense Amplifiers

Core or thin-film memory systems provide another example of an interface requirement. Circuits are required to translate the low-level memory signals outputs to normal logic levels. This type of circuit combines gain and level shifting with the comparator function shown in Figure 5-36. Such an amplifier may be used with a magnetic core memory where it can be adjusted for the rejection of signals below a preset voltage level. Available circuits of this type allow threshold level adjustment to set of input signals rejection.

5.6 Counters

Counters are of such great importance and available in wide variety as to deserve separate consideration. Many counters are made easily with integrated circuits flip-flop elements. The choice of a particular form is based on factors including speed, economy, count length and convenience. As previously shown, the binary flip-flop is the basic element whether used directly or arranged for binary or BCD counting. The addition of control signals produces the variety and extends the usefulness of counters.

5.6.1 Ripple Counters

Ripple counters employ triggered flip-flops in the asynchronous mode to effectuate counting. The output of each stage in a ripple counter is connected to the clock input of the following stages (Figure 5-41). Using JK binary elements, this type of counter may be extended as a chain to achieve any count length desired. Decade counters which cycle through ten counts and repeat are most common. This type of counter can be set up to skip numbers if desired. The primary advantages of this type of counter is its inherent simplicity and economy. The obvious limitation is the propagation time through the counter which is the sum of the delays through each flip-flop.

5.6.2 Simultaneous Carry Counters

The propagation delay may be reduced by using a simultaneous carry counter (Figure 5-42) in which all flip-flops are simultaneously clocked; logic gate bypasses cause all of the scheduled flip-flops to change simultaneously with the trailing edge of the clock pulse. The propagation time of this counter is the time required for flip-flop change of state to propagate through the gates.

5.6.3 Johnson Counters

The Johnson counter is a simple form of counter using a combination of JK flip-flops and shift register configuration. Illustrated in Figure 5-43, it is a shift register with the inverse output of the last stage connected to both the J and K inputs of the first stage. This counter will cycle through 2^N-1 states (N equals the number of stages). It is desirable to include circuitry to provide an initial clearing to avoid getting into the state with all flip-flops set since this counter will not automatically reset on recycle.

LOGIC LEVEL TRANSLATOR
(SATURATED TO UNSATURATED)

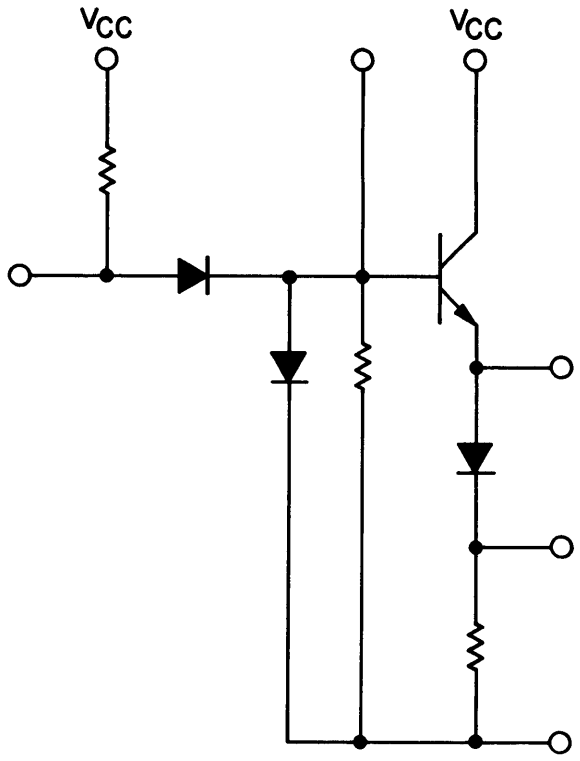


Figure 5-40

BINARY RIPPLE COUNTER

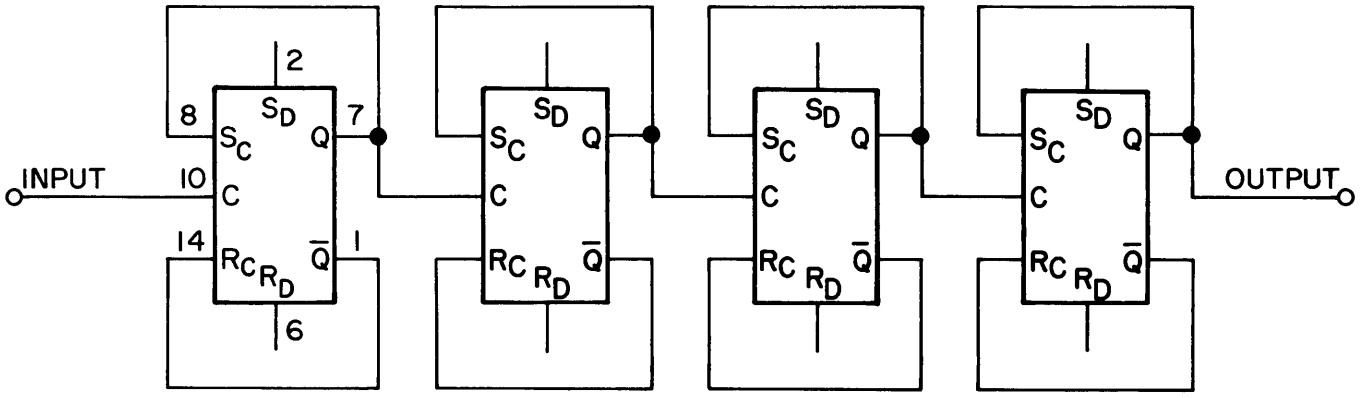


Figure 5-41

SIMULTANEOUS CARRY COUNTER SERIAL LOGIC

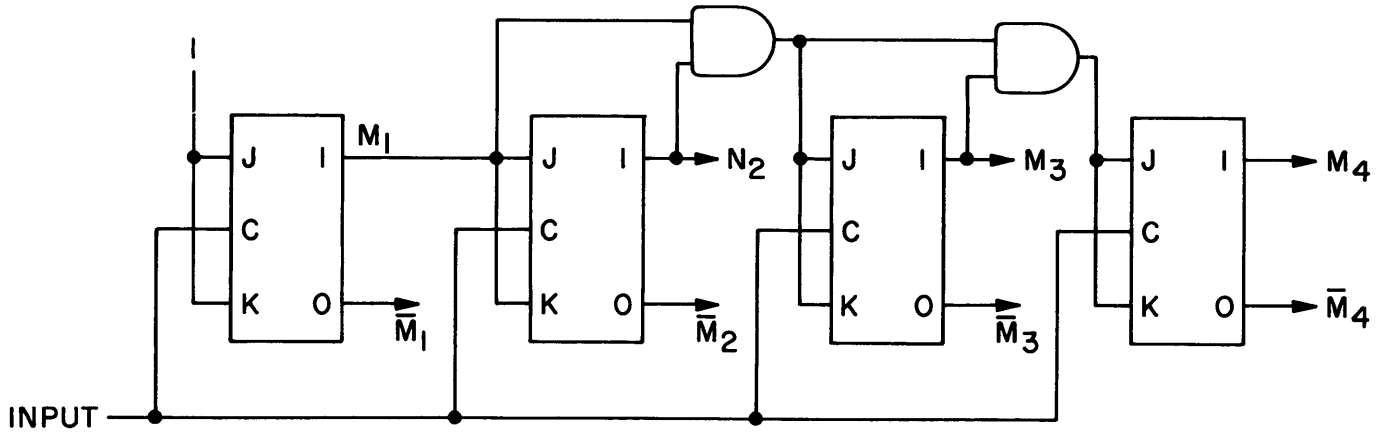


Figure 5-42

JOHNSON COUNTER

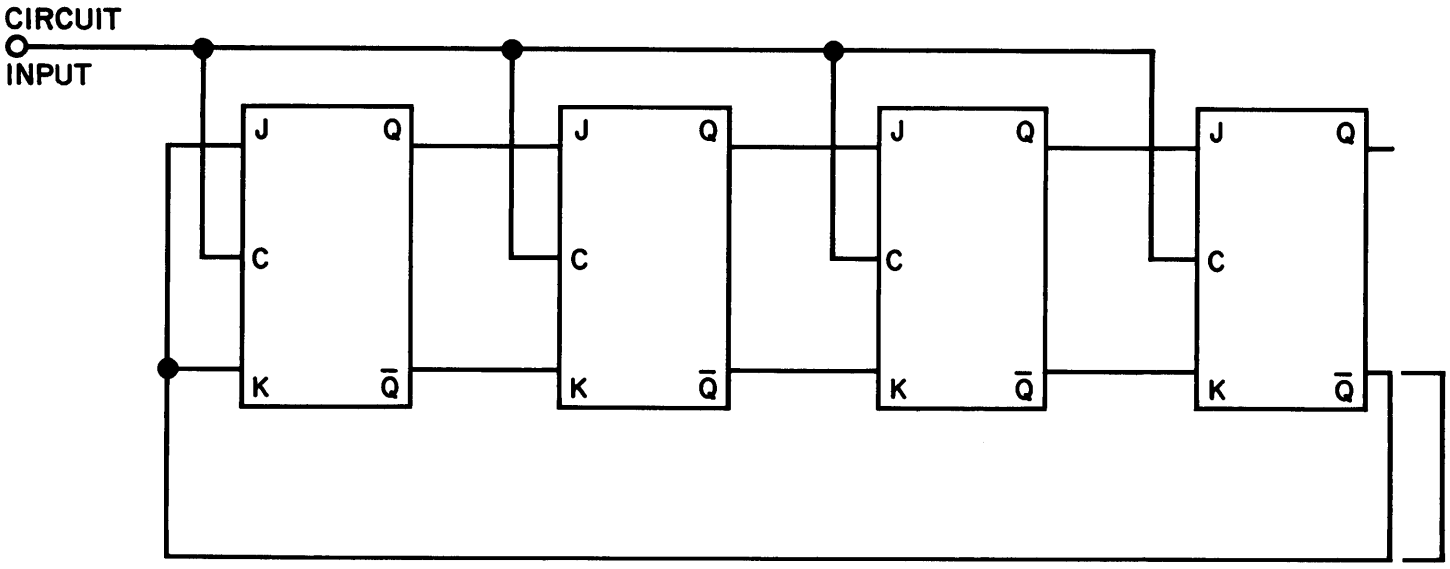


Figure 5-43

5.6.4 Shift Counters

A class of counters constructed with shift register stages only are referred to as shift counters. The most basic form is a shift register connected in a ring with one stage set to one and all other stages set to zero. When the register is shifted, the marker - (1) circulates around the ring. The advantage is that it requires no decoding. Figure 5-44 indicates the arrangement of a two stage counter. This particular two stage counter is sometimes used in the first stages of a high speed counter because maximum rate at which either stage must cycle is only one cycle for each four counts.

5.7 Clock Signal Considerations

Reliable system operation depends on proper timing and wave shape of the control or "clock" signal. In most systems, there will be several clock drivers. Each driver supplies proper signal and the relative timing between driver outputs must be maintained within certain tolerance limits.

5.7.1 Clock Waveform

The important parameters of a clock waveform are pulse-width, fall-time, and the time between pulses. The sum of these individual times is the frequency of the clock.

The pulse fall time is important because it establishes when the output stage of a flip-flop element is set. Typical DTL flip-flops might require fall-time less than 100 nanoseconds, but not faster than about 20 nanoseconds. This is because the input stage capacitor must discharge into the output flip-flop at the proper rate to set the output. Another reason why fall time must be controlled is that the precise time in which the clock signal transfers a setting from the input to the output is indeterminant within the transition region.

5.7.2 Clock Skew

If the clock falls very slowly, it will spend a long time in the transition region reducing the tolerance available for clock "skew". This is a variation in the relative timing between the various clock drivers in a system. "Skew" is measured from the falling edge of the clock signal since this is the critical time in which the inputs of the flip-flop are shut off and the new value set in the output stage. The maximum "skew" that may be tolerated is a determined minimum response time of the flip-flop. The requirement is that the last clock to fall must be down before the output of the first flip-flop to change rises.

5.7.3 Clock Jitter

Clock jitter is a variation in the period of the clock which may occur due to instability of the master oscillator or time base generator. The net effect of clock jitter is to reduce the down (or off) time of the clock-which should be taken into consideration as a logic design limit.

5.8 Digital System Design Considerations

Material to be covered under system design will include general information as to requirements of a digital system, a brief organizational approach, counting circuits, shift registers, clocking considerations and system speed considerations. A typical digital system receives data, operates on it and provides some form of output. This simplified concept of a digital system is illustrated in Figure 5-45. Thus, the functions of memory data manipulation and sequential control are found within the system.

Typically, the design steps involved in any system design are as follows:

1. Definition of task
2. Develop flow chart
3. Define the major register and control elements in the form of an equipment form diagram

TWO STAGE CYCLIC COUNTER

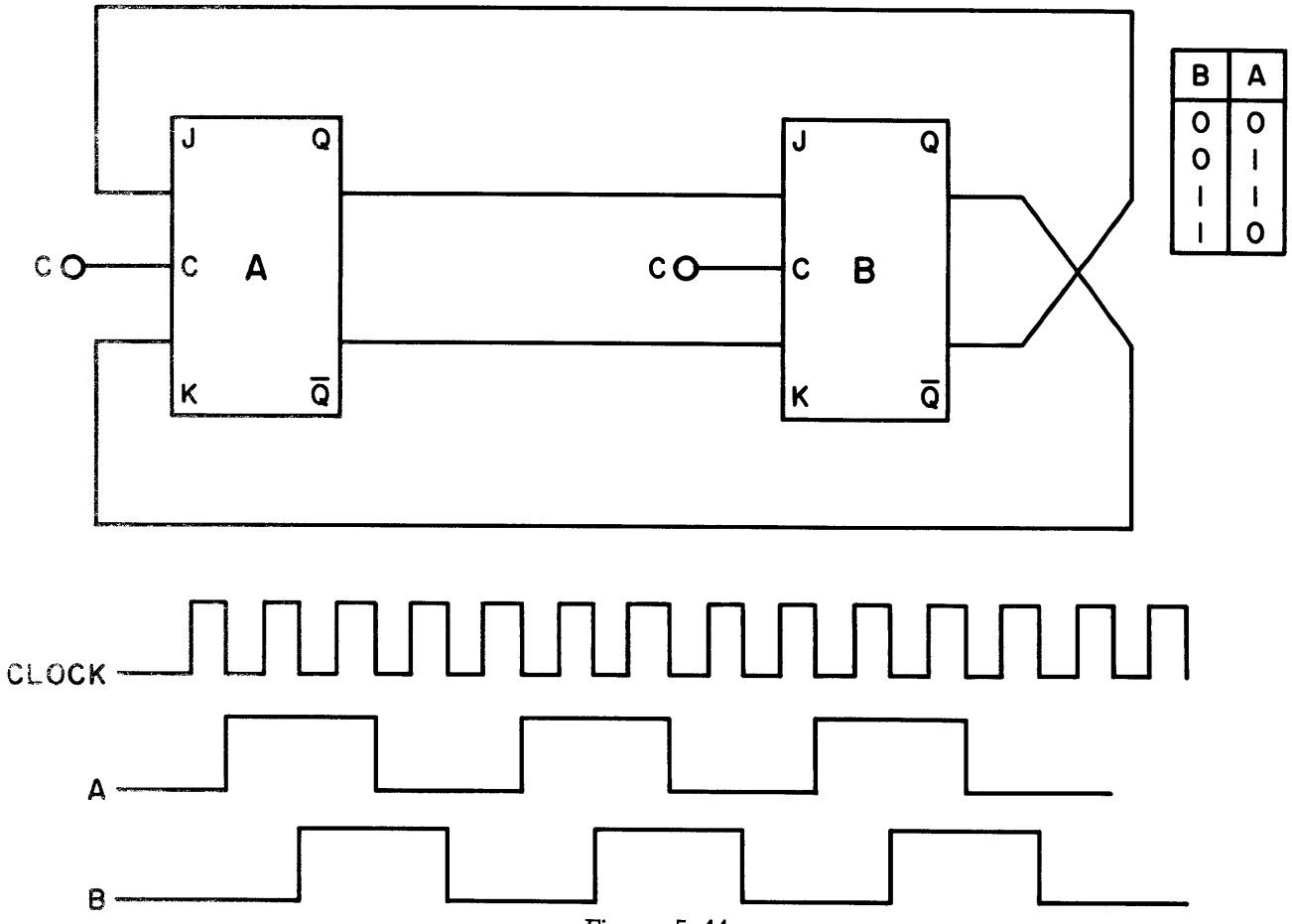


Figure 5-44

DIGITAL SYSTEM SHOWING SUBSYSTEM LEVEL OF ORGANIZATION

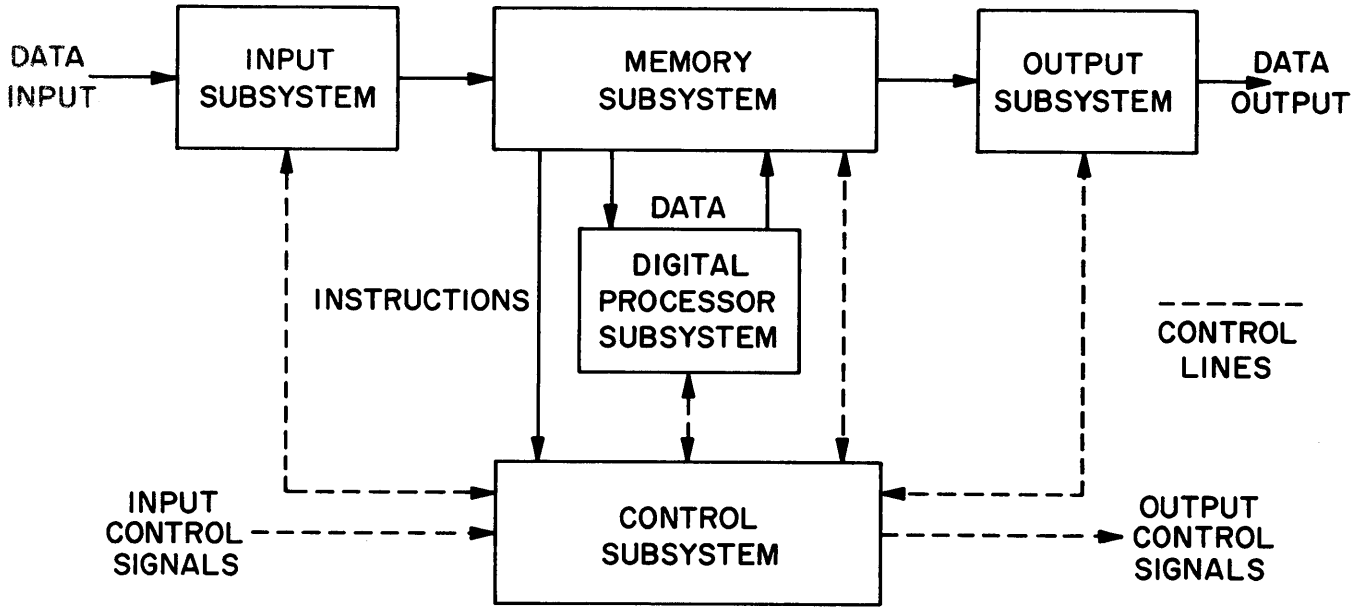


Figure 5-45

5.8 (Continued)

4. Select a control scheme
5. Select a circuit system
6. Write the detailed logic equations
7. Convert equations into implemented forms in those instances where the original form does not correctly match the circuit elements used
8. Check time in the critical areas
9. Prepare a logic schematic.

This logical sequence of steps can seldom be accomplished serially since specific problems in one area frequently require modifications of previous steps. Thus, the design process involves several iterations through the design cycle.

Typically, the design steps involved in any system design are as follows:

5.8.1 Definition of Task

This portion of the problem is the key to the eventual cost and performance of the finished system. The task definition must be complete with all of the major parameters defined as accurately as possible. In general, systems which do not accomplish the desired overall objectives fail due to inadequate definition of the job.

5.8.2 Develop Flow Chart

The flow chart is the primary tool of the system designer since it will break down each of the steps of the problem solving process. The flow chart pictorially illustrates the sequence of events in the system and the major paths of information flow. Frequently, the problem to be solved must be restated, further modifying item 1.

5.8.3 Define the Major Control and Data Storage Registers in the Form of a General Block Diagram

Analysis of the flow chart will enable the system designer to estimate the general physical configuration of the equipment. The quantities of registers to be provided is a function of the desired degree of parallelism, memory capability and the cost/performance of the logic hardware.

5.8.4 Select a Control Scheme

The method of control to be used in defining the internal states in the system can be extremely critical since many methods do not provide flexibility for future change. The trade-off's in flexibility vs cost must be carefully evaluated at this point. Frequently, an awkward and inflexible control scheme will impose restrictions on the logic circuits with respect to speed.

5.8.5 Select a Circuit System

The selection of a circuit system is based on the speeds required to implement the block diagram within the available time for the proper solution of the problem as defined by the system flow chart. The achievement of the lowest possible cost at the desired speed is, of course, one of the major objectives. Other significant and important points are briefly discussed in Section 5.9 and its associated Figures 5-46 and 5-47.

5.8.6 Write the Detailed Logic Equations

The detailed logic design is based on the block diagram and the characteristics of the selected circuit set. This is the first point in the design cycle where detailed data concerning the circuits are required to accomplish the design. The equations now form the basic structure of the system.

5.8.7 Convert the Equations to Accommodate the Specified Characteristics of the Logic Circuit Set

Each equation is checked for feasibility of implementation within the constraints of fan-out, fan-in, cost and the desirability of alternate choices. Occasionally, the logician is constrained to the point where special circuit modifications become highly desirable to solve a difficult and critical portion of the design.

COMPARATIVE CHARACTERISTICS OF SEVERAL CIRCUIT TYPES

MANUFACTURER TYPE	SPEED		FAN OUT		NOISE IMMUNITY		POWER DISSIPATION		TEMPERATURE RANGE °C		SUPPLY VOLTAGES
	GATE DELAY FAN OUT = 3 nsec	BINARY COUNT MHz	GATE	BUFFER	GATE & BINARY mV	% OF LOGIC SWING	SINGLE GATE mW	BINARY ELEMENT mW	MIN.	MAX.	VOLTS
FAIRCHILD mWμL900 DCTL	50	8	4	30	300	20	2	15	-55	+125	+3 ± 10%
FAIRCHILD HSμL900 DCTL	15	10	5	25	250	18	12	52	-55 +15	+125 +55	+3 ± 10%
TEXAS INSTR. SERIES 51 RCTL	200	0.8	5	25			2	2	-55	+125	+3
WESTINGHOUSE WM 200 DTL	35	11	11	17	550	10	8	50	-55	+125	+6
FAIRCHILD 930 DTL	25	10	9	20	700 550	18 15	5	20	-55	+125	+4 ± 10%
SIGNETICS SE 100 DTL	30	10	5	25	500	14	7	16	-55	+125	+4 AND -2 OR 0
SIGNETICS UTILOGIC	25	8	10	17	1000	35	5	90	0	+70	+4.5
MOTOROLA MC 300 CML	7	30	26	-	320	40	35	52	-55	+125	-5.2 -1.15 REF.
MOTOROLA MC 1060 CML	3	-	10	-	250	40	300	-	0	+70	-5.2
SYLVANIA SUHL-I TTL	10	20	15	30	1100	30	15	50	-55	+125	+5 ± 10%
STEWART WARNER SWG TTL			12	24					0	+75	
SYLVANIA SUHL-II TTL	6	30	12 10	-	1000	33	22	55	-55 0	+125 +75	+5 ± 10%
FAIRCHILD CTL	4*	30	8	25	500*	10	50	250	15	+55	+4.5 AND -2.0 ± 10%

* GATE DOES NOT PROVIDE THRESHOLDING
NOISE MARGIN IS FOR INVERTER
3 LEVELS OF "AND" PRODUCING 250 mV

Figure 5-46

PERFORMANCE RANKING OF BASIC CIRCUIT TYPES

TYPE OF TRANSISTOR LOGIC	SPEED	FAN-OUT	NOISE IMMUNITY	POWER LEVEL	MFG COST	EASE OF APPLICATION
HIGH SPEED CURRENT MODE	1	3b	1b	7	6	7
COMPLEMENTARY TRANSISTOR	2	4a	5	6	1	6
CURRENT MODE	3	1	1a	5	4	5
TRANSISTOR-TRANSISTOR	4	2	2b	4	3a	4
DIRECT COUPLED HIGH SPEED	5	4b	4	3	2	2
DIODE	6	3a	2a	2	3b	1
DIRECT COUPLED LOW POWER	7	5	3	1	5	3

Figure 5-47

5.8.8 Check Timing for the Critical Areas in the Resulting Design

Circuit information becomes the data base for development of the timing charts which illustrate the detailed sequence of events in the machine. From these charts, clock skew and clock jitter limits may be determined and compared with various methods and circuitry for clock generation and distribution. Unless the circuits are extremely fast, special clock circuits are usually required. Logic sets which provide buffers and a higher speed version using the same power supplies and logic swings are popular for their effectiveness in solving clock problems and critical timing situations.

5.8.9 Prepare a Logic Schematic

Although the preparation of final logic schematics is not always required, many firms require the final documentation to be in logic schematic form. There is a growing trend to provide both logic schematic and complete equations for purposes of checking and customer convenience. The form of the logic schematic varies, but, in general, there will be a complete listing of all the logic elements utilized, signal wiring is shown pictorially and in list form, and timing information.

Although this list presents the steps in system design in a logical sequential form, it seldom can be accomplished in a direct, step-by-step manner. As was mentioned, the interaction between the problem definition and the flow charting of the system approach frequently produce a new and changing definition of the problem and also produce strong gyrations in the flow chart. In fact, it is significant to note that at each step, changes and restrictions can cause appreciable modifications in all of the prior steps.

Aside from the changes imposed in the system design as a result of developing new knowledge, as an attempt is made to obtain a conceptual solution, the changes which may result as a function of circuit performance are also severe. In many cases, new circuits become available during the course of a program which enable simplifying design techniques to be applied. It is important, therefore, to fully realize that the system engineer must be continually kept abreast of circuit advances independently of the status of a particular system development.

5.8.10 Comparison of Circuit Systems

The data shown in Figure 5-46, illustrates the range of the significant circuit parameters, useful for system design. Typical values have been used rather than worst-case limits, to reflect more accurately the performance likely to be obtained in a system design. The objective is to provide a uniform basis for comparing the circuit classes. It should be noted that these parameters are not suitable for actual design since the influence of the wiring media is extremely important, especially at the high speeds attained by some of the devices. The source data were taken from the manufacturer's specification sheets; consequently, it is subject to the variability encountered with the use of different testing methods, test fixtures, etc.

With respect to speed, CML retains its historical lead in this significant parameter, retaining excellent percentage noise margins but with moderately high power dissipations. The spread in the speed attained by the various circuit implementations is currently nearly two orders of magnitude; from the 200 nsec obtained with the T. I. Series 51, to the 3 nsec with the Motorola MC 1050 Series. It is apparent that elements in the higher speed ranges, i.e., in the region of 10 nsec and faster, will require extreme care in packaging design to limit the effects of noise pickup and cross coupling. The high speed Motorola circuit requires terminated transmission lines for all but the very shortest of point to point connections. The classification of speed with respect to

5.8.10 (Continued)

"high", "medium" and "low" has always been dependent upon the state of the circuit art. It is, however, becoming increasingly apparent that speeds which cannot be utilized without terminated transmission lines will warrant the use of the term "high speed", whereas, those circuits which can be connected with open wire should be classified as "medium speed". The advent of Complementary Transistor Logic and the increasing popularity of T^2 Logic has increased the useful speed of medium speed circuits to about the 4 to 8 nsec region. The direct coupled and RCTL devices continue to be used by many systems heavily dependent upon good noise margins and the ease of design obtained with these straightforward logic circuits. In many applications, speed is not a critical factor for the overall system effectiveness.

Fan-out comparisons between the various logic devices is becoming increasingly difficult to effectively evaluate. For example, the CTL circuit approach does not provide rethresholding between logic "AND" levels. There is, consequently, a slight degradation in the logic voltage levels as the signal propagates from stage to stage. The value of the signal degradation is heavily dependent upon the loading upon the gate with respect to fan-out and fan-in. It is difficult to compare this approach to the more conventional techniques; Figure 5-46 illustrates the typical application of the element where three levels of logic are permitted between re-referencing elements. The system effectiveness of high fan-out is also questionable from the standpoint that an average system infrequently utilizes fan-out above 5. A practical savings in buffer elements may be realized for some applications, with some of the logic sets, but this saving may not be significant in the long run.

Noise immunity may be interpreted from two standpoints. First, the absolute value of the noise margin obtained would lead one to T^2L after glancing at the listing of characteristics. The speed of this device, however, is such to produce ringing and cross coupling difficulties with systems requiring extremely long cables or lines. The second method is based on the observation that many noise inducing effects are proportional to the total logic swing, hence, the percent value of noise immunity is an effective parameter to compare circuit performance. It is apparent that neither method presents a complete picture of the noise capability with the packaging and wiring media undefined. System designers should insist upon a full evaluation in the wiring media system intended for a given project. The ranking is based upon the most common method of assigning premium value to the highest percentage of the logic swing.

Power dissipation is highest for the highest frequency circuits and is lowest for the low frequency circuits, as may be expected for the increasing amount of energy required to switch the device rapidly, as well as the increase in average power dissipation as the basic repetition rate increases. It should be noted that many of the logic families offer multiple gates in one physical package and that the combined power dissipation may reach values of the order of several hundred milliwatts. Careful packaging design is therefore indicated to insure adequate cooling in the system. It should be noted that the CTL circuit family requires unused logic inputs to be connected to the positive power supply thus increasing the average power dissipation. Finally, the high speed CML does not show the power dissipation used in terminating resistors which can be appreciable for large systems with relatively long distances between subsystem elements.

5.8.10 (Continued)

The relative ease of application is among the factors ranked in Figure 5-47. In this listing, the value of "1" is assigned to the most desirable performance and the lower values receive proportionally higher ratings. In view of the narrow spreads between some of the devices, further subdivision as "a" and "b" status has been utilized to indicate marginal differences. Logic devices such as DTL and RCTL enjoy great popularity partly because of the simplicity of the design task. The circuit speeds are not high enough to cause problems in wiring rules. Also, their capability of rereferencing at each level of logic permits easy computation of the loading of devices and rapid computation of the propagation delay from stage to stage. This is not the case with the high speed CML or the CTL circuit family. In the former case, the speed is so high as to cause difficulty in predicting the performance with various wire lengths and loading combinations. In the case of the CTL circuit, it is necessary to maintain a count of the previous number of "unit loads" and adjust the logic commensurately. The incorporation of changes into the logic design is difficult for either of the two logic families, as reflected in the ranking of the ease of application.

Complementary logic is potentially extremely low in cost, although the continuing heavy competition in pricing is apt to submerge latent advantages of one approach over another. The relative comparison is perhaps the most attractive method of obtaining a "fix" on the dynamic price relationships in the volatile integrated circuit business. This is especially true of circuits offered for industrial applications at prices which are a fraction of units specified for military use. The cost ranking is based primarily on the complexity of the various circuits and considerations of factors which affect yield. The influence of volume purchasing is not factored into the ranking, but is a significant variable in the comparisons of the logic families for a specific application.

SECTION 6 LINEAR INTEGRATED CIRCUIT APPLICATION ENGINEERING

6.1 Introduction

Utilization of integrated circuit technology has developed far less rapidly for linear circuits than for digital applications. However, there remains strong motivation in most circuit areas to begin to make such conversions. In most instances, the usual arguments of economics, reliability and space-weight savings apply in the same manner as they do with digital circuits.

Computers, whose digital circuits may be fully integrated, require analog circuits in peripheral equipment. While most of these are presently being built in discrete component form, integrated sense amplifiers and other peripheral circuits are leading the trend toward integration to exploit space and economic savings. Military and space exploration electronic equipments are using the capabilities of linear integrated circuits advantageously. Commercial applications include hearing aids, communications systems and navigation equipment. Several major television set manufacturers have announced the use of linear integrated circuits in many of their newer models.

A number of linear circuits have already been produced in integrated form and are receiving a wide degree of acceptance. The first large scale conversion has been the differential amplifier, since this circuit lends itself to integrated technology. In addition, operational amplifiers are converted rather easily to integrated form. There has also been considerable work on video and other wide band amplifiers. Finally, work has been done with audio amplifiers in the laboratory, along with RF and IF amplifiers in integrated circuit form.

The conversion of both differential and operational amplifiers has been greatly expedited because of significant advantages. These circuits require active devices with closely matched properties, a quality difficult to obtain with discrete components. The fabrication process for integrated circuits can produce practically identical pairs of transistor and close spacing of these units on a monolithic chip assures excellent thermal "tracking". Many circuit functions can be designed using operational and differential amplifiers as the basic building blocks.

These designs frequently require the use of external components. In linear circuit design, there are a number of specific applications requiring one or more circuits of each type in each piece of equipment. Considerations do not allow designing new integrated circuits for each such requirement. Rather, universal circuit chips are being developed, which can be used to perform many different functions through the use of appropriate external components.

In this new technology, there is much room for ingenuity in clever, sophisticated design. The competent design engineer might begin by thinking in terms of circuit functions, rather than what may be available. For example, many high volume digital modules may be adapted to perform linear circuit functions. Logic gates, for example, may be used as squelch switches and multivibrators may be used as oscillators.

6.2 Systems Considerations

The fixed cost involved in the manufacture of integrated circuits makes it desirable to use a given integrated circuit configuration in as many different circuit functions as possible. Hence, knowledgeable design with integrated circuits will begin at the systems level. Often, minor adjustments in the block diagram can greatly reduce the variety of different functions required. Also, requirements for blocks that may be difficult to make may be minimized.

6.2 (Continued)

One interesting approach to minimizing difficulties in integrated circuit design is to use lumped selectivity, that is, to tune or couple at the end of several stages rather than between each stage. Another subtle approach may involve what might best be described as a selective placement of gain in a string of amplifiers to counter the noise problem. Considerable noise may be accepted in one stage which is overcome by the overall gain of several stages. This concept is hard to define, but there is much room for the imaginative circuit designer in these areas.

The single integrated circuit design may be made more flexible by leaving one or more components out of the monolithic chip or by using tabs on components so that they may be externally selected to suit a particular requirement in the block diagram. Another alternative that may be more expensive is to add masks to the original mask set which will change a component value or slightly modify the circuit configurations. The "master slice" approach, whereby a number of components are made in the substrate, and those desired are connected by the metalization pattern, is a version of this technique. Thus, one integrated circuit may perform many different functions with a minimum increase in cost.

6.3 Basic Design Considerations

Linear integrated circuit design is not radically different from design using discrete components, once the advantages, limitations and new economic effects are thoroughly understood. Gaining this knowledge is not too different from learning the practicalities of discrete components that design engineers learn in the early phases of design training. It is the intent of this section to delineate, insofar as possible, the new rules in practical form.

There are three major considerations in contemplating linear integrated circuit design.

1. Advantages - it is now possible to obtain almost perfectly matched resistors, transistors and to gain almost perfect thermal tracking between components

2. Limitations - the limitations are the large capacitive parasitics, wide component tolerances and inability to fabricate inductors and large size capacitors

3. Economic factors - among the new operating economic factors are that active devices are now less expensive than passive devices. Transistors may be fabricated for a fraction of the cost of a resistor or capacitor - gain is cheap.

As will be shown, inherent characteristics of integrated circuits greatly facilitate design of differential ampliers. In addition, nonlinear bias compensation is much more easily accomplished. (This will be explored in some detail under "Biasing Considerations").

A superficial examination of limitations would seem to place major problem areas in terms of lack of large capacitive values and inability to fabricate inductances. Leading industrial authorities have stated that the biggest change, in terms of linear circuit design using integrated circuits, is the wide tolerance range encountered. This area will require the closest attention by design supervision in the immediate future. A close study of fabrication details will indicate the wide resistor and capacitor tolerances that may be expected. High yield circuits must be designed to accommodate these wide tolerances.

6.3 (Continued)

Perhaps one of the better ways to gain understanding of this acute tolerance problem is to take advantage of several manufacturer's master "breadboard" specifications. These chips are offered with the leads of the components brought out to bonding pads. While it may not be feasible to actually procure these breadboards and make up circuits (although this is certainly desirable), it should be relatively easy to obtain specifications from such companies and make a a paper design using the cited tolerances. They may be then easily breadboarded, using discrete components.

As previously indicted, the economics of design have changed. The ability to fabricate large numbers of active devices inexpensively has triggered considerable investigation concerning replacement of linear circuits with digital circuits, wherever applicable. In any event, it is desirable to avoid the use of large value capacitors (which simply can not be made). Even lower values are more expensive than transistors. This is also true of resistors. As a general rule, the small area devices are the least expensive.

There is no present capability for fabricating inductors and transformers of any consequence. In addition, parasitics are a much bigger problem than with discrete component design at frequencies above a few megahertz. Much work is going on in all areas of the integrated circuit industry to resolve these and other problems, but there is much room for the knowledgeable design engineer to avoid or at least minimize, these considerations.

6.3.1 Biasing Considerations

There are several reasons for using low power-drain designs when dealing with integrated circuits. Probably the first is that integrated circuits don't need as much bias power as most conventional circuits. This is a result of using small transistor geometries to conserve chip area. A small geometry silicon planar transistor provides adequate gain-bandwidth products at much lower current levels than the germanium alloy types often used in conventional circuit designs. For example, a typical integrated circuit transistor may occupy only 25 to 100 square mils and have a gain-bandwidth product (F_τ) of over 300 MHz at 8 milliwatts (2 mA, 4 V) bias power. 30 to 35 db power gain at 20 MHz is typical. The available common emitter power gain may be calculated as follows:

$$G_e = \frac{F_\tau}{8\pi f^2 r'_b C_c} \qquad 2f_{\alpha e} < f < 2f_{\alpha b}$$

where:

f = operating frequency
F = gain-bandwidth product
r'_b = base resistance
C_c = collector to base feedback capacitance

When designing for low bias power, the supply voltage should be lowered rather than the operating current, for the following reasons:

1. The voltage has a smaller effect on F_τ than the emitter current

2. It allows the use of more heavily doped collector material with its attendant reduction in series collector resistance

3. It reduces the resistor values required in the circuit, thus reducing chip size requirements

4. It allows the size reduction capabilities to be realized without creating heat build-up problems.

6.3.2 Bias Stabilization

The most common method of bias stabilization (Figure 6-1) uses a resistor voltage divider. R_1 and R_2 provide a voltage source for the base and an emitter resistor (R_3) to provide emitter current degeneration. The sum of the values of R_1 and R_2 is determined so as to allow bleeder current flow, which is large compared to the maximum allowable base current. This reduces the effect of h_{FE} and I_{CO} variations on the voltage established by the voltage divider. I_{CO} is not normally significant in silicon planar integrated circuit transistors. The emitter resistor value is selected to provide a voltage drop which is large compared to the temperature-caused variations in the V_{BE} of the transistor ($V_{BE} \cong 2mV/°C$). The resistor ratio tolerance and temperature tracking of diffused integrated circuit resistors provide excellent collector-emitter voltage stability with this bias scheme. The emitter current is, however, subject to variations resulting from the absolute values of the resistors. In situations where low current drain is not an important consideration, this type of biasing yields satisfactorily low total resistances. If low current drain is important, nonlinear compensations should be used.

Nonlinear compensation is more easily accomplished in integrated circuits than in conventional circuits. Figure 6-2 shows a bias scheme using a diode in the base bias network. This diode can be formed simultaneously with the emitter base junction of the transistor in a monolithic silicon circuit. The degree of matching of forward voltage drop versus temperature characteristics of the diode and the transistor emitter - bias junction is far better than can be obtained in discrete component circuits without special matching techniques. The value of R_3 may be reduced by a factor of 10 or more because the voltage required across it now only has to equal the variation in the difference between the diode drop and the emitter base drop. This is typically 10 to 100 microvolts per °C. This reduction in emitter resistor value may eliminate the need for an emitter bypass capacitor in AC amplifier circuits.

In an integrated circuit, the formation of the temperature compensating diode results in a parasitic transistor which can cause trouble in some cases. This potential problem is eliminated by shorting the collector base junction of this transistor. Thus, the diode may be represented as shown in Figure 6-3.

6.3.3 Direct Coupling

Direct coupling and DC feedback often may be used to eliminate some resistors from integrated amplifier circuits. The integrated circuit structure has the inherent advantage of providing tight thermal coupling between the diode and the transistor; however, they should be close to each other on the chip if there is significant power dissipation in the circuit. Figure 6-4 shows a two stage common emitter requiring only 4 resistors. The emitter current of the first stage will change by an amount determined as shown:

$$\Delta I_{e1} = \frac{2\Delta V_{BE}}{R_1} \qquad I_{c1} >> I_{b2}$$

$$\Delta I_{e2} = \frac{\Delta V_{BE}}{R_3} \qquad I_{b1} R_4 << V_{BE}$$

This circuit can be fabricated easily in silicon monolithic form. It can provide stable gains of 60 db or more in a single chip.

In the design of integrated circuits DC amplifiers, the temperature compensation advantages of diode bias stabilization and differential amplifier circuitry should be utilized wherever practical. Allowances must be made for the temperature coefficient of the diffused resistors. In critical cases, it may be desirable to use compatible thin film resistors such as Nichrome to reduce the temperature coefficient.

AMPLIFIER BIAS METHOD FOR STABILIZATION

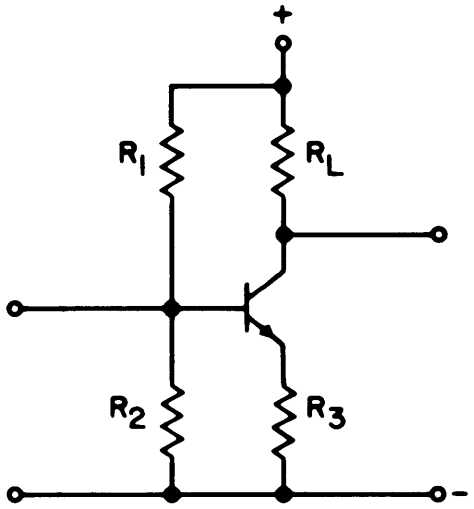


Figure 6-1

BIAS METHOD UTILIZING DIODE COMPENSATION

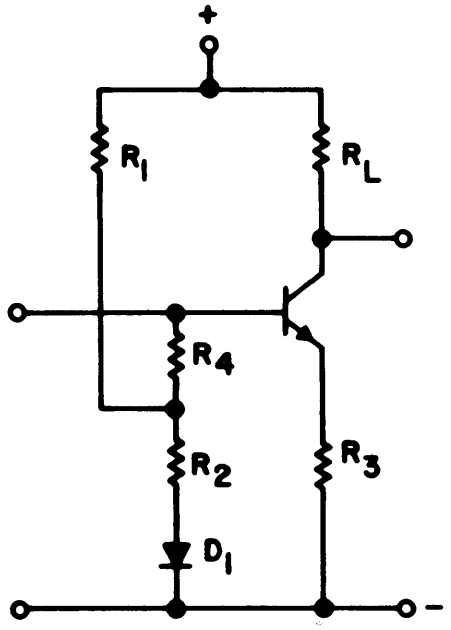


Figure 6-2

DIODE EQUIVALENT CIRCUIT

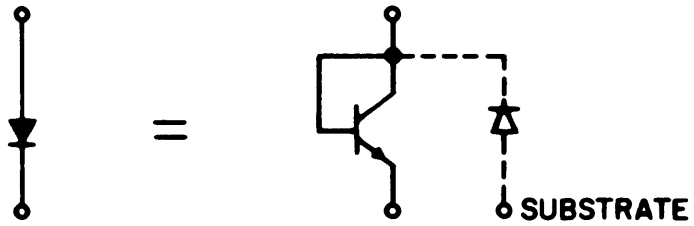


Figure 6-3

A TWO STAGE COMMON EMITTER AMPLIFIER

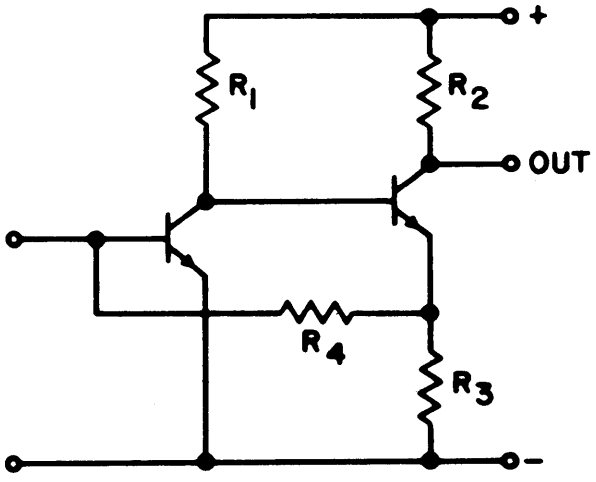


Figure 6-4

6.3.4 Differential Input

A differential input stage can be used to improve the stability of a single-ended DC amplifier such as shown in Figure 6-5. Complete differential amplifiers provide excellent stability and should be used when the circuit function does not require a common terminal between input and output. A multistage differential amplifier using transistors of the same polarity requires level translation to return the output level to zero. The output level may be returned to zero by using transistors of opposite polarity for the output stage, but the fabrication of both NPN and PNP transistors in a single monolithic chip is at present a costly process. A more practical approach is to form the NPN stages in one chip and the PNP stage in another. The two chips may be packaged together so that feedback loops do not have to leave the package. It is sometimes practical to use the same layout for both the PNP and NPN differential amplifier stages, thus saving the mask making costs. However, PNP integrated circuits have some drawbacks which are not significant in NPN circuits. The resistors are the major problem area. A PNP integrated circuit would have N-type resistors since they are formed during the base diffusion. N-type resistors have two fundamental disadvantages. N-type regions have lower impurity concentration for a given sheet resistance due to the higher mobility of electrons. The lighter doping causes somewhat greater variability of sheet resistance. The other major disadvantage of the N-type resistor is due to the surrounding P-type material which is more subject to channeling. Surface channels can cause drastic nonlinear effects. The annular technique used on PNP transistors tends to reduce this, but it requires extra diffusions and more substrate area. One solution to this problem is the use of compatible thin film resistors on top of the oxide in PNP circuits. The same layout can still be used, but several extra masks are required. The extra processing increases the cost of the PNP chip, but it is still more economical than fabricating both polarities in the same chip.

6.3.5 Capacitors and Capacitance Multipliers

In coupling applications, the most bothersome parasitic is shunt capacitance. Typical ratios of useful to parasitic capacitance are from 2:1 to 5:1, depending upon their size and bias condition. This parasitic simply adds to the desired capacitance when it is used as a bypass. Diffused capacitors can be used quite satisfactorily where a low value bypass is required, but they do have somewhat higher Equivalent Series Resistance (ESR) than their discrete component counterparts. It is often possible to design the circuit to use the low values of bypass capacitors available in monolithic form. For instance, a common-base amplifier may be used instead of a common-emitter stage. The base bypass capacitor need only be $1/\beta$ times as large as an emitter bypass capacitor. Also, as pointed out earlier, some types of bias schemes can reduce the emitter resistor requirements to the point where bypassing may not be necessary. Capacitance multipliers can be used to increase the effectiveness of bypass capacitors (Figure 6-6). This circuit increases the effective value of C by the β of Q_2; however, it increases the current drain requirements significantly because Q_2 should be operated at a higher current than Q_1. This is necessary because the internal emitter resistance appears as part of the Equivalent Series Resistance (ESR) of the equivalent bypass capacitor.

Another application for bypass capacitors is frequency response shaping. A capacitor is often shunted from collector to ground to "roll off" the high end response of an amplifier. The capacitance values required for audio response shaping are much too large for economical integration, but special circuit arrangements such as capacitance multiplication may be employed in some of these cases. Another valuable method of increasing the effective value of a capacitor is to connect it from collector to base in a common-emitter amplifier, or output to input in any combination of stages having a

6.3.5 (Continued)

voltage gain and phase reversal. The value of capacitance appearing across the input of the stage is given by:

$$C_{eq} = CA_v$$

where:

A_v = operating voltage gain

6.3.6 Frequency Response

It is important to consider the effects on performance resulting from replacing of discrete components, resistors, capacitors and transistors. Consider the video amplifier circuit in Figure 6-7. The response of a typical diffused resistor is shown in Figure 6-8a. The response is flat out to 10 MHz and then rolls off at 3 db/octave. All resistors will affect frequency response when associated with the signal flow. Typically, collector resistors would start rolling off at 10 MHz. The base resistor might begin at 20 megahertz. This resistor has a higher frequency response because circuit considerations allow a wide tolerance. It can be physically narrow reducing the parasitic capacitance. Figure 6-8b shows the response of a transistor amplifier, with ideal passive components. The composite response of the transistor and resistors is shown in Figure 6-8c.

The frequency response of integrated capacitors has a degradation caused by both capacitive parasitics and by a high equivalent series resistance. The MOS capacitor is the most widely used integrated capacitor. The size of the capacitance is limited to 100 to 200 pf. When this type of capacitor is used as a bypass capacitor, the circuit performance is severely degraded. (Figure 6-8d). The reason for this is that the value of capacitance is small and the series resistance is degrading because it is in series with the bypass capacitor. On the other hand, coupling capacitors have more serious degradation because the parasitic capacitance shunts the signal to ground. The ESR in this case causes little difficulty.

6.4 Classes of Linear Circuits

For convenience, the circuit functions performed by integrated electronics are divided into five categories:

1. Differential amplifiers
2. Band pass amplifiers
3. Audio amplifiers
4. Video amplifiers
5. Miscellaneous linear circuits

The problems of designing the integrated circuits are somewhat different for each category, although many features are common. For example, the bias arrangement is nearly the same for all linear integrated circuits, involving the extensive use of diodes and transistors.

6.4.1 Differential Amplifiers

A differential amplifier has two input terminals and two output nodes, which allow the application of two input signals (often the two leads to a single signal source above ground). The output develops an amplified version of the voltage difference between the input terminals, rejecting signals between either input and ground. This makes the amplifier useful in many measurement systems and also adapts it to analog computer service.

This type of amplifier must be symmetrical in all respects, shown in Figure 6-9. Each element of one half must be precisely like its

DIFFERENTIAL INPUT STAGE

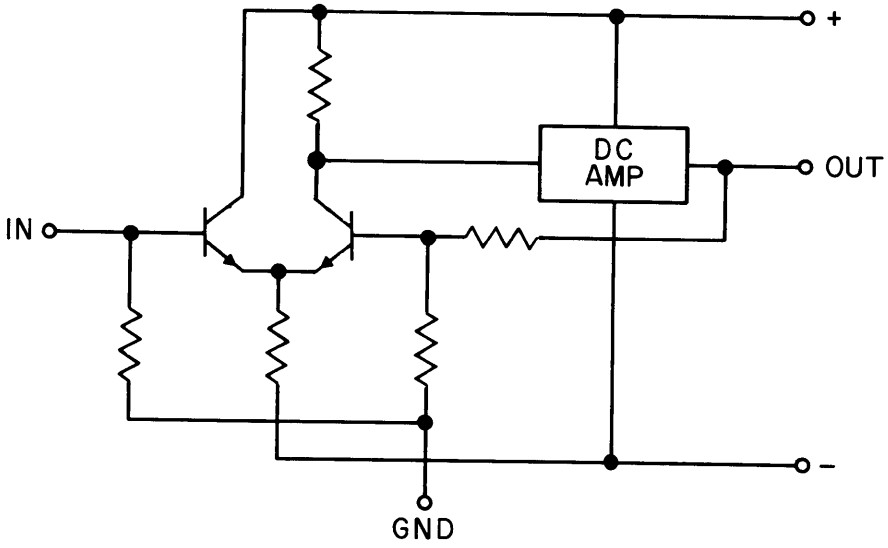


Figure 6-5

CAPACITANCE MULTIPLIER

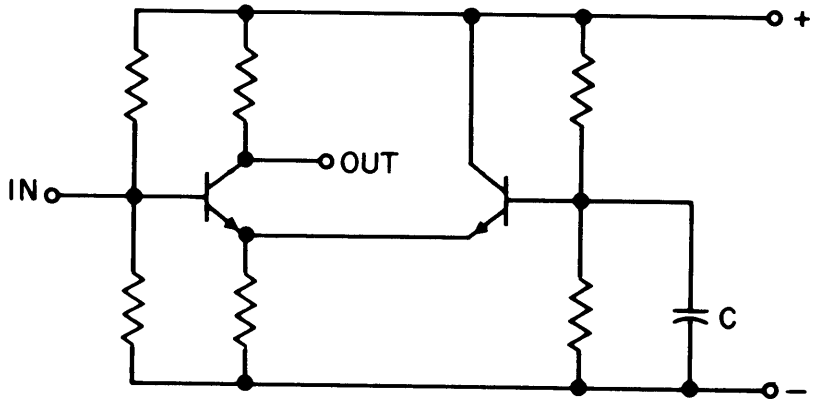


Figure 6-6

VIDEO AMPLIFIER

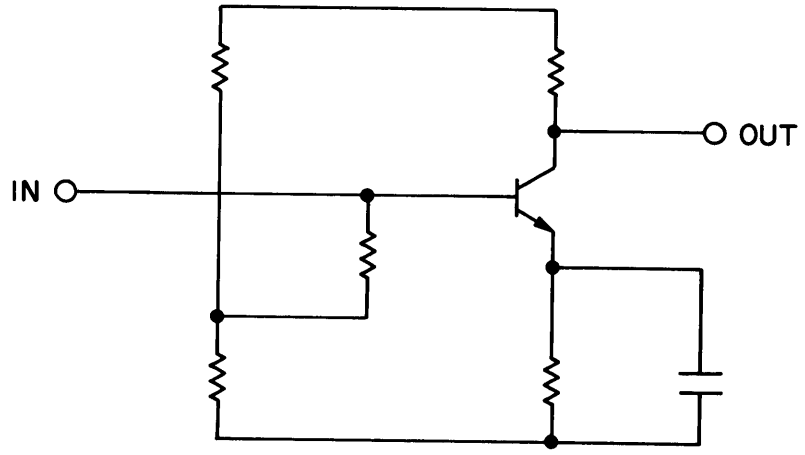


Figure 6-7

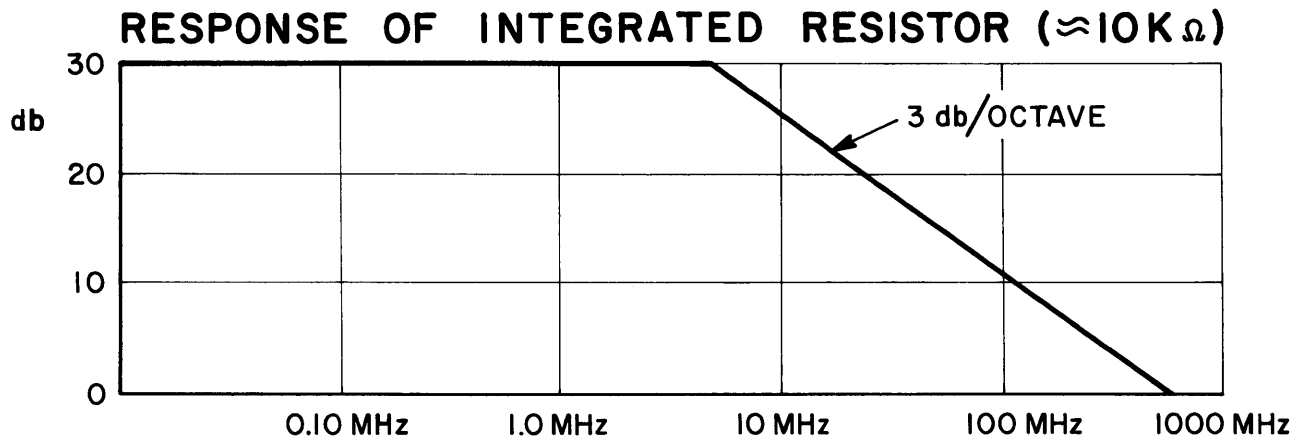


Figure 6-8A

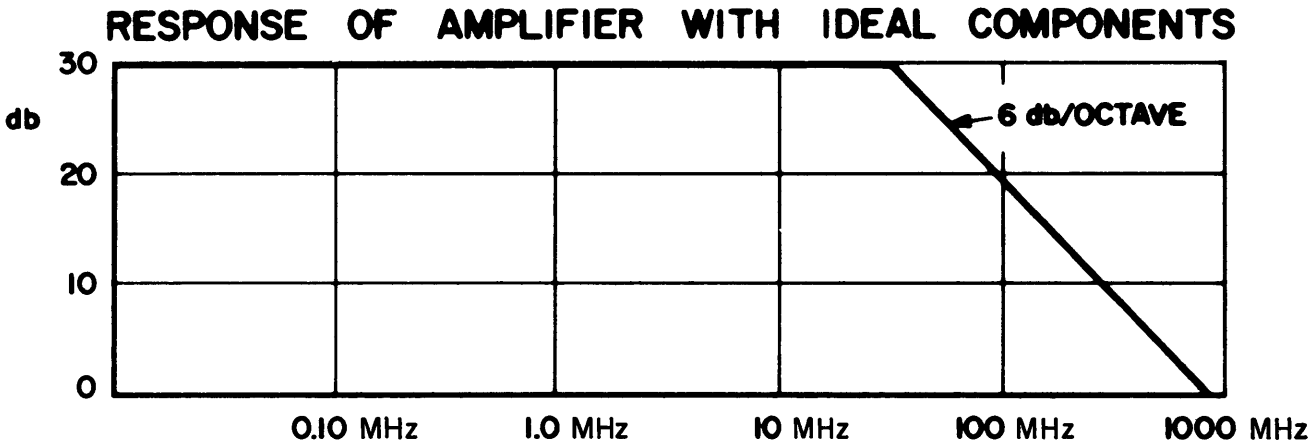


Figure 6-8B

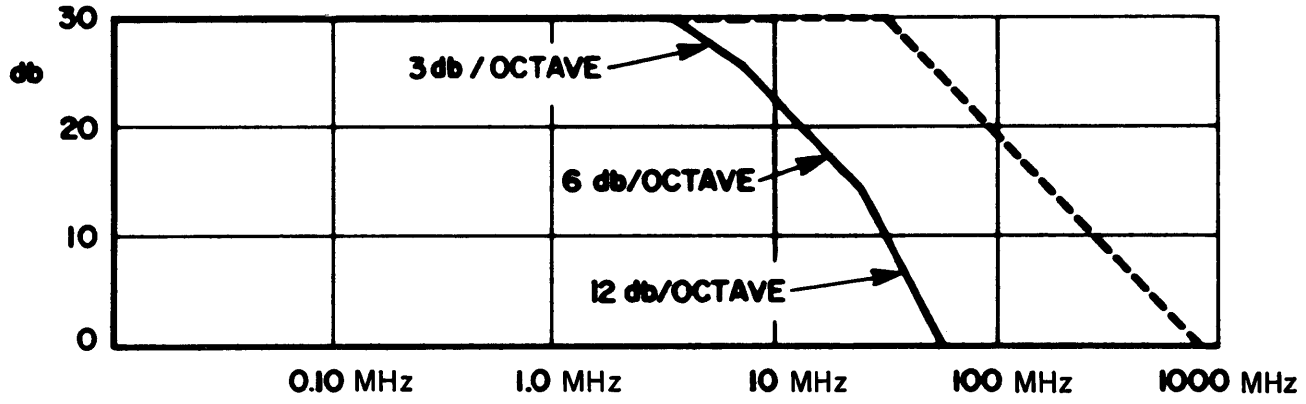


Figure 6-8C

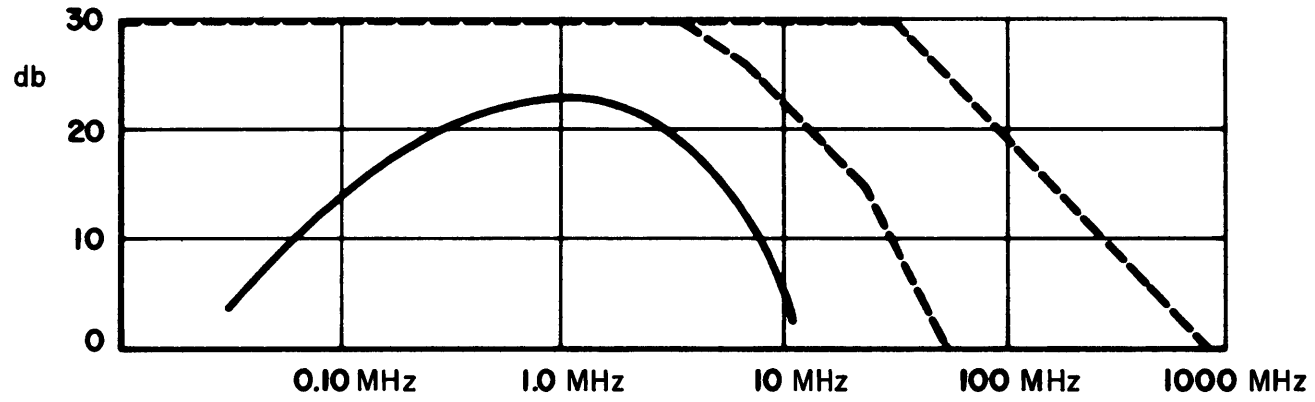


Figure 6-8D

6.4.1 (Continued)

counterpart in the other half. This requirement includes both absolute component values and tracking with temperature changes. Satisfying this requirement, while difficult in discrete form, is inherent in monolithic structures. Process variations that may cause difficulty in holding tight tolerances, affect the corresponding components in an identical manner. The matching of components and their tracking with temperature is better than can be accomplished by matching of individually produced components. The good thermal conductivity of silicon will assure that the components will operate at nearly identical temperatures. In discrete component circuits, this condition cannot be duplicated even by the use of thermally controlled ovens because of differences resulting from local power dissipation.

Differential amplifiers can be used as operational amplifiers or as ordinary single input and output amplifiers. They are extremely versatile; they may be operated with differential or single-ended inputs or outputs; they have frequency responses from DC to above 40 MHz; gains in the range of 40 to 80 db; and they are widely adaptable to a considerable range of practical applications.

6.4.2 Operational Amplifiers

Perhaps the most versatile type of differential amplifier is the operational amplifier having a differential input and a single-ended output. The output node carries zero potential when the difference between input voltages ($V_1 - V_2$) is zero, and the output node swings both positive and negative with input signals of different polarities. For optimum performance, the operational amplifier should possess:

1. High differential input impedance (greater than 20 Kohms)
2. Low single-ended output impedance (less than 200 ohms)
3. Large open-loop gain (greater than 1000).

The circuit shown in Figure 6-10 will provide single-ended outputs from a differential amplifier. In monolithic form, the entire circuit shown would be placed upon a single chip. Some circuits avoid the use of PNP transistors, while some manufacturers use lateral PNP's and substrate PNP's. Another manufacturer uses multiple diffusions to make a vertical PNP in the same substrate as the NPN.

If the basic operational amplifier supplies large gain-bandwidth products and sizable negative feedback is applied, the overall performance can be made almost independent of the amplifier's characteristics. Only external components will seriously affect the response. The two basic configurations are shown in Figures 6-11 and 6-12, along with the significant equations. The gain expressions can be used with small error for closed-loop gains below 10 and open-loop gains greater than 1000. High input impedances of the operational amplifier above 20 Kohms (and low output impedances, below 200 ohms) also improve the approximations.

From the equation for gain, it is seen that gain may be traded for bandwidth or for higher or lower input impedance (the inverting amplifier has low input impedance, while the noninverting version is high).

The operational amplifier's two major problems involve saturation and instability. The dynamic range limitation is reached when a common mode signal is sufficiently large to drive one of the input transistors into saturation. This destroys the operating efficiency of the amplifier. It can be avoided by assuring that the closed-loop gain exceeds 10, or using feedback resistances is greater than 50 Kohms. This problem may also be minimized by connecting a limiting diode between the input terminal and ground.

SYMMETRICAL AMPLIFIER CIRCUIT, AN IDEAL FORM FOR INTEGRATION.

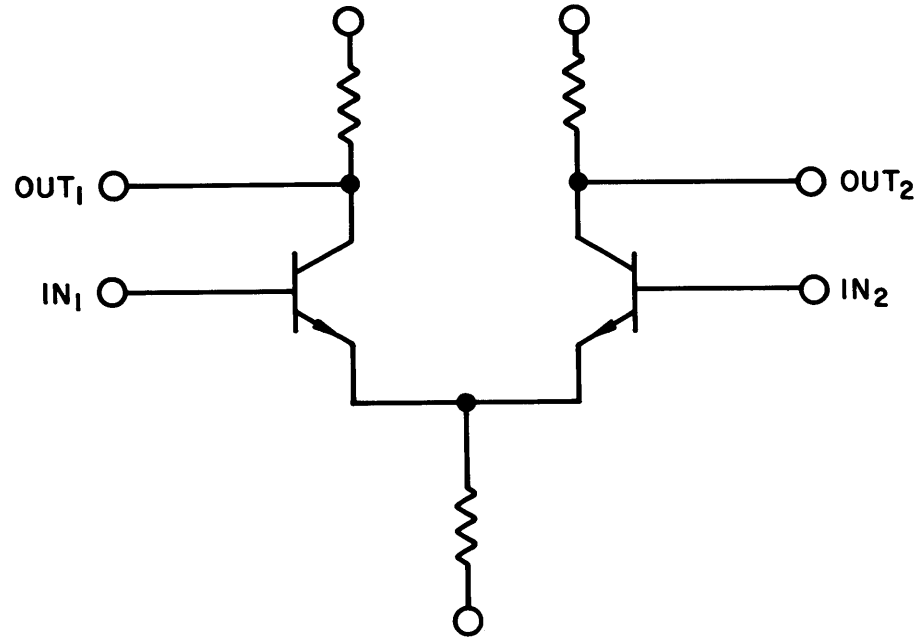


Figure 6-9

FORMING A SINGLE-ENDED OUTPUT FROM A DIFFERENTIAL AMPLIFIER

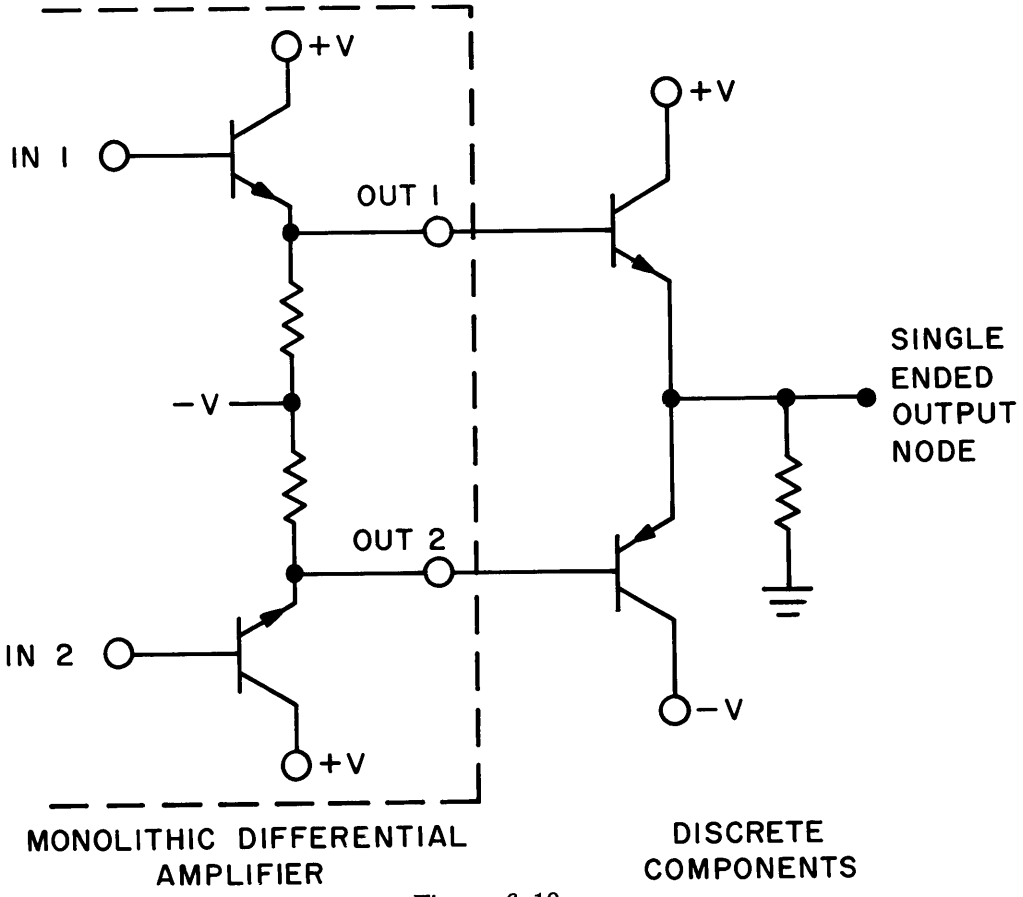
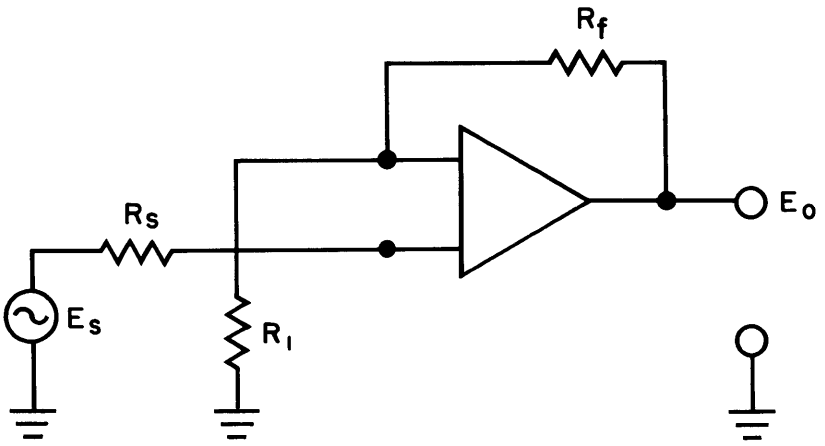


Figure 6-10

NON-INVERTING OPERATIONAL AMPLIFIER WITH FEED-BACK

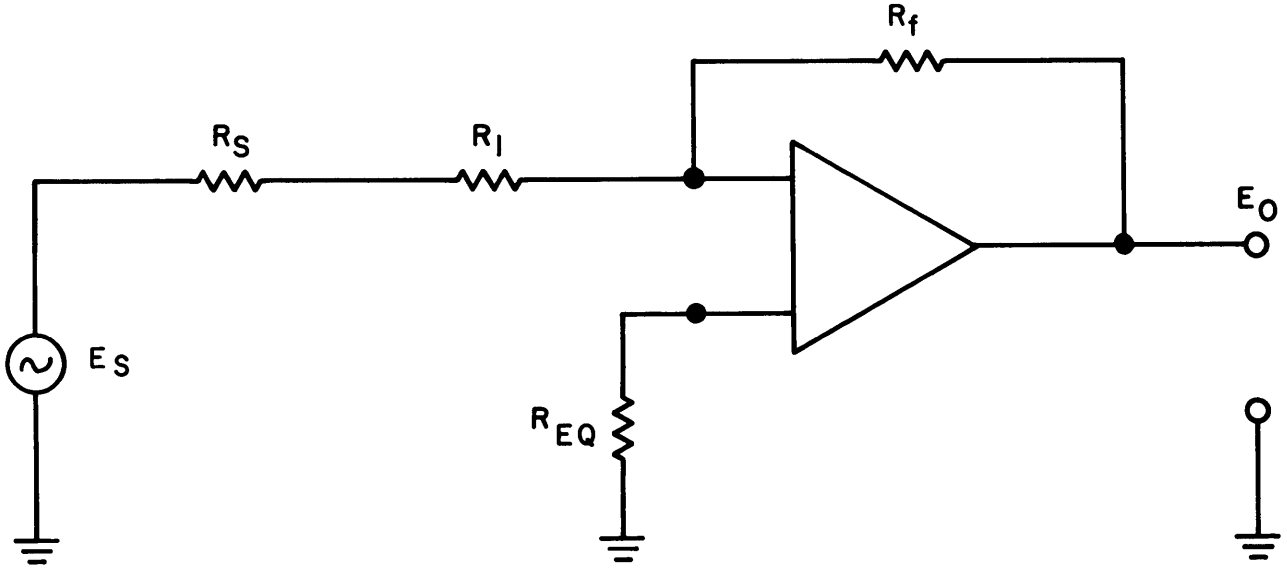


$$\text{VOLTAGE GAIN : } A_V = \frac{R_f + R_I}{R_I}$$

$$\text{INPUT IMPEDANCE : } R_{IN} = \frac{A_{VO}}{A_V} R_{IN}$$

Figure 6-11

INVERTING OPERATIONAL AMPLIFIER WITH FEED-BACK



$$\text{VOLTAGE GAIN : } A_V = \frac{R_f}{R_I + R_S}$$

$$\text{INPUT IMPEDANCE : } R'_{in} = \frac{R_{in}}{A_{VO}}$$

Figure 6-12

6.4.2 (Continued)

The use of a feedback circuit can cause oscillation of the amplifier if careful design is not exercised. In the operational amplifier, oscillation may occur if the stage roll-off is greater than 12 db per octave. This is due to the phase shift associated with the fast roll-off, which may exceed 180°. However, new rules must be employed with integrated circuit amplifiers for the parasitic capacitance of the resistor differs from the isolated resistances of the discrete component amplifier. The distributed nature of these elements causes the phase shift to approach 45°, rather than 90°, as each time constant of an orthodox network provides. The result is a slight degradation of the frequency of oscillation.

An RC roll-off network with a cutoff frequency lower than that of the amplifier will cause a premature roll-off, at the rate of 6 db per octave. The maximum phase shift is 90°, so that oscillation cannot occur if the gain drops below unity before the steeper roll-offs and larger phase shifts take effect. For maximum bandwidth, roll-off circuits may be placed across R_f or the input terminals or both, as illustrated in Figure 6-13.

An example of an amplifier which sacrifices gain for high input impedance is shown in Figure 6-14. Here the voltage gain is only 4, but the bootstrap input has raised the input impedance to several megohms. Thus, the amplifier makes an excellent match to a Piezoelectric transducer, such as a crystal microphone, a high impedance phone pickup or other instrumentation transducer.

6.4.3 Band-Pass Amplifiers

Frequency discrimination is a common requirement and, specified in terms of bandpass, the selectivity ratio is usually defined as the ratio of the 60 db range of frequencies to the 6 db range. RF and IF amplifiers, used extensively in communication systems, are specified in this manner.

In the application of transistors to communication equipment, the discrete component approach has been to insert a sharp-skirted passive filter ahead of the IF stages and then amplify with RC stages. If the external filter's size can be tolerated in the integrated circuit counterpart, the series of RC stages may be produced efficiently in integrated form. This use of lumped selectivity is a practical method of building tuned amplifiers without the use of inductance, thus eliminating one of the components that cannot be built in integrated circuit form.

A variety of high-pass, low-pass and band-pass amplifiers may be formed from careful selection of feedback elements, around the basic operational stages. Examples of these are shown in Figures 6-15 and 6-16. A low-pass amplifier employs a single RC section in the feedback link to provide the roll-off at the frequency for which the capacitance C_f equals the value of R_f. The band-pass amplifier utilizes one of many schemes - a twin-T or notch filter. The filter has great attenuation over a narrow band of frequencies and small loss for all other frequencies. The amplifier's gain response is then identical in form to the attenuation characteristics of this filter.

The band-pass amplifier (Figure 6-16), has low Q, due to the slow fall-off of gain on either side of the band center. However, it does permit the entire network to be built in integrated circuit form. Since the operational amplifier has two input terminals, it is especially useful in bridge circuits. Figure 6-17 shows a thermistor bridge feeding such an amplifier.

Any ripple or noise in the power supply is attenuated by the common mode rejection feature. In many diode circuits (such as mixers, rectifiers, clippers, clamps and peak detectors), the threshold

USE OF RC ROLL-OFF CIRCUITS TO FORESTALL OSCILLATION

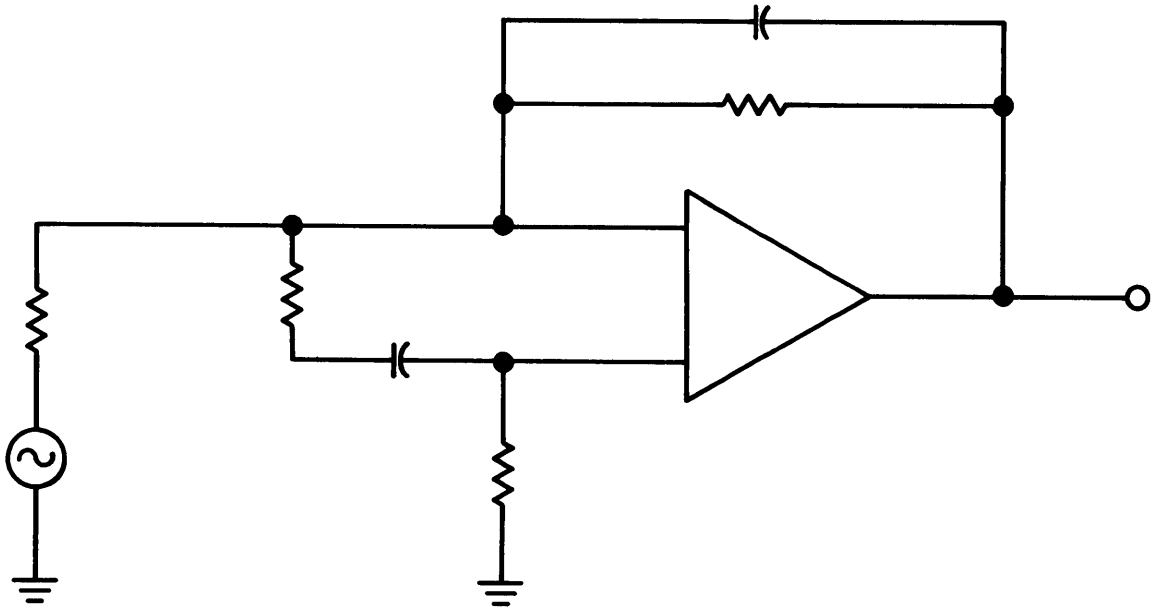


Figure 6-13

HIGH INPUT IMPEDANCE AMPLIFIER

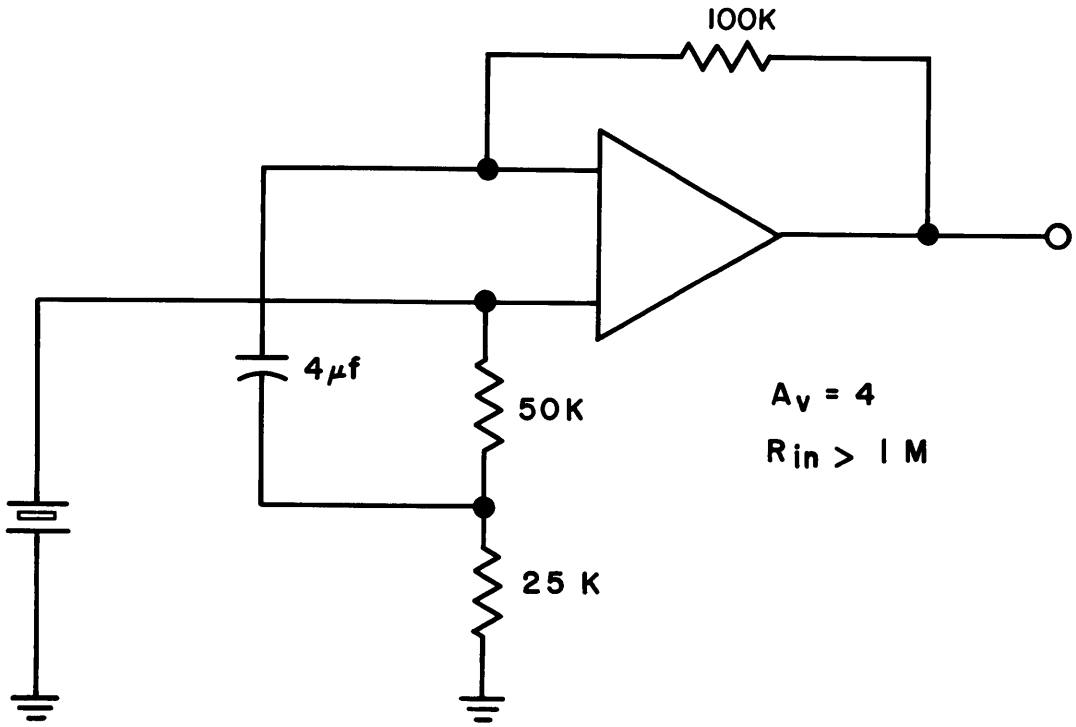


Figure 6-14

LOW-PASS AMPLIFIER DESIGN

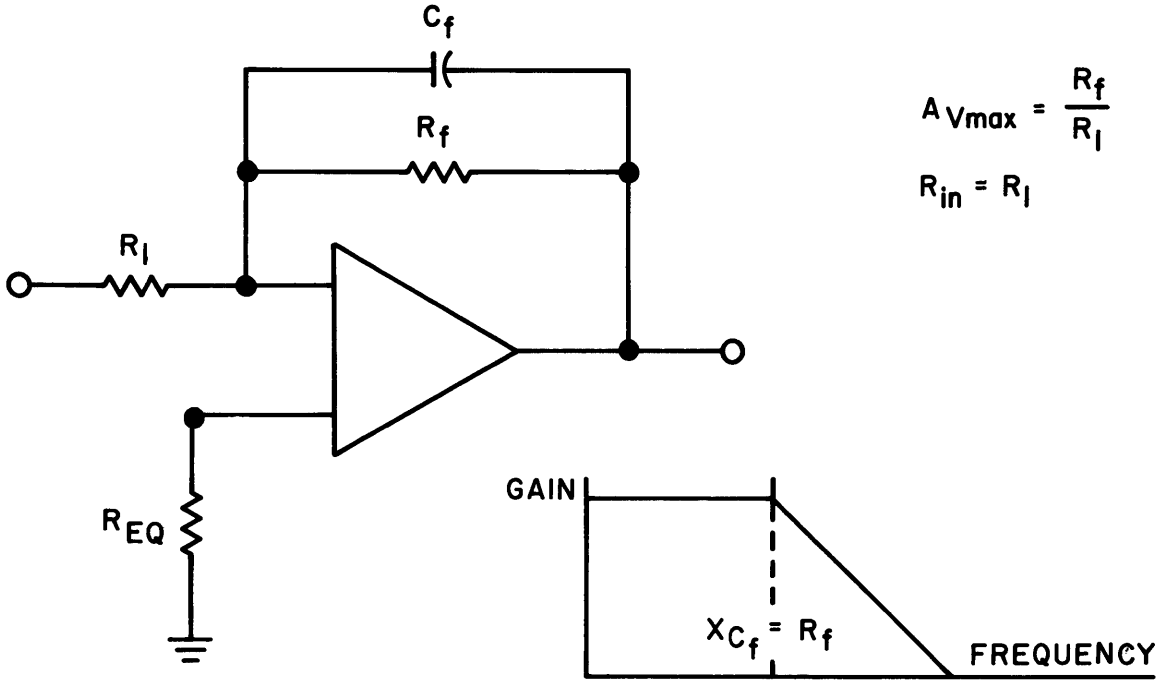


Figure 6-15

BAND-PASS AMPLIFIER DESIGN

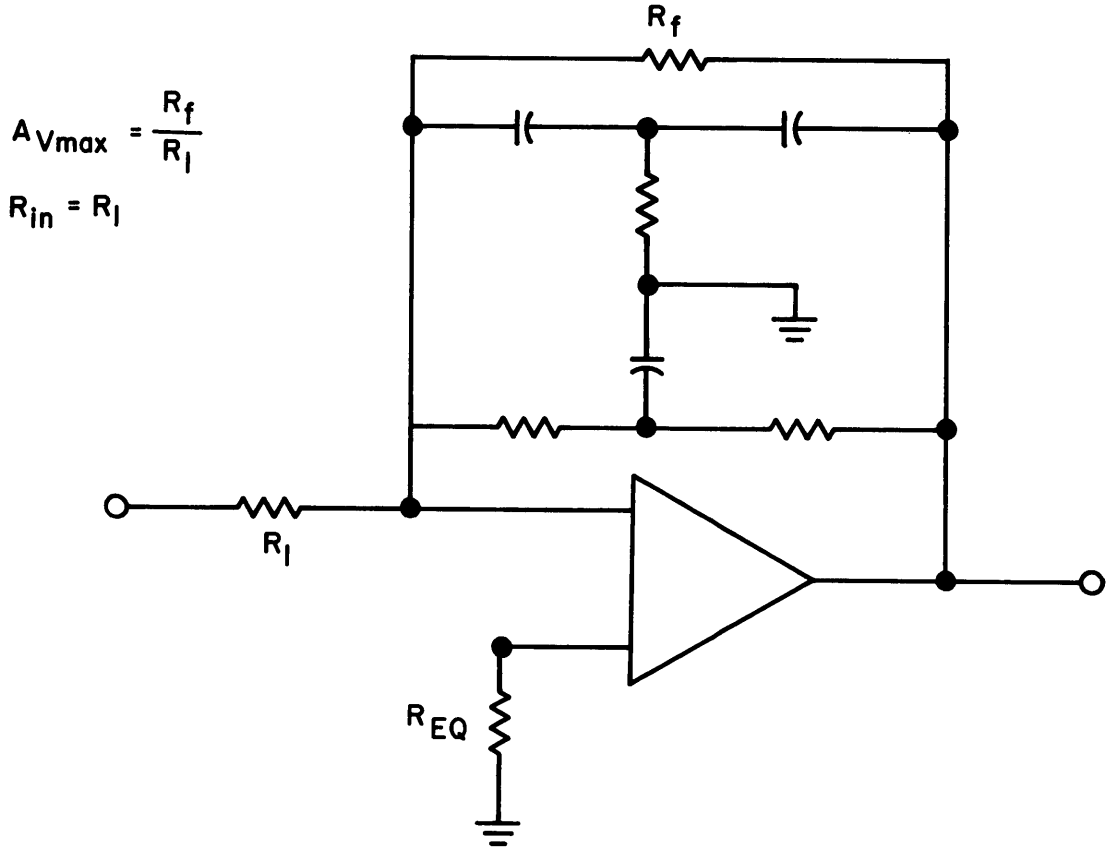


Figure 6-16

6.4.3 (Continued) voltage of silicon diodes could be a serious problem. The high open-loop gain of the operational amplifier reduces the threshold voltage as shown in the circuit of Figure 6-18. The inverting amplifier yields zero output for a positive input voltage and for negative input voltages, an inverted duplicate of the input. The threshold voltage, normally about 700 millivolts, is divided by the open-loop gain of the amplifier; it typically becomes about 1 millivolt. A similar technique may be used to design a peak detector. The output voltage is always positive and equal to the negative peak of the input signal.

6 4.4 Audio Amplifiers The major advantages which integrated audio amplifiers offer are smaller size, decreased power drain, potentially lower cost and greater reliability. The audio amplifier eventually drives a loudspeaker, a servomotor, or some other massive component. In addition, volume or loudness and tone controls are normally required; so, the size and weight advantages of the integrated circuit over the discrete component counterpart become lost.

Technically, the audio amplifier offers a challenge to the integrated circuit designer, particularly in the high-power stages. The challenge consists of designing efficient high-gain amplifiers with minimum use of NPN-PNP complementary transistors. The highest power stages are adaptable to integration, but require special thermal design. Currently, multichip techniques are being used in the 1 to 40 watt range.

6.4.5 Video Amplifiers Video amplifiers are characterized by broad bandwidth from DC upwards. As used in television, they are required to have flat frequency response from about 30 hertz up to and above 4 MHz. It is usually more convenient to specify the amplifier's response to a step or square wave input voltage, in terms of its gain, rise time, delay time, percent overshoot and the sag of the signal, with respect to time. Thus, a television video amplifier with one microsecond rise time will require about 1.5% of a horizontal line to make the transition from black to white in the picture. Obviously an amplifier with 0.2 μsec rise-time will produce sharper edges on the images on the kinescope. One requirement often encountered is the need for automatic gain control (AGC). Transistors can have their gain controlled by changing the emitter current or collector voltage as a function of incoming signal level. In good AGC circuits, a stage of gain is used to improve the AGC properties. Integrated circuits provide additional inexpensive transistors for this purpose.

Nevertheless, the ability to trade gain for bandwidth permits these amplifiers to serve a variety of applications, particularly in receiver design. Since it is generally easier to obtain gain at low than at high frequencies, receivers have usually used high-gain low-frequency circuits and lower-gain high-frequency circuits. The gain-bandwidth characteristics are, therefore, well suited to receiver service.

As a practical example of the use of adjustable gain-bandwidth characteristics, consider the design of a double-conversion communications receiver, a block diagram of which appears in Figure 6-19. The second IF amplifier must provide a gain of 100 db, but the frequency (455 KHz) is so low that the full gain of a video amplifier could not be attained. The first IF requires only 23 db gain, but at a frequency of 10.7 MHz. However, one video stage with 35 db of open-loop gain could be used with 12 db of feedback to extend its frequency range beyond 10.7 MHz.

The same technique will permit the RF stage to be built from the basic video amplifier by using a large amount of negative feedback. Theoretically, for each 6 db of feedback, another octave of bandwidth is acquired. Application of 24 db of feedback should, therefore,

THERMISTOR BRIDGE AMPLIFIER

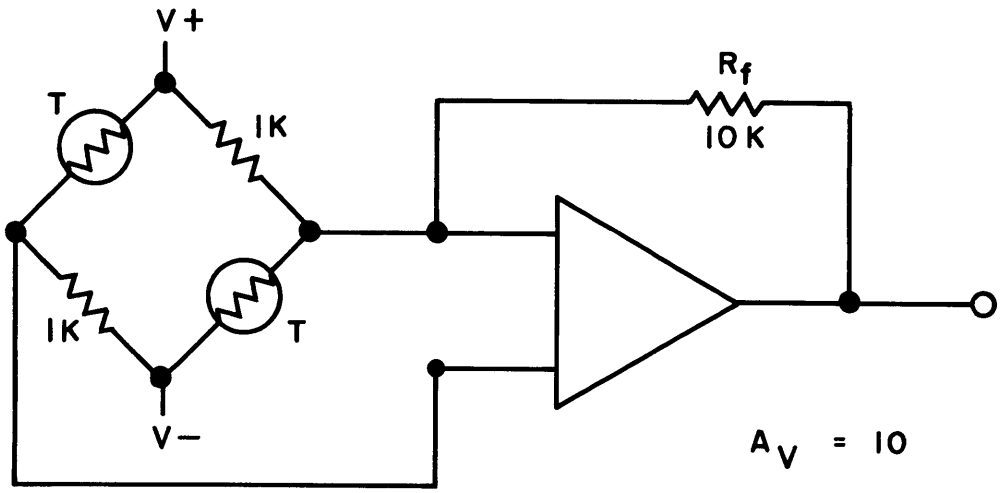


Figure 6-17

HALF-WAVE RECTIFIER WITH VERY LOW THRESHOLD VOLTAGE (~1mV)

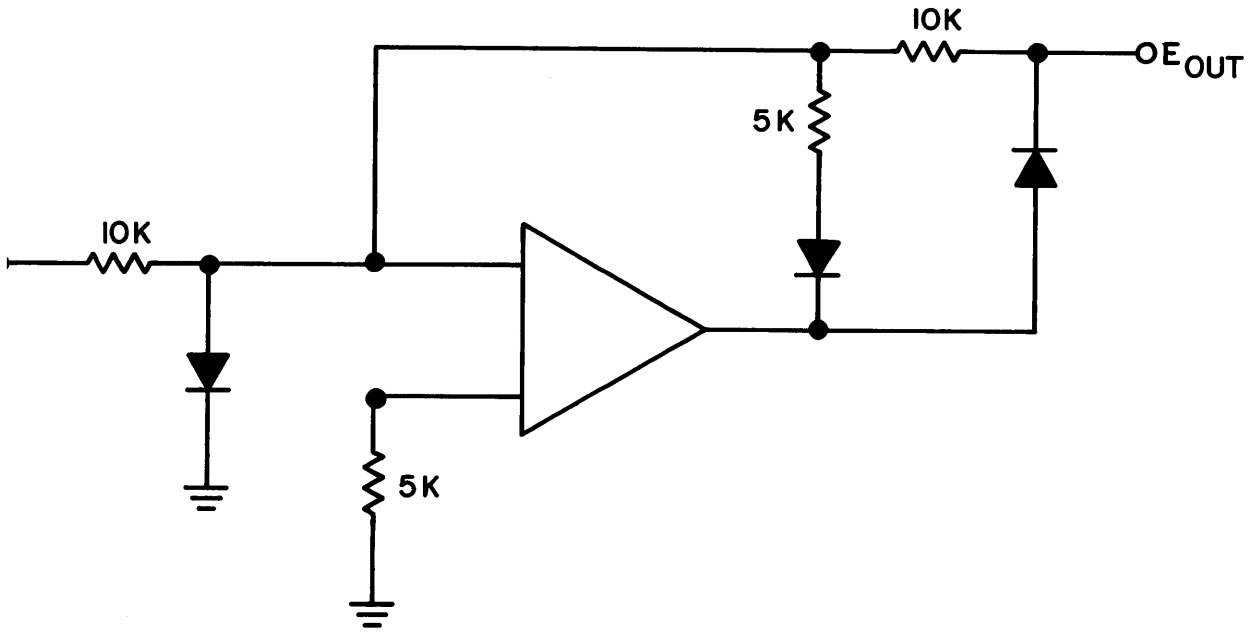


Figure 6-18

6.4.5 (Continued)

result in 4 octaves of bandwidth, so that the 50 MHz RF frequency would demand only 3.2 MHz bandwidth from the video amplifier (without feedback), much less than is available. Thus, one integrated circuit video amplifier can be used for both IF amplifiers and the RF stage as well.

Furthermore, the oscillators can be built from the same basic circuit. Since the basic video amplifier can be arranged to have two direct-coupled common-emitter circuits in addition to an emitter follower, a gain element with in-phase input and output signals is available. A frequency selective element with the proper impedance transformation is all that is required for an oscillator. Use of this circuit in the construction of an LC oscillator is shown in Figure 6-20. A crystal oscillator can be obtained by including a suitable crystal in the circuit.

Following the detector of this receiver, an audio amplifier is required. This may be made from the same feedback networks yielding the proper roll-offs. Most video amplifiers will drive low power transducers directly. Larger output requirements will necessitate using additional stages beyond the integrated circuitry. Preamplifiers for microphones, phonographs and tape recorders may also be built from the same video circuit. Still another modification will convert this basic circuit into a sweep generator, voltage-controlled oscillator, or a clock generator.

6.5 Special Circuit Configurations

6.5.1 Darlington Amplifier

The Darlington amplifier is particularly easy to fabricate in integrated form. They are capable of providing high gain in a small space. In applications requiring only a moderately high input impedance, the Darlington connection may be used. As can be seen from the circuit shown in Figure 6-21, the collectors are tied together, thus eliminating the need for separate isolation areas in the chip. This results in efficient use of chip area.

6.5.2 RF Grounded-Collector Circuits

By holding the collector at RF ground, a number of difficulties can be avoided. The parasitic capacitance associated with diffused resistors need not be considered in transformer coupled RF circuits because the resistors may all be placed at RF ground, as shown in Figure 6-22. In cases where it is necessary to have RF voltage appear across diffused resistors, the parasitic will introduce some additional losses and should be considered in tuned circuit design.

Although monolithic circuit parasitics normally exhibit only minor disadvantages in high frequency amplifiers, their effects can be serious in high frequency oscillator circuits. The parasitic capacitances vary with bias voltage in the same manner as in a varactor diode. The following equation describes this behavior.

$$C = k \frac{1}{(V - V_T)^{1/n}}$$

where:

V = applied voltage (Forward)
V_T = contact potential
(n is a function of impurity grading and normally is between 2 and 3)

At low bias levels where V_T is significant compared to the applied voltage, the capacitance also varies with temperature. This is due to the contact potential's temperature dependence. The contact

DOUBLE - CONVERSION RECEIVER GAIN REQUIREMENTS

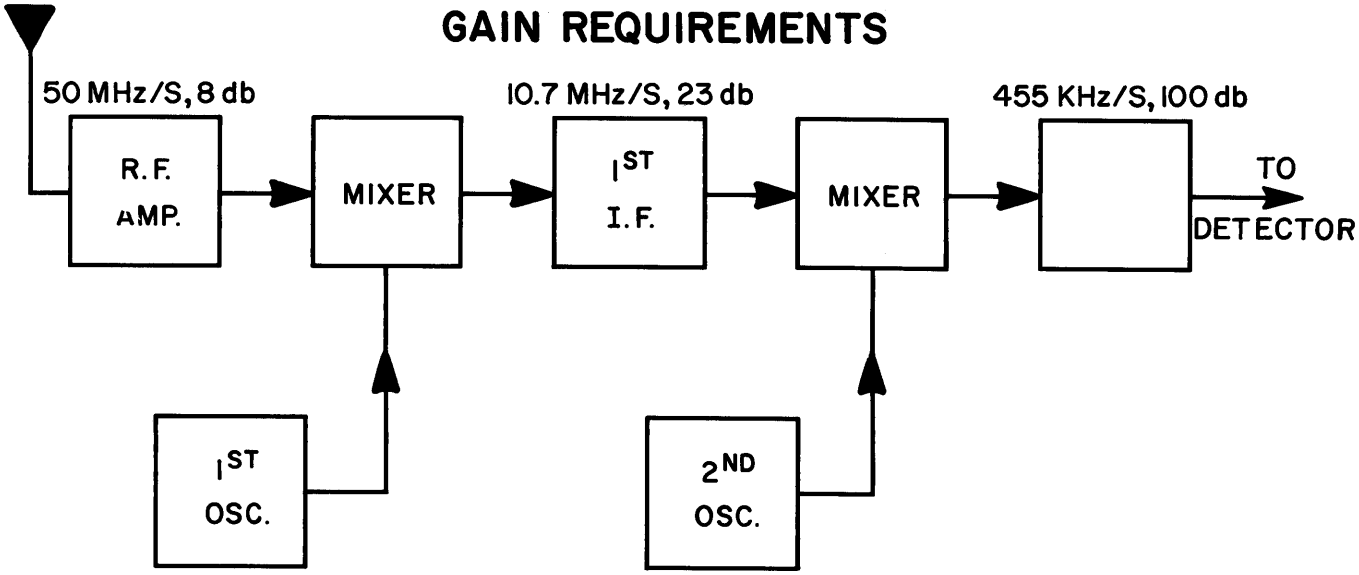


Figure 6-19

L-C OSCILLATOR BUILD FROM BASIC VIDEO AMPLIFIER

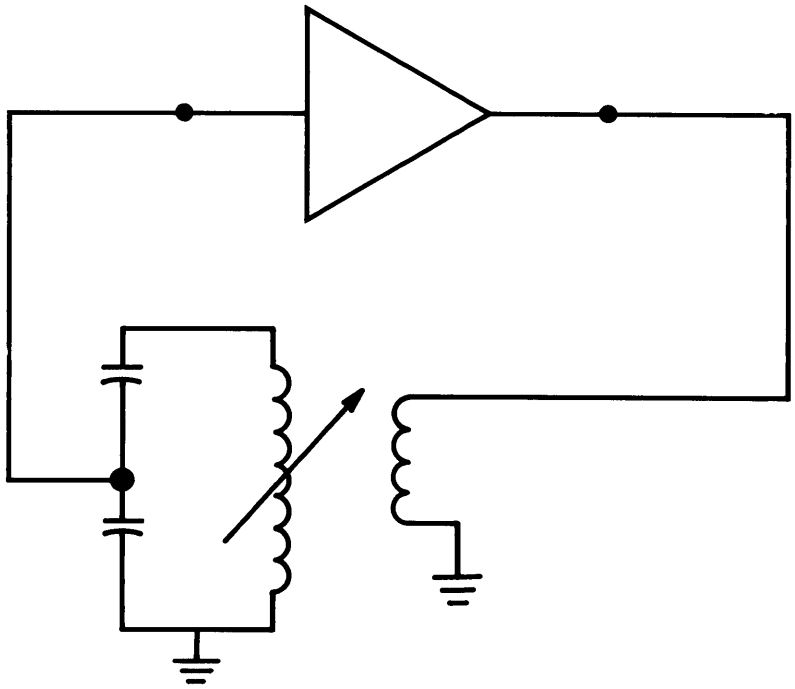


Figure 6-20

DARLINGTON AMPLIFIER CONNECTION

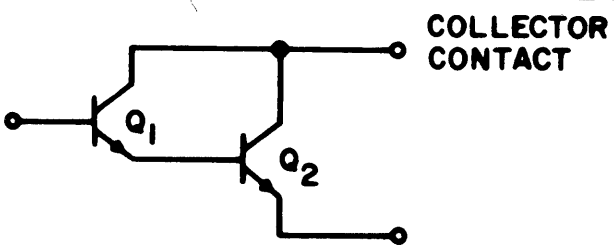


Figure 6-21

6.5.2 (Continued)

potential is given by the following:

$$V_T = \frac{kT}{q} \ln \frac{N_D N_A}{n_i^2}$$

These variations in circuit 'stray' capacitance will cause considerable frequency shift even in crystal controlled oscillators. These effects may be circumvented through the use of grounded collector circuits and either thin film resistors or additional tuned circuits which allow the resistors to be placed at RF ground.

6.5.3 Pulsed Power Supplies

Power output may be increased without increased dissipation by using high efficiency circuit designs such as class D and class B with pulsating DC collector supply. Class D amplifiers operate in a switching mode and use the interval of either pulse width or pulse rate variations to represent an analog signal. Since the transistors switch rapidly between cutoff and saturation (which are both low dissipation states), efficiencies as high as 95% can easily be achieved.

If the amplifier is to be operated at only one frequency (such as a servo amplifier), a pulsating DC supply may be used with a conventional class B circuit to reduce the collector-to-emitter voltage and thus, the dissipation. Figure 6-23 illustrates this type of operation. Since the collector-to-emitter voltage is equal to the difference between the supply voltage and the output voltage, it will approach zero as the output voltage increases. At full output, the transistors are operating as synchronous switches to convert the pulsating full wave DC to an AC wave.

6.5.4 Totem Pole Circuit

Integrated circuits are often used in equipment in which size is an important consideration. It therefore would be desirable to eliminate some of the bulky components (such as transformers) usually associated with power amplifiers. There are several class B, single-ended, push-pull circuits which allow direct connection to the load. Figure 6-24 shows the so-called totem pole circuit. Two versions are shown, one of which uses a split supply to eliminate the output coupling capacitor used in the other. Both require a driver transformer, but eliminate the output transformer.

6.5.5 Designs Eliminating Transformers

Transformers are invariably large and bulky compared to integrated circuit chips. It is usually desirable to avoid their use whenever possible. A modification of the basic totem pole circuit is shown in Figure 6-25. This circuit uses a direct coupled phase-splitter to eliminate the driver transformer. The two halves of the output stage do not have the same voltage gain since one is operating as a common-emitter stage and the other as an emitter-follower. The inbalance is corrected in the phase splitter by making R_1 larger than R_2. Complementary symmetric circuits, such as are shown in Figure 6-26, can also be used to eliminate transformers, but require multichip fabrication techniques at present.

6.6 Digital Circuits Applied to Linear Functions

Digital circuits are available in integrated form in many designs at a relatively low cost. It appears that, for some time to come, they will be available in a larger variety at lower cost than analog or linear circuits. Linear circuit designers will find many opportunities for the use of digital circuits, particularly with the advent of MOS technology.

Rise time in a digital circuit is related to frequency, since both measure the maximum rate of change of voltage with time. The normal definition of rise time is arbitary; the time required for the output to go 10% to 90% of final value when the circuit is driven from a step voltage. The exact form that time response assumes

AMPLIFIER CIRCUIT WITH ALL RESISTORS AT RF GROUND

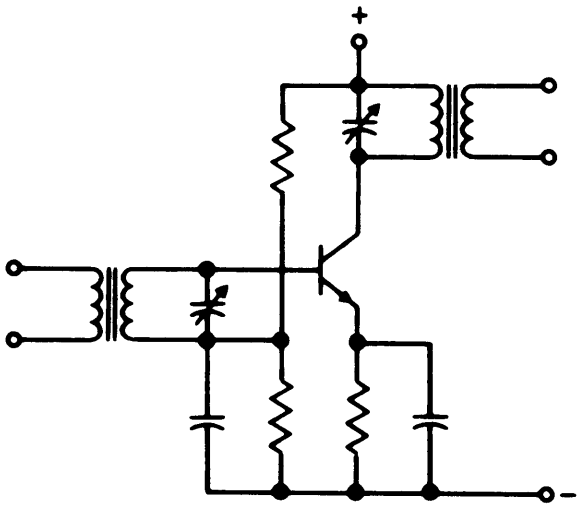


Figure 6-22

METHOD OF REDUCING POWER DISSIPATION IN INTEGRATED CIRCUITS

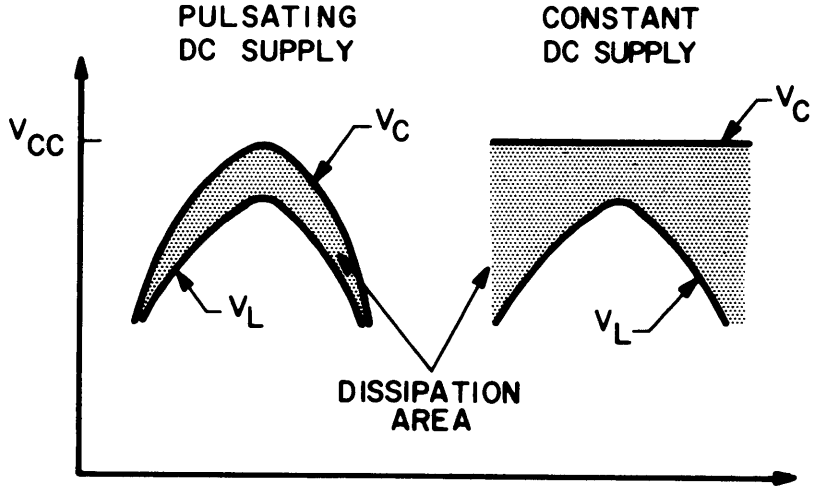
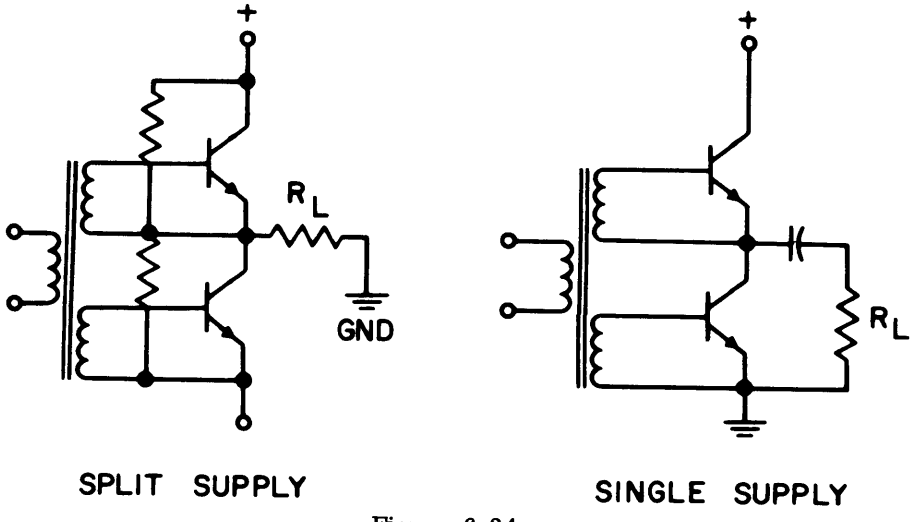


Figure 6-23

"TOTEM POLE" CIRCUITS



SPLIT SUPPLY

SINGLE SUPPLY

Figure 6-24

DIRECT COUPLED PHASE SPLITTER AMPLIFIER CIRCUIT

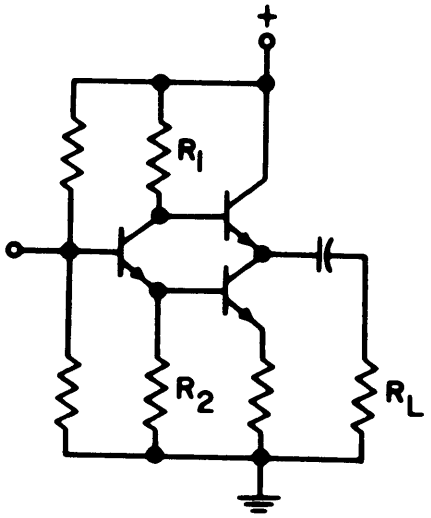


Figure 6-25

COMPLEMENTARY SYMMETRY TYPE OF AMPLIFIER CIRCUIT

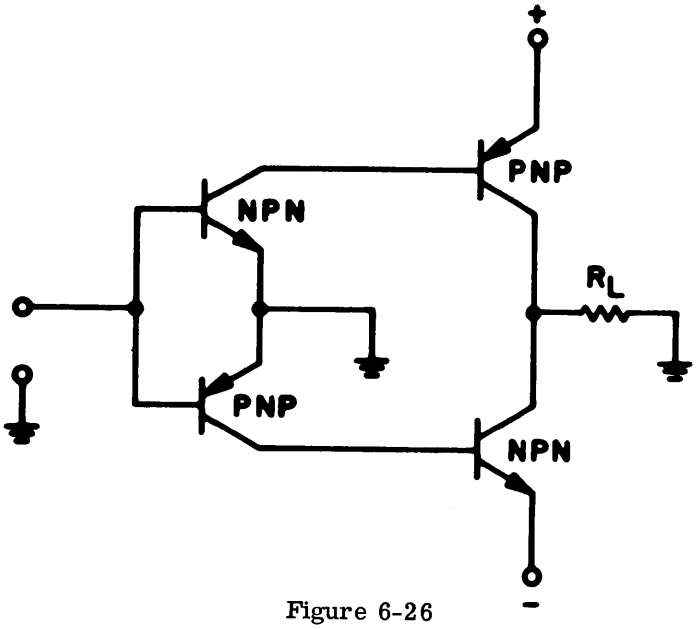


Figure 6-26

6.6 (Continued)

is predictable from a plot of gain versus frequency, but usually one can use the simple relationship:

$$\text{Rise time} = \frac{0.4}{f_U}$$

where f_U is the 3 db bandwidth of the amplifier. Thus, the bandwidth, with switching circuit amplifier, is about 400 MHz divided by the rise time in nanoseconds.

In switching circuits, a quantity comparable to gain can be discovered in the graph showing the transfer characteristics of the gate. Figure 6-27 shows typical input-output characteristics for a gate at different temperatures. The slope of this curve and the linear active region of the transistor, reveals a gain of the circuit when used as a linear amplifier. Since the break points at either end of this linear region reveal the onset of cutoff and saturation effects within the transistor, the graph also shows the dynamic range of the amplifier. Some indication of the amount of nonlinearity is to be expected from certain magnitudes of drive signal can be predicted. The graph also shows the AGC properties of the gate when used as a linear amplifier. If automatic gain control is applied to such a gate, the slope of the transfer characteristics would change revealing the gain changes and also the limits of linear operation. Thus, the effect of the application of AGC on reduction of the dynamic range of the amplifier can be observed. This is an undesirable feature of many AGC circuits. Figure 6-28 shows how the curve changes when AGC modifies the gain of the stage. Here, the dynamic range is reduced about 30% by the AGC voltage.

6.6.1 An Audio Amplifier Using Digital Techniques

Due to the advent of MOS technology, an extremely inexpensive redundancy of transistors, considerable investigation is underway using digital circuits to replace linear functions. One interesting operation in this regard is the pulse modulated audio amplifier. Though this idea was proposed many years ago (about 1930), it has only become practical with the advent of integrated circuits.

The technique employed is called pulse width modulation. It involves class D amplification, using a square wave at a frequency of about 100 KHz to switch an inductive load between the positive and negative terminals of a power supply. If the duty cycle is 50%, no current flows in the load. If the input signal is made to change the duty cycle, a current will flow in the load corresponding to the input signal. The theoretical efficiency is 100%. The high efficiencies thus obtained enables low power integrated circuits to drive large loads. In the past, the major drawback to this method has been the complexity of the circuit required to generate and modulate the square wave. Integrated circuits appear to be able to solve this problem and thus provide a solution to the implementation of high powered integrated audio and servo power amplifier circuits.

6.7 Commercially Available Integrated Circuits

The number and variety of commercial integrated circuits is increasing rapidly. Almost all major suppliers include several of these among their standard product lines. It is particularly instructional to see how the various suppliers are meeting the customer's linear system requirements in integrated form. These have been selected to reflect the variety of different techniques in common use.

6.7.1 Video Amplifiers

The first class of linear circuits, which was available in monolithic form as a standard item, was the RF or video type of amplifier.

TRANSFER CURVE FOR TYPICAL GATE (SLOPE DETERMINES VOLTAGE GAIN)

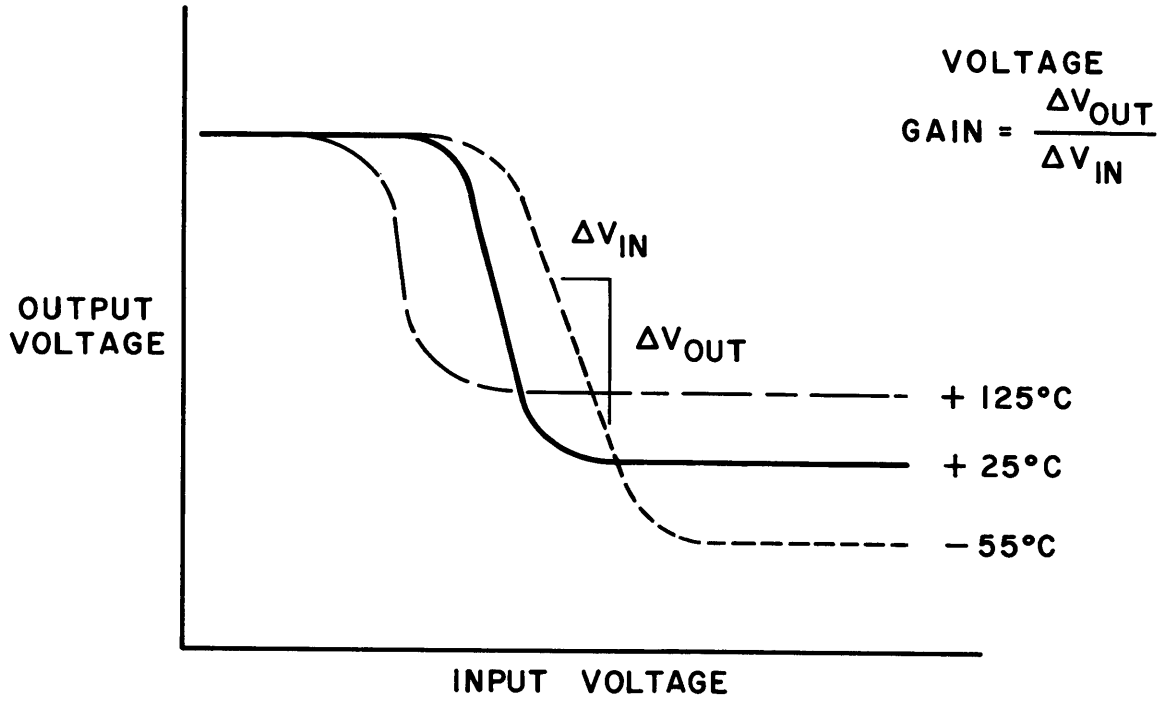


Figure 6-27

APPLICATION OF AGC TO A GATE USED AS A LINEAR AMPLIFIER

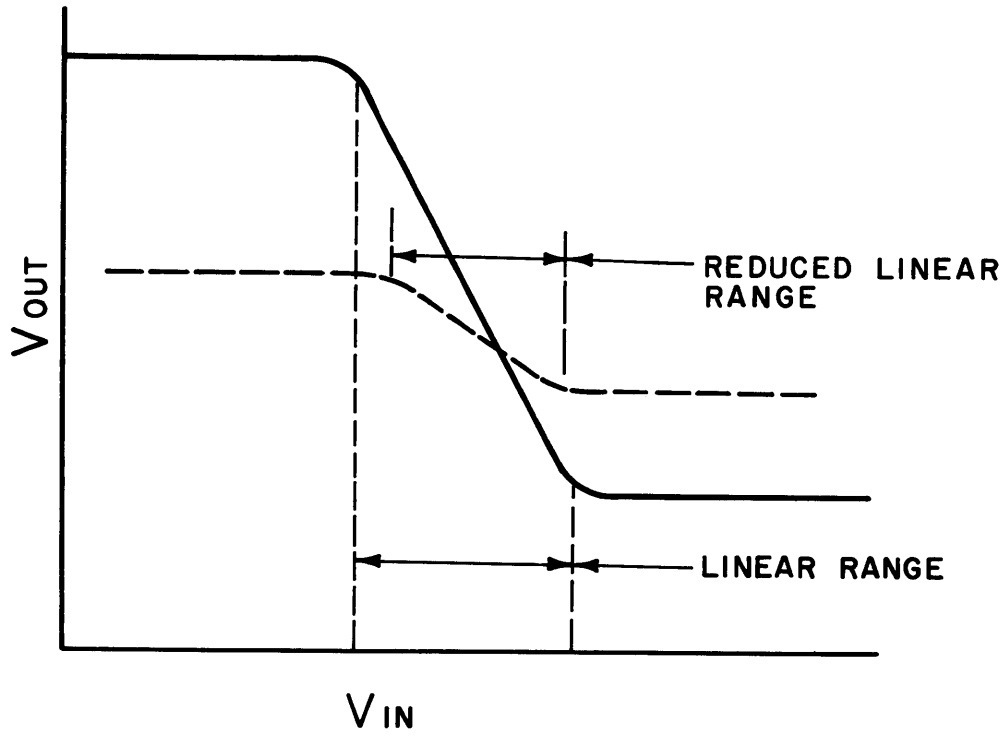


Figure 6-28

6.7.1 (Continued)

Several types of these circuits are now available from various manufacturers. One of the first circuits available was the Signetics SE501 video amplifier, as shown in Figure 6-29. This monolithic circuit was designed as a general purpose direct-coupled, wide band amplifier. The pin connections were designed to permit external adjustment of the amplifier characteristics. The unit has a voltage gain of 100 and an adjustable bandwidth of 10 to 40 MHz.

A typical video amplifier available in integrated form is shown in Figure 6-29. The chip has been designed with versatility in mind, as can be seen from the number of alternate connections available in the feedback network. Curves supplied with the data sheet show that the basic open-loop gain is about 35 db, with a 3 db cutoff frequency of about 3 MHz. This performance is achieved by grounding Terminal 2, connecting Terminals 7 and 8, and taking the output from Terminal 6. For greater bandwidth and lower gain, it is possible to connect Terminal 2 to Terminal 3, thus applying a modest amount of degenerative feedback to the amplifier. The result is a reference gain of 25 db and a bandwidth of 20 MHz. For still larger bandwidth, connect Terminals 3 and 4 together, increasing the negative feedback. The result is a low frequency gain of 18 db with a bandwidth of 40 MHz. These results are shown graphically in Figure 6-30.

Another example of this type of amplifier is shown in Figure 6-31. This unit is a Nippon Electric Company Model μPC3 3-stage direct-coupled linear amplifier. This circuit utilizes a zener diode to stabilize the biasing voltage of the transistors. The circuit has a gain of 20 db with a bandwidth of 24 MHz.

In general, the amplifiers built with integrated circuit fabrication techniques will differ in gain versus frequency properties from their discrete component counterparts. The exact nature of the frequency roll-off at high frequencies depends upon the relative importance of transistor limitations and capacitive effects. However, the capacitances associated with monolithic circuits are different from shunt capacitances in discrete component circuits.

6.7.2 Audio Amplifiers

Audio amplifiers are another class of circuit which has a wide range of applications for a given circuit. One example of this type of circuit, available in integrated form, is the Motorola MC 1524 audio power amplifier, as shown in Figure 6-32. This unit is a multichip circuit which is capable of efficient, low distortion operation with up to 1 watt of audio output from a single TO-5 can. It was designed for miniature battery operated equipment and has low standby current drain. The output is directly coupled to the load, thus eliminating the need for an output transformer. Because of the balanced circuit, negligible DC current flows in the load.

A choice of feedback options provides a variety of gain, distortion and frequency shaping requirements. In a typical operating circuit, the response is flat between 20 cps and 30 KHz.

Another form of hearing aid amplifier is shown in Figure 6-33. This is a Westinghouse WS182 monolithic circuit which is capable of 72 db gain and 3 mW output with a 1.5 volt supply. The circuit is essentially a balanced preamplifier driving a push-pull output stage. Direct coupling is used throughout and separate DC and AC feedback paths are used.

VIDEO AMPLIFIER SE 501G
(Signetics)

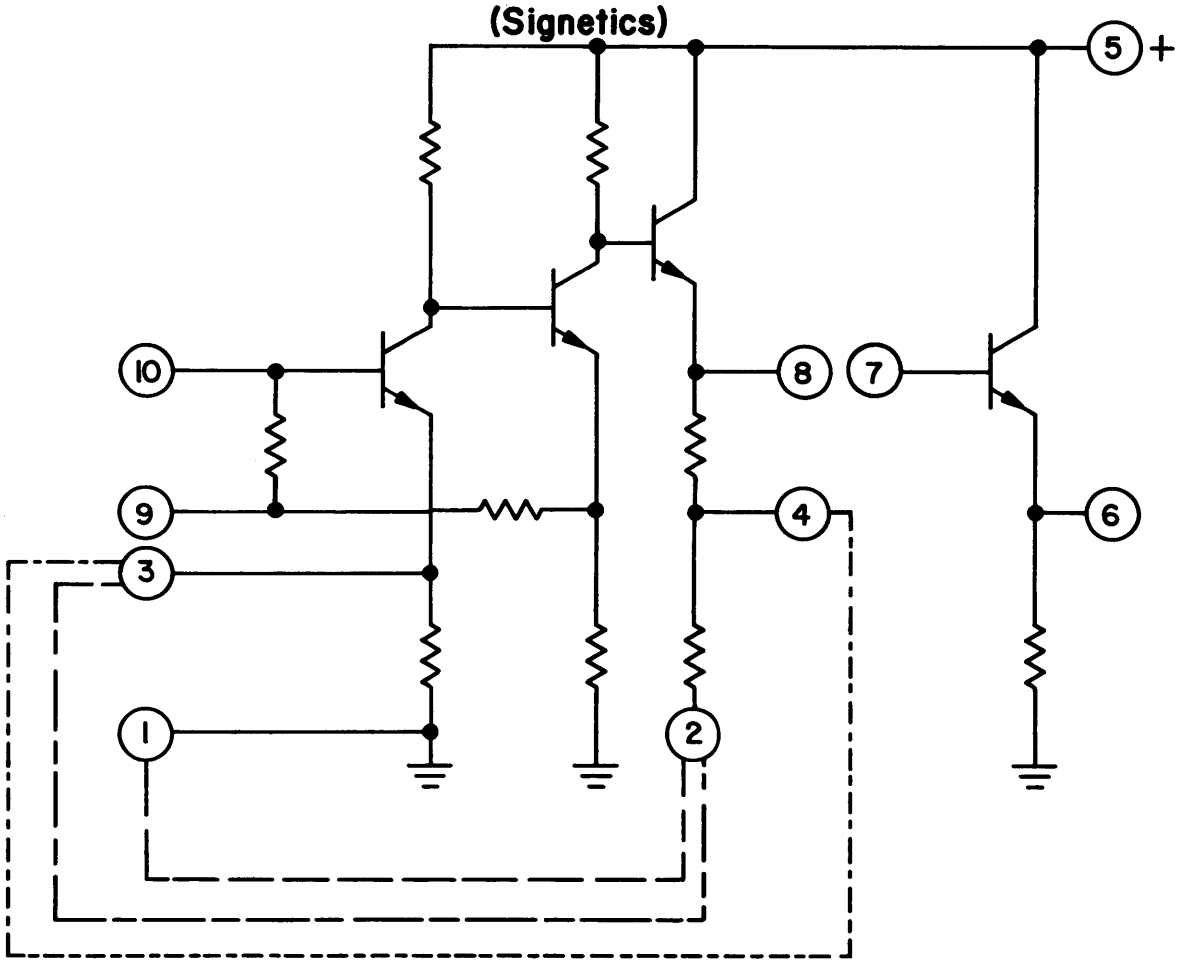


Figure 6-29

RESPONSE CURVES FOR THE SIGNETICS SE 501G
GAIN CAN BE TRADED FOR BANDWIDTH BY MEANS OF ALTERNATIVE CONNECTIONS OF THE MODULE

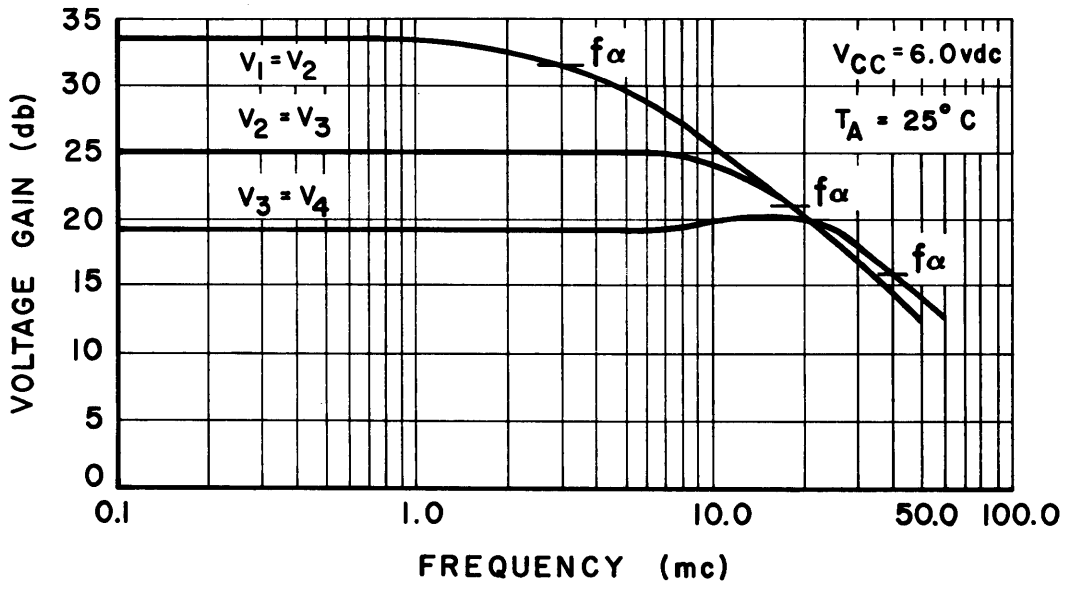


Figure 6-30

VIDEO AMPLIFIER μPC3

(Nippon Electric Co.)

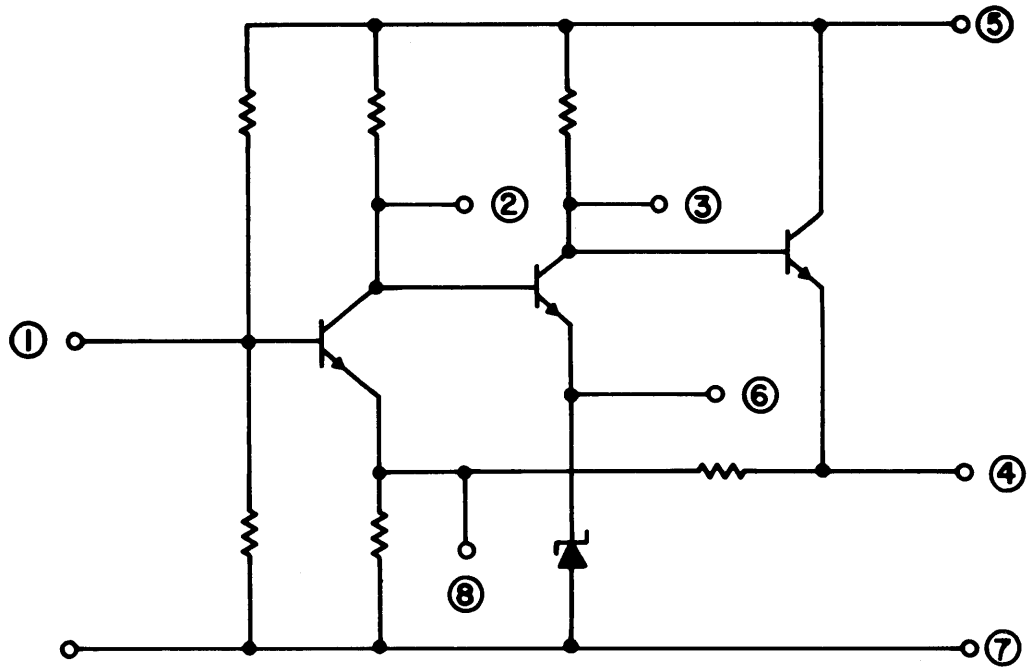


Figure 6-31

AUDIO POWER AMPLIFIER MC 1524

(Motorola)

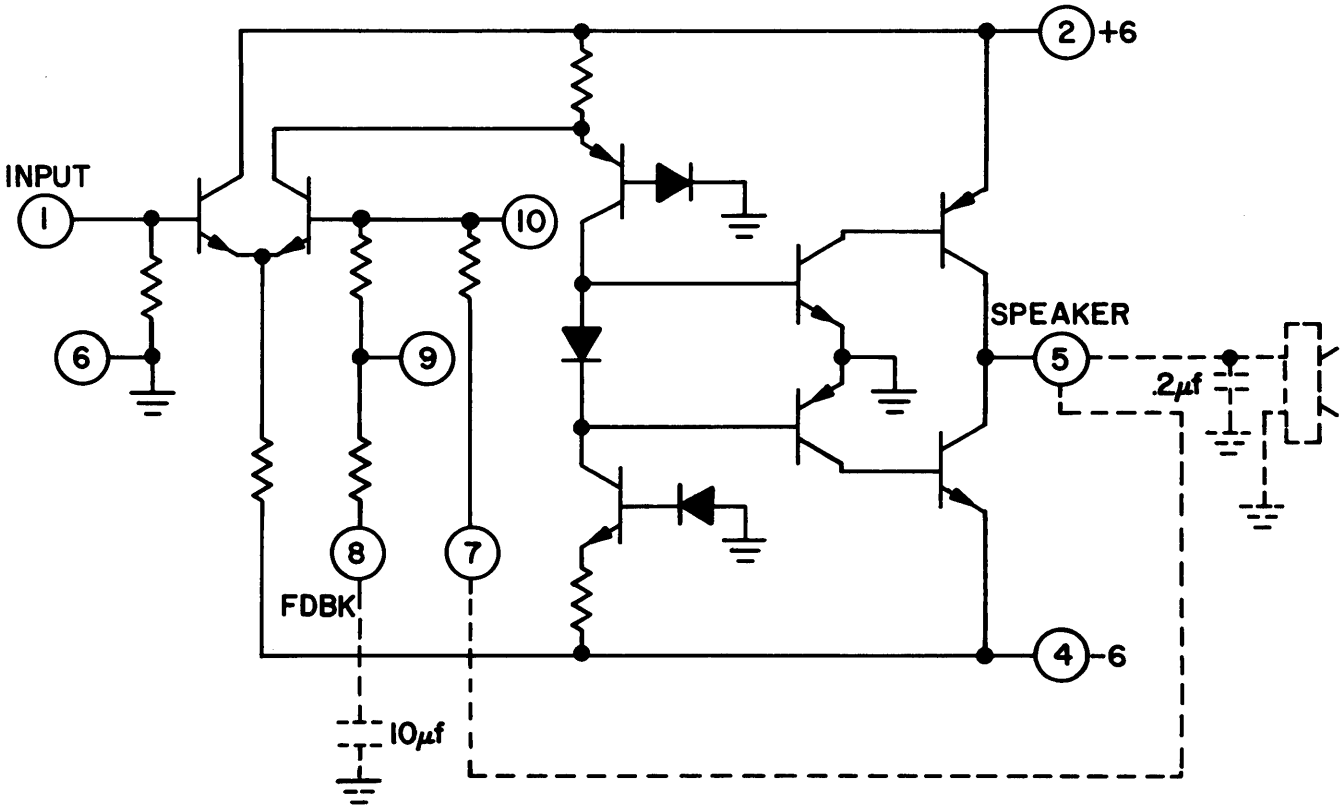


Figure 6-32

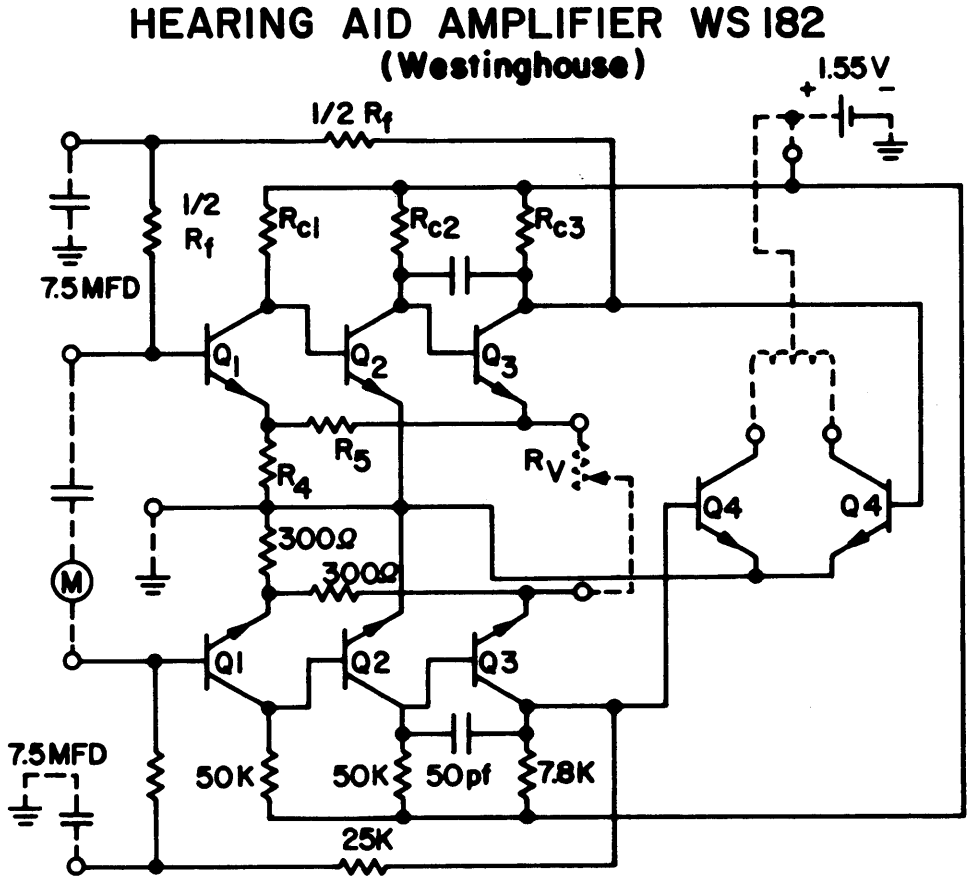

HEARING AID AMPLIFIER WS 182
(Westinghouse)
1.55V
+
-
1/2 Rf
1/2
Rf
7.5MFD
Rc1
Rc2
Rc3
Q1
Q2
Q3
R5
R4
RV
300Ω
300Ω
M
Q1
Q2
Q3
Q4
Q4
7.5MFD
50K
50K
50pf
7.8K
25K

Figure 6-33

6.7.3 Differential and Operational Amplifiers

The third class of linear circuits that offers a large number of applications for standard items is the differential operational amplifier. By utilizing various external connections and feedback loops, a basic amplifier circuit may be used for a variety of applications.

One example of this type of circuit is the Texas Instruments SN5510 operational amplifier, as shown in Figure 6-34. This unit has an open-loop gain of 40 db and a flat frequency response to 40 MHz. It offers both differential inputs and differential emitter-follower outputs. Its differential voltage gain is typically 46 db with common mode rejection of 60 db.

Another example of an operational amplifier is a Fairchild μA702A DC amplifier, as shown in Figure 6-35. This monolithic unit is intended for use in analog computers, or as an intrumentation amplifier. It has an open-loop voltage gain of 2600 and a bandwidth of 30 MHz. Also offered by Fairchild is a μA709 which has an open-loop gain of 50,000 (This is with a bandwidth of 1 MHz), see Figure 6-36.

Figure 6-37 shows a low level differential amplifier made by Amelco. It consists of five NPN transistors and associated resistors constructed in monolithic form. The manufacturer states that thermal coupling is tight and that there is close V_{BE} with common mode feedback, resulting in extremely low drain and excellent stability. It has a bandwidth of 400 KHz and differential gain up to 2,000.

6.7.4 Servo Amplifiers

The Norden Company has developed a series of integrated circuits for servo applications. The family includes both monolithic structures and multichip arrangements to achieve high power capabilities. Figure 6-38 is a monolithic error amplifier circuit capable of dissipating between 120 and 350 mW safely.

This circuit primarily is intended for use in regulating power supplies and includes automatic short-circuit protection and overload protection. Other members of this family are capable of from 5 to 40 watts of output.

6.7.5 Television Circuitry

Admiral Corp and RCA are using integrated circuits in their newest line of television receivers. Zenith has indicated that their use is 'near at hand.' RCA has combined IF amplification, limiting, FM detection and audio amplification on a single chip monolithic integrated circuit (Figure 6-39). Several external components are employed as well as a series of PN junctions to perform the filter capacitor function. Adding to the interest in this and closely related types of circuits is the RCA pricing which in thousand quantities ranges from $1.25 to $3.15.

TYPE SN5510 MONOLITHIC WIDEBAND VIDEO AMPLIFIER

(Texas Instruments Inc)

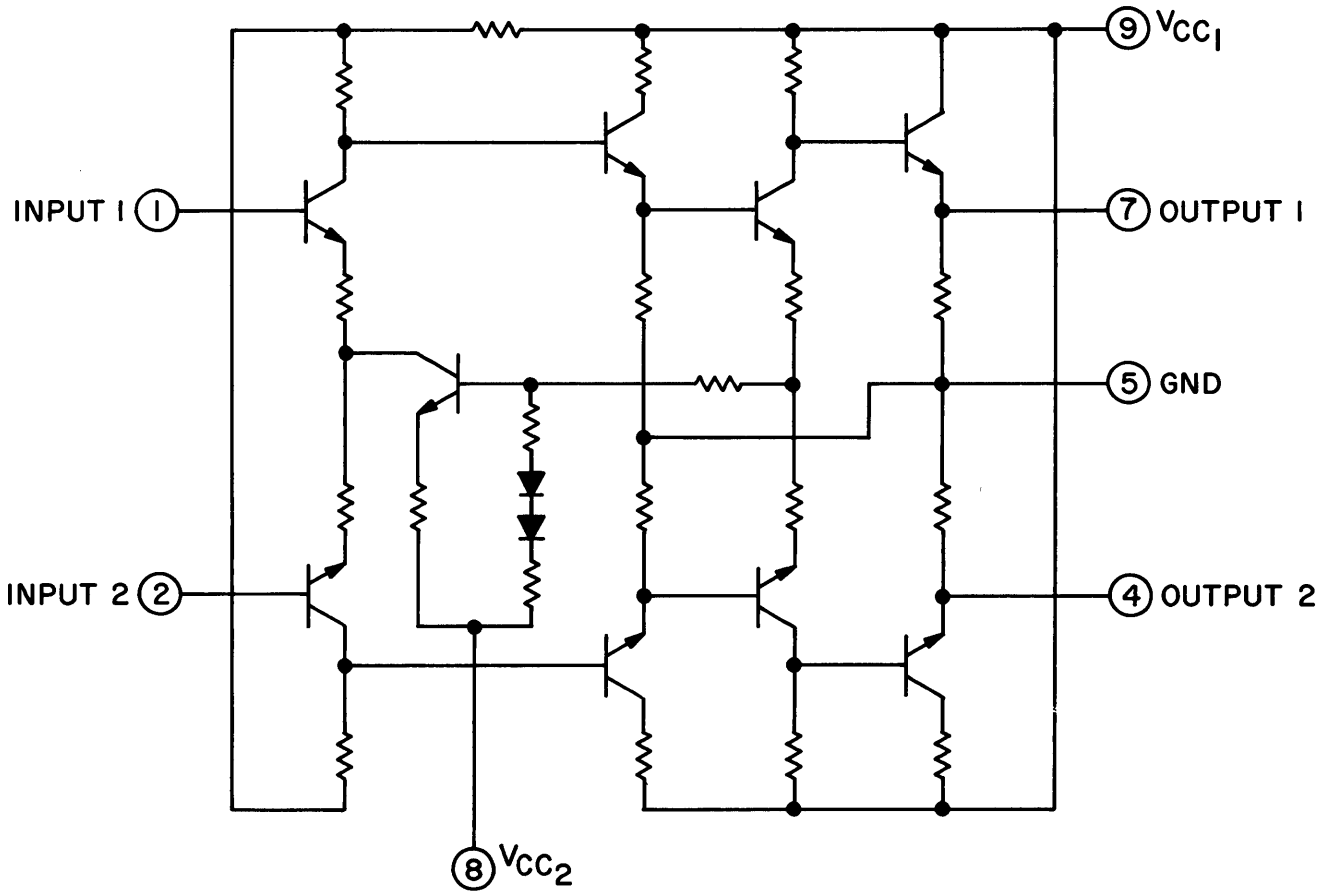


Figure 6-34

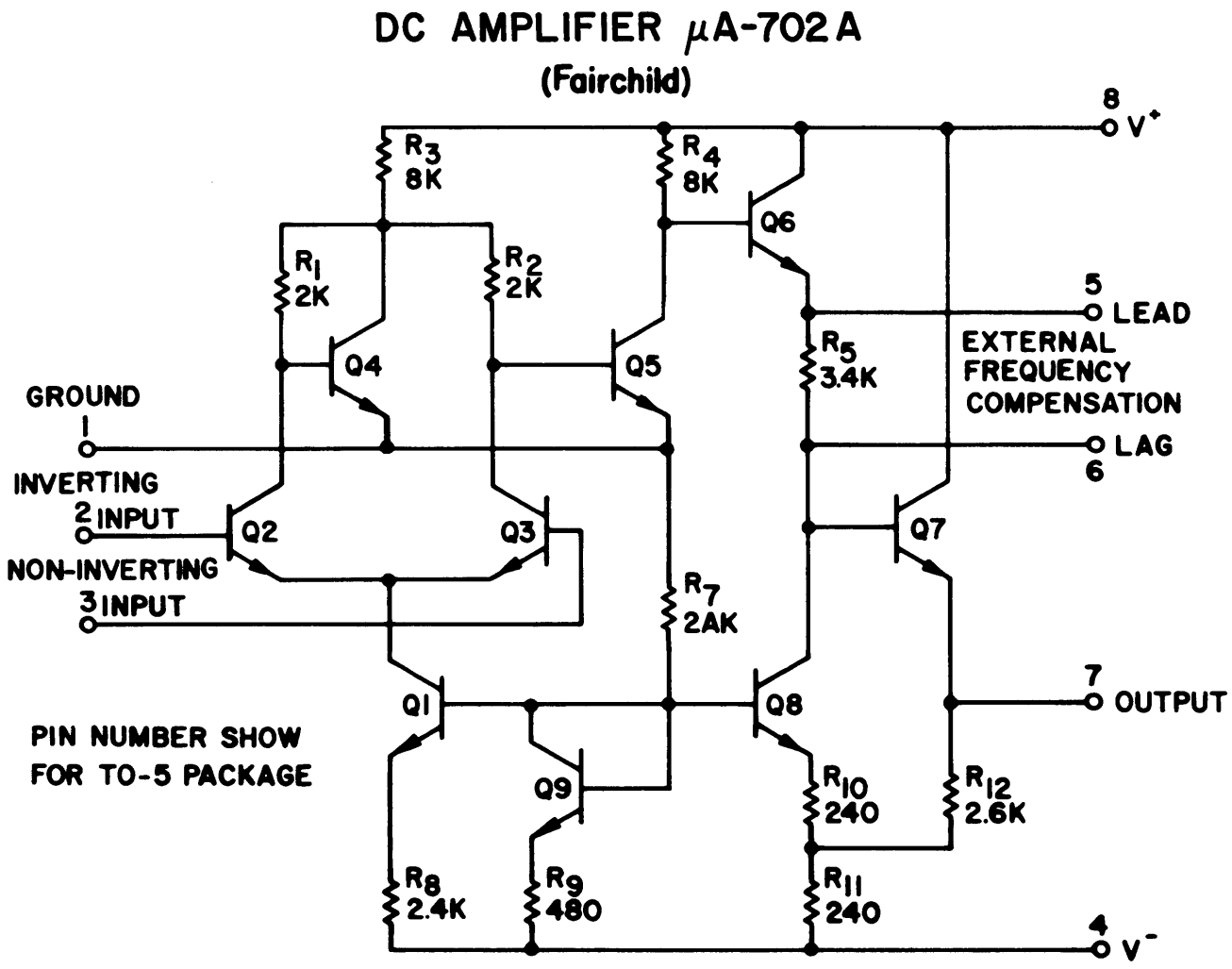

DC AMPLIFIER μA-702A
(Fairchild)
8
V+
R3
8K
R4
8K
Q6
R1
2K
R2
2K
5
LEAD
Q4
Q5
R5
3.4K
EXTERNAL
FREQUENCY
COMPENSATION
GROUND
1
LAG
6
INVERTING
2 INPUT
Q2
Q3
Q7
NON-INVERTING
3 INPUT
R7
2AK
7
OUTPUT
Q1
Q8
PIN NUMBER SHOW
FOR TO-5 PACKAGE
Q9
R10
240
R12
2.6K
R8
2.4K
R9
480
R11
240
4
V-

Figure 6-35

μA 709C OPERATIONAL AMPLIFIER (Fairchild)

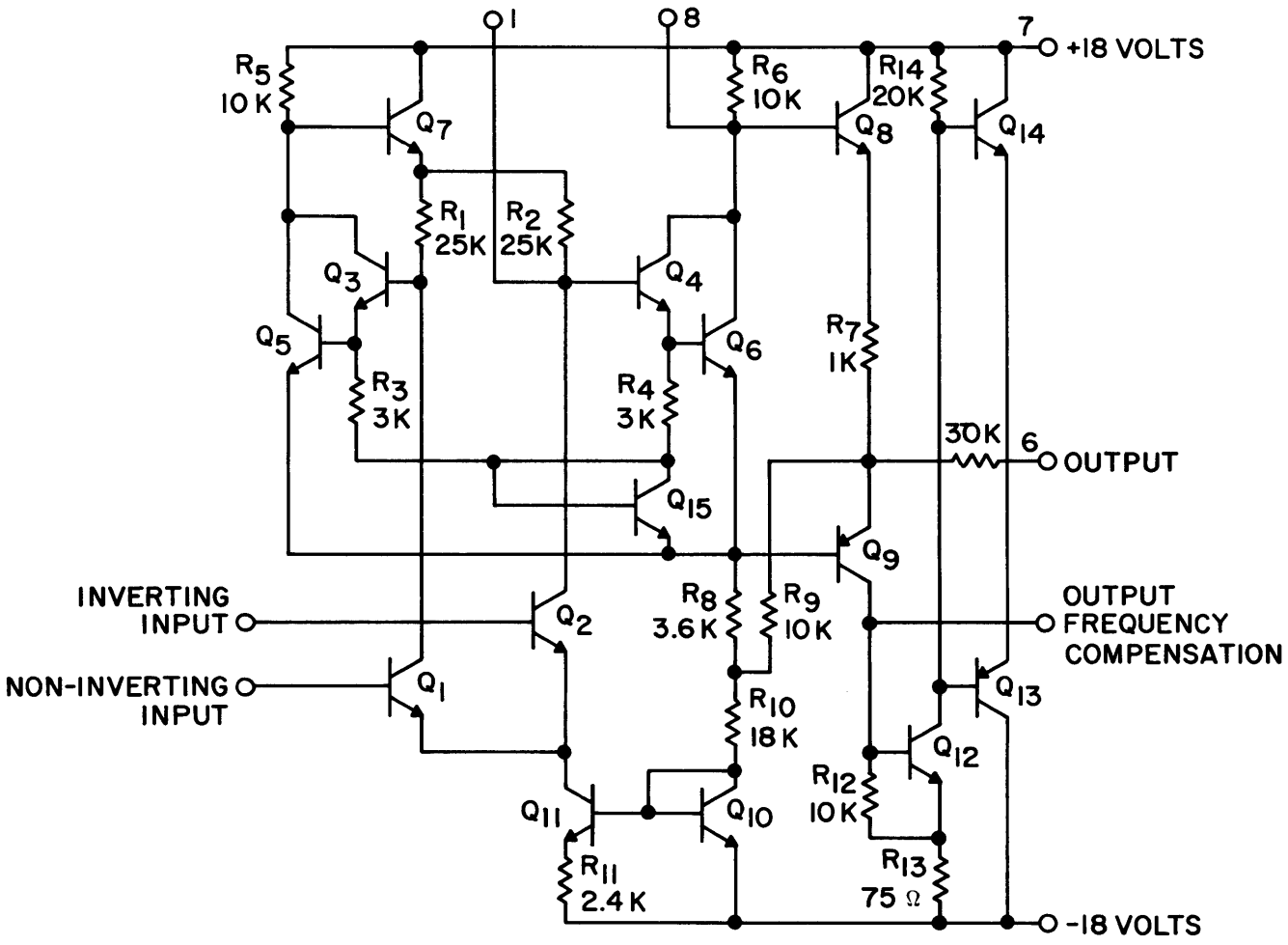


Figure 6-36

DIFFERENTIAL AMPLIFIER D13-000
(Amelco)

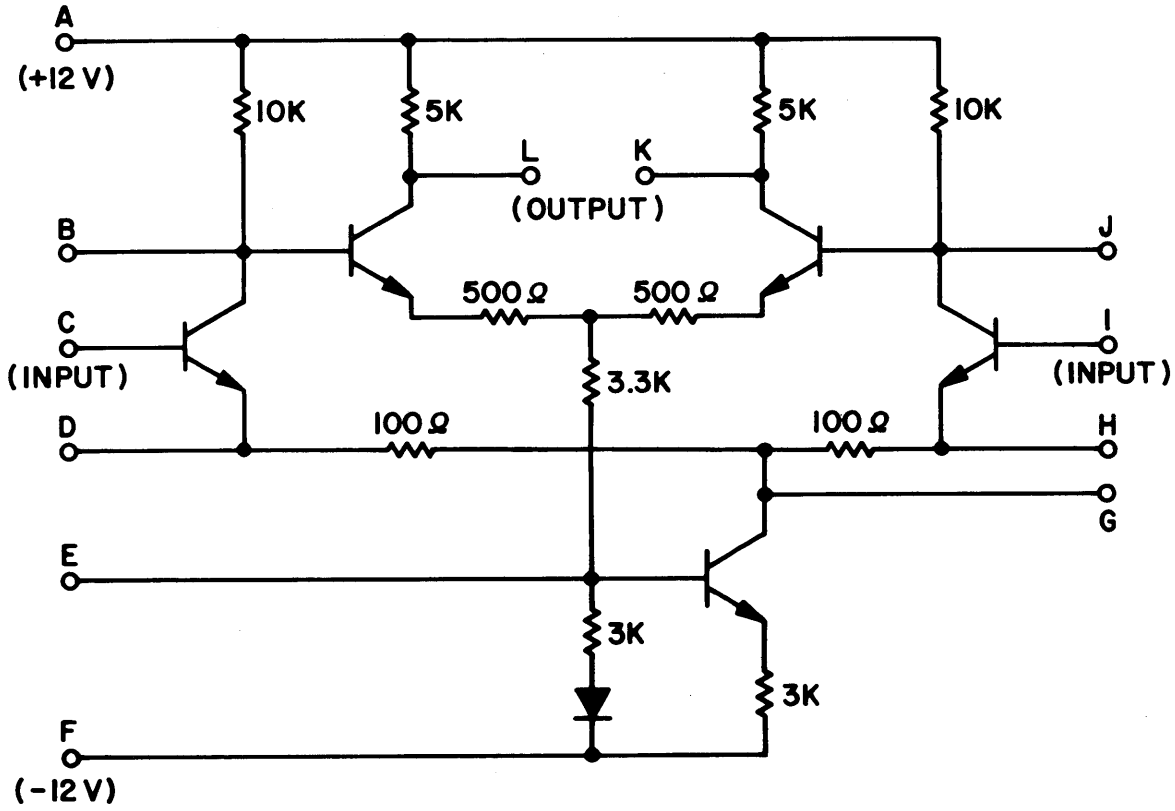


Figure 6-37

ERROR AMPLIFIER NM-1004
(Norden)

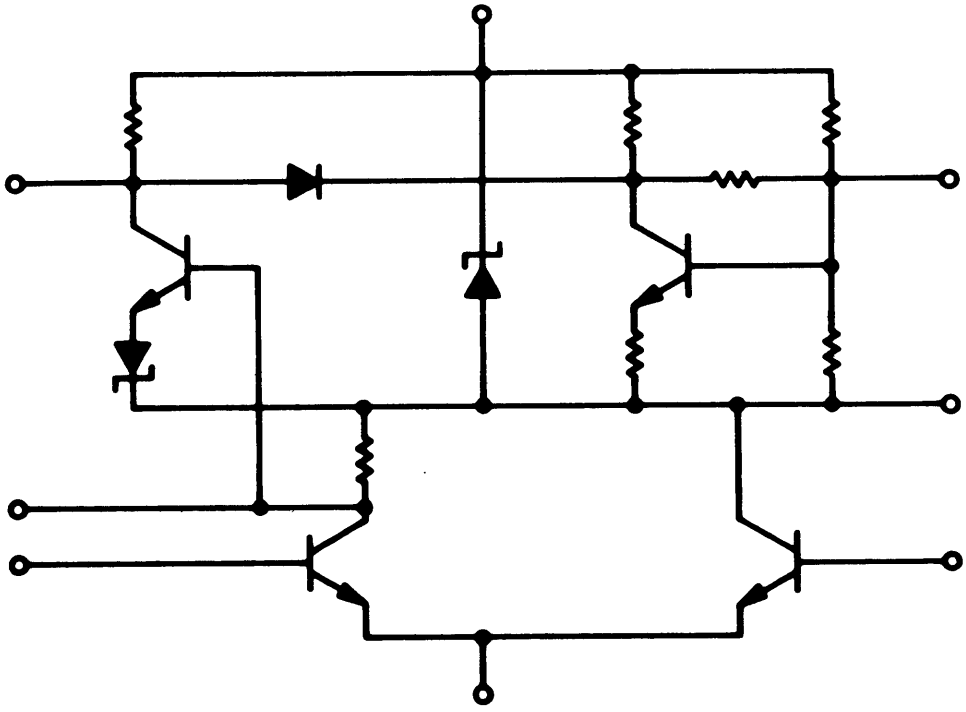


Figure 6-38

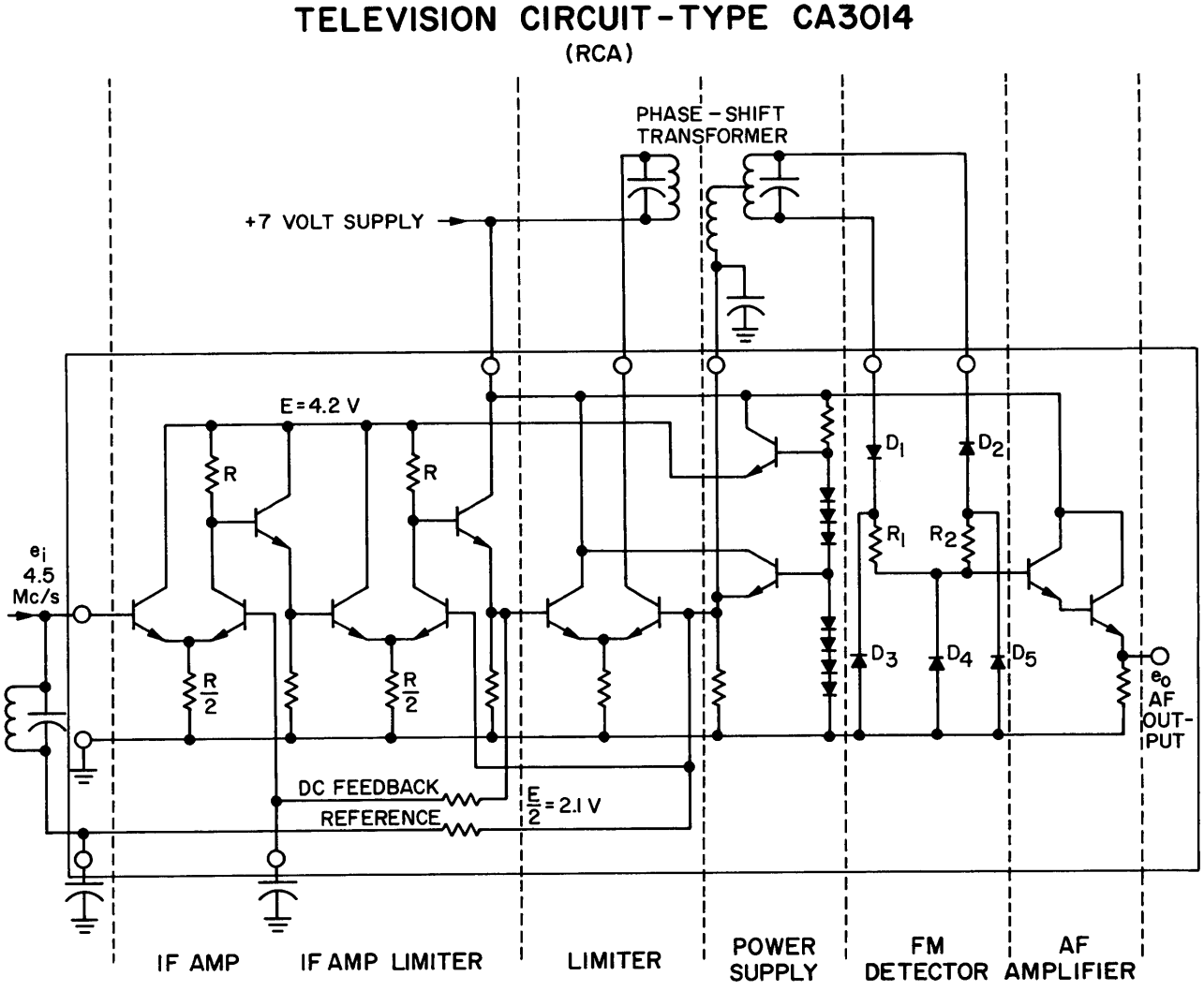

TELEVISION CIRCUIT-TYPE CA3014
(RCA)
PHASE-SHIFT TRANSFORMER
+7 VOLT SUPPLY
E=4.2 V
R
R
e_i 4.5 Mc/s
$\frac{R}{2}$
$\frac{R}{2}$
DC FEEDBACK
REFERENCE
$\frac{E}{2}$ = 2.1 V
D_1
D_2
R_1
R_2
D_3
D_4
D_5
e_o AF OUT-PUT
IF AMP
IF AMP LIMITER
LIMITER
POWER SUPPLY
FM DETECTOR
AF AMPLIFIER

Figure 6-39

SECTION 7 THE VENDOR-USER INTERFACE AND SPECIFICATION

7.0 Introduction

Integrated circuits are changing the nature of the vendor-user interface. The integrated circuit supplier is not simply a parts supplier, but rather a subcontractor. As such, he participates in the design at the systems, subsystems and circuit levels from the project inception through production. In his liaison capacity, the marketing specialist must work effectively, not only with the designers and purchasing, but also with standards and quality control personnel.

Design Phases

This method of operation actually varies considerably as a function of the personalities of the people involved and their areas of activity such as Military, commercial, or entertainment. The marketing specialist's function also varies materially through the four basic phases of the design.

1. Systems conceptional design
2. Prototype design
3. Engineering design and evaluation
4. Production.

Timing

Timing may require that several of these stages of design be telescoped together or at the other end of the spectrum, protracted. Major factors involved in the vendor-user interface determine the marketing specialist's relationship with the aforementioned personnel have been materially changed by integrated circuits.

The basic function involves making sales and assuring profits for his own company while helping the customer to look good. This is just as true with integrated circuit sales as with any other commodity. Also the old saying, "It's always easier to sell what you haven't got" holds in this area.

In this section, the areas and ways in which the vendor-user interfaces are modified, between discrete components and integrated circuits, will be enumerated.

7.1 Systems Conceptual Design

It is mandatory that the integrated circuits specialist establish communication with the designers from the inception of the systems design. He must provide application data and background information. His own training must be technically sufficient to intelligently evaluate the problem of feasibility and direct the design activity toward his products. He must, in addition, have the support of his home office and sufficient additional applications information on his own products and development work to adequately service the special needs of his client. In this area, he must be aware of new product development schedules and design objectives. His goal, to help customers attain optimum designs for their continuing success, must also be his concern. In this endeavor, he must anticipate and communicate the likelihood of any special circuit design becoming a standard which will have substantial future advantages, or whether it will probably become obsolete. The prospect of future sales makes dangerous absolute adherence to the dictum of "Let the Buyer beware".

Begin Specifications Negotiations

It is in the systems conceptual design area that specifications negotiations must be started. This area of work is mostly technical, adding to that already performed by the marketing specialist and the customer's design engineers.

7.2 Prototype and Engineering Design

The most important change brought about by integrated circuits to component marketing is being felt during the prototype development phase of design. As Tom Cooper of Electronics Procurements said, "The integrated circuit, is by its nature, a specialized device.

7.2 (Continued)

Once your equipment is committed to a particular circuit or even to a particular design concept, much of the opportunity for good buying is past. The cost of redesign in order to change a vendor will outweigh all but the most blatant violation by suppliers. At the present time, it appears that the competition among integrated circuit manufacturers will be manifest during the design stage – not at production time."

Cost of Redesign

Education

To assure achieving his desired sales objectives, the marketing specialist must educate both the design engineers and purchasing agents in the sophistication of integrated circuits. Invariably with any product, the truely knowledgeable customer is easier to work with. However, integrated circuits make it mandatory that the designers give up some of their numerous prerogatives long exercised while designing with discrete components. A major barrier to doing this is overcoming the reluctance of the designer to fully reveal his plans and requirements to outsiders. Complete and accurate information is necessary if the marketing specialist is to provide the kind of support necessary to achieve the best technical as well as the most economical designs.

Small Quantity Orders

Engineering development is characterized by small quantity orders and large numbers of special circuit design requests, many of which are usually in the state-of-the-art category. The total cost of serving such requests is astronomical. Adding to this cost is the large risk involved with whether or not a given project may ever come to fruition, or the chance of "Big" production never coming. These considerations have forced many suppliers to do their own integrated circuit prototype design work secretly or only for preferred customers whose past performance indicated that the risk is less. Because small quantity orders involve only a limited number of dollars, there is also the grave problem of them being lost at the factory or given very low priority compared to the larger more profitable production orders. However, it should be born in mind that these small orders, despite all their nuisances and profitability problems, are the keys to the larger production orders.

7.3 Production

When an integrated circuit equipment has entered production, the marketing specialist must deal primarily with the purchasing department. Integrated circuits have caused a trend toward "Team Purchasing" in which the purchasing agent, design engineer and quality control or component engineer are all involved.

Team Purchasing

Second Source

Production requires scheduled component delivery to a clearly stated set of specifications after the product and vendor have been qualitifed. In many areas, the sales opportunity, to support large productions, is enhanced by having a second source of supply, and interchangeability. Even in this area, a major problem may exist in which the specifications for several different, company products may be identical, minor proprietary production technique differences cause slight variations. These frequently manifest themselves in ways which cause differences in operation which are intolerable in the final equipment. One instance of this occurred when one supplier used an MOS type integrated capacitor while the second used a P-N junction type. The latter, being voltage variable and more temperature sensitive, caused oscillation. During production, specification waivers and engineering changes can become extremely difficult and very expensive. These problems are more extensive with specially designed than standard circuits. It is far better for the equipment designer to employ standard circuits wherever possible. Usually, if he exercises ingenuity in making various kinds of interconnection arrangements of the standard products, he can achieve his design objectives. The use of standard parts will help to assure maintaining production schedules.

Engineering Changes

7.4 Price Negotiations and Contracts

Price Trends

Integrated circuits have been changing more rapidly than most other segments of the electronics market. Technical innovations and yield improvement have been largely responsible for these gyrations. Their rapid acceptance and high volume production have stabilized sufficiently so that reasonable price projections can now be made. Their past history of periodic shortages has led to long term lumped requirement delivery contracts based on these projected prices. The annual sales contract has resulted. Figure 7-1 indicates the trends in pricing and projections. The upper line indicates the industry average selling price as a function of time. The lower part of the figure indicates the average projection for future delivery. The dotted line shows that whereas the then current industry average selling price in 1965 was $10., the projection for delivery in 1967 is $3. The basis for this technique and proper pricing requires accurate projection of the improvement in production techniques and volume production cost advantages to be made. The latter part technique involved here is illustrated in more detailed form in Figure 7-2. The factors which in sum aggregate the actual cost as a function of volume are considered. The factory and direct labor cost overhead plus engineering and start-up cost plus management sales and overhead plus the important area of profit and taxes are taken into consideration in plotting a minimum selling price for the function of production volume.

Price Projections

Future Delivery

In establishing the price, cost projections take into consideration these larger volumes at the future dates. Having to negotiate prices on integrated circuits as with any other commodity, it is necessary to have exact specifications as well as accurate assessment of quantity requirements. To a great extent, competition will exert increasing influence on the establishment of prices. The trend in integrated circuits and semiconductors has accelerated toward long term contracts to encourage increased usage and assure the volume necessary to profitability.

Cost of Reliability Assurance

One of the most controversial areas of price negotiation involves the cost of reliability assurance. The extremely high reliability of integrated circuits requires costly testing and evaluation procedures to assure these reliability levels. The controversy involves the payment of the cost of this reliability assurance and who should pay for it – the supplier or the user. Price differentials between commercial and military products where the only important differences are reliability and quality assurance frequently involve ratios as high as four and five to one. Until recently, most military contractors were willing to pay the price of this reliability assurance. Increasing competition and higher costs in this area, however, are making equipment suppliers less willing to pay the cost and the integrated circuit suppliers are more reluctant to commit large parts of their staffs to conducting the evaluations.

7.4.1 Standard Procurement Terms and Conditions

Standard conditions of sale are normally put on the reverse sides of purchase orders. Although they are usually ignored, their content should be reviewed. Companies involved with extensive government contracts usually employ a government-developed format. This common set of terms and conditions with one exception, appear to be generally acceptable with integrated circuits. The one exception is paragraph No. 4 as follows:

> "No. 4 Changes: Buyer may at any time, by written order, and without notice to the sureties, make changes within the general scope of this purchase order, in any one or more of the following: (I) Drawings, designs, or specifications, where the supply is to be furnished or to be specially manufactured for Buyer in accordance therewith; (II) Method of shipment or

BID AND SELLING PRICES AS FUNCTIONS OF TIME

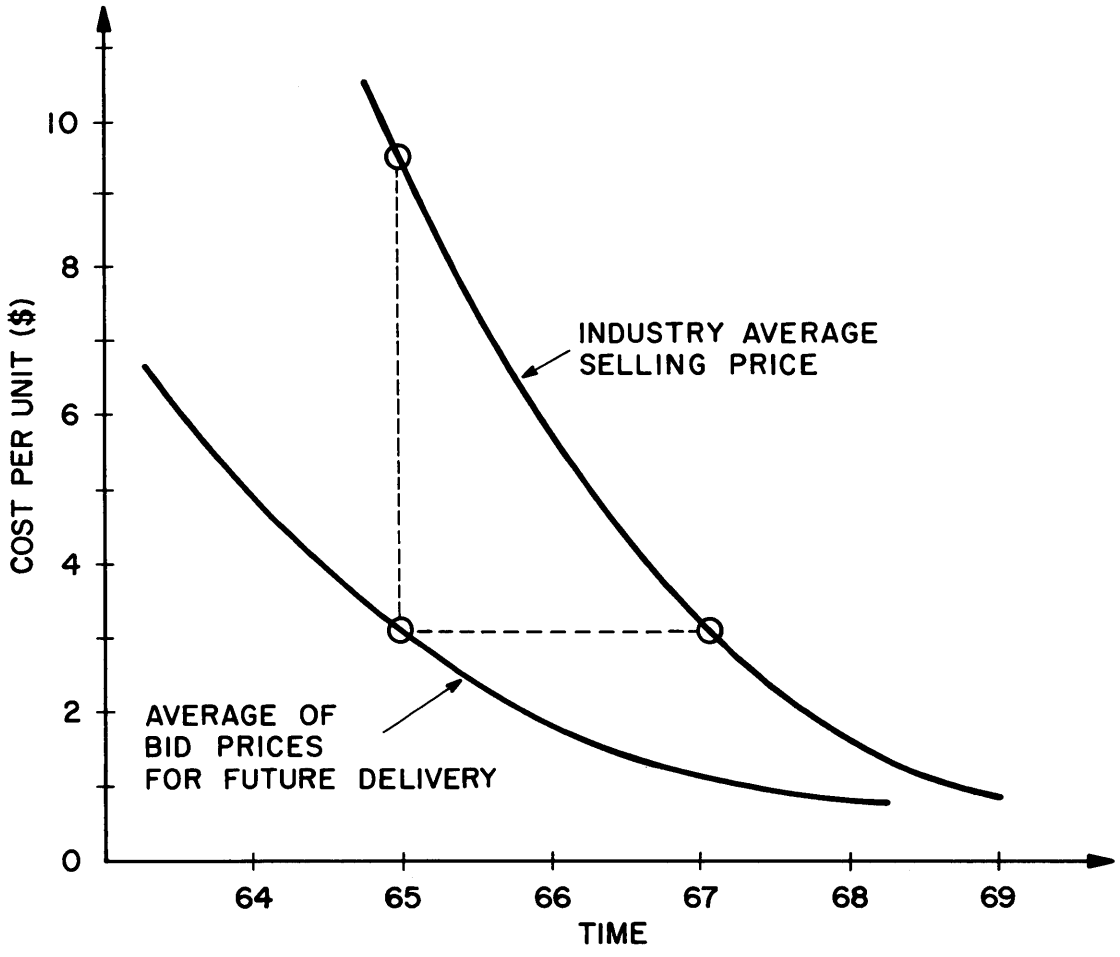


Figure 7-1

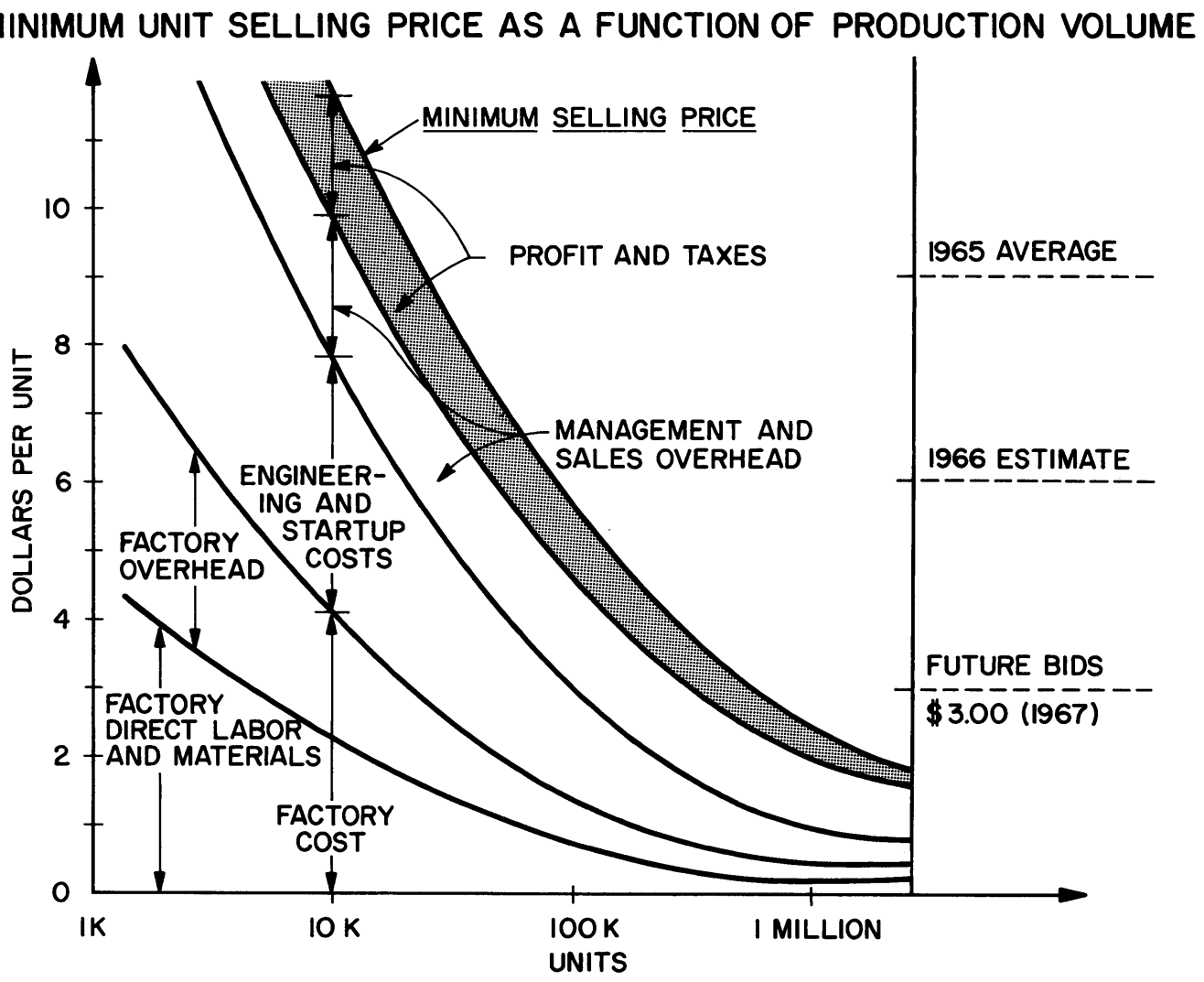

MINIMUM UNIT SELLING PRICE AS A FUNCTION OF PRODUCTION VOLUME
MINIMUM SELLING PRICE
PROFIT AND TAXES
MANAGEMENT AND SALES OVERHEAD
ENGINEER-ING AND STARTUP COSTS
FACTORY OVERHEAD
FACTORY DIRECT LABOR AND MATERIALS
FACTORY COST
1965 AVERAGE
1966 ESTIMATE
FUTURE BIDS
$3.00 (1967)
DOLLARS PER UNIT
0
2
4
6
8
10
1K
10 K
100 K
1 MILLION
UNITS

Figure 7-2

7.4.1 (Continued)

packing; (III) Place of delivery; (IV) The period of performance of work, and Seller shall comply therewith. If any such change causes an increase or decrease in the cost of, or the time required for the performance of any part of the work under this purchase order, whether changed or not changed by any such order, an applicable adjustment shall be made in the purchase order or price delivery schedule or both, and the purchase order shall be modified in writing accordingly. Any claim by Seller for adjustment under this clause must be asserted within thirty days from the date of receipt by Seller of the notification of change, provided, however, that Buyer, if it decides that the facts justify such action, may receive and act upon any such claim asserted at any time prior to final payment under this purchase order. Where the cost of property made obsolete or excess as a result of a change is included in Seller's claim for adjustment, Buyer shall have the right to prescribe the manner of disposition of such property. Failure to agree on any claim for equitable adjustment under this clause shall be a dispute and Seller may thereupon pursue any remedy which it may have in any court of competent jurisdiction. Pending the resolution of any such dispute, the Seller shall diligently pursue the performance of the purchase order as changed. Except as expressly provided for elsewhere in this purchase order, the parties agree that there shall be no adjustment in the price or time for performance hereunder, unless an authorized representative of Buyer's purchasing department shall have directed a change hereto by the issuance of a written change order."

To comply with this clause is almost impossible for any vendor of custom integrated circuits. Process changes drastically alter yields, life and reliability. If required, the wording of this clause should be restructured to provide for (a) change feasibility studies, (b) increased time limits, (thirty days is not reasonable), (c) establishment of cost and evaluation responsibilities, (d) price renegotiations.

7.5 Standard Integrated Circuits versus Specials

Rapid development of the integrated circuits state-of-the-art has presented many problems. Equipment requiring further state-of-the-art improvements is being developed. Much of this effort is dependent upon laboratory samples available only at extremely high costs. Long periods frequently may be involved in obtaining engineering samples if they become available at all. Subsequent production of integrated circuits like the samples is equally problematical. In some cases, state-of-the-art samples become standard production units. In other cases, they may be discarded, obsolete, or proven impossible to produce economically and thus impossible to obtain. In either event, large risks are involved and close cooperation, between supplier and user, is mandatory.

State-of-the-art Samples

Economics

The economics of any design decision will invariably recommend the use of standard integrated circuits, if available. This may extend to major modification of the system design to accommodate standard circuits. The only exception to this is the instance where the production potential of the system is great enough to make any custom circuit into a standard. Even then, economics dictates that the custom circuit be capable of production at high yield levels. There are, however, many systems which are so far advanced that they are incapable of employing currently available standard circuits. In these instances in which the supplier has integrated circuits in advanced development with the likelihood of their going into production, it would seem reasonable to consider them for use. Mutual confidence between supplier and user is required, as well as adequate communications, since proprietary plans of one or

7.5 (Continued) both parties may be involved.

Production Planning

The basic decision between use of special or custom integrated circuits versus standards is closely related to timing. Custom circuits today may be standards tomorrow. To make this decision intelligently requires knowledge of the state-of-the-art circuit developments, usage trends and areas of activity in the various segments of the integrated circuit industry. It is the marketing specialist's responsibility to keep the systems designer as thoroughly informed as possible while protecting proprietary plans. He is also responsible for providing realistic estimates and not intentionally misleading the user.

Selection

The technique of selection of transistors to tightened or special parameter limits has long been a common procedure. Pricing under these circumstances has involved 'dollar-price-averaging', such as shown in Figure 7-3. Gain, breakdown voltage, leakage current, saturation voltage, noise figure are but a few of the parameters employed in the selection. The more choice units command sufficiently large prices as to exceed the costs of extra testing, etc.

Military and Commercial Temperature Ranges

With integrated circuits, the opportunity for selection is much more limited. To date, the only selection basis of major significance involves the range of temperatures throughout which the circuit is specified to operate. The military temperature range is -55 to +125°C while 0 to 55°C serves the commercial range. Another selection basis that has received limited application involves the number of circuits (fan-out) that can be driven. (Figure 7-4). As with discrete components, the higher performance units command premiums higher than the selection costs.

Special Selections

Additional special selections based on operational characteristics have not been successful. They have served only as a basis for reducing yield and increasing price. In some instances, suppliers have used pseudospecial selections as a basis of trying to block out competition. By including the special tests in the specification, they have listed the devices as custom designed for the customer. This technique has not endeared the supplier to the user when the latter realized what had happened.

7.6 In-House Facilities

Almost all major and many smaller electronic equipment companies are developing in-house integrated circuit facilities to some degree. Most of these are primarily intended to provide necessary capabilities for fabricating sample quantities and make state-of-the-art investigations. However, they are often being used as a threat of an internal source of supply available to compete with potential suppliers.

Economics of 'Make or Buy'

Any evaluation of a "Make or Buy" decision leads to the inevitable conclusion that the economics favor "buying" in almost every case, the only exceptions being those of the largest equipment manufacturers. Figure 7-5 shows a cost versus volume comparison. From this, it can be seen that most of the larger volume buyers of integrated circuits don't have sufficient volume to compete with the much larger production rates desirable to the major suppliers. Considerations such as training knowledgeable designers, maintaining proprietary and state-of-the-art information, establishment of a second source or a reputation for leadership, etc., are among the justifications for the development of in-house capability. Laboratory facilities are becoming a requisite to advanced systems design and evaluation.

DOLLAR COST AVERAGING OF A TRANSISTOR RUN

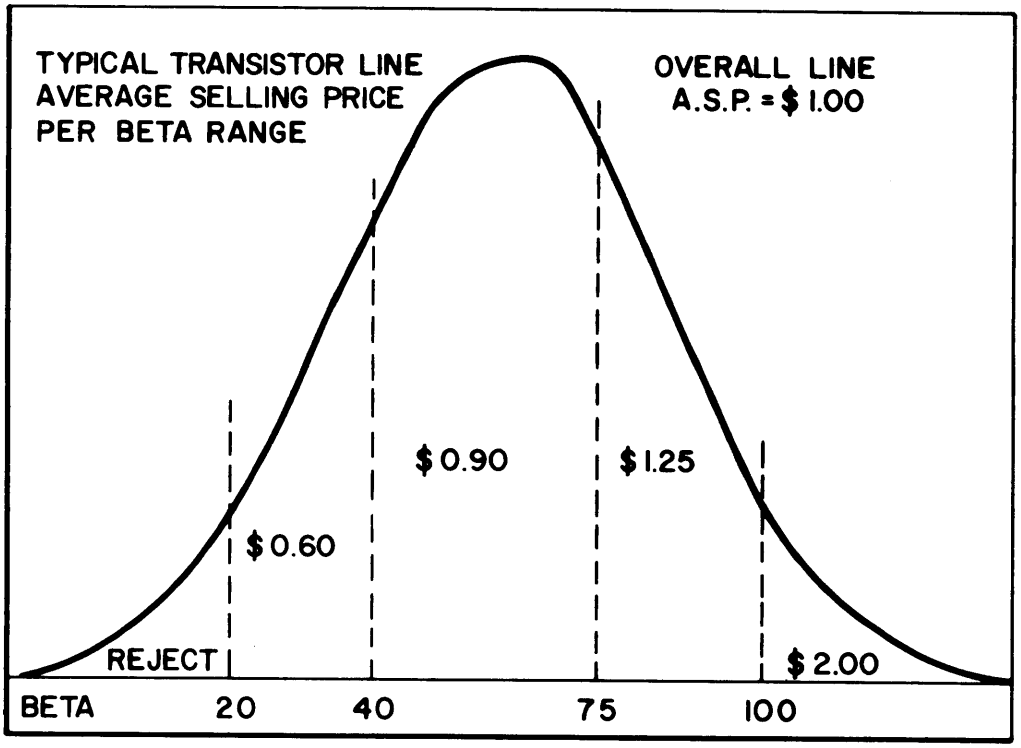
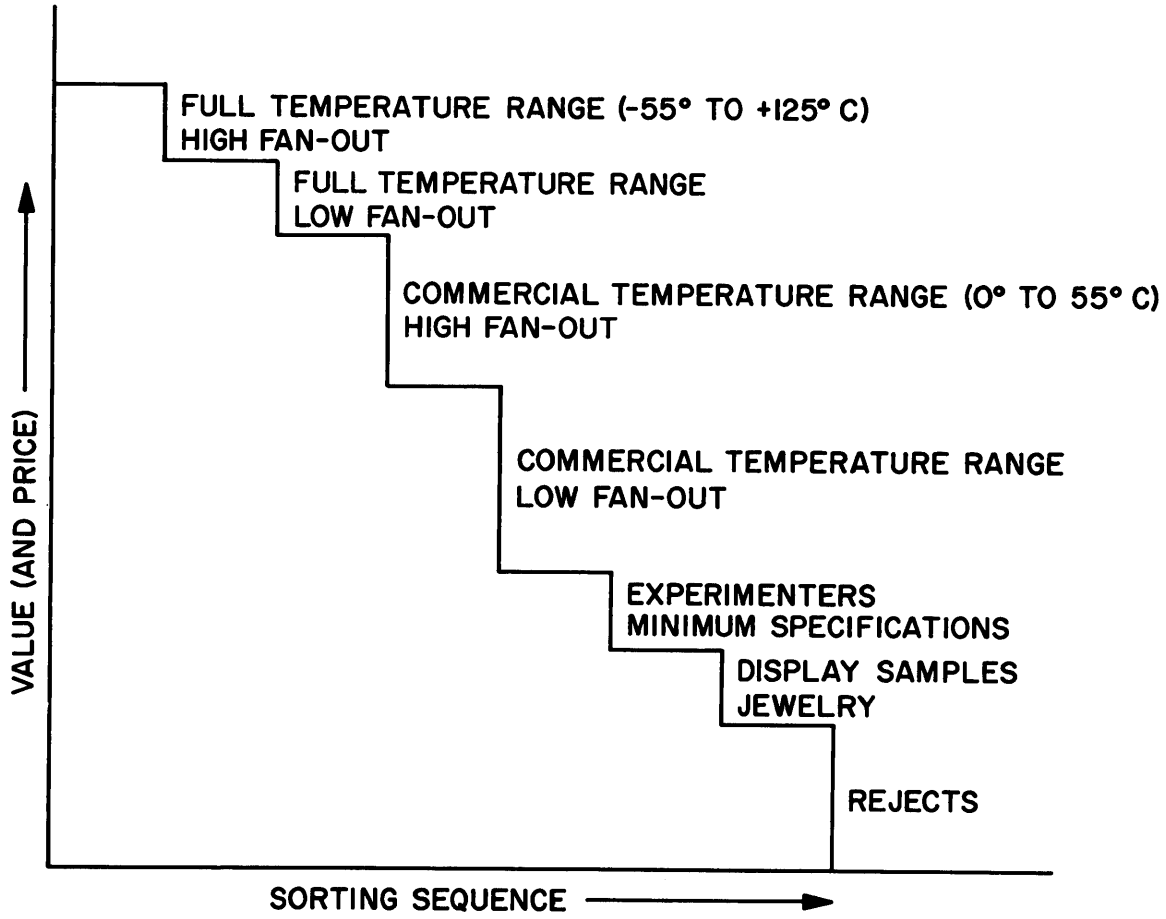


Figure 7-3

INTEGRATED CIRCUIT SORTING



7.6 (Continued)

Working with Companies Having In-House Capability

Effective marketing specialists are finding that work with the companies that have such facilities as compared to those without is more successful. They are finding that if the buyers and designers are truly knowledgeable, there is less misunderstanding and difficulty in establishing correct specifications and schedules. The price negotiations, however, may be a little more combative. The greatest danger in this area arises from adequate training of personnel who believe that they are truly knowledgeable. This coincides with the old adage "A little knowledge is a dangerous thing."

Advantages of Customer In-House Facilities to the Supplier

At times, exceedingly large demands develop for experimental samples and custom and production quantities of integrated circuits. The type of situation such as we have recently been experiencing has overwhelmed the industry's production and development capabilities. Under these conditions, it is of advantage to have in-house facilities. For the supplier, they relieve some of the overload and for the user, they assure more rapid deliveries. More attractive delivery schedules of commercial products and elimination of some of the less profitable small orders are thus negated by the in-house facility. Where a true contractor - subcontractor relationship has been established, then the advantages of in-house facilities are enhanced even more. The supplier can then rely upon rapid and accurate evaluation of his product from which important improvements can develop. The user can also be more confident of satisfactory end results.

7.7 Specifications - General

The Purpose of Specifications

"Specification" denotes a written statement of the characteristics which must be exhibited in order to perform an intended function. Specifications represent a specialized communications system. It is universally agreed that perfect procurement specifications do not exist and are never likely to be written. The written document represents a studied attempt to state, in a logical manner, the best technical reasoning available to satisfy a given procurement. The most important characteristic in a specification, as with any written agreement, is the intent of the parties concerned. No specification, no matter how detailed, will fully protect the purchaser from carelessness or dishonesty. Conversely, many procurements are successful despite glaring specification errors.

Reliability Specification Requirements

Specifications in recent years have been complicated by the addition of reliability requirements. The actual requirements for a given part increase both with the demands upon and complexity of the system in which it is used. Space systems today by their nature have absolute requirements for reliability. Their reliability specifications are often more important and demand correspondingly greater attention than the operational characteristics.

There is no alternative to the procurement document stating the various tests and inspection procedures to be performed and the criteria for acceptance or rejection. Unfortunately, while these procedures can assure the operational characteristics, they cannot guarantee the required reliability. To avoid this problem, many of the newer specifications are reflecting increased control by the purchaser over the product - from raw materials through manufacturing processes to final testing and approval. These actions appear to be producing higher quality components, but only at great expense.

7.7 (Continued)

Standardization

Unfortunately, there has been virtually no standardization between the parts suppliers or parts procurers in terms of reliability specifications and requirements. Special testing for higher reliability usually entails long periods of time and extremely high costs. One of the major problems in this area results from the guide line for including reliability specifications. It is either not clear or incomplete. Such guidelines have been issued by certain military agencies, but they have been in conflict with those supplied from other agencies. There have, however, been several component quality assurance programs (CQAP) that have been relatively effective although expensive. Noteworthy among them are those on the Minute-Man and Apollo.

Supplier Qualification

Establishing the supplier's ability to produce and evaluating it with respect to reliability are particularly difficult. A result of the contractor - subcontractor relationship developed with respect to integrated circuits increases the need for qualifying not only the product, but the production line and the manufacturer's entire capability to provide all of the services related to supplying. A sequential arrangement for such an evaluation is shown in Figure 7-6. A marketing specialist on his first call to any major equipment supplier should investigate that company's approach to supplier qualification.

Specification Language

Any specification, no matter how detailed, is at best an imperfect expression of a reasoned idea. Many users seemingly have taken great pride in past semiconductor negotiations, e. g. in trying to obtain the lowest possible leakage specifications on a given transistor. It has not mattered when this specification had no significance. They seem to have concluded that in some way, it is directly relatable with reliability. While more nearly true in the early days of semiconductors, in recent years, its meaning has diminished and the practical individual knows this. In any event, this philosophy applied to integrated circuits will continue to produce stumbling blocks in the negotiation of reasonable specifications. Integrated circuits specifications and purchasing require a degree of sophistication that has not been common to the electronics industry. It is the responsibility of the marketing specialist to carry the brunt of the educational process and to imbue the customer with systems and black box concepts of purchasing. Under such circumstances, individual specifications may be less precise while overall objective specifications become the acceptance criteria.

7.8 Specification Content

As a convenience, specification sheets can be divided into three broad areas. They are:

Group A Specifications include the operation of the integrated circuit and other attributes which can be tested directly

Group B Specifications include the mechanical and environmental testing. A typical military format for these tests is shown in Figure 7-7. Many suppliers are using similar formats for commercial products with modified test conditions and limits.

Group C Specifications cover life or quality acceptance testing.

Supplemental references and additional specifications covering qualification, test conditions and procedures are also frequently required. They should be included as an integral part of the specification document or by numerical reference where standard or Military specifications are involved. Many companies have established a comprehensive control specification which is included by reference in all procurement specifications.

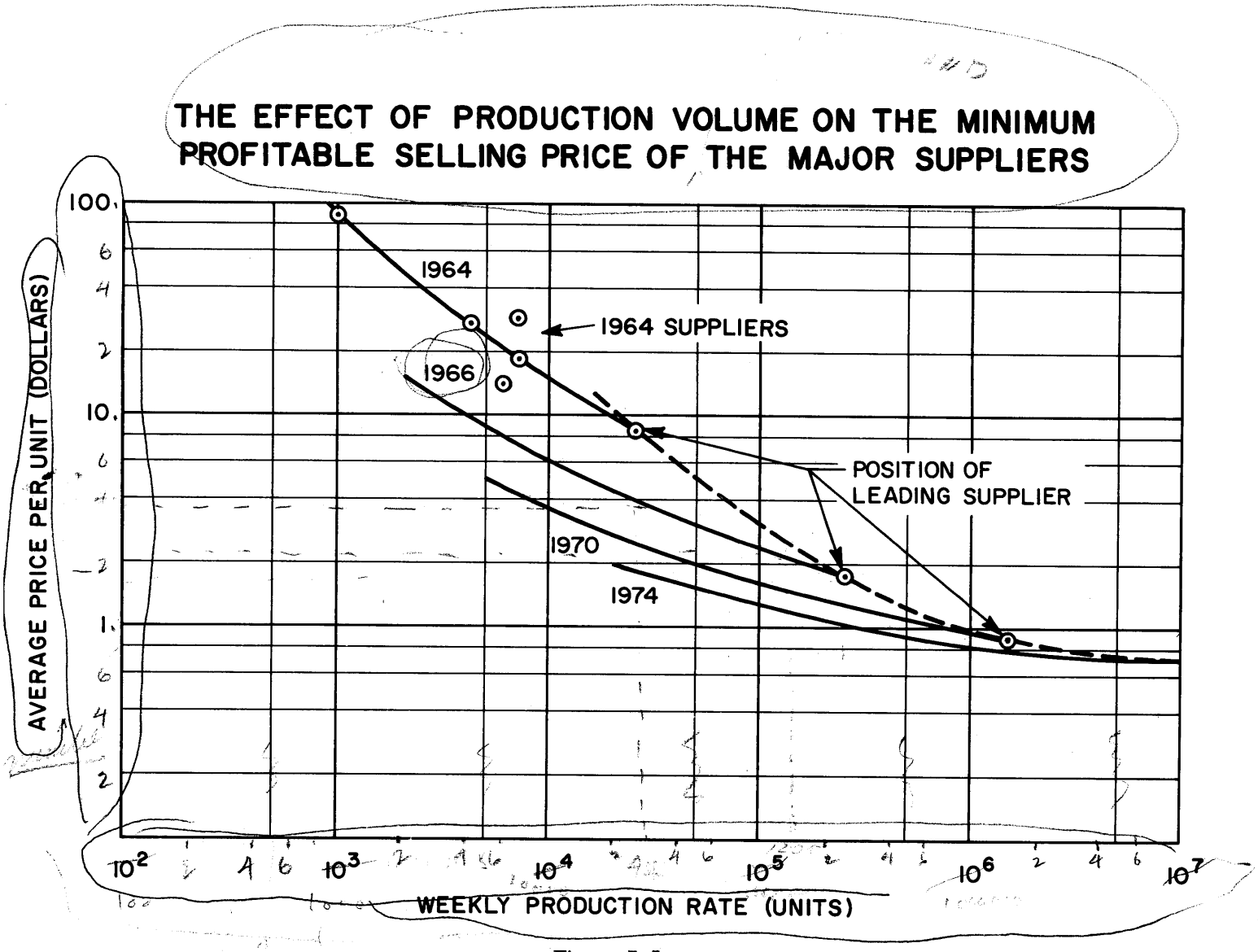


Figure 7-5

PRODUCT, LINE AND VENDOR QUALIFICATIONS

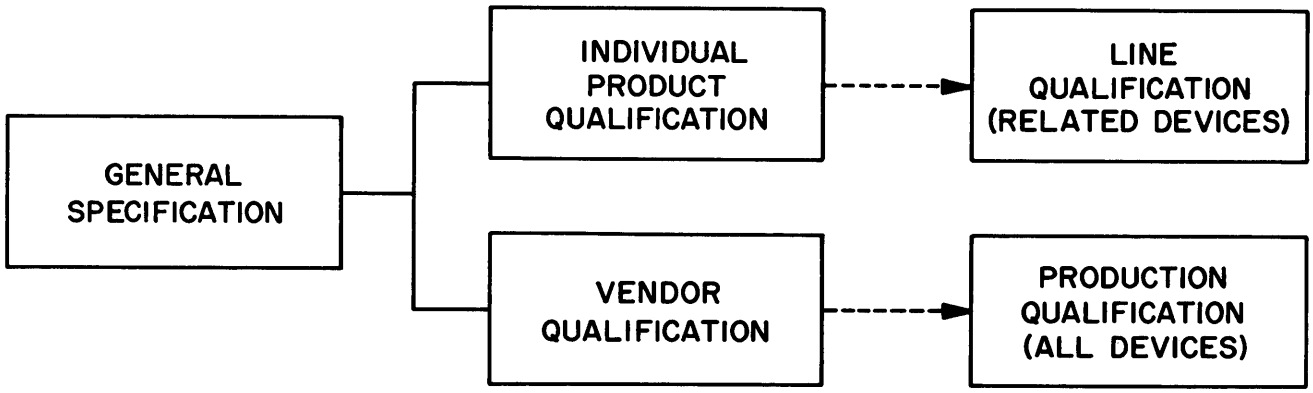


Figure 7-6

GROUP B TESTS

TEST	MIL-STD-750 METHOD	SPECIFIC CONDITIONS	COMMENTS
Subgroup 1			
Physical dimensions	2066	--	General test includes visual inspection of quality and workmanship.
Subgroup 2			
Soldering heat	2031	1 cycle	Solderability of leads. Damage from thermal shock.
Temperature cycling	1051	-65 to 175°C, 10 cycles 1/2 hr. at extremes	Examined for mechanical damage and electrical malfunction.
Thermal Shock (Glass strain)	1056 Cond. A	-65 to 175°C 5 cycles	Evaluates hermeticity of seal.
Moisture Resistance	1021	Combination temperature-humidity cycling	Evaluates hermeticity of package and corrosion.
Subgroup 3			
Shock	2016	5 Blows, X_1, Y_1, Y_2, 500G, 1 msec (Total 15 blows)	Test ability to withstand mechanical shock in several planes.
Vibration fatigue	2046	10G (non-operating), 96 hrs. 3 orientations	Test for mechanical breakdown.
Vibration variable frequency	2056	10G peak, 3 orientations	Checks for mechanical resonance breakdown.
Constant Acceleration	2006	10,000G, X_1, Y_1, Y_2	Check for mechanical damage.
Subgroup 4			
Terminal strength	2036 Cond. E	3 leads at random - 90° bend	Specified radius, check for breaking of lead or glass seal - flaking of plating.
Subgroup 5			
Salt Atmosphere (Corrosion)	1041	--	Checks for electrical malfunction and readability of markings.
Subgroup 6			
High Temperature life (non-operating)	1031	T_A = 175°C	Quality assurance test under "storage".
Subgroup 7			
Steady state operation life	1026	Max. rated dissipation	Quality assurance conditions under D. C.

Figure 7-7

7.8.1 Group A Specifications

A general summary format for Group A specifications is included in Figure 7-8.

General Description

The first item-General Description-should state in simple generic terms what kind of integrated circuit is involved, its basic function, and material or construction. If the circuit has been especially designed or tested for a specific systems application, this should also be referenced in this section. Frequently, these generic descriptions become the only control against dissimilar products and unforeseen performance differences, e.g. monolithic and multichip circuits might meet the same electrical performance criteria, but their life, reliability and unspecified electrical performance characteristics may vary widely.

Electronic Description

Electronic Description, the second item, should specify electrical performance in generic terms. It may be in the form of logic symbol diagrams, logic equations, truth tables, or in linear circuits, general gain, frequency, or performance characteristics, i.e., amplifier-oscillator, audio-video.

Mechanical Data

Mechanical data, subject to visual inspection, should include detailed package drawings, terminal and marking designations and precautions relating to handling and mounting. Information on mounting positions and techniques should be included whenever special consideration is required. Internal interconnections should also be included with the terminal designations. Substrate and package connections are often neglected, sometimes with unfortunate results.

Maximum Limits

The fourth category, Maximum Limits, presents a major problem with integrated circuits compared with transistors and most other discrete components. Since many of the individual electronic components of an integrated circuit are not all available at the terminals, maximum voltage and current limit tests can't be conducted. Most designers, quality control and purchasing agents familiar with discrete semiconductor devices have been indoctrinated so that they include complete maximum limit specifications on those devices. They are now frustrated because with integrated circuits, this is invariably impossible. Typically, lead wires or metalization limit the maximum current rather than the electronic components. Isolated junctions are rarely available to test breakdown voltage.

Electrical Characteristics

Electrical characteristics, the 5th category, are most critical from the designers point of view. The necessity of evaluating the integrated circuit as a black-box electronic subsystem necessitates that this section of the specifications be extensive. The large number of terminals and various combinations thereof requires its own test. Because of the large number of tests required, the use of electronic data processing (EDP) expedites the interpretation of the massive amounts of data required for each circuit.

Automated Testing

7.8.2 Life Test Specifications

Life test specifications by their nature require the use of initial test acceptance criteria and measurement data to establish the basis for comparison with end-of-life test data. Similar before-and-after tests must be compared to determine acceptability. Life testing is further complicated by the need for containing the method of sampling, test conditions and the length of the test. The variety of life tests possible is numerous. Most widely used are:

Storage Life Tests

1. High temperature storage. Storing units without connection to the terminals requires the minimum of space and equipment, hence is the least expensive method of life testing

GROUP A SPECIFICATIONS FOR INTEGRATED CIRCUITS

TEST	MIL-STD-750 METHOD	SPECIFIC CONDITIONS	COMMENTS
Subgroup 1			
General Description			
Subgroup 2			
Electronic Description			
Subgroup 3			
Mechanical Data Package Outline Terminal Designation Handling and Mounting precautions Marking			
Subgroup 4			
Maximum Limits Ambient Temperature Limits Maximum Power Dissipation (Power-Temperature Derating) Maximum Voltage (between each pair of terminals) Maximum Current			
Subgroup 5			
Electrical Characteristics Static Transfer Speed Performance			

Figure 7-8

7.8.2 (Continued)

Operating Life Tests

2. Operating life tests with power applied, more sophisticated arrangements are required:

   a. Ring counter gates and flip-flops can be so arranged to transfer off-on signals from one to the next in a ring so that operation will continue until one of the units fails. This technique provides one of the simplest operating life test arrangements with a clearly defined failure criteria

   b. Maximum power dissipation operation is frequently required. This is particularly difficult to establish for integrated circuits for the same reasons involved in the establishment of proper maximum ratings

   c. Cycled power on and high temperature storage life tests are frequently considered to be the best because they simulate actual field operation under the most adverse conditions. These types of tests are particularly expensive because of the elaborate test setup required.

7.8.3 Standards, References and Procedures

Complete standards for testing integrated circuits have not yet been established. The Military services, the suppliers [through Electronic Industry Association (EIA)] and various users are attempting to generate such standards in addition to those which already exist. Some of the Military specifications that may be used completely or in part for integrated circuits are:

MIL-S-19491A	Semiconductor Devices, Preparation for Delivery of
MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-202B	Test Methods for Electronic and Electrical Component Parts
MIL-STD-750	Military Standard Test Methods for Semiconductor Devices
MIL-M-23700	Microelectronic Functional Devices, General Specifications for
MIL-S-19500	Semiconductor Devices, General Specifications for
MIL-R-38103A	Semiconductor Device Established Reliability, Attachment 1
MIL-STD-806B	Graphic Symbols for Logic Diagrams

The inadequacy of these for integrated circuits is reflected in the necessity of including complete explanations for test conditions, acceptance criteria and stabilization (burn-in) within each individual specification or as an addendum thereto.

SECTION 8 FUTURE CAPABILITIES OF INTEGRATED CIRCUITS

8.0 Introduction

At the present time, the term "integrated circuits" is generally used synonymously with "microelectronics". However, an integrated circuit need not necessarily be small. In fact, as integrated circuits penetrate further into additional facets of electronics, particularly those requiring higher current and power, the integrated circuit and associated package will necessarily become larger in order to permit adequate power dissipation.

The two basic or "classical" types of integrated circuits are semiconductor-monolithic and thin-film. In addition, there are "hybrid" integrated circuits in which these types are combined either together or with discrete components.

Monolithic and Thin-Film Circuits:

To create a monolithic integrated circuit, all circuit elements - transistors, diodes, resistors and capacitors - are fabricated within a single block of silicon.

In the thin-film integrated circuit, one or more of a number of different elements or compounds is deposited selectively on a passive substrate. Deposited materials include tantalum, nichrome, cermet, etc., for resistors; silicon monoxide, aluminum silicate, tantalum (after anodization) for capacitors; copper and aluminum, which provide low resistivity layers, for conductors. Processes used for thin-film deposition include evaporation,(nichrome), sputtering, (tantalum) and vapor deposition, (aluminum silicate). At the present time, there are no commercially available thin-film active elements (diodes or transistors). Hence, in all thin-film circuits of today, diodes and transistors must be affixed to the circuit, e.g., by welding, as shown in Figure 8-1. An alternative approach, which has gained considerable favor recently is the "flip-chip" approach, illustrated in Section 4.

Active Elements

The major advantage of the semiconductor monolithic approach is that the active elements are easily obtained as part of the fabrication – easier than most resistors or capacitors. The continuing lack of active thin-film elements is the most obvious disadvantage of the thin-film circuits. However, the quality and performance characteristics of the passive thin-film components usually are superior to the corresponding elements in the monolithic approach. With thin-film resistors, a wider range of values is possible, the temperature coefficient is lower by an order of magnitude and the high frequency characteristics are also superior. The advantages and disadvantages of the two approaches are summarized in Figure 8-2.

Parasitics

In Figure 8-2, the entry "parasitics" refers to parasitic capacitance between the circuit elements and the ground plane. In the thin-film approach, the parasitic capacitances need not be any larger than in discrete-component circuits and may be lower since the size of the circuit elements can be smaller. In the monolithic structures the need to isolate the various portions of the circuits, (e.g., two transistors whose collector terminals are at different potentials) leads to substantial capacitances between elements and substrate.

Inductance

Inspection of Figure 8-2 shows that the circuit element "inductance" is conspicuous by its absence. Although flat helical spirals of conductors can be incorporated into either type of circuit, the range of inductance values and the Q obtained are severely limited. Hence, for most practical purposes, inductance can not be obtained within either classical type of integrated circuits. Where inductance is absolutely necessary, a small inductor

THIN FILM ASSEMBLY TECHNIQUE

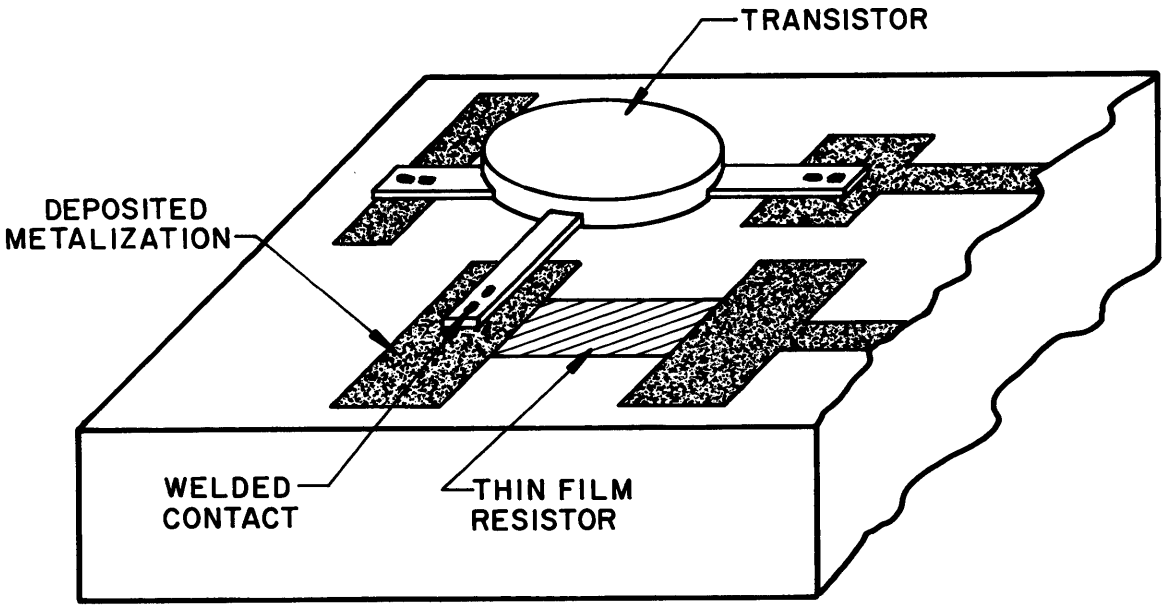


Figure 8-1

CLASSICAL INTEGRATED CIRCUITS

COMPONENT OR CHARACTERISTIC	MONOLITHIC SILICON TYPE	THIN FILM TYPE
TRANSISTOR - DIODE	INTEGRAL	MUST BE AFFIXED
RESISTANCE	POOR TEMP. COEFF. LIMITED RANGE	GOOD TEMP. COEFF. WIDER RANGE
CAPACITANCE	POOR Q LOW VALUES VOLTAGE VARIABLE	GOOD Q HIGHER VALUES
PARASITICS	HIGH	LOW
SIZE	SMALLER	SMALL
COST	LOWER COST IN LARGE QUANTITY	HIGHER ASSEMBLY COST

Figure 8-2

8.0 (Continued)

can be added as a discrete component to an otherwise fully integrated circuit, either externally or within the same package. Alternatively, the need for the inductance can usually be eliminated by revising the circuit design.

8.1 Future Capabilities of Integrated Circuits

8.1.1 Frequency Response and Speed

High frequency and/or high speed capabilities of present integrated circuits are limited by either parasitic capacitances or the speed of the transistors. In the case of the diffused silicon monolithic circuit, parasitic capacitance is comparatively high as a result of the use of a reverse biased P-N junction for isolation. Several companies have announced schemes for fabricating monolithic integrated circuits in which the isolation is provided by a fairly thick layer of silicon oxide (Figure 8-3). With these techniques, the parasitic capacitances of monolithic circuits can be reduced by a factor of ten. Consequently, this technique permits the speed of many circuits to be substantially improved. For example, a 40 per reduction in rise and fall time of an emitter-coupled logic circuit and a 400 percent increase in bandwidth of an amplifier have been reported for standard monolithic circuits employing dielectric isolation rather than P-N junction isolation.

Isolation

Geometry

A second possible limitation of the high speed performance of integrated circuits is the frequency response of the transistor. This, in turn, is directly related to the size of the device; generally, the smaller the transistor, the higher its frequency response. With the silicon planar technology used in fabricating monolithic circuits, the size of the device has been limited by the allowable tolerances on the various fabrication steps, including masking, photolithography and etching.

Tolerance

The tolerances are a function of the state-of-the-art which has improved with time. Figure 8-4 shows the emitter-base geometry for one fairly common type of transistor, comparing the smallest commercially available version in 1959 with that obtainable in 1966. These data also are plotted in a different way in the curve of Figure 8-5 which shows the smallest commercial-sized transistor area as a function of time. The dotted portion of the curve represents an extrapolation, which appears to be consistent with recently reported laboratory developments. These should be implemented in commercial production in the near future. The straight line indicates that the smallest linear dimension of the transistor has been decreasing by a factor of two, every three years.

Ultimately any of several physical limits will be reached, e.g., the wavelength of light which is used in the photolithography process. However, in anticipation of approaching this limit, work is already underway in several research laboratories to develop electron beam technology for forming extremely small configurations.

8.1.2 Frequency Selection

Another problem related to frequency response is that of frequency selection. As noted, it is difficult to obtain inductance for integrated circuits. One practical alternative is to use miniature toroidal coils, externally. If inductors must be avoided, one alternative for tuned circuits is the electromechanical filter, especially those using piezoelectric elements, to provide the parallel resonant function.

Another increasingly popular way of avoiding the use of inductance is to convert from analog to digital techniques. This is particularly desirable as digital circuitry continues to become less expensive owing to the growing use of these types of integrated circuits. For example, in the area of frequency selection, bandpass filters can be built using digital techniques. However, such systems are complicated, requiring a large number of devices which makes them expensive to develop.

EXAMPLE OF DIELECTRIC ISOLATION

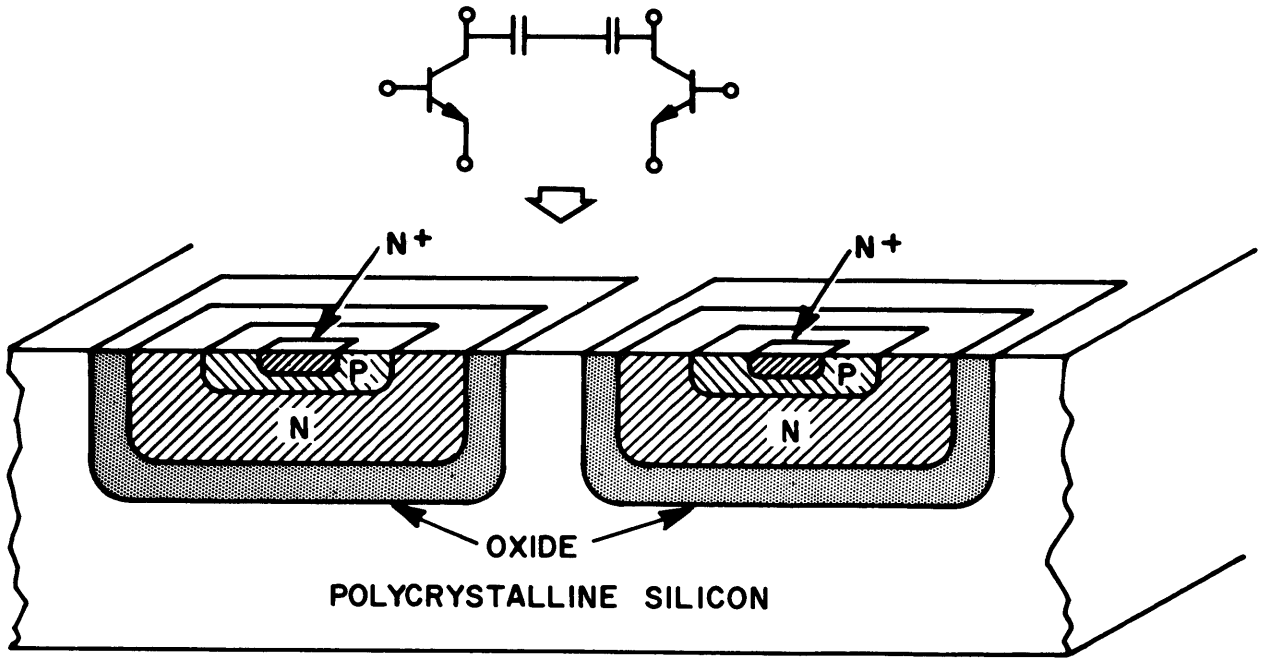


Figure 8-3

THE EFFECT OF PROCESS IMPROVEMENT ON TRANSISTOR ACTIVE AREA

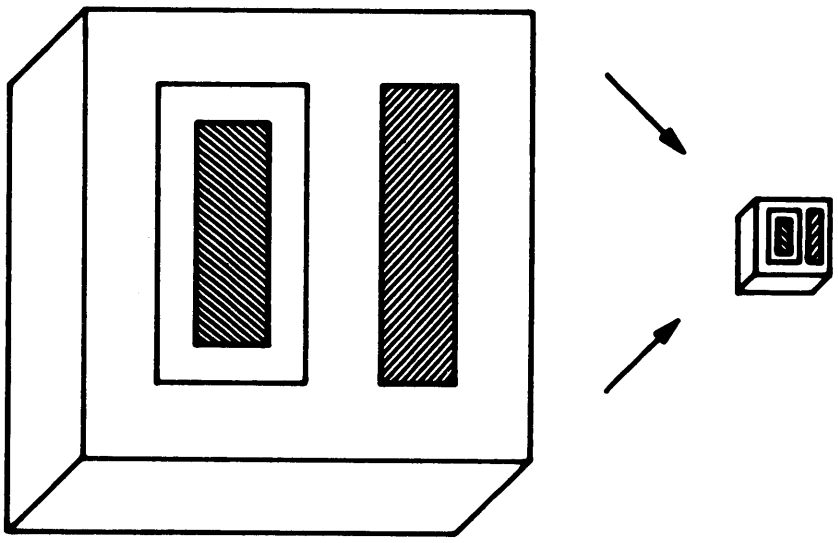


Figure 8-4

8.1.3 Frequency Selection

Another approach to frequency selection without inductors is by means of RC filters, e.g., a "twin-T" network. Present integrated circuits, however, are limited as to selectivity and stability by the available tolerances on the passive circuit elements. With present tolerances of about 10 percent, this approach is almost completely impractical. However, as component tolerances continue to improve,the use of RC precision networks should become feasible for these applications.

8.1.4 High Voltage - High Power

Most commercially available integrated circuits have been designed for low power applications. In fact, for digital circuits, emphasis has been on decreasing the propagation delay time. However, the trend has changed recently with the major emphasis now directed to reduce the power dissipation, even at the sacrifice of speed. Almost all of the applications for digital circuits have required power dissipations of less than a watt. They usually employ power supply voltages between 6 and 12 volts, so that the safe maximum device/circuit voltage ratings are of the order of 20 volts. As new applications continue to emerge, a greater range will be required. For example, the use of integrated circuits in connection with memory circuits or display devices require that this maximum voltage limit be increased.

Breakdown Voltage

Present silicon technology permits an increase in breakdown voltage to approximately 100 volts. Additional engineering in material technology and process control might be required to obtain good yields with this higher resistivity material through the many necessary processing steps.

Higher voltage transistors in discrete form generally are obtained by selection. In an integrated circuit, this is not feasible, hence it might be more desirable to connect several transistors in series for higher voltage applications. Series connection requires high breakdown voltage between individual devices and the substrate.

This is now possible by the use of the dielectric isolation techniques described. This type of technique appears to be capable of permitting series connections capable of withstanding 500 to 1000 volt breakdown.

To date, integrated circuits have been limited primarily to microstructures. However, this is not a necessary limitation, and higher power circuits can also become integrated. Power dissipation of present structures is in fractions of a watt, but some circuits are available with dissipations up to 1 or 2 watts higher. A 2 watt class B amplifier has been advertised. Another firm has announced a 40-watt servo amplifier.

Heat Sinks and Cooling

Higher power integrated circuits will have to be packaged in the same way as conventional transistors and diodes, in lower thermal-resistance packages in addition to employing heat sink and other known cooling techniques. This should present no great problems, except for overcoming the psychological block that insists that an integrated circuit be small. Commonly employed chip sizes have been employed in discrete transistor form to achieve power levels in the 100 watt range. Solutions must be obtained for the obvious problems resulting from proximity and thermal coupling between elements in structures. Actually, thermal feedback has been used by one manufacturer in an experimental circuit to a distinct advantage, viz., to provide a low-pass feedback network which otherwise could be obtained only with large values of capacitance.

8.2 Present Technology Indicators

Several realistic predictions based upon recent experimental developments indicate the future of integrated circuits. A few of these are already making their debut, illustrating the fast development pace of this technology. From an understanding of the basic developments, reasonable extrapolations into the future may be made.

Extensive research and development work is being done in attempts to remove the limitations and improve each of the two basic types of integrated circuits (Figure 8-2).

New Classes of Integrated Circuits

A new class of integrated circuit, combining the monolithic silicon with thin-film techniques, shows promise. This combination has been called by various names, such as "compatible thin-film monolithic." The active circuit elements and some less critical resistances, are fabricated in the monolithic structure, then, thin-film deposition techniques place passive circuit elements directly on the silicon oxide layer comprising the upper surface of the monolithic structure.

Compatible

The advantages of circuits constructed in this manner include all of those listed for thin-film components. It also permits use of the same metalization type of interconnection scheme as used in monolithic fabrication with its advantageous economics. The extra thin-film processes, however, add materially to processing costs.

Proponents of thin-film technology have devoted considerable effort to finding a suitable thin-film active device. One such structure described in the literature is shown in Figure 8-6. However, a commercially satisfactory device has not yet been made available. In the meantime, attention has been turned to development of a thin-film transistor using the monolithic silicon technology.

MOS

The result of this "cross-breeding" is the MOS (metal-oxide-semiconductor) device as shown in Figure 8-7. This device, similar to that shown in Figure 8-6, also has a strong resemblance to the conventional field effect transistor. Functionally, a voltage is applied between the source and drain electrodes, and the amount of current in this circuit is determined by the potential applied to the gate electrode.

The fabrication technique employed to form the source and drain electrodes is identical with that of monolithic silicon, namely selective diffusion. Integrated circuits fabricated with these devices are quite different from conventional bipolar circuits, although the circuit function may be similar. For example, by incorporating a diffused resistor in an array of MOS transistors, a simple NOR gate is obtained, as illustrated in Figure 8-8. Several manufacturers recently have announced fully integrated circuits employing MOS structures. One of the most striking is a 200 element shift-register in an arrangement such as that indicated in Figure 8-9.

8.3 Conclusion

Although the field of integrated circuits is relatively new, its technology to a great degree is based upon that of transistors and diodes, both silicon and germanium. Hence, by reviewing the progress made in development of these structures over the past several years, noting particularly the major quality and economic improvements as well as the rapid technological advances, it is reasonable to extrapolate further striking improvements in integrated circuits. Higher speed, higher power, both more complex and new functions, further major price reductions, and realization of the extremely high reliability promise, are on the immediate horizon.

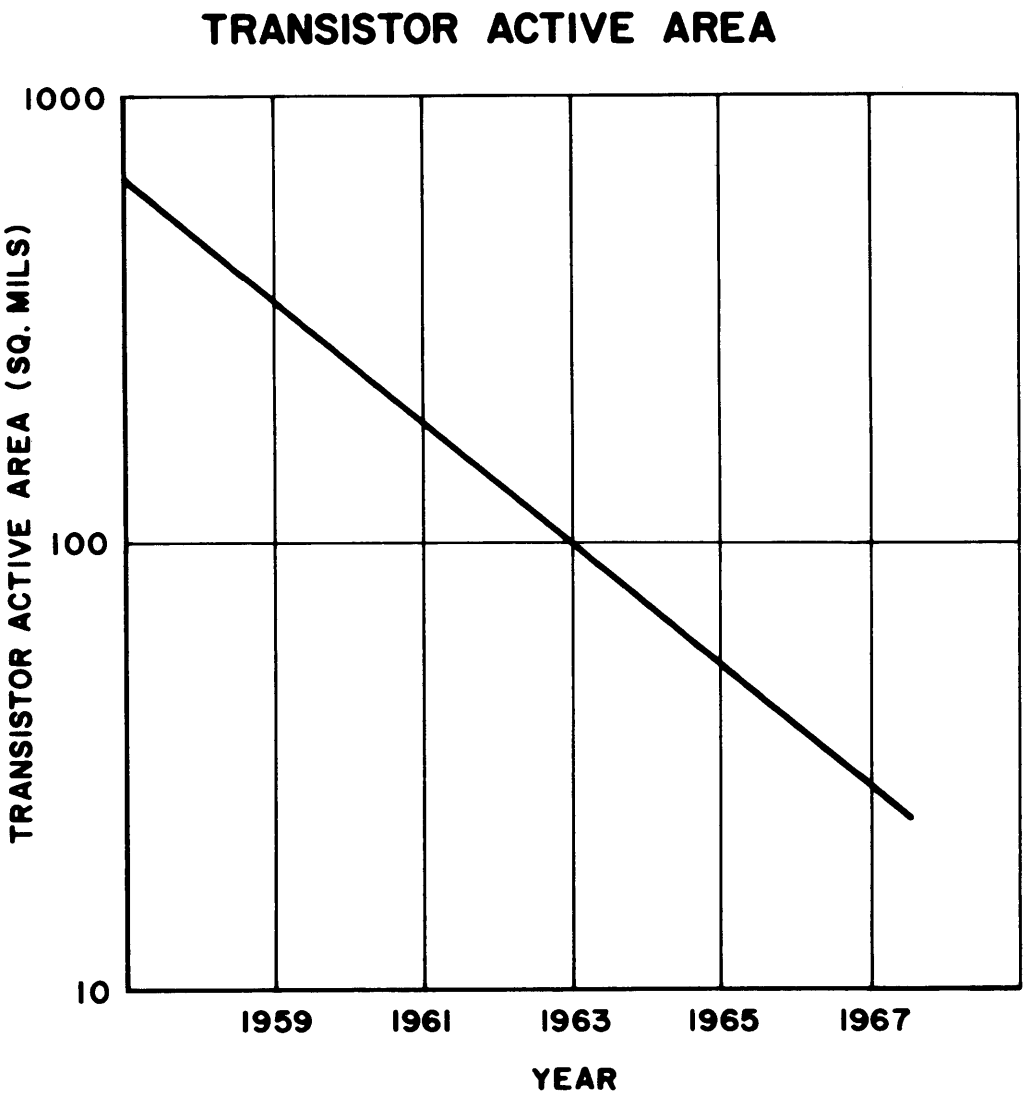


Figure 8-5

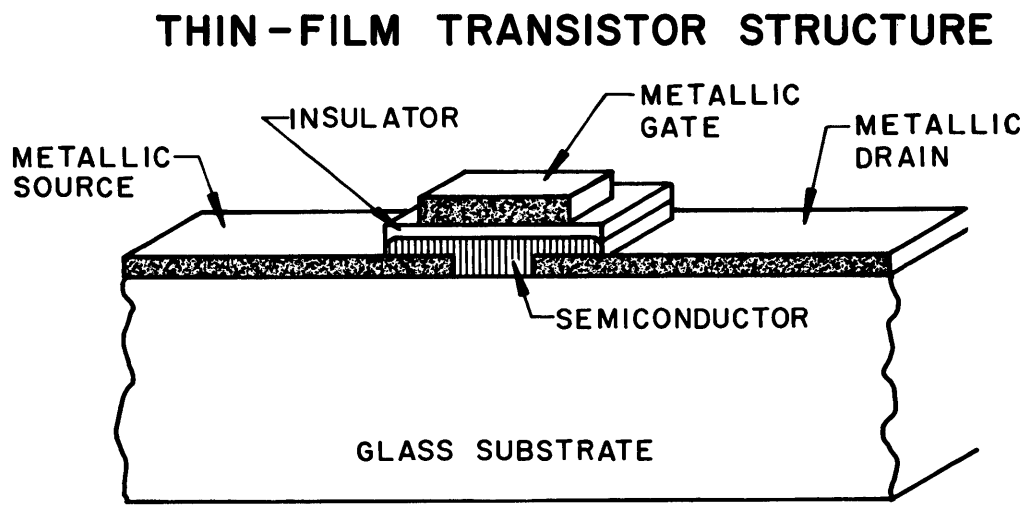


Figure 8-6

METAL – OXIDE – SILICON – TRANSISTOR
"MOST"

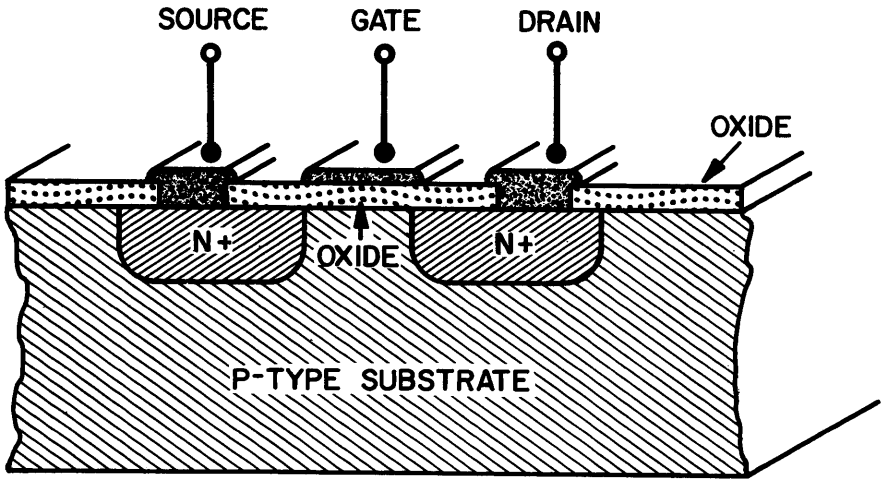


Figure 8-7

INTEGRATED MOS TRANSISTOR
NOR GATE

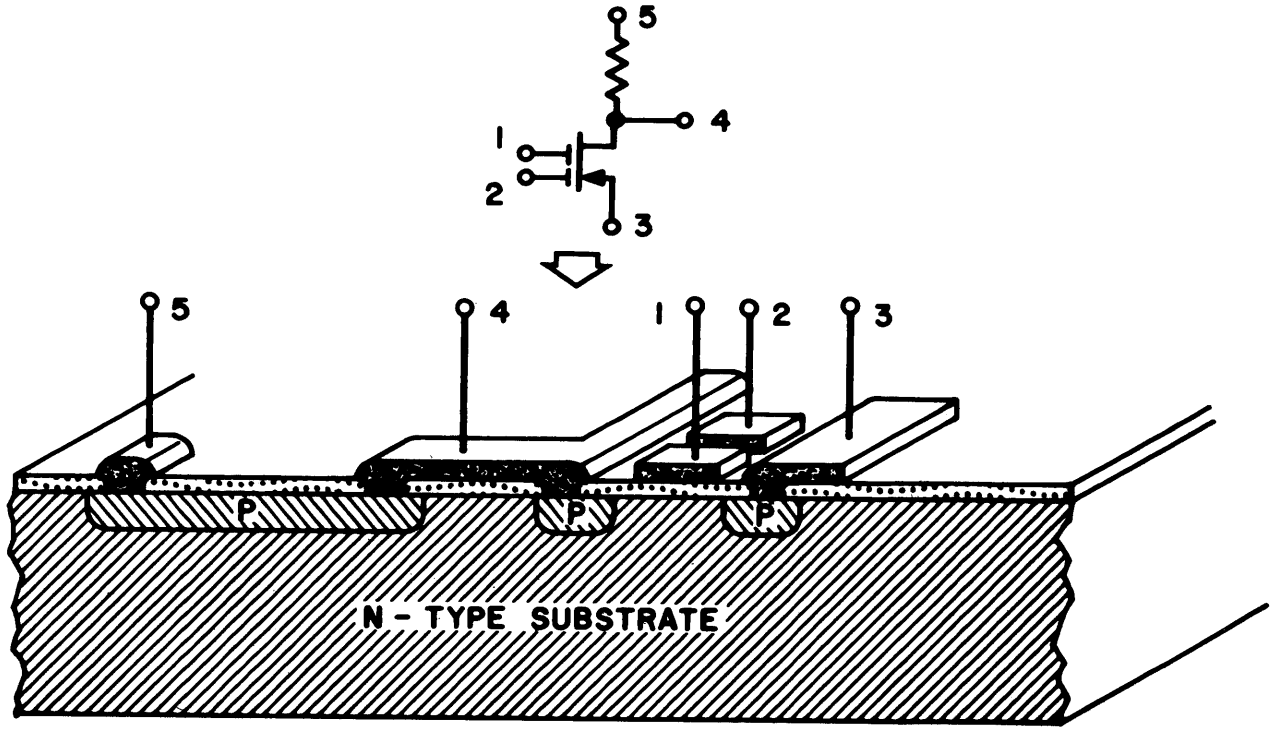


Figure 8-8

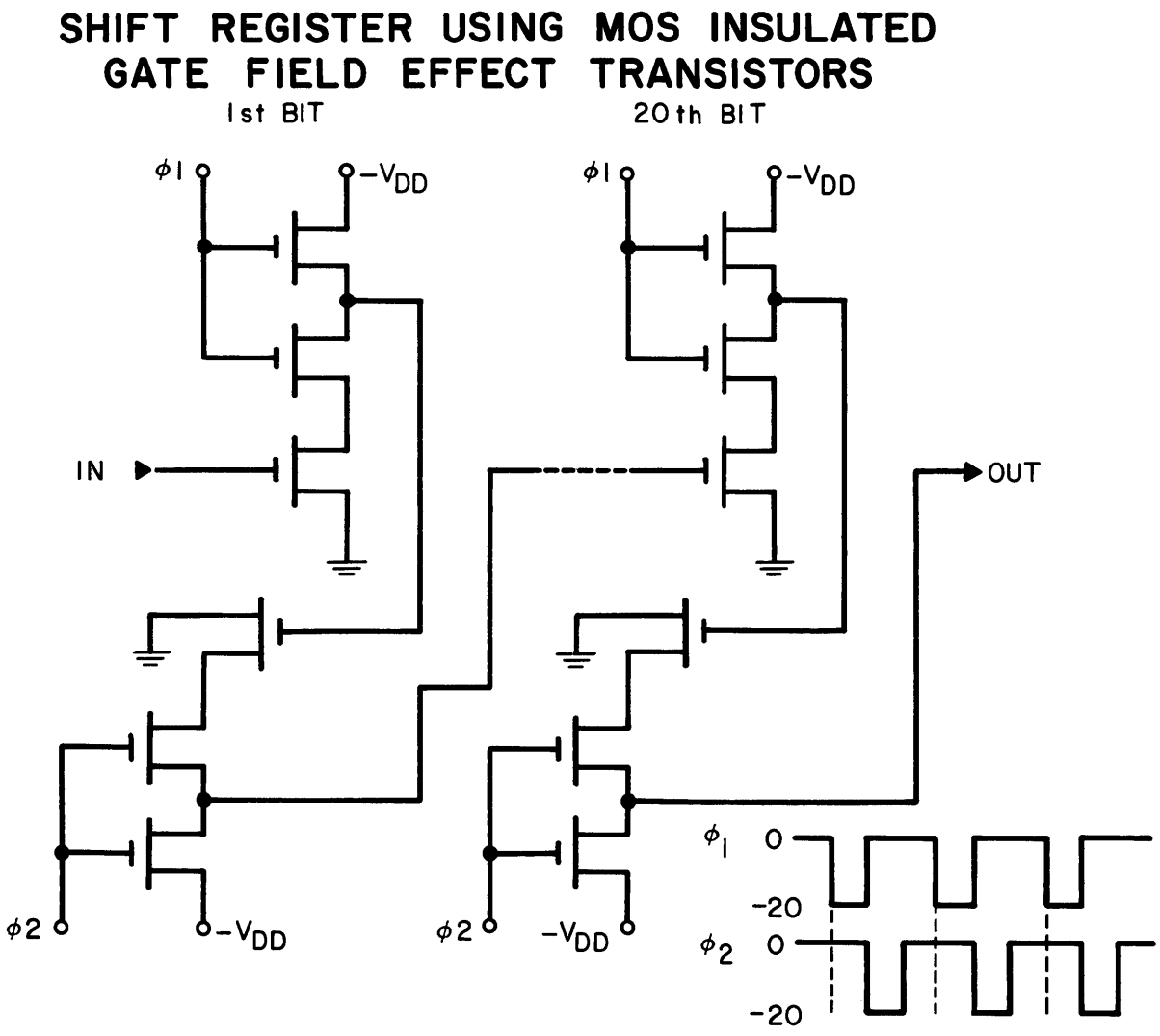

SHIFT REGISTER USING MOS INSULATED GATE FIELD EFFECT TRANSISTORS
1st BIT
20th BIT
φ1
-VDD
IN
OUT
φ2
-VDD
φ1 0
-20
φ2 0
-20

Figure 8-9

8.3 (Continued)

The electronic equipment manufacturer must continue to seek to maintain a competitive edge in his market. His efforts in quest of this goal must be fully cognizant of the total economic and technological environment. Integrated circuits enter into both of these areas of consideration.

Each segment of the electronics industry, whether major or minor, views integrated circuit problems from different vantage points – from aerospace to T. V. sets; from computers to telecommunications. Each company tends to maintain the maximum possible contributed value to its firm's products, and to extend or expand its product line while simultaneously maximizing profits.

Technical Improvements Will Affect Market

Technical breakthroughs will continue. They will change the course, economics and distribution of the total market dollars as well as significantly modifying the positions of individual companies. Important prizes await those companies making significant contributions as well as those able to recognize such contributions and react rapidly. Among the most important "breakthroughs" that seem imminent for integrated circuits will be improvements in packaging. Both novel flip-chip arrangements and molded low cost epoxy seem most promising.

The leadership position in integrated circuit manufacturing characteristically has been the maximum profit position. It may, however, require such large R&D investments that the second, third, or fourth spot might yield a comparable return on investment.

The continuing extension of integrated circuits capability together with concurrent decreasing costs will cause an expansion of the market. Initially, this effort will continue to be at the expense of discrete components. Later, the efforts for maximum dollars will become more sharply focused on the opening and exploitation of new markets or conversion of nonelectronic markets as yet unknown with respect to integrated circuits. The electronic industry will continue to expand without a maximum dollar limit. There is no apparent limiting factor on human desires for electronic "goodies".

APPENDIX A THE FUNDAMENTALS OF BINARY LOGIC AND LOGIC ELEMENTS

A.0 Introduction

The marketing specialist must understand binary logic and basic logic elements to communicate intelligently with his customers. This appendix, included as a basic reference, presents this material in simplified form.

A.1 Numerical Codes

Quantizing information has made possible the mathematics as we know it. Whereas we most frequently use the decimal system, vestiges of the duodecimal system (based on 12) of Egyptian origin remain in our society (dozen, gross, etc.). The binary system (based on 2) is convenient for electronics interpretation where the on or off conditions of a switch represent the two possibilities.

A.1.1 Decimal Numbers

The common decimal number system is composed of the ten digits (0, 1, ... 9). To indicate a value larger than 9, two or more digits must be arranged in a prescribed manner. Each position represents a coefficient having a value ten times the value of the next position to the right. This can be expressed as ten raised to some power. The one's position is 10^0, the ten's position is 10^1, etc. (Any number raised to the 0 power is always equal to one).

A.1.2 Binary Numbers

Although electric circuits can be constructed to process decimal information using ten levels of voltage or current, it is considerably more practical to use only two levels. In modern digital computers, information is expressed in terms of the two-states – "on" or "off". This is consistent with the binary number system in which the symbols '0' and '1' represent the states.

The symbols '0' and '1' standing alone represent the integers 0 and 1, respectively. Integers greater than 1 are expressed by using a position notation, similar to that of the common decimal system, except they represent powers of 2 rather than of 10. Thus, any number may be written as a series of 1's and 0's, as illustrated for 0 through 20 in Figure A-1. Figure A-2 illustrates the use of the general positional multiplication scheme to represent the number 169.

An easy method of converting from binary to decimal numbers is shown in Figure A-3. Beginning at the left side of the binary number, the computation is performed by taking the number in the first column, doubling it and adding the product to the next column to the right. The process is repeated with each column until the last is added. The example worked out in Figure A-3 for 10101001 or 169 may seem complex, however, with large binary numbers, this system eliminates the need to know the higher powers of two, and permits the translation almost by inspection.

An equally simple process of converting from decimal to binary is indicated in Figure A-4 using the number 169. The conversion is accomplished by dividing the number under consideration by 2 repeatedly and, in each step writing the remainder (1 or 0) left over from each division at the right as shown. The binary equivalent is then read from the bottom upward.

A.1.3 Binary Coded Decimals

Since computer inputs and outputs are usually in the form of standard decimal numbers, it is frequently desirable to convert directly between the binary and decimal systems. This is accomplished by binary-coded-decimals (BCD).

BINARY AND DECIMAL EQUIVALENTS

DECIMALS		BINARY				
TENS	ONES	SIXTEENS	EIGHTS	FOURS	TWOS	ONES
	0					0
	1					1
	2				1	0
	3				1	1
	4			1	0	0
	5			1	0	1
	6			1	1	0
	7			1	1	1
	8		1	0	0	0
	9		1	0	0	1
1	0		1	0	1	0
1	1		1	0	1	1
1	2		1	1	0	0
1	3		1	1	0	1
1	4		1	1	1	0
1	5		1	1	1	1
1	6	1	0	0	0	0
1	7	1	0	0	0	1
1	8	1	0	0	1	0
1	9	1	0	0	1	1
2	0	1	0	1	0	0

Figure A-1

TRANSLATION OF BINARY FORM TO DECIMAL

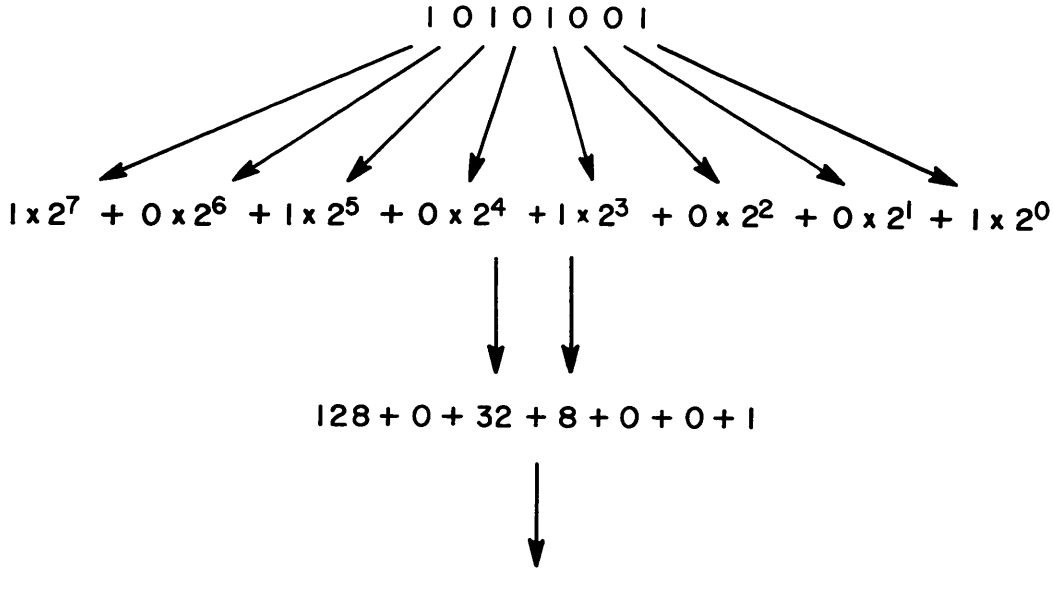


Figure A-2

CONVERSION OF BINARY NUMBER TO DECIMAL NUMBER

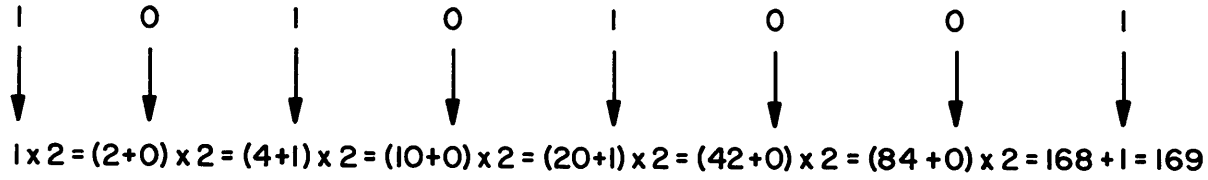


Figure A-3

CONVERSION OF DECIMAL NUMBER TO BINARY NUMBER

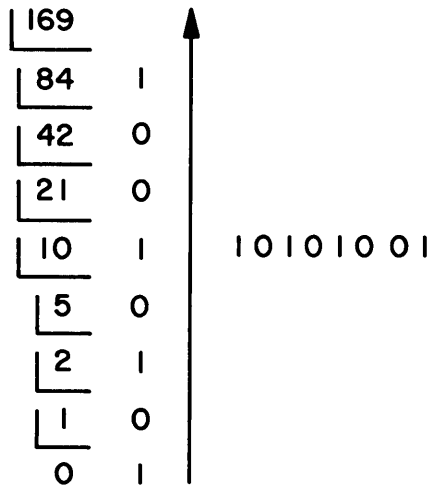


Figure A-4

A.1.3 (Continued)

The most common example of BCD employs the 8421 code. This code, as shown in Figure A-5 employs only four binary bits which are arranged to recycle upon reaching 10. Thus each set of four binaries represents each decimal digit.

A.1.4 Binary Arithmetic

Arithmetic operations are performed in the same manner with binary numbers as decimal numbers. The basic rules for binary arithmetic are shown in Figure A-6. Examples of binary arithmetic operations are listed in Figure A-7.

A.2 Logic Elements

There are three basic logic elements: AND, OR and NOT used to implement logic operations.

AND:

An AND logic element produces an output only when all inputs are "On". A simple electrical equivalent of a three-input AND element, in which an "On" input represents a closed switch, is shown in Figure A-8.

The AND "truth table" shown in Figure A-8 is a convenient way of charting all possible combinations of inputs with their resulting output. In this truth table, '1' indicates an 'On' condition, a closed switch, or an illuminated bulb, while the '0' indicates an 'Off' condition, and open switch, or no light. A graphical symbol for the AND element frequently used in systems diagrams is also shown in Figure A-8.

OR:

An OR logic element shown in Figure A-9 produces an output if any input, A, B, or C is "On". This element's truth table and standard logic symbol are also shown.

NOT:

To complete the range of logic actions required, a third element is required. The NOT logic shown in Figure A-10 inverts any input signal, from '1' to '0', or from '0' to '1'. Its truth table and symbol are also included.

NAND:

Many systems require a NOT function in combination with an AND gate. These functions, combined in one circuit, form a NAND circuit (NOT-AND) where inversion takes place as the logic function is being performed. Figure A-11 illustrates the combination of AND and OR logic functions with inversions and the resulting symbols.

NOR:

Most practical logic circuits are now constructed in this manner because amplifiers required to compensate for losses and maintain signal levels normally provide inversion. The inverting amplifier element also provides improved fanout capabilities and signal level reference. The same combination technique applies to an OR circuit combined with a NOT function to give a NOR circuit (NOT-OR). (Figure A-11b)

A.3 Memory Elements (Flip-Flops)

The flip-flop element performs the logical operation of remembering. This element has two outputs each with two possible states ('1' and '0'). It can be changed from one state to the other by suitable signals at the input, and without another input remains (remembers) indefinitely in the last state into which it has been set.

A simple method of constructing this element is cross-connecting two NOR gates as shown in Figure A-12. Most available flip-flops have additional circuitry to permit greater versatility and allow for controls. The truth table and logic symbol for any basic flip-flop element are also shown in Figure A-12.

8421 BCD CODE

DECIMAL			8421 CODE
0			0000
1			0001
2			0010
3			0011
4			0100
5			0101
6			0110
7			0111
8			1000
9			1001
10		0001	0000
11		0001	0001
'		'	'
'		'	'
'		'	'
'		'	'
'		'	'
99		1001	1001
'		'	'
'		'	'
'		'	'
285	0010	1000	0101

Figure A-5

BINARY ARITHMETIC OPERATIONS

BINARY ADDITION

A + B = S (Sum)

0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0 & 1 to carry

BINARY SUBTRACTION

A - B = D (Difference)

0 - 0 = 0
0 - 1 = 1 & 1 to borrow
1 - 0 = 1
1 - 1 = 0

BINARY MULTIPLICATION

A x B = P (Product)

0 x 0 = 0
0 x 1 = 0
1 x 0 = 0
1 x 1 = 1

BINARY DIVISION

A ÷ B = Q (Quotient)

0 ÷ 0 = ?
0 ÷ 1 = 0
1 ÷ 0 = ?
1 ÷ 1 = 1

Figure A-6

EXAMPLES OF ARITHMETIC OPERATIONS

ADDITION

```
  1              11
 101101         101101
+ 1010         + 1100
--------       --------
 110111         111001
```

SUBTRACTION

```
 101101         101101
- 1100         -11001
--------       --------
 100001          10100
```

MULTIPLICATION

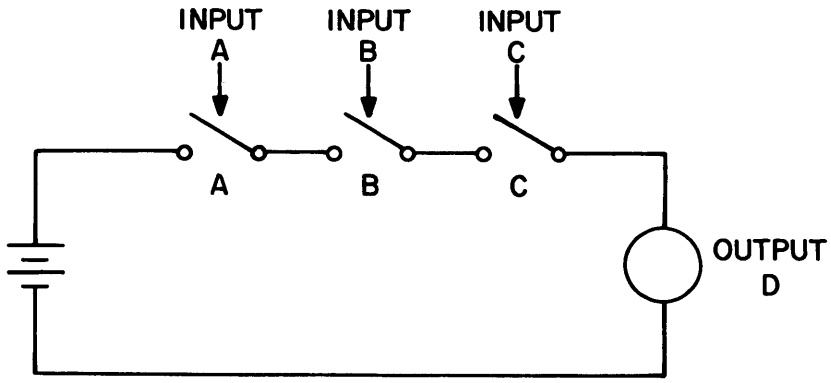
```
   101101
   x  101
   ------
   101101
   00000
 101101
 --------
 11100001
```

DIVISION

```
        1001
   ------------
101 | 101101
      101
      ---
       0001
       0000
       ----
         10
         00
         --
        101
        101
        ===
```

Figure A-7

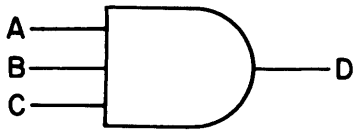
AND LOGIC ELEMENT



ELECTRICAL EQUIVALENT

A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

TRUTH TABLE

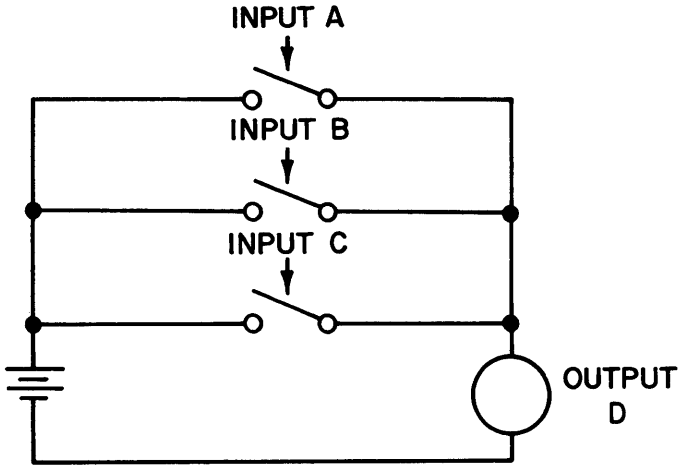


AND

LOGIC SYMBOL

Figure A-8

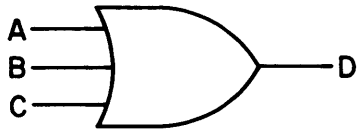
OR LOGIC ELEMENT



ELECTRICAL EQUIVALENT

A	B	C	D
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1

TRUTH TABLE

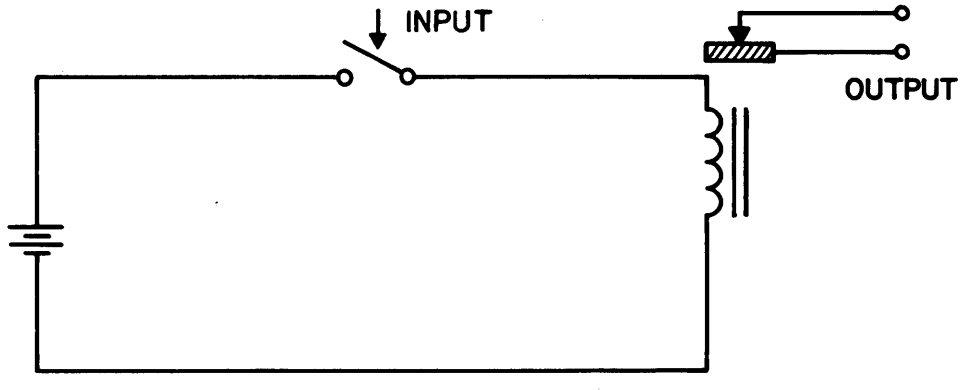


OR

LOGIC SYMBOL

Figure A-9

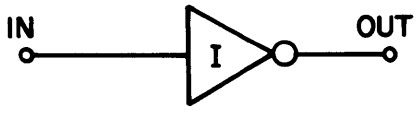
NOT LOGIC ELEMENTS



ELECTRICAL EQUIVALENT

A	$\bar{A}$
0	1
1	0

TRUTH TABLE

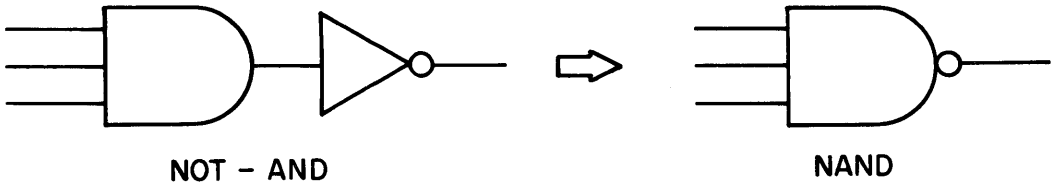


NOT

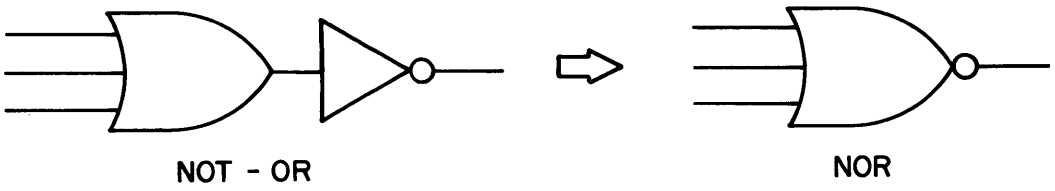
LOGIC SYMBOL

Figure A-10

COMBINED LOGIC FUNCTIONS



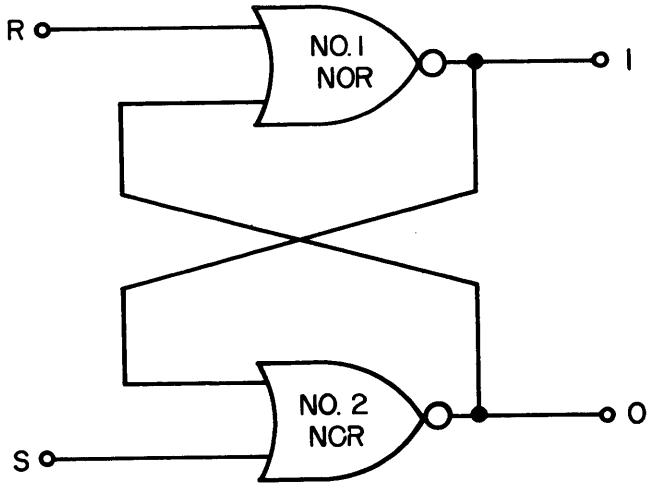
a.



b.

Figure A-11

BASIC FLIP-FLOP CONFIGURATION



TRUTH TABLE

S	R	1	0
0	0	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
1	1	INDETERMINATE	

LOGIC SYMBOL

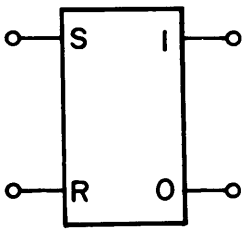


Figure A-12

A.4 Positive-Negative Logic Systems

The logic elements as described were defined on the basis of a positive logic system. However, logic operations also can be carried out in a negative logic system by simply exchanging each '1' for '0' and '0' for '1'. Figure A-13 illustrates the definition of a '1' and '0' in both positive and negative logic systems.

For example, reviewing the OR function in Figure A-9 and redefining it in the negative logic system – inputs A, B and C must be down to keep the output D down. Thus the OR circuit now becomes an AND logic circuit. This illustrates a basic principle: Reversing the definition of the logic levels (positive to negative) changes an OR circuit to an AND circuit. The converse is also true. The use of positive or negative logic is discretionary on the part of logic designers.

A.5 Simple Logic Circuits

In electronic computers, the basic logic functions are implemented in circuit form. The two logic states, '0' and '1' are indicated by voltage levels, as shown in Figure A-14.

The following examples shown practical circuit configurations for implementing the basic logic. A basic AND gate circuit, employing diodes to provide the required 'On' and 'Off' states, is shown in Figure A-15. Similarly, a basic OR gate configuration is shown in Figure A-16. The NOT, or inversions function, can be performed with a simple transistor amplifier, as shown in Figure A-17. For the reasons previously noted, most logic circuits are constructed directly as NAND or NOR elements such as shown in Figure A-18.

A.6 Boolean Algebra

The functions performed by the three basic logic and memory elements also may be expressed in a compact digital circuit language, or algebra, to aid in the analysis of complex logic systems. Boolean Algebra, or the algebra of logic, was invented by George Boole in 1854. He associated the value 'one' with true statements, and 'zero' with false statements. Given a sequence of statements joined by the connectives AND, OR, and NOT, Boole was able to apply his logic to deduce the truth or falsity of the resulting compound statements for any assumption about the component statements.

Boolean AND:
'A and B' is written as: (A·B) or simply as: (AB)

Boolean OR:
'A or B' is written as: (A+B)

Boolean NOT:
'NOT A' is written as: $\bar{A}$

The NOT, or inverse, function notation also applies to complete expressions. For example:

'NOT A and B' is written as $(\overline{AB})$

Parentheses are used to set off isolated expressions, just as they are in ordinary algebra. For example:

'A or B, and C' written as (A+B)C

The basic rules for manipulation of logic functions, by Boolean Algebra, are shown in Figure A-19.

Boolean Algebra is used to simplify system design and eliminate unnecessary logic circuits. Figure A-20 illustrates an example of two combinations of logic functions which perform identically.

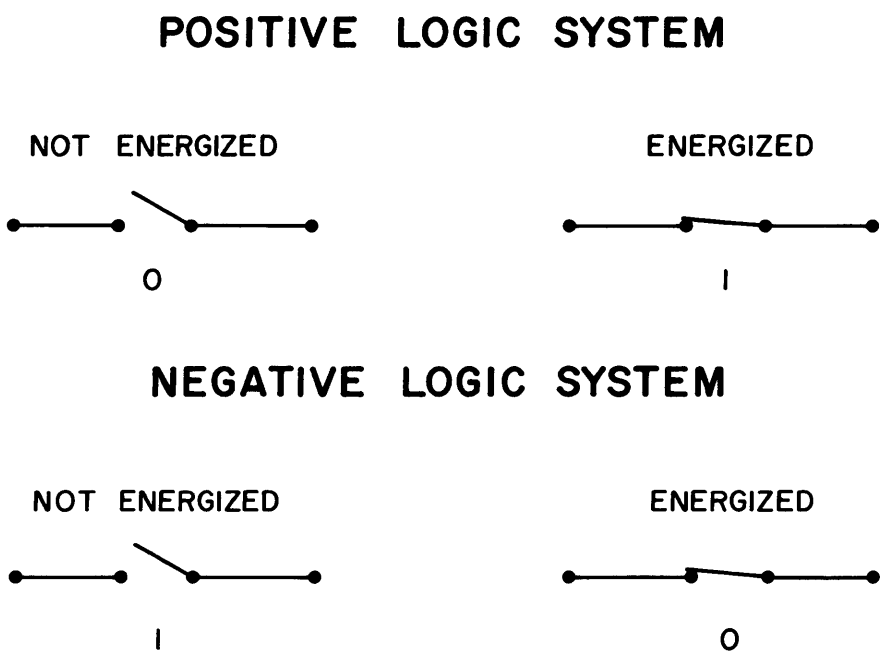


Figure A-13

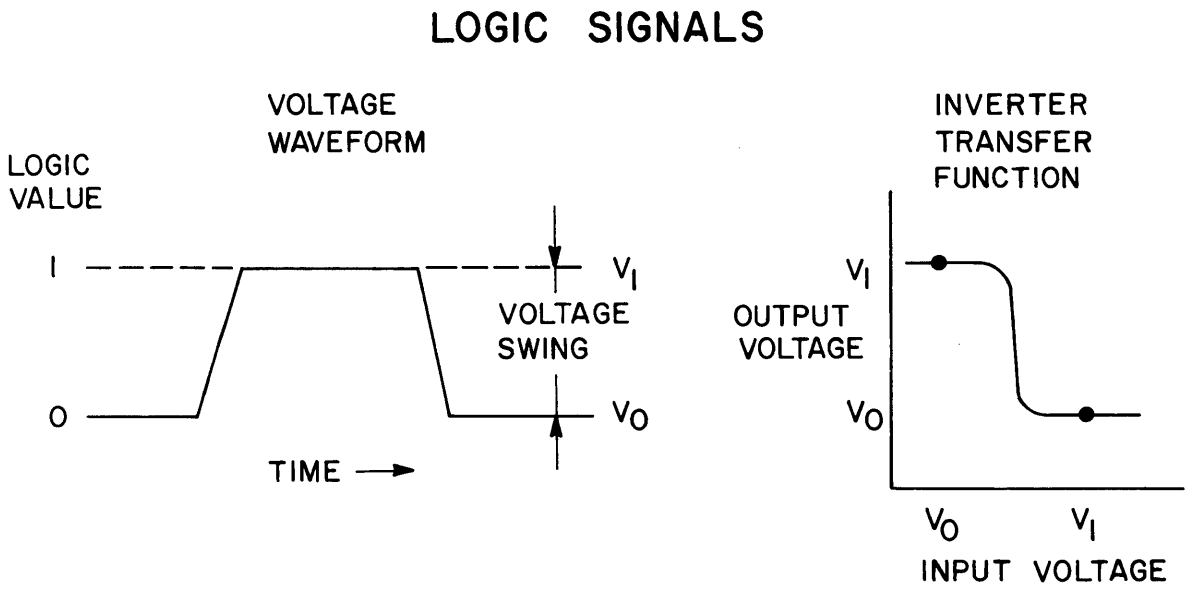


Figure A-14

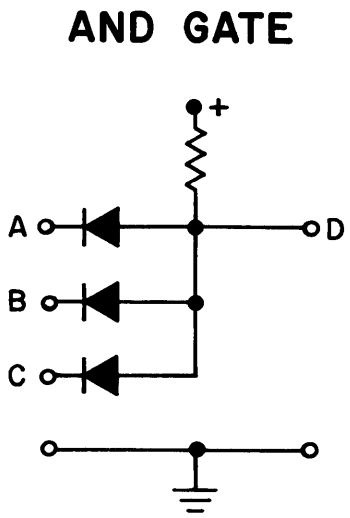


Figure A-15

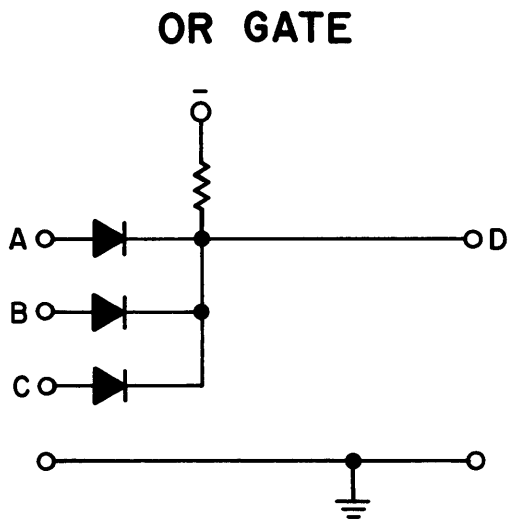


Figure A-16

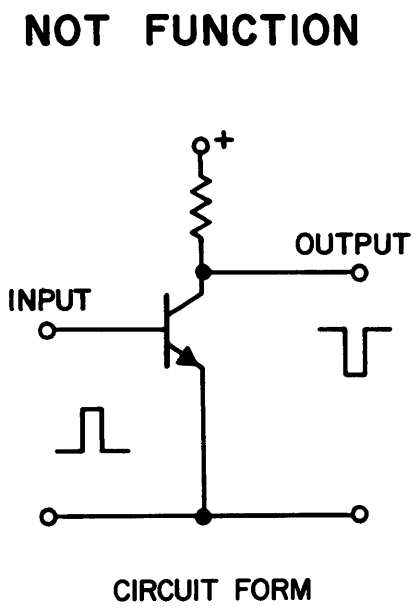
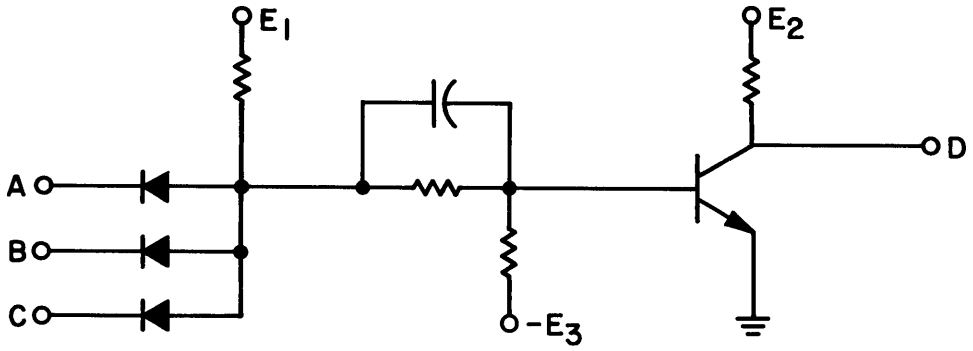


Figure A-17

A BASIC NAND GATE



A BASIC NOR GATE

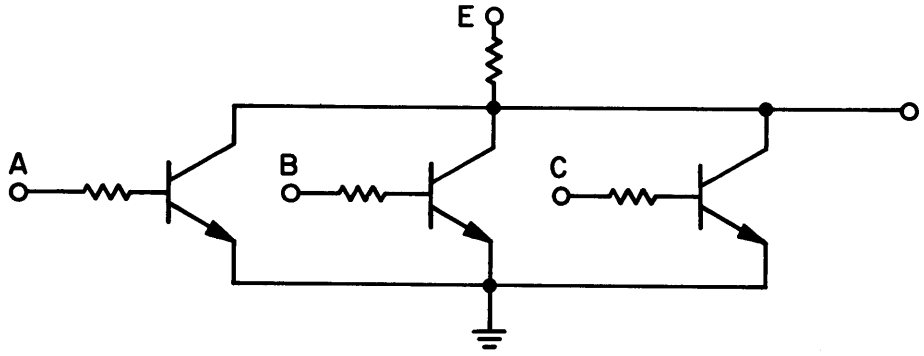


Figure A-18

BOOLEAN ALGEBRA THEOREMS

POSTULATES

1. $A + 0 = A$
2. $A \cdot 1 = A$
3. $A \cdot \overline{A} = 0$
4. $A + \overline{A} = 1$

THEOREMS

1. $A + A = A$
2. $A \cdot A = A$
3. $A + 1 = 1$
4. $A \cdot 0 = 0$
5. $A + AB = A$
6. $A(A+B) = A$
7. $\overline{\overline{A}} = A$
8. $\overline{(A+B)} = \overline{A}\,\overline{B}$
9. $\overline{AB} = \overline{A}+\overline{B}$

DeMORGAN'S THEOREM

10. $(A+B)+C = A+(B+C)$
11. $(AB)C = A(BC)$
12. $A+\overline{A}B = A+B$
13. $A(\overline{A}+B) = AB$
14. $(A+B)(\overline{A}+C) = AC+\overline{A}B$
15. $\overline{(AC+B\overline{C})} = \overline{A}C+\overline{B}\,\overline{C}$
16. $\overline{(A+C)(B+\overline{C})} = (\overline{A}+C)(\overline{B}+\overline{C})$

Figure A-19

CIRCUITS WHICH PERFORM IDENTICAL FUNCTIONS

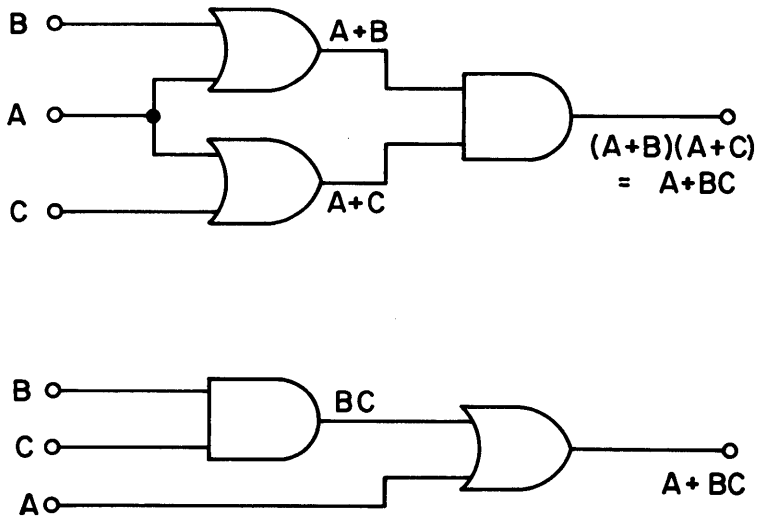


Figure A-20

APPENDIX B GLOSSARY

Alignment	The arranging of the mask and wafer in correct positions, one with respect to the other.
Alignment Pattern	Special patterns which facilitate alignment of the various patterns in their proper positions, usually parts of test patterns.
Amplifier	A device which uses an active component to increase the voltage or power of a signal without distorting its waveshape.
Darlington Amplifier	An amplifier in which the collectors are tied together.
Differential Amplifier	An amplifier which amplifies the voltage difference between two input signals and has two inputs and two outputs.
Batch	The total number of units which are processed at one and the same time.
Black Box	A synonym for an electrical device whose characteristics can be determined only by making measurements and otherwise testing from external leads or terminals.
Bonding	The process of joining one material to another (usually metals), e. g., attachment of the integrated circuit die to the header or substrate or leads to the die.
Ball Bonding	A thermal compression bonding technique used only with gold wire. The wire end is melted to form a ball which provides a larger area of contact than otherwise possible.
Die Bonding	A process which involves the attachment of the integrated circuit chip to the header or substrate.
Stitch Bonding	A thermal compression bonding technique which utilizes a combination of heat and pressure to join fine wires to integrated circuit dice and other materials (usually several wedge bonds).
Thermal Compression Bonding	A method of direct bonding which does not use an intermediary metal or melting, but rather the plastic flow of materials resulting from the combination of heat and pressure.
Ultrasonic Bonding	A bonding technique which utilizes ultrsonic energy and pressure to form the bond.
Wedge Bonding	A form of thermal compression bonding used for microelectronic assembly, so named because a tungsten or tungsten carbide wedge is used.
Bonding Pads	Comparatively large metalization areas usually placed around the perimeter of the integrated circuit die which provide the areas in which wires or other interconnecting contacts are made.
Buried Layer	A low resistivity diffused region placed under the collector to reduce the series resistance of the collector.
Burn-In	The process of applying power to stabilize or adjust electronic components.
Cermet	Is a combination of ceramic and metal powders used for thin film resistors (and thick film).

Chip (Also Die or Dice)	A piece of semiconductor material, usually a section of a silicon wafer, upon which a component or an integrated circuit is fabricated.
Compatible	Compatibility is the quality of being or working with others.
Compatible Circuits	A class of integrated circuits whose components include both monolithic forms and thin films deposited directly on the surface of the monolithic.
Diffusion	Diffusion in integrated circuits, refers to solid state diffusion. It is a process by means of which diffusants are caused to enter a regular crystalline structure in controlled quantities. Their presence tends to change the semiconductor material's electrical characteristics. Solid state diffusions are characteristically conducted at relatively high temperatures under extremely carefully controlled conditions.
Base Diffusion	The diffusion during which the base regions of transistors are formed.
Drive-In	The second part of a two-part diffusion. It is the part of the operation in which the diffusant deposited during predeposition is diffused further into the wafer to achieve the desired impurity profile.
Emitter Diffusion	The diffusion during which the emitters of the transistors are formed.
Isolation Diffusion	A method of achieving isolation by diffusing in such a manner that PN junctions surround the areas to be isolated from one another.
Pre-Deposition	The first part of a two-part diffusion. In this part, a high concentration is diffused shallowly into the surface. This acts as a source for the second or drive-in portion of the process.
Dopant (also Diffusant)	Dopants are the materials used to change the characteristics of a semiconductor crystal.
Epitaxial Growth	Epitaxial growth is a process of growing layers of material on a carefully selected substrate.
Etch	A chemical process of dissolving material.
Etch Cutting	A chemical process used in cutting a wafer into dice.
Selective Etching	Etching which is done so that certain material is dissolved, but other materials are not affected by the etchant.
Failure Rate	A rate of failure per unit time, for example, 3 failures per 164 hours or 1 failure per day, etc.
Fan-In	The number of inputs to a logic element.
Fan-Out	The number of circuits which a logic element is required to drive.
Field Effect Transistors (FET)	A Field Effect Transistor is an active element whose characteristics are determined and controlled by means of potentials imposed from external terminals.
Flip-Chip	An assembly technique in which the integrated circuit chip or component is turned over or "flipped" so that it will be face to face with the substrate or package base.

Integrated Circuit	The term "integrated circuit" has been applied both to a class of very small circuit structures and to a specific circuit structure (monolithic).
Hybrid Thin Film Circuit	These are circuits in which the active components are assembled after the fabrication of the thin film components.
Linear Integrated Circuit	An integrated circuit capable of performing a linear function.
Thin-Film Circuit	Are circuits which are composed of thin film (passive) components.
Integration	Integration is a process whereby the individual components or parts lose their identity as a result of inaccessibility.
Isolation	Isolation is a process of electrically separating electronic components.
Dielectric Isolation	A method of isolating regions of a semiconductor wafer from one another by interposing layers of insulating material.
Diode Isolation	The method of isolating regions of a semiconductor wafer from another, by the use of PN junctions, which in use are reversed biased.
Epitaxial Layer Isolation	Accomplished by diffusing all the way through the thickness of the epitaxial layer, the junctions thus formed by the diffusion when reverse biased, constitute diode isolation.
Resistive Isolation	Accomplished by separating the electronic components to be isolated from one another by high resistivity material.
Large Scale Integration (LSI)	A form of integrated circuit containing a large number of logic elements on one chip frequently requiring several layers for metalization. It is equivalent in complexity to 100 or more gates.
Lateral PNP Transistor	An integrated transistor which is made in such a way that the transistor action is laterally across the surface of the diffusions rather than vertically through the N and P diffusions.
Logic Elements	
AND	Any device having two or more elements and a single output in which the output is in a given state (on) only when all inputs are in the same given state (on).
Clock	In a computer, the accurately timed signals which are used to form signals corresponding to data that are to be or being processed.
Gate	A circuit having an output and a number of inputs so designed that the output is energized when and only when a certain combination of pulses is present at the inputs.
NAND	A combination into a single circuit of the NOT and AND functions.
NOR	A combination into a single circuit of the NOT and OR functions.
NOT (also Inversion)	Any device having a single input and a single output such that the output is in a given state (on) when, and only when, the input is in the opposite state (off).

OR	Any device having two or more inputs and a single output in which the output is in a given state (on) whenever one or more inputs are in the same given state (on) and is off only when none of the inputs are in the given state (on).
Logic Family	A group of logic circuits. The grouping of these circuits is based upon similarities in component grouping or arrangements.
Current Mode Logic (CML)	A form of logic element in which the switching transistors operate in the nonsaturated region.
Complementary Transistor Logic (CTL)	A logic family which uses emitter-coupled AND/OR gates with PNP and NPN transistors.
Direct Coupled Transistor Logic (DCTL)	A form of logic circuit which takes its name from the direct coupling of the output of one stage to the input of the next.
Diode Transistor Logic (DTL)	A form of logic in which series diodes are used to inject input signals and series diodes (with the base) are used to secure proper biasing levels.
Emitter Coupled Transistor Logic (ECTL)	A form of current mode logic in which the output is usually available from an emitter follower output stage.
High Level Transistor-Transistor Logic (HLT^2L)	A form of transistor-transistor-logic which can accommodate large signal voltage swings.
Low Level Logic (LLL)	A form of diode transistor logic which has higher noise pulse immunity, higher speed, larger voltage swing and larger load handling capability as compared to DTL logic circuits.
Resistor Capacitor Transistor Logic (RCTL)	A modification of the DCTL or RTL circuit in which a capacitor is placed in parallel with the base input resistor.
Resistor Transistor Logic (RTL)	A type of DCTL element which has resistors in series with the transistor bases.
Transistor Transistor Logic (TTL or T^2L)	A form of DTL circuit which has the input diode configuration physically modified so that the input appears to be a transistor with one base and collector and the number of emitters corresponding to the number of input diodes.
Low Frequency Characteristics	Those device characteristics which are related to the AC variations of the signals.
Mask	Usually, a photographic device used to control the location or amount of material deposited or removed during a wafer fabrication process.
MCBF	Mean-Cycles-Between-Failures is obtained by dividing mean-time-between-failures by the length of time required to complete one operating cycle.
Metalization	Metalization is the process of depositing a thin film of metal and patterning it to form the desired interconnection arrangement.

Microelectronics	Microscopically small components or circuits made by means of thin film or semiconductor techniques.
Monolithic	A monolitic integrated circuit is one in which all of the components are fabricated within a single piece of material.
Metal-Oxide-Silicon (MOS)	Metal oxide silicon devices employ a structure which is composed of a metal layer usually deposited over a silicon dioxide layer which in turn is formed from a silicon substrate. Field effect transistors and capacitors can be made in this way.
MTBF	Mean-Time-Between-Failures is the reciprocal of the sum of the failure rates of every component in a system.
Multichip	A multichip integrated circuit is one in which each of the components or groups of components is on its own individual chip and these chips are packaged together, within a single package.
Parasitic	A parasitic is an undesirable stray capacitance, inductive coupling, or resistance leakage, as well as undesired transistor actions. The first and last are most serious in monolithic integrated circuits.
Photo Resist (P. R.)	Light sensitive material usually applied in thin films deposited uniformly on the wafer or substrate. They are used to establish the patterns for controlled etching and diffusion.
Planar Process	The "planar process" of forming integrated circuit and semiconductor components is based upon the use of a single surface for referencing each successive operation. The planar process depends upon the repeated use of silicon dioxide (SiO_2) from one surface to control the location of diffusions.
Probing	A term used to describe testing techniques for maintaining process control that employs very finely tipped probes.
Propagation Delay	The propagation delay of a circuit is the finite period of time (delay) measured from the instant when the input signal(s) is applied until the output has reached its final value.
Resolution	The ability to separate between adjacent lines. A mechanical limitation which frequently determines the limits on electrical characteristics.
Sheet Resistance	Sheet resistance is a characteristic of material that is formed in such a way so that its resistivity varies as a function of its cross-sectional structure. Sheet resistance is expressed as R_S in terms of ohms per square, where the square refers to surface area but has no dimensions.
Single Crystal	Is a piece of material having a continuous, regular crystalline lattice structure and having no internal grain boundaries.
Substrate	A substrate is the starting material into or on which circuit components are placed.
Active Substrates	Are silicon wafers containing diffused components, upon which thin films are deposited.
Passive Substrates	Is a glass or ceramic substrate upon which thin film components could be deposited.

Test Pattern	Special pattern arrangements which are used to determine the adequacy of the various processing steps and other testing.
Yield	Yield is the ratio of the number of acceptable units to the maximum number possible.