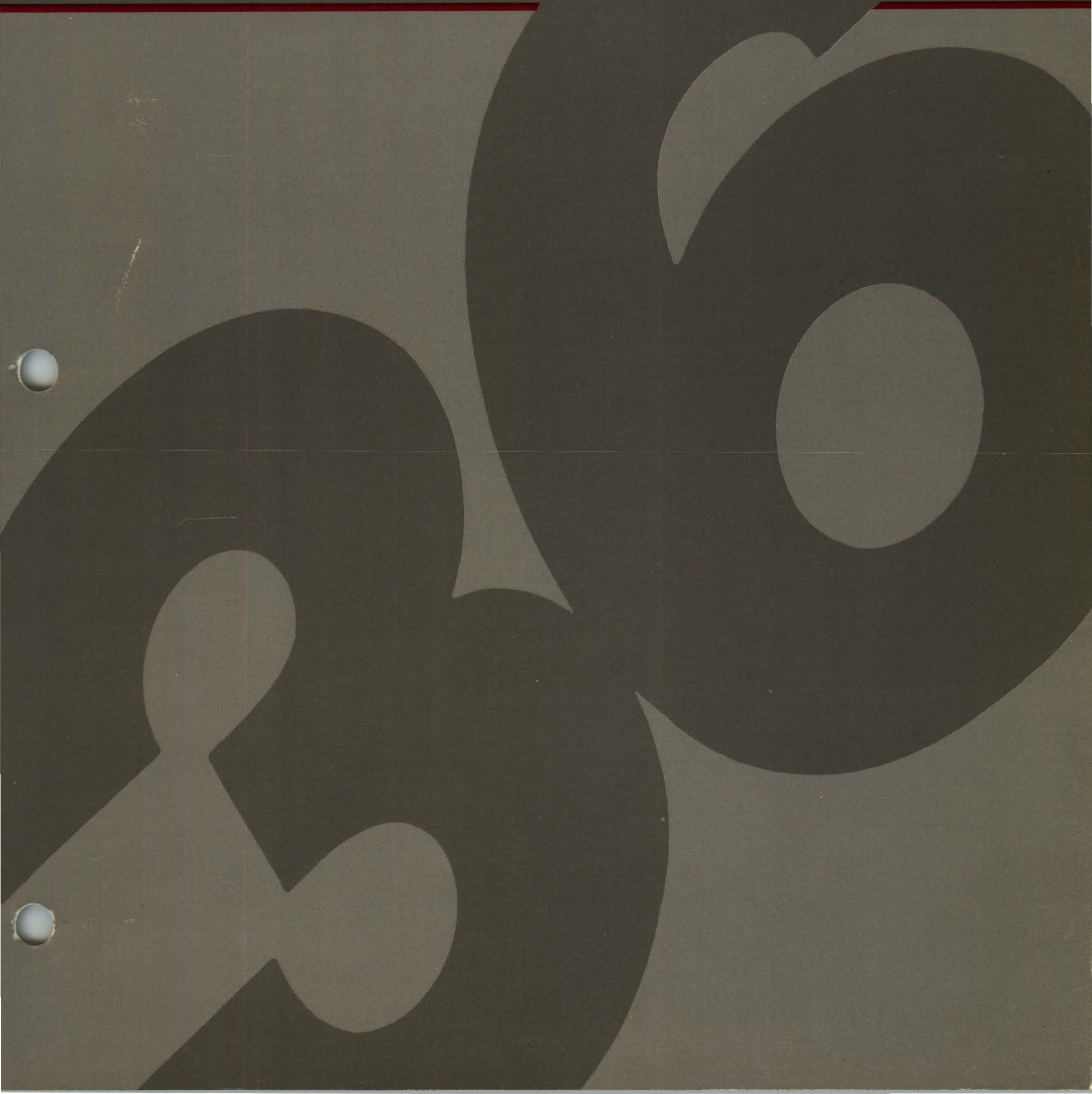
IBM System/36

Functions Reference Manual



IBM System/36

Functions Reference Manual

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This major revision makes obsolete SA21-9436-4.

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Contents

About This Manual

This manual describes the machine instructions, status bytes, and other information needed to understand system programs from the hardware viewpoint.

Who should use this manual . . .

This reference manual is intended for persons interested in the operation and the characteristics of the 5360 System Unit, the 5362 System Unit, and the 5364 System Unit at the machine code level. Readers should be familiar with data processing techniques and should understand programming at the machine code level.

What you should know . . .

Before reading this manual you should be familiar with the information in the following IBM system publications:

- *Data Communications Concepts,* GC21-5169
- *System Reference,* SC21-9020
- *Operating Your System—5360, 5362,* SC21-9452
- *Operating Your System—5364,* SC21-9453
- *System Problem Determination,* SC21-7919 for the 5360 System Unit, SC21-9063 for the 5362 System Unit, or SC21-9375 for the 5364 System Unit.

If you need more information . . .

You might need some or all of the following information while using this manual.

- *System Data Areas*, LY21-0592, provides the IOB bytes for each device and the priority level of the error conditions.

- *Program Problem Diagnosis and Diagnostic Aids,* SY21-0593, tells how to determine the cause of the problem and what to do if the problem continues.

- *Communications and Systems Management Guide*, SC21-8010, contains information about the Communications and Systems Management feature, which includes change management (DSNX support for a DSX network) and problem management (alert support for an NCCF/NPDA network).

- *Diskette General Information*, GA21-9182, provides information on how to load and operate the diskette.

- *System Messages*, SC21-7938, explains the messages you may see on your display screen.

- *Programming with Assembler*, SC21-7908, provides additional information about some of the machine instructions that are used with the assembler.

- *1255 Magnetic Character Reader Reference and Logic Manual*, GN21-8001, provides additional information about how to program and operate the Magnetic Character Reader.

- *X.25 Interface for Attaching IBM SNA Nodes to Packet-Switched Data Networks-General Information Manual*, GA27-3345, provides additional information about the elements of CCITT Recommendation X.25.

- *Enhanced 5250 Emulation Program User's Guide*, G570-2202, provides information for using the IBM Personal Computer as a 5250 work station (display and/or printer).

- *3270 Device Emulation Guide*, SC21-7912, provides configuration and operating information for BSC 3270 device emulation and SNA 3270 device emulation.

- *Scientific Macroinstructions Functions Reference Manual,* SA21-9275, provides information about scientific macroinstructions.

- *Using System/36 Communications,* SC21-9082, provides information about using communications with System/36.

How this manual has changed . . .

The following information has been added since the last edition of this manual:

- 9332 Disk Drive

- 3196 Display Station

- 3197 Display
- 3812 Printer
- 4210 Printer
- 4234 Printer
- 4245 Printer
- Local Area Network (LAN) attachment
- 6157 Tape Drive
- 3270 Remote Attachment
- Increase in main memory size
- Three additional ideographic languages
- Second asynchronous communications line for the 5364 System Unit
- Previously omitted information and diagrams.

Abbreviations and Acronyms

A	add to register
A	address field
ac	alternating current
ACE	action control element
ACK	acknowledgment
ACR	address compare register
ACR	abandon call and retry
ACU	autocall unit
adv	advance
AID	attention identification
ALC	add logical characters
ALI	add logical immediate
ALT	alternate
AL1	arithmetic logical 1
AL2	arithmetic logical 2
AM	amplitude modulation
A/N	alphanumeric
A/N/K	alphanumeric and Katakana
APA	all points addressable
AQE	allocation queue element
ARR	address recall register
ASCII	American National Standard Code for Information Interchange
ASF	auto sheet feed
ATR	address translation register
AZ	add zoned decimal

BC	branch on condition
BCC	block check character
BOR	beginning of read
BOT	beginning of tape
bpi	bits per inch
bps	bits per second
BSC	binary synchronous communications

C	control field
CC	completion code
cc	cause code
CCITT	Consultative Committee on International Telegraphy and Telephony
CCR	configuration control register
CE	customer engineer
CF	Cluster feature
CGCS	coded graphic character set
CHRNX	cylinder, head, record length, number of records

CLC	compare logical characters
CLI	compare logical immediate
CMR	control mode register
COD	change of direction
CPI	characters per inch
CPGID	code page global identification
CPS	call progress signal
CRC	cyclic redundancy check
CRQ	call request
CS	communication services
CSB	common storage block
CSIPL	control storage initial program load
CSP	control storage processor
CTF	continuous forms
CTS	clear to send

D	delete record
dd	diagnostic code
DBA	data buffer address
DBI	data bus in
DBO	data bus out
DCB	data control block
DCL	device control language
DCP	diagnostic control program
DDFF	distributed disk file facility
DDSA	Digital Data Service Adapter
DFCA	device function controller attachment
DID	document insertion device
DISC	disconnect
DE	disk enclosure
DLE	data link escape
DLE SYN	transparent synchronous idle
DLO	data line occupied
DM	disconnected mode
DMA	direct memory access
DOD	document on demand
DP	data processing
DPQ	data processing quality
DPR	digit present
DQ	draft quality
DSA	data storage attachment
DSC	distant station connected or data storage controller
DSR	data set ready
DSX	distributed systems executive
DSNX	distributed systems node executive
DTE	data terminal equipment
DTR	data terminal ready
DTF	define the file
DTT	define the table
DUB	device unit block

EC	exemption condition (5219)
EBCDIC	extended binary coded decimal interchange code
ECC	error checking and correction
ECM	event control mask

ED	edit
EIA/CCITT	Electronic Industries Association/Consultative Committee on International Telegraphy and Telephony
ELCA	eight-line communications attachment
ELLC	enhanced logical link control
ENQ	enquire
EOT	end of transmission or end of tape
EOJ	end of job
ERB	error recovery block
ERAP	error recording and analysis procedures
ETB	end of transmission block
ETX	end of text
F	flag
FC	frame check
FCS	frame check sequence
FDIOCH	fixed disk input output control handler
FDIOS	fixed disk input output supervisor
FID	font identification
FIFO	first-in-first-out
FMD	function management data
FRMR	frame reject
GCGID	graphic character set global identification
GCID	global character set identification
GFI	general failure index
GFID	graphic font identification
H	head
HDX	half-duplex
HDLC	high level data link control
I	information field
I/O	input/output
IAR	instruction address register
ID	identification
IDE	information description element
IDEO	ideographic
IPDS	intelligent printer data stream
IGC	ideographic character
IOB	input/output block
IOCH	input/output control handler
IOS	input/output supervisor
IPL	initial program load
ips	inches per second
IRS	inter record separator
ITB	intermediate text block
ITC	insert and test characters
IUS	intermediate unit separator
JC	jump on condition
kbd	keyboard

L	load
LA	load address
LAC	load alternate characters
LAN	Local Area Network
LC	logical channel
LCCB	logical channel control block
LCD	liquid crystal display
LCGN	logical channel group number
LCI	logical channel indicator
LCID	logical channel identification
LCN	logical channel number
LCRN	logical channel reference number
LCRR	length count recall register
LCT	logical channel table
LED	light-emitting diode
LGID	local character set identification
LIFO	last-in-first-out
LLC	logical link control
LPDA	link problem determination aids
LPI	lines per inch
LPMR	load program mode register
LRC	longitudinal redundancy check
LSD	Index Down key on 5219 Printer
LU	logical unit
MAB	memory address buffer
MCR	magnetic character reader
MDT	modify data tag
MIC	message identification code
MLCA	multiline communications attachment
MLT	modified line tag
MPL	main program level or maximum page length
MRJE	multi-leaving remote job entry
MSAR	main storage address register
MSD	Index Up key on 5219 Printer
MSF	manual sheet feed
MSIPL	main storage initial program load
MSP	main storage processor
MSR	magnetic stripe reader
MVC	move characters
MVI	move logical immediate
MVX	move hexadecimal character
NAC	network access control
NAK	negative acknowledgment
NAP	network access processor
NCB	network control block
NCP	network control parameter
NDM	normal disconnect mode
NEP	never ending program
NIU	network information unit
NLQ	near letter quality
NPDA	network problem determination application
Nr	number received
NRF	no record found
NRM	normal response mode

NRZI	nonreturn to zero inverted
Ns	number sent

OC	over current
OCB	operations control block
OCR	optical character reader
OV	over voltage

P/F	poll/final
PACT	prefix address contained translation register
PAR	program address register
PATR	PACT register for ATRs
PCPL	physical current print line
PCSP	PACT register for CSP access
PDS	printer data stream
PIAR	PACT register for IARs
PIC	parent interconnect control
PIO	programmed I/O
PIU	path information unit
PLA	programmable logic array
PLO	phase lock oscillator
PMR	program mode register
PND	present next digit
PPQ	process pending queue
Pr	packet receive sequence number
PREG	PACT register for register area
PRPQ	programming request for price quotation
Ps	packet send sequence number
PSDN	packet switching data network
PSH	physical service header
PSM	proportional spacing mode
PSR	program status register
PTIOCH	printer terminal input/output control handler
PU	physical unit
PUB	printer unit block
PUBQHDR	printer unit block queue handler
PVC	permanent virtual circuit
PWI	power indicator

QHDR	queue header
QLLC	qualified logical link control

R	record number
RD	request disconnect
RDOTF	read data on the fly
RDS	receive data space
RFM	read file mark
RID	receive initial delayed
RIM	request initialization mode
RNR	receive not ready
ROTF	read file mark on the fly
RPM	revolutions per minute
RPOA	recognized private operating agency
RQD	request definite response
RR	receive ready

RSDL	receive signal line detect
RSP	response
RTS	request to send
RVI	reverse interrupt
S	subtract from register
SABM	set synchronous balanced mode
SBF	set bits off masked
SBN	set bits on masked
SCS	SNA character string
SCT	subsystem control table
SDLC	synchronous data link control
SERDES	serialization deserialization
SFD	select font density
SHM	short-hold mode
SI	shift in
SICB	serial interface control block
SLC	subtract logical characters
SLCA	single line communications attachment
SLI	subtract logical immediate
SMF	system measurement facility
SNA	systems network architecture
SNBU	switched network backup
SNRM	set normal response mode
SO	shift out
SOH	start of header
SQS	station queue space
SRC	shift right character or system reference code
SSP	System Support Program Product
SSP-ICF	System Support Program Product-Interactive Communications Feature
SST	station state table
ST	store register
STX	start of text
SUBR	subroutine
SVC	supervisor call or switched virtual circuit
SYN	synchronous idle
SZ	subtract zoned decimal
TB	task block
TBF	test bits off
TBN	test bits on
TCB	terminal control block
TDS	transmit data space
TI	test indicate
TOF	top of form
TTD	temporary text delay
TUB	terminal unit block
UA	unnumbered acknowledgment
UDT	unit definition table
UPSI	user program status indicator
UV	under voltage

VC	virtual circuit
VCB	virtual circuit block
VCP	virtual circuit parameters
VRC	vertical redundancy check
WACK	wait before transmit-positive acknowledgment
WFM	write file mark
WMPR	write micro processor register
WP	word processing
WSC	work station controller
WSCF	work station control field
WSDM	work station data management
WSIOCH	work station input/output control handler
WSQS	work station queue space
WSWA	work station work area
XDLE	transparent data link escape
XENQ	transparent block cancel
XETB	transparent end of text block
XETX	transparent end of text
XFD	transmit frame description
XFER	transfer
XID	exchange station identification
XITB	transparent intermediate block
XMIT	transmit
XR	index register
XSTX	transparent start of text
XSYN	transparent synchronous idle
XTTD	transparent temporary text delay
ZAZ	zero and add zoned

Chapter 1. What These Systems Are

The IBM System/36 is a 5360 System Unit, a 5362 System Unit, or a 5364 System Unit, which are small interactive data processing systems that are usually used to control many work stations. They work in both batch mode and in a multiprogramming environment. The following table, Figure 1-1, lists the available system hardware:

Function	5360 System Unit	5362 System Unit	5364 System Unit
Main Storage	--	--	--
128 kilobytes	Standard	Standard	Not available
256 kilobytes	Feature	Feature	Discontinued
384 kilobytes	Feature	Feature	Not available
512 kilobytes	Feature	Feature	Not available
768 kilobytes	Feature	Feature	Not available
1024 kilobytes	Feature	Feature	Standard
2048 kilobytes	Feature	Feature	Not available
3072 kilobytes	Feature	Not available	Not available
4096 kilobytes	Feature	Not available	Not available
5120 kilobytes	Feature	Not available	Not available
6144 kilobytes	Feature	Not available	Not available
7168 kilobytes	Feature	Not available	Not available
Disk Storage	--	--	--
30.8 megabytes	Standard	Standard	Not available
41.9 megabytes	Not available	Not available	Standard
61.6 megabytes	Not available	Feature	Not available
83.8 megabytes	Not available	Not available	Feature (on Model A01) Standard (on Model B01)
92.5 megabytes	Not available	Feature	Not available

Figure 1-1 (Part 1 of 5). System Hardware and Features

Function	5360 System Unit	5362 System Unit	5364 System Unit
123.3 megabytes	Not available	Feature	Not available
200.9 megabytes	Feature	Not available	Not available
261.6 megabytes	Not available	Feature	Not available
292.5 megabytes	Not available	Feature	Not available
323.3 megabytes	Not available	Feature	Not available
359.7 megabytes	Feature	Not available	Not available
401.8 megabytes	Feature	Not available	Not available
461.6 megabytes	Not available	Feature	Not available
492.5 megabytes	Not available	Feature	Not available
523.3 megabytes	Not available	Feature	Not available
602.7 megabytes (discontinued)	Feature	Not available	Not available
719.3 megabytes	Feature	Not available	Not available
761.5 megabytes	Feature	Not available	Not available
803.6 megabytes (discontinued)	Feature	Not available	Not available
1079.0 megabytes	Feature	Not available	Not available
1121.1 megabytes	Feature	Not available	Not available
1438.6 megabytes	Feature	Not available	Not available
Diskette Drive	--	--	--
51TD	Standard	Standard	Emulated
72MD	Feature	Not available	Not available
5-1/4 inch drive	Not available	Not available	Standard
Tape Drive	--	--	--
8809	Feature	Not available	Not available
6157	Feature	Feature	Feature
1255 Magnetic Character Reader	Feature	Not available	Not available
Communications	--	--	--
Communications attachment	Standard	Standard	Available through the IBM Personal Computer
SLCA	Feature	Feature	Not available
MLCA	Feature	Feature	Not available
ELCA	Feature	Not available	Not available
X.21	Feature	Feature	Not available
V.35	Feature	Feature	Not available

Figure 1-1 (Part 2 of 5). System Hardware and Features

Function	**5360 System Unit**	**5362 System Unit**	**5364 System Unit**
EIA	Feature	Feature	Not available
EIA (autocall)	Feature	Feature	Not available
DDSA	Feature	Feature	Not available
1200 BPS integrated modem	Feature (see Note 4)	Not available	Not available
LAN Attachment	Feature	Feature	Available through the IBM Personal Computer
5170 used as LAN controller	See Note 5	See Note 5	Not available
X.25	Feature	Feature	Not available
Console with Display Screen and Keyboard	One required	One required	IBM Personal Computer
Local Work Station witih Display Screen and Keyboard	--	--	--
3179 Model 2	See Note 1	See Note 1	Available
3180 Model 2	See Note 1	See Note 1	Available
3196	See Note 1	See Note 1	Available
3197 Model C	See Note 1	See Note 1	Available
3197 Model D	See Note 1	See Note 1	Available
5251 Model 11	See Note 1	See Note 1	Available
5291	See Note 1	See Note 1	Available
5291-2	See Note 1	See Note 1	Available
5292 Model 1	See Note 1	See Note 1	Available
5292 Model 2	See Note 1	See Note 1	Available
5555 Model B01	See Note 1	See Note 1	Not available
Personal Computer with 5250 Emulation	See Note 1	See Note 1	Standard
3270 Remote Attachment	Feature	Feature	Feature
3270 Emulation	Feature	Feature	Not available
Magnetic Stripe Reader	Feature	Feature	Not available
Local Work Stations	6 basic, 36, or 72 feature	6 basic or 28 feature	6 basic and 16 feature
Maximum Remote Work Stations	64	64	64
Additional work station attachment	--	--	--

Figure 1-1 (Part 3 of 5). System Hardware and Features

Function	**5360 System Unit**	**5362 System Unit**	**5364 System Unit**
First additional work station attachment	Feature	Feature	Not available
Second additional work station attachment	Feature	Not available	Not available
Remote Work Station Controllers	--	--	--
5251 Model 12	Feature	Feature	Feature
5294	Feature	Feature	Feature
Personal Computer with 5294 Emulation	Feature	Feature	Feature
Printers	--	--	--
3262 Model B1	See Note 3	Not available	Not available
3550	Not available	Not available	Available
3812	See Note 2	See Note 2	Available
4210 Printer	See Note 2	See Note 2	Available
4214 Model 2	See Note 2	See Note 2	Available
4224 Model 1	See Note 2	See Note 2	Available
4224 Model 2	See Note 2	See Note 2	Available
4234	See Note 2	See Note 2	Available
4245 Model T12	See Note 2	See Note 2	Available
4245 Model T20	See Note 2	See Note 2	Available
5216	Not available	Not available	Available through the IBM Personal Computer
5219 Model D01	See Note 2	See Note 2	Available
5219 Model D02	See Note 2	See Note 2	Available
5224 Model 1	See Note 2	See Note 2	Available
5224 Model 2	See Note 2	See Note 2	Available
5224 Model 12	See Note 2	See Note 2	Not available
5225 Model 1	See Note 2	See Note 2	Available
5225 Model 2	See Note 2	See Note 2	Available
5225 Model 3	See Note 2	See Note 2	Available
5225 Model 4	See Note 2	See Note 2	Available
5225 Model 11	See Note 2	See Note 2	Not available
5225 Model 12	See Note 2	See Note 2	Not available

Figure 1-1 (Part 4 of 5). System Hardware and Features

Function	5360 System Unit	5362 System Unit	5364 System Unit
5256 Model 1	See Note 2	See Note 2	Available
5256 Model 2	See Note 2	See Note 2	Available
5256 Model 3	See Note 2	See Note 2	Available
5262 Model 1	See Note 2	See Note 2	Not available
5553 Model B01	See Note 2	See Note 2	Not available
5557 Model B01	See Note 2	See Note 2	Not available

Figure 1-1 (Part 5 of 5). System Hardware and Features

Notes:

1. *The base system requires at least one native or local display which will be the system console.*

2. *The base system requires a native or local printer and these printers can be used for local printers.*

3. *The 3262 cannot be used as a remote printer.*

4. *The 1200 BPS integrated modem (38LS) is available with SLCA (feature code 2500) and MLCA on the 5360 System Unit.*

5. *The LAN attachment requires an IBM PERSONAL COMPUTER AT® as a LAN controller on the 5360 and 5362 System Units.*

The system overlaps operations of the input/output devices with each other and with processing unit operations.

Parts of the System

Main Storage Processors, Control Storage Processors, and Data Storage Controllers

The system's processor has a main storage processor, an integrated control storage processor, and a data storage controller that supply some of the arithmetic, supervisor, and logical functions, and all the input/output control functions for the system.

The smallest main storage size is 131,072 (128K) 8-bit data bytes. The 5360 System Unit can be ordered with up to 7,302,684 (7M) 8-bit bytes of main storage. The 5362 System Unit can be ordered with up to 2,097,152 (2M) 8-bit bytes of main storage. The 5364 System Unit can be ordered with up to 1,048,576 (1M) 8-bit bytes of main storage. See Figure 1-1 for main storage size available.

Control storage on the system contains 64K 16-bit words (128K bytes), which are available for control use.

The data storage controller of the 5360 System Unit and 5362 System Unit Model C processes disk I/O, diskette I/O, and tape I/O (on systems that have the tape attachment). This data storage controller also transfers data from device to device.

The system uses a 2-byte wide I/O channel and can provide 2-bytes at a time from the main storage or control storage.

Display Stations

The operator uses the display station to enter data to the system and to communicate with the system. Each keyboard can contain a set of alphameric keys (in the standard typewriter pattern), a set of adding machine keys in 10-key pattern, and a set of function keys which the operator uses to select system functions. The display screen displays data and messages. Under program control, the main storage data and the contents of registers can be displayed on the display screen and, if desired, changed by using the keyboard.

Refer to Chapter 6 in this manual for additional information on the displays.

Personal Computer 5250 Emulation

The IBM Personal Computer with the Enhanced 5250 Emulation Program supports the IBM 5250 Information Display System. The Emulation Program allows the Personal Computer to emulate (imitate the functions of) the IBM 5250 display stations and printers and to use the functions of the host. The attachment and program allow the Personal Computer to perform the function of two work stations at the same time on one twinaxial cable. For more information, refer to *Enhanced 5250 Emulation Program User's Guide* , G570-2202.

3179 Model 2 Display Station

The 3179 Model 2 Display Station is fully buffered and is used for inquiry and data entry applications.

The display station can display up to 1920 characters at the same time. The characters are displayed in 24 rows with 80 characters in each row.

It may be used as the system console, as a work station, or as a remote work station.

When connected as a remote work station, the display station may be attached only through the 5294 Work Station Controller.

The 3179 Model 2 is a color display.

3180 Model 2 Display Station

The 3180 Model 2 Display Station is fully buffered and is used for inquiry and data entry applications.

The display station can display up to 3564 characters at the same time. The characters can be displayed in 24 rows with 80 characters in each row for a total of 1920 characters or in 27 rows with 132 characters in each row for a total of 3564 characters.

The 3180 Display Station may be used as the system console, as a work station, or as a remote work station. When connected as a remote work station, it may be attached only through the 5294 Work Station Controller.

3196 Display Station

The 3196 Display Station is fully buffered and is used for inquiry and data entry applications.

The display station can display up to 1920 characters at the same time. The characters are displayed in 24 rows with 80 characters in each row.

It may be used as the system console, as a work station, or as a remote work station.

When connected as a remote work station, the display station can be attached only through the 5294 Work Station Controller.

The 3196 Display Station Models A1 and A2 display green letters on a black screen. The 3196 Display Station Models B1 and B2 display amber letters on a black screen.

5251 Display Station

The 5251 Display Station is fully buffered and is used for inquiry and data entry applications.

The display station can display up to 1920 characters at the same time. The characters are displayed in 24 rows with 80 characters in each row.

It may be used as the system console, as a work station, or as a remote work station.

5291 Display Station Models 1 and 2

These display stations are fully buffered and are used for inquiry and data entry applications.

The 5291 Display Station can display up to 1920 characters at the same time. The characters are displayed in 24 rows with 80 characters in each row.

The 5291 Display Station may be used as the system console, as a work station, or as a remote work station.

5292 Display Station Models 1 and 2

The 5292 Display Station is fully buffered and is used for inquiry and data entry applications.

The display stations can display up to 1920 characters at the same time. The characters are displayed in 24 rows with 80 characters in each row.

It may be used as the system console, as a work station, or as a remote work station.

The 5292 Model 1 is a color display, and the 5292 Model 2 is a color with graphics display.

5555 Display Station (Ideographic Feature Required)

The 5555 Display Station is a fully buffered display consisting of a display screen only. This display (when used with a separately ordered keyboard) is used to enter and display ideographic, alphanumeric (A/N), and Katakana characters.

The display screen can display 24 rows of information containing 80 alphanumeric-Katakana (A/N/K) or 40 ideographic character positions per row.

The 5555 Display Station may be used as the system console, as a work station, or as a remote work station. When connected as a remote work station, it may be attached only through the 5294 Work Station Controller.

Printers

The different printers provide a variety of printing speeds, type fonts, line spacing, and quality of printing to satisfy your special needs.

Refer to Chapter 5 in this manual for additional information on the printer models and speeds.

3262 Printer

The 3262 Printer supplies fully buffered print rates of 650 lines per minute (3262 Model B1) with a 48-character set and 132 print positions. Other character set belts are also available, but the print speed may change with different character set belts. The printer has a carriage that permits printing of either 6 or 8 lines per inch, with the control of a switch. The 3262 Printer is not available on the 5362 and 5364 System Units.

3812 Printer

The 3812 Pageprinter is a nonimpact, electrophotographic, desk-top printer. It uses a light-emitting diode printhead and produces letter quality single-sided printed output.

It is an automatic cut-sheet feed printer capable of a maximum throughput of 12 pages per minute.

4210 Printer

The 4210 Printer is a table-top, wire matrix printer that consists of an IBM Proprinter XL (420L) with an integrated protocol converter and a redesigned operator panel.

It is a multiple speed print quality printer capable of 200 cps in data processing (DP) quality and 40 cps in near letter quality (NLQ).

4214 Printer

The 4214 Printer is a wire matrix printer that prints serially at 200 characters per second at data processing quality and 50 characters per second at near letter quality.

4224 Printer

The 4224 Printer is a wire matrix printer that prints serially at a maximum of 200 characters per second (4224 Model 101) or 400 characters per second (4224 Models 102, 1E2, and 1C2) when in draft quality mode.

The 4224 Printer operates with intelligent printer data stream commands.

The printer provides a draft quality document or a near letter quality document.

4234 Printer

The 4234 Printer is a dot band, impact, matrix printer. The print bands are changeable to provide variable dot sizes.

The printer offers three print qualities: draft, data processing, and near letter quality.

The 4234 Printer's average print speed is 300 lines per minute in data processing mode, with 6 lines per inch and 10 characters per inch.

4245 Printer

The 4245 Printer is an engraved band, impact printer. It is capable of printing 6-part forms. This printer is available in two models (T12 and T20). With a 48-character print band, these models are capable of 1200 and 2000 lines per minute, respectively.

5219 Printer

The 5219 Printer is a letter quality printer that prints characters by using a print wheel. The character set can be changed by changing the print wheel. The printer (depending on the model number and the command sent) prints 40 or 60 characters per second and does proportional spacing or spaces the characters at 10, 12, or 15 characters per inch.

5224 and 5225 Printers

The 5224 and the 5225 Printers print characters by using a series of dots in a matrix. The characters are made by printing a pattern of dots that matches a stored image in the printer. There are fifteen 95-character sets and one 184-character set available. The 5224 Printers are available in Models 1, 2, and 12. The 5225 Printers are available in Models 1 through 4, 11, and 12. The print speeds of the printers are 95 to 560 lines per minute. The maximum line length is 198 print positions at 15 characters per inch spacing and 132 print positions at 10 characters per inch spacing. Refer to Chapter 5 in this manual for additional information on the printer models and speed.

The printers can be set by manual selection to print at 4 or 8 lines per inch:

- 4 or 6 for 5224 Model 12 and 5225 Models 11 and 12.
- 6 or 8 for 5224 Models 1 and 2, and 5225 Models 1, 2, 3, and 4.

The printers can be set by program control (depending on the configuration) to print 4 to 8 lines per inch.

Note: *Speed depends on line length, spacing, and line skipping. The speed does not vary with the character set. A remote printer might not operate at its rated speed because of a slower communications line speed.*

5256 Printer

The 5256 Printer prints in both directions at 40, 80, or 120 characters per second. This printer prints characters by using a series of dots in a matrix; characters are made by printing a pattern of dots that match a stored image in the printer adapter. The print line can be up to 132 characters long. In addition, the printer has a switch controlled carriage that permits printing of either 6 lines per inch or 8 lines per inch.

5262 Printer

The 5262 Printer prints 650 lines per minute with a 48-character set and using 132 characters per line. Other character set belts are also available, but the print speed may change with different character set belts. In addition, the printer has a switch controlled carriage that permits printing of either 6 lines per inch or 8 lines per inch.

5553 and 5557 Printers (Ideographic Only)

The 5553 and 5557 Printers print ideographic characters by using a series of dots in a matrix that matches a stored image in the printer. The 5553 and 5557 Printers (at 6 lines per inch) print 60 or 90 characters per second with 80 or 132 print positions, respectively.

Disk Storage

Each system model has disk storage that is internal. The 5362 System Unit also has disk storage that is external. Refer to Figure 1-1 for the size of the drives used on each system configuration.

Diskette Drive

Each system model has a diskette drive. The 5360 and 5362 System Units use IBM diskette 1, IBM diskette 2D, or equivalent diskettes. The 5364 System Unit uses IBM 5-1/4 inch or equivalent diskettes. This permits the 5360 and 5362 System Units to read diskettes written by IBM 3741 Data Stations, and similar devices, and to exchange data with other systems. Data and programs can also be written on diskettes, then stored offline to use if the operating diskette gets damaged.

Data on diskettes that are not used on other systems need not be in the basic data exchange format.

The data on the diskettes can be compressed by using the diskette data compression command.

Model	Diskette Density	System Unit
51TD	1D, 2D	5360 and 5362
72MD	1D, 2D	5360
5-1/4 inch diskette drive	1D, 2D	5364

Figure 1-2. Diskette Drive and Density

8809 Tape Drive

The 5360 System Unit can have one or two 8809 Tape Drives attached.

6157 Tape Drive

The 5360, 5362, and 5364 System Units can have one 6157 Tape Drive attached.

Magnetic Character Reader

The 5360 System Unit can have a 1255 Magnetic Character Reader (MCR) attached.

Data Communications Features

Three telecommunications attachments are available for the system: the single-line communications attachment (SLCA), the multiline communications attachment (MLCA), and the eight-line communications attachment (ELCA). The eight-line communications attachment (ELCA) is available only on the 5360 System Unit. Only one telecommunications attachment can be installed and operated at a time. All three telecommunications attachments supply binary synchronous communications (BSC) and synchronous data link control (SDLC). The MLCA or ELCA on the 5360 and 5362 System Units also support X.25.

The SLCA or MLCA support asynchronous communications on the 5362 System Unit. The ELCA or SLCA (feature code 2550) support asynchronous communications on the 5360 System Unit. The IBM Personal Computer supports asynchronous communications for the 5364 System Unit.

In addition to the telecommunications attachments, you can attach a Local Area Network (LAN) attachment. The LAN attachment uses an IBM 5170 Personal Computer as the controller for two LAN ports on the 5360 and 5362 System Units. The IBM Personal Computer, used as the system console on the 5364 System Unit, provides the equivalent function.

SLCA Data Rates

The single-line communications attachment can operate at data rates of 600 to 9600 bits per second. If the asynchronous communication is used, data rates can be 75 to 9600 bits per second.

The 5362 will allow a second SLCA communications line. This second line is used with asynchronous communications and can operate at 75 to 9600 bits per second.

MLCA Data Rates (5362 System Unit)

The multiline communications attachment for the 5362 System Unit can control one to four communications lines at the same time. Each of the MLCA communications lines 1 through 4 can operate at data rates of 600 to 19,200 bits per second (75 to 9600 bits per second if asynchronous communication is used). Any one, but only one, of the MLCA communications lines can operate at a speed greater than 19,200 bits per second, and the maximum line speed is 57,600 bits per second. The maximum MLCA accumulated line speed of the four lines is 115.2K bits per second. The maximum line speed of an X.25 line is 19,200 bits per second when operating only one X.25 line and 9600 bits per second when operating two or more X.25 lines. X.25 is a full duplex operation, so the line speed must be counted twice when figuring the maximum accumulated line speed. Only one V.35 line is allowed.

MLCA Data Rates (5360 System Unit)

The multiline communications attachment for the 5360 System Unit can control one to four communications lines at the same time. Each of the MLCA communications lines 1 through 4 can operate at data rates of 600 to 9600 bits per second. Only the MLCA communications line 4 can operate at data rates of 600 to 57,600 bits per second. The maximum MLCA accumulated line speed of the four lines is 67.2K bits per second. The maximum line speed of an X.25 line is 9600 bits per second. X.25 is a full duplex operation, so the line speed must be counted twice when figuring the maximum accumulated line speed. Only one V.35 line and one X.25 line is allowed.

ELCA Data Rates (5360 System Unit)

The eight-line communications attachment (ELCA) for the 5360 System Unit can control one to eight communications lines at the same time.

Any of the ELCA communications lines can operate at a speed of 600 to 19,200 bits per second (75 to 9600 bits per second if asynchronous communication is used). Any one, but only one, of the ELCA communications lines can operate at a speed greater than 19,200 bits per second, and the maximum line speed is 57,600 bits per second. The maximum ELCA accumulated line speed is 170K bits per second.

The maximum line speed of an X.25 line is 19,200 bits per second when operating only one X.25 line and 9600 bits per second when operating two or more X.25 lines. X.25 is a full duplex operation, so the line speed must be counted twice when figuring the maximum accumulated line speed. Only one V.35 line is allowed.

Data Formats

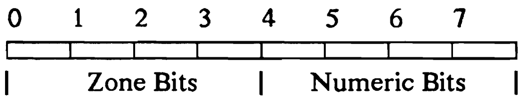
Data in main storage is in 8-bit bytes (plus ECC bytes). The instruction the system is doing determines how the data is used. A byte is used either as a character (decimal, alphabetic, or special) or as binary numbers (logical data).

The system uses EBCDIC (extended binary coded decimal interchange code) for storing and processing characters in main storage.

Alphanumeric Character Format

In character format, each byte of data is divided into two groups of 4 bits. Bits 0 through 3 make up the zone part, and bits 4 through 7 make up the numeric part. The character format represents a decimal digit, a special control character, or one of the characters that can be printed or displayed by the system (these characters are *graphics*). The following chart shows the byte interpreted for character format.

Character Zone and Digit Bits



For decimal arithmetic operations, the zone bits of the rightmost byte in the field indicates the sign of the number. (The system ignores the zone bits in all the other bytes of the number during the decimal arithmetic operation.) A zone containing hex B or D (binary 1011 or 1101) specifies a negative number. Any other hexadecimal digit in the zone specifies a positive number.

Ideographic Character Format

The ideographic character set is too large for all possible characters to be represented by the bit combinations possible in 1 byte. Each ideographic character code is contained in 2 bytes. Ideographic language support allows the system, the display station, and the printer to recognize and process the 2-byte ideographic character codes and also 1-byte alphanumeric and Katakana character codes. Ideographic data is identified by a Shift-Out (SO) character (hex 0E) preceding the ideographic character string and a Shift-In (SI) character (hex 0F) following the string.

The 2-byte format used for ideographic characters allows over 64,000 possible bit combinations for character codes. The valid character codes for the Ideographic feature are assigned in groups within this range. The first (high-order) byte of the 2-byte character code specifies the character group **(ward)** of a particular character. The second (low-order) byte specifies the displacement **(location)** within a ward.

Each language the System/36 supports has its own basic ideographic character set. Multiple ideographic character set languages are not concurrently supported on a system. Each basic ideographic character set comes with a header containing the language of the country and the valid character codes for the given language.

The character code assignments for the Japanese basic ideographic character set are:

Ward	Character Codes
00-3F	Invalid codes (except hex 0000 and hex 1C1C).
40	Only 4040 (space) is valid.
41 (see note)	Extended international character codes.
42 (see note)	Alphanumeric character codes.
43 (see note)	Katakana and lowercase alphanumeric codes.
44 (see note)	Hiragana character codes.
45-55 (see note)	Basic ideographic codes (hex 4541-hex 55FA).
56-68 (see note)	Extended (alternate) ideographic codes (hex 5641-hex 687F).
69-7F (see note)	User-defined optional character codes.
80-EF	Invalid codes.
F0-FF	Invalid codes except: • Hex F040 through F0FF, hex F140 through hex F1FF, and hex F240 through hex F2BF (extended character generator) • Hex F040 through hex F0FF and hex F140 through hex F17F for the character generator used in the 5224 or 5225 Printer • Hex F040 through hex F0BF for the extended character generator used with the 5553 and 5557 Printers

Figure 1-3. Japanese Ideographic Character Codes

Note: Within these wards, only charactεrs with location values of hex 41 through hex FE are valid except as otherwise noted.

The character code assignments for the Korean basic ideographic character set are:

Ward	Character Codes
00-3F	Invalid codes (except hex 0000 and hex 1C1C).
40	Only 4040 (space) is valid.
41	Special symbol codes.
42 (see note)	Alphameric character codes.
43-45	Invalid codes.
46 (see note)	Extended international character codes.
47-4F	Invalid codes.
50-67	Korean Hanja character codes.
68-83	Invalid codes.
84-D3	Korean Hangeul character codes.
D4-DD	User-defined optional character codes.
DE-FE	Invalid codes.
FF	Header containing the language of the country and the valid character codes for the given language.

Figure 1-3.1. Korean Ideographic Character Codes

Note: Within these wards, only the characters with location values of hex 41 through hex FE are valid except where otherwise noted.

The character code assignments for the Traditional Chinese (Taiwan and Hong Kong) basic ideographic character set are:

Ward	**Character Codes**
00-3F	Invalid codes (except hex 0000 and hex 1C1C).
40	Only 4040 (space) is valid.
41 (see note)	Extended international character codes.
42 (see note)	Alphameric character codes.
43-44	Invalid codes.
45-46	IBM Taiwan unique symbol codes.
47-4B	Invalid codes.
4C-68	Chinese character codes, first set.
69-91	Chinese character codes, second set.
92-CF	Invalid codes.
D0-DD	User-defined optional character codes.
DE-FE	Invalid codes.
FF	Header containing the language of the country and the valid character codes for the given language.

Figure 1-3.2. Traditional Chinese Ideographic Character Codes

Note: Within these wards, only the characters with location values of hex 41 through hex FE are valid except where otherwise noted.

The character code assignments for the Simplified Chinese (People's Republic of China) basic ideographic character set are:

Ward	Character Codes
00-3F	Invalid codes (except hex 0000 and hex 1C1C).
40	Only 4040 (space) is valid.
41 (see note)	Extended international character codes.
42 (see note)	Alphameric character codes.
43-44	Invalid codes.
45-46	Chinese unique symbol codes.
47-489F	Invalid codes.
48A0-5C9F	Chinese character codes, first set.
5CA0-6F	Chinese character codes, second set.
70-75	Invalid codes.
76-7F	User-defined optional character codes.
80-FE	Invalid codes.
FF	Header containing the language of the country and the valid character codes for the given language.

Figure 1-3.3. Simplified Chinese Ideographic Character Codes

Note: Within these wards, only the characters with location values of hex 41 through hex FE are valid except where otherwise noted.

Figure 1-3.4 shows the numbers of characters in each character set.

Language Supported	Basic Characters	IBM Extended Characters	User Defined Characters
Japanese	3710	3487	4270
Korean	3487	3990	1900
Traditional Chinese (Taiwan & Hong Kong)	3904	9932	2660
Simplified Chinese (People's Republic of China)	7475	0	1900

Figure 1-3.4. IBM Ideographic Languages Support

Display Fields

The Ideographic feature provides three new types of fields that may be defined in a display screen format. They are:

- **Ideographic-only:** This field type accepts only ideographic characters.
- **Either:** This type may be set by the system or the operator to accept either ideographic or alphanumeric-Katakana (A/N/K) characters.
- **Open:** This field type may be changed by the operator during entry to accept either ideographic or alphanumeric-Katakana (A/N/K) characters.

Binary Format (Logical Data)

In binary format, bits in a byte define binary digits, and the complete byte is an unsigned binary number. Bits are said to be on if set to 1, and off if set to 0. The following chart shows decimal 7 as a binary number. Notice that the parity bit is set to 0 (see "Parity" later in this chapter).

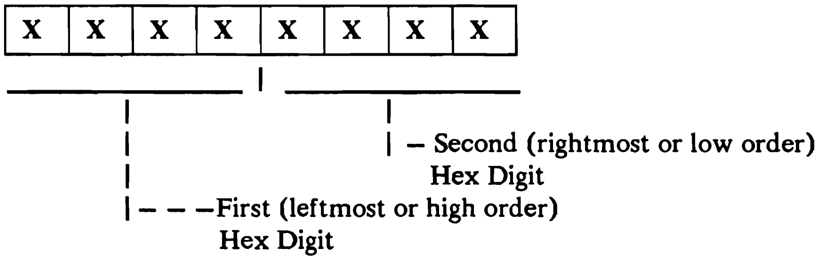
Unsigned Binary Number

P	0	1	2	3	4	5	6	7
0	0	0	0	0	0	1	1	1

Hexadecimal Digits

Each byte can be divided into two groups of 4 bits, and each of these groups can be represented as a single hexadecimal digit:

Bits to Hexadecimal Digits


X X X X X X X X
– Second (rightmost or low order) Hex Digit
– – –First (leftmost or high order) Hex Digit

The hexadecimal value of each arrangement of bits is shown in Figure 1-4:

Bits	Hex Digit		Bits	Hex Digit
0000	0		1000	8
0001	1		1001	9
0010	2		1010	A
0011	3		1011	B
0100	4		1100	C
0101	5		1101	D
0110	6		1110	E
0111	7		1111	F

Figure 1-4. Single Hexadecimal Digits

Throughout this manual, values stored in bytes are often shown in hexadecimal.

Parity

Associated with each byte is a parity bit that is generated by the system (and checked by the system during various operations). The parity bit ensures that the number of bits set to 1 in each byte is an odd number. If the represented data causes the byte to have an even number of 1-bits, the system sets the parity bit to 1 to make the byte contain an odd number of 1-bits. If the represented data has an odd number of 1-bits, the system sets the parity bit to 0 to maintain an odd number of 1-bits in the byte. When the bytes are stored in main storage the parity bit is replaced with the ECC code. When the bytes are taken out of main storage the ECC code is used to correct single bit errors and then replaced with the parity bit to provide checking throughout the system.

Addressing

Main storage is addressed in binary, using hexadecimal notation. The instructions can refer to a main storage location. The main storage locations are consecutively numbered from hex 000000 to the upper limit of storage. The location of any field or group of bytes is usually specified by the address of the rightmost (low-order or highest-numbered address) byte in the field. The exception is the insert and test character instruction, and most control blocks which specify the leftmost byte. The addressing arrangement lets the supervisor (in privileged mode) address 7302K bytes of real storage with a 3-byte address. The prefix address contained translation (PACT) registers provide a source for addressing all possible bytes of main storage. The addressing is available to the supervisor through the privileged Q code set which is part of the load, store, and load address instructions. The instruction gets a 2-byte immediate address from the instruction and forms a 3-byte address from the PACT register that is addressed by the op-code and the 2-byte address contained in, or referenced by, the instruction.

A main storage address can be specified by either of two methods: direct addressing or base displacement addressing. The type of addressing to be used is specified by bits 0 through 3 of the first byte (the operation code) of the instruction. These 4 bits are looked at as pairs: bits 0 and 1 and bits 2 and 3. Bits 0 and 1 control addressing for operand 1. Bits 2 and 3 control addressing for operand 2. When bits 0 and 1 equal binary 11, operand 1 is not used; when bits 2 and 3 equal binary 11, operand 2 is not used. Figure 1-5 describes operation code functions in addressing main storage.

```
Operation Code
 0   1   2   3   4   5   6   7
+---+---+---+---+---+---+---+---+
| X | X | X | X | X | X | X | X |
+---+---+---+---+---+---+---+---+

 _______         ________________
   |   _______   |
   |      |      |--Defines type of operation to be performed.
   |      |
   |      |      | How the main storage address of operand 2 is
   |      |      | specified by the instructions:
   |      |      |
   |      |      |    00 =   Operand 2 of the instruction contains
   |      |      |           a 2-byte address (direct addressing).
   |      |      |    01 =   Contents of XR1 (index register 1) is
   |      |      |           added to the single byte in the
   |      |      |           operand 2 section of the instruction.
   |      |      |           The result specifies the
   |      |------|           storage location being addressed (base
   |             |           displacement addressing).
   |             |    10 =   Contents of XR2 (index register 2) is
   |             |           added to the single byte in the operand
   |             |           2 section of the instruction.  The
   |             |           result specifies the storage address
   |             |           being addressed (base displacement
   |             |           addressing).
   |             |    11 =   Operand 2 is not used in this
   |                         instruction.
   |
   |             | How the main storage address of operand 1
   |             | is specified by the instructions:
   |             |
   |             |    00 =   Operand 1 of the instruction contains
   |             |           a 2-byte storage (direct  addressing).
   |             |    01 =   Contents of XR1 is added to the single
   |             |           byte in the operand 1 section of the
   |             |           instruction.  The result specifies the
   |-------------|           storage location being addressed (base
                 |           displacement addressing).
                 |    10  =  Contents of XR2 is added to the single
                 |           byte in the operand 1 section of the
                 |           instruction.  The result specifies the
                 |           storage location being addressed
                 |           (base displacement addressing).
                 |    11  =  Operand 1 is not used in this
                 |           instruction.
```

Note: *When bits 0, 1, 2, and 3 = 1111 (hex F), the instruction is a command instruction and does not address main storage.*

Figure 1-5. Operation Code Function in Addressing Main Storage

Direct Addressing

When either or both bit pairs in the operation code are 00, the matching operand uses direct addressing.

When direct addressing is used, the storage address is taken directly from the instruction and the direct addressing prefix address register (PDIR). The address in the instruction is 2 bytes long (see Figure 1-6).

Op Code Binary	Q-Byte in Hex	Direct Address in Hex
0000xxxx	xx	xxxx
00xxxxxx	xx	xxxx
xx00xxxx	xx	xxxx

Figure 1-6. Direct Addressing

Base Displacement Addressing

When either or both bit pairs of the operation code have one bit equal to 1 and the other bit equal to 0, the specified operand uses base displacement addressing.

In base displacement addressing, the 1-byte displacement contained in the instruction is added to a 2-byte address contained in an index register. Depending on which bit is 1 in the operation code, bit pair determines the index register to be used (see Figure 1-5). Both bit pairs can use the same index register when doing an instruction.

The 1-byte displacement allows a value large enough to allow a base displacement of 255 storage positions without changing the base value in the register.

Op Code Binary	Q-Byte in Hex	Operand Displacement in Hex
xx01xxxx	xx	xx
xx10xxxx	xx	xx
01xxxxxx	xx	xx
10xxxxxx	xx	xx

Figure 1-7. Base Displacement Addressing

Instruction Formats

Instruction formats are recognized by the way they address storage. The length of each instruction is determined by the type of addressing being performed.

All instruction formats have two parts in common: the op code and the Q-byte. Each of these parts is one byte long. The op code determines the type of addressing (therefore the format of the instruction), and the operation to be performed. The function of the Q-byte is determined by the instruction and is described with each instruction. For example, the Q-byte may specify the length of the data to be read.

Command Instructions

Command instructions are always 3 bytes long, and bits 0 through 3 of the operation code are always 1111. In a command instruction, the Q-byte contains one of the following function specifications:

- Mask
- Branch condition
- Immediate data byte

The control byte contains additional information to perform the command, or contains an address displacement (see Figure 1-8).

Op Code Binary	Q-Byte in Hex	Control in Hex
1111xxxx	xx	xx

Figure 1-8. Command Instruction

One-Address Instructions

One-address instructions can be either 3 or 4 bytes long. These instructions have either bit pair (bit 0 and 1 or bits 2 and 3) of the op code being both 1's. The other bit pair can be 01, 10, or 00. If these bits are 00, the operand is addressed directly and the instruction is 4 bytes long. If the bits are 01 or 10, the operand is addressed with base-displacement; the instruction is 3 bytes long; and index register 1 (01) or index register 2 (10), is used. The Q-byte of a one-address instruction can contain:

- An operand
- A mask
- A branch condition
- A data selection

- A register number

Op Code in Binary	Q-Byte in Hex	Operand Displacement in Hex
1110xxxx	xx	xx
1101xxxx	xx	xx
1011xxxx	xx	xx
0111xxxx	xx	xx

Figure 1-9. One-Address Instruction—Base-Displacement Addressing

Op Code in Binary	Q-Byte in Hex	Operand High-Order Bytes of Address in Hex	Operand Low-Order Bytes of Address in Hex
0011xxxx	xx	xx	xx
1100xxxx	xx	xx	xx

Figure 1-10. One-Address Instruction—Direct Addressing

Two-Address Instructions

Two-address instructions can be 4, 5, or 6 bytes long. This instruction type is distinct because *neither* bits 0 and 1 *nor* bits 2 and 3 of the op code are a pair of 1's. If all 4 bits are 0's, both operands are addressed direct, and the instruction is 6 bytes long. If only *one* of the bits 0 through 3 is 1, one of the addresses is direct; the other address is base displacement. The instruction is then 5 bytes long. If 1 bit from each of the bit pairs is 1, all addressing is base displacement and the instruction is 4 bytes long.

The index register used in base displacement addressing is determined by which bit in the bit pairs is 1. If the bits equal 01, index register 1 is used; if the bits equal 10, index register 2 is used. Both operands of an instruction can use the same index register.

Op Code in Binary	Q-Byte in Hex	Operand 1 Displacement Address in Hex	Operand 2 Displacement Address in Hex
0101xxxx	xx	xx	xx
0110xxxx	xx	xx	xx
1001xxxx	xx	xx	xx
1010xxxx	xx	xx	xx

Figure 1-11. Two-Address Instruction—Both Addresses Base Displacement

Op Code in Binary	Q-Byte in Hex	Operand 1 High-Order Bytes of Address in Hex	Operand 1 Low-Order Bytes of Address in Hex	Operand 2 Displacement Address in Hex
0001xxxx	xx	xx	xx	xx
0010xxxx	xx	xx	xx	xx

Figure 1-12. Two-Address Instruction—Operand 1 Direct Addressing

Op Code in Binary	Q-Byte in Hex	Operand 1 Displacement Address in Hex	Operand 2 High-Order Bytes of Address in Hex	Operand 2 Low-Order Bytes of Address in Hex
0100xxxx	xx	xx	xx	xx
1000xxxx	xx	xx	xx	xx

Figure 1-13. Two-Address Instruction—Operand 2 Direct Addressing

Op Code Binary	Q-Byte in Hex	Operand 1 High-Order Byte of Address in Hex	Operand 1 High-Order Bytes of Address in Hex	Operand 2 High-Order Bytes of Address in Hex	Operand 2 Low-Order Bytes of Address in Hex
0000xxxx	xx	xx	xx	xx	xx

Figure 1-14. Two-Address Instruction—Both Addresses Direct Addressing

Modes of System Operation

The system operates in three modes: cycle steal, interrupt, and process.

Cycle Steal Mode

Data may be moved by a cycle steal. When there is a request for data the control storage processor addresses storage and controls the movement of the data. The data is moved one or two bytes at a time when there are available openings in the processing of other data. The cycle steal operation has a higher priority than most other main storage processor operations.

Interrupt Mode

At the end of most input and output operations, the control processor is informed that the operation has ended and that the program should branch to a special interrupt handler routine. While the system is processing data in the interrupt routine, it is said to be operating in the *interrupt mode.*

Process Mode

The system is free to handle normal I/O control and data processing operations when it is not operating in either the cycle steal mode, or interrupt mode. Then the system operates in *process mode.*

Instruction Registers

Instruction Address Register (IAR)

The instruction address register, along with a prefix address contained translation (PACT) register, holds the address of the first byte of the next instruction in the stored program. This register is also used with the load, load address, add, subtract, and store instructions.

Address Recall Register (ARR)

Whenever the program branches, the system places the next following address (that is, the address of the instruction that follows the branch on condition instruction) in the address recall register. At the end of the branched to routine, the program can load the contents of the address recall register into the instruction address register or branch to a displacement off the ARR. This returns control to the point at which the branch occurred, if the ARR is not changed by the routine. Because the ARR is a 2-byte register the PIAR is not affected when the ARR is used to return control.

The address recall register is changed by zero and add zoned, load ARR, load address to ARR, add to ARR, subtract from ARR, decimal add and subtract, and insert and test characters instructions. (All machine instructions are described in Chapter 3 in this manual.)

Index Registers 1 and 2 (XR1 and XR2)

Index registers are general purpose registers. For example they hold base addresses for base displacement addressing.

Op Register

The op register is a main storage register and holds each control byte as it is taken from main storage. Control bytes are used for hardware functions and selections, setting of the program status register, selection of the index registers, and the processor clock controls.

Q Register

The Q register is a main storage register that holds the Q-byte and does one of the following:

- Holds a byte that specifies the length of the operands used. This length count is decreased as the instruction is performed.

- Is used with the op register to control operations and to select registers to be changed or stored.

- Holds the immediate data for use in the command.

- Holds the mask for the command.

A backup Q register (except for the 5360 Model D System Unit) in the local store stack is used to reload the real Q register when a complement operation is again needed.

Work Registers

The work registers are main storage registers WR4 through WR7. They are used as temporary storage areas for calculations and movement of data.

Program Status Register (PSR)

The program status register (PSR) is a main storage register that contains the main storage processor conditions. These conditions are tested by the branch-on-condition (BC), and jump-on-condition (JC) instructions. The contents of the program status register can be changed by:

- A system reset

- A load register (L) instruction that references the PSR

- Any of the following instructions: A, S, ZAZ, AZ, SZ, CLC, CLI, ALC, ALI, SLC, SLI, TBN, or TBF

- An instruction that changes or shifts bits

Program status register bits 0 and 1 are not assigned and are always 0. Bits 5, 6, and 7 (high, low, and equal) cannot be loaded at the same time. For the main storage processor load register instruction, if the PSR is loaded with bit 7, bits 5 and 6 are forced off. If the PSR is loaded with bits 6 and 7 off, bit 5 is on. If the PSR is loaded with the bit 6 on and bit 7 off, bit 5 is off.

When the PSR is loaded from the control storage processor by a write micro processor register (WMPR) instruction, bits 5 and 7 of the WMPR are used to load bits 5, 6, and 7 of the PSR. WMPR bit 7 on sets PSR bit 7 on and bits 5 and 6 off. WMPR bits 5 and 7 off sets the PSR bit 6 on. WMPR bit 5 on and bit 7 off sets the PSR bit 6 off.

Bit	**Contents**
0	Not used
1	Not used
2	Binary overflow
3	Test false
4	Decimal overflow
5	High
6	Low
7	Equal

Refer to the desired machine instruction for more information.

Prefix Address Contained Translation Registers (PACT)

The prefix address contained translation (PACT) registers provide real main storage addressing up to 7302K bytes. The registers also allow main storage addresses to shift between the various 64K-byte blocks of main storage by changing the values in the PACT registers. The control storage processor loads the values into the PACT registers PREG, PATR, and PCSP. For some machine instructions, the remaining PACT registers are loaded, by using the load or load address instruction, or from main storage during the fast task switching. The PACT registers are single byte registers, and 7 PACT registers are used in the hardware to address main storage. The PACT register does not change the address bits contained in the main storage address register. If the PACT register contains hex 80, the storage (addressed by the 2-byte register) to which the PACT register corresponds, is addressed through the address translate register to form a 20-bit main storage address. If the PACT register contains some value other than hex 80, that value is concatenated with the contents of the 2-byte registesr, to which the PACT register corresponds, to form a 20-bit main storage address.

System Address	PACT Registers	Used For
A0	PDIR	Operand addresses with direct addressing
A1	PXR1	Operand addresses indexed with XR1
A2	PXR2	Operand addresses indexed with XR2
A3	PIAR	Instruction fetch
A4	PREG	Fast task switch for MSP registers
A5	PATR	Fast task switch for ATRs
A6		Not used
A7[1]	PCSP	Main storage operations from the CSP

Bit 0 in the PDIR, PXR1, PXR2, and PIAR registers is really bit 0 in the program mode register. Bit 0 in the PCSP register is really bit 7 of the CMR.

Program Mode Register (PMR)

The program mode register (along with the prefix address contained translation register) controls main storage addressing and protection. Control storage instructions are used to load or sense the program mode register. The program mode register can also be loaded from the main storage processor using the load program mode register instruction. Bit assignments in the 8-bit program mode register are as follows:

Bit	Meaning When On
0	Dispatching disabled.
1	Reserved.
2	Reserved.
3[2]	Addresses calculated using XR1 are translated.
4[2]	Main storage processor instruction address register is translated.
5[2]	Addresses calculated using XR2 are translated.
6[2]	Direct addresses are translated.
7	Not privileged mode.

[1] On the 5360 Model D System Unit this register is in the control storage processor.

[2] These bits are really the same bits as bit 0 in the corresponding PACT registers.

Control Mode Register (CMR)

The control mode register and the PCSP register control main storage addressing and protection from the control storage processor. This register is located in the control storage processor for the 5360 Model D System Unit. Bit assignments in the 8-bit program register are:

Bit	Meaning When On
0-4	Reserved.
5-6	Used in combination to select the ATR bank when translated addressing is used (CMR bit 7 on).
7[1]	Addresses are translated.

[1] This bit is really the same bit as bit 0 in PCSP register.

Address Translation Registers (ATRs)

Address translation registers (ATRs) provide main storage addressing by page (2K address blocks). The address translation registers can only address main storage up to 7300K bytes, but a maximum storage size of 7302K bytes can be addressed. The 128 local storage registers named address translation registers (ATR) provide the addressing. Sixty-four of these are for program level (task) addressing; eight for the PACT register addressing; the other 56 are for input/output uses.

Each ATR stores 9 bits of data that is accessed as 2 bytes. Address translation register data contents of hex 0000 through hex 01FE provide address translation by addressing 511 2K-byte pages in main storage. A page is protected by loading its address translation register with hex FFFF, which is stored as 1FF. The storage protection mechanism is operable only when address translation is in effect. Any request to access a protected storage location by the control storage processor causes a storage exception. A machine check interrupt is generated. If the request to access a protected storage location is made by the main storage program, a level 5 interrupt to the control processor is generated.

Translate mode is controlled through the program mode register or control mode register contents. When in translate mode, the program mode register or the control mode register directs the main storage address register (MSAR), bits 0 through 4, to select one of 32 address translation registers. The resulting 20-bit real address is made by linking the contents of the 9 low-order bits of the selected address translation register with the 11 low-order bits (5 through 15) of the main storage address register.

Configuration Control Register (CCR)

The configuration control register (CCR) is used to change the configuration of main storage and select the main storage address compare condition by using programs. The CCR is loaded using the control store processor program. The CCR is an 8-bit register with bits 0 through 3 used for the main storage address compare condition that is in the main storage program. Bits 4 through 7 are used to determine the size of the main storage that was placed in the unit definition.

For the 5360 Model D System Unit, all 8-bits of the CCR are reserved. The memory configuration register (MCR) is used to determine the size of main storage.

CCR	
Bits 4-7	Storage
Hex	Size
4	2M
5	1M
6	768K
7	512K
8	384K
9	256K
B	128K

Memory Configuration Register (MCR)

Note: The memory configuration register (MCR) is only available with the 5360 Model D System Unit.

The MCR is divided into four 2-bit segments. Each segment is associated with one memory card slot, and describes the sizes of the memory card in that slot.

At power-on:

1. The MSP or CSP assumes a memory configuration of four reserved 2-bit segments.

2. The diagnostic code is run to determine true memory configuration.

3. The diagnostic code loads the memory configuration register (MCR) in the MSP or CSP to check for invalid addressing.

Card Slot 1	Card Slot 2	Card Slot 3	Card Slot 4
0 1	0 1	0 1	0 1
0 1	2 3	4 5	6 7

Slot Bits Decodes	Memory Card Size
0 0	No memory card
0 1	1 megabyte card
1 0	2 megabyte card
1 1	Reserved

Figure 1-15. MCR Bit Definitions

Slot number	5360 Model D board location
1	A-A1U2
2	A-A1T2
3	A-A1S2
4	A-A1R2

Figure 1-16. 5260 Model D System Unit Slot Definitions

Address Compare Register (ACR)

The address compare register (ACR) is loaded with a 19-bit (for the 5360 System Unit), a 20-bit (for the 5362 or 5364 System Units), or a 21-bit (for the 5360 Model D) main storage address by the control store processor program and the alter/display routine. The ACR provides a means of loading a main storage address so that a compare can be made to it by using the CCR or the main storage address stop bit in status byte 6.

Input Output Blocks (IOBs)

Each input/output function has specific parameters that the program must define before the operation is performed. The parameters are moved into input/output blocks, which are consecutive main storage positions into which parameters are placed in defined fields.

When an input/output operation is started, the program must present the address of the leftmost byte of the input/output block to the system (in index register 1).

When an input/output block is needed for a device refer to the *System Data Areas* manual for a description of the input/output bytes and bits.

General Input/Output Operations

All input/output operations are done by the input/output code for that operation. At initialization time, the control storage code for the input/output device is loaded and the attachment is enabled.

Chapter 2. System Control Panel and Unit Emergency Switch

5360 System Unit Control Panel and Unit Emergency Switch

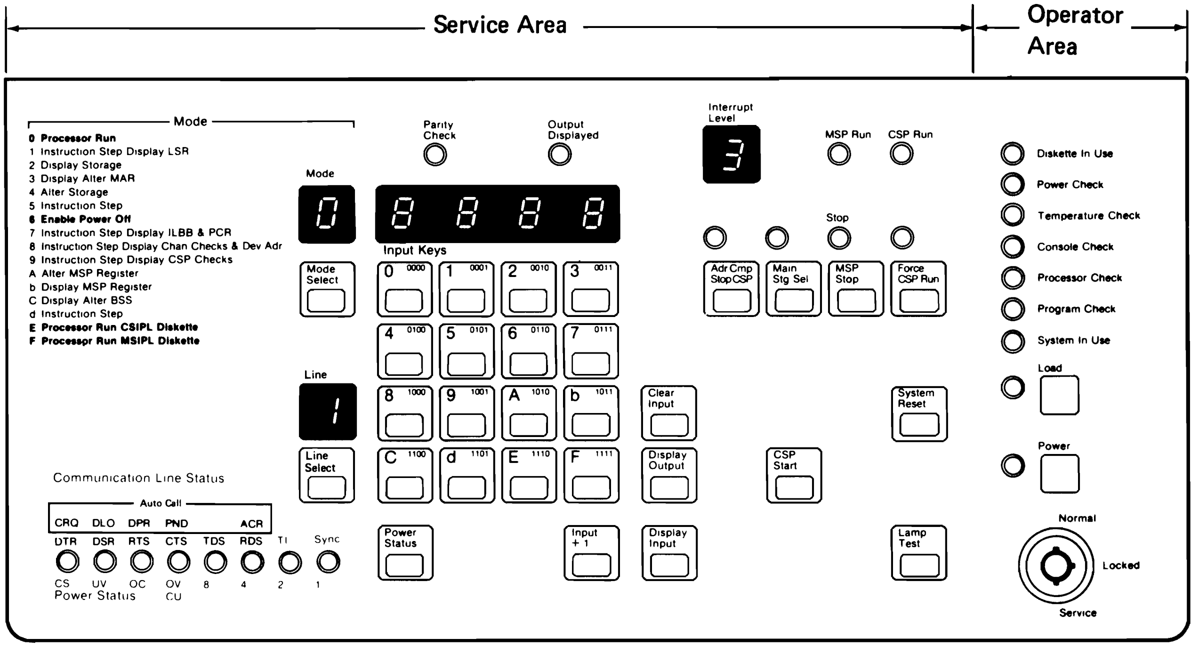


Figure 2-1. 5360 System Unit Control Panel

Operator Area of the 5360 System Unit Control Panel

Security Switch

Controls the power-on operation of the system and the mode of operation of the processor:

- Normal position: Permits you to power on the system and load the SSP programs from the disk.

- Locked position: Prevents power on.

- Service position: Permits you to power on the system and use the full function of the control panel. Only your service representative normally uses this mode.

Power Key

Turn the Security switch key to the Normal position. Press the Power key to power on the system. When the system powers on, a system reset occurs and the Power light goes on.

The normal way to power off the system (when the SSP is installed and running) is to enter the POWER OFF command at the system console. If a job is running, the system sends a message to the console, and you can complete the job and close the files without losing any information.

Another way to power off the system is to press the Mode Select key, enter mode 6 in the Mode display, then press the Power key. The system immediately powers off and, if a job is running, the information can be lost.

After powering off the system you can turn the Security switch key to the Locked position and remove the key. This prevents others from powering on the system.

When you power off the system the following occurs:

- On the 5360 System Unit, the Power Check light flashes (for a maximum of 15 seconds) and then goes off.

- The system saves or loses the contents of storage and registers, as determined by the way you power off or the option you select.

- The system saves any information stored in the power failure latches (the latest power failure information).

Power Light

The Power light (beside the Power key) goes on when you power on the system. The Power light goes off when you power off the system.

Load Key and Load Light

Press the Mode Select key, enter 0 in the Mode display, then press the Load key. This starts the control storage initial program load and the main storage initial program load sequences.

When you press the Load key, the Load light (beside the Load key) goes on. The Load light remains on until the first part of the control storage load routine loads correctly.

Diskette in Use Light

The Diskette in Use light goes on when system requests to use the diskette drive. This light goes off when the system removes the request to use the diskette drive.

Power Check Light

The Power Check light goes on if the voltage or current output of one of the system power supplies is wrong. When the Power Check light goes on, the system has powered off, but power status information is kept. If this light goes on, record the power status information (see the *System Problem Determination* manual).

Temperature Check Light

If one of the system temperature sensing devices senses an overheated condition, the system powers off, and the Temperature Check light goes on. This light remains on until the temperature inside the system unit falls to a normal level and the Power key is pressed to power on the system. If this problem occurs again, see the *System Problem Determination* manual.

Console Check Light

The Console Check light goes on if the system console or the work station controller fails. If the system console fails, you can assign another work station as the system console before processing continues (if you specified an alternate console when you prepared the system for use). If the work station controller fails, the cause of the failure must be found and corrected before processing can continue. See the *System Problem Determination* manual. The Console Check light goes off when the cause of the failure is corrected or when you assign the alternate console.

Processor Check Light

The Processor Check light goes on if the processing unit senses an error for which there is no correction procedure. If the Processor Check light goes on, see the *System Problem Determination* manual.

Program Check Light

The Program Check light goes on if the control storage program senses a program error for which there is no correction procedure. If the Program Check light goes on, see the *System Problem Determination* manual.

System in Use Light

The System in Use light goes on when one or more programs or commands are using main storage. The System In Use light does not go on when remote work stations are running but not using main storage. When the System In Use light is on, you should not power off the system by entering mode 6 and pressing the Power key; you can lose information by doing this. If the SSP is installed and running, you can power off the system without losing information by entering the POWER OFF command.

5360 System Unit Emergency Switch

CAUTION
Use the Unit Emergency switch only for emergencies.

The Unit Emergency switch, on the left side of the system unit:

- Must remain set to the Power Enable position during normal system operation.

- Removes all system power (except the AC voltage to the control power supply) when set to the Power Off position.

Do not use the Unit Emergency switch instead of the normal power-off procedure described under Power key. When you power on the system, you must use the Power key to correctly prepare the system for use.

Service Area of the 5360 System Unit Control Panel

The service representative normally uses the area of the system control panel under the cover on the left side. Also, the operator can load the system, power off the system, or display information by using the controls in this area. When an application program needs the operator to use the switches in this area, the program gives the operator instructions on how to use them.

This section describes the switches and lights in the service area of the system control panel.

CSP Start Key and CSP Run Light

In modes 2, 3, 4, A, and B this key is enabled only when the Security switch key is in the service position. After using other keys in this area to select an operation (with the CSP stopped), pressing the CSP Start key starts the CSP. The CSP does the next instruction and then, on the Input/Output display, shows the information that you selected.

If you selected one of the three processor run modes (0, E, or F), the normal CSP processing continues. If not, the CSP stops after completing the next instruction.

The CSP Run light remains on while the CSP is running.

MSP Run Light

The MSP (main storage processor) Run light is on while the main storage processor does instructions. The MSP Run light goes off when the main storage processor stops.

MSP Stop Key

The MSP Stop key can operate only while the Security switch key is in service position. After the MSP does each instruction, the control storage routine tests to determine if the MSP Stop key was pressed. If the MSP Stop key was pressed:

- The MSP stops.

- The CSP continues to run.

- The Alter/Display routine becomes active, and the options appear on the system console.

MSP Stop Light

Depending on the control storage processor size, the MSP Stop light goes on for one-half second and goes off or stays on, when you press the MSP Stop key (operates only when the Security key switch is in the Service position).

Input Keys

Use the 16 Input keys (0 through F) together with other keys on the control panel to enter, alter, or display data stored in main storage or local storage registers.

Mode Select Key and Mode Display

Using this key together with an Input key selects a mode and displays it in the Mode display. You can use modes E and F only while the Security key switch is in the service position.

During normal processing, you must set the Mode display to 0.

If the Mode display displays 0, the system loads from disk drive A.

If the Mode display displays E, the system loads from the diskette drive.

If the Mode display displays F, the system loads the control store program from disk drive A and the main store program from the diskette drive.

Your service representative uses modes E and F to load diagnostic programs.

Line Select Key and Line Display

Using the Line Select key with an Input key selects the communications line that you want to display in the Line display. When the Line display displays a communications line number, the eight Communication Line Status lights at the bottom of the control panel show the state of that line.

Power Status Key and Indicators

Pressing the Power Status key causes the eight lights that normally show the state of a communications line to change function and show the status of system power. The "Power Check Light Is On" section of the *System Problem Determination* manual describes this procedure.

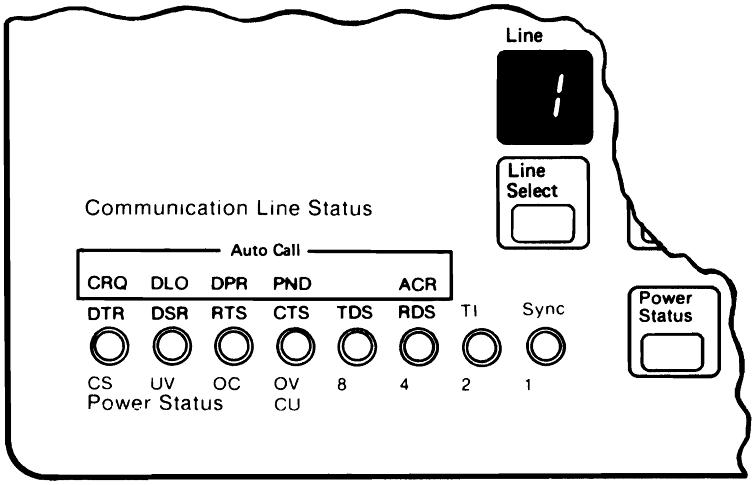


Figure 2-2. Communication Line Status and Power Status Indicators

Hexadecimal Display

The four-character Input/Output display (above the input keys) displays some system registers and information on the condition of the system. This display also shows a system reference code when the processor check light or the program check light goes on (in the operator area of the control panel). Your service representative uses the control panel keys to select the information for display.

Display Output Key and Output Displayed Light

Pressing the Display Output key causes the Input/Output display to show the data that you requested on the condition of the system. The Output Displayed light shows that you pressed the Display Output key or that the system is displaying data because of another action.

Display Input Key

When you press the Display Input key, the Input/Output display shows the contents of the input register.

Input +1 Key

Pressing the Input +1 key adds one to the input register each time it is pressed. The Input/Output display changes to input mode and displays the new input register with the one added. When you release the Input +1 key, the Input/Output display shows the information that you requested.

Clear Input Key

The Clear Input key sets the input register to all zeros and sets the Input/Output display to input mode.

Parity Check Light

If it is on, it shows that a parity error occurred on the data from the CSP to the Input/Output display. This light is off while the CSP Run light is on or when you select modes 4, 5, 6, A, or D.

Interrupt Level Display

The Interrupt Level display is a single-character hexadecimal display that shows which CSP interrupt level is active.

Adr Cmp Stop CSP Key and Light

You can stop the CSP on a control storage address by entering the address in the input register then pressing the Address Compare Stop CSP key. You can also use this key to stop the CSP on CSP access to main storage (when the Main Storage Select light is on) by setting the MSP configuration control record, address compare registers, and status byte 6, bit 0.

Pressing and releasing the Address Compare Stop CSP key causes the Address Compare Stop CSP light (above the key) to go on. Selecting mode 0, E, or F, and pressing the CSP Start key starts the address compare stop CSP function. This function causes the CSP to stop at the completion of the microinstruction in process when an address compare occurs. The address compare stop CSP can be done for a CSP access to control storage or main storage.

Pressing the Address Compare Stop CSP key again stops the function and causes the Address Compare Stop CSP light to go off.

Main Stg Sel Key and Light

Pressing the Main Stg Sel (Main Storage Select) key causes the Main Storage Select light to go on. Use this key with the Mode Select key and the Input keys to change or display the contents of an address in main storage. Use this key also with the Adr Cmp Stop CSP key to stop the CSP when a main storage address compare occurs.

You must place the compare address in the main storage address compare register.

Pressing the Main Stg Sel key again causes the Main Storage Select light to go off. This also returns the system to control storage select mode so that you can change or display control storage.

Force CSP Run Key and Light

Pressing the Force CSP Run key causes the Force CSP Run light (above the key) to go on and causes the CSP to disable machine check interrupts. This lets the CSP run while machine checks are present.

Pressing the Force CSP Run key again causes the Force CSP Run light to go off and returns the CSP to normal operation. Any machine checks cause the CSP to stop, and they must be reset to continue.

System Reset Key

When the CSP Run light is off and the Mode Select display is not set to 0, E, or F, pressing the System Reset key causes the System In Use light to go off and causes the system to do a system reset.

The System Reset key resets the system registers and latches so the system can start at a known state. The System Reset key does not reset the following control panel operations:

- Address Compare Stop CSP
- Main Storage Select
- Force CSP Run
- Input registers
- Mode Select
- Line Select
- Display mode

Lamp Test Key

When you press the Lamp Test key:

- If the system is powered on, all system lights and all parts of the hexadecimal displays go on.
- If system powered off:
  - The Power Check and Temperature Check lights go on.
  - The eight lights for Power Status and Communication Line Status go on.

5362 System Unit Control Panel and Unit Emergency Switch

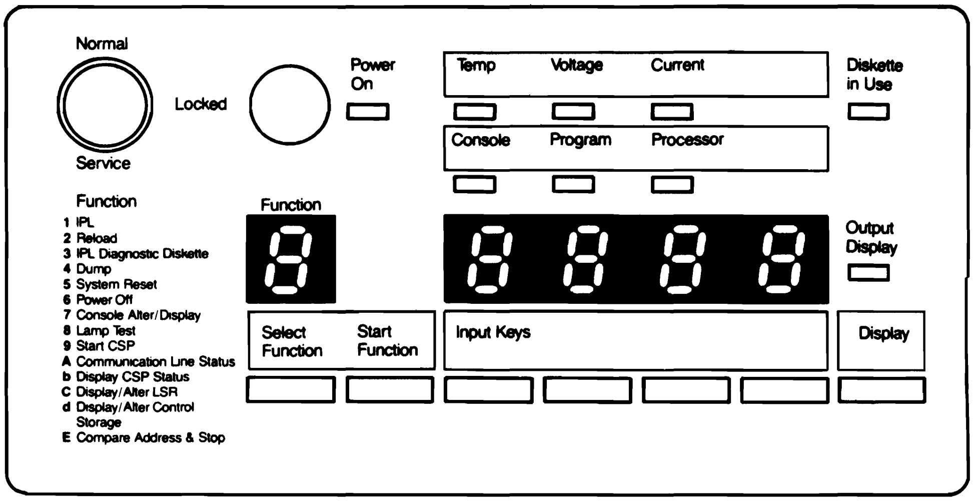


Figure 2-3. 5362 System Unit Control Panel

Operator Area of the 5362 System Unit Control Panel

Security Switch

Controls the power-on operation of the system and the mode of operation of the processor:

- **Normal position:** Permits you to power on the system; the system automatically does an IPL from the disk.

- **Locked position:** Prevents power-on.

- **Service position:** Permits you to power on the system and use the full function of the control panel. Only your service representative normally uses this mode.

Power On Key

Turn the Security switch key to the Normal position. Press the Power On key to power on the system. When the system powers on, a system reset occurs and the Power On light goes on.

The normal way to power off the system (when the SSP is installed and running) is to enter the POWER OFF command at the system console. If a job is running, the system sends a message to the console, and you can complete the job and close the files without losing any information.

Another way to power off the system is to place the Keylock switch in the service position, press the Select Function key until function 6 is in the Function display, then press the Start Function key. The system powers off in 20 seconds and if a job is running, the information can be lost.

After powering off the system you can turn the Security switch key to the Locked position and remove the key. This prevents others from powering on the system.

When you power off the system the following occurs:

- The Power On light flashes (for a maximum of 20 seconds) and then goes off.

- The system can save or lose the contents of storage and registers, depending on the way you power off the system.

- The system saves any information stored in the power failure latches (the latest power failure information).

Power On Light

The Power On light (beside the Power On key) goes on when you power on the system. The Power On light goes off when you power off the system.

Diskette in Use Light

The Diskette in Use light goes on when system requests to use the diskette drive. This light goes off when the system removes the request to use the diskette drive.

Temperature Light

If one of the system temperature sensing devices senses an overheated condition, the system powers off, and the Temperature Check light goes on. This light remains on until the temperature inside the system unit falls to a normal level and the Power key is pressed to power on the system. If this problem occurs again, see the *System Problem Determination* manual.

Voltage Light

The Voltage light goes on if the voltage output of one of the system power supplies is wrong. When the Voltage light goes on, the system has powered off. (See the *System Problem Determination* manual.)

Current Light

The Current light goes on if the current output of one of the system power supplies is wrong. When the Current light goes on, the system has powered off. (See the *System Problem Determination* manual.)

Console Light

The Console light goes on if the system console or the work station controller fails. If the system console fails, you can assign another work station as the system console before processing continues (if you specified an alternate console when you prepared the system for use). If the work station controller fails, the cause of the failure must be found and corrected before processing can continue. See the *System Problem Determination* manual. The Console light goes off when the cause of the failure is corrected or when you assign the alternate console.

Program Light

The Program light goes on if the control storage program senses a program error for which there is no correction procedure. If the Program light goes on, see the *System Problem Determination* manual.

Processor Light

The Processor light goes on if the processing unit senses an error for which there is no correction procedure. If the Processor light goes on, see the *System Problem Determination* manual.

5362 System Unit Emergency Switch

CAUTION
Use the Unit Emergency switch only for emergencies.

The Unit Emergency switch, on the front of the system unit:

- Must remain set to the Power Enable position during normal system operation

- Removes all system power when set to the Power Off position

Do not use the Unit Emergency switch instead of the normal power-off procedure described under Power On key.

Service Area of the 5362 System Unit Control Panel

The service representative normally uses the bottom area of the system control panel. Also, the operator can load the system, power off the system, or display information by using the controls in this area. When an application program needs the operator to use the switches in this area, the program gives the operator instructions on how to use them.

This section describes the switches and lights in the service area of the system control panel.

Input Keys

Use the four Input keys, (together with other keys on the control panel) to enter, alter, or display data stored in control storage or local storage registers.

Select Function Key and Function Display

Using this key selects a function and displays it in the Function display.

When the Security key switch is in the Normal position, you can only use function 1. When the Security key switch is in the Service position, you can use any function. Your service representative uses function 3 to load diagnostic programs.

The function codes and their operations are:

Function	Operation
1	*IPL:* The system loads from disk drive A.
2	*Reload:* The system loads the control store program from disk drive A and the main store program from the diskette drive.
3	*IPL Diagnostic Diskette:* The system loads from the diskette drive.
4	*Dump:* Causes the system to dump main storage and control storage.
5	*System Reset:* Pressing the Start Function key causes the system to do a system reset. The system reset resets the system registers and latches so the system can start at a known state.
6	*Power Off:* Press the Start Function key. The system immediately powers off and, if a job is running, the information can be lost.
7	*Console Alter/Display:* Pressing the Start Function key gives you the Alter/Display menu.
8	*Lamp Test:* Pressing the Start Function key causes all the system lights and all parts of the hexadecimal displays to go on.
9	*Start CSP:* Press the Start Function key to start the CSP.
A	*Communication Line Status:* Enter a communications line to be selected (with the Input Keys) and press the Start Function key. The status of the communication line is displayed in the Output Display. *Note: A template is used to decode the output display to determine the status of the communications lines.*
B	*Display CSP Status:* The status of the control storage processor is displayed in the Output Display.
C	*Display/Alter LSR:* After using the Input keys to select an LSR (with the CSP stopped), pressing the Start Function key starts the CSP. The CSP shows (on the Output display) the information that you requested. The information can then be altered.

D *Display/Alter Control Storage:* After using the Input keys to select a control storage address (with the CSP stopped), pressing the Start Function key starts the CSP. The CSP shows (on the Output display) the information in the address you selected. The information can then be altered.

E *Compare Address & Stop:* You can stop the CSP on the control storage address by entering the address in the Output display then pressing the Start Function key.

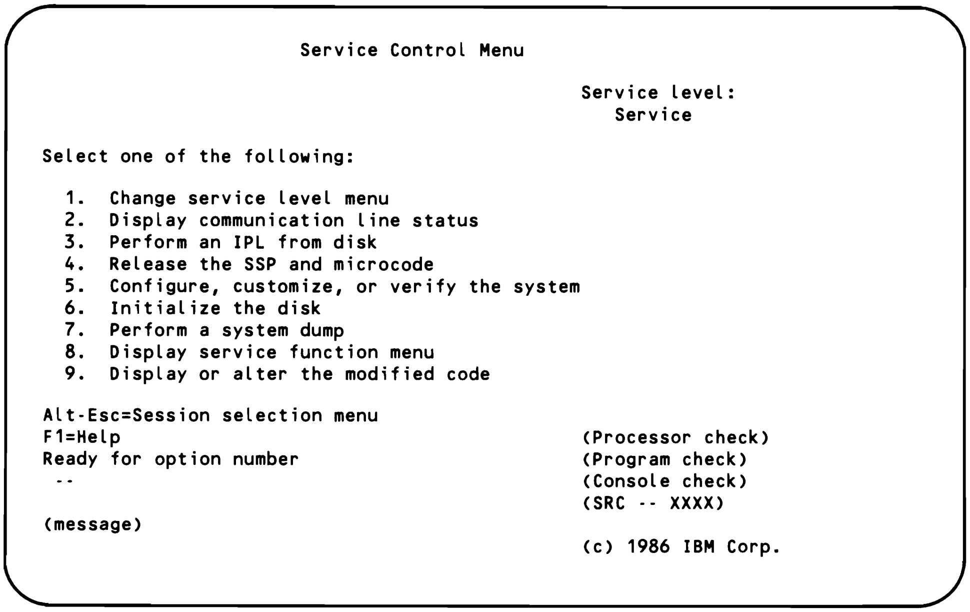
Output Display (Hexadecimal)

The four-character display (above the input keys) displays some system registers and information on the condition of the system. This display also shows a system reference code when the processor check light or the program check light goes on (in the operator area of the control panel). Your service representative uses the control panel keys to select the information for display.

Output Display Key and Output Display Light

Pressing the Output Display key causes the Output display to show the data that you requested on the condition of the system. The Output Display light shows that you pressed the Output Display key or that the system is displaying output data because of another action.

5364 System Unit Service Menu



```
                         Service Control Menu

                                                Service level:
                                                   Service

 Select one of the following:

   1.  Change service level menu
   2.  Display communication line status
   3.  Perform an IPL from disk
   4.  Release the SSP and microcode
   5.  Configure, customize, or verify the system
   6.  Initialize the disk
   7.  Perform a system dump
   8.  Display service function menu
   9.  Display or alter the modified code

 Alt-Esc=Session selection menu
 F1=Help                                        (Processor check)
 Ready for option number                        (Program check)
  --                                            (Console check)
                                                (SRC -- XXXX)
 (message)
                                                (c) 1986 IBM Corp.
```

Figure 2-4. 5364 Service Control Menu

Operator Area of the 5364 System Unit

The 5364 System Unit uses the IBM Personal Computer screen as the system console and operator panel. All system setup and commands are entered through the PC rather than by setting switches, and the status conditions from the host are displayed on the PC display rather than by using lights or indicators.

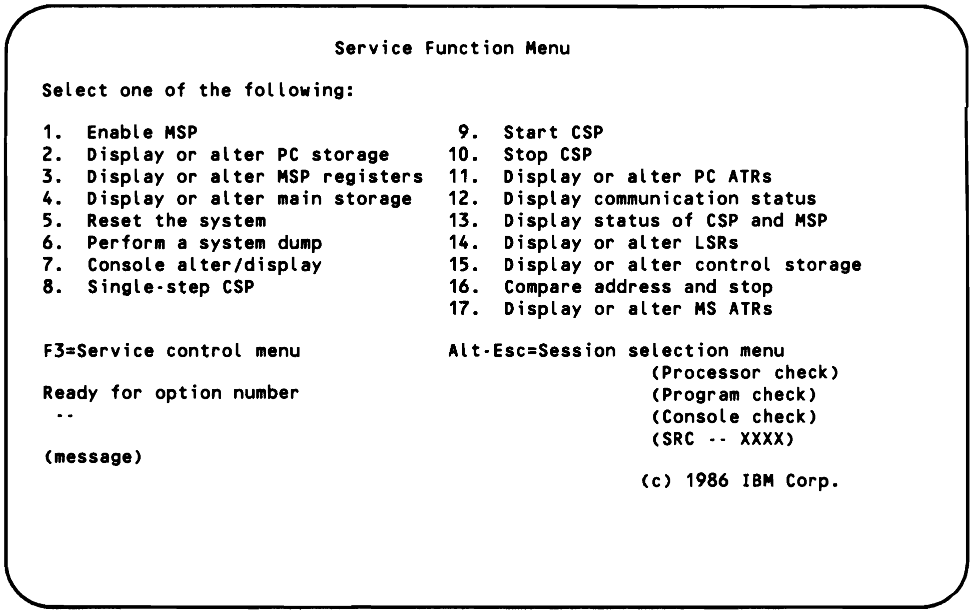
5364 System Unit Power Switch

To use 5364 System Unit, set the Power switch to the | (On) position. The Power switch is on the right side of the unit, at the rear. All system power is removed when this switch is set to Off.

5364 Service Control Menu Screen

Select option 3 (Service Session display) from the 5364 Session Selection menu to display the Service Control Menu screen. The Service Control Menu screen is shown in Figure 2-4.

Select option 8 from the Service Control Menu screen to display the Service Function Menu screen.



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                         Service Function Menu

Select one of the following:

1.  Enable MSP                          9.  Start CSP
2.  Display or alter PC storage        10.  Stop CSP
3.  Display or alter MSP registers     11.  Display or alter PC ATRs
4.  Display or alter main storage      12.  Display communication status
5.  Reset the system                   13.  Display status of CSP and MSP
6.  Perform a system dump              14.  Display or alter LSRs
7.  Console alter/display              15.  Display or alter control storage
8.  Single-step CSP                    16.  Compare address and stop
                                       17.  Display or alter MS ATRs

F3=Service control menu                Alt-Esc=Session selection menu
                                                (Processor check)
Ready for option number                         (Program check)
 --                                             (Console check)
                                                (SRC -- XXXX)
(message)
                                               (c) 1986 IBM Corp.
```

Figure 2-5. 5364 Service Function Menu

5364 Service Function Menu Screen

For detailed information, refer to *Program Problem Diagnosis and Diagnostic Aids,* SY21-0593.

Selection codes for the service functions are:

Option	Operation
1	*Enable MSP:* Enables the Main Storage Processor.
2	*Display or alter PC storage:* Allows you to display or alter contents of selected locations in PC storage.
3	*Display or alter MSP registers:* Displays a set of MSP registers. If a register is desired that is not already shown, there is a procedure for displaying or altering MSP registers. Otherwise, registers that are shown are altered directly on the screen.
4	*Display or alter main storage:* Allows you to display or alter main storage.
5	*Reset the system:* Allows you to reset the system.
6	*Perform a system dump:* Allows you to force a storage dump to disk.
7	*Console alter/display:* Allows you to stop the MSP while the CSP continues to run. The alter/display routine becomes active, and the options appear on the system console.
8	*Single-step CSP:* Allows you to single-step the Central Storage Processor.
9	*Start CSP:* Allows you to start the Central Storage Processor at a specified address.
10	*Stop CSP:* Allows you to stop the Central Storage Processor at a specified address.
11	*Display or alter PC ATRs:* Allows you to display or alter PC ATRs.
12	*Display communication status:* Allows you to display the communication status.
13	*Display status of CSP and MSP:* Allows you to display the status of the Central Storage Processor and the Main Storage Processor.
14	*Display or alter LSRs:* Allows you to display or alter contents of the CSP/SS local storage registers (LSRs).
15	*Display or alter control storage:* Allows you to display or alter contents of selected locations in control storage.
16	*Compare address and stop:* Allows you to stop the CSP/SS or a target control storage address.
17	*Display or alter MS ATRs:* Allows you to display or alter MS ATRs.

Chapter 3. Machine Instructions

Each system machine instruction is described here in detail. The instructions are in two groups:

- Main memory
- SVCs

The main memory machine instructions are arranged alphabetically by name, and the SVCs are arranged alphabetically by their R-byte hex code.

For a listing of the mnemonic for each op code, refer to Appendix A, "Instruction Formats," in this manual.

The following is a listing of the machine instructions and SVCs in alphabetic order according to their name:

"Action Control Element Build and Queue" on page 3-141
"Add Logical Characters (ALC)" on page 3-4
"Add Logical Immediate (ALI)" on page 3-7
"Add to Register (A)" on page 3-9
"Add Zoned Decimal (AZ)" on page 3-13
"Assign" on page 3-78
"Asynchronous Task Ready Check" on page 3-112
"Asynchronous Task Wait" on page 3-95
"ATASK" on page 3-126

"Branch On Condition (BC)" on page 3-16

"Compare Logical Characters (CLC)" on page 3-19
"Compare Logical Immediate (CLI)" on page 3-21
"Control Storage Transient Scheduler" on page 3-142

"Data Communications IOCH" on page 3-136
"Diskette Data Compression" on page 3-138
"Diskette IOS" on page 3-133
"DSC I/O" on page 3-140
"DTASK" on page 3-127
"DTWAL" on page 3-129
"Dump Task/Terminate Task" on page 3-109

"Edit (ED)" on page 3-23
"Event Post" on page 3-73
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"Fast Transfer" on page 3-84
"Fixed Disk IOS" on page 3-132
"Free Assigned Areas" on page 3-80
"Free Second Request Block" on page 3-77

"General Post" on page 3-70
"General Wait" on page 3-68
"Get Page" on page 3-93

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"Load Address (LA)" on page 3-31
"Load Program Mode Register (LPMR)" on page 3-34
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"Post Action Control Element" on page 3-97
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"Scan System Queue" on page 3-100
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"Set Bits Off Masked (SBF)" on page 3-43
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"Set Transient Area Not Busy" on page 3-97
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"SMFC" on page 3-132
"Specific Resource Dequeue" on page 3-103
"Store Register (ST)" on page 3-46
"Subtract from Register (S)" on page 3-48
"Subtract Logical Characters (SLC)" on page 3-51
"Subtract Logical Immediate (SLI)" on page 3-54
"Subtract Zoned Decimal (SZ)" on page 3-56
"Supervisor Call (SVC)" on page 3-67
"System Control Block Access" on page 3-88

Add Logical Characters (ALC)

	Op Code (Hex)	Q-Byte* (Hex)	Operand Addresses** (Hex)			
Operands	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
A1(L1),A2	0E	L1-1	Operand 1 address		Operand 2 address	
A1(L1),D2(,R1)	1E	L1-1	Operand 1 address		Op 2 disp from XR1	---
A1(L1),D2(,R2)	2E	L1-1	Operand 1 address		Op 2 disp from XR2	---
D1(L1,R1),A2	4E	L1-1	Op 1 disp from XR1	Operand 2 address		---
D1(L1,R1),D2(,R1)	5E	L1-1	Op 1 disp from XR1	Op 2 disp from XR1	---	
D1(L1,R1),D2(,R2)	6E	L1-1	Op 1 disp from XR1	Op 2 disp from XR2	---	
D1(L1,R2),A2	8E	L1-1	Op 1 disp from XR2	Operand 2 address		---
D1(L1,R2),D2(,R1)	9E	L1-1	Op 1 disp from XR2	Op 2 disp from XR1	---	
D1(L1,R2),D2(,R2)	AE	L1-1	Op 1 disp from XR2	Op 2 disp from XR2	---	

* The Q-byte designates the operand length:

L1-1 = the number of bytes in either operand, minus 1.

Maximum length of each operand is 256 bytes; both operand must be the same length.

** The operands may overlap. Address operands by their rightmost byte.

Operation

The Add Logical Characters (ALC) machine instruction adds the binary number in operand 2 to the binary number in operand 1 and stores the result in operand 1.

Program Note

The system resets the binary overflow bit during this operation if a carry does not occur from the high-order byte.

CAUTION
Overlapping the operands with the rightmost byte of the first operand to the left of the rightmost byte of the second operand destroys part of the second operand before it is used in the operation.

Resulting Program Status Byte Settings

Bit	Name	Condition Indicated
7	Equal	Zero results
6	Low	No carry occurred from the high-order byte and result not zero
5	High	Carry occurred from the high-order byte and result not zero
4	Decimal overflow	Bit not affected
3	Test false	Bit not affected
2	Binary overflow	Carry occurred from the high-order byte

Example

Instruction

5E	03	00	10

Operand 1 before Operation

		00110101	11001011	11101101	01100100
		0CBD	0CBE	0CBF	0CC0<-Storage Positions

Operand 2 before and after Operation

		01011011	01010101	01111000	11001101
		0CCD	0CCE	0CCF	0CD0<-Storage Positions

Operand 1 after Operation

		10010001	00100001	01100110	00110001
		0CBD	0CBE	0CBF	0CC0<-Storage Positions

Program Status Register before Operation

00000001

0 7 <-----Bits

Program Status Register after Operation

00000010

0 7 <-----Bits

Add Logical Immediate (ALI)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	Byte 1	Byte 2	Byte 3	Byte 4
A1,I	3F	I	Operand 1 address	
D1(,R1),I	7F	I	Op 1 disp from XR1	---
D1(,R2),I	BF	I	Op 1 disp from XR2	---

* I = 1 byte of immediate data (that is, 1 byte of actual data).

** Operand 1 is a 1-byte field; operand 2 is not used.

Operation

The Add Logical Immediate (ALI) machine instruction subtracts the binary number in the immediate data byte from the binary number in operand 1 and stores the result in operand 1. The 2's complement of the immediate data byte is put in the Q-byte. If the value in the Q-byte is numerically smaller than operand 1, the result occurs as if operand 1 has an additional high-order binary digit.

Program Notes

The Add Logical Immediate instruction is the Subtract Logical Immediate instruction with a 2's complement of the immediate data byte. The assembler must provide the 2's complement of the immediate data.

Resulting Program Status Byte Settings

Bit	Name	Condition Indicated
7	Equal	Operand 1 value before subtract is equal to the complement of the Q-byte value
6	Low	Operand 1 value before subtract is less than the complement of the Q-byte value
5	High	Operand 1 value before subtract is greater than the complement of the Q-byte value
4	Decimal overflow	Bit not affected
3	Test false	Bit not affected
2	Binary overflow	Bit not affected

Example

The assembler changes the add of the data to a subtract of the 2's complement of the immediate data such as hex 0B to hex F5 in the example.

Assembler instruction ALI X'0021',X'0B'

3F	F5	00	21

Operand 1 before Operation

00

0021 <-----Storage Positions

Operand 1 after Operation

0B

0021 <-----Storage Positions

Program Status Byte after Operation

00000010

0 7 <-----Bits

Add to Register (A)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
A1,RX	36	Rx	Operand 1 address	
D1(,R1),RX	76	Rx	Op 1 disp from XR1	---
D1(,R2),RX	B6	Rx	Op 1 disp from XR2	---

* Rx specifies the register whose contents are modified by the machine instruction.

** Operand 1 is a 2-byte field addressed by its rightmost byte; operand 2 is not used.

Operation

The Add to Register (A) machine instruction adds the binary number in operand 1 to the contents of the 2-byte register selected by the Q-byte and stores the result in the register. The Q-byte coding is:

Q-Byte

Hex	**Register Specified**
00	None, the system ignores (no-op) the instruction
01	XR1
02	XR2
03	XR1
04	Q, program status register
08	Address recall register
10	Instruction address register
20	Instruction address register
40	Instruction address register
41	XR1
42	XR2
43	Address recall register
44	WR4
45	WR5
46	WR6
47	WR7
A0[1]	PDIR
A1[1]	PXR1, XR1
A2[1]	PXR2, XR2
A3[1]	PIAR, IAR
All others	Reserved; do not use

[1] These Q-bytes make the instruction privileged so they can only be used by privileged programs. No carry is added to the PACT of the register that contains the total after the addition. If the PDIR is used the instruction is a no op, since only the high order byte of the PDIR is defined and the instruction only affects the low order two bytes.

Program Notes

- If the Q-code is hex 04 (program status register), the high order byte (of the two byte field addressed by the instruction) is placed in the length count recall register and the low byte is placed in the program status register. Adding to the program status register causes unpredictable results; a hex 04 is forced into the high byte before the addition is done.
- This machine instruction does not change the operand.

CAUTION
The results in the program status register are not reliable if it is the register selected.

Resulting Program Status Byte Settings

Bit	Name	Condition Indicated
7	Equal	Zero results
6	Low	No carry occurred from the leftmost byte and result not zero
5	High	Carry occurred from the leftmost byte and result not zero
4	Decimal overflow	Bit not affected
3	Test false	Bit not affected
2	Binary overflow	Carry occurred from the high order byte

Example

Instruction

36	00000010	00	04

Operand 1

01001000	00100000	
0003	0004	<-----Storage Positions

Index Register 2 before Operation

00110101	01101010

Index Register 2 after Operation

01111101	10001010

Program Status Byte after Operation

00000010

0 7 <-----Bits

Add Zoned Decimal (AZ)

	Op Code (Hex)	Q-Byte* (Hex)		Operand Addresses** (Hex)			
Operands	Byte 1	Byte 2		Byte 3	Byte 4	Byte 5	Byte 6
A1(L1),A2(L2)	06	L1-L2	L2-1	Operand 1 address		Operand 2 address	
A1(L1),D2(L2,R1)	16	L1-L2	L2-1	Operand 1 address		Op 2 disp from XR1	---
A1(L1),D2(L2,R2)	26	L1-L2	L2-1	Operand 1 address		Op 2 disp from XR2	---
D1(L1,R1),A2(L2)	46	L1-L2	L2-1	Op 1 disp from XR1	Operand 2 address		---
D1(L1,R1),D2(L2,R1)	56	L1-L2	L2-1	Op 1 disp from XR1	Op 2 disp from XR1	---	
D1(L1,R1),D2(L2,R2)	66	L1-L2	L2-1	Op 1 disp from XR1	Op 2 disp from XR2	---	
D1(L1,R2),A2(L2)	86	L1-L2	L2-1	Op 1 disp from XR2	Operand 2 address		---
D1(L1,R2),D2(L2,R1)	96	L1-L2	L2-1	Op 1 disp from XR2	Op 2 disp from XR1	---	
D1(L1,R2),D2(L2,R2)	A6	L1-L2	L2-1	Op 1 disp from XR2	Op 2 disp from XR2	---	

* The Q-byte designates the operand length:

L1-L2 (4 bits) = the number of bytes in operand 1, minus the number of bytes in operand 2.

L2-1 (4 bits) = the number of bytes in operand 2, minus 1.

Maximum length of operand 1 is 31 bytes; maximum length of operand 2 is is 16 bytes.

** The operands may overlap. Address operands by their rightmost byte.

Operation

The Add Zoned Decimal (AZ) machine instruction algebraically adds the second operand to the first operand and stores the result in the first operand.

The main storage processor sets the zone bits of all bytes except the rightmost byte in the first operand to hex F (binary 1111). It sets the zone bits of the rightmost byte in the first operand to (1) hex F (binary 1111) if the result of the operation is either positive or zero, or (2) hex D (binary 1101) if the result is negative.

Program Notes

- The second operand is not changed unless the fields overlap.
- The system does not check for allowed decimal digits in either operand.
- The decimal overflow condition indicator (program status bit 4) may be set on during this operation. Program status bit 4 can be reset by:
  - A system reset
  - Testing decimal overflow with a branch on condition or jump on condition instruction
  - Loading a 0 in bit 4 of the program status register using the load register instruction
- The system stores the rightmost address of operand 1 in the address recall register (ARR) and leaves the ARR modified with data that should not be used.

CAUTION

Overlapping the operands with the rightmost byte of the first operand to the left of the rightmost byte of the second operand destroys part of the second operand before it is used in the operation.

Resulting Program Status Byte Setting

Bit	Name	Condition Indicated
7	Equal	Zero results
6	Low	Negative results
5	High	Positive results
4	Decimal overflow	Carry occurred from the leftmost position of operand 1
3	Test false	Bit not affected
2	Binary overflow	Bit not affected

Example

Instruction

04	22	00	10	00	20

Operand 1 before Operation

	F7	F6	F3	F6	F9
	000C	000D	000E	000F	0010 <-----Storage Positions

Operand 2 before and after Operation

			F4	F2	F5
			001E	001F	0020 <-----Storage Positions

Operand 1 after Operation

	F0	F0	F4	F2	F5
	000C	000D	000E	000F	0010 <-----Storage Positions

Program Status Register before Operation

```
00000001
0       7 <-----Bits
```

Program Status Register after Operation

```
00000100
0       7 <-----Bits
```

Branch On Condition (BC)

	Op Code (Hex)	Q-Byte* (Binary)	Branch to Address** (Hex)	
Operands	Byte 1	Byte 2	Byte 3	Byte 4
A1,I	C0	xxxx xxxx	Direct address	
D1(,R1),I	D0	xxxx xxxx	Disp from XR1	---
D1(,R2),I	E0	xxxx xxxx	Disp from XR2	---
D1(,R8),I	F0	xxxx xxxx	Disp from ARR	---

* The Q-byte contains a binary mask specifying which program status register positions are tested by the instruction.

** If the ARR is used in the operand, the address being branched to is determined before the ARR is changed to the next sequential instruction.

Operation

The Branch On Condition (BC) machine instruction tests the program status register (rightmost byte) under control of the Q-byte. If the register meets the condition set up by the Q-byte, the system places the branch to address in the instruction address register, places the address of the next sequential machine instruction in the address recall register, and branches to the branch to address. If the register does not meet at least one condition set up by the Q-byte, the system places the address of the next sequential machine instruction in the instruction address register, and the program advances to the next sequential machine instruction.

The Q-byte determines what conditions are tested and if the branch is to occur on condition true (when the specified program status register bit is 1) or occur on condition false (when the specified program status register bit is 0). When bit 0 of the Q-byte is 1 (condition true), the branch occurs if any of the indicators tested is 1 (associated bit is 1). When bit 0 of the Q-byte is 0 (condition false), the branch occurs if all the indicators tested are 0 (associated bits are all zero).

Bits 2 through 7 of the Q-byte determine the bits to be tested in the program status register. These bits, and the conditions they represent, are:

Q-Byte

Bit	**Condition Tested**
7	Equal
6	Low
5	High
4	Decimal overflow
3	Test false
2	Binary overflow

Program Notes

- The branch to address is placed in the instruction address register before the next sequential instruction address is placed in the address recall register.
- A branch to a displacement off the ARR is in effect a return, provided the ARR has not been changed since the previous branch.
- The address placed in the address recall register remains there until a decimal add, decimal subtract, insert and test character, zero and add zoned, or another branch on condition machine instruction is executed. Load register, load address into register, add register, and subtract from register instructions change the address in the ARR if the ARR is the target register.
- Bits 5, 6, and 7 of the program status byte can never all be zero:
  - A Q-byte of hex 80, x7, or xF (where x is 0, 1, 2, 3, 4, 5, 6, or 7) causes the system to ignore the machine instruction (no operation occurs).
  - A Q-byte of hex 00, x7, xF (where x is 8, 9, A, B, C, D, E, or F) causes an unconditional branch.

Resulting Program Status Byte Setting

Bit	Name	Condition Indicated
7	Equal	Bit not affected
6	Low	Bit not affected
5	High	Bit not affected
4	Decimal overflow	Turned off if tested; otherwise, not affected
3	Test false	Turned off if tested; otherwise, not affected
2	Binary overflow	Bit not affected

Example

Instruction

C0	10001000	02	BF

0BCC 0BCD 0BCE 0BCF <-----Storage Positions

Program Status Byte before Operation

00011001

Instruction Address Register after Operation

02	BF

Address Recall Register after Operation

0B	D0

Program Status Byte after Operation

00010001

0 7 <-----Bits

Compare Logical Characters (CLC)

	Op Code (Hex)	Q-Byte* (Hex)	Operand Addresses** (Hex)			
Operands	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
A1(L1),A2	0D	L1-1	Operand 1 address		Operand 2 address	
A1(L1),D2(,R1)	1D	L1-1	Operand 1 address		Op 2 disp from XR1	---
A1(L1),D2(,R2)	2D	L1-1	Operand 1 address		Op 2 disp from XR2	---
D1(L1,R1),A2	4D	L1-1	Op 1 disp from XR1	Operand 2 address		---
D1(L1,R1),D2(,R1)	5D	L1-1	Op 1 disp from XR1	Op 2 disp from XR1	---	
D1(L1,R1),D2(,R2)	6D	L1-1	Op 1 disp from XR1	Op 2 disp from XR2	---	
D1(L1,R2),A2	8D	L1-1	Op 1 disp from XR2	Operand 2 address		---
D1(L1,R2),D2(,R1)	9D	L1-1	Op 1 disp from XR2	Op 2 disp from XR1	---	
D1(L1,R2),D2(,R2)	AD	L1-1	Op 1 disp from XR2	Op 2 disp from XR2	---	

* The Q-byte designates the operand length:

L1-1 = the number of bytes in either operand, minus 1.

Maximum length or each operand is 256 bytes; both operands must be the same length.

** The operands may overlap. Address operands by their rightmost byte.

Operation

The Compare Logical Characters (CLC) machine instruction compares operand 1 with operand 2, byte by byte, and sets the program status register depending on the result of the compare. The compare looks at each operand as a binary quantity; that is, matching bytes from the two operands are compared, bit for bit.

Program Note

Neither operand is changed by the machine instruction.

Resulting Program Status Byte Setting

Bit	Name	Condition Indicated
7	Equal	Operand values are equal
6	Low	Operand 1 value is smaller than operand 2 value
5	High	Operand 1 value is greater than operand 2 value
4	Decimal overflow	Bit not affected
3	Test false	Bit not affected
2	Binary overflow	Bit not affected

Example

Instruction

0D	02	00	12	00	02

Operand 1 before and after Operation

27	FA	26

0010 0011 0012 <-----Storage Positions

Operand 2 before and after Operation

23	FA	26

0000 0001 0002 <-----Storage Positions

Program Status Byte before Operation

00100001

0 7 <-----Bits

Program Status Byte after Operation

00100100

0 7 <-----Bits

Compare Logical Immediate (CLI)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	Byte 1	Byte 2	Byte 3	Byte 4
A1,I	3D	I	Operand 1 address	
D1(,R1),I	7D	I	Op 1 disp from XR1	---
D1(,R2),I	BD	I	Op 1 disp from XR2	---

* I = 1 byte of immediate data (that is, 1 byte of actual data that is to be used in binary form).

** Operand 1 is a 1-byte field; operand 2 is not used.

Operation

The Compare Logical Immediate (CLI) machine instruction compares all the bits in the Q-byte with all the bits in operand 1 and stores the result in the program status byte.

Program Note

Neither the Q-byte nor operand 1 is changed by this operation.

Resulting Program Status Byte Setting

Bit	Name	Condition Indicated
7	Equal	Operand 1 value is equal to Q-byte value
6	Low	Operand 1 value is less than Q-byte value
5	High	Operand 1 value is greater than Q-byte value
4	Decimal overflow	Bit not affected
3	Test false	Bit not affected
2	Binary overflow	Bit not affected

Example

Instruction

3D	7F	00	21

Operand 1 before and after Operation

75

0021 <-----Storage Positions

Program Status Byte after Operation

00000010

0 7 <-----Bits

Edit (ED)

	Op Code (Hex)	Q-Byte* (Hex)	Operand Addresses** (Hex)			
Operands	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
A1(L1),A2	0A	L1-1	Operand 1 address		Operand 2 address	
A1(L1),D2(,R1)	1A	L1-1	Operand 1 address		Op 2 disp from XR1	---
A1(L1),D2(,R2)	2A	L1-1	Operand 1 address		Op 2 disp from XR2	---
D1(L1,R1),A2	4A	L1-1	Op 1 disp from XR1	Operand 2 address		---
D1(L1,R1),D2(,R1)	5A	L1-1	Op 1 disp from XR1	Op 2 disp from XR1	---	
D1(L1,R1),D2(,R2)	6A	L1-1	Op 1 disp from XR1	Op 2 disp from XR2	---	
D1(L1,R2),A2	8A	L1-1	Op 1 disp from XR2	Operand 2 address		---
D1(L1,R2),D2(,R1)	9A	L1-1	Op 1 disp from XR2	Op 2 disp from XR1	---	
D1(L1,R2),D2(,R2)	AA	L1-1	Op 1 disp from XR2	Op 2 disp from XR2	---	

* The Q-byte designates the operand length:

L1-1 = the number of bytes in operand 1, minus 1.

Operand 2 must contain as many bytes as there are hex 20s in operand 1.

** The operands may overlap. Address operands by their rightmost byte.

Operation

The Edit (ED) machine instruction replaces bytes containing hex 20 in operand 1 with characters from operand 2. Starting at the rightmost position in both operands, the processing unit inspects operand 1 for hex 20s. When the system finds the first hex 20, it moves the rightmost byte from operand 2 into that hex 20 location, then inspects the next bytes in operand 1 for the next sequential hex 20. Locating the next hex 20, the system moves the next byte from operand 2 into that operand 1 position. The operation continues until all the bytes in operand 1 have been examined for hex 20. During the operation, the system sets the zone bits of all replaced operand 1 bytes to hex F (binary 1111).

Program Note

Operand 2 is not changed during this instruction.

CAUTION
Overlapping the operands with the rightmost byte of the first operand to the left of the rightmost byte of the second operand might destroy part of the second operand before it is used in the operation.

Resulting Program Status Byte Settings

Bit	Name	Condition Indicated
7	Equal	Operand 2 zero
6	Low	Operand 2 negative
5	High	Operand 2 positive
4	Decimal overflow	Bit not affected
3	Test false	Bit not affected
2	Binary overflow	Bit not affected

Note: The program status register setting is shown only if one of the following conditions is true:

- *The program status byte bit 7 is set before EDIT is executed.*
- *The rightmost byte of operand 1 is a hex 20.*
- *Operand 2 is not zero.*

The recommended way to get a correct program status register value is to set the program status register bit 7 on. To do this issue a compare logical character command and use equal operands.

Example

Instruction

0A	0A	00	BF	00	07

Operand 1 before Operation

*	20	,	20	20	20	.	20	20		*	
00B5	00B6	00B7	00B8	00B9	00BA	00BB	00BC	00BD	00BE	00BF	<-Storage Positions

Operand 2 before and after Operation

0	1	0	8	0	R	
0002	0003	0004	0005	0006	0007	<-----Storage Positions

Note: R represents hex D9 (-9)

Operand 1 after Operation

*	0	,	1	0	8	.	0	9		*	
00B5	00B6	00B7	00B8	00B9	00BA	00BB	00BC	00BD	00BE	00BF	<-Storage Positions

Note: Storage position 00BD contains a 9 because the zone bits of all replaced characters in the edit pattern are set to hex F (binary 1111).

Program Status Bits after Operation

```
00000010
0      7 <-----Bits
```

Insert and Test Characters (ITC)

	Op Code (Hex)	Q-Byte* (Hex)	Operand Addresses** (Hex)			
Operands	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**
A1(L1),A2	0B	L1-1	Operand 1 address		Operand 2 address	
A1(L1),D2(,R1)	1B	L1-1	Operand 1 address		Op 2 disp from XR1	---
A1(L1),D2(,R2)	2B	L1-1	Operand 1 address		Op 2 disp from XR2	---
D1(L1,R1),A2	4B	L1-1	Op 1 disp from XR1	Operand 2 address		---
D1(L1,R1),D2(,R1)	5B	L1-1	Op 1 disp from XR1	Op 2 disp from XR1	---	
D1(L1,R1),D2(,R2)	6B	L1-1	Op 1 disp from XR1	Op 2 disp from XR2	---	
D1(L1,R2),A2	8B	L1-1	Op 1 disp from XR2	Operand 2 address		---
D1(L1,R2),D2(,R1)	9B	L1-1	Op 1 disp from XR2	Op 2 disp from XR1	---	
D1(L1,R2),D2(,R2)	AB	L1-1	Op 1 disp from XR2	Op 2 disp from XR2	---	

* The Q-byte designates the operand length:

L1-1 = the number of bytes in operand 1, minus 1.

Operand 2 is a 1-byte field.

** Address operand 1 by its leftmost position.

Operation

The single character at the operand 2 address replaces all the characters to the left of the first significant digit in operand 1. Only the decimal digits 1 through 9 are significant.

If the leftmost byte of a field to be printed contains a character that must not be replaced (for example, a dollar sign), the first operand should start with the byte to the right of that character.

The operation occurs from left to right. Filling operand 1 with the character from operand 2 or finding a significant digit in operand 1 ends the operation.

Program Notes

- Operand 2 is not changed.
- At the end of this operation, the address recall register contains the address of the first significant digit; if no significant digit is found, it contains the address of the byte to the right of the first operand. This new information remains in the register until the system executes the next subtract zoned, add zoned, branch, zero and add zoned, load, load address, or insert and test characters instruction that loads the ARR.

Note: The PACT address for the first operand is not passed to the ARR. Special handling is required for the PACT address if you are using both translated and not translated addresses.

Resulting Program Status Byte Settings

The Insert and Test Characters (ITC) machine instruction does not affect the program status register.

Example

Instruction

OB	09	00	B6	00	10

Operand 1 before Operation

*	0	,	1	0	8	.	0	9		*	
OOB5	OOB6	OOB7	OOB8	OOB9	OOBA	OOBB	OOBC	OOBD	OOBE	OOBF	<-Storage Positions

Operand 2 before and after Operation

*

0010 <-----Storage Positions

Operand 1 after Operation

*	*	*	1	0	8	.	0	9		*	
OOB5	OOB6	OOB7	OOB8	OOB9	OOBA	OOBB	OOBC	OOBD	OOBE	OOBF	<-Storage Positions

Note: The first operand does not include address OOB5.

Address Recall Register after Operation

00	B8

Jump On Condition (JC)

	Op Code* (Hex)	Q-Byte** (Hex)	R-Byte*** (Hex)
Operation	Byte 1	Byte 2	Byte 3
A1,I	F2	xxxx xxxx	IAR disp
A1,I	F1	xxxx xxxx	IAR disp

* An op code of hex F2 is a jump forwards, and an op code of hex F1 is a jump backwards.

** The Q-byte contains a binary mask that indicates which status register bits (the bits in the rightmost byte of the program status register) are tested by the machine instruction.

*** The R-byte is a displacement that is added to or subtracted from the address in the machine instruction address register after the program has been incremented past the jump instruction.

Operation

The Jump On Condition (JC) machine instruction, under control of the Q-byte, tests the 1-byte program status register. If the register meets the conditions set up by the Q-byte, the system adds (if the op code is hex F2) or subtracts (if the op code is hex F1) the value stored in the instruction R-byte (byte 3) to the contents of the instruction address register and stores the result in the instruction address register. The program jumps to the new address stored in the instruction address register at the end of the jump on condition operation. If the register does not meet the condition(s) set up by the Q-byte, the system advances to the next sequential machine instruction in the program. The Q-byte determines what conditions are tested and if the jump is to occur on condition true (when the specified program status register bit is 1) or condition false (when the specified program status register bit is 0).

Bits 2 through 7 of the Q-byte determine the bits to be tested in program status register's rightmost byte. These bits, and the conditions they represent, are:

Q-Byte

Bit	Condition Tested
7	Equal
6	Low
5	High
4	Decimal overflow
3	Test false
2	Binary overflow

When bit 0 of the Q-byte is 1 (condition true), the jump occurs if any of the indicators tested is on (associated bit is 1). When bit 0 of the Q-byte is 0 (condition false), the jump occurs if all the indicators tested are off (associated bits all are 0).

Program Notes

- The assembler generates an op code of F1 if the jump to label value is less than the current value in the instruction address register after the IAR has been incremented past the jump instruction. The assembler generates an op code of F2 if the jump to label value is greater than or equal to the current value in the instruction address register. The op code of hex F1 is used for jump backwards and the R-byte is calculated by subtracting the IAR from the jump address. The op code of hex F2 is used for jump forwards and the R-byte is calculated by adding the jump address to the IAR.

- Bits 5, 6, and 7 of the program status byte can never all be zero:

  - A Q-byte of hex 80, x7, or xF (where x is 0, 1, 2, 3, 4, 5, 6, or 7) causes the system to ignore the machine instruction (no operation occurs), except the program status register bits 3 and 4 are reset if tested.

  - A Q-byte of hex 00, x7, or xF (where x is 8, 9, A, B, C, D, E, or F) causes an unconditional jump.

Resulting Program Status Byte Setting

Bit	Name	Condition Indicated
7	Equal	Bit not affected
6	Low	Bit not affected
5	High	Bit not affected
4	Decimal overflow	Turned off if tested; otherwise, not affected
3	Test false	Turned off if tested; otherwise, not affected
2	Binary overflow	Bit not affected

Example

Instruction

F2	00110000	0F

0BBD 0BBE 0BBF <-----Storage Positions

Instruction Address Register after Operation

0B	CF

Program Status Byte before Operation

00001001

0 7 <-----Bits

Program Status Byte after Operation

00001001

0 7 <-----Bits

Load Address (LA)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
A1,RX	C2	Rx	xx	xx
D1(,R1),RX	D2	Rx	xx	---
D1(,R2),RX	E2	Rx	xx	---

* Rx specifies the register into which the address is to be loaded.

** When the op code is C2, the system moves the machine instruction bytes 3 and 4 value (operand address) to the register specified by the Q-byte. When the op code is D2, the system adds the machine instruction byte 3 value to the contents of XR1 and stores the result in the register specified by the Q-byte. When the op code is E2, the system adds the machine instruction byte 3 value to the contents of XR2 and stores the result in the register specified by the Q-byte.

Operation

If the instruction is in the 4-byte format (op-code C2), the 2-byte operand is taken from the instruction stream and loaded into the register specified by the Q-byte.

If the instruction is in the 3-byte format (op code D2 or E2), the 1-byte operand is taken from the instruction stream and added to the contents of the index register specified by the op code. The result of this addition is loaded into the register specified by the Q code.

When bit 0 of a valid defined Q code is on, the instruction operates on three bytes of data rather than the normal two bytes. If the instruction is direct (op code C2), the most significant byte of data is taken from the PACT register PDIR and catenated to the two bytes of immediate data contained in operand 2 of the instruction. This data is then moved to the appropriate index register and associated PACT register. If the instruction is indexed (op code D2 or E2), the most significant byte of data is taken from the PACT register PXR1 or PXR2 respectively and catenated to the 2-byte sum of the contents of the highest 2 bytes of the index register, XR1 or XR2 respectively, and the single byte displacement field contained in operand 2. This data is then moved to the selected index register and associated PACT register. If the PDIR is to be loaded the least significant 2 bytes are not used. The Q-byte coding is:

Q-Byte

Hex	Register Specified
00	XR2
01	XR1
02	XR2
03	XR1
04[2]	LCRR, RSVD
08	Address recall register
10	Instruction address register
20	Instruction address register
40	Instruction address register
41	XR1
42	XR2
43	Address recall register
44	WR4
45	WR5
46	WR6
47	WR7
A0[1]	PDIR
A1[1]	PXR1, XR1
A2[1]	PXR2, XR2
A3[1]	PIAR, IAR
All others	Reserved; do not use

[1] These Q-bytes make the instruction privileged so they can only be used by privileged programs. They are used in a 3-byte load address, where the most significant byte comes from the PDIR, PXR1, or PXR2 PACT register. Which PACT register is used is determined by the op code of C2, D2, or E2 respectively.

[2] The instruction does not load the program status register.

Program Notes

- You can use the Load Address (LA) machine instruction to perform an unconditional branch without changing the address recall register; load the branch address into the instruction address register. At the end of this machine instruction, the program advances to the machine instruction at that address. This function is also supported mnemonically by the branch direct (BD) instruction.

- The Load Address (LA) machine instruction does not load the program status register.

Resulting Program Status Byte Setting

The Load Address (LA) machine instruction does not affect the program status register.

Example

Instruction

D2	02	05

Index Register 1

2A	15

Index Register 2 after Operation

2A	1A

Load Program Mode Register (LPMR)

	Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Operation	Byte 1	I2 Byte 2	I1 Byte 3
I1,I2	F6	80 or 00	I

Operation

If the Q-byte equals hex 80 then the contents of the program mode register bits 0 and 7 are replaced by the corresponding values in the R-byte.

If the Q-byte equals hex 00 then all bits 0 through 7 from the R-byte are put in the PMR and the PACT bits are also replaced.

If the Q-byte equals something other that hex 00 or hex 80 the instruction is treated as an invalid op code.

If this instruction is used when program mode register bit 7 is on (program is not privileged), the instruction execution is inhibited and a main storage processor storage exception check occurs.

This instruction is privileged.

The bit assignments in the program mode register are:

PMR-Byte

Bit	**Description**
0	Enable/disable task dispatching
1	Not used
2	Not used
3	PXR1 (translation bit)
4	PIAR (translation bit)
5	PXR2 (translation bit)
6	PDIR (translation bit)
7	Not privileged mode

Resulting Program Status Byte Setting

The Load Program Mode Register (LPMR) instruction does not affect the program status register.

Load Register (L)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
A1,RX	35	Rx	Operand 1 address	
D1(,R1),RX	75	Rx	Op 1 disp from XR1	---
D1(,R2),RX	B5	Rx	Op 1 disp from XR2	---

* Rx specifies the register into which data is loaded.

** Operand 1 is a 2- or 3-byte field addressed by its rightmost byte; operand 2 is not used. Operand 1 will be a 3-byte field if the Q-byte is A0, A1, A2, or A3.

Operation

The Load Register (L) machine instruction moves data from the 2-byte or 3-byte field specified by the operand address into the register specified by the Q-byte. The Q-byte coding is:

Q-Byte

Hex	**Register Specified**
00	None, the system ignores (no-op) the instruction
01	XR1
02	XR2
03	XR1
04	LCRR, PSR
08	Address recall register
10	Instruction address register
20	Instruction address register
40	Instruction address register
41	XR1
42	XR2
43	Address recall register
44	WR4
45	WR5
46	WR6
47	WR7
A0[1]	PDIR
A1[1]	PXR1, XR1
A2[1]	PXR2, XR2
A3[1]	PIAR, IAR
All others	Reserved; do not use

[1] These Q-bytes make the instruction privileged so they can only be used by privileged programs. They are 3-byte fields and are loaded as a 2-byte register preceded by a 1-byte PACT. If the PDIR is used the two low order bytes are not loaded, but the left hand byte of the 3-byte field is loaded in the PDIR.

Program Notes

- You can use the Load Register (L) machine instruction to perform an unconditional branch without changing the address recall register; load the branch to address into the instruction address register. At the end of this machine instruction, the program advances to the machine instruction at that address.

- If the Q-code is hex 04 (program status register), the high order byte (of the 2-byte field addressed by the instruction) is placed in the length count recall register and the low byte is placed in the program status register. The six rightmost bits (bits 2 through 7) of the program status register are condition indicators. These bits are designated the program status byte throughout this manual. The other program status register bits are not used and are always set to zero. The PSR must have one, and only one of bits 5, 6, or 7 on. If some other combination of bits are loaded into the PSR they are reset to one of the following combinations:

Operand 1 Bits			Resultant PSR Bits		
13	14	15	5	6	7
X	0	0	1	0	0
X	0	1	0	0	1
X	1	0	0	1	0
X	X	1	0	0	1

X can be either 1 or 0.

Resulting Program Status Byte Setting

The Load Register (L) machine instruction does not affect the program status register unless that is the register specified by the Q-byte.

Example

Instruction

35	00000010	00	11

Operand

00000000	00000010

0010 0011 <-----Storage Positions

Index Register 2 before Operation

00001100	00110001

0 7 8 15 <-----Bits
Byte 0 Byte 1

Index Register 2 after Operation

00000000	00000010

0 7 8 15 <-----Bits
Byte 0 Byte 1

Move Characters (MVC)

	Op Code (Hex)	Q-Byte* (Hex)	Operand Addresses** (Hex)			
Operands	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**
A1(L1),A2	0C	L-1	Operand 1 address		Operand 2 address	
A1(L1),D2(,R1)	1C	L-1	Operand 1 address		Op 2 disp from XR1	---
A1(L1),D2(,R2)	2C	L-1	Operand 1 address		Op 2 disp from XR2	---
D1(L1,R1),A2	4C	L-1	Op 1 disp from XR1	Operand 2 address		---
D1(L1,R1),D2(,R1)	5C	L-1	Op 1 disp from XR1	Op 2 disp from XR1	---	
D1(L1,R1),D2(,R2)	6C	L-1	Op 1 disp from XR1	Op 2 disp from XR2	---	
D1(L1,R2),A2	8C	L-1	Op 1 disp from XR2	Operand 2 address		---
D1(L1,R2),D2(,R1)	9C	L-1	Op 1 disp from XR2	Op 2 disp from XR1	---	
D1(L1,R2),D2(,R2)	AC	L-1	Op 1 disp from XR2	Op 2 disp from XR2	---	

* The Q-byte designates the operand length:

L-1 = the number of bytes in either operand, minus 1.

Maximum length of each operand is 256 bytes; both operand must be the same length.

** The operands may overlap. Address operands by their rightmost byte.

Operation

The Move Characters (MVC) machine instruction places the contents of operand 2, byte by byte, into operand 1. It is possible to propagate one character through a complete field by setting the operand 2 address one byte to the right of the operand 1 address.

Program Note

CAUTION
Overlapping the operands with the rightmost byte of the first operand to the left of the rightmost byte of the second operand destroys part of the second operand before it is used in the operation.

Resulting Program Status Byte Setting

The Move Characters (MVC) machine instruction does not affect the program status register.

Example

Instruction

0C	05	1A	06	2B	5A

Operand 1 before Operation

D1	C1	D4	C5	E2	40

1A01 1A02 1A03 1A04 1A05 1A06 <-----Storage Positions

Operand 2 before Operation

D9	D6	C2	C5	D9	E3

2B55 2B56 2B57 2B58 2B59 2B5A <-----Storage Positions

Operand 1 after Operation

D9	D6	C2	C5	D9	E3

1A01 1A02 1A03 1A04 1A05 1A06 <-----Storage Positions

Move Hexadecimal Character (MVX)

	Op Code (Hex)	Q-Byte* (Hex)	Operand Addresses** (Hex)			
Operands	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**
A1(I),A2	08	I	Operand 1 address		Operand 2 address	
A1(I),D2(,R1)	18	I	Operand 1 address		Op 2 disp from XR1	---
A1(I),D2(,R2)	28	I	Operand 1 address		Op 2 disp from XR2	---
D1(I,R1),A2	48	I	Op 1 disp from XR1	Operand 2 address		---
D1(I,R1),D2(,R1)	58	I	Op 1 disp from XR1	Op 2 disp from XR1	---	
D1(I,R1),D2(,R2)	68	I	Op 1 disp from XR1	Op 2 disp from XR2	---	
D1(I,R2),A2	88	I	Op 1 disp from XR2	Operand 2 address		---
D1(I,R2),D2(,R1)	98	I	Op 1 disp from XR2	Op 2 disp from XR1	---	
D1(I,R2),D2(,R2)	A8	I	Op 1 disp from XR2	Op 2 disp from XR2	---	

* I = one byte of immediate data that specifies which portion of each 1-byte operand is used in the operation.

** Both operands are 1-byte fields.

Operation

The Move Hexadecimal Character (MVX) machine instruction moves the numeric part (bits 4 through 7) or the zone part (bits 0 through 3) of the second operand to the numeric or zone part of the first operand, as specified by the Q-byte. Q-byte coding is:

Q-Byte

Hex	**Register Specified**
00	Move data from operand 2 zone portion to operand 1 zone portion
01	Move data from operand 2 numeric portion to operand 1 zone portion

02 Move data from operand 2 zone portion to operand 1 numeric portion

03 Move data from operand 2 numeric portion to operand 1 numeric portion

Program Notes

- The 6 leftmost bits in the Q-byte immediate data should be 0's.
- The second operand is not changed unless both operands specify the same byte.

Resulting Program Status Byte Setting

The Move Hexadecimal Character (MVX) machine instruction does not affect the program status register.

Example

Instruction

98	01	A0	65

Index register 1 = 2B15
Index register 2 = 1F20

Operand 1 before Operation

2F

1FC0 <-----Storage Positions

Operand 2 before and after Operation

4C

2B7A <-----Storage Positions

Operand 1 after Operation

CF

1FC0 <-----Storage Positions

Move Logical Immediate (MVI)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	Byte 1	Byte 2	Byte 3	Byte 4
A1,I	3C	I	Operand 1 address	
D1(,R1),I	7C	I	Op 1 disp from XR1	---
D1(,R2),I	BC	I	Op 1 disp from XR2	---

* I = 1 byte of immediate data (for example, 1 byte of actual data or a 1-byte mask).

** Operand 1 is a 1-byte field; operand 2 is not used.

Operation

The Move Logical Immediate (MVI) machine instruction moves the Q-byte into operand 1.

Resulting Program Status Byte Setting

The Move Logical Immediate (MVI) machine instruction does not affect the program status register.

Example

Instruction

3C	AF	2F	CB

Operand 1 before Operation

00

2FCB <-----Storage Positions

Operand 1 after Operation

AF

2FCB <-----Storage Positions

Set Bits Off Masked (SBF)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	Byte 1	Byte 2	Byte 3	Byte 4
A1,I	3B	xxxx xxxx	Operand 1 address	
D1(,R1),I	7B	xxxx xxxx	Op 1 disp from XR1	---
D1(,R2),I	BB	xxxx xxxx	Op 1 disp from XR2	---

* The Q-byte contains a 1-byte binary mask specifying operand bits to be turned on.

** Operand 1 is a 1-byte field; operand 2 is not used.

Operation

The system looks at the Q-byte, bit by bit. If it finds a binary 1 in the Q-byte, the system sets the corresponding bit in the operand byte to 0; if it finds a binary 0 in the Q-byte, it does not change the corresponding bit in the operand.

Resulting Program Status Byte Setting

The Set Bits Off Masked (SBF) machine instruction does not affect the program status register.

Example

Instruction

3B	10000001	00	30

Operand 1 before Operation

01111001

0030 <-----Storage Positions

Operand 1 after Operation

01111000

0030 <-----Storage Positions

Set Bits On Masked (SBN)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	Byte 1	Byte 2	Byte 3	Byte 4
A1,I	3A	xxxx xxxx	Operand 1 address	
D1(,R1),I	7A	xxxx xxxx	Op 1 disp from XR1	---
D1(,R2),I	BA	xxxx xxxx	Op 1 disp from XR2	---

* The Q-byte contains a 1-byte binary mask specifying operand bits to be turned on.

** Operand 1 is a 1-byte field; operand 2 is not used.

Operation

The system looks at the Q-byte, bit by bit. If it finds a binary 1 in the Q-byte, it sets the corresponding bit in the operand byte to 1; if the system finds a binary 0 in the Q-byte, it does not change the corresponding bit in the operand.

Resulting Program Status Byte Setting

The Set Bits on Masked (SBN) machine instruction does not affect the program status register.

Example

Instruction

3A	01011010	00	20

Operand 1 before Operation

00001100

0020 <-----Storage Positions

Operand 1 after Operation

01011110

0020 <-----Storage Positions

Shift Right Character (SRC)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)		
Operands	**Byte 1**	**Byte 2**		**Byte 3**	**Byte 4**
A1,(L),I	3E	I-1	L-1	Operand 1 address	
D1(L,R1),I	7E	I-1	L-1	Op 1 disp from XR1	---
D1(L,R2),I	BE	I-1	L-1	Op 1 disp from XR2	---

* The Q-byte designates how much is to be shifted:

I-1 (4 bits) = the number of bits to be shifted, minus 1.

L-1 (4 bits) = the number of bytes to be shifted, minus 1.

The maximum length of operand 1 is 16 bytes; the maximum number of bit positions to be shifted is 16.

** Address operand 1 by its rightmost byte; operand 2 is not used.

Operation

The Shift Right Character (SRC) machine instruction shifts operand 1 to the right one more than the number of bit positions specified by the number in bits 0 through 3 of the Q-byte. Incoming bits are set to zero. The system resets the binary overflow bit during this operation if no 1s are shifted out.

Resulting Program Status Byte Settings

Bit	Name	Condition Indicated
7	Equal	The remaining string is all zeros.
6	Low	Even and not zero.
5	High	Odd.
4	Decimal overflow	Bit not affected.
3	Test false	Bit not affected.
2	Binary overflow	Any 1s shifted out.

Example

Instruction

BE	31	00

Index register 2 = 1FC0

Operand 1 before Operation

1E	2F

1FBF 1FC0 <-----Storage Positions

Operand 1 after Operation

01	E2

1FBF 1FC0<-----Storage Positions

Program Status Byte after Operation

00100010

0 7 <-----Bits

Store Register (ST)

	Op Code (Hex)	**Q-Byte* (Binary)**	**Operand Addresses** (Hex)**	
Operands	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
A1,RX	34	Rx	Operand 1 address	
D1(,R1),RX	74	Rx	Op 1 disp from XR1	---
D1(,R2),RX	B4	Rx	Op 1 disp from XR2	---

* Rx specifies the register whose contents are to be stored.

** Operand 1 is a 2- or 3-byte field addressed by its rightmost byte; operand 2 is not used. Operand 1 will be a 3-byte field if the Q-byte is A0, A1, A2, or A3.

Operation

The Store Register (ST) machine instruction places the contents of the register specified by the Q-byte into the 2-byte or 3-byte field specified by the operand address. If XR1 or XR2 is being stored using the A1 or A2 Q-byte registers, the operand must be a 3-byte field.

Q-Byte

Hex	**Register Specified**
00	None, the system ignores (no-op) the instruction
01	XR1
02	XR2
03	XR1
04	Q, program status register
08	Address recall register
10	Instruction address register
20	Instruction address register
40	Instruction address register
41	WR1 which equal the two right bytes of XR1
42	WR2 which equal the two right bytes of XR2
43	Address recall register
44	WR4
45	WR5
46	WR6
47	WR7
A0[1]	PDIR
A1[1]	PXR1, XR1
A2[1]	PXR2, XR2
A3[1]	PIAR, IAR
All others	Reserved; do not use

[1] These Q-bytes make the instruction privileged so they can only be used by privileged programs. They are 3-byte fields, and they are stored as a 2-byte register preceded by a 1-byte PACT. If the stored PDIR is used the two low order bytes are not affected, but the PDIR is stored in the left hand byte of the 3-byte field.

Program Notes

The LCRR and PSR is stored in the 2-byte field addressed by the instruction.

Resulting Program Status Byte Setting

The Store Register (ST) machine instruction does not affect the program status register.

Example

Instruction

34	00001000	32	BB

Address Recall Register

0A	CD

Operand before Operation

2F	C2

32BA 32BB <-----Storage Positions

Operand after Operation

0A	CD

32BA 32BB <-----Storage Positions

Subtract from Register (S)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
A1,RX	37	Rx	Operand 1 address	
D1(,R1),RX	77	Rx	Op 1 disp from XR1	---
D1(,R2),RX	B7	Rx	Op 1 disp from XR2	---

* Rx specifies the register whose contents are modified by the machine instruction.

** Operand 1 is a 2-byte field addressed by its rightmost byte; operand 2 is not used. No carry is added to the PACT of the register that contains the total after the subtraction.

Operation

The Subtract from Register (S) machine instruction subtracts the binary number in operand 1 from the contents of the 2-byte register selected by the Q-byte and stores the result in the register. If operand 1 is numerically greater than the contents of the register the result occurs as if the contents of the register has an additional high-order binary digit. The Q-byte coding is:

Q-Byte

Hex	Register Specified
00	None, the system ignores (no-op) the instruction
01	XR1
02	XR2
03	XR1
04	Q, program status register
08	Address recall register
10	Instruction address register
20	Instruction address register
40	Instruction address register
41	XR1
42	XR2
43	Address recall register
44	WR4
45	WR5
46	WR6
47	WR7
A0[1]	PDIR
A1[1]	PXR1, XR1
A2[1]	PXR2, XR2
A3[1]	PIAR, IAR
All others	Reserved; do not use

[1] These Q-bytes make the instruction privileged so they can only be used by privileged programs. No carry is added to the PACT of the register that contains the total after the subtraction. If the PDIR is used the instruction is a no op, since only the high order byte of the PDIR is defined and the instruction only affects the low order two bytes.

Program Notes

- If the Q-code is hex 04 (program status register), the high order byte (of the two byte field addressed by the instruction) is placed in the length count recall register and the low byte is placed in the program status register. Subtracting from the program status register causes unpredictable results; a hex 04 is forced into the high byte before the subtraction is done.
- This machine instruction does not change the operand.

CAUTION
The results in the program status register are not reliable if it is the register selected.

Resulting Program Status Byte Settings

Bit	Name	Condition Indicated
7	Equal	Zero results.
6	Low	Contents of register was less than operand 1 before the operation.
5	High	Contents of register was greater than operand 1 before the operation.
4	Decimal overflow	Bit not affected.
3	Test false	Bit not affected.
2	Binary overflow	Bit not affected.

Example

Instruction

37	00000010	00	04

Operand 1

01001000	00100000

0003 0004 <-----Storage Positions

Index Register 2 before Operation

01110101	01101010

Index Register 2 after Operation

00101101	01001010

Program Status Byte after Operation

00000100

0 7 <-----Bits

Subtract Logical Characters (SLC)

	Op Code (Hex)	Q-Byte* (Hex)	Operand Addresses** (Hex)			
Operands	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**
A1(L1),A2	0F	L1-1	Operand 1 address		Operand 2 address	
A1(L1),D2(,R1)	1F	L1-1	Operand 1 address		Op 2 disp from XR1	---
A1(L1),D2(,R2)	2F	L1-1	Operand 1 address		Op 2 disp from XR2	---
D1(L1,R1),A2	4F	L1-1	Op 1 disp from XR1	Operand 2 address		---
D1(L1,R1),D2(,R1)	5F	L1-1	Op 1 disp from XR1	Op 2 disp from XR1	---	
D1(L1,R1),D2(,R2)	6F	L1-1	Op 1 disp from XR1	Op 2 disp from XR2	---	
D1(L1,R2),A2	8F	L1-1	Op 1 disp from XR2	Operand 2 address		---
D1(L1,R2),D2(,R1)	9F	L1-1	Op 1 disp from XR2	Op 2 disp from XR1	---	
D1(L1,R2),D2(,R2)	AF	L1-1	Op 1 disp from XR2	Op 2 disp from XR2	---	

* The Q-byte designates the operand length:

L1-1 = the number of bytes in either operand, minus 1.

Maximum length of each operand is 256 bytes; both operand must be the same length.

** The operands may overlap. Address operands by their rightmost byte.

Operation

The Subtract Logical Characters (SLC) machine instruction subtracts the binary number in operand 2 from the binary number in operand 1 and stores the result in operand 1. If the second operand is numerically larger than the number stored in the first operand, the result occurs as if the first operand has an additional high-order binary digit. The result can never be negative. For example:

```
First operand     0110 1101
Second operand    0111 1110
Result            1110 1111
```

Program Note

CAUTION

Overlapping the operands with the rightmost byte of the first operand to the left of the rightmost byte of the second operand destroys part of the second operand before it is used in the operation.

Resulting Program Status Byte Settings

Bit	Name	Condition Indicated
7	Equal	Zero results.
6	Low	Operand 1 was smaller than operand 2 before execution.
5	High	Operand 1 is greater than operand 2 before the operation.
4	Decimal overflow	Bit not affected.
3	Test false	Bit not affected.
2	Binary overflow	Bit not affected.

Example

Instruction

AF	03	00	10

Note: Index register 1 = 0CC0

Operand 1 before Operation

		10010110	01011010	01110111	10111111
		0CBD	0CBE	0CBF	0CC0<-Storage Positions

Operand 2 before and after Operation

		01110100	10000110	01100010	10100100
		0CCD	0CCE	0CCF	0CD0<-Storage Positions

Operand 1 after Operation

		00100001	11010100	00010101	00011011
		0CBD	0CBE	0CBF	0CC0<-Storage Positions

Program Status Register before Operation

00000001

0 7 <-----Bits

Program Status Register after Operation

00000100

0 7 <-----Bits

Subtract Logical Immediate (SLI)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	Byte 1	Byte 2	Byte 3	Byte 4
A1,I	3F	I	Operand 1 address	
D1(,R1),I	7F	I	Op 1 disp from XR1	---
D1(,R2),I	BF	I	Op 1 disp from XR2	---

* I = 1 byte of immediate data (that is, 1 byte of actual data).

** Operand 1 is a 1-byte field; operand 2 is not used.

Operation

The Subtract Logical Immediate (SLI) machine instruction subtracts the binary number in the Q-byte from the binary number in operand 1 and stores the result in operand 1. If the value in the Q byte is numerically larger than operand 1, the result occurs as if operand 1 has an additional high-order binary digit.

Resulting Program Status Byte Settings

Bit	Name	Condition Indicated
7	Equal	Operand 1 value before the operation is equal to the the Q-byte value.
6	Low	Operand 1 value before the operation is less than the the Q-byte value.
5	High	Operand 1 value before the operation is greater than the Q-byte value.
4	Decimal overflow	Bit not affected.
3	Test false	Bit not affected.
2	Binary overflow	Bit not affected.

Example

Instruction

3F	F5	00	21

Operand 1 before Operation

75

0021 <-----Storage Positions

Operand 1 after Operation

80

0021 <-----Storage Positions

Program Status Byte after Operation

00000010

0   7 <-----Bits

Subtract Zoned Decimal (SZ)

	Op Code (Hex)	Q-Byte* (Hex)		Operand Addresses** (Hex)			
Operands	**Byte 1**	**Byte 2**		**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**
A1(L1),A2(L2)	07	L1-L2	L2-1	Operand 1 address		Operand 2 address	
A1(L1),D2(L2,R1)	17	L1-L2	L2-1	Operand 1 address		Op 2 disp from XR1	---
A1(L1),D2(L2,R2)	27	L1-L2	L2-1	Operand 1 address		Op 2 disp from XR2	---
D1(L1,R1),A2(L2)	47	L1-L2	L2-1	Op 1 disp from XR1	Operand 2 address		---
D1(L1,R1),D2(L2,R1)	57	L1-L2	L2-1	Op 1 disp from XR1	Op 2 disp from XR1	---	
D1(L1,R1),D2(L2,R2)	67	L1-L2	L2-1	Op 1 disp from XR1	Op 2 disp from XR2	---	
D1(L1,R2),A2(L2)	87	L1-L2	L2-1	Op 1 disp from XR2	Operand 2 address		---
D1(L1,R2),D2(L2,R1)	97	L1-L2	L2-1	Op 1 disp from XR2	Op 2 disp from XR1	---	
D1(L1,R2),D2(L2,R2)	A7	L1-L2	L2-1	Op 1 disp from XR2	Op 2 disp from XR2	---	

* The Q-byte designates the operand length:

L1-L2 (4 bits) = the number of bytes in operand 1, minus the number of bytes in operand 2.

L2-1 (4 bits) = the number of bytes in operand 2, minus 1.

Maximum length of operand 1 is 31 bytes; maximum length of operand 2 is is 16 bytes.

** The operands may overlap. Address operands by their rightmost byte.

Operation

The Subtract Zoned Decimal (SZ) machine instruction algebraically subtracts operand 2 from operand 1, byte by byte, and stores the result in operand 1. The main storage processor sets the zone bits of all operand 1 bytes except the rightmost byte to hex F (binary 1111). It sets the zone bits of the rightmost byte in operand 1 to (1) hex F (binary 1111) if the result of the operation is either positive or 0, or (2) hex D (binary 1101) if the result is negative.

Program Notes

- The second operand is not changed unless the fields overlap.

- The system does not check for valid decimal digits in either operand.

- The decimal overflow condition indicator (program status bit 4) may be set on during this operation. Program status bit 4 can be reset by:

  - A system reset

  - Testing decimal overflow with a branch on condition or jump on condition instruction

  - Loading a 0 in bit 4 of the program status register using the load register instruction

- The system stores the rightmost address of operand 1 in the address recall register (ARR) and leaves the ARR modified with data that should not be used.

CAUTION
Overlapping the operands with the rightmost byte of the first operand to the left of the rightmost byte of the second operand destroys part of the second operand before it is used in the operation.

Resulting Program Status Byte Setting

Bit	Name	Condition Indicated
7	Equal	Zero results
6	Low	Negative results
5	High	Positive results
4	Decimal overflow	Carry occurred from the leftmost position of operand 1
3	Test false	Bit not affected
2	Binary overflow	Bit not affected

Example

Instruction

07	22	00	10	00	20

Operand 1 before Operation

	F7	F6	F3	F6	F9

000C 000D 000E 000F 0010 <-----Storage Positions

Operand 2 before and after Operation

			F4	F2	F5

001E 001F 0020 <-----Storage Positions

Operand 1 after Operation

	F7	F5	F9	F4	F4

000C 000D 000E 000F 0010 <-----Storage Positions

Program Status Register before Operation

00000001

0 7 <-----Bits

Program Status Register after Operation

00000100

0 7 <-----Bits

Test Bits Off Masked (TBF)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	Byte 1	Byte 2	Byte 3	Byte 4
A1,I	39	xxxx xxxx	Operand 1 address	
D1(,R1),I	79	xxxx xxxx	Op 1 disp from XR1	---
D1(,R2),I	B9	xxxx xxxx	Op 1 disp from XR2	---

* The Q-byte contains a 1-byte binary mask specifying operand bits for testing.

** Operand 1 is a 1-byte field; operand 2 is not used.

Operation

The Test Bits Off Masked (TBF) machine instruction tests specified bits in the operand byte to see if they are off. For each mask bit (Q-byte bit) that is a 1, the system tests the matching bit in the operand. If any tested bit is a 1, the system turns the test false indicator (in the program status register) on.

Program Notes

- The operand and Q-byte are not changed.
- The Test Bits Off Masked (TBF) operation may turn on the test false condition. The test false condition is turned off by system reset, by using test false as a condition in a branch on condition or jump on condition instruction, or by loading a binary 0 into the program status register bit 11 (bit 3 of the rightmost program status register byte).

Resulting Program Status Byte Setting

Bit	Name	Condition Indicated
7	Equal	Bit not affected.
6	Low	Bit not affected.
5	High	Bit not affected.
4	Decimal overflow	Bit not affected.
3	Test false	At least one of the tested bits is on.
2	Binary overflow	Bit not affected.

Example

Instruction

39	01101100	00	25

Operand 1 before and after Operation

10010100

0025 <-----Storage Position

Program Status Byte after Operation

00010000

0 7 <-----Bits

Test Bits On Masked (TBN)

	Op Code (Hex)	Q-Byte* (Binary)	Operand Addresses** (Hex)	
Operands	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
A1,I	38	xxxx xxxx	Operand 1 address	
D1(,R1),I	78	xxxx xxxx	Op 1 disp from XR1	---
D1(,R2),I	B8	xxxx xxxx	Op 1 disp from XR2	---

* The Q-byte contains a 1-byte binary mask specifying operand bits for testing.

** Operand 1 is a 1-byte field; operand 2 is not used.

Operation

The Test Bits on Masked (TBN) machine instruction tests specified bits in the operand byte to see if they are on. For each mask bit (Q-byte bit) on, the system tests the matching bit in the operand. If any tested bit is off, the system turns the test false indicator (in the program status register) on.

Program Notes

- The operand and Q-byte are not changed.
- The Test Bits on Masked (TBN) operation may turn on the test false condition. The test false condition is turned off by:
  - System reset
  - Using test false as a condition in a branch on condition or a jump on condition instruction
  - Loading a binary 0 into program status register bit 11 (bit 3 of the rightmost program status register byte)

Resulting Program Status Byte Setting

Bit	Name	Condition Indicated
7	Equal	Bit not affected.
6	Low	Bit not affected.
5	High	Bit not affected.
4	Decimal overflow	Bit not affected.
3	Test false	At least one of the tested bits is not on.
2	Binary overflow	Bit not affected.

Example

Instruction

38	00010110	00	21

Operand 1 before and after Operation

```
| 10010101 |
    0021     <-----Storage Position
```

Program Status Byte after Operation

```
| 00010000 |
 0        7 <-----Bits
```

Transfer (XFER)

	Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Operands	Byte 1	I Byte 2	I Byte 3
I1,I2	F5	01	xx
I1,I2	F5	02	xx

Operation

The Transfer (XFER) machine instruction transfers control to the extended control store supervisor. The main storage processor is halted until it is again started by the control storage processor.

Program Notes

When the Q-byte is hex 02 the instruction is used for BASIC language and the R-byte must be hex 00. When the Q-byte is hex 01 the instruction is used for FORTRAN language and the R-byte for this instruction has the following meanings:

R-Byte

Hex	Meaning
01	Start main program execution
02	Start subprogram execution
03	Again enter user program after call operation
04	Subroutine return to calling module
05	Start next scientific instruction
06	Invalid
07	Start next scientific instruction after invoke scientific instruction
08-0F	Invalid

Resulting Program Status Byte Setting

The Transfer (XFER) instruction does not affect the program status register.

Zero and Add Zoned (ZAZ)

	Op Code (Hex)	Q-Byte* (Hex)		Operand Addresses** (Hex)			
Operands	**Byte 1**	**Byte 2**		**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**
A1(L1),A1(L2)	04	L1-L2	L2-1	Operand 1 address		Operand 2 address	
A1(L1),D2(L2,R1)	14	L1-L2	L2-1	Operand 1 address		Op 2 disp from XR1	---
A1(L1),D2(L2,R2)	24	L1-L2	L2-1	Operand 1 address		Op 2 disp from XR2	---
D1(L1,R1),A2(L2)	44	L1-L2	L2-1	Op 1 disp from XR1	Operand 2 address		---
D1(L1,R1),D2(L2,R1)	54	L1-L2	L2-1	Op 1 disp from XR1	Op 2 disp from XR1	---	
D1(L1,R1),D2(L2,R2)	64	L1-L2	L2-1	Op 1 disp from XR1	Op 2 disp from XR2	---	
D1(L1,R2),A2(L2)	84	L1-L2	L2-1	Op 1 disp from XR2	Operand 2 address		---
D1(L1,R2),D2(L2,R1)	94	L1-L2	L2-1	Op 1 disp from XR2	Op 2 disp from XR1	---	
D1(L1,R2),D2(L2,R2)	A4	L1-L2	L2-1	Op 1 disp from XR2	Op 2 disp from XR2	---	

* The Q-byte designates the operand length:

L1-L2 (4 bits) = the number of bytes in operand 1, minus the number of bytes in operand 2.

L2-1 (4 bits) = the number of bytes in operand 2, minus 1.

Maximum length of operand 1 is 31 bytes; maximum length of operand 2 is is 16 bytes.

** The operands may overlap. Address operands by their rightmost byte.

Operation parameters

The Zero and Add Zoned (ZAZ) machine instruction copies data from the second operand, byte by byte starting with the rightmost byte, into the first operand. If the first operand is longer than the second operand, the main storage processor fills the extra positions with high-order EBCDIC zeros (hex F0).

The main storage processor sets the zone bits of all bytes except the rightmost byte in the first operand to hex F (binary 1111). It sets the zone bits of the rightmost byte in the first operand to (1) hex F if the value moved is either zero or positive, or (2) hex D (binary 1101) if the value moved is negative.

Program Notes

- The second operand is not changed unless the fields overlap.
- The system stores the rightmost address of operand 1 in the address recall register (ARR) and leaves the ARR modified with data that should not be used.

CAUTION
Overlapping the operands with the rightmost byte of the first operand to the left of the rightmost byte of the second operand destroys part of the second operand before it is used in the operation.

Resulting Program Status Byte Setting

Bit	Name	Condition Indicated
7	Equal	Zero result
6	Low	Negative result
5	High	Positive result
4	Decimal overflow	Bit not affected
3	Test false	Bit not affected
2	Binary overflow	Bit not affected

Example

Instruction

04	22	00	10	00	20

Operand 1 before Operation

	F7	F6	F3	F6	F9	
	000C	000D	000E	000F	0010	<-----Storage Positions

Operand 2 before and after Operation

			F4	F2	F5	
			001E	001F	0020	<-----Storage Positions

Operand 1 after Operation

	F0	F0	F4	F2	F5	
	000C	000D	000E	000F	0010	<-----Storage Positions

Program Status Register before Operation

00000001	
0 7	<-----Bits

Program Status Register after Operation

00000100	
0 7	<-----Bits

Supervisor Call (SVC)

	Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Operation	**Byte 1**	**Byte 2**	**Byte 3**
I2,I1	F4	xx	xx

The supervisor call instruction stops the main storage processor and generates an interrupt to the control processor. The main storage processor hardware saves the status of the main storage processor registers when the processor stops. The control store SVC processor uses the R-byte to determine what type of supervisor call has been requested. The individual supervisor call handlers use the Q-byte to further define the requested function.

The three primary types of supervisor calls are:

- Immediate supervisor call: The request is processed immediately on interrupt level five (IL5) by the specified supervisor call handler. On completion, the main storage processor is again started either for the task that issued the immediate SVC or for another more important task that is ready (if task switching is not disabled).

- Overlapped: The SVC is processed on the main program level while a different task (if ready) runs in the main storage processor, unless task switching is disabled.

- Delayed supervisor call: The SVC is processed on the MPL while a different task (if ready) runs in the main storage processor, unless task switching is disabled. Data related to this request is saved in an action control element and chained to one of the delayed supervisor call processor handler's queues. Control is returned to the requesting task when the delayed supervisor call is complete or when the ACE is built, depending on the Q-byte (see the Q-byte definition for each delayed supervisor call).

The supervisor call instructions are 3 to 6 bytes long, depending on the number of inline parameters passed with the request. The format and function of each supervisor call is described on the following pages. Control returns to the requesting task immediately following the last byte of the requested supervisor call instruction. A supervisor call op code cannot reside within the last 5 bytes of the last 2K page of a task.

General Wait

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)	
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
F4	xx	00	xx	xx

This is an overlapped and privileged SVC.

The general wait supervisor call instruction allows multiple tasks to wait on a specified condition. There are 16 separate conditions which may be passed to the general wait handler through the inline parameter list (bytes 4 and 5). The condition passed is saved in the caller's task block in the field's TB_WMASK and TB_WMSK2. The task does not receive control of the main storage processor until the condition being waited on is posted using supervisor call 01 (general post).

With overlapped SVCs, the SVCs are not always processed in the same order that they are issued. This could cause a task to finish in a general wait with nothing to post it because the general post was processed before the general wait. The main store program should disable task switching to serialize the processing of general waits and general posts.

The first 8 bits of the inline parameter list (byte 4) are reserved for use by the control storage supervisor:

Inline parameter 1

Bit	Meaning if On
80	System queue space (SQS) failure
40	Task work area allocate failure
20	Test and set failure
10	Not used
08	Not used
04	Disk resource failure
02	Disk record failure
01	Work station release wait

Inline parameter 2

Bit	Meaning if On
80	Printer allocate failure
40	Communication line allocate failure
20	Diskette allocate failure
10	Disk space allocate failure
08	Other device allocation failure
04	ICS transient waiter
02	Quick lock failure
01	Not used

Input Parameters

Q-Byte

Bit	Meaning if On
0	Not used.
1	Long wait: Storage owned by the task is released immediately.
2-5	Not used.
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program and its storage cannot be released.

Inline parameter 1: General wait mask (byte 4).

Inline parameter 2: General wait mask (byte 5).

Example

Program A wants to be placed into a wait state on the printer. Another program (program B) currently owns the printer resource. When program B is done with the printer, the program always issues a general post (supervisor call 01). Program A issues the following supervisor call:

Assembler	Object Code	Description
SVC SVCGWAIT,00 DC XL2'0080'	F400000080	Issue the SVC

Program A waits until the general post before continuing.

In this system the programs must use 0080 for the printer.

General Post

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)	
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
F4	00	01	xx	xx

This is an overlapped and privileged SVC.

The general post supervisor call instruction allows a task to post all tasks waiting on a specified condition. These tasks are made ready and receive control on the basis of their current priorities. The conditions specified on the general post supervisor call must match the conditions specified on the general wait (supervisor call 00). The first inline parameter list byte (byte 4) is reserved for use by the control storage supervisor.

A general post affects only those tasks in a general wait at the time the general post is processed. A general wait processed any time after the general post will not be satisfied by that general post. The general wait task remains waiting.

With overlapped SVCs, the SVCs are not always processed in the same order that they are issued. This could cause a task to finish in a general wait with nothing to post it because the general post was processed before the general wait. The main store program should disable task switching to serialize the processing of general waits and general posts.

Input Parameters

Q-Byte

Bit	Meaning if On
0, 1, 3-7	Not used.
2	Sets off the lock byte indicator, specified in work register 5, in task block lock byte 1.

Inline parameter 1: General wait mask post code (byte 4).

Inline parameter 2: General wait mask post code (byte 5).

Work register 5: The lock mask is reset in task block lock byte 1. This only applies if bit 2 is on in the Q-byte.

Example

A program owns the printer resource and now wants to free it. A general post is issued for any program currently in a wait state on the printer resource.

Assembler	Object Code	Description
SVC SVCGPOST,00 DC XL2'0080'	F400010080	Issue the SVC

In this system the main storage program must use 0080 for the printer.

Note: If no tasks are currently waiting for the printer resource, this supervisor call does not post any tasks.

Event Wait

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	02

This is an overlapped and privileged SVC.

The event wait supervisor call instruction allows the user to wait for completion of a specified event (specific wait) or any one of a group of events (multiple wait). For specific waits, the address of the event control mask being waited on must be in index register 1 (XR1). The event is defined complete if the 7th byte of the event control mask has bit 1 = 1, or the related action control element (ACE) is on the task complete queue. If bit 3 of the Q-byte is on, the wait is satisfied if command processor (CP) error bit is on in the ACE.

For multiple waits, Q-byte bit 4 must be on. In this case, the wait is satisfied if any event is complete for this task and bit 0 = 1 in the 6th byte of the event control mask, or the wait is satisfied if the multiple wait bit in the ACE is on and any event type requirements are met. If bit 4 and bit 5 of the Q-byte is on, then work register 6 contains event types, or 0 for all event types. The multiple wait is only satisfied if the event types match. When a wait is satisfied, control returns with index register 1 containing the address of the completed event control mask. If bit 2 of the Q-byte is on, the content of XR2 is set from the XR2 value in the ACE. If bits 4 and 5 of the Q-byte is on, WR6 is set to the event type from the ACE. For more information on the event control mask and the action control elements, refer to the *System Data Areas* manual.

Input Parameters

Q-Byte

Bit	Meaning if On
1	Long wait: storage and programs are released immediately.
2	Return XR2.
3	Command processor asynchronous wait.
4	Multiple wait: only a multiple wait event satisfies this wait.
5	Event type: Only valid with the multiple wait. WR6 contains the event type or types that can satisfy the wait on input and contains the event type that satisfies the wait on output.
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program, and storage cannot be released.
7	Wait: If off, this SVC does not put the task in a wait if no event is complete.

Index register 1: Contains the address of the event control mask. This register is meaningless if the multiple wait is specified (Q-byte bit 4).

Work register 6: Contains the event type or types. Work register 6 is only used if the Q-byte bits 4 and 5 are on.

Output Values

Index register 1: Contains the address of the event that satisfies this wait.

Index register 2: Contains XR2 value associated with the complete event if requested (Q-byte bit 2).

Work register 6: Contains event type associated with the complete event if requested (Q-byte bit 4 and 5).

PSR: If Q-byte bit 7 is off (wait without wait), the program status register is set equal if the wait is satisfied and not equal if the wait is not satisfied.

Example

A user issues a request for disk I/O. Index register 1 contains the address of the disk input/output block (hex 003000). The user issues an event wait supervisor call to wait for completion of the disk operation.

Assembler	Object Code	Description
SVC SVCWAIT,00	F40102	Issue the SVC

with index register 1 containing address 003000
and location 003006 containing hex 00.

When the disk operation is completed without error, control returns with location 003006 containing hex 40.

Event Post

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)	
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
F4	xx	03	xx	xx

This is an overlapped and privileged SVC.

The event post supervisor call instruction indicates that a specified event is complete. The event post instruction uses the 7-byte event control mask whose address is given by the requesting task in index register 1 (XR1). The 7th byte of the event control mask is altered to hex 4n where n is the completion code given by the user in the second inline parameter byte (byte 5).

The first inline parameter byte (byte 4) specifies the queue header number associated with the event. An action control element, related to the event, must have previously been queued to this system queue. Bytes 3, 4, and 5 of the event control mask must contain the address of the related action control element. If there is no action control element address, the event post request is ignored.

If the task associated with the event being posted is waiting for the event to complete, the task is made ready and is given control of the main storage processor on the basis of its current priority. If the task associated with the event being posted is not waiting for the event to complete, the action control element is left on the task complete queue.

Note: The event address must be in real storage.

Input Parameters

Q-Byte

Bit	Meaning if On
0-7	Not used.

Inline parameter 1: The queue header number.

Inline parameter 2

Bit	Meaning if On
0	Not used.
1	Last-in-first-out (LIFO) queue action control element to complete queue of task being posted.
2-3	Not used; must be zero.
4-7	Completion code (0-F).

Example

Program A issues supervisor call 02 (SVC SVCWAIT,00) with index register 1 equal to 006000. Program B then issues:

Assembler	Object Code	Description
SVC SVCPOST,00 DC XL1'48' DC XL1'44'	F400034844	Issue the SVC

Index register 1 points to location 006000. Location 006006 contains 00.

After event post, location 006006 contains 44 and program A is made ready to run in the main storage processor.

Note: An action control element must be queued to system queue header number hex 48.

Transfer Control by ID

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	Byte 2	Byte 3	Byte 4
F4	xx	04	xx

This is an overlapped SVC.

This supervisor call may be privileged, depending on the program to which control is being transferred.

The transfer control supervisor call allows programs to pass control to specified SSP routines.

The ID of the transient to be given control is passed in inline parameter one and is an index into the main storage transfer control table.

The main storage transfer control table contains 5-byte transfer blocks for common SSP routines.

Transfer Table Entry

Bytes	Description
0, 1, 2	Program disk address, or program block address if the program is resident.
3	Number of program sectors.
4	Program execution attributes:

Hex	*Attributes*
80	Program executes in translated storage.
40	Program requires swapping to disk.
20	Requester must be privileged.
10	Program is resident (program block address is in bytes 0 through 2).
08	Not used.
04	Core size not equal to program size.
02	Program requires the system transient area.
01	Not used.

Input parameters

Q-Byte

Hex	Meaning if On
80	Not used
40	Long wait
20	Asynchronous transfer; module called runs as a separate task
10	Not used
08	Satisfies multiple wait
04	Event type given in WR6
02	Not used
01	Return control to the requesting program

Inline parameter 1: Identifies the requested entry in the transfer control table.

Example

Program A issues a transfer control to a resident program with inline parameter 1 equal to hex 3F.

Assembler	Object Code	Description
SVC SVCXFER,01 DC XL1'3F'	F400043F	Issue the SVC

The value in the table related to hex 3F is 0023800F10

After this supervisor call, control is given to the routine whose program block address is 002380. The program block contains the start control address of the routine.

Free Second Request Block

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	00	05

This is an overlapped and privileged SVC.

The second request block is dequeued from the task block request block chain and freed.

Input Parameters

Q-byte: Not used; must be zero.

Output Values

The RB__RBQ field, of the current RB (TB__RBQ) now contains the address of what was the 3rd RB on the stack, if any, before the free second request block was issued.

Example

The program issues a free second request block supervisor call with TB__RBQ = 007200. Locations 007202-007204 = 007800 and locations 007802-007804 = 008500. After the user issues:

Assembler	Object Code	Description
SVC SVCUNSTK,00	F40005	Issue the SVC

The locations 007202-007204 = 008500.

Assign

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	xx	06

This is an overlapped and privileged SVC.

The assign supervisor call instruction allocates the storage out of the system queue space. Storage is assigned in multiples of 16 bytes on 16-byte boundaries.

The amount of storage to be assigned must be loaded into index register 1 when the Assign SVC instruction is performed. An option to queue assigned areas to the task block of the requester is available using a bit in the Q-byte (bit 5 = 1 or to a different task block, when Q-byte bit 2 also is on, where the task block address is passed in XR2). For a queued request the control storage supervisor adds 5 bytes to the amount of storage to be assigned; the last 5 bytes assigned are then used to maintain the queue. The requester must not change this area.

If enough space is not available, the user may either wait for some free space to become available (Q-byte bit 7=1) or have control returned immediately with index register 1 set to all zeros (Q-byte bit 7 = 0). Requests for large amounts of free space are more likely to fail since the area assigned must be contiguous space. A wait request to assign more than 2K bytes of space is invalid.

Input Parameters

Q-Byte

Bit	Meaning if On
0,1,3,4	Not used; must be zero.
2	Queue to the task block whose address is passed in XR2. Bit 5 must also be on.
5	Queue the assigned area to the requester's TB.
6	Reserved
7	Wait for assign area to become available.

Index register 1: Length of storage to assign.

Index register 2: If bits 2 and 5 are on in the Q-byte queue, the address of the task block is passed in XR2.

Output Values

Index register 1: Address of the area assigned (zero if no space is assigned and the no wait option of the Q-byte is specified).

Example

Program A issues the assign supervisor call to allocate 256 bytes of storage from system queue space (SQS) and queue it to the task block. Program A is willing to wait for the storage if space is not immediately available. Program A loads index register 1 with hex 100 and issues:

Assembler	Object Code	Description
SVC SVCASGN,05	F40506	Issue the SVC

After this supervisor call has executed, an area of length hex 0110 is assigned to program A. The last 5 bytes are used to queue this area to the task block of program A. The address of the hex 0110 bytes allocated to the program is returned in index register 1 (that is, for example, index register 1 contains 004850).

Note: This is always a 16-byte boundary.

Free Assigned Areas

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	07

This is an overlapped and privileged SVC.

The free instruction returns previously assigned storage area to the system queue space. This area freed is either merged to one of the current free areas (if adjacent) or queued to the free chain. The type of assign used when getting storage (queued or not queued) must be indicated. This supervisor call also permits a partial free of the originally assigned area (nonqueued only) if the area freed is a multiple of 16 bytes on a 16-byte boundary.

Input Parameters

Q-Byte

Bit	Meaning
0-1	Not used; must be zero.
2	The area to be freed is queued to the TB whose address is passed in XR2. Bit 5 must also be on.
3-4	Not used; must be zero.
5	The area to be freed is queued to a task block. If bit 2 is off, the area is queued to the requester's task block. If Bit 2 is on, the area is queued to the task block whose address is passed in XR2.
6-7	Not used; must be zero.

Index register 1: Address of area to free.

Index register 2: task block address, if the area to be freed is queued to a task block other than the one from the requester.

Work register 6: Length of the area to be freed. If the area is queued to a task block, this length does not include the 5 bytes added on to the assigned area to maintain the queue.

Example

Program A wants to free 256 bytes of storage area that was previously assigned from system queue space. The address of the area assigned is hex 004850. The original request was a queued request. Program A loads index register 1 with hex 004850 and work register 6 with hex 100 then issues:

Assembler	Object Code	Description
SVC SVCFREE,04	F40407	Issue the SVC

The total area of hex 0110 bytes is freed and is made available for other users of system queue space and then is dequeued from the task block of program A.

Increment System Event Counters

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	Byte 2	Byte 3	Byte 4
F4	xx	08	xx

This is an overlapped and privileged SVC.

This function allows a main storage routine to increase the system event counters in control storage. For a description of the system event counters, see the *System Data Areas* manual.

Input Parameters

Q-byte: Not used; must be zero.

Inline Parameters

Input parameter 1: Displacement in table of system event counter (range 0 to 23).

Example

Assembler	Object Code	Description
SVC SVCISEC,00 DC XL'10'	F4000810	Issue the SVC

The seventeenth counter (a displacement of hex 10 in the system event counter table) is incremented by 1.

Sense Data Switches

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	00	09

Note: This SVC cannot be used on the 5364 System Unit.

This is an overlapped and privileged SVC.

The sense data switches supervisor call senses the switch values and returns the values in the XR1 register.

Output Parameters

Index register 1: Contains the output switch values.

Example

Program A wants to set the output switch values into index register 1.

Assembler	Object Code	Description
SVC SVCSNSSW,00	F40009	Issue the SVC

Set Task Privileged

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	00	0A

This is an immediate and dynamically privileged SVC.

The set task privileged supervisor call sets the program mode register to privileged for this task.

Input Parameters

Q-byte: Must be zero.

Example

Program A (which is dynamically privileged) wants to run as a privileged task.

Assembler	Object Code	Description
SVC SVCPRIV,00	F4000A	Issue the SVC

Post Action Controller Status Word

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	Byte 2	Byte 3	Byte 4
F4	00	0B	xx

This is an overlapped and privileged SVC.

This routine posts the appropriate control storage routine to be executed. The control storage routine receives control on the basis of its priority after the supervisor call has executed.

Input Parameters

Q-byte: Not used; must be zero.

Inline parameter 1: The mask value associated with the action controller routine is to be posted. The ACWEQ macro contains the equates used for posting action controller routines. Refer to the *System Data Areas* manual for the equates used.

Example

Program A issues the following instruction.

Assembler	Object Code	Description
SVC SVCPPSVC,00 DC XL1'17'	F4000B17	Issue the SVC

The action controller routine associated with the value hex 17 is given control after this instruction is performed. The exact time that control is passed to the routine is dependent on other work being done by the control storage processor.

Fast Transfer

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	Byte 2	Byte 3	Byte 4
F4	00	0C	xx

This is an immediate and not privileged SVC.

This instruction passes control from the requester to a routine that is resident in main storage. The particular routine to be given control is determined by the inline parameter given with this SVC. The requested routine receives control with dispatching disabled and in privileged mode.

Input Parameters

Q-byte: Not used; must be zero.

Inline parameter 1: Identifies the routine to be given control. It corresponds to an offset into the system fast transfer control table from which the entry address of the desired routine is taken.

The fast transfer table has a 4-byte save area for the fast transfer caller and four 4-byte entries of main storage resident data management routine addresses that can be called when a fast transfer SVC (SVCFXFER) is issued. The label D1FXTBL@ is the direct area word that points to the table. The five data management routines that the caller can transfer control to are:

Hex	Routine
00	Disk data management request
04	Work station request
08	Printer request
0C	Spool request
10	Folder management I/O request

Example

Program A issues a Fast Transfer with inline parameter 1 equal to hex 04.

Assembler	Object Code	Description
SVC SVCFXFER,00	F4000C	Issue the SVC
DC XL1'04'	04	

The value in the fast transfer table related to hex 04 is 006320.

After this instruction is executed the requested resident routine is given control at address 006320 with dispatching disabled and is in privileged mode.

Fast Exit

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	Byte 2	Byte 3	Byte 4
F4	xx	0D	xx

This is an immediate and privileged SVC.

This instruction exits a resident routine that was provided control by a Fast Transfer SVC. Control may be given back to the program that originally issued the Fast Transfer SVC, or it may be provided to any routine that may be accessed by the Transfer Control/System Transient SVC. In the latter case the fast exit instruction is changed to an overlapped SVC (with an R-Byte of hex 04). The routine to be provided control is a logical extension of the resident routine requested by the original Fast Transfer SVC; more processing is to be performed before returning control to the original program.

Input Parameters

Q-Byte

Bit	Meaning
0-6	Not used; must be zero.
7	If off, return control to the program originally issuing the Fast Transfer SVC. If on, pass control to the routine identified by inline parameter 1.

Inline parameter 1: Identifies the program to be given control via the system transfer control table. See the Transfer Control/system transient SVC for further information. This parameter is used only if bit 7 = 1 in the Q-Byte.

Example

A resident routine wishes to pass control to another program before returning control to the original program.

```
Assembler           Object Code      Description

SVC SVCFEXIT,1      F4010D           Issue the SVC
DC XL1'1C'          1C
```

The program identified by entry hex 1C in the System Transfer Table will be given control. When it exits, control will be passed back to the original program.

Queue/Dequeue

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)		
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
F4	00	0E	xx	xx	xx

This is an immediate and privileged SVC.

This instruction provides the functions to maintain the system queues. The functions provided are:

- Queue FIFO (first-in-first-out): Place the block at the end of queue.
- Queue LIFO (last-in-first-out): Place the block first on the queue.
- Queue FIFO by priority: Place the block at the end of blocks of equal priority.
- Queue LIFO by priority: Place the block at the front of blocks of equal priority.
- Dequeue.

These functions are provided for any of the system queues or for a queue header passed by the caller. The chaining field may be located anywhere within the first 256 bytes of the block to be manipulated. The priority field, if given, must be located within the first 16 bytes of the block to be queued.

No check is made for an invalid queue (that is, never ending or recursive queue). All blocks and the queue header must be located in real storage.

Input Parameters

Q-Byte: Not used; must be zero.

Inline parameter 1: Queue header number. The queue header number is the displacement from the start of the queue headers to the right byte and divided by four. The queue header number is valid for system requests only. Refer to the HEADR macro in *System Data Areas* manual for system queue header displacements.

Inline parameter 2: Displacement into control block of chaining field: range 0 to 255, right byte.

Inline parameter 3: Queuing indicators and priority field displacement.

Bit	Meaning if On
0	Priority request.
1	System request (system queue header number is in inline parameter 1).
2	Dequeue request.
3	LIFO request.
4-7	Priority field displacement (0-F).

Index register 1: Address of control block.

Index register 2: Address of queue header for nonsystem requests (right byte).

Example

Program A wants to FIFO queue control block X to the system queue located at offset hex 4F into the system queues. The offset into the control block of the right byte of the chaining field is hex 07:

Assembler	Object Code	Description
SVC SVCQUEUE,00 DC XL3'130740'	F4000E130740	Issue the SVC

Index register 1 contains 0034A0. Location 0034A0 contains 000044008700329000.

Currently the given system queue has the following values:

000B4F = 0042F0
0042F0 = 000000000000338000
003380 = 000000000000000000

After the queue request:

```
000B4F = 0042F0
0042F0 = 000000000000338000
003380 = 00000000000034A000
0034A0 = 000044008700000000
```

System Control Block Access

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)	
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
F4	00	0F	xx	xx

This is an overlapped and privileged SVC.

This instruction allows a main storage user to access 2 or 3 bytes from a control storage direct area. This routine also allows a main storage user to pick up 3 bytes from a system queue header in main storage.

Input Parameters

Q-Byte Not used, must be zero.

Inline parameter 1: Area and function.

Bit	Meaning

0	Specifies the input or output register
	If = 0 uses the XR2 register
	If = 1 uses the XR1 register

1-3	Identifies direct area to be used
	If = 000, direct area 0
	If = 001, direct area 1
	If = 010, direct area 2
	If = 011, direct area 3
	If = 100, direct area 4
	If = 101, direct area 5
	If = 110, direct area 6
	If = 111, direct area 7

4	Specifies 2-byte or 3-byte operation
	If = 0 uses 2-byte operation
	If = 1 uses 3-byte operation

5	Specifies the location of the prefix byte If = 0 prefix is in low byte If = 1 prefix is in high byte
6	(If = 1) Queue header request
7	(If = 1) Put request

Inline parameter 2: Displacement from the start of the direct area to the word that contains the right hand two data bytes.

Inline parameter 3: Displacement from the start of the direct area to the word that contains the left hand two data bytes. This parameter is ignored if the Q-Byte bit 4 is off.

Index register 1 or 2: Two or three byte data area (if put request).

Output Parameters

Index register 1 or 2: Data area retrieved (if get request).

Example

Program A wants to get 2 bytes from control storage location 2047, with location 2047 containing 0A42. Index register 1 contains 801000 before the instruction.

Assembler	Object Code	Description
SVC SVCSCB,00 DC XL3'204700'	F4000F20470D	Issue the SVC

with location 2047 containing 0A42.

After executing the instruction, index register 1 contains 000A42.

Transfer Control by Address

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)		
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
F4	xx	10	xx	xx	xx

This is an overlapped and privileged SVC.

This instruction provides the same function as the transfer control by ID instruction (R-Byte of 04) for transferring to programs not contained in the system transfer control table. The address of the table entry is passed directly by the caller in inline parameters 1 and 2 (bytes 4 and 5).

Input parameters

Q-Byte

Bit	Meaning if On
0	Not used
1	Not used
2	Asynchronous transfer; the module called runs as a separate task
3	Not used
4	Satisfies multiple wait
5	Event type given in WR6
6	Not used
7	Return control to the requesting program

Inline parameters 1 and 2: Address in main storage of a transient/transfer control table entry may be in either real or translated storage; however, it must be the same translation as the caller's instruction address register.

Inline parameter 3: Entry point number. The entry point number is an index into the entry point table of the program. SSP programs can optionally define multiple entry points in a table that is pointed to by the identifier of the program. See IDEQ in the *System Data Areas* manual.

Example

Program A wants to pass control to a program with the disk sequential sector address of the program specified within the task storage.

Assembler	Object Code	Description
SVC SVCXCTL,00 DC AL2(TRAN@) DC XL1(00)	F40010184200	Issue the SVC

where TRAN@ is at location 1842 and location 1842 contains 000F920602

This supervisor call loads the program from the disk sequential sector address of 0F92 (for a length of 6 sectors) into main storage. Control is given to the transient, after it is loaded, at the start of the program (entry point 0).

Main Storage Exit

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	00	11

This is an overlapped and privileged SVC.

This instruction returns control to the caller of a routine. Control is returned at the next sequential instruction following the transfer supervisor call (either 04 or 10).

Note: *The RETURN-NO capability described under supervisor call 04 or 10 may cause control to be returned to a module other than the immediate caller. If RETURN-NO indicator is used on supervisor call 04 or 10, control is returned to the most recent routine that specified RETURN-YES. If no RETURN-YES has been specified (the program has no caller), then the task is terminated.*

Input Parameters

Q-Byte: Not used; must be zero.

Example

Program X has completed execution and wants to return control to its caller. The main storage transient exit instruction is issued:

Assembler	Object Code	Description
SVC SVCEXIT,00	F40011	Issue the SVC

Control is returned to the next sequential instruction of the caller of program X, if program X was called with RETURN-Y. If program X has no caller the task is sent to termination.

Get Page

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)	
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
F4	xx	12	xx	xx

This is an overlapped and not privileged SVC.

This instruction expands the user's main storage size up to the region size.

Input Parameters

Inline parameters 1 and 2: Address of where to store the last logical address plus 1. Since this address is one byte beyond the end of the caller's addressable storage, any address equal to, or greater than this value causes the program to end, but not in a normal way. The par byte is assumed to be the same as the par for the IAR.

Output Parameters

The last logical address plus 1 is returned in the address passed by the caller in the inline parameters 1 and 2.

Example

Program A is a translated program currently executing in 14K of main storage. When program A was requested, the user specified a region size of 24K. To acquire the additional storage, program A issues:

Assembler	Object Code	Description
SVC SVCGETP,00 DC XL2'2200'	F400122200	Issue the SVC

After this supervisor call executes, location hex 802200 contains the address plus 1 of the last byte in the region of program A. If program A originates at location 0000, and the full 24K was allocated, locations 802200 and 802201 contains the value hex 6000 (24K beyond the origin location of 0000). If for example 20K was allocated to program A, then locations 802200 and 802201 contains hex 5000.

Maintain User Area Pages

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	Byte 2	Byte 3	Byte 4
F4	00	13	xx

This is an overlapped and privileged SVC.

The maintain user area pages supervisor call performs various functions pertaining to the user storage. The specific function to be performed is indicated by the value specified in the inline parameter 1.

Input Parameters

Q-Byte: Not used; must be zero.

Inline parameter 1: Specifies the function to be performed.

Value Hex	Meaning
00	Return number of pages in the user area.
01	Pin the requested storage (make it nonswappable). If the index register 1 is nonzero, the index register 1 contains the address of the storage block which identifies the storage to be pinned. If index register 1 is zero, the number of pages to pin is indicated in work register 6.
02	Unpin the requested storage (make it swappable). Index register 1 contains the address of the storage block which identifies the storage to be unpinned.
03	Create a swappable storage region for the specified job. The address of the JCB is given in index register 1. The size of the region is specified in work register 6.
04	Change the swappable storage region for the specified job. The address of the JCB is given in index register 1. The new size of the region is specified in work register 6.
05	Delete the swappable storage region for the specified job. The address of the JCB is given in index register 1.

Index register 1: Specifies the storage block address for the functions specified by hex 01 and 02, and the JCB address for the functions specified by hex 03, 04, and 05.

Work register 6: Specifies the number of pages to pin for the function specified by hex 01 if no storage block address is given, and specifies the desired swappable region size for the functions specified by hex 03 and 04.

Output Parameters

Program status register: An equal condition is returned for all successful requests. A low condition is returned for all failing requests. Functions requested by hex 00, 02, and 05 cannot fail. Functions requested by hex 01, 03, and 04 will fail if there is not enough main storage to satisfy the request.

Work register 6: Contains the current number of pages in the user area of main storage for all successful requests.

Example

A program wants to retrieve the number of pages in the user area of main storage.

Assembler	Object Code	Description
SVC SVCMSPAG,00	F4001300	Issue the SVC requesting the number of pages in the user area of main storage to be returned in work register 6.
DC XL1'00'		

Asynchronous Task Wait

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	Byte 2	Byte 3	Byte 4
F4	xx	17	xx

This is an overlapped and privileged SVC.

This instruction places the task block (TB) specified in index register 1 into a wait state. The type of wait (defined under supervisor call 1E, task wait) is specified using inline parameter 1.

Task switching must be disabled when this supervisor call is issued (see LPMR instruction).

Input Parameters

Q-Byte

Bit	Meaning if On
0	Not used
1	Long wait; storage and programs are released immediately
2	Not used
3	Not used
4	Not used
5	Not used
6	Not used
7	Not used

Inline parameter 1: Wait type.

Index register 1: Address of task control block to be placed in a wait state.

Output Parameters

Program status register: Equal if task was put in a wait. Not equal if task could not be put in a wait.

Example

Program A and program B are executing under two different TBs. Program A wants to suspend the execution of program B.

Assembler	Object Code	Description
L @TBB,XR1		Load B's TB address
SVC SVCTKWT,00	F4001702	Issue the SVC
DC XL1'02'		

where @TBB contains B's TB address.

Program B's TB is placed in a suspended wait until it is posted by program A using supervisor call 1D.

Set Transient Area Not Busy

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	00	18

This is an overlapped and privileged SVC.

The main storage transient area is set not busy. The control store supervisor will now schedule the next task waiting for the transient area.

Input Parameters

Q-Byte: Not used; must be zero.

Example

Program A issued a fetch request from the transient area (supervisor call 52). The module loaded receives control outside the transient area. This module needs to release the transient area for other programs:

Assembler	Object Code	Description
SVC SVCXNTOF,00	F40018	Issue the SVC

Post Action Control Element

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)	
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
F4	00	19	xx	xx

This is an overlapped and privileged SVC.

This instruction posts an event complete using the action control element address as input. The event control mask address is retrieved from the action control element (in the index register 1 save area field) and the event is posted as in event post (supervisor call 03).

The first inline parameter byte (byte 4) specifies the queue header number associated with the event. An action control element, related to the event, must have previously been queued to this system queue. Bytes 3, 4, and 5 of the event control mask must contain the address of the related action control element. If there is no action control element address, the event post request is ignored.

Input Parameters

Q-Byte: Not used.

Inline parameter 1: The queue header number where the action control element can be found.

Inline parameter 2: Indicators and completion code.

Bit	Meaning
0	Not used.
1	(If = 1) Queue last-in-first-out to task control block complete queue.
2-3	Not used.
4-7	Completion code (0 through F).

Index register 1: Action control element address.

Example

Program A wants to post an event complete. The event was created using supervisor call 4C. The address of the action control element created by supervisor call 4C is hex 003470. Program A issues:

Assembler	Object Code	Description
L ACE,XR1		Load ACE address into XR1
SVC SVCPOSTA,00	F400194800	Issue the SVC
DC XL1'48'		
DC XL1'00'		

where ACE contains the action control element address

After completion of this supervisor call, the action control element at location hex 003470 is dequeued from the system header number 48 and queued to the task block field TB__CMPLQ of the task that issued the supervisor call 4C. If the task is already waiting for the post, the action control element is dequeued and freed. The task is then made ready to run.

Log Trace Information

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)		
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
F4	00	1A	xx	xx	xx

This is an immediate and not privileged SVC.

This instruction logs trace entries in the resident main storage trace buffer. The entry is only logged if the trace ID table is enabled. The function trace ID table for the main trace table is located at hex 0250 in main storage. The function trace ID tables for alternate trace tables are located in the trace control block queued to the trace control block queue. The function trace ID is used to index to the bit in the table.

The first inline parameter byte (byte 4) specifies the function trace ID. The trace ID is a number from hex·10 to hex 7F. Bit 0 is not used and should be zero. Bits 1 through 4 specify the byte index and bits 5 through 7 identify the bit within the byte to determine if the trace ID is enabled.

Example

Function Trace ID = Hex 73
Trace ID Table (Hex 0250) = Hex 00000000000000100000000000000000

where the log trace entry will be logged since bit 3 (binary 00010000) of the 8th byte is set on.

The second inline parameter byte (byte 5) specifies the trace sub function ID. Any value from 0 to 255 may be specified, and is used only for reference.

The third inline parameter byte (byte 6) specifies the number of bytes of data to be moved (logged), from the data addressed by index register two, to the trace table buffer. Any value from 1 to 30 may be specified.

Input Parameters

Q-Byte: Not used; must be zero.

Index register 2: Address of information to be placed in trace table entry.

Inline parameter 1: Function trace ID (hex 10-7F).

Inline parameter 2: Sub function trace ID (0-255).

Inline parameter 3: Length of data to trace (1-30).

Example

Program A wants to log 15 bytes of data to the system trace table. The component trace ID is hex 73 and the subcomponent trace ID is hex 02. The data is at locations hex 002000 to 00200E.

Assembler	Object Code	Description
LA TRACE, XR2	C2A22000	Load trace buffer address into XR2
SVC SVCLOG,00	F4001A	Issue the SVC
DC XL1'73'	73	Inline 1 trace ID
DC XL1(02)	02	Inline 2 sub ID
DC XL1(15)	0F	Inline 3 length of entry

where TRACE is the address of the data to be traced.

The information is moved to the trace table only if the trace ID (hex 73) is enabled. Fifteen bytes are moved from the data addressed by address register 2.

Scan System Queue

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)	
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
F4	xx	1B	xx	xx

This is an immediate and privileged SVC.

This instruction allows you to scan a queue for a specific value in one of the blocks on the queue. The search argument is passed by the caller and the address of the block containing the value is returned.

Input Parameters

Q-Byte

Bit	Meaning
0	Not used.
1	Scanning the chain field.
2-4	Not used.
5-7	Length, or if 0 then return the first element on the queue.

Inline parameter 1: Argument displacement, a 1, 2, or 3-byte field (right byte).

Inline parameter 2: Chain field displacement (right byte).

Index register 1: Search argument right justified.

Index register 2: Queue header address of queue to be scanned (right byte). Queue header address must be a real address.

Output Parameters

Index register 2: Contains the address of the control block containing the passed argument. If the argument is not found, the right two bytes of index register 2 are set to 0000.

Example

Program A wants to scan the disk spindle A1 active queue to find if the task block for this program has any request pending.

```
Assembler              Object Code      Description

L   @TB,XR1                             Load address of TB
                                        into XR1
LA  QHDFDA,XR2                          Load queue header
                                        into XR2
SVC SVCQSCAN,00        F4001B1504       Issue the SVC
DC  AL1(ACETB@)
DC  AL1(ACECHAIN)
```

where @TB contains the address of the task block. QHDFDA is the queue header address. ACETB@ is the displacement of the task block address within the ACE. ACECHAIN is the chain field displacement.

If an action control element (ACE) exists on the specified queue with the task block address specified in index register 1, the address of the action control element is returned in index register 2. Otherwise, index register 2 is returned with the low two bytes set to zeros.

Task Post

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	**Byte 2**	**Byte 3**	**Byte 4**
F4	00	1D	xx

This is an overlapped and privileged SVC.

The task post supervisor call posts a task's execution status. Inline parameter 1 contains the condition to be posted. TB__STAT2 contains the task wait conditions that are turned off when the task post supervisor call is requested. If TB__STAT2 becomes all zeros because of the post, the task can be made ready to run. Task suspended is the only wait conditions available for posting from main storage.

All other wait codes are handled internally by the control storage supervisor and should be posted only when purging associated requests.

Input Parameters

Q-Byte: Not used; must be zero.

Inline parameter 1: Task post conditions.

Index register 1: Task block address of task to be posted.

Example

Program A has been suspended by an earlier task wait. To restart program A, the following supervisor call is issued:

Assembler	Object Code	Description
L @TASKA,1		Load address of TASKA TB
SVC SVCTPOST,00	F4001D02	Issue the SVC
DC XL1'02'		

where @TASKA contains the TASKA TB address.

Task Wait

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	Byte 2	Byte 3	Byte 4
F4	xx	1E	xx

This is an overlapped and privileged SVC.

This instruction places the requesting task into a wait state. Inline parameter1 is read into TB__STAT2. The task remains in the wait state until all the bits in TB__STAT2 are set off by task post (supervisor call 1D). In addition, if task dispatching is disabled, task wait automatically enables dispatching. The valid conditions to be set on in TB__STAT2 are:

- Event wait
- General wait
- Resource enqueue
- Timer wait
- Internal delayed SVC

- Suspend wait

Input Parameters

Q-Byte

Bit	Meaning
0	Not used; must be zero.
1	Long wait; storage and programs are released immediately.
2-5	Not used; must be zero.
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program and its storage cannot be released.
7	Not used; must be zero.

Inline parameter 1: Wait conditions to be set on in TB__STAT2.

Example

Assembler	Object Code	Description
SVC SVCTWAIT,00 DC XL1'02'	F4001E08	Issue the SVC

Program A waits until its task block is specifically posted by another program for the suspend wait condition.

Specific Resource Dequeue

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	00	20

This is an overlapped and privileged SVC.

This SVC updates the active share levels for the horizontal queue (nested queues) after an AQE was dequeued from the nested queue. This SVC allows the dequeue of a nested AQE that is not the top AQE.

Input Parameters

Q-Byte: Not used.

Index register 1: JCB address.

Index register 2: Resource queue header.

Example

Assembler	Object Code	Description
SVC SVCSPDEQ,00	F40020	Issue the SVC

The user program must perform the following sequence of instructions to dequeue an AQE that may be inactive (not the top AQE of the nested queue).

Task switching should be disabled while performing the following code:

Assembler	Object Code	Description
L RESQ@,XR2		Load the resource queue address
L JCB@,XR1		Load the JCB address
SVC SVCSCAN,03		Scan the resource queue for an AQE belonging to this JCB
DC AL1(AQETB@)		
DC AL1(AQECHAIN)		
L AQE@,XR1		Load AQE address save area address
ST AQENODE,XR2		Save the AQE address
CLC 0(3,XR1),XR2		Is this the desired AQE address
BE LABEL		YES, issue resource dequeue
		NO, do the following
L AQE@,XR1		Load AQE address
L JCB@,XR2		Load JCB address
LA JCBDAQEQ(,XR2 XR2)		Load JCB AQE queue header address
SVC SVCQUEUE,00		Dequeue the AQE from the JCB AQE queue
DC AL1(00)		
DC AL1(AQECBQ)		
DC AL1(X’20’)		
L AQENODE,XR2		
LA AQECBQ(,XR2),XR2		Load the nested queue header address
SVC SVCQUEUE,00		Dequeue the AQE from the nested queue
DC (00)		
DC (AQENESTQ)		
DC (X’20’)		

```
L   AQELEN,WR6                          Load the AQE length
SVC SVCFREE,00                          Free the AQE system
                                        queue space
L   RESQA,XR2                           Load resource queue
                                        header address
L   JCB@,XR1                            Load JCB address
SVC SVCPDEQ,00           F40020         Reevaluate the nested queue
                                        share level
ALC JCB@,ONE                            Set TCB address to a false
                                        value
L   JCB@,XR1                            Load JCB address
L   RESQA,XR2                           Load resource queue header
                                        address
SVC SVCRENQ,10                          Issue resource dequeue
DC  AL1(X'20')
```

The AQE will now be dequeued.

Resource Enqueue/Dequeue

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	**Byte 2**	**Byte 3**	**Byte 4**
F4	xx	21	xx

This is an overlapped and privileged SVC.

This instruction enqueues and dequeues allocation queue elements (AQEs) on a queue. It checks the share level of each queued entry and processes each accordingly.

For enqueues:

> If the caller can share with the current owners and all those waiting higher on the queue, control is returned to the caller with an allocation queue element queued to the passed queue and the equal condition set in the program status register. If the caller's task cannot share with the owning task, a nonequal program status condition is returned (low if the owner is never ending or his task is suspended, high otherwise).
>
> Optionally, a caller may wait for the resource to become available (Q code, bit 7 = 1). In this case, control will always return with equal program status condition. The allocation queue element stays enqueued to the queue and ownership is given when the caller shares with all AQEs above him.

Any more resource enqueues for the same task and same resource will only change the share level in the same AQE. Therefore, once the resource dequeue is issued, ownership of the resource is completely given up.

You may choose to nest enqueues. When nesting is active a new AQE is built for each enqueue. You may think of the resource queues as a column of queues and the nested queues as a row of queues. Each job may have only one AQE on the resource queue, but may have many AQEs on the nested queue.

For nested queues the caller retains ownership of the resource at the current level if it does not receive ownership at the new level.

For dequeues:

The allocation queue element allocated for this task is removed from the passed queue. If an allocation queue element for the caller is not queued, a nonequal program status register is returned.

For nested queues the caller releases ownership of the resource at the active level but still has ownership at its previous level (the level in the first nested AQE).

Input Parameters

Q-Byte

Bit	**Meaning**
0	Not used
1	Long wait; storage and programs are released immediately if RENQ results in a wait
2	Critical system resource
3	JCB address is in XR1
4	Not used
5	Return AQE address in XR2
6	Not used
7	Wait

Inline parameter 1

Bit	**Meaning**
Bit 0 = 0	Dequeue request
Bit 0 = 1	Enqueue request
Bit 1 = 1	NEP requester
Bit 2 = 0	Queue by TB
Bit 2 = 1	Queue by JCB
Bit 3 = 0	Nested queueing inactive
Bit 3 = 1	Nested queueing active
Bit 4 = 1	Extended level 1 active if level 1 is selected (shares with extended level 1 and 0)
Bit 5-7 = 000	Level 0 (shares with 0, 1, 2)
Bit 5-7 = 001	Level 1 (shares with 0, 1)
Bit 5-7 = 010	Level 2 (shares with 0)
Bit 5-7 = 011	Level 3 (does not share)

Index register 1: JCB address if Q-Byte bit 3 is set.

Index register 2: Address of the resource queue header (right byte). The queue header address must be a real address.

Example

Program A and program B want to use the same common area. To prevent interfering with each other, both programs agree to enqueue on the resource by defining a queue header at locations hex 000C01-000C03 in main storage. This queue header represents the resource for programs A and B. When program A issues:

Assembler	Object Code	Description
LA X'0C03',XR2	C2020C03	Load resource queue header into XR2
SVC SVCRENQ,1 DC XL1'83'	F4012183	Issue the SVC

Program A is allocated the resource and an allocation queue element (AQE) queued to locations hex 000C01-000C03. If program B now tries to allocate the same resource, program B's task block is placed in a general wait (if the Q-Byte bit 7 = 1) and an AQE put on the resource queue. When program A has completed its access of the common area, program A issues:

Assembler	Object Code	Description
LA X'0C03',XR2	C2020C03	Load resource queue header into XR2
SVC SVCRENQ,00 DC XL1'00'	F4002100	Issue the SVC

The allocation queue element for program A that was queued to locations hex 000C01-000C03 is dequeued and freed. Program B is automatically given control of the resource and the resource allocation queue element is updated to indicate program B's task block is now the owner of the specified resource.

Note: This example shows two programs requesting exclusive ownership of a resource. Various levels of sharing are possible using levels 0, 1, 2, and extended level 1.

Dump Task/Terminate Task

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)	
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
F4	xx	22	xx	xx

This is an immediate and not privileged SVC.

This instruction ends the calling task with the message identification (error) code passed in inline parameters 1 and 2. A task dump is taken to disk, diskette, or printer. The abnormal termination bit in the task block is set on. The message identification code (MIC) is stored in the task block.

Input Parameters

Q-Byte

Hex	Meaning
00	Dump this task.
01	XR1 contains the address of the task block to dump.

Inline parameters 1 and 2: Hexadecimal value of the MIC number to be used to indicate the error. If the MIC value is 0000 control is returned to the next sequential instruction following the Dump Task/Terminate Task supervisor call. If the MIC value is 0001-00FF it causes the system to program check. If the MIC value is 0100 or greater it causes a task dump to be taken and a message to be issued. The instruction address register for the issuing task is set to 0AFB (the end of job supervisor call) in the system communications area.

Example

Program A wants to end with a task dump and stop and issue MIC 0300. Program A issues:

Assembler	Object Code	Description
SVC SVCDUMP,00	F40022	Issue the SVC
DC XL'012C'	012C	

Note: If the MIC is hex 0038, a task dump is taken but the task is not terminated. Control is returned to the next sequential instruction after the dump SVC.

Test and Set

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	Byte 2	Byte 3	Byte 4
F4	xx	23	xx

This is an overlapped and privileged SVC.

This instruction allows a main storage routine to test a selected bit in storage and set the bit on at the same time. If the bit is already on, the task is put into a general wait if bit 7 is on in the Q-Byte.

Input Parameters

Q-Byte

Bit	Meaning if On
0	Not used; must be zero.
1	Long wait; storage and programs are released immediately if a wait.
2	Set the lock indicator in task block lock byte 1. Pass, in work register 5, the bit to be set on.
3-5	Not used; must be zero.
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program, and its storage cannot be released.
7	Wait if bit is already on.

Inline parameter 1: Identifies the bit to be tested.

Index register 1: Address of the byte to be tested and set.

The byte containing the bit to be tested must be in real storage (XR1 must have a real address, therefore cannot be translated).

Work register 5: Lock indicator to be set on in the requester's task block lock byte. This only applies if bit 2 is on in the Q-Byte.

Output Values

Program status register: False if the bit is on and the no wait Q-Byte is specified.

Example

Program A and program B want to exclude one another when accessing a common area. The common area is located at 005C in main storage. Both programs issue the following supervisor call before accessing the common area:

Assembler	Object Code	Description
LA X'005C,XR1	C201005C	Load address of the byte to be tested into XR1
SVC SVCTEST,4 DC XL1'02'	F4042302	Issue the SVC

If bit 6 at location hex 005C is on when the supervisor call is issued by program A, then program A is placed in a general wait. If the bit is off, it is set on and control returned immediately to program A.

After accessing the common area, both program A and program B must set the bit off and issue a supervisor call 01 (general post) for the test and set failure condition to take the waiting task out of general wait.

Task Block Priority Queue

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	**Byte 2**	**Byte 3**	**Byte 4**
F4	00	24	xx

This is an overlapped and privileged SVC.

This instruction takes the new task priority and stores it in the task block. The SVC then again queues the task block on the task priority queue and task ready queue by the new priority.

Input Parameters

Inline parameter 1: Priority.

Hex	Meaning
40	Batch priority (lowest)
80	Medium priority
81	Normal priority (interactive) and variable

C0	User high priority
Fx	System priorities

The higher the priority, the better the service that is given to a program.

The priority values given above are general values and any value between those listed can be used. Even priority values are only variable within a range (down to a value). Odd priority values are variable to any value. The behavior of the task determines how its priority varies.

Index register 1: Task block address.

Example

Program A wants to change its priority from its current value to interactive priority.

Assembler	Object Code	Description
L @TBA,XR1		Load priority task block address into XR1
SVC SVCPRIQ,00 DC XL1'81'	F002481	Issue the SVC

where @TBA contains the address of the task block of program A.

After executing this supervisor call, program A runs at the new priority.

Asynchronous Task Ready Check

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	00	25

This is an overlapped and privileged SVC.

This SVC accepts a task block address as input and determines whether the task is in an event wait, and, if so, whether the event is completed. Task block status byte 2 (TB__STAT2) is checked first to see if the passed task is in an event wait. If the task is not waiting, control is returned to the caller. If the task is waiting the complete queue of the given task is checked for an event that satisfies the tasks wait. If no event is complete, control is returned to the caller. If an event is complete, the task is posted.

Input Parameters

Q-Byte: Not used; must be zero.

Index register 1: Task block address of task to be checked.

Example

Program A wants to have program B's task block checked to determine if program B's previous wait is now satisfied.

Assembler	Object Code	Description
L @TBB,XR1		Load B's task block address into XR1
SVC SVCRDYCK, 00	F40025	Issue the SVC

where @TBB contains B's task block address.

Program B is ready to run if its previous wait is now satisfied.

Prepare Print Buffer (Not Ideographic)

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	00	26

This is an overlapped and privileged SVC.

This instruction inserts printer control codes into the print buffer to cause the requested skip and space operations. It also maintains a record of the current logical line in the print input/output block (IOB).

This instruction scans the data to be printed. When it finds more than three contiguous blanks, it compresses those blanks and replaces that data with the relative horizontal print position control codes. If it finds a character less than hex 40 (blank), it replaces that character with a hex FF so that the graphic error action previously set in the printer applies, provided hex FF has not been defined as a printable character by the load alternate characters (LAC) printer control code. This scan, compression, and replacement is done within the print buffer.

If the data is to be routed directly to the printer instead of being spooled, this instruction updates the forms length and current line fields of the associated printer unit block (PUB).

Input Parameters

Q-Byte: Not used; must be zero.

Index register 1: The address of the print input/output block (IOB).

Example

Program A wants to skip to line 1, print a line, and space one line after printing. The IOB address is hex 004540 and the print buffer is at hex 006000. The print buffer address must be real.

Program A moves the data to be printed to address hex 006006 and sets the following fields in the IOB:

- The flag byte ($IOBPFL0), to identify whether the output is to be spooled
- The address of the print buffer ($IOBPDAT)
- The length of the data in the print buffer ($IOBPLNG)
- The control byte ($IOBPCTL) to indicate a print operation
- The skip before printing ($IOBPSKB) and space after printing ($IOBPSPA) fields to 1
- The forms length ($IOBPFML)
- The printer unit block (PUB) address field ($IOBPPUB)
- The current line number ($IOBPCLN)

Program A also loads index register 1 with hex 004540, and then issues:

Assembler	**Object Code**	**Description**
SVC SVCPREP,00	F40026	Issue the SVC

The required control codes are inserted into the print buffer, the data is compressed, and $IOBPLNG is updated to reflect the number of characters in the print buffer. $IOBP#FF is set to the number of forms feed printer control codes that is inserted into the print buffer before the data is printed. $IOBP#AF contains the number of forms feed printer control codes inserted into the print buffer after the data to be printed. $IOBPCLN is updated to the new current line value, and control is returned to program A.

Prepare Print Buffer (Ideographic)

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	00	26

This is an overlapped and privileged SVC.

This instruction inserts printer control codes into the print buffer to cause the requested skip and space operations. It also maintains a record of the current logical line in the print input/output block (IOB).

This instruction scans the data to be printed. When scanning the data to be printed:

- If the 2-byte mode indicator ($IOBPCTL:$IOBP2BM) is on at the beginning of the scan, the begin scan of data in ideographic mode indicator ($IOBPCTL:$IOBP2BS) is set on.

- When the scan finds a character less than hex 40 that is neither a shift character (hex 0E for SO or hex 0F for SI) nor the point number of a 2-byte character, it replaces that character with hex FF. The effect of the replacement is that the printer processes the character on the basis of the previously set graphic error action, if hex FF has not been previously defined as a printable character by the Load Alternate Characters printer command.

- When an SO (hex 0E) control code is found, the 2-byte mode ($IOBCPTL:$IOBP2BM) indicator in the printer IOB is set on, if the System Support Program's Ideographic feature is installed. (See the SCAMKKKF indicator in the SCADSSPF field of the system communication area.) If the feature is not installed, or if the system is already in the 2-byte mode, the character is processed as a character less than hex 40.

- When an SI (hex 0F) control code is found, the 2-byte mode ($IOBPCTL:$IOBP2BM) indicator in the printer IOB is set off. If the 2-byte mode is not on, the character is processed as a character less the hex 40.

- When the 2-byte mode ($IOBPCTL:$IOBP2BM) indicator is on:

  - If the output is being sent directly to a printer that cannot print the data, the SO and SI control characters and the 2-byte character codes (both the ward and the point numbers) are set to blank.

  - If the output is being spooled or sent directly to a printer that can print the data, the 2-byte character code ($IOBPCTL:$IOBP2BC) indicator is set on; and if the ward number byte is equal to or greater than the lowest ward number of a character that requires extended character processing, the extended character processing required ($IOBPCTL:$IOBPRPR) indicator in the IOB is also set on, if the user has not disallowed this function by setting the ($IOBPCTL:$IOBPNRP) indicator.

- When the scan detects more than three contiguous blanks in a record, the blanks are compressed and replaced with relative horizontal presentation position SCS control code, if the blanks are not part of a SO/SI-enclosed character string in which the hex 40 (blank) substring is terminated by a point number that is not hex 40. Such a character is invalid and prevents the compression of any immediately preceding characters.

- When the scan finds valid blanks at the end of a record, it discards them.

Notes:

1. *The 5224 Model 12, the 5225 Model 11 or 12, 5553, and 5557 printers requires an even number of paired data bytes between the SO (hex 0E) and SI (hex 0F) SCS control characters to correctly print ideographic characters. The System/36 control storage program assumes that this requirement is met.*

2. *System/36 support of the 5224, 5225, 5553, and 5557 printers requires that the ward and the point numbers of an ideographic character be sent to the printer as part of one request.*

3. *If ideographic data that does not meet the preceding requirements is sent to the printer, the results are unpredictable.*

4. *If the output is spooled to a nonideographic printer, and the spool writer has determined that the spool file entry contains ideographic data, the spool writer issues a message 5833 with 0, 1, and 2 options. If you select the 0 option, this causes the output to be held on the spool file. If you select the 1 option, this processes the data as though it were being sent directly to a nonideographic printer. (SO, SI, and ideographic characters are set to blank.) If you select the 2 option, this causes the spool writer to stop.*

Input Parameters

Q-Byte: Not used; must be zero.

Index register 1: The address of the print input/output block (IOB).

Example

Program A wants to skip to line 1, print a line, and space one line after printing. The IOB address is hex 004540 and the print buffer is at hex 006000. The print buffer address must be real.

Program A moves the data to be printed to address hex 006006 and sets the following fields in the IOB:

- The flag byte ($IOBPFL0), to identify whether the output is to be spooled.

- The address of the print buffer ($IOBPDAT).

- The length of the data in the print buffer ($IOBPLNG).

- The printer unit block (PUB) address field ($IOBPPUB).

- The forms length ($IOBPFML).
- The current line number ($IOBPCLN).
- The control byte ($IOBPCTL) to indicate a print operation ($IOBPPRT), whether extended character processing is allowed ($IOBPNPR), and whether the printer is capable of printing 2-byte characters ($IOBP2BD).
- The skip before printing ($IOBPSKB) and space after printing ($IOBPSPA) fields to 1.

Program A also loads index register 1 with hex 004540, and then issues:

Assembler	Object Code	Description
SVC SVCPREP,00	F40026	Issue the SVC

The required control codes are inserted into the print buffer, the data is compressed, and $IOBPLNG is updated to reflect the number of characters in the print buffer. $IOBP#BF is set to the number of forms feed printer control codes that are inserted into the print buffer before the data is printed. $IOBP#AF contains the number of forms feed printer control codes inserted into the print buffer after the data to be printed. $IOBPCTL is updated to indicate that the data in the print buffer does or does not begin in 2-byte mode ($IOBP2BS), that any 2-byte characters do or do not require extended character processing ($IOBPRPR) to be printed, and that the print buffer does or does not contain any 2-byte characters ($IOBP2BC). $IOBPCLN is updated to the new current line value, and control is returned to program A.

Post Task by Task ID

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	**Byte 2**	**Byte 3**	**Byte 4**
F4	xx	2B	xx

This is an overlapped and privileged SVC.

This instruction assigns a 32-byte area to be used as an action control element (ACE). This ACE is queued to the completed event queue (TB__CMPLQ) of the TB whose ID is given in WR5. If the task ID is posting itself, the task ID in WR5 may be 0000. This ACE is initialized in the same manner as the action control element build and queue SVC (4C) and is used to post the specified task in the same manner as the post action control element SVC (19). Index register 1 is not required to contain the address of an event control mask (ECM). The TB being posted must issue a multiple event wait SVC (02, Q-Byte bit 4=1) or a specific event wait SVC (02, Q-Byte bit 4=1) when the post task by task ID SVC (2B) is issued. An event type must be given in WR6 if the Q-Byte bit 5=1.

Input Parameters

Q-Byte

Bit	**Meaning if On**
0-2	Not used; must be zero.
3	Command processor asynchronous wait.
4	This event is a multiple event wait candidate.
5	Event type given.
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program and the storage cannot be released.
7	Not used; must be zero.

Inline parameter 1

Bit	**Meaning**
1	Last-in-first-out (LIFO) queue action control element to complete queue of task being posted.
2-3	Not used; must be zero.

Index register 1: XR1 value.

Index register 2: XR2 value.

Work register 5: Task ID.

Work register 6: Event type if Q-Byte bit 5 = 1.

Program status register: Equal if given task ID is found. Not equal if given task ID is not found.

Example

Program A (task ID 13) wants to post program B (task ID 07). Program B issues a multiple event wait SVC when expecting to be posted from program A. To post, program A issues:

Assembler	**Object Code**	**Description**
LA X'0007',WR5	C2450007	
SVC SVCPOSTI,8	F4082B00	Issue the SVC
DC XL1'00'		

When program B issues the multiple event wait, the wait is satisfied and program B continues executing with XR1 equaling the value that program A had in XR1 when it posted program B. This value must have been agreed on between programs A and B. It can be any value and is not assumed to contain the address of an event control mask (ECM).

Translated Assign

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	xx	2C

This is an overlapped and privileged SVC.

This instruction assigns storage from a system work space (SWS), a task work space (TWS), or from a program. The amount of storage to assign and the address of the storage block or program block describing the area from which the storage is to be assigned must be given as input. Storage is assigned in 64 byte multiples on 64 byte boundaries. The length assigned must not be zero and not exceed FFC0 hex bytes.

The address of the assigned storage is returned as a virtual storage address. That storage must be mapped (see the MAP SVC) before it can be addressed. As an option, the storage may be mapped before it is assigned. If the storage is mapped before it is assigned the address of the assigned storage is returned as a translated address and may be addressed immediately.

Another option allows the caller to request that storage be assigned so that it requires the fewest possible pages of main storage to map to the assigned area.

Another option allows the storage to be assigned with or without wait. If wait is not specified, and there is not enough storage available, a low condition is set in the PSR to indicate that no space was assigned. If wait is specified, the task is put into a wait state until space becomes available or until the system has been able to enlarge the SWS/TWS enough to assign the requested space. However, if one of the following conditions occur the wait request is ignored and a low condition is returned in the PSR indicating that the space was not assigned:

- If the storage is to be assigned from a program
- If a mapped address is specified
- If the storage is from a TWS that has already reached its maximum size

All successful assigns return an equal condition in the PSR.

Input Parameters

Q-Byte

Bit	Meaning
0	Not used; must be zero.
1	Long wait; storage and programs are released immediately if a wait.
2	Assign the storage so that it requires the fewest possible main storage pages to map to it.
3-4	Not used; must be zero.
5	A mapped address is given in work register 7. The complete storage area from which space may be assigned must be able to be mapped at the specified address. The address of the space assigned is returned as a translated address, created by adding the virtual storage address of the area assigned to the specified mapped address. If the space is to be assigned from a program, this parameter is required and represents the address at the end of the program and the beginning of the area from which storage may be assigned.
6	Not used; must be zero.
7	Wait for space to become available if enough space is not available immediately.

Index register 1: Contains the address of the storage block used to describe the SWS/TWS from which space is to be assigned, or if space is to be assigned from a program, it contains the address of the program block.

Work register 6: Contains the length in bytes of the storage to assign.

Work register 7: Contains the address to which the storage is mapped if bit 5 of the Q-Byte = 1.

Output Parameters

Program status register: Set to equal if the storage was successfully assigned.

Set to low if the storage was not assigned.

Index register 1: Contains the address of the assigned storage. If bit 5 of the Q-Byte is zero, this is a virtual address. It is the displacement of the area assigned in the work space, with the high order bit on.

If bit 5 of the Q-Byte is one, this is a translated address (hex 80nnnn) created by adding the mapped address to the displacement of the assigned area.

Example

Program A has created a Task Work Space and now wants to assign a 256-byte element (without wait) from it. The address of the storage block was returned when the Task Work Space was created, and program A must now ensure that address is loaded into XR1, and then issue:

Assembler	Object Code	Description
L SB@,XR1		Load storage block address into XR1
LA 256,WR6	C2460100	
SVC SVCXASGN,00	F4002C	Issue the SVC

where SB@ contains the storage block address.

When the SVC instruction has been executed and has successfully assigned the requested storage, an equal condition is returned in the PSR, and XR1 contains the displacement of the assigned storage within the work space, with the high order bit on (for example, hex 800000).

Translated Free

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	xx	2D

This is an overlapped and privileged SVC.

This instruction frees storage previously assigned by the Translated Assign SVC from a System Work Space (SWS), a Task Work Space (TWS), or from a program. The freed storage is then available for following translated assigns. The amount of storage to be freed, the address of the storage to be freed, and the address of the storage block or program block describing the area from which the storage was previously assigned must be given as input.

If a mapped address was given when the storage was assigned, the same mapped address must also be given when the storage is freed.

Partial free areas of the originally assigned area may be requested if each area to free begins on a 64-byte boundary.

Input Parameters

Q-Byte

Bit	Meaning
0-4	Not used; must be zero.
5	The address to be freed is a translated (instead of a virtual) address. The mapped address is given in work register 7.
6-7	Not used; must be zero.

Index register 1: The address of the area to free. This may be a translated address or a virtual address according to the setting of bit 5 of the Q-Byte.

Index register 2: The address of the storage block or program block from which the area to be freed was assigned.

Work register 6: The length of the storage to free (in bytes).

Work register 7: The mapped address if the area to be freed is mapped (see bit 5 of the Q-Byte).

Example

Program A wants to free a previously assigned element. The virtual address of the element (for example hex 800000 is loaded into Index Register one, and the address of the storage block for the task work space is loaded into index register two). The length of the element to be freed (256-bytes) is loaded into work register six and the translated free SVC is issued as follows:

Assembler	Object Code	Description
L @TOFREE,XR1		Load the TOFREE address into XR1
LA 256,WR6	C2460100	
SVC SVCXFREE,00	F4002D	Issue the SVC

where @TOFREE contains the address of the area to be freed.

Time of Day

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	00	2E

This is an overlapped and privileged SVC.

This function returns the current time of day in timer units. The value is passed back in index register 1 and index register 2.

Note: *Because index register 1 and index register 2 are used, the information that was in these registers is destroyed.*

Input Parameters

Q-Byte: Not used; must be zero.

Example:

Program A needs the time of day. Program A issues:

Assembler	Object Code	Description
SVC SVCTOD,00	F4002E	Issue the SVC

MAP

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	2F

This is an overlapped and privileged SVC.

This instruction establishes translated addressability to system work spaces, task work spaces, and other programs. The caller describes the data to be mapped and the logical address within the region to where it should be mapped, via the map parameter list. Refer to the *System Data Areas* manual for a parameter list description. The SVC builds one or more map table entries and puts the entries into the map table in the request block.

Input Parameters

Q-Byte

Bit	Meaning
0	Not used; must be zero.
1	Long wait; storage and programs are released immediately if a wait.
2-7	Not used; must be zero.

Index register 1: A logical or virtual address of the data to be mapped if USING-XR1 is indicated in the parameter list. The length of the data if LNGTH-XR1 is indicated in the parameter list. Refer to the *System Data Areas* manual for a parameter list description.

Index register 2: Points at the left most byte of the parameter list. Refer to the *System Data Areas* manual for a parameters list description.

Work register 4: A logical or virtual address of the data to be mapped if USING-WR4 is indicated in the parameter list. The length of the data if LNGTH-WR4 is indicated in the parameter list. Refer to the *System Data Areas* manual for a parameter list description

Work register 5: A logical or virtual address of the data to be mapped if USING-WR5 is indicated in the parameter list. The length of the data if LNGTH-WR5 is indicated in the parameter list. Refer to the *System Data Areas* manual for a parameter list description

Work register 6: A logical or virtual address of the data to be mapped if USING-WR6 is indicated in the parameter list. The length of the data if LNGTH-WR6 is indicated in the parameter list. Refer to the *System Data Areas* manual for a parameter list description

Work register 7: A logical or virtual address of the data to be mapped if USING-WR7 is indicated in the parameter list. The length of the data if LNGTH-WR7 is indicated in the parameter list. Refer to the *System Data Areas* manual for a parameter list description

Output Registers

Index register 1: The mapper's logical address of the data that was mapped if USING-XR1 was indicated in the parameter list.

Work register 4: The mapper's logical address of the data that was mapped if USING-WR4 was indicated in the parameter list.

Work register 5: The mapper's logical address of the data that was mapped if USING-WR5 was indicated in the parameter list.

Work register 6: The mapper's logical address of the data that was mapped if USING-WR6 was indicated in the parameter list.

Work register 7: The mapper's logical address of the data that was mapped if USING-WR7 was indicated in the parameter list.

Example

Assembler	Object Code	Description
LA X'2080',XR2	C2A22080	Load parameter list address
SVC SVCMAP,00	F4002F	Issue SVC

Parameter List

Assuming XR1 contains hex 800000 and location hex 802080 contains (the parameter list) hex 5148010800810000 then the SVC maps the first page (virtual page 0) of the task work space type (hex 81) to logical address hex 5000. At the end of the SVC, XR1 contains hex 805000 and the program is able to address data from hex 5000 through hex 57FF.

QLOCK

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	00	30

This is an overlapped and privileged SVC.

This instruction scans the system priority queue for the highest priority task waiting for the qlock being released. The address of the qlock is passed in WR6. The highest priority task is then posted to own the released qlock.

Input Parameters

Q-Byte: Not used; must be zero.

Work register 6: The address of the qlock.

Example

Assembler	Object Code	Description
LA 256,70	C2460100	Load QLOCK value into WR6
SVC SVCQLOCK,00	F4002D	Issue SVC

ATASK

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	31

This is an overlapped and privileged SVC.

This instruction assigns and formats a program block in the system queue space, and allocates a swap area in the task work area. A task work area allocate failure results in a return to the caller with the PSR set to high. Otherwise, the PSR is returned set to equal.

Input Parameters

Q-Byte

Bit	Meaning
0-2	Not used; must be zero.
3	Allocate maximum swap area.
4-7	Not used; must be zero.

Work register 6: Must contain the region size in the high byte and the main storage size in the low byte.

Output Registers

Index register 1: Program block address.

Example

The main store attachment program wants to create a program block for the task being attached. It loads the region and main storage size into work station register 6 then issues the SVC. After the SVC completes, index register 1 contains the address of the program block that was built.

Assembler	Object Code	Description
L JCB@,XR2		Load JCB address
L JCBDRGSZ(XR2),WR6		Load region and main storage size
SVC SVCAT,00	F40031	Issue SVC

where JCB@ contains the job control block address.

DTASK

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	00xx	32

This is an overlapped and privileged SVC.

This instruction is issued whenever there has been a failure to attach a task and the ATASK is already completed. It is issued to purge the program block. This instruction dequeues and frees the program block and deallocates any associated swap area in the task work area. Any main storage allocated is freed and queued to the free page storage block.

Input Parameters

Q-Byte: Not used; must be zero.

Index register 1: Program block address.

Example

The main store detach program is ready to purge a program block. It loads the program block address into XR1 and issues the SVC. At the completion of the SVC the program block has been dequeued and freed along with all main storage and swap area associated with that program.

Assembler	Object Code	Description
L PB@,XR1		Load the program block address
SVC SVCDT,00	F40032	Issue SVC

where PB@ contains the program block address.

TWAL

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	33

This is an overlapped and privileged SVC.

This instruction allocates a task work area. The value returned in XR2 is a relative disk address and not an actual disk address. A variable size area on the disk (in one sector portions) can be allocated rather than just one track. The default value is 60 sectors.

Input Parameters

Q-Byte

Bit	Meaning
0	Not used; must be zero.
1	Long wait; storage and programs are released immediately if a wait.
2-6	Not used; must be zero.
7	The task will wait for a task work area to be freed if a task work area is not available.

Work register 6: Contains the number of sectors of the task work area to assign.

Output Registers

Index register 2: Relative disk address. This is a one byte base identifier and a two byte sector displacement address if the task work area was assigned to the requester.

Program status register: Is equal if the task work area was assigned to the requester. Is high if the task work area was not available.

Example

The program allocates a 256-sector task work area.

Assembler	Object Code	Description
LA 256,WR6	C2460100	Load the number of sectors needed
SVC SVCTWAL,0	F40033	Issue the SVC

DTWAL

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	34

This is an overlapped and privileged SVC.

This instruction frees the task work area specified by the calling task.

Input Parameters

Q-Byte: Not used; must be zero.

Index register 2: Contains the relative disk address of the area to be freed.

Work register 6: Contains the number of sectors to be freed.

Example

This program frees 256 bytes of task work area.

Assembler	Object Code	Description
LA 256,WR6	C2460100	Load the number of sectors to free
SVC SVCDTWAL,00	F40034	Issue the SVC

WRK

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	35

This is an overlapped and privileged SVC.

This instruction provides work space maintenance. A work space can be created or freed for the system or for a task. The type of operation (creation or deletion) and the description of the work space (system or task work space, size of work space, and other factors) is contained in the WRK parameter list. Refer to the *System Data Areas* manual for the parameter list description. The SVC supports the following three functions:

1. Conditional creation: A new work space is created if one of the same type does not exist.

2. Unconditional creation: A new work space is always created.

3. Deletion: An existing work space is deleted.

For creation the WRK SVC assigns and builds a storage block to describe the work space and allocates a swap area on disk from the task work area. Before the work space can be addressed some area must be assigned (XASGN) and mapped (MAP). For deletion the SVC frees the swap area, storage block, and any main storage associated with the area.

Note: If the work space is still in use, then it is marked for deletion and then deleted when there are no other users. A storage block marked for deletion cannot be mapped by new users.

Input Parameters

Q-Byte

Bit	Meaning
0	Not used; must be zero.
1	Long wait; storage and programs are released immediately if a wait.
2-6	Not used; must be zero.
7	The task waits for work space to be allocated if the swap area is not available.

Index register 1: Contains the address of the parameter list.

Output Registers

Index register 1: Contains the address of the storage block found, assigned or deleted.

Program status register: Contains the status of the completed WRK command.

Command Type	Status	Description
Conditional	Equal	Work space created
Conditional	High	Work space already existed or task ID specified but not found
Conditional	Low	TWA allocate failure
Unconditional	Equal	Work space created
Unconditional	High	Task ID specified but not found
Unconditional	Low	TWA allocate failure
Delete	Equal	Work space deleted
Delete	High	Task ID specified but not found
Delete	Low	No work space found to delete

Example

Assembler	Object Code	Description
LA PARML,XR1	C2A15000	Load the parameter list address
SVC SVCWRK,00	F40035	Issue the SVC

where PARML is the address of the parameter list.

Parameter List

```
           0 1 2 3 4 5 6 7 8 9 A B
805000 = 028100100000000200000000
```

Issuing this SVC unconditionally creates a 2 page (4096 byte) task work space for the task with a task ID of hex 0002. The storage block address is returned in index register one.

SMFC

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	36

This is an overlapped and privileged SVC.

This instruction is used by BSC communications interrupt handler to indicate to the SMF communications microcode that an error has occurred on the communications line. SMF communications microcode is then able to collect the needed information about the state of the communications line.

Input Parameters

Q-Byte

Bit	Meaning
0-1	Not used; must be zero.
2	If on, it equals receive error. If off, it equals transmit error.
3-7	Not used; must be zero.

Index register 1: Input/output block.

Fixed Disk IOS

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	40

This is a delayed and privileged SVC. However, read operations will be regarded as an immediate SVC if the disk cache is active and the data to be read is found in the cache.

Index register 1 must point to the input/output block (IOB), which is defined in the *System Data Areas* manual.

Input Parameters

Q-Byte

Bit	Meaning if On
1	Long wait (storage released immediately).
2	Bypass disk cache if it is active.
3	Different task posted on completion (TB address in XR2).
4	Satisfies multiple wait.
5	Event type given in WR6 (if bit 5 is off the default event type is used).
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program, and its storage cannot be released.
7	Wait on this event.

Index register 1: Input/output block (IOB) address.

Note: *If the IOB address (in XR1) is translated, then the IOB cannot be posted with the event post SVC (R-Byte 03) and cannot be waited for more than once with the event wait SVC (R-Byte 02).*

Index register 2: Other TB address if Q bit 3 is on.

Work register 6: Event type if Q bit 5 is on. If Q bit 5 is off the system uses the default event type. Refer to EVTYP in the *System Data Areas* manual.

Diskette IOS

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	xx	41

This is a delayed and privileged SVC.

Index register 1 points to the input/output block (IOB), which is defined in the *System Data Areas* manual.

Input Parameters

Q-Byte

Bit	Meaning if On
1	Long wait (storage released immediately).
3	Different task posted on completion (TB address in XR2).
4	Satisfies multiple wait.
5	Event type given in WR6 (if bit 5 is off the default event type is used).
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program and its storage cannot be released.
7	Wait on this event.

Index register 1: Input/output block (IOB) address.

Note: If the IOB address (in XR1) is translated, then the IOB cannot be posted with the event post SVC (R-Byte 03) and cannot be waited for more than once with the event wait SVC (R-Byte 02).

Index register 2: Other TB address if Q bit 3 is on.

Work register 6: Event type if Q bit 5 is on. If Q bit 5 is off the system uses the default event type. Refer to EVTYP in the *System Data Areas* manual.

Work Station/Printer IOCH

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	42

This is a delayed and privileged SVC for printer requests.

Index register 1 points to the input/output block (IOB), which is defined in the *System Data Areas* manual.

Input Parameters

Q-Byte

Bit	Meaning if On
1	Long wait (storage released immediately).
3	Different task posted on completion (TB address in XR2).
4	Satisfies multiple wait.
5	Event type given in WR6 (if bit 5 is off the default event type is used).
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program and its storage cannot be released.
7	Wait on this event.

Index register 1: Input/output block (IOB) address.

Note: The IOB address (in XR1) must be real.

XR2 register: Other TB address if Q bit 3 is on.

Work register 6: Event type if Q bit 5 is on. If Q bit 5 is off the system uses the default event type. Refer to EVTYP in the *System Data Areas* manual.

Work Station IOCH

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	43

This is a delayed and privileged SVC for display station requests.

Index register 1 must point to the input/output block (IOB), which is defined in the *System Data Areas* manual.

Input Parameters

Q-Byte

Bit	Meaning if On
0	Not used.

1	Long wait (storage released immediately).
3	Different task posted on completion (TB address in XR2).
4	Satisfies multiple wait.
5	Event type given in WR6 (if bit 5 is off the default event type is used).
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program and its storage cannot be released.
7	Wait on this event.

Index register 1: Input/output block (IOB) address.

Note: The IOB address (in XR1) must be real.

XR2 register: Other TB address if Q bit 3 is on.

Work register 6: Event type if Q bit 5 is on. If Q bit 5 is off the system uses the default event type. Refer to EVTYP in the *System Data Areas* manual.

Data Communications IOCH

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	xx	44

This is a delayed and privileged SVC.

Index register 1 points to the input/output block (IOB), which is defined in the *System Data Areas* manual.

Input Parameters

Q-Byte

Bit	**Meaning if On**
1	Long wait (storage released immediately).
3	Different task posted on completion (TB address in XR2).
4	Satisfies multiple wait.

5	Event type given in WR6 (if bit 5 is off the default event type is used).
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program and its storage cannot be released.
7	Wait on this event.

Index register 1: Input/output block (IOB) address.

Note: The IOB address (in XR1) must be real.

XR2 register: Other TB address if Q bit 3 is on.

Work register 6: Event type if Q bit 5 is on. If Q bit 5 is off the system uses the default event type. Refer to EVTYP in the *System Data Areas* manual.

Local Area Network IOCH

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	xx	49

This is a delayed and privileged SVC.

Index register 1 points to the input/output block (IOB), which is defined in the *System Data Areas* manual.

Input Parameters

Q-Byte

Bit	Meaning if On
1	Long wait (storage released immediately).
3	Different task posted on completion (TB address in XR2).
4	Satisfies multiple wait.
5	Event type given in WR6 (if bit 5 is off, default event type is used).

6 Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program and its storage cannot be released.

7 Wait on this event.

Index register 1: IOB address.

Note: The IOB address (in XR1) must be real.

XR2 register: Other TB address if Q bit 3 is on.

Work register 6: Event type if Q bit 5 is on. If Q bit 5 is off, the system uses the default event type. Refer to EVTYP in the *System Data Areas* manual.

Diskette Data Compression

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	01	45

This is a delayed and privileged SVC.

Index register 1 points to the input/output block (IOB), which is defined in the *System Data Areas* manual.

Input Parameters

Index register 1: Input/output block (IOB) address.

Notes:

1. *The IOB address (in XR1) is real.*

2. *Index register 1 points to a diskette IOB. The chain field in the diskette IOB points to a disk IOB. The IOB address in the chain field is real.*

Tape IOS

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	46

This is a delayed and privileged SVC.

Index register 1 points to the input/output block (IOB), which is defined in the *System Data Areas* manual.

Input Parameters

Q-Byte

Bit	Meaning if On
1	Long wait (storage released immediately).
3	Different task posted on completion (TB address in XR2).
4	Satisfies multiple wait.
5	Event type given in WR6 (if bit 5 is off the default event type is used).
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program and its storage cannot be released.
7	Wait on this event.

Index register 1: Input/output block (IOB) address, which must be a real address.

Index register 2: Other TB address if Q bit 3 is on.

Work register 6: Event type if Q bit 5 is on. If Q bit 5 is off, no event type is assigned (event type zero is used). Refer to EVTYP in the *System Data Areas* manual.

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1255 Magnetic Character Reader IOS

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	Byte 2	Byte 3
F4	xx	47

This is a delayed and privileged SVC.

Index register 1 points to the input/output block (IOB), which is defined in the *System Data Areas* manual.

Input Parameters

Q-Byte

Bit	Meaning if On
1	Long wait (storage released immediately).
3	Different task posted on completion (TB address in XR2).
4	Satisfies multiple wait.
5	Event type given in WR6 (if bit 5 is off, the default event type is used).
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program, and its storage cannot be released.
7	Wait on this event.

Index register 1: Input/output block (IOB) address, which must be a real address.

Index register 2: Other TB address if Q bit 3 is on.

Work register 6: Event type if Q bit 5 is on. If Q bit 5 is off, the system uses no event type (zero). Refer to EVTYP in the *System Data Areas* manual.

DSC I/O

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)
Byte 1	**Byte 2**	**Byte 3**
F4	xx	48

This is a delayed and privileged SVC.

This SVC starts or stops SMF in the data storage controller, reads the SMF counters from the data storage controller into main storage, and sends information to the data storage controller during an initial program load.

Input Parameters

Q-Byte

Bit	Meaning if On
1	Long wait (storage released immediately).
3	Different task posted on completion (TB address in XR2).
4	Satisfies multiple wait.
5	Event type given in WR6 (if bit 5 is off no event type is used).
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program, and its storage cannot be released.
7	Wait on this event.

Index register 1: Address of the DSC IOB. The IOB must be in real main storage.

Index register 2: Other TB address if Q bit 3 is on.

Work register 6: Event type if Q bit 5 is on. If Q bit 5 is off no event type is assigned (event type zero is used). Refer to EVTYP in the *System Data Areas* manual.

Action Control Element Build and Queue

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	Byte 2	Byte 3	Byte 4
F4	xx	4C	xx

This is an overlapped and privileged SVC.

The action control element build and queue supervisor call instruction assigns a 32-byte area to be used for the action control element. This action control element is then queued to the passed system queue header (a first-in-first-out queue). The action control element is initialized with the current values of the task. The values in XR1 and XR2 are saved in the ACE. When the ACE address is requested, the ACE address is stored in the event control mask which is addressed by XR1 and returned in XR2.

Input Parameters

Q-Byte

Bit	Meaning if On
0-1, 7	Not used.
2	Store the ACE address in the event control mask addressed by XR1 and return the ACE address in XR2.
3	Put different TB address in ACE (TB address in XR2).
4	This event satisfies a multiple wait.
5	Event type given in WR6.
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program, and its storage cannot be released.

Inline parameter 1: System queue header number.

Index Register 1: If the Q-Byte bit 2 is on, XR1 must contain the event control mask address. The address must be real. The ACE address is stored in the event control mask. Refer to the *System Data Areas* manual for the location of the ACE address in the event control mask.

Index register 2: Other TB address if Q-bit 3 is on,

Work register 6: Event type if the Q-Byte bit 5 is on. Refer to "EVTYP" section of the *System Data Areas* manual for the event types.

Output Values

Index register 2: Address of the action control element if requested in input (Q bit 2).

Program A wants to create an action control element and have it queued to the system queue header number 48. The address of the action control element is requested.

```
Assembler           Object Code      Description

SVC SVCPQSVC,00     F40004C49        Issue the SVC
DC XL1'48'
```

With index register 2 containing hex 000000 and address 000148 containing hex 000000.

After execution of the supervisor call, an action control element is built at location 003470, for example. Location 0148 is set to 003470 and index register 2 is returned, also containing address 003470.

Control Storage Transient Scheduler

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)		
Byte 1	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**
F4	xx	50	xx	xx	xx

This is a delayed SVC.

This supervisor call is privileged except when a transient ID of hex 0A (timer) is specified in inline parameter 1.

This instruction loads control storage transients. The control storage transient to be loaded is identified by a 1-byte transient number given as inline parameter 1 (byte 4). If the transient area is not busy, the requested transient is loaded into the transient area and control is passed to the transient. If the transient area is busy the request is queued and handled when the transient area is not busy.

Control is returned to the caller after the transient has executed completely.

Input Parameters

Q-Byte: Dependent on transient requested.

Inline parameter 1: Control storage transient identification. Refer to the *System Data Areas* manual for the transient identification.

Inline parameters 2 and 3: Input to the transient.

Example

Program A wants to call a control storage transient to get the time of day. The transient ID is hex 0A and the input to this transient requires hex 40 in inline parameter 2 and index register 2 must contain the address of a 14-byte timer request block (TRB).

Assembler	Object Code	Description
LA @TRB,XR2		Loads the TRB address into the XR2 register
SVC SVCCXNT,00	F400500A4000	Issue the SVC
DC XL’0A’		
DC XL2’4000’		

where @TRB is the address of the TRB.

When the supervisor call completes, the timer request block contains the current time and date.

Task Work Area Accesses

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)		
Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
F4	xx	51	xx	xx	xx

This is a delayed and privileged SVC. However, read operations will be regarded as an immediate SVC if the disk cache is active and the data to be read is found in the cache.

This instruction is used to access the task work area or the other areas on the disk. The disk area address passed may be a relative disk address, such as a swap area address or a sequential sector address. Task work area access supports keyed variable length access where the key is an offset to the sector to be accessed. Task work area accesses SVC also supports indirect addressing of the disk area address using index register 1.

Input Parameters

Q-Byte

Bit	Meaning if On
0-1	Not used; must be zero.
2	Bypass disk cache if it is active.

3-5	Not used; must be zero.
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program and its storage cannot be released.
7	Not used; must be zero.

Inline parameter 1: Type Byte (get/put).

Bit	**Meaning if On**
0-3	Not used; must be zero.
4	(If = 0) disk address in XR1. (If = 1) indirect main storage address is passed in XR1 (bit 5 must be 0).
5	(If = 0) disk address in XR1. (If = 1) disk address in JCBWSWA (refer to JCBEQ in the *System Data Areas* manual).
6	(If = 0) disk address is sequential sector address. (If = 1) disk address is relative sector address.
7	(If = 0) get. (If = 1) put.

Inline parameter 2: Key (0-255).

Inline parameter 3: Number of disk sectors (0-255).

Index register 1: Disk area address or indirect main storage address of the disk address. Indirect address must be a real address.

Index register 2: Main storage address of data.

Example

Program A, a translated program, wants to read from the work station work area. The relative address in the JCBWSWA is 000100. Program A wants to read 4 sectors at offset 8 from the task work area. The data address in main storage is hex 802000.

Assembler	**Object Code**	**Description**
LA X'2000',XR2	C2A22000	Load the data address
SVC SVCTWA,00	F40051060804	Issue the SVC
DC XL1'06'		
DC XL1'08'		
DC XL1'04'		

The data located at relative disk address 000100 through 000103 is read into translated storage at locations hex 802000 through 8023FF.

Main Storage Relocating Loader

Op Code (Hex)	Q-Byte (Hex)	R-Byte (Hex)	Inline Parameter List (Hex)
Byte 1	Byte 2	Byte 3	Byte 4
F4	xx	52	xx

This is a delayed and not privileged SVC.

This instruction uses a relocating loader parameter list pointed to by index register 2. It determines the type of request and takes the necessary action as given by inline parameter 1 (byte 4). If relocation is required, the relocation transient is called to perform the relocation after the module has been read into storage.

Input Parameters

Q-Byte

Bit	Meaning if On
0-5	Not used; must be zero.
6	Reusable program is not refreshable. This bit only applies to reusable programs. No other task can own this reusable program and the storage cannot be released.
7	Not used; must be zero.

Inline parameters:

Hex Value	Type of Request
01	Load by relative address: Adds the task loader disk address, stored in the TB on previous loads, to the relative address passed in the user's parameter list. The resulting address is the location of the desired module, and control returns to the calling program.
02	Load to address: Reads the module into storage and returns control to the calling program.
04	Fetch: Adds the task relocation factor to the module's link-edit address and, using the resulting value as the load address, reads the module into storage and passes control to the module's start control address.
06	Fetch to address: Reads the module into storage and passes control to the module's start control address.

0A System load to address: Updates the task relocation factor and disk address values (in the tasks task block) from the loader's parameter list. Reads the module into storage and returns control to the calling program.

0E System fetch to address: Updates the task relocation factor and disk address values (in the tasks task block) from the loader's parameter list. Reads the module into storage and passes control to the module's start control address.

11 Load a memory resident overlay by relative address: Adds the task loader disk address (stored in the task block) to the relative address passed in the user's parameter list. The resulting address is the location of the desired overlay. The overlay is loaded or mapped to by the calling program. Control is returned to the calling program.

Index register 2: Relocating loader parameter list. (See the *System Data Areas* manual for these parameters.)

Example

Program A loads a subroutine from disk into main storage. The sequential sector address of the module is 010342. The parameter list built by program A is:

```
010342000F00200000200000000F002000
```

The loader supervisor call issued is:

Assembler	Object Code	Description
LA @PL,XR2		Load the parameter list
SVC SVCLOAD,00	F4005202	Issue the SVC
DC XL1'02'		

where @PL is the address of the parameter list.

Program A has control returned when the subroutine is loaded at main storage locations 002000 through 002FFF.

Relocation of the subroutine is not necessary since the load address and link address of the subroutine are identical.

Chapter 4. Programming Considerations

Conditioning the Program Status Registers

Machine Instruction	Condition	Binary Overflow	Test False	Decimal Overflow	High	Low	Equal
Zero and add zoned decimal	Set				Operand 2 positive	Operand 2 negative	Operand 2 zero
Zero and add zoned decimal	Reset				Operand 2 negative or zero	Operand 2 positive or zero	Operand 2 not zero
Add and subtrack zoned decimal	Set			Result overflow	Result postive	Result negative	Result zero
Add and subtract zoned decimal	Reset				Result negative or zero	Result positive or zero	Result not zero
Edit	Set				Operand 2 positive	Operand 2 negative	Operand 2 zero
Edit	Reset				Operand 2 not positive	Operand 2 not negative	Operand 2 not zero
Compare logical characters	Set				Operand 1 greater than operand 2	Operand 1 less than operand 2	Operand 1 equal to operand 2
Compare logical characters	Reset				Operand 1 not greater than operand 2	Operand 1 not less than operand 2	Operands not equal

Machine Instruction	Condition	Binary Overflow	Test False	Decimal Overflow	High	Low	Equal
Subtract logical immediate and compare logical immediate	Set				Operand 1 greater than immediate data	Operand 1 less than immediate data	Operand 1 equal to immediate data
Subtract logical immediate and compare logical immediate	Reset				Operand 1 not greater than immediate data	Operand 1 not less than immediate data	Operand 1 not equal to immediate data
Add logical characters	Set	Carry out			Carry out and result not zero	No carry and result not zero	Result zero
Add logical characters	Reset	Reset at start of instruction			No carry or result zero	Carry out or result zero	Result not zero
Subtract logical characters or subtracts from registers	Set				Operand 1 greater than operand 2	Operand 1 less than operand 2	Result zero
Subtract logical characters or subtracts from registers	Reset				Operand 1 not greater than operand 2	Operand 1 not less than operand 2	Result not zero
Add to register	Set	Carry out			Carry out and result not zero	No carry and result not zero	Result zero
Add to register	Reset	Start of instruction			No carry or result zero	Carry out or result zero	Result not zero
Test bits on			Tested bit not all ones				

Machine Instruction	Condition	Binary Overflow	Test False	Decimal Overflow	High	Low	Equal
Tested bits off			Tested bits not all zeros				
Branch or jump on	Set						
Branch or jump on	Reset		Reset if tested	Reset if tested			
Load register (PSR)	Set	Set if loaded bit 10 on	Set if loaded bit 11 on	Set if loaded bit 12 on	Set if loaded bit 15 off and bit 14 off	Set if loaded bit 15 off and bit 14 on	Set if loaded bit 15 on
Load register (PSR)	Reset	Reset if loaded bit 10 off	Reset if loaded bit 11 off	Reset if loaded bit 12 off	Reset if bit 15 on, or bit 15 off, and bit 14 on	Reset if bit 15 on, or bit 15 off and bit 14 off	Reset if loaded bit 15 off
System reset	Set						Equal set on
System reset	Reset	Binary overflow reset	Test reset	Decimal overflow reset	High reset	Low reset	
Shift right character	Set	Any ones shifted out			Result off	Result even and not zero	Result zero
Shift right character	Reset	No ones shifted out			Result not odd	Result not even or result zero	Result not zero

Note: The program status byte setting for EDIT will be shown only if one of the following conditions is true:

- *The program status byte bit 7 is set before the EDIT is executed.*
- *The rightmost byte of operand 1 is hex 20.*
- *Operand 2 is not zero.*

Chapter 5. Printers

Printers Used

The systems can use any of the following printers, except as noted:

- Native attached printer: IBM 3262 Printer Model B1 (5360 System Unit only).

- Local attached printers:

  IBM 3812 Printer
  IBM 4210 Printer
  IBM 4214 Printer (Model 2)
  IBM 4224 Printer (Models 101, 102, 1E2, 1C2)
  IBM 4234 Printer (Model 2)
  IBM 4245 Printer (Models T12 and T20)
  IBM 5219 Printer (Models D01 and D02)
  IBM 5224 Printer (Models 1, 2, and 12)
  IBM 5225 Printer (Models 1, 2, 3, 4, 11, and 12)
  IBM 5256 Printer (Models 1, 2, and 3)
  IBM 5262 Printer (Model 1)
  IBM 5553 Printer (Model B01) (ideographic)
  IBM 5557 Printer (Model B01) (ideographic)

- 3270 Remote Attachment printers:

  The following printers can be attached to a 3274 controller Model 61C, 51C, 41C, 31C, 21C, or 1C.

  IBM 3268 Printer (all models)
  IBM 3287 Printer (Models 1, 1C, 2, and 2C)
  IBM 3289 Printer (all models)

Notes:

1. *The 3262 Printer is a native attachment (to the 5360 System Unit only). The printer is attached directly to the system and is not part of a work station network.*

2. *The 5219, 5224, 5225, 5256, and 5262 Printers can be attached as remote work stations through the 5294 Remote Control Unit or through a remote 5251 (Model 12) Display Station which contains a controller.*

3. *The 3812, 4210, 4214, 4224, 4234, 5553, and 5557 Printers can be attached as remote work stations only by using the 5294 Remote Control Unit. The 5553 and 5557 Printers must be attached to the 5294 Remote Control Unit through a 5555 Display.*

4. *When the 5553 or 5557 is used as a local work station, it must be attached through a 5555 Display.*

The printer functions and their programming characteristics are described in this chapter.

Physical Characteristics

3262 Printer (5360 System Unit Only)

The 3262 Printer has a normal print rate of 650 lines per minute. This rate was measured using a 48-character set belt while printing 132 positions to a line with single-line spacing at 6 lines per inch. Other characteristics of this printer are:

- 132 print positions per line.

- 6 or 8 lines per inch, switch selected.

- 10 characters per inch pitch.

- Forms width: 3.5 inches to 16 inches.

- Forms length: 3 inches to 14 inches.

  Note: Stacking problems may occur on forms less than 6 inches long.

- Character sets of 48, 64, 96, or 128 characters; or the 188-character multinational character set.

- Special character-set belts with restricted character sets to increase the rate of handling data.

- Supports character translation. For example, if the printer belt does not have lower case, a translation table can be used to cause printing in upper case.

3812 Printer

The 3812 Printer is a nonimpact, electrophotographic desk-top printer and has a maximum print rate of 12 pages per minute. Other characteristics of the 3812 Printer are:

- 10, 12, or 15 characters per inch and proportional spacing.
- Letter quality print.
- 240 x 240 PEL density.
- All points addressable.
- 62 standard fonts including proportionally spaced and typographical fonts.
- 0, 90, 180, and 270 degree page rotation.
- Forms width: 7.2 inches to 8.5 inches.
- Forms length: 10.1 inches to 14 inches.

4210 Printer

The 4210 Printer is a low function/low cost/low usage wire matrix printer. It is the 420L (IBM Proprinter XL) printer with an integrated protocol converter providing the interface to the IBM System/36. It also has a redesigned operator panel to provide the indicators, keys, and functions familiar in the System/36 environment.

Other features are:

- Paper handling capabilities
  - 15-inch-wide continuous forms (Pinfeed)
  - A4 size cut sheet (Function feed)
  - Multi-part forms
  - Paper movement of 1/72-inch
  - Maximum forms length of 255 inches
- Print options
  - 5, 10, 12, and 17.1 cpi
  - Double high/double wide printing
  - Emphasized printing
  - Proportional speed printing

- Print qualities
  - Data Processing (DP)
  - Near Letter Quality (NLQ)
- Printer characteristics
  - Paper-load assist
  - 12 x 9 print cell
  - 13.2-inch print line
  - 4 million-character-average ribbon life
  - 10.2 million characters per year average usage
  - 51 million-character print head
- Print speed
  -

Mode	**Max. Burst Speed (CPs)**
DP 10 or 12 cpi	200
17.1 cpi	171.25
Emphasized 10 or 12 cpi	100
NLQ 10 or 12 cpi	40
Double wide 10 or 12 cpi	100
Double wide 17.1 cpi	85.6
Double high	8.7
Double high/Double wide	9.1

4214 Printer

The 4214 Printer is a stand-alone, 9-wire, serial matrix printer.

The 4214 Printer has print rates of 50 and 200 characters per second. When any of the characters are all points addressable (APA), the printing slows to 78 characters per second print rate. The printer uses a 9-high, 7-wide print matrix to produce the printed character. Near letter quality printing is produced by printing the line twice with a small horizontal offset for the second printing.

4214 Model Number	Characters Per Inch	Characters Per Second Print Speed
2	10	50 or 200
2	15	50 or 200

Note: The speed does not vary with the character set.

Other characteristics of the 4214 Printer are:

- The lines per inch and characters per inch pitch can be set by program control, which overrides the operator panel switch setting.
- 10 or 15 characters per inch.
- Forms width (continuous forms): 5 inches to 14.88 inches.
- Forms length (continuous forms): 3 inches to 14 inches.
- Forms width (manual sheet feed): 5 inches to 12 inches.
- Forms length (manual sheet feed): 3.5 inches to 14 inches.
- Character set of 188 characters.

Note: A remotely attached 4214 Printer might not operate at rated speed because of communications line speed.

4224 Printer

The 4224 printer is a serial wire matrix impact printer that supports the intelligent printer data stream (IPDS).

Draft quality (DP) printing on the 4224 Printer is provided using a 9-high, 10-wide character box. This printer also provides data-processing quality (DPTEXT) printing by doubling the horizontal dots and using a 9-high, 20-wide character box. Near-letter quality (NLQ) printing is provided by doubling both the vertical and horizontal dots and using an 18-high, 20-wide character box.

The maximum print rate is 200 characters per second for the 4224 Model 101 Printer and 400 characters per second for the 4224 Model 102, 1E2, and 1C2 Printers. The following table shows the character per second print speed for the different models and quality of printing:

Model Number	Draft Quality	Data-Processing Quality	Near-Letter Quality
101	200	100	50
102, 1E2, and 1C2	400	200	100

Note: A remotely attached 4224 Printer might not operate at rated speed because of the communications line speed.

Other characteristics of the 4224 Printer are:

- 198 print positions per line (at 15 characters per inch)
- The lines per inch spacing is set in 1/72-inch increments by program control.
- 10, 12, or 15 characters per inch and proportional spacing.
- The characters per inch is set by program control or at the operator panel.
- A good print quality is maintained on up to four-part forms.
- Forms width: 3 inches to 16.2 inches.
- Forms length: 3 inches to 14.2 inches.
- Forms feed by continuous tractor feed.

- Forms feed using a bidirectional forms feed with document on demand forms separator.

- Audible alarm that alerts the operator that there is an error condition, that there is an end of paper feed, or that the Forms key or Stop key is pressed. The alarm sound can be stopped by pressing the Stop key.

4234 Printer

The 4234 Printer is a dot band impact matrix printer.

The 4234 Printer has a normal print rate of 300 lines per minute at 6 lines per inch, with 10 characters per inch in the data-processing quality mode. The following chart shows lines per minute print speed for different print qualities:

Lines Per Inch/ Character Per Inch	**Draft Quality**	**Data-Processing Quality**	**Near-Letter Quality**
6 lines per inch			
10 characters per inch	410	300	120
15 characters per inch	125	85	60

Note: Values shown are for upper case printing only. Mixed case printing decreases throughput rate by approximately 10%.

Other characteristics of the 4234 Printer are:

- 10 or 15 characters per inch.

- 4, 6, and 8 lines per inch.

- Lines-per-inch spacing is set in 1/144-inch increments.

4245 Printer

The 4245 Printer is a stand-alone, engraved band impact printer. Printing speed depends upon the number of characters on the print band, line spacing, and page format. Nominal speeds for 6 lines per inch with single-line spacing are shown in the following chart:

Number of Characters (Print Belt)	Lines per minute	
	Model T12	**Model T20**
48	1270	2000
52	1120	1791
50-64	980	1570
94-116	640	1051
108-142	445	744

Other characteristics of the 4245 Printer are:

- 10 characters per inch.
- 6 or 8 lines per inch, host selected.
- 132 print positions per line.
- 255 lines per page.
- 6-part form capability.

5219 Printer

The 5219 Printer is a letter quality printer and has an average print rate of 24 to 38 characters per second. The rate is determined by the model selected and is shown in the following chart:

5219 Model Number	Characters Per Inch	Characters Per Second Print Speed
1	10	26
1	12	26
1	15	24
1	PSM	24
2	10	38
2	12	38
2	15	38
2	PSM	34

Other characteristics of the 5219 Printer are:

- Supports 10, 12, or 15 characters per inch and proportional spacing mode (PSM) that is selected by the data stream command.
- Supports 4, 5-1/3, 6, 8, 9.6, 12, 24, or 48 lines per inch. Line spacing is selected by the data stream command.
- Supports manual feed cut sheet, tractor feed, envelopes, and automatic sheet feed paper handling.
- Handles paper widths of 3.15 inches to 15.4 inches.
- Supports multiple character sets and multiple print wheels.

- Provides a print quality (ribbon saver mode or normal mode) that is selected by the data stream command or a switch on the operator panel.
- Provides right justification, tab, continuous underscore, continuous overstrike, subscript, and superscript that are selected with the data stream command.

Note: The remotely attached 5219 Printer might not operate at the average speed because of the communications line speed.

5224 and 5225 Printers

The 5224 Printer and the 5225 Printer have print rates of 90 to 560 lines per minute; the rate is determined by the model selected and is shown in the following charts:

5224 Model Number	Characters Per Inch	Characters Per Line	Lines Per Minute Print Speed	Characters Per Line	Lines Per Minute Print Speed
1	10	74	140	132	90
1	15	111	95	198	60
2	10	74	240	132	120
2	15	111	170	198	85
12	10 (alphameric)	84	190	132	110
12	5 (IGC)	84	50	132	30

5225 Model Number	Characters Per Inch	Characters Per Line	Lines Per Minute Print Speed	Characters Per Line	Lines Per Minute Print Speed
1	10	74	280	132	130
1	15	111	195	198	90
2	10	98	400	132	205
2	15	147	290	198	145
3	10	118	490	132	330
3	15	177	355	198	235
4	10	130	560	132	520

5225 Model Number	Characters Per Inch	Characters Per Line	Lines Per Minute Print Speed	Characters Per Line	Lines Per Minute Print Speed
4	15	195	420	198	385
11	10 (alphameric)	124	300	232	255
11	5 (IGC)	-	85	-	-
12	10 (alphameric)	124	475	132	365
12	5 (IGC)	-	140	-	-

Note: For all models of the 5224 and 5225 Printers, the print speed shown in the charts is the maximum lines per minute. The speed depends on line length, spacing, and line skipping. The speed does not vary with the character set.

Other characteristics of the 5224 and 5225 Printers are:

- 132 or 198 print positions per line.
- 4, 6, or 8 lines per inch.
- The lines per inch can be set by program control.
- 10 or 15 characters per inch.
- The characters per inch pitch can be set by an operator panel switch or by program control.
- Forms width (continuous forms): 3 inches to 17.7 inches.
- Forms length (continuous forms): 6 inches to 12.5 inches.
- Character sets of 96 characters and 188-multinational characters.

Note: A remotely attached 5224 or 5225 Printer might not operate at rated speed because of the communications line speed.

5224 Model 12 and 5225 Model 11 and 12 (Ideographic)

The ideographic printers have print rates of 50 to 470 lines per minute. The rate is determined by the model and is shown in the previous charts.

Other characteristics of the 5224 Model 12 and 5225 Models 11 and 12 Printers are:

- The characters per inch is set by program control.
- Paper handling is manual feed or tractor feed.

- Forms width (manual feed): 7.2 inches to 14.3 inches.
- Forms length (manual feed): 7.2 inches to 11.7 inches.
- Forms width (continuous forms): 4.5 inches to 16 inches.
- Forms length (continuous forms): 5 inches to 11.7 inches.
- Shift out (SO) and shift in (SI) control characters for IGC mode can be selected.
- Multiple character sets are selectable.
- IGC characters are in an 18 x 18 dot matrix.
- A/N/K characters are in a 7 x 8 dot matrix.

Note: *A remotely attached ideographic printer might not operate at rated speed because of the communications line speed.*

5256 Printer

The 5256 Printer has print rates of 40, 80, or 120 characters per second; the rate is determined by the model selected and is shown in the following chart:

5256 Model Number	Characters Per Inch	Characters Per Second Print Speed
1	10	40
2	10	80
3	10	120

Other characteristics of the 5256 Printer are:

- 132 print positions per line.
- 6 or 8 lines per inch.
- 10 characters per inch.
- Single form or ledger card processing. The maximum size of the forms is 14-1/2 inches wide by 14 inches long. The minimum size is 6 inches wide by 3 inches long.
- Character sets of 96 or 128 characters; or the 188-character multinational character set.

Note: *A remotely attached 5256 Printer might not operate at rated speed because of the communications line speed.*

5262 Printer

The 5262 Printer is a stand-alone, belt printer and has a print rate of 650 lines per minute (using the 48-character set and 132 characters per line).

Other characteristics of the 5262 Printer are:

- 132 print positions per line.
- 6 or 8 lines per inch (manual or program controlled).
- 10 characters per inch.
- Single form or ledger card processing. The maximum size of the forms is 16 inches wide by 14 inches long. The minimum size is 3.5 inches wide by 3 inches long.
- Character sets of 48, 64, or 96 characters; the 128-character Katakana multinational character set; or the 188-character multinational character set.
- Uses the same commands as the 5256 Printer.
- Uses the same error codes as the 5256 Printer but some of the meanings are different.

Note: A remotely attached 5262 Printer might not operate at rated speed because of the communications line speed.

5553 or 5557 Printer

The 5553 or 5557 Printer has print rates of 30, 40, 60, and 120 characters per second. The rate is determined by the mode and is shown in the following chart.

Mode	Characters Per Inch	Characters Per Second Print Speed
IGC	5	30
IGC	6.7	40
A/N/K	10	60, 120

Note: Alphanumeric/Katakana (A/N/K) print speed is 120 CPS when every even horizontal dot is skipped.

Other characteristics of the 5553 Printer are:

- The characters per inch can be set by program control.
- Lines per inch is set in 1/72-inch increments by program control. The default is 6 lines per inch.

- Paper handling is manual feed cut sheet, tractor feed, or automatic sheet feed.
- Forms width (cut sheets): 7.2 inches to 14.3 inches.
- Forms length (cut sheets): 7.2 inches to 11.7 inches.
- Forms width (continuous forms): 4.5 inches to 16 inches.
- Forms length (continuous forms): 5 inches to 11.7 inches.
- Character rotation and grid line printing.
- The positions for shift out (SO) and shift in (SI) control characters for IGC mode can be selected. For example:
  - Blank spaces are printed.
  - Spaces are suppressed.
  - SO spaces are suppressed; SI provides two blank spaces.
- Multiple character sets are selectable.
- IGC characters are in an 18-by-24, 24-by-24, or 27-by-24 dot matrix.
- A/N/K characters are in a 13-by-18 dot matrix.

Note: *A remotely attached 5553 or 5557 Printer might not operate at rated speed because of the communications line speed.*

Printer Switches, Keys, and Lights

3262 Switches, Keys, and Lights

The operator panel on the 3262 Printer contains lights and touch keys and is shown in Figure 5-1.

Note: *After system IPL, the 3262 Printer controller is loaded with the default belt image of 48 characters and a default forms length of 1. The 3262 Printer controller is initialized, with the belt image and forms length contained in the system configuration record, when the first print request is issued to the printer.*

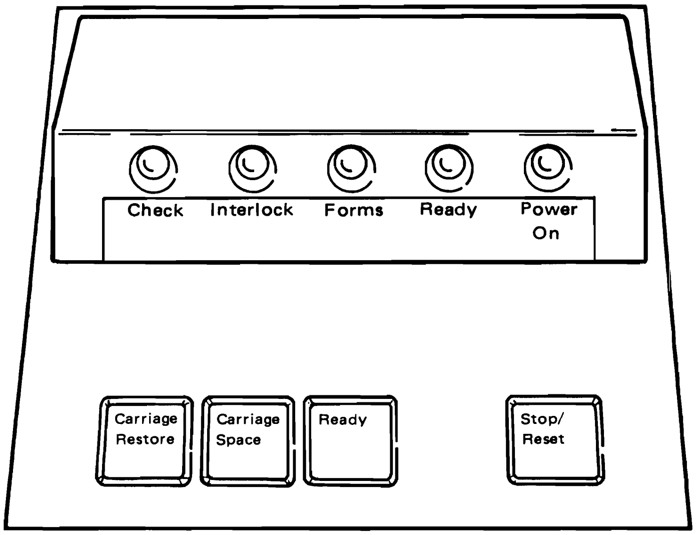


Figure 5-1. 3262 Printer Operator Panel

The Emergency Power switch is located on the side of the 3262 Printer.

3262 Operator Panel Switches and Keys

Carriage Restore key: Before the first print request is issued to the printer, this key (1) advances the carriage a single line if the Check, Interlock, and Ready lights are off and (2) sets the horizontal print position to 1.

After the first print request has been issued to the printer, this key (1) skips the carriage to line 1 of the next form if the Check, Interlock, and Ready lights are off and (2) sets the horizontal print position to 1.

Carriage Space key: Causes the carriage to advance a single line if the Check, Interlock, and Ready lights are off. This key does not affect the horizontal print position.

Ready key: Turns on the Ready light, sets the printer to a ready state, starts the print belt, and signals the processor that the printer is ready to receive commands. This key does not work when the Check, Interlock, or Forms light is on, or if the printer controller is not running.

Stop/Reset key: Causes the printer to stop and the Ready light to go off. If the printer is printing when the Stop/Reset key is pressed, the current line is completed before the printer stops. This key also resets printer check conditions (Check and Forms lights are reset). In addition, it is used for operator error recovery procedures as described under "Printer Status Bytes and Error Recovery Procedures," later in this chapter.

3262 Operator Panel Lights

The Check, Interlock, and Forms lights flash on and off when active.

Check: A check condition was sensed and informs the operator that error recovery action is needed. (Also see the description of the Forms light.) If the check condition is corrected, the Check light can be turned off by pressing the Stop/Reset key.

Interlock: The print unit is open or the belt cover is not in place.

Forms: Less than 35.6 centimeters (14 inches) of forms are still in the 3262 Printer below the current print line and more forms must be placed in the printer. If the Forms light is on at the same time as the Check light, a carriage check condition is indicated; this might be a forms jam or loss of vertical position.

Ready: If the Check, Interlock, and Forms lights are off, the Ready light is turned on by the system in response to the Ready key; it indicates the printer is ready to print.

Power On: The power to the printer is on.

3812 Printer Switches, Keys, and Lights

The operator panel on the 3812 Printer contains switches, touch keys, and lights and is shown in Figure 5-1.1. There are four keys, ten LED indicators, and one 3-digit LED display. The Power switch is on the lower left side of the printer and turns power on or off.

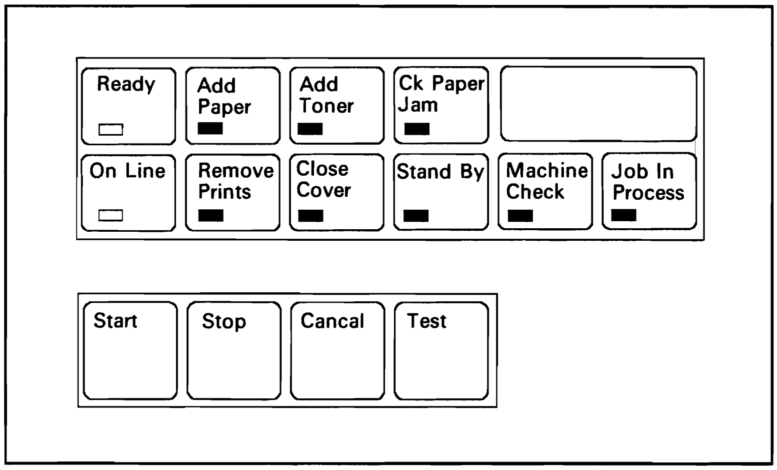


Figure 5-1.1. 3812 Operator Panel

3812 Operator Panel Keys

Start key: Starts or restarts a print job.

Stop key: Interrupts an active job.

Cancel key: Interrupts an active job, and with the appropriate host support, also cancels the job by sending a cancel request status to the host.

Test key: Invokes test prints of available font samples and test patterns. This test print continues until the Stop key is pressed.

3812 Operator Panel Lights and Indicators

Ready light: The printer is ready to print data or perform commands from the system.

On line light: The printer is connected to the host and is ready to receive and send data.

Add Paper light: The printer needs more paper, or the input paper cassette is not installed.

Remove Prints light: The print exit tray is full. Printing is suspended until prints are removed from the tray.

Add Toner light: The toner level is low (about 300 prints can still be made), or there is no toner in the cartridge and the developer level is low. In this case, the lighted message is accompanied by an error code in the operator panel display, and all printing operations are discontinued.

Close Cover light: The top or front cover is open. Printing is suspended until the cover is closed.

Clr (clear) Paper Jam light: A paper jam has occurred. Printing is suspended until the operator clears the jam. There are four areas where paper jams can occur. These areas are designated by a label under the top cover. The code in the LED display indicates where the paper jam occurred. After the paper jam is cleared, the printer continues printing without an operator restart or further intervention.

Stand By light: This is a blinking light that comes on for any of the following reasons:

- The printer is going through a warm-up diagnostic cycle. When this cycle is complete, the Stand By light goes off and the Ready light comes on.

- A printer error has occurred. The Stand By light continues to blink until the error has been corrected, and the Start key has been pressed.

- The printer is printing fonts and test patterns. Both the Stand By and Ready lights are on. Pressing the Stop key terminates the test print and turns off the Stand By light.

Machine Check light: An exception condition exists due to a machine problem. All printing is suspended until intervention by the operator (power-off or test). At the same time, a machine check status code is shown in the LED display. This indicates the nature of the exception.

Job In Process light: This light helps the customer distinguish between active and idle states. It comes on for any of the following reasons:

- The printer is printing fonts and test patterns.
- The printer is performing a diagnostic test.
- Data is being transmitted to, or processed by, the printer.

LED display: Indicates what is needed for operator intervention or what caused an error condition. The displayed numbers indicate one of the following types of messages:

- Operational-state message (to be associated with information in the lighted messages).
- Diagnostic state message.
- User message.

Refer to the indicator lights for a description of conditions that cause a value to be placed in the LED display. Also, refer to the *IBM Pageprinter Problem Determination Procedures,* S544-3337.

3812 Font Selection

The following table lists the fonts supported by the IBM 3812 Printer attached to an IBM System/36.

For those using the IBM System/36 API PRPQ and the TRANS option to select fonts, parameters "Global Font ID" (gfgf) and "Font Width" (fwfw) for the Set Font Global (SFG) command are given in both hexadecimal and decimal.

The font attribute (fa), also a part of SFG, is ignored by the 3812 Printer; proportionally spaced fonts are always printed proportionally spaced and fixed pitch fonts are always printed fixed pitch regardless of the attribute speed.

When using typographic fonts, justification is not supported. In addition, since the 3812 Printer is not aware of the size of the font being used, line endings (that is, how many characters will fit on a line) are the user's responsibility.

Font Name	Pitch	Font ID (Simulated)	Font ID Hex (gfgf)[1]	Font Width[2]	Font Width Hex (fwfw)[3]	5219	DW/36-5	API PRPQ
OCR-B	10	3	03	144	90			●
ORATOR[4]	10	5	05	144	90	●	●	●
Courier 10	10	11	0B	144	90	●	●	●
Prestige Pica	10	12	0C	144	90	●	●	●
Artisan 10	10	13 (11)	0D	144	90	●	●	●
Courier Italic 10	10	18	12	144	90		●	●
OCR-A	10	19	13	144	90			●
Pica	10	20 (12)	14	144	90	●	●	●
Math Symbol 10	10	30 or 198 (11)	1E	144	90	●		●
ORATOR BOLD	10	38	26	144	90		●	●
Gothic Bold 10	10	39	27	144	90		●	●
Gothic Text 10	10	40	28	144	90		●	●
Roman Text 10	10	41	29	144	90		●	●
Serif Text 10	10	42	2A	144	90		●	●
Serif Italic 10	10	43	2B	144	90		●	●
カタカナ [Katakana]	10	44	2C	144	90		●	●
Courier Bold 10	10	46	2E	144	90		●	●
שלום [Shalom]	10	50	32	144	90		●	●
Gothic Text 12	12	66	42	120	78		●	●
Gothic Italic 12	12	68	44	120	78		●	●
Gothic Bold 12	12	69	45	120	78		●	●
Serif Text 12	12	70	46	120	78		●	●
Serif Italic 12	12	71	47	120	78		●	●
Serif Bold 12	12	72	48	120	78		●	●
Math Symbol 12	12	80 (86)	50	120	78	●	●	●
Script	12	84	54	120	78	●	●	●
Courier 12	12	85	55	120	78	●	●	●
Prestige Elite	12	86	56	120	78	●	●	●
Letter Gothic 12	12	87	57	120	78	●	●	●
Light Italic 12	12	91 (112)	5B	120	78	●	●	●
Letter Gothic Bold	12	110	6E	120	78		●	●
Prestige Elite Bold	12	111	6F	120	78		●	●
Prestige Elite Italic	12	112	70	120	78		●	●
Boldface Italic	PS	155	9B	120	78		●	●
Modern	PS	158 (175)	9E	120	78	●	●	●

Figure 5-1.2 (Part 1 of 2). 3812 Font Selection

Font Name	Pitch	Font ID (Simulated)	Font ID Hex (gfgf)	Font Width	Font Width Hex (fwfw)	5219	DW/36-5	API PRPQ
Boldface	PS	159	9F	120	78	●	●	●
Essay	PS	160	A0	120	78	●	●	●
Essay Italic	PS	162	A2	120	78	●	●	●
Essay Bold	PS	163	A3	120	78		●	●
ברק [Barak]	PS	168	A8	120	78		●	●
Essay Light	PS	173	AD	120	78		●	●
Document	PS	175	AF	120	78		●	●
Gothic Text 13	13	204	CC	108	6C			●
Prestige 15	15	221 (230)	DD	96	60	●	●	●
Courier 15	15	223 (230)	DF	96	60	●	●	●
Math Symbol 15	15	225 (80)	E1	96	60	●	●	●
Serif Text 15	15	229	E5	96	60	●	●	●
Gothic Text 15	15	230	E6	96	60	●	●	●
Courier Bold 5	5	245	F5	288	120			●
Courier 17	17	252	FC	84	54			●
Courier Bold 17	17	253	FD	84	54			●
Courier 17 (sub/super)	17	254	FE	84	54			●
Gothic Text 20	20	281	119	72	48			●
Gothic Text 27	27	290	122	54	36			●
Sonoran-Serif 8-pt Roman Medium	typ	751	2EF	54	36			●
Sonoran-Serif 10-pt Roman Medium	typ	1051	41B	66	42			●
Sonoran-Serif 10-pt Roman Bold	typ	1053	41D	66	42			●
Sonoran-Serif 10-pt Italic Medium	typ	1056	420	66	42			●
Sonoran-Serif 12-pt Roman Medium	typ	1351	547	84	54			●
Sonoran-Serif 16-pt Roman Bold	typ	1653	675	108	6C			●
Sonoran- Serif 24-pt Roman Bold	typ	2103	837	162	A2			●

Figure 5-1.2 (Part 2 of 2). 3812 Font Selection

Notes:

1. *When used in printer commands, (gfgf) must be preceded by 00.*

2. *The decimal width of the font.*

3. *Used with printer commands as (fwfw).*

4. *Same font as Rhetoric on the 5219.*

4210 Operator Panel

The operator panel of the 4210 Printer is shown in Figure 5-1.2. Its features are:

- Seven light emitting diode (LED) indicators to display the current status of the printer.

- Six keys to control the state and actions of the printer.

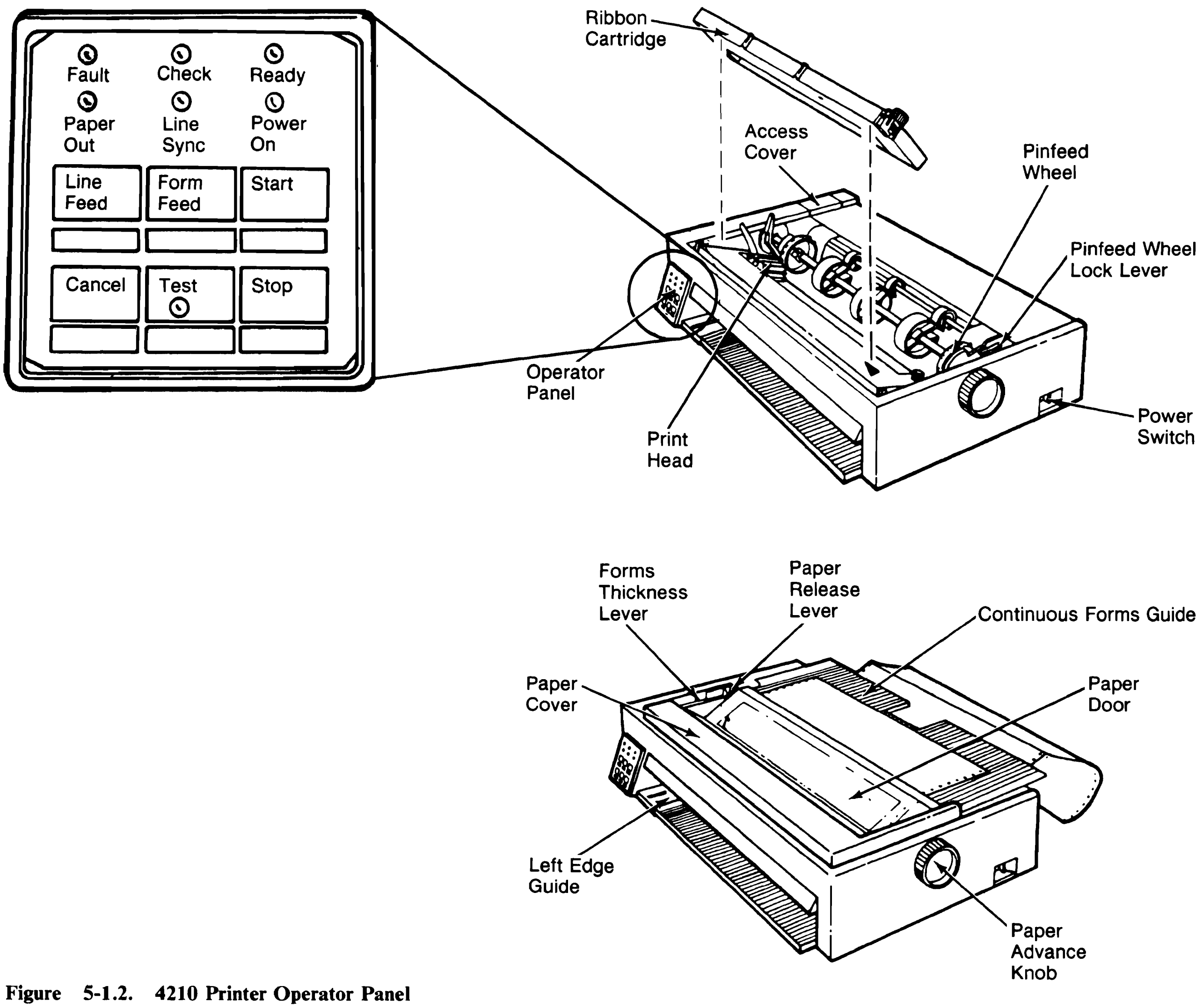


Figure 5-1.2. 4210 Printer Operator Panel

4210 Operator Panel Lights

Fault Light

The **Fault** light is on when the printer detects a hardware error with the printer. This light also is on if the printer switches are set to an invalid printer address or language selection.

Check Light

The **Check** light is on when the printer detects an error between the printer and computer. Contact your computer operator when this light comes on.

Ready Light

The **Ready** light is on when the printer is ready to receive information for printing. The **Ready** light blinks when the printer is in the setup mode. We will tell you more about the setup mode later in this section.

Paper Out Light

The **Paper Out** light blinks when you need to put paper in the printer.

The **Paper Out** light on indicates near-letter-quality (NLQ) print mode is active.

Line Sync Light

The **Line Sync** light is on when the printer is communicating with the computer.

Power On Light

The **Power On** light is on when the printer power is on.

Test Light

The **Test** light comes on when you press the **Test** key to indicate that the printer is in test mode.

The following chart summarizes the meaning of the lights on the operator panel.

Light	Status	Meaning
Fault	On ● Fault	Printer error.
Check	On ● Check	Printer detects an error between the printer and computer.
Ready	On ● Ready	Printer is ready to print.
Ready	Blinking ○ Ready	Setup mode is on.
Power On	On ● Power On	Printer power is on.
Line Sync	On ● Line Sync	Printer is communicating with the computer.
Paper Out	Blinking ○ Paper Out	Printer is out of paper. 1
Paper Out	On ● Paper Out	NLQ mode is active.
Test	On Test ●	Test mode is on.

The 4210 Printer can be in one of the following states:

- Ready state

  When the 4210 Printer is in the Ready state, it is under control of the IBM System/36. The System/36 can send data for printing and receive printer status from the 4210. This state is entered by pressing the Start key from the Not Ready state. The function keys enabled are:

  - STOP
  - Form feed
  - Line feed

From the Ready state, the 4210 can be placed in one of the following modes:

  - NLQ mode
    The Form Feed key is used to select/cancel NLQ mode

  - Quiet mode
    The Line Feed key is used to select/cancel Quiet mode

  - Setup mode
    The Line Feed key is pressed and held and the Stop key is pressed to select the Setup mode. This mode allows the operator to select features of the printer not available in the Printer Data Stream. Pressing the Start key cancels Setup mode.

- Not Ready state

  When the 4210 Printer is in the Not Ready state, it is under control of the operator. The function keys enabled are:

  - Start

  - Cancel

  - Form Feed

  - Line Feed

  - Test

- Test/offline state

  The Test state is entered from the Not Ready state when the Test key is pressed. In this state, the 4210 is not communicating with the System/36. The function keys enabled are:

  - Test

  - Cancel

  - Form Feed

  - Line Feed

- Error state

  The 4210 Printer enters the Error state when an exception condition has occurred and the Stop key has not been pressed. If the exception condition is in a Data Loss situation, the exception must be cleared using the Cancel key. The Cancel key notifies the System/36 operator that the print job is suspended for possible restart after the proper error recovery action.

  The only function key enabled is the Cancel key.

The following charts show the function of each operator key for the various printer modes:

Line Feed Key

If the printer is:	**Pressing the Line Feed key allows you to:**
Not ready (**Ready** light off)	Advance paper one line.
Ready (**Ready** light on)	Set **Quiet mode** on or off.
Ready, and the **Stop** key is pressed and held	Enter **Setup mode**.
In Setup mode (**Ready** light blinking)	Step through setup menu.
Off	Begin self test. You must press and hold the Line Feed key while switching power On (I) until printing starts. To stop the self test, you must switch power Off (O).

Form Feed Key

If the printer is:	**Pressing the Form Feed key allows you to:**
Not ready (**Ready** light off)	Feed to top of form position.
Ready (**Ready** light on)	Set NLQ print mode on or off.
In Setup mode (**Ready** light blinking)	Select a function.
Out of paper (**Paper Out** light blinking)	Begin paper load assist.

Start Key

If the printer is:	**Pressing the Start key allows you to:**
Not ready (**Ready** light off)	Make printer ready.
In Setup mode (**Ready** light blinking)	End Setup mode.

Stop Key

If the printer is:	**Pressing the Stop key allows you to:**
Ready (**Ready** light on)	Make printer not ready.
Ready, and the **Line Feed** key is pressed and held	Place the printer in Setup mode.

Test Key

If the printer is:	Pressing the Test key allows you to:
Not ready (**Ready** light off)	Run the printer test.

Cancel Key

If the printer is:	Pressing the Cancel key allows you to:
Not ready (**Ready** light off)	Send a request to the computer to stop sending print data. *Note: Printing stops when the printer buffer is empty.*
Not ready, and the **Fault** light is on	Clear the error when the **Stop** key is pressed.
In Test mode	Exit Test mode.

4214 Printer Switches, Keys, and Display

4214 Power Switch

The Power switch is on the front of the printer and turns power on or off. Each time the Power switch is set to on, the printer is reset and a test is started to determine possible problems in the printer. If no problems are detected, the display will indicate 00 STOPPED and one of the words ASF, MSF, DOD, or CTF, depending on the present forms selection mode.

4214 Operator Panel

The operator panel on the 4214 Printer contains switches, keys, and lights and is shown in Figure 5-2.

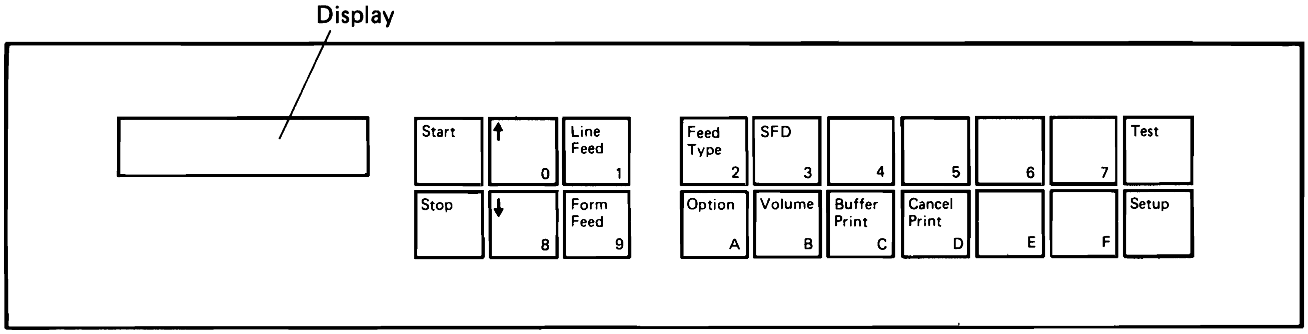


Figure 5-2. 4214 Printer Operator Panel

4214 Operator Panel Switches and Keys

All keys, except the Test key, are made active by first pressing the Stop key. When the keys are pressed, there will be a sound. If a key is used in typamatic mode, the sound will occur at the typamatic rate. The sound volume can be changed by the operator by using the option function of the operator panel.

All keys are active when the printer is not ready (unless there is a print check error), regardless of what causes the not ready condition.

All keys that change operator changeable parameters (feed type, CPI, LPI, font density, volume, and buffer print) operate as follows:

- Pressing the key displays the current configuration setting.
- A change may now be made by keying in the new value. The value is entered high order first (hundreds, tens, units). Leading zeros need not be entered except when OPTION is being displayed.
- Pressing the Start key causes the new value to be checked for validity. If it is invalid, 09 STOPPED (invalid operation) is displayed immediately and the old value is not changed. If it is valid, working RAM is changed to the new value and option 99 can be used to store the non-volatile RAM.
- Pressing the Stop key instead of the Start key causes the key change in process to be canceled with no change being made.

All keys that perform a print or forms operation such as (up arrow), (down arrow), Setup, Form Feed, Line Feed, Start, and Stop keys operate as follows:

- Normal operation (no errors indicated): When a key is pressed, the operation is performed.
- Exception operation (an error is indicated):
  - When a key is pressed, the error indication is cleared, the alarm is turned off, and the operation is performed. The Stop key simply resets the error and the alarm, and displays STOPPED. The Start key resets the error and the alarm, and displays READY.
  - If the operation is not successful, an error is displayed again and the alarm is turned on. If the operation is successful, normal operation continues.

Following is a list of the operator panel keys and their functions.

Start key: Pressing the Start key causes the following:

- If STOPPED is being displayed, the printer goes ready and disables all other keys except the Stop key and the Test key. READY is displayed in the LCD.
- If a working RAM change is being made and the current value in the LCD is invalid, 09 STOPPED (invalid operation) is displayed immediately and the old value is not changed. If it is valid, working RAM is changed to the new

value displayed in the LCD and option 99 can be used to store the non-volatile RAM.

- If manual sheet feed (MSF) is active and a form is in the printer but not positioned under the print head, it causes the form to feed to the top of the form.

Stop key: Pressing the Stop key causes:

- The alarm to be turned off
- An error being displayed in the liquid crystal display (LCD) to be cleared if the error condition has been removed
- The printer to go not ready with STOPPED displayed in the LCD
- A change parameter operation to be ended with no change to the parameter if the option key was not pressed first

(Up arrow)/0 key:

- Vernier to move paper forward. Each individual depression will move the form a distance equal to the motor step in effect at the time (1/120th or 1/108th of an inch).

(Down arrow)/8 key: Vernier to move paper backward in motor step increments the same as the (up arrow) key.

Line Feed/1 key:

- Causes the form to move up one line. Hold the key pressed, and the form continues to move up one line at a time.

Form Feed/9 key:

- Moves the paper to the top of the next form if printing continuous forms or documents on demand.
- Ejects the form if you are feeding cut forms by hand.

Feed Type/2 key: Displays or changes the types of forms handling operations that can be used.

The LCD displays FEED = n; where n can equal:

n	Function
1	Continuous tractor feed
2	Document on demand
3	Manual sheet feed
4	Automatic sheet feed 1
5	Automatic sheet feed 2
6	Automatic sheet feed 3

Use option 76 to unlock from the automatic sheet feed operation.

Option/A key: Checks or changes settings for which the printer does not have keys and causes the new option to take effect.

When a change is made, it becomes the current operating value. This function overrides what was copied to working RAM from nonvolatile RAM during power on reset. However nonvolatile RAM is not automatically changed when working RAM is changed. Option 99 will store working RAM into nonvolatile RAM if it is desired to keep the present values for the next power on reset.

The option mode is entered by pressing the Option key. 'OPTION = ' is then displayed in the LCD. Next, a two-digit option number is entered. The leading zero is required. This causes the current value of the particular option to be displayed in the LCD. If a change to this option is desired, the change can then be keyed in. If no change is desired, the Start or Stop keys will cause an exit from the option mode, or pressing the Option key again will allow a new option number to be entered and displayed.

Once an option value is changed by the operator, the Stop key can be used to quit the operation in process with no change made. The Start and Option keys both cause the new value to be checked for validity and if valid, stored in working RAM. If the Start key is used, the LCD displays STOPPED. If the Option key is used, the LCD displays 'OPTION ='. The next option desired can then be entered. If the value is invalid or if an invalid option number is entered, the LCD displays '09 STOPPED' (invalid operation).

Following is a list of the options available:

Option Name	**Option Number**	**n**	**Description**
KYBD = n	01	1	Off (keyboard feedback volume)
		2	Low (keyboard feedback volume)
		3	Medium (keyboard feedback volume)
		4	High (keyboard feedback volume)
LANG = nn	02	01	U.S./Canada (bilingual)
		02	Austrian/German
		03	Belgian
		04	Brazilian
		05	Canadian French
		06	Danish/Norwegian
		07	Finnish/Swedish
		08	French
		09	International #5
		10	Italian
		11	Japan (Latin)
		12	Portuguese

Option Name	Option Number	n	Description
		13	Latin America (Spanish speaking)
		14	United Kingdom
			The following *display* option is used to determine which language the words READY, STOPPED, and TEST will be displayed in.
DISPLAY = n	03	1	English
		2	French
		3	German
		4	Italian
		5	Spanish
CPI = nn	04	5	Characters per inch
		10	Characters per inch
		12	Characters per inch
		15	Characters per inch
		16	Characters per inch
MPP = n	05	1-220	Maximum print position
LPI = n	06	3	Lines per inch
		4	Lines per inch
		6	Lines per inch
		8	Lines per inch
MPL = n	07	1-255	Maximum page length
TEST = n	77	0	Disable Test key unless Stop has been pressed.
		1	Test key is active all the time.
PERM = n	99	1	Does nothing.
		2	Causes working RAM to be stored in nonvolatile RAM. This function is reset to 1 following the store operation.
ADDR = n	08	0-6	Device address

SFD/3 key: Displays or changes the font density.

The LCD will display SFD = n; where n can be:

n	Function
1	DPQ (data processing quality)
2	NLQ (near letter quality)

Volume/B key: Displays or changes the alarm volume.

The LCD will display VOLUME = n; where n can be:

n	Function
1	Off
2	Low
3	High

Buffer Print/C key: Changes the format (normal or hexadecimal printing) in which the receive buffer data is to be printed. Each depression of the switch causes a change to the other printing mode.

Cancel Print/D key: Is used to set the cancel print request status. If the request is accepted, printing stops and a status code 59 is displayed.

Test key: Stops sending to the controller and initiates the test previously selected. The system treats the printer as turned off.

Setup key: Causes the current print line to become the top of the form. The display shows TOP OF FORM. The printer prints an H on that line.

If you hold the key pressed, the printer prints 24 more Hs on the line. The line of Hs can be used to position the forms correctly.

4214 Operator Panel Display

Display: A 16-character hexadecimal liquid crystal display (LCD) indicator is used to display status codes and messages. Positions 1 through 3 from the left indicate the status codes. Positions 4 through 12 from the left indicate the messages. Positions 13 through 16 from the left indicate the document feed mode (ASF1, ASF2, ASF3, MSF, CTF, or DOD).

4224 Printer Switches, Keys, and Lights

The operator panel on the 4224 Printer contains keys and lights as shown in Figure 5-3.

The current values of the keys are stored when the printer is powered off and become the current values again when the printer is powered on.

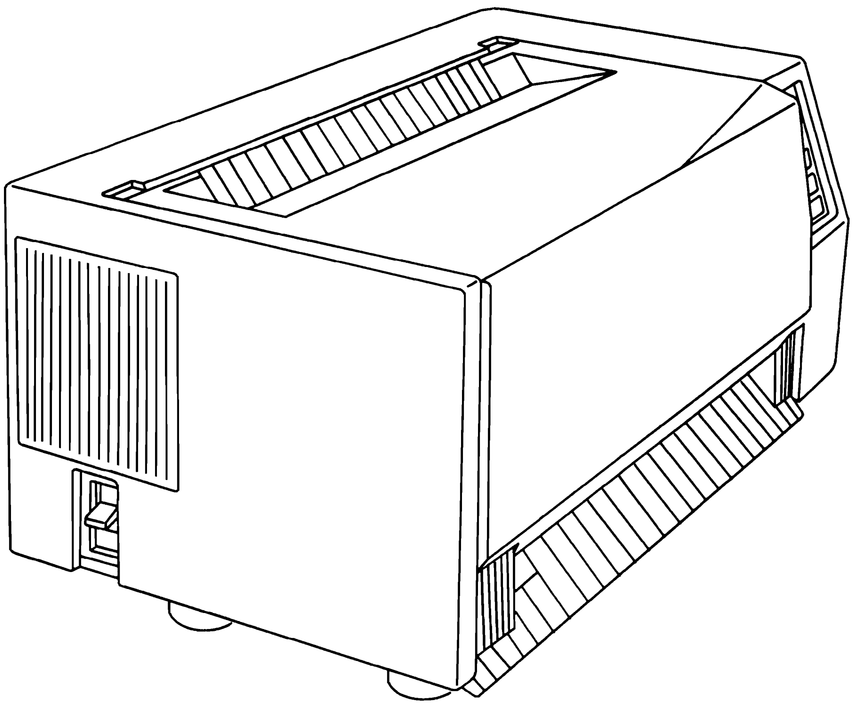


Figure 5-3. 4224 Printer Operator Panel

4224 Operator Panel Switches and Keys

Power switch: Turns power on or off to the printer. Also starts a test to determine that the correct voltage is available, for the printer units, each time the Power switch is set to on.

Start key: If no errors are present and if the test for power on is complete, this key turns on the Ready light and makes the printer ready to perform commands or resume printing, and removes the 00 status. When in the test mode, pressing this key will cause the printer to start the test.

Stop key: Causes the printer to stop during the current operation and turn the Ready light off. If an error is present, pressing this key will cause the printer to try to reset the error condition, reset the indicator to 00, and shut off the alarm.

Top of Form key: Causes the printer to establish the forms line under the print head as the first print position on the form. The Top of Form key is usable only when the printer is not ready. If you power the printer on while holding down the Top of Form key, initial factory defaults are restored.

Form Feed/Forms Device key: Causes the carriage to skip to top of forms position of the next form. The Form Feed key is usable only when the printer is not ready.

Load/Eject key: Is used to eject the forms or load a new form. The Load/Eject key is usable only when the printer is not ready.

Cancel key (Alternate and Cancel key): Is used to request a cancel function from the host. If the request is accepted, the cancel request status is set. When the Cancel key is pressed, and a cancel request is accepted, a 59 will be displayed, an alarm will sound, and all printing will stop. When in offline mode, this key is used to return the printer to online mode. This key combination is usable only when the printer is online and not ready.

Test (Alternate and Test key): Puts the printer in the test mode for problem determination. The test keys are usable only when the printer is not ready.

Up Arrow (Line Space) key: Causes the carriage to advance 1/72 of an inch when pressed and released. If the key is held down, the carriage will continue to advance until the key is released. The Up Arrow key is usable only when the printer is not ready.

Down Arrow key: Causes the carriage to reverse feed 1/72 of an inch when pressed and released. If the key is held down, the carriage will continue to reverse feed until the key is released. The Down Arrow key is usable only when the printer is not ready.

Alternate key: If pressed and held while pressing another key, the other key will have a different function. This key is functional only when the printer is in the not ready state.

Left Arrow key: Causes the physical print position on the form to move to the left about 2/100 of an inch each time it is pressed and released. The number of 1/100ths of an inch moved is displayed in the control panel display. Maximum print position shift is 2/10 of an inch from the home position. The Left Arrow key is usable only when the printer is not ready.

Right Arrow key: Causes the physical print position on the form to move to the right about 2/100 of an inch each time it is pressed and released. The number of 1/100ths of an inch moved is displayed in the control panel display. Maximum print position shift is 2/10 of an inch from the home position. The Right Arrow key is usable only when the printer is not ready.

PA1 (7 key): Causes the printer to send a program attention 1 signal to the host. The key is usable only when the printer is not ready.

PA2 (8 key): Causes the printer to send a program attention 2 signal to the host. The key is usable only when the printer is not ready.

4224 Operator Panel Lights

Ready light: Turned on by the Start key and turned off by the Stop/Reset key or when any error is present.

Display: Double alphameric LED indicators used to display various status codes.

4234 Printer Switches, Keys, and Lights

The operator panel on the 4234 Printer contains switches, touch keys, and lights and is shown in Figure 5-3.1. There are a print quality switch, a language selector switch, an address selector switch, sixteen function keys, eight discrete LED indicators, and a status indicator (SI) consisting of two alphameric LED indicators. A list of selected error status codes is also displayed on the panel, under the cover. The Power switch is on the left-hand side of the operator panel and turns power on or off.

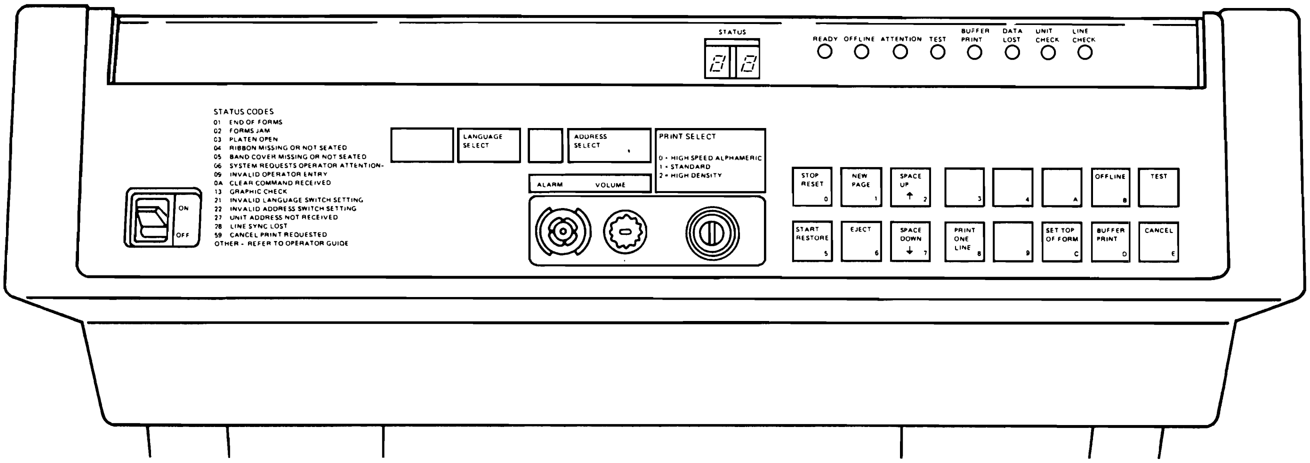


Figure 5-3.1. 4234 Printer Operator Panel

4234 Operator Panel Switches and Keys

Print Quality switch: A rotary switch that selects print quality: draft, data-processing, quality, or near-letter quality. The current setting can be noted by the position of the switch. Data-processing quality is the default if no specific position is set. A change in the setting is only accepted in stop mode. Switch selection can be overridden by the host. Control can be reinstated to the operator panel only by host relinquishment or by turning the printer off, then on again.

Language Selector switch: Establishes language-use tables when the printer is turned on.

Address Selector switch: Sets the printer address with which the unit responds to host polling. Valid values range from 000 through 110.

Stop/Reset key: Interrupts the current printing operation and places the printer in stop mode. Turns off the Ready light and turns on the Attention light. This key also deactivates buffer print mode.

New Page key: Causes the carriage to skip to line 1 of the next form (if the Ready light is off and no errors are present).

Space Up key: Operates only in stop mode. Causes a single-line feed action, and is typematic. When the Start/Restore key is pressed, and if less than two logical page boundaries are crossed with this function, the form is reverse fed back to the proper physical print position on the interrupted logical page. Normal printing then resumes. If more than two boundaries are crossed, the form is advanced to the proper physical print position on the current logical page.

Offline key: Enables the offline mode if the printer is in online mode and not ready. The offline light is turned on. If this key is pressed accidentally, it can be reset by pressing the Stop/Reset key. If you press the Test key in offline mode, the printer remains in offline mode until it is turned off, then turned on again. If the printer is in offline mode and the Test key is not pressed, the Cancel key can be used to bring the printer back online.

Test key: This key is active at all times once the printer has warmed up. Pressing the Test key causes the entire complement of diagnostics to be run, as well as contents of the buffers, error log, and other pertinent information to be printed once the key is released. This key also can be used to select specific test procedures. If an abnormal completion is encountered during any of these tests, the appropriate error status code is displayed.

Start/Restore key: Causes the printer to exit stop mode and enter operating (ready) mode. Normal printing then resumes.

Eject key: Operates only in stop mode. Causes the forms to be ejected a fixed distance so that perforation of the form desired is at the tear bar. When the Start/Restore key is pressed, forms move in the reverse direction a distance equal to the eject.

Space Down key: Operates only in stop mode. Causes a single reverse line-feed action, and is typematic. When the Start/Restore key is pressed, and if less than two logical page boundaries are crossed with this function, the form is reverse fed back to the proper physical print position on the interrupted logical page. Normal printing then resumes. If more than two boundaries are crossed, the form is advanced to the proper physical print position on the current logical page. Exercise caution when using this key.

Print One Line key: If no errors are present, this key causes the printer to perform all host operations up to and including printing one line. In buffer print mode, this key causes one data buffer to be printed in hexadecimal code.

Top of Form key: Operates only in stop mode. Causes the carriage to skip to line 1 of the next form if the Ready light is off and no errors are present. When the Start/Restore key is pressed, and if less than two logical page boundaries are crossed with this function, the form is reverse fed back to the proper physical print position on the interrupted logical page. Normal printing then resumes. If more than two boundaries are crossed, the form is advanced to the proper physical print position on the current logical page.

Buffer Print key: Operates only in stop mode. Causes data sent to the printer to be printed in hexadecimal code. In this mode, format control codes are not executed and are tested as data. As an aid in counting, a hexadecimal count is printed above every 17th character and a vertical bar is printed above every 8th character, starting from the second character on the left.

Cancel key: When pressed, a status of '59' momentarily displays in the SI, a short alarm sounds, and Cancel Request status is set. This key also acts to exit offline and test modes.

4234 Operator Panel Lights and Indicators

Ready light: The printer is ready to print or is printing. Pressing the Start/Restore key turns on the Ready light. After an eject operation, the Start/Restore key must be pressed twice to turn on the Ready light. An error condition, or pressing the Stop/Reset key, turns off the Ready light.

Offline light: The printer is not communicating with the control unit/computer. Pressing the Offline key turns on this light. Pressing the Stop/Reset key turns off this light.

Attention light: The printer is not ready. Other indicator lights show printer conditions that require operator attention. Error conditions, or pressing the Stop/Reset key, turns on this light.

Test light: Printer tests are running. Pressing the Test key turns on this light. The light remains on until tests complete successfully (no errors interrupted the tests).

Buffer Print light: The printer recognizes a buffer print request.

Data Lost light: The printer lost data from the control unit/computer when an error occurred.

Unit Check light: The printer detects an error. The printer then displays the appropriate status code.

Line Check light: The printer detects a line parity error from the control unit/computer. No action by the operator affects this light. The error is corrected by the control unit/computer.

Audible Alarm: Alerts the operator when an intervention is required or unit check condition has been detected. The alarm can be displayed by pressing the Stop/Reset key. The volume level of the alarm can be controlled by a mechanical adjustment.

4245 Printer Switches, Keys and Lights

The operator panel at the front of the 4245 Printer contains switches, touch keys, and lights and is shown in Figure 5-3.2. There are five keys, ten lights, and two switches.

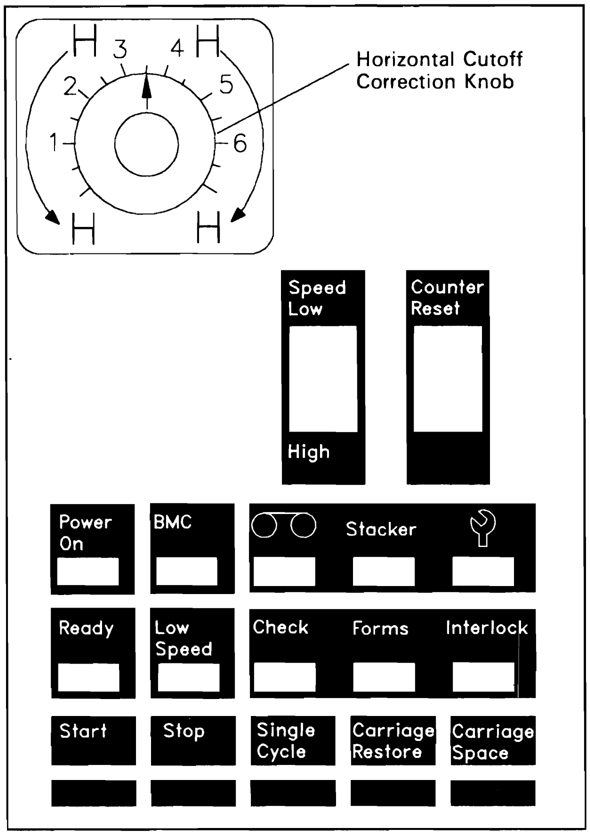


Figure 5-3.2. 4245 Printer Operator Panel

The operator panel at the rear of the 4245 Printer contains four keys and is shown in Figure 5-3.3. The upper three keys are duplicates of keys on the front operator panel. The fourth key controls the stacker tray position.

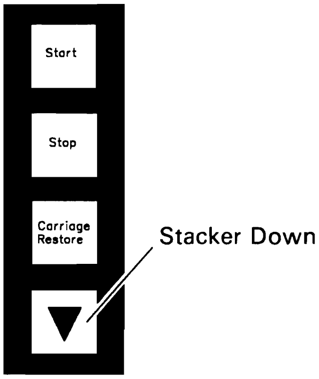


Figure 5-3.3. 4245 Printer Rear Operator Panel

The auxiliary operator panel at the right front cover of the 4245 Printer contains five switches and seven lights and is shown in Figure 5-3.4. The switches are for power control and are primarily used by your IBM Service Representative. The lights indicate power status and the printer's line synchronization status.

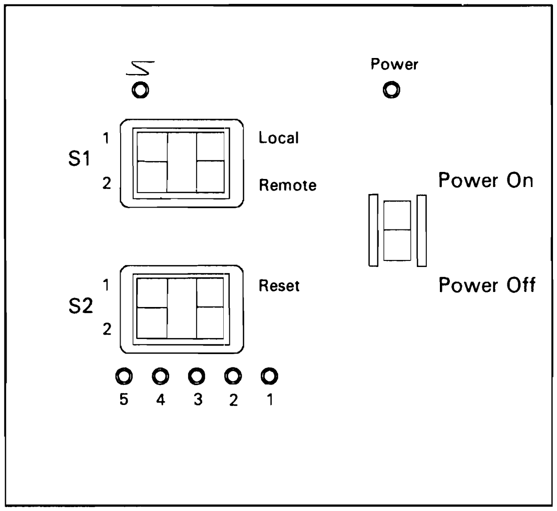


Figure 5-3.4. 4245 Printer Auxiliary Operator Panel

4245 Unit Emergency Switch

CAUTION
Use the Unit Emergency switch only for emergencies.

The Unit Emergency switch is located on the right front cover of the printer. It immediately turns off all power to the printer.

4245 Operator Panel Keys and Switches

Speed Low/High switch: Used only on Model T20, this switch changes the print band speed. The low·print speed may be chosen for better printed copy, or for further improvement of print quality when using nonstandard print bands. This switch also operates as a test switch for BMC.

Start key: If no errors are present, and if the power-on test is complete, this key turns on the Ready light, starts the print band motor, reads the print band identification, and loads the print band image into a table. The Start key starts print operations and resets check conditions. The first activation of the Start key or the Single Cycle key after power on renders the printer online to the system.

Stop key: Interrupts the printing process, switches the printer to the not ready state, and turns off the Ready light. When the front unit is open, pressing the Stop key activates the ribbon drive as long as the Stop key is pressed.

Single Cycle key: Operates only when the printer is in the not ready state. Pressing this key switches the printer to the ready state, prints one line, and switches the printer back to the not ready state. Repetitive pressing of this key prints line for line, as often as the key is pressed. The first activation of the Start key, or the Single Cycle key, after power on renders the printer online to the system.

Carriage Restore key: Operates only when the printer is in the not ready state. Pressing this key advances the forms carriage to the first print line of the next page.

Carriage Space key: Operates only when the printer is in the not ready state. Pressing this key advances the carriage a single space.

Stacker Down key (triangle): Only located on the rear operator panel. Operates only when the printer is in the not ready state. Pressing this key lowers the stacker tray until the lowest position is reached or the key is released. The stacker tray must be moved up manually.

4245 Operator Panel Lights and Indicators

Power On light: The green Power-on light on the front operator panel indicates successful power on the printer unit. The red Power-on light at the auxiliary operator panel is turned on when the power-up sequence is started and is turned off when the power-down sequence ends.

Ready light: Turns on when the printer switches to the ready state. This is expected after pressing the Start key. The Ready light is turned off when the printer switches from the ready state to the not ready state. This happens after pressing the Stop key or when an error condition occurs.

BMC light: Used only on Model T20, this light indicates the print band drive is not working properly. The light either flashes or remains steadily on.

Low Speed light: Used only on Model T20, this light indicates when low speed is accepted by the printer.

Ribbon Check light: The ribbon has too much skew to the left.

Stacker Check light: The stacker is full or a paper jam has occurred in the stacker. The printer switches to the not ready state.

Call CE light (wrench): The platen-protection tape is nearly filled. The remaining printing time is approximately five hours. After that time, a printer error is issued, the printer stops and cannot be run again until a new platen-protection tape is installed.

Check light: An error condition is detected by the work station controller.

Forms light: End-of-form, torn forms, or a forms jam exists.

Interlock light: The front unit is opened.

Printer Line Synchronization light: On the auxiliary operator panel only. Indicates communication status with the work station controller. The light is on if the work station controller is polling, issuing commands, or sending data. The light turns off if a signal has not been received for 250 microseconds.

Maintenance Panel

The maintenance panel is mainly used by your IBM service representative, but you can use it for functions which are not covered by other operator panels.

The maintenance panel is stored in a small compartment on the right side of the printer. See Figures 5-3.5 and 5-3.6. The maintenance panel becomes operational when you open the cover. The cover should be closed when the maintenance panel is not in use.

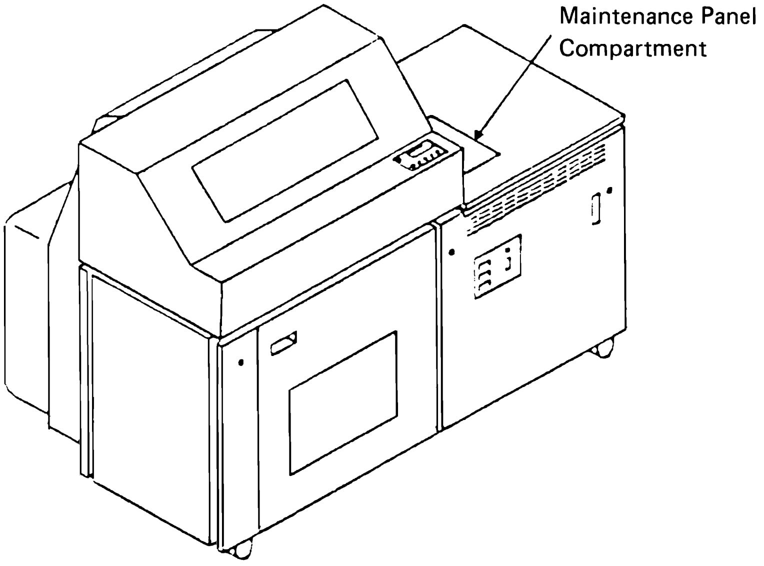


Figure 5-3.5. 4245 Printer Maintenance Panel Location

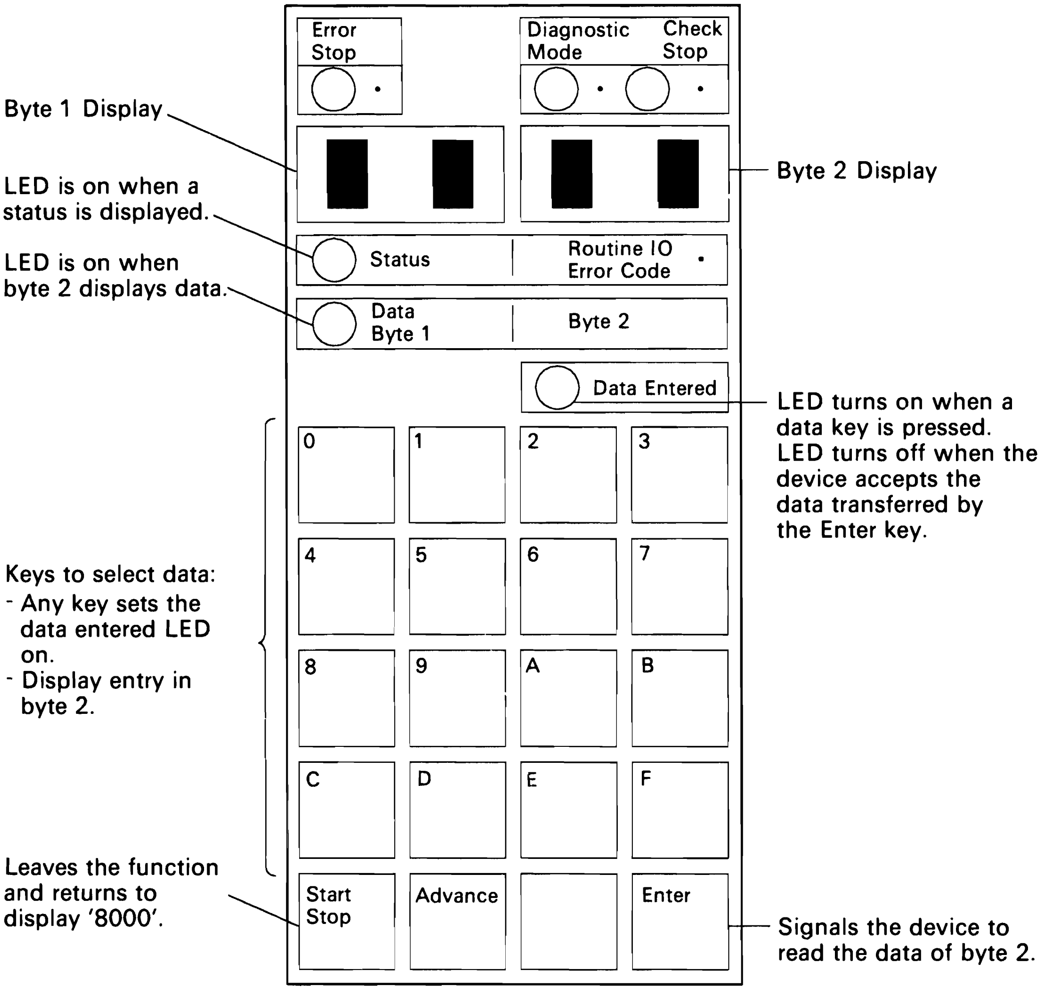

Error Stop
Diagnostic Mode
Check Stop
Byte 1 Display
Byte 2 Display
LED is on when a status is displayed.
LED is on when byte 2 displays data.
Status
Routine IO Error Code
Data Byte 1
Byte 2
Data Entered
LED turns on when a data key is pressed. LED turns off when the device accepts the data transferred by the Enter key.
0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F
Keys to select data:
- Any key sets the data entered LED on.
- Display entry in byte 2.
Leaves the function and returns to display '8000'.
Start Stop
Advance
Enter
Signals the device to read the data of byte 2.

Figure 5-3.6. 4245 Printer Maintenance Panel

Before doing any functions from the maintenance panel:

1. Stop the printer.

2. Press the Start/Stop key on the maintenance panel. 8000 appears in the LED display.

There are three categories of functions:

- Alter/display printer defaults.

- Display address.

- Cancel print job.

Alter/Display Printer Defaults

Defaults for the page image are stored in nonvolatile memory. Default values can be displayed and altered through the maintenance panel when the printer is in the not ready state.

At power-on time, default values become the effective settings. They can be overwritten when:

- Corresponding data stream control codes are received.
- New host or new work station controller default values are received.
- Default values are altered through the maintenance panel. New default values become actual effective settings.

Note: Only printer default values, not actual effective settings, can be displayed through the maintenance panel.

The procedure to alter/display a default value is:

1. Enter a '2xxx' hexadecimal code with the data keys.
2. Press the Enter key.
3. Press the Start/Stop key to leave the alter/display function.

Line Density (LPI)

This code sets line density in lines per inch.

Value range:

2106 ===> 6 lpi
2108 ===> 8 lpi

Default value: 2106

Graphic Error Code

This code sets the default graphic error code.

Value range:

2640 through 26FE

Default value: 2660 (hyphen)

Maximum Page Length

This code sets the maximum page length. The value is entered in hexadecimal notation.

Value range:

2301 through 23FF

Default value: 2342 (66 in decimal)

Maximum Print Position

This code sets the maximum print position. The value is entered in hexadecimal notation.

Value range:

2401 through 2484

Default value: 2484 (132 in decimal)

Set Printer ID and Graphic Error Action

This code sets the printer ID and action to be taken when the printer tries to print a graphic character not in its range of characters.

The preface code for all these values is hex 29.

Example: If you entered hex 2908, you would be setting the unique 4245 printer ID.

Allowable values are:

2900: Use the 5256 Printer ID (hex A0) and process the graphic error character action as specified in the data stream.

2910: Use the 5256 Printer ID (hex A0) and overwrite the graphic error character action sent by the host in the data stream.

2908: Use the unique 4245 Printer ID (hex A5) and process the graphic error character action as specified in the data stream.

2918: Use the unique 4245 Printer ID (hex A5) and overwrite the graphic error character action sent by the host in the data stream.

Default graphic error character value: 60 (hyphen)

Display Address

The display address function displays the current device address. The function is used by the customer to remember the address when reconfiguring the printer.

Value ranges:

3E00 through 3E06

Cancel print jobs:

- Enter the hexadecimal code 1C and press the Enter key.
- Press the Start/Stop key to leave the function without executing the typed-in code.

5219 Printer Switches, Keys, and Lights

The operator panel on the 5219 Printer contains switches, keys, and lights and is shown in Figure 5-4. There are eight keys, two seven-segment LED displays, and ten LED indicators. The Power switch is located to the right of the operator panel. When the Power switch is up, power is on and when the switch is down, power is off.

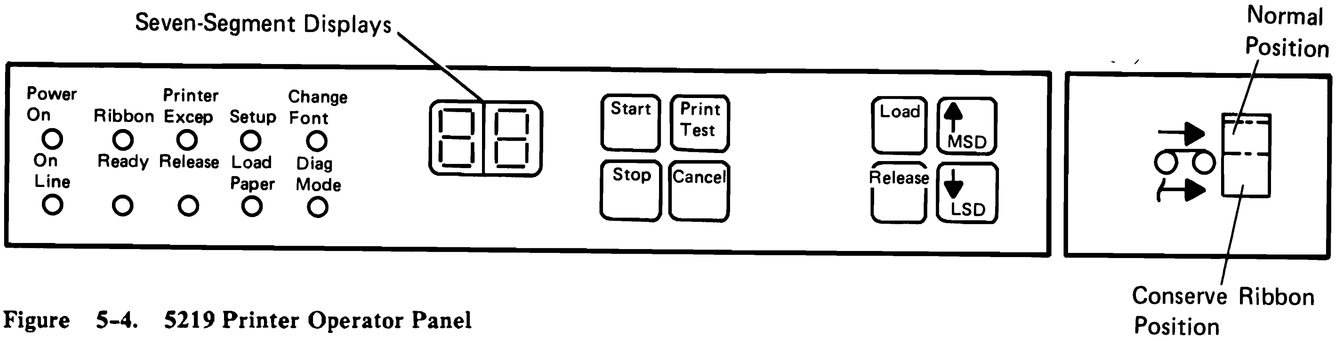


Figure 5-4. 5219 Printer Operator Panel

5219 Operator Panel, Switches, and Keys

Start key: Clears the seven-segment displays, turns the Ready light on, and allows normal printing to start.

Stop key: Stops the printer from printing and centers the escapement carrier to allow the operator access to the ribbon and print wheel. Turns off the ready indicator and the audible alarm (if on).

Print Test key: Causes printing of all the characters on the print wheel that is presently installed. This key causes the operation only if the Ready light is not on.

Cancel key: Causes the printer to set the cancel request bit on in the second poll response byte to the system.

Load key: Feeds the paper to the start position if the Ready light is off and the printer cover is closed. This key is ignored if pressed when the Ready light is on and the printer is printing, or if the Ready light is off and the printer cover is open.

Release key: Reverses the position of the pinch feed rollers. This key functions only when the printer is not ready.

Index Up (MSD) key: Moves the forms up (forward) while the key is pressed. The key causes the operation only when the Ready light is not on.

Index Down (LSD) key: Moves the forms down (reverse) while the key is pressed. The key causes the operation only when the Ready light is not on.

Ribbon Saver switch: This switch has a conserve ribbon (data printing) position and a normal (quality printing) position. The switch allows you to conserve the ribbon and increase its life by decreasing the print quality. When the switch is set to normal (quality printing), the data stream commands cannot change the printer to conserve ribbon and decrease the quality of printing.

5219 Operator Panel Lights and Indicators

Power On light: The power supply is producing the required level of voltage.

On Line light: The commands are being received from the work station controller that selected this printer.

Ribbon light: There is no ribbon cartridge in the printer or the ribbon will print less than 200 characters before it reaches the end.

Ready light: The printer is ready to print.

Printer Excep (exception) light: Detected a data stream exception. The seven-segment displays contain a two-digit value that defines the exception detected.

Release light: The pinch feed rollers are not clamping the paper. This indicator can be on only when the Ready light is off.

Setup light: Detected a print setup command that contains allowed setup information. The seven-segment displays contain the setup code from the command.

Load Paper light: The printer needs more paper. If you are using tractor feed and are out of paper when the printer is powered on, the Load Paper light will not indicate paper is needed, but if you are printing and run out of paper, it indicates more paper is needed.

Change Font light: The print wheel needs changing to a different font. The seven-segment displays identify the required print wheel.

Diag Mode light: The 5219 Printer is in diagnostic mode.

Seven-Segment displays: The seven-segment displays indicate what is needed for operator intervention or what caused an error condition. If a clear command is received when the printer is not ready, hex 0A is indicated. Refer to the indicator lights for a description of the conditions that cause a value to be placed in the seven-segment displays.

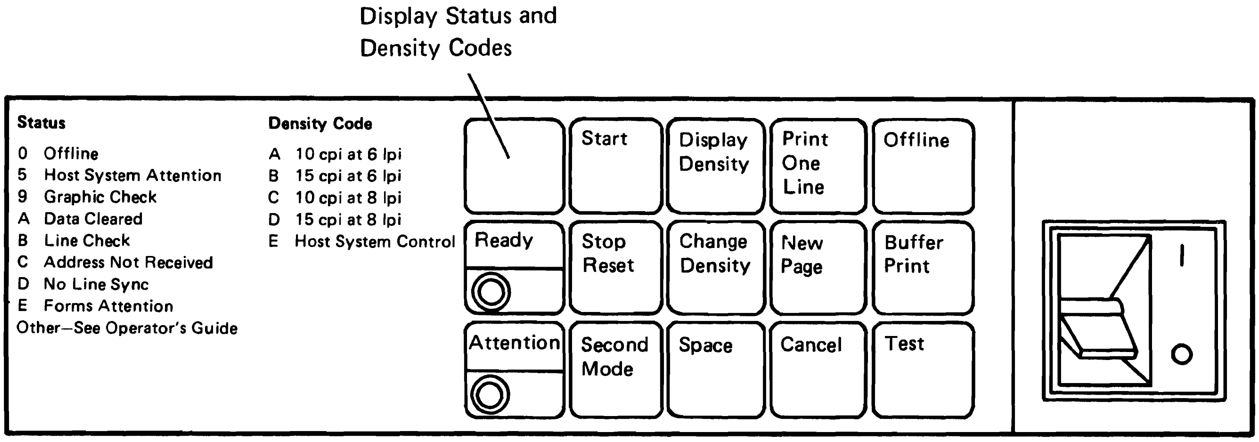
Printer Excep (exception) and Setup lights: When these two indicators are on at the same time, they indicate a mechnical or electrical error condition. The seven-segment display identifies the error condition.

Printer Excep (exception) and Load Paper lights: When these two indicators are on at the same time, they indicate the automatic sheet feeder drawer is empty. The seven-segment display identifies the empty drawer.

Setup and Load Paper lights: When these two indicators are on at the same time, they indicate the detection of a change in the paper feed method. The seven-segment display identifies the new paper feed method required.

5224 Printer Switches, Keys, and Lights

The operator panel on the 5224 Printer contains switches, keys, and lights as shown in Figure 5-5.



Legend
cpi—Characters per inch
lpi—Lines per inch

Figure 5-5. 5224 Printer Operator Panel

5224 Operator Panel Switches and Keys

Power switch: Turns power on or off to the printer. Also starts the power-on test each time the Power switch is set to on.

Start key: If no errors are present and if the power-on test is complete, this key turns on the Ready light and makes the printer ready to perform commands.

Stop/Reset key: Causes the printer to stop after the current operation is ended. Turns the Ready light off and turns the Attention light on. The Stop/Reset key also resets some error conditions.

Second Mode key: Causes the second digit of the 2-digit error code to be displayed after a permanent error. The alternate display occurs only while the key is held down.

Display Density key: Causes the present lines per inch and characters per inch setting (a single hexadecimal number) to be displayed (if no errors are present and the Stop key has been pressed).

Change Density key: Sets the print lines per inch and characters per inch for the printer.

Space key: Causes the carriage to advance a single line if the Ready light is off and no errors are present. This key does not affect the horizontal print position.

Print One Line key: Is used to print a single line (if a print command is being sent to the printer).

New Page key: Causes the carriage to skip to line 1 of the next form and sets the horizontal print position to 1 if the Ready light is off and no errors are present.

Cancel key: Is used to set the cancel request status. The Second Mode key must be held down while the Cancel key is pressed.

Offline key: Puts the printer in offline mode for check out and problem determination.

Buffer Print key: Causes all data to print in the hexadecimal code and to print the corresponding character that the hexadecimal code represents.

Test key: Puts the printer in the test mode for problem determination. Testing is started when the Start key is pressed.

5224 Operator Panel Lights

Attention light: Informs the operator that the printer cannot accept commands from the processor and that the printer requires attention.

Ready light: Turned on by the Start key and turned off by the Stop/Reset key or when any error is present.

Display: A single hexadecimal digit LED indicator is used to display the error codes, lines per inch, and the characters per inch setting. The error codes are listed in the "Work Station Status Bytes and Error Recovery" section in Chapter 10. The Second Mode key is pressed to view the second digit of a 2-digit error code after a permanent error is detected.

If there is no permanent error detected, you can press the Display Density key and the LED indicator shows a 1-digit print character per inch setting.

5225 Printer Switches, Keys, and Lights

The operator panel on the 5225 Printer contains switches, keys, and lights and is shown in Figure 5-6.

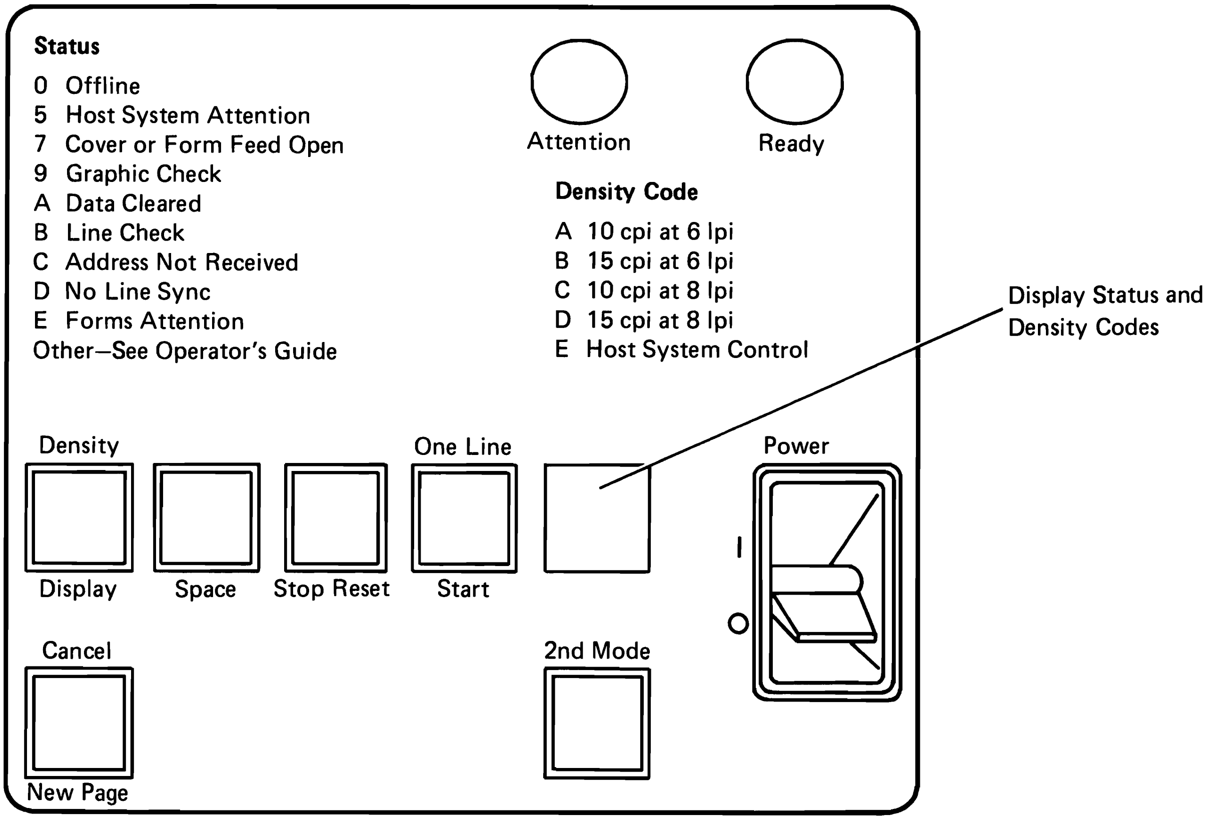


Figure 5-6. 5225 Printer Operator Panel

5225 Operator Panel Switches and Keys

Power switch: Turns power on or off to the printer. Also starts the power-on test each time the Power switch is set to on (|).

Display/Density key: Causes the present lines per inch and characters per inch setting (a single hexadecimal number) to be displayed if no errors are present and the Stop key has been pressed. The Display/Density key can also be used to select the lines per inch and characters per inch setting if the 2nd Mode key is pressed and held first.

Space key: Causes the carriage to advance a single line if the Ready light is off and no errors are present. This key does not affect the horizontal print position.

Stop/Reset key: Causes the printer to stop after the current operation is ended and turns off the Ready light. The Stop/Reset key also resets some error conditions.

Start/One Line key: If no errors are present and if the tests for the power being on are complete, this key turns on the Ready light and makes the printer ready to perform commands. The Start/One Line key can also be used to print a single line (if a print command is being sent to the printer) if the 2nd Mode key is pressed and held first.

Display: Displays the error codes, the lines per inch, and characters per inch setting. The error codes are listed in status byte 10 in the "Work Station Status Bytes and Error Recovery" section in Chapter 10.

New Page/Cancel key: Causes the carriage to skip to line 1 of the next form if the Ready light is off and no errors are present. The New Page/Cancel key also is used to set the cancel request status byte if the 2nd Mode key is first pressed and held.

2nd Mode key: Causes the second digit of the two-digit error code to be displayed after a hard error. Also used with the Display/Density, Start/One Line, and New Page/Cancel keys as described in the previous paragraphs about these keys.

5225 Operator Panel Lights

Attention light: Informs the operator that the printer cannot accept commands from the system and that the printer requires attention.

Ready light: Turned on by the Start/One Line key and turned off by the Stop/Reset key or when any error is present.

5256 Printer Switches, Keys, and Lights

The operator panel on the 5256 Printer contains lights and switches and is shown in Figure 5-7.

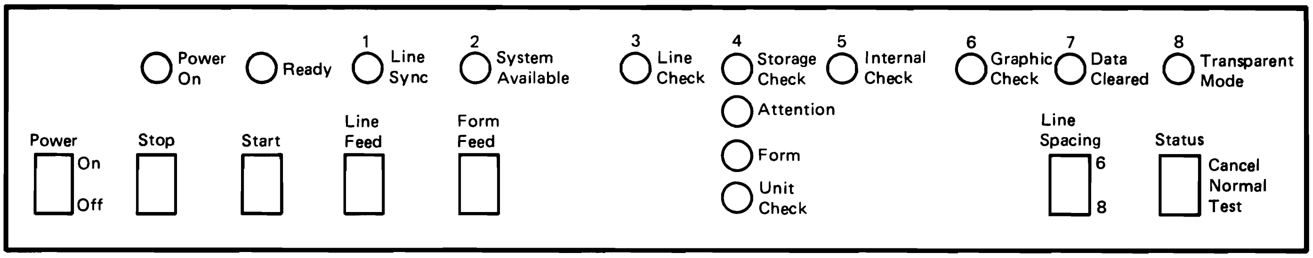


Figure 5-7. 5256 Printer Operator Panel

5256 Operator Panel, Switches, and Keys

Power: Turns the printer on or off.

Stop: Makes the printer not ready and permits the operator to position the forms. The Stop switch *must* be pressed before you position the forms by hand, or the system loses control of the vertical position. If the Stop switch is pressed while the printer is printing, the current line of printing is completed before the printer stops. This switch also resets some printer check conditions.

Start: If the Attention, Form, and Unit Check lights are off, the Start switch makes the printer ready to perform commands.

Line Feed: Permits a single line feed, but before this switch can be used the printer must be not ready; press the Stop switch to make the printer not ready.

The horizontal print position is not affected by the line feed command or the Line Feed switch.

Form Feed: Permits a series of single line feeds to the first line of the next form. The printer must be not ready before the Form Feed switch will work.

Line Spacing: Selects the number of lines to be printed per inch; 6 or 8 lines per inch can be selected. If the printing is 8 lines per inch, some characters might print over other characters; for example, if tall characters are printed one above the other.

Status: Selects online (Normal) or offline (Test) mode. The Cancel position generates a request to cancel the current print operation. The request is reported to the system and a message is displayed.

When in online mode, the printer can respond to any command from the system if the Ready light is on. When in offline mode, the printer does not respond to any commands from the system. Offline mode is used for problem determination.

5256 Operator Panel Lights

The operator panel has five status lights that show the status of the printer and eight dual-purpose lights that display diagnostic program information.

Status Lights

Power On: The power to the printer is on.

Ready: The printer is ready to print data or perform commands from the system.

Attention: Operator action is needed. If the alarm is installed, the alarm is also sounded.

Forms: There is some type of forms problem such as forms jammed or end-of-forms.

Unit Check: A check condition occurred in the printer.

Diagnostic Lights

Each of the eight diagnostic lights shows one of two conditions, depending on the position of the Status switch. The following paragraphs describe the meaning of each light when the printer is online (the Status switch is in the Normal position). The device check status conditions are given in parentheses after the light names; these conditions are indicated when the printer is offline (the Status switch is in the Test position).

Line Sync (wire check): Signals from the controller caused the device to be synchronous with the system. This light is reset by an internally generated signal.

System Available (slow speed check): The printer recognized its own address. This light is reset by an internally generated signal.

Line Check (fast speed check): There was a parity check from the data received from the controller. The line parity status is sent to the system and the light is reset by the system.

Storage Check (left margin check): There was a parity check in the printer controller storage. To reset the light, power to the printer must be turned off.

Internal Check (no emitters): There was a parity check in the printer. To reset the light, power to the printer must be turned off.

Graphic Check (emitter sequence check): A character that cannot be printed was sensed. The printer stops printing.

Data Cleared (forms stopped): A clear command has been received from the system. The Data Cleared light does not come on if the printer is ready.

Transparent Mode (forms position lost): The printer is in a mode of operation which causes the hexadecimal code for each byte of input data to be displayed directly above the output of the character.

5262 Printer Switches, Keys, and Lights

The operator panel on the 5262 Printer contains lights and switches and is shown in Figure 5-8.

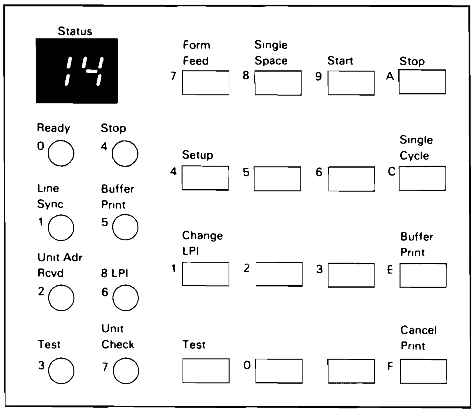


Figure 5-8. 5262 Printer Operator Panel

5262 Operator Panel Switches and Keys

The Emergency Power switch is located on the right side of the 5262 Printer.

Form Feed key: Operates only in stop mode. It causes the printer to perform a single form feed based upon the current definition of presentation surface parameters such as LPI and MPL (default operation is a single line move).

Single Space key: Operates only in stop mode. It causes the printer to perform a single line feed operation, with the logical current print line counter (LCPL) being incremented by one. This key is typamatic, so holding it down will result in multiple line advancements.

Start key: Causes the printer to exit stop mode and enter operating (ready) mode. Normal printing then resumes.

Stop key: Interrupts the current printing operation and places the printer in stop mode. The Ready indicator is turned off, and the stop indicator is turned on. Any data in the print line buffers when the Stop key was pressed will be printed.

Setup key: Operates only in stop mode. Pressing the key causes the line counter to be reset to line 1, then a line of 25 Hs is printed, starting at print position one.

Single Cycle key: Operates only in stop mode. Allows the printer to print a single line. The printer performs all commands received until a print is executed. This function enables the operator to align forms and to advance printing one line at a time from end of forms to out of paper.

Change LPI key: Operates only in stop mode. When pressed, this key changes the current lines per inch from 6 to 8 or 8 to 6; it turns the 8 LPI indicator on if 8 lines per inch is selected and off if 6 lines per inch is selected.

Buffer Print key: Puts the printer in the buffer print mode. All data printed is in hexadecimal code with the character represented by the hexadecimal code printed directly below.

Test key: Used to place the printer in test mode and perform off-line diagnostics.

Cancel Print key: Initiates a request to the host to cancel printing. If the request is accepted, it results in a clear command being sent that stops printing in progress and clears the input buffers. Upon execution, a status code of 59 is momentarily displayed.

Selector Switches: Under the operator panel are two 8-position selector switches. Positions 5 through 8 of the left switch are for language ID selection, and positions 4 through 8 of the right switch select the band image to be loaded into the band image buffer. The print mechanism must be idle (in Test key mode) to load the band image into the buffer.

5262 Operator Panel Lights

Status indicator: The Status Indicator informs the operator of the present condition of the printer, or of some invalid operator action, so that the operator can take appropriate action. The indicator consists of two seven-segment light emitting diodes that display the printer status codes. If a printer operation is in process and no errors have occurred, the Status indicator is blank. Indicator lights may also be on when a status code is displayed.

Note: *An invalid operator panel key selection is signaled by a momentary display of 09 (Operator Check), followed by a display of the previous status code.*

Status Codes	Machine Condition
00-13, 16	Conditions that require operator attention or intervention.
0A	Data cleared.
14	No line activity.
15	No address received.
33, 39	Communication and host-related failures.

59	Cancel key pressed (code momentarily displayed).
d0	Printer is in test mode.
CF	Correct finish of diagnostic test.

Ready: The Ready light indicates that the printer is ready to print. Pressing the Start key causes the Ready light to turn on. The light turns off when the Stop or Test key is pressed, or an error occurs.

Stop: The Stop light indicates that the printer is in stop state. Pressing the Stop key causes the Stop light to turn on, and pressing the Start key causes the Stop light to turn off if no error is present.

Line Sync: The Line Sync light indicates the communications line from the host to the printer is established and ready for communication.

Buffer Print: The Buffer Print light indicates that the printer is performing the buffer print function. To exit from the buffer print function, press the Buffer Print key. To enter or exit from buffer print function, the printer must be in the stop state.

Unit Adr Rcvd: The Unit Address Received light indicates to the operator that the input line is active and that this printer address was received. If the printer does not receive the address in one second, the Unit Address Received light goes off and code 15 is displayed in the Status Indicator.

8 LPI: When the 8 LPI light is on, it indicates that the print line vertical spacing is eight lines per inch. If the light is off, the print line vertical spacing is 6 lines per inch.

Test: The Test light indicates that the printer is offline and in test mode. It is on while the basic assurance test (BAT) is executing, or when the Test key is pressed and a test is in progress. If the Unit Check light is on with the Test light, it indicates that an error occurred during the basic assurance test. The Test light goes off when the test is completed successfully.

Unit Check: The Unit Check light indicates an error condition that may require operator intervention. The Status Indicator displays a code number that identifies the error condition. The Unit Check light and the Status Indicator turn off when the error condition is corrected and the Stop key is pressed.

Audible alarm: Alerts the operator when intervention is required or unit check condition is detected. The alarm can be stopped by pressing the Stop/Reset key. The volume level of the alarm can be controlled by a mechanical adjustment.

5553 or 5557 Operator Panel Switches and Keys

The operator panel on the 5553 or 5557 Printer contains switches, keys, and lights and is shown in Figure 5-9 and Figure 5-10.

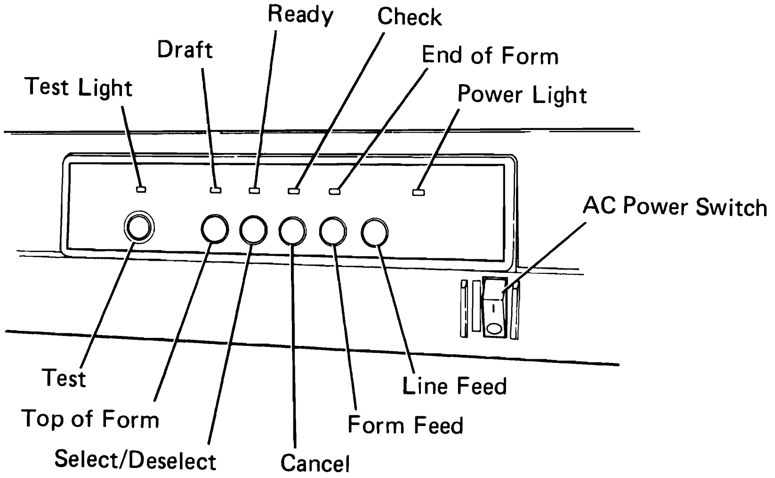


Figure 5-9. 5553 Printer Operator Panel

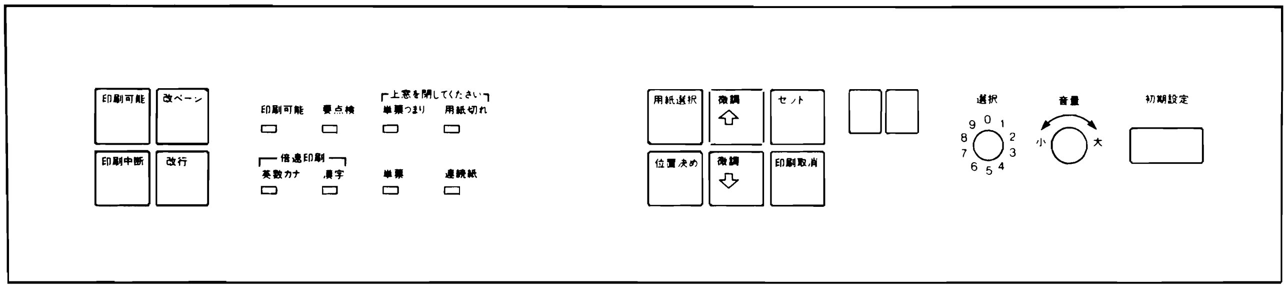


Figure 5-10. 5557 Printer Operator Panel

5553 or 5557 Printer Operator Panel Switches and Keys

Test switch: Puts the printer in test mode to execute printer verification tests. Pressing the switch again ends test mode.

Note: The Test switch is active when the printer is running. Do not press this switch while printing a job.

Top of Form (TOF) Key: Causes the printer to set the current line as the first print line for the form. The TOF switch can only be used when the printer is in the deselect (not ready) mode.

Select/Deselect mode hey: Pressing this key alternately selects the printer (makes it ready) or deselects the printer (makes it not ready). The mode is indicated by the Ready light. Pressing the key while in the select mode stops the printer after the current operation is ended.

Cancel switch: Causes the cancel request status bit to be sent to the host. Cancel request can only be sent when the printer is in the deselect (not ready) mode. When the cancel request is accepted, printing is stopped and the input buffers are cleared.

Forms Feed switch: This switch advances the form to the first print line of the next form. This switch can only be used when the printer is in the deselect (not ready) mode.

Line Feed switch: Causes the carriage to advance the form a single line if the printer is in the deselect (not ready) mode.

AC Power switch: Turns power on or off to the printer. A power-up test is run each time the printer is powered up. The power on light is turned on.

5553 or 5557 Operator Panel Lights

Test light: The printer is in test mode.

Draft light: The printer is in data printing mode when this light is on, and in quality printing mode when the light is off.

Ready light: The printer is ready when the light is on.

Check light: Indicates an error condition. The error codes are listed in the "Work Station Status Bytes and Error Recovery" section in Chapter 11.

End of Form (EOF) light: The printer is out of forms.

Power light: The printer power is on.

Programming Characteristics of Printers

The system program handles all printers the same because each printer attached to the system has an associated printer unit block (PUB). The PUBs, located in real main storage, are chained together on a queue with the PUBs for the local printers at the start of the queue.

The PUBQHDR byte of the PUB, which contains the queue header displacement, points to the associated print queue, QHDPTn. Printers 1, 9, 17, 25 and so on use QHDPT1, printers 2, 10, 18, 26 and so on use QHDPT2. The QHDPTn points to an action control element and the action control element contains the address of the printer's associated input/output block (IOB); this relationship is shown in Figure 5-11. The PUB, IOB, and action control element (ACE) are described in the *System Data Areas* manual.

Note: *The PUBs for remotely attached printers are created on an as-required basis when the remote printer is varied online and are located in main storage after the PUBs for locally attached devices.*

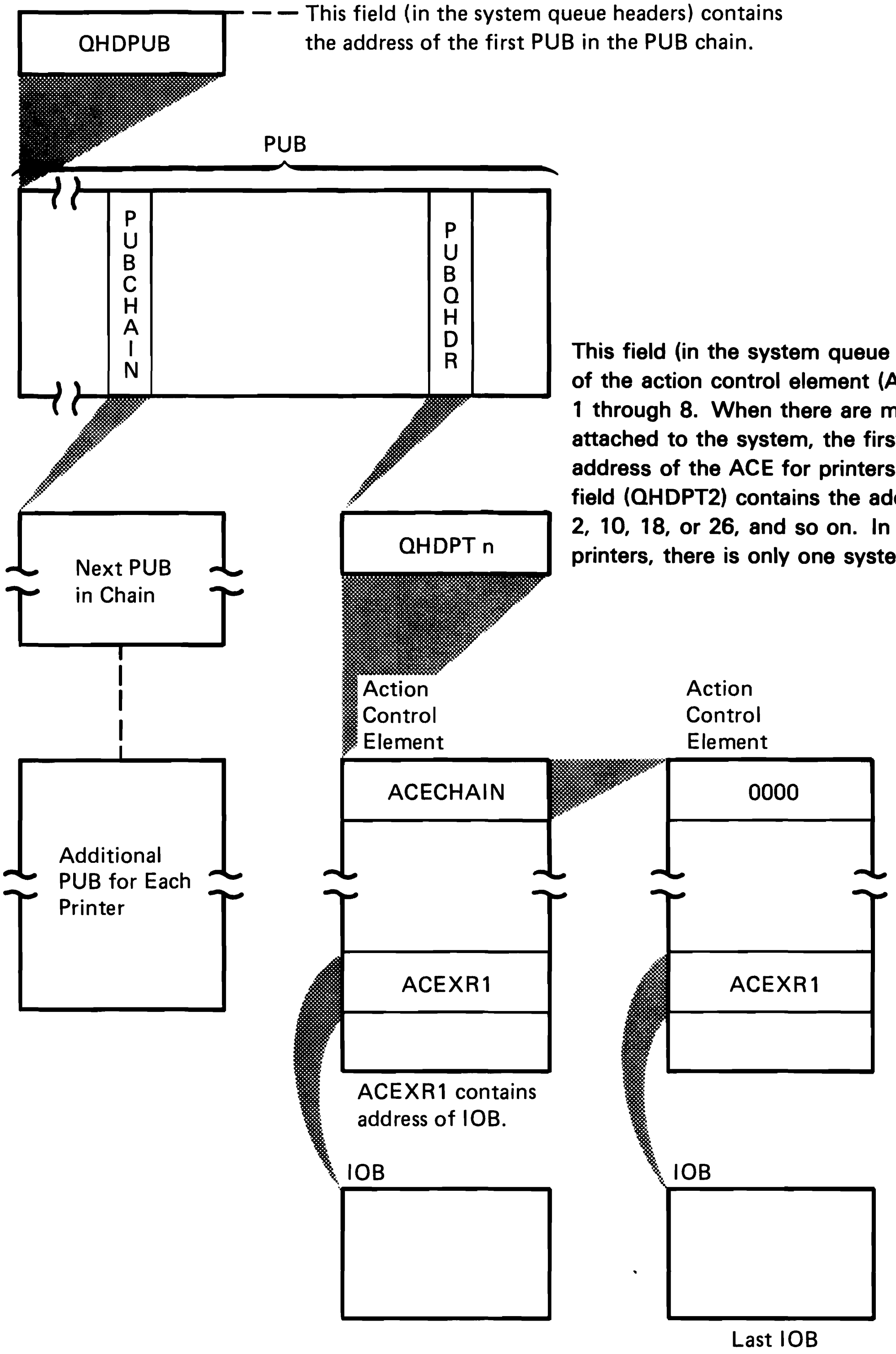
Programming Characteristics of Local and Remote Printers

Program operation of each printer attached to the system is controlled by:

- An input/output block and a printer unit block
- A set of commands that must be assembled by the user's program
- The appropriate supervisor call instruction

Figure 5-12 shows the relationship of the host system to the local work stations and how the IOB, commands, and orders are passed.

Figure 5-13 shows the relationship of the host system to the remote work stations and how the IOB, commands, and orders are passed.



This field (in the system queue headers) contains the address of the first PUB in the PUB chain.

This field (in the system queue headers) contains the address of the action control element (ACE) where n is a number from 1 through 8. When there are more than 8 local printers attached to the system, the first field (QHDPT1) contains the address of the ACE for printers 1, 9, 17, or 25. The second field (QHDPT2) contains the address of the ACE for printers 2, 10, 18, or 26, and so on. In the case of remotely attached printers, there is only one system queue header–QHDRPT.

ACEXR1 contains address of IOB.

Figure 5-11. Relation of PUB to IOB

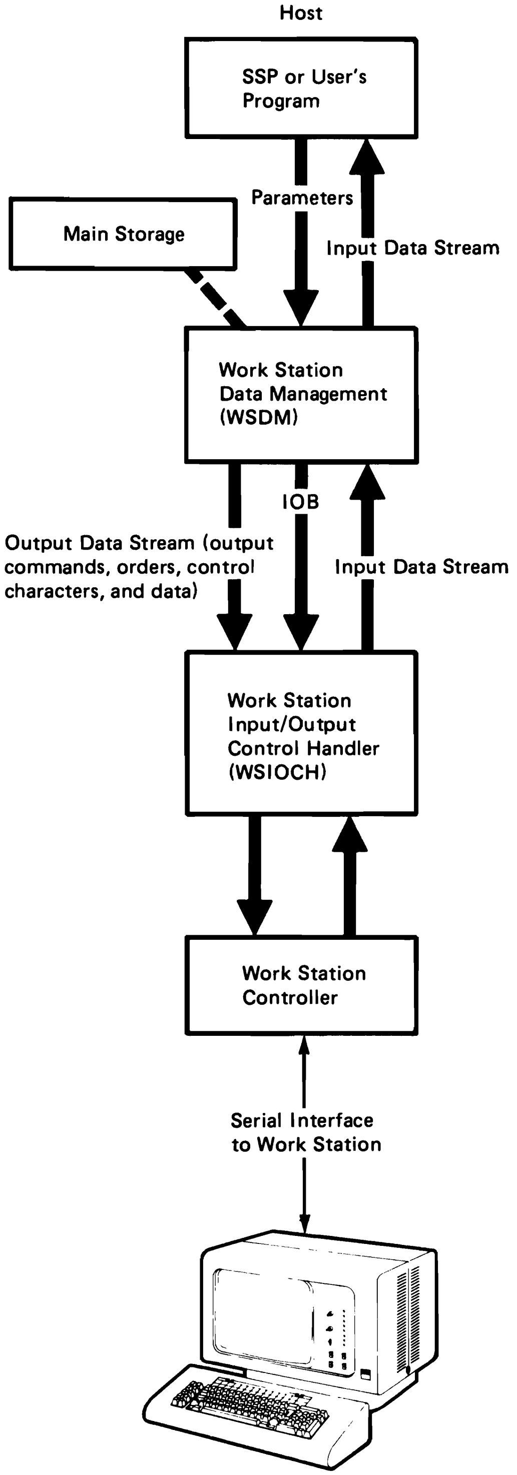

Host
SSP or User's Program
Parameters
Input Data Stream
Main Storage
Work Station Data Management (WSDM)
IOB
Output Data Stream (output commands, orders, control characters, and data)
Input Data Stream
Work Station Input/Output Control Handler (WSIOCH)
Work Station Controller
Serial Interface to Work Station

Figure 5-12. Relationship of Host System to the Local Work Stations

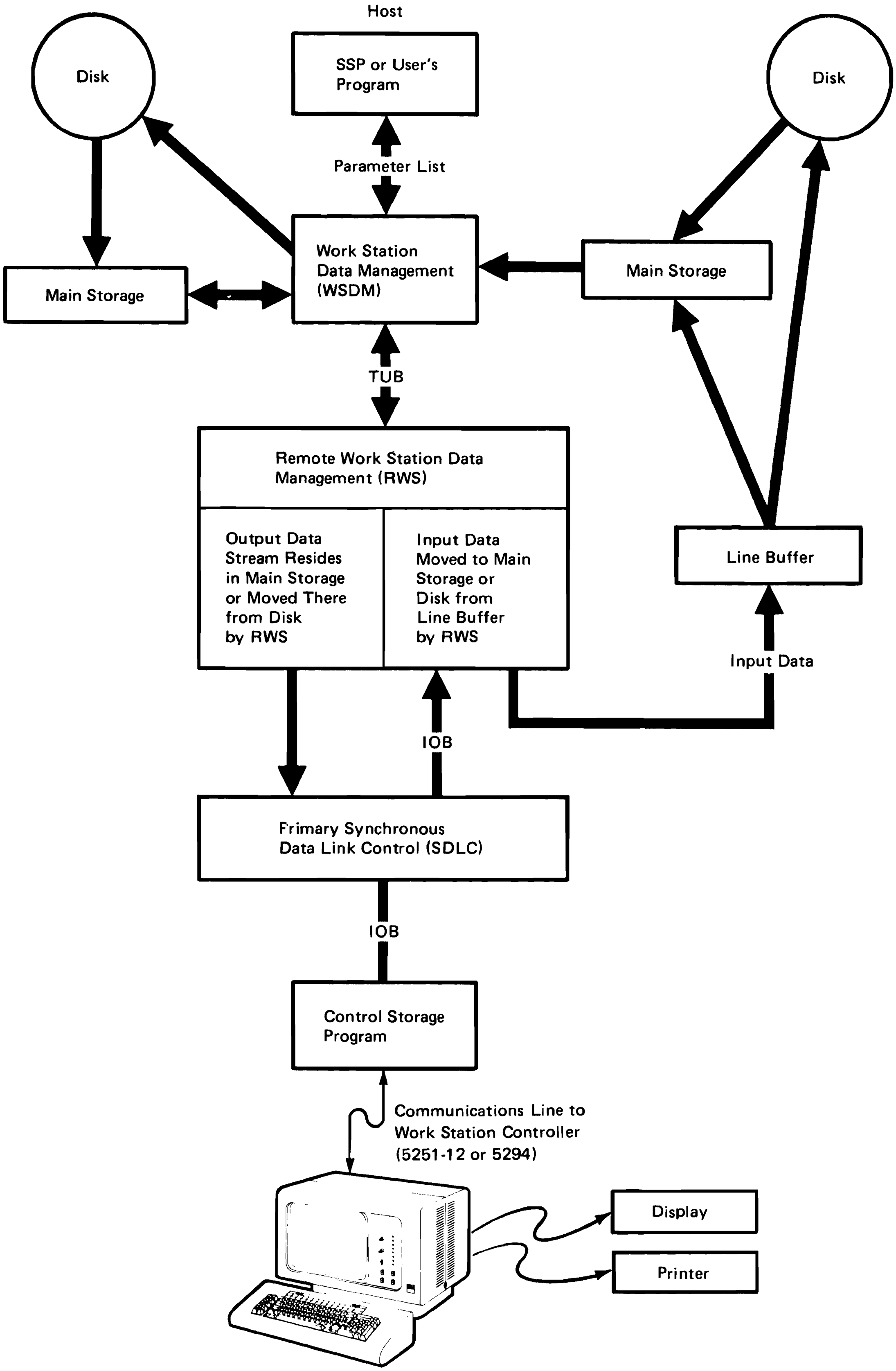

Host
SSP or User's Program
Disk
Disk
Parameter List
Work Station Data Management (WSDM)
Main Storage
Main Storage
TUB
Remote Work Station Data Management (RWS)
Output Data Stream Resides in Main Storage or Moved There from Disk by RWS
Input Data Moved to Main Storage or Disk from Line Buffer by RWS
Line Buffer
Input Data
IOB
Frimary Synchronous Data Link Control (SDLC)
IOB
Control Storage Program
Communications Line to Work Station Controller (5251-12 or 5294)
Display
Printer

Figure 5-13. Relationship of Host System to the Remote Work Stations

Printer Unit Block

For a definition of each bit in the printer unit block refer to the *System Data Areas* manual.

The printer unit block (PUB), located in real main storage, is used by the work station input/output control handler (WSIOCH) routine and the printer input/output control handler (PTIOCH) routine to identify local printers and their associated IOB queues and by the IBM SSP remote work station support to identify remote printers and their associated IOB queues. WSIOCH is common for locally attached display stations and work station attached printers. PTIOCH supports the natively attached 3262 Printer.

Printer Input/Output Block

For a definition of each bit in the input/output block refer to the *System Data Areas* manual.

The IOB contains a command in bytes 0A and 0B of the input/output block (IOB) located in real main storage. Each IOB is queued and sent to the printer by a Supervisor Call instruction. More than one operation may be queued by sending more than one Supervisor Call instruction. See Chapter 3 for a description of the Supervisor Call instructions.

For printer output data stream commands the IOB contains an address of a data stream in main or control storage. This data stream contains the commands to the printer and the data, if any, to be printed. Before using an IOB, the completion code (bits 0 through 4), unit address, and queue header displacement must be copied from the correct printer unit block and the PUB address must be set.

Notes:

1. *The printer IOB must be on an 8-byte boundary.*
2. *When the 3262 Printer is being used, any command or block of data such as a belt image load command or a print line of data cannot extend across more than one buffer boundary.*

The printer input/output block is separate from the printer unit block and has 40 bytes of information. The printer unit block has 96 bytes of information.

Commands

The system controls the printers with a set of commands that are sent to the work station controller and printers. They consist of commands:

- To the controller
- To the printer
- For the printer data stream

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