Series/1

GA34-0034-5

File No. S1-16

IBM Series/1
Reference Summary

IBM

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GA34-0034-5

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IBM Series/1
Reference Summary

Sixth Edition (September 1985)

This is a major revision of, and obsoletes, GA34-0034-4. New information includes:

- 4950 Processor
  - New and modified instructions
  - Modified address key register (AKR).
- 4950/5170 Model 495 Asynchronous Communications
- 4950/5170 Model 495 Disk/Diskette Attachment
- 4971 Printer and the 4201 Proprinter
- Series/1 to PC channel attachment.

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Contents

Section 1. Series/1 Processor

Instructions

List of Instructions by Mnemonic

The instructions are in alphabetical sequence based on assembler mnemonics. See "Assembler Syntax" in this section for syntax definitions.

Symbols used in the list are:

*	Indirect address
**	This instruction is treated as a NOP on the 4954 and 4956 processors.
***	This instruction is modified for 4-bit mode operation on the 4956 processor models E and 60E. See *IBM Series/1 4956 Processor Model E (60E) and Processor Features Description*, GA34-0289 (GA34-0293).
#	This instruction applies to the 4956 processor models E and 60E only. It is intended to be used exclusively by the operating system, and, therefore, does not represent an assembler mnemonic. However, it may be entered in machine code if necessary. See "Hexadecimal List of Instructions" in this section and *IBM Series/1 4956 Processor Model E (60E) and Processor Features Description*, GA34-0289 (GA34-0293).
†	This instruction applies to 4950, 4954, 4955, and 4956 processors that have the floating-point feature installed.
††	This instruction is not used on the 4953 processor.
†††	This instruction applies to the 4950, 4952, 4954, and 4956 processors only.
FT	Format type. The number in this column can be used to find the correct hardware format for the instruction. See "Instruction Format Types" in this section.
&	4950 Emulated Instruction
&&	4950 Emulated Instruction in this syntax only
&&&	4950 Emulated Instruction for storage protect, EOS, and address translation

Mnemonic	Instruction name	Syntax	Ft
AA	Add Address	raddr,reg[,reg]	15
		raddr,addr4	8
AB	Add Byte	reg,addr4	23
		addr4,reg	23
ABI	Add Byte Immediate	byte,reg	1
ACY	Add Carry Register	reg	14
AD&	Add Doubleword	reg,addr4	24
		addr4,reg	24
		addr5,addr4	21
ARIB #	Address Resolution with Indirect Branch		
ARIBON #	Address Resolution with Indirect Branch-On		
ARIBOFF #	Address Resolution with Indirect Branch-Off		
AW	Add Word	reg,reg,	14
		reg,addr4	23
		addr4,reg	23
		addr5,addr4&&	21
		longaddr,reg	13
AWCY	Add Word With Carry	reg,reg	14
AWI	Add Word Immediate	word,reg[,reg]	15
		word,addr4	8
B	Branch Unconditional	longaddr	13
BAL	Branch and Link	longaddr,reg	13
BALS	Branch and Link Short	(reg,jdisp)*	28
		(reg)*	28
		addr*	28
BALX	Branch and Link External	See BAL	
BC	Branch on Condition	cond,longaddr	13
BCC	Branch on Condition Code	cond,longaddr	13
BCY	Branch on Carry	See BC	

Mnemonic	Instruction name	Syntax	Ft
BE	Branch on Equal	See BC	
BER	Branch on Error	See BNCC	
BEV	Branch on Even	See BC	
BGE	Branch on Arithmetically Greater Than or Equal	See BNC	
BGT	Branch on Arithmetically Greater Than	See BNC	
BLE	Branch on Arithmetically Less Than or Equal	See BC	
BLGE	Branch on Logically Greater Than or Equal	See BNC	
BLGT	Branch on Logically Greater Than	See BNC	
BLLE	Branch on Logically Less Than or Equal	See BC	
BLLT	Branch on Logically Less Than	See BC	
BLT	Branch on Arithmetically Less Than	See BC	
BMIX	Branch if Mixed	See BC	
BN	Branch on Negative	See BC	
BNC	Branch on Not Condition	cond,longaddr	13
BNCC	Branch on Not Condition Code	cond,longaddr	13
BNCY	Branch on No Carry	See BNC	
BNE	Branch on Not Equal	See BNC	
BNER	Branch if Not Error	See BCC	
BNEV	Branch on Not Even	See BNC	
BNMIX	Branch if Not Mixed	See BNC	

Mnemonic	**Instruction name**	**Syntax**	**Ft**
BNN	Branch on Not Negative	See BNC	
BNOFF	Branch if Not Off	See BNC	
BNON	Branch if Not On	See BNC	
BNOV	Branch on Not Overflow	longaddr	13
BNP	Branch on Not Positive	See BNC	
BNZ	Branch on Not Zero	See BNC	
BOFF	Branch if Off	See BC	
BON	Branch if On	See BC	
BOV	Branch on Overflow	longaddr	13
BP	Branch on Positive	See BC	
BX	Branch External	vcon (See B)	
BXS	Branch Indexed Short	(reg$^{1-7}$,jdisp)	10
		(reg$^{1-7}$)	10
		addr	10
BZ	Branch on Zero	See BC	
CA	Compare Address	raddr,reg	15
		raddr,addr4	8
CB	Compare Byte	addr4,reg	23
		addr5,addr4&&	17
CBI	Compare Byte Immediate	byte,reg	27
CD&	Compare Doubleword	addr4,reg	24
		addr5,addr4	18
CFED	Compare Byte Field Equal and Decrement	(reg),(reg)	5
CFEN	Compare Byte Field Equal and Increment	(reg),(reg)	5
CFNED	Compare Byte Field Not Equal and Decrement	(reg),(reg)	5

Mnemonic	Instruction name	Syntax	Ft
CFNEN	Compare Byte Field Not Equal and Increment	(reg),(reg)	5
CMR	Complement Register	reg[,reg]	14
CPAKR ††***	Copy Address Key Register	addr4 reg	11 16
CPCL	Copy Current Level	reg	16
CPCLK †††&	Copy Clock	reg	16
CPCMP †††&	Copy Comparator	reg	16
CPCON&	Copy Console Data Buffer	reg	16
CPFLB †&	Copy Floating level Block	freg,addr4	11
CPIMR	Copy Interrupt Mask Register	addr4	11
CPIPF&	Copy In-Process Flags	addr4	11
CPISK††	Copy Instruction Space Key	addr4 reg	11 16
CPLB	Copy Level Block	reg,addr4	11
CPLSR	Copy Level Status Register	reg	14
CPOOK ††	Copy Operand 1 Key	addr4 reg	11 16
CPOTK ††	Copy Operand 2 Key	addr4 reg	11 16
CPPSR ***	Copy Processor Status and Reset	addr4	11
CPSK ††**&	Copy Storage Key	reg,addr4	11
CPSR ††***&	Copy Segmentation Register	reg,addr4	11
CW	Compare Word	reg,reg add4,reg addr5,addr4&&	14 23 17

Mnemonic	Instruction name	Syntax	Ft
CWI	Compare Word Immediate	word,reg word,addr4	15 8
DB&	Divide Byte	addr4,reg	26
DD&	Divide Doubleword	addr4,reg	26
DIAG	Diagnose	ubyte	12
DIS***&&&	Disable	ubyte	12
DW&	Divide Word	addr4,reg	26
EN***&&&	Enable	ubyte	12
FA†&	Floating Add	addr4,freg freg,freg	3 4
FAD†&	Floating Add Double	addr4,freg freg,freg	3 4
FC†&	Floating Compare	freg,freg	4
FCD†&	Floating Compare Double	freg,freg	4
FD†&	Floating Divide	addr4,freg freg,freg	3 4
FDD†&	Floating Divide Double	addr4,freg freg,freg	3 4
FFD	Fill Byte Field and Decrement	reg,(reg)	5
FFN	Fill Byte Field and Increment	reg,(reg)	5
FM†&	Floating Multiply	addr4,freg freg,freg	3 4
FMD†&	Floating Multiply Double	addr4,freg freg,freg	3 4
FMV†&	Floating Move	addr4,freg freg,freg freg,addr4	3 4 3
FMVC†&	Floating Move and Convert	addr4,freg freg,addr4	3 3
FMVCD †&	Floating Move and Convert Double	addr4,freg freg,addr4	3 3
FMVD†&	Floating Move Double	addr4,freg freg,freg freg,addr4	3 4 3

Mnemonic	Instruction name	Syntax	Ft
FS†&	Floating Subtract	addr4,freg	3
		freg,freg	4
FSD†&	Floating Subtract Double	addr4,freg	3
		freg,freg	4
IO	Operate I/O	longaddr	13
IOPK††	Interchange Operand Keys		12
IR	Interchange Registers	reg,reg	14
J	Jump Unconditional	jdisp	10
		jaddr	10
JAL	Jump and Link	jdisp,reg	19
		jaddr,reg	19
JC	Jump on Condition	cond,jdisp	2
		cond,jaddr	2
JCT	Jump on Count	jdisp,reg	22
		jaddr,reg	22
JCY	Jump on Carry	See JC	
JE	Jump on Equal	See JC	
JEV	Jump on Even	See JC	
JGE	Jump on Arithmetically Greater Than or Equal	See JNC	
JGT	Jump on Arithmetically Greater Than	See JNC	
JLE	Jump on Arithmetically Less Than or Equal	See JC	
JLGE	Jump on Logically Greater Than or Equal	See JNC	
JLGT	Jump on Logically Greater Than	See JNC	
JLLE	Jump on Logically Less Than or Equal	See JC	

Mnemonic	Instruction name	Syntax	Ft
JLLT	Jump on Logically Less Than	See JC	
JLT	Jump on Arithmetically Less Than	See JC	
JMIX	Jump if Mixed	See JC	
JN	Jump on Negative	See JC	
JNC	Jump on Not Condition	cond,jdisp cond,jaddr	2 2
JNCY	Jump on No Carry	See JNC	
JNE	Jump on Not Equal	See JNC	
JNEV	Jump on Not Even	See JNC	
JNMIX	Jump if Not Mixed	See JNC	
JNN	Jump on Not Negative	See JNC	
JNOFF	Jump if Not Off	See JNC	
JNON	Jump if Not On	See JNC	
JNP	Jump on Not Positive	See JNC	
JNZ	Jump on Not Zero	See JNC	
JOFF	Jump if Off	See JC	
JON	Jump if On	See JC	
JP	Jump on Positive	See JC	
JZ	Jump on Zero	See JC	
LEX	Level Exit	[ubyte]	12
LMB	Load Multiple and Branch	addr4	7
MB&	Multiply Byte	addr4,reg	26
MD&	Multiply Doubleword	addr4,reg	26
MVA	Move Address	addr4,reg raddr,addr4	7 8
MVB	Move Byte	reg,addr4 addr4,reg addr5,addr4	23 23 17
MVBI	Move Byte Immediate	byte,reg	1
MVBZ	Move Byte and Zero	addr4,reg	23

Mnemonic	Instruction name	Syntax	Ft
MVD	Move Doubleword	reg,addr4&&	24
		addr4,reg&&	24
		addr5,addr4	18
MVDZ&	Move Doubleword and Zero	addr4,reg	24
MVFD	Move Byte Field and Decrement	(reg),(reg)	5
MVFN	Move Byte Field and Increment	(reg),(reg)	5
MVW	Move Word	reg,reg	14
		reg,addr4	23
		addr4,reg	23
		addr5,addr4	17
		reg,longaddr	13
		longaddr,reg	13
MVWI	Move Word Immediate	word,reg	7
		word,addr4	8
MVWS	Move Word Short	reg,shortaddr	20
		shortaddr4,reg	25
MVWZ	Move Word and Zero	addr4,reg	23
MW&	Multiply Word	addr4,reg	26
NOP	No Operation		10
NWI	And Word Immediate	word,reg[,reg]	15
OB	OR Byte	reg,addr4	23
		addr4,reg	23
		addr5,addr4&&	17
OD&	OR Doubleword	reg,addr4	24
		addr4,reg	24
		addr5,addr4	18
OW	OR Word	reg,reg	14
		reg,addr4	23
		addr4,reg	23
		addr5,addr4&&	17
		longaddr,reg	13
OWI	OR Word Immediate	word,reg[,reg]	15
		word,addr4	8
PB	Pop Byte	addr4,reg	26

Mnemonic	Instruction name	Syntax	Ft
PD	Pop Doubleword	addr4,reg	26
PSB	Push Byte	reg,addr4	26
PSD	Push Doubleword	reg,addr4	26
PSW	Push Word	reg,addr4	26
PW	Pop Word	addr4,reg	26
RBTB	Reset Bits Byte	reg,addr4	23
		addr4,reg	23
		addr5,addr4&&	17
RBTD&	Reset Bits Doubleword	reg,addr4	24
		addr4,reg	24
		addr5,addr4	18
RBTW	Reset Bits Word	reg,reg	14
		reg,addr4	23
		addr4,reg	23
		addr5,addr4&&	17
		longaddr,reg	13
RBTWI	Reset Bits Word Immediate	word,reg[,reg]	15
		word,addr4	8
SA	Subtract Address	raddr,reg[,reg]	15
		raddr,addr4	8
SB	Subtract Byte	reg,addr4	23
		addr4,reg	23
SBTB	Set Bits Byte	reg,addr4	23
		addr4,reg	23
		addr5,addr4	17
SBTD	Set Bits Doubleword	reg,addr4	24
		addr4,reg	24
		addr5,addr4	18
SBTW	Set Bits Word	reg,reg	14
		reg,addr4	23
		addr4,reg	23
		addr5,addr4	17
		longaddr,reg	13
SBTWI	Set Bits Word Immediate	word,reg[,reg]	15
		word,addr4	8
SCY	Subtract Carry Indicator	reg	14

Mnemonic	Instruction name	Syntax	Ft
SD&	Subtract Doubleword	reg,addr4	24
		addr4,reg	24
		addr5,addr4	21
SEAKR ††***	Set Address Key Register	addr4	11
		reg	16
SECLK †††&	Set Clock	reg	16
SECMP †††	Set Comparator	reg	16
SECON&	Set Console Data Lights	reg	16
SEFLB †&	Set Floating Level Block	reg,addr4	11
SEIMR	Set Interrupt Mask Register	addr4	11
SEIND	Set Indicators	reg	14
SEISK††	Set Instruction Space Key	addr4	11
		reg	16
SELB	Set Level Block	reg,addr4	11
SEOOK ††	Set Operand 1 Key	addr4	11
		reg	16
SEOTK ††	Set Operand 2 Key	addr4	11
		reg	16
SESK ††**&	Set Storage Key	reg,addr4	11
SESR ††***&	Set Segmentation Register	reg,addr4	11
SFED	Scan Byte Field Equal and Decrement	reg,(reg)	5
SFEN	Scan Byte Field Equal and Increment	reg,(reg)	5
SFNED	Scan Byte Field Not Equal and Decrement	reg,(reg)	5

Mnemonic	Instruction name	Syntax	Ft
SFNEN	Scan Byte Field Not Equal and Increment	reg,(reg)	5
SLC	Shift Left Circular	cnt16,reg	6
		reg,reg&&	14
SLCD&	Shift Left Circular Double	cnt31,reg	6
		reg,reg	14
SLL&	Shift Left Logical	cnt16,reg	6
		reg,reg	14
SLLD&	Shift Left Logical Double	cnt31,reg	6
		reg,reg	14
SLT&	Shift Left and Test	reg,reg	14
SLTD&	Shift Left and Test Double	reg,reg	14
SRA	Shift Right Arithmetic	cnt16,reg	6
		reg,reg&&	14
SRAD&	Shift Right Arithmetic Double	cnt31,reg	6
		reg,reg	14
SRL	Shift Right Logical	cnt16,reg	6
		reg,reg&&	14
SRLD&	Shift Right Logical Double	cnt31,reg	6
		reg,reg	14
STM	Store Multiple	reg, addr4[,abcnt]	8
STOP	Stop	[ubyte]	12
SVC	Supervisor Call	ubyte	12
SW	Subtract Word	reg,reg	14
		reg,addr4	23
		addr4,reg	23
		addr5,addr4&&	21
		longaddr,reg	13
SWCY	Subtract Word With Carry	reg,reg	14
SWI	Subtract Word Immediate	word,addr4	8
		word,reg[,reg]	15
TBT	Test Bit	(reg,bitdisp)	9
TBTR	Test Bit and Reset	(reg,bitdisp)	9

Mnemonic	Instruction name	Syntax	Ft
TBTS	Test Bit and Set	(reg,bitdisp)	9
TBTV	Test Bit and Invert	(reg,bitdisp)	9
TWI	Test Word Immediate	word,reg	15
		word,addr4	8
VR	Invert Register	reg[,reg]	14
XB	Exclusive OR Byte	reg,addr4	23
		addr4,reg	23
XD&	Exclusive OR Doubleword	reg,addr4	24
		addr4,reg	24
XW	Exclusive OR Word	reg,reg	14
		reg,addr4	23
		addr4,reg	23
		longaddr,reg	13
XWI	Exclusive OR Word Immediate	word,reg[,reg]	15

Hexadecimal List of Instructions

The hexadecimal equivalent (four digits) for the first instruction word is shown in the list.

Symbols used in the list are:

(*)	There are two versions of an instruction: direct address and indirect address.
**	This instruction is treated as a NOP by the 4954 and 4956 processo rs.
***	This instruction is modified for 4-bit mode operation on the 4956 processor models E and 60E. See *IBM Series/1 4956 Processor Model E (60E) and Processor Features Description*, GA34-0289 (GA34-0293).
#	This instruction applies to the 4956 processor models E and 60E only. It is intended to be used exclusively by the operating system, and, therefore, does not represent an assembler mnemonic. However, it may be entered in machine code if necessary. See *IBM Series/1 4956 Processor Model E (60E) and Processor Features Description*, GA34-0289 (GA34-0293).
%	Even hexadecimal digit
@	Odd hexadecimal digit
X	Any hexadecimal digit
†	This instruction applies to the 4950, 4954, 4955, and 4956 processors that have the floating-point feature installed.
††	This instruction is not used on the 4953 processor.
†††	This instruction applies to the 4950, 4952, 4954, and 4956 processors only.
FT	The number in the FT column refers to an instruction format type. See "Instruction Format Types" in this section.

Some of the branch and jump instructions have versions of the assembler syntax that are not shown. See "Assembler Syntax" in this section for syntax definitions.

Extended mnemonics are not shown in the chart. See the list on the following page.

Instruction	**Extended mnemonics**
B	BX
BAL	BALX
BC	BCY, BE, BEV, BLE, BLLE, BLLT, BLT, BMIX, BN, BOFF, BON, BP, BZ
BCC	BNER
BNC	BGE, BGT, BLGE, BLGT, BNCY, BNE, BNEV, BNMIX, BNN, BNOFF, BNON, BNP, BNZ
BNCC	BER
CPAKR	CPISK, CPOOK, CPOTK
JC	JCY, JE, JEV, JLE, JLLE, JLLT, JLT, JMIX, JN, JOFF, JON, JP, JZ
JNC	JGE, JGT, JLGE, JLGT, JNCY, JNE, JNEV, JNMIX, JNN, JNOFF, JNON, JNP, JNZ
SEAKR	SEISK, SEOOK, SEOTK

Hexadecimal digits				*Mnemonic*	*Syntax*	*FT*
0	0–7	X	X	ABI	byte,reg	1
0	8–F	X	X	MVBI	byte,reg	1
1	0–7	X	X	JC	cond,jdisp	2
1	8–F	X	X	JNC	cond,jdisp	2
2	0–3	X	0	FA†	addr4,freg	3
2	0–3	X	1	FAD†	addr4,freg	3
2	0–3	X	2	FS†	addr4,freg	3
2	0–3	X	3	FSD†	addr4,freg	3
2	0–3	X	4	FM†	addr4,freg	3
2	0–3	X	5	FMD†	addr4,freg	3
2	0–3	X	6	FD†	addr4,freg	3
2	0–3	X	7	FDD†	addr4,freg	3
2	0–3	X	8	FMVC†	addr4,freg	3
2	0–3	X	9	FMVCD†	addr4,freg	3
2	0–3	X	A	FMV†	addr4,freg	3
2	0–3	X	B	FMVD†	addr4,freg	3
2	0–3	X	C	FMVC†	freg,addr4	3
2	0–3	X	D	FMVCD†	freg,addr4	3
2	0–3	X	E	FMV†	freg,addr4	3
2	0–3	X	F	FMVD†	freg,addr4	3
2	4–7	X	0	FA†	freg,freg	4
2	4–7	X	1	FAD†	freg,freg	4
2	4–7	X	2	FS†	freg,freg	4
2	4–7	X	3	FSD†	freg,freg	4
2	4–7	X	4	FM†	freg,freg	4
2	4–7	X	5	FMD†	freg,freg	4
2	4–7	X	6	FD†	freg,freg	4
2	4–7	X	7	FDD†	freg,freg	4
2	4–7	X	8	FMV†	freg,freg	4
2	4–7	X	9	FMVD†	freg,freg	4
2	4–7	X	A	FC†	freg,freg	4
2	4–7	X	B	FCD†	freg,freg	4
2	4–7	X	C	invalid		4
2	4–7	X	D	invalid		4

Hexadecimal digits				*Mnemonic*	*Syntax*	*FT*
2	4–7	X	E	invalid		4
2	4–7	X	F	invalid		4
2	8–F	X	0	MVFD	(reg),(reg)	5
2	8–F	X	1	invalid		5
2	8–F	X	2	CFNED	(reg),(reg)	5
2	8–F	X	3	CFED	(reg),(reg)	5
2	8–F	X	4	MVFN	(reg),(reg)	5
2	8–F	X	5	invalid		5
2	8–F	X	6	CFNEN	(reg),(reg)	5
2	8–F	X	7	CFEN	(reg),(reg)	5
2	8–F	X	8	FFD	reg,(reg)	5
2	8–F	X	9	invalid		5
2	8–F	X	A	SFNED	reg,(reg)	5
2	8–F	X	B	SFED	reg,(reg)	5
2	8–F	X	C	FFN	reg,(reg)	5
2	8–F	X	D	invalid		5
2	8–F	X	E	SFNEN	reg,(reg)	5
2	8–F	X	F	SFEN	reg,(reg)	5
3	0–7	X	0	SLC	cnt16,reg	6
3	0–7	X	1	SLL	cnt16,reg	6
3	0–7	X	2	SRL	cnt16,reg	6
3	0–7	X	3	SRA	cnt16,reg	6
3	0–7	X	4	SLCD	cnt31,reg	6
3	0–7	X	5	SLLD	cnt31,reg	6
3	0–7	X	6	SRLD	cnt31,reg	6
3	0–7	X	7	SRAD	cnt31,reg	6
3	0–7	X	8	SLC	cnt16,reg	6
3	0–7	X	9	SLL	cnt16,reg	6
3	0–7	X	A	SRL	cnt16,reg	6
3	0–7	X	B	SRA	cnt16,reg	6
3	0–7	X	C	SLCD	cnt31,reg	6
3	0–7	X	D	SLLD	cnt31,reg	6
3	0–7	X	E	SRLD	cnt31,reg	6
3	0–7	X	F	SRAD	cnt31,reg	6
3	8–F	X	X	invalid		

Hexadecimal digits				*Mnemonic*	*Syntax*	*FT*
4	0	X	0	MVA	addr,addr4	8
4	0	X	0	MVWI	word,addr4	8
4	0–7	X	1	invalid		8
4	0–7	X	2	invalid		8
4	0–7	X	3	invalid		8
4	0–7	X	4	MVA	raddr4,reg	7
4	0–7	X	4	MVWI	word,reg	7
4	0–7	X	5	invalid		8
4	0–7	X	6	invalid		8
4	0–7	X	7	invalid		8
4	0	X	8	STM	reg,addr4[,abcnt]	8
4	0	X	9	AWI	word,addr4	8
4	0	X	9	AA	raddr,addr4	8
4	0	X	A	LMB	addr4	7
4	0	X	B	TWI	word,addr4	8
4	0	X	C	OWI	word,addr4	8
4	0	X	C	SBTWI	word,addr4	8
4	0	X	D	RBTWI	word,addr4	8
4	0	X	E	SWI	word,addr4	8
4	0	X	E	SA	raddr,addr4	8
4	0	X	F	CWI	word,addr4	8
4	0	X	F	CA	raddr,addr4	8
4	8–F	0–3	X	TBT	(reg,bitdisp)	9
4	8–F	4–7	X	TBTS	(reg,bitdisp)	9
4	8–F	8–B	X	TBTR	(reg,bitdisp)	9
4	8–F	C–F	X	TBTV	(reg,bitdisp)	9
5	0	0	0	NOP		10
5	0	X	X	J	jdisp	10
5	1–7	X	X	BXS	(reg$^{1-7}$,jdisp)	10
5	8	X	0	SEIMR	addr4	11
5	8–F	X	1	SESR ††***	reg,addr4	11
5	8–B	X	2	SEAKR ††***	addr4	11
5	8–F	X	3	SEFLB†	reg,addr4	11
5	8–F	X	4	SESK††**	reg,addr4	11
5	8–F	X	5	invalid		11
5	8–F	X	6	SELB	reg,addr4	11
5	8–F	X	7	invalid		11

Hexadecimal digits				*Mnemonic*	*Syntax*	*FT*
5	8	X	8	CPIMR	addr4	11
5	8–F	X	9	CPSR ††***	reg,addr4	11
5	8–B	X	A	CPAKR ††***	addr4	11
5	8–F	X	B	CPFLB†	reg,addr4	11
5	8–F	X	C	CPSK††**	reg,addr4	11
5	8	X	D	CPIPF	addr4	11
5	8–F	X	E	CPLB	reg,addr4	11
5	8	X	F	CPPSR***	addr4	11
6	0	X	X	SVC	ubyte	12
6	1	X	X	LEX	[ubyte]	12
6	2	X	X	EN***	ubyte	12
6	3	X	X	DIS***	ubyte	12
6	4	X	X	STOP	[ubyte]	12
6	5	X	X	DIAG	ubyte	12
6	6	X	X	IOPK††		12
6	7	X	X	invalid		12
6	8–F	X	0	BC	cond,longaddr(*)	13
6	8–F	X	1	BNC	cond,longaddr(*)	13
6	8	X	2	B	longaddr(*)	13
6	8–F	X	3	BAL	longaddr(*),reg	13
6	8–F	X	4	BCC	cond,longaddr(*)	13
6	8–F	X	5	BNCC	cond,longaddr(*)	13
6	8	X	6	BOV	longaddr(*)	13
6	8	X	7	BNOV	longaddr(*)	13
6	8–F	X	8	MVW	longaddr(*),reg	13
6	8–F	X	9	OW	longaddr(*),reg	13
6	8–F	X	9	SBTW	longaddr(*),reg	13
6	8–F	X	A	RBTW	longaddr(*),reg	13
6	8–F	X	B	XW	longaddr(*),reg	13
6	8	X	C	IO	longaddr(*)	13
6	8–F	X	D	MVW	reg,longaddr(*)	13
6	8–F	X	E	AW	longaddr(*),reg	13
6	8–F	X	F	SW	longaddr(*),reg	13
7	0–7	%	0	RBTW	reg,reg	14
7	0–7	%	1	OW	reg,reg	14
7	0–7	%	1	SBTW	reg,reg	14
7	0	%	2	SCY	reg	14

Hexadecimal digits				*Mnemonic*	*Syntax*	*FT*
7	0–7	%	3	XW	reg,reg	14
7	0–7	%	4	MVW	reg,reg	14
7	0–7	%	5	CW	reg,reg	14
7	0–7	%	6	CMR	reg[,reg]	14
7	0–7	%	7	IR	reg,reg	14
7	0–7	%	8	AW	reg,reg	14
7	0–7	%	9	AWCY	reg,reg	14
7	0–7	%	A	SW	reg,reg	14
7	0–7	%	B	SWCY	reg,reg	14
7	0	%	C	ACY	reg	14
7	0–7	%	D	VR	reg[,reg]	14
7	0	%	E	CPLSR	reg	14
7	0	%	F	SEIND	reg	14
7	0–7	@	0	SLC	reg,reg	14
7	0–7	@	1	SLL	reg,reg	14
7	0–7	@	2	SRL	reg,reg	14
7	0–7	@	3	SRA	reg,reg	14
7	0–7	@	4	SLCD	reg,reg	14
7	0–7	@	5	SLLD	reg,reg	14
7	0–7	@	6	SRLD	reg,reg	14
7	0–7	@	7	SRAD	reg,reg	14
7	0–7	@	8	invalid		14
7	0–7	@	9	SLT	reg,reg	14
7	0–7	@	A	invalid		14
7	0–7	@	B	invalid		14
7	0–7	@	C	invalid		14
7	0–7	@	D	SLTD	reg,reg	14
7	0–7	@	E	invalid		14
7	0–7	@	F	invalid		14
7	8	8	E	ARIBON#		
7	8	8	E	ARIBOFF#		
7	8	8	F	ARIB#		
7	8–F	%	0	NWI	word,reg[,reg]	15
7	8–F	%	1	AWI	word,reg[,reg]	15
7	8–F	%	1	AA	raddr,reg[,reg]	15
7	8–F	%	2	SWI	word,reg[,reg]	15
7	8–F	%	2	SA	raddr,reg[,reg]	15
7	8–F	%	3	OWI	word,reg[,reg]	15
7	8–F	%	3	SBTWI	word,reg[,reg]	15
7	8–F	%	4	RBTWI	word,reg[,reg]	15

Hexadecimal digits				*Mnemonic*	*Syntax*	*FT*
7	8–F	%	5	XWI	word,reg[,reg]	15
7	8–F	0	7	TWI	word,reg	15
7	8–F	%	8	invalid		15
7	8–F	%	9	invalid		15
7	8–F	%	A	invalid		15
7	8–F	%	B	invalid		15
7	8–F	%	C	invalid		15
7	8–F	%	D	invalid		15
7	8–F	%	E	invalid		15
7	8–F	%	F	invalid		15
7	8	@	0	SECON	reg	16
7	8–F	@	1	invalid		16
7	8–B	@	2	SEAKR ††***	reg	16
7	8–F	@	3	invalid		16
7	8	@	4	SECLK†††	reg	16
7	8–F	@	4	invalid		16
7	8	@	5	SECMP†††	reg	16
7	8–F	@	5	invalid		16
7	8–F	@	6	invalid		16
7	8–F	@	7	invalid		16
7	8	@	8	CPCON	reg	16
7	8	@	9	CPCL	reg	16
7	8–B	@	A	CPAKR ††***	reg	16
7	8–F	@	B	invalid		16
7	8	@	C	CPCLK†††	reg	16
7	8–F	@	C	invalid		16
7	8	@	D	CPCMP†††	reg	16
7	8–F	@	D	invalid		16
7	8–F	@	E	invalid		16
7	8–F	@	F	invalid		16
8	0–7	X	0	MVB	addr5,addr4	17
8	0–7	X	1	OB	addr5,addr4	17
8	0–7	X	1	SBTB	addr5,addr4	17
8	0–7	X	2	RBTB	addr5,addr4	17
8	0–7	X	3	CB	addr5,addr4	17
8	0–7	X	4	MVB	addr5,addr4	17
8	0–7	X	5	OB	addr5,addr4	17
8	0–7	X	5	SBTB	addr5,addr4	17
8	0–7	X	6	RBTB	addr5,addr4	17

Hexadecimal digits				*Mnemonic*	*Syntax*	*FT*
8	0–7	X	7	CB	addr5,addr4	17
8	0–7	X	8	MVB	addr5,addr4	17
8	0–7	X	9	OB	addr5,addr4	17
8	0–7	X	9	SBTB	addr5,addr4	17
8	0–7	X	A	RBTB	addr5,addr4	17
8	0–7	X	B	CB	addr5,addr4	17
8	0–7	X	C	MVB	addr5,addr4	17
8	0–7	X	D	OB	addr5,addr4	17
8	0–7	X	D	SBTB	addr5,addr4	17
8	0–7	X	E	RBTB	addr5,addr4	17
8	0–7	X	F	CB	addr5,addr4	17
8	8–F	X	0	MVW	addr5,addr4	17
8	8–F	X	1	OW	addr5,addr4	17
8	8–F	X	1	SBTW	addr5,addr4	17
8	8–F	X	2	RBTW	addr5,addr4	17
8	8–F	X	3	CW	addr5,addr4	17
8	8–F	X	4	MVW	addr5,addr4	17
8	8–F	X	5	OW	addr5,addr4	17
8	8–F	X	5	SBTW	addr5,addr4	17
8	8–F	X	6	RBTW	addr5,addr4	17
8	8–F	X	7	CW	addr5,addr4	17
8	8–F	X	8	MVW	addr5,addr4	17
8	8–F	X	9	OW	addr5,addr4	17
8	8–F	X	9	SBTW	addr5,addr4	17
8	8–F	X	A	RBTW	addr5,addr4	17
8	8–F	X	B	CW	addr5,addr4	17
8	8–F	X	C	MVW	addr5,addr4	17
8	8–F	X	D	OW	addr5,addr4	17
8	8–F	X	D	SBTW	addr5,addr4	17
8	8–F	X	E	RBTW	addr5,addr4	17
8	8–F	X	F	CW	addr5,addr4	17
9	0–7	X	0	MVD	addr5,addr4	18
9	0–7	X	1	OD	addr5,addr4	18
9	0–7	X	1	SBTD	addr5,addr4	18
9	0–7	X	2	RBTD	addr5,addr4	18
9	0–7	X	3	CD	addr5,addr4	18
9	0–7	X	4	MVD	addr5,addr4	18
9	0–7	X	5	OD	addr5,addr4	18

Hexadecimal digits				*Mnemonic*	*Syntax*	*FT*
9	0–7	X	5	SBTD	addr5,addr4	18
9	0–7	X	6	RBTD	addr5,addr4	18
9	0–7	X	7	CD	addr5,addr4	18
9	0–7	X	8	MVD	addr5,addr4	18
9	0–7	X	9	OD	addr5,addr4	18
9	0–7	X	9	SBTD	addr5,addr4	18
9	0–7	X	A	RBTD	addr5,addr4	18
9	0–7	X	B	CD	addr5,addr4	18
9	0–7	X	C	MVD	addr5,addr4	18
9	0–7	X	D	OD	addr5,addr4	18
9	0–7	X	D	SBTD	addr5,addr4	18
9	0–7	X	E	RBTD	addr5,addr4	18
9	0–7	X	F	CD	addr5,addr4	18
9	8–F	X	X	JAL	jdisp,reg	19
A	0–7	X	X	MVWS	reg,shortaddr(*)	20
A	8–F	X	0	AW	addr5,addr4	21
A	8–F	X	1	SW	addr5,addr4	21
A	8–F	X	2	AD	addr5,addr4	21
A	8–F	X	3	SD	addr5,addr4	21
A	8–F	X	4	AW	addr5,addr4	21
A	8–F	X	5	SW	addr5,addr4	21
A	8–F	X	6	AD	addr5,addr4	21
A	8–F	X	7	SD	addr5,addr4	21
A	8–F	X	8	AW	addr5,addr4	21
A	8–F	X	9	SW	addr5,addr4	21
A	8–F	X	A	AD	addr5,addr4	21
A	8–F	X	B	SD	addr5,addr4	21
A	8–F	X	C	AW	addr5,addr4	21
A	8–F	X	D	SW	addr5,addr4	21
A	8–F	X	E	AD	addr5,addr4	21
A	8–F	X	F	SD	addr5,addr4	21
B	0–7	X	X	invalid		
B	8–F	X	X	JCT	jdisp,reg	22
C	0–7	X	0	MVB	addr4,reg	23
C	0–7	X	1	OB	addr4,reg	23

Hexadecimal digits				*Mnemonic*	*Syntax*	*FT*
C	0–7	X	1	SBTB	addr4,reg	23
C	0–7	X	2	RBTB	addr4,reg	23
C	0–7	X	3	XB	addr4,reg	23
C	0–7	X	4	CB	addr4,reg	23
C	0–7	X	5	MVBZ	addr4,reg	23
C	0–7	X	6	AB	addr4,reg	23
C	0–7	X	7	SB	addr4,reg	23
C	0–7	X	8	MVB	reg,addr4	23
C	0–7	X	9	OB	reg,addr4	23
C	0–7	X	9	SBTB	reg,addr4	23
C	0–7	X	A	RBTB	reg,addr4	23
C	0–7	X	B	XB	reg,addr4	23
C	0–7	X	C	unused		23
C	0–7	X	D	unused		23
C	0–7	X	E	AB	reg,addr4	23
C	0–7	X	F	SB	reg,addr4	23
C	8–F	X	0	MVW	addr4,reg	23
C	8–F	X	1	OW	addr4,reg	23
C	8–F	X	1	SBTW	addr4,reg	23
C	8–F	X	2	RBTW	addr4,reg	23
C	8–F	X	3	XW	addr4,reg	23
C	8–F	X	4	CW	addr4,reg	23
C	8–F	X	5	MVWZ	addr4,reg	23
C	8–F	X	6	AW	addr4,reg	23
C	8–F	X	7	SW	addr4,reg	23
C	8–F	X	8	MVW	reg,addr4	23
C	8–F	X	9	OW	reg,addr4	23
C	8–F	X	9	SBTW	reg,addr4	23
C	8–F	X	A	RBTW	reg,addr4	23
C	8–F	X	B	XW	reg,addr4	23
C	8–F	X	C	unused		23
C	8–F	X	D	unused		23
C	8–F	X	E	AW	reg,addr4	23
C	8–F	X	F	SW	reg,addr4	23
D	0–7	X	0	MVD	addr4,reg	24
D	0–7	X	1	OD	addr4,reg	24
D	0–7	X	1	SBTD	addr4,reg	24

Hexadecimal digits				*Mnemonic*	*Syntax*	*FT*
D	0–7	X	2	RBTD	addr4,reg	24
D	0–7	X	3	XD	addr4,reg	24
D	0–7	X	4	CD	addr4,reg	24
D	0–7	X	5	MVDZ	addr4,reg	24
D	0–7	X	6	AD	addr4,reg	24
D	0–7	X	7	SD	addr4,reg	24
D	0–7	X	8	MVD	reg,addr4	24
D	0–7	X	9	OD	reg,addr4	24
D	0–7	X	9	SBTD	reg,addr4	24
D	0–7	X	A	RBTD	reg,addr4	24
D	0–7	X	B	XD	reg,addr4	24
D	0–7	X	C	unused		24
D	0–7	X	D	unused		24
D	0–7	X	E	AD	reg,addr4	24
D	0–7	X	F	SD	reg,addr4	24
D	8–F	X	X	invalid		24
E	0–7	X	X	MVWS	shortaddr(*),reg	25
E	8–F	X	0	PSB	reg,addr4	26
E	8–F	X	1	MB	addr4,reg	26
E	8–F	X	2	DB	addr4,reg	26
E	8–F	X	3	PB	addr4,reg	26
E	8–F	X	4	PSW	reg,addr4	26
E	8–F	X	5	MW	addr4,reg	26
E	8–F	X	6	DW	addr4,reg	26
E	8–F	X	7	PW	addr4,reg	26
E	8–F	X	8	PSD	reg,addr4	26
E	8–F	X	9	MD	addr4,reg	26
E	8–F	X	A	DD	addr4,reg	26
E	8–F	X	B	PD	addr4,reg	26
E	8–F	X	C	invalid		26
E	8–F	X	D	invalid		26
E	8–F	X	E	invalid		26
E	8–F	X	F	invalid		26
F	0–7	X	X	CBI	byte,reg	27
F	8–F	X	X	BALS	(reg,jdisp)*	28

Assembler Syntax

Coding Notes

1. Data flow, when it modifies a field, is always from left to right.
2. Registers used in effective address calculations are always in parentheses.
3. An address specification followed by an asterisk indicates indirect addressing. Here, the effective address is the contents of the addressed storage location.
4. The *(reg)+* format indicates that, after use, the contents of *reg* are increased by the number of bytes addressed.

Legend for Machine Instruction Operands

abcnt	An absolute value or expression representing the size of a work storage area to be allocated by the Store Multiple (STM) instruction. The value you code must be an even number in the range 0 to 16382.	
addr	An address value. Code an absolute or relocatable expression in the range 0 to 65535.	
addr4	An address value that you code in one of the following forms:	
	(reg^{0-3})	The effective address is the contents of the register reg^{0-3}.
	(reg^{0-3})+	The effective address is the contents of the register reg^{0-3}. After an instruction uses it, the contents of the register are increased by the number of bytes addressed by the instruction.

addr	The effective address is the value of *addr*, unless the instruction and *addr* are within the range of the same USING statement. If they are, the assembler computes the effective address as a displacement (-32768 to +32767 or 0 to 65535) from the base register, which must be reg$^{1-3}$.
addr*	The effective address is the contents of storage at the address defined by *addr*, unless the instruction and *addr* are within the domain and range of the same USING statement. If they are, the assembler computes the effective address as the contents of storage at the address defined by a displacement (0 to 255) from the base register, which must be reg$^{1-3}$.
disp(addr)*	If the instruction is in the domain of a USING directive and the operand is in the range of the same USING directive, then the assembler will compute the displacement and register combination which will reference the requested location; that is, the resulting addressing mode will be disp1(reg$^{1-3}$,disp2)*.

(reg^{1-3},waddr)	The effective address is the contents of the register reg^{1-3}, added to the value of *waddr.*
disp1(reg^{1-3},disp2)*	The effective address is calculated as follows: The contents of the register reg^{1-3} are added to the value of the displacement *disp2* to form an address. The contents of that storage location are added to the value of *disp1* to form the effective address.
disp(reg^{1-3})*	The effective address is the contents of storage at the address defined by the contents of reg^{1-3}, added to the value of *disp.*
(reg^{1-3})*	The effective address is the contents of storage at the address defined by the contents of reg^{1-3}.
(reg^{1-3},disp)*	The contents of reg^{1-3} are added to *disp*, forming an address. The contents of storage at that address form the effective address.

For byte addressing, the effective address can be even or odd. For word or doubleword addressing, the effective address must be even.

addr5	An address value that you code in one of the following forms:

(reg)	The effective address is the contents of the register *reg.*

(reg)+	The effective address is the contents of the register *reg*. After an instruction uses it, the contents of the register are increased by the number of bytes addressed by the instruction.
addr	The effective address is the value of *addr*, unless the instruction and *addr* are within the domain and range of the same USING statement. If they are, the assembler computes the effective address as a displacement (-32768 to +32767 or 0 to 65535) from the base register, which must be reg$^{1-7}$.
addr*	The effective address is the contents of storage at the addressed defined by *addr*, unless the instruction and *addr* are within the domain and range of the same USING statement. If they are, the assembler computes the effective address as the contents of storage at the address defined by a displacement (0 to 255) from the base register, which must be reg$^{1-7}$.

disp(addr)*	If the instruction is in the domain of a USING directive and the operand is in the range of the same USING directive, then the assembler will compute the displacement and register combination which will reference the requested location; that is, the resulting addressing mode will be disp1(reg$^{1-7}$,disp2)*.
(reg$^{1-7}$,waddr)	The effective address is the contents of *reg*$^{1-7}$, added to the value of *waddr*.
disp1(reg$^{1-7}$,disp2)*	The effective address is calculated as follows: The contents of the register *reg*$^{1-7}$ are added to the value of the displacement *disp2* to form an address. The contents of that storage location are added to the value of *disp1* to form the effective address.
disp(reg$^{1-7}$)*	The effective address is the contents of storage at the address defined by the contents of *reg*$^{1-7}$, added to the value of *disp*.

(reg$^{1-7}$)*	The effective address is the contents of storage at the address defined by the contents of *reg*$^{1-7}$.
(reg$^{1-7}$,disp)*	The contents of *reg*$^{1-7}$ are added to *disp*, forming an address. The contents of storage at that address form the effective address.

For byte addressing, the effective address can be even or odd. For word or doubleword addressing, the effective address must be even.

bitdisp	A displacement into a bit field. Code an absolute value or expression in the range 0–63.
byte	A byte value. Code an absolute value or expression in the range -128 to +127 or 0 to 255.
cnt16	A single word (one register) shift count. Code an absolute value or expression in the range 0–16.
cnt31	A doubleword (register pair) shift count. Code an absolute value or expression in the range 0–31.
cond	A condition code value. Code an absolute value or expression in the range 0–7.
disp	A byte address displacement. Code an absolute value or expression in the range 0 to 255.
freg	A floating-point register. Code either a predefined floating register symbol (FR0–FR3) or a symbol that is equated to the desired register number (0, 1, 2, or 3). Symbols are equated with EQUR statements, which must precede the instruction using the register symbol.

jaddr	The address of an instruction that is within the range -256 to +254 bytes of the byte following a jump instruction. Code a relocatable expression.	
jdisp	A byte address displacement. Code an even absolute value or expression in the range -256 to +254.	
longaddr	An address value that you code in one of the following forms:	
	addr	The effective address is the value of *addr*, unless the instruction and *addr* are within the domain and range of the same USING statement. If they are, the assembler computes the effective address as a displacement (-32768 to +32767 or 0 to 65535) from the base register, which must be reg^{1-7}.
	addr*	The effective address is the contents of storage at the address defined by *addr*, unless the instruction and *addr* are within the domain and range of the same USING statement. If they are, the assembler computes the effective address as the contents of storage at the address defined by a displacement (-32768 to +32767 or 0 to 65535) from the base register, which must be reg^{1-7}.

(reg$^{1-7}$,waddr)	The effective address is the contents of *reg*$^{1-7}$, added to the value of *waddr*.
(reg$^{1-7}$,waddr)*	The contents of the *reg*$^{1-7}$, plus *waddr*, form an address. The contents of storage at that location form the effective address.
(reg$^{1-7}$)	The effective address is the contents of the register *reg*$^{1-7}$.
(reg$^{1-7}$)*	The effective address is the contents of storage at the address defined by the contents of *reg*$^{1-7}$.

raddr	An address value. Code a relocatable expression in the range 0 to 65535.
reg	A general-purpose register. Code either a predefined register symbol (R0–R7) or a symbol that is equated to the desired register number (0, 1, 2, 3, 4, 5, 6, or 7). Symbols are equated with EQUR statements, which must precede the instruction using the register symbol.
reg$^{0-3}$	A general-purpose register. Code either a predefined register symbol (R0–R3) or a symbol that is equated to the desired register number (0, 1, 2, or 3). Symbols are equated with EQUR statements, which must precede the instruction using the register symbol.
reg$^{1-3}$	A general-purpose register. Code either a predefined register symbol (R1–R3) or a symbol that is equated to the desired register number (1, 2, or 3). Symbols are equated with EQUR statements, which must precede the instruction using the register symbol.

reg$^{1-7}$	A general-purpose register. Code either a predefined register symbol (R1–R7) or a symbol that is equated to the desired register number (1, 2, 3, 4, 5, 6, or 7). Symbols are equated with EQUR statements, which must precede the instruction using the register symbol.	
shortaddr	An address value that you code in one of the following forms:	
	(reg$^{0-3}$, wdisp)	The effective address is the value of *wdisp* added to the contents of *reg*$^{0-3}$.
	(reg$^{0-3}$, wdisp)*	The effective address is the contents of storage at the address defined by the value of *wdisp* added to the contents of *reg*$^{0-3}$.
	(reg$^{0-3}$)	The effective address is the contents of (*reg*$^{0-3}$).
	(reg$^{0-3}$)*	The effective address is the contents of storage at the address defined by the contents of *reg*$^{0-3}$.
	addr	To use this form, the instruction and *addr* must be in the domain and range of the same USING statement. The assembler computes a displacement (0–62) and register combination that refers to the requested location.

addr*	Same as *addr*, except the assembler computes the effective address as the contents of storage at the address defined by a displacement (0–62) and register combination.

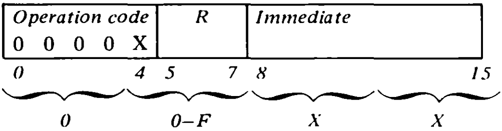
Note: For *addr* and *addr**, the base register must be reg^{0-3}.

ubyte	An unsigned byte value or mask. Code an absolute value or expression in the range 0 to 255.
vcon	An ordinary symbol that is defined externally from the current source program.
waddr	A one-word address value. Code an absolute or relocatable expression in the range -32768 to +32767 or 0 to 65535.
wdisp	An even byte address displacement. Code an absolute value or expression in the range 0–62.
word	A word value. Code an absolute value or expression in the range -32768 to +32767 or 0 to 65535.

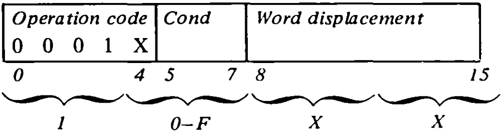
Instruction Format Types

X – Within instruction word (binary 0 or 1)
X – Beneath bracket (any hexadecimal digit)
Fun – Function field

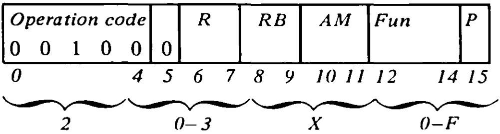
Type 1



Type 2

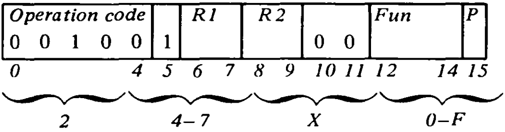


Type 3

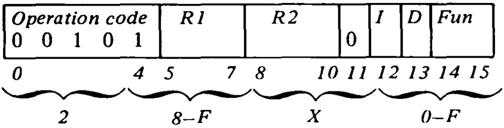


See note 1 (end of this list).

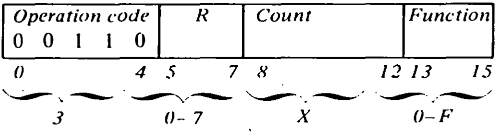
Type 4



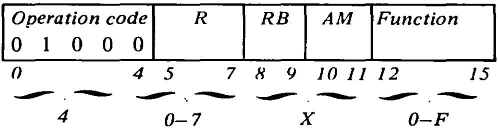
Type 5



Type 6

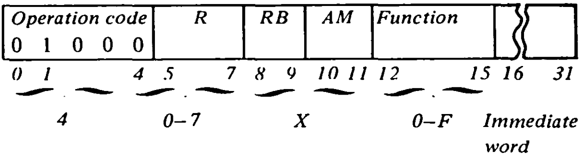


Type 7



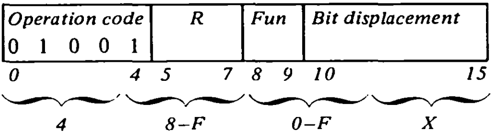
See note 1 (end of this list).

Type 8

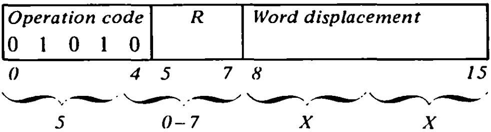


See note 2 (end of this list).

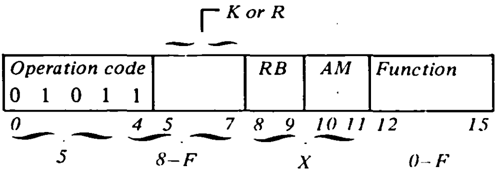
Type 9



Type 10

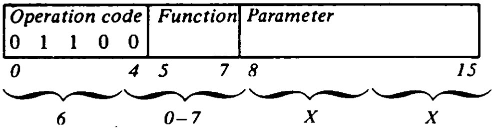


Type 11

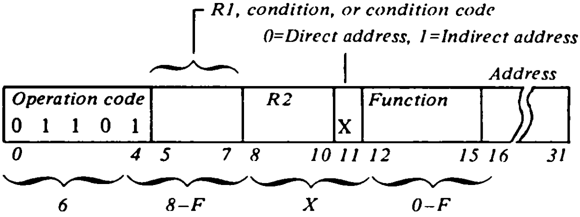


See note 1 (end of this list).

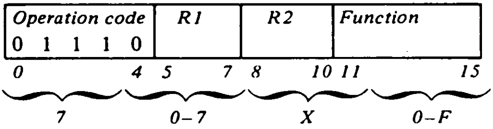
Type 12



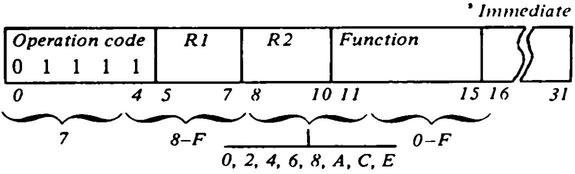
Type 13



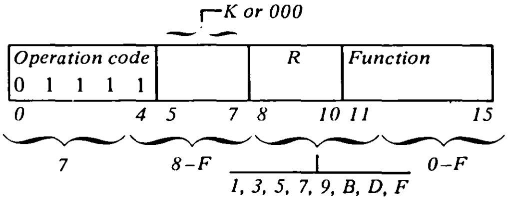
Type 14



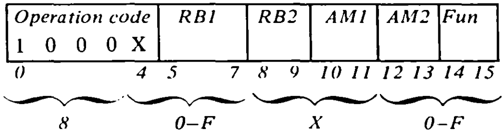
Type 15



Type 16

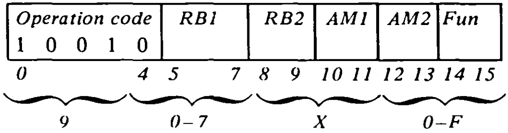


Type 17



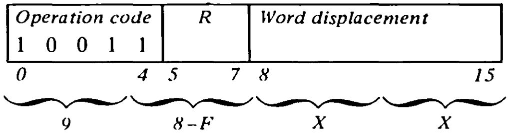
See note 3 (end of this list).

Type 18

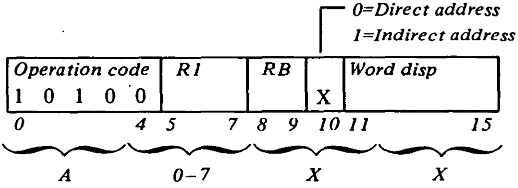


See note 3 (end of this list).

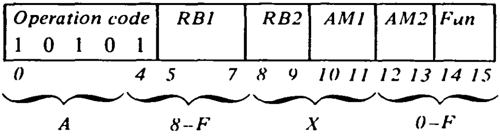
Type 19



Type 20

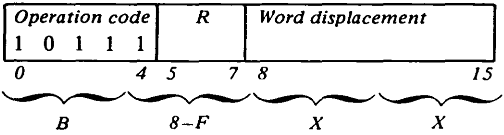


Type 21

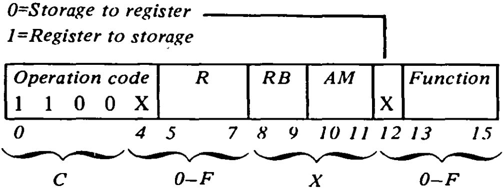


See note 3 (end of this list).

Type 22

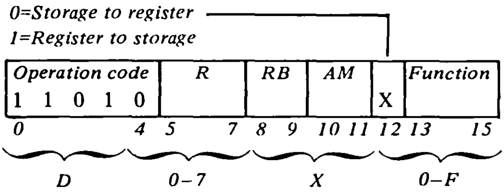


Type 23



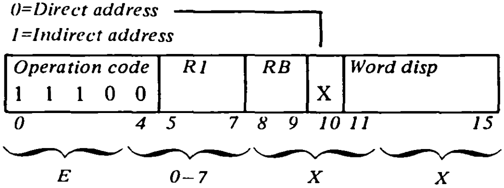
See note 1 (end of this list).

Type 24

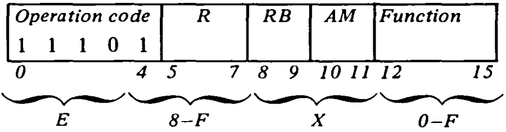


See note 1 (end of this list).

Type 25

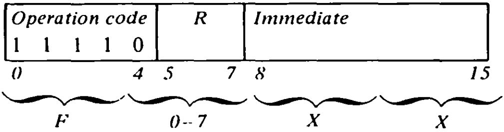


Type 26

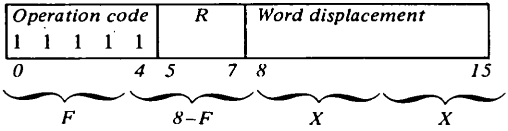


See note 1 (end of this list).

Type 27



Type 28



Notes:

1. An addressing mode (AM) word, when required, is appended to the instruction word in bit positions 16–31.
2. An addressing mode (AM) word, when required, is appended to the instruction word in bit positions 16–31. The immediate word is then moved to bit positions 32–47.
3. One or two addressing mode (AM) words may be appended to the instruction word. If one word is appended, bit positions 16–31 are used. If a second word is also appended, it appears in bit positions 32–47.

Code Conversion Table

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII*	*Eight bit data interchange*	*PTTC/EBCD*	*PTTC/ Correspondence*
0	00	0000 0000	NUL	NUL	NUL		
1	01	0001	SOH	SOH	NUL	space	space
2	02	0010	STX	STX		1	1,]
3	03	0011	ETX	ETX	@		
4	04	0100	PF	EOT		2	2
5	05	0101	HT	ENQ	space		
6	06	0110	LC	ACK			
7	07	0111	DEL	BEL		3	3
8	08	1000		BS		4	5
9	09	1001	RLF	HT			
10	0A	1010	SMM	LF	P (even parity)		
11	0B	1011	VT	VT	P (odd parity)	5	7
12	0C	1100	FF	FF	0 (even parity)		
13	0D	1101	CR	CR	0 (odd parity)	6	6
14	0E	1110	SO	SO		7	8
15	0F	1111	SI	SI			
16	10	0001 0000	DLE	DLE		8	4
17	11	0001	DC1	DC1			
18	12	0010	DC2	DC2	H (even parity)		

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII*	*Eight bit data inter-change*	*PTTC/EBCD*	*PTTC/ Correspondence*
19	13	0011	TM	DC3	H (odd parity)	9	0
20	14	0100	RES	DC4	((even parity)		
21	15	0101	NL	NAK	((odd parity)	0	z
22	16	0110	BS	SYN		Ⓓ (EOA)	Ⓓ (EOA),9
23	17	0111	IL	ETB			
24	18	1000	CAN	CAN			
25	19	1001	EM	EM			
26	1A	1010	CC	SUB			
27	1B	1011	CU1	ESC	X		
28	1C	1100	IFS	FS		upper case	upper case
29	1D	1101	IGS	GS	8		⩞
30	1E	1110	IRS	RS			
31	1F	1111	IUS	US		Ⓒ (EOT)	Ⓒ (EOT)
32	20	0010 0000	DS	space		@	t
33	21	0001	SOS	!	EOT		
34	22	0010	FS	”	D (even parity)		
35	23	0011		#	D (odd parity)	/	x
36	24	0100	BYP	$	S (even parity)		
37	25	0101	LF	%	S (odd parity)	s	n

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII*	*Eight bit data interchange*	*PTTC/EBCD*	*PTTC/ Correspondence*
38	26	0110	ETB	&		t	u
39	27	0111	ESC	'			
40	28	1000		(			
41	29	1001		)		u	e
42	2A	1010	SM	*		v	d
43	2B	1011	CU2	+	T		
44	2C	1100		,		w	k
45	2D	1101	ENQ	-	4		
46	2E	1110	ACK	.			
47	2F	1111	BEL	/		x	c
48	30	0011 0000		0	form feed		
49	31	0001		1	form feed	y	l
50	32	0010	SYN	2		z	h
51	33	0011		3	L		
52	34	0100	PN	4			
53	35	0101	RS	5			
54	36	0110	UC	6			
55	37	0011 0111	EOT	7		Ⓢ (SOA), comma	b
56	38	1000		8			

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII*	*Eight bit data interchange*	*PTTC/EBCD*	*PTTC/ Correspondence*
57	39	1001		9			
58	3A	1010		:	\ (even parity)		
59	3B	1011	CU3	;	\ (odd parity)	index	index
60	3C	1100	DC4	<	< (even parity)		
61	3D	1101	NAK	=	< (odd parity)	Ⓑ (EOB)	
62	3E	1110		>			
63	3F	1111	SUB	?			
64	40	0100 0000	space	@		N ,-	!
65	41	0001		A	EOA		
66	42	0010		B	B (even parity)		
67	43	0011		C	B (odd parity)	i	m
68	44	0100		D	" (even parity)		
69	45	0101		E	" (odd parity)	k	
70	46	0110		F		l	v
71	47	0111		G			
72	48	1000		H			
73	49	1001		I		m	,
74	4A	1010	¢	J		n	r
75	4B	1011	.	K	R		

Decimal	Hex	Binary	EBCDIC	ASCII	Eight bit data interchange	PTTC/EBCD	PTTC/ Correspondence
76	4C	1100	<	L		o	i
77	4D	1101	(	M	2		
78	4E	1110	+	N			
79	4F	1111	]	O		p	a
80	50	0101 0000	&	P	line feed		
81	51	0001		Q	line feed	q	o
82	52	0010		R		r	s
83	53	0011		S	J		
84	54	0100		T			
85	55	0101		U	*		
86	56	0110		V			
87	57	0111		W		$	w
88	58	1000		X			
89	59	1001		Y			
90	5A	1010	!	Z	Z (even parity)		
91	5B	1011	$	[	Z (odd parity)	CRLF	CRLF
92	5C	1100	*	\	: (even parity)		
93	5D	1101	)	]	: (odd parity)	backspace	backspace
94	5E	1110	;	^		idle	idle

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII*	*Eight bit data inter-change*	*PTTC/EBCD*	*PTTC/ Correspondence*
95	5F	1111	¬				
96	60	0110 0000	-		ACK		
97	61	0001	/	a		&	j
98	62	0010		b		a	g
99	63	0011		c	F		
100	64	0100		d		b	
101	65	0101		e	&		
102	66	0110		f			
103	67	0111		g		c	f
104	68	1000		h		d	p
105	69	1001		i			
106	6A	1010	¦	j	V (even parity)		
107	6B	1011	,	k	V (odd parity)	e	
108	6C	1100	%	l	6 (even parity)		
109	6D	1101	–	m	6 (odd parity)	f	q
110	6E	1110	>	n		g	comma
111	6F	1111	?	o			
112	70	0111 0000		p		h	/
113	71	0001		q	shift out		

Decimal	Hex	Binary	EBCDIC	ASCII	Eight bit data interchange	PTTC/EBCD	PTTC/ Correspondence
114	72	0010		r	N (even parity)		
115	73	0011		s	N (odd parity)	i	y
116	74	0100		t	. (even parity)		
117	75	0111 0101		u	. (odd parity)		
118	76	0110		v		Ⓨ ,period	-
119	77	0111		w			
120	78	1000		x			
121	79	1001	`	y			
122	7A	1010	:	z		horiz tab	tab
123	7B	1011	#	{	↑		
124	7C	1100	@	|		lower case	lower case
125	7D	1101	'	}	>		
126	7E	1110	=	~			
127	7F	1111	"	DEL		delete	
128	80	1000 0000					
129	81	0001	a		SOM	space	space
130	82	0010	b		A (even parity)	=	±, [
131	83	0011	c		A (odd parity)		
132	84	0100	d		! (even parity)	<	@

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII*	*Eight bit data interchange*	*PTTC/EBCD*	*PTTC/ Correspondence*
133	85	0101	e		! (odd parity)		
134	86	0110	f				
135	87	0111	g			;	#
136	88	1000	h		X-ON	:	%
137	89	1001	i				
138	8A	1010					
139	8B	1011			Q	%	&
140	8C	1100					
141	8D	1101			1	'	¢
142	8E	1110				>	*
143	8F	1111					
144	90	1001 0000			horiz tab	*	$
145	91	0001	j		horiz tab		
146	92	0010	k				
147	93	0011	l		I	(	)
148	94	0100	m				
149	95	0101	n		)	)	Z
150	96	0110	o			Ⓓ (EOA),"	(
151	97	0111	p				

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII*	*Eight bit data inter-change*	*PTTC/EBCD*	*PTTC/ Correspondence*
152	98	1000	q				
153	99	1001	r				
154	9A	1010			Y (even parity)		
155	9B	1011			Y (odd parity)		
156	9C	1100			9 (even parity)	upper case	upper case
157	9D	1101			9 (odd parity)		
158	9E	1110					
159	9F	1111				Ⓒ (EOT)	Ⓒ (EOT)
160	A0	1010 0000			WRU (even)	¢	T
161	A1	0001	~		WRU (odd)		
162	A2	0010	s				
163	A3	0011	t		E	?	X
164	A4	0100	u				
165	A5	0101	v		%	S	N
166	A6	0110	w			T	U
167	A7	0111	x				
168	A8	1000	y				
169	A9	1001	z			U	E
170	AA	1010			U (even parity)	V	D

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII*	*Eight bit data inter-change*	*PTTC/EBCD*	*PTTC/ Correspondence*
171	AB	1011			U (odd parity)		
172	AC	1100			5 (even parity)	W	K
173	AD	1101			5 (odd parity)		
174	AE	1110					
175	AF	1111				X	C
176	B0	1011 0000					
177	B1	0001			return	Y	L
178	B2	0010			M (even parity)	Z	H
179	B3	1011 0011			M (odd parity)		
180	B4	0100			- (even parity)		
181	B5	0101			- (odd parity)		
182	B6	0110					
183	B7	0111				Ⓢ (SOA), |	B
184	B8	1000					
185	B9	1001					
186	BA	1010					
187	BB	1011			]	index	index
188	BC	1100					

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII*	*Eight bit data inter-change*	*PTTC/EBCD*	*PTTC/ Correspondence*
189	BD	1101			=	Ⓑ (EOB)	
190	BE	1110					
191	BF	1111					
192	C0	1100 0000	{		EOM (even)	Ⓝ ,–	
193	C1	0001	A		EOM (odd)		
194	C2	0010	B				
195	C3	0011	C		C	J	M
196	C4	0100	D				
197	C5	0101	E		#	K	
198	C6	0110	F			L	V
199	C7	0111	G				
200	C8	1000	H				
201	C9	1001	I		X-OFF	M	”
202	CA	1010			S (even parity)	N	R
203	CB	1011			S (odd parity)		
204	CC	1100	⑀		3 (even parity)	O	I
205	CD	1101			3 (odd parity)		
206	CE	1110	⑂				
207	CF	1111				P	A

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII*	*Eight bit data interchange*	*PTTC/EBCD*	*PTTC/ Correspondence*
208	D0	1101 0000	}				
209	D1	0001	J		vertical tab	Q	O
210	D2	0010	K		K (even parity)	R	S
211	D3	0011	L		K (odd parity)		
212	D4	0100	M		+ (even parity)		
213	D5	0101	N		+ (odd parity)		
214	D6	0110	O				
215	D7	0111	P			!	W
216	D8	1000	Q				
217	D9	1001	R				
218	DA	1010					
219	DB	1011			[	CRLF	CRLF
220	DC	1100					
221	DD	1101			;	backspace	backspace
222	DE	1110				idle	idle
223	DF	1111			PAD		
224	E0	1110 0000	\				
225	E1	0001			bell	+	J
226	E2	0010	S		G (even parity)	A	G

Decimal	Hex	Binary	EBCDIC	ASCII	Eight bit data inter-change	PTTC/EBCD	PTTC/ Correspondence
227	E3	0011	T		G (odd parity)		
228	E4	0100	U		, (even parity)	B	+
229	E5	0101	V		, (odd parity)		
230	E6	0110	W				
231	E7	0111	X			C	F
232	E8	1000	Y			D	P
233	E9	1001	Z				
234	EA	1010					
235	EB	1011			W	E	
236	EC	1100	⑂				
237	ED	1101			7	F	Q
238	EE	1110				G	comma
239	EF	1111					
240	F0	1111 0000	0		shift in (even)	H	?
241	F1	0001	1		shift in (odd)		
242	F2	0010	2				
243	F3	0011	3		O	I	Y
244	F4	0100	4				
245	F5	0101	5		/		

Decimal	*Hex*	*Binary*	*EBCDIC*	*ASCII*	*Eight bit data inter-change*	*PTTC/EBCD*	*PTTC/ Correspondence*
246	F6	0110	6			Ⓨ , ¬	
247	F7	0111	7				—
248	F8	1000	8				
249	F9	1001	9				
250	FA	1010	LVM		⇐ (even parity)	horiz tab	tab
251	FB	1011			⇐ (odd parity)		
252	FC	1100			? (even parity)	lower case	lower case
253	FD	1101			? (odd parity)		
254	FE	1110					
255	FF	1111			delete rub out	delete	

Class Interrupt Priority

Priority	*Exception condition*	*Class interrupt routine*
0	CPU control check I/O check	Machine check
1	Invalid function (Note 1)	Program check
2	Privilege violate	
3	Invalid function (Notes 2 and 3)	
4	Protect check (Note 4)	
5	Invalid storage address Specification check	
6	Storage parity	Machine check
7	Power warning Thermal warning	Power/thermal warning
8	Supervisor call	Supervisor call
9	Invalid function (Note 5)	Soft exception trap
10	Floating-point exception (Notes 3 and 4)	
11	Stack exception	
12	Trace	Trace
13	Clock (Note 6)	Clock
14	Console	Console

Notes:

1. Caused by an illegal operation code or function combination.
2. A Copy Segmentation Register (CPSR) or Set Segmentation Register (SESR) instruction is attempted and the translator feature is not installed. The translator feature is not available on the 4953 processor.
3. Not applicable on the 4952 processor
4. Not applicable on the 4953 processor.
5. A floating-point instruction is attempted and the floating-point feature is not installed. The floating-point feature is not available on the 4952 and 4953 processors.
6. Applies to the 4950, 4952, 4954, and 4956 processors only.

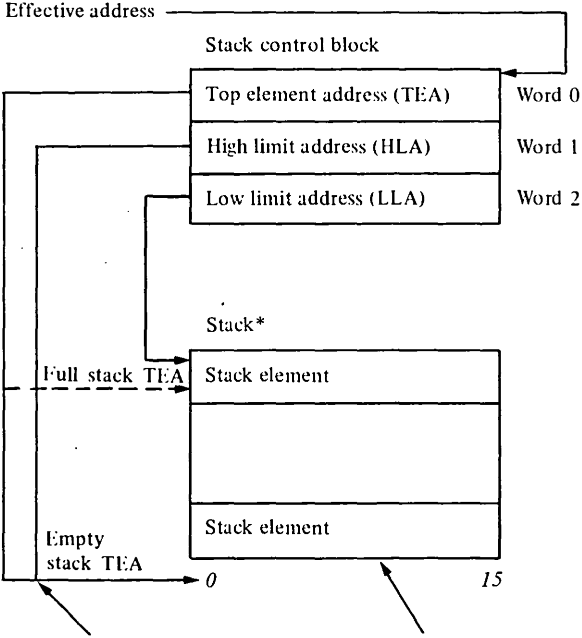
Control Blocks

Level Status Block

Main storage address (LSB pointer)	Instruction address register
	Address key register*
	Level status register
	Register 0
	Register 1
	Register 2
	Register 3
	Register 4
	Register 5
	Register 6
+14 (Hex)	Register 7
	0 15

* This word is zero for the 4953 processor

Stack Control Block



The TEA for an empty stack points to the same place as the HLA

Stack element shown is 1 word; element can be 1, 2, or 4 bytes wide

*The size of the stack (in elements) is equal to HLA - LLA.

Indicators Tested by Conditional Branch and Jump Instructions

*Cond field bits**	*Extended mnemonics*		*Indicators tested*
	Branch	*Jump*	*0 1 2 3 4*
			E C O N Z
000	BE, BOFF, BZ	JE, JOFF, JZ	X X X X 1
	BNE, BNOFF, BNZ	JNE, JNOFF, JNZ	X X X X 0
001	BMIX, BP	JMIX, JP	X X X 0 0
	BNMIX, BNP	JNMIX, JNP	X X X X 1 X X X 1 X
010	BN, BON	JN, JON	X X X 1 X
	BNN, BNON	JNN, JNON	X X X 0 X
011	BEV	JEV	1 X X X X
	BNEV	JNEV	0 X X X X
100	BLT	JLT	X X 0 1 X X X 1 0 X
	BGE	JGE	X X 1 1 X X X 0 0 X
101	BLE	JLE	X X 0 1 X X X 1 0 X X X X X 1
	BGT	JGT	X X 1 1 0 X X 0 0 0
110	BLLE	JLLE	X 1 X X X X X X X 1
	BLGT	JLGT	X 0 X X 0
111	BCY, BLLT	JCY, JLLT	X 1 X X X
	BLGE, BNCY	JLGE, JNCY	X 0 X X X

*Bits 5–7 of the instruction word for:
Branch on Condition (BC)
Branch on Not Condition (BNC)
Jump on Condition (JC)
Jump on Not Condition (JNC)

X - The indicator is not tested

LSR bit	*Indicator*
0	E - even
1	C - carry
2	O - overflow
3	N - negative
4	Z - zero

Registers

Address Key Register (AKR)—Standard*

Bit	**Contents**
0	Equate operand spaces
1	Not used; always 0
2	Not used; always 0
3	Not used; always 0
4	Not used; always 0
5	Operand-1 key (bit 0)
6	Operand-1 key (bit 1)
7	Operand-1 key (bit 2)
8	Not used; always 0
9	Operand-2 key (bit 0)
10	Operand-2 key (bit 1)
11	Operand-2 key (bit 2)
12	Not used; always 0
13	Instruction space key (bit 0)
14	Instruction space key (bit 1)
15	Instruction space key (bit 2)

*Not applicable on the 4950 processor, 4953 processor, nor on the 4956 processor models E and 60E in 4-bit mode

Address Key Register (AKR)—4956 Processor Models E and 60E (4-Bit Mode)

Bit	Contents
0	Equate operand spaces
1	Not used; always 0
2	Not used; always 0
3	Not used; always 0
4	Operand-1 key (bit 0)
5	Operand-1 key (bit 1)
6	Operand-1 key (bit 2)
7	Operand-1 key (bit 3)
8	Operand-2 key (bit 0)
9	Operand-2 key (bit 1)
10	Operand-2 key (bit 2)
11	Operand-2 key (bit 3)
12	Instruction space key (bit 0)
13	Instruction space key (bit 1)
14	Instruction space key (bit 2)
15	Instruction space key (bit 3)

Address Key Register (AKR)—4950 Processor (5-Bit Mode)

Bit	Contents
0	Equate operand spaces (E.O.S.)
1	Operand-1 key (bit 0)
2	Operand-2 key (bit 0)
3	Instruction space key (bit 0)
4	Operand-1 key (bit 1)
5	Operand-1 key (bit 2)
6	Operand-1 key (bit 3)
7	Operand-1 key (bit 4)
8	Operand-2 key (bit 1)
9	Operand-2 key (bit 2)
10	Operand-2 key (bit 3)
11	Operand-2 key (bit 4)
12	Instruction space key (bit 1)
13	Instruction space key (bit 2)
14	Instruction space key (bit 3)
15	Instruction space key (bit 4)

Level Status Register (LSR)

Bit	Contents
0	Even indicator
1	Carry indicator
2	Overflow indicator
3	Negative result indicator
4	Zero result indicator
5	Not used; always 0
6	Not used; always 0
7	Not used; always 0
8	Supervisor state
9	In process
10	Trace
11	Summary mark
12	Not used; always 0
13	Not used; always 0
14	Not used; always 0
15	Not used; always 0

Mask Register—Interrupt Level

Bit	Priority level
0	0
1	1
2	2
3	3

Note: If a bit position is set to 1, the corresponding level is allowed to interrupt.

Processor Status Word (PSW)

Bit	Contents
0	Specification check
1	Invalid storage address
2	Privilege violate
3	Protect check*
4	Invalid function
5	Floating-point exception**
6	Stack exception
7	Not used; always 0†
8	Storage parity check Double bit storage error (ECC)***
9	Not used; always 0
10	CPU control check
11	I/O check
12	Sequence indicator
13	Auto-IPL
14	Translator enabled*
15	Power/thermal warning

*Not used by the 4953 processor; always 0

**Not used by the 4952 and 4953 processors; always 0

***Used by the 4956 processor only

†Indicates 4-bit mode enabled on the 4956 processor models E and 60E

Segmentation Register*

Bit	Meaning
0–5	Zeros** Segment address***
6	S-bit** Segment address***
7–12	Segment address
13	Valid bit
14	Read-only bit
15–31	Zeros

*Not applicable on the 4953 processor

**Applies to the 4952 processor only

***Applies to the 4950, 4954, 4955, and 4956 processors only

Reserved Storage Locations

Main storage address (Hex)	*Contents of word*
022E	Device FF DDB pointer
0032	Device 01 DDB pointer
0030	Device 00 DDB pointer
002E	Reserved
002C	Reserved
002A	I/O Handler SIA**
0028	I/O LSB pointer**
0026	Clock interrupt SIA*
0024	Clock interrupt LSB pointer*
0022	Soft exception trap SIA
0020	Soft exception trap LSB pointer
001E	Console interrupt SIA
001C	Console interrupt LSB pointer
001A	Trace SIA
0018	Trace LSB pointer
0016	Power failure SIA
0014	Power failure LSB pointer
0012	SVC SIA
0010	SVC LSB pointer
000E	Program check SIA
000C	Program check LSB pointer
000A	Machine check SIA
0008	Machine check LSB pointer
0006	Reserved
0004	Reserved
0002	Restart instruction word 2
0000	Restart instruction word 1

*Applies to the 4950, 4952, 4954, and 4956 processors only.
**Applies to the 4950 processor only.

Section 2. Common I/O

Condition Codes

I/O Instruction Condition Codes

These codes are reported during execution of an Operate I/O instruction.

	LSR position				
Condition code (CC)	**Even**	**Carry**	**Over-flow**	**Reported by**	**Meaning**
0	0	0	0	channel	Device not attached
1	0	0	1	device	Busy
2	0	1	0	device	Busy after reset
3	0	1	1	chan/dev	Command reject
4	1	0	0	device	Intervention required
5	1	0	1	chan/dev	Interface data check
6	1	1	0	controller	Controller busy
7	1	1	1	chan/dev	Satisfactory

Interrupt Condition Codes

These condition codes are reported by the device or controller during priority interrupt acceptance.

	LSR position				
Condition code (CC)	Even	Carry	Over-flow	Reported by	Meaning
0	0	0	0	controller	Controller end
1	0	0	1	device	Program controlled interrupt (PCI)
2	0	1	0	device	Exception
3	0	1	1	device	Device end
4	1	0	0	device	Attention
5	1	0	1	device	Attention and PCI
6	1	1	0	device	Attention and exception
7	1	1	1	device	Attention and device end

Device ID Word

Device ID Word Format

Class	0	Assigned code		
0 *3*	*4*	*5* *13*	*14*	*15*

Bits 0–3	Assigned class code
Bit 4	Reserved—always zero
Bits 5–13	Assigned code
Bit 14	Zero—not a cycle-steal device One—cycle-steal device
Bit 15	Zero—IBM device One—OEM device

List of Device ID Words

Device or feature	ID word (hex)
Communications feature—Asynchronous	
Single line	100E
Two line	210E
Four line	220E
Six line	230E
Eight line	200E
Communications feature—BSC	
Single line	1006
Two line	2106
Four line	2206
Six line	2306
Eight line	2006
Customer Direct Program Control Adapter feature	*
Integrated DI/DO Non-Isolated feature	
Digital input	C010
Digital output	C018
Local Communications Controller Attachment Feature	320E
Multidrop Workstation Attachment	
1 Domain	203E
2 Domain	213E
4 Domain	223E
8 Domain	233E
Multifunction attachment feature	
Model 1	020B
Model 2	020A
Printer Attachment—5200 Series	
1 Domain	202E
2 Domain	212E
4 Domain	222E
8 Domain	232E

*See *IBM Series/1 Attachment Features Description*, GA34-0031, for the format of this word.

Device or feature	ID word (hex)
Communications feature—Programmable Multiline Attachment	
Two line	2116
Four line	2216
Six line	2316
Eight line	2016
Programmable Two-Channel Switch feature	003C
Communications feature—SDLC	1016
Series/1–Personal Computer Attachment feature	321E
Series/1–System/370 Channel Attachment feature	4002
Synchronous Communications Single-Line Control	5042
Teletypewriter Adapter feature	0010
Timer feature	0028
Two Channel Switch feature	0030
4950/5170 Model 495 Disk/Diskette Adapter	3212
4962 Disk Storage Unit	
Models 1 and 2	00AA
Models 1F and 2F	00BA
Models 3 and 4	00CA
4963 Disk Subsystem	
1–2 Devices	3106
3–4 Devices	3206
4964 Diskette Unit	0106
4965 Storage and I/O Expansion Unit	
Model 1	5212
Models 30D and 60D	5152
4966 Diskette Magazine Unit	0126
4967 High-Performance Disk Subsystem	
1–2 Drives	3116
3–4 Drives	3216

Device or feature	**ID word (hex)**
4968 Magnetic Tape Unit	0102
4969 Magnetic Tape Subsystem	
1–2 Devices	3186
3–4 Devices	3286
4971/4201 Proprinter	0403
4973 Line Printer	0306
4974 Printer	0206
4978 Display Station Attachment	040E
4979 Display Station	0406
4982 Sensor I/O Unit	
AI with multirange amplifier	8028
AI without multirange amplifier	8020
Analog output	8040
Digital output	8018
Isolated DI/PI	8008
Nonisolated DI/PI	8010
Reed relay multiplexer	8030
Solid state multiplexer	8038
4987 Programmable Communications Subsystem	
1–4 Devices	221E
5–8 Devices	231E
9–16 Devices	241E
17–32 Devices	251E
5250 Information Display System Attachment	0416
7880 Audio distribution system	2412

Immediate Device Control Block (IDCB)

Command	*Device address*	*Immediate field*
0 7	*8 15*	*16 31*

Hex*	Specific command	Type of operation
0X	Read	DPC
1X	Read	DPC
20	Read ID	DPC
2X	Read Status	DPC
3X	Unused	Unused
4X	Write	DPC
5X	Write	DPC
60	Prepare	DPC
6X	Control	DPC
6F	Device Reset	DPC
7X	Start	Cycle-Steal
7F	Start Cycle-Steal Status	Cycle-Steal
F0	Halt I/O	Channel

*The hexadecimal X is a device dependent value other than the values defined by the system.

Interrupt ID Word

IIB	*Device address*
0 *7*	*8* *15*

Bits 0–7	*Interrupt information byte (IIB).* For interrupt condition codes 2 and 6, the IIB has a special format and is called an interrupt status byte (ISB). For other interrupt condition codes, implementation of the IIB is device dependent. Exceptions are: CC0 — The IIB is set to zero. CC1, CC5 — The IIB contains a DCB identifier. CC3, CC7 — Bit 0 may be set to one if suppress exception is in effect.
Bits 8–15	*Device address.* This byte contains the address of the interrupting device.

Interrupt Status Byte (ISB)

DPC Devices

Bit	Meaning
0	Device status available
1	Delayed command reject
2	Device dependent
3	Device dependent
4	Device dependent
5	Device dependent
6	Device dependent
7	Device dependent

Cycle-Steal Devices

Bit	Meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4950, 4952, or 4953 processor

Section 3. I/O Devices and Features

Communications Feature—Asynchronous

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1*,2*,5,7
60	Prepare	0,1**,5,7
6F	Device Reset	0,7
70	Start	0,1,2*,5,6**,7
7C	Start Control	0,1,2*,5,6**,7
7D	Start Diagnostic 1	0,1,2*,5,6**,7
7E	Start Diagnostic 2	0,1,2*,5,6**,7
7F	Start Cycle-Steal Status	0,1,2*,5,6**,7

*Not reported by the multiple-line attachments
**Not reported by any single-line communications attachment

Device Control Block (DCB)

Word	
0	Control word
1	Not used
2	Timer 1
3	Timer 2
4	Not used
5	Chain address–must be even address
6	Byte count
7	Data address

0 *15*

Asynchronous

Control Word (DCB Word 0)

Bit	Meaning	
0	Chaining flag	
1	Not used—zero	
2	Input flag—data cycle-steal to storage	
3	Not used—zero	
4	Not used—zero	
5–7	Cycle-steal address key	
8–9	Not used—zeros	
10–15	Operation	
	000000	Transmit
	000001	Transmit end
	000010	Transmit allow break
	000011	Transmit end allow break
	000100	Receive
	000101	Receive with time-out
	100100	Receive response
	100101	Receive response with time-out
	000110	Ring enable
	000111	Ring enable with time-out
	001000	DTR enable
	001001	DTR enable with time-out
	001010	DTR enable with tone/generate answertone
	001011	DTR enable with tone and time-out/generate answertone with time-out
	001100	DTR disable
	001101	Set control PTTC
	011101	Set control 8-bit interchange
	001110	Program delay
	001111	Reset

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0	Overrun
1	Time-out
2	Block check error
3	DCB reject
4	EOB, count not zero
5	VRC error
6	Break detected
7	Stop-bit error
8	Not used—zero
9	Modem interface error
10–15	Not used—zeros

Word 2

Bit	Meaning
0	Data terminal ready
1	Data set ready
2	Request to send
3	Clear to send
4	Ring indicator
5	Receive mode
6–15	Not used—zeros

Interrupt Condition Codes Reported

CC0*, CC2, CC3

*Not reported by single-line attachments

Interrupt Information Byte (IIB)

Condition code	IIB Contents
0, 3	Always zeros
2	Cycle-steal interrupt status byte (ISB)

Asynchronous

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

Communications Feature—BSC

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1*,2*,5,7
60	Prepare	0,1**,5,7
6F	Device Reset	0,7
70	Start	0,1,2*,5,6**,7
7C#	Start Control	0,1,2*,5,6**,7
7D#	Start Diagnostic 1	0,1,2*,5,6**,7
7E#	Start Diagnostic 2	0,1,2*,5,6**,7
7F	Start Cycle-Steal Status	0,1,2*,5,6**,7
F0	Halt I/O	N/A

Not supported by the 4950 processor
* Not reported by multiple-line attachments
** Not reported by single-line attachments

Device Control Block (DCB)

Word	
0	Control word
1	Not used
2	Not used
3	Not used
4	Not used
5	Chain address
6	Byte count
7	Data address

0 *15*

BSC

Control Word (DCB Word 0)

Bit	Meaning
0	Chaining flag
1	Not used—zero
2	Input flag
3	Not used—zero
4	Not used—zero
5–7	Cycle-steal address key
8	Half rate
9*	ASCII mode
10	Enable terminal (DTR)
11	Disable terminal (DTR)
12	Start timer
13	Transmit operation
14	Exit transparent
15	Not used—zero

* Not supported on the 4950 processor

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0	Overrun
1	Time-out
2	Modem interface error
3	Block check error
4	Multipoint transmit error
5*	Answertone jumper installed
6	Multipoint tributary jumper installed
7*	Internal clock jumper installed
8–15	Multipoint address

*Not used for a device attached to a 4950 processor

Word 2

Bit	Meaning
0	Data terminal ready
1	Data set ready
2	Request to send
3	Clear to send
4	Ring indicator
5	Half rate selected
6	Transmit mode latch
7	Not used—zero
8–15*	Indicator panel switch setting

*Not used for a device attached to a 4950 processor

Interrupt Condition Codes Reported

CC0*#, CC2, CC3, CC4#, CC6#, CC7#

*Not reported by single-line attachments

#Not reported by the 4950 processor

Interrupt Information Byte (IIB)

Condition code	IIB Contents
0, 3, 4, 7	Always zeros
2, 6	Cycle-steal interrupt status byte (ISB)

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4950, 4952, or 4953 processor

Customer Direct Program Control Adapter Feature

I/O Commands

Hex	Command	I/O instruction CCs reported
0X	Read Data	0,1,2,3,4,5,6,7
1X	Read Data	0,1,2,3,4,5,6,7
20	Read ID	0,5,7
2X	Read Status	0,1,2,3,4,5,6,7
2E	Read Adapter Status Word	0,5,7
2F	Read Adapter Diagnostic Data	0,5,7,
4X	Write Data	0,1,2,3,4,5,6,7
5X	Write Data	0,1,2,3,4,5,6,7
60	Prepare	0,5,7
61	Set Diagnostic Mode	0,5,7
62	Reset Diagnostic Mode	0,5,7
6X	Write Control	0,1,2,3,4,5,6,7

Device Status Word

Bit	Meaning
0	Local diagnostic mode
1	External diagnostic mode
2	Output parity error
3	Input parity error
4	Parity option selected
5	Eight device addresses
6	Four device addresses
7	Diagnostic interrupt masking
8–15	Zeros

Interrupt Condition Codes Reported

CC0, CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	IIB contents
0, 3, 4, 7	Device dependent*
2, 6	DPC interrupt status byte*

*Device dependent status is defined by the I/O device designer.

Integrated DI/DO Non-Isolated Feature

I/O Commands

Hex	Command	I/O instruction CCs reported
00	Read DI	0,1,5,7
01	Read PI	0,5,7
02	Read P1 With Reset	0,1,5,7
20	Read ID	0,5,7
21	Read DO	0,5,7
28	Read Status	0,5,7
48	Write DO	0,1,5,7
60	Prepare	0,5,7
68	Arm PI	0,1,5,7
69	Arm DI External Sync	0,1,5,7
69	Arm DO External Sync	0,1,5,7
6A	Set Test 0	0,1,5,7
6B	Set Test 1 (DI/PI)	0,1,5,7
6B	Set Diagnostic External Sync (DO)	0,1,5,7
6C	Disable DO	0,1,5,7
6F	Device Reset	0,7

Device Status Word

DI Status Word

Bit	Meaning
0, 1	Zero
2	PI mode is armed
3	External sync mode is armed
4	Set-test-1 mode is set
5	Set-test-0 mode is set
6, 7	Interrupt state
8–15	Zero

DO Status Word

Bit	**Meaning**
0, 1	Zero
2	Disable mode is set
3	External sync mode is armed
4	Diagnostic external sync was set
5	Zero
6, 7	Interrupt state
8–15	Zero

Interrupt Condition Codes Reported

CC4

Interrupt Information Byte (IIB)

DI Group

Condition code	**IIB contents**
4	Same as bits 0–7 of the DI status word

DO Group

Condition code	**IIB contents**
4	Same as bits 0–7 of the DO status word

Local Communications Controller Attachment Feature

I/O Commands

Hex	**Command**	**I/O instruction CCs reported**
20	Read ID	0,5,7
40	Initiate Diagnose	0,1,2,3,5,6,7
41	Set Bypass	0,1,2,3,5,6,7
42	Reset Bypass	0,1,2,3,5,6,7
43	Clear Ring	0,1,2,3,5,6,7
44	IPL Request	0,1,2,3,5,6,7
45	Disable Frame Capture	0,1,2,3,5,6,7
46	Enable Frame Capture	0,1,2,3,5,6,7
60	Prepare	0,5,7
6F	Device Reset	0,7

Device Control Block (DCB)

Word		
0	DCB control word	
1	Ring address	Reserved
2	Attachment microcontroller storage address	
3	DCB ID	Reserved
4	Status address	
5	Chain address	
6	Data byte count	
7	Data address	
	0	*15*

Control Word (DCB Word 0)

Bit	Meaning
0	Chaining flag
1	Program-controlled interrupt (PCI)
2	Input flag
3	Extended DCB (XD)
4	Suppress exception
5–7	Cycle-steal address key
8	RAS diagnostic monitor mode
9	Reserved
10–14	Modifier bits
15	Burst mode (not supported, always 0)

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0–15	Residual count

Word 2

Bit	Meaning
0–15	Start cycle-steal device status

Word 3

Bit	Meaning
0–15	Hardware status

Local Communications

Word 4

Bit	Meaning
0–15	Frame byte count

Word 5

Word 5 is the DCB address contained in the IDCB.

Word 6

Word 6 contains the subchannel current DCB address.

Words 7–14

These words contain the current DCB.

Residual Status Block (RSB)

Word 0

Bit	Meaning
0–15	Residual count

Word 1

Bit	Meaning
0	End of chain
1–14	Not used—zeros
15	No exception

Word 2

Bit	Meaning
0–15	Residual address

Word 3

Bit	Meaning
0–7	Ring address (word 1 of DCB)
8–15	DCB byte 0 (bits 0–7 of current DCB control word)

Word 4

Bit	Meaning
0–15	Data address (word 7 of DCB)

Interrupt Condition Codes Reported

CC0, CC1, CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents	
0	Zeros	
1	DCB identifier	
2	Cycle-steal interrupt status byte (ISB)	
3	Bit 0 may be set to 1 if suppress exception is in effect	
4	**Bit**	**Meaning**
	0–4	Not used
	5	Cable open/short condition detected
	6	Accumulator error overflow
	7	Set IPL frame was received and the ring remote IPL jumper is not installed
5–7	Not used	

Local Communications

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device-dependent status available
1	Delayed command reject
2	Incorrect-length record
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Multidrop Workstation Attachment

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,3,5,7
60	Prepare	0,3,5,7
6F	Device Reset	0,3,7
70–73	Start	0,1,2,3,5,6,7
7C	Start Control	0,1,2,3,5,6,7
7F	Start Cycle-Steal Status	0,1,2,3,5,6,7

Device Control Block (DCB)—General Format

Word	
0	Control word
1	Operation dependent parameters
2	Operation dependent parameters
3	Operation dependent parameters
4	Operation dependent parameters
5	DCB chain address
6	Byte count
7	Data address
	0 … *15*

Multidrop Workstation

Device Control Block (DCB)—Start Control Command

<table>
<tr><td><i>Word</i></td><td colspan="3"></td></tr>
<tr><td><i>0</i></td><td>X 0 X 0 0</td><td>KEY</td><td>Operation</td></tr>
<tr><td><i>1</i></td><td colspan="3">Operation dependent parameters</td></tr>
<tr><td><i>2</i></td><td colspan="3">Operation dependent parameters</td></tr>
<tr><td><i>3</i></td><td colspan="3">Operation dependent parameters</td></tr>
<tr><td><i>4</i></td><td colspan="3">Operation dependent parameters</td></tr>
<tr><td><i>5</i></td><td colspan="3">DCB chain address</td></tr>
<tr><td><i>6</i></td><td colspan="3">Byte count</td></tr>
<tr><td><i>7</i></td><td colspan="3">Data address</td></tr>
<tr><td></td><td><i>0</i></td><td></td><td><i>15</i></td></tr>
</table>

Control Word (DCB Word 0)—Start Control Command

Bit	Meaning	
0	Chaining flag	
1	Set to 0	
2	Input flag	
3, 4	Set to 0	
5–7	Cycle-steal address key	
8–15	Attachment control operation:	
	10100000	Enable options
	10100001	Disable options
	10110000	Read error log
	10110001	Read error log and clear
	11010000	Start diagnostic 0
	11100010*	Initialize attachment
	11100100	Read attachment storage
	11101000	Load attachment storage
	11101010*	Load attachment storage and initialize
	11101100*	Execute attachment storage
	11101110	Write device definition data
	11110010	Clear attachment storage
	11111101	Read attachment definition
	11111110	Read device definition data
	11111111	Start cycle-steal read ID

*Chaining not supported

Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	Address of last-attempted data transfer

Multidrop Workstation

Words 1–2

Device dependent. See device description manual.

Word 3—Attachment Status

Bit	Meaning
0	Initialized
1	Attachment storage checksum error
2	Device defined
3	Storage incompatibility error
4	Device ready
5–7	Residual address key
8–11	Not used—zeros
12	Attachment hardware error
13	Read-only storage checksum error
14	Attachment storage data error
15	Not used

Word 4—Device ID

Hex 0402 for 4980
Hex FFFF for Null

Word 5

Not used

Words 6–7

Device dependent. See device description manual.

Word 8—Device Definition Errors

Bit	Meaning
0	Invalid device ID
1	Invalid line speed
2	Invalid port address
3	Device station address conflict. The device station address is assigned to another device on the same port.
4	Line speed conflict. A different line speed is assigned to another device on the same port.
5	Invalid device station address
6–15	Not used

Word 9—Software Recoverable Error

Bit	Meaning
0	Invalid operation from the attachment. The device does not recognize the operation from the attachment. The invalid operation is stored in word 11.
1	Incorrect operation from the attachment. The device received an operation that was not allowed or was out of sequence.
2–15	Not used

Multidrop Workstation

Word 10—Software Unrecoverable Error

Bit	Meaning
0	Invalid operation from the device. The invalid operation is stored in word 11.
1	Incorrect operation from the device
2	Data security violation
3–5	Not used
6	Device power-on-reset failure. The POR diagnostic word received from the device is in word 11.
7	Device disconnect/failure. The device is incorrectly responding to orders. It is either disconnected, powered-off, or has a hardware failure.
8	Not used
9	Receive error. The attachment ends the operation with an exception interrupt due to unrecoverable receive errors such as frame check sequence, end operation, and overrun.
10	Frame reject. The device received invalid frames from the attachment.
11	Transmit error. The attachment ends the operation with an exception interrupt due to unconfirmed transmit errors.
12–15	Not used

Word 11—Diagnostic/Failing Order

This word contains one of the following:

- Invalid order from attachment (if word 9 bit 0 is set to 1)
- Invalid order from the device (if word 10 bit 0 is set to 1)
- Power-on-reset diagnostic word (if word 10 bit 6 is set to 1).

Word 12—Device Read-Only Storage Level

A hexadecimal number in the device read-only storage that defines the device read-only storage compatibility with the storage load residing on the device diskette.

Word 13

Device dependent

Interrupt Condition Codes Reported

CC0, CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents
0	Hex FF—Request to Read Attachment Error Log Interrupt
2	Cycle-steal interrupt status byte (ISB)
3	Always zero
4	Key interrupt codes

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device dependent status available
1	Delayed command reject
2	Incorrect length record
3	DCB specification check
4	Storage data check
5	Invalid storage check
6	Protect check
7	Interface data check

Multifunction Attachment Feature

I/O Commands

Hex	Command
20	Read ID
60	Prepare
6F	Device Reset
70*	Start
7C	Start Control
7F*	Start Cycle-Steal Status

*4975 Printer command

Device Control Block (DCB)

Word	
0	Control word
1	Start address
2	Not used
3	Not used
4	Not used
5	Chain address
6	Byte count
7	Data address

Control Word (DCB Word 0)

Bit	**Meaning**	
0	Chaining flag*	
1	Reserved	
2	Input flag	
3	Reserved	
4	Reserved	
5–7	Cycle-steal address key	
8–15	Attachment-directed operation	
	FF	Start cycle-steal read ID
	FD	Start cycle-steal attachment status
	EC	Execute attachment storage
	E8	Load attachment storage
	E2	Initialize attachment
	EA	Load attachment storage and initialize
	E4	Read attachment storage
	D0	Start diagnostic

*Chaining is supported for all Start Control commands except Start Diagnostic (D0). See start CS attachment status.

Cycle-Steal Status Words*

Word 0—Residual Address

Bit	**Meaning**
0–15	Address of last-attempted data transfer

*Listed for the Multifunction Attachment Feature when used with Asynchronous/Synchronous Communications. See also cycle-steal status words for the 4975 Printer and Binary Synchronous Communications.

Multifunction

Word 1

Bit	Meaning
0	Overrun error
1	Time-out
2	Not used
3	DCB reject
4	Not used
5	Communications error
6	Break
7	Communications error
8	Not used
9	Communications interface error
10	Not used
11	Not used
12	Not used
13	Not used
14	Not used
15	Not used

Word 2

Bit	Meaning
0	Data terminal read (DTR)
1	Data set read (DSR)
2	Request to send (RTS)
3	Clear to send (CTS)
4	Not used
5	Not used
6	Echoplex
7	Receive data lead (when set to 1 = space state)
8–15	Communications panel switch settings

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device-dependent status available
1	Delayed command reject
2	Incorrect-length record
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Printer Attachment—5200 Series

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,3,5,7
60	Prepare	0,3,5,7
6F	Device Reset	0,3,7
70	Start I/O	0,1,2,3,5,6,7
7C	Start Control	0,1,2,3,5,6,7
7F	Start Cycle-Steal Status	0,1,2,3,5,6,7

Device Control Block (DCB)—Data Stream Mode

Word		
0	Control word	
1	Not used (0's)	
2	Not used (0's)	
3	Mode control	Not used (0's)
4	Not used (0's)	
5	Chain address	
6	Byte count	
7	Data address	
	0 7	*8 15*

Control Word (DCB Word 0)

Bit	**Meaning**
0	Chaining flag
1	Not used
2	Input flag
3, 4	Not used
5–7	Cycle-steal address key
8	Print complete attention interrupt
9–12	Not used
13	Data transfer mode
14, 15	Not used

5200 Series

Device Control Block (DCB)—Emulation Mode

Word		
0	Control word	
1	Forms length	Not used (0's)
2	Skip modifier	Space modifier
3	Mode control	Not used (0's)
4	Character set selection	Not used (0's)
5	Chain address	
6	Byte count	
7	Data address	
	0 *7*	*8* *15*

Control Word (DCB Word 0)

Bit	**Meaning**
0	Chaining flag
1	Not used
2	Input flag
3, 4	Not used
5–7	Cycle-steal address key
8	Forms parameter
9–11	Not used
12	Forms spacing control
13	Data transfer mode
14	Use words 3 and 4
15	Not used

Device Control Block (DCB)—Start Control Command

Word	
0	Control word
1	Attachment storage start address/summary mask
2	Not used
3	Not used
4	Not used
5	Chain address
6	Byte count
7	Data address

0 15

5200 Series

Control Word (DCB Word 0)

Bit	Meaning	
0	Chaining flag	
1	Not used	
2	Input flag	
3, 4	Not used	
5–7	Cycle-steal address key	
8–15	Attachment control operation:	
	11111111	Start Cycle-Steal Read ID
	11111110	Read Device Definition Data
	11111101	Read Attachment Definition
	11110010	Clear Attachment Storage
	11101100	Execute Attachment Storage
	11101000	Load Attachment Storage
	11101010	Load Attachment Storage and Intialize
	11101110	Write Device Definition Data
	11100100	Read Attachment Storage
	11100010	Initialize Attachment
	11010000	Start Diagnostic 0
	10100000	Enable Options
	10100001	Disable Options
	10110000	Read Error Log
	10110001	Read Error Log and Clear

Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	Address of last-attempted data transfer (security mode only)

Word 1—Program Status

Bit	Meaning
0	Not ready
1	Device error
2	Not used
3	Wait
4–7	Not used
8	Communications error
9–11	Not used
12	End of forms or forms jam
13–15	Not used

Word 2—Printer Status/Printer Return Code

Bit	Meaning
0	Mode
1	Status available (bits 8–15)
2	Debug/security mode
3–7	Not used
8–15	Printer return code*

*See *IBM Series/1 Printer Attachment—5200 Series Description*, GA34-0240.

Word 3—Attachment Status

Bit	**Meaning**
0	Initialized
1	Attachment storage checksum error
2	Device defined
3	Storage incompatibility error
4	Device ready
5–7	Residual key
8–11	Not used
12	Attachment hardware error
13	Attachment read-only-storage checksum error
14	Attachment storage data error detected
15	Not used

Word 4—Printer ID

Bit	**Meaning**
0–7	Defined printer ID
8–15	Hardware printer ID

Word 5—Forms Length/Line Density

Bit	**Meaning**
0–7	Forms length—Emulation Mode
8–15	Line density—Emulation Mode

Hex	**Meaning**
09	8 LPI
0C	6 LPI

In Data Stream mode, Status Word 5 is not used.

Word 6—Character Density/Character Set

Bit	Meaning
0–7	Character density—Emulation Mode
8–15	Character set—Emulation Mode

Bits 0–7:

Hex	Meaning
0A	10 CPI
0F	15 CPI

Bits 8–15:

Hex	Meaning
0	International
1	United States/Canada
2	Austria/Germany
3	Belgium
4	Brazil
5	French Canadian
6	Denmark/Norway
7	Finland/Sweden
8	France
9	Italy
A	Japan
B	Katakana
C	Portugal
D	Spain
E	Spanish speaking
F	United Kingdom

In Data Stream mode, Status Word 6 is not used.

Word 7

Not used

Interrupt Condition Codes Reported

CC0, CC2, CC3, CC4, CC7

Interrupt Information Byte (IIB)

Condition code	IIB contents
0	FF (hex), Request to Read Attachment Error Log Interrupt
2	Cycle-steal interrupt status byte (ISB)
3	Always zero
4	A printer return code

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device dependent status available
1	Delayed command reject
2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage
6	Protect check
7	Interface data check

Communications Feature—Programmable Multiline Attachment

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
50	Write Data	0,1,5,6,7
60	Prepare	0,1,5,7
6F	Device Reset	0,7
70	Start	0,1,5,6,7
7C	Start Control	0,1,5,6,7
7D	Start Diagnostic 1	0,1,5,6,7
7E	Start Diagnostic 2	0,1,5,6,7
7F	Start Cycle-Steal Status	0,1,5,6,7

Device Control Block (DCB)—General Format

Word		
0	Control word	
1	Not used	Not used
2	Timer 1	
3	Timer 2*	
4	Not used	
5	Chain address–must be even address	
6	Byte count	
7	Data address	
	0	*15*

*Dual function word. In transmit, it contains Timer 2 and PCI information. In receive, it contains only PCI information.

Multiline

Device Control Block (DCB)—Set Mode and Set Control (Asynchronous)

Word		
0	Control word	
1	Bit rate constant	Line control character
2	Line control character	Line control character
3	Line control character	Line control character
4	Line control character	Line control character
5	Chain address	
6	Byte count	
7	Data address	
	0 7	8 15

Device Control Block (DCB)—Set Mode (Synchronous)

Word		
0	Control word	
1	Bit rate constant	Line control character
2	Line control character	Line control character
3	Line control character	Line control character
4	Line control character	Line control character
5	Chain address	
6	Quantity of synchronization characters (1 or 2)	
7	Address of synchronization character	
	0 7	8 15

Multiline

Control Word (DCB Word 0)

Bit	**Meaning**	
0	Chaining flag	
1	Program-controlled interrupt	
2	Input flag	
3, 4	Not used—zeros	
5–7	Cycle-steal address key	
8–15	Operation	
	00000000	Transmit
	00000001	Transmit end
	00010001	Transmit end with pre-receive
	00000010	Transmit allow break
	00000011	Transmit end allow break
	00010011	Transmit end allow break with pre-receive
	00000100	Receive
	00000101	Receive with time-out
	00010100	Receive with block check character
	00010101	Receive with time-out and block check character
	00100100	Receive with echo-plex
	00100101	Receive with time-out and echo-plex
	00110100	Receive with echo-plex and block check character
	00110101	Receive with echo-plex, time-out, and block check character
	01000100	Receive transparent
	01000101	Receive transparent with timer
	01100100	Receive transparent with echo-plex
	01100101	Receive transparent with echo-plex and timer
	01110100	Read adapter buffer
	00000110	Ring monitor
	00000111	Ring monitor with time-out
	00001000	Data terminal ready (DTR) enable
	00001001	DTR enable with time-out
	00001010	DTR enable with answertone
	00001011	DTR enable with answertone and time-out

00001100	DTR disable
00011101	Set control*
00001110	Program delay
00001111	Reset
00001101	Not supported. If issued, ISB bit 3 (DCB specification check) is set equal to 1.

*The attachment is placed in asynchronous mode with 8 data bits, no parity, and 2 stop bits.

Multiline

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0	Overrun
1	Time-out
2	Not used
3	DCB reject
4	Not used
5	Parity error detected on receive
6	Break
7	Stop bit error
8	Not used
9	Modem interface error
10, 11	Not used—zeros
12	Error during pre-receive
13–14	Not used—zeros
15	Adapter buffer status

Word 2

Bit	Meaning
0	Data terminal ready
1	Data set ready
2	Request to send
3	Clear to send
4	External clocks
5	Data carrier detect
6	Echo-plex
7	Receive data lead (when set to 1, equals the mark state)
8–15	Indicator panel setting

Interrupt Condition Codes Reported

CC0, CC1, CC2, CC3

Interrupt Information Byte (IIB)

Condition code	IIB contents
0, 3	Always zeros
1	Program-controlled interrupt identifier
2	Cycle-steal interrupt status byte (ISB)

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

Programmable Two-Channel Switch Feature

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read Device ID	0,7
21	Read Device Status Word	0,7
22	Read Sync Word	0,7
23	Read Diagnostic Wrap Word	0,7
40	Write Common I/O Release	0,3,4,7
41	Write Request Connection	0,3,4,7
42	Write Sync Word	0,5,7
43	Write Resume	0,3,4,7
44	System Reset to Common I/O	0,3,7
4F	Write Console Ack	0,5,7
50	Write Emergency Release	0,3,4,7
51	Write Emergency Connect Enable	0,3,4,7
52	Write Emergency Connect	0,3,4,7
53	Write Diagnostic Sync Word	0,3,5,7
54	Block Operate I/O to Common I/O	0,3,7
5F	Write Diagnostic Wrap Word	0,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7

Device Status Word

Bit	Meaning
0	Configuration information
1, 2	Status of switch
3	Program/manual mode
4	IPL from remote source
5	System reset from remote system
6–9	IPL designation
10	Request for connection received and pending
11	Request for connection interrupt pending
12	Request for connection received and pending
13	Service mode
14	Block operate I/O mode
15	Reserved

Interrupt Condition Codes Reported

CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents	
4	Bit 0	Write sync word command
	Bit 1	Read sync word command
	Bit 2	Write diagnostic sync word command
	Bit 3	Write request connection command
	Bit 4	Write common I/O release
	Bit 5	Write emergency connect command
	Bit 6	Write emergency release command
	Bit 7	IPL, system reset, or input from console received

Communications Feature—SDLC

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1,2,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,5,6,7
7D#	Start Diagnostic 1	0,1,2,5,6,7
7E#	Start Diagnostic 2	0,1,2,5,6,7
7F	Start Cycle-Steal Status	0,1,2,5,6,7
F0	Halt I/O	N/A

#Not supported by the 4950 processor

Device Control Block (DCB)

Word		
0	Control word	
1	Timer 1	Timer 2
2	Not used (zeros)	
3	Not used (zeros)	
4	Status address	
5	Chain address	
6	Byte count	
7	Data address	
	0	15

Control Word (DCB Word 0)

Bit	Meaning
0	Chaining flag
1	Not used—zero
2	Input flag
3	Not used—zero
4	Suppress exception (SE)
5–7	Cycle-steal address key
8	Half rate
9	NRZI coding
10	Enable terminal
11	Disable terminal
12	Pad (leading)
13	Secondary/primary
14	Transmit operation
15	Hold line active (HLA)

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0–15	Residual byte count

SDLC

Word 2

Bit	**Meaning**
0	Overrun
1	Abort
2	Long frame
3	Block check error
4	Time-out
5	Idle detected
7	Modem interface error
8–12	Not used—zeros
13	Business machine clock selected
14	Answertone jumper installed
15	Modem delay jumper installed

Word 3

Bit	**Meaning**
0	Data terminal ready
1	Data set ready
2	Request to send
3	Clear to send
4	Ring indicator
5	Half rate selected
6	Transmit mode latch
7	Not used—zero
8–15	Secondary station address

Residual Status Block (RSB)

Word 0

Bit	**Meaning**
0–15	Residual byte count

Word 1

Bit	Meaning
0	End of chain (EOC)
1–7	Not used—zero
8	Overrun
9	Abort
10	Long frame
11	Block check error
12–14	Not used—zero
15	No exception (NE)

Interrupt Condition Codes Reported

CC2, CC3, CC4#, CC6#, CC7

Not reported by the 4950 processor

Interrupt Information Byte (IIB)

Condition code	IIB contents
2, 6	Cycle-steal interrupt status byte
3	Bit 0 suppressed exception; bits 1–7 are zeros
4, 7	Always zeros

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4950, 4952, or 4953 processor

Series/1 to PC Attachment

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,7
43*	Clear Interface	0,1,2,5,6,7
44*	IPL Request	0,1,2,5,6,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70*	Start Write	0,1,2,5,6,7
71*	Start Read	0,1,2,5,6,7
7C	Start Control Store	0,1,2,5,6,7
7D#	Start Diagnostics	0,1,2,5,6,7
7F	Start Cycle Steal Status	0,1,2,5,6,7
F0	Halt I/O	N/A

* Used only under loaded microcode control

Used only under ROS control

Device Control Block (DCB) for the Start Control Store Command (Hex 7C)

Word	
0	DCB control word
1	Attachment storage start address
2	Operation dependent information
3	Not used (0's)
4	Not used (0's)
5	Chain address
6	Data byte count
7	Data address

0 *15*

Control Word (DCB Word 0) for the Start Control Store Command (Hex 7C)

Bit	Meaning
0	Chaining flag
1	Not Used (0)
2	Input flag
3–4	Not Used (0)
5–7	Cycle-steal address key
8–15	Attachment Control Operation

Hex	Attachment Control Operation
E8	Load Attachment Storage
E2	Initialize Attachment
EA	Load Attachment Storage And Initialize
FD	Read Attachment Definition
E4	Read Attachment Storage
F2	Clear Attachment Storage
D0*	Start Diagnostic 0

* Used under ROS control only

Operation Dependent Information (DCB Word 2)

DCB word 2 is used only for E2, E4, E8, and EA operations.

Bit	Meaning
0	Reverse inhibit
1	Checksum inhibit
2	Clear storage
3–4	Reserved (must be zero)
5–7	Function ID
8–11	Reserved (must be zero)
12–15	Paging

Series/1 to PC

Device Control Block (DCB) for the Start Write Command (Hex 70)

Word		
0	DCB control word	
1	Station address	Reserved
2	Not used	
3	DCB ID	Reserved
4	Not used	
5	Chain address (must be even address)	
6	Data byte count	
7	Data address	

0 *15*

Control Word (DCB Word 0) for the Start Write Command (Hex 70)

Bit	Meaning
0	Chaining flag
1	Program-controlled interrupt (PCI)
2	Input flag
3–4	Not Used (0)
5–7	Cycle-steal address key
8–15	Device Control Operation

Hex	Device Control Operation
00	No-op
02	Set IPL
04	Status Request
08	Read Request
06	Write Request
0C	Write Data End
0E	Broadcast Message

Device Control Block (DCB) for the Start Read Command (Hex 71)

Word		
0	DCB control word	
1	Station address	Reserved
2	Not used (0's)	
3	DCB ID	Reserved
4	Residual station block address (must be even)	
5	DCB chaining address (must be even)	
6	Data byte count	
7	Data address (must be even, bit 15=0)	
	0	15

Control Word (DCB Word 0) for the Start Read Command (Hex 71)

Bit	Meaning
0	Chaining flag
1	Program-controlled interrupt (PCI)
2	Input flag
3	Not Used (0)
4	Suppress Exception Flag
5–7	Cycle-steal address key
8–15	Device Control Operation

Hex	Device Control Operation
00	No-op
02	Specific Read
12	Non-specific Read

Series/1 to PC

Device Control Block (DCB) for the Start Diagnostics Command (Hex 7D)

Word	
0	DCB control word
1	Not used (0's)
2	Not used (0's)
3	Not used (0's)
4	Not used (0's)
5	Not used (0's)
6	Data byte count (must be 8)*
7	Data address (must be even)*
	0 15

*used only when word 0, bit 13 is set to 1.

Control Word (DCB Word 0) for the Start Diagnostics Command (Hex 7D)

Bit	Meaning
0–1	Not Used (0)
2	Input flag
3–4	Not Used (0)
5–7	Cycle-steal address key
8–12	Not used
13	Cable Wrap Test
14	On-Card Wrap Test
15	Internal Card Test

Note: Bit 15 is highest priority test, followed by bit 14, then bit 13.

Device Control Block (DCB) for the Start Cycle Steal Status Command (Hex 7F)

Word	
0	DCB control word
1	Not used
2	Not used
3	Not used
4	Not used
5	Not used
6	Data byte count
7	Data address
	0 15

Control Word (DCB Word 0) for the Start Cycle Steal Status Command (Hex 7F)

Bit	**Meaning**
0–1	Not Used (0)
2	Input flag
3–4	Not Used (0)
5–7	Cycle-steal address key
8–15	Not used

Series/1 to PC

Cycle-Steal Status Words (Loaded Microcode Control)

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0–15	Residual count

Word 2

Bit	Meaning
0	Station not found
1	Data transfer parity error
2	Frame refused
3–4	Not Used
5	Attachment buffer full
6	Busy, no specific response
7	Receive error
8–15	Not used

Word 3

Bit	Meaning
0–5	Not used
6	Receive enable
7	Receive frame in buffer
8–15	Not used

Word 4

Bit	Meaning
0–15	Frame byte count

Word 5

Word 5 is the DCB address contained in the IDCB.

Word 6

Word 6 contains the subchannel current DCB address.

Words 7–14

These words contain the current DCB.

Cycle-Steal Status Words (ROS Control)

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0	Initailized
1	Attachment storage checksum error
2	Attachment storage parity error
3	Storage compatibility error
4	Attachment hardware error
5–7	Residual key
8–11	Not used
12	Attachment storage address error
13	Function ID compare error
14–15	Not used

Word 2

Bit	Meaning
0–3	Not used
4	Deviced defined
5–7	Function ID
8–11	ROS level

Word 3

Bit	Meaning
0–15	Last DCB Address

Series/1 to PC

Words 4–14

These words are not used and are all FF (all bits on).

Residual Status Block (RSB) under Loaded Microcode Control

Word 0

Bit	Meaning
0–15	Residual count

Word 1

Bit	Meaning
0	End of chain
1–14	Not used—zeros
15	No exception

Word 2

Bit	Meaning
0–15	Residual address

Word 3

Bit	Meaning
0–7	Station address (word 1 of DCB)
8–15	DCB byte 0 (bits 0–7 of current DCB control word)

Word 4

Bit	Meaning
0–15	Data address (word 7 of DCB)

Interrupt Condition Codes Reported

CC0, CC1, CC2, CC3

Interrupt Information Byte (IIB)*

Bit	ISB meaning
0	Suppress Exception
1–7	Not Used

* Used only with CC3

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device-dependent status available
1	Delayed command reject
2	Incorrect-length record
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Series/1—System/370 Channel Attachment Feature

Series/1 I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
21	Read Status	0,1,2,5,7
60	Prepare	0,5,7
62	Disable System/370 Device Address	0,1,2,3,5,7
63	Enable System/370 Device Address	0,1,2,3,4,5,7
64	Set System/370 Device End	0,1,2,3,4,5,7
65	Set Attention to System/370	0,1,2,3,4,5,7
6F	Device Reset	0,7
70	Start	0,1,2,3,4,5,7
71	Start Diagnostic	0,1,4,5,7
7F	Start Cycle-Steal Status	0,1,2,5,7

Series/1 Device Control Block (DCB)

Word	
0	Control word
1	Not used (not fetched)
2	Not used (not fetched)
3	Not used (not fetched)
4	Device parameter word 4 (status address)
5	Not used (not fetched)
6	Count
7	Data address
	0 … *15*

Control Word (DCB Word 0)

Bit	**Meaning**
0, 1	Not used—must be zeros
2	Input flag
3	Not used—must be zero
4	Suppress exception
5–7	Cycle-steal address key
8–15	Not used—must be zeros

Series/1–S/370

Series/1 Device Status Word

Bit	**Meaning**
0	Not used—zero
1	Online
2	System/370 busy or chaining
3	System/370 reset
4	System/370 interface disconnect
5	Time-out
6	System/370 error
7	Attention command
8–12	System/370 device address
13–15	System/370 command

Series/1 Cycle-Steal Status Words

Word 0

Bit	**Meaning**
0–15	Residual address

Word 1

Bit	**Meaning**
0–15	Residual byte count

Word 2

Bit	**Meaning**
0–3	Residual data indicator (RDI)
4–15	Not used—zeros

Word 3

Same as Series/1 Device Status Word

Series/1 Residual Status Block (RSB)

Word 0

Bit	Meaning
0–15	Residual byte count

Word 1

Bit	Meaning
0	Always set to 1
2–14	Not used—zeros
15	No exception

Word 2

Bit	Meaning
0–3	Residual data indicator (RDI)
4–15	Not used—zeros

Series/1 Interrupt Condition Codes Reported

CC2, CC3, CC4, CC7

Series/1 Interrupt Information Byte (IIB)

Condition code	IIB contents	
2	Cycle-steal interrupt status byte	
3, 4, 7	**Bit**	**Meaning**
	0	Permissive device end
	1	Online
	2	Chaining device end
	3	System/370 reset
	4	System/370 interface disconnect
	5	Time-out
	6	Chaining attention
	7	Attention command

Series/1–S/370

Series/1 Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Not used
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

System/370 I/O Commands

Hex	Command
00	Test I/O
01	Write
02	Read Buffer
03	No-Operation
04	Sense
05	Erase/Write
06	Read Modified
0B	Select
0D	Diagnostic Write
0E	Diagnostic Read
0F	Erase All Unprotected
33	Subsystem Load Enable
E4	Sense I/O

System/370 Data for a Sense Command

Bit	Meaning
0	Command reject
1	Intervention required
2	Bus out check
3	Not used—zero
4	Data check
5	Unit specify
6	Control check
7	Not used—zero

System/370 Data for a Sense I/O Command

Byte	**Data (hex)**
0	FF
1	49
2	50
3	0X

X = 0, Inhibit IPL jumper installed
X = 1, Inhibit IPL jumper not installed

System/370 Status Byte

Bit	**Meaning**
0	Attention
1	Status modifier
2	Control unit end
3	Busy
4	Channel end
5	Device end
6	Unit check
7	Not used—zero

Synchronous Communications Single-Line Control

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1,2,5,6,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,5,6,7
71	Start Control	0,1,2,5,6,7
72	Start Modification	0,1,2,5,6,7
7D	Start Diagnostic 1	0,1,2,5,6,7
7E	Start Diagnostic 2	0,1,2,5,6,7
7F	Start Cycle-Steal Status	0,1,2,5,6,7

Device Control Block (DCB)—SDLC/HDLC

Word		
0	Control word	
1	Timer 1	Timer 2
2	Not used (0's)	
3	DCB ID	Not used (0's)
4	Status address	
5	Chaining address	
6	Byte count	
7	Data address	
	0	*15*

Control Word (DCB Word 0)—SDLC/HDLC

Bit	**Meaning**
0	Chaining flag
1	Program-controlled interrupt (PCI)
2	Input flag
3	Not used—zero
4	Suppress exception (SE)
5–7	Cycle-steal address key
8	Not used—zero
9	NRZI coding
10	Enable
11	Disable
12	Pad/control
13	Secondary/primary
14	Transmit operation
15	Hold line active (HLA)

SCSLC

Device Control Block (DCB)—BSC

Word	0	15
0	Control word	
1	Not used	
2	Not used	
3	DCB ID	Not used (0's)
4	Not used	
5	Chaining address	
6	Byte count	
7	Data address	

Control Word (DCB Word 0)—BSC

Bit	**Meaning**
0	Chaining flag
1	Program-controlled interrupt (PCI)
2	Input flag
3	Not used—zero
4	Not used—zero
5–7	Cycle-steal address key
8	Not used—zero
9	Set ASCII mode
10	Enable
11	Disable
12	Start timer
13	Transmit operation
14	Exit transparent
15	Not used—zero

Device Control Block (DCB)—Leased Operation—SDLC/HDLC/BSC

Word																
0	X	0	0	0	0	K	E	Y	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	X	X	X	0	0
2	Not used															
3	Not used															
4	Not used															
5	Chaining address															
6	Not used															
7	Not used															
	0															15

SCSLC

Control Words (DCB Words 0–1)—SDLC/HDLC/BSC

Word 0

Bit	Meaning
0	Chaining
1–4	Not used—zeros
5–7	Cycle-steal address key
8–15	Not used—zeros

Word 1

Bit	Meaning
0–10	Not used—zeros
11	PCI
12	Duplex mode
13	Installation test
14	Not used—zero
15	Not used—zero

Device Control Block (DCB)—X.21 Switched Operation

<table>
<tr><td>Word</td><td colspan="3"></td></tr>
<tr><td>0</td><td>X 0 X 0 X</td><td>K E Y</td><td>0 0 0 0 0 X X X</td></tr>
<tr><td>1</td><td colspan="3">Operation dependent</td></tr>
<tr><td>2</td><td colspan="3">Not used (0’s)</td></tr>
<tr><td>3</td><td colspan="3">Not used (0’s)</td></tr>
<tr><td>4</td><td colspan="3">Operation dependent</td></tr>
<tr><td>5</td><td colspan="3">Operation dependent</td></tr>
<tr><td>6</td><td colspan="3">Operation dependent</td></tr>
<tr><td>7</td><td colspan="3">Operation dependent</td></tr>
<tr><td></td><td>0</td><td></td><td>15</td></tr>
</table>

Control Word (DCB Word 0) Switched Line—SDLC/HDLC/BSC

Bit	**Meaning**	
0–4	Operation (used with bits 8–15)	
	X0000	Set mode (bit 0 = chaining flag)
	00101	Network provided information
	00101	Auto-answer
	00000	Clear
5–7	Cycle-steal address key	
8–15	Modifier bits	
	00000000	Set mode
	00000001	Network provided information
	00000010	Auto-answer
	00000100	Clear

SCSLC

Cycle-Steal Status Words—SDLC/HDLC

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0–15	Residual byte count

Word 2

Bit	Meaning
0	Overrun
1	Abort
2	Long frame
3	Block check error
4	Time-out
5	Idle detected
6	Nonproductive receive time-out
7	DCE interface error
8–12	Not used—zeros
13	Local attach 1
14, 15	Not used—zeros

Word 3

Bit	Meaning
0	Data terminal ready
1	Data set ready
2	Request to send
3	Clear to send
4, 5	Not used—zeros
6	Transmit mode
7	Not used—zero
8–15	Secondary station address

Word 4

Bit	Meaning
0–8	Not used—zeros
9	X.21 switched operation
10	V.35 operation
11	Not used—zero
12	Local attach 2 operation
13	Not used—zero
14	IPL allowed
15	BSC operation

Word 5

Bit	Meaning
0–7	X.21 interface state
8	Transmit interface line (X.21)
9	Receive interface line (X.21)
10	Indicator interface line (X.21)
11	Control interface line (X.21)
12	Not used—zero
13–15	DTE time-out (X.21)

Cycle-Steal Status Words—BSC

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0	Overrun
1	Time-out
2	DCE interface error
3	Block check error
4	Multipoint transmit error
5	Not used—zero
6	Multipoint tributary jumper installed
7	Improper configuration
8–15	Multipoint address

SCSLC

Word 2

Bit	Meaning
0	Data terminal ready
1	Data set ready
2	Request to send
3	Clear to send
4, 5	Not used—zeros
6	Transmit mode
7	Not used—zero
8–15	Indicator panel switch setting

Word 3

Bit	Meaning
0–8	Not used—zeros
9	X.21 switched operation
10	V.35 operation
11	Not used—zero
12	Local attach 2 operation
13	Not used—zero
14	IPL allowed
15	BSC operation

Word 4

Bit	Meaning
0–7	X.21 interface state
8	Transmit interface line (X.21)
9	Receive interface line (X.21)
10	Indicator interface line (X.21)
11	Control interface line (X.21)
12	Not used—zero
13–15	DTE time-out (X.21)

Interrupt Condition Codes Reported—SDLC/HDLC/BSC

CC0, CC1, CC2, CC3, CC4

Interrupt Information Byte (IIB)—SDLC/HDLC/BSC

Condition code	IIB contents
0–1	DCB identifier
2	Cycle-steal interrupt status byte (ISB)
3*	Bit 0 on = Permissive device end
4	Bit 0 on = Successful DCE initiated clear Bit 7 on = Unsuccessful DCE initiated clear

*Applies to SDLC/HDLC only

Interrupt Status Byte (ISB)—SDLC/HDLC/BSC

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2*	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

*Applies to BSC only

Telephone Communications Attachment Feature

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1,3,5,6,7
50	Write Initial Attachment Storage Load	0,1,3,5,6,7
60	Prepare	0,1,3,5,6,7
6F	Device Reset	0,1,3,5,6,7
70	Start Cycle-Steal	0,1,3,5,6,7
71	Load Adapter Parameters	0,1,3,5,6,7
72	Display Adapter Control Block	0,1,3,5,6,7
7D	Diagnostic Check Sum	0,1,3,5,6,7
7E	Controller Storage Load	0,1,3,5,6,7
7F	Start Cycle-Steal Status	0,1,3,5,6,7

Device Control Block (DCB)

Word		
0	Control Word	
1	Operation modifier	Function ID
2	Timer 1	Timer 2 (pace)
3	DCB ID	Audio output level
4	Key response index pointer	
5	Chaining address	
6	Byte count	
7	Data address	
	0	15

Telephone Comm.

Control Word (DCB Word 0)

Bit	Meaning
0	Chaining flag
1	PCI
2	Input flag
3, 4	Not used—zeros
5–7	Cycle-steal address key
8–14	Not used–zeros
15	Key response flag

Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	Address of last-attempted data transfer

Word 1—Residual Count

Bit	Meaning
0–15	Number of bytes remaining to be transferred when the error occurred

Word 2—Device Status

Bit	Meaning
0	On hook
1	Coupler cut-through not detected
2	Invalid dial digit
3	No dial tone
4	Number busy
5	Dialing error
6	No answer
7	Disconnected
8	Received time-out
9	Invalid generate programmed tone
10	Disconnect error
11	Key tone received
12–15	Key tone codes

Word 3—Device Status

Bit	Meaning
0–7	Not used
8, 9	Checksum error
10	Audio output level selected
11	Automatic gain control locked
12–15	Audio input level

Interrupt Condition Codes Reported

CC0, CC1, CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents
3, 4	Cycle-steal interrupt status byte (ISB)

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect-length record
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Teletypewriter Adapter Feature

I/O Commands

Hex	Command	I/O instruction CCs reported
10	Read	0,1,3,5,7
11	Read	0,1,3,5,7
20	Read ID	0,5,7
50	Write	0,1,3,5,7
51	Write	0,1,3,5,7
60	Prepare	0,5,7
6E	Reset to Diagnostic Wrap	0,1,3,5,7
6F	Device Reset	0,1,3,5,7

Device Status Word

Device status is reported via condition codes.

Interrupt Condition Codes Reported

CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	IIB contents
2, 3, 4, 6, 7	Always zeros

Timer Feature

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
24	Read Timer Value	0,1,3,5,7
25	Read Timer Mode	0,1,3,5,7
60	Prepare	0,5,7
64	Set Timer Period and Initial Value	0,1,3,5,7
65	Set Timer Mode	0,1,3,5,7
66	Set Timer Periodic	0,1,3,5,7
67	Set Timer Aperiodic	0,1,3,5,7
6E	Stop Timer	0,1,3,5,7
6F	Device Reset	0,7

Device Status Word

Device status is reported via condition codes.

Interrupt Condition Codes Reported

CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	IIB contents
2, 3, 4, 6, 7	Always zeros

Two Channel Switch Feature

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
23	Read Status Word	0,1,5,7
50	Console Acknowledge	0,1,5,7
53	Reserve	0,1,3,4,5,7
60	Prepare	0,5,7
63	Reset and Connect	0,1,3,5,7
66	Start Operations Monitor	0,1,3,4,5,7
6C	Reset Operations Monitor	0,7
6F	Device Reset	0,7

Device Status Word

Bit	Meaning
0	CIO connected
1	Control mode in effect
2	Operations monitor time-out
3	Reserve
4	Operations monitor run
5	Operations monitor time-out incurred
6, 7	Zeros
8	CIO connection alert
9	Control mode alert
10	IIPL blocked
11	Polarity
12, 13	Operations monitor initial period
14, 15	Operations monitor warning period

Interrupt Condition Codes Reported

CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	IIB contents	
2	DPC interrupt status byte (ISB)	
3	Always zero	
4	Bits 0, 1	Always zeros
	Bit 2	Connect go-ahead
	Bit 3	Ready
	Bit 4	Operations monitor warning
	Bit 5	Always zero
	Bit 6	Console attention
	Bit 7	Console reset
6	Same as CC4	
7	Same as CC4	

Interrupt Status Byte (ISB)

Bit	ISB meaning
0, 1	Always zeros
2	Connect go-ahead
3	Ready
4	Operation monitor warning
5	Always zero
6	Console attention
7	Console reset

Note: Bits 0–7 are always zeros for CC2

4950/5170 Model 495 Asynchronous

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
50*	DPC Write	0,1,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,5,7
7C#*	Start Control	0,1,5,7
7D*	Start Diagnostic 1	0,1,5,7
7F	Start Cycle-Steal Status	0,1,5,7
F0	Halt I/O	N/A

Supported by the 4950 processor for
set expanded mode only
* Not supported by the IBM Personal Computer Display

Device Control Block (DCB) with Word 0, Bit 8 Off

Word	
0	Control word
1	Not used
2	Timer 1
3	Timer 2
4	Not used
5	Chain address (must be even address)
6	Byte count
7	Data address

0 *15*

Control Word (DCB Word 0) with Bit 8 Off

Bit	Meaning	
0	Chaining flag	
1	Not used—zero	
2	Input flag—data cycle-steal to storage	
3–4	Not used—zero	
5–7	Cycle-steal address key	
8–15	Operation	
	00	Transmit
	01	Transmit end
	02#	Transmit allow break
	03#	Transmit end allow break
	04	Receive
	05	Receive with time-out
	06*	Ring monitor (RS232 only)
	07*	Ring monitor with time-out (RS232 only)
	08	DTR enable
	09	DTR enable with time-out
	0A+	DTR enable with answertone
	0B+	DTR enable with answertone and time-out
	0C	DTR disable
	0E	Program delay
	0F	Reset
	1D	Set control
	74	Read adapter buffer
	11*##	Transmit end with pre-receive
	13*##	Transmit end, allow break with pre-receive
	44*##	Receive transparent
	45*##	Receive transparent with time-out

* Not supported by the IBM Personal Computer Display

+ Answertone will not be generated

Break ignored on the IBM Personal Computer Display

Supported by the 5170 Model 495 (terminal/host adapter) only

4950/5170 Asynch

Device Control Block (DCB) with Word 0, Bit 8 On

Word		
0	Control word	
1	Bit-rate constant	Line-control character
2	Line-control character	Line-control character
3	Line-control character	Line-control character
4	Line-control character	Line-control character
5	Chain address (must be even)	
6	Not used (0)	
7	Not used (0)	
	0	15

Control Word (DCB Word 0) with Bit 8 On

Bit	Meaning	
0	Chaining flag	
1	Not used—zero	
2	Input flag—data cycle-steal to storage	
3–4	Not used—zero	
5–7	Cycle-steal address key	
8	Bit 8 is on (1)	
9	mode:	
	0	Asynchronous mode
	1	Synchronous mode (not supported)
10–11	Character size:	
	00	5 bits
	01	6 bits
	10	7 bits
	11	8 bits
12–13	Stop bits (in asynchronous mode)	

	01	1 stop bit used
	11	2 stop bits used
14	Parity type (0–odd; 1–even)	
15	Parity (0–disabled; 1–enabled)	

Device Control Block (DCB)—Start Control Command in set expanded mode

Word	
0	Contains the value X'01'
1	Not used
2	Not used
3	Bit 14 – Attention interrupt Bit 15 – Continuous receive
4	Not used
5	Not used
6	Must contain all zeros (0)
7	Not used

0 *15*

Cycle-Steal Status Words

Word 0

Bit	**Meaning**
0–15	Residual address

4950/5170 Asynch

Word 1

Bit	Meaning
0	Overrun
1	Time-out
2	Not used
3	DCB reject
4	Not used
5	VRC error
6	Break detected
7	Stop-bit error
8	Not used—zero
9	Modem interface error
10–11	Not used—zeros
12	Error during pre-receive, adapter buffer overflow
13–14	Not used—zeros
15	Characters in adapter buffer

Word 2

Bit	Meaning
0	Data terminal ready
1	Data set ready
2	Request to send
3	Clear to send
4–15	Not used—zeros

Interrupt Condition Codes Reported

CC2, CC3, CC4, CC6

Interrupt Information Byte (IIB)

Condition code	IIB Contents
2,6	Cycle-steal interrupt status byte (ISB)
3	Always zeros
4	Attention Character

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check (always zero)
7	Interface data check

4950/5170 Model 495 Disk/Diskette Adapter

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,5,7
7F	Start Cycle Steal Status	0,1,5,7
F0	Halt I/O	N/A

Device Control Block (DCB)

<table>
<tr><th>Word</th><th colspan="2"></th></tr>
<tr><td>0</td><td colspan="2">Control word</td></tr>
<tr><td>1</td><td colspan="2">Not used</td></tr>
<tr><td>2</td><td colspan="2">RBA (bits 4-19)</td></tr>
<tr><td>3</td><td>RBA
(bits 0-3)</td><td>Not used</td></tr>
<tr><td>4</td><td colspan="2">Residual status byte address</td></tr>
<tr><td>5</td><td colspan="2">Chain address</td></tr>
<tr><td>6</td><td colspan="2">Byte count</td></tr>
<tr><td>7</td><td colspan="2">Data address</td></tr>
<tr><td></td><td>0</td><td>15</td></tr>
</table>

Control Word (DCB Word 0)

Bit	Meaning
0	Chaining flag
1	Not used (0)
2	Input flag
3	Not Used (0)
4	Suppress exception flag
5–7	Cycle-steal address key
8–15	Cycle steal operation command

Hex	Command
01	Recalibrate
10	Read data
16	Read media parms
20	Write data
21	Write data with read verify
26	Load media parms
27	Format diskette

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0–15	Residual count

Word 2

Bit	Meaning
0–3	Number of soft error retries (CRC or ECC check)
4–11	Reserved
12	Data unsafe
13	File not ready
14	Reserved
15	Soft error retry

4950 Disk/Diskette

Word 3

Bit	Meaning
0–3	Number of retries (no-record-found error)
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check
8	Attachment interface parity check
9	Reserved
10	Common adapter ROS parity check
11	Reserved
12	Common adapter RAM parity check
13	Reserved
14–15	Write error retries

Word 4

Bit	Meaning
0	Hard error
1	Attachment-detected interface parity check
2	Attachment global timeout
3	Control mark
4	Interrupt code
5	Write fault
6	Attachment equipment check
7	Write error
8	Adapter storage parity error
9	Data error in data field
10	Bad cylinder
11	Missing address mark in data field
12	Cycle-steal status error
13	End of disk or diskette
14	Interrupt code
15	No data

Word 5

Bit	Meaning
0	CRC or ECC check
1	Overrun
2	No index
3	Not writable
4	Wrong cylinder
5	Invalid command parameter
6	Missing address mark
7	Disk unit timeout or hardware check
8–10	Head address
11–12	Unit select
13	Seek incomplete
14	Home
15	Not ready

Word 6

Bit	Meaning
0–1	Reserved
2	Cache write through
3	Reserved
4	Cache enabled
5–6	Reserved
7	Cache installed
8–15	Read hit percentage (BCD coded)

Word 7

Bit	Meaning
0–15	Reserved (all zeros)

Word 8

Bit	Meaning
0–15	Last DCB address

Words 9–10

Bit	Meaning
0–15	Logical record number

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Words 11–12

Bit	Meaning
0–15	Reserved

Word 13

Bit	Meaning
0	Sector Size Invalid
1	Maximum RBA Address Invalid
2–15	Reserved

Interrupt Condition Codes Reported

CC2, CC3

Interrupt Information Byte (IIB)

Bit	Meaning
0	Permissive Device End
1–7	Always zeros

Interrupt Status Byte (ISB)

Bit	Meaning
0	Device status available
1	Delayed command reject
2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check (always zero)
7	Interface data check

4962 Disk Storage Unit

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,3,5,7
7F	Start Cycle-Steal Status	0,1,3,5,7

Device Control Block (DCB)

Word		
0	Control word	
1	Seek control word	
2	Physical sector count	Flag
3	Cylinder address	
4	Head selection	Sector number
5	Chain address	
6	Byte count	
7	Data address	
	0	*15*

Control Word (DCB Word 0)

Bit	Meaning	
0	Chaining flag	
1	Not used—zero	
2	Input flag	
3	Not used—zero	
4	Not used—zero	
5–7	Cycle-steal address key	
8–15	Modifier bits (operation)	
	00000001	Write data
	00000010	Write sector ID
	00000011	Write sector ID skewed
	00001001	Read data
	00001100	Read verify
	00001010	Read sector ID
	00001011	Read sector ID skewed
	00001000	Read diagnostic
	00000101	Seek
	00000111	Seek recalibrate

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0	End of track
1	Sync check
2	Echo check
3	No record found
4	Write gate check
5	Serializer/deserializer check
6	PLO out of sync check
7	Unsafe
8	File data check
9	Seek check
10	Brake failure
11	Write unsafe
12	Select unsafe
13	Servo unsafe
14	Attachment buffer parity check
15	Not ready or power off

Word 2

Bit	Meaning
0–9	Zero
10–15	Sector number (write error); Sector number plus one (no write error)

Word 3

Reserved

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Interrupt Condition Codes Reported

CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents
2	Cycle-steal interrupt status byte (ISB)
3, 4	Always zeros

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1, 2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

4963 Disk Subsystem

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
40	Load Disk Unit Control Block 0	0,5,7
41	Attachment General Diagnostic Test	0,5,7
48	Load Sense Diagnostic Word 1	0,5,7
49	Load Sense Diagnostic Word 2	0,5,7
4D	Force End Operation	0,5,7
4E	Attachment Storage Diagnostic	0,5,7
4F	Diagnostic Reset Disk Unit Control	0,5,7
52	Load Seek Required Address Direct	0,5,7
53	Load Seek Control Direct	0,5,7
54	Sense Disk Unit	0,5,7
55	Sense Disk Unit Diagnostic Bytes 1, 2, 3	0,5,7
56	Sense Disk Unit Diagnostic Bytes 1, 2, 3 Multiple Sample Test	0,5,7
57	Sense Disk Unit Diagnostic Wrap	0,5,7
5A	Disk Speed Timing Diagnostic	0,5,7
5D	Disk Unit Control Diagnostic	0,5,7
60	Prepare	0,5,7
6F	Device Reset	0,5,7

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Hex	Command	I/O instruction CCs reported
70	Start	0,1,2,5,6,7
7D	Start Cycle-Steal Diagnostic	0,1,2,5,6,7
7F	Start Cycle-Steal Status	0,1,2,5,6,7

Device Control Block (DCB)

Word				
0	Control word			
1	Byte 0 Flag			Byte 1 Sector/record
2	0 0	Bits 1–5 Head	6 6	Bits 7–15 Cylinder
3	Not used			Byte 1 Scan/repeat count
4	Residual status block address			
5	DCB chain address			
6	Byte count			
7	Starting data address			
	0			15

Control Word (DCB Word 0)

Bit	Meaning
0	Chaining flag
1	Not used
2	Input flag
3	Not used
4	Suppress exception
5–7	Cycle-steal address key
8–15	Disk operation field (modifier bits). See note on following page.

00000000	Seek
00000001	Recalibrate
00001001	Calibrate
00001000	Overlapped seek
00001011	Time seek diagnostic
0001X000	Read data
0001X001	Read verify
0001X010	Read data repeat
0001Y011	Read disk unit data buffer diagnostic
0001X100	Read ID
0001X101	Read extended
0001X110	Read diagnostic record 1
0001X111	Read diagnostic record 2
0010X000	Write data
0010X001	Write data with read verify
0010X010	Write data repeat
0010X011	Write data repeat with read verify
00101101	Write ID with read verify
00101111	Write ID extended with read verify
1010X001	Write data security with read verify
0011X000	Scan equal
0011X010	Scan high or equal
0011X001	Scan low or equal

Note: An X in position 12 means that bit 12 specifies whether or not this operation invokes the automatic seek function. If bit 12 equals 0, and the head-and-cylinder address specified in the DCB is different than the one at which the access mechanism is currently positioned, the disk unit moves the access mechanism to the DCB-specified location before performing the defined operation; if bit 12 equals 1, seeking is inhibited. A Y in position 12 means that it does not matter what value bit 12 has for the operation to be performed correctly.

Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	DCB/data address of the last attempted cycle-steal transfer associated with a start command

Word 1—Residual Count

Bit	Meaning
0–15	Residual byte count of data for last DCB operation

Word 2—Retry Counts Word 1

Bit	Meaning
0–3	Cyclic redundancy check (CRC)
4–7	Write echo check
8–11	Missing sector pulse
12	Data unsafe
13	Disk unit not ready
14, 15	Spare

Word 3—Retry Counts Word 2

Bit	Meaning
0–3	No record found
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check
8	Disk unit interface parity check
9–11	Not used
12–15	Write error

Word 4—Error Status Word 1

Bit	Meaning
0	Permanent error
1	Interface parity check
2	Attachment time-out
3	Alternate sector processed
4	Temporary error retry
5–7	Disk unit configuration
	000 Not used
	001 Not used
	010 Models 29A and B (no fixed heads)
	011 Models 64A and B (no fixed heads)
	100 Disk unit not attached
	101 Not used
	110 Models 23A and B (eight fixed heads)
	111 Models 58A and B (eight fixed heads)
8	Scan not equal
9	Scan equal
10	Attachment equipment check
11	Write error
12	Cycle-steal status error
13	End of disk
14	Attachment local time-out
15	Disk unit interface error

Word 5—Error Status Word 2

Bit	Meaning
0	CRC
1	Disk unit parity check
2	Disk unit interface parity check
3	Write gate return check
4	No record found
5	Invalid operation parameter
6	Missing sector pulse
7	Disk unit time-out
8	Fixed head not selected
9	Brake applied
10	Track unavailable
11	Disk unit command error
12	Data unsafe
13	Seek incomplete
14	Home
15	Not ready

Word 6—Last DCB Address

Bit	Meaning
0–15	Address of last DCB used

Word 7—Current Head and Cylinder

Bit	Meaning
0–15	Head and cylinder address of current disk location

Word 8—Previous Head and Cylinder

Bit	Meaning
0–15	Head and cylinder address of previous disk location

Word 9—Flag, Sector, Record

Bit	Meaning
0–15	Last record on which a read or write operation was attempted during last DCB operation

Word 10—Head and Cylinder

Bit	Meaning
0–15	Head and cylinder of last record on which a read or write operation was attempted

Word 11—Disk Unit Diagnostic Sense Bytes 1 and 2

(Diagnostic sense byte 1)

Bit	Meaning
0	On track
1	Linear region normal
2	Index/sector pulse
3	Out direction
4	Not drive out
5	Not drive in
6	Tag parity error
7	Read-only-storage error

(Diagnostic sense byte 2)

Bit	Meaning
0	Behind home
1	Missing clocks divided by 2
2	Not missing clocks error latch
3	Coil current low
4	Missing servo signal
5	Off data track
6	Not missing position error signal
7	Counter 5 in sync

Word 12—Disk Unit Diagnostic Sense Byte 3 and Wrap Byte

Bit	Meaning
0	Not shift
1	Not off track write
2	Inside automatic gain control window
3	Not automatic gain control freeze
4	Demand pulsing
5	Not read and write
6	Not servo protect and write
7	Illegal move
8–15	Disk unit cylinder number or interface error bits

Residual Status Block (RSB)

Word 0—Residual Count

Bit	Meaning
0–15	Not used

Word 1—Residual Status Block Flags

Bit	Meaning
0	End of chain
1	Retry
2–14	Not used
15	No exception

Word 2—Retry Counts Word 1

Bit	Meaning
0–3	CRC
4–7	Write echo check
8–11	Missing sector pulse
12	Data unsafe
13	Not ready
14, 15	Not used

Word 3—Retry Counts Word 2

Bit	Meaning
0–3	No record found
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check
8	Disk unit interface parity check
9–11	Not used
12–15	Write error

Word 4—Error Status Word

Bit	Meaning	
0–2	Not used	
3	Alternate sector processed	
4	Temporary error retry	
5–7	Configuration	
	000	Not used
	001	Not used
	010	Models 29A and B (no fixed heads)
	011	Models 64A and B (no fixed heads)
	100	Disk unit not attached
	101	Not used
	110	Models 23A and B (eight fixed heads)
	111	Models 58A and B (eight fixed heads)
8	Scan not equal	
9	Scan equal	
10–12	Not used	
13	End of disk	
14, 15	Not used	

Interrupt Condition Codes Reported

CC0, CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	IIB contents
2, 6	Cycle-steal interrupt status byte (ISB) with bit 2 always returned as zero
3, 7	Cycle-steal interrupt status byte (ISB) with bits 3–7 not used
0, 4	Always zeros

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

4964 Diskette Unit

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1,2,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,5,7
7F	Start Cycle-Steal Status	0,1,2,5,7

Device Control Block (DCB)

Word		
0	Control word	
1	Seek control word	
2	Format data word	
3	Sector length	Cylinder
4	Head selection	Sector number
5	Chain address	
6	Byte count	
7	Data address	
	0	15

Control Word (DCB Word 0)

Bit	Meaning	
0	Chaining flag	
1	Not used—zero	
2	Input flag	
3	Not used—zero	
4	Not used—zero	
5–7	Cycle-steal address key	
8–15	Modifier bits (operation)	
	00000001	Write data/data AM
	0000010	Format track
	00000011	Wirte data/control AM
	00001001	Read data
	00001100	Read verify
	00001010	Read sector ID
	00000101	Seek
	00000111	Seek recalibrate

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

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Word 1

Bit	Meaning
0	Not used—zero
1	No data field found
2	Overrun
3	Control AM
4	File not ready
5	No record found
6	End of track
7	File data check
8	Incorrect index time
9	Invalid diskette surface
10–12	Not used—zeros
13	No erase current
14	No write gate
15	Erase current stuck on

Word 2

Bit	Meaning
0–7	N-byte (last search argument)*
8–15	C-byte (last search argument)

*Same format as N-byte in DCB word 3

Word 3

Bit	Meaning
0–7	H-byte (last search argument)
8–15	R-byte (last search argument)

Interrupt Condition Codes Reported

CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents
2	Cycle-steal interrupt status byte (ISB)
3	Always zero
4	00 (hex) two-sided diskette 80 (hex) one-sided diskette

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

4965 Storage and I/O Expansion Unit (Model 1)

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,5,6,7
7D	Start Cycle-Steal Diagnostic	0,1,2,5,6,7
7F	Start Cycle-Steal Status	0,1,2,5,6,7

Device Control Block (DCB)

Word	
0	Control word
1	Parameter word 1
2	Parameter word 2
3	Parameter word 3
4	Residual status block address
5	DCB chain address
6	Byte count
7	Data address

0 *15*

Control Word (DCB Word 0)

Bit	Meaning	
0	Chaining flag	
1	Not used—must be zero	
2	Input flag	
3	Not used—must be zero	
4	Suppress exception	
5–7	Cycle-steal address key	
8–15	Modifier field	
	00000000	Seek
	00000010	Recalibrate head
	0000X100	Format track
	0000X101	Format track defective
	00000111	Set FM/MFM bit
	0000X110	Verify format track/data compare
	S001X000	Read data
	S001X001	Read verify/cyclic redundancy check
	S001X010	Read verify/compare data
	0001X100	Read sector ID
	0001X110	Read diagnostic record
	S010X000	Write data/data address marker
	S010X001	Write data/control address marker
	S010X010	Write data with read verify
	01010000	Read attachment storage
	01100001	Write attachment storage

Note: The S in bit position 8 denotes spiral read/write as an option. The X in bit position 12 denotes automatic seek as an option.

4965 (Model 1)

Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	DCB/data address/residual status block address

Word 1—Residual Count

Bit	Meaning
0–15	Residual byte count of data of last DCB operation

Word 2—Retry Counts Word 1

Bit	Meaning
0	Storage data check count
1	Invalid storage address count
2	Protect check error count
3	Interface data check
4–6	Seek errors retry count
7	Not used
8–15	Control address markers encountered count

Word 3—Retry Counts Word 2

Bit	Meaning
0	Not used
1	Parity error count
2–7	CRC check error retry count or data verify error count
8, 9	Not used
10–15	No record found error count

Word 4—Retry Counts Word 3

Bit	Meaning
0, 1	Not used
2–7	No data found error count
8, 9	Underrun/overrun error count
10–15	Equipment check error count

Word 5—Diagnostic Status

Bit	Meaning
0–15	Special diagnostic use

Word 6—Error Status Word 1

Bit	Meaning
0	Permanent error
1	Attachment detected parity check
2	Attachment time-out
3	Not used
4	Not used
5	Wrong type of diskette selected
6	Head seek error
7	Not used
8	Write/erase gate
9	Not used
10	Attachment equipment check
11	Overrun/underrun
12	Read verify error
13	Related error
14	Not used
15	Temporary error retry

4965 (Model 1)

Word 7—Error Status Word 2

Bit	Meaning
0	Cyclic redundancy check
1	Not used
2	Exceeded control AM count
3	Not used
4	No record found
5	No data found
6	Control address marker found
7	ID check
8	Not used
9	Diskette not up to speed
10	Not used
11	End of track
12–14	Not used
15	Diskette unit not ready

Word 8

Not Used

Word 9—Movable Head Status Word

Bit	Meaning
0–3	Not used
4	Head access latch 0
5	Head access latch 1
6–13	Not used
14	Heads at cylinder 0
15	Not used

Word 10—Last DCB Address

Bit	Meaning
0–15	Address of last DCB used

Word 11—Current Diskette Head and Cylinder

Bit	Meaning
0–4	Not used
5	Head
6–8	Not used
9–15	Cylinder

Word 12—Previous Diskette Head and Cylinder

Bit	Meaning
0–4	Not used
5	Head
6–8	Not used
9–15	Cylinder

Residual Status Block (RSB)

Word 0—Residual Count

Always zeros

Word 1—Residual Status Block Flags

Bit	Meaning
0	End of chain
1	Hardware retry
2–14	Not used
15	No exception

4965 (Model 1)

Word 2—Retry Counts Word 1

Bit	Meaning
0	Storage data check count
1	Invalid storage address count
2	Protect check error count
3	Interface data check
4–6	Seek errors retry count
7	Not used
8–15	Control AMs encountered count

Word 3—Retry Counts Word 2

Bit	Meaning
0	Not used
1	Parity error count
2–7	CRC check error retry count or data verify error count
8, 9	Not used
10–15	No record found error count

Word 4—Retry Counts Word 3

Bit	Meaning
0, 1	Not used
2–7	No data found error count
8, 9	Underrun/overrun error count
10–15	Equipment check error count

Word 5—Error Status Word

Bit	Meaning
0–14	Not used
15	Soft error retry

Interrupt Condition Codes Reported

CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	IIB contents
2	Cycle-steal interrupt status byte (ISB)
3, 4, 6, 7	Bit 0 = Permissive device end (Refer to RSB contents.)

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device-dependent status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check
8–15	Device address

4965 Storage and I/O Expansion Unit (Models 30D and 60D)

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read Device ID	0,5,7
43	Clear Error Log	0,1,2,5,6,7
45	Write Cache Control	0,1,2,5,6,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,5,6,7
7C	Start Control	0,1,2,5,6,7
7D	Start Cycle-Steal Diagnostic	0,1,2,5,6,7
7F	Start Cycle-Steal Status	0,1,2,5,6,7

Device Control Block (DCB) for a Start Command

Word	
0	Control word
1	Parameter word 1
2	Parameter word 2
3	Parameter word 3
4	Residual status block address
5	DCB chain address
6	Byte count
7	Data address

0 *15*

Control Word (DCB Word 0)

Bit	Meaning	
0	Chaining flag	
1	Not used—must be zero	
2	Input flag	
3	Not used—must be zero	
4	Suppress exception	
5–7	Cycle-steal address key	
8–15	Modifier field	
	R0000001	Recalibrate
	R0010000	Read data
	R0010001	Read verify
	R0010100	Read ID
	R0011000	Read disk direct
	R0010110	Read data recovery
	R0100000	Write data
	R0100001	Write data/read verify
	R0100010	Write data repeat
	R0100100	Write format
	R0100101	Write ID
	R0100111	Write ID extended

Note: All Start operations have an inhibit retry (R) bit. This bit, along with the suppress exception (SE) bit, has the following meaning:

1. If R = 0, error retries are performed. If R = 1, no error retries are performed, but error-recovery procedures (ERPs) are performed. This bit is used for diagnostic purposes only, and should remain 0 for normal operation.
2. If SE = 0, no error retires nor ERPs are performed. If SE = 1, error retries and ERPs are performed.

4965 (30D and 60D)

Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	DCB/data address/residual status block address

Word 1—Residual Count

Bit	Meaning
0–15	Residual byte count of data of last DCB operation

Word 2—Retry Counts Word 1

Bit	Meaning
0, 1	No record found temporary error count
2, 3	Temporary seek error count
4, 5	ECC correction temporary error count
6, 7	Disk interface parity check temporary error count
8	Storage data check
9	Invalid storage address
10	Protect check
11	Interface data check
12, 13	Not used
14	Logical record number (bit 2)
15	Logical record number (bit 3)

Word 3—Logical Record Number

Bit	Meaning
0–15	Relative block address bits 4–19

Word 4—Error Status Word 1

Bit	Meaning
0	Permanent error
1	Attachment detected parity check
2	Attachment time-out
3	ECC corrected
4	Temporary error retry
5	Cache parity check
6	Attachment equipment check
7	Reserved and not used
8	Disk controller interface error (local time-out)
9	Data/control error
10	Disk error
11	ECC inverted
12	Cycle-steal status error
13	Model 60D
14	Cable Z continuity check
15	Cable Y continuity check

Word 5—Error Status Word 2

Bit	Meaning
0	CRC/ECC check
1	No record found
2	Over/under run
3	DMA parity error
4	No sync character found
5	Transfer ready stop
6	Data encode error
7	Write protect error
8, 9	Disk detected parity check
10	Invalid head switch
11	Reserved and not used
12	Cable open
13	Interface check
14	Invalid command sequence
15	Disk not ready

4965 (30D and 60D)

Word 6—Cache Information

Bit	**Meaning**
0, 1	Reserved and not used
2	Cache write through
3	Cache prefetch invoked
4	Cache enabled
5	Cache used for this operation
6	Total read hit
7	Cache installed
8–15	Read hit ratio % (BCD coded)

Word 7—Error Sense and Attachment Status

Bit	**Meaning**
0–7	Last attachment error encountered
8–11	Internal error modifier
12–15	Number of disabled cache pages

Word 8—Last DCB Address

Bit	**Meaning**
0–15	Starting address of last DCB used by attachment

Word 9—Disk Diagnostic Word 1

Bit	Meaning
0	Speed 0
1	Index
2	Sector
3	Device busy
4	Data time
5	Unsafe
6	DBO parity error
7	Write gate return
8	DE unsafe
9	Card unsafe
10	Sync unsafe
11	Servo unsafe
12	Oper unsafe
13	Seek unsafe
14	DBO parity error
15	Motor/processor error

Word 10—Disk Diagnostic Word 2

Bit	Meaning
0	Command bit 0
1	Command bit 1
2	Command bit 2
3	Command bit 3
4	Command bit 4
5	Command bit 5
6	Command bit 6
7	Command bit 7
8	Diagnostic mode 2 = 0
9	Diagnostic mode 1 = 0
10	Version A1
11	Home
12	Behind home
13	Spare
14	DBO parity error
15	Safe speed fine

4965 (30D and 60D)

Word 11—Disk Diagnostic Word 3

Bit	Meaning
0	Base line adj. wrap
1	North polarity
2	Recal. settle, invoke, seek error
3	Automatic gain control hold
4	A2 unsafe encode
5	A1 unsafe encode
6	A0 unsafe encode
7	Overcurrent latched
8	Up control/ramp
9	Forward/+ reverse drive
10	Motor is slow
11	Motor is fast
12	Up motor drive
13	Safe speed coarse
14	Enable ID search
15	Motor error

Word 12—Disk Diagnostic Word 4

Bit	Meaning
0	Diagnostic mode 2 = 1
1	Diagnostic mode 1 = 0
2	P4 motor
3	P3 motor
4	P2 motor
5	P1 motor
6	Hall sensor 2
7	Hall sensor 1
8	Index or sector
9	Track type 1
10	Track type 0
11	PES 1 (2 tracks)
12	PES 2
13	PES 3
14	PES 4
15	PES 5 (1/8 track)

Word 13—Disk Diagnostic Word 5

Bit	Meaning
0	Servo/seek
1	TK foll/settle
2	Seek mode
3	Missing sector
4	ID mode
5	ID in sync
6	On track fine
7	On track coarse
8	Diagnostic mode 2 = 0
9	Diagnostic mode 1 = 1
10	Head select B
11	Head select A
12, 13	Reserved and not used
14	Drive out
15	Drive in

Word 14—Attachment Diagnostic Word 1

Bit	Meaning
0–7	Disk controller interrupt byte 0
8	Reserved and not used
9	Controller model jumper
10–15	Reserved and not used

Word 15—Attachment Diagnostic Word 2

Bit	Meaning
0–7	Reserved and not used
8–15	Disk buffer word count

4965 (30D and 60D)

Residual Status Block (RSB)

Word 0—Residual Count

This word is reserved and is always zeros.

Word 1—Residual Status Block Flags

Bit	**Meaning**
0	End of chain
1	Hardware retry
2–14	Reserved and not used
15	No exception

Word 2—Retry Counts Word 1

Bit	**Meaning**
0, 1	No record found retry count
2, 3	Seek error retry count
4, 5	Number of records that are ECC corrected
6, 7	Disk interface parity check retry count
8	Storage data check count
9	Invalid storage address retry
10	Protect check retry
11	Interface data check retry
12, 13	Reserved and not used
14	Logical record number (bit 2, word 3)
15	Logical record number (bit 3, word 3)

Word 3—Logical Record Number

Bit	**Meaning**
0, 1	Reserved and not used
2, 3	See word 2, bits 14, 15
4–15	Relative block address

Word 4—Cache Information

Bit	Meaning
0, 1	Reserved and not used
2	Cache write through
3	Cache prefetch invoked
4	Cache enabled
5	Cache used for this operation
6	Total read hit
7	Cache installed
8–15	Read hit ratio % (BCD coded)

Word 5—Error Sense and Attachment Status

Bit	Meaning
0–3	Disk controller interface error
4–7	Data path when error encountered
8–11	Internal error modifier
12–15	Number of disabled cache pages

Interrupt Condition Codes Reported

CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	IIB Contents
2	Cycle-steal Interrupt Status (ISB)
3, 4, 6, 7	Bit 0 = Permissive device end (Refer to RSB contents.)

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device-dependent status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

4966 Diskette Magazine Unit

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,5,7
7D	Start Cycle-Steal Diagnostic	0,1,2,5,7
7F	Start Cycle-Steal Status	0,1,2,5,7

Device Control Block (DCB)

Word			
0	*Control word*		
	X 0 X 0 X	*Addr key*	Device dependent
1	Device parameter 1		
2	Device parameter 2		
3	Device parameter 3		
4	Residual status block address		
5	DCB chain address		
6	Byte count		
7	Data address		
	0		*15*

Control Word (DCB Word 0)

Bit	Meaning	
0	Chaining flag	
1	Not used	
2	Input flag	
3	Not used	
4	Suppress exception	
5–7	Cycle-steal address key	
8–15	Diskette operation field	
	00000000	Seek (movable carriage/heads)
	00000001	Recalibrate home
	00000010	Recalibrate head
	00000011	Recalibrate/unload
	0000X100	Format track
	0000X101	Format track defective
	0000X110	Verify format track/data compare
	0001X000	Read data
	0001X001	Read verify/CRC
	0001X010	Read verify/data compare
	0001X100	Read sector ID
	0001X110	Read diagnostic
	01010000	Read attachment device buffer
	0010X001	Write data/control address marker
	0010X000	Write data/data address marker
	0010X010	Write data with read verify/data address marker
	01100001	Write attachment device buffer

Note: An X in position 12 means that bit 12 specifies whether or not this operation invokes the automatic seek function. If bit 12 equals 0, and the head-and-cylinder address specified in the DCB is different than the one at which the access mechanism is currently positioned, the disk unit moves the access mechanism to the DCB-specified location before performing the defined operation; if bit 12 equals 1, seeking is inhibited.

Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	DCB/data address/residual status block address

Word 1—Residual Address

Bit	Meaning
0–15	Residual byte count of data of last DCB operation

Word 2—Retry Counts Word 1

Bit	Meaning
0, 1	Movable carriage errors
2–7	CRC error or data verify errors
8–10	Seek errors
11–15	Control address markers encountered

Word 3—Retry Counts Word 2

Bit	Meaning
0, 1	Not used
2–7	No record found errors
8–10	Not used
11	Parity error
12	Storage data check
13	Invalid storage address
14	Protect check
15	Interface data check

Word 4—Retry Counts Word 3

Bit	Meaning
0, 1	Not used
2–7	No data found errors
8, 9	Underrun/overrun errors
10–15	Equipment check errors

Word 5—Diagnostic Status

Bit	Meaning
0–15	Special diagnostic use

Word 6—Error Status Word 1

Bit	Meaning
0	Permanent error
1	Attachment detected parity check
2	Attachment time-out
3	Movable carriage summary error
4	Not used
5	Wrong type of diskette
6	Head seek error
7	Not used
8	Write gate
9	Erase gate
10	Attachment equipment check
11	Overrun/underrun
12	Read verify error
13, 14	Not used
15	Temporary error retry

Word 7—Error Status Word 2

Bit	Meaning
0	CRC check
1–3	Not used
4	No record found
5	No data found
6	Control address marker found
7	ID check
8	Not used
9	Diskette not up to speed
10	Diskette not selected
11	End of track
12–14	Not used
15	Diskette unit not ready

Word 8—Movable Carriage Status Word 1

Bit	Meaning	
0	Operation	
1	Movable carriage error	
2	Parity check	
3	Movable carriage wrap	
4	Command reject	
5	Motion check	
6	Invalid operation	
7	Not used	
8–11	Check modifier codes	
	00000000	Reserved
	00000001	Carriage bed malfunction 1
	00000010	Carriage bed malfunction 2
	00000011	Picker malfunction 1
	00000100	Picker malfunction 2
	00000101	Fail to eject
	00000110	Fail to pick up
	00000111	Diskette window failed to close
	00001000	Diskette window failed to open
	00001001	Carriage bed operation aborted
	00001010	Reserved
	00001011	Command out of sequence
	00001100	Command reject, improper state 1
	00001101	Command reject, improper state 2
	00001110	Reserved
	00001111	Reserved
12–14	Special diagnostic use	
15	Movable carriage recalibrate	

Word 9—Movable Carriage Status Word 2

Bit	Meaning
0	Cover open latch
1	In orientation latch
2	Cover open
3	Not used
4–11	Special diagnostic use
12, 13	Not used
14	Heads at cylinder 0
15	Recalibrate home complete

Word 10—Last DCB Address

Bit	Meaning
0–15	Address of last DCB used

Word 11—Current Diskette Head and Cylinder Position

Bit	Meaning
0–4	Diskette position number
5	Head selected
6–8	Not used
9–15	Cylinder number

Word 12—Previous Diskette Head and Cylinder Position

Bit	Meaning
0–4	Diskette position number
5	Head selected
6–8	Not used
9–15	Cylinder number

Residual Status Block (RSB)

Word 0—Residual Count

Bit	Meaning
0–15	Not used

Word 1—Residual Status Block Flags

Bit	Meaning
0	End of chain
1	Hardware retry
2–14	Not used
15	No exception

Word 2—Retry Counts Word 1

Bit	Meaning
0, 1	Movable carriage errors
2–7	CRC errors or data verify errors
8–10	Seek errors
11–15	Control address markers encountered

Word 3—Retry Counts Word 2

Bit	Meaning
0, 1	Not used
2–7	No record found errors
8–10	Not used
11	Parity check error
12	Storage data check
13	Invalid storage address
14	Protect check
15	Interface data check

Word 4—Retry Counts Word 3

Bit	Meaning
0, 1	Not used
2–7	No data found errors
8, 9	Underrun/overrun errors
10–15	Equipment check errors

Word 5—Error Status Word

Bit	Meaning
0–14	Not used
15	Temporary error

Interrupt Condition Codes Reported

CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	IIB Contents
2, 6	Cycle-steal interrupt status byte (ISB)
3, 4, 7	Always zeros

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

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I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1,2,5,6,7
41	Attachment Gen. Diag.	0,1,2,5,6,7
42	Attachment Cache Diag.	0,1,2,5,6,7
43	Clear Error Log	0,1,2,5,6,7
45	Write Cache Control	0,1,2,5,6,7
48	Load Diagnostic Word 1	0,1,2,5,6,7
49	Load Diagnostic Word 2	0,1,2,5,6,7
4C	Enable Data Collection Mode	0,1,2,5,6,7
4F	Diag. Reset Common Adapter	0,1,2,5,6,7
52	Load Seek Required Addr. Direct	0,1,2,5,6,7
53	Load Seek Control Direct	0,1,2,5,6,7
54	Sense Disk Unit Direct	0,1,2,5,6,7
60	Prepare	0,1,2,5,6,7
6F	Device Reset	0,1,2,5,6,7
70	Start	0,1,2,5,6,7
7C	Start Control	0,1,2,5,6,7
7D	Start Cycle-Steal Diagnostic	0,1,2,5,6,7
7F	Start Cycle-Steal Status	0,1,2,5,6,7

Device Control Block (DCB)—Physical Operations

Word		
0	Control word	
1	0 0 0 0 0 0 0 0	Phy. sector number
2	0	Head/cylinder number
3	Not used (0's)	
4	Residual status block address	
5	DCB chaining address	
6	Byte count	
7	Data address	
	0	15

Control Word (DCB Word 0)

Bit	**Meaning**	
0	Chaining flag	
1	Not used—zero	
2	Input flag	
3	Not used—zero	
4	Suppress exception	
5–7	Cycle-steal address key	
8–15	Modifier bits	
	00000001	Recalibrate
	X0011110	Read Data Recovery Record 1
	X0011111	Read Data Recovery Record 2
	00010100	Read ID
	X0100100	Write Format
	00100101	Write ID
	00110111	Scan Alternate IDs

Note: X = 1 indicates operation is to be performed with ECC inverted. Otherwise, normal ECC is assumed.

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Device Control Block (DCB)—Logical Operations

Word		
0	Control word	
1	Not used (0's)	
2	Relative block address	
3	Rel. block address	Record count
4	Residual status block address	
5	DCB chaining address	
6	Byte count	
7	Data address	
	0	15

Control Word (DCB Word 0)

Bit	Meaning	
0	Chaining flag	
1	Not used—zero	
2	Input flag	
3	Not used—zero	
4	Suppress exception	
5–7	Cycle-steal address key	
8–15	Modifier bits	
	X0010000	Read Data
	X0011000	Read Disk Unit Direct
	X0010001	Read Verify
	00010010	Read Data Repeat
	X0100001	Write Data with Read Verify
	X0100000	Write Data
	00100010	Write Data Repeat
	00110110	Scan Read Single ID

Note: X = 1 indicates operation is to be performed with ECC inverted. Otherwise, normal ECC is assumed.

Device Control Block (DCB)—Scan Operations

Word		
0	Control word	
1	KN(8)	SL(8)
2	Relative block address	
3	RBA(4)	
4	Residual status block address	
5	DCB chaining address	
6	DL(8)	KL(8)
7	Key/data address	

0 *15*

Control Word (DCB Word 0)

Bit	**Meaning**	
0	Chaining flag	
1	Not used—zero	
2	Input flag	
3	Not used—zero	
4	Suppress exception	
5–7	Cycle-steal address key	
8–15	Modifier bits	
	F0110000	Scan Data Equal
	F0110001	Scan data not equal
	F0110010	Scan data low or equal
	F0110011	Scan data low
	F0110100	Scan data high or equal
	F0110101	Scan data high

Note: F = 1 indicates only data length following the key hit is returned to storage. Otherwise, the entire record (256 bytes) containing the key hit is returned.

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Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	DCB/RSB/data address of the last attempted cycle-steal transfer associated with a start command

Word 1—Residual Count

Bit	Meaning
0–15	Residual byte count of data for last DCB operation

Word 2—Error Status

Bit	Meaning
0–3	CRC/ECC check retry count
4–7	Write gate return check retry count
8–11	Sector sync/format retry count
12	Data unsafe retry
13	Disk not ready retry
14	ECC invoked
15	Any soft error retry

Word 3—Error Status

Bit	Meaning
0–3	No record found retry count
4	Storage data check retry
5	Invalid storage address retry
6	Protect check retry
7	Interface data check retry
8	Attachment interface parity check retry
9	Common adapter clock out of sync
10	Common adapter read only storage parity check
11	Sector synchronization parity check
12	Common adapter storage parity check
13	Storage patch rejected
14, 15	Write error retry count

Word 4—Error Status

Bit	Meaning
0	Hard error
1	Attachment detected interface parity check
2	Attachment global time-out
3	Attachment interface cable continuity check
4	Attachment detected premature end
5	Disk unit not attached
6	Attachment equipment check
7	Write error
8	SERDES or storage parity error
9	Data buffer/internal card parity error
10	Channel error check
11	ECC inverted
12	Cycle-steal status error
13	End of disk
14	Attachment local time-out
15	Disk interface error

Word 5—Error Status

Bit	Meaning
0	CRC/ECC check
1	Tag out parity check
2	Channel data parity error
3	Write gate return check
4	No record found
5	Invalid command parameter
6	Sector or format check
7	Disk unit time-out or hardware check
8	Head offset invoked
9	Brake applied
10	Head/track unavailable
11	Disk unit command error
12	Data unsafe
13	Seek incomplete
14	Home
15	Not ready

Word 6—Cache Information

Bit	Meaning
0	Operation end interrupt received
1	Data operation ready interrupt received
2	Cache write through
3	Cache prefetch invoked
4	Cache enabled
5–7	Cache status/failing cache module
	These bits have a dual definition. Under error-free conditions, they have the following meanings:
5	Cache used for this operation
6	Total read hit
7	Cache installed (always 1)
8–15	Read hit ratio percentage (BCD coded)

Word 7—Scan Information

Bit	Meaning
0–3	Spare
4	Scan not hit
5	Scan equal hit
6	Scan high compare
7	Scan low compare
8–15	Scan hit count

Word 8—Last DCB Address

Bit	Meaning
0–15	Address of last DCB fetched

Word 9—Logical Record Number

Bit	Meaning
12–15	High order 4 bits of the RBA

Word 10—Logical Record Number

Bit	Meaning
0–15	RBA of last record processed unless ECC invoked or head offset invoked (low order bits)

Word 11—Disk Unit Diagnostic Sense Bytes 1 and 2

(Diagnostic Sense Byte 1)

Bits	Meaning
0 1 2	
1 1 1	Power not good
1 1 0	PLO out of sync
1 0 1	Disk speed/VCO check
1 0 0	Seek time-out error
0 1 1	Unexpected guard band
0 1 0	Servo off-track error
0 0 1	Guard band 2
0 0 0	System service request
3	On track
4	Guard band
5 6	
1 1	Not used
1 0	Crossing tracks inward
0 1	Crossing tracks outward
0 0	Captured on track or retracted
7	Interrupt

(Diagnostic Sense Byte 2)

Bit	Meaning
0	Odd track
1	Access reset
2	Depress profile
3	Accelerate
4–6	Not used
7	Retract

Word 12—Disk Unit Diagnostic Sense Byte 3 and Wrap Byte

(Diagnostic Sense Byte 3)

Bits	Meaning
0 1 2	
1 1 1	Write and AE unsafe
1 1 0	Not write and AE unsafe w/AE selected
1 0 1	Write and AE select error
1 0 0	AE unsafe w/o AE selected
0 1 1	Write and read or write head off servo
0 1 0	Write and sector overrun
0 0 1	Write and servo not on track
0 0 0	Write and not ready
3, 4	Data unsafe when bits 0, 1, and 2 = 0
5	Not used
6	Sector counter error
7	Card/cable unseated
8–15	Diagnostic wrap byte
	If CSSW4, bit 15 = 1, bits 8–11 mean:
8	Disk unit cable continuity check
9	No control sample received from disk unit
10	Disk unit daisy bus parity error
11	Disk unit interrupt not reset after sense
	If CSSW5, bit 7 = 1, bits 12–15 mean:
12	Disk unit interrupt not received
13	Read or write hardware time-out
14	Hardware check
15	Buffer port address check

Word 13—Attachment Diagnostic

Bit	Meaning
0–2	Failure path
3–7	Number of disabled cache pages
8–15	Error modifier (engineering use only)

Interrupt Condition Codes Reported

CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	Bit	Meaning
2		Interrupt Status Byte (ISB)
3, 4, 6, 7	0	Permissive device end
	1	Scan not hit
	2	Scan equal hit
	3	Scan high compare
	4	Scan low compare
	5–7	Not used

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device dependent status available
1	Delayed command reject
2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

4968 Magnetic Tape Unit

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,3,5,7
7C	Start Control	0,1,2,3,5,7
7E	Start Status	0,1,2,3,5,7
7F	Start Cycle-Steal Status	0,1,2,3,5,7

Device Control Block (DCB)

Word			
0	*Control*	*Addr key*	
	X 0 X 0 X	X X X	0 0 0 0 0 0 0 0
1	4968 operation code		
2	Not used (0's)		
3	Not used (0's)	Repeat count	
4	Residual status block address		
5	DCB chain address		
6	Byte count		
7	Data address		

Word 1 (Tape Unit Operation)

Bit	Meaning	
0–7	Operation Code	
	Hex	**Operation**
	FE	Write record
	FD	Read record
	FB	Write tape mark
	F7	Erase
	EF	Space record forward
	DF	Space record reverse
	EE	Space tape mark forward
	DE	Space tape mark reverse
	B0	Rewind to load point
	69	Security erase/rewind
	30	Rewind/unload
	C0	Set 1600 cpi
	C1	Set 3200 cpi
8–12	Not used—zeros	
13	Extended gap	
14	Not used—zero	
15	Speed select	

Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	DCB, data address, or residual status block address

Word 1—Residual Byte Count

Bit	Meaning
0–15	Residual byte count of the data associated with the last DCB operation

Word 2—Overflow Byte Count

Bit	Meaning
0–15	Number of bytes read in excess of byte count

Word 3—Residual Status Word 1

Bit	Meaning
0	Ready
1	Not used
2	File protect
3	Load point
4	End of tape
5	Tape mark
6	Not used
7	Indents
8, 9	Not used
10	Any error
11–15	Not used

Word 4—Residual Status Word 2

Bit	Meaning
0	Timer
1	Tape controller error
2	Corrected data error
3	Not used
4	Tape controller command reject
5	Attachment parity check
6, 7	Not used
8	Equipment check
9	Not used
10	Attachment time-out
11	Not used
12–15	Retry count

Word 5—Current Status

Bit	Meaning
0	Ready
1	Not used
2	File protect
3	Load point
4	End of tape
5–15	Not used

Word 6—Residual Repeat Count

Bit	Meaning
0–15	Count specified in DCB word 3 less the number of successfule repeat operations

Word 7—Last DCB Address

Bit	Meaning
0–15	Address of last DCB used

Start Status (Current Status Word)

Bit	Meaning
0	Ready
1	Not used
2	File protect
3	Load point
4	End of tape
5–15	Not used

Residual Status Block (RSB)

Word 0—Residual Byte Count

Bit	Meaning
0–15	Byte count specified in DCB word 6, less the number of bytes transferred

Word 1—Residual Status Block Flags

Bit	Meaning
0	End of chain
1	Retry
2–11	Not used
12	Corrected error
13	Tape controller error
14	Incorrect record length
15	No error

Word 2—Overflow Byte count

Bit	**Meaning**
0–15	Number of bytes read in excess of the byte count

Word 3—Residual Address

Bit	**Meaning**
0–15	Address of the last cycle-steal data transfer

Word 4—Error Status Word

Bit	**Meaning**
0	Timer
1	Tape controller error
2	Corrected error
3	Not used
4	Tape controller command reject
5	Attachment parity error
6, 7	Not used
8	Equipment check
9	Not used
10	Attachment time-out
11	Not used
12–15	Retry count

Word 5—Last DCB Address

Bit	**Meaning**
0–15	Starting address of the last DCB used by the 4968

Interrupt Condition Codes Reported

CCO, CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	**IIB contents**	
0	Hex FF—Request to Read Attachment Error Log Interrupt	
2, 6	Cycle-steal interrupt status byte (ISB)	
3, 7	Bit 0	Permissive device end
	Bits 1–7	Always zero
4	Always zero	

Interrupt Status Byte (ISB)

Bit	**ISB meaning**
0	Device dependent status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage check
6	Protect check
7	Interface data check

4969 Magnetic Tape Subsystem

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,3,5,6,7
7E	Start Status	0,1,2,3,5,6,7
7F	Start Cycle-Steal Status	0,1,2,3,5,6,7

Device Control Block (DCB)

Word	
0	Control word
1	Tape unit control
2	Unused
3	Repeat count
4	Residual status block address
5	DCB chain address
6	Byte count
7	Data address
	0 *15*

Control Word (DCB Word 0)

Bit	Meaning	
0	Chaining flag	
1	Not used—must be zero	
2	Input flag	
3	Not used—must be zero	
4	Suppress exception	
5–7	Cycle-steal address key	
8–15	Start cycle-steal diagnostics (zeros for all other commands)	
	00000001	Diagnostic wrap A
	00000010	Diagnostic wrap B
	00000011	Diagnostic wrap C
	00000100	Diagnostic wrap D
	00000101	Diagnostic wrap E
	00000110	Diagnostic wrap F
	00010000	Read diagnostic patch
	00010001	Write diagnostic patch
	00010010	Read only storage diagnostic
	00010011	Diagnostic read
	00010100	Diagnostic write

Tape Controller Operation (DCB Word 1)

Bit	Meaning	
0–7	00110000	Rewind offline
	01110000	Offline
	10110000	Rewind to load point
	11011110	Backspace tape mark
	11101110	Forward space tape mark
	11101111	Forward space record
	11110111	Erase
	11111101	Read record
	11111110	Write record

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Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	DCB address, data address, or residual status block address

Word 1—Residual Byte Count

Bit	Meaning
0–15	Residual byte count of data for last DCB operation

Word 2—Overflow Byte Count

Bit	Meaning
0–15	Number of bytes read in excess of the byte count

Word 3—Residual Status Word 1

Bit	Meaning
0	Ready
1	NRZI (This bit equals 1 for NRZI or 0 for PE)
2	File protect
3	Load point
4	End of tape
5	Tape mark read
6	Tape controller busy
7	Idents read
8	Command sent
9	Not used
10	Any error
11	Not used
12	Tape controller power on
13	Not used
14	Threshold level selected
15	Not used

Word 4—Residual Status Word 2

Bit	Meaning
0	Timer
1	Tape controller error
2	Corrected data error (PE only)
3	CRC parity bit (NRZI only)
4	Tape controller command reject
5	Adapter parity error
6	Buffer parity error
7	Tape controller parity error
8	Equipment check
9	Attachment parity error
10	Attachment local time-out
11	Cycle-steal status error
12	Retry count 0
13	Retry count 1
14	Retry count 2
15	Retry count 3

Word 5—Current Status

Bit	Meaning
0	Ready
1	NRZI
2	File protect
3	Load point
4, 5	Not used
6	Tape controller busy
7–11	Not used
12	Tape controller power on
13–15	Not used

Word 6—Residual Repeat Count

Bit	Meaning
0–15	Count specified in DCB word 3, less the number of successful repeat operations

Word 7—Last DCB Address

Bit	Meaning
0–15	Address of last DCB used

Residual Status Block (RSB)

Word 0—Residual Count

Bit	Meaning
0–15	Byte count specified in DCB word 6, less number of bytes transferred

Word 1—Residual Status Block Flags

Bit	Meaning
0	End of chain
1	Hardware retry
2–11	Not used
12	Corrected error
13	Tape controller parity error
14	Incorrect record length
15	No error

Word 2—Overflow Byte Count

Bit	Meaning
0–15	Number of bytes read in excess of the byte count

Word 3—Residual Address

Bit	Meaning
0–15	Address of the data for the last cycle-steal data transfer

Word 4—Error Status Word

Bit	Meaning
0	Timer
1	Tape controller error
2	Corrected data error (PE only)
3	CRC parity bit (NRZI only)
4	Tape controller command reject
5	Attachment parity error
6	Buffer parity error
7	Tape controller parity error
8	Equipment check
9	Attachment parity error
10	Attachment local time-out
11	Cycle-steal status error
12	Retry count 0
13	Retry count 1
14	Retry count 2
15	Retry count 3

Word 5—Last DCB Address

Bit	Meaning
0–15	Starting address of the last DCB used by the selected tape unit

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Interrupt Condition Codes Reported

CC0, CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	IIB contents	
0, 4	Always zero	
2, 6	Cycle-steal interrupt status byte (ISB)	
3, 7	Bit 0	Permissive device end
	Bits 1–7	Not used

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

4971 Printer and the 4201 Proprinter

Information in this section applies to the IBM 4971 Printer and the IBM 4201 Proprinter.

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,5,7
7F	Start Cycle-Steal Status	0,1,5,7
F0	Halt I/O	N/A

Device Control Block (DCB)

Word		
0	*Control word* X 0 X 0 0 *Addr key*	Control parameters
1	Byte 0 Form length	Byte 1 Overflow line
2	Byte 0 Skip modifier	Byte 1 Space modifier
3	Byte 0 Mode control	Byte 1 Vernier control
4	Font and character set selection	
5	Chain address	
6	Byte count	
7	Data address	
	0	*15*

4971/Proprinter

Control Word (DCB Word 0)

Bit	Meaning
0	Chaining flag
1	Reserved (0)
2	Input flag (always 0)
3, 4	Reserved (0)
5–7	Cycle-steal address key
8	Forms parameter
9–11	Reserved (0)
12	Forms spacing control
13	Reserved (0)
14	DCB identifier
15	No retry

Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	Address of last-attempted data transfer

Word 1—Device Status 1

Bit	Meaning
0	Not ready
1	Not used
2	Not used
3	Wait
4	Not used
5	Not used
6	Not used
7	Not used
8	Not used
9	Not used
10	Not used
11	Overflow
12	End-of-forms
13	Invalid font
14	Not used
15	Invalid length

Word 2—Current Line Position

Bit	Meaning
0–7	Not used—must be 00
8–15	Current line position

Word 3—Forms Length/Overflow Line

Bit	Meaning
0–7	Form length
8–15	Overflow line

Words 4 and 5—Not used

Word 6—Model (Byte 0)/Character Set (Byte 1)

Bit	Meaning
0–11	Not used

Hexadecimal value in bits 12–15	Meaning
0	International/multinational
1	United States and Canada
2	Austria and Germany
3	Belgium
4	Brazil
5	French Canadian
6	Denmark and Norway
7	Finland and Sweden
8	France
9	Italy
A	Japan-English
B	International/multinational
C	Portugal
D	Spain
E	Spanish speaking, other than Spain
F	United Kingdom

Word 7

Not used

4971/Proprinter

Interrupt Condition Codes Reported

CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents
2	Cycle-steal interrupt status byte (ISB)
3, 4	Always zero

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check (always zero)
7	Interface data check

4973 Line Printer

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1,2,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,3,5,7
7F	Start Cycle-Steal Status	0,1,2,3,5,7

Device Control Block (DCB)

Word		
0	Control word	
1	Byte 0 Form length	Byte 1 Overflow line
2	Byte 0 Skip modifier	Byte 1 Space modifier
3	Not used	
4	Reserved for diagnostics	
5	DCB chain address	
6	Byte count	
7	Data address	

0 *15*

Control Word (DCB Word 0)

Bit	Meaning	
0	Chaining flag	
1	Not used—zero	
2	Input flag	
3, 4	Not used—zeros	
5–7	Cycle-steal address key	
8–11	Operation	
	0000	Carriage control and print line
	1000	Set forms parameters, carriage control, and print line
	0100	Initialize belt translator
	0010	Transfer belt translator
	0001	Reserved for diagnostics
12	Forms spacing	
13, 14	Not used—zeros	
15	Retry	

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0	Printer power off
1	Attachment storage check
2	Over temperature
3	Disabled
4	Throat open
5	Cover open
6	Off line test mode
7	Forms jammed
8	Hammer check
9	External interface check
10	Printer interface check
11	Overflow
12	End of forms
13	Belt sync check
14	Belt speed check
15	4973 Model 2 installed

Word 2

Bit	Meaning
0–7	Residual line count
8–15	Current forms position

Word 3

Bit	Meaning
0–7	Form length
8–15	Overflow line

Words 4—6

Reserved for diagnostics

Word 7

Bit	Meaning
0–7	Character set length
8–15	Printer interface status

Word 8–25

Occurrence log

Interrupt Condition Codes Reported

CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents
2	Cycle-steal interrupt status byte (ISB)
3, 4	Always zero

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

4974 Printer

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1,2,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,3,5,7
7F	Start Cycle-Steal Status	0,1,2,3,5,7

Device Control Block (DCB)

Word		
0	Control word	
1	Byte 0 Form length	Byte 1 Overflow line
2	Byte 0 Skip modifier	Byte 1 Space modifier
3	Not used	
4	Diagnostic address	
5	DCB chain address	
6	Byte count	
7	Starting data address	
	0	15

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Control Word (DCB Word 0)

Bit	Meaning
0	Chaining flag
1	Not used—zero
2	Input flag
3, 4	Not used—zeros
5–7	Cycle-steal address key
8	Forms parameter bit
9	Initialize wire image buffer
10	Wire image transfer
11	Diagnostic
12	Forms spacing control
13, 14	Not used—zeros
15	Retry

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

Word 1

Bit	Meaning
0	Printer not ready
1	Printer wire check
2	Printer power check
3	Wait
4	Forms emitter check
5	Margin check
6	Print emitter check
7	Forms stalled
8	Attachment wire check
9	External interface
10	Printer interface check
11	Overflow
12	End of forms
13	Invalid wire image
14	No print emitter
15	Not used—zero

Word 2

Bit	Meaning
0–7	Residual line count
8–15	Current forms position

Word 3

Bit	Meaning
0–7	Forms length
8–15	Overflow line

Word 4–6

Reserved for diagnostics

Word 7

Bit	Meaning
0–7	Logical left margin
8–15	Logical right margin

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Interrupt Condition Codes Reported

CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents
2	Cycle-steal interrupt status byte (ISB)
3, 4	Always zero

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

4975 Printer

I/O Commands

Hex	**Command**
20*	Read ID
60*	Prepare
6F*	Device Reset
70	Start
7C*	Start Control
7F	Start Cycle-Steal Status

*Multi-Function Attachment Feature command

Device Control Block (DCB)

Word		
0	*Control word* X 0 X 0 0 *Addr key*	Control parameters
1	Byte 0 Form length	Byte 1 Overflow line
2	Byte 0 Skip modifier	Byte 1 Space modifier
3	Byte 0 Mode control	Byte 1 Vernier control
4	Font and character set selection	
5	Chain address	
6	Byte count	
7	Data address	
	0	*15*

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Control Word (DCB Word 0)

Bit	Meaning
0	Chaining flag
1	Reserved
2	Input flag (always 0)
3, 4	Reserved
5–7	Cycle-steal address key
8	Forms parameter
9–11	Reserved
12	Forms spacing control
13	Reserved
14	DCB identifier
15	No retry

Cycle Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	Address of last-attempted data transfer

Word 1—Device Status 1

Bit	Meaning
0	Printer hardware problem
1	11 volt power check
2	24 volt power check
3	Wait
4	Forms emitter check (02L and 02R only)
5	Margin check
6	Print emitter check (02L and 02R only)
7	Forms stalled (02L and 02R only)
8	Buffer overrun
9	TP error
10	Used by MFA
11	Overflow
12	End-of-forms
13	Cartridge parameter error (02L and 02R only)
14	No print emitter (02L and 02R only)
15	Invalid length

Word 2—Current Line Position

Bit	Meaning
0–7	Not used—must be 00
8–15	Current line position

Word 3—Forms Length/Overflow Line

Bit	Meaning
0–7	Form length
8–15	Overflow line

Word 4—02L and 02R Only

Byte 0 = Cartridge ID

hex ‘01’	Initial cartridge with standard test functions
hex ‘02’	Special printing cartridge feature (See *IBM Series/1 4975 Printer Special Printing Cartridge Feature Description*, GA34-0250)

Byte 1 = ROS level for cartridge type

Word 5—Printer Hardware Status

Bit	Meaning
0	Not used
1	Mode switch check
2	Left-margin switch check (Not used on models 02L and 02R)
3	End of forms switch check
4	Printer USART check
5	Power supply check
6	Print cartridge check (02L and 02R only)
7–15	Not used

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Word 6—Model (Byte 0)/Character Set (Byte 1)

Bit	**Meaning**
0–3	ROS level
4	draft font
	0 = Multilingual
	1 = Katakana
5–7	Printer model
	001 = 01 models
	010 = 02 models
8–11	Not used

Hexadecimal value in bits 12–15	**Meaning**
0	Multilingual (same as B)
1	United States and Canada
2	Austria and Germany
3	Belgium
4	Brazil
5	Canadian French
6	Denmark and Norway
7	Finland and Sweden
8	France
9	Italy
A	Japan-English
B	Defaults to multilingual (same as 0)
C	Portugal
D	Spain
E	Spanish speaking, other than Spain
F	United Kingdom

Word 7

Reserved for MFA status

Interrupt Condition Codes Reported

CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents
2	Cycle-steal interrupt status byte (ISB)
3, 4	Always zero

Interrupt Status Byte (ISB)*

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

*Same as for the Multi-Function Attachment Feature

4978 Display Station Attachment

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read Device ID	0,1,2,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start Data	0,1,2,5,7
71	Start Image Storage	0,1,2,5,7
72	Start Control Store	0,1,2,5,7
73	Start Field Table	0,1,2,5,7
74	Start Expansion	0,1,2,5,7
7F	Start Cycle-Steal Status	0,1,2,5,7

Device Control Block (DCB)—Start Commands

Word	
0	Control word
1	Operation dependent parameters
2	Operation dependent parameters
3	Operation dependent parameters
4	Operation dependent parameters
5	DCB chaining address
6	Byte count
7	Data storage address

0 *15*

Control Word (DCB Word 0)

Bit	**Meaning**
0	Chaining flag
1	Not used—zero
2	Input flag
3, 4	Not used—zeros
5–7	Cycle-steal address key
8–15	Control parameters

For a Start Data command:

Bit	**Meaning**
8	Erase-after
9	End-of-field (EOF)
10	End-of-line (EOL)
11	Erase
12	Post-cursor position
13	Pre-cursor position
14	Up/down shift
15	Shift

For a Start Image Store or a Start Control command:

Bit	**Meaning**
8–15	Not used—zeros

For a Start Field Table command:

Bit	**Meaning**
8	Not used—zero
9	End-of-field (EOF)
10	End-of-line (EOL)
11	Not used—zero
12	Post-cursor position
13	Pre-cursor position
14, 15	Not used—zeros

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Cycle-Steal Status Words

Word 0—Residual Address

Bit	Meaning
0–15	Address of last-attempted data transfer

Word 1—Cursor Address and Control

Bit	Meaning
0	E-bit
1	Ready status
2	Keyboard status
3	Display blank status
4	L-bit
5–15	Cursor address

Word 2—Error

Bit	Meaning
0–7	Not used—zeros
8–11	Hex coded error associated with CC2
12–15	Hex coded operation check associated with CC2

Interrupt Condition Codes Reported

CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents
2	Interrupt status byte (ISB)
3, 4	Keyboard interrupt or device ready

Interrupt Status Byte (ISB)

Bit	**ISB meaning**
0	Device dependent status available
1	Delayed command reject
2	Not used—zero
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

4979 Display Station

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1,2,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,5,7
7F	Start Cycle-Steal Status	0,1,2,3,5,7

Device Control Block (DCB)

Word		
0	Control word	
1	Post-cursor address (bits 5–15)	
2	Pre-cursor address (bits 5–15)	
3	Shift boundaries	(bits 0–7 HI boundary) (bits 8–15 LO boundary)
4	Control parameters	Shift count
5	DCB chain address	
6	Byte count	
7	Data storage address	
	0	*15*

Control Word (DCB Word 0)

Bit	Meaning
0	Chaining flag
1	Not used—zero
2	Input flag
3, 4	Not used—zeros
5–7	Cycle-steal address key
8	Erase-after
9	End-of-field (EOF)
10	End-of-line (EOL)
11	Erase
12	Post-cursor position
13	Pre-cursor position
14	UP/DN shift
15	Shift

Word 4

Bit	Meaning
0	M-bit
1	Display protect
2	KBD lockout
3	Blank/unblank
4–10	Not used—zeros
11–15	Shift count

Cycle-Steal Status Words

Word 0

Bit	Meaning
0–15	Residual address

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Word 1

Bit	Meaning
0	Not used—zero
1	Ready status
2	Keyboard status
3	Display blank status
4	Not used—zero
5–15	Cursor address

Word 2

Bit	Meaning
0–7	Not used—zeros
8–11	DCB checks
12–15	Operational checks

Interrupt Condition Codes Reported

CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents	
2	Cycle-steal interrupt status byte (ISB)	
3	Always zero	
4	Bits 0–3	Always zero
	Bit 4	Ready status detected
	Bits 5–7	Keyboard code bits

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

4982 Sensor I/O Unit

I/O Commands

Hex	Command	I/O instruction CCs reported
00	Read ADC	0,1,2,5,7
00	Read DI	0,1,5,7
01	Read PI	0,5,7
02	Read PI With Reset	0,1,5,7
20	Read ID (AI)	0,1,2,5,7
20	Read ID (other)	0,5,7
28	Read Status (AI)	0,1,2,5,7
28	Read Status (other)	0,5,7
2E	Read Status	0,5,7
2F	Read Diagnostic Data	0,5,7
48	Convert AI	0,1,2,5,7
48	Write AO Point 0	0,5,7
48	Write DO	0,5,7
49	Write AO Point 1	0,5,7
60	Prepare	0,5,7
61	Set Diagnostic Mode	0,5,7
62	Reset Diagnostic Mode	0,5,7
68	Convert Diagnostic Zero (AI)	0,1,2,5,7
68	Arm PI	0,1,5,7
69	Arm DI External Sync	0,1,5,7
6A	Convert Diagnostic Voltage (AI)	0,1,2,5,7
6A	Set Test 0 (DI/PI)	0,1,5,7
6B	Set Test 1	0,1,5,7
6F	Device Reset	0,7

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Device Status Words

Attachment Feature

Bit	Meaning
0	Local diagnostic mode
1	External diagnostic mode
2	Output parity error
3	Input parity error
4	Parity option selected
5	Eight device address
6	Four device address
7	Sensor I/O unit attachment feature
8–15	Zero

AI Control

Bit	Meaning	
0–7	Zero	
8–15	Feature ID	
	00100000	Without multirange amplifier
	00101000	With multirange amplifier

Multiplexer

Bit	Meaning	
0–7	Zero	
8–15	Feature ID	
	00110000	Reed relay multiplexer
	00111000	Solid state multiplexer

AO Feature

Bit	Meaning	
0–7	(See below.)	
	0000XX00	Point 0 = ±5V
	0001XX00	Point 0 = ±10V
	0010XX00	Point 0 = 0 to 10V
	00XX0000	Point 1 = ±5V
	00XX0100	Point 1 = ±10V
	00XX1000	Point 1 = 0 to 10V
8–15	Feature ID	
	01000000	Analog output

DI/PI Feature

Bit	Meaning	
0–7	(See below.)	
	00XXXX00	No interrupt is pending
	00XXXX01	An interrupt has been serviced
	00XXXX10	Not presented
	00XXXX11	An interrupt is pending
	00XX01XX	Diagnostic set test 0 mode
	00XX10XX	Diagnostic set test 1 mode
	0001XXXX	External sync armed
	0010XXXX	PI armed
8–15	Feature ID	
	00001000	Isolated DI/PI
	00010000	Nonisolated DI/PI

DO Feature

Bit	Meaning	
0–7	Zero	
8–15	Feature ID	
	00011000	Digital output

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Interrupt Condition Codes Reported

CC2, CC3, CC4

Interrupt Information Byte (IIB)

AI Control

Condition code	IIB contents	
2	DPC interrupt status byte (ISB)	
	Bits 0, 1	Zero
	Bit 2	Invalid channel
	Bit 3	Invalid range
	Bit 4	Overvoltage
	Bits 5–7	Zero
3	Always zero	

DI/PI Feature

Condition code	IIB Contents
4	Same as bits 0–7 of the DI/PI device status word

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Not used
2–7	Device dependent (described in the individual sensor I/O feature command description)

4987 Programmable Communications Subsystem

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start Read/Write	0,1,3,5,6,7
72	Open	0,1,3,5,6,7
74	Close	0,1,3,5,6,7
76	Controller Storage Load	0,1,3,5,6,7
78	Load Scan Table	0,1,3,5,6,7
7A	Dump	0,1,3,5,6,7
7B	Start Timer	0,1,3,5,6,7
7C	Trace	0,1,3,5,6,7
7D	Diagnostic Test 1	0,1,3,5,6,7
7E	Diagnostic Test 2	0,1,3,5,6,7
7F	Start Cycle-Steal Status	0,1,3,5,6,7

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Device Control Block (DCB)—General Format

Word		
0	Control word	
1	Function ID	Parameter 1
2	Parameter 2	
3	DCB ID	Parameter 3
4	Residual status address	
5	Chain address	
6	Data byte count	
7	Data address	
	0	15

Device Control Block (DCB)—Extended

Word		
0	Control word	
1	Function ID	Parameter 1
2	Parameter 2	
3	DCB ID	Parameter 3
4	Residual status address	
5	Chain address	
6	Directory count	
7	Directory address	
	0	15

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Control Word (DCB Word 0)

Bit	**Meaning**	
0	Chaining flag	
1	Program controlled interrupt	
2	Input flag	
3	Extended DCB (XD)	
	0	Standard DCB
	1	Extended DCB
4	Suppress exception (SE)	
5–7	Cycle-steal address key	
8–11	XD modifier field	
	0000	Standard DCB
	1000	Extended DCB
12–15	Zeros	

Cycle-Steal Status Words

Word 0

Bit	**Meaning**
0–15	Residual address

Word 1

Bit	**Meaning**
0–15	Residual byte count

Word 2

Bit	Meaning
0	Data overrun
1	Auto poll terminated
2	VRC error
3	Interrupt break received
4	Time-out while dialing or time-out while waiting for ring
5	Receive time-out
6	Invalid control character table
7	Chaining error
8	Function string overrun
9	Monitor table error
10	Branch and link stack error
11	Controller storage load not allowed or invalid controller storage address
12	Line not open
13	Open error
14	Invalid order or invalid branch or jump address
15	Invalid function identifier

Word 3

Bit	Meaning
0	Modem interface error
1	No power
2	Data line occupied
3	Abandon call and retry
4	Controller or channel hardware error
5	Channel/device attachment error
6	4987 power-on reset
7	Controller not ready or controller storage not loaded
8	Stop bit error
9	LRC or CRC error
10	Invalid order sequence
11–15	Reserved

4987

Word 4

Bit	**Meaning**
0	Data terminal ready
1	Transmit mode
2–7	Device dependent
8	Exception end condition
9–15	Specific exception

Residual Status Block (RSB)—General Format

DCB

Word 0

Bit	**Meaning**
0–15	Residual byte count

Word 1

Bit	**Meaning**
0	End of chain (EOC)
1	Retry (RT)
2–14	Not used—zeros
15	No exception (NE)

Word 2

Bit	**Meaning**
0–7	Retry count
8–15	Not used—zeros

Residual Status Block (RSB)—Extended DCB

Word 0

Bit	Meaning
0–15	Residual directory count

Word 1

Bit	Meaning
0	End of chain (EOC)
1	Retry (RT)
2–14	Not used—zeros
15	No exception (NE)

Word 2

Bit	Meaning
0–15	Residual segment count

Word 3

Bit	Meaning
0–7	Retry count
8–15	Not used—zeros

Interrupt Condition Codes Reported

CCO, CC1, CC2, CC3, CC4

Interrupt Information Byte (IIB)

Condition code	IIB contents
0, 4	Always zero
1	DCB identifier
2	Cycle-steal interrupt status byte (ISB)
3	Bits are set by function string orders

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Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

5250 Information Display System Attachment Feature

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1,2,5,7
60	Prepare	0,5,7
6F	Device Reset	0,7
70	Start	0,1,2,5,7
72	Start Control Store	0,1,2,5,7
7F	Start Cycle-Steal Status	0,1,2,5,7

Device Control Block (DCB)

Word	
0	Control word
1	Device dependent
2	Device dependent
3	Device dependent
4	Status address
5	DCB chain address
6	Byte count
7	Data address

0 *15*

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Control Word (DCB Word 0)

Bit	Meaning
0	Chaining flag
1	Not used—zero
2	Input flag
3	Not used—zero
4	Suppress exception
5–7	Cycle-steal address key
8–15	Modifier bits (device dependent; used to define operations for specific start commands)

Cycle-Steal Status Words

Word 0—Residual Address

Word 1—Residual Byte Count

Word 2—Residual Status Block Information

Bit	Meaning
0	End of chain (EOC)
1–7	Not used—zeros
8, 9	Presented as zeros
10	Short incorrect record length
11–14	Presented as zeros
15	No exception (NE)

Word 3

(Check condition byte 0)

Bit	Meaning
0	Data stream reject
1	Station byte count inconsistency
2	Resources temporarily unavailable
3–7	Not used—zeros

(Station address byte 1)

Bit	Meaning
0–3	Cable address
4	Not used—zero
5–7	Cable station address

Words 4–6

Device dependent. These words contain the ending status of the station addressed on completion of station-directed operations.

Word 7

(Operation checks byte 0)

Bit	Meaning
0	Incorrect controller storage image check sum
1	Controller storage image imcompatibility with hardware engineering change level
2–7	Not used—zeros

(DCB specification checks byte 1)

Device dependent. This byte further defines the reason for DCB specification check on an exception interrupt with DCB specification check set in the ISB.

Word 8

(Status byte 0)

Bit	Meaning
0	Initialized
1	Armed
2, 3	Not used—zeros
4–7	Not used—may be zeros or ones

(Residual address key byte 1*)

Bit	Meaning
0–4	Not used—zeros
5–7	Residual address key

*Resets to all zeros only on a power-on reset

Residual Status Block (RSB)

Bit	Meaning
0–15	Residual byte count

Word 1

Bit	Meaning
0	EOC
1–7	Not used—zeros
8, 9	Presented as zeros
10	Short incorrect record length
11–14	Presented as zeros
15	NE

Interrupt Condition Codes Reported

CC2, CC3, CC4, CC6, CC7

Interrupt Information Byte (IIB)

Condition code	IIB contents	
2, 6	Cycle-steal interrupt status byte (ISB)	
3	Bit 0	Permissive device end
	Bits 1–7	Always zeros
4	Bit 0	Always zero
	Bit 1	Hardware check (bit is set on when check occurs)
	Bits 2–7	Always zeros
7	Bit 0	Permissive device end
	Bit 1	Hardware check (bit is set on when check occurs)
	Bits 2–7	Always zeros

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Interrupt Status Byte (ISB)

Bit	**ISB meaning**
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor

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