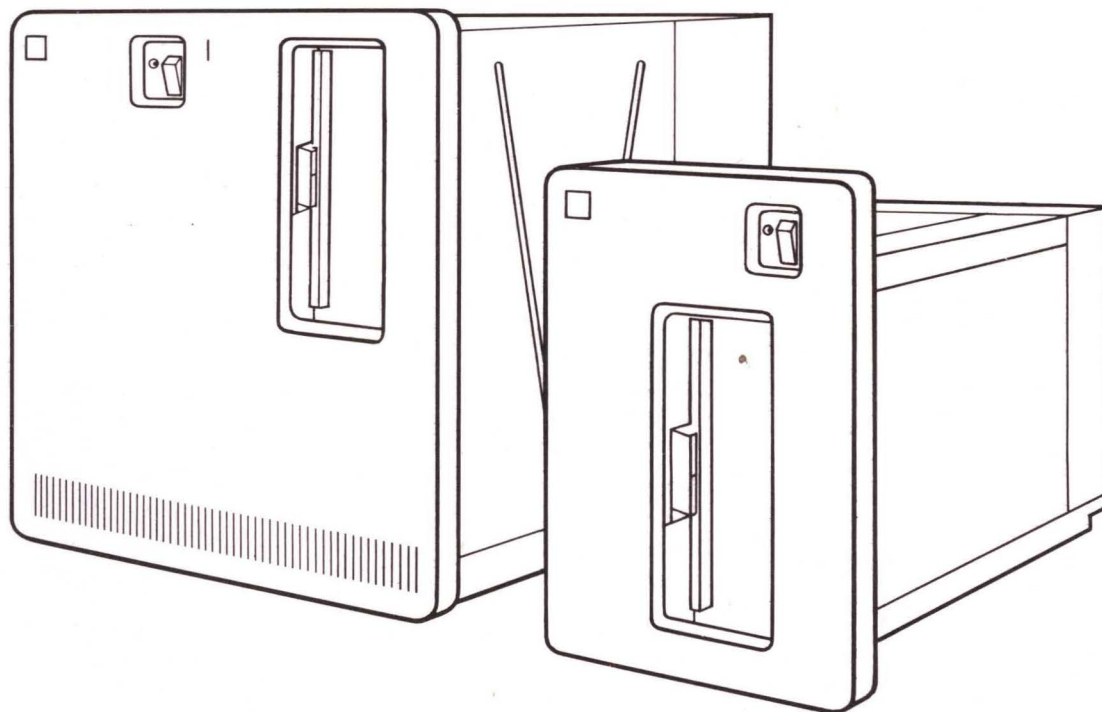


GA34-0024-1

File No. S1-07

IBM Series/1

4962 Disk Storage Unit and
4964 Diskette Unit
Description



DISK AND DISKETTE DESCRIPTION

Second Edition (March 1977)

This is a major revision of, and obsoletes not only GA34-0024-0 but also Series/1 4964 Diskette Unit Description, GA34-0023-0. Significant changes in this new edition include: the addition of Chapter 4, "Programming Diskette Operations," and restructuring of Chapters 1 and 2 to include diskette unit information previously presented in GA34-0023-0.

Changes are periodically made to the information herein; any such changes will be reported in subsequent revisions or Technical Newsletters. Before using this publication in connection with the operation of IBM systems, have your IBM representative confirm editions that are applicable and current.

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This manual is intended for those interested in the physical characteristics and operation of either the IBM Series/1 4962 Disk Storage Unit or the 4964 Diskette Unit. It assumes the reader understands data processing terminology and is familiar with binary and hexadecimal numbering systems. The manual contains the machine code information required to plan, correct, and modify programs written in the assembler language.

Chapter 1, "IBM Series/1 4962 Disk Storage Unit and 4964 Diskette Unit," describes the characteristics and capacities of disk and diskette units and the functions of Series/1 4962/4964 Attachment Features.

Chapter 2, "Disk and Diskette Data Format," describes how data is arranged on the disk and diskette surfaces.

Chapter 3, "Programming Disk Operations," describes the instructions and control blocks required to execute input/output operations on the disk unit. This chapter also contains disk unit status and interrupt information.

Chapter 4, "Programming Diskette Operations," describes the instructions and control blocks required to execute input/output operations on the diskette unit. This chapter also contains diskette unit status and interrupt information.

Prerequisite Publications

IBM Series/1 Model 5 4955 Processor and Processor Features Description, GA34-0021

IBM Series/1 Model 3 4953 Processor and Processor Features Description, GA34-0022

IBM Series/1 System Summary, GA34-0035

Related Publications

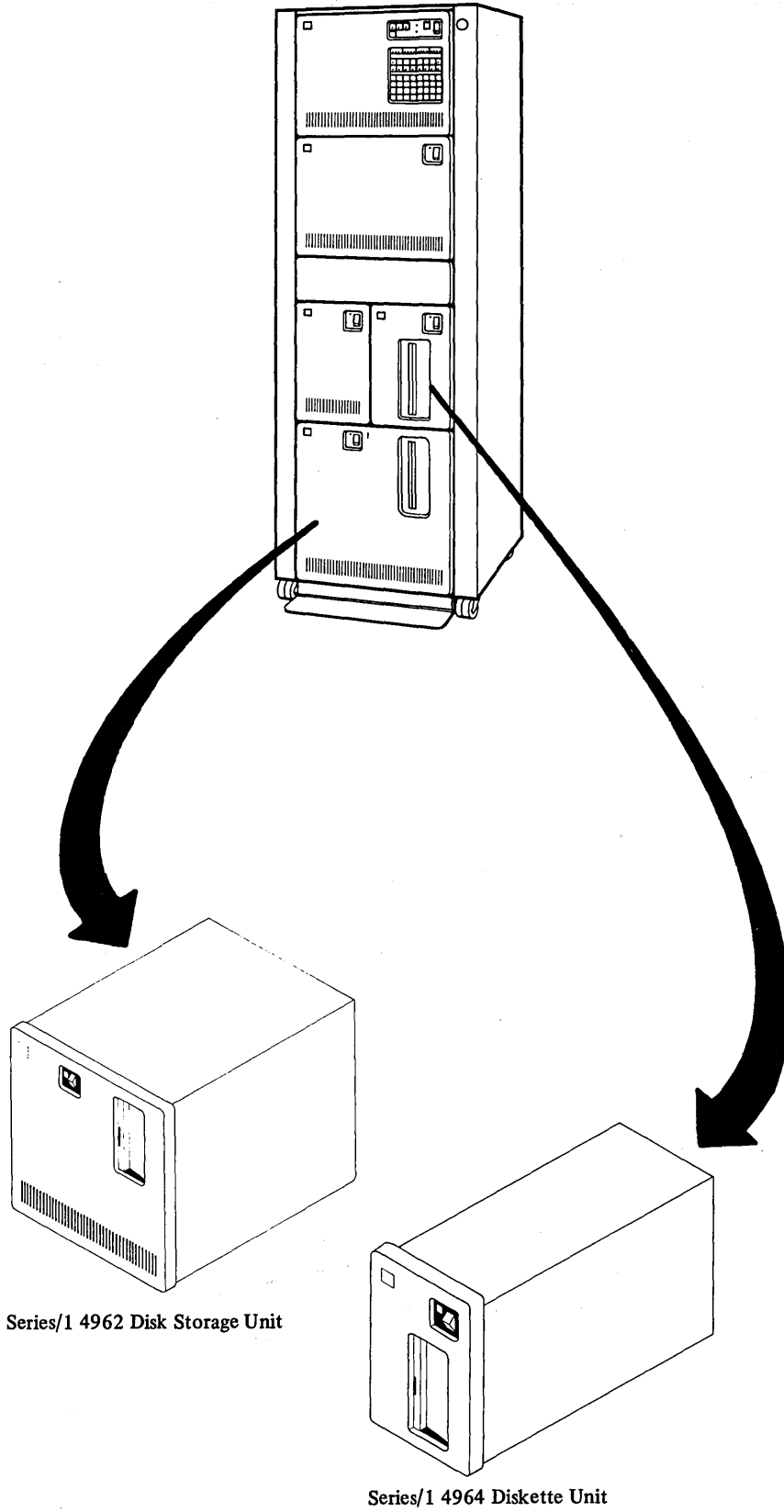
IBM Series/1 Installation Manual—Physical Planning, GA34-0029

IBM Series/1 Configurator, GA34-0042

IBM Diskette General Information Manual, GA21-9182

IBM Series/1 Operator's Guide, GA34-0039

IBM Series/1 Unit Configuration



Series/1 4962 Disk Storage Unit

Series/1 4964 Diskette Unit

Chapter 1. IBM Series/1 4962 Disk Storage Unit and 4964 Diskette Unit

Introduction

The IBM Series/1 4962 Disk Storage Unit and 4964 Diskette Unit are direct access storage devices designed for use with IBM Series/1 processors.

IBM 4962 Disk Storage Unit

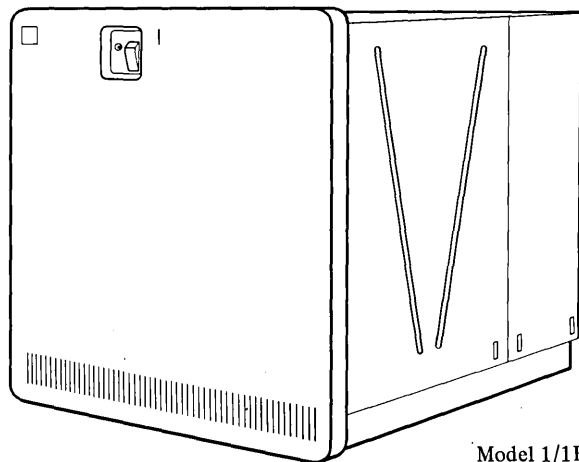
The 4962 Disk Storage Unit consists of a fixed disk and access mechanism, the disk drive electronics that retrieve and record data on the disk, and the cables that connect the disk storage unit to an IBM Series/1 processor attachment.

The disk and access mechanism are sealed in an enclosure that:

- eliminates operator handling
- reduces exposure to external contaminants
- eliminates preventive maintenance

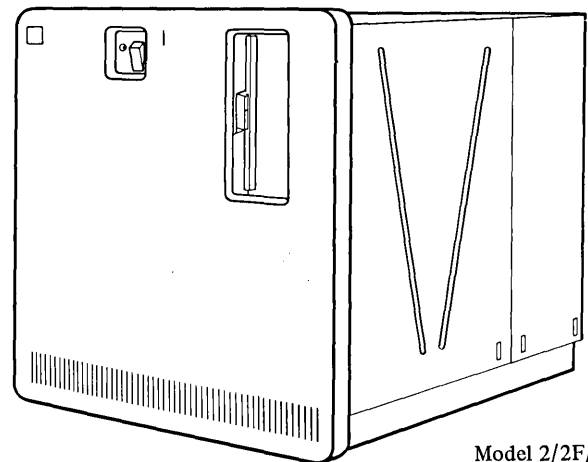
Models

Six models of the 4962 Disk Storage Unit are available. All models have Initial Program Load (IPL) capability and can be mounted in either an Electronic Industries Association rack (RS-310B) or an IBM 4997 Model 1 or Model 2 Rack Enclosure.



Model 1/1F/3

IBM 4962 Disk Storage Unit



Model 2/2F/4

Model 1 contains a fixed disk with a maximum formatted storage capacity of 9,308,160 bytes. The disk is accessed by two movable heads.

Model 1F contains a fixed disk that is accessed by two movable heads and eight fixed heads. Maximum formatted storage capacity is 9,308,160 bytes for the movable heads and 122,880 bytes for the fixed heads.

Model 2 is a combination disk and diskette unit that contains:

- A fixed disk with a maximum formatted storage capacity of 9,308,160 bytes. The disk is accessed by two movable heads.
- A removable diskette with a maximum formatted storage capacity of 606,208 bytes (512-byte sectors). The diskette is accessed by two movable heads.

Model 2F is a combination disk and diskette unit that contains:

- A fixed disk that is accessed by two movable heads and eight fixed heads. Maximum formatted storage capacity is 9,308,160 bytes for the movable heads and 122,880 bytes for the fixed heads.
- A removable diskette with a maximum formatted storage capacity of 606,208 bytes (512-byte sectors). The diskette is accessed by two movable heads.

Model 3 contains a fixed disk with a maximum formatted storage capacity of 13,962,240 bytes. The disk is accessed by three movable heads.

Model 4 is a combination disk and diskette unit that contains:

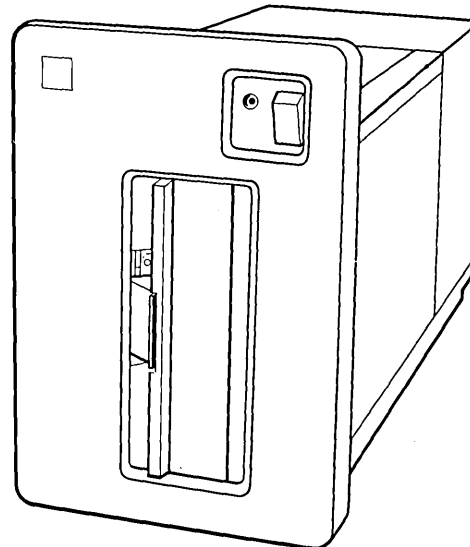
- A fixed disk with a maximum formatted storage capacity of 13,962,240 bytes. The disk is accessed by three movable heads.
- A removable diskette with a maximum formatted storage capacity of 606,208 bytes (512-byte sectors). The diskette is accessed by two movable heads.

Disk units in all models of the 4962 are functionally identical and can be designated as either the primary or alternate system IPL device. The diskette unit in the 4962 Model 2, 2F, and 4 is functionally identical to the 4964 Diskette Unit. Each disk and diskette unit, alone or combined, attaches to individual Series/1 attachments that allow totally independent and fully overlapped operation.

IBM 4964 Diskette Unit

The 4964 Diskette Unit retrieves and records data on removable one-sided or two-sided magnetic diskettes. The unit consists of an access mechanism, the diskette drive electronics that record and retrieve data on the diskette and a single cable for connecting the diskette unit to an IBM Series/1 processor attachment.

IBM 4964 Diskette Unit



Model 1

Models

One model of the 4964 Diskette Unit is available. The 4964 Model 1 has Initial Program Load (IPL) capability. It can be designated as either the primary or alternate system IPL device. The unit has two movable heads for reading and writing data. An IBM Diskette 2 (two-sided diskette) recorded in 512-byte sector format provides maximum storage capacity (606,208 bytes). An IBM Diskette 1 (one-sided diskette) recorded in 128-byte format provides Basic Data Exchange.

The diskette unit mounts in one-half the width of an Electronic Industries Association rack (RS-310B) or an IBM 4997 Model 1 or Model 2 Rack Enclosure.

Basic Data Exchange

An IBM 4964 Diskette Unit and Attachment Feature connected to a Series/1 processor can exchange diskette data with the following IBM devices using a one-sided diskette recorded in basic data exchange format (128-byte sector format):

- IBM 3540 Diskette Input/Output Unit
- IBM 3741 Data Station
- IBM 3742 Dual Data Station
- IBM 3747 Data Converter
- IBM 3773/3774/3775/3776 Communication Terminals
- IBM 3881 Optical Mark Reader, Model 3
- IBM 3890 Document Processor
- IBM 5231 Controller, Model 2
- IBM 5320 System Unit—System/32

Disk Specifications

The functional specifications of the disk unit are:

Rotational speed	2964 ± 3%	RPM
Time of rotation	20.2	ms
Average rotational delay or latency	10.1	ms (nominal)
Data Transfer Rate		
To or from channel*	380,000	bytes/sec
On and off disk (instantaneous)	889,000	bytes/sec
Movable Head Storage		
Sectors per track	60	
Bytes per sector	256	
Bytes per track	15,360	
Tracks per cylinder		
Models 1, 1F, 2, 2F	2	
Models 3, 4	3	
Bytes per cylinder		
Models 1, 1F, 2, 2F	30,720	
Models 3, 4	46,080	
Cylinders	303	
Total Storage Capacity		
Models 1, 1F, 2, 2F	9,308,160	bytes
Models 3, 4	13,962,240	bytes
Access Times		
Cylinder to cylinder	10	ms (maximum)
Average seek (101 cylinders)	40	ms (maximum)
Fixed Head Storage		
Number of heads	8	
Sectors per track	60	
Bytes per sector	256	
Bytes per track	15,360	
Total storage capacity	122,880	bytes

*Time average for multiple sector transfers over two rotations of the disk.

Diskette Specifications

The functional specifications of the IBM 4964 Diskette Unit and the diskette unit included with 4962 Models 2, 2F, and 4 are:

Maximum data storage capacity (formatted with 512-byte sectors)	606	kilobytes
Data transfer rate	31.2	kilobytes/sec
Data tracks/diskette surface	74	tracks
Rotational speed	360	RPM
Latency	83.8	milliseconds
Track-to-track access time*	40	milliseconds

*Derived from:

$$T (\text{number of track crossing} \times 5 \text{ ms}) + (35 \text{ ms settling time})$$

Diskette data tracks contain either 128, 256, or 512-byte sectors. Refer to "Format Track Operation" in Chapter 4.

	128 Bytes Per Sector	256 Bytes Per Sector	512 Bytes Per Sector
IBM Diskette 1	246,272 ¹	284,160	303,104
IBM Diskette 2	492,544	568,320 ²	606,208

¹The basic data exchange format for an IBM Diskette 1.

²Preinitialized format of an IBM Diskette 2.

Disk/Diskette Attachments

IBM Series/1 processor attachment features used with the 4962 and 4964 units:

- interpret and control execution of commands
- provide the path for data between the channel and the disk/diskette
- serialize and deserialize data
- furnish status information to the channel
- check the accuracy of data transferred to and from the channel
- check sector buffer parity (disk attachment only)
- perform a Cyclic Redundancy Check (CRC) of each data field and sector ID transferred to or from the disk/diskette

A 1024-byte buffer is used in every I/O operation that transfers data to or from the disk. Buffering sectors of data eliminates the possibility of overrunning the channel.

Note. Diskette data is not buffered.

Attachment feature cards for the disk and diskette units plug into feature card slots in the IBM Series/1 processor card file or the IBM Series/1 4959 Input/Output Expansion Unit.

Operator Controls

A Power On/Off switch and Power On indicator are located on the front panel of the 4962 and 4964 units.

1. Power switch. Power is applied to the disk/diskette unit when this switch is placed in the *ON* position. Nominally, 16 seconds after power is applied the disk unit is 'ready' for operations.
2. Power On indicator. This light indicates the power switch is in the *ON* position.
3. Diskette access door. This door must be closed and latched after inserting or removing a diskette.

Chapter 2. Disk/Diskette Data Format

This chapter describes how data is arranged or formatted on the disk and diskette. Cylinder, track, and sector descriptions are included for both the disk and diskette. The functions of the diskette index hole are also explained.

Disk Surface Format

On all models of the 4962, one side of the disk is divided into two data bands; the inner band is accessed by head 0, and the outer band by head 1. Each band contains a head landing zone (LZ) and 303 data tracks. A band of 303 factory written servo tracks on the other side of the disk is used for tracking and seeking.

On 4962 Models 1F, 2F, 3, and 4, a third band of data is located on the servo-track side of the disk. Models 1F and 2F have an eight-track band that is accessed by fixed heads, and Models 3 and 4 have a 303-track band that is accessed by a third movable head. See Figure 2-1.

Note. To insure data integrity, data under the fixed heads should be refreshed after each power-on. The IBM Series/1 Realtime Programming System relieves the user of this responsibility.

Servo Tracks

Factory written servo tracks assure precise head positioning. Combinations of timing and position pulses define the beginning of each track and sector.

Data Tracks

Data tracks accessed by the movable read/write heads are numbered 000 to 302. Each track is divided into sixty, 256-byte, fixed length sectors. Individual track capacity is 15,360 data bytes.

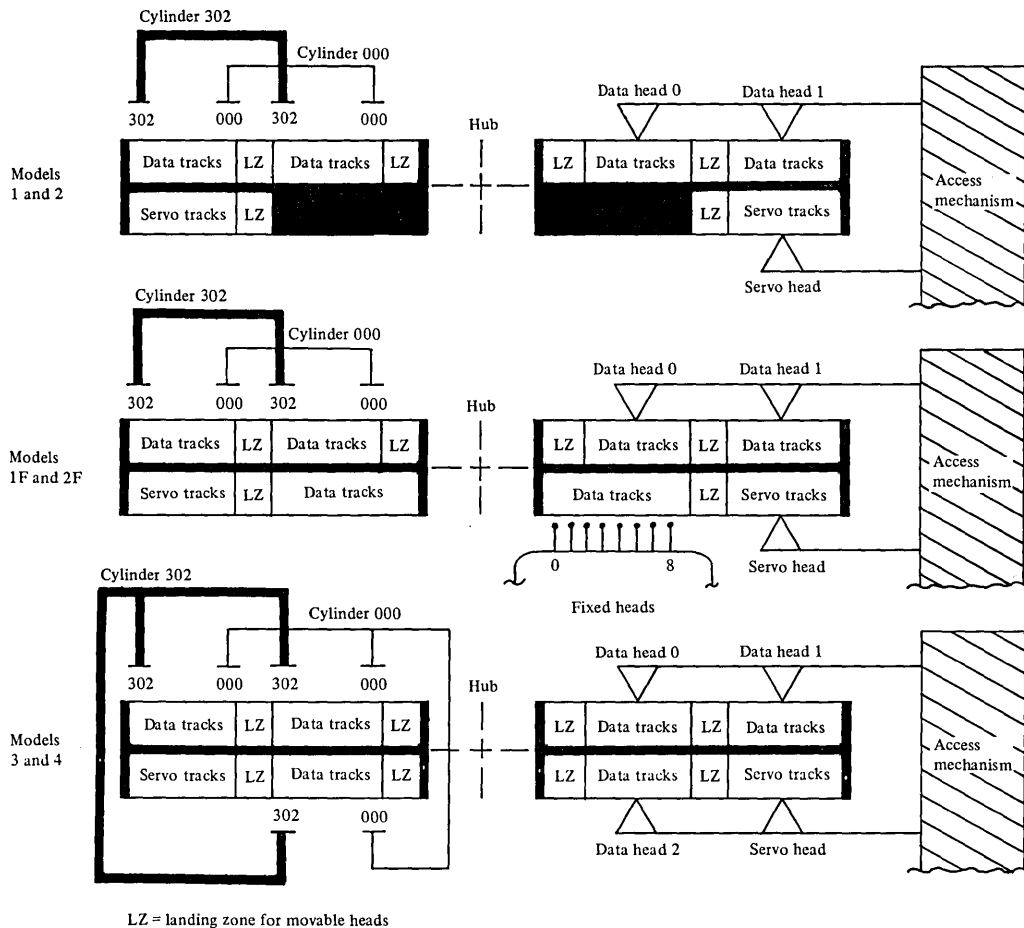


Figure 2-1. IBM 4962 disk surface format

Cylinders

A cylinder consists of two tracks, one in each data band accessed by the movable heads. See Figure 2-1. Cylinder 000 is located toward the center of the disk, and cylinder 302 is located toward the outer edge of the disk. Two of the 303 cylinders are reserved; cylinder 001 is reserved for alternate sectors, and cylinder 302 is reserved for maintenance use.

Sectors

The sector is the addressable unit on the disk surface. Each sector consists of an identification field (sector ID) and a 256-byte data field. Before accessing the data field, the sector ID is read to verify that the correct sector has been found. Sectors on the disk are numbered 00, 30, 01, 31 . . . 28, 58, 29, 59 to allow recovery time between writing a data field and reading the next sector ID. See Figure 2-2. For programming purposes the sectors can be considered consecutively numbered. For example, moving from sector 06 to sector 07 is a shift of one sector.

Records are stored in the data portions of sectors. If a record is less than 256 bytes, the remainder of the sector is padded with binary zeros before the data field CRC is written. If a record is longer than 256 bytes, it is written over as many sectors as its length requires. Records must not exceed track capacity (60 sectors).

Sector ID Field Format

The sector ID field is seven bytes in length. Each sector on the disk has a unique ID field. The ID field has the following format:

1	2	3	4	5	6	7
Flag	Cylinder addr	Head addr	Sector addr	CRC bytes		

where:

flag	indicates the disk surface condition for the sector
cylinder address	indicates the cylinder on which the sector is located
head address	indicates the head used to access the sector
sector address	indicates the number of the sector on the track
CRC	indicates the cyclic redundancy check bytes calculated and written for the sector ID field. CRC bytes are also written for the data field after the data area. The CRC bytes are recalculated each time information is read from the disk and compared with the CRC bytes written previously. An unequal comparison sets error indicators.

Further information on specifying the fields in the sector ID can be found under "Using the DCB" in Chapter 3.

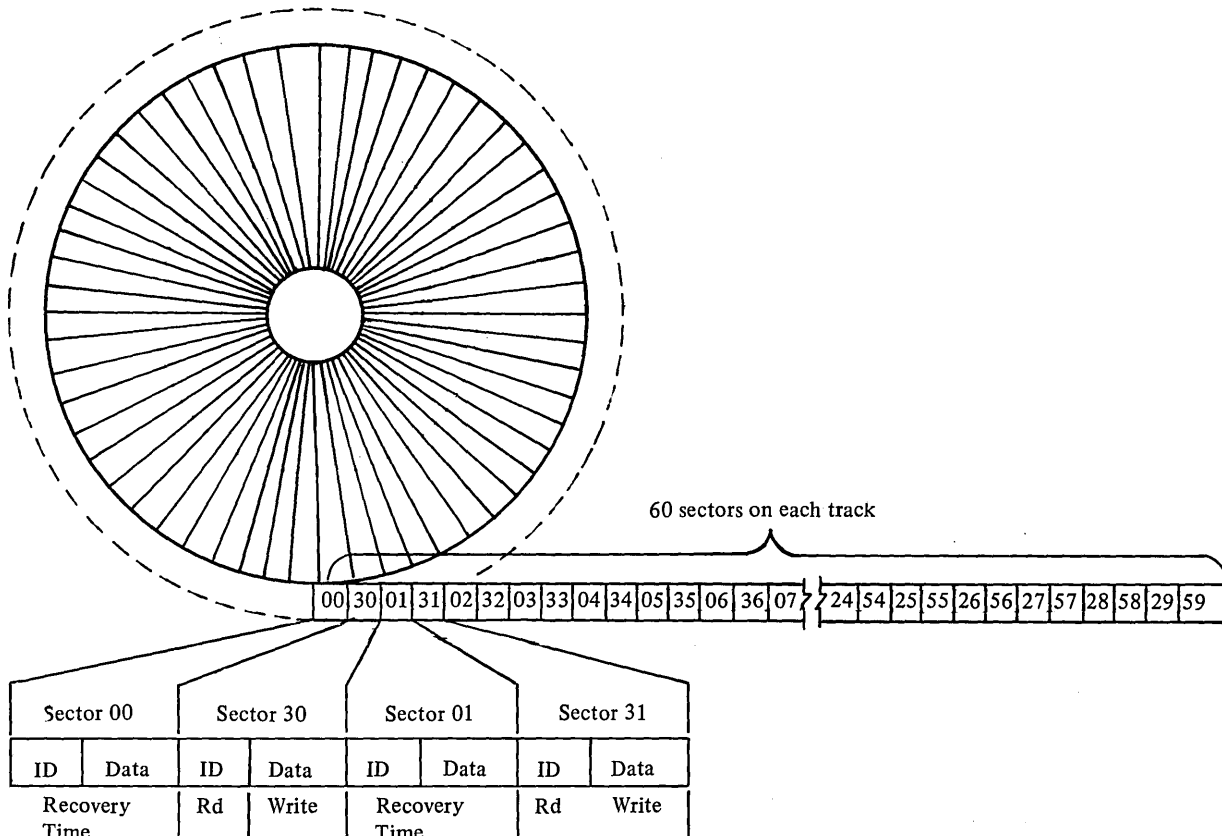


Figure 2-2. Sector numbering

Diskette

The diskette storage medium is a magnetically coated disk that is permanently enclosed in a jacket. Small slots in the jacket allow the read/write heads to contact the surfaces as the disk rotates within the jacket. The disk and jacket, together, are referred to as a *diskette*. See Figure 2-3.

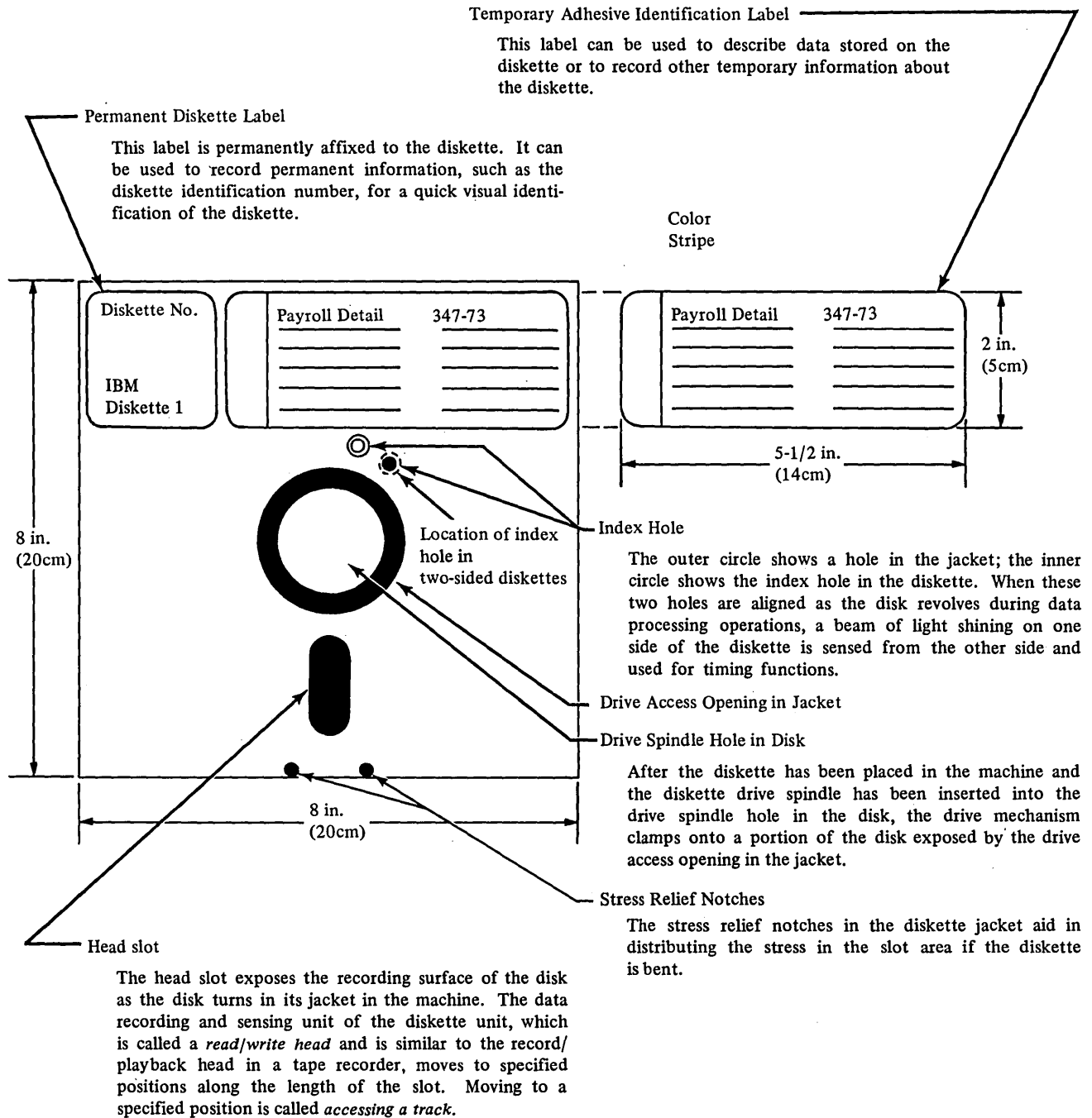


Figure 2-3. Diskette storage medium

Diskette Surface Format

Depending on the type of diskette (IBM Diskette 1 or Diskette 2), one or both sides are formatted with tracks divided into sectors. The Diskette 1 contains 74 data tracks on the head 0 side of the diskette. The head 1 side of the Diskette 1 is blank and cannot be used. The Diskette 2 contains 74 data tracks on both sides of the diskette. The number of sectors on each track—26, 15, or 8—depends on the sector length—128, 256, or 512 bytes respectively.

Cylinders

On a Diskette 1, the terms *cylinder* and *track* are synonymous. On a Diskette 2, a cylinder consists of the pair of tracks (one on each side) that can be read or written without moving the heads.

Index

When the index hole in the diskette passes a light source, an index timing pulse is generated. The index timing pulse signals the beginning of a track and occurs each time the diskette rotates. The index timing pulse is used to begin Format Track operations and to determine whether a Diskette 1 or Diskette 2 is installed in the diskette unit. See Figure 2-4.

An attempt to access the head 1 side of a Diskette 1 ends the operation and sets the DCB specification check in the interrupt status byte to 1. Refer to "Interrupt Status Byte" in Chapter 4.

Tracks

Diskette surfaces are divided into 77 tracks with each track divided into fixed-length sectors. A sector is a physical location on the diskette; sector format is described in the following section. A sector can hold all or part of a record. If the record is shorter than the sector length, unused bytes are padded with binary zeros. If a record is longer than the sector length, the record is written over as many sectors as its length requires.

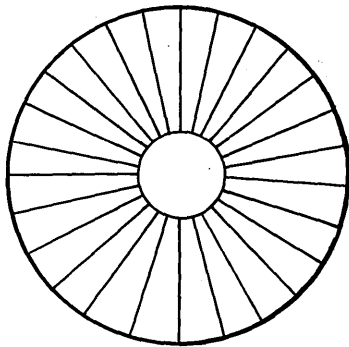
The data storage capacity of a track depends on track format. Tracks can be formatted with one of three fixed-length sector sizes:

Sector Size Capacity	Sectors per Track	Track Storage Capacity
128 bytes	26	3328 bytes
256 bytes	15	3840 bytes
512 bytes	8	4096 bytes

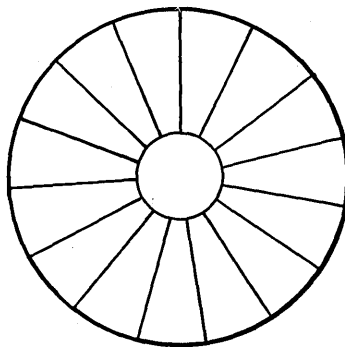
The ability to choose a sector size is especially useful if records length requirements change from job to job and thus from diskette to diskette. The sector size that provides the most efficient use of diskette space can be chosen depending on the record length required.

Tracks must be numbered from 00 (outermost) to 76 (innermost). The tracks should be used in the following ways:

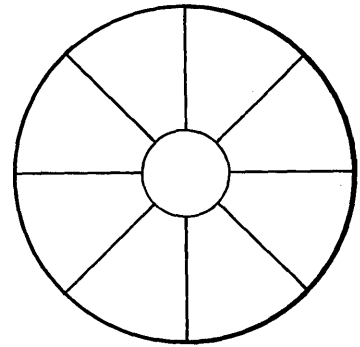
- Reserve track 00 for system use as a label track.
- Reserve track 01 through 74 for data; until used for data they contain unallocated free space.
- Reserve tracks 75 and 76 for use as alternates.



26 Sectors



15 Sectors



8 Sectors

Sectors

Each sector consists of a sector identifier (sector ID) and a data field. The sector ID holds the unique address for the sector. Refer to the following section, "Sector ID Format."

Sector numbers are assigned beginning with 01 for the first sector after index. There are 26 sectors if the sector length for the diskette is 128 bytes, 15 sectors if the length is 256 bytes, and 8 sectors if the length is 512 bytes.

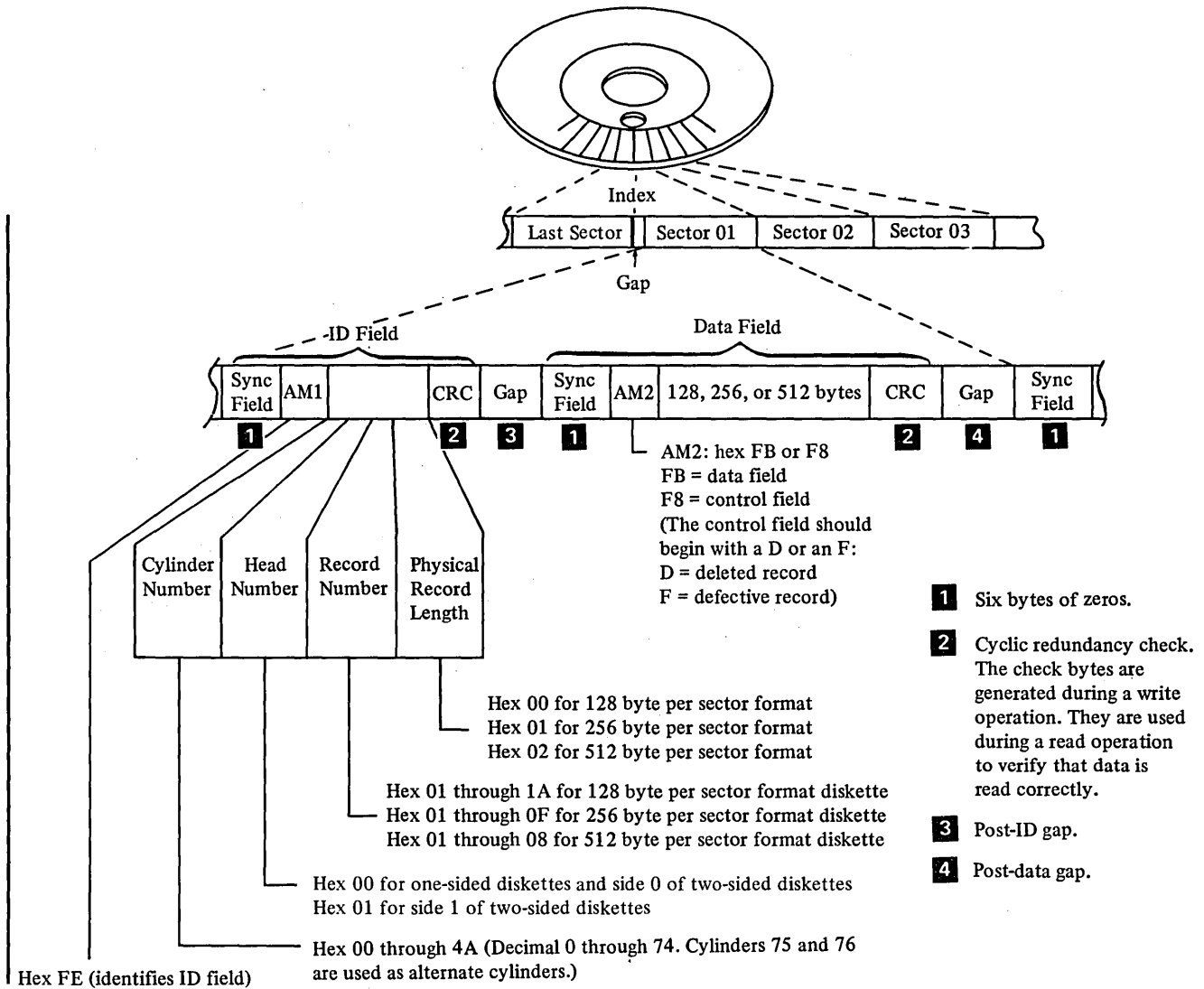


Figure 2-4. Diskette track format

Sector ID Format

The sector ID consists of seven bytes, and each sector on the diskette has a unique ID. The sector ID has the following format:

ID

AM1 Byte	C Byte	H Byte	R Byte	N Byte	CRC Byte	CRC Byte
-------------	-----------	-----------	-----------	-----------	-------------	-------------

AM1. This Address Marker (AM) signals the start of each sector. The AM1 byte is always X'FE'.

C-Byte. The C-byte contains a binary number that designates the cylinder in which the sector is located (cylinders 00 through 76). The C-byte corresponds to the cylinder address byte in the Device Control Block (DCB). Refer to "Using the DCB" in Chapter 4.

H-Byte. The H-byte identifies the head used to access the sector. Because the diskette unit contains two heads, 0 and 1, this byte must contain a value of either X'00' or X'01'. Otherwise, the response to all data transfer operations except Read Sector ID is 'no record found'. The H-byte corresponds to the head selection byte in the Device Control Block (DCB). Refer to "Using the DCB" in Chapter 4.

R-Byte. The R-byte identifies the sector number. The sector number must be specified with a binary number that represents 01 through 26 for 128-byte sectors, 01 through 15 for 256-byte sectors, or 01 through 08 for 512-byte sectors. The R-byte in the sector ID corresponds to the sector number byte in the Device Control Block (DCB). Refer to "Using the DCB" in Chapter 4 and the note after "CRC Bytes" in this chapter.

N-Byte. The N-byte designates the byte length of each sector on the track. The N-byte must contain hexadecimal:

- 00 for tracks formatted with 128-byte sectors
- 01 for tracks formatted with 256-byte sectors
- 02 for tracks formatted with 512-byte sectors

Using any other N-byte designation causes a DCB specification check for all data transfer operations except Read Sector ID. The N-byte corresponds to the sector length byte in the Device Control Block (DCB). Refer to "Using the DCB" in Chapter 4 and the note after "CRC Bytes" in this chapter.

CRC Bytes. A two-byte Cyclic Redundancy Check (CRC) field is calculated as each sector ID is written. The CRC bytes are written immediately after the sector ID bytes. They are also calculated and written after the data field in each sector. The CRC bytes are recalculated each time information is read from the diskette and compared with previously written CRC bytes. An unequal comparison sets error indications.

The cyclic redundancy check provides the following error detection capability:

- 100% of odd bit errors
- 100% of single burst failures of 16 bits or less
- 99.9985% of random errors

Note. During all data transfer operations except Read Sector ID, the C-byte, H-byte, R-byte, and N-byte of the sector ID are specified as a search argument in the DCB. The required sector is located by comparing sector IDs on the diskette with the search argument in the DCB. When an equal comparison occurs, the data transfer begins.

Chapter 3. Programming Disk Operations

This chapter describes the I/O commands required to perform input/output operations on the IBM 4962 Disk Storage Unit. The commands that can be issued, the instruction and control blocks required for each command, and the individual disk operations are described. Status information and I/O interrupts are also described in this chapter.

Data Transfer Operations

Data is transferred on the I/O channel in a parallel operation (16 data bits plus 2 parity bits). On a write operation, parity bits are removed and the data bits are transferred serially to the disk. On a read operation, the data bits are read serially from the disk, parity bits are added, and the information is transferred one word at a time into processor storage. The direction in which data moves on the channel is determined by the I/O command. The command also determines whether data is transferred to or from processor storage under direct program control only, or under direct program control and in cycle steal mode.

Direct Program Control (DPC)

An I/O command executed under direct program control transfers a word of data or control information into or from processor storage. After moving the immediate data, the processor continues with other instructions.

Cycle Steal (CS) Mode

When data is transferred in cycle steal mode, processing and I/O operations are overlapped. Overlapping allows the processor to execute other instructions while the disk unit is cycle stealing the data required to complete an I/O operation. Data is moved to or from processor storage by stealing cycles from the processor.

Initiating a Disk Operation

Every I/O operation to the disk unit requires (in processor storage):

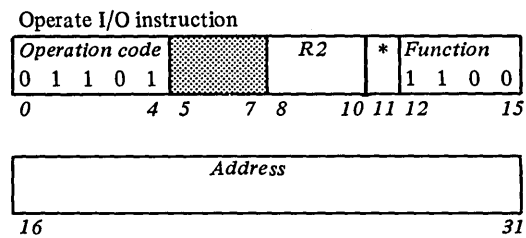
1. an Operate I/O instruction
2. an I/O command, device address, and an immediate data field.

Operate I/O Instruction

The Operate I/O instruction points to an Immediate Device Control Block (IDCB) in storage containing an I/O command, device address, and immediate data field. Refer to the following section for more detail. Every Operate I/O instruction must have an associated IDCB.

Note. The Operate I/O instruction is described more completely in IBM Series/1 processor unit description manuals. Refer to the Preface of this manual for titles and order numbers.

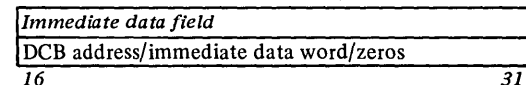
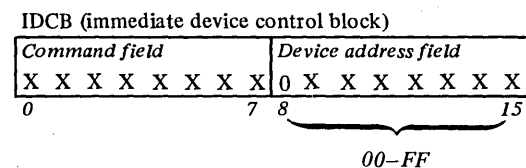
The format of the Operate I/O instruction is:



Using the IDCB

An Immediate Device Control Block (IDCB) must be reserved in processor storage for every I/O command issued to the disk unit. Before issuing an Operate I/O instruction to the disk unit, an I/O command must be stored in the command field of the associated IDCB. The immediate data field of the IDCB must contain a data word, a DCB address or zeros. I/O commands that execute only under direct program control require a data word or zeros, while commands that also transfer data in cycle steal mode require a DCB address. Refer to the following section.

The format of the IDCB is:



I/O Commands and Disk Operations

The I/O command, stored in the IDCB, determines whether a single word of immediate data is transferred under direct program control only or, following the DPC operation, additional words of data are to be transferred into or from processor storage in cycle steal mode. See Figure 3-1.

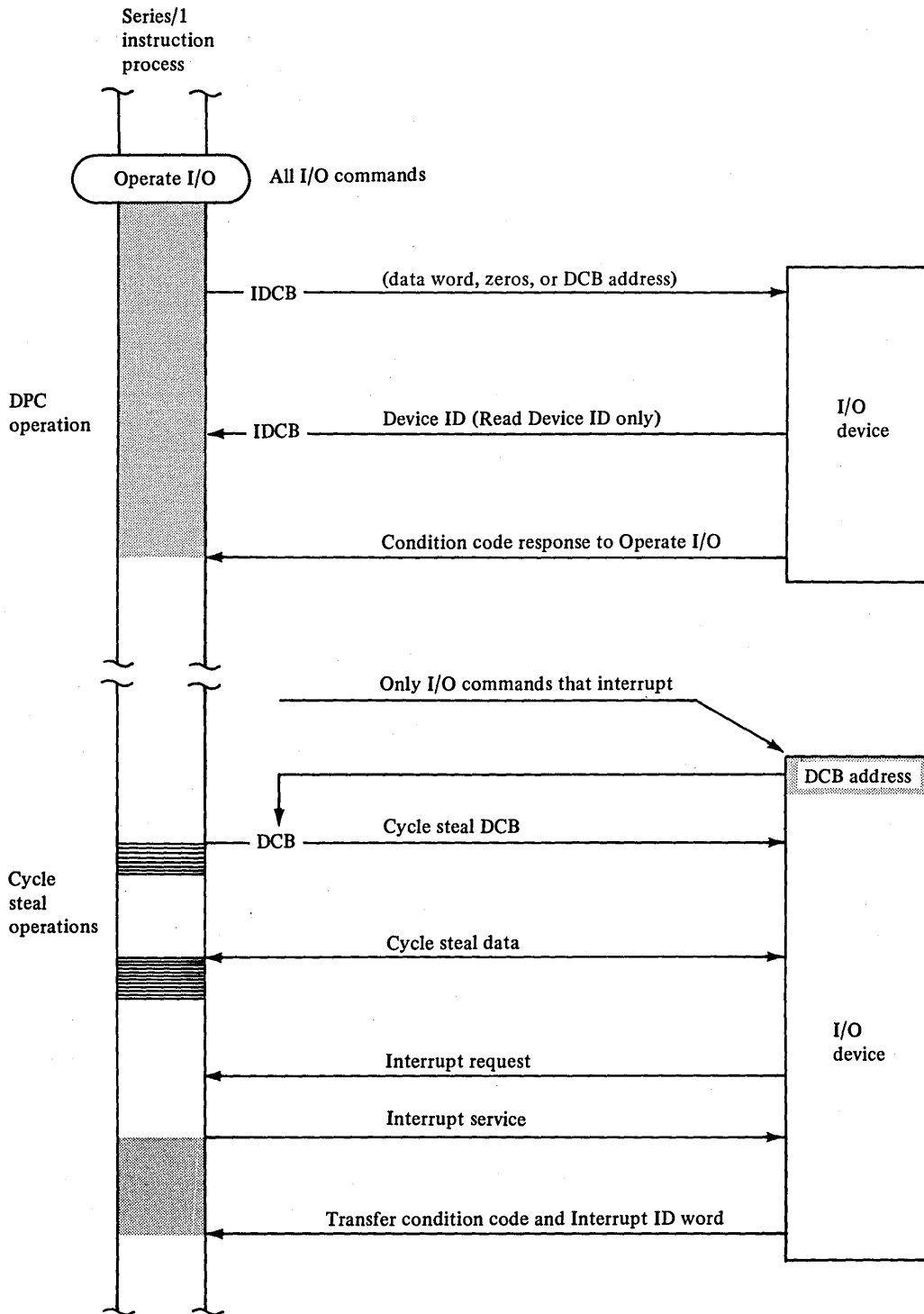


Figure 3-1. Overview of an I/O operation

Command Execution Under Direct Program Control

Prepare, Device Reset, and Read Device ID commands transfer a single word of data to or from the immediate data field of an IDCB in storage. Command execution is complete when a condition code is reported to the processor following the DPC operation. Refer to "Condition Codes" later in this chapter. Processing of other instructions resumes when the I/O operation ends. See Figure 3-2.

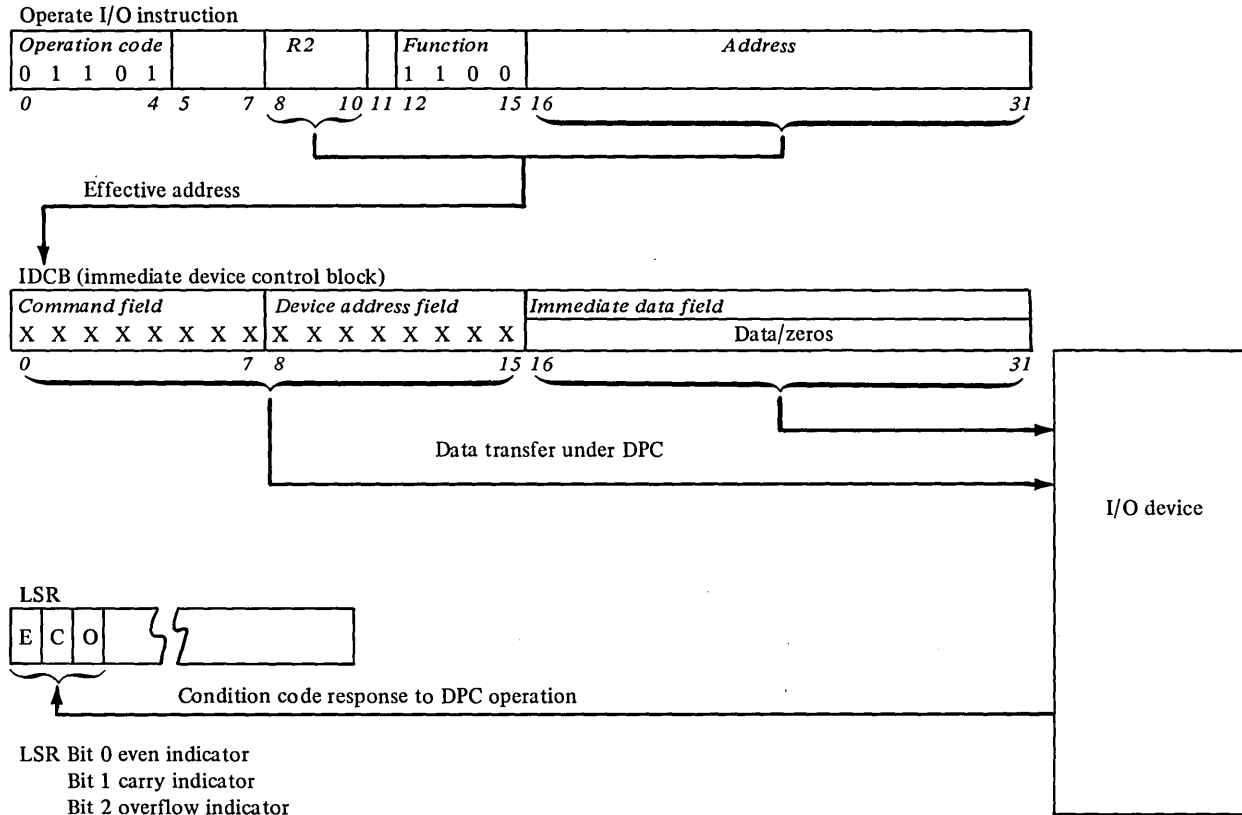
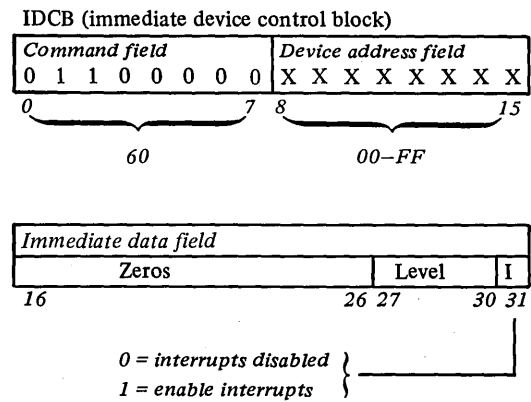


Figure 3-2. I/O operation initiated and executed exclusively under direct program control

Prepare Command

Before using any of the interrupt-causing commands, a Prepare command must be issued to the disk unit. The Prepare command transfers a word containing interrupt parameters from the IDCB immediate data field associated with the command to the *Prepare Register* in the disk attachment. The interrupt parameters in this word establish whether the disk unit is allowed to interrupt, and if so, the level on which processing operations can be interrupted. The Prepare command is executed under direct program control and does not cause an interrupt.



Note. Refer to "Prerequisite Publications" in the Preface of this manual. Processor description manuals contain information about interrupt levels.

Device Reset Command

The Device Reset command resets all pending interrupts and previously established control and status conditions. The device ID, device address, data address, residual address, and prepare registers are not reset by this command. The command code and device address in the IDCB supply the information required to execute the Device Reset command. Although the IDCB immediate data field is not used and not checked, set the bits to zero. The Device Reset command is executed under direct program control and does not cause an interrupt.

The format of the IDCB for a Device Reset command is:

IDCB (immediate device control block)

Command field	Device address field
0 1 1 0 1 1 1 1	X X X X X X X X
0 7	8 15
6F	00-FF

Immediate data field
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
16 31

Read Device ID Command

The Read Device ID command loads the disk unit device ID word into the immediate data field of the IDCB associated with the command. Read Device ID executes under direct program control: the device ID is transferred immediately into storage, and a condition code is reported to the processor. Refer to "Status Information" later in this chapter. The Read Device ID command does not cause an interrupt.

The format of the IDCB for the Read Device ID command is:

IDCB (immediate device control block)

Command field	Device address field
0 0 1 0 0 0 0 0	X X X X X X X X
0 7	8 15
20	00-FF

Immediate data field
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
16 31

During command execution, the device ID is transferred under DPC to this field. After execution of the Read Device ID command, the immediate data field in the IDCB associated with the command contains:

Immediate data field
Model dependent
16 31

- 00AA = without fixed heads (Models 1 and 2)
- 00BA = with fixed heads (Models 1F and 2F)
- 00CA = with three movable heads (Models 3 and 4)

Command Execution in CS Mode

Start and Start Cycle Steal Status commands transfer data in cycle steal mode. The DCB address associated with either command, however, is transferred under DPC from the IDCB immediate data field in processor storage to the disk unit. See Figure 3-2. When the disk unit accepts the command and DCB address, a condition code is reported to the processor. The processor continues with other operations and the disk unit begins cycle stealing the data required to complete the I/O operation. When the transfer of data in cycle steal mode ends, an interrupt request is sent to the processor. At interrupt presentation time a condition code and interrupt ID word are transferred to the processor. The I/O operation ends and the processor continues with other operations.

The immediate data field of an IDCB containing either a Start or Start Cycle Steal Status command must point to a Device Control Block (DCB). See Figure 3-3. The DCB must contain the control information and device parameters required to execute an I/O operation in cycle steal mode. Refer to the following section.

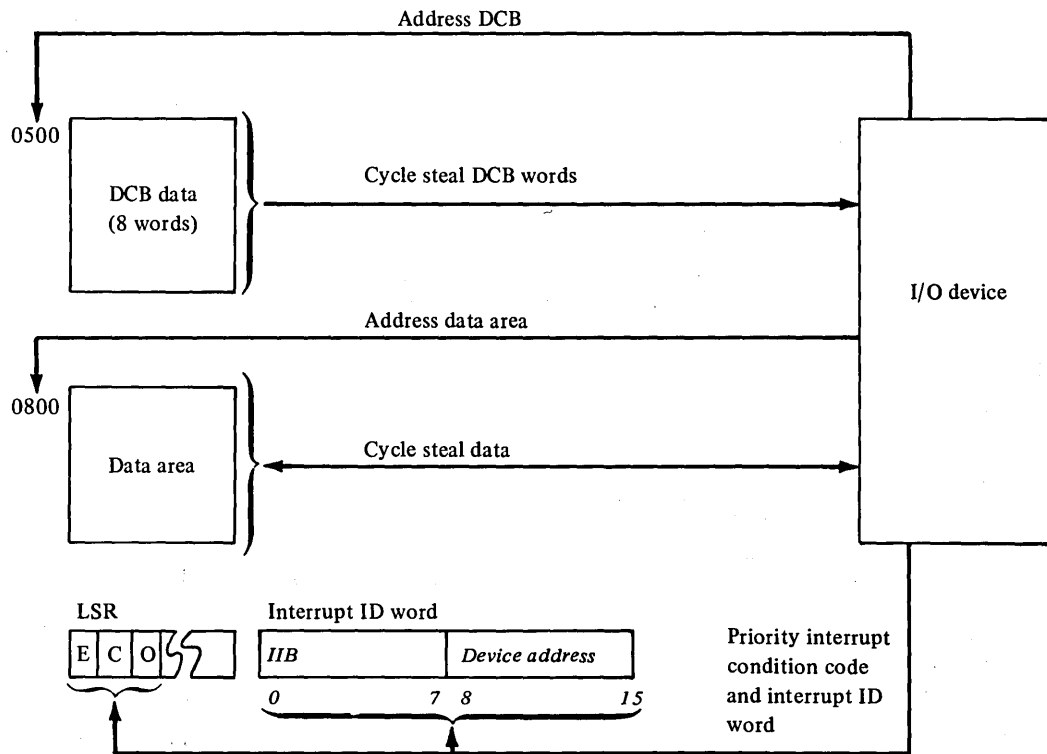
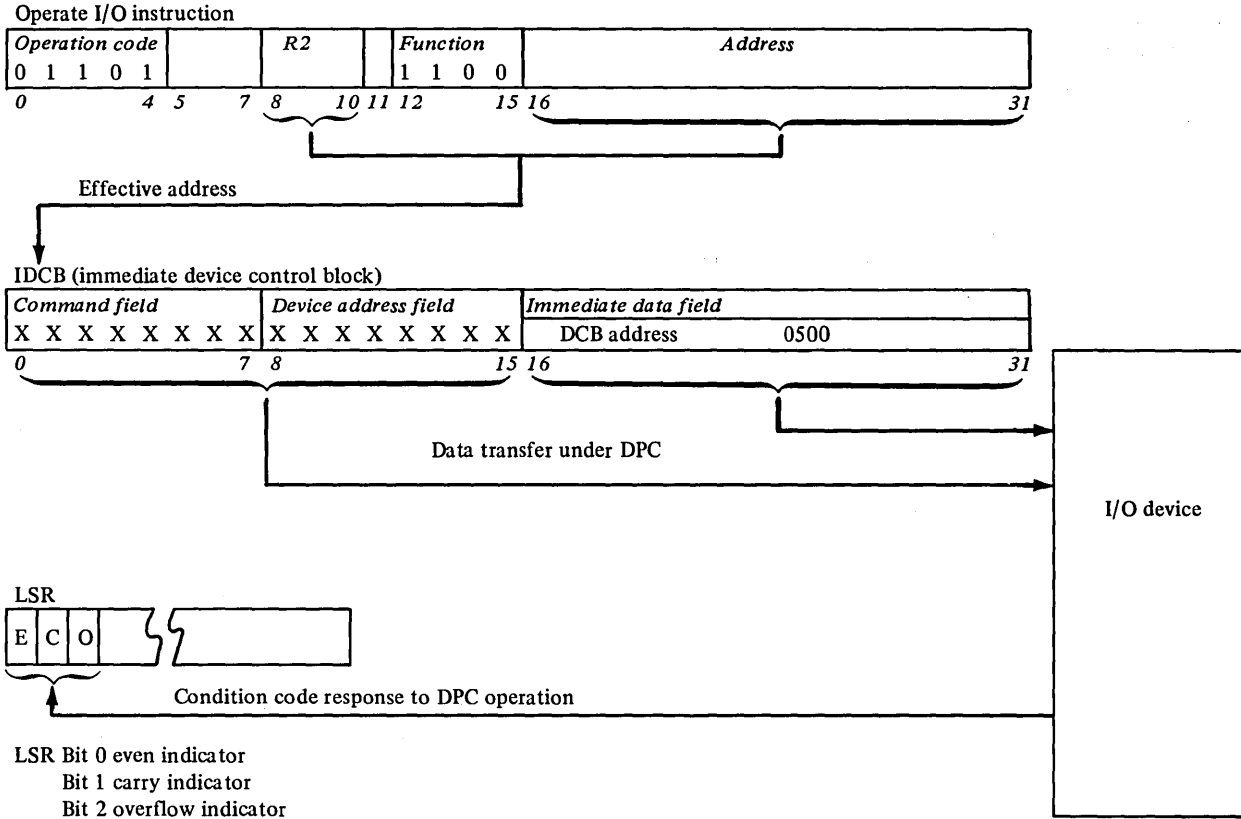


Figure 3-3. I/O operation initiated under direct program control and executed in cycle steal mode

Using the DCB

A Device Control Block (DCB), comprised of eight contiguous words in processor storage, must be reserved for every I/O operation that moves data in cycle steal mode. See Figure 3-4. A separate DCB is required for:

- a Start command
- a Start Cycle Steal Status command
- all disk operations included in a DCB command chaining sequence (refer to "DCB Command Chaining" later in this chapter.)

Device parameters that define and control the I/O operation must be stored in each DCB.

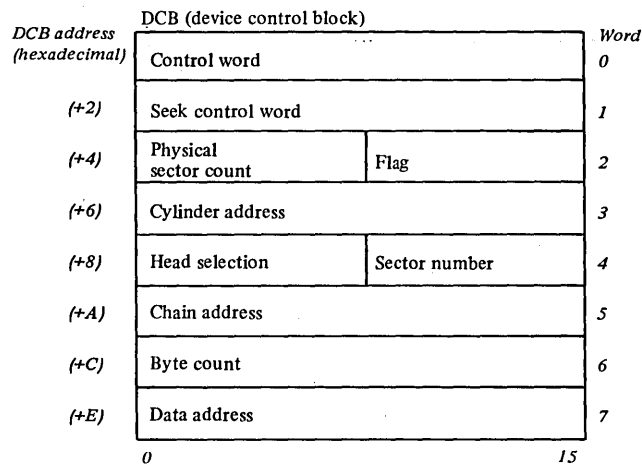


Figure 3-4. DCB format (Start command shown)

General information about each word and field in the DCB is supplied in the sections that follow; specific information appears in the description for each operation later in this chapter.

DCB Control Word (DCB Word 0)

Figure 3-5 shows the format of the DCB control word. This word occupies the first position of each DCB associated with a Start or Start Cycle Steal Status command. The DCB control word delineates the disk operation.

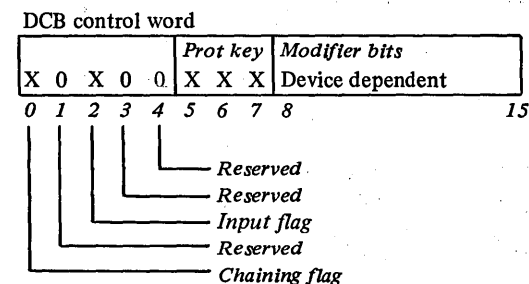


Figure 3-5. DCB control word format

The meaning of the bits is as follows:

- Bit 0 (chaining flag)**: Set this bit to 1 to specify DCB command chaining. When the operation called for by the current DCB ends, the chain address stored in DCB word 5 points to the next DCB in the chained sequence. Refer to "DCB Command Chaining" later in this chapter.
- Bit 1 (reserved)**: Set this bit to 0 to avoid future code obsolescence.
- Bit 2 (input flag)**: Set the input flag bit to 1 for disk operations that transfer data into processor storage. Set the bit to 0 for disk operations that transfer data from storage and for Seek/Seek Recalibrate operations.

Note. If the input flag bit setting is not consistent with the type of operation: the operation ends and an interrupt request is sent to the processor. At interrupt presentation time, an exception condition and a DCB specification check are presented to the processor.

- Bit 3 (reserved)**: Set this bit to 0 to avoid future code obsolescence.
- Bit 4 (reserved)**: Set this bit to 0 to avoid future code obsolescence.
- Bits 5-7 (address key)**: These bits represent the cycle steal address key required for storage authorization at cycle steal request time.
- Bits 8-15**: The bits in this field are device dependent modifiers of the Start command. A bit configuration must be selected that represents the disk operation to be performed. The selected disk operation must be compatible with the setting of the input flag bit (bit 2). The hexadecimal designation for each disk operation and the corresponding setting of bit 2 are shown in Figure 3-6.

Note. Burst mode (bit 15) is not supported by the 4962 and 4964.

Bit 2	DCB control word modifier bits 8-15	Hexadecimal equivalent	Operation
0	00000001	01	Write Data
0	00000010	02	Write Sector ID
0	00000011	03	Write Sector ID Skewed
1	00001001	09	Read Data
1	00001100	0C	Read Verify
1	00001010	0A	Read Sector ID
1	00001011	0B	Read Sector ID Skewed
1	00001000	08	Read Diagnostic
0	00000101	05	Seek
0	00000111	07	Seek Recalibrate

Figure 3-6. DCB control word modifier bit configurations

Seek Control Word (DCB Word 1)

The seek control word is used, in conjunction with the head address specified in the high-order byte of DCB word 4, to control Seek operations. The seek control word specifies the direction of the seek—either toward the outer perimeter of the disk or toward its center—and the number of cylinders to be crossed. Figure 3-7 shows the format of the seek control word.

Notes.

1. Use the seek control word only for Seek operations.
2. If the seek control word is set to zero, no seek movement occurs.
3. Because they are not required for a Seek operation, set DCB word 3, DCB word 6, and the sector number in DCB word 4 to zero. The search argument and byte count are not used in Seek operations.

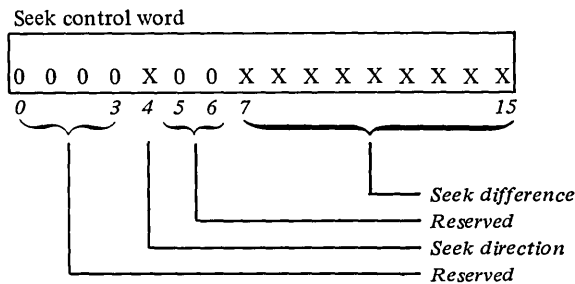


Figure 3-7. Seek control word format

The meaning of the seek direction and seek difference fields are as follows:

- Bit 4 (seek direction) To increase the cylinder number (seek toward the outer edge of the disk), set this bit to 0. To seek to a lower cylinder number (toward the center of the disk), set this bit to 1.
- Bits 7–15 (seek difference) These nine bits specify the seek difference (the number of cylinders to be moved). If a seek difference of zero is specified, no movement occurs and a device end condition code is transferred to the processor at interrupt presentation time.

Bits 0–3 and 5–6 in the seek control word are reserved and must be set to zeros to avoid future code obsolescence.

Physical Sector Count and Flag (DCB Word 2)

DCB word 2 is comprised of two one-byte fields: the physical sector count and the flag byte of the search argument.

Physical Sector Count

This byte is required only for the sector-counting disk operations: Write Sector ID, Write Sector ID Skewed, Read Sector ID, Read Sector ID Skewed, and Read Diagnostic. These disk operations are used to locate a specific sector on the disk without reading sector ID bytes. Factory written sector bytes are recorded at the beginning of every sector location on the disk. The sector counting operations locate a specific sector on a track, by counting these sector bytes. A physical sector byte count that is one less than the desired physical sector location must be stored in the DCB associated with each sector-counting disk operation. For example:

Desired physical sector location	Physical byte count
00	59
01	00
02	01
03	02

Flag

A search argument comprised of the flag byte, the cylinder address in DCB word 3, and the head and sector addresses in DCB word 4 is used to locate the first sector in a Read Data, Write Data, or Read Verify operation. Sector IDs are read from the disk track, and compared to the search argument. When an equal comparison occurs, the transfer of data begins. The flag byte is the first byte of the sector ID; bits 6 and 7 specify the disk surface condition for the sector. Bits 0–5 are reserved and must be set to zero to avoid future code obsolescence. Bits 6 and 7 have the following meanings:

Bits 6–7	Disk surface condition indicator
00	good primary sector
10	defective primary sector
01	good alternate sector
11	defective alternate sector (cylinder 001)

Cylinder Address (DCB Word 3)

The cylinder address of the required sector must be specified in DCB word 3. The cylinder address is the second and third bytes in the sector ID. A right adjusted binary number from 000 to 302 must be specified to identify the cylinder containing the data to be accessed. The cylinder address is part of the search argument used to locate the first sector involved in a Read Data, Write Data, or Read Verify operation.

Notes.

1. Bits 0–6 of the cylinder address must always be set to zeros.
2. A cylinder address of 152 should be specified in the DCB search argument for Write Sector ID and Write Sector ID Skewed operations on the fixed R/W heads.

Head Selection and Sector Number (DCB Word 4)

DCB word 4 consists of two one-byte fields: head selection and sector number.

Head Selection

Head selection can only be accomplished with the Seek operation. To change head selection without changing cylinders, perform a Seek operation with the desired head designation in the head selection byte and a seek difference of zero in the seek control word (DCB word 1). The possible bit configurations (and their hexadecimal equivalents) for the head selection byte are:

	Head selection byte bit configurations	Hexadecimal equivalents
Select movable head:	0 0000 0000	00
	1 0000 0001	01
	2 0000 0010	02
Select fixed head:	0 1000 0000	80
	1 1000 0001	81
	2 1000 0010	82
	3 1000 0011	83
	4 1000 0100	84
	5 1000 0101	85
	6 1000 0110	86
7 1000 0111	87	

Head Selection and Sector Number (DCB Word 4)

DCB word 4 consists of two one-byte fields: head selection and sector number.

Head Selection

Head selection can only be accomplished with the Seek operation. To change head selection without changing cylinders, perform a Seek operation with the desired head designation in the head selection byte and a seek difference of zero in the seek control word (DCB word 1). The possible bit configurations (and their hexadecimal equivalents) for the head selection byte are:

		Head selection byte bit configurations	Hexadecimal equivalents
Select movable head:	0	0000 0000	00
	1	0000 0001	01
	2	0000 0010	02
Select fixed head:	0	1000 0000	80
	1	1000 0001	81
	2	1000 0010	82
	3	1000 0011	83
	4	1000 0100	84
	5	1000 0101	85
	6	1000 0110	86
7	1000 0111	87	

Sector Number

The low-order byte of DCB word 4 specifies the sector number. A right-adjusted binary number from 00 to 59 must be used to specify the sector to be accessed.

Chain Address (DCB Word 5)

To chain disk operations, set the chaining flag bit in the DCB control word (DCB word 0) to 1. The address of the next DCB in the chain must be specified in the chain address (DCB word 5). The address must be an even number. If the chained-to address is an odd number (bit 15 is on), no data is transferred, and a DCB specification check is set in the interrupt status byte and transferred to the processor at interrupt presentation time.

Byte Count (DCB Word 6)

The byte count specifies the number of bytes to be transferred between processor storage and the disk unit. The byte count must be an even number and cannot be zero. If bit 15 is set on (indicating an odd byte count) or the count is zero: the operation ends, no data transfer takes place, and a DCB specification check is presented to the processor.

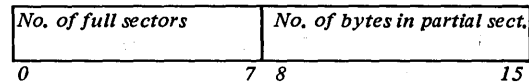
Several I/O operations to the disk unit require a specific hexadecimal value in the byte count:

1. The byte count for a Start Cycle Steal Status command must contain X'0008'.

2. For disk operations initiated with a Start command, the following hexadecimal values must be stored in the byte count:

Disk operation	Byte count (in hex)
Read Sector ID	0006
Read Sector ID Skewed	0006
Write Sector ID	0006
Write Sector ID Skewed	0006
Read Diagnostic	0100

3. For Read Data, Write Data, and Read Verify operations, the byte count depends on the program requirements. For these operations, the byte count has the following format:

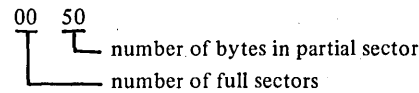


Bits 0–7 specify the number of *full* sectors to be transferred. For example: if a record is exactly 512 bytes long (two sectors), store X'02' in bits 0–7 of the byte count.

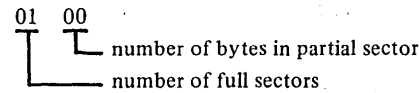
Bits 8–15 are used if the record is less than a full sector, or if the last sector in a multi-sector transfer contains less than 256 bytes of data. Use a hexadecimal value to specify the number of bytes in a partially filled sector.

Example:

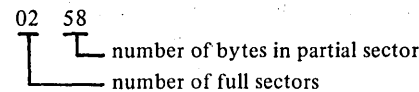
To transfer an 80-byte record, specify (in hexadecimal)



To transfer a 256-byte record, specify (in hexadecimal)



To transfer a 600-byte record, specify (in hexadecimal)



Note. On write operations involving a sector that is only partially filled with data, the disk unit writes the data called for in the DCB and then pads the balance of the sector with binary zeros. When the record is subsequently read, the padded zeros are included in the data field CRC verification. Only the number of data bytes specified in the DCB byte count, however, are transferred into storage.

Data Address (DCB Word 7)

This DCB word contains the beginning address of the processor storage location used in the data transfer. During a read operation, the first word read from the disk is stored into this location; data is transferred into succeeding storage locations until the byte count has been fulfilled. During a write operation, the word stored at this location is written to the first word in the sector specified; words are written in succeeding locations on the disk until the byte count has been fulfilled.

The data address stored in this word must identify a storage location on an even address boundary. If the data address is odd (bit 15 is set to one), the operation ends and an interrupt request is sent to the processor. At interrupt presentation time, a DCB specification check is transferred to the processor. Refer to "I/O Interrupts" later in this chapter.

DCB Command Chaining

Obtaining a new DCB upon completion of the operation specified in the current DCB without issuing a new Operate I/O instruction is called DCB command chaining. The DCBs belonging to such a sequence are said to be chained.

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Sector Number

The low-order byte of DCB word 4 specifies the sector number. A right-adjusted binary number from 00 to 59 must be used to specify the sector to be accessed.

Chain Address (DCB Word 5)

To chain disk operations, set the chaining flag bit in the DCB control word (DCB word 0) to 1. The address of the next DCB in the chain must be specified in the chain address (DCB word 5). The address must be an even number. If the chained-to address is an odd number (bit 15 is on), no data is transferred, and a DCB specification check is set in the interrupt status byte and transferred to the processor at interrupt presentation time.

Byte Count (DCB Word 6)

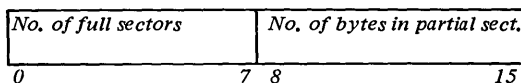
The byte count specifies the number of bytes to be transferred between processor storage and the disk unit. The byte count must be an even number and cannot be zero. If bit 15 is set on (indicating an odd byte count) or the count is zero: the operation ends, no data transfer takes place, and a DCB specification check is presented to the processor.

Several I/O operations to the disk unit require a specific hexadecimal value in the byte count:

1. The byte count for a Start Cycle Steal Status command must contain X'0008'.
2. For disk operations initiated with a Start command, the following hexadecimal values must be stored in the byte count:

Disk operation	Byte count (in hex)
Read Sector ID	0006
Read Sector ID Skewed	0006
Write Sector ID	0006
Write Sector ID Skewed	0006
Read Diagnostic	0100

3. For Read Data, Write Data, and Read Verify operations, the byte count depends on the program requirements. For these operations, the byte count has the following format:

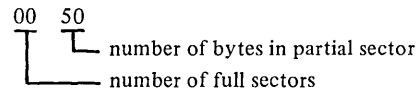


Bits 0–7 specify the number of *full* sectors to be transferred. For example: if a record is exactly 512 bytes long (two sectors), store X'02' in bits 0–7 of the byte count.

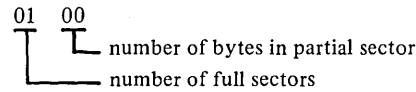
Bits 8–15 are used if the record is less than a full sector, or if the last sector in a multi-sector transfer contains less than 256 bytes of data. Use a hexadecimal value to specify the number of bytes in a partially filled sector.

Example:

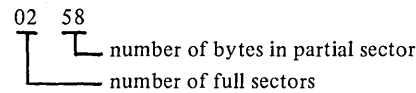
To transfer an 80-byte record, specify (in hexadecimal)



To transfer a 256-byte record, specify (in hexadecimal)



To transfer a 600-byte record, specify (in hexadecimal)



Note. On write operations involving a sector that is only partially filled with data, the disk unit writes the data called for in the DCB and then pads the balance of the sector with binary zeros. When the record is subsequently read, the padded zeros are included in the data field CRC verification. Only the number of data bytes specified in the DCB byte count, however, are transferred into storage.

Data Address (DCB Word 7)

This DCB word contains the beginning address of the processor storage location used in the data transfer. During a read operation, the first word read from the disk is stored into this location; data is transferred into succeeding storage locations until the byte count has been fulfilled. During a write operation, the word stored at this location is written to the first word in the sector specified; words are written in succeeding locations on the disk until the byte count has been fulfilled.

The data address stored in this word must identify a storage location on an even address boundary. If the data address is odd (bit 15 is set to one), the operation ends and an interrupt request is sent to the processor. At interrupt presentation time, a DCB specification check is transferred to the processor. Refer to "I/O Interrupts" later in this chapter.

DCB Command Chaining

Obtaining a new DCB upon completion of the operation specified in the current DCB without issuing a new Operate I/O instruction is called DCB command chaining. The DCBs belonging to such a sequence are said to be chained.

When DCBs are chained, the first DCB in the chain contains the address of the next DCB. As each operation in a chained sequence is completed, the chain address stored in the current DCB is used to cycle steal the next DCB in the chain. The chained-to DCB is examined to determine which operation is next in the sequence and whether the associated device parameters are valid. DCB command chaining operations continue until a DCB is fetched that has the chaining bit in the control word (DCB word 0) set to 0, indicating the last operation in the chain. If an error occurs, chaining to succeeding DCBs is automatically suspended, and an interrupt request is sent to the processor. Normally, an interrupt is not requested until the disk unit has completed the last operation in the chain.

DCB command chaining reduces the processing time required to execute I/O operations to the disk unit. For example: a single Operate I/O instruction can:

- Seek to a new cylinder location and change head selection
- write a record
- verify that the record was written properly
- seek to a new cylinder location and change head selection
- read a record, etc.

Start Command

Start commands initiate I/O disk operations that transfer data into or from processor storage in cycle steal mode. An interrupt request is sent to the processor when the I/O operation ends. An Operate I/O instruction must point to an IDCB containing each Start command, and the IDCB immediate-field must contain the address of a DCB. The control information and parameters required for a particular disk operation must be stored in the DCB associated with that operation. Refer to "Using the DCB" earlier in this chapter. The disk operations initiated with a Start command are:

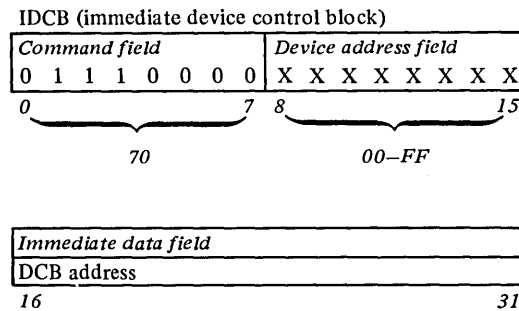
- Seek
- Seek Recalibrate
- Read Data
- Write Data
- Read Verify
- Write Sector ID
- Read Sector ID
- Write Sector ID skewed
- Read Sector ID skewed
- Read Diagnostic

Note. Refer to the description of each individual disk operation in this chapter for the format of each DCB control word and the programming considerations applicable to each operation.

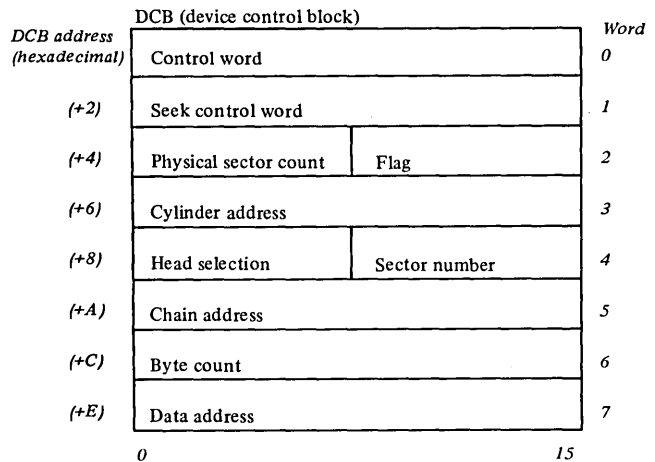
When the Operate I/O instruction is issued, the Start command is transferred under direct program control from the IDCB to the attachment where it is checked for errors and validity. If the command is accepted, a 'satisfactory'

condition code (CC=7) is sent to the processor. While the disk unit is 'busy' executing the I/O operations, the processor continues with other operations. Beginning at the DCB address specified in the IDCB, the eight words in the DCB are transferred to the disk unit from processor storage. The data is transferred in cycle steal mode one word at a time. The DCB information is decoded and the disk unit begins executing the operation called for in DCB control word (DCB word 0). When the operation (or operations when chaining) ends, an interrupt request is sent to the processor. At interrupt presentation time, a condition code and an interrupt ID word containing status information are presented to the processor.

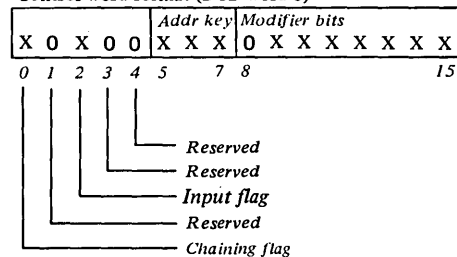
The format of the IDCB for a Start command is:



The format of the DCB for a Start command is:



Control word format (DCB word 0)



Programming Considerations

1. Every disk operation initiated with a Start command that requires a change in either head selection or cylinder location must be preceded by a Seek operation.
2. When DCB command chaining is used to perform a series of disk operations, an interrupt is not requested until either an error occurs or the last operation in the chained sequence is complete.
3. To specify DCB chaining:
 - a. For every operation in a DCB command-chained-sequence, except the last, set the chaining flag in each DCB control word (DCB word 0) to 1.
 - b. Set the address of the chained-to DCB in the chain address (DCB word 5).
4. For every I/O operation initiated with a Start command that is not included in a DCB command-chained-sequence, store (in processor storage):
 - a. an Operate I/O instruction that points to an IDCB
 - b. a Start command with a device address and a DCB address in an IDCB
 - c. a DCB that contains device parameters and control information defining a particular disk operation
5. The disk unit responds 'busy' to all commands except Prepare, Device Reset, Read ID, or Halt I/O from the time the Start command is received until an interrupt request is serviced by the processor.
6. A cylinder address of 152 should be specified when a fixed head is accessed by a Write Sector ID or Write Sector ID Skewed operation. The movable heads *must* be positioned over cylinder 152 for every Write Sector ID or Write Sector ID Skewed operation performed on the fixed heads. The position of the movable heads is of no importance for all other fixed head operations.

Seek Operation

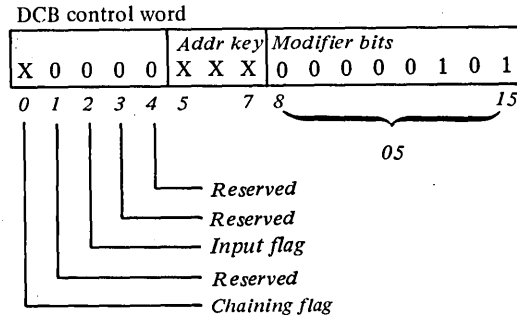
A seek must precede every I/O operation to the disk unit requiring a move of the heads to another cylinder or a change in head selection. The Seek operation can be used to change: head selection, only; cylinder location, only; or both head selection and cylinder location. The DCB associated with a Seek operation is transferred to or from processor storage in cycle steal mode. An interrupt request is sent to the processor when the disk unit completes the operation. A condition code and interrupt ID word are transferred to the processor when the interrupt is serviced. Refer to "I/O Interrupts" and "Condition Codes" later in this chapter.

The control information and parameters required for a Seek operation must be stored in a DCB. The DCB must contain:

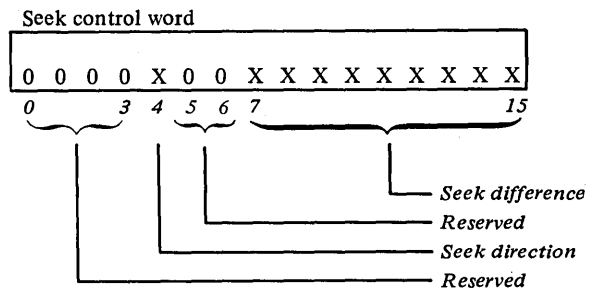
- a DCB control word defining a Seek operation to the disk unit (DCB word 0).
- a seek control word specifying the seek direction and number of cylinders to be crossed (DCB word 1).

- a head select byte that specifies which head is to be used (high-order byte of DCB word 4).
- a chain address if DCB command chaining is specified in the DCB control word.
- zeros in unused DCB fields.

The format of the DCB control word for a Seek operation is:



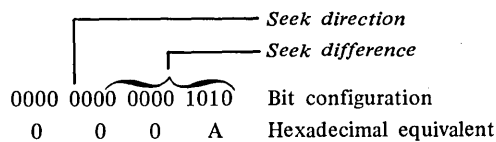
The format of the seek control word (DCB word 1) is:



Set the seek direction bit (bit 4) to 0 to increase the cylinder number; set the bit to 1 to decrease the cylinder number. Set the nine bits in the seek difference field to specify the number of cylinders the movable heads must cross to reach the desired cylinder. Set all other bits to zero.

Example:

To start from cylinder 10 and seek to cylinder 20, the seek control word would be:



Programming Considerations

1. To change head selection without moving the heads, specify a seek control word of zero and indicate the desired head in the head selection field (the high-order byte of DCB word 4).
2. If a Seek operation does not execute successfully within approximately two seconds, the operation ends immediately and an interrupt request is sent to the processor. At interrupt presentation time, an exception condition (CC=2) and an interrupt ID word containing status information are presented to the processor. If the seek difference specified to reach cylinder 000 is greater than required, a seek recalibrate automatically occurs (no error is indicated).

Seek Recalibrate Operation

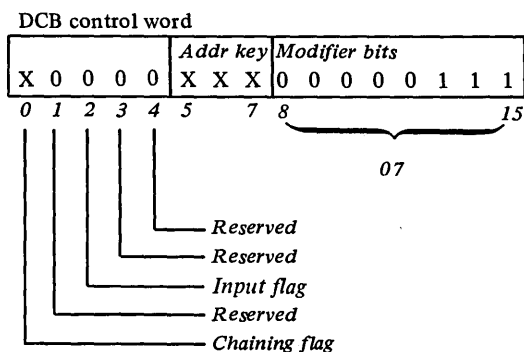
The Seek Recalibrate operation automatically moves the access mechanism to cylinder 000 and selects head 0. This operation can be used during initialization to return the heads to cylinder 000 from an indeterminate location. The DCB data associated with a Seek Recalibrate operation, is transferred to or from processor storage in cycle steal mode and when the disk unit completes the operation an interrupt request is sent to the processor. When the processor services the interrupt request, a condition code and an interrupt ID word are transferred to the processor. Refer to "Interrupts" and "Condition Codes" later in this chapter.

The control information and parameters required for a Seek Recalibrate operation must be stored in a DCB. The DCB must contain:

- a DCB control word that defines a Seek Recalibrate operation to the disk unit (DCB word 0).
- a chain address in DCB word 5 if DCB command chaining is specified in the DCB control word for this operation. Refer to "DCB Command Chaining" earlier in this chapter.

Although the data in the DCB seek control word (DCB word 1) is not needed for this operation, it is checked for proper parity. Set unused DCB words and fields to zero.

The format of the DCB control word for a Seek Recalibrate operation is:



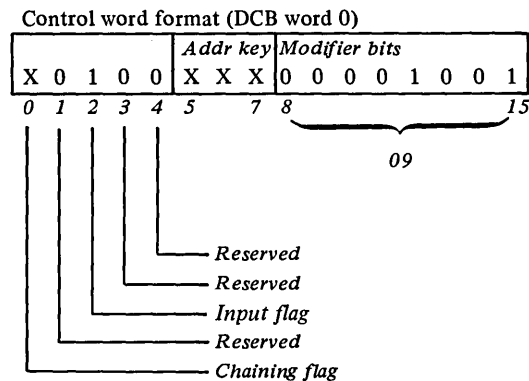
Read Data Operation

The Read Data operation retrieves a data record stored in one or more sectors on the disk and transfers the data into contiguous processor storage locations, beginning at the data address specified in the DCB. The Read Data operation transfers data in cycle steal mode and an interrupt request is sent to the processor when the operation ends.

When the disk unit performs the Read Data operation, the head selected with a previous Seek operation immediately begins to read the disk for the sector ID specified by the search argument in the DCB. When the disk unit locates the sector, the information in the data field is transferred from the disk to the attachment buffer. The data field is verified by recalculating the CRC bytes for the data field and comparing the result with the previously written data field CRC bytes. Although the sector being read may not be completely filled with data (padded zeros added) the disk unit must read to the end of the sector to verify the CRC bytes. Only those bytes specified by the DCB byte count, however, are transferred into storage.

The DCB for a Read Data operation must contain: a DCB control word, sector ID search argument (flag, cylinder address, head selection, sector number), byte count, and data address. Specify the chain address in DCB word 5 and set the chaining flag in DCB word 0 to 1 when command chaining to another DCB. Set unused DCB words and fields to zero.

The format of the DCB control word for a Read Data operation is:



Programming Considerations

1. To read more than one sector, set the high-order byte of the byte count field (DCB word 6) to indicate the number of full sectors to be read. If the last sector is only partially filled with data, set the low-order byte of the byte count field to indicate the number of data bytes in the last sector. If all sectors are filled, set the high-order byte to the number of sectors and the low-order byte to zero. To read less than one full sector, set the high-order byte to zero. Set the low-order byte to indicate the number of data bytes to be read.

- If a sector buffer is available for data but the sector ID field specified cannot be located after at least one full rotation of the disk, the no record found bit (bit 2) in cycle steal status word 1 is set to 1.

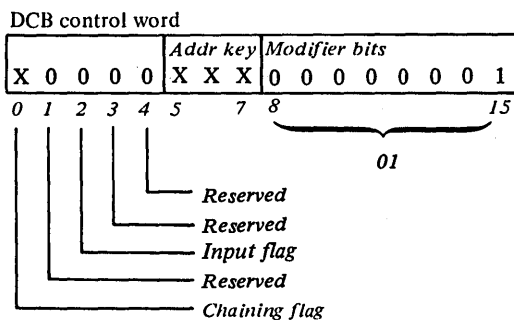
Write Data Operation

The Write Data operation transfers a data record from contiguous processor storage locations to one or more sectors on the disk. When the disk unit executes a Write Data operation, data from the DCB specified storage locations are transferred in cycle steal mode to the location on the disk specified by the search argument in the DCB. An interrupt request is presented to the processor when the disk unit completes the operation.

If the last sector being written is not a full sector, the disk unit writes the data bytes, then pads the sector to the end with zeros. The number of data bytes written for a partially-filled sector is determined from the value stored in the low-order byte of the DCB byte count (DCB word 6).

The DCB for a Write Data operation must contain: a DCB control word, sector ID search argument (flag, cylinder address, head selection, sector number), byte count, and data address. Specify the chain address in DCB word 5 and set the chaining flag in DCB word 0 to 1 when command chaining to another DCB. Set unused DCB words and fields to zero.

The format of the DCB control word for a Write Data operation is:



Programming Considerations

- To write more than one sector, set the high-order byte of the byte count field (DCB word 6) to indicate the number of full sectors to be written. If the last sector is only partially filled with data, set the low-order byte of the byte count field to indicate the number of data bytes in the last sector. If all sectors are filled, set the high-order byte to the number of sectors and the low-order byte to zero. To write less than one full sector, set the high order byte to zero. Set the low-order byte to indicate the number of data bytes to be written.

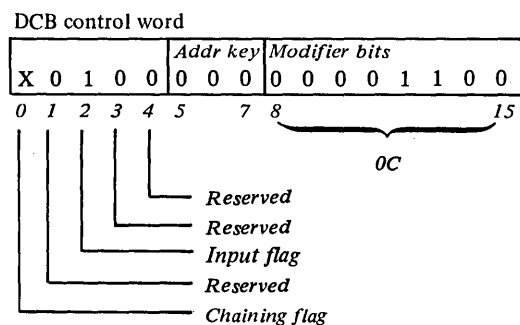
- If a sector buffer is full but the specified sector ID field cannot be located after at least one rotation of the disk, the no record found bit (bit 2) in cycle steal status word 1 is set to 1.
- If an attempt is made to write more sectors than can be contained on a single track, an exception condition code (CC=2) and the status available bit (bit 0) in the ISB are set to 1. The end-of-track bit (bit 0) in cycle steal status word 1 is also set to 1.
- A data check can occur only on the sector ID field when the disk unit is executing a Write Data operation. When this occurs, an exception condition code (CC=2) is set, the status information available bit (bit 0) in the ISB is set to 1, and the file data check and no record found bits (bits 3 and 8) in cycle steal status word 1 are set to 1. The associated data field is not written.

Read Verify Operation

The Read Verify operation should be used after each write data to validate the previously-written data. The Read Verify operation is similar to the Read Data operation. Each specified sector is read completely and the Cyclic Redundancy Check (CRC) bytes are checked to verify the data; however, the data from the disk is not transferred into processor storage. When the operation ends, an interrupt request is sent to the processor.

With the exception of the control word (DCB word 0), the fields of the DCB for a Read Verify operation should be the same as those for the previous write operation. The required DCB fields are: control word, sector ID search argument (flag, cylinder address, head selection, sector number), byte count, and data address. Specify the chain address in DCB word 5 and set the chaining flag in DCB word 0 to 1 when command chaining to another DCB. Set unused DCB words and fields to zero.

The format of the DCB control word for Read Verify is:



Programming Considerations

1. If the CRC check results in an unequal compare:
 - a. an exception condition code (CC=2) is posted
 - b. status information is set in the cycle steal status words
 - c. the status available bit (bit 0) in the ISB is set to 1 and an interrupt is requested.
 A Start Cycle Steal Status command can then be issued to determine the cause of the error. Refer to "Start Cycle Steal Status Command" later in this chapter.
2. If the byte count in the DCB is zero, the operation ends immediately, the DCB Specification check bit in the ISB is set to 1, and an interrupt request is sent to the processor.

Write Sector ID Operation

The Write Sector ID operation records sector ID information on the disk at the location specified in the associated DCB. The sector ID information is transferred from the processor storage location specified in the DCB. The Write Sector ID operation transfers data in cycle steal mode and causes an interrupt when execution is complete.

Write Sector ID is a sector counting operation. The physical sector count field in the DCB is used to determine where the new sector ID should be written. Set the physical sector count field to one less than the number of the physical sector to be written. Beginning at the index point on the track, the sector count is decremented by 1 each time a sector pulse is sensed. When the count reaches zero, the sector ID from storage is written in the next sector location on the disk. For example, to write a sector ID field for sector 3, set the physical sector count to 2 and issue the Write Sector ID; the operation works as follows:

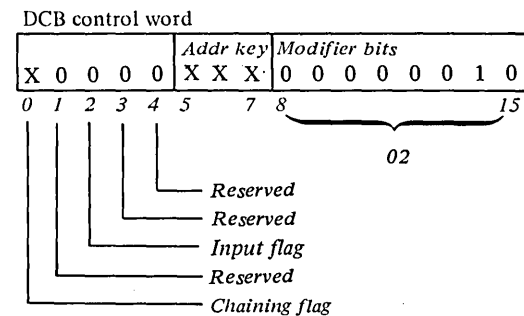
Initial physical sector count = 02

Sequence of events

1. Sense index
2. Sense sector 0
 - a. Check for 00 byte count value
 - b. Decrement count (minus one)
3. Sense sector 1
 - a. Check for 00 byte count value
 - b. Decrement count (minus one)
4. Sense sector 2
 - a. Check for 00 byte count value
 - b. Write sector ID field for sector 3

The DCB for Write Sector ID must contain the following fields: control word, physical sector count, byte count (must be set to X'0006'), data address. Specify the chain address in DCB word 5 and set the chaining flag in DCB word 0 to 1 when command chaining to another DCB. Set unused DCB words and fields to zero.

The format of the DCB control word for Write Sector ID is:



The address word (DCB word 7) must point to the location in storage where the five-byte sector ID to be written is stored. The five bytes correspond to the flag, cylinder address, head selection, and sector number fields in the DCB. Refer to "Using the DCB" earlier in this chapter for information on specifying values for these fields. The two-byte CRC field is written by the disk unit.

Programming Considerations

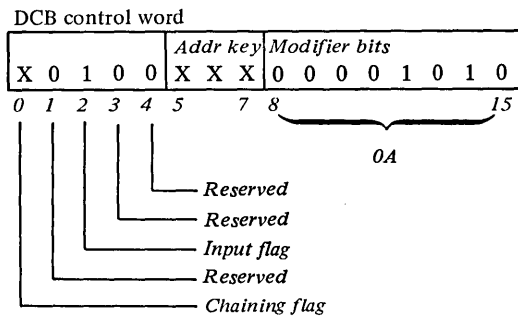
1. If the physical sector byte count is greater than 59, the operation ends immediately, a DCB specification check is set in the ISB, and an interrupt request is presented to the processor.
2. A cylinder address of 152 *must* be specified when a fixed head is accessed during Write Sector ID, or Write Sector ID Skewed operations. The movable heads *must* be positioned over cylinder 152 for every Write Sector ID or Write Sector ID Skewed operation performed on the fixed heads. The position of the movable heads is of no importance for all other fixed head operations.

Read Sector ID Operation

The Read Sector ID operation transfers a sector ID from the disk into the processor storage location specified by the DCB. Six bytes of information—sync byte (0E), flag, cylinder address, head selection, and sector number—are transferred. The Read Sector ID operation operates in cycle steal mode, and an interrupt request is presented to the processor when the operation is completed. Read Sector ID is a sector counting operation. That is, the physical sector byte count field in the DCB determines which sector ID should be brought into storage. Set the physical sector byte count field to one less than the number of the sector to be read. Beginning at the index point on the track, the byte count is decremented by 1 each time a sector ID field is sensed. When the count reaches zero, the next sector ID field is read from the disk and transferred into storage.

The DCB for Read Sector ID must contain the following fields: control word, physical sector count, byte count (must be set to X'0006'), and data address. Specify the chain address in DCB word 5 and set the chaining flag in DCB word 0 to 1 when command chaining to another DCB. Set unused DCB words and fields to zero.

The format of the DCB control word for Read Sector ID is:



The address word (DCB word 7) must point to the location in storage where the five-byte sector ID from the disk is to be stored. The information in the five bytes corresponds to the flag, cylinder address, head selection, and sector number fields in the DCB. Refer to "Using the DCB" earlier in this chapter for information on the content of these fields. The two CRC bytes in the sector ID field are not transferred into storage.

Programming Considerations

If the physical sector byte count is greater than 59, the operation ends immediately, a DCB specification check is posted in the ISB, and an interrupt request is sent to the processor.

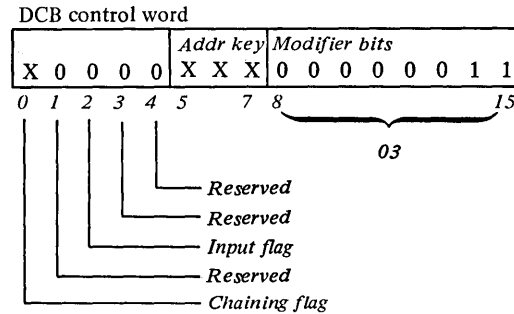
Write Sector ID Skewed Operation

Write Sector ID Skewed is used to write a sector ID field on the disk when a surface defect in the sector ID field prevents the successful completion of a Write Sector ID operation. Write Sector ID Skewed shifts the sector ID field 64 bytes beyond the sector pulse to skip over the surface defect. The Write Sector ID Skewed operation destroys part of the data field. Before using a Write Sector ID Skewed, use a Read Diagnostic operation to recover any data in the defective sector. The sector ID that is written should have bits 6 and 7 of the flag set to 1 and 0 respectively, and the cylinder address should be set to reflect the address of the alternate sector.

In all other respects, a Write Sector ID Skewed operation works the same as a Write Sector ID operation. Data is transferred in cycle steal mode and when the data transfer is completed, an interrupt request is presented to the processor.

The DCB for a Write Sector ID Skewed operation must contain: a DCB control word, physical sector count, byte count (must be set to X'0006'), and data address. Specify the chain address in DCB word 5 and set the chaining flag in DCB word 0 to 1 when command chaining to another DCB. Set unused DCB words and fields to zero.

The format of the DCB control word for a Write Sector ID Skewed operation is:



The physical sector count field must be set to one less than the number of the sectors to be written. The data address word (DCB word 7) must point to the location in processor storage where the five-byte sector ID to be written on the disk is stored. The five bytes correspond to the flag, cylinder address, head selection, and sector number fields in the DCB. Refer to "Using the DCB" earlier in this chapter for information on specifying values for these fields.

Programming Considerations

1. Because it does not leave enough room in the sector for a data field, the Write Sector ID Skewed operation must only be used for defective sectors. The surface condition bit (bit 6) in the flag byte of the sector ID field that is written must always be set to 1.
2. A cylinder address of 152 *must* be specified when a fixed head is accessed during Write Sector ID Skewed operations.

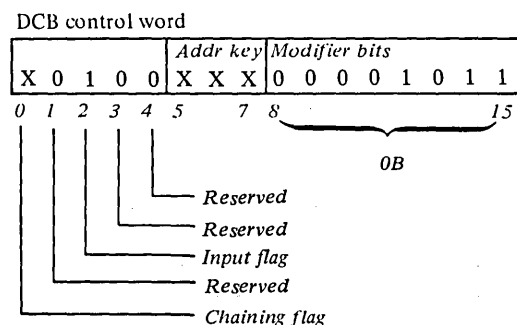
Read Sector ID Skewed Operation

The Read Sector ID Skewed operation is used to read a sector ID that has been written 64 bytes beyond the sector pulse by the Write Sector ID Skewed operation. It locates the sector ID written 64 bytes past the sector pulse and transfers six bytes of sector ID information into the processor storage location specified in the data address word of the DCB. The Read Sector ID Skewed operation is a sector counting operation that transfers data into storage in cycle steal mode. When the data transfer ends, an interrupt request is sent to the processor.

Except for searching 64 bytes beyond the sector pulse, the Read Sector ID Skewed operation works the same as the Read Sector ID operation.

The DCB for a Read Sector ID Skewed operation must contain: a DCB control word, physical sector count, byte count (must be set to X'0006'), and data address. Specify the chain address in DCB word 5 and set the chaining flag in DCB word 0 to 1 when command chaining to another DCB. Set unused DCB words and fields to zero.

The format of the DCB control word for Read Sector ID Skewed is:



The physical sector count field must be set to one less than the number of the physical sector to be read. The data address word (DCB word 7) must point to the location in processor storage where the five-byte sector ID from the disk is to be stored. The information in the five bytes corresponds to the flag, cylinder address, head selection, and sector number fields in the DCB. Refer to "Using the DCB" earlier in this chapter for information on the content of these fields. The CRC bytes in the sector ID field are not transferred into storage.

Programming Considerations

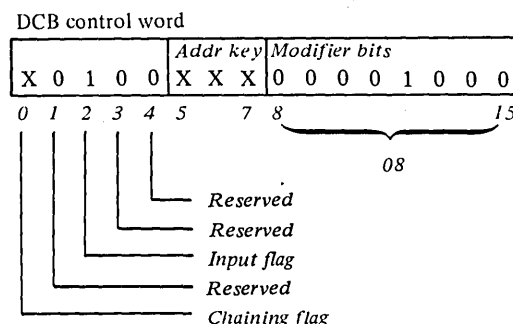
This operation should be used when a Read Sector ID operation consistently results in a data check or sync check. The possibility exists that the sector ID was written 64 bytes beyond the sector pulse by a Write Sector ID Skewed operation.

Read Diagnostic Operation

The Read Diagnostic operation retrieves a data record from a sector with a defective sector ID. Read diagnostic is a sector-counting operation; it determines the required location on the disk from the physical sector byte count field in the DCB. Set the physical sector byte count field (DCB word 2) to one less than the sector containing the desired data field. Beginning at the index point on the track, the byte count is reduced by 1 each time a sector ID is sensed. When the count reaches zero, the data field from the next sector on the disk is transferred into processor storage. The storage location is specified in the data address word (DCB word 7). The Read Diagnostic operation transfers data in cycle steal mode and requests an interrupt when the operation is completed.

The DCB for Read Diagnostic operation must contain the following fields: control word, physical sector count, byte count (must be set to X'0100'), and data address. Specify the chain address in DCB word 5 and set the chaining flag in DCB word 0 to 1 when command chaining to another DCB. Set unused DCB words and fields to zero.

The format of the DCB control word for a Read Diagnostic operation is:



The address word (DCB word 7) must point to a location in storage where the 256 bytes of data are to be stored.

Programming Considerations

1. If the physical sector count field is greater than 59, the operation ends immediately, a DCB specification check is posted in the ISB, and an interrupt request is sent to the processor.
2. Sector ID errors detected during the Read Diagnostic operation are ignored.

Immediate ID Operations

There are two immediate ID operations:

- Read sector ID immediate
- Write sector ID immediate

Immediate ID operations are time dependent and are intended to read or write a full track at the maximum rate of data transfer.

To read or write a full track of IDs using an immediate ID operation, the program must be in a dedicated mode and timing requirements must be adhered to. The timing requirements are as follows:

1. Loop on read diagnostic—sense word 1 testing index long (bit 07) for a 0 condition.
2. Loop on read diagnostic—sense word 1 testing index long (bit 07) for a 1 condition.

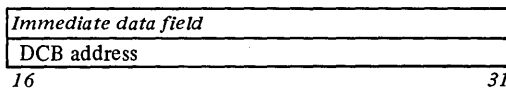
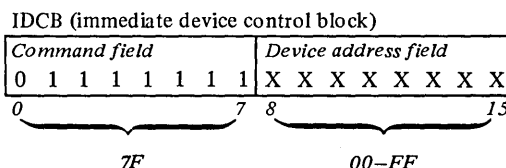
3. Read or write immediate ID operation—issue either a read or write immediate ID operation with 30 DCBs chained together. Each DCB is formatted the same as a normal read or write ID operation except the physical sector count field is not used. The 30 IDs to be read or written start with logical sector 01 and continue sequentially through ID and end with logical 00. See logical sector to physical sector conversion chart below.
4. Loop on read diagnostic—sense word 1 testing index long (bit 07) for a 0 condition.
5. Read or write immediate ID operation—issue either a read or write immediate ID operation with 30 DCBs chained together. The 30 IDs to be read or written start with logical sector 1F and continue sequentially through 3B and end with 1E. See logical sector to physical sector conversion chart below.

Hex conversion of logical sector number to physical sector number			
Logical	Physical	Logical	Physical
00	00	0F	1E
1E	01	2D	1F
01	02	10	20
1F	03	2E	21
02	04	11	22
20	05	2F	23
03	06	12	24
21	07	30	25
04	08	13	26
22	09	31	27
05	0A	14	28
23	0B	32	29
06	0C	15	2A
24	0D	33	2B
07	0E	16	2C
25	0F	34	2D
08	10	17	2E
26	11	35	2F
09	12	18	30
27	13	36	31
0A	14	19	32
28	15	37	33
0B	16	1A	34
29	17	38	35
0C	18	1B	36
2A	19	39	37
0D	1A	1C	38
2B	1B	3A	39
0E	1C	1D	3A
2C	1D	3B	3B

Start Cycle Steal Status Command

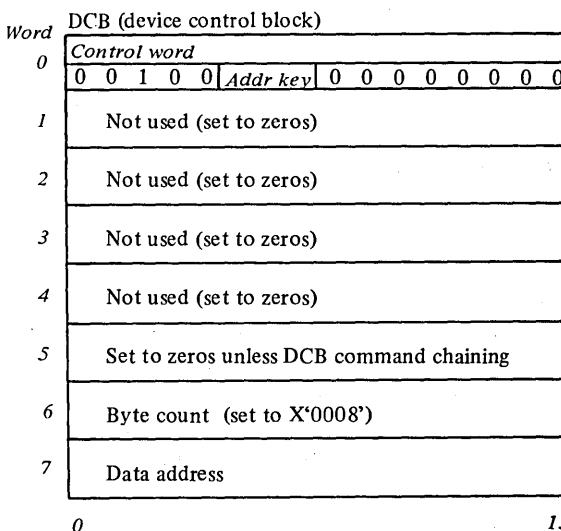
The Start Cycle Steal Status command transfers four words of status information into processor storage beginning at the data address location specified in DCB word 7. The information in the cycle steal status words can be used to determine why the previous command did not execute properly. The command operates in cycle steal mode and an interrupt request is presented to the processor when the operation ends.

The Start Cycle Steal Status command requires an Operate I/O instruction with the address of an IDCB, an IDCB with the address of a DCB, and the DCB. The format of the IDCB is:



The DCB for a Start Cycle Steal Status command must contain: a DCB control word, a byte count (must be set to X'0008'), and a data address. The data address specifies the storage location into which the four words of status information are to be transferred. All unused DCB words and fields must be set to zero.

The format of the DCB for a Start Cycle Steal Status command is:



Programming Considerations

1. If the file data check bit (bit 8 of SCSS word 1) is set to 1 after a Read Data or Read Verify operation, the invalid field can be either the sector ID or the data. The sector ID field is invalid if the no record found bit (bit 3 of SCSS word 1) is also set to 1. The data field is invalid if the no record found bit is set to 0. If the sector ID field caused the error and the operation involved multiple sectors, any data transferred before the error occurred is valid. Refer to the residual address in SCSS word 0 to determine the address of the last data word transferred into processor storage.
2. If the file data check bit (bit 8 of SCSS word 1) is set to 1 after a Write data operation, an invalid sector ID field was detected. When an invalid sector ID is detected, the associated data field is not written. If the operation involved multiple sectors, the sector number the disk unit attempted to write is located in cycle steal status word 2. All data fields up to the invalid sector will have been written.
3. The chaining flag in the control word (DCB word 0) must be set to 0. DCB command chaining is not supported for the Start Cycle Steal Status command.
4. The disk unit responds 'busy' to all commands except Prepare, Read Device ID, Device Reset, or Halt I/O from the time a Start Cycle Steal Status command is received until an interrupt request is serviced by the processor.

Status Information

Three types of status information (see Figure 3-9) inform the processor of the results of input/output operations:

- Condition codes
- Interrupt ID word
- Cycle steal status information

Condition Codes

Condition codes are posted after execution of each I/O instruction. See Figure 3-8. For commands that do not cause interrupts, the condition code reported after the Operate I/O instruction executes is the only status information available. The appropriate condition code is set in the Even, Carry, and Overflow bit positions of the *level status register* (LSR) in the processor. (Refer to "Prerequisite Publications" in the Preface of this manual for order number of IBM Series/1 processor unit description manuals.)

Command	Condition Code (CC) Values							
	CC0	CC1	CC2	CC3	CC4	CC5	CC6	CC7
Prepare	X					X		X
Device reset	X							X
Read device ID	X					X		X
Start	X	X		X		X		X
Start cycle steal status	X	X		X		X		X

CC

Value	Meaning
0	Device not attached
1	Busy
2	Not reported
3	Command reject
4	Not reported
5	Interface data check
6	Not reported
7	Satisfactory

Notes.

1. If an odd DCB address is stored in the IDCBC immediate data field for a Start or Start Cycle Steal Status command, a command reject condition (CC=3) is reported.
2. If the disk unit is not ready for operations when a Start command is issued, a command reject condition code (CC=3) is reported.
3. Condition code zero (CC=0) is reported if the disk unit is not attached to the channel.

Figure 3-8. Condition code responses to Operate I/O instructions

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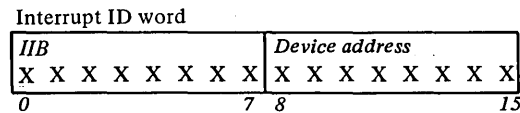
When commands and changing status within the disk attachment cause interrupts, a condition code is also transferred into the processor LSR at interrupt presentation time. The condition code values that can be reported at interrupt presentation time are:

CC Value	Meaning
0	Not reported
1	Not reported
2	Exception
3	Device end (satisfactory)
4	Attention
5	Not reported
6	Not reported
7	Not reported

For condition code 2, a second level of status is available in the Interrupt Status Byte (ISB) of the interrupt ID word. For condition codes 3 and 4, the interrupt status byte contains binary zeros.

Interrupt ID Word

Interrupt status information is transferred to the processor in an interrupt ID word. The low-order byte of the interrupt ID word contains the address of the interrupting device: the high-order byte is an Interrupt Information Byte (IIB).



If commands that cause interrupts fail to end properly (CC=2), the IIB has a special format and is called the Interrupt Status Byte (ISB).

Interrupt Status Byte (ISB)

When an interrupt is caused by an exception condition (CC=2), the interrupt ID word containing the device address and Interrupt Status Byte (ISB) is transferred to the processor. The ISB bit meanings are:

ISB bit	Meaning
0	<i>Device Status Available.</i> Additional information about the operation is available when this bit is set 1. The information is stored in cycle steal status word 1. To obtain the information, issue a Start Cycle Steal Status command. Refer to "Start Cycle Steal Status Command" earlier in this chapter.
1	<i>Not reported.</i> This bit is always set to 0.
2	<i>Not reported.</i> This bit is always set to 0.
3	<i>DCB Specification Check.</i> If this bit is set to 1, the disk operation failed because of an invalid DCB parameter. Any of the eight words in the DCB associated with the disk operation can set this bit to 1. The residual address stored in cycle steal status word 0 points to the DCB word containing the invalid parameter. To obtain the residual address, refer to "Start Cycle Steal Status Command" earlier in this chapter.
4	<i>Storage Data Check.</i> If data accessed from processor storage during a cycle steal output operation is out of parity, the operation is terminated and this bit is set to 1. A machine check condition does not occur, and the parity of the data in that storage location is not corrected. If a data storage check occurs, the data in the partially filled sector buffer is not written on the disk.
5	<i>Invalid Storage Address.</i> When the storage address specified in the DCB is outside the storage capacity of processor storage, this bit is set to 1. The bit can be set during either an input or output cycle steal operation. The operation is terminated immediately.
6	<i>Protect Check.</i> An attempt to move data into a processor storage location using an incorrect cycle steal address key sets this bit to 1. The operation is terminated immediately.
7	<i>Interface Data Check.</i> When a parity error is detected at the interface this bit is set to 1. The operation is terminated immediately.

Figure 3-9 summarizes the status information available in condition codes, in the ISB, and in cycle steal status word 1.

Operate I/O Instruction Execution Time	
<i>CC Value</i>	<i>Meaning</i>
0	Device not attached
1	Busy
2	Not reported
3	Command reject
4	Not reported
5	Interface data check
6	Not reported
7	Satisfactory

Interrupt Presentation Time	
<i>CC Value</i>	<i>Meaning</i>
0	Not reported
1	Not reported
2	Exception
3	Device end (satisfactory)
4	Attention
5	Not reported
6	Not reported
7	Not reported

Indicates more information in interrupt status byte (ISB)

Interrupt Status Byte	
<i>Bit Position</i>	<i>Meaning</i>
0	Device status available
1	Not reported
2	Not reported
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Indicates more information in cycle steal status word 1

Issue a start cycle steal status command	
<i>Cycle Steal Status Word 1</i>	
<i>Bit Position</i>	<i>Meaning</i>
00	End of track
01	Sync check
02	Echo check
03	No record found
04	Write gate check
05	Serializer/deserializer check
06	PLO out of sync check
07	Unsafe
08	File data check
09	Seek check
10	Brake failure
11	Write unsafe
12	Select unsafe
13	Servo unsafe
14	Attachment buffer parity check
15	Not ready or power off

Figure 3-9. Status information summary

Cycle Steal Status Words

Cycle steal status words containing additional status information are transferred into processor storage by the Start Cycle Steal Status command.

Cycle Steal Status Word 0

This word contains the residual address. For read operations, cycle steal status word 0 contains the processor storage address where the last cycle steal of data occurred. For write operations, the residual address may be up to four sectors in advance of the sector being written on the disk. The residual address can be either the address of a word of data or the address of a word in the DCB. The residual address is *not* updated during Start Cycle Steal Status command execution.

Cycle Steal Status Word 1

Each bit in this word indicates a reason why a normal end-of-operation response to the previous Start command did not occur. The bits have the following meanings.

Bit

Position	Meaning
0	<i>End of track.</i> When at least one but not all of the sectors in a multiple sector operation has been transferred and the end of the last sector on the track is detected, this bit is set to 1.
1	<i>Sync check.</i> When an unequal comparison for the 'OE' sync byte at the beginning of either an ID or data field occurs, this bit is set to 1. If an ID field caused the error, bit 3 of SCSS word 1 is also set to 1.
2	<i>Echo check.</i> If data sent from the serializer-deserializer (serdes) register to the disk does not compare equal to the data "echoes" resulting from the write operation, this bit is set to 1.
3	<i>No record found.</i> If, after at least one rotation of the disk, the disk unit has not found a sector ID that compares equal to the search argument sector ID, this bit is set to 1.
4	<i>Write gate check.</i> When a sector or index pulse is sensed, 'write gate' should be inactive. If 'write gate' is active when a sector or index pulse is sensed, this bit is set to 1.
5	<i>Serializer-deserializer check.</i> If a bit is either lost or gained when the parallel channel data is converted to serial data during a write operation, this bit is set to 1.
6	<i>Phase locked oscillator (PLO) out of sync check.</i> When the PLO in the disk unit is not synchronized, this bit is set to 1.
7	<i>Unsafe.</i> If a malfunction results in an unsafe condition, this bit is set to 1. If an unsafe condition exists, read/write and Seek operations are inhibited. An unsafe condition indicates that one or more of the unsafe conditions (bits 11–13) are present.
8	<i>File data check.</i> If the CRC bytes that validate each sector ID field and data field are in error, this bit is set to 1.
9	<i>Seek check.</i> If a Seek operation fails to execute successfully within approximately two seconds, this bit is set to 1.

10	<i>Brake failure.</i> The brake coil has either opened or shorted.
11	<i>Write unsafe.</i> Write selected and no write transitions detected, or write not selected and write current detected.
12	<i>Select unsafe.</i> Write selected and more than one head selected.
13	<i>Servo unsafe.</i> Write selected and heads not on track, or write selected and PLO out of sync.
14	<i>Attachment buffer parity check.</i> If parity is incorrect for a word of data from the device buffer during a read operation, this bit is set to 0. Words with incorrect parity are not transferred into processor storage.
15	<i>Not ready or power off.</i> When power-up is incomplete or the disk unit is (1) not up to rotational speed, (2) failed to recalibrate after initial power-up, or (3) is unsafe, this bit is set to 1. The unsafe and associated not ready condition may be reset with a Device Reset or Halt I/O command.

Notes.

- Bits 0 through 6, 8, 9, and 14 are reset if the response to the next Start command is a condition code of 7 (satisfactory).
- Bit 7, bits 10 through 13, and also bit 15 (unless set to 1 by a power-on delay) may be reset using a system reset, a power-on reset, or Device Reset or Halt I/O command.

Cycle Steal Status Word 2

If a write operation ends early because of an error, this word identifies the last sector the disk unit attempted to write. Bits 0 through 9 of cycle steal status word 2 are set to zero, and bits 10 through 15 are set to indicate the sector number. An exception condition code (CC=2) is presented at interrupt presentation time. For write operations that end normally, the sector number found in bits 10 through 15 is one greater than the last sector transferred to the disk unit.

Cycle Steal Status Word 3

This word is reserved.

I/O Interrupts

The disk unit can interrupt the processor with two types of interrupts: end-of-operation and attention. Before either type can interrupt the processor, however, the disk unit must be prepared to interrupt. Refer to "Prepare Command" described earlier in this chapter.

Note. Hardware processing of an interrupt includes automatic branching to a service routine. The processor uses a reserved area in storage for branch information. Refer to "Prerequisite Publications" in the Preface of this manual. Processor description manuals explain reserved storage and interrupt handling.

End-of-Operation Interrupts

When an operation initiated by any of the interrupt-causing commands ends normally or ends due to an error, an interrupt request is sent to the processor. The interrupt-causing commands are:

- Start
- Start Cycle Steal Status (SCSS)

The disk unit enters the 'busy' state when either command is received from the processor. Until the disk unit completes an operation initiated by an interrupt-causing command, it responds 'busy' to all other such commands. However, non-interrupting commands (Prepare, Device Reset, Read ID, or Halt I/O) are accepted and executed. A condition code is reported for all interrupt-causing commands when the I/O instruction is executed and when the interrupt request is serviced by the processor. The first condition code indicates whether the command has been accepted and the second is transferred to the processor with interrupt status information at interrupt presentation time. See Figure 3-9.

Interrupt status information is transferred to the processor in an interrupt ID word. The low-order byte of the interrupt ID word is the device address; the high-order byte is called an Interrupt Information Byte (IIB). If interrupt-causing commands fail to end properly (CC=2), the IIB has a special meaning and is called an Interrupt Status Byte (ISB).

Attention Interrupts

The attention interrupt request is sent to the processor only when:

1. A Prepare command has been issued which allows interrupts.
2. The disk unit is not 'busy'.
3. The disk unit has become 'ready' (operational).

Note. When the disk unit goes from 'ready' (operational) to 'not ready' (not operational), an attention interrupt request is *not* sent to the processor.

Resets (Disk)

Several methods of resetting controls and registers are available.

Power-on Reset. Resets: residual address register, prepare register, last sector register, data register (16 bits), and cycle steal request.

System Reset. Resets: prepare register, last sector register, and cycle steal request.

Initial Program Load (IPL). Resets: prepare register, last sector register, and cycle steal request.

Halt I/O Command. Resets: last sector register and cycle steal request.

Device Reset Command. Resets: last sector register.

Initial Program Load (IPL)

An Initial Program Load (IPL) operation loads 128 words (256 bytes) of control information from cylinder 000, sector 00 on the disk into processor storage beginning at location zero. The information initializes the processor with the program data required to begin operations. Initial Program Load operations are hardware initiated only.

When 'IPL select' is received from the processor an automatic Seek Recalibrate operation selects head 0 and moves the access mechanism to cylinder 000. Following the Seek/Recalibrate operation, a Read Data operation with a byte count of X'0100' (256 decimal) transfers the data from sector 00 on the disk into storage. When the IPL sequence ends, a device end condition code is presented to the processor on interrupt level 0. If an error is detected during the IPL sequence, the load indicator on the processor console remains *on* until another attempt to IPL succeeds or a system reset/power-on reset occurs.

The 4962 Disk Storage Unit can be used as either a primary or alternate system IPL source.

Data Security

If a disk enclosure is removed from a disk unit and returned to the factory for any reason (defective, reconfiguration, etc.), proprietary information that may be stored on the disk is treated in the following manner:

<i>Disk Enclosure Condition</i>	<i>Action</i>
Operational	Data stored on the disk is overwritten using a single write operation on every track.
Disk enclosure is defective but the disk is ok.	Data stored on the disk is overwritten using a single write operation on every track, and repairs are made.
Defective disk	The disk is demagnetized and destroyed.

The user is responsible for restoring data on disks returned from the factory.

Fixed Head Data Integrity. Data stored in tracks accessed by the eight fixed heads should be refreshed after every power-off/power-on cycle. Ambient magnetic fields in the vicinity of the disk enclosure should not exceed two gauss.

If the disk enclosure is removed from the disk unit for any reason, the integrity of the data stored on the disk may be affected.

Chapter 4. Programming Diskette Operations

This chapter describes the I/O commands required to perform input/output operations on the IBM 4964 Diskette Unit, and the diskette unit in an IBM 4962 Disk Storage Unit Model 2, 2F, and 4. The commands that can be issued, the instruction and control blocks required for each command, and the individual diskette operation are described. Status information and I/O interrupts are also described in this chapter.

Data Transfer Operations

Data is transferred on the I/O channel in a parallel operation (16 data bits plus 2 parity bits). On a write operation, parity bits are removed and the data bits are transferred serially to the diskette. On a read operation, the data bits are read serially from the diskette, parity bits are added, and the information is transferred one word at a time into processor storage. The direction in which data moves is determined by the I/O command. The command also determines whether data moves to or from processor storage under direct program control only, or under direct program control and in cycle steal mode.

Direct Program Control (DPC)

An I/O command executed under direct program control transfers a word of data or control information to or from processor storage. After moving the immediate data word, the processor continues with other instructions.

Cycle Steal (CS)

When data is transferred in cycle steal mode, processing and I/O operations are overlapped. Overlapping allows the processor to execute other instructions while the diskette unit is cycle stealing the data required to complete the I/O operation. Data is transferred by stealing storage cycles from the processor.

Initiating a Diskette Operation

Every I/O operation to the diskette unit requires (in processor storage):

1. an Operate I/O instruction
2. an I/O command, device address, and immediate data field.

Operate I/O Instruction

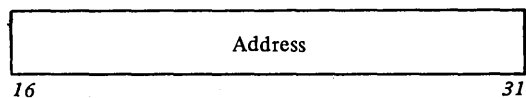
The Operate I/O instruction points to an Immediate Device Control Block (IDCB) in storage containing an I/O command, device address, and immediate data field. Refer to "Using the IDCB" later in this chapter. Every Operate I/O instruction must have an associated IDCB.

Note. The Operate I/O instruction is described more completely in IBM Series/1 processor unit description manuals. Refer to "Prerequisite Publications" in the Preface of this manual for titles and order numbers.

The format of the Operate I/O instruction is:

Operate I/O Instruction

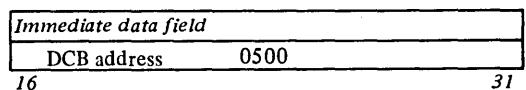
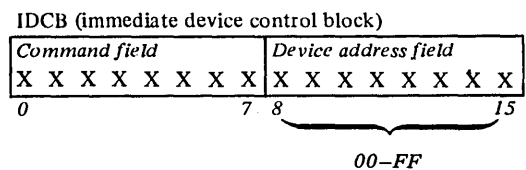
Operation Code				R2				Function					
0	1	1	0	1					*	1	1	0	0
0				4 5 7 8				10 11 12 15					



Using the IDCB

An Immediate Device Control Block (IDCB) must be reserved in processor storage for every I/O command issued to the diskette unit. Before issuing an Operate I/O instruction to the diskette unit, an I/O command and device address must be stored in the associated IDCB. The immediate data field of the IDCB must contain a data word, a DCB address, or zeros. I/O commands that execute only under direct program control require a data word or zeros, while commands that also transfer data in cycle steal mode require a DCB address. Refer to "I/O Commands and Diskette Operations."

The format of the IDCB is:



I/O Commands and Diskette Operations

The I/O command stored in the IDCB determines whether a single word of immediate data is transferred under direct program control only or, following the DPC operation, additional words of data are to be transferred into or from processor storage in cycle steal mode. See Figure 4-1.

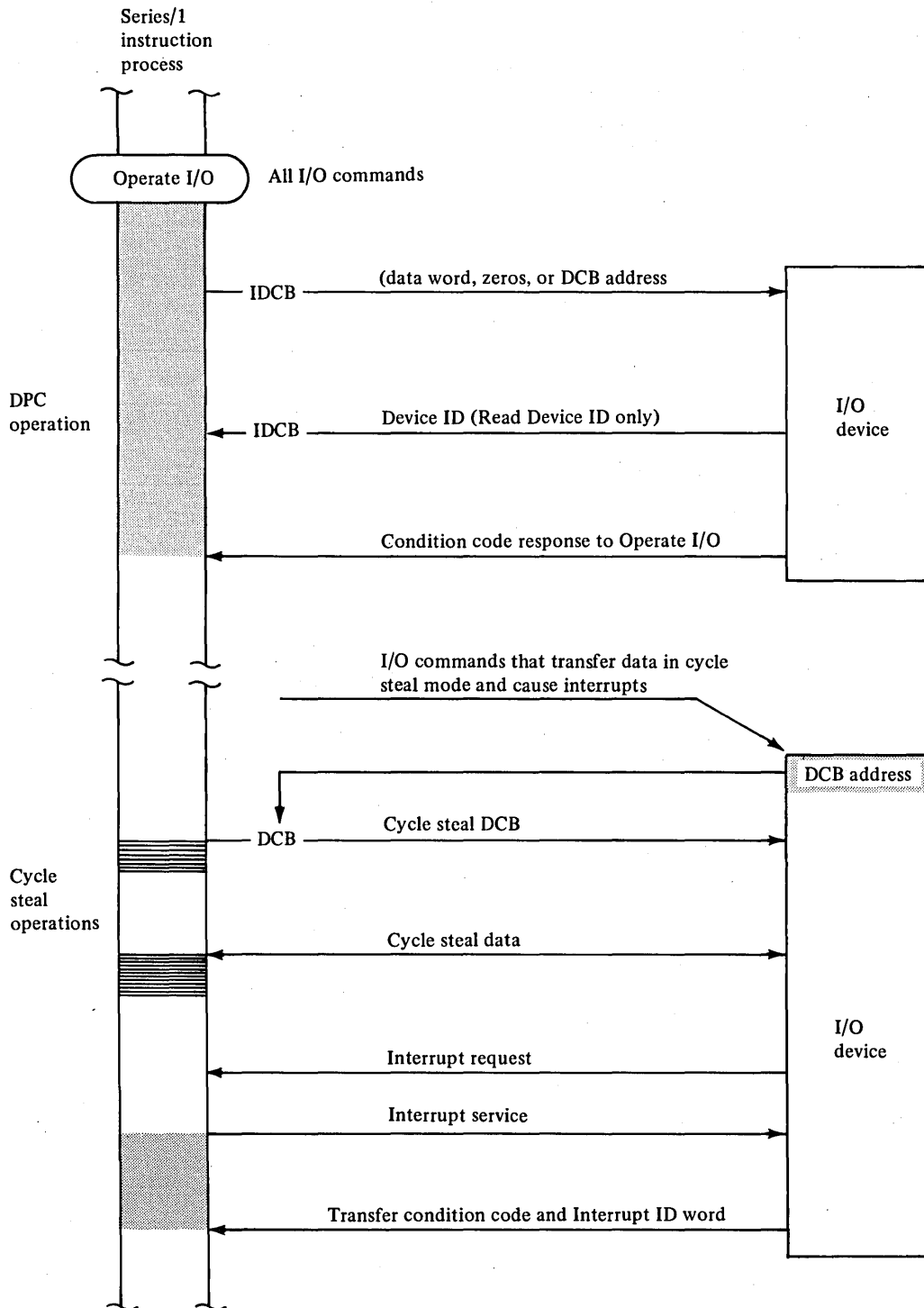


Figure 4-1. Overview of an I/O operation

Command Execution Under Direct Program Control

Prepare, Device Reset, and Read Device ID commands transfer a single word of data under direct program control to or from the immediate data field of an IDCB in processor storage. See Figure 4-2. Command execution is complete when a condition code is reported to the processor following the DPC operation. Refer to "Condition Codes" later in this chapter. Processing of other instructions resumes when the I/O operation ends.

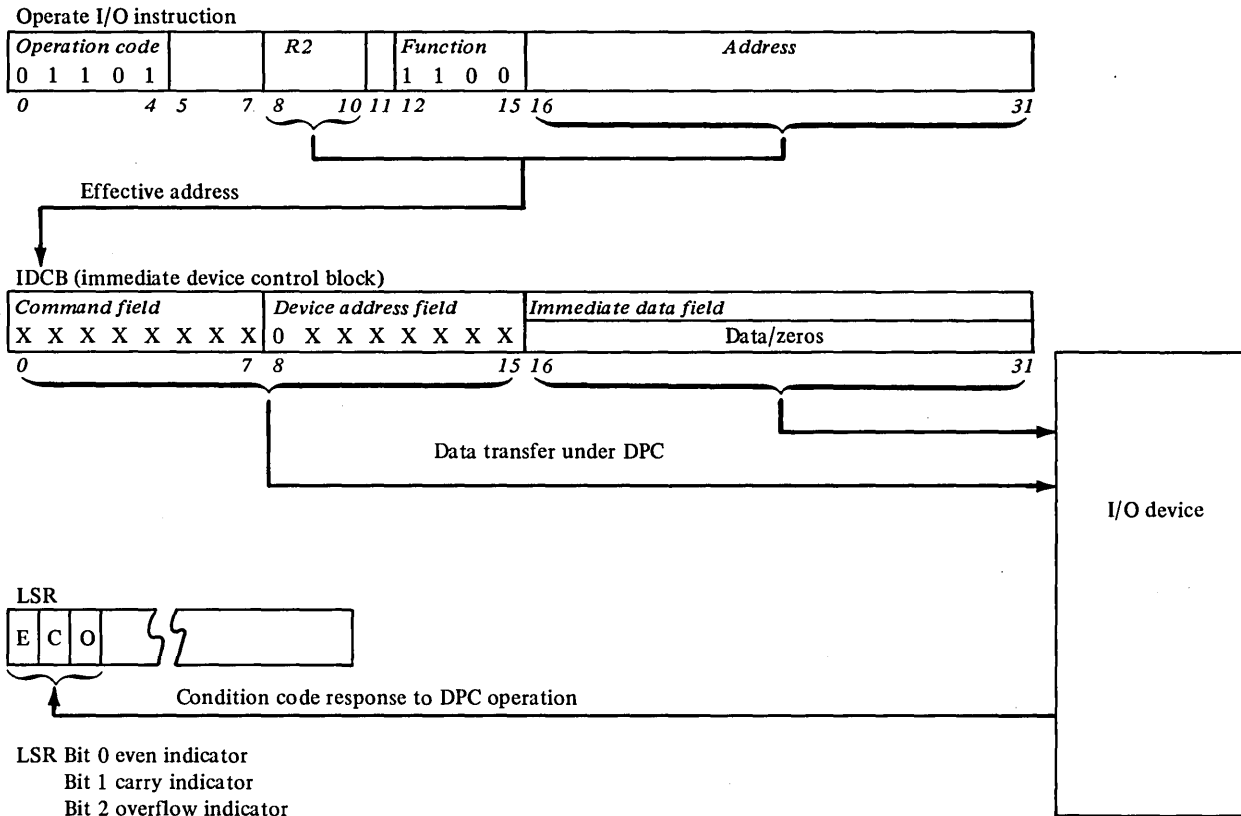
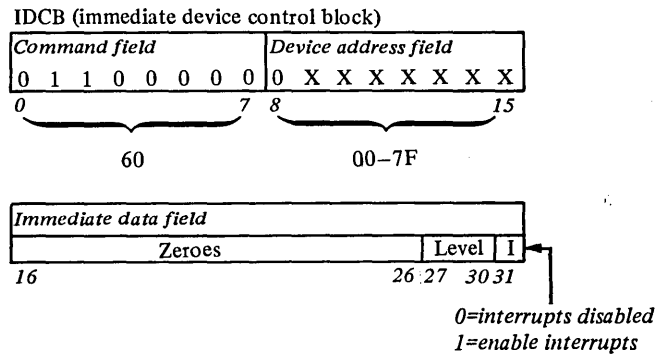


Figure 4-2. I/O operation initiated and executed exclusively under direct program control

Prepare Command

Before using any of the interrupt-causing commands, a Prepare command must be issued to the diskette unit. The Prepare command transfers a word containing interrupt parameters from the IDCB immediate data field associated with the command to the *Prepare Register* in the diskette attachment. The interrupt parameters in this word establish whether the diskette unit is allowed to interrupt, and if so, the level on which processing operations can be interrupted. The Prepare command is executed under direct program control (DPC) and does not cause an interrupt.



Note. For information about interrupt levels, refer to "Prerequisite Publications" in the Preface of this manual.

Device Reset Command

The Device Reset command resets all pending interrupts and previously established control and status conditions. The device ID, device address, data address, residual address, and prepare registers are not reset by this command. The command code and device address in the IDCB supply the information required to execute the Device Reset command. Although the IDCB immediate data field is not used and not checked, set the bits to zeros. The Device Reset command is executed under direct program control and does not cause an interrupt.

The format of the IDCB for a Device Reset command is:

IDCB (immediate device control block)

Command field								Device address field							
0	1	1	0	1	1	1	1	0	X	X	X	X	X	X	X
0 7								8 15							
6F								00-7F							

Immediate data field															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16 31															

Read Device ID Command

The Read Device ID command loads the diskette unit device ID word into the immediate data field of the IDCB associated with the command. Read Device ID executes under direct program control; the device ID is transferred immediately into storage, and a condition code is reported to the processor. Refer to "Status Information" later in this chapter.

The format of the IDCB for the Read Device ID command is:

IDCB (immediate device control block)

Command field								Device address field							
0	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X
0 7								8 15							
20								00-7F							

Immediate data field															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16 31															

Before issuing a Read Device ID command, set the IDCB immediate data field associated with the command to zero. During command execution, the device ID is transferred under DPC to this field. After execution of the Read Device ID command, the immediate data field in the IDCB associated with the command contains:

Immediate data field																
0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0
16 31																
X'0106'																

Command Execution in CS Mode

Start and Start Cycle Steal Status commands transfer data in cycle steal mode. The DCB address associated with either command, however, is transferred under DPC from the IDCB immediate data field in processor storage to the diskette unit. See Figure 4-3. When the diskette unit accepts the command and DCB address, a condition code is reported to the processor. The processor continues with other operations and the diskette unit begins cycle stealing the data required to complete the I/O operation. When the transfer of data in cycle steal mode ends, an interrupt request is sent to the processor. At interrupt presentation time, a condition code and interrupt ID word are transferred to the processor. The I/O operation ends and the processor continues with other operations.

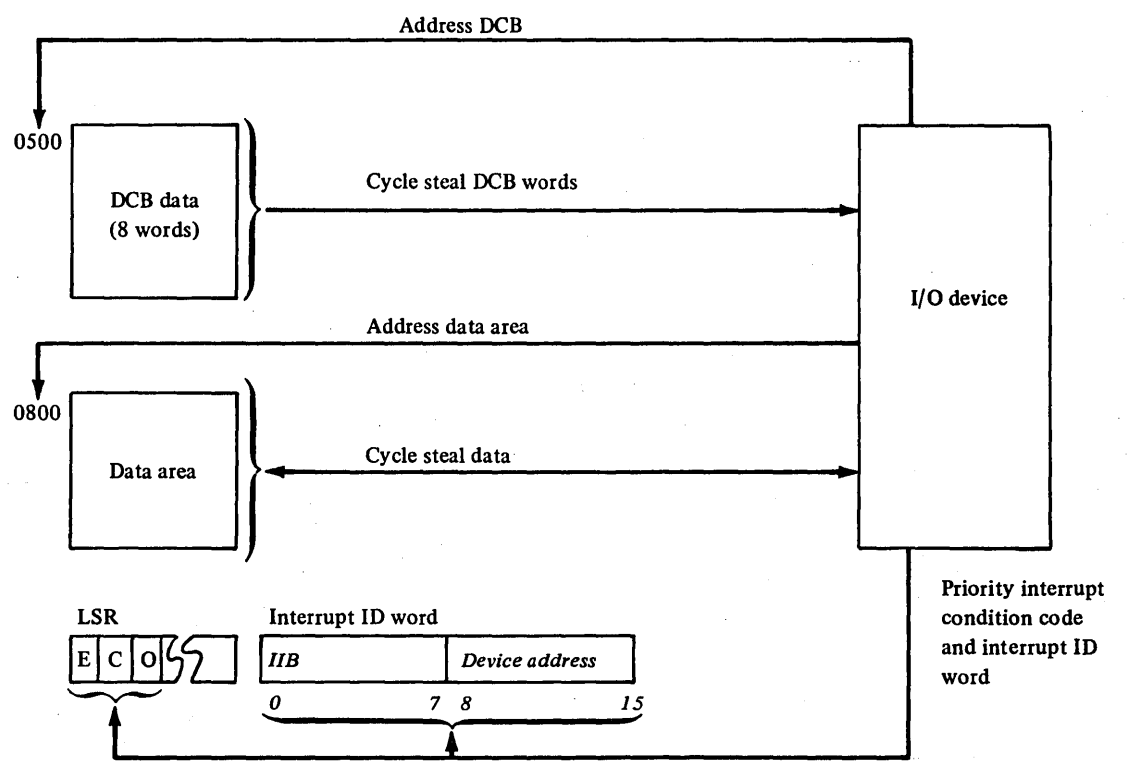
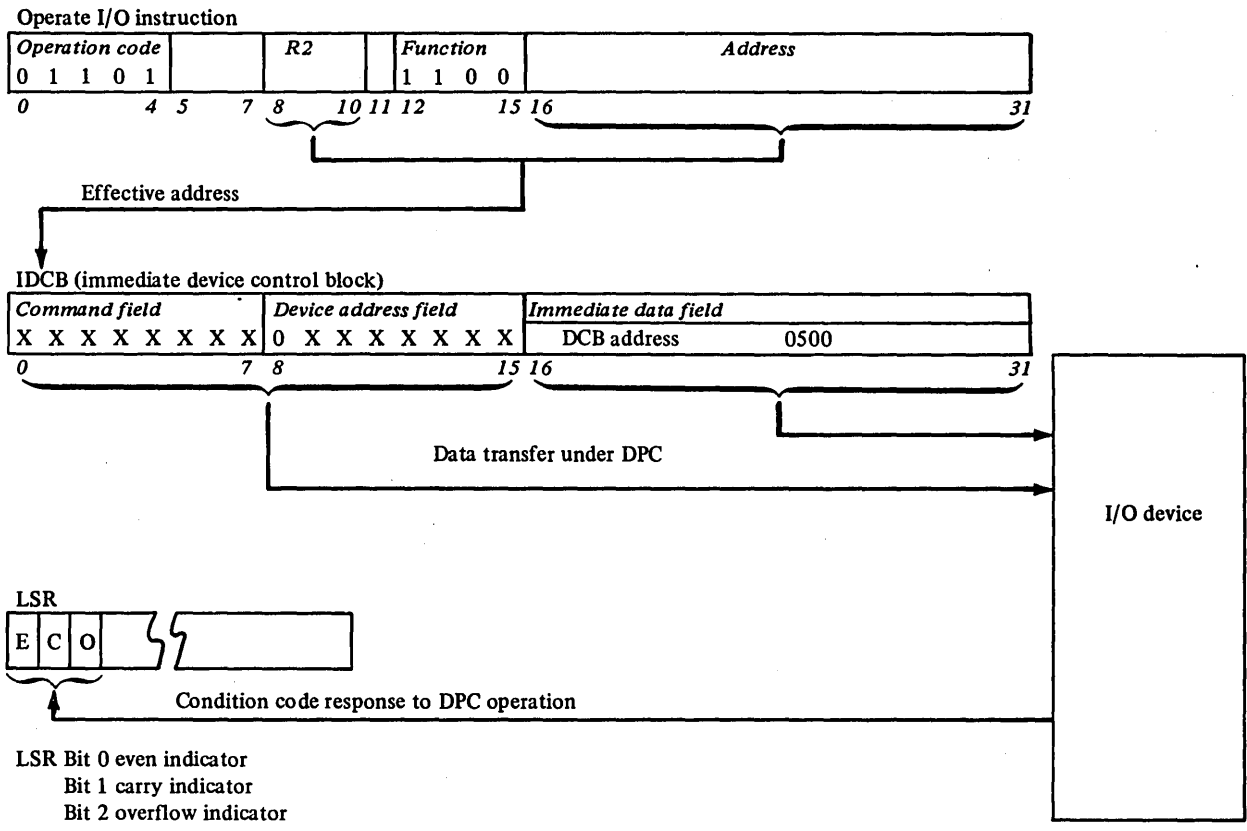


Figure 4-3. I/O operation initiated under direct program control and executed in cycle steal mode

Using the DCB

A Device Control Block (DCB) comprised of eight contiguous processor storage locations must be reserved for every I/O operation that transfers data in cycle steal mode and causes interrupts. See Figure 4-4. A separate DCB is required for:

- a Start command
- a Start Cycle Steal Status command
- all diskette operations included in a DCB command chaining sequence (refer to "DCB Command Chaining" in this chapter.)

Device parameters that define and control the diskette operation must be stored in a DCB.

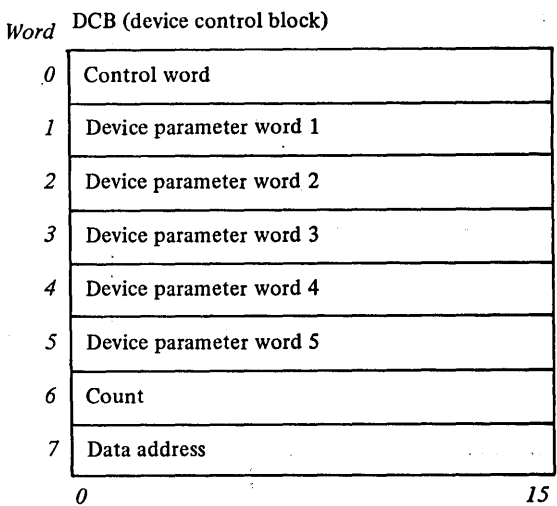


Figure 4-4. DCB format (Start command shown)

General information about each word and field in the DCB is supplied in the sections that follow; specific information about each operation is presented later in this chapter.

DCB Control Word (DCB Word 0)

Figure 4-5 shows the format of the DCB control word. This word occupies the first position of each DCB associated with a Start or Start Cycle Steal Status command. The DCB control word delineates the diskette operation.

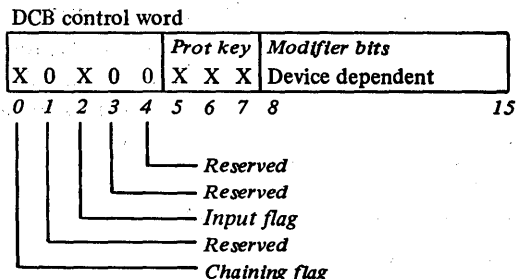


Figure 4-5. DCB control word format

The meaning of the bits is as follows:

- Bit 0 (chaining flag)** Set this bit to 1 to specify DCB command chaining. When the operation called for by the current DCB ends, the chain address stored in DCB word 5 points to the next DCB in the chained sequence. Refer to "DCB Command Chaining" later in this chapter.
- Bit 1 (reserved)** Set this bit to 0 to avoid future code obsolescence.
- Bit 2 (input flag)** Set the input flag bit to 1 for diskette operations that transfer data into processor storage. Set the bit to 0 for diskette operations that transfer data from storage and for Seek/Seek Recalibrate operations.
- Note.* If the input flag bit setting is not consistent with the type of operation, the operation ends and an interrupt request is sent to the processor. At interrupt presentation time, an exception condition and a DCB specification check are presented to the processor.
- Bit 3 (reserved)** Set this bit to 0 to avoid future code obsolescence.
- Bit 4 (reserved)** Set this bit to 0 to avoid future code obsolescence.
- Bits 5-7 (address key)** These bits represent the cycle steal address key required for storage authorization at cycle steal request time.
- Bits 8-15** The bits in this field are device dependent modifiers of the Start command. A bit configuration must be selected that represents the diskette operation to be performed. The selected operation must be compatible with the setting of the input flag (bit 2). The hexadecimal designation for each operation and the corresponding setting of bit 2 are shown in Figure 4-6.

Note. Burst mode (bit 15) is not supported by the 4962 and 4964.

Bit 2	DCB control word modifier bits 8-15	Hexadecimal equivalent	Operation
0	00000001	01	Write Data/Data AM
0	00000010	02	Format Track
0	00000011	03	Write Data/Control AM
1	00001001	09	Read Data
0	00001100	0C	Read Verify
1	00001010	0A	Read Sector ID
0	00000101	05	Seek
0	00000111	07	Seek Recalibrate

Figure 4-6. DCB control word modifier bit configurations

Seek Control Word (DCB Word 1)

The seek control word is used, in conjunction with the head address specified in the high-order byte of DCB word 4, to control the Seek operation. The seek control word specifies the direction of the seek—either toward the outer perimeter of the diskette or toward its center—and the number of cylinders to be crossed. Figure 4-7 shows the format of the seek control word.

Notes.

1. The seek control word is used only for Seek operations.
2. If the seek control word is set to zero for a Seek operation, no seek movement occurs.
3. Because they are not required for a Seek operation, set DCB word 3, DCB word 6, and the sector number field in DCB word 4 to zeros.

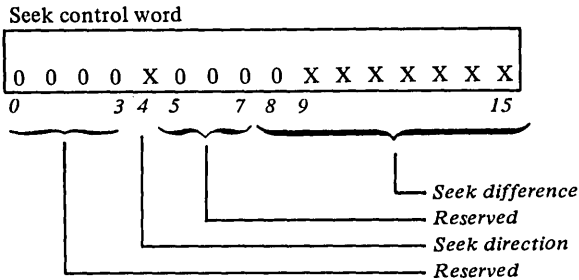


Figure 4-7. Seek control word format

The meaning of the seek direction and seek difference fields are as follows:

- Bit 4 (seek direction)** To increase the cylinder number (seek toward the center of the diskette), set this bit to 0. To seek to a lower cylinder number (toward the outer edge of the diskette), set this bit to 1.
- Bits 8–15 (seek difference)** These eight bits specify the seek difference (the number of cylinders to be moved). If a seek difference of zero is specified, no cylinders are crossed and a device end condition is reported at interrupt presentation time.

Note. Designating a seek difference beyond either physical cylinder limit (00/76) does not necessarily place the heads at cylinder 00 or 76. The access mechanism may stop in the wrong track or between tracks. In either case, an error will not be detected until a subsequent read or write operation fails to locate the proper sector ID.

Bits 0–3 and 5–7 in the seek control word are reserved; set them to 0 to avoid future code obsolescence.

Format Data Word (DCB Word 2)

The format data word contains the word of data to be written in every word of every sector on a track during a Format Track operation. The sector length and cylinder fields in DCB word 3 must contain valid values. If the sector length byte contains binary 1111 0000, the entire track is formatted into 128-byte defective sectors. Refer to “Format Track” later in this chapter for more information. obsolescence). Refer to “Format Track” later in this chapter for more information.

Sector Length and Cylinder (DCB Word 3)

DCB word 3 consists of two one-byte fields: the sector length and cylinder.

Sector Length

The sector length field specifies the length of the sectors on the diskette. The field must contain one of the following binary values:

- 0000 0000 for 128-byte sectors
- 0001 0000 for 256-byte sectors
- 0010 0000 for 512-byte sectors
- 1111 0000 format track defective

The sector length field corresponds to the N-byte in the sector ID on the diskette. It is part of the search argument used to locate the required sector.

Cylinder

The cylinder field contains a right-adjusted binary number from 01–76 that indicates the number of the cylinder containing the desired sector. If the number specified does not fall within the acceptable range (00–76), the operation ends immediately with an exception condition code and a DCB specification check is indicated in the ISB at interrupt presentation time.

The cylinder field corresponds to the C-field in the sector ID on the diskette. It is used as part of the search argument to locate the required sector. On Format Track operations, the cylinder specified in this field is written as part of the track sector IDs.

Head Selection and Sector Number (DCB Word 4)

DCB word 4 consists of two one-byte fields: head selection and sector number.

Head Selection

The head selection byte specifies which head is to be used to access the data. Specify 0000 0000 for head 0; specify 0000 0001 for head 1 (bits 0–6 should be set to zeros to avoid future code obsolescence). Specifying any other value will result in a ‘no record found’ response to all operations except Read Sector ID.

The head selection byte corresponds to the H-byte in the sector ID on the diskette. It is part of the search argument used to locate the required sector.

The head selection byte is used during a Seek operation to specify the head to be used for all succeeding data transfer operations; the head selected can be changed only by performing another seek. Seek Recalibrate operations automatically select head 0 but are not normally used to change head selection.

Sector Number

The sector number field contains the number of the specific sector to be accessed. The range of valid values depends on the sector length specified in the first byte of DCB word 3. The valid values for sector length and sector number are:

<i>Contents of sector length field (binary)</i>	<i>Sector length</i>	<i>Possible values for sector number field (binary)</i>	<i>Decimal equivalents</i>
0000 0000	128 bytes	0000 0001 0001 1010	01–26
0001 0000	256 bytes	0000 0001 0000 1111	01–15
0010 0000	512 bytes	0000 0001 0000 1000	01–08

If the value stored in the sector number byte of DCB word 4 exceeds the acceptable range for the sector length indicated in the sector length field of DCB word 3, the operation ends immediately and an interrupt request is sent to the processor. An exception condition code (CC=2) and a DCB specification check are transferred to the processor at interrupt presentation time.

The sector number field corresponds to the R-byte in the sector ID on the diskette. It is part of the search argument used to locate the required sector.

Chain Address (DCB Word 5)

To chain operations together, set the chaining flag bit in the DCB control word (DCB word 0) to 1. The address of the next DCB in the chain must also be specified in DCB word 5. The address must be an even number. If the chained-to address is an odd number (bit 15 is on), the operation ends immediately and an interrupt request is sent to the processor. An exception condition code (CC=2) and a DCB specification check are transferred to the processor at interrupt presentation time.

Byte Count (DCB Word 6)

The byte count specifies the number of bytes to be transferred to or from main storage. The byte count must be an even number for all data transfer operations. If bit 15 is set on (indicating an odd byte count), the operation ends immediately, data is not transferred, and an interrupt is requested. An exception condition (CC=2) and a DCB specification check in the ISB are transferred to the processor at interrupt presentation time.

The Start Cycle Steal Status command requires a byte count of either X'0004' or X'0008'; the Read Sector ID operation requires a byte count of X'0004'. Other data transfer operations (Write Data/Data AM, Write Data/Control AM, Read Data, or Read Verify) require a byte count that indicates the length of the record to be transferred. The byte count is used in conjunction with the sector length (N-byte in DCB word 3) to determine the number of sectors required for the record. For example, if a 134-byte record is to be written, the byte count must contain X'0086'. If the diskette is formatted into 128-byte sectors, the N-byte in DCB word 3 would be zero. The diskette unit would write 128 bytes of the record into the

sector identified in the sector ID search argument; the last 6 bytes would be written in the next logical sector, and the remainder of the sector would be padded with binary zeros. When the record is subsequently read, the padded zeros are included in the data field CRC verification. Only the number of data bytes specified in the DCB byte count, however, are transferred into processor storage.

Data Address (DCB Word 7)

This word contains the beginning address of the processor storage location used in the data transfer. During a read operation, the first word read from the diskette is stored in this location; data is transferred to succeeding storage locations until the byte count has been fulfilled. During a write operation, the word stored at this location is written in the first word position of the specified sector; until the byte count reaches zero, words from succeeding processor storage locations are transferred to the sector location specified in the DCB.

The data address stored in this word must identify a storage location that is on an even address boundary. If the data address is odd (bit 15 is set to 1), the operation ends and an interrupt is requested. At interrupt presentation time, a DCB specification check is transferred to the processor. Refer to "Interrupts" later in this chapter.

DCB Command Chaining

Obtaining a new DCB upon completion of the operation specified in the current DCB without issuing a new Operate I/O instruction is called DCB command chaining. The DCBs belonging to such a sequence are said to be chained.

When DCBs are chained, the first DCB in the chain contains the address of the next DCB. As each operation in a chained sequence is completed, the chain address in the current DCB is used to cycle steal the next DCB in the chain. The chained-to DCB is examined to determine the next operation in the sequence and whether the device parameters associated with it are valid. DCB command chaining operations continue until a DCB is fetched that has the chain bit in the control word (DCB word 0) set to 0, indicating the last operation in the chain. If an error occurs, chaining to succeeding DCBs is automatically suspended, and an interrupt request is sent to the processor. Normally, an interrupt request is not sent to the processor until the diskette unit has completed the last operation in the chain.

DCB command chaining reduces the processing time required to execute I/O operations to the diskette unit. For example; a single Operate I/O instruction, can:

- seek to a new cylinder location and change head selection
- write a record
- verify that the record was written properly
- seek to a new cylinder location and change head selection
- read a record, etc.

Start Command

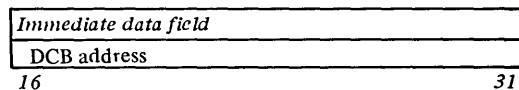
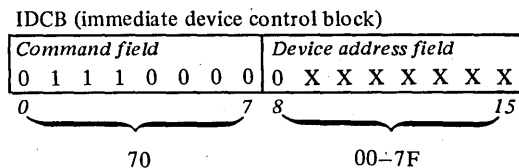
Start commands initiate I/O diskette operations that transfer data to or from processor storage in cycle steal mode. An interrupt request is sent to the processor when the I/O operation ends. An Operate I/O instruction must point to an IDCB containing each Start command and the IDCB immediate field must contain the address of a DCB. The control information and parameters for a particular diskette operation must be stored in the DCB associated with that operation. Refer to "Using the DCB" earlier in this chapter. The diskette operations initiated with a Start command are:

- Seek
- Seek Recalibrate
- Write Data/Data AM
- Write Data/Control AM
- Read Data
- Read Verify
- Read Sector ID
- Format Track

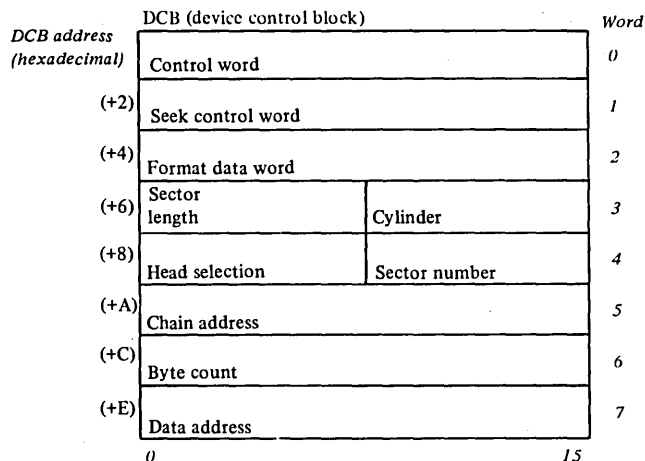
Note. Refer to the description of each individual diskette operation for the format of each DCB control word and for programming considerations applicable to each operation.

When the Operate I/O instruction is issued, the Start command is transferred under direct program control from the IDCB to the diskette attachment, where it is checked for errors and validity. If the command is accepted, a 'satisfactory' condition code (CC=7) is sent to the processor. While the diskette unit is 'busy' executing the I/O operation, the processor continues with other operations. Beginning at the DCB address specified in the IDCB, the eight words in the DCB are transferred to the diskette unit. The data is transferred in cycle steal mode one word at a time. The DCB information is decoded and the diskette unit begins executing the operation called for in the DCB control word (DCB word 0). When the operation (or operations when chaining) ends, an interrupt request is sent to the processor. At interrupt presentation time, a condition code and interrupt ID word containing status information are presented to the processor.

The format of the IDCB for a Start command is:



The format of the DCB for a Start command is:



Programming Considerations

1. A Seek operation must precede every diskette operation that requires a change in either head selection or cylinder location.
2. When DCB command chaining is used to perform a series of diskette operations, an interrupt is not requested until either an error occurs or the last operation in the chained sequence is complete.
3. To specify DCB command chaining:
 - a. For every operation in a DCB command-chained-sequence, except the last, set the chaining flag in each DCB control word (DCB word 0) to 1.
 - b. Set the address of the chained-to DCB in the chain address (DCB word 5).
4. For every I/O operation initiated with a Start command that is not included in a DCB command-chaining sequence, store (in processor storage):
 - a. an Operate I/O instruction that points to an IDCB
 - b. a Start command with a device address and a DCB address in an IDCB
 - c. a DCB that contains device parameters and control information defining a particular diskette operation
5. The diskette unit responds 'busy' to all commands except Prepare, Device Reset, Read ID, or Halt I/O from the time the Start command is received until an interrupt request is serviced by the processor.

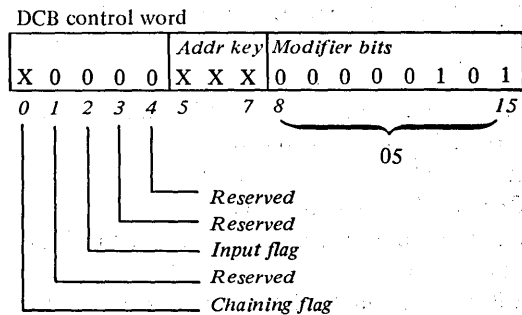
Seek Operation

A Seek operation must precede every I/O operation requiring a move of the heads to another cylinder or a change in head selection. The Seek operation can be used to change: head selection, only; cylinder location, only; or both head selection and cylinder location. The DCB associated with a Seek operation is transferred to or from processor storage in cycle steal mode. An interrupt request is sent to the processor when the diskette unit completes the operation. A condition code and interrupt ID word are transferred to the processor when the interrupt request is serviced. Refer to "Interrupts" and "Condition Codes" later in this chapter.

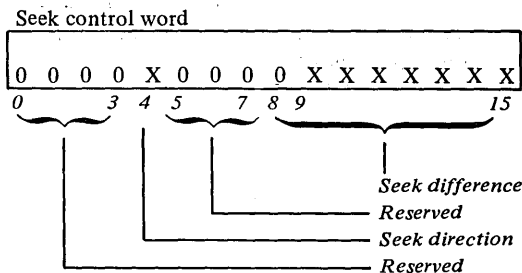
The control information and parameters required for a Seek operation must be stored in a DCB. The DCB must contain:

- a DCB control word defining a Seek operation to the diskette unit (DCB word 0).
- a seek control word that specifies the seek direction and number of cylinders to be crossed (DCB word 1).
- a head select byte that specifies which head is to be used (high-order byte of DCB word 4).
- a chain address if DCB command chaining is specified in the DCB control word.
- zeros in unused DCB fields.

The format of the DCB control word for a Seek operation is:



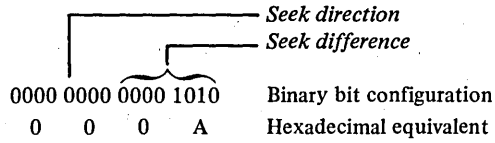
The format of the seek control word (DCB word 1) is:



Set the seek direction bit (bit 4) to 0 to increase the cylinder number; set the bit to 1 to decrease the cylinder number. Set the eight bits in the seek difference field to specify the number of cylinders the heads must cross to reach the desired cylinder. Set all other bits to zeros.

Example:

To start from cylinder 10 and seek to cylinder 20, the seek control word would be:



For every Seek operation, the head used to access data must be specified in the head selection field of DCB word 4. Specify binary 0000 0000 for head 0 and 0000 0001 for head 1. Bits 0-6 should be set to zero to avoid future code obsolescence. Specifying any other value results in a *no record found* response.

Programming Considerations

1. To change head selection without moving the heads, specify a seek control word of zero and indicate the desired head in the head selection field (the high-order byte of DCB word 4).
2. If a value outside the valid cylinder range (00 through 76) is set in the seek control word, the heads will not necessarily stop at cylinder 00 or cylinder 76. The access mechanism might stop anywhere, even between tracks. In either case, a failure is not detected until a subsequent data transfer operation fails to locate the required sector.

3. The time required to perform a Seek operation can be calculated with the following formula:

$$5N + 35 \text{ milliseconds (head settling time)}$$

where:

N = the number of cylinders the head must move

Seek Recalibrate Operation

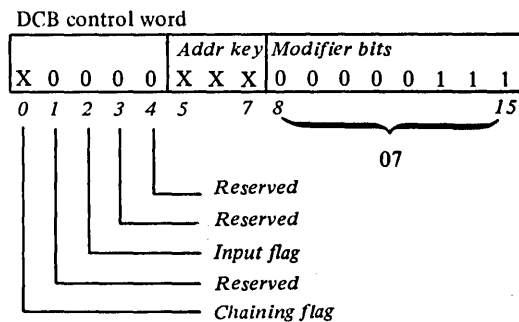
The Seek Recalibrate operation automatically moves the access mechanism to cylinder 00 and selects head 0. Because a Seek Recalibrate operation requires 0.41 seconds to execute, it should only be used in error recovery or initialization routines. During a Seek Recalibrate operation, no data is transferred to or from processor storage in cycle steal mode. An interrupt request is sent to the processor when the diskette unit completes the operation. When the processor services the interrupt request, a condition code and an interrupt ID word are transferred to the processor. Refer to "Interrupts" and "Condition Codes" later in this chapter.

The control information and parameters required for a Seek Recalibrate operation must be stored in a DCB. The DCB must contain:

- A DCB control word that defines a Seek Recalibrate operation to the diskette unit (DCB word 0).
- A chain address in DCB word 5 if DCB command chaining is specified in the DCB control word for this operation. Refer to "DCB Command Chaining" earlier in this chapter.

Although the data in the DCB seek control word (DCB word 1) is not needed for this operation, it is checked for proper parity. All unused DCB words and fields must be set to zero.

The format of the DCB control word for a Seek Recalibrate operation is:

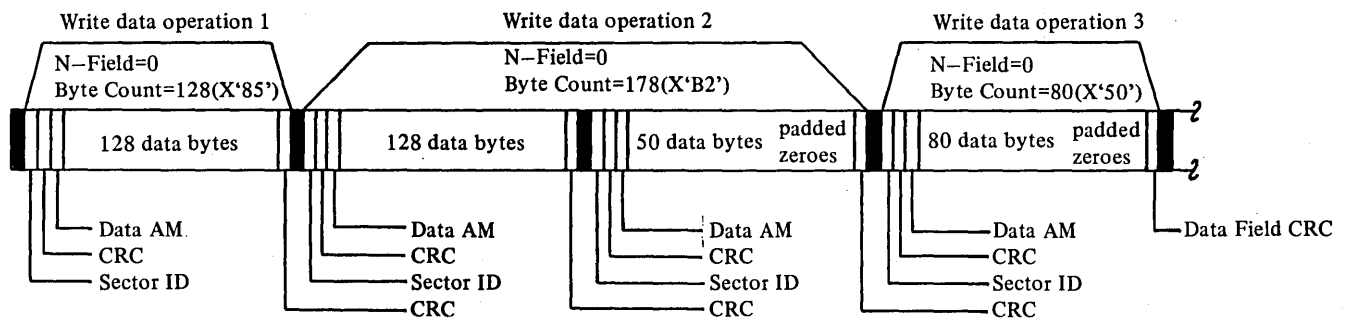


Write Data/Data AM Operation

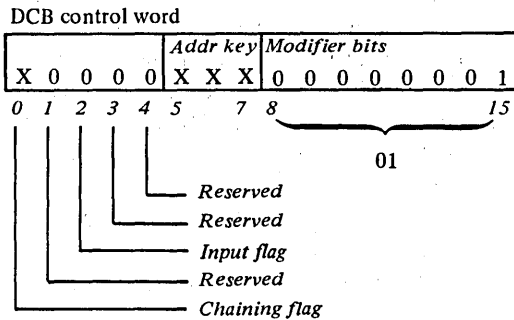
The Write Data/Data AM operation transfers a data record from contiguous processor storage locations to one or more sectors on the diskette. When the diskette unit executes a Write Data/Data AM operation, data from the storage location specified in the DCB is transferred in cycle steal mode to the location on the diskette specified by the search argument in the DCB. The diskette unit automatically writes a data address marker (AM) preceding the data in each sector written. A data AM indicates that the sector contains data. To write a sector of control information, refer to "Write Data/Control AM Operation" in the next section.

If the sector being written is not a full sector, the diskette unit writes the data bytes, then pads the sector to the end with zeros. The number of data bytes written is determined from the byte count stored in the DCB (DCB word 6). Records longer than one sector are written over as many sectors as required to satisfy the byte count.

The DCB for a Write Data/Data AM operation must contain: a control word, sector ID search argument (sector length, cylinder, head selection, sector number), byte count, and data address. Set the chaining flag in DCB word 0 to 1 and specify a chain address in DCB word 5 when command chaining to another DCB. Set unused DCB words and fields to zero.



The format of the DCB control word for a Write Data/Data AM operation is:



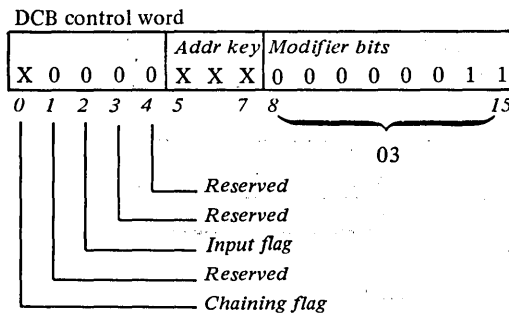
Programming Considerations

1. If the sector ID specified in the search argument cannot be located after at least one rotation of the diskette, or if a sector ID error is detected, the operation ends immediately and an interrupt request is sent to the processor. An exception condition code (CC=2) and an interrupt ID word containing status information are transferred to the processor when the interrupt request is serviced.
2. The data field of a sector is not written if an error is detected in the sector ID. The file data check bit (bit 07 in cycle steal status word 1) is set to 1 if the sector ID contains a CRC error. The sector ID being search for could be in cycle steal status words 2 and 3 (refer to "Cycle Steal Status Words 2 and 3" later in this chapter). Progress on a multiple sector transfer prior to detection of the invalid sector ID can be determined from the residual address in cycle steal status word 0. All data fields up to the invalid sector ID will have been written.
3. All Write Data operations *should be followed immediately* by a Read Verify operation to validate the data. Refer to "Read Verify Operation" later in this chapter.
4. If a Write Data operation is attempted with the DCB command chaining bit set to 0 and a DCB byte count of zero, the operation ends after the DCB is fetched, and an interrupt request is sent to the processor. A device end condition code (CC=3) and an interrupt ID word containing accumulated status are transferred to the processor when the interrupt request is serviced.
5. The sector length specified in the DCB must be consistent with the length of the sectors on the diskette. For 128-byte sectors specify X'00'; for 256-byte sectors, X'10'; and for 512-byte sectors, X'20'.
6. A Seek operation must precede every Write Data/Data AM operation that requires a move of the heads to another cylinder or a change in head selection.

Write Data/Control AM Operation

The Write Data/Control AM operation is similar to the Write Data/Data AM operation. The only difference between the two operations is the address marker that is written in the byte immediately preceding each sector data field. The Write Data/Control AM operation automatically writes X'F8' in the AM2 byte, which indicates that the data field contains control information. Refer to "Write Data/Data AM" for operating details and programming considerations.

The format of the DCB control word for a Write Data/Control AM is:

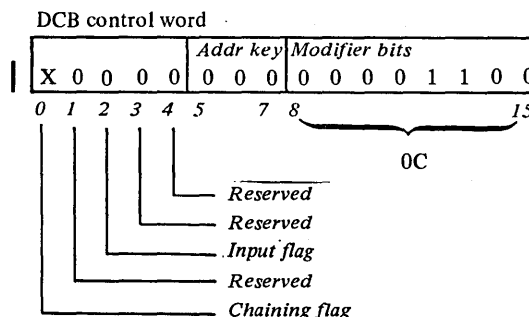


Read Verify Operation

The Read Verify operation should be used after each write data to validate the previously-written data. The operation is similar to the Read Data operation. Each specified sector is read completely and the Cyclic Redundancy Check (CRC) bytes are checked to verify the data; however, data from the diskette is not transferred to processor storage. When the operation ends, an interrupt request is sent to the processor.

With the exception of the control word (DCB word 0), the fields of the DCB for a Read Verify operation should be the same as those for the previous write operation. The required DCB fields are: control word, sector ID search argument (sector length, cylinder, head selection, sector number), byte count, and data address. Set the chaining flag in DCB word 0 to 1 and specify the chain address in DCB word 5 when command chaining to another DCB. Set unused DCB words and fields to zero.

The format of the DCB control word for a Read Verify operation is:



Programming Considerations

1. If the CRC check results in an 'unequal' compare:
 - a. an exception condition code (CC=2) is posted
 - b. status information is set in the cycle steal status words
 - c. the status available bit (bit 0) in the ISB is set to 1
 - d. an interrupt request is sent to the processor.
 Issue a Start Cycle Steal Status command, described later in this chapter, to determine the cause of the error.
2. If the byte count in the DCB is zero; the operation ends immediately, the DCB specification check bit in the ISB is set to 1, and an interrupt request is sent to the processor.
3. Read Verify operations do not check for the presence of control address markers.

Read Data Operation

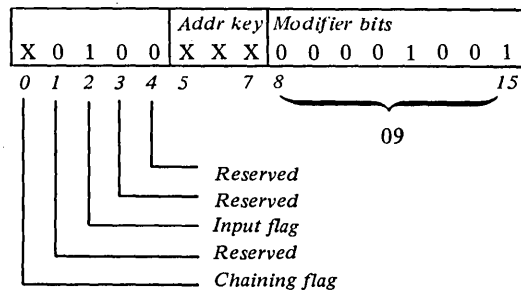
The Read Data operation retrieves a data record stored in one or more sectors on the diskette and transfers the data into contiguous processor storage locations, beginning at the data address specified in the DCB. The Read Data operation transfers data in cycle steal mode and an interrupt request is sent to the processor when the operation ends.

When the diskette unit performs the Read Data operation, the head selected with a previous Seek operation begins immediately to read the diskette surface for the sector ID specified by the search argument in the DCB. When the sector is located, the data field information is transferred into storage in cycle steal mode. The data is verified by recalculating the CRC bytes for the data field as the data is read from the diskette and comparing the result with the previously written data field CRC bytes. Although the sector being read may not be completely filled with data (padded zeros added), the diskette unit must read to the end of the sector to verify the CRC bytes. Only those bytes specified by the DCB byte count, however, are transferred into storage.

The DCB for a Read Data operation must contain: a DCB control word, sector ID search argument (sector length, cylinder address, head selection, sector number), byte count, and data address. Set the chaining flag in DCB word 0 to 1 and specify a chain address in DCB word 5 when command chaining to another DCB. Set unused DCB words and fields to zero.

The format of the DCB control word for a Read Data operation is:

Control word format (DCB word 0)



Programming Considerations

1. If a sector ID matching the search argument is not located after one rotation of the diskette, or if a sector ID error is detected, the operation ends immediately, and an interrupt request is sent to the processor. An exception condition code and interrupt ID word containing status information are transferred to the processor when the interrupt is serviced.
2. A multiple sector read cannot continue beyond a sector containing a control address marker (AM). When a control AM is detected, the diskette unit reads data until the end of the sector containing the control AM, ends the operation, and requests an interrupt.
3. A Seek operation must precede every Read Data operation that requires a move of the heads to another cylinder or a change in head selection.

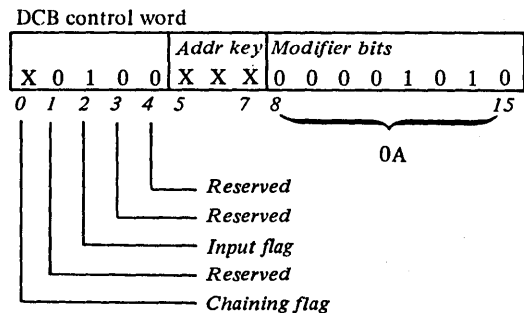
Read Sector ID Operation

The Read Sector ID operation is normally used to determine which head is selected and on which track the head is located. After determining from the DCB control word (DCB word 0) that a Read Sector ID operation is called for, the diskette unit immediately begins to read data from the track under the selected head. The first sector ID detected is loaded into a search argument register. The register contents (the N, C, H, and R-fields) are transferred via cycle steal into processor storage beginning at the data address specified in the DCB.

Note. The high order bits (0-3) and low order bits (4-7) of the N-byte are interchanged before they are stored.

When the diskette unit successfully completes the operation, an interrupt request is sent to the processor. A device end condition code is transferred to the processor when the interrupt request is serviced.

The format of the DCB control word for a Read Sector ID operation is:



Programming Considerations

If a DCB byte count containing any value other than X'0004' is detected:

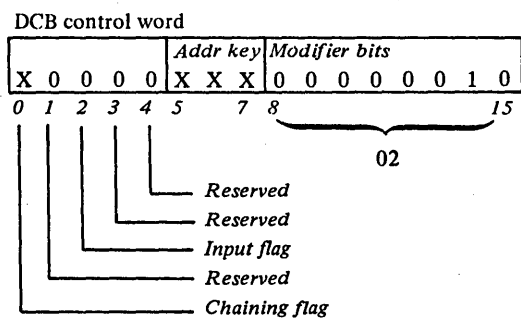
- the Read Sector ID operation ends immediately
- an exception condition (CC=2) is posted
- an interrupt request is sent to the processor.

An exception condition code and an interrupt ID word containing a DCB specification check are transferred to the processor when the interrupt request is serviced.

Format Track Operation

The Format Track operation is normally used to initialize a track on the diskette into twenty-six 128-byte sectors, fifteen 256-byte sectors, or eight 512-byte sectors. The Format Track operation can also be used to identify a defective track by initializing the sector IDs with a unique data pattern. When 1111 0000 is specified in the DCB N-field, the specified diskette track is automatically initialized with 128-byte sectors containing *one-bits* in every sector ID on the track.

The format of the DCB control word for a Format Track operation is:



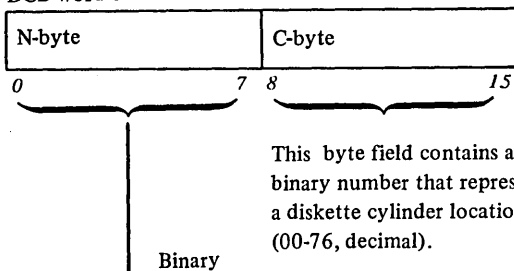
X= determined by program requirements

The DCB for a Format Track operation must contain: a DCB control word, a format data word, and a sector length and cylinder designation (DCB word 3).

Set the chaining flag in DCB word 0 to 1 and specify a chain address in DCB word 5 when chaining to another DCB. Set unused DCB words and fields to zero.

Store the data to be repeated for every word, on every record, on the track in the DCB format data word. The C-byte in DCB word 3 must contain the cylinder address of the track. The C-byte value is written in the sector ID of each sector formatted on the track. The C-byte value is checked for validity: it must be a binary number equal to 00 through 76 (decimal). The N-byte in DCB word 3 specifies the intended size of every sector on the diskette track. The N-byte must contain 0000 0000 for 128-byte sectors, 0001 0000 for 256-byte sectors, 0010 0000 for 512-byte sectors, or 1111 0000 for defective sectors. If X'F0' is specified in the N-byte, the track is initialized with 128-byte sectors containing *one bits* in every sector ID on the track.

DCB word 3



0000 0000=128-byte sectors
0001 0000=256-byte sectors
0010 0000=512-byte sectors
1111 0000=Defective

Note. Set bits 4-7 to zeros to avoid future code obsolescence.

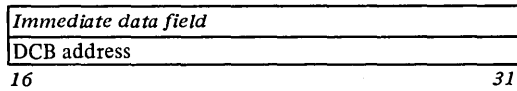
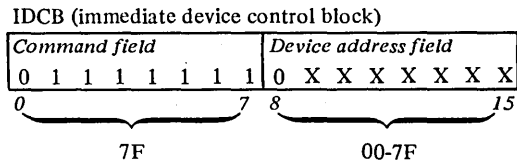
Programming Considerations

1. Every Format Track operation to the diskette unit must be preceded by a Seek operation if a change in cylinder location or head selection is required.
2. A Read Sector ID operation can be used to check the cylinder location of the heads before each Format Track operation is executed. The C-byte value in DCB word 3 must specify the logical address of the track to be formatted.
3. If an invalid N-field is detected in the DCB associated with a Format Track operation, the operation ends immediately after the DCB transfer is complete and an interrupt request is sent to the processor. A DCB specification check (bit 3) is set in the ISB and transferred to the processor with an exception condition code when the interrupt request is serviced. The N-byte must contain either 0000 0000, 0001 0000, 00010 0000, or 1111 0000. (Bits 4-7 must be set to zeros to avoid future code obsolescence.)

Start Cycle Steal Status Command

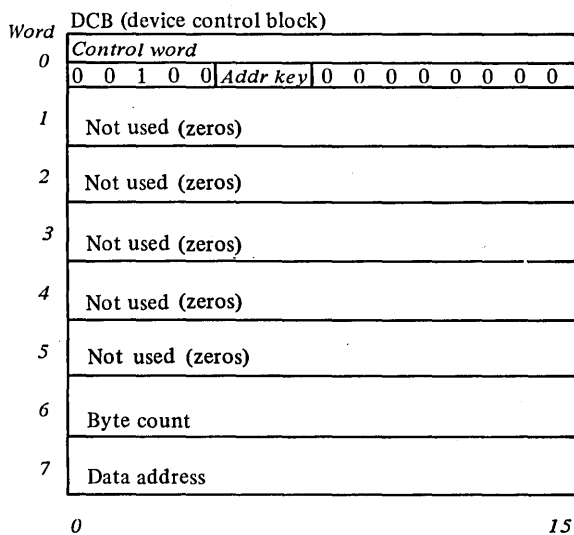
The Start Cycle Steal Status (SCSS) command transfers two or four words of status information into processor storage beginning at the data address location specified in the DCB. This information is available when the status available bit is set to 1 in the ISB at interrupt presentation time; the information can determine why the preceding I/O operation failed. Refer to "Status Information" later in this chapter. The SCSS command transfers data in cycle steal mode and causes an interrupt when command execution is complete.

The SCSS command requires an Operate I/O instruction with the address of an IDCB, and IDCB with the address of a DCB, and a DCB. The format of the IDCB is:



The DCB for a SCSS command must contain: a DCB control word, a byte count (must be set to either X'0004' or X'0008'), and a data address. The data address specifies the beginning storage location into which the two or four words of status information are to be transferred. The SCSS command *cannot* be included in a DCB command chaining operation. Set the chaining flag in the DCB control word to 0. Set unused DCB words and fields to zero.

The format of the DCB for the SCSS command is:



Programming Considerations

1. The Start Cycle Steal Status command *cannot* be included in DCB command chaining operations. The SCSS command does not support chaining.
2. The *no data field found bit* (bit 01) in SCSS word 1 can be caused by a diskette surface defect or a poorly written record.
3. If the *file not ready bit* (bit 04) in SCSS word 1 is set to 1: a diskette has not been inserted in the diskette unit, the diskette has been inserted improperly, or the access door has been left open. Bit 04 can be set to 1 by other means, but check the above before contacting maintenance personnel.
4. If the *no record found bit* (bit 05) is set to 1 after a Write Data, Read Verify, or Read Data operation; suspect a seek error, track defect, poorly written track, or an invalid search argument.
5. If the *file data check bit* (bit 07) is set to 1 after a Read Sector ID operation, the search argument in the DCB might be invalid. The operation should be repeated.
6. If the *file data check bit* (bit 07) in SCSS word 1 is set to 1 after a Read Data or Read Verify operation, the invalid field can be either the sector ID or the data field. The sector ID is invalid if the no record found bit (bit 05) in SCSS word 1 is set to 1. The data field is invalid if the no record found bit is set to 0. If the sector ID caused the error and the operation involved multiple sectors, any data transferred before the error occurred is valid. Refer to the residual address in SCSS word 0 to determine the address of the last data word successfully transferred into processor storage. The most previous sector transferred into storage may contain invalid data.
7. If the *file data check bit* (bit 07) in SCSS word 1 is set to 1 after a Write Data operation, the diskette unit detected an invalid sector ID. The data field associated with the invalid sector ID is not written. If the operation involved multiple sectors, refer to the residual address in SCSS word 0 to determine the address of the last data word successfully transferred to the diskette surface. All data fields up to the invalid sector will have been written.
8. The diskette unit responds 'busy' to all commands except Read Device ID, Prepare, Device Reset or Halt I/O from the time it receives the Start Cycle Steal Status command until an interrupt request is serviced by the processor.

9. If the *index pulse at incorrect time bit* (bit 08) in SCSS word 1 is set to 1 after a Read Data or Read Verify operation, an index pulse was detected between the sector ID and the associated data field.
10. If the *index pulse at incorrect time bit* (bit 08) in SCSS word 1 is set to 1 after a Format Track operation, an index pulse was detected before the track initialization operation ended. Suspect a file speed error.

Status Information

Three types of status information (see Figure 4-9) inform the processor of the results of input/output operations:

- conditions codes
- interrupt ID word
- cycle steal status words

Condition Codes

Condition codes are reported after execution of each Operate I/O instruction. See Figure 4-8. For commands that do not cause interrupts, the condition code reported after the Operate I/O instruction executes is the only status information available. The appropriate condition code is transferred into the *even*, *carry*, and *overflow* bit positions of the Level Status Register (LSR) in the processor. (Refer to "Prerequisite Publications" in the Preface of this manual for order numbers of IBM Series/1 processor unit description manuals.)

Command	Condition Code (CC) Values							
	CC0	CC1	CC2	CC3	CC4	CC5	CC6	CC7
Prepare	X					X		X
Device reset	X							X
Read device ID	X	X	X			X		X
Start	X	X	X			X		X
Start cycle steal status	X	X	X			X		X

CC Value	Meaning
0	Device not attached
1	Busy
2	Busy after reset
3	Not reported
4	Not reported
5	Interface data check
6	Not reported
7	Satisfactory

Note. Condition code zero (CC = 0) is reported if the diskette unit is not attached to the channel or power is off the unit.

Figure 4-8. Condition code responses to Operate I/O instructions

When commands and changing states within the diskette attachment cause interrupts, a condition code is also transferred into the processor LSR at interrupt presentation time. The condition code values that can be reported at interrupt presentation time are:

CC value	Meaning
0	Not reported
1	Not reported
2	Exception
3	Device end (satisfactory)
4	Attention
5	Not reported
6	Not reported
7	Not reported

For condition code 2, a second level of status is available in the Interrupt Status Byte (ISB) of the interrupt ID word. For condition code 3, the Interrupt Information Byte (IIB) contains zeros. Refer to "Interrupt ID Word." For condition code 4, the IIB indicates whether a one-sided diskette (X'80') or a two-sided diskette (X'00') is inserted in the unit.

Note. Hardware processing of an interrupt includes automatic branching to a service routine. The processor uses a reserved area in storage for branch information. Refer to "Prerequisite Publications" in the Preface of this manual. Processor description manuals explain reserved storage and interrupt handling.

Interrupt ID Word

Interrupt status information is transferred to the processor in an interrupt ID word. The low-order byte of the interrupt ID word contains the address of the interrupting device: the high-order byte is an Interrupt Information Byte (IIB).

Interrupt ID word															
IIB								Device address							
X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X
0								7 8 15							

If commands that cause interrupts fail to end properly (CC=2), the IIB has a special format and is called the Interrupt Status Byte (ISB).

Interrupt Status Byte (ISB)

When an interrupt caused by an exception condition is serviced by the processor, the interrupt ID word containing the device address and interrupt status byte (ISB) is transferred to the processor. The ISB bit meanings are:

ISB

bit	Meaning
0	<i>Device status available.</i> Additional information about the operation is available when this bit is set to 1. The information is stored in cycle steal status word 1. To obtain the information, issue a Start Cycle Steal Status command. Refer to "Start Cycle Steal Status Command" earlier in this chapter.
1	<i>Delayed command reject.</i> This bit is set to 1 when an error in the Operate I/O instruction is detected. An invalid I/O command or an odd DCB address in the IDCBC can cause this kind of error.
2	<i>Not reported.</i> This bit is always set to 0.
3	<i>DCB Specification Check.</i> If this bit is set to 1, the diskette operation failed because of an invalid DCB parameter. Any of the eight words in the DCB associated with the diskette operation can set this bit to 1. The residual address stored in cycle steal status word 0 points to the DCB word containing the invalid parameter. To obtain the residual address, refer to "Start Cycle Steal Status Command" earlier in this chapter.
4	<i>Storage Data Check.</i> If data accessed from processor storage during a cycle steal output operation is out of parity, this bit is set to 1. A machine check condition does not occur, and the parity of the data in that storage location is not corrected.
5	<i>Invalid Storage Address.</i> If the storage address specified in the DCB is outside the capacity of processor storage, this bit is set to 1. This bit can be set to 1 during an input or output cycle steal operation. The operation ends immediately.
6	<i>Protect Check.</i> An attempt to transfer data into a processor storage location using an incorrect cycle steal address key, sets this bit to 1. The operation ends immediately.
7	<i>Interface Data Check.</i> If a parity error is detected at the interface, this bit is set to 1. The operation ends immediately.

Figure 4-9 summarizes the status information available in condition codes, in the ISB, and in the cycle steal status words.

Operate I/O Instruction Execution Time

<i>CC Value</i>	<i>Meaning</i>
0	Device not attached
1	Busy
2	Busy after reset
3	Not reported
4	Not reported
5	Interface data check
6	Not reported
7	Satisfactory

Interrupt Presentation Time

<i>CC Value</i>	<i>Meaning</i>
0	Not reported
1	Not reported
2	Exception
3	Device end (satisfactory)
4	Attention
5	Not reported
6	Not reported
7	Not reported

Interrupt Status Byte

<i>Bit Position</i>	<i>Meaning</i>
0	Device status available
1	Delayed command reject
2	Not reported
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Indicates more information in interrupt status byte (ISB)

Indicates more information in cycle steal status word 1

Issue a start cycle steal status command

Cycle Steal Status Word 1

<i>Bit Position</i>	<i>Meaning</i>
00	Not used
01	No data field found
02	Overrun
03	Control AM
04	File not ready
05	No record found
06	End of track
07	File data check
08	Incorrect index time
09	Invalid diskette surface
10	Not used
11	Not used
12	Not used
13	No erase current
14	No write gate
15	Erase current stuck on

Figure 4-9. Status information summary

Cycle Steal Status Information

If the diskette unit is not ready when a Start command is issued by the processor, or if the diskette unit drops 'ready', while executing an I/O operation initiated with a Start command, an interrupt request is sent to the processor. At interrupt presentation time, the status available bit in the ISB is set to 1 to indicate that additional status information is available. A Start Cycle Steal Status command can then be issued to obtain the status information.

Cycle Steal Status Word 0

This word contains the *residual address*; the processor storage location where the last cycle steal of data occurred. The residual address can be either the address of a word of data or the address of a word in the DCB. Execution of the SCSS command does not affect this address.

Cycle Steal Status Word 1

Each bit used in this word indicates a reason why the a normal end-of-operation response to the preceding I/O operation did occur. The bits have the following meanings:

Bit Position	Meaning
00	Not used
01	<i>No data field found.</i> This bit may be set by a Read Data or Read Verify operation. If the bit is set to 1, the diskette unit located the correct sector ID but did not find the associated data field.
02	<i>Overrun.</i> During cycle steal transfer operations a cycle steal request must be serviced by the processor within 48 microseconds or the overrun bit is set on. This condition arises when demands for I/O activity exceed the capability of the channel.
03	<i>Control address marker (AM).</i> This bit is set to 1 if, during a Read Data operation, a control AM is detected in front of a sector data field. The operation ends after the sector or portion thereof containing the control AM has been transferred into processor storage. <i>Note.</i> A check for the presence of control AMs does not occur during Read Verify Operations.
04	<i>File not ready.</i> If the diskette unit is not ready to execute or drops ready while executing a Seek, Seek Recalibrate, Write Data, Read Data, Read Verify, Read Sector ID, or Format Track operation, this bit is set to 1.
05	<i>No record found.</i> If, after at least one rotation of the diskette, a sector ID has not been found that compares 'equal' to the search argument sector ID in the DCB, this bit is set to 1. If this bit is set to 1 after a Read Sector ID operation, it means the diskette unit did not locate any sector IDs on the track (suspect an unformatted track).
06	<i>End of track.</i> If at least one but not all of the sectors in a multiple sector operation has been transferred and the end of the last logical sector on the track is detected, this bit is set to 1.

07	<i>File data check.</i> This bit is set to 1 if a data error is detected on the diskette. The CRC bytes, recorded at the end of every sector ID and data field, are used for error detection.
08	<i>Index pulse at incorrect time.</i> Refer to "Programming Considerations" that follow the SCSS command description.
09	<i>Invalid diskette side selected.</i> Two types of diskettes are available for use in the diskette unit: one type is designed for data storage on only one surface (one-sided diskette), and the other type is designed for data storage on both surfaces (two-sided diskette). If a one-sided diskette is inserted in the diskette unit, head 0 must be selected for all Seek operations. If head 1 is specified, the operation ends and the <i>invalid diskette side selected</i> bit is set to 1.
10--12	Not used
13	<i>No erase current.</i> If this bit is set to 1 after a Write Data (Data AM or Control AM) or Format Track operation, the data that was written over and the data written are probably not retrievable. Retry <i>one time only</i> and then call for maintenance.
14	<i>No write gate.</i> Same as bit 13.
15	<i>Erase current stuck on.</i> If this bit is set to 1 after any diskette operation, <i>retry one time only</i> and then call for maintenance.

Cycle Steal Status Words 2 and 3

SCSS words 2 and 3 contain the search argument used in the data field access operation that resulted in the interrupt. The N, C, H, and R-bytes returned in these two SCSS words point to the sector location that caused the error and ended the operation. The information is only useful if the preceding operation was a Write Data, Read Verify, or Read Data operation that failed because of a data field error. The information is especially useful if the I/O operation involved multiple sectors.

I/O Interrupts

The diskette unit can interrupt processing with two types of interrupts: end-of-operation and attention. Before an interrupt request can be presented to the processor, however, the diskette unit must be prepared to interrupt with the Prepare command described earlier in this chapter.

Note. Hardware processing of an interrupt includes automatic branching to a service routine. The processor uses a reserved area in processor storage for branch information. Refer to "Prerequisite Publications" in the Preface of this manual. Processor description manuals explain reserved storage and interrupt handling.

If the diskette unit is 'not ready' when a Start command is issued by the processor, or if the diskette unit drops 'ready', while executing an I/O operation initiated with a Start command, an interrupt request is sent to the processor. At interrupt presentation time, the status available bit in the ISB is set to 1 to indicate that additional status information is available. A Start Cycle Steal Status command can be issued to obtain the status information. Refer to "Start Cycle Status Command" earlier in this chapter.

End-of-Operation Interrupts

When an operation initiated by either of the interrupt-causing commands ends normally or is terminated by an error, an end-of-operation interrupt request is sent to the processor. The interrupt-causing commands are:

- Start
- Start Cycle Steal Status (SCSS)

Until the diskette unit completes an operation initiated by an interrupt-causing command, it responds 'busy' to all other such commands. However, the non-interrupting commands (Prepare, Device Reset, Read Device ID, or Halt I/O) are accepted and executed. The diskette unit reports a condition code when the Operate I/O instruction is executed and also when an interrupt request is serviced by the processor. The first condition code indicates whether the command has been accepted; the second condition code and an interrupt ID word are transferred to the processor at interrupt presentation time.

Attention Interrupt

An attention interrupt request is sent to the processor for only one reason; to notify the processor that the diskette unit is 'ready' (operational).

Attention interrupt requests are inhibited during Initial Program Load (IPL) operations. If the diskette unit is 'not ready' when an IPL operation is attempted, a 'wait' state exists until the diskette unit becomes ready and begins the IPL sequence. When the IPL operation ends, an end-of-operation request is sent to the processor. At interrupt presentation time, a device end condition is reported to the processor. If an attention interrupt request is pending when an IPL is initiated, the interrupt request is reset.

Note. An attention interrupt request is *not* sent to the processor when 'ready' *drops*.

Resets (Diskette)

Several methods of resetting controls and registers are available. The diskette unit remains 'busy' for 200 microseconds after every reset other than power-on reset.

Power-on Reset. Resets all controls and registers including the prepare register. In addition, head 0 is automatically selected, the residual address is reset to X'0001', and cycle steal status word 1 is reset to zero.

Note. The diskette unit remains 'busy' for 12 seconds after a power-on reset. This timeout should be taken into account especially when auto-IPL is used with the diskette unit.

System Reset. Resets all controls and registers except the prepare and residual address registers.

Initial Program Load (IPL). Resets the prepare register, last sector register, and cycle steal request.

Halt I/O Command. Resets all controls and registers except the prepare and residual address registers.

Device Reset Command. Resets all controls and registers except the prepare and residual address registers.

Initial Program Load (IPL)

An Initial Program Load (IPL) operation loads information from cylinder 00 on the head 0 side of the diskette into processor storage beginning at location 0000. The information initializes the processor with the program data required to begin operations. Initial program load operations are hardware initiated only.

An 'IPL select' signal from the processor to the diskette unit produces an automatic Seek Recalibrate operation which locates the head access mechanism at cylinder 00 with head 0 selected. Following the Seek Recalibrate operation, an automatic Read Data operation with a byte count of X'0100' (256 decimal) transfers data from the first two sectors following the index into processor storage in cycle steal mode. When the IPL sequence ends successfully, a device end condition code is presented to the processor on interrupt level 0 at interrupt presentation time. If the IPL operation fails, check that the diskette is inserted properly in the diskette unit and that the Power On/Off switch is in the *ON* position before attempting another IPL operation.

The 4964 Diskette Unit can be used as either a primary or alternate system IPL source.



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IBM Series/1
4962 Disk Storage Unit and
4964 Diskette Unit
Description

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This Technical Newsletter provides replacement pages for the subject publication. Pages to be inserted and/or removed are:

- iii, iv
- 2-1, 2-2
- 2-5, 2-6
- 3-5 through 3-8
- 3-8.1, 3-8.2 (added)
- 4-5, 4-6
- 4-9 through 4-12
- 4-17, 4-18
- X-1 through X-4

A technical change to the text or to an illustration is indicated by a vertical line to the left of the change.

Summary of Amendments

This technical newsletter:

- Adds information about alternate sector assignment for the 4962
- Incorporates miscellaneous technical changes

Note. Please file this cover letter at the back of the manual to provide a record of changes.



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**IBM Series/1
4962 Disk Storage Unit and
4964 Diskette Unit
Description**

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This Technical Newsletter provides replacement pages for the subject publication. Pages to be inserted and/or removed are:

iii, iv
1-1 through 1-4
2-1, 2-2
3-3, 3-4
3-7, 3-8
3-13 through 3-16
3-16.1, 3-16.2 (added)

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Summary of Amendments

The addition of information pertaining to Models 3 and 4 of the IBM 4962 Disk Storage Unit.

Note. Please file this cover letter at the back of the manual to provide a record of changes.

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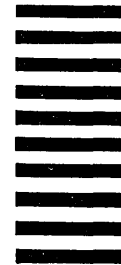
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