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AIR TRAINING COMMAND

STUDENT TEXT

ABR30533-1

CORE STORAGE

15 August 1966

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Computer Systems Department
KTTC, Mississippi

Student Text
Course ABR30533-1
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Student Text for AN/FSQ-7 & 8

Core Storage

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Core Storage Element

Introduction to Memory Element

A. Function of Memory

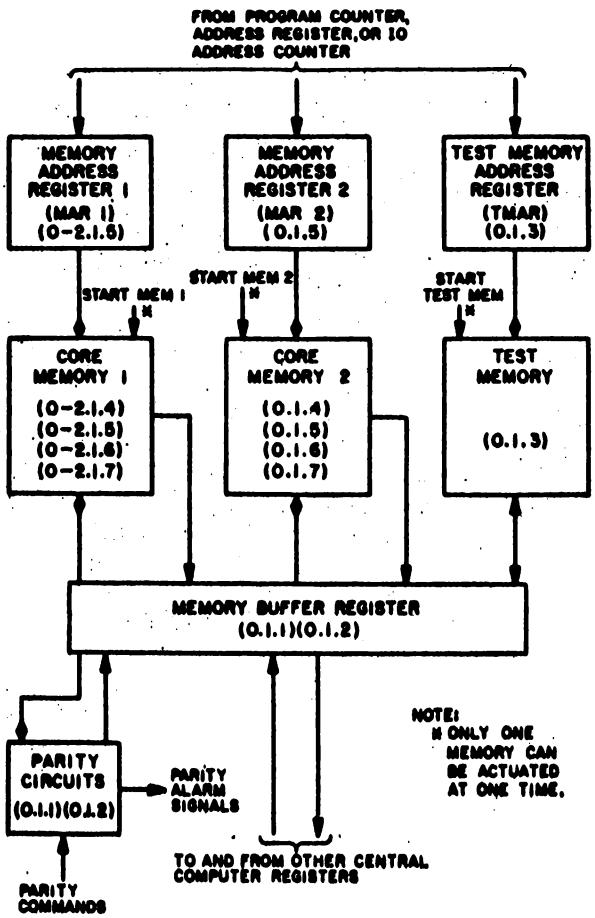
1. The memory element of the Central Computer is a computer-controlled, large-capacity, randon-access, high speed storage facility which provides for the semipermanent storage of all information (operating program, raw data, and processed results) required for or resulting from the normal operation of the Central Computer. The memory storage circuits do not differentiate between instruction words and data words (raw or processed). The memory "readout" cycle (equivalent to PT, OTa, and BO machine cycles) results in the transfer of a memory word out of a specific memory location; the memory "store" cycle (equivalent to OTB and BI machine cycles) results in clearing the specified memory location and storing the desired memory word in the cleared location. Each type of cycle requires 6.0 usec for execution.

B. Block Diagram Analysis

1. The three memory address registers are actually an integral part of the associated memory device since it is used to condition the internal address selection circuits within that memory. Each of the three memory devices is capable of storing different quantities of information; core memory 1 has a storage capacity of $65,536_{(10)}$ memory words, core memory 2 has a storage capacity of $4,096_{(10)}$ memory words, and test memory has an effective storage capacity of $16_{(10)}$ memory words. The storage medium used in each of the core memory devices is a 3-dimensional ferrite core array. Test memory storage is accomplished by the use of a manually wired control panel, two toggle switch registers, and a flip-flop register.

Refer to Page 0060

2. During computer operation, each memory cycle is initiated by the transfer of the desired memory address to the three memory address registers, and the subsequent application of a start-memory pulse to initiate the internal operations in the selected memory. Concurrently, the memory buffer registers are cleared to prepare them for the temporary storage of data to be transferred from either the selected memory location or from an external register, depending upon the type of cycle in process. During the execution of a memory "readout" cycle, the contents of the specified memory location are transferred to the memory buffer register approximately 3.0 usec after the cycle was initiated. The memory buffer register contents are then transferred to a specific computer register as directed by a computer command.



Memory Element, Block Diagram

Since the cores operate on the principle of destructive readout (the information contained in the selected core register is erased), the latter portion of the memory "readout" cycle is used to store the memory buffer contents back into the specified core memory location. During the execution of a memory "store" cycle, the first 3.0 usec are used to erase the contents of the specified memory location and to transfer the new word from one of the computer registers to the memory buffer register. During the latter portion of this memory cycle, the new information is stored in the cleared memory location.

3. The parity circuits associated with the memory buffer register provide a means of checking the accuracy of information transfer into and out of either of the core memory devices. During each memory "store" cycle, a parity bit is assigned to the memory word(33rd bit of memory word) before it is stored into the specified core memory location. During each memory readout cycle, the parity bit is checked to determine whether the initial transfer into and the present transfer out of the core memory was accurately accomplished. If the parity check shows that the memory word is in error, a parity-alarm signal is generated to inform the operating personnel of the malfunction.

4. The memory storage devices and the parity circuits operate independently of each other.

C. Memory Location Selection

1. By program counter during P. T. Time (except when "Branch FF" is set)
   By ADR Reg. during O. T. Time and during P. T. Time when "Branch FF" is set.
   By I/O Adr. Ctr. during BI or BO Time.

2. One of the above is sent to the three Memory Address Regs. which do the actual selecting of the specified address in memory.

D. Memory Address Assignment

1. AN/FSQ-7 256^2 & 64^2 Memory

   a. Memory Normal-Reverse Switch in Normal Position

      0.00000 - 1.77777 Memory I (256^2)
      2.00000 - 2.07777 Memory II (64^2)
      2.10000 - 3.77757 Memory II (64^2) will be selected
      3.77760 - 3.77777 Test Memory

b. Memory Normal-Reverse Switch in Reverse Position

0.00000 - 0.07777 Memory II (64^2)
0.10000 - 1.77777 Memory II (64^2) will be selected
2.00000 - 3.77757 Memory I(256^2)
3.77760 - 3.77777 Test Memory

2. 2. AN/FSQ-8 Two 64^2 Memories

a. Memory Normal-Reverse Switch in Normal Position

0.00000 - 0,07777 Memory I
0.10000 - 0.17777 Memory II
0.20000 - 0.20017 Test Memory
0.20020 - 0.37777 Test Memory will be selected

b. Memory Normal-Reverse Switch in Reverse Position

0.00000 - 0.07777 Memory II
0.10000 - 0.17777 Memory I
0.20000 - 0.20017 Test Memory
0.20020 - 0.37777 Test Memory will be selected

c. Clock and Abnormal Selections

0.60000 - 0.77777 Clock Reg.
1.00000 - 1.07777 Memory I
1.10000 - 1.17777 Memory II
1.20000 - 1.37777 Test Memory
1.40000 - 1.47777 Memory I
1.50000 - 1.57777 Memory II
1.60000 - 1.67777 Clock Reg.
1.70000 - 1.77777 Clock Reg. if CAC, Test Memory if not CAC.

E. Physical Description

1. AN-FSQ-7

a. One 256^2 Memory and one 64^2 Memory for each computer.

b. 256^2 Memory
Units 65, 66 and 67

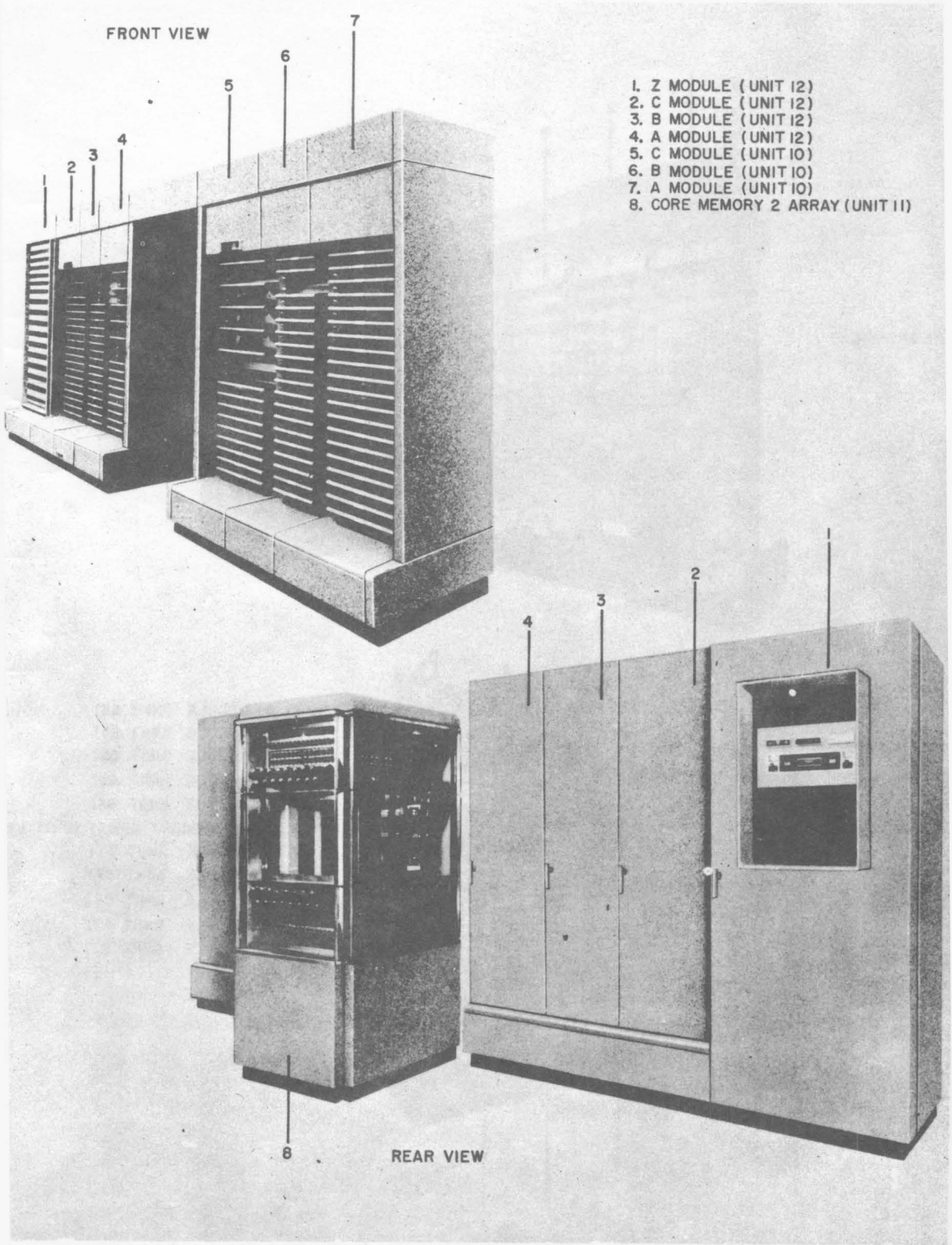
Refer to Page 0097

c. 64^2 Memory
Units 10, 11, and 12

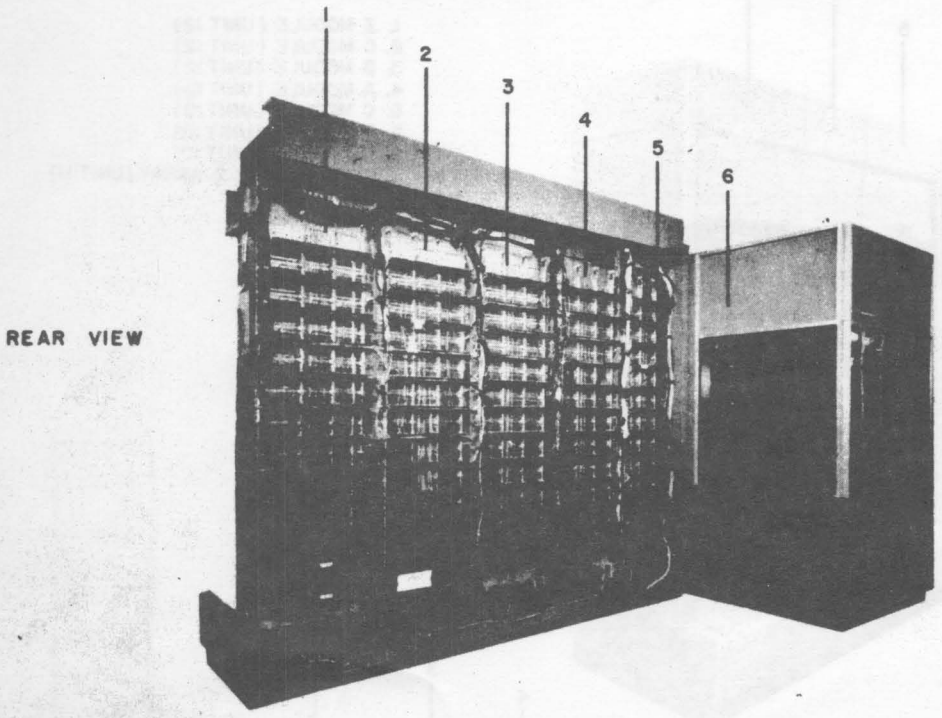
2. AN-FSQ-8

a. Two 64^2 Memories

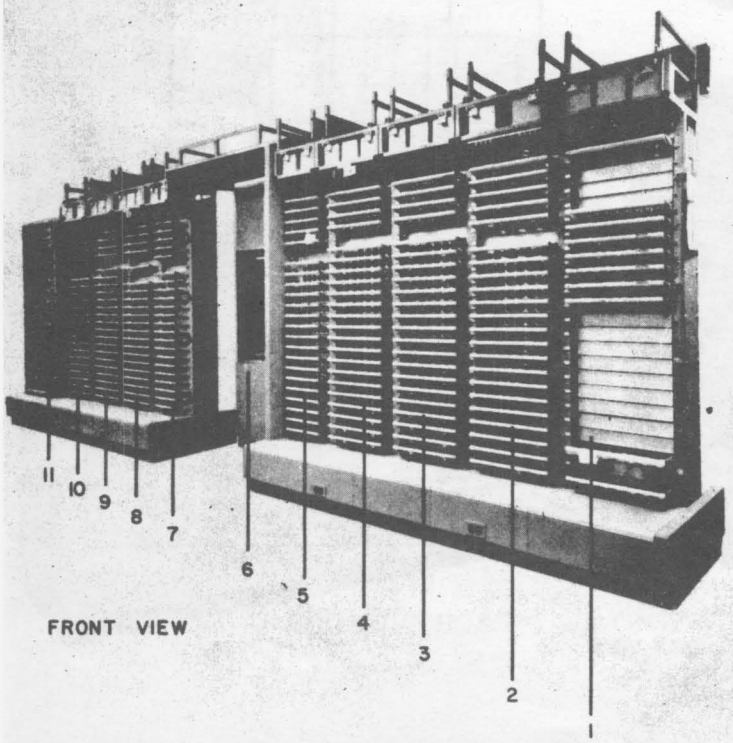
b. Units 7, 8 and 9 (64^2 Mem.) are used instead of Units 65, 66 and 67 (256^2 Mem.)



Core Memory 2 Units (Units 10, 11, and 12)



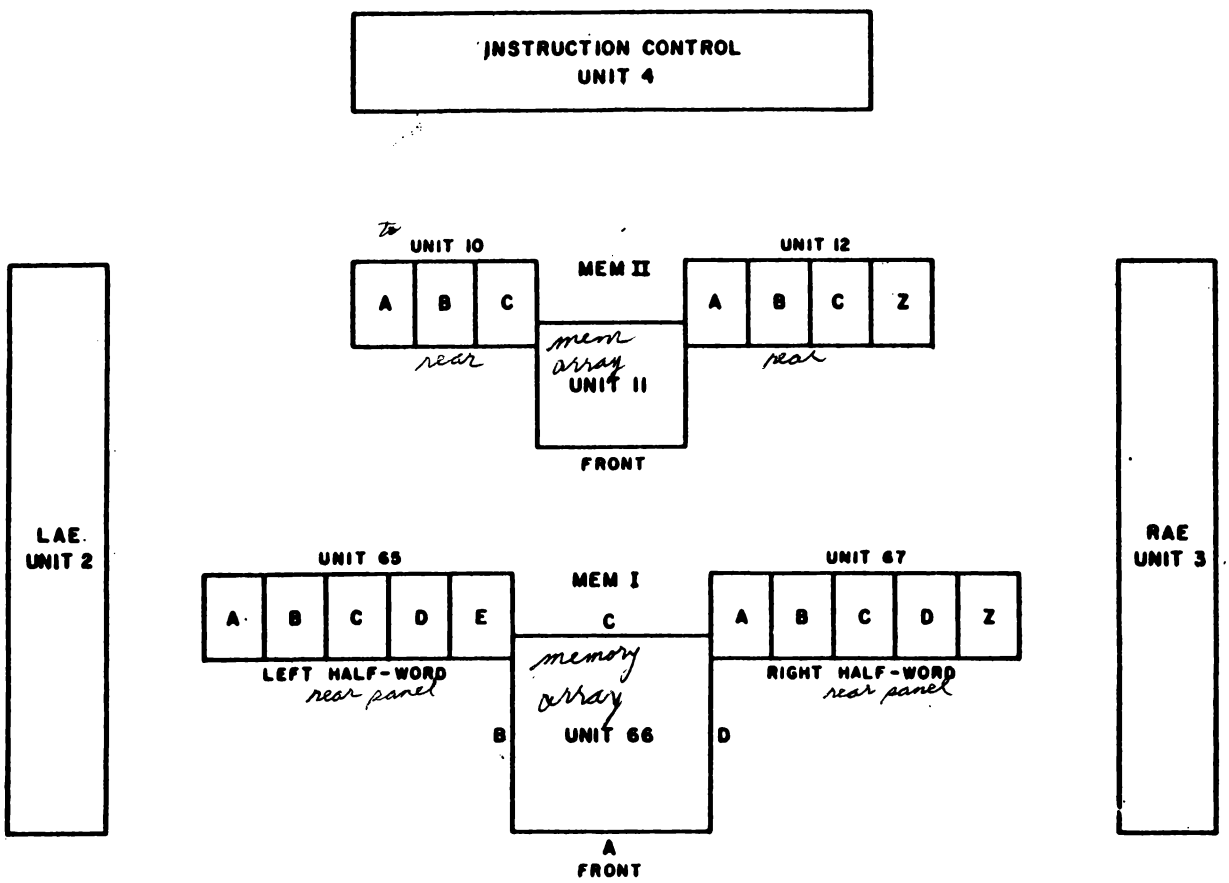
REAR VIEW



FRONT VIEW

1. A MODULE (UNIT 65)
2. B MODULE (UNIT 65)
3. C MODULE (UNIT 65)
4. D MODULE (UNIT 65)
5. E MODULE (UNIT 65)
6. CORE MEMORY ARRAY (UNIT 66)
7. A MODULE (UNIT 67)
8. B MODULE (UNIT 67)
9. C MODULE (UNIT 67)
10. D MODULE (UNIT 67)
11. Z MODULE (UNIT 67)

Core Memory 1 Units (Units 65, 66, and 67)



FLOOR LAYOUT OF MEMORY UNITS

F. Memory Cycle Definition

1. One complete operation of memory.

2. Comprised of a read cycle followed by a write cycle.

   a. Read Cycle - The time during which information in the selected memory location is taken from that location (read) and transferred to the memory buffers.

NOTE: During OT-B time of a store class instruction, and during Break-In time of an I/O operation, the information is read from the specified memory but is not transferred to the memory buffers. This is because new information is to be placed in the memory and the old information is to be destroyed.

   b. Write Cycle - The time during which the information contained in the memory buffers is placed (written) into the selected memory location.

3. Once a memory cycle is started it cannot be stopped by computer action.

G. Summary Questions:

1. Answer the following True or False:

   a. One disadvantage of Core Memory is that it has destructive readout. T

   b. The Program Ctr. may condition the MAR. only during PT Time. T

   c. Information read out of Core Memory is always transferred to the Memory Buffers. F

   d. A parity check will check for an odd number of failing bits. T

   e. One advantage of Core Memory is that access to information is faster than what it is for drums. T

   f. Address 2.00000 thru 3.77757 can be used to select Mem. I. T

   g. An AN-FSQ-7 computer does not have Units 7, 8 and 9. T

   h. If the read portion of a memory cycle is started a write cycle will also occur. T

   i. During a memory "store" cycle, a read cycle occurs first to destroy the previous contents of memory. T

j. Once a memory cycle is started it cannot be stopped by computer action.

2. Complete the following statements

a. In an AN-FSQ-7 computer the ferrite core arrays will be contained in units 11 and 66.

b. Modular units 10 and 65 do not contain Z modules.

c. The A side of Unit 66 is referred to as the front side.

II. Basic Ferrite Core Theory

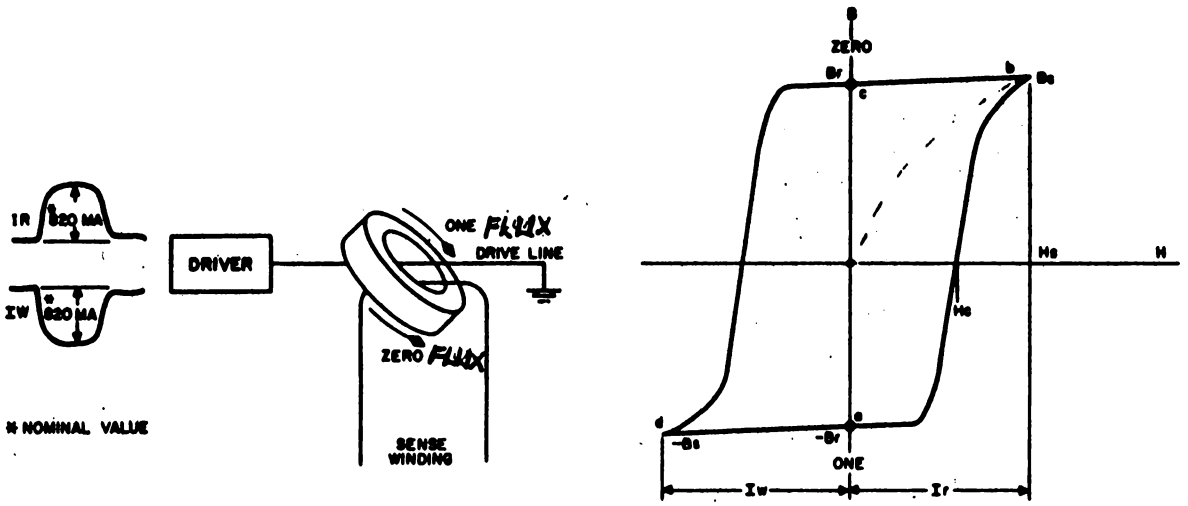
A. Ferrite Core Physical Description

1. The principal component of a magnetic core memory storage device is a ferrite core which possesses a square hysteresis loop, a low coercive force, and a short flux reversal or switching time. The ferrite core used in the two core memory devices is composed of a mixture of ferric and manganese oxide powders which are bonded together in the form of a toroid having an inside diameter of 0.050 inch (0.127 cm), an outside diameter of 0.080 inch (0.203 cm), and a thickness of 0.025 inch (0.0635 cm). A carefully controlled sintering or firing process imparts the desired characteristics to the core.

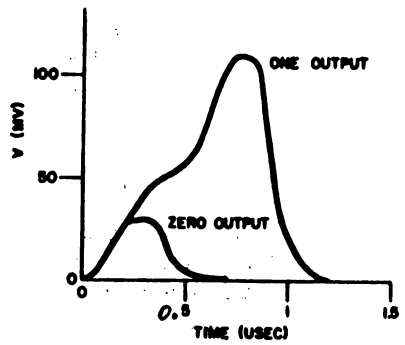
B: Magnetic Characteristics - Major Hysteresis Loop

1. The usefulness of a ferrite core as a binary storage device depends upon four important characteristics; the ability of the core to remain in one of two stable magnetic states, the squareness ratio, the switching time, and the ratio of coercive force to applied field required to produce the major or saturation hysteresis loop. The major hysteresis loop of a typical ferrite core is a plot of flux density (B) versus applied magnetic field intensity (H).

Refer to Page 0120



Major Hysteresis Loop



Typical Response of a Ferrite Core

Core Storage Element

2. Storage of binary information in a ferrite core is dependent on the ability of the core to retain a relatively large value of residual or remnant flux upon the termination of a driving or switching pulse of current. Two primary states of residual or remnant flux density (B_r and $-B_r$) are possible and these have been defined as the zero and one states respectively. To switch a core from one state to the other, it is necesssry to apply a current pulse of I_r or I_w ma (depending on the initial content of the core) to the drive line that links the core. The resultant applied field of 820 ma-turns will saturate the core in the desired direction, causing the flux state to reverse by traversing the loop path a-b-c or c-d-a.

3. During core memory operation, the state of a core is determined by applying a read current pulse (I_r) to the drive line, and detecting the resultant changes in flux density by measuring the voltage induced in a sense winding. If the core was initially in the one state, application of the read current pulse(I_r) will cause the core to be switched to the zero state (traversing path a-b-c) with the result that a relatively large change in flux density ($2B_r$) will be detected by the sense winding (one output signal). If the core was initially in the zero state, application of the read current pulse (I_r) will not switch the core (path c-b-c is traversed), with the result that a relatively small change in flux density will be detected by the sense winding (zero output signal). The amplitude of the zero output signal is dependent upon the ratio of the residual flux density (B_r) to the saturation flux density (B_s), which is defined as the squareness ratio ($R_s = B_r/B_s$) of the core. This ratio is important in that it determines the relationship between the amplitudes of the one and zero output signals. The magnitude of the zero output signal decreases as the value of R_s approaches 1, with the result that the difference between the amplitudes of the one and zero output signals becomes greater. Ferrite cores used in the two core memories have a squareness ratio greater than 0.95.

Refer to Page 0120

4. The time required to produce a flux change or flux reversal is of equal or greater importance than the squareness ratio. The zero output signal is not only smaller in amplitude than the one signal, but also peaks earlier and is of shorter duration. Since these differences exist, it would appear that information detection could be accomplished by either a difference time or a difference-amplitude sampling technique. However, in a practical core memory, a difference-time sampling technique must be used because the noise signals generated in the memory make the difference-amplitude sampling technique unfeasible.

Core Storage Element

The time required for a core to switch from one state to the other is defined as the switching time, T_s. This time is actually measured as the elapsed time between the time that the driving current pulse reached 50 percent of its amplitude, and the time at which the one putput signal has dropped to 10 percent of its peak amplitude. The switching time for cores used in the memories is approximately 1.2 usec for an applied field of 820 ma through a 1-turn drive winding.

5. Simplified Hysteresis loop sequence for a new ferrite core.

   a. Assume the core has never been magnetized. (New Core) (Intersection of "B" & "H" lines.)

   b. Apply 820 mils of Read current. (Core is driven to saturation. (Point "b".)

   c. Remove current. Magnetism returns to point "C".

   d. Apply 820 mils of Write Current. Magnetism of core is switched to point "d".

   e. Remove Write Current. Magnetism returns to Point "a".

   f. Apply Read Current. Core switches from "a" to "b".

   g. Remove Read Current. Core falls back to "c".

   h. The switching of the core induces a voltage in the Sense winding. (Approx. 100 MV).

C. Explanation of Sensing a "One".

1. Core never returns to the non-magnetized state.

Refer to Page 0120

2. If the "Read" current switches the core from a "One", point "a", to a "Zero", point "C", the induced voltage in the Sense winding indicates that the core was a one. If the core was in the Zero state, point "c", the Read current would switch the core to point "b", and then back to point "c". The switching of the core from "c" to "b" to "c" does not induce the voltage necessary for a One.

3. The core switching from a "Zero" to a "One" as a result of Write current also induces a voltage in the sense winding but this is not used or sampled to indicate an output from the core.

4. The switching of a core, when reading a "One ", to the "Zero" state of magnetism indicates that CORE Readout is "Destructive". A "One " could not be read from the core again unless Write current had switched the core back to the "One " state.

D. Summary Questions:

1. Answer the following questions True or False:

   a. One of the most important characteristics of a ferrite core is its ability to remain magnetized after the magnetizing force has been removed. T

   b. The only difference between a one and a zero in a ferrite core is the amount of flux. F

   c. A core is set to a one or a zero depending on the direction of magnetizing flux. T

   d. A core contains a zero immediately after the read cycle T

   e. The only difference between a one and a zero pulse on the sense winding is the amplitude. F

   f. The switching time for ferrite cores is 1.2 usec. T

   g. The same amplitude signal is induced into the sense winding when a core is switched from a zero to a one as when it is switched from a one to a zero. T

2. Complete the following statements:

   a. The read current amplitude is 520 ma.

   b. The amplitude of a one pulse on the sense winding is 100 mv.

   c. If a core contains a zero when read current is applied a signal will be present on the sense winding for .5 usec.

Core Storage Element

III. 64^2 Core Plane

A. 4096 $(_{10})$ cores in a 64^2 plane. $10,000_{(8)}$ Refer to Page 0170

1. Each plane has its own Memory Buffer FF.

B. "X" and "Y" Windings

1. Used to drive the selected cores during both the read cycle and the write cycle. Current flows in one direction during read cycle and opposite direction during write cycle.

2. The "X" winding carries one-half the current necessary to switch a ferrite core.

3. The "Y" winding carries one-half the current necessary to switch a ferrite core.

4. A "X" and "Y" winding pass through the hole in a ferrite core once. This is effectively "one-turn" for each winding.

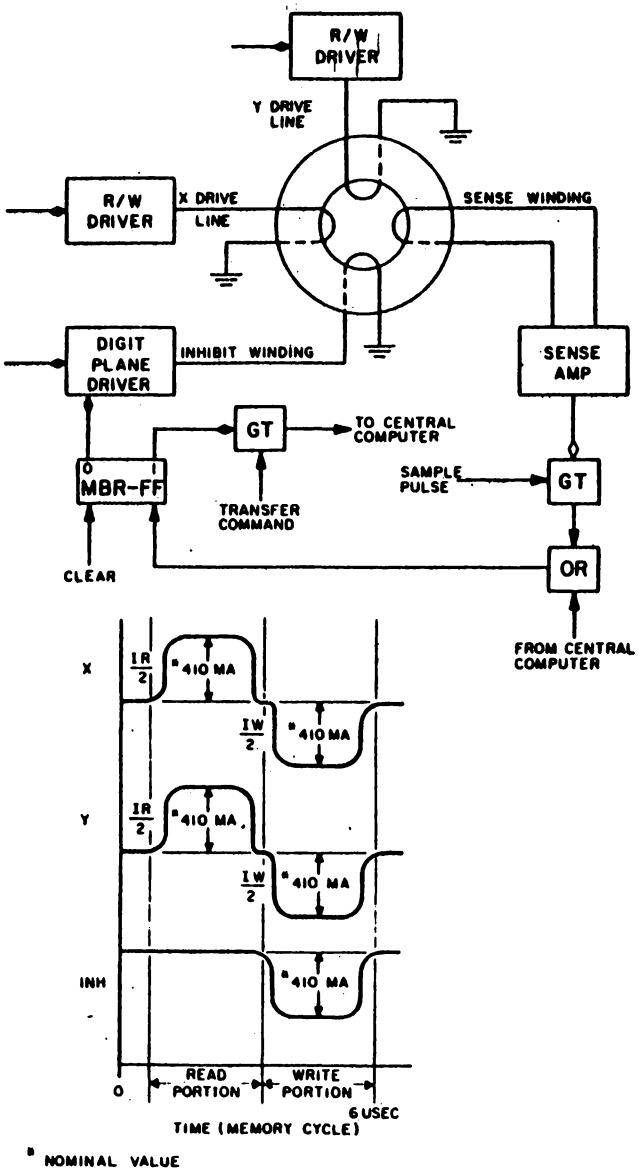
5. Number of windings (64 each)

   a. 64X times 64Y gives total possible selection of 4096_{10} (10,0008) addresses.

   b. Each winding (X or Y) passes through 64 cores on every plane.

   c. Only one core on a given plane is fully selected (both X and Y currents passing through it) for any address selection. 126 cores (63X and 63Y) are half selected at the same time. A core must be fully selected to change its state.

6. The "coincident current" method of selection of a particular ferrite core (1 of 4096) is accomplished by having all the "X" windings enter on the "Left and Right" sides of a plane, while all the "X" windings enter on the "Top and Bottom" of the plane (Looking at the illustration).



* NOMINAL VALUE

Ferrite Core Windings

Core Storage Element

a. Only one "X" and one "Y" winding will be selected for carrying current at a time.

b. Where the two lines (Y and Y) cross or intersect in the plane is the fully selected location. (The two currents will add, applying full switching current to a core.)

C. Sense Winding

1. The sense winding passes through all the cores of a single plane. Refer to Pg. 0170

2. The sense winding is used to sense the switching of the selected location.

a. If the fully selected location is switched from the "one" state to the "zero" state, the sense winding will feel the change (reversal of flux induces voltage on sense winding). The switching of a core will cause a sense amplifier circuit to condition a GT. The GT will be sampled and the output sent to the plane's Memory Buffer FF.

b. If the ferrite core was a zero the sense winding will not feel as much flux reversal. The SA will not condition the GT for a long enough period of time to allow the GT to remain conditioned at the time the sample pulse occurs. The Buffer FF will not be set. This will indicate that the location contained a zero.

D. Inhibit Winding

1. The Inhibit winding passes through all the cores of a plane. Refer to Pg. 0170

2. The Inhibit winding is wound parallel to the "Y" windings.

3. The Inhibit winding prevents a "one" from being written in a core location.

a. The "X" and "Y" winding always try to write a "one" in the selected location.

b. If the Memory Buffer FF contains a "zero" the inhibit winding will prevent the storing of a one by canceling out one-half (410 ma) of the Write current.

c. The Inhibit current is the same as 410 ma of "Read" current applied during the "Write" portion of a Memory cycle.

d. When storing a "zero" in a location the location feels only one-half write current and does not switch to the "one" state.

E. Total Windings

1. Each ferrite core in memory has 4 windings (X, Y:, Sense and Inhibit) passing through it.

F. Summary Questions:

1. Answer the following questions True or False:

   a. There are 64X and 64Y windings per core array. T

   b. There are 4096 cores per plane. T

   c. 64 sense windings are used per core array. F

   d. 33 inhibit windings are used per core array. F

   e. Inhibit windings run parallel to the X windings. F

   f. One sense winding passes through every core of a particular plane. T

2. Complete the following statements:

   a. The drive current on an X line is 410 ma.

   b. Inhibit current cancels the effect of 1/2 drive current during WRT time.

   c. The Digit Plane Driver is conditioned by the MEM BFR ON/OFF.

IV. Half-Selected Ferrtie Cores

A. Minor Hysteresis Loops

1. Each selected X and Y line carries one-half amplitude current. The core at the junction of a selected X and Y line receives the full current. A core receiving full current, therefore, switches to either the 0 or the 1 state, depending upon whether a read or a write operation is being carried out. When writing a 0, a third current, called the inhibit current, is present. This current affects all the cores in the plane and has a value of a nominal half-read current. Therefore, when writing a 0, all cores recieve the inhibit current. The selected core receives the full-write current and the inhibit current, resulting in only half-write current. This flux change is not sufficient to switch the core to the 1 state. The half-amplitude currents are insufficient to cause a core to switch; however, they do cause the state of magnetization of a core to change slightly.

Refer to Pg. 0220

2. A core which is in a modified state of magnetization is considered to be in a disturbed state. In the coincident current scheme, there are five basic states of magnetization. These are as follows:

   a. Read-disturbed 0

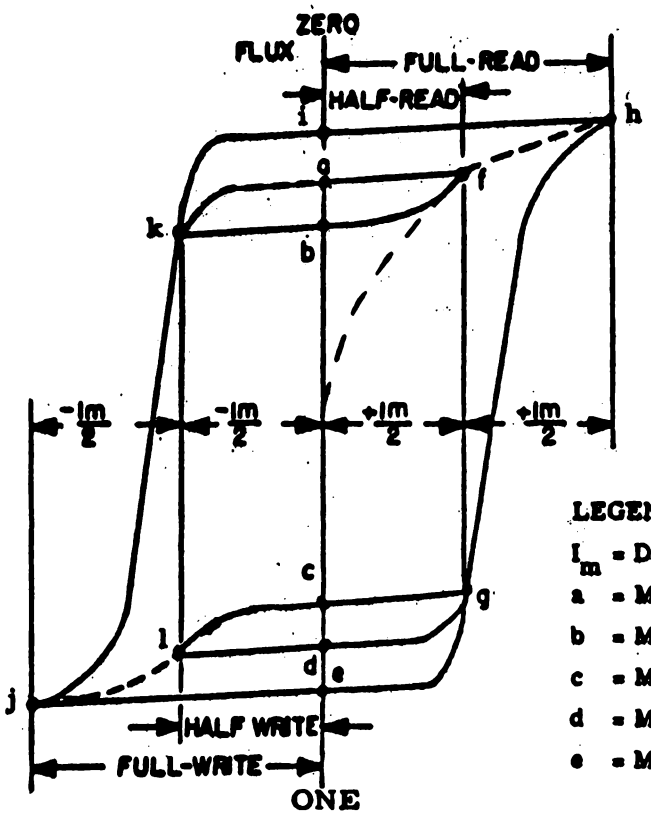
   b. Write-disturbed 0

   c. Read-disturbed 1

   d. Write-disturbed 1

   e. Undisturbed or newly written 1.

3. A sixth state, an undisturbed or newly written 0, does not exist because a read is always followed by a write operation. In writing a 0, a half-write current actually passes through the core, resulting in the write-disturbed 0 condition. (Actually, there are 14 basic states in the memory. However, these 14 states can be reduced to the 5 mentioned if the minor deviations produced by the other 9 states are neglected.)



LEGEND:

I_m = Driving current necessary to saturate the core

a = Magnetic state of core defined as read disturbed 0

b = Magnetic state of core defined as write disturbed 0

c = Magnetic state of core defined as read disturbed 1

d = Magnetic state of core defined as write disturbed 1

e = Magnetic state of core defined as undisturbed or newly-written 1

MAGNETIC HYSTERESIS LOOP FOR CORE

Core Storage Element

4. A hysteresis loop showing the five basic states is illustrated. A careful examination of the hysteresis loop reveals that there are different paths to be followed, depending upon the past history of the core. Specifically, a half-selected (half-read current applied to a core) read-disturbed 0 traverses the path from point "a" to point "f" and back to point "a" again. The resultant flux change is therefore very small. When half-selected, a core initially at the write-disturbed 1 position traverses the path from point d to point g to point c. A net flux change results from traversing this path. Hence, one basic fact is revealed; i.e., a half-selected write-disturbed 1 induces a greater voltage into the sense winding than the half-selected read-disturbed 0. Refer to Pg. 0220

5. A half-selected read-disturbed 1 produces a greater flux change than does a half-selected read-disturbed 0. That this is true is perhaps better understood by comprehending the fact that applying a half-selected current to a core in the 1 state tends to desaturate the core, whereas a half-selected current applied to a core in the 0 state tends to drive the core into saturation. The output of a core traversing minor loops, such as the read-disturbed 1 and read-disturbed 0, is dependent only upon the magnitude of the differential, or incremental, permeabilities. The differential permeability is known to be least at saturation of the material. The output of a half-selected read-disturbed 0, which tends toward saturation, is less than the output of a half-selected read-disturbed 1. The difference between the output of a half-selected 1 and a half-selected 0 is defined as: Refer to Pg. 0220

   $0 = {}^{h}V_1 - {}^{h}V_o$

   ${}^{h}V_1$ = Voltage output of a half-selected 1

   ${}^{h}V_o$ = Voltage output of a half-selected 0

6. Consider <u>half-selected</u> cores

   a. Assume magnetism of core to be point (b). Refer to Pg. 0220

   b. Apply 1/2 read current and then remove. Half-selected core moves on magnetic path (b) - (f) - (a). Core is a read disturbed zero.

   c. Apply and remove 1/2 write current. Path is (a) - (k) - (b). Core is a write disturbed zero.

   d. Assume magnetism of core to be at point (e).

   e. Apply and remove 1/2 read current. Magnetic path (e) - (g) - (c). Core is a read disturbed one.

f. Apply and remove 1/2 write current. Magnetic path (c) - (1) - (d). Core is a write disturbed one.

7. Cancellation of the half-selected cores half-write by inhibit current.

   a. All cores except the fully selected core will be read disturbed "1"s or "0"s after an inhibit current.

   b. The fully selected core will be a write disturbed core after an inhibit cycle.

8. Effective current pulse sequence applied to cores of one memory plane. Selected core is to contain a:

	1	0
a. Selected core (1)	Full-Read Full-Write	Full-Read, Half-Write
b. Half-selected Cores (126)	Half-Read, Half-Write	Half-Read, No Pulse
c. Nonselected Cores (3,969)	No Pulse, No Pulse	No Pulse, Half-Read

B. Summary Questions:

1. Answer the following questions True or False:

   a. One half write current will not change the magnetic lines of flux in a core. F

   b. A newly written zero condition is possible immediately after a read cycle. T

   c. A properly adjusted memory can read a core in any of the disturbed one conditions as a one. T

   d. All cores will be disturbed after writing a zero into any core. T

   e. There can never be more than one undisturbed core in a core plane at any one time. F

2. Complete the following statements:

   a. Point E on the hysteresis loop represents a newly written 1.

Core Storage Element

b. Point B on the hysteresis loop represents a write disturbed 0.

c. Point A on the hysteresis loop represents a read disturbed 0.

d. Point C on the hysteresis loop represents a read disturbed 1.

e. Point D on the hysteresis loop represents a write disturbed 1.

V. Analysis of Ferrite Core Output Signals

A. Effect of Half-Selections

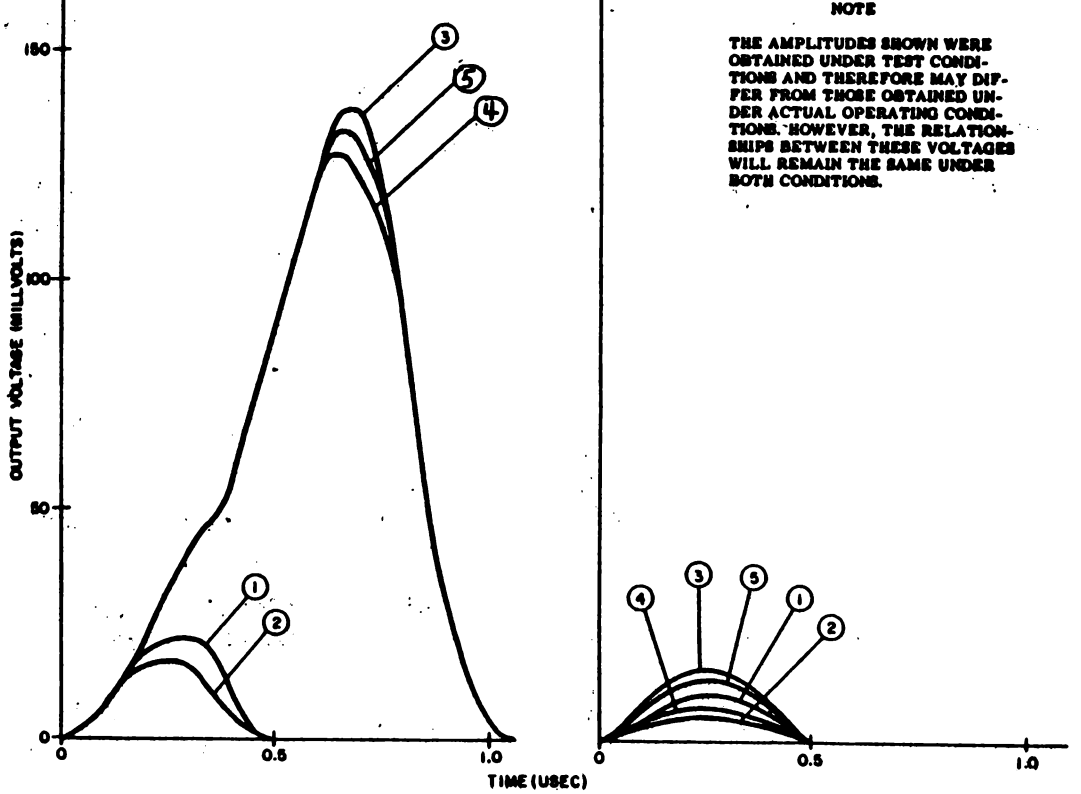
1. Approximate output from a ferrite core: Refer to Page 0260

Waveform	Full Read	Half Selected
1. Write Disturbed "0"	22MV	10MV
2. Read Disturbed "0"	16MV	5MV
3. Undisturbed "1"	139 MV	14MV
4. Read Disturbed "1"	131MV	7MV
5. Write Disturbed "1"	135MV	12MV

2. The induced voltages caused by half-selection are 0.5 usec. in duration. Refer to Page 0260

3. If all of the half-selected core outputs were added together it can be seen that a large pulse would be the result.

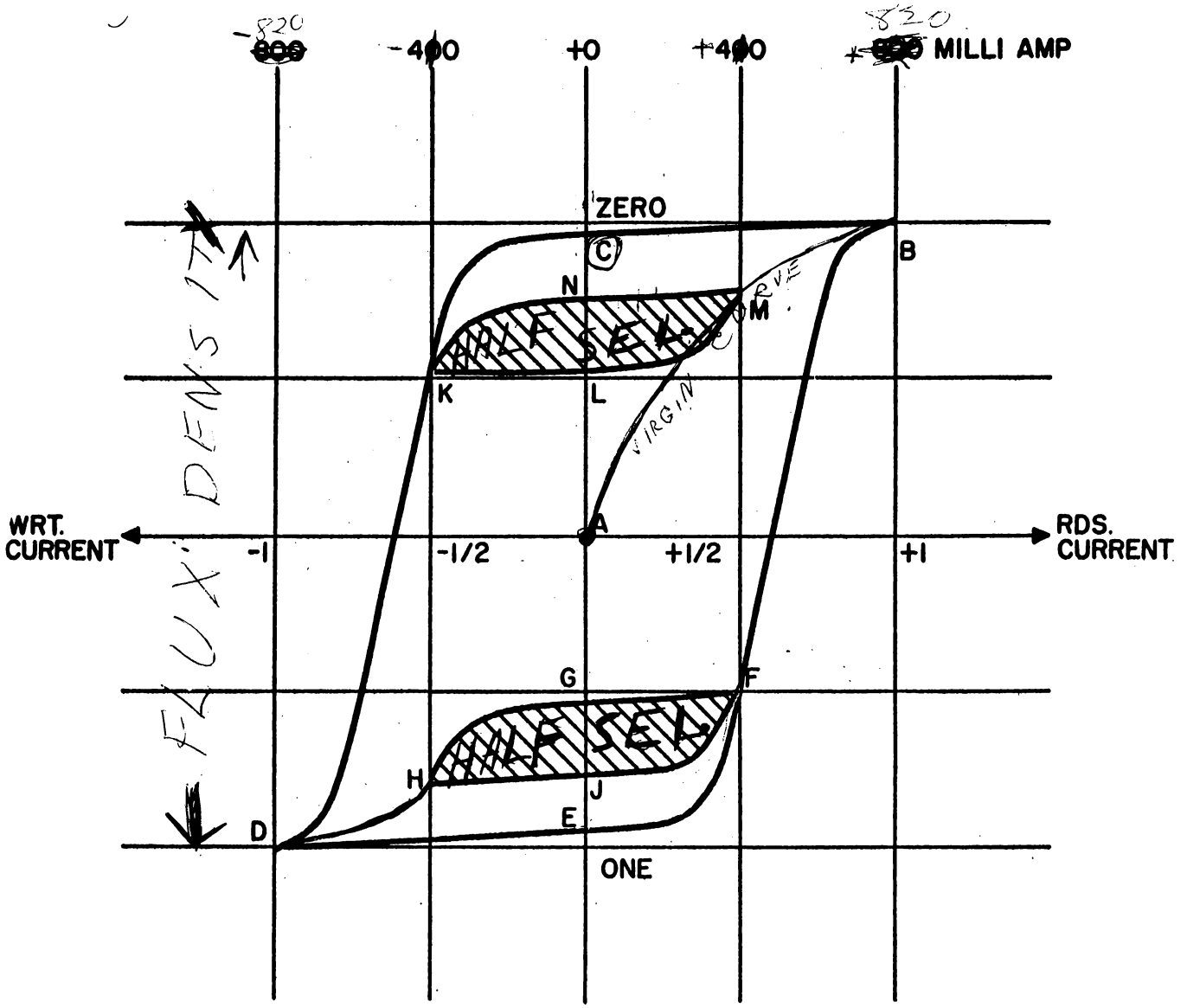
	INITIAL STATE OF CORE	OUTPUT WHEN I_r IS APPLIED	AMP. IN MV	OUTPUT WHEN $I_r/2$ IS APPLIED	AMP. IN MV.
1	w0	$_wV_0$ - FULL SELECTED WRITE DISTURBED ZERO	23	$_wV_{h0}$ - HALF SELECTED WRITE DISTURBED ZERO	10
2	r0	$_rV_0$ - FULL SELECTED READ DISTURBED ZERO	16	$_rV_{h0}$ - HALF SELECTED READ DISTURBED ZERO	5
3	s1	$_sV_1$ - FULL SELECTED UNDISTURBED ONE	139	$_sV_{h1}$ - HALF SELECTED UNDISTURBED ONE	14
4	r1	$_rV_1$ - FULL SELECTED READ DISTURBED ONE	131	$_rV_{h1}$ - HALF SELECTED READ DISTURBED ONE	7
5	w1	$_wV_1$ - FULL SELECTED WRITE DISTURBED ONE	135	$_wV_{h1}$ - HALF SELECTED WRITE DISTURBED ONE	13



NOTE

THE AMPLITUDES SHOWN WERE OBTAINED UNDER TEST CONDITIONS AND THEREFORE MAY DIFFER FROM THOSE OBTAINED UNDER ACTUAL OPERATING CONDITIONS. HOWEVER, THE RELATIONSHIPS BETWEEN THESE VOLTAGES WILL REMAIN THE SAME UNDER BOTH CONDITIONS.

Outputs of a Typical Ferrite Core



	FULLY SEL. OUTPUT IN MV.	HALF SEL. OUTPUT IN MV.
C - UNDISTURBED ZERO (IMPOSSIBLE)	-	-
N - RDS DISTURBED ZERO	16	5
L - WRT DISTURBED ZERO	22	10
G - RDS DISTURBED ONE	131	7
J - WRT DISTURBED ONE	135	12
E - UNDISTURBED ONE	139	14

NOTE: BASE WIDTH OF A FULLY SELECTED "1" BIT OUTPUT IS APPROXIMATELY TWICE THAT FOR A "0" BIT.

Example:

126 X 5 MV (smallest output) = 630 MV / output of selected core.

This cumulative output of the sense winding is undesirable because "One" amplitude would be present on the sense winding during every cycle.

4. Two efforts are made to nullify the effect of half-selections. Core polarity and the timing of the sample pulse which strobes the GT conditioned by the SA.

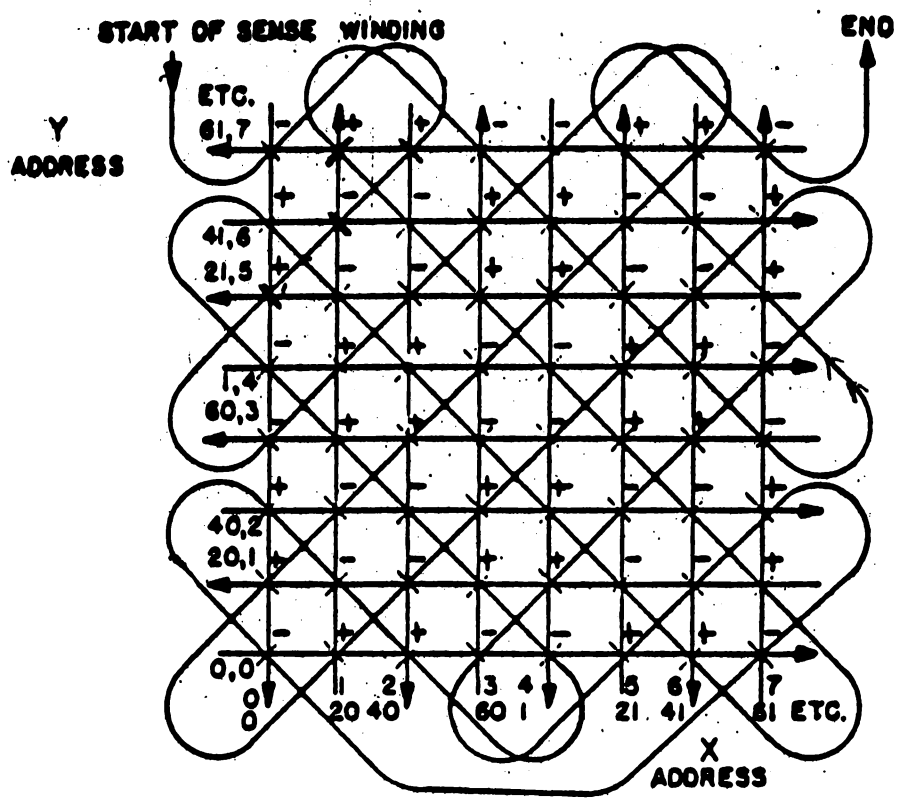
B. Core Polarity

1. When a core is read out (i.e., the core is switched to the 0 state), a signal of a given polarity is induced into the sense winding. The polarity of the voltage is the same for either a 1 or a 0 and is determined by the wiring geometry of the plane. After the polarity of a core in the corner of an array is established, the geometry of the array is such that a polarity pattern follows. To determine the polarity, use should be made of only the right hand rule and Lenz's law.

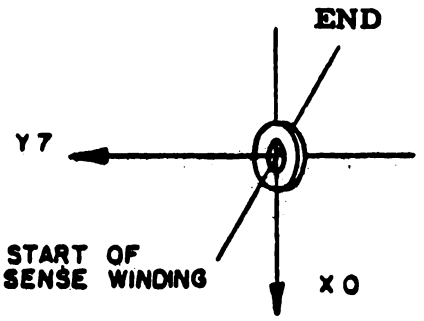
2. Illustrated is a view of the core at X0, Y7. By grasping the X or Y line with the right hand and pointing the thumb in the direction of current flow, the fingers of the right hand indicate the direction of flux in the core to be counter-clockwise. Lenz's law states that the current which flows as a result of an induced voltage is such as to oppose the buildup of flux. Refer to Page 0280

3. The direction of the flux in the core has been determined to be counterclockwise by means of the right hand rule. If the sense winding is now grasped with the right hand so as to oppose the flux in the core, then the thumb points in the direction of the "end" terminal of the sense winding. If the current induced in the sense winding by an individual core flows toward the "end" terminal, then by DEFINITION that core is said to be a negative core. If the induced current flows toward the "start" end, the core inducing the current is considered to be a positive core.

4. It should be noted that the polarity of a signal in the sense winding is a relative thing. The item desired as an end result is the difference of voltage between the two ends of the winding. To achieve this, the output of the sense winding is amplified by a differential amplifier and then converted to a positive voltage that is used as the gating voltage on the suppressor of a gate tube. This gate tube is sensed by 0.1 -usec pulses at strobe time, thereby emitting a 0.1-usec pulse when the core contained a 1.



(a)



(b)

NOTE: ARROWHEADS INDICATE THE DIRECTION OF CURRENT FLOW THROUGH THE WIRES DURING READ TIME.

Core Storage Element

C. Polarities of Typical Core Plane

1. The $(33)_{10}$ planes in the memory each contain $(4096)_{10}$ cores which are located at the intersections of the X and Y lines. The sense and inhibit windings link every core in a plane. The direction of the driving currents and the manner in which the sense winding links the cores determines the the polarity of the signal induced into the sense winding. A given core output is only sampled during read-out time, thus the polarities pertain only during that time.

2. The output of a given core will have the same polarity regardless of whether a core contains a 0 or a 1. Hence it is seen that the indications from the plane are either positive or negative and independent of whether the core contains a 0 or a 1.

3. An 8 by 8 plane and the polarities associated with the core outputs are illustrated. Each X and Y line contains an equal number of positive and negative polarities. A larger plane, such as the $(64)_{10}$ by $(64)_{10}$, is merely a continuation of the polarity pattern corresponding to the first eight positions in the $(64)_{10}$ by $(64)_{10}$ array.

Refer to Page 0280

4. The pattern formed by the cores (4 of the same polarity in a group) is referred to as a checkerboard pattern.

D. Core Polarity Summary

1. The sense winding is wound to produce positive and negative cores so as to have the voltages induced on the sense winding by the half selected cores tend to cancel.

   a. The voltage from positive cores tends to cancel the voltage from negative cores or vice versa.

   b. Both a "1" and "0" give the same polarity output from a given core. Only the amplitude varies.

2. The output on the sense winding of a 64^2 plane consists of:

   a. The fully selected core. (1)

   b. Plus the half-selected cores of the same polarity. (62)

   c. Minus the half-selected cores of the opposite polarity. (64)

Core Storage Element

Analysis of Sense Winding Output Voltage

1. When the selected X and Y drive lines are energized with half-amplitude read current pulses (to read out the contents of the selected core), a total of 127 cores are involved in producing the sense winding output voltage. That is, when a particular core is selected, the sense winding output represents the summation of the selected core output voltage and the noise voltages generated by the 126 half-selected cores (63 cores on each of the selected X and Y drive lines). Each X and Y drive line contains a number of positive and negative cores; therefore, in a 64 by 64 core matrix, each drive line will contain 32 positive and 32 negative cores. Thus, because of this sense winding polarity pattern, the application of coincident half-read current pulses to the selected X and Y drive lines of a memory plane will result in the generation of 62 (31 cores on the selected X and Y drive lines) half-selected output voltages whose polarity is the same as the polarity of the selected core output voltage, and 64 (32 cores on the selected X and Y drive lines) half-selected output voltages whose polarity is opposite to the polarity of the selected core output voltage. As a result, the half-selected output voltages of 124 of the 126 half-selected cores (62 positive and 62 negative output voltages) will tend to cancel each other. However, complete cancellation of these 62 pairs of half-selected cores (a pair consists of one positive and one negative half-selected core) can only occur under specific conditions since the amplitude of the individual half-selected output voltage depends upon which flux state the core exhibits prior to the application of the half-read current pulse. The half-selected output voltages of 2 of the 126 half-selected cores whose polarity is opposite to the polarity of the selected core will not be cancelled; therefore, these two half-selected output voltages will subtract from the selected core output voltage. The equation to express the sense winding output voltage produced during the read portion of the memory cycle may be written as follows:

$$V_{out} = V_s - 2V_h \pm 62V_d$$

Where:

V_{out} = the output voltage of the sense winding

V_s = the output voltage of the selected core

V_h = the average half-selected output voltage whose polarity is opposite to the selected core output voltage

V_d = the difference between the average positive half-selected output voltage and the average negative half-selected output voltage.

2. The last term of the equation, which deals with the summation of the half-selected output voltages that tend to cancel each other, is defined as the delta voltage of the sense winding output. The delta voltage may be either positive, negative, or zero, depending upon whether the average positive half-selected output voltage is larger than, smaller than, or equal to the average negative half-selected output voltage. Since the delta voltage is obtained from 62 pairs of half-selected cores, it follows that, if each core of a pair of cores is in the same flux state and if the characteristics of all the cores are considered to be exactly the same, the application of a half-read current pulse to the half-selected cores will cause each core of a pair of cores to generate a half-selected output voltage that is exactly equal to, but of opposite polarity to, its mate. If each of the 62 pairs of half-selected cores is thus balanced, the delta voltage will be equal to zero to provide for the maximum cancellation of half-selected output signals. In memory maintenance programming, this condition of maximum cancellation of half-select output voltages is obtained by using either a 1's or a 0's test pattern wherein all the cores of a memory plane are in either the one or zero flux state.

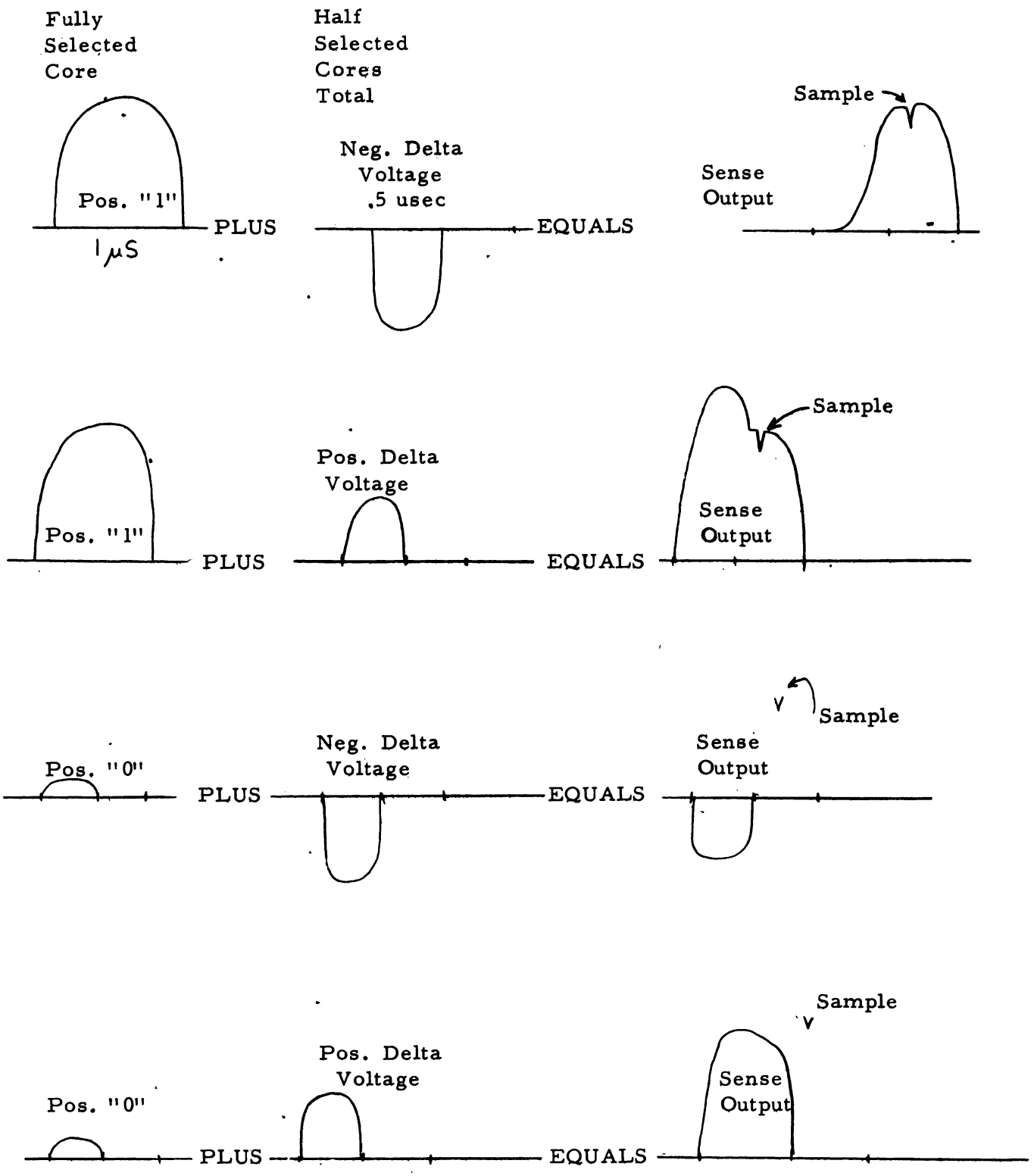
3. A study of the equation reveals that the maximum value of delta voltage is obtained when all the half-selected cores of one polarity produce the smallest half-selected output voltages, while all the half-selected cores of the opposite polarity produce the largest half-selected output voltages. The smallest half-selected output voltage is produced by a core in the read disturbed zero flux state, and that the largest half-selected output voltage is produced by a core in the undisturbed one flux state. However, since it is only possible for one core on an X or Y drive line to exhibit the undisturbed one flux state at any particular time (an attempt to cause a second core to exhibit the undisturbed one flux state will cause the existing undisturbed core to be write disturbed), this flux state does not enter into the determination of the maximum value of delta voltage. Instead, the maximum value of delta voltage is obtained when all the half-selected cores of one polarity are in the read disturbed zero flux state, and all the half-selected cores of the opposite polarity are in the write disturbed one (w1) flux state.

4. Since the delta voltage can be of either polarity, the maximum value of delta voltage can be produced in two different ways; that is, by two different test patterns. The maximum positive delta voltage is produced when all the plus half-selected cores are in the write disturbed one (W1) flux state and all the minus half-selected cores are in the read disturbed zero (rz) flux state. If all the cores of the plane contain the pattern just described, the plane is said to contain a regular checkerboard pattern. The maximum negative delta voltage is produced when all the plus half-selected cores are in the read disturbed zero (rz) flux state and all the minus half-selected cores are in the write disturbed one (w1) flux state. The test pattern that will produce this condition is defined as the inverted checkerboard pattern. Since the polarity of the delta and selected core output voltages can be individually positive or negative, eight separate conditions exist whereby the maximum value of delta voltage will either add to or subtract from the selected core output voltage to produce the maximum distortion of the selected core output voltage.

MAXIMUM DELTA VOLTAGE COMBINATIONS

SELECTED CORE POLARITY AND CONTENT	NEGATIVE CORES	POSITIVE CORES	RESULTANT POLARITY	RESULTANT OUTPUT SENSE WINDING VOLTAGE
Positive 1	rz	w1	+	Larger positive 1
Positive 1	w1	rz	-	Smaller positive 1
Negative 1	rz	w1	+	Smaller negative 1
Negative 1	w1	rz	-	Larger negative 1
Positive 0	rz	w1	+	Larger positive 0
Positive 0	w1	rz	-	Smaller positive 0
Negative 0	rz	w1	+	Smaller negative 0
Negative 0	w1	rz	-	Larger negative 0

5. If all the cores of a plane have identical characteristics, the maximum value of delta voltage produced under the above mentioned conditions will have a peak amplitude in excess of 400 mv and a duration of approximately 0.5 usec. Since the delta voltage and the selected core output voltage both start at the same time, the delta voltage always distorts the selected core output signal. If the selected



HALF-SELECTIONS AFFECT ON FULLY SELECTED FERRITE CORE

core initially contained a 0, the delta voltage will completely mask the 0 output voltage since both voltages have the same duration. However, if the selected core initially contains a 1, the delta voltage will only distort the first 50 percent of the 1 output signal and the 135-mv (approxiamte) peak of the 1 output signal will not be affected. It is because of this important timing factor that a time difference sampling technique can be used (during the execution of a memory readout cycle) to reliably determine whether the selected core contained a 0 or a 1. That is, although the peak amplitude of the delta voltage can be much greater than the amplitude of the selected core output signal, reliable memory operation is obtained by sampling the sense amplifier output voltage at a specific time, namely just past the peak of the amplified 1 signal. Because the contents of the selected core is sampled at a specific time, reliable discrimination between a 0 and a 1 output signal depends upon the ability of the sense amplifier to faithfully reproduce the relative timing of the sense winding waveform.

Refer to Page 033

6. Example:

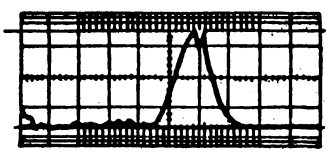
   Assume all positive cores contain "1's" and all negative cores contain "0's". Assume all cores are read disturbed.

   Read out a core containing a "1".

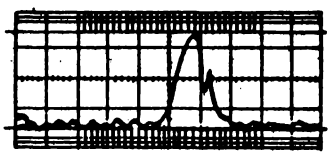
Fully selected core	/ 131 MV
plus 62 half-selected cores containing "1's" (31x & 31y)	
62 X 7 = 434	/ 434 MV
Minus 64 half-selected cores containing "0's" (32x & 32y)	
64 X 5 = 320	- 320 MV
Total	/ 245 MV

F. Core Peaking Characteristics

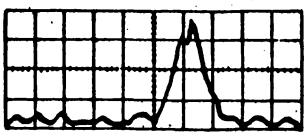
1. The cores in a memory plane, under identical operating conditions, do not all uniformly peak at the same time, nor with the same amplitudes. Core peaking may be classified into four general categories:
   a. Normal
   b. Early peaking
   c. Late peaking
   d. Low amplitude



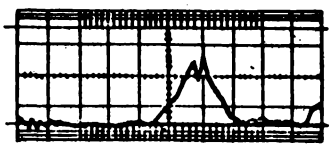
(A) NORMAL



(B) EARLY

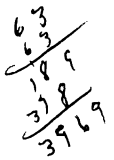


(C) LATE



(D) LOW AMPLITUDE

CORE PEAKING CHARACTERISTICS



2. Examples of the four conditions were observed at the G2 test point of the sense amplifier. In each case, allied circuitry has been eliminated as a possible cause of the peaking conditions noted, so that the waveforms reflect the true characteristics of the core itself. Observation of the conditions shown do not necessarily imply defective cores. This is based on the fact that since core characteristics are known to vary, the criterion to be used to determine a core's acceptance is proper memory operation; that is, if margins are good, and reliable memory operation is present, the core is acceptable. Under these conditions, it is always considered good practice to record the location of the suspect core(s) for future failure analysis. This course of action is particularly important because it is conceivable that at some future date, under adequate margins, these cores will probably be the first to fail.

Refer to Page 05

3. Refer to Maintenance Handbook #13 for the proper procedure to follow if a ferrite core is suspected of causing failures.

G. Summary Questions:

1. Answer the following questions True or False:

   a. Half select noise may be much larger than a one signal.

   b. The gate conditioned by the one signal is not strobed until the half select noise pulse is reduced to near zero.

   c. The half select noise from positive and negative cores should completely cancel.

   d. 127 cores can be half selected at one time.

   e. There will be 63 positive and 63 negative half selected cores during the read portion of a memory cycle.

   f. The polarity of a core is determined by the direction of X and Y drive current thru the core.

   g. The sense amplifier must be designed to condition a gate when either a positive or a negative one is read.

   h. If a core peaks too early the gate may not be conditioned by a one when the sample pulse occurs.

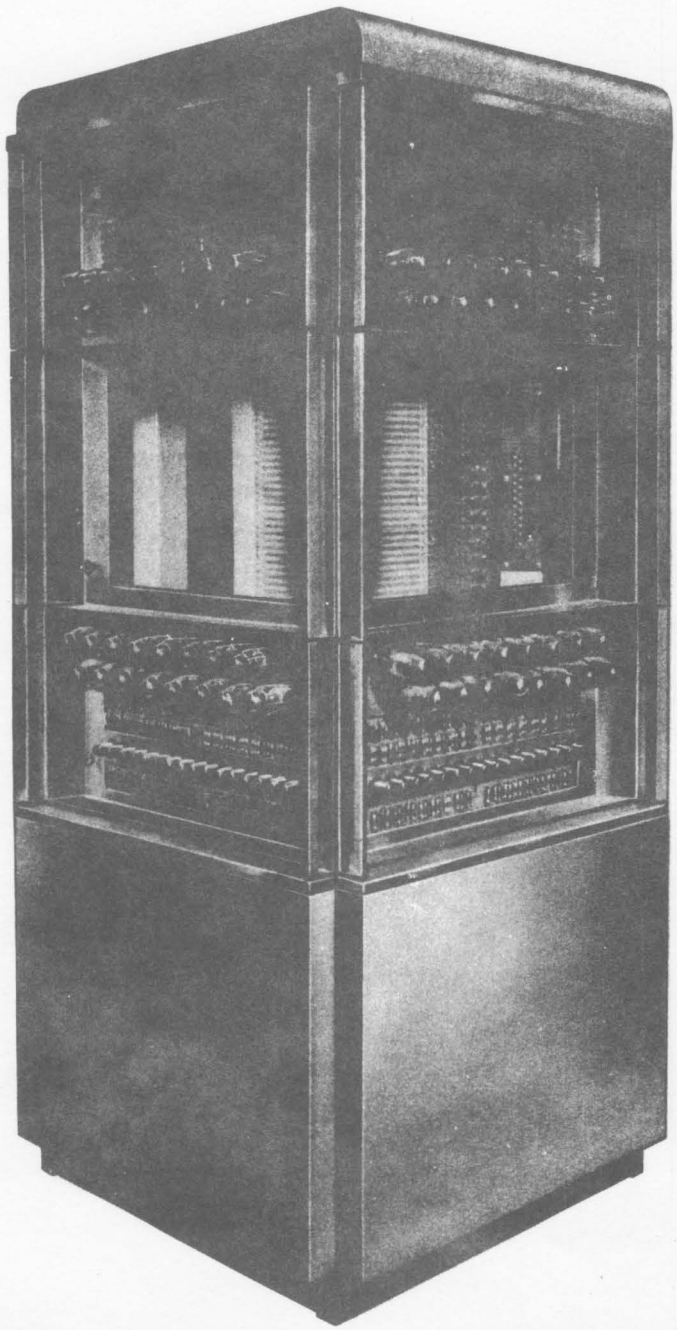
Core Storage Element

VI. 64^2 Ferrite Core Array

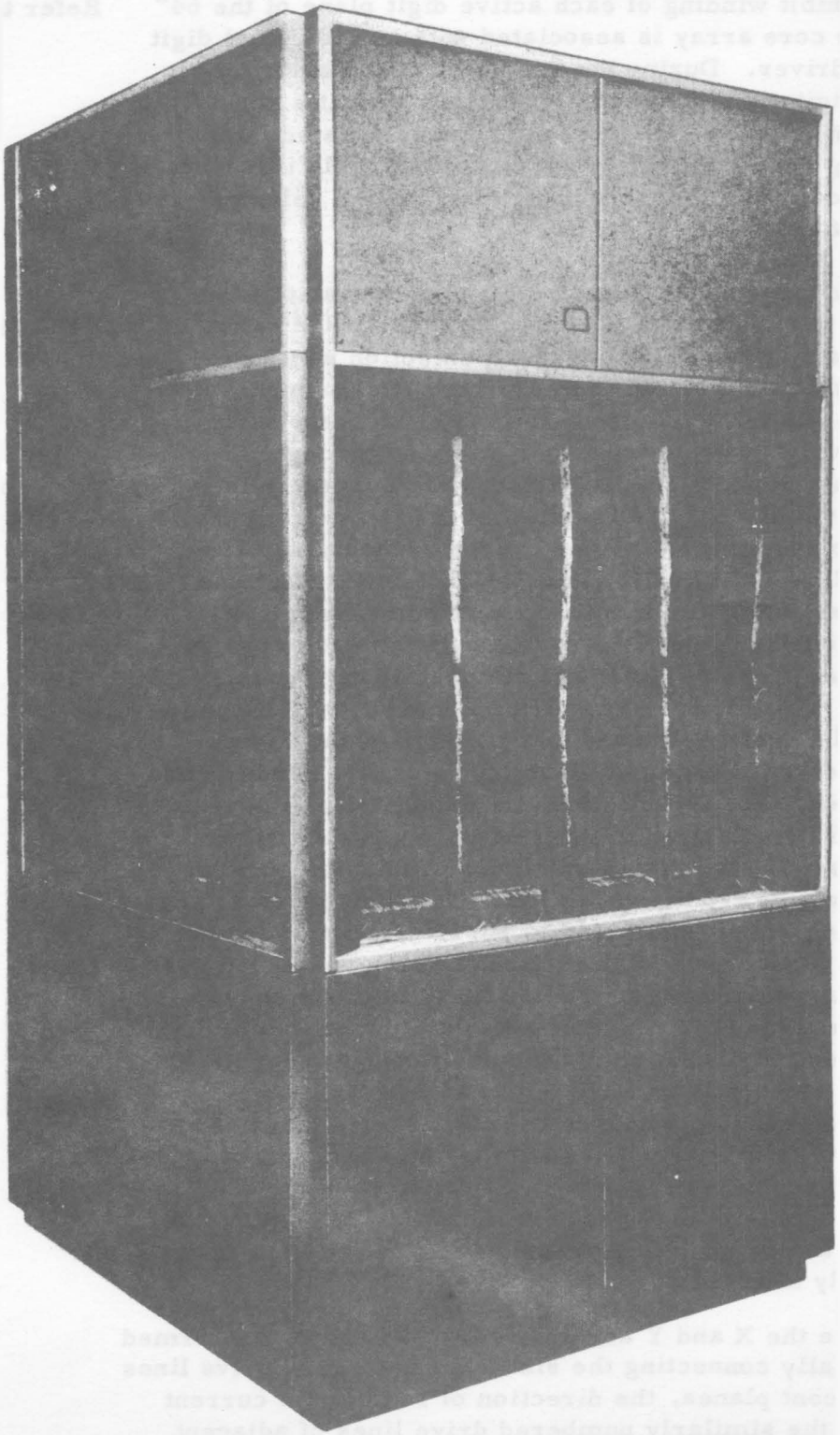
A. Physical Description

1. The 64^2 ferrite core array contained in Unit 11 is the principal component of core memory 2 since it is the information storage center of this memory device. Refer to Page 0380

2. The storage capacity of the 64^2 ferrite core array is equal to 4,096 words of 34 bits each. Since a single core can store one bit of information, the array contains 4,096 x 34 or 139,264 ferrite cores. These cores are arranged in a 3-dimensional array in which each horizontal layer or digit plane contains 4,096 cores arranged in a 64 x 64 square formation. The 34 digit planes of this array are stacked vertically, and the X and Y selection windings of these planes are interconnected to form the X and Y selection windings of the array. Actuation of the current drivers associated with one X and one Y selection winding will mutually affect the vertical column of 34 cores (one core in each plane) that represent the selected memory register. Since only 33 of these digit planes are connected to sense amplifier and digit plane drivers, only 33 planes can be active at any time. The 18th plane of the array, which is required to provide for the symmetrical wiring of the array, is used as a spare plane. Refer to Logic 0.1.7 Refer to Page 0400



64^2 Memory Unit



256² Memory Unit

Core Storage Element

2. Inhibit Winding

a. The inhibit winding of each active digit plane of the 64^2 ferrite core array is associated with an individual digit plane driver. During the execution of a memory cycle each digit plane driver is controlled so that a read current pulse will be applied to the associated inhibit winding during the write portion of the cycle if it is required to inhibit the writing of a 1 in the selected core of the plane.

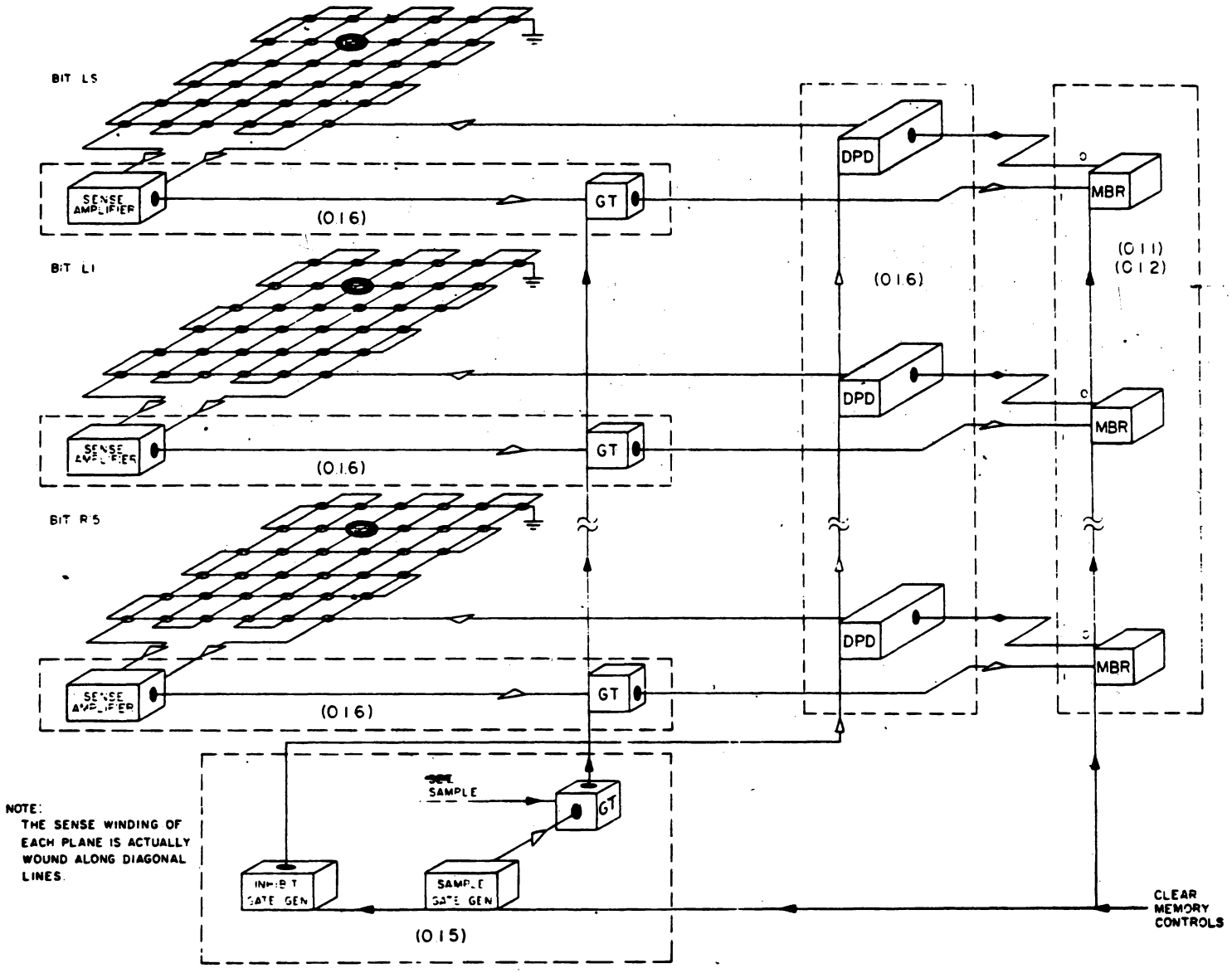
Refer to Pg. 0170

b. The inhibit winding of each digit plane consists of a 1-turn winding which is wound through all the cores of a plane in parallel with the Y selection windings. Because the direction of this winding is alternated in adjacent rows of cores, the inhibit current pulse effectively flows in opposite directions through alternate rows of cores. Since write current pulses (negative) are applied to adjacent Y selection windings in opposing directions, the proper connection of the digit plane driver will cause the individual magnetic fields set up by the inhibit current pulse and the Y selection winding write current pulse in each core of the selected row of cores to completely cancel each other. To illustrate this point, consider the following example, which assumes that the digit plane shown represents the topmost plane of the array. Under this condition, a read-write current driver will be connected to the Y-O selection winding on the right side of the array so that the direction of this winding through this plane will be from right to left. The digit plane driver for this plane is connected to pin I1 of the next lower plane. As a result of the internal array wiring (jumper wires serially connected from pin I1 of the even-numbered plane to pin I8 of the odd-numbered plane), the direction of the inhibit winding through the Y-O row of cores will be from left to right. Since the Y selection winding write current and the inhibit current are flowing in opposite directions, the magnetic fields set up by these two windings will be in opposite directions for each core in the Y-O row of cores. The net result is that these two fields cancel each other in each of the mutually affected cores.

Refer to Pg. 0430 and Logic 0, 1, 7

Refer to Pg. 0450

c. Because the X and Y array selection windings are formed by serially connecting the similarly numbered drive lines of adjacent planes, the direction of read-write current flow in the similarly numbered drive lines of adjacent digit planes will always be in mutually opposing directions. To compensate for the effects of the winding reversal of the similarly numbered X and Y drive lines of adjacent planes, the direction of the inhibit winding must also be



64² Sense and Inhibit Winding Pictorial

reversed in adjacent planes. In the 64^2 ferrite core array, the inhibit winding reversal is accomplished by the physical inversion of alternate planes of the array. To illustrate the manner in which this is accomplished, consider the inhibit winding connections of the odd-even pair of planes shown. From the previous example, it was determined the inhibit winding of an odd-numbered plane is wound through the Y-O row of cores in a left to right direction. Thus, for an even-numbered plane, the inhibit winding must be wound through its Y-O row of cores in a right to left direction. The digit plane driver for an even-numbered plane is connected to pin I1 of the associated odd-numbered plane. As a result of the internal array wiring (jumper wires serially connected from pin I1 of an odd-numbered plane to pin I8 of an even-numbered plane) and because the plane is relatively upside down, the direction of the inhibit winding through the Y-O row of cores of the even-numbered plane will be from right to left.

3. Sense Winding

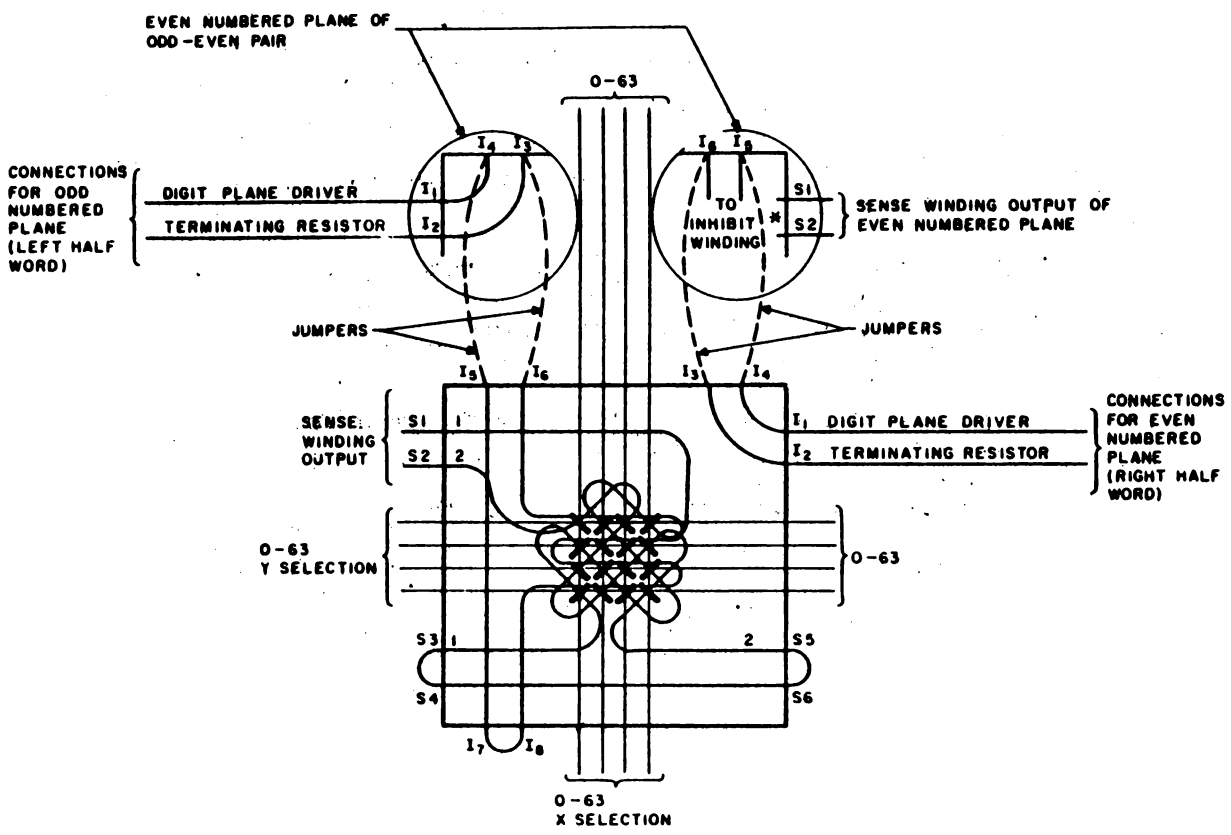
   a. The sense winding of each active digit plane is associated with a differential input sense amplifier which functions to amplify the induced voltages produced by the switching action of each core in the plane. Each digit plane has two separate sense windings (labeled 1 and 2) which are connected in series by means of internal and external jumper wires to form one long winding. Each individual sense winding which passes through half of the cores of the plane follows a diagonal path in order to minimize the capacitive and inductive coupling between itself and the other windings of the plane. The two ends of the sense winding (S1 and S2) are connected to the differential input sense amplifier so that only the induced voltage will be amplified. That is, since capacitive-coupled voltages do not produce a difference voltage between these two terminals, they will be rejected by the amplifier.

Refer to Pages 0440 and 0450

4. The left-half word bits (S-15 and Parity) are processed in Unit 10. The Inhibit and Sense connections for these bits enter on the left rear corner of the array.

Refer to Logic

5. The right-half word bits (S-15) are processed in Unit 12. The Inhibit and Sense connections for these bits enter on the right rear corner of the array.



Top View of 64² Digit Plane (Odd)

C. Summary Questions:

1. Answer the following questions True or False:

   a. One address in memory is a vertical row of 33 cores.

   b. The 18th plane is a dummy plane.

   c. It is necessary to change only four wires when replacing a bad plane with the spare.

   d. Odd numbered plane output are processed in unit 12.

   e. DPD current from unit 10 enters an even plane.

2. Complete the following statements:

   a. There are _____ ferrite core planes in the 64^2 memory array.

   b. Each drive winding goes thru _____ ferrite cores.

   c. Adjacent drive lines have current flowing in _____ directions.

   d. The sense winding was wired in the present manner for cancellation of _____ noise.

   e. Both ends of the sense winding connect to the _____

Core Storage Element

VII. Overall Logic of 64^2 Memory

A. Selection Section

1. Selection of the 64^2 core memory register from which information is to be read, or into which information is to be stored, is controlled by the selection section. This section contains the flip-flop memory address register which is composed of 12 flip-flops. Six of these flip-flops and a diode matrix decoder are associated with the X portion of the selection section; the other six flip-flops and a second decoder are associated with the Y portion. The two portions operate similarly and are controlled simultaneously to select one X and one Y core memory current driver. Since the two portions of the selection section are exactly the same, the following discussion will deal only with selection of an X driver.

   Note: Bit identification

   1. X - MAR - (R10-R15)
   2. Y - MAR - (R4 - R9).
   3. Odd-Even Bits (R9 and R15)
   4. X bits 10-14 are utilized to select one pair of X lines (i.e. 0-1, 2-3, 4-5, etc.). The odd-even bit (R15) is then used to determine which of the two lines is actually selected. If R15 is a "1", the odd line is selected and if a "0", the even line is selected. As opposed to having an AND circuit for each line, this System allows the use of fewer diodes.

Use Page 2890 to select an address

2. At the beginning of each memory cycle, the memory address register flip-flops are reset by a clear-memory-controls pulse from the instruction control element. Approximately 0.6 usec later, new address information is transferred to the memory address register from either the program counter, the address register, or the IO address counter. The output levels from both the 1 and 0 sides of five of the flip-flops (bits R10 through R14) are supplied to the diode matrix decoder, and the output of the sixth flip-flop (R15) is fed to the memory gate generator circuits. The information which the decoder accepts from the five flip-flops is decoded in diode negative AND circuits to select one of 32 output lines. The 31 non-selected lines have an output level of +10V; the selected line has an output level of -30V. The selected output level is amplified by two Matrix Output Amplifiers to partially condition two adjacent core memory drivers, one for an even address and one for an odd address. One of these two drivers is then further selected by the proper memory gate generator. (MGG)

NOTE

The memory gate generators are logical AND circuits, each requiring both a d-c level from the sixth memory address register flip-flop and a read or a write level from the timing and gating section. Four memory gate generators are used, two for reading (read odd, read even) and two for writing (write odd, write even).

3. If the sixth memory address register flip-flop is in the cleared state, the d-c level from its 0 side is at + 10V and conditions the read-even and write-even memory gate generators. When conditioned by a read or a write level from the timing and gating section, these generators activate the read or write lines of the 32 even-core memory drivers and cause the selected current driver to generate a read or write current pulse. If the sixth flip-flop is set, it conditions the read-odd and write-odd memory gate generators, which, in turn, activate the read or write control lines of the 32 odd core memory drivers. When these gate generators are conditioned by a read or a write level from the timing and gating section, the partially selected current driver will generate a read or write current pulse.

NOTE

In the Y selection section, the outputs of bits R4 through R8 are supplied to the diode matrix decoder and the outputs of bit R9 are used to select the odd or even pair or memory gate generators.

4. The X and Y core memory drivers, which are partially conditioned by the diode matrix decoders through the matrix output amplifiers, are further conditioned at the proper time by a read or a write pulse from the selected memory gate generators described above. The selected X and Y drivers supply current pulses to an X and a Y line of the core memory array. These current pulses are of sufficient amplitude and duration to half-select the cores on the respective lines. At the intersection of the two lines, the individual half-select current pulses are algebraically added to apply a full-amplitude current pulse to the selected core. Overall operation of the core memory drivers is the same during the read and the write functions, except that the polarity of the output is reversed.

B. Selection Section Circuits

1. Diode Matrix Decoder (DMD)

NOTE: The following explanation can be applied to the X DMD and/or the YDMD:

a. Comprised of 4 sets of negative AND circuits, each having 8 output lines.

b. Used to select one of 32 possible output lines.

c. Inputs - Zero and one levels from the MAR flip-flops (+10V or -30V.)

d. Outputs - one selected line at -30V, 31 non-selected lines at +10V. Each line feeds 2 Matrix Output Amplifiers.

2. Matrix Output Amplifier (MOA)

a. Comprised of inverter amplifier and cathode follower. (MOA is comprised of 1/2 of 2 tubes.)

b. Used to invert and amplify the DMD signal.

c. Input - one line from DMD feeds 2 MOA's.
   1) Selected input - -30V
   2) Non-selected input - +10V

d. Output - each MOA feeds both grids of 1 Core Memory driver.
   1) MOA - Input +10 Output +10
   2) MOA - Input -30 Output +90

e. 64X MOA's and 64 Y MOA's - 1 per Core Memory Driver.

3. Core Memory Driver (CMD)

a. Comprised of two triode amplifiers housed in one envelope.

b. When selected, one half of tube supplies current during read time and other half during write time.

c. Inputs

   1) Control grid conditioning voltage from MOA (+90 V selected, +10V non-selected).

   2) Cathode conditioning voltage from Memory Gate Generator (+100V selected, +180V non-selected).

Note: "Read MGG" conditions 1 cathode during read time and the write MGG conditions the second cathode during write time.

d. Output - Approximately 410 ma to the associated X or Y winding.

e. 64 X CMD's and 64 Y CMD's - 1 per line,

f. 1 "X" CMD and ' "Y" CMD conduct for 1 given selection.

4. Memory Gate Generator (MGG)

a. Used to half select all odd or all even CMD's (X or Y),

b. Logically comprised of a gate feeding a cathode follower,

c. Inputs (to gate tube)

1) Supressor grid conditioning voltage from odd-even flip-flops (R9 or R15). (+10V selected, -30V non-selected.)

2) Control grid conditioning voltage from Read or Write FF. It should be noted that this input is capacity coupled.

d. Output - conditioning level to cathode of 32 CMD's,

Note: Cathode resistance of the MGG cathode follower is variable to be able to adjust the amount of current through the CMD's.

e. 4 X MGG's and 4 Y MGG's.

Note: The following breakdown can be used to illustrate either the X MGG's, the Y MGG's or both. In the examples given, X MGG's will be assumed.

1) Read Even MGG

a) Conditioned when the Read FF is Set and the Odd-Even FF (Bit 15) is clear.

b) Conditions the "Read" portion of the 32 even CMD's.

2) Read Odd MGG
   a) Conditioned when both the Read FF and the Odd-Even FF (Bit 15) are set.
   b) Conditions the "Read" portion of the 32 odd CMD's.

3) Write Even MGG
   a) Conditioned when the Write FF is Set and the Odd-Even FF (Bit 15) is clear. Conditions the "Write" portion of the 32 even CMD's.

4) Write Odd MGG
   a) Conditioned when both the Write FF and the Odd-Even FF (Bit 15) are set.
   b) Conditions the "Write" portion of the 32 oddCMD's.

Note: Each MGG conditions 32 cathodes. It should also be noted, however, that only one of these 32 should have its grid conditioned at the same time. Therefore, during read time the read portion of only 1 X CMD should conduct and during write time the "write" portion of the same CMD should conduct. Since the Y circuitry is identical, it can be seen that 1X and 1 Y CMD conduct for any given selection. 1 MGG can supply sufficient current for only 1 CMD. If, due to some malfunction, an attempt is made to drive 2 or more CMD's the selection will fail.

C. Sense Section and Memory Buffer Register

1. The sense section of the 64^2 core memory consists of 33 amplifiers and 33 gate tubes, one set for each plane of the core memory array. Each individual sense amplifier amplifies the output voltages induced in the sense winding of the associated plane.

2. The output of a sense amplifier - a nonstandard pulse which is positive regardless of the polarity of the input signal - is applied to and conditions a gate tube circuit. If the selected core contains a 1 prior to being read out, the gate tube, when sampled, provides the standard pulse required to activate the memory buffer register. The gate tube is sampled by a standard pulse gated by the sample gate generator. The time relationship between the sense amplifier output and the sample pulse is adjusted so that the sample pulse occurs at approximately the peak of an amplified 1 output signal. Thus, if a core containing a 1 is read out during a readout cycle, the sampled gate tube develops an output which sets the associated memory buffer register flip-flop to the 1 state. If the core contains a 0, the flip-flop remains in the 0 state.

3. The output of the 0 side of the memory buffer register flip-flop conditions an associated digit plane driver in order to provide the necessary control to subsequently restore the original content to the selected core. If the core contains a 1 prior to readout, the X and Y write current pulses write a 1 back into the core. However, if the core contains a 0 prior to readout, the associated digit plane driver is conditioned, resulting in the generation of an inhibit current pulse (coincident with the X and Y write current pulses) which prevents the writing of a 1, thus effectively writing a 0.

D. Inhibit Section

Note: For most Memory Cycles, the same information that is read from a location is replaced in that location. Since it is inherent in this system that, when writing is performed we always try to write a "1", some system must be introduced to allow the retention of a zero where a zero is desired. This is the function of the Inhibit Section.

1. The digit plane driver section consists of 33 functionally identical circuits, one corresponding to each active plane of the core memory array. These circuits function to supply the inhibit current pulses to the associated planes.

2. The output of a digit plane driver is a negative current pulse having an amplitude of approximately 410 ma. Because of the inhibit winding geometry, the inhibit current pulse has the same effect as a half-select current pulse in the read direction. To inhibit the writing of a 1, the inhibit current pulse (effectively + 1/2 amp) adds algebraically to the X-write current pulse (- 1/2 amp) and the Y-write current pulse (- 1/2amp) to produce an effective field of - 1/2amp turns . (+ 1/2) + (- 1/2) + (- 1/2) = - 1/2

3. The input stage of each digit plane driver consists of a gate tube which is conditioned by the 0 side of the associated memory buffer register flip-flop when the selected core contained a 0. The other input to this gate tube is supplied by the inhibit gate generator, which is located in the timing and gating section. The output of the gate tube supplies a cathode follower, a differential amplifier, and a d-c power amplifier which drives the low-impedance, high-current inhibit winding of the core memory array plane.

note: Logic 0.1.7 should indicate DPD inputs from memor buffer FF come from B2 pins (clear outpu of FF)

E. Timing and Control Section

1. The timing and gating control section of the 64^2 core memory receives the start-memory pulse from the program element for both types of memory cycles and during the

execution of a memory "store" cycle, this section also receives The inhibit-sample pulse from the instruction control element. The timing and gating section provides the three gate signals and the sample pulse to operate the various portions of the core memory in proper sequence.

2. Clear Memory Controls - TP-O

Refer to Logic 0.1.4

a. Clear MAR to all 1's
b. Clear Sample FF

Note: The read and write FF's (X & Y) and the inhibit FF's (left and right) will be clear at this time as a result of the last memory cycle.

3. Start Memory

a. PT-O delayed
b. OT-O delayed
c. BI-O delayed
d. BO-O delayed

4. The start-memory pulse is applied to the memory time pulse distribuotr, which is a chain of delay lines. The start-memory pulse delayed 0.1 usec is used to set the read-gate generator. This is subsequently cleared by the start-memory pulse delayed approximately 2.2 usec. The 1-side output of the read gate generator, which is a positive pulse, is applied to the selection section and determines the timing and duration of the read-current pulse that is supplied to the selected X and Y driver lines.

5. The sample gate generator of the timing and gating section deffers from the other gate generators in this section in that the O-side output controls a gate tube which is sampled by the sample pulse from the memory time pulse distributor. During a memory "readout" cycle, the inhibit-sample pulse is not generated, and the sample gate generator remains in the o state. In this condition, the gate passes the sample pulse to the sense section approximately 2.0 usec after the start memory pulse is initiated. During the memory "store" cycle, an inhibit-sample pulse from the instruction control element is supplied to the sample-gate-generator flip-flop, setting the flip-flop to the 1 state. Thus, the gate tube is deconditioned when sensed by the sample pulse.

a. OT "B" -3 on Store class instruction

b. BI -3 on an I/O operation

c. Sets Sample FF which inhibits the sample pulse. This prevents the information read from the selected address from being placed in the Memory buffers. Therefore, new information can be placed in the buffers and, during the write cycle, this new information will be placed into the selected register.

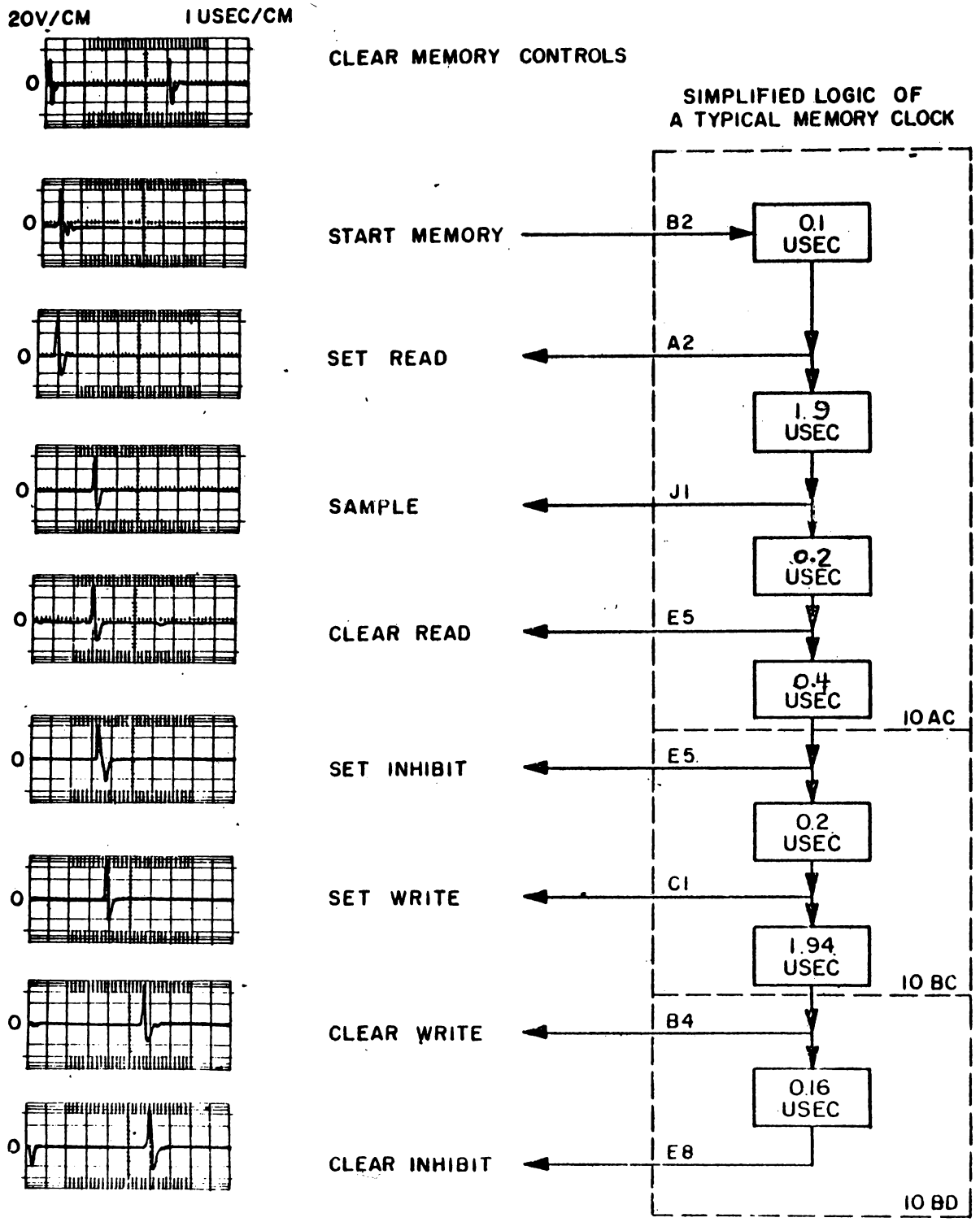
6. The write-gate-generator flip-flop receives a set-write pulse from the memory time pulse distributor approximately 2.8 usec after the start-memory pulse is initiated and receives a clear-write-gate-generator pulse approximately 1.9 usec later. The resultant output pulse from the write-gate-generator flip-flop, which is approximately 1.9 usec in duration, is applied to the selection section and determines the timing and duration of the write current pulse that is supplied to the selected X and Y driver lines.

7. The inhibit gate generator is similar to the read and write gate generators in operation and function. The set-inhibit pulse is supplied by the memory time pulse distributor approximately 2.6 usec after the start-memory pulse is initiated. The clear-inhibit pulse (from the same source) is received approximately 4.9 usec after the start-memory pulse is initiated. The 1-side output pulse of the inhibit-gate-generator flip-flop is approximately 2.3 usec in duration and overlaps the write-gate-generator output. The inhibit gate is applied to the 33 digit plane drivers; however, only the drivers which are conditioned by the associated memory buffer register flip-flops can generate an inhibit current pulse.

8. Outputs from clock

a. Set Read X & Y (SM / .1) Refer to Page 0550
b. Sample Pulse (SM / 2.0)
c. Clear Read X & Y (SM / 2.2)
d. Set Inhibit (SM / 2.6)
e. Set Write (SM / 2.8)
f. Clear Write (SM / 4.7)
g. Clear Inhibit (SM / 4.9)

NOTE: Clock is merely a series of delays; once started, it cannot be stopped.



MEMORY PULSE DISTRIBUTOR, WAVEFORM ANALYSIS

F. Summary Questions:

1. Answer the following questions True or False:

   a. An MGG is conditioned by two -30V levels.

   b. Four MGGs will be fully selected each memory cycle.

   c. After a memory cycle is once started it cannot be stopped by normal computer operation.

   d. No sample pulse leaves the memory clock during a store cycle.

   e. The memory clock is a series of delays.

2. Complete the following statements:

   a. When selecting a "Y" address, bits _____ are used.

   b. Bits _____ determine whether even or odd addresses will be selected.

   c. The DMD is used to select one of _____ possible lines and the selected line output voltage is _____.

   d. The output of the DMD will condition two _____ whereby the DMD output voltage is _____ and amplified.

   e. The CMD will be conditioned by the _____ and the _____.

   f. Outputs of the Read/Write FF and Odd/Even FF will condition the _____.

   g. The _____ will be conditioned by the zero side of the Memory Buffer FF and will produce _____ of current.

   h. Approximately _____ will be induced in the _____ winding when a selected core is switched from a one to a zero.

   i. Inhibit current flows through a core in the same direction as the _____ current in _____ winding.

   j. There are _____ CMDs in each 64^2 memory.

   k. There are _____ MOAs in each 64^2 memory.

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VIII. Diode Matrix Decoder

A. Operation

1. The following explanation is for the Y DMD, but, with the exception of bit designations, it could also apply to the X DMD. Refer to Page 0590

   a. The "power" and "not power" philosophy (i.e. 2^7 and 2^{-7})

      1) Bits are labeled from the least significant bit of a word (R15) towards the most significant bit (R4 in this case.)

      2) The "0" power is then used to indicate the least significant bit and as progression is made toward the most significant bit, 1 power is added for each bit (i.e. R15 = "0", R14 = 1, R13 = 2, R4 = "11").

      3) The "power" (2^7) and "not power" (2^{-7}) are used to indicate respectively the set and clear sides of the R8 F.F.

   b. DMD is divided into 4 equal Sections which are located on the 4 Y driver panels. (YA, YB, YC & YD).

      1) YA feeds lines $0\text{-}15_{10}$ (0-178).

      2) YB = $16\text{-}31_{10}$ ($20\text{-}37_8$)

      3) YC = $32\text{-}47_{10}$ ($40\text{-}57_8$)

      4) YD = $48\text{-}63_{10}$ ($60\text{-}77_8$)

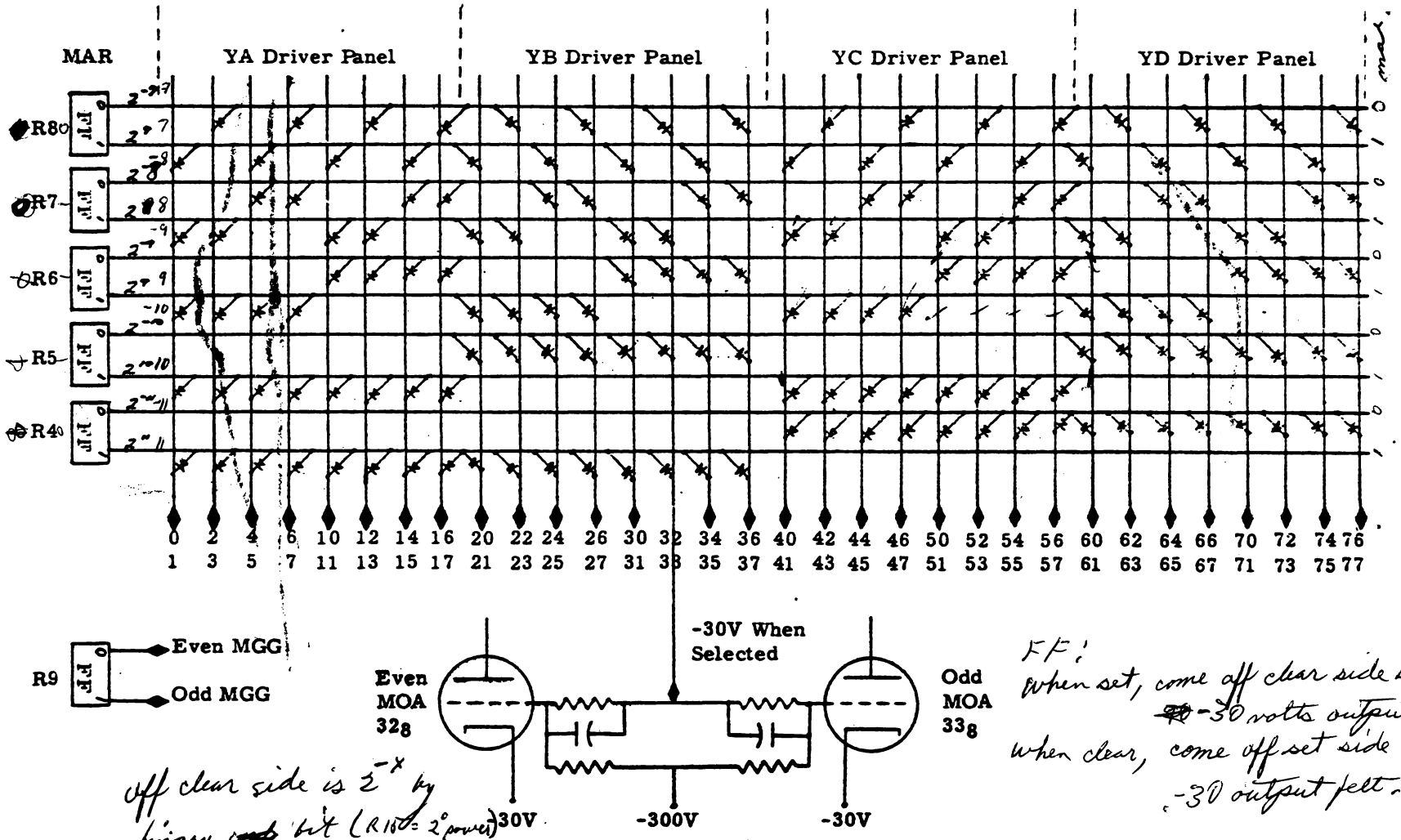
2. Load the Y MAR F.F.'s with 34_8 and develop the negative AND circuit which will condition line 34_8 - 35_8 coming out of the Y DMD. It should be noted that a Y selection of 35_8 brings this line up also. Refer to Page 05

   a. With 64_{10} possible Y selections, it can be seen at this time that, with the use of the Odd-Even bit, there need only be 32_{10} negative AND cir cuits feeding out of the DMD since each output feeds 2 Y MOA's which in turn feed 2 Y CMD's. The one actually used will be determined by the Odd-Even bit.

3. The action of Open and Shorted diodes. Refer to Page 06

   a. Open diode

      1) The line containing the open diode will select



off clear side is 2^{-x} by binary bit (R180 = 2° power)

off set side is 2^{x} by binary bitposition (R 7 = 2^{8})

FF:
when set, come off clear side so that -30 volts output is felt
when clear, come off set side so that -30 output felt.

0590

TEST CHART FOR DIODE MATRIX DECODER

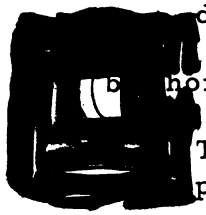
Matrix Diodes	*Octal Address Groups
2^1 or 2^7	0, 1, 4, 5, 10, 11, 14, 15, 20, 21, 24, 25, 30, 31, 34, 35, 40, 41, 44, 45, 50, 51, 54, 55, 60, 61, 64, 65, 70, 71, 74, 75.
2^{-1} or 2^{-7}	2, 3, 6, 7, 12, 13, 16, 17, 22, 23, 26, 27, 32, 33, 36, 37, 42, 43, 46, 47, 52, 53, 56, 57, 62, 63, 66, 67, 72, 73, 76, 77.
2^2 or 2^8	0, 1, 2, 3, 10, 11, 12, 13, 20, 21, 22, 23, 30, 31, 32, 33, 40, 41, 42, 43, 50, 51, 52, 53, 60, 61, 62, 63, 70, 71, 72, 73.
2^{-2} or 2^{-8}	4, 5, 6, 7, 14, 15, 16, 17, 24, 25, 26, 27, 34, 35, 36, 37, 44, 45, 46, 47, 54, 55, 56, 57, 64, 65, 66, 67, 74, 75, 76, 77.
2^3 or 2^9	0-7, 20-27, 40-47, 60-67.
2^{-3} or 2^{-9}	10-17, 30-37, 50-57, 70-77.
2^4 or 2^{10}	0-17, 40-57.
2^{-4} or 2^{-10}	20-37, 60-77.
2^5 or 2^{11}	0-37.
2^{-5} or 2^{-11}	40-77.

Note: *In the listed data, a diode is shorted if all the addresses in the group fail except two. The address pair that does not fail contains the defective diode.

properly but will cause a failure when some other line is selected.

EXAMPLE: Assume the diode connecting line "0-1" to the 2" F. F. (R4) is open. When a selection of "0" or "1" is made the circuitry, operates properly. However, when a selection of 40_8 or 41_8 is made, this selection plus line "0-1" will be at -30 volts, this will cause the selection to fail since the selected MGG will be trying to drive 2 CMD's and it is not capable of doing this.

Refer to Page 0590



b. Shorted diode

The line containing the shorted diode will select properly but will cause a failure when various other lines are selected.

Refer to Page -590

EXAMPLE: Assume the diode connecting the "0-1" line to the 2" F. F, is shorted. When a selection of "0" or "1" is made, the circuit operates properly. However, any other selection which has a "0" in the bit R4 position will fail since this will cause the 2" line to go to -30V and will cause the "0-1" line to be selected.

NOTE: Work several problems with open and shorted diodes.

B. Summary Questions:

1. Answer the following questions True or False:

   a. 2^7 represents the clear side of a FF when the FF is set.

   b. Five diodes are used on each DMD output line.

   c. Each Y driver panel will half select 32 drive lines.

   d. Each selected DMD output conditions two MOA circuits.

   e. An open diode in the DMD can cause two lines to be selected at one time.

   f. A negative AND circuit is the same as an OR circuit.

2. Troubleshooting Questions
   a. Diode feeding X address line 26, 27 from the 2^5 FF is open. This will cause what other X address line to be selected simultaneously with 26, 27?
   b. Diode feeding Y address line 52, 53 from the 2^8 FF is open. This will cause what other Y address line to be selected simultaneously with 52, 53?

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c. Diode feeding Y address line 42, 43 from the 2^{10} FF is open. This will cause what other Y address to be selected simultaneously with 42, 43?

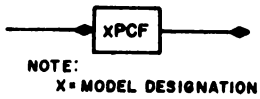
d. Diode feeding X address line 74, 75 from the 2^{-3} FF is open. This will cause what other X address line to be selected simultaneously with 74, 75?

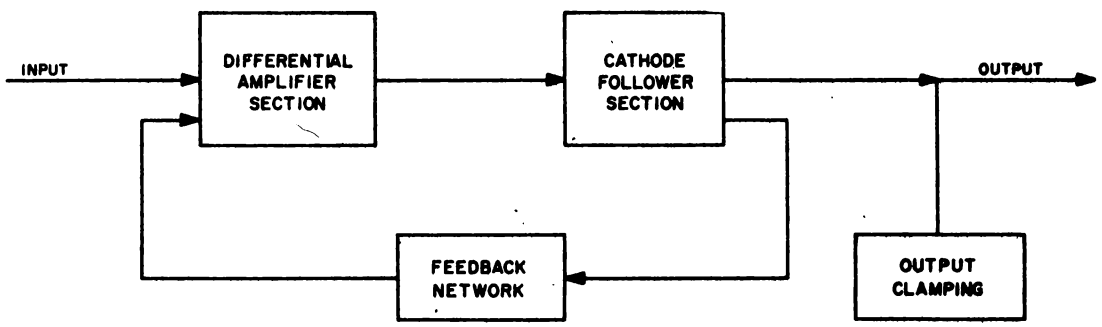
A. Power Cathode Followers

1. Function

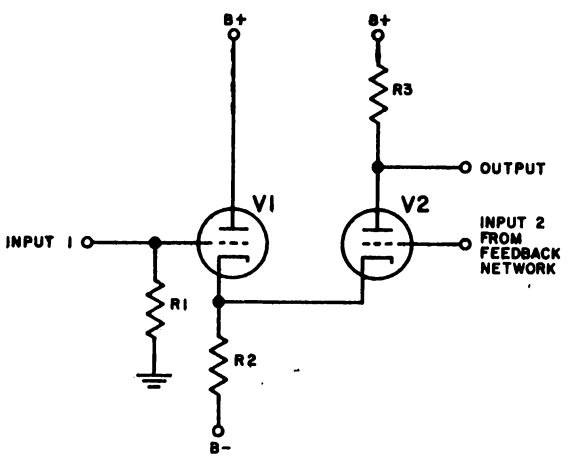
a. The power cathode follower (PCF) is a nonlogic circuit that amplifies power. It is essentially a modified cathode follower circuit designed to satisfy the comparatively large power requirements of specific types of loads. Its high-input and low-output impedance makes the circuit particularly useful as an isolating device, driving low-impedance loads from a high impedance source. Circuit features are incorporated into the PCF to regulate the output levels and to maintain or shape the output waveform.

b. There are 25 models of the PCF employed in AN/FSQ-7 and AN/FSQ-8 equipment, each adapted to the driving requirements of its respective load. For example,





Power Cathode Follower, Block Diagram



Differential Amplifier, Simplified Schematic Diagram

some PCF's are specifically designed to amplify pulse power, others to amplify level power; some PCF's are employed to drive only resistive loads, others to drive only capacitive loads, and still others to feed resistive-capacitive loads. Each of the 25 models belongs to one of two general groups: standard PCF's and special PCF's.

Refer to Page 0670

c. All of the 18 standard PCF's have the same general circuit configuration; each circuit consists of an input differential amplifier section and an output cathode follower section. Degenerative feedback is employed between the sections to stabilize the output voltage. The output is clamped at its lower level. The most significant difference between the standard PCF's is the number of parallel sections in the output cathode follower section. If the rated plate current of a single tube is insufficient to provide required power output, one or more triode sections are added in parallel. The next most significant difference between these models is the value of cathode output resistors. A large cathode output resistance is desirable when driving a resistive load; a small cathode output resistance would make for a fast fall time where a capacitive load is fed. A compromise value is used for a resistive-capacitive load.

Refer to Page 0630 and Logic 0.1.5 (c PCF's)

2. Principles of Operation

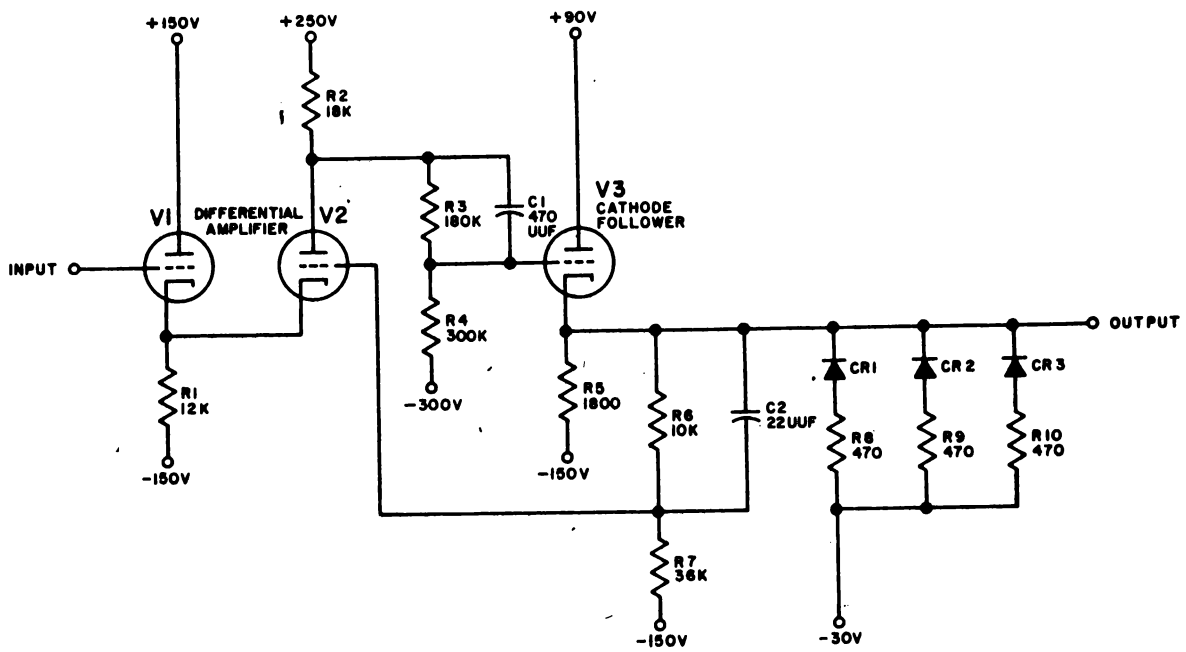
a. All PCF's both standard and special, consist of an input differential amplifier and an output cathode follower section. Specific models employ degenerative feedback to stablize the output voltageand output clamping to protect subsequent circuits. The feedback is applied to the differential amplifier, and in effect, adjusts the voltage applied to the cathode follower section maintaining the PCF output at a constant level for a given input level.

Refer to Page 0630

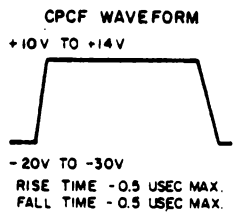
b. A simplified differential amplifier consists of a cathode follower (V_1) and an amplifier (V_2). The inputs (input 1) to the cathode follower section of the differential amplifier are usually +10V and -30V levels. The output of V1 is direct-coupled to the cathode of V2 (common cathode resistor R1 is used.) The other input (input 2) to amplifier V2 is a portion of the output voltage of the PCF. Amplifier V2 amplifies the difference in potential between its grid and cathode.

Refer to Page 0650

c. If the PCF output voltage should rise for a given input, the feedback to the grid of V2 becomes more positive and the plate voltage drops. This decrease in plate voltage in turn causes the output voltage to drop.



Power Cathode Follower, Model A, Schematic Diagram



POWER CATHODE FOLLOWER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Speedup capacitor
C2	Feedback capacitor (speedup) reducing positive and negative overshoot
CR1, CR2, CR3	Output clamping diodes
R1	Common cathode resistor for V1 and V2
R2	Plate load resistor for V2
R3, R4	Voltage divider
R5	Cathode resistor for V3
R6, R7	Feedback voltage divider network
R8, R9, R10	Current limiting and equalizing resistors for CR1, CR2, and CR3, respectively

3. Standard Power Cathode Followers

a. Since all the standard PCF's are basically the same, only the model A (aPCF) will be discussed in detail.

b. The nominal inputs to the aPCF are +10V and -30V levels. With the input at +10V the common cathodes of V1 and V2 are approximately +11V. Assuming that there is an output voltage of +13.5V at the cathode of V3, the grid of V2 is set at a voltage (+7V) determined by the attenuating network composed of resistors R6 and R7. The resultant voltage at the grid of V2 holds the tube close to cutoff, fixing the plate potential at +194V. A proportionate voltage is applied to the grid of the output circuit through voltage divider network R3 and R4 (+10V), which causes V3 to conduct heavily and maintain the output voltage at +13.5V. Refer to Page 0650

c. If the output voltage drifts below +13.5V, the voltage at the grid of V2 falls. This causes a reduction in plate potential of V2 and a resultant increase in the plate potential of V2 and the grid of V3. With a more positive grid, the plate current through V3 increases, causing the output voltage to rise to +13.5V. Similarly, if the output voltage drifts positive, the grid of V2 becomes more positive, increasing conduction and lowering the plate potential of V2 and the grid potential of V3. This reduces the plate current of V3 and causes the output voltage to fall to +13.5V.

d. Assume that the input level is now -30V; the common cathode potential of V1 and V2 is approximately -26V. With an output of -32V (balanced condition), the voltage fed back to the grid of V2 is -28V. The resultant bias on the grid of V2 fixes the plate voltage of V2 at +100V. As a result of voltage divider R3 and R5, the grid voltage of V3 equals -50V and an output voltage of -32V is developed at the cathode of V3. Changes in this output level are fed back to the grid of V2, causing the output to be restored to its normal level in the same manner as described above.

e. Capacitor C1 compensates for the transition time loss caused by voltage divider R3 and R5. Capacitor C2 is a speedup capacitor in the feedback network which reduces positive and negative overshoot in the circuit. Clamping diodes CR1, CR2, and CR3 protect subsequent circuits should the +90V supply fail and also clamp the lower output level at approximately -32V.

POWER CATHODE FOLLOWER, MODEL-DISTINGUISHING CHARACTERISTICS

	INPUT LEVELS		STAGE COMPLEMENT						OUTPUT LEVELS	
				DIFFERENTIAL AMPLIFIER			OUTPUT SECTION			
MODEL	UPPER (volts)	LOWER (volts)	INPUT CATHODE FOLLOWER	CATHODE FOLLOWER	AMPLIFIER	INTER-MEDIATE DRIVER	CATHODE FOLLOWER	OUTPUT RESISTANCE	UPPER (volts)	LOWER (volts)
A	+10	−30	—	1	1	—	1	1.8K	+12.75 ±2.75	−32.5 ±2.5
B	+10	−30	—	1	1	—	1	1.8K	+12.75 ±2.75	−16 ±1
*C	+10	−30	1	—	—	—	8	3.7K	+12 ±2	−25 ±5
*E	+10	−30	2	2	2	1	3	600	+6.5 ±1.5	−24 ±4
F	+10	−30	—	1	1	—	2	27K	+12.75 ±2.75	−30.5 ±3.5
G	+10	−30	—	1	1	—	4	27K	+13.4 ±3.4	−30 ±4
H	+10	−30	—	1	1	—	3	900	+13.5 ±1.5	−24 ±4.0
J	+10	−30	—	1	1	—	3	700	+12.0 ±2.0	−32 ±2
K	+10	−30	—	1	1	—	1	450	+13.0 ±3.0	−29 ±3
N	+10	−30	—	1	1	—	4	450	+5.5 ±5.5	−24.5 ±4.5
P	+10	−30	—	1	1	—	4	600	+13.0 ±4.0	−30 ±5.0
*Q	+10	−30	1	2	2	—	4	1.8K	+12.55 ±1.25	−30 ±3.0
R	+10	−30	—	1	1	—	10	200	+5.5 ±5.5	−24 ±4.0
S	0	−15	—	1	1	—	8	900	+3.35 ±3.35	−23 ±3.0
T	+10	−30	—	1	1	—	2	980	+12 ±2.0	−26.5 ±5.5
U	0	−24	—	1	1	—	2	3K	+5.0 ±5.0	−30.5 ±1.5
V	0	−24	—	1	1	—	2	1.8K	+5.0 ±5.0	−30.5 ±1.5
W	+10	−30	—	1	1	—	3	640	+12 ±2.0	−30.5 ±2.5
Y	+10	−30	—	1	1	—	6	320	+5.0 ±5.0	−16 ±1.0
Z	+10	−18	—	1	1	—	3	900	+8.0 ±5.0	−16 ±1.0
*AA	+10	−30	—	—	1	—	1	1.8K	+12.5 ±2.5	−31.5 ±1.5
*DD	+10	−30	—	1	1	—	4	900	−27	−61.5 ±6.0
FF	+10	−30	—	1	1	—	2	1.2K	+12.0 ±3.0	−30 ±2.0
**GG	+10	−21	1	**	**	—	1	3.2K	+12.5 ±2.5	−30
*HH	+10	−30	—	2	2	1	5	360	+12 ±2.0	−33 ±3.0

Special power cathode followers
**Grounded grid amplifier used instead of differential amplifier*

Core Storage Element

4. Special Power Cathode Followers

   a. The special PCF's are modified standard PCF's. Therefore, since the fundamental building block of these PCF's is a standard PCF, the special PCF's will only be discussed in terms of their modifications with respect to the aPCF.

      NOTE: cPCF used in conjunction with MAR FF's.

   b. The cPCF consists of an input cathode follower which feeds a PCF output section made up of eight parallel cathode followers. The cPCF does not employ an input differential amplifier section and therefore does not contain a feedback loop.

      NOTE: ePCF used in conjunction with IGG FF's.

   c. The ePCF is employed as a pulse power amplifier instead of a level power amplifier. The input stage is an isolation cathode follower comprising two triodes in parallel whose output is capacitively coupled to a differential amplifier. The output of the differential amplifier is applied to the output cathode follower section through an intermediate driver stage.

B. Matrix Output Amplifier

1. Function

a. The matrix output amplifier (MOA) is a logic DC amplifying circuit which provides signal inversion and a shift in output signal level to either partially condition or decondition a core memory driver. There are 128 MOA circuits used in each 64^2 core memory element.

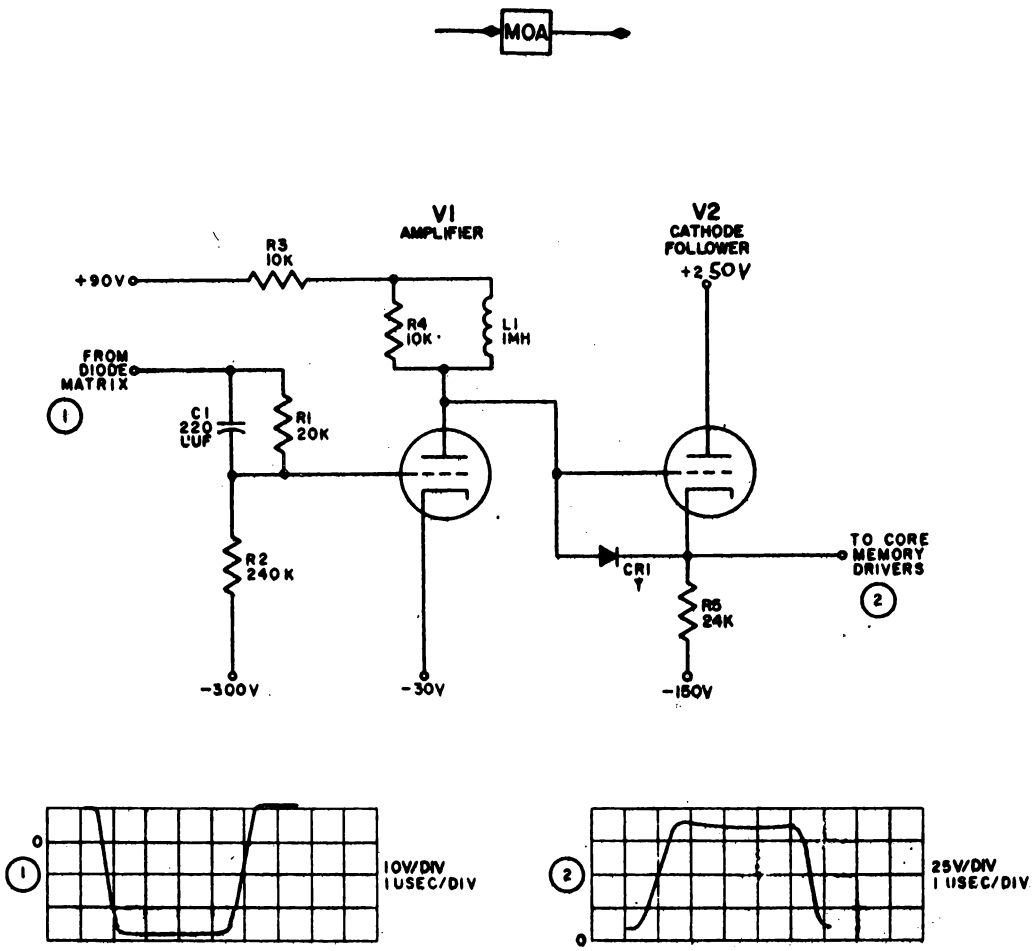
2. Principles of Operation

a. The circuit consists of a d-c amplifier (V1), a cathode follower (V2) and associated circuits.

Refer to Page 0700 and Logic 0.1.5

b. The input signal is applied to the voltage divider network consisting of R1 and R2. When the input signal level is at +10V, the divider network functions to lower the signal level applied to the grid of V1. Because of a high postive grid bias on V1, grid current flows in this tube, causing it to conduct heavily and resulting in the plate voltage dropping from +90V to approximately +10V.

c. When the input signal is a -30V level the grid signal applied to V1 is -50V. Consequently, no plate current flows in this tube, making the output rise to approximately +90V.



Matrix Output Amplifier, Schematic Diagram

MATRIX OUTPUT AMPLIFIER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Voltage divider network
R3	Part of plate load (with L1).
R4	Damping resistor
R5	V2 cathode load
C1	Input compensating capacitor
L1	Choke serving as peaking coil in V1 plate load
CR1	Crystal diode prevents V2 grid from becoming more than 1V positive with respect to cathode.

Information

d. The operation of V_2 is that of a standard cathode follower circuit.

C. Core Memory Driver

1. Function

a. The core memory driver (CMD) is a logic AND circuit which is capable of generating bidirectional output current pulses. There are 128 CMD's used in the core memory element. Each CMD supplies read and write current pulses to one X or Y line of a core memory afray. The nominal value of these current pulses is equal to one-half the current needed to switch a ferrite core. Only one X and one Y core memory driver is fully selected at any one time.

2. Principles of Operation

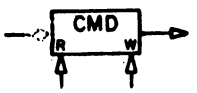
a. The circuit consists of a dual triode (V1) one half of which drives read pulses and the other half of which drives write pulses. The plates of the tube are connected to a center-tapped pulse transformer.

Refer to page 0720 and logic 0.1.5

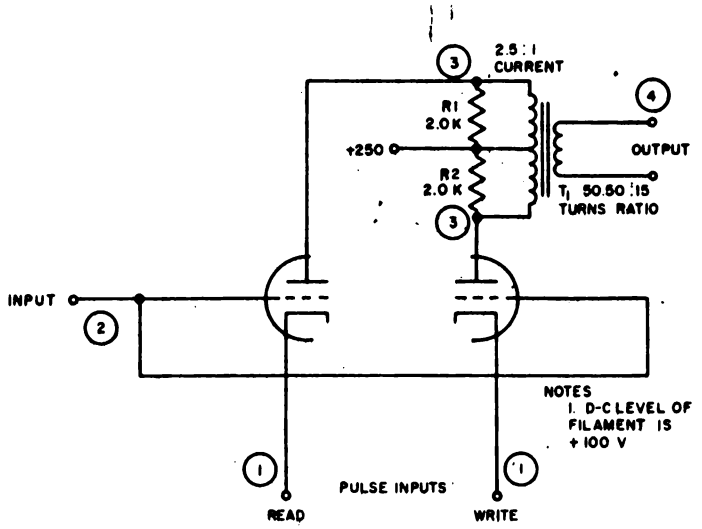
b. An unselected matrix output amplifier applies approximately +10V to the grids of V1. The cathodes are held at +180V by the memory gate generator outputs to which the cathodes are connected. As long as these cathodes are held at +180V, the CMD tubes will not conduct since the input from the matrix output amplifier is not sufficient to overcome the positive cathode potential.

c. When a read pulse is applied to the read memory gate generator, the output of the generator falls toward -300V but is caught at about +90V. This lowers the bias on the CMD, permitting the read side of V1 to conduct. When the read side of V1 is conductiong a current flows in the pulse transformer secondary. The polarity of this current is defined as the read direction. The current ratio of the polse transformer is 2.5 to 1. Consequently, a primary current of 160 ma produces a current of 400 ma in the secondary. A current of this magnitude is necessary to drive a core to the coincident current method of core selection used in the memory element.

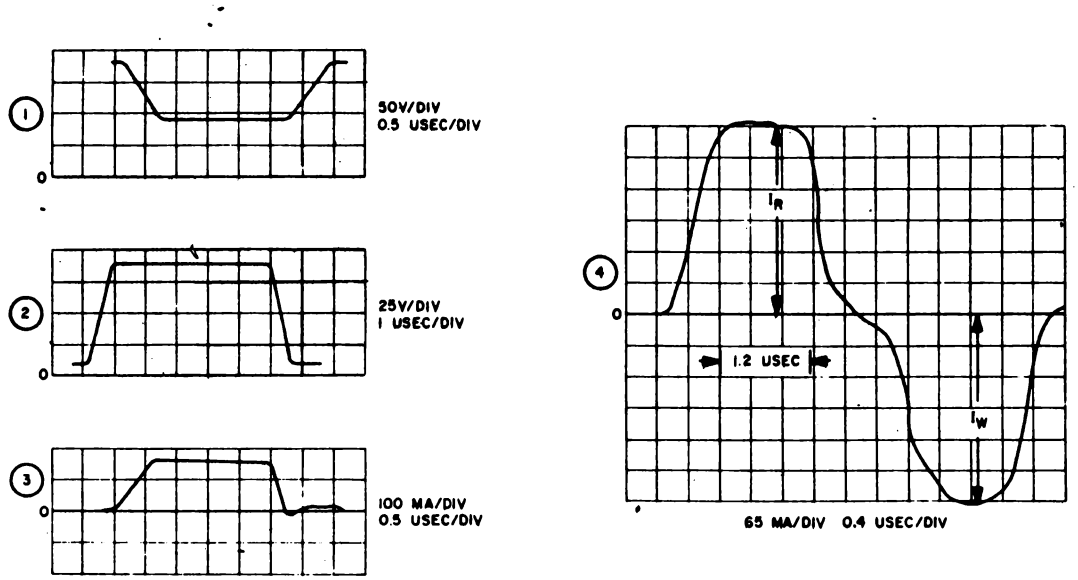
d. When a write pulse is applied to the write cathode of V1, the other half-tube conducts; since this current is in the opposite direction in the pulse transformer primary, the secondary current is of opposite polarity to equal to the read pulse, depending on how the memory gate generator output is adjusted.



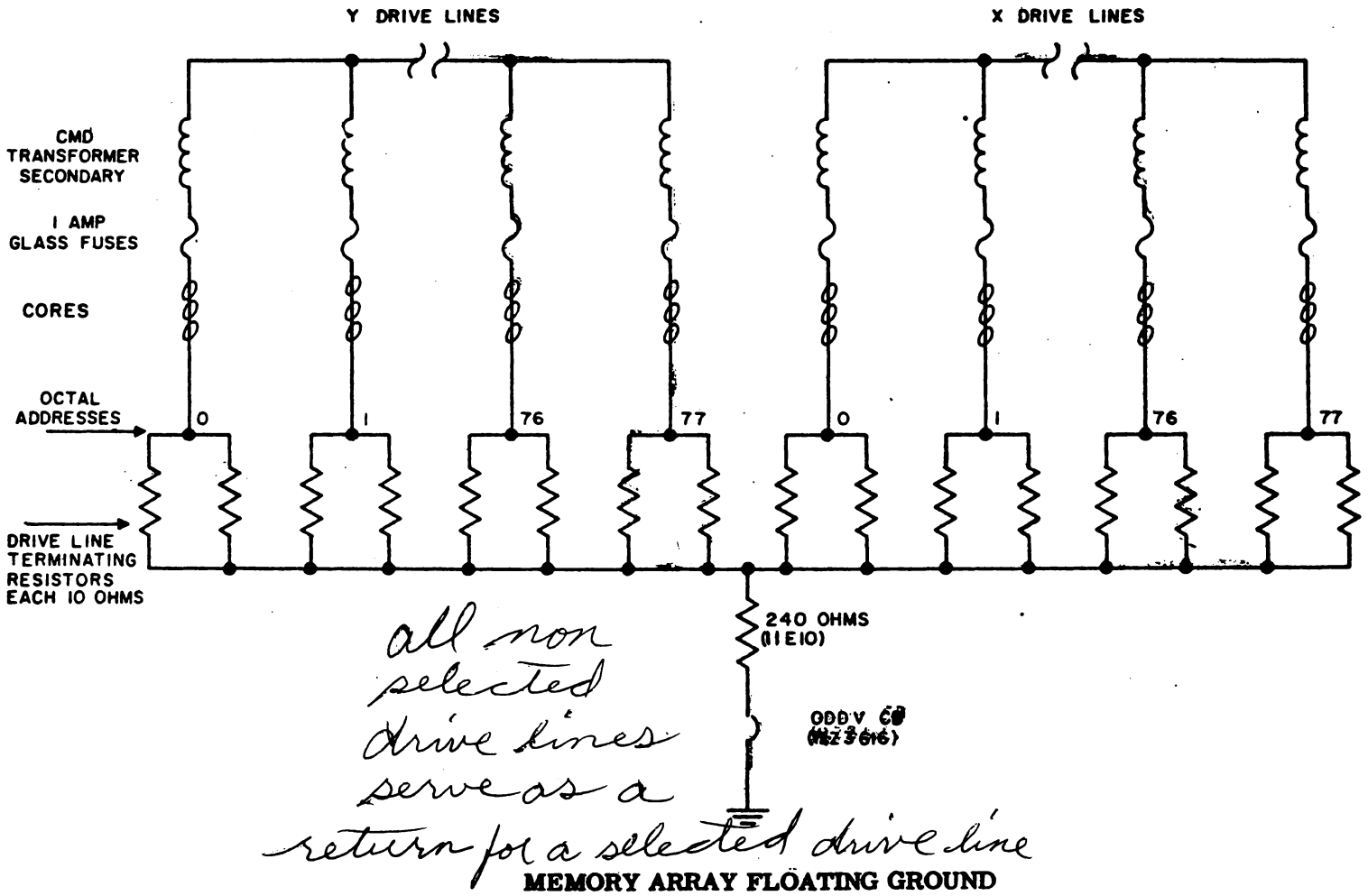
Core Memory Driver,
Logic Block Symbol



VI



Core Memory Driver, Schematic Diagram


Y DRIVE LINES
X DRIVE LINES
CMD TRANSFORMER SECONDARY
1 AMP GLASS FUSES
CORES
OCTAL ADDRESSES
0
1
76
77
0
1
76
77
DRIVE LINE TERMINATING RESISTORS EACH 10 OHMS
240 OHMS (1E10)
all non selected drive lines serve as a return for a selected drive line
MEMORY ARRAY FLOATING GROUND

0730

D. Memory Array Floating Ground - Odd Voltage CB

1. The drive-line paralleled 10-ohm terminating resistors (effective load of 5 ohms) are not returned directly to ground because it was found that such a connection introduced noise on the drive lines, resulting in lowered margins. Hence, an accidental ground such as may be introduced during troubleshooting (solder splash or other foreign matter) will adversely affect margins.

Refer to Page 0730 and Logic 0.1.7

2. The inclusion of the ODD V circuit breaker (CB) was dictated by good design practice. Since the memory array operates better without a ground connection, a safety hazard condition arose based on the possibility of a short developing between the primary (250V) and secondary windings of the CMD transformer. Under these conditions, the memory array would be hot and maintenance personnel working on it would be endangered. Protection against this possibility is afforded by the CB. The 240-ohm resistor, in addition to limiting the current through the CB, further isolates the memory array from ground.

3. Summarizing: for best operation, the memory array must be maintained above ground. In addition , for safety reasons, the memory array must be returned to ground. Both conditions are satisfied by the use of the 240-ohm resistor and the CB (which has an inherent resistance of approximately 130 ohms) in a floating-ground arrangement.

E. Memory Gate Generator

1. Function

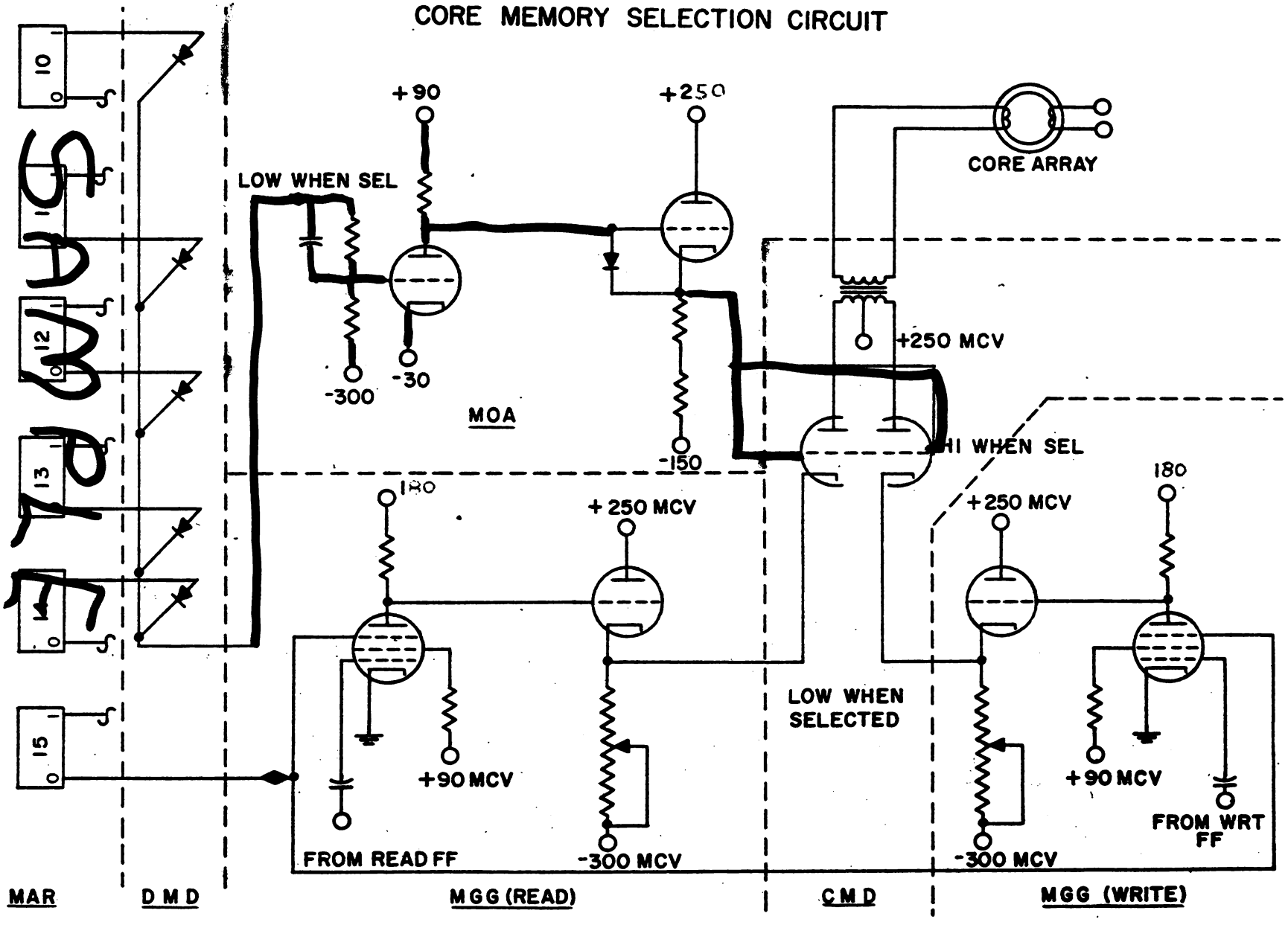
a. The memory gate generator (MGG) is a logic vacuum tube AND circuit and power amplifier which controls the read or write pulses of one of 32 core memory drivers in the Central Computer

Refer to P, 0750

2. Basic Operation

a. The input signal to the suppressor grids of V1 and V2 is a d-c level of either +10V or -30V. When the suppressor grid is at the -30V level, the tubes are completely cut off, regardless of the signal applied to the control grid. When the suppressor grid is at the +10V level, the tubes are partially conditioned and plate conduction will occur when a positive pulse signal is applied to the control grids. The voltage divider consisting of R1 and R2 keeps the plates of V1 and V2 at +180V when the tube is cut off and at +40V when the tubes are conducting. The output voltage of V1 and V2 is fed to the control grids of V3 and V4.

Refer to page 0770 and Logic 0.1.9


CORE MEMORY SELECTION CIRCUIT
10
11
12
13
14
15
0
+90
+250
LOW WHEN SEL
CORE ARRAY
+250 MCV
-300
-30
MOA
-150
HI WHEN SEL
180
+250 MCV
180
+250 MCV
LOW WHEN SELECTED
+90 MCV
+90 MCV
FROM WRT FF
FROM READ FF
-300 MCV
-300 MCV
MAR
D M D
MGG (READ)
C M D
MGG (WRITE)

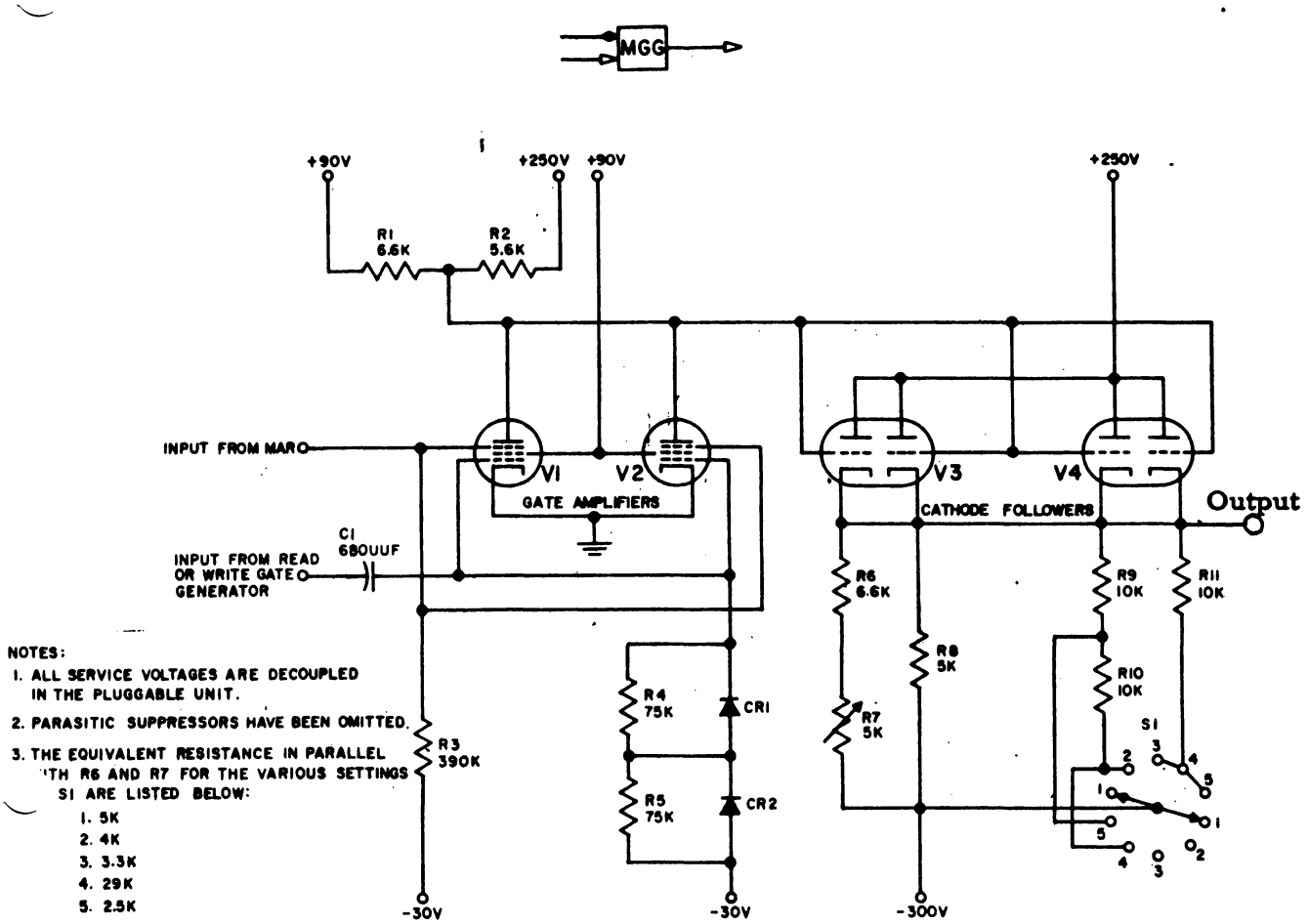
0750

3. Detailed Operation

a. With no inputs to tubes V1 and V2, the voltage at both the suppressor grid and the control grid is -30V, insuring that the tube is below cutoff. When partially selected, the suppressor grid is at the /10V level. The input to the control grid of these tubes is a-c coupled through capacitor C1 and the combination of resistors R4, and crystal diodes CR1 and CR2. This input supplies a positive pulse to the grid when a particular memory gate generator is selected. When the input signal goes positive from the -30V level to the /10V level, the capacitor cannot charge instantaneously and therefore the 40V signal is applied to the control grids of tubes V1 and V2. Because the input signal is positive, crystal diodes CR1 and CR2 do not conduct. Therefore, the effective resistance coupling the input is R4 and R5 in series. Thus for a positive pulse input, the time constant of the coupling network is C1 times R4 plus R5, giving a resultant time constant of approximately 102 usec. Since the normal input pulse length is 2 to 3 usec, the time constant is very much larger than the pulse duration and very little charge is built on C1.

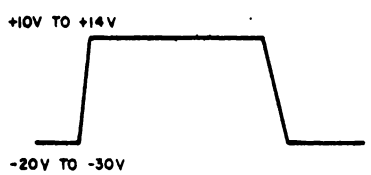
b. When the input signal goes from the /10V level to the -30V level, the signal on the control grids of V1 and V2 falls 40V. However, during the time that the input signal is at /10V, the capacitor picks up some charge, and a small negative overshoot will be obtained as the grid signal falls toward -30V. When this happens, the time constant of the resistor-capacitor coupling will be greatly reduced because the forward resistance of CR1 and CR2 will come into play, since a positive voltage will be applied to the plates of the diodes with respect to the cathodes. The plate voltage of the diodes is stabilized at -30V; however, if some negative overshoot exists, the voltage on the cathodes of the diodes will be in a position to conduct. Resistors R4 and R5, which parallel the diodes, are effectively shorted out, and the resultant time constant is slightly greater than 0.1 usec. The time constant now is a very small percentage of the overall pulse duration and therefore C1 will charge very very rapidly, to stabilize the control grid input signal at -30V.

c. The output voltage of V1 and V2, which is normally at the /180 level, is supplied to the control grids of cathode followers V3 and V4 which are connected in parallel. Under these conditions, the cathode current, flowing through the common cathode resistor in the cathode follower circuit, produces an output of approximately /180V, because, since the tube is at maximum conduction, very little cathode bias builtup is present.



Memory Gate Generator, Schematic Diagram

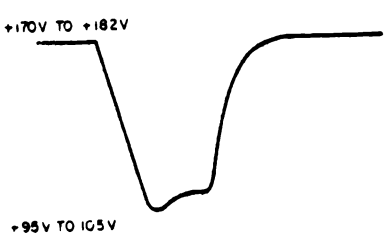
Input



RISE TIME -0.5 USEC MAX.
FALL TIME -0.5 USEC MAX.

X-Y READ AND X-Y WRITE

Output



MEMORY GATE GENERATOR, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Voltage divider
R3	V1 and V2 suppressor grid isolation resistor
R4, R5	Equalizing resistors for CR1 and CR2
R6, R7, R8, R9 R10, R11	Resistor network which determines value of cathode resistance; with R7 as potentiometer which provides for adjustment of cathode resistance to vary current flowing through selected CMD
C1	Input coupling capacitor
CR1, CR2	Input clamping diodes
S1	Selects portions of resistor network for cathode resistance

d. When the input to V3 and V4 falls to the /40V level, the cathodes tend to follow that fall. However, since the memory gate generator is used to supply current to one of 32 core memory drivers and the input to the selected CMD is at approximately a /90V level, the cathode of the MGG is caught at a level in the vicinity of /90V. As the MGG output falls, the core memory driver conducts, a current pulse is generated in the core memory driver, and the cathode follower switches plate control from the plates of tubes V3 and V4 to the to the plate of the core memory driver. Tubes V3 and V4 are cut off, and all current flowing through the cathode resistors of the memory gate generator is under direct control of the selected core memory driver.

Refer to Pg. 077

F. Digit Plane Driver, Model A

1. Function

a. The digit plane driver (DPD) is a logic circuit which functions as a negative current pulse generator. Model A is used in Central Computer memory 2.

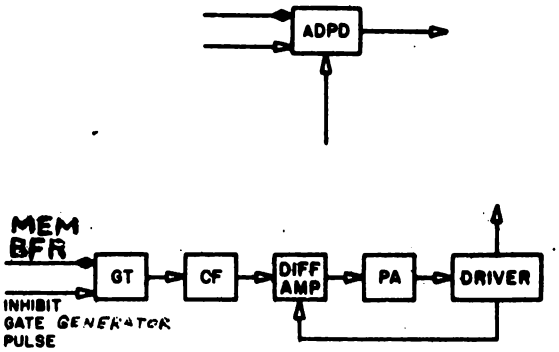
2. Basic Operation

a. A block diagram of the aDPD is shown. The input stage of the DPD consists of a d-c gate tube. The input from the memory buffer has standard levels of -30 and /10V. When the DPD is not to be selected this input is at the -30 level. When the DPD is to generate an inhibit pulse on its associated memory plane, the input is at the /10V. level. The other input to the d-c gate tube also has standard levels of -30 and /10V. When the DPD is used to generate a current pulse, the inhibit pulse is used to control the current pulse width. If the memory buffer FF is set when the inhibit pulse is applied, no output is generated. However, if the memory buffer FF is clear, application of the inhibit pulse to the d-c gate causes a negative pulse to be applied to the cathode follower. The output of the cathode follower is fed into the difference amplifier. Because of the feedback loop from the driver stage of the DPD, the output pulse of the difference amplifier is a negative signal. The negative signal is applied to the pulse amplifier which performs amplification, a shift in level and inversion. The output of the pulse amplifier is applied to the driver stage and conditions it, causing a current pulse to be generated by this stage. The current pulse developed in the inhibit winding is a negative pulse of approx. 410 ma, controlled in duration and of approx. 2.5 usec duration at the 10-percent point.

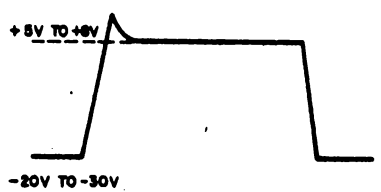
Refer to page 0790 and Logic 0.1.6

DIGIT PLANE DRIVER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Part of divider network between V1 grid and −150V supply (with CR1)
R3	V1 plate load resistor
R4	V2A grid-return resistor
R5	Common cathode resistor for V2A and V2B
R6, R7, R8	Form voltage divider in V2B grid circuit
R9	V3A plate load resistor
R10	V3B grid resistor
R11	V3B plate load resistor
R12	V4 plate load resistor
R13	Equalizing resistor
R14, R15	Voltage divider connected between −300 and −150V supplies
R16	Damping resistor
CR1	Part of divider network in V1 grid circuit (with R1 and R2)
CR2, CR3	Clamp V2A grid at +10V in quiescent state
CR4	Grid-clamping diode for V4A and V4B
C1	Coupling capacitor
C2	Shunting capacitor
C3	Shunting capacitor
C4	Coupling capacitor
C5	Coupling capacitor
C6	Bypass capacitor



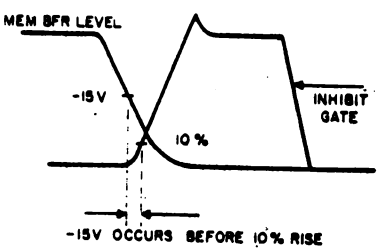
Digit Plane Driver, Model A, Block Diagram



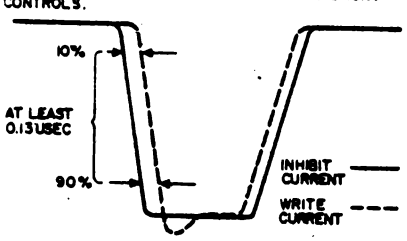
RISE TIME - 0.3 USEC MAX.
FALL TIME - 0.3 USEC MAX.

INHIBIT LHW - RHW ONLY

WHEN MEASURING AT THE INPUT TO THE DPD, THE MEMORY BUFFER LEVEL SHALL BE DOWN TO -15V BEFORE THE 10% RISE OF THE INHIBIT GATE GENERATOR



THE INHIBIT CURRENT SHALL START AT LEAST 0.13 USEC BEFORE WRITE CURRENT AT ALL CORRESPONDING POINTS OF THE PULSE BETWEEN THE 10% AND 90% POINTS. THE END OF INHIBIT MUST OCCUR AT THE SAME TIME OR LATER THAN THE END OF WRITE, BUT NO LATER THAN 6.6 USEC FROM CLEAR-MEMORY-CONTROLS.



Core Storage Element

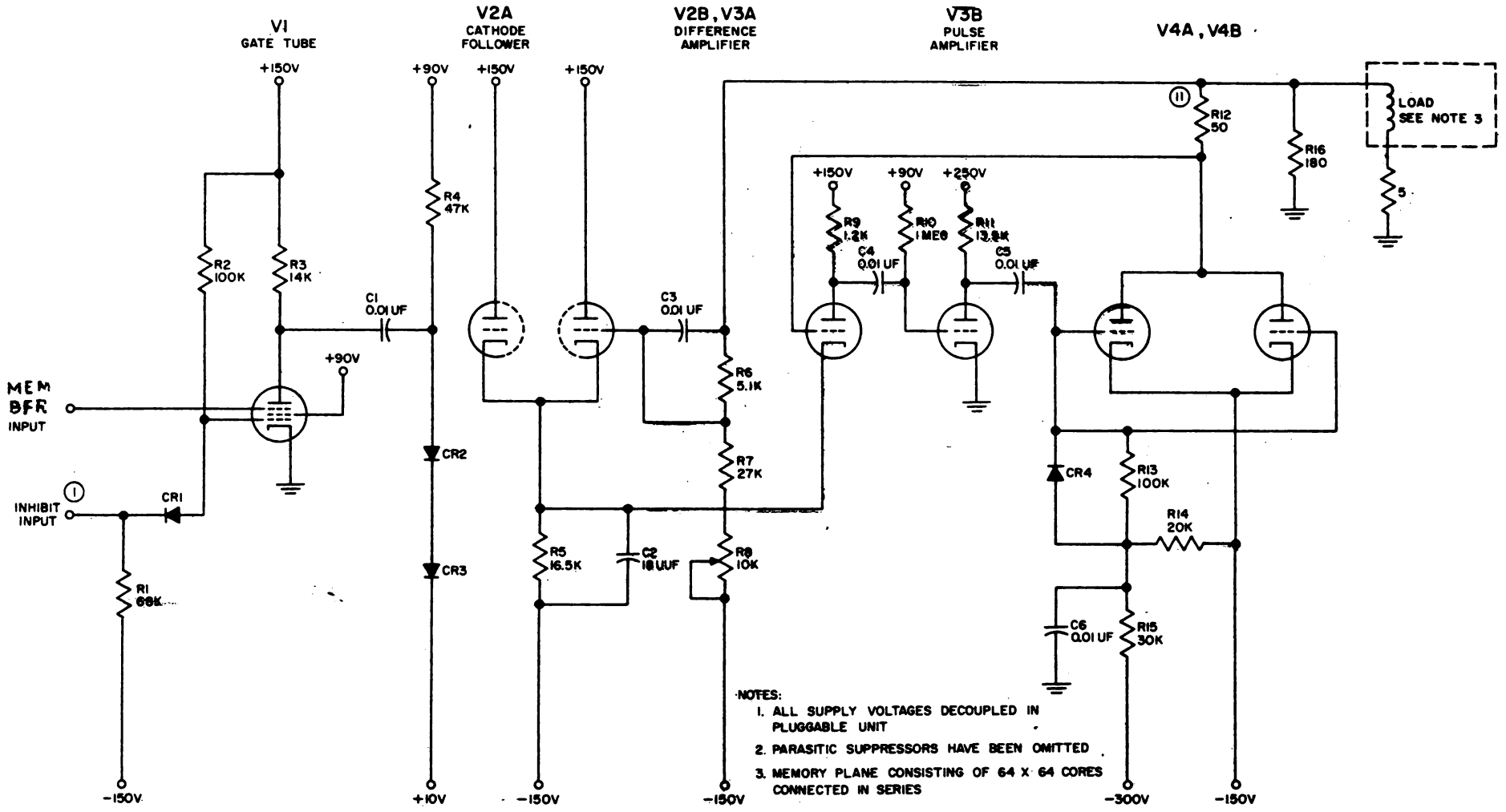
3. Detailed Operation

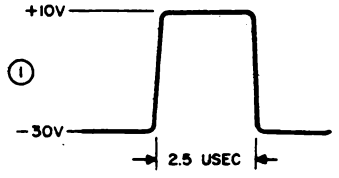
a. The circuit consists of a d-c gate tube (V1), a cathode follower (V2A), a difference amplifier (V2B and V3A), a pulse amplifier (V3B), and a driver tube (V4A and V4B connected in parallel). Refer to page 0810

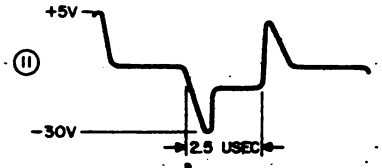
b. The memory buffer input line to V1 is normally at the -30 V level. If the level on this line is at +10V when the inhibit pulse is applied to the input grid of V1, the tube conducts, thereby lowering its plate voltage from the normal +15V supply to a +60V level. The output of V1, which is coupled to the grid of cathode follower V2A, is a negative pulse of approximately 90V in amplitude, and, since the inhibit pulse is approximately 2.5 usec in duration, the output of V1 is also of that duration.

c. In the quiescent state, the grid of V2A is held at approximately the +10V level by the action of resistor R4 and crystal diodes CR2 and CR3. When the output of V1 is coupled to the control grid of V2A, it causes this tube to be cut off, and the voltage on the cathode starts to fall from +10V to -80V. It does not reach -80V, however, but is caught by the cathode of V2B. The cathodes of V2B and V3A are connected to the V2A cathode and under steady-state conditions, all three cathodes are at the +10V level. When V2A conducts, the cathodes of V2B and V3A maintain these tubes at cutoff. When V2A is cut off, the current through the common cathode resistor utilized by these three tubes drops and the cathode of V3B becomes more negative. This causes V3B to conduct, lower its plate voltage and the negative signal thus generated is applied to the grid of V3B through a coupling capacitor.

d. Under steady-state conditions, V3B is conducting heavily, with the result that the plate is at a low level. Therefore, when the negative signal is transmitted from V3A to the grid of V3B, this tube is driven toward cutoff and the output pulse from its plate is coupled to the grids of V4A and V4B. These tubes are normally at cutoff with the cathode voltage being supplied by the -150 supply and the grids obtaining their voltage from the top point of a voltage divider connected between -150V and -300V. When the positive signal is transferred from the plate of V3B to the control grids of V4A and V4B, crystal diode CR4 is cut off, representing a very high resistance path. As a result, the driving path of coupling capacitor C5 is through grid resistor R13. Because of the values of these two components, the







Digit Plane Driver, Model A, Schematic Diagram

0180

time constant is very long compared to the pulse duration of the signal supplied by V3B. This signal causes the bias on the grids of V4A and V4B to decrease, resulting in a heavy conduction through the tubes, causing a nominal current pulse of approximately 410ma to flow through a dropping resistor in the plate circuit, resulting in a 20V drop. This 20V drop represents itself as a negative signal to the grid of V3A. Thus, the earlier negative signal generated by the plate of V3A which is transferred to the grid of V3B is reduced in magnitude with the result that V3B will not cut off. Instead, a negative bias is applied to it and the positive signal transferred to the grids of V4A and V4B, is not quite so positive. The amount of current flowing through the inhibit winding is a direct result of the voltage supplied to the grid of V3B. As this voltage is made more negative, a higher value of current flows through the inhibit winding; conversely, as this voltage is made more positive, the inhibit winding current is decreased. The initial current pulse magnitude sent to the inhibit winding is larger so as to overcome the reactance of the highly inductive inhibit winding. The negative feedback restores the current pulse magnitude to a nomina value once the reactance has been overcome.

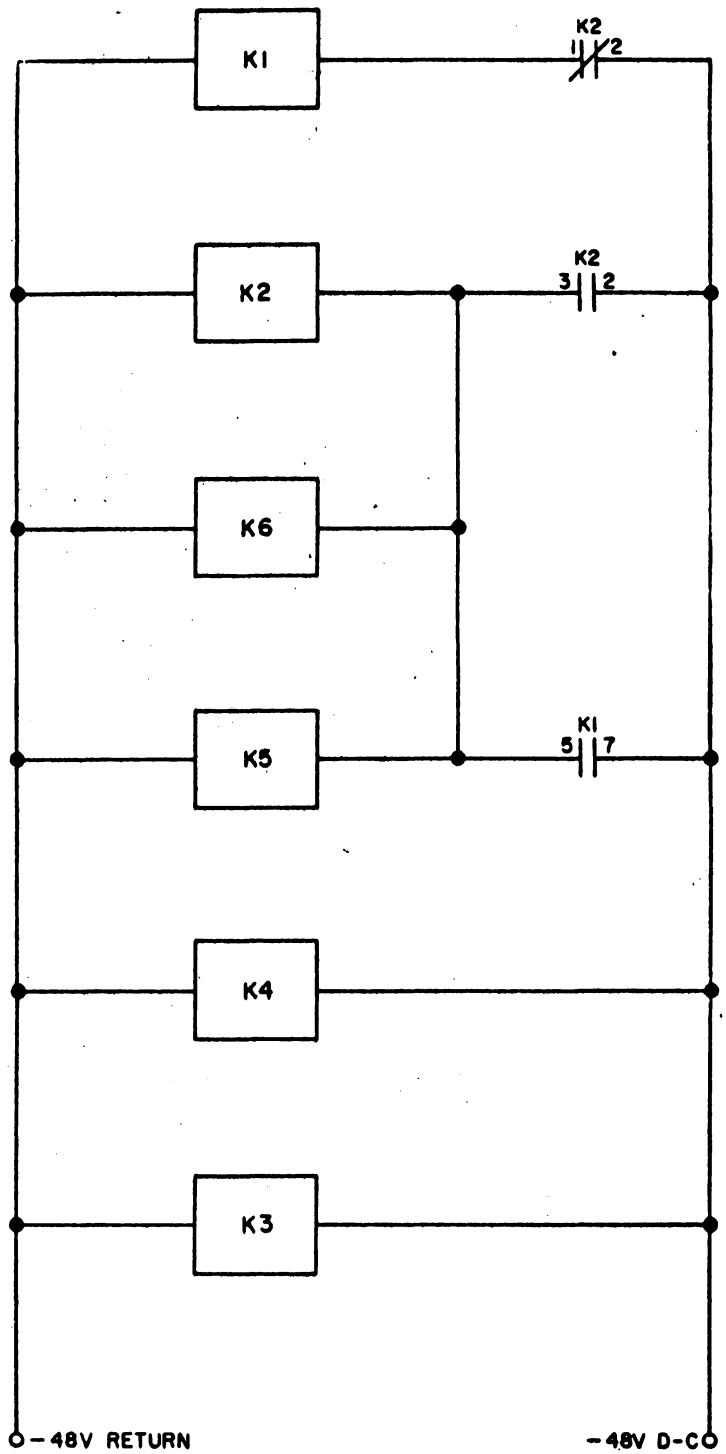
G. DPD Decoupling

1. A problem which has the effect of producing spurious oscillations (noise) on the -150V or +150V lines is invariable due to a defect in the DPD decoupling circuitry located in the Z module. The specific indications of faulty DPD decoupling are:
   a. Memory operates erratically.
   b. The +150 DPD DECOUPLER and -150 DPD DECOUPLER lights on the Z module are not lit, although the bulbs are good.

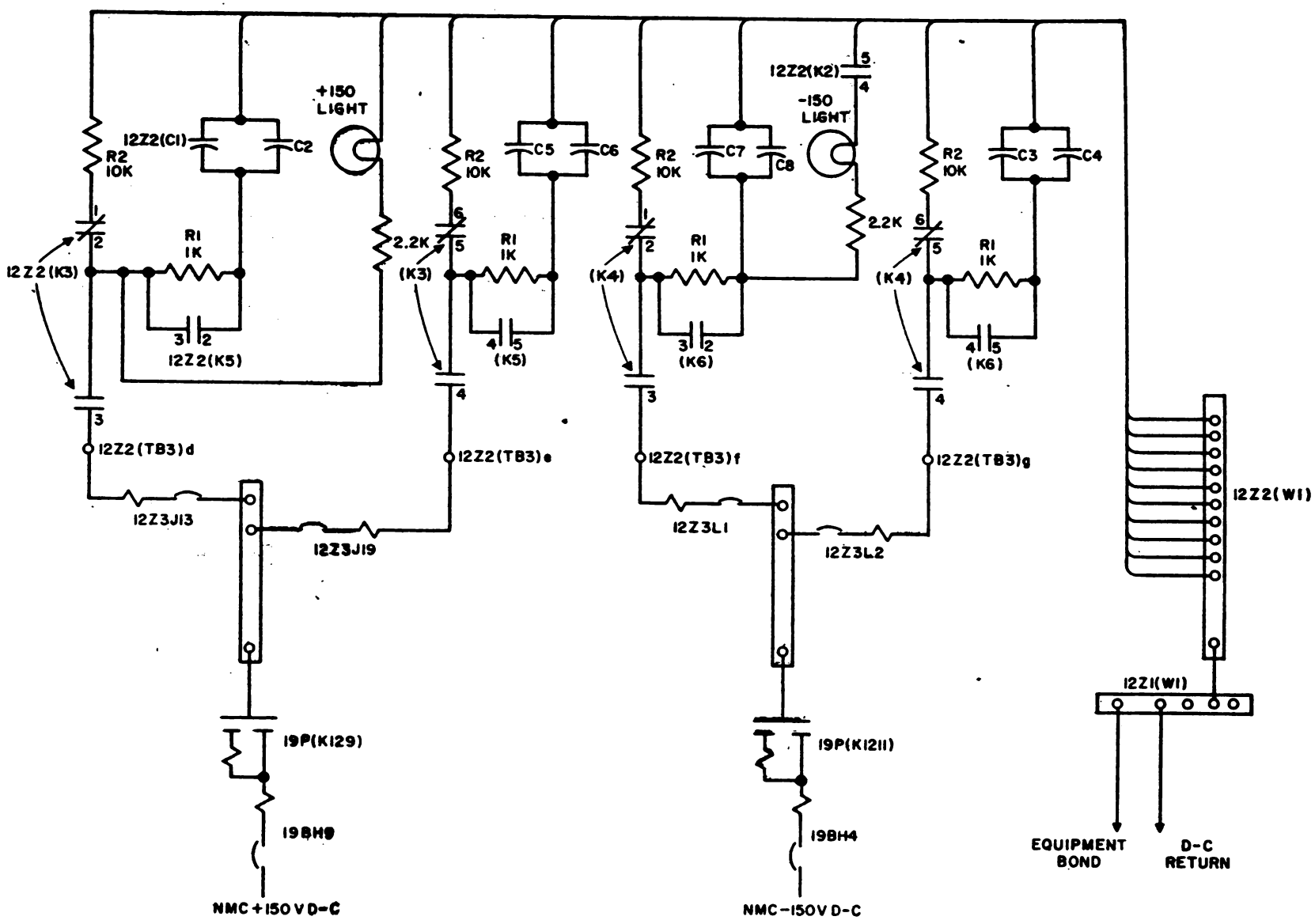
2. Circuit Description

   a. The decoupling circuitry utilizes six relays which are connected to the -48V d-c source. These relays are of the instantaneous type except for K1 which is a 10-second thermal delay relay. Refer to page 0830 & page 0840

   b. When d-c voltage is applied, -48V dc picks K3 and K4. This permits +150V to charge the decoupling capacitors C1, C2, C5 and C6, and -150V to charge the decoupling capacitors C3, C4, C7 and C8. The charging path is through the respective current-limiting resistors designated R1. These resistors prevent the charging current from exceeding the ratings of the circuit breakers 12Z3 -J13, -J19, +L1, and -L2. After 10 seconds, relay K1 is energized and picks K2, K5 and K6. Relay K2 holds K5, K6 and K2, and drops K1. Relay K2 also completes the -150V lamp circuit. Relays K5 and K6 short out their respective current-limiting resistors (R1) thus permitting the capacitors C1 through C8 to decouple any spurious information present on the -150V and +150V lines.



RELAY CONNECTIONS, DPD
DECOUPLING



DPD DECOUPLING CIRCUITRY, SIMPLIFIED DIAGRAM

c. When the -48V is removed, the decoupling capacitors are discharged respectively through a path consisting of: the current-limiting resistors designated R2, the K3 and K4 relay points shown, and the current - limiting resistors designated R1.

H. Sense Amplifier, Model B

1. Function

a. The model B sense amplifier (bSA) is a logic circuit which develops a positive output signal regardless of the polarity of the input signal.

2. Principles of Operation, Basic

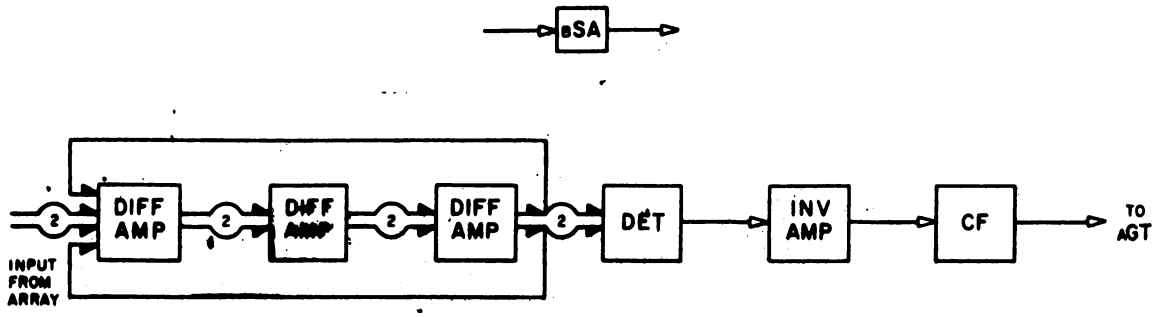
a. Two inputs are supplied to the first stage of the amplifier from a sense winding in the array. The difference stages of the amplifier have balanced inputs, and half of the signal induced in the sense winding is applied to each input of the first stage; these input signals are 180 degrees out of phase with each other. The first three stages amplify the difference signal existing between these two inputs and generate difference signals on two output lines. The difference signal on the output lines from the third stage is applied to a detector and is also returned to the first stage to provide negative feedback. Although the two input signals to the detector are of equal amplitude but 180 degrees out of phase, the detector is actuated by the positive input only, producing a single line output pulse of negative polarity. The negative signal is amplified and inverted by the inverter-amplifier stage to produce a positive pulse output which is fed to a cathode follower. The positive output pulse from the cathode follower is applied to the suppressor grid of a model A gate tube, thereby conditioning the gate tube.

Refer to Page 0860

3. Principles of Operation, Detailed

a. The first three stages, V1, V2 and V3, form a conventional class A difference amplifier, with negative feedback from the third difference-amplifier plates applied to the grids of the input stage. Tube V1 is a low-noise tube which is used to decrease microphonic noise. With no signal applied to the inputs, the level of both grids is at approximately +1V, with the result that the common cathodes are at approximately +4V. The plates of V1A and V1B are both at approximately +100V. Since both sides of the tube are identical, the plate voltages are equal. If a 100-mv signal is induced in the sense winding, a 50-mv signal to ground is applied to each input. However, the signal on one grid is 180 degrees

Refer to Page 0880 and Logic 0.1.6



Sense Amplifier, Model B, Block Diagram

SENSE AMPLIFIER, MODEL B, FUNCTION OF DETAIL PARTS

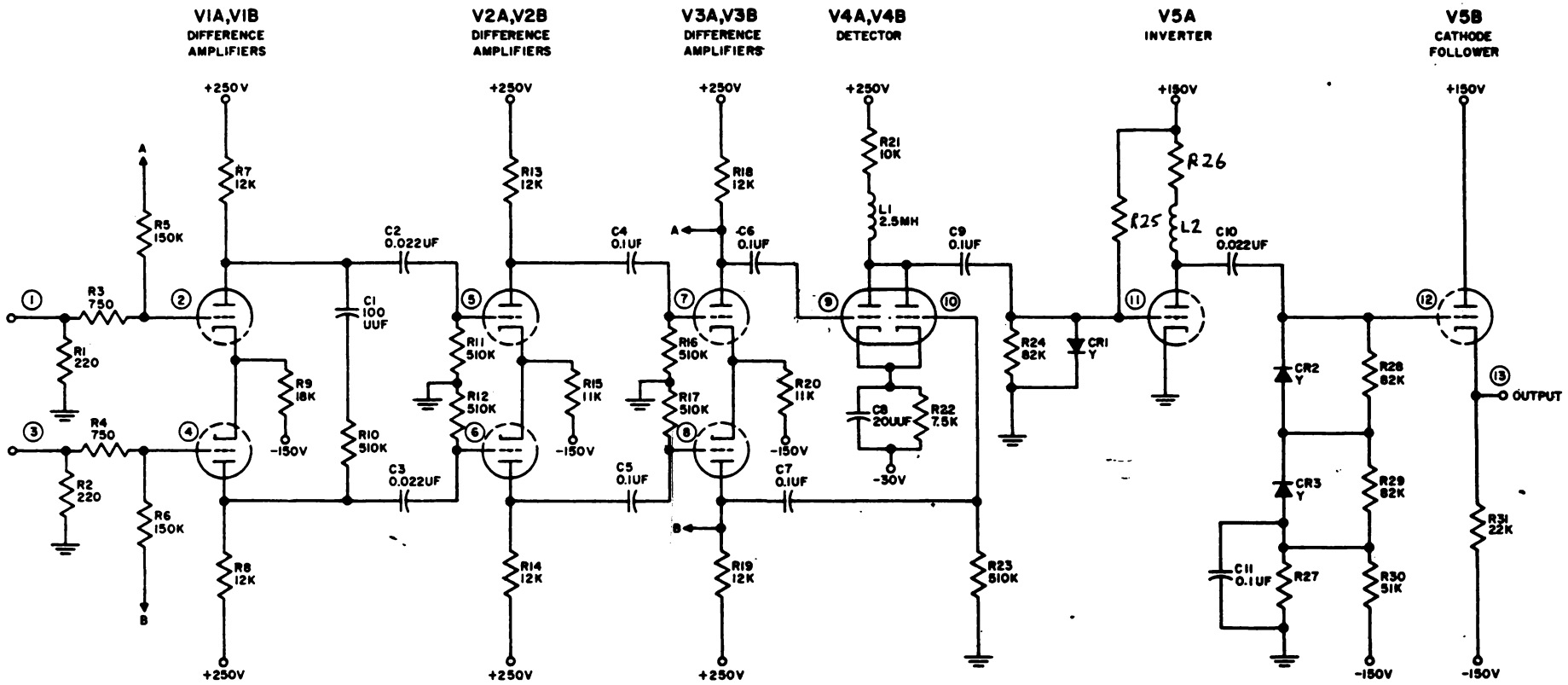
REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1, R2	Input load resistors for V1	R27	Part of voltage divider between −150V and ground (with R30)
R3, R4	Current-limiting resistors	R28, R29	Equalizing resistors for CR2 and CR3
R5, R6	Feedback resistors	R30	Part of voltage divider between −150V and ground (with R27)
R7, R8	Plate load resistors for V1	R31	Cathode resistor for V5B
R9	Cathode resistor for V1	CR1	Part of V5A grid clamping (with R24 and R25)
R10	Part of stabilization network (with C1)	CR2, CR3	V5B grid-clamping diodes
R11, R12	Form part of RC coupling networks between V1 and V2 (with C2 and C3)	C1	Part of stabilization network with (R10)
R13, R14	Plate load resistors for V2	C2, C3	Part of RC coupling network between V1 and V2 (with R11 and R12)
R15	Cathode resistor for V2	C4, C5	Part of RC coupling network between V2 and V3 (with R16 and R17)
R16, R17	Form part of RC coupling network between V2 and V3 (with C4 and C5)	C6, C7	Coupling capacitors between V3 and V4
R18, R19	Plate load resistors for V3	C8	Bypass capacitor in V4 cathode circuit
R20	Cathode resistor for V3	C9	Coupling capacitor between V4 and V5A
R21	Plate load for V4 (with L1)	C10	Coupling capacitor between V5A and V5B
R22	Part of cathode bias network for V4 (with C8)	C11	Bypass capacitor
R23	Grid return for V4B		
R24, R25	Part of grid-clamping circuit for V5A (with CR1)		
R26	Plate load for V5A (with L2)		

out of phase with that on the other grid; therefore, one grid rises by 50 mv whereas the other falls by 50 mv. The grid signal causes one plate to fall while the other rises. Since operation is based on the linear portion of the tube characteristics, the changes in plate current are equal but 180 degrees out of phase and the total cathode current will remain the same. The signals from the two plates are resistance-capacitance coupled to the second stage.

b. The second and third stages further amplify the signal anf furnish two equal and opposite output signals to the detector stage. Regardless of the polarity of the input pulse, a positive pulse is generated at one of the two outputs of the third stage. Detector stage V4 is a mixer circuit biased at about 4V, or near cutoff. Both halves of the twin triode which is used as a detector share a common plate load and a common cathode load. Two inputs are supplied by the two outputs of the third difference amplifier, V3, but, since the detector is sensitive to positive signals only, it makes use of only one. A positive signal on either grid produces a negative signal at the plate of V4. This negative signal is coupled to the grid of inverter-amplifier stage V5A. With a 100-mv input to the difference amplifier, the input to the detector is approximately 9V and the resultant output only 6V. The gain of the detector stage is less than unity because of the large cathode resistor employed, and because, owing to the imperfect cutoff of the tube, the negative signal on the second grid has some effect.

c. Inverter-amplifier stage V5A is a triode amplifier with a gain of approximately 10. The stage is operated at zero bias in order to allow a larger negative input signal to be attained before cutoff. Diode clamp CR1 is used across the grid resistor to prevent base-line shift. Shunt-peaking is used in the plate circuit to decrease the rise and fall time of the signal. Since the amplifier drives a cathode follower (V5B) that has a low input capacity, a relatively small inductance is used. For a 100-mv input to the difference amplifier, the output of the inverter-amplifier is about 52V.

d. Cathode follower V5B receives a positive pulse from inverter-amplifier V5A, and provides a low impedance source for conditioning the gate tube. The input to the cathode follower is clamped to prevent base-line shift. Two diodes, CR2 and CR3, are used in series because of the high back voltage developed. The grid is biased by means of a voltage divider network connected to a -150V marginal checking line. The grid, and therefore the cathode, is normally at -26V. The gate tube suppressor



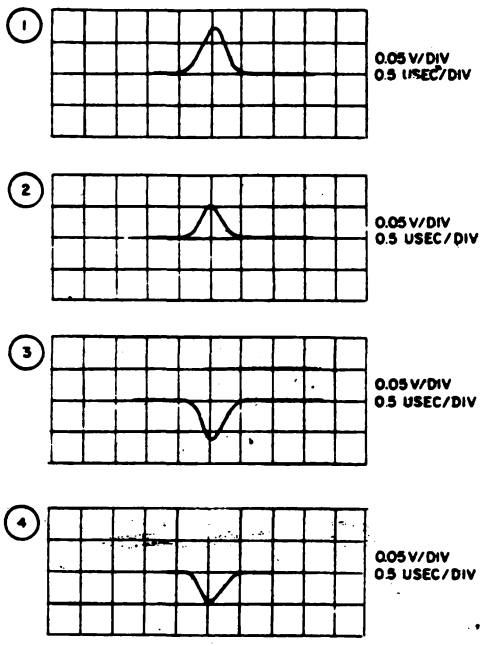
NOTES:

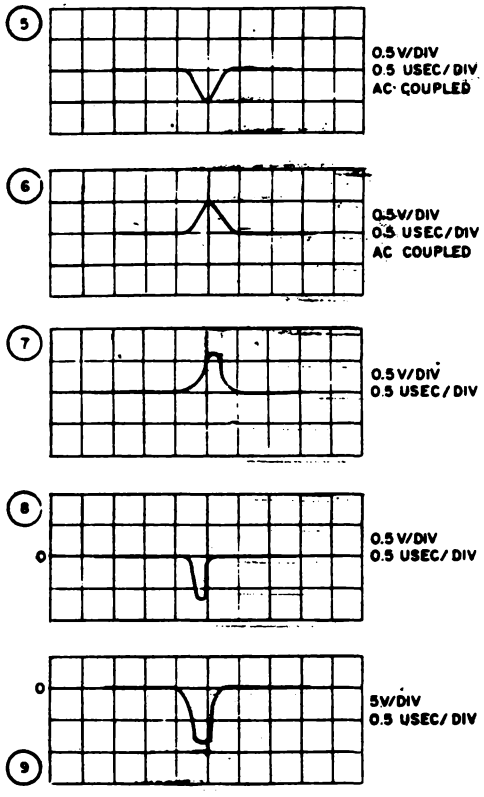
1. ALL SUPPLY VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT
2. PARASITIC SUPPRESSORS HAVE BEEN OMITTED

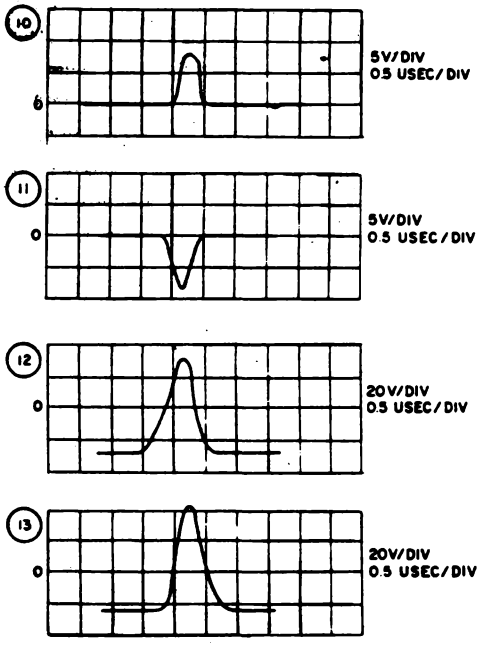
Sense Amplifier, Model B, Schematic Diagram

0880

0680


1
0.05 V/DIV
0.5 USEC/DIV
2
0.05 V/DIV
0.5 USEC/DIV
3
0.05 V/DIV
0.5 USEC/DIV
4
0.05 V/DIV
0.5 USEC/DIV


5
0.5 V/DIV
0.5 USEC/DIV
AC COUPLED
6
0.5 V/DIV
0.5 USEC/DIV
AC COUPLED
7
0.5 V/DIV
0.5 USEC/DIV
8
0
0.5 V/DIV
0.5 USEC/DIV
0
9
5V/DIV
0.5 USEC/DIV


10
6
5V/DIV
0.5 USEC/DIV
11
0
5V/DIV
0.5 USEC/DIV
12
0
20V/DIV
0.5 USEC/DIV
13
0
20V/DIV
0.5 USEC/DIV

grid, since it is directly coupled to the output of the cathode follower, is also at -26V in the absence of a signal. If a sufficient signal is supplied to the suppressor grid when the gate tube is sampled, the gate tube conducts and produces a pulse. Conduction of the suppressor grid at this time loads the cathode follower. The loading effect is represented in the form of a notch in the pulse waveform taken at the suppressor grid of the gate tube.

I. Summary Questions

1. Power Cathode Follower

True or false-

a. This is a power amplifier. _____

b. Degenerative feedback is used to stabilize the output voltage. _____

c. A smaller cathode resistor is used for capacitive loads. _____

d. Capacitor C2 reduces overshoot in the circuit. _____

e. CR1, CR2 and CR3 clamps the lower output to 28 volts. _____

2. Matrix Output Amplifier

a. The MOA inverts and amplifies the output of the DMD. _____

b. There are 128 MOA's in memory #2. _____

c. The output of a selected MOA is #102. _____

d. The output of an MOA supplies the necessary conditioning voltage to cause an MXG to conduct _____

3. Core Memory Driver

a. One CMD supplies both read and write currents to a drive line thru the array. _____

b. The direction of current thru a drive line is determined by an MOA output. _____

c. Only one CMD will be conditioned at any one time. _____

d. The CMD controls the amount of drive current to the array. _____

e. 400 ma of current flows thru the CMD when it is conducting. _____

4. Memory Array Floating Ground

a. Drive current from one CMD will flow thru all 64 drive lines. _____

b. 400 ma of current will flow thru the circuit breaker each time a drive line is selected. _____

c. The circuit breaker protects against a short between the primary and secondary of the CMD transformer. _____

d. The floating ground isolates noise on the ground bus from the drive lines. _____

5. Memory Gate Generator

a. One MGG supplies current to 32 drive lines in the array. _____

b. The length of time that the odd-even FF (R9 or R15) is set will determine the time that current is flowing in a drive line. _____

c. The maximum voltage swing out of an MGG is 90V. _____

d. The MGG adjustments control the amplitude of drive current thru the array. _____

e. Two CMD's and two MGG's will be conditioned during each memory cycle. _____

6. Digit Plane Driver

a. One DPD supplies current to 4096 cores. _____

b. A DPD is conditioned by two ±10V levels. _____

c. The DPD supplies 410 ma of current in the read direction during write time. _____

d. Two inhibit FFs are necessary because the left and right half words are inhibited at different times. _____

e. All DPD's will be cut off when writing positive zeros in both half words. _____

Core Storage Element

7. Sense Amplifier

   a. Either a negative or positive core will cause a positive output from the sense amplifier. _____

   b. The first three difference amplifiers operate at cutoff. _____

   c. Detector stage V 4 will be controlled by a negative level. _____

   d. V 5A is an inverter amplifier. _____

   e. The detector stage V4 also an amplifier. _____

X. 64^2 Memory Unit Physical Characteristics

A. Drive Line Connections

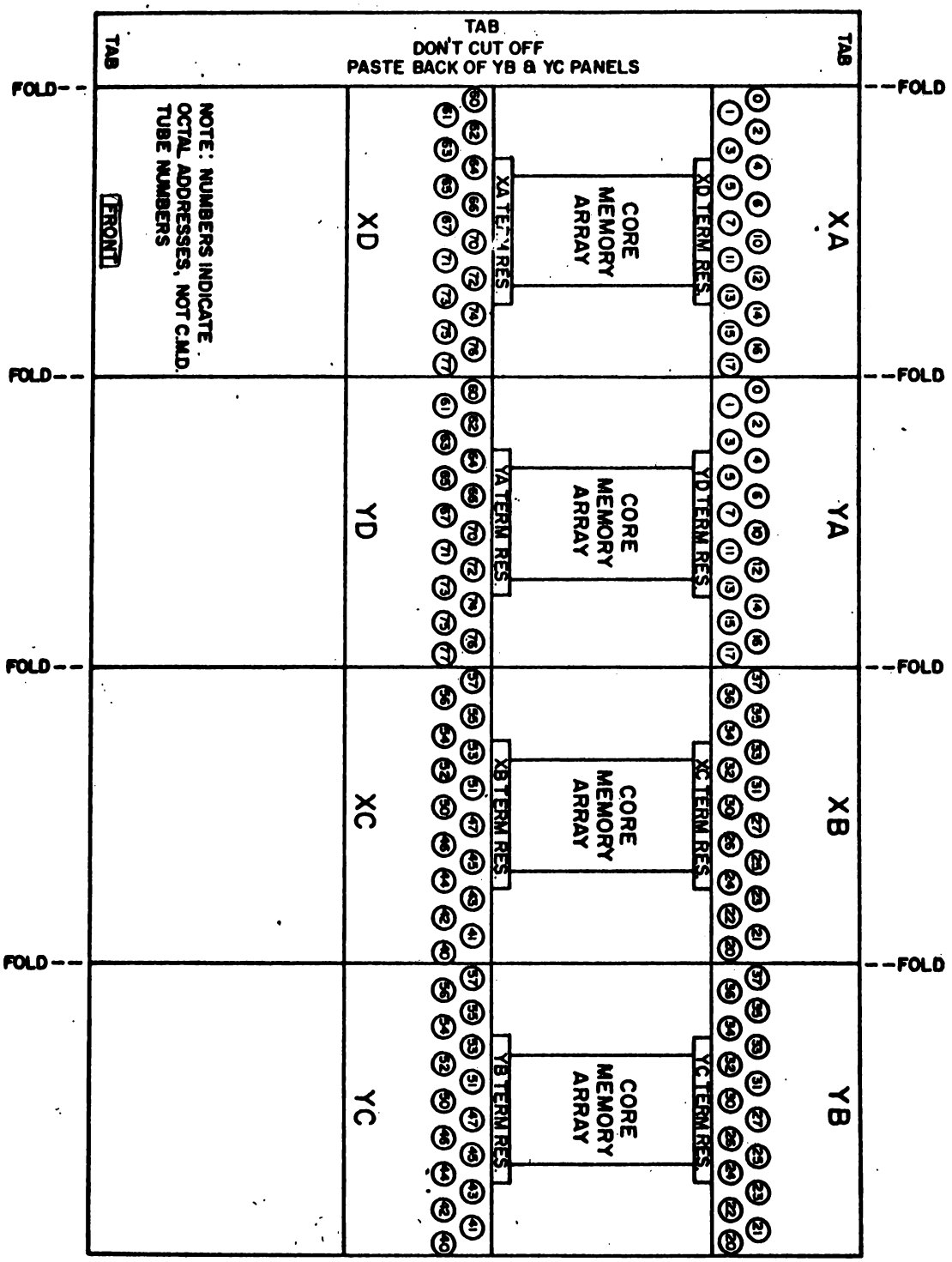
1. Selection of a memory word involves the simultaneous application of read-write current pulses to similarly addressed cores in each plane. The corresponding X and Y drive lines in each of the 34 planes of the array will be involved in the operation. To provide a control so that one current driver can supply read-write current pulses to the corresponding X or Y drive line of each plane, the similarly numbered X and Y drive lines of all the planes are connected in series (by means of jumpers) so that common selection windings will be formed. One end of each of the 64 X and 64 Y selection windings is connected to a read-write current driver; the other end of each winding is connected to a terminating resistor. In the ferrite core array, all the X selection line drivers (64) are connected to the front and back sides of the array and all the Y selection line drivers (64) are connected to the left and right sides of the array. Since the input and output connections of the X and Y selecting windings are exactly the same, the following discussion will deal with Y selection windings only.

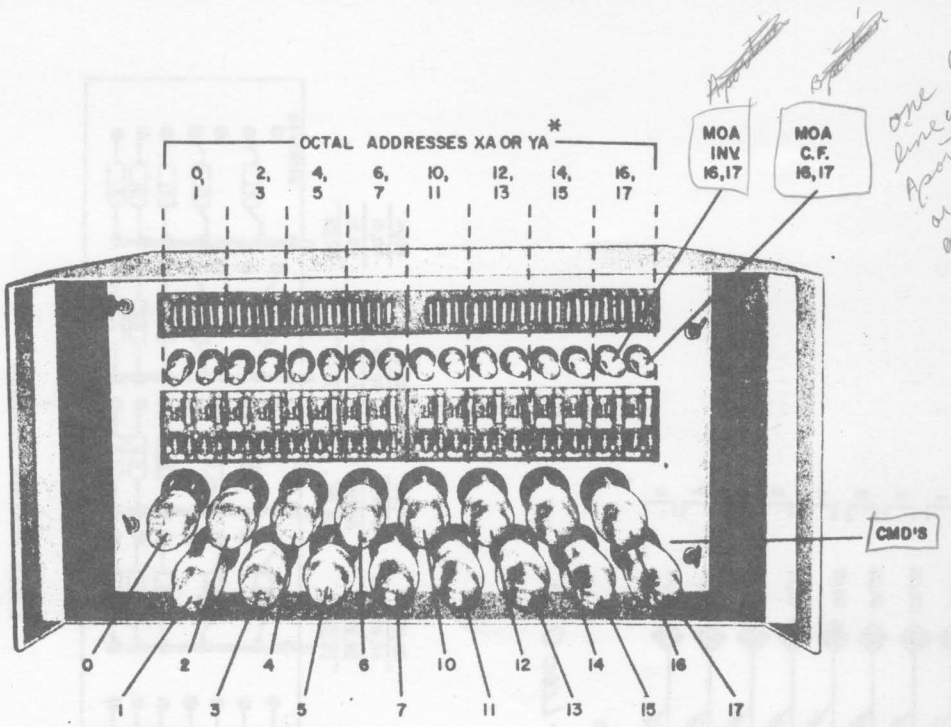
2. The 64 Y line current drivers are divided into four equal groups. Each group of 16 drivers is contained in a pluggable driver panel which is connected to the array in a specific manner. The 16 Y line drivers of driver panel YA are connected (on the right side of the array) to every fourth Y selection line of plane 3, starting with line Y-0. Since the similarly numbered Y lines of each of the 34 digit planes are connected in series (by connecting the similarly numbered terminals of adjacent planes on alternate sides of the array), each of these Y lines will terminate on the right side of plane 36. To complete the circuit of each of these windings, the associated terminals of this plane are connected to individual terminating resistors and a common 240-ohm resistor and a circuit breaker arrangement.

Refer to page 0400

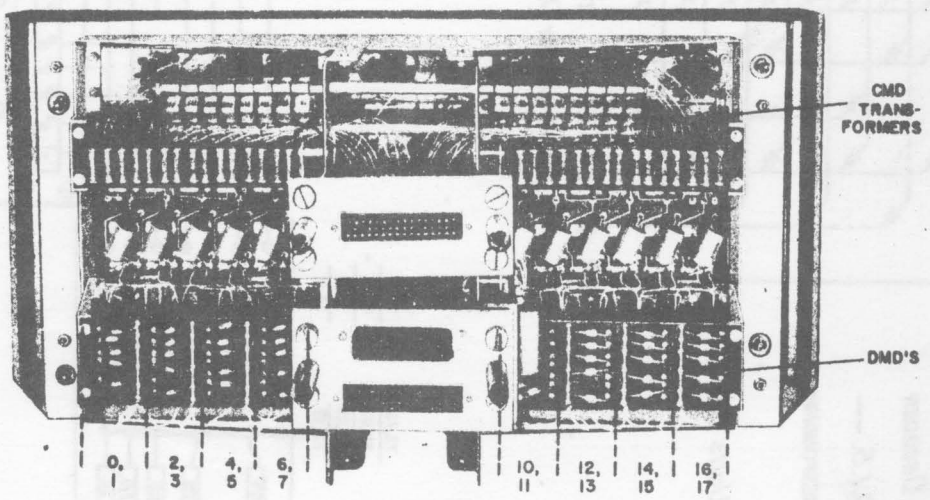
3. The 16 current drivers of each of the other Y driver panels are connected to the array in a similar manner; that is, the current drivers are connected to one end of the array and the associated terminating resistors are connected to the other end. Because the Y line current drivers are connected to the array in the sequence noted, the direction of read-write current flow in the adjacent Y lines of each plane will be in mutually opposing directions.

0940


TAB
DON'T CUT OFF
PASTE BACK OF YB & YC PANELS
TAB
TAB
FOLD
FOLD
FOLD
FOLD
FOLD
FOLD
FOLD
FOLD
XA
XB
XC
XD
YA
YB
YC
YD
CORE MEMORY ARRAY
XA TERM RES.
XB TERM RES.
XC TERM RES.
XD TERM RES.
YA TERM RES.
YB TERM RES.
YC TERM RES.
YD TERM RES.
NOTE: NUMBERS INDICATE OCTAL ADDRESSES, NOT C.M.D. TUBE NUMBERS
FRONT



FRONT VIEW



REAR VIEW

MEMORY DRIVER PANEL, ADDRESS LOCATIONS

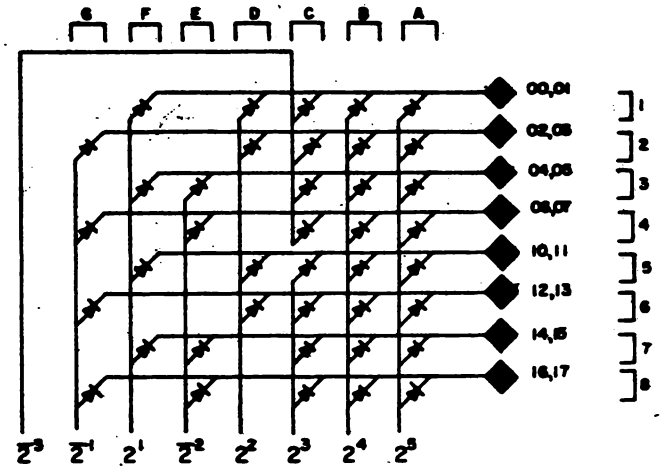
Note: * The memory driver panel circuitry demonstrated is similar for

XB or YB (octal addresses 37-20)

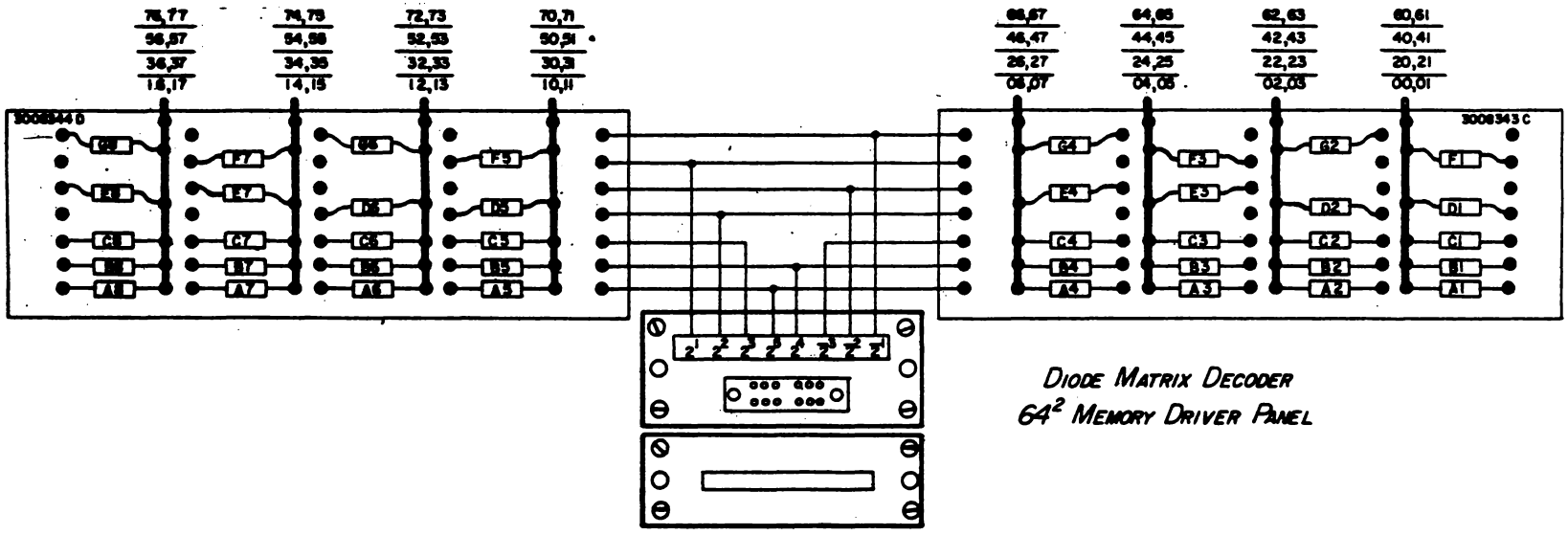
XC or YC (octal addresses 57-40)

XD or YD (octal addresses 60-77)

This Chart Illustrates The Correlation Between The Diode Matrix Decoder As It Is Shown On Logic 0.1.5. — And As It Exists On A Corresponding Driver Panel.
($X_A, X_B, X_C, X_D, Y_A, Y_B, Y_C, Y_D$) On Units 8 or 11



Diode Matrix Decoder — Logic 0.1.5

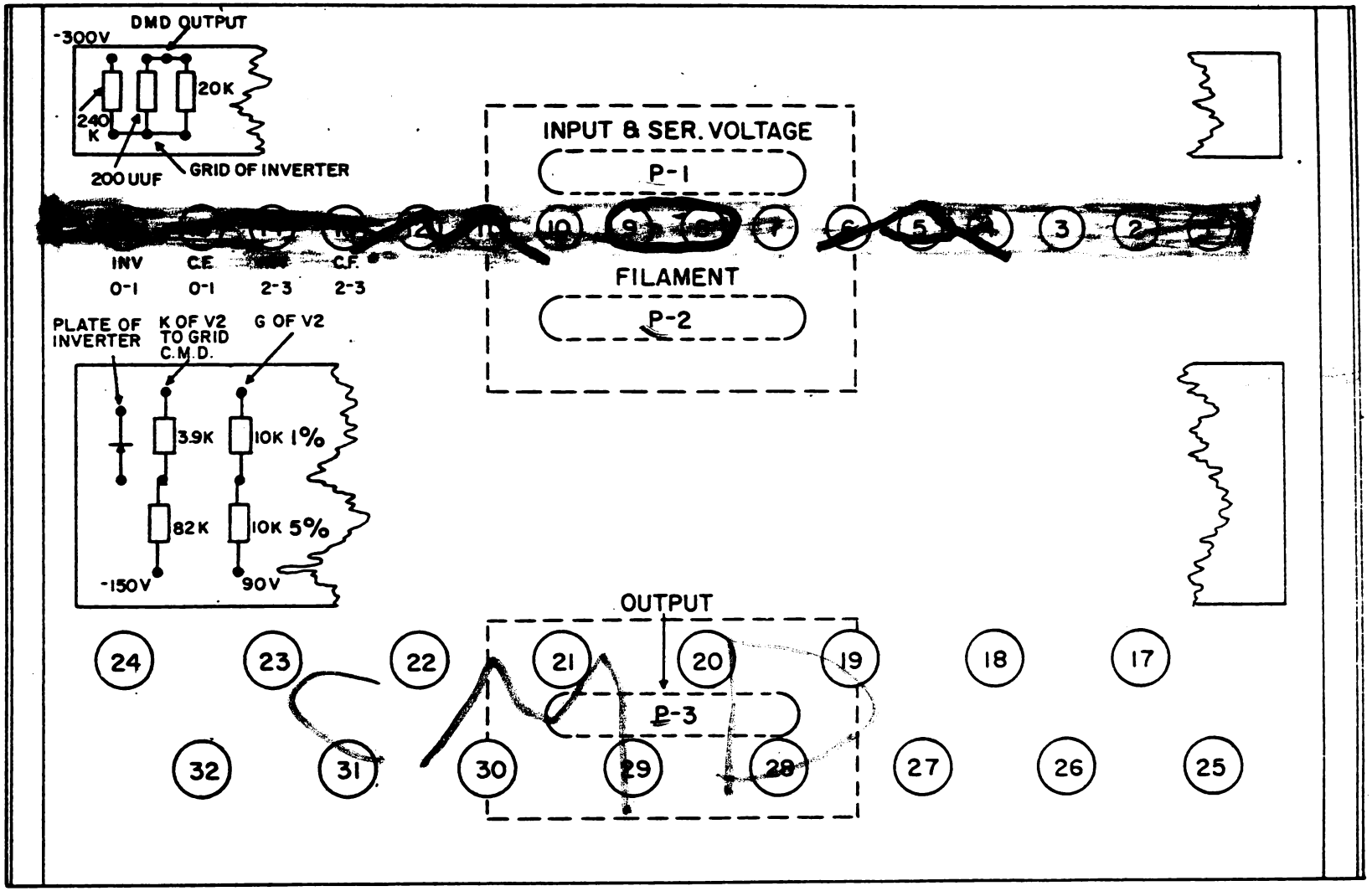


Diode Matrix Decoder
64^2 Memory Driver Panel

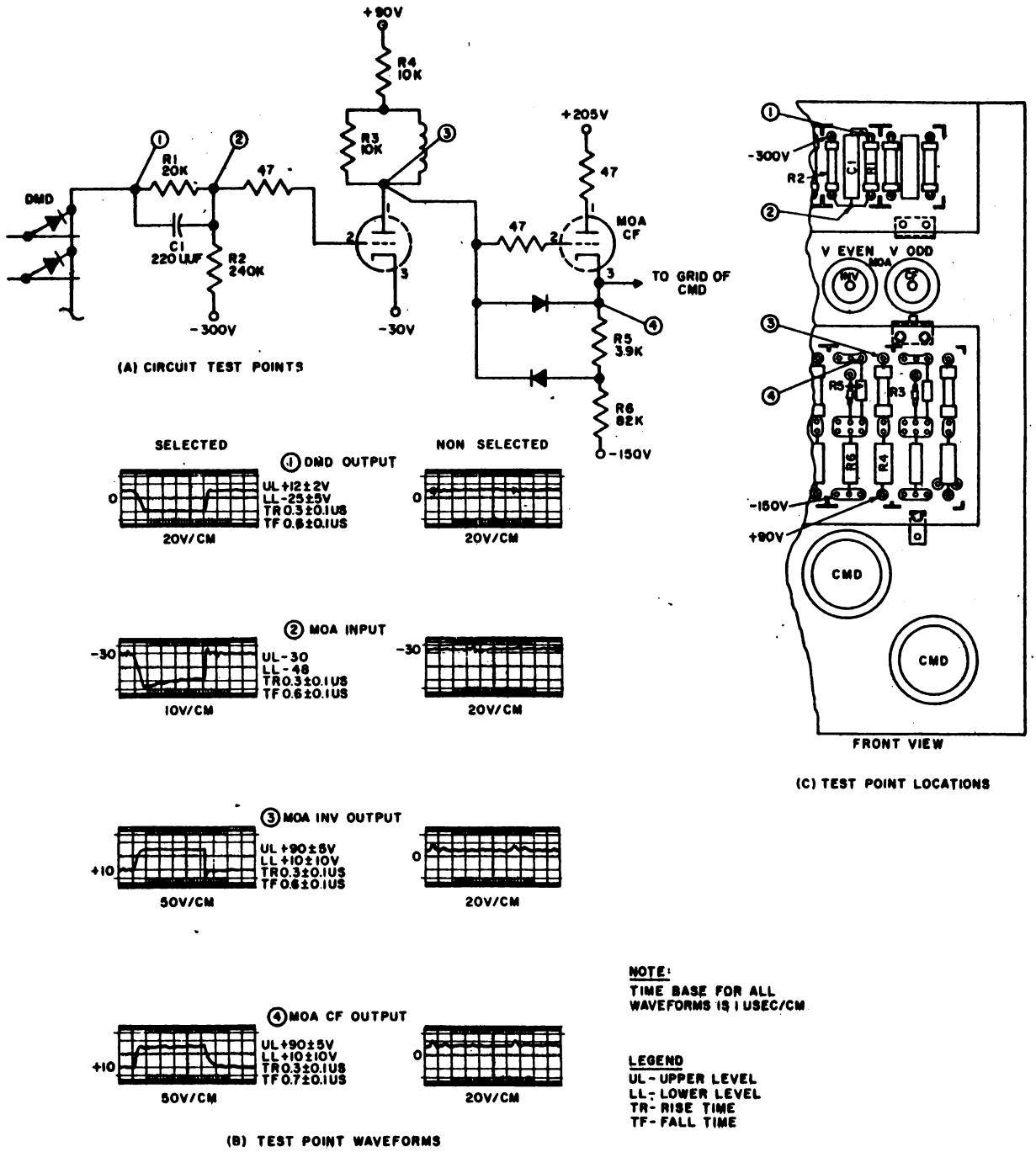
0960

	Address	Address	cmd socket no.	moa socket nos.
PANEL A	0	40	24	16a 15a
	1	41	32	16b 15b
	2	42	23	14a 13a
	3	43	31	14b 13b
	4	44	22	12a 11a
	5	45	30	12b 11b
	6	46	21	10a 9a
	7	47	29	10b 9b
PANEL C	10	50	20	8a 7a
	11	51	28	8b 7b
	12	52	19	6a 5a
	13	53	27	6b 5b
	14	54	18	4a 3a
	15	55	26	4b 3b
	16	56	17	2a 1a
	17	57	25	2b 1b
PANEL B	20	60	25	2b 1b
	21	61	17	2a 1a
	22	62	26	4b 3b
	23	63	18	4a 3a
	24	64	27	6b 5b
	25	65	19	6a 5a
	26	66	28	8b 7b
	27	67	20	8a 7a
PANEL D	30	70	29	10b 9b
	31	71	21	10a 9a
	32	72	30	12b 11b
	33	73	22	12a 11a
	34	74	31	14b 13b
	35	75	23	14a 13a
	36	76	32	16b 15b
	37	77	24	16a 15a

CORE MEMORY DRIVER PANEL ADDRESS
TO TUBE CONVERSATION CHART



MEMORY DRIVER PANEL



MEMORY DRIVER PANEL, WAVEFORM ANALYSIS

4. The 64 X selection winding current drivers and terminating resistors are connected to the front and back sides of the array in exactly the same manner as described above. The current drivers contained in driver panels XA and XD are connected to the front side of the array, and the current drivers contained in driver panels XB and XC are connected to the rear side of the array. Refer to page 0940

B. Core Memory Driver Panels

1. Eight Driver Panels

   a. XA thru XD Refer to page 0950
   b. YA thru YD & Logic 0.1.5
   c. X on front and rear
   d. Y on left and right sides of array
   e. 16 CMD's per Driver Panel
   f. 16 MOA's per Driver Panel
   g. 1/4 of a DMD per Panel Refer to page 0960
   h. Each panel has 16 X or Y drive lines coming from it. (Logic 0.1.5 to 0.1.7)
   i. Each panel drives every fourth line in array Refer to page 0400
   j. Terminating Resistor and Fuses for each drive line on same side of array as Driver Panel that the line came from. (Even number of planes counting Spare Plane.) Refer to page 0400

2. Tube Location

   a. Physical numbering of CMD and MOA tubes Refer to pages 0970 & 0980
   b. Octal (address) numbering of CMD and MOA tubes.

3. Component Location

   a. MOA and CMD Circuits Refer to page 0990

4. Connections to Unit 8 or 11

   a. P1 - inputs and service voltages Refer to page 0980
   b. P2 - Filaments & Logic 0.1.5
   c. P3 - Outputs

C. Summary Questions

1. Answer the following questions TRUE or FALSE.

   a. The 64 Y line current drivers are divided into four equal groups. _____

   b. Two memory driver panels are located on each side of Unit 11.

Core Storage Element

c. Drive line terminating resistors are located on the same side of the array as the driver of those lines. _____

d. All lines are driven from the top of the array to the bottom. _____

e. Panels A and D contain X drivers _____

f. DMD's, MOA's and CMD's are located in the driver panels. _____

g. One DMD is located in one driver panel. _____

h. One physical tube on the driver panel contains one MOA. _____

i. All input and output signals enter and leave the driver panel through the same plug. _____

j. Some MOA components are located in Unit 10. _____

XI. Array Connections from Units 10 and 12

A. Physical Location

1. SA's

a. Left half word
b. Right half word
c. Parity

Refer to page 1020

2. DPD's

a. Left half word
b. Right half word
c. Parity

Refer to page 1020

NOTE: Left half word in Unit 10, Right half word in Unit 12.

Unit 7 or 10

PU	Modules A	B	C
C	Memory pulse distributor number 1 (clock)	Memory pulse distributor number 2 (clock)	MGG X read odd
D	Inhibit gate gen left half-word	Memory pulse distributor number 3 (clock)	
E	Clr mem control PA's sample left half-word	Spare	MGG X write odd
F	Sense ampl bit L15	Digit plane driver bit L15	
G	L14	L14	MGG X read even
H	L13	L13	
J	L12	L12	MGG X write even
K	L11	L11	
L	L10	L10	X read gate gen X write gate gen
M	L9	L9	Spare
N	L8	L8	Spare
P	L7	L7	X MAR 2^0
R	L6	L6	PCF X MAR 2^0, 2^1
S	L5	L5	X MAR 2^1
T	L4	L4	X MAR 2^2
U	L3	L3	PCF X MAR 2^2, 2^3
V	L2	L2	X MAR 2^3
W	L1	L1	X MAR 2^4
X	L0	L0	PCF X MAR 2^4, 2^5
Y	Parity	Parity	X MAR 2^5

Unit 9 or 12

Modules A	B	C	PU
MGG Y read odd	Spare	Spare	C
	Spare	Inhibit gate gen right half-word	D
MGG Y write odd	Spare	Spare	E
	Spare	Sample gate gen	F
MGG Y read even	Digit plane driver bit R15	Sense ampl bit R15	G
	R14	R14	H
MGG Y write even	R13	R13	J
	R12	R12	K
Y read gate gen Y write gate gen	R11	R11	L
Spare	R10	R10	M
Spare	R9	R9	N
Y MAR 2^6	R8	R8	P
PCF Y MAR 2^6, 2^7	R7	R7	R
Y MAR 2^7	R6	R6	S
Y MAR 2^8	R5	R5	T
PCF Y MAR 2^8, 2^9	R4	R4	U
Y MAR 2^9	R3	R3	V
Y MAR 2^{10}	R2	R2	W
PCF Y MAR 2^{10}, 2^{11}	R1	R1	X
Y MAR 2^{11}	R0	R0	Y

LAYOUT OF MEMORY PLUGGABLE UNITS

B. Array Connections from SA's and DPD's

1. Units 10, 11 and 12 Arrangement Refer to Page 1040 and Logic 0.1.7

   a. Unit 11 (Array) between 10 and 12.

   b. Unit 11 Rear side between 10 and 12.

      1) Front side of Unit 11 corresponds to wiring side of Units 10 and 12.

   c. Left half word SA's and DPD connections on left rear corner of array. Right half word SA's and DPD connections on Right rear corner of array. Refer to Page 1040

NOTE: Correlate terminal board and edge connector location in Array Unit layout on Logic 0.1.7. Refer to Page 1050

EXAMPLES:

1) DPD wiring for L15. Logic 0.1.6 and 0.1.7 DPD lines to Left Rear corner of Plane 4 from 10 BFF6. Lines Make 90% turn in plane 4 and come out on rear side of Plane 4. They then jumper up and into Plane 3 on rear side of array.

2) DPD wiring for R15, Logic 0.1.6 and 0.1.7 DPD lines to Right rear corner of Plane 3 from 12 BGF6. Lines make 90% turn in Plane 3 and come out on rear side of Plane 3. They then jumper down to Plane 4 on rear side of array.

3) SA wiring for L15. Logic 0.1.7 and 0.1.6 SA lines come out of Plane 3 to board 11E14. Wires then go to edge connector points 11B1e and 11B1g. From these points lines go to 10AFA1 and 10AFA5 and into SA.

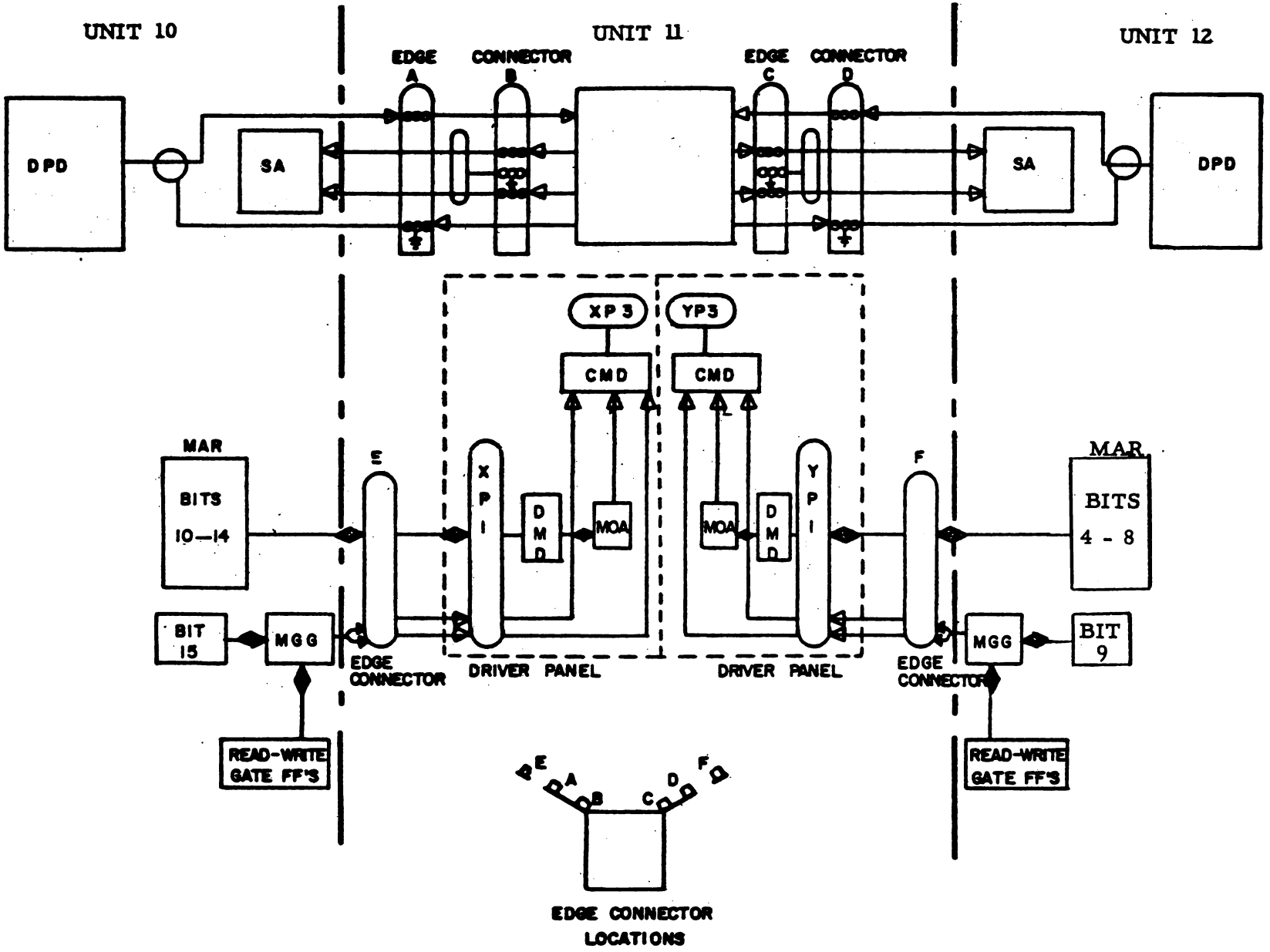
4) SA for R15. Follow wiring and location the same as for L15.

Other Connections and Locations of Components in Unit 11.

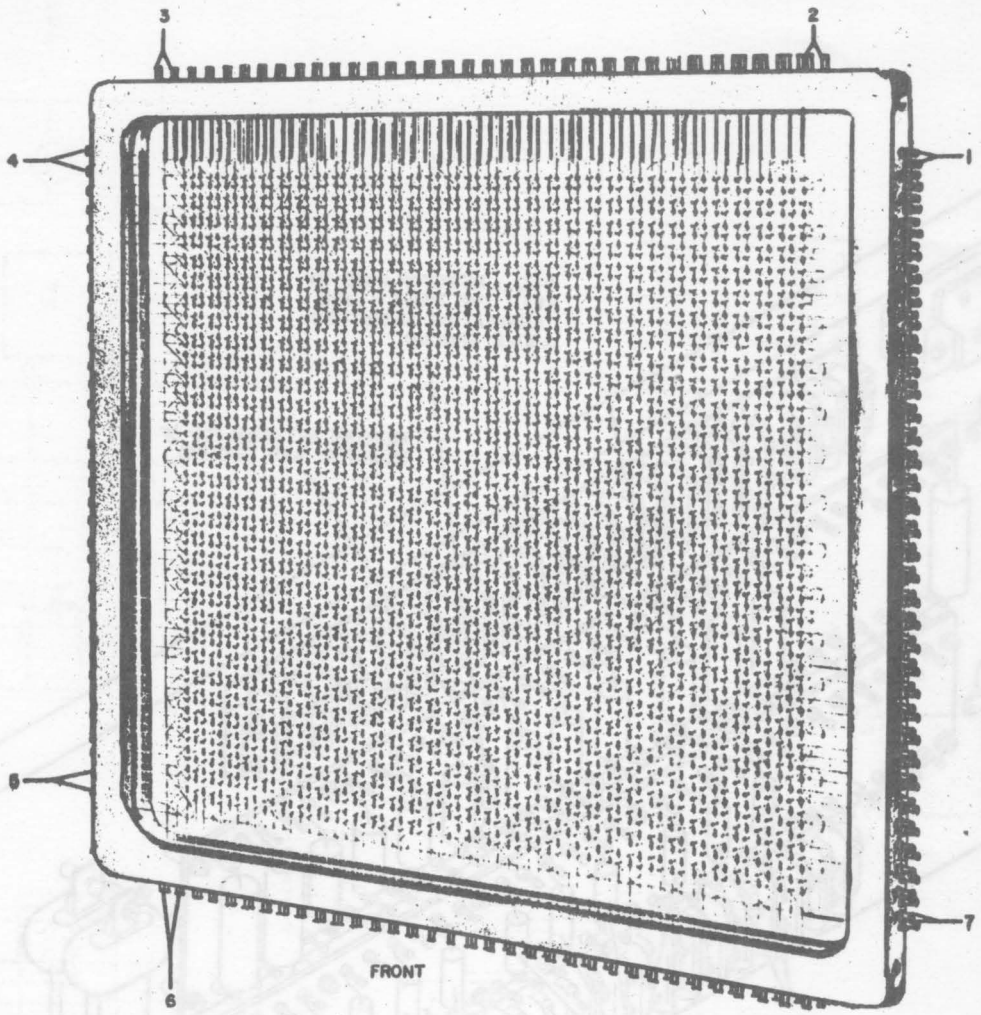
1. Clamping diodes and their location on Unit 11. Logic 0.1.5 and 0.1.7.

2. Service voltage terminal board and RC filters. Logic 0.1.7. Refer to Page 1060

3. Filament Transformers on Logic 0.1.7.



CORE MEMORY INTER — UNIT CONNECTIONS

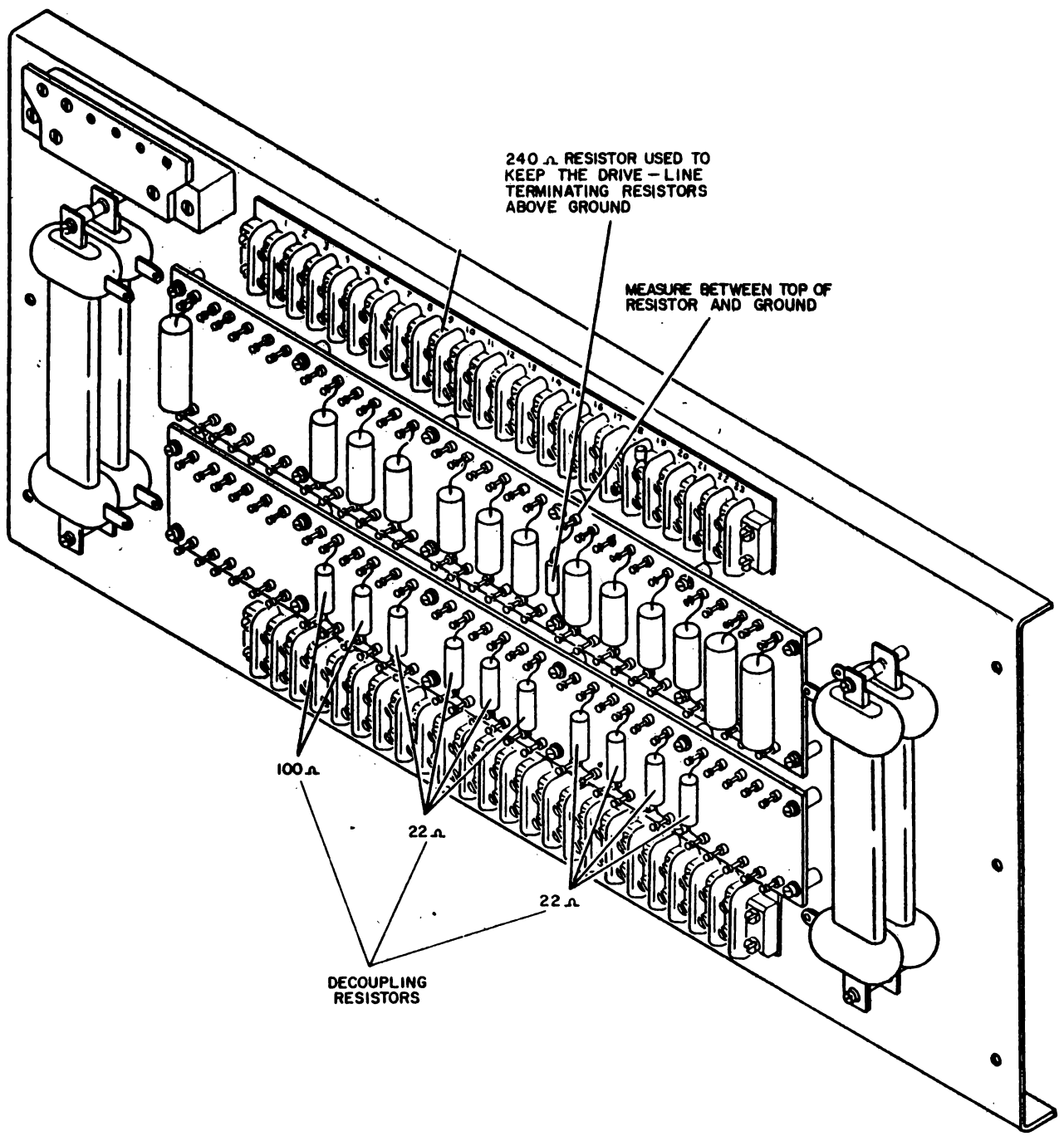


FERRITE CORE MEMORY PLANE

Note: The following legend is based on the analyzation of an odd plane (plane 5). A similar analysis is applicable between the corresponding numbers of all other active planes.

1. **Connection from DPD for the inhibit winding of plane 6.**
2. **Jumper from plane 5 to the inhibit winding of plane 6.**
3. **Inhibit winding connection for plane 5 jumpered from plane 6.**
4. **Sense winding connection for plane 5.**

5,6,7. **Jumpers within plane 5.**



DC DISTRIBUTION PANEL ASSEMBLY

(UNIT 11, E8, E9 and E10)

D. Summary Questions

1. The SA's, DPD's and the inhibit gate generator FF for the Left Half word are all located in Unit 10. _____

2. L15 DPD wires go thru plane 4. _____

3. PU 10AR contains the SA for bit Right 6. _____

4. Tube number 6 in PU 12 CX is the detector stage. _____

5. All DPD windings go thru two planes. _____

6. All fuses and termination resistors for the left half word are located on 11E26. _____

7. SA PU pins A2 and A6 are used to decrease PU pin connection resistance. _____

8. Mem. Buff. FFR8 is located in PU 3GP. _____

9. The Parity Bit SA is located in Unit 10. _____

10. Filament transformers are located in rows A & B. _____

Memory Testing

A. Purpose

1. The purpose of memory testing is twofold. to insure that the memory design is adequate so that it can successfully operate under all possible conditions; to anticipate equipment failure due to component deterioration and thus prevent failure during an operational program.

2. In the design and building of a memory, engineering effort is concentrated on finding and eliminating all the problems concerned with the operation of a memory from a

circuit and analytic point of view. Since the memory is run from a computer and must operate in conjunction with a program, a series of programs should be used to check out the final memory design. When the memory operates with the test program under the prescribed margins it can be considered a finished product, devoid of all known problems.

3. The use of test programs to assist in the solution of memory problems can be very advantageous for several reasons:

   a. The running of a test program with margins is a nearly infallible evaluation of the nature and extent of memory design problems and will clearly indicate the memory problem areas. The test program can save time by having the computer print out the exact area that needs the most work. It is also entirely possible that the program will indicate an unsuspected problem area. On the other hand, a circuit design problem may prove insignificant as far as the operation of the program is concerned.

   b. The running of a test program which provides a thorough analysis and printout of the failure pattern gives a much more complete picture of the memory failure than could be obtained otherwise. This, alone, can save many engineering manhours of study when it comes to defining a problem area.

B. Programming for Field MAintenance

1. The field program should comprise one master deck which provides the function of reliability, marginal check and tuning.

   There are three general classifications of maintenance programs:

   a. Reliability - designed to test the equipment as stringently and frequently as possible in order to introduce all situations where a failure is possible.

   b. Diagnostic - designed to check out individual pieces of equipment in detail to provide complete information as to which circuits are failing. This information can be obtained effectively with margins.

   c. Marginal Check - designed to indicate deteriorating components which need replacing.

2. In memory testing, all three types are combined into one program, as it is not possible to write a single program that will accurately diagnose memory failures.

3. The purpose of the field program is to find circuit failures before they cause a loss of computer time. This is done by providing a reliability test which creates worse noise patterns than any other program and a marginal check portion which anticipates circuit failures by stimulating aging conditions and causing the more deteriorated components to fail.

4. In order to produce memories of desired reliability it is necessary to provide adjustments on various circuits to compensate for manufacturing variations. The setting of these adjustments with the program and margins can be made very efficiently by providing an audible indication of failure rather than a printed one. Thus the maintenance personnel can make adjustments and immediately know the results rather than having to return to the console, to select a printout and to wait for it to be run.

5. When possible, the test program should not be contained in the memory undergoing test but in a separate memory.

C. Basic Slow-Speed Tests

1. These tests provide a check which should reveal almost any solid trouble in memory. They should be very simple and run at a slow speed to give a simple signal which is easy to analyze and gives maximum assistance to the debugging of a newly-built memory.

2. 1's Discrimination, in this test, every location in memory is loaded with all 1's and then checked to see if all 1's can be read out. This test shows the memory's ability to write and read 1's correctly. It checks the following equipment:

   a. Memory Buffer Register (1's side only)

   b. Memory pulse distributor except inhibit controls

   c. Sense Amplifiers and path to memory buffer register

   d. Ferrite core array

   e. Driving Circuits

3. 0's Discrimination, in this test, every location in memory is loaded with all 0's and then checked to see if all 0's can be read out. This test shows the memory's ability to write and read 0's correctly. It checks the following equipment:

   a. Memory Buffer Register 0 side and paths to digit plane driver

   b. Digit plane drivers and control circuits

   c. Sense amplifier ability to block pulses from the array.

4. Addressing Test, in this test each location in memory is loaded with a constant, identical to the address of that location. Each location is then read and checked to see that it contains the proper constant. This test shows whether each location in memory can be distinctly addressed. The following circuits are checked in addition to those checked by 1's and 0's discrimination:

   a. Memory Address Register

   b. Address Decoders

   c. All memory drivers

   By using the addressing test in combination with the 1's discrimination and 0's discrimination tests, errors can be isolated to a smaller portion of the memory.

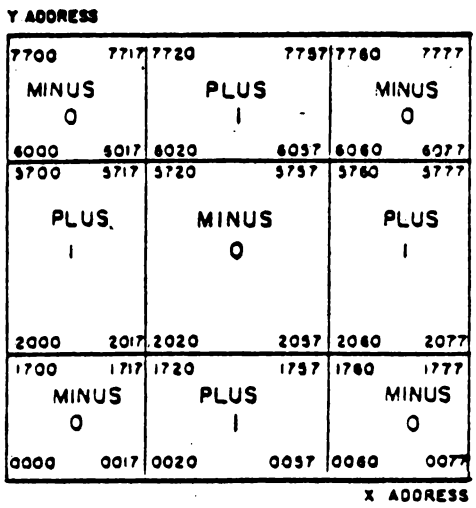
D. Checkerboard-Complement Test

1. The checkerboard pattern in memory is a group of 1's and 0's arranged so that the address (in octal designation) pattern of 1's and 0's resembles a group of rectangles and squares similar to the physical arrangement of a checkerboard. These configurations of 1's and 0's are used produce smaller 1 outputs and larger 0 outputs than are possible with other arrangements of 1's and 0's. The principal use of the checkerboard is to check the operation of memory when the resultant indication of 1's and 0's is the poorest. There are two types of checkerboards; the regular checkerboard and the inverted checkerboard. The arrangements of 1's and 0's by address for both checkerboards is illustrated.

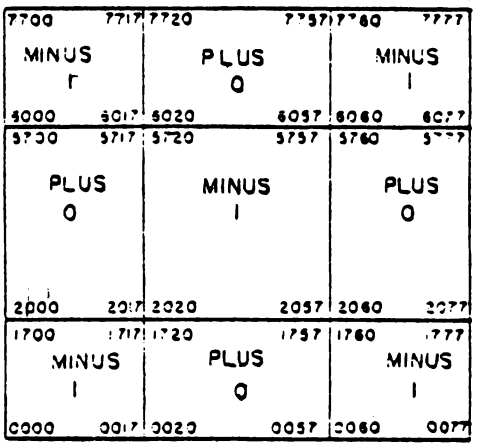
Refer to Page 11

2. Addressing

   a. An address in memory is designated by bits R4 through R15. Bits R4 through R9 designate the Y address, and bits R10 through R15 designate the X address. An address, then, merely states which X and Y core memory drivers (CMD)

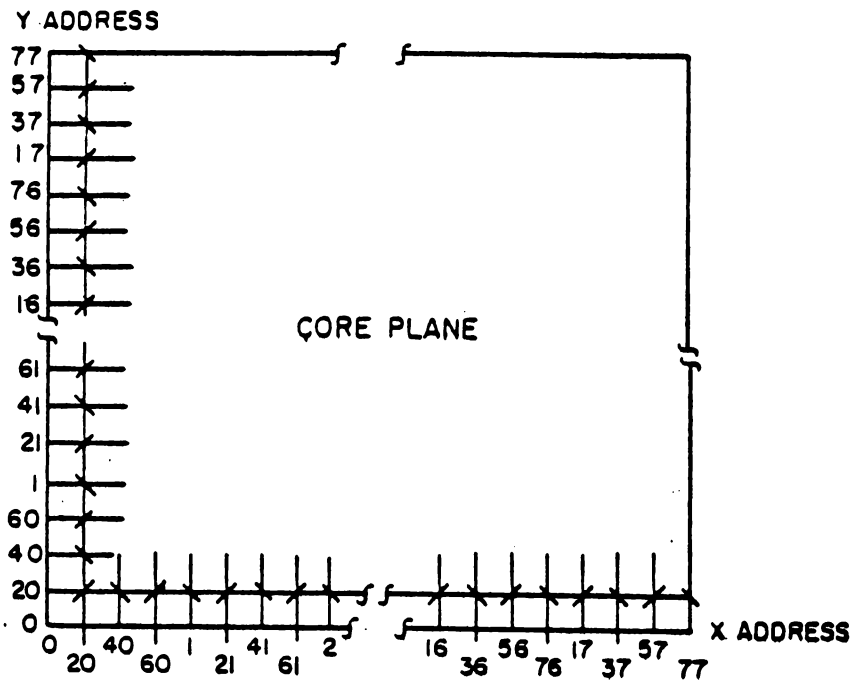


OCTAL ADDRESSES OF REGULAR CHECKERBOARD (MINUS AND PLUS INDICATE CORE POLARITIES)



OCTAL ADDRESSES OF INVERTED CHECKERBOARD (MINUS AND PLUS INDICATE CORE POLARITIES)

CHECKERBOARD PATTERNS



OCTAL ADDRESSES IN MEMORY

are selected. In the memory array, the $(100)_8$ or $(64)_{10}$ X and $(100)_8$ or $(64)_{10}$ Y core memory drivers are located on eight panels, each containing $(20)_8$ or $(16)_{10}$ core memory drivers.

b. To keep wire lengths to a minimum and to make a neat package, each successive core memory driver is physically attached to every fourth line coming out of the array. This means that successive addresses are four physical lines apart. The octal addressing by lines in the array is illustrated. Refer to Page 1.

3. Arrangement of 1's and 0's to form checkerboard

a. The X and Y lines in an array contain a similar number of plus and minus polarities; therefore, cancellation of the half-selected outputs tends to take place. However, a half-selected 1 output is larger than a half-selected 0 output, and this difference is defined as the 0-voltage. An arrangment of 1's and 0's that causes the 0-voltage to be added or subtracted from the desired output is known as the checkerboard.

b. If 0's are placed at the negative polarities and 1's at the positive polarities, the voltages from these half-selected 0's and 1's will not cancel completely. Some net positive voltage will appear in the sense amplifier winding and will be the sum of all the 0-voltages. These 0-voltages can be made to add or subtract from the desired output.

4. Outputs of Checkerboard

a. There are eight distinct possibilities for the 0-voltage to combine with the 0's and 1's.

POSSIBLE o-VOLTAGE COMBINATIONS

Condition	Core Output	o-Voltage	Resultant Output Voltage
1	Positive 1	Positive	Larger positive 1 output
2	Positive 1	Negative	Smaller positive 1 output
3	Negative 1	Positive	Smaller negative 1 output
4	Negative 1	Negative	Larger negative 1 output
5	Positive 0	Positive	Larger positive 0 output
6	Positive 0	Negative	Smaller positive 0 output
7	Negative 0	Positive	Smaller negative 0 output
8	Negative 0	Negative	Larger negative 0 output

b. Conditions 2 and 3 produce a smaller indication of a 1. Conditions 5 and 8 produce larger 0's; i.e., they tend more to a 1 output. These conditions are undesirable in the operation of the memory. Figure 1 (a) shows lines X4 and Y4 of the 8 by 8 array, with 1's at the positive locations and 0's at the negative locations. This is the regular checkerboard. The core at the junction of the X and Y lines contains a negative polarity 0. When this core is read out, the positive o-voltage subtracts from the negative output and tends to make the output smaller. This is a desirable situation, since little or no output is desired when reading out a 0. However, if a 1 is now stored at this position and then read out, the positive o-voltages again subtract from the negative output, resulting in a smaller negative 1. This is an undesirable situation because the 1 output is made smaller. Refer to Page 1140

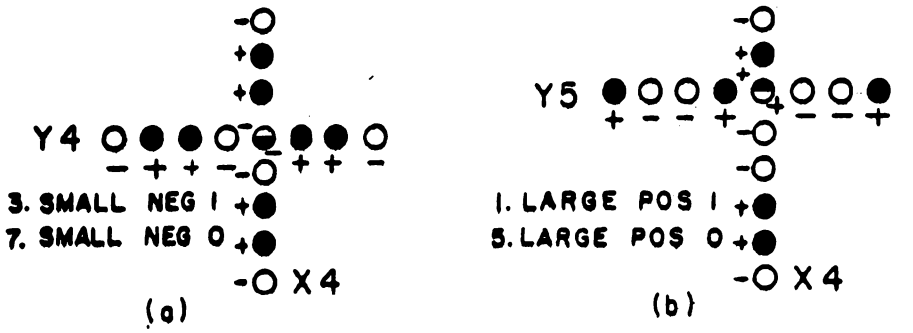
c. To achieve this smaller 1 output, a 1 must be written at a negative polarity location. This is a deviation from the general definition of the regular checkerboard; therefore, the difficult portion of this test is achieved when the original contents are complemented. To describe this test more completely, the term complemented checkerboard is used. Figure 1 (b) shows line X4 and Y5 of the 8 by 8 array. When reading out the positive 1 contained at this junction, the positive o-voltages now add to the 1 output, resulting in a larger positive 1 output. This is a desirable situation. When this location is complemented and the 0 is read out, the positive o-voltages combine with the 0 output, resulting in a larger positive 0 output. This large positive 0 is not desirable because it tends to yield a 1 output when a 0 is desired.

d. Figures 1 (c) and (d) show the conditions for obtaining the larger negative 0 and the smaller positive 1, respectively, which are both undesirable conditions. It should also be noted that these two figures are a result of having 1's at the negative locations and 0's at the positive locations. This is the inverted checkerboard.

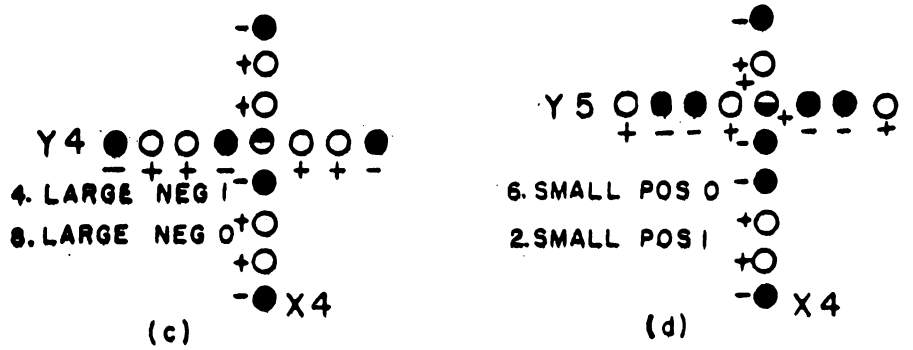
E. BASIC HIGH-SPEED TESTS

1. Basic high-speed tests provide a check of the ability of a memory to operate properly at its normal speed when executing a program. In general, these tests are executed by reading out of the memory at its operating speed, by reading out all locations, or by reading out a single location repeatedly.

2. A basic high-speed test is the checkerboard test at maximum repetition rate. A checkerboard pattern is loaded into the memory and then read out at maximum repetition rate. This test actually assists the 1 and 0 output because the polarities



CONDITIONS FROM REGULAR CHECKERBOARD



CONDITIONS FROM INVERTED CHECKERBOARD

LEGEND:

○ ZERO ◒ ZERO COMPLEMENTED TO ONE FOR TEST

● ONE ◓ ONE COMPLEMENTED TO ZERO FOR TEST

FIGURE 1 OUTPUTS FROM CHECKERBOARD PATTERNS

involved are additive. The test is critical because it produces the maximum amount of inhibit noises when 0 is written. This can be a problem in two respects:

a. The inhibit noise from a cycle where 0 was written can cause an error during the read portion of the cycle following.

b. The inhibit noise can build up an oscillation in the sense winding due to the continuous running.

3. In general, this test will make the sense winding output look quite unsatisfactory.

F. PROGRAMMING TECHNIQUES FOR WORST PATTERN TESTING

1. As previously stated, there are two undesirable conditions for reading from core memory. Disregarding polarity, these conditions are reading of a 0 which is made to approach a 1 value, and reading a 1 which is made to approach a 0 value.

2. Considering first the case where the reading out of a weakest 1 is desired, it has been shown that a straight complement checkerboard test tends towards this condition. Due to the fact that in complementing the 1 to a 0 the 1's on the selected X and Y lines are left in the read-disturbed state, the o-voltages produced by the straight complement checkerboard test is not the largest. The largest o-voltage is produced by pairing read-disturbed 0's with write-disturbed 1's on the selected line. Therefore, if all the 1's on a selected line are write-disturbed, and all the 0's are read disturbed, the o-voltage is maximum and the worst possible signal-to-noise ratio is produced.

3. Considering this condition in connection with the overall regular checkerboard pattern, the conditions to be established for any particular core appears as shown in figure 2. In this figure, if 6370 is the location to be tested, all the 0's on the Y(63) line should be weak 0's or read disturbed, and all the 1's should be strong 1's or write disturbed. The same may be said concerning the 1's and 0's on the X(70) line. Refer to Page

a. To accomplish this test, the procedure is as follows;

1) Load the regular checkerboard pattern. The status of the selected core will be 0. The status of half-selected 1's on the selected line will be indefinite 1, and the status of half-selected 0's on the selected line will be indefinite 0.

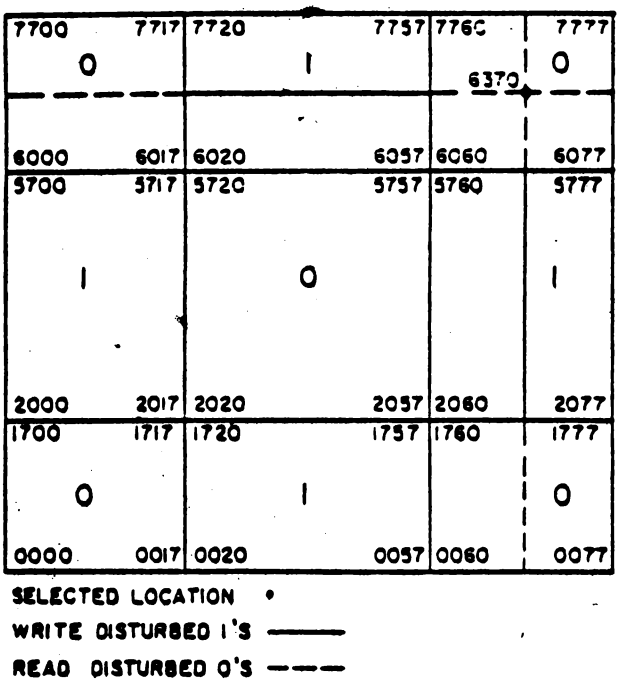


FIGURE 2 CHECKERBOARD PATTERN FOR TESTING FOR WEAKEST 1's

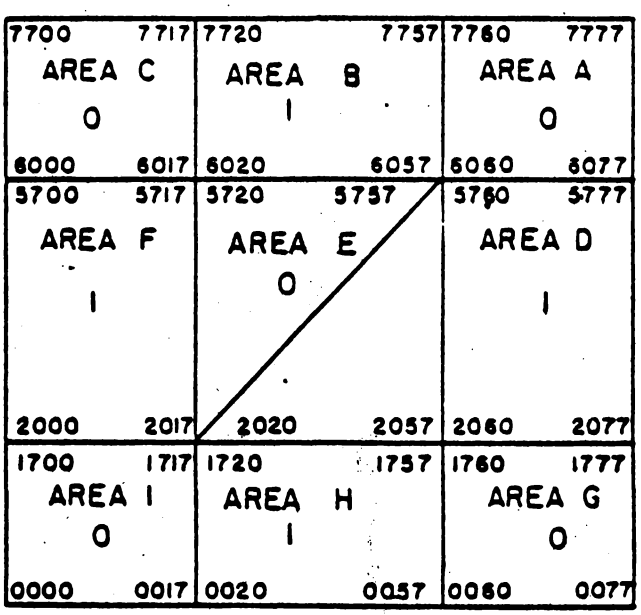


FIGURE 3 DIAGONAL FOR TESTING IN AREAS A, C, G, AND I FOR WEAKEST 1 READ-OUT

2.) Place a diagonal of 1's in area E, as shown in figure 3. The status of the selected core will be indefinite 0. The status of the half-selected 1's on the selected line will be write-disturbed 1's. The status of half-selected 0's on the selected line will be indefinite 0. Refer to Page 1160

3.) Complement the test location. To do this, clear and subtract and full ~~shape~~ the test location. The status of the selected core will be a freshly written 1. The status of half-selected 1's on the selected line will be write-disturbed 1's. The status of half-selected 0's on the selected line will be write-disturbed 0's.

4.) Clear and add a location containing all 0's. The status of the selected core will be a read-distrubed 1. The status of half-selected 1's on ths selected line will be read-disturbed 1's. The status of half-selected 0's on the selected line will be read-disturbed 0's.

5.) Clear and add all the locations along the chosen diagonal for the area being tested. This causes the 1's on the selected X and Y lines to become write disturbed. The status of the selected core will be read-disturbed 1's. The status of half-selected 1's on the selected line will be write-disturbed 1's. The status of half-selected 0's on the selected line will be read-disturbed 0's. The test condition is now set up.

6.) Read out the test location and check to ascertain that its contents are all 1's. Restore the test location to its original value.

7.) Repeat steps 3 through 6 for all locations in areas A, C, E, G, and I. This will test the read-out of weakest negative 1's from these locations.

b. When testing Area E for weakest 1, place diagonals in areas A and I as shown in figure 4. Refer to Page 1180

c. The same basic procedure is used for testing the reading of weak positive 1's using the inverted checkerboard pattern, except that the diagonals used are necessarily different. The diagonals used are shown in figures 5 and 6. Refer to Page 1200

d. By using both the regular and inverted checkerboard patterns, the read-out of both weak negative and weak positive 1's is accomplished.

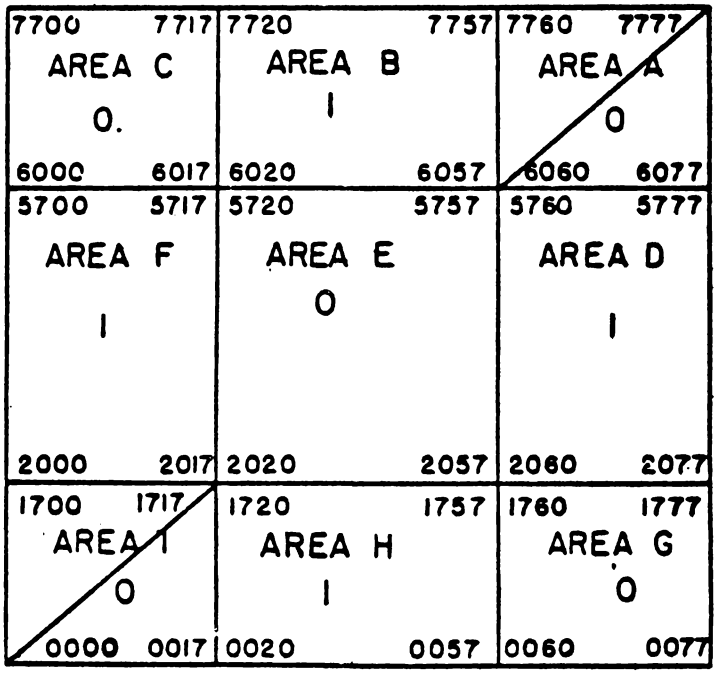


FIGURE 4 DIAGONALS FOR TESTING IN AREA E FOR WEAKEST 1 READ-OUT

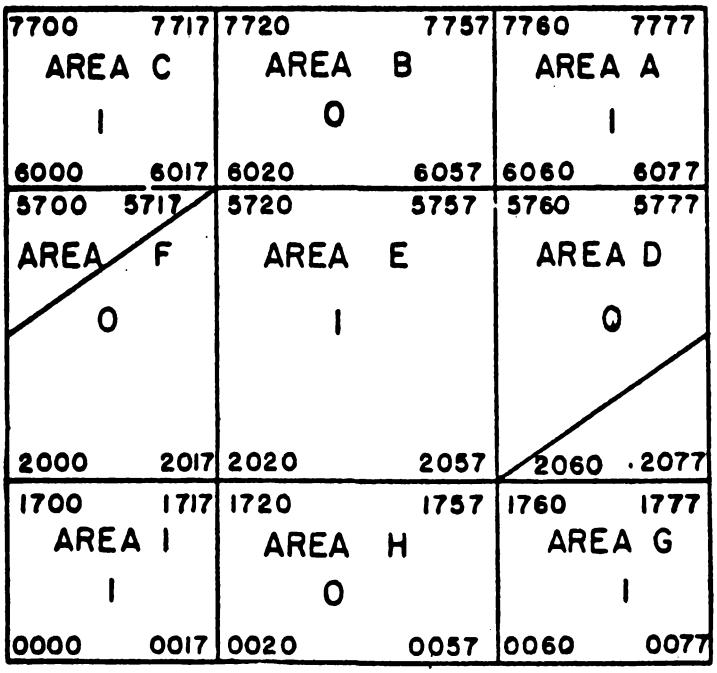


FIGURE 5 DIAGONALS FOR TESTING IN AREAS B AND H OF INVERTED CHECKERBOARD FOR WEAKEST 1 READ-OUT

4. Testing for Strongest 0's

a. The second case to be considered is the reading out of the strongest o's. The conditions necessary for a complement test which yields the strongest 0 output are similar to that of the weakest 1, except that the test areas of the checkerboard are reversed. This variation causes programming of this technique to be more cumbersome. Consideration must be given to the conditions necessary to yield the desired read of the strongest 0's. A location from an area of the checkerboard containing 1's must be complemented. All the 0's on the coincident lines of the complemented location must be weak or read disturbed. The 1's on these coincident lines must be strong or write disturbed.

b. In figure 7, location 7042 is assumed to be the complemented test location. Consequently, all the 1's on the Y(70) line must be write-disturbed and the 0's must be read-disturbed in order to effect a strongest 0 read-out. These same conditions are true for the 1's and 0's on the X(42) line. Refer to Page 1200

c. General Procedure

1) Load the regular checkerboard pattern. The status of the selected core is indefinite 1. The status of half-selected 1's on the selected line is indefinite 1's. The status of half-selected 0's on the selected line is indefinite 0's.

2.) Complement the test location. To do this, clear and subtract the test location and store it back. The status of the selected core becomes read-disturbed 0. The status of half-selected 1's on the selected line is read-disturbed 1's. The status of half-selected 0's on the selected line is read-disturbed 0's.

3) Disturb a series of lines according to the area of 1's the test location is in. Refer to (d) for an explanation of these lines. In disturbing some of these lines, it becomes necessary to skip certain addresses in order to leave the half-selected 0's on the coincident lines in the read-disturbed condition. Several groups of lines used are shown in figures 8 through 11. This process leaves all the 1's on the selected X and Y lines in the write-disturbed condition. The status of the test location is read-disturbed 0. The status of half-selected cores on the selected line is write-disturbed 1's. The status of half-selected 0's on the selected line is read-disturbed 0's.

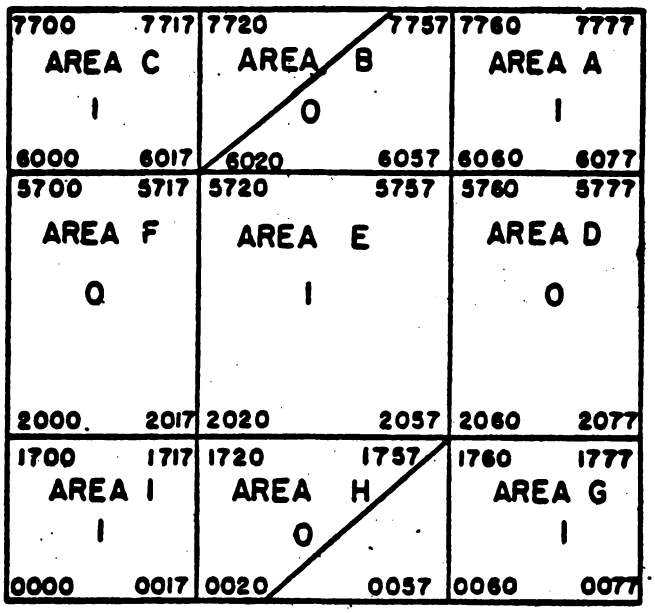


FIGURE 6 DIAGONALS FOR TESTING IN AREAS D AND F OF INVERTED CHECKERBOARD PATTERN FOR WEAKEST 1 READ-OUT

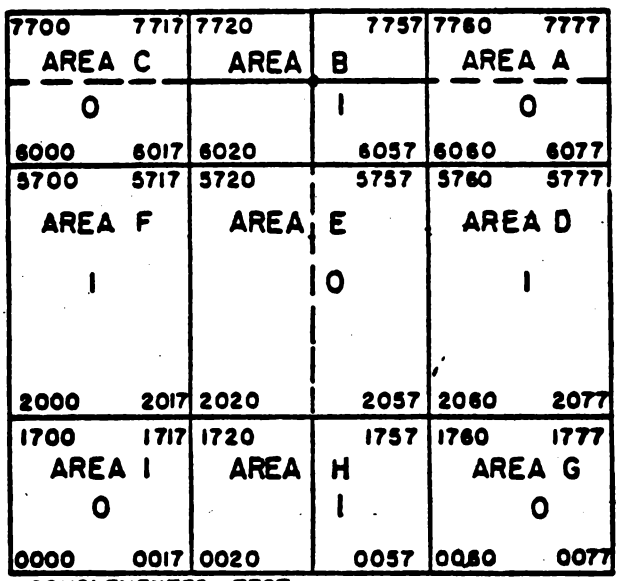


FIGURE 7 CHECKERBOARD PATTERNS FOR TESTING FOR STRONGEST 0's

4) Read out the test location and check its contents for all 0's.

5) Repeat steps 2, 3 and 4 for all locations in the test area excluding those necessary for disturb purposes.

d. The disturb lines for the different areas are shown in figures 8 through 11.

1) In figure 8, assume location 7040 to be the test location. Consequently, the line of 1's between 6020 and 7720 is disturbed, omitting location 7020. This is the location which, if it were disturbed, would cause the 0's on the Y(70) line to become write-disturbed. The line between 0020 and 1720 is also disturbed without omission. Finally, the line between 1720 and 1757 is disturbed omitting location 1740. If this location were disturbed, the 0's on the X (40) line would become write-disturbed. By disturbing along the same lines and omitting any location which contains the X or Y address of the test location, it is then possible to check all the locations in area B excluding the line used for disturbing.

2) In figure 9, assume location 1035 to be the test location. Consequently, the line of 1's between 0020 and 1720 is disturbed, omitting location 1020. This is the location, which if it were disturbed, would cause the 0's on the Y(10) line to become write-disturbed. The line between 6020 and 7720 is also disturbed without omission. Finally, the line between 6020 and 6057 is disturbed, omitting location 6035. If this location were disturbed, the 0's on the X(35) line would become write-disturbed. By disturbing along the same lines, and omitting any location which contains the X or Y address of the test location, it is then possible to check all the locations in area H excluding the line used for disturbing.

3) Figure 10 shows the lines used for disturbing when when testing area D for the strongest 0 read-out. The theory explained for figures 8 and 9 is identical for this case except for the variation in the chosen disturb lines.

4) Figure 11 shows the lines used for disturbing when testing area F for the strongest 0 read-out. The theory explained for figures 8 and 9 is identical for this case except for the variation in the chosen disturb lines.

5. CONCLUSION

a. The complement checkerboard tests are used to determine the operational status of memory during a discrimination test.

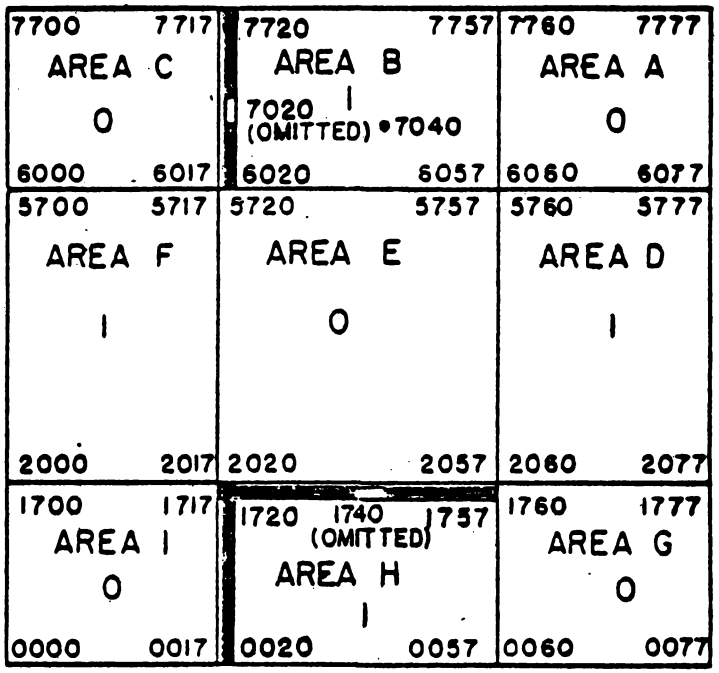


FIGURE 8 DISTURB LINES FOR AREA B

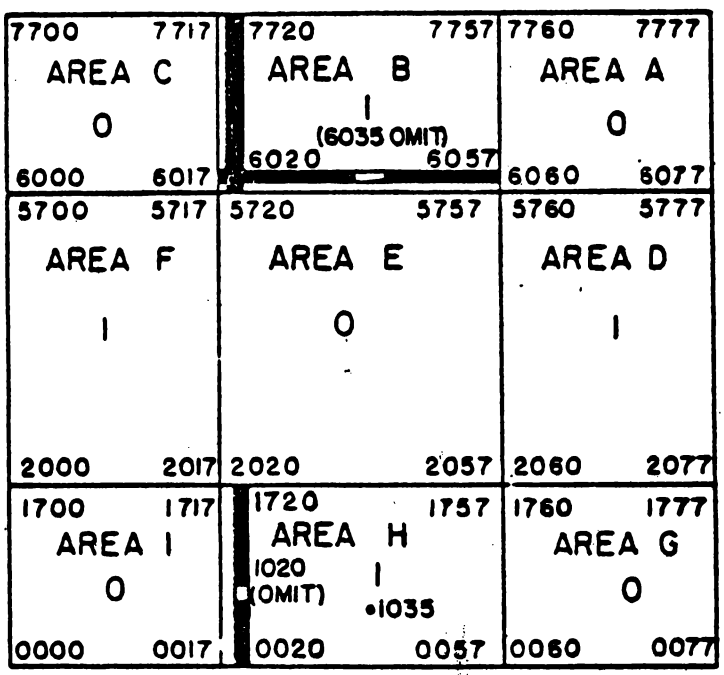


FIGURE 9 DISTURB LINES FOR AREA H

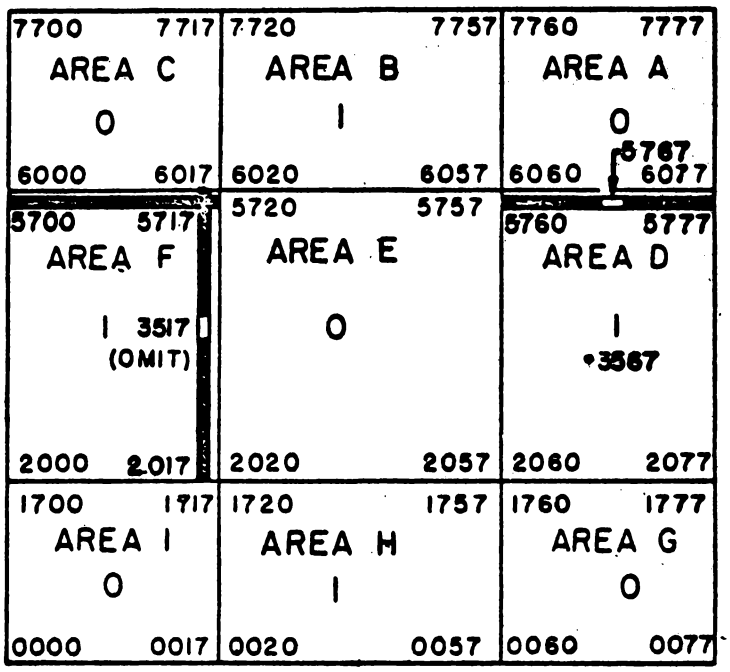


FIGURE 10 DISTURB LINES FOR AREA D

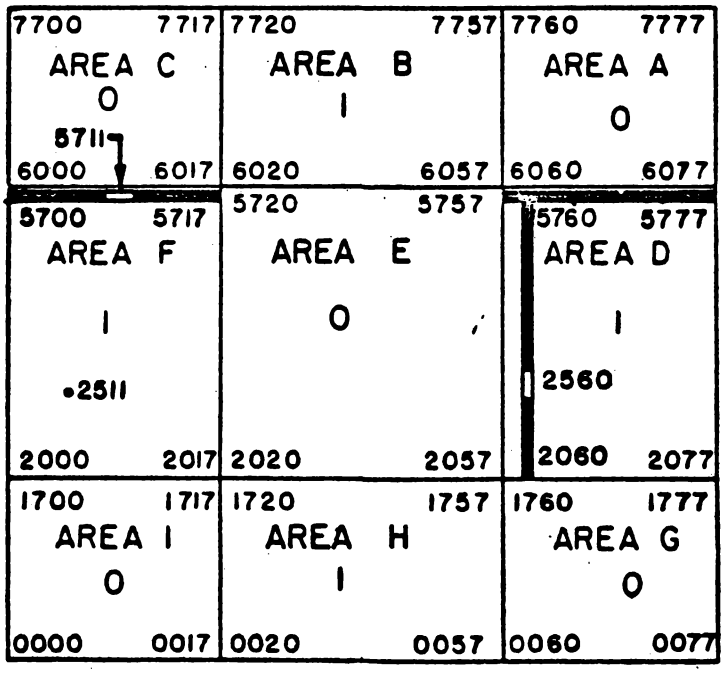


FIGURE 11 DISTURB LINES FOR AREA F

The worst pattern tests utilize the complement checkerboard, but with one important modification; i.e., the io-voltage is made to be a maximum. As a result, the discrimination test is the most severe because the 1's being read out are the smallest possible and the 0's being read out are the largest.

G. PROBLEMS IN MEMORY TESTING

1. Delta and Inhibit Noise

a. A pattern is loaded into memory and the maximum repetition rate operation is carried out. The pattern is such that inhibit noise from the previous cycle and delta noise from the read cycle combine to produce a maximum of noise upon readout. Refer to Page 1250

b. Since inhibit noise oscillates, it is necessary to determine the exact nature of the inhibit noise at the following sample time to decide whether a positive or negative fall of inhibit noise is desired.

2. Crosstalk

a. In general, the problem of crosstalk is that lines carrying pulse currents couple noise currents into nearby lines. This is a problem wherever most of the lines in the array and connecting cables run parallel, especially with respect to the sense lines.

b. The problem of crosstalk can be defined, mathematically, by the formula for inductive coupling. When an X or Y line is fully selected, it induces a current in the line adjacent to it. A general expression for this is: Refer to Page 106

$$I_2 = -k \frac{\Delta I_1}{\Delta t} \times L \times \frac{1}{a^2}$$

Where: I_2 = Induced current in adjacent line

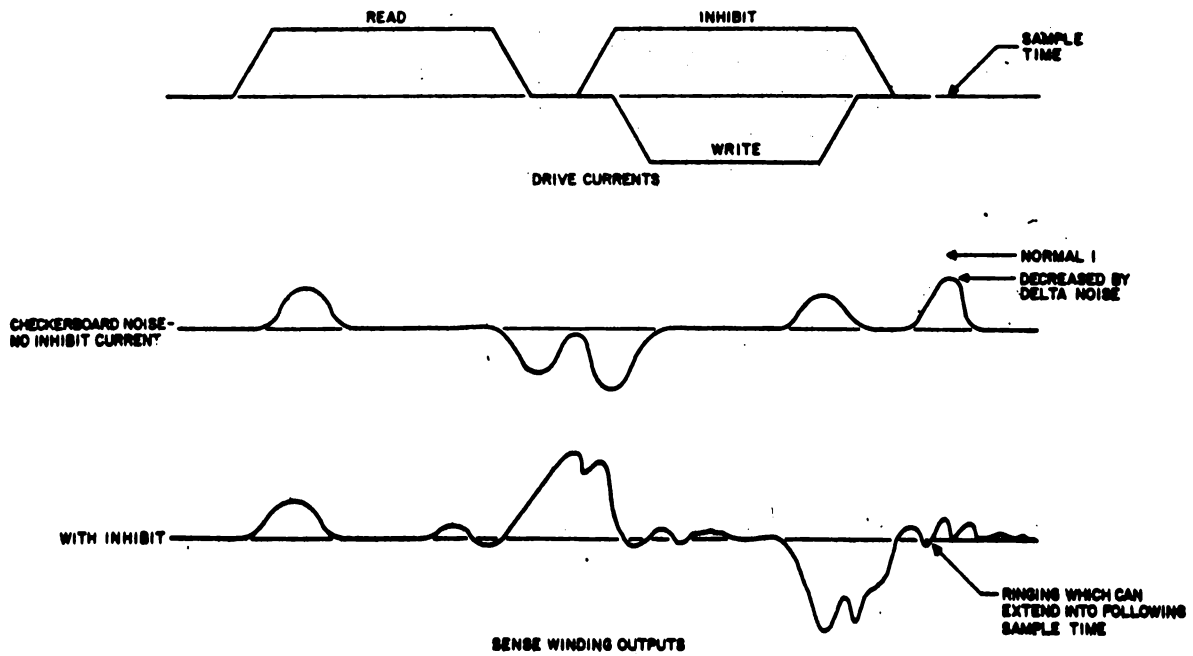
I_1 = Current in selected line

L = Distance along lines that are parallel

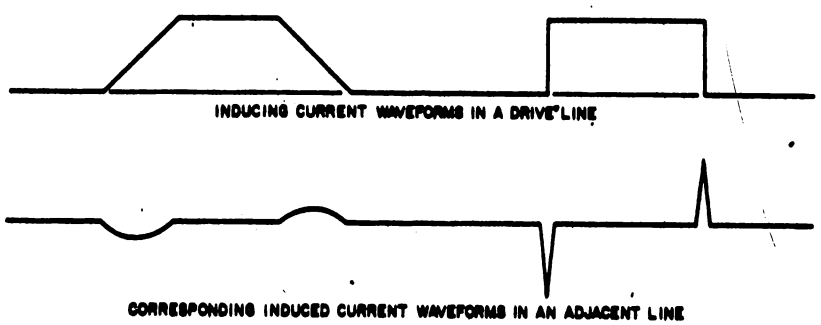
a = Separation of lines

k = Proportionality constant

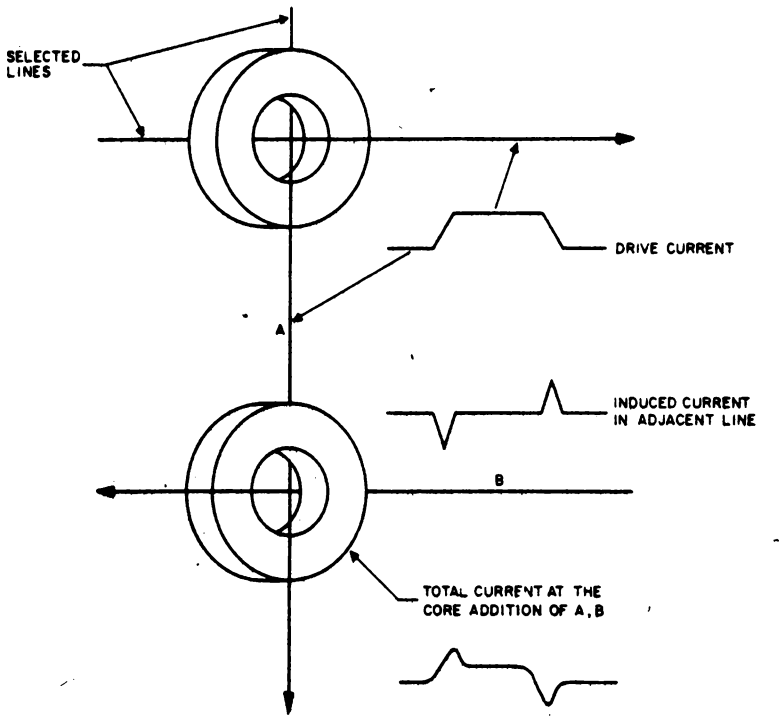
The minus sign (-) indicates that the induced current flows in the opposite direction to the inducing current.



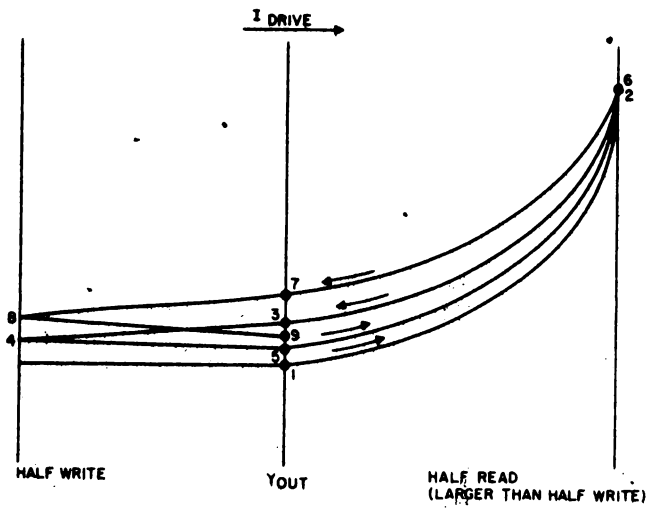
AN EXAMPLE OF TEST READ-OUT



INDUCED CURRENT WAVEFORMS



MUTUALLY-COUPLED CORES



ASYMMETRICAL CORE SWITCHING
("WALKING")

3. Crosstalk Between Sense Lines

   a. If all data bits in memory, except one, are 1's and the other data bit is a 0, it is possible for this 0 bit to turn into a 1 bit due to noise created by all of the other 1's. This noise pickup can occur in several places: in the array sense windings, in the connecting leads of the array, in the array unit connecting plugs and in the cables between the array unit and the sense amplifiers.

   b. Once the signal has emerged from the sense amplifier it is a standard signal and, theoretically, no longer a noise problem since all Central Computer signal handling is designed to eliminate this type of problem. However, if there is a long cable run between the memory unit and Central Computer it is still possible to pick up extra noise.

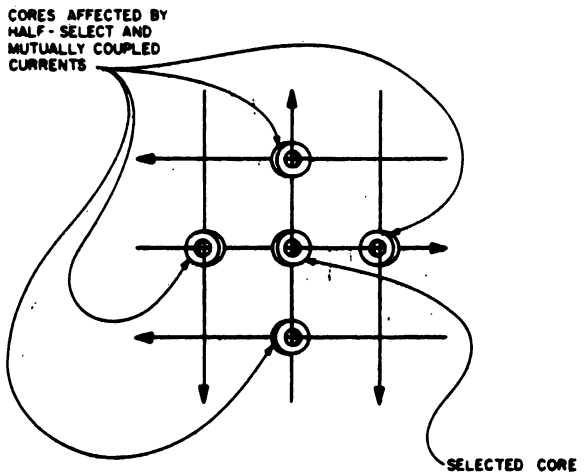
4. Crosstalk Between Digit and Sense Line

   a. The problem of crosstalk between digit plane and sense lines is similar to that of inhibit noise ringing into the following cycle, except that the problem is caused by direct crosstalk from digit plane wires to sense wires. If the drive currents were turned off entirely, and only the digit plane drive operated, this type of noise would still be present. Ringing can be minimized by a termination which will damp out oscillations as quickly as possible.

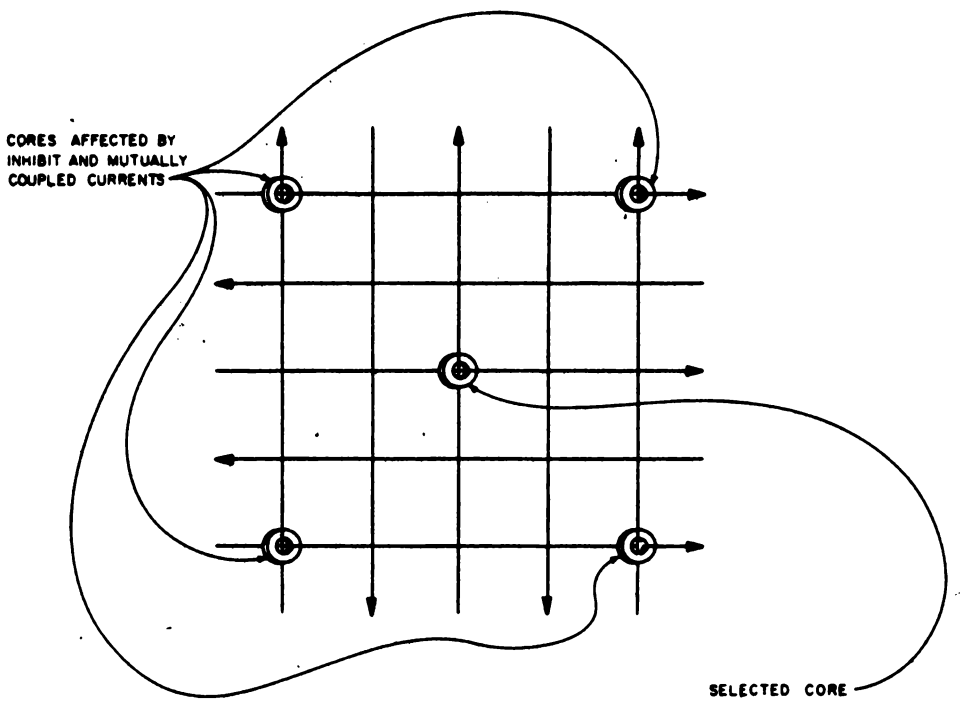
5. Crosstalk Between Driver Lines

   a. The X and Y drive lines run parallel throughout the array, resulting in a large amount of crosstalk. Examination of a pair of lines will show how mutual coupling produces unequal read and write currents (asymmetrical switching). Core B sees a half-read current with an additional spike of current as shown. This can condition the hysteresis state of the core further than would a half-read current and, thus, produce an increased noise condition in the memory. Refer to Page 1260

   b. The magnetic operation in asymmetrical switching is illustrated where it is assumed that a series of alternate read and write currents are applied with the write currents larger than the read currents. Successive cycles approach an irreversible magnetic state, each cycle being closer to an irreversible state by about 90 percent. The changing or shifting of a core's magnetic state by asymmetrical switching is known as "walking". Walked magnetic states are to be avoided because they can produce more noise than the read and write disturbed states. For instance, a read-disturbed 1 which has been walked further in the read Refer to Page 1260



(A)
WHEN READING OR WRITING a1



(B)
WHEN WRITING a0

CORES IN ARRAY AFFECTED BY MUTUAL COUPLING

direction will have an even greater half-read output since it is further from saturation.

c. The mutually-coupled current exists only as long as a rate of change in the inducing current takes place. Thus, to a certain extent, it can be assumed that the addition of the half-read and the mutually-coupled current do not produce a bit current greater than a half-read current.

However there are two considerations which make this assumption subject to error:

1) Due to the self-inductance and delay of the lines, it cannot be said that the induced current lasts exactly as long as the inducing rate of change.

2) The induced current is produced by one axis of the memory drive, while the half-select current to which it is adding, is produced by the other axis of the memory drive. These two drives are not fixed in time relation to each other nor are they necessarily simultaneous throughout the array.

6. A test for mutual coupling effects would be to create ferrite core delta noise conditions using the half-select current, plus the mutually-coupled current, in such a way as to produce a maximum noise similar to the checkerboard-complement, worst-pattern test. The details of such a test vary, depending on the memory design. The following cases will, in general, be present:

a. During the reading of a 1 or 0 and during the writing of a 1 the four adjacent cores are pulsed with a half-select.

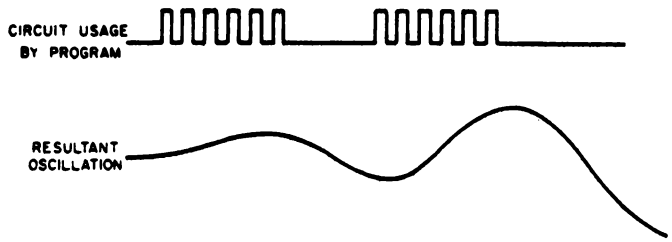
Refer to Page 1280

b. During the writing of a 0, the inhibit current combines with the mutually-coupled current two lines away, which is now in the opposite direction to produce noise in the read direction which combines with the inhibit current and two mutually coupled currents in the read direction.

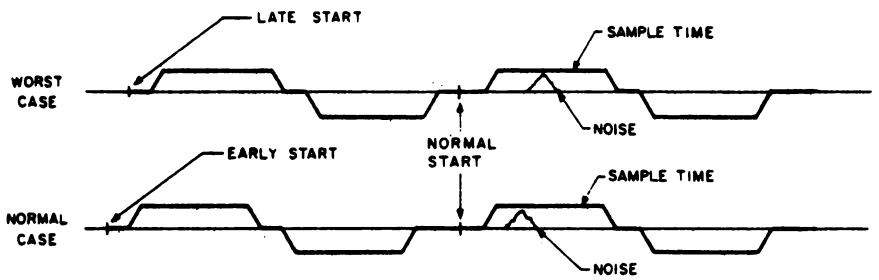
H. FREQUENCY SENSITIVITY TESTS

1. The problem is one of testing the entire system, in all possible modes of operation, to see that no frequency instability exists. It is difficult to define exactly what is being sought, except that each circuit should be tested. The method of testing is to subject the circuit to alternating periods of usage and nonusage. The length of the periods should be variable. The possible buildup of effects within a circuit tested at, or near, the resonant frequency is illustrated.

Refer to Page 1300



EFFECTS OF BURST DELAY
UPON A RESONANT CIRCUIT



WORST COMBINATION OF START MEMORY TIMINGS

I. VARIATION IN THE TIMING OF START MEMORY

1. In connection with the problem of interference between memory cycles, one further situation must be checked; the situation where the maximum amount of interference is created, and memory is started at its latest time, followed by a start at its earliest time. The result of this situation is an effective shortening of the memory cycle and aggravation of the interference problem because the noise extends later into the following memory cycle and affects the signal at sample time. Refer to Page 1300

2. Due to the fact that memory can be started from several address registers within the machine, there will be variations in the start memory time with respect to the Central Computer machine cycle. The two extremes are illustrated.

J. EARLY PEAKING CORES

1. When a ferrite core is deficient in ferrite material because of an air gap or a hard spot, its 1 output does not take as long to rise as does the 1 output of a normal core. In fact, the 1 output may occur so early that the sample pulse will miss its peak altogether. There are several ways to detect these early peaking cores.

2. By increasing the read current, the peaking time of all cores is decreased and failures will begin to occur. A plot can then be made of the number of failures vs. the read current amplitude from which a decision can be made to remove some of the worst offenders. It may be apparent that a few cores are seriously affecting the margins in which case they should be removed.

3. Another way of detecting early peaking cores is the use of a test which reads out the same location several times. This heats up the core and decreases its amplitude and makes it peak early.

K. THE PARITY BIT

1. The parity bit is an obvious aid to memory testing, for it indicates any memory failure involving an odd number of data bits. With a parity check, the memory test can omit the checking routine entirely whenever no parity occurs. It can be argued that an even number of bits might be in error, but the chances of this holding true for an entire test, are very small. Also, most of the simpler tests must use a checking routine regardless of parity indications, so that such types of failures would be detected in most cases.

2. The parity bit is a necessity for the development and debugging of new tests. It is sometimes true that a memory test will fail in some entirely unexpected manner. This failure is easily found by stopping on memory parity and analyzing the situation. Otherwise, this failure may never be noticed, and a design or operation problem would be un-noticed for some time.

3. The parity bit is also an aid in reassuring that the memory program has not itself been altered. It is important that the program perform its function exactly as intended. The parity bit is an important aid to the test debugging, for memory error printouts should occur if, and only if, a memory parity occurs.

L. A SEPARATE MEMORY FOR THE TESTING PROGRAM

1. A separate memory from which the test program can operate directly has several obvious advantages:

   a. It allows testing of all the locations in the memory at once; otherwise, two programs are required.

   b. It allows uninterrupted testing. Without a separate memory, the program must be reloaded when a failure causes destruction of the program. If a single memory must be used, some type of storage, as drums or cards, in addition to cards should be provided to minimize reloading time.

   c. It allows complete testing of some types of operation which would not be otherwise possible.

   d. It allows a more complete breakdown of the error and thus a more informative printout. Otherwise, error data must be printed immediately or, if margins are used, stored elsewhere until the data can be reliably processed and printed.

   e. It allows a simpler operation of a marginal check program since drum or tape storage is not required.

M. FACILITY FOR THE READOUT OF MEMORY AT MAXIMUM SPEED

1. This is the facility to read all the information out of a memory and to rewrite each word as it is read at the maximum repetition rate. For reference, a parity bit in the data word is used, each word being checked for good parity and an alarm indicated if a bad parity word is read out. This facility allows a quick check for correct operation of the maximum repetition rate (MRR) test used.

2. The only other way of making this check of MRR operation is to place instructions in the memory and have the program operate as a noise pattern, itself. The reading or writing of drums from memory does not suffice as the memory usually operates with a shorter cycle than drums. Using a program, itself, to generate these noise conditions presents some major problems. The most obvious problem is that, since the program is designed to produce the maximum amount of noise during its operation, failure of any kind will produce a program modification, and the possibility of losing control of the program. The possibility of losing control of the program will be great, for the contents of each memory location and the sequence of the program would be combined so as to produce the greatest possible amount of noise, and likely memory failure. Loss of program control would then require manual intervention and could occur quite frequently. Another difficulty with the use of a program as a MRR test is that pattern words would be difficult to design. Not only does the effect of the word format upon the memory have to be considered, but the word format must be meaningful as an instruction, and if the address portion is referenced it must not alter the sequence of noise signals. In short, programming directly for worst noise, due to MRR, is not practical.

3. Another advantage of MRR operation is that the memory circuits can be tested for oscillation more effectively, since a particular circuit can be used at the MRR during the burst and consequently build up a greater noise than if it would be used at one-half or one-third of the MRR.

N. INSTRUCTION FOR COMPARING DATA WORDS

1. The problem of obtaining and analyzing error data becomes important from a time standpoint. Larger, more complex memory elements require a larger number of program steps to check and analyze its operation.

2. In order to check a data word, it is not sufficient to use a parity alarm, for the chances of getting an even number of bit failures increases considerably when margins are applied and failures encouraged. The thorough checking of memory requires the use of an instruction which makes a full comparison between the pattern word and the word just read out of memory. The parity bits should be included as part of this check. Inability to directly compare parity complicates the program considerably in checking for the correct status of the parity bit. At this point, the minimum requirement is the ability to determine the magnitude of the parity bit.

3. Lack of both a compare instruction and parity bit results in a program which ignores the parity bit altogether, except in one or two specially designed test routines. This is unfortunate as the parity bit and associated circuits are just as important as the data bits.

0. DATA REDUCTION

1. When a memory test program is run, basic analysis of its failure is simple. When certain addresses fail to store information correctly, the problem is to examine all such failures in an attempt to find which circuit is involved in all of the failures. This problem can lead to a monumental task, as a 64² memory can have upwards of 1,000 such failures. Considering the number of circuits and the combinations of addressing patterns that occur, it is evident that as memories get larger and more complex some tool will be necessary to aid in analyzing failures.

2. One solution to the problem is to take the raw error data and perform the correlation of error patterns and then to print out the results of this correlation. In this way, raw error data, which ordinarily would cover 228 pages and take two hours to print, can be compiled in five minutes and printed out on one page. For a moderately complex memory this is the only solution. Errors in the higher order address bits, for instance, would not become evident until a good portion of the 228 pages of raw data had been examined. Diagnosis of some address problems depends upon proper grouping of the address bits for reading, and recognition of certain patterns of failure.

3. Another aspect of the problem is that few memory failures are limited to only one circuit. There is always interaction of some kind between various memory circuits. Such an interaction could be a serious memory problem and its proper diagnosis could be vital. The diagnosis must permit all aspects of the failure to be seen readily in a meaningful breakdown.

4. To develop a useful data breakdown, time and experience on the machine provide the final criterion. The first attempt to analyze failure modes will most likely include some areas not necessary and others which experience will indicate require further breakdown.

5. In general, the procedure for setting up a data reduction system is as follows:

   a. Provide a total error count.

   b. Provide an error count for bits picked and dropped in each digit plane.

c. Provide an error count for each separate sense winding and associated sense amplifier.

d. Provide a count for each inhibit winding and its associated driver.

e. Provide a count for each individual X and Y driver circuit. It may not be necessary to show core selection matrices or switches because these are passive electrical networks which usually do not cause much trouble.

6. The above breakdown may seem sketchy but it will prove adequate for anyone with a little experience. Steps c and d can be accomplished by subdividing the array into squares whose size is determined by the sense windings in one direction and by the inhibit winding in the other. The assumption of a single error has proven to be a reasonable one in most cases so that tracing an error printout back to a single source will prove effective. The data derived will provide enough indications to arrive at the proper conclusion by a cross reference.

7. When a failure occurs along one axis, all lines in the other axis which cross the failing line will be affected in like manner. Thus an unbalanced distribution of errors among the elements of one axis indicates a failing element; whereas an equal distribution of errors among the elements of an axis indicates a trouble affecting all elements similarly.

8. At this point, an error print routine is as important as the test routine, for it is through the error print routine that Engineering is able to quickly and accurately determine the effects of the various tests upon the memory.

9. This program should be kept simple and easy to use, so that one has available a basic tool which is easy to use.

10. The program could be organized in four basic sections, as follows:

a. A front end control which converts a manual switch setting into the selection of the desired test routine. Selection should be such that any combination of routines may be selected, by using a separate switch for each routine, and such that, if no selection is made, all routines are run.

b. Test routines which perform the desired test upon memory by presenting error information to the error routine. The test routines should be closed routines.

c. An error routine which converts the error information presented by the test routine into the form desired by the operator and prints out. This should also be a closed subroutine.

d. Utility routines are closed subroutines which are used frequently, such as checkerboard loaders and checkers.

P. MARGINAL CHECKING

1. The major advantage of marginal checking during an engineering evaluation is to collect data on the operation of memory with respect to the relative effects of various tests, and with respect to the operation of memory over a period of time. This data is very important to the complete evaluation of all modes of memory operation in order to achieve an optimum design and maximum reliability. This data is also important as a basis for selecting a complete and efficient set of memory tests for the final program.

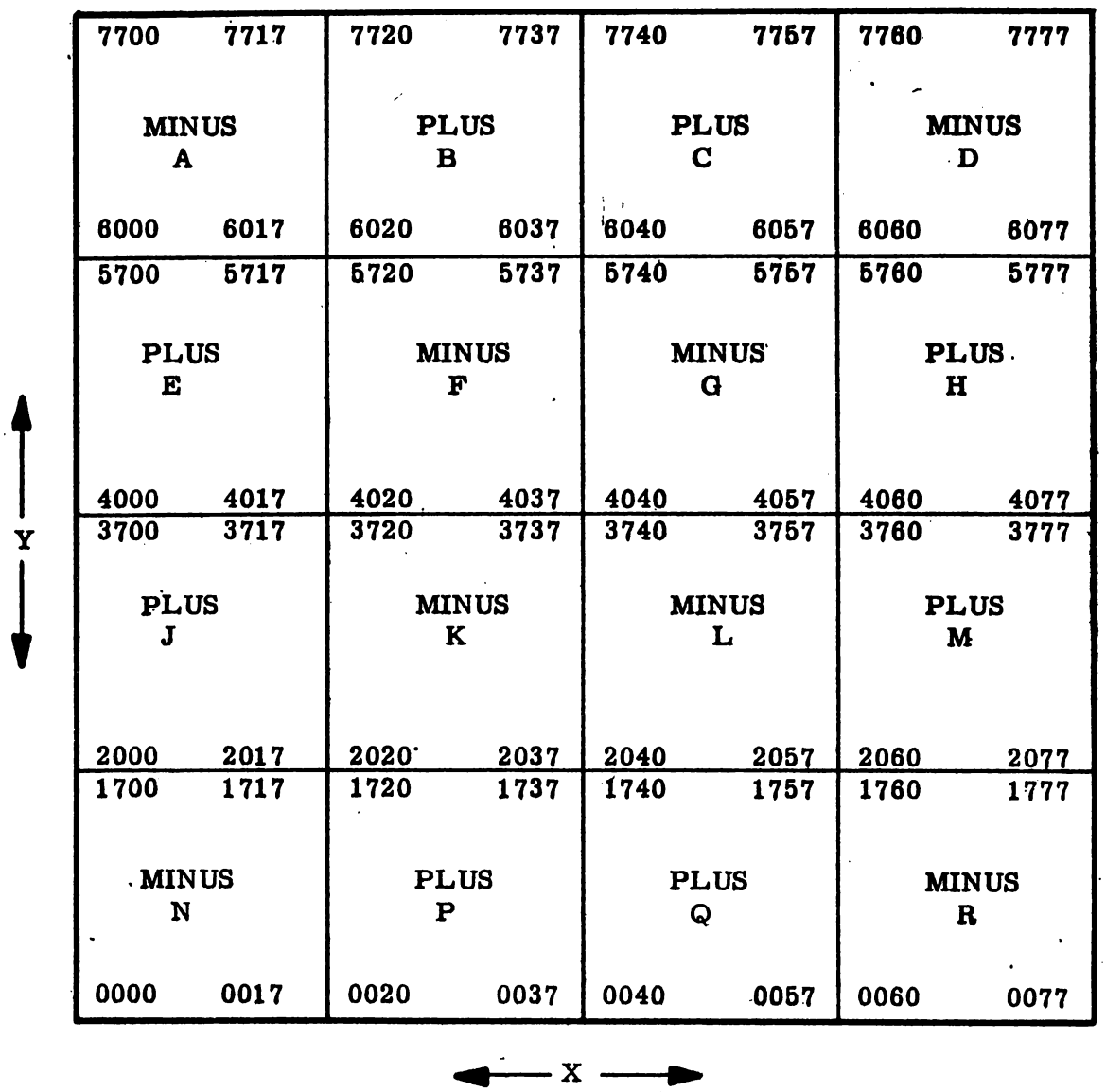
2. One problem associated with marginal checking on a production basis is that it takes a large amout of time because of the number of lines to be checked and the length of some of the tests.

3. During initial test evaluation, it is helpful to keep all records of failure margins taken for all routines as each is run with excursions on all marginal check lines. This data is important for several reasons:

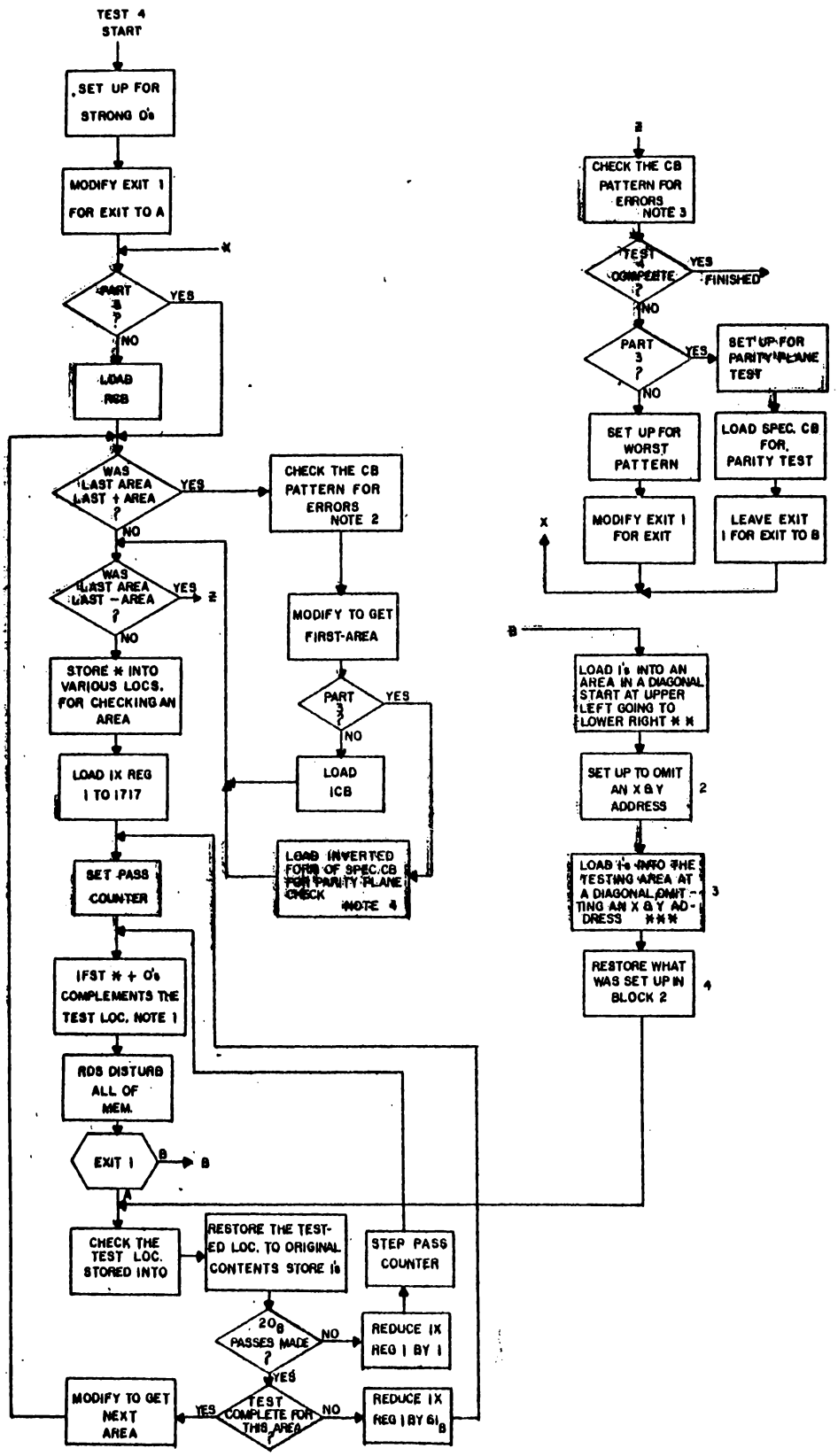
a. The data indicates the relative effectiveness of each test for finding various failures under margins. When the time arrives for writing a finished program which runs selected routines for each margin, this failure data is essential to making a selection of routines which will be effective and yet not take excessive time.

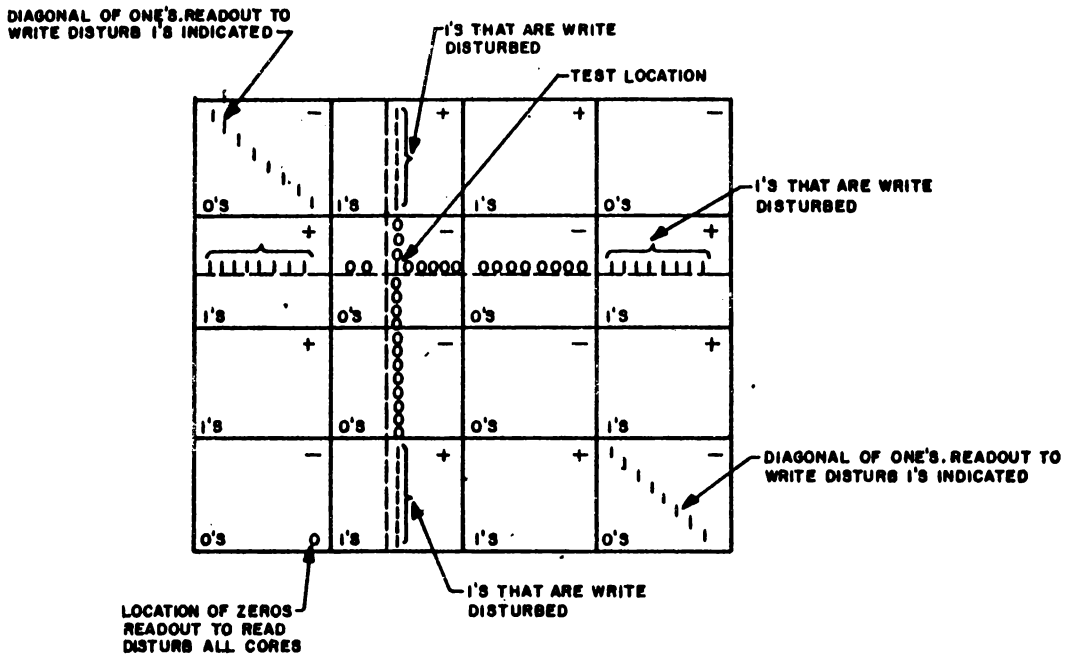
b. The data shows the overall relationships of circuits throughout memory. It is not always possible to predict the effects of one circuit upon another. For instance, two different tests run with margins on a given circuit may, at their respective failure excursions, indicate two entirely different types of memory failures, which are caused by the same circuit. Knowledge of these circuit relations is vital to the complete understanding of various circuit limitations in memory and indicates what circuit and logic improvements might be needed.

c. The failure data indicates the effects of various ways of compensating in the memory. This compenstaion involves the selection of an optimum operating point for the

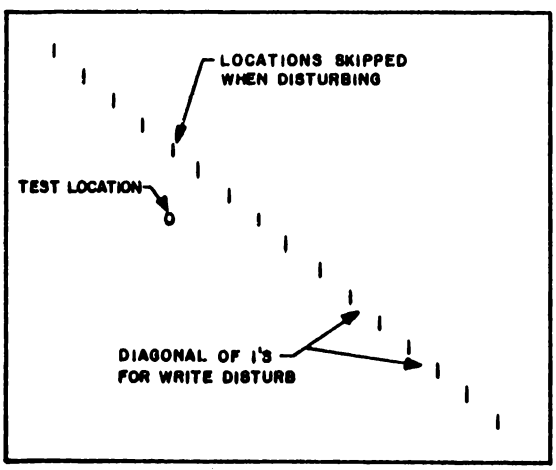


Octal addresses of checkerboard pattern in 64^2 memory
(Minus and Plus indicate core polarity)


TEST 4 START
SET UP FOR STRONG 0's
MODIFY EXIT 1 FOR EXIT TO A
PART 3 ?
YES
NO
LOAD RGB
WAS LAST AREA LAST + AREA ?
YES
NO
CHECK THE CB PATTERN FOR ERRORS NOTE 2
WAS LAST AREA LAST - AREA ?
YES
NO
MODIFY TO GET FIRST-AREA
PART 3 ?
YES
NO
LOAD ICB
STORE * INTO VARIOUS LOCS. FOR CHECKING AN AREA
LOAD IX REG 1 TO 1717
LOAD INVERTED FORM OF SPEC.CB FOR PARITY PLANE CHECK NOTE 4
SET PASS COUNTER
IFST * + 0's COMPLEMENTS THE TEST LOC. NOTE 1
RDS DISTURB ALL OF MEM.
EXIT 1
B
CHECK THE TEST LOC. STORED INTO
RESTORE THE TESTED LOC. TO ORIGINAL CONTENTS STORE 1s
STEP PASS COUNTER
20_8 PASSES MADE ?
NO
YES
REDUCE IX REG 1 BY 1
MODIFY TO GET NEXT AREA
YES
TEST COMPLETE FOR THIS AREA ?
NO
REDUCE IX REG 1 BY 61_8
A
CHECK THE CB PATTERN FOR ERRORS NOTE 3
TEST COMPLETE ?
YES
FINISHED
NO
PART 3 ?
YES
SET UP FOR PARITY PLANE TEST
NO
SET UP FOR WORST PATTERN
LOAD SPEC. CB FOR PARITY TEST
MODIFY EXIT 1 FOR EXIT
LEAVE EXIT 1 FOR EXIT TO B
X
B
LOAD 1's INTO AN AREA IN A DIAGONAL START AT UPPER LEFT GOING TO LOWER RIGHT * *
SET UP TO OMIT AN X & Y ADDRESS
2
LOAD 1's INTO THE TESTING AREA AT A DIAGONAL OMITTING AN X & Y ADDRESS * * *
3
RESTORE WHAT WAS SET UP IN BLOCK 2
4



TYPICAL WORST-PATTERN TEST SET-UP



AREA OF CHECKERBOARD PATTERN CONTAINING ZEROS TO BE TESTED

* These numbers run in sequence as follows:

Block	Plus Areas	Neg. Areas	Block		PASS	Test Area		PASS	Test Area
J	212000	210000	N	**	first	H	***	first	J
M	212060	210060	R		second	E		Second	M
E	214000	216000	A		third	M		third	E
H	214060	216060	D		fourth .	J		fourth	H
P	210020	212020	K		fifth	C		fifth	P
Q	210040	212040	L		sixth	B		sixth	Q
B	216020	214020	F		seventh	Q		seventh	B
C	216040	214040	G		eighth	P		eighth	C

Note 1 on the parity plane check 1.77777, 1.77776 will be stored into the tested loc. to compliment the parity bit.

Note 2 will check for RCB except on parity plane check. An error routine will be branched to when an error is found.

Note 3 will check for ICB except on parity plane check.

Note 4 The first special CB loaded is:

a. Positive cores contain -0

1.) This will cause the parity plane positive cores to contain ONES.

b. Negative cores contain 1.77777, 1.77776

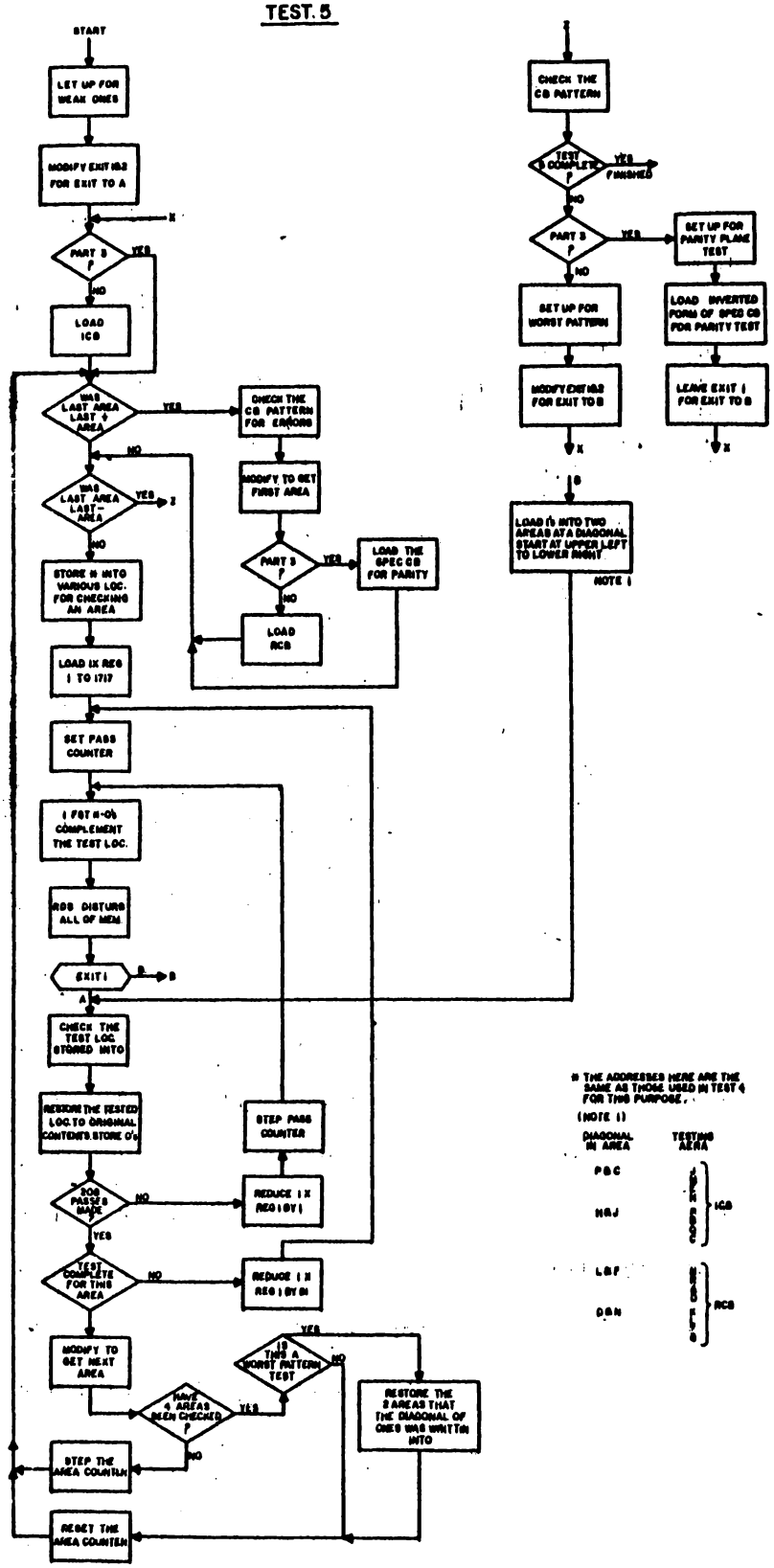
1.) This will cause the parity plane negative cores to contain ZEROS.

c. This effectively puts a RCB in the parity plane.

When the inverted form of the special CB is loaded:

a. The parity plane will have an ICB pattern in it.

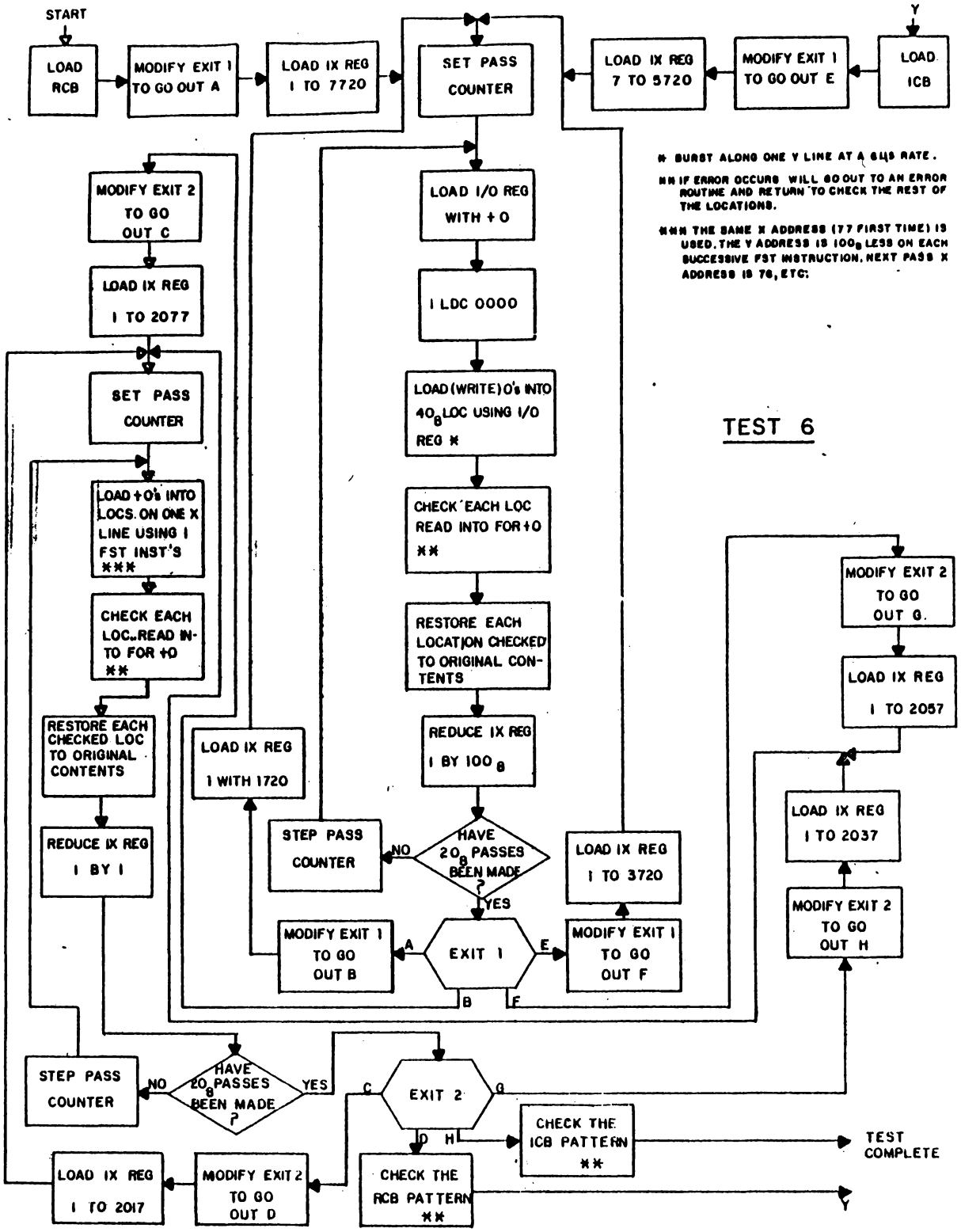
TEST 5



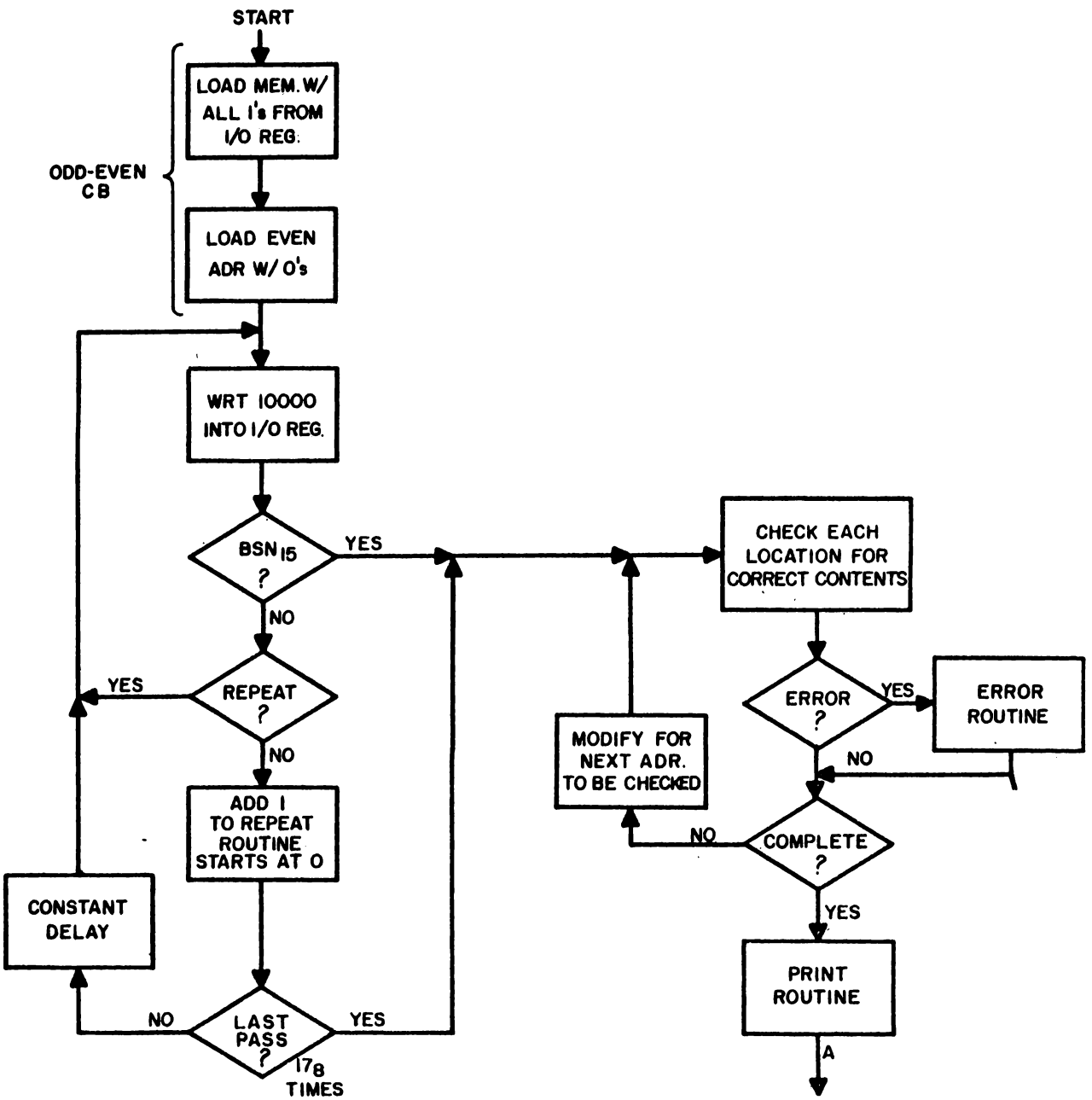
* THE ADDRESSES HERE ARE THE SAME AS THOSE USED IN TEST 4 FOR THIS PURPOSE.

(NOTE 1)

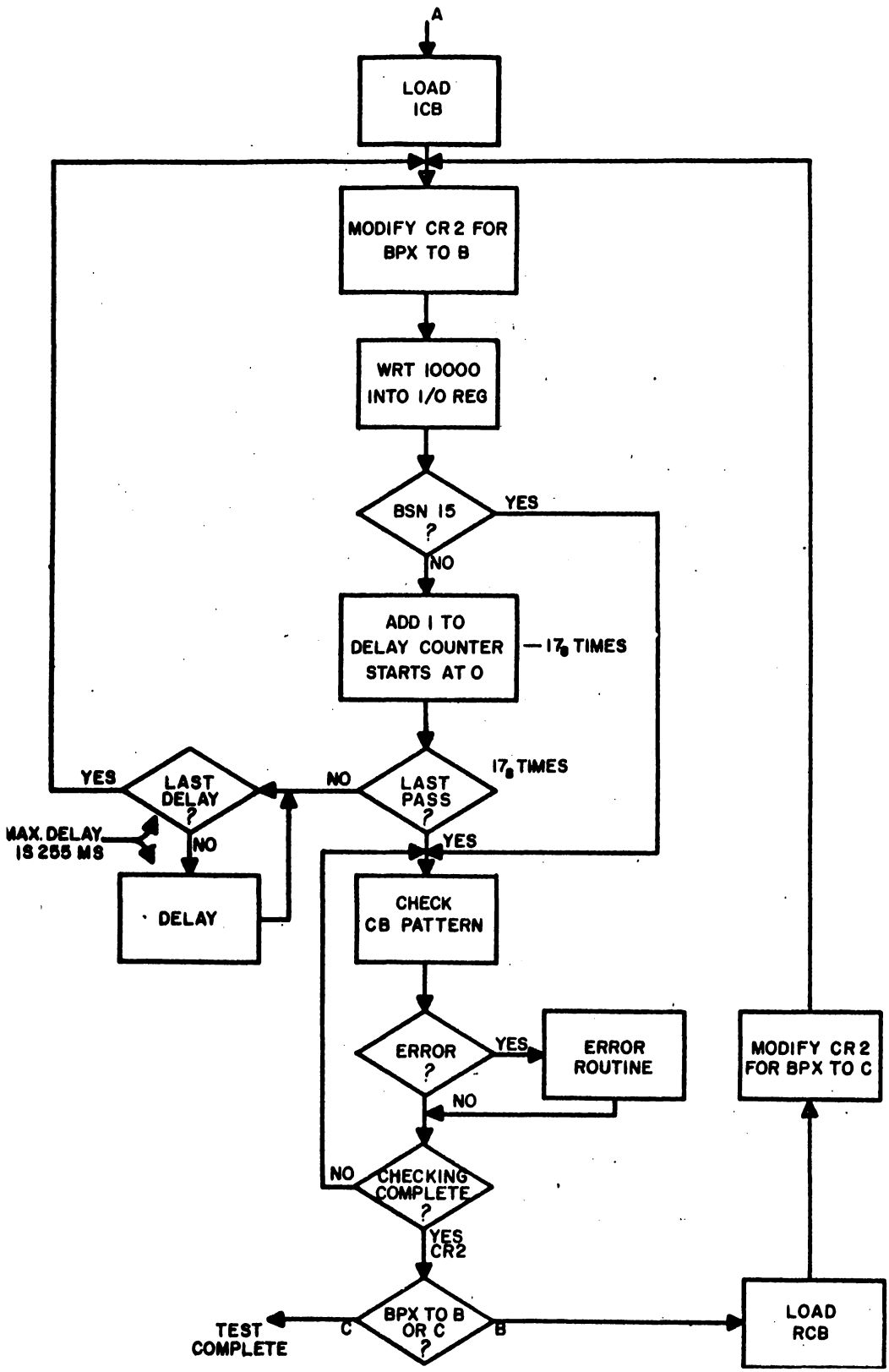
DIAGONAL IN AREA	TESTING AREA
P&C	ICB
N&J	ICB
L&F	RCB
D&N	RCB

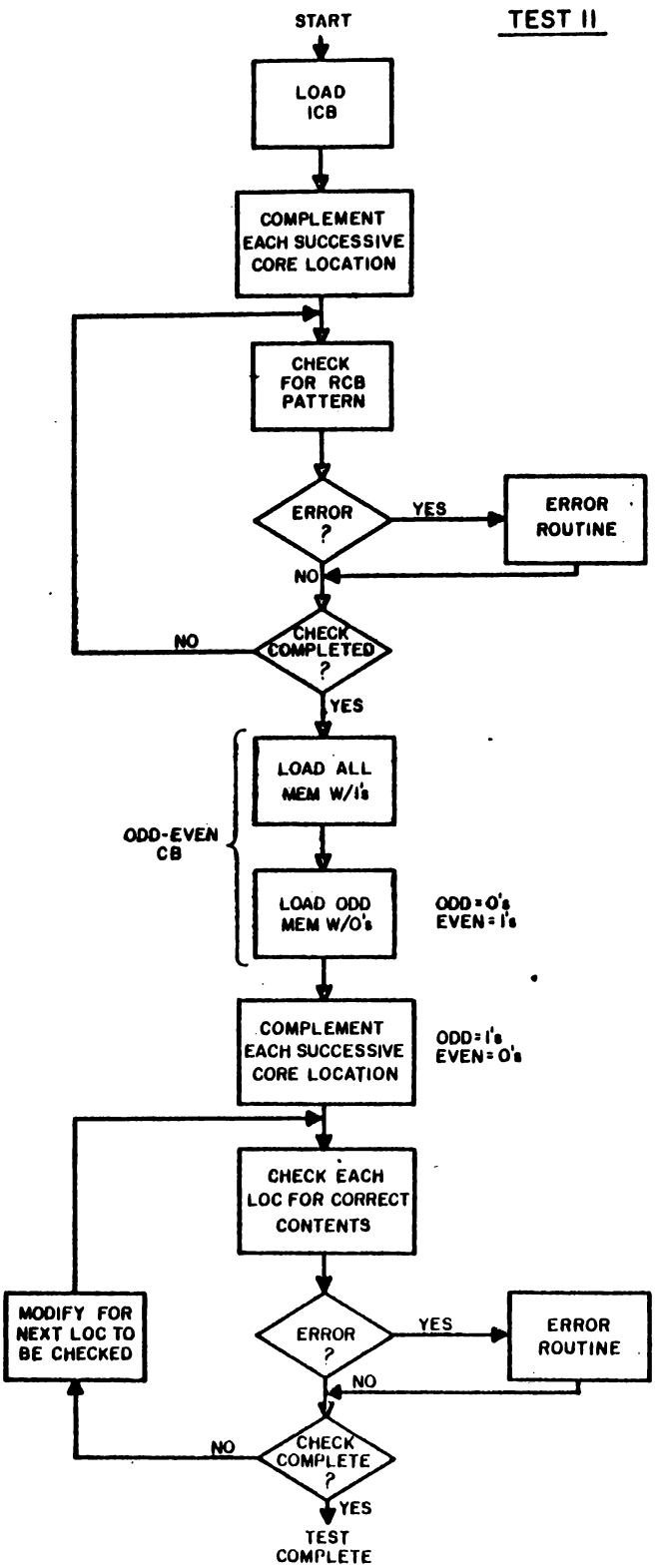

START
LOAD RCB
MODIFY EXIT 1 TO GO OUT A
LOAD IX REG 1 TO 7720
SET PASS COUNTER
LOAD IX REG 7 TO 5720
MODIFY EXIT 1 TO GO OUT E
LOAD ICB
Y
* BURST ALONG ONE Y LINE AT A 6µS RATE.
** IF ERROR OCCURS WILL GO OUT TO AN ERROR ROUTINE AND RETURN TO CHECK THE REST OF THE LOCATIONS.
*** THE SAME X ADDRESS (77 FIRST TIME) IS USED. THE Y ADDRESS IS 100₈ LESS ON EACH SUCCESSIVE FST INSTRUCTION. NEXT PASS X ADDRESS IS 76, ETC.
TEST 6
MODIFY EXIT 2 TO GO OUT C
LOAD IX REG 1 TO 2077
SET PASS COUNTER
LOAD +0's INTO LOCS. ON ONE X LINE USING 1 FST INST'S ***
CHECK EACH LOC. READ INTO FOR +0 **
RESTORE EACH CHECKED LOC TO ORIGINAL CONTENTS
REDUCE IX REG 1 BY 1
LOAD IX REG 1 WITH 1720
LOAD I/O REG WITH +0
1 LDC 0000
LOAD (WRITE) 0's INTO 40₈ LOC USING I/O REG *
CHECK EACH LOC READ INTO FOR +0 **
RESTORE EACH LOCATION CHECKED TO ORIGINAL CONTENTS
REDUCE IX REG 1 BY 100₈
STEP PASS COUNTER
NO
HAVE 20₈ PASSES BEEN MADE ?
YES
LOAD IX REG 1 TO 3720
MODIFY EXIT 1 TO GO OUT B
A
EXIT 1
E
MODIFY EXIT 1 TO GO OUT F
B
F
MODIFY EXIT 2 TO GO OUT G.
LOAD IX REG 1 TO 2057
LOAD IX REG 1 TO 2037
MODIFY EXIT 2 TO GO OUT H
STEP PASS COUNTER
NO
HAVE 20₈ PASSES BEEN MADE ?
YES
C
EXIT 2
G
D
H
CHECK THE ICB PATTERN **
TEST COMPLETE
LOAD IX REG 1 TO 2017
MODIFY EXIT 2 TO GO OUT D
CHECK THE RCB PATTERN **
Y

TEST 10
PART 1

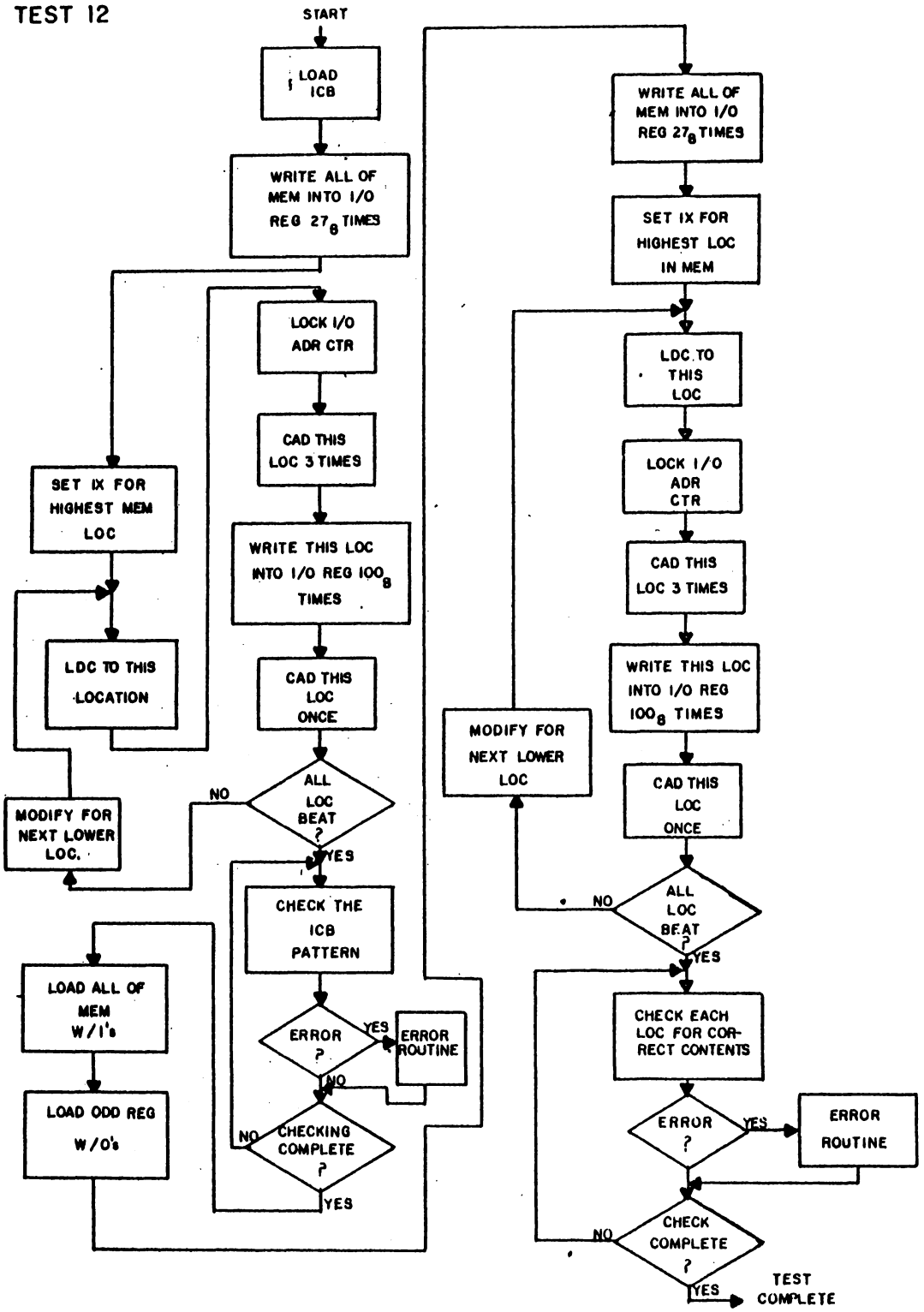


TEST 10
PART 2

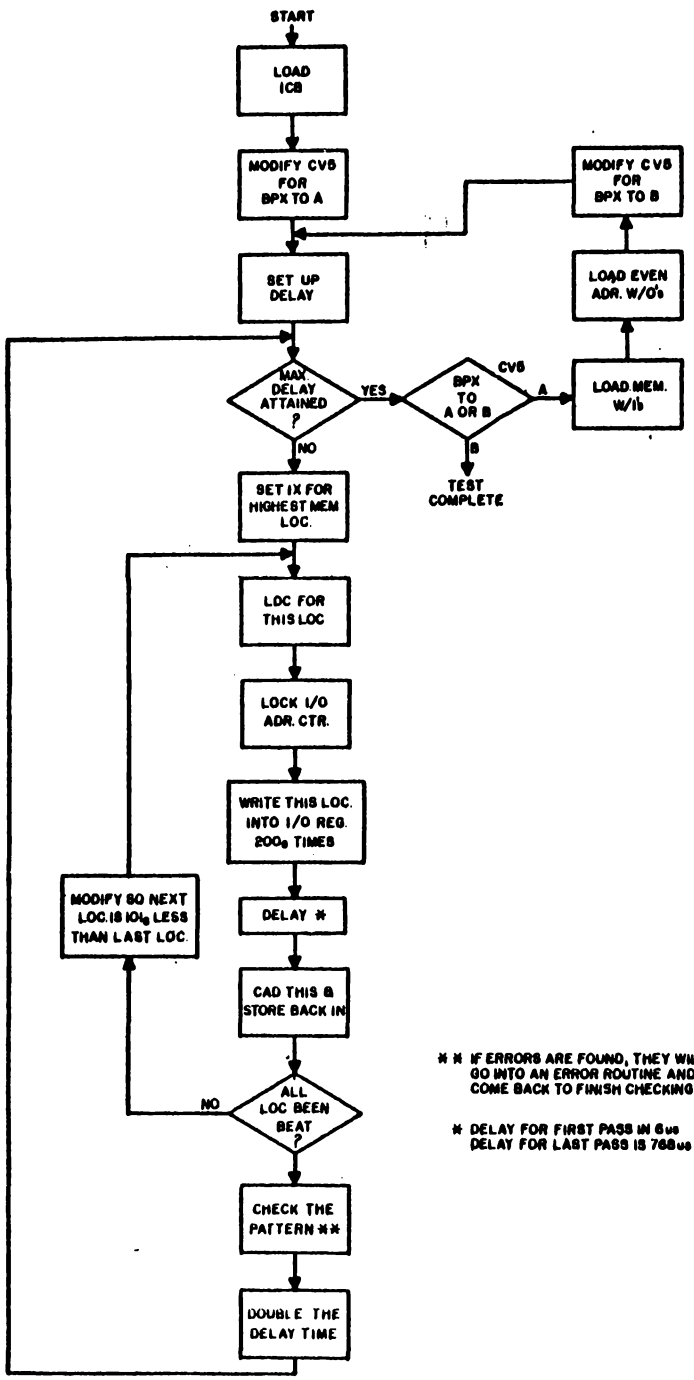



TEST II
START
LOAD ICB
COMPLEMENT EACH SUCCESSIVE CORE LOCATION
CHECK FOR RCB PATTERN
ERROR ?
YES
ERROR ROUTINE
NO
CHECK COMPLETED ?
NO
YES
ODD-EVEN CB
LOAD ALL MEM W/1's
LOAD ODD MEM W/0's
ODD=0's EVEN=1's
COMPLEMENT EACH SUCCESSIVE CORE LOCATION
ODD=1's EVEN=0's
CHECK EACH LOC FOR CORRECT CONTENTS
MODIFY FOR NEXT LOC TO BE CHECKED
ERROR ?
YES
ERROR ROUTINE
NO
CHECK COMPLETE ?
NO
YES
TEST COMPLETE

TEST 12


START
LOAD ICB
WRITE ALL OF MEM INTO I/O REG 27_8 TIMES
LOCK I/O ADR CTR
CAD THIS LOC 3 TIMES
WRITE THIS LOC INTO I/O REG 100_8 TIMES
CAD THIS LOC ONCE
ALL LOC BEAT ?
NO
YES
SET IX FOR HIGHEST MEM LOC
LOC TO THIS LOCATION
MODIFY FOR NEXT LOWER LOC.
CHECK THE ICB PATTERN
ERROR ?
YES
ERROR ROUTINE
NO
CHECKING COMPLETE ?
NO
YES
LOAD ALL OF MEM W/1's
LOAD ODD REG W/0's
WRITE ALL OF MEM INTO I/O REG 27_8 TIMES
SET IX FOR HIGHEST LOC IN MEM
LOC TO THIS LOC
LOCK I/O ADR CTR
CAD THIS LOC 3 TIMES
WRITE THIS LOC INTO I/O REG 100_8 TIMES
CAD THIS LOC ONCE
ALL LOC BEAT ?
NO
YES
MODIFY FOR NEXT LOWER LOC
CHECK EACH LOC FOR CORRECT CONTENTS
ERROR ?
YES
ERROR ROUTINE
CHECK COMPLETE ?
NO
YES
TEST COMPLETE

TEST 13



** IF ERRORS ARE FOUND, THEY WILL GO INTO AN ERROR ROUTINE AND COME BACK TO FINISH CHECKING.

* DELAY FOR FIRST PASS IS 6 us
DELAY FOR LAST PASS IS 768 us

various parameters which affect memory operation. This is, tolerances on memory operations are so close that certain circuits must be adjusted individually for the memory in which they operate. Another reason for such compensation is that the several adjustments work against each other so that an adjustment that aids one parameter hinders another.

4. It is desirable to perform routine marginal check in as short a time as possible. Several ways of decreasing this time are listed below:

   a. After performing the weakest portion of a test, check the pattern only if a memory failure has occurred.

   b. Keep record of the past failure excursion, and begin checking at the lower excursion.

   c. For each MC line, run only those routines which are critical, as described above.

   d. When several routines are to be run, schedule the longest routines to be run last.

   e. When a routine fails, do not run previously successful routines at lower excursions.

   f. Construct tests such that the failing location can be individually tested first.

Q. Summary Questions

1. A program that is designed to test the equipment as stringently and frequently as possible is called a _____program.

2. A program that is designed to localize a failing component is called a _____program.

3. A program that is designed to localize deteriorating components is called a _____ program.

4. A faster method of error indication than printouts when tuning is _____ _____.

5. When a memory is under test, the test program should be contained in the_____memory.

6. An inoperative DPD could be detected with the _____ discrimination test.

7. An addressing error would not be detected with _____ discrimination test.

8. The checkerboard pattern is used to produce _____ one's and _____ zero's.

9. Inhibit noise when storing a zero may cause a _____ to be read in error during the next memory cycle.

10. Half select noises may cause _____ zeros to be read as _____.

11. Noise between planes is refered to as _____.

12. When a core switches completely before sample time it is refered to as an _____ _____ core.

13. One advantage of Data Reduction is that the _____ can compile data faster than an _____ device can print it.

14. One major disadvantage of Marginal Checking is the amount of _____ required to run a marginal checking program.

15. Early peaking core can be detected in most cases by _____ the drive current.

III. Little Memory Program

NOTE: The latest Little Memory Program specification should be obtained and the following items studied.

A. General Information

1. Function
2. General Control Information
3. Manual Controls
4. Program Initiation and Control

TROUBLE #1

TEST NO-01

TOTAL ERRORS 10000

DIGIT PLANE ERRORS

	PICK	DROP		PICK	DROP
LS	0	0	RS	0	0
1	0	0	1	0	0
2	0	0	2	0	0
3	0	0	3	0	0
4	0	0	4	0	0
5	0	0	5	0	0
6	0	0	6	0	0
7	0	0	7	0	0
8	0	0	8	0	0
9	0	0	9	0	0
10	0	0	10	0	0
11	0	0	11	0	0
12	0	0	12	0	10000
13	0	0	13	0	0
14	0	0	14	0	0
15	0	0	15	0	0

MGGS

XODD XEVN YODD YEVN

4000 4000 4000 4000

DRIVER PANELS

	A	B	C	D
X	2000	2000	2000	2000
Y	2000	2000	2000	2000

X AND Y LINE ERRORS

	XL	ERRS	XL	ERRS	YL	ERRS	YL	ERRS
	0	100	40	100	0	100	40	100
	1	100	41	100	1	100	41	100
	2	100	42	100	2	100	42	100
	3	100	43	100	3	100	43	100
	4	100	44	100	4	100	44	100
	5	100	45	100	5	100	45	100
	6	100	46	100	6	100	46	100
	7	100	47	100	7	100	47	100
	10	100	50	100	10	100	50	100
	11	100	51	100	11	100	51	100
	12	100	52	100	12	100	52	100
	13	100	53	100	13	100	53	100
	14	100	54	100	14	100	54	100
	15	100	55	100	15	100	55	100
	16	100	56	100	16	100	56	100
	17	100	57	100	17	100	57	100
	20	100	60	100	20	100	60	100
	21	100	61	100	21	100	61	100
	22	100	62	100	22	100	62	100
	23	100	63	100	23	100	63	100
	24	100	64	100	24	100	64	100
	25	100	65	100	25	100	65	100
	26	100	66	100	26	100	66	100
	27	100	67	100	27	100	67	100
	30	100	70	100	30	100	70	100
	31	100	71	100	31	100	71	100
	32	100	72	100	32	100	72	100
	33	100	73	100	33	100	73	100
	34	100	74	100	34	100	74	100
	35	100	75	100	35	100	75	100
	36	100	76	100	36	100	76	100
	37	100	77	100	37	100	77	100

TEST NO-02
SUCCESS

TEST NO-03
(OVER)

TROUBLE #1

TEST NO-03

TOTAL ERRORS 04000

DIGIT PLANE ERRORS					X AND Y LINE ERRORS					
	PICK	DROP		PICK	DROP	XL ERRS	XL ERRS	YL ERRS	YL ERRS	
LS	0	0	RS	0	0	0	0 40	0 0	40 40	40
1	0	0	1	0	0	1	0 41	0 1	40 41	40
2	0	0	2	0	0	2	0 42	0 2	40 42	40
3	0	0	3	0	0	3	0 43	0 3	40 43	40
4	0	0	4	0	0	4	0 44	0 4	40 44	40
5	0	0	5	0	0	5	0 45	0 5	40 45	40
6	0	0	6	0	0	6	0 46	0 6	40 46	40
7	0	0	7	0	0	7	0 47	0 7	40 47	40
8	0	0	8	0	0	10	100 50	100 10	40 50	40
9	0	0	9	0	0	11	100 51	100 11	40 51	40
10	0	0	10	0	0	12	100 52	100 12	40 52	40
11	0	0	11	0	0	13	100 53	100 13	40 53	40
12	0	0	12	0	4000	14	100 54	100 14	40 54	40
13	0	0	13	0	0	15	100 55	100 15	40 55	40
14	0	0	14	0	0	16	100 56	100 16	40 56	40
15	0	0	15	0	0	17	100 57	100 17	40 57	40
						20	0 60	0 20	40 60	40
MGGS						21	0 61	0 21	40 61	40
XODD XEVN YODD YEVN						22	0 62	0 22	40 62	40
2000 2000 2000 2000						23	0 63	0 23	40 63	40
DRIVER PANELS						24	0 64	0 24	40 64	40
	A	B	C	D		25	0 65	0 25	40 65	40
X	1000	1000	1000	1000		26	0 66	0 26	40 66	40
Y	1000	1000	1000	1000		27	0 67	0 27	40 67	40
						30	100 70	100 30	40 70	40
						31	100 71	100 31	40 71	40
						32	100 72	100 32	40 72	40
						33	100 73	100 33	40 73	40
						34	100 74	100 34	40 74	40
						35	100 75	100 35	40 75	40
						36	100 76	100 36	40 76	40
						37	100 77	100 37	40 77	40

TEST NO-01

LOC	CONTENTS	
7777	1 111 111 111 111 111	1 111 111 111 110 111
7776	1 111 111 111 111 111	1 111 111 111 110 111
7775	1 111 111 111 111 111	1 111 111 111 110 111
7774	1 111 111 111 111 111	1 111 111 111 110 111
7773	1 111 111 111 111 111	1 111 111 111 110 111
7772	1 111 111 111 111 111	1 111 111 111 110 111
7771	1 111 111 111 111 111	1 111 111 111 110 111
7770	1 111 111 111 111 111	1 111 111 111 110 111
7767	1 111 111 111 111 111	1 111 111 111 110 111
7766	1 111 111 111 111 111	1 111 111 111 110 111
7765	1 111 111 111 111 111	1 111 111 111 110 111
7764	1 111 111 111 111 111	1 111 111 111 110 111

(ETC.)

Trouble # 1 SA for R12 Defective

TROUBLE #2

TEST NO-01
TOTAL ERRORS 00100
DIGIT PLANE ERRORS

	PICK	DROP		PICK	DROP
LS	0	100	RS	0	100
1	0	100	1	0	100
2	0	100	2	0	100
3	0	100	3	0	100
4	0	100	4	0	100
5	0	100	5	0	100
6	0	100	6	0	100
7	0	100	7	0	100
8	0	100	8	0	100
9	0	100	9	0	100
10	0	100	10	0	100
11	0	100	11	0	100
12	0	100	12	0	100
13	0	100	13	0	100
14	0	100	14	0	100
15	0	100	15	0	100

MGGS

XODD	XEVN	YODD	YEVN
40	40	0	100

DRIVER PANELS

	A	B	C	D
X	20	20	20	20
Y	0	0	0	100

X AND Y LINE ERRORS

	XL ERRS		YL ERRS	
0	1	40	0	40	0
1	1	41	1	0	0
2	1	42	1	2	0
3	1	43	1	3	0
4	1	44	1	4	0
5	1	45	1	5	0
6	1	46	1	6	0
7	1	47	1	7	0
10	1	50	1	10	0
11	1	51	1	11	0
12	1	52	1	12	0
13	1	53	1	13	0
14	1	54	1	14	0
15	1	55	1	15	0
16	1	56	1	16	0
17	1	57	1	17	0
20	1	60	1	20	0
21	1	61	1	21	0
22	1	62	1	22	0
23	1	63	1	23	0
24	1	64	1	24	0
25	1	65	1	25	0
26	1	66	1	26	0
27	1	67	1	27	0
30	1	70	1	30	0
31	1	71	1	31	0
32	1	72	1	32	0
33	1	73	1	33	0
34	1	74	1	34	0
35	1	75	1	35	0
36	1	76	1	36	0
37	1	77	1	37	0

TEST NO-02
SUCCESS

TEST NO-03
(OVER)

TROUBLE #2

TEST NO-03

TOTAL ERRORS 00100

DIGIT PLANE ERRORS

LS	PICK	DROP	RS	PICK	DROP
1	0	0	1	0	0
2	0	0	2	0	0
3	0	0	3	0	0
4	0	100	4	0	100
5	0	100	5	0	100
6	0	0	6	0	0
7	0	100	7	0	100
8	0	100	8	0	100
9	0	0	9	0	0
10	0	40	10	0	40
11	0	40	11	0	40
12	0	40	12	0	40
13	0	40	13	0	40
14	0	40	14	0	40
15	0	40	15	0	40

MGGS

XODD	XEVN	YODD	YEVN
40	40	0	100

DRIVER PANELS

	A	B	C	D
X	20	20	20	20
Y	0	0	0	100

X AND Y LINE ERRORS

	XL ERRS		XL ERRS		YL ERRS		YL ERRS	
0	1	40	1	0	0	40	0
1	1	41	1	1	0	41	0
2	1	42	1	2	0	42	0
3	1	43	1	3	0	43	0
4	1	44	1	4	0	44	0
5	1	45	1	5	0	45	0
6	1	46	1	6	0	46	0
7	1	47	1	7	0	47	0
10	1	50	1	10	0	50	0
11	1	51	1	11	0	51	0
12	1	52	1	12	0	52	0
13	1	53	1	13	0	53	0
14	1	54	1	14	0	54	0
15	1	55	1	15	0	55	0
16	1	56	1	16	0	56	0
17	1	57	1	17	0	57	0
20	1	60	1	20	0	60	0
21	1	61	1	21	0	61	0
22	1	62	1	22	0	62	0
23	1	63	1	23	0	63	0
24	1	64	1	24	0	64	0
25	1	65	1	25	0	65	0
26	1	66	1	26	0	66	100
27	1	67	1	27	0	67	0
30	1	70	1	30	0	70	0
31	1	71	1	31	0	71	0
32	1	72	1	32	0	72	0
33	1	73	1	33	0	73	0
34	1	74	1	34	0	74	0
35	1	75	1	35	0	75	0
36	1	76	1	36	0	76	0
37	1	77	1	37	0	77	0

Trouble # 2 CMD or MOA for "Y"66 Defective

TROUBLE #3

TEST NO-01
SUCCESS

TEST NO-02

TOTAL ERRORS 10000

DIGIT PLANE ERRORS

PICK	DROP		PICK	DROP
LS 10000	0	RS	10000	0
1 10000	0	1	10000	0
2 10000	0	2	10000	0
3 10000	0	3	10000	0
4 10000	0	4	10000	0
5 10000	0	5	10000	0
6 10000	0	6	10000	0
7 10000	0	7	10000	0
8 10000	0	8	10000	0
9 10000	0	9	10000	0
10 10000	0	10	10000	0
11 10000	0	11	10000	0
12 10000	0	12	10000	0
13 10000	0	13	10000	0
14 10000	0	14	10000	0
15 10000	0	15	10000	0

MGGS

XODD	XEVN	YODD	YEVN
4000	4000	4000	4000

DRIVER PANELS

	A	B	C	D
X	2000	2000	2000	2000
Y	2000	2000	2000	2000

X AND Y LINE ERRORS

	XL ERRS		XL ERRS		YL ERRS		YL ERRS	
0	0	100	40	100	0	100	40	100
0	1	100	41	100	1	100	41	100
0	2	100	42	100	2	100	42	100
0	3	100	43	100	3	100	43	100
0	4	100	44	100	4	100	44	100
0	5	100	45	100	5	100	45	100
0	6	100	46	100	6	100	46	100
0	7	100	47	100	7	100	47	100
0	10	100	50	100	10	100	50	100
0	11	100	51	100	11	100	51	100
0	12	100	52	100	12	100	52	100
0	13	100	53	100	13	100	53	100
0	14	100	54	100	14	100	54	100
0	15	100	55	100	15	100	55	100
0	16	100	56	100	16	100	56	100
0	17	100	57	100	17	100	57	100
	20	100	60	100	20	100	60	100
	21	100	61	100	21	100	61	100
	22	100	62	100	22	100	62	100
	23	100	63	100	23	100	63	100
	24	100	64	100	24	100	64	100
	25	100	65	100	25	100	65	100
	26	100	66	100	26	100	66	100
	27	100	67	100	27	100	67	100
	30	100	70	100	30	100	70	100
	31	100	71	100	31	100	71	100
	32	100	72	100	32	100	72	100
	33	100	73	100	33	100	73	100
	34	100	74	100	34	100	74	100
	35	100	75	100	35	100	75	100
	36	100	76	100	36	100	76	100
	37	100	77	100	37	100	77	100

TEST NO-03
(OVER)

1387

TROUBLE #3

TEST NO-03

TOTAL ERRORS 10000

DIGIT PLANE ERRORS

	PICK	DROP		PICK	DROP
LS	10000	0	RS	10000	0
1	10000	0	1	10000	0
2	10000	0	2	10000	0
3	10000	0	3	10000	0
4	4000	0	4	4000	0
5	4000	0	5	4000	0
6	4000	0	6	4000	0
7	4000	0	7	4000	0
8	4000	0	8	4000	0
9	4000	0	9	4000	0
10	4000	0	10	4000	0
11	4000	0	11	4000	0
12	4000	0	12	4000	0
13	4000	0	13	4000	0
14	4000	0	14	4000	0
15	4000	0	15	4000	0

MGGS

XODD	XEVN	YODD	YEVN
4000	4000	4000	4000

DRIVER PANELS

	A	B	C	D
X	2000	2000	2000	2000
Y	2000	2000	2000	2000

X AND Y LINE ERRORS

	XL	ERRS	XL	ERRS	YL	ERRS	YL	ERRS
0	0	100	40	100	0	100	40	100
	1	100	41	100	1	100	41	100
	2	100	42	100	2	100	42	100
	3	100	43	100	3	100	43	100
	4	100	44	100	4	100	44	100
	5	100	45	100	5	100	45	100
	6	100	46	100	6	100	46	100
	7	100	47	100	7	100	47	100
	10	100	50	100	10	100	50	100
	11	100	51	100	11	100	51	100
	12	100	52	100	12	100	52	100
	13	100	53	100	13	100	53	100
	14	100	54	100	14	100	54	100
	15	100	55	100	15	100	55	100
	16	100	56	100	16	100	56	100
	17	100	57	100	17	100	57	100
	20	100	60	100	20	100	60	100
	21	100	61	100	21	100	61	100
	22	100	62	100	22	100	62	100
	23	100	63	100	23	100	63	100
	24	100	64	100	24	100	64	100
	25	100	65	100	25	100	65	100
	26	100	66	100	26	100	66	100
	27	100	67	100	27	100	67	100
	30	100	70	100	30	100	70	100
	31	100	71	100	31	100	71	100
	32	100	72	100	32	100	72	100
	33	100	73	100	33	100	73	100
	34	100	74	100	34	100	74	100
	35	100	75	100	35	100	75	100
	36	100	76	100	36	100	76	100
	37	100	77	100	37	100	77	100

Trouble # 3 SET INHIBIT CLOCK output missing

TROUBLE #4

TEST NO-01
SUCCESS
TEST NO-02
SUCCESS

TEST NO-03
TOTAL ERRORS 04000

DIGIT PLANE ERRORS

	PICK	DROP		PICK	DROP
LS	0	0	RS	0	0
1	0	0	1	0	0
2	0	0	2	0	0
3	0	0	3	0	0
4	0	0	4	0	0
5	0	0	5	0	0
6	0	0	6	0	0
7	0	0	7	0	0
8	0	0	8	0	0
9	0	0	9	0	0
10	0	0	10	0	0
11	0	0	11	0	0
12	0	0	12	0	0
13	0	0	13	0	0
14	0	0	14	0	0
15	0	4000	15	0	4000

MGGS

XODD	XEVN	YODD	YEVN
4000	0	2000	2000

DRIVER PANELS

	A	B	C	D
X	1000	1000	1000	1000
Y	1000	1000	1000	1000

X AND Y LINE ERRORS

	XL ERRS	XL ERRS	YL ERRS	YL ERRS
0	0	40	0	40
1	100	41	100	40
2	0	42	0	40
3	100	43	100	40
4	0	44	0	40
5	100	45	100	40
6	0	46	0	40
7	100	47	100	40
10	0	50	0	40
11	100	51	100	40
12	0	52	0	40
13	100	53	100	40
14	0	54	0	40
15	100	55	100	40
16	0	56	0	40
17	100	57	100	40
20	0	60	0	40
21	100	61	100	40
22	0	62	0	40
23	100	63	100	40
24	0	64	0	40
25	100	65	100	40
26	0	66	0	40
27	100	67	100	40
30	0	70	0	40
31	100	71	100	40
32	0	72	0	40
33	100	73	100	40
34	0	74	0	40
35	100	75	100	40
36	0	76	0	40
37	100	77	100	40

Trouble # 4 R15 MAR FF cannot be set

TEST NO-01
SUCCESS

TEST NO-02
TOTAL ERRORS 10000
DIGIT PLANE ERRORS

	PICK	DROP		PICK	DROP
LS	0	0	RS	0	0
1	0	0	1	0	0
2	0	0	2	0	0
3	0	0	3	0	0
4	0	0	4	0	0
5	0	0	5	0	0
6	0	0	6	0	0
7	0	0	7	0	0
8	0	0	8	0	0
9	0	0	9	0	0
10	0	0	10	0	0
11	0	0	11	0	0
12	0	0	12	10000	0
13	0	0	13	0	0
14	0	0	14	0	0
15	0	0	15	0	0

MGGS

XODD	XEVN	YODD	YEVN
4000	4000	4000	4000

DRIVER PANELS

	A	B	C	D
X	2000	2000	2000	2000
Y	2000	2000	2000	2000

X AND Y LINE ERRORS

	XL	ERRS	XL	ERRS	YL	ERRS	YL	ERRS
0	0	100	40	100	0	100	40	100
1	1	100	41	100	1	100	41	100
2	2	100	42	100	2	100	42	100
3	3	100	43	100	3	100	43	100
4	4	100	44	100	4	100	44	100
5	5	100	45	100	5	100	45	100
6	6	100	46	100	6	100	46	100
7	7	100	47	100	7	100	47	100
8	10	100	50	100	10	100	50	100
9	11	100	51	100	11	100	51	100
10	12	100	52	100	12	100	52	100
11	13	100	53	100	13	100	53	100
12	14	100	54	100	14	100	54	100
13	15	100	55	100	15	100	55	100
14	16	100	56	100	16	100	56	100
15	17	100	57	100	17	100	57	100
	20	100	60	100	20	100	60	100
	21	100	61	100	21	100	61	100
	22	100	62	100	22	100	62	100
	23	100	63	100	23	100	63	100
	24	100	64	100	24	100	64	100
	25	100	65	100	25	100	65	100
	26	100	66	100	26	100	66	100
	27	100	67	100	27	100	67	100
	30	100	70	100	30	100	70	100
	31	100	71	100	31	100	71	100
	32	100	72	100	32	100	72	100
	33	100	73	100	33	100	73	100
	34	100	74	100	34	100	74	100
	35	100	75	100	35	100	75	100
	36	100	76	100	36	100	76	100
	37	100	77	100	37	100	77	100

TEST NO-03
(OVER)

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TROUBLE #5

TEST NO-03

TOTAL ERRORS 04000

DIGIT PLANE ERRORS						X AND Y LINE ERRORS					
	PICK	DROP		PICK	DROP	XL	ERRS	XL	ERRS	YL	ERRS	YL	ERRS
LS	0	0	RS	0	0	0	100	40	100	0	40	40	40
1	0	0	1	0	0	1	100	41	100	1	40	41	40
2	0	0	2	0	0	2	100	42	100	2	40	42	40
3	0	0	3	0	0	3	100	43	100	3	40	43	40
4	0	0	4	0	0	4	100	44	100	4	40	44	40
5	0	0	5	0	0	5	100	45	100	5	40	45	40
6	0	0	6	0	0	6	100	46	100	6	40	46	40
7	0	0	7	0	0	7	100	47	100	7	40	47	40
8	0	0	8	0	0	10	0	50	0	10	40	50	40
9	0	0	9	0	0	11	0	51	0	11	40	51	40
10	0	0	10	0	0	12	0	52	0	12	40	52	40
11	0	0	11	0	0	13	0	53	0	13	40	53	40
12	0	0	12	4000	0	14	0	54	0	14	40	54	40
13	0	0	13	0	0	15	0	55	0	15	40	55	40
14	0	0	14	0	0	16	0	56	0	16	40	56	40
15	0	0	15	0	0	17	0	57	0	17	40	57	40
						20	100	60	100	20	40	60	40
MGGS						21	100	61	100	21	40	61	40
XODD	XEVN	YODD	YEVN			22	100	62	100	22	40	62	40
2000	2000	2000	2000			23	100	63	100	23	40	63	40
DRIVER PANELS						24	100	64	100	24	40	64	40
	A	B	C	D		25	100	65	100	25	40	65	40
X	1000	1000	1000	1000		26	100	66	100	26	40	66	40
Y	1000	1000	1000	1000		27	100	67	100	27	40	67	40
						30	0	70	0	30	40	70	40
						31	0	71	0	31	40	71	40
						32	0	72	0	32	40	72	40
						33	0	73	0	33	40	73	40
						34	0	74	0	34	40	74	40
						35	0	75	0	35	40	75	40
						36	0	76	0	36	40	76	40
						37	0	77	0	37	40	77	40

Trouble #5 DPD for R12 Defective

B. Program Routines

1. Ones discrimination
2. Zeros discrimination
3. Regular addressing
4. Regular checkerboard complement
5. Inverted checkerboard complement
6. P. R. F. Test
7. Regular checkerboard, worst pattern weak one.
8. Regular checkerboard, strong zero.
9. Inverted checkerboard, weak one.
10. Inverted checkerboard, worst pattern, strong zero.
11. Study the overall flow diagram of the program.

C. Diagnostic Techniques

1. Refer to Maintenance Handbook Number 13 (642 Memory), Diagnostic Techniques Section for information about programs, printouts and characteristics of the 642 Memory.

D. Summary Questions

1. The Little Memory Program checks overall _____ and runs _____ on lines in MC group _____.

2. If a CMD did not conduct, this error would be detected with test number _____.

3. If a DPD would not conduct, this error would be detected by test number _____.

4. If a Memory Buffer FF would not set, this would be detected by test number _____.

5. Area one of the data reduction printout gives the _____ number and the total number of _____ failing.

6. Area two of the printout does not list failing _____ bits.

7. Area three lists the total errors on each _____ line.

XIV. Maintenance Procedures

A. General

NOTE: Refer to Maintenance Handbook Number 13 (642Memory) Corrective Procedures Section for the latest information about the items listed below.

1. Tuning Procedures for X10 Oscilloscope Probe.
2. Voltage Calibration of Tektronix Oscilloscope.
3. Sweep Calibration of Tektronix Oscilloscope.
4. 642 Memory Tuning Procedure.
5. Spare Clock's
6. P. U.'s that require adjustment upon replacement.
7. SA & DPD replacement.
8. Connecting the Spare Plane.

B. Summary Questions:

1. The Oscilloscope probe should only be adjusted when viewing the _____ _____ waveform.
2. The _____ _____ should be used when adjusting voltage calibration on the oscilloscope.
3. The Time Mark Generator is for _____ calibration.
4. When it becomes necessary to remove windows from Unit 11 for waveform checks remove only _____ at a time.

IV. Introduction to 256^2 Memory

A. Comparison of 64^2 and 256^2 Memories

		256^2	64^2
1.	Storage locations	$200{,}000_8$	$10{,}000_8$
2.	MAR	16 Bits	12 Bits
3.	DPD's	132	33
4.	SA's	33	33
5.	Sample times	8	1
6.	Memory Cycle	6 microsec.	6 microsec.
7.	Frame Nos.	65, 66, 67	10, 11, 12
8.	X & Y Drivers	512 Tape Cores	128 CMD's

B. Block Diagram Analysis

1. The 256^2 memory is divided into five sections: the selection section, the array section, the sense section, the DPD section, and the timing and gating section. The block diagram also includes the MBR since it is the only path by which information can be transferred into or out of the memory. This register is not a part of the 256^2 memory since it performs a common function for all three of the computer memories.

Refer to Page 14

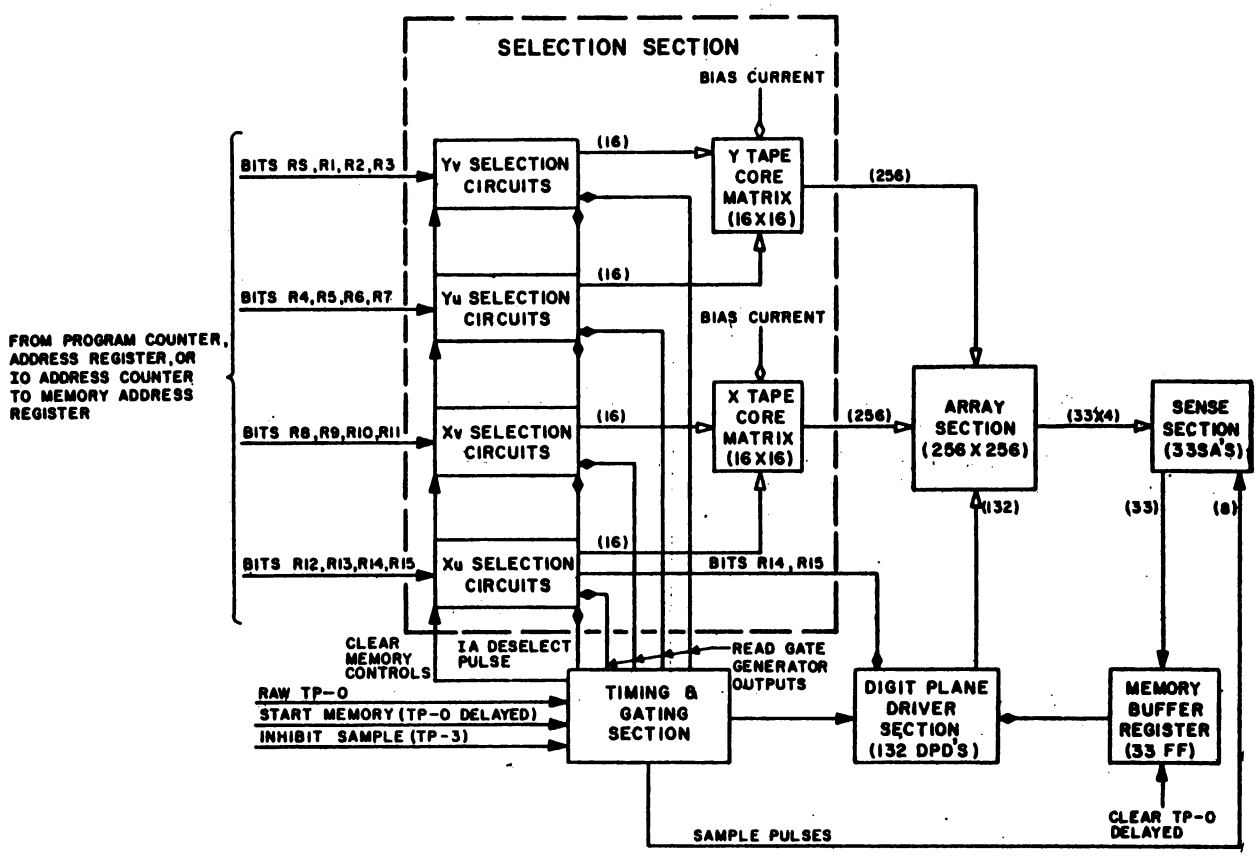
2. Normal operation of the 256^2 memory consists of transferring information into or out of specific registers of the core array. As a result, two specific types of memory cycles are possible; i.e., a readout cycle during which old information is obtained from selected cores, and a store cycle during which new information is stored in the selected cores.

3. The following sequence of events occurs during execution of a readout cycle:

   a. The desired address information is transferred to the selection circuits to condition the desired X and Y line drivers.

   b. A start memory pulse is generated.

   c. The MBR is cleared to prepare it for the subsequent information transfer.



256² Memory Device, Block Diagram

d. Read-current pulses are applied to the selected X and Y lines to switch all of the selected cores to the 0 state.

e. A sample pulse is generated to sample the output of the sense amplifiers. Individual outputs are used to set associated bits of the MBR.

f. Write-current pulses are applied to the selected X and Y lines to rewrite the information just read out. An inhibit-current pulse is applied to selected inhibit region of each plane, if required to prevent the writing of a 1 in the selected core.

g. The memory selection circuits are reset to prepare them for the next memory cycle.

4. The following sequence of events occurs during execution of the store cycle:

a. The desired address information is transferred to the selection circuits to condition the desired X and Y line drivers.

b. A start-memory pulse is generated.

c. The MBR is cleared.

d. New information is transferred to the MBR from an external source and an inhibit-sample pulse is generated.

e. Read-current pulses are applied to the selected X and Y lines to switch all of the selected cores to the 0 state, thus in effect erasing the old content.

f. Write-current pulses are applied to the selected X and Y lines to write the new information into the selected cores. An inhibit-current pulse is applied to the selected inhibit region of each plane, if required to prevent the writing of a 1 in the selected core.

g. The memory selection circuits are reset to prepare them for the next memory cycle.

5. Actually, during the operation of the 256^2 memory, a third type of cycle is possible, namely, the memory "not selected" cycle. The only operation performed in the 256^2 memory during such a condition (i.e., a memory cycle is executed but does not select the 256^2 memory) is that the memory selection circuits are reset to prepare them for the next memory cycle.

6. The operations performed during the execution of either a readout cycle or a store cycle are very similar, the only difference being that in the readout cycle a sample pulse is generated, while in the store cycle, the sample pulse is inhibited and the MBR is loaded from an external source. Since the two cycles are similar, the following analysis will be based on a readout cycle. This analysis will not discuss the various timing details since this information is covered in subsequent sections. Refer to page 1420

7. At TP 0, the content of the program counter, address register, or I0 address counter, which specifies the desired memory address, is transferred to the MAR (which was reset during the preceding memory cycle), four bits of information being transferred to each of the four selection circuit groups. The portion of the desired address contained in each selection circuit group is then decoded to condition one of its 16 tape core drivers; thus one tape core driver is conditioned in each of the four selection circuit groups.

8. Also at TP 0, a clear-memory-controls pulse (row TP 0) is applied to a 1.5 usec delay line in the timing and gating section. If the 256^2 memory is not selected for operation, then this delayed pulse will be gated to clear the MAR to prepare it for the next memory cycle. If the 256^2 memory is selected for operation, then this delayed TP 0 pulse is suppressed and the MAR is cleared later in the memory cycle by a delayed start memory 1 pulse.

9. If the 256^2 memory is selected for operation, then a start-memory-1 pulse is generated at approximately TP 0 +0.4 usec and applied to the timing and gating section. This pulse is applied to the memory pulse distributor (delay line clock) and also sets the Xv and Yv read gate generators. The output levels of these read gate generators are applied to their associated selection circuit groups to activate the conditioned tape core driver in each group. As a result, a read current pulse is generated on one of the 16 Xv and one of the 16 Yv matrix selection lines to partially select one line of 16 tape cores in each tape core matrix.

   a. The X or Y tape core matrix contains 256 tape cores connected in a 16 by 16 square formation. Selection of a specific core is based on the coincident current principle. However, because the cores are affected by a biasing current (a separate biasing winding is used), the selected tape core will generate a positive output when the coincident read-current pulses are applied and a negative output when the read-current pulses are terminated.

b. MAR - 16FF's - RS thru R15

Y - RS-R7

1) Yv - RS-R3
2) Yu - R4-R7

X - R8-R15

1) Xv - R8-R11
2) Xu - R12-R15

10. If the 256^2 memory is selected for operation, then the remaining internal operations are controlled by delayed-start-memory-control pulses which are obtained by tapping the delay line at various points. The first clock pulse is used to set the Xu and Yu read gate generators to initiate a read-current pulse on the selected Xu and Yu matrix selection lines. Since the Yv and Xv read gate generators have already been set, coincident read-current pulses are applied to one U and one V selection line of each tape core matrix. The tape core at the intersection of the selected U and V lines is switched to produce a positive output current pulse of sufficient amplitude and duration to half select a ferrite core. The tape core matrices operate in unison, thereby fully selecting a ferrite core. The current pulses are supplied to the 256^2 array to cause the 33 selected cores to be switched to the 0 state. The selected core output signals are applied to the sense section where they are amplified and applied to condition 33 gates. These gates are sensed by a clock-sample pulse; the conditioned gates will pass the sample pulse to set the associated bits of the MBR which was cleared at TP 1.

11. Clock pulses now clear the read gate generators, terminating the read-current pulses applied to the selected lines of the tape core matrices. Termination of the read-current pulses causes the two selected tape cores (one X and one Y) to be switched back to their original state. This action produces negative output current pulses of sufficient amplitide and duration to write half select the ferrite cores on the selected lines (one X and one Y) of the array. Since the two current pulses are generated in unison, the ferrite cores at the intersection of the selected X and Y line will be switched to the 1 state. However, the outputs of the MBR combined with the inhibit gate generator output are used to control the action of the 33 DPD's associated with the selected inhibit region of the array. If a particular bit of the original memory word contained a 0, the associated memory buffer flip-flop will contain a 0. Under this condition the associated DPD will generate an

inhibit-current pulse in the selected inhibit region of the array. Since the inhibit-current pulse is timed to actually overlap the write-current pulses applied to the array, the selected core of the associated plane will not be switched to the 1 state, but will remain in the 0 state.

12. During the latter portion of the memory cycle, a clock pulse is used to reset the memory address register (each selection circuit group contains 4 of the MAR flip-flops) in preparation for the next memory cycle. Since the output levels of the MAR are only used during the first half of the memory cycle (to specify which tape core drivers are to be activated), this reset action does not affect the remaining internal operations of the memory cycle being executed.

C. 256^2 Core Plane

1. Sub-planes are 64^2 planes

   a. Arranged in 4 x 4 layout to form one 256^2 plane. Refer to page 1470

2. Sub-planes are numbered 0 thru 17

3. Sense Sections Refer to page 1490

   a. Array is divided into 4 Sense Sections - 4 sub-planes per section.

   b. Sense sections are designated by letter A thru D as shown.

   c. Sense sections by sub-plane

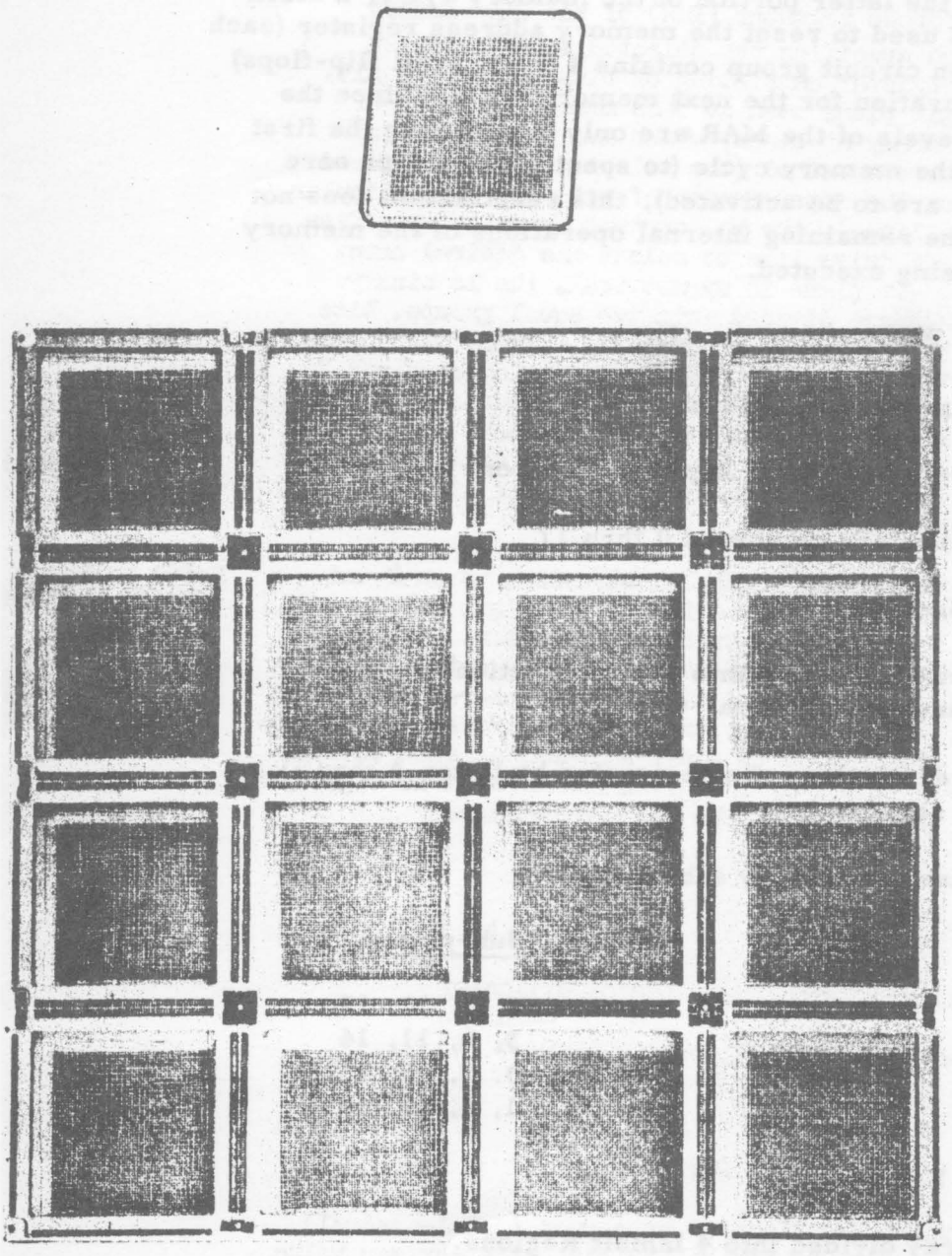
Section	Sub-planes
A	2, 5, 10, 17
B	3, 6, 11, 14
C	0, 7, 12, 15
D	1, 4, 13, 16

4. Inhibit Regions

   a. Array divided into 4 Inhibit Regions.

   b. Inhibit regions by sub-plane.

Region	Sub-planes
0	0, 4, 10, 14
1	1, 5, 11, 15
2	2, 6, 12, 16
3	3, 7, 13, 17



Comparison of 64^2 and 256^2 Core Memory Planes

D. Ocquad Addressing

1. The memory address register (MAR) of the 256^2 memory element, which specifies the selected memory address is a 16-bit register consisting of bits R8 through R15. Since the digit plane used in this memory consists of a 256 by 256 array of cores, which are selected by a coincident current method (the selected core is defined as the core at the intersection of mutually perpendicular X and Y drive lines), the MAR content actually specifies one X and one Y drive line to select the desired core. Because the digit plane is symmetrical, the 16 binary bits of the MAR are divided into two equal groups, bits R8 through R7 and bits R8 through R15. These two groups of binary bits are used to specify the selected Y and X drive lines respectively. Since the MAR content is usually designated by a 6-digit octal number, a conversion scheme is employed to convert the octal address designation into a short symmetrical system of X and Y drive line designation.

2. The MAR bits have been relabeled according to an X and Y notation, and regrouped to form two 3-digit numbers, based on an octal-quadral system of notation. The first two digits of each of these numbers are in octal notation (radix of 8), and the third digit is in quadral notation (radix of 4). To determine the X and Y line octal-quadral designation (ocquad) of an octal address, or vice versa, the binary equivalent of the given number must be regrouped to form the six digits of the desired notation.

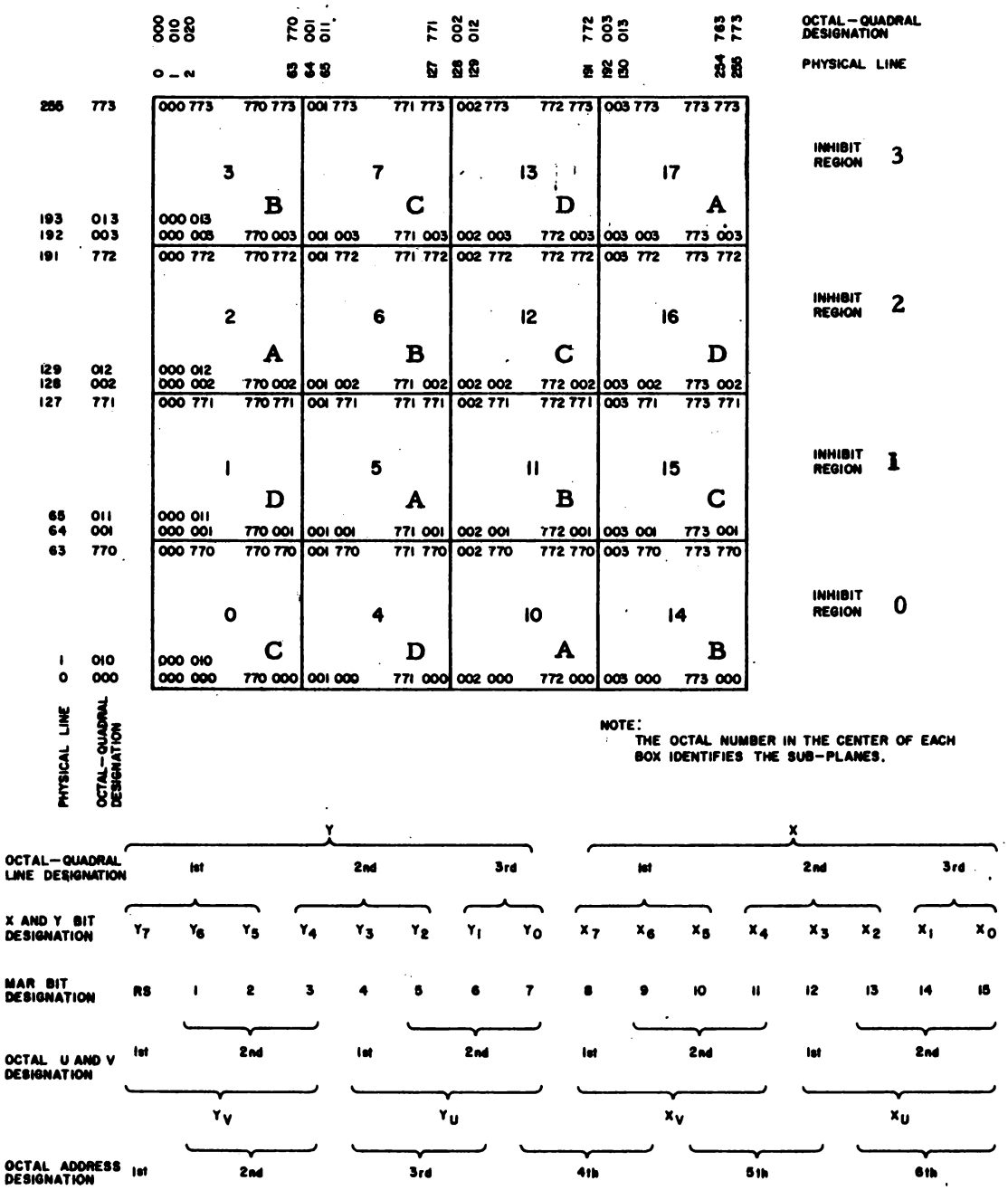
Refer to Page 1490

Example:

Octal Address	0	1	2	3	4	5
Binary Equivalent	000	101	001	111	001	01
Octal-Quadrant Equivalent	0	5	0	7	1	1
			Y		X	

NOTE

Since the third digit of an ocquad (octal-quadral) number represents two binary bits, the maximum value of this digit is 3. If a 1 is added to an ocquad number ending in 3, this maximum is exceeded, and the third digit develops a carry that is added to the next significant digit; namely, digit 2.



Addressing of 256² Memory

Example:

$543_{(ocquad)} + 1 = 550_{(ocquad)}$

In all cases, numbers to be added to an ocquad number must also be in ocquad notation.

3. The physical X and Y drive lines of each subplane are no longer referenced to the individual subplanes; rather, for addressing purposes, the X and Y drive lines are numbered in consecutive decimal order from 0 to 255. It should also be noted (from the ocquad designation shown for the associated physical lines) that consecutive X lines are contained in consecutive inhibit regions, and consecutive Y lines are contained in consecutive columns of subplanes. Since the MAR is grouped in a symmetrical system, the table is applicable for both X and Y line designation.

Refer to table Pages 1510 and 1520

4. In using the table to determine the physical line specified by an ocquad number, the least significant digit (3rd) of the ocquad number should be examined first to pinpoint the applicable columns as follows:

CONTENT OF 3rd DIGIT	PHYSICAL LINE COLUMNS
0	1
1	2
2	3
3	4

5. Since the first two digits of the ocquad numbers in each pair of columns are listed in consecutive order from 00 to 77, a brief search will yield the desired results.

Example:

Ocquad number 612 = physical line 177
The third digit of the example specifies that the ocquad number is contained in column 3 of page 1520.

Reference to the table shows that the ocquad number specifies physical line 177.

6. A study of the new addressing scheme reveals that selected cores can also be located by first identifying the subplane specified, and then determining which X and Y drive lines are specified within the selected subplane. It should also be noted that the third digit of the X line ocquad designation is always the same within an inhibit region, and the third

RELATIONSHIP OF PHYSICAL LINES TO OCQUAD LINE DESIGNATION

PHYS LINE	X-Y OCQUAD ADR	PHYS LINE	X-Y OCQUAD ADR	PHYS LINE	X-Y OCQUAD ADR	PHYS LINE	X-Y OCQUAD ADR
0	000	33	410	64	001	97	411
1	010	34	420	65	011	98	421
2	020	35	430	66	021	99	431
3	030	36	440	67	031	100	441
4	040	37	450	68	041	101	451
5	050	38	460	69	051	102	461
6	060	39	470	70	061	103	471
7	070	40	500	71	071	104	501
8	100	41	510	72	101	105	511
9	110	42	520	73	111	106	521
10	120	43	530	74	121	107	531
11	130	44	540	75	131	108	541
12	140	45	550	76	141	109	551
13	150	46	560	77	151	110	561
14	160	47	570	78	161	111	571
15	170	48	600	79	171	112	601
16	200	49	610	80	201	113	611
17	210	50	620	81	211	114	621
18	220	51	630	82	221	115	631
19	230	52	640	83	231	116	641
20	240	53	650	84	241	117	651
21	250	54	660	85	251	118	661
22	260	55	670	86	261	119	671
23	270	56	700	87	271	120	701
24	300	57	710	88	301	121	711
25	310	58	720	89	311	122	721
26	320	59	730	90	321	123	731
27	330	60	740	91	331	124	741
28	340	61	750	92	341	125	751
29	350	62	760	93	351	126	761
30	360	63	770	94	361	127	771
31	370			95	371		
32	400			96	401		

RELATIONSHIP OF PHYSICAL LINES TO OCQUAD LINE DESIGNATION (cont'd)

PHYS LINE	X-Y OCQUAD ADR	PHYS LINE	X-Y OCQUAD ADR	PHYS LINE	X-Y OCQUAD ADR	PHYS LINE	X-Y OCQUAD ADR
128	002	161	412	192	003	225	413
129	012	162	422	193	013	226	423
130	022	163	432	194	023	227	433
131	032	164	442	195	033	228	443
132	042	165	452	196	043	229	453
133	052	166	462	197	053	230	463
134	062	167	472	198	063	231	473
135	072	168	502	199	073	232	503
136	102	169	512	200	103	233	513
137	112	170	522	201	113	234	523
138	122	171	532	202	123	235	533
139	132	172	542	203	133	236	543
140	142	173	552	204	143	237	553
141	152	174	562	205	153	238	563
142	162	175	572	206	163	239	573
143	172	176	602	207	173	240	603
144	202	177	612	208	203	241	613
145	212	178	622	209	213	242	623
146	222	179	632	210	223	243	633
147	232	180	642	211	233	244	643
148	242	181	652	212	243	245	653
149	252	182	662	213	253	246	663
150	262	183	672	214	263	247	673
151	272	184	702	215	273	248	703
152	302	185	712	216	303	249	713
153	312	186	722	217	313	250	723
154	322	187	732	218	323	251	733
155	332	188	742	219	333	252	743
156	342	189	752	220	343	253	753
157	352	190	762	221	353	254	763
158	362	191	772	222	363	255	773
159	372			223	373		
160	402			224	403		

digit of the Y line ocquad designation is always the same within a column of subplanes. As a result the octal subplane designation corresponds to and is readily identified by regrouping the binary equivalent of the third and sixth digits of the ocquad address designation. These two ocquad digits, which consist of MAR bits Y_1, Y_0, X_1, and X_0, are regrouped so that the first digit of the octal subplane designation is specified by the content of bit Y_1, while the second digit is specified by the sum of bits Y_0, X_1, and X_0. Since the first two digits of the X and Y line ocquad designation specify consecutive physical X and Y lines (in octal notation) within a subplane, it is only necessary to determine which subplane is selected in order to completely identify the selected X and Y drive lines. The following example will serve to illustrate this fact.

Ocquad address	123 451
Binary equivalent of third and sixth digits	1101
Octal equivalent of third and sixth digits	15

Thus, ocquad address 123 451 selects the core at the intersection of Y = $12_{(8)}$ (10_{10}) and X = 45_8 (37_{10}) of subplane 15_8.

7. Subplane Selection

MAR BIT GROUPING				SELECTED SUBPLANE
Y_1	Y_0	X_1	X_0	(OCTAL)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	10
1	0	0	1	11
1	0	1	0	12
1	0	1	1	13
1	1	0	0	14
1	1	0	1	15
1	1	1	0	16
1	1	1	1	17

8. Numbers added to or subtracted from an ocquad number must of necessity be in ocquad notation. Thus, if it is desired to add the index register content to a memory address specified in ocquad notation, it is necessary to first convert the index register content into ocquad notation. In performing the actual addition, it must be noted that the third and sixth digits of the ocquad number are actually in quadral notation (radix of 4); therefore, the maximum number that can be expressed by these digits is 3. If this value is exceeded during the addition of quadral digits, develop a carry of 1 to the next most significant digit. The numerical difference represents the value of the quadral digit. When subtracting ocquad numbers (e.g., modification of the index register content by the index interval), these same precautions must be observed. The following examples serve to illustrate the addition and subtraction processes.

	OCTAL NOTATION	OCQUAD NOTATION
(1) Memory Address	0.03163	012 343
Index Register	0.01234	002 470
Sum	0.04417	021 033
(2) Index Register	0.01234	002 470
Index Interval	0.00452	001 122
Difference	0.00562	001 342

E. Summary Questions

1. There are 8 sample Times in the 256^2 Memory.

2. List the expanded memory frame numbers and state which is the array. 65 66 67

3. List which MAR Bits feed each of the four selection circuits. R 5 - R 3 R 4 R 2 R 1 R 0 - 15

4. A given ferrite core is to have a "0" written into it. How many cores on the same digit plane will receive inhibit current? 40 thru

5. A tape core will supply half-read current to how many ferrite cores? ≤ 1148

6. One SWD supplies current to how many ~~DDC~~ CCD's? 16 wd $\frac{1}{2}$ 20 (8)

7. In what manner is write current obtained? when read current is dropped, the bias taking over

Core Storage Element

8. How many inhibit regions are there in expanded memory? 4

9. Address 1.23456 is located in what subplane? 16

10. Convert the following octal addresses to their Octal-Quadral equivalent:

a.	0.76543	371	303
b.	0.53217	252	433
c.	0.76460	371	140
d.	1.23456	513	132
e.	1.76763	771	743

XVI. 256^2 Ferrite Core Array

A. Function and Capacity

1. The 256^2 ferrite core array contained in Unit 66 is the principal component of core memory 1 since it is the information storage center of this memory device.

2. The storage capacity of the 256^2 ferrite core array is equal to $65,536_{10}$ words of 33 bits each. Since a single core can store one bit of information, the array contains 65,536 x 33 or 2,162,688 ferrite cores. These cores are arranged in a 3-dimensional array in which each horizontal layer or digit plane contains 65,536 cores arranged in a 256 x 256 square formation. The 33 digit planes of this array are stacked vertically and the X and Y selection windings of these planes are interconnected to form the X and Y selection windings of the array. Actuation of the current drivers associated with one X and one Y selection winding will mutually affect the vertical column of 33 cores (one core in each digit plane) that represents the selected memory register.

Refer to page 1570

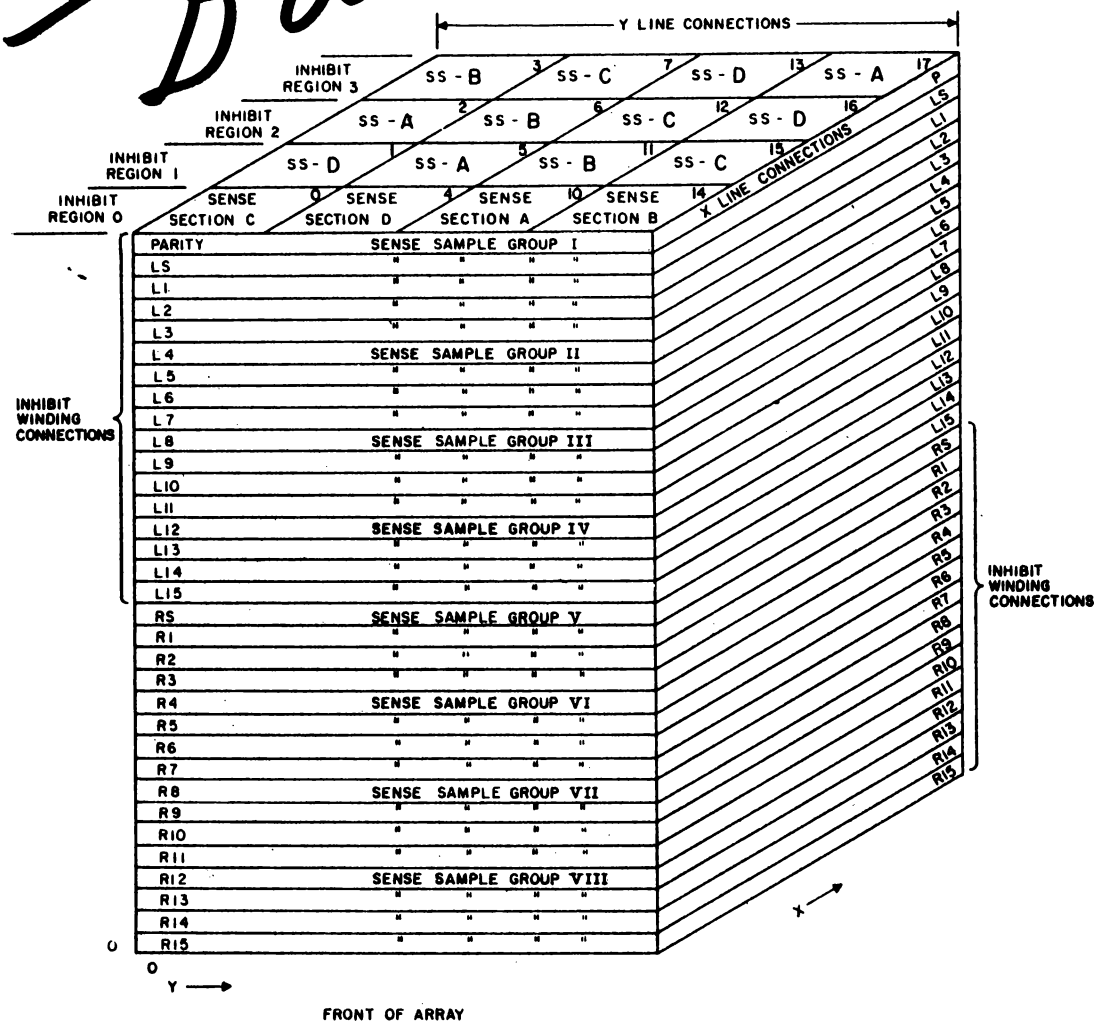
B. X and Y Selection Lines

1. Selection of a memory register involves the simultaneous application of read-write current pulses to the similarly addressed core in each digit plane. Therefore, the corresponding X and Y drive lines in each of the 33 digit planes of the array will be involved in the operation. In order to provide a control so that one current driver can supply read-write current pulses to the corresponding X or Y drive line of each digit plane, the similarly numbered X and Y drive lines of all digit planes are connected in series (by means of jumpers) so that common selection windings will be formed. One end of each of the 256X and 256Y selection windings is connected to a read-write current driver; the other end of each winding is connected to a terminating resistor. In this ferrite core array all of the X selection line drivers (256) are connected to the left and right sides of the array while all of the Y selection line drivers (256) are connected to the front and rear sides of the array. In each case, the selection line drivers are connected to the parity plane while the selection line terminating resistors are connected to the bit R15 plane. Since the input and output connections of the X and Y selection windings are the same, the following discussion will deal with the X selection windings only.

Refer to page 1590

2. The 256 X read-write current drivers, one for each X selection line, are connected to the array as shown. Current drivers for even numbered lines (0, 2, 4, etc.) are connected

33 planes
NO Spares
Direct



256² Memory Array

to the even numbered pins on the right side of the parity plane. The even numbered pins on the left side of the parity plane are jumpered to similarly numbered pins on the left side of the bit LS plane, the bit LS plane is similarly connected to plane L1 on the right side of the array, etc. Alternate planes are similarly connected to include the 33 planes of the array. The terminating resistors for these even numbered lines are connected to the left side of the bit R15 plane and mounted on the lower left side of the array.

3. Drivers for odd-numbered lines (1, 3, 5, ... 63) are connected to the odd-numbered pins on the left side of the parity plane. The odd-numbered pins on the right side of the parity plane are jumpered to similarly numbered pins on the right side of the LS plane. Alternate planes are similarly connected to include all 33 planes of the array. The terminating resistors for these odd-numbered lines are connected to the right side of the R15 plane. These terminating resistors are mounted on the lower right side of the array.

4. The Y selection windings are connected on the front and back sides of the array in exactly the same manner as described above. The even-numbered Y line drivers are connected to the even-numbered pins (0, 2, 4, etc.) on the front side of the parity plane; the odd-numbered Y line drivers are connected to the odd-numbered pins (1, 3, 5, etc.) on the rear side of the parity plane. The terminating resistors for even-numbered Y lines are mounted on the lower rear side of the array; the odd-numbered Y line terminating resistors are mounted on the lower front side of the array.

5. X and Y Addressing Refer to page 1590

   a. Ocquad Addresses

      1) Left to right facing panels A & D

      2) Right to left facing panels B & C

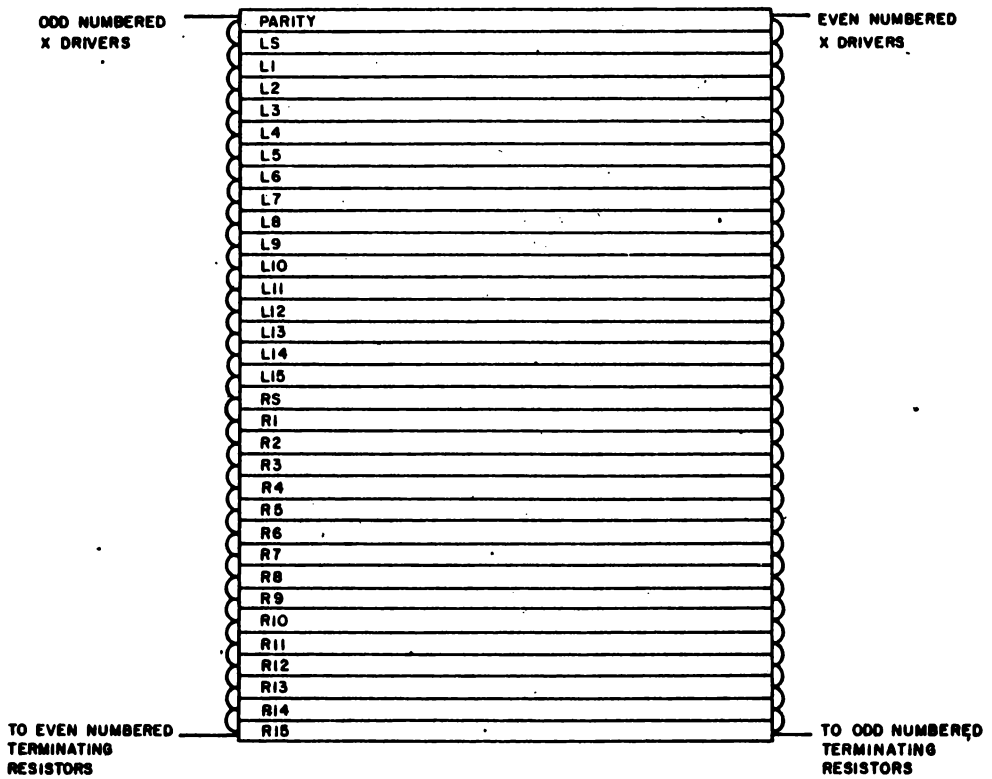
   b. Physical Lines

      1) Even physical drive lines (0, 2 - 62) enter on Panels A & D

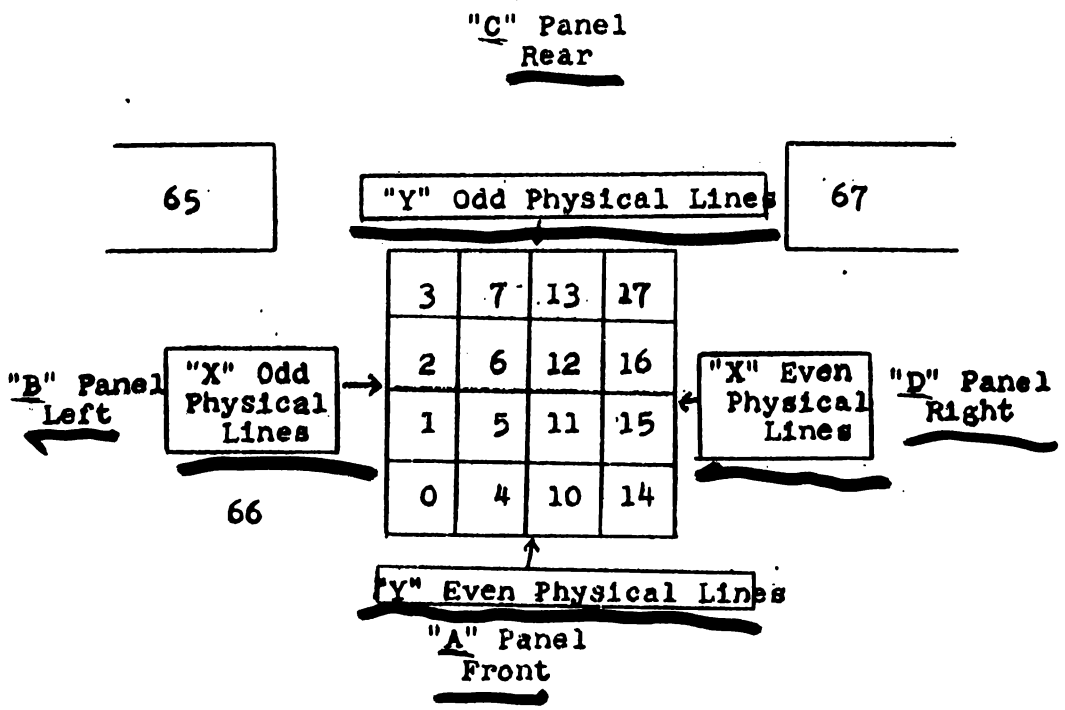
      2) Odd physical drive lines (1, 3 - 63) enter on Panels B & C

   c. Ocquad Even Addresses

      1) "Y" even addresses enter on sub-planes 0, 3, 10 & 13.



Front View of 256² Ferrite Core Array



2) "X" even addresses enter on sub-planes 0, 2, 14 & 16

d. Ocquad Odd Addresses

1) "Y" odd addresses enter on sub-planes 4, 7, 14 & 17.

2) "X" odd addresses enter on sub-planes 1, 15, 3 & 17.

e. Octal Portion of Ocquad Address

1) The octal portion of the ocquad address can be used to determine the panel that a drive line for a particular address enters the array.

Example: The octal portion (000 000 00) of an address will enter the array on its decimal equivalent.

Octal Portion	Physical Line	
0 - 76 enters on	0 - 62	Panels A & D
1 - 77 enters on	1 - 63	Panels B & C

6. Summarize

a. The quadral portion of the ocquad address can be used to determine the section (0-3) of the plane that a drive line enters the plane.

NOTE: Sections left to right (0-3) facing A & D.

b. The Octal portion of the ocquad address can be used to determine the line and side of the plane that an address enters.

c. Panel letter used in place of Module letter - 66A, 66B, 66C & 66D.

d. Odd & Even terminology (63 is the highest odd physical line, 0 is the lowest even physical line that enters a sub-plane.

C. Inhibit Windings

1. Each digit plane of the 256^2 ferrite core array is composed of 16 subplanes. Each subplane contains 4,096 cores arranged in a 64 x 64 square formation and all of the windings required for memory operation. Two distinct types of subplanes are used in the construction of this

array in order to provide for wiring symmetry. The two types of subplanes are very similar and differ only in the manner in which the inhibit winding is wound. The 256^2 array is actually composed of two types of digit planes. One type of subplane is used in the construction of 17 digit planes, while the second type is used in the construction of the other 16 digit planes of the array.

2. An abbreviated version of each type of subplane using 16 cores in a 4 x 4 formation reveals that the only difference between the two types of subplanes is that in the Type 1 subplane the inhibit winding is wound parallel to the X windings, while in the Type 2 subplane the inhibit winding is wound parallel to the Y windings.

Refer to Pages 1630 & 1640

   a. Inhibit parallel to Y drive lines in 17 of the Planes. (Parity Ll, L3 - R15, Odd bit planes)

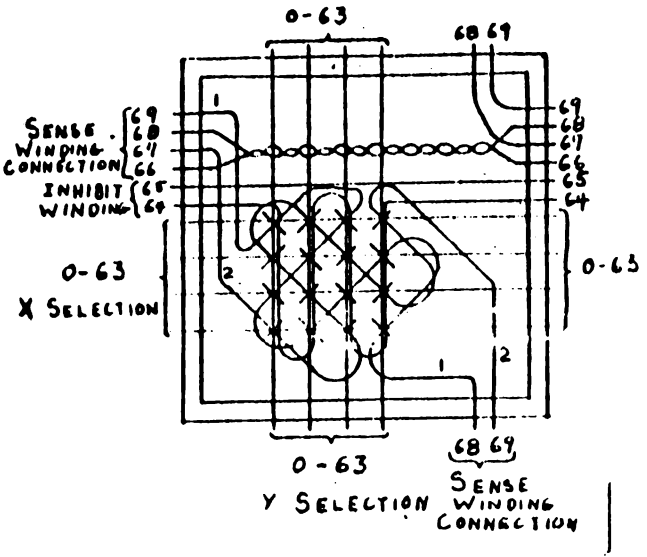
   b. Inhibit Parallel to X drive lines in 16 of the Planes. (L8, L2, - R14, Even Bit Planes)

3. The inhibit windings of four subplanes in a row are connected in series to form one winding. As a result, four such independent windings are obtained, one for each of the four inhibit regions into which the digit plane is divided. The four inhibit region windings of each digit plane are associated with individual DPD's. These drivers are controlled so that inhibit current, if required, is only generated in the inhibit regions which contains the selected core.

Refer to Pages 1660 and 1670

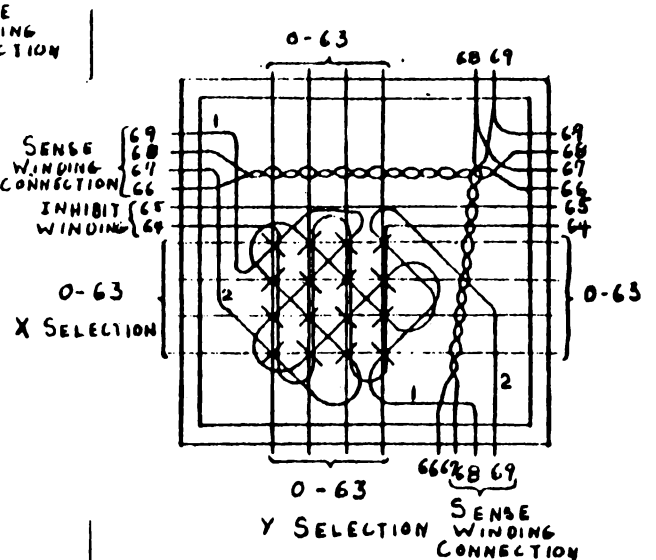
4. The subplane feedthrough wires (internally connected between pin 65 on the left and right sides) of each inhibit region are also connected in series to form a long wire. This feedthrough wire is connected to the inhibit region winding on one side of the digit plane (jumper between pins 64 and 65) so that the DPD input and terminating connections can both be made on the opposite side of the digit plane.

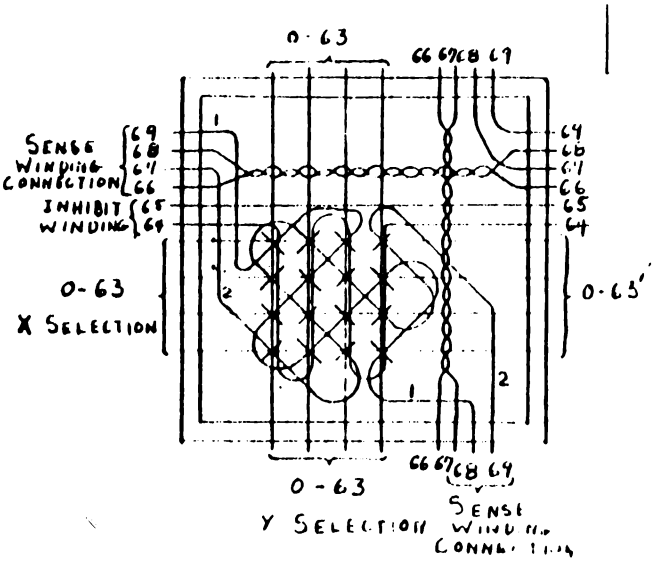
5. The external connections to the inhibt region windings readily identify the digit plane as being in either the left or right half-word. A digit plane of the left half-word (pins 64 and 65) for the inhibit region windings are located on the left side of the plane, while the feedthrough and inhibit windings are jumpered together (pins 64 and 65) on the right side of the plane. Conversely, the inhibit winding input and terminating connections for right half-word planes are made on the right side of the digit planes, while the feedthrough and inhibit windings are jumpered together (pins 64 and 65) on the left side of the plane.



Note: This sub-plane used for sub-planes 2, 3, 6, 7, 12, 13, 16, & 17 in Odd Bit positions. Even Bit positions have Inhibit Windings parallel to the X Windings.

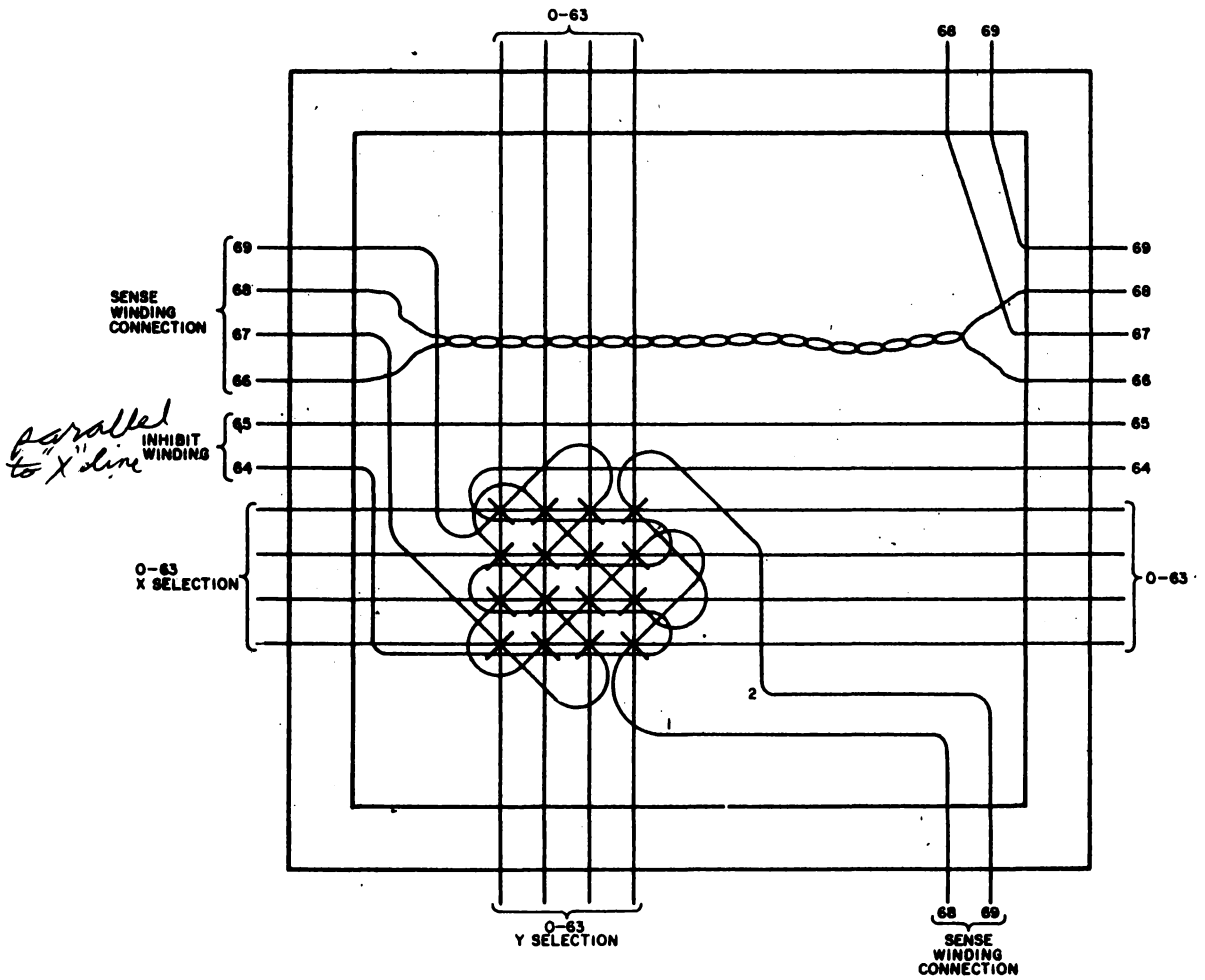
Note: This sub-plane used for sub-planes 1, 5, 11, & 15 in Bit positions Parity, L1, L3, L5 etc. Even Bit positions will have the same winding configuration with exception of Inhibit which runs parallel to the X Winding.





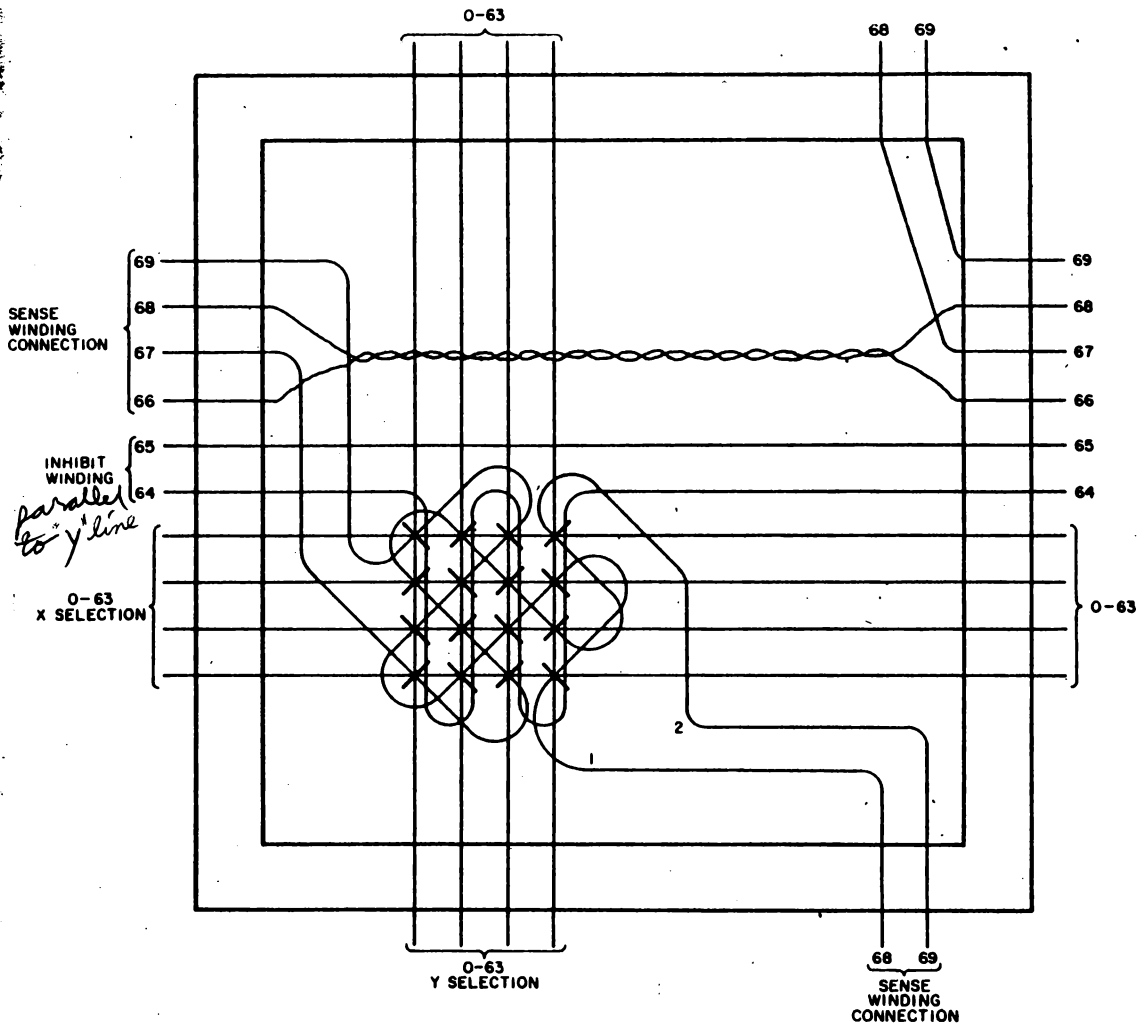
Note: This sub-plane used for sub-planes 0, 4, 10, & 14 in Odd Bit positions. Even Bit positions have Inhibit Windings parallel to the X Windings.

SENSE WINDING SUBPLANES



256^2 Subplane Wiring, Type 1

All Even Planes



256^2 Subplane Wiring, Type 2

all oddplanes

6. Because the X and Y array selection windings are formed by serially connecting the similarly numbered drive lines of adjacent digit planes, the direction of read-write current flow in the similarly numbered drive lines of adjacent digit planes will always be in mutually opposing directions. Since the inhibit-current pulse must always oppose the write-current pulses that are applied to the selected X and Y windings of each digit plane, the direction of the inhibit winding must also be reversed in adjacent digit planes. The required reversal in the inhibit winding direction of adjacent planes is accomplished by alternately connecting the DPD (associated with each digit plane) to pins 64 and 65 for each successive digit plane of the array.

7. Since the DPD's associated with the left half-word are all connected to the left side of the array, each DPD of the topmost or parity plane will be connected to pin 64 on the left side of the plane. Each DPD of the next lower or LS plane will be connected to pin 64 on the right side of the plane. This alternate pattern is repeated for the remainder of the left half-word with the result that each DPD of the L15 plane will be connected to pin 64 on the left side of the plane. Since the DPD's associated with the right half-word are connected to the right side of the array, each DPD of the RS plane will be connected to pin 64 on the right side of the plane. The alternate pattern of connecting the DPD's is resumed for each successive digit plane comprising the remainder of the right half-word.

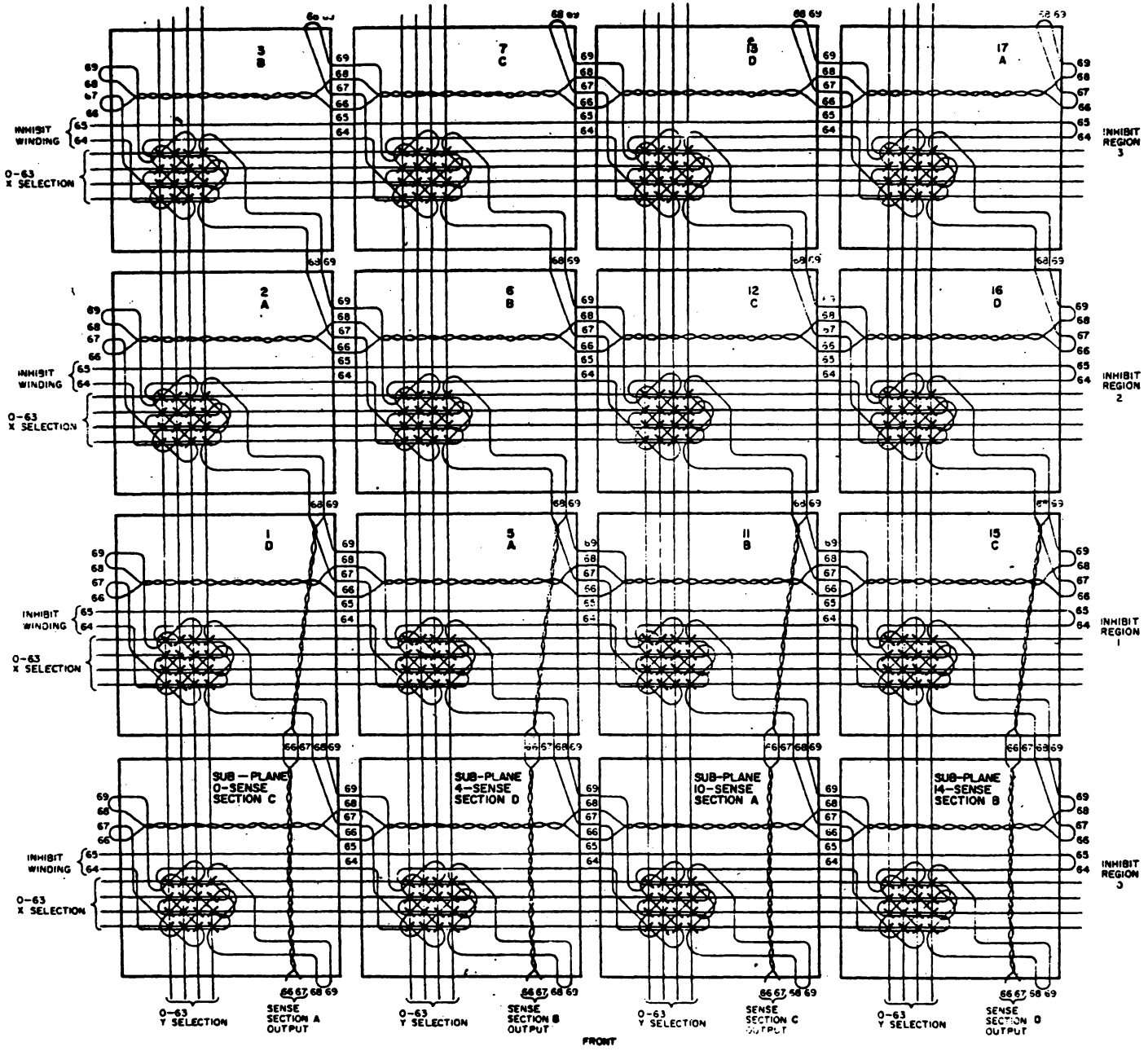
Refer to page 1570

8. The inhibit winding of each subplane of the 256^2 ferrite core array is associated with a digit plane driver (DPD). During the execution of a memory cycle, the associated DPD is controlled so that an inhibit-current pulse will be applied to the subplane inhibit winding (during the write portion of the cycle) if it is required to inhibit the writing of a 1 in the selected core of the subplane.

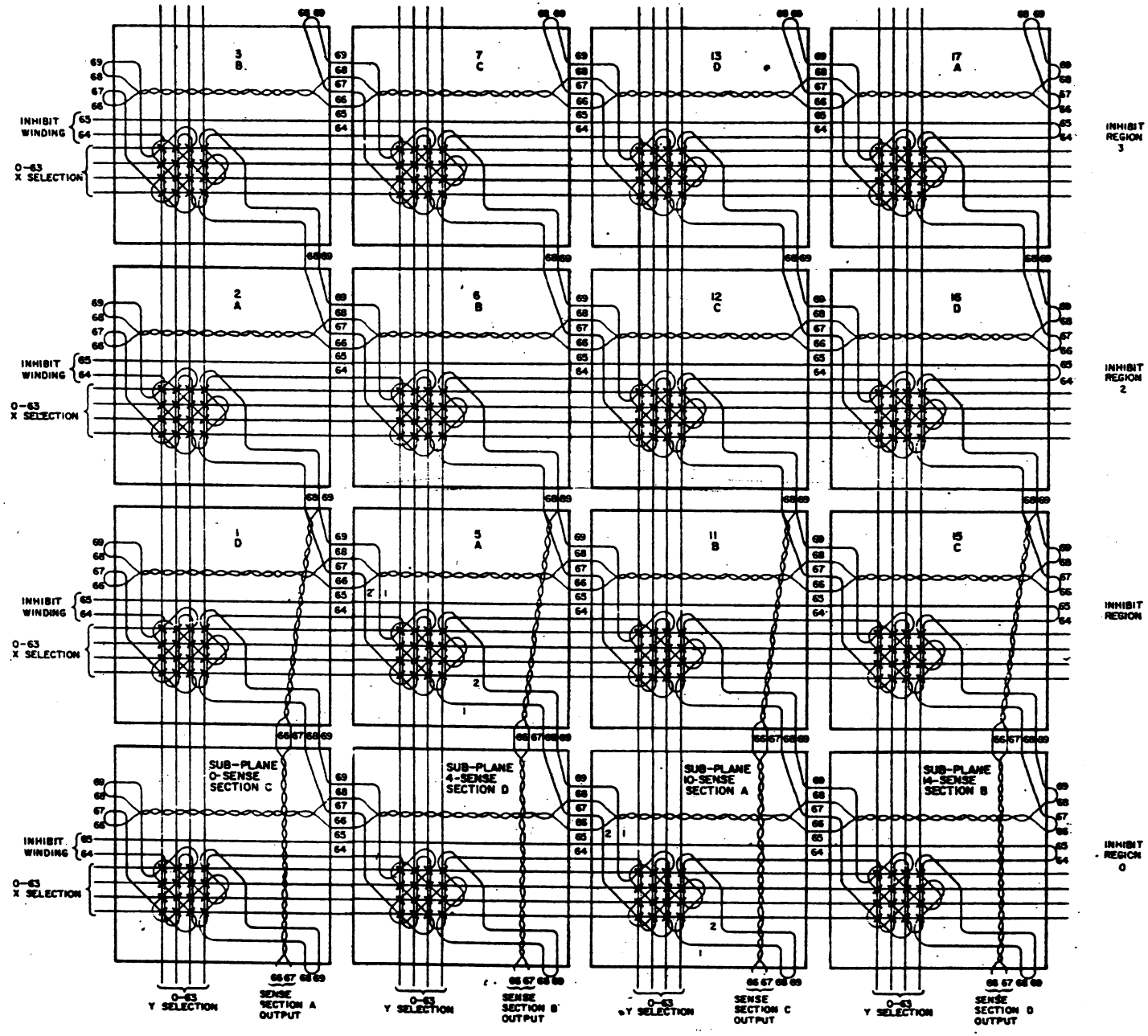
D. Sense Windings

1. The sense winding of each subplane of the array is associated with a differential input sense amplifier which functions to amplify the induced voltages that are produced by the switching action of each core in the subplane. Each subplane has two separate windings, labeled 1 and 2. (In the digit plane, these individual windings are connected in series by means of internal external jumper wires to form one long winding.) Each winding passes through half of the cores of the subplane following diagonal paths in order to minimize the

Refer to pages 1660 & 1670



256² f Plane Wiring, Type 1



256³ Digit Plane Wiring, Type 2

capacitive and inductive coupling between itself and the other windings of the subplane.

2. The subplanes of each digit plane are grouped into four sense sections with four subplanes in each section. The sense windings in the four subplanes of each sense section are connected in a series parallel arrangement to provide common output points. These common output points are connected to the front side of the digit plane by means of the vertical twisted pair wires that were added to the subplanes of inhibit regions 0 and 1. Refer to Pages 166 and 1670

3. Sense section A consists of subplanes 2, 5, 10, and 17. The sense windings of subplanes 5 and 10 are connected in series, and the sense windings of subplanes 2 and 17 are also connected in series. These two series-connected groups of windings are connected in parallel (by means of the twisted pair wires in subplanes 0 and 1) to supply one input to the associated sense amplifier.

4. Pin 69 at the back of subplane 1 is connected to pin 69 on the left side of the jumpered connection into subplane 5, then through sense winding 1 of subplane 5 and sense winding 2 of subplane 10 to pin 69 at front of subplane 10. Pin 69 is connected to pin 68. From pin 68 the path goes through sense winding 1 of subplane 10 and sense winding 3 of subplane 5 to pin 68 at the back of subplane 1. The series connection of the sense windings of subplanes 2 and 17 is similar to that for subplanes 5 and 10 with the addition of the twisted pair connecting link running through subplanes 2, 6, 12 and 16.

5. From pins 68 and 69 at the back of subplane 1, the series-parallel connected subplane sense windings are connected through twisted pair links in subplanes 1 and 0 to pins 66 and 67 at the front of subplane 0. These terminals are the external connections of the sense section A sense windings.

6. The connection of the sense windings of the other sense sections is similar to that just described for section A. Signals from the four sense sections of one digit plane are applied to the four input preamplifier channels of one sense amplifier. Thus, as a result of this wiring scheme, a single sense amplifier can detect and amplify the output signal from any core in a digit plane.

7. Sense Winding Outputs Refer to Page 170

   a. Output of sense winding felt by sense amplifier depends on where the fully selected core is on sense winding.

b. If the fully selected core is close to an end of the sense winding, then the output of the core will be felt by that end of the winding sooner than the output at the opposite end. (Less delay.)

c. The maximum output from the sense winding is when the core in the center of the series-parallel wiring arrangement is switched. As a result of the signal being produced at the center of the winding, maximum difference is felt by the SA at the ends of the winding.

8. Sense Winding Summary

a. Four per plane (A, B, C & D)

b. Sense windings effectively OR'rd together as input to to one SA.

c. Each SA input A, B, C & D to feel $\frac{1}{4}$ of the half-selections.

d. Each SA input A, B, C & D to feel $\frac{1}{4}$ the effects of an inhibit cycle.

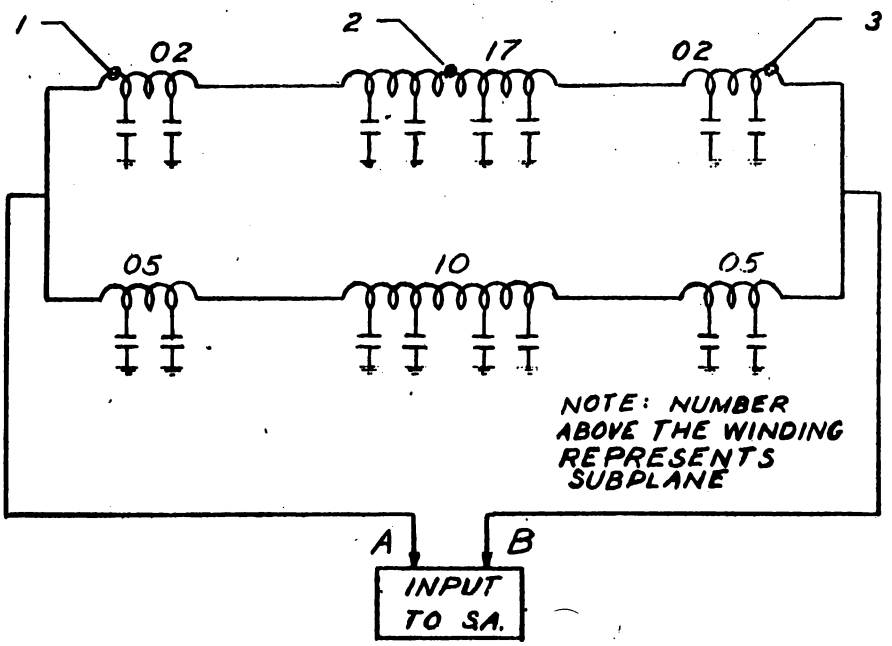
e. Of the noise generated on the four (4) SA windings, since they are effectively OR'ed together at the input to the SA, only the largest amplitude noise (as a result of half-selections and inhibit cycles) developed on one of the four inputs to the SA is felt by the common SA.

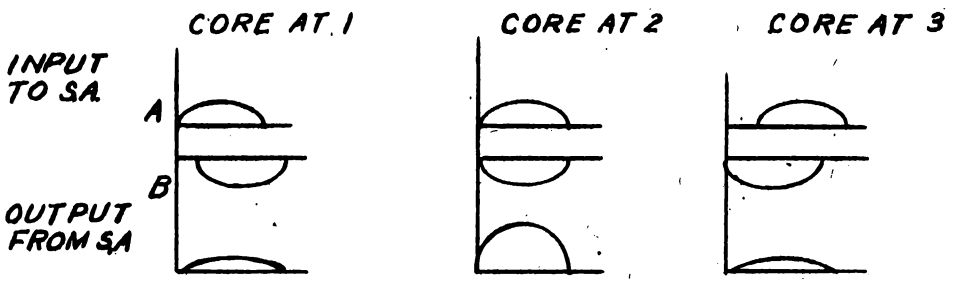
f. By having four inputs to the SA, the inputs could come at different times with respect to one another. This means that the duration or width of the common SA input could vary if the four input section outputs came at different times. Refer to Page 1700

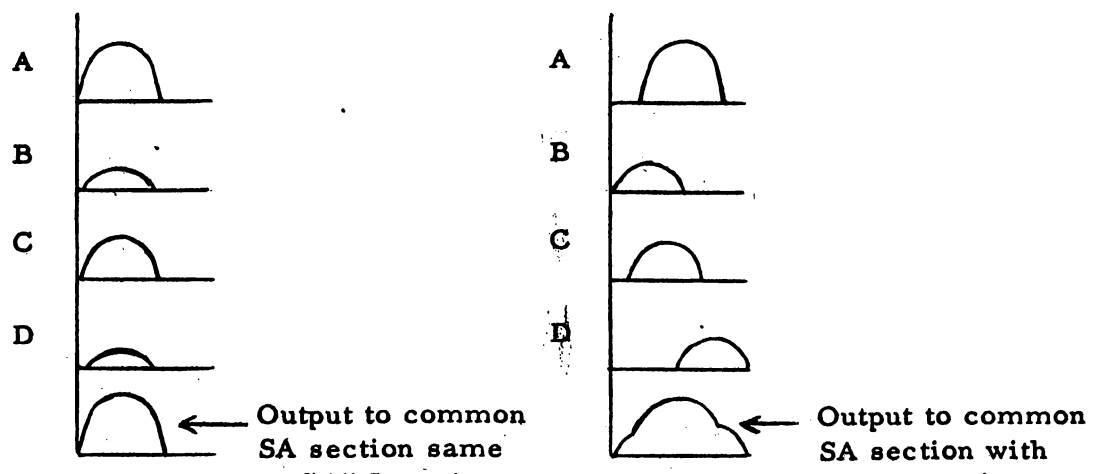
9. Sense Winding Sample Groups

a. Because the X and Y selection windings are electrically long, a definite amount of time is required for the read-write current pulses to appear at any specified point on the line; that is, these current pulses are delayed slightly as they travel through the array. This delay in the selection-line-current pulses affects the array readout timing, since all of the selected cores are not being switched at the same time. For optimum results, when a core is switched, the sense amplifier should be sampled. To insure optimum results the sense amplifiers are grouped to be sampled progressively. The time difference between these sense group sample pulses is approximately 0.04 usec. Refer to Page 1570

SENSE WINDING - SENSE REGION A







SA INPUTS

Core Storage Element

E. Transmission Line Characteristics

NOTE: Due to their length in relation to the wave lengths of the drive pulses the windings in the array must be considered as transmission lines and problems relative to them solved as such.

1. There are 256 X and 256 Y lines each approximately 100 ft. long.

2. There are 132 inhibit wires each approximately 192 ft. long.

3. There are 264 series sections of sense wire with each section approximately 100 ft. long.

4. Pulses are essentially square waves, many harmonics of which represent a much higher frequency than the repetition rate of the pulse.

5. A transmission line is two-conductors. The windings, when in the vicinity of ground, fulfills this requirement by using ground as the other conductor.

6. Drive lines of 100 ft. (as X or Y) represent an electrical length approximately one wave length long. This classifies the drive line as a long transmission line with inherent transmission line characteristics.

   a. Sense windings in parallel do not exhibit transmission line characteristics, the series portions of them do.

7. Transmission Line Characteristics

   a. Series inductance of the wire which takes into account the effect of all the ferrite cores on the wire.

   b. Series resistance of the wire at both DC and high frequency.

   c. Shunt resistance of the wire to all other wires in the array.

   d. Capacitance from the wire to all other wires in the array.

8. The characteristic impedance of the line is matched with a proper value of terminating load resistance.

   a. Series and shunt resistances are considered negligible effect.

b. Characteristic impedance calculated and lines terminated as follows:

1) X and Y lines = 140 ohms 55w

2) Inhibit lines = 147 ohms 25w

F. Summary Questions

1. For the following octal addresses, determine from the Ocquad designation what the corresponding "X" and "Y" physical drive lines are:

a. 0.74747 094 249
b. 1.73212 182 162
c. 1.66677 123 239
d. 0.00314 000 051
e. 0.45112 222 322

000.000.000.110.001.100

2. One drive line passes thru how many ferrite cores. 256 8448

3. How many ferrite cores will be half selected during the selection of an address? 510 16830

4. How many DPD's are used in 2562 memory? 132(10)

5. Which bits of the address word are used to select a DPD? ~~the last~~ 2 4 5 8 of MAR

6. How many cores on one sense winding will have inhibit current flowing thru them at any one time?

10 thousand [redacted]

256
33
768
768
0

2
400
100
0

556

Simplified Logic 256^2 Memory

A. Address Selection

1. The address selection process consists of decoding the contents of the memory address register and determining, on the basis of the information thus obtained, which X line and which Y line in the ferrite core array is to be driven in the subsequent reading and writing process. When read and write-current pulses are applied to the selected array lines, the read and write processes take place in the cores of the selected address; that is, in the cores at the junctions of the selected X and Y lines.

Refer to foldout Page 2900 Logic Diagram 256^2 Memory

2. The MAR content - which is transferred from either the program counter, address register, or IO address counter - is decoded by four groups of selection circuits. Two of these circuit groups are used to drive the U and V selection lines of one tape core (CCD) matrix. Each circuit group decodes four bits of the address to select one of its 16 switch drivers (SWD). When a read-gate signal is applied to the associated current regulator (CR), the selected switch driver delivers a current pulse to one U or one V selection line of its associated tape core (CCD) matrix. Each matrix receives a current pulse on both a U and V line and, as a result, a current pulse is generated on one of its 256 output lines. This current pulse drives one selection line of the ferrite core array. One tape core matrix drives an X line, and the other drives a Y line to complete the selection and driving process.

CIRCUIT GROUP	DIODE MATRIX DECODER INPUTS
Yv	R5-R3
Yu	R4-R7
Xv	R8-R11
Xu	R12-R15

B. Sense Section

1. The output of each sense section is connected to one of the four input sections of a sense amplifier; thus, each sense amplifier consists of four separate input sections and a common section. The common section of the sense amplifier contains a gating circuit which is sensed by a sample pulse to determine the output of the selected core. During a readout cycle, if the selected core contained a one, the associated MBR flip-flop, which is cleared at the beginning of the cycle, will be set to the 1 state. If the core contained a 0 the associated MBR flip-flop will remain in the 0 state.

2. The sample pulse does not sense all 33 sense amplifiers at the same time, but rather is delayed in steps of approximately 0.04 usec to sample groups of sense amplifiers. This delay in sample time between the first group and subsequent groups of sense amplifiers is required because of the delay inherent in the X and Y selection lines. For optimum results if a 1 is read out of a plane, it is necessary to sample the amplified output pulse when it is at its peak. The use of eight sample pulses compensates for the selection line delays and permits maximum memory reliability.

   a. Bit Sample Times

      1) P-L3
      2) L4-L7
      3) L8-L11
      4) L12-L15
      5) RS-R3
      6) R4-R7
      7) R8-R11
      8) R12-R15

3. During a store cycle the sample pulse generated by the memory clock must not be applied to the sense amplifiers. When such a cycle is executed, an inhibit sample pulse is supplied to the memory element at the beginning of the cycle. This pulse sets the sample gate generator, thereby deconditioning the sample gate so that the sample pulse will be inhibited during this cycle. The sample gate generator is cleared at the end of each memory cycle; thus a readout cycle is executed if an inhibit sample pulse is not supplied to the memory.

C. Inhibit Section

1. The DPD section of the 256^2 memory element contains 132 DPD's, which are used to supply inhibit current pulses to the memory planes of the array. The output of a DPD is a current pulse of approximately 410 ma, and the winding geometry of the array ensures that this output will have the same effect as a half-select read current pulse. An inhibit current pulse is used during the write portion of a memory cycle to prevent the writing of a one by cancelling the effect of one of the write-current pulses applied to the selected core of the plane.

2. The memory plane is divided into four inhibit regions, each region containing four subplanes. The individual subplane digit windings of an inhibit region are connected in series to form a common inhibit region digit winding. One DPD is used to supply an inhibit-current pulse to one inhibit region digit winding; thus, four DPD's are

required per memory plane. The four DPD's of each plane are controlled to supply an inhibit-current pulse, if required, to the inhibit region which contains the selected core.

3. Because of the method of addressing used in the 256^2 memory, consecutive memory addresses are contained in consecutive inhibit regions. Since four inhibit regions are available, the two least significant bits of a memory address contained in MAR bits R14 and R15 are used to determine which inhibit region is selected.

INHIBIT REGION	SUBPLANES	MAR BITS R14 and R15
0	0,4,10,14	00
1	1,5,11,15	01
2	2,6,12,16	10
3	3,7, 13,17	11

4. The inhibit gate generators are in the cleared state at the beginning of each memory cycle. If the 256^2 memory is selected for operation, a start-memory pulse is applied to the memory clock to initiate memory operation. During the read portion of the memory cycle, information is transferred to the MBR from either the selected memory address (readout cycle) or from an external source (store cycle). In either case, during the write portion of the memory cycle, the information contained in the MBR is written into the selected address. If specific bits of the MBR contain 0's then an inhibit current must be generated in the selected inhibit region of the associated memory planes to overlap the write-current pulse, thereby preventing the writing of a 1 in the selected core. A set-inhibit pulse is generated by the memory clock which senses the gate tubes controlled by MAR bits R14 and R15 to set the inhibit gate generator for the selected inhibit region. The selected inhibit gate generator develops a negative pulse (/10 to -30) on its 0-side output which is applied to the -AND input circuit of each associated DPD. If a particular MBR flip-flop contains a 0 its 1-side output will be at a -30-volt level and the negative AND circuit will activate the associated DPD circuit. An inhibit-current pulse will thus be generated in the selected inhibit region of the associated plane.

5. The selected inhibit gate generator is cleared approximately 2.0 usec after it was set; thus the inhibit-current pulse (2.0usec in duration) will properly overlap the write-current pulses.

6. There are two Inhibit Gate Generator Sections - one for the left word, one for right word. Both function the same.

D. Timing and Control Section.

1. The timing and control section consists of a memory pulse distributor (MPD) and the entire complement of gate generators controlled by it. The MPD is actually a long delay line (approximately 6.0 usec) which receives a start-memory pulse at the beginning of each 256^2 memory cycle. The delay line is tapped at several points, and the various delayed pulses are used to control the gating circuits. These gating circuits consist of flip-flops, whose output levels control the various memory circuit functions.

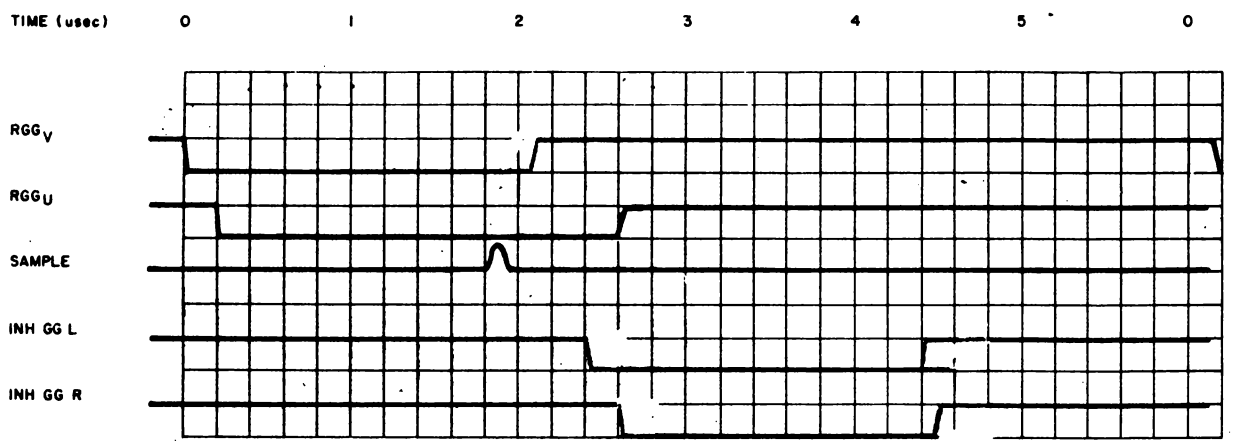
2. Three different input signals are supplied from the Central Computer System to condition and activate these circuits.

   a. TP 0 pulse
   b. Start-memory pulse (TP 0 delayed)
   c. Inhibit sample pulse (TP 2)

3. The first signal is supplied to the 256^2 memory, regardless of its selection status. If the 256^2 memory is not selected, the TP 0 pulse initiates action to reset the MAR and IA deselect flip-flop. If the 256^2 memory is selected for operation, the second pulse, start memory is also generated to control the timing of the read-, write- and inhibit-current pulses required during the execution of both the store cycle (OTb or B1) and the readout cycle(PT, OT or BO). During execution of the store cycle, the third pulse, inhibit sample, is also generated to inhibit the sampling of the sense amplifier, thereby erasing the content of the specified memory location during the read portion of the cycle.

4. The V gate generators are set by the start-memory-delayed pulse (approximately TP 0 +0.4 usec) to supply a negative gate to the conditioned Xv and Yv current regulators, which in turn control the generation of the current pulses supplied to the specified V selection lines of the tape core matrices. The TP 0 pulse is also applied to MPD IV; however in this example the MPD IV gate tube is conditioned when sensed, so that no action results. Approximately 0.2 usec after the start-memory pulse was generated, the U read gate generators are set to supply current pulses to the specified U selection lines of the tape core matrices. As a result, each tape core matrix is now supplied with U and V current pulses and the selected tape core of each matrix will switch to provide read-current pulses to the associated X and Y drive lines of the array.

Refer to timin chart on page 1770



256² Memory Selected, Timing Chart

5. Approximately 1.9 usec after the start-memory pulse was generated, MPD I develops a sample pulse which is applied to the sample gate generator tube. If a memory readout cycle is being executed, the gate tube will be conditioned so that the eight sample pulses will be applied to the 33 sense amplifiers. Staggered sample timing is required because of the delay characteristics of the X-Y drive lines.

6. Approximately 2 usec (MPD I) after the start-memory pulse, the Xv and Yv read gate generators are cleared to terminate the read-current pulses.

7. Approximately .6 usec later, MPD II generates a pulse to clear the Xu and Yu read gate generators to initiate the write portion of the cycle. The U and V read gate generators are set and cleared at separate times in order to speed up selection and also to reduce the noise generated in the sense winding. The action of clearing the read gate generators causes the two selected tape cores (one in each tape core matrix) to be switched back to the original state, thus generating the write-current pulses required by the associated array drive lines.

8. Approximately 2.4 usec after the start memory pulse the selected left word inhibit gate generator is set by a MPD II pulse which senses the six gate tubes controlled by the MAR bit R14 and R15 flip-flops. About 0.2 usec later the selected right word inhibit gate generator is set in exactly the same manner. The selected inhibit-gate pulses (negative pulses from 0 side output) sense the 33 digit plane drivers of the associated inhibit region; only those DPD's that are conditioned (at a -30-volt level) by the 1 side of the associated MBR flip-flop will pass the inhibit gate to activate the associated DPD, which in turn generates an inhibit-current pulse.

9. The left and right word inhibit gate generators are cleared at approximately 4.4 usec and 4.5 usec, respectively, after the start-memory pulse. Since the inhibit-current pulse of each plane must overlap the write-current pulse, staggered setting and clearing of the left and right word inhibit gates is required because of the delay characteristics of the X and Y drive lines.

10. During a memory cycle in which core memory 1 is selected, the MAR and IA deselect flip-flop are cleared by a MPD II pulse which is developed approximately 3.1 usec after the start-memory pulse was generated. Since the read gate generators are cleared prior to this time, the clearing of these controls does not affect the operation of the selected tape core in each of the tape core matrices. That is, the write portion of the memory cycle is not

affected by this clearing action. The MAR is cleared at this time in order to provide more time for the selection of the next memory address during the next memory cycle. If core memory 1 is not selected during a memory cycle , then the MAR and IA deselect flip-flop are cleared by a delayed TP 0 pulse. A raw RP 0 pulse is applied to MPD IV during every memory cycle. This pulse is delayed 1.5 usec and applied to the MPD IV gate which is controlled by the Yu read gate generator. Since this gate generator is set only by a delayed-start-memory pulse, the gate tube (MPD IV) is conditioned only when core memory 1 is not selected. If this latter condition exists, a core-memory-not-selected pulse is routed through MPD II to clear the MAR and IA deselect flip-flop approximately 1.5 usec after TP 0. The clear inhibit pulses which are generated by MPD III do not perform any useful function since none of the inhibit gate generators were set.

E. Summary Questions:

1. Answer the following questions TRUE or FALSE:

   a. The DMD will be cleared at TP-11 time.

   b. The four RGG's will be set at the same time.

   c. The MAR is loaded at TP-0 delayed time.

   d. There are 8 sample times approximately .04 usec apart.

2. What is the output current of a selected tape core?

3. The lagging edge of the read pulse is mainly controlled by the turn off time of which current in a fully selected tape core.

4. One CR supplies current to how many SWD's?

5. A core is located in Sub-Plane 15, the "X" address is 41_8. The "Y" address is 16_8. Determine the octal word designation for these locations.

   a. 0.35605
   b. 1.63411
   c. 0.16345
   d. 1.33411
   e. 0.35601

6. The total number of CCD's used with 256^2 memory is:

   a. 64
   b. 256
   c. 32
   d. 512
   e. 1024

7. When one **X** CCD is selected, how many **X** CCD's are half selected?

   a. 32
   b. 31
   c. 15
   d. 30
   e. 16

8. The write current is produced by turning off the V & U current. True _____ False _____.

9. The length of the read or write pulse is determined by the switching time of the tape cores. True _____ False _____.

10. Two SWD's must be fully conditioned to apply read current to one "X" line. True ___ False _____.

11. There are 510 half-selected cores for each fully-selected core in the 256^2 Memory. True_____ False_____.

12. An open "V" winding will effect 4096 addressed in the 256^2 array. True_____ False_____.

XVIII. Units 65, 66 and 67 Familiarization

A. Unit 66 Contents

1. CCD's (Two assemblies each panel)

2. 33 - 256^2 planes

3. X & Y terminating resistors

4. DPD terminating resistors

5. Various connectors for lines in and out of array.

6. Resistor and coil assemblies.

Refer to Pages 1860 and 1870

B. Unit 66 Designations

1. Panel A-D

2. Row A - PP

3. Suitcase (Left to right any panel) 1-8

4. Pin on Suitcase, A - S, T is common. (Measure current A-S common is T.)

Refer to Pages 1820, 1830, 1840 and 1850

Note: Ocquad address
Left to right - Panels A & D
Right to left - Panels B & C

Note: Use A address and locate X & Y termination terminals.

Example: 0.12345 = X 711, Y 050.
X 66 DPP4N, Y 66 APPIC

5. Tape Core Assemblies, Row B, 4 & 5 all panels.

6. DPD Termination Resistor Units

a. "B" and "D" panels
b. "A" Row

1820

c. 1 - 4 Assemblies
d. Pins A - T

Note: Assemblies designated left to right, both panels. Inhibit region reverses on Panel "B".

7. Study other assembly and connector designations on the panels.

8. 240 ohm resistor and CB shown in "Phantom" logic on bottom of Panel C. (X & Y Drive lines floating.)

9. The 256^2 plane's sections are designated 1-4 left to right facing the panel.

Example:
66AD1 Region 00
66AD2 Region 01
66AD3 Region 10
66AD4 Region 11

66CD1 Region 11
66CD2 Region 10
66CD3 Region 01
66CD4 Region 00

C. Unit 65 and 67 Contents

1. 5 modules each.

2. Extra tall modules (Row C - CC)

Refer to pages 1890 & 1900

3. Frame 65 is associated with the X circuitry in general, the Memory clocks the left word DPD's and Sense Amps, and Bias Fixing networks.

4. Frame 67 is associated in general with Y circuitry, Memory Clock #4, Right Word DPD's and Right Word S.A.'s.

5. Physical Location to Unit 66

Note: The SA's in both Units are the circuits next to the array.

6. Z Module
-450v supply and scope calibrator power source.

Refer to page 1910

a. -450v for CR's

D. Summary Questions

1. On which physical drive line and which sub-plane does the following address enter the array.
a. 0.54631
b. 1.77326
c. 1.66532
d. 0.45321
e. 1.00537

UNIT 67

PU	MODULES A		MODULES B		MODULES C		MODULES D		Z	PU
C	SWD'S Yv= 11, 12,		SWD'S Yv= 06, 07, 10		SWD'S Yu= 06, 07		SWD'S Yu=10, 11			C
D	SWD'S Yv= 13, 14		SWD'S Yv= 03,04,05		SWD'S Yu=04, 05		SWD'S Yu=12, 13			D
E	SWD'S Yv = 15, 16		SWD'S Yv=00, 01, 02		SWD'S Yu = 02, 03		SWD'S Yu=14, 15			E
F	SWD'S Yv =17		INH GG RHW INH REGION 2 (10)		INH GG RHW INH REGION 0(00)		SWD'S Yu =16, 17			F
G	Y RGG		SPARE		SPARE		Yv CR			G
H	SPARE		INH GG RHW INH REGION 3(11)		INH GG RHW INH REGION 1(01)		SPARE			H
J	MPD IV		SPARE		SWD'S Yu=00, 01		Yu CR			J
K	SA's	BIT R15	DPD'S INH REGS (10)(11)	BIT R15	DPD'S INH REGS (00)(01)	BIT R15	IA'S Yv =14, 15, 16, 17			K
L		R14		R14		R14	IA'S Yv=10, 11, 12, 13			L
M		R13		R13		R13	IA'S Yv=04, 05, 06, 07			M
N		R12		R12		R12	IA'S Yv=00, 01, 02, 03		POWER MODULE	N
P		R11		R11		R11	IA'S Yu =14, 15, 16, 17			P
R		R10		R10		R10	IA'S Yu=10, 11, 12, 13			R
S		R 9		R 9		R 9	IA'S Yu=04, 05, 06, 07			S
T		R 8		R 8		R 8	IA'S Yu=00, 01, 02, 03			T
U		R 7		R 7		R 7	Yu MAR	BIT R7		U
V		R 6		R 6		R 6		R6		V
W		R 5		R 5		R 5		R5		W
X		R 4		R 4		R 4		R4		X
Y		R 3		R 3		R 3	Yv MAR	BIT R3		Y
AA		R 2		R 2		R 2		R2		AA
BB		R 1		R 1		R 1		R1		BB
CC		RS		RS		RS		RS		CC

MODULAR LAYOUT, UNIT 67

1840

UNIT 65

PU	MODULES A	B	C	D	E	PU
C	SWD'S Xu=00,01	SWD'S Xu=02,03	SWD'S Xu=04,05	SWD'S Xv=06,07,10	SWD'S Xv=11,12	C
D	SPARE	SWD'S Xu=10,11	SWD'S Xu=06,07	SWD'S Xv=03,04,05	SWD'S Xv=13,14	D
E	SPARE	SWD'S Xu=12,13	SWD'S Xu=14,15	SWD'S Xv=00,01,02	SWD'S Xv=15,16	E
F	SPARE	SWD'S Xu=16,17	INH GG LHW INH REGION 1(01)	INH GG LHW INH REGION 3(11)	SWD'S Xv=17	F
G	DPD SEL GT'S RHW	Xv CR	SPARE	SPARE	X R GG	G
H	DPD SEL GT'S LHW	SPARE	INH GG LHW INH REGION 0(00)	INH GG LHW INH REGION 2(10)	SPARE	H
J	MPD I	Xu CR	DPD'S INH REGS (00)(01) L15	DPD'S INH REGS(10)(11) BIT L15	SA's BIT L15	J
K	MPD II	IA'S Xv=14,15,16,17	L14	L14	L14	K
L	MPD III	IA'S Xv=10,11,12,13	L13	L13	L13	L
M	SAMPLE GG	IA'S Xv=04,05,06,07	L12	L12	L12	M
N	IA DESELECT	IA'S Xv=00,01,02,03	L11	L11	L11	N
P	SPARE	IA'S Xu=14,15,16,17	L10	L10	L10	P
R		IA'S Xu=10,11,12,13	L9	L9	L9	R
S		IA'S Xu=04,05,06,07	L8	L8	L8	S
T		IA'S Xu=00,01,02,03	L7	L7	L7	T
U		Xu MAR BIT R15	L6	L6	L6	U
V		R14	L5	L5	L5	V
W		R13	L4	L4	L4	W
X		R12	L3	L3	L3	X
Y		Xv MAR BIT R11	L2	L2	L2	Y
AA	X-BFN	R10	L1	L1	L1	AA
BB	SPARE	R9	LS	LS	LS	BB
CC	Y-BFN	R8	P	P	P	CC

MODULAR LAYOUT, UNIT 65

1850

2. Locate the terminating resistors of the "X" and "Y" drive lines for the following addresses:

   a. 0.62345
   b. 1.36215
   c. 0.24261
   d. 0.75316
   e. 0.71575
   f. 0.47343
   g. 1.01007
   h. 1.32120
   i. 1.47176
   j. 0.63453

3. Locate the CCD P. U. for the following failing "X" addresses:

   a. 1.25733
   b. 1.57652
   c. 0.76575
   d. 1.61570
   e. 1.25003

4. Complete the following questions:

   Unit 66

   a. Panel "A" contains the "Y" even _____ and the "Y" _____ terminating resistors.

   b. DPD terminating resistors are located on Panels _____ and _____.

   c. The "Pulse Shaping Networks" are located on Panel _____ and are Units _____.

   d. CCD's resistors for Y(v) selections are located on Panel _____ in Units 66.

   e. To locate a defective DPD P. U. we utilize the _____ of the _____ address.

5. For the following addresses and bits designated locate the DPD connection necessary in order to observe the Inhibit Current:

   a. 0.47630 - P

   b. 1.77777 - R8

   c. 1.23456 - L15

   d. 0.00005 - L4

   e. 0.13570 - R8

6. Bit R9 is lost on every address. Which of the following could cause this:

   a. 66AGG3 pin 65 open (0.2.1.7)
   b. 66DGG3 pin 65 open (0.2.1.7)
   c. 65ER3a not connected (0.2.1.6)
   d. 67AS3a not connected (0.2.1.6)
   e. 65ERE8 open (0.2.1.6)

7. With C shim between 66AE1-0 and 66AF1-0 missing, how many addresses would fail? Which addresses (0.2.1.7)

8. SWD 4 - 67 BC (0.2.1.5 Sheet #2, 24A) fails to conduct which of the following addresses should fail?

   a. 0.50164 & 0.50166
   b. 0.70164& 0.50166
   c. 0.76435 & 0.54215
   d. 1.00001 & 0.00001
   e. None of the above.

9. What is the input terminal on the plane for R9 Inhibit of address 0.25252 (Logic 0.2.1.6)

   a. 66BP2-64
   b. 66BN2-65
   c. 66DFF3-64
   d. 66DGG3-65
   e. 66DHH3-64

1870

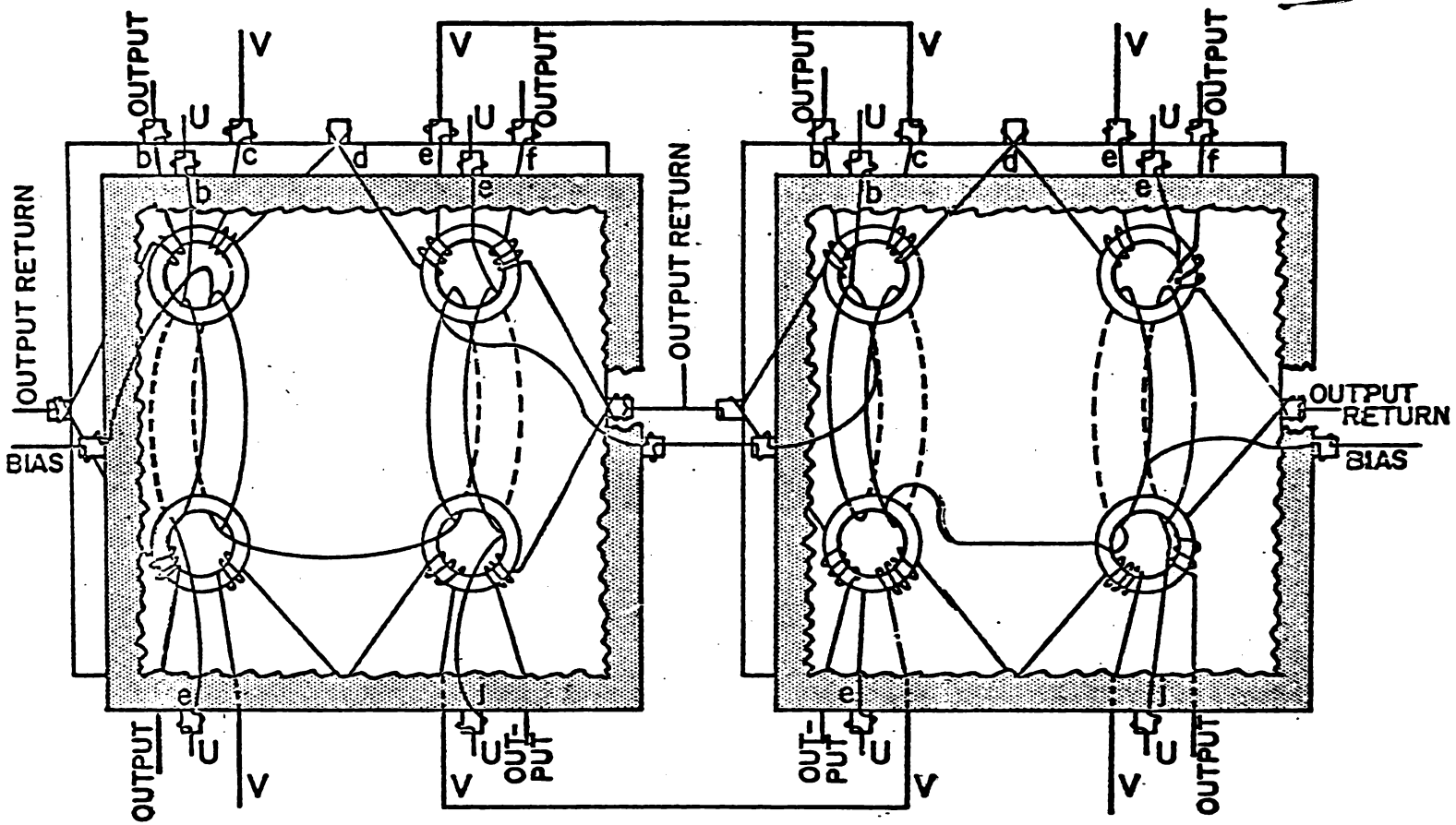
XIX. 256^2 Special Circuits

A. INTRODUCTION

The special circuits required for operation of the 256^2 memory will be presented in the following order:

1950

TAPE CORE LAYOUT



Top card has six connections on it; Bias (in and out), 4 U winding connections; center portion of card phantomed out to illustrate windings on cores.

Figure 9

B. Diode Matrix Decoder

1. The four DMD circuits are physically alike, and the only functional difference between them is the source of input signals and the destination of the output signals. The input signals are representative of information contained in the MAR. Since the circuit groups are alike, the following discussion will be based on only one of these; namely, the Xu selection circuit group.

DMD

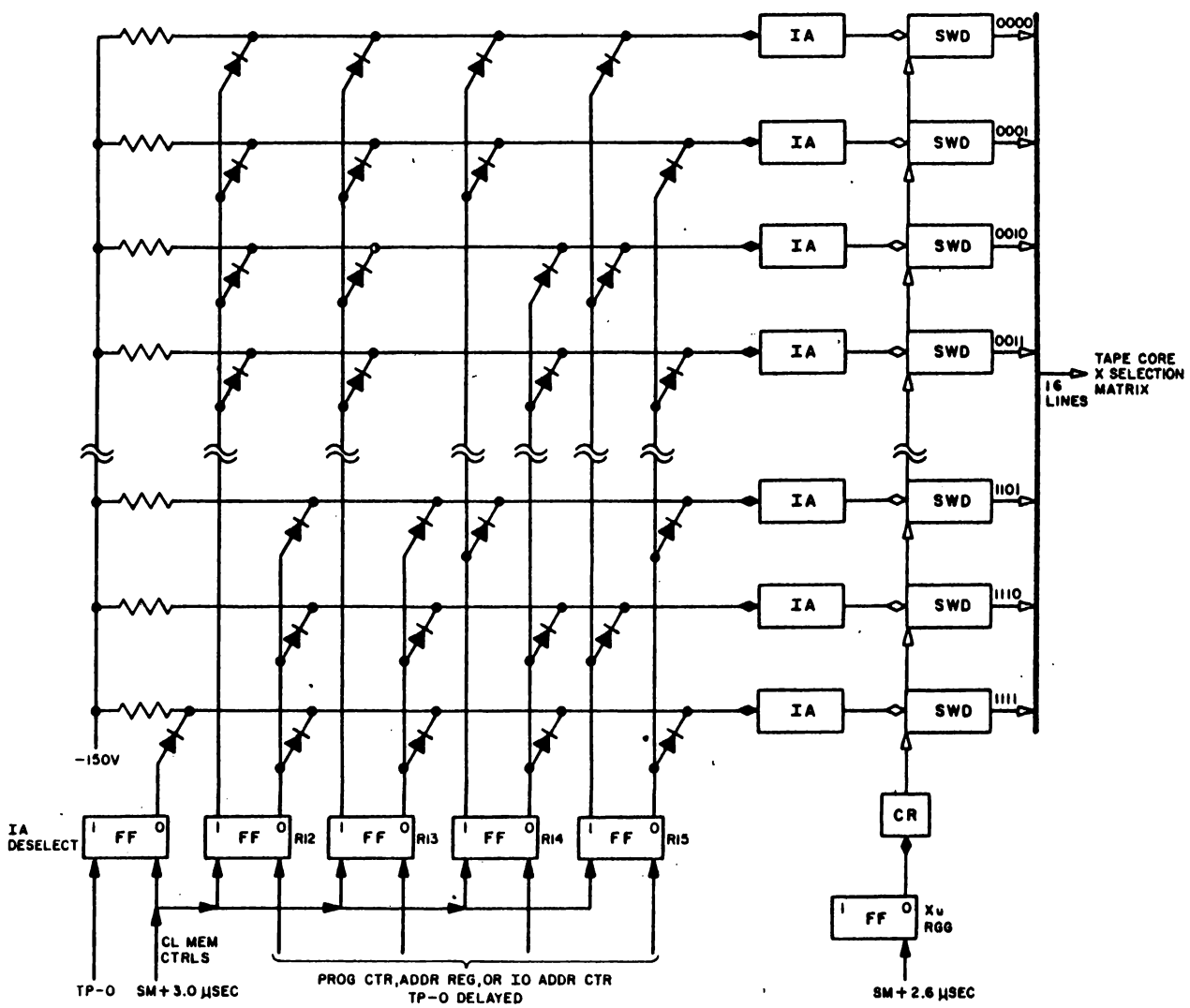
2. The clear-memory-controls pulse (delayed TP 0 or start-memory pulse) resets the MAR flip-flops and the input amplifier (IA) deselect flip-flop. At TP 0, the IA deselect flip-flop is set and the desired address is transferred to the MAR. The bit R12, R13, R14 and R15 flip-flop content is decoded by a 16-way AND diode matrix decoder (DMD) to condition one of the 16 input amplifiers. The 4-digit binary numbers associated with each of the matrix outputs can be selected (-30-volt level) at any one time; the remaining 15 outputs are at a +10-volt level. The outputs of the DMD are applied to the input amplifiers which invert, amplify and change the level of the input signal. The nonselected input amplifier outputs are at a -240-volt level (+10-volt input), and the selected input amplifier is at -150-volt level (-30-volt input).

Refer to pg. 2000

3. It should be noted that the -AND circuit whose output is designated by 1111 has an additional input from the IA deselect flip-flop. This additional input is required because the input amplifiers have capacitive coupling between stages and clamping circuits to hold their outputs at the nonselect level of -240 volts. When an input amplifier is selected, it can maintain its selected output level of -150 volts for only a short time, determined by the time constant of the capacitive coupling network. The output level will fall to the -240-volt level even though the input signal remains constant at a -30-volt level.

IA in & out

4. This means that when the same input amplifier is to be used during a number of consecutive cycles, it must be deselected and then selected again for each memory cycle. Deselection of 15 of the 16 input amplifiers is performed automatically when the MAR is cleared and then set to the new address. The 16th input amplifier is driven by the -AND circuit whose inputs are from the 0 sides of the bit R12, R13, R14 and R15 memory address register flip-flops. When each of these four flip-flops contains 1, designating the clear condition, four -30-volt conditioning levels are applied to the -AND circuit. If a number of consecutive memory cycles are executed in which address bits R12, R13, R14 and R15 remain cleared (contain 1's), the MAR flip-flop input levels to the -AND circuit will remain constant. To



Xu Selection Circuits

provide the IA deselection in this case, the -AND circuit has five inputs instead of four. The fifth input comes from the 0 side of the IA deselect flip-flop. The IA deselect flip-flop is set at TP 0 and applies a -30-volt level to the -AND circuit, enabling it to act as any other -AND circuit in the matrix. When the memory address register is cleared, the IA deselect flip-flop is also cleared. Its output to the -AND circuit becomes +10V, effectively deselecting the -AND circuit and the input amplifier it drives. Thus, in all cases a -30-volt gate is actually applied to the selected input amplifier, thereby insuring proper action.

1910

5. The output of each input amplifier is applied to an associated SWD. A switch driver is a gating circuit which, when conditioned by a -150-volt level, will pass a current pulse generated by a current regulator (CR) to drive the selected U line of the X tape core. The current regulator is a power amplifier which is activated by a negative read gate signal to generate a current pulse in one of the 16 associated SWD's. Only one SWD can have an output at any one time. The active SWD is the one receiving both a -150-volt conditioning level from an input amplifier and a current pulse from a current regulator.

C. Input Amplifier, Model B

1. Function Circuit on 1930

IA

a. The Model B input amplifier (bIA), employed in the 256^2 memory, functions as an inverter, amplifier, and level setter. The inputs to the bIA are standard levels of +10 and -30V obtained from a diode matrix in the memory address register; the outputs are non-standard levels of -240 and -150V, respectively. These outputs are fed to associated switch drivers as conditioning levels. (A -240V level will cut off the switch driver; a -150V level enables the switch driver to conduct.)

1920

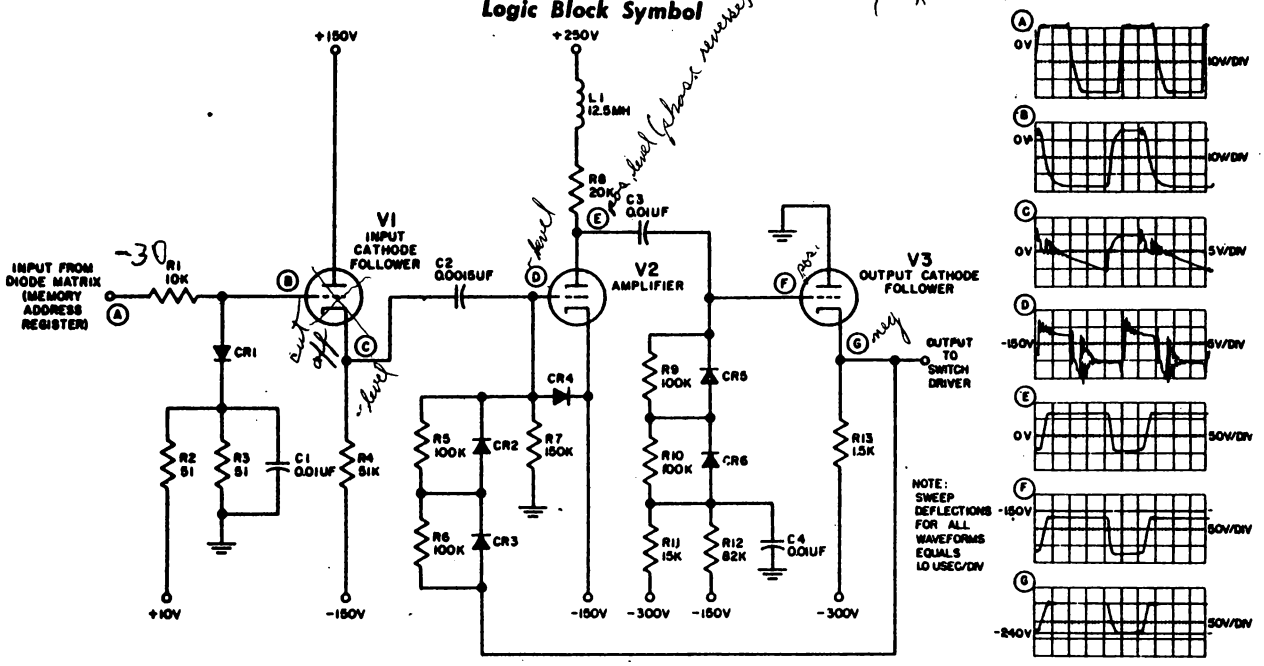
2. Principles of Operation

a. The bIA consists of three stages; an input cathode follower (VI), an amplifier (V2), and an output cathode follower (V3). The input cathode follower is employed as a buffer between the high output impedance of the associated input diode matrix and the low input impedance of the amplifier.

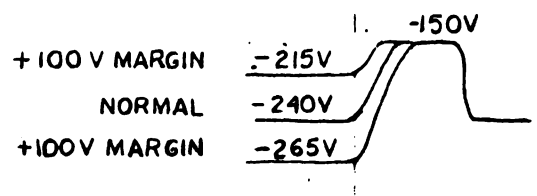
Refer to page 2030

b. The inputs supplied by the diode matrix are either /10 or -30 levels. Assume that the prevailing input level to the bIA is /10V; the voltage appearing at the grid of the input cathode follower is clamped at /5V by diode CR1. This clamping potential is obtained from the voltage divider consisting of resistors R2 and R3. The resulting potential at the cathode of V1 is /5V. The exponential rise noted in waveform C is due to the charge curve of capacitor C2. The grid voltage of V2 is established at -148V by the voltage divider consisting of resistors R5, R6 and R7 returned to the cathode of V3 whose potential is at -240V. Diodes CR2 and CR3 are cut off during this period of operation. The positive spike noted in waveform D at the transition time between the two states of operation for the bIA is due to capacitor C2 charging to the established d-c levels. Since the cathode of V2 is returned to -150V, the grid of V2 is slightly

Input Amplifier, Model B, Logic Block Symbol



Input Amplifier, Model B, Schematic Diagram



INPUT AMPLIFIER, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
C1	Bypass capacitor	R2, R3	Voltage divider
C2, C3	Coupling capacitors	R4	Cathode load resistor for V1
C4	Bypass capacitor	R5, R6	Part of voltage divider (with R7) returned to cathode of V3 and equalizing resistors for CR2 and CR3, respectively
CR1	Crystal diode, clamps V1 grid at +5V	R7	Part of voltage divider (with R5 and R6) and grid-limiting resistor for V2
CR2, CR3	Crystal diodes, clamp V2 grid at upper output level	R8	Plate load resistor for V2
CR4	Crystal diode, grid current bypass for V2	R9, R10	Voltage equalizing resistors for CR5 and CR6, respectively
CR5, CR6	Crystal diodes, clamp V3 grid at −273V	R11, R12	Voltage divider
L1	Peaking coil	R13	Cathode load resistor for V3
R1	Grid-limiting resistor		

positive with respect to its cathode, causing grid current to flow. In order to avoid exceeding the grid dissipation limit of V2, specifically during the initial period of the C2 charge curve, diode CR4 is placed between the grid and cathode of V2 to absorb a portion of the grid current flow. As a result of the bias level established for V2, its plate voltage at this time is -40V. The voltage divider, comprised of resistors R11 and R12, sets the grid voltage of V3 at -273V. This voltage is held at this level by clamping diodes CR5 and CR6. With the grid voltage at -273V, the resultant cathode potential is -240V. Thus, with a +10V input level to the bIA, a nonstandard level of -240V is established at the output.

c. When the input level shifts to -30V, the cathode potential of V1 decreases toward -5V. The exponential decrease of this voltage, illustrated in waveform C, is due to the discharge of capacitor C2. The voltage change at the cathode of V1 is coupled through C2 to the grid of V2. The resultant drop in the grid potential of V2 causes the plate voltage of V2 to rise from -40V to +65V. This change of 105V is coupled to the grid of V3 through capacitor C3, causing its grid potential to increase to -170V (diodes CR5 and CR6 are cut off at this time). As a result of this increase, the output cathode potential of V3 rises to -150V. Thus, with a -30V input level, a nonstandard level of -150V is developed by the bIA and applied to the associated switch drivers. This output level is also fed back to the grid of V2 through CR2 and CR3 to stabilize this upper output level. Diodes CR2 and CR3 remain cut off until the output voltage becomes more positive than the voltage appearing at the grid of V2. When the diodes conduct, the output voltage controls the grid voltage of V2. An increase in the output causes the grid of V2 to become more positive, decreasing the plate voltage of V2. This change is coupled to V3 with a resultant decrease in the grid voltage of V3 and consequently a decrease in the output level. The converse occurs for a decrease in the output voltage. It is in this manner that this degenerative feedback loop stabilizes the upper output level. Diodes CR2 and CR3 are cut off when the lower output level is developed. The negative voltage spike at the grid of V2 (See waveform D) is due to the delay in the feedback signal before CR2 and CR3 are made to conduct.

3. Input Amplifier Outputs

a. The I. A. (input Amplifier) output is -240v to -150v. These levels are maintained primarily by diodes in a feedback and clamping circuit. When these diodes go

bad one of the levels changes. If the -150V level goes to approximately -50 the result is excessive drive current on the lines selected by the I.A. If the -240V level goes more positive it tends to allow the associated switch driver (SWD) to go into partial conduction. This means that the SWD steals current from the selected circuit.

The most efficient method of detecting bad I.A.'s is thru scoping.

b. On a High PRF the deconditioning level on the output CF (5998 tube) goes to a more positive valve if the tube has the bad characteristic of excessive grid emission.

The 5998 tube is checked for this condition by testing in the P. U. Lab.

c. The I.A. margin finds defective I.A.'s. The best test is addressing with a ±100 volt excursion. The resultant printout will show one (if only one is bad) I.A. failing very few times. This is the defective one. If more than one is bad the indications are not conclusive.

Note: Bad IA will have least number of errors.

4. Margin applied to IA (-300 MC-C 1234) has the following effect on the output: Refer to Page 2030

a. Negative margin makes rise time of output appear to come later (in time) to SWD.

b. Positive margin makes rise time earlier and 90v swing is lessened (-215v to -150v).

5. All IA outputs should be exactly the same, a 90v positive output referenced at -240v. The -240v going more positive will partially condition a SWD which is not selected to steal the current from the selected SWD. The -150v level going more positive will cause high and early read currents.

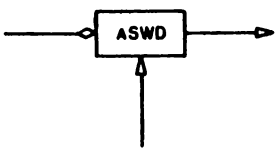
Switch Driver

SWD

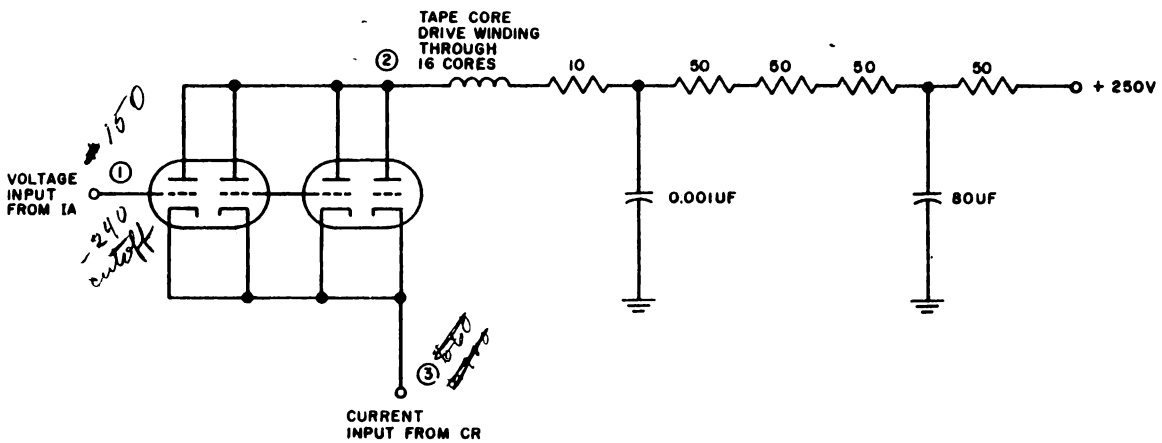
1. Function

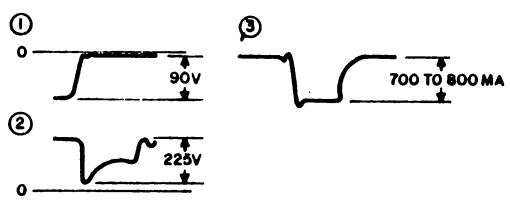
a. The switch driver (SWD) is a logic circuit which provides a nonstandard current pulse. The logic block symbol for the aSWD is shown on page 2060.

1960



Switch Driver, Model A,
Logic Block Symbol





Switch Driver, Model A, Schematic Diagram

b. In Central Computer logic, the SWD is used to isolate the current regulator pulse source from the back voltage produced by the 16 x 16 tape core matrix of the expanded memory. The SWD also affords a means of switching the current pulse to difference lines of the tape core matrix, thereby eliminating the need for separate pulse inputs for each line.

2. Detailed Operation

a. The circuit requires two coincident inputs to produce an output. The input amplifier supplies the SWD with nonstandard levels of -150V and -240V; the other input is a nonstandard current pulse from the current regulator. An output is produced only if a SWD is conditioned by the upper -150V level from its associated input amplifier and, at the same time, is supplied with a driving current from the current regulator.

b. Output usually considered in milliamps since the function is to furnish current.

1) If driving U windings current required is about 980 ma.

2) If driving V windings current required is about 670 ma.

c. Output of SWD supplies half-read current to 16 CCD's.

1) Thus selected SWD must be turned on or conducting.

2) Selected SWD has most positive signal on grid.

3) Deselected Swd must be turned OFF.

d. Two model switch drivers are used in the computer. Only the model A is shown on page 2060. The only difference is the model B contains only one tube. Two tubes are necessary to drive a V line and three are needed to drive a U line. Thus, one model A switch drive or two model B switch drivers in parallel can be used for V drive. One A switch driver in parallel with one B switch driver will be used for U drive.

3. Circuit Refinements

a. The components to the right of the tape core drive winding is not a part of the switch driver. These components are used to improve the leading edge of the current waveform to the tape cores. Page 2060

1980

b. The capacitors will hold the voltage at the termination end of the tape core drive winding at a high value until a short time after the Switch Driver has started to conduct. This reduces the affect of the high initial impedance of the tape core drive winding.

E. Current Regulator

1. Function

a. The Model B current regulator is a logic circuit which converts a voltage pulse to a current pulse.

b. The conditioning level is supplied by the Read Gate Generator FF.

c. The output pulse of current will supply all 16 switch drivers for either U or V. Only one switch driver will conduct in either U or V, which will allow the total current from the current regulator to flow thru 16 tape cores.

d. Circuit Requirements

1) Rise time should be adjustable from approximately 0.2 to 0.5 usec.

2) Amplitude should be variable from 500 to more than 1,000 ma.

3) Fall time should be adjustable from 0.2 usec to approximately 1 usec.

4) Time stability of the leading 90-percent point of the output current should be plus or minus 40 musec at end of life.

5) Amplitude stability of the output at end of life should be ± 2.5 percent, with a short time (1,500 hours) stability of ± 0.5 percent.

6) The top of the output current pulse should be adjustable from zero slope to a positive slope giving an increase, in the output current pulse, of approximately 20 percent across the width of the pulse. Adjustment of the output pulse slope is necessary to compensate for the capacity losses resulting from driving the tape core matrix. Compensation for capacity losses is necessary to obtain the flat-topped pulse required to switch the ferrite core. The tape core

output time constant was sufficiently long so as not to cause any more than 2-percent droop of the output pulse.

2. Basic Operation

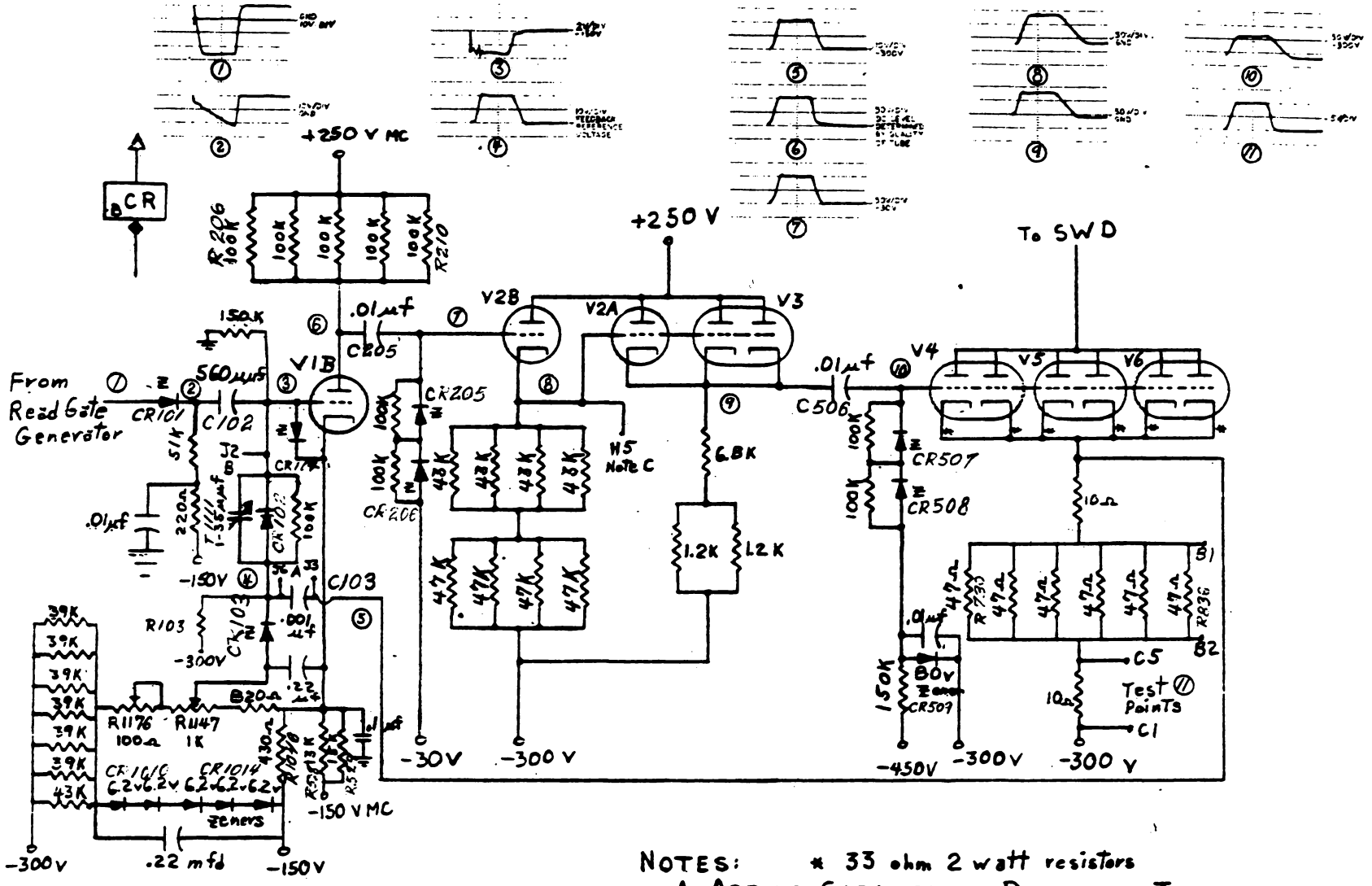
a. The model B current regulator consists of an amplifier (V1B, circuit diagram), a buffer cathode follower (V2B), a driver cathode follower (V2A, V3B and V3A), and an output stage of three twin triodes in parallel (V4, V5 and V6), which are one-half of a cascode amplifier with feedback to the input of the input amplifier. The switch driver circuits are 5998 tubes in parallel which serve as the upper half of the cascode amplifier formed by the output stage of the current regulator and the switch driver. The current regulator, turned on by standard levels (on by -30V and off by 10V), supplies a negative, 4.0 usec, 420 to 1200 ma pulse through a switch driver to one side of the 16^2 tape core matrix. The switch driver is conditioned by a -150V (rising from -240V) d-c level received from the input amplifiers and applied to the grids of the switch drivers.

Refer to Page 2100

3. Detailed Operation

a. Negative signals cut off the amplifier V1B, causing a sharp rise in plate voltage. Since only 6V of the negative 40V input transition is needed to cut the tube off, the input is too fast for the circuit to follow, if the fall of the input is equal to or less than 0.5 usec.

b. The rise of the plate of V1B is coupled through C205 to the buffer cathode follower V2B. V2B provides buffering for the drive necessary for the relatively low input impedance of the driver cathode follower, V2A, V3B and V3A. The positive signal on the grid of V2B back-biases the d-c restoring diodes, CR205 and CR206. The rising signal on the grid of V2B causes the cathode voltage to rise which, in turn, raises the voltages on the grids of the driver cathode follower (V2A, V3B, V3A). The cathode rise of the driver cathode follower is coupled to the grids of the final stage (V4, V5 and V6) by C506. The rise on the grids of the final stage back-biases the d-c restoring diodes CR507 and CR508, and, at the same time, raises the output cathode voltages. Part of this voltage rise is fed back to the grid of the input amplifier, V1B. The rising feedback voltage back-biases CR103 and forward-biases CR102, at which time the output feedback voltage takes over control of the amplifier grid.



Current Regulator, Model B, Schematic Diagram

2000

c. Trimmer capacitor T1111 provides a portion of the feedback voltage to the grid of V1B prior to CR102 becoming forward-biased. This initial feedback has a tendency to increase the current through V1B (or, more accurately, to decrease the rate at which the current is falling), thereby slowing the rise time of V1B. The plate of V1B, in the absence of feedback, rises sufficiently fast to produce an output rise time of approximately 0.1 usec. The feedback not only slows the rise time, but also makes the rise time of the circuit independent of the load resistance and plate voltage of V1B. Terminals are provided across the trimmer capacitor T1111 (refer to note B in the circuit schematic) to allow capacitance external to the circuit to be added in order to change the range of the rise time control.

d. The signal required at the amplifier grid for normal circuit operation is -2V. Prior to the arrival of the feedback signal through C103, diode CR103 is forward biased by the current drawn by R103. The plate voltage of CR103 is normally fixed by the divider across the Zener diodes CR1010 to CR1014 at between -160V and -180V. Since the voltage drop across CR103 is small, the voltage at the grid side of C103 is approximately equal to the voltage out of the divider across the Zener diodes.

e. If the grid side of C103 is at a potential of -170V, this point is 20V negative with respect to the cathode of V1B. An 18V positive signal fed back through C103 would raise the grid of V1B to a potential of 2V negative with respect to its cathode. This 18V signal then would determine the output current, which would be 18V divided by the cathode resistance of the final stage.

f. The time constant resulting from C103 charging through R103 and the forward impedances of CR102 and R104 have been selected so that C103 will, during the width of a pulse, lose sufficient charge to increase the grid-cathode potential of V1B. The discharge of C103 decreases the voltage applied at the junction of CR102 and CR103. This voltage fall lowers the amplifier grid voltage, causing the plate voltage to rise. The voltage rise is coupled to the output, giving the output a positive slope across the top of the pulse. Terminals are provided across C103 (see note B) in order that external capacity can be added to increase the time constant.

g. If the time constant produced by C103 and R103 is made sufficiently long, the voltage at the grid of V1B remains constant during the width of the pulse. Consequently, the plate voltage of V1B remains constant and the output is a flat-topped waveform. Potentiometers R1147 and R1176 permit coarse and fine adjustment of the voltage fed back through C103. As the input signal rises toward +10V, CR101 is forward-biased at a time when the input signal becomes more positive than the cathode voltage of CR101. At this time the cathode of CR101 begins to rise, causing the grid of V1B to rise. The grid rises about 2V to a point where the grid-cathode potential is equal to zero. At this point, the grid ceases to rise; however, the cathode of CR101 continues to rise, changing C102. The changing path for C102 is through the plate of the cathode follower driving the circuit (read gate generator), CR101, the grid-cathode diode of V1B, and the parallel diode CR104 to -150V. After CR101 has been forward-biased, approximately 3V of the input signal are required to turn the circuit off. Therefore, the turn-off of the circuit is independent of the positive transition of the input signal. As V1B draws grid current, the plate voltage is decreased by the current through V1B. This falling voltage cuts off V2B. The fall time will be determined by the cathode resistance of V2B and the capacitance seen by the cathode (refer to note C).

h. The output can be adjusted also by changing the cathode resistor of the output state (B1 - B2). Since the output current is the feedback voltage divided by the cathode resistance, the range of the output current will be increased by shorting resistors R730 and R836. The stability of the circuit is a function of the feedback voltage and is directly proportional to the amplitude of the feedback voltage. Therefore, in order to obtain the same stability with a small output current as would be achieved with a large output current, the cathode resistance must be increased.

i. The fall time of the circuit is adjustable by adding external capacitance to ground from the cathode of the buffer cathode follower (see note C). Increasing the capacitance to ground from this point will increase the fall time of the cathode of V2B, thereby increasing the fall time of the grids of the final stage and the fall time of the output. Since the input capacity of V2B is quite small, the grid will fall faster than the cathode, cutting off V2B. The fall time will be determined by the cathode resistance of V2B and the capacitance that may be added externally to adjust the fall time.

j. The circuit is shut off as the input signal goes from -30V to +10V. With C205 charging through the plate load of V1B during the time of a pulse, the d-c voltage must be restored by diodes CR205 and CR206 when the circuit is turned off. The d-c voltage across C506 is restored by diodes CR507 and CR508.

k. When the input is a +10V, the grid of V1B is held slightly positive with respect to the cathode by current flowing from ground through R104 and through the grid cathode of V1B and CR104 to -150V. CR104 was added to decrease the charging current of C102 through the grid circuit of V1B in order to keep grid dissipation within acceptable limits. With the grid at approximately -150V, CR102 is back-biased since CR103 is forward-biased by R103 and the voltage at the center-tap of R1147. The grid of the buffer cathode follower (V2B) is biased at -30V; therefore, the cathode is slightly more positive and the cathodes of the driver cathode follower (V2A, V3B, V3A) are still more positive. The final stage (V4, V5, V6) is biased at cutoff (approximately 80V) by Zener diode CR509, and no current flows from the output.

l. Waveforms for the model B current regulator and switch driver are shown on the circuit diagram, Page 2100 . The input is fed through CR101 to make the circuit independent of the driving stage. If CR101 were not used C102 would discharge through the cathode resistor of the cathode follower driving the current regulator circuit during the pulse time. If this occurred, the rise time would be a function of the driving circuit used and, therefore, would be impossible to predict. With the configuration used, the driving circuit merely triggers the input, after which CR101 is back-biased and the discharge path is through R101. The discharge is constant, regardless of the driving source.

m. A Zener diode network is utilized for the feedback reference supply (voltage between cathode of V1B and moving contact of R1147) in order to meet the design stability specifications. The diode network is referenced at -150V to provide a plate supply sufficiently large to prevent supply variations from affecting the rise time and amplitude from V1B.

n. The plate of the amplifier is a-c coupled to the grid of the buffer cathode follower to make the plate-cathode potential of V2B independent of the quality at V1B. D-c coupling between V1B and V2B would have two primary disadvantages:

1) A possible loss in signal and consequent reduction in loop gain and stability.

2) A change in the plate-cathode potential of V2B as the characteristics of V1B changed with life. When V2B is pulsed, grid current will be drawn if the plate cathode potential has previously been decreased.

o. In addition, a-c coupling is required between the driver cathode follower and the final stage in order to avoid signal loss, to make the cutoff voltage independent of the tubes and to protect the circuitry from failures which would allow the circuit to be turned on for long periods of time.

p. The bias voltage of the final stage is critical because it will affect the size of the signal necessary to produce a given current. Furthermore, the bias voltage will affect the time of the 10 and 90 percent points of the output rise if the signal has to change to compensate for a change in the biased voltage. These considerations prove the necessity of having the bias voltage independent of power supplies or resistors. The bias voltage of the output stage is stabilized with a Zener diode, CR509, making the amplitude, rise time and the leading 90-percent point of the output independent of the power supplies.

4. Marginal Checking

a. The model B current regulator is marginal checked by varying the +250V plate supply of V1B. The +250 MCV safe limits are 100V. The circuit is considered to have failed when the output leading 90-percent point varies in time by ± 40 musec or more, or in amplitude by ± 2.5 percent or more. A positive excursion causes the output to move earlier in time and to increase in amplitude. The positive excursion necessary to cause a circuit with nominal components to fail is 250V. A negative excursion will cause the output to move later in time and decrease in amplitude. A negative 75V margin will cause the output of a nominal circuit to move later in time by 40 musec and to decrease in amplitude by 2 percent.

b. The negative excursion on the +250 MCV line will decrease when any component or voltage changes, as is shown by the marginal check curves included in the appendix (figs. C-1 to C-39). For example, the +250V margins will be decreased if the filament supply is low, even though all of the other parameters are nominal.

Refer to Maintenance Handbook

c. If CR104 opens, the marginal checking system will not detect the malfunction. With CR104 open, the grid dissipation of V1B will exceed the maximum rating and the life of the tube will be shortened. Therefore, if V1B needs to be replaced frequently, CR104 is probably open.

d. The general reliability of the 256^2 memory is a function of the permissible variation of the drive currents. Because of this fact, a marginal check voltage was added to the model B current regulator to allow output current variation, thereby facilitating memory tune-up and system evaluation. The -150V marginal check supply is introduced in the cathode return of V1B, thereby affecting the feedback reference voltage and the output current of the circuit. With no excursion applied, resistors R1046, R528 and R529 are in parallel and appear as an equivalent network of 400 ohms to the -150 supply. Therefore, the circuit is not affected by variations of the -150V or the -150MCV supplies as long as no excursions are applied.

e. The equivalent resistance of R1046, R528 and R529 is critical. The equivalent resistance has been chosen so as to eliminate changes in the output amplitude when the pulse repetition frequency is changed.

f. A positive excursion increases the output current. The change in the output current is approximately 15 percent for 100V excursions. The percentage change is independent of the output current.

g. The switch drivers are marginal checked by varying the +250V plate return. The safe limits are +0V and -50V. A negative excursion will decrease the switch drive plate-cathode voltage, causing grid current to flow. Since the total cathode current from the switch driver is regulated by the current regulator, grid current will cause a reduction in plate current. The reduction in plate current will cause a reduction in the memory drive current resulting in improper retention of information by the memory.

5. Circuit Characteristics

a. Input Signal

Upper level	$+10 \pm 5$ V
	-2
Lower level	-30 ± 5 V
	-2
Rise time	0.5 usec, maximum
Fall time	0.5 usec, maximum
Polarity	Negative
Pulse width	4.0 usec maximum (at 90-percent point)
PRF	169 kc, maximum

b. Load Presented to Driver

I (OR)	3.4 ma (maximum, when circuit is not selected)
I (AND)	0.15 ma (maximum, when circuit is selected at 50-percent duty cycle and maximum PRF)
Capacity	120 uuf

c. Output Characteristics:

Amplitude	600 to 1,200 ma, with external jumper across cathode resistors of V2B
Rise time	0.27 to 0.5 usec, with no external capacity added.
Rise time lag	0.1 usec at the 10-percent point of the current pulse with respect to the 10-percent point of the input voltage
Fall time	Adjustable by the addition of external capacity

Pulse top slope

External capacity	Pulse slope
0	-160 ma/usec
0.001 uf	60 ma/usec
0.0025 uf	20 ma/usec
0.004 uf	0 ma/usec
0.01 uf	-12 ma/usec

PRF	169 kc, maximum
Pulse width	Approximately the same as the input (4.0 usec maximum at 90-percent points)
Output load	As many as 16 logical switch drivers, each as many as 3 model B switch drivers, or a model B and a model A switch driver in parallel.

F. Tape Core Matrix

TAPE CORE MATRIX

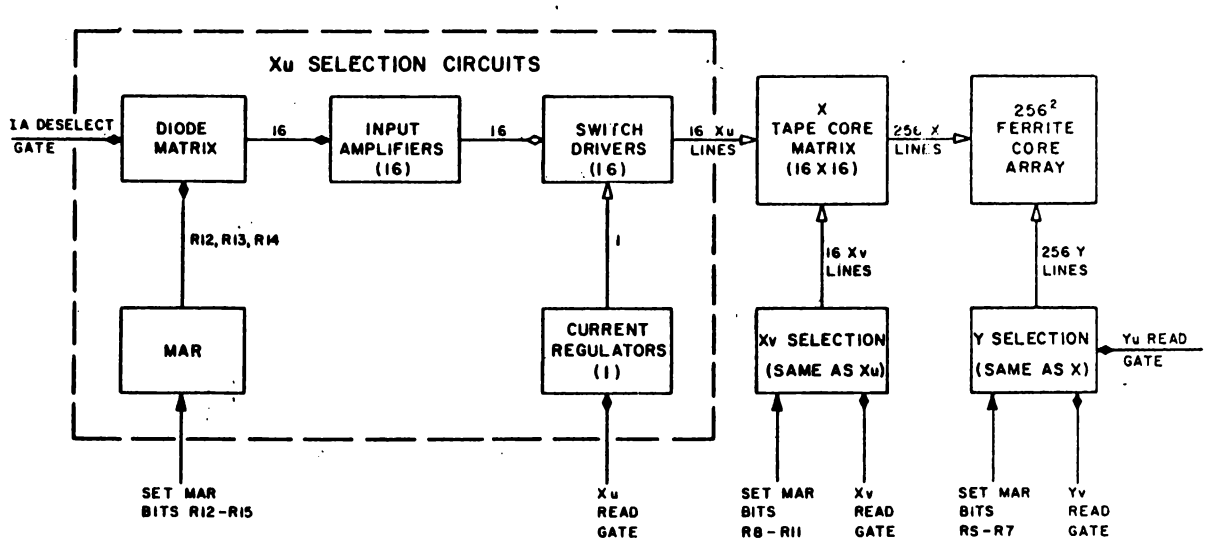
1. Function

a. Selects the correct X or Y drive line in the ferrite core array.

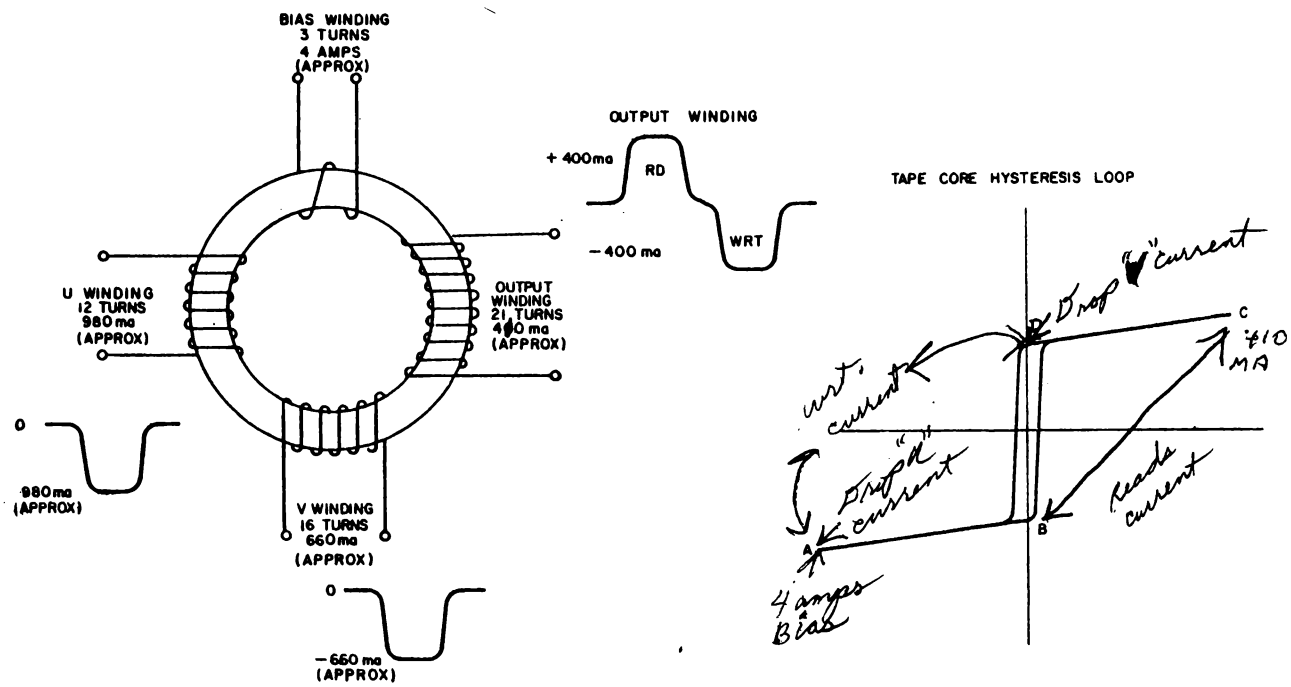
b. Supplies 400 ma of read and write current to the ferrite cores.

2. Basic Operation

a. Page 2170 shows the electrical characteristics of the tape core used in the tape core matrices. The U, V, and bias windings produce approximately equal applied



Memory Selection Circuits, Block Diagram

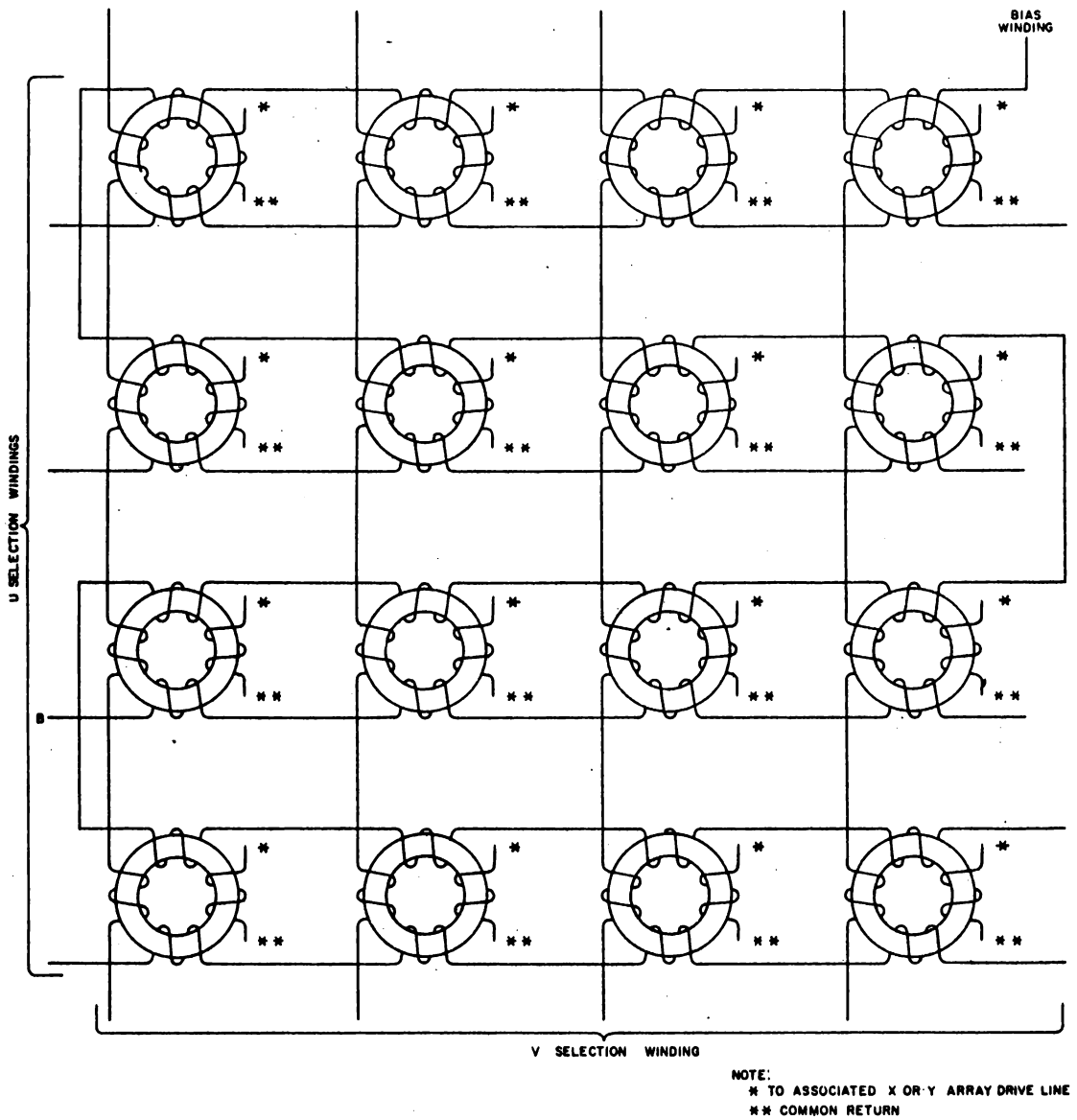


Tape Core Characteristics

fields; however, the windings are connected in such a manner that the bias field opposes the U and V fields. Under nonselected conditions, the U and V windings are not energized and the bias field will cause the core to settle at point A of the hysteresis loop. If a tape core is half selected, that is, if either the U or V windings is energized singly, the resultant field will cancel the bias field and the core will settle at point B. Since only a relatively small change in flux is produced, the output winding signal will be an early peaking positive pulse of approximately 40 ma at its peak. For half selected tape cores, a similar negative output signal is obtained when the U or V current pulse is terminated. If a tape core is fully selected, that is, if both the U and V windings are energized simultaneously, the resultant field will cause the core to switch to point C, producing a relatively large change in flux to yield approximately a 400-ma signal on the output winding. This signal is the read-current pulse used to half read select a ferrite core. When the U and V current pulses are terminated the bias field will cause the tape core to switch back to point A, again producing a relatively large change in flux to yield approximately a 400-ma signal on the output winding. This latter signal is the write-current pulse used to half write select a ferrite core.

b. Page ~~2190~~ 2690 shows the arrangement and connection of the tape cores to form a portion of the tape core matrix. As previously stated, only one U and V line can be energized at any one time; therefore, only the core at the intersection of the selected U and V line can be switched to produce read-write currents. Each tape core output winding is connected to one X or one Y winding; thus, only the selected array drive line will receive the required half-amplitude current required by the ferrite cores. The half-selected tape cores produce small noise pulses.

c. Since all four of the selection circuits groups are actuated by read gates at approximately the same time, current pulses will be applied to the selected U and V lines of each tape core matrix. At the point of coincidence, a tape core is selected in each matrix which, in turn, supplies the required coincident read-write current pulses to its associated X or U array drive line. Page 2200 , which constitutes the tape core matrix selection gridwork, identifies the array drive line (in physical and ocquad notation) associated with the output winding of each tape core. Since the ocquad address notation provides symmetry in specifying the selected X and Y drive lines, this table represents both the X and Y tape core



Tape Core Matrix, Schematic Diagram

X AND Y TAPE CORE MATRIX OUTPUT.

V (Octal)

U (Octal)	00	01	02	03	04	05	06	07	10	11	12	13	14	15	16	17
	0	4	8	12	16	20	24	28	32	36	40	44	48	52	56	60
00	000	040	100	140	200	240	300	340	400	440	500	540	600	640	700	740
	64	68	72	76	80	84	88	92	96	100	104	108	112	116	120	124
01	001	041	101	141	201	241	301	341	401	441	501	541	601	641	701	741
	128	132	136	140	144	148	152	156	160	164	168	172	176	180	184	188
02	002	042	102	142	202	242	302	342	402	442	502	542	602	642	702	742
	192	196	200	204	208	212	216	220	224	224	232	236	240	244	248	252
03	003	043	103	143	203	243	303	343	403	443	503	543	603	643	703	743
	1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61
04	010	050	110	150	210	250	310	350	410	450	510	550	610	650	710	750
	65	69	73	77	81	85	89	93	97	101	105	109	113	117	121	125
05	001	051	111	151	211	251	311	351	411	451	511	551	611	651	711	751
	129	133	137	141	145	149	153	157	161	165	169	173	177	181	185	189
06	012	052	112	152	212	252	312	352	412	452	512	552	612	652	712	752
	193	197	201	205	209	213	217	221	225	229	233	237	241	245	249	253
07	013	053	113	153	213	253	313	353	413	453	513	553	613	653	713	753
	2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62
10	020	060	120	160	220	260	320	360	420	460	520	560	620	660	720	760
	66	70	74	78	82	86	90	94	98	102	106	110	114	118	122	126
11	021	061	121	161	221	261	321	361	421	461	521	561	621	661	721	761
	130	134	138	142	146	150	154	158	162	166	170	174	178	182	186	190
12	022	062	122	162	222	262	322	362	422	462	522	562	622	662	722	762
	194	198	202	206	210	214	218	222	226	230	234	238	242	246	250	254
13	023	063	123	163	223	263	323	363	423	463	523	563	623	663	723	763
	3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63
14	030	070	130	170	230	270	330	370	430	470	530	570	630	670	730	770
	67	71	75	79	83	87	91	95	99	103	107	111	115	119	123	127
15	031	071	131	171	231	271	331	371	431	471	531	571	631	671	731	771
	131	135	139	143	147	151	155	159	163	167	171	175	179	183	187	191
16	032	072	132	172	232	272	332	372	432	472	532	572	632	672	732	772
	195	199	203	207	211	215	219	223	227	231	235	239	243	247	251	255
17	033	073	133	173	233	273	333	373	433	473	533	573	633	673	733	773

Drive line # octal-guard numbers

matrices. As noted in the table, the 2-digit octal numbers in the leftmost column specify the U input lines, and the 2-digit octal numbers in the topmost row specify the V input lines. During memory operation, the tape core at the intersection of the selected U and V lines will generate the required read-write current pulses. The individual tape core output windings are connected to the array X or Y drive lines as shown by the identification numbers contained in each box. The upper number in each box specifies the physical X or Y drive line, and the lower number, which is obtained by regrouping the combined binary equivalent of the selected U and V lines, designates the ocquad coding of that line.

3. Detailed Operation

a. All tape cores have 4 amps (nominal) bias current applied at all times. This gives a net force of 12 N I (Ampere Turns) which places the core at A on the hysteresis loop.

b. Switching a Tape Core

1) First apply 610 ma. (nominal) drive current on 16 turn V winding. This gives 12 N I which oppose the Bias bringing the core to point B on the hysteresis loop.

2) Second apply 980 ma (nominal) drive current on 12 turn U winding. This gives 12 N I which will switch the tape core inducing read current in the output winding. With V and U both supplying current, tape core will be at point C on the hysteresis loop.

SEL. CORE 410 MA

3) Write current is supplied by:

a) First removing V current allowing tape core to go to point D on hysteresis loop.

b) Second removing U current allowing bias current to switch the tape core back to point A. This induces a current of equal magnitude but of opposite polarity to Read current.

c. Tape Core Half-Selections

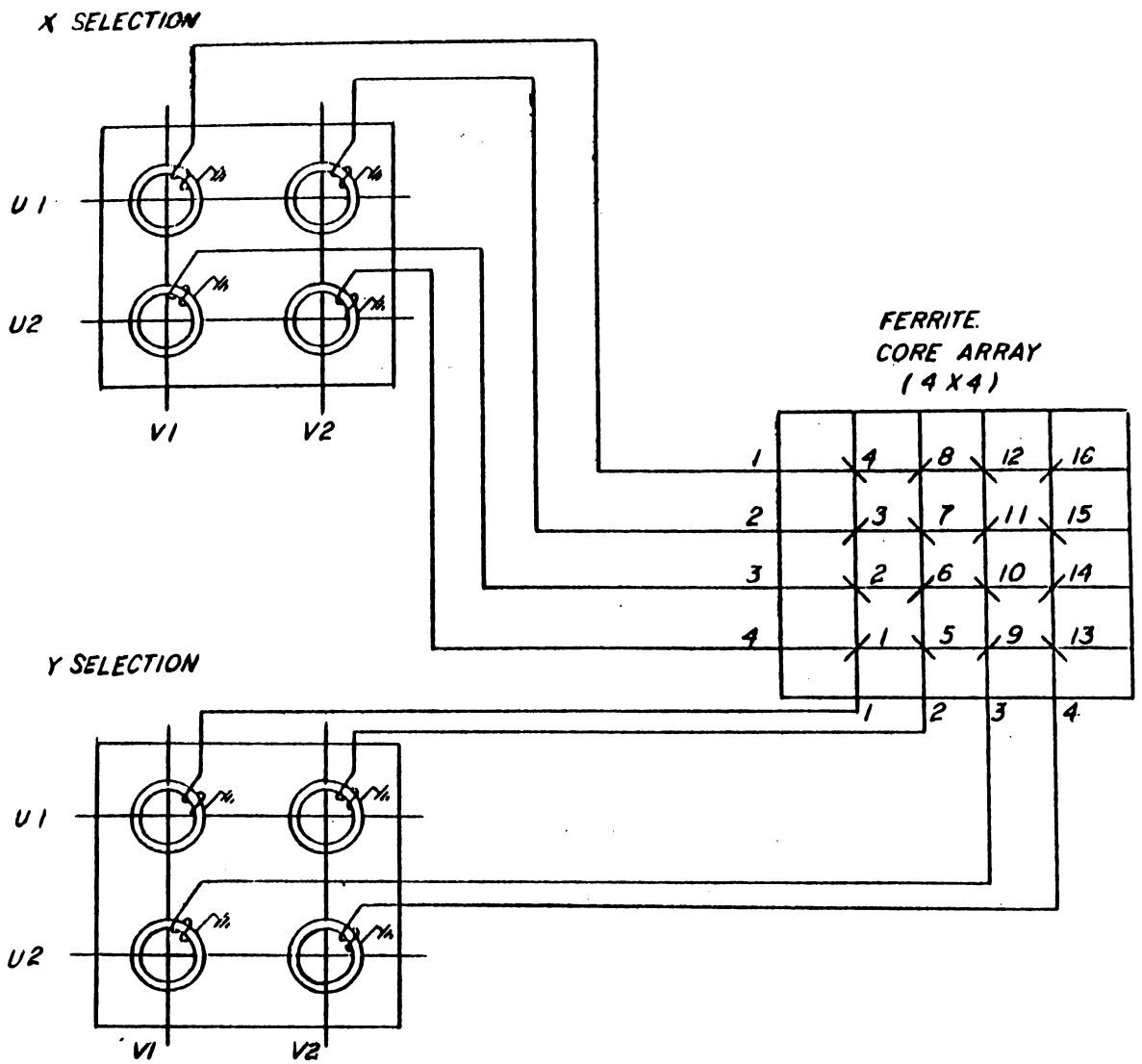
1) Consider the case where X ul and X vl are supplied current.

Refer to Page 2170

a) Tape core 1 is fully switched inducing read current in X line 1.

b) Tape cores 2 and 3 are half switched inducing half selections in X lines 2 & 3.

c) Tape core 4 remains unchanged.


X SELECTION
U1
U2
V1
V2
FERRITE
CORE ARRAY
(4X4)
1
2
3
4
4
8
12
16
3
7
11
15
2
6
10
14
1
5
9
13
1
2
3
4
Y SELECTION
U1
U2
V1
V2

2130

2. Consider what is happening in the array.

   a. Assume full read current is supplied to X line 1 and Y line 2.

      (1) Ferrite core #8 will be switched to a "0".

      (2) Ferrite cores #4, 12, 16, 5, 6, 7, will be half switched.

   b. Half selects will be felt on the following ferrite cores.

      (1) V half selects

         (a) X line 3 - cores 2, 6, 10, 14

         (b) Y line 4 - cores 13, 14, 15, 16

      (2) U half selects

         (a) X line 2 - cores 3, 7, 11, 15

         (b) Y line 1 - cores 1, 2, 3, 4

   c. Areas where half-selects can be a problem.

      (1) Wherever a half select tape core output adds on to a ferrite core which has half read current applied.

         (a) Ferrite cores 4, 12 and 16 have half read current applied on X line 1.

         (b) Core 16 has a tape core V-half select from Y line 4.

         (c) Core 4 has a tape core U-half select from y line 1.

      (2) Summarizing

         (a) Cores 6 and 16 have half read current plus V-half selects.

         (b) Cores 4 and 7 have half read current plus U-half selects.

   d. Solution to half-select problem.

      (1) V-current is turned on .2 micro-seconds before U thereby allowing V-half selects to die away before read current is applied.

(2) The time duration of U-half selects is minimized thereby allowing these to die away before 400 mils of read current is reached.

BFN
4 AMPS

G. Bias Fixing Network

1. Purpose

a. Provides a constant current thru the bias winds of the 16 x 16 tape core matrix.

2. Basic Operation

a. Four transistors are used to supply and regulate the four amps of current to the bias winding of the tape cores. Refer to Page 2250

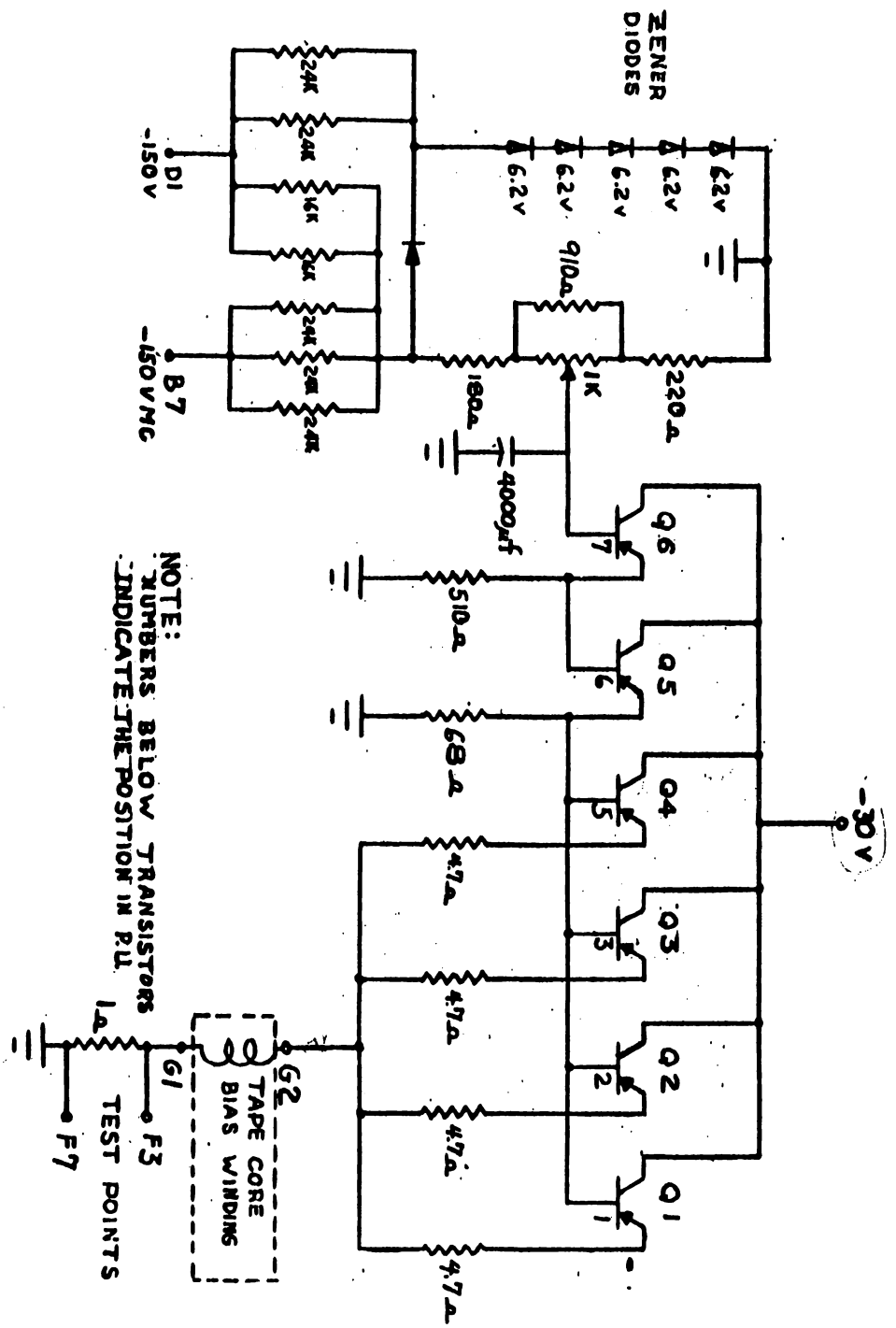
b. Two emitter followers are used to isolate the current adjustment circuit from the large base currents that are drawn from the regulator transistors.

3. Detailed Operation

a. The voltage divider network was designed to keep a constant voltage across the three resistors and the pot unless margins are applied. It was found that margins would not predict circuit failure so margins are no longer applied to this circuit. The five zener diodes will keep a constant -31V on the left side of the Y diode. The voltage divider to the right of the Y diode would cause -27V to be present below the 180 Ω resistor if the Y diode was not in the circuit. The -27V on the right side of the Y diode will cause it to conduct. When the Y diode starts to conduct the right end of the Y diode will go to a voltage slightly more positive than -31V. The voltage spread across the pot will be about -7 to -24.7. This pot will be adjusted for 4 amps of current thru the bias winding. After the pot has been adjusted for correct current thru the winding, the large capacitor connected to the wiper arm of the pot will hold the voltage constant when fast changes in base current of Q6 occur.

b. The two emmiter followers Q5 & Q6 are used to isolate the large base currents of Q1 thru Q4 from the voltage divider network. Q6 will have small base current due to the large emitter resistor. More base current will flow in the Q5 transistor due to the smaller emitter resistor. Very large base current will flow in Q1 thru Q4. By changing the setting of the pot, the bias can be changed on Q1 thru Q4.

BFN



BIAS FIXING NETWORK

2160

c. Q1 thru Q4 are used to adjust and regulate the current thru the bias winding. This current will be held constant if the -30V power supply voltage varies or if a current is induced into the bias winding from the tape core switching. The power transistors used in this circuit require a large back bias for cutoff. In normal operation the emitter is about -15 volts and the base is about -19V. If the current thru the bias winding increases, more voltage will be dropped across the 4.7 resistors. This will cause a more negative potential to be applied to the emitters of Q1 thru Q4. This decrease in forward bias will result in a decrease in conduction, returning the current to the correct value. An increase in current can be caused by changes in the -30V supply or by a tape core switching which will induce a current into the bias winding.

d. Test points F3 and F7 are used when adjusting the potentiometer for the desired current. The pot will be adjusted for 4 volts between the test points.

H. Sense Amplifier Model C

5A

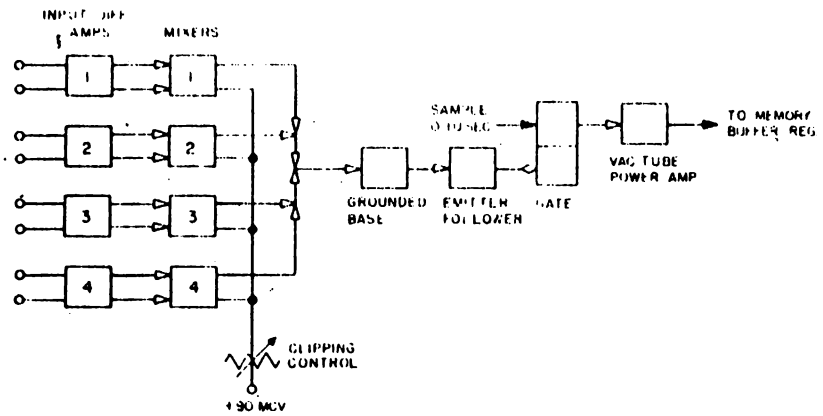
1. Purpose

a. When a 1 is read out of the memory cores by a reversal of their magnetization, voltages are induced in the sense windings of the cores. The sense amplifier discriminates between these signal voltages and the inherent noise voltages and amplifies the signals. These signal voltages are then used to condition a gate circuit which passes a sample pulse and sets a flip-flop in the memory buffer register.

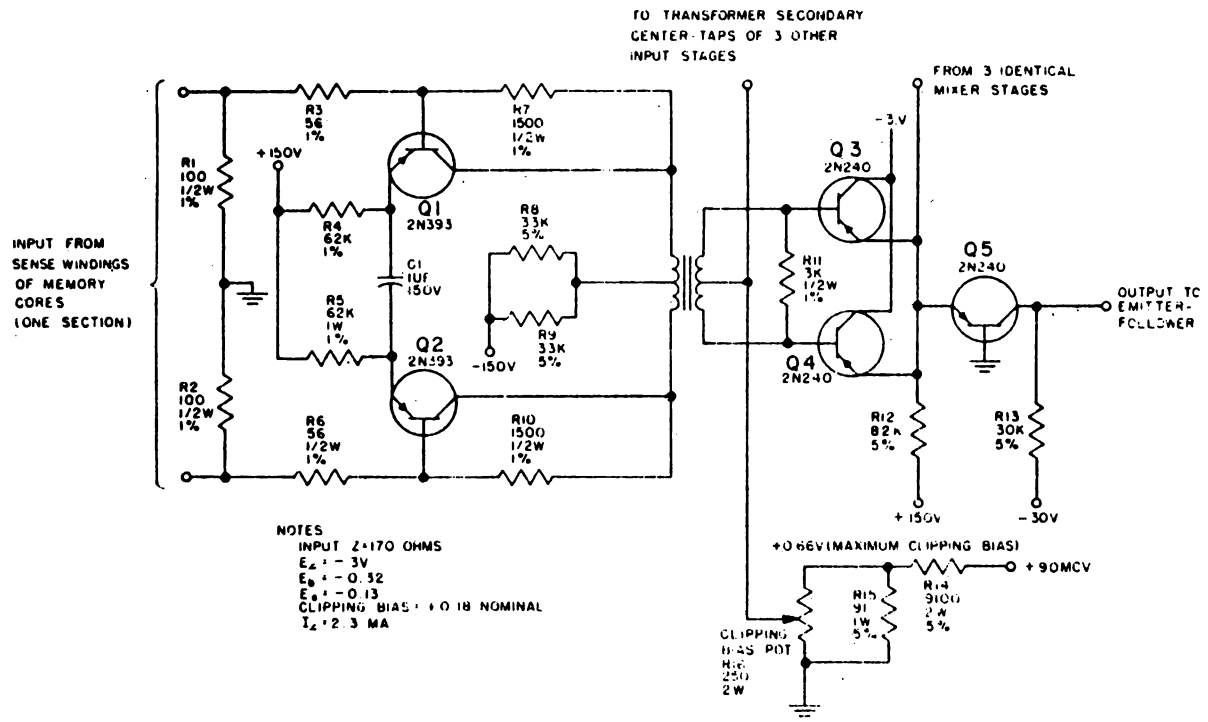
b. The programming requirements for the AN/FSQ-7 led to the development of a core memory plane with 256^2 addresses. The output of this expanded memory plane is only one-half the amplitude of that of the 64^2 memory plane, with no decrease in noise level. The model C sense amplifier was designed to provide the additional selectivity and compactness required with the 256^2 core memory plane.

2. Basic Operation

The model C sense amplifier is a logic element which functions as a voltage amplifier and a gate circuit. The block diagram of the sense amplifier, page 2270, is the circuit diagram for one difference input amplifier stage and associated mixer. Four identical difference amplifiers are at the input, one for each of the four sense sections in a memory plane. Each consists of two transistors which produce an output only when a difference signal (voltages of opposite polarity) is applied at their input.



SENSE AMPLIFIER, MODEL C, BLOCK DIAGRAM



DIFFERENCE INPUT AMPLIFIER WITH FEEDBACK

Common mode disturbances (noise pulses of equal amplitude and polarity) cancel each other out. For a given memory address, only one of the four sense sections in a plane may provide a 1 signal to an associated difference amplifier. This is a pulse voltage approximately 1 usec wide at the base and 40 to 100 millivolts (mv) in amplitude. Each amplifier is followed by a mixer and the outputs of all four mixers are connected in parallel into a grounded base amplifier. Regardless of the polarity of the amplified difference signal, the mixer supplies a negative pulse to the grounded base amplifier, which then goes to an emitter follower. The operation of the grounded base amplifier and emitter follower is analogous to that of a grounded grid amplifier and a cathode follower, respectively. The amplified 1 signal from the emitter follower conditions a gate circuit. The conditioned gate passes a 0.1-usec sampling pulse. The final stage of the sense amplifier is a vacuum tube pulse amplifier that supplies the 20-volt power pulse required to drive the coaxial cable between the memory units and the memory buffer register.

3. Detailed Operation

a. The difference amplifiers page 2270 (Q1 and Q2) are operating class A. Before a signal is applied from the sense winding, both transistors are operating near a mid point between saturation and cutoff. This is made possible by selecting the correct size components between -150V and +150V. The bias for Q1 and Q2 will be developed across R7 and R10. R1 and R2 are used as termination resistors for the sense winding. R 3 and R 6 are base current limiting resistors. When a voltage is induced into the sense winding due to a core switching from a one to a zero, one end of the winding goes negative and the other goes positive. The positive end of the winding will cause the transistor that is connected to that end to decrease conduction. The negative end of the winding will cause the transistor that is connected to that end to increase conduction. Assume that the base of Q1 goes positive and the base of Q2 goes negative. Q1 will decrease conduction and Q2 will increase conduction. The decrease in collector current from Q1 will cause the top of the primary of the transformer will go negative. The increase in collector current from Q2 will cause the bottom end of the primary to go positive. This change in primary voltage will cause a voltage to be induced into the secondary winding of the transformer.

The capacitor C1 will maintain a constant voltage at the emitters of the two transistors. The capacitor is large enough so that it will not charge appreciably during the time a signal is applied to the transistors. This will increase the gain of the amplifier when a difference signal is present.

Large currents in the X and Y drive lines causes voltages to be induced into the sense winding that are in phase at the two ends of the sense winding. This is called common mode noise and can approach 10 volts in amplitude. The sense amplifier has been designed to completely cancel this noise. When both Q1 and Q2 bases go positive at the same time, the gain will be less than unity due to the change in emitter voltage that follows the change in base voltage. The capacitor C1 will not be charging or discharging because both plates will be going positive at the same rate. The current increase thru the two transistors will be equal. This will cause no voltage to be induced into the secondary winding of the transformer. Therefore, any common mode noise will be canceled.

b. The mixer stage is biased by the clipping bias pot. Both Q3 and Q4 will be cut off. The emitters are near ground potential due to the conduction of Q5. When a signal is induced into the secondary winding of the transformer, one of the mixer transistors will be driven further from cutoff by the positive end of the secondary and the other one will be driven into saturation by the negative end. When either Q3 or Q4 starts to conduct, additional current flows thru the R12 resistor. This will cause the emitter of Q5 to go negative, which will turn Q5 off. The collector of Q5 will be a negative square wave during the time that either Q3 or Q4 are conducting.

c. Transistor Q6 is an emitter follower that is used to match impedance between the grounded base amplifier and the gate circuit. Refer to Page 2300

d. The level from the emitter follower is used to condition the gate circuit. Before a signal is applied to the gate, Q7 and Q8 are biased cutoff. When a negative signal is applied to the base of either transistors, current will not flow thru the primary of the pulse transformer until a negative signal is applied to both transistor bases at the same time. Current thru the primary of the pulse transformer will cause a large positive pulse to be applied to the grid of the pulse amplifier Y1.

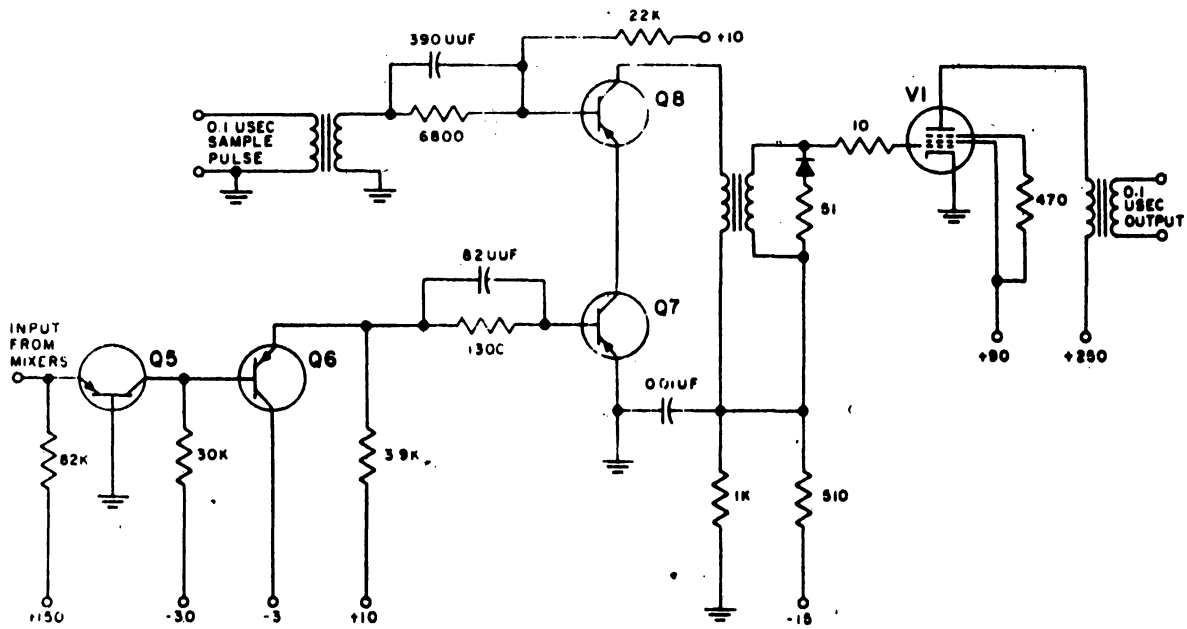
e. The pulse amplifier is the same as that used throughout the computer.

I. Digit Plane Driver

ADDD

1. Purpose

a. The digit plane driver, model C, supplies a current pulse, known as inhibit current, of approximately 2.2 usec and



AMPLIFIERS AND GATE CIRCUIT

370-430 ma to one-fourth of the digit plane windings of a 256^2 ferrite core memory plane. The inhibit current maintains a condition in those cores that had contained 0's readout by opposing the write-current pulse, thus preventing the writing of 1's into these particular cores.

b. Four DPD's are used for each of the 33 ferrite core planes, or a total of 132 DPD's for the 256^2 memory system.

2. Basic Operation

a. The digit plane driver, model C, consists of a feedback amplifier, a cathode follower and a driver. The amplifier provides the voltage swing necessary to turn the 5998 driver on and off. The cathode follower improves the fall time of the negative output and also supplies the grid current required by the 5998. The input to the amplifier is the difference between a 2.2-usec, -30V pulse and a feedback voltage obtained from the driver output. The output current amplitude can be varied. Refer to Page 2320

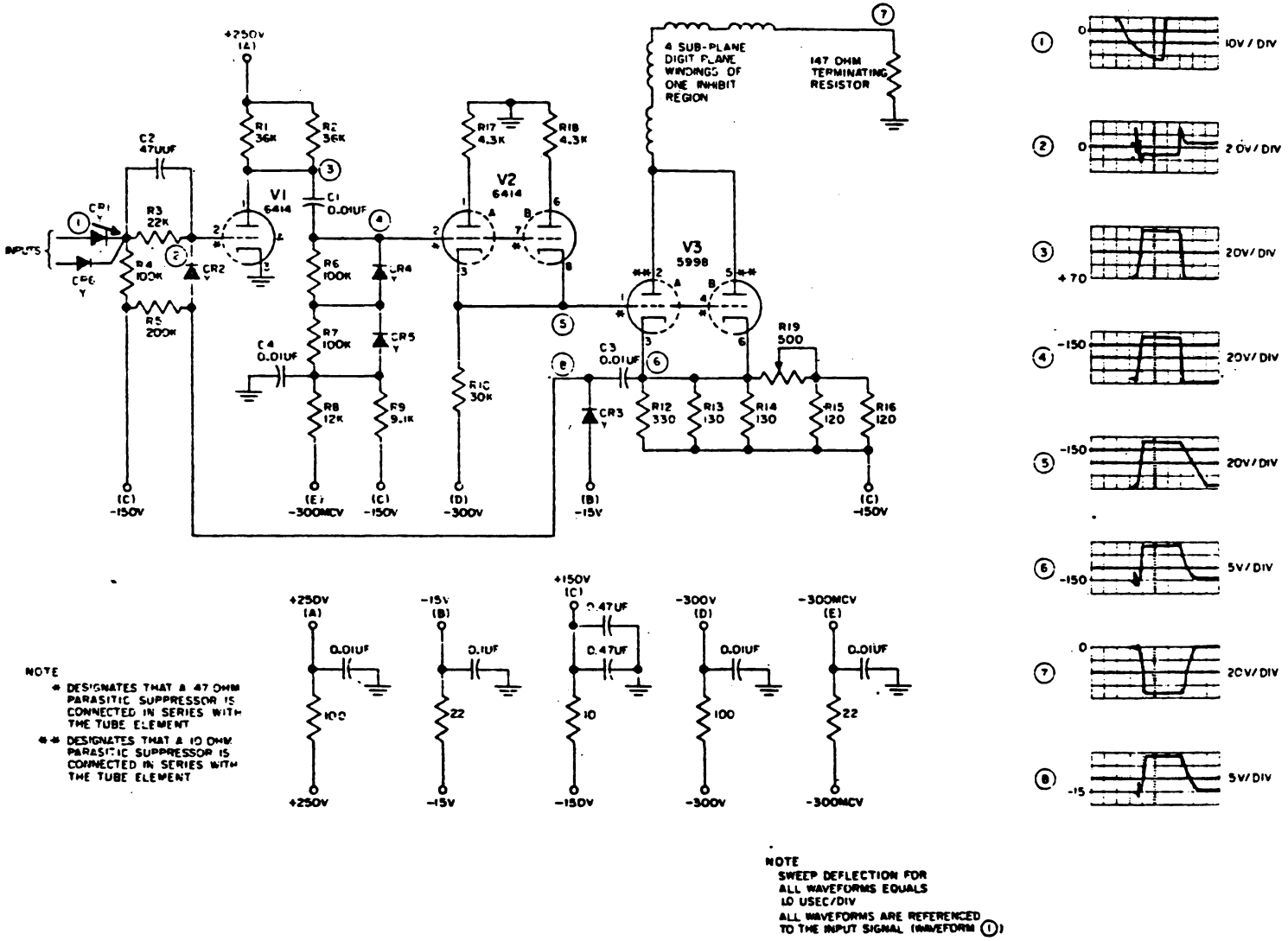
b. The digit plane driver circuit operates only when an inhibit current is needed to prevent the writing of a 1 into a memory core (thus storing a 0). The inputs to the -AND circuit are a 2.2-usec, -30V pulse from the inhibit gate generator and a -30V level from the 1 side of one of the flip-flops in the memory buffer register.

3. Detailed Operation

a. The input -ξ circuit, CR1, CR6 and R4 will keep a $\not$10V level on the left end of R3 while either input is $\not$10V. The grid current from V1 thru R3 will cause the grid to be slightly more positive than ground. The charge on capacitor C2 will be equal to the voltage drop across R3 or $\not$10V. Current will be flowing from -150V thru R5 and CR3 to -15V. This will clamp the plate of CR2 to -15V. CR2 will be cut off due to the 15V back bias. The plate of V1 is $\not$70V due to the near ground potential on the grid.

b. The grid of V 2 is clamped to -215V by voltage divider R8 and R9. V2 will be conducting and the grid current will be flowing thru the forward resistance of CR4 and CR5. The cathodes of V2 will be slightly more positive than the grids, or -212V. This is applied to the grids of V3.

c. V3 cathodes will be at -150 when the grids are at -212V. V3 will be cut off.



NOTE

* DESIGNATES THAT A 47 OHM PARASITIC SUPPRESSOR IS CONNECTED IN SERIES WITH THE TUBE ELEMENT

** DESIGNATES THAT A 10 OHM PARASITIC SUPPRESSOR IS CONNECTED IN SERIES WITH THE TUBE ELEMENT

NOTE

SWEEP DEFLECTION FOR ALL WAVEFORMS EQUALS 10 USEC/DIV

ALL WAVEFORMS ARE REFERENCED TO THE INPUT SIGNAL (WAVEFORM ①)

DIGIT PLANE DRIVER, MODEL C, SCHEMATIC DIAGRAM

3220

d. When a negative signal is applied to both inputs to the -ξ circuit, the right end of the diodes will go negative at an exponiental rate determined by the size of C2 and R3. The right side of R3 will try to go to -10V due to the 10V charge on C2. This causes V1 to start toward cutoff, but as the plate goes positive the change will be applied to V3 thru the cathode followers. This causes a 13V volt positive change to be applied to the right side of capacitor C3. This causes the left side of the capacitor to go positive by the same amount. The left side of capacitor C3 was -15V prior to the time the signal was applied. +13V added to this will be -2V. This is the voltage that will now be applied to the plate of CR-2. The cathode cannot be much more negative than the plate, so the grid of V1 will be near -2. This will not completely cut off V1. The plate voltage will now be about +140V.

e. The +70V change on the plate of V9 will be coupled thru capacitor C1 to the grid of V2. The cathode of V2 will go positive at the same rate. The positive change on the grid of V3 will cause it to conduct. 460 ma will flow thru the cathode resistors. 440 of this will flow thru the digit plane winding. The remaining 20 ma will be grid current.

f. The output current can be adjusted from 330 ma to 440 ma.

g. When either of the two inputs to the -ξ goes positive, the capacitor C2 will couple this change to the grid of V1. As the plate goes negative, the capacitor C1 will discharge thru the forward resistance of CR4 and CR5. Resistors R6 and R7 equalize the voltage across the diodes.

h. The resistors and capacitors below the schematic on page 2320 are decoupling circuits in the different voltage lines.

Core Storage Element

2240

J. Summary Questions:

1. Diode Matrix Decoder

   a. The DMD is made up of _____ circuits.

   b. The DMD conditions _____.

   c. The input to the DMD's are from _____.

   d. A selected output line is _____ volts.

   e. The IA deselect FF controls the fifth line into the - circuit for address line number _____.

   f. The IA deselect FF is necessary due to the _____ _____ in the IA's.

2. Input Amplifier

   a. This circuit is used as an _____, _____ and _____ _____.

   b. The input is from the _____ circuit.

   c. When the input to the circuit is /10 the output is _____.

   d. When the input to the circuit is -30 the output is _____.

   e. CR5 and CR6 are used as a _____ _____path for C3.

3. Switch Driver

   a. The switch driver inputs are from an _____ and a _____.

   b. This circuit is used to switch _____ from one tape core drive line to another.

   c. The amount of current thru the SWD will be controlled by the _____.

2250

d. One SWD supplies current to _____ CCD's.

e. The pulse shaping network is used to compensate for the _____ of the tape core drive winding.

4. Current Regulator

a. This circuit is used to convert a _____ pulse to a _____ pulse.

b. The conditioning level is supplied by the _____FF.

c. One SWD supplies drive current to _____ tape cores.

d. The Zener diode (CR509) is used to keep a constant _____ on V4, V5 and V6.

e. By increasing the capacitance at H5, V2A will be turned off _____ V2B is turned off.

f. Adding capacitance between J3 and J6 will cause the top of the current pulse to increase at a _____ rate.

g. The pulse slope is used to keep the current thru the drive line _____.

5. Tape Core Matrix

a. U currents and V currents are applied to the matrix at different times to decrease the affects of _____ _____ noise on the ferrite cores.

b. The switching of a tape core is accomplished during read time with the _____ winding.

c. The _____ winding overcomes the effect of the bias current.

d. The number of U windings was decreased from 16 to 12 to _____ the rise time of the current pulse.

e. One tape core that will not switch will cause _____ memory addresses to fail.

6. Bias Fixing Network

a. Develops the driving force to cause _____current when U and V drives are removed.

b. The value of current delivered by the BFN is _____ amps.

c. The two emitter followers are used to _____ the large base current of Q1 thru Q4 from the voltage divider network.

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d. The pot is adjusted for _____ volts from F3 to F7.

7. Sense Amplifier

a. This circuit is designed to _____ one signals from ferrite cores.

b. This circuit amplifies a one signal from either a _____ or a _____ core.

c. The difference amplifiers are operating class _____.

d. The mixer stage is sensitive to either a _____ or a _____ output from the difference amplifier.

e. The mixer stage is biased by the clipping level pot to prevent _____ bits or _____ from conditioning the gate circuit.

f. Q7 and Q8 make up the _____ circuit.

8. Digit Plane Dirver

a. This circuit supplies _____ ma of current to ferrite cores in the _____. direction during _____ time.

b. The DPD prevents the writing of _____ into ferrite cores.

c. CR1 and CR6 are used as a _____ circuit.

d. R8 and R9 are used to develope the _____ voltage for V2.

e. One DPD supplies current to _____ sub planes.

XX. 256^2 Logic Analysis

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A. Logic 0-2.1.4

1. TP-0 MAR F-F Loading

   a. From Address Reg. - Logic 0.4.1 IP-0 OT gated pulse to transfer Address Reg. to MAR #1 C/D Zones 14 thru 7.
   b. From I/O Address Reg. - Logic 0.4.1 (Zone 4E) 6GD F1- pulse from 0.2.3 6DD (k7) 1, (Zone 4E) TP-0 Gated by Write FF on, or Read FF on.
   c. From Program Cntr. - Logic 0.4.1 (Zone 4-1C) gated IP-O, PT (Zone A5) pulse into 6GEH3 out H7 to transfer P.C. to OR circuits in Address Reg. to MAR.

2. TP-O + approximately .5 microseconds - Start Memory

   a. Set "V" Read Gate Generators. Logic 0.2.1.4 (Zone 11C) 67AG and (Zone 6C) 65 EG - 30 volts is thus applied to the X and Y "V" CR's so that the SWD which was grid conditioned by the IA will now supply X & Y "V" current to the CCD's.

3. Start Memory + .2 microseconds.

   a. Set "U" Read Gate Generators. Logic 0.2.1.4 (Zones 11 A-C and 7C). The X and Y "U" CR's are conditioned as with the "V" above, and the fully selected CCD's, (two-one for X and one for Y), will develop READ current in a Ferrite core address.

4. Start Memory + 1.9 microseconds - "SAMPLE"

   a. Eight sample pulses to sense amplifiers started by pulse from MPD #1, Logic 0,2.1.4 (Zone 11A) out of Sample Gate Generator (Zone 10C) thru progressive delays.
   b. These samples are approximately .04 microseconds apart are introduced into the S.A. circuitry on Logic 0.2.1.6 (Left Side) where they strobe transistorized gate tubes.

      1) #1 Parity thru L3
      2) #2 L4 thru L7
      3) #3 L8 thru L11
      4) #4 L12 thru L15
      5) #5 RS thru R3
      6) #6 R4 thru R7
      7) #7 R8 thru R11
      8) #8 R12 thru R15

c. As a result of Read current, the S.A., detecting a "1" bit in the selected ferrite core, will set the corresponding Memory Buffer FF.

5. Start Memory + 2 usec. - CLR Read V

   a. Pulse out of MPD #1 Logic 0. 2. 1. 4 (Zone 10A) to clear Yv RGG 67 AG (Zone 11C) and 65 EG (Zone 6C).
   b. This allows fully selected CCD to return to zero NI state.

6. Start Memory + 2. 4 usec. - Set Inhibit Left Word

   a. Pulse from MPD #2 Logic 0. 2. 1. 4 (Zone 9A) to DPD Selection Gates (Zone 9-8C) to Inhibit Gate Generators (Zone 9-8D) as gated by Bits R14, 15 from the MAR.

7. Start Memory + 2. 6 usec - Set Inhibit Right Word

   a. Pulse from MPD #2 to DPD Selection Gates Logic 0. 2. 1. 4 (Zone 4-3C).

8. Start Memory + 2. 6 usecs - Clear Read U

   a. Pulse from MPD #2 Logic 0. 2. 1. 4 (Zone 9A) to Yu R. G. G. (Zone 11C) 67 AG, and Xu RGG (Zone 6C) 65 EG.
   b. This is negative logic since setting the U RGG's causes the removal of all selection current on the CCD's and permits bias current to reinstate the fully selected CCD to the quiescent state and in the process producing a WRITE current on the coincident lines in the ferrite core array.

9. Start Memory + 3. 1 usec. Clear MAR (to 1's) IA deselect, and Sample Gate Generator

   a. Logic 0. 2. 1. 4 (Zone 9B) 65AK B1 to 65 AG & 65 AH (Zone 14B); to 65 AM A3 (Zone 10C).

10. Start Memory + 4. 4 usecs - Clear Inhibit Left

    a. Logic 0. 2. 1. 4 (Zone 8A) clear inhibit left pulse to clear inhibit gate generators (Zone 9-8D) thereby turning off DPD's for left word, Logic 0. 2. 1. 6.

11. Start Memory + 4. 5 usecs. - Clear Inhibit Right

    a. Logic 0. 2. 1. 4 (Zone 8A) clear inhibit right pulse to clear inhibit gate generators (Zone 4. 3D) thereby turning off DPD's for the Right Word, Logic 0. 2. 1. 6.

Note: The following is the Time Sequence and Affected Logic with Memory I not selected.

12. TP-0 - Delayed

a. Load MAR F-F's, Logic 0. 4. 1 - similar with cases under Part II A except with LS of Address Register set indicating Memory II. A pulse from Logic 0. 4. 1, 4 EP H7, (Zone 13B) strobes transfer gates.
b. TP-0 Set IA Deselect F-F Logic 0. 2. 1. 5 (Zone 11E).
c. TP-0 Into Clock IV Logic 0. 2. 1. 4 (Zone 12B) and out 67AJC1 after 1. 5 usec. delay.

13. TP-0 + 1. 5

Logic 0. 2. 1. 4 (Zone 9A) - pulse into 65 AKC5 and out 65 AKB1 to Clear MAR, IA Deselect F-F, and Sample Gate Generator FF.

B. Logic 0-2. 1. 5 (1 & 2)

1. Familiarization

a. MAR & PCA (16A-E)
b. -AND Circuits (15A-E)
c. IA Deselect FF (14E)
d. IA's (15A-E)
e. SWD's (u & v) (12A-E) (11-6A)
f. BFN (12A)
g. CR's (u & v) (13A and 5A)

Note: Jumper B1 to B2 uCR
Tilt & Padding on uCR

h. Tape core assemblies
i. Damping Resistors for SWD's, 500 ohms, located between two bus bars close to output of SWD's on logic.
j. Pulse Shaping Network

1) u - 5B
2) v - 5E

k. Chokes for BFN (5D & 11A) (Physical location in center of Unit 66)

l. -48v Interlock (5E) (P.U.'s must be plugged in to bring up D. C.)

m. Explanation chart on tape core Plug Pins. (Middle of Matrix.)

Note: Chart is for output winding connection to parity plane. (Input shown on logic).

P. U. Pin

66	D	B	4	D	KK
Unit	Panel	Row	Tape Core P.Unit	Conn. or Plug	Pin of Conn.

Plane Pin

66	D	D	1	0
Unit	Panel	Row	Section or Subplane of Panel L to R facing panel (1,2,3,4)	Subplane Pin 0-63 L-R

n. Point to point wiring of CR's Charts II and III.

o. Chart I for BFN choke wiring.

p. Connectors between Unit 65 (SWD's) and Unit 66 are shown on Page 1820. (Mounted on top of Unit 66)

C. Logic 0.2.1.6

1. SA's

a. Sample Delays
b. Left Word Chart
c. Right Word Chart
d. Input from Array
e. Output to MEM Buffer

2. DPD's

a. Inputs from IGG's
b. Each PU has two DPD's
c. Explain Charts
d. Output to Array

D. Logic 0.2.1.7

1. Sheet #1 used for determining X and Y drive line connections to specific planes as well as sense winding output connections.

2. Sheet #2 used for determining CCD, plane and termination resistor locations within the 256^2 Array.

E. Summary Questions:

1. GT2, 65 AH Logic 0-2.1.4. C 5 will not pass a pulse. How many memory addresses will fail if all zeros are written into and read from memory?

2. 65BUG1 0-2.1.5. E14 is open. Which addresses cannot be selected in memory?

3. List the P.U. pins where the drive lines leave the tape core matrices for each of the following addresses:

   a. 0.00137
   b. 1.04160
   c. 1.76341
   d. 0.73155
   e. 0.42032

4. Output winding of the Tape Core for Xu = 1110 and Xv = 0010 is open. After the following program halts, what are the contents of the accumulator?

1.23454	CAD	1.23455
1.23455	ADD	1.23456
1.23456	ADD	1.23457
1.23457	HLT	1.23460

   A. 0.00000 1.72616
   B. 0.02100 1.72616
   C. 0.00000 0.00000
   D. 0.02100 0.47136
   E. 0.01040 1.23456

XXI. 256^2 Memory Diagnostic Techniques

A. Introduction

1. The 256^2 memory is larger and more complex than its predecessor, the 64^2 memory. Because of these considerations a malfunction, when it occurs, requires a more constructive approach to effectively isolate the malfunction.

2. An important prerequisite for effective 256^2 memory maintenance is knowledge of the equipment's operational characteristics. In this respect it differs little from the basic maintenance requirements for any piece of electronic gear, however, it cannot be too strongly emphasized with regard to this equipment. It will be assumed, throughout this section, that the reader is thoroughly familiar with the theory of operation, including the logic, and individual circuit characteristics. Margins and the effect of these margins on the applicable circuits and on the overall system are analyzed in this section.

3. As with other areas of the Central Computer, the initial approach to 256^2 memory maintenance is with maintenance programs. The program, CKA BIG MEM 01, developed for the 256^2 memory, differs from others in that it provides error indications in a form that lends itself readily to a more complete evaluation of the trouble area. The method employed for this process is data reduction, which is a compact printout designed to show the number of errors encountered in the pertinent areas of the 256^2 memory while running the various program test routines such as 1's and 0's discrimination, addressing, checkerboard, etc. From this information an interpretation is possible that permits the malfunction to be isolated to a specific area of the equipment. Thereafter, conventional maintenance techniques should suffice in correcting the deficiency.

NOTE

Data reduction is favored over straight line print for most diagnostic procedures because of the time factor involved. This is due to the fact that to indicate the maximum of $'200,000_8$ errors with a straight line print using the 150 line-per-minute printer would require in excess of 7 hours. Data reduction, by comparison, prints $200,00_8$ errors in less than 4 minutes. For a small number of errors the program does permit, through the proper selection of SENSE switches, use of either straight line or data reduction print. Refer to the program writeup for details.

4. The diagnostic philosophy for the 256² memory, therefore, entails a thorough knowledge of the equipment's operation in order to best interpret the results obtained with data reduction, as the two are inseparable. In addition, the program CKA BIG MEM 1 must be completely understood so that the tests and options provided therein can be used to the greatest advantage in achieving the flexibility desired for evaluating and tracking down any particular malfunction indication. This latter fact is so important that the program tests and options are individually analyzed in this section.

B. CKA BIG MEM 1 Explanation

1. This program was designed to be a Reliability. Marginal and tuning program for the 256² memory.

2. Program Loading Using Big Memory

   a. Place the MEMORY NORMAL-REVERSE switch in the NORMAL position.

   b. Place the M.C. System in CALCULATOR mode.

   c. Place a DCS printer board into the line printer.

   d. Place BPX 2.00000 into the A switches (1.05100 0.00000).

   e. Place the TEST MEMORY switch to ASSIGNED.

   f. Place the program deck into the card reader hopper. The deck consists of 203 cards (000-202) not counting the MC data cards.

   g. Depress the MASTER RESET and LOAD FROM CARD READER push buttons.

3. Program Loading Using Little Memory

   a. Repeat steps a, b, c and d above.

   b. Place TEST MEMORY switch to UNASSIGNED.

   c. Place the BIG MEMORY TEST MEMORY plugboard into TEST MEMORY.

   d. Remove the first card from the program deck and place the deck into the card reader hopper.

   e. Depress the MASTER RESET and START FROM TEST MEMORY push buttons.

   f. Place TEST MEMORY to ASSIGNED after the deck has started to load.

Note: In both cases above the normal reverse switch is in the Normal position. The BIG MEMORY plugboard will load the program into little memory.

4. Program Modes

a. Mode A

1) Complete Reliability Run of the program thru all test routines.

2) This Mode is selected by loading all B switches in the "0" position.

3) Continuous running of the program will be indicated by the stepping of the Right Test Register which is used as a pass counter. The time for one pass thru the program is 2 minutes.

4) The program has no error HLT's.

5) Less than 10 errors will be printed in straight line print. More than 10 errors will use data reduction.

b. Mode B

1) Non-Marginal Check run of the program with selected test routines.

2) At least one of the Right B switches from R2 thru R15 must be in the one position. L8 and L1 must both be in the zero position.

3) Instead of the program running thru the entire program as in Mode A, only the Routine selected by the Right B switches will be run.

4) The type of error print will be selected with the sense switches.

a)	Bypass all errors	SS 3 ACTIVE
b)	Straight line print	SS 1 ACTIVE
c)	Data reduction	SS 2 ACTIVE
d)	Least error print	No SENSE Switches
	Less than 10	Straight line print
	10 or more	Data reduction

5) Individual subplanes can be selected with L11 thru L15 B switches.

a) To test all subplanes, place B switch L11 = 0.

b) To test selected subplanes, place B switch L11 = 1 and select the subplane with B switches L12-L15 as follows:

EXAMPLE:		L11	L12	L13	L14	L15
SUBPL	0	1	0	0	0	0
SUBPL	1	1	0	0	0	1
SUBPL	2	1	0	0	1	0
*****	*	*	*	*	*	*
SUBPL	17	1	1	1	1	1

6) If the program runs successfully and data reduction is selected, the program will cause a success printout.

7) Prior to running margins the program will make one reliability pass through every test routine. If any errors are encountered the appropriate error printout will be obtained.

a) No Sense Switch-Least Error
b) Sense Switch 1 - Straight Line Print
c) Sense Switch 2 - Data Reduction

Note: After the error printout the following lines will print: "Reliability Pass Fouled Auto Margins Should Not Be Run".

8) The M. C. System must be placed in Calculator mode prior to running margins.

9) Error Indications

a) Printout of the MC word causing the failure, along with the number of the routine failing, under INFO.

b) If the failure was caused by bad parity, under INFO will be "0.77701" for Test No. 1, etc. for the other test.

c) LEAST-ERROR printout of information failures for the first routine that fails if running to prescribed.

c. Mode C

1) In this mode, <u>all</u> memory margins are tested. Margins may be run to prescribed, failure, or failure-minus-one. No test routines may be selected.

2) This Mode is selected by setting LS of the B switches to a 1. All other B switches must be in the zero position. Place MC data cards in the reader.

3) Three different types of margins may be selected.

a)	SS 4 ACTIVE	Run prescribed margins
b)	SS 3 ACTIVE	Run failure-minus-one margins (FMO)
c)	SS 3 & 4 ACTIVE	Run to failure

4) A successful printout will be determined by the type of margin selected.

	Running to:	Success Indication
a)	Prescribed	No Printout
b)	FMO	"OK" printed for lines that fail at FMO
c)	Failure	"OK" printed for lines that fail above prescribed

5) The time required to run the program will be determined by the type of margin selected.

Prescribed - 18 minutes; FMO - 18 minutes; Failure - 25 minutes.

d. Mode D

1) This mode allows running of selected margins with selected error printouts. Margins may be run to prescribed, failure or failure minus one. No test routines may be selected.

2) This mode is selected by first leaving LS of the B switches cleared and inserting the "Ident" number of the desired marginal check line in R8 thru R15 of the B switches. After the MC System is placed in Calculator mode, the MC data cards are placed in the reader and BP X 644 is put into the A switches . The start from Test Memory push button will cause the card reader to operate until the desired ident is found. The reader will then stop and the program will HLT with the Program Counter equal to 2.00665. Set the A switches to BPX 0 and the B switches to all cleared except Ls to a 1. Press the continue push button and the MC data cards remaining in the reader will be run.

3) Three different types of margins may be run.

a)	SS 1 ACTIVE	Run prescribed margins
b)	SS 3 ACTIVE	Run failure-minus-one margins (FMO)
c)	SS 3 & 4 ACTIVE	Run to failure

4) Types of error print selections:

a)	All Sense Switches OFF	Least-Error printout
b)	Sense Switch #1 Active	Straight-Line printout
c)	Sense Switch #2 Active	Data Reduction printout
d)	All " " "	Least-Error "
e)	Only " " #3&4 "	No info error "

5) A successful margin will be indicated by an "OK" printout or no "Fail" printout.

e. Mode E

1) This mode provides tuning routines for scoping and fine tuning of memory. No test routines may be selected.

2) This mode is selected by L1 of the B switches and any other B switch from L2 thru L15 to select the desired tuning routine.

Note: If more than one B switch from L2 thru L15 are ones, the tuning will be selected by the switch nearest L1.

5. Program Test Routines

a. There are many weaknesses to serial type equipment such as a memory device. This means to properly test this equipment, many different stringent type conditions must be put on this equipment to insure that it is functioning properly. Some of these more stringent tests, however, are not advantageous for trouble shooting basic catastrophic type troubles. For this type, we have basic tests such as: Ones discrimination, Zeroes discrimination, and addressing. Once these basic type test are running properly we approach the more stringent type test. Some of these utilize several stringent applications such as, pattern and frequency, to provide a more effective test and to hold the number of tests to a minimum. Some of the conditions that must be tested in the 256^2 memory are as follows:

1) The ability for each core to read a one-(ones disc).
2) The ability for each core to read a zero-(zeros disc).

3) The ability for each address to be properly selected (addressing).
4) The ability to continuously read from a particular address at a 6 u s rate - Regular and Inverted checkerboard beat test.
5) The ability to send successive addresses at a 6 u s rate in a burst type condition with a stringent pattern - Regular and Inverted maximum voltage test.
6) The ability to read successive addresses at a 6 u s rate in a burst type condition with a stringent alternate pattern - Regular and Inverted maximum voltage alternate pattern.
7) The ability to read stringent patterns that create noise on the sense amplifiers - test 12 and 13.
8) The ability to perform I/O Memory cycles and computer memory cycles with differences in start memory timings - I/O Compatibility.
9) The ability to perform test under the most stringent patterns such as the worst pattern.
10) The ability to perform test which create core history such as Test 6 through 14.

b. Test Routine 1 - Ones Discrimination

1) This tests the memory's ability to read Ones from each core. This is done by writing Ones into each address and then attempting to read Ones back from each address.
2) Records all errors.
3) Useful for isolating failures.
4) Checks SA's for dropping bits
5) Checks DPD's for continuous conduction.
6) Does not prove address selection system is functioning correctly.
7) Does not check parity.

c. Test Routine 2 - Zeros Discrimination

1) This is similar to Test No. 1 except it tests for zeros.
2) Checks DPD for non-conduction.
3) Checks SAs for continuous conduction.
4) Will run successfully with memory units power off.

d. Test Routine 3 - Addressing

(1) This routine places a constant equal to the address in both left and right half memory words.

(2) This may be the only test routine that fails when an addressing malfunction is present.

(3) Address 0.00000 does not fail if power goes down.

e. Test Routine 4 - Regular Checkerboard Beat Test

(1) This Test loads the regular checkerboard pattern into memory and then locks the I/O ADR CTR on to each address and writes 40_8 words into the I/O reg. After each address is treated in this manner, the program then checks the contents of memory for information failures.

(2) The regular checkerboard pattern puts all ones into each address that is made up of positive cores and zeros into each address that is made up of negative cores. Positive or Negative cores are identical except that they induce a different polarity voltage into the sense winding when they are switched from a one to a zero. All of the cores in one address will be the same polarity.

(3) The primary cause of failure is the repetitive selection of the same address rather than the use of the checkerboard pattern. This pattern will cause some failures that would not be detected by all ones or all zeros due to the lack of cancellation between half select noises in the checkerboard.

f. Test Routine 5 - Inverted Checkerboard Beat Test

(1) Same as test 4 except the positive cores are loaded with zeros and the negative cores are loaded with ones.

g. Test Routine 6 - Regular Checkerboard Maximum Voltage Test

(1) This test loads the checkerboard pattern into the subplanes in such a manner as to create a maximum voltage across the sense windings. Prior to loading this pattern the memory is cleared at a 6 usec rate, twice to create stringent conditions upon the memory. Once the pattern is loaded the memory contents are written into the I/O REG at a 6 usec rate. The test, then senses for a memory parity error. If it senses one, it then checks the contents of memory for an error. If there is no memory parity, it assumes no error.

2) This pattern is loaded in such a manner to cause a maximum voltage to be induced into a sense winding. The SA's must recover before the next address is selected or a zero may be read as a one.

h. Test Routine 7 - Inverted Checkerboard Voltage Test.

1) This is the same as Test Routine 6 except the maximum voltage is in the opposite direction.

i. Test Routines 10 & 11 - Maximum Voltage Alternate Checkerboard Regular.

1) This test is identical to Tests 6 & 7 except the way in which voltage is developed across the sense windings. This test is designed to check for cross-talk between planes.

j. Test Routines 12 & 13 - Regular and Inverted Checkerboard Maximum Voltage Parity Test.

1) These tests are of similar function as Test No. 6 and 7. However, it tests for maximum voltage of the parity bit. In doing so, it utilizes such a word make up as to test for noise on the sense amplifier ground bus and concentrate on bit positions L7, L8 and R7, R8 to pick up the noise.

Note: These SA's seem to be more sensitive to noise than any others. Therefore, the test pattern used in this routine was chosen so as to irritate this condition. The tendency is to pick bits.

k. Test Routine 14 - I/O Compatibility

1) This test interleaves I/O and computer memory cycles at a 6 u s rate to test the difference in start memory cycles (OT & BO) effects on memory operation. This test is automatically bypassed if main drums are in MANUAL TEST.

l. Test Routine 15 - Worst Pattern Weak Ones Test.

1) This test, by utilizing checkerboard pattern, and disturbing cores in a logical sequence, causes the addition of the cores outputs along a selected line to subtract from that of the fully selected core, causing a weak One. This tests the weakest and sometimes the earliest peaking cores.

m. Test Routine 16 - Worst Pattern Fast Pass

1) This test is the same as test 15 except only a portion of memory is checked.

6. Tuning Routines

a. The tuning options have been designed primarily to be used as an aid in tuning memory. Their use should not be limited to tuning, however, they can be very useful in scoping and isolating malfunctions.

b. To select any of these routines L1 of the B switches must contain a 1.

c. Start Memory Timings (BSw. L2)

1) Selects memory for the five different types of memory cycles. (PT, OTA, OTB, BO and BI)

2) Used to set memory and MAR timings.

d. Diagonal of Array (B Sw. L3)

1) This routine provides read/write current on every X and Y line on the array. This is done by full storing 1.77777, along a diagonal in the array.

2) Provides read/write current to every drive line.

3) Used for scoping read/write waveforms.

e. Diagonal of Tape Cores (B Sw. L4)

1) This routine selects tape cores in each tape core matrix along a diagonal. The routine uses a series of FST instructions. 1.77777, 1.77777 is stored in each memory address selected.

2) Used for scoping SWD and IA outputs.

f. Scope Any Address (B Sw. L5)

1) Reads 1's from the I/O register into the address specified by the right B switches.

g. Read-Write current (B Sw. L6)

1) This routine pulses three selected addresses so that the Read/Write currents and the half select noise from u and v can all be seen on one drive line from the tape core matrix.

h. DPD Adjustment (B Sw. L7)

1) This routine loads memory with all 1's. The entire memory is then written into the IO register 16 times. Memory is then reloaded and the process repeated as long as B switch L-7 remains down.

2) To adjust a DPD, the SA input is shorted (across input capacitor). This will place 0's in one Sense Section in one plane during the read in cycle of the program. This will give a clean inhibit current waveform for the four DPD's associated with one plane. To adjust the next plane, move the shorting lead.

3) This routine is also useful in scoping the SA test point while writing 1s into the IO register from every memory location. This shows the SA test point with a sample and a 1 waveform.

i. SA Adjust With Scope (B Sw. L8)

1) This routine reads 1.77777, 1.77777 into address 16140 from the IO register at a 6-usec rate.

2) Shows a "1" platform without a sample pulse at the SA test point.

3) Used for adjusting the width of the "1" output using the clipping level.

j. SA Adjust by Ear Zeros (B Sw L9)

1) This tests the memory's ability to read ZEROES, at a six microsecond rate and with a negative margin applied to /90 B3, without picking ONES. If a bit failure occurs it will be displayed in the LIVE TEST register and an audible tone will be heard from the Duplex Maintenance Console speaker.

Note: To check all bits - A switches -- BPX 2.00000
0.00000 0.00000
1.77777 1.77777

To check individual bits - Clear the A switches and then select that bit in the same switches.

k. SA Adjust By Ear Ones (B Sw L10)

1) This is identical to the L9 selection except that it checks for ONES dropping. This routine should run successfully with a /25V margin on the /90 B3 line.

l. SA Adjust By Ear Parity (B Sw L11)

1) This routine should only be run when routines L9 and L10 have been brought up to a desired margin. The error indication for this bit is an audible tone which may occur with a positive or negative margin applied to ∕90 B3 line.

m. CR Adjust By Ear (B Sw L12)

1) This routine reads ONES and ZEROES from memory and causes an audible beep if bits are picked or dropped. This routine is used in conjunction with the tuning procedures utilizing margins - 150 C1234 on the CR's.

n. Automatic Margins to Failure (B Sw L13)

1) This routine will automatically run margins to failure with selected routines on ∕90 B3 SA - and -90 B3 SA - and ∕150 routines on ∕90 B3 and - excursions, and -150 C1234∕ and - excursions. One line of octal print can be obtained on each excursion failure by depressing SENSE switch 1. The option of running just B3, C1234, or both is as follows:

L13	ON - Automatic margins to failure - B3 and C1234
L13 & L14	ON - Automatic margins to failure - B3
L13 & L15	ON - Automatic margins to failure - C1234

7. Data Reduction

a. Is used to provide the operator with a complete and compact picture of the error pattern occurring in the 256^2 memory. This is not a diagnostic printout, in the sense that it points to the exact pluggable unit that is faulty, but is an attempt to give the operator as complete of a picture as possible of the errors encountered so that he can decide which unit is at fault. Utilizing common sense and logical deductions, this feature can be used as a vital tool in maintaining the 256^2 memory.

b. This feature compiles 200000 errors in approximately 4 minutes in contrast to eight to nine hours to print each error separately as in a straight line print.

c. It displays this reduction of errors in a readable form.

d. Each error is broken down into the following categories and stored until the selected routine is finished.

1) BITS PICKED or dropped.
2) Address - into appropriate switch drivers.

3) Subplanes
4) Inhibit regions

e. When the routine is finished it accumulates all the stored information and prints this out in a readable form (Data Reduction format).

TEST NO (Note 1)								Total Number of Errors (Note 2)		
WDS	YV	YU	XV	XU	BIT	DROP	LH PICK	DROP	RH	PICK
0					8					
01					1					
2					2					
3					3					
04					4					
5	(NOTE 3)				5		(NOTE 4)			
6					6					
7					7					
10					8					
1					9					
2					10					
3					11					
4					12					
5					13					
16					14					
7					15					
INHIBIT REG 3	-B				-C		-D	-A		
INHIBIT REG 2	-A				-B		-C	-D		(NOTE 5)
INHIBIT REG 1	-D				-A		-B	-C		
INHIBIT REG 0	-C				-D		-A	-B		

DATA REDUCTION FORMAT

LEGEND

Note 1 An octal number will be printed here that is indicative of the test routing being run at the time of failure.

Note 2 An octal number will be printed here that is indicative of the cumulative total of errors depicted in the individual inhibit regions shown at the bottom of the form. The errors represent address failures not bit failures.

Note 3 The information in this area for the individual Yv, Yu, Xv, and Xu SWD selections reflects the errors counted, in octal notation, on the individual Y and X drive lines of the memory array that utilize the applicable SWD line selections.

Note 4 The information in this area represents the result of examining the left and right half-word digit planes for dropping and picking 1's. If either is present, the total number is depicted, on octal notation, in the appropriate column adjacent to the affected bit.

Note 5 The information in this area reflects a running count, in octal notation, of the number of errors in each subplane. Since the 4 x 4 configuration of subplanes for each digit plane is identified by inhibit region and sense section in the arrangement shown, the resultant printout information establishes a logical pattern for analyzing failures peculiar to DPD and SA circuitry.

f. Typical Data Reduction Printout

TEST NO. 1 TOTAL NUMBER OF ERRORS - 40000

SWDS	YV	YU			BIT	DROP	LH	PICK	DROP	RH	PICK
00	2000	2000	2000	2000	S-	0		0	0		0
01	2000	2000	2000	2000	1	0		0	0		0
02	2000	2000	2000	2000	2	0		0	0		0
03	2000	2000	2000	2000	3	0		0	0		0
04	2000	2000	2000	2000	4	0		0	0		0
05	2000	2000	2000	2000	5	0		0	0		0
06	2000	2000	2000	2000	6	0		0	0		0
07	2000	2000	2000	2000	7	0		0	0		0
10	2000	2000	2000	2000	8	0		0	0		0
11	2000	2000	2000	2000	9	0		0	0		0
12	2000	2000	2000	2000	10	0		0	0		0
13	2000	2000	2000	2000	11	0		0	0		0
14	2000	2000	2000	2000	12	0		0	0		0
15	2000	2000	2000	2000	13	0		0	40000		0
16	2000	2000	2000	2000	14	0		0	0		0
17	2000	2000	2000	2000	15	0		0	0		0

INHIBIT REG 3	0-B	0-C	10000-D	0-A
INHIBIT REG 2	0-A	0-B	0-C	10000-D
INHIBIT REG 1	10000-D	0-A	0-B	0-C
INHIBIT REG 0	0-C	10000-D	0-A	0-B

1) In this example, a 1's test (Test No. 1) has been run that produces 40,000 errors. Examination of area 1 reveals there are 2,000 errors indicated for each u and v selection line. There is nothing significantly different here since the errors are common, however, in area 2 there are 40,000 dropped 1's indicated for digit plane R13 whereas the remaining digit planes show no errors of any kind. In area 3 there are 10,000 errors indicated for each

of the subplanes in sense section D; all other sense sections are unaffected. From the foregoing, the significant differences are found in both area 2 and area 3. Analyzation of this information shows that 40,000 1's from digit plane R13 are being dropped. Usually this type of trouble is associated with the SA, however, if the SA for R13 was inoperative it would be impossible to read out any 1's thereby producing 200,000 errors. Area 3 supplies the answer since the problem is further isolated to the four subplanes (10,000 errors apiece) incorporating the sense section D winding. Since a single sense section represents one of four inputs to a SA, the most likely diagnosis for this malfunction would be a loss of sense section D input to the SA for R13. Actually the trouble was induced by shorting out the capacitor on the sense section D input to the SA for R13.

2) The common 2,000 error indication noted in area 1 reflects the number of errors counted on the memory array Y and X drive lines that are selected by the applicable u and v lines. All the u and v selections are involved because the four affected subplanes (1, 4, 13, 16) in R13 are in separate locations in each of the four inhibit regions, therefore, one example should suffice in explaining the 2,000 error count for all lines. Consider Yu = 06; this selection drives 20Y-odd drive lines in subplane 13 (as well as 12, 11 and 10). Since these Y drives in the affected subplane 13 are intersected by 100 X-drive lines the maximum number of errors is 2,000 (100 x 20). This amount is then reflected on the applicable selection line Yu = 06.

7. Straight Line Print

a. This option is especially useful when only a few errors are encountered. In order to determine which info pattern is being used it is necessary to be familiar with the selected test being run.

b. Utilizing the Straight Line print in conjunction with data reduction can be especially useful in the case where there are two shorted drive lines or a weak drive line. This is because of the ocquad-address printout which can be readily interpreted into the exact X or Y lines effected.

C. Data Reduction Printout Analysis

1. The following examples of induced failure printouts should be analyzed for the failing circuit before the analysis portion is read.

2. The Logic Diagram on Page 2900 should be used as an aid in analyzing the printouts.

DATA REDUCTION PRINTOUT, EXAMPLE #1

Test No. 1 TOTAL NUMBER OF ERRORS - 200000

SWDS	YV	YU	XV	XU	BIT	DROP	LH PICK	DROP	RH PICK
00	10000	10000	10000	10000	S-	0	0	0	0
01	10000	10000	10000	10000	1	0	0	0	0
02	10000	10000	10000	10000	2	0	0	0	0
03	10000	10000	10000	10000	3	0	0	0	0
04	10000	10000	10000	10000	4	0	0	0	0
05	10000	10000	10000	10000	5	0	0	0	0
06	10000	10000	10000	10000	6	0	0	0	0
07	10000	10000	10000	10000	7	0	0	0	0
10	10000	10000	10000	10000	8	0	0	200000	0
11	10000	10000	10000	10000	9	0	0	200000	0
12	10000	10000	10000	10000	10	0	0	200000	0
13	10000	10000	10000	10000	11	0	0	200000	0
14	10000	10000	10000	10000	12	0	0	200000	0
15	10000	10000	10000	10000	13	0	0	200000	0
16	10000	10000	10000	10000	14	0	0	200000	0
17	10000	10000	10000	10000	15	0	0	200000	0

****

INHIBIT REG 3	10000-B	10000-C	10000-D	10000-A
INHIBIT REG 2	10000-A	10000-B	10000-C	10000-D
INHIBIT REG 1	10000-D	10000-A	10000-B	10000-C
INHIBIT REG 0	10000-C	10000-D	10000-A	10000-B

Test No. 2 SUCCESS

Core Storage Element

1. Identify the test(s) causing the errors.
   For this particular malfunction two tests were run; test 1, (1's discrimination) caused 200,000 errors; whereas test 2 (0's discrimination), produced no errors and printed success.

2. Evaluate the three areas for significant differences.
   Area 1 - uniform errors (each 10,000), not significant
   Area 2 - 200,000 errors for each of the digit planes R8-R15. This is significant because it is not a uniform indication affecting all planes.
   Area 3 - uniform errors (each 10,000), not significant.

3. Interpret the significant indications
   Droppage of 200,000 1's means every location of digit planes R8-R15 is affected.

4. Diagnose the probable trouble
   Usually 200,000 dropped 1's in a plane indicates a defective SA, however, since there are eight planes involved, it is unlikely that the eight associated SA's are inoperative. A missing sample pulse will give the same indication as a bad SA. Since there are eight sample times in the 256^2 memory, examine the delay taps for the one which would affect the subject planes. Examination revealed the sample tap for planes R8-R15 had been removed.

Remarks

The common 10,000 errors in area 1 reflect the number of errors counted on the memory array Y and X drive lines that are selected by the applicable u and v lines. For example, consider Yu = 05; this selection drives 20Y-odd drive lines through subplanes 7, 6, 5, and 4. The intersection of these Y drives with the 100 X-drive lines in each of the four subplanes results in 2,000 (20 x 100) errors per subplane or a total of 10,000 (4 x 2,000) errors for the four subplanes. Test number 2 printed success because in a 0's test, 0's cannot be dropped.

DATA REDUCTION PRINTOUT, EXAMPLE #2

TEST NO. 2 TOTAL NUMBER OF ERRORS - 200000

SWDS	YV	YU	YV	YU	BIT	DROP	LH PICK	DROP	RH PICK
00	10000	10000	10000	10000	S-	0	200000	0	0
01	10000	10000	10000	10000	1	0	200000	0	0
02	10000	10000	10000	10000	2	0	200000	0	0
03	10000	10000	10000	10000	3	0	200000	0	0
04	10000	10000	10000	10000	4	0	200000	0	0
05	10000	10000	10000	10000	5	0	200000	0	0
06	10000	10000	10000	10000	6	0	200000	0	0
07	10000	10000	10000	10000	7	0	200000	0	0
10	10000	10000	10000	10000	8	0	200000	0	0
11	10000	10000	10000	10000	9	0	200000	0	0
12	10000	10000	10000	10000	10	0	200000	0	0
13	10000	10000	10000	10000	11	0	200000	0	0
14	10000	10000	10000	10000	12	0	200000	0	0
15	10000	10000	10000	10000	13	0	200000	0	0
16	10000	10000	10000	10000	14	0	200000	0	0
17	10000	10000	10000	10000	15	0	200000	0	0

****

INHIBIT REG 3	10000-B	10000-C	10000-D	10000-A
INHIBIT REG 2	10000-A	10000-B	10000-C	10000-D
INHIBIT REG 1	10000-D	10000-A	10000-B	10000-C
INHIBIT REG 0	10000-C	10000-D	10000-A	10000-B

Core Storage Element

1. Identify the test(s) causing the errors
   For this particular malfunction two tests were run; test 1 printed success, however, test 2 caused 200,000 errors.

2. Evaluate the three areas for significant differences.
   Area 1 - uniform errors (each 10,000), not significant.
   Area 2 - 200,000 errors for each digit plane in the entire left-hand word (LHW). This is significant because the right-hand work (RHW) is not affected similarly.
   Area 3 - uniform errors (each 10,000), not significant.

3. Interpret the significant indications.
   The malfunction is detected on a 0's test whereby the entire 200,000 locations on each digit plane in the LHW contain 1's instead of 0's.

4. Diagnose the probable trouble.
   Picked bits usually indicates the absence of inhibit current. The 256^2 memory requires four DPD's per plane to generate the inhibit current for each of the four inhibit regions, therefore, for the 16 planes affected there are 64 DPD's. The DPD's are eliminated as the possible cause since the quantity involved, makes it more likely to be a malfunction that is common to all of them. This could be either the LHW inhibit gate generators or the DPD selection gates, however, since there are four each it is unlikely that a group of four would be defective at the same time. A loss of the set-inhibit-LHW pulse from the clock, however, would affect all DPD selection gates. Examination revealed that this clock pulse had been removed.

Remarks

Refer to remarks for the previous example, number 1, it is also applicable to indication in area 1 here. Test 1 (1's test) printed success because this malfunction affects 0's only.

DATA REDUCTION PRINTOUT, EXAMPLE 3

TEST NO. 2 TOTAL NUMBER OF ERRORS - 40000

SWDS	YV	YU	XV	XU	BIT	DROP	LH PICK	DROP	RH PICK
00	2000	2000	2000	0	S-	0	0	0	0
01	2000	2000	2000	10000	1	0	0	0	0
02	2000	2000	2000	0	2	0	0	0	0
03	2000	2000	2000	0	3	0	0	0	0
04	2000	2000	2000	0	4	0	0	0	0
05	2000	2000	2000	10000	5	0	0	0	0
06	2000	2000	2000	0	6	0	0	0	0
07	2000	2000	2000	0	7	0	0	0	0
10	2000	2000	2000	0	8	0	0	0	0
11	2000	2000	2000	10000	9	0	0	0	0
12	2000	2000	2000	0	10	0	0	0	0
13	2000	2000	2000	0	11	0	0	0	0
14	2000	2000	2000	0	12	0	0	0	0
15	2000	2000	2000	10000	13	0	0	0	0
16	2000	2000	2000	0	14	0	0	0	0
17	2000	2000	2000	0	15	0	40000	0	0

****

INHIBIT REG 3	0-B	0-C	0-D	0-A
INHIBIT REG 2	0-A	0-B	0-C	0-D
INHIBIT REG 1	10000-D	10000-A	10000-B	10000-C
INHIBIT REG 0	0-C	0-D	0-A	0-B

ANALYSIS

1. Identify the test(s) causing the errors.
   For this malfunction two tests were run; test 1 printed success, however, test 2 caused 40,000 errors.

2. Evaluate the three areas for significant differences.
   Area 1 - 10,000 errors for Xu = 01, 05, 11 and 15; this is significant since all other Xu selections contain no errors.
   Area 2 - 40,000 errors for digit plane L15; this is significant since all other planes are errorless.
   Area 3 - 10,000 errors in each subplane of inhibit region 1; this is significant because all the other inhibit regions show no errors.

3. Interpret the significant indications
   The malfunction is detected by a 0's test whereby 40,000 locations on digit plane L15 are shown to contain 1's instead of 0's. The significant indications in area 1 and area 3 isolate the 40,000 errors on plane L15 to the four subplanes (each with 10,000 errors) comprising inhibit region 1.

4. Diagnose the probable trouble
   Picked bits usually indicate the absence of inhibit current. Since the symptoms are isolated to one inhibit region in one specific digit plane, the most likely source of trouble is the applicable DPD. Examination revealed that the L15 DPD for inhibit region 1 was defective.

Remarks

The Xu = 01, 05, 11 and 15 represent the selection lines for the 100 X-drive lines in inhibit region 1, therefore, each reflects the maximum of 10,000 errors. The other Xu lines show no errors because they select the X-drive lines in the remaining three inhibit regions which were unaffected. The errors shown for each of the Yv, Yu, and Xv represent the intersection of the 20 memory array drive lines each selects with the affected 100 X-drive lines in the subplanes of inhibit region 1. As a result there are 2,000 errors (20 x 100) reflected on these lines in area 1.

DATA REDUCTION PRINTOUT, EXAMPLE 4

TEST NO. 1 TOTAL NUMBER OF ERRORS - 400

SWDS	YV	YU	XV	XU	BIT	DROP	LH PICK	DROP	LH PICK
00	20	20	0	0	S-	400	0	400	0
01	20	20	0	0	1	400	0	400	0
02	20	20	0	0	2	400	0	400	0
03	20	20	0	0	3	400	0	400	0
04	20	20	0	0	4	400	0	400	0
05	20	20	0	400	5	400	0	400	0
06	20	20	0	0	6	400	0	400	0
07	20	20	0	0	7	400	0	400	0
10	20	20	400	0	8	400	0	400	0
11	20	20	0	0	9	0	0	400	0
12	20	20	0	0	10	400	0	400	0
13	20	20	0	0	11	400	0	400	0
14	20	20	0	0	12	400	0	400	0
15	20	20	0	0	13	400	0	400	0
16	20	20	0	0	14	400	0	400	0
17	20	20	0	0	15	400	0	400	0

****

INHIBIT REG 3	0-B	0-C	0-D	0-A
INHIBIT REG 2	0-A	0-D	0-C	0-D
INHIBIT REG 1	100-D	100-A	100-B	100-C
INHIBIT REG 0	0-C	0-D	0-A	0-B

OCQUAD	YV	YU	XV	XU	TEST	LEFT HAND WORD	RIGHT HAND WORD
OCQUAD	YV	YU	XV	XU			
773 411	17	17	10	05	1	0000 000 001 000 000	0000 000 000 000 000
772 411	17	16	10	05	1	0000 000 001 000 000	0000 000 000 000 000
771 411	17	15	10	05	1	0000 000 001 000 000	0000 000 000 000 000
770 411	17	14	10	05	1	0000 000 001 000 000	0000 000 000 000 000
763 411	17	13	10	05	1	0000 000 001 000 000	0000 000 000 000 000
762 411	17	12	10	05	1	0000 000 001 000 000	0000 000 000 000 000
761 411	17	11	10	05	1	0000 000 001 000 000	0000 000 000 000 000
760 411	17	10	10	05	1	0000 000 001 000 000	0000 000 000 000 000
753 411	17	07	10	05	1	0000 000 001 000 000	0000 000 000 000 000
752 411	17	06	10	05	1	0000 000 001 000 000	0000 000 000 000 000
751 411	17	05	10	05	1	0000 000 001 000 000	0000 000 000 000 000
750 411	17	04	10	05	1	0000 000 001 000 000	0000 000 000 000 000
743 411	17	03	10	05	1	0000 000 001 000 000	0000 000 000 000 000
742 411	17	02	10	05	1	0000 000 001 000 000	0000 000 000 000 000
741 411	17	01	10	05	1	0000 000 001 000 000	0000 000 000 000 000
740 411	17	00	10	05	1	0000 000 001 000 000	0000 000 000 000 000
733 411	16	17	10	05	1	0000 000 001 000 000	0000 000 000 000 000
732 411	16	16	10	05	1	0000 000 001 000 000	0000 000 000 000 000

ANALYSIS

1. Identify the test causing the errors

   Test 1 caused 400 errors as shown in the upper data reduction print. The lower format is a partial straight line print of the same malfunction.

2. Evaluate the three data reduction areas for significant differences.

   Area 1 - 400 errors each on Xv = 10 and Xu = 05; this is significant since all other Xv and Xu lines contain no errors.

   Area 2 - No droppage on digit plane L9; this is significant because the other digit planes in both the LHW and RHW show 400 errors.

   Area 3 - 100 errors in each subplane comprising inhibit region 1; this is significant because the other inhibit regions are errorless.

3. Interpret the significant indications

   The manfunction is detected by a 1's test which identifies L9 as the source of trouble (area 2). The indications in area 3 serve to show that the 400 dropped bits in every plane but L9 are the result of totaling the individual 400 dropped errors in each of the four subplanes comprising inhibit region 1. Finally, the information in area 1 pinpoints the trouble within inhibit region 1 to the drive line selected by Xv = 10 ;and Xu = 05. This is ocquad 411, and is confirmed in the straight line print.

4. Diagnose the probable trouble

   Because of the small number of errors the trouble most likely is isolated to the single drive line (411) in digit plane L9. This is due to the fact that if any of the allied circuitry failed solidly there would be considerably more drive lines affected and consequently more errors. Examination revealed that the X-drive line (411) was opened by removal of the C shim at the input to digit plane L9.

Remarks

The 100 errors in each subplane (area 3) is due to the intersection of 100 Y-drive lines with the open X-drive line (100 X1). The 400 errors in area 1 reflect the total number of errors counted along the X-drive line (ocquad 411) in the four subplanes (100 X4). The 20(errors for the Yv and Yu lines reflect the error count due to the intersection of the 20 drive lines each selects with the open X-drive line (20 X1). The 400 dropped bits in every plane but L9.

DATA REDUCTION PRINTOUT, EXAMPLE #5

TEST NO. 1 TOTAL NUMBER OF ERRORS - 1000

SWDS	YV	YU	XV	XU	BIT	DROP	LH PICK	DROP	RH PICK
00	40	40	0	0	S	1000	0	1000	0
01	40	40	0	0	1	1000	0	1000	0
02	40	40	0	0	2	1000	0	1000	0
03	40	40	0	0	3	1000	0	1000	0
04	40	40	0	0	4	1000	0	1000	0
05	40	40	0	0	5	1000	0	1000	0
06	40	40	0	400	6	1000	0	1000	0
07	40	40	0	0	7	1000	0	1000	0
10	40	40	0	0	8	1000	0	1000	0
11	40	40	0	0	9	1000	0	1000	0
12	40	40	0	0	10	1000	0	1000	0
13	40	40	0	0	11	1000	0	1000	0
14	40	40	0	0	12	1000	0	1000	0
15	40	40	0	0	13	1000	0	1000	0
16	40	40	0	400	14	1000	0	1000	0
17	40	40	1000	0	15	1000	0	1000	0

****

INHIBIT REG 3	0-B	0-C	0-D	0-A
INHIBIT REG 2	200-A	200-B	200-C	200-D
INHIBIT REG 1	0-D	0-A	0-B	0-C
INHIBIT REG 0	0-C	0-D	0-A	0-B

TEST NO. 2 SUCCESS

OCQUAD		YV	YU	XV	XU	TEST	LEFT HAND WORD	RIGHT HAND WORD
773	772	17	17	17	16	1	0000 000 000 000 000	0000 000 000 000 000
773	772	17	17	17	06	1	0000 000 000 000 000	0000 000 000 000 000
772	772	17	16	17	16	1	0000 000 000 000 000	0000 000 000 000 000
772	752	17	16	17	06	1	0000 000 000 000 000	0000 000 000 000 000
771	772	17	15	17	16	1	0000 000 000 000 000	0000 000 000 000 000
771	752	17	15	17	06	1	0000 000 000 000 000	0000 000 000 000 000
770	772	17	14	17	16	1	0000 000 000 000 000	0000 000 000 000 000
770	752	17	14	17	06	1	0000 000 000 000 000	0000 000 000 000 000
763	772	17	13	17	16	1	0000 000 000 000 000	0000 000 000 000 000
763	752	17	13	17	06	1	0000 000 000 000 000	0000 000 000 000 000
762	772	17	12	16	16	1	0000 000 000 000 000	0000 000 000 000 000
762	752	17	12	17	06	1	0000 000 000 000 000	0000 000 000 000 000
761	772	17	11	17	16	1	0000 000 000 000 000	0000 000 000 000 000
761	752	17	11	17	06	1	0000 000 000 000 000	0000 000 000 000 000
760	772	17	10	17	16	1	0000 000 000 000 000	0000 000 000 000 000

ANALYSIS

1. Identify the test causing the errors.
   Test 1 caused 1,000 errors as shown in the upper data reduction print. The lower format is a partial straight line print of the same malfunctions. Test 2 printed success.

2. Evaluate the three data reduction areas for significant differences
   Area 1 - 400 errors each on Xu = 06 and Xu = 16; this is significant because the other Xu lines contain no errors. 1,000 errors on Xv = 17; this is significant because the other Xv lines are errorless.
   Area 2 - Uniform errors (1,000 dropped bits) for each digit plane are usually indicative of a selection circuit malfunction although for this example the trouble is elsewhere.
   Area 3 - 200 errors in each subplane comprising inhibit region 2; this is significant because the other inhibit regions are unaffected.

3. Interpret the significant indications
   In area 1 the combination of Xv = 17 and Xu = 16 selects X-drive 752 (ocquad); and the combination of XV = 17 and Xu = 16 selects X-drive line 772 (ocquad). These lines represent two X-odd drive lines that feed each of the four subplanes in inhibit region 2 for all of the digit planes. The 200 error indications in area 3 confirm the fact that there are two lines involved (100 errors per line). The straight line print further identifies the two affected drive lines as being 772 and 752.

4. Diagnose the probable trouble
   The malfunction cannot be due to a solid selection circuit defect because such a deficiency would normally affect a minimum of 20 drive lines. Since two drives represented by 752 and 772 are physically adjacent to each other it is likely that the lines are shorted together, which was found to be the actual malfunction.

Remarks

Since Xv = 17 is common to both Xu line selections, if reflects the total of the individual 400 error counts indicated for these lines, that is, 1,000 (400 x 2). The other error counts are double those found in example number 4 because they represent the involvement of two lines instead of one.

DATA REDUCTION PRINTOUT, EXAMPLE #6

TEST NO. 1 TOTAL NUMBER OF ERRORS - 10000

SWDS	YV	YU	XV	XU	BIT	DROP	LH PICK	DROP	RH PICK
00	400	400	400	100000	S	10000	0	10000	0
01	400	400	400	0	1	10000	0	10000	0
02	400	400	400	0	2	10000	0	10000	0
03	400	400	400	0	3	10000	0	10000	0
04	400	400	400	0	4	10000	0	10000	0
05	400	400	400	0	5	10000	0	10000	0
06	400	400	400	0	6	10000	0	10000	0
07	400	400	400	0	7	10000	0	10000	0
10	400	400	400	0	8	10000	0	10000	0
11	400	400	400	0	9	10000	0	10000	0
12	400	400	400	0	10	10000	0	10000	0
13	400	400	400	0	11	10000	0	10000	0
14	400	400	400	0	12	10000	0	10000	0
15	400	400	400	0	13	10000	0	10000	0
16	400	400	400	0	14	10000	0	10000	0
17	400	400	400	0	15	10000	0	10000	0

****

INHIBIT REG 3	0-B	0-C	0-D	0-A
INHIBIT REG 2	0-A	0-B	0-C	0-A
INHIBIT REG 1	0-D	0-A	0-B	0-C
INHIBIT REG 0	2000-C	2000-D	2000-A	2000-B

TEST NO. 2 SUCCESS

2580

ANALYSIS

1. Identify the test causing the errors
   Test 1 caused 10,000 errors. Test 2 printed success

2. Evaluate the three data reduction areas for significant differences

   Area 1 - 10,000 errors for Xu = 00; this is significant because the remaining Xu lines contain no errors.

   Area 2 - Uniform 10,000 errors for each digit plane is usually indicative of a selection circuit malfunction.

   Area 3 - 2000 errors in each subplane comprising inhibit region 0; this is significant because the other inhibit regions are unaffected.

3. Interpret the significant indications.

   The malfunction is detected by a 1's test whereby 10,000 locations in each of the digit planes contain 0's instead of 1's. The latter type of common error indications implies trouble in the selection circuitry. A check of the selection circuit results obtained in area 1 highlights the fact that the malfunction may be associated with the highly significant indication for selection line Xu = 00. If this selection was unavailable 20 x-drive lines in the memory array would be affected. Since these drives are fed to the four subplanes of inhibit region 0 for each of the digit planes, there would be an error produced for each intersection with 100-Y-drive lines for a total of 2,000 (100 x 20) per subplane or 10,000 (2,000 x 4) for four subplanes in the same inhibit region. This reasoning is confirmed by the results obtained in area 3.

4. Diagnose the probable trouble

   The selection circuitry consists of the tape core matrix, the SWD's the IA's and the MAR. Starting with the tape core matrix and working backwards the malfunction can be due to an open winding for Xu = 00, however, this is not as likely as a defective PU in the other circuitry, which merits first consideration. Since the SWD (Xu = 00) feeds the tape core matrix, it should be investigated next. Substitution of this unit corrected the malfunction.

Remarks

The 400 errors for the selection lines in area 1 reflect the errors counted on the respective drive lines in the memory array, that is, each selection accounts for 20 lines which are affected by the 20 lines due to the defective SWD, hence 400 errors result (20 x 20).

ANALYSIS

Identify the test causing the errors

Test 1 caused 70,000 errors, Test 2 printed success

Evaluate the three data reduction areas for significant differences

Area 1 - 10,000 errors each for Xv = 04, 05, 06, 07, 14, 15, and 16; this is significant because the remaining Xv selections are unaffected.

Area 2 - Uniform errors (70,000 dropped bits) for each digit plane is usually indicative of a selection circuit malfunction.

Area 3 - Uniform errors (each 3,400), not significant

Interpret the significant indications

The malfunction is detected by a 1's test whereby 70,000 locations in each of the digit planes contain 0's instead of 1's. This implies trouble in the selection circuitry which, if it exists, should be apparent by analyzing area 1. The one important thing that may be construed as a pattern in area 1 is the 10,000 errors groupings consisting of Xv = 04, 05, 06, and 07; and of Xv = 14, 15 and 16. Taken indivually each of these selections, if unavailable, would affect four X-drive lines in each of the four inhibit regions (for a total of 20 (4 x 4) X-drive lines). The intersection of these four lines in any of the inhibit regions with the 100 Y-drives would produce 400 (4 x 100) errors in each subplane will be 3,400 (7 x 400). This latter quantity is confirmed by the results obtained on area 3. The total number of errors per digit plane is the sum of all 20 subplanes or 70,000 (3400 x 20) shown in area 2.

Diagnose the probable trouble

The predominant clues are the Xv groupings. The logical approach is to examine the selection circuitry that is common to these groupings. Starting with the tape core matrix, eliminates it as a possible source. Next the SWD PU groupings are examined and none correspond. There is an IA PU, however, that generates the grouping Xv = 04, 05, 06 and 07, and another IA PU that comes close with Xv = 14, 15, 16 and 17. Since it is apparent that at least two PU's are involved, it is not likely that both will be defective at the same time and moreover the second PU doesn't entirely satisfy the condition observed since Xv = 17 produced no errors. The input to the IA's is next examined, this is the diode matrix decoder, see figure 4-4. It is found that the 0-side of the R9 flip-flop is common to the Xv grouping affected, however, it includes Xv = 17 which is not affected The latter condition can occur if the diode connecting the R9 flip-flop to line to line 17 was shorted since this would permit proper selection of Xv = 17 but not the other lines. Examination revealed that this diode was shorted.

Core Storage Element

DATA REDUCTION PRINTOUT, EXAMPLE #7

TEST NO. 1 TOTAL NUMBER OF ERRORS - 70000

SWDS	YV	YU	XU	XU	BIT	DROP LH	PICK LH	DROP RH	PICK RH
00	3400	3400	0	3400	S-	70000	0	70000	0
01	3400	3400	0	3400	1-	70000	0	70000	0
02	3400	3400	0	3400	2-	70000	0	70000	0
03	3400	3400	0	3400	3-	70000	0	70000	0
04	3400	3400	10000	3400	4	70000	0	70000	0
05	3400	3400	10000	3400	5	70000	0	70000	0
06	3400	3400	10000	3400	6	70000	0	70000	0
07	3400	3400	10000	3400	7	70000	0	70000	0
10	3400	3400	0	3400	8	70000	0	70000	0
11	3400	3400	0	3400	9	70000	0	70000	0
12	3400	3400	0	3400	10	70000	0	70000	0
13	3400	3400	0	3400	11	70000	0	70000	0
14	3400	3400	10000	3400	12	70000	0	70000	0
15	3400	3400	10000	3400	13	70000	0	70000	0
16	3400	3400	10000	3400	14	70000	0	70000	0
17	3400	3400	0	3400	15	70000	0	70000	0

****

INHIBIT REG 3	3400-B	3400-C	3400-D	3400-A
INHIBIT REG 2	3400-A	3400-B	3400-C	3400-D
INHIBIT REG 1	3400-D	3400-A	3400-B	3400-C
INHIBIT REG 0	3400-C	3400-D	3400-A	3400-B

TEST NO. 2 SUCCESS

XXII. 256^2 Memory Tuning Procedure

A. General

1. A memory, once tuned, should not be retuned unless all other efforts fail to establish what caused the detuning of the memory.

2. Tuning is used to peak performance from the Memory. The biggest problem encountered in tuning is that all troubles have not been cleared from the Memory. There is no guaranteed method of eliminating all troubles, but one good approach is to scope all non adjustable circuits to be sure their outputs are correct. The waveform checks may be taken care of by P. M. but it is still necessary to check before tuning. The necessity for this has been proven time and again. The following are examples of inadequate troubleshooting:

   a. Open sense winding. One half of the sense winding "D" for L-14 was open causing picked bits. This trouble was "tuned out" but kept re-occurring until finally through extensive troubleshooting it was found.'

   b. MAR cathode with very slow rise time (negative transition) was tuned out.

   c. Defective SWDs, CRs, DPDs and BFNs have also been tuned away. It should be obvious from the preceeding that a man can, using the 171 adjustments available, tune away almost any trouble. It is not possible to stress too strongly the idea of making sure the machine is in good condition before tweaking or tuning.

3. The tuning procedure given here is designed to prevent as much as possible "tuning out" troubles. A great number of methods have been employed to date but none of them specified particular settings for the circuits. This procedure specifies absolute settings for all but 35 of the 171 adjustable circuits in the memory. We know that if this method does not work there is a defective component in the memory.

4. In this procedure the BFNs, CRs and DPDs are set to predetermined values. Slight adjustments are made to the SAs and V CRs only. If proper margins cannot be obtained, then the troubles in the memory should be found.

6. Throughout the core memory tuning procedure reference will be made to the test equipment required for the specific memory adjustment under discussion. The requirements will vary depending on the test performed, however, they will include one or more pieces of test gear. In order to eliminate any undue delays in obtaining equipment while in the process of tuning

the memory, it is recommended that the following test equipment and accessories be provided before a memory tune is initiated:

a. Oscilloscope - Tektronix 545 3034735 or 541.

b. It may be desirable to have an extension cord for the scope. Oscilloscope Plug-In-Unit Preamplifier - Tektronix 53/54G (3034757).

c. Graticule (3033583).

d. Differential Voltmeter-Fluke 801 (3033786).

e. X10 Oscilloscope Probes (2 required) - Tektronix 510A (3033788) equipped with alligator clip and regular hook tips. If available, the Hewlett Packard probes (3116884) may be substituted for the Tektronix type. These probes must be equipped with ground jumpers.

f. Test leads - (2 required) equipped with alligator clips for use with the differential voltmeter. Lead types 3116503 and 3116504 may be used.

g. Jumper lead to be constructed by site personnel. Dimension is 6-inches, equipped with alligator clips on both ends.

h. Sync lead for oscilloscope (at least 12-feet long) - to be constructed by site personnel using coaxial cable and X10 probe body.

i. Hood-Tektronix H510 (3033343).

j. Long screwdrivers (2required) - one equipped with a very narrow blade.

k. Head set for communication with the maintenance console.

l. Wrench to "snug up" pot locking nuts.

B. Check and Adjustment of BFNs

1. This check must be made initially to insure that the tape cores are receiving the proper bias current. It is a critical test and must be made under static conditions, that is, without a program running. In addition, it should not be attempted unless the memory has been operative for a minimum period of 60 minutes.

2. The BFN check consists of measuring the voltage drop that occurs due to the tape core bias current flowing through a 1 ohm test resistor. This voltage is available across test-point pins for each of the BFNs:

a. X BFN 65ABBL21 and L25

Y BFN 65ABBL29 and L25

NOTE

65ABBL25 is a common ground connection for both BFNs. The BFNs are located as follows:

65AAA	X
65ACC	Y

The adjustment is in the V4 position of each P. U. Make sure that BFN P.U. latches are properly adjusted.

3. The voltage obtained across the test resistor is to be 4V ∕ .01V. If the measured value differs from 4.0V ∕ .01V, the BFN must be adjusted to comply.

4. To perform the BFN check, and adjustment, if necessary, requires the highly accurate differential voltmeter, P/N 3033786. The only tool needed is a long narrow-blade type screwdriver for making bias adjustments. Ensure that the differential voltmeter has been on for at least 30 minutes and proceed to calibrate it as follows:

5. Calibration check of the differential voltmeter should be done by the man who will make all meter readings:

   a. Connect the test leads to the ∕ and - terminal posts.

   b. Turn the NULL control knob until the designation VTVM is displayed in the window.

   c. Place the VOLTS RANGE switch in the CAL position.

   d. Turn the controls designated A, B, C, D and E until a 0 appears in each of the respective windows.

   e. Short the test leads together throughout the calibration check.

   f. Depress the CAL PUSH knob and at the same time adjust the ADJ CAL control until the meter pointer is exactly on 0.

   g. Set the VOLTS RANGE switch to 5, and ensure that the NULL control is still set to VTVM.

   h. Adjust the variable control designated ZERO until the meter pointer is exactly on 0. There are two ZERO controls, adjust the one labeled VTVM-10V-1V.

i. Turn the NULL control to display the designation 10V in the window and repeat step 8.

j. Turn the NULL control to display 1V and repeat step 8.

k. Turn the NULL control to display, 1V and adjust the ZERO control (labeled .1V - .01V) until the meter pointer is exactly on 0.

l. Set the NULL control to VTVM.

6. Measurement of BFN voltage for the X BFN

a. The setting for the front panel controls should be:

VOLTS RANGE	5
NULL	VTVM
A	4
B, C, D, E	0

b. Connect the voltmeter leads for the X BFN as follows:

Negative Lead	65ABBL21	Negative Voltage Terminal
Positive Lead	65ABBL25	Ground

NOTE

If the leads are properly connected, the meter needle will deflect to the right.

c. The voltmeter should be positioned so that the man making adjustments also reads the meter.

d. Set the NULL control to the 10V setting and observe the meter. If the meter deflects from the 0, it is necessary to adjust the potentiometer on the front panel of the BFN pluggable unit for a 0 meter reading. Sug up the pot locking nut before adjusting.

NOTE

The BFN reacts slowly to any adjustment; this should be taken into consideration when making any type of adjustment.

e. Increase the sensitivity of the voltmeter by setting the NULL control to 1V. If the meter deflects off 0, readjust the BFN again for a meter reading of 0.

f. For a final check, increase the voltmeter sensitivity to the 0.1V NULL range. If the meter deflects off 0, readjust the RFN for a meter reading of 0. This is the final setting. Do not use the .01V range because the increased sensitivity only produces erratic operation with inconclusive results.

g. Set the Voltmeter to the NULL VTVM range.

h. Move the Positive Voltmeter lead to 65ABBL29 and repeat steps 3 thru 7.

Check and Adjustment of DPDs

1. This check consists of measuring and adjusting, if necessary, inhibit current. All 132 DPDs will be set to this value. This procedure is written for L15. The entire check procedure accorded bit L15 is then repeated for each of the other 32-bits in the data word.

2. The inhibit currents are scoped at the DPD terminating resistors located on panels B and D.

3. Scope Set Up for DPD Check.

   a. Set Square Calibrator to dial to 100v. Set the VOLTS/CM dials to 1. Tune both A and B probes for perfect square wave. Adjust Diff Balance by plugging both probes into the CAL OUT jack adjust triggering STABILITY for a free running sweep. Adjust DIFF BAL control for the narrowest line possible. Plug only the A probe into the CAL OUT jack and reduce output to 50v. Adjust the VARIABLE VOLTS/CM knob to deflect a square wave across exactly 38 on the special graticule.

   b. Remember that the smallest 4 divisions at top and bottom of the graticule are 1 mm each and total graduation top to bottom is 42 mm. After obtaining this adjustment do not change setting of VARIABLE VOLTS/CM dial. With controls thus adjusted the correct DPD waveform of 54V will cover 41 mm as indicated. Note that a set up error of 1 mm would cause all DPDs to be adjusted out of specs. (1 mm = 1.3V.)

   c. Depress the L7 of the B Switches. This routine reads 1's from the I/O Register. Under these conditions inhibit current will not be generated, therefore, it is necessary to compensate for this condtion by shorting out the applicable SA input for each bit under test to simulate the writing of 0's. This is best accomplished by jumpering across the 820 uufd capacitor in the sense section "A" input, using the 6-inch jumper lead. Connect the jumper

to back panel pins 1 and 3 on the resistor board that is applicable to the particular bit under test.

4. Using the calibrated oscilloscope and probes, set the TRIGGER SLOPE to EXT ∫ and connect the TRIGGER INPUT sync lead to 65AJA1 or 67AGF2 (start memory pulse). (67AU29.)

5. Set the preamp Input Selector switch to A-B on the DC side.

6. Connect the INPUT A probe to 66BA4T (DPD terminating resistor test point for L15 inhibit region 0), and the INPUT B probe to 66BAW1 (common ground return).

7. Short out the SA Input for L15 65EGU1 and U3.

8. Set the TIME/CM sweep controls to 2 usec/cm, and use the TRIGGERING LEVEL control to sync in the inhibit current waveform. When it is in sync, turn the 5X MAGNIFIER to ON. The observed waveform should be similar to that illustrated. Sweep time is equal to 0.4 usec/cm.

9. If the observed waveform does not occupy exactly 41 mm of deflection, the inhibit region 0 adjustment on the DPD located at 65CJ should be adjusted. With this requirement satisfied, measure the rise and fall times for conformance within the limits provided in Figure 1. If proper amplitude cannot be obtained, or if the rise and fall time measurements are out of limits, the affected DPD should be replaced.

NOTE

If the rise and fall times are incorrect for all the inhibit currents within one of the inhibit regions, the trouble is not in the individual DPDs but rather in the inhibit gate generator for that particular inhibit region.

10. Remove the INPUT A probe and reconnect it to 66BA3T (DPD terminating resistor test point for L15 inhibit region 1), the INPUT B probes remains at the ground return point. Repeat step 9.

11. Remove the INPUT A probe and reconnect it to 66BA2T (DPD terminating resistor test point for L15 inhibit region 1), the INPUT B probes remains at the ground return point. Repeat step 9.

12. Remove the INPUT A probe and reconnect it to 66BA1T (DPD terminating resistor test point for L15 inhibit region 3), the INPUT B probe remains at the ground return point. Repeat step 9.

13. Remove the short from the SA input for L15.

14. Repeat steps 6 through 13 for each of the remaining bits in the left half-word, moving the INPUT A probe to the applicable DPD terminating resistor test points. In each case ensure that the applicable SA input is shorted out for the individual bit under test.

15. Repeat steps 6 through 13 for each bit, R8 through R15, in the right half-word, moving the INPUT A probe to the applicable DPD terminating resistor test points. For the right half-word, the INPUT B probe should be connected to 66DAW1, In each case ensure that the applicable SA input is shorted out for the individual bit under test.

16. Upon completion of all DPD adjustments be sure to remove the SA shorting jumpers.

D. Check and Adjustment of CRs.

1. Scope Setup for CR Adjustments.

a. The scope should be plugged in so that modules 67D and 65B can be reached without charging the line cord. Allow a 10 minute warm-up period for scope to stabilize. The 53/54G preamp, to be used on all memory circuits, has two front panel screwdriver adjustments which should now be checked.

b. Differential Balance

First, individually tune both probes (6 ft. #3033788) to a perfect square-wave from the CAL OUT jack. Then connect both the input A and B probes to the CAL OUT jack. Select inputs A-B on DC and set both VOLTS/CM dials to .2. Adjust SQUARE-AVE CALIBRATOR dials to obtain 50 volts output. Turn the STABILITY CONTROL clockwise so that the sweep will be visible. The sweep should be a single straight line, the two inputs exactly cancelling each other. Adjust the DIFF BAL screwdriver adjustment until the line is straightened.

c. DC Balance

After the probes have been tuned and the DIFF BAL adjusted, carefully adjust the DC BAL control so that no vertical shift of the trace is observed when rotating the VARIABLE VOLTS/CM dial. While making this adjustment, the trace should be free running with no input to the preamp.

d. The next step is to adjust vertical sensitivity as follows: Reduce SQUARE-WAVE CALIBRATOR output to 10 volts. Attach INPUT A probe to CAL OUT jack. Adjust VARIABLE VOLTS/CM knob to deflect square-wave across 40 mm (4CM).

NOTE

After obtaining this adjustment do not change setting of the VARIABLE VOLTS/CM, focus or astigmatism knobs. The scope is now ready for use.

2. With the Big Memory 1A program previously loaded, set up as follows:

   a. "A" Switches - BPX 200,000

   b. "B" Switches - 0.42000 1.73546

   c. TEST MEMORY - Assigned

   d. Start from test memory

      NOTE: This selected address in the right "B" switches will result in less ringing across each of the CR test points, permitting improved accuracy of amplitude and rise time measurements.

3. Scope Points

   NOTE: The probes should be equipped with insulated aligator clips for attaching to test points located on resistor boards.

   Terminals are as follows:

   XV — Input A probe to 65BGU16
   Input B probe to 65BGU12

   XU — Input A probe to 65BJU16
   Input B probe to 65BJU12

   XV — Input A probe to 67DGU16
   Input B probe to 67DGU12

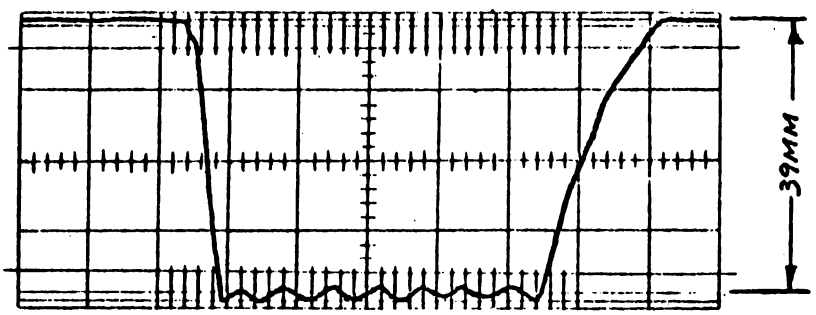
   YU — Input A probe to 67DJU16
   Input B probe to 67DJU12

4. CR AMPLITUDE ADJUSTMENT

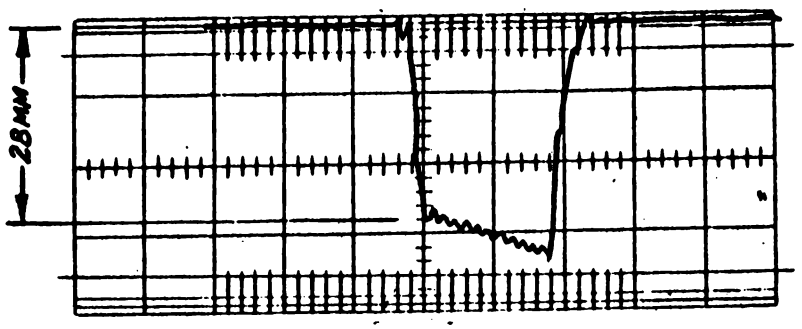
   a. The amplitude of all four CRs should now be adjusted.

   Refer to Pages 2800 and 2820

   b. Center the fine amplitude adjustment (V3) and obtain approximate desired adjustments using the course pot. (V1 position.)



U CR PROPERLY ADJUSTED



V CR PROPERLY ADJUSTED

5. Fast Margins

   a. Preliminary adjustments having now been completed. Run fast margins on the CRs. Set up is as follows:

      NOTE

      Big Mem 1A must have been previously loaded into memory according to the program write-up.

MC System	CALC Mode
"A" Switches	BPX 200,000
"B" Switches	Depress L1, L13, & L15 Tune MC CR's only
Sense Switches	#1 Active
Test Memory	Assigned

      Start from Test Memory

   b. The first failing address for each excursion will be included in the printout. Be aware of the fact that many more addresses are probably failing and bits may not be significant.

6. Margin Analysis

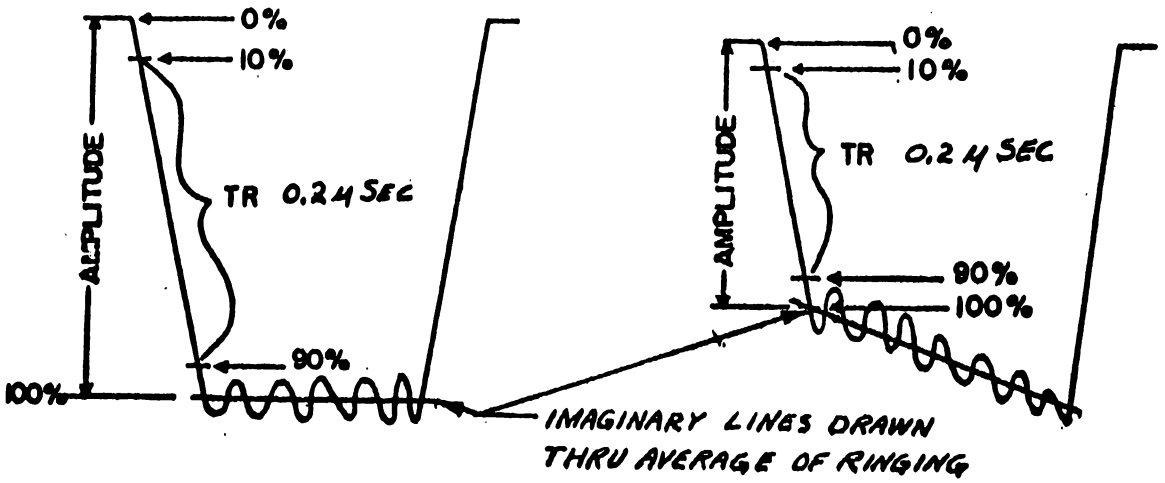
   a. Upon completing fast margins examine the printout to determine if an unbalance exists in the CR margins. It is expected that in some cases the memory will fail at 0 volts in one direction but have a high margin in the opposite direction. As a typical example, assume
q the failing CR margins to be /50 and -10. This unbalance in the positive direction normally indicates that read current is low. A positive margin increases CR output and thus, read current. Always change current in the direction of the biggest margin.

7. Read Current Adjustment

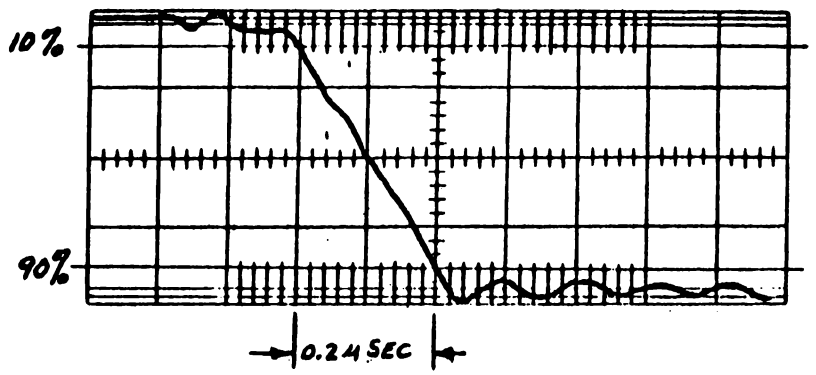
   a. Only the V CR's should be adjusted. Using the R/W CURRENT ADJ. 3 ADR (L1 and L6 of "B" SW.) routine of Big Memory 1A, adjust both XV and YV in the same direction, by the same amount. Observe X and Y read current respectively while making this adjustment. The terminals for observing read current on the array are as follows:

      X - ADR 30 66BPP8D

      Y - ADR 07 66APP1D

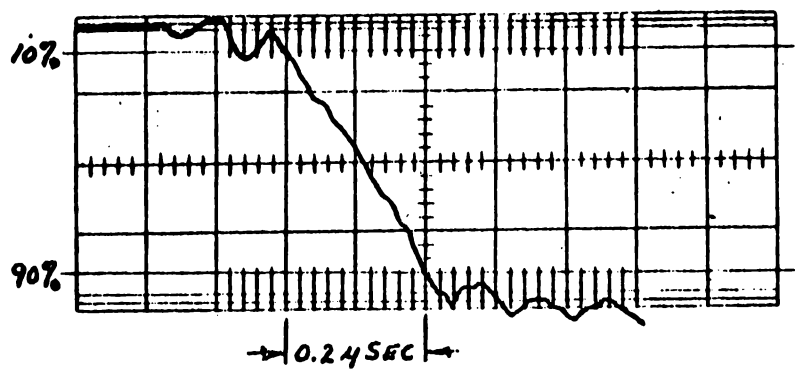


UCR Test Point **VCR Test Point**



U CR RISE TIME

Sweep . 1usec/cm **Vertical VOLTS/CM dial . 2v/cm**



V CR RISE TIME

Sweep . 1usec/cm **Vertical VOLTS/CM dial . 1v/cm**

b. Normally, a 1 volt change is sufficient, however, if extreme unbalance exists, a 2 volt change in read current amplitude can be made. To accurately monitor this adjustment, set up scope as follows:

1) Adjust square wave calibrator to obtain 20 V. output. Connect probe A to CAL OUT jack. Adjust the VARIABLE VOLTS/CM knob to deflect square wave across 40 MM. Switch to external sync, start memory. Attach probe B to bottom ground connection on suitcase and probe A to read current terminal on suitcase. Read on A-B DC. Using vertical position and horizontal controls, position top of read waveform in center of graticule on 2 CM line. Each vertical minor scale division (2MM) will now equal 1 volt.

2) Following this adjustment repeat the fast margins tuning routine, this time including the ∕90 B3 SA line (L1 and L13 of "B" switches). Refer to printout and first consider the results of the CR margin. If the spread between the absolute value of the positive and negative failing excursion is more than 15 volts, readjust the X and Y V CR's in the direction indicated.

EXAMPLE: ∕50 - 30

The spread in this case is 20 V (50-30 = 20). Read current must be increased slightly to reduce this spread.

3) Remember, if unbalance is in the positive direction, increase read current, or if the negative excursion is the largest, decrease read current. A very small change in read current will have a large effect on margins. ALWAYS DISCONNECT ALL SCOPE LEADS FROM FRAME FOLLOWING EACH ADJUSTMENT.

8. Printout Analysis

a. At this time it might be well to stop and consider just what is being accomplished. For instance it is possible that one or two sense amps may now be restricting the CR margin, or, the CRs are still out of adjustment. This can be determined by analyzing the single line printout that occurred with each failing excursion. If in all cases, the bit failures are random, the CRs require further adjustment. But, if three or fewer bits are consistently holding the CR margin down in the weakest direction, then these SAs require adjustment.

E. Sense Amplifier Adjustment

1. When satisfied that the V CRs are near the desired setting, on the basis of the preceding analysis, go to the SA "Beep" routine of Big Mem 1A. Set up is as follows:

MC System	-	Manual Mode
"A" Switches	-	BPX 200,000
"B" Switches	-	Depress L1 and L9 (zeros)
Test Memory	-	Assigned

Start from Test Memory

2. Apply a -34 volt excursion to /90B3. By adjusting the volume of the computer speaker, an audible indication of bit failures can be obtained. If the "A" switches are cleared, or contain BPX 200,000 all bits will be checked and failing bits displayed in the live test register. If desired, bits may be tested one at a time by clearing the "A" switches and then depressing the corresponding toggle switch.

a. Several methods of utilizing the audible beep have been investigated. The following procedure is considered to be most practical. From frame 12, dial the computer speaker and connect headphones to jack provided on the back of frame 12. The man on the console should dial the same number so that he is in direct contact with the man out on the floor making adjustments. The beep level allows normal voice communications. The man on the console should clear the "A" switches to observe all failures and then lock on the left most failing bit by depressing the corresponding "A" switch. The operator equipped with headphones can then use the beep to guide him in properly adjusting the individual SA clipping level. The SAs are located as follows:'

LHW - P thru L15 - 65ECC thru 65EJ respectively

RHW - R5 thru R15 - 67ACC thru 67 AK respectively

If necessary, refer to the PU layout card to make sure that you are adjusting the desired SA. Do not over adjust or these same bits will then fail with a positive excursion. The desired position of this adjustment is that point at which the beep just stops. The smallest increment of angular rotation to stop the beep is required. Alternately lock on and adjust each of the failing bits until all failures are cleared with the -34 volt excursion applied.

b. Depress L10 and clear L9 of the "B" switches and apply a +25 volt excursion to the +90B3 line. This is the SA beep test for ones routine. Repeat above procedure, alternately locking on and adjusting each bit until all failures have cleared. Then recheck the -34 volt excursion (with L9 of the "B" sw.) to see if any SAs were adjusted too far.

3. Parity Routine

a. For adjusting the parity bit, a separate tuning routine of Big Mem 1A is used. Both ones and zeros are combined into one test. Depress L11 and clear L9 of the "B" switches. Alternately apply a -34 and +25 volt excursion to the +90B3 line and adjust as required.

4. Failure Margins

a. After the sense amps have been adjusted, select the CR and SA margin cards from the deck to run automatic failure margins on these lines. These can be determined from MC card indent number. Refer to the program write-up. Set up the machine as follows:

MC System	-	CALC Mode
"A" Switches	-	BPX 200,000
"B" Switches	-	Set LS = 1
Test Memory	-	Assigned
Sense Switches	-	1, 2, 3 and 4 active

b. Place the 4 selected MC word cards in the card reader hopper, ready I/O units, reset flip flops and start from test memory.

c. It will again be necessary to analyze the printouts to determine if a few SAs are limiting the CR margin or if read current requires further adjustment. As a general rule if 3 or fewer bits are restricting the margin, adjust the SAs but if more than 3 bits, adjust the VCRs. Remember changes in read current will be made by adjusting the VCRs only. The UCRs were set up to 9.8 volt and must remain there.

d. The marginal balance of the CRs shall be considered complete when the positive failing excursion is one increment greater than the negative failing excursion. Try for +40 and -35 which should be possible in all cases. (60 or 70 v spread.)

5. Fine Tuning

a. Precise adjustment of the clipping level of each SA is required to obtain adequate CR and SA margins. The beep test, as previously used, will permit fairly close adjustment. But, to obtain a fine tune, analysis of the data reduction printouts and variations of the beep margin are required. This is due to the fact that ones and zeros discrimination, used by the beep routine are not as difficult as most of the longer tests. Ordinarily the more complex tests will fail with a considerably lower margin. It is possible to fail on the "beat" test (4 or 5) at ∕16 volts and ones discrimination to run at safe limits (∕25).

b. As we are restricted by the ∕25 volt safe limits, the most practical way to obtain the required "fine tune" is to shift the beep margin. If a bit is failing below the desired ∕25 volt margin (using the entire program) go to the zeros beep routine (L1 and L9 of "B" sw.) and determine the point of failure in the negative direction. Then decrease this manual margin by approximately 5 volts and adjust the SA so that failure will occur at anything greater than, but will run at, the applied margin. As an example, if the bit is found to fail at -40V, decrease margin to -35 or -36 volts and readjust at that point. Care should be exercised as this is a delicate adjustment.

c. If a bit fails to make the -25V program margin approximately 5 volts in the negative direction.

d. To determine the results of each adjustment, select the failing test routine and, using data reduction, (SS #2) apply a manual margin equal to the automatic margin that failed. The failing test number was contained in the previous failure margins printout. This should only be used to see if margin is shifted sufficiently to allow this test to run. Always follow with automatic failure margins.

e. If unable to obtain the desired adjustment of a specific sense amplifier (insufficient margins) check each of the 4 DPD's for that bit.

NOTE

Accurately set up scope and also compare with nearby bits. If results are still negative, try replacing the sense amp. The tune of memory should be considered complete when the ∕90 B3 margin is ∕25 volts with the -150 C1234 line at ∕40 and -35 volts. Note that these are desired margins and because of variations between

memories, margins somewhat better or worse might be obtained.

F. IA Scoping Procedure

1. The IA (Input Amplifier) output is -150V to -240V. These levels are maintained primarily by diodes in a feedback and clamping circuit. When these diodes go bad one of the levels change. The condition of the 5998 tube in the output stage also affects these levels. If the -150V level goes to approximately -50 the result is excessive drive current on the lines selected by the IA. This gives erratic failures usually traceable thru printout analysis to the bad circuit. The number of failures may not be great although it is significant. If the -240V level goes more positive, it tends to allow the associated switch driver (SWD) to go into partial conduction. This means that the SWD steals current from the selected circuit. If only one IA is bad, the printout will show the failure by the least number of errors. If more than one IA is bad, it will not be possible to find it with a printout.

2. Scope Set Up

Set SQUARE-WAVE CALIBRATOR to obtain 100V square-wave output.

Attach INPUT A probe to Cal Out jack.

Select input A on DC and set VOLTS/CM dial to 2.

Using horizontal sweep and vertical position controls, display several cycles of top of the square-wave across the center of the graticule.

Tune probe to obtain "flat topped" square-wave.

Adjust vertical position and VARIABLE VOLTS/CM controls to deflect square-wave across 40 MM (4CM) as indicated in Figure 1.

Attach INPUT A probe to the -150V supply line at the IA module. With the trace free-running adjust vertical position control only, to position trace on top CM line of graticule. The scope is now calibrated and ready for use.

3. PROGRAM SET-UP

a. "A" Switches - BPX 200,000

b. "B" Switches - Depress L1 and L4

c. Test Memory - Assigned

d. Start from test memory.

4. This tuning routine stores "one" bits in a series of locations so that every IA is pulsed once per loop.

5. The scope points are B1, C1, G1 and H1 of each IA pluggable unit. The IAs are located as follows:

XY	-	65BK, B1, BM and BN
XU	-	65BP, BR, BS and BT
YV	-	67DK, DL, DM and DN
YU	-	67DP, DR, DS and DT

6. Use external sync, start memory. The specifications on the IA output are as follows:

UPPER LEVEL - ∱2 or -5V with respect to -150V supply

LOWER LEVEL - -240V ∱10V

7. Failure of the lower level is more common as several components, when defective, cause similar indications. Normally the trace reaches -240V but then rises rather sharply to near -225V while deselected. Any IA having this lower level more positive than -230, should be replaced.

G. Summary Questions:

1. Many troubles in memory may appear to be corrected by _____ but will re-occur later.

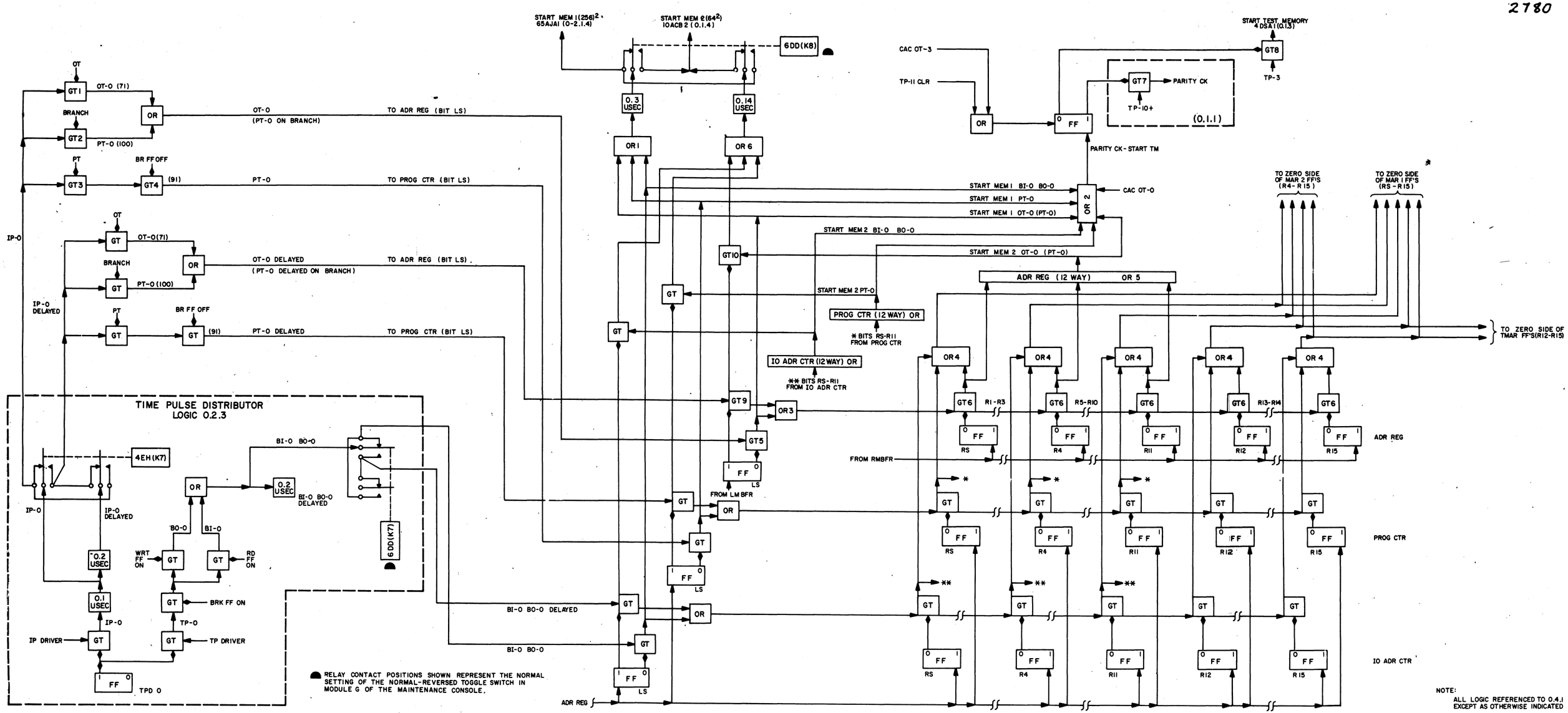
2. The major weak point of this tuning procedure is the necessity for _____ _____ of test equipment.

3. The adjustment of the _____ is first in the tuning procedure.

4. The DPD waveform should be _____ volts in amplitude.

5. When adjusting read current only the _____ CRs are adjusted while the scope is connected across the drive line _____ _____.

6. If more than one IA is bad the _____ _____ should be scoped to locate the troubles.



NOTE:
ALL LOGIC REFERENCED TO 0.4.1 EXCEPT AS OTHERWISE INDICATED

Memory Unit and Address Selection