IBM

Technical Reference
Options and Adapters
Volume 2

IBM Industrial Computer

IBM

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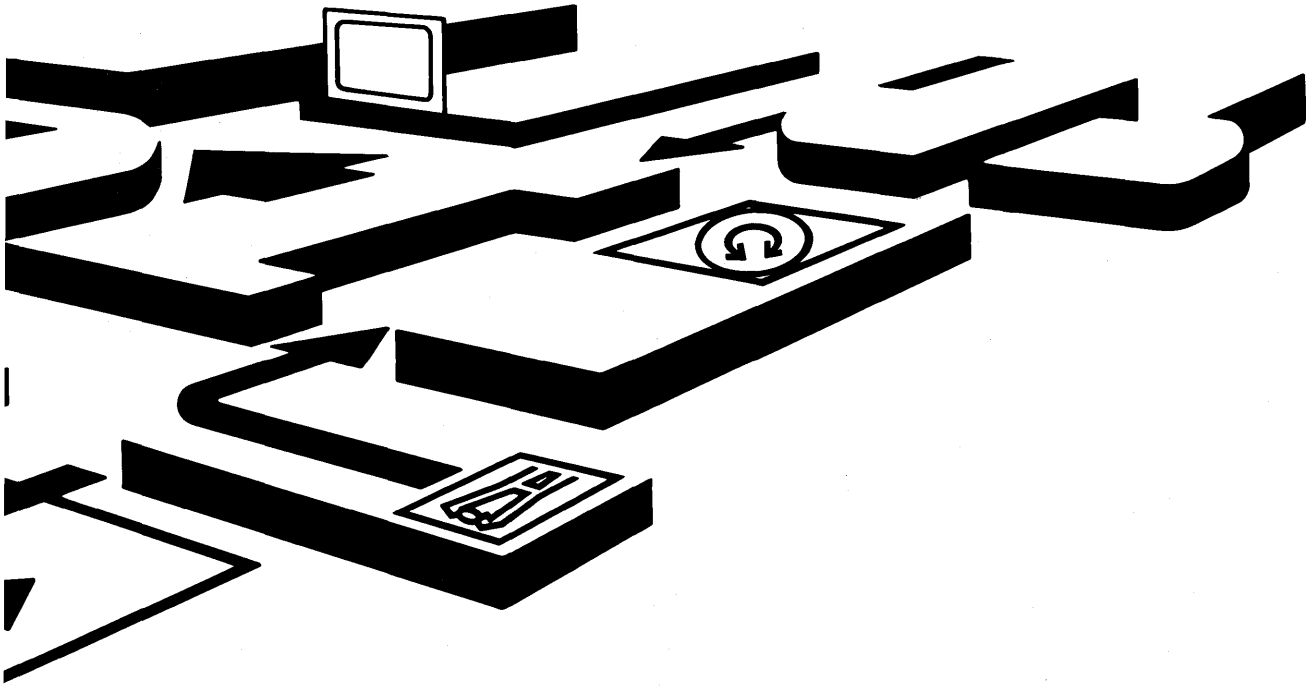


IBM Industrial Computer

IBM Monochrome Display and Printer Adapter

Contents

IBM Monochrome Display and Printer Adapter

Monochrome Display Adapter Function

The IBM Monochrome Display and Printer Adapter has two functions. The first is to provide an interface to the IBM Monochrome Display. The second is to provide a parallel interface for the IBM Printers. We will discuss this adapter by function.

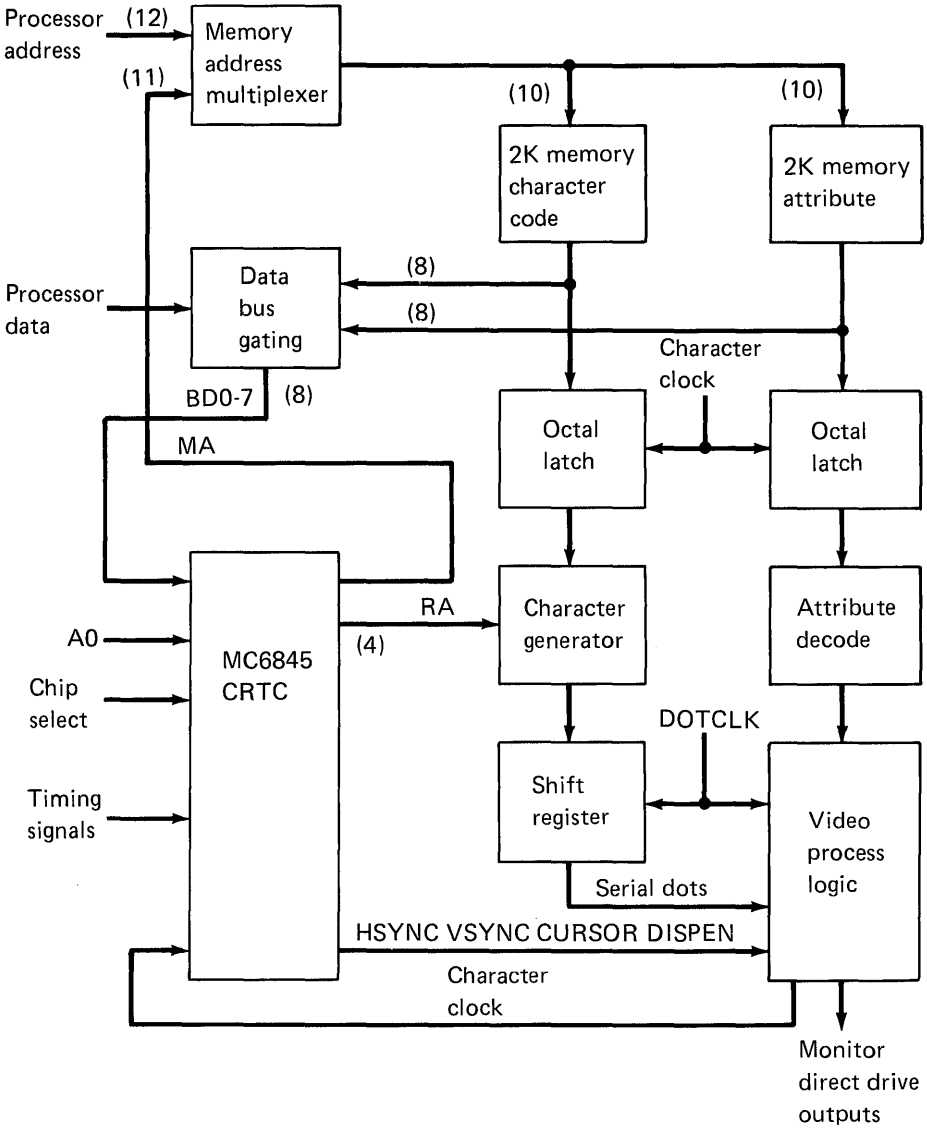
The IBM Monochrome Display and Printer Adapter is designed around the Motorola 6845 CRT Controller module. There are 4K bytes of RAM on the adapter that are used for the display buffer. This buffer has two ports to which the system-unit microprocessor has direct access. No parity is provided on the display buffer.

Two bytes are fetched from the display buffer in 553 ns, providing a data rate of 1.8M-bytes/second.

The adapter supports 256 different character codes. An 8K-byte character generator contains the fonts for the character codes. The characters, values, and screen characteristics are given in "Of Characters, Keystrokes, and Colors" in your *Technical Reference* system manual.

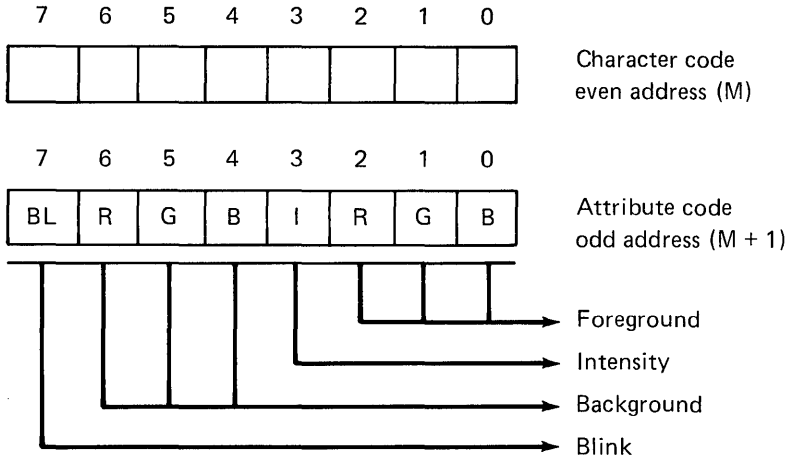
Monochrome Display Adapter Function *(continued)*

The following is a block diagram of the monochrome display adapter portion of the IBM Monochrome Display and Printer Adapter.



IBM monochrome display adapter block diagram

Monochrome Display Adapter Function *(continued)*



The adapter decodes the character attribute byte as defined above. The blink and intensity bits may be combined with the foreground and background bits to further enhance the character attribute functions listed below:

Background			Foreground			
R	G	B	R	G	B	Function
0	0	0	0	0	0	Non-display
0	0	0	0	0	1	Underline
0	0	0	1	1	1	White character/black background
1	1	1	0	0	0	Reverse video

The 4K display buffer supports one screen of the 25 rows of 80 characters, plus a character attribute for each display character. The starting address of the buffer is hex B0000. The display buffer can be read using direct memory access (DMA); however, at least one wait state will be inserted by the system-unit microprocessor. The duration of the wait state will vary, because the microprocessor/monitor access is synchronized with the character clock on this adapter.

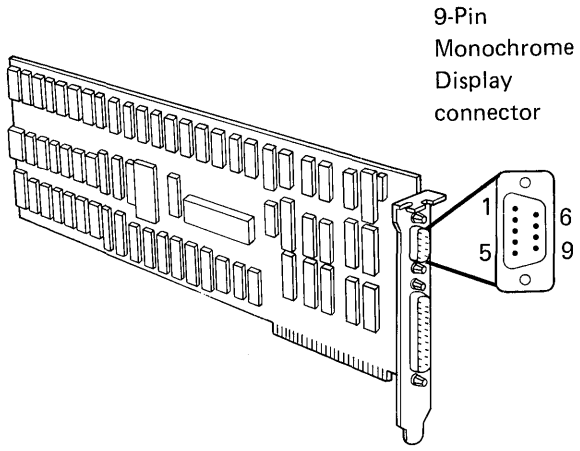
Interrupt level 7 is used on the parallel interface. Interrupts can be enabled or disabled through the printer control port. The interrupt is a high-level active signal.

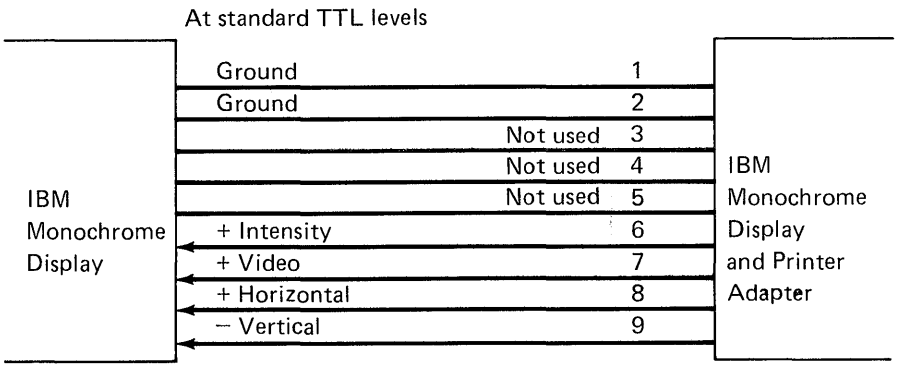
Monochrome Display Adapter Function *(continued)*

Bit number	Function
0	+ Horizontal drive
1	Reserved
2	Reserved
3	+ Black/white video

6845 CRT status port (Hex 3BA)

Connector Specifications



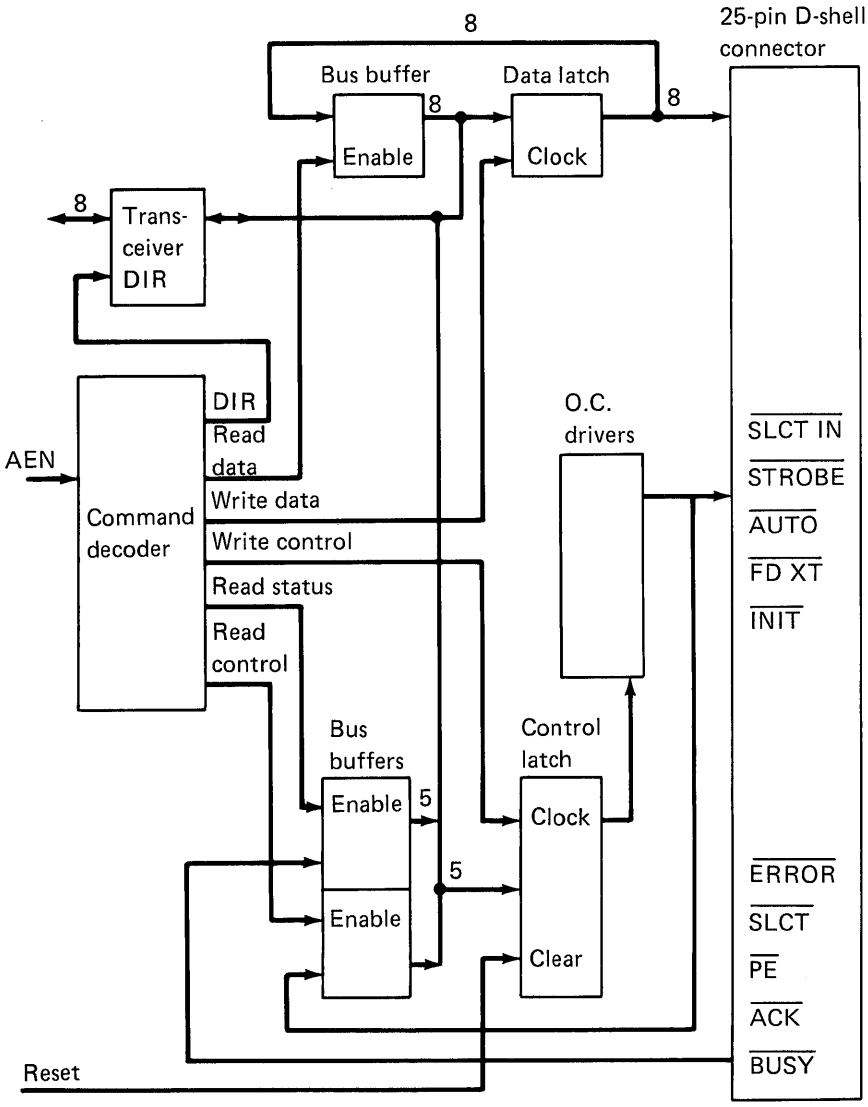


Note: Signal voltages are 0.0 to 0.6 Vdc at down level and +2.4 to 3.5 Vdc at high level.

Connector specifications

Printer Adapter Function *(continued)*

The following is a block diagram of the printer adapter portion of the Monochrome Display and Printer Adapter.



Printer adapter block diagram

Printer Adapter Function *(continued)*

IBM monochrome display and printer adapter
Input from address hex 3BC

This instruction presents the system-unit microprocessor with data present on the pins associated with the output to hex 3BC. This should normally reflect the exact value that was last written to hex 3BC. If an external device should be driving data on these pins at the time of an input (in violation of usage ground rules), this data will be ORed with the latch contents.

IBM monochrome display and printer adapter
Input from address hex 3BD

This instruction presents the realtime status to the system-unit microprocessor from the pins as follows.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pin 11	Pin 10	Pin 12	Pin 13	Pin 15	–	–	–

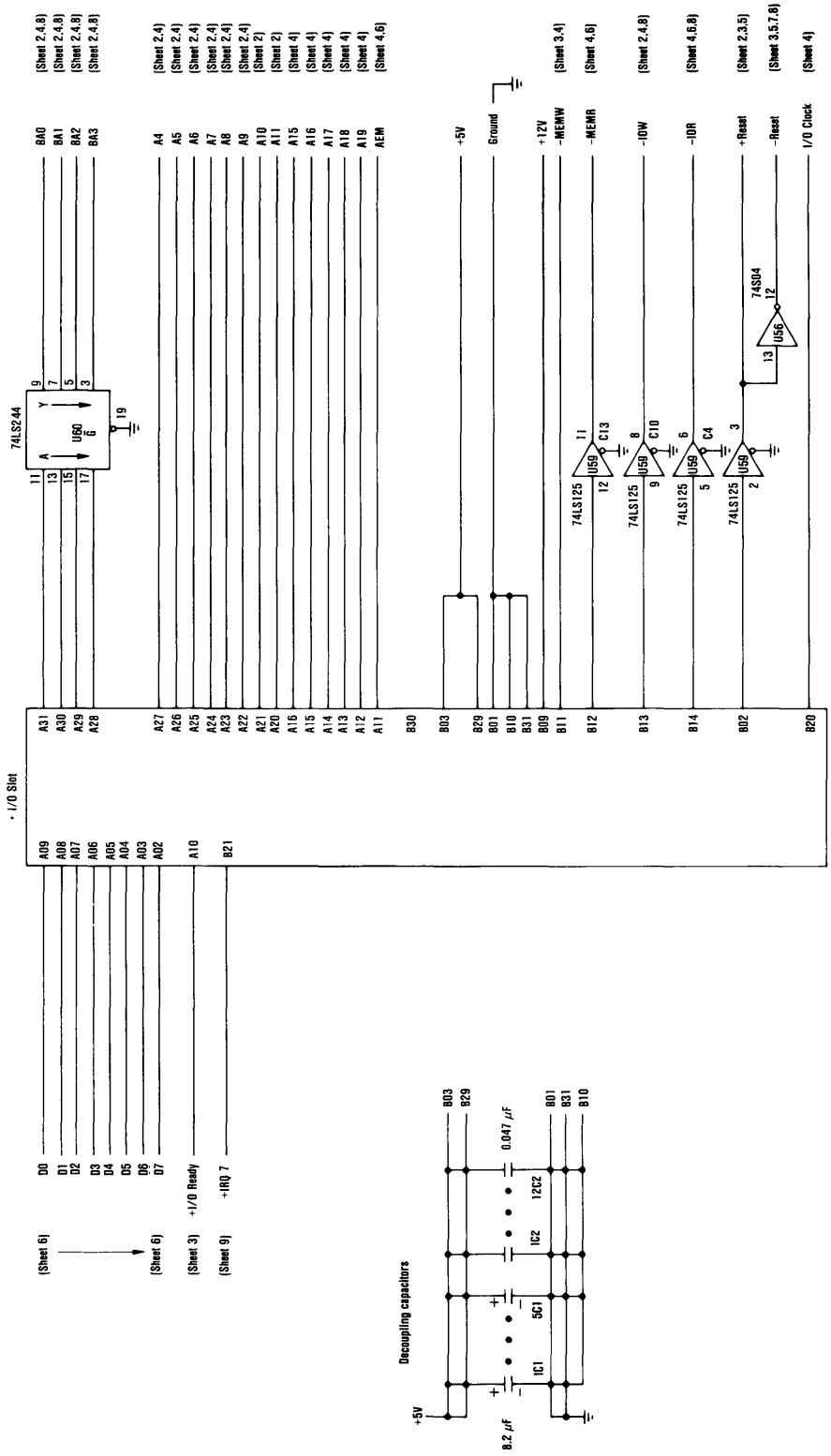
IBM monochrome display and printer adapter
Input from address hex 3BE

This instruction causes the data present on pins 1, 14, 16, 17, and the IRQ bit to be read by the system-unit microprocessor. In the absence of external drive applied to these pins, data read by the system-unit microprocessor will match data last written to hex 3BE in the same bit positions. Notice that data bits 0–2 are not included. If external drivers are dotted to these pins, that data will be ORed with data applied to the pins by the hex 3BE latch.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			IRQ Enable	$\overline{\text{Pin 17}}$	Pin 16	$\overline{\text{Pin 14}}$	$\overline{\text{Pin 1}}$
			Por = 0	Por = 1	Por = 0	Por = 1	Por = 1

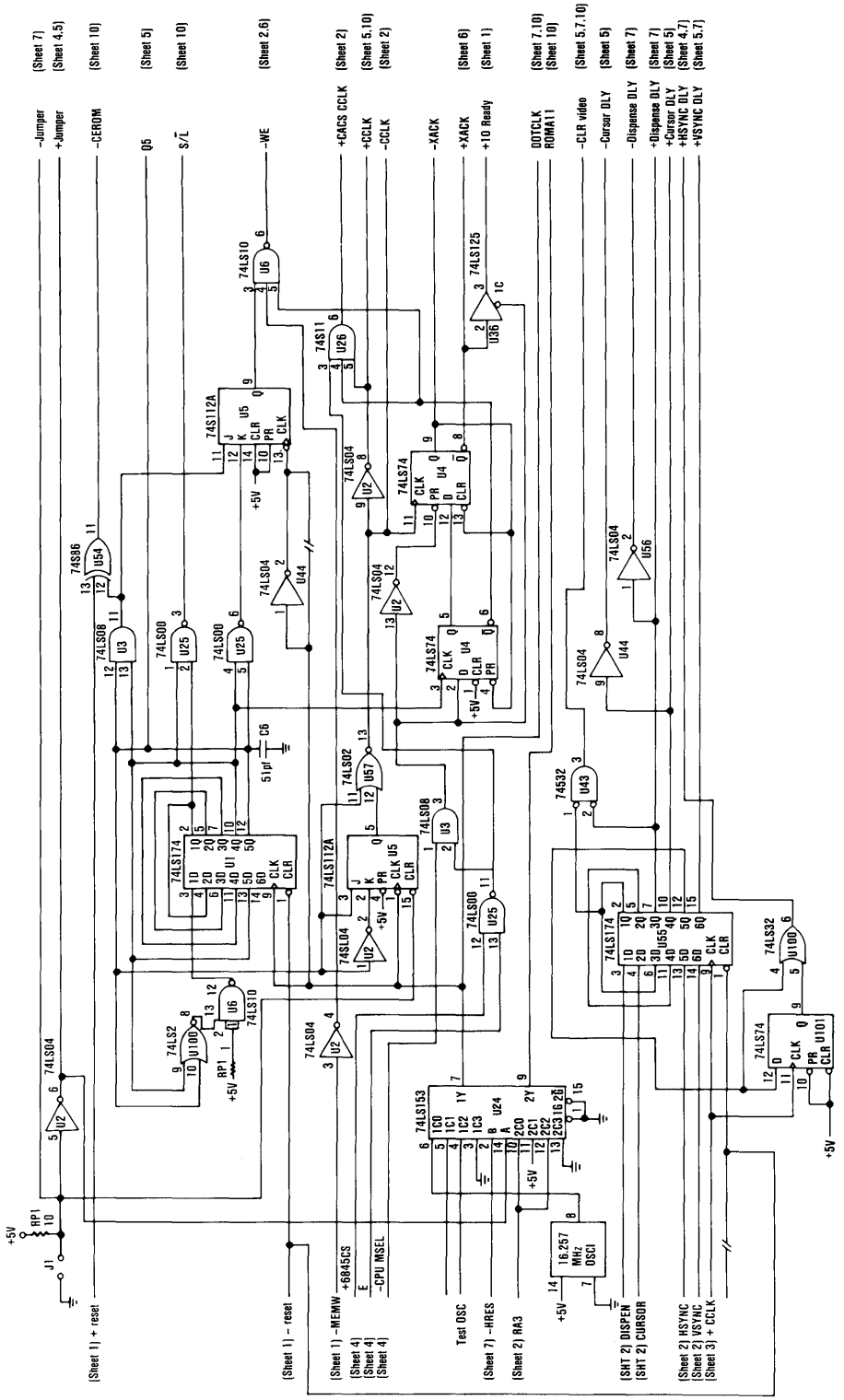
These pins assume the states shown after a reset from the system-unit microprocessor.

Logic Diagrams



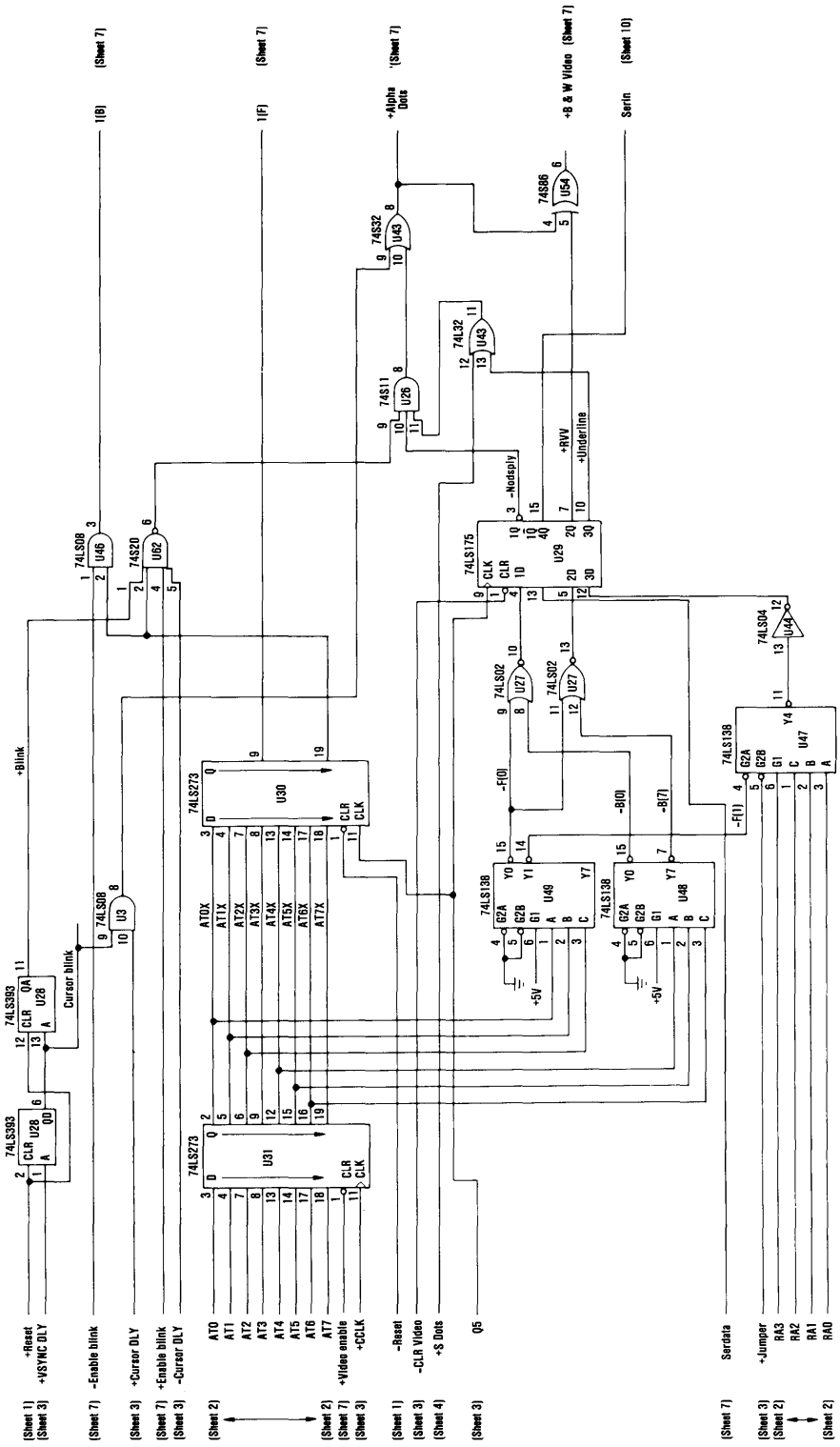
Monochrome display adapter (Part 1 of 10)

Logic Diagrams *(continued)*



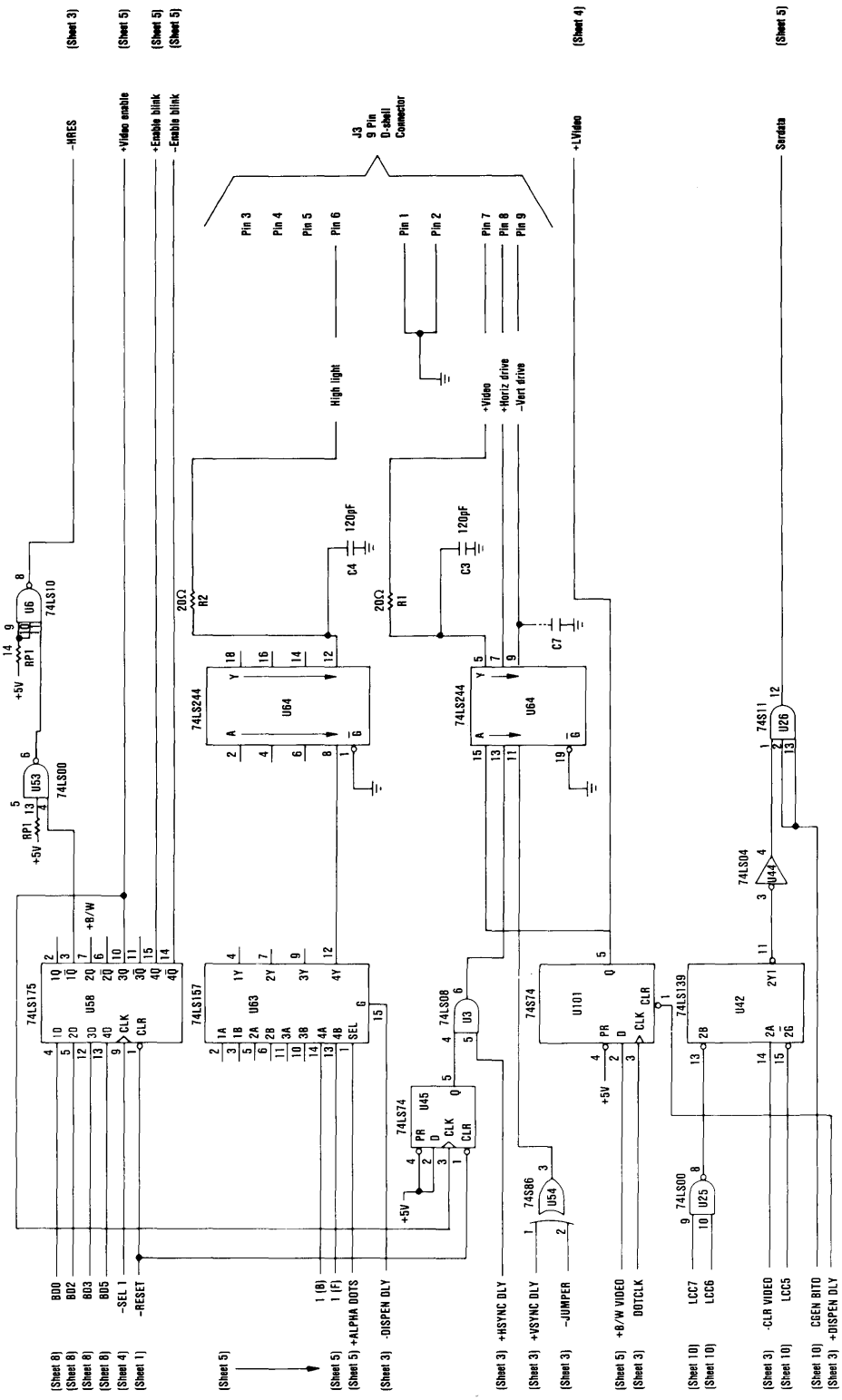
Monochrome display adapter (Part 3 of 10)

Logic Diagrams *(continued)*



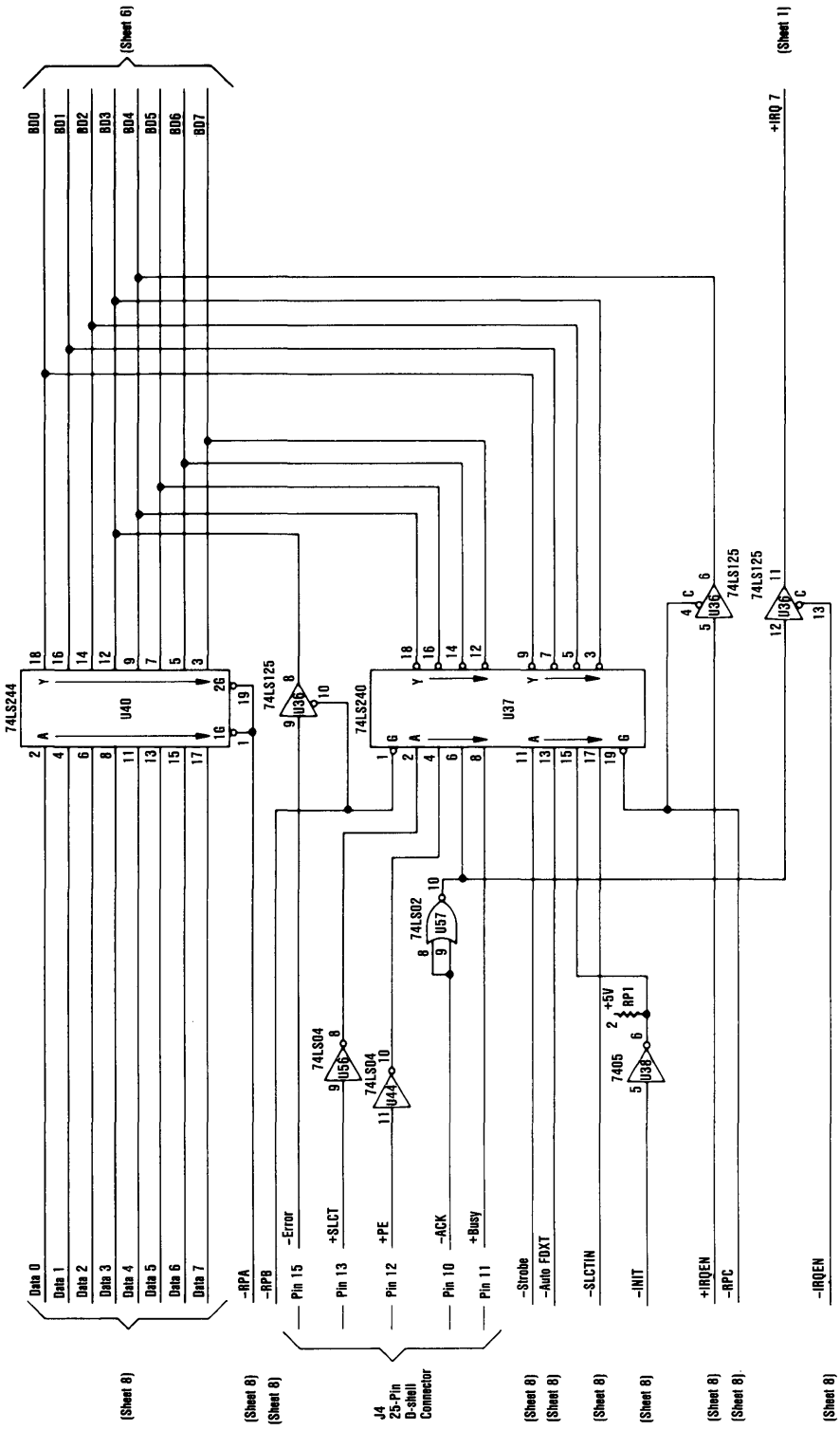
Monochrome display adapter (Part 5 of 10)

Logic Diagrams *(continued)*



Monochrome display adapter (Part 7 of 10)

Logic Diagrams *(continued)*



Monochrome display adapter (Part 9 of 10)

IBM Color/Graphics Monitor Adapter

Contents

IBM Color/Graphics Monitor Adapter

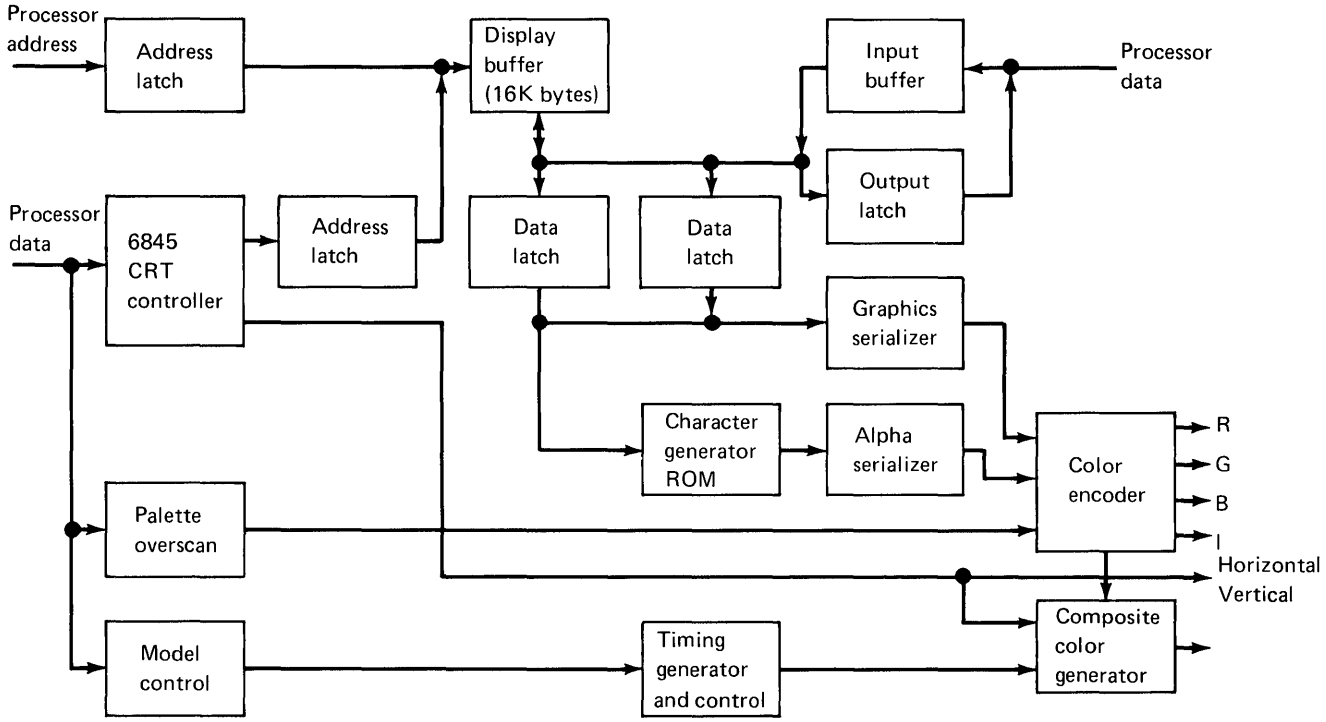
Description

The IBM Color/Graphics Monitor Adapter is designed to attach to the IBM 5532 Industrial Color Display, or to a variety of television-frequency monitors.

The adapter is capable of operating in black-and-white or color. It provides three video interfaces: a composite-video port, a direct-drive port, and a connection interface for driving a user-supplied RF modulator. A light pen interface is also provided.

The adapter has two basic modes of operation: alphanumeric (A/N) and all-points-addressable (APA) graphics. Additional modes are available within the A/N or APA graphics modes. In the A/N mode, the display can be operated in either a 40-column by 25-row mode for a low-resolution monitor, or in an 80-column by 25-row mode for high-resolution monitors. In both modes, characters are defined in an 8-wide by 8-high character box and are 7-wide by 7-high, double dotted characters with one descender. Both uppercase and lowercase characters are supported in all modes.

The character attributes of reverse video, blinking, and highlighting are available in the black-and-white mode. In the color mode, 16 foreground and 8 background colors are available for each character. In addition, blinking on a per-character basis is available.



Color/graphics monitor adapter block diagram

Character Generator

A ROS character generator is used with 8K bytes of storage that cannot be read from or written to under program control. This is a general-purpose ROS character generator with three character fonts. Two character fonts are used on the Color/Graphics Monitor Adapter: a 7-high by 7-wide double-dot font and a 7-high by 5-wide single-dot font. The font is selected by a jumper (P3). The single-dot font is selected by inserting the jumper; the double-dot font is selected by removing the jumper.

Timing Generator

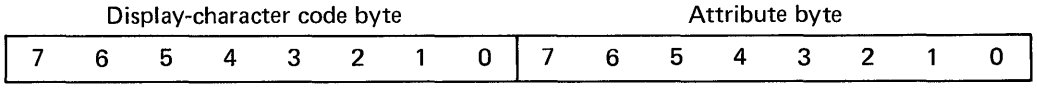
This generator produces the timing signals used by the 6845 CRT Controller and by the dynamic memory. It also solves the processor/graphic controller contentions for access to the display buffer.

Composite Color Generator

This generator produces base-band-video color information.

Alphanumeric Mode

Every display character position in the alphanumeric mode is defined by two bytes in the regen buffer (a part of the monitor adapter), not the system memory. Both the Color/Graphics Monitor Adapter and the Monochrome Display and Printer Adapter use the following 2-byte character-attribute format.



The low-resolution alphanumeric mode:

- Supports home color televisions or low-resolution monitors
- Displays up to 25 rows of 40 characters each
- Has a ROS character generator that contains dot patterns for a maximum of 256 different characters
- Requires 2,000 bytes of read/write memory (on the adapter)
- Has an 8-high by 8-wide character box
- Has two jumper-controlled character fonts available: a 7-high by 5-wide single-dot character font with one descender, and a 7-high by 7-wide double-dotted character font with one descender
- Has one character attribute for each character.

The high-resolution alphanumeric mode:

- Supports the IBM Color Display or other color monitor with direct-drive capability
- Supports a black-and-white composite-video monitor
- Displays up to 25 rows of 80 characters each
- Has a ROS display generator that contains dot patterns for a maximum of 256 characters
- Requires 4,000 bytes of read/write memory (on the adapter)
- Has an 8-high by 8-wide character box
- Has two jumper-controlled character fonts available: a 7-high by 5-wide single-dot character font with one descender, and a 7-high by 7-wide double-dot character font with one descender
- Has one character attribute for each character.

Low-Resolution Color/Graphics Mode

The low-resolution mode supports home televisions or color monitors. This mode is not supported in ROM. The low-resolution mode:

- Contains a maximum of 160 PELs by 100 rows, with each PEL being 2-high by 2-wide
- Specifies one of 16 colors for each PEL by the I, R, G, and B bits
- Requires 16,000 bytes of read/write memory on the adapter
- Uses memory-mapped graphics.

Medium-Resolution Color/Graphics Mode

The medium-resolution mode supports home televisions or color monitors. The medium-resolution mode:

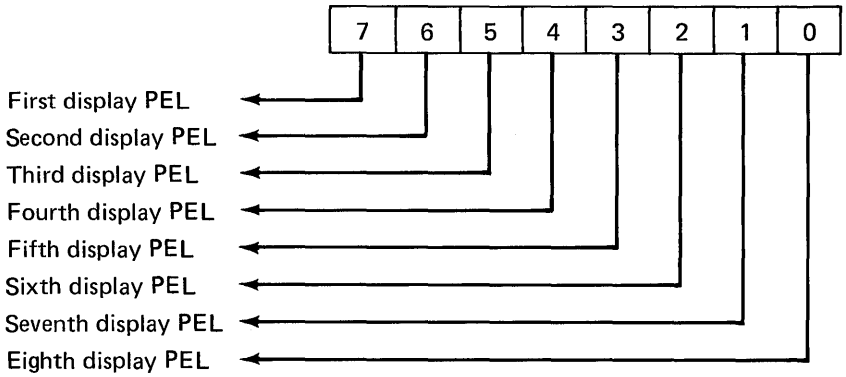
- Contains a maximum of 320 PELs by 200 rows, with each PEL being 1-high by 1-wide
- Preselects one of four colors for each PEL
- Requires 16,000 bytes of read/write memory on the adapter
- Uses memory-mapped graphics
- Formats four PELs per byte in the following manner:

7	6	5	4	3	2	1	0
C1	C0	C1	C0	C1	C0	C1	C0
First Display PEL		Second Display PEL		Third Display PEL		Fourth Display PEL	

High-Resolution Black-and-White Graphics Mode

The high-resolution mode supports color monitors. This mode:

- Contains a maximum of 640 PELs by 200 rows, with each PEL being 1-high by 1-wide.
- Supports black-and-white only.
- Requires 16,000 bytes of read/write memory on the adapter.
- Addressing and mapping procedures are the same as medium-resolution color/graphics, but the data format is different. In this mode, each bit in memory is mapped to a PEL on the screen.
- Formats eight PELs per byte in the following manner:



Programming Considerations

Programming the Mode Control and Status Register

The following I/O devices are defined on the Color/Graphics Monitor Adapter:

Hex address	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Function of register
3D8	1	1	1	1	0	1	1	0	0	0	Mode control register (D0)
3D9	1	1	1	1	0	1	1	0	0	1	Color select register (D0)
3DA	1	1	1	1	0	1	1	0	1	0	Status register (D1)
3DB	1	1	1	1	0	1	1	0	1	1	Clear light pen latch
3DC	1	1	1	1	0	1	1	1	0	0	Preset light pen latch
3D4	1	1	1	1	0	1	0	Z	Z	0	6845 index register
3D5	1	1	1	1	0	1	0	Z	Z	1	6845 data register
Z = don't care condition											

Programming the 6845 CRT Controller

The controller has 19 internal accessible registers, which are used to define and control a raster-scan CRT display. One of these registers, the index register, is used as a pointer to the the other 18 registers. It is a write-only register, which is loaded from the processor by executing an "out" instruction to I/O address hex 3D4. The five least-significant bits of the I/O bus are loaded into the index register.

In order to load any of the other 18 registers, the index register is first loaded with the necessary pointer, then the data register is loaded with the information to be placed in the selected register. The data register is loaded from the processor by executing an "out" instruction to I/O address hex 3D5.

Color-Select Register

The color-select register is a 6-bit output-only register. Its I/O address is hex 3D9, and it can be written to using a processor "out" command. The following are the bit definitions for this register.

Bit 0 Selects blue border color in 40-by-25 alphanumeric mode.
Selects blue background color (C0-C1) in 320-by-200 graphics mode.
Selects blue foreground color in 640-by-200 graphics mode.

Bit 1 Selects green border color in 40-by-25 alphanumeric mode.
Selects green background color (C0-C1) in 320-by-200 graphics mode.
Selects green foreground color in 640-by-200 graphics mode.

Bit 2 Selects red border color in 40-by-25 alphanumeric mode.
Selects red background color (C0-C1) in 320-by-200 graphics mode.
Selects red foreground color in 640-by-200 graphics mode.

Bit 3 Selects intensified border color in 40-by-25 alphanumeric mode.
Selects intensified background color (C0-C1) in 320-by-200 graphics mode.
Selects intensified foreground color in 640-by-200 graphics mode.

Bit 4 Selects alternate, intensified set of colors in the graphics mode.
Selects background colors in the alphanumeric mode.

Mode-Control Register

The mode-control register is a 6-bit output-only register. Its I/O address is hex 3D8, and it can be written to using a processor "out" command. The following are bit definitions for this register.

Bit 0 A 1 selects 80-by-25 alphanumeric mode.
A 0 selects 40-by-25 alphanumeric mode.

Bit 1 A 1 selects 320-by-200 graphics mode.
A 0 selects alphanumeric mode.

Bit 2 A 1 selects black-and-white mode.
A 0 selects color mode.

Bit 3 A 1 enables the video signal. The video signal is disabled when changing modes.

Bit 4 A 1 selects the high-resolution (640-by-200) black-and-white graphics mode. One of eight colors can be selected on direct-drive monitors in this mode by using register hex 3D9.

Bit 5 A 1 will change the character background intensity to the blinking attribute function for alphanumeric modes. When the high-order attribute is not selected, 16 background colors or intensified colors are available. This bit is set to 1 to allow the blinking function.

Status Register

The status register is a 4-bit read-only register. Its I/O address is hex 3DA, and it can be read using the processor "in" instruction. The following are bit definitions for this register.

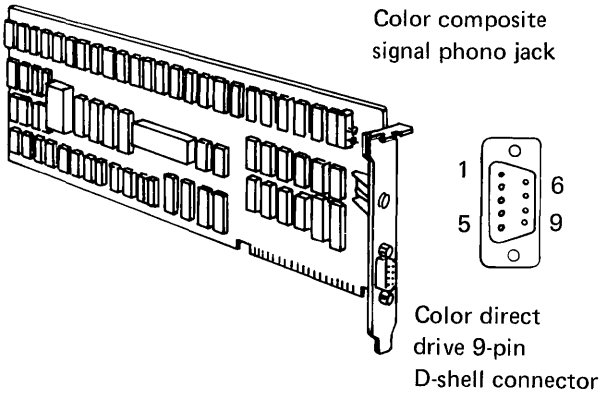
Bit 0 A 1 indicates that a regen-buffer memory access can be made without interfering with the display.

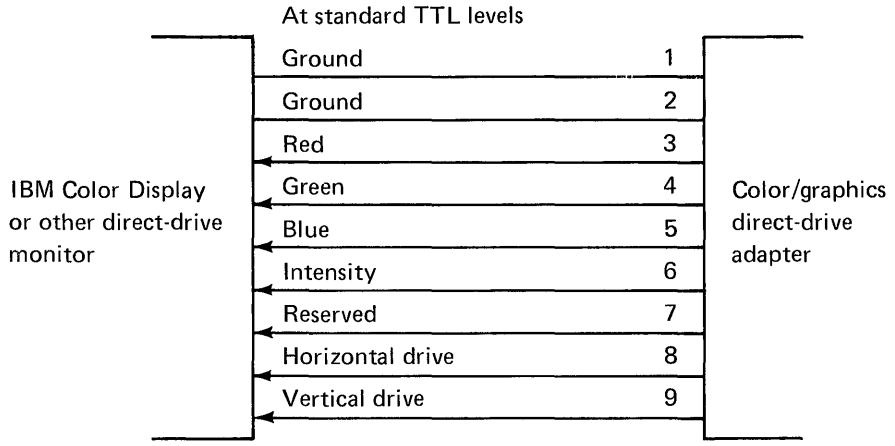
Bit 1 A 1 indicates that a positive-going edge from the light pen has set the light pen's trigger. This trigger is reset when power is turned on and may also be cleared by a processor "out" command to hex address 3DB. No specific data setting is required; the action is address-activated.

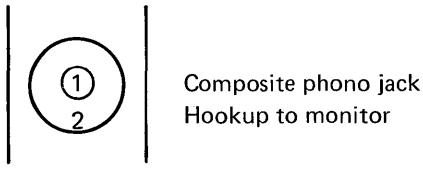
Bit 2 The light pen switch is reflected in this bit. The switch is not latched or debounced. A 0 indicates that the switch is on.

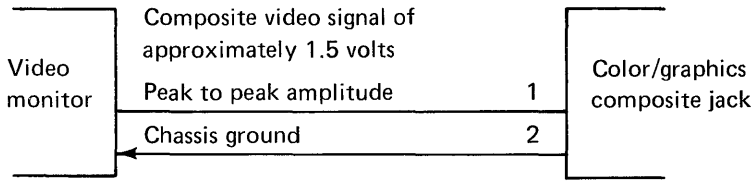
Bit 3 A 1 indicates that the raster is in a vertical retrace mode. Screen-buffer updating can be performed at this time.

Specifications





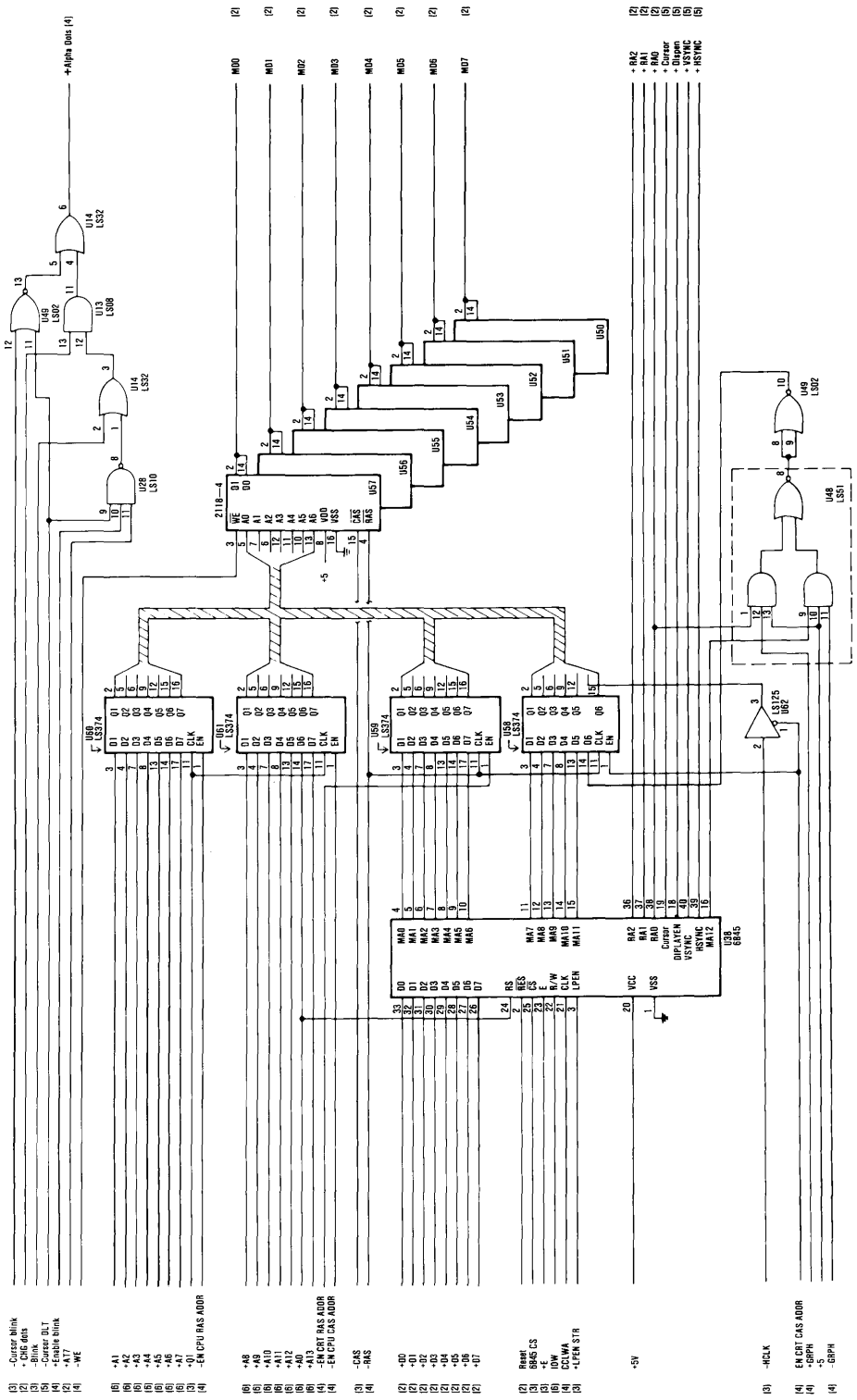




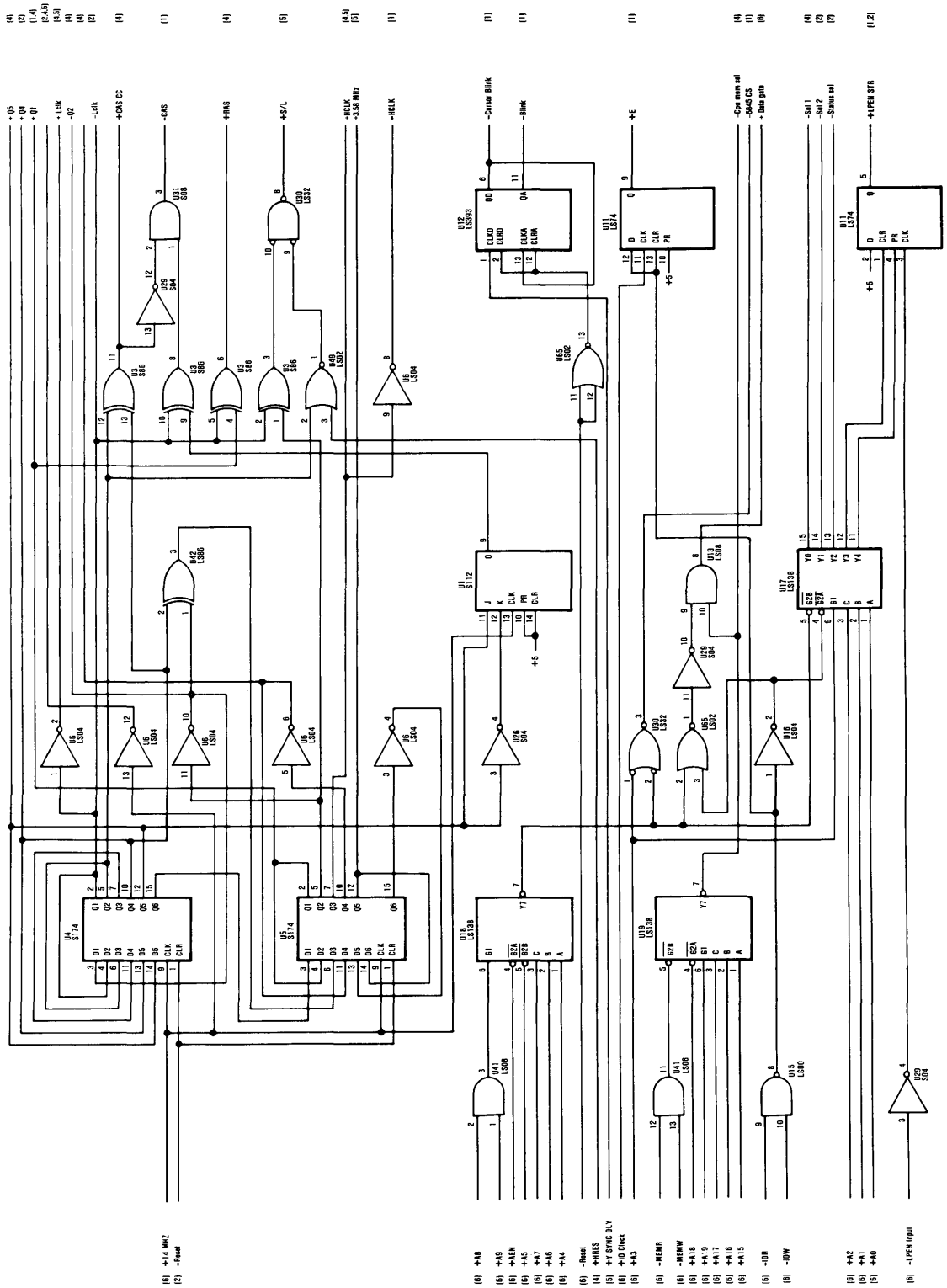
Connector specifications (Part 1 of 2)

Logic Diagrams

The following pages contain the logic diagrams for the IBM Color/Graphics Monitor Adapter.

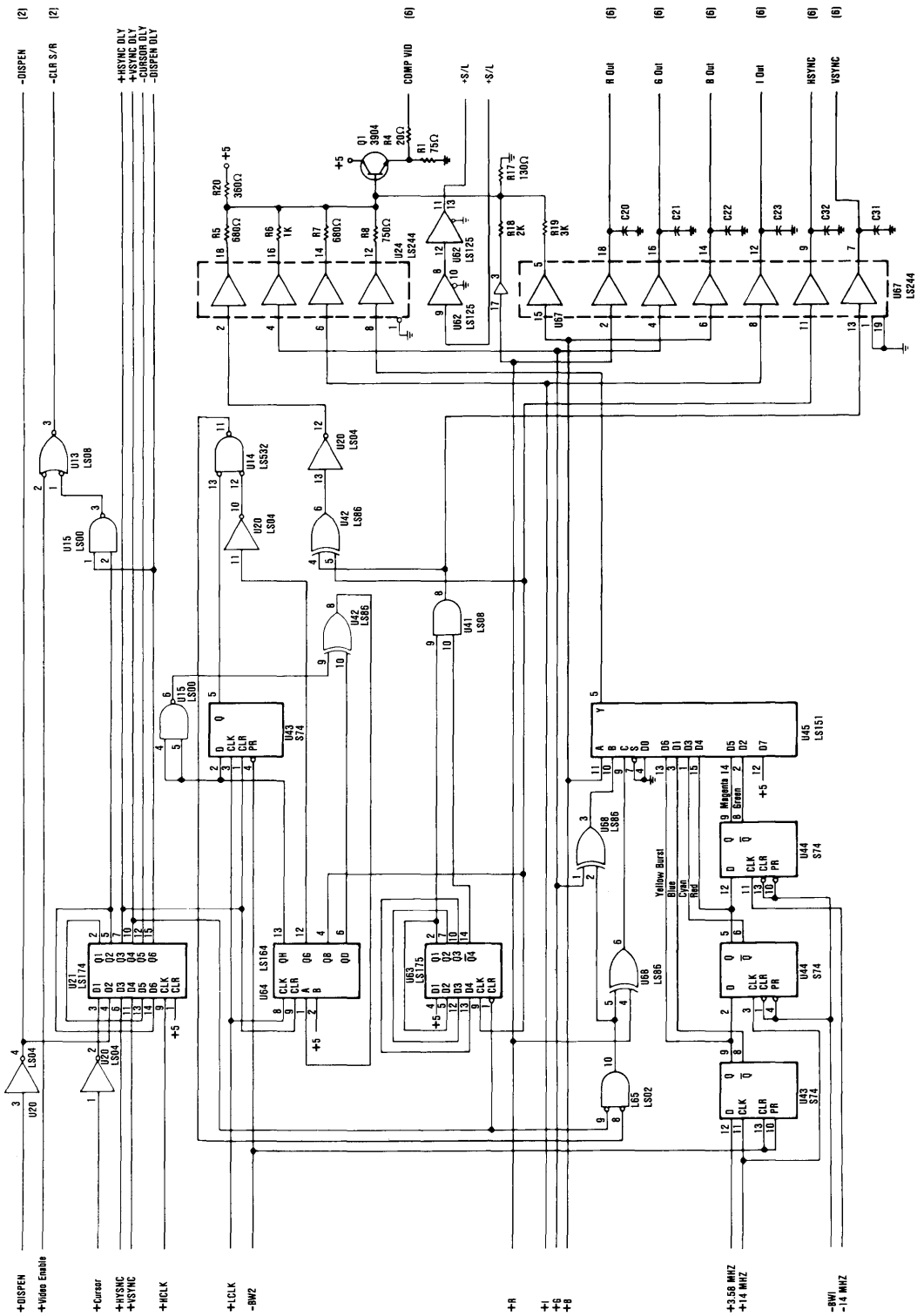


Color/Graphics Monitor Adapter (Part 1 of 6)



Color/Graphics Monitor Adapter (Part 3 of 6)

Logic Diagrams *(continued)*



Color/Graphics Monitor Adapter (Part 5 of 6)

IBM Printer Adapter

Contents

IBM Printer Adapter

Description

The IBM Printer Adapter is specifically designed to attach printers with a parallel port-interface, but it can be used as a general input/output port for any device or application that matches its input/output capabilities. It has 12 TTL-buffer output points, which are latched and can be written and read under program control using the microprocessor In or Out instruction. The adapter also has five steady-state input points that may be read using the microprocessor's In instructions.

In addition, one input can also be used to create a microprocessor interrupt. This interrupt can be enabled and disabled under program control. A reset from the power-on circuit is also ORed with a program output point, allowing a device to receive a "power-on reset" when the system unit's microprocessor is reset.

The input/output signals are made available at the back of the adapter through a right-angle, printed-circuit-board-mounted, 25-pin, D-shell connector. This connector protrudes through the rear panel of the system unit or expansion unit, where a cable may be attached.

When this adapter is used to attach a printer, data or printer commands are loaded into an 8-bit, latched, output port, and the strobe line is activated, writing data to the printer. The program then may read the input ports for printer status indicating when the next character can be written, or it may use the interrupt line to indicate "not busy" to the software.

The output ports may also be read at the card's interface for diagnostic loop functions. This allows faults to be isolated to the adapter or the attaching device.

This same function is also part of the IBM Monochrome Display and Printer Adapter.

Programming Considerations

The Printer Adapter responds to five I/O instructions; two output and three input. The output instructions transfer data into two latches whose outputs are presented on pins of a 25-pin D-shell connector.

Two of the three input instructions allow the system unit's microprocessor to read back the contents of the two latches. The third allows the system unit's microprocessor to read the real-time status from a group of pins on the connector.

A description of each instruction follows.

Printer Adapter			
Output to address hex 378			
Bit 3	Bit 2	Bit 1	Bit 0
Pin 5	Pin 4	Pin 3	Pin 2

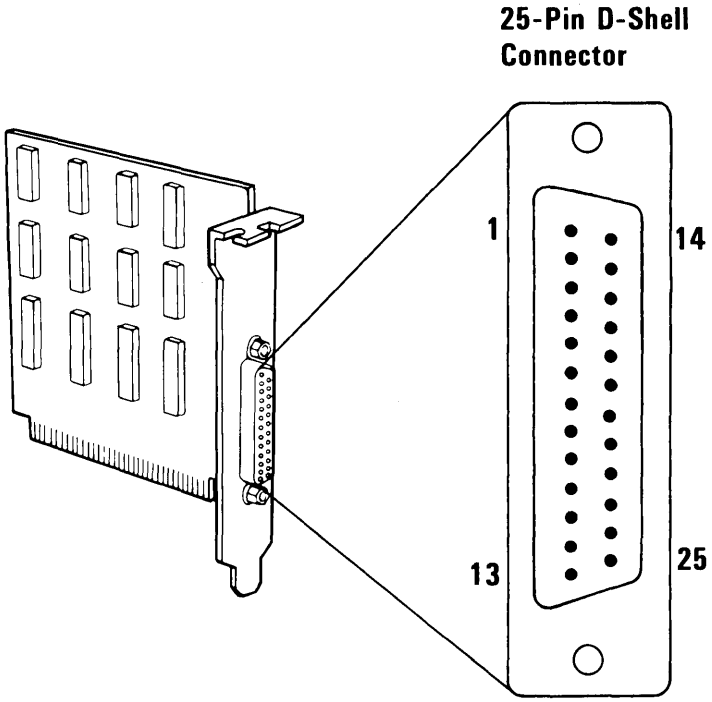
The instruction captures data from the data bus and is present on the respective pins. Each of these pins is capable of sourcing 2.6 mA and sinking 24 mA.

It is essential that the external device does not try to pull these lines to ground.

Printer Adapter			
Output to address hex 37A			
$\overline{\text{Bit 3}}$	Bit 2	$\overline{\text{Bit 1}}$	$\overline{\text{Bit 0}}$
Pin 17	Pin 16	Pin 14	Pin 1

This instruction causes the latch to capture the five least significant bits of the data bus. The four least significant bits present their outputs, or inverted versions of their outputs, to the respective pins as shown in the previous figure. If bit 4 is written as a 1, the card will interrupt the system unit's microprocessor on the condition that pin 10 changes from high to low.

Specifications



At Standard TTL Levels

Signal Name	Adapter Pin Number	
– Strobe	1	
+ Data Bit 0	2	
+ Data Bit 1	3	
+ Data Bit 2	4	
+ Data Bit 3	5	
+ Data Bit 4	6	
+ Data Bit 5	7	
+ Data Bit 6	8	
+ Data Bit 7	9	Printer
– Acknowledge	10	Adapter
+ Busy	11	
+ P.End (out of paper)	12	
+ Select	13	
– Auto Feed	14	
– Error	15	
– Initialize Printer	16	
– Select Input	17	
Ground	18-25	

Printer

Connector Specifications

IBM 5-1/4 Inch Diskette Drive Adapter

Contents

IBM 5-1/4 Inch Diskette Drive Adapter

Description

The IBM 5-1/4 inch Diskette Drive Adapter fits into one of the expansion slots in the system unit. It is connected to one or two diskette drives through an internal, daisy-chained flat cable. The adapter has a connector at the other end that extends through the rear panel of the system unit. This connector has signals for two additional external diskette drives; thus, the 5-1/4 inch diskette drive adapter can attach four 5-1/4 inch drives — two internal and two external.

The adapter is designed for double-density, MFM-coded, diskette drives and uses write precompensation with an analog phase-lock loop for clock and data recovery. The adapter is a general-purpose device using the NEC PD765 or equivalent controller. Therefore, the diskette drive parameters are programmable. In addition, the attachment supports the diskette drive's write-protect feature. The adapter is buffered on the I/O bus and uses the system board's direct memory access (DMA) for record data transfers. An interrupt level also is used to indicate when an operation is complete and that a status condition requires microprocessor attention.

In general, the 5-1/4 inch diskette drive adapter presents a high-level command interface to software I/O drivers.

Programming Considerations

This attachment consists of an 8-bit digital output register in parallel with a NEC PD765 or equivalent floppy disk controller (FDC).

In the following description, drive numbers 0, 1, 2, and 3 are equivalent to drives A, B, C, and D.

Digital-Output Register

The Digital-Output register (DOR) is an output-only register used to control drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface "reset" line. The bits have the following functions:

Bits 0 and 1 These bits are decoded by the hardware to select one drive if its motor is on:

Bit 1 0	Drive
0 0	0 (A)
0 1	1 (B)
1 0	2 (C)
1 1	3 (D)

Bit 2 The FDC is held reset when this bit is clear. It must be set by the program to enable the FDC.

Bit 3 This bit allows the FDC interrupt and DMA requests to be gated onto the I/O interface. If this bit is cleared, the interrupt and DMA request I/O interface drivers are disabled.

Bits 4, 5, 6, and 7 These bits control, respectively, the motors of drives 0, 1, 2 (A, B, C), and 3 (D). If a bit is clear, the associated motor is off, and the drive cannot be selected.

Floppy Disk Controller

The floppy disk controller (FDC) contains two registers that may be accessed by the system-unit microprocessor: a status register and a data register. The 8-bit main status register contains the status information of the FDC and may be accessed at any time. The 8-bit data register (actually consisting of several registers in a stack with only one register presented to the data bus at a time) stores data, commands, parameters, and provides floppy disk drive (FDD) status information. Data bytes are read from or written to the data register in order to program or obtain results after a particular command. The main status register can only be read and is used to facilitate the transfer of data between the system-unit microprocessor and FDC.

Programming Considerations *(continued)*

Symbol	Name	Description
A0	Address line 0	A0 controls selection of main status register (A0 = 0) or data register (A0 = 1).
C	Cylinder number	C stands for the current/selected cylinder (track) number of the medium.
D	Data	D stands for the data pattern that is going to be written into a sector.
D7-D0	Data bus	8-bit data bus, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	Data length	When N is defined as 00, DTL stands for the data length that users are going to read from or write to the sector.
EOT	End of track	EOT stands for the final sector number on a cylinder.
GPL	Gap length	GPL stands for the length of gap 3 (spacing between sectors excluding VCO sync field).
H	Head address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1. (H - HD in all command words).
HLT	Head load time	HLT stands for the head load time in the FDD (4 to 512 ms in 4-ms increments).
HUT	Head unload time	HUT stands for the head unload time after a read or write operation has occurred (0 to 480 ms in 32-ms increments).
MF	FM or MFM mode	If MF is low, FM mode is selected; if it is high, MFM mode is selected only if MFM is implemented.
MT	Multi-track	If MT is high, a multi-track operation is to be performed. (A cylinder under both HD0 and HD1 will be read or written.)
N	Number	N stands for the number of data bytes written in a sector.
NCN	New cylinder number	NCN stands for a new cylinder number, which is going to be reached as a result of the seek operation. (Desired position of the head.)
ND	Non-DMA mode	ND stands for operation in the non-DMA mode.
PCN	Present cylinder number	PCN stands for cylinder number at the completion of sense-interrupt-status command indicating the position of the head at present time.
R	Record	R stands for the sector number, which will be read or written.
R/W	Read/write	R/W stands for either read (R) or write (W) signal.
SC	Sector	SC indicates the number of sectors per cylinder.
SK	Skip	SK stands for skip deleted-data address mark.
SRT	Step rate time	SRT stands for the stepping rate for the FDD (2 to 32 ms in 2-ms increments.
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	STO-3 stand for one of four registers that store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A0 = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.

Symbol Descriptions (Part 1 of 2)

Command Summary

In the following table, 0 indicates "logical 0" for that bit, 1 means "logical 1," and X means "don't care."

Phase	R/W	Data bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Read data								
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information
	W					H				prior to command
	W					R				execution.
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and main system.
Result	R					ST 0				Status information
	R					ST 1				after command execution.
	R					ST 2				
	R					C				Sector ID information
	R					H				after command
	R					R				execution.
	R					N				
		Read deleted data								
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information
	W					H				prior to command
	W					R				execution.
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and main system.
Result	R					ST 0				Status information
	R					ST 1				after command execution.
	R					ST 2				
	R					C				Sector ID information
	R					H				after command
	R					R				execution.
	R					N				

Phase	R/W	Data bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Read a Track								
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information
	W	H								prior to command
	W	R								execution.
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system. FDC reads all of cylinder's contents from index hole to EOT.
Result	R	ST 0								Status information after
	R	ST 1								command execution.
	R	ST 2								
	R	C								Sector ID information
	R	H								after command
	R	R								execution.
	R	N								
		Read ID								
Command	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the cylinder is stored in data register.
Result	R	ST 0								Status information after
	R	ST 1								command execution.
	R	ST 2								
	R	C								Sector ID information
	R	H								during execution
	R	R								phase.
	R	N								

Phase	R/W	Data bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Scan low or equal								
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information
	W	H								prior to command
	W	R								execution.
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST 0								Status information
	R	ST 1								after command execution.
	R	ST 2								
	R	C								Sector ID information
	R	H								after command
	R	R								execution.
	R	N								
		Scan high or equal								
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information
	W	H								prior to command
	W	R								execution.
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST 0								Status information
	R	ST 1								after command execution.
	R	ST 2								
	R	C								Sector ID information
	R	H								after command
	R	R								execution.
	R	N								

Bit			
No.	**Name**	**Symbol**	**Description**
D7 D6	Interrupt Code	IC	D7 = 0 and D6 = 0 Normal termination of command (NT). Command was completed and properly executed. D7 = 0 and D6 = 1 Abnormal termination of command (AT). Execution of command was started, but was not successfully completed. D7 = 1 and D6 = 0 Invalid command issue (IC). Command that was issued was never started. D7 = 1 and D6 = 1 Abnormal termination because, during command execution, the ready signal from FDD changed state.
D5	Seek End	SE	When the FDC completes the seek command, this flag is set to 1 (high).
D4	Equipment Check	EC	If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (recalibrate command), then this flag is set.
D3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to side 1 of a single-sided drive, then this flag is set.
D2	Head Address	HD	This flag is used to indicate the state of the head at interrupt.
D1 D0	Unit Select 1 Unit Select 0	US 1 US 0	These flags are used to indicate a drive unit number at interrupt.

Command status register 0

Bit			
No.	Name	Symbol	Description
D7	–	–	Not used. This bit is always 0 (low).
D6	Control Mark	CM	During execution of the read data or scan command, if the FDC encounters a sector that contains a deleted data address mark, this flag is set.
D5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data, then this flag is set.
D4	Wrong Cylinder	WC	This bit is related to the ND bit, and when the contents of C on the medium are different from that stored in the ID register, this flag is set.
D3	Scan Equal Hit	SH	During execution of the scan command, if the condition of "equal" is satisfied, this flag is set.
D2	Scan Not Satisfied	SN	During execution of the scan command, if the FDC cannot find a sector on the cylinder that meets the condition, then this flag is set.
D1	Bad Cylinder	BC	This bit is related to the ND bit, and when the contents of C on the medium are different from that stored in the ID register, and the contents of C is FF, then this flag is set.
D0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark, then this flag is set.

Command status register 2

Bit			
No.	Name	Symbol	Description
D7	Fault	FT	This bit is the status of the fault signal from the FDD.
D6	Write Protected	WP	This bit is the status of the write-protected signal from the FDD.
D5	Ready	RY	This bit is the status of the ready signal from the FDD.
D4	Track 0	T0	This bit is the status of the track 0 signal from the FDD.
D3	Two Side	TS	This bit is the status of the two-side signal from the FDD.
D2	Head Address	HD	This bit is the status of the side-select signal from the FDD.
D1	Unit Select 1	US 1	This bit is the status of the unit-select-1 signal from the FDD.
D0	Unit Select 0	US 0	This bit is the status of the unit-select-0 signal from the FDD.

Command status register 3

Programming Considerations *(continued)*

Drive Constants

Head load	35 ms
Head settle	15 ms
Motor start	250 ms

Comments

- Head loads with drive select, wait HD load time before R/W.
- Following access, wait HD settle time before R/W.
- Drive motors should be off when not in use. Only A or B and C or D may run simultaneously. Wait motor start time before R/W.
- Motor must be on for drive to be selected.
- Data errors can occur while using a home television as the system display. Placing the TV too close to the diskette area can cause this to occur. To correct the problem, move the TV away from, or to the opposite side of the system unit.

Interface *(continued)*

+IRQ6 (Adapter output, driver: 74LS 3-state): This line is made active when the FDC has completed an operation. It results in an interrupt to a routine that should examine the FDC result bytes to reset the line and determine the ending condition.

Interface *(continued)*

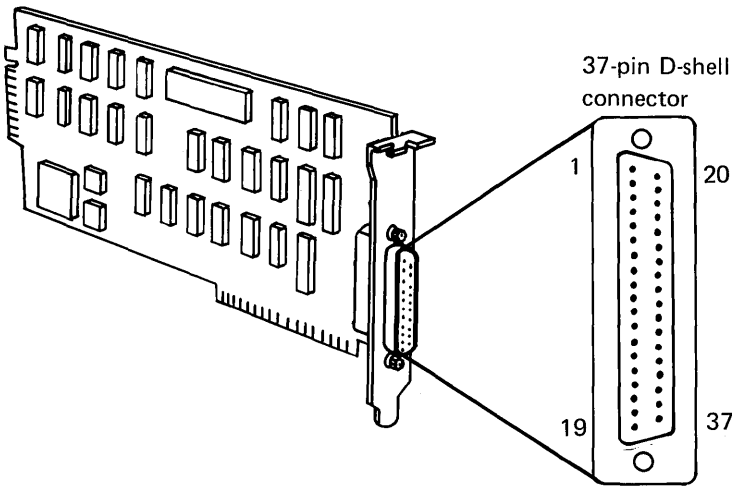
Adapter Outputs

Drive Select A and B	(Driver: 7438): These two lines are used by drives A and B to degate all drivers to the adapter and receivers from the attachment (except "motor enable") when the line associated with a drive is inactive.
Motor Enable A and B	(Driver: 7438): The drive associated with each of these lines must control its spindle motor such that it starts when the line becomes active and stops when the line becomes inactive.
Step	(Driver: 7438): The selected drive moves the read/write head one cylinder in or out per the direction line for each pulse present on this line.
Direction	(Driver: 7438): For each recognized pulse of the "step" line, the read/write head moves one cylinder toward the spindle if this line is active, and away from the spindle if inactive.
Head Select	(Driver: 7438): Head 1 (upper head) will be selected when this line is active (low).
Write Data	(Driver: 7438): For each inactive-to-active transition of this line while "write enable" is active, the selected drive causes a flux change to be stored on the diskette.
Write Enable	(Driver: 7348): The drive disables write current in the head unless this line is active.

Adapter Inputs

Index	The selected drive must supply one pulse per diskette revolution on this line.
Write Protect	The selected drive must make this line active if a write-protected diskette is in the drive.
Track 0	The selected drive must make this line active if the read/write head is over track 0.
Read Data	The selected drive supplies a pulse on this line for each flux change encountered on the diskette.

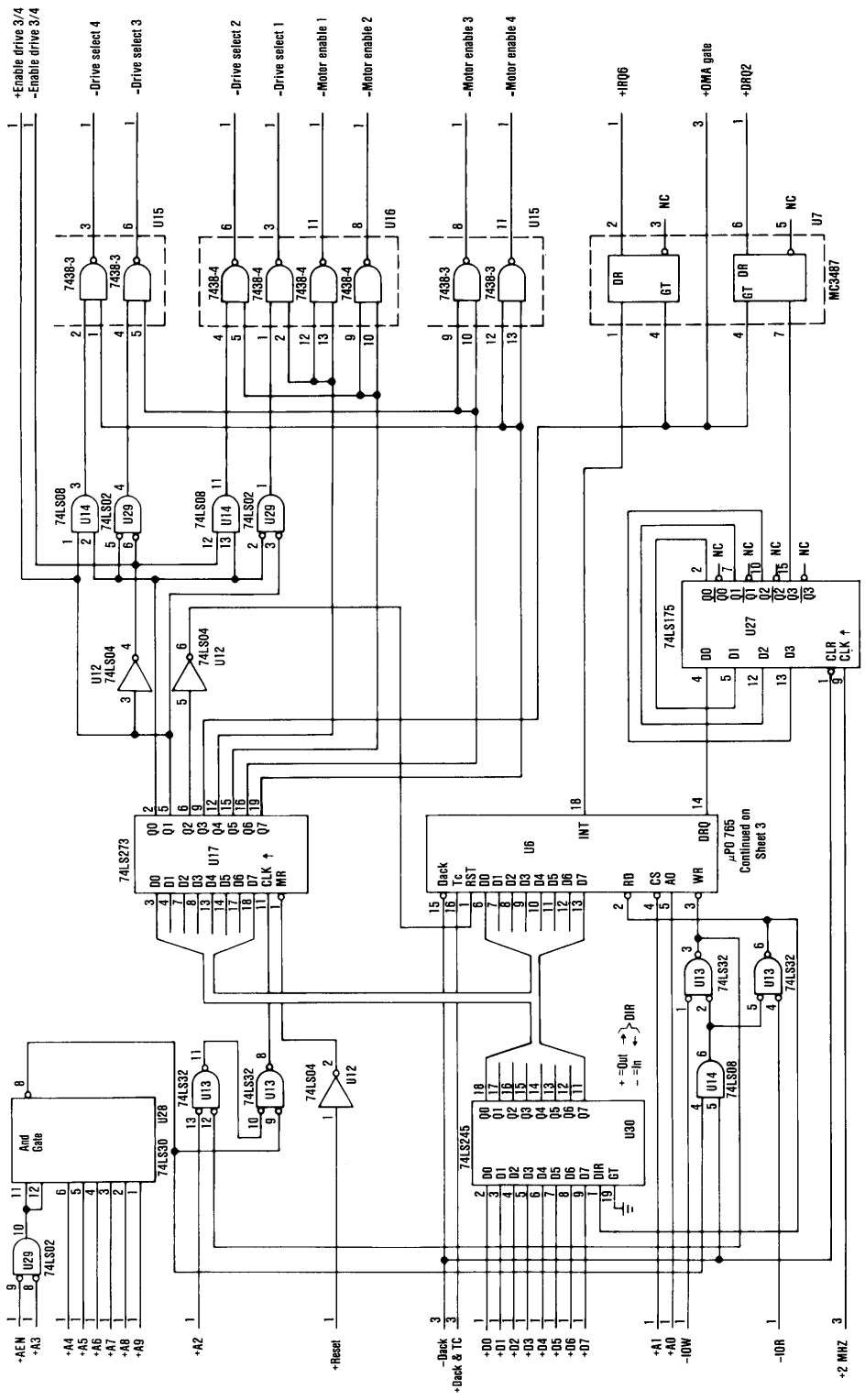
Connector Specifications *(continued)*



	At standard TTL levels	Pin number	
	Unused	1-5	
	Index	6	→
	Motor enable C	7	←
	Drive select D	8	←
	Drive select C	9	←
	Motor enable D	10	←
	Direction (stepper motor)	11	←
External drives	Step pulse	12	← Drive adapter
	Write data	13	←
	Write enable	14	←
	Track 0	15	→
	Write protect	16	→
	Read data	17	→
	Select head 1	18	←
	Ground	20-37	

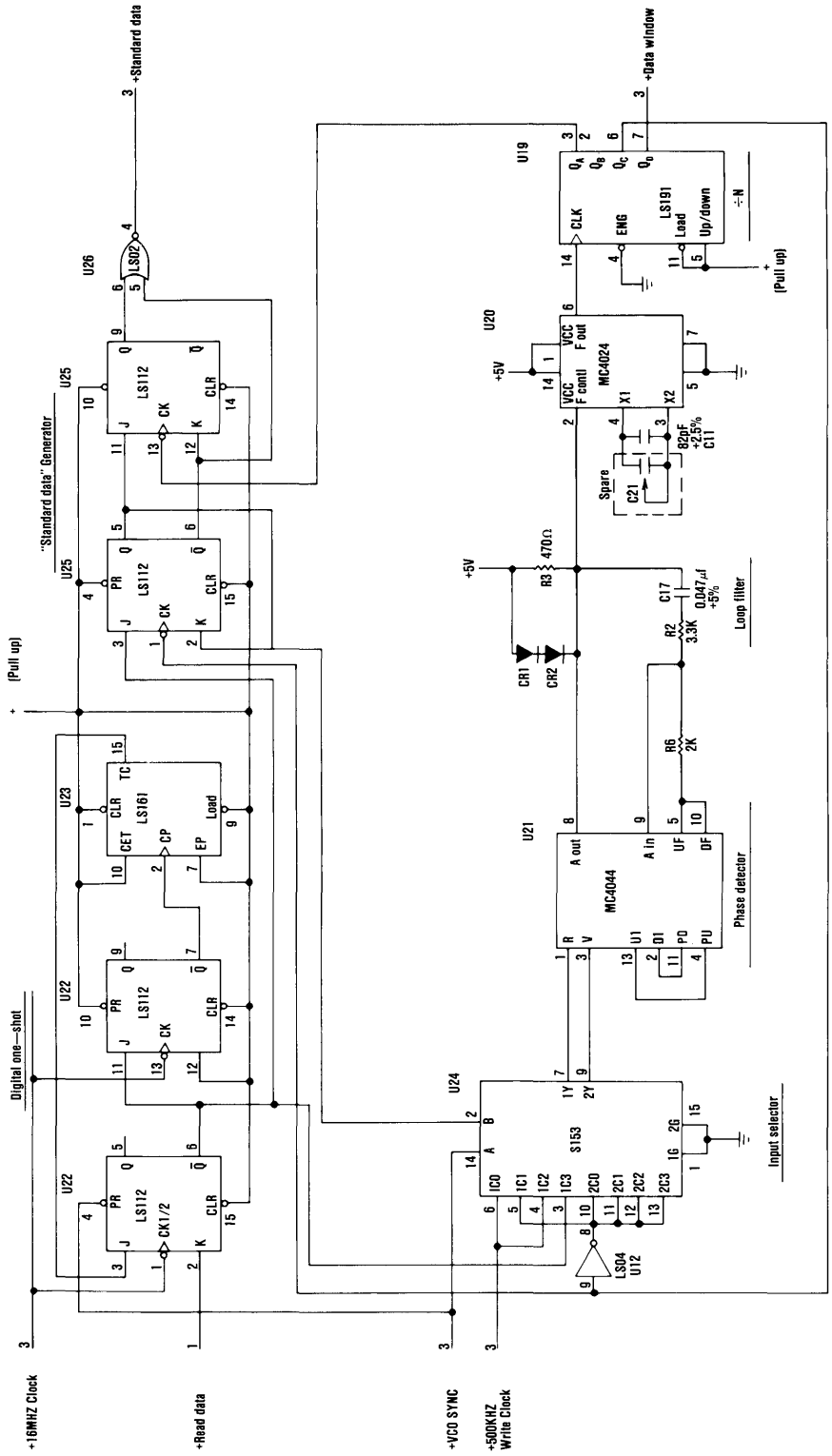
Connector specifications (Part 2 of 2)

Logic Diagrams *(continued)*



5-1/4 inch diskette drive adapter (Part 2 of 4)

Logic Diagrams *(continued)*



5-1/4 inch diskette drive adapter (Part 4 of 4)

IBM Fixed Disk Adapter

Contents

IBM Fixed Disk Adapter

Description

The Fixed Disk Adapter attaches to one or two fixed disk drive units through an internal, daisy-chained, flat cable (data/control cable). Each system supports a maximum of one Fixed Disk Adapter and one fixed disk drive.

The adapter is buffered on the I/O bus and uses the system board's direct memory access (DMA) for record data transfers. An interrupt level also is used to indicate operation completion and status conditions that require microprocessor attention.

The Fixed Disk Adapter provides automatic 11-bit burst error detection and correction in the form of 32-bit error checking and correction (ECC).

The device level control for the Fixed Disk Adapter is contained on a ROM module on the adapter. A listing of this device level control can be found in "BIOS Listing" of this section.

Warning: The last cylinder on the fixed disk drive is reserved for diagnostic use. The diagnostic write test will destroy any data on this cylinder.

Fixed Disk Controller

The disk controller has two registers that may be accessed by the system-unit microprocessor: a status register and a data register. The 8-bit status register contains the status information of the disk controller, and can be accessed at any time. The 8-bit data register (actually consisting of several registers in a stack with only one register presented to the data bus) stores data, commands, and parameters, and provides the disk controller's status information. Data bytes are read from, or written to the data register in order to program or obtain the results after a particular command. The status register is a read-only register that is used to help the transfer of data between the system-unit microprocessor and the disk controller. The controller-select pulse is generated by writing to port address hex 322.

Programming Considerations

Status Register

At the end of all commands from the system board, the disk controller sends a completion status byte to the system board. This byte informs the system-unit microprocessor if an error occurred during the execution of the command. The following shows the format of this byte.

Bit	7	6	5	4	3	2	1	0
	0	0	d	0	0	0	e	0

Bits 0, 1, 2, 3, 4, 6, 7 These bits are set to zero.

Bit 1 When set, this bit shows an error has occurred during command execution.

Bit 5 This bit shows the logical unit number of the drive.

If the interrupts are enabled, the controller sends an interrupt when it is ready to transfer the status byte. Busy from the disk controller is unasserted when the byte is transferred to complete the command.

Disk Controller Error Tables

The following disk controller error tables list the error types and error codes found in byte 0:

	Error type	Error code	
Bits	5 4	3 2 1 0	Description
	0 0	0 0 0 0	The controller did not detect any error during the execution of the previous operation.
	0 0	0 0 0 1	The controller did not detect an index signal from the drive.
	0 0	0 0 1 0	The controller did not get a seek-complete signal from the drive after a seek operation (for all non-buffered step seeks).
	0 0	0 0 1 1	The controller detected a write fault from the drive during the last operation.
	0 0	0 1 0 0	After the controller selected the drive, the drive did not respond with a ready signal.
	0 0	0 1 0 1	Not used.
	0 0	0 1 1 0	After stepping the maximum number of cylinders, the controller did not receive the track 00 signal from the drive.
	0 0	0 1 1 1	Not used.
	0 0	1 0 0 0	The drive is still seeking. This status is reported by the Test Drive Ready command for an overlap seek condition when the drive has not completed the seek. No time-out is measured by the controller for the seek to complete.

	Error type	Error code	
Bits	5 4	3 2 1 0	Description
	1 0	0 0 0 0	Invalid Command: The controller has received an invalid command from the system unit.
	1 0	0 0 0 1	Illegal Disk Address. The controller detected an address that is beyond the maximum range.

	Error type	Error code	
Bits	5 4	3 2 1 0	Description
	1 1	0 0 0 0	RAM Error: The controller detected a data error during the RAM sector-buffer diagnostic test.
	1 1	0 0 0 1	Program Memory Checksum Error: During this internal diagnostic test, the controller detected a program-memory checksum error.
	1 1	0 0 1 0	ECC Polynominal Error: During the controller's internal diagnostic tests, the hardware ECC generator failed its test.

Control Byte

Byte 5 is the control field of the DCB and allows the user to select options for several types of disk drives. The format of this byte is as follows:

Bits	7	6	5	4	3	2	1	0
	r	a	0	0	0	s	s	s

Remarks

r = retries
s = step option
a = retry option on data ECC error

Bit 7 Disables the four retries by the controller on all disk-access commands. Set this bit only during the evaluation of the performance of a disk drive.

Bit 6 If set to 0 during read commands, a reread is attempted when an ECC error occurs. If no error occurs during reread, the command will finish without an error status. If this bit is set to 1, no reread is attempted.

Bits 5, 4, 3 Set to 0.

Bits 2, 1, 0 These bits define the type of drive and select the step option. See the following figure.

Bits 2,	1,	0	
0	0	0	This drive is not specified and defaults to 3 milliseconds per step
0	0	1	N/A
0	1	0	N/A
0	1	1	N/A
1	0	0	200 microseconds per step.
1	0	1	70 microseconds per step (specified by BIOS).
1	1	0	3 milliseconds per step.
1	1	1	3 milliseconds per step.

Format Track (Class 0, Opcode 06)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	0
Byte 1	0	0	d	Head number				
Byte 2	ch	0	0	0	0	0	0	
Byte 3	Cylinder low							
Byte 4	0	0	0	Interleave				
Byte 5	r	0	0	0	0	s	s	s

d = drive (0 or 1)
r = retries
s = step option
ch = cylinder high

Interleave: 1 to 16 for 512-byte sectors

Format Bad Track (Class 0, Opcode 07)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	1
Byte 1	0	0	d	Head number				
Byte 2	ch	0	0	0	0	0	0	
Byte 3	Cylinder low							
Byte 4	0	0	0	Interleave				
Byte 5	r	0	0	0	0	s	s	s

d = drive (0 or 1)
r = retries
s = step option
ch = cylinder high

Interleave: 1 to 16 for 512-byte sectors

Read (Class 0, Opcode 08)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	0	0
Byte 1	0	0	d	Head number				
Byte 2	ch	Sector number						
Byte 3	Cylinder low							
Byte 5	r	a	0	0	0	s	s	s

d = drive (0 or 1)
r = retries
a = retry option on data ECC error
s = step option
ch = cylinder high

Reserved (Class 0, Opcode 09)

This Opcode is not used

Write (Class 0, Opcode 0A)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	1	0
Byte 1	0	0	d	Head number				
Byte 2	ch	Sector number						
Byte 3	Cylinder low							
Byte 4	Block count							
Byte 5	r	0	0	0	0	s	s	s

d = drive (0 or 1)
r = retries
s = step option
ch = cylinder high

Seek (Class 0, Opcode 0B)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	1	1
Byte 1	0	0	d	Head number				
Byte 2	ch	0	0	0	0	0	0	
Byte 3	Cylinder low							
Byte 4	x	x	x	x	x	x	x	x
Byte 5	r	0	0	0	0	s	s	s

d = drive (0 or 1)
r = retries
s = step option
x = don't care
ch = cylinder high

Drive diagnostic (Class 7, Opcode 03)

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	0	1	1
Byte 1	0	0	d	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	r	0	0	0	0	s	s	s

d = drive (0 or 1)
s = step option
r = retries
x = don't care

Controller internal diagnostics (Class 7, Opcode 04)

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	0	0

Bytes 1, 2, 3, 4, 5, = don't care

Read long* (Class 7, Opcode 05)

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	0	1
Byte 1	0	0	d	Head Number				
Byte 2	ch	Sector Number						
Byte 3	Cylinder Low							
Byte 4	Block Count							
Byte 5	r	0	0	0	0	s	s	s

d = drive (0 or 1)
s = step option
r = retries
ch = cylinder high

Write long (Class 7, Opcode 06)**

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	1	0
Byte 1	0	0	d	Head Number				
Byte 2	ch	Sector number						
Byte 3	Cylinder Low							
Byte 4	Block Count							
Byte 5	r	0	0	0	0	s	s	s

d = drive (0 or 1)
s = step option
r = retries
ch = cylinder high

*Returns 512 bytes plus 4 bytes of ECC data per sector.
**Requires 512 bytes plus 4 bytes of ECC data per sector.

Interface

The following lines are used by the disk controller:

A0–A19 Positive true 20-bit address. The least-significant 10 bits contain the I/O address within the range of hex 320 to hex 323 when an I/O read or write is executed by the system unit. The full 20 bits are decoded to address the read-only memory (ROM) between the addresses of hex C8000 and C9FFF.

DO–D7 Positive 8-bit data bus over which data and status information is passed between the system board and the controller.

-IOR Negative true signal that is asserted when the system board reads status or data from the controller under either programmed I/O or DMA control.

-IOW Negative true signal that is asserted when the system board sends a command or data to the controller under either programmed I/O or DMA control.

AEN Positive true signal that is asserted when the DMA in the system board is generating the I/O Read (-IOR) or I/O Write (-IOW) signals and has control of the address and data buses.

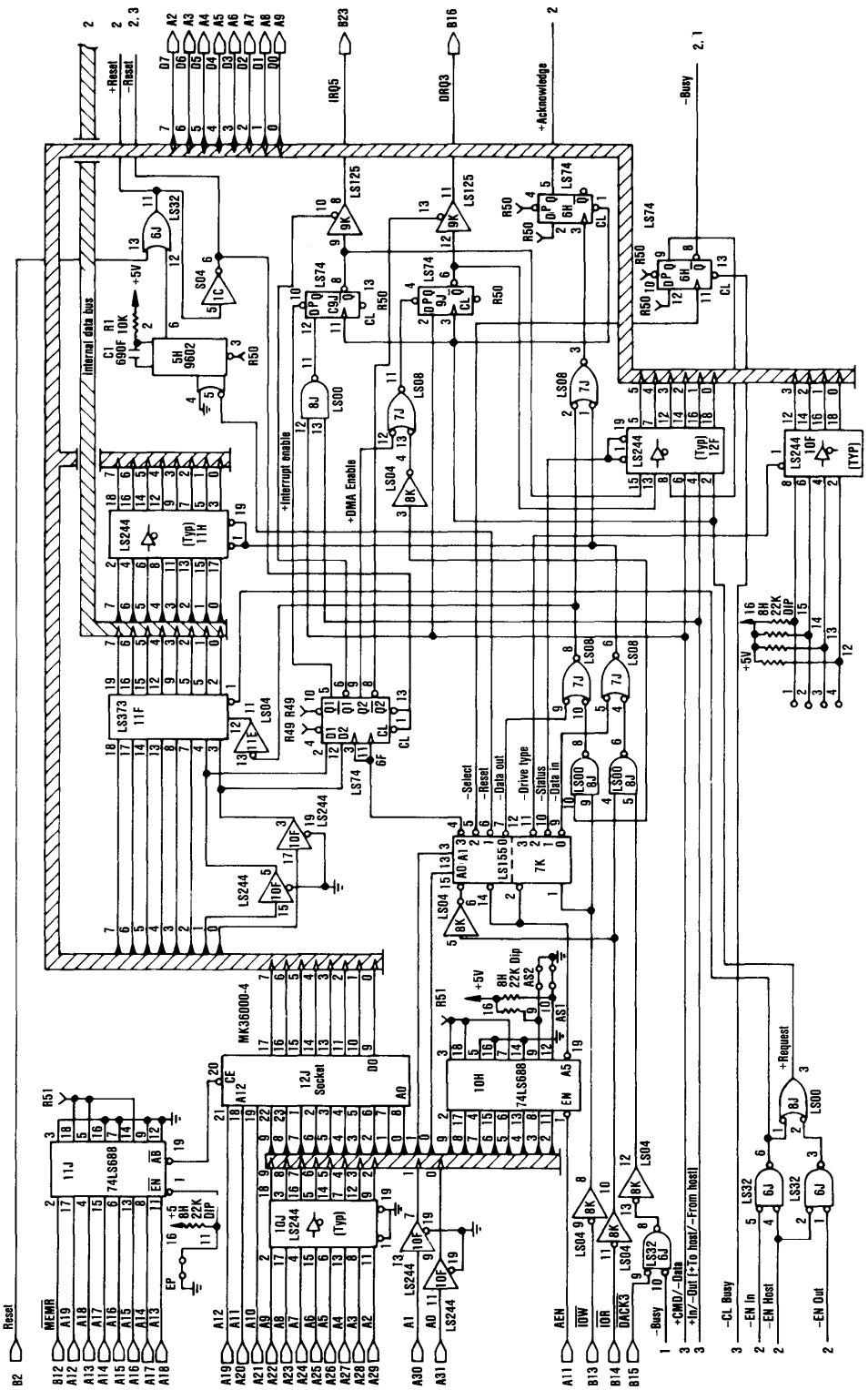
RESET Positive true signal that forces the disk controller to its initial power-up condition.

IRQ 5 Positive true interrupt-request signal that is asserted by the controller when enabled to interrupt the system board on the return ending status byte from the controller.

DRQ 3 Positive true DMA-request signal that is asserted by the controller when data is available for transfer to or from the controller under DMA control. This signal remains active until the system board's DMA channel activates the DMA-acknowledge signal (-DACK 3) in response.

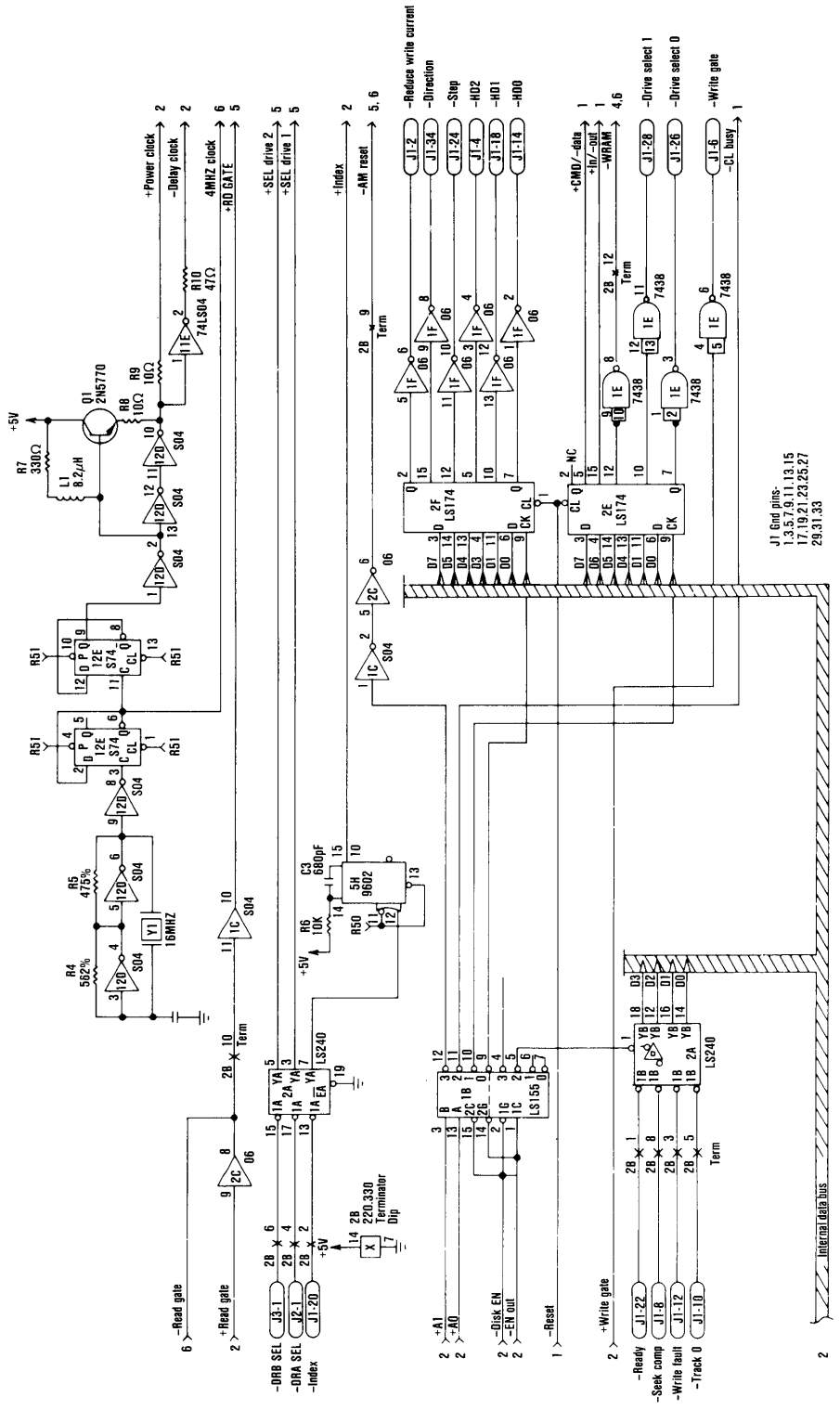
-DACK 3 This signal is true when negative, and is generated by the system board DMA channel in response to a DMA request (DRQ 3).

Logic Diagrams

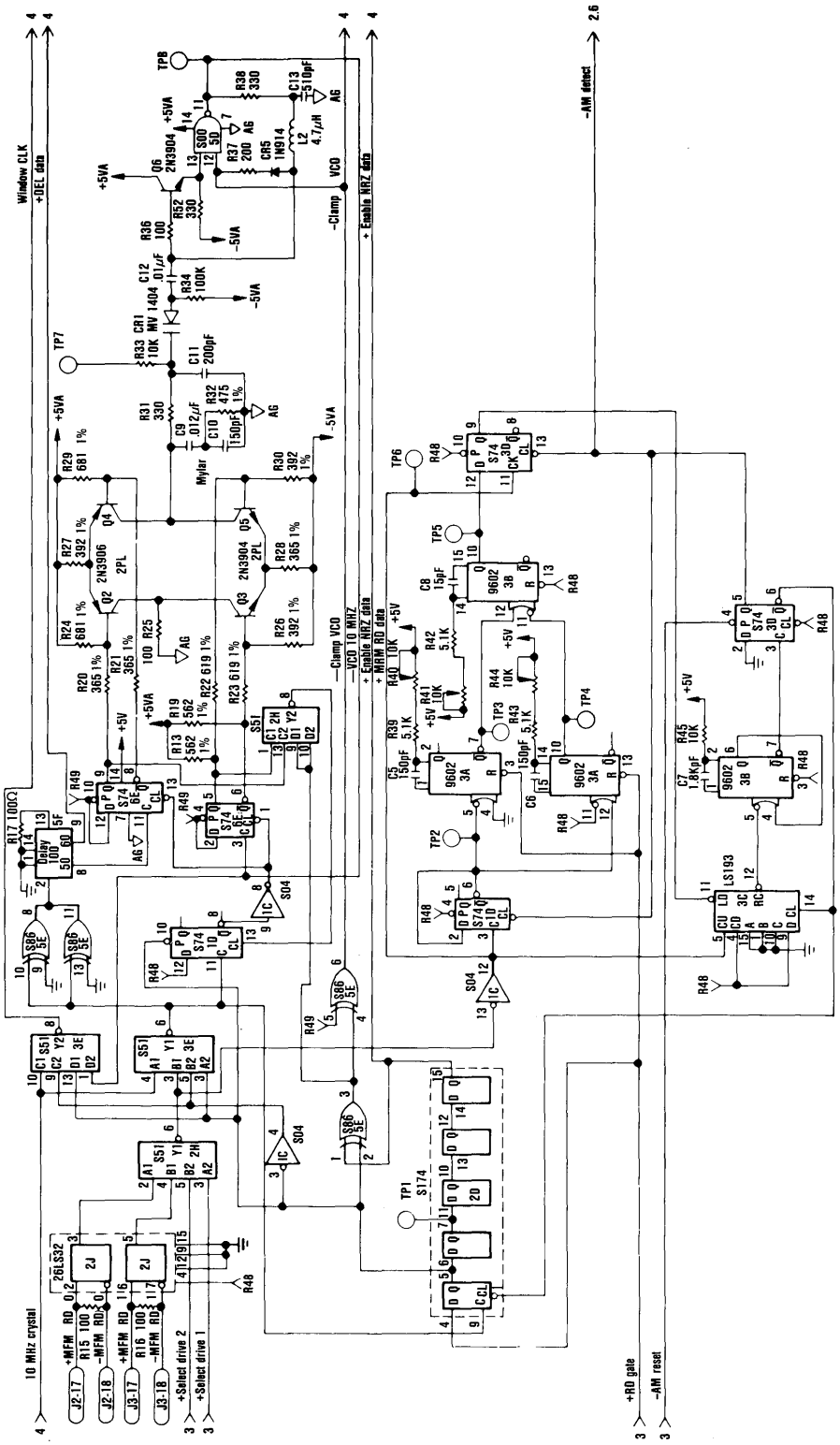


Fixed disk drive adapter (Part 1 of 6)

Logic Diagrams *(continued)*



Logic Diagrams *(continued)*



Fixed disk drive adapter (Part 5 of 6)

BIOS Listing

The BIOS Listing for the IBM Fixed Disk Adapter follows.

```
LOC OBJ                 LINE    SOURCE

                          1     $TITLE(FIXED DISK BIOS FOR IBM DISK CONTROLLER)
                          2
                          3     ;-- INT 13 ------------------------------------------------------
                          4     ;                                                                :
                          5     ; FIXED DISK I/O INTERFACE                                       :
                          6     ;                                                                :
                          7     ;       THIS INTERFACE PROVIDES ACCESS TO 5 1/4" FIXED DISKS     :
                          8     ;       THROUGH THE IBM FIXED DISK CONTROLLER.                   :
                          9     ;                                                                :
                         10     ;---------------------------------------------------------------
                         11
                         12     ;---------------------------------------------------------------
                         13     ;       THE  BIOS ROUTINES ARE MEANT TO BE ACCESSED THROUGH      :
                         14     ;       SOFTWARE INTERRUPTS ONLY.  ANY ADDRESSES PRESENT IN      :
                         15     ;       THE LISTINGS  ARE INCLUDED  ONLY FOR  COMPLETENESS,      :
                         16     ;       NOT FOR  REFERENCE.   APPLICATIONS WHICH  REFERENCE      :
                         17     ;       ABSOLUTE   ADDRESSES   WITHIN   THE   CODE  SEGMENT     :
                         18     ;       VIOLATE THE STRUCTURE AND DESIGN OF BIOS.                :
                         19     ;---------------------------------------------------------------
                         20     ;
                         21     ; INPUT     (AH = HEX VALUE)
                         22     ;
                         23     ;       (AH)=00 RESET DISK (DL = 80H,81H) / DISKETTE
                         24     ;       (AH)=01 READ THE STATUS OF THE LAST DISK OPERATION INTO (AL)
                         25     ;               NOTE: DL < 80H - DISKETTE
                         26     ;                     DL > 80H - DISK
                         27     ;       (AH)=02 READ THE DESIRED SECTORS INTO MEMORY
                         28     ;       (AH)=03 WRITE THE DESIRED SECTORS FROM MEMORY
                         29     ;       (AH)=04 VERIFY THE DESIRED SECTORS
                         30     ;       (AH)=05 FORMAT THE DESIRED TRACK
                         31     ;       (AH)=06 FORMAT THE DESIRED TRACK AND SET BAD SECTOR FLAGS
                         32     ;       (AH)=07 FORMAT THE DRIVE STARTING AT THE DESIRED TRACK
                         33     ;       (AH)=08 RETURN THE CURRENT DRIVE PARAMETERS
                         34     ;
                         35     ;       (AH)=09 INITIALIZE DRIVE PAIR CHARACTERISTICS
                         36     ;               INTERRUPT 41 POINTS TO DATA BLOCK
                         37     ;       (AH)=0A READ LONG
                         38     ;       (AH)=0B WRITE LONG
                         39     ;       NOTE: READ AND WRITE LONG ENCOMPASS 512 + 4 BYTES ECC
                         40     ;       (AH)=0C SEEK
                         41     ;       (AH)=0D ALTERNATE DISK RESET (SEE DL)
                         42     ;       (AH)=0E READ SECTOR BUFFER
                         43     ;       (AH)=0F WRITE SECTOR BUFFER,
                         44     ;               (RECOMMENDED PRACTICE BEFORE FORMATTING)
                         45     ;       (AH)=10 TEST DRIVE READY
                         46     ;       (AH)=11 RECALIBRATE
                         47     ;       (AH)=12 CONTROLLER RAM DIAGNOSTIC
                         48     ;       (AH)=13 DRIVE DIAGNOSTIC
                         49     ;       (AH)=14 CONTROLLER INTERNAL DIAGNOSTIC
                         50     ;
                         51     ;               REGISTERS USED FOR FIXED DISK OPERATIONS
                         52     ;
                         53     ;               (DL)    -  DRIVE NUMBER      (80H-87H FOR DISK, VALUE CHECKED)
                         54     ;               (DH)    -  HEAD NUMBER       (0-7 ALLOWED, NOT VALUE CHECKED)
                         55     ;               (CH)    -  CYLINDER NUMBER   (0-1023, NOT VALUE CHECKED)(SEE CL)
                         56     ;               (CL)    -  SECTOR NUMBER     (1-17, NOT VALUE CHECKED)
                         57     ;
                         58     ;                          NOTE: HIGH 2 BITS OF CYLINDER NUMBER ARE PLACED
                         59     ;                                IN THE HIGH 2 BITS OF THE CL REGISTER
                         60     ;                                (10 BITS TOTAL)
                         61     ;               (AL)    -  NUMBER OF SECTORS (MAXIMUM POSSIBLE RANGE 1-80H,
                         62     ;                                             FOR READ/WRITE LONG 1-79H)
                         63     ;                          (INTERLEAVE VALUE FOR FORMAT 1-16D)
                         64     ;               (ES:BX) - ADDRESS OF BUFFER FOR READS AND WRITES,
                         65     ;                          (NOT REQUIRED FOR VERIFY)
                         66     ;
                         67     ; OUTPUT
                         68     ;       AH = STATUS OF CURRENT OPERATION
                         69     ;            STATUS BITS ARE DEFINED IN THE EQUATES BELOW
                         70     ;       CY = 0  SUCCESSFUL OPERATION (AH=0 ON RETURN)
                         71     ;       CY = 1  FAILED OPERATION (AH HAS ERROR REASON)
                         72     ;
                         73     ;       NOTE: ERROR 11H INDICATES THAT THE DATA READ HAD A RECOVERABLE
                         74     ;               ERROR WHICH WAS CORRECTED BY THE ECC ALGORITHM.  THE DATA
                         75     ;               IS PROBABLY GOOD,   HOWEVER THE BIOS ROUTINE INDICATES AN
                         76     ;               ERROR TO ALLOW THE CONTROLLING PROGRAM A CHANCE TO DECIDE
                         77     ;               FOR  ITSELF.  THE  ERROR  MAY  NOT  RECUR  IF THE DATA IS
```

BIOS Listing *(continued)*

```
LOC OBJ                  LINE    SOURCE

                         155     ;       HF_PORT+0 - READ DATA (FROM CONTROLLER TO CPU)  :
                         156     ;       HF_PORT+1 - READ CONTROLLER HARDWARE STATUS     :
                         157     ;                   (CONTROLLER TO CPU)                 :
                         158     ;       HF_PORT+2 - READ CONFIGURATION SWITCHES         :
                         159     ;       HF_PORT+3 - NOT USED                            :
                         160     ;     > WHEN WRITTEN TO:                          :
                         161     ;       HF_PORT+0 - WRITE DATA (FROM CPU TO CONTROLLER) :
                         162     ;       HF_PORT+1 - CONTROLLER RESET                    :
                         163     ;       HF_PORT+2 - GENERATE CONTROLLER SELECT PULSE    :
                         164     ;       HF_PORT+3 - WRITE PATTERN TO DMA AND INTERRUPT  :
                         165     ;                   MASK REGISTER                       :
                         166     ;                                                       :
                         167     ;-------------------------------------------------------
                         168
  0320                   169     HF_PORT         EQU     0320H           ; DISK PORT
  0008                   170     R1_BUSY         EQU     00001000B       ; DISK PORT 1 BUSY BIT
  0004                   171     R1_BUS          EQU     00000100B       ;             COMMAND/DATA BIT
  0002                   172     R1_IOMODE       EQU     00000010B       ;             MODE BIT
  0001                   173     R1_REQ          EQU     00000001B       ;             REQUEST BIT
                         174
  0047                   175     DMA_READ        EQU     01000111B       ; CHANNEL 3 (047H)
  004B                   176     DMA_WRITE       EQU     01001011B       ; CHANNEL 3 (04BH)
  0000                   177     DMA             EQU     0               ; DMA ADDRESS
  0082                   178     DMA_HIGH        EQU     082H            ; PORT FOR HIGH 4 BITS OF DMA
                         179
  0000                   180     TST_RDY_CMD     EQU     00000000B       ; CNTLR READY (00H)
  0001                   181     RECAL_CMD       EQU     00000001B       ;       RECAL (01H)
  0003                   182     SENSE_CMD       EQU     00000011B       ;       SENSE (03H)
  0004                   183     FMTDRV_CMD      EQU     00000100B       ;       DRIVE (04H)
  0005                   184     CHK_TRK_CMD     EQU     00000101B       ;       T CHK (05H)
  0006                   185     FMTTRK_CMD      EQU     00000110B       ;       TRACK (06H)
  0007                   186     FMTBAD_CMD      EQU     00000111B       ;       BAD   (07H)
  0008                   187     READ_CMD        EQU     00001000B       ;       READ  (08H)
  000A                   188     WRITE_CMD       EQU     00001010B       ;       WRITE (0AH)
  000B                   189     SEEK_CMD        EQU     00001011B       ;       SEEK  (0BH)
  000C                   190     INIT_DRV_CMD    EQU     00001100B       ;       INIT  (0CH)
  000D                   191     RD_ECC_CMD      EQU     00001101B       ;       BURST (0DH)
  000E                   192     RD_BUFF_CMD     EQU     00001110B       ;       BUFFR (0EH)
  000F                   193     WR_BUFF_CMD     EQU     00001111B       ;       BUFFR (0FH)
  00E0                   194     RAM_DIAG_CMD    EQU     11100000B       ;       RAM   (E0H)
  00E3                   195     CHK_DRV_CMD     EQU     11100011B       ;       DRV   (E3H)
  00E4                   196     CNTLR_DIAG_CMD  EQU     11100100B       ;       CNTLR (E4H)
  00E5                   197     RD_LONG_CMD     EQU     11100101B       ;       RLONG (E5H)
  00E6                   198     WR_LONG_CMD     EQU     11100110B       ;       WLONG (E6H)
                         199
  0020                   200     INT_CTL_PORT    EQU     20H             ; 8259 CONTROL PORT
  0020                   201     EOI             EQU     20H             ; END OF INTERRUPT COMMAND
                         202
  0008                   203     MAX_FILE        EQU     8
  0002                   204     S_MAX_FILE      EQU     2
                         205
                         206             ASSUME  CS:CODE
0000                     207             ORG     0H
0000 55                  208             DB      055H                    ; GENERIC BIOS HEADER
0001 AA                  209             DB      0AAH
0002 10                  210             DB      16D
                         211
                         212     ;--------------------------------------------------------------
                         213     ; FIXED DISK I/O SETUP                                       :
                         214     ;                                                            :
                         215     ;  -  ESTABLISH TRANSFER VECTORS FOR THE FIXED DISK         :
                         216     ;  -  PERFORM POWER ON DIAGNOSTICS                          :
                         217     ;     SHOULD AN ERROR OCCUR A "1701" MESSAGE IS DISPLAYED    :
                         218     ;                                                            :
                         219     ;--------------------------------------------------------------
                         220
0003                     221     DISK_SETUP      PROC    FAR
0003 EB1E                222             JMP     SHORT   L3
0005 35303030303539      223             DB      '5000059 (C)COPYRIGHT  IBM 1982'        ; COPYRIGHT NOTICE
     20284329434F50
     59524947485420
     2049424D203139
     3832
0023                     224     L3:
                         225             ASSUME  DS:DUMMY
0023 2BC0                226             SUB     AX,AX                                   ; ZERO
0025 8ED8                227             MOV     DS,AX
```

BIOS Listing *(continued)*

```
LOC OBJ                 LINE    SOURCE

00E5 8EC0               305             MOV     ES,AX                   ; SET SEGMENT
00E7 2BDB               306             SUB     BX,BX
00E9 B8000F             307             MOV     AX,0F00H                ; WRITE SECTOR BUFFER
00EC CD13               308             INT     13H
00EE 7252               309             JC      ERROR_EX
                        310
00F0 FE067500           311             INC     HF_NUM                  ; DRIVE ZERO RESPONDED
                        312
00F4 BA1302             313             MOV     DX,213H                 ; EXPANSION BOX
00F7 B000               314             MOV     AL,0
00F9 EE                 315             OUT     DX,AL                   ; TURN BOX OFF
00FA BA2103             316             MOV     DX,321H                 ; TEST IF CONTROLLER
00FD EC                 317             IN      AL,DX                   ; ... IS IN THE SYSTEM UNIT
00FE 240F               318             AND     AL,0FH
0100 3C0F               319             CMP     AL,0FH
0102 7406               320             JE      BOX_ON
0104 C7066C00A401       321             MOV     TIMER_LOW,420D          ; CONTROLLER IS IN SYSTEM UNIT
010A                    322     BOX_ON:
010A BA1302             323             MOV     DX,213H                 ; EXPANSION BOX
010D B0FF               324             MOV     AL,0FFH
010F EE                 325             OUT     DX,AL                   ; TURN BOX ON
                        326
0110 B90100             327             MOV     CX,1                    ; ATTEMPT NEXT DRIVES
0113 BA8100             328             MOV     DX,081H
0116                    329     P3:
0116 2BC0               330             SUB     AX,AX                   ; RESET
0118 CD13               331             INT     13H
011A 7240               332             JC      POD_DONE
011C B80011             333             MOV     AX,01100H               ; RECAL
011F CD13               334             INT     13H
0121 730B               335             JNC     P5
0123 A16C00             336             MOV     AX,TIMER_LOW
0126 3DBE01             337             CMP     AX,446D                 ; 25 SECONDS
0129 72EB               338             JB      P3
012B EB2F90             339             JMP     POD_DONE
012E                    340     P5:
012E B80009             341             MOV     AX,0900H                ; INITIALIZE CHARACTERISTICS
0131 CD13               342             INT     13H
0133 7227               343             JC      POD_DONE
0135 FE067500           344             INC     HF_NUM                  ; TALLY ANOTHER DRIVE
0139 81FA8100           345             CMP     DX,(80H + S_MAX_FILE - 1)
013D 731D               346             JAE     POD_DONE
013F 42                 347             INC     DX
0140 EBD4               348             JMP     P3
                        349
                        350     ;----- POD ERROR
                        351
0142                    352     ERROR_EX:
0142 BD0F00             353             MOV     BP,0FH                  ; POD ERROR FLAG
0145 2BC0               354             SUB     AX,AX
0147 8BF0               355             MOV     SI,AX
0149 B9060090           356             MOV     CX,F17L                 ; MESSAGE CHARACTER COUNT
014D B700               357             MOV     BH,0                    ; PAGE ZERO
014F                    358     OUT_CH:
014F 2E8A846801         359             MOV     AL,CS:F17[SI]     ; GET BYTE
0154 B40E               360             MOV     AH,14D                  ; VIDEO OUT
0156 CD10               361             INT     10H                     ; DISPLAY CHARACTER
0158 46                 362             INC     SI                      ; NEXT CHAR
0159 E2F4               363             LOOP    OUT_CH                  ; DO MORE
015B F9                 364             STC
015C                    365     POD_DONE:
015C FA                 366             CLI
015D E421               367             IN      AL,021H                 ; BE SURE TIMER IS DISABLED
015F 0C01               368             OR      AL,01H
0161 E621               369             OUT     021H,AL
0163 FB                 370             STI
0164 E8A500             371             CALL    DSBL
0167 CB                 372             RET
                        373
0168 31373031           374     F17     DB      '1701',0DH,0AH
016C 0D
016D 0A
  0006                  375     F17L    EQU     $-F17
                        376
016E                    377     HD_RESET_1      PROC    NEAR
016E 51                 378             PUSH    CX                      ; SAVE REGISTER
016F 52                 379             PUSH    DX
```

BIOS Listing *(continued)*

```
LOC OBJ                 LINE    SOURCE

01C8 EA007C0000          457            JMP     BOOT_LOCN
                         458
                         459    ;----- ATTEMPT BOOTSTRAP FROM FIXED DISK
                         460
01CD                     461    H5:
01CD 2BC0                462            SUB     AX,AX                   ; RESET DISKETTE
01CF 2BD2                463            SUB     DX,DX
01D1 CD13                464            INT     13H
01D3 B90300              465            MOV     CX,3                    ; SET RETRY COUNT
01D6                     466    H6:                                     ; IPL_SYSTEM
01D6 51                  467            PUSH    CX                      ; SAVE RETRY COUNT
01D7 BA8000              468            MOV     DX,0080H                ; FIXED DISK ZERO
01DA 2BC0                469            SUB     AX,AX                   ; RESET THE FIXED DISK
01DC CD13                470            INT     13H                     ; FILE IO CALL
01DE 7212                471            JC      H7                      ; IF ERROR, TRY AGAIN
01E0 B80102              472            MOV     AX,0201H                ; READ IN THE SINGLE SECTOR
01E3 2BDB                473            SUB     BX,BX
01E5 8EC3                474            MOV     ES,BX
01E7 BB007C              475            MOV     BX,OFFSET BOOT_LOCN     ; TO THE BOOT LOCATION
01EA BA8000              476            MOV     DX,80H                  ; DRIVE NUMBER
01ED B90100              477            MOV     CX,1                    ; SECTOR 1, TRACK 0
01F0 CD13                478            INT     13H                     ; FILE IO CALL
01F2 59                  479    H7: POP   CX                            ; RECOVER RETRY COUNT
01F3 7208                480            JC      H8
01F5 A1FE7D              481            MOV     AX,WORD PTR BOOT_LOCN+510D
01F8 3D55AA              482            CMP     AX,0AA55H               ; TEST FOR GENERIC BOOT BLOCK
01FB 74CB                483            JZ      H4
01FD                     484    H8:
01FD E2D7                485            LOOP    H6                      ; DO IT FOR RETRY TIMES
                         486
                         487    ;------ UNABLE TO IPL FROM THE DISKETTE OR FIXED DISK
                         488
01FF CD18                489            INT     18H                     ; RESIDENT BASIC
                         490
0201                     491    DISKETTE_TBL:
                         492
0201 CF                  493            DB      11001111B               ; SRT=C, HD UNLOAD=OF - 1ST SPEC BYTE
0202 02                  494            DB      2                       ; HD LOAD=1, MODE=DMA - 2ND SPEC BYTE
0203 25                  495            DB      25H                     ; WAIT AFTER OPN TIL MOTOR OFF
0204 02                  496            DB      2                       ; 512 BYTES PER SECTOR
0205 08                  497            DB      8                       ; EOT (LAST SECTOR ON TRACK)
0206 2A                  498            DB      02AH                    ; GAP LENGTH
0207 FF                  499            DB      0FFH                    ; DTL
0208 50                  500            DB      050H                    ; GAP LENGTH FOR FORMAT
0209 F6                  501            DB      0F6H                    ; FILL BYTE FOR FORMAT
020A 19                  502            DB      25                      ; HEAD SETTLE TIME (MILLISECONDS)
020B 04                  503            DB      4                       ; MOTOR START TIME (1/8 SECOND)
                         504
                         505    ;----- MAKE SURE THAT ALL HOUSEKEEPING IS DONE BEFORE EXIT
                         506
020C                     507    DSBL    PROC    NEAR
                         508            ASSUME  DS:DATA
020C 1E                  509            PUSH    DS                      ; SAVE SEGMENT
020D B84000              510            MOV     AX,DATA
0210 8ED8                511            MOV     DS,AX
                         512
0212 8A267700            513            MOV     AH,PORT_OFF
0216 50                  514            PUSH    AX                      ; SAVE OFFSET
                         515
0217 C606770000          516            MOV     PORT_OFF,0H
021C E86905              517            CALL    PORT_3
021F 2AC0                518            SUB     AL,AL
0221 EE                  519            OUT     DX,AL                   ; RESET INT/DMA MASK
0222 C606770004          520            MOV     PORT_OFF,4H
0227 E85E05              521            CALL    PORT_3
022A 2AC0                522            SUB     AL,AL
022C EE                  523            OUT     DX,AL                   ; RESET INT/DMA MASK
022D C606770008          524            MOV     PORT_OFF,8H
0232 E85305              525            CALL    PORT_3
0235 2AC0                526            SUB     AL,AL
0237 EE                  527            OUT     DX,AL                   ; RESET INT/DMA MASK
0238 C60677000C          528            MOV     PORT_OFF,0CH
023D E84805              529            CALL    PORT_3
0240 2AC0                530            SUB     AL,AL
0242 EE                  531            OUT     DX,AL                   ; RESET INT/DMA MASK
0243 B007                532            MOV     AL,07H
0245 E60A                533            OUT     DMA+10,AL               ; SET DMA MODE TO DISABLE
```

BIOS Listing *(continued)*

```
LOC OBJ                 LINE    SOURCE

02B4 F204               611             DW      DISK_SEEK               ; 00CH
02B6 3803               612             DW      DISK_RESET              ; 00DH
02B8 F904               613             DW      RD_BUFF                 ; 00EH
02BA 0705               614             DW      WR_BUFF                 ; 00FH
02BC 1505               615             DW      TST_RDY                 ; 010H
02BE 1C05               616             DW      HDISK_RECAL             ; 011H
02C0 2305               617             DW      RAM_DIAG                ; 012H
02C2 2A05               618             DW      CHK_DRV                 ; 013H
02C4 3105               619             DW      CNTLR_DIAG              ; 014H
  002A                  620     M1L     EQU     $-M1
                        621
02C6                    622     SETUP_A PROC    NEAR
                        623
02C6 C606740000         624             MOV     DISK_STATUS,0           ; RESET THE STATUS INDICATOR
02CB 51                 625             PUSH    CX                      ; SAVE CX
                        626
                        627     ;----- CALCULATE THE PORT OFFSET
                        628
02CC 8AEA               629             MOV     CH,DL                   ; SAVE DL
02CE 80CA01             630             OR      DL,1
02D1 FECA               631             DEC     DL
02D3 D0E2               632             SHL     DL,1                    ; GENERATE OFFSET
02D5 88167700           633             MOV     PORT_OFF,DL             ; STORE OFFSET
02D9 8AD5               634             MOV     DL,CH                   ; RESTORE DL
02DB 80E201             635             AND     DL,1
                        636
02DE B105               637             MOV     CL,5                    ; SHIFT COUNT
02E0 D2E2               638             SHL     DL,CL                   ; DRIVE NUMBER (0,1)
02E2 0AD6               639             OR      DL,DH                   ; HEAD NUMBER
02E4 88164300           640             MOV     CMD_BLOCK+1,DL
02E8 59                 641             POP     CX
02E9 C3                 642             RET
                        643     SETUP_A ENDP
                        644
02EA                    645     DISK_IO_CONT    PROC    NEAR
02EA 50                 646             PUSH    AX
02EB B84000             647             MOV     AX,DATA
02EE 8ED8               648             MOV     DS,AX                   ; ESTABLISH SEGMENT
02F0 58                 649             POP     AX
02F1 80FC01             650             CMP     AH,01H                  ; RETURN STATUS
02F4 7503               651             JNZ     A4
02F6 EB5590             652             JMP     RETURN_STATUS
02F9                    653     A4:
02F9 80EA80             654             SUB     DL,80H                  ; CONVERT DRIVE NUMBER TO 0 BASED RANGE
02FC 80FA08             655             CMP     DL,MAX_FILE             ; LEGAL DRIVE TEST
02FF 732F               656             JAE     BAD_COMMAND
                        657
0301 E8C2FF             658             CALL    SETUP_A
                        659
                        660     ;----- SET UP COMMAND BLOCK
                        661
0304 FEC9               662             DEC     CL                      ; SECTORS 0-16 FOR CONTROLLER
0306 C606420000         663             MOV     CMD_BLOCK+0,0
030B 880E4400           664             MOV     CMD_BLOCK+2,CL          ; SECTOR AND HIGH 2 BITS CYLINDER
030F 882E4500           665             MOV     CMD_BLOCK+3,CH          ; CYLINDER
0313 A24600             666             MOV     CMD_BLOCK+4,AL          ; INTERLEAVE / BLOCK COUNT
0316 A07600             667             MOV     AL,CONTROL_BYTE         ; CONTROL BYTE (STEP OPTION)
0319 A24700             668             MOV     CMD_BLOCK+5,AL
031C 50                 669             PUSH    AX                      ; SAVE AX
031D 8AC4               670             MOV     AL,AH                   ; GET INTO LOW BYTE
031F 32E4               671             XOR     AH,AH                   ; ZERO HIGH BYTE
0321 D1E0               672             SAL     AX,1                    ; *2 FOR TABLE LOOKUP
0323 8BF0               673             MOV     SI,AX                   ; PUT INTO SI FOR BRANCH
0325 3D2A00             674             CMP     AX,M1L                  ; TEST WITHIN RANGE
0328 58                 675             POP     AX                      ; RESTORE AX
0329 7305               676             JNB     BAD_COMMAND
032B 2EFFA49C02         677             JMP     WORD PTR CS:[SI + OFFSET M1]
0330                    678     BAD_COMMAND:
0330 C606740001         679             MOV     DISK_STATUS,BAD_CMD     ; COMMAND ERROR
0335 B000               680             MOV     AL,0
0337 C3                 681             RET
                        682     DISK_IO_CONT    ENDP
                        683
                        684     ;-----------------------------------------------
                        685     ;       RESET THE DISK SYSTEM  (AH = 000H)      :
                        686     ;-----------------------------------------------
                        687
```

BIOS Listing *(continued)*

```
LOC OBJ                 LINE    SOURCE

                        764     ;--------------------------------------------
                        765     ;       GET PARAMETERS   (AH = 8)            :
                        766     ;--------------------------------------------
                        767
0390                    768     GET_PARM_N      LABEL   NEAR
0390                    769     GET_PARM        PROC    FAR             ; GET DRIVE PARAMETERS
0390 1E                 770             PUSH    DS                      ; SAVE REGISTERS
0391 06                 771             PUSH    ES
0392 53                 772             PUSH    BX
                        773
                        774             ASSUME  DS:DUMMY
0393 2BC0               775             SUB     AX,AX                   ; ESTABLISH ADDRESSING
0395 8ED8               776             MOV     DS,AX
0397 C41E0401           777             LES     BX,HF_TBL_VEC
                        778             ASSUME  DS:DATA
039B B84000             779             MOV     AX,DATA
039E 8ED8               780             MOV     DS,AX                   ; ESTABLISH SEGMENT
                        781
03A0 80EA80             782             SUB     DL,80H
03A3 80FA08             783             CMP     DL,MAX_FILE             ; TEST WITHIN RANGE
03A6 732F               784             JAE     G4
                        785
03A8 E81BFF             786             CALL    SETUP_A
                        787
03AB E8DF03             788             CALL    SW2_OFFS
03AE 7227               789             JC      G4
03B0 03D8               790             ADD     BX,AX
                        791
03B2 268B07             792             MOV     AX,ES:[BX]          ; MAX NUMBER OF CYLINDERS
03B5 2D0200             793             SUB     AX,2                    ; ADJUST FOR 0-N
                        794                                             ; AND RESERVE LAST TRACK
03B8 8AE8               795             MOV     CH,AL
03BA 250003             796             AND     AX,0300H                ; HIGH TWO BITS OF CYL
03BD D1E8               797             SHR     AX,1
03BF D1E8               798             SHR     AX,1
03C1 0C11               799             OR      AL,011H                 ; SECTORS
03C3 8AC8               800             MOV     CL,AL
                        801
03C5 268A7702           802             MOV     DH,ES:[BX][2]       ; HEADS
03C9 FECE               803             DEC     DH                      ; 0-N RANGE
03CB 8A167500           804             MOV     DL,HF_NUM               ; DRIVE COUNT
03CF 2BC0               805             SUB     AX,AX
03D1                    806     G5:
03D1 5B                 807             POP     BX                      ; RESTORE REGISTERS
03D2 07                 808             POP     ES
03D3 1F                 809             POP     DS
03D4 CA0200             810             RET     2
03D7                    811     G4:
03D7 C606740007         812             MOV     DISK_STATUS,INIT_FAIL   ; OPERATION FAILED
03DC B407               813             MOV     AH,INIT_FAIL
03DE 2AC0               814             SUB     AL,AL
03E0 2BD2               815             SUB     DX,DX
03E2 2BC9               816             SUB     CX,CX
03E4 F9                 817             STC                             ; SET ERROR FLAG
03E5 EBEA               818             JMP     G5
                        819     GET_PARM        ENDP
                        820
                        821     ;--------------------------------------------------------
                        822     ; INITIALIZE DRIVE CHARACTERISTICS                      :
                        823     ;                                                       :
                        824     ; FIXED DISK PARAMETER TABLE                           :
                        825     ;                                                       :
                        826     ;  -  THE TABLE IS COMPOSED OF A BLOCK DEFINED AS: :
                        827     ;                                                      :
                        828     ;       (1 WORD) - MAXIMUM NUMBER OF CYLINDERS         :
                        829     ;       (1 BYTE) - MAXIMUM NUMBER OF HEADS             :
                        830     ;       (1 WORD) - STARTING REDUCED WRITE CURRENT CYL   :
                        831     ;       (1 WORD) - STARTING WRITE PRECOMPENSATION CYL   :
                        832     ;       (1 BYTE) - MAXIMUM ECC DATA BURST LENGTH       :
                        833     ;       (1 BYTE) - CONTROL BYTE (DRIVE STEP OPTION)    :
                        834     ;                  BIT    7 DISABLE DISK-ACCESS RETRIES :
                        835     ;                  BIT    6 DISABLE ECC RETRIES         :
                        836     ;                  BITS 5-3 ZERO                        :
                        837     ;                  BITS 2-0 DRIVE OPTION                :
                        838     ;       (1 BYTE) - STANDARD TIME OUT VALUE (SEE BELOW) :
                        839     ;       (1 BYTE) - TIME OUT VALUE FOR FORMAT DRIVE     :
                        840     ;       (1 BYTE) - TIME OUT VALUE FOR CHECK DRIVE      :
                        841     ;       (4 BYTES)                                      :
```

BIOS Listing *(continued)*

```
LOC OBJ                 LINE    SOURCE

041A 3201               919             DW      0306D
041C 0000               920             DW      0000D
041E 0B                 921             DB      0BH
041F 05                 922             DB      05H
0420 0C                 923             DB      0CH                     ; STANDARD
0421 B4                 924             DB      0B4H                    ; FORMAT DRIVE
0422 28                 925             DB      028H                    ; CHECK DRIVE
0423 00000000           926             DB      0,0,0,0
                        927
0427                    928     INIT_DRV        PROC    NEAR
                        929
                        930     ;----- DO DRIVE ZERO
                        931
0427 C60642000C         932             MOV     CMD_BLOCK+0,INIT_DRV_CMD
042C C606430000         933             MOV     CMD_BLOCK+1,0
0431 E81000             934             CALL    INIT_DRV_R
0434 720D               935             JC      INIT_DRV_OUT
                        936
                        937     ;----- DO DRIVE ONE
                        938
0436 C60642000C         939             MOV     CMD_BLOCK+0,INIT_DRV_CMD
043B C606430020         940             MOV     CMD_BLOCK+1,00100000B
0440 E80100             941             CALL    INIT_DRV_R
0443                    942     INIT_DRV_OUT:
0443 C3                 943             RET
                        944     INIT_DRV        ENDP
                        945
0444                    946     INIT_DRV_R      PROC    NEAR
                        947             ASSUME  ES:CODE
0444 2AC0               948             SUB     AL,AL
0446 E81901             949             CALL    COMMAND                 ; ISSUE THE COMMAND
0449 7301               950             JNC     B1
044B C3                 951             RET
044C                    952     B1:
044C 1E                 953             PUSH    DS                      ; SAVE SEGMENT
                        954             ASSUME  DS:DUMMY
044D 2BC0               955             SUB     AX,AX
044F 8ED8               956             MOV     DS,AX                   ; ESTABLISH SEGMENT
0451 C41E0401           957             LES     BX,HF_TBL_VEC
0455 1F                 958             POP     DS                      ; RESTORE SEGMENT
                        959             ASSUME  DS:DATA
0456 E83403             960             CALL    SW2_OFFS
0459 7257               961             JC      B3
045B 03D8               962             ADD     BX,AX
                        963
                        964     ;----- SEND DRIVE PARAMETERS MOST SIGNIFICANT BYTE FIRST
                        965
045D BF0100             966             MOV     DI,1
0460 E85F00             967             CALL    INIT_DRV_S
0463 724D               968             JC      B3
                        969
0465 BF0000             970             MOV     DI,0
0468 E85700             971             CALL    INIT_DRV_S
046B 7245               972             JC      B3
                        973
046D BF0200             974             MOV     DI,2
0470 E84F00             975             CALL    INIT_DRV_S
0473 723D               976             JC      B3
                        977
0475 BF0400             978             MOV     DI,4
0478 E84700             979             CALL    INIT_DRV_S
047B 7235               980             JC      B3
                        981
047D BF0300             982             MOV     DI,3
0480 E83F00             983             CALL    INIT_DRV_S
0483 722D               984             JC      B3
                        985
0485 BF0600             986             MOV     DI,6
0488 E83700             987             CALL    INIT_DRV_S
048B 7225               988             JC      B3
                        989
048D BF0500             990             MOV     DI,5
0490 E82F00             991             CALL    INIT_DRV_S
0493 721D               992             JC      B3
                        993
0495 BF0700             994             MOV     DI,7
0498 E82700             995             CALL    INIT_DRV_S
```

BIOS Listing *(continued)*

```
LOC OBJ                  LINE    SOURCE

                         1073    DISK_SEEK       ENDP
                         1074
                         1075    ;--------------------------------------------
                         1076    ;       READ SECTOR BUFFER    (AH = 0EH)          :
                         1077    ;--------------------------------------------
                         1078
04F9                     1079    RD_BUFF PROC    NEAR
04F9 C60642000E          1080            MOV     CMD_BLOCK+0,RD_BUFF_CMD
04FE C606460001          1081            MOV     CMD_BLOCK+4,1           ; ONLY ONE BLOCK
0503 B047                1082            MOV     AL,DMA_READ
0505 EB3E                1083            JMP     SHORT   DMA_OPN
                         1084    RD_BUFF ENDP
                         1085
                         1086    ;--------------------------------------------
                         1087    ;       WRITE SECTOR BUFFER    (AH = 0FH)         :
                         1088    ;--------------------------------------------
                         1089
0507                     1090    WR_BUFF PROC    NEAR
0507 C60642000F          1091            MOV     CMD_BLOCK+0,WR_BUFF_CMD
050C C606460001          1092            MOV     CMD_BLOCK+4,1           ; ONLY ONE BLOCK
0511 B04B                1093            MOV     AL,DMA_WRITE
0513 EB30                1094            JMP     SHORT   DMA_OPN
                         1095    WR_BUFF ENDP
                         1096
                         1097    ;--------------------------------------------
                         1098    ;       TEST DISK READY    (AH = 010H)          :
                         1099    ;--------------------------------------------
                         1100
0515                     1101    TST_RDY PROC    NEAR
0515 C606420000          1102            MOV     CMD_BLOCK+0,TST_RDY_CMD
051A EB1A                1103            JMP     SHORT   NDMA_OPN
                         1104    TST_RDY ENDP
                         1105
                         1106    ;--------------------------------------------
                         1107    ;       RECALIBRATE    (AH = 011H)              :
                         1108    ;--------------------------------------------
                         1109
051C                     1110    HDISK_RECAL     PROC    NEAR
051C C606420001          1111            MOV     CMD_BLOCK,RECAL_CMD
0521 EB13                1112            JMP     SHORT   NDMA_OPN
                         1113    HDISK_RECAL     ENDP
                         1114
                         1115    ;-------------------------------------------------------
                         1116    ;       CONTROLLER RAM DIAGNOSTICS    (AH = 012H)       :
                         1117    ;-------------------------------------------------------
                         1118
0523                     1119    RAM_DIAG        PROC    NEAR
0523 C6064200E0          1120            MOV     CMD_BLOCK+0,RAM_DIAG_CMD
0528 EB0C                1121            JMP     SHORT   NDMA_OPN
                         1122    RAM_DIAG        ENDP
                         1123
                         1124    ;--------------------------------------------
                         1125    ;       DRIVE DIAGNOSTICS    (AH = 013H)         :
                         1126    ;--------------------------------------------
                         1127
052A                     1128    CHK_DRV PROC    NEAR
052A C6064200E3          1129            MOV     CMD_BLOCK+0,CHK_DRV_CMD
052F EB05                1130            JMP     SHORT   NDMA_OPN
                         1131    CHK_DRV ENDP
                         1132
                         1133    ;-----------------------------------------------------------
                         1134    ;      CONTROLLER INTERNAL DIAGNOSTICS    (AH = 014H)     :
                         1135    ;-----------------------------------------------------------
                         1136
0531                     1137    CNTLR_DIAG      PROC    NEAR
0531 C6064200E4          1138            MOV     CMD_BLOCK+0,CNTLR_DIAG_CMD
                         1139    CNTLR_DIAG      ENDP
                         1140
                         1141    ;-------------------------------------------------------
                         1142    ;                    SUPPORT ROUTINES                   :
                         1143    ;-------------------------------------------------------
                         1144
0536                     1145    NDMA_OPN:
0536 B002                1146            MOV     AL,02H
0538 E82700              1147            CALL    COMMAND                 ; ISSUE THE COMMAND
053B 7221                1148            JC      G11
053D EB16                1149            JMP     SHORT   G3
```

BIOS Listing *(continued)*

```
LOC OBJ                  LINE    SOURCE

                         1227    ;                                                :
                         1228    ; BYTE 2                                         :
                         1229    ;       BITS 7-5   CYLINDER HIGH                 :
                         1230    ;       BITS 4-0   SECTOR NUMBER                 :
                         1231    ;                                                :
                         1232    ; BYTE 3                                         :
                         1233    ;       BITS 7-0   CYLINDER LOW                  :
                         1234    ;                                                :
                         1235    ;-------------------------------------------------
                         1236
059C                     1237    ERROR_CHK       PROC    NEAR
                         1238            ASSUME  ES:DATA
059C A07400              1239            MOV     AL,DISK_STATUS          ; CHECK IF THERE WAS AN ERROR
059F 0AC0                1240            OR      AL,AL
05A1 7501                1241            JNZ     G21
05A3 C3                  1242            RET
                         1243
                         1244    ;----- PERFORM SENSE STATUS
                         1245
05A4                     1246    G21:
05A4 B84000              1247            MOV     AX,DATA
05A7 8EC0                1248            MOV     ES,AX                   ; ESTABLISH SEGMENT
05A9 2BC0                1249            SUB     AX,AX
05AB 8BF8                1250            MOV     DI,AX
05AD C606420003          1251            MOV     CMD_BLOCK+0,SENSE_CMD
05B2 2AC0                1252            SUB     AL,AL
05B4 E8ABFF              1253            CALL    COMMAND                 ; ISSUE SENSE STATUS COMMAND
05B7 7223                1254            JC      SENSE_ABORT             ; CANNOT RECOVER
05B9 B90400              1255            MOV     CX,4
05BC                     1256    G22:
05BC E8CB00              1257            CALL    HD_WAIT_REQ
05BF 7220                1258            JC      G24
05C1 E8AD01              1259            CALL    PORT_0
05C4 EC                  1260            IN      AL,DX
05C5 26884542            1261            MOV     ES:HD_ERROR[DI],AL ; STORE AWAY SENSE BYTES
05C9 47                  1262            INC     DI
05CA E8B101              1263            CALL    PORT_1
05CD E2ED                1264            LOOP    G22
05CF E8B800              1265            CALL    HD_WAIT_REQ
05D2 720D                1266            JC      G24
05D4 E89A01              1267            CALL    PORT_0
05D7 EC                  1268            IN      AL,DX
05D8 A802                1269            TEST    AL,2
05DA 740F                1270            JZ      STAT_ERR
05DC                     1271    SENSE_ABORT:
05DC C6067400FF          1272            MOV     DISK_STATUS,SENSE_FAIL
05E1                     1273    G24:
05E1 F9                  1274            STC
05E2 C3                  1275            RET
                         1276    ERROR_CHK       ENDP
                         1277
05E3 1A06                1278    T_0     DW      TYPE_0
05E5 2706                1279    T_1     DW      TYPE_1
05E7 6A06                1280    T_2     DW      TYPE_2
05E9 7706                1281    T_3     DW      TYPE_3
                         1282
05EB                     1283    STAT_ERR:
05EB 268A1E4200          1284            MOV     BL,ES:HD_ERROR    ; GET ERROR BYTE
05F0 8AC3                1285            MOV     AL,BL
05F2 240F                1286            AND     AL,0FH
05F4 80E330              1287            AND     BL,00110000B            ; ISOLATE TYPE
05F7 2AFF                1288            SUB     BH,BH
05F9 B103                1289            MOV     CL,3
05FB D3EB                1290            SHR     BX,CL                   ; ADJUST
05FD 2EFFA7E305          1291            JMP     WORD PTR CS:[BX + OFFSET T_0]
                         1292            ASSUME ES:NOTHING
                         1293
0602                     1294    TYPE0_TABLE     LABEL   BYTE
0602 00204020800020      1295            DB      0,BAD_CNTLR,BAD_SEEK,BAD_CNTLR,TIME_OUT,0,BAD_CNTLR
0609 0040                1296            DB      0,BAD_SEEK
  0009                   1297    TYPE0_LEN       EQU     $-TYPE0_TABLE
060B                     1298    TYPE1_TABLE     LABEL   BYTE
060B 1010020004          1299            DB      BAD_ECC,BAD_ECC,BAD_ADDR_MARK,0,RECORD_NOT_FND
0610 400000110B          1300            DB      BAD_SEEK,0,0,DATA_CORRECTED,BAD_TRACK
  000A                   1301    TYPE1_LEN       EQU     $-TYPE1_TABLE
0615                     1302    TYPE2_TABLE     LABEL   BYTE
0615 0102                1303            DB      BAD_CMD,BAD_ADDR_MARK
```

BIOS Listing *(continued)*

```
LOC OBJ                  LINE    SOURCE

068B 2BC9                1381            SUB     CX,CX
068D E8EE00              1382            CALL    PORT_1
0690                     1383    L1:
0690 EC                  1384            IN      AL,DX
0691 A801                1385            TEST    AL,R1_REQ
0693 7508                1386            JNZ     L2
0695 E2F9                1387            LOOP    L1
0697 C606740080          1388            MOV     DISK_STATUS,TIME_OUT
069C F9                  1389            STC
069D                     1390    L2:
069D 59                  1391            POP     CX
069E C3                  1392            RET
                         1393    HD_WAIT_REQ     ENDP
                         1394
                         1395    ;--------------------------------------------------------
                         1396    ; DMA_SETUP                                            :
                         1397    ;       THIS ROUTINE SETS UP FOR DMA OPERATIONS.       :
                         1398    ; INPUT                                                :
                         1399    ;       (AL) = MODE BYTE FOR THE DMA                   :
                         1400    ;       (ES:BX) = ADDRESS TO READ/WRITE THE DATA  :
                         1401    ; OUTPUT                                               :
                         1402    ;       (AX) DESTROYED                                 :
                         1403    ;--------------------------------------------------------
069F                     1404    DMA_SETUP       PROC    NEAR
069F 50                  1405            PUSH    AX
06A0 A04600              1406            MOV     AL,CMD_BLOCK+4
06A3 3C81                1407            CMP     AL,81H                  ; BLOCK COUNT OUT OF RANGE
06A5 58                  1408            POP     AX
06A6 7202                1409            JB      J1
06A8 F9                  1410            STC
06A9 C3                  1411            RET
06AA                     1412    J1:
06AA 51                  1413            PUSH    CX                      ; SAVE THE REGISTER
06AB FA                  1414            CLI                             ; NO MORE INTERRUPTS
06AC E60C                1415            OUT     DMA+12,AL               ; SET THE FIRST/LAST F/F
06AE 50                  1416            PUSH    AX
06AF 58                  1417            POP     AX
06B0 E60B                1418            OUT     DMA+11,AL               ; OUTPUT THE MODE BYTE
06B2 8CC0                1419            MOV     AX,ES                   ; GET THE ES VALUE
06B4 B104                1420            MOV     CL,4                    ; SHIFT COUNT
06B6 D3C0                1421            ROL     AX,CL                   ; ROTATE LEFT
06B8 8AE8                1422            MOV     CH,AL                   ; GET HIGHEST NYBBLE OF ES TO CH
06BA 24F0                1423            AND     AL,0F0H                 ; ZERO THE LOW NYBBLE FROM SEGMENT
06BC 03C3                1424            ADD     AX,BX                   ; TEST FOR CARRY FROM ADDITION
06BE 7302                1425            JNC     J33
06C0 FEC5                1426            INC     CH                      ; CARRY MEANS HIGH 4 BITS MUST BE INC
06C2                     1427    J33:
06C2 50                  1428            PUSH    AX                      ; SAVE START ADDRESS
06C3 E606                1429            OUT     DMA+6,AL                ; OUTPUT LOW ADDRESS
06C5 8AC4                1430            MOV     AL,AH
06C7 E606                1431            OUT     DMA+6,AL                ; OUTPUT HIGH ADDRESS
06C9 8AC5                1432            MOV     AL,CH                   ; GET HIGH 4 BITS
06CB 240F                1433            AND     AL,0FH
06CD E682                1434            OUT     DMA_HIGH,AL             ; OUTPUT THE HIGH 4 BITS TO PAGE REG
                         1435
                         1436    ;------ DETERMINE COUNT
                         1437
06CF A04600              1438            MOV     AL,CMD_BLOCK+4          ; RECOVER BLOCK COUNT
06D2 D0E0                1439            SHL     AL,1                    ; MULTIPLY BY 512 BYTES PER SECTOR
06D4 FEC8                1440            DEC     AL                      ;   AND DECREMENT VALUE BY ONE
06D6 8AE0                1441            MOV     AH,AL
06D8 B0FF                1442            MOV     AL,0FFH
                         1443
                         1444    ;----- HANDLE READ AND WRITE LONG (516D BYTE BLOCKS)
                         1445
06DA 50                  1446            PUSH    AX                      ; SAVE REGISTER
06DB A04200              1447            MOV     AL,CMD_BLOCK+0          ; GET COMMAND
06DE 3CE5                1448            CMP     AL,RD_LONG_CMD
06E0 7407                1449            JE      ADD4
06E2 3CE6                1450            CMP     AL,WR_LONG_CMD
06E4 7403                1451            JE      ADD4
06E6 58                  1452            POP     AX                      ; RESTORE REGISTER
06E7 EB11                1453            JMP     SHORT   J20
06E9                     1454    ADD4:
06E9 58                  1455            POP     AX                      ; RESTORE REGISTER
06EA B80402              1456            MOV     AX,516D                 ; ONE BLOCK (512) PLUS 4 BYTES ECC
06ED 53                  1457            PUSH    BX
```

BIOS Listing *(continued)*

```
LOC OBJ                  LINE    SOURCE

075C 07                  1535            POP     ES
075D 59                  1536            POP     CX
075E 5B                  1537            POP     BX
075F C3                  1538            RET
                         1539    WAIT_INT        ENDP
                         1540
0760                     1541    HD_INT  PROC    NEAR
0760 50                  1542            PUSH    AX
0761 B020                1543            MOV     AL,EOI                  ; END OF INTERRUPT
0763 E620                1544            OUT     INT_CTL_PORT,AL
0765 B007                1545            MOV     AL,07H                  ; SET DMA MODE TO DISABLE
0767 E60A                1546            OUT     DMA+10,AL
0769 E421                1547            IN      AL,021H
076B 0C20                1548            OR      AL,020H
076D E621                1549            OUT     021H,AL
076F 58                  1550            POP     AX
0770 CF                  1551            IRET
                         1552    HD_INT  ENDP
                         1553
                         1554    ;---------------------------------------
                         1555    ; PORTS                                 :
                         1556    ;       GENERATE PROPER PORT VALUE      :
                         1557    ;       BASED ON THE PORT OFFSET        :
                         1558    ;---------------------------------------
                         1559
0771                     1560    PORT_0  PROC    NEAR
0771 BA2003              1561            MOV     DX,HF_PORT              ; BASE VALUE
0774 50                  1562            PUSH    AX
0775 2AE4                1563            SUB     AH,AH
0777 A07700              1564            MOV     AL,PORT_OFF             ; ADD IN THE OFFSET
077A 03D0                1565            ADD     DX,AX
077C 58                  1566            POP     AX
077D C3                  1567            RET
                         1568    PORT_0  ENDP
                         1569
077E                     1570    PORT_1  PROC    NEAR
077E E8F0FF              1571            CALL    PORT_0
0781 42                  1572            INC     DX                      ; INCREMENT TO PORT ONE
0782 C3                  1573            RET
                         1574    PORT_1  ENDP
                         1575
0783                     1576    PORT_2  PROC    NEAR
0783 E8F8FF              1577            CALL    PORT_1
0786 42                  1578            INC     DX                      ; INCREMENT TO PORT TWO
0787 C3                  1579            RET
                         1580    PORT_2  ENDP
                         1581
0788                     1582    PORT_3  PROC    NEAR
0788 E8F8FF              1583            CALL    PORT_2
078B 42                  1584            INC     DX                      ; INCREMENT TO PORT THREE
078C C3                  1585            RET
                         1586    PORT_3  ENDP
                         1587
                         1588    ;-----------------------------------------------
                         1589    ; SW2_OFFS                                      :
                         1590    ;       DETERMINE PARAMETER TABLE OFFSET        :
                         1591    ;       USING CONTROLLER PORT TWO AND           :
                         1592    ;       DRIVE NUMBER SPECIFIER (0-1)            :
                         1593    ;-----------------------------------------------
                         1594
078D                     1595    SW2_OFFS        PROC    NEAR
078D E8F3FF              1596            CALL    PORT_2
0790 EC                  1597            IN      AL,DX                   ; READ PORT 2
0791 50                  1598            PUSH    AX
0792 E8E9FF              1599            CALL    PORT_1
0795 EC                  1600            IN      AL,DX
0796 2402                1601            AND     AL,2                    ; CHECK FOR ERROR
0798 58                  1602            POP     AX
0799 7516                1603            JNZ     SW2_OFFS_ERR
079B 8A264300            1604            MOV     AH,CMD_BLOCK+1
079F 80E420              1605            AND     AH,00100000B            ; DRIVE 0 OR 1
07A2 7504                1606            JNZ     SW2_AND
07A4 D0E8                1607            SHR     AL,1                    ; ADJUST
07A6 D0E8                1608            SHR     AL,1
07A8                     1609    SW2_AND:
07A8 2403                1610            AND     AL,011B                 ; ISOLATE
07AA B104                1611            MOV     CL,4
```

Fixed Disk & Diskette Drive Adapter

Contents

Fixed Disk & Diskette Drive Adapter

Description

The Fixed Disk and Diskette Drive Adapter connects to the functions system board using one of the system expansion slots. The adapter controls the 5-1/4 inch diskette drives and fixed disk drives. Connectors on the adapter supply all the signals necessary to operate up to two fixed drives and one diskette drive or one fixed drive and two diskette drives. The adapter will allow concurrent data operations on one diskette and one fixed disk drive.

The adapter operates when connected to a system board expansion slot. This channel is described in the "System Board" section of the IBM Personal Computer AT *Technical Reference* Manual.

Task File Registers *(continued)*

Diagnostic Mode

01	No errors
02	Controller error
03	Sector buffer error
04	ECC device error
05	Control processor error

The following are bit definitions for the operational mode.

Operational Mode

Bit 0	Data Address Mark (DAM) Not Found–This bit indicates that DAM could not be found within 16 bytes of the ID field.
Bit 1	TR 000 Error–This bit will be set if, during a Restore command, the track 000 line from the fixed disk is not true within 1023 step pulses to the drive.
Bit 2	Aborted Command–A command is aborted based on the drive status (Write Fault, Not Seek Complete, Drive Not Ready, or an invalid command). The status and error registers may be decoded to determine the cause.
Bit 3	Not used.
Bit 4	ID Not Found–The ID field with the specified cylinder, head, and sector number could not be found. If retries are enabled, the controller attempts to read the ID 16 times before indicating the error. If retries are disabled, the track is scanned a maximum of two times before setting this error bit.
Bit 5	Not used
Bit 6	Data ECC Error–This bit indicates that an uncorrectable ECC error occurred in the target's data field during a read command.
Bit 7	Bad Block Detect–This bit indicates that the bad block mark was detected in the target's ID field. No Read or Write commands will be executed in any data fields marked bad.

Bit 3–Bit 0 Head Select Bits–Bits 3 through 0 specify the desired read/write head. Bit 0 is the least-significant (0101 selects head 5). The adapter supports up to 16 read/write heads. For access to heads 8 through 15, bit 3 of the fixed disk register (address hex 3F6) must be set to 1.

Note: This register must be loaded with the maximum number of heads for each drive before a Set Parameters command is issued.

Status Register

The controller sets up the status register with the command status after execution. The program must look at this register to determine the result of any operation. If the busy bit is set, no other bits are valid. A read of the status register clears interrupt request 14. If 'write fault' or 'error' is active, or if 'seek complete' or 'ready' is inactive, a multi-sector operation is aborted.

The following defines the bits of the status register.

Bit 7 Busy–This bit indicates the controller's status. A 1 indicates the controller is executing a command. If this bit is set, no other status register bit is valid, and the other registers reflect the status register's contents; therefore, the busy bit must examined before any fixed disk register is read.

Bit 6 Drive Ready–A 1 on this bit together with a 1 on seek complete bit (bit 4) indicates that the fixed disk drive is ready to read, write, or seek. A 0 indicates that read, write, and seek are inhibited.

Bit 5 Write Fault–A 1 on this bit indicates improper operation of the drive; read, write, or seek is inhibited.

Bit 4 Seek Complete–A 1 on this bit indicates that the read/write heads have completed a seek operation.

Bit 3 Data Request–This bit indicates that the sector buffer requires servicing during a Read or Write command. If either bit 7 (busy) or this bit is active, a command is being executed. Upon receipt of any command, this bit is reset.

Bit 2 Corrected Data–A 1 on this bit indicates that the data read from the disk was successfully corrected by the ECC algorithm. Soft errors will not end multi-sector operations.

Bit 1 Index–This bit is set to 1 each revolution of the disk.

Bit 0 Error–A 1 on this bit indicates that the previous command ended in an error, and that one or more bits are set in the error register. The next command from the controller resets the error bit. This bit, when set, halts multi-sector operations.

The following figure shows the bit definitions for bits L and T.

Bit	Definition	0	1
L	Data Mode	Data Only	Data Plus 4 Byte ECC
T	Retry Mode	Retries Enabled	Retries Disabled

L and T Bit Definitions

Note: The system verifies the operation of ECC by reading and writing with the ECC bytes. When retries are disabled, ECC and ID field retries are limited to less than two complete revolutions.

Following are descriptions of the valid command-register commands.

Restore: The controller issues step pulses to the drive at 3 milliseconds per step until the track 000 indicator from the drive is active. If track 000 is not active within 1023 steps, the error bit in the status register is set, and a track 000 error is placed in the error register. The implied seek step rate is set by this command.

Seek: The Seek command moves the R/W heads to the cylinder specified in the task files. The adapter supports overlapped seeking on two drives or setup of the buffered seek stepping rate for the implied seek during a Read/Write command. An interrupt is generated at the completion of the command.

Read Sector: A number of sectors (1–256) may be read from the fixed disk with or without the ECC field appended in the Programmed I/O (PIO) mode. If the heads are not over the target track, the controller issues step pulses to the drive and checks for the proper ID field before reading any data. The stepping rate used during the implied seek s the value specified during the previous Seek or Restore command. Data errors, up to 5 bits in length, are automatically corrected on Read Short commands. If an uncorrectable error occurs, the data transfer still takes place; however, a multi-sector read ends after the system reads the sector in error. Interrupts occur as each sector is ready to be read by the system. No interrupt is generated at the end of the command, after the lost sector is read by the system.

Write Sector: A number of sectors (1–256) may be written to the fixed disk with or without the ECC field appended in the PIO mode. The Write Sector command also supports implied seeks. Interrupts for the Write command occur before each sector is transferred to the buffer (except the first) and at the end of the command. The first sector may be written to the buffer immediately after the command has been sent, and 'data request' is active.

Format Track: The track specified by the task file is formatted with ID and data fields according to the interleave table transferred to the buffer. The interleave table is composed of two bytes per sector as follows: 00, Physical Sector 1, 00, Physical Sector 2, . . . 00,Physical Sector 17. The table for 2-to-1 interleave is: 00, 01, 00, 0A, 00, 02, 00, 0B, 00, 03, 00, 0C, 00, 04, 00, 0D, 00, 05, 00, 0E, 00, 06, 00, 0F, 00, 07, 00, 10, 00, 08, 00, 11, 00, 09. The data transfer must be 512 bytes even though the table may be only 34 bytes. The sector count register must be loaded with the number of sectors per track before each Format Track command. An interrupt is generated at the completion of the command; the Format Track command supports no error reporting. A bad block may be specified by replacing a 00 table entry with an 80. When switching between drives, a restore command must be executed prior to attempting a format.

Diskette Function *(continued)*

Digital Output Register (Hex 3F2)

The digital output register (DOR) is an output-only register used to control drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bit definitions follow.

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Drive B Motor Enable

Bit 4 Drive A Motor Enable

Bit 3 Enable Diskette Interrupts and DMA

Bit 2 Diskette Function Reset

Bit 1 Reserved

Bit 0 Drive Select–A 0 on this bit indicates that drive A is selected.

Note: A channel reset clears all bits.

Digital Input Register (Hex 3F7)

The digital input register is an 8-bit, read- only register used for diagnostic purposes. The following are bit definitions for this register.

Bit 7 Diskette Change

Bit 6 Write Gate

Bit 5 Head Select 3/Reduced Write Current

Bit 4 Head Select 2

Bit 3 Head Select 1

Bit 2 Head Select 0

Bit 1 Drive Select 1

Bit 0 Drive Select 0

Note: Bits 0 through 6 apply to the currently selected fixed disk drive.

Diskette Controller Commands

The diskette controller can perform 11 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the diskette controller and the processor, each command can be considered to consist of three phases:

Command Phase: The processor issues a sequence of Write commands to the diskette controller that direct the controller to perform a specific operation.

Execution Phase: The diskette controller performs the specified operation

Result Phase: After completion of the operation, status and other housekeeping information is made available to the processor through a sequence of Read commands to the processor.

The following is a list of commands that may be issued to the diskette controller.

- Read Data
- Format a Track
- Scan Equal
- Scan Low or Equal
- Scan High or Equal
- Recalibrate
- Sense Interrupt Status
- Specify
- Sense Drive Status
- Seek
- Invalid

Diskette Controller Commands *(continued)*

PCN	Present Cylinder Number — The cylinder number at the completion of a Sense interrupt status command (present position of the head).
R	Record — The sector number to be read or written.
R/W	Read/Write — This stands for either a 'read' or 'write' signal.
SC	Sector — The number of sectors per cylinder.
SK	Skip — This stands for skip deleted-data address mark.
SRT	This 4 bit byte indicates the stepping rate for the diskette drive as follows:
1111	1 millisecond
1110	2 milliseconds
1101	3 milliseconds
1111	2 milliseconds
1110	4 milliseconds
1101	6 milliseconds
ST 0 — ST 1	Status 0 — Status 3 — One of the four registers that stores status information after a command is executed.
STP	Scan Test — If STP is 1, the data in contiguous sectors is compared with the data sent by the processor during a scan operation. If STP is 2, then alternate sections are read and compared.
US0—US1	Unit Select — The selected driver number encoded the same as bits 0 and 1 of the digital output register (DOR).

Controller Commands *(continued)*

Format a Track

Command Phase

The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	MF	0	0	1	1	0	0
X	X	X	X	X	HD	US1	US0
				N			
				SC			
				GPL			
				D			

Result Phase

The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

Scan Equal

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
MT	MF	SK	1	0	0	0	1
X	X	X	X	X	HD	US1	US0
				C			
				H			
				R			
				N			
				EOT			
				GPL			
				STP			

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

Controller Commands *(continued)*

Recalibrate

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	1
X	X	X	X	X	0	US1	US0

Result Phase: This command has no result phase.

Sense Interrupt Status

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0

Result Phase: The following bytes are issued by the controller in the result phase:

STO
PCN

Specify

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1
(	SRT	)		(	HUT	)	
(	HLT	)		(	ND	)	

Result Phase: This command has no result phase.

Sense Driver Status

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0
X	X	X	X	X	HD	US1	US0

Result Phase: The following bytes are issued by the controller in the result phase:

ST3

Command Status Registers

The following is information about the command status registers ST0 through ST3.

Command Status Register 0 (ST0)

The following are bit definitions for command status register 0.

Bit 7—Bit 6 Interrupt Code (IC)

- **00** Normal Termination of Command (NT) — The command was completed and properly executed.
- **01** Abrupt Termination of Command (AT) — The execution of the command was started but not successfully completed.
- **10** Invalid Command Issue (IC) — The issued command was never started.
- **11** Abnormal termination because, during the execution of a command, the 'ready' signal from the diskette drive changed state.

Bit 5 Seek End (SE) — Set to 1 when the controller completes the Seek command.

Bit 4 Equipment Check (EC) — Set if a 'fault' signal is received from the diskette drive, or if the 'track—0' signal fails to occur after 77 step pulses (Recalibrate Command).

Bit 3 Not Ready (NR) — This flag is set when the diskette drive is in the not-ready state and a Read or Write command is issued. It is also set if a Read or Write command is issued to side 1 of a single-sided diskette drive.

Bit 2 Head Address (HD) — Indicates the state of the head at interrupt.

Bit 1–Bit 0 Unit select 1 and 2 (US 1 and 2) — Indicate a drive's unit number at interrupt.

Command Status Register 1 (ST1)

The following are bit definitions for command status register 1.

Bit 7 End of Cylinder (EC) — Set when the controller tries to gain access to a sector beyond the final sector of a cylinder.

Bit 6 Not Used — Always 0.

Bit 5 Data Error (DE) — Set when the controller detects a CRC error in either the ID field or the data field.

Bit 4 Overrun (OR) — Set if the controller is not serviced by the main system within a certain time limit during data transfers.

Bit 3 Not Used — This bit is always set to 0.

Command Status Registers *(continued)*

Command Status Register 3 (ST3)

The following are bit definitions for command status register 3.

Bit 7 Fault (FT) — Status of the 'fault' signal from the diskette drive.

Bit 6 Write Protect (WP) — Status of the 'write-protect' signal from the diskette drive.

Bit 5 Ready (RY) — Status of the 'ready' signal from the diskette drive.

Bit 4 Track 0 (T0) — Status of the 'track 0' signal from the diskette drive.

Bit 3 Two Side (TS) — Status of the 'two side' signal from the diskette drive.

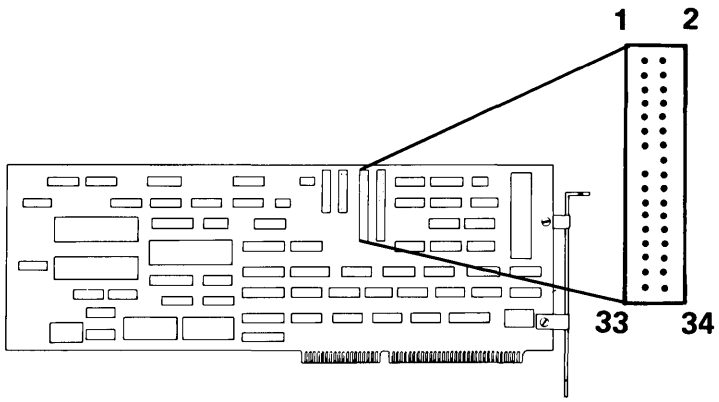
Bit 2 Head Address (HD) — Status of the 'side-select' signal from the diskette drive.

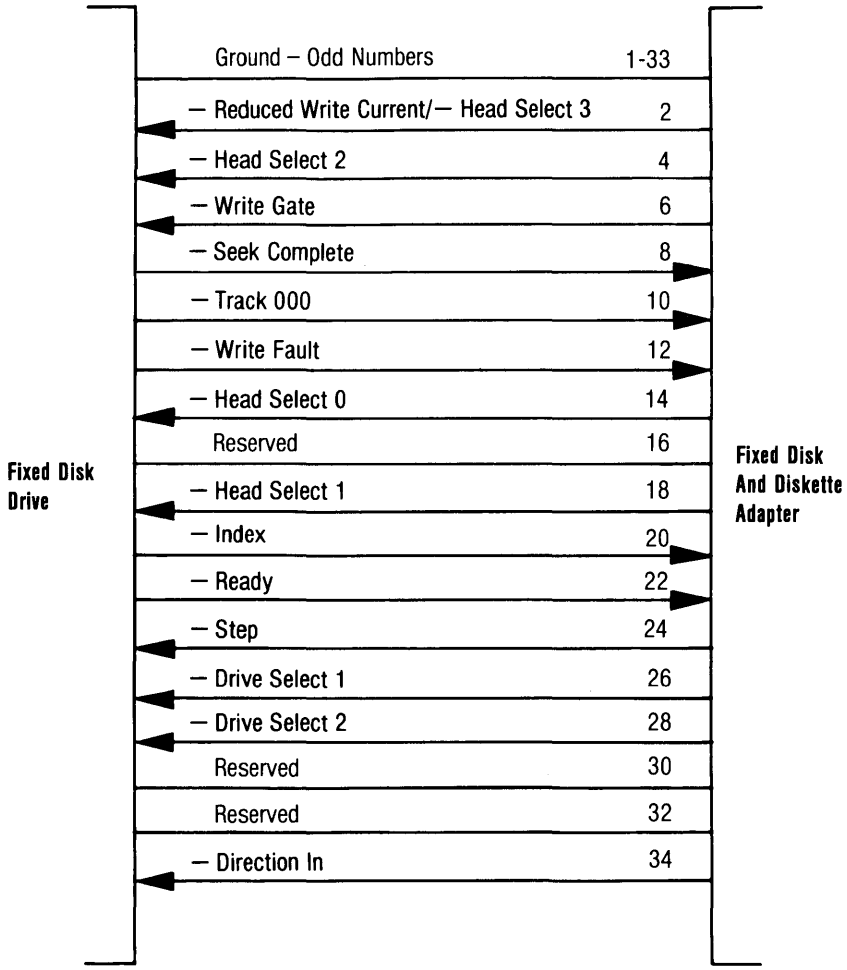
Bit 1 Unit Select 1 (US 1) — Status of the 'unit-select-1' signal from the diskette drive.

Bit 0 Unit Select 0 (US 0) — Status of the 'unit select 0' signal from the diskette drive.

Interface Lines

The interface to the fixed disk drive consists of two cables: 'control' and 'data'. The following figures show signals and pin assignments for these cables.

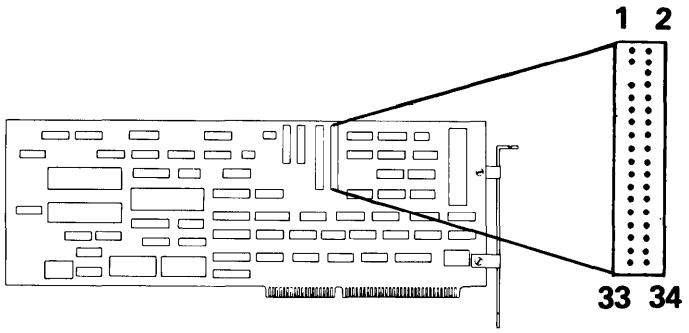


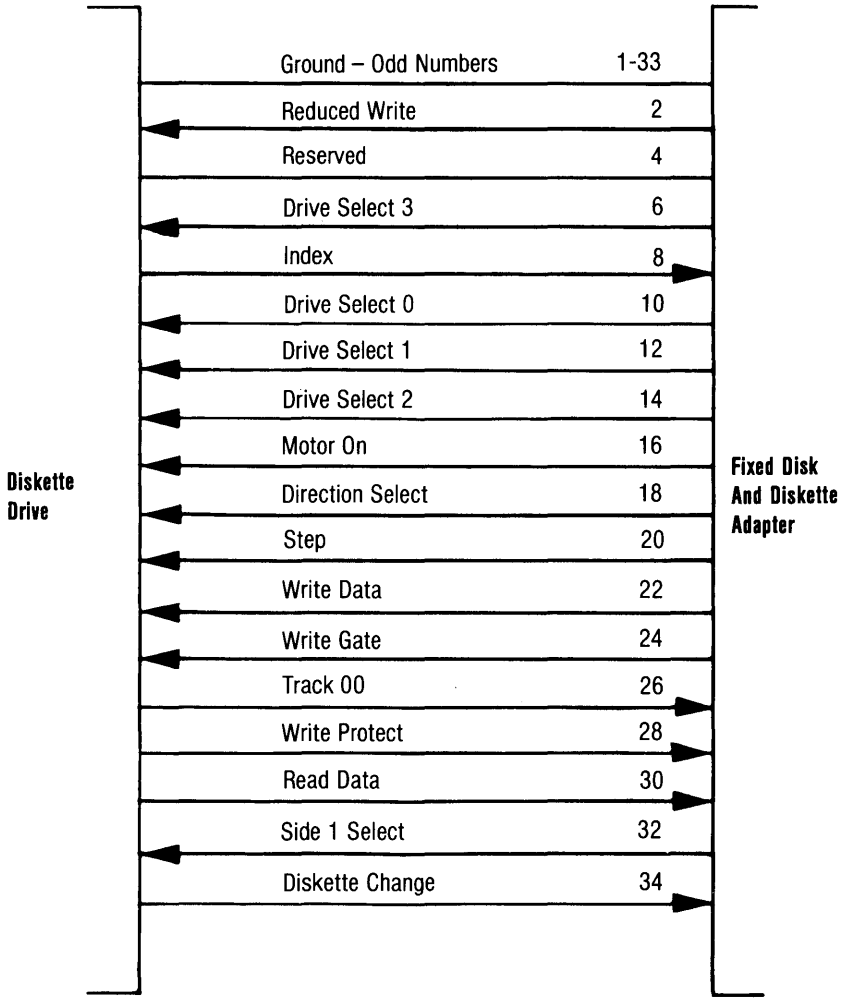


Note: Connection is through a 2-by-17 Berg connector. Pin 15 is reserved to polarize the connector.

Interface Lines *(continued)*

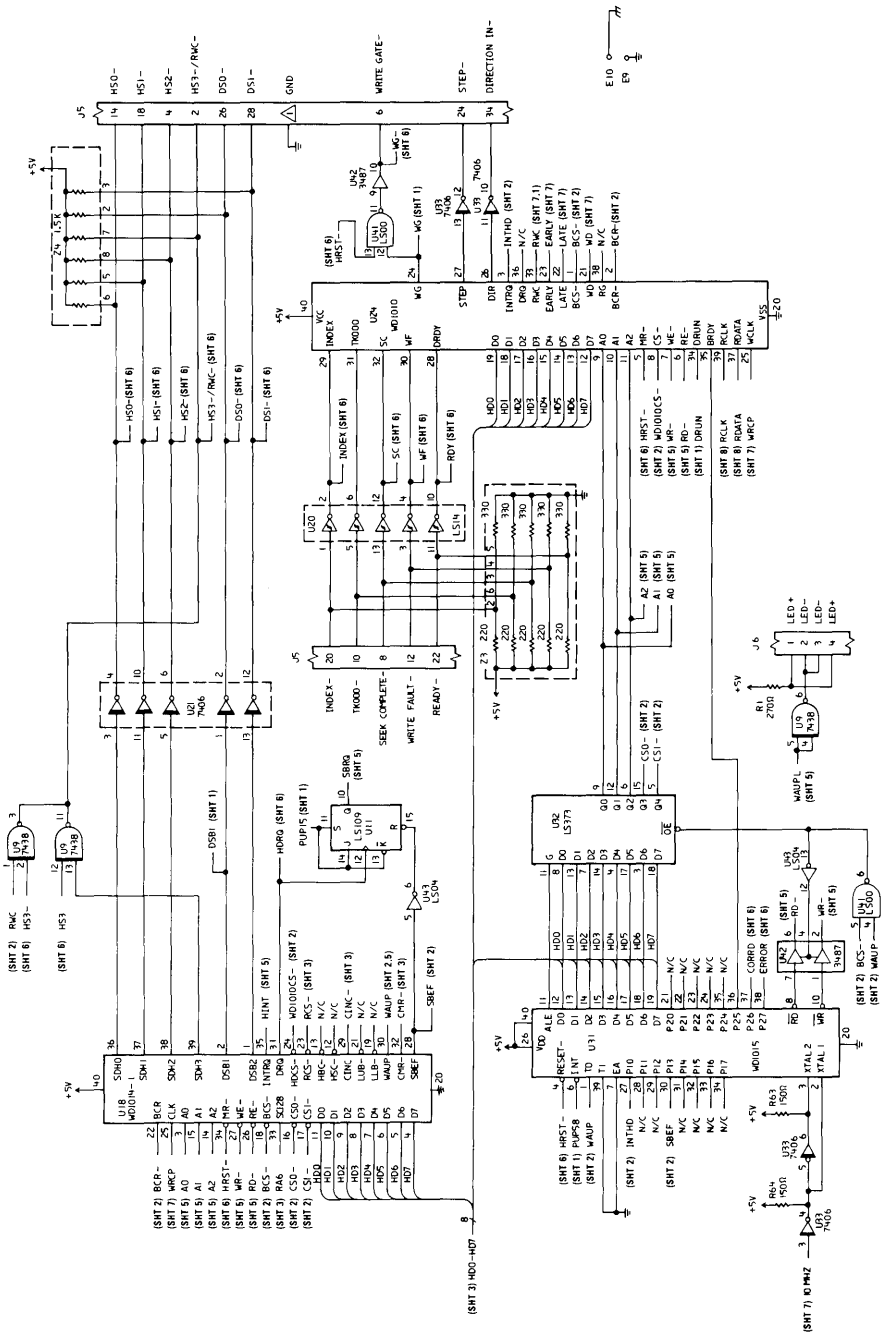
The interface to the diskette drives is a single cable that carries both data and control signals. The signals and pin assignments as follows.





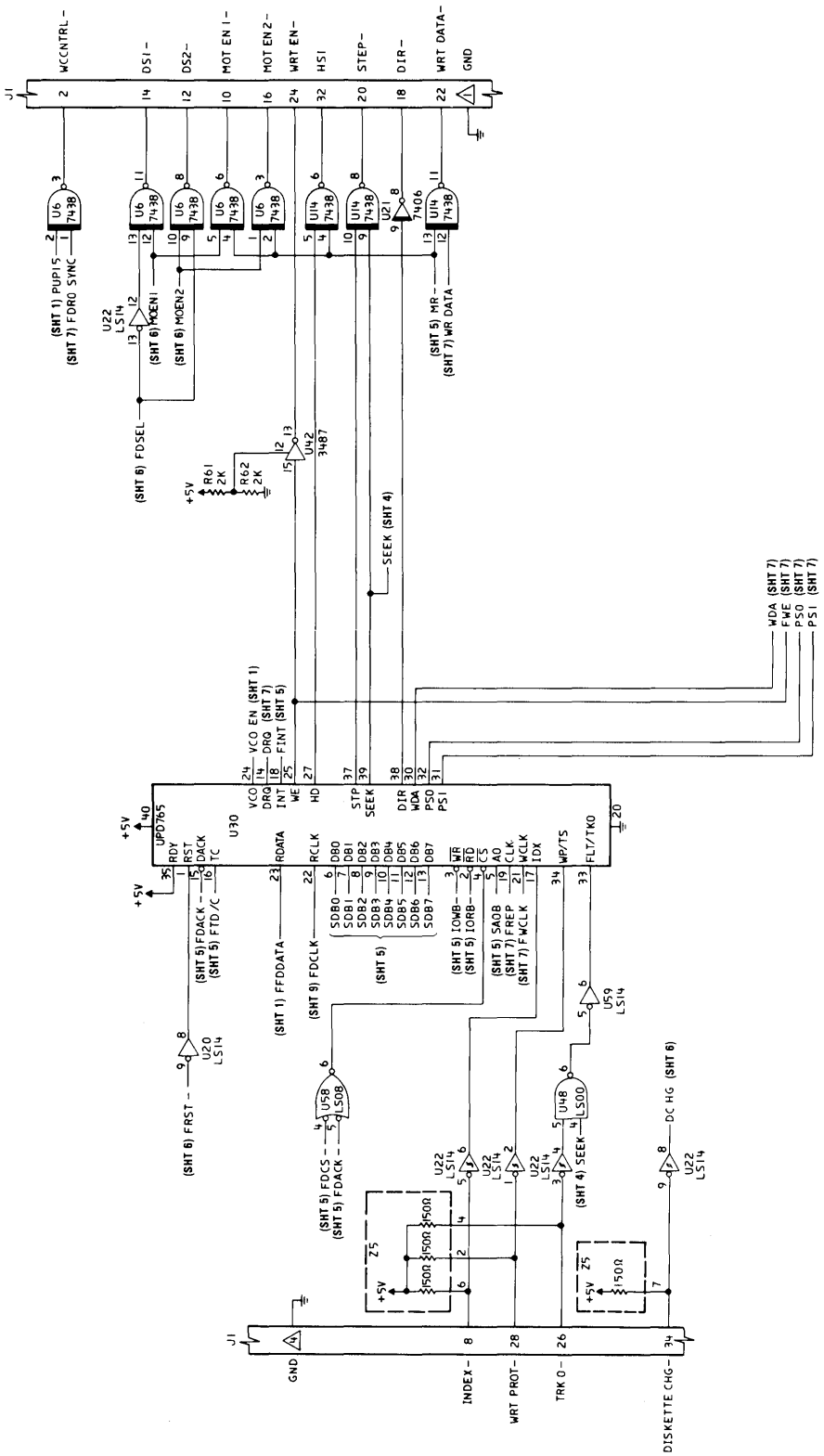
Note: Connection is through a 2-by-17 Berg connector. Pin 5 is reserved to polarize the connector.

Logic Diagrams *(continued)*



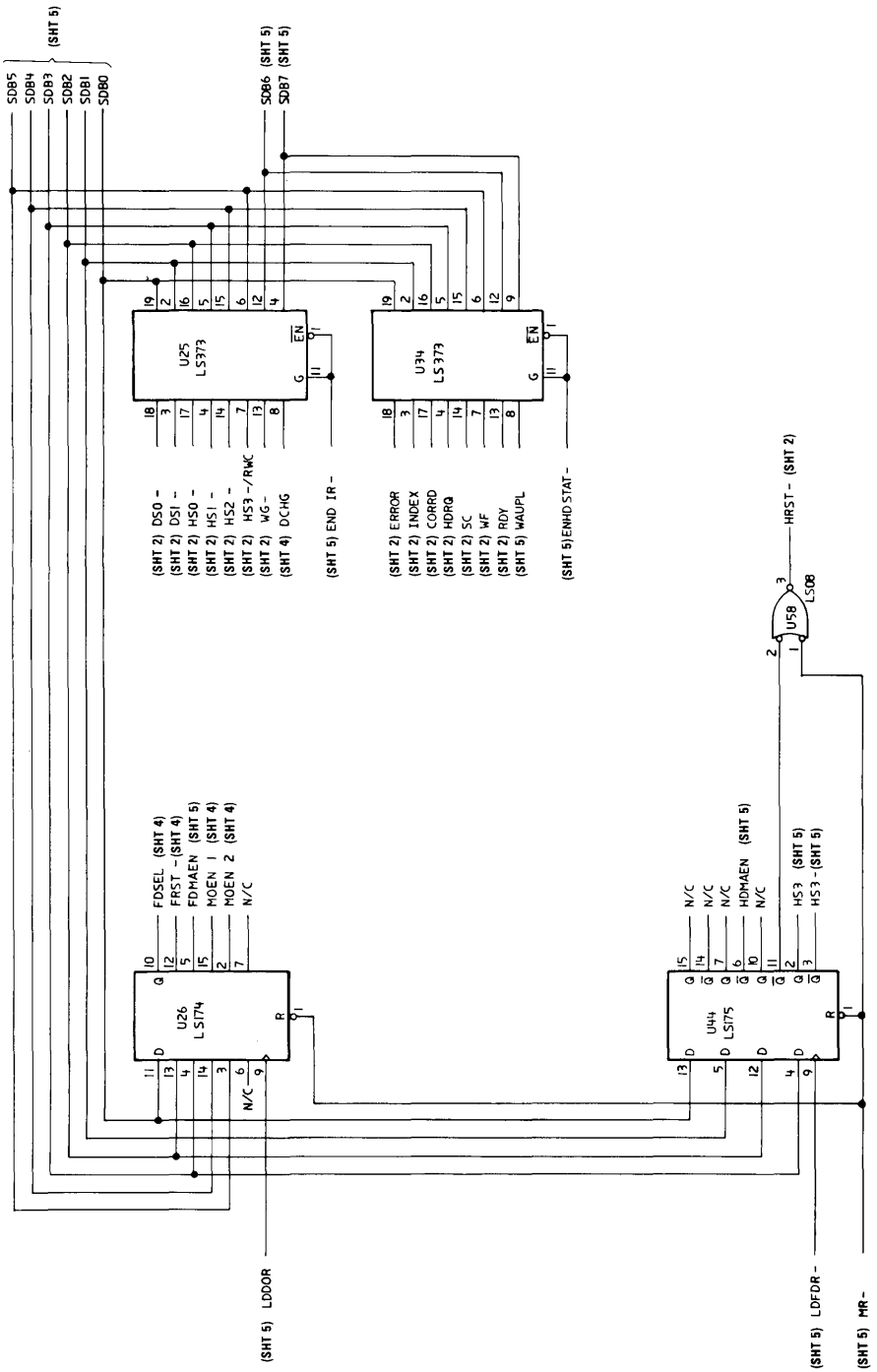
Fixed Disk and Diskette Drive Adapter (Sheet 2 of 9)

Logic Diagrams *(continued)*



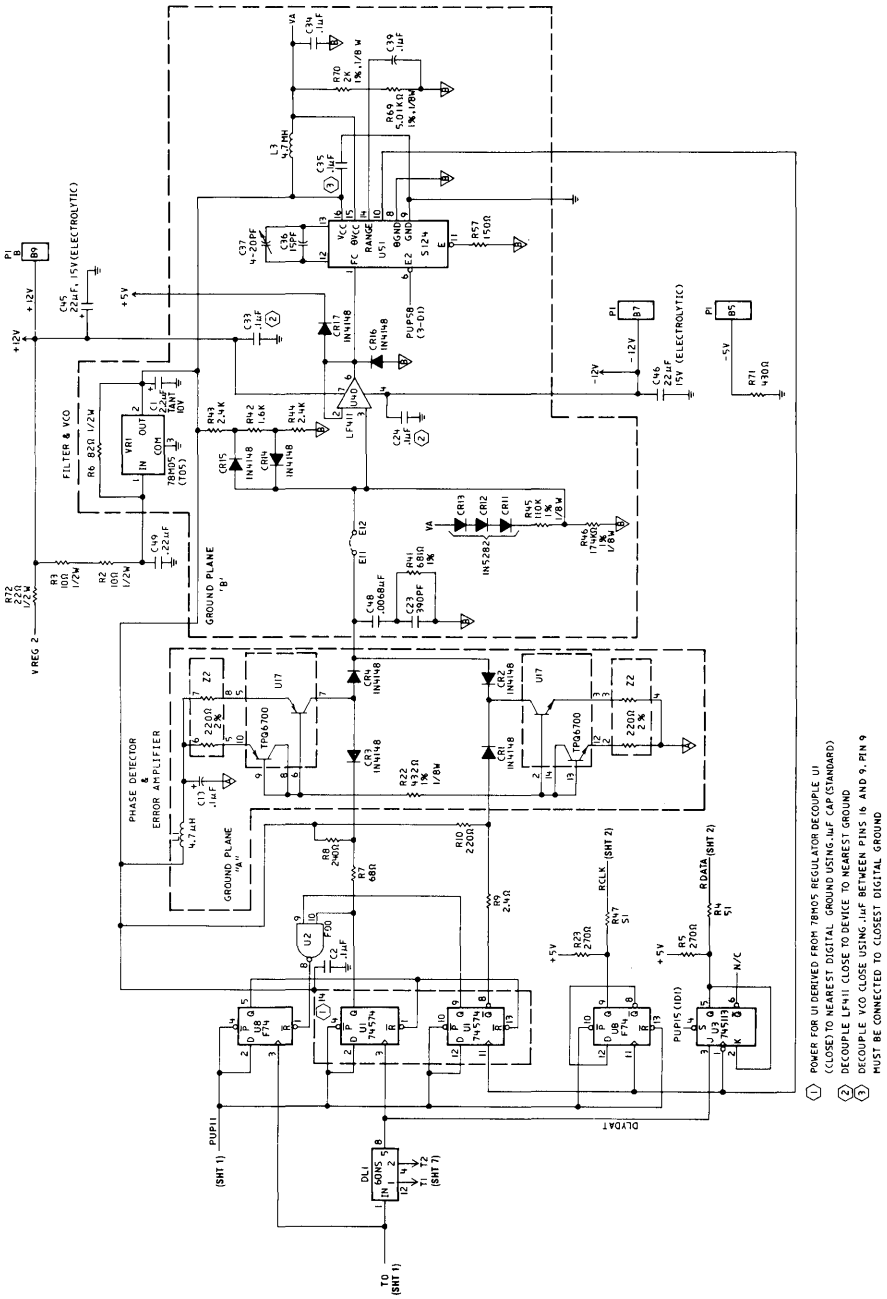
Fixed Disk and Diskette Drive Adapter (Sheet 4 of 9)

Logic Diagrams *(continued)*



Fixed Disk and Diskette Drive Adapter (Sheet 6 of 9)

Logic Diagrams *(continued)*



Fixed Disk and Diskette Drive Adapter (Sheet 8 of 9)

IBM Asynchronous Communications Adapter

Contents

IBM Asynchronous Communications Adapter

Description

The Asynchronous Communications Adapter's system control signals and voltage requirements are provided through a 2-by-31 position card-edge connector. Two jumper modules are provided on the adapter. One jumper module selects either RS-232C or current-loop operation. The other jumper module selects one of two addresses for the adapter, so two adapters may be used in one system. An additional jumper is required on connector J13 if the adapter is to be installed in expansion slot 8 (see "Selecting the Interface Format and Adapter Address" in this section).

The adapter is fully programmable and supports asynchronous communications only. It will add and remove start bits, stop bits, and parity bits. A programmable baud-rate generator allows operation from 50 baud to 9600 baud. Five-, six-, seven-, or eight-bit characters with 1, 1-1/2, or 2 stop bits are supported. A fully prioritized interrupt system controls transmit, receive, error, line status, and data set interrupts. Diagnostic capabilities provide loopback functions of transmit/receive and input/output signals.

The major component of the adapter is an INS8250 LSI chip or functional equivalent. Features in addition to those listed above are:

- Full double buffering eliminating the need for precise synchronization
- Independent receiver clock input
- False-start bit detection
- Line-break generation and detection

Programming Considerations

Modes Of Operation

The different modes of operation are selected by programming the 8250 Asynchronous Communications Element. This is done by selecting the I/O address (hex 3F8 to 3FF primary, and hex 2F8 to 2FF secondary) and writing data out to the adapter. Address bits A0, A1, and A2, select the different registers that define the modes of operation. Also, bit 7, the divisor latch access bit (DLAB), of the line-control register is used to select certain registers.

I/O decode (in hex)			
Primary adapter	Alternate adapter	Register selected	DLAB state
3F8	2F8	TX buffer	DLAB = 0 (Write)
3F8	2F8	RX buffer	DLAB = 0 (Read)
3F8	2F8	Divisor latch LSB	DLAB = 1
3F9	2F9	Divisor latch MSB	DLAB = 1
3F9	2F9	Interrupt enable register	
3FA	2FA	Interrupt identification registers	
3FB	2FB	Line control register	
3FC	2FC	Modem control register	
3FD	2FD	Line status register	
3FE	2FE	Modem status register	

I/O decodes

Programming Considerations *(continued)*

INS8250

The INS8250 has a number of accessible registers. The system programmer may access or control any of the INS8250 registers through the system-unit microprocessor. These registers are used to control INS8250 operations and to transmit and receive data. The following figure provides a listing and description of the accessible registers.

Register/signal	Reset control	Reset state
Interrupt enable register	Master reset	All bits low (0-3 forced and 4-7 permanent).
Interrupt identification register	Master reset	Bit 0 is high, bits 1 and 2 low, bits 3-7 are permanently low
Line control register	Master reset	All bits low
Modem control register	Master reset	All bits low
Line status register	Master reset	Except bits 5 and 6 are high
Modem status register	Master reset	Bits 0-3 low Bits 4-7 -input signal
SOUT	Master reset	High
INTRPT (RCVR errors)	Read LSR/MR	Low
INTRPT (RCVR data ready)	Read RBR/MR	Low
INTRPT (RCVR data ready)	Read IIR/ Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
OUT 2	Master reset	High
RTS	Master reset	High
DTR	Master reset	High
OUT 1	Master reset	High

Asynchronous communications reset functions

Bit 4: This bit is the even parity select bit. When bit 3 is a logical 1 and bit 4 is a logical 0, an odd number of logical 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logical 1 and bit 4 is a logical 1, an even number of bits is transmitted or checked.

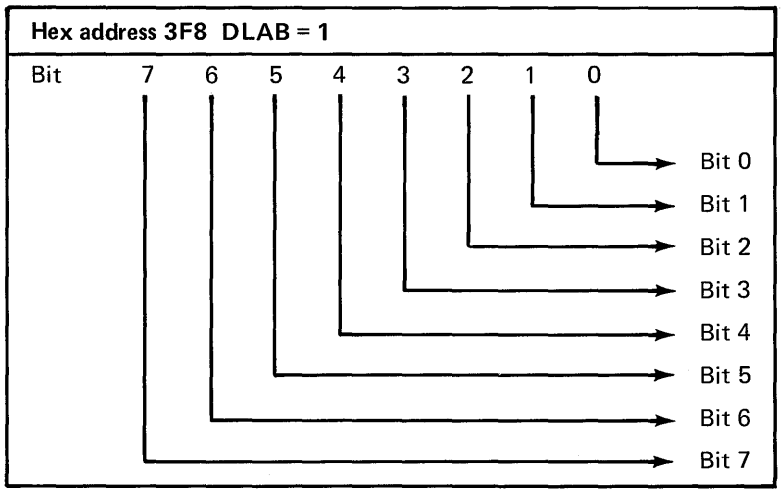
Bit 5: This bit is the stick parity bit. When bit 3 is a logical 1 and bit 5 is a logical 1, the parity bit is transmitted and then detected by the receiver as a logical 0 if bit 4 is a logical 1, or as a logical 1 if bit 4 is a logical 0.

Bit 6: This bit is the set break control bit. When bit 6 is a logical 1, the serial output (SOUT) is forced to the spacing (logical 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logical 0. This feature enables the system-unit microprocessor to alert a terminal in a computer communications system.

Bit 7: This bit is the divisor latch access bit (DLAB). It must be set high (logical 1) to access the divisor latches of the baud-rate generator during a read or write operation. It must be set low (logical 0) to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

Programmable Baud-Rate Generator

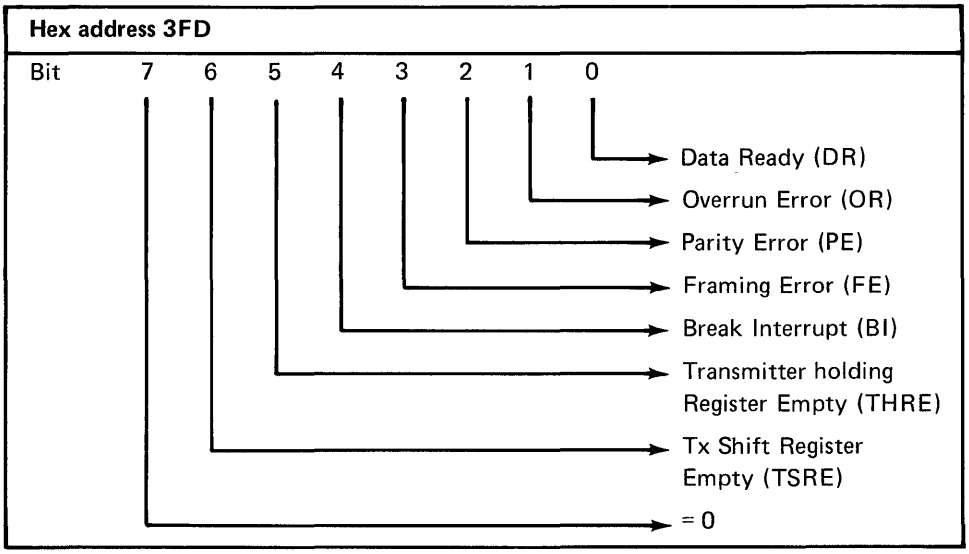
The INS8250 contains a programmable baud-rate generator that is capable of taking the clock input (1.8432 MHz) and dividing it by any divisor from 1 to (2^{16}-1). The output frequency of the baud generator is 16 x the baud rate (divisor # =(frequency input)/(baud rate x 16)). Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization in order to ensure desired operation of the baud-rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.



Divisor latch least significant bit (DLL)

Line Status Register (LSR)

This 8-bit register provides status information to the system-unit microprocessor concerning the data transfer. The contents of the line status register are indicated and described in the following figure.



Line status register (LSR)

Bit 0: This bit is the receiver data ready (DR) indicator. Bit 0 is set to logical 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. Bit 0 may be reset to a logical 0 either by the system-unit microprocessor reading the data in the receiver buffer register or by writing logical 0 into it from the system-unit microprocessor.

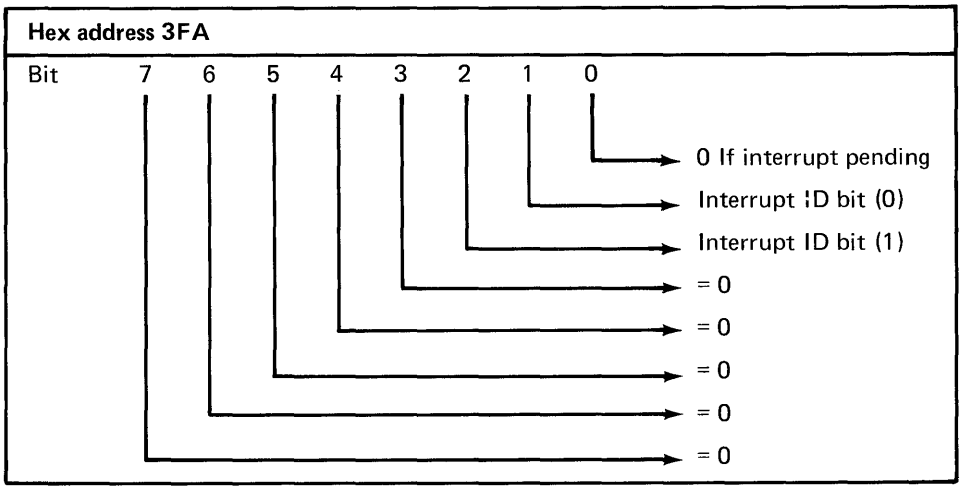
Bit 1: This bit is the overrun error (OE) indicator. Bit 1 indicates that data in the receiver buffer register was not read by the system-unit microprocessor before the next character was transferred into the receiver buffer register, thereby destroying the previous character. The OE indicator is reset whenever the system-unit microprocessor reads the contents of the line status register.

Bit 2: This bit is the parity error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity select bit. The PE bit is set to logical 1 upon detection of a parity error and is reset to logical 0 whenever the system-unit microprocessor reads the contents of the line status register.

Interrupt Identification Register (IIR)

The INS8250 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250 prioritizes interrupts into four levels: receiver line status (priority 1), received data ready (priority 2), transmitter-holding-register-empty (priority 3), and modem status (priority 4).

Information indicating that a prioritized interrupt is pending, and the type of prioritized interrupt, is stored in the interrupt identification register. Refer to the "Interrupt Control Functions" table on the next page. The interrupt identification register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending, and no other interrupts are acknowledged until that particular interrupt is serviced by the system-unit microprocessor. The contents of the IIR are indicated and described in the following figure.



Interrupt identification register (IIR)

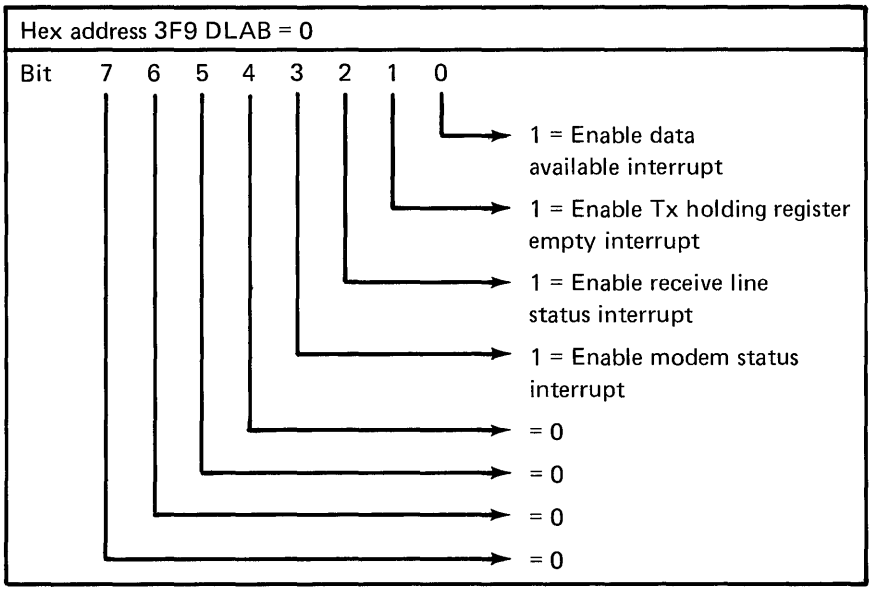
Bit 0: This bit can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending, and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is logical 1, no interrupt is pending, and polling (if used) is continued.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending, as indicated in the "Interrupt Control Functions" table.

Bits 3 through 7: These five bits of the IIR are always logical 0.

Interrupt Enable Register

This 8-bit register enables the four types of interrupt of the INS8250 to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt enable register. Similarly, by setting the appropriate bits of this register to logical 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the interrupt identification register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. The contents of the interrupt enable register are indicated and described in the following figure.



Interrupt enable register (IER)

Bit 0: This bit enables the received-data-available interrupt when set to logical 1.

Bit 1: This bit enables the transmitter-holding-register-empty interrupt when set to logical 1.

Bit 2: This bit enables the receiver-line-status interrupt when set to logical 1.

Bit 3: This bit enables the modem-status interrupt when set to logical 1.

Bits 4 through 7: These four bits are always logical 0.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts also are operational, but the interrupts' sources are now the lower four bits of the modem control register instead of the four modem control inputs. The interrupts are still controlled by the interrupt enable register.

The INS8250 interrupt system can be tested by writing into the lower four bits of the modem status register. Setting any of these bits to a logical 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to normal operation, the registers must be reprogrammed for normal operation, then bit 4 of the modem control register must be reset to logical 0.

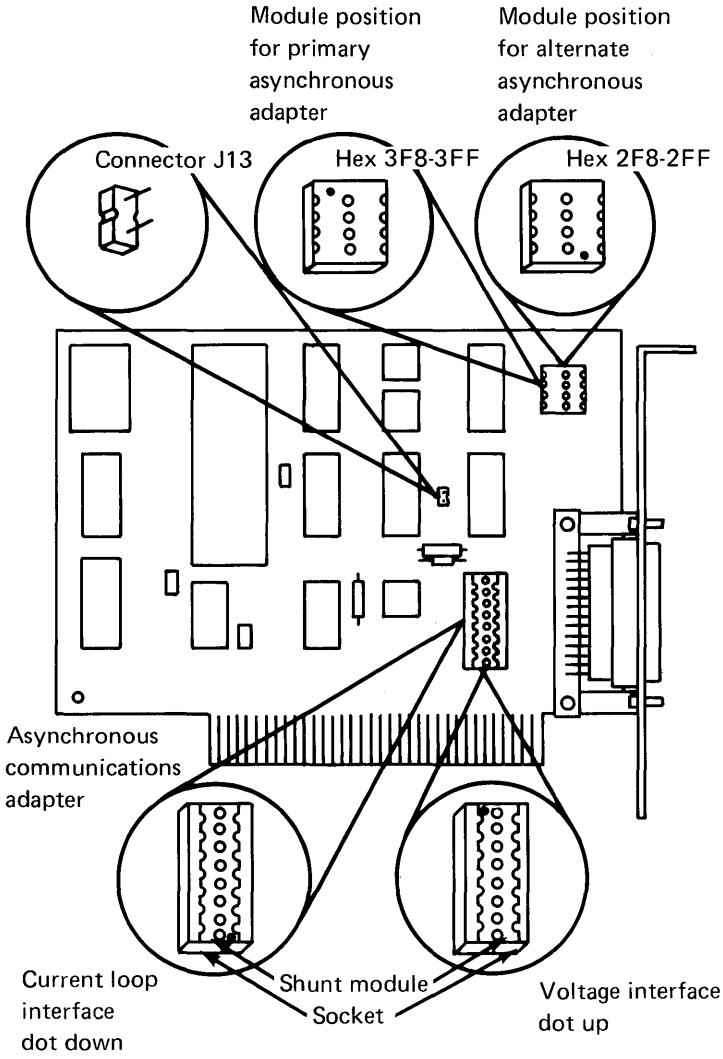
Bits 5 through 7: These bits are permanently set to logical 0.

Bit 6: This bit is the complement of the ring indicator (-RI) input. If bit 4 of the MCR is set to logical 1, the bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the received line signal detect (-RLSD) input. If bit 4 of the MCR is set to logical 1, the bit is equivalent to OUT 2 of the MCR.

Selecting the Interface Format and Adapter Address

The voltage or current-loop interface and adapter address are selected by plugging in programmed shunt modules with the locator dots up or down. See the following figure for the configurations.



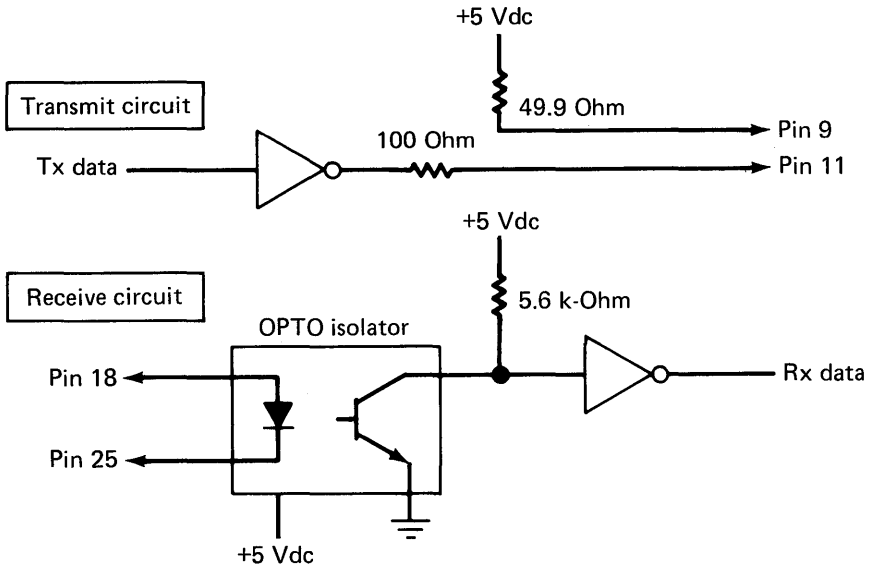
If the adapter is to be installed in expansion slot 8, a jumper is required on connector J13.

Interface

The communications adapter provides an EIA RS-232C-like interface. One 25-pin, D-shell, male connector is provided to attach various peripheral devices. In addition, a current-loop interface is also located in this same connector. A jumper block is provided to manually select either the voltage interface or the current-loop interface.

The current-loop interface is provided to attach certain printers provided by IBM that use this particular type of interface. IBM recommends that the current loop not be used beyond a distance of 15.3 meters (50 feet) as measured by the length of cable between the two interconnected points.

Pin 18	+ receive current loop data
Pin 25	- receive current loop return
Pin 11	- transmit current loop data
Pin 9	+ transmit current loop return



Current loop interface

For interface control circuits, the function is on when the voltage is more positive than +3 Vdc with respect to signal ground and is off when the voltage is more negative than -3 Vdc with respect to signal ground.

INS8250 Functional Pin Description

The following describes the function of all INS8250 input/output pins. Some of these descriptions refer to internal circuits.

> **Note:** In the following descriptions, a low represents a logical 0 (0 Vdc nominal) and a high represents a logical 1 (+2.4. Vdc nominal).

Input Signals

Chip Select (CS0, CS1, -CS2), Pins 12-14: When CS0 and CS1 are high and -CS2 is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) address strobe (-ADS) input. This enables communications between the INS8250 and the system-unit microprocessor.

Data Input Strobe (DISTR, -DISTR), Pins 22 and 21: When DISTR is high or -DISTR is low while the chip is selected, it allows the system-unit microprocessor to read status information or data from a selected register of the INS8250.

> **Note:** Only an active DISTR or -DISTR input is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the -DISTR line input permanently high, if not used.

Data Output Strobe (DOSTR, -DOSTR), Pins 19 and 18: When DOSTR is high or -DOSTR is low while the chip is selected, it allows the system-unit microprocessor to write data or control words into a selected register of the INS8250.

> **Note:** Only an active DOSTR or -DOSTR input is required to transfer data to the INS8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the -DOSTR input permanently high, if not used.

Address Strobe (-ADS), Pin 25: When low, provides latching for the register select (A0, A1, A2) and chip select (CS0, CS1, -CS2) signals.

> **Note:** An active -ADS input is required when the register select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the ADS input permanently low.

Register Select (A0, A1, A2), Pins 26-28: These three inputs are used during a read or write operation to select an INS8250 register to read or write to as indicated in the following table. Note that the state of the divisor latch access bit (DLAB), which is the most significant bit of the line-control register, affects the selection of certain INS8250 registers. The DLAB must be set high by the system software to access the baud-rate generator divisor latches.

Received Line Signal Detect (-RLSD), Pin 38: When low, indicates that the data carrier had been detected by the modem or data set. The -RLSD signal is a modem-control function input whose condition can be tested by the system-unit microprocessor by reading bit 7 (RLSD) of the modem status register. Bit 3 (DRLSD) of the modem status register indicates whether the RLSD input has changed state since the previous reading of the modem status register.

> **Note:** Whenever the RLSD bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

Ring Indicator (-RI), Pin 39: When low, indicates that a telephone ringing signal has been received by the modem or data set. The -RI signal is a modem-control function input whose condition can be tested by the system-unit microprocessor by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates whether the -RI input has changed from a low to high state since the previous reading of the modem status register.

> **Note:** Whenever the RI bit of the modem status register changes from a high to a low state, an interrupt is generated if the modem status interrupt is enabled.

VCC, Pin 40: +5 Vdc supply.

VSS, Pin 20: Ground (0 Vdc) reference.

Output Signals

Data Terminal Ready (-DTR), Pin 33: When low, informs the modem or data set that the INS8250 is ready to communicate. The -DTR output signal can be set to an active low by programming bit 0 (DTR) of the modem control register to a high level. The -DTR signal is set high upon a master reset operation.

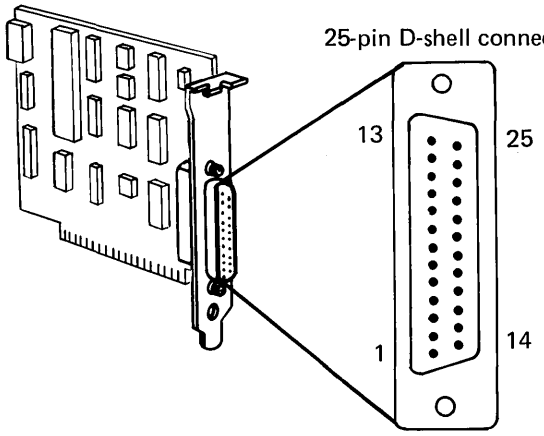
Request to Send (-RTS), Pin 32: When low, informs the modem or data set that the INS8250 is ready to transmit data. The -RTS output signal can be set to an active low by programming bit 1 (RTS) of the modem control register to a high level. The -RTS signal is set high upon a master reset operation.

Output 1 (-OUT 1), Pin 34: User-designated output that can be set to an active low by programming bit 2 (-OUT 1) of the modem control register to a high level. The -OUT 1 signal is set high upon a master reset operation.

Output 2 (-OUT 2), Pin 31: User-designated output that can be set to an active low by programming bit 3 (-OUT 2) of the modem control register to a high level. The -OUT 2 signal is set high upon a master reset operation.

Connector Specifications

The following page shows the connecter pin assignments and specifications for the Asynchronous Communications Adapter.



	Description	Pin	
	No connection	1	
	Transmitted data	2	
←	Received data	3	
	Request to send	4	→
←	Clear to send	5	
	Data set ready	6	→
	Signal ground	7	
	Received line signal detector	8	→
←	+ Transmit current loop data	9	
	No connection	10	
←	− Transmit current loop data	11	
	No connection	12	
External device	No connection	13	Asynchronous communications adapter (RS-232C)
	No connection	14	
	No connection	15	
	No connection	16	
	No connection	17	
	+ Receive current loop data	18	→
	No connection	19	
	Data terminal ready	20	
←	No connection	21	
	Ring indicator	22	→
	No connection	23	
	No connection	24	
	− Receive current loop return	25	→

Note: To avoid inducing voltage surges on interchange circuits, signals from interchange circuits shall not be used to drive inductive devices, such as relay coils.

Connector specifications

IBM Binary Synchronous Communications Adapter

Contents

IBM Binary Synchronous Communications Adapter

Description

The IBM Binary Synchronous Communications (BSC) Adapter provides an RS-232C-compatible communications interface for the IBM 5531 Industrial Computer family of products. All system control, voltage, and data signals are provided through a 2-by-31 position card-edge connector. External interface is in the form of Electronic Industries Association (EIA) drivers and receivers connected to an RS-232C, standard 25-pin, D-shell connector.

The adapter is programmed to operate in a binary synchronous mode. Maximum transmission rate is 9600 bits per second (bps). The main feature of the adapter is an Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART). An Intel 8255A-5 Programmable Peripheral Interface (PPI) also is used for expanded modem operation, and an Intel 8253-5 Programmable Interval Timer provides time-outs and generates interrupts.

Programming Considerations

Before starting data transmission or reception, the system unit programs the BSC adapter to define control and gating ports, timer functions and counts, and the communications environment.

Typical Programming Sequence

The 8255A-5 Programmable Peripheral Interface (PPI) is set for the proper mode by selecting address hex 3A3 and writing the control word. This defines port A as an input, port B as an output for modem control and gating, and port C for 4-bit input and 4-bit output. An output to port C sets the adapter to the wrap mode, disallows interrupts, and gates external clocks (address = hex 3A2, data = hex 0D). The adapter is now isolated from the communication interface, and setup continues.

Bit 4 of the PPI's port B brings the USART reset pin high, holds it, then drops it. This resets the internal registers of the USART.

The USART uses the 8253-5 Programmable Interval Timer (PIT) in the synchronous mode for inactivity time-outs to interrupt the system unit after a preselected amount of time has elapsed from the start of a communication operation. Counter 0 is not used for synchronous operation. Counters 1 and 2 connect to interrupt-level 4 and, being programmed to terminal-count values, provide the desired time delay before generating a level-4 interrupt. These interrupts signal the system that a predetermined amount of time has elapsed without a TxRDY (level 4) or an RxRDY (level 3) interrupt being sent to the system unit.

USART Programming

After the support devices on the BSC adapter are programmed, the USART is loaded with a set of control words that defines the communication environment. The control words consist of mode instructions and command instructions.

Both the mode and command instructions must conform to a specified sequence for proper device operation. The mode instruction must be inserted immediately after a reset operation before using the USART for data communications. The required synchronization characters for the defined communication technique are then loaded into the USART (usually hex 32 for BSC). All control words written to the USART after the mode instruction will load the command instruction. Command instructions can be written to the USART in the data block any time during its operation.

To return to the mode instruction, the master reset bit in the command instruction word is set to start an internal reset operation, which places the USART back into the mode instruction. Command instructions must follow the mode instructions or synchronization characters.

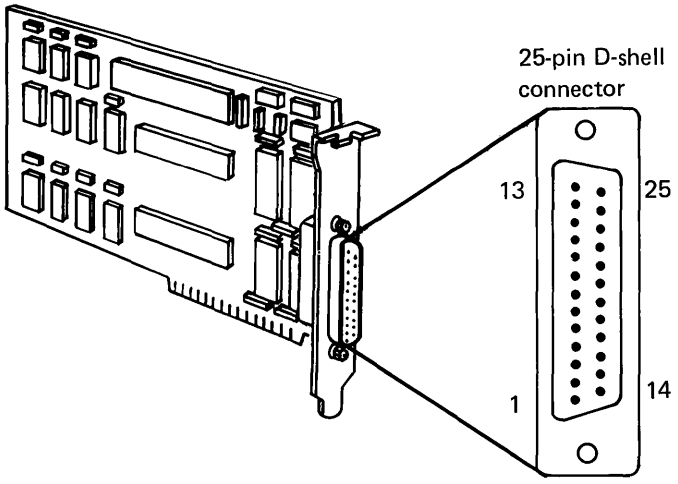
Programming Considerations *(continued)*

The following are device addresses:

Hex address		Device	Register name	Function
Primary	Alternate			
3A0	380	8255	Port A data	Internal/external sensing
3A1	381	8255	Port B data	External modem interface
3A2	382	8255	Port C data	Internal control
3A3	383	8255	Mode set	8255 mode initialization
3A4	384	8253	Counter 0 LSB	Not used in sync mode
3A4	384	8253	Counter 0 MSB	Not used in sync mode
3A5	385	8253	Counter 1 LSB	Inactivity time outs
3A5	385	8253	Counter 1 MSB	Inactivity time outs
3A6	386	8253	Counter 2 LSB	Inactivity time outs
3A6	385	8253	Counter 2 MSB	Inactivity time outs
3A7	387	8253	Mode register	8253 mode set
3A8	388	8251	Data select	Data
3A9	389	8251	Command status	USART status

Device address summary

Connector Specifications



	Signal name — description	Pin	
	No connection	1	
←	Transmitted data	2	
→	Received data	3	
←	Request to send	4	
→	Clear to send	5	
→	Data set ready	6	
	Signal ground	7	
→	Received line signal detector	8	
	No connection	9	
	No connection	10	
←	Select standby*	11	
←	No connection	12	
	No connection	13	
	No connection	14	
→	Transmitter signal element timing	15	
	No connection	16	
→	Receiver signal element timing	17	
←	Test (IBM modems only)*	18	
	No connection	19	
←	Data terminal ready	20	
	No connection	21	
→	Ring indicator	22	
←	Data signal rate selector	23	
	No connection	24	
	Test Indicate (IBM modems only)*	25	

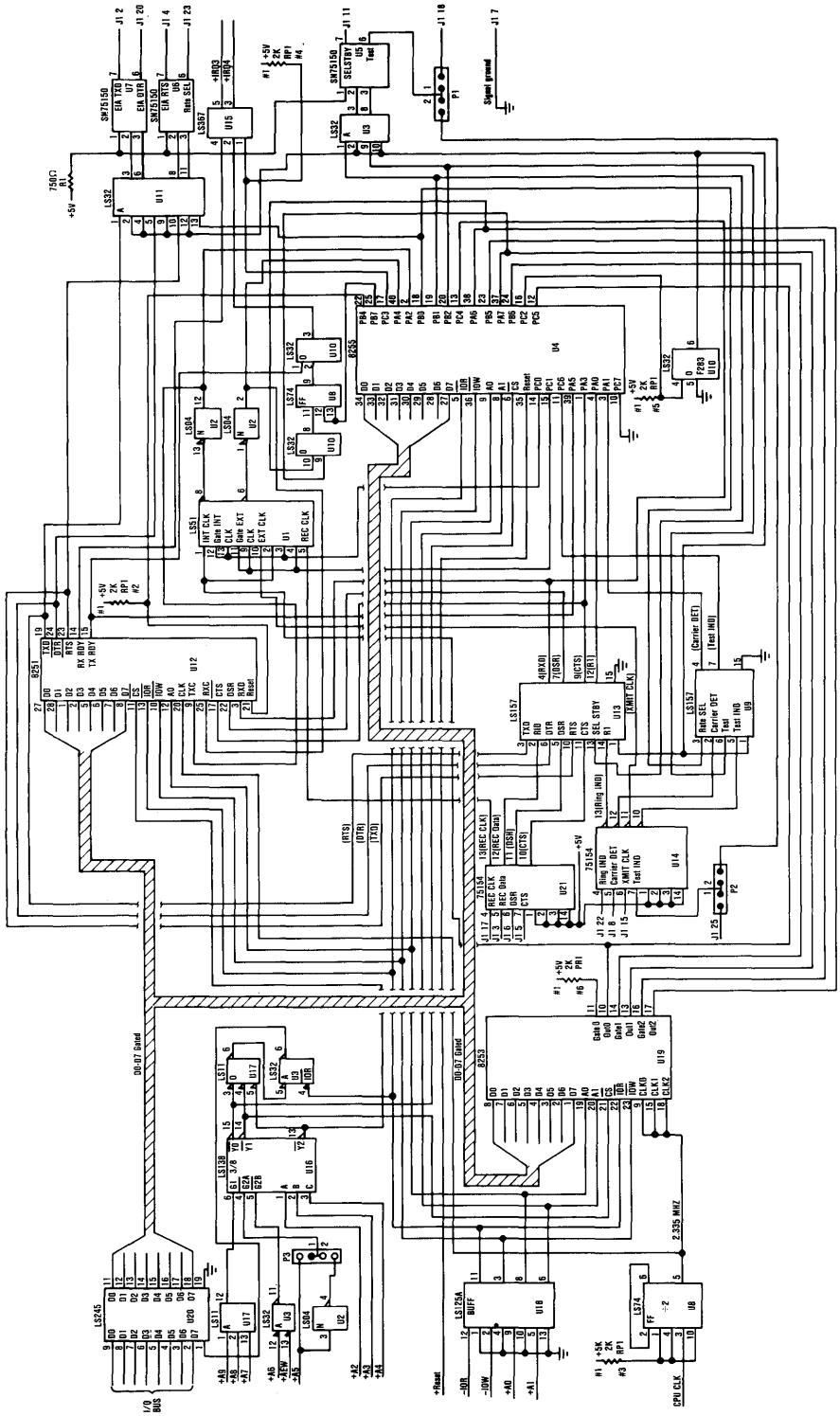
External device

Binary synchronous communications adapter

*Not standardized by EIA (Electronic Industries Association).

Connector specifications

Logic Diagrams *(continued)*



Binary synchronous communications adapter (Part 2 of 2)

IBM Synchronous Data Link Control (SDLC) Communications Adapter

Contents

IBM Synchronous Data Link Control (SDLC) Communications Adapter

Description

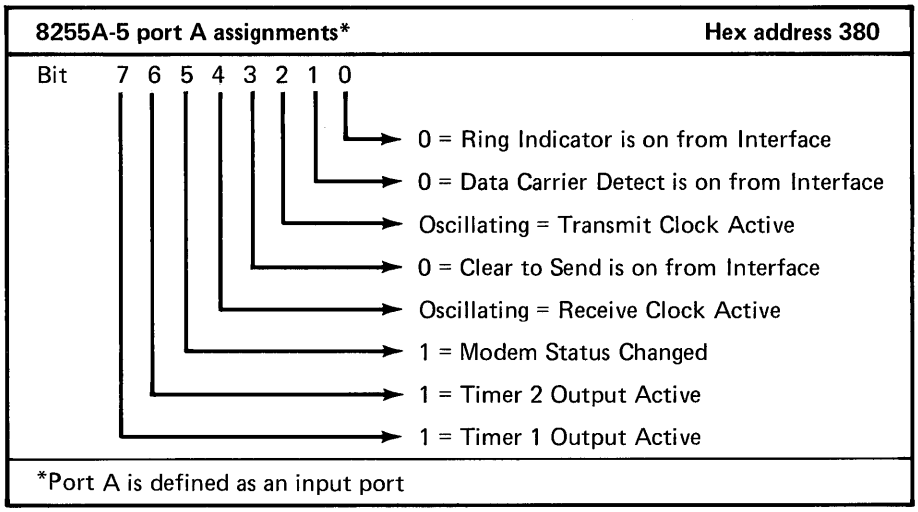
The IBM Synchronous Data Link Control (SDLC) Communications Adapter provides communications support to the system in a half-duplex synchronous mode. The adapter receives address, data, and control signals from the system board through the internal bus. Electronic Industries Association (EIA) drivers and receivers connect to an RS-232C standard 25-pin, D-shell, male connector.

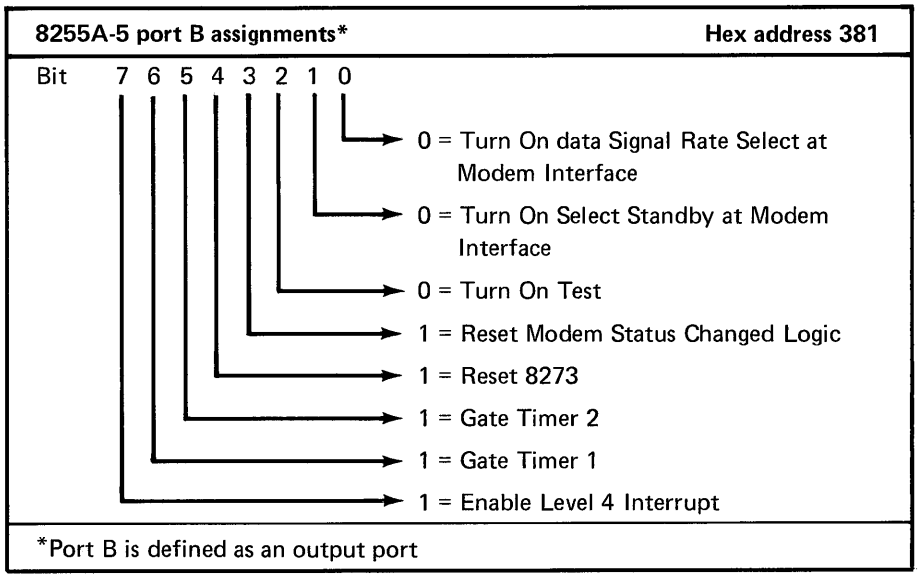
The adapter is programmed by communications software to operate in a half-duplex mode. Maximum transmission rate is 9600 bits per second, as generated by the attached modem or other data communications equipment.

The SDLC adapter uses an Intel 8273 SDLC Protocol Controller and an Intel 8255A-5 Programmable Peripheral Interface (PPI) for an expanded external modem interface. An Intel 8253 Programmable Interval Timer (PIT) generates timing and interrupt signals. Internal test-loop capability is provided for diagnostic purposes.

8255A-5 Programmable Peripheral Interface

The 8255A-5 PPI has three 8-bit ports: A, B, and C. Descriptions of each bit of these ports follow.





Programming Considerations

Initializing the Adapter (Typical Sequence)

Before the 8273 SDLC Protocol Controller is started, the support devices on the adapter must be set to the correct modes of operation.

Set up the 8255A-5 Programmable Peripheral Interface by selecting the mode set address for the PPI and by writing the appropriate control word to hex 98 to set ports A, B, and C to the modes described previously in this section.

Next, send a bit pattern to port C to disallow interrupts, set wrap mode on, and gate the external clock pins (address is hex 382, data is hex 0D). The adapter is now isolated from the communications interface.

The controller reset line is brought high through bit 4 of port B, held, then dropped. This action resets the internal registers of the controller.

8253-5 Programmable Interval Timer

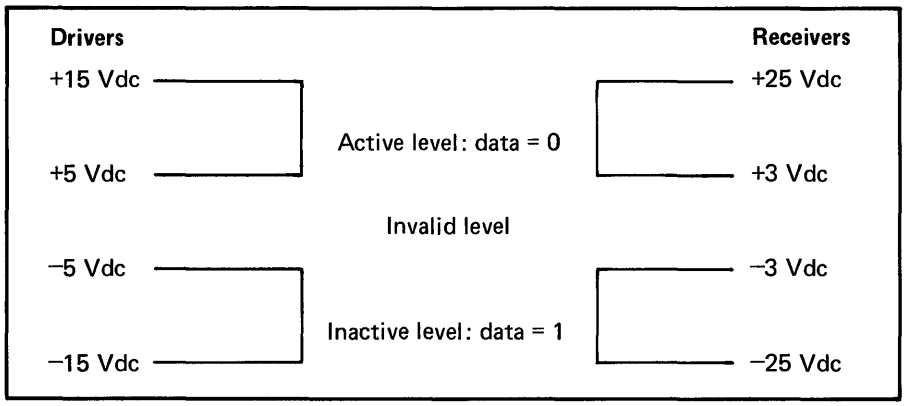
The PIT's counters 1 and 2 terminal-count values are set to values that will provide the desired time delay before a level-4 interrupt is generated. These interrupts may be used to indicate to the communication programs that a predetermined amount of time has elapsed without a result interrupt (interrupt-level 3). The terminal-count values for these counters are set for any time delay the programmer requires. Counter 0 also is set to mode 3 (generates square-wave signal used to drive counter 2 input).

The counter modes are set up by selecting the address for the PIT's counter-mode register and by writing the control word for each individual counter to the device separately.

When the support devices are set to the correct modes and the 8273 SDLC Protocol Controller is reset, it is ready to be set up for the operating mode that defines the communications environment in which it will be used.

Interface

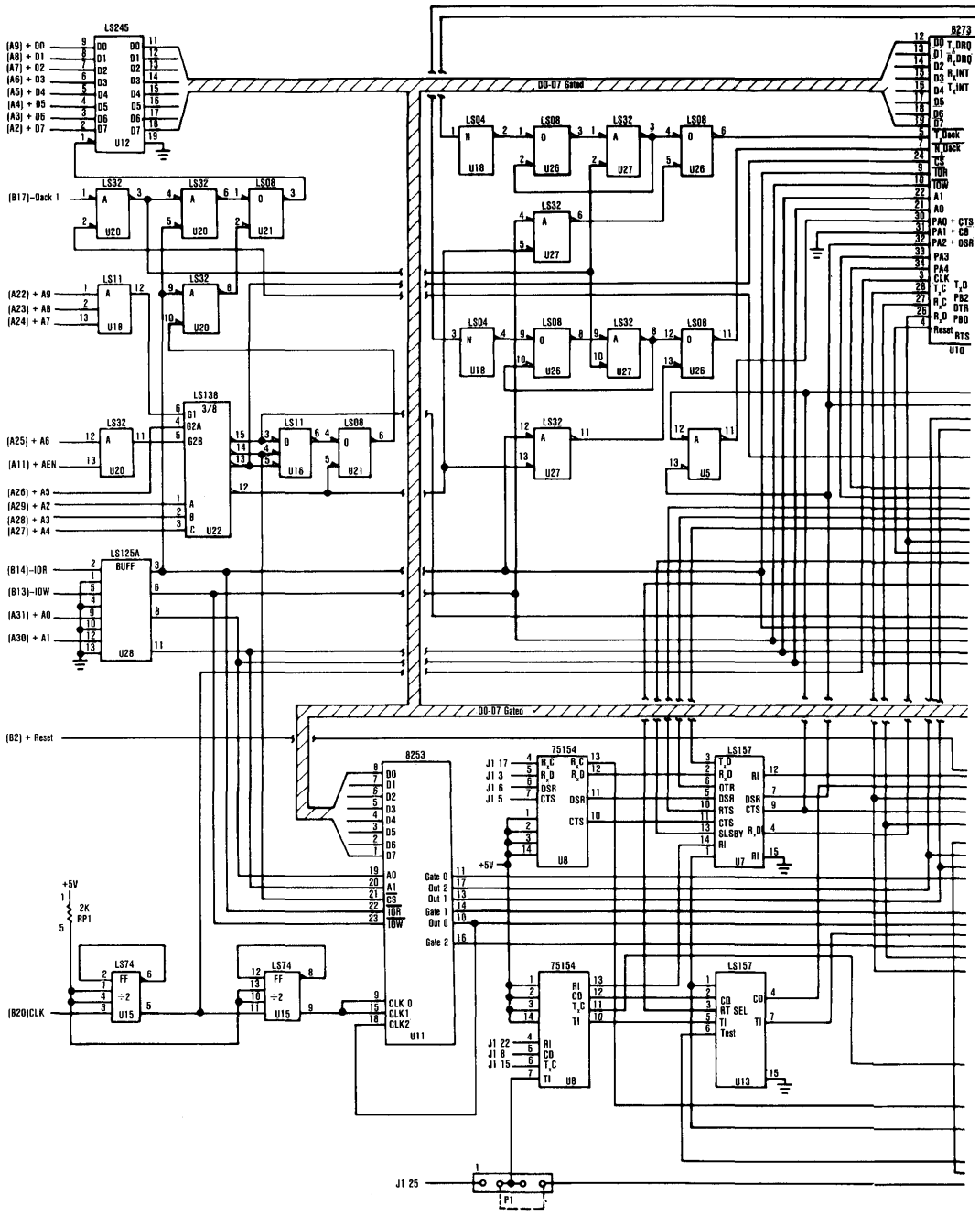
The SDLC Communications Adapter conforms to interface signal levels standardized by the Electronic Industries Association (EIA) RS-232C Standard. These levels are shown in the following figure.



Additional lines used but not standardized by the EIA are pins 11, 18, and 25. These lines are designated as "select standby," "test," and "test indicate," respectively. "Select standby" supports the switched network backup facility of a modem that has this option. "Test" and "test indicate" support a modem-wrap function for modems that are designed for business-machine controlled modem-wraps. Two jumpers on the adapter (P1 and P2) connect "test" and "test indicate" to the interface.

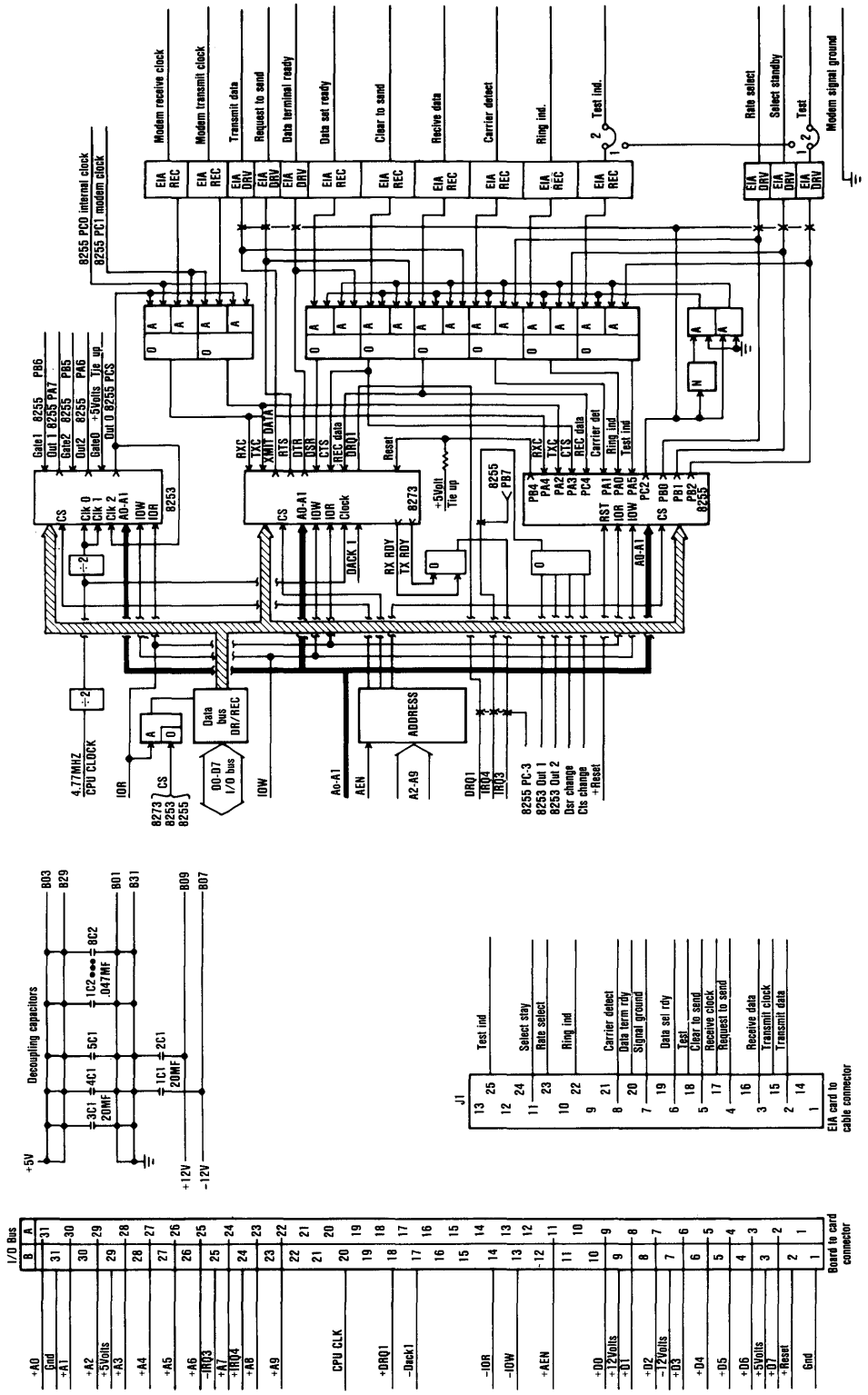
Logic Diagrams

The following pages contain the logic diagrams for the IBM Synchronous Data Link Control (SDLC) Adapter.



SDLC communications adapter (Part 1 of 3)

Logic Diagrams *(continued)*



SDLC communications adapter (Part 3 of 3)

IBM Cluster Adapter

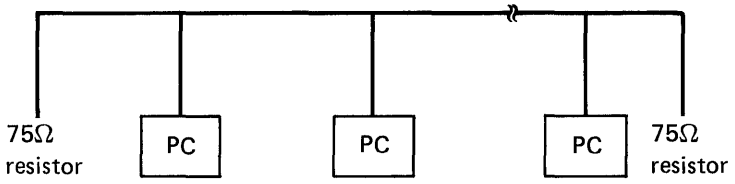
Contents

IBM Cluster Adapter

Description

The Cluster Adapter is a 10.16 cm (4 in.) high by 25.4 cm (10 in.) wide communication adapter used for linking up to 64 IBM 5531 Industrial Computers. The transmission rate is 375,000 bits per second (bps). A multi-drop bus architecture passively links (cluster operation is unaffected if the power to any station is off) the 5531s to a coaxial cable. The coaxial cable bus can be a maximum length of 1 km (3280 ft) and requires a 75-ohm terminating resistor at both ends to minimize signal reflection. The coaxial cable drop can be a maximum length of 5 m (16.4 ft) and a minimum length of 1 m (3.3 ft).

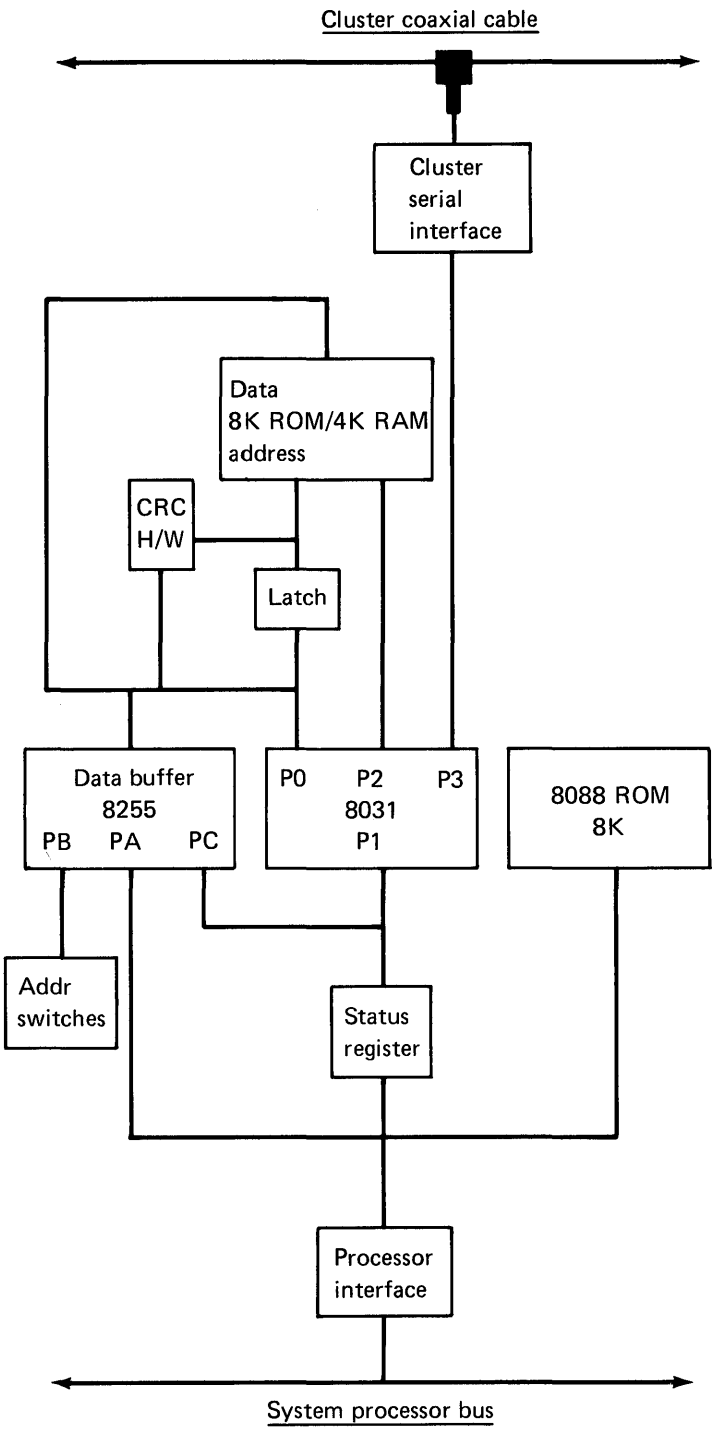
The following is an example of a cluster:



Cluster example

The IBM 5531 Industrial Computers share the bus through a distributed-access protocol called carrier sense multiple access with collision avoidance (CSMA/CA). With this protocol, each 5531 (station) that wants to transmit, calculates its own access-window wait time after no signal is sensed on the bus. The wait time differs for each station and changes with each transmission to prevent collisions (two stations transmitting at the same time). If cluster traffic is light (no signal is on the coaxial cable for approximately 2.8 milliseconds), a station that wants to transmit establishes cluster synchronization by transmitting all 1's (111 . . . 1) for 150 microseconds, thereby forcing a carrier sense transition (On-to-Off). The station can then calculate its access-window wait time.

The following is a block diagram of the Cluster Adapter:



Cluster adapter block diagram

8031 Ports

The 8031 on the Cluster Adapter provides external memory addresses through ports 0 and 2.

- Port 0 is an 8-bit, open-drain, bidirectional, I/O port used as the multiplexed low-order address and data bus.
- Port 2 is a bidirectional I/O port and provides the high-order address byte for the external memory.
- Port 1 of the 8031 is an 8-bit, bidirectional, I/O port used on the adapter for status conditions.
- Port 3 is an 8-bit, bidirectional, I/O port used as a serial port and as a source for external memory and serial-transmission control lines.

The following is a summary of the 8031 port signals:

	Port 0	Port 2	Port 3	Port 1
	External memory address			
Bits	Low order byte and data bus	High order address byte only	Transmission and control lines	Status
7	A7/D7	A15	–RD	Direction to 8031
6	A6/D6	A14	–WR	Error
5	A5/D5	A13	–CRC INT	Communication port busy
4	A4/D4	A12	–RTS	RX virtual I/O frame available
3	A3/D3	A11	+Internal Loop	RX frame in (FIFO)
2	A2/D2	A10	–Carrier Sense	Data available for 8088 (0 = active)
1	A1/D1	A9	+TXD	Command or data available for 8031
0	A0/D0	A8	+RXD	Command in progress

Summary of 8031 port signals

The following is the 8031 memory map:

Start address (hex)	Function
0000	DLCP ROM
2000	RAM
3000	8255 port A
3001	8255 port B
3002	8255 port C
3003	8255 control
3004	2653 character register
3005	2653 status register
3006	2653 mode register
3007	2653 CRC upper/lower registers

8031 memory map

8088 Accessible ROM

The 8088 (System Processor) Accessible ROM is an 8K x 8-bit ROM and contains the 8088 code necessary to perform the remote initial program load (IPL) and power-on diagnostic functions.

2653 Polynomial Generator Checker

The 2653 Polynomial Generator Checker is used by the 8031 Microcomputer to compute the Cyclic Redundancy Check (CRC) value for transmitted or received data blocks for error checking.

The 2653 is programmed by the 8031 in the automatic mode to generate the American National Standards Institute (ANSI) CRC-16 values. Two 8-bit characters are read from the 2653 character register into the Block Check Character (BCC) generation unit to calculate the 16-bit check character.

Programming is achieved as follows:

- The Clear CRC command, hex 02, is issued to the 2653 command register at address hex 3005.
- The Automatic Accumulation Mode command, hex 49, is issued to the 2653 mode register at address hex 3006.
- The Start Accumulation command, hex 01, is issued to the 2653 command register at address hex 3005.
- Characters to be accumulated are written to the character register at address hex 3004.

Cluster Adapter I/O Register Definitions

The following defines the Cluster Adapter I/O registers:

Adapter	I/O address (hex)	Device
Adapter 1	0790	Adapter status register
	0791	Adapter command data (output)
		Adapter result data (input)
	0792	Adapter interrupt register
	0793	Adapter reset control
Adapter 2	0B90	Adapter status register
	0B91	Adapter command/data (output)
		Adapter result/data (input)
	0B92	Adapter interrupt register
	0B93	Adapter reset control
Adapter 3	1390	Adapter status register
	1391	Adapter command/data (output)
		Adapter result/data (input)
	1392	Adapter interrupt register
	1393	Adapter reset control
Adapter 4	2390	Adapter status register
	2391	Adapter command/data (output)
		Adapter result/data (input)
	2392	Adapter interrupt register
	2393	Adapter reset control

Cluster adapter I/O registers

Definition of bits at port 0791 (for adapter 1) (Command or parameters for 8031)	
Bit	**Definition**
7	Command or Data Bit 7
6	Command or Data Bit 6
5	Command or Data Bit 5
4	Command or Data Bit 4
3	Command or Data Bit 3
2	Command or Data Bit 2
1	Command or Data Bit 1
0	Command or Data Bit 0

Cluster adapter command/data register (output)

Definition of bits at port 0791 (for adapter 1) (Result or data from 8031)	
Bit	**Definition**
7	Result or Data Bit 7
6	Result or Data Bit 6
5	Result or Data Bit 5
4	Result or Data Bit 4
3	Result or Data Bit 3
2	Result or Data Bit 2
1	Result or Data Bit 1
0	Result or Data Bit 0

Cluster adapter result/data register (input)

Cluster Adapter Interrupts

The Cluster Adapter may be set (one jumper selectable) to allow interrupts on either interrupt-level 3 or interrupt-level 7. An adapter error detected by diagnostic tests is reported if the interrupt jumper is missing. The received frames must be available or the Transmit operation complete (if initiated by a Transmit command with the Initiate Transmit bit set).

Up to four Cluster Adapters can be installed at a station. Each adapter can be enabled/disabled and all are similar in operation. If enabled, the adapter generates interrupts on levels 3 or 7 provided one of the following conditions is met:

- A received frame is available
- The Transmit Frame command is complete
- The Cluster Status command is complete.

The following description is for adapter 1:

- Interrupts are enabled by executing an output instruction to the adapter's interrupt enable register.

- Interrupts are disabled by writing the hex 00 instruction to the adapter's reset register. Also, additional interrupts are disabled by generating the interrupt request. The adapter must be re-enabled after each interrupt if additional interrupts are desired.

- To avoid resetting the adapter, data bit 0 must be set to a 0 when an output is sent to the adapter's reset register.

  No interrupt handler is provided for the cluster, and must be provided by the user who requires interrupt capability. The interrupt condition is provided in the adapter's interrupt register, as described in the Cluster Adapter Interrupt Status Bits table.

Higher Layer Communication Program BIOS Interface

When the Power switch is set to On, the hex 5A software interrupt vector is set to the address of the Cluster Adapter BIOS by the adapter's self-test diagnostic code.

Notes:

1. The DLCP must be initialized before it can process most of its commands.

2. Interrupt hex 5A is reserved for the Cluster Adapter BIOS and should not be changed.

The higher layer communication program must access the Cluster Adapter BIOS through an interrupt hex 5A instruction. The program must set the Extra Segment (ES) Register output to the segment and the Base Index (BX) Register output to the offset of the Link Control Block (LCB) before invoking the cluster DLCP BIOS. All parameters, the return code, and the cluster status are passed through the LCB.

The format of the LCB is shown below:

Link Control Block (LCB)	Number of bytes
Destination station physical address	1
Source station physical address	1
Command	1
Buffer 1 length	2
Buffer 1 address	2 (offset)
	2 (segment)
Buffer 2 length	2
Buffer 2 address	2 (offset)
	2 (segment)
Return code	1
Cluster status	1
Select adapter	1

Structure of Link Control Block (LCB)

The following control frame is transmitted by the DLCP when the Power switch is set to On or at initialization:

Initializing — Broadcast to all stations to indicate that the source station is in the process of initializing and all connections to that station should be set to the disconnected state. Also, if any station has the same station address, it sends a duplicate-address response back to the initializing station.

In addition, the DLCP determines if it is necessary to send a connect frame to establish connection with the destination station. If this station's Cluster Status table indicates that it is not connected to the destination station, the DLCP transmits a connect frame to establish connection and then transmits the information frame. If a not-connected control frame is received in response to the transmission of a frame, the DLCP transmits a connect frame to establish connection, then transmits the information frame.

Frame Format

The basic unit of information transmitted is a frame. The On-to-Off transition of the "carrier sense" signal identifies the beginning of a frame, and the Off-to-On transition identifies the end. A frame consists of fixed control fields and an optional variable-length information field. The following shows the format of a frame:

Field	Number of bytes	Note
Destination address	1	Control field
Source address	1	
Transmit window token	1	
Control	1	
Sequence	1	
Byte count	2	
Control CRC	2	
Information	1 to 578	Information field
Data CRC	2	

Frame format

Note: The minimum and maximum total number of bytes transmitted for a frame is 9 and 587, respectively. The transmission time for a frame ranges from approximately 1 millisecond (ms) for a minimum length frame up to approximately 16.5 ms for the maximum length frame. However, additional time may be required to gain access to the cluster before a frame can be sent.

Types of Frames Used by the DLCP

The following types of frames are used by the DLCP:

Acknowledge (hex 10)

Confirms receipt of a frame.

Initializing (hex 21)

Indicates that the source station is re-initializing. Existing connections to this station should be cleared.

Virtual Disk (hex 82)

Identifies that this frame contains a data block. Sent as a result of the source station issuing a Transmit Virtual Frame DLCP command. One buffer is reserved for this frame.

Information (hex 83)

Signifies the frame contains a data block. Sent as a result of the source station issuing a Transmit Frame DLCP command. There is a first-in-first-out (FIFO) buffer set aside for this frame.

Connect (hex 04)

Establishes the virtual point-to-point connection between a pair of stations.

Broadcast (hex 45)

Signifies that the frame is a broadcast or multicast frame.

Not Connected (hex 16)

Indicates that the receiving station is not connected to the sending station.

Frame Sequence Byte

If one of the acknowledge frames did not reach the transmitting station, the frame sequence byte is used to make sure that no duplicate information frames are received. The least-significant four bits in the Cluster Status Entry are used for maintaining a sequence number for transmitted and received frames. The first two bits are used for the sequence number for received frames. The two least-significant bits are used for the sequence number for transmitted frames. The sequence numbers are incremented each time a transmitting station sends an information frame and each time the receiving station accepts an information frame. If a mismatch occurs between the two stations, the sender marks the destination station in the disconnected state and sends a connect frame to try to reconnect with the destination station. If the connection attempt is successful, the frame is transmitted again.

Byte Count

The byte count is the number of information bytes to be transmitted. If the frame is a control frame, the byte count is zero. There are two bytes allocated for the byte count.

Control CRC

A 16-bit cyclic redundancy check (CRC) is calculated and appended to the end of the control block. A hardware CRC generator is used. The receiving station compares the control CRC received with the CRC calculated from the received data and makes sure they are the same. If they are not the same, the receiving station ignores the rest of the frame.

Data CRC

A 16-bit CRC is calculated and appended to the end of the data block. The receiving station compares the data CRC received with the CRC calculated from the received information bytes and makes sure they are the same. If they are not the same, the receiving station ignores the received frame.

Explanation of Timing

TR = Time allocated for a receiver to start transmitting a response.
T1 = Time delay for 1st Transmit Access Window.
T2 = Time delay for 2nd Transmit Access Window.
•
•
•
T64 = Time delay for 64th Transmit Access Window.
SN = Station N's address with the bits in reverse order.
Token = Transmit Window Token which is decremented by 2 for each transmitted frame.

Delay time for Station N = TR + ((Token + SN) mod 128) x transmit window/2.

Notes:

1. TR is approximately 200 μs.

2. Transmit Access Window is approximately 40 μs.

A station must see its Transmit Window flag change from Off to On before it is permitted to transmit. The case where it does not see the change is covered in the next section.

Explanation of Timing

TR = Time allocated for a receiver to start transmitting a response.
T1 = Time delay for 1st Transmit Access Window.
T2 = Time delay for 2nd Transmit Access Window.
•
•
•
T64 = Time delay for 64th Transmit Access Window.

Note: Average cluster access time is 1480 μs if the cluster is lightly loaded.

A station that is initializing waits the time of two complete synchronization periods before sending its broadcast initializing frame to allow it to become synchronized with the cluster. If no frames are received in that time, it uses the procedure above to establish a synchronized transmit period.

Frame Reception

The leading edge of the "carrier sense" signal is used to interrupt the 8031 Microcomputer. The 8031 interrupt service routine updates its Transmit Window Token to the value transmitted with the frame, and also sets the timer 0 counter to the calculated Transmit Access Window based on the new token value. If the frame is not addressed to this station, the DLCP ignores the rest of the frame and leaves the interrupt routine.

If the frame is addressed to the station, the DLCP checks the Cluster Adapter status to see if it can accept the frame. If this station is not connected to the source station then a not-connected control frame is transmitted to the source station. If the frame is out of sequence, an bad error control frame is transmitted to the source station.

If the DLCP can accept the frame, a check is made that a receive buffer is available. If a buffer cannot be obtained, a frame-reject control frame is sent back to the transmitting station. This indicates that the frame cannot be accepted at this time and another attempt should be made. If the frame is received correctly, DLCP transmits an Acknowledge frame to the transmitting station and return the control to the interrupted 8031 program.

Cluster Status Table

The DLCP keeps track of the status and sequence numbers for connection with stations 0 through 63 in the Cluster Table in the Cluster Adapter's RAM space. Offset 0 in the Cluster Table corresponds to the status for connection to station 0, offset 1 for station 1, and so on. The offset corresponding to a station's own address is used to store a duplicate-station address indicator.

The bits for each Cluster Status Table byte are designated in the following chart:

Cluster status entry (1 byte)		
C	7	1 = Connected
RB1	6	Response ID
RB0	5	Response ID
P	4	1 = response pending
RS1	3	Received frame sequence
RS0	2	Received frame sequence
TS1	1	Transmitted frame sequence
TS0	0	Transmitted frame sequence

Cluster status table entry

Bit 7 - Connected (C) is set to 1 when your station has sent a connect frame and an acknowledge frame has been received, or when a connect frame has been received and an acknowledge has been sent. Connected is reset when a not-connected, bad error, or initializing control frame is received.

Bit 6, 5 - Response ID

The following table defines the meaning of these two bits:

Bit 6 RB1	Bit 5 RB0	Type of response
0	0	Acknowledge
0	1	Frame Reject
1	0	Not Connected

Response ID in cluster table status entry

6. An acknowledge information frame is expected with the following data:

Command	=	hex 92	(Response to IPL request)
Session ID	=	hex xxxx	(2 bytes)
Status	=	hex 00	(Non-zero is irrecoverable error)

xxxx = any hexadecimal number

The server station's address is saved at the least-significant byte of vector INT hex E1.

Up to eight retries are made unless a response from the disk server station is received. Approximately 4 seconds are allowed between retries. After the eight retries have been used, the user timer-interrupt vector is restored and then control is passed to the bootstrap routine.

Note: If a Keep-Alive command is received from the disk server station, an additional 30 seconds is allowed.

7. Next, the Remote IPL program requests a data block containing program code from the disk server station. The request has the following form:

Command	=	hex 93	Request IPL data block
Session ID	=	hex xxxx	(2 bytes)
Status	=	hex 00	(Non-zero is irrecoverable error)

xxxx = any hexadecimal number

The request is sent using the DLCP BIOS command's Transmit Frame (hex 03). Retries are made for up to 20 seconds if the return code indicates a Frame Reject or a No Response error.

9. The above two steps are repeated until the end of the program code is received. The user timer-interrupt vector is restored and control passes to the loaded program by a jump to hex 07C0:0000.

Notes:

1. The Remote IPL function is performed, even if local drives are attached, if the Remote IPL switch on Cluster Adapter 1 is On. Remote IPL is supported only for Cluster Adapter 1. The Remote IPL function can be stopped by pressing Control Break, and normal loading from local diskette drives occurs.

2. For every block of data received, an arrow rotates in a clockwise direction on the screen.

3. After power-on or system reset, the cursor is moved to the right three columns for about one second. Special ROM diagnostic tests for the adapter can be executed by immediately pressing "Ctrl D" on the keyboard. Also, a request to load a general diagnostic program over the cluster can be selected by pressing "Ctrl L" at which time a blinking L is displayed. The adapter sends out a broadcast frame requesting a diagnostic program load. (The first data byte of the request frame is set to hex 90.)

DLCP Return Codes

The following table indicates the Return Codes that are defined for the cluster DLCP:

DLCP return codes	
Return code	**Meaning**
Hex 00	Successful completion
Hex 30	Initialization failed
Hex 31	Cluster busy timeout (carrier sense active for 2 seconds)
Hex 32	Duplicate station address on cluster
Hex 33	No response from destination
Hex 34	Frame rejected at destination
Hex 35	Reserved
Hex 36	Cluster access timeout (could not gain access to cluster within a 13 second timeout)
Hex 37	Information field too long (more than 578 bytes)
Hex 38	Information field empty
Hex 39	DLCP command in progress
Hex 3A	Initialization required
Hex 3B	Received frame not available
Hex 3C	Error detected with 8031 (due to command timeout or other processor interface error
Hex 3D	Extended return code in cluster status field
Hex 3E	Invalid initialization parameters (too many or too large buffers specified)
Hex 3F	Previous DLCP BIOS command initiated with Initiate Transmit bit set is not complete

Cluster DLCP return codes

Note: A return code of hex 00 indicates successful completion of the DLCP BIOS command. Most of the other return codes indicate error conditions.

Initialization Control Block (ICB)

The calling program must set the buffer 1 address field in the LCB to the address of an initialization control block (ICB). The figure below shows the composition and bytes that make up the ICB:

Byte	Byte definition	Value
0	(Bits) 7 6 5 4 3 2 1 0	0
	(Value) 0 0 0 0 0 NVB MM1 MM2	
1	Number of large buffers	4
2	Number of small buffers	10
3	Large buffer size	584 ÷ 8
4	Samll buffer size	40
5	Maximum number of retries for no response	8
6	Maximum number of retries for rejected frame	2
7	Transmit Access Window (TAW)	40 ÷ 2
8	Time period reserved for response	200 ÷ 20
9	Time from frame start to first byte	150 ÷ 2
10	Time between control field and data field	100 ÷ 2
11	Timeout waiting for response to be received	300 ÷ 6
12	Timeout waiting for next byte to be received	300 ÷ 6
13	Timeout waiting for command to complete	7
14	Timeout waiting to access cluster	200

Initialization Control Block (ICB)

Byte 1 - This byte indicates the number of large buffers allocated in the 8031 RAM for incoming frames.

Byte 2 - This byte indicates the number of small buffers allocated in the 8031 RAM for incoming frames.

Byte 3 - This byte indicates the large buffer size (each unit represents 8 bytes). Six bytes of the large buffer are reserved for control information.

Byte 4 - This byte indicates the small buffer size (each unit represents 1 byte). Six bytes of the small buffer are reserved for control information.

Byte 5 - This byte indicates the maximum number of times a frame is transmitted with no response from the destination station.

Byte 7 - This byte is used to specify the Transmit Access Window (TAW) time period in microseconds. For a 40 microseconds TAW, set this byte to 20. After every transmitted frame, an Access Time Period is allocated, which is 64 times the TAW time period.

Byte 8 - The value of this byte times TAW divided by 2 equals the amount of time (microseconds.) reserved after each frame for a response frame to be transmitted.

Byte 9 - The value of this byte times 2 equals the delay in microseconds after the start of a transmit frame before the first byte (destination) is transmitted.

Byte 10 - The value of this byte times 2 equals the delay in microseconds between the control field and data field of a frame.

Byte 11 - The value of this byte times 6 equals the time allowed in microseconds for a response frame to be received.

Byte 12 - The value of this byte times 6 equals the time allowed in microseconds for the next byte of a frame to be received.

Byte 13 - The value of this byte times 16.7 equals the number of seconds allowed for any command in progress to finish before the 8031 indicates error hex 3C to the Cluster Adapter BIOS code.

Byte 14 - The value of this byte times 67 milliseconds equals the amount of time allowed waiting to access the cluster before error hex 36 is returned.

Receive Frame (from FIFO queue) = Hex 02

Function: This command is used to retrieve a data frame sent from another station (using Transmit Frame) from the First-In-First-Out (FIFO) queue.

The FIFO queue can contain four full size frames and 10 small frames.

Notes:

1. The field's destination, command, and cluster status in the LCB are modified.

2. If the adapter is in monitor mode, the first byte returned is the Transmit Window Token. The second byte is the first data byte of the information field of the received frame.

Return code	Definition
hex 00	Successful completion
hex 32	Duplicate station address in the cluster
hex 37	Information field too long
hex 38	No information field present
hex 39	Command in progress
hex 3A	Initialization required
hex 3B	No receive frame exists
hex 3C	Error detected with 8031

Transmit Frame = Hex 03

Function: This command is used to transmit a data frame to another station where it can be retrieved by using the Receive Frame command.

Note: See also "Special Transmit Mode Command Bits" in this chapter.

Return code	Definition
hex 00	Successful completion
hex 31	Cluster always busy
hex 32	Duplicate station address in the cluster
hex 33	No response from destination
hex 34	Exceed allowed number of rejected frames
hex 36	Cluster access time-out
hex 37	Information field too long (frame is not sent)
hex 38	No information field present (frame is not sent)
hex 39	Command in progress
hex 3A	Initialization required
hex 3C	Error detected with 8031

Display Cluster Status = Hex 05

Function: This command is used to determine and then display the cluster status. The On/Off status of 64 stations is displayed. Stations that have the Power switch set to On are displayed in reverse video. Your station is displayed in reverse video and blinking. If another station in the cluster has the same address as your station, a long beep sounds. Only those stations that are initialized can be displayed.

Notes:

1. The screen should be cleared before issuing this command.

2. Type of status (destination field):

1. Hex 00 = report stations that are On

2. Hex FF = report stations that are initialized.

Return code	Definition
hex 00	Successful completion
hex 31	Cluster always busy
hex 36	Cluster access time-out
hex 39	Command in progress
hex 3C	Error detected with 8031

Programming Considerations *(continued)*

This page explains the cluster status that may appear on your screen.

NN is any station address from 0 to 63.

****** The station you are using is indicated on the screen in blinking reverse video, and the box is marked by two asterisks.

XX Stations that have their Power switches set to On are displayed in reverse video, and their boxes are marked by two Xs.

X* Another station has the same address as your station; a long beep sounds every 3 seconds, the box is displayed in blinking reverse video, and is marked by an X and an asterisk.

NN A station address not in the cluster is indicated by a box displayed in normal video and not marked with Xs or asterisks.

Link Control Block (LCB)		
Field	**Value at entry**	**Value at exit**
Destination	Type of status	Unchanged
Source	Don't care	Unchanged
Command	= 06 (hex)	Unchanged
Buffer 1 length	Number of stations to check	Unchanged
Buffer 1 address	Points to calling program's buffer 1	Unchanged
Buffer 2 length	Don't care	Unchanged
Buffer 2 address	Don't care	Unchanged
Return code	Don't care	Set to return code
Cluster status	Don't care	Extended return code on error
Select adapter	= 0 for adapter 1 = 1 for adapter 2 = 2 for adapter 3 = 3 for adapter 4	Unchanged

Cluster status = hex 06

Transmit Broadcast Frame = Hex 08

Function: This command is used to transmit a data frame to another station where it can be retrieved by using the Receive Frame command. No acknowledgment to the frame is sent by the receiving stations.

Notes:

1. Transmit Frame and Transmit Virtual Frames are converted to Broadcast Frames if the destination station number is greater than 127.

2. See also "Special Transmit Mode Command Bits" in this chapter.

Return code	Definition
hex 00	Successful completion
hex 31	Cluster always busy
hex 32	Duplicate station address in cluster
hex 36	Cluster access time-out
hex 37	Information field too long (frame is not sent)
hex 38	No information field present (frame is not sent)
hex 39	Command in progress
hex 3A	Initialization required
hex 3C	Error detected with 8031

Transmit Virtual Frame = Hex 09

Function: This command is used to transmit a data frame containing sector information from the disk server station. The information can be retrieved only by using the Receive Virtual Frame command.

Note: See "Special Transmit Mode Command Bits" in this chapter.

Return code	Definition
hex 00	Successful completion
hex 31	Cluster always busy
hex 32	Duplicate station address in cluster
hex 33	No response from destination
hex 34	Frame rejected at destination
hex 36	Cluster access time-out
hex 37	Information field too long (frame is not sent)
hex 38	No information field present (frame is not sent)
hex 39	Command in progress
hex 3A	Initialization required
hex 3C	Error detected with 8031

Stop DLCP = Hex 0A

Function: This command is used to temporarily inhibit the DLCP from receiving or transmitting frames. Issue a Start DLCP command to leave the stopped state.

Return code	Definition
hex 00	Successful completion
hex 39	Command in progress
hex 3A	Initialization required
hex 3C	Error detected with 8031

Link Control Block (LCB)		
Field	**Value at entry**	**Value at exit**
Destination	Don't care	Unchanged
Source	Don't care	Unchanged
Command	= 0A (hex)	Unchanged
Buffer 1 length	Don't care	Unchanged
Buffer 1 address	Don't care	Unchanged
Buffer 2 length	Don't care	Unchanged
Buffer 2 address	Don't care	Unchanged
Return code	Don't care	Set to return code
Cluster status	Don't care	Unchanged
Select adapter	= 0 for adapter 1 = 1 for adapter 2 = 2 for adapter 3 = 3 for adapter 4	Unchanged

Stop DLCP = hex 0A

Set Multicast Address = Hex 0C

Function: This command is used to set the desired multicast address. The multicast address is a variation of the broadcast address (hex FF). More than one station may be assigned the same multicast address. A default value of hex FF is set when a cluster Initialization command is issued to the DLCP. A frame sent, using the Transmit Broadcast Frame command (8), to the group multicast address is received by all stations that share the multicast address.

Return code	Definition
hex 00	Successful completion
hex 39	Command in progress
hex 3C	Error detected with 8031

Link Control Block (LCB)		
Field	**Value at entry**	**Value at exit**
Destination	Desired multicast address	Unchanged
Source	Don't care	Unchanged
Command	= 0C (hex)	Unchanged
Buffer 1 length	Don't care	Unchanged
Buffer 1 address	Don't care	Unchanged
Buffer 2 length	Don't care	Unchanged
Buffer 2 address	Don't care	Unchanged
Return code	Don't care	Set to return code
Cluster status	Don't care	Unchanged
Select adapter	= 0 for adapter 1 = 1 for adapter 2 = 2 for adapter 3 = 3 for adapter 4	Unchanged

Set multicast address = hex 0C

Read IPL Switch = Hex 0E

Function: This command is used to read the state of the Remote IPL switch on the requesting station.

Return code	Definition
hex 00	Successful completion
hex 39	Command in progress
hex 3C	Error detected with 8031

Link Control Block (LCB)		
Field	**Value at entry**	**Value at exit**
Destination	Don't care	Unchanged
Source	Don't care	This station's address
Command	= 0E (hex)	Unchanged
Buffer 1 length	Don't care	Unchanged
Buffer 1 address	Don't care	Unchanged
Buffer 2 length	Don't care	Unchanged
Buffer 2 address	Don't care	Unchanged
Return code	Don't care	Set to return code
Cluster status	Don't care	IPL switch (00 = no IPL FF = IPL)
Select adapter	= 0 for adapter 1 = 1 for adapter 2 = 2 for adapter 3 = 3 for adapter 4	Unchanged

Read IPL switch = hex 0E

Dump Statistics = Hex 10

Function: This command is used to transfer the current communication statistics block from the adapter.

Link Control Block (LCB)		
Field	**Value at entry**	**Value at exit**
Destination	Don't care	Unchanged
Source	Don't care	Unchanged
Command	= 10 (hex)	Unchanged
Buffer 1 length	12 bytes	Unchanged
Buffer 1 address	Points to calling program's buffer 1	Unchanged
Buffer 2 length	Don't care	Unchanged
Buffer 2 address	Don't care	Unchanged
Return code	Don't care	Set to return code
Cluster status	Don't care	Unchanged
Select adapter	= 0 for adapter 1 = 1 for adapter 2 = 2 for adapter 3 = 3 for adapter 4	Unchanged

Dump statistics = hex 10

Diagnostic Function 1 = Hex 11

Function: This command is used to run an internal diagnostic test.

(Reserved for diagnostic use only.)

Bit 1 Test adapter processor-to-processor interface
Bit 2 Reserved
Bit 3 Test driver and receiver logic (terminating plug required for diagnostic use)
Bit 4 Test interrupt logic (set transmit interrupt status bit)
Bit 5 Test interrupt logic (set receive interrupt status bit)
Bit 6 Clear transmit and receive interrupt status bits (no interrupt)
Bit 7 Set transmit and receive interrupt status bits (no interrupt).

Return code	Definition
hex 00	Successful completion
hex 39	Command in progress
hex 3C	Error detected with 8031
hex 3D	Error detected by 8031 diagnostic test (reason for error in Cluster Status field)

Link Control Block (LCB)		
Field	**Value at entry**	**Value at exit**
Destination	Test number**	Unchanged
Source	Don't care	Unchanged
Command	= 11 (hex)	Unchanged
Buffer 1 length	Don't care	Unchanged
Buffer 1 address	Don't care	Unchanged
Buffer 2 length	Don't care	Unchanged
Buffer 2 address	Don't care	Unchanged
Return code	Don't care	Set to return code
Cluster status	Don't care	Extended return code
Select adapter	= 0 for adapter 1 = 1 for adapter 2 = 2 for adapter 3 = 3 for adapter 4	Unchanged

Diagnostic function 1 = hex 11

Note: ** Test number (Destination field)

Diagnostic Function 3 = Hex 13

Function: This command is used to transfer data from the adapter's RAM to a buffer in system memory. The data is transferred starting at the address specified by the buffer 2 address (offset) in 8031 memory to buffer 1 in the main system's memory.

(Reserved for diagnostic use only.)

Return code	Definition
hex 00	Successful completion
hex 39	Command in progress
hex 3C	Error detected with 8031

Link Control Block (LCB)		
Field	**Value at entry**	**Value at exit**
Destination	Don't care	Unchanged
Source	Don't care	Unchanged
Command	= 13 (hex)	Unchanged
Buffer 1 length	Length of calling program's buffer 1	Unchanged
Buffer 1 address	Points to buffer 1	Unchanged
Buffer 2 length	Don't care	Unchanged
Buffer 2 address	Set offset to address in 8031 RAM space from which to get data	Unchanged
Return code	Don't care	Set to return code
Cluster status	Don't care	Unchanged
Select adapter	= 0 for adapter 1 = 1 for adapter 2 = 2 for adapter 3 = 3 for adapter 4	Unchanged

Diagnostic function 3 = hex 13

Diagnostic Function 5 = Hex 15

Function: This command is used to transfer data from the 8031's internal RAM to a buffer in system memory. The data is transferred starting at the address specified by buffer 2 address (offset) in 8031 memory to buffer 1 in the main system's memory.

(Reserved for diagnostic use only.)

Return code	Definition
hex 00	Successful completion
hex 39	Command in progress
hex 3C	Error detected with 8031

Link Control Block (LCB)		
Field	**Value at entry**	**Value at exit**
Destination	Don't care	Unchanged
Source	Don't care	Unchanged
Command	= 15 (hex)	Unchanged
Buffer 1 length	Length of calling program's buffer 1	Unchanged
Buffer 1 address	Points to buffer 1	Unchanged
Buffer 2 length	Don't care	Unchanged
Buffer 2 address	Set offset to address in 8031 RAM from which to get data	Unchanged
Return code	Don't care	Set to return code
Cluster status	Don't care	Unchanged
Select adapter	= 0 for adapter 1 = 1 for adapter 2 = 2 for adapter 3 = 3 for adapter 4	Unchanged

Diagnostic function 5 = hex 15

Diagnostic Function 7 = Hex 17

Function: This command is used to transmit any type of frame to another station. For example, a control frame may be sent to another station.

(Reserved for diagnostic use only.)

Return code	Definition
hex 00	Successful completion
hex 31	Cluster always busy
hex 32	Duplicate station address in cluster
hex 33	No response from destination
hex 34	Exceeded allowed rejected frames
hex 36	Cluster access time-out
hex 37	Information field too long
hex 39	Command in progress
hex 3A	Initialization required
hex 3C	Error detected with 8031

Link Control Block (LCB)		
Field	**Value at entry**	**Value at exit**
Destination	Destination	Unchanged
Source	Frame type	Unchanged
Command	= 17 (hex)	Unchanged
Buffer 1 length	Length of calling program's buffer 1	Unchanged
Buffer 1 address	Points to calling program's buffer 1	Unchanged
Buffer 2 length	Length of calling program's buffer 2	Unchanged
Buffer 2 address	Points to calling program's buffer 2	Unchanged
Return code	Don't care	Set to return code
Cluster/status	Don't care	Unchanged
Select adapter	= 0 for adapter 1 = 1 for adapter 2 = 2 for adapter 3 = 3 for adapter 4	Unchanged

Diagnostic function 7 = hex 17

Interface

System Processor I/O Interface

Four Cluster Adapters can be installed at each station. The Cluster Adapter number is selected by switch positions 1 through 4 of switch block 2. These positions correspond to I/O address bits 10, 11, 12, and 13. An adapter is selected when a select switch is On, and the adapter receives a high level (1) on the corresponding I/O address bit.

Note: High level is 1 and low level is 0.

If multiple Cluster Adapters are installed at a station, each adapter can have only one address select switch set to On. A station cannot have two Cluster Adapters with the same address.

Notes:

1. When more than one address select switch is On, the Cluster Adapter decodes and responds to all I/O addresses selected.
2. Cluster Adapter 1 is the only adapter that decodes and responds to all memory addresses; therefore, if more than one Cluster Adapter is set as number 1 (C1), undesirable results occur.
3. If a Cluster Adapter does not have a select switch set to On, it does not respond.

The following shows the station-address switch settings on switch block 1.

Station	Switch block 1 switch settings					
	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6
0	Off	Off	Off	Off	Off	Off
1	On	Off	Off	Off	Off	Off
2	Off	On	Off	Off	Off	Off
3	On	On	Off	Off	Off	Off
4	Off	Off	On	Off	Off	Off
5	On	Off	On	Off	Off	Off
6	Off	On	On	Off	Off	Off
7	On	On	On	Off	Off	Off
8	Off	Off	Off	On	Off	Off
9	On	Off	Off	On	Off	Off
10	Off	On	Off	On	Off	Off
11	On	On	Off	On	Off	Off
12	Off	Off	On	On	Off	Off
13	On	Off	On	On	Off	Off
14	Off	On	On	On	Off	Off

Notes:

1. Bit switches 7 and 8 are not applicable to the station address.
2. "On" represents the closed/on position.
3. "Off" represents the open/off position.

Station address switch settings

Station	Switch block 1 switch settings					
	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6
48	Off	Off	Off	Off	On	On
49	On	Off	Off	Off	On	On
50	Off	On	Off	Off	On	On
51	On	On	Off	Off	On	On
52	Off	Off	On	Off	On	On
53	On	Off	On	Off	On	On
54	Off	On	On	Off	On	On
55	On	On	On	Off	On	On
56	Off	Off	Off	On	On	On
57	On	Off	Off	On	On	On
58	Off	On	Off	On	On	On
59	On	On	Off	On	On	On
60	Off	Off	On	On	On	On
61	On	Off	On	On	On	On
62	Off	On	On	On	On	On
63	On	On	On	On	On	On

Station address switch settings

Interface *(continued)*

System Processor Memory Interface

The memory addresses assigned to the Cluster Adapter are hex D0000 through hex D7FFF. These addresses are fully decoded only on adapter 1, and are selected by setting the C1 select switch (SW2-1) to On. Each station must have one Cluster Adapter selected as number 1.

System Processor Interrupt Interface

The Cluster Adapter provides an interrupt interface to the system processor with Interrupt Request 3 (IRQ3) or Interrupt Request 7 (IRQ7). The desired interrupt is selected using the interrupt select jumper on the Cluster Adapter. The selection of the interrupt is dependent on the programming requirements.

The following is a sequence of the interrupt process for adapter 1:

1. The system processor enables interrupts by writing to the adapter interrupt enable register at address hex 0792.

2. Upon receipt of an interrupt condition, the 8031 sends a negative active (0) pulse of 10 microseconds on the port C bit 0 (PC0) line of the 8255 which is connected to IRQ3 or IRQ7. The low-to-high transition of this line prevents this adapter and other Cluster Adapters in the system from generating further interrupt requests. The 8031 processor also sets either Port C1 (PC1) or Port C2 (PC2) of the 8255 to indicate the source of the interrupt. PC1 corresponds to a transmit interrupt, and PC2 corresponds to a receive interrupt. If both PC1 and PC2 are set, the source of the interrupt is the completion of a Cluster Status command.

3. The system processor reads I/O addresses hex 0792, 0B92, 1392, and 2392 on each Cluster Adapter to determine the cause of the interrupt. After all pending requests are handled, the system processor re-enables interrupts on all desired adapters.

8255 Programmable Peripheral Interface (PPI)

The 8255 is used to provide an asynchronous interface between the system processor and the 8031 Microcomputer without the use of interrupts or direct memory access (DMA).

- Input Buffer Full (IBF)

  A high signal on the IBF (PC5) output indicates that data from the 8088 has been loaded into Port A. IBF provides input to the adapter status register and to the 8031.

- -Strobe Input (-STB)

  A low signal on the -STB (PC4) loads data from the 8088 into Port A.

The following is a summary of the 8255 port signals:

8255 port signals			
Bit	Port A mode 2	Port B mode 0	Port C mode 2
7	Data bit 7	Remote IPL	–OBF
6	Data bit 6	Reserved	–ACK
5	Data bit 5	Station address bit 5	+IBF
4	Data bit 4	Station address bit 4	–STB
3	Data bit 3	Station address bit 3	Reserved
2	Data bit 2	Station address bit 2	Receive frame interrup
1	Data bit 1	Station address bit 1	TX complete interrupt
0	Data bit 0	Station address bit 0	Interrupt request

Summary of 8255 port signals

Interface *(continued)*

Carrier Sense Circuitry

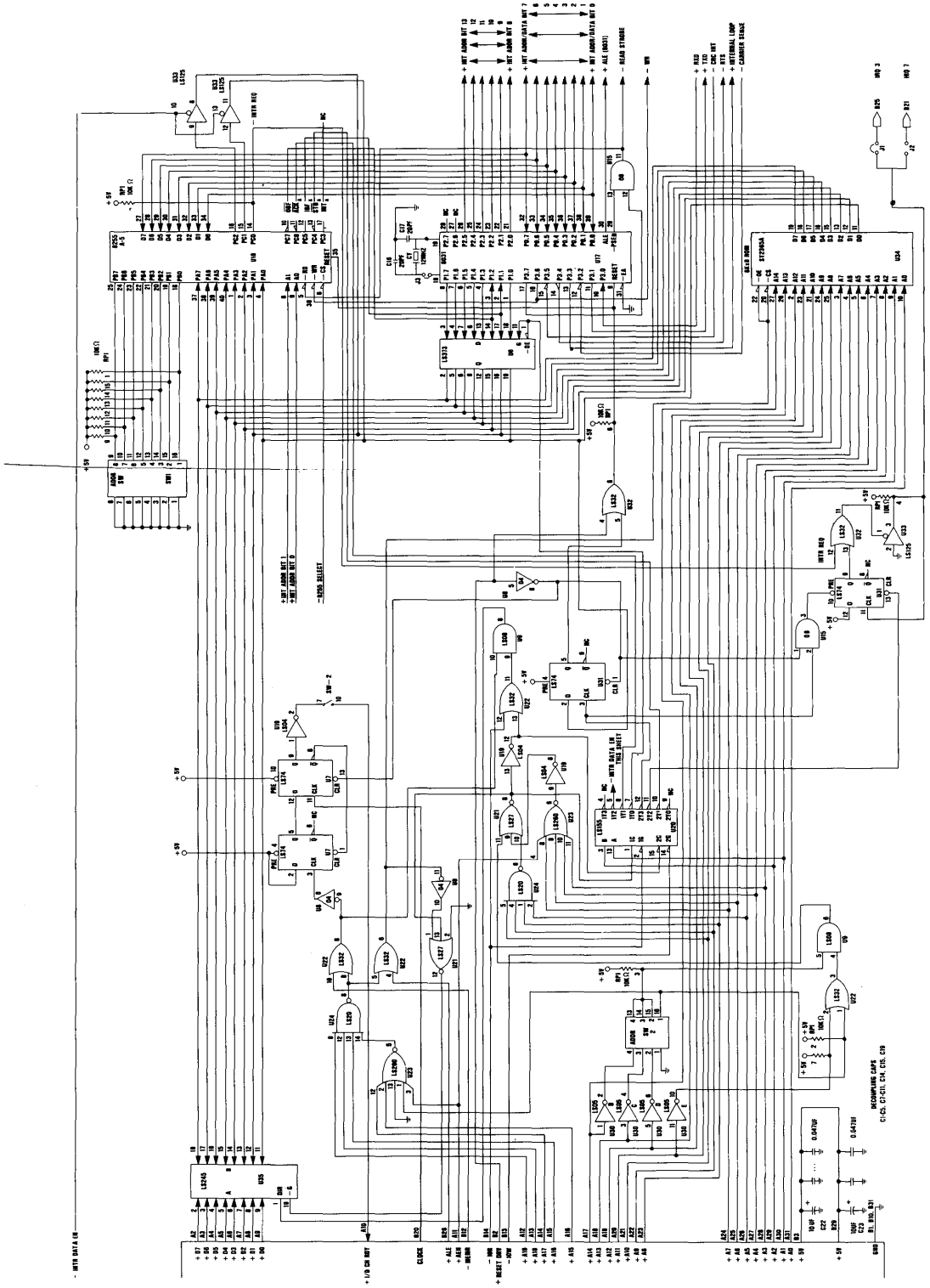
The carrier sense circuitry provides information about the state of the Cluster Adapter. This information is needed to implement the collision-avoidance protocol. The amplified signal received from the bus is passed through a comparator to detect the negative voltage state (less than approximately -150 millivolts). This negative portion of the signal is inverted into +NRXD and then ORed with the positive portion (greater than approximately +150 millivolts) of the +RXD signal. The result is then sent to the clear input of a 74LS161 counter. As long as this ORed signal (CLR) is active (0), the counter is held reset. When the signal goes inactive (1), the counter begins counting on the rising edges of the 8031 +ALE signal. On the fourth +ALE pulse, the counter is disabled and the -Carrier Sense signal goes inactive (1). The time delay between the bus going inactive and -Carrier Sense going inactive is 1.5 microseconds.

Internal Loopback Mode

The Cluster Adapter provides logic to allow the 8031 to receive the data it is transmitting without interference from the bus by wrapping the transmitter to the receiver on the Cluster Adapter.

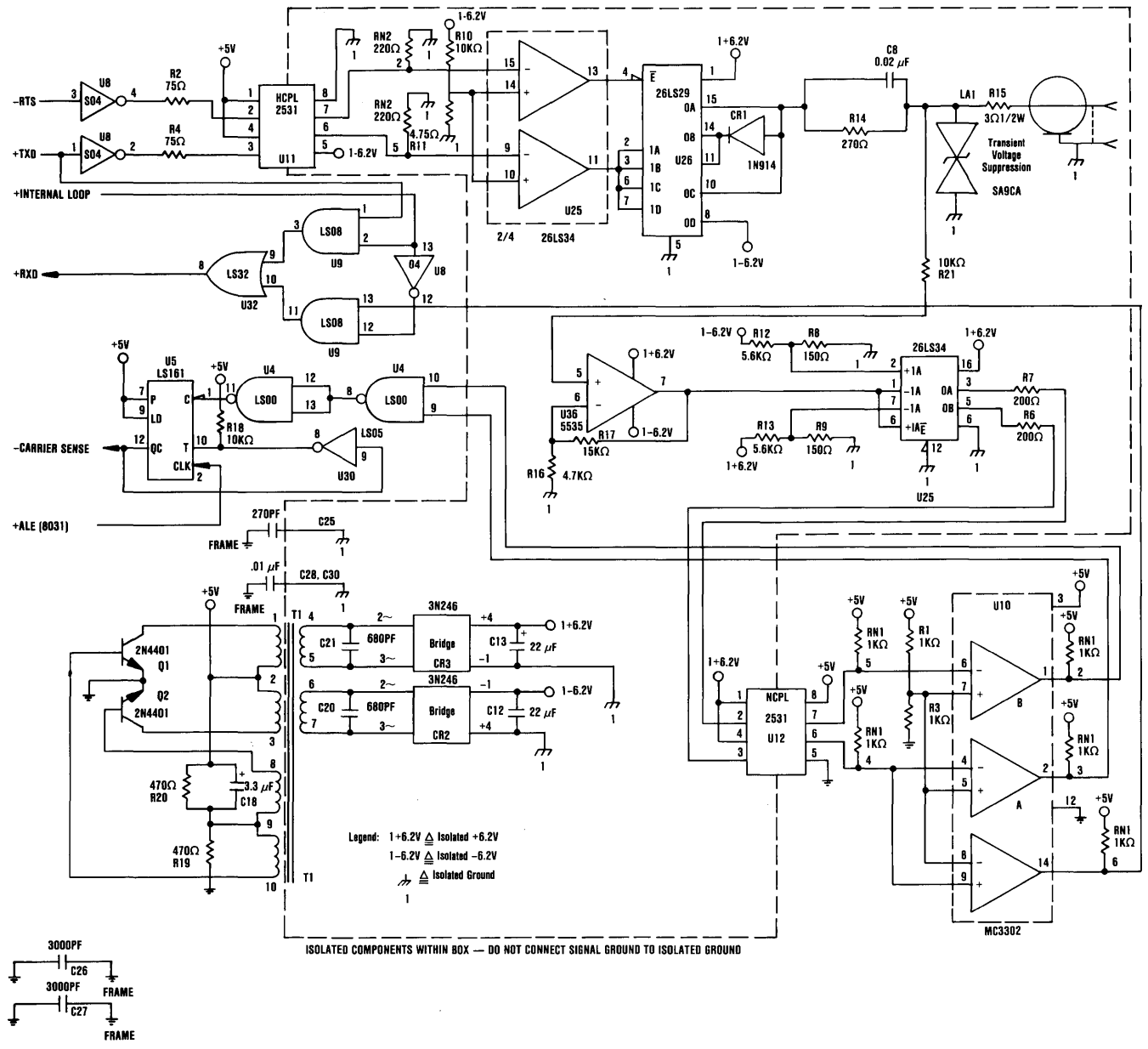
The adapter is placed into internal loopback mode when the 8031 microprocessor code sets the +Internal Loop signal active (1). This mode returns any data transmitted on +TXD to +RXD. Notice that -RTS may or may not be active. If -RTS is active, the data not only returns to +RXD, but also is transmitted to the bus.

Logic Diagrams



Cluster adapter (Part 1 of 3)

Logic Diagrams *(continued)*



Cluster adapter (Part 3 of 3)

IBM Game Control Adapter

Contents

IBM Game Control Adapter

Description

The IBM Game Control Adapter allows up to four paddles or two joysticks to be attached to the system. This adapter fits into one of the system board's or expansion board's expansion slots. The game control interface cable attaches to the rear of the adapter. In addition, four inputs for switches are provided. Paddle and joystick positions are determined by changing resistive values sent to the adapter. The adapter, when used with system software, converts the present resistive value to a relative paddle or joystick position. On receipt of an output signal, four timing circuits are started. By determining the time required for the circuit to timeout (a function of the resistance), the paddle position can be determined. This adapter could be used as a general purpose I/O card with four analog (resistive) inputs plus four digital input points.

Programming Considerations

Address Decode

The select on the Game Control Adapter is generate by two 74LS138s as an address decoder. AEN must be inactive while the address is hex 201 in order to generate the select. The select allows a write to fire the one-shots, or a read to give the values of the trigger buttons and one-shot outputs.

Data Bus Buffer/Driver

The data bus is buffered by a 74LS244 buffer/driver. For an In from address hex 201, the Game Control Adapter will drive the data bus; at all other times, the buffer is left in the high impedance state.

Trigger Buttons

The trigger button inputs are read by an In from address hex 201. A trigger button is on each joystick or paddle. These values are seen on data bits 7 through 4. These buttons default to an open state and are read as 1. When a button is pressed, it is read as 0. Software should be aware that these buttons are not debounced in hardware.

Joystick Positions

The joystick position is indicated by a potentiometer for each coordinate. Each potentiometer has a range of 0 to 100 kilohms that varies the time constant for each of the four one-shots. As this time constant is set at different values, the output of the one-shot will be of varying durations.

All four one-shots are fired at once by an Out to address hex 201. All four one-shot outputs will go true after the fire pulse and will remain high for varying times depending on where each potentiometer is set.

These four one-shot outputs are read by an In from address hex 201 and are seen on data bits 3 through 0.

Interface

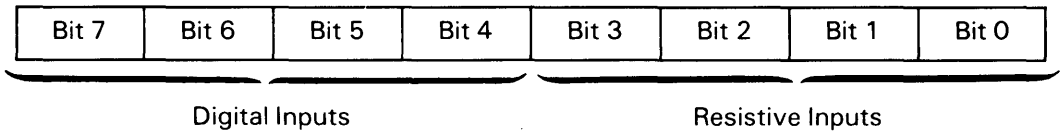
The Game Control Adapter has eight input lines; four digital inputs and four resistive inputs. The inputs are read with one In from address hex 201.

The four digital inputs each have a 1-kilohm pullup resistor to ç5 Vdc. With no drives on these inputs, a 1 is read. For a 0 reading, the inputs must be pulled to ground.

The four resistive pullups, measured to + 5 Vdc, will be converted to a digital pulse with a duration proportional to the resistive load, according to the following equation:

Time = 24.2 μs + 0.011 (r) μs

The user must first begin the conversion by an Out to address hex 201. An In from address hex 201 will force the digital pulse to go high and remain high for the duration according to the resistance value. All four bits (bit 3–bit 0) function in the same manner; their digital pulse will all go high simultaneously and will reset independently according to the input resistance value.

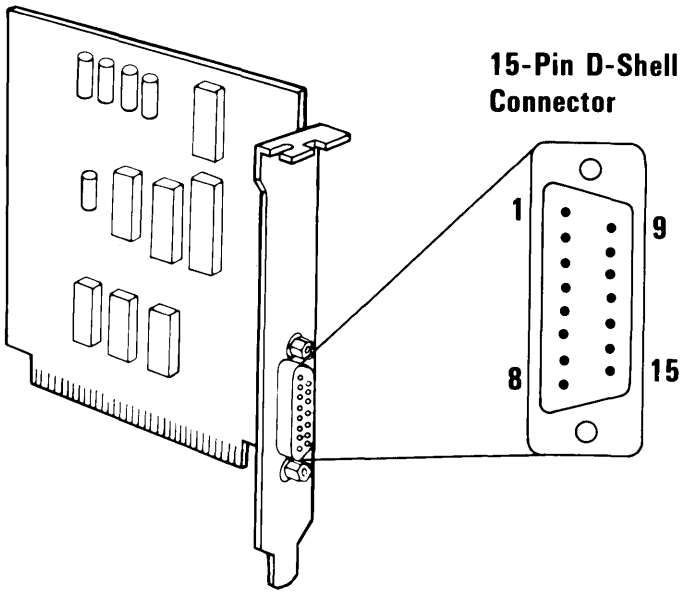


The typical input to the Game Control Adapter is a set of joysticks or game paddles.

The joysticks will typically be a set of two (A and B). These will have one or two buttons each with two variable resistances each, with a range of 0 to 100 kilohms. One variable resistance will indicate the X coordinate and the other variable resistance will indicate the Y coordinate. The joystick should be attached to give the following input data:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B-#2 Button	B-#1 Button	A-#2 Button	A-#1 Button	B-Y Coordinate	B-X Coordinate	A-Y Coordinate	A-X Coordinate

Specifications



At Standard TTL Levels

	Voltage	Adapter Pin No.	
	+ 5 Vdc	1	
	Button 4	2	
	Position 0	3	
	Ground	4	
	Ground	5	
	Position 1	6	
	Button 5	7	
External Devices	+ 5 Vdc	8	Game Control Adapter
	+ 5 Vdc	9	
	Button 6	10	
	Position 2	11	
	Ground	12	
	Position 3	13	
	Button 7	14	
	+ 5 Vdc	15	

Connector Specifications

IBM Personal Computer AT Communications Cable

Contents

IBM Personal Computer AT Communications Cable

Description

The IBM Personal Computer AT Communications Cable cable is for connection of an IBM communications adapter with a 9-pin D-shell connector toa modem or other RS-232C DCE (data communications equipment). It is fully shielded and provides a high quality, low noise channel for interface between the communications adapter and DCE.

IBM Communications Adapter Cable

Contents

IBM Communications Adapter Cable

Description

The IBM Communications Adapter Cable is a 3.05 m (10-ft) cable designed to connect an IBM communications adapter to a modem or other RS232-C data communications equipment (DCE). It is fully shielded and provides a high quality, low noise channel for interface between the communications adapter and DCE.

The connector ends are 25-pin D-shell connectors. All pin connections conform with the EIA RS232-C standard. In addition, connection is provided on pins 11, 18, and 25. These pins are designated as 'select standby,' 'test,' and 'test indicate,' respectively, on some modems. 'Select standby' is used to support the switched network backup facility, if applicable. 'Test' and 'test indicate' support a modem wrap function on modems designed for business-machine controlled modem wraps.

Serial/Parallel Adapter

Contents

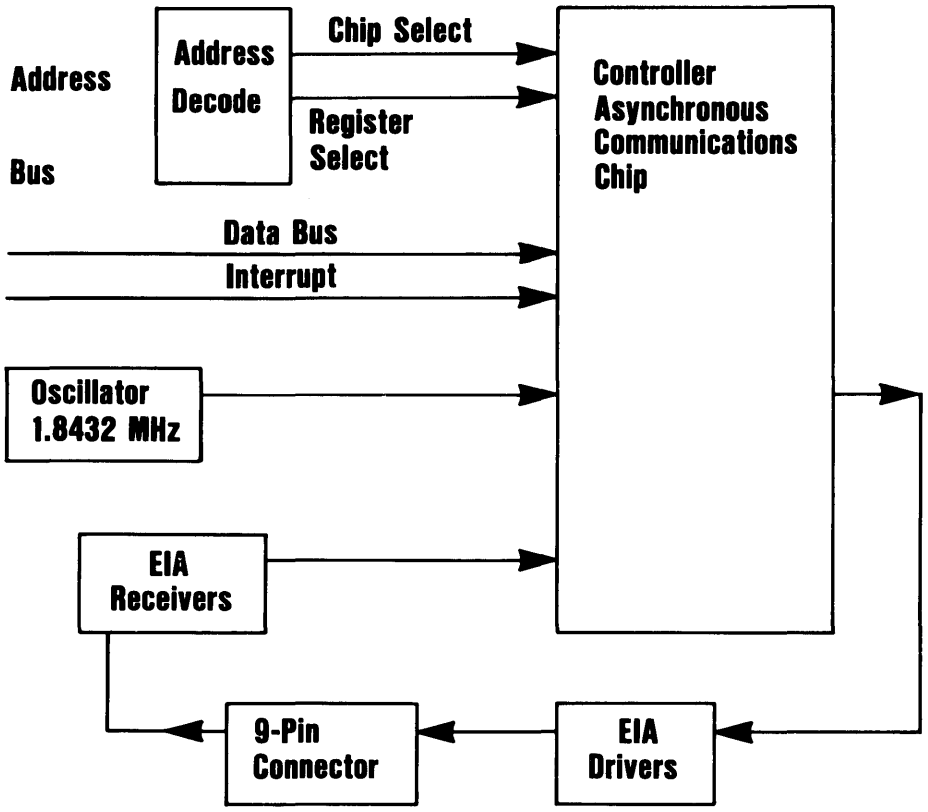
Serial/Parallel Adapter

Description

The Serial/Parallel Adapter provides a parallel port and a serial port. It plugs into a system-board expansion slot. All system-control signals and voltage requirements are provided through a 2- by 31-position card edge connector.

Serial Portion of the Adapter *(continued)*

The following figure is a block diagram of the serial portion of the adapter.



Serial Portion Block Diagram

The serial portion of the adapter has a controller that provides the following functions:

- Adds or deletes standard, asynchronous-communications bits to or from a serial data stream.
- Provides full, double buffering, which eliminates the need for precise synchronization.
- Provides a programmable baud-rate generator.
- Provides modem controls (CTS, RTS, DSR, DTR, RI, and CD).

Controller Specifications

The following describes the function of controller input/output signals.

Input Signals

-Clear to Send

(-CTS), Pin 36 — The '-CTS' signal is a modem-control function input, the condition of which can be tested by the processor by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates if the '-CTS' input has changed state since the previous reading.

> **Note:** Whenever the CTS bit of the modem status register changes state, an interrupt is generated if the modem-status interrupt is enabled.

-Data Set Ready

(-DSR), Pin 37 — When low, indicates the modem or data set is ready to establish the communications link and transfer data with the controller. The '-DSR' signal is a modem-control function input, the condition of which can be tested by the processor reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates if the '-DSR' input has changed since the previous reading.

> **Note:** Whenever the DSR bit of the modem status register changes state, an interrupt is generated if the modem-status interrupt is enabled.

-Data Carrier Detect

(-DCD), Pin 38 — When low, indicates the modem or data set detected a data carrier. The '-DCD' signal is a modem-control function input, the condition of which can be tested by the processor reading bit 7 (DCD) of the modem status register. Bit 3 (DCD) of the modem status register indicates if the '-DCD' input has changed state since the previous reading.

> **Note:** Whenever the DCD bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

-Ring Indicator

(-RI), Pin 39 — When low, indicates the modem or data set detected a telephone ringing signal. The '-RI' signal is a modem-control function input, the condition of which can be tested by the processor reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates if the '-RI' input has changed from an active to an inactive state since the previous reading.

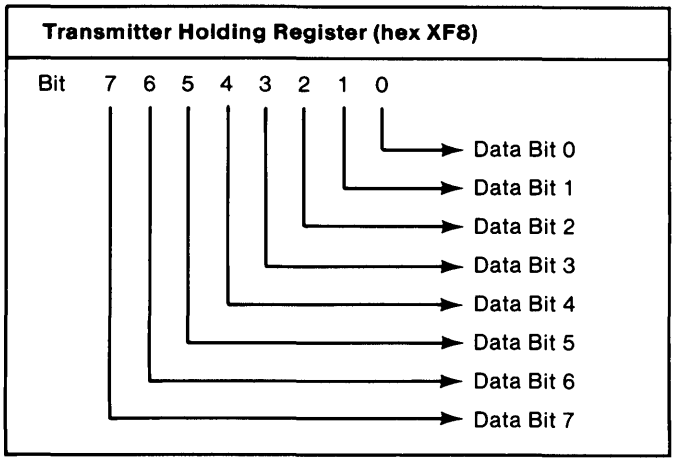
> **Note:** Whenever the RI bit of the modem status register changes from an inactive to an active state, an interrupt is generated if the modem-status interrupt is enabled.

VCC Pin 40 — + 5 Vdc supply

VSS Pin 20 — Ground (0 Vdc) reference

Transmitter Holding Register (Hex XF8)

The transmitter holding register (THR) contains the character to be sent.

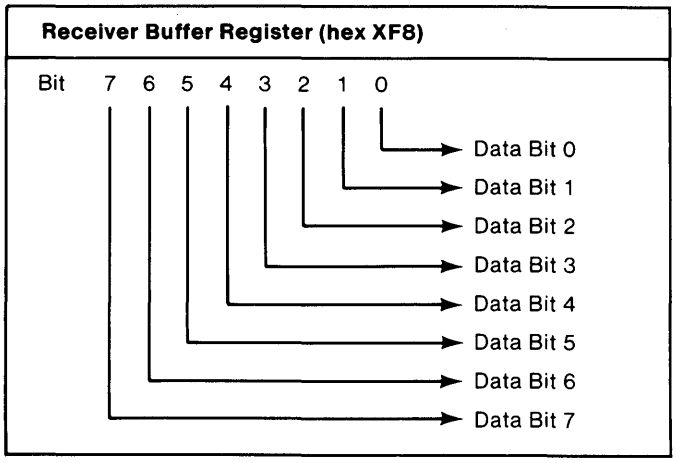


Transmitter Holding Register

Bit 0 is the least-significant bit and the first bit sent serially.

Receiver Buffer Register (Hex XF8)

The receiver buffer register (RBR) contains the received character.

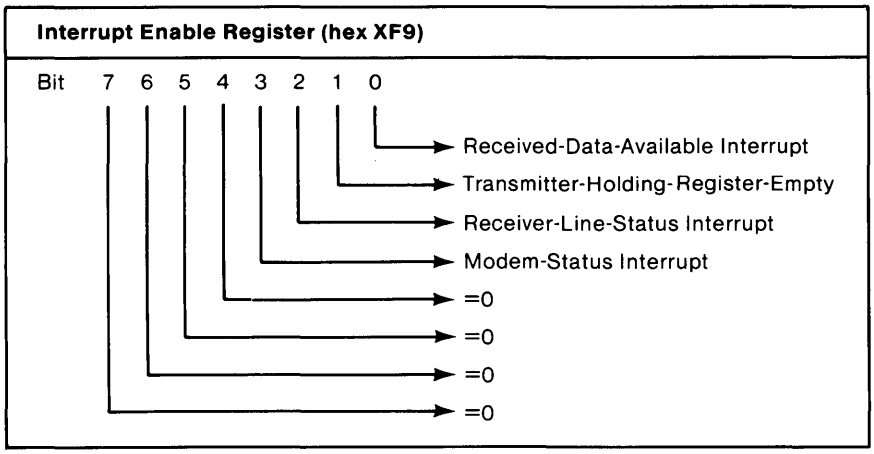


Receiver Buffer Register

Bit 0 is the least-significant bit and the first bit received serially.

Interrupt Enable Register (Hex XF9)

This 8-bit register allows the four types of controller interrupts to separately activate the 'chip-interrupt' (INTRPT) output signal. The interrupt system can be totally disabled by resetting bits 0 through 3 of the interrupt enable register (IER). Similarly, by setting the appropriate bits of this register to logical 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the 'IER' and the active 'INTRPT' output from the chip. All other system functions operate normally, including the setting of the line-status and modem-status registers.



Interrupt Enable Register

Bit 0 When set to logical 1, enables the received-data-available interrupt.

Bit 1 When set to logical 1, enables the transmitter-holding-register-empty interrupt.

Bit 2 When set to logical 1, enables the receiver-line-status interrupt.

Bit 3 When set to logical 1, enables the modem-status interrupt.

Bits 4–7 These four bits are always logical 0.

Bits 1–2 These two bits identify the pending interrupt that has the highest priority interrupt pending, as shown in the following figure.

Bits 3–7 These five bits are always logical 0.

Interrupt ID Register			Interrupt Set And Reset Functions			
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	-	None	None	-
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR (if source of interrupt) or writing into the THR
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

Interrupt Priority

Bit 4 This bit is the even-parity-select bit. When bit 3 is a logical 1 and bit 4 is a logical 0, an odd number of logical 1's is sent or checked in the data word bits and parity bit. When both bit 3 and bit 4 are a logical 1, an even number of bits is sent or checked.

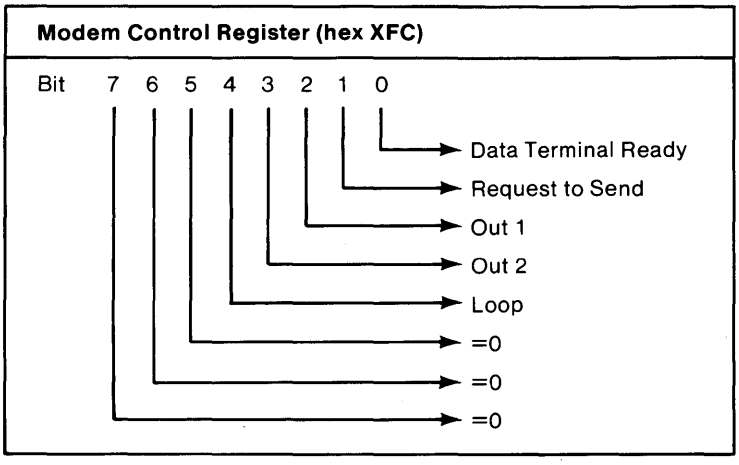
Bit 5 This bit is the stuck-parity bit. When bit 3 is a logical 1 and bit 5 is a logical 1, the parity bit is sent and then detected by the receiver as a logical 0, if bit 4 is a logical 1, or as a logical 1 if bit 4 is a logical 0.

Bit 6 This bit is the set-break control bit. When bit 6 is set to a logical 1, the serial output (SOUT) is forced to the spacing (logical 0) state and remains there regardless of other transmitter activity. The set-break is disabled by setting bit 6 to logical 0. This feature enables the microprocessor to select a specific terminal in a computer communications system.

Bit 7 This bit is the divisor-latch access bit (DLAB). It must be set high (logical 1) to gain access to the divisor latches of the baud-rate generator during a read or write operation. It must be set low (logical 0) to gain access to the receiver buffer, the transmitter holding register, or the interrupt enable register.

Modem Control Register (Hex XFC)

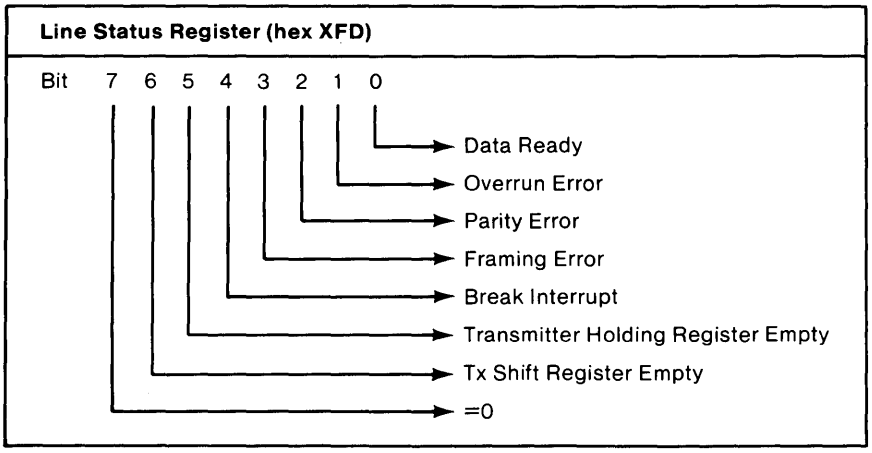
This 8-bit register controls the data exchange with the modem or data set (an external device acting as a modem).



Modem Control Register

Line Status Register (Hex XFD)

This 8-bit register provides the processor with status information about the data transfer.



Line Status Register

Bit 0 This bit is the receiver data ready (DR) indicator. It is set to logical 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. Bit 0 may be reset to logical 0 by the processor either reading the data in the receiver's buffer register or writing logical 0 in it.

Bit 1 This bit is the overrun error (OE) indicator. It indicates that data in the receiver's buffer register was not read by the processor before the next character was transferred into the register, thereby destroying the previous character. The OE indicator is reset whenever the processor reads the contents of the line status register.

Bit 2 This bit is the parity error (PE) indicator and indicates the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to logical 1 upon detection of a parity error, and is reset to logical 0 whenever the processor reads the contents of the line status register.

Bit 3 This bit is the framing error (FE) indicator. It indicates the received character did not have a valid stop bit. Bit 3 is set to logical 1 whenever the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level).

Bit 4 This bit is the break interrupt (BI) indicator. It is set to logical 1 whenever the received data input is held in the spacing state (logical 0) for longer than a fullword transmission time (that is, the total time of start bit + data bits + parity + stop bits).

Note: Bits 1 through 4 are error conditions that produce a receiver line-status interrupt whenever any of the corresponding conditions are detected.

Controller Specifications *(continued)*

Bit 4 This bit is the opposite of the '-clear-to-send' (-CTS) input. If bit 4 of the MCR loop is set to a logical 1, this bit is equivalent to RTS of the MCR.

Bit 5 This bit is the opposite of the '-data-set-ready' (-DSR) input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to DTR of the MCR.

Bit 6 This bit is the opposite of the '-ring-indicator' (-RI) input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to OUT 1 of the MCR.

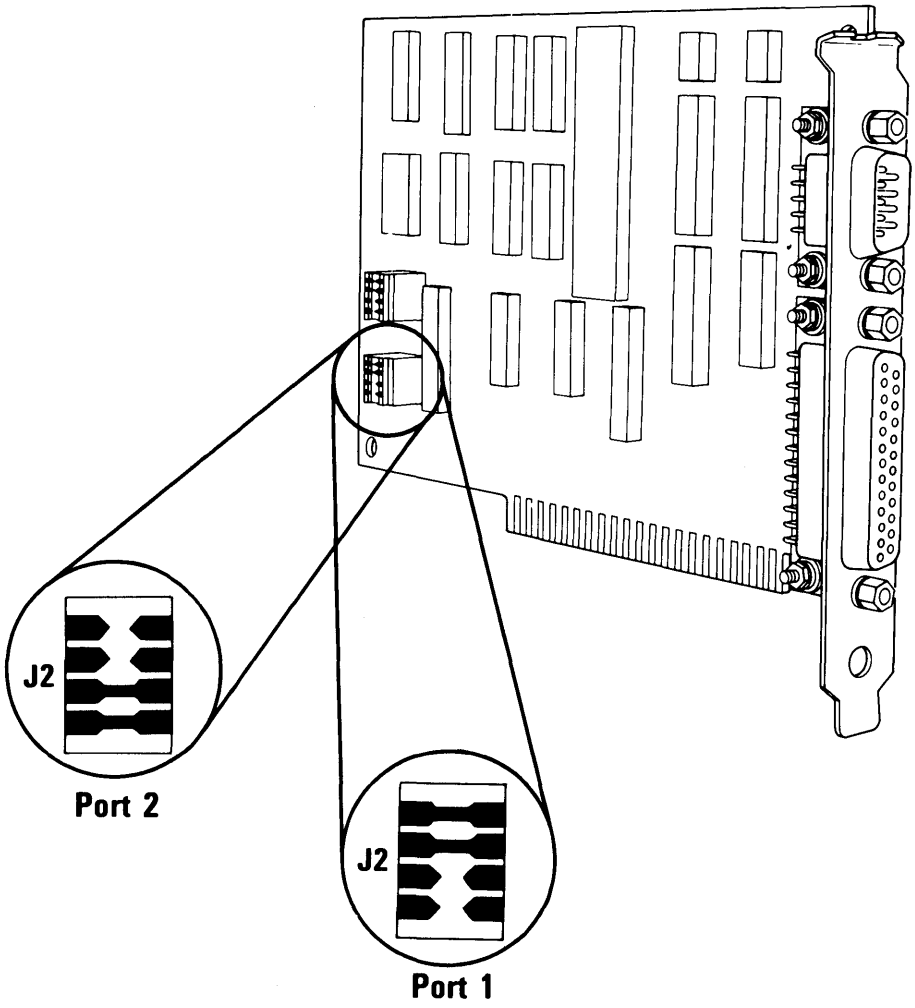
Bit 7 This bit is the opposite of the '-data-carrier-detect' (-DCD) input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to OUT 2 of the MCR.

Programmable Baud-Rate Generator

The controller has a programmable baud-rate generator that can divide the clock input (1.8432 MHz) by any divisor from 1 to 655,535 or 2^{16}-1. The output frequency of the baud-rate generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during setup to ensure desired operation of the baud-rate generator. When either of the divisor latches is loaded, a 16-bit baud counter is immediately loaded. This prevents long counts on the first load.

Parallel Portion of the Adapter

The parallel portion of the adapter makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL levels. The rear of the adapter has a 25-pin, D-shell connector. This port may be addressed as either parallel port 1 or 2. The port address is determined by the position of jumper J2, as shown in the following figure.



Printer Application*(continued)*

Bit 5 Not used

Bit 4 + IRQ Enable — A 1 in this position allows an interrupt to occur when '-ACK' changes from true to false.

Bit 3 + SLCT IN — A 1 in this bit position selects the printer.

Bit 2 -INIT — A 0 starts the printer (50-microsecond pulse, minimum).

Bit 1 + AUTO FD XT — A 1 causes the printer to line-feed after a line is printed.

Bit 0 + STROBE — A 0.5-microsecond minimum, high, active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microsecond before and after the strobe pulse.

Printer Status- Address X79, X7D

Printer status is stored at this address to be read by the microprocessor. The following are bit definitions for this byte.

Bit 7 -BUSY — When this signal is active, the printer is busy and cannot accept data. It may become active during data entry, while the printer is offline, during printing, when the print head is changing positions, or while in an error state.

Bit 6 -ACK — This bit represents the current state of the printer's '-ACK' signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before '-BUSY' stops.

Bit 5 + PE — A 1 means the printer has detected the end of paper.

Bit 4 + SLCT — A 1 means the printer is selected.

Bit 3 -Error — A 0 means the printer has encountered an error condition.

Bit 2 Unused.

Bit 1 Unused.

Bit 0 Unused.

Specifications

The following figures list characteristics of the output driver.

Sink current	24 mA	Max
Source Current	-2.6 mA	Max
High-Level Output Voltage	2.4 Vdc	Min
Low-Level Output Voltage	0.5 Vdc	Max

Parallel Data and Processor IRQ

Sink Current	16 mA	Max
Source Current	0.55 mA	Max
High Level Output Voltage	5 Vdc	Minus Pull-Up
Low Level Output Voltage	0.4 Vdc	Max

Parallel Control

Sink Current	24 mA	Max
Source Current	-15 mA	Max
High Level Output Voltage	2.0 Vdc	Min
Low Level Output Voltage	0.5 Vdc	Max

Parallel Processor Interface (Except IRQ)

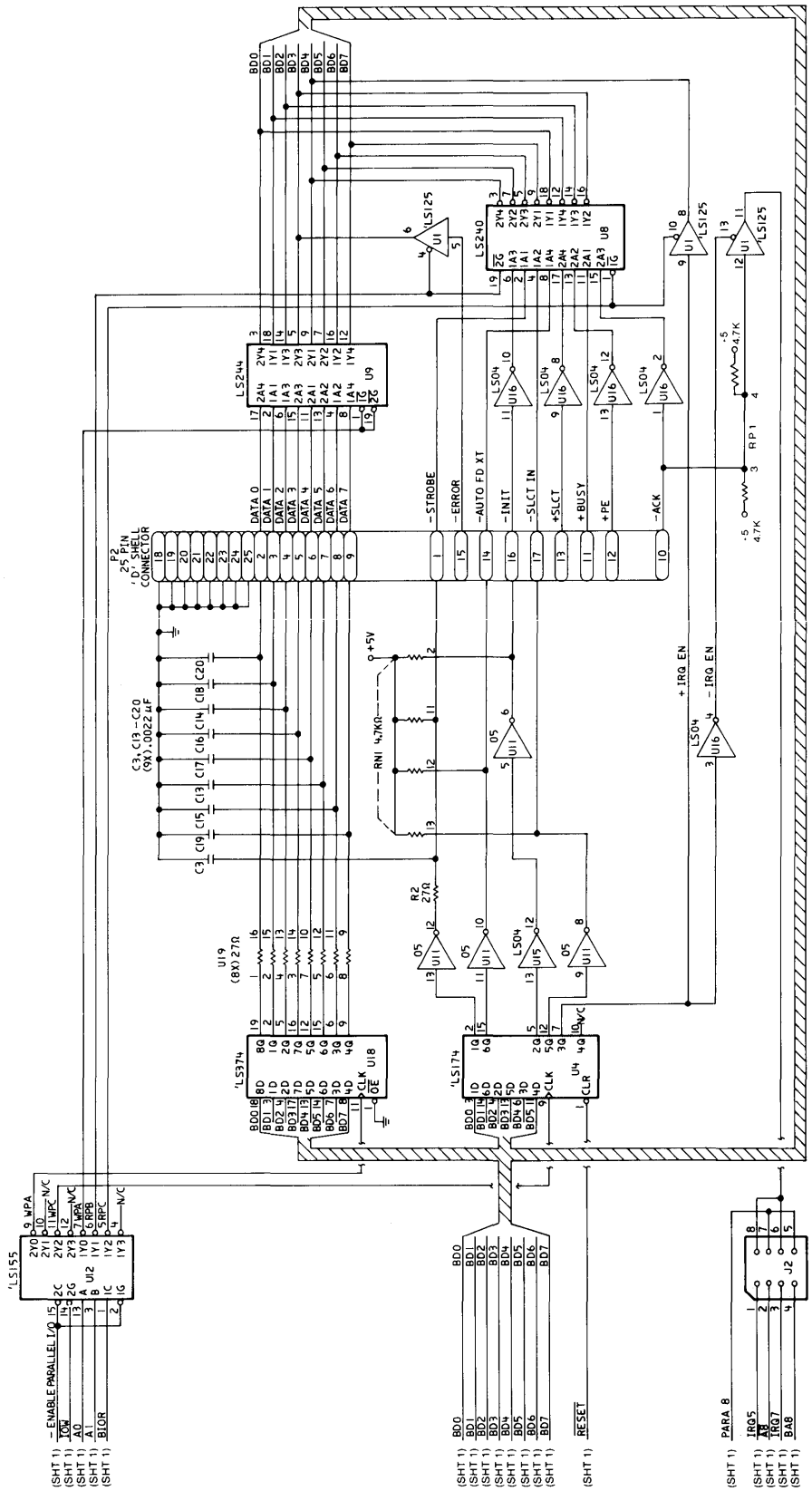
The following are the specifications for the serial interface.

Function	Condition
On	Spacing condition (binary 0, positive voltage).
Off	Marking condition (binary 1, negative voltage).

Voltage	Function
Above +15 Vdc	Invalid
+3 Vdc to +15 Vdc	On
-3 Vdc to +3 Vdc	Invalid
-3 Vdc to -15 Vdc	Off
Below -15 Vdc	Invalid

Serial Port Functions

Logic Diagrams *(continued)*



Serial/Printer Adapter (Sheet 2 of 3)

IBM Prototype Card

Contents

IBM Prototype Card

Description

The IBM Prototype Card is 106.7 millimeters (4.2 inches) high by 335.3 millimeters (13.2 inches) long and plugs into an expansion unit or system unit expansion slot. All system control signals and voltage requirements are provided through a 2- by 31-position card-edge tab.

The card contains a voltage bus (+ 5 Vdc) and ground bus (0 Vdc). Each bus borders the card, with the voltage bus on the back (pin side) and the ground bus on the front (component side). A system interface design is provided on the Prototype Card.

The Prototype Card can also accommodate a D-shell connector if it is needed. The connector size can range from a 9- to a 37-position connector.

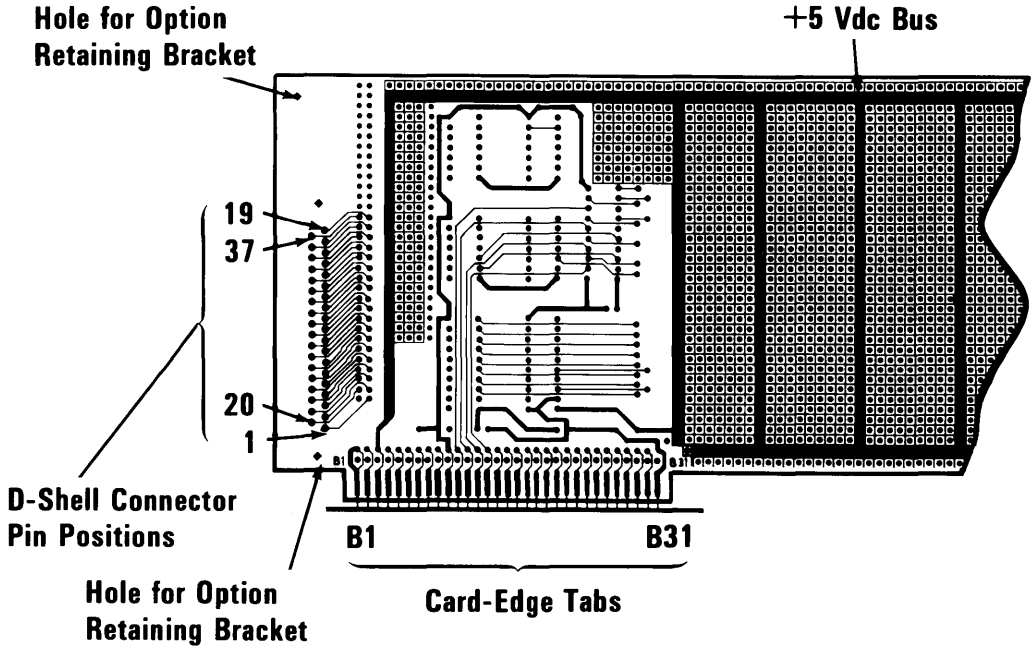
Warning: Install all components on the component side of the Prototype Card. The total width of the card, including components, should not exceed 12.7 millimeters (0.500 inch). If these specifications are not met, components on the Prototype Card may touch other cards plugged into adjacent slots.

I/O Channel Interface

The Prototype Card has two layers screened onto it (one on the front and one on the back). It also has 3,909 plated through-holes that are 10.1 millimeters (0.040 inch) in size and have a 1.52-millimeter (0.060-inch) pad, which is on a 2.54-millimeter (0.10-inch) grid. There are 37 plated through-holes that are 1.22 millimeter (0.048 inch) in size. These holes are at the rear of the card (viewed as if installed in the machine). These 37 holes are used for a 9- to 37-position D-shell connector. The card also has 5 holes that are 3.18 millimeters (0.125 inch) in size. One hole is located just above the two rows of D-shell connector holes, and the other four are located in the corners of the board (one in each corner).

Prototype Card Layout *(continued)*

The pin side has a + 5-Vdc bus, 1.27 millimeters (0.05 inch) wide, screened onto it, and card-edge tabs that are labeled B1 through B31.



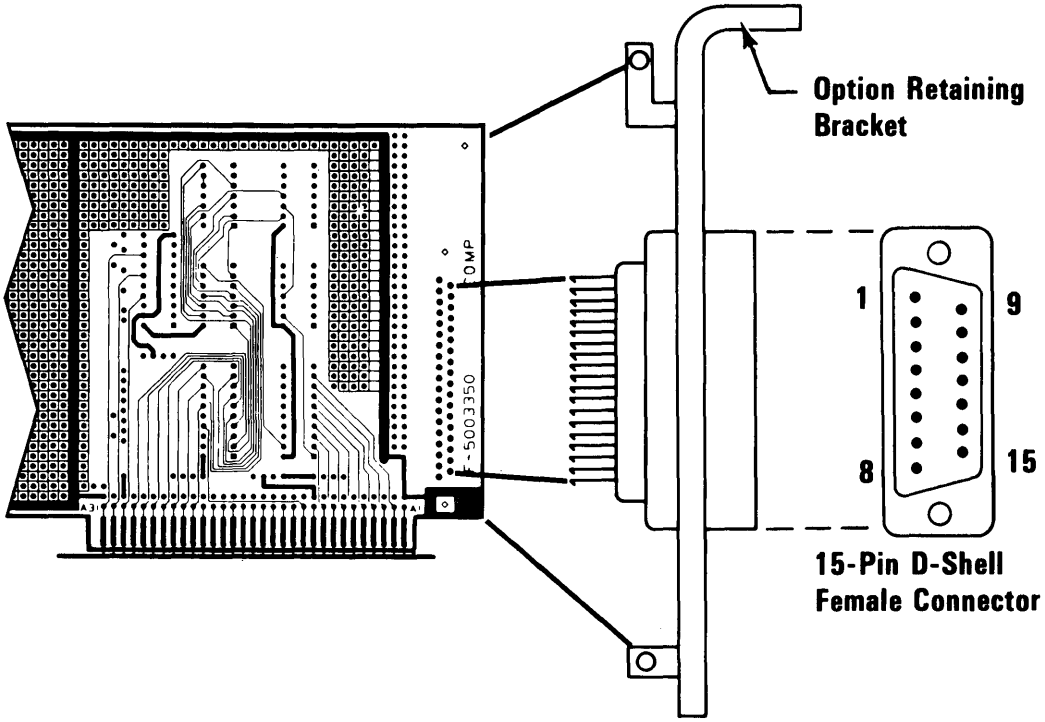
Each card-edge tab is connected to a plated through-hole by a 0.3-millimeter (0.012-inch) land. There are three ground tabs connected to the ground bus by three 0.3-millimeter (0.012-inch) lands. Also, there are two + 5-Vdc tabs connected to the voltage bus by two 0.3-millimeter (0.012-inch) lands.

For additional interfacing information, refer to "I/O Channel Description" and "I/O Channel Diagram" in your *Technical Reference* system manual. If the recommended interface logic is used, the following list of TTL-type numbers will help you select the necessary components.

Component	TTL Number	Description
U1	74LS245	Octal Bus Transceiver
U2, U5	74LS244	Octal Buffers Line Driver/Line Receivers
U4	74LS04	Hex Inverters
U3	74LS08	Quadruple 2 - Input Positive - AND Gate
U6	74LS02	Quadruple 2 - Input Positive - NOR Gate
U7	74LS21	Dual 4 - Input Positive - AND Gate
C1		10.0 µF Tantalum Capacitor
C2, C3, C4		0.047 µF Ceramic Capacitor

External Interface *(continued)*

The following example shows how a 15-pin, D-shell, female connector is attached to a prototype card.



Component Side

Prototype Adapter

Contents

Prototype Adapter

Description

The Prototype Adapter is 121.9 millimeters (4.8 inches) high by 333.25 millimeters (13.12 inches) long and plugs into any system-unit expansion slot except number 1 or 7. Two card-edge tabs, one 2-by 31- position and one 2-by 18-position, provide all system control signals and voltages.

The adapter has a voltage bus (+ 5 Vdc) and a ground bus (0 Vdc). Each bus borders the adapter, with the ground bus on the component side and the voltage bus on the pin side. A system interface is also provided on the adapter with a jumper to specify whether the device has an 8- or a 16-bit data bus.

This adapter also accommodates a D-shell connector from 9 to 37 positions.

Warning: All components must be installed on the component side of the adapter. The total width of the adapter, including components, may not exceed 12.7 millimeters (0.5 inch). If these specifications are not met, components on the Prototype Adapter may touch other adapters plugged into adjacent expansion slots.

Adapter Design

The following information is provided to assist design in designing an adapter using the Prototype Adapter.

Designing an Input/Output Adapter

The following information may be used to design an input/output type of adapter.

Programming

Insert a Jump instruction after all I/O read (IOR) or I/O write (IOW) assembler language instructions to avoid a potential timing problem caused by slow I/O devices. The following figure shows a typical programming sequence.

Before	After
Your Code	Your Code
IOR	IOR
Your Code	JMP NEXT
	NEXT: Your Code

Program Sequence

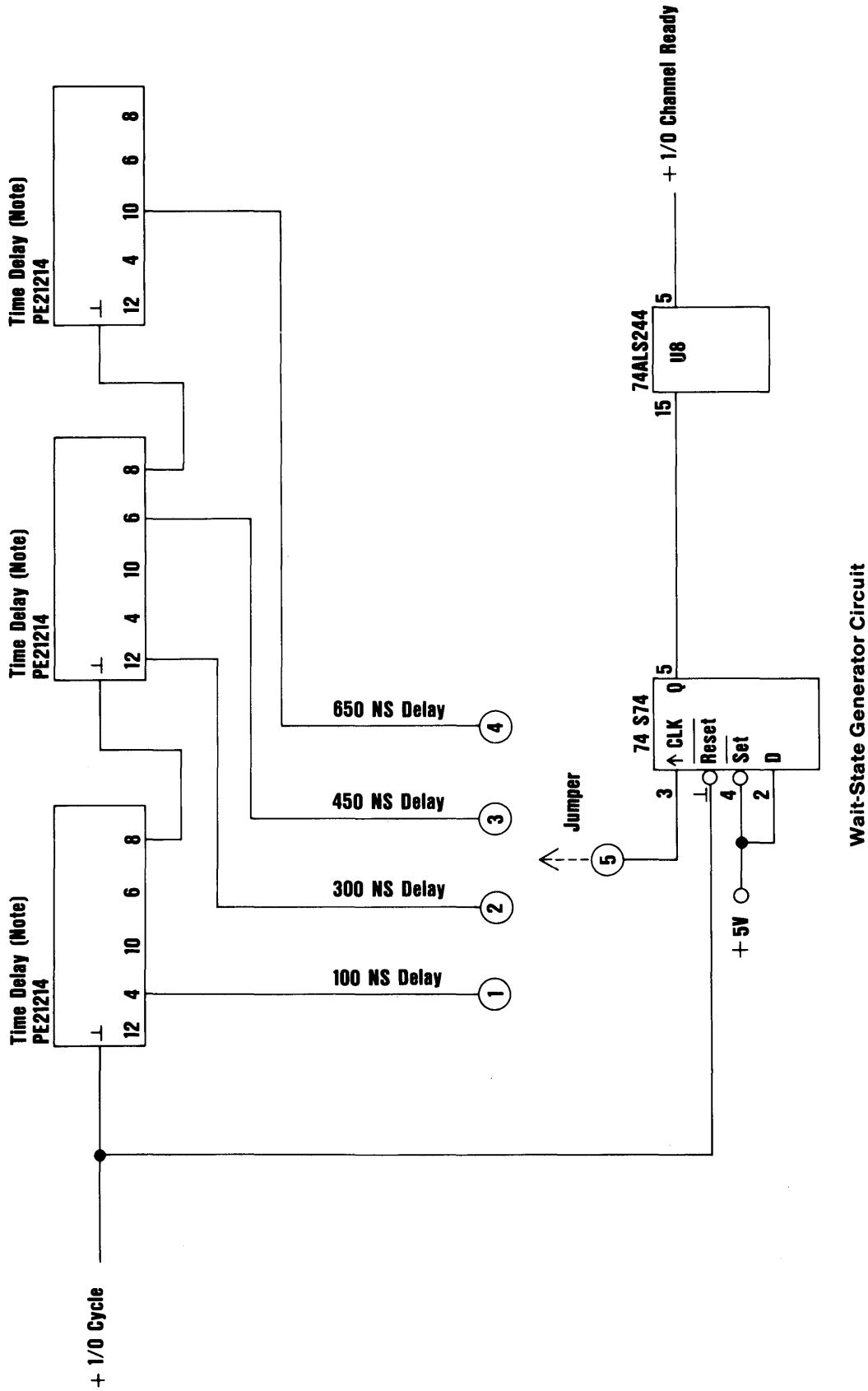
Jumper Wire (J1)

Your design can use either 8 bits of the data bus (jumper off) or the full 16 bits of the data bus (jumper on). Most devices have 8-bit data buses.

Wait-State Generator Circuits

If your device runs too slow, you must add a wait-state generator to make the I/O read and write signals longer. First, determine the time needed by your device from the start of an IOR signal until it can put data on the system's data bus. Next, compare that time with the time given by the system's microprocessor. The system microprocessor gives 750 nanoseconds for 8-bit devices and 250 nanoseconds for 16-bit devices.

Adapter Design *(continued)*



System Address Lines (SA)

The 20 lowest-order address lines are SA0 through SA19. SA address bits are active a minimum of 30 nanoseconds before a control line goes active, and they stay active until a minimum of 66 nanoseconds *after* the control line goes inactive. Timings are at the adapter socket.

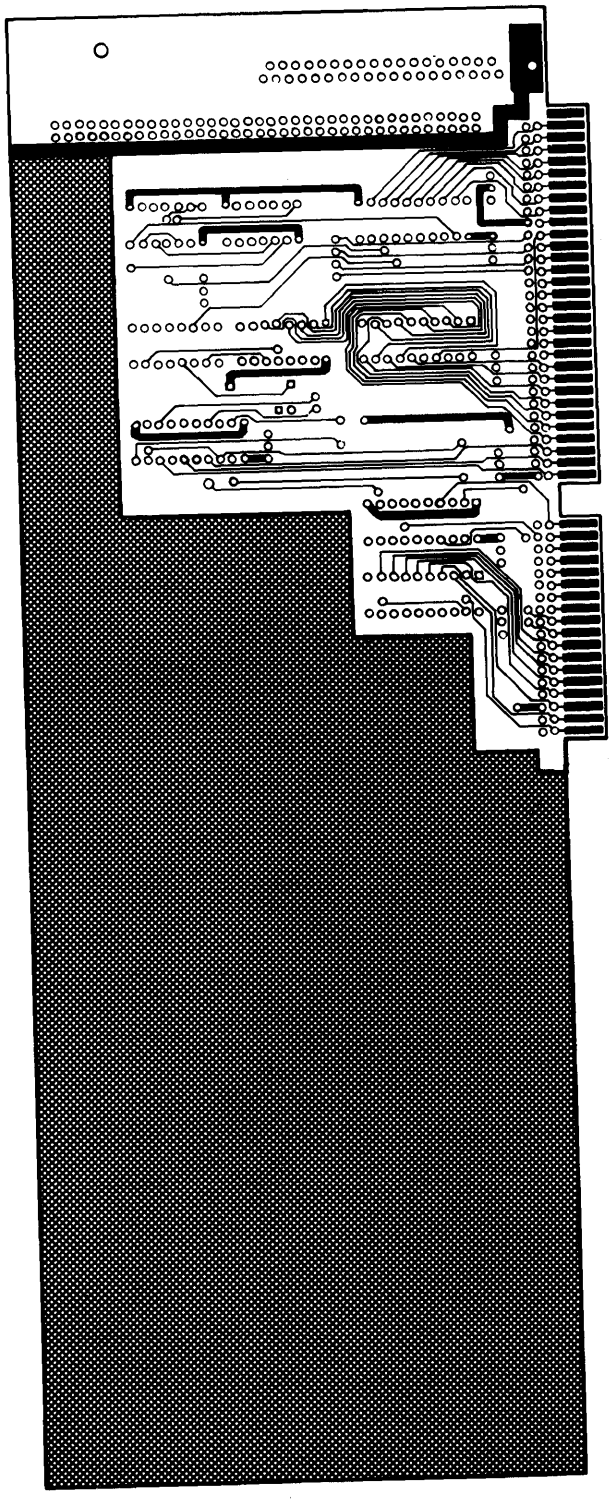
Local Address Lines (LA)

There are seven high-order address lines called LA17 through LA23. LA address bits are active a minimum of 159 nanoseconds before a control line goes active, and they stay active until typically 83 nanoseconds *before* the control line goes inactive. LA bits should be decoded to select the particular address range your memory occupies. Because this decode will go inactive 83 nanoseconds before the control line goes inactive, it may be necessary to latch the decode. The output of this decoder circuit should be connected to the input of a transparent latch, such as a 74ALS573 (BALE should be connected to the clock pin on the latch). If this is done, the output of the 74LS573 will be active approximately 30 nanoseconds before a control line goes active, and will stay active until approximately 66 nanoseconds *after* the control line goes inactive. Timings are at the adapter socket.

Prototype Adapter Layout *(continued)*

Component Side

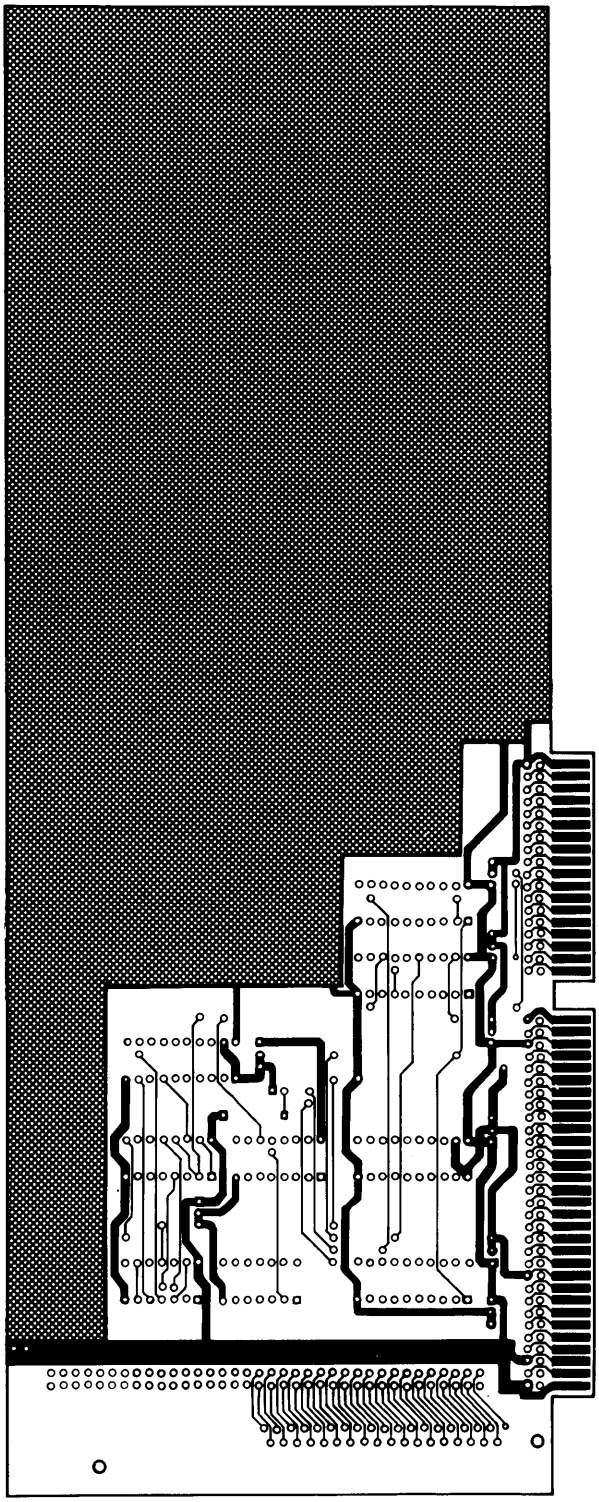
The component side of the adapter has a ground bus, 1.27 millimeters (0.05 inch) wide screened onto it and two card-edge tabs labeled A1 through A31 and C1 through C31. The following figure shows the ground bus and card edge-tabs.



Prototype Adapter Layout *(continued)*

Pin Side

The pin side of the adapter has a 5-Vdc bus, 1.27 millimeters (0.05 inch) wide, screened onto it, and two card-edge tabs: labeled B1 through B31 and D1 through D18. The following figure shows the 5-Vdc bus and card edge-tabs.



Interfaces

Internal Interface

Because of the number of adapters that may be installed in the system, I/O bus loading should be limited to 1 Schottky TTL load. If the recommended interface logic is used, this requirement is met. Power limitations may be found under 'Power Supply' in the IBM Personal Computer AT Technical Reference Manual.

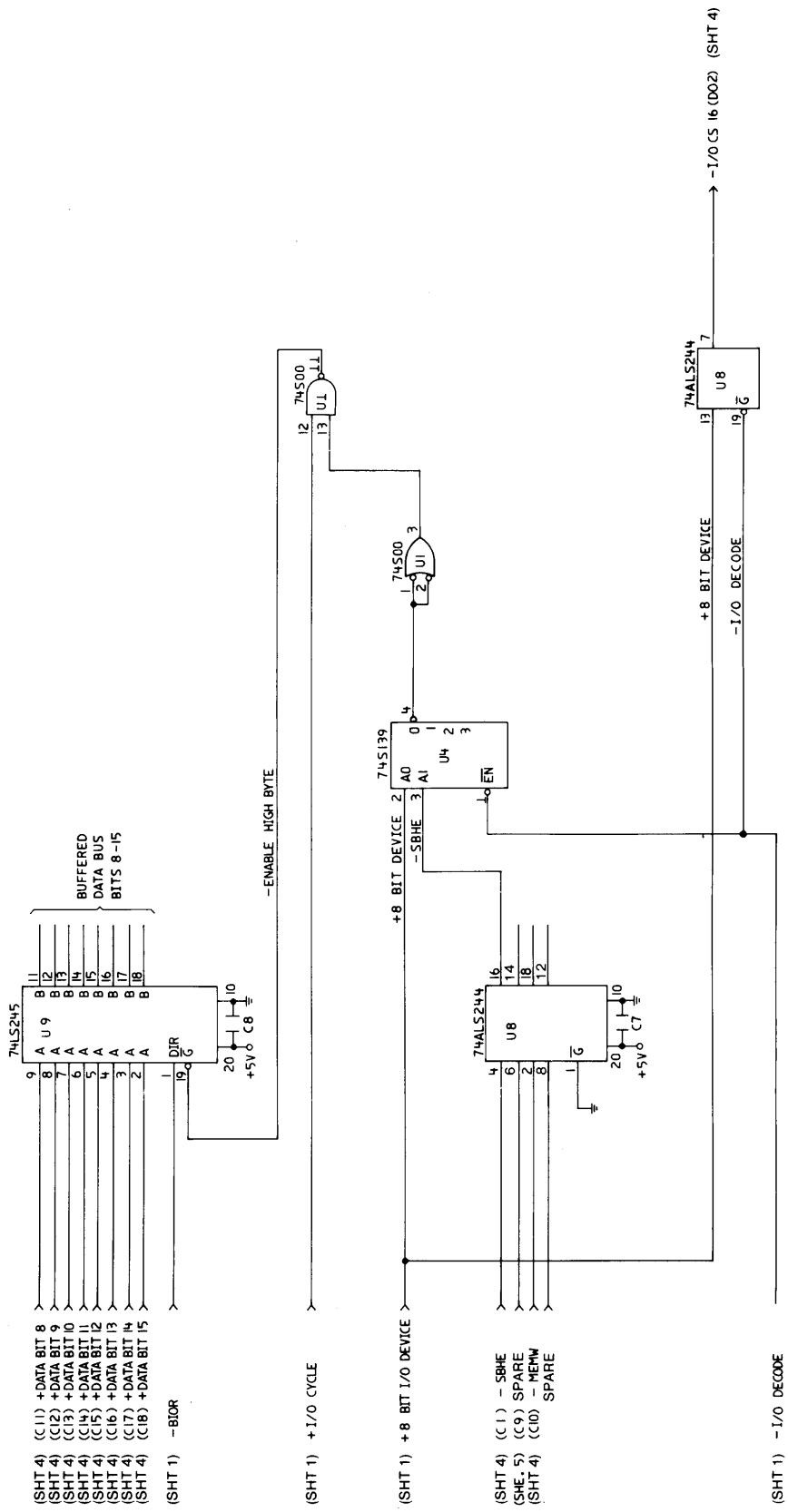
External Interface

The following figure lists the recommended connectors for the rear of the adapter.

Connector	Part no. (Amp) or Equivalent
9-Pin D-Shell (Male)	205865-1
9-Pin D-Shell (Female)	205866-1
15-Pin D-Shell (Male)	205867-1
15-Pin D-Shell (Female)	205868-1
25-Pin D-Shell (Male)	205857-1
25-Pin D-Shell (Female)	205858-1
37-Pin D-Shell (Male)	205859-1
37-Pin D-Shell (Female)	205860-1

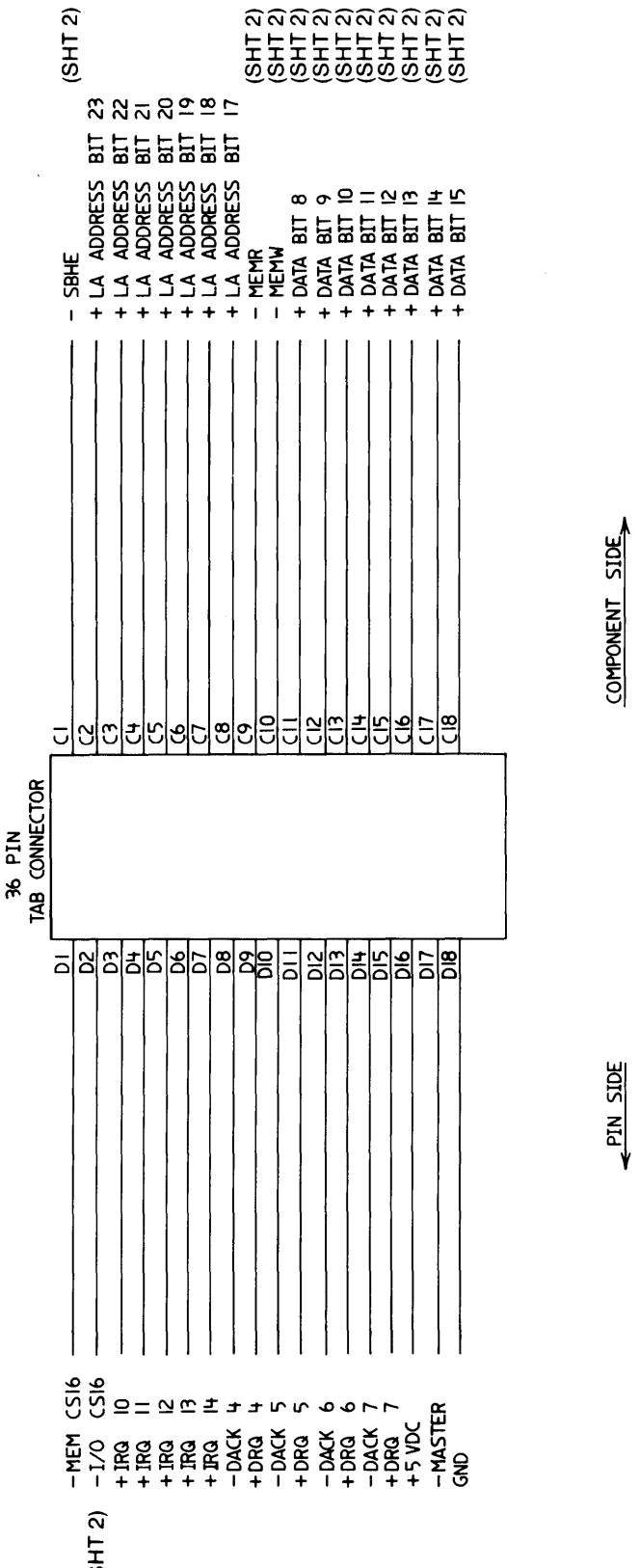
Recommended Connectors

Logic Diagrams *(continued)*



Prototype Adapter (Sheet 2 of 4)

Logic Diagrams *(continued)*



Prototype Adapter (Sheet 4 of 4)

Glossary

A. Ampere.

ac. Alternating current.

accumulator. A register in which the result of an operation is formed.

active high. Designates a signal that has to go high to produce an effect. Synonymous with positive true.

active low. Designates a signal that has to go low to produce an effect. Synonymous with negative true.

adapter. An auxiliary device or unit used to extend the operation of another system.

address bus. One or more conductors used to carry the binary-coded address from the processor throughout the rest of the system.

algorithm. A finite set of well-defined rules for the solution of a problem in a finite number of steps.

all points addressable (APA). A mode in which all points of a displayable image can be controlled by the user.

alphameric. Synonym for alphanumeric.

alphanumeric (A/N). Pertaining to a character set that contains letters, digits, and usually other characters, such as punctuation marks. Synonymous with alphameric.

alternating current (ac). A current that periodically reverses its direction of flow.

American National Standard Code for Information Exchange (ASCII). The standard code, using a coded character set consisting of 7-bit coded characters (8 bits including parity check), used for information exchange between data processing systems, data communication systems, and associated equipment. The ASCII set consists of control characters and graphic characters.

ampere (A). The basic unit of electric current.

A/N. Alphanumeric

analog. Pertaining to data in the form of continuously variable physical quantities. Contrast with digital.

AND. A logic operator having the property that if P is a statement, Q is a statement, R is a statement,..., then the AND of P, Q, R,...is true if all statements are true, false if any statement is false.

AND gate. A logic gate in which the output is 1 only if all inputs are 1.

AND operation. The boolean operation whose result has the boolean value 1, if and only if, each operand has the boolean value 1. Synonymous with conjunction.

APA. All points addressable.

ASCII. American National Standard Code for Information Exchange.

assemble. To translate a program expressed in an assembler language into a computer language.

CCITT. International Telegraph and Telephone Consultative Committee.

Celsius (C). A temperature scale. Contrast with Fahrenheit (F).

central processing unit (CPU). Term for processing unit.

channel. A path along which signals can be sent; for example, data channel, output channel.

character generator. In computer graphics, a functional unit that converts the coded representation of a graphic character into the shape of the character for display. In word processing, the means within equipment for generating visual characters or symbols from coded data.

character set. A finite set of different characters upon which agreement has been reached and that is considered complete for some purpose. A set of unique representations called characters. A defined collection of characters.

characters per second (cps). A standard unit of measurement for the speed at which a printer prints.

check key. A group of characters, derived from and appended to a data item, that can be used to detect errors in the data item during processing.

closed circuit. A continuous unbroken circuit; that is, one in which current can flow. Contrast with open circuit.

CMOS. Complementary metal oxide semiconductor.

code. A set of unambiguous rules specifying the manner in which data may be represented in a discrete form. Synonymous with coding scheme. A set of items, such as abbreviations, representing the members of another set. To represent data or a computer program in a symbolic form that can be accepted by a data processor. Loosely, one or more computer programs, or part of a computer program.

coding scheme. Synonym for code.

collector. An element in a transistor toward which current flows.

column address strobe (CAS). A signal that latches the column addresses in a memory chip.

compile. To translate a computer program expressed in a problem-oriented language into a computer-oriented language. To prepare a machine-language program from a computer program written in another programming language by making use of the overall logic structure of the program, or generating more than one computer instruction for each symbolic statement, or both, as well as performing the function of an assembler.

complementary metal oxide semiconductor (CMOS). A logic circuit family that uses very little power. It works with a wide range of power supply voltages.

computer. A functional unit that can perform substantial computation, including numerous arithmetic operations or logic operations, without intervention by a human operator during a run.

computer instruction code. A code used to represent the instructions in an instruction set. Synonymous with machine code.

computer program. A sequence of instructions suitable for processing by a computer.

computer word. A word stored in one computer location and capable of being treated as a unit.

configuration. The arrangement of a computer system or network as defined by the nature, number, and the chief characteristics of its functional units. More specifically, the term configuration may refer to a hardware configuration or a software configuration. The devices and programs that make up a system, subsystem, or network.

conjunction. Synonym for AND operation.

contiguous. Touching or joining at the edge or boundary; adjacent.

control character. A character whose occurrence in a particular context initiates, modifies, or stops a control operation.

control operation. An action that affects the recording, processing, transmission, or interpretation of data; for example, starting or stopping a process, carriage return, font change, rewind, and end of transmission.

control storage. A portion of storage that contains microcode.

cps. Characters per second.

CPU. Central processing unit.

CRC. Cyclic redundancy check.

CRT. Cathode ray tube.

CRT display. Cathode ray tube display.

CTS. Clear to send. Associated with modem control.

cursor. In computer graphics, a movable marker that is used to indicate a position on a display. A displayed symbol that acts as a marker to help the user locate a point in text, in a system command, or in storage. A movable spot of light on the screen of a display device, usually indicating where the next character is to be entered, replaced, or deleted.

DTR. In the IBM Personal Computer, data terminal ready. Associated with modem control.

dual in-line package (DIP). A widely used container for an integrated circuit. DIPs have pins in two parallel rows. The pins are spaced 1/10 inch apart. See also DIP switch.

duplex. In data communication, pertaining to a simultaneous two-way independent transmission in both directions. Contrast with half-duplex.

duty cycle. In the operation of a device, the ratio of on time to idle time. Duty cycle is expressed as a decimal or percentage.

dynamic memory. RAM using transistors and capacitors as the memory elements. This memory requires a refresh (recharge) cycle every few milliseconds. Contrast with static memory.

EBCDIC. Extended binary-coded decimal interchange code.

ECC. Error checking and correction.

edge connector. A terminal block with a number of contacts attached to the edge of a printed-circuit board to facilitate plugging into a foundation circuit.

EIA. Electronic Industries Association.

electromagnet. Any device that exhibits magnetism only while an electric current flows through it.

enable. To initiate the operation of a circuit or device.

end of block (EOB). A code that marks the end of a block of data.

end of file (EOF). An internal label, immediately following the last record of a file, signaling the end of that file. It may include control totals for comparison with counts accumulated during processing.

end-of-text (ETX). A transmission control character used to terminate text.

end-of-transmission (EOT). A transmission control character used to indicate the conclusion of a transmission, which may have included one or more texts and any associated message headings.

end-of-transmission-block (ETB). A transmission control character used to indicate the end of a transmission block of data when data is divided into such blocks for transmission purposes.

EOB. End of block.

EOF. End of file.

EOT. End-of-transmission.

EPROM. Erasable programmable read-only memory.

erasable programmable read-only memory (EPROM). A PROM in which the user can erase old information and enter new information.

error checking and correction (ECC). The detection and correction of all single-bit errors, plus the detection of double-bit and some multiple-bit errors.

ESC. The escape character.

escape character (ESC). A code extension character used, in some cases, with one or more succeeding characters to indicate by some convention or agreement that the coded representations following the character or the group of characters are to be interpreted according to a different code or according to a different coded character set.

ETB. End-of-transmission-block.

ETX. End-of-text.

extended binary-coded decimal interchange code (EBCDIC). A set of 256 characters, each represented by eight bits.

F. Fahrenheit.

Fahrenheit (F). A temperature scale. Contrast with Celsius (C).

falling edge. Synonym for negative-going edge.

FCC. Federal Communications Commission.

fetch. To locate and load a quanity of data from storage.

FF. The form feed character.

field. In a record, a specified area used for a particular category of data. In a data base, the smallest unit of data that can be referred to.

fixed disk drive. In the IBM Personal Computer, a unit consisting of nonremovable magnetic disks, and a device for storing data on and retrieving data from the disks.

flag. Any of various types of indicators used for identification. A character that signals the occurrence of some condition, such as the end of a word. Deprecated term for mark.

flexible disk. Synonym for diskette.

flip-flop. A circuit or device containing active elements, capable of assuming either one of two stable states at a given time.

inhibited. Pertaining to a state of a processing unit in which certain types of interruptions are not allowed to occur. Pertaining to the state in which a transmission control unit or an audio response unit cannot accept incoming calls on a line.

initialize. To set counters, switches, addresses, or contents of storage to 0 or other starting values at the beginning of, or at prescribed points in, the operation of a computer routine.

input/output (I/O). Pertaining to a device or to a channel that may be involved in an input process, and, at a different time, in an output process. In the English language, "input/output" may be used in place of such terms as "input/output, data" "input/output signal," and "input/output terminals," when such usage is clear in a given context. Pertaining to a device whose parts can be performing an input process and an output process at the same time. Pertaining to either input or output, or both.

instruction. In a programming language, a meaningful expression that specifies one operation and identifies its operands, if any.

instruction set. The set of instructions of a computer, of a programming language, or of the programming languages in a programming system.

interface. A device that alters or converts actual electrical signals between distinct devices, programs, or systems.

interleave. To arrange parts of one sequence of things or events so that they alternate with parts of one or more other sequences of the same nature and so that each sequence retains its identity.

interrupt. A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed. In a data transmission, to take an action at a receiving station that causes the transmitting station to terminate a transmission. Synonymous with interruption.

I/O. Input/output.

I/O area. Synonym for buffer.

irrecoverable error. An error that makes recovery impossible without the use of recovery techniques external to the computer program or run.

joystick. In computer graphics, a lever that can pivot in all directions and that is used as a locator device.

k. Prefix kilo; 1000.

K. When referring to storage capacity, 1024. (1024 = 2 to the 10th power.)

Kb. 1024 bytes.

kg. Kilogram; 1000 grams.

kHz. Kilohertz; 1000 hertz.

kilo (k). Prefix 1000

kilogram (kg). 1000 grams.

kilohertz (kHz). 1000 hertz

latch. A simple logic-circuit storage element. A feedback loop in sequential digital circuits used to maintain a state.

least-significant digit. The rightmost digit. See also low-order position.

LED. Light-emitting diode.

light-emitting diode (LED). A semiconductor device that gives off visible or infrared light when activated.

load. In programming, to enter data into storage or working registers.

low power Schottky TTL. A version (LS series) of TTL giving a good compromise between low power and high speed. See also transistor-transistor logic and Schottky TTL.

low-order position. The rightmost position in a string of characters. See also least-significant digit.

m. Prefix milli; 0.001. Meter.

M. Prefix mega; 1 000 000. When referring to computer storage capacity, 1&rbl.048&rbl.576. (1 048 576 = 2 to the 20th power.)

mA. Milliampere; 0.001 ampere.

machine code. The machine language used for entering text and program instructions onto the recording medium or into storage and which is subsequently used for processing and printout.

machine language. A language that is used directly by a machine. Deprecated term for computer instruction code.

magnetic disk. A flat circular plate with a magnetizable surface layer on which data can be stored by magnetic recording. See also diskette.

main storage. Program-addressable storage from which instructions and other data can be loaded directly into registers for subsequent execution or processing. Contrast with auxiliary storage.

mark. A symbol or symbols that indicate the beginning or the end of a field, of a word, of an item of data, or of a set of data such as a file, a record, or a block.

nano (n) . Prefix 0.000 000 001.

nanosecond (ns) . 0.000 000 001 second.

negative true . Synonym for active low.

negative-going edge . The edge of a pulse or signal changing in a negative direction. Synonymous with falling edge.

non-return-to-zero change-on-ones recording (NRZI) . A transmission encoding method in which the data terminal equipment changes the signal to the opposite state to send a binary 1 and leaves it in the same state to send a binary 0.

non-return-to-zero (inverted) recording (NRZI) . Deprecated term for non-return-to-zero change-on-ones recording.

NOR . A logic operator having the property that if P is a statement, Q is a statement, R is a statement,..., then the NOR of P, Q, R,... is true if all statements are false, false if at least one statement is true.

NOR gate . A gate in which the output is 0 only if at least one input is 1.

NOT . A logical operator having the property that if P is a statement, then the NOT of P is true if P is false, false if P is true.

NRZI . Non-return-to-zero change-on-ones recording.

ns . Nanosecond; 0.000 000 001 second.

NUL . The null character.

null character (NUL) . A control character that is used to accomplish media-fill or time-fill, and that may be inserted into or removed from, a sequence of characters without affecting the meaning of the sequence; however, the control of the equipment or the format may be affected by this character.

odd-even check . Synonym for parity check.

offline . Pertaining to the operation of a functional unit without the continual control of a computer.

one-shot . A circuit that delivers one output pulse of desired duration for each input (trigger) pulse.

open circuit . A discontinuous circuit; that is, one that is broken at one or more points and, consequently, cannot conduct current. Contrast with closed circuit. Pertaining to a no-load condition; for example, the open-circuit voltage of a power supply.

open collector . A switching transistor without an internal connection between its collector and the voltage supply. A connection from the collector to the voltage supply is made through an external (pull-up) resistor.

operand . An entity to which an operation is applied. That which is operated upon. An operand is usually identified by an address part of an instruction.

operating system . Software that controls the execution of programs; an operating system may provide services such as resource allocation, scheduling, input/output control, and data management.

OR . A logic operator having the property that if P is a statement, Q is a statement, R is a statement,..., then the OR of P, Q, R,... is true if at least one statement is true, false if all statements are false.

OR gate . A gate in which the output is 1 only if at least one input is 1.

output . Pertaining to a device, process, or channel involved in an output process, or to the data or states involved in an output process.

output process . The process that consists of the delivery of data from a data processing system, or from any part of it. The return of information from a data processing system to an end user, including the translation of data from a machine language to a language that the end user can understand.

overcurrent . A current of higher than specified strength.

overflow indicator . An indicator that signifies when the last line on a has been printed or passed. An indicator that is set on if the result of an arithmetic operation exceeds the capacity of the accumulator.

overrun . Loss of data because a receiving device is unable to accept data at the rate it is transmitted.

overvoltage . A voltage of higher than specified value.

parallel . Pertaining to the concurrent or simultaneous operation of two or more devices, or to the concurrent performance of two or more activities. Pertaining to the concurrent or simultaneous occurrence of two or more related activities in multiple devices or channels. Pertaining to the simultaneity of two or more processes. Pertaining to the simultaneous processing of the individual parts of a whole, such as the bits of a character and the characters of a word, using separate facilities for the various parts. Contrast with serial.

parameter . A variable that is given a constant value for a specified application and that may denote the application. A name in a procedure that is used to refer to an argument passed to that procedure.

parity bit . A binary digit appended to a group of binary digits to make the sum of all the digits either always odd (odd parity) or always even (even parity).

read. To acquire or interpret data from a storage device, from a data medium, or from another source.

read-only memory (ROM). A storage device whose contents cannot be modified. The memory is retained when power is removed.

read/write memory. A storage device whose contents can be modified. Also called RAM.

recoverable error. An error condition that allows continued execution of a program.

red-green-blue-intensity (RGBI). The description of a direct-drive color monitor that accepts input signals of red, green, blue, and intensity.

redundancy check. A check that depends on extra characters attached to data for the detection of errors. See cyclic redundancy check.

register. A storage device, having a specified storage capacity such as a bit, a byte, or a computer word, and usually intended for a special purpose. A storage device in which specific data is stored.

retry. To resend the current block of data (from the last EOB or ETB) a prescribed number of times, or until it is entered correctly or accepted.

reverse video. A form of highlighting a character, field, or cursor by reversing the color of the character, field, or cursor with its background; for example, changing a red character on a black background to a black character on a red background.

RF. Radio frequency.

RF modulator. The device used to convert the composite video signal to the antenna level input of a home TV.

RGBI. Red-green-blue-intensity.

rising edge. Synonym for positive-going edge.

ROM. Read-only memory.

ROM/BIOS. The ROM resident basic input/output system, which provides the level control of the major I/O devices in the computer system.

row address strobe (RAS). A signal that latches the row address in a memory chip.

RS-232C. A standard by the EIA for communication between computers and external equipment.

RTS. Request to send. Associated with modem control.

run. A single continuous performance of a computer program or routine.

schematic. The representation, usually in a drawing or diagram form, of a logical or physical structure.

Schottky TTL. A version (S series) of TTL with faster switching speed, but requiring more power. See also transistor-transistor logic and low power Schottky TTL.

SDLC. Synchronous Data Link Control.

sector. That part of a track or band on a magnetic drum, a magnetic disk, or a disk pack that can be accessed by the magnetic heads in the course of a predetermined rotational displacement of the particular device.

SERDES. Serializer/deserializer.

serial. Pertaining to the sequential performance of two or more activities in a single device. In English, the modifiers serial and parallel usually refer to devices, as opposed to sequential and consecutive, which refer to processes. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. Pertaining to the sequential processing of the individual parts of a whole, such as the bits of a character or the characters of a word, using the same facilities for successive parts. Contrast with parallel.

serializer/deserializer (SERDES). A device that serializes output from, and deserializes input to, a business machine.

setup. In a computer that consists of an assembly of individual computing units, the arrangement of interconnections between the units, and the adjustments needed for the computer to operate. The preparation of a computing system to perform a job or job step. Setup is usually performed by an operator and often involves performing routine functions, such as mounting tape reels. The preparation of the system for normal operation.

short circuit. A low-resistance path through which current flows, rather than through a component or circuit.

signal. A variation of a physical quantity, used to convey data.

sink. A device or circuit into which current drains.

software. Computer programs, procedures, and rules concerned with the operation of a data processing system. Contrast with hardware.

source. The origin of a signal or electrical energy.

square wave. An alternating or pulsating current or voltage whose waveshape is square.

square wave generator. A signal generator delivering an output signal having a square waveform.

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Technical Reference Options and Adapters Volume 2
Part Number 6523280

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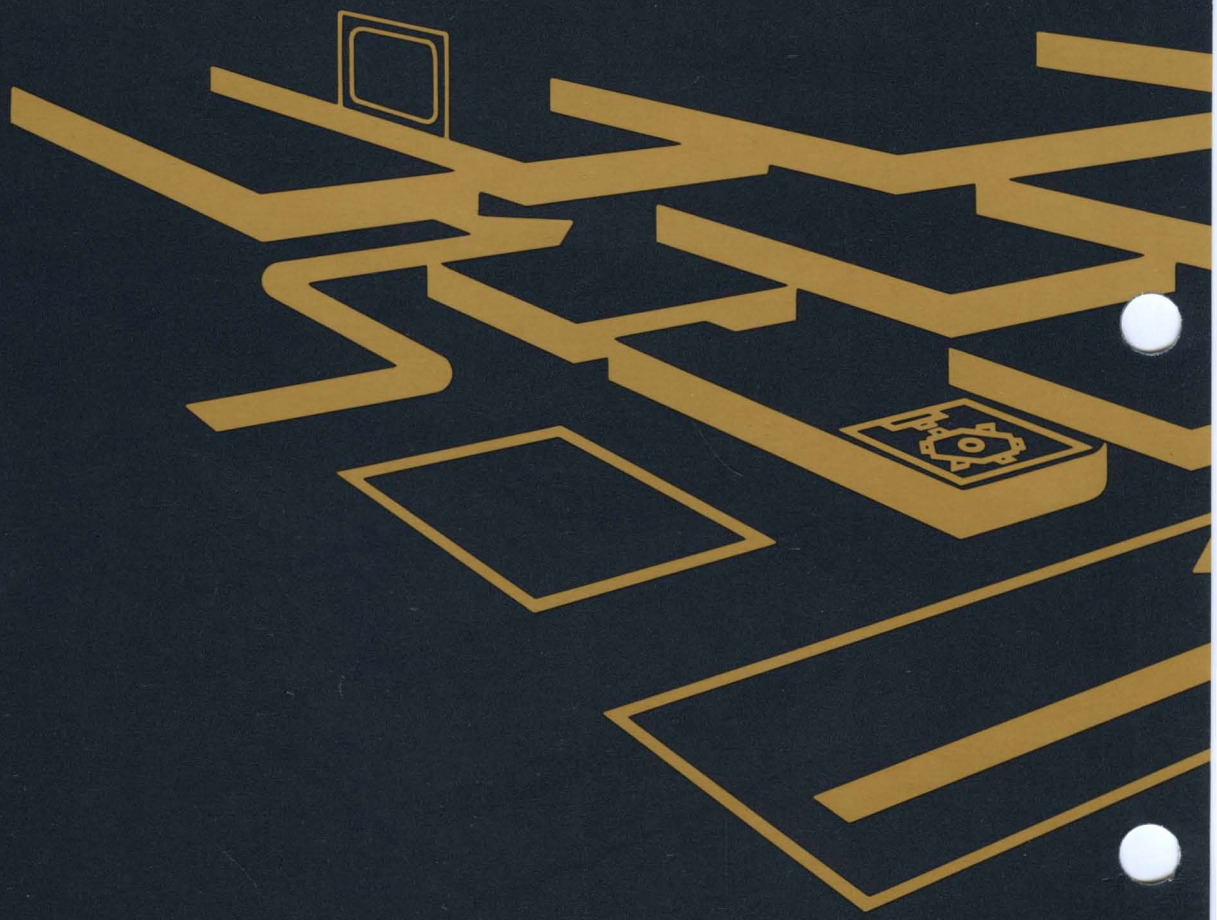

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