IBM Maintenance Library

3803-2/ 3420 S/N	3803-2/ 3420 S/N	3803-2/ 3420 S/N	3803-2/ 3420 S/N
MLM	**MLM**	**MLM**	**MLM**
PLAN START SENSE MAP 00-000 1A-000 6A-XXX 1B-000 6B-XXX	INTF 07-000 CARR 08-000 MAP 11-000 15-XXX	MAP 16-000 21-XXX	OPER 40-000 58-XXX REF 75-001 85-XXX INST 90-000 INDEX
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3803-2 / 3420

Magnetic Tape Subsystem Maintenance Manual

3803-2/3420

XG0005 Seq 1 of 2	2736038 Part Number	See EC History	845958 1 Sep 79					

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SAFETY

PERSONAL

The importance of personal safety cannot be overemphasized. To ensure personal safety and the safety of co-workers, follow established safety practices and procedures at all times.

Look for and obey the DANGER notices found in the maintenance documentation. All CEs must be familiar with the general safety practices and the procedures for artiticial respiration outlines in IBM Form 229-1264. For convenience, this form is duplicated to the right.

MACHINE

To protect machines from damage, turn off power before removing or inserting circuit cards of components. Do not leave internal machine areas needlessly exposed, avoid shoring panel pins when scoping, and handle machine parts sarefully, in addition, look for and observe the CAUTION notices found in maintenance documentation.

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it; for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment - eliminate unsafe acts.

ARTIFICIAL RESPIRATION

General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects. Pull tongue forward.
3. Loosen Clothing – Keep Victim Warm
   Take care of these items after victim is breathing by himself or when help is available.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

1. Place victim on his back immediately.
2. Clear throat of water, food, or foreign matter.
3. Tilt head back to open air passage.
4. Lift jaw up to keep tongue out of air passage.
5. Pinch nostrils to prevent air leakage when you blow.
6. Blow until you see chest rise.
7. Remove your lips and allow lungs to empty.
8. Listen for snoring and gurglings – signs of throat obstruction.
9. Repeat mouth to mouth breathing 10-20 times a minute. Continue rescue breathing until victim breathes for himself.

Thumb and finger positions

Final mouth-to-mouth position

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BASIC SUBSYSTEM

The IBM 3803-2/3420 Magnetic Tape Subsystem consists of an IBM 3803 Model 2 Tape Control and one or more IBM 3420 Magnetic Tape Units. The 3420 tape units are available in six models with tape speeds of 75, 125, and 200 inches per second (ips) (190,5/317,5/508 cm/sec) for Models 3 and 4, 5 and 6, and 7 and 8, respectively.

The 3803 Model 2 operates in 6250 bpi and 1600 bpi modes.

A 3803 tape control without any switching features controls up to eight 3420 tape units (1×8 configuration, also called selection logic).

The 3803 command set, status responses, and basic sense data are compatible with those used by IBM 2400-series tape subsystems. However, there are some minor programming differences. For example:

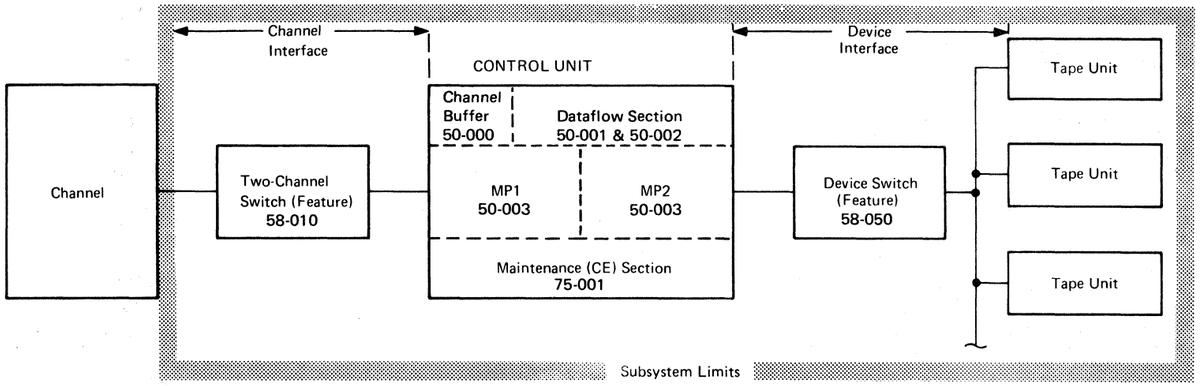
1. The number of sense bytes and contents of those bytes differ from those used by 2400-series subsystems.
2. All commands not shown on 40-005 and 40-008 set COMMAND REJECT in the sense information which, in turn, sets Unit Check in the status byte, indicating to the system that something is wrong.
3. A sense command must be issued after an error condition sets Unit Check in the unit status byte.

In most instances, non-time dependent programs that operate successfully on an IBM 2400-series tape subsystem will operate correctly on an IBM 3803-2/3420 subsystem.

3420 TAPE UNIT

Information presented in this section applies to all models of the tape unit.

With compatible features, 3420 Models 3, 5, and 7 can be attached to the 3803-2 without modification.



3803/3420 Subsystem Schematic

AUTOMATIC THREADING

A write reel latch secures the file reel to the reel hub automatically. When the operator places a file reel or cartridge on the reel hub and presses LOAD/REWIND, the power window closes, the write reel latch secures the file reel to the hub, and tape is automatically threaded, loaded into the vacuum columns, and positioned at load point without further operator action.

IBM Easy load cartridge

When used with a solid-flange tape reel (standard IBM 10.5 inch), the optional, IBM Easy Load Cartridge reduces tape handling and helps prevent tape contamination or physical damage.

During a load operation, if the first threading sequence is unsuccessful, tape is rewound into the cartridge and another attempt is made.

TAPE TRANSPORT

A single direct-drive capstan moves tape forward or backward. Air bearings reduce friction and tape wear since the oxide (recording) surface of the tape contacts only the read/write head and the tape cleaner. Short, tapered vacuum columns greatly reduce tape inertia when starting and stopping tape. The tapered columns and single, direct-drive capstan start and stop tape quickly and smoothly.

REWINDING

Tape remains in the vacuum columns during rewind operations. Rewind ends when a photocell senses a) reflective marker on beginning-of-tape (load point) reflective marker on tape.

During a rewind unload operation, tape is rewound completely onto the file reel. The tape unit is left in unloaded status, with the tape reel latch unlocked and the window open, allowing the operator to remove the file reel.

READ BACK CHECKING

A two-gap read/write head with 0.150 inch (3,81 mm) between read and write gaps allows read back checking during a write operation. Moving forward, tape passes first the write gap, then the read gap.

FULL-WIDTH ERASURE

An erase head applies a strong magnetic field that erases the entire width of tape during write operations. Full-width erasure prevents interchangeability problems when tape is written on one tape unit and read on another; it also reduces the chances of leaving extraneous bits in interblock gaps or skip areas.

During a write, write tape mark, or erase operation, the tape unit monitors the erase head operation. On a 3420 Model 4, 6, or 8, an erase head failure drops tape unit ready status and halts tape motion. On a 3420 Model 3, 5, or 7, an erase head failure sets Unit Check, but does not drop ready status.

FILE PROTECTION

A write enable ring must be present in the file reel when writing. To avoid destroying information on tape, the write enable ring is removed. A reel without the ring is "file-protected". FILE PROTECT turns on when the reel is mounted and no writing can occur.

3420 MODELS 4, 6, AND 8

Models 4, 6, and 8 tape units can write and read 6250 bpi tapes with 0.3-inch interblock gaps. Nominal data rates are 470, 780, and 1250 kilobytes per second at 6250 bpi.

A tape cleaning mechanism is added.

3420 Models 3, 5, and 7 can be converted in the field to Models 4, 6, and 8.

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RECORDING METHODS

6250 BPI

In 6250 bpi mode, 6250 data bytes per inch (246 data bytes per mm) are recorded in nine parallel tracks on tape. 6250 bpi tapes are written with an identification burst (ID burst) in track 1 at load point. The ID burst is followed by a control burst and a 0.3-inch (7,62 mm) IBG before a data block is written.

6250 bpi is a basic density on 3803 Model 2 and on 3420 Models 4, 6, and 8.

6250 BPI ERROR CORRECTION

The 6250 bpi format employs an error-correcting/detecting code capable of correcting all single-track errors on the strength of the code alone and correcting all double-track errors with the aid of track pointers. Pointers such as phase error and incorrect pattern are indications of questionable data. If the errors fall outside the code capability, Data Check and Unit Check are set and Error Recovery Procedures (ERPs) are invoked.

1600 BPI

In 1600 bpi mode, 1600 bytes per inch (63 bytes per mm) are recorded in nine parallel tracks on tape. The data format uses eight of the nine bits for data, the ninth is a parity bit. Data is recorded in odd parity. The eight bits of one byte can represent an alphabetic character, zoned decimal digit, two decimal digits (packed), a special character, or eight binary bits.

1600 bpi is a basic density on the 3803 Model 2 and on 3420 Models 3, 5, and 7, and a feature on 3420 Models 4, 6, and 8.

NINE-TRACK NRZI

In nine-track NRZI, data is recorded at 800 bpi (31,5 bytes per mm) in nine parallel tracks on tape. Data representation is the same as for 1600 bpi PE. For nine-track NRZI operation, the dual density feature is required on a Model 3, 5, or 7 tape unit and the nine-track NRZI feature is required on a 3803 Model 2.

SEVEN-TRACK NRZI

In seven-track NRZI mode, data is recorded at 200, 556, or 800 bpi (7, 6/21, 9/31, 5 bytes per mm). The data format uses six of the seven bits for data and the seventh bit for parity checking. Data is recorded in either odd or even parity. The six bits of one character can represent a BCD character or six binary bits. For seven-track NRZI operation, a seven-track feature is required on both a 3420 Model 3, 5, or 7 and on the 3803-2.

INTERBLOCK GAP

An interblock gap (IBG) is the erased section of tape used to indicate the end of a block or record. Interblock gaps are:

6250 bpi: 0.3 inch (7,6 mm) nominal.

Nine-track PE/NRZI: 0.6 inch (15,2 mm) nominal; 0.5 inch (12,7 mm) minimum.

Seven-track: 0.75 inch (19,05 mm) nominal; 0.68 inch (17,27 mm) minimum.

MAGNETIC TAPE AND REELS

Most tape volumes that operate satisfactorily on 3420 Models 3, 5, and 7 will operate with equal or better read/write reliability for an equivalent number of bytes transferred on 3420 Models 4, 6, or 8. Tape must conform to *IBM Half-Inch Tape Specifications*, GA32-0006.

3420 SUBSYSTEM CHARACTERISTICS

	Model 3	Model 4	Model 5	Model 6	Model 7	Model 8
Tape Speed (Read or Write)						
(ips)	75	75	125	125	200	200
(cm/sec)	190,5	190,5	317,5	317,5	508	508
6250 Read Access Time, nominal*(ms)		2.3		1.6		1.1
1600 Read Access Time, nominal*(ms)	4.0	4.0	2.9	2.6	2.0	1.65
6250 Write Access Time, nominal*(ms)		2.1		1.5		0.95
1600 Write Access Time, nominal*(ms)	4.0	3.0	2.9	2.0	2.0	1.28
Forward Start Time, nominal**(ms)	1.8	1.4	1.4	1.1	1.3	.08
Data Rates (Kb/sec; Kd/sec):						
6250 BPI		470/940		780/1560		1250/2500
1600 BPI PE	120/240	120/240	200/400	200/400	320/640	320/640
800 BPI NRZI (9-Track)	60/120		100/200		160/320	
800 BPI NRZI (7-Track)	60		100		160	
556 BPI NRZI (7-Track)	41.7		69.5		111.2	
200 BPI NRZI (7-Track)		15.0	25.0		40.0	
Passing Times per Byte (μsec):						
6250 BPI		2.133		1.28		0.80
1600 BPI PE	8.3	8.3	5.0	5.0	3.1	3.1
800 BPI NRZI	16.7		10.0		6.2	
556 BPI NRZI	24.0		14.4		9.0	
200 BPI NRZI	66.7		40.0		25.0	
Passing Times, IBG (ms):						
6250 BPI		4.0		2.4		1.5
9-track (PE and NRZI)	8.0	8.0	4.8	4.8	3.0	3.0
7-track (NRZI)	10.0		6.0		3.75	
Rewind Time (2400-foot reel)	60	60	60	60	45	45
Rewind/Unload Time:						
(2400-foot reel) (sec)	66	66	66	66	51	51
Load Operation, approximate time (in sec.) to 'tape unit ready' (after reel/cartridge is mounted and LOAD/REWIND is pressed)	10	10	10	10	7	7

* Read access time is the interval from initiation of a Forward Read command given to the tape control when tape is not at load point, until the first data byte is read when tape is brought up to speed from stopped status.

Write access time is the interval from the issuance of a Move command given to the tape unit when tape is not at load point, until the first data byte is written on tape when tape is brought up to speed from stopped status.

** Start time is the interval from the issuance of a Move command to the tape unit, until tape attains 90% of specified velocity.

3803 MODEL 2 TAPE CONTROL

The 3803 Model 2 Tape Control connects to the I/O interface of an IBM System/360 Model 50 and above (by RPQ only) or an IBM System/370, Model 135 and above. The tape control has a CE panel, two microprogram control sections, a read section, a write section, and a channel buffer section.

Note: "I/O Interface" refers to a set of lines over which the tape control and system channel exchange control and data signals. Interface lines and operations are described in *IBM System/360 and System/370 I/O Interface, Channel to Control Unit, Original Equipment Manufacturers' Information*, Order Number GA22-6974. The 3803 may exceed an interface signal sequence of 32 microseconds, and may produce a worst case interface signal sequence of up to 50 microseconds on some instructions when in seven-track mode with the two-channel switch feature installed.

The 3803 Model 2 operates at 6250 or 1600 bpi. The 3803 Model 2 with appropriate features can process nine-track, 800 bpi NRZI and seven-track, 200/556/800 bpi NRZI tape when used with 3420 Model 3, 5, and 7 tape units having the companion NRZI features.

All data transfers are in burst mode. The tape control executes one command on one tape unit at a time. The tape control parity checks each data byte transferred between the system and a tape unit. On write operations, bus out parity is checked and parity is generated, if necessary, before the byte is sent to the tape unit. On read operations, tape control parity is checked and generated, if necessary, before the byte is placed on the I/O interface. On sense operations, correct parity is supplied for each byte. Parity is also checked on command bytes.

I/O commands issued by the channel are executed with microprograms resident in two independent read-only storage (ROS) units. One ROS unit controls communication lines to the channel, while the other ROS unit controls communication lines to the tape unit.

ADDRESSING

Every tape unit has a unique device address, which consists of a channel address, a tape control address, and a tape unit address. Pluggable jumpers assign the tape control address when the system is installed. The tape control has separate device interface connectors for each tape unit address. A tape unit's address is determined by the tape control connector to which it is attached. There is no address decoding at the tape unit or device interface level.

METERING

A usage meter is installed in the tape control and in each tape unit. The tape control's usage meter records elapsed time whenever the METERING OUT line is active and the tape control is in online status (Enabled). A tape unit's usage meter records elapsed time when the tape control METERING OUT line is active, tape unit is loaded, and the tape is not at load point. METERING IN is used by the central processing unit (CPU) metering circuits; this line is active from the time a command is accepted by the tape control until Device End is generated for that command. See *IBM System/360 and System/370 I/O Interface: Channel to Control Unit OEMI*, Order Number GA22-6974.

ENABLE/DISABLE SWITCH

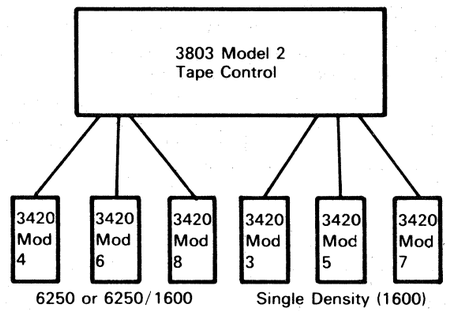
This switch allows the tape control and all attached tape units to be put online or taken offline so a customer engineer can use the CE panel switches and indicators to diagnose errors. Whenever the tape control is placed in offline status (Disabled), the usage meters in the tape control and all attached tape units are prevented from running. When the two-channel switch feature is installed, a second Enable/Disable switch is provided on the 3803.

POWER ON/OFF SEQUENCING

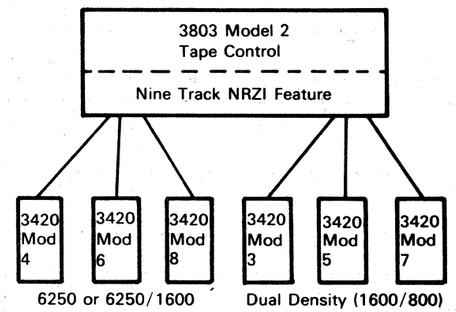
Normal power on/power off sequencing for the 3803-2/3420 tape subsystem is controlled by system power interlock circuits. Maintenance activities may necessitate dropping power in the tape control and attached tape units while power remains on in the system. To take the subsystem offline, see 12-010.

3803-2/3420 CONFIGURATIONS

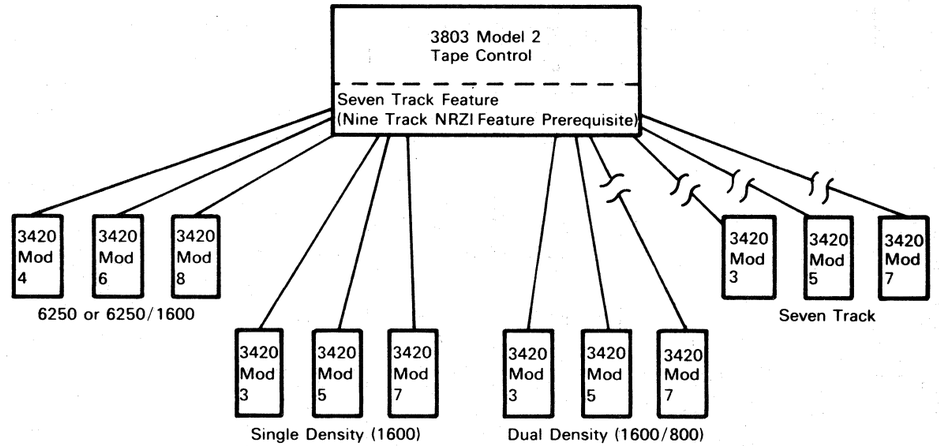
Operation with Model 4/6/8 Tape Units (6250 or 1600 bpi Mode and Models 3/5/7 1600 bpi Tape Units



Operation with Model 4/6/8 Tape Units (6250 or 1600 bpi Mode) and Model 3/5/7 Tape Units (1600 bpi PE and 800 NRZI Modes)



Operation with 3420 Model 4/6/8 Tape Units (6250 or 6250/1600 bpi Modes) and Nine and Seven Track Tape Units (Nine Track 1600 bpi PE and Nine Track 1600/800 bpi and Seven Track 200/556/800 bpi NRZI Modes)



MAXIMUM OF 8 TAPE UNITS PER TAPE CONTROL

For 3420 Model 8 Power Requirements, see 90-180.

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3803 MODEL 2 FEATURES

Features available on a 3803 Model 2 are nine-track NRZI, seven-track (NRZI), two-channel switch, and device switch. For switch feature descriptions, see Section 58-005 through 58-111.

NINE-TRACK NRZI

The nine-track NRZI feature, available on the 3803 Model 2, permits operation in nine-track NRZI mode. Nine-track NRZI operation requires a 3420 Model 3, 5, or 7 Tape Unit with the dual density feature.

SEVEN-TRACK NRZI

The seven-track feature permits operation in seven-track NRZI mode. Seven-track operation with a 3803 Model 2 is at 800/556/200 bpi. The seven-track feature contains both the data translator and data converter for seven-track operations. The operation is similar to that of the 3803-1 with the seven-track feature. For seven-track operation, the seven-track feature on a 3420 Model 3, 5, or 7 and on the 3803 Model 2 is required. The nine-track NRZI feature is a prerequisite for the seven-track feature on the 3803 Model 2.

Writing a tape with the translator on causes eight-bit bytes from the I/O interface to be written on tape as six-bit BCD characters; reading such a tape causes six-bit BCD characters to be translated into their EBCDIC equivalents. When using the translator, data rates are not changed and there are no changes in the tape unit's operation.

Writing a tape with the data converter on causes four tape characters (24 data bits) to be written for every three storage bytes (24 data bits); reading such a tape reverses the process by converting four tape characters into three storage bytes. When operating with the data converter on, the data transfer rate is 75 percent of the rate with data converter off.

DENSITY FEATURE COMBINATIONS

Density (bpi) (Note 1)	3803-1	3803-2	3420-3/5/7 (Note 2)	3420-4/6/8 (Note 3)
6250, 9-Track	Not Applicable	Standard	Not Applicable	6250 Feature
1600, 9-Track	Standard	Standard	1600 Feature	6250/1600 Feature
800, 9-Track	Dual Density Feature	9-Track NRZI Feature	Dual Density Feature	Not Applicable
800, 7-Track	7-Track Feature	7-Track Feature (Note 4)	7-Track Feature	Not Applicable
556, 7-Track	7-Track Feature	7-Track Feature (Note 4)	7-Track Feature	Not Applicable
200, 7-Track	RPQ only	7-Track Feature (Note 4)	7-Track Feature	Not Applicable

Notes:

1. Density must be specified for each 9-track 3420 tape unit.
2. 3420-3/5/7 can be operated by a 3803-1 or 3803-2.
3. 3420-4/6/8 can be operated by a 3803-2 only.
4. 9-track NRZI feature is a prerequisite for 7-track feature on 3803-2.

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COMMANDS AND INSTRUCTIONS

COMMANDS

Commands executed by this subsystem fall into one of the following three categories:

1. Burst Commands
2. Motion Control Commands
3. Non-Motion Control Commands

The table on this page and the one on 40-008 list the subsystem commands and command codes. Commands not listed will set COMMAND REJECT.

Programming Note: The 3803/3420 subsystem has no interlocking to prevent improper sequencing of write- and read-type operations that may result in writing extraneous bits or leaving partial blocks on tape. Avoiding these improper sequences is a program responsibility.

Avoid the following two basic sequences:

1. A write-type operation after a forward read-type operation **except**:

   a. When the block or Tape Mark (TM) read is known to be followed by a TM. A tape mark is a special block used to separate files.

   b. When the block or TM read is known to have been followed by erase record gap (ERG) or is known to have been the last block written before a backward operation.

   For example: **R R W* avoid.**
   W B R W* allowed.

2. A read forward-type operation following write-type operations.

   For example: **R B W R* avoid.**
   W B R R* avoid.

   W indicates a write-type operation: write, write TM, or (ERG).

   R indicates a forward read-type operation: read forward, forward space block, or forward space file.

   B indicates a backward read-type operation: read backward, backspace block, or backspace file.

   * indicates the logical record on which problems may occur.

Because it may be difficult or impossible to ensure the above safe situations, a write after read forward sequence should be used only in applications where strict control of format and command sequence exists.

Write is allowable following a backspace. Assume the following tape format with labels where * is used to denote a TM:

VOL HDR * DATA SET * EOF * HDR * DATA SET * EOF **

A rewrite of the last data set involves the following safe and proper sequence. After processing the next to last end of file (EOF) and TM, read foward to verify the header (HDR) label of the last data set, backspace, write a new HDR, and rewrite the data set. If a new data set is being added, the read forward verifies the second consecutive TM, and thus, the true end of a data set on this tape. A backspace, write new HDR, etc., completes the sequence.

Burst Commands	Command Byte 0	1	2	3	4	5	6	7	Hex
Write	0	0	0	0	0	0	0	1	01
Read Forward	0	0	0	0	0	0	1	0	02
Read Backward	0	0	0	0	1	1	0	0	0C
Sense	0	0	0	0	0	1	0	0	04
Sense Reserve	1	1	1	1	0	1	0	0	F4
Sense Release	1	1	0	1	0	1	0	0	D4
Request Track-In-Error	0	0	0	1	1	0	1	1	1B
Loop Write-To-Read	1	0	0	0	1	0	1	1	8B
Set Diagnose	0	1	0	0	1	0	1	1	4B

Motion Control Commands	Command Byte 0	1	2	3	4	5	6	7	Hex
Rewind	0	0	0	0	0	1	1	1	07
Rewind Unload	0	0	0	0	1	1	1	1	0F
Erase Gap	0	0	0	1	0	1	1	1	17
Write Tape Mark	0	0	0	1	1	1	1	1	1F
Backspace Block	0	0	1	0	0	1	1	1	27
Backspace File	0	0	1	0	1	1	1	1	2F
Forward Space Block	0	0	1	1	0	1	1	1	37
Forward Space File	0	0	1	1	1	1	1	1	3F
Data Security Erase	1	0	0	1	0	1	1	1	97

Non-Motion Control Commands	Command Byte 0	1	2	3	4	5	6	7	Hex
No-Operation	0	0	0	0	0	0	1	1	03
Diagnostic Mode Set	0	0	0	0	1	0	1	1	0B
Mode Set 1	See 40-008								
Mode Set 2	See 40-008								

BURST COMMANDS

Burst commands transfer data across the channel/tape control interface. Channel End and Device End are signaled when the operation is complete (ending status).

The burst commands are:

Write
Read Forward
Read Backward
Sense
Sense Reserve
Sense Release
Request Track-In-Error
Loop Write-To-Read (maintenance aid*)
Set Diagnose (maintenance aid*)

* Diagnostic programs issue maintenance aid commands via start I/Os (SIOs) that are op-codes in the Channel Command Word (CCW).

WRITE

Write records data on tape as it moves forward and creates an interblock gap (IBG) at the end of each block. The tape control checks the parity of each data byte received from the I/O interface.

READ FORWARD

Read Forward sets the tape unit to forward read status. As the tape moves, data is read until the read head detects the next IBG. The tape control checks and, if necessary and possible, corrects the bits of each byte transferred to the I/O interface. Sensing a tape mark sets Unit Exception with Channel End and Device End in the Unit Status byte.

READ BACKWARD

Read Backward sets the tape unit to backward read status. The operation of the command is similar to Read Forward, except that the 7-track NRZI data converter mode cannot be used. Data flow and controls are the same as in Read Forward. A Read Backward, given at load point or into load point, sets Unit Check. The tape unit remains in backward status at the end of a Read Backward command.

SENSE

Sense transfers the sense bytes to channel. There are 24 bytes of sense data available. The CCW specifies the number of sense bytes to be transferred and the starting storage address. The information transferred includes unusual conditions associated with the last operation and provides details about the current conditions present in the tape control and tape unit. A sense command addressed to a tape unit that is not ready will be executed.

SENSE RESERVE

Sense Reserve reserves the addressed tape control for the channel issuing this command. The tape control will remain reserved for the channel until either:

- A Sense Release command is issued from the reserving channel, or
- A system reset occurs.

Attempting to select a tape control that is reserved to another channel results in a Control Unit Busy indication. The Sense Reserve command should only be issued by the Control Program.

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SENSE RELEASE

Sense Release releases the reserved tape control so it is available to either channel. The Sense Release command should only be issued by the control program.

Programming Note: Sense Reserve and Sense Release commands can only be used on subsystems having the two-channel switch feature. If these commands are issued to a tape control without this feature, COMMAND REJECT results. When using these commands, they must be the first command in a chain or COMMAND REJECT results.

The Sense Reserve and Sense Release commands are not supported by IBM Operating Systems.

REQUEST TRACK-IN-ERROR (REQUEST TIE)

Request TIE returns to the tape control a data byte containing track-in-error information for 9-track and sensing level information for 7-track tape units. This information is transmitted to the channel in sense byte 2 on a Sense command following a Read, Read Backward, Write, or Loop Write to Read command.

When issued following a 6250 bpi or PE operation, Request TIE is treated as a No Operation (NOP Reset Sense.

When issued following a 9-track NRZI read operation, a Request TIE either:

- Enables the tape control to perform a correction read operation if the data byte contains a single bit, or
- Does not enable the tape control to perform a correction read operation if the data byte contains bits 6 and 7, which indicate an uncorrectable error.

When issued following a 7-track read operation, the Request TIE byte controls the read clipping level in the following sequence:

Second attempt—Middle Level
Third attempt—Low Level
Fourth attempt—High Level

Clipping levels are cyclically altered in this way as long as read attempts result in Vertical Redundancy Check (VRC) errors.

LOOP WRITE-TO-READ (LWR)

Loop Write-to-Read checks the tape control and tape unit data and control paths without moving tape. In 6250 or 1600 bpi mode, LWR writes and error checks the record. In NRZI mode, LWR writes the record but checks only for Write Trigger VRC errors. Read errors will occur during the NRZI operation but will be reset by ALU2 when the LWR operation is completed.

On 9-track 3420 tape units, a LWR command issued at beginning-of-tape (BOT) is executed in 1600 bpi mode. Elsewhere on tape, LWR is executed in the current operating mode of the tape unit.

LWR does not require the tape unit to be in write status, but the tape unit must be ready. Execution of an LWR does not change the status of the tape unit. An LWR performed from the processing unit uses the same data path as a Write command.

SET DIAGNOSE '4B'

Set Diagnose is used to call microdiagnostic routines. Bytes are transferred from channel to the tape control to modify the operation of succeeding commands in the chain.

FLAG BYTE 1

Bit	Write	Read
0	Diagnostic Write	N/A
1	N/A	IBG Measure
2	Inhibit Postamble	Read Access
3	Var Go-down Time	Var Go-down Time
4	Inhibit Preamble	N/A
5	LWR	DMR
6	TUBO Mask	N/A
7	Change Direction	Change Direction

Diagnostic Write

Performs the same function as the 'OB' command.

PE - causes writing to be inhibited in any track when the write data contains successive one bits.

NRZI - 9 track - Inhibits writing P bits.
7 track - Inhibits writing C bits.

Inhibit Postamble

Prevents writing the last 39 zeros of the postamble. The ending all-ones marker and the first zero is written.

Variable Go-down Time

Two bytes (flag bytes 3 and 4) are sent to the tape control unit. These bytes are used to control the wait time before starting the next operation in the chain following the Set Diagnostic (48) command.

Count values are:

103.15 Microseconds to decrement one count.

27 Milliseconds to decrement the low order counter 256 ('FF') counts and cause one decrement of the high order count.

Inhibit Preamble

Prevents writing the first 39 zeros of the preamble. The last (40th) zero and the beginning all-ones marker is written.

Loop Write-To-Read

Write data is sent to the tape unit. In the MST board it is gated to the read circuits and then returned to the tape control unit for read checking.

Set TUBO Mask

Flag byte 3 is used as a mask to control the tape unit Bus Out. Any bit on in flag byte 3 causes that tape unit Bus Out bit to be held active, and thus prevents the tape unit from writing data for that specific bit.

Change Direction

Change Direction allows the following word (CCW) chain to progress through turnaround, if necessary, and up to the point of activating the Move line to the tape unit. At this point, the operation is terminated. The tape unit is left in forward or backward, write or read status, depending on the operation follow the Change Direction instruction.

FLAG BYTE 2

Bit	Description
0	Block Data Check
1	N/A
2	Block Interrupts
3	Force Control Unit Busy
4-7	N/A

FLAG BYTE 3 (OPTIONS)

DMR Go-Up Time in tack pulses

GDT Hi order byte of go-down count

TUBO Mask Byte used to mask TU Bus Out

FLAG BYTE 4 (OPTIONS)

DMR Go-down time measure count equivalent to tach pulses. No tach pulse when tape is not moving.

GDT Lo order byte of go-down count.

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MOTION CONTROL COMMANDS

Motion control commands move tape but do not transfer information across the channel/tape control interface.

All motion control commands operate as follows:

1. Channel End is signaled when the command is accepted (initial status).
2. For commands other than Rewind/Unload, device end is signaled when the operation is completed (ending status).
3. The tape control responds with BUSY if the tape control is addressed while executing the command. As a result, the 3803 is obligated to present a CUE interrupt to the channel that received the BUSY as soon as the current operation is complete.

Note: For Rewind/Unload, Channel End is signaled in initial status, and Device End, Control Unit End, and Unit Check are signaled in an interrupt status cycle after the command becomes effective at the tape unit. Device End is signaled again when the operator reloads tape, presses START, and the tape unit goes from not-ready to ready providing the tape control has not been offline in the interim.

Motion control commands are:

Rewind
Rewind/Unload
Erase Gap
Write Tape Mark
Backspace Block
Backspace File
Forward Space Block
Forward Space File
Data Security Erase

REWIND (REW)

Rewind causes the selected tape unit to rewind tape to load point.

REWIND UNLOAD (RUN)

Rewind Unload causes the selected tape unit to rewind tape to load point, removes tape from the columns, finishes winding tape onto the right reel, closes the cartridge (if used), and opens the window.

ERASE RECORD GAP (ERG)

Erase Record Gap causes the selected tape unit to move tape forward and erase tape as follows:

	Single ERG	Successive ERGs
6250 bpi	3.75 in. (95,3 mm)	3.45 in. (87,6 mm)
1600 bpi and 800 bpi 9-track	4.2 in. (106,7 mm)	3.6 in. (91,4 mm)
7-track	4.5 in. (114,3 mm)	3.75 in. (95,3 mm)

WRITE TAPE MARK (WTM)

Write Tape Mark causes the selected tape unit to move tape forward and write a tape mark block.

At 6250 and 1600 bpi, a WTM causes the subsystem to write a tape mark preceded by an Erase record gap.

Data Check, Equipment Check, and Unit Check can be set during a Write Tape Mark (WTM) operation.

Attempting to write a tape mark on a file-protected tape unit sets COMMAND REJECT.

BACKSPACE BLOCK (BSB)

Backspace Block causes tape to move backward to the next interblock gap or to load point, whichever comes first. No data bytes are transferred. Channel End is signaled when the command is accepted. Device End is signaled at the next interblock gap or load point. Sensing a tape mark sets Unit Exception, with Device End in the status byte. Backspacing into or at load point sets Unit Check with Device End in the status byte. The tape unit remains in backward status.

BACKSPACE FILE (BSF)

Backspace File causes the selected tape unit to move tape backward to the interblock gap on the load point side of a tape mark, or to load point, whichever comes first. No data bytes are transferred. Unit Exception is not set when tape mark is sensed.

Backspacing into or at load point sets Unit Check with Device End in the status byte. Device End is signaled at the completion of the operation. The tape unit remains in backward status.

FORWARD SPACE BLOCK (FSB)

Forward Space Block causes the selected tape unit to move tape forward to the next interblock gap. Initial status contains Channel End. Sensing a tape mark sets Unit Exception, with Device End in the status byte.

FORWARD SPACE FILE (FSF)

Forward Space File causes the selected tape unit to move tape forward to the interblock gap beyond the next tape mark. No data bytes are transferred. Initial status contains Channel End. Device End is signaled at the completion of the operation. Sensing the tape mark does not set the Unit Exception bit.

Programming Note: The tape control responds with a Control Unit Busy sequence while performing an ERG, WTM, BSB, BSF, FSB, or FSF operation.

DATA SECURITY ERASE (DSE)

Data Security Erase causes the selected tape unit to erase tape from the point at which the operation is initiated until the end-of-tape marker is sensed.

The DSE command is accepted by the tape control only when chained immediately following an Erase Gap command. Receipt of this command under any other condition results in COMMAND REJECT. If the command is accepted, initial status contains Channel End, and Device End is signaled when the operation is complete. An attempt to erase a file-protected tape sets COMMAND REJECT. Unit Exception never occurs as a result of this command. Data Security Erase at end of tape (EOT) causes an immediate ending sequence. The tape control does not remain busy after initial selection. An attempt to select the tape unit while executing a DSE results in busy status.

During DSE execution, the tape unit monitors erase head current to ensure that tape is erased. If erase head failure is detected, the operation is terminated by dropping TAPE UNIT READY. Device End and Unit Check are issued as a result of dropping READY. At the completion of a DSE, the tape control presents Device End to channel.

Programming Note: If the tape unit drops ready or fails logically during DSE, the ending status containing Device End and sense byte 7, bit 4 (Erase Head Failure) is also set.

Device End is signaled when the EOT marker is sensed during a normal DSE completion. However, a sense command should be performed to assure EOT was reached. Upon completion of the DSE, the operating program must issue sufficient erase gap commands to ensure erasure of any data written beyond the EOT marker. Issuing 14 erase gap commands, which erases about 4 feet (1,22m) of tape, is generally sufficient. The channel must be enabled for interrupts to detect a Unit Check condition due to manual intervention. When Device End is signaled, a sense command should be performed to ensure the tape unit reached EOT.

The Data Security Erase command is not currently supported by IBM Operating Systems. DOS supports DSE via a Magnetic Tape Command (MTC).

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NON-MOTION CONTROL COMMANDS

Non-motion control commands do not move tape and do not transfer data across the channel/tape control interface.

Channel End and Device End are signaled when non-motion control commands are accepted (initial status).

Non-motion control commands are:

No-Operation
Mode Set 1
Mode Set 2
Diagnostic Mode Set (maintenance aid)

NO-OPERATION (NOP)

NOP performs no function in the tape control or tape unit, and does not transmit data or move tape. NOP does not reset tape control sense data.

Programming Note: Placing a NOP command at the end of a series of chained commands delays channel disconnect from the tape control until the NOP is executed. Indiscriminate use of this command delays the channel program, and may contribute to a channel overload condition.

MODE SET 1 (MS 1)

Mode Set 1 commands sent to tape controls with the 7-track NRZI feature establish an operating mode for succeeding 7-track NRZI operations. Bits 0 and 1 control density (200/556/800 bpi) and bits 2, 3, and 4 control parity (odd or even), data converter (on or off), and translator (on or off) circuits in the tape control. See chart on this page.

A Mode Set 1 command affects operation of all 7-track tape units attached to the tape control. Unless reset, the tape control retains its mode setting until it receives another Mode Set command.

MODE SET 2 (MS 2)

Mode Set 2 commands sent to a 3803 Model 2, set the operating mode for succeeding write-type operations. Modes are: 6250 bpi, 1600 bpi PE, or 800 bpi nine-track NRZI. Unless reset, the tape control retains its mode setting until it receives another Mode Set command.

DIAGNOSTIC MODE SET (DMS)

DMS causes an artificial signal-loss condition that checks read and write error detection circuits.

- At 6250 bpi, track P is made all zeros and the program supplies the error correcting code as part of the data.
- At 6250 bpi Diagnostic Read inhibits single- and double-track error corr check characters to channel with data.
- At 1600 bpi, whenever write data contains successive one bits in any track, writing in that track is inhibited until the last one bit is reached.
- In 9-track NRZI mode, no bits are written in track P.
- In 7-track NRZI mode, no bits are written in track C.

A Diagnostic Mode Set command affects only operations for the command chain in which it is issued.

Mode Set Commands

Set Density			Parity		Data Converter		Translator		Command Byte								
200	556	800	Odd	Even	On	Off	On	Off	0	1	2	3	4	5	6	7	Hex
Mode Set 1 (7-Track) (See Note)																	
X			X		X			X	0	0	0	1	0	0	1	1	13
X				X		X		X	0	0	1	0	0	0	1	1	23
X				X		X	X		0	0	1	0	1	0	1	1	2B
X			X			X		X	0	0	1	1	0	0	1	1	33
X			X			X	X		0	0	1	1	1	0	1	1	3B
	X		X		X			X	0	1	0	1	0	0	1	1	53
	X			X		X		X	0	1	1	0	0	0	1	1	63
	X			X		X	X		0	1	1	0	1	0	1	1	6B
	X		X			X		X	0	1	1	1	0	0	1	1	73
	X		X			X	X		0	1	1	1	1	0	1	1	7B
		X	X		X			X	1	0	0	1	0	0	1	1	93
		X		X		X		X	1	0	1	0	0	0	1	1	A3
		X		X		X	X		1	0	1	0	1	0	1	1	AB
		X	X			X		X	1	0	1	1	0	0	1	1	B3
		X	X			X	X		1	0	1	1	1	0	1	1	BB
Mode Set 2 (9-Track)																	
800	**1600**	**6250**															
		X							1	1	0	1	0	0	1	1	D3
	X								1	1	0	0	0	0	1	1	C3
X									1	1	0	0	1	0	1	1	CB

Note: Seven-track Mode Set 1 commands are treated as 'NOP reset sense' when issued to a tape control without the seven-track NRZI compatibility feature.

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I/O INSTRUCTIONS

In addition to initiating one of the I/O operations by means of the Start I/O (SIO) instruction, the program can cause certain actions at the tape control by using the Test I/O and Halt I/O instructions.

TEST I/O

A Test I/O instruction performed by the Central Processing Unit (CPU), causes the status byte for the selected tape unit to be sent to the channel for analysis. No actual operation is performed.

Note: A Test I/O command issued to a not ready tape unit results in a contingent connection on tape control units with the two-channel switch.

HALT I/O

A Halt I/O instruction causes data transfer to stop. The tape control disconnects from the channel and proceeds independently to the completion of the operation. When the operation is completed, the tape control tries to re-establish connection with the channel to transfer ending status. If addressed while completing the operation, the tape control returns a BUSY signal.

If a Halt I/O instruction is executed after STATUS IN and before tape motion is started during a Write or Read operation, the operation is canceled, and Channel End, Device End, Unit Check, and Data Check are generated.

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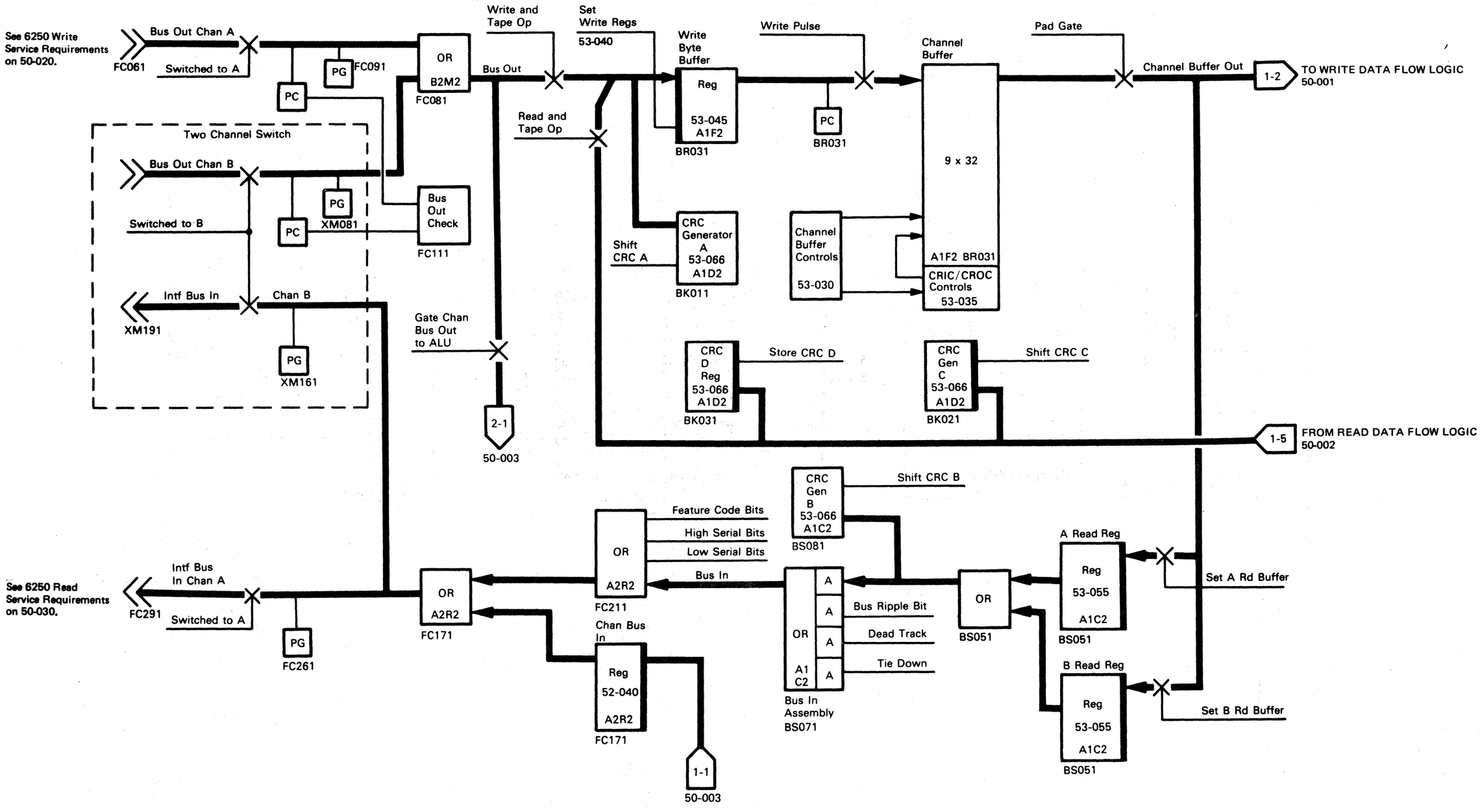
READ/WRITE FLOW LOGIC



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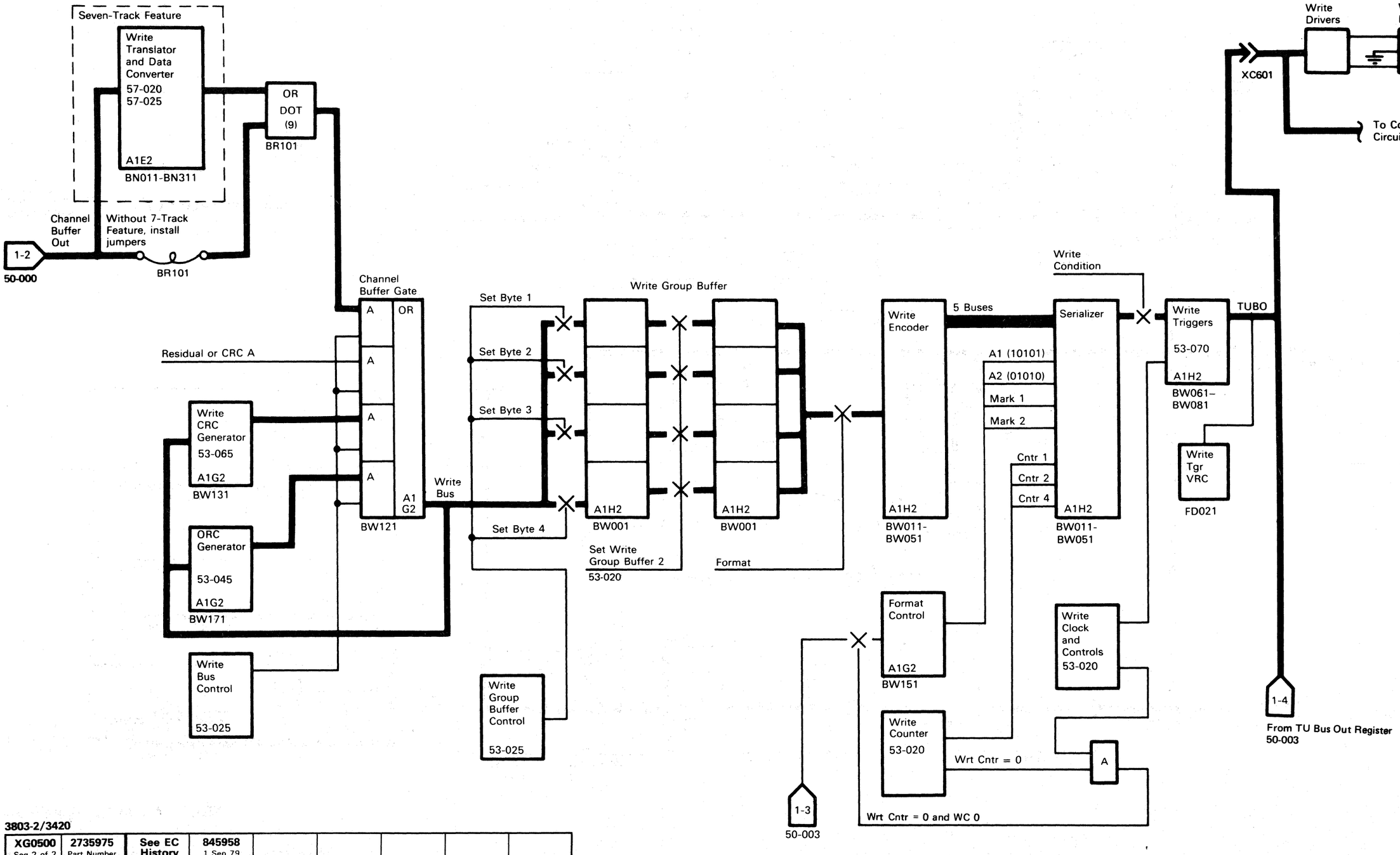
WRITE DATA FLOW LOGIC



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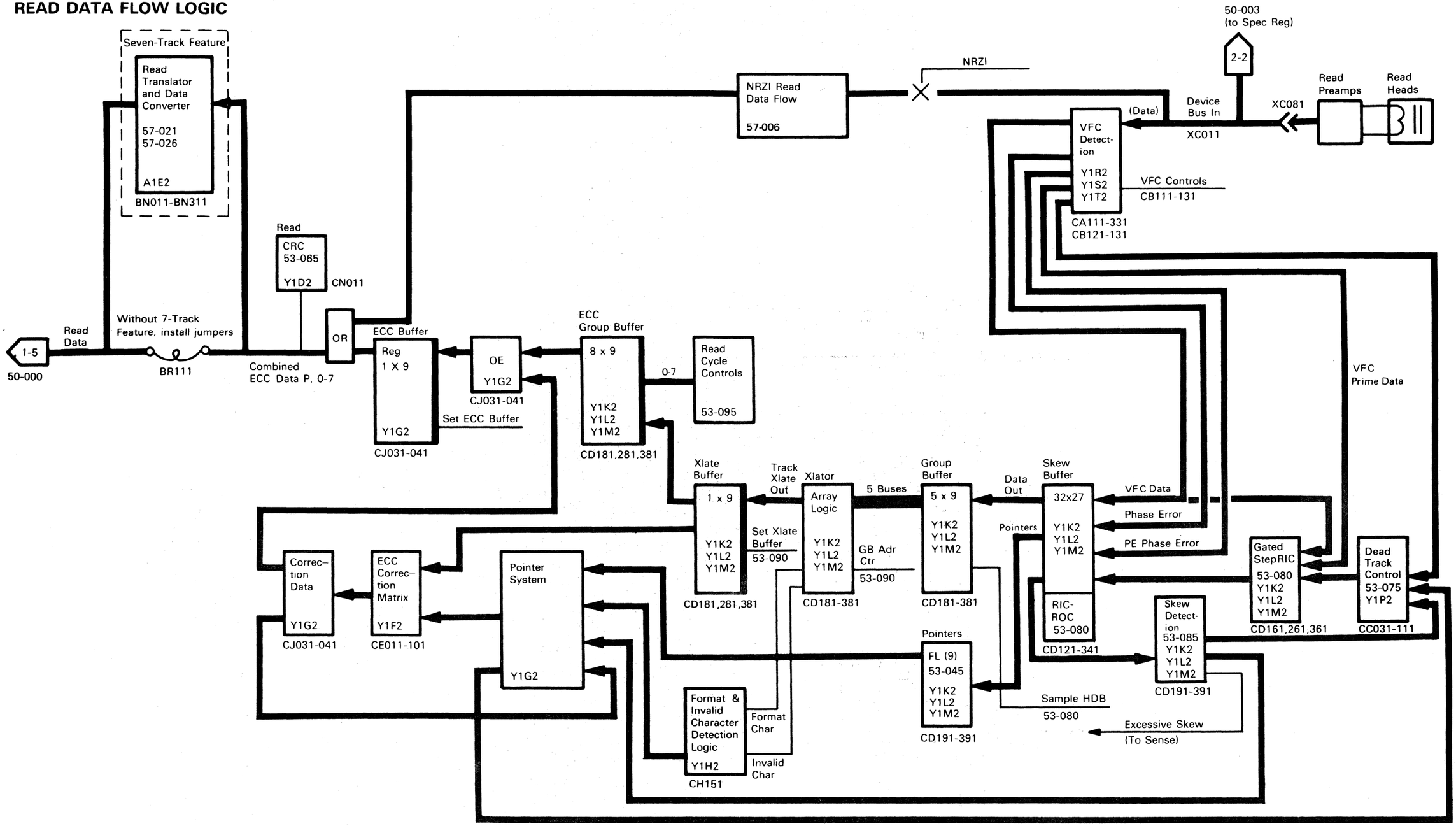
READ DATA FLOW LOGIC



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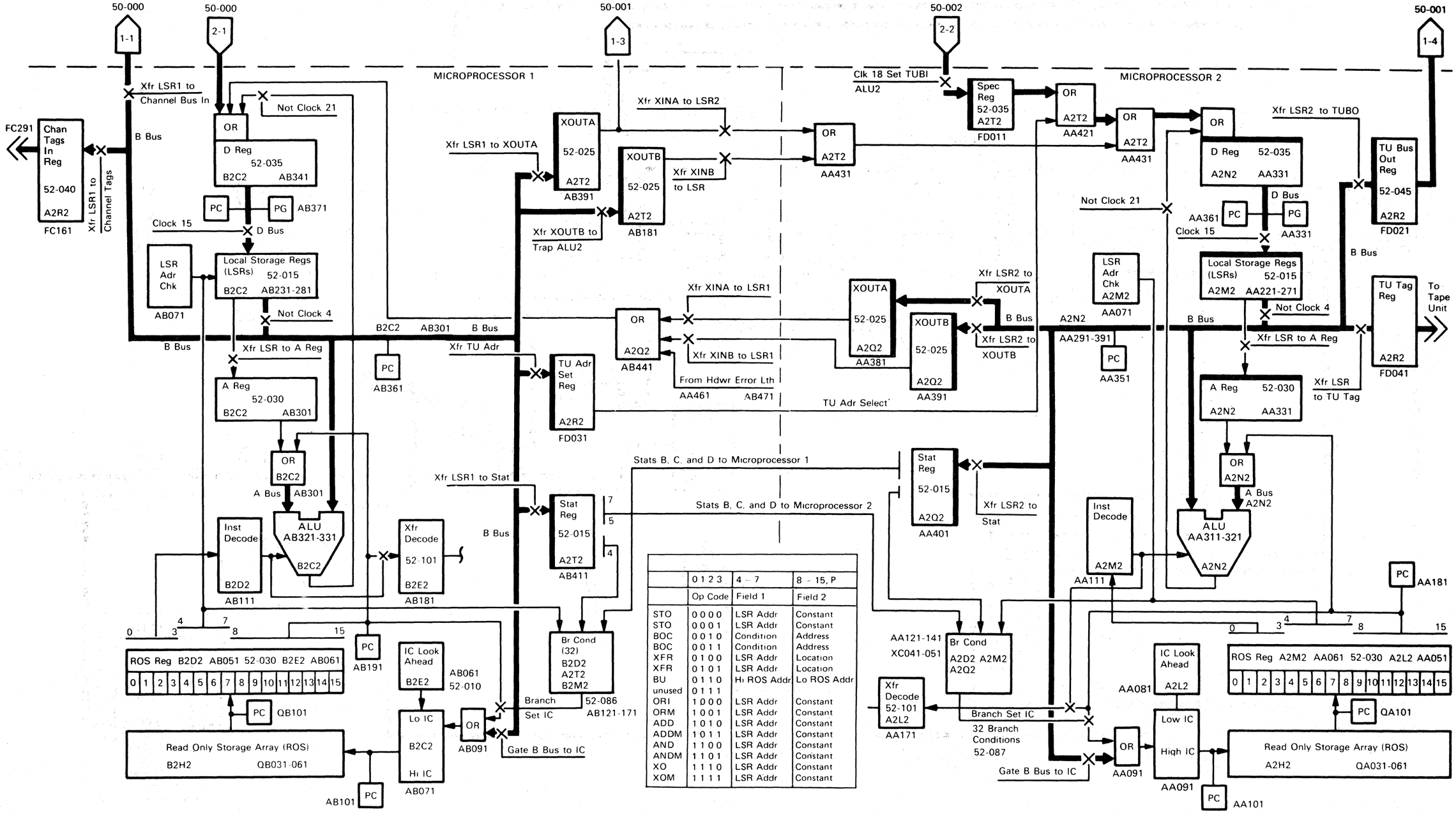
MICROPROCESSORS (MP1/MP2) SCHEMATIC



	0 1 2 3	4 – 7	8 – 15, P
	Op Code	Field 1	Field 2
STO	0 0 0 0	LSR Addr	Constant
STO	0 0 0 1	LSR Addr	Constant
BOC	0 0 1 0	Condition	Address
BOC	0 0 1 1	Condition	Address
XFR	0 1 0 0	LSR Addr	Location
XFR	0 1 0 1	LSR Addr	Location
BU	0 1 1 0	Hi ROS Addr	Lo ROS Addr
unused	0 1 1 1		
ORI	1 0 0 0	LSR Addr	Constant
ORM	1 0 0 1	LSR Addr	Constant
ADD	1 0 1 0	LSR Addr	Constant
ADDM	1 0 1 1	LSR Addr	Constant
AND	1 1 0 0	LSR Addr	Constant
ANDM	1 1 0 1	LSR Addr	Constant
XO	1 1 1 0	LSR Addr	Constant
XOM	1 1 1 1	LSR Addr	Constant

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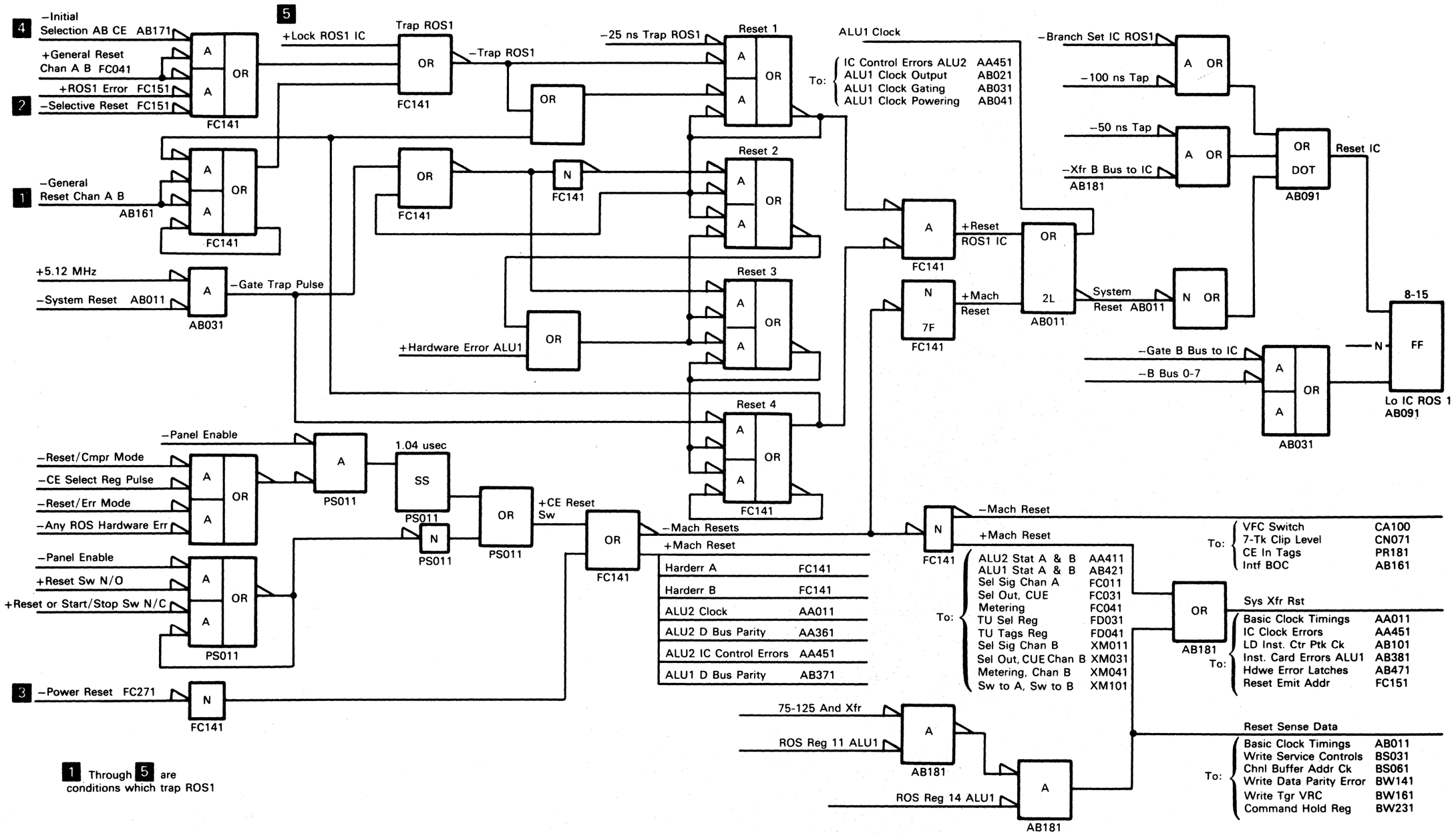
ROS 1 TRAP CONDITIONS



1 Through 5 are conditions which trap ROS1

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ROS 1 TRAP CONDITIONS (Cont'd)

Both hardware and microprograms generate resets. Types of resets are General, Selective, and Machine.

[1] GENERAL RESET resets all flags, stats, and reserve bits that apply to the selecting interface.

[2] SELECTIVE RESET performs the same functions except the Control Unit Reserve and Hold Interface bits are not reset.

[3] POWER ON RESET and CE panel resets generate MACHINE RESET. Turning power on and pressing RESET both generate POWER ON RESET. POWER ON RESET clears some LSRs and initiates INTERFACE CHECKOUT. Channel outbound tags are checked to ensure all are inactive and all inbound tags except OP IN are activated. Contents of the CHANNEL BUS IN register are sent to CHANNEL BUS OUT.

[4] INITIAL SELECTION AB CE traps ROS 1 to 000 at each selection of the tape control.

[5] LOCK ROS 1 IC traps ROS 1 to 000 when an ALU 1 hardware error occurs.

MP2 is activated for the proper reset after Stat B has been set on or off to reset only the selecting interface. CONTROL UNIT BUSY is activated for the duration of the reset and is deactivated at completion of MP2 reset.

If MP2 has hardware errors, the tape control "hangs up" with BUSY active and loops on a trap address.

If all steps are completed correctly, the reset is finished. Any failure "hangs up" the tape control at a trap address and BUSY remains active.

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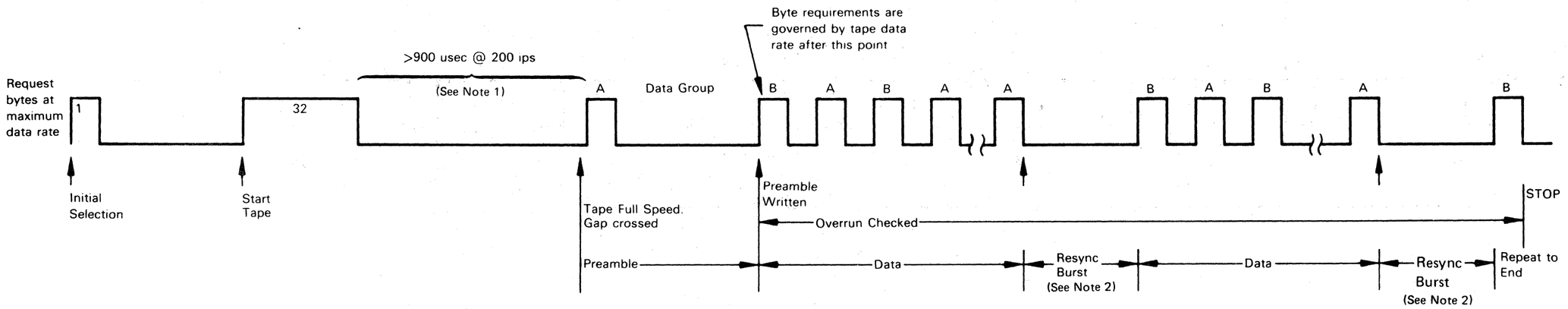
6250 WRITE SERVICE REQUIREMENTS

The write buffers fill automatically at the maximum rate permitted by the control unit, cable, and channel delays. This diagram shows when byte requirements occur. The channel must respond only to the average need during the period of overrun, checking such that at least one ECC (error correction code) group remains in control unit buffers at all times until stop occurs. Note that no individual channel byte transfer is overrun checked.

36 bytes are pre-buffered and one ECC group or more must remain in the buffer at all times prior to Stop. This time could permit some data chaining or be considered a safety factor.



Notes:

[1] Proportionately more on lower speed tape units.

[2] The Resync Burst consists of a mark 1 group, 2 sync groups, and a mark 2 group. It is interleaved in a block of data after every 158 data groups, and is used to re-synchronize the read circuits during a 6250 read operation.

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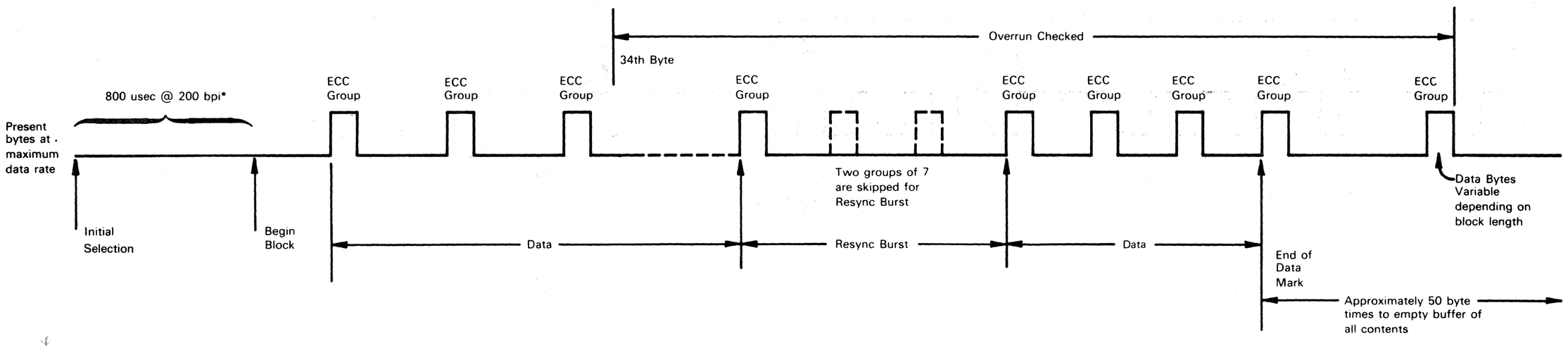
6250 READ SERVICE REQUIREMENTS

The channel buffer and both read byte buffers are empty at the start. Overrun is called only if there is insufficient room in the buffer for a waiting ECC group. The ECC rate varies according to corrections required but follows the tape rate average over periods of 50 bytes or more. The channel has until the postamble end to accept all data from the buffer. Note that no individual data transfer is checked for overrun. To overrun, the buffer fills during a channel lag.

There is excess read buffer capacity equivalent to 10 usec* available for "slip" or possible data chaining. The time may be distributed or lumped. Overrun check effectively starts at the 34th byte since that is the total buffer capacity.



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MICROPROCESSOR CLOCKS CONTROL LOGIC

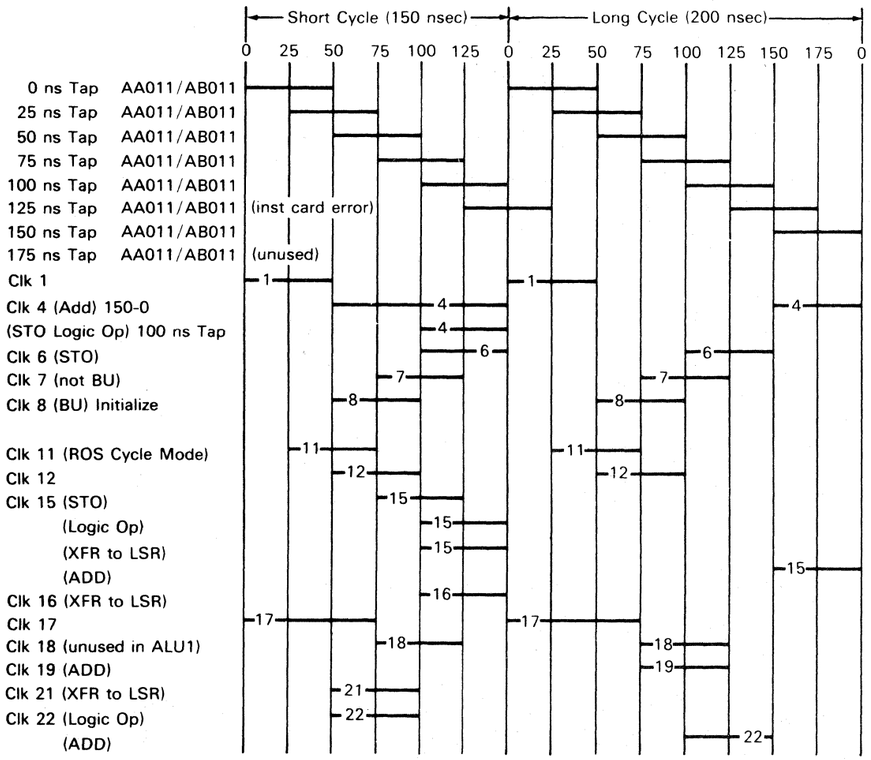
Hardware clocks control both microprocessors (MP1 and MP2). The clocks are stepped by 20.48-MHz pulses.

The MP2 clock is similar to the MP1 clock shown.

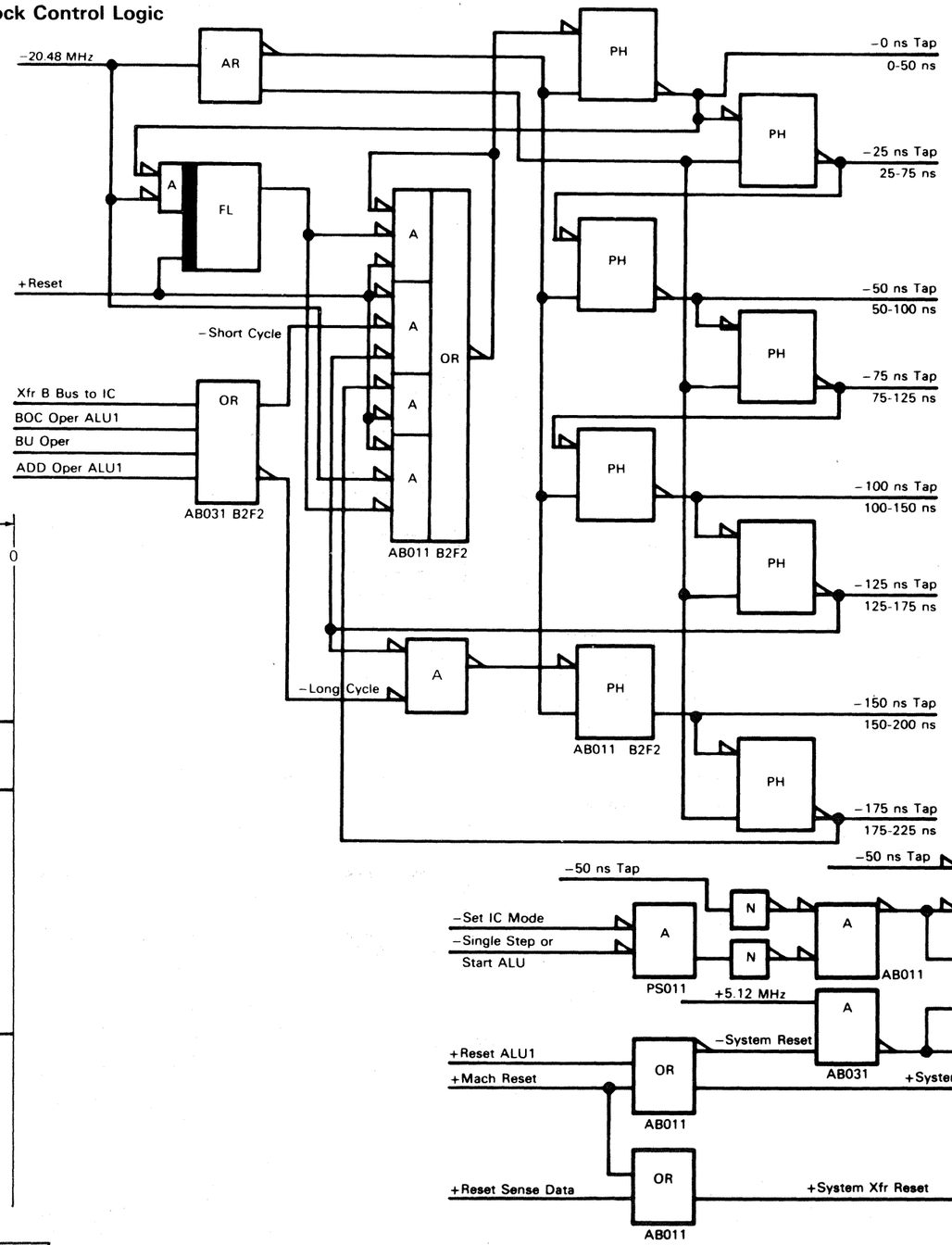
The clocks run on either 150- or 200-nanosecond cycles. The length of the cycle depends on the instruction.

The numbers on the clock outputs (CLK1—CLK22) bear no relationship to the times these lines become active within the clock cycle.

Clock Timing Chart



MP1 Clock Control Logic



3803-2/3420

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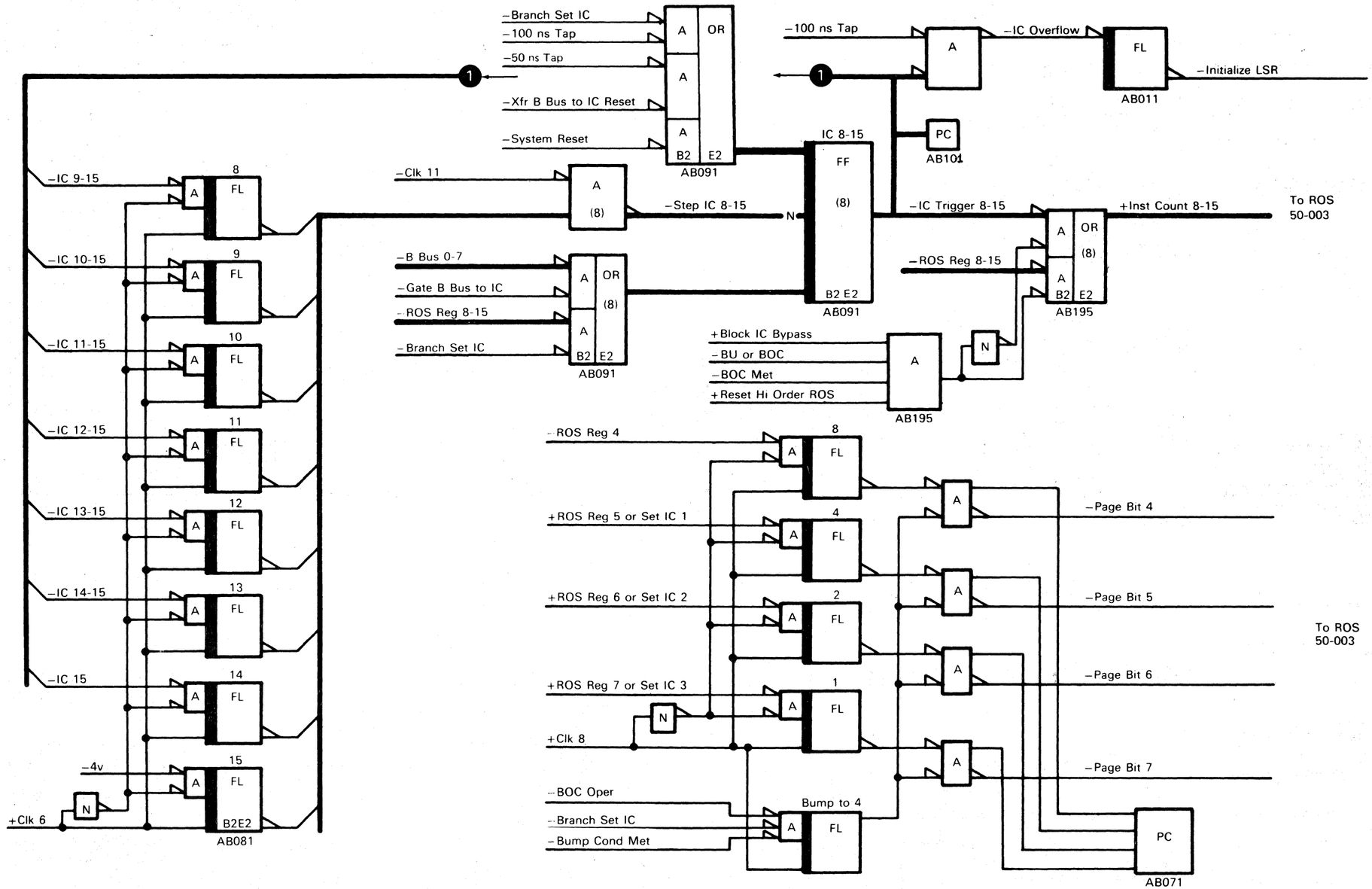
MICROPROCESSOR 1 INSTRUCTION COUNTER (IC)

MP2 IC is similar on:

ALD AA071, 081, 091
Cards A2L2, A2M2



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LOCAL STORAGE REGISTERS

The Local Storage Registers (LSRs) serve as buffers to hold command codes, addresses, error conditions, and any other data the microprocessors use. Each microprocessor has 32 Local Storage Registers. Each register holds one byte (8 bits) of data and a parity bit. The registers are numbered LSR 0 through LSR 31.

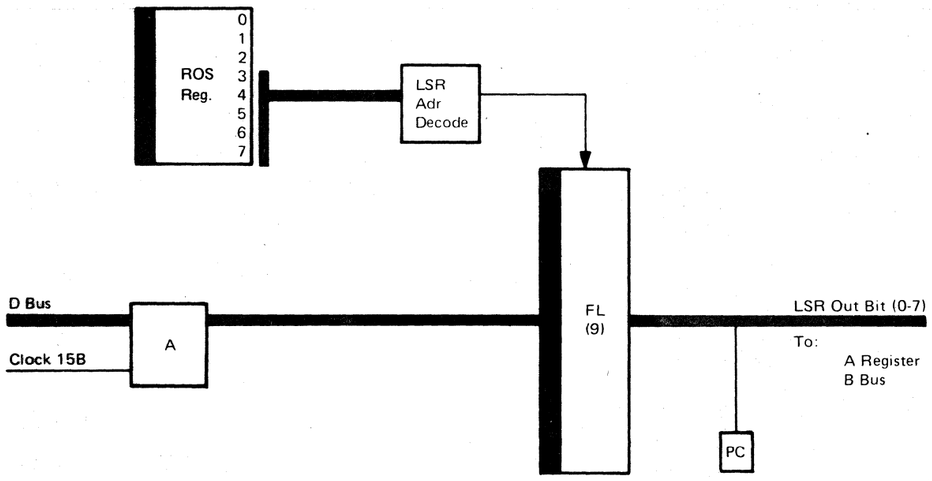
Data from the D Register is stored in the LSRs, and the output from the LSRs goes to the A Register and the B Bus.

Microprogram instructions gate the contents of the LSRs to other registers.

When the LSRs are used, Field 1 of the microprogram instruction addresses a specific register.

The procedure on page 12-012 displays contents of local storage registers.

ROS/LSR Logic



	MP1 ALD	MP1 Card	MP2 ALD	MP2 Card
LSRs	AB231	B2C2	AA221	A2N2
LSR Decode	AB201	B2D2	AA191	A2N2
Address Decode	AB071	B2D2	AA071	A2N2
Parity Check	AB361	B2C2	AA351	A2N2

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STAT REGISTERS

STAT registers are used for microprocessor to microprocessor communication and for microprocessor to data flow communication.

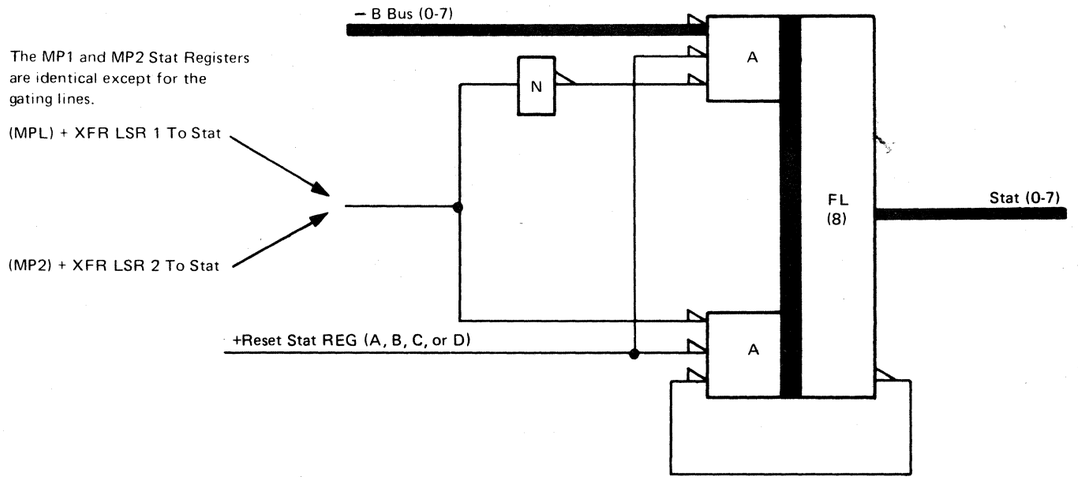
MP1 Stat Register Usage

MP1 Stat	
0	Stop
1	Sense
2	Sense II
3	Diag. Mode
4	Stat A
5	Stat B
6	Stat C
7	Stat D

MP2 Stat Register Usage

MP2 Stat	
0	Tape Op
1	Start R/W
2	Wr ID
3	7 Trk
4	Stat A
5	Stat B
6	Stat C
7	Stat D

MP1/MP2 Stat Registers



MP1 ALD	MP1 Card	MP2 ALD	MP2 Card
AB411	A2T2	AA401	A2Q2

CROSSOVER (XOUTA/XOUTB) REGISTERS

The MP1 XOUTA Crossover Register is both a buffer for MP1 control information and a transfer register when sending a byte of information to MP2.

The individual bits from XOUTA (XOUTA BIT x) are used for the following:

Bit	Location	Function
0	FC211	Gates unit serial number to Channel.
1	FC211 BW311 BW151	Gates EC level and features data to channel Gates 7-track Mode Sets Generates WRITE END GATE TO DF
2	BN311	Gates 7-track Mode Sets
3	BN311 BW151	Gates 7-track Mode Sets Gates Write Tape Mark
4	BN311 CN031 BW151	Gates 7-track Mode Sets Gates NRZI Track-in-Error Gates WRITE MARK 1
5	CN031 BW151 BN231	Gates NRZI Track-in-Error Gates WRITE MARK 2 Gates WRITE OP TO DF
6	PR161 CN031 BW151	Gates the Sense Bytes to Channel Gates NRZI Track-in-Error Gates WRITE A2
7	PR161 CN031 BW151	Gates Sense Bytes to Channel Gates NRZI Track-in-Error Gates WRITE A1

The contents of XOUTA are gated to MP2 by XFR XINA TO LSR 2 on AA431. Output of XOUTA in MP1 is called XINA in MP2.

MP1 XOUTB crossover register is a transfer register sending a byte of information to MP2. When MP1 XOUTB is used, MP2 traps to address 000. The contents of XOUTA becomes an index to a specific routine in MP2.

The MP2 XOUTA crossover register is both a buffer for MP2 control information and a transfer register when sending a byte of information to MP1.

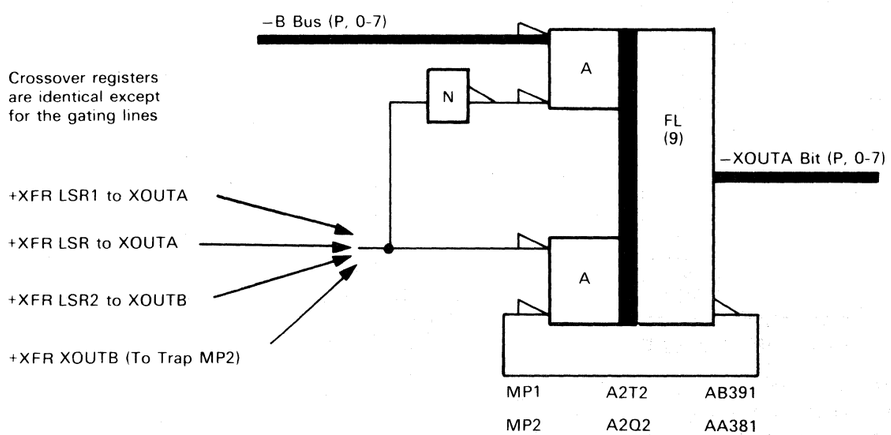
Bits from XOUTA (XOUTA BIT x) are used as follows:

Bit	ALD	Function
0	BW231	Gates PE Mode
1	AA141	Gates forward operation
2	AA141	Allows envelope loss
3	CC021	Gates Sync Mode for Detection
4	BW231	Gates 6250 Mode
5	CB111	Gates Detection Frequency
6	AA141	Gates low gain to read logic
7	CB111	Gates detection frequency

The contents of XOUTA are gated to MP1 by XFR XINA TO LSR 1 on AB441. Output of XOUTA in MP2 is known as XINA in MP1.

The MP2 XOUTB Crossover Register is a transfer register sending a byte of information to MP1. This register is primarily used to send sense bytes from MP2 to MP1 for transfer to channel.

Crossover Register



MP1 XOUTA Register Bit Usage

MP1 XOUTA	Sense Stat On	Dataflow Control	6250 BPI Write	1600 BPI Write	NRZI Write	XFR TIE
P						
0			Format	Format	Format	Any binary combination over 8 will Dead Track only track 0.
1		7-track Mode Set*	End Gate	End Gate	End Gate	
2		7-track Mode Set*				
3		7-track Mode Set*	Tape Mark	Tape Mark		P 0 1 2 3 4 5 6 7
4		7-track Mode Set*	00111	00111		1
5		Write#	11100	11100		1 1 1 1
6	Bin 2	PE	01010			1 1 1 1
7	Bin 1	NRZI	10101			1 1 1 1
	Real Time gating of Sense Bytes	* Bits 1-4 of 7-track Mode Set.				
		# Bits are phase locked in dataflow hardware by rise of TAPE OP to allow use of register for write format.	Strobed into write controls at each group boundary except bit 3 which is real time.			Microprogram encoded.

MP2 XOUTA Bit Usage

MP2 XOUTA	Data Control
P	
0	PE
1	Forward
2	Allow Env. Loss
3	Sync
4	6250
5	Speed
6	Low Gain
7	Speed

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MICROPROCESSOR LISTINGS

Microprocessors 1 and 2 have different listings that can be identified by ALU1 or ALU2 printed in the upper left corner of each page.

Listings are in four parts:

1. General reference information, sense byte descriptions, Local Storage Register layout, branch condition codes, transfer codes, etc.
2. Equate statements which specify a symbolic name for a value. Equate statements are generally followed by a description of the use of the constant.
3. Listing of the executable instructions.
4. Cross reference table containing all symbolic names used in the listing. This table includes the length of the referenced field, its value, the statement number in which it is defined, and the statement number of all instructions using the symbolic name.

COMMUNICATION BETWEEN MICROPROCESSORS

Either microprocessor can move a byte of information from an LSR to either the XOUTA or XOUTB registers. The other microprocessor can then move the byte of information from the XOUTA or XOUTB register to an LSR.

Each microprocessor can test, with Branch On Condition instructions, STAT BITS B, C, and D from the other microprocessor.

LINKING MICROPROGRAM ROUTINES

LINK registers store microprogram addresses for return to a major routine from subroutines. Before branching to a subroutine, the address of a Branch Unconditional instruction is stored in a LINK register. The Branch Unconditional instruction must be in the same page as the subroutine to which the program is branching. When the subroutine has completed its function, the contents of the LINK register are transferred to the Instruction Counter. The microprogram then branches to the Branch Unconditional instruction, which, in turn, branches to the return point in the calling routine.

MP1 has six link registers named LINK1 through LINK6 and MP2 has three LINK registers named LINK1 through LINK3. The LINK registers are local storage registers used for linkage purposes. The specific local storage registers used for linkage are:

LINK	MP1	MP2
LINK1	LSR16	LSR28
LINK2	LSR17	LSR25
LINK3	LSR18	LSR26
LINK4	LSR19	
LINK5	LSR24	
LINK6	LSR25	

Multiple link registers are available because there may be several possible branches out of a subroutine.

MICROPROCESSOR (MP1 AND MP2) FUNCTIONS

Two microprocessors (50-003) control logic operations of the tape control.

Operation of MP2 is dependent on the operation of MP1. MP2 remains idle until MP1 supplies it with an address at which to begin. MP1 operates constantly, either executing a routine required by the operation being performed or polling the possible conditions that can require the execution of a routine.

Microprocessors consist of:

Read Only Storage (ROS) in which the microprogram is stored for use by the microprocessor. The contents of ROS cannot be modified by the microprogram.

An Arithmetic Logic Unit (ALU) which performs all arithmetic and logic operations: ADD, AND, OR, and XOR.

Registers and Buses to hold or transfer data for subsequent use.

Read Only Storage is addressed by three-digit hexidecimal numbers 000 through 7FF. Each addressable unit in the Read Only Storage is 16 bits long. The first digit of the address specifies a page (block of 256 addresses) of Read Only Storage. Each microprocessor has 8 pages of storage, 0 through 7. The two low-order digits specify one of the possible 256 addresses in a page.

In general, MP1 handles all logic operations dealing with the channel and MP2 handles the operations dealing with the tape units.

The microprocessors can transfer bytes of information between them and test single bits stored in the other microprocessor.

MICROPROCESSOR INSTRUCTIONS

The microprocessors use 12 instructions. See following pages.

MICROPROCESSOR INSTRUCTION FORMAT

Microprocessor instructions have the following format:

[label]OPCODE field1,field2[comments]

where **label** is a one- to eight-character name by which the instruction can be referenced. Branch instructions point to locations in the microprogram by label.

OPCODE is the operation to be performed on the data or addresses in Field 1 or Field 2.

Field 1 is generally the address of a Local Storage Register. In some instructions this field may be a branch condition or ROS page number.

Field 2 is generally a constant, referred to as a decimal number or by a symbolic name. The value of symbolic constants for each microprocessor is listed in the beginning of the listings as EQU statements. In some instructions this field may be a branch address or transfer code.

Field 2 can contain several symbolic constants combined arithmetically, that is, the sum or difference of two or more constants.

For example, the constant in the instruction:

ADD WORK1,ONES-174

results in the constant hexidecimal FF (ONES) minus the decimal value 174, or a decimal value of 81.

MICROPROGRAM EC's

Microprogram EC's are applied with two Array Patch Cards, type DE01, which provide auxiliary ROS arrays. The arrays contain four sets of microcode patches (ALU1 and 2 for 3803-1 and 2). Plug each card as shown in Figure 1 in order to select the proper patches for it's location. The following patches are active when these two cards are installed (refer to page 52-102 for the patch listings):

1. Alternate Path Device Busy
2. Velocity Retry Extension
3. Turnaround Delay
4. Allocated Busy
5. Truncated Postamble
6. Extra Device End
7. Sense Reset

Verify factory plugging:

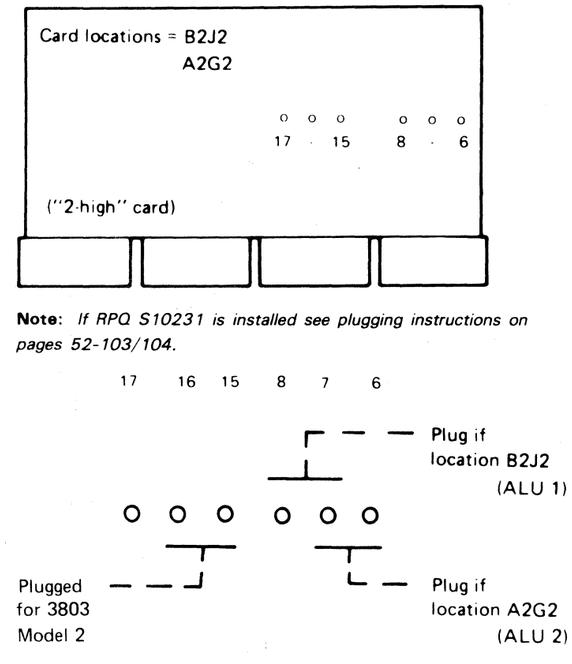

FIGURE 1

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HIGH-ORDER ROS REGISTER

The High-Order ROS Register in each microprocessor holds the 8 high-order bits of a microprogram instruction. The registers in MP1 and MP2 are identical. Bits 0 through 3 contain the operation code. Bits 3 through 7 contain a branch condition or LSR address. Bits 4 through 7 and the Hi/Lo latch can also contain the LSR address.

Bit 3 will be zero for OR, AND, ADD, XO, and STO instructions. In these instructions, bit 3=0 allows the addressed LSR to be updated.

Bit 3 in this register serves different purposes, depending on the instruction being executed. Bit 3 is part of the operation code for the modified instructions ORM, ADDM, ANDM, and XOM. This use prevents updating the LSR by blocking the gate to the LSR, CLK 15.

Bit 3 is part of the branch condition code for the BOC instruction. There are 32 branch condition codes used.

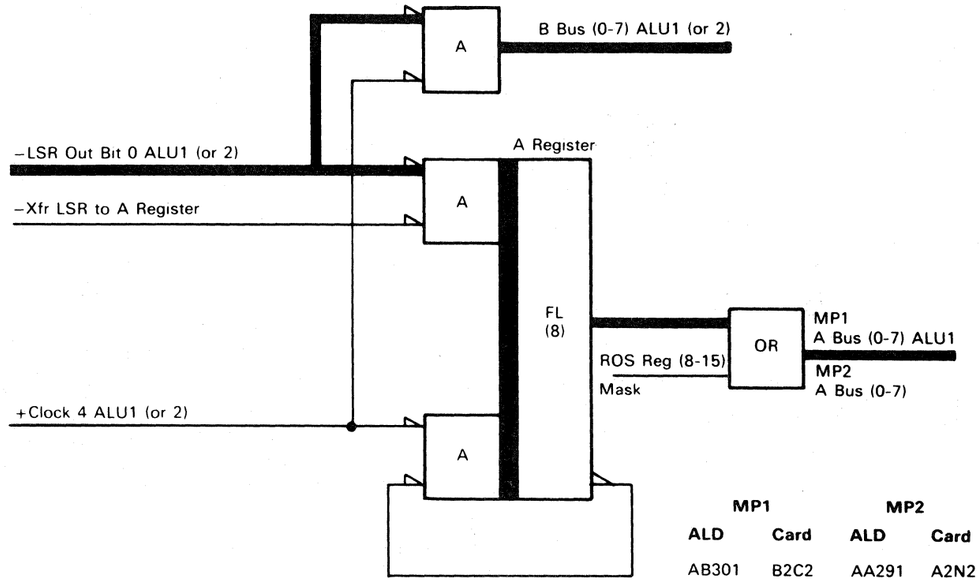
LOW-ORDER ROS REGISTER

The Low-Order ROS register in each microprocessor holds the 8 low-order bits of a microprogram instruction. The registers in MP1 and MP2 are identical. The output from these registers goes to the A Bus, the transfer decode circuits, or the Instruction Counter, depending on the instruction.

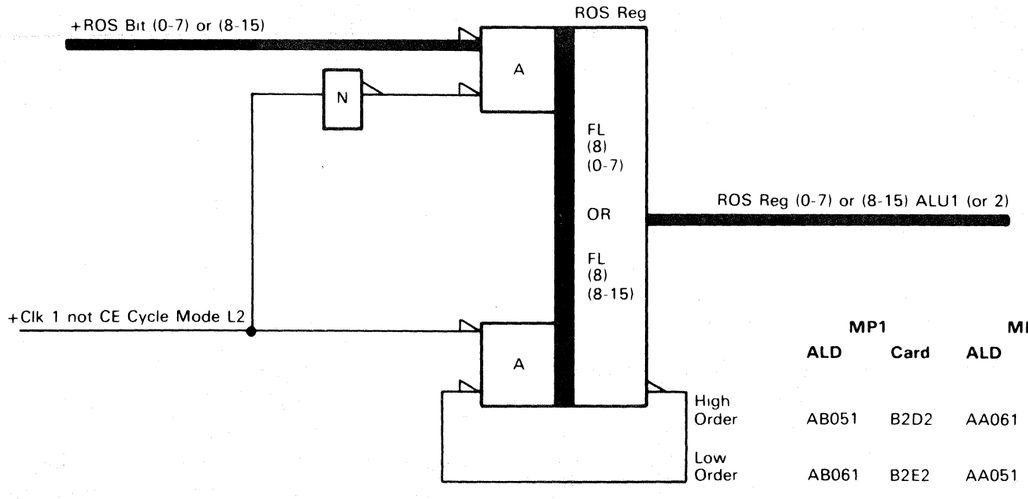
A REGISTER

The A Register serves as a buffer for information from an LSR that is used as input to the ALU. The contents of the selected LSR are gated to the A Register by XFR LSR TO A REGISTER. The next logic operation (ADD, AND, OR, or XOR) ORs the contents of the A Register with the contents of the instruction's Field 2 and places the result on the A Bus.

During logic operations, the A Register is reset by the CLK 4 line.



	MP1		MP2	
	ALD	Card	ALD	Card
	AB301	B2C2	AA291	A2N2



	MP1		MP2	
	ALD	Card	ALD	Card
High Order	AB051	B2D2	AA061	A2M2
Low Order	AB061	B2E2	AA051	A2L2

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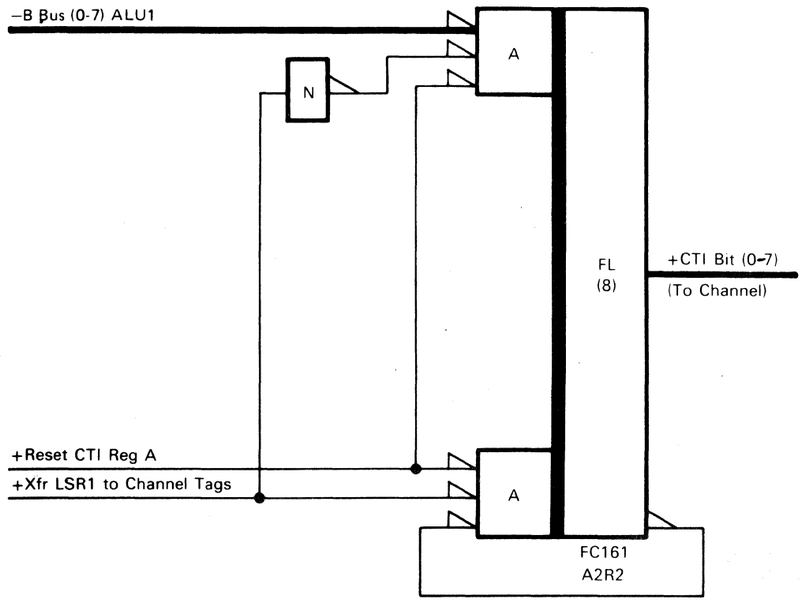
CHANNEL TAGS IN REGISTER

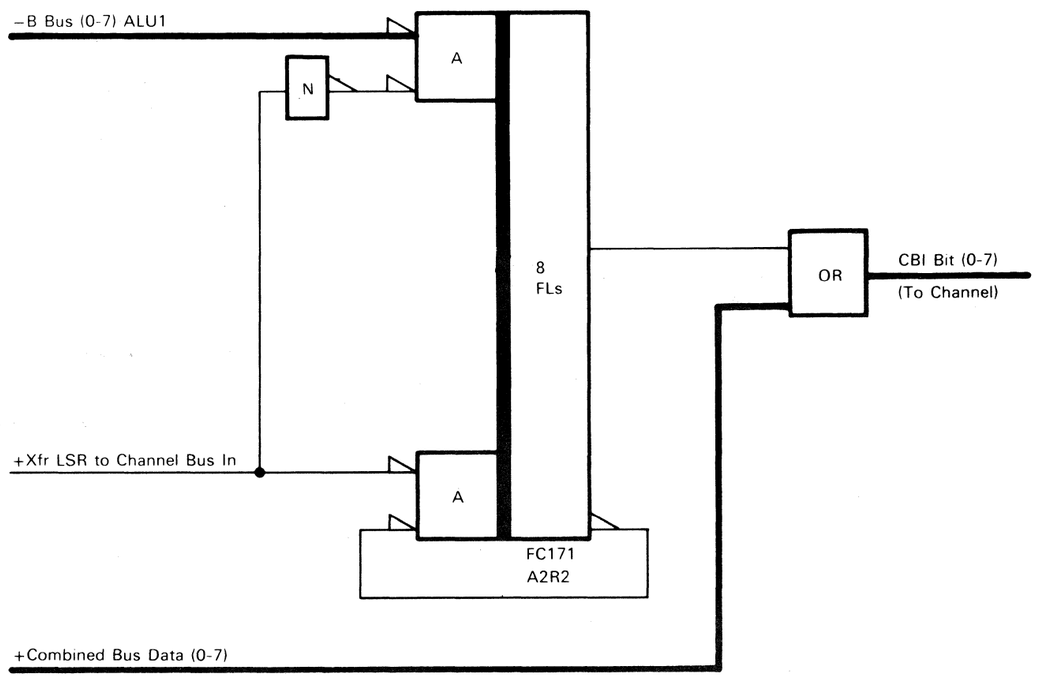
The Channel Tags in register holds the channel tags bits until they are transferred to the Channel Bus In. Individual register bits are used as follows:



Bit	Function
0	Chain Hold A
1	Chain Hold B
2	Hold Interface or Busy
3	CU Busy
4	Service In
5	Status In CTI Bit 5 to CE
6	Address In CTI Bit 6 to CE
7	Op In

CHANNEL BUS IN REGISTER

The Channel Bus In register serves as a buffer to transfer bytes from LSRs in MP1 to channel.



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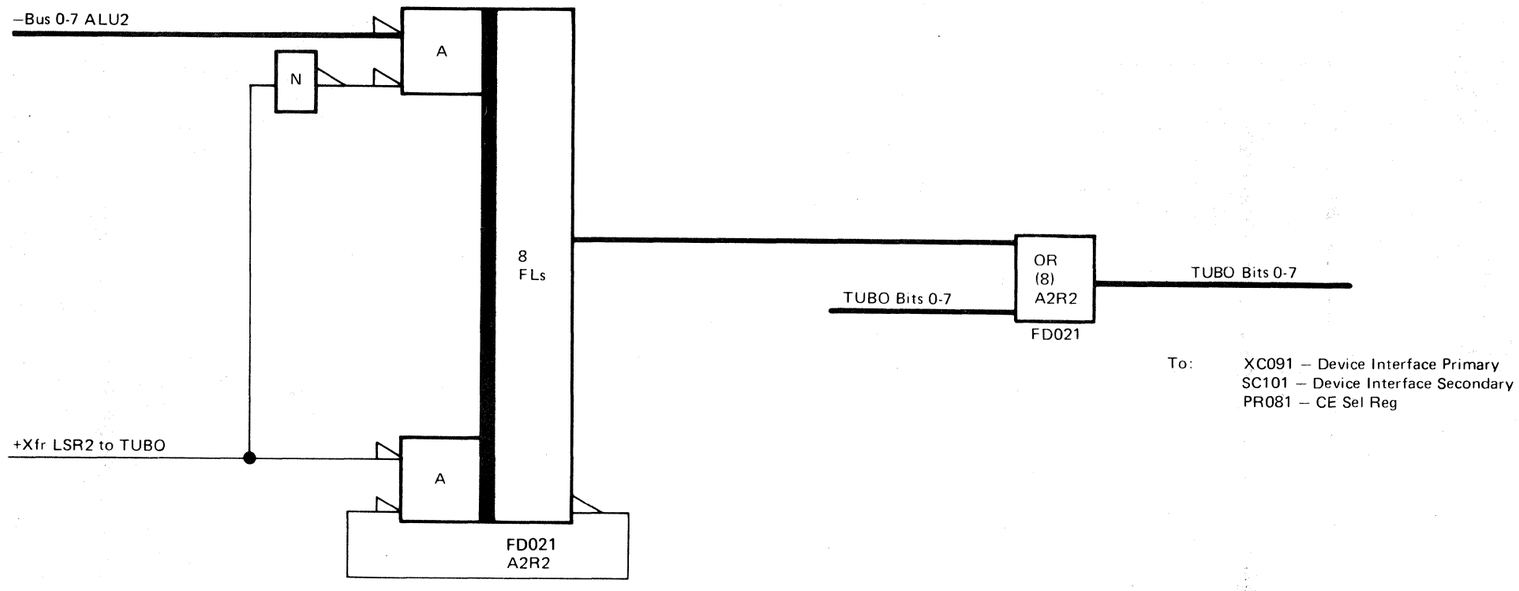
TAPE UNIT BUS OUT (TUBO) REGISTER

The TUBO register is a buffer to hold control information. High speed output is ORed with data bus bits.

The TUBO register stores MP2 control information for the 3420. The output information is multiplexed with tag lines (MOVE, CONTROL, COMMAND) to control tape unit functions.



To: XC091 – Device Interface Primary
SC101 – Device Interface Secondary
PR081 – CE Sel Reg

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D REGISTERS

The D Register serves as a buffer between the ALUs and LSRs.

A CLK 22 pulse loads the data into the D Register and resets individual positions when no data is available to load them.

Transfer (XFR) microinstructions gate input from BUS OUT.

CLK 21 degates D Register input from the ALU during store and transfer operations. During logic operations, this input remains active because CLK 21 does not occur.

MP1 SPECIAL REGISTER (HARDWARE ERRORS)

The Special Register in MP1 (AB461) is not used as a conventional register, because the input gate is always active and the latchback is always inactive. MP1 hardware errors merely pass through the register becoming SPEC REG BITS 0-7. When needed, parity bit is generated to maintain odd parity.

Special Register bits are activated as follows:

Spec Reg Bit	Error Line
0	ALU Parity Error ALU1
1	ROS Parity Error ALU1
2	IC or XFR Parity Error ALU1
3	Microprogram Error ALU1
4	Instruction Care Error ALU1
5	D Bus Parity error ALU1
6	Unused
7	Branch Error Interface ALU1

MP2 SPECIAL REGISTER (TU BUS IN)

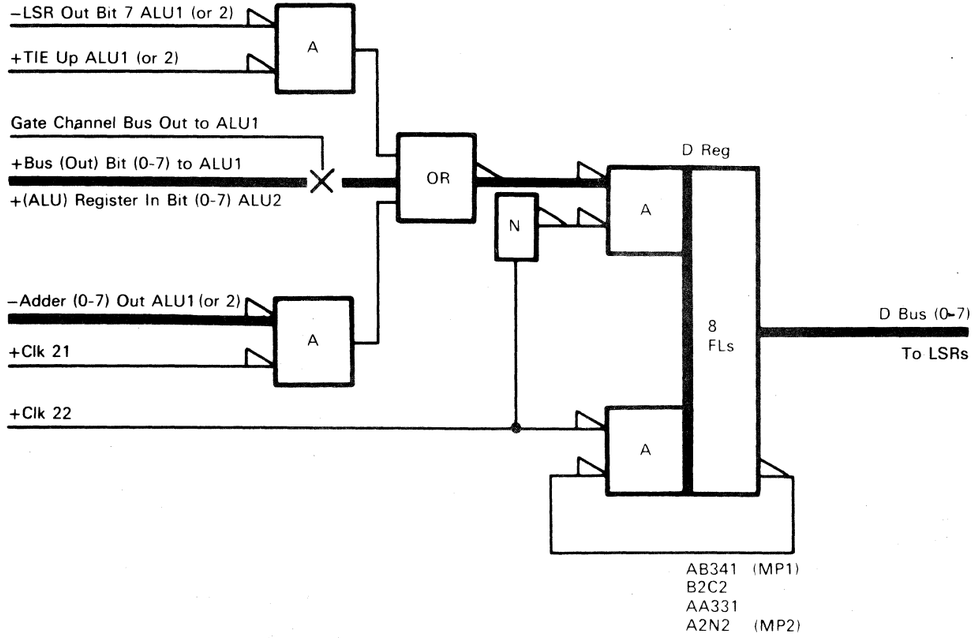
The Special Register in MP2 (FD011) is used as the Tape Unit Bus In Register. The Device Bus In bits are called DEVICE BITS LATCHED. The register gate is CLK 18 SET TUBI ALU2. When needed, parity bit is generated to maintain odd parity.

MIST OR TCS REGISTER (MP1)

The MIST (Multi-Interface Tags) Register (FC181) is used as a Request In Register when the Two-Channel Switch (TCS) feature is installed. This register has four bits assigned as suppressable and non-suppressable REQUEST INS for Channel A and B.

Bit functions are:

Bit	Function
4	Suppressable REQUEST IN Channel A
5	Non-suppressable REQUEST IN Channel A
6	Suppressable REQUEST IN Channel B
7	Non-suppressable REQUEST IN Channel B



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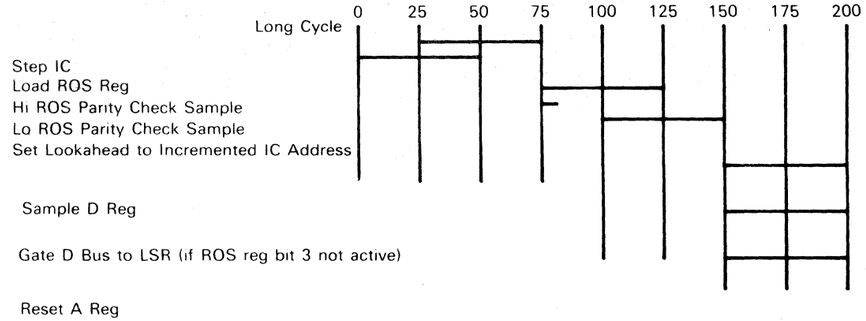
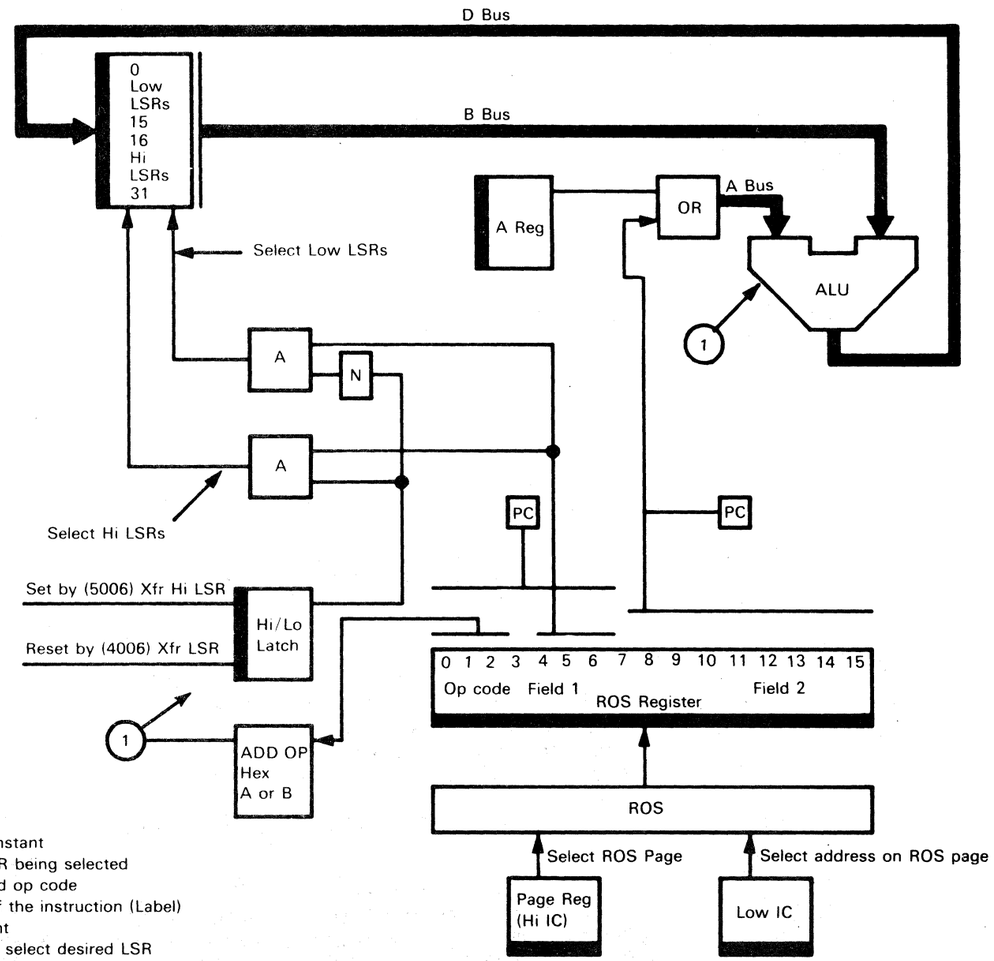
OPER—ARITHMETIC ADD

ADD/ADDM (HEX CODE A OR B)

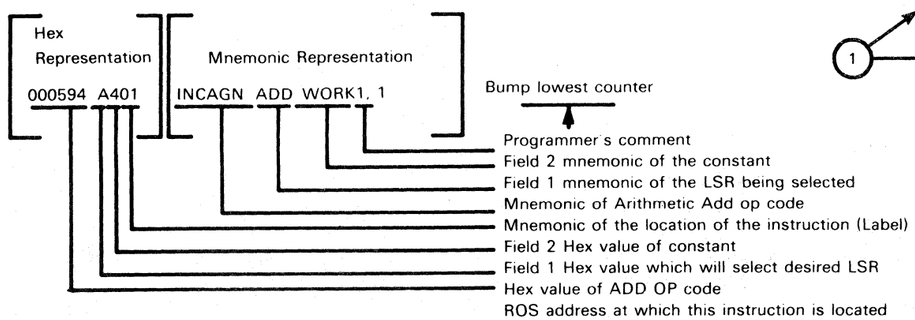
1. The LSR byte selected by Field 1 (ROS reg bits 4-7) is placed on the B Bus.
2. The A register is ORed with the constant in Field 2 (ROS reg bits 8-15).
3. The result is placed on the A bus.
4. The A bus and the B bus are added together.
5. The result is placed on the D bus.

If the operation is an ADD, the D bus is stored into the LSR byte addressed by Field 1 and the Hi/Lo latch. The result of an ADDM operation is not stored in an LSR. The result of either operation remains on the D bus until the next ALU operation. While on the D bus, the result of the operation is available for branch control. The A Register is reset at the end of the operation.





Sample of an Arithmetic ADD Instruction



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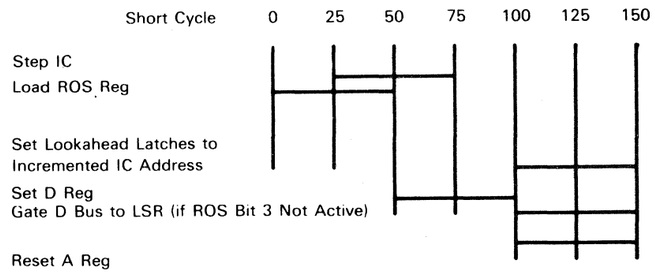
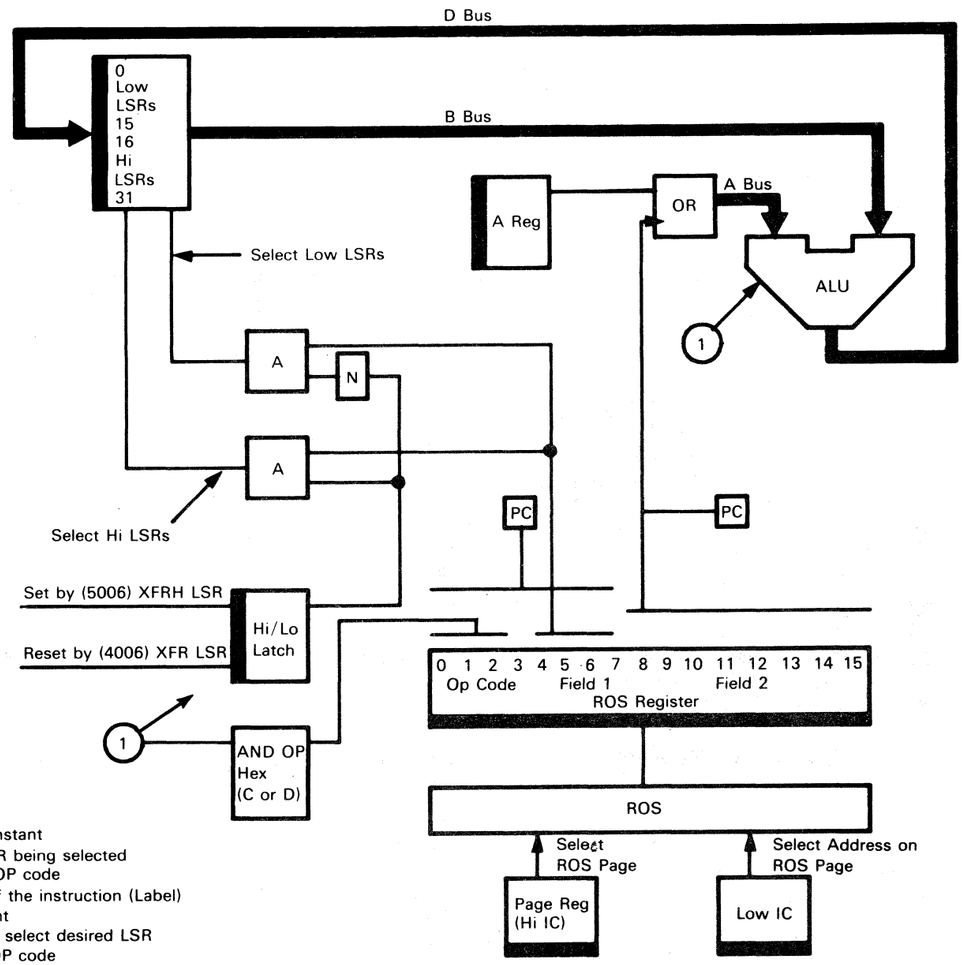
52-065

AND/ANDM (HEX CODE C OR D)

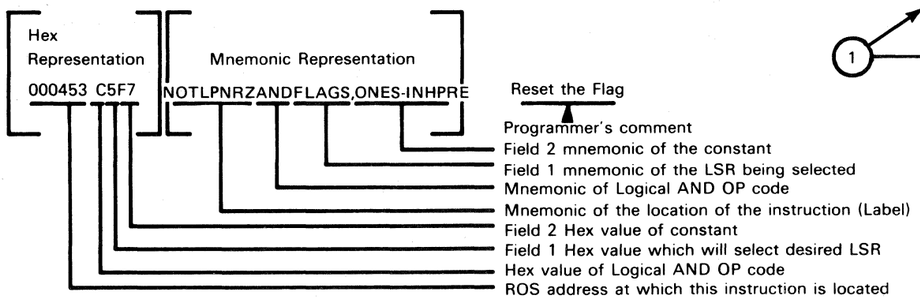
1. The LSR byte selected by Field 1 is placed on the B bus.
2. The A Register is ORed with the constant in Field 2.
3. The result is placed on the A bus.
4. The A bus and the B bus are ANDed.
5. The result is placed on the D bus.

If the operation is an AND, the D bus is stored back into the LSR byte addressed by Field 1 and the HI/LO latch. The result of an ANDM is not stored in an LSR. The result of either operation remains on the D bus until the next ALU operation. While on the D bus, the result of the ANDM operation is available for branch control. The A Register is reset at the end of the operation.





Sample of a Logical AND Instruction



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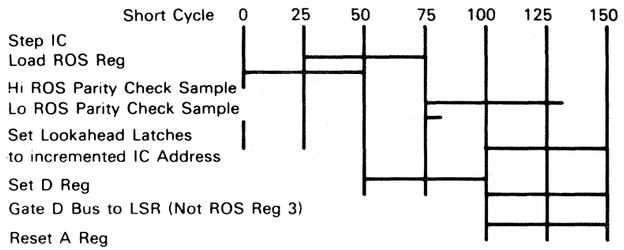
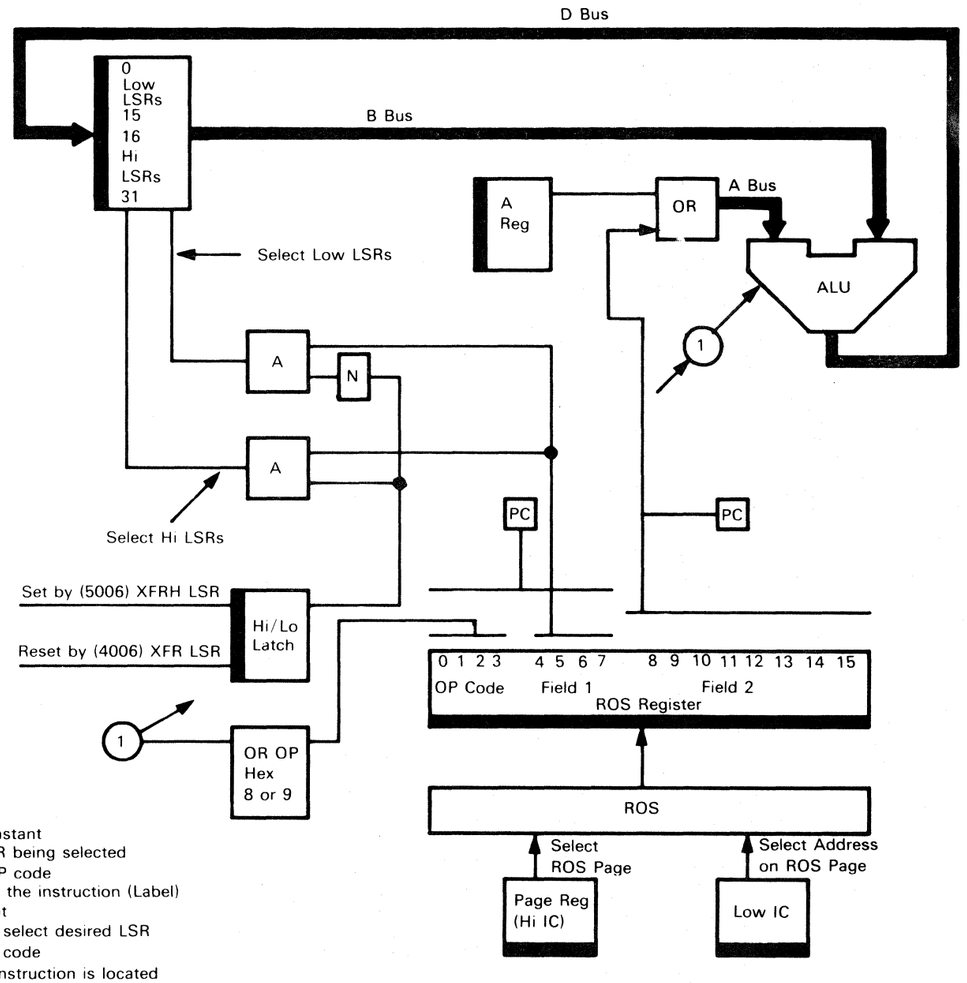
OPER—LOGICAL OR

ORI/ORM (HEX CODE 8 OR 9)

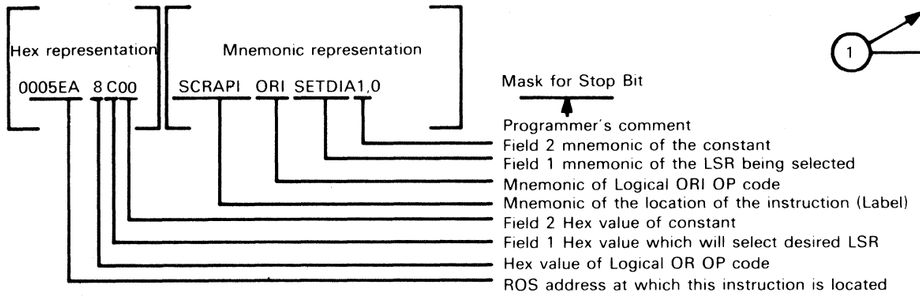
1. The LSR byte selected by Field 1 is placed on the B bus.
2. The A register is ORed with the constant in Field 2.
3. The result is placed on the A bus.
4. The A bus and the B bus are ORed.
5. The result is placed on the D bus.

If the operation is an ORI, the D bus is stored back into the LSR byte addressed by Field 1 and the Hi/Lo latch. The result of an ORM is not stored in the LSR. The result of either operation remains on the D bus until the next ALU operation. While on the D bus, the result of the operation is available for branch control. The A Register is reset at the end of the operation.





Sample Logical OR Instruction



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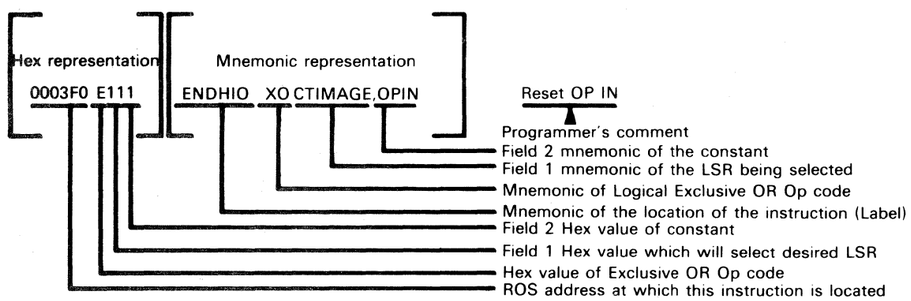
OPER—LOGICAL EXCLUSIVE OR

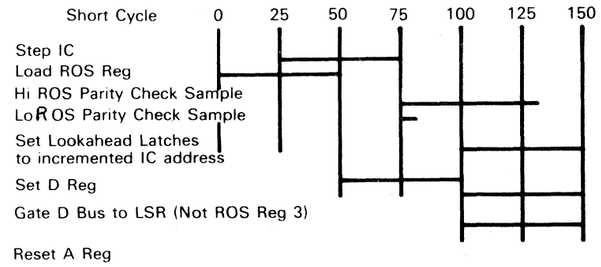
XO/XOM (HEX CODE E OR F)

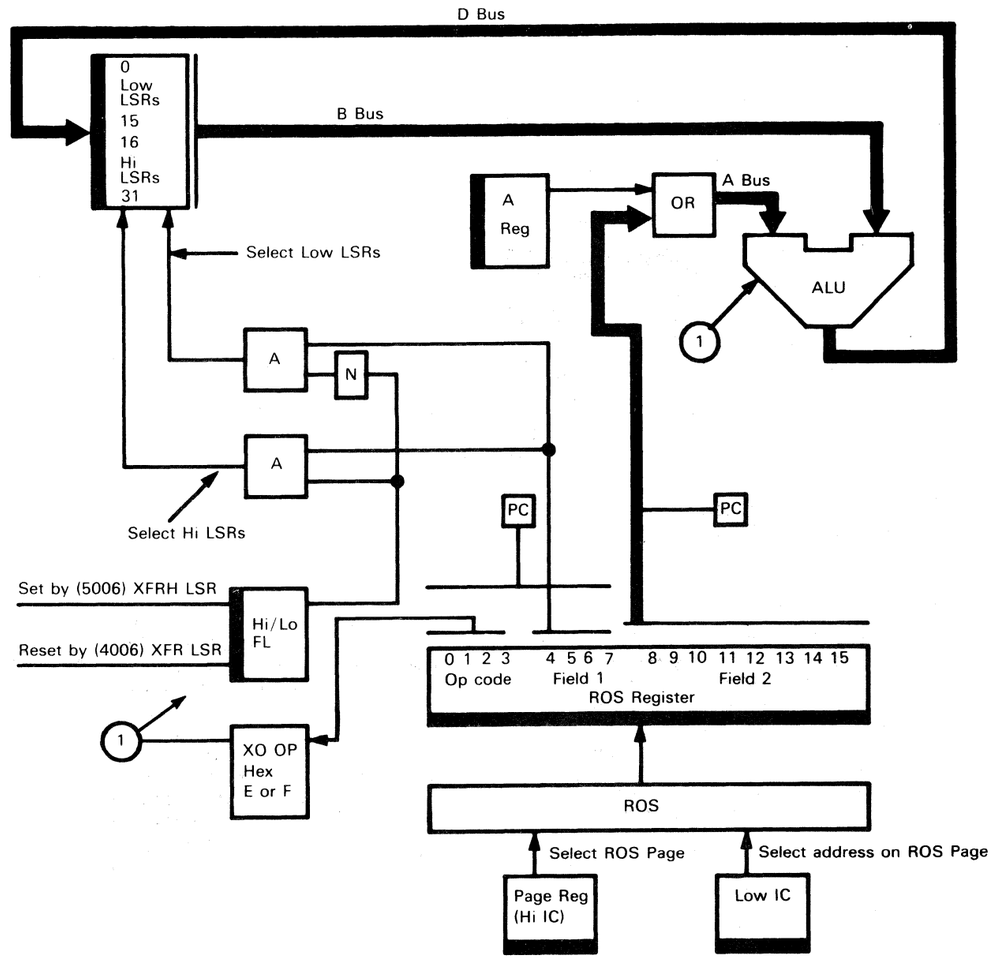
1. The LSR byte selected by Field 1 is placed on the B bus.
2. The A register is ORed with the constant in Field 2.
3. The result is placed on the A bus.
4. The A bus and the B bus are exclusive ORed.
5. The result is placed on the D bus.

If the operation is an XO the D bus is stored in the LSR byte addressed by Field 1 and the Hi/Lo latch. The result of an XOM operation is not stored in an LSR. The result of either operation remains on the D bus until the next ALU operation. While on the D bus, the result of the operation is available for branch control. The A Register is reset at the end of the operation.

Sample Logical Exclusive OR Instruction







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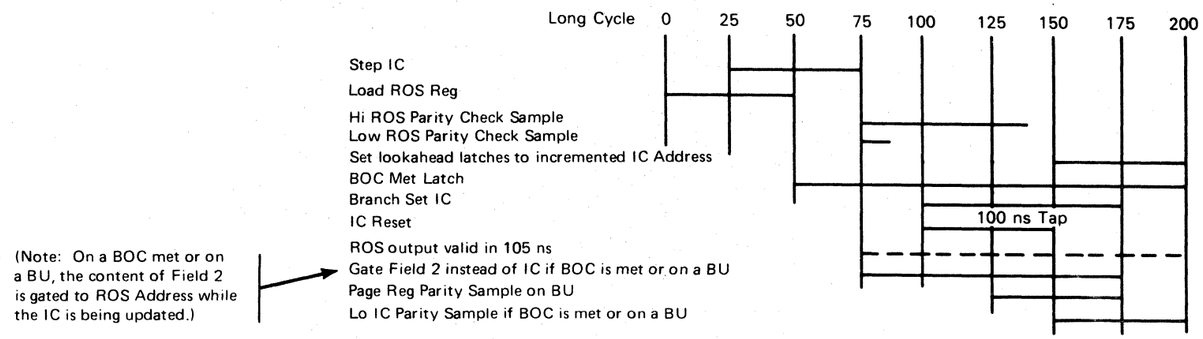
OPER—BRANCH ON CONDITION

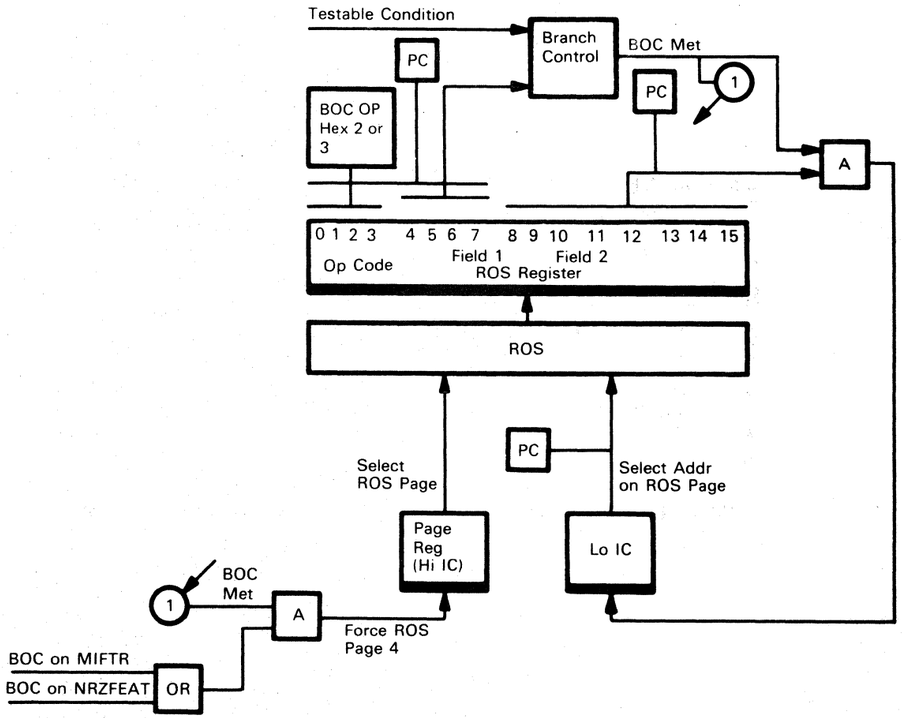
BOC (HEX CODE 2 OR 3)

ROS reg Field 1, together with bit 3, is decoded to test one of 32 conditions. If the BOC is met, ROS reg Field 2 is set into the Lo IC. See 52-086 for a complete listing of MP1 and MP2 branch conditions.

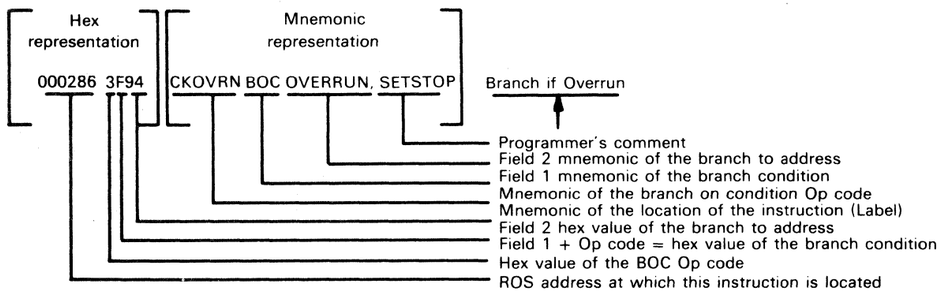
The contents of the A reg are not altered.

Special Condition—If the two-channel switch or NRZI features are installed, a BOC on these features (BOC on 'MIFTR' or 'NRZFEAT') results in a successful BOC with the Hi IC forced to ROS page 4. See logic diagram.





Sample of a Branch On Condition Instruction



(**Note**: On a BOC met or on a BU, the contents of Field 2 are gated to ROS Address while the IC is being updated.)

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MP1 BRANCH CONDITIONS

BOC Instr+ Field 1	ROS Reg Bits 3	4	5	6	7	Microprogram Name of Line Sensed	Logic Line Name of Condition Sensed	Branch Cond Logic Page	Source Logic
20	0	0	0	0	0	DBUS D Reg equal 0	ALU output all zero ALU1	AB121	AB371
21					1	NALCO not ALU carry out	Not ALU carry ALU1	AB121	AB371
22				1	0	ALUR ALU2/ALU1 Error	Any hardware error ALU2	AB121	AA461
23				1	1	MIFTR** MIS or 7-Trk Feature	Feature present ALU1	AB121	AB131
24			1	0	0	BOPE Bus Out parity error	Not Bus Out parity odd	AB131	FC151
25			1	0	1	NCUEA Not CU End Chan A	Not CUE pending Chan A	AB131	FC031
26			1	1	0	SELO Select Out	Gated Select Out	AB131	FC141
27			1	1	1	DFLER	Data Check (Not Tape Op)	AB131	BW241
27			1	1	1	Clock"B"	Write Grp "B" (Tape Op)	AB131	BW151
28		1	0	0	0	ADROUT Addr Out A or B	Address Out A B CE	AB171	AB171
29		1	0	0	1	CMDOUT Cmd Out A or B	Command Out A B CE	AB171	FC151
2A		1	0	1	0	STATA Stat A ALU1	Stat A ALU1	AB151	AB141
2B		1	0	1	1	STAT B Stat B ALU2	Stat B ALU2 to ALU1	AB151	AA141
2C		1	1	0	0	SELRST Selective Reset	Selective Reset	AB171	FC151
2D		1	1	0	1	SVCOUT Service Out	Service Out only on write ops. Service In or Service Out on read ops.	AB171	FC151
2E		1	1	1	0	SCB Switched to Chan "B"	Switched to Chan "B"	AB161	XM101
2F		1	1	1	1	PWRRST Power On Reset	Mach or Gen Reset Chan A B	AB161	AB161
30	1	0	0	0	0	DREG0* D Reg Bit 0 On	D Bus 0 ALU1	AB121	AB341
31	1	0	0	0	1	DREG1 D Reg Bit 1 On	D Bus 1 ALU1	AB121	AB341
32	1	0	0	1	0	DREG2* D Reg Bit 2 On	D Bus 2 ALU1	AB121	AB341
33	1	0	0	1	1	DREG3* D Reg Bit 3 On	D Bus 3 ALU1	AB121	AB341
34	1	0	1	0	0	DREG4* D Reg Bit 4 On	D Bus 4 ALU1	AB131	AB351
35	1	0	1	0	1	DREG5* D Reg Bit 5 On	D Bus 5 ALU1	AB131	AB351
36	1	0	1	1	0	DREG6* D Reg Bit 6 On	D Bus 6 ALU1	AB131	AB351
37	1	0	1	1	1	DREG7* D Reg Bit 7 On	D Bus 7 ALU1	AB131	AB351
38	1	1	0	0	0	OPRIN Operation In	Channel Operation In	AB171	FC141
39	1	1	0	0	1	SUPO Suppress Out	Suppress A B	AB171	FC151
3A	1	1	0	1	0	STATC Stat C ALU2	Stat C ALU2 to ALU1	AB151	AA141
3B	1	1	0	1	1	STATD Stat D ALU2	ALU2 Locked Status	AB151	AA451
3C	1	1	1	0	0	NGENR Not Gen Reset	Not General Reset Chan A B	AB171	FC041
3D	1	1	1	0	1	ISEL Initial Selection	Initial Selection A B CE	AB171	AB171
3E	1	1	1	1	0	NCUEB Not CUE for Chan	Not CUE PENDING Chan B	AB161	XM031
3E	1	1	1	1	0	Buffer Branch	RD Channel Buffer (Stop to DF)	AB161	BR011
3F	1	1	1	1	1	Overrun	Data Flow Detected Overrun (Not Tape Op)	AB161	BW241
3F	1	1	1	1	1	All Ones	End of Data being written (Tape Op)	AB161	BW151

* May be called other names as well.

** If this feature is installed, force Hi IC to ROS Page 4.

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MP2 BRANCH CONDITIONS

BOC Instr+ Field 1	ROS Reg Bits 3	4	5	6	7	Microprogram Name of Line Sensed	Logic Line Name of Condition Sensed	Branch Cond Logic Page	Source Logic
20	0	0	0	0	0	DBUS D Reg equal 0	ALU0	AA121	AA361
21					1	NALCO	Not ALU carry	AA121	AA361
22				1	0	ROCROT	ROS rotation (Tape Op)	AA121	CB411
22				1	0	CRC NEPR	CRC not equal EPR (Not Tape Op)	AA121	CN011
23				1	1	NRZFEAT** Installed	Feature present	AA121	AA131
24			1	0	0	RD Time	Read Time	AA131	BW221
25			1	0	1	N Seven	Not Seven Track	AA131	AA131
26			1	1	0	TACHFF	Tach Velocity (Write CKT)	AA131	XC031
27			1	1	1	STOP Stop Command	Stat Bit 0 ALU1 to ALU2	AA131	AB141
28		1	0	0	0	ENDATA Ending Zeros	End of Data (Tape Op)	XC041	BW241
28		1	0	0	0	CRCMAT	CRC OK (Not Tape Op)	XC041	CH111
29		1	0	0	1	NCONVCK	Data CC Check (Not Tape Op)	XC041	BN071
29		1	0	0	1	NSAGC ID	Inverse TM (Tape Op)	XC041	CC001
2A		1	0	1	0	STATA Stat A ALU2	Stat A ALU2	XC041	AA141
2B		1	0	1	1	STATB Stat B ALU1	Stat B ALU1	XC041	AB141
2C		1	1	0	0	NPTE	Data P Track Only (Tape Op)	XC051	BW231
2C		1	1	0	0	DEN 556	556 bpi (7-Track)	XC051	BN311
2D		1	1	0	1	DATA RDY	Data Rdy from DF (Tape Op)	XC051	CH131
2D		1	1	0	1	RPQ	RPQ Installed (Not Tape Op)	XC051	RPQ
2E		1	1	1	0	BOR	Beginning of Record (Tape Op)	XC051	CC001
2F		1	1	1	1	IBG	IBG Detected (Tape Op)	XC051	CC001
30	1	0	0	0	0	DREG0* D Reg Bit 0 On	D Bus 0 ALU2	AA121	AA331
31	1	0	0	0	1	DREG1* D Reg Bit 1 On	D Bus 1 ALU2	AA121	AA331
32	1	0	0	1	0	DREG2* D Reg Bit 2 On	D Bus 2 ALU2	AA121	AA331
33	1	0	0	1	1	DREG3* D Reg Bit 3 On	D Bus 3 ALU2	AA121	AA331
34	1	0	1	0	0	DREG4* D Reg Bit 4 On	D Bus 4 ALU2	AA131	AA341
35	1	0	1	0	1	DREG5* D Reg Bit 5 On	D Bus 5 ALU2	AA131	AA341
36	1	0	1	1	0	DREG6* D Reg Bit 6 On	D Bus 6 ALU2	AA131	AA341
37	1	0	1	1	1	DREG7* D Reg Bit 7 On	D Bus 7 ALU2	AA131	AA341
38	1	1	0	0	0	6400	RLC Branch	XC041	BW231
39	1	1	0	0	1	N1TE	Not One Track Envelope	XC041	BW231
39	1	1	0	0	1	DEN 200	Density 200 (Seven Track)	XC041	BN311
3A	1	1	0	1	0	STATC Stat C ALU1	Stat C ALU1 Mark on Wall	XC041	AB141
3B	1	1	0	1	1	STATD Stat D ALU1	Stat D ALU1	XC041	AB141
3C	1	1	1	0	0	NENVLOS	No Envelope Loss (Not Tape Op)	XC051	CC011
3C	1	1	1	0	0	NBLOCK	No Zone Up (Tape Op)	XC051	CC011
3D	1	1	1	0	1	NTM	Tape Mark	XC051	CC001
3E	1	1	1	1	0	BSYTACH	Busy or Tach	XC051	XC031
3F	1	1	1	1	1	DEVATTN	Interrupt	XC051	XC031

* May be called other names as well.

** If this feature is installed, force Hi IC to ROS Page 4.

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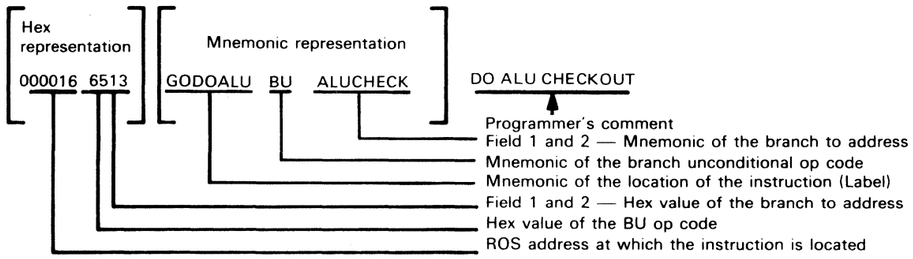
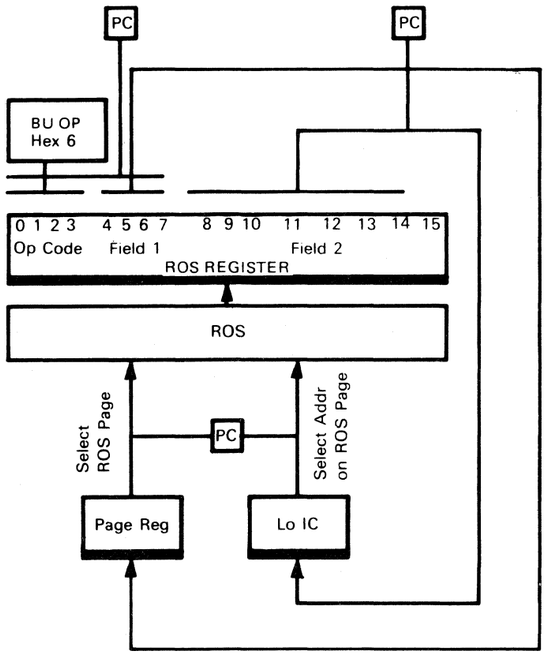
BRANCH UNCONDITIONAL - BU (HEX CODE 6)

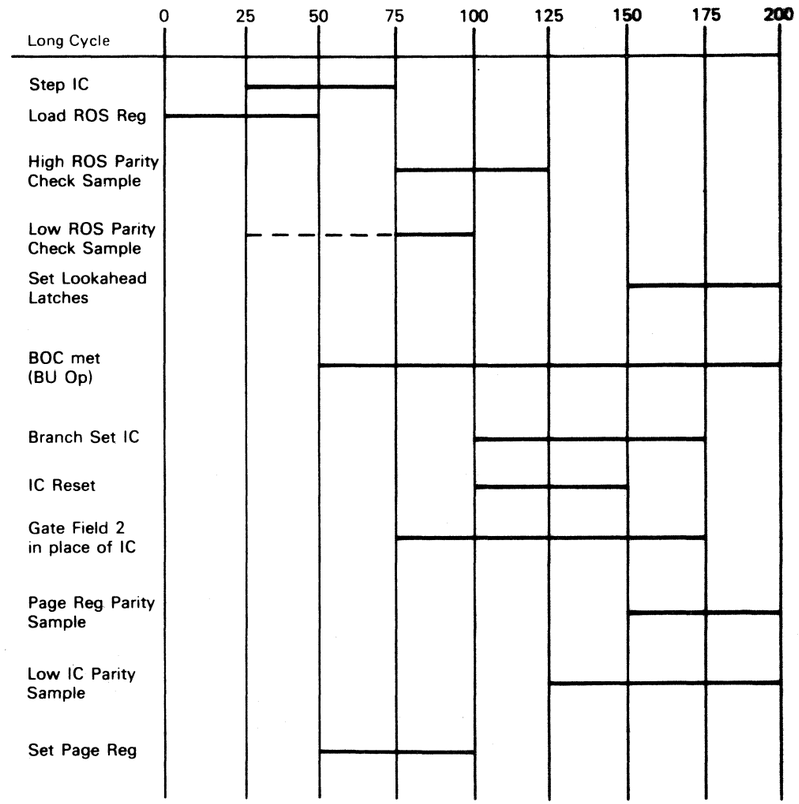
1. The contents of ROS reg Fields 1 and 2 are set into the Hi IC and Lo IC.
2. The contents of the A reg are not altered.

Sample of a Branch Unconditional Instruction





BRANCH UNCONDITIONAL



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NOTES:

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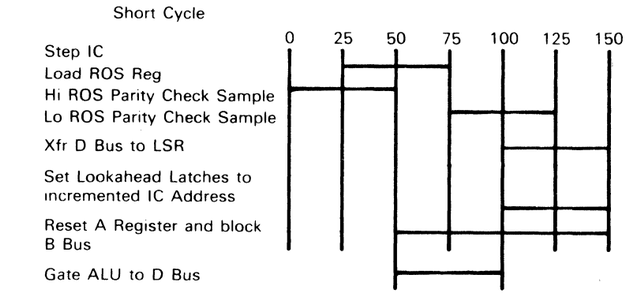
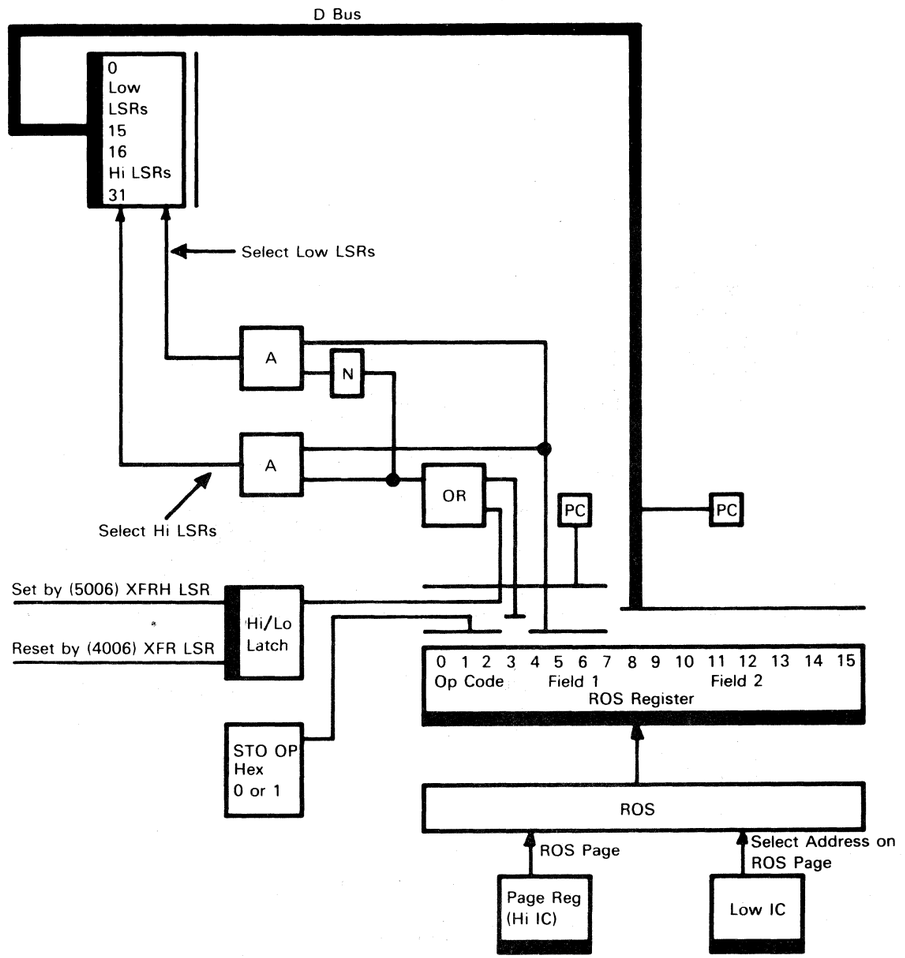
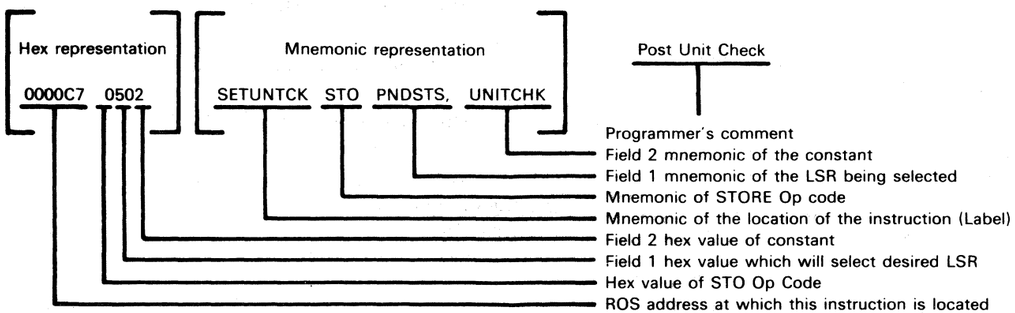
STORE - STO (HEX CODE 0 OR 1)

1. The contents of Field 2 are stored in an LSR selected by Field 1.
2. LSR selection is modified by the condition of the HI/LO latch and ROS register bit 3 (see logic diagram).
3. The A register is reset.





Sample of a STORE Instruction



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TRANSFER - XFR (HEX CODE 4 OR 5)

The hex value (transfer decode) in Field 2 controls all transfer operations. All XFR decodes for both ROS1 and ROS2 are on 52-101.

Some transfer decodes cause data to be transferred between an LSR selected by Field 1 and a hardware register selected by Field 2. LSR selection is modified by the condition of the HI/LO latch and ROS reg bit 3 (see logic diagram).

Some transfer decodes do not select LSRs (that is, Field 1 is ignored). These operations create miscellaneous Set, Reset, and Gating pulses to hardware.

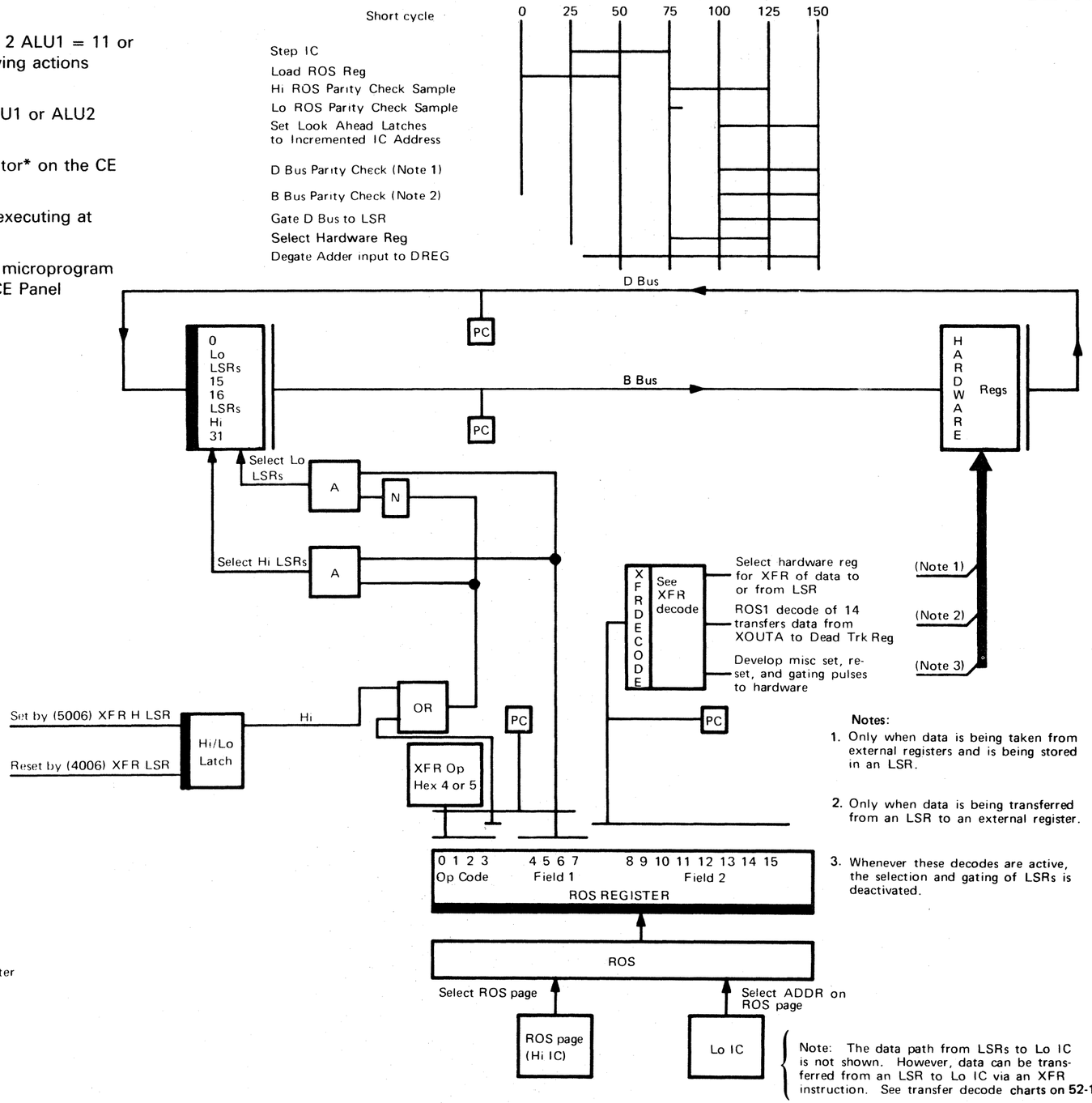
One transfer decode (ROS1 XFR decode of 14) transfers data from one hardware register to another (ROS1 XOUTA TO DEAD TRK REG).

Contents of the A register are not altered except as described under special condition 1 below.

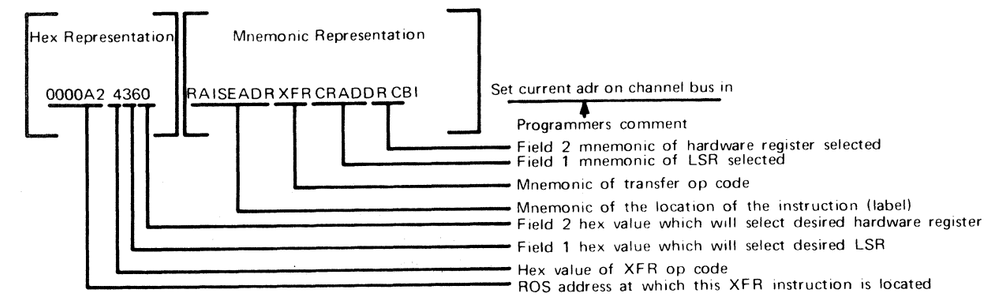
Special Conditions:

1. Whenever a XFR from LSR to A reg (Field 2 hex 21) is decoded, the XFR is really a logical OR (for example, A register bits that were ON remain ON).
2. Whenever a XFR 'HDWERR' (Field 2 ALU1 = 11 or ALU2 = 44) is decoded, the following actions occur:
   a. Bit 4 in sense byte 11 or 12 (ALU1 or ALU2 respectively) is set.
   b. The UPGM Control Check indicator* on the CE panel is turned on.
   c. IC is reset to 000 (ROS1 starts executing at 000—ROS2 holds at 000).

   * For additional information on microprogram control check, see 75-003: "CE Panel Indicators."



Sample Transfer Instruction



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MICROPROGRAM TRANSFER DECODES

TRANSFER DECODE—MP1

DECODE	MP1		
Field 2	Micro-program Name	Use	Logic Line Names XFR Decode AB181
05	RSTDOMTD	Reset device committed latch	Reset committed latch ALU1*
06	LSR	Set local store sel latch hi or low	Set LSR hi or lo*
09	CUREA	Reset CUE or general reset latch Intf A	Reset CUE Chan A*
0A	CUREB	Reset CUE or general reset latch Intf B	Reset CUE Chan B*
11	HDWERR	Set Sense Byte 11 Bit 4 (force ROS 1 ALU hardware error)***	XFR Set Checkout error*
12	CLEAR	Reset all hardware error latches for ROS1, ROS2 and data flow	Reset Sense Data*
14	TIP	MP1 XOUTA to Dead Track register	Xfr XOUTA to DT Reg
18	Spare		Spare Xfr 18
21	AR	LSR to A Reg	Xfr LSR to A Reg
22	IC	LSR to Instr. Ctr (Lo IC)	Xfr B Bus to IC
24	TUADR	LSR to TU Address Reg	Xfr TU Address
28	STAT	LSR to ROS1 Stat Reg	Xfr LSR1 to Stat
41	XOUTB	LSR to ROS1 XOUTB Reg	Xfr XOUTB TO Trap ALU2
42	XOUTA	LSR to ROS1 XOUTA Reg	Xfr LSR1 to XOUTA
43**		- - - -	- - - -
44	PING	Hardware Error Reset	Reset PING Pulse*
48	MIST	LSR to set or reset Req In Tags	Xfr LSR1 to Request Tags
50	CTI	LSR to Channel Tags In Reg	Xfr LSR1 to Channel Tags
60	CBI	LSR to Channel Bus In Tags Reg	Xfr LSR1 to Channel Bus In
81	EXT	ROS2 ALU hardware error reg to LSR	Xfr Ext inputs to LSR1
82	INHP	Not used	- - - -
84	HDWR	ROS1 ALU hardware error to LSR	Xfr Hardware Reg
88	XINB	ROS2 XOUTB Reg to ROS1 LSR	Xfr XINB to LSR1
90	XINA	ROS2 XOUTA Reg to ROS1 LSR	Xfr XINA to LSR1
A0	CBO	Channel Bus Out Reg to LSR	Gate Chan Bus Out to ALU

TRANSFER DECODE—MP2

DECODE	MP2		
Field 2	Micro-program Name	Use	Logic Line Names XFR Decodes AA171
05	Spare sense byte 11 bit 4 (force	- - - -	Spare
06	LSR	Set local store sel latch hi or lo	Set LSR hi or lo*
09	Reset ERR	Reset errors single byte noise	File Operation Pulse
0A	CRC	Shift CRC Pulse	Spare Xfr 0A
11	Indf	Set Diagnostic Channel Buffer Read	Pulse Reset CRC
12	POINTERS	Sample pulse to set TIE	Step Format Count
14	Red Light	Set CE Panel Uprog det DF error	SKB and Det Ctrl
18	Buff CRC	Sample Buffer CRC error latch	Spare Xfr 18
21	AR	LSR to A Reg	Xfr LSR to A Reg
22	IC	LSR to Instr. Ctr (Lo IC)	Xfr B Bus to IC
24	TUTAG	LSR to TU Tags Reg	Xfr LSR2 to TU Tags 24
28	STAT	LSR to ROS2 Stat Reg	Xfr LSR2 to Stat
41	XOUTB	LSR to ROS2 XOUTB Reg	Xfr LSR2 to XOUTB
42	XOUTA	LSR to ROS2 XOUTA Reg	Xfr LSR2 to XOUTA
43**	XANXB	- - - -	- - - -
44	HDWERR	Set sense byte 12, bit 4 (force ROS2 ALU hardware error)***	Xfr Set Checkout Error
48	Spare	- - - -	- - - -
50	COMITD	Reset Device Committed latch	Reset Committed latch pulse*
60	TUBO	LSR to TU Bus Out Reg	Xfr LSR2 to TU Bus Out
81	TUBI	TU Bus In Reg to LSR	Gate Device Bus In to LSR2
82	INHP	Inhibit Parity on D Bus	Inhibit Parity on D Bus
84	XADDR	TU Bit Address Reg to LSR	Gate TU Addr to ALU2
88	XINB	ROS1 XOUTB Reg to ROS2 LSR	Xfr XINB to LSR
90	XINA	ROS1 XOUTA Reg to ROS2 LSR	Xfr XINA to LSR2

* These transfer operations cause no actual information transfer.
** With transfer decode of 43, transfer decodes 41 and 42 are executed simultaneously.
*** Also sets CE Panel UPGM Error light (Control Check Indicators).

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ALU1

Instr Addr	* Patch Store Control	Object Code	Source Statement			Patch Name
2DC	ENTER	C400		AND	WORK 1, ZERO	ALLOCATED BUSY
2DD	RETURN	62DE		BU	2DE	
328	ENTER	4828	DEPRIM4	XFR	STATIMG, STAT	ALTERNATE PATH DEVICE BUSY
329		3B8C		BOC	STATD, DEPRIM70	
32A		6380		BU	380, FREEAREA	
380		3A82	FREEAREA	BOC	STATC, CKCONCHA	
381	RETURN	632B		BU	32B	
382		D981	CKCONCHA	ANDM	FLAGS, CONCON+CHAIN	
383		2085		BOC	DBUS, TAG0	
384	RETURN	6338	PCHKONA	BU	338	
385		0202	TAG0	STO	XOUTAIM, SETSTATC	
386		4228		XFR	XOUTAIM, STAT	
387		A202	PA1DLY	ADD	XOUTAIM, X'02'	
388		2187		BOC	NALCO, PA1DLY	
389		0200		STO	XOUTAIM, 0	
38A		4828		XFR	STATIMG, STAT	
38B		6384		BU	PCHKONA	
38C	RETURN	633A	DEPRIM70	BU	33A	
335	ENTER	4828	DEPRIM6	XFR	STATDMG, STAT	
336		2B82		BOC	STATB, CKCONCHA	
337	RETURN	6337		BU	337	
0A3	ENTER	8520		ORI	PNDSTS, CUE	EXTRA DEVICE END
0A4		D50C		ANDM	PNDSTS, CEND+DEND	
0A5		34AA		BOC	DREG4, RTN1	
0A6		20AA		BOC	DBUS, RTN1	
0A7		4642		XFR	PNDADDR, XOUTA	
0A8		14EB		STO	XOUTBIM, NDXSTS	
0A9		5441		XFR	XOUTBIM, XOUTB	
0AA	RETURN	6296	RTN1	BU	TERMSTA2	
0F0	ENTER	1348		STO	LINK4, TERMATE	SENSE RESET
0F1	RETURN	5322		XFR	LINK4, IC	

ALU 2

Instr Addr	* Patch Store Control	Object Code	Source Statement			Patch Name
213	ENTER	1600	WRTSTR1	STOH	SENSE 1, 0	VELOCITY RETRY EXTENSION
214	RETURN	1300	VELSTR	STOH	WORK 4, ZERO	
7B8	ENTER	0200		STO	WORK 3, 0	
7B9	RETURN	1500		STOH	WORK 5, ZERO	
15A	ENTER	D708	DODELAY	ANDM	SENSE 2, HIDEN	TURNAROUND DELAY
15B	RETURN	615C		BU	15C	
53F	ENTER	6744	CTLRET6	BU	ERASE6	TRUNCATED POSTAMBLE
744	RETURN	0083	ERASE6	STO	WORK 1, X'83'	
36E	ENTER	8402	DRVUNTCK	ORI	STATIMG, SETSTATC	ALTERNATE PATH DEVICE BUSY
36F		63C0		BU	3C0, FREEAREA	
3C0		4428	FREEAREA	XFR	STATIMG, STAT	
3C1		3AC4	PPOLMTIX	BOC	STATC, TAG00	
3C2		3BCE		BOC	STATD, EXITPTCH	
3C3		63C1		BU	PPOLMTIX	
3C4		0002	TAG00	STO	WORK 1, RESET	
3C5		4060		XFR	WORK 1, TUBO	
3C6		000A		STO	WORK 1, DEVSEL+COMMD	
3C7		4024		XFR	WORK 1, TUTAG	
3C8		0000		STO	WORK 1, 0	
3C9		A000		ADD	WORK 1, 0	
3CA		4024		XFR	WORK 1, TUTAG	
3CB		A024	TAG002	ADD	WORK 1, 36	
3CC		21CB		BOC	NALCO, TAG002	
3CD		4050		XFR	COMITD	
3CE	RETURN	6370	EXITPTCH	BU	POLLMTIX	

* **Note 1**: *ENTER Enables the patch store for succeeding instructions, and RETURN Disables the patch store for succeeding instructions.*

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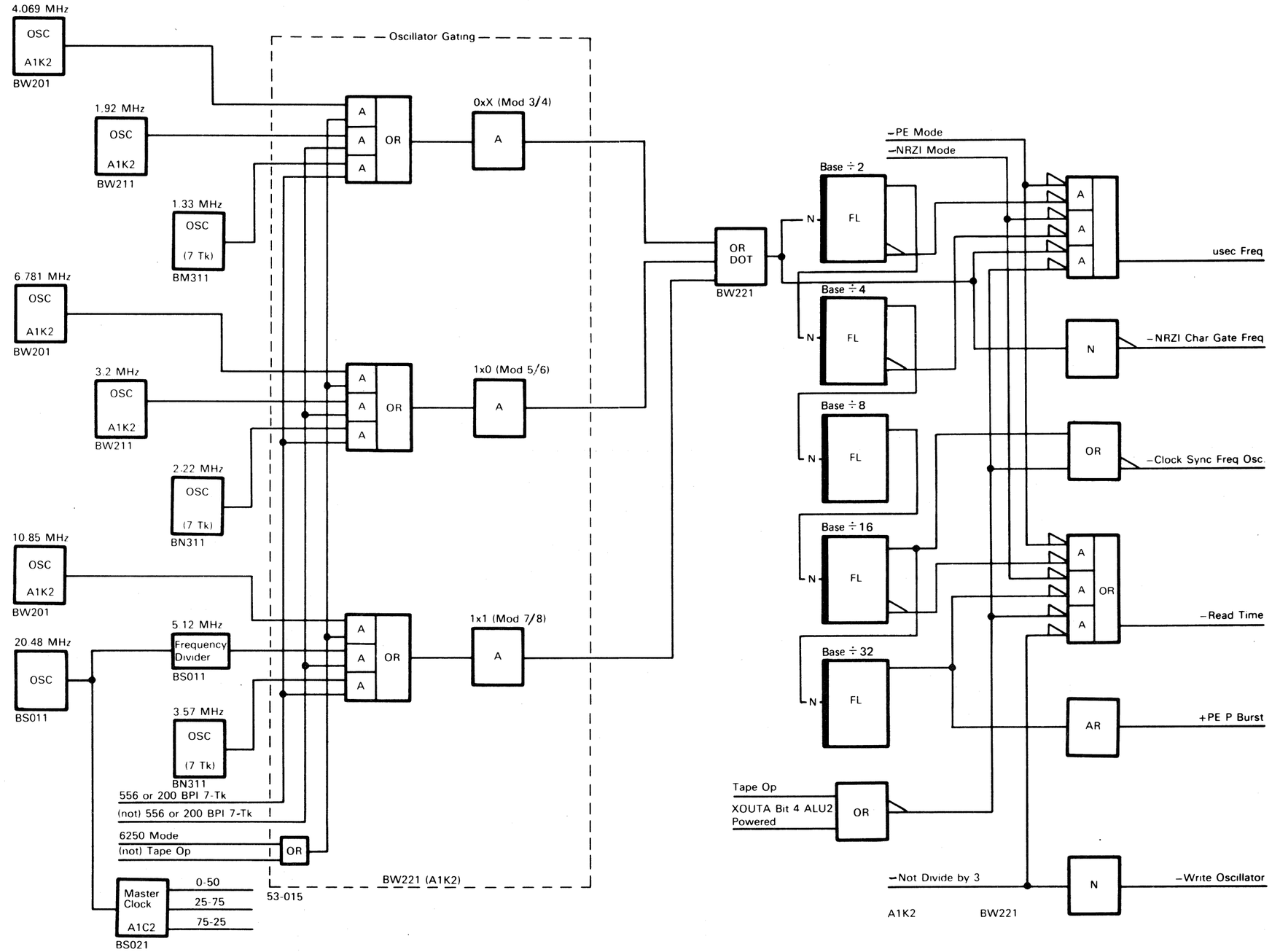
OSCILLATOR GATING

Crystal oscillators supply the basic timing pulses that drive the clocks and counters throughout the 3803.

The Microsecond Frequency used at any specific time depends on the speed of the tape unit addressed. The Detection Register gates the correct frequency.

The master clock controls the read clock stepping pulses.



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READ/WRITE CLOCKS AND COUNTERS

CLOCK/ COUNTER	ALD	CONTROL (Reset)	INPUT	OUTPUT	MLM PAGE	USE
Data Flow Clock	BS021	Tape Op	10.24 MHz	8 pulses *0 - 50 *25 - 75 *50 - 100 *75 - 025	53-015	Controls all data flow. *Plus 4 delayed pulses.
Write Clock	BW101	Wr Cond	usec Freq	WC0 - 11, WC0 - 15 (PE/NRZI)	53-020	Flip write triggers at WC7. Sample VRC at WC3 and 11 Step Write Counter at WC9 and 11.
Write Counter	BW091 BW101	XOUTA 4(6250)	WC9, WC11, WC5(PE)	Cntr 0 - 4	53-020	Gate Write Encoders BW011 - 051.
Byte Counter	BR041	Tape Op Repowered	75 - 25 Del	Set Byte 1 - 4	53-025	Gates CRC and Residual bytes.
Group Buffer Counter	CB441	Tape Op	ROC 25 - 75 or 0 - 25	Binary Counter 1, 2, 4	53-090	Group Buffer and 6250 Xlator Address Control.
CRIC	BR011	Wr Cyc Latch	75 - 25	CRIC 1 - 5	53-035	Channel Buffer Read In.
CROC	BR011	Rd Cyc Latch	75 - 25	CROC 1 - 5	53-035	Channel Buffer Read Out.
Frame Counters	CJ021	Counter Resets	PE Decode A6, C7, 25 - 75	Count = 8	--	Reset Valid Pointer and Hardware Pointer Latches.
Frame Buffer Counter	CH041	Tape Op	25 - 75	FB1, 2, 4 and Decode 0 - 7	53-095	Controls ECC Group Buffer Address, Error Matrix Switching, Data Correction, and Data Xfer to Channel Buffer.
Frame Buffer Format Counter	CH051	Tape Op Step Cntr Latch 75 - 25	75 - 25	Decode A, B, C, AB, ABC	53-095	Controls Format Clocks and Error Correction.
RIC (9)	CDx11	Tape Op or Dead Track	6250 Ones or Step RIC	Count 10 Ones or SKB Addr 0 - 31	53-080	Gates address to write bytes into Skew Buffer, and counts 10 ones (6250) or 10 zeros (PE) during preamble.
ROC (1)	CB411	Tape Op	Step ROC (RD3)	ROC 1 - 5	53-080	Gates address to read bytes out of Skew Buffer.
Microprocessor Clocks	AB011 AA011	Reset ALU IC	20.48 MHz	8 pulses at 0, 25, 50, 75, 100, 125, 150, 175 Nsec	52-005	Control microprocessor operations.

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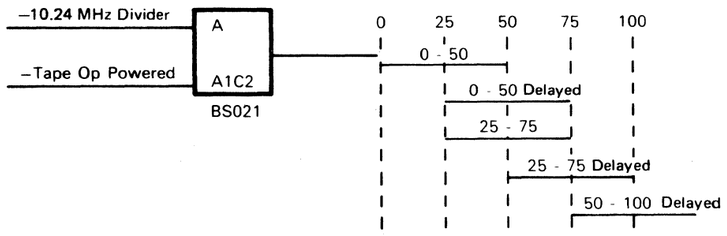
DATA FLOW CLOCK



Clock Output	ALD	Use
-0 - 50 Clock Bus YA	CD151 CD251 CD351 CH061 CH081	Skew and Master Clock Zone 1 Skew and Master Clock Zone 2 Skew and Master Clock Zone 3 Format Character Clocks Residual Frame Controls
-0 - 50 Clock Bus YB	CB411 CE101 CN281	ROC Counter S1 Register NRZI Hi Clip and Read VRC
-0 - 50 Delayed	BS051	Read Buffer Controls
-0 - 50 Clock Bus A1 Delayed	BN051 BR071	DC and Xlate Controls Cycle Request Latches
-25 - 75 Clock Bus YA	CD151 CD251 CH061 CH141	Skew and Master Clock Zone 1 Skew and Master Clock Zone 2 Format Character Clocks Modular 7 Residue Compare Equal
-25 - 75 Clock Bus YB	CB411 CD351 CN281	ROC Counter Skew and Master Clock Zone 3 NRZI Hi Clip and Read VRC
-25 - 75 Clock Bus A1 Delayed	BN071 BR071	Read DC and Xlate Control (7-trk Mode) Cycle Request Latches
-75 - 25 Delayed	BS051	Read Buffer Controls

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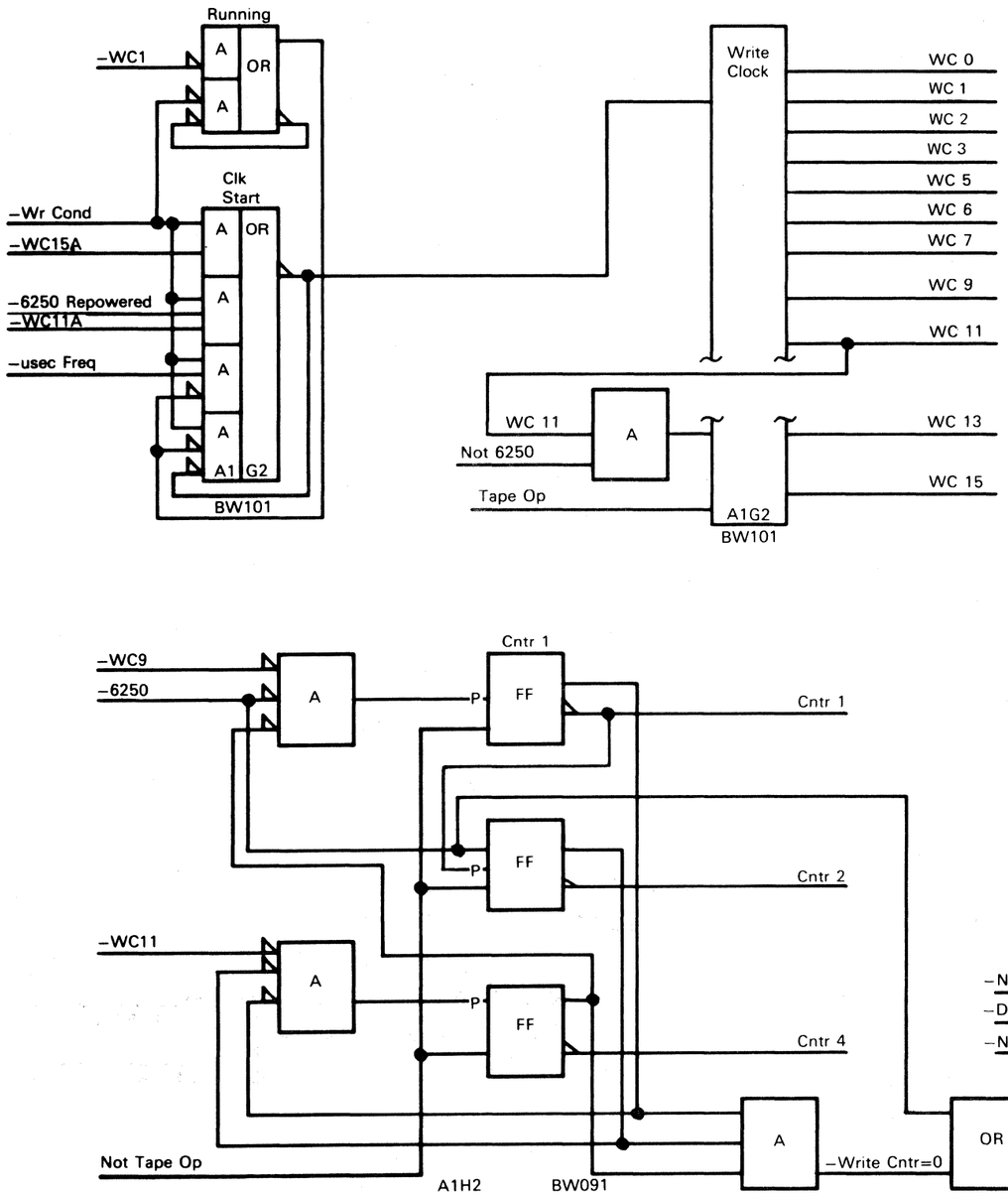
WRITE CLOCK AND WRITE COUNTER



Write Counter: Gates bytes to the write triggers.

WRITE CLOCK

WC Pulse	ALD	Use
0	BW151	Reset Error Sample. With CNTR=0, Gate Write Controls A1, A2, Mark1, Mark2, Format, Initiate Sample, All Ones Branch Condition.
1	BW161 BW151	Reset WRITE TIME GATE. With WRITE CNTR=0, flip CNTR B FF. (Write Group B Branch)
2	BW151	Gate SET 2ND BUFFER.
3	BW161	Sample WR TGR VRC.
5	BW091	PE Diagnostic Mode.
6	BW151 BW161	Set SAMPLE FL if CNTR 4 is On. Flip ODD/EVEN CHAR FF.
7	BW161	Generate WR TGR GATE if not NRZI.
9	BW091	Step WRITE COUNTER 1.
11	BW091 BW101 BW151 BW161	Step WRITE COUNTER 4 if 1 and 2 are off. Restart Clock (6250). Set Write Controls. Sample WR TGR VRC.
13	BW161	Set WRITE TIME GATE (PE and NRZI).
15	BW151 BW161 BW101	Gate SAMPLE SET trigger. Generate WRITE TRIGGER GATE. Restart Clock (PE and NRZI).

WRITE COUNTER

Wr Cntr	ALD	Use
0	BW151 BW151	With WC0, See WC0 Pulse. Gate END MARK FL. Gate CNTR B FL at WC1.
1, 2, 4A	BW011-051	Gate Write Encoder.
4	BW151	With WC6 and Not NRZI, Sample BUFFER EMPTY. With WC15 and NRZI, Sample BUFFER EMPTY.

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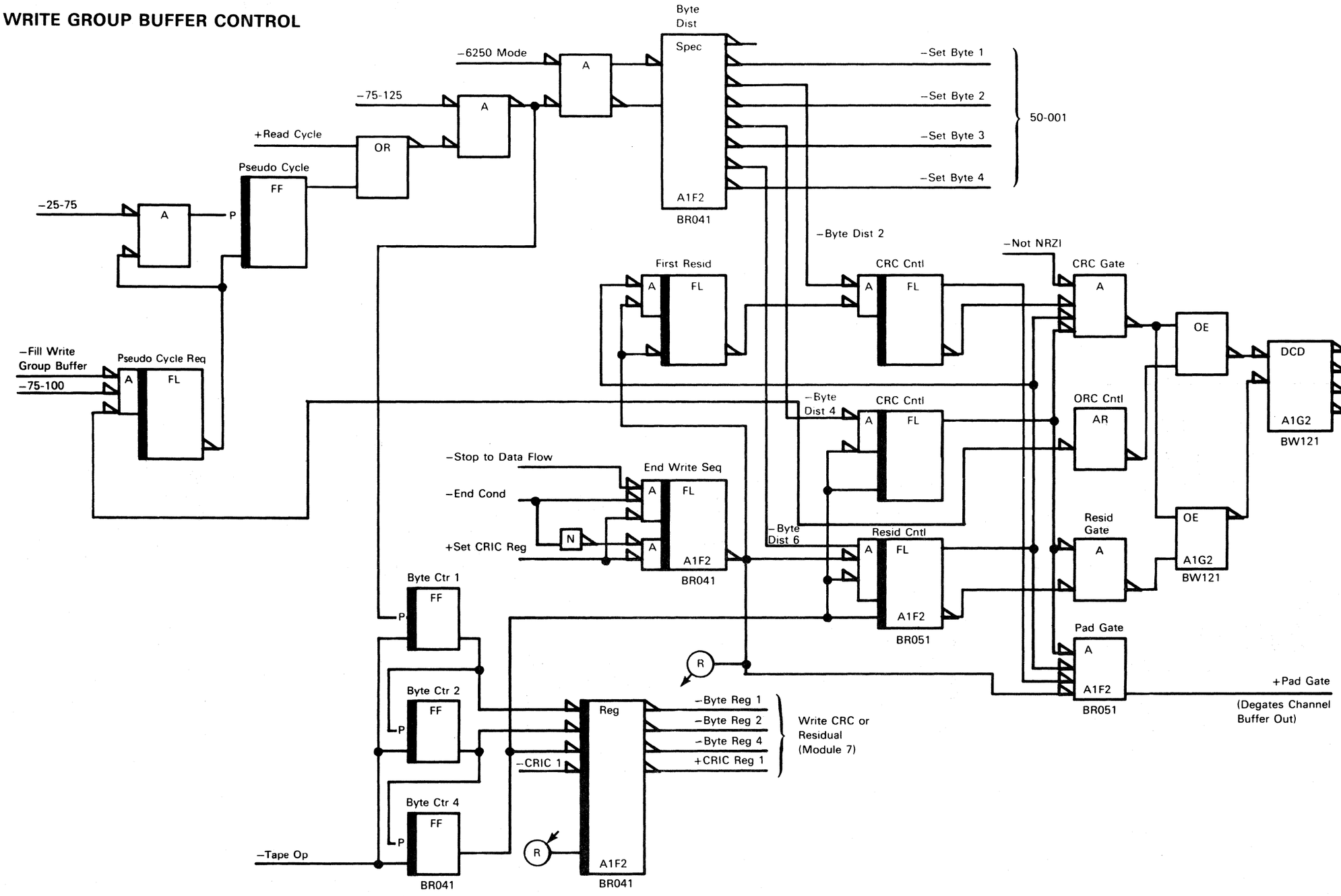
WRITE GROUP BUFFER CONTROL



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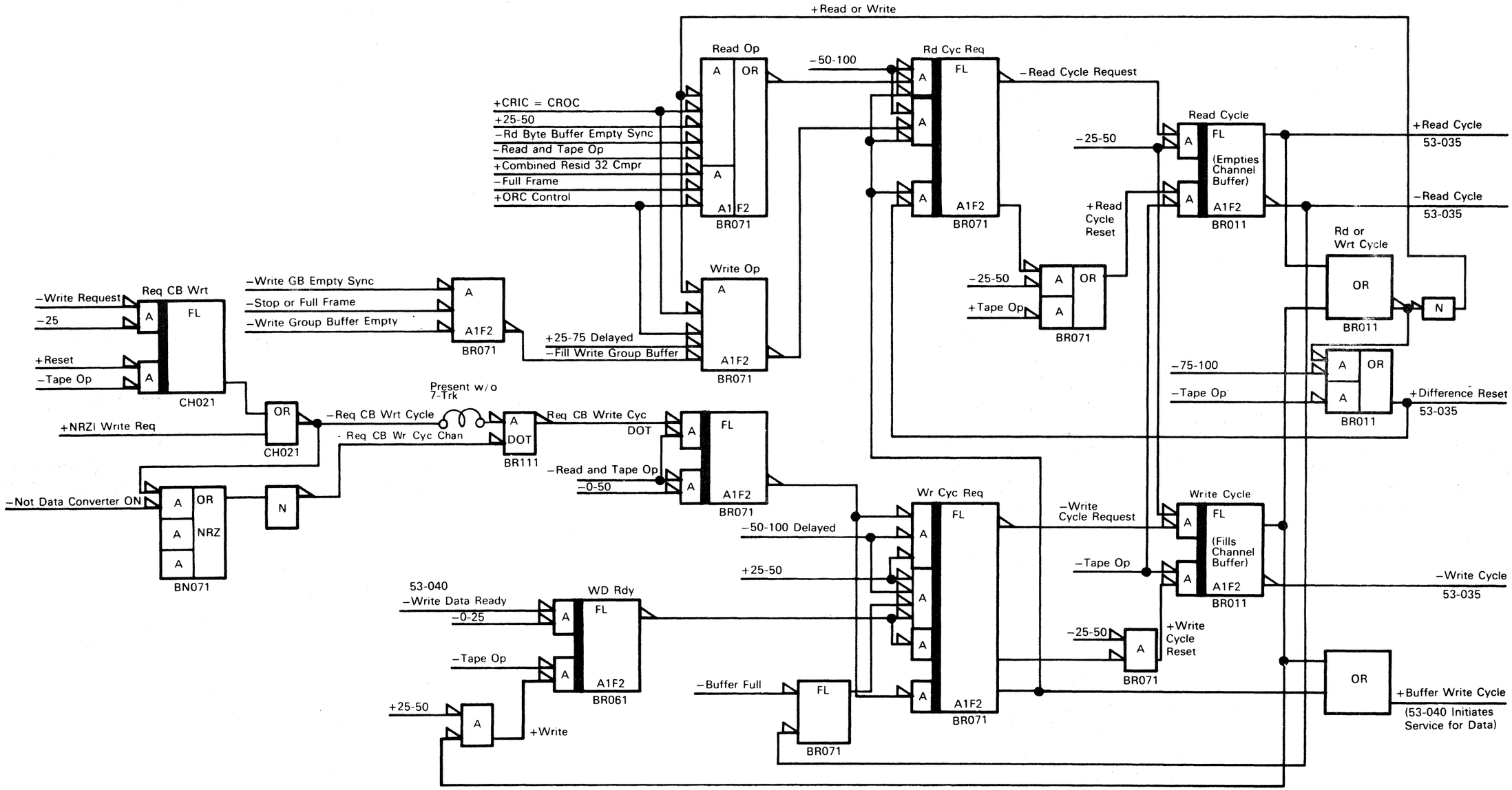
CHANNEL BUFFER CONTROLS



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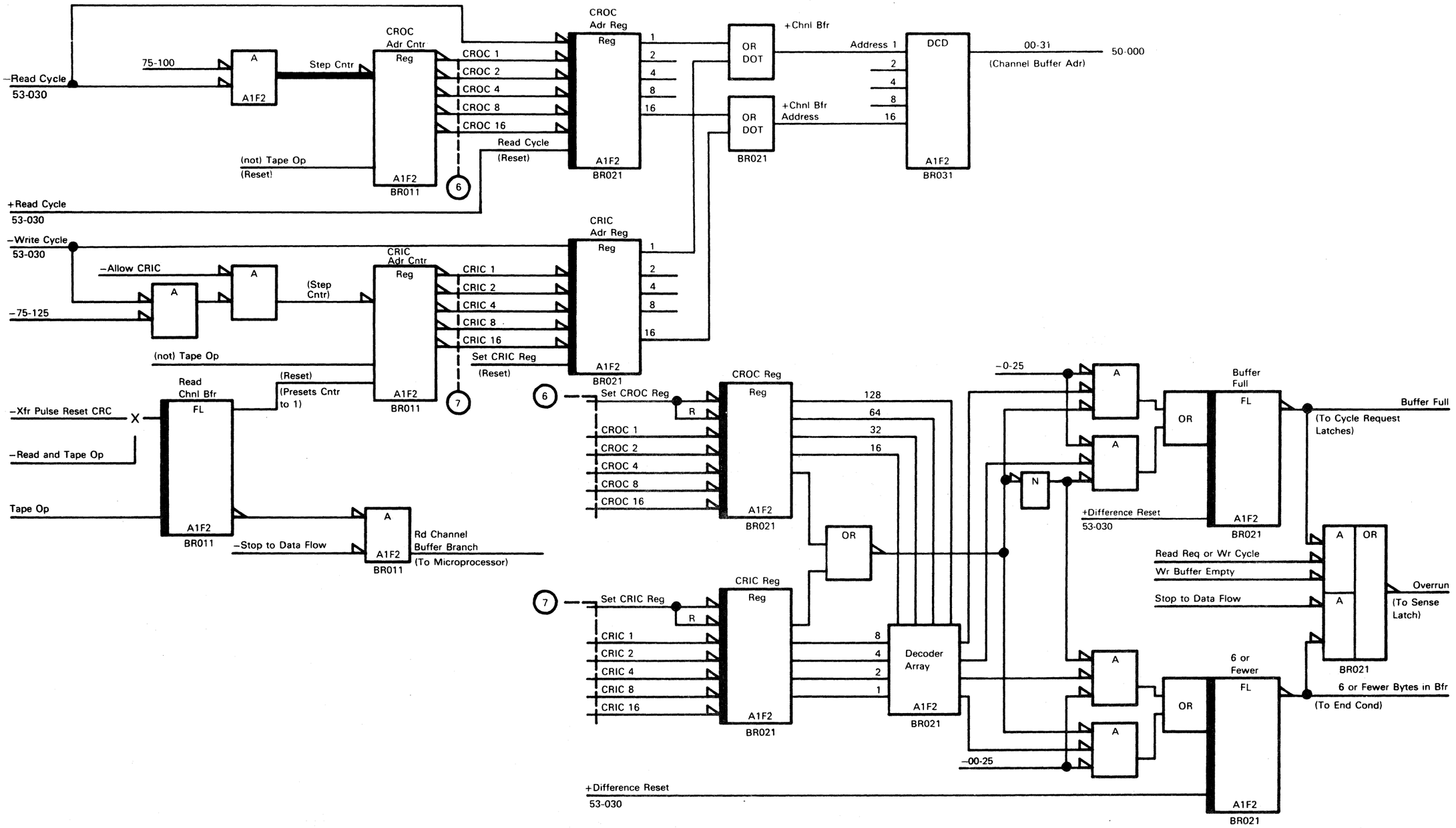

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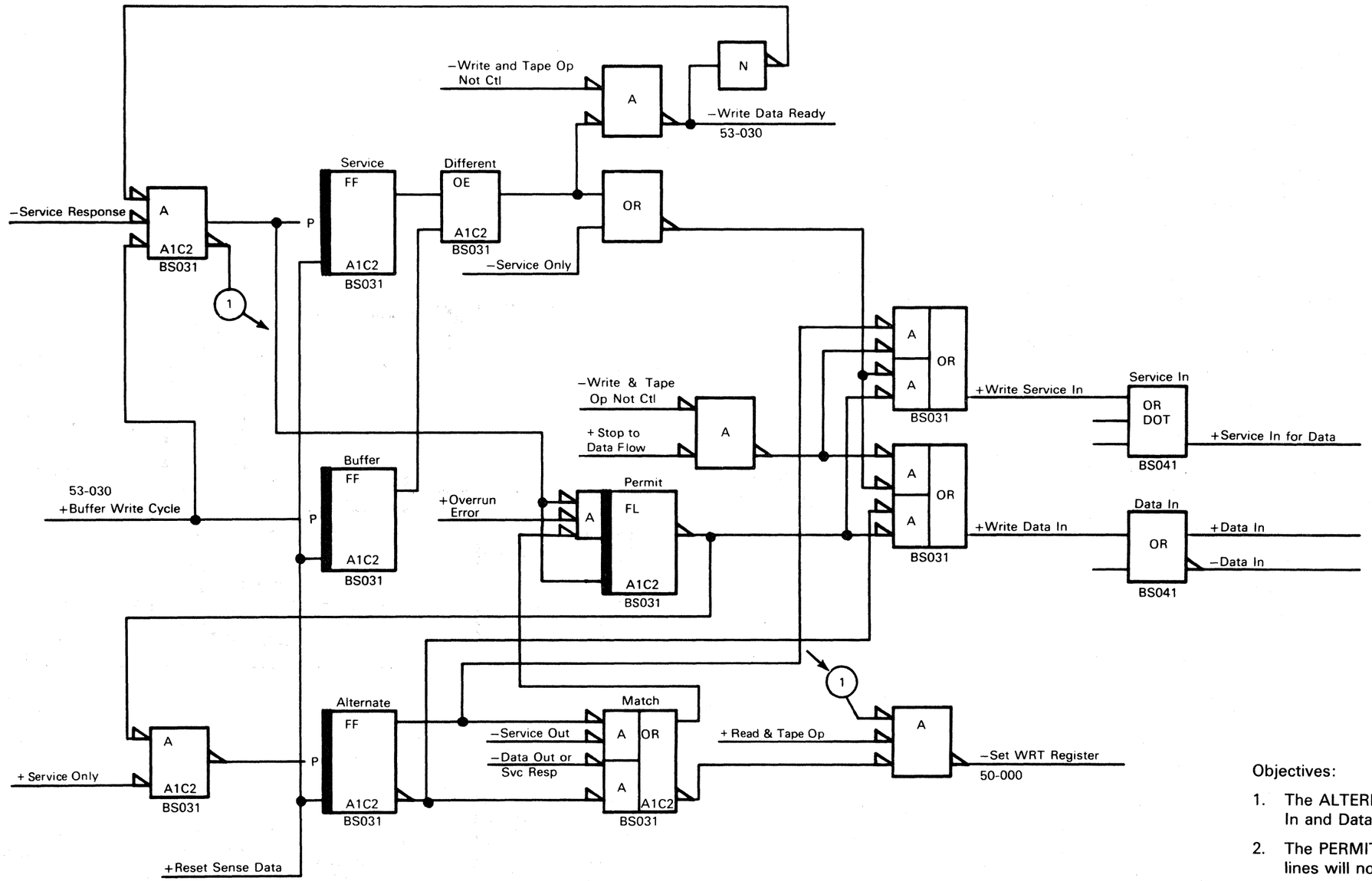
WRITE SERVICE CONTROLS



Objectives:

1. The ALTERNATE flip flop controls alternate Service In and Data In cycles.
2. The PERMIT flip latch ensures that multiple tag lines will not be active at the same time.
3. Buffer Write Cycle or Req controls Service Different and Buffer.

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XG2200 Seq 2 of 2	2735992 Part Number	See EC History	845958 1 Sep 79					

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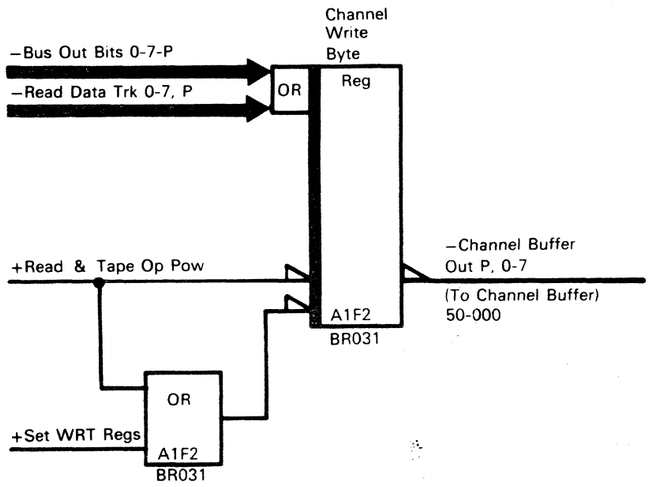
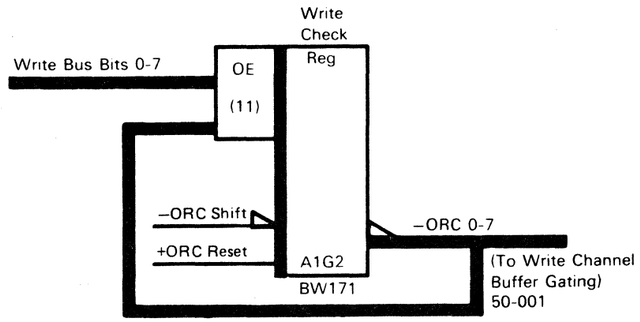
CHANNEL WRITE BYTE REGISTER



Objective:

This register is a temporary buffer for the channel buffer write byte from either interface bus out or read data track.

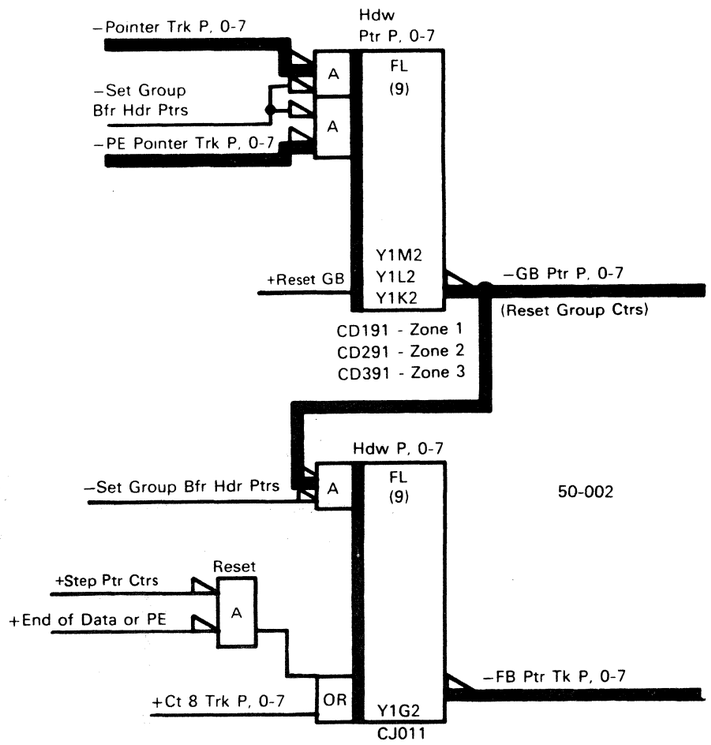
WRITE CHECK REGISTER



Objective:

An ORC byte character is generated for each ECC group.

POINTER REGISTERS



Objective:

The POINTER register accumulates the pointers for one group of 6250 data. These pointers are used for correction as required.

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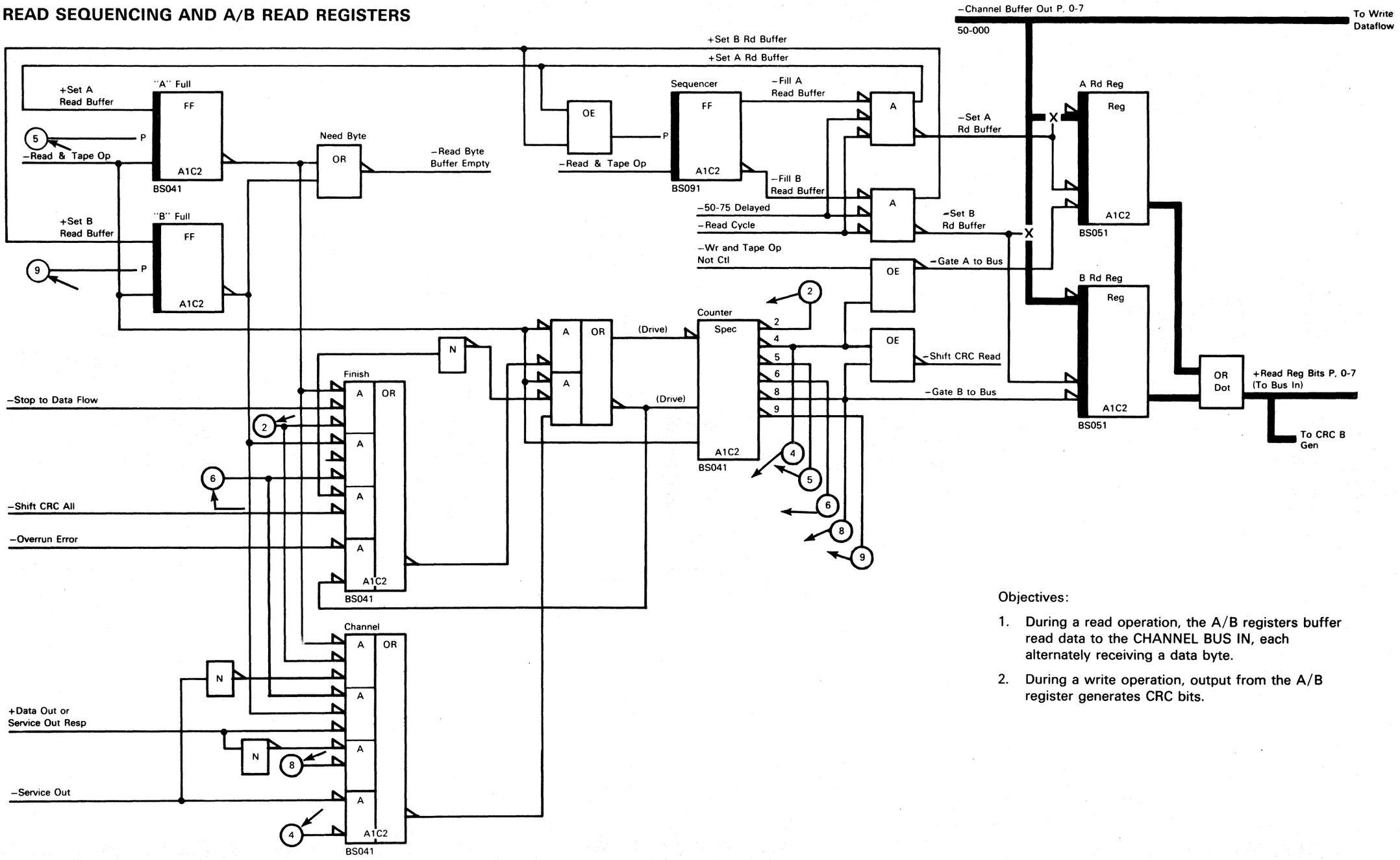
READ SEQUENCING AND A/B READ REGISTERS



Objectives:

1. During a read operation, the A/B registers buffer read data to the CHANNEL BUS IN, each alternately receiving a data byte.
2. During a write operation, output from the A/B register generates CRC bits.

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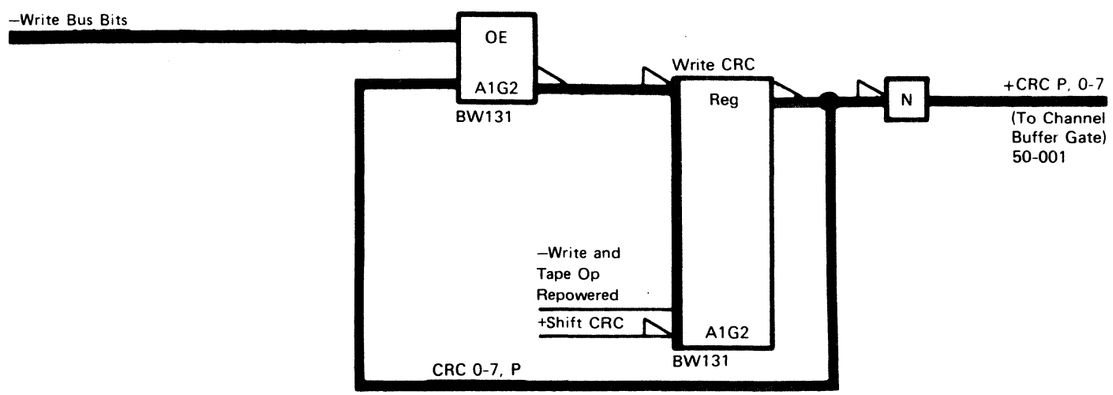
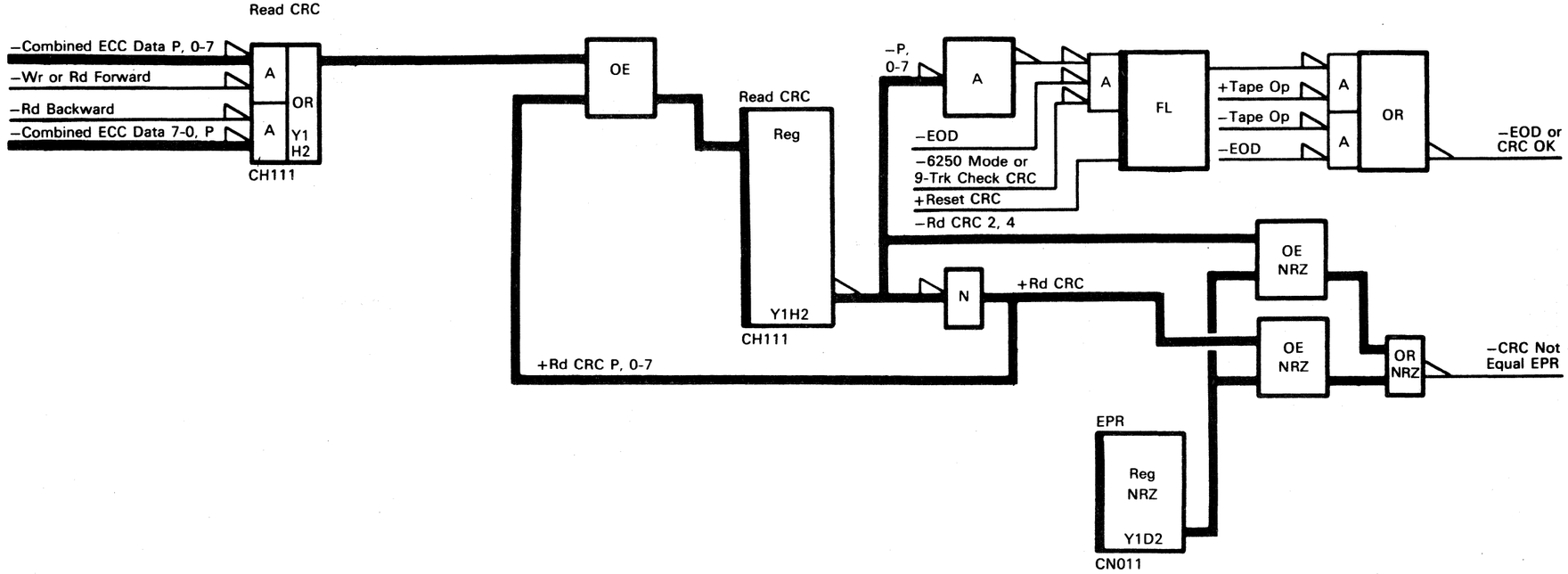
CRC GENERATORS





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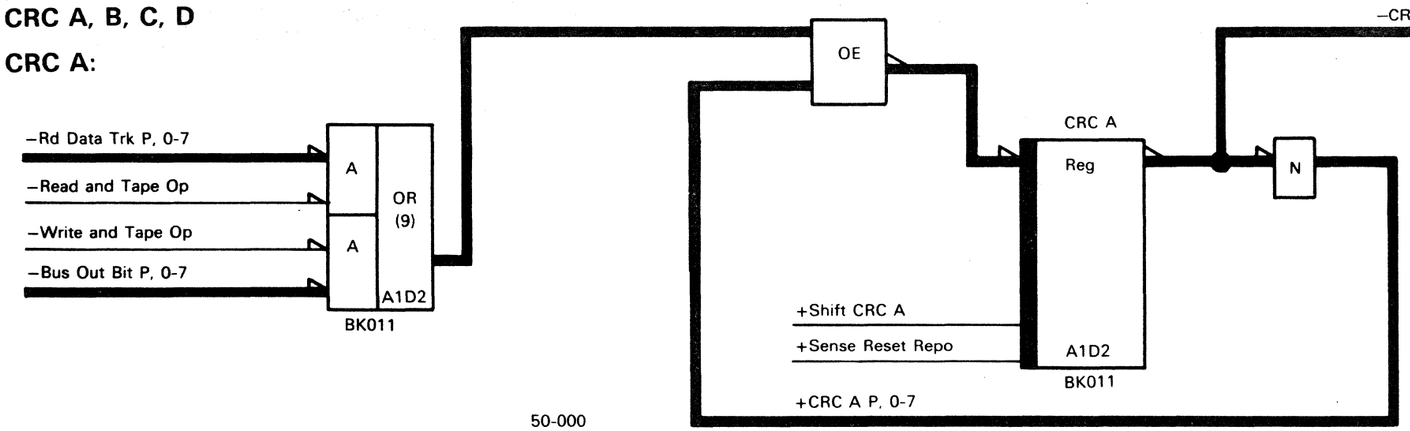
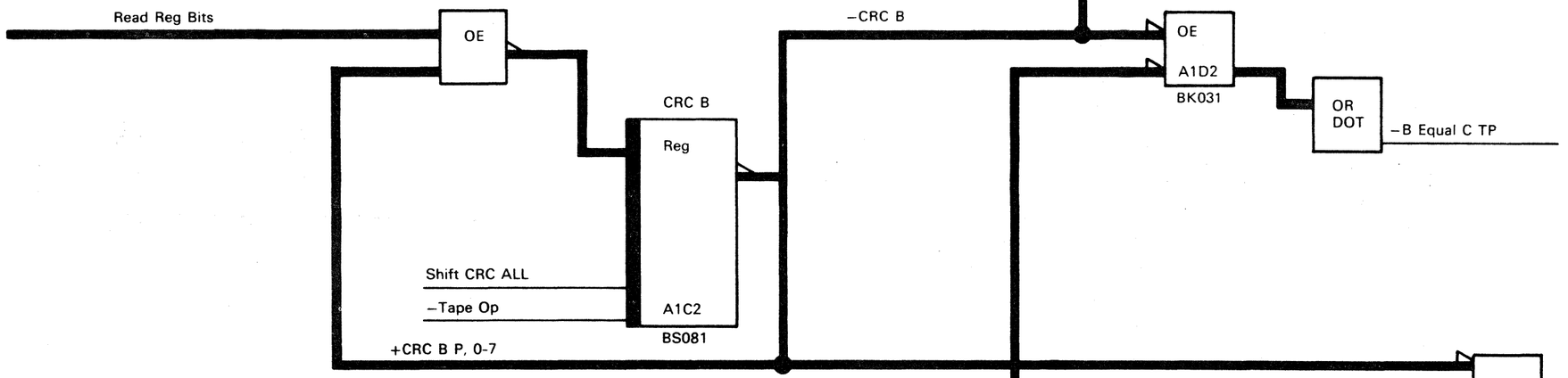
CRC A, B, C, D

CRC A:

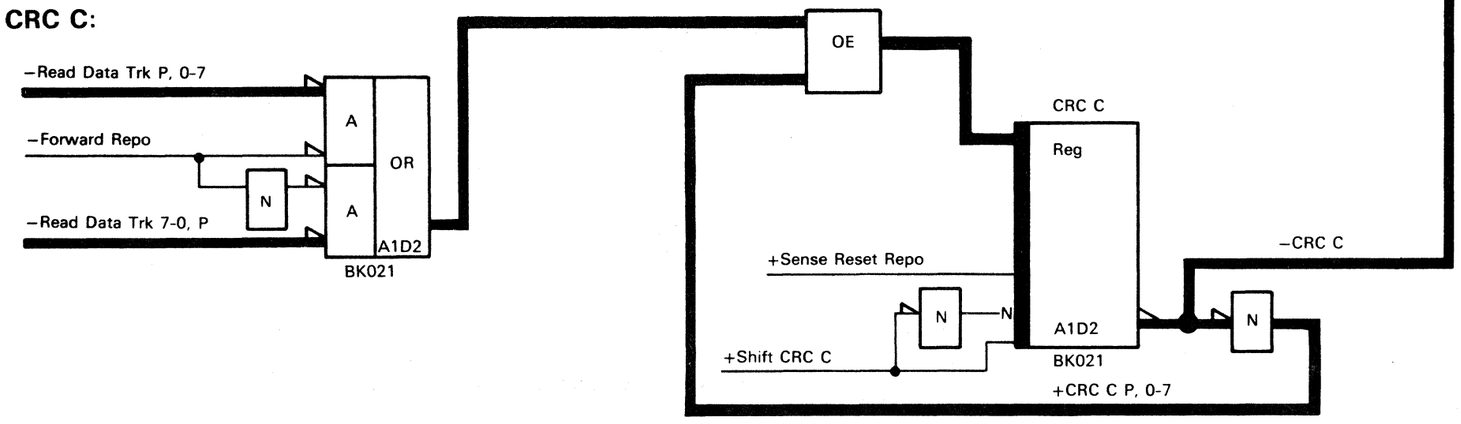


	6250	PE/ NRZI	Error	Sense
Write	A = B B = D	A = B B = C	P Compare CRC III	Byte 3, Bit 7 Byte 9, Bit 3
Read Fwd.	A = B B = D	A = B	P Compare CRC III	Byte 3, Bit 7 Byte 9, Bit 3
Read Bkwd.	A = B C = Match	A = B	P Compare CRC III	Byte 3, Bit 7 Byte 9, Bit 3

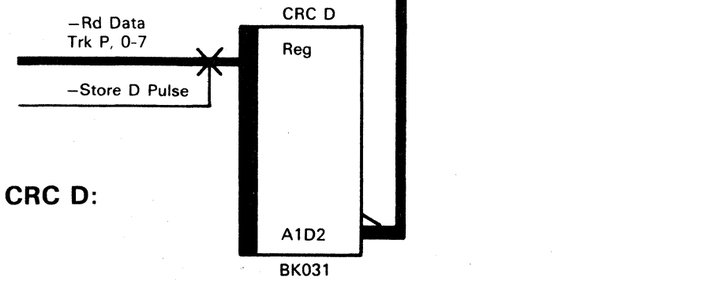
CRC B:



CRC C:



CRC D:



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CYCLIC REDUNDANCY CHECK (CRC) GENERATION

Two cyclic redundancy check (CRC) errors set sense bits. A CRC error sets sense byte 3, bit 3 and a CRC III error sets sense byte 9, bit 3. See 50-000, 50-001, and 50-002 for relationships to data flow.

CRC GENERATION DURING 9-TRACK WRITE OPERATIONS

Write data from the channel is shifted into the CRC A register (50-000), byte by byte, as the channel buffer is loaded. As the data is being read out of the channel buffer, the output is shifted into the CRC B register (50-000), as demanded by the write section. Accumulated contents of CRC A and CRC B registers are compared when the channel buffer empties (53-066). Dropping or picking up a bit or bits in transferring data through the channel buffer results in a mismatch and sets P COMPARE ERROR (byte 3 bit 7) and sense byte 9, bit 2.

a. 6250 bpi Mode

   The content of the CRC A register is written on tape as the CRC III byte. The CRC III byte is also shifted into the Write CRC generator (50-001) with data and other bytes. Content of the WRITE CRC register is also written on tape as a CRC byte.

b. PE Mode

   CRC III is generated during PE operations for write checking, but is not written on tape.

c. 9-Track NRZI Mode

   Only the accumulated data bytes generate the CRC byte.

CRC USE DURING READ BACK CHECK OF WRITE OPERATIONS

a. 6250 bpi Mode

   Data previously written is read back through the normal read data path and the Check CRC Byte is stored in the CRC D register (50-000). CRC D is compared with CRC B; a mismatch sets CRC III error and sense byte 9, bit 3.

   During the read back check, all data bytes and other bytes are shifted in the READ CRC register. The result should be a match pattern in the READ CRC register. Any other pattern sets CRC error only.

b. PE/9-Track NRZI Modes

   Only data bytes are read back and stored in CRC C register (50-000). Contents of CRC C register are compared with CRC B (53-066). A mismatch sets CRC III error and sense byte 9, bit 3.

c. 9-Track NRZI Mode

   All data bytes are read back and combined with the CRC byte in the READ CRC register (53-065). The accumulated bits should result in a match pattern. Any other pattern sets CRC Error.

CRC GENERATION DURING 9-TRACK READ FORWARD OPERATIONS

CRC generation during a read forward operation is similar to CRC generation during the read back check of a write operation. Data bytes read from tape go to the channel buffer (50-000) and also into CRC A register. CHANNEL BUFFER FULL initiates data transfer to the Interface Bus In and also shifts bytes into CRC B register. Accumulated contents of CRC A and CRC B registers are compared when the channel buffer empties (53-066). Dropping or picking up a bit or bits in transferring data through the channel buffer results in a mismatch and sets P COMPARE ERROR (byte 3 bit 7) and sense byte 9, bit 2.

6250 bpi Mode:

CRC generation and use during 6250 read operations is identical to CRC use during read back checking.

CRC GENERATION DURING 9-TRACK READ BACKWARD OPERATIONS

CRC generation detects the loss or gain of bits transferred through the channel buffer during both read backward and read forward operations.

6250 bpi Mode:

Read CRC error determinations are identical in 6250 read backward and read back checking operations except that bytes are shifted into registers in a reverse order.

The CRC C register accumulates combined data bytes and the check CRC bytes. With no read errors, the result should be a match pattern in the CRC C register. Any other pattern sets CRC III error and sense byte 9, bit 3.

7-Track NRZI operations do not use a CRC checking procedure.

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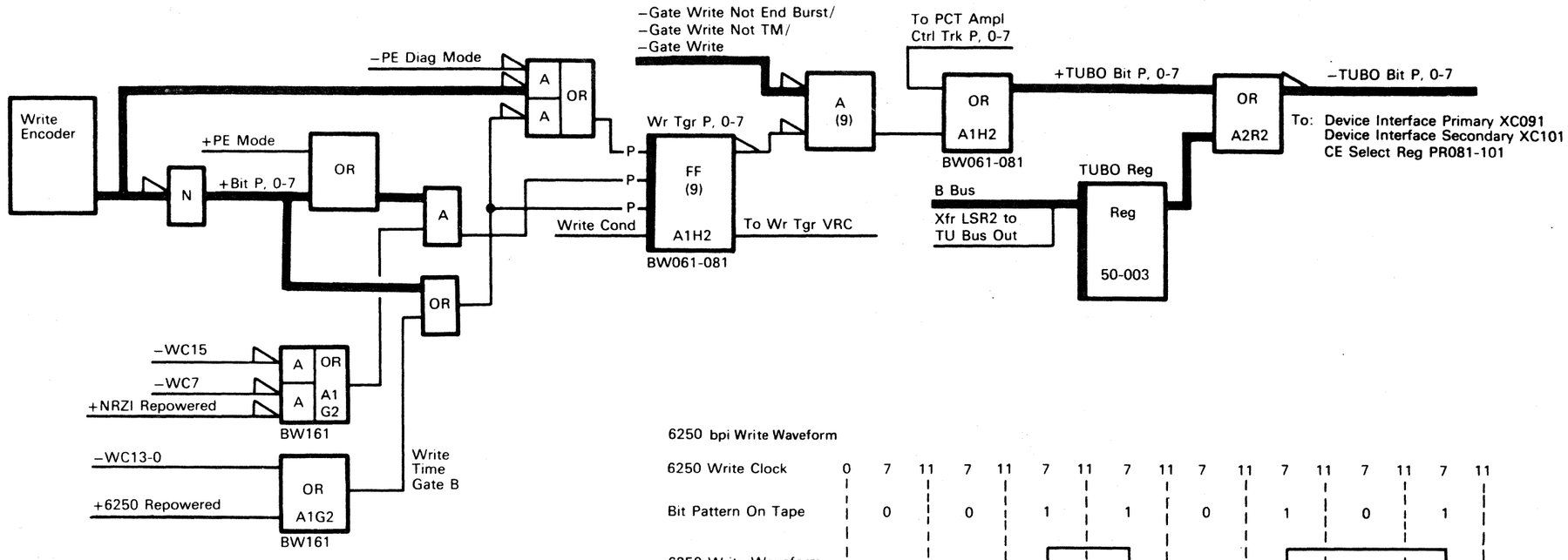
WRITE TRIGGERS



WRITE TRIGGER OPERATION

Data bytes from the CHANNEL BUS OUT consist of binary ones and binary zeros. The tape control and tape unit convert these binary bits to flux changes on tape. The 6250 bpi and NRZI methods of writing distinguish ones from zeros by a flux change for a one and no flux change for a zero.

Phase encoding (PE) distinguishes ones from zeros by the direction of flux change. A flux change in one direction indicates a one bit and in the opposite direction indicates a zero bit.

Write triggers produce magnetic flux changes on tape in one direction when they are flipped on and in the opposite direction when they are flipped off.

6250 BPI WRITE TRIGGER OPERATION

6250 bpi method of writing on tape flips the WRITE TRIGGERS at Write Clock 7 to write one bits on tape. The Write Clock runs to Write Clock 11 and then starts over.

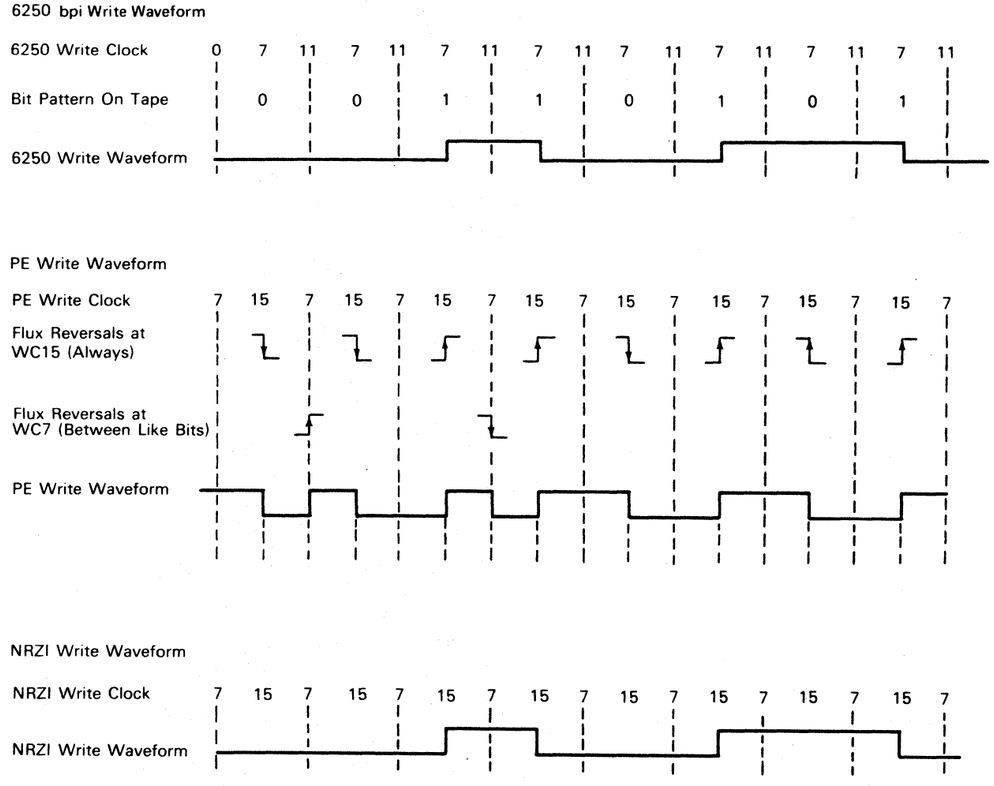
PE WRITE TRIGGER OPERATION

In PE operation, the write clock runs from 0 through 15 for each cycle.

Each byte is set into the write encoder. For each bit of the byte that is a one, the corresponding write trigger is "set up" at WC7. All write triggers are flipped at WC15 to write a byte on tape with flux reversals in one direction for one bits and in the opposite direction for zero bits.

NRZI WRITE TRIGGER OPERATION

For a NRZI write operation, each byte is set into the write encoder. For each one-bit of the byte, the corresponding write trigger is flipped to write a flux reversal on tape. For zero-bits of each byte, the write trigger is not flipped, and thus, no flux reversal is written.



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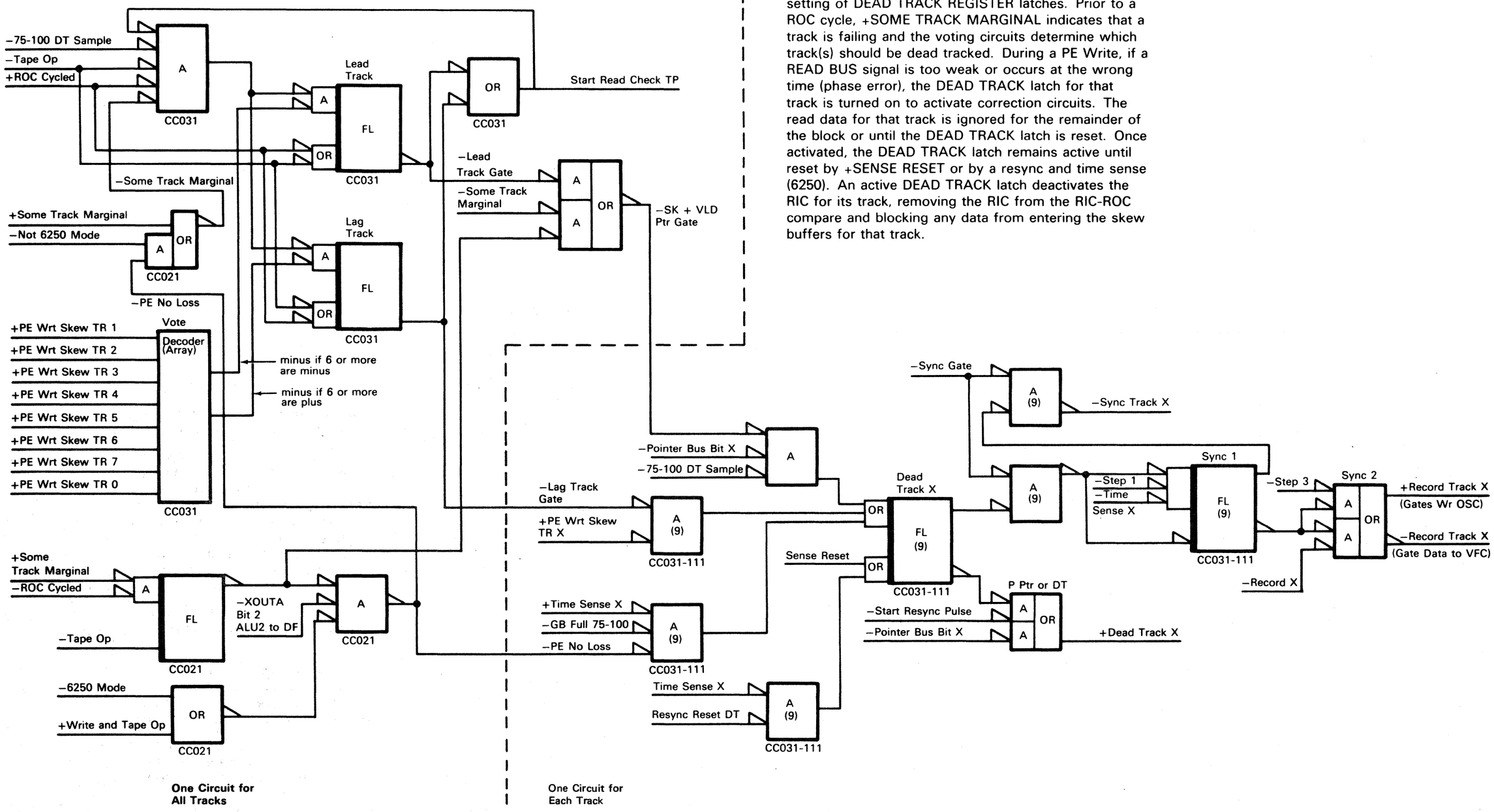
DEAD TRACK REGISTER



The DEAD TRACK register contains one latch for each track. After ROC has cycled, the Pointer Bus controls setting of DEAD TRACK REGISTER latches. Prior to a ROC cycle, +SOME TRACK MARGINAL indicates that a track is failing and the voting circuits determine which track(s) should be dead tracked. During a PE Write, if a READ BUS signal is too weak or occurs at the wrong time (phase error), the DEAD TRACK latch for that track is turned on to activate correction circuits. The read data for that track is ignored for the remainder of the block or until the DEAD TRACK latch is reset. Once activated, the DEAD TRACK latch remains active until reset by +SENSE RESET or by a resync and time sense (6250). An active DEAD TRACK latch deactivates the RIC for its track, removing the RIC from the RIC-ROC compare and blocking any data from entering the skew buffers for that track.

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RIC-ROC

The read section contains nine 32-position Read In Counters (RICs), one for each track, and one 32-position Read Out Counter (ROC).

A RIC specifies which skew buffer position receives the next one or zero bit for a data byte read from tape. When a bit is detected, it is placed in the skew buffer, and the RIC for that track is stepped to the next position.

The ROC selects the skew buffer position from which a byte is transferred to the group buffer.

Initially, all RICs and ROC are reset. As each bit of the first data byte enters skew buffer position 0, the corresponding RIC is stepped from 0 to 1. When none of the RICs are equal to ROC, RIC-ROC NO-COMPARE is activated, indicating that all bits of the byte have entered the skew buffer. RIC-ROC NO-COMPARE gates outputs of the ROC counter to the ROC image register and steps the Read Ready Counter, which times the read out of the skew buffer.

The operation continues in this manner until GROUP BUFFER FULL or IBG becomes active to stop the read out.

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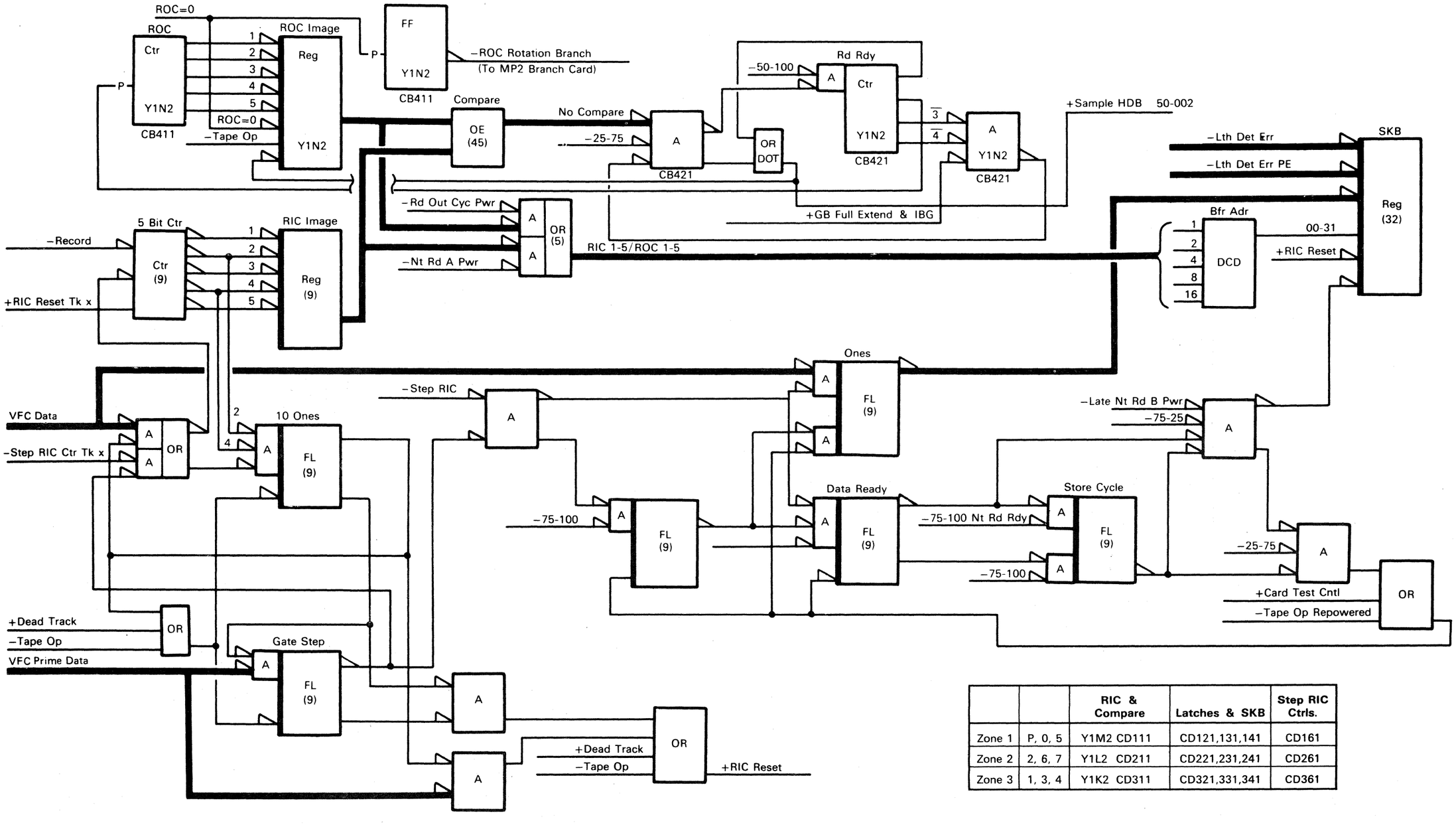
RIC-ROC



		RIC & Compare	Latches & SKB	Step RIC Ctrls.
Zone 1	P, 0, 5	Y1M2 CD111	CD121,131,141	CD161
Zone 2	2, 6, 7	Y1L2 CD211	CD221,231,241	CD261
Zone 3	1, 3, 4	Y1K2 CD311	CD321,331,341	CD361

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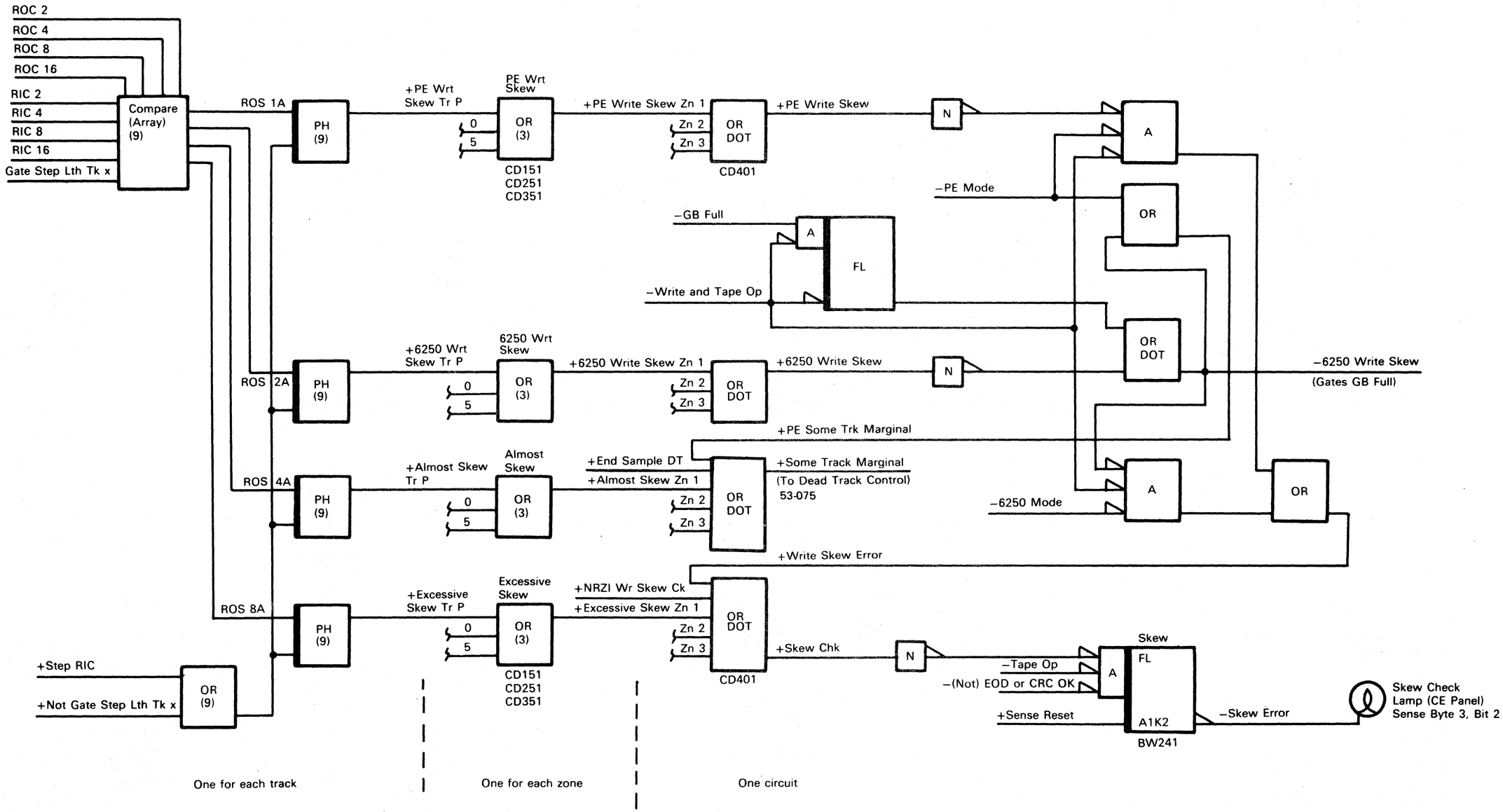
SKEW DETECTION



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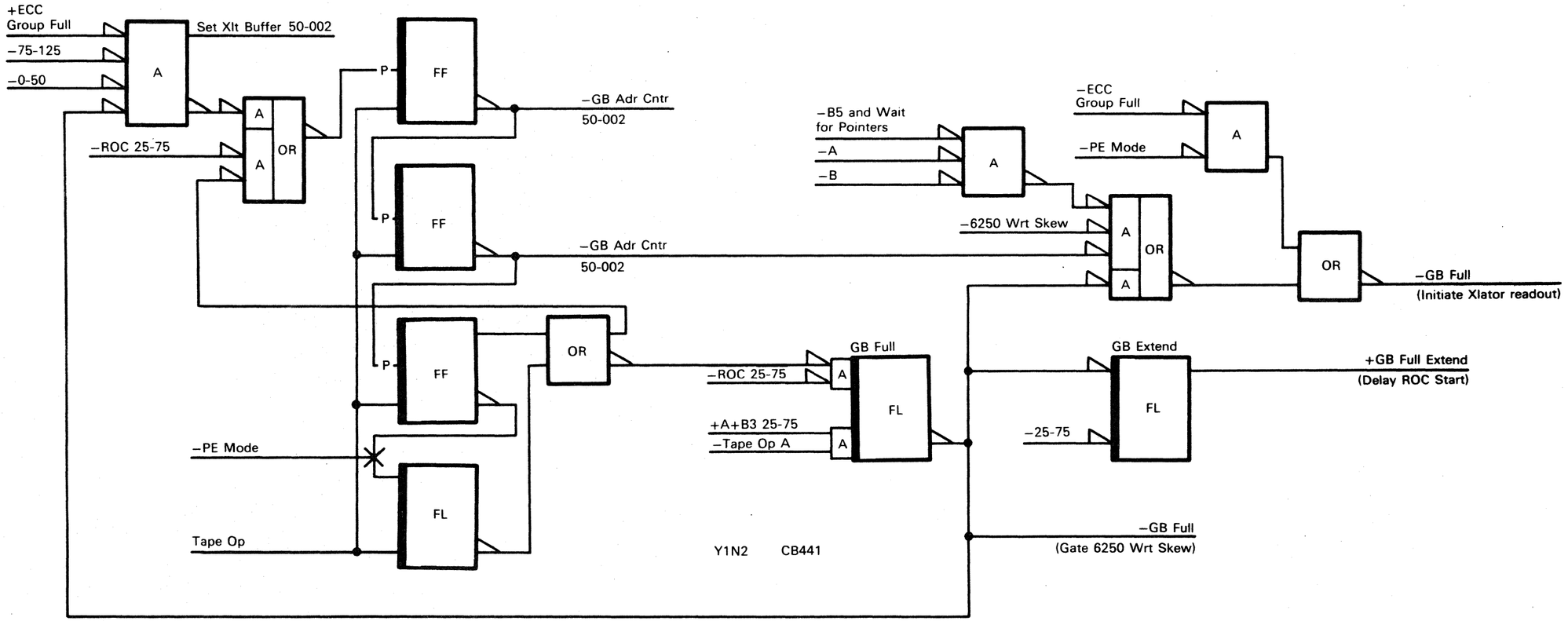
GROUP BUFFER COUNTER

Objectives:

1. Limits skew buffer read out to one 6250 group of data (5 bytes per group).
2. Controls skew buffer read out in PE Mode after the first five bytes are read out to give one-byte-in and one-byte-out control.
3. Controls translator operation during a group buffer read out to convert five parallel 6250 bytes into four serial data bytes.
4. Controls translator operation to detect 6250 characters and to decode format marks.
5. Group buffer counter counts to five and conditions translator for read out to ECC group buffer. If ECC group buffer is full, counter stepping is inhibited.



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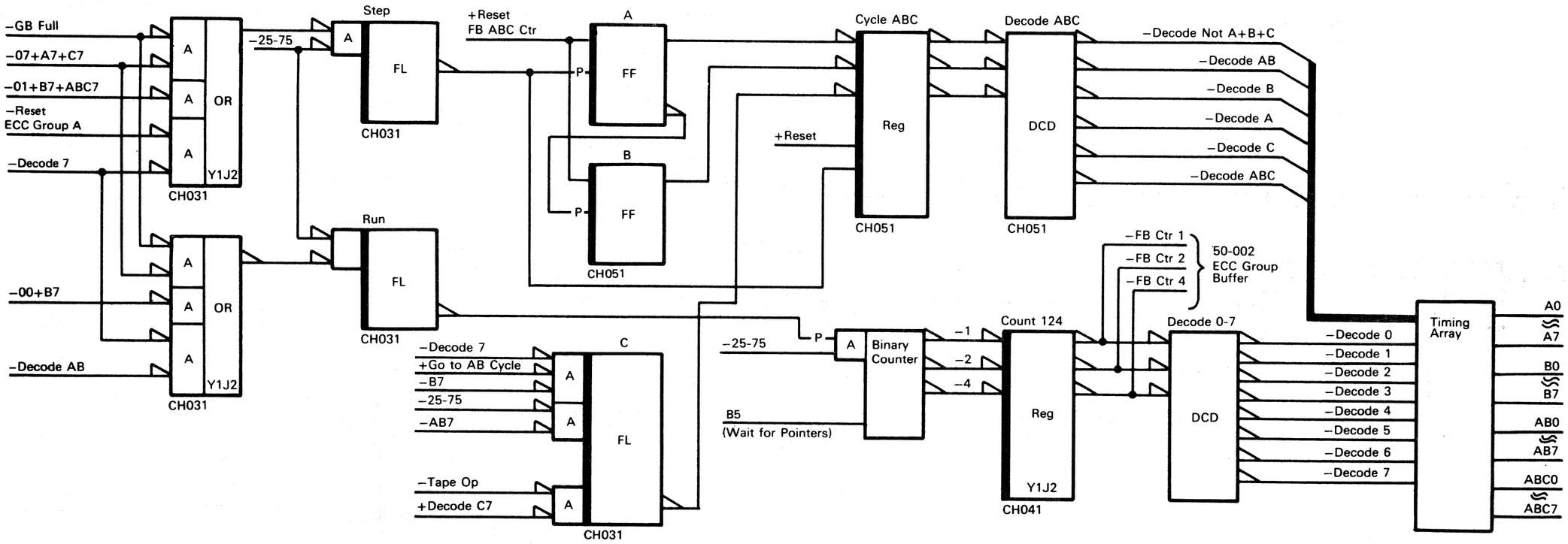
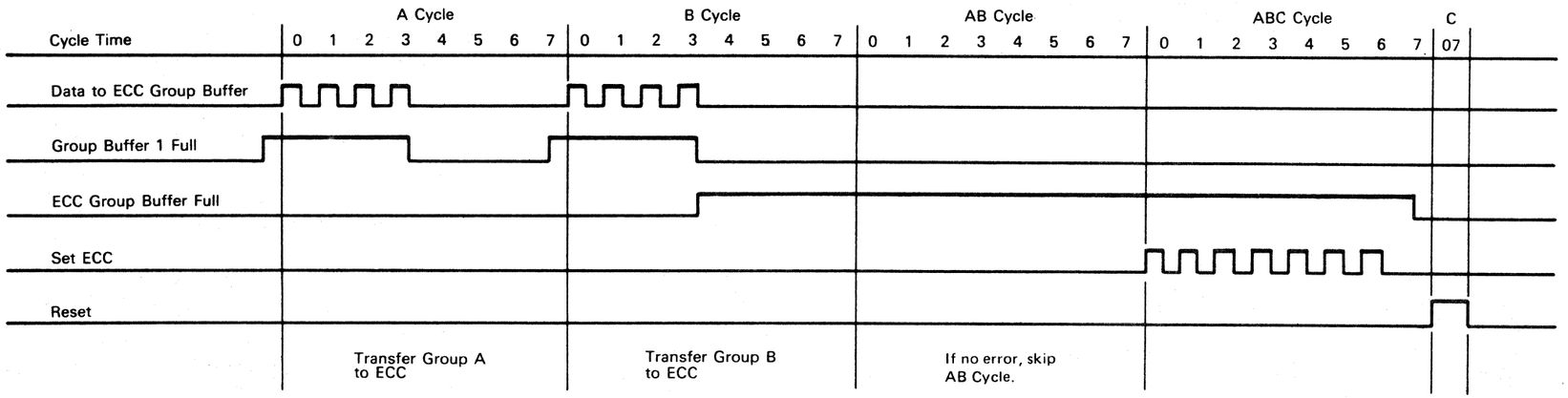
READ CYCLE CONTROLS





Clock is initialized with 00-07 only when TAPE OP becomes active.

Format Groups and PE mode use "A" cycles only.

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INITIAL SELECTION OF TAPE UNIT

DESCRIPTION

The initial selection sequence is the communication between the channel and tape control that initiates an operation.

During initial selection, the tape control obtains initial status information that indicates the availability of the selected tape unit. If the tape unit response indicates it is available, the tape control activates lines that tell the tape unit to perform a specific command. In response to the command, the tape unit furnishes additional status information that indicates its ability to perform the specified command. If the tape unit is capable of performing the command, the tape control activates MOVE to the tape unit.

The communication between the tape control and tape unit is over the device interface lines.

DEVICE INTERFACE LINES

The device interface is composed of the following lines that perform the listed functions:

BUS OUT (9 lines): Transmits commands, amplitude sensing levels, write data, and sense byte identification to the tape unit.

MOVE tag: Initiates tape motion.

COMMAND tag: In conjunction with BUS OUT, initiates the execution of a command.

CONTROL tag: In conjunction with BUS OUT, initiates the execution of a control command.

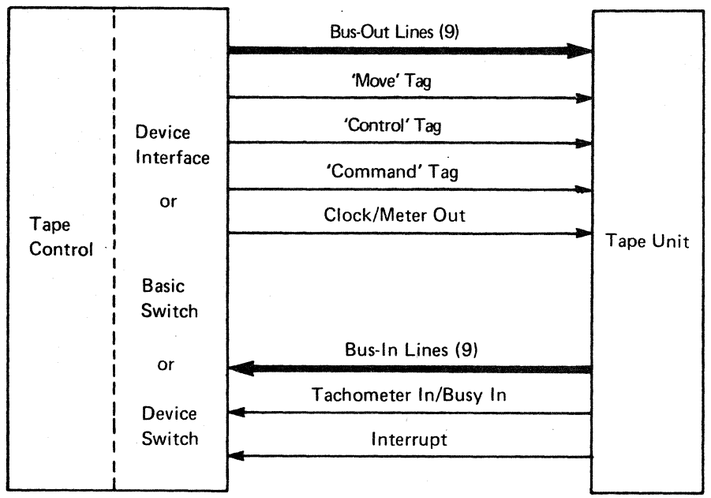
CLOCK/METER OUT: Causes the tape unit usage meter to run.

BUS IN (9 lines): Transmits status, sense information, and read data to the tape control.

TACHOMETER IN/BUSY IN: When no tag is active, this line indicates that the tape unit is busy. When any OUT tag is active, this line carries the capstan tachometer pulses to the tape control.

INTERRUPT: This line signals the tape control that one of the following unusual conditions has occurred in the tape unit.

- Load Check
- Loss of mechanical ready during a rewind
- Transition from not ready to ready status occurred
- Transition from ready to not ready status occurred while the MOVE tag was active
- BOT was sensed during a read backward operation



Device Interface Lines

BUS OUT Lines

BUS OUT Bit	COMMAND Tag Active	CONTROL Tag Active
0	Backward read	Rewind Unload
1	Forward read	Not used
2	Diagnostic (LWR)	(Mod 4, 6, 8 only) Diagnostic (set high sense)
3	Pulse	NRZI or 6250 bpi mode
4	Write	(Mod 4, 6, 8 only) Diagnostic (set low sense)
5	Set Extend Stop (Mod 4, 6, 8 only)	Data security erase
6	Reset error latches	(Mod 4, 6, 8 only) Erase Status
7	Not used	Rewind

BUS IN Lines

BUS IN Bit	COMMAND STATUS Byte	CONTROL STATUS Byte
0	Backward	Rewind Unload
1	Gap control	Not used
2	Diagnostic mode	(Mod 4, 6, 8 only) High Sense ON
3	(Mod 4, 6, 8 only) Opposite direction	NRZI or 6250 bpi mode
4	write status	(Mode 4, 6, 8 only) Low sense ON
5	Extended Stop (Mod 4, 6, 8 only)	Erase
6	Unit Check	(Mod 4, 6, 8 only) Erase status ON
7	(Mod 4, 6, 8 only) Positioning	Rewind

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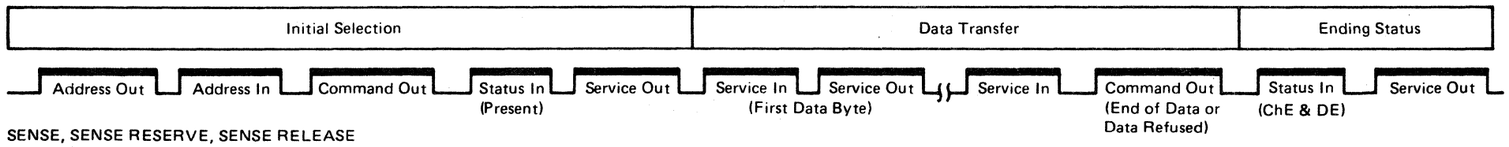
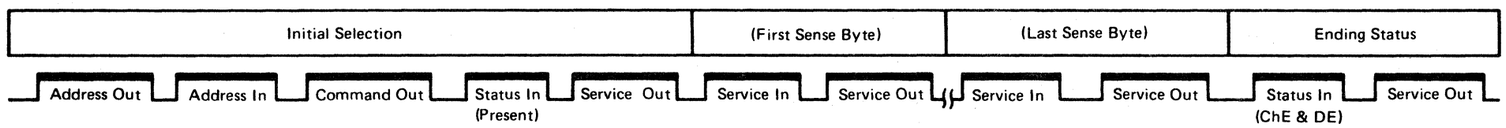
COMMAND SEQUENCE (TAG LINES/STATUS)

BURST COMMANDS

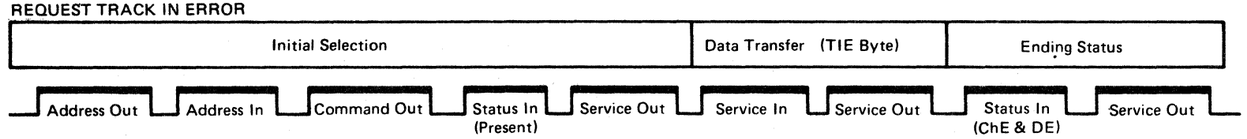
WRITE, LWR, READ, READ BACKWARD



SENSE, SENSE RESERVE, SENSE RELEASE

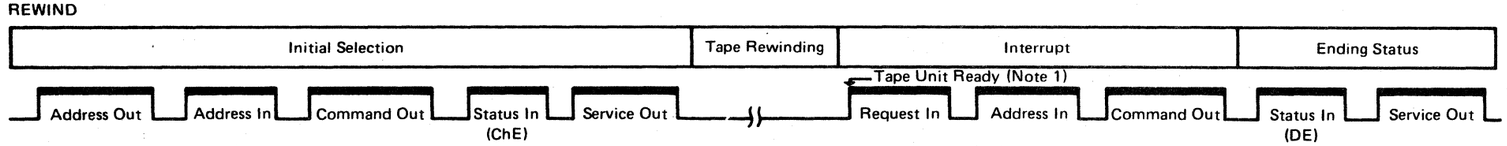


REQUEST TRACK IN ERROR

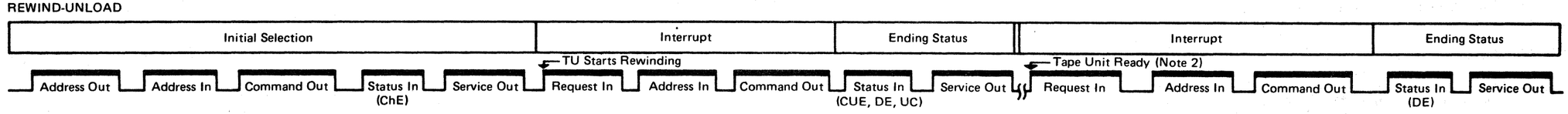


MOTION CONTROL COMMANDS

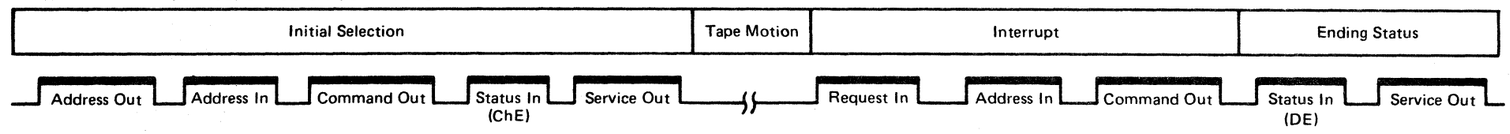
REWIND



REWIND-UNLOAD

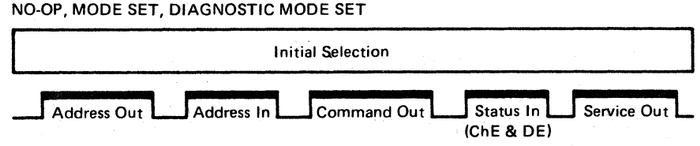


WRITE TAPE MARK, SPACE, ERASE GAP, DATA SECURITY ERASE



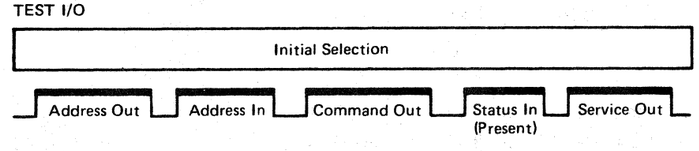
NON-MOTION CONTROL COMMANDS

NO-OP, MODE SET, DIAGNOSTIC MODE SET



INSTRUCTIONS

TEST I/O



Notes:

1. Request-in interrupt sequence initiated when 'rewinding' line goes from active to inactive state.
2. Request-in interrupt sequence initiated only if operator reloads and 'readies' tape unit to generate second 'device end.'

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TAPE CONTROL AND TAPE UNIT SELECTION

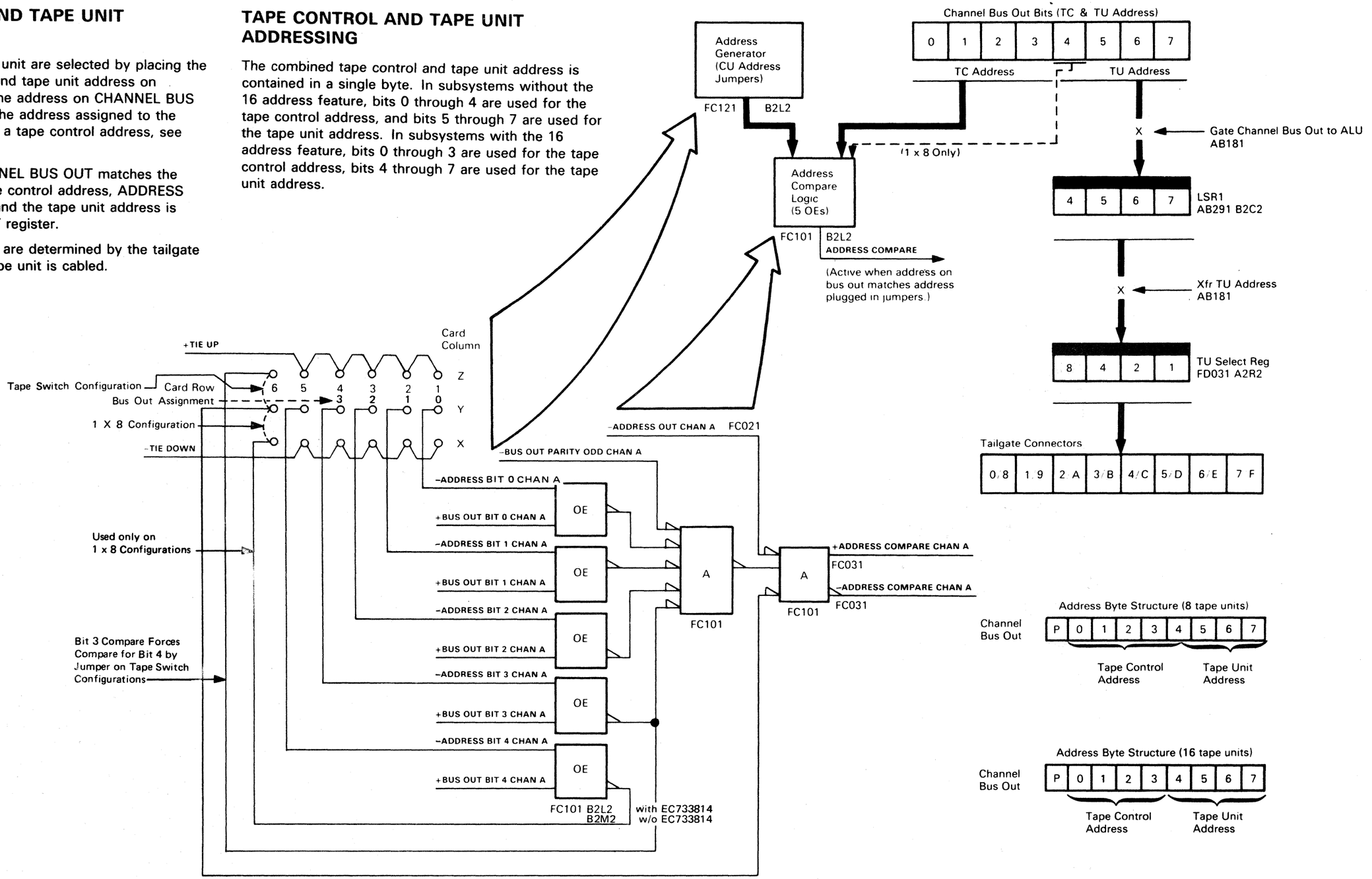
A tape control and tape unit are selected by placing the combined tape control and tape unit address on CHANNEL BUS OUT. The address on CHANNEL BUS OUT is compared with the address assigned to the tape control. (To assign a tape control address, see 90-110.)

If the address on CHANNEL BUS OUT matches the internally generated tape control address, ADDRESS COMPARE is activated and the tape unit address is gated to the TU SELECT register.

The tape unit addresses are determined by the tailgate position to which the tape unit is cabled.

TAPE CONTROL AND TAPE UNIT ADDRESSING

The combined tape control and tape unit address is contained in a single byte. In subsystems without the 16 address feature, bits 0 through 4 are used for the tape control address, and bits 5 through 7 are used for the tape unit address. In subsystems with the 16 address feature, bits 0 through 3 are used for the tape control address, bits 4 through 7 are used for the tape unit address.



3803-2/3420

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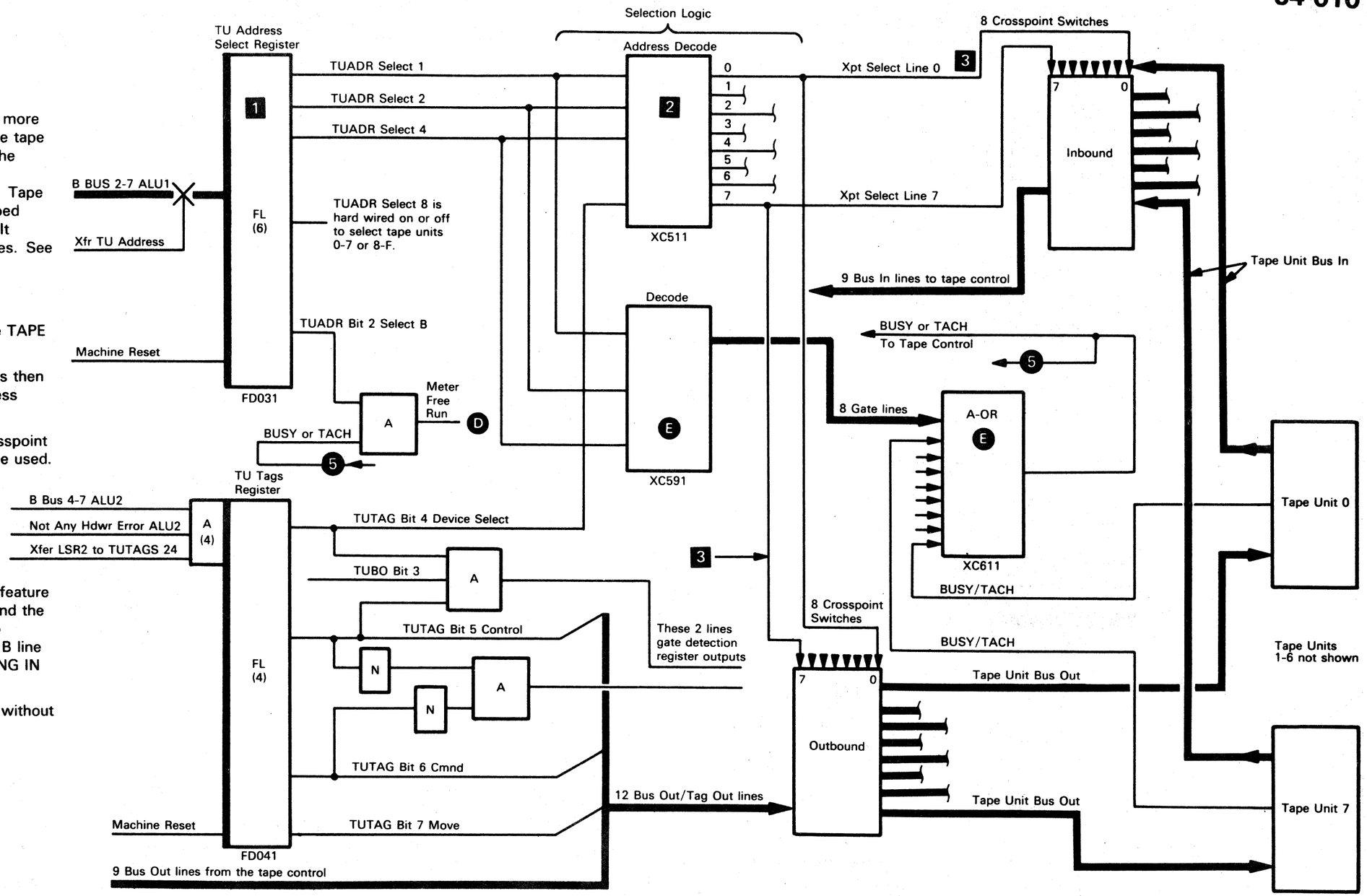
TAPE UNIT SELECTION LOGIC

TAPE UNIT SELECTION PRIORITY

On subsystems with a Device Switching feature, more than one tape control may try to access the same tape unit at the same time. To handle this situation, the switching logic has card jumpers that establish priorities for each tape control in the subsystem. Tape controls with device switching features are shipped with device selection priorities already plugged. It should not be necessary to change these priorities. See Section 90.

Tape Unit Selection

1. A four bit address on the B Bus is set in the TAPE UNIT ADDRESS SELECT register.
2. The inbound and outbound address decoders then decode ROS2's TUTAG BIT 4 and the Address Select lines.
3. One of eight select lines is active to the crosspoint switches to determine which tape unit will be used.



- D On machines with the Two-Channel Switch feature installed, the TUADR BIT 2 SELECT B line and the BUSY/TACH line generate METERING IN to channel B. The NOT TUADR BIT 2 SELECT B line and the BUSY/TACH line generate METERING IN to channel A.
- E This circuit interrogates a tape unit's status without selecting the tape unit.

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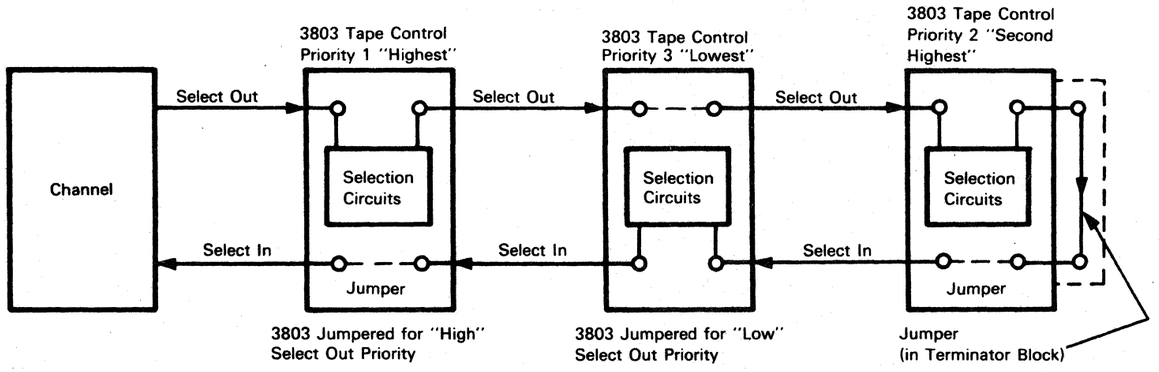
CHANNEL PRIORITY CIRCUITS

- 'Select out' priority determines the order in which tape controls are selected if more than one tape control requires service at the same time.
- A tape control's 'select out' priority is determined by jumpers in the tape control and by the tape control's location on the I/O interface.
- The select signal leaves channel on the SELECT OUT line and returns to channel on the SELECT IN line if it is not 'trapped' by a tape control requiring service.
- A tape control not requiring service propagates the select signal to the next lower priority tape control.
- Jumpers in each tape control determine whether the tape control will respond to the SELECT OUT line ('select out priority high') or the SELECT IN line ('select out priority low').
- All units shipped from the factory are jumpered for high 'select out' priority. If it is necessary to change the priority, see 90-120.
- Device Selection priority circuits are present in tape subsystems where a tape unit is accessed by more than one tape control. See 54-010. These circuits act as 'tie breakers' when two or more tape controls are trying to select a tape unit at the same time.
- Additional jumpers in the switching logic of each 'host' tape control establish device selection priorities (1, 2, 3, or 4) for each tape control in a tape switching configuration.



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NOTES:

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54-021

LOOP WRITE TO READ (LWR)

Loop write to read allows checking tape control and tape unit data and control paths without moving tape. The LWR (8B) command can be initiated from the processing unit or the CE panel. An LWR performed from the processing unit uses the same data path as a normal write operation. The following sense byte errors cannot be detected:

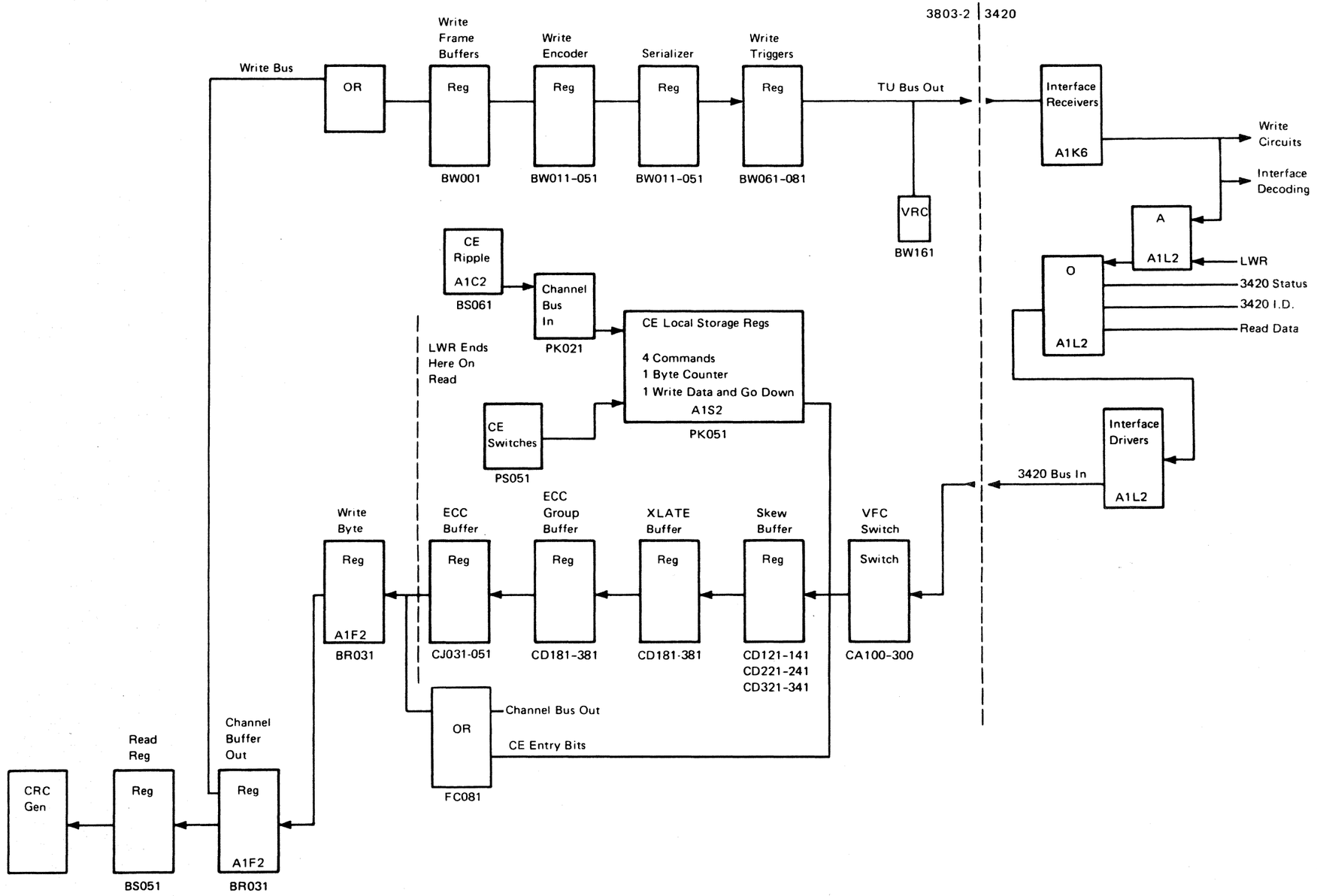
Data Checks:
- Early Begin Read Back check
- Early Ending Read Back check
- Slow Begin Read Back check
- Slow End Read Back check
- Velocity During Write check

Equipment Checks:
- No Block on Record Read Back check
- No Block Detected on WTM
- Velocity check
- Tach Start failure

A loop write to read operation is initiated from the CE panel by entering the command code (8B), and it receives its data from one of two locations. A count of service responses generates a ripple pattern, which is selected by putting the Command Control switch at the Ripple position. The fixed data comes from the Write Data switches when the Command Control switch is in the Write Data position. A CE panel LWR writes continuously until it is stopped by operating the Reset switch, except when the LWR with gaps jumper is installed (A1S2G08 to ground).

LWR TAPE UNIT OPERATION

The tape control activates SET DIAGNOSTIC and the COMMAND tag. The DIAGNOSTIC MODE latch is set in the tape unit (FT104). READ/WRITE GATE (FT104) ANDs with DIAGNOSTIC MODE to activate LOOP SELECT (FT147). The tape control activates the MOVE tag and drops the COMMAND tag, then the diagnostic latch degates Move command to prevent tape motion. LOOP SELECT active gates BUS OUT data back to tape control via the tape unit response lines.



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NOTES:

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55-006

BASIC RECORDING TECHNIQUE

DESCRIPTION

Three types of recording techniques are used in the IBM 3803-2/3420.

- Phase encoded (PE)
- Non-return to zero IBM (NRZI)
- 6250 bpi group coded recording (GCR)

Data bytes contain a combination of one and zero bits to represent binary ones and zeros. The PE tape system uses a flux change from minus to plus to represent a one bit, and a flux change from plus to minus to represent a zero bit. (The NRZI system uses a flux change in either direction to represent a one bit and lack of a flux change to represent a zero bit.) Flux changes on tape are created by changing the direction of current through the write heads by the write triggers.

PHASE ENCODED (PE)

(See Figure 1)

- At write clock (WC) 15, flip all write triggers to write ones or zeros on tape.
- To write a PE one bit, the write register is reset. Set up write trigger by setting it at WC 7 if not already on from previous byte so that write trigger can be reset at WC 15 (complemented).
- To write a PE zero bit, reset the write trigger at WC 7 so that WC 15 turns it on.

NRZI

(See Figure 2)

Flip write trigger at WC 15 to write one bits only. Do not flip write trigger to indicate a zero bit.

6250 BPI

(See 55-008)

MODE SET 1(SEVEN-TRACK NRZI OPERATION)

Mode set 1 commands sent to seven-track tape controls establish tape unit operating mode for succeeding seven-track NRZI operation. Bits 0 and 1 control density (556/800 bpi); and bits 2, 3, and 4 control parity (odd or even), data converter (on or off) and translator (on or off) circuits in the 3803.

A mode set 1 command affects operation of all seven-track tape units attached to the 3803. Unless reset, the 3803 retains its mode setting until it receives another mode set 1 command.

Mode set 1 commands sent to a 3803 without the seven-track features are treated as no-op commands, except that sense data bytes are reset (no-op reset sense). Channel end and device end are set during initial selection. 200 bpi mode set 1 commands (hex codes 13, 23, 2B, and 33) default to 555 bpi.

MODE SET 2 (NINE-TRACK PE/NRZI OPERATION)

Mode set 2 commands sent to PE/NRZI dual density tape controls set operating mode (1600 bpi PE or 800 bpi NRZI) for succeeding write or write tape mark (WTM) operations. Mode set 2 commands sent to a 3803 without the dual density feature are treated as no-op commands, except that sense data bytes are reset (no-op reset sense). Channel end and device end are set during initial selection.

DIAGNOSTIC MODE SET

A diagnostic mode set command causes an artifical signal loss condition that checks read and write error detection circuits.

- In PE mode, whenever write data contains successive one bits in any track, writing in that track is inhibited until the last one-bit is reached.
- In nine-track NRZI mode, no bits are written in track P.
- In seven-track NRZI mode, no bits are written in track C.

A diagnostic mode set command affects only write operations for the command in which it is issued. Channel end and device end are set during initial selection.

Note: For additional information, see 53-070.

Figure 1. Bit Cell and PE Write Waveform

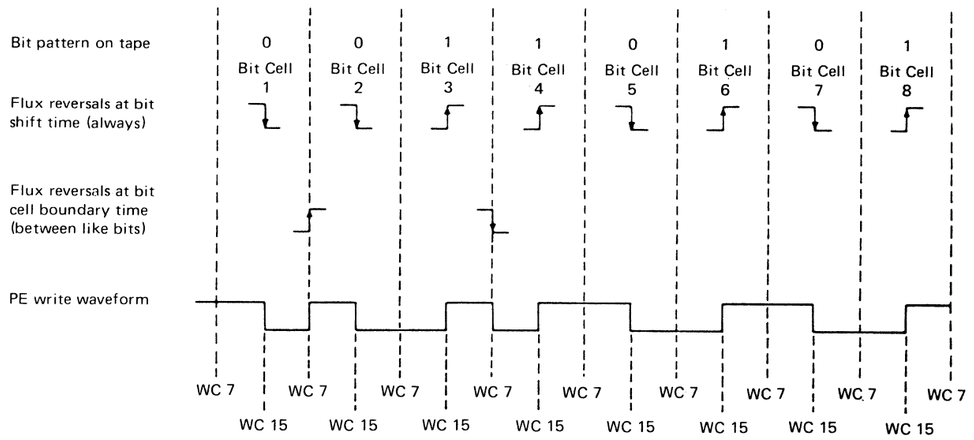
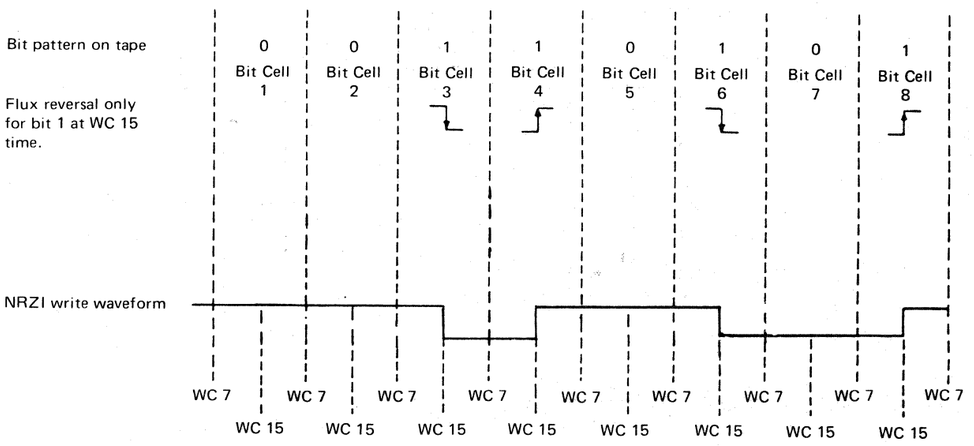


Figure 2. Bit Cell and NRZI Write Waveform



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55-007

GROUP CODED RECORDING (6250 BPI)

Group coded recording (GCR) offers many advantages over previously used recording methods. This recording offers higher reliability even with existing tape libraries. Greatly expanded error correction capability has been engineered into GCR. Higher data rates and lower access times give higher throughput, reduced channel time, resulting in higher system performance. Data is compacted on tape, reducing rewind times, shortening the length of tape required for a data set, reducing the number of reels, reducing mounts and dismounts, and improving overall tape handling.

The data is recorded in blocks, or groups of characters. A block of data may be a single character or byte, or a number of bytes as determined by the programming system used. The significant improvements in the GCR mode are:

1. The information data is recorded at an effective density of 6250 bytes per inch (bpi) of tape.
2. The separation between blocks (IBG) is 0.3 inches (7,6 mm).
3. Simultaneous errors in any two of the nine tracks are corrected automatically.

GCR BLOCK

A GCR block consists of a preamble, data, and a postamble (see 55-009). The preamble and postamble are each 80 bytes long and serve to synchronize the read detection circuits in a manner similar to previous 1600 bpi subsystems. The data portion of the block consists of the following:

1. Data to be written by the 6250 bpi feature is continuously collected in seven character groups (9 bits in each character) and is held in the control unit 6250 bpi feature circuitry. (see 50-000 through 50-002 for second level logic details.) An error correction character is generated and then added to the seven characters to make an eight character *data group*. This data group is then divided into two subgroups of four characters each. The four bits in each of the 9 tracks are encoded into five bits. (see Figure 1a through 1e.) This matrix of bits, 9x10, is recorded on the tape (see Figure 3a on 55-010).

Reading of the tape reverses the process, with error correction occuring where needed. There are as many of these 10 bit storage groups as there are multiples of seven channel data bytes in the record block.

2. The remainder, or last group of the channel data bytes (zero to six bytes) is encoded with whatever pad bytes are necessary, an auxilliary check character, and the error correction code (ECC) generated from these into a 10-byte residual group. This residual data group is created for every block recorded even though no residual bytes are found in the record. The auxiliary check character verifies read and write operations.
3. End of data (EOD) is signaled by a unique subgroup of five bytes immediately preceding the residual group.
4. Following the residual group, a 8-byte cyclic redundancy check (CRC) is encoded into a ten bit group. This group, with the auxiliary check character, ensures the integrity of the read and write operation, including verifying any error corrections that may have taken place.
5. Interleaved into the recorded block, every 158 storage groups, is a resync burst. This burst allows the tape control to put into full operation any track(s) that have lost synchronization or were dead tracked due to tape defects. The action limits dead tracking for greater throughput.

Figure 1a.

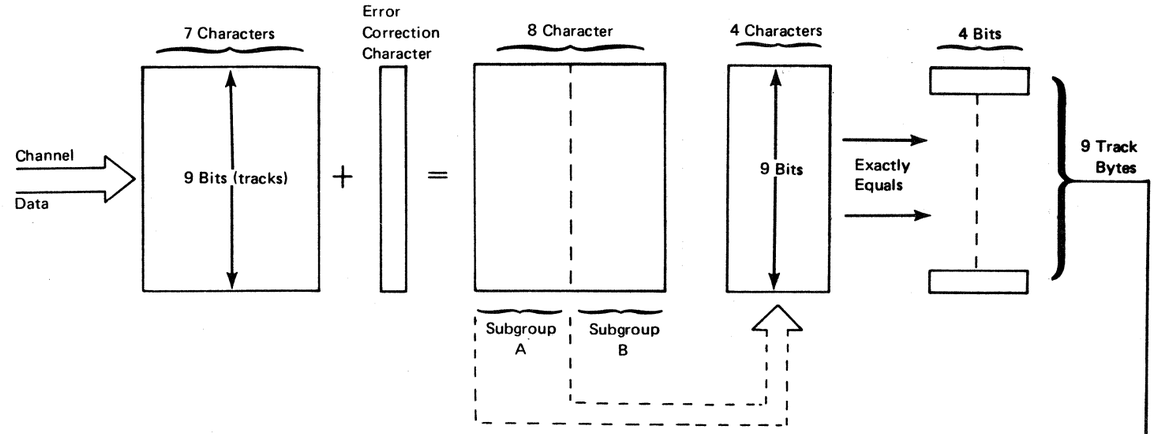

Figure 1b.

Figure 1c.

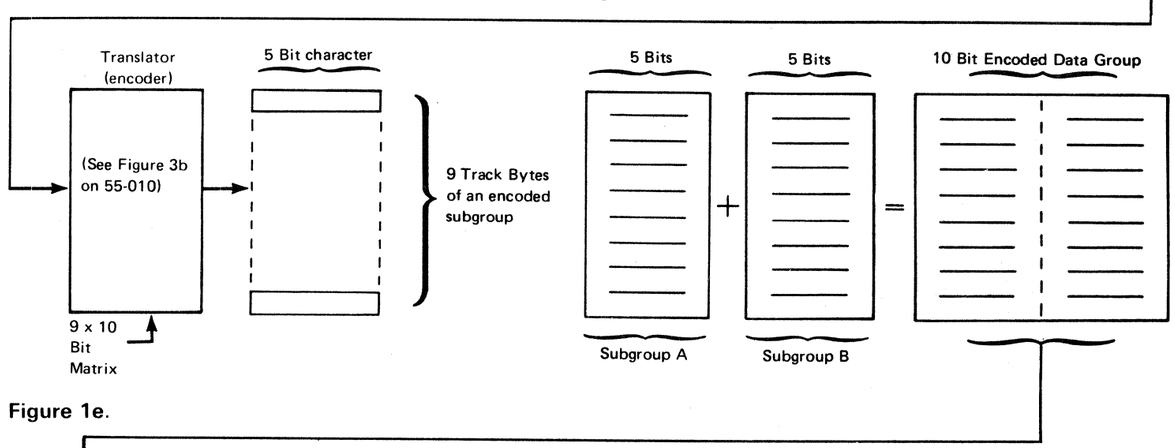

Figure 1d.

Figure 1e.

Note: There are 1106 bytes of channel input data in each 1580 (6250 bpi) group recorded data block written on tape.

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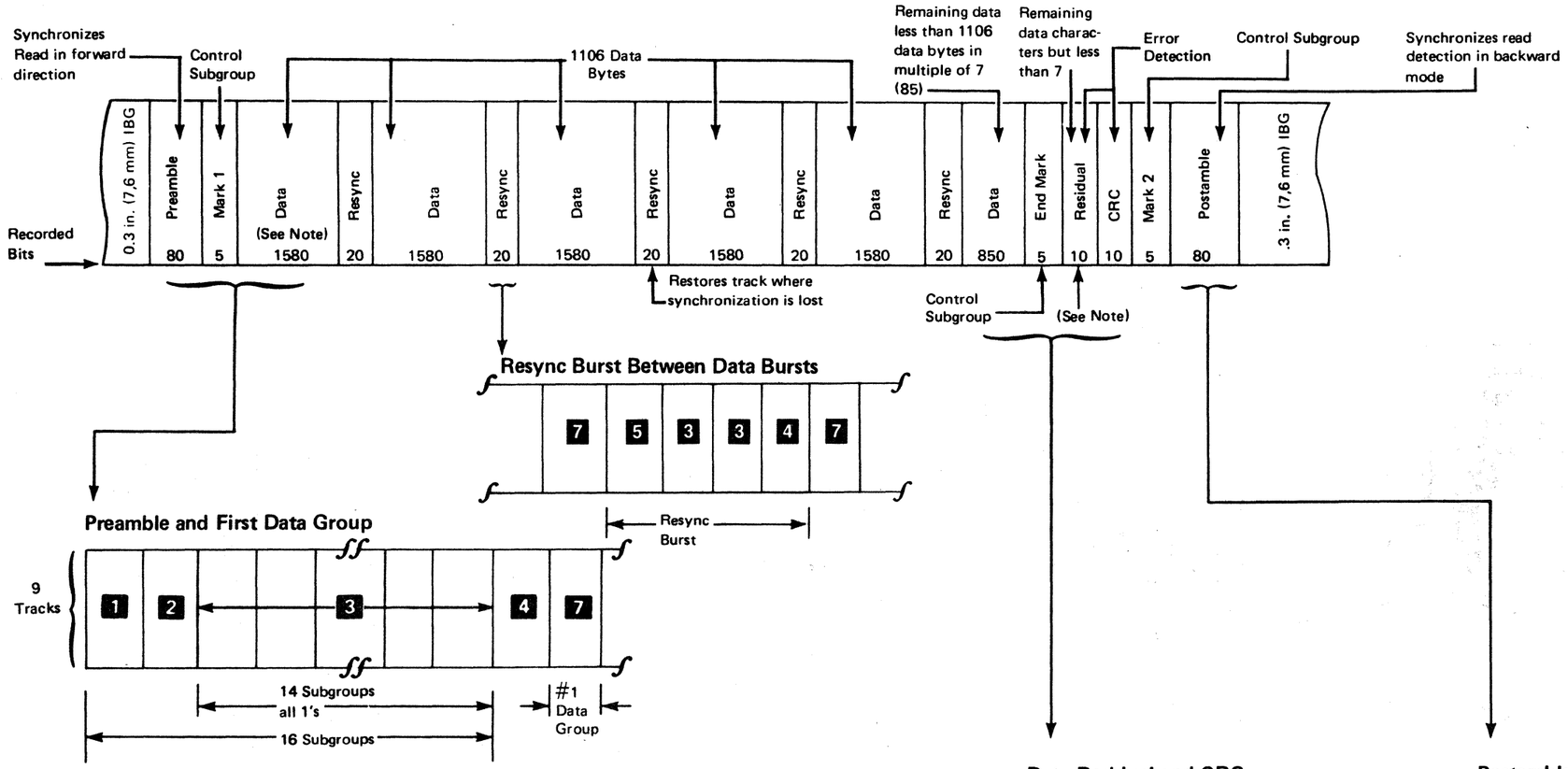
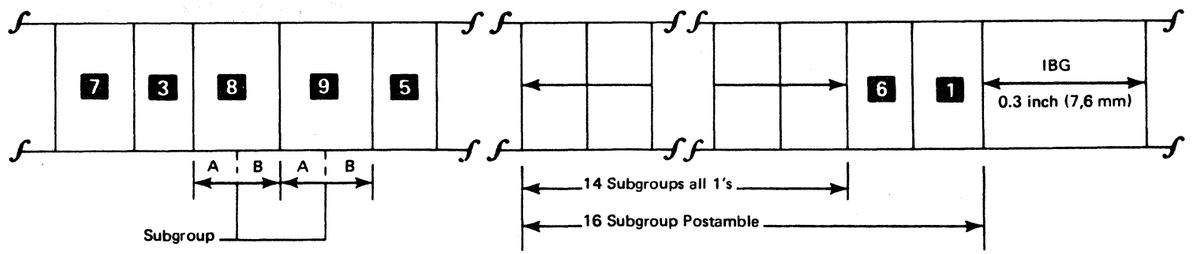
GROUP CODED RECORDING 6250 BPI



Note: From first data bytes through residual bytes (9042 fci) equals 6250 bpi of customer data.

Legend

For all bits (tracks 1 through 9)			
Key	Name	Pattern	Comments
1	Term	10101	
2	Second 1	01111	
3	Sync	11111	
4	Mark 1	00111	
5	Mark 2	11100	
6	Second 2	11110	
7	Data	DDDD DDDE or GGGG GGGG	
8	Residual	XXXX XXXE or HHHH HHNE	
9	CRC	BCCC CCXE	
		(See 55-010 Legend 2 for data symbols.)	



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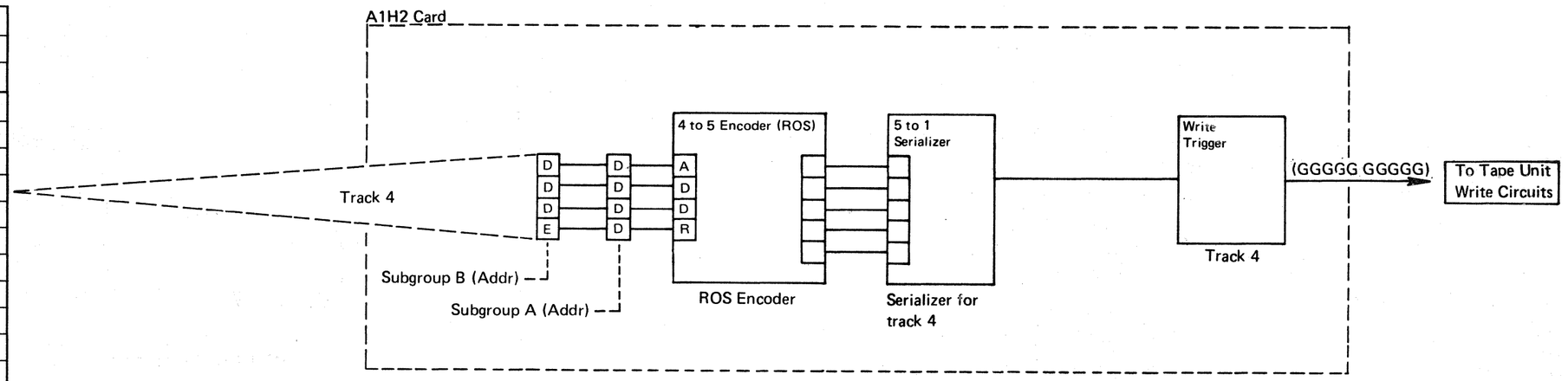
GROUP CODED RECORDING 6250 BPI (Cont'd)

6250 bpi does not relate to actual writing density on tape, but to effective data density. Actual density (9042 bpi) is greater due to the formatting and encoding. This formatting and encoding is transparent to the user. The formatting and encoding method allows reliable error correction for any two tracks simultaneously in error. Also, tracks are not immediately dequeued or dead tracks assigned when an error occurs as they were in the past. It is conceivable that a block could have errors in all nine tracks and appear to the user to be read error free as long as only two tracks have errors at any given instant.

Figure 3a. Encoded Data Group

Physical Tracks	DATA GROUP		STORAGE GROUP	
	Subgroup		Subgroup	
	A	B	A	B
	DDDD	DDDD	GGGGG	GGGGG
2	DDDD	DDDD	GGGGG	GGGGG
3	DDDD	DDDD	GGGGG	GGGGG
4	DDDD	DDDD	GGGGG	GGGGG
5	DDDD	DDDD	GGGGG	GGGGG
6	DDDD	DDDD	GGGGG	GGGGG
7	DDDD	DDDD	GGGGG	GGGGG
8	DDDD	DDDD	GGGGG	GGGGG
9	DDDD	DDDD	GGGGG	GGGGG
	1234	5678	12345	678910
Group Positions				

Figure 3b. How 4 Bit (Address) Becomes 5 Data Bits



Note: This illustration is only one of nine such circuits. (See 50-001 for further details.)

Legend 2. Data Symbols

Symbol	Data Represented
B	CRC or Pad Characters
C	Cyclic Redundancy Check Characters
D	Channel Data Characters
E	ECC Characters
G	Encoded Group Recorded Bits
L	Last Character
N	Auxiliary CRC
X	Residual Character

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COMMON START I/O (SIO) ROUTINE

This section introduces the microprogram controls used to read and write a record from load point. Addresses noted within the charts are key checkpoint addresses which perform a major function.

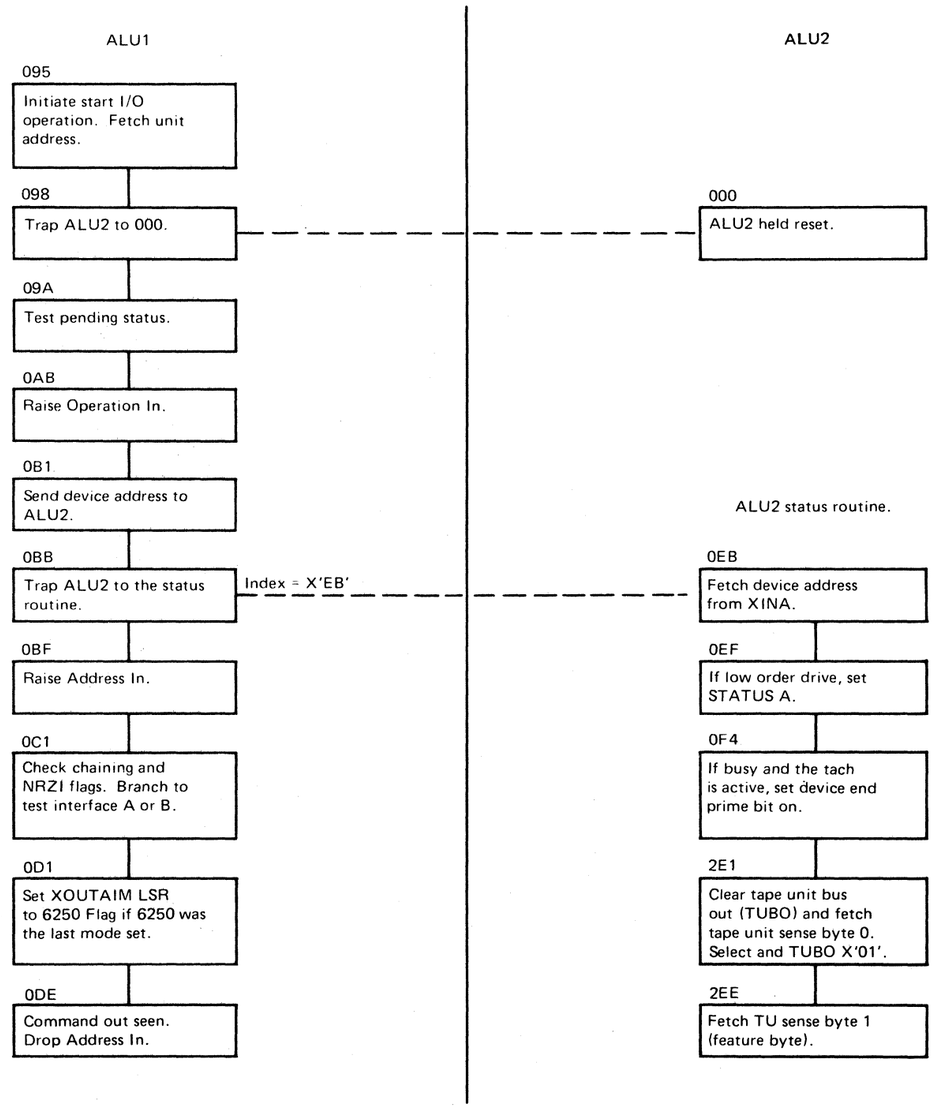
These charts provide major syncronization points within a routine, and lay out a path to check the path through the microcode. The common Start I/O routine is followed by the write operation, then the read operation from load point. The paths shown are for single, unchained operations with no exceptional conditions.

Using the compare ROS stop sync on ROS address of the CE panel (see sequence 10 on page 12-011), synchronization can be developed at various points within the operation being performed.

Remember that many routines are commonly used many times and will provide unstable synchronization points.

Some knowledge of basic microprogram concepts is assumed. XOUTA and XOUTB registers as well as the status registers A, B, C, and D provide response back and forth between the ALUs. ALU1 basically controls the processing unit channel, while ALU2 controls the device interface. Both ALUs control various portions of the data flow.

ALU2 is a slave to ALU1, and is controlled by a transfer command and XOUTB branch index byte being passed from ALU1 to ALU2. Response from ALU2 is by way of ALU2 status registers.



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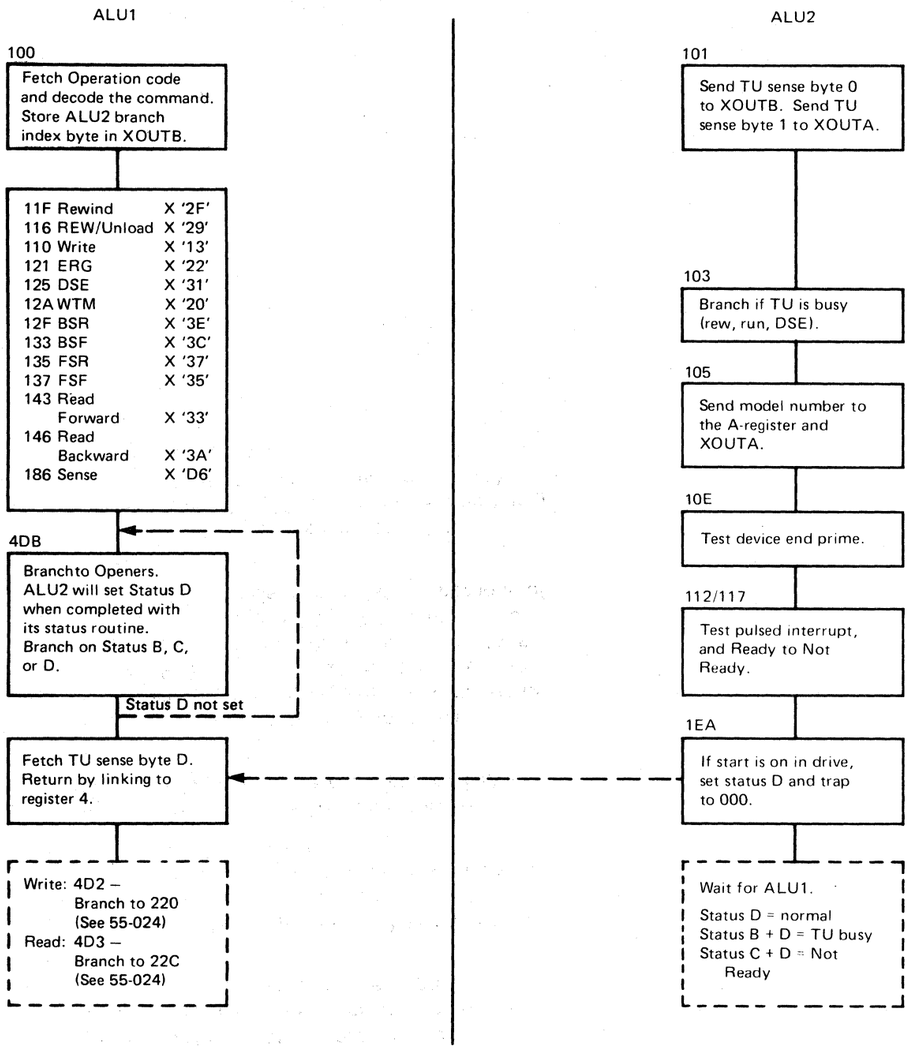
COMMON START I/O (SIO) ROUTINE (Cont'd)



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BRANCH TO WRITE FROM LOAD POINT

Write from load point is performed by controlling drive motion and controls with ALU2. ALU2 also sets the data flow control to write the single 1 or P track identification (ID) at load point.

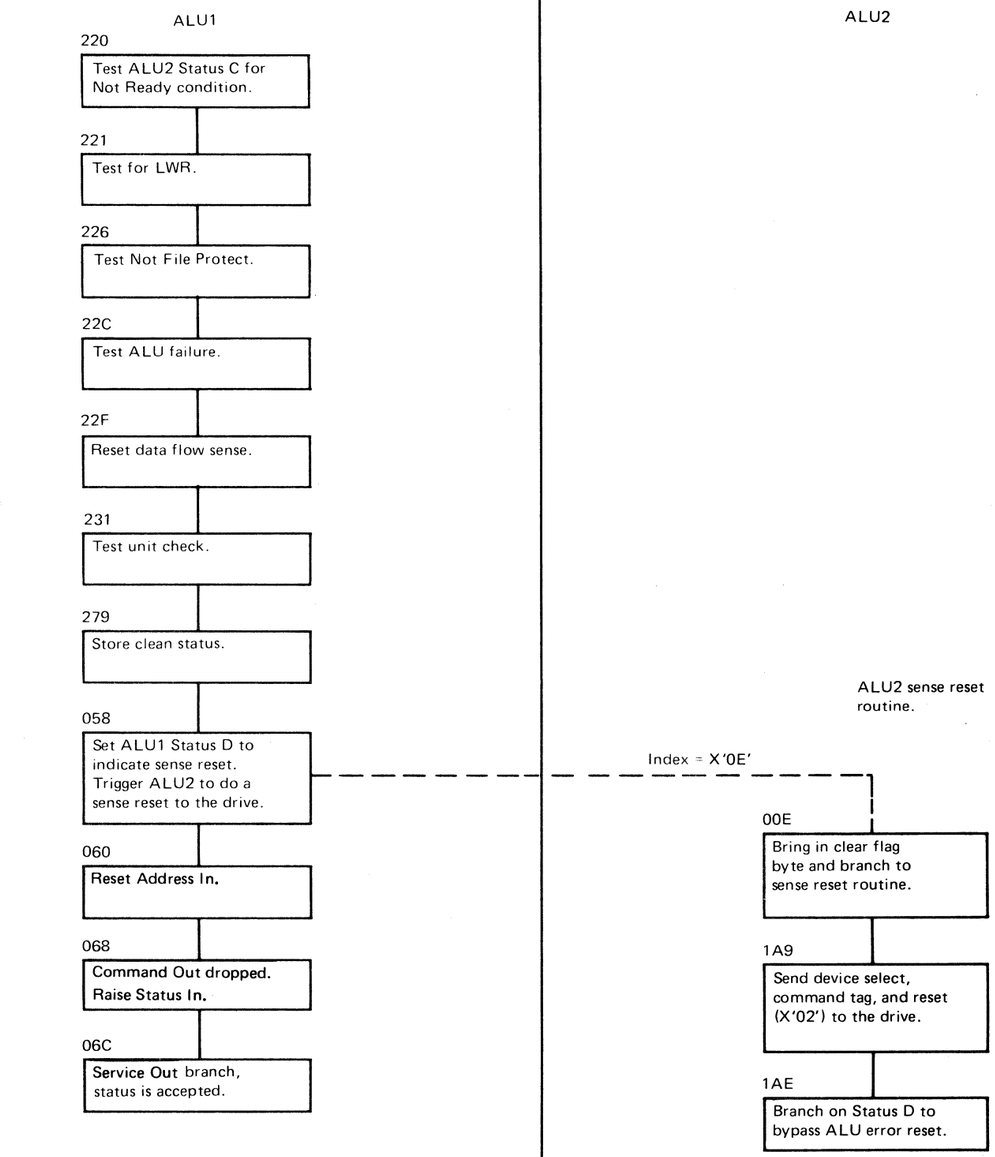
ALU1 initiates the first data Service-In cycle, then relinquishes data transfer to the hardware. ALU1 also controls the write triggers for all control characters within the preamble, postamble, and resync burst.

Once the data portion of the write command is entered, ALU2 monitors velocity during the tach period transitions to test for velocity change during write.

The write operation is divided into the following steps:

1. Trigger ALU2 to issue a sense reset to the drive. ALU1 will monitor ALU2 Status D, which indicates that ALU2 is finished with sense reset.
2. Fetch TU sense bytes 0 and 1 and test for drive status.
3. Raise Service In for one byte of data before turning control of the channel over to the data flow section.
4. ALU1 again allows ALU2 to perform the write operation.
5. Set Erase in the drive (not Write Status yet) and erase backward, then forward. (Backward 150 tachs, forward 140 tachs.)
6. Test for Tach Start fail or Velocity Error, then write 1-track ID burst.
7. Write self-adjusting gain control (SAGC) burst with the inverse Tape Mark (no zone 1) attached to the end.
8. Set SAGC circuits in the drive to perform read back check.
9. Write record preamble consisting of the following characters: 10101, 01111, seventy 1s, 00111.
10. The hardware data flow section now takes over the writing of data while ALU2 monitors the capstan tach velocity in the drive.
11. Every 1106 channel bytes (158 storage groups on tape), ALU1 intersperses a resync burst consisting of: 00111, 11111, 11111, 11100.
12. When data is complete, the hardware writes an all ones character.
13. ALU1 checks for an all ones character indicating the end of data. This allows for writing of the residual and CRC frames.
14. ALU1 then writes the postamble consisting of the following characters: 11100, seventy 1s, 11110, 10101.
15. ALU2 waits for IBG, then tests for errors. ALU2 finishes by setting Status D and trapping to 000.

WRITE FROM LOAD POINT



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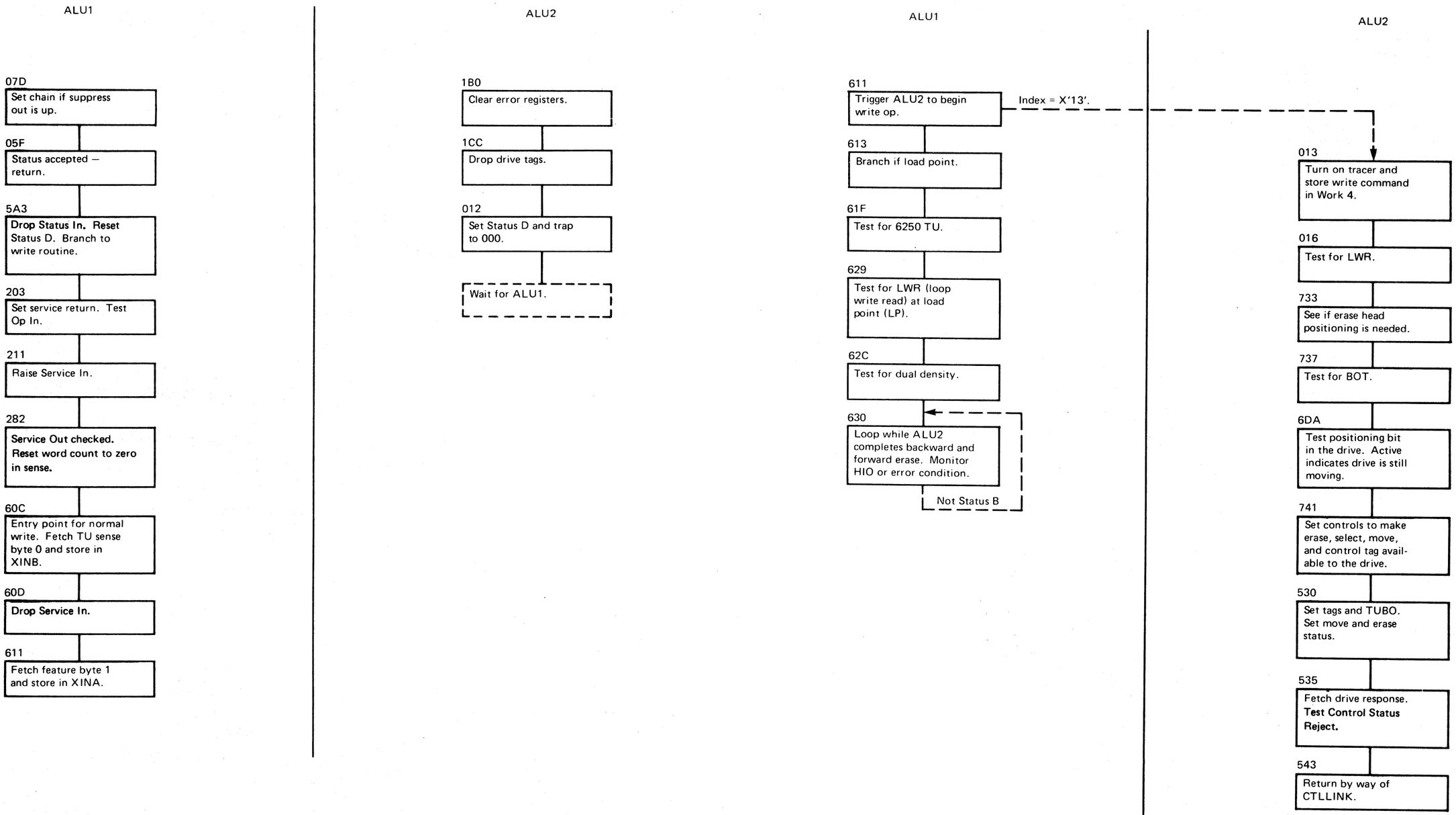
BRANCH TO WRITE FROM LOAD POINT (Cont'd)

WRITE FROM LOAD POINT



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BRANCH TO WRITE FROM LOAD POINT (Cont'd)

WRITE FROM LOAD POINT

ALU1

ALU1 still looping until ALU2 sets Status B.

ALU2

74E
Load backward tach count = 150.

781
Wait for read time, then start count and raise Move tag to the drive.

78C
Count down check – set no tach error if 256 counts were received without seeing tach pulse.

792
COUNTONE – tach seen, increase count by one.

793
Test flags and opposite direction bit.

Count not = 0

79B
Count ran out. Drop command tag.

751
Load forward tach count = 145.

753
Store write command (X'08') in Work 4. (Sets forward in TU.)

768
Raise Command tag and place Work 4 on TUBO.

770
Fetch drive response. **Test Command Status Reject.**

ALU1

ALU1 still looping until ALU2 sets Status B.

ALU2

778
Drop command tag and TUBO.

785
Wait for **read time.** Begin count down.

79B
Count down complete. Return to routine.

756
Drop move and store write command in Work 4.

138
Turnaround and test BOT.

13E
Branch if 6250 feature is present.

151
Fetch mode set from XINA. Test if 6250 feature is present.

156
Set 6250 in XOUTAIM.

17A
Test backward.

161
Write and command tag to TUBO.

16C
Fetch drive response. **Test Command Status Reject.**

182
Test LWR and turnaround.

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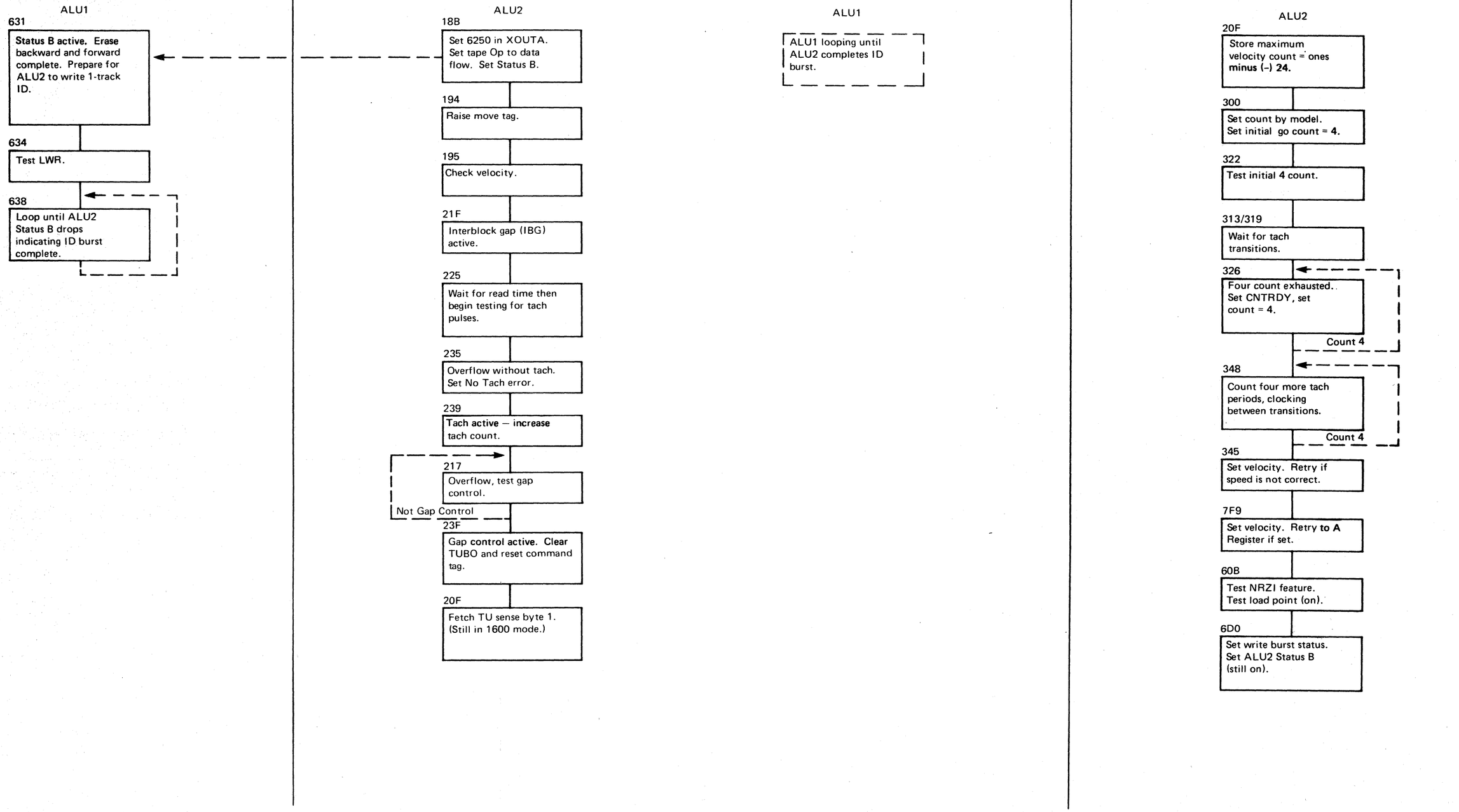
BRANCH TO WRITE FROM LOAD POINT (Cont'd)

WRITE FROM LOAD POINT



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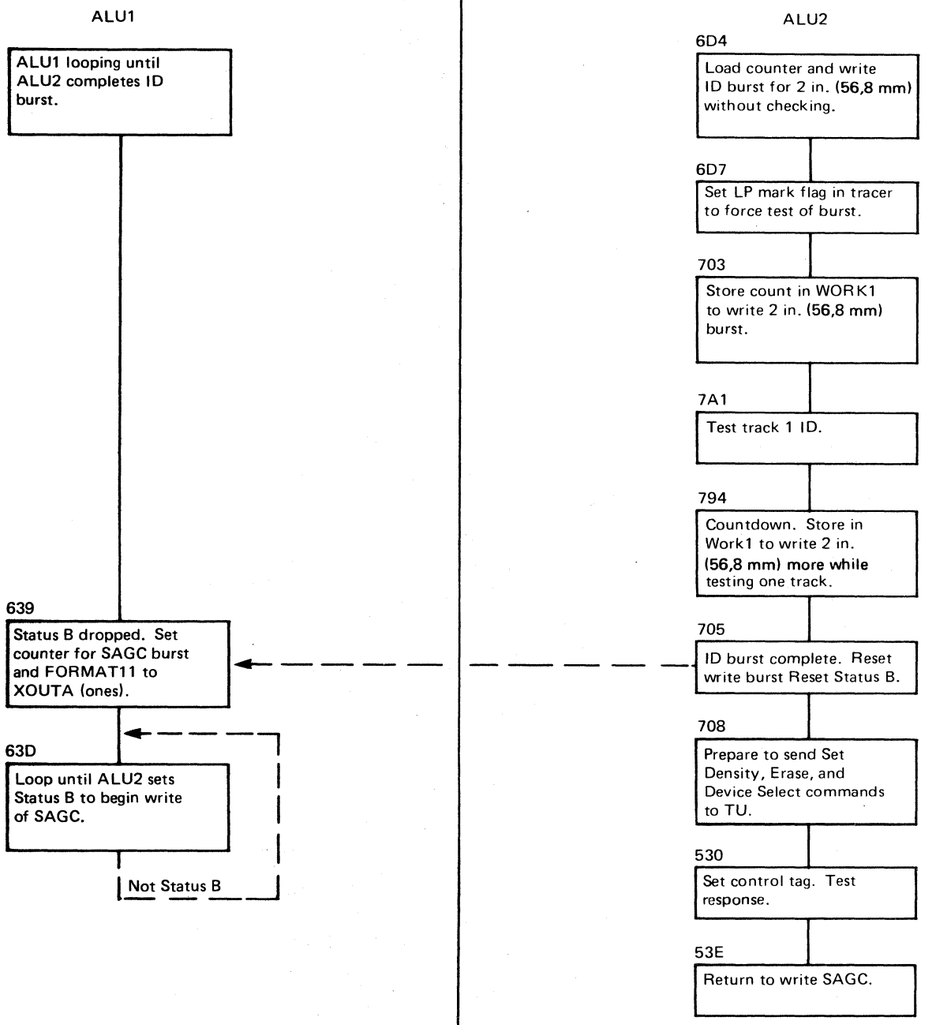
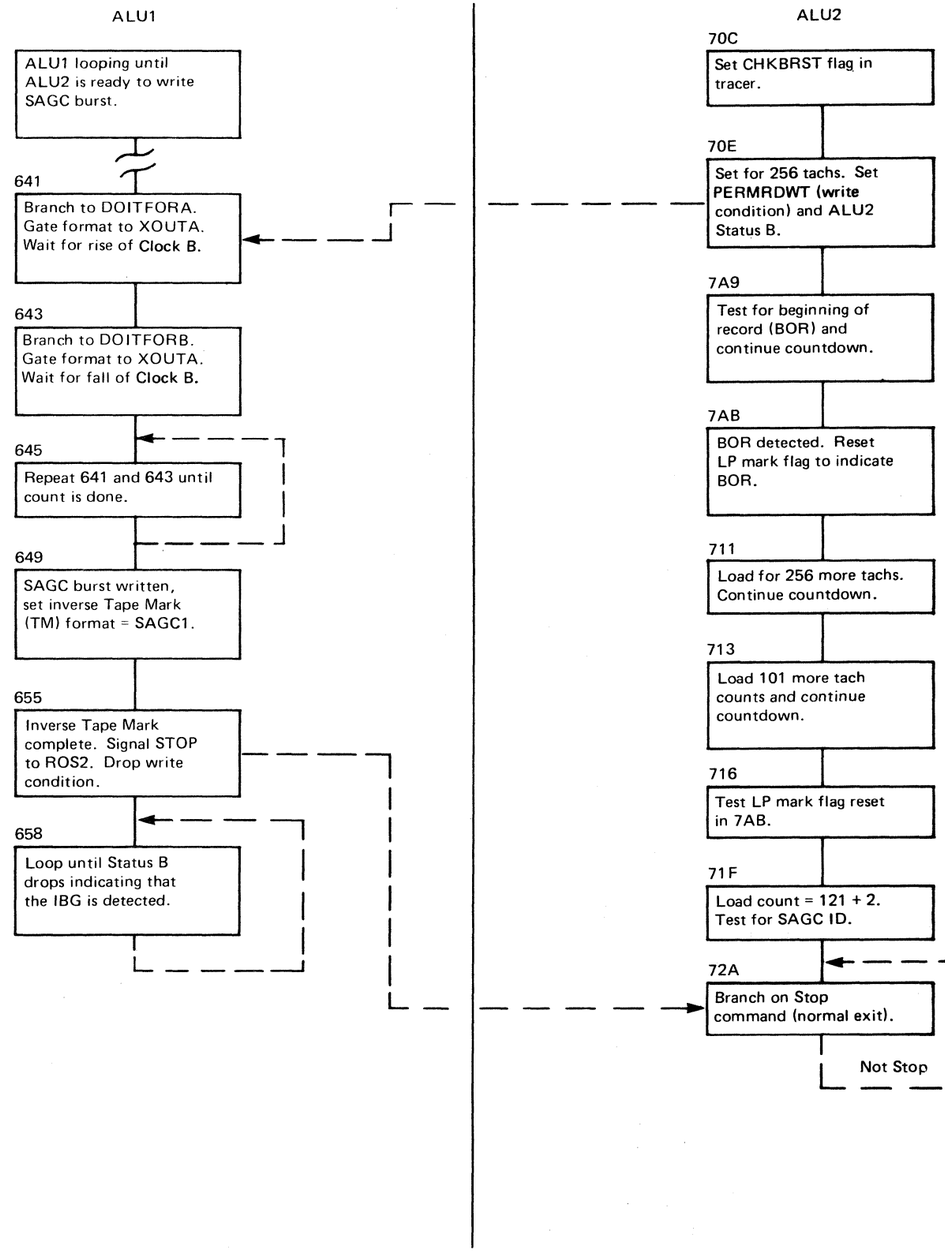
BRANCH TO WRITE FROM LOAD POINT (Cont'd)

WRITE FROM LOAD POINT





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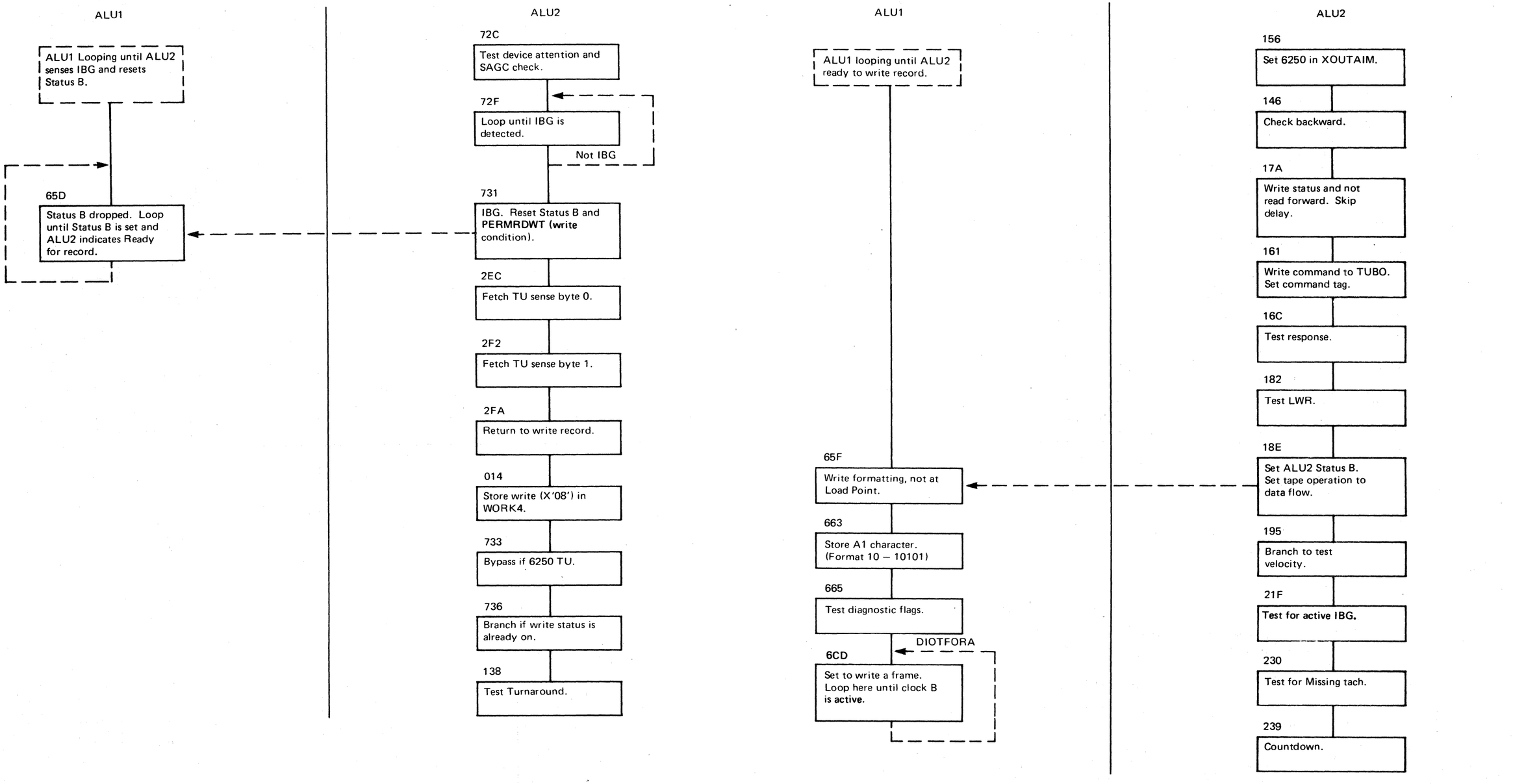
BRANCH TO WRITE FROM LOAD POINT (Cont'd)

WRITE FROM LOAD POINT



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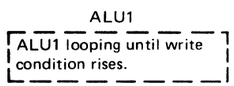
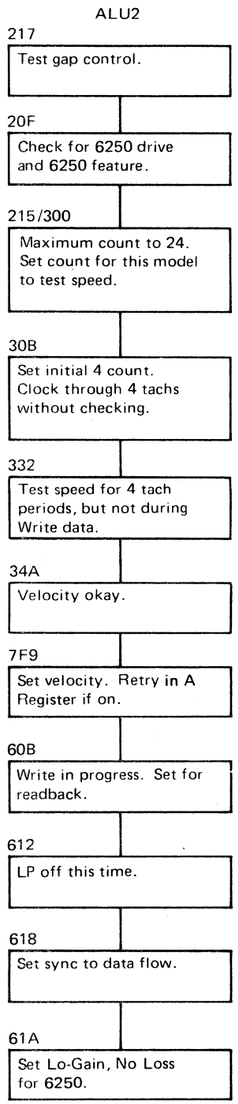
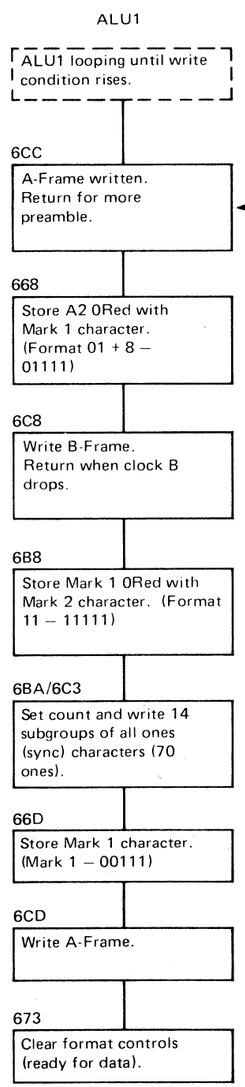
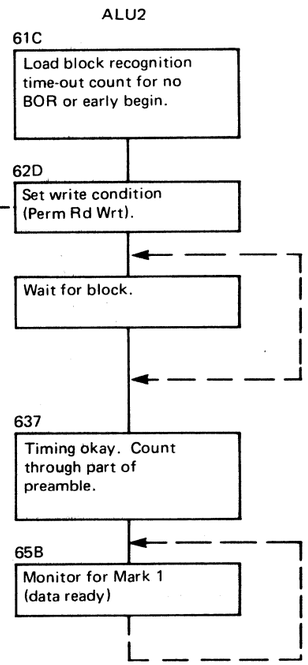
BRANCH TO WRITE FROM LOAD POINT (Cont'd)

WRITE FROM LOAD POINT









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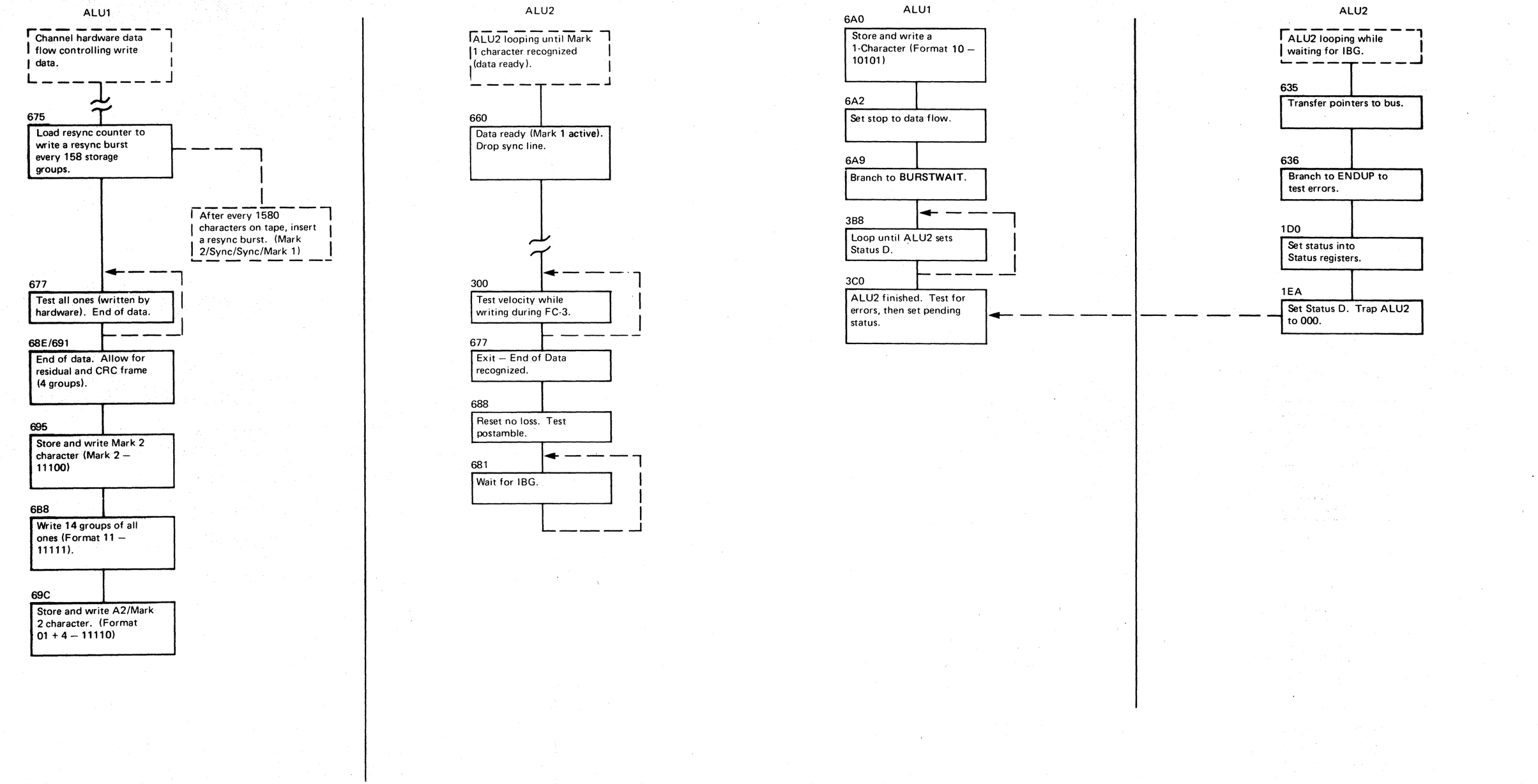
BRANCH TO WRITE FROM LOAD POINT (Cont'd)

WRITE FROM LOAD POINT



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BRANCH TO READ FROM LOAD POINT

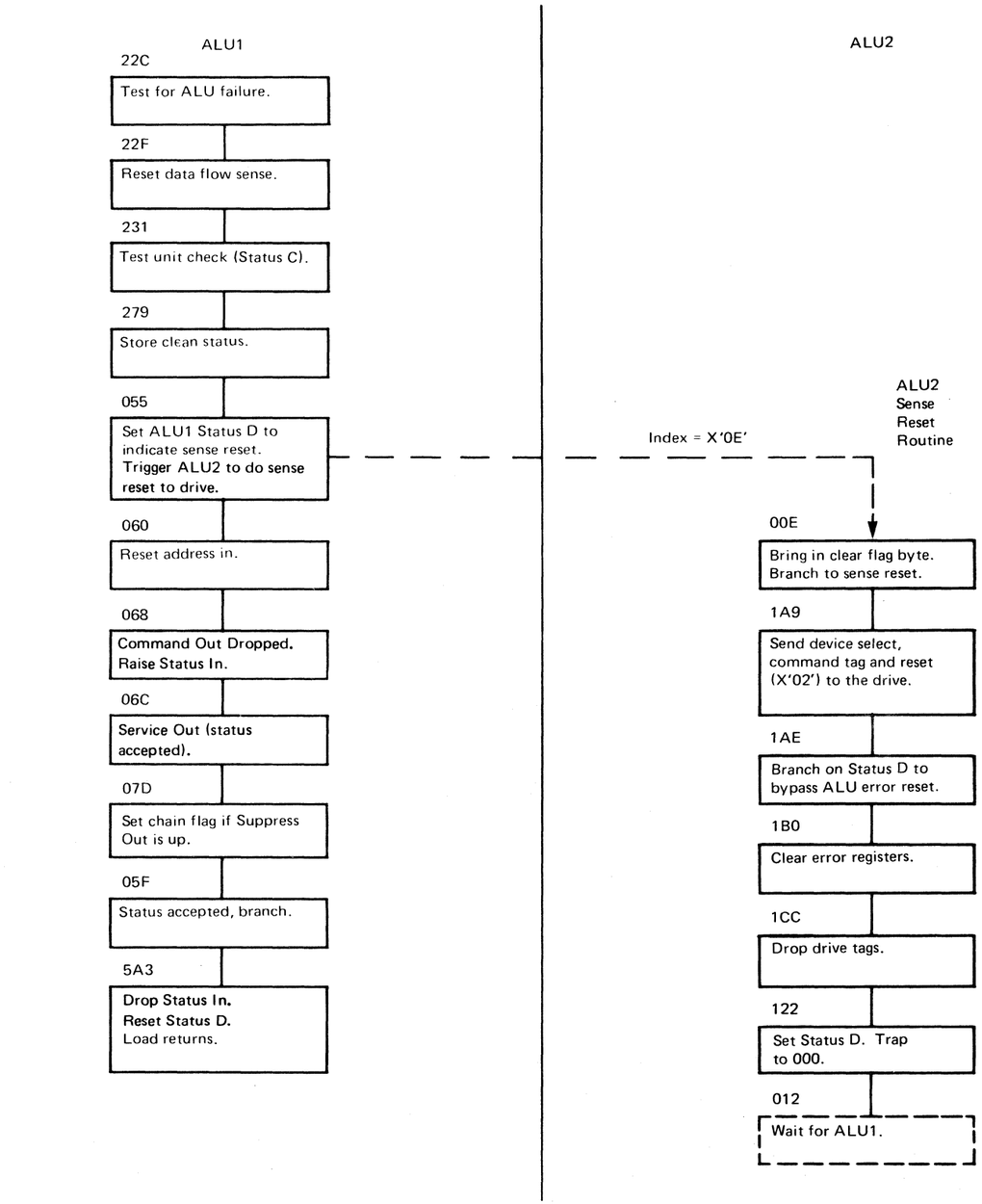
Read from load point is basically performed by ALU2 and the hardware data flow controls.

Once ALU1 has triggered ALU2 to perform sense reset to the drive, and again to initiate the read from load point, ALU1 is basically finished. ALU1 tests to be sure that the first service cycle takes place, then goes into a loop until ALU2 finishes and sets Status D.

The read forward operation from load point steps follow:

1. ALU1 triggers ALU2 to issue a sense reset to the drive.
2. ALU1 triggers ALU2 to begin the read operation. If Status D from ALU2 is sensed before the first service cycle, an error is signalled.
3. ALU2 tests the status of the drive and checks for correct velocity.
4. Move 3 in. (76,2mm) of tape, then test for a 1-track envelope indicating a 6250 bpi tape.
5. Count through part of SAGC, then initiate read SAGC circuits in the drive.
6. Clock through 550 tachs, then check the Inverse Tape Mark.
7. When IBG is reached, fetch two bytes of drive sense and test status to this point.
8. Set read condition after gap control comes up again, and wait for the Mark 1 character preceding the data.
9. The hardware data flow now takes over until the end of data is sensed.
10. Test for errors. ALU2 sets Status D when finished, altering ALU1.
11. ALU1 compares the modulo count then branches to the status handler.

READ FROM LOAD POINT



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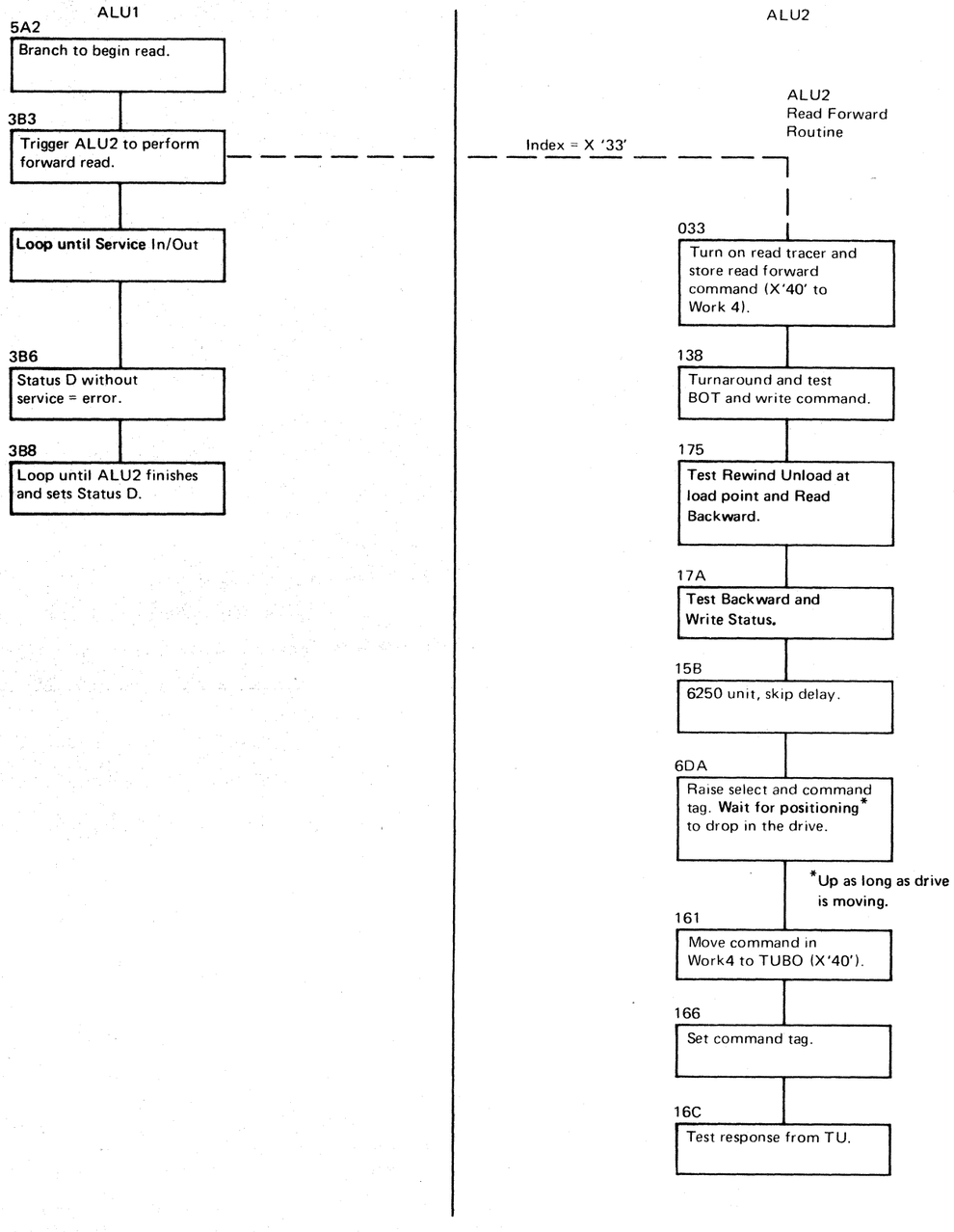
BRANCH TO READ FROM LOAD POINT (Cont'd)

READ FROM LOAD POINT



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BRANCH TO READ FROM LOAD POINT (Cont'd)

READ FROM LOAD POINT

ALU1

ALU1 still looping until ALU2 finishes.

ALU2

26B
Test 1-track envelope.

280
Test P 1-track error not sensed. Track burst.

278
Increase NRZI count if neither.

270
If count times out, set for **Not Capable.**

Normal Path

270
1-Track and overflow. Turn off PE control and set hi-density control.

275
Count through part of SAGC burst. Tape is 6250.

2BA
Entering SAGC burst. Load set density controls.

530
Set SAGC circuits in TU (initiate SAGC).

28E
Count 550 tachs through SAGC burst.

293
Nearing end of SAGC. Test BOR and device attention (SAGC check).

ALU1

ALU1 still looping until ALU2 finishes.

ALU2

29C
Check for inverse Tape Mark (SAGC ID).

29D
Test device attention.

29E
Wait for IBG.

2E0
Fetch 2 bytes of sense from the drive.

Link 1 = FB

038
Store Read Forward. Ready for record.

049
Branch to turnaround.

Link 1 = 56

17B
Drive in forward status, skip delay.

161
Read to TUBO (test response).

18D
Set Status B and tape operation.

194
Raise move tag.

219
Test velocity.

Link 2 = 17

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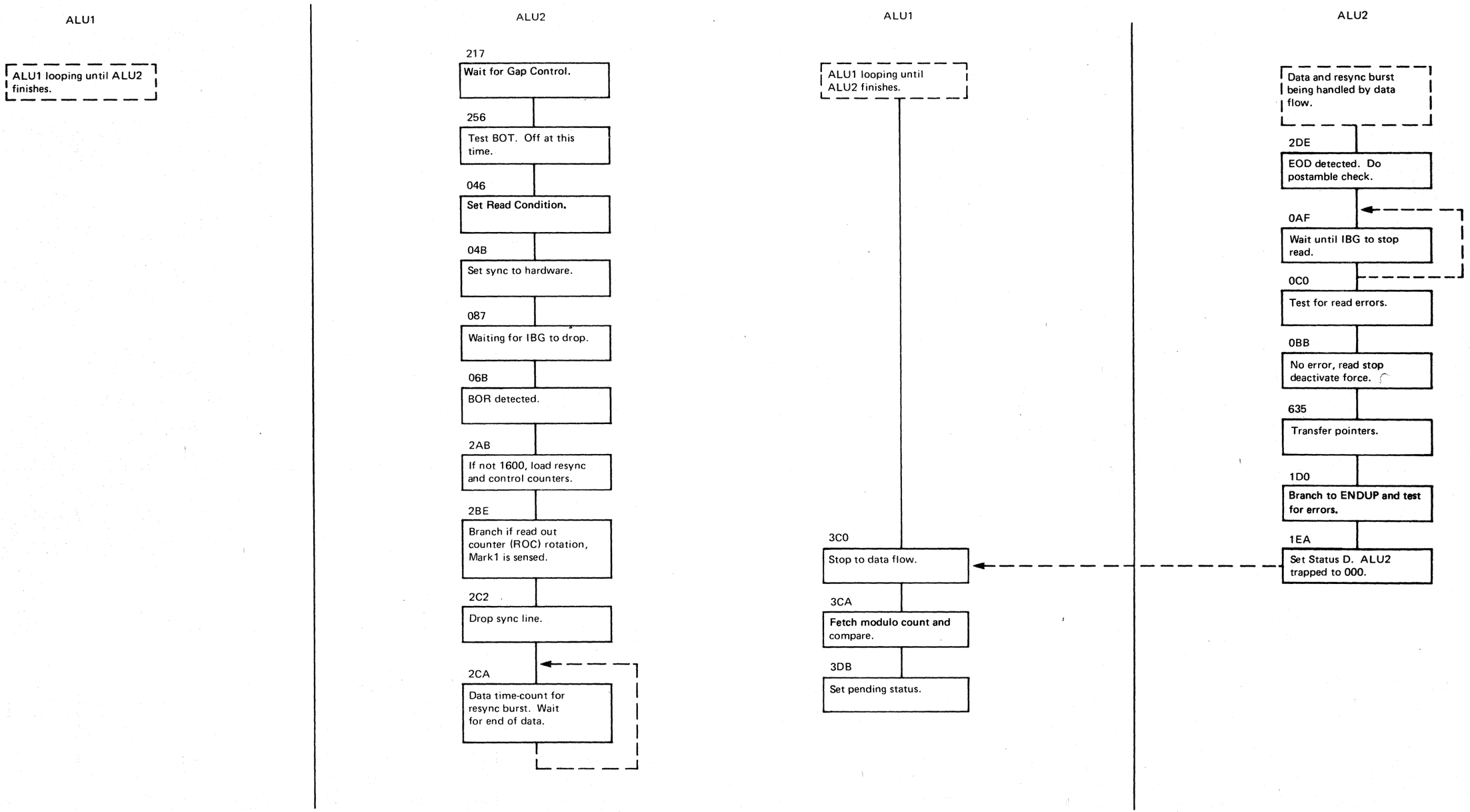
BRANCH TO READ FROM LOAD POINT (Cont'd)

READ FROM LOAD POINT



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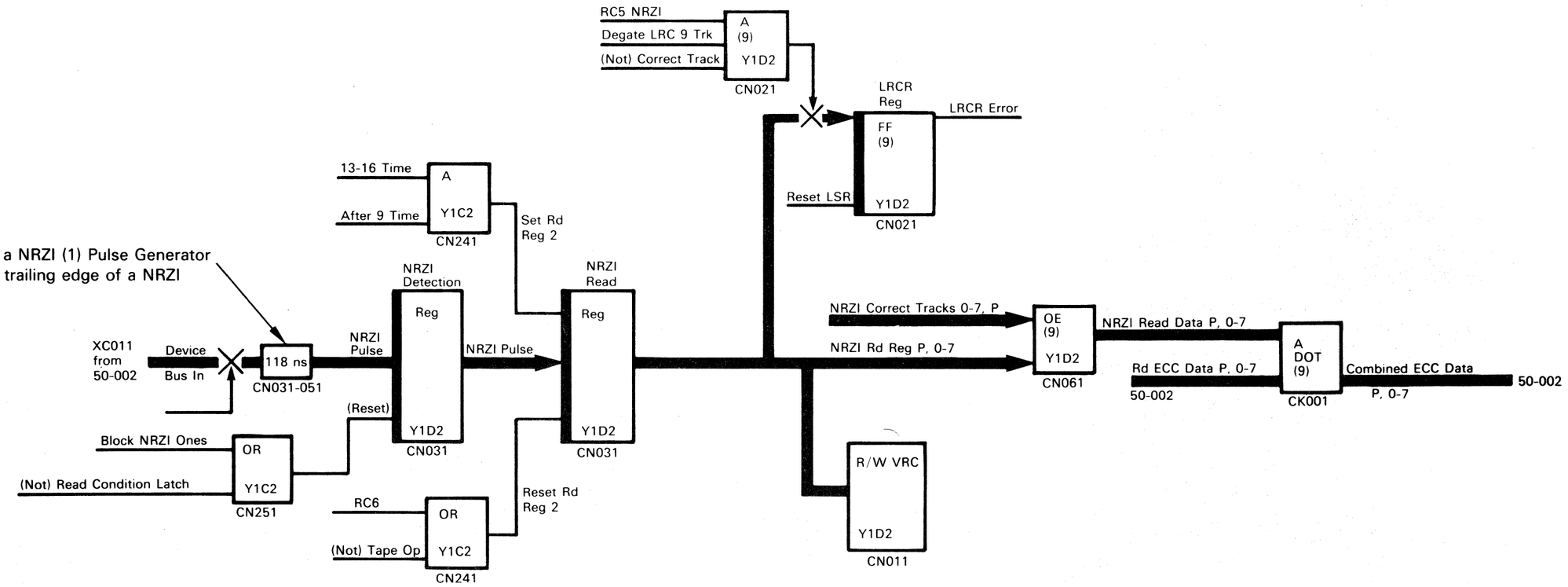
NRZI READ DATA FLOW



Note: The 118 ns delay is a NRZI (1) Pulse Generator which uses the de-skewed trailing edge of a NRZI pulse from the tape unit.

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WRITE TRANSLATOR (CARD A1E2)

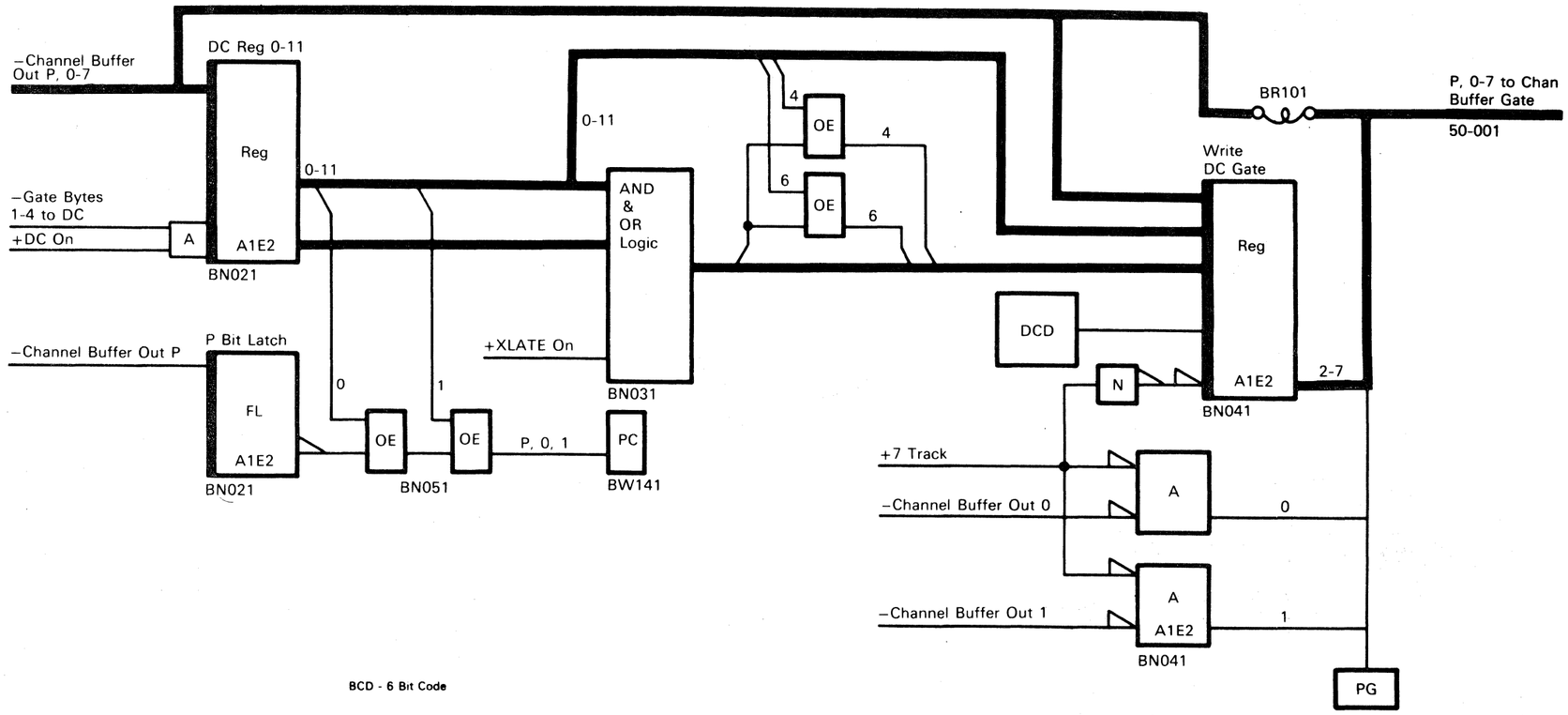
TRANSLATOR

Some tape subsystems use a six-bit BCD code. Each character of the six-bit code can be translated to an equivalent eight-bit character for processing by 9-track tape subsystems. A translator in the tape control translates eight-bit code to six-bit code while writing, and translates six-bit code to eight-bit code while reading. The translator operates only if Microprocessor 1 XOUTA bits 2 and 4 are on at the rise of TAPE OP and Microprocessor 2 Stat bits 0 and 3 are on.

On 7-track write operations with the translator off, the tape control discards the two high-order bit positions (BUS OUT bits 0 and 1) of each byte from channel. Only the six low order data bits (plus a parity bit) are transferred to the tape unit.

On 7-track read operations with the translator off, the tape control inserts zeros in the two high order bit positions (BUS IN bits 0 and 1) of each byte when transferring it to channel.

ECBDIC AND BCD CODES



EBCDIC - 8 Bit Code

Bits 4567	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
	00				01				10				11			← Bits 0, 1
0000	BL	&	−	0	BL	&	−	0	>	<	‡	0	>	<	‡	0
0001	A	J	/	1	A	J	/	1	A	J	/	1	A	J	/	1
0010	B	K	S	2	B	K	S	2	B	K	S	2	B	K	S	2
0011	C	L	T	3	C	L	T	3	C	L	T	3	C	L	T	3
0100	D	M	U	4	D	M	U	4	D	M	U	4	D	M	U	4
0101	E	N	V	5	E	N	V	5	E	N	V	5	E	N	V	5
0110	F	O	W	6	F	O	W	6	F	O	W	6	F	O	W	6
0111	G	P	X	7	G	P	X	7	G	P	X	7	G	P	X	7
1000	H	Q	Y	8	H	Q	Y	8	H	Q	Y	8	H	Q	Y	8
1001	I	R	Z	9	I	R	Z	9	I	R	Z	9	I	R	Z	9 ← Note 2
1010	>	<	‡	ŏ	>	<	‡	ŏ	BL	&	−	ŏ	BL	&	−	ŏ
1011	.	$	,	#	.	$	,	#	.	$	,	#	.	$	,	#
1100	◄	•	%	@	◄	•	%	@	◄	•	%	@	◄	•	%	@
1101	(	)	WS	v	(	)	WS	v	(	)	WS	v	(	)	WS	v
1110	+	;	▲	▬	+	;	▲	▬	+	;	▲	▬	+	;	▲	▬
1111	GM	MC	SM	TM	GM	MC	SM	TM	GM	MC	SM	TM	GM	MC	SM	TM
	0 1 2 3				4 5 6 7				8 9 10 11				12 13 14 15			

Note 2

BCD - 6 Bit Code

4,5,6,7	—	−A	B−	BA ← BCD
8421	00	01	10	11 ← Tracks
0000	BL	ŏ	−	&
0001	1	/	J	A
0010	2	S	K	B
0011	3	T	L	C
0100	4	U	M	D
0101	5	V	N	E
0110	6	W	O	F
0111	7	X	P	G
1000	8	Y	Q	H
1001	9	Z	R	I
1010	0	‡	<	>
1011	#	,	$	.
1100	@	%	•	◄
1101	v	WS	)	(
1110	▬	▲	;	+
1111	TM	MC	SM	GM

Notes:

[1] The graphics in these charts may not be identical to those printed by the printer or printer-keyboard. The graphics are intended as references for translating bit codes on a read or write operation.

[2] The write translator accepts the complete EBCDIC code and translates the bits to the BCD code. However, the read translator translates the BCD code only to the bits outlined.

[3] When operating in the even-parity mode, the EBCDIC blank (bl) is translated to a BCD substitute blank (bl), and the BCD substitute blank is translated to an EBCDIC blank (01000000). The odd parity blank's bit code is 000000.

3803-2/3420

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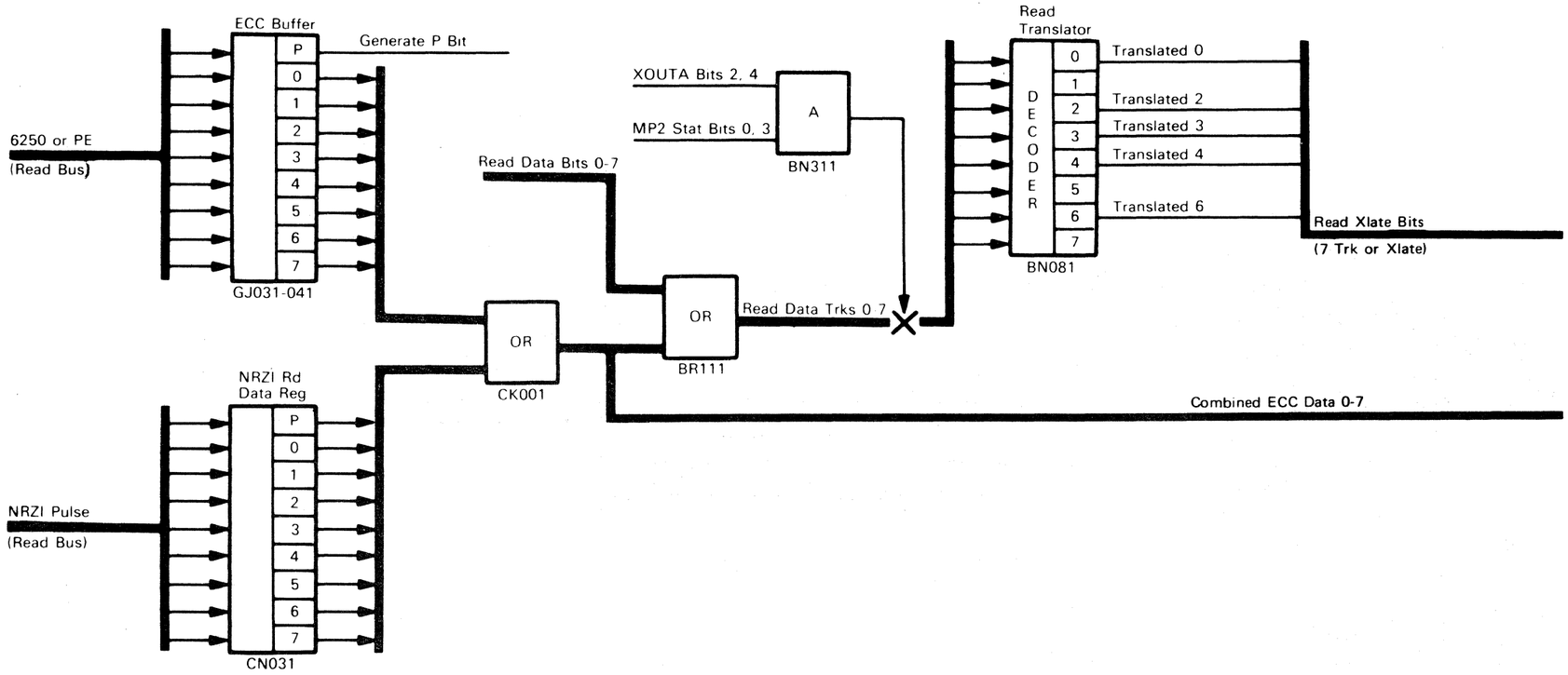
READ TRANSLATOR (CARD A1E1)

Read Translator Data Flow

ANDs and ORs translate bits 0-7 to determine EBCDIC code.



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WRITE DATA CONVERTER (CARD A1E2)

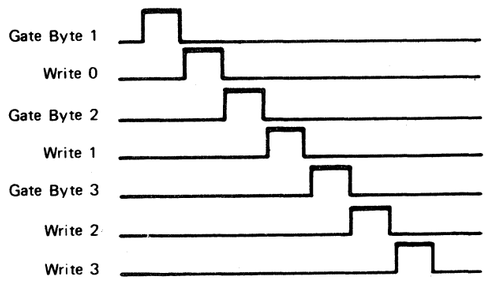
The data converter is used for 7-track write and read forward operations only.

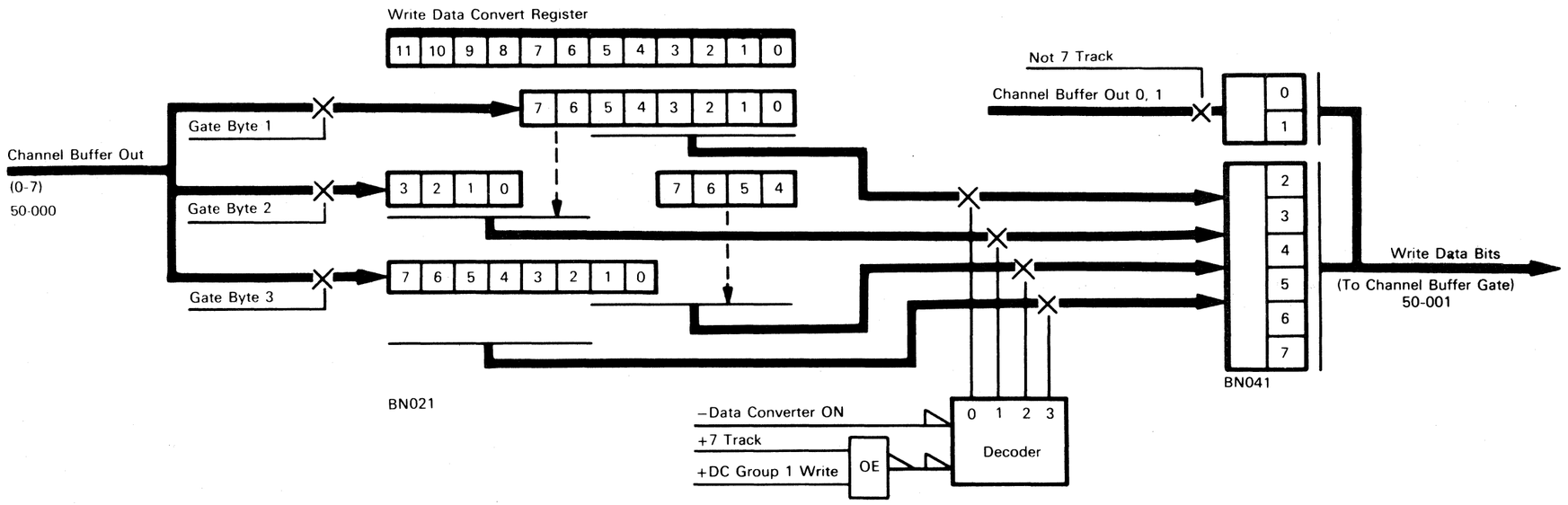
The data converter is disabled during read backward operations, but is left on for the next write or read forward operation.

The data converter is turned on and off by a mode set command. When Microprocessor 1 XOUTA BIT 2 is on at the rise of TAPE OP (MP2, Status 0), the data converter is off. When Microprocessor 1 XOUTA BIT 2 is off at the rise of TAPE OP (MP2, Status 0), the data converter is on.

During a write operation, three 8-bit EBCDIC bytes from channel are converted to four 6-bit BCD characters for writing on tape. If the byte count is not a multiple of three, any remaining bits of the last 6-bit character are set to zero.

DATA CONVERT WRITE TIMING





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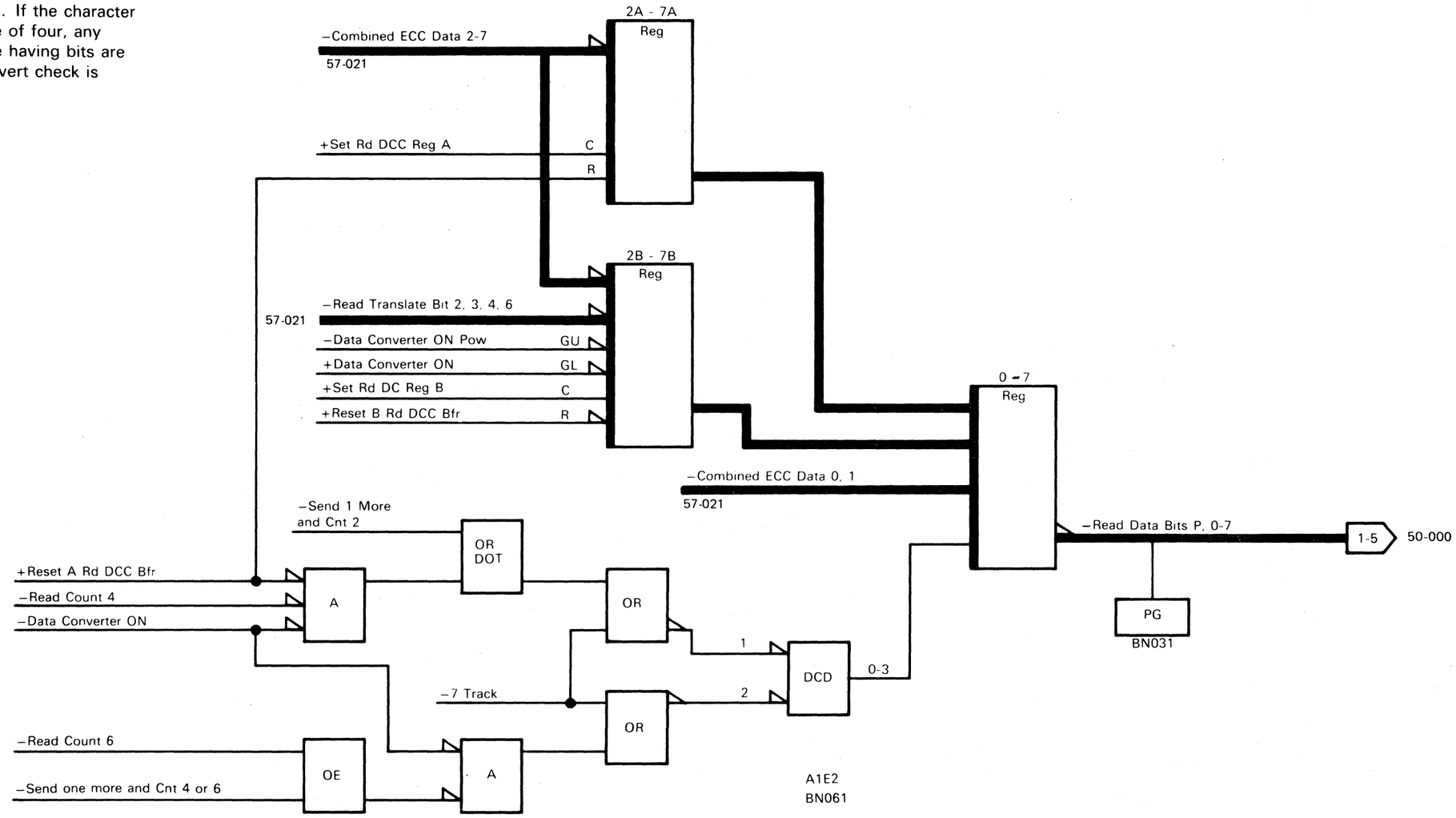
READ DATA CONVERTER

During a read operation, four 6-bit characters (plus parity) from tape are converted to three 8-bit bytes (plus parity) for transfer to channel. If the character count of the block is not a multiple of four, any remaining positions in the last byte having bits are padded with zeros, and a data convert check is indicated.



XG3400 Seq 1 of 2	2736004 Part Number	See EC History	845958 1 Sep 79					

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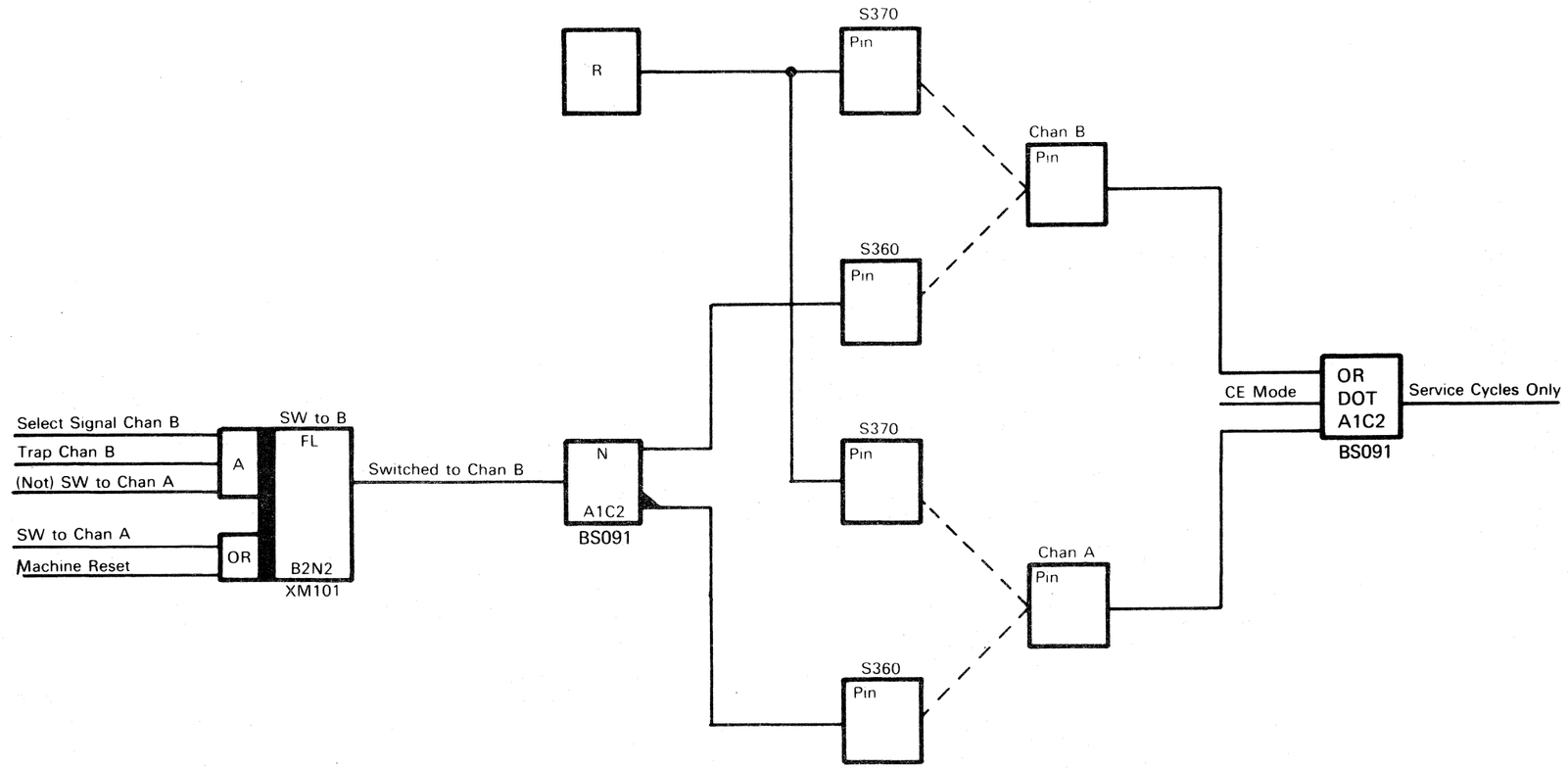
OBJECTIVES

1. The switching circuit enables a 3803-2 to be attached to either a System/360 or a System/370.
2. Selection is accomplished by plugging cards to reflect system type on which the tape subsystem is installed. See installation, Page 90-130 or AA010, Sheet 2.
3. When plugged for S/360, a Service In/Service Out sequence is used.
4. When plugged for S/370, a Service In/Service Out/Data In/Data Out sequence is used.



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A 3803-2 tape control with a two-channel switch (TCS) [1] operates with two channel interfaces. All 3803-2 operations can be performed on either channel interface. Channels attached to the TCS interfaces can be attached to the same system or to separate systems, allowing tape units on the tape control with the TCS feature to be shared by two channels on a single system, or by two systems. In addition to all normal operations, a tape control with this feature can execute Reserve and Release commands for program control of interface switching. The large block in the center of the diagram and the unshaded blocks represent control circuits for a standard tape control. The shaded blocks represent additional logical functions installed on the tape control for the Two-Channel switch.

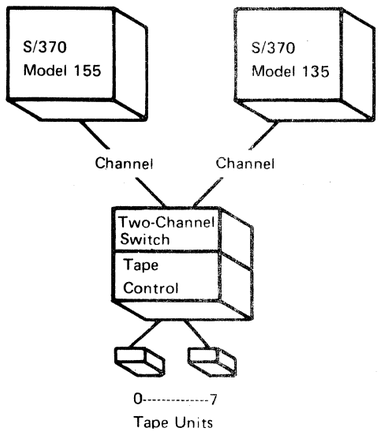
Channel interface lines going into or out of the tape control pass through interface switch circuits. The circuits consist of gated drivers that connect the tape control to either channel interface (A or B).

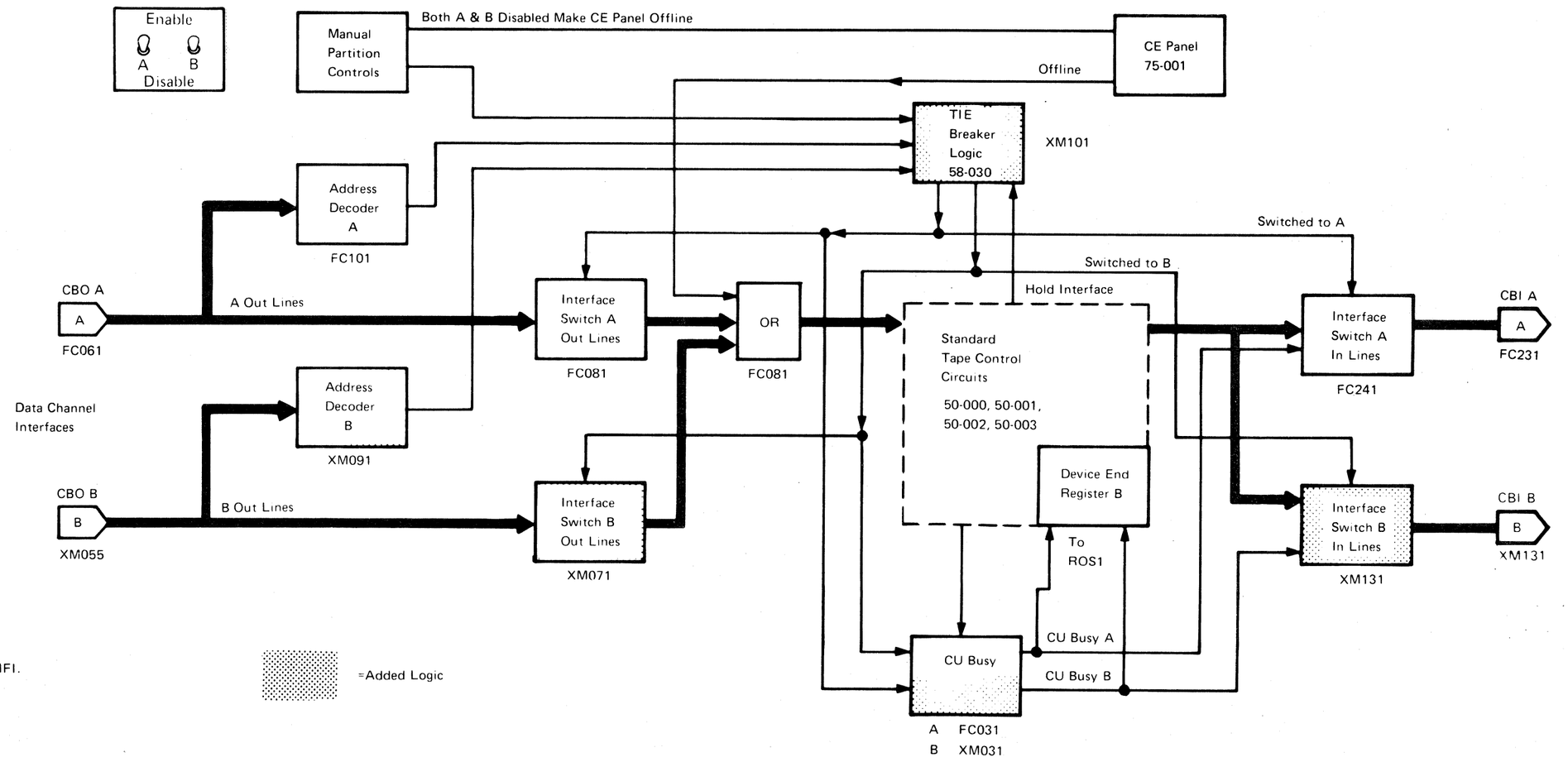
Tie-breaker logic (XM101) controls the interface switch lines so only one channel operates the subsystem, preventing one channel from interfering with the operation of the other. When neither interface is reserved or operating, the interface switch circuits are in a neutral state, and either interface can initiate an Initial Selection sequence.

Address decoders monitor the bus out lines of each interface. If the tape control address appears on the bus out lines along with an ADDRESS OUT tag, the decoders send a signal to the interface switch controls. When no interfering conditions exist, the controls connect that interface to the tape control. If the tape control is reserved or operating with the other interface, a 'short busy' sequence is sent to the interface attempting to break in.

When the tape control becomes available, a Control Unit End status byte is sent to the channel that previously received the BUSY signal.

Two Systems Sharing a Tape Control Through the Use of a Two-Channel Switch





NOTE: [1] TCS is shown as 2CS on logic pages and in the MFI.

=Added Logic

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OPER—TWO-CHANNEL SWITCH (TCS) (Cont'd)

The Sense/Reserve command (F4) locks the two-channel switching circuits to one interface, so the other interface does not have access to the tape control. The Sense/Release command (D4) resets the reserved condition and allows the tape control to accept commands from either interface.

When a tape unit completes an operation, a Device End signal is sent to the channel. A tape control with the Two-Channel switch uses the second Device End LSR to ensure that the Device End is returned to the channel that initiated the operation. See Device End on 58-012.

RESETS

The Reset circuits of the two-channel switch are interlocked so a Reset from one channel cannot disrupt operations on the other channel. A Reset can be accepted only from the operating channel. Resets are further conditioned to prevent a channel from destroying information needed by the other channel.

INTERFACE SWITCH CONTROL

A tape control with a Two-Channel switch monitors addresses on two channel interfaces. When the tape control receives its own address, it tries to start an operation with the interface attempting selection. If the tape control is neither busy nor reserved, the OPERATIONAL IN latch for that interface is activated. If the tape control is busy or reserved to interface A, interface B ADDRESS OUT will be answered with a SHORT BUSY sequence, and vice versa. The interface which received SHORT BUSY will receive a CU END when the tape control is available. If the channel stacks status containing UNIT CHECK or UNIT EXCEPTION, the tape control will remain connected to that interface until status is accepted. If both interfaces attempt selection simultaneously, a tie-breaker circuit resolves the selection. See 58-030.

The purpose of interface switching circuits is to connect the tape control 'common' circuits to whichever interface is operating. To operate with an interface, output from the OPERATIONAL IN latch (FC141) gates interface drivers for the corresponding interface when OPERATIONAL IN is gated by –SWITCHED TO CHANNEL A (or B) (58-030).

The two-channel switch microprogram is entered by branching from Initial Selection (or Ending Sequence) to ensure that data is sent to or from the proper interface.

RESERVE/RELEASE OPERATION

- A Sense/Reserve command locks the tape control to an interface until a Sense/Release command or a Reset is received from that interface.
- A Sense/Release command resets the RESERVE flag to allow operation on either interface.
- A Sense/Reserve or Sense/Release command, while chained, results in Command Reject.
- After Initial Selection, operation of Sense/Reserve and Sense/Release commands are identical to a Sense command.

The Sense/Reserve and Sense/Release commands enable the tape control to remain locked to one interface. Executing a Sense/Reserve command places a tape control under exclusive control of one channel until that channel issues a Sense/Release command. A Sense/Reserve command from channel A or B activates the RESERVE flag for A or B. A Sense/Release command deactivates the RESERVE flag.

Modifier bits, in positions 0,1,2, and 3 of a Sense command byte identify the reserve and release operations. After Initial Selection, modifier bit 2 determines whether the command is a Reserve or a Release. If bit 2 is on, (command code F4) Reserve is indicated. If bit 2 is off, (command code D4) Release is indicated.

SENSE/RESERVE COMMAND [F4]

A Sense/Reserve command locks the tape control to the interface of whichever channel initiated the command.

During Command Out of a Sense/Reserve command, the current command is masked for the F4 configuration. If an (F4) command is recognized, the microprogram checks for chaining (SETRESV). If chaining is not indicated, CURFLAG (20) is set in FLAGS1 (LSR 10) to reserve the tape control. If chaining is indicated, Command Reject is set.

In a valid Sense/Reserve command, bit 2 from the CHANNEL TAGS IN (CTI) register (FC161) prevents resetting the SWITCHED TO CHANNEL A or SWITCHED TO CHANNEL B latch (58-030) and the tape control remains reserved to the operating interface.

Output of the SWITCHED TO A (or B) latch blocks interface switch circuits for the opposite interface (58-030) until a reset or Sense/Release command is received from the operating interface.

SENSE/RELEASE COMMAND [D4]

A Sense/Release command resets the RESERVE flag to allow the tape control to operate with either interface. As in the sense/reserve operation, the Sense/Release command checks for chaining. A valid Sense/Release command leaves position 2 of the CHANNEL TAGS IN register reset so the SWITCHED TO CHANNEL A and SWITCHED TO CHANNEL B latches are reset at the end of each chain of commands.

SELECTION

Address decoders in the tape control continuously monitor both interfaces. If the correct address bits arrive on the bus out lines along with an ADDRESS OUT tag, the SELECT OUT latch is reset. CONTROL UNIT END latch OFF ANDs with a minus output from the SELECT OUT latch to generate TRAP CHANNEL A or TRAP CHANNEL B.

Assume that the tape control is idle and is addressed by channel A. The TRAP CHANNEL A line ANDs with the SELECT SIGNAL CHAN A to set the SWITCHED TO CHANNEL A (tie breaker) latch. SWITCHED TO CHANNEL A ANDs with DELAY SELECT SIGNAL CHAN A to generate INITIAL SELECTION CHAN A.

Once interface A is addressed and selected, it arms the CONTROL UNIT BUSY AND circuit in interface B. If interface B tries to use the tape control during the time interface A is locked onto the switch, the CONTROL UNIT END latch for interface B is set.

When interface A is finished operating, MP1 determines that the Two-Channel switch is installed, and MP2 checks status of the CONTROL UNIT END latches. If either CUE latch is on, MP1 presents CUE status to the interface associated with that latch. The CUE will have a random tape unit address unless presented along with Device End.

PARTITIONING

Partitioning, achieved by operating the Enable/Disable switches, restricts the accessability of the tape control to either channel. Partitioning bypasses SELECT OUT and degates all interface functions. When both interfaces are partitioned (both switches set to DISABLE), the tape control is offline and the CE panel controls can be used.

IMPLICIT CONNECTION

An implicit connection is one that does not depend on program intervention for release. The duration of the connection is determined by the time required for the tape control to perform a command or a chain of commands. The switch reverts to neutral on completion (at the tape control level) of the last command in a chain.

An implicit connection is extended if the channel stacks primary status. The stacked status must then be accepted by the channel to terminate the connection. If the status byte contains Unit Check, a contingent connection is made and acceptance of the status by the channel does not terminate the connection.

If the channel stacks secondary status containing Unit Exception or Unit Check, connection to that channel will be maintained until the status is accepted by the channel. If the status byte contains Unit Check, a contingent connection is made and acceptance of status by the channel does not terminate the connection.

If the channel stacks secondary status other than Unit Check or Unit Exception, the switch returns to neutral and is available to either channel. Any further attempts by the tape control to present this status to the channel that indicated STACK STATUS are controlled by SUPPRESS OUT from that channel.

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CONTINGENT CONNECTION

A contingent connection is initiated when the last status byte contains Unit Check. The connection is maintained until a command other than Test I/O or NOP is received from the channel to which status was presented. Any command other than Test I/O or NOP to that tape unit clears the contingent connection if the tape unit is READY.

The purpose of the contingent connection is to ensure an available path to the tape unit and the transmission of sense data from the tape unit to the proper channel. If a Test I/O or NOP is issued by the addressed channel to a tape unit other than the one contingently connected, the tape control responds with SHORT BUSY and retains the connection.

BUSY

While the tape control is operating with one interface, a SELECT from the other interface will be answered with a SHORT BUSY signal (Bits P, 1, 3). Assume that the B interface is operating when the A interface attempts to address the tape control (58-030). The SWITCHED TO CHANNEL B latch blocks the setting of the SWITCHED TO CHANNEL A latch. However, –SELECT SIGNAL CHANNEL A is ANDed with –ADDR COMPARE CHAN A and NOT PROPAGATE SEL OUT CHAN A to reset the CHANNEL A SEL OUT latch. With the latch reset, the minus output of the off side of the latch is ANDed with –ENABLE CHAN A and OPERATIONAL IN to condition one input to the channel A CUE latch. A second conditioning input is OPERATIONAL IN, and the third is the minus output from the CU BUSY AND circuit. Thus, the CUE latch for channel A, is turned on to send CU BUSY STATUS CHAN A to the A interface.

The BUSY signal sent to channel A is a Unit Status byte with bits 1 and 3 on. Bit 3 indicates BUSY, while bit 1 (status modifier) indicates that the BUSY condition applies to the tape control. Bits P, 1, and 3 are forced onto the BUS IN lines at the same time the STATUS IN tag line is forced up. The STATUS IN latch is not turned on during this SHORT BUSY sequence.

CONTROL UNIT END

The CONTROL UNIT END latch (58-030) remains on, remembering that channel B tried to break into channel A operations. This latch also sends +CUE PENDING CHAN B to the microprogram branch-on-condition logic (AB161) to notify the B interface that a Channel End is pending. When the tape control is no longer operating with, or reserved by, interface A, the SW TO CHAN A latch turns off, –TRAP CHAN B is active, and the SELECT CHAN B line is still active to turn on the SW TO CHAN B latch.

The SW TO CHAN B latch gates the output from OPERATIONAL IN to channel B to send a Unit Status byte to channel B. The status byte will contain a CUE (bit 2) indicating the tape control is now available for other operations. A standard REQUEST-IN sequence is used to transmit the CUE status byte.

At the end of an operation, the SW TO CHAN A (or B) latch is reset unless a chain, STACK, INTERRUPT, or UNIT CHECK condition exists. OPERATIONAL IN is reset in the Burst Ending Sequence when CHANNEL TAGS IN register bit 7 is reset.

With OP IN reset, no REQUEST IN, no ADDRESS OUT, and no SELECT OUT for the tape control, the SELECT OUT latch is active. (Note that the SELECT OUT latch is turned on when the tape control is inactive.) With the SELECT OUT latch active, the plus output degates –RESPONDING TO CHAN A (or B). –RESPONDING TO CHAN A (or B) inactive resets the SW TO CHAN A (or B) latch, and the tape control is available for another selection sequence.

STACK

In some cases the channel may refuse the end status byte, this turns on a 'stack' condition. If the status byte contains Unit Check or Unit Exception, the tape control remains connected to that interface until the channel accepts the status. If the status byte contains Unit Check, the connection is maintained until a command other than NOP or Test I/O is received from the channel to which the status was presented. This procedure makes certain the channel has an opportunity to interrogate a unit check condition before the other channel disturbs the tape control. When the interface connection is maintained because of a unit check, the connection is defined as "contingent" (not part of the normal routine).

Stacking of status other than Unit Check or Unit Exception does not maintain the interface connection. The TCS will be reset to neutral, and the tape control will become available to either channel.

STACK INTERRUPT

A Halt I/O command received by the tape control before the channel accepts the ending status causes the MP1 microprogram to reset OP IN and check for two-channel operation and contingent connection. If a contingent connection is needed to prevent loss of error information, the microprogram branches to a 'Hold Interface' routine.

With no contingent connection, an interrupt cycle is initiated to present the stacked status. CONTROL UNIT BUSY will be reset (if applicable) and HOLD INTERFACE will be set if the STACK or STATUS PENDING flag is on.

DEVICE END

The purpose of Device End circuits is to signal the data channel when a tape unit has completed a task and is ready to accept a new one. On a tape control with the two-channel switch feature, separate LSRs in MP2 are used to store the Device End signal for each channel. The second Device End LSR ensures that the Device End is returned to the channel that initiated the operation.

A Device End received while the two-channel switch is in a neutral state causes the tape control to enter an interrupt status. The tape control then presents the Device End to the channel that initiated the Device End operation, if that interface has not been partitioned. Partitioning resets pending Device Ends for that interface.

An interrupt due to a Control Unit End sends Device End, including the address of that device, and Control Unit End, to the channel.

TIE BREAKER

Tie-breaker logic (XM101) on 58-010) controls the interface switch lines so only one channel operates the subsystem, preventing one channel from interfering with the operation of the other. When neither interface is reserved or operating, the interface switch circuits are in a neutral state, and either interface can initiate an Initial Selection sequence.

Address decoders monitor the bus out lines of each interface. If the tape control address appears on the bus out lines along with an ADDRESS OUT tag, the decoders send a signal to the interface switch controls. When no interfering conditions exist, the controls connect that interface to the tape control. If the tape control is reserved or operating with the other interface, a 'short busy' sequence is sent to the interface attempting to break in.

When the tape control becomes available, a Control Unit End status byte is sent to the channel that previously received the BUSY signal.

See 58-030 for schematic details.

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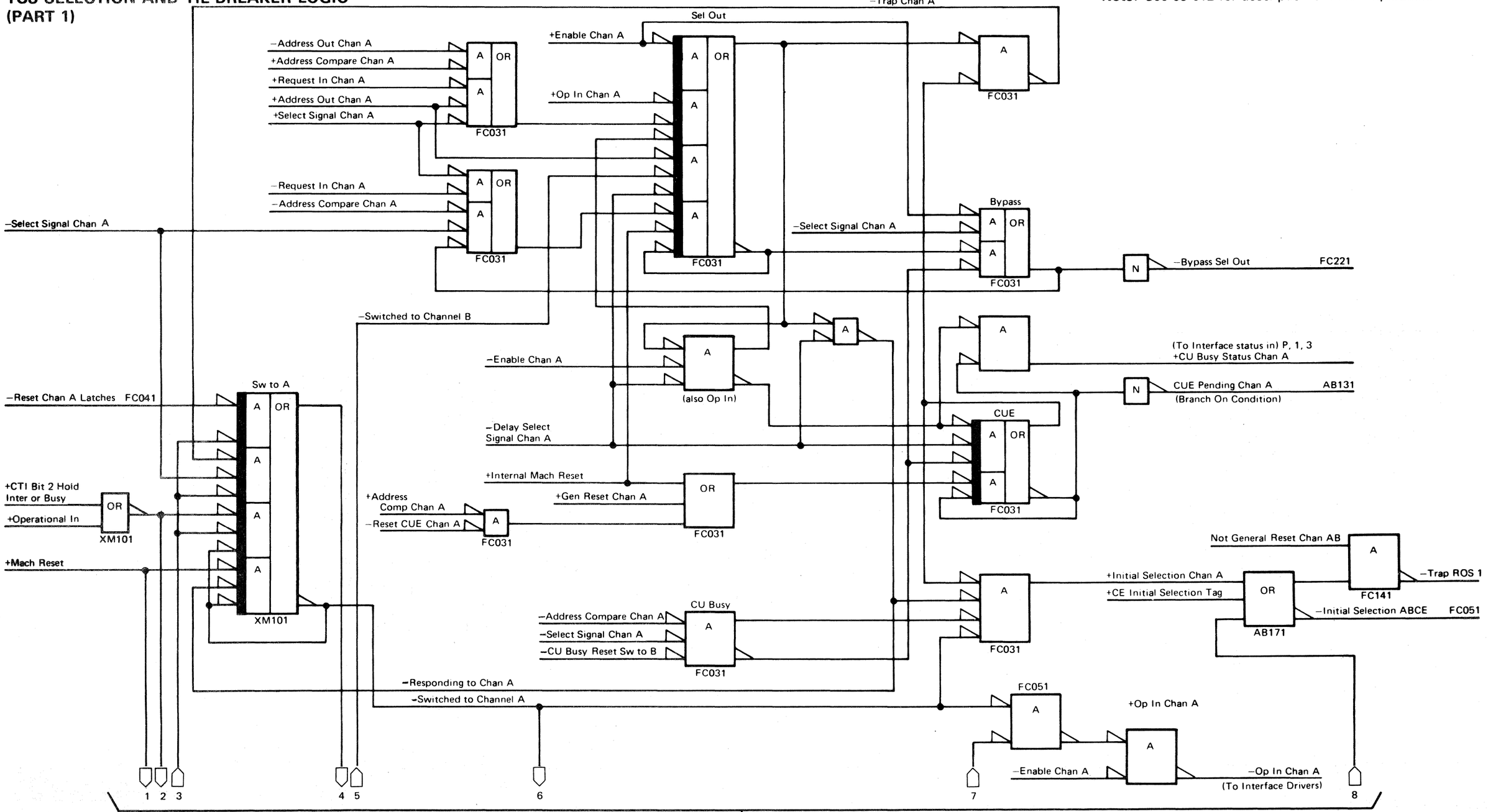
TCS SELECTION AND TIE-BREAKER LOGIC (PART 1)

Note: See 58-012 for description of circuit operation.



58-031

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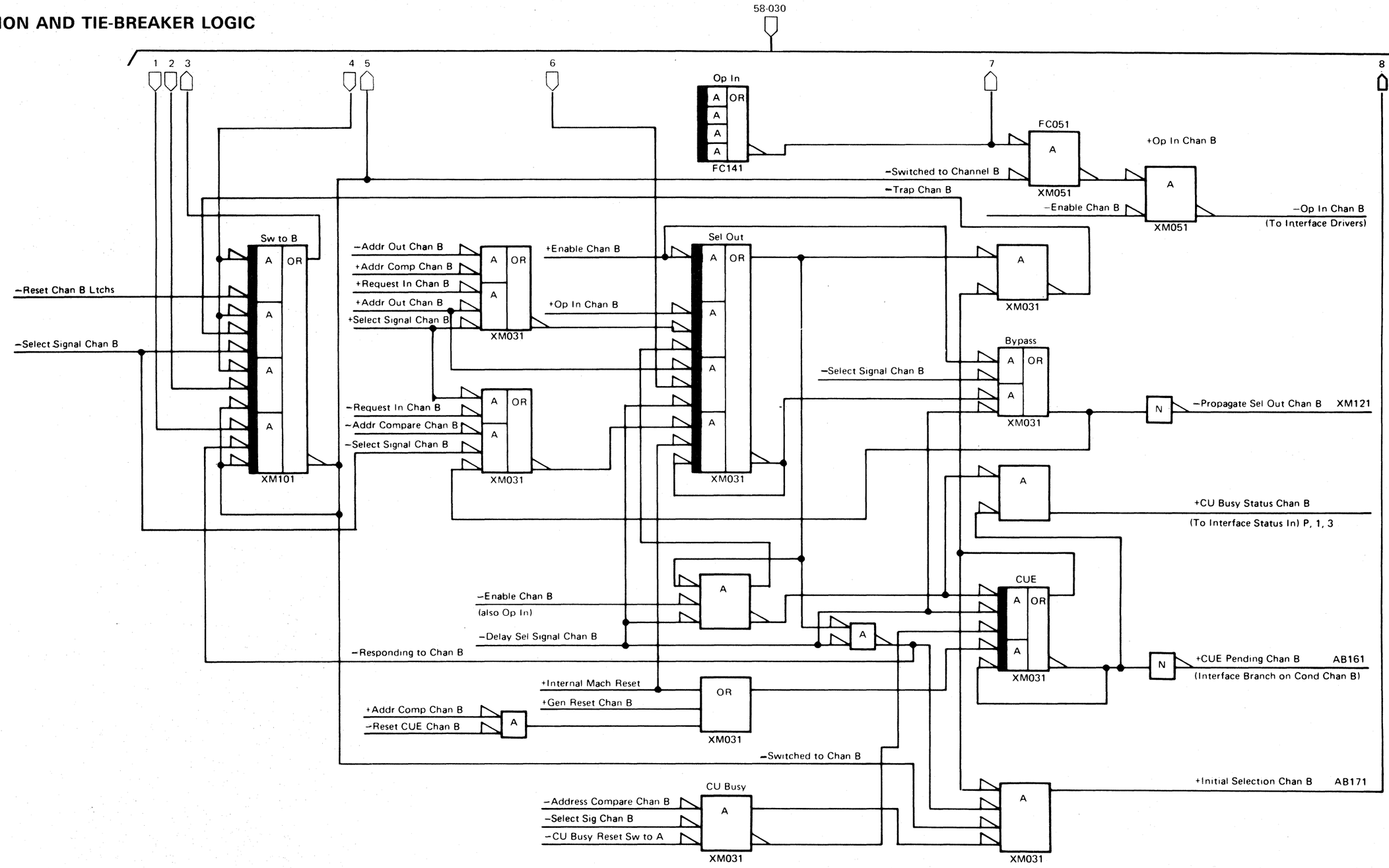
TCS SELECTION AND TIE-BREAKER LOGIC (PART 2)



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DESCRIPTION

Device switching allows access to a maximum of sixteen tape units by two, three, or four tape controls, and permits simultaneous operation of as many tape units as there are tape controls.

3803 Models 1 and 2 can be mixed in a switching configuration; however, attempting to access a 3420 Model 4, 6, or 8 through a 3803 Model 1 produces unpredictable results.

Device switching is performed via the Communicator and Device Switch features. Three Device Switch features (58-051) available with the tape subsystem are:

- 2 Control Switch used with 2x8 and 2x16 configurations
- 3 Control Switch used with 3x8 and 3x16 configurations
- 4 Control Switch used with 4x8 and 4x16 configurations

The minimum switching subsystem configuration allows two tape controls to access up to 8 tape units and is called a 2x8 configuration. The maximum configuration is 4 tape controls and 16 tape units (4x16). A non-switching configuration (1x8) is referred to as Selection Logic.

Device Switching logic is installed only in those tape controls that have attached tape units.

The location of the Device Switches depends on the configuration desired. For example: In a 2x8, 3x8, or 4x8 configuration, the switching feature is required only on the first tape control while in the 2x16, 3x16, and 4x16 configurations, the switching feature is required on Tape Controls 1 and 2 (58-051). The 2x16 configuration consists of two tape controls, each with a Communicator 1, a 2 Control Switch, and eight tape units. The tape controls may be connected to either different channels of the same system or on different systems.

Device switching logic is logically invisible (except for BUSY responses during Initial Selection and Device End interrupts, which result when tape units become available). Device switching logic is modular to allow flexibility for a variety of system configurations. Subsystem priority and device addressing are assigned by pluggable jumpers within the switch. Any tape unit may be partitioned (made unavailable) to any tape control via toggle switches on the tape control operator's panel (58-060).

2 Control Switch

The 2 Control Switch is a 2x8 configuration of hardware switching logic (58-051, 58-055). Tape Units 0 - 7 (attached to Tape Control 1) can be accessed by the Communicator in Tape Control 2 as well as the Communicator of Tape Control 1. A 2x16 configuration is obtained by installing a 2 Control Switch in both Tape Controls 1 and 2, allowing the Communicator in each tape control to access its own eight 3420s, as well as 3420s of the other tape control.

3 Control Switch

A 3x8 configuration is obtained by installing a 3 Control Switch in Tape Control 1 only and a Communicator 1 in Tape Controls 1, 2, and 3 (58-051). Tape units attach to Tape Control 1.

A 3x16 configuration is obtained by installing a 3 Control Switch in both Tape Controls 1 and 2. A third tape control must be added to the configuration. Tape Control 3 does not contain any switching hardware or attach any tape units, but does contain a Communicator.

4 Control Switch

A 4x8 configuration is obtained by installing a 4 Control Switch in Tape Control 1 and a Communicator 1 in Tape Controls 2, 3, and 4 (58-051). Tape units attach to Tape Control 1.

A 4x16 configuration is obtained by installing a 4 Control Switch in both Tape Controls 1 and 2. Two more tape controls must be added to the configuration. Tape Controls 3 and 4 do not contain any switching hardware or attach any tape units, but each contains a communicator.

The 3 Control Switch and the 4 Control Switch are expansions of the 2 Control Switch. They allow access to eight attached tape units by the additional Communicators.

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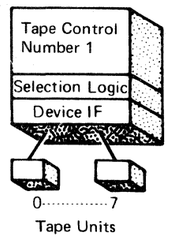
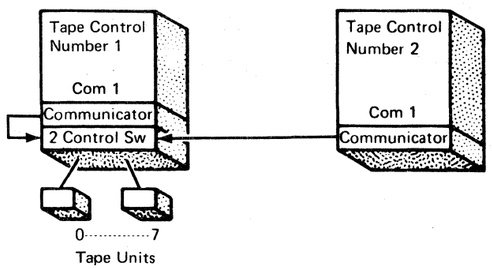
1 x 8 Configuration



2 X 8 Configuration



Notes:

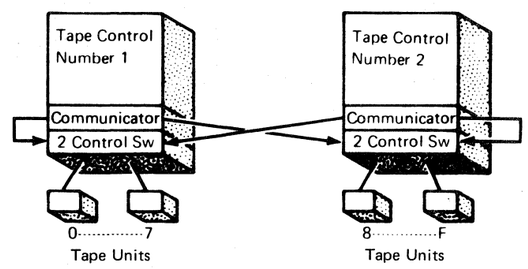
[1] Maximum of 16 tape units and 4 tape controls.

[2] Tape units attach only to tape controls with switching features.

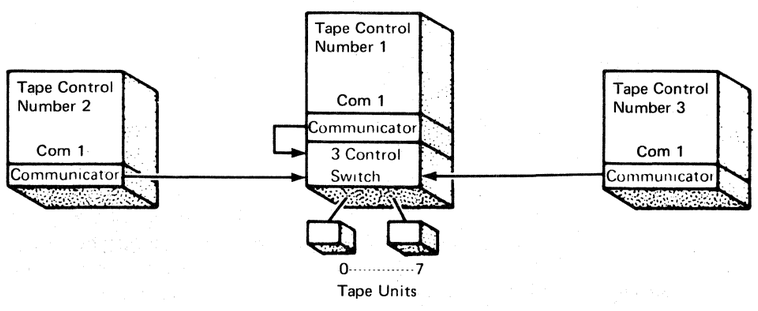
[3] Any or all control units may have two channel switch features.

[4] For 3420 Model 8 power requirements, see 90-180.

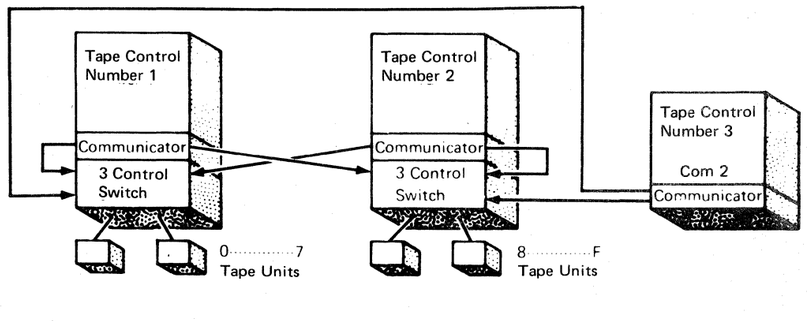
2 x 16 Configuration



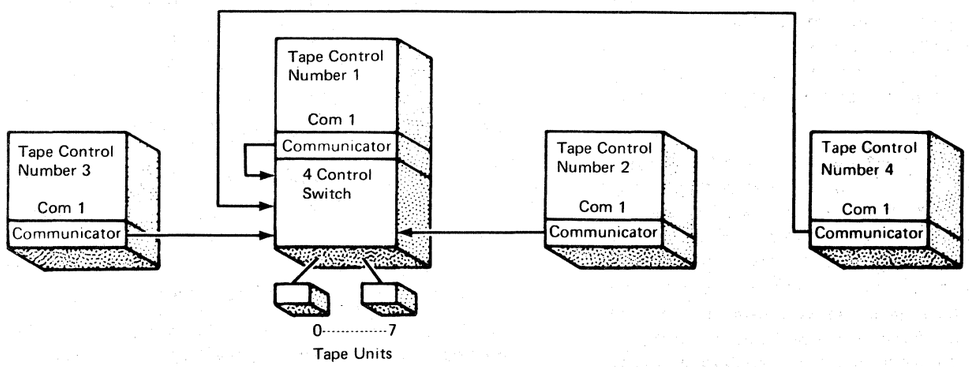
3 X 8 Configuration



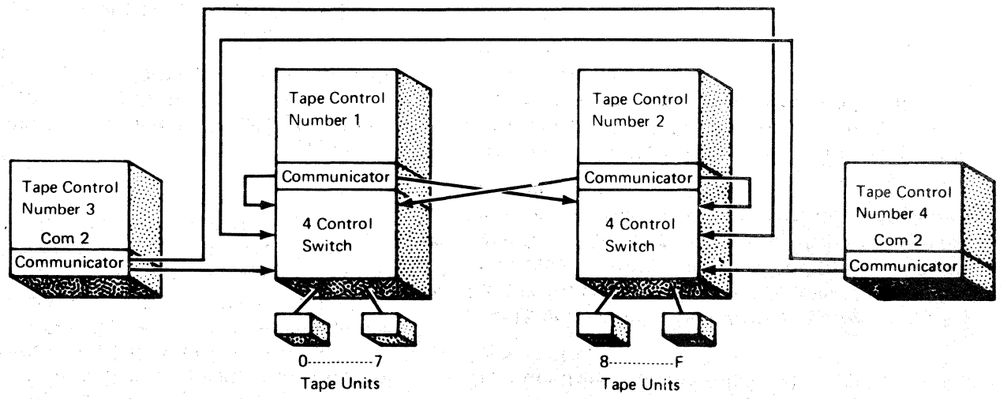
3 x 16 Configuration



4 x 8 Configutation



4 x 16 Configuration



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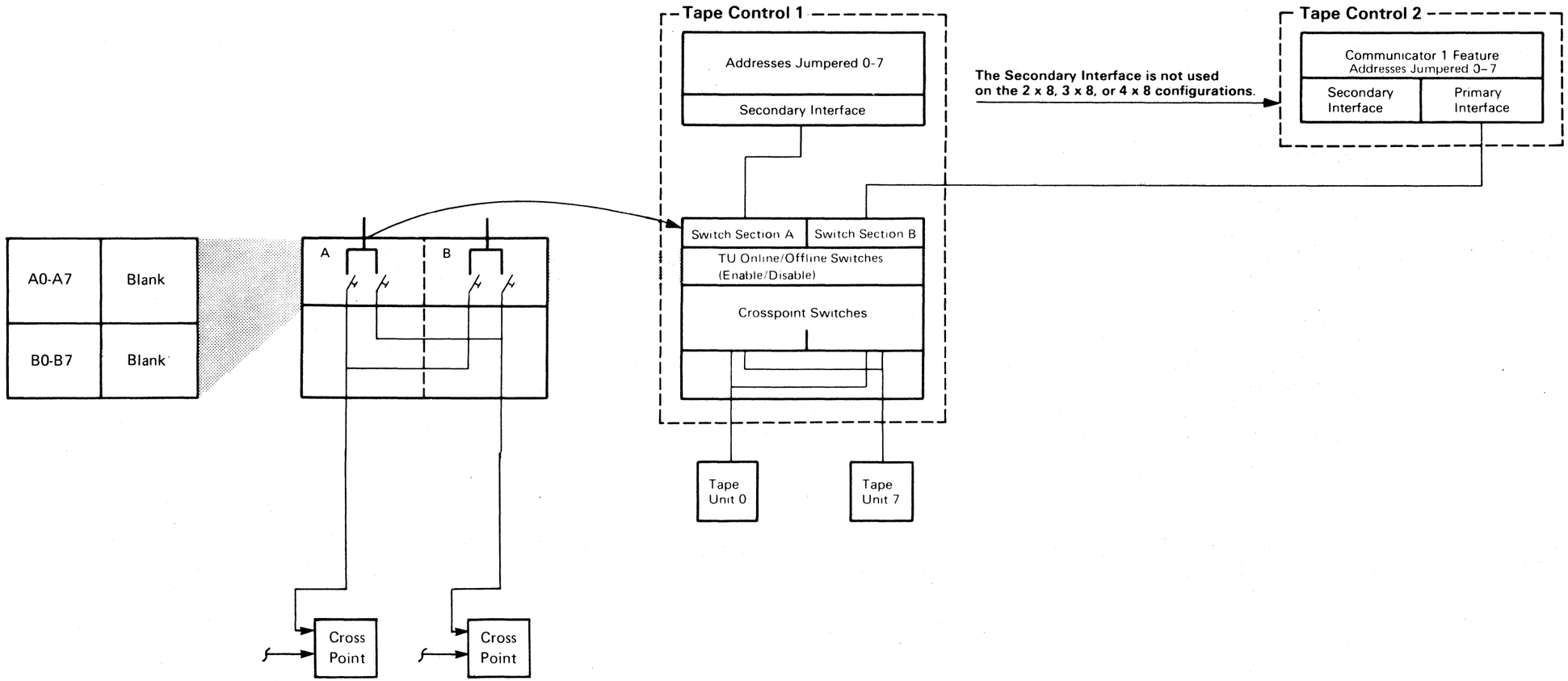
58-051

OPER—2x8 SWITCH LOGIC

OPERATOR PANEL SWITCHES (16)

Switch Section A on Tape Control 1 directs Tape Control 1's access path to Tape Units 0-7. Switch Section B on Tape Control 1 directs Tape Control 2's access to Tape Units 0-7.



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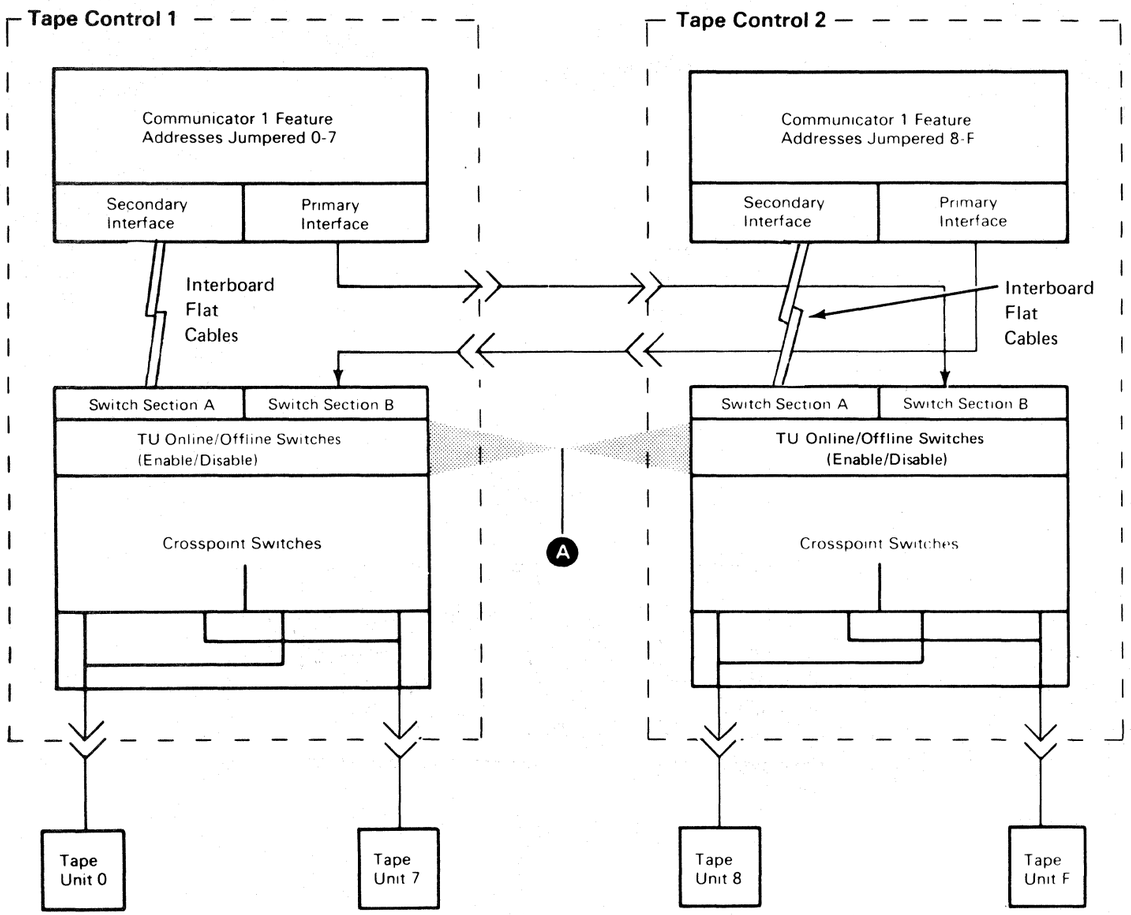


Switch section A on tape control 1 directs tape control 1's access path to tape units 0-7. Switch section B on tape control 1 directs tape control 2's access to tape units 0-7.

Tape control 2 switches are similar to tape control 1, except section A directs tape control 2's access to tape units 8-F. Section B controls the access of tape control 1 to tape units 8-F.

OPERATION

The Device Switch is controlled by lines from the tape control. Although there are necessary switching delays, data transfers, control requests, and responses, tape unit status is sent to the tape control as if the switch were not present.

Selection: When DEVICE SELECT (58-090) is activated, with the device address on the DEVICE SWITCH bus and the node is enabled, the switch tries to set the COMMITTED latch for the node. **Note:** A "node" is the logic circuitry required to select and assign one tape unit to a requesting tape control. If the device has already been selected by another tape control, a BUSY indication is returned to the tape control attempting selection. If the device is not busy, the COMMITTED latch is set. The latch output is then sent to the other tape control nodes for that device to prevent selection by them. At the same time the committed latch is set, the SELECT crosspoint line to that node will become active and GATE BUS OUT will be the response to the selecting tape control. The BUS OUT and BUS IN connection has now been established between the tape control and tape unit. SWITCH SELECT is not required to select a tape unit, although it is always active in 3803 subsystems.

Committed: Once the COMMITTED latch is set for a given node, it remains set until reset by the selecting tape control. Reset is accomplished by addressing and sending a 50 ns pulse on the SET/RESET line.

Priority: When two or more tape controls attempt to select a tape unit at the same time, priority of access is determined by jumpers plugged on Tape Controls 1 and 2 (58-100). See Section 90 for plugging details.

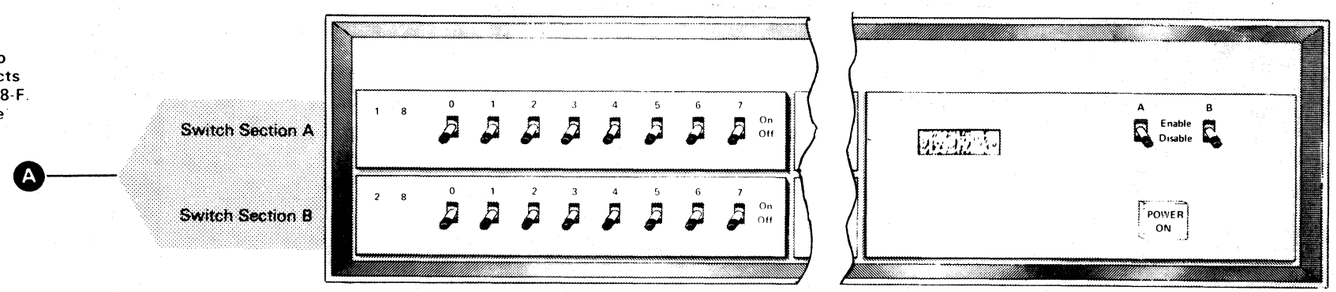
LINE DEFINITIONS (58-100)

Busy/Tach: The BUSY/TACH line indicates the state of the device (busy or not busy) to the tape control.

Device Operating Interface A and B (2 lines): A device operating line is active when a committed tape unit (one for which a COMMITTED latch has been set) has its BUSY/TACH line active. The DEVICE OP INTF A line to the tape control is used for generating the METERING IN line for its channel interface. The DEVICE OP INTF B line serves the same function but is used by the second channel interface when the Two-Channel Switch feature is installed.

Run Meter: When the node is enabled, the RUN METER line is sent to the device for meter operation.

Set/Reset: The SET/RESET line is tied active so the ENABLE/DISABLE latch can be set to the corresponding state of the Enable/Disable switch on the operator's panel.



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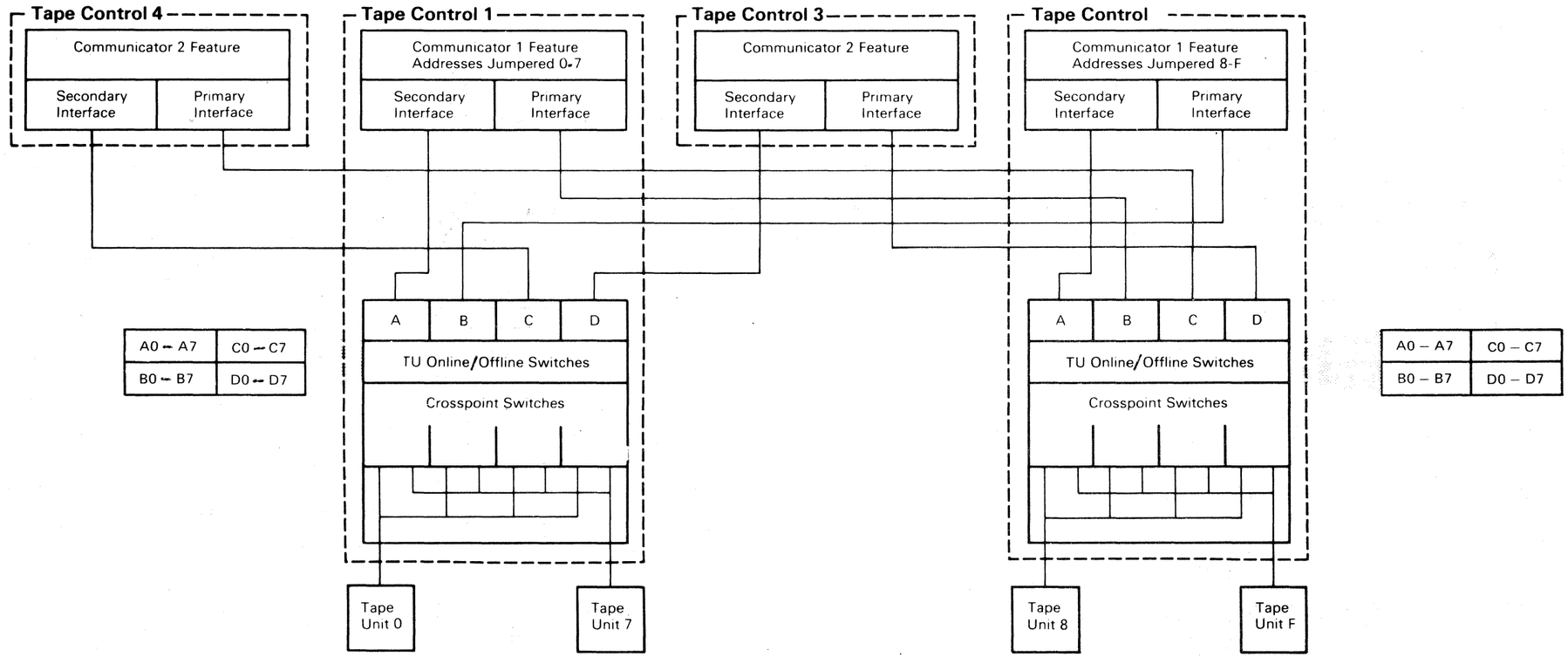
Notes:

[1] The maximum switch configuration consists of 16 tape units and 4 tape controls.

[2] Tape units attach only to the tape controls with device switching features.

[3] Any or all tape controls may have a Two-Channel Switch feature.



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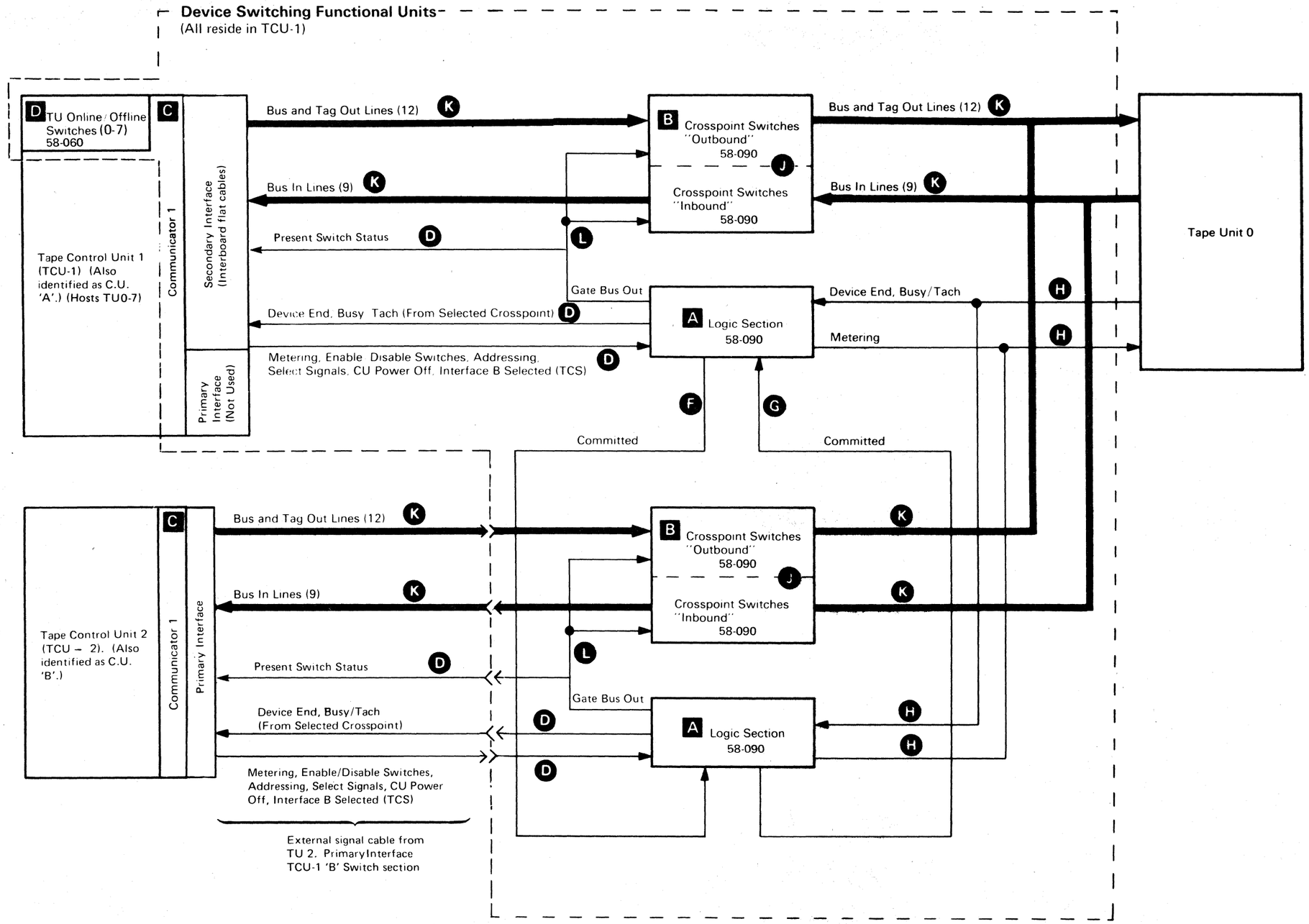
Functional Units of the Device Switch are:

- Ⓐ **Logic Section:** The logic section communicates with the tape control to provide status, device address, and accessing interlocks. The information exchanged establishes tape unit attachment to the tape control and presents switch status to the operating tape control or controls in the subsystem configuration.
- Ⓑ **Crosspoint Section:** The crosspoint section is a switch matrix capable of switching twelve inbound and twelve outbound lines. Each node (tape control/tape unit path) is controlled by the logic section.
- Ⓒ **Communicator:** The communicator replaces the selection logic circuits and associated device interface cabling in the basic tape control with different logic circuits and cabling to the device switches. The communicator divides the device interface into primary and secondary and controls the gating of each according to the address of the device being selected. The communicator consists of interface drivers and receivers.

The Communicator 1 feature has only one external (primary) interface. The Communicator 2 feature has two external interfaces (primary and secondary). The secondary interface connects attached tape units through Switch Section A (58-055, 58-060). The primary interface connects a 3803 that does not have tape units attached to another tape control through Switch Section B.

- Ⓓ **Tape Unit Online/Offline Switches:** Tape unit toggle switches (58-060, 58-100) are located on the operator's panel of each tape control having a device switch feature. These switches enable the operator to determine tape unit availability to each tape control in the configuration. In a 4x16 configuration, four tape controls can access 16 tape units so there are 64 toggle switches, 32 each on Tape Controls 1 and 2. There are no switches in Tape Controls 3 and 4.

Note: Ⓐ, Ⓓ, Ⓕ, Ⓖ, Ⓗ, Ⓚ, Ⓛ refer to charts located in ALD XC-700 pages.



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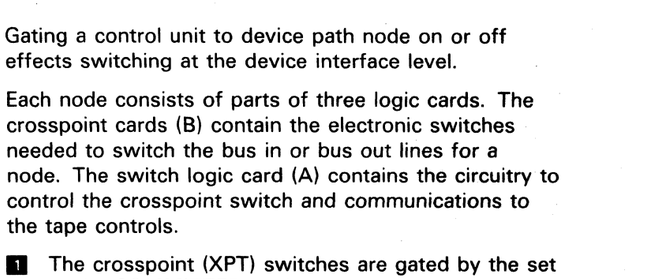
58-080

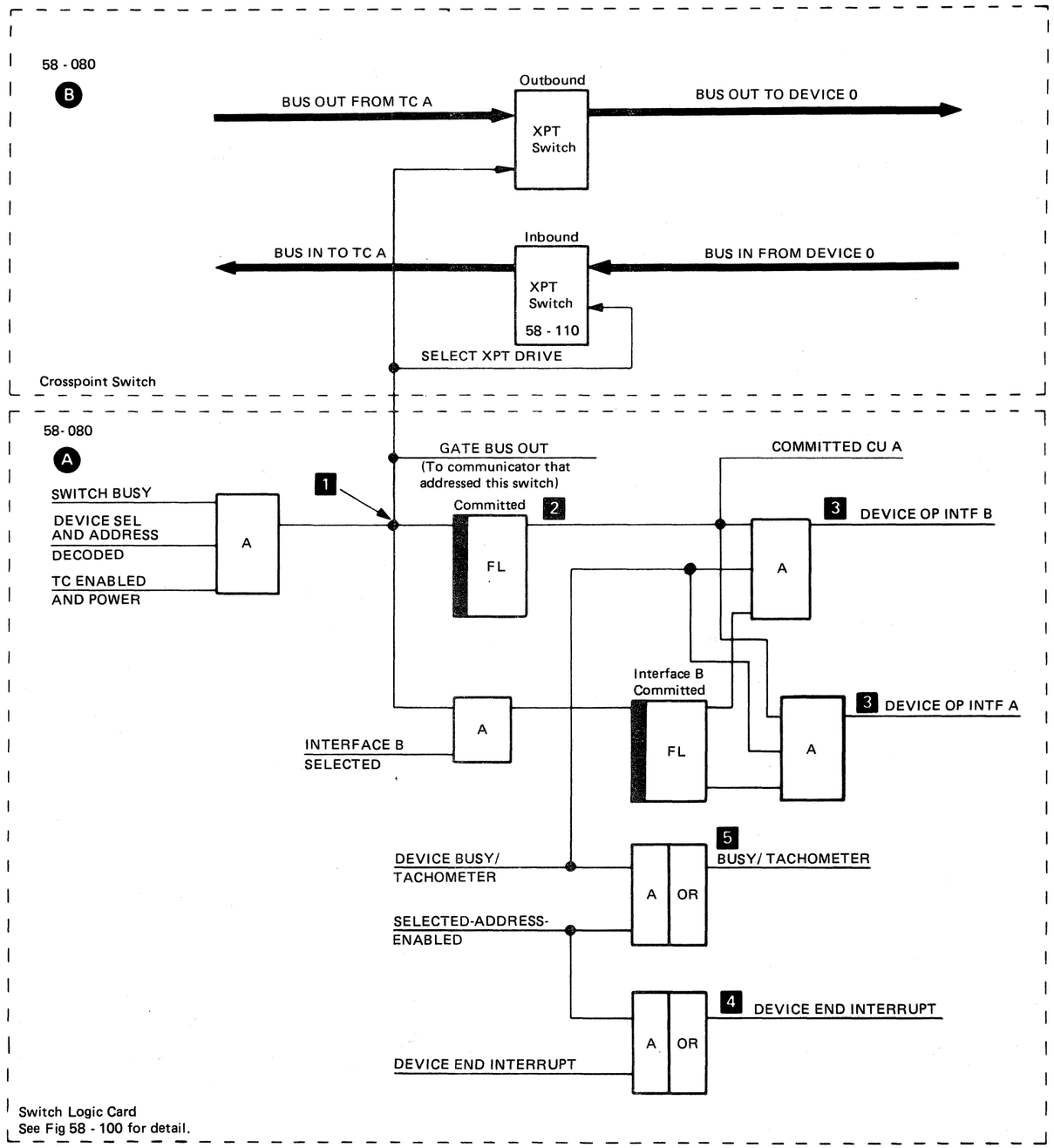
OPER—DEVICE SWITCH NODE

Gating a control unit to device path node on or off effects switching at the device interface level.

Each node consists of parts of three logic cards. The crosspoint cards (B) contain the electronic switches needed to switch the bus in or bus out lines for a node. The switch logic card (A) contains the circuitry to control the crosspoint switch and communications to the tape controls.

1. The crosspoint (XPT) switches are gated by the set to the COMMITTED latch.
2. COMMITTED lines prevent simultaneous selection of the same device by more than one tape control.
3. INTERFACE COMMITTED, COMMITTED, and DEVICE BUSY are ANDed to generate DEVICE OPERATIONAL, which is sent to the tape control to develop METER IN for the channel interface.
4. DEVICE END INTERRUPT lines are scanned by the tape control to determine which tape unit has a DEVICE END INTERRUPT pending.
5. BUSY/TACH is available to the tape control when the node is selected and enabled and the DEVICE BUSY or SWITCH BUSY line is inactive.





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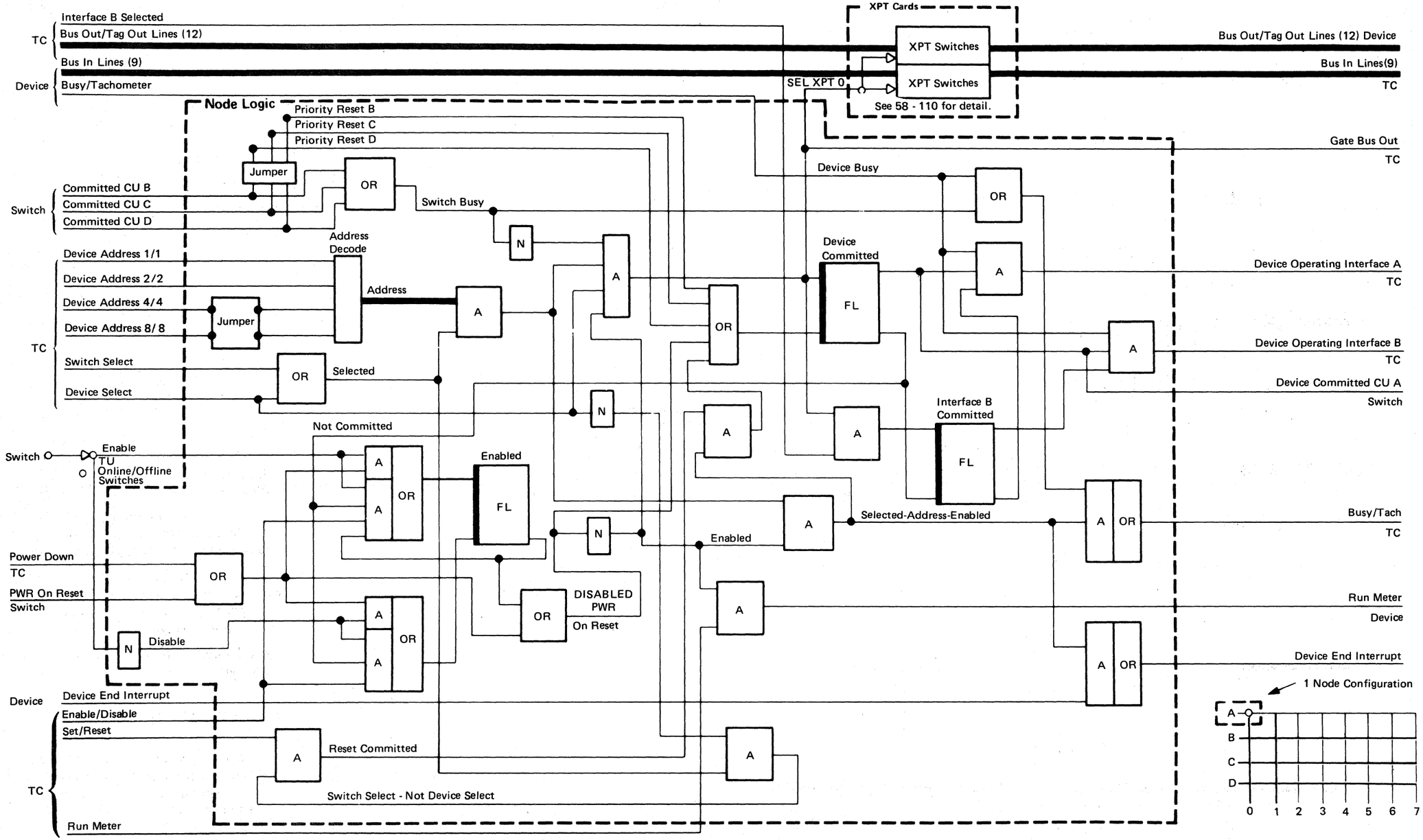

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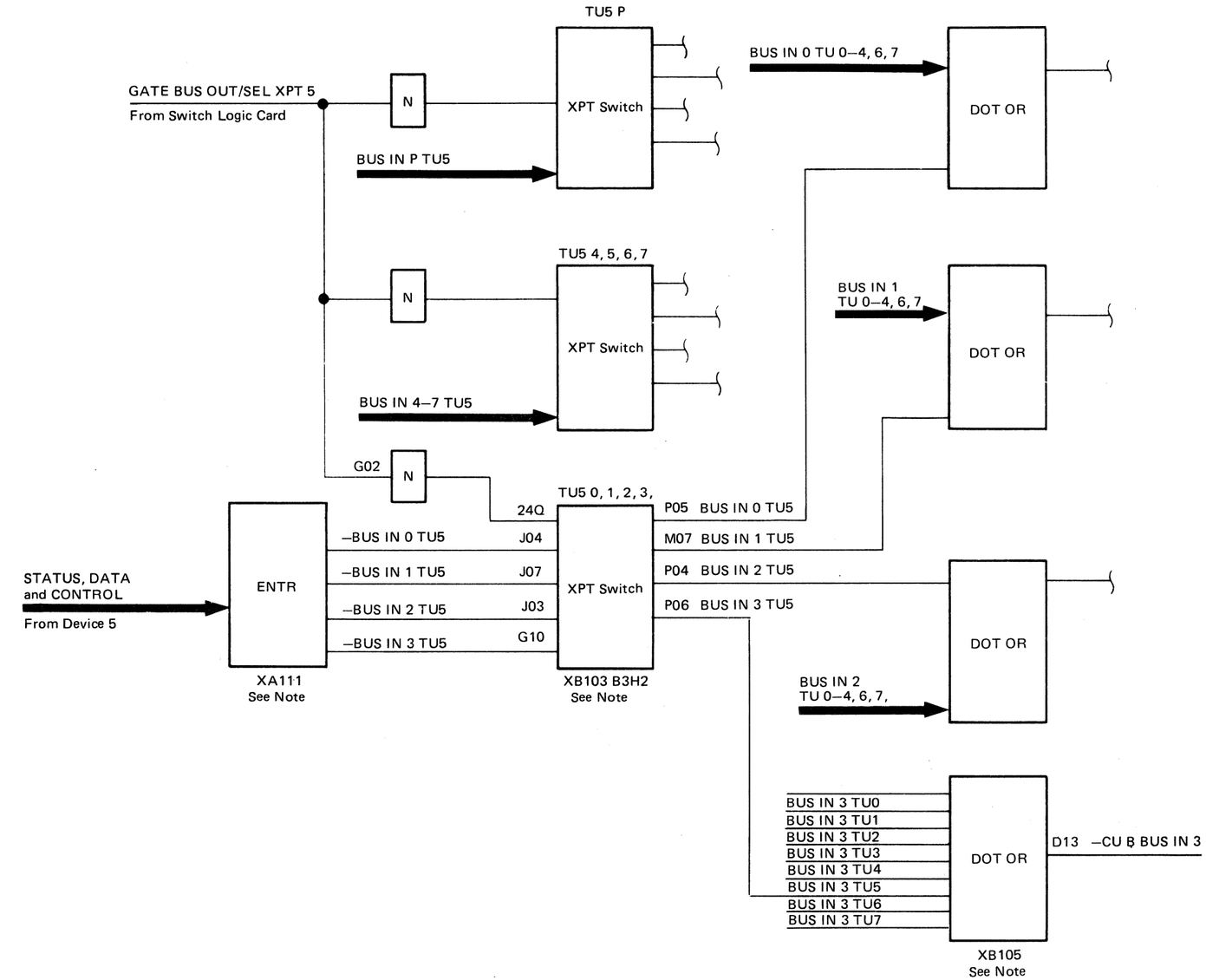

Note: See ALD pages XCnnn.

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NOTES:

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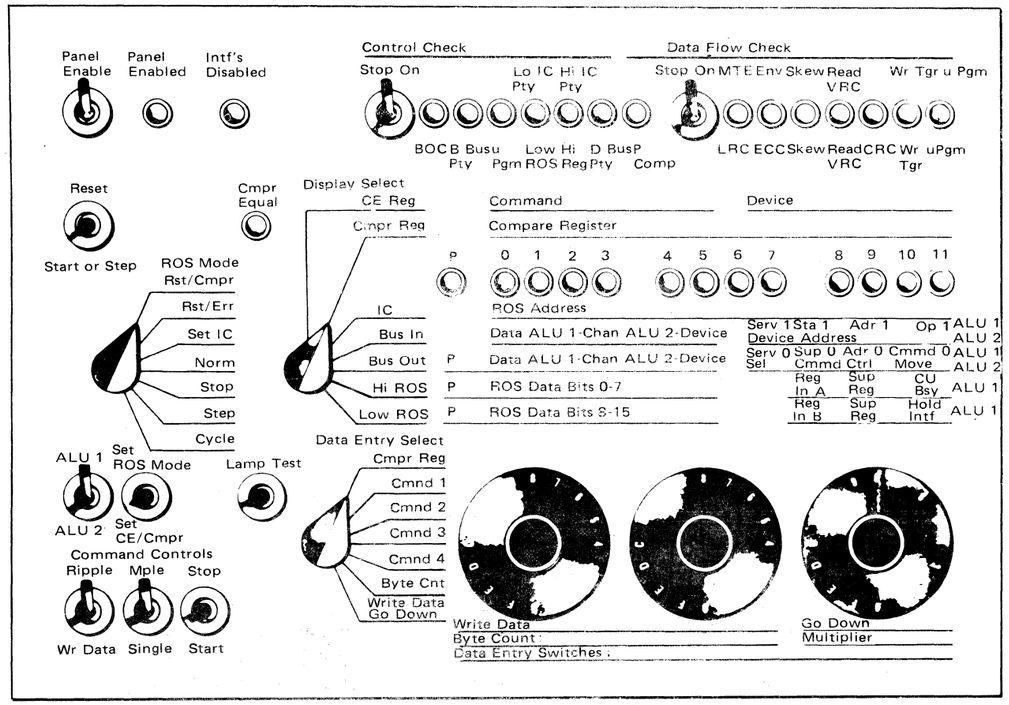
3803 CE PANEL DESCRIPTION



CE PANEL SWITCHES

PANEL ENABLE (TWO-POSITION TOGGLE)

Active only if ROS is in normal mode. It may be necessary to raise the Set ROS Mode momentary switch to establish this mode. The Panel Enabled light is ON when the switch is ON.

Note: If the Panel Enabled light does not light, set the ROS Mode rotary switch to Norm and operate the Set ROS Mode switch (momentary).

On

Allows the CE panel functions identified by yellow lettering to be performed with the Interface Disabled light either on or off.

Allows all CE panel functions to be performed with the Interface Disabled light On.

Off

Degates the following functions:

1. Stop On—Control Check
2. Stop On—Data Flow Check
3. Reset/Start or Step
4. ROS Mode
5. Command Control switches (3)

STOP ON-CONTROL CHECK (TWO-POSITION TOGGLE)

Active only while ROS is in Stop mode.

On

Stops both ALUs when any control check is recognized in the ALU selected by the ALU1/ALU2 switch. The exact stopping location depends on the type of error; it is usually two less than the stop address except for a BOC. Generally, microprogram-detected errors will not be recognized until a transfer hardware error (XFR HDWERR) microinstruction is executed. Most other errors will stop the ALUs when the failure occurs.

Disables the compare register equal features of the ROS Mode switch Stop position.

Off

Allows normal tape control operation.

RESET/START OR STEP (TWO-POSITION MOMENTARY TOGGLE)

Active only while the Panel Enabled light is On.

Reset (UP)

Sets both ALUs to Instruction Counter (IC) address 000 and causes a Power-on Reset Branch Condition.

Start or Step (Down)

Starts both ALUs after a stop condition, with subsequent running of the ALUs controlled by the ROS Mode switch. Also resets the Compare Equal light at any time without interlocks.

STOP ON-DATA FLOW CHECK (TWO-POSITION TOGGLE)

Active only while Interface Disabled light is On (CE Mode).

On

Stops both ALUs at the completion of a command in which a failure occurs on Unit Check condition.

Off

Normal tape control operation.

Note: When in CE Mode, the tape control stops on Unit Exception, regardless of switch position. To inhibit a Stop-On-Unit-Exception when tape control is in CE Mode, jumper AA1T2J12 to ground.

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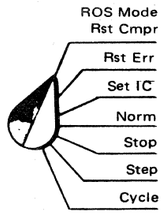
LAMP TEST (TWO-POSITION TOGGLE)

Allows you to test the CE panel indicator lights.

ROS MODE (SEVEN-POSITION ROTARY)



Active only while the Panel Enabled light is On. After selecting any of the seven positions of the ROS Mode switch, activate the Set ROS Mode momentary toggle switch to set the mode.

Rst/Cmpr

When the IC address of the selected ALU equals the data in the compare register, both ALUs are reset to location 000 and allowed to continue running. (The Display Select switch must be in IC position.)

Rst/Err

When a control check occurs, both ALUs are reset to location 000 and allowed to continue running.

Set IC

Allows the contents of the compare register to set IC of the ALU selected by the ALU1/ALU2 switch.

Norm

Normal running condition of both ALUs.

Stop

When the data in the compare register equals the IC address of the ALU selected by the ALU1/ALU2 switch, and the Display Select switch is in IC position, both ALUs are stopped. The instructions at the stopped addresses will not have been executed.

When the Stop On-Control Check switch is active, both ALUs are stopped only when an error occurs in the ALU selected by the ALU1/ALU2 switch.

Note: If compare equal stop function does not work, make sure the Control Check Stop switch is off.

Step

Operating the Start or Step momentary switch allows stepping the ALU selected by the ALU1/ALU2 switch, while the ALU not selected runs normally.

Cycle

Allows the repetitive execution of an instruction at a selected address. Step or stop at the instruction address on which you want to cycle. Set ROS Mode to Cycle and press Start or Stop.

ALU1/ALU2 (TWO-POSITION TOGGLE)

Selects the ALU to be controlled by the ROS Mode switch.

Selects the ALU when the Display Select switch is set to the IC, Bus In, Bus Out, Hi ROS, or Low ROS position.

SET ROS MODE/SET CE COMPR (TWO-POSITION MOMENTARY TOGGLE)

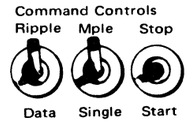
Set ROS Mode

Sets the selected ROS mode.

Set CE/Compr

Sets the data, selected by the three hex rotary switches into the register selected by the Data Entry Select switch. The Set CE/Compr switch operates without the panel enabled or the interface disabled.

COMMAND CONTROLS



Active only while the Intf's Disabled light is on.

Ripple/Wr Data

Establishes the data pattern mode for offline write commands.

Mple/Single

MPLE allows continuous cycling of the four commands entered with the Data Entry Select switch.

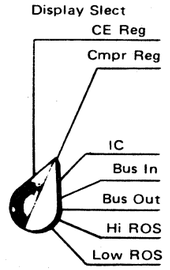
SINGLE allows single stepping of the four commands with each activation of the momentary Start switch.

Stop/Start

STOP halts the continuous cycling of the four commands when the Mple/Single switch is in the MPLE position.

START initiates the commands stored in the CE command registers.

DISPLAY SELECT (SEVEN-POSITION ROTARY)



CE Reg

1. Displays command/device in conjunction with Data Entry Select.
2. Displays Write Data/Go Down or Byte Ct/Multiplier in conjunction with Data Entry Select.

Note: Some stop-on-error conditions stop the CE clock, which prevents displaying the contents of the CE registers.

Cmpr Reg

Displays data currently in the compare register in indicators 0 through 11.

IC

Displays the IC address of the selected ALU in indicators 0 through 11.

Bus In

With ALU1 selected, displays Channel Bus In data in indicators 0 through 7 and In Tags in indicators 8 through 11.

With ALU2 selected, displays TU Bus In data in indicators 0 through 7 and the device address in indicators 8 through 11.

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Bus Out

With ALU1 selected, displays Channel Bus Out data in 0 through 7, and outbound control or tags in 8 through 11. Parity is only assured when the microprogram activates CHANNEL BUS OUT.

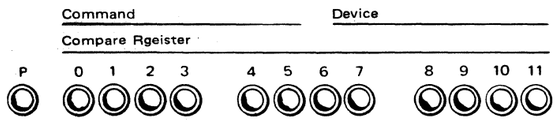
With ALU2 selected, displays TU Bus Out data in 0 through 7 and outbound controls or tags in 8 through 11.

Hi ROS

With ALU1 selected, displays ROS1 data bits 0-7 P1 in 0 through 7 and control lines in 9 through 11.

With ALU2 selected, displays ROS2 data bits 0-7 P1 in 0 through 7 only.

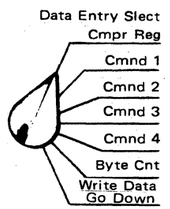
Low ROS



With ALU1 selected, displays ROS1 data bits 8-15 P2 in 0 through 7 and control lines in 9 through 11.

With ALU2 selected, displays ROS2 data bits 8-15 P2 in 0 through 7 only.

DATA ENTRY SELECT (SEVEN-POSITION ROTARY)



Cmpr Reg

Allows data in the three Data Entry switches to be entered in the compare register.

Cmnd 1, 2, 3, and 4

With the Data Entry Select switch in one of the four positions (Cmnd 1, 2, 3, or 4), a command and its associated device address (0-F) may be entered into one of the four command positions.

Byte Cnt

The three Data Entry switch positions determine the total byte count. The left and center switches count to a maximum of 256. The right, or Multiplier switch counts in multiples of 1024. Position zero of the Multiplier switch adds zero to the total of the other two switches. Position 1 would add 1024, 2 would add 2048, etc. To provide a byte count of 3140, set the left and center switches each to 4, and set the right switch to 3.

Note: Check to ensure you get the correct byte count.

Byte Count Dialed	Byte Count Written
00 to FE	Byte Count dialed +3
FF	2

Write Data Go Down

Write Data and Go Down determine those bits to be written and establishes the go-down time. The left and center data entry switches determine the bits to be written. For example, the Ripple/Wr Data switch in Wr Data, 8 in the left switch, and 3 in the center switch writes the following:

0 1 2 3 4 5 6 7
1 0 0 0 0 0 1 1

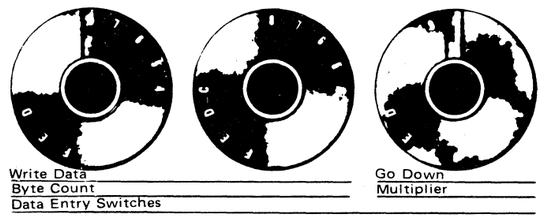
Note: The P bit is automatically generated when required.

The right switch determines the go-down time. Position zero gives a go-down of 6.0 milliseconds. The total range is from 6.0 milliseconds to approximately 0.5 second. Each position, 0 to F, represents approximately 26 milliseconds. A setting of 3 results in a go-down time of 6 milliseconds + (3 x 26), or approximately 84 milliseconds.

- To write continuously, jumper from AA1R2J12 to ground.
- To do an LWR with go-down time, jumper from AA1S2G08 to ground.

Data Entry

The three rotary switches are used to enter data into various registers. Set a command into the left switch and the TU address into the right switch. For example, 01A entered into the Command register indicates a write command to device A.



CE PANEL INDICATORS

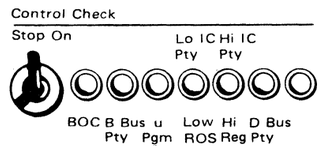
INTF'S DISABLED

Indicates when the tape control is offline. The manual Enable/Disable switch(es) on the CU operator's panel must be in Disabled position before the lamp comes on.

CMPR EQUAL

Indicates that the data entered in the CE/Compare register equals that contained in any register selected for comparison.

CONTROL CHECK INDICATORS



BOC

Checks the 16 branch conditions not checked by the HI IC PARITY/HI ROS register circuits. (A total of 32 BOCs are checked.) If an even number of BOC groups are active, a BOC error is indicated.

B-Bus Parity

Checks the output of an LSR for odd parity on the B Bus on instructions which transfer data from ALU to an external register. If parity is even, the error is gated to the hardware error latches and CE panel indicator.

Note: When displaying the LSRs, B-Bus parity errors can occur because LSRs are not set to odd parity with power-on reset.

Hi IC Pty/Hi ROS Reg Pty

The circuits that set this indicator are:

1. Hi IC parity check.
2. Hi ROS register parity check.
3. Instruction Decode error. (ROS instruction check to be sure only one ROS operation was decoded.)
4. BOC Error. (Check of 16 branch conditions.)

Lo IC Pty/Low ROS Reg Pty

Checks parity of the IC (low order) and ROS register (low order). An even parity error sets the HARDWARE ERROR latch and CE panel indicator. Lo IC Parity is checked only on a BU or a successful BOC. Low ROS Parity is checked on every instruction cycle.

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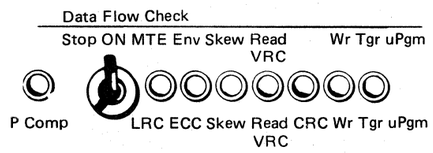
D Bus Pty

Checks the parity of information to be stored in an LSR at 100 ns time. Bits 0-8 from the D Bus are exclusive-ORed with the P bit from Bus Out. Even parity sets the D BUS PARITY ERROR latch and HARDWARE ERROR 5 latch, and lights the CE panel indicator. This error condition is only checked on a transfer of data into the ALU from an external source.

U Pgm

Monitors the selected ALU and signals an error when the ALU detects any hardware error, including checkout errors for both ALUs.

Data Flow Check Indicators



P Comp

The P Comp indicator (also C Compare) is set by the following conditions:

1. When parity of the byte sent to the channel buffer on read operations is wrong.
2. Buffer Overrun.
3. Write Address error.
4. If CHANNEL BUFFER READ IN counter gets out of step.
5. Write buffers are empty when a write tape cycle occurs.
6. Parity does not match between the channel buffer and the write buffer outputs on write operations.
7. When operating in 7-track data convert mode and a count of bits before and after conversion does not match.
8. When operating in 7-track mode with the Data Converter off and the count of bits for each byte as it enters and leaves the register fails to compare.

MTE/LRC

1. Set during a 6250 bpi write operation when there are two or more error pointers:
2. Set during a PE operation when there are two or more error pointers.
3. Set during a NRZI operation when a block has an odd number of bits in any track (LRC).

ENV/ECC

1. Set when any track signal falls below threshold on read or write. Does not set Data Check.
2. Set during a PE operation when any error pointer is set or when any track falls below threshold. Sets Data Check on write only.
3. Set during a NRZI write operation if NRZI Register 2 has incorrect parity.

Skew

Set when vertical misalignment of bits exceeds acceptable limits. (If all bits in a byte are not received by the read circuits within a specified period, the bit has excessive "skew" and Skew Error is set.)

1. During a 6250 bpi/PE read operation if RIC leads ROC by 30 bits.
2. During a 6250 bpi write operation if RIC leads ROC by 14 bits.
3. During a PE write operation if RIC leads ROC by 4 bits.
4. During a NRZI write operation by skew gate.

Read VRC

1. 6250 bpi Mode
   a. Set during single-track error correction if a match is not found.
   b. Set during a write operation if hardware pointer and correction code indicate different tracks.
2. Set during a PE operation if a parity error occurs and no track pointers are on.

CRC

Set during 6250 bpi and 9-track NRZI operations when the CRC byte calculated for a read operation does not match the CRC byte written on tape.

Wr Tgr

Set when the output of the write triggers has incorrect parity.

U Pgm

Set when ALU2 detects any microprogram error, including End Data Check on PE operations, and any error indicated in sense byte 8, bits 0-6; sense byte 9, bit 1; and sense byte 10, bits 0-7.

NOTES ON CE PANEL OPERATION

- A Start I/O command to a tape unit that has Unit Check or Busy in its initial status byte will prevent stepping to the next command. This condition can be caused by a Not Ready tape unit.
- CE command sequence hang up: when an error occurs on a 3803 with the Two-Channel Switch (TCS) feature installed, a "contingent connection" is established without Stop On Error ON. This is caused by dedicated sense data from the failing tape unit. There are three ways to proceed:
  1. Issue a Sense command to the same tape unit after any other type of command.
  2. Issue all four internal program commands, except a Test I/O or NOP, to the same tape unit. A Mode Set command can also cause a hang condition, so it may be necessary to replace this command following initial setup.
  3. In order to allow command cycling to multiple tape units without changing the command setup, set ROS Mode to Rst/Cmpr using IC address 302 on ALU1. This restarts both microcodes at 000 on contingent-connection conditions and performs a general reset. To eliminate the need for pressing the CE Command Start pushbutton, connect a jumper from AB2Q2S10 (General Reset FC041) to AA1T2G05 (Start Key Latch PK035).

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TOOLS AND TEST EQUIPMENT

The tools and test equipment listed in this section are required to properly service 3420 Magnetic Tape Units and 3803 Tape Controls.

KEPT AT THE BRANCH OFFICE	
Part	**Name**
1848621	Stress Tape (order from Mechanicsburg)
432152	Master Signal-Level Tape (order through IRD Sales) (See Note 1.)
451064	Degausser (See Note 1.)
453522	Developing Solution
453585	*Digitec 251 Meter (Digitec 201 Meter, P/N 453046, may be used if available)
460874	Scale, 0 to 6 pounds (belt adjustment)
2515376	Capstan Prealignment Gauge
2515390	Capstan Adjustment Wrench (rear adjustments)
2515401	Reel Motor and Hub Adjustment Tools: (see 08-460)
2523723	Capstan Adjustment Wrench (front adjustments)
5861448	7-Track NRZI Threshold Adjustment Card
5861455	PE Threshold Adjustment Card
5861452	Dual Density Threshold Adjustment Card
* Trademark of United Systems Corporation	

KEPT AT THE CUSTOMER'S ACCOUNT	
Part	**Name**
453511	Tape Transport Cleaner Scratch tape Oscilloscope (Model 453, 454, 561, 545, 766H or equivalent)
352465	Tape Cleaning Kit
432641	Master Skew Tape (See Note 1.)
453500	Manometer, 30 inch (two needed for series connection) (See Notes 1 and 2.)
453504	Tee and Hose Assembly (See Note 2.)
453522	Tape Developing Solution
1765342	Tape Unit Tester
1846251	Shim, Right Reel Hub Alignment
1846252	Hex Wrench, Right Reel Hub
2512745	Adapter Hose (See Note 2.)
2513154	Pressure Divider (See Note 2.)
2501611	Tape Unit Cleaning Brush
2512063	Crimper (supplied by marketing representative)
2515390	Capstan Box Wrench (read adjustment capstan only)
1848621	6250 bpi Stress Tape

Notes:

1. *Discussed in more detail in this section.*
2. *Not needed if pressure/vacuum gauge P/N 5495384 is* available.

MASTER TAPES

Master skew tapes and master signal-level tapes are manufactured to rigid specifications. They are the standards that are used by CEs to obtain optimum tape unit performance.

Because tape unit performance is directly affected by the accuracy of these master tapes, the following precautions should be taken:

1. Use master tapes only for their intended purpose.
2. Handle tapes with care.
3. Make only full-reel passes in order to have even wear throughout the length of the tape.
4. Identify master tapes as such and mark the reels with the letter "m," as a reminder to make full passes only.

MASTER SKEW TAPES

Master skew tapes have a density of 800 FCI and are written with one solid bit across the width of the tape. These tapes are written on a specially adapted tape unit at the Tape Test Center with accuracy held to within 0.375 usec total skew between the leading and lagging bits of a 112 ips tape unit.

The master skew tape will run off the reel when reading forward because it is written with no interblock gaps (IBGs). In order to create an IBG and save time during skew adjustments, make the following alterations to the master skew tape:

1. Read the master skew tape forward to the end of tape EOT reflective marker.
2. Install a write enable ring.
3. Write one record of any size beyond the EOT marker.
4. Remove the write enable ring.
5. Rewind the tape.

After the preceding one-time preparatory steps, set the tape control CE panel as follows when you use the skew tape:

1. Command 1-Read Forward ('02')
2. Command 2-Read Backward ('0C')
3. Command 3-Read Forward ('02')
4. Command 4-Read Backward ('0C')

The master skew tape will read forward to the end of the reel, read backward, and repeat the cycle. This permits checking skew from the rear of the tape unit without manipulating the controls.

MASTER SIGNAL-LEVEL TAPES

Master signal-level tapes have the ability to produce a signal to within ±2% of the primary master. (A primary master, which is established as an IBM standard, is the base for instrument alignment.)

All new master signal-level tapes are checked at 3200 FCI and 800 FCI. The suffix letter "A" is added to the part number to allow field identification of 3200/800/556 FCI tapes as opposed to the former 800/556 FCI tapes. Thus, for example, a master signal-level tape checked out at both 3200 FCI and 800 FCI would have P/N 432152A.

DEGAUSSER

Caution: The degausser will demagnitize any material such as tape, disks, etc. Power off the tape unit.

To degauss the read/write head:

1. Remove magnetic tape from the tape unit. Do not place the tape on top of the tape unit.
2. Plug degausser into 110 Vac receptacle.
3. Press the pushbutton on the degausser while it is at least 1 foot (30,5 cm) away from the read/write head and move it slowly toward the head.
4. Hold the degausser against the front surface of the head for about 10 seconds.
5. Pull the degausser straight away from the head very slowly to a distance of at least 1 foot (30,5 cm) and release the pushbutton.

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WATER MANOMETER

Note: *The use of a 30 inch (76,20 cm) manometer or the 80 inch (203,20 cm) pressure/vacuum gauge is not dependent on the English (metric) system of measurement.*

Use the requested tool by part number and name, and measure to the specified units (whether metric or English) to obtain the desired adjustment or reading.

Shown are several setups for using the water manometer, part number 453500. Part A shows a single manometer measuring a pressure of less than 30 inches (76,20 cm). Part B shows two manometers in series measuring a pressure between 30 and 60 inches (76,20 cm and 152,90 cm). Part C shows using the pressure divider and a single manometer measuring a pressure greater than 30 inches (76,20 cm).

General instructions for using the manometer are:

1. Remove the tee from the tee and hose assembly, and connect the hose on the line to be checked.
2. Set up the water manometer by opening both top valves one full turn from closed position. (Incorrect readings will occur if valves are opened too far.) Connect the pressure-sensing hose to one port, leaving the other port open.
3. Fill the water manometer with tap water, maintaining the water level near the 0 position on the scale. Zero the manometer by sliding the scale up or down until the 0 mark lines up within 0.2 inch (5,7 mm) of the bottom of the meniscus in both columns.
4. Set conditions for the specific item to be checked according to the pneumatic-adjustment decal located on the transfer valve and manifold.
5. Read the vacuum level. (The vacuum level is the sum of the displacement of the water level in each column.)

PROCEDURES

Note: *Take readings at bottom of meniscus.*

1 Using a single manometer to measure a pressure of less than 30 inches (76,20 cm). Read at bottom of each meniscus and add the two readings together to get total pressure (W). W = 2.0 + 1.7 = 3.7.

2 Using two manometers in series to measure a pressure between 30 and 60 inches (76,30 and 152,40 cm). Read at bottom of each meniscus and add the four readings together to get total pressure (the sum of X + Y). X + Y = 2.0 + 1.7 + 2.0 + 1.7 = 7.4 inches.

3 Using a pressure divider with a single manometer to measure a pressure of greater than 30 inches (76,30). First, measure a known pressure of less than 30 inches. Second, insert the divider and adjust the divider's adjusting screw until the manometer reading is 40% of its original reading. Third, measure the pressure of greater than 30 inches by reading at the bottom of each meniscus, adding the two readings together (to get Z), and multiplying Z by 2.5 to get pressure. 2.5Z = 2.5(2.0 + 1.7) = 2.5(3.7) = 9.25 inches. The maximum reading possible with this combination is 75 inches (190,50 cm).

4 Using a pressure/vacuum gauge to measure a pressure greater than 80 inches (203,20 cm).

a. Measure a known pressure less than 80 inches (203,20 cm).

b. Insert the pressure divider between the measurement part and the gauge and adjust the divider's adjusting screw until the gauge reads 40% of its original reading.

c. Measure the pressure greater than 80 inches (203,20 cm) and record the reading (Z).

d. Multiply Z by 2.5 to get the total pressure.

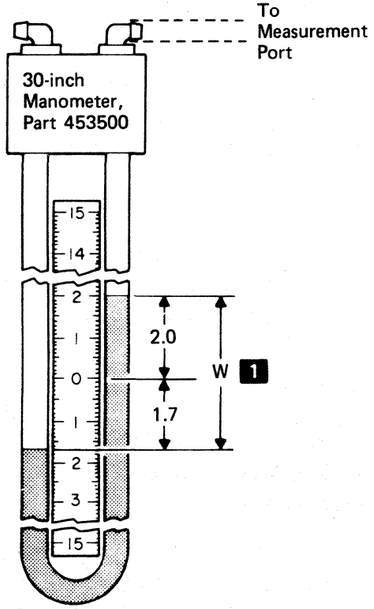
Example: If Z reading is 33.2, 33.2 x 2.5 = 83.0 inches

PRESSURE/VACUUM GAUGE

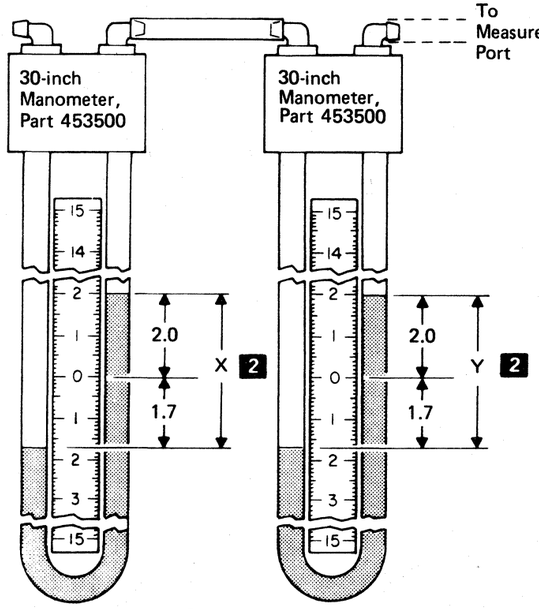
Shown below is pressure/vacuum gauge, part 5495384. To use the gauge:

1. Attach the gauge hose to the fitting to be tested.
2. Read the dial directly in pressure or vacuum. (For measurements above 80 inches (203,20 cm), add 1 inch (2,54 cm)to the reading for each 1/16 inch (1,59 mm) of pointer travel beyond the end of the scale.)

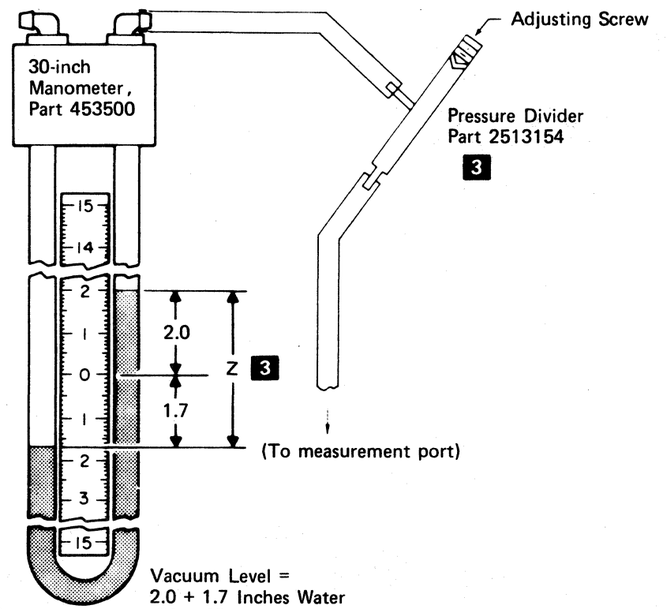
Caution: Disconnect from test point before loading or unloading tape unit to prevent damage or miscalibration of gauge.



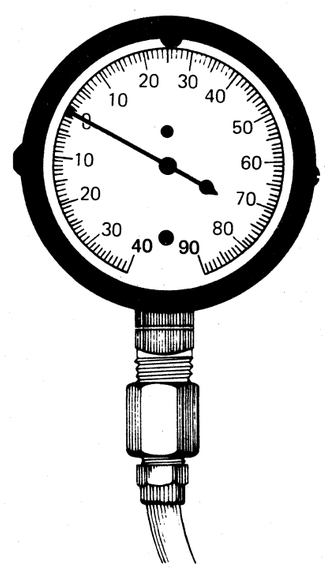
Part A



Part B



Part C



4 Pressure/Vacuum Gauge Part 5495384

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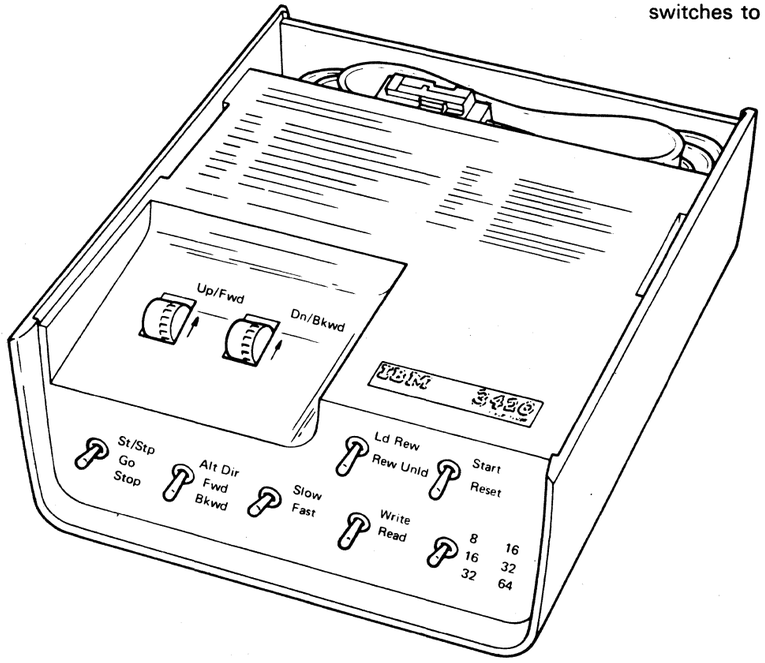
80-010

3420 FIELD TESTER

Caution: Use extreme care when attaching the field tester because an error can damage the tape unit, the tester, or both. Be sure to use only the 3420 field tester, part 1765342, when doing offline maintenance on 3420 tape units. Do not use the 2420 Field Tester. When testing Models 4, 6, and 8, a field tester at EC level 734316 must be used. A temporary jumper must be installed from K2P02 to M2D06 for 6250 operation.

When operated with the field tester, the tape unit loads and unloads tape, reads, writes, and moves tape forward or backward.

To test several tape units simultaneously, use the manual controls on the tape control CE panel.



To use the field tester:

1. Unload the tape unit.
2. Switch the unit off line at the logic gate. To ensure that the on-off line switch circuitry is operating correctly, monitor the - interface disable and + int dis or - off lines. Refer to page FT910 of the 3420 ALDS. Check the following levels for proper operation of the on-off line switch circuits.

Position of On-Offline SW	A1L6D04	A1L6B03
Online	+6v	-4v
Offline	Gnd	Gnd

3. With the arrow on the cable pointing up, plug the tester into the wiring side of the logic gate at location A1N5. Another way to be sure the cable is plugged correctly is to make sure the notches on the cable connector are toward the center of the logic gate. Select, on the tape unit operator's panel, comes on when the Read/Write switch is in the READ position, or in the WRITE position with the MOVE tag active. You can now use the tester switches to load and Ready the tape unit.

Caution: The field tester can cause tape dump and damage under the following conditions:

1. When moving tape with field tester, the direction switch position is changed before activating "Stop".
2. When attached to a tape unit and set to "Fwd" and either "St/Stop" or "Go", the tape unit is loaded and goes to Load Point and becomes Ready. If RESET on the tape unit console is activated and the tape unit does not dump tape, and then Reset is followed by activating UNLOAD, the tape will run off the end of the reel.
3. When using "Alt Dir", RESET is activated on the tape unit.

Conditions 1, 2, and 3 above can be eliminated by always putting the tester in "Stop" before doing any other operation.

The switches on the tester operate the tape unit by remote control as follows:

Start/Reset

Operates the same as the control on the tape unit operator's panel. Start makes the unit ready. Reset resets the unit.

Ld Rew/Rew Unld

Ld Rew loads tape if none is loaded, and rewinds tape to load point if tape was loaded but is not at load point. Rew Unld rewinds tape from any position, unloads the unit, closes the cartridge if one is used, and lowers the power window.

Up/Fwd

Up/Fwd controls either the time the MOVE line is active during a start/stop operation, or the duration of forward motion in an alternate-direction operation.

Dn/Bkwd

Dn/Bkwd controls either the time the MOVE line is inactive during a start/stop operation, or the duration of backward motion in an alternate-direction operation.

St/Stp/Go/Stop

St/Stp causes interruptions in tape motion. Use the Up/Fwd control and Slow/Fast switch to adjust go-up time. Use the Dn/Bkwd control and Slow/Fast switch to adjust go-down time. Go ensures continuous tape movement. Use the Alt Dir/Fwd/Bkwd switch to control direction. Stp halts tape motion.

Alt Dir/Fwd/Bkwd

St/Stp/Go/Stop switch must be at Go to enable this switch. Alt Dir is active in read status only; it moves tape alternately forward and backward. Use Up/Fwd control and Slow/Fast switch to adjust duration of forward movement. Use Dn/Bkwd control and Slow/Fast switch to adjust duration of backward movement. Fwd causes forward tape motion. Bkwd causes backward tape motion.

Slow/Fast

This is a range switch for the Up/Fwd and Dn/Bkwd controls. Slow extends the go-up/down timing range to approximately 3.0 seconds. Fast decreases the go-up/down timing range to approximately 7.0 ms.

Write/Read

Write causes the tape unit to write with gaps. Each time the tape unit writes, as in a start/stop operation, it generates a PE gap of 0.528 inch (13,4 mm) and a GCR gap of 0.275 inch (7,0 mm). Read causes continuous reading.

8/16/32 (Models 3, 5, 7) See Note

This switch controls the frequency of the tester's write oscillator. The three positions result in write frequencies of 800 fci (NRZI), and 1600 and 3200 fci (PE), respectively.

16/32/64 (Model 4, 6, 8) See Note

When a field tester at EC level 734316 is used on 3420 Models 4, 6, and 8 with the provided jumper installed, these switch positions represent 1600, 3200, and 6400 fci as the label shows. Frequencies generated by the tester are for practical offline test only. Do not confuse these tester frequencies with normal online recording densities.

Note: *The back panel wiring on cable position A1N5 on Models 4, 6, and 8 is such that the frequency of the tester is doubled.*

XH0400 Seq 1 of 2	2736016 Part Number	See EC History	845958 1 Sep 79	846627A 3 Dec 80	847298 15 Aug 83			

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NOTES:

3803-2/3420

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GENERAL CLEANING INSTRUCTIONS

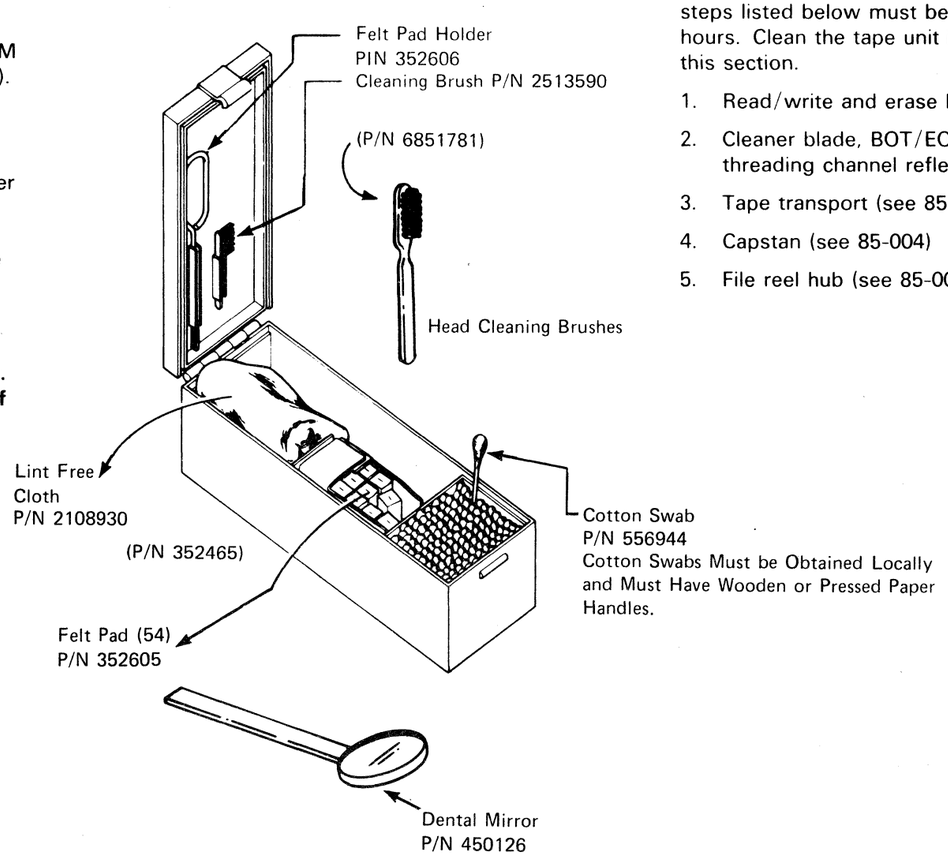
This procedure makes all previous 3420 tape unit cleaning procedures obsolete.

Items used by this procedure are contained in the IBM Tape Cleaning Kit, part number 352465 (see Figure 1).

Use IBM tape transport cleaner, part 8493001. Performance results cannot be guaranteed when other chemical formulations are used. Other chemical formulations have not been tested by IBM, and their use may impair performance or cause damage to the tape unit or tape.

DANGER
When using tape cleaner, do not get it on skin or clothing. Follow the instructions on the container. Do not use metal instruments to clean any part of the tape unit.

Figure 1. IBM Tape Cleaning Kit



DAILY CLEANING PROCEDURE

To promote reliable tape unit performance, all of the steps listed below must be performed every eight hours. Clean the tape unit in the sequence presented in this section.

1. Read/write and erase heads (see 85-001)
2. Cleaner blade, BOT/EOT block, rewind plunger, and threading channel reflector (see 85-002)
3. Tape transport (see 85-003)
4. Capstan (see 85-004)
5. File reel hub (see 85-004)

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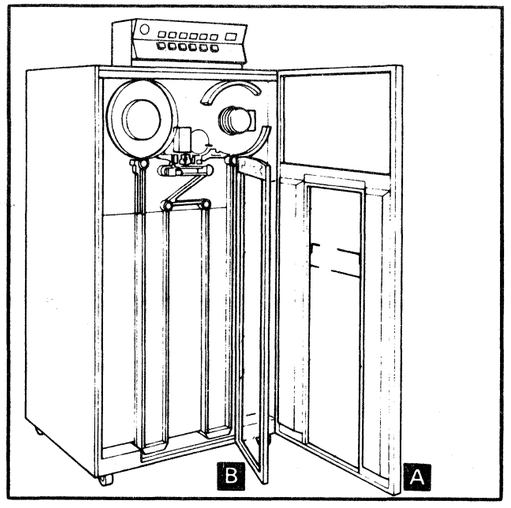
TAPE UNIT CLEANING PROCEDURE FOR 3420 MODELS 3 THROUGH 8

1. R/W AND ERASE HEADS

1.1 Unload tape and remove from tape unit.

1.2 Open outer (A) and inner (B) doors.

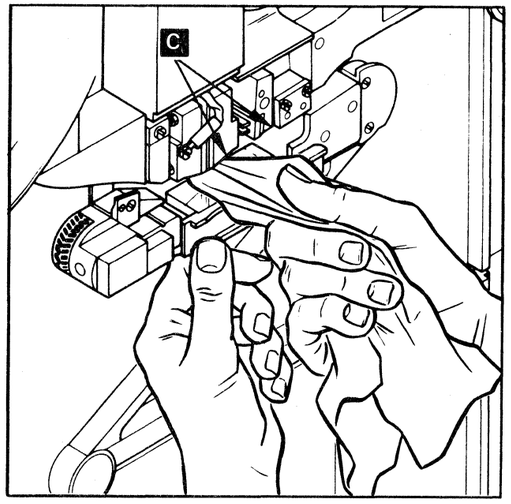


1.3 Dampen clean area of lint-free cloth with tape cleaner.

1.4 When cleaning Models 3, 5, and 7, hold the inspection mirror down, use dampened cloth to clean the R/W and erase heads (C) using a circular motion.

1.5 When cleaning Models 4, 6, and 8, hold autocleaner in and clean the R/W and erase heads (C) with a dampened cloth using a circular motion. To reach the inside tracks, wrap the dampened cloth around a cotton swab.

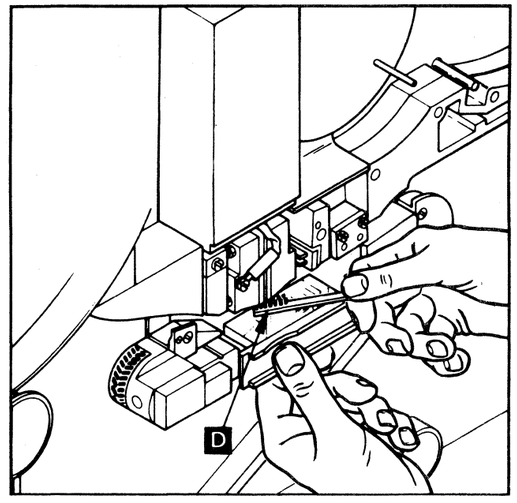
1.6 Repeat steps 1.3 and 1.4 or 1.5 until cloth remains clean.



1.7 Use inspection mirror for Models 3, 5, and 7 or dental mirror for Models 4, 6, and 8, to carefully inspect heads. (Clean mirror with dry cloth, if dirty.) If heads do not look clean, perform step 1.8, otherwise wipe heads with dry clean cloth and go to step 2.

To remove stubborn residue from heads—

1.8 Use either style head cleaning brush dampened with tape cleaner to remove residue (D) and then return to step 1.3.



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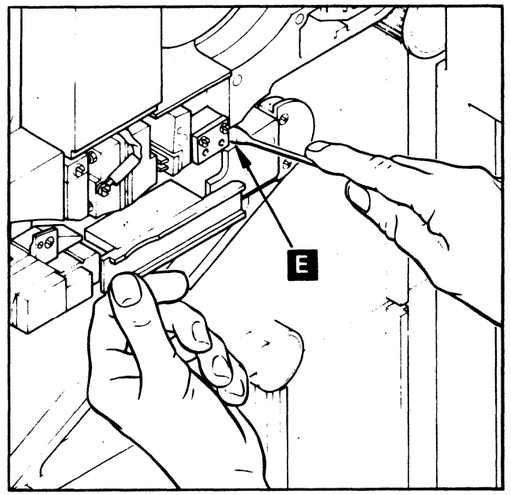
TAPE UNIT CLEANING PROCEDURE FOR 3420 MODELS 3 THROUGH 8

2. CLEANER BLADE, BOT/EOT BLOCK, REWIND PLUNGER, AND THREADING CHANNEL REFLECTOR

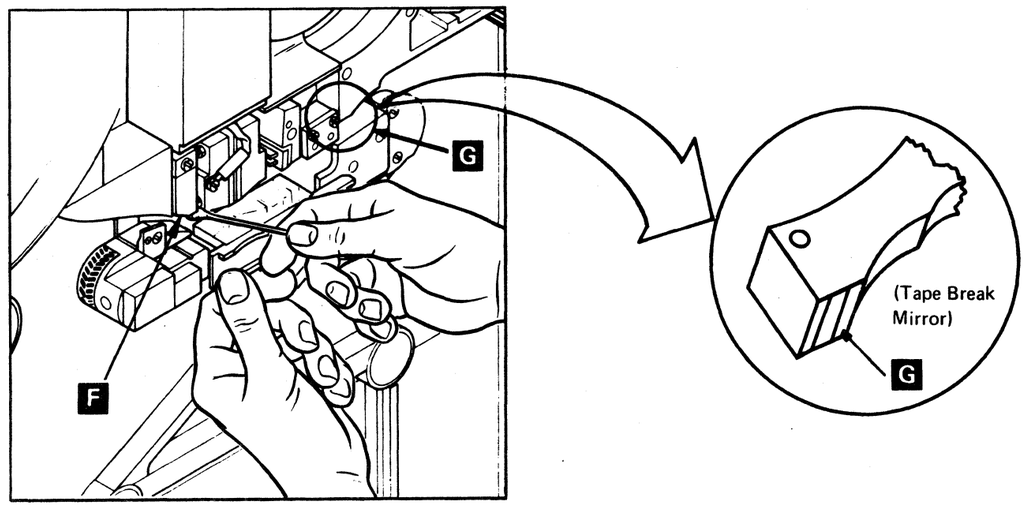
2.1 Hold the inspection mirror down, or the autocleaner in, when cleaning. Use a cotton swab dampened with tape cleaner to clean the following items.

2.1.1 BOT/EOT block Ⓔ

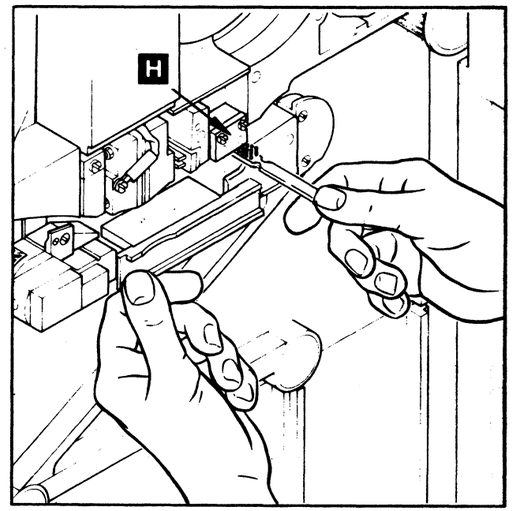


2.1.2 Rewind plunger/filler block Ⓕ

2.1.3 Threading channel reflector Ⓖ



2.2 Use the head cleaning brush (P/N 6851781) dampened with tape cleaner to clean the cleaner block Ⓗ. Wipe with cloth.



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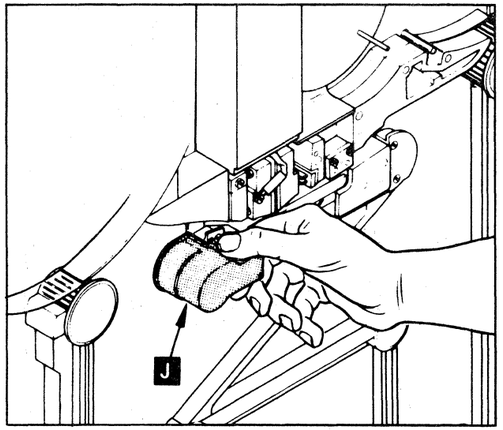
TAPE UNIT CLEANING PROCEDURE FOR 3240 MODELS 3 THROUGH 8

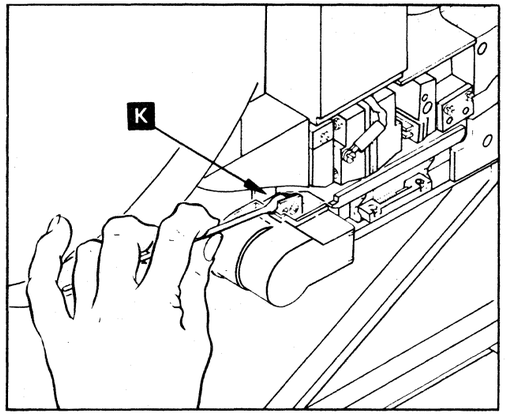
3. TAPE TRANSPORT

3.1 Install capstan cover (J).

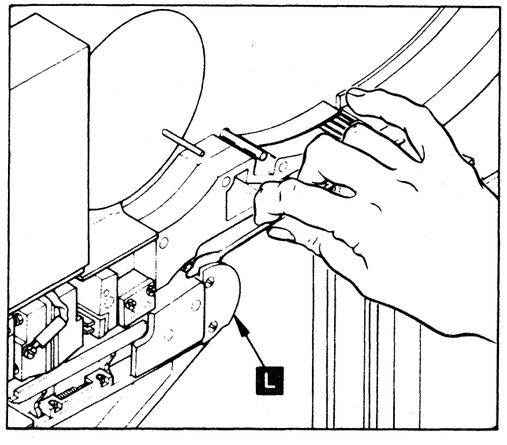


3.2 Dampen cotton swab with tape cleaner and clean the following:

3.2.1 Front and back guides (K).



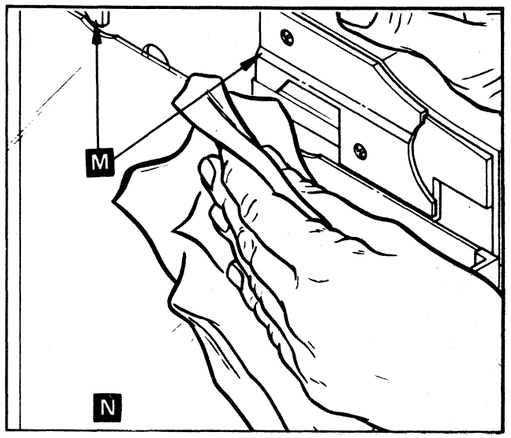
3.2.2 D-bearing (L).



3.3 Use a lint-free cloth dampened with tape cleaner to clean the following:

3.3.1 Threading plates (M).

3.3.2 Back of inner door (N).



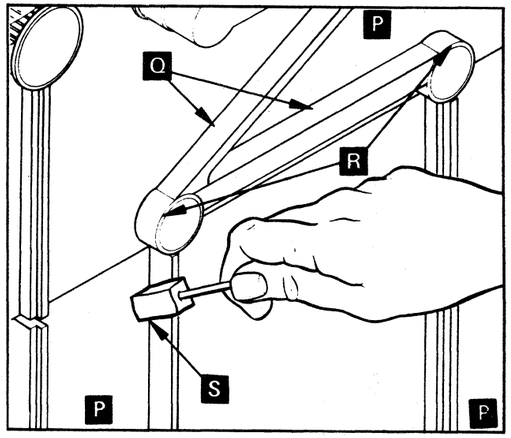
3.3.3 Back wall (P) and sides (Q) of vacuum columns

3.3.4 Air bearings (R). **Note:** If residue remains in vacuum column corners, perform steps 3.3.5 and 3.3.6, otherwise go to step 3.4.

To remove stubborn residue in corners of vacuum columns—

3.3.5 Put clean felt pad on handle making sure the handle does not go through the end of pad.

3.3.6 Dampen felt pad with tape cleaner and clean vacuum column corners as shown (S). Make sure no contact is made with capstan cover and/or capstan.

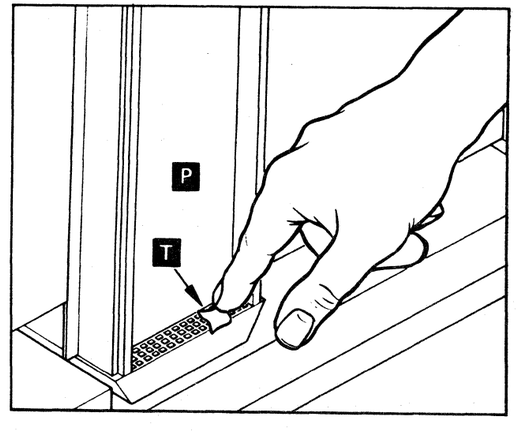


Caution: You may need to use water to remove residue left in the vacuum columns by some tapes. Do not get water on any other part of the machine. Water will damage the capstan.

3.3.7 Use a lint-free cloth dampened with tape cleaner to remove any residue left by the felt pad.

3.4 Check bottom of vacuum columns (T) for bits of tape and remove if present.

3.5 Remove capstan cover and replace in storage area.



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TAPE UNIT CLEANING PROCEDURE FOR 3420 MODELS 3 THROUGH 8

4. CAPSTAN CLEANING—NORMAL PROCEDURE

This procedure must be done at regular intervals by the customer. Tape will slip on a dirty capstan while accelerating.

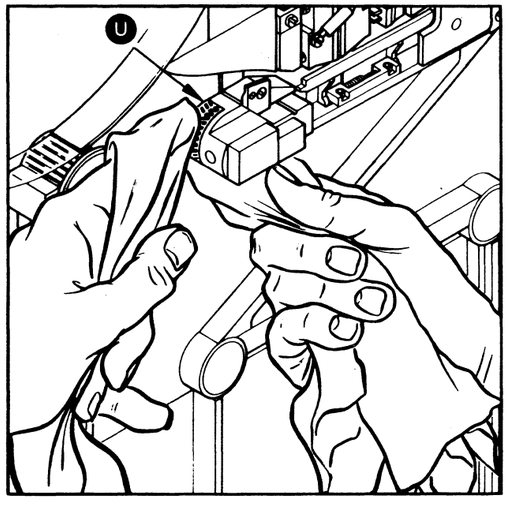
Caution: Any capstans not kept free of glaze will eventually build a deposit that cannot be removed by a reasonable amount of scrubbing.

4.1 Wrap a clean, dry cloth around one index finger and a lint-free cloth dampened with tape cleaner around the other index finger.

4.2 Vigorously wipe the capstan rubber with the dampened cloth (without bending the capstan) while rotating the capstan with the dry-cloth-covered finger (U).

4.3 Continue this procedure until the capstan has a definite dull rubber finish. Any glaze must be removed in order to operate reliably.

4.4 If the glaze cannot be removed, follow the special Glazed Capstan Cleaning procedure on page 08-700.



5. FILE REEL HUB

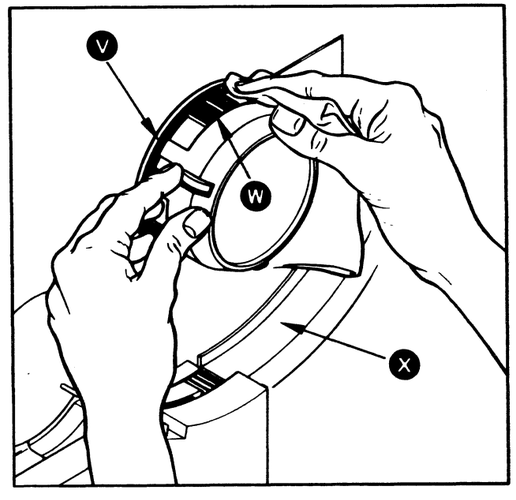
5.1 With a lint-free cloth dampened with tape cleaner, use a light pressure to clean the following:

5.1.1 Back rubber flange (V).

5.1.2 Rubber ring (W) or rubber pads on some models.

6. CARTRIDGE RESTRAINT

6.1 Use a lint free cloth to clean lower restraint (X). This metal is porous and the air flow can be restricted by using fluids or abrasive material during cleaning.



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3803/3420 PREVENTIVE MAINTENANCE SCHEDULE

3420 Tape Unit

Code U	Code R	Location Operation	Frequency	Action
0		Door Slide and Stop Pin	4 months	Lubricate the door slide and the stop pin with IBM #17.
		General Cleaning	4 months	1. Clean front deck and base. 2. Remove tape cleaner block and clean with tape cleaner. 3. Remove air bearing (D bearing) next to EOT/BOT block and clean. Inspect guide behind bearing and replace if grooved. 4. Clean NRZI guides. 5. Clean EOT/BOT channel mirror. 6. Clean the fiber optic lamp. Use a tissue lightly moistened with water. **Caution: Allow lamp to cool before cleaning.** Remove the manifold and fiber bundles to provide access to the lamp. Replace the lamp (08-620) if it is not clear. **Note:** Cleaning or replacement of the fiber optic lamp may require the readjustment of the EOT/BOT and capstan squaring.
		Capstan Tach Squaring Circuit	4 months	Check and adjust Capstan Squaring. See 08-120 or 08-130. Ensure capstan is free from dents and does not bind.
		Capstan Tracking	4 months	Check and adjust Capstan Tracking. See 08-000.
		EOT/BOT	4 months	Check and adjust EOT/BOT. See 08-580.
		File Protect Pin	4 months	1. Push plunger in, check for binds. 2. Check that plunger extends in front of the right hub flange. 3. Replace unit if any checks produce unsatisfactory results.
		Power Window Safety Bail	4 months	Check for the correct operation of the power window safety bail. If incorrect, tighten the setscrew in the safety bail terminator, and adjust the safety bail switch assembly (see 08-000).
2		Parts Replacement	12 months	Order one of the following B/Ms for required parts. B/M 8492273 Puralator type filter B/M 8492274 Cuno type filter
		Tape Cleaner Block	12 months	Replace the tape cleaner block. Supplied with parts replacement B/M.
		Pneumatic Supply	12 months	Check pneumatic supply belts.
		Input Filter	12 months	Replace filter element of the pressure pump input filter. Supplied with parts replacement B/M. Check for Puralator or Cuno type.
		Cooling Filter	12 months	Clean cooling air filter or replace as necessary.
		Air Bearing Cleaning	12 months	1. Remove bearings. 2. Brush each bearing to remove oxide deposits. 3. Install new decorative covers on air bearing. Supplied with parts replacement B/M.
		Vacuum Column Door Foam	12 months	Inspect foam in front of vacuum door glass. See 08-690. If foam replacement is required, order B/M 4469244
		DC Voltage	12 months	Check the dc voltages. (08-570)
		EOT/BOT	12 months	Remove EOT/BOT by removing the two screws and gently move block forward being careful not to damage the fiber bundles if present. Clean EOT/BOT with a cotton swab dampened with tape cleaner. Replace EOT/BOT block.
		Capstan Motor Mod-8	12 months	Clean screens on back of motor with vacuum cleaner.
		Radius Sense	12 months	Clean the ends of the fiber optic bundle if present with a damp cloth, see 08-610 for removal. Apply a felt pad to the handle and lightly dampen with tape cleaning fluid. Hold pad to the inside front of left reel flange and spin by hand. This will clean the reflective strips located inside the left reel.
		Reel Tach	12 months	Check reel tachs for glaze. Replace reel tachs if glazed.
		Glass Bead Tape	12 months	Inspect glass bead tape on stubby bar and in vacuum columns. See note. Ensure that stubby bars are not loose and have proper clearance. See 08-000.
		High Speed Rewind Plunger	12 months	Check operation of the High Speed Rewind Plunger. (08-000) Models 3, 5, and 7 only.
		Autocleaner Check	12 months	1. Check operation of autocleaner by marking the ribbon and observing ribbon movement. The ribbon should move from bottom to top. 2. Check the supply of autocleaner ribbon. Order a new autocleaner cartridge when approximately 3/4 inches of ribbon is visible through the cartridge window. Models 4, 6, and 8 only.
		Preamps	12 months	Check and adjust preamps (08-290 or 08-300).
3		Output Filter	36 months	Replace with P/N 2524998.
4		Vacuum Tubing	60 months	Replace vacuum tubing (order B/M 4416409).
		Pressure Tubing	60 months	Replace pnuematic pressure tubing (order B/M 4416408).
		Vacuum Pressure Switches	60 months	Right switch plate - with seven holes - B/M 6851766 - with five holes, one switch top, three grouped center, one at bottom - B/M 6851768 two switches top, three at bottom - B/M 6851764 Left switch plate - with five holes, three switches top, two at bottom - B/M 6851765 -all other configurations - B/M 6851767 Tape transport switches Model 3,5,7 - B/M 6851770 Model 4,6,7 - B/M 6851771

Note:

Inspect the glass bead surface of the stubby bars and vacuum columns.

Replace if the glass bead is nicked, scratched, burred or has an area obviously worn to the touch. (If not obviously worn, do not replace).

Run finger on the glass bead surface at the bottom of the vacuum column. This is a good glass bead surface and may be used as a reference.

A worn glass bead surface will cause tape motion problems.

3803 Control Unit

Code U	Code R	Location Operation	Frequency	Action
0		Air Filter	2 months	Check cooling air filter for restriction of air flow. Clean or replace as required.
2		dc Voltage	6 months	Check dc voltages. Adjust as required to the levels specified on decals.

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SUBSYSTEM INSTALLATION

INTRODUCTION

This section contains installation instructions for the IBM 3803 Model 2/3420 Magnetic Tape Subsystem. Companion publications pertaining to this product are:

1. *3803 Model 2/3420 Subsystem Description,* GA32-0021
2. *3420 Model 4, 6 and 8 Parts Catalog,* S132-0007
3. *3803 Models 1 and 2 Parts Catalog,* S132-0004
4. *3420 Operator's Guide Card,* S232-0003
5. *3803/3420 OLT Users Guide*

Safety Note: Ensure your own safety by using caution at all times and by being aware of potentially dangerous areas of the machine. Read and follow the safety suggestions in Form 229-1264, a pocket-sized card issued to all customer engineers and reprinted at the front of this manual.

Caution: No portion of this procedure is to be omitted. Perform all steps including checks and adjustments.

INSTRUCTIONS

Perform the following basic steps for *each* 3803 Model 2/3420 installation, regardless of the subsystem configuration:

1. Refer to the checklist on 90-020 and initial each box when an installation procedure is completed.
2. Complete the configuration worksheet on 90-040. Refer to the instructions on 90-030.
3. Unpack units. (See Unpacking Instructions on this page.)

Note: Before moving 3420 tape units into place, be sure to remove packing tape from the air flow mercury switch and install the front kickplate. Check ESD grounding. See 90-190, F7 and F8 before moving machines into place.

4. Remove the wire seal from the 3803 and 3420's, 90-180, only at this time.
5. Install four caster locks.
6. Install front and both side kickplates. See 90-090.
7. Install rear kickplate. See 90-090.
8. Install and plug cables. See 90-050 through 90-080.

Note: The tag and bus cable pairs must be of equal length. Paired cables of unequal length cause timing errors resulting in hard-to-diagnose subsystem problems.

9. Plug address/feature/priority card jumpers to match configuration requirements, see 90-110.

Note: Check the factory-installed items such as card jumpering, and all card and cable seating. Particularly check the write head and read head card seating.

10. Rework the 3420 Field Tester, see 90-170.

Note: Make sure customer's power matches subsystem requirements. Check for correct blower and motor rotation.

11. Perform power supply checks and note special tape unit power supply requirements, see 90-180.
12. Perform **all checks and adjustments** on 90-190.
13. Run system diagnostics on 90-200. (Refer to User's Guide.)
14. If any Emulator is run on a S/360, install jumper, see 90-200.
15. Generate a read only tape, on 90-200.

Note: It is possible to combine 3803 Models 1 and 2 in one subsystem. Be sure your customer understands that a 3803 Model 1 tape control **cannot** address any 3420 Models 4, 6, or 8 tape units.

UNPACKING INSTRUCTIONS

Unpack tape control and tape units.

Refer to Unpacking Instructions, which are in a plastic envelope attached to each unit. Move discarded packing material away from work area. File Unpacking Instructions for future reference if tape subsystem is to be moved.

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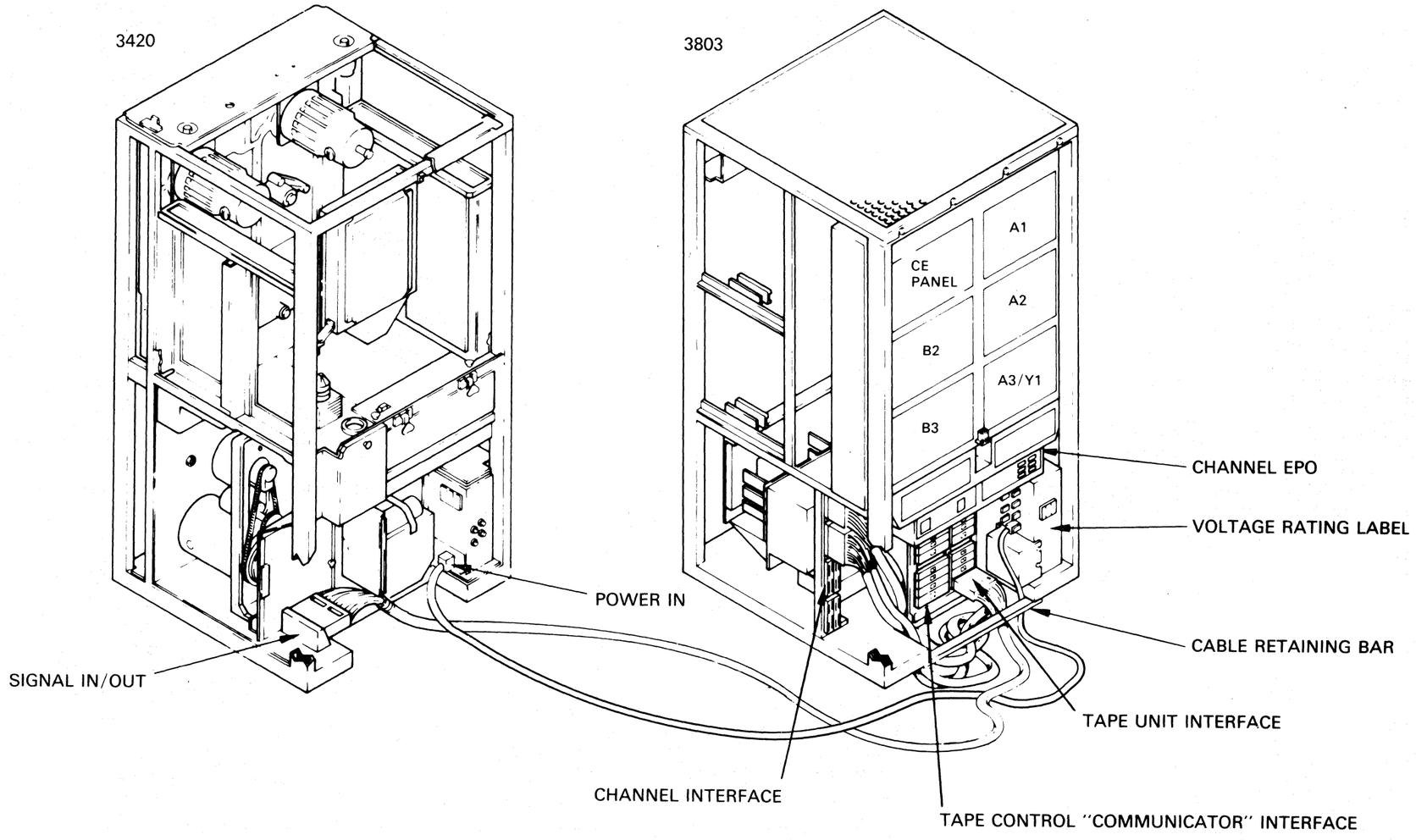
CHANNEL ATTACHMENT

The 3803 Model 2 at 6250 bpi will attach to these systems via the indicated channels:

System	3420-8	3420-6	3420-4
370/195	2860/2880	2860/2880	2860/2880
370/168	2860/2880	2860/2880	2860/2880
370/165-2	2860/2880	2860/2880	2860/2880
370/165	2860/2880	2860/2880	2860/2880
370/158	BKMPX	BKMPX	BKMPX
370/155-2	BKMPX	BKMPX	BKMPX
370/155	BKMPX	BKMPX	BKMPX
370/145	SEL	SEL	SEL
370/135	SEL	SEL	SEL
360/195	2860/2880	2860/2880	2860/2880
360/91	2860	2860	2860
360/85	2860/2880	2860/2880	2860/2880
360/75	2860	2860	2860
360/65-67	2860	2860	2860
360/50	N/A	N/A	SEL



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INSTALLATION CHECKLIST

3803-2 TAPE CONTROL

Installation Procedure	Reference Page	Initial Box When Completed
Configuration Worksheet	90-030	
Unpacking	90-000	
Cables	90-060 90-070 90-080	
Cable Retaining Bar	90-060	
Kickplates	90-090	
Address/Priority/Feature Plugging	90-110	
Card and Cable Seating	90-000	
Operator's Panel Labels	90-160	
Wire Seal Removal	90-180	
Check Capacitor Mounting Screws	90-180	
Power Supply Checks	90-180	
ESD Check and Adjustment	90-190	
System Diagnostics	90-200	
Emulator (If applicable)	90-200	
Generate READ ONLY Tape	90-200	

3420 TAPE UNIT

Installation Procedure	Reference Page	Initial Each Box When Completed							
		0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
Unpacking	90-000								
Cables	90-060 90-070								
Caster Locks	90-000								
Kickplates	90-090 90-100								
Field Tester Conversion	90-170								
Wire Seal Removal	90-180								
Power Supply Checks	90-180								
Checks and Adjustments	90-190								
System Diagnostics	90-200								

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CONFIGURATION WORKSHEET INSTRUCTIONS

Complete the configuration worksheet on Page 90-040 for your installation. Check customer requirements before configuring each system. When installation is completed, place worksheet in the front of subsystem ALDs and keep as a subsystem cabling history.

Complete all applicable blocks in the worksheet for each 3803 tape control:

1. Indicate each 3803 serial number in decimal.
2. Indicate processing unit/Channel identity and cable numbers.
3. Assign an address to each 3803 tape control in hex (bits 0-4, Example: 18X/3BX).
4. Assign "Select Out" priority ("high"/"low") for each interface by checking applicable box.
5. Indicate features installed on each 3803 tape control.
6. Assign 3420 addresses to each 3803. Check the 0-7 (low order) block on one "host" 3803, and the 8-F (high order) block on the other "host" 3803.
7. Draw in cabling for your configuration and insert cable key numbers.

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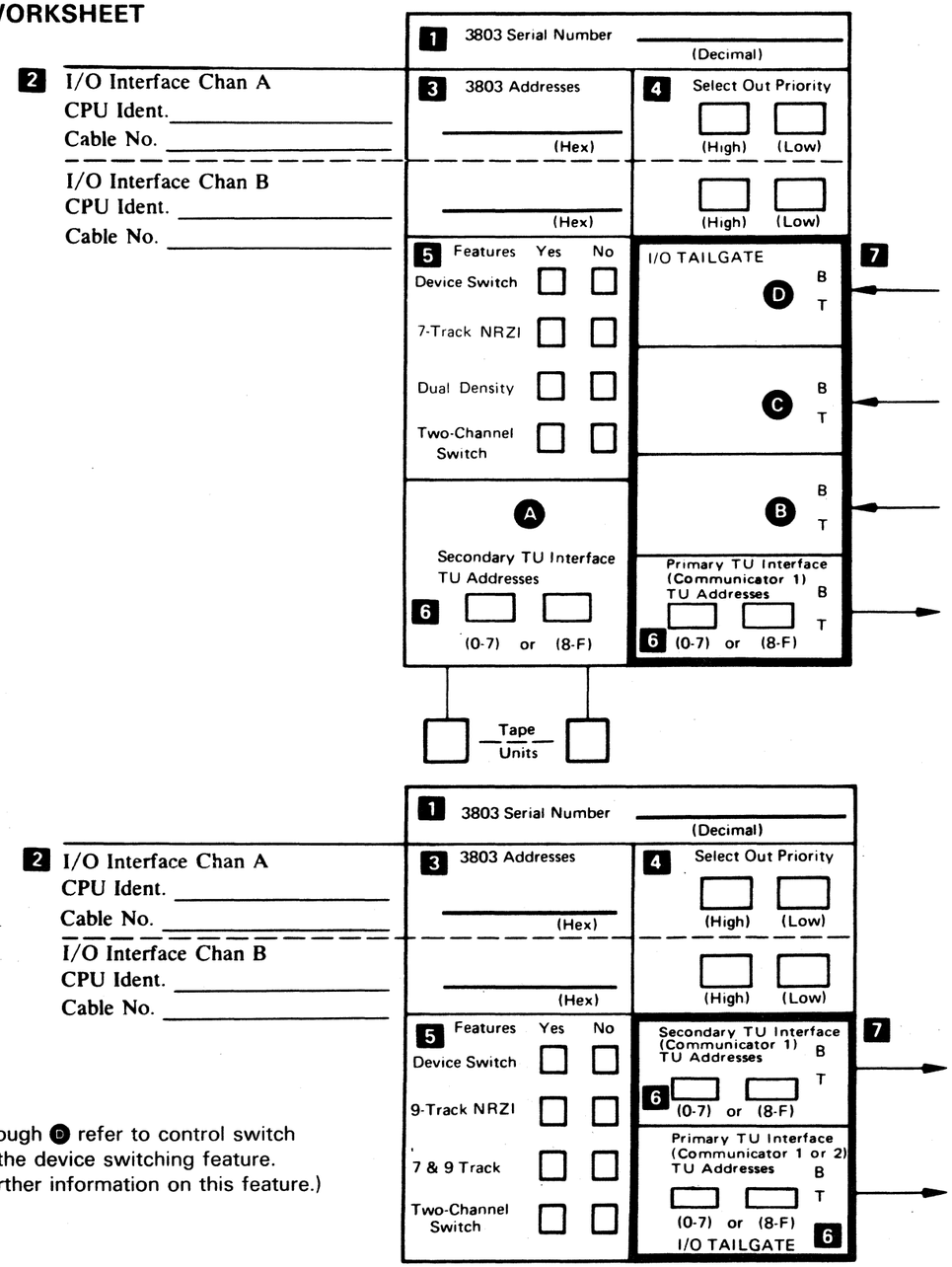
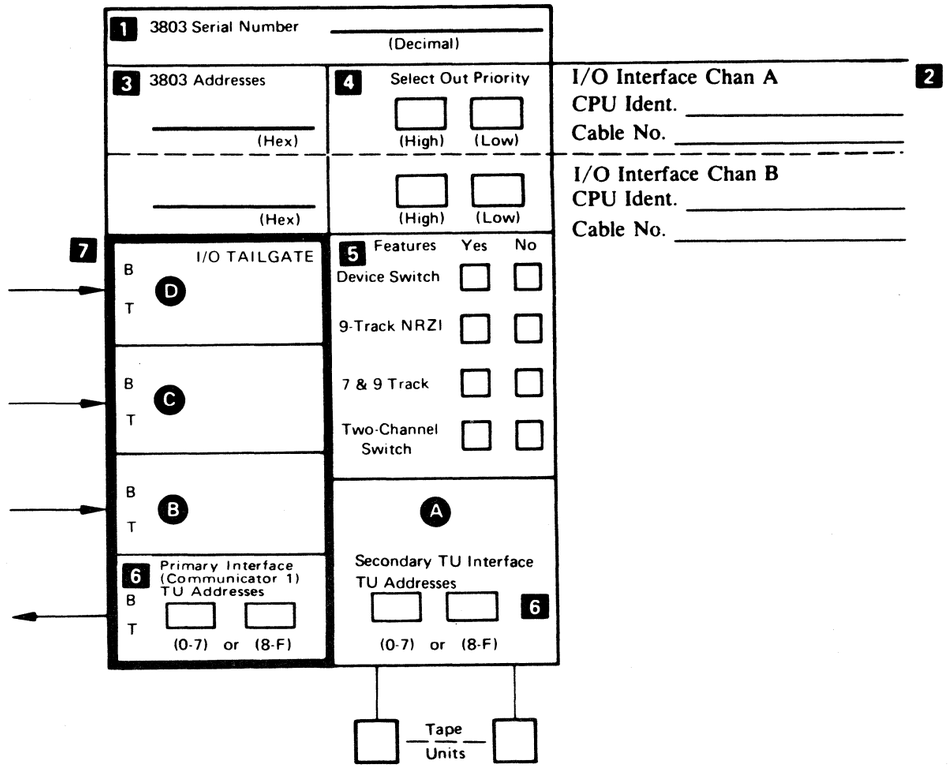
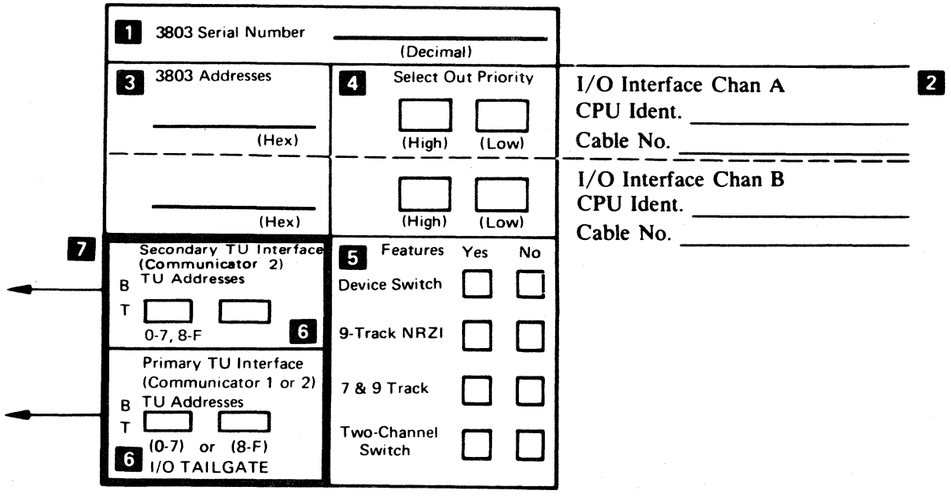
CONFIGURATION WORKSHEET







Note: Symbols Ⓐ through Ⓓ refer to control switch paths A through D of the device switching feature. (See Section 58 for further information on this feature.)

XJ0300 Seq 1 of 2	2736022 Part Number	See EC History	845958 1 Sep 79	847298 15 Aug 83				

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SECTION A: DEVICE SWITCHING FEATURE

A-1 Tape subsystem configuration flexibility is provided by field-installable switching features that allow up to 16 tape units to be switched between four tape controls. The three device switching features available with the tape subsystem are:

2 Control Switch (2 X 8 or 2 X 16 configuration, see Figures 1 and 4 on page 90-051)

3 Control Switch (3 X 8 or 3 X 16 configuration, see Figures 2 and 3 on page 90-051)

4 Control Switch (4 X 8 or 4 X 16 configuration, see Figures 5 and 6 on page 90-052)

A 3803 must have a Communicator installed in order to be switched. The Communicator sends tape unit selection and device interface signals to one of two device switches, depending on whether tape units 0 through 7 or 8 through F are being addressed. The location of the device switches depends on the configuration desired. For example: In a 2, 3, or 4 X 8 configuration, the switching feature is required only on the first 3803.

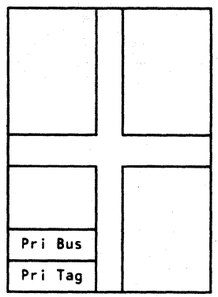
The Communicator is installed by removing the selection logic circuits and the associated device interface cabling in the basic 3803. Different logic circuitry and cables to the device switches are then installed.

Using a combination of the Communicator and the 2, 3, or 4 Control Switch, two, three, or four interconnected tape controls can address a maximum of 16 tape units. Figures 1 through 6 show some possible switching configurations and cabling.

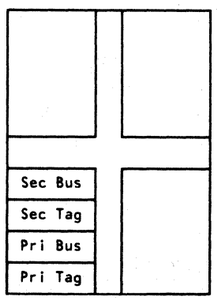
Note:

[1] The dark gray end of the signal cable is indicated by the arrow tip. (See Figure 1, 90-060.)

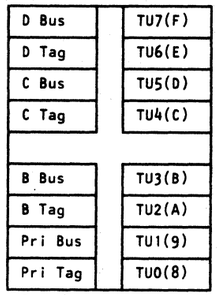
Figure 7. Cable Connectors



Non-host 3803 with Communicator 1 feature only. Sales Feature (FC)9071.



Non-host 3803 with Communicator 2 feature only. (FC)9073.



Host 3803 with 4-Control Switch feature. (It also has the Communicator 1 feature.)

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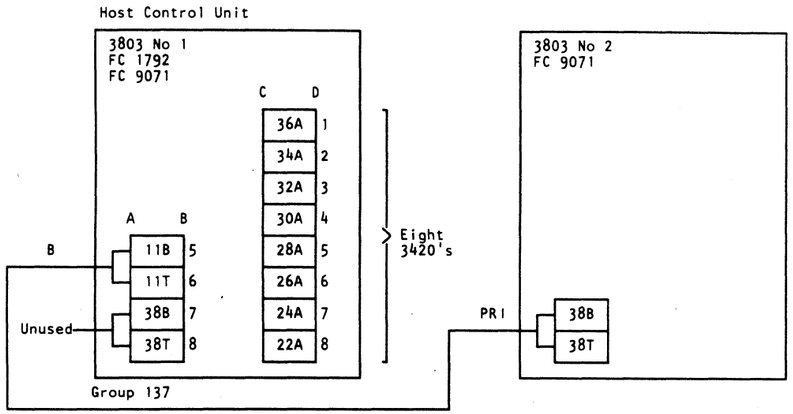

Figure 1. 2 x 8 Switch Option

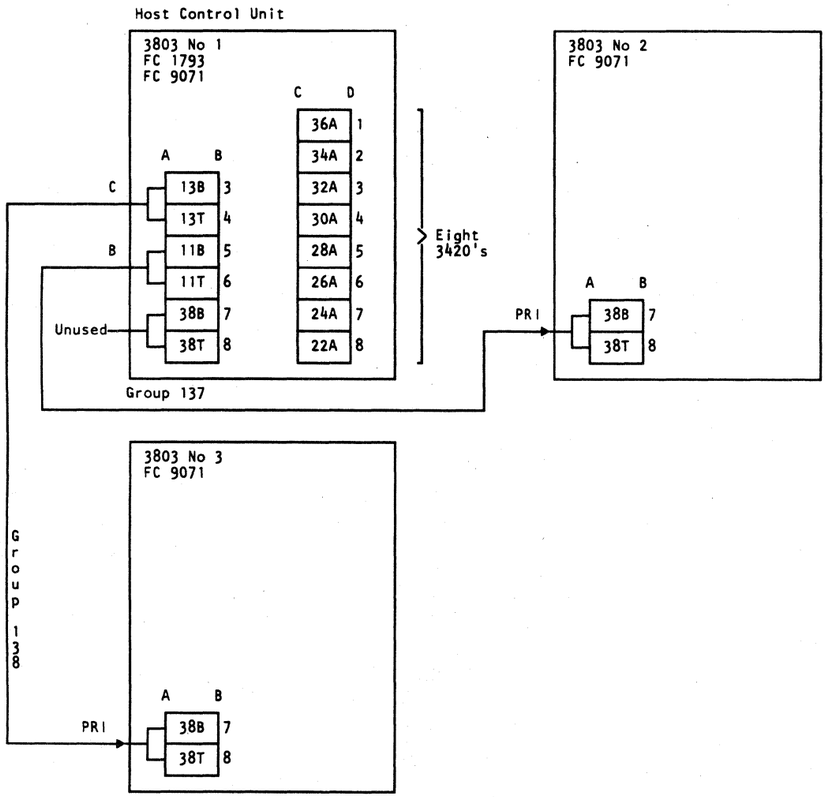

Figure 2. 3 x 8 Switch Option

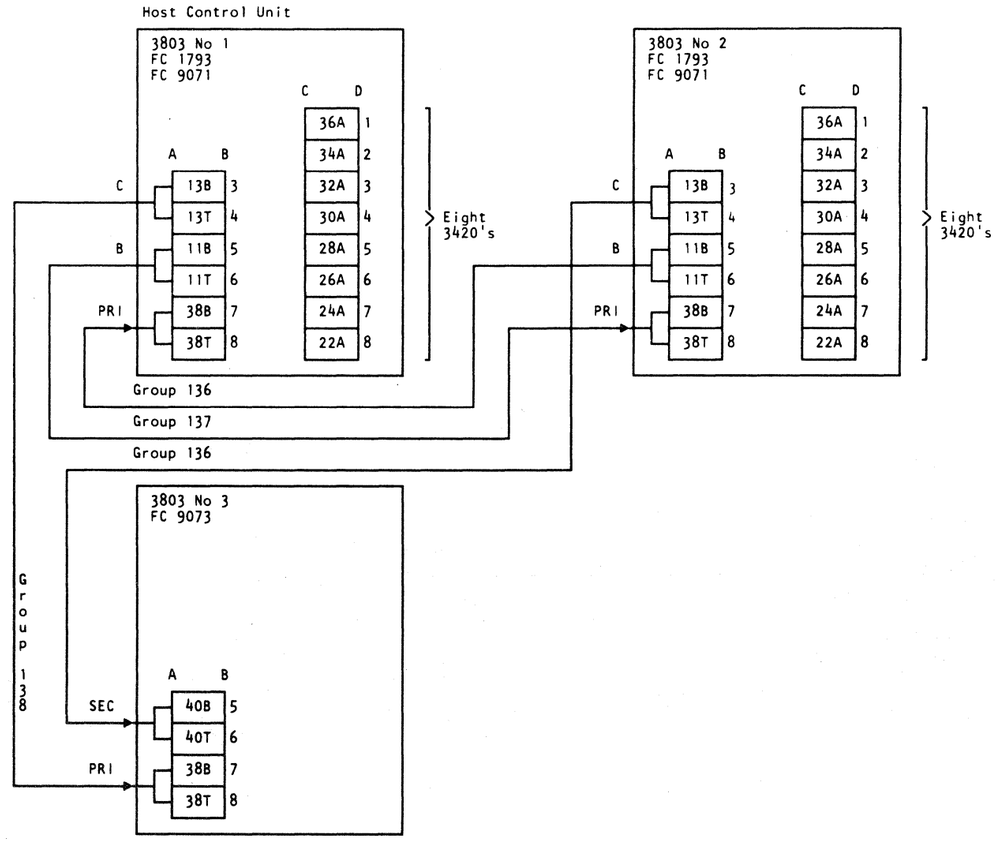

Figure 3. 3 x 16 Switch Option

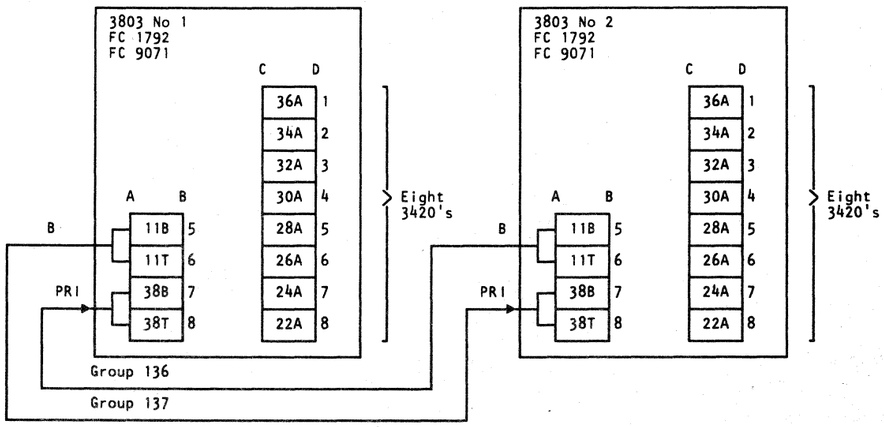

Figure 4. 2 x 16 Switch Option

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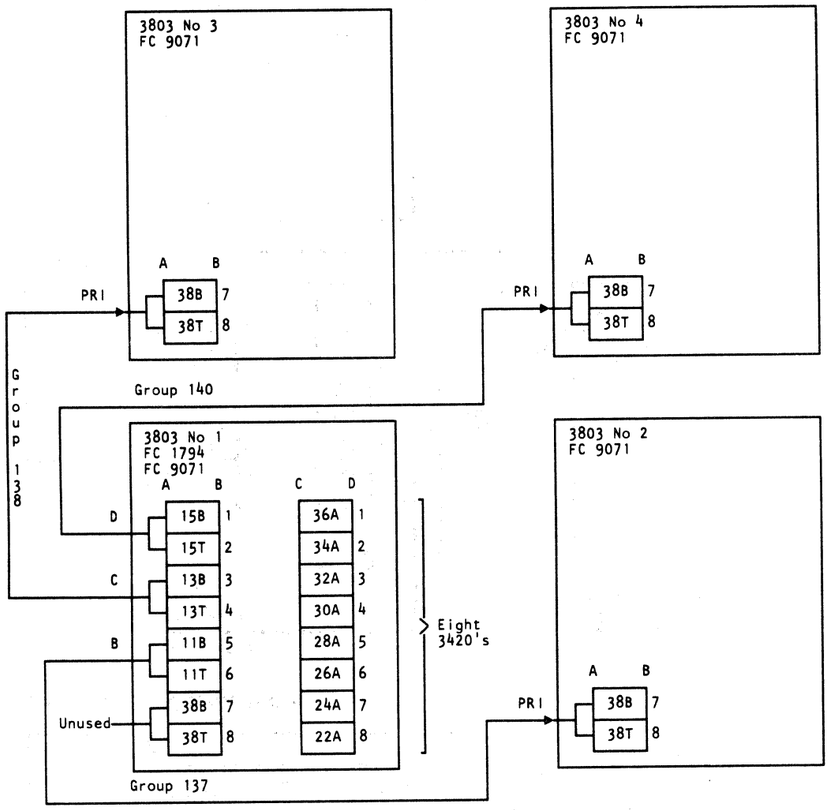

Figure 5. 4 x 8 Switch Option

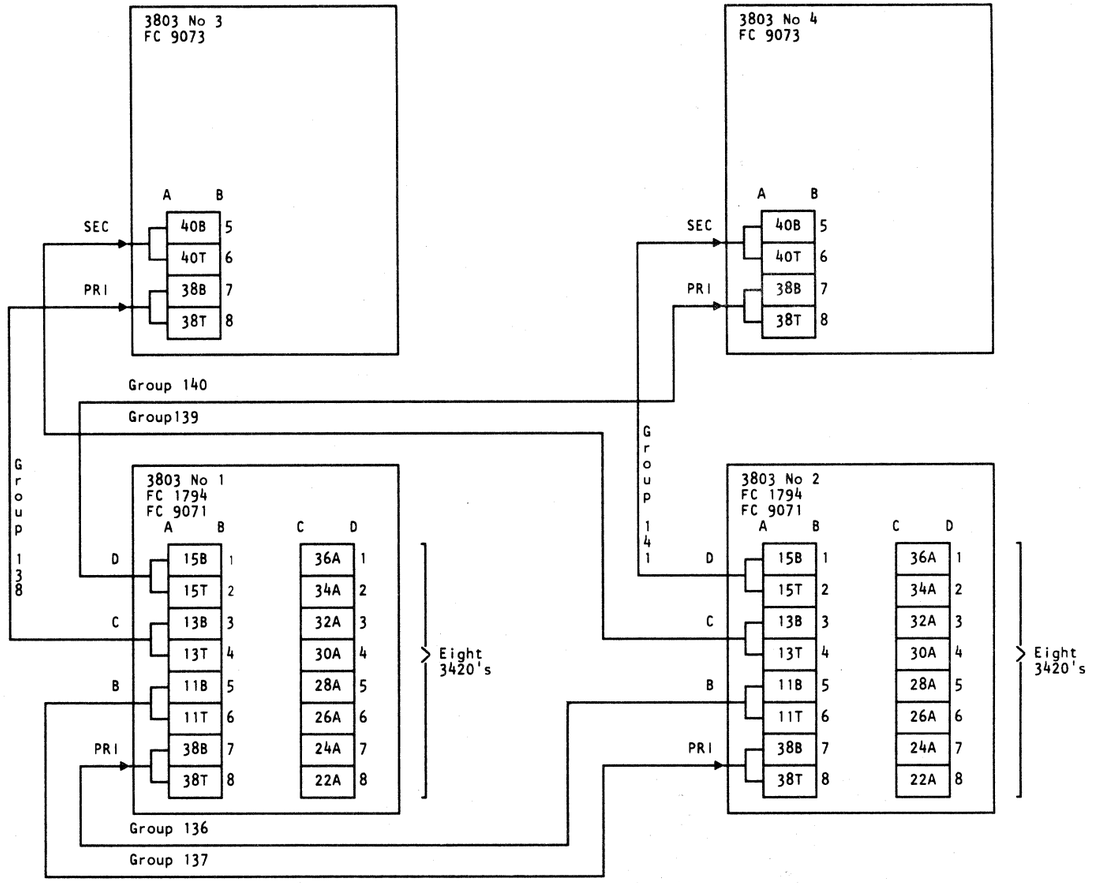

Figure 6. 4 x 16 Switch Option

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SECTION B. SUBSYSTEM CABLING

B-1 Unpack the interface and power cables and lay in place.

Refer to the "Key Number" or "Connector ID" and "X-Length" shown on each interface cable label when placing cables (see Figure 3).

Refer to power cable connector (see Figure 2) to ensure that power cables will be located correctly.

Caution: Ensure that the color scheme on the connectors is followed.

B-2 Plug Cables and Terminators:

a. Plug cables at tape control and tape units. Each tape unit's address is determined by the position on the tape control interface panel to which its signal cable is connected.

Caution: Do not connect 3803 power cable to customer's receptacle at this time.

b. Insert terminators in "outgoing" cable positions in subsystems where "outgoing" cables 132 and 133 are not used.

c. Install cable retaining bars when cabling is complete.

B-3 Observe 'from' and 'to' designations given in Figure 1, Page 90-070. Red or red-striped labels indicate 'from' end of cables; white labels indicate 'to' ends of cables.

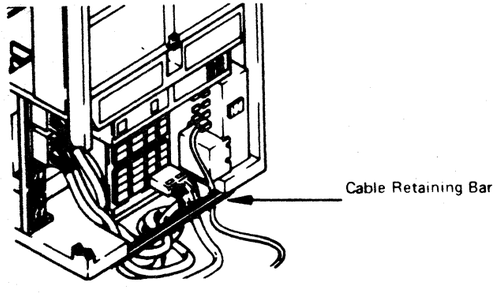
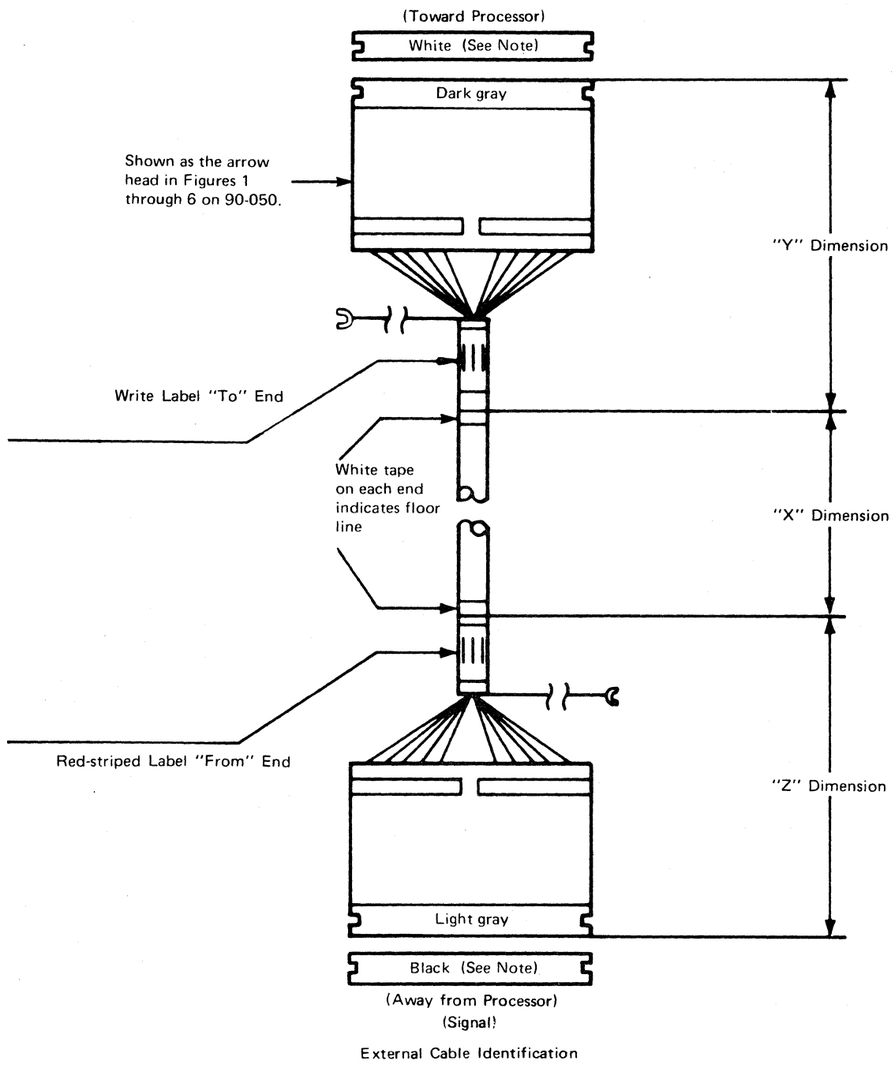


Figure 1. Signal Cable



Note: On chrome plated tape unit signal cable connectors, observe the color at the center screw hole.

Figure 2. Power Cable

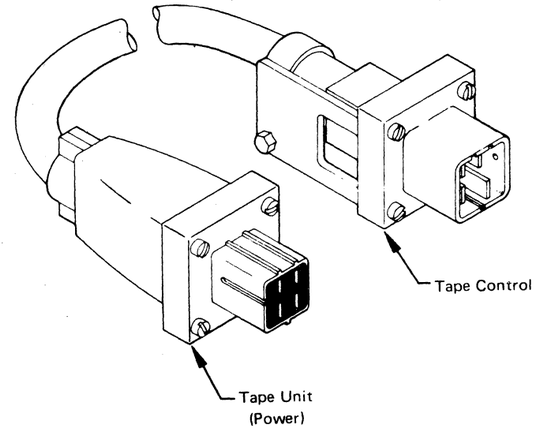


Figure 3. Dimension Explanation

"X" Dimension = Distance Between Cable Entry Holes in Floor

"Y" & "Z" Dimension = Distance Above the Floor from the Entry Hole to the Connection within the Machine

Total length = sum of X, Y, and Z dimensions.

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SUBSYSTEM INSTALLATION (Cont'd)

SECTION B. SUBSYSTEM CABLING (Cont'd)

Figure 1. External Cables

Note: *Cables are identified by either key number or connector ID.*

Group No.	Conn. ID	Plug Location	Cable Group	Key No.	Cable P/N	From	To	Notes
-	-	-	129	129A 129B	2281630 2523073	3420 Signal 60 Hz 3420 Power 60 Hz	3803	4, 5, 7
3920	1B (Chan A) 3B (Chan B) 1T (Chan A) 3T (Chan B)	01S-A1A1 01S-A1A5 01S-A1A3 01S-A1A7	130	130 B 130 T	5353920 5353920	3803	Multiplexor Channel	1, 9
3920	1B (Chan A) 3B (Chan B) 1T (Chan A) 3T (Chan B)	01S-A1A1 01S-A1A5 01S-A1A3 01S-A1A7	131	131 B 131 T	5353920 5353920	3803	Selector Channel	1, 9
-	2B (Chan A) 4B (Chan B) 2T (Chan A) 4T (Chan B)	01S-A1B1 01S-A1B5 01S-A1B3 01S-A1B7	132	132B 132T	5353920 5353920	3803	Control Unit	1, 9
-	2B (Chan A) 4B (Chan B) 2T (Chan A) 4T (Chan B)	01S-A1B1 01S-A1B5 01S-A1B3 01S-A1B7	133	133B 133T	5353920 5353920	3803	Channel-Channel Adapter	1, 3, 9
1178	5A (Chan A) 7A (Chan B)	J11 J13	134	134A	5351178	3803	Channel EPO	2
1178	9A	01U-A1	135	135A	5351178	3803	2065/2167	8
6456	11B 11T	01T-A1A5 01T-A1A6	136	136B 136T	5466456 5466456	3803 No. 2	3803 No. 1	4
6456	11B 11T	01T-A1A5 01T-A1A6	137	137B 137T	5466456 5466456	3803 No. 1	3803 No. 2	4
6456	13B 13T	01T-A1A3 01T-A1A4	138	138B 138T	5466456 5466456	3803 No. 1	3803 No. 3	4
6556	13B 13T	01T-A1A3 01T-A1A4	139	139B 139T	5466456 5466456	3803 No. 2	3803 No. 3	4
6556	15B 15T	01T-A1A1 01T-A1A2	140	140B 140T	5466456 5466456	3803 No. 1	3803 No. 4	4
6556	15B 15T	01T-A1A1 01T-A1A2	141	141B 141T	5466456 5466456	3803 No. 2	3803 No. 4	4
-	-	-	142 or 129	142A 142B	2281630 2521595	3420 Signal 50 Hz 3420 Power 50 Hz	3803	4, 5, 6, 7
143	1A	Signal	143 or (143)	143A	2281630	3420 Signal 60 Hz	3803	4, 6, 7
144	3A	Power	144 or (144)	144A	2523073	3420 Power 60 Hz	3803	6, 7
145	3A	Power	-	-	2521595	3420 Power 50 Hz	3803	6, 7

Figure 2. Channel Cable Maximum Length for 6250 bpi.

System	From 3803-2 With	To Channel	Length - Feet (Meters)
S/360	3420-8	2860 2880	72 (22,0) 119 (36,3)
S/370	3420-8	2860 Mod 135	72 (22,0)
		Mod 155 Mod 155-2 Mod 158	103 (31,4)
		Mod 145 2880	119 (36,3)
4331	3420-6/8	None	N/A
	3420-4	BYTEMPX*	103 (31,4)
All Other Systems	3420-8	BKMPX*	119 (36,3)

* Tape operations allowed only when all other byte channel devices are quiesent.

Notes:

[1] To attach eight or less tape controls to one channel, the last tape control must be attached to the channel with a sum of no more than 200 feet (61,0m) of cable. If the tape control is attached to a 3420-6, subtract 15 feet (4,5m) for each intervening control unit between the channel and the last tape control. If the tape control is attached to a 3420-8, subtract 20 feet (6,1m) for each intervening control unit between the channel and the last tape control (see Note 10). For cable length limitations when attaching a 3803-2 at 6250 BPI, see Figure 2.

[2] Sequence and Control (EPO).

[3] Channel to channel adapter (Sales Feature 1850).

[4] Total cable length from a 3420 tape unit to the most remote 3803 tape control must not exceed 120 feet (36,6m). (Group 129 or 142, or 143, plus group 136-141.)

[5] Includes both signal and power cable. A maximum of eight 3420 tape units can be connected to each 3803 Tape Control 1 and 2. Tape units cannot be connected to tape control 3 and 4 for power requirements unless they are used with cable group 144.

[6] Parenthesis indicates cables to be used in World Trade countries for 60 Hz machines.

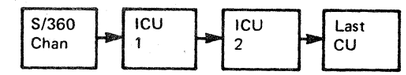
[7] When the number of 3420s to be connected to a 3803 Model 2 exceeds the limitations of power (60 Hz), each extra 3420 tape unit may be supplied power by another 3803 tape control using cable group 144. Cable group 143 is available to signal attach tape units using cable group 144. With SF9001 installed, the 3803 Model 2 may power a total of eight 3420s (any model).

[8] For use with remote channel switch special feature.

[9] Part number 5466456 (24 Signal) may be substituted for 5353920 (20 Signal) for cable group numbers 130, 131, 132 and 133.

[10] Terminators are required when the 3803 is the last control unit in a chain or the only control unit on the channel. Use either 5440649 (20 position) or 2282675 (24 position) bus terminators and either 5808324 (20 position) or 2282676 (24 position) tag terminators as determined by the number of signal lines per cable.

Example:



200 feet (61, 0m) (Maximum 200 feet (61, 0m) per Figure 2)
– 30 feet (9, 0m) (Two intervening CU = 2 X –15 ft)
170 feet (52, 0m) Maximum cable length that can be used

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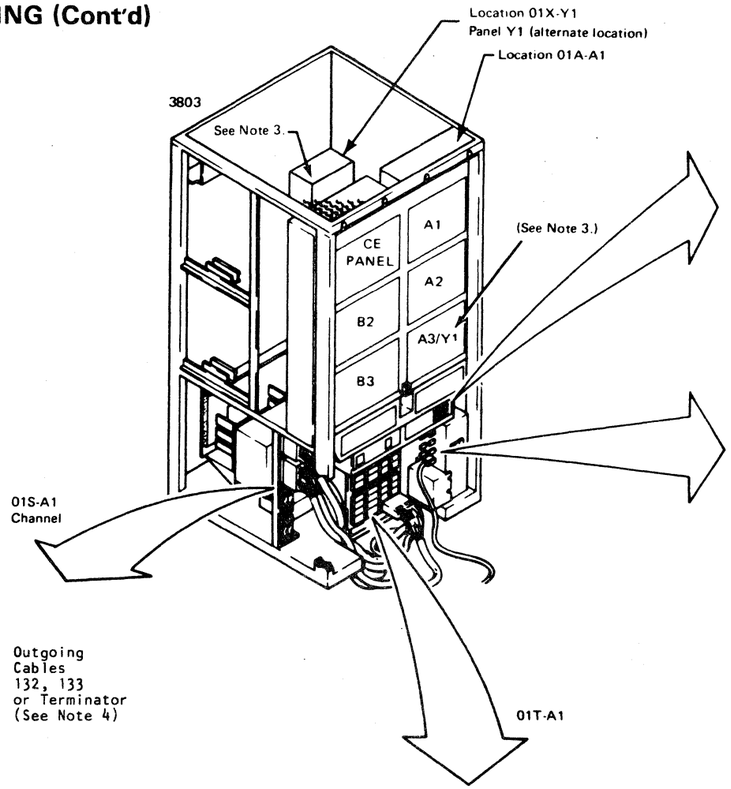
SECTION B. SUBSYSTEM CABLING (Cont'd)



	A	B	
1	1B Bus Chan A	2B Bus Chan A	1
3	1T Tag Chan A	2T Tag Chan A	3
5	3B * Bus Chan B	4B * Bus Chan B	5
7	3T * Tag Chan B	4T * Tag Chan B	7

Incoming Cables 130, 131, 132, 133 (See Note 4)

Outgoing Cables 132, 133 or Terminator (See Note 4)

	Chan A	Chan B	
	5A (J11)	7A (J13)	EPO 134A See Note 1.

(J5)	18A	20A	(J1)
(J6)	14A	16A	(J2)
(J7)	10A	12A	(J3)
(J8)	6A	8A	(J4)

Tape Unit Power 129B (8) 60 Hz 142B (8) 50 Hz

Communicator

3803 No 1	3803 No 2	3803 No 3	3803 No 4		A	C	
140B	141B			1	Bus 15B	TU 7 (F) 36A	1 ←01TA1C1
140T	141T			2	Tag 15T	TU 6 (E) 34A	2
138B	139B			3	Bus 13B	TU 5 (D) 32A	3
138T	139T			4	Tag 13T	TU 4 (C) 30A	4
137B	136B	139B	141B	5	Bus 40B or 11B	TU 3 (B) 28A	5
137T	136T	139T	141T	6	Tag 40T or 11T	TU 2 (A) 26A	6
136B	137B	138B	140B	7	Bus 38B	TU 1 (9) 24A	7
136T	137T	138T	140T	8	Tag 38T	TU 0 (8) 22A	8 ←01TA1C8

(See Details on 90-050)

129A (8) 60 Hz
142B (8) 50 Hz
3803 Nos 1 and 2 only

Caution: Refer to ALD AA005 Feature Plug List before installing a replacement logic board.

Notes:

Two-channel switch diagnostics AD through AG can only be run when both channel interfaces are cabled to the same central processing unit. If it is necessary to run diagnostics AD through AG during initial checkout, plan temporary cabling to meet this requirement.

[1] Both EPO cables must be plugged if the two channel switch feature is installed, and the two channels are not on the same processing unit or not on the same channel frame. Remove any temporary jumper plugs.

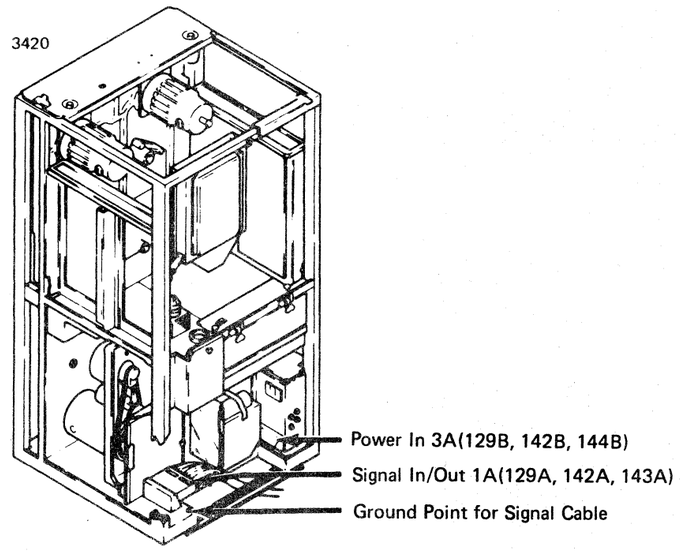
[2] For cable, part 5466456 (48 pin), use terminator, part 2282675 (bus) and 2282676 (tag).

For cable, part 5353920 (40 pin), use terminator, part 5440649 (bus) and 5440650 (tag).

[3] Panel Y1 is located in position 01A-A3 unless the 3803-2 has optional features installed. On feature machines, panel Y1 is located in positon 01X-Y.

[4] For cable group number, key number, part number, to and from relationship, see Figure 1 on 90-070.

* Cables plugged when the two-channel switch feature is present.



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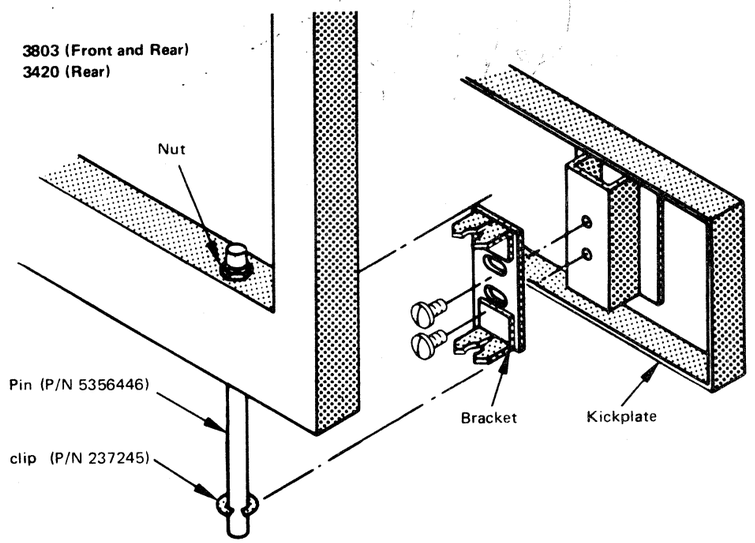
SECTION C. KICKPLATES

C-1 Install 3803 front and rear kickplates and 3420 rear kickplates as shown in Figure 1.

1. Attach pins, nuts, and retaining clips to front and rear frame members of the 3803 and rear frame member of each 3420 as shown in Figure 1.
2. Mount kickplates by pushing brackets onto pins. Clips must be positioned below lower flange of brackets.

   Note: Leave 3420 rear kickplates off until cabling is complete.
3. Turn nuts on pins to level kickplates.
4. If necessary, realign 3803 covers after kickplate installation.

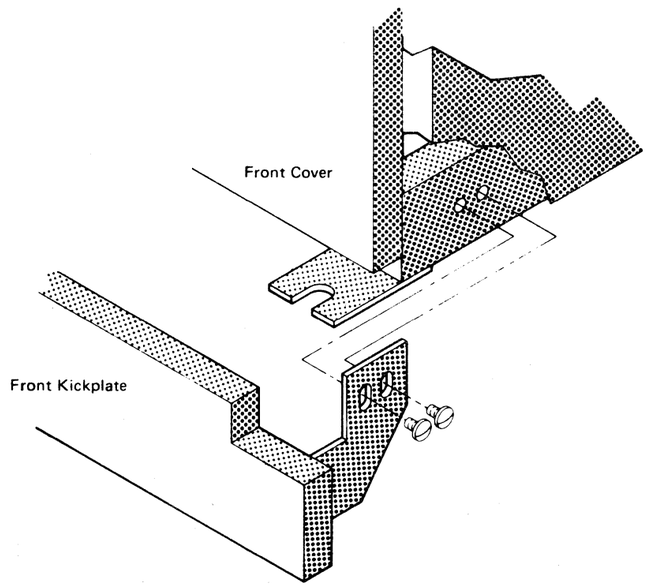
Figure 1. 3803 (Front and Rear Kickplates)
3420 (Rear Kickplates)



C-2 Install 3420 front kickplates as shown in Figure 2.

1. Install front kickplates before moving tape units into place.
2. Elongated holes in the bracket allow kickplate to be leveled and adjusted to clear the front cover.

Figure 2. 3420 (Front Kickplates)



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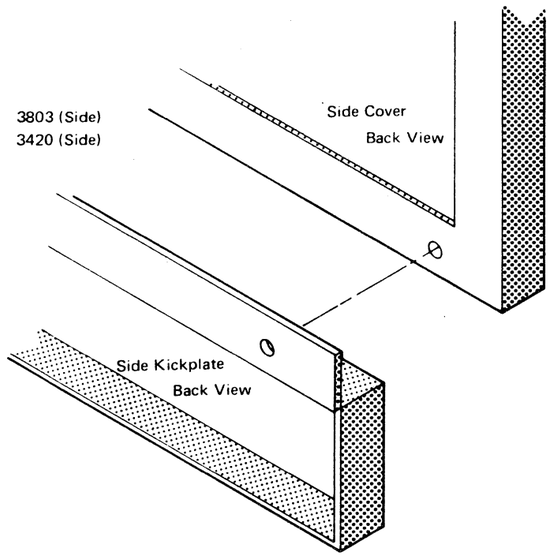
SECTION C. KICKPLATES (Cont'd)

C-3 Install 3803 and 3420 side kickplates as shown in Figure 3.

1. Install side kickplates only on the machines at each end of a group. Use screw P/N 731629.
2. Open or remove covers to attach kickplates. Use 12-inch (305 mm) kickplate, part 2501286 (notched corner), on cover adjacent to tape unit power door hinge. Use 13 1/8-inch (333 mm) kickplate, part 5356406, on remaining side covers for 3420 tape units and 3803 tape controls.

Figure 3. 3803, 3420 Side Kickplates

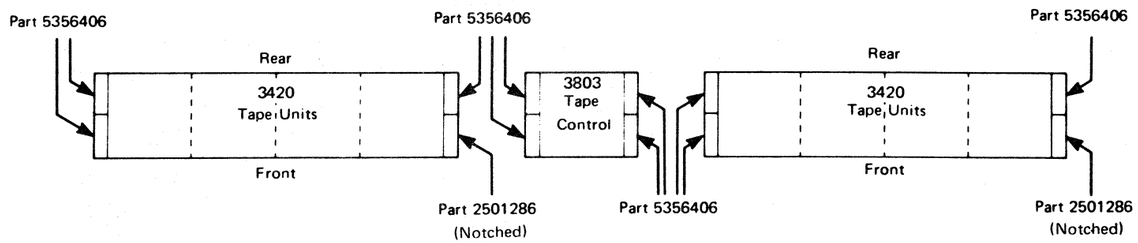


C-4 Typical Subsystem Configuration

Sufficient side kickplates, parts 2501286 and 5356406, are shipped for the configuration shown in Figure 4. Kickplates are not provided for installation between adjacent tape units. Order additional side kickplates by MES, if needed for other configurations.

C-5 Install caster locks (4each), P/N 280336.

Figure 4. Subsystem Configuration



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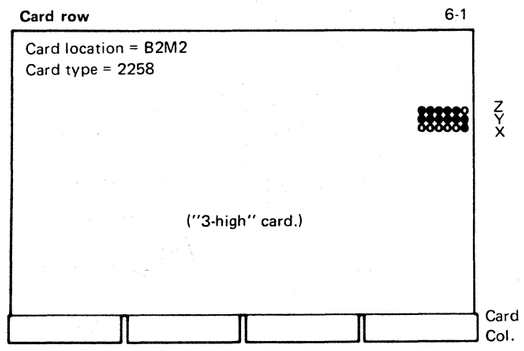
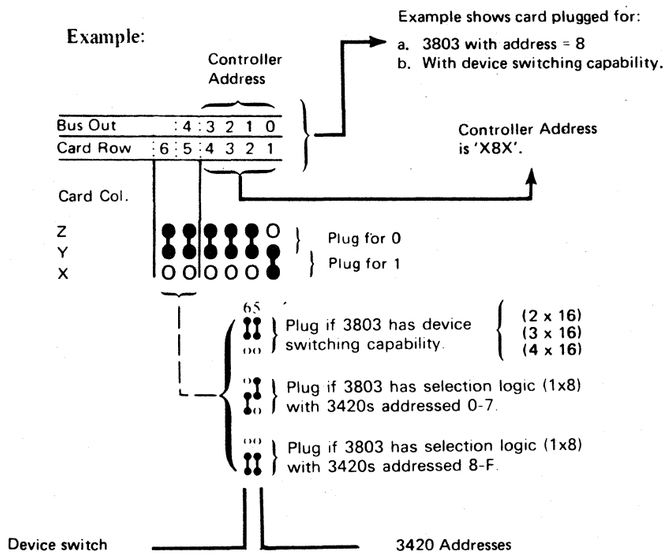
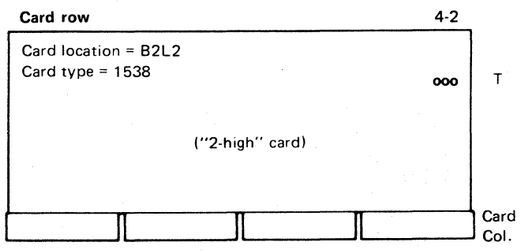
SECTION D. TAPE CONTROL ADDRESS/FEATURE/PRIORITY CARD PLUGGING

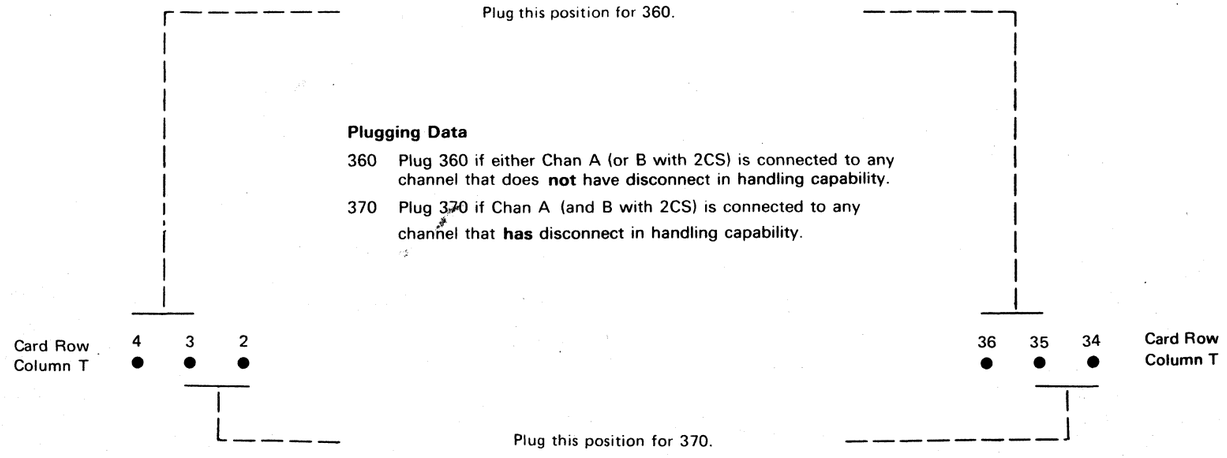
D-1 3803 Address (Channel "A"): Verify factory plugging.

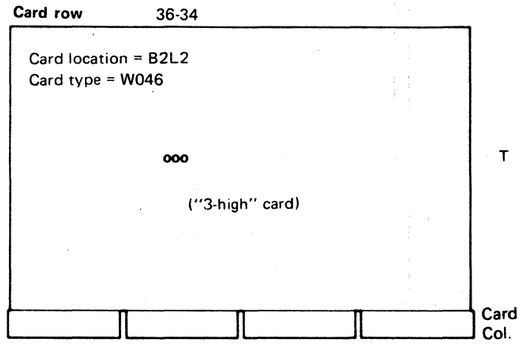




D-2 **Disconnect-In Handling:** S/360 or S/370.







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SECTION D. TAPE CONTROL ADDRESS/ FEATURE/PRIORITY CARD PLUGGING (Cont'd)

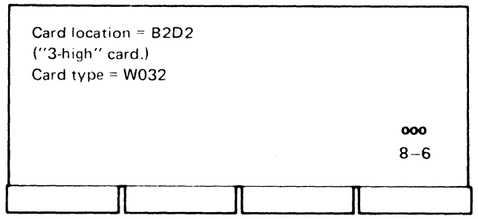
D-3 Select Out Priority:

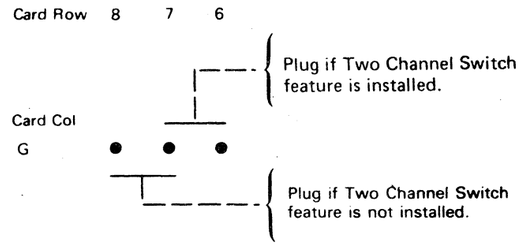
Tape controls are factory-wired to respond to a select out signal (high priority). **If ("low priority") is desired**, change the B2 panel wiring to convert a 3803 tape control to respond to a select in signal. Refer to wiring charts below for rework.

'High' Priority (3803 Responds to 'Select Out')		'Low' Priority (3803 Responds to 'Select In')	
Channel A (FC281)			
From	**To**	**From**	**To**
V4D09 T4B08 S2P11	S2P09 V4B08 T4D09	V4D09 T4B08 S2P11	T4D09 S2P09 V4B08
Channel B (XM181)			
From	**To**	**From**	**To**
U6C02 U4B08 R2P11	R2P09 U6B04 U4D09	U6C02 U4B08 R2P11	U4D09 R2P09 U6B04

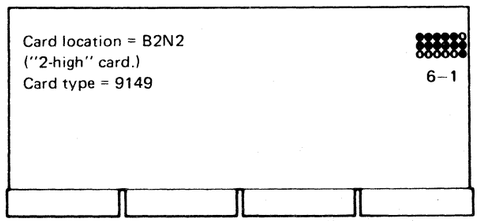
D-4 Features (when applicable to your machine):

a. **Two Channel Switch Feature:** Verify factory plugging.

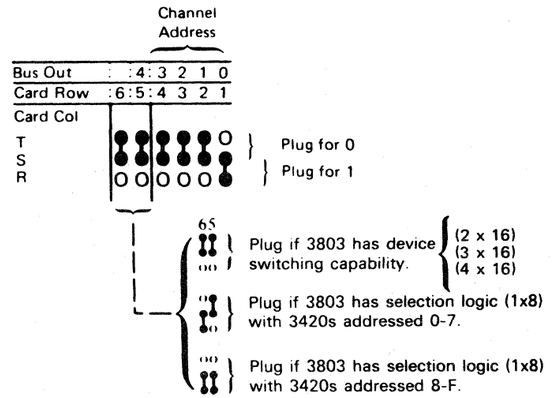




b. **Two-channel switch feature (3803 Address Channel "B"):** Verify factory plugging.

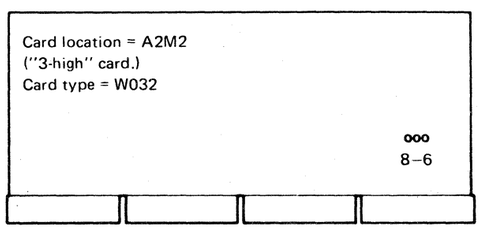


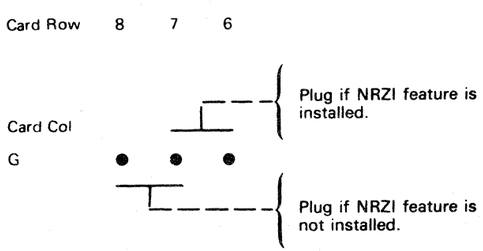
Example:



Example shows card plugged for:
a. 3803 with address = 8.
b. With device switching capability.

c. **NRZI Feature:** Verify factory plugging.





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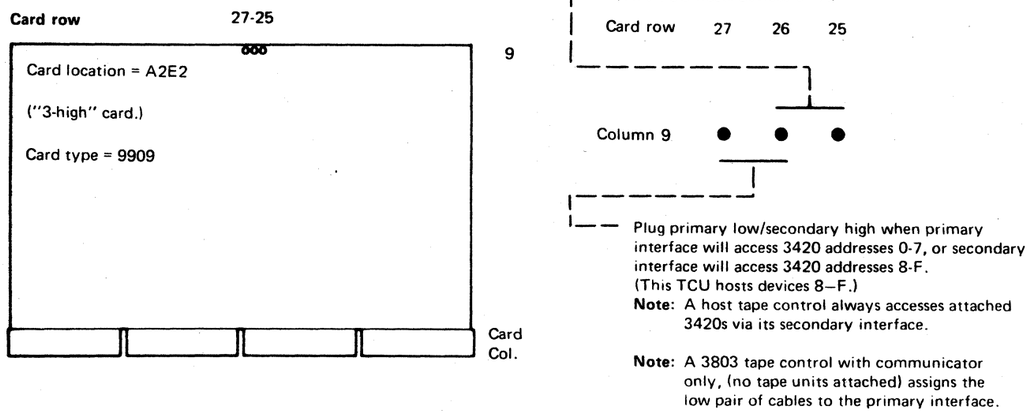
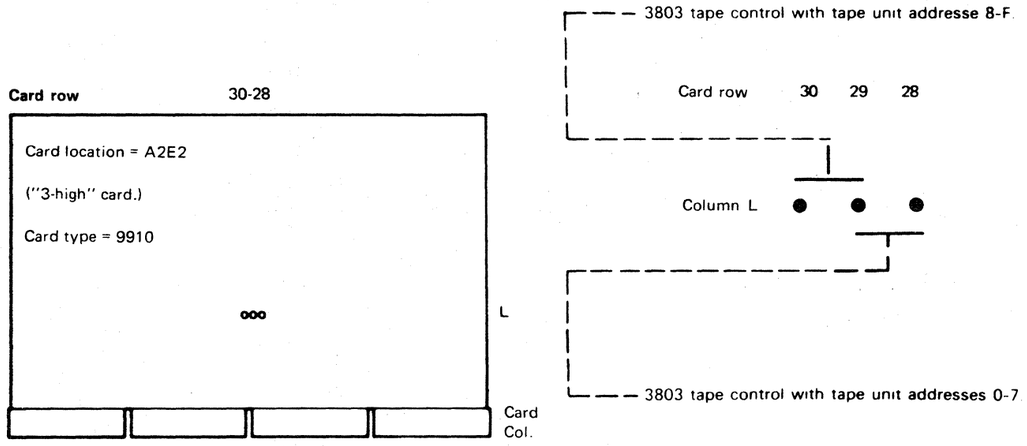
SECTION D. TAPE CONTROL ADDRESS/FEATURE/PRIORITY CARD PLUGGING (Cont'd)

D-5 Primary/Secondary Tape Unit Interface Control:

a. With device switching capability.

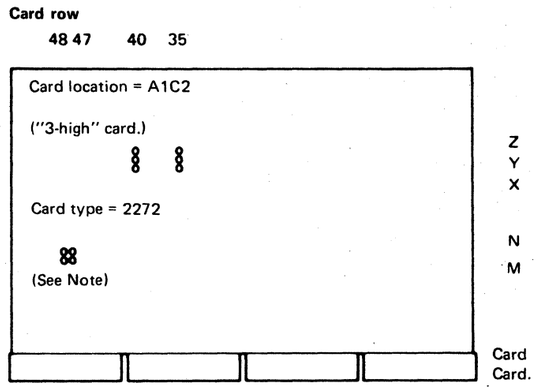


b. With selection logic (1x8).



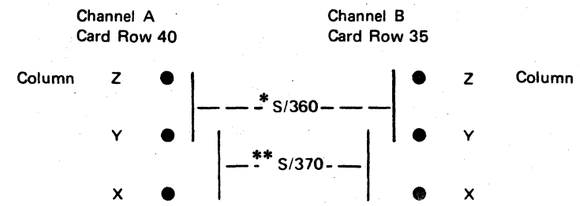
Note: A 3803 tape control with selection logic (1x8) only uses the secondary interface.

D-6 a. **Data In Handling:** S/360 or S/370.



Note: Data Flow Check asymmetry. **Do not change** jumpers unless card is replaced. This is a factory adjustment only.

b. If you have Selection Logic (2x8), go to step D-9 on page 90-160, if device entry, else go to 90-180.
If you have 2x, 3x or 4x switch, proceed to step D-7 on page 90-140.



Plug each channel independently as follows:*

*360 Plug 360 if the attached channel does **not** have data in/data out capability.

370 Plug 370 if the attached channel **has data in/data out capability.

If attached to a 2880 channel, bus out checks may occur if channel timings are not optimized. The 2880 must be at EC718040 level or higher.

*W/O 2CS—Channel B may be plugged to 360 or 370 since it is not used.

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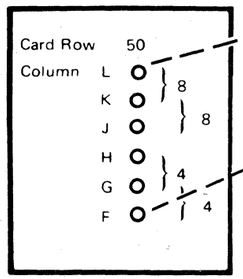
SECTION D. TAPE CONTROL ADDRESS/FEATURE/PRIORITY CARD PLUGGING (Cont'd)

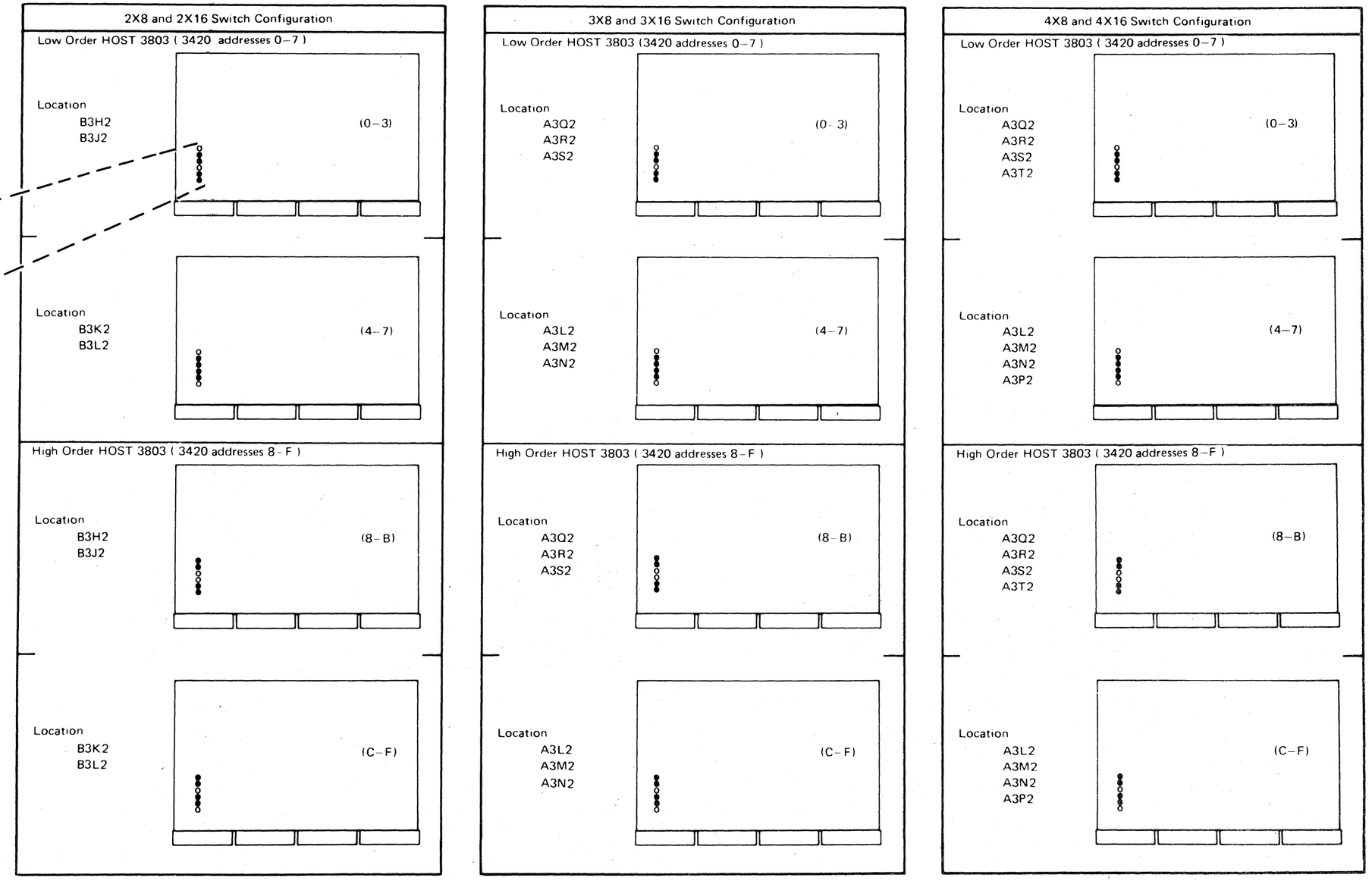
D-7 Tape Switching Feature Address Control: Change or verify jumper plugging of host 3803 tape controls only.

1. For installations with less than a full complement of 3420 tape units (for example, 2x12), plug all cards present as if the non-existent tape units had addresses assigned to them.

Jumper cable locations for switch cards:



2. As each switch card is pulled, refer to the chart on Page 90-150 and verify that device selection priority assignments are correct.



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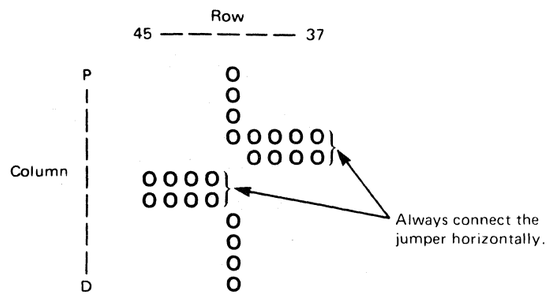
SECTION D. TAPE CONTROL ADDRESS/FEATURE/PRIORITY CARD PLUGGING (Cont'd)

D-8 Device Selection Priority Assignments: Verify that factory plugging of priority jumpers on the switch cards is correct.

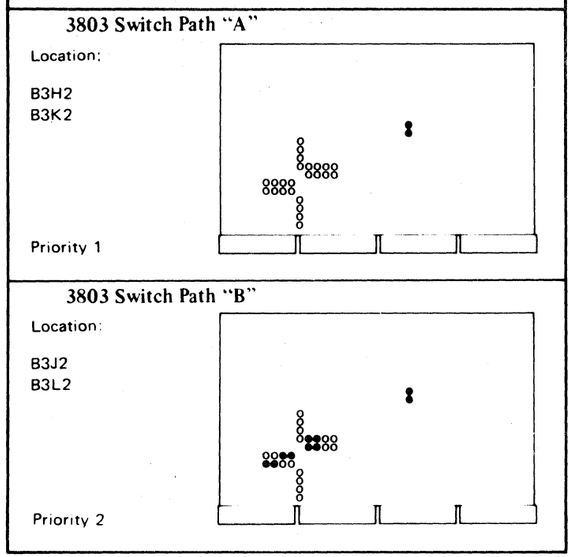
Plugging Rules:

1. A priority must be assigned to each set of cards.
2. No duplication of priority should exist between sets of cards in one 3803 tape control.
3. All cards must have T23-U23 connected by a jumper wire.
4. Factory plugging for these cards should be as shown, and should not have to be changed for any installation.
5. This plugging establishes priority; if two 3803s try to access the same 3420 tape unit simultaneously, the 3803 with the least number of jumpers will take control.

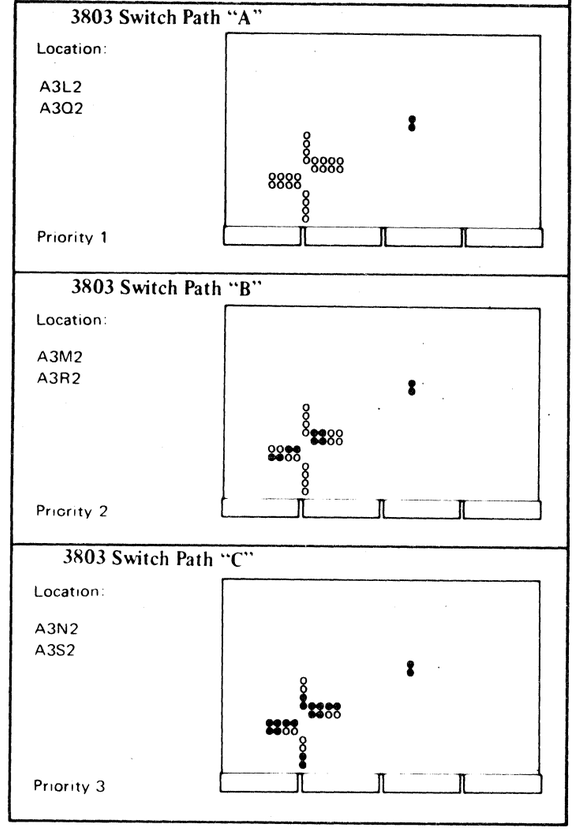
Connect a jumper cable to locations for switch cards as shown below:



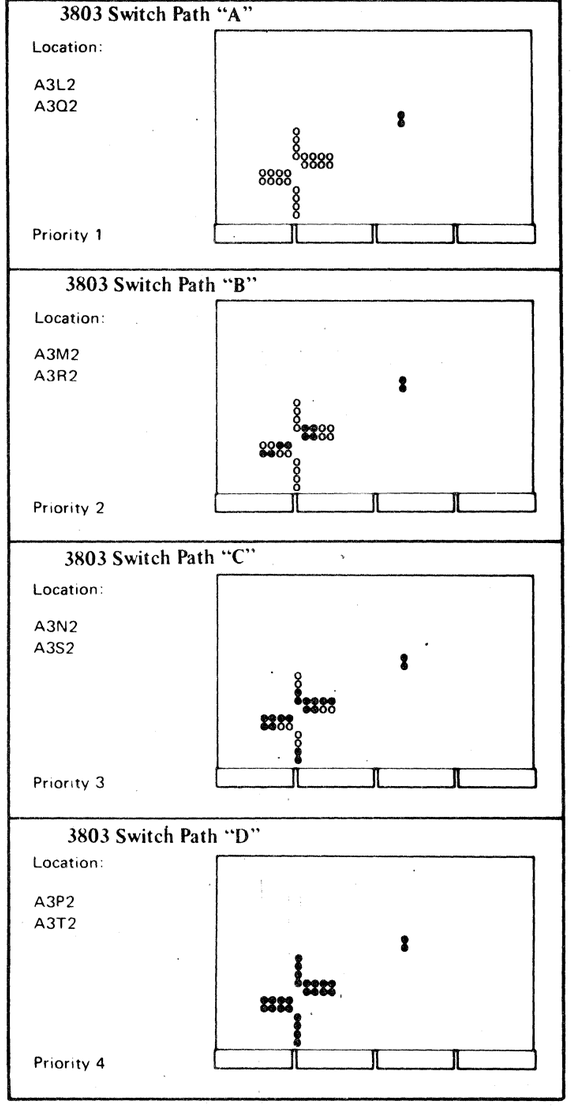
2x8 and 2x16 Switch Configuration



3x8 and 3x16 Switch Configurations



4x8 and 4x16 Switch Configuration



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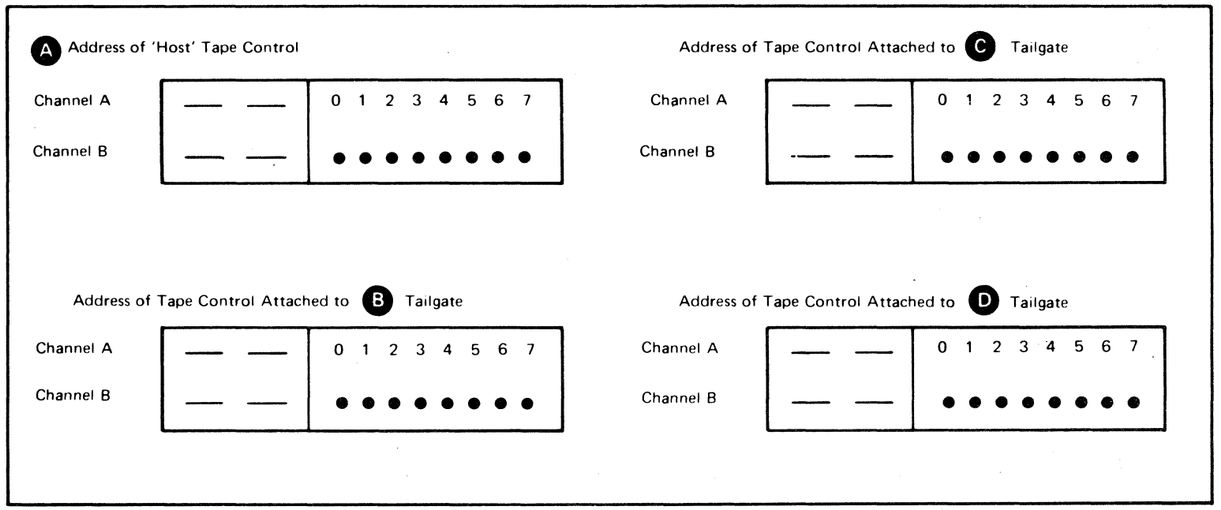
SECTION D. TAPE CONTROL ADDRESS/FEATURE/PRIORITY CARD PLUGGING (Cont'd)

D-9 Apply labels to tape control operator's panel as shown.

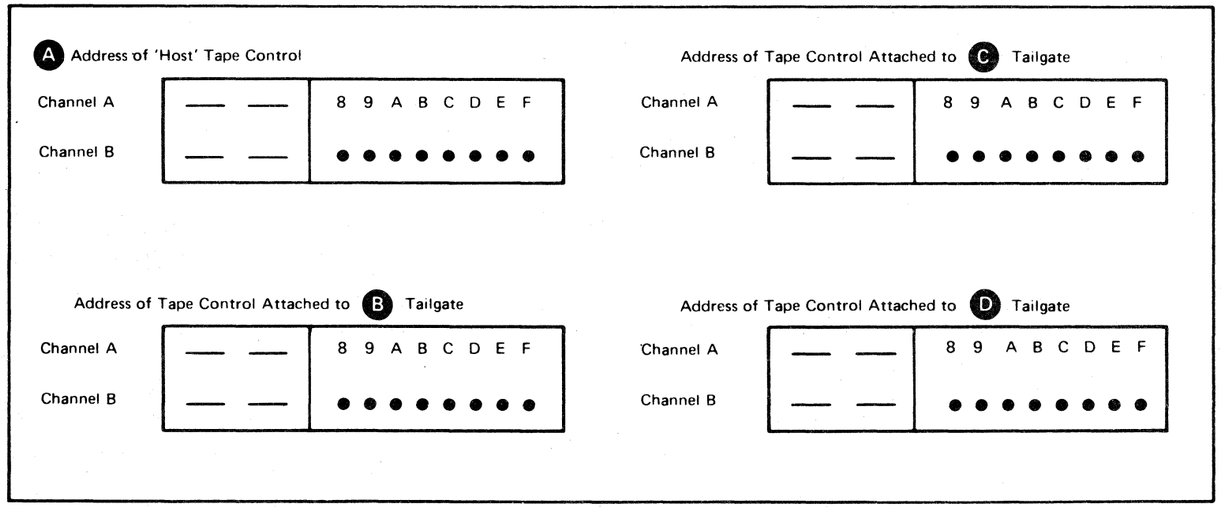
a. Operator's Panel Labels
For the 3803 that "hosts" tape units 0-7:

1. Use labels furnished to indicate addresses of tape control associated with each group of operator panel switches.
2. Apply 3420 address labels 0-7 above each group of switches as shown.



b. Operator's Panel Labels
For the 3803 that "hosts" tape units 8-F:

1. Use labels furnished to indicate tape control addresses associated with each group of operator panel switches.
2. Apply 3420 address labels 8-F above each group of switches as shown.



Note: Symbols A through D refer to control switch paths A through D of the device switching feature.

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FIELD TESTER CONVERSION

Do the following rework to make the field tester compatible with 3420 Models 4, 6, and 8. The new EC Level is 734316. (The field tester remains compatible to 3420 Models 3, 5, and 7.)

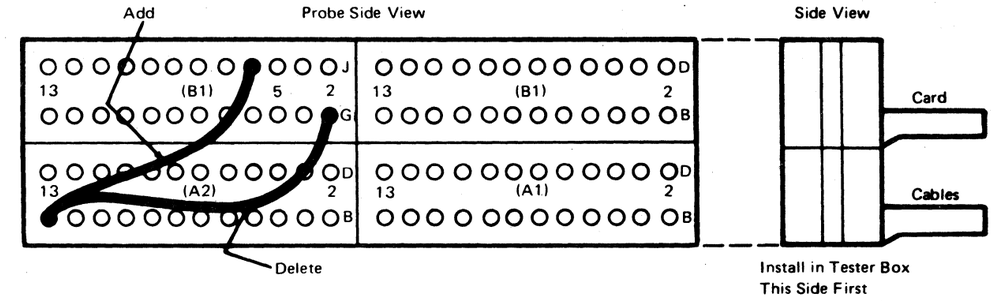
1. Remove the four screws from the bottom of the tester. Then remove the cover. Check the probe side of the card/connector socket block:
   a. If connections are made by means of a printed circuit card, replace the cover and four retaining screws, then skip to step 7.
   b. If connections are made by means of wire wrapping, proceed to step 2.
2. Remove the logic card, unplug the signal cables, and slide the connector block out.
3. Delete yellow wire from B1G02 to A2B13.
4. Add #30 gauge SLT wire from B1J05 to A2B13.
5. Reassemble the tester: slide the connector block into the tester, plug the cables, and install the logic card.
6. Replace the cover and the four retaining screws.
7. Install label, part 1845758, to the right of the data rate switch (8, 16, 32) as shown.
8. Install label, part 1845760, over the existing instructions (1-3) on top of the tester.
9. **Before** converting a Model 3, 5, or 7 tape unit to a Model 4, 6, or 8, take the tape unit offline. Then connect the field tester.

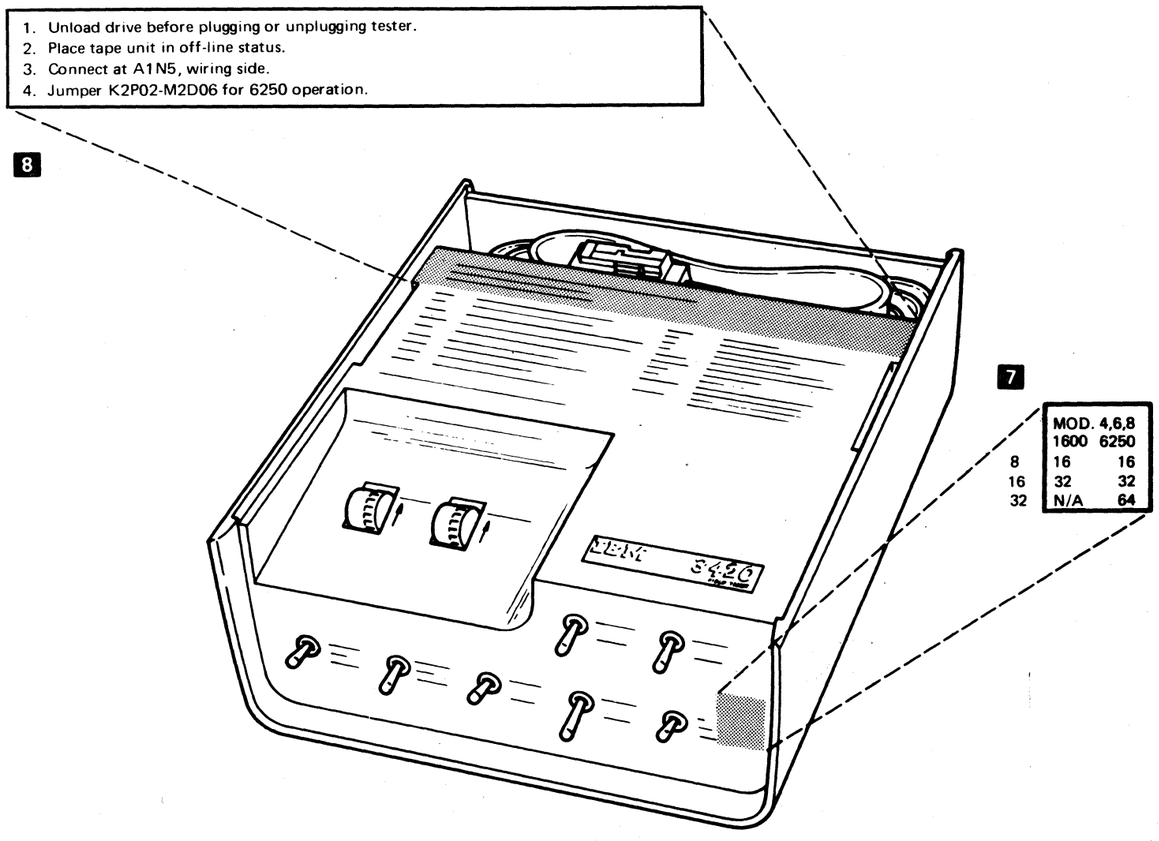
   Note: Simulate a Model 4, 6, or 8 by grounding N5B02 on the tape unit.
10. Mount and load a CE work tape. Then set the field tester to WRITE CONTINUOUS. See 80-020.
11. Scope test point A1H1B11 (–WRITE DATA TRACK P), at the tape unit. Observe a full write cycle period and compare to the chart below. Make sure the data rate switch is set correctly for the tape unit model being used.

    Note: Times are nominal and are given in microseconds. Tolerance is ±5%.

Model	Data Rate Switch Position			
	8	16	32	64
3	32.8	16.4	8.2	—
4	—	16.4	8.2	4.1
5	20.0	10.0	5.0	—
6	—	10.0	5.0	2.5
7	12.4	6.2	3.1	—
8	—	6.2	3.1	1.6

Note: Take any 3420 tape unit Incident Report (IR) and code your time, using Service Code 33, ECA #991.





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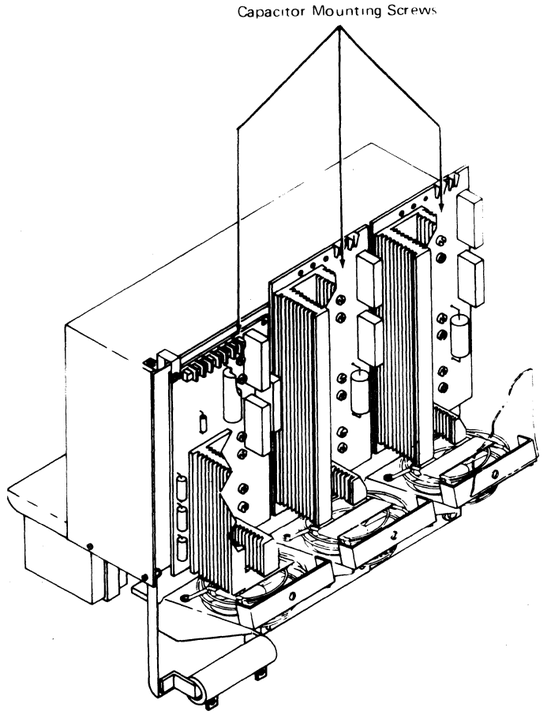
SECTION E. POWER SUPPLY CHECKS

E-1 Remove the wire seal from the 3420 tape unit J1 power connector, and the wire seal from around the 3803 Model 2 power plug.

E-2 With power off, check the 18 filter capacitor mounting screws on the 3803 Model 2 tape control's +6v and −4v power supplies. If loose, tighten the screws being careful not to over-torque and damage the power board. Also, check all other power supply screws and connections. (See 08-575.)



E-3 With power off, check that the customer's supply voltage matches that shown on the voltage rating label.

Note: To connect a 3803 tape control for operation at a different input voltage, refer to 3803 logic page YF010 (60 Hz) or YF015 (50 Hz).

See Page 08-570 to determine if each tape unit has a modified power supply. Then, refer to logic pages listed for the connections to be changed:

Frequency	Logic Pages Affected
(Model 3, 5, 7)	
60 Hz	YB010*, YB020#, YB030#
50 Hz	YB015*, YB025#, YB035#
(Model 4, 6, 8)	
60 Hz	Yf010*, YF020#, YF030#
50 Hz	YF015*, YF025#, YF035#

* For tape units with "Modified" power supplies.

\# For all tape units.

E-4 Customer Power Phasing

Check three-phase ac power receptacles to ensure proper motor rotation in each unit. Any improper phasing must be corrected before power is applied to the subsystem.

E-5 With power on, check that all blowers and motors operate correctly.

a. Incorrect phasing of input voltage causes the tape unit pneumatic supply motor to turn backward, preventing the tape unit from loading.

b. The cooling fan assembly blower motor in the tape unit will run backwards. Remove filter from machine and observe the direction of the fan as power is dropped. Fan should turn clockwise when viewed from below. (See arrow.)

Note: All blowers in the tape control are single phase.

E-6 Mount and load a tape. Using a Digital Voltmeter, part 453585, 453046, or equivalent, check that the +6 volt and −4 volt power supplies are within the tolerances listed:

3420 Tape Unit Models 3, 5, and 7:

	Test Point	Tolerance (Note 1)
+6v	A1G1E09-A1G2D08	±0.1v
-4.05v	A1N3D02-A1N3D08	±0.05v

3420 Tape Unit models 4, 6, and 8:

	Test Point	Tolerance (Note 1)
+6v	A1G2B11-A1G2D08	±0.1v
-4.05v	A1H1C09-A1G2D08	±0.05v

Note 1: Ripple specifications for −4v and +6v are 24 mv peak-to-peak. Measure at power supply. Refer to DC Logic page for your machine for TB locations. (YB020, YB025 or YF020, YF025)

3803 Tape Control

	Test Point	Tolerance (Note 2)
+6v	B2S2M11-B2S2D08	±0.01v
-4.0v	A2T4B06-A2T4D08	±0.01v

Note 2: Ripple specification for −4v is 80 mv peak-to-peak and for +6v is 10 mv peak-to-peak. Measure at power supply.

Caution: A ground loop has been purposely installed in the 3803 tape control for electro-static discharge (ESD) control. The installed ground loop is in the tape signal tail gate connector, and must be disassembled to check for other ground loops.
The tape control is checked at the factory for ground loops.

Special Power Requirements—3420 Model 8, 60 Hz Only

In certain 1x8 or 2x16 - 3420 configurations, which include the 3420 Model 8, a single 3803 **cannot** supply the power necessary for the operation of the subsystem without a special power feature. The table below shows the maximum number of tape units that may be powered from one 3803 without this special feature.

Number of 3420 Model 8's	Number of 3420 Model 7's	Number of 3420 Model 3-6
6	0	0
5	1	0
5	0	2
4	2	1
4	1	2
4	0	3
3	4	0
3	3	1
3	2	2
3	1	4
3	0	5
2	5	0
2	4	2
2	3	3
2	2	4
2	1	5
2	0	6
1	*	*

* If only one 3420 Model 8, then any combination of seven additional tape units is permissible.

If your customer's requirement exceeds the table, you must order SF9001 for the 3803(s). (For example, if he needs more than six Model 8s or two Model 8s and six Model 7s on a single 3803).

In all cases where this power supply feature is ordered, the customer must install a **100 Amp power source.**

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SECTION F. CHECKS AND ADJUSTMENTS

Note: Make sure the write head card is seated properly before continuing.

This section outlines checks, adjustments, and tests to ensure that the tape units and tape controls operate normally when the subsystem is turned over to the customer. See "Checks, Adjustments, Removals, and Replacements" sections of this manual for details.

F-1 Altitude Vacuum Level Setting—3420

Using a water manometer with a pressure divider; or a pressure/vacuum gauge, part 5495384, measure the vacuum according to the decal on the transfer valve. If incorrect:

a. 3420 Models 3 through 7:

Check that the vacuum pump belt and transfer valve plug are set as shown in 08-410.

b. 3420 Model 8 only:

Adjust vacuum line restrictor to obtain vacuum shown in 08-410.

F-2 Regulator Air Pressure—3420

Check/adjust pressure as shown in 08-405.

F-3 Capstan—3420

Caution: Allow fiber optics lamp to warm up 20 to 30 minutes before making adjustments.

Do capstan tach adjustment. See 08-130 for models 3, 5, 7 or 08-120 for models 4, 6, 8.

F-4 Mechanical Skew—3420

a. Visually check tracking before adjusting the skew plate. Perform procedure on page 08-150 or 08-160.

b. Check that mechanical skew meets the specifications given in 08-170 (1600 and 6250 bpi) or 08-180 (NRZI).

F-5 BOT/EOT—3420

Caution: Allow fiber optics lamp to warm up 20 to 30 minutes before making the adjustments.

Verify BOT/EOT adjustment. See 08-580.

F-6 Autocleaner Tape Direction—3420

Caution: Do not check autocleaner until tape unit has been positioned online, and just prior to returning machine to customer.

Check that autocleaner tape moves from bottom to top by marking tape and observing direction. See 08-380, "Autocleaner Operational Check".

F-7 ESD Grounding—3420 and 3803

Check that each door strike and roller assembly is adjusted correctly to ensure sufficient electro-static discharge (ESD) grounding.

3420 lower rear door (1).
3803 upper and lower on the front and rear doors (4).

This adjustment is accomplished as follows:

a. With the screws loose, adjust the roller assembly so the door roller will latch on the strike plate.

b. If necessary, adjust the plate mounted between the strike and frame to ensure proper grounding between the plate and finger stock assembly.

Note: Check that the door latching adjustment is still correct.

F-8 ESD Grounding—3803

a. Check the adjustment of the ESD plates on both the left and right sides. Be sure the plates are installed with the hem toward the inside of the machine.

Caution: Be sure that the plates are not adjusted to bow too much because the plates will reverse bow when the door is closed and lose proper grounding.

b. If necessary, adjust the plates so that each one bows out sufficiently to make contact with the hat section of the side cover.

c. Check the side door latch for a firm latching and adjust, if necessary.

F-9 Data Flow Clock Asymmetry Adjustment—3803

If the A1C2 card is replaced in the 3803, see ALD AA010 sheet 2 of 3, for adjustment procedure. (Originally factory adjusted.)

XJ1000 Seq 2 of 2	2736029 Part Number	See EC History	845958 1 Sep 79	846927 20 Jun 80				

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SECTION G. SYSTEM DIAGNOSTICS

Note: Make sure the write head card is seated properly before continuing.

G-1 Run 3420 OLTs A-K, M-X and AB through AG. (AB) through AG must be run under OLTSEP. AB is a diagnostic for 3803s with a device switching feature. AD through AG are optional for 3803s with the two-channel switch feature. (You must have a "dedicated" system to run diagnostics AB through AG.)

Note: OLT section 3420L will run only under sense switch setting (3420L/EXT=9). Verify PE clipping levels on machines with PE feature.

G-2 Verify serial numbers, EC levels, and features from the diagnostic printout.

a. If the tape control information is incorrect, see plugging chart on 90-210, or AA010 in the 3803 ALDs.

b. If the tape unit information is incorrect, see plugging chart on 90-210, and 90-212 or A6106 in the 3420 ALDs.

G-3 When the diagnostics have run error free, generate and save for future use a **read only** tape in 6250 bpi mode.

a. Enter the following as shown:

r 01,'DEVICE/3420A-G/fe,ext=z/'

b. To ensure that a good tape has been generated, the program must run without error. When a good tape has been generated, remove the write enable ring.

c. Mark this reel **6250 bpi READ ONLY** and save for diagnostic use with Section 00-010 of the MLMs.

Note: The CE should retain the output from Sections "V" and "W" of the OLTs which will give a printed table listing of all tape unit performance measurements.

EMULATOR: (If applicable to your machine.)

If the 3803 is attached to a System/360 on which any emulator is run, install a jumper on each tape unit to disable LOAD FAIL IRPT:

3420-3, 5, and 7, between A1H2U12 and A1H2U08

3420-4, 6, and 8, between A1M2U12 and A1M2U08

XJ1100 Seq 1 of 2	2736030 Part Number	See EC History	845958 1 Sep 79	846927 20 Jun 80	847298 15 Aug 83			

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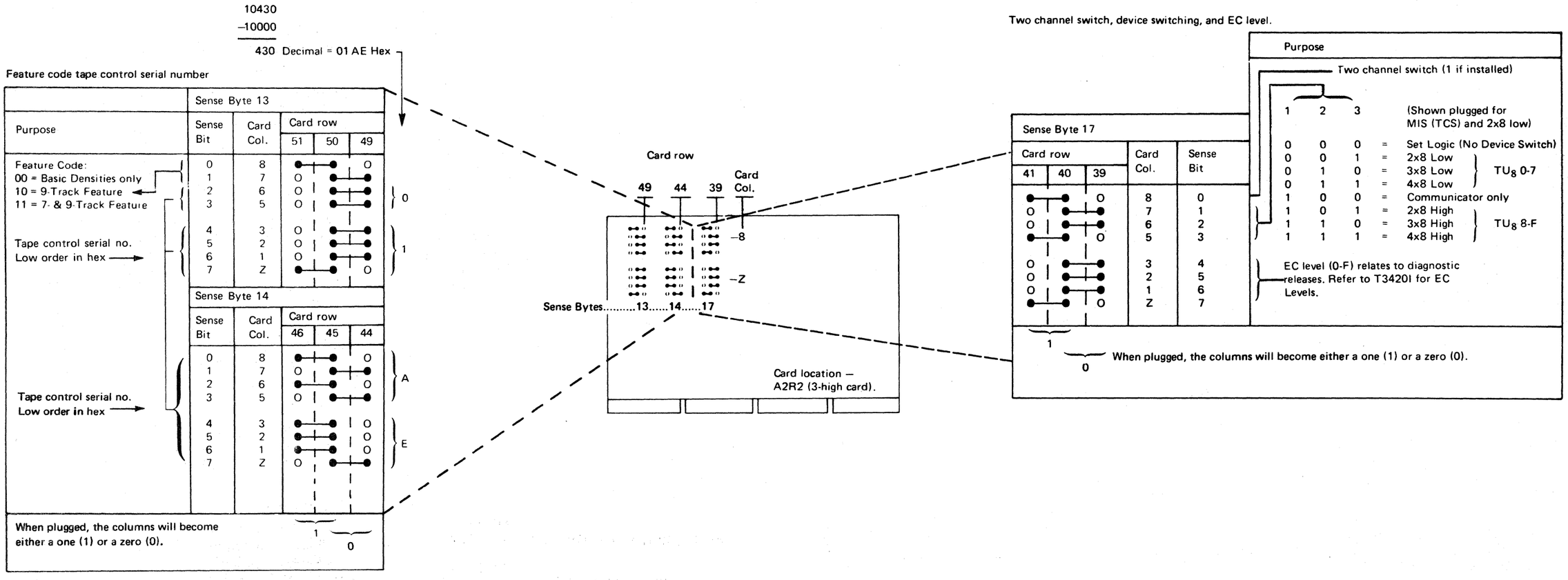
SECTION G. SYSTEM DIAGNOSTICS (Cont'd)

G-4 Tape Control Serial Number/EC Level/Feature Code: Verify from diagnostic printout that factory plugging is correct when diagnostics are run.

Plugging example: tape control serial number is 10430, with 9-track feature.



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SECTION G. SYSTEM DIAGNOSTICS (Cont'd)

G-5 Tape Unit Serial Number/Model Number/EC Level/ Feature Code: Verify from diagnostic printout that factory plugging is correct on all tape units when diagnostics are run (3420) ALD A6106.

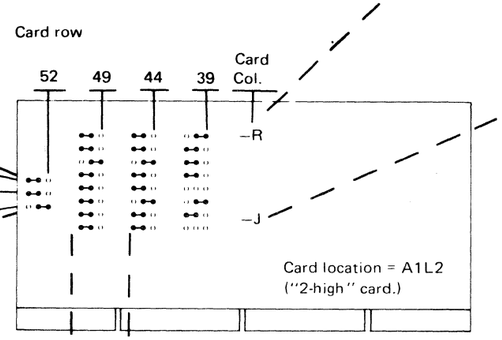
Tape Model	Alpha
Model 3	A, B, P
Model 5	C, D, Q
Model 7	E, F, R
Model 4	G, H, S
Model 6	J, K, T
Model 8	M, N, U

Plugging example: Wired for model 4.

Original model number (Models 4,6, and 8) (See Notes)

Original Model No.	Card Col.	Card row 54	53	52
L M N – Card Col. 0 1 0 – Model 3 0 1 1 – Model 4 1 0 0 – Model 5 1 0 1 – Model 6 1 1 0 – Model 7 1 1 1 – Model 8	N M L			O O ●
When plugged, the columns will become either a one (1) or a zero (0).		1		0

90-99XXX machines plug for model of tape unit.



Plugging example: Wired for EC734801 and feature code 6250/1600 bpi.

EC Level/Feature Code

Card row 41	40	39	Card Col.	Purpose
				EC Level
O	●	●	R	N P Q R Card Col. (Ref.)
●	●	O	Q	1 1 1 1 = EC No. 734776
●	●	O	P	0 0 0 1 = EC No. 734801
●	●	O	N	0 0 0 0 = EC No. 735810 or higher
O	O	O		Feature Code
O	●	●	L	K L = Card Column (Ref.)
●	●	O	K	0 0 = Basic Densities 6250 only
				0 1 = 6250/1600 bpi
0				
1				
1				
0				

When plugged, the columns will become either a one (1) or a zero (0).

Tape Unit Serial Number

Card row 46	45	44	Example Values	Plug Valve	Card Col.
●	●	O		1	R
●	●	O		2	Q
O	●	●	4	4	P
●	●	O		8	N
●	●	O		16	M
O	●	●	32	32	L
●	●	O		64	K
●	●	O		128	J

Card row 51	50	49	Example Values	Plug Value	Card Col.
●	●	O		256	R
●	●	O		512	Q
O	●	●	1024	1024	P
●	●	O		2048	N
●	●	O		4096	M
●	●	O		8192	L
●	●	O		16384	K
●	●	O		32768	J
			1060		

To plug serial number: Plug pins to equal the last four digits of the serial number using chart at left.

Plugging example: Tape unit serial number is 81060.

Plug positions to give a sum of 1060.

Notes:

[1] The original model number is the high-order digit or alpha character in the serial number, and is not changed with model conversion. See table to convert alpha to model type.

[2] For tape units with a high order digit in the serial number, other than 3 through 8, the diagnostic will print the original model number as the high order digit of the serial number.

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NOTES:

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90-213

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