IBM Maintenance Library

3705-80 Communications Controller
Theory-Maintenance
Volume III

SY27-0209-1

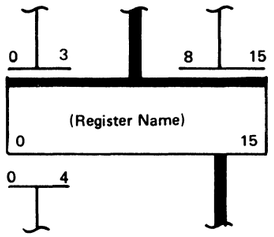
Abbreviations

A	And circuit or ampere
AA	automatic answering
ABAR	attachment buffer address register
ABO	adapter bus out (register)
ac	alternating current
ACO	automatic call originate
ACF/NCP/ VS	Advanced Communications Function for Network Control Program/Virtual Storage
ACR	abandm call and retry
ACU	automatic calling unit
adr	address
AEQ	automatic equalizer
AHR	add halfword register (instruction)
ALD	automated logic diagram
ALU	arithmetic logic unit
AMP	amplifier
APAR	authorized program analysis report
AR	add register (instruction)
ARI	add register immediate (instruction)
B	branch (instruction)
BAL	branch and link (instruction)
BALR	branch and link register (instruction)
BAR	buffer address register
BB	branch on bit (instruction)
BC	bit clock
BCB	bit control block
BCC	bit clock control
BCL	branch on C latch (instruction)
BCT	branch on count (instruction)
BO	bus out
BP	break point
bps	bit per second
BSC	binary synchronous communication
BSM	bridge storage module
BZL	branch on Z latch (instruction)
CA	channel adapter
CACHKR	channel adapter check register
CACR	channel adapter control register
CADB	channel adapter data buffer
CAMR	channel adapter mode register
CASNSR	channel adapter sense register
CASTR	channel adapter status register
CB	circuit breaker
CBAR	CSB buffer address register
CCB	character control block
CCR	compare character register (instruction)
CCT	coupler cut through (modem)
CCU	central control unit
CD	carrier detect
CDS	configuration data set
CE	Channel End (status)
chan	channel
char	character
CHR	compare halfword register (instruction)
ck	check
clk	clock
cm	centimeter
CMDR	channel adapter command register
CMND	command
com	common
COS	Call Originate Status
CP	circuit protector
CPU	central processing unit
CR	compare register (instruction)
CRC	cyclic redundancy check
CRI	compare register immediate (instruction)
CRQ	Call Request
CS	cycle steal
CSAR	cycle steal address register
CSB	communication scanner base
CSCD	clear to send, carrier detect
CSMC	cycle steal message counter
ctrl	control
CTS	Clear To Send
CUE	Control Unit End (status)
CW	control word
CWAR	control word address register
CWCNTR	control word byte count register
DAA	data access arrangement
DA	data modem ready
dB	decibel
DBAR	diagnostic buffer address register
dc	direct current
DCE	data circuit-terminating equipment
DCM	diagnostic control monitor
DCR	data channel ready
DE	Device End (status)
DET	detector
diag	diagnostic
dist	distance
DLO	data line occupied
DOS	Disk Operating System
DPR	digit present
DR	display register or data ring (modem)
DCS	distant station connect (ACO only)
DSR	data set ready
DT	data tip (modem)
DTE	data terminal equipment
DTR	data terminal ready
EC	edge connector
EB	extended buffer
ECP	emulation control program
EIA	Electronic Industries Association
enbl	enable
EON	end of number (ACO only)
EPO	emergency power off
ESC	emulation subchannel
EXT	external
FCS	final control sequence
FET	field effect transistor modem card
FETOM	Field Engineering Theory of Operation Manual
FF	flip flop
FL	flip latch
FRU	field replaceable unit
GB	ground bus
gnd	ground
grp	group
hex	hexadecimal
Hlfwd	halfword
horz	horizontal
HS	heat sink
Hz	Hertz
I	instruction (cycle)
IAR	instruction address register
IC	insert character (instruction)
ICS	initial control sequence
ICT	insert character and count (instruction)
ICW	interface control word
IFT	internal functional test
IN	input (instruction)
INCWAR	inbound control word address register
Init	initial
int	internal
intf	interface
I/O	input/output
IPL	initial program load
IR	interrupt remember
irpt	interrupt
ISACR	initial selection address and command register
L	load (instruction)
LA	load address (instruction)
LAR	lagging address register
LCD	line code definer
LCOR	load character with offset register (instruction)
LCR	load character register (instruction)
LED	light emitting diode
LGF	leading graphics flag
LH	load halfword (instruction)
LHOR	load halfword with offset register (instruction)
LHR	load halfword register (instruction)
LIB	line interface base
lim	limiter
LOR	load with offset register (instruction)
LOSC	last oscillator sample condition
LR	load register (instruction)
LRI	load register immediate (instruction)
LS or ls	local store
lt	latch
L1	level 1
L2	level 2
L3	level 3
L4	level 4
L5	level 5
mA	milliampere
Mem TB	memory terminal board
modem	modulator/demodulator
ms/divn	milliseconds per division
MST	monolithic system technology
mV	millivolt
NB	Digit Signal
N/C	normally closed
NCP	network control program
NCR	and character register (instruction)
NHR	and halfword register (instruction)
N/O	normally open
NR	and register (instruction)
NRI	and register immediate (instruction)
NRZI	non-return-to-zero inverted
ns	nanoseconds
NSC	native subchannel
OBR	outboard recorder
O/C	overcurrent
OCR	or character register (instruction)
OE	exclusive or
OH	off hook (modem)
OHR	or halfword register (instruction)
OLT	on line test
OLTEP	on line test executive program
OLTLIB	on line test library
OLTSEP	on line test standalone executive program
op	operation
op reg	operation register
OR	or register (instruction)
ORI	or register immediate (instruction)
OS	Operating System
OSC	oscillator
OUT	output (instruction)
OUTCWAR	outbound control word address register
OVRN	overrun
O/V	overvoltage
P	parity
PC	parity check
PCF	primary control field
PCI	program controlled interrupt
PDF	parallel data field
PEP	partitioned emulation programming
PG	parity generation
pgm	program
PH	polarity hold
PND	Present Next Digit
P/N	part number
POR	power on reset
pos	position

POSC	present oscillator sample condition
pot	potentiometer
P-P	post processor modem card
PPB	prime power box
PUT	programmable unijunction transistor
PWI	power indicator
R	resistance or resistor
rcv	receive
rd	read
rdy	ready
RE	register and external register (instructions)
ref	reference
reg	register
regen	regenerative
req	request
RI	register immediate (instruction) or ring indicator (modem)
RLSD	receive line signal detector
RMS	root mean square
ROS	read-only storage
RPL	remote program loader
RR	register to register (instructions)
RS	register to storage (instructions)
RSA	register and storage with addition (instructions)
RT	register branch or register and branch (instructions)
RTS	Request To Send
rly	relay
SAR	storage address register
SCF	secondary control field
SCR	silicon controlled rectifier or subtract character register (instruction)
SCRID	silicon controlled rectifier indicator driver
SDF	serial data field
SDLC	synchronous data link control
SDR	storage data register
sec	second
sel	selection
SEP	separator (ACO only)
seq	sequence
SG	signal ground
SH	switch hook (modem)
SHR	subtract halfword register (instruction)
SIG	signal
SIO	start I/O
SMS	standard modular system
SR	subtract register (instruction)
SRI	subtract register immediate (instruction)
SRL	Systems Reference Library
S/S	start/stop
ST	store (instruction)
STC	store character (instruction)
STCT	store character and count (instruction)
STH	store halfword (instruction)
stk	stacked
svc	service
sw	switch
SYN	synchronous idle
sync	synchronization or synchronous
TAR	temporary address register
TB	terminal board
TIC	Transfer In Channel
tr	trigger
TRM	test register under mask (instruction)
TSL	Technical Service Letter
T2	test 2
T3	test 3
T4	test 4
UC	Unit Check (status)
UE	Unit Exception (status)
V	volts
V/divn	volts per division
wd	word
wr	write
XCR	exclusive-or character register (instruction)
xfer	transfer
xfmr	transformer
XHR	exclusive-or halfword register (instruction)
xmt	transmit
XR	exclusive-or register (instruction)
XRI	exclusive-or register immediate (instruction)
2W	two-wire line connection (implies half-duplex)
4W	four-wire line connection (implies duplex, but actual duplex depends on the line set type and telephone company equipment).

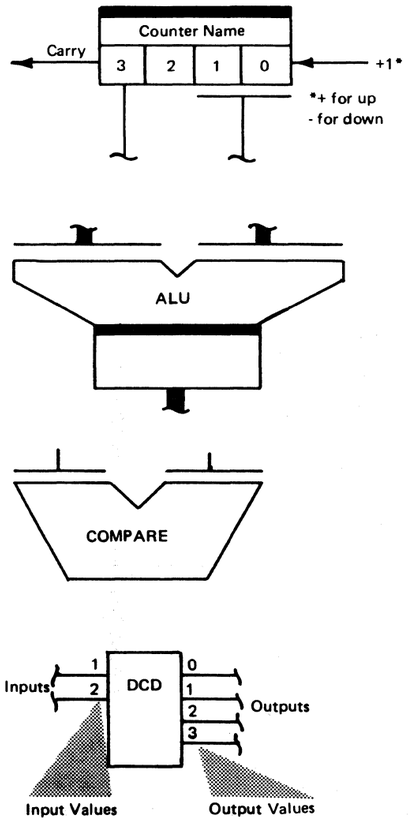
Legend
(Part 1 of 2)

1. Logic Diagrams



Register

The input side is denoted by a thick line. A partial transfer of contents is shown by numbered input and/or output lines.



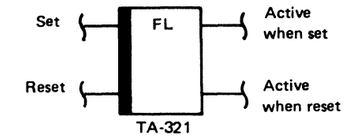
Counter

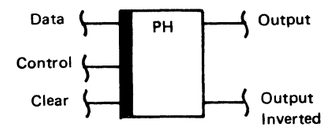
ALU

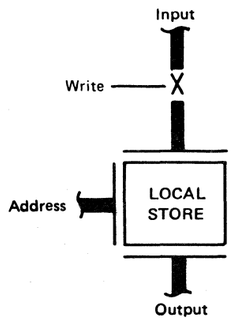
Compare

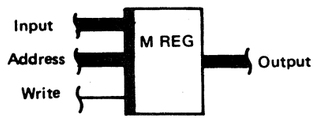
Decode

The active output is the output whose output value equals the sum of the active input values.









Flip Latch

Input side is denoted by a thick line. ALD reference page may be shown beneath.

Polarity Hold

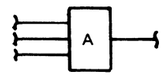
The 'output' of the polarity hold block is at the indicated polarity when both the 'data' and the 'control' lines go to their indicated polarity. When the 'control' line goes to the polarity opposite to that indicated, the 'output' line holds at the polarity it is at. When the 'clear' line goes to its indicated polarity, the 'output' line goes to the polarity opposite to that indicated.

Local Store

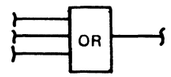
Read---Output from the local store addressed. Contents of local store is not destroyed.
Write---Input contents stored in the local store addressed when 'write' is active.

M REG

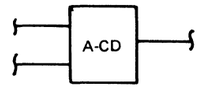
See Local Store



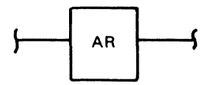
AND



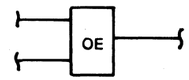
OR



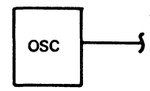
AND Current Driver



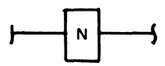
Amplifier



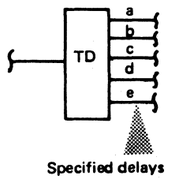
Exclusive OR



Oscillator



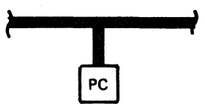
Negator (Inverter)



Time Delay

An input pulse starts the time delay. Each output pulse has the same duration as the input pulse but is delayed by the specified amount.

Legend
(Part 2 of 2)

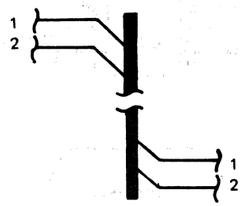


Parity Check

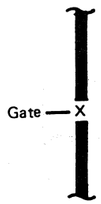
Parity check on the data bus

Parity Generate

Parity generated on the data bus



Multiple Line Transfer

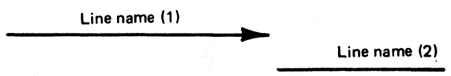


Gated Bus

Gate must be active for data to flow on bus.

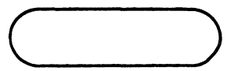
Test Point

Signal that may be scoped.



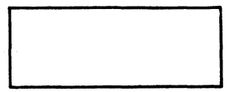
Above symbol indicates change in line name.

2. Flowcharts



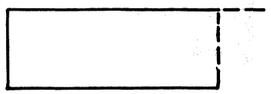
Terminal

Indicates the beginning or end of the event.



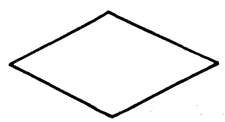
Process

Indicates a major function or event.



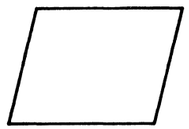
Annotation

Gives descriptive comment or explanatory note.



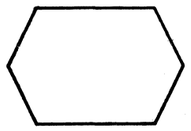
Decision

Indicates a point in a flowchart where a branch to an alternate path is possible.



Input-Output

CCU executes the control program input/output instructions.

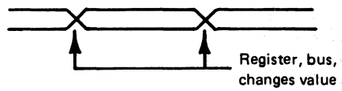


Hardware Process

Type 2 scanner hardware action resulting from input/output instructions or signals from the line/autocall interface.

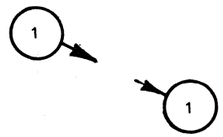
3. Timing Charts

Numerals at the beginning and end of the bar identify the signal(s) (also on the same chart) that activate and deactivate this line. '(Not)' with the number indicates that lack of the signal conditions the line.



Register, bus, or local store content changes value at these points.

4. General



On-page Connector

Indicates a connection between two parts of the same page. The arrow leaving the symbol points (line-of-sight) to a correspondingly-numbered symbol.

Off-page Connector

Indicates a connection between diagrams located on separate pages. The location of the correspondingly-lettered symbol is shown adjacent the symbol.

CONTENTS-VOLUME 3

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power AC and DC when removing or assembling major components, working in immediate area of power supplies, performing mechanical inspection of power supplies and installing changes in machine circuitry.
3. Wall box power switch when turned off should be locked or tagged in off position. "Do not Operate" tags, form 229-1266, affixed when applicable. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuity anywhere in the machine, the following precautions must be followed.
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Rings, wrist watches, chains, bracelets, metal cuff links, shall not be worn.
   c. Only insulated pliers and screwdrivers shall be used.
   d. Keep one hand in pocket.
   e. When using test instruments be certain controls are set correctly and proper capacity, insulated probes are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc. – use suitable rubber mats purchased locally if necessary).
5. Safety Glasses must be worn when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Parts cleaning, using solvents, sprays, cleaners, chemicals, etc.
   f. All other conditions that may be hazardous to your eyes. REMEMBER, THEY ARE YOUR EYES.
6. Special safety instructions such as handling Cathode Ray Tubes and extreme high voltages, must be followed as outlined in CEM's and Safety Section of the Maintenance Manuals.
7. Do not use solvents, chemicals, greases or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles—this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. All safety devices such as guards, shields, signs, ground wires, etc. shall be restored after maintenance.
12. Each Customer Engineer is responsible to be certain that no action on his part renders product unsafe or exposes hazards to customer personnel.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. All machine covers must be in place before machine is returned to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it (i.e., under desk or table).
16. Avoid touching mechanical moving parts (i.e., when lubricating, checking for play, etc.).
17. When using stroboscope—do not touch ANYTHING—it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CE's and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

KNOWING SAFETY RULES IS NOT ENOUGH
AN UNSAFE ACT WILL INEVITABLY LEAD TO AN ACCIDENT
USE GOOD JUDGMENT – ELIMINATE UNSAFE ACTS

229-1264-1

Artificial Respiration
GENERAL CONSIDERATIONS

1. **Start Immediately, Seconds Count**
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim or apply stimulants.
2. **Check Mouth for Obstructions**
   Remove foreign objects—Pull tongue forward.
3. **Loosen Clothing—Keep Warm**
   Take care of these items after victim is breathing by himself or when help is available.
4. **Remain in Position**
   After victim revives, be ready to resume respiration if necessary.
5. **Call a Doctor**
   Have someone summon medical aid.
6. **Don't Give Up**
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults
Victim on His Back Immediately

1. **Clear throat** of water, food, or foreign matter.
2. **Tilt head back** to open air passage.
3. **Lift jaw up** to keep tongue out of air passage.
4. **Pinch nostrils** to prevent air leakage when you blow.
5. **Blow** until you see chest rise.
6. **Remove your lips** and allow lungs to empty.
7. **Listen** for snoring and gurglings, signs of throat obstruction.
8. **Repeat mouth to mouth breathings** 10-20 times a minute.

Continue rescue breathing until he breathes for himself.

NO

Thumb and finger positions

Final mouth to mouth position

Reprint Courtesy Mine Safety Appliances Co.

LOCATION OF LOGIC PAGES BY VOLUME NUMBER

Volume	Logic Pages	Contents
41	YZ	Power supply-installation instruction
42	AA–CV	CCU
A42	CW–CZ	ROS-Type 2 attachment base–CCU
43	DF–DZ	CCU
44	MM	Storage
45	TA–TB	Type 2 scanner
46	VA	LIB-reference material
47	VB	LIB-line sets 1, 2, 3, 4, 5, 8, and 9
48	RA–RS	Type 1 channel adapter
A48	PA–PS	Type 4 channel adapter
49	GA–GC	Remote Program Loader Diskette Controller

Type 1 Channel Adapter

INTRODUCTION

The type 1 channel adapter (CA) handles data transfers between the 3705-80 and the channel with the CCU interrupt facilities. This adapter accepts a range of subchannel addresses and commands consistent with the IBM 2701, IBM 2702, and IBM 2703 transmission control units. However, the 3705-80 must be assigned a single subchannel address to be used when the 3705-80 is not emulating one of the other transmission control units.

The range of subchannel addresses and commands enables the 3705-80 to emulate the other IBM control units under program control.

The type 1 channel adapter does not cycle steal data into storage. This adapter requires control program intervention for each inbound and outbound data transfer.

Data transfers between the channel and the channel adapter are controlled by the data-status control register. Up to four bytes can be transferred (byte count in status control register) before the control program intervenes in the operation. However, each 4 byte transfer requires control program intervention before and after the transfer.

Channel Adapter Modes of Operation

The type 1 channel adapter operates in either native subchannel (NSC) or emulation subchannel (ESC) mode. The 3705-80 control program selects the mode with an Output X'67' instruction (see 8-130). NSC mode uses a single channel address for each channel interface installed, and must be used in the initial program load. The 3705-80 control program handles line control and message assembly while operating in this mode.

ESC mode uses a range of addresses assigned to each communication line attached to the 3705-80. The host processor is responsible for line control while operating in this mode. ESC mode is used when IBM 2701, 2702, or 2703 operation is emulated.

Address Assignment

During initial selection, the channel adapter must be able to recognize the I/O device address presented on the channel bus-out if the channel interface is enabled. Since the type 1 CA can have a NSC address and a range of ESC addresses, alternate means of assigning the addresses are provided.

The NSC address is assigned on the plug card at Y4P2, RC104. The NSC address can be any address from 0 to 255. If the Two Channel Switch feature is installed, NSC addresses for interface A and B are assigned by different plug cards (A on Y4P2, B on Y4R2, RF106, Y4P2 is an address source for the control program). The 2 NSC addresses need not be identical.

ESC addresses are assigned on the plug card at Y4M2, RC302-305, and are a contiguous group of addresses. The lowest address in the group can be 0 or any multiple of 16 from 0 to 240. The highest address that can be assigned must be greater than the lowest address and 1 less than an even multiple of 4 from 3 to 255. The range of addresses can be set to include a minimum of 4 and a maximum of 256 addresses. The range of addresses must be the same for both interfaces if the Two Channel Switch feature is installed.

Refer to FEALD YZ000 pages 10-13 for I/O channel address jumpering.

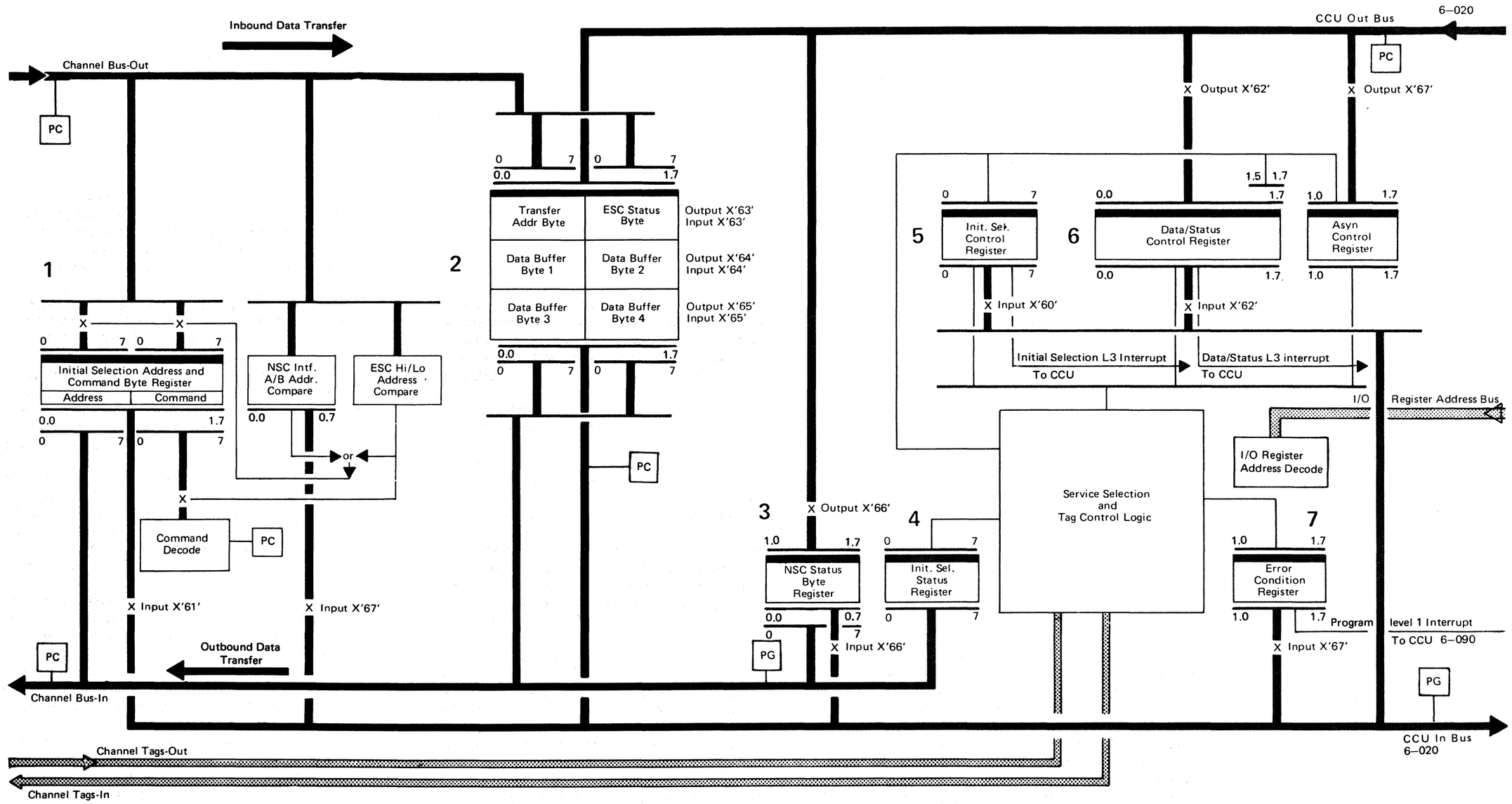
WARNING

The hard stop latch disables the channel interface without extinguishing the interface enabled light. The channel adapter does not recognize its address and trap select out if the hard stop latch is set.

Channel Commands

The type 1 channel adapter initially accepts as a valid command any configuration from X'00' to X'FF'. The only limitation is that the command byte must be in parity on the channel. The channel adapter presents an initial status of X'00' if the parity is correct and the command is not a No-Op, an ESC Test I/O, or a Start I/O clearing NSC stacked status. The CA then requests an initial selection level 3 interrupt so that the control program can further determine if the command is valid for the subchannel address the command was issued to. If the command is not valid for that address (determined by the control program), the CA presents CE, DE, and UC status to the channel under program control.

TYPE 1 CA DATA FLOW (PART 1 OF 2)



TYPE 1 CA DATA FLOW (PART 2 OF 2)

1 Initial Selection Address and Command Register

This register contains the I/O device address byte and command byte presented to the channel adapter during initial selection. The register can be accessed by Input X'61' which should be executed only if the type 1 channel adapter initial or data/status level 3 interrupt request is set. See 8-070 for Input X'61' description. This register is referred to as the SIO register in the ALD's.

2 Local Store

The local store provides buffering for the I/O address byte used in all data and status transfer sequences initiated by the 3705-80. Buffering for up to four bytes of data for inbound and outbound data transfers is provided here also.

The control program loads or accesses the I/O device address and the emulation status byte with Output X'63' and Input X'63' respectively. The data bytes are transferred with X'64' or X'65' instructions, see chart below.

Data Byte	*Data Transfer*	
	Out	*In*
1	X'64'	X'64'
2	X'64'	X'64'
3	X'65'	X'65'
4	X'65'	X'65'

3 NSC Status Byte Register

The current status of the NSC is maintained in this register and gated over the channel interface during NSC status transfer sequences. The control program should set the NSC status by executing an Output X'66' instruction. The control program has access to this register with the Input X'66' instruction.

4 Initial Selection Status Register

The status byte is generated and presented to the channel from this register during initial selection sequences except under the following conditions.

- An initial selection sequence occurs for the native mode subchannel before the NSC status byte provided by the control program has been accepted. The NSC status byte from the NSC status register is presented instead of the hardware generated status.
- An initial selection sequence occurs for an emulation address when the control program has signaled that an ESC status transfer sequence is required and has signaled that ESC Test I/O status is available. The ESC status byte provided by the program is presented instead of hardware generated status.

5 Initial Selection Control Register

The information in this register identifies the event causing the type 1 channel adapter initial level 3 interrupt request to be set. The register can be accessed by Input X'60', which should be executed only if the interrupt request is set.

6 Data/Status Control Register

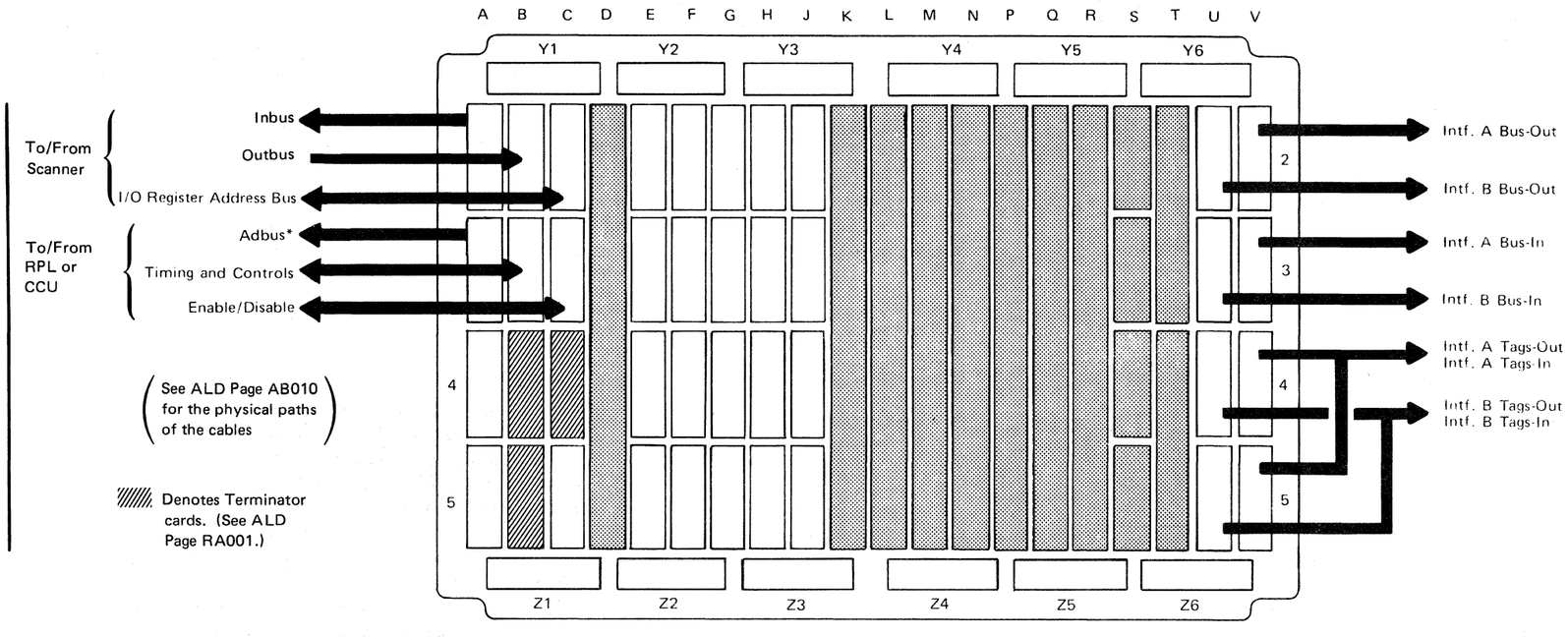
The information in this register controls and identifies events that cause the type 1 channel adapter data/status level 3 interrupt request to be set. The register can be accessed by Input X'62', which should be executed only if the interrupt request is set. The control program can perform various control functions by setting or resetting bits in this register with an Output X'62' instruction. The instruction should be executed only when the control program is servicing a type 1 CA level 3 interrupt request.

7 Error/Condition Register

The error/condition register is a collection of latches that are set when the CA detects an error or an occurrence of specific asynchronous conditions. The 3705-80 control program has access to this register with an Input X'67' instruction, (see page 8-140). The errors indicated by the error/condition register cause type 1 CA error interrupts (see page 8-360).

CARD FUNCTIONS AND LOCATIONS

Card Loc.	ALD Page	Function
A4D2	RA101	I/O Decodes (Type 1 Scanner and CA) I/O Feedback L1 Bid Basic Clocking **Inbus Doting** **Inbus Gating**
A4P2	RC101	Chan. Intf. Tags and Control Chan Intf A Receivers Intf. A control **Channel Address Jumper** Channel Address Parity Check Local Store Assembler Byte 0 Local Store Byte 0 Intf B Address
A4N2	RC201	Tag Control Clock Tag Control, Start I/O and Op-In Tag Control Tag In latches Tag Control stack chaining stop or Halt I/O Tag Control Enable and Sel. Sys Reset Tag Control Powering
A4M2	RC301	Bus-Out Repowering Low Address Jumpering Low Address Logic High Address Jumpering High Address Logic Start I/O and Command Registers Local Store Byte 1 Command Decode Outbus Inversion
A4L2	RC401	**Outbus Termination** Initial Selection Control Service Transfer Control Byte Count Initial Status Generation
AAK2	RC501	Input/Output Control Assembler and Local Store control Asynchronous Interrupt control NSC Control RN Asynchronous Information Error Latches
A4T2	RC601	NSC Status Register Asynchronous Interrupt Control
A4T4	RC801 RC802	Interface A Select Out Relay Interface B Select Out Relay
A4Q2	RC701	Bus-In Drivers Intf. A Tag-In Drivers Intf. A Select Out Relay Driver and Control gates Bus-In Error Latch
A4R2	RF101	Intf. B Receivers
A4S2	RF201	**Bus-In Drivers, Intf. B** **Tag-In Drivers Intf. B** **Select Out Relay and Control Gates** **Bus In Error Latch**



01A-A4 Board
CARD SIDE

*The Adbus is not used with the type 1 CA

INPUT AND OUTPUT INSTRUCTIONS

The type 1 channel adapter relies on the 3705-80 control program to use input and output instructions to control data transfers. The control program initiates channel data and status transfers, and transfers data between the CA and the CCU with input and output instructions.

Each input or output instruction addresses an external register. The input instructions gate the external register to CCU general registers via the CCU Inbus. Output instructions gate CCU general registers to CA registers via the CCU Outbus. The 'I/O register address bus' is decoded in the type 1 attachment base.

Executing an Input or Output X'60', X'61', X'62', X'63', X'64', X'65', or X'66' when the CA is actively handling a data or status transfer sequence causes an in/out check to occur; see 8-360.

Control Panel Access to CA Registers

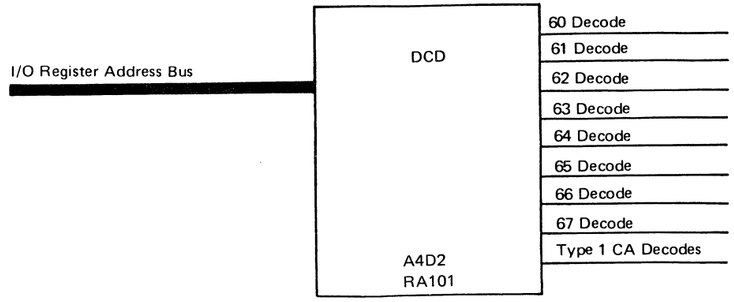
Type 1 CA registers X'60' through X'66' should be accessed from the control panel with Input or Output instructions only when either of the type 1 CA level 3 interrupts are pending.

To ensure that this interrupt remains pending, the 3705-80 should be in either Program Stop or Hard Stop mode before these instructions are executed from the control panel.

If these conditions are not met, the following occurs:

1. If the type 1 CA is in the process of a data or status transfer sequence and an Input or Output X'60' through X'66' is initiated from the control panel, the type 1 CA hardware:
   a. Causes a type 1 CA level 1 interrupt request.
   b. Sets the type 1 CA In/Out instruction accept latch.
   c. Gates X'0000' onto the CCU Inbus to be displayed in display B if the instruction is an Input.
   d. Does not recognize Output instructions.
2. If the type 1 CA is not transferring data or status and a type 1 CA level 3 interrupt request is not pending, one of the following occurs:
   a. For Input X'60', X'61', or X'66' instructions, either the instruction is executed without error or, if at the same time the instruction is being executed, the CA is being selected by the host processor channel, the CCU may sample invalid data from the type 1 CA. The data in display B should be considered invalid.
   b. For Output X'66' instructions, either the instruction is executed without error or, if at the same time the instruction is being executed, the type 1 CA is being selected by the host processor channel, a type 1 CA channel bus in check and a type 1 CA level 1 interrupt request may be set or a processor data check may be detected at the host processor.
3. If the type 1 CA is in the process of presenting ESC status to a Test I/O issued to an ESC address, and an Input X'60' through X'66' or an Output X'62' through X'66' is executed, one of the following occur:
   a. The instruction executes without error.
   b. If at the same time any of these instructions are being executed, the type 1 CA is being selected by the host processor channel, either a type 1 channel bus in check, a type 1 CA local store, a level 1 interrupt request, or a processor data check may occur.

Input and Output X'67' can be executed from the 3705-80 control panel without causing an error.

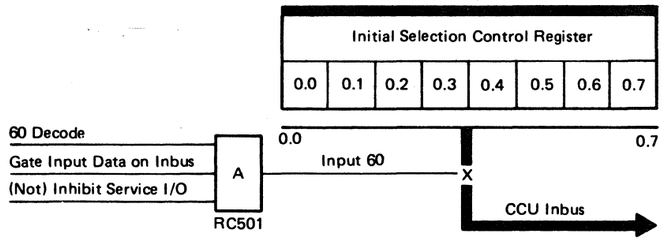


I/O Reg Bus Bits							
1	2	3	4	5	6	7	Decode
1	1	0	0	0	0	0	60
1	1	0	0	0	0	1	61
1	1	0	0	0	1	0	62
1	1	0	0	0	1	1	63
1	1	0	0	1	0	0	64
1	1	0	0	1	0	1	65
1	1	0	0	1	1	0	66
1	1	0	0	1	1	1	67

Input X'60' Instruction

Input X'60' transfers the contents of the initial selection control register into a CCU general register. The 3705-80 control program uses this instruction to determine the exact cause of a type 1 CA initial selection level 3 interrupt.

An Output X'60' resets the initial selection control register and the L3 interrupt request resulting from the initial selection.



Bit	*Logic Page*	*Function*
0.0	RC402	Input Initial Selection State*
0.1	RC205	Input Initial Interface Disconnect
0.2	RC205	Input Initial Selective Reset
0.3	RC402	Input Initial Bus Out Check
0.4		0
0.5	RC402	Input Stack Initial
0.6	RC505	NSC Status Cleared
0.7	RC205	Input System Reset

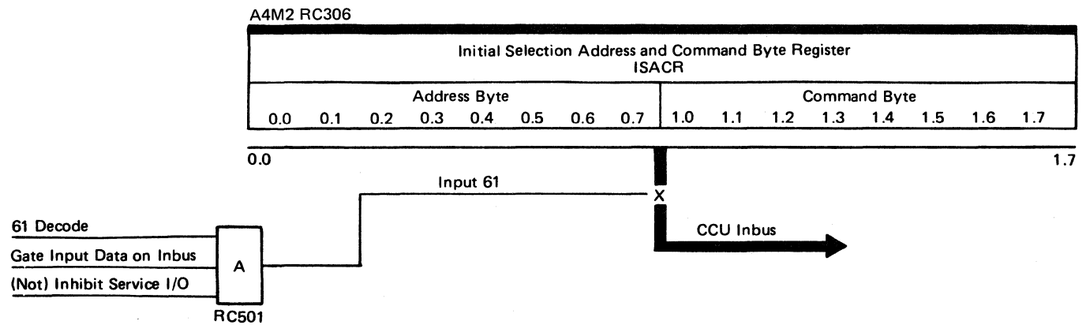
*Normal Initial Selective

Input X'61' Instruction

Input X'61' transfers the contents of the initial selection address and command byte register into a CCU general register. During an initial selection sequence, a type 1 CA initial selection level 3 interrupt is requested, and the 3705-80 control program must investigate the subchannel address and command causing the interrupt. Byte 0 is the address to which the command in byte 1 was issued.

The 3705-80 control program must store the address and command because the host processor can send the CA a new command before the 3705-80 control program has completed the previous one when in ESC mode. The 3705-80 control program must also control the CA action for each command.

An Output X'61' instruction has no effect on the channel adapter.



Output X'62' Instruction

This instruction initiates inbound and outbound data transfers and status presentations. The 3705-80 control program uses this instruction to control CA action and to specify the number of bytes of data to transfer across the channel interface on a channel data transfer.

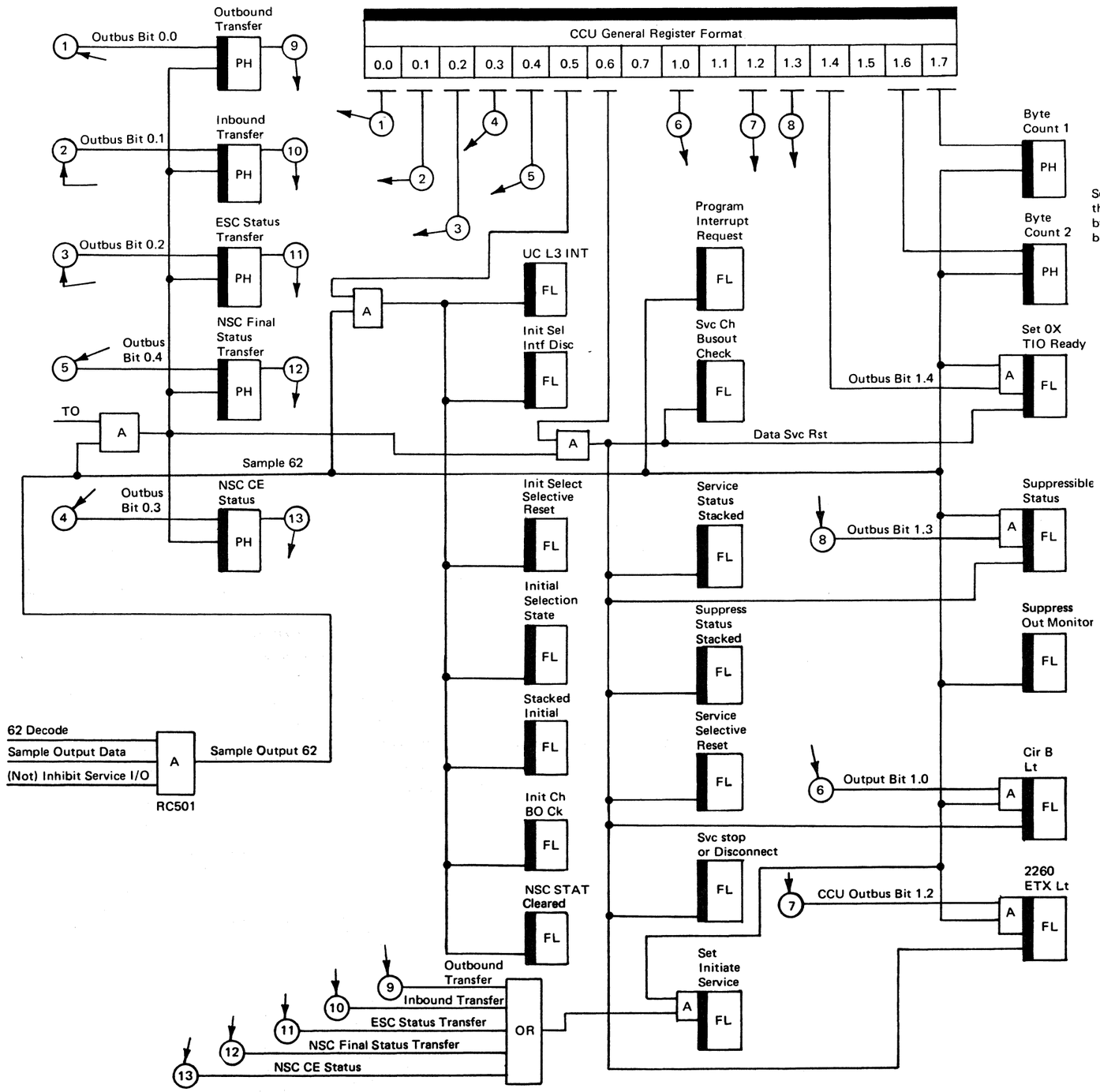
Byte Count	*Bits*		
	1.5	*1.6*	*1.7*
1	0	0	1
2	0	1	0
3	0	1	1
4	X	0	0

X This bit may be on or off for a byte count of four.

Summary of Output X'62' bit definitions and ALD locations

Bit	*Card Location*	*ALD Page*	*Function*
0.0*	A4L2	RC403	1 = set; 0 = rst outbound transfer
0.1*	A4L2	RC403	1 = set; 0 = rst inbound transfer
0.2*	A4L2	RC403	1 = set; 0 = rst ESC status transfer
0.3*	A4L2	RC403	1 = set; 0 = rst NSC channel end status
0.4*	A4L2	RC403	1 = set; 0 = rst NSC final status transfer
0.5	A4K2	RC503	Reset NSC status cleared
	A4L2	RC402	Reset initial channel bus out check
	A4L2	RC402	Reset stacked initial
	A4L2	RC402	Reset initial selection state
	A4L2	RC402	Reset Unit Check L3 interrupt
	A4N2	RC205	Reset initial selection interface disconnect
	A4N2	RC205	Reset initial selection selective reset
0.6	A4K2	RC504	Reset monitor for 2260 ETX
	A4K2	RC504	Reset monitor for circle B
	A4L2	RC406	Reset 0X TIO ready
	A4L2	RC405	Reset service channel bus-out check
	A4L2	RC405	Reset service status stack
	A4N2	RC204	Reset suppressible status
	A4N2	RC205	Reset service selective reset
	A4N2	RC205	Reset svc stop or disconnect
	A4N2	RC204	Reset suppress status stack
0.7	— —	— —	This bit ignored
1.0	A4K2	RC504	Set monitor for circle B
1.1	— —	— —	This bit ignored
1.2	A4K2	RC504	Set Monitor for 2260 ETX
1.3	A4N2	RC204	Set suppressible status
1.4	A4L2	RC406	Set 0X TIO ready
1.5	A4K2	RC504	This bit ignored
1.6	A4L2	RC404	Byte count 2
1.7	A4L2	RC404	Byte count 1

*Any of these bits with 'Sample 62' set Initiate Service, A4L2, RC404



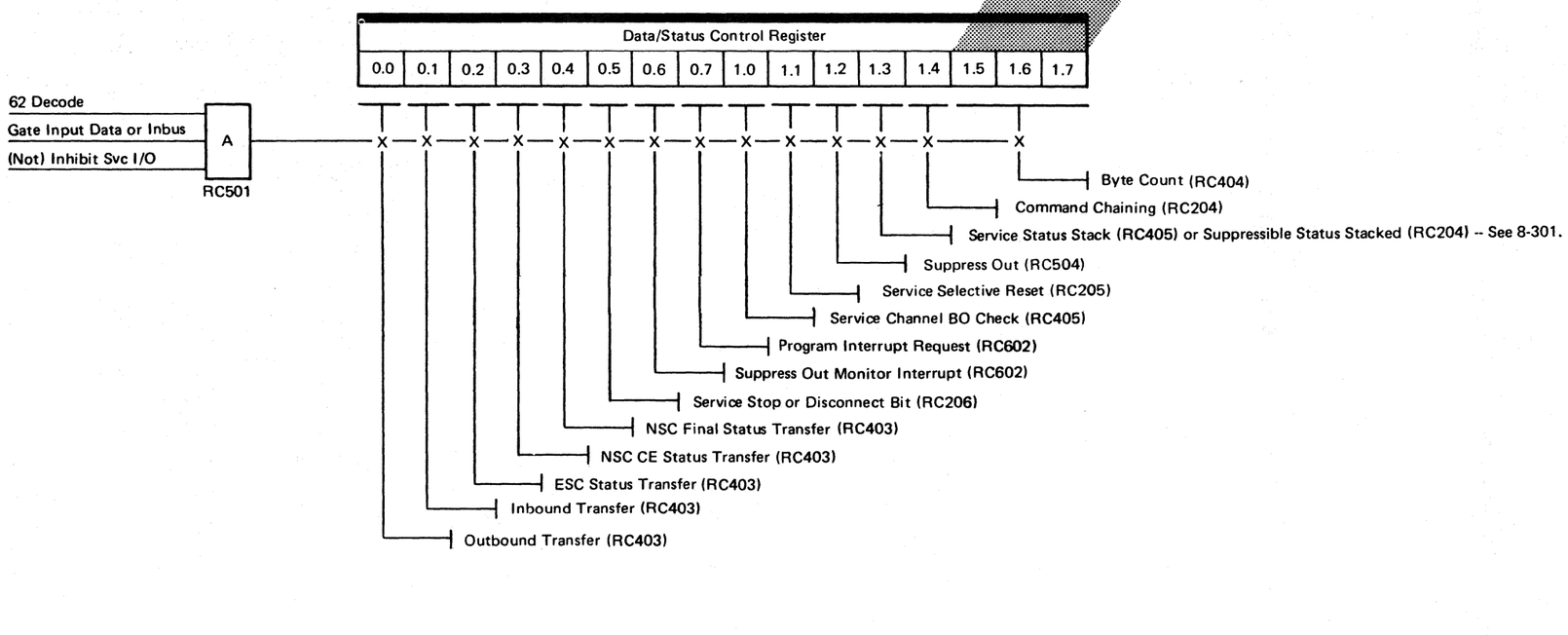
See the chart on this page for the byte count combinations.

Input X'62' Instruction

This instruction transfers the contents of the data/status control register into a CCU general register. The 3705-80 control program uses this instruction to determine the exact cause of a type 1 CA data/status level 3 interrupt.

Count transferred to the CCU

Count	Bits		
	1.5	1.6	1.7
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0

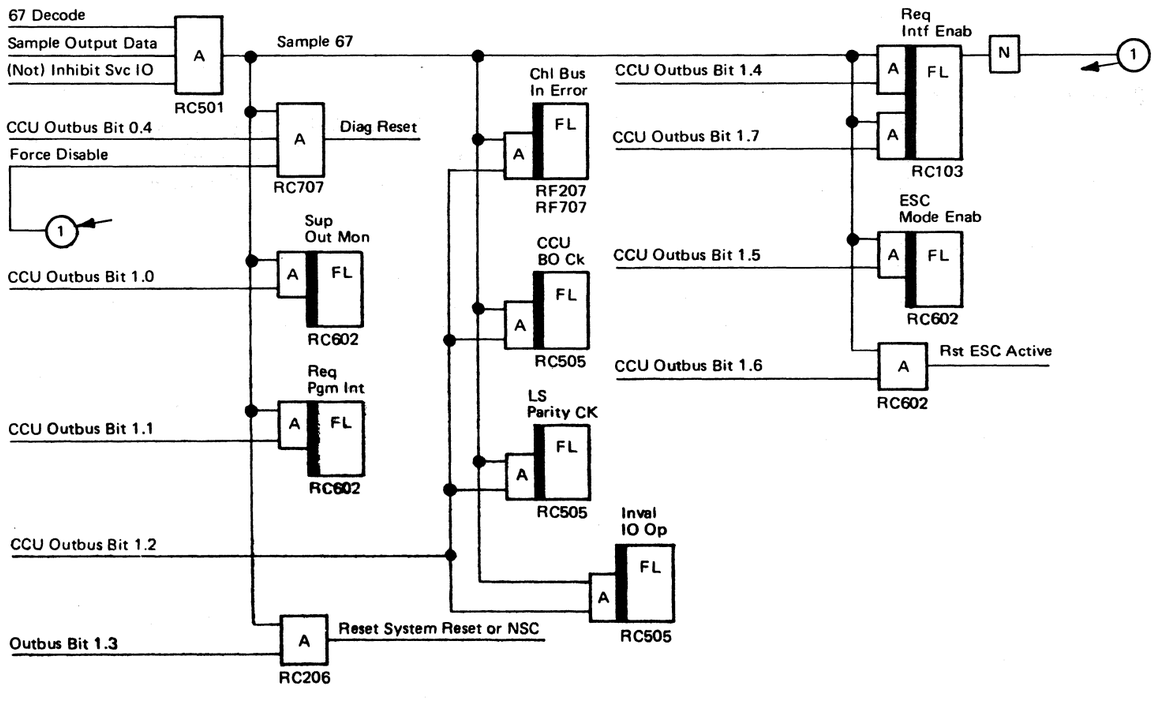


Output and Input X'67' Instruction

The Output X'67' instruction sets or resets the various control latches. The 3705-80 control program must execute an Output X'67' instruction to enable the CA interface before the CA can transfer data to or from the channel.

Summary of Outbus bits during Output X'67'

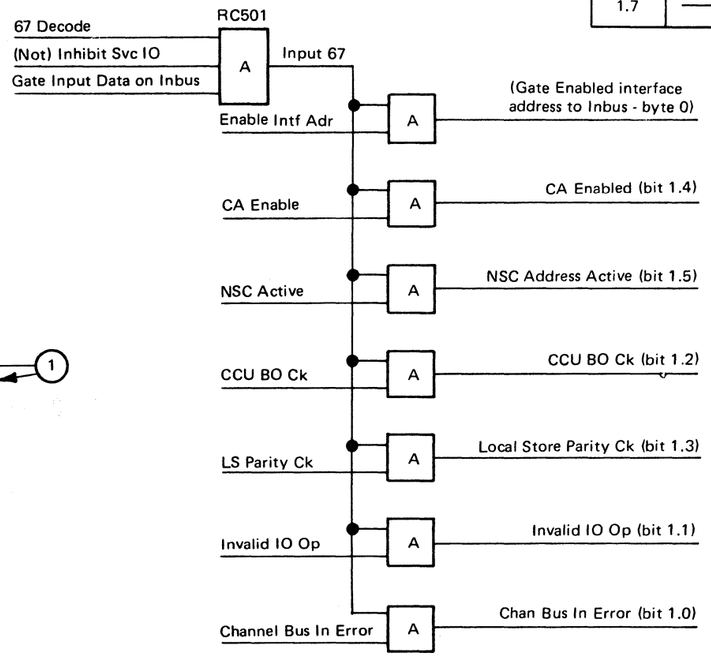
Bit	*Card Loc.*	*ALD Page*	*Function*
0.4	A4Q2	RC707	Diagnostic reset
1.0	A4T2	RC602	Set suppress out monitor
1.1	A4T2	RC602	Set request program interrupt
1.2	A4K2	RC507 RC507 RC507 RC707 RF207	Reset invalid I/O Op Reset local store parity check Reset CCU outbus check Reset channel bus in error (interface A) Reset channel bus in error (interface B)
1.3	A4N2	RC206	Reset system reset or NSC
1.4	A4P2	RC103	Request interface enable
1.5	A4T2	RC602	Set ESC mode enable
1.6	A4T2	RC602	Reset ESC active
1.7	A4P2	RC103	Reset interface enable



The Input X'67' transfers the error condition register and the hardware address of the NSC channel interface address to the CCU.

Summary of Inbus bits during Input X'67':

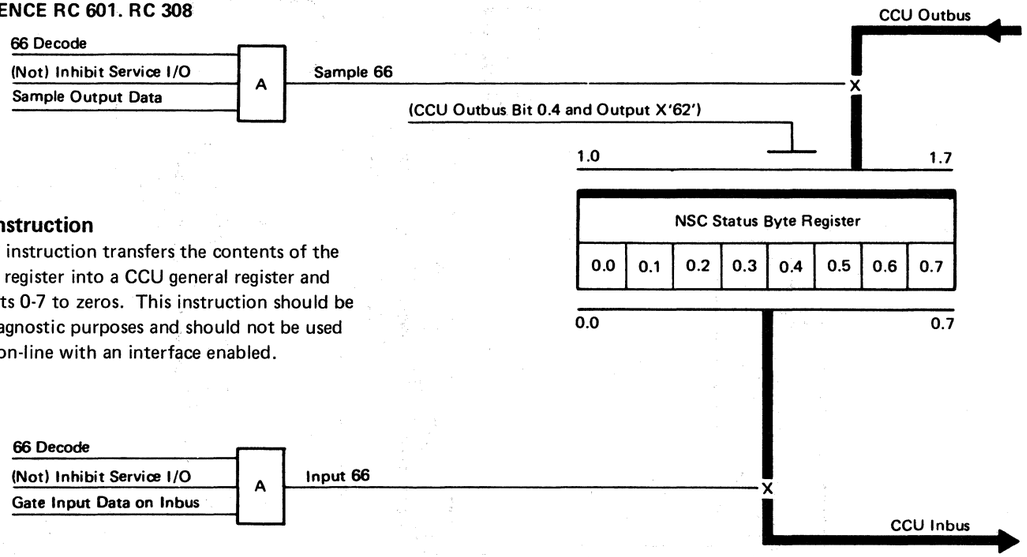
Bit	*Card Loc.*	*Logic Page*	*Function*
0.0-0.7	A4P2	RC104	NSC hardware address intf A
0.0-0.7	A4P2	RC107	NSC hardware address intf B
1.0	A4Q2	RC707	Chan bus in error
1.1	A4K2	RC507	Invalid I/O Op
1.2	A4K2	RC507	CCU outbus check
1.3	A4K2	RC507	Local store parity check
1.4	A4K2	RC504	CA enabled
1.5	A4K2	RC504	NSC address active
1.6	—	—	0
1.7	—	—	0



Output X'66' Instruction

The Output X'66' instruction loads the final status byte to be presented to the channel into the NSC Status Byte Register.

LOGIC REFERENCE RC 601. RC 308



Input X'66' Instruction

The Input X'66' instruction transfers the contents of the NSC status byte register into a CCU general register and forces byte 1, bits 0-7 to zeros. This instruction should be used only for diagnostic purposes and should not be used when the CA is on-line with an interface enabled.

NSC STATUS BYTE REGISTER BIT DEFINITIONS

Bit 0.0 – Attention
Bit 0.1 – Status Modifier
Bit 0.2 – 0
Bit 0.3 – 0
Bit 0.4 – Channel End (CE)
Bit 0.5 – Device End (DE)
Bit 0.6 – Unit Check (UC)
Bit 0.7 – Unit Exception (UE)

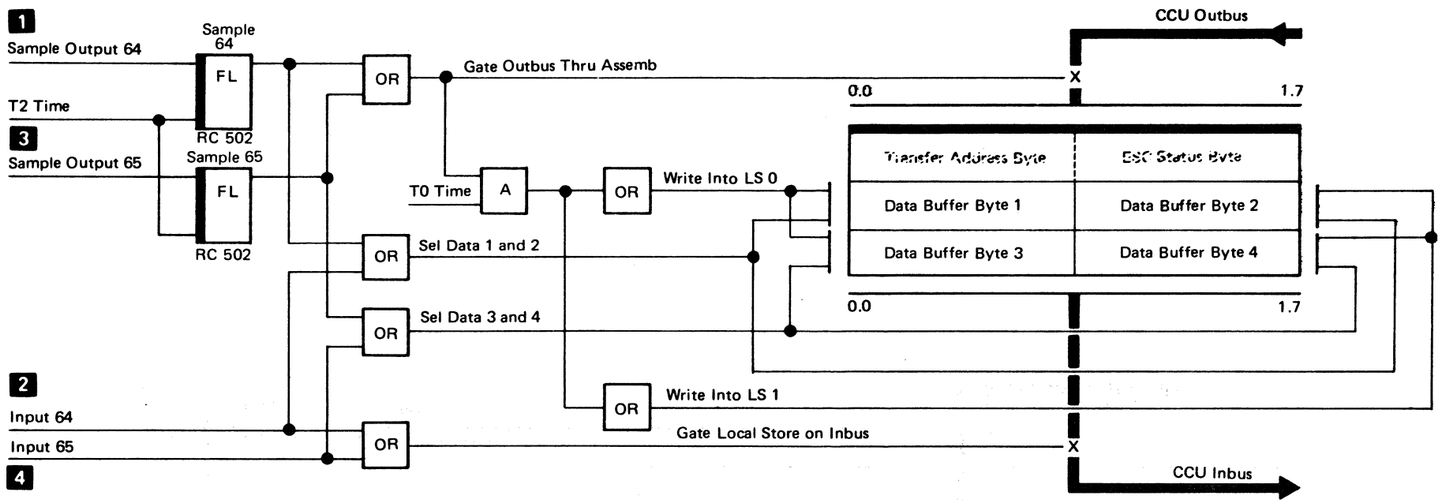
Output and Input X'64' Instruction

1

Output X'64' instruction loads data buffer byte 1 and data buffer byte 2 with the first two data bytes to be transferred across the channel to the host processor. These two data bytes are transferred to the host processor one byte at a time during an outbound data transfer.

2

Input X'64' transfers into a CCU general register the two data bytes that were received from the channel and stored in data buffer byte 1 and data buffer byte 2.



Output and Input X'65' Instruction

3

Output X'65' instruction loads data buffer byte 3 and data buffer byte 4 with the second two bytes to be transferred across the channel to the host processor. These two data bytes are transferred to the host processor one byte at a time during an outbound data transfer.

4

Input X'65' transfers into a CCU general register the two data bytes that were received from the channel and stored in data buffer byte 3 and data buffer byte 4.

Output and Input X'63' Instructions

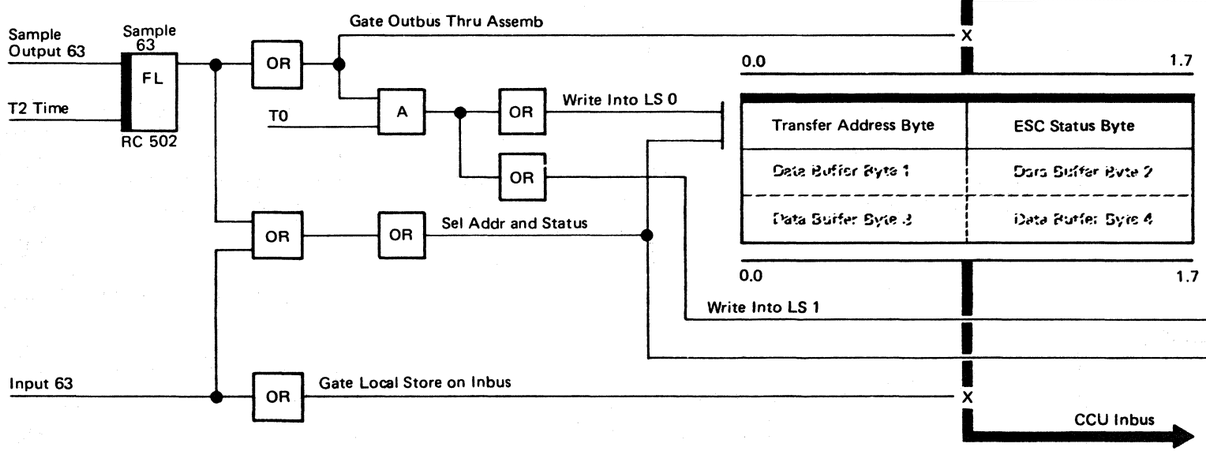
The 3705-80 control program uses the Output X'63' instruction to load the subchannel address (byte 0) and ESC status byte (byte 1) into the local store buffer. The CA identifies itself to the channel by gating byte 0 onto the channel bus-in, during the data transfer and gates byte 1 onto the channel bus-in to transfer the ESC status to the host processor. (NSC address and status take a different path, see page 8-170.)

The 3705-80 control program must ensure that the correct address and status bytes are stored in the register. Otherwise, incorrect channel operation occurs.

With the Input X'63' instruction, the 3705-80 control program can determine the last subchannel address provided to the host processor. The level 3 interrupt request latch should be set for this instruction to execute.

CCU Outbus Bit Definitions

Bits	*Definition*
0.0-0.7	Subchannel address
1.0	Attention
1.1	Status modifier (SM)
1.2	Control unit end (CUE)
1.3	Busy
1.4	Channel end (CE)
1.5	Device end (DE)
1.6	Unit check (UC)
1.7	Unit exception (UE)

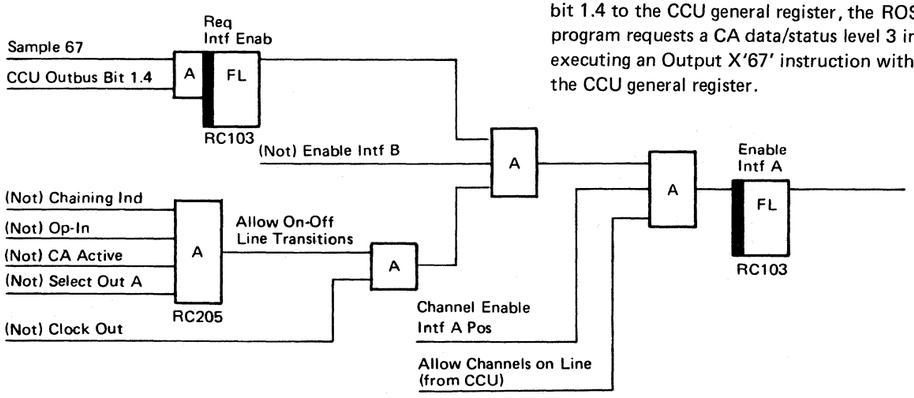


CHANNEL ADAPTER INITIALIZATION (IPL) (PART 1 OF 2)

- Channel adapter initialization involves enabling the CA to a channel interface and requesting a Write IPL command from the host processor.

The type 1 CA is not affected by the reset performed in IPL phase 1 unless the IPL sequence is started by a power on sequence. Therefore, the ROS bootstrap program must handle the following situations:

1. Channel interface disabled.
2. Channel interface enabled without a channel command in progress.
3. Channel interface enabled with a channel command in progress.



The CA can be enabled to one of two channel interfaces. The second channel interface is optional and allows the CA to be attached to two different host processors. The CA can also be attached to the same channel through the interfaces. However, only one interface can be enabled at a time.

The channel interface must be enabled for the channel and CA to communicate. The manual procedure to enable a channel interface is described on page 1-050. The bootstrap program must execute an Output X'67' instruction with bit 1.4 on in the general register. This bit allows the channel interface to be enabled. The ROS bootstrap program checks for the interface to become enabled with an Input X'67' instruction. When the Input X'67' transfers bit 1.4 to the CCU general register, the ROS bootstrap program requests a CA data/status level 3 interrupt by executing an Output X'67' instruction with bit 1.1 on in the CCU general register.

If no channel command is in progress, the program signals the CA to send an asynchronous status of Device End (DE) Unit Check (UC) to the channel. The bootstrap program must execute the following instructions to present the asynchronous attention.

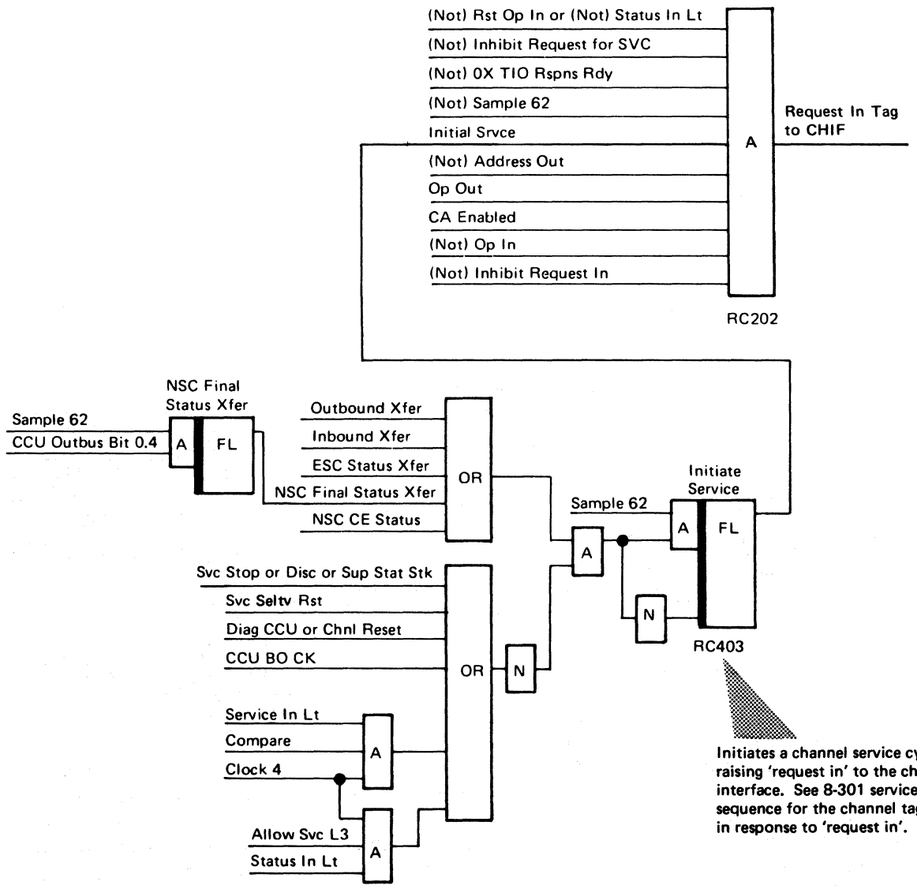
Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Output X'67'	0000 0000	0000 1000	Enable channel interface
Input X'67'	0000 0000	0000 1000	Interface enabled the ROS bootstrap program loops on this instruction until the interface is enabled.
Output X'67'	0000 0000	0100 0000	Program requests a level 3 interrupt. The ROS bootstrap program executes in level 1 which makes this routine different from the control program routine.

The ROS bootstrap program senses the requested interrupt and executes the following sequence of instructions.

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0000 0001	0000 0000	0.7 = Program requested level 3 interrupt
Output X'63'	Address	0000 0000	Byte 0 = NSC address Byte 1 = all zeros
Output X'66'	0000 0000	0000 0110	1.5 = Device End 1.6 = Unit Check **Note:** *If a channel command is pending when the IPL sequence is started, the ROS bootstrap program adds Channel End (CE) to the status byte to signal the host CPU to end the pending command.*
Output X'62'	0000 1000	0000 0000	0.4 = NSC Final Status transfer

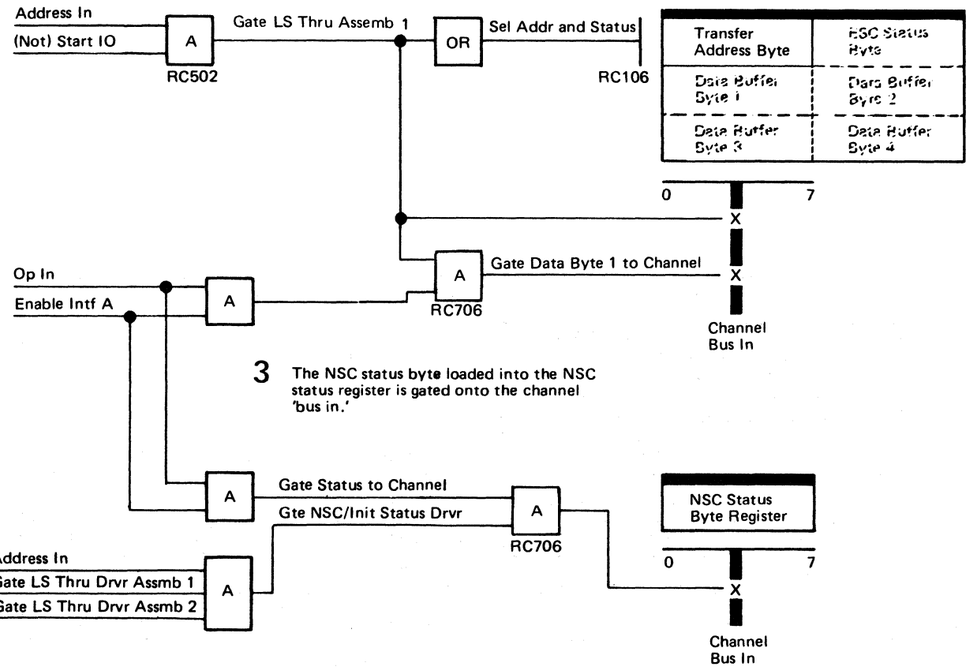
CHANNEL ADAPTER INITIALIZATION (PART 2 OF 2)

1 The Output X'62' sets bit 0.4 in the data/status control register and causes the CA to attach to the channel and initiate a channel transfer.



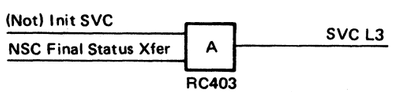
Initiates a channel service cycle by raising 'request in' to the channel interface. See 8-301 service status sequence for the channel tag sequence in response to 'request in'.

2 The NSC address loaded into the transfer address byte buffer is gated onto the channel 'bus in' to identify the device requesting channel service.



3 The NSC status byte loaded into the NSC status register is gated onto the channel 'bus in.'

4 The CA requests a data/status level 3 interrupt to signal the ROS bootstrap program that the status transfer is complete.



EXPECTED CPU RESPONSE TO ASYNCHRONOUS STATUS

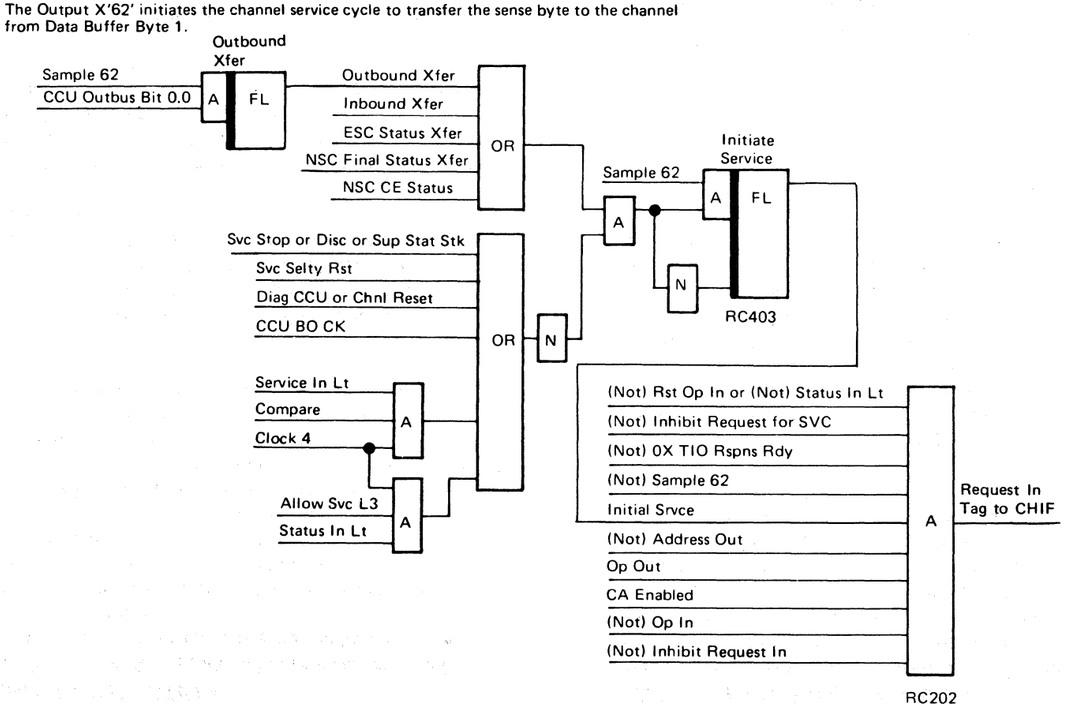
The ROS bootstrap program expects to receive a Channel Sense command in response to the asynchronous DE, UC Status so the program loops waiting for an initial selection level 3 interrupt from the CA.

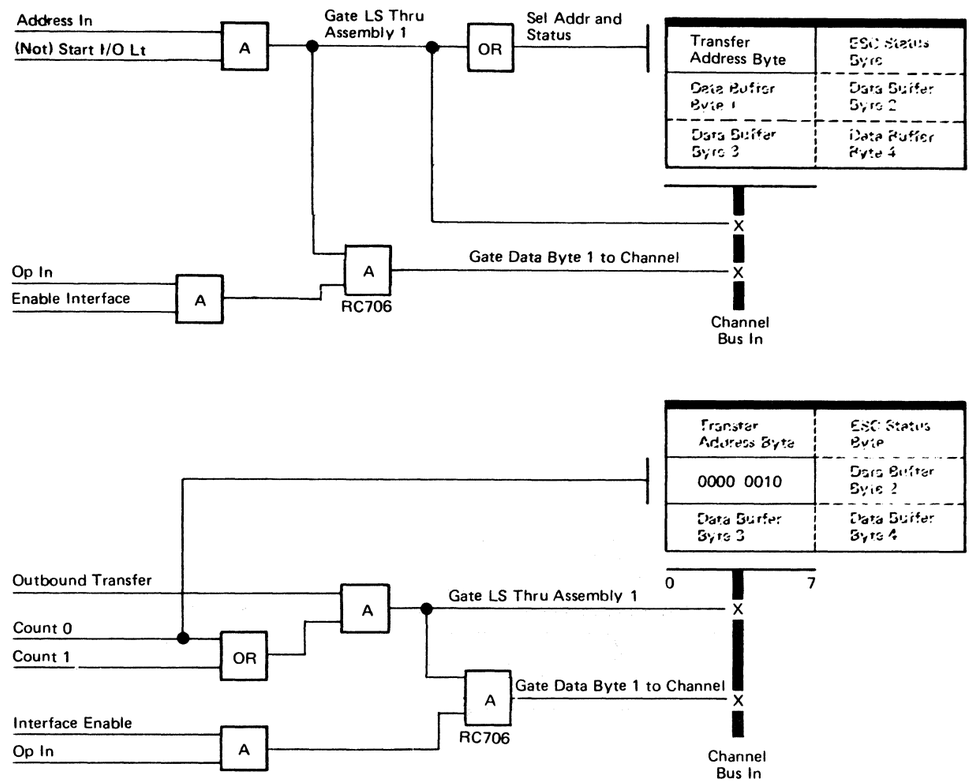
Because the ROS bootstrap program can only handle a Sense or Write IPL command, it rejects others by presenting final status of CE, DE, and UC.

However, any command received by the CA starts an initial selection sequence. When the channel Sense command starts the initial selection sequence, and requests a type 1 CA initial selection level 3 interrupt, the ROS bootstrap program responds with the following instructions:

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0000 1000	Type 1 CA Initial Selection L3 Interrupt
Input X'60'	1000 0000	0000 0000	Normal initial selection
Input X'61'	Address	Command	Byte 0 = address of NSC Byte 1 = command
Output X'63'	Address	0000 0000	Byte 0 = NSC address
Output X'64'	0000 0010	0000 0000	0.6 = Not initialized (sense byte)
Output X'62'	1000 0100	0000 0001	0.0 = Outbound transfer sequence 0.5 = Reset initial selection 1.7 = byte count of one

The Output X'62' initiates the channel service cycle to transfer the sense byte to the channel from Data Buffer Byte 1.





SENSE BIT DEFINITIONS

Bit 0 – Command Reject. This bit indicated that the channel command presented to the channel adapter is not a valid command for a particular subchannel address or not valid for the NSC address.

Bit 1 – Intervention Required. This bit indicated that programming errors were detected by either the CA, the CCU, or the 3705-80 control program. CA hardware sets this bit when the CA is executing a channel Read, Write, or Write Break command.

Bit 2 – Bus Out Check. This bit indicated a parity check was detected on the I/O channel bus out during the initial selection command byte transfer or during host processor to 3705-80 data transfer.

Note: *Refer to the Program Logic Manual for the sense bit definitions because they are program dependent.*

Bit 3 – Equipment Check. This bit indicates that an internal hardware check or a parity check is detected during a data transfer between the CCU and the channel adapter.

Bit 4 – Data check.

Bit 5 – Not used.

Bit 6 – This bit indicated that the CCU is not initialized. The host CPU is expected to respond to this bit with a Write IPL command.

Bit 7 – Abort. This bit indicated that the 3705-80 control program has terminated its channel operation in an abnormal manner.

SENSE COMMAND ENDING STATUS

Ending status can be presented to the channel in one of three combinations:

1. CE, DE presented together - normal operation.
2. Split CE, DE, (that is, not together).
3. CE, DE, and UC, - occurs when interface disconnect is received during a Sense command.

INITIAL SELECTION

- The CA decodes its address from the channel 'bus out' and stores it in the initial selection address and command byte register.
- The CA decodes the channel command and either:
  1. Executes the command without control program intervention, (No-Op, NSC Test I/O).
  2. Requests an initial selection level 3 interrupt so the 3705-80 control program can process the command. The command byte is stored in the initial selection address and command byte register.
- The CA gates initial status to the channel 'bus in' for each command without control program intervention.

Each channel command issued to the CA starts an initial selection sequence. Since the 3705-80 can emulate either an IBM 2701, IBM 2702, or an IBM 2703, or operate in native mode (NSC), some differences occur during several commands.

In native mode (NSC address), the CA handles No-Op and Test I/O commands without control program intervention. The CA also handles No-Op without control program intervention when the 3705-80 is operating in emulation mode (ESC address).

In order for the CA to decode its address or commands, the CA must be enabled with respect to a channel interface as described in Channel Adapter Initialization, 8-140. If the 3705-80 is to operate in emulation mode (ESC), the 3705-80 control program must also set ESC operational with an Output X'67' instruction.

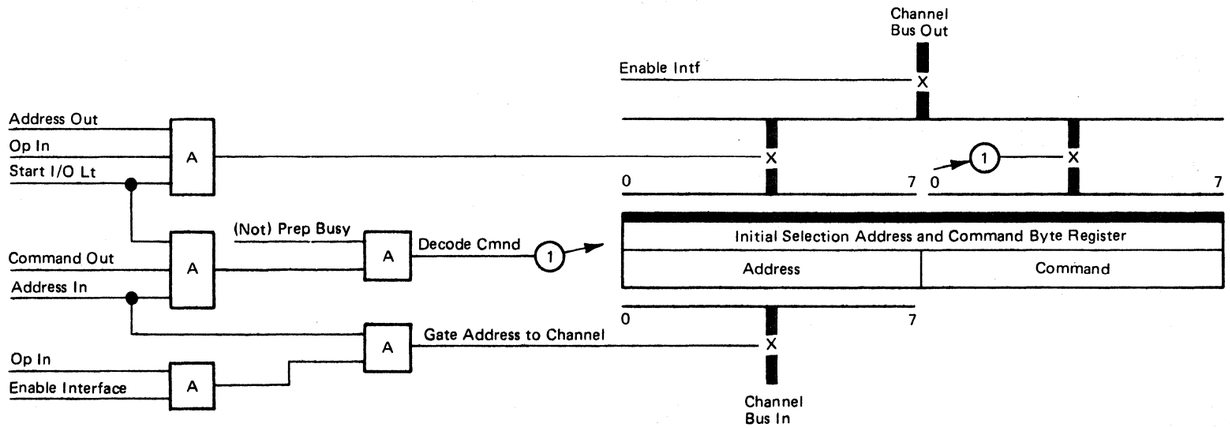
If the CA raises 'request in' to start a data/status transfer, but the channel responds with 'address out' and 'select out' (initial selection sequence), the initial selection sequence overrides the data/status transfer. The 3705-80 control program must remember that the data/status in the local store was not transferred to the channel and must present it again. This can only occur during ESC mode.

CA Decodes and Stores the Address

The CA can recognize a range of addresses as described on 8-000. The addresses that are hardware plugged are compared to the address from the channel to determine when the channel is addressing the CA. The NSC address is plugged on card A4P2 (RC104 for interface A and RC107 and RC106 for interface B). The low ESC address is plugged on card A4M2 (RC302), and the high ESC address is plugged on card A4M2 (RC304).

If the address is valid, it is gated into the initial selection address and command byte register. The CA gates the address onto the channel 'bus in' and receives a channel command in response. Channel commands are also maintained in the initial selection address and command byte register. The action taken for each command varies, depending upon the mode (ESC or NSC) and the command. Refer to the discussions of the different commands to determine how they are executed.

LOGIC REFERENCE: RC 306



WRITE IPL COMMAND (PART 1 OF 2)

- A channel Write IPL command is required to transfer the program load module from the host processor to 3705-80 storage.
- The CCU is not initialized until control is passed from the ROS bootstrap program to the program load module.
- The 3705-80 is controlled by the ROS bootstrap program during the Write IPL command execution.

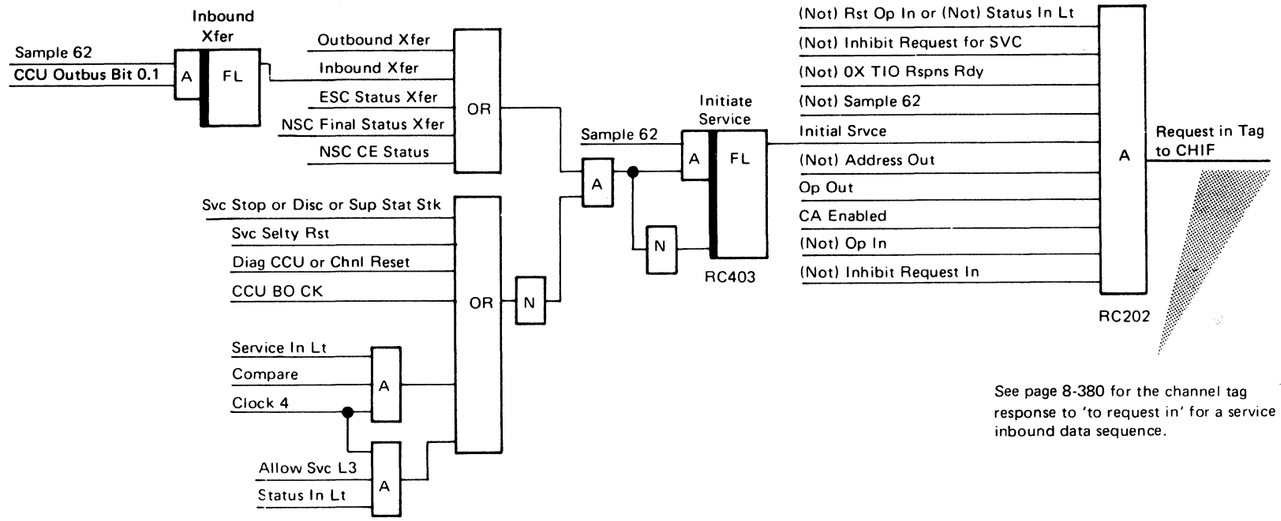
The 3705-80 ROS bootstrap program expects a Write IPL command in response to the not initialized sense bit. If a command other than Write IPL is decoded by the CA, the ROS bootstrap program signals the CA to end the command by presenting Channel End (CE), Device End (DE), and Unit Check (UC) status to the channel.

When the Write IPL command is decoded by the CA, a Type 1 CA initial selection level 3 interrupt is requested.

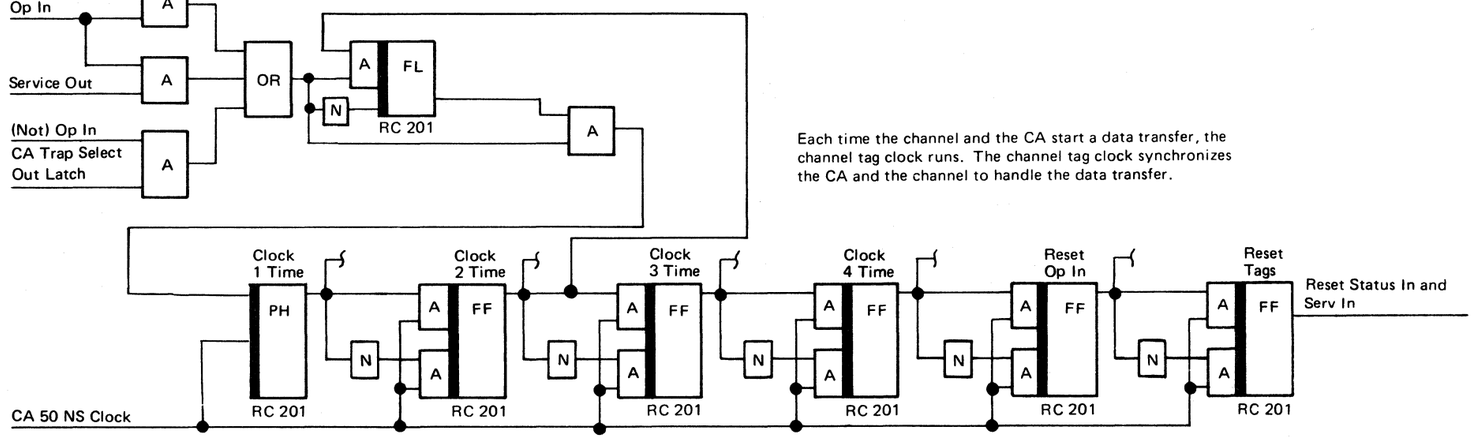
The 3705-80 control program responds to the interrupt request with the following instructions:

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0000 1000	Type 1 CA initial selection level 3 interrupt
Input X'60'	1000 0000	0000 0000	Normal initial selection (see note)
Input X'61'	Address	0000 0101	Byte 0 = address Byte 1 = Write IPL command
Output X'63'	Address	0000 0000	Byte 0 = NSC address Byte 1 = all zeros
Output X'62'	0100 0110	0000 0010	0.1 = Inbound transfer sequence 0.5 = Reset initial selection 0.6 = Reset data service 1.6-1.7 = Number of bytes to transfer. The ROS bootstrap program always requests two data bytes during IPL.

Note: *Bit 0.0 is the only bit expected to be on at this time. Other bits may be on at different times and indicate different conditions to the 3705-80 control program. See Input X'60' instruction 8-070 for descriptions of the other bits in this register.*



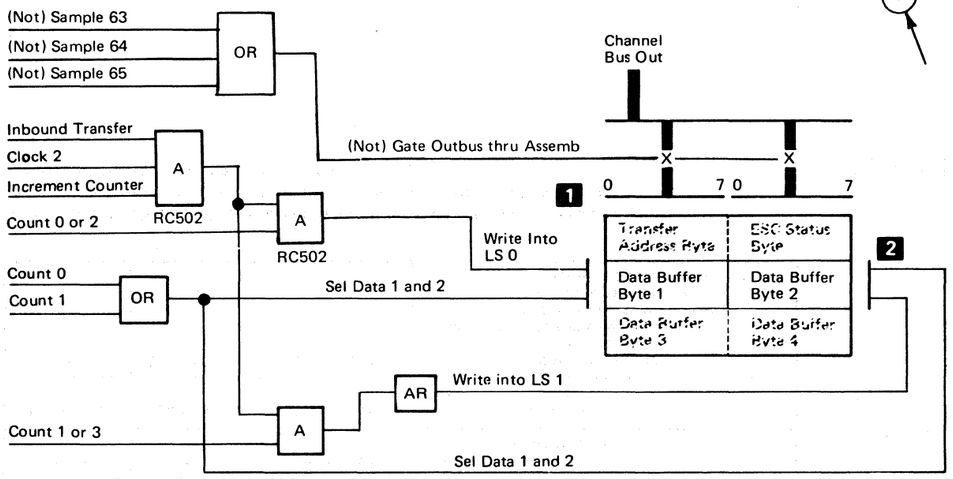
See page 8-380 for the channel tag response to 'to request in' for a service inbound data sequence.



Each time the channel and the CA start a data transfer, the channel tag clock runs. The channel tag clock synchronizes the CA and the channel to handle the data transfer.

WRITE IPL
(PART 2 OF 2)

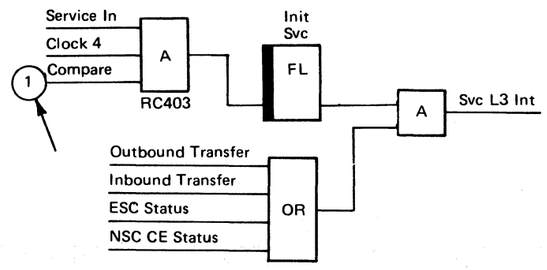
Data transfers across the channel one byte at a time, and each byte is gated into the local store data buffer. The byte count is incremented for each byte transferred.

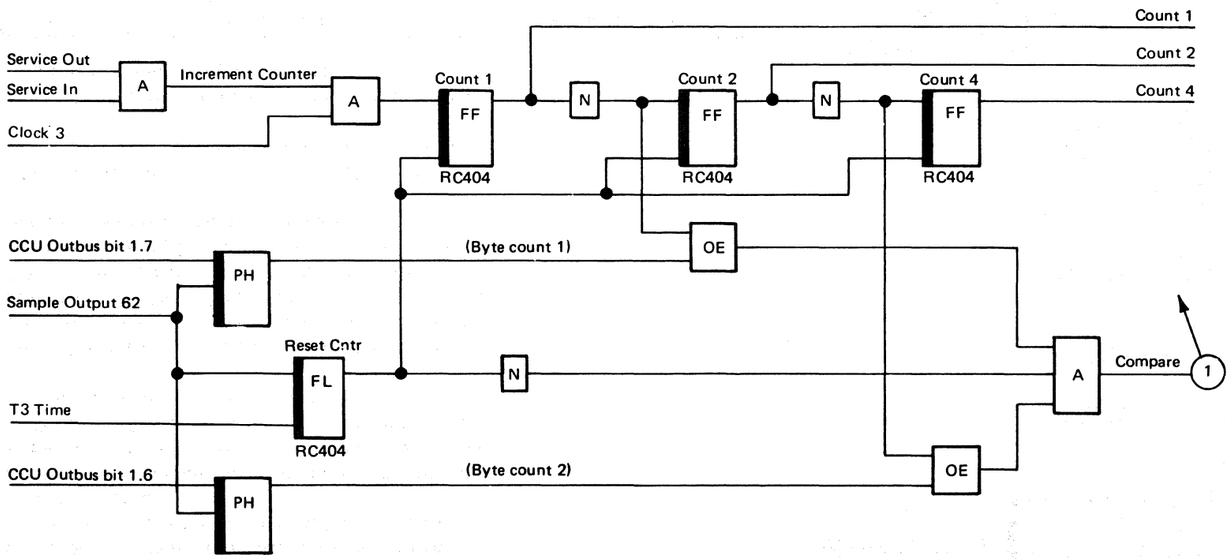


1 Loads byte 1 into Data Buffer Byte 1

2 Loads byte 2 into Data Buffer Byte 2

When the number of bytes transferred equals the count specified by the Output X'62' instruction, the CA requests a level 3 data/status interrupt.





In response to the CA data/status level three interrupt, the 3705-80 control program must execute the following instructions.

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt.
Input X'62'	0100 0*00	0000 0XXX	0.1 = inbound data transfer *0.5 if on indicates a channel stop or interface disconnect. The control program should end the channel command. 1.5-1.7 = the number of bytes transferred.
Input X'63'	Address	0000 0000	Byte 0 = Subchannel address Byte 1 = all zeros
Input X'64'	Data byte	Data byte	Byte 0 = data byte 1 Byte 1 = data byte 2
Output X'62'	0100 0010	0000 0010	0.1 = inbound data transfer 0.6 = reset data/status condition 1.6 = request 2 bytes of data

Note: *This bit pattern is valid only if the CA is to continue the data transfer. The ROS bootstrap program expects to transfer up to 1022 data bytes before ending the channel command and requests 2 bytes of data on each transfer. This sequence is repeated until the transfer is completed. If the transfer is to end, see 8-280.*

If bit 0.5 is on during the input X'62', the channel has signaled the end of the data transfer by initiating a channel stop sequence. The 3705-80 control program should send the final status to the channel with the following instructions.

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Output X'63'	Address	0000 0000	byte 0 = subchannel address See note 1
Output X'66'	0000 0000	0000 1100	1.0 = Attention 1.1 = Status Modifier 1.2 = 0 1.3 = 0 1.4 = Channel End See note 2 1.5 = Device End See note 2 1.6 = Unit Check 1.7 = Unit Exception
Output X'62'	0000 1010	0000 0000	0.4 = Set NSC Final Status Transfer. 0.6 = Reset data/status L3 interrupt

Notes:

1. *The 3705-80 control program does not necessarily have to execute this instruction since the NSC address in the transfer address byte register should not have changed during the data transfer.*
2. *This is the normal final status that should be presented. However, the 3705-80 control program can present other bits to designate different conditions if needed.*

CA DECODES A CHANNEL COMMAND

The CA accepts any command byte if it is in correct parity on the channel 'Bus Out'. The command is handled without control program intervention if (1) the 3705-80 is in native mode, and the command is a No-Op or Test I/O, or (2) the 3705-80 is in emulation mode, and the command is a No-Op.

Note: *Depending upon whether the 3705-80 is in native mode (NSC) or emulation mode (ESC), different action may be taken for a channel command. Where there is a difference, NSC information is in the left hand column and ESC information is in the right hand column.*

Otherwise, the command is stored in the initial selection address and command byte register, and an initial selection level 3 interrupt is requested so the 3705-80 control program can handle the command as required.

NSC

No-Op Command

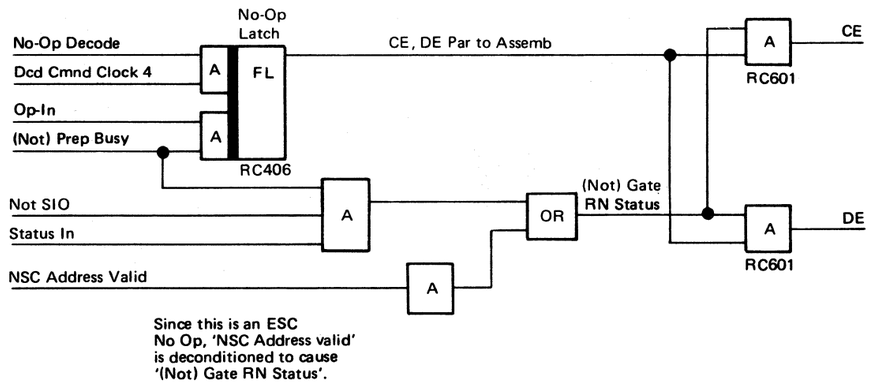
If the CA is free of commands when the No-Op is decoded, CE, DE status is presented immediately to the channel 'Bus In'. See diagram for ESC No-Op.

If any pending status is available, or the CA is not free of commands, the CA presents that status along with Busy to the channel 'Bus In'.

ESC

No-Op Command

The CA immediately presents CE, DE status to the channel.



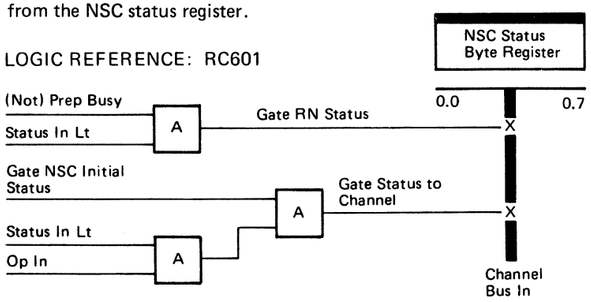
NSC

Test I/O

- Presents initial status of X'00', or presents any pending status with the initial status.

If NSC status is pending, Test I/O initial status is gated from the NSC status register.

LOGIC REFERENCE: RC601



If NSC status is not pending, Test I/O initial status is gated from the initial selection status register.

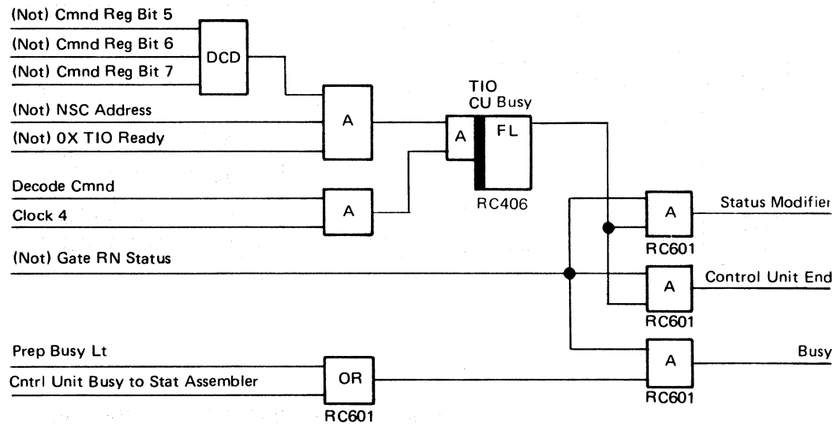
LOGIC REFERENCE: RC406

ESC

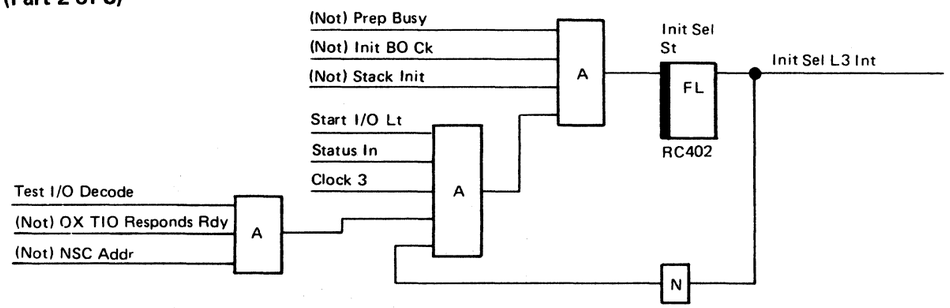
Test I/O
(Part 1 of 3)

- Presents initial status of
  - Status Modifier
  - Control Unit End
  - Busy
- Requests a level 3 interrupt so that the 3705-80 control program can present the status of the subchannel address to which the command was issued.

The CA presents the initial status for this command and requests an initial selection level 3 interrupt so that the 3705-80 control program can load the status byte for the subchannel address into the ESC status byte register in local store.



Test I/O
(Part 2 of 3)



The 3705-80 control program must determine the status to return to the channel after determining which subchannel address the Test I/O was issued to. The 3705-80 control program must execute the following instructions in response to the level 3 interrupt.

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0000 1000	Type 1 CA initial selection level 3 interrupt.
Input X'60'	1000 0000	0000 0000	Normal Initial Selection
Input X'61'	address	0000 0000	byte 0 = address requesting service byte 1 = Test I/O decode
Output X'63'	address	status	byte 0 = subchannel address byte 1 = status of subchannel
Output X'62'	0010 0110	0000 1000	0.2 = ESC final status transfer 0.5 = Reset Initial Selection 0.6 = Reset data/status control 1.4 = ESC Test I/O Status Ready

The host processor program must loop on the Test I/O command. When the next initial selection sequence occurs, the hardware compares the address presented to the adapter on the channel 'Bus Out' to the address maintained in the initial selection address and command byte register.

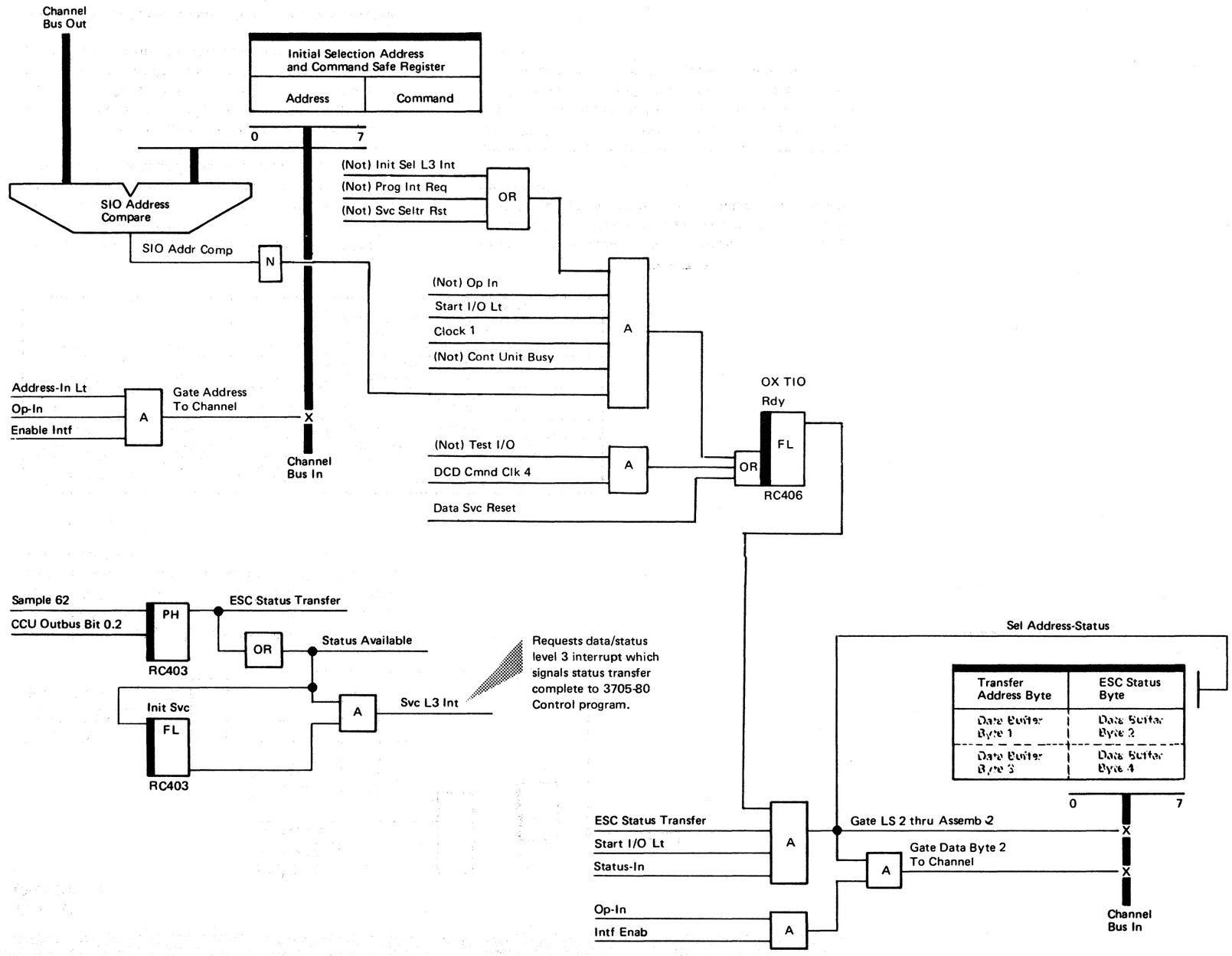
If these addresses compare and the subsequent command is a Test I/O command, the CA presents the status byte loaded by an Output X'63' instruction and then requests a data/status level 3 interrupt so that the 3705-80 control program can determine that the status was presented.

If the addresses do not compare during the initial selection sequence or if the command is not a Test I/O command, the CA resets out of the ESC Test I/O mode and handles this sequence as a normal initial selection. If this occurs, the 3705-80 control program does not sense a data/status level 3 interrupt request resulting from the completion of the Test I/O.

Between the time the Test I/O is first issued, and the time the 3705-80 control program executes the Output X'62' to transfer the status, the CA responds with a short control unit busy status (Status Modifier, Control Unit End, and Busy) to any initial selection sequence from the host processor.

NSC ESC

TEST I/O
(Part 3 of 3)

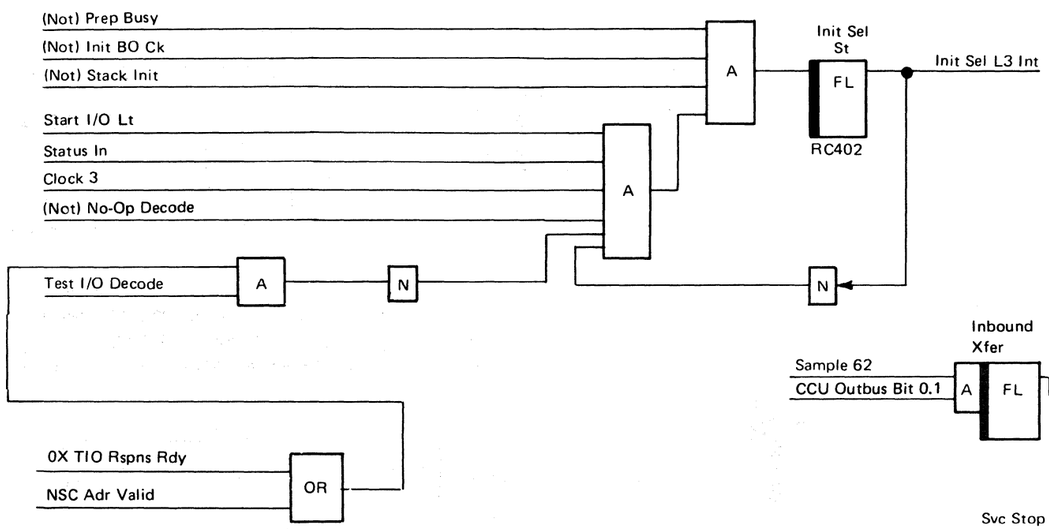


INBOUND DATA TRANSFERS (PART 1 OF 3)

Inbound data transfers result from commands that require the passing of data from the host processor to 3705-80 storage.

When the commands are decoded, they request an initial selection level 3 interrupt so that the 3705-80 control program can determine what action to take to service the command. The commands start an initial selection sequence as shown on 8-170.

CA Requests an Initial Selection Level 3 Interrupt



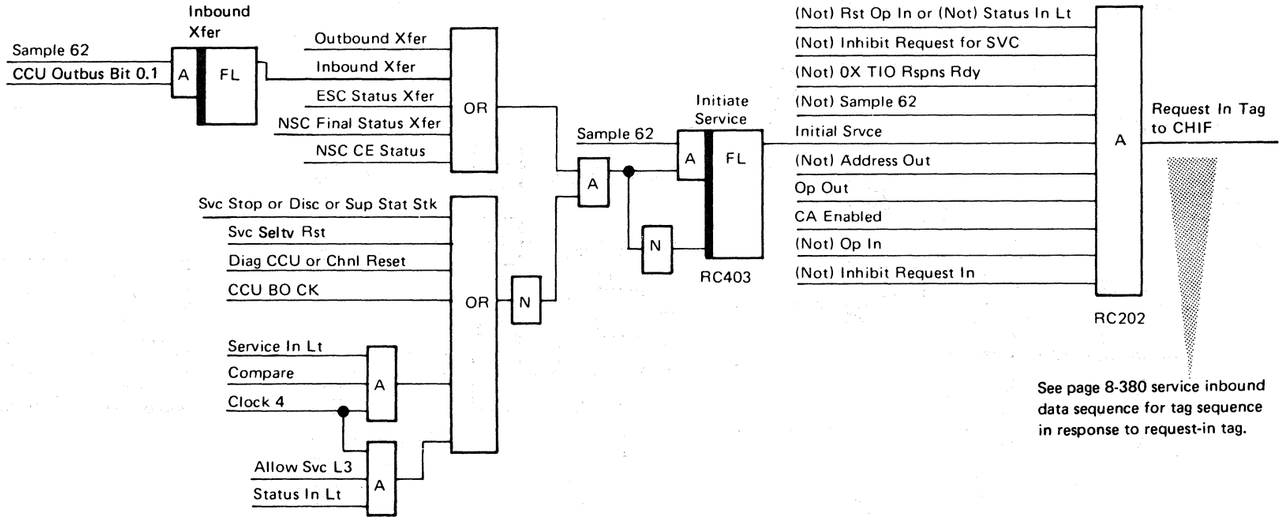
Control Program Responds to the Interrupt

The 3705-80 control program responds to the initial selection level 3 interrupt with the following sequence of instructions.

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0000 1000	Type 1 CA initial selection level 3 interrupt
Input X'60'	1000 0000	0000 0000	Normal initial selection *
Input X'61'	Address	Command	Byte 0 = subchannel address Byte 1 = command
Output X'63'	Address	0000 0000	Byte 0 = address Byte 1 = all zeros
Output X'62'	0100 0110	0000 0000	0.1 = inbound data transfer 0.5 = reset initial selection 0.6 = reset data/status control 1.6-1.7 = 0 to request 4 bytes transferred in

*If other bits are on during this input, the 3705-80 control program must take appropriate action to service the condition indicated by the bit.

The Output X'62' instruction intiates a channel service cycle to transfer the data from the host processor to the CA local store.

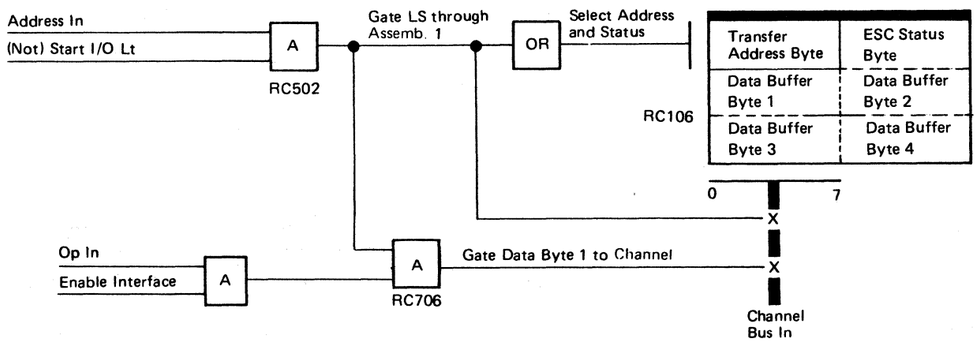


See page 8-380 service inbound data sequence for tag sequence in response to request-in tag.

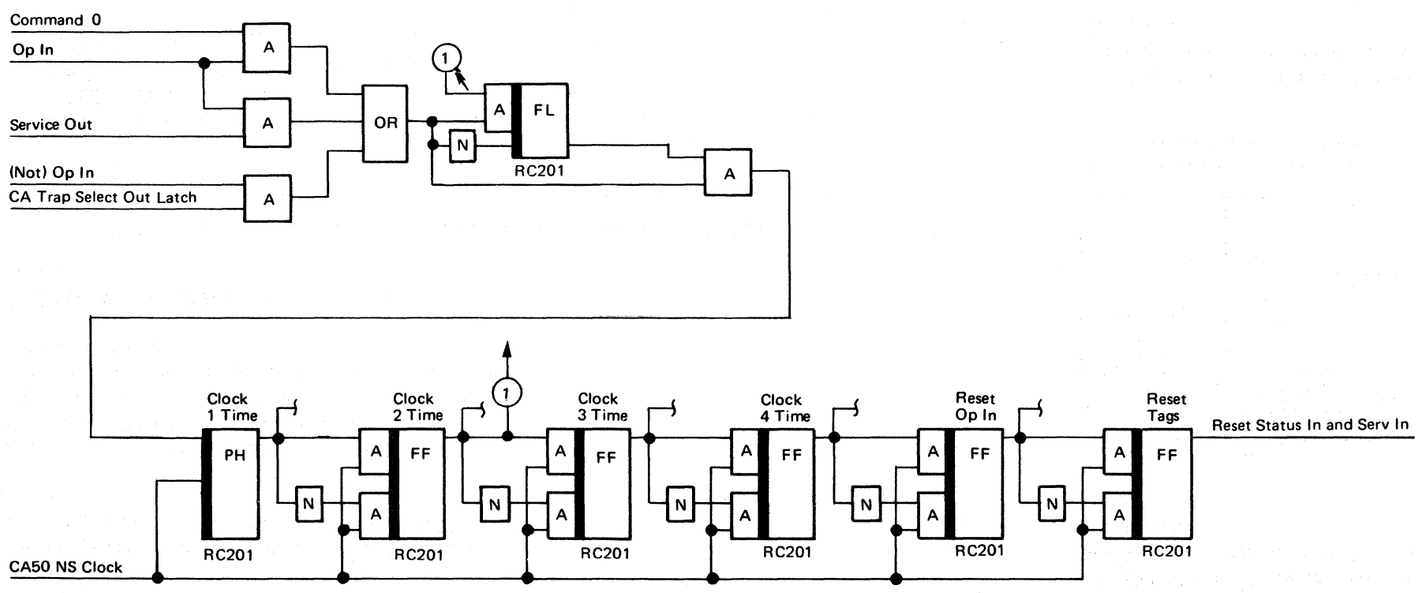
INBOUND DATA TRANSFER (PART 2 OF 3)

CA and Channel Transfer Data

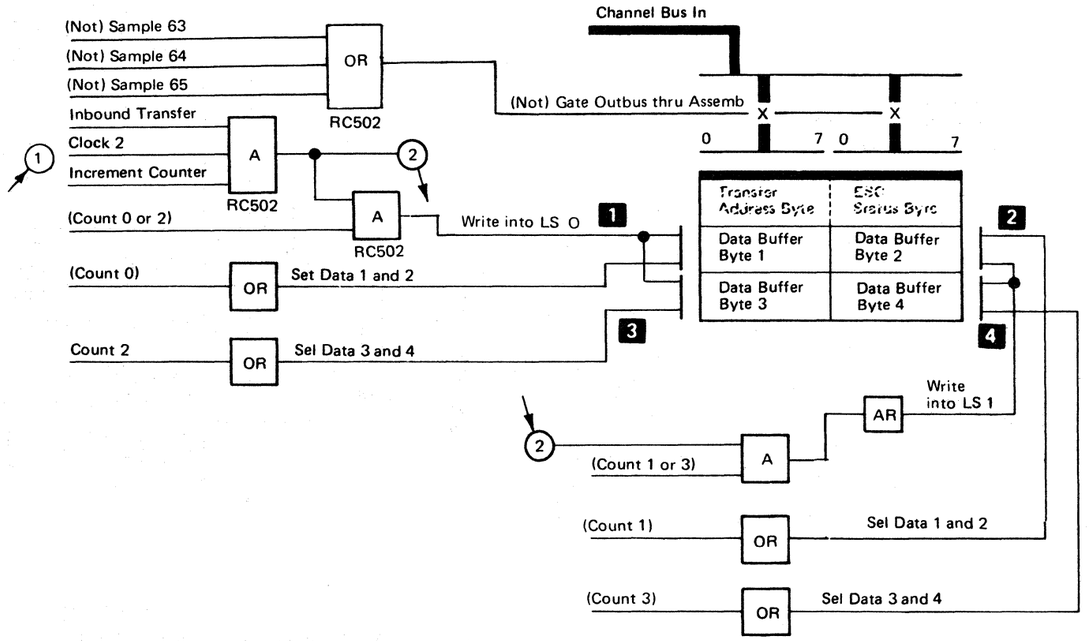
1 After trapping select out, the CA identifies itself to the channel. Refer to page 8-320 for an explanation of 'request in' to the channel.



2 The channel tag clock operates each time the channel and the CA start a data transfer. The clock synchronizes the CA and the channel to handle the data transfer.



3A Data transfers across the channel one byte at a time, and each byte is gated into the local store data buffer. The byte count is incremented for each byte transferred. When the byte count equals the number of bytes specified in the Output X'62' instruction, the CA requests a level 3 interrupt.



1 Loads byte 1 into Data Buffer Byte 1

2 Loads byte 2 into Data Buffer Byte 2

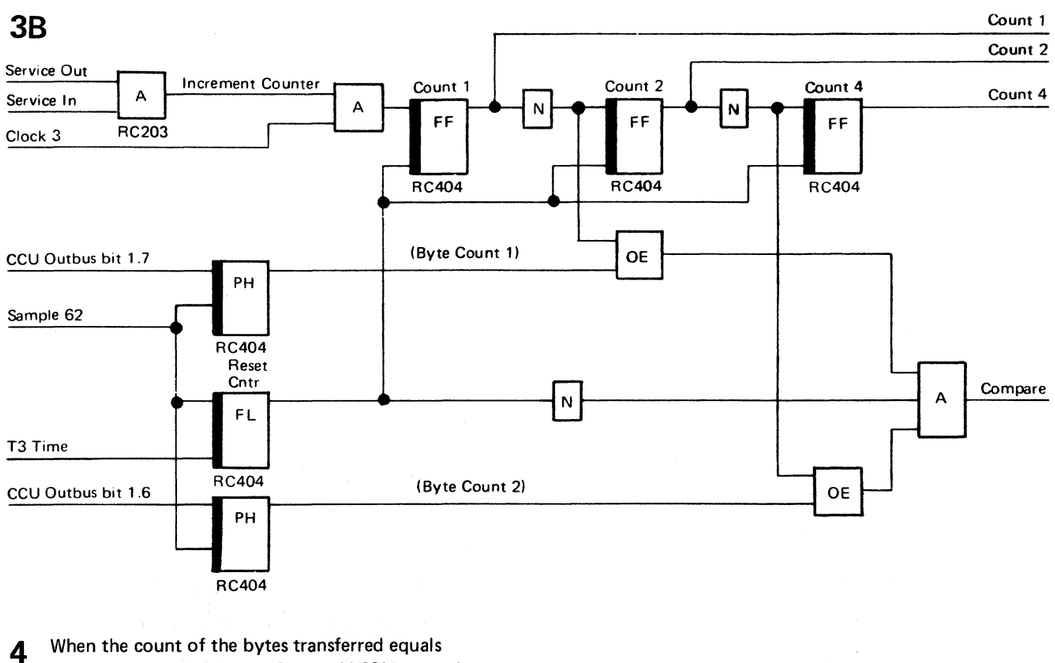
3 Loads byte 3 into Data Buffer Byte 3

4 Loads byte 4 into Data Buffer Byte 4

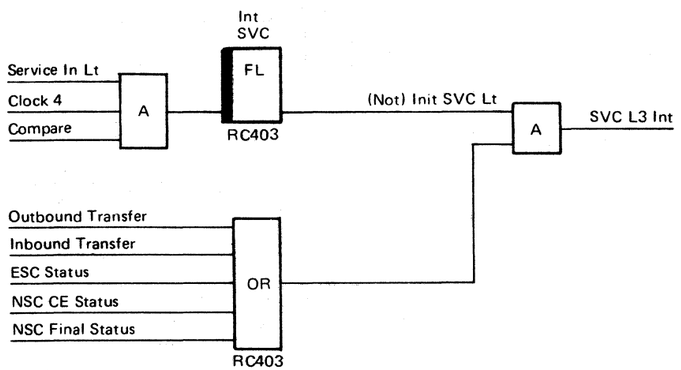
INBOUND DATA TRANSFER (PART 3 OF 3)

CA and Channel Transfer Data

3B



4 When the count of the bytes transferred equals the count specified by the Output X'62' instruction, the CA requests a level 3 data/status interrupt by resetting the initiate service FL.



5 In response to the CA data/status level 3 interrupt, the 3705-80 control program must execute the following instructions.

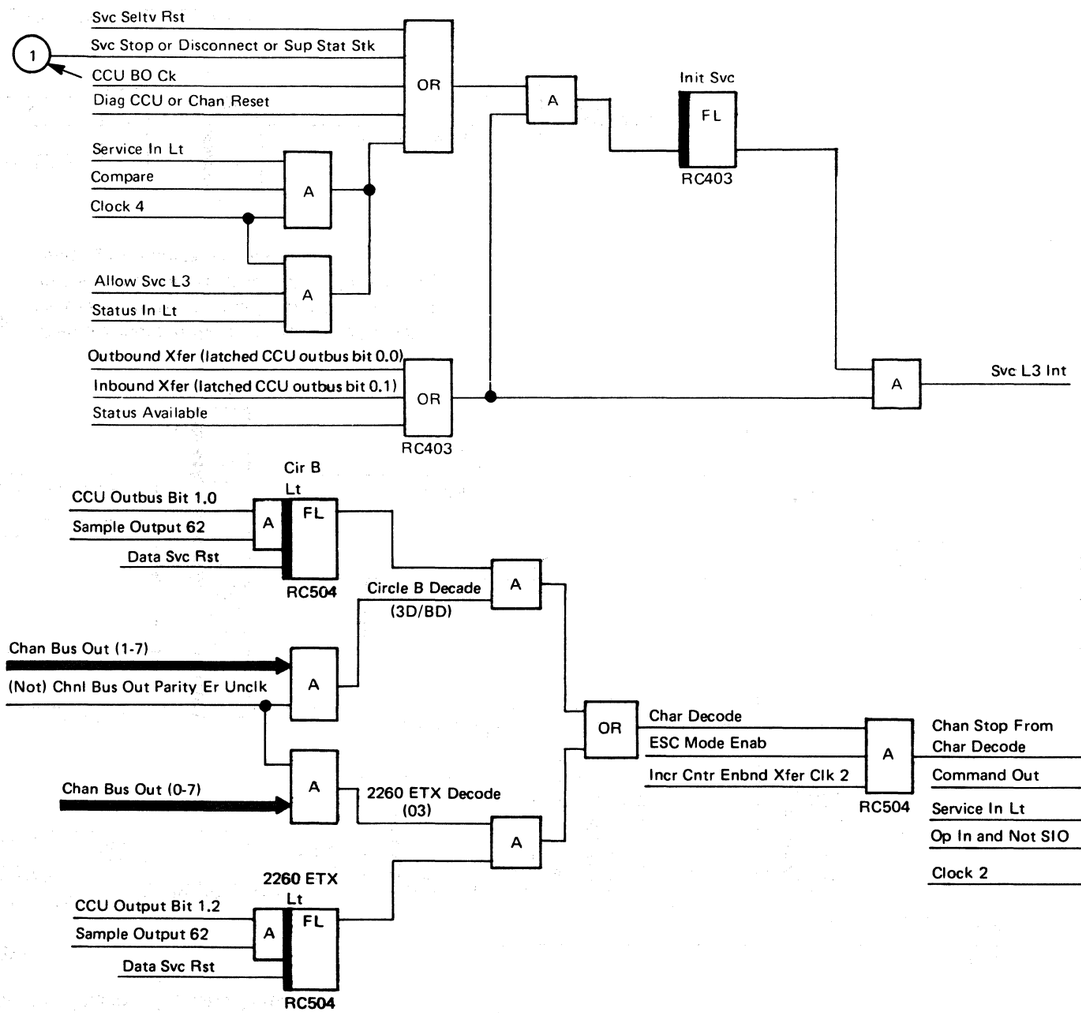
Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt.
Input X'62'	0100 0*00	0000 0XXX	0.1 = inbound data transfer *0.5 if on indicates a channel stop condition, and the control program should end the channel command. 1.5-1.7 = the number of bytes transferred.
Input X'63'	Address	0000 0000	Byte 0 = subchannel address Byte 1 = all zeros
Input X'64'	Data byte	Data byte	Byte 0 = data byte 1 (Note 1) Byte 1 = data byte 2 (Note 1)
Input X'65'	Data byte	Data byte	Byte 0 = data byte 3 (Note 1) Byte 1 = data byte 4 (Note 1)
Output X'62'	0100 0010	0000 00XX	0.1 = inbound data transfer 0.6 = reset data service condition (if required). 1.6-1.7 = Indicate the number of bytes of data. (Note 2)

Notes:

1. *Execution of Input X'64' and X'65' depends upon how many data bytes are requested.*
2. *This bit pattern is valid only if the CA is to continue the data transfer. If the transfer is to end, see 8-280.*

ENDING AN INBOUND TRANSFER (PART 1 OF 3)

When the host CPU has transferred all the inbound data, a channel stop sequence is initiated. When the 3705-80 control program executes the Input X'62' instruction in response to the data/status level 3 interrupt, bit 0.5 is transferred to the CCU general register so that the 3705-80 control program can take appropriate action to end the command. The channel stop sequence initiates a Type 1 CA data/status level 3 interrupt.



The 3705-80 control program responds to the data/status level 3 interrupt with the following instructions.

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'63'	Address	0000 0000	Byte 0 = address the channel adapter was serving when channel stop occurred.
Input X'62'	0100 0100	0000 0XXX	0.1 = inbound transfer 0.5 = service stop or disconnect 1.5-1.7 = transferred byte count.

Note: *Where differences exist in NSC and ESC status transfer, NSC information appears on the left, and ESC information on the right of the page.*

When the channel adapter is in ESC mode, the channel adapter hardware (1) monitors the channel bus out for a circle B character (X'3D' or 'BD') if the 'circle B' latch is set, or (2) monitors the channel bus out for a 2260 ETX character (X'03') if the '2260 ETX' latch is set. When either character is decoded, a channel stop is initiated as described above. The 'circle B' and '2260 ETC' latches are set by the 3705-80 control program to maintain compatibility with the IBM 2703.

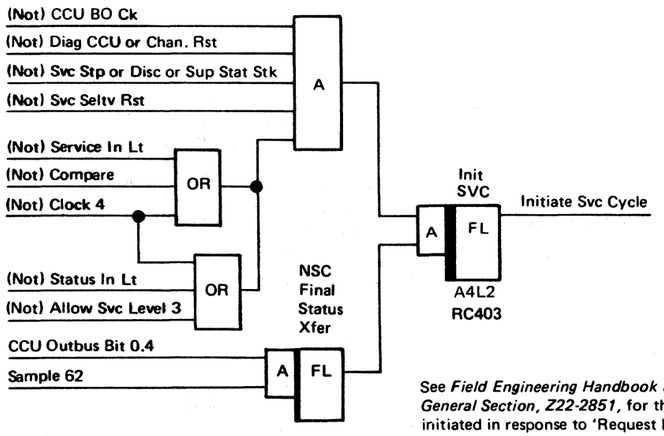
ENDING AN INBOUND TRANSFER (PART 2 OF 3)

NSC

The 3705-80 control program must determine what action to take to end the command. When the 3705-80 control program is ready to present its final status, it executes the following instructions if operating in NSC mode.

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Output X'63'	Address	0000 0000	byte 0 = subchannel address
Output X'66'	0000 0000	0000 1100	1.0 = Attention 1.1 = Status Modifier 1.2 = 0 1.3 = 0 1.4 = Channel End* 1.5 = Device End* 1.6 = Unit Check 1.7 = Unit Exception
Output X'62'	0000 1000	0000 0000	0.4 = Set NSC Final Status Transfer

*This is the normal final status that should be presented. However, the 3705-80 control program can present other bits to designate different conditions if needed.



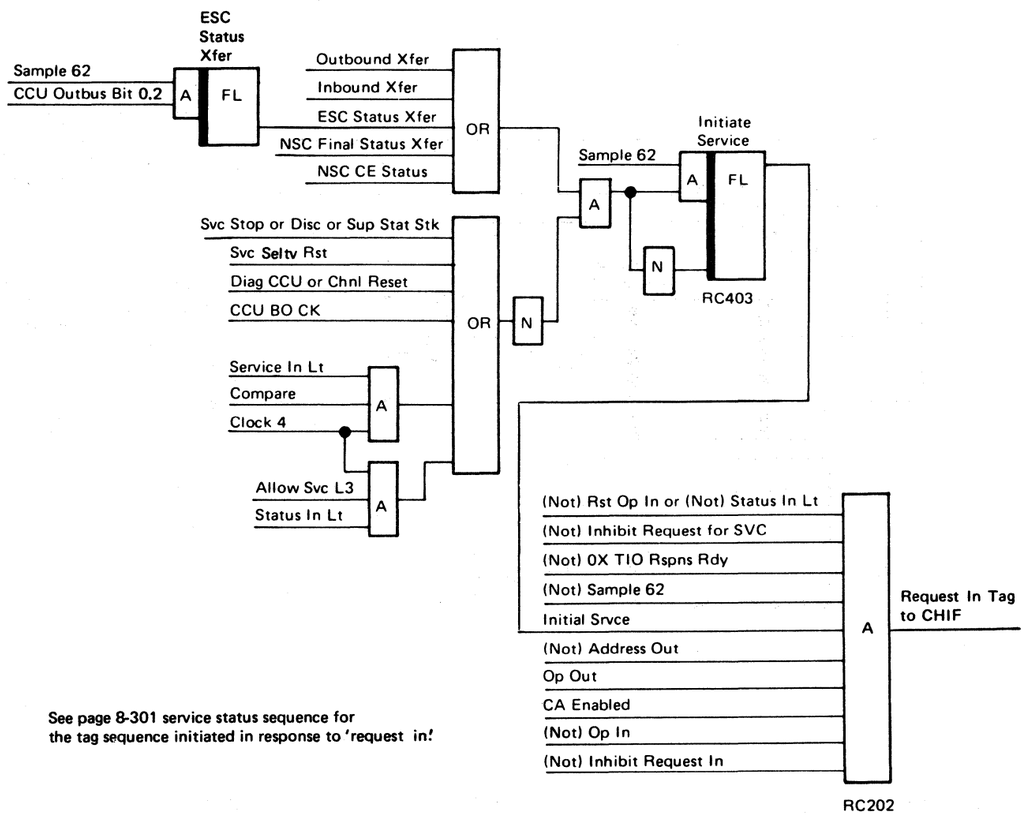
See *Field Engineering Handbook System/360 General Section, Z22-2851,* for the tag sequence initiated in response to 'Request In' from a control unit.

ESC

The 3705-80 control program executes these instructions to present final status if operating in ESC mode.

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Output X'63'	Address	0000 1100	Byte 0 = ESC address 1.4 = Channel End* 1.5 = Device End*
Output X'62'	0010 0000	0000 0000	0.2 = ESC status transfer

*These are the normal final status bits. However, the 3705-80 control program can set other status bits if conditions warrant.

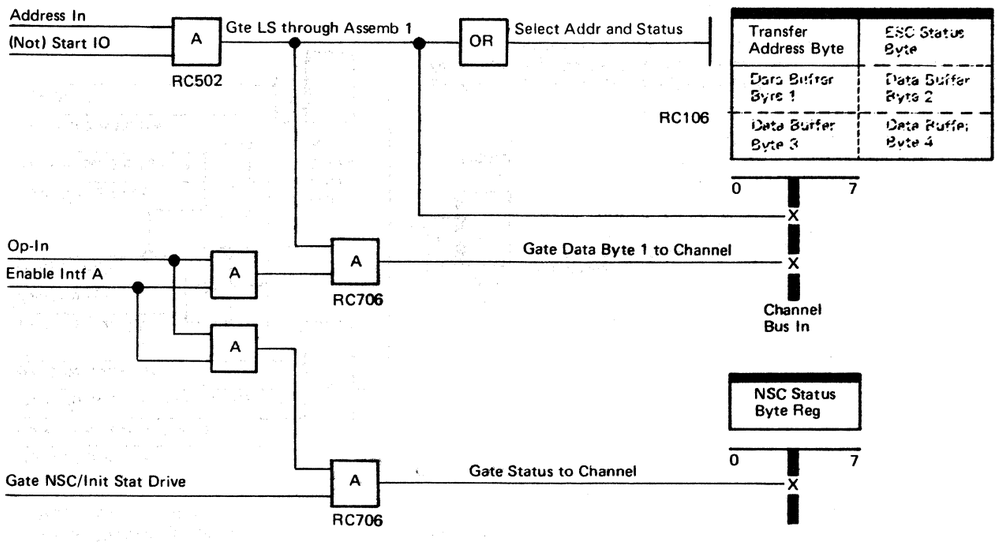


See page 8-301 service status sequence for the tag sequence initiated in response to 'request in!'

ENDING AN INBOUND TRANSFER (PART 3 OF 3)

NSC

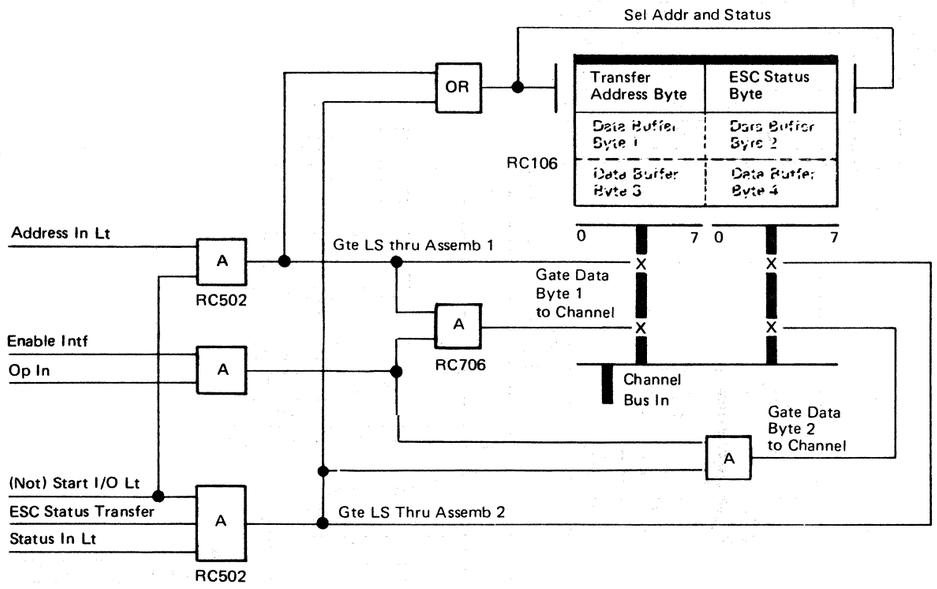
The CA identifies itself to the channel and gates the status byte to the channel 'Bus In'.



'Status in', 'Clock 4' and 'allow svc L3' reset the 'Init Svc' flip latch to request a data/status level 3 interrupt which signals the 3705-80 control program that the status transfer is complete.

ESC

The CA identifies itself to the channel and transfers the final status byte to the channel 'Bus In'.



'Status in', 'Clock 4' and 'allow svc L3' reset the 'Init Svc' flip latch to request a data/status level 3 interrupt which signals the 3705-80 control program that the status transfer is complete.

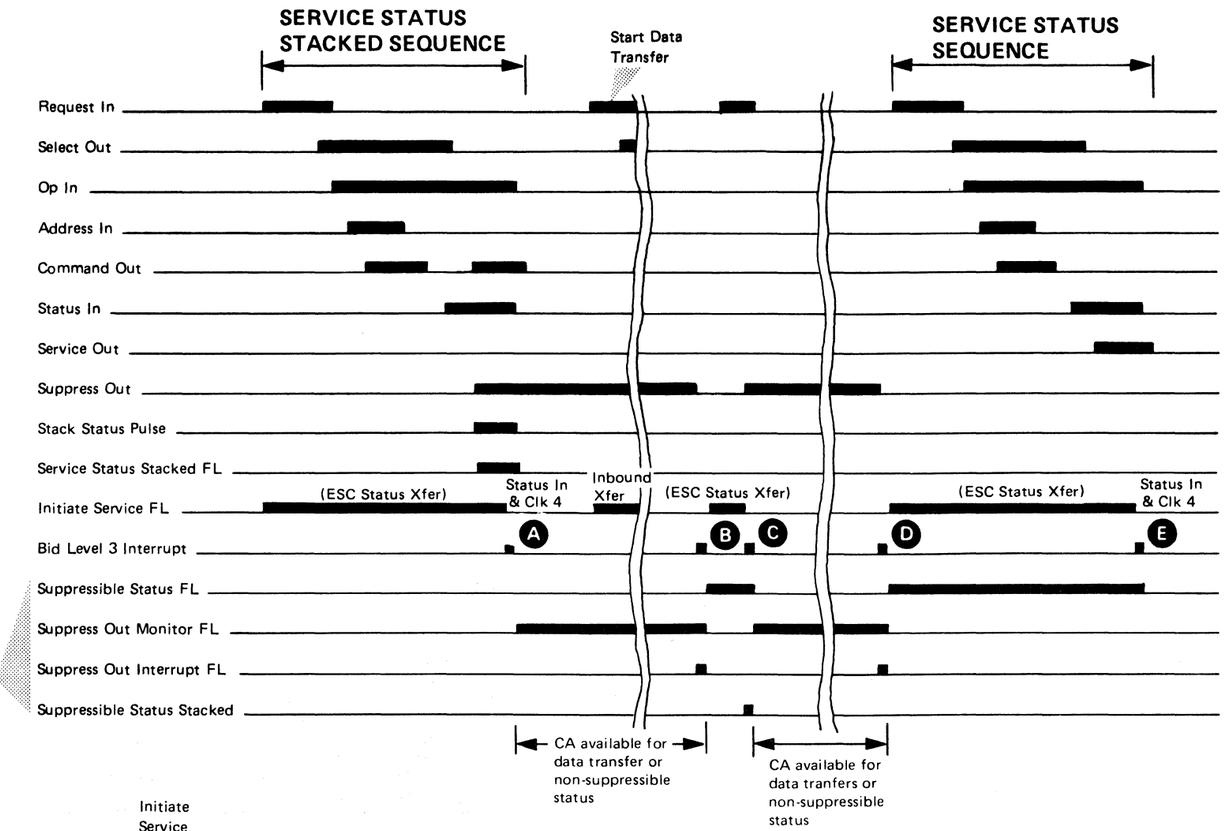
ENDING SEQUENCE WHEN SERVICE STATUS IS STACKED (PART 1 OF 2)

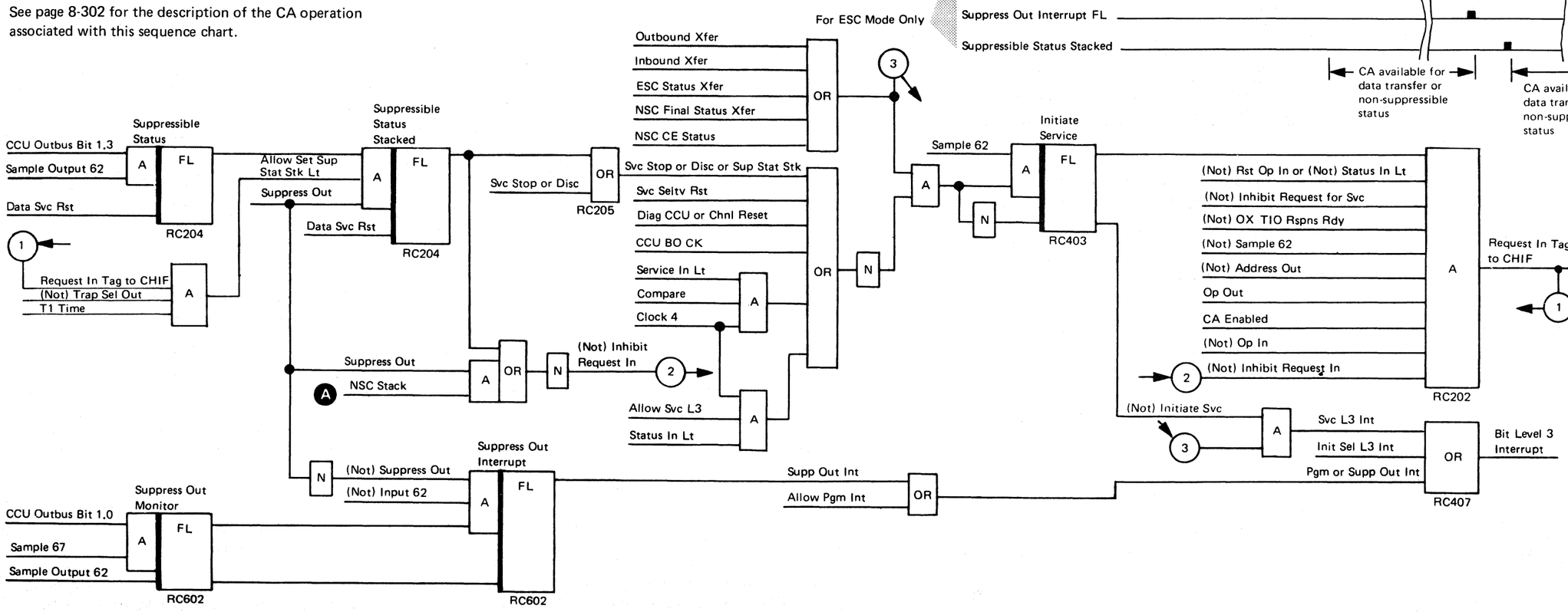
If the channel is unable to immediately handle status from the CA that causes a host processor interruption, the channel responds to 'status in' with 'command out' (stack status) and raises 'suppress out'. Once status is presented to the channel and stacked, it becomes suppressible status. The CA must not present the suppressible status to the channel until the channel drops 'suppress out' to indicate it can handle the status.

When the CA is in NSC mode, the CA hardware inhibits 'request in' until 'suppress out' falls and then presents the suppressible status. (A)

When the CA is in ESC mode, the CA hardware cannot be tied up waiting for 'suppress out' to fall. Data transfers must be allowed to continue for the lines not presenting suppressible ESC status. The fact that 'suppress out' is up does not prevent the channel from servicing data transfers—just suppressible status transfers. The 3705-80 control program determines when 'suppress out' drops and then presents the suppressible status from the stack status queue.

See page 8-302 for the description of the CA operation associated with this sequence chart.





ENDING SEQUENCE WHEN SERVICE STATUS IS STACKED (PART 2 OF 2)

The general sequence of events that occur in the channel interface, the CA, and the 3705-80 control program for ESC mode is shown in the sequence chart on page 8-301.

The 3705-80 control program executes Output X'62' to initiate service. This causes 'request in' to start a service status sequence. 'Status in' resets initiate service causing a type 1 CA level 3 interrupt. The 3705-80 control program must determine that the status has been stacked and that 'suppress out' is up; then turn on the suppress out monitor latch to detect when 'suppress out' is down. The 3705-80 control program executes the following instructions at (A) in the sequence chart. The CA is now available for data transfers or nonsuppressible status for the other ESC lines.

(A)

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0010 0000	0011 0000	0,2 = ESC status transfer 1,2 = Suppress out 1,3 = Service status stacked
Output X'62'	0000 0010	0000 0000	0,2 = 0 to reset ESC status transfer (inhibits a continuous bid level 3 interrupt) 0,6 = Data service reset (resets service status stacked)
Output X'67'	0000 0000	1000 0000	1,0 = Set suppress out monitor

When 'suppress out' falls, the suppress out interrupt latch turns on causing a type 1 CA level 3 interrupt. The 3705-80 control program executes the following instructions at (B) in the sequence chart to start another service status sequence to present the suppressible status to the channel. At the same time, the suppressible status latch is set.

(B)

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0000 0010	0000 0000	0,6 = Suppress out monitor
Output X'62'	0010 0000	0001 0000	0,2 = 1 to set ESC status transfer 1,3 = Set suppressible status Reset suppress out monitor

If for some reason, the channel can not immediately handle any status before it brings up 'select out', the channel raises 'suppress out' again. The suppressible status stacked latch is set when 'request in' and 'suppress out' are up and the suppressible status latch is on. This causes a type 1 CA level 3 interrupt that drops 'request in' and also notifies the 3705-80 control program the channel can not accept the status. The 3705-80 control program executes the following instructions at (C) that set the suppress out monitor latch to detect when 'suppress out' falls. The CA is now available for data transfer or non-suppressible status for the other ESC lines.

(C)

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0010 0000	0011 0000	0,2 = ESC status transfer 1,2 = Suppress out 1,3 = Suppressible status stacked
Output X'62'	0000 0010	0000 0000	0,2 = 0 to reset ESC status transfer (inhibits a continuous bit level 3 interrupt) 0,6 = Data service reset (resets suppressible status) (resets suppressible status stacked)
Output X'67'	0000 0000	1000 0000	1,0 = Set suppress out monitor

When 'suppress out' falls, the suppress out interrupt latch turns on, causing a type 1 CA level 3 interrupt. The 3705-80 control program executes the following instructions at (D) in the sequence chart to start another service status sequence to present the suppressible status to the channel. At the same time, the suppressible status latch is set.

(D)

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0000 0010	0000 0000	0,6 = Suppress out monitor
Output X'62'	0010 0010	0001 0000	0,2 = 1 to set ESC status transfer 0,6 = Data service reset 1,3 = Set suppressible status Reset suppress out monitor

'Status in' resets initiate service causing a type 1 CA level 3 interrupt. The 3705-80 control executes the following instructions at (E) in the sequence chart to determine that the status has been accepted by the channel.

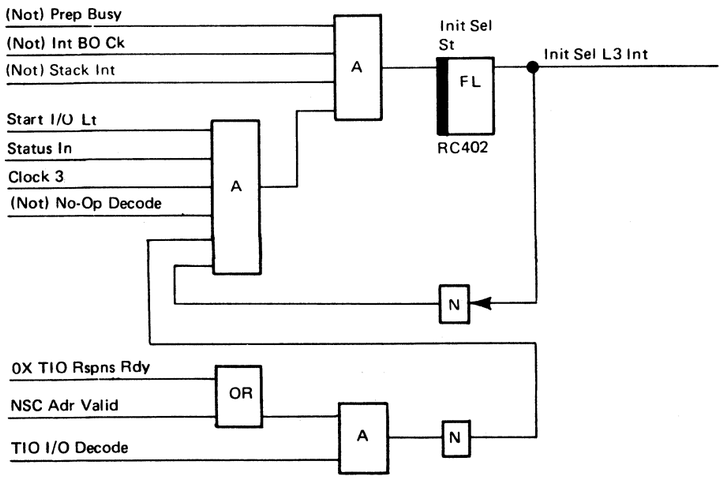
(E)

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	0010 0000	0000 0000	0,2 = ESC status transfer
Output X'62'	0000 0010	0000 0000	0,2 = 0 to reset ESC status transfer (inhibits a continuous bid level 3 interrupt) 0,6 = Data service reset (resets suppressible status)

OUTBOUND DATA TRANSFERS (PART 1 OF 3)

Outbound data transfers result from channel Read commands that direct the transfer of data from 3705-80 storage to the host processor. They are handled by the CA basically the same whether the CA is in ESC or NSC mode. The major difference is the way final status is presented to the channel.

CA Decodes the Command and Requests an Interrupt



The 3705-80 control program responds to the initial select level 3 interrupt with the following instructions.

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0000 1000	Type 1 CA initial selection level 3 interrupt
Input X'60'	1000 0000	0000 0000	Normal initial selection (Note 1)
Input X'61'	address	command	Byte 0 = address byte 1 = command
Output X'63'	address	0000 0000	byte 0 = transfer address byte 1 = all zeros
Output X'64'	data	data	Byte 0 = data byte 1 byte 1 = data byte 2
Output X'65'	data	data	byte 0 = data byte 3 byte 1 = data byte 4
Output X'62'	1000 0110	0000 0000	0.0 = outbound data transfer 0.5 = reset initial selection 0.6 = reset data/status control 1.6-1.7 = 0 to transfer four bytes (Note 2)

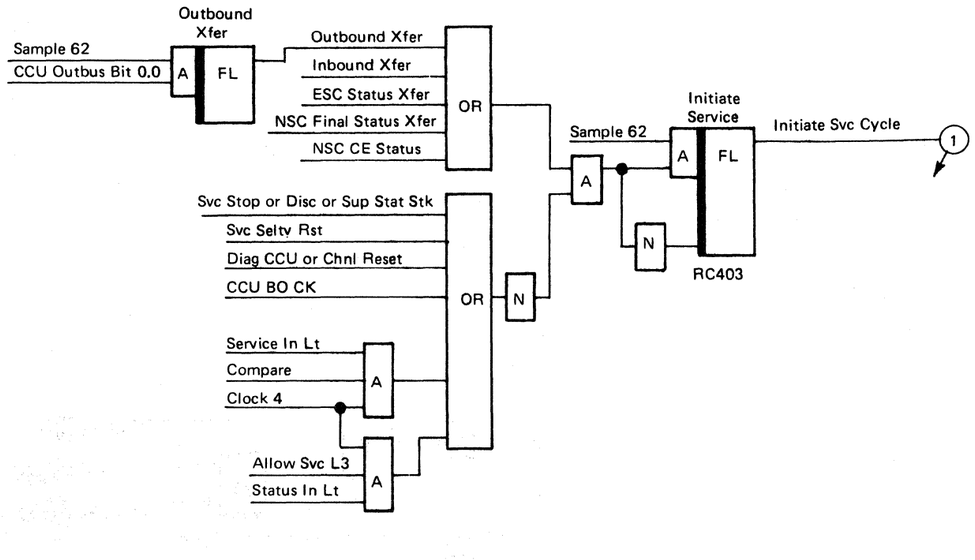
Notes:

1. *Other bits may be transferred to the CCU during this input. If other bits are on, the 3705-80 control program must take action differently from the normal initial selection.*
2. *From one to four bytes of data may be transferred to the channel. If less than four are to be transferred, the Output X'64' and X'65' vary accordingly.*

OUTBOUND DATA TRANSFERS (PART 2 OF 3)

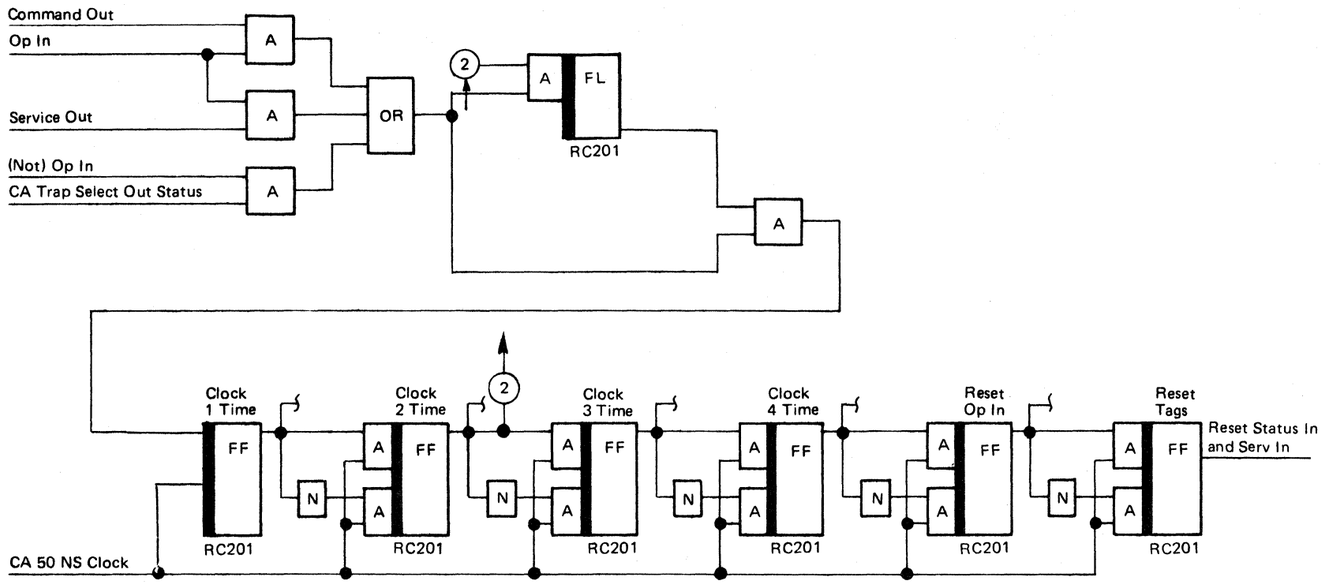
CA and Channel Transfer Data

The Output X'62' instruction starts a channel service cycle so that the data loaded into the data buffer bytes can be transferred to the channel.



See page 8-380 for the tag sequence resulting from 'request in' to the channel. The data is gated on bus in by 'service in' because this is an outbound data transfer instead of an inbound data transfer as shown.

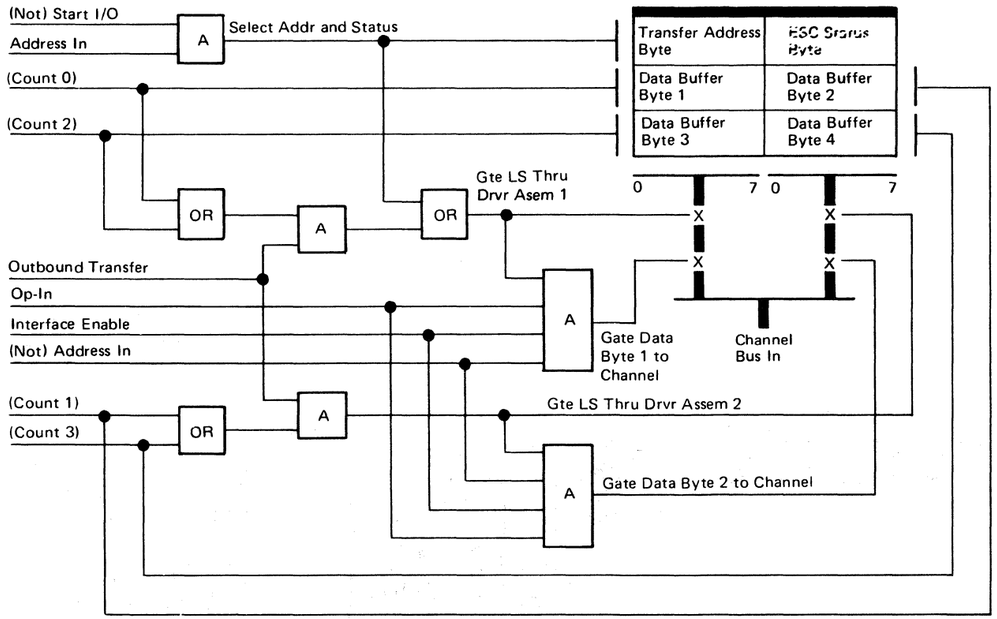
The channel tag clock operates, each time the channel and the CA start a data transfer. The clock synchronizes the CA and the channel to handle the data transfer.

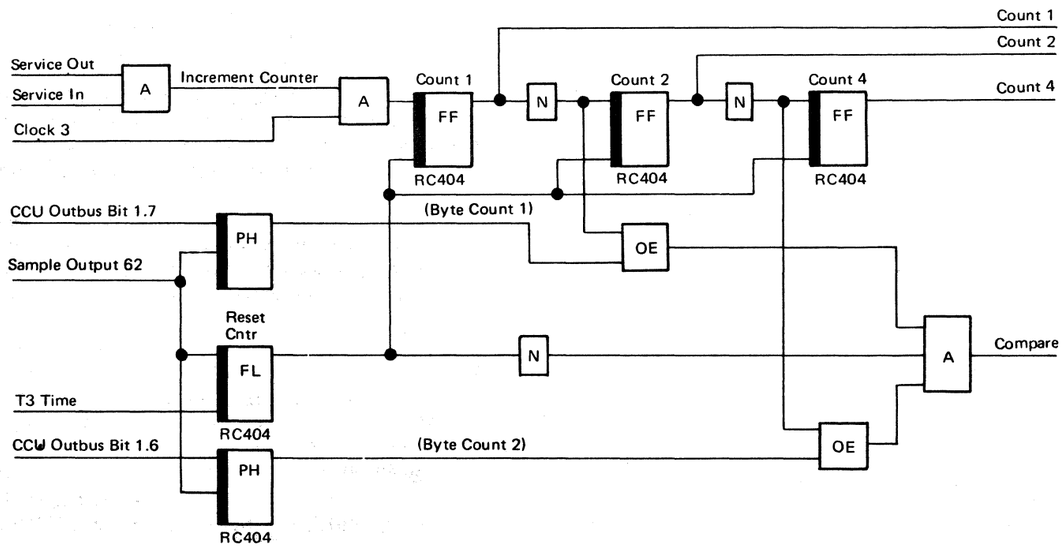


OUTBOUND DATA TRANSFERS (PART 3 OF 3)

CA and Channel Transfer Data (Continued)

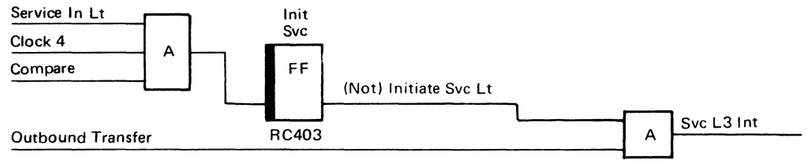
The CA transfers the data to the channel 'Bus In' one byte at a time. As each byte is transferred across the channel interface, the byte count is incremented.





CA and CCU Transfer Data

When the number of bytes transferred across the channel interface equals the number specified in the byte count, the CA requests a type 1 CA data/status level 3 interrupt.



The 3705-80 control program responds to the level 3 data/status interrupt with the following instructions.

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0001 0000	Type 1 CA data status level 3 interrupt
Input X'62'	1000 0000	0000 0100	0.0 = outbound data transfer 1.5 = number of bytes transferred in (four indicated by bit 1.5)
Output X'64'	Data byte	Data byte	Byte 0 = data byte 1 Byte 1 = data byte 2
Output X'65'	Data byte	Data byte	Byte 0 = data byte 3 Byte 1 = data byte 4
Output X'62'	1000 0010	0000 0000	0.0 = outbound data transfer 0.6 = reset data service condition 1.6 and 1.7 off indicate transfer in four bytes.

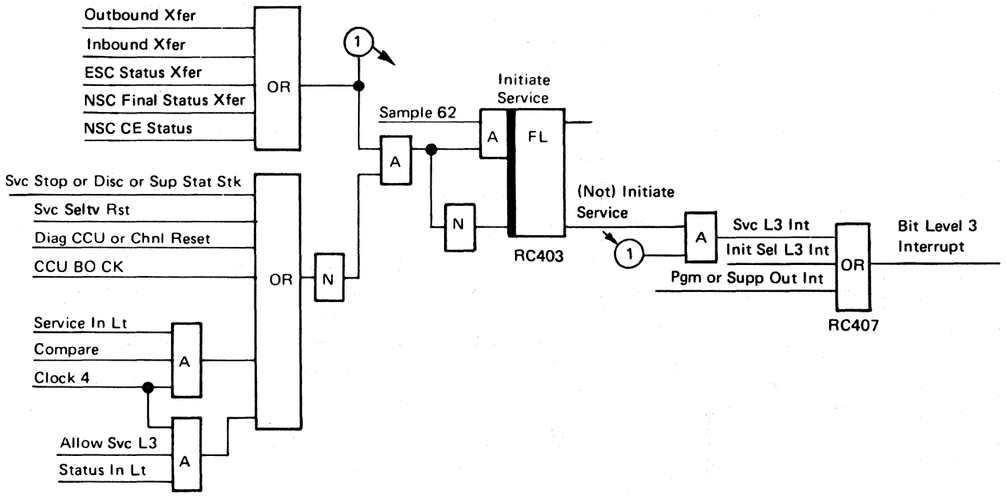
ENDING AN OUTBOUND TRANSFER (PART 1 OF 2)

Outbound data transfers can be ended either by the host processor or the 3705-80 control program. The host processor ends the transfer by initiating a channel stop sequence or with a Halt I/O. The 3705-80 control program ends the transfer by initiating a status transfer rather than a data transfer.

Note: *There are some differences in the NSC and ESC status presentation. Where differences exist, NSC information appears on the left, and ESC information appears on the right of the page.*

Channel Initiates a Channel Stop

When the host processor has transferred all the data it has to transfer with the active command, it begins a channel stop sequence to signal the 3705-80.



The 3705-80 control program responds to the data/status level 3 interrupt with the following instructions.

Instruction	*General Register Bits* *Byte 0*	*Byte 1*	*Indication or Function*
Input X'77'	0000 0000	0001 0000	Type 1 CA data/status level 3 interrupt
Input X'62'	1000 0100	000G 0XXX	0.0 = Outbound transfer 0.5 = Channel Stop or Intf disconnect 1.5-1.7 = Number of bytes transferred
Input X'61'	Address	Command	Byte 0 = last address presented to the CA* Byte 1 = last command presented to the CA*
Input X'63'	Address	0000 0000	Byte 0 = address CA was serving when channel stop occurred Byte 1 = should be all zeros unless a status byte was loaded into the register.

* If the CA received a new channel command while still processing the previous command, the contents of the initial selection address and command byte register change to reflect the new command and address. The Input X'63' provides the address that was being served when the stop sequence occurred.

ENDING AN OUTBOUND TRANSFER (PART 2 OF 2)

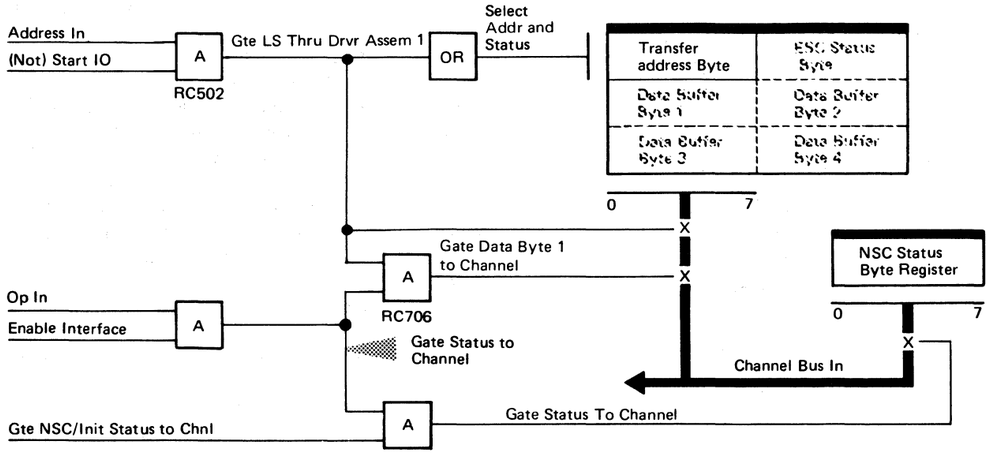
NSC

The 3705-80 control program executes the following instructions to present the final status to the channel.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Output X'63'	address	0000 0000	Byte 0 = Subchannel address whose status is being presented. (Note 1)
Output X'66'	0000 0000	0000 1100	1.0 = Attention 1.1 = Status Modifier 1.2 = * (Not used) 1.3 = * (Not used) 1.4 = Channel End (Note 2) 1.5 = Device End (Note 2) 1.6 = Unit Check 1.7 = Unit Exception
Output X'62'	0000 1000	0000 0000	0.4 = Set NSC final status transfer.

Notes:

1. *In NSC mode, this address should not change from transfer to transfer. The 3705-80 control program may not need to reload the address into this register after it has been loaded correctly the first time.*
2. *This is the normal final status that should be presented to the channel. However, the 3705-80 control program can determine whether additional status bits should be presented.*



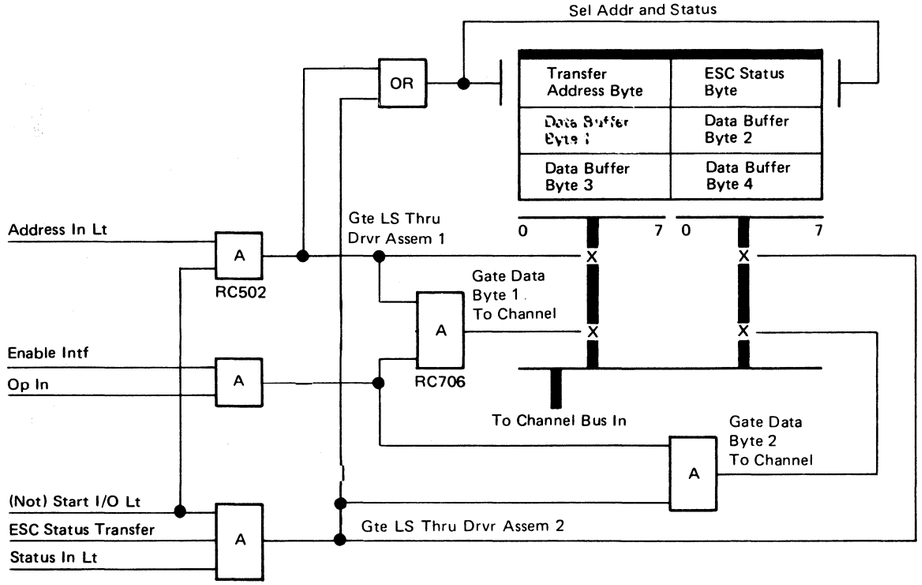
'Status In', 'Clock 4', and 'allow svc L3' reset the 'Init Svc' flip latch to request a data/status level 3 interrupt which signals the 3705-80 control program that the status transfer is complete.

ESC

The 3705-80 control program executes the following instructions to present the final status to the channel.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Output X'63'	address	0000 1100	Byte 0 = subchannel address to which the status is to be presented. 1.0 = Attention 1.1 = Status Modifier 1.2 = Control Unit End 1.3 = Busy 1.4 = Channel End (See Note) 1.5 = Device End (See Note) 1.6 = Unit Check 1.7 = Unit Exception
Output X'62'	0010 0000	0000 0000	0.2 = ESC status transfer

Note: *This is the normal final status to present to the channel. However, the 3705-80 control program can determine if other bits should be presented.*



'Status In', 'Clock 4', and 'allow svc L3' reset the 'Init Svc' flip latch to request a data/status level 3 interrupt which signals the 3705-80 control program that the status transfer is complete.

CA ERROR INTERRUPTS

The type I channel adapter requests a level 1 interrupt whenever:

- A channel 'Bus-In' check occurs.

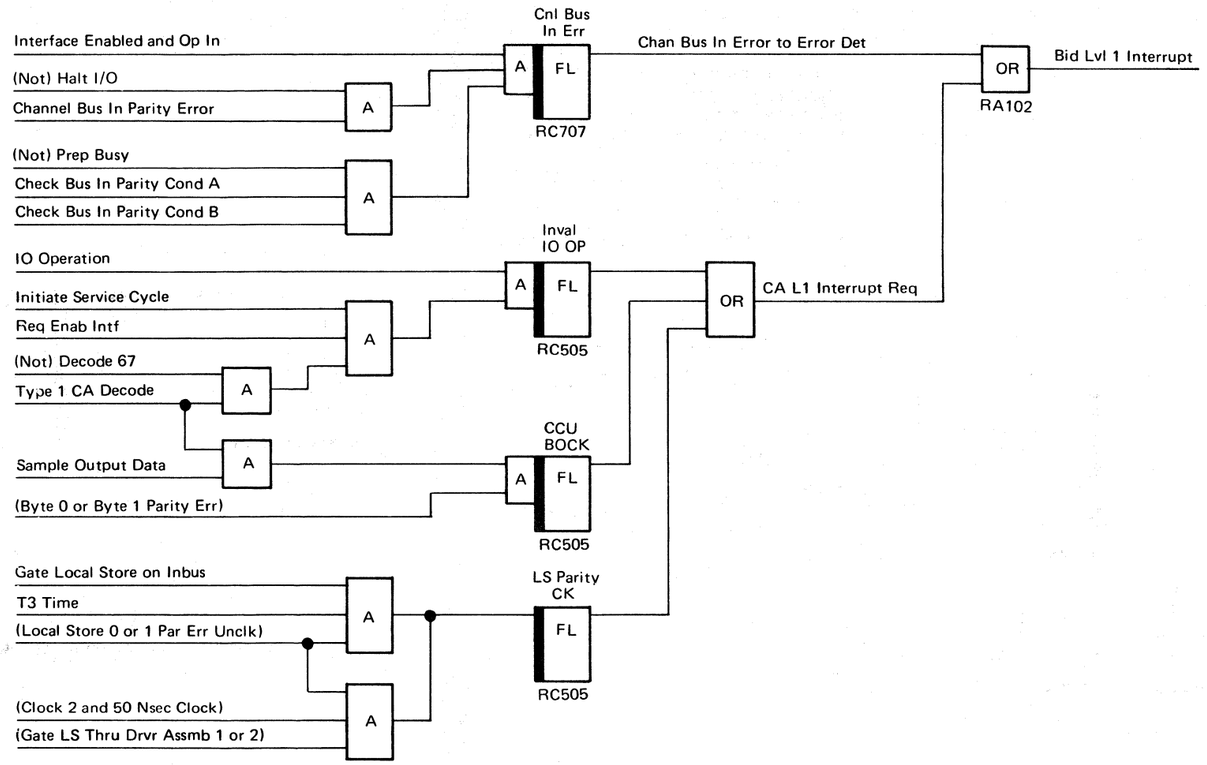
  The channel adapter hardware detects bad parity in the data byte being sent across the channel to the processor.

  The control program should respond to the interrupt with an Input X'67' instruction to transfer the contents of the error condition register to the CCU. Bit 1.0 should be transferred if a channel 'Bus-In' check occurred.
- An in/out instruction accept check occurs.

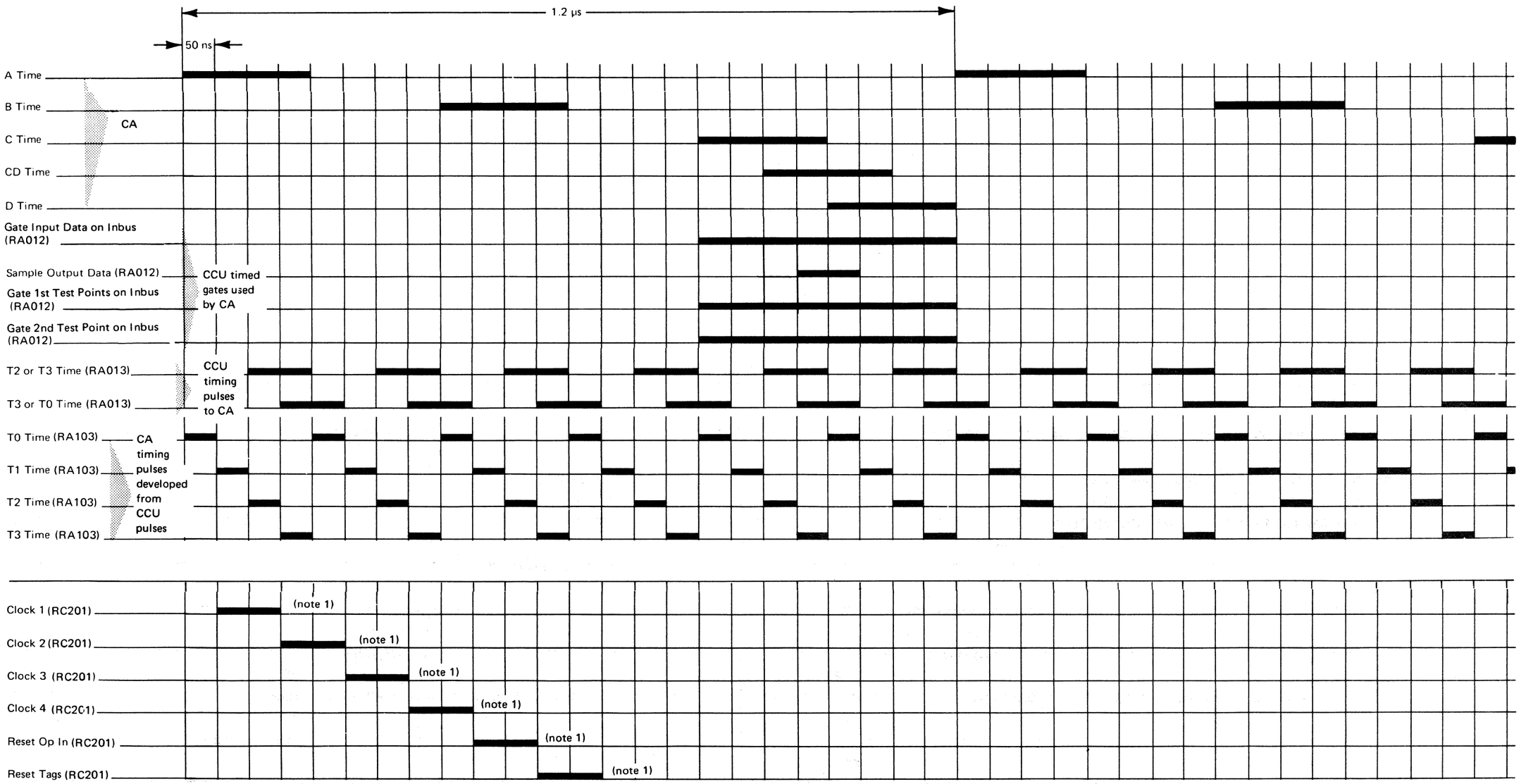
  An in/out instruction accept check (invalid I/O op) occurs if the control program executes an Input or Output X'60', X'61', X'62', X'63', X'64', X'65', or X'66' instruction while the CA is actively handling any data or status transfer sequence. When the control program responds to the level 1 interrupt with an Input X'67', bit 1.1 is transferred to the CCU.
- A 'CCU Outbus' check occurs.

  When bad parity is detected on the 'CCU Outbus', the CA requests a level 1 interrupt. Bit 1.2 is returned to the CCU from the error condition register when the control program executes an Input X'67' instruction in response to the interrupt.
- A local store check occurs.

  Bad parity being gated from the local store registers causes a level 1 interrupt request. Bit 1.3 is returned to the CCU from the error condition register when the control program executes an Input X'67' instruction in response to the interrupt.



CA TIMING

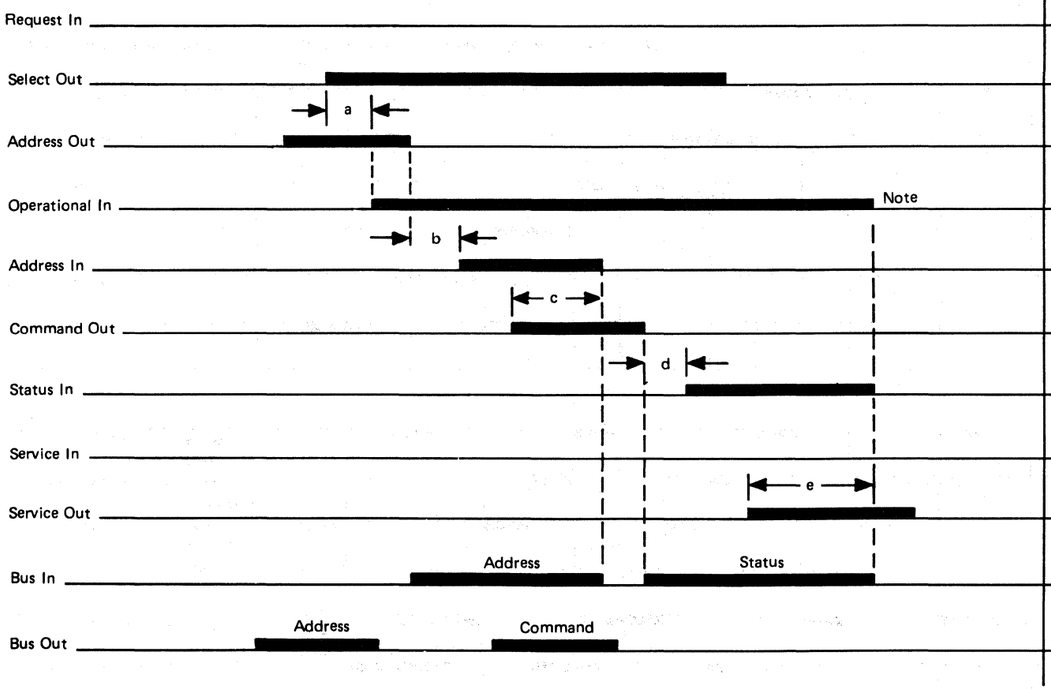


Note:

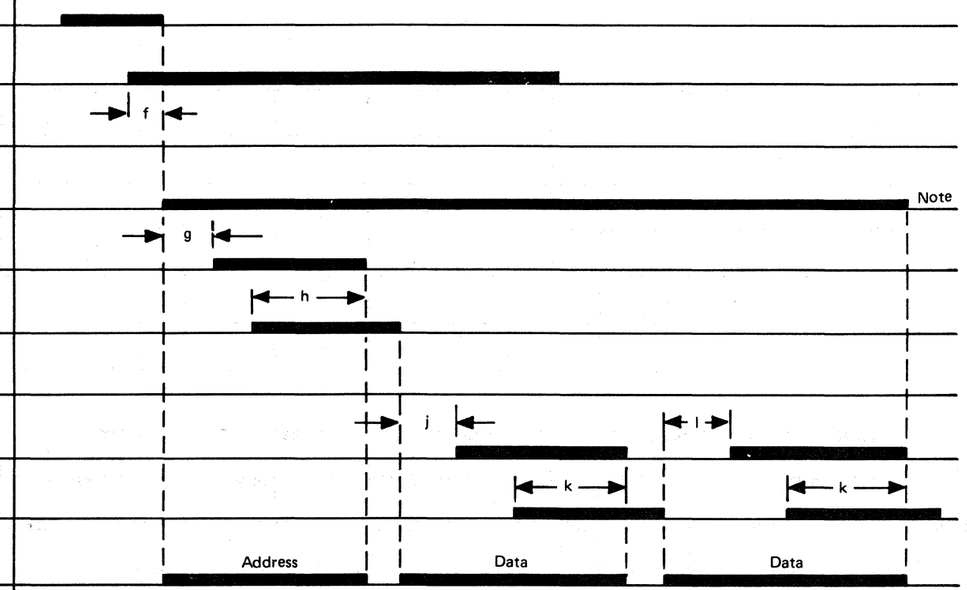
1. Clock times are not related to A, B, etc time, and clock times occur on either T1 or T3 time.

CHANNEL INTERFACE SEQUENCES

INITIAL SELECTION SEQUENCE



SERVICE INBOUND DATA SEQUENCE
(See 8-301 for service status sequence)



a	-	Rise of 'select out' inbound to rise of 'operational in'	200-350ns
b	-	Rise of 'address in' after the fall of 'address out'	300-350ns
c	-	Fall of 'address in' after the rise of 'command out'	400-500ns
d	-	Rise of 'status in' after the fall of 'command out'	300-350ns
e	-	Fall of 'status in' after the rise of 'service out'	500-600ns
f	-	Fall of 'request in' after the rise of 'select out' inbound	200-350ns
		Rise of 'operational in' after the rise of 'select out' inbound	200-250ns
g	-	Rise of 'address in' after the rise of 'operational in'	350ns
h	-	Fall of 'address in' after the rise of 'command out'	400-500ns
j	-	Rise of 'service in' after the fall of 'command out'	300-350ns
k	-	Fall of 'service in' after the rise of 'service out'	500-600ns
l	-	Rise of 'service in' after the fall of 'service out'	300-350ns

Note: *'Operational in' falls as shown provided 'select out' is down. If 'select out' is up when 'status in' or 'service in' falls, 'operational in' falls with the fall of 'select out'.*

Type 2 Communication Scanner (Part 1 of 2)

INTRODUCTION

The type 2 communication scanner provides the interface between the line attachment hardware (line or autocall interfaces) and the CCU. The primary function of the scanner is to monitor the communication lines for service requests. A single type 2 scanner is installed in the 3705-80, as indicated in the type 2 scanner configuration diagram. The scanner supports both synchronous and asynchronous half-duplex and duplex *lines* operating at various line speeds. For each line interface, the control program initializes the line type (BSC, start-stop, autocall), character length, type of bit clocking (business machine or modem), bit clocking speed for business machine clocking, and interrupt priority.

Functions of the Type 2 Scanner

The type 2 scanner:

- Scans the line/autocall interface addresses in the LIB positions it supports.
- Performs character assembly/disassembly
- Provides character buffering
- Signals program level 2 interrupts to the attachment base when program service is required—such as character service.
- Provides bit clock addresses for the LIB positions it supports so the LIB can generate the strobe pulse for receive operations.
- Provides up to four oscillators that generate business machine transmit and receive pulses for use by the line/autocall interfaces.
- Signals program level 1 interrupts for failures in the scanner, LIB, and line/autocall interface. The cause of the level 1 interrupt is buffered in the check register.
- Monitors the state of certain carrier equipment and autocall unit lines for interfaces that are selected by the control program and buffers the state in the display register where the program may display it on the control panel.

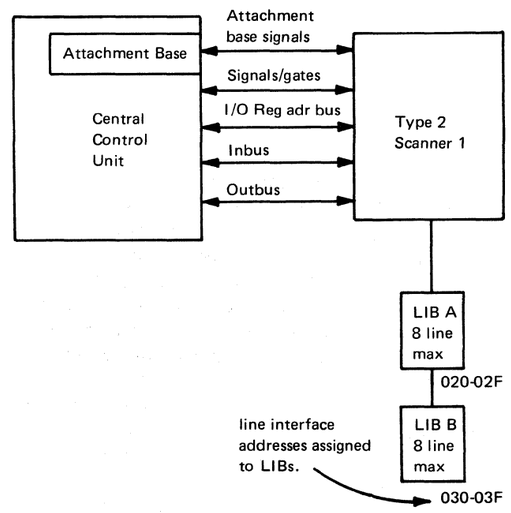
Attachment Base

The attachment base provides common interface controls to the central control unit and line addressing controls for the type 2 scanner and is contained on two cards located at A-B3D2 and A-B3E2 (see B-030).

The attachment base:

- Generates line interface addresses for the type 2 scanners for scan addressing
- Performs address substitution under program control
- Provides a buffer for the interface address for program addressing
- Provides the mechanism for buffering program level 2 interrupts by priority.

TYPE 2 SCANNER CONFIGURATION



Scanner Initialization

The scanner and its associated LIBs are placed in a disabled state (1) during a power-on sequence, (2) during an IPL, (3) by a control panel reset, or (4) during the execution of an Output X'43' when the general register specified by the R field contains appropriate bits. The control program must *enable* each scanner by executing Output X'43' with bits 0.1 = 1 and 1.6 = 1 before the control program can initialize each ICW (interface control word) and the associated line or autocall interface. This initialization must occur before the line interface can be placed in operation.

Interface Control Word

The ICW provides the normal communications link between the control program and the scanner, and between the control program and the interface hardware. The scanner contains 32 ICWs, one for each of the line/autocall interfaces that may be attached. Certain fields within the ICW are used to buffer information about the interface between successive scans.

The ICW:

- Buffers and serializes the character to be transmitted
- Deserializes and buffers the received character
- Buffers the autocall digit
- Buffers the status of autocall lines
- Buffers the mode of operation
- Buffers the status of the operation
- Is used to initialize the line interface hardware and the scanner operation for that interface.

TYPE 2 COMMUNICATION SCANNER INTRODUCTION (PART 2 OF 2)

Program Addressing

The control program accesses the ICW or scanner during that part of the scanner cycle called CCU time. During CCU time, the scanner implements the input and output instructions (see Input/Output section) that apply to that scanner. During this time, the interface address in ABAR (attachment buffer address register) accesses the associated ICW and selects the scanner. The control program executes input instructions to obtain the status of this ICW, or executes output instructions to change the contents of this ICW.

The control program also executes input instructions to obtain (1) the interface address in ABAR, (2) the status of the check register, and (3) the status of the display register.

The control program also executes output instructions to (1) set the interface address in ABAR, (2) set the state of the substitution control register, (3) set the state of the upper scan limit latches in the scanner, (4) enable or disable the LIB or scanner, or (5) set or reset the scanner control functions.

Scan Addressing

The scanner services the line/autocall interface during that part of the scanner cycle called CSB time. During CSB time, the scan counter in the attachment base provides an interface address to the scanner for scan addressing. The scanner uses the interface address to access the corresponding line/autocall interface and the associated ICW. The scanner receives the status of the line/autocall interface and determines if a bit service request is active. If a request is active, the scanner, under control of the primary control field in the ICW, performs the bit service operation and updates the ICW content. The scanner signals a character service level 2 interrupt when appropriate. If the scanner does not detect a bit service request, the bit service operation does not occur.

The scan counter furnishes 96 discrete interface addresses to the scanner. The address substitution mechanism in the attachment base can modify certain addresses before they are sent to the scanners. The scanner contains an upper scan limit mechanism for modifying the interface address received from the attachment base. Modification only occurs during scan addressing. Address substitution and upper scan limit modification are both under control of the program.

Level 1 Interrupts

Failures in the scanner can affect all communication lines attached to the 3705-80, or can affect at least a group of lines within a particular LIB. The detection of one or more of the failures is indicated by a type 2 scanner n level 1 interrupt request. The scanner contains a check register which buffers the condition that causes the level 1 interrupt.

Transmit Operation

The program initializes the operation and places the first character into the SDF (serial data field) and the second character into the PDF (parallel data field) of the ICW associated with that line interface. The SDF serializes the character and sends it to the line interface a bit at a time under control of the bit service request from the line interface. The line interface then sends the bits to the modem or transmission line under control of the transmit oscillator located in the scanner or external clock in the modem. The control program must furnish all the data to be transmitted (such as line control, initial SYN and PAD, and response characters). The scanner only adds the start and stop bits for start-stop operations.

When the character has been transmitted, the scanner requests a level 2 interrupt to signal the control program that another character can be sent to the scanner. The scanner transfers the next character from the PDF to the SDF so transmission can continue while the control program (1) loads the next character into the PDF, or (2) signals the scanner that the last character has been transmitted by changing to transmit turnaround mode.

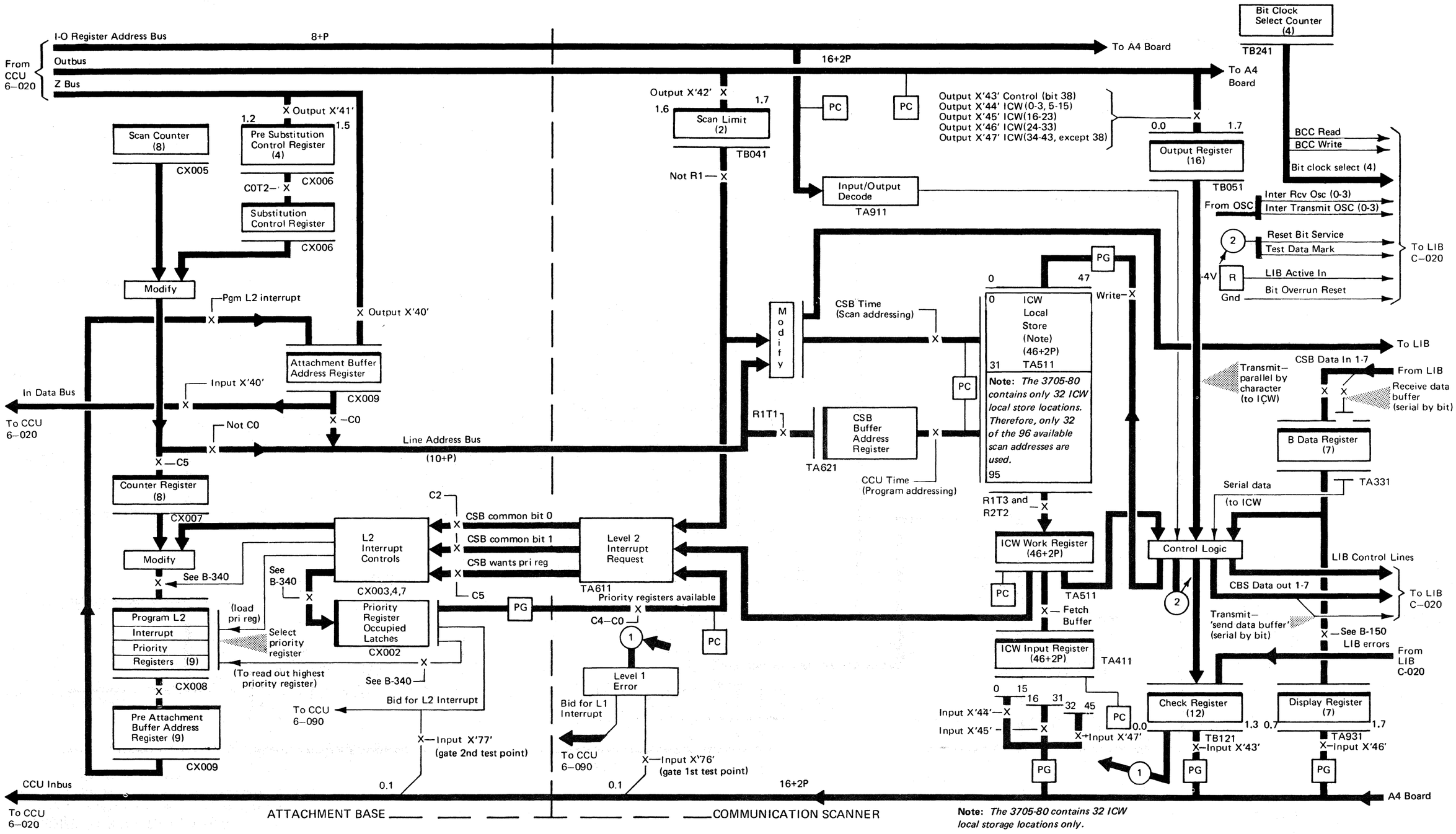
Receive Operation

The line interface receives the bits from the modem or transmission line. The line interface strobes the bits into its receive buffer. The strobe is under control of the bit clock control (located in the LIB) for business machine clocking. The scanner contains the receive oscillator that controls the bit clock circuit in the LIB. The modem receive clock pulses generate the strobe pulses when external clocking is specified by the control program for synchronous operation. In either case, the strobe generates a bit service request in the line interface which signals the scanner that the receive buffer contains the received bit. The scanner places the bits into the SDF until a character has been assembled and then transfers the character to the parallel data field. The scanner strips the start and stop bits off the character and then causes a program level 2 interrupt. The control program can execute an input instruction to obtain the character in the PDF.

The only character the scanner recognizes is the first SYN character used for phase initialization in synchronous operation. The second SYN character must be recognized by the control program before 'character phase' is identified by the program. If the second character is not the SYN character, the control program changes the operating mode from receiving to monitoring, and the search for character phase resumes.

The control program determines when an ending character or sequence has been received and changes the operating mode accordingly.

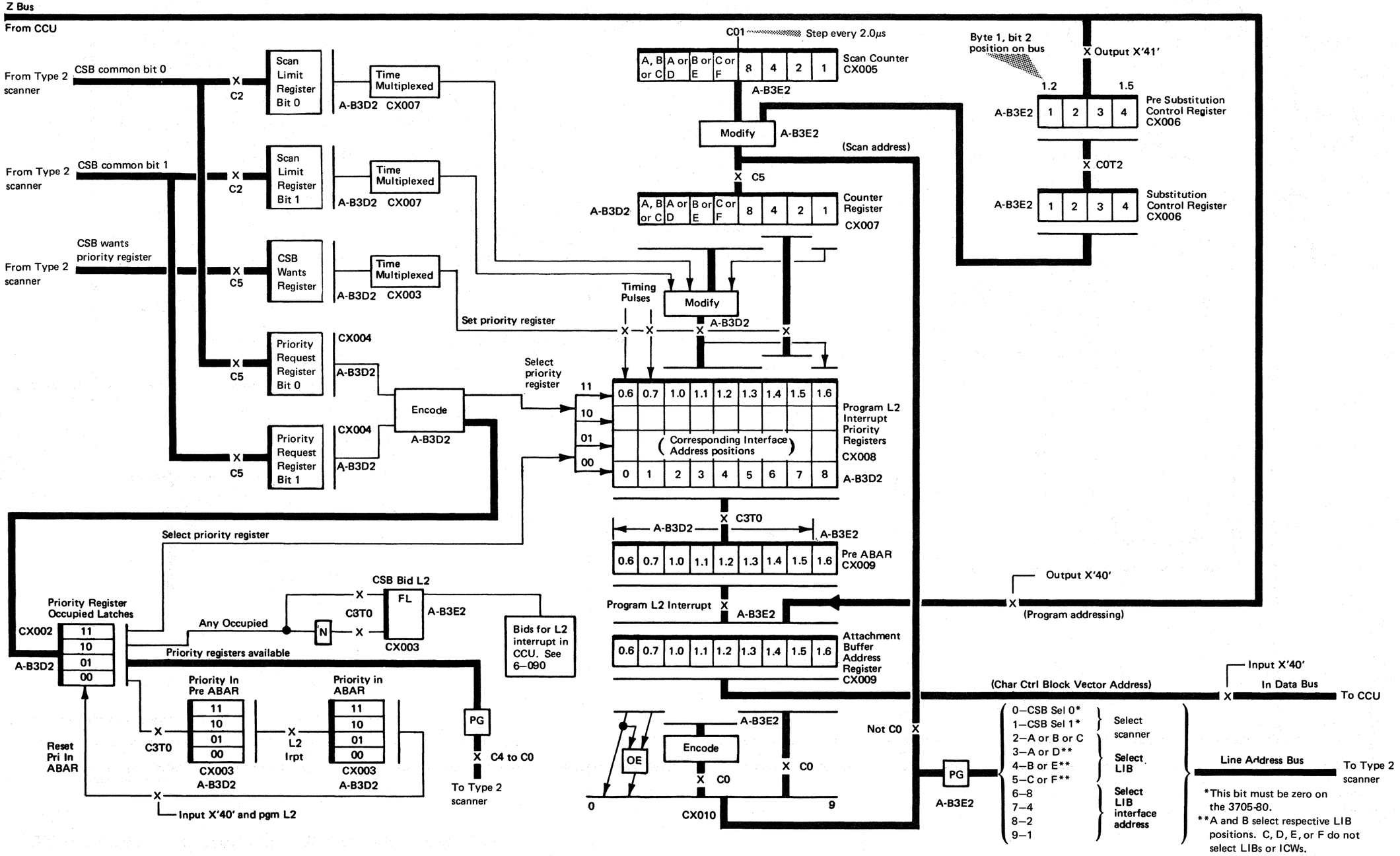
ATTACHMENT BASE AND COMMUNICATION SCANNER DATA FLOW



Note: *The 3705-80 contains 32 ICW local storage locations only.*

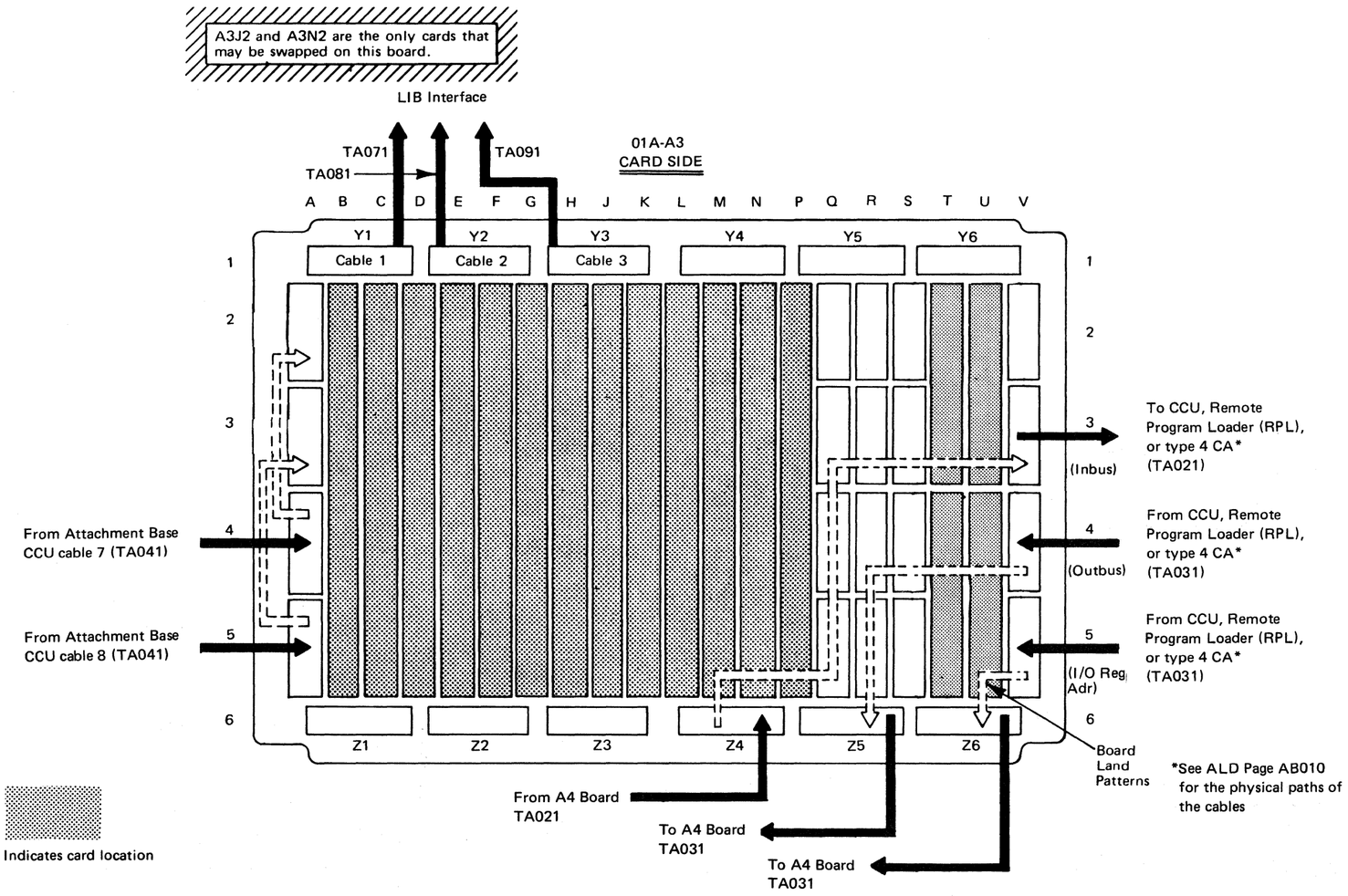
ATTACHMENT BASE DATA FLOW

The logic for the attachment base is located on two MST cards A-B3D2 and A-B3E2. The logic is distributed between the cards as indicated on this page.



TYPE 2 COMMUNICATION SCANNER BOARD LAYOUT

Card Location	*ALD Page*	*Function*
A3B2	TB211	Inbus powering
	TB231	Dial inputs to SDF
	TB231	Work register gate
	TB241	BCC Drive
A3C2	TB111	Mask LIB errors
	TB121	BCC errors
	TB131	Check register
	TB141	Ser L1 interrupt
	TB141	POR latch
	TB141	POR or sel LIB reset
	TB151	Gate test points CSB errors
	TB161	Check register parity
	TB161	Inbus parity bit
A3D2	TA911	Input-Output decode
	TA921	I.W. output remember latches
	TA931	Display register
	TA941	CSB clock
A3E2	TA311	Data out 7
	TA311	Test data
	TA321	Ctrl out A and B
	TA321	Ctrl in A and C
	TA331	B data register
	TA341	Feedback check
	TA341	Data in 1-7
	TA341	Modem rec space/DPR
	TA361	Bit service reset
	TA371	Ctrl in/out termination
A3F2	TA811	New PCF
	TA811	PCF decode
	TA821	Set PCF states 0-4-5-6-9-C
	TA831	Interrupt Go
	TA841	Set LCD C, D
	TA841	Set PCF state 7
	TA851	SDF 0-8 is empty
A3G2	TB011	Ones CTR & last line state
	TB011	Insert/Delete 0
	TB011	Flag/Abort detect
	TB011	NRZI encode
	TB031	Outreg
	TB041	Upper scan limit latches
	TB051	New bit
	TB061	Display request
A3H2	TA211	SDF update controls
	TA221	SDF direct update
	TA221	SDF shift update
	TA231	SDF output update
	TA231	PDF update
	TA261	Tag generation
	TA261	Tag detection
	TA271	New SDF
A3J2	TA545	ICW local store 23-44, P2
	TA565	ICW local store parity error
	TA571	ICW local store parity generation
A3K2	TA411	Input register
	TA451	Parity generation and check
A3L2	TA611	Interrupt generation
	TA611	Priority Available
	TA621	CSB BAR and parity check
	TA631	LIB select
	TA621	Address select
	TA651	Address parity and check



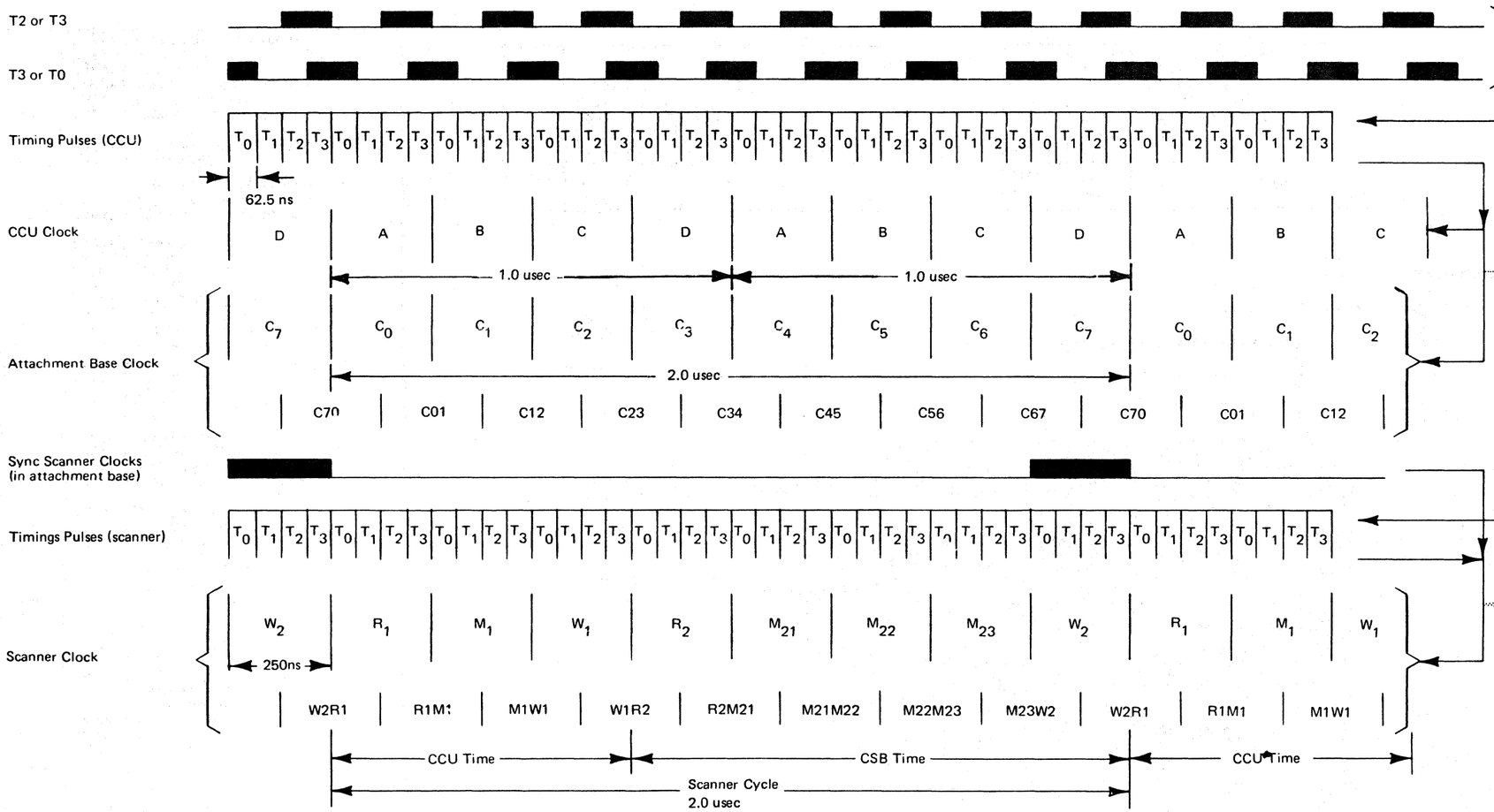
Card Location	*ALD Page*	*Function*
A3M2	TA711	SDF to PDF 4-5-6-7-8 bit transfer
	TA731	PDF direct
	TA731	Out reg to PDF
	TA741	New PDF
	TA761	Data out 1-2-3-4-5-6

Card Location	*ALD Page*	*Function*
A3N2	TA511	ICW local store 0-22, P1
	TA531	ICW local store parity error
	TA535	ICW local store parity generation
A3P2	TA111	LCD decode and update
	TA121	New SCF 0-7
	TA121	Sw-line security
	TA151	LCD, PCF powering

Card Location	*ALD Page*	*Function*
A3T2	TB411*	Internal Xmt-Rcv Oscillator 0
A3T4	TB412*	Internal Xmt-Rcv Oscillator 1
A3U2	TB413*	Internal Xmt-Rcv Oscillator 2
A3U4	TB414*	Internal Xmt-Rcv Oscillator 3

*Contains card P/N by bit rate

CLOCK AND TIMINGS – STORAGE



Basic CCU timing pulses generate timing pulses T0-T3 in CCU and scanner

CCU timing pulses generate clocks in CCU and attachment base

Note: *The attachment base clock and the scanner clock are SYNCHRONOUS with each other.*

Scanner clock is generated by the 'sync scanner clock' and the scanner timing pulses

Note: *The CCU clock and the attachment base clock are SYNCHRONOUS with each other.*

CCU Time – Program addressing occurs as described on B-010 and B-290. ABAR supplies the address of the ICW that the control program wants to input or output.

R1 – ICW local store read out

M1 – ICW content modified as required by an Input or Output instruction.

W1 – Modified ICW contents written into ICW local store

CSB Time – Scan addressing occurs as described on B-010 and B-220. The scanner uses the address from the scan counter to determine the state of a line on the scanner and to modify the contents of the associated ICW, if required, if bit service request is active.

R2 – ICW local store read out

M21, M22, M23 – ICW contents modified as required if bit service request is active from the interrogated line.

W2 – Modified ICW contents written into ICW local store

ICW CONTROL AND DATA FIELDS

See B-090 for the ICW associated with the autocall interface.

The ICW (interface control word) is the link between the control program and the type 2 scanner, and between the type 2 scanner and the interface hardware. In addition, certain fields within the ICW are used to buffer information about the interface between successive scans.

The ICW is made up of 46 information bits and 2 parity bits and is physically located in the scanner local store. The scanner contains one ICW for each possible interface that can be attached. The ICW local store contains 32 ICWs, however, only those ICWs associated with an attached interface should be addressed by the control program. The scanner still scans those ICWs that are not associated with an attached interface but are within the range of addresses controlled by the upper scan limit and substitution control register.

PDF (Parallel Data Field)

An eight bit character buffer in the data flow between the program and the ICW serial data field.

SCF (Secondary Control Field)

See B-061 for bit definitions.

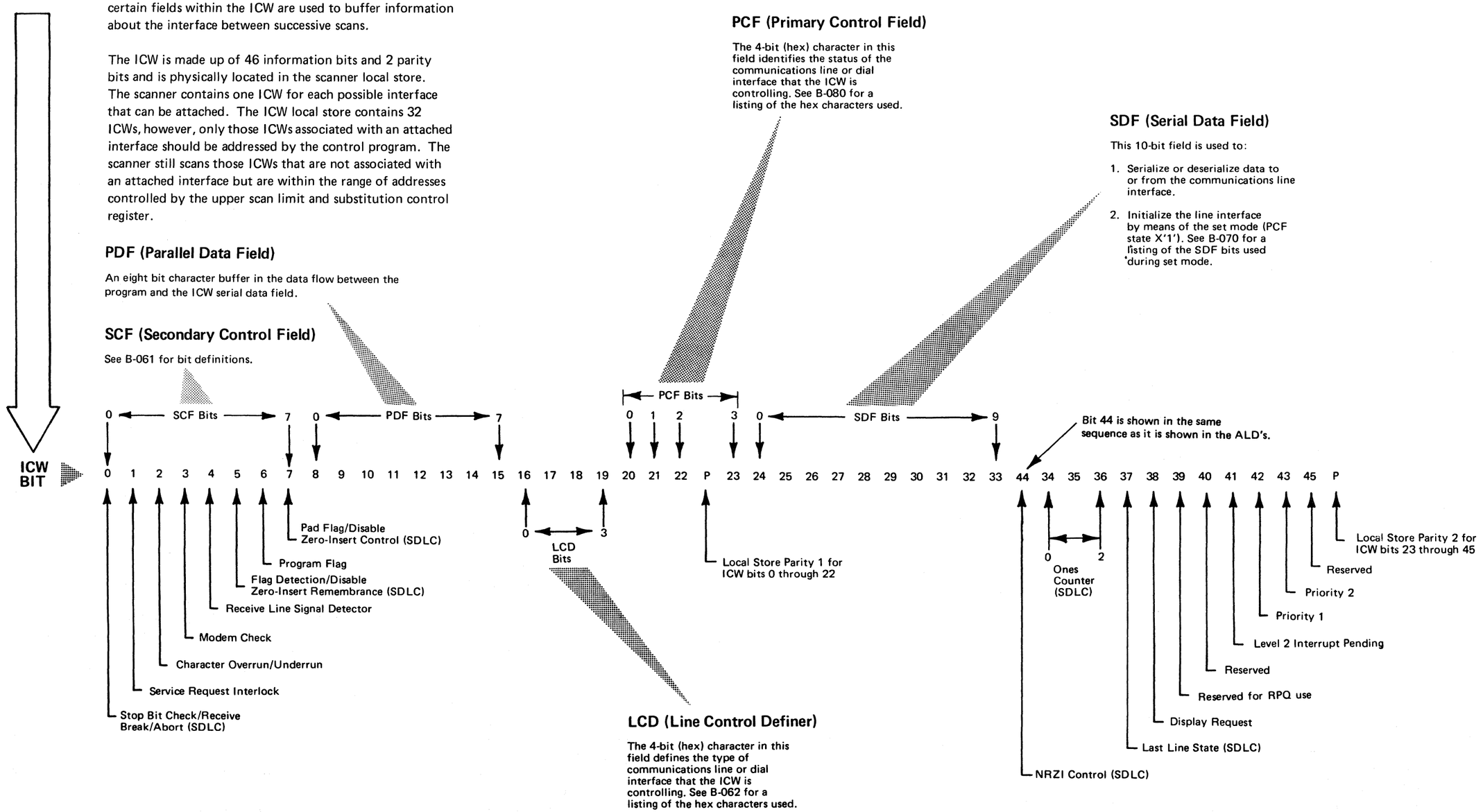
PCF (Primary Control Field)

The 4-bit (hex) character in this field identifies the status of the communications line or dial interface that the ICW is controlling. See B-080 for a listing of the hex characters used.

SDF (Serial Data Field)

This 10-bit field is used to:

1. Serialize or deserialize data to or from the communications line interface.
2. Initialize the line interface by means of the set mode (PCF state X'1'). See B-070 for a listing of the SDF bits used during set mode.



LCD (Line Control Definer)

The 4-bit (hex) character in this field defines the type of communications line or dial interface that the ICW is controlling. See B-062 for a listing of the hex characters used.

ICW–SECONDARY CONTROL FIELD

SCF 0 (Stop Bit Check/Receive Break/Abort)

The scanner sets this bit to a 1 when the scanner detects:

- a space for the stop bit on a start-stop line in the receive state (PCF X'7').
- a 'modem receive space' at 'tag detect' on a start-stop line in the transmit data state (PCF X'9'). When the control program detects this bit set for two consecutive characters, this condition should be interpreted as a 'receive break' signal.
- seven consecutive one bits (SDLC) abort in the receive data stream on a SDLC line in the receive information state (PCF X'6 or 7').

SCF 0 set to a 1 resets SCF 1 (service request interlock).

The service routine executes an Output X'44' with byte 0.0 set to a 1 to reset this bit to 0.

SCF 1 (Service Request Interlock)

The scanner sets this bit to 1 when the scanner signals for a level 2 interrupt request by raising 'interrupt go' except when:

- SCF bits 0, 2, or 3 are set or being set.
- a SDLC Flag is detected.
- a SDLC abort is detected.

This bit is reset to 0 when:

- a SDLC abort is detected.
- the service routine executes an Output X'44' with byte 0.1 set to a 1.
  SCF bits 0, 2, or 3 are set to 1.

The scanner uses this bit for overrun/underrun detection.

SCF 2 (Character Overrun/Underrun)

The scanner sets this bit to 1 when the scanner:

- attempts to set SCF 1 (service request interlock) and it is already set.
- detects a SDLC Flag in other than the predicted position in the SDF when in receive information state (PCF X'7'). See B-530 for information on predicted position.

SCF 2 set to a 1 resets SCF 1 (service request interlock).

The control program executes an Output X'44' with byte 0.2 set to 1 to reset this bit to 0.

SCF 3 (Modem Check)

The scanner sets this bit to 1 if the scanner detects:

- Data Set Ready is inactive during PCF states 5 through D for start-stop, BSC, or SDLC.
- Clear To Send is inactive during PCF states 9, A, B, or D for start-stop, BSC, or SDLC.
- a TTY echo check for start-stop.
- receive line signal detect (carrier detect) inactive on a start-stop line in receive state (PCF X'7') when the pad flag (SCF 7) is a 1 (switched line security).

SCF 3 set to a 1 resets SCF 1 (service request interlock).

The control program executes an Output X'44' with byte 0.3 set to a 1 to reset this bit to 0.

SCF 4 (Receive Line Signal Detector)

The scanner sets this bit to 1 if the modem is receiving a carrier signal for a start-stop, BSC, or SDLC line interface.

The scanner resets this bit to 0 when the carrier signal becomes inactive.

SCF 5 (Flag Detection/Disable Zero-Insert Remembrance)

SDLC Receive Operation

The scanner sets this bit to 1 when a Flag is detected in the receive data stream when in PCF states X'4, 5, 6, or 7' and when using LCD codes X'8, 9'. This bit set to 1 does not cause a level 2 interrupt but a level 2 interrupt may be generated because of the change of PCF states caused by detecting the Flag. For example; a Flag detected in PCF X'7' sets PCF state 6 and this activates the signal 'interrupt go' which starts the level 2 interrupt request.

The control program executes Output X'44' with bit 0.5 set to 1 to reset SCF 5.

SDLC Transmit Operation

The scanner sets this bit to 1:

- as a character is transferred from the PDF to the SDF (tag detected) while in PCF state X'8, 9, A, C, or D and using SDLC code if SCF 7 (disable zero-insert control) is set to 1.
- when the scanner is in PCF X'8' (initial transmit) using SDLC code when Clear To Send becomes active. The scanner sets PCF X'9' at the same time.

While SCF 5 is a 1, the ones counter is forced to a state of 001 which disables the automatic insertion of a zero after five consecutive one bits.

The scanner resets this bit to 0 on a transmit operation as the tag is detected if SCF 7 is a 0. While SCF 5 is a 0, the ones counter controls inserting a zero bit in the data stream after the transmission of 5 consecutive one bits.

The control program must *never* reset SCF 5 (Output X'44' with bit 0.5 set to 1) when in transmit mode.

SCF 6 (Program Flag)

The control program executes Output X'44' with byte 0.6 set to a 1 to set this bit to a 1. This bit is used for program test and skip purposes.

The control program executes Output X'44' with byte 0.6 set to a 0 to reset this bit to a 0.

SCF 7 (Pad Flag/Disable Zero-Insert Control)

This bit is set to a 1 by the service routine (Output X'44' with byte 0.7 set to 1) when:

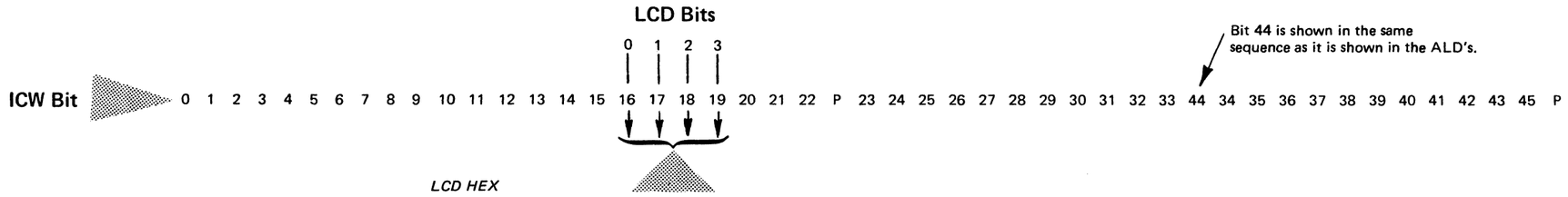
- the 'send data' line must be held at a mark level for the complete character time for a start-stop transmission. When this bit is set to a 1, the scanner forces a mark for the start bit. The other mark bits deserialize normally from a X'FF' simultaneously set in the PDF.
- it is desired to monitor 'receive carrier detect' on a start-stop line in receive state (PCF X'7') for switched line security reasons. If 'receive carrier detect' becomes inactive, the scanner sets SCF 3 (modem check) to a 1.
- a Flag or Abort character is set into the PDF on a transmit operation when using SDLC code.
  This 1 state is transferred to SCF 5 (disable zero-insert remembrance) as the next transmit tag is detected. When SCF 5 is a 1, the scanner forces the ones counter to a state of 001 thus blocking the automatic insertion of zero bits after 5 consecutive one bits. This allows the transmission of the Flag or the Abort (X'7F') characters.
- handling the level 2 interrupt for the address character on a receive operation (PCF X'7') when using SDLC code.
  The 1 state is not transferred to SCF 5 during the receive operation. When SCF 7 is a 1, the active level of receive 'tag detected' forces a '7 bit xfer' which insures transferring the entire 8-bit control character to the PDF.

The service routine executes Output X'44' with byte 0.7 set to 0 to reset this bit after the desired action has been completed.

ICW—LCD FIELD

LCD (Line Control Definer)

The LCD is used during transmit and receive operations to define the line control used by the line set type. The scanner uses the LCD field to determine the position of the character within the PDF (parallel data field) and SDF (serial data field), and to set up the proper PDF—to—SDF transfer during a transmit operation, and the proper SDF—to—PDF transfer during a receive operation.



LCD HEX CHARACTER	*EXAMPLE OF TERMINAL TYPE*
5	IBM 1030
4	IBM 1050, 1060, 2740, and 2741
6	IBM 2845/2848
C	IBM BSC System with EBCDIC CODE
D	IBM BSC System with USASCII CODE
3	Autocall
9	IBM 3705-80 (with Remote Program Loader)

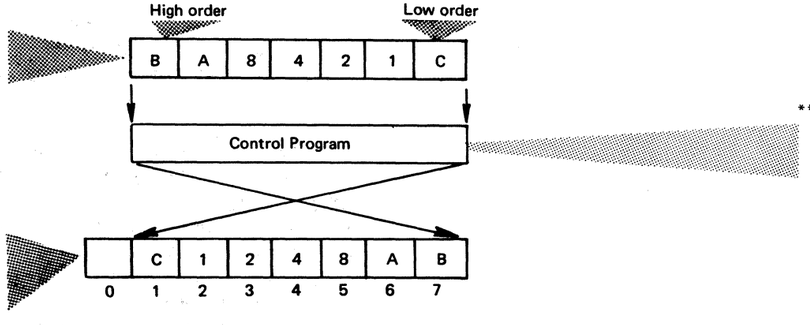
LCD HEX CHARACTER		*TYPE OF LINE CONTROL*
0	***	Start-Stop 9 bits per character—6 data bits—1 start bit 2 stop bits on transmit
1		Not Used
2	***	Start-Stop 8 bits per character—5 data bits—1 start bit 2 stop bits on transmit
3		Dial (Auto-Call Unit)
4	***	Start-Stop 9 bits per character—7 data bits—1 start bit 1 stop bit
5	***	Start-Stop 10 bits per character—7 data bits—1 start bit 2 stop bits on transmit
6	***	Start-Stop 10 bits per character—8 data bits—1 start bit 1 stop bit
7	***	Start-Stop 11 bits per character—8 data bits—1 start bit 2 stop bits on transmit
8		Monitor Flag
9		SDLC 8 bit byte length
A		Reserved
B		Reserved
C		EBCDIC
D		USASCII
E		Reserved
F	****	Feedback Error

***These LCD states require the control program to reverse the character before executing Output X'44' (to place the character in the PDF for transmit operations), or after executing Input X'44' (to obtain the character from the PDF for receive operations). This only occurs if the terminal requires the high order bit of the data character in the host processor to be the first data bit on the transmission line. This is shown as the B bit in the LCD X'4' example.

When the terminal requires the low order bit of the data character in the host processor to be the first data bit on the transmission line, the control program should not reverse the character as above. For example: LCD X'6' when the terminal is the IBM 2848.

Example—LCD X'4'

Host processor contains character in BCD code in this format



Scanner requires character in this BCD format in PDF to transmit B bit first

Summary of LCD Code Changes Due to Receiving SDLC Flag and BSC SYN Characters

LCD State	*Flag* Detected During PCF X'4, 5, or 7'*	*Flag* Detected During PCF X'6'*	*EBCDIC SYN (X'32') Character Detected During PCF X'4 or 5'*	*USASCII SYN (X'16') Character Detected During PCF X'4 or 5'*
LCD X'9' (SDLC 8)	• Sets LCD X'9' • Resets SDF** • Inserts 'tag' bit in SDF 2 • Sets PCF X'6' • Causes a level 2 interrupt request • Sets SCF 5 bit • Inhibits set of SCF 1 • Inhibits SDF-to-PDF transfer • Checks that Flag was received on 'boundary' (state 7 only)	• Sets LCD X'9' • Resets SDF** • Inserts 'tag' bit in SDF 2 • Leave in PCF X'6' • Inhibits level 2 interrupt request • Sets SCF 5 bit • Inhibit set of SCF 1 • Inhibits SDF-to-PDF transfer	• Sets LCD X'C' • Sets PCF X'7' • Resets SDF** • Inserts 'tag' bit in SDF 2	• Sets LCD X'D' • Sets PCF X'7' • Resets SDF** • Inserts 'tag' bit in SDF 2

LCD State	*Flag* Detected During PCF X'5'*
LCD X'8' (Monitor Flag)	• Sets LCD X'9' • Resets SDF** • Inserts 'tag' bit in SDF 2 • Sets PCF X'6' • Causes a level 2 interrupt request • Sets SCF 5 bit • Inhibits set of SCF 1 • Inhibits SDF-to-PDF transfer

*'SDLC Frame Detect' is the notation used in the ALD logic for 'Flag Detect'.
**The scanner resets the SDF by inhibiting 'shift' and leaving 'SDF direct' inactive.

****A Feedback error can be forced by the 3705-80 Emulation Program to set up presentation of Equipment check sense for some level 1 errors. See Emulation Program Logic Manuals SY30-3001 and SY30-3031.

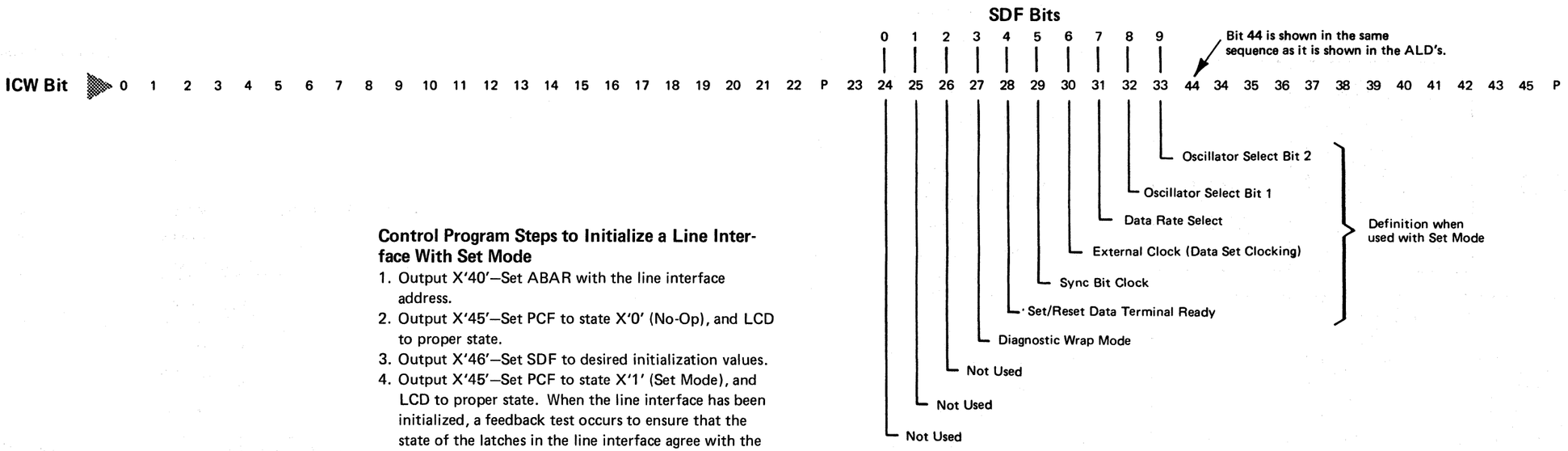
ICW–SDF FIELD

See B-090 for autocall interface

SDF (Serial Data Field)

The SDF is primarily used as a character serializer/deserializer field. On receive operations, the data coming from the line interface is placed in the SDF bit-by-bit to assemble a character. The character transfers to the PDF after the character has been assembled. The program must execute Input X'44' to obtain the character. When transmitting, the character transfers from the PDF to the SDF under hardware control. The SDF sends a bit at a time to the line interface where the bits are sent to the line or modem.

Set Mode (PCF X'1') uses the SDF to initialize the line interface. The definition of the SDF bits, when used for Set Mode, is shown below.



Control Program Steps to Initialize a Line Interface With Set Mode

1. Output X'40'–Set ABAR with the line interface address.
2. Output X'45'–Set PCF to state X'0' (No-Op), and LCD to proper state.
3. Output X'46'–Set SDF to desired initialization values.
4. Output X'45'–Set PCF to state X'1' (Set Mode), and LCD to proper state. When the line interface has been initialized, a feedback test occurs to ensure that the state of the latches in the line interface agree with the state of the SDF. The scanner sets PCF X'0' and generates a level 2 interrupt request.

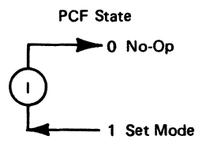
   If a feedback check occurred, the scanner sets the LCD to state F (Feedback Error).

ICW—PRIMARY CONTROL FIELD

See B-090 for PCF for autocall interface.

- The PCF (primary control field) defines the state of the line interface at any particular time. It is used to buffer the operation being performed on that line interface between successive scans.
- The control program initially sets the status of the PCF.
- The control program executes Output X'45' to set or change the PCF state.
- The type 2 scanner automatically changes PCF status under certain conditions (see diagrams).
- The control program executes Input X'45' to determine the PCF status.
- The scanner interpretation of the PCF depends upon the state of the LCD field. The interpretations for a binary synchronous interface, a start-stop interface, and a synchronous data link control interface are shown on this page. See B-090 for the interpretation of the PCF for an autocall interface.

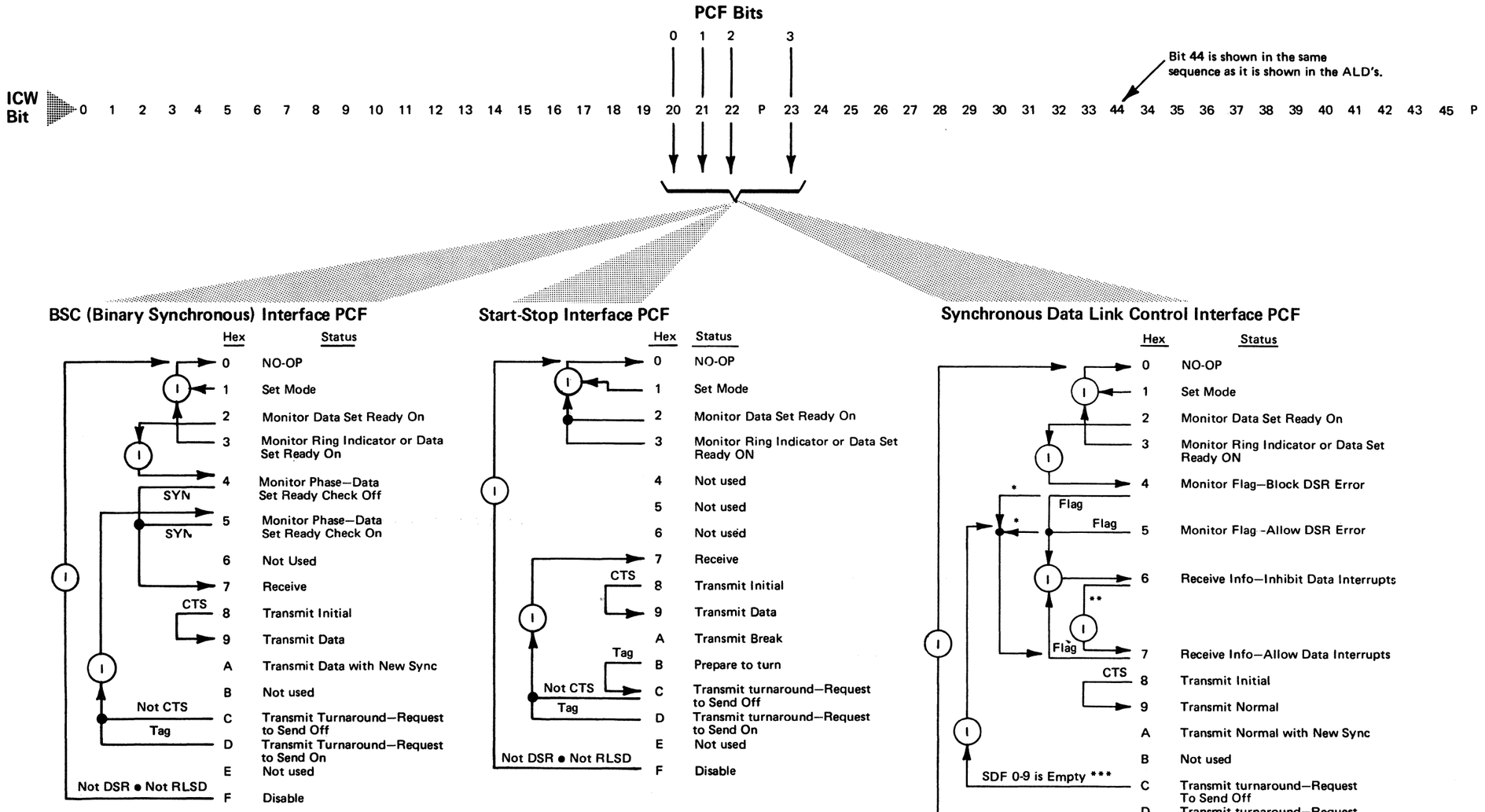
Explanation of diagrams.



The control program sets PCF X'1'. This is indicated by no line going toward 1.

Once the scanner executes set mode (PCF X'1'), the scanner automatically sets PCF X'0' (No-Op). This is indicated by the line leaving 1 and going to 0. A level 2 interrupt request occurs and is indicated by the (1) inserted within the line.

Note: *See B-310 for the logic circuits that cause 'interrupt go'. This causes the level 2 interrupt request.*



For a complete description of these PCF states and the conditions under which they are used, see the *IBM 3705-80 Communications Controller Principles of Operation*, GC 30-3074.

*EBCDIC or USASCII 'SYNC' character received in LCD X'9' (SDLC 8).
**Tag • non-Flag character
*** When PCF state C is executed in SDLC mode, the normal 'tag detected' (SDF 0-8 is empty and SDF 9=1) is delayed until a zero is shifted into SDF 9. During the next gated bit service, the 'SDF 0-9 is empty' condition generates the 'tag' line that (1) resets the RTS and transmit mode latches in the line interface, (2) sets PCF state X'5' (Monitor Flag-Allow DSR Error), and (3) places the line in a level 2 interrupt pending state.

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ICW-BITS 34-37 AND 44 (SDLC)

ICW Bits 34-36 (SDLC Ones Counter)

SDLC Receive Operation

The ones counter is used to detect:

- inserted zeros to be deleted from the bit stream during PCF X'6 or 7'. 1
- Flag sequences during PCF X'4, 5, 6, or 7'. 2
- seven consecutive ones sequence (Abort) during PCF X'6 or 7'. 3

SDLC Transmit Operation

The ones counter is used to insert a zero after five consecutive one bits during PCF X'8, 9, A, C, or D' when SCF 5 (disable zero-insert remembrance) is a 0. 4

Ones Counter Controls

The scanner adds 1 to the ones counter at 'SDLC bit time' when the ones counter is not zero and a 1 was transmitted 5 or received provided SCF 5 bit is 0 when in the transmit state. Adding 1 with the count at 7 causes the ones counter to go to 000 which stops the counting. This occurs when the Abort sequence is detected.

The scanner resets the ones counter to 001 at 'SDLC bit time' when:

- 'Xmt data' is 0 when in PCF states X'8, 9, A, C, or D'. 6
- the received bit is 0 (normal mode) when in PCF states X'4, 5, 6, or 7'.
- the received bit differs from the last line state (NRZI mode) when in PCF states X'4, 5, 6, or 7'. 7
- 'new SCF 5' (disable zero-insert remembrance) is a 1 when in PCF states X'8, 9, A, C, or D'. 8

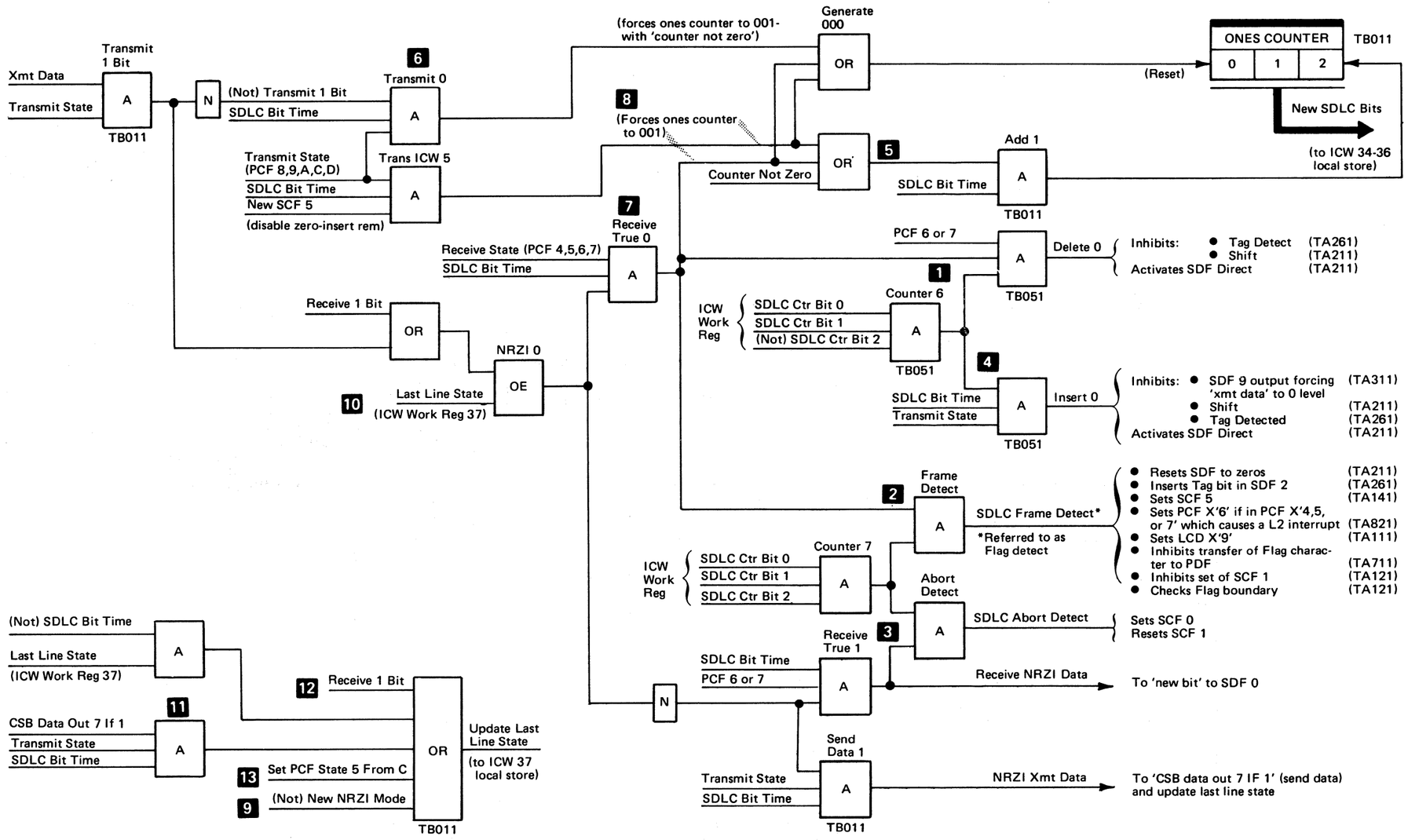
ICW Bit 37 (Last Line State)

- The scanner holds this bit at a 1 during normal mode (ICW 9 bit 44=0). When this bit is a 1, it conditions the Exclusive OR circuit to pass the transmitted and received bits unchanged. 10
- During a NRZI mode transmit operation, the scanner sets this bit to the state of the bit being sent to the LIB. 11
  - When Clear To Send is inactive and the line interface is in PCF state 8, 'xmt data' is at the 1 (mark) level and the scanner sets this bit to 1.
  - When Clear To Send is active, the scanner sets this bit to 1 if the 'xmt data' state is the same as the old last line state. If different, the scanner resets this bit to 0.
- During a NRZI mode receive operation, the scanner sets this bit to 1 when the received bit from the LIB is a 1 and resets this bit to 0 when the received bit is a 0. 12
- The scanner sets this bit to 1 when PCF state 5 is set from PCF state C when Clear To Send becomes active. 13
- Control program sets this bit to 1 by executing Output X'47' with byte 1.1 set to 1 for diagnostic purposes.
- Control program resets this bit to 0 by executing Output X'47' with byte 1.1 set to 0.

ICW Bit 44 (NRZI Control)

Control program sets this bit to 1 by executing Output X'46' with byte 0.0 set to 1. This causes the data to be transmitted in NRZI mode when in PCF state X'9, A, C, or D'. In NRZI mode the 'send data buffer' in the line interface is complemented when a zero is transmitted and unchanged when a one is transmitted.

Control program resets this bit to 0 by executing Output X'46' with byte 0.0 set to 0. Data is transferred in normal mode with this bit at 0. 9



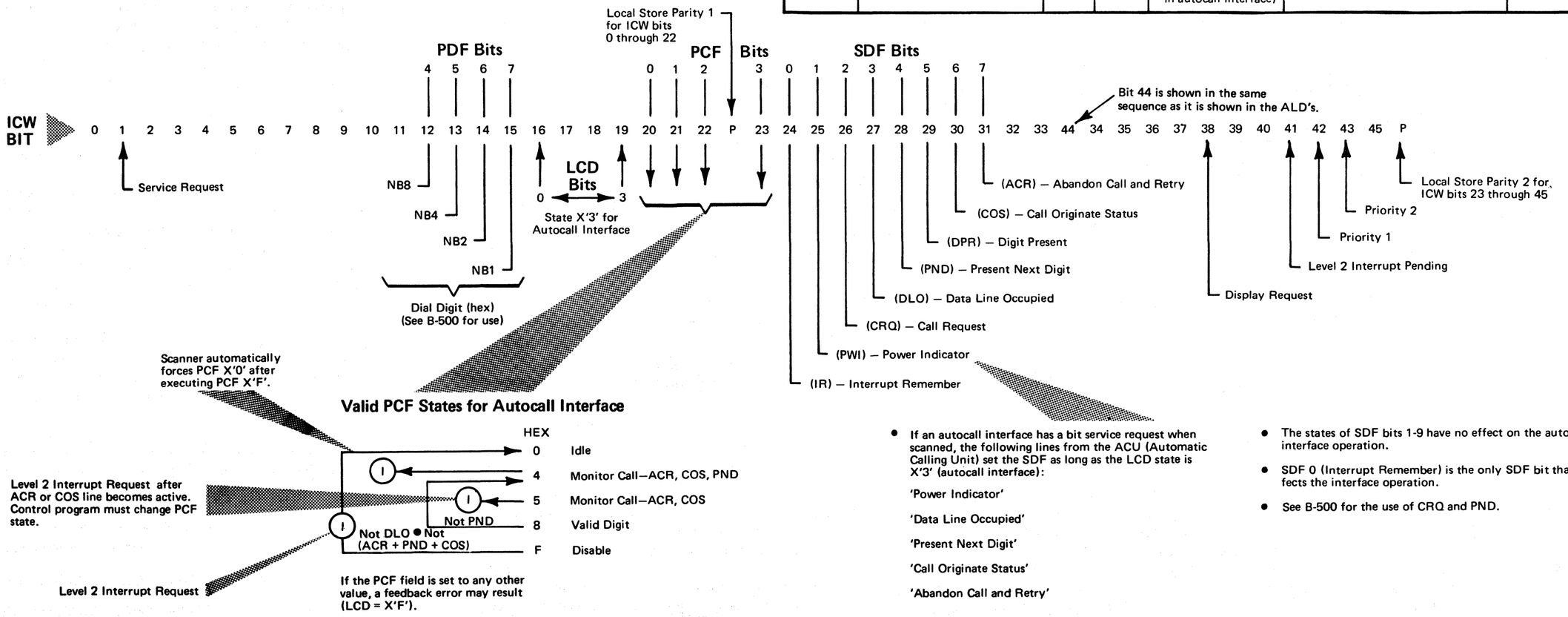
ICW FOR AUTOCALL INTERFACE

- The bits/fields shown below are the only positions of the ICW defined for autocall interfaces.
- For proper autocall interface operation, the LCD field of the ICW associated with an autocall interface must be set to X'3'. Autocall interface operation is then controlled by the state of the PCF field of the ICW associated with the interface.
- The lowest speed internal clock installed in each scanner (OSC 0) generates bit service requests for all autocall interfaces installed in the LIBs supported by the scanner.

SUMMARY OF THE EFFECT OF PCF STATES UPON ICW BIT POSITIONS

Note: *To be effective, LCD state must be X'3' during the scan of the autocall interface and a bit service request must be detected.*

PCF State (Hex)	*Conditions To Set PCF*	*CRQ (SDF 2)*	*DPR (SDF 5)*	*NB 1,2,4,8 (Dial Digit-hex)*	*Level 2 Interrupt Request*	*IR (SDF 0)*
0	1 – By control program 2 – From PCF X'F' when ACR, COS,PND' and DLO inactive	Reset	Reset	Zeros (resets digit buffer in autocall interface)	1– Yes, after PCF changes state to 0 2– See state 'F'	No Change
4	By control program PND falls in PCF X'8'	Set	Reset	Zeros (resets digit buffer in autocall interface)	Yes–if IR is reset and ACR, COS, or PND lead is active No–if IR bit is set	Set No Change
5	By control program	Set	Reset	Zeros (resets digit buffer in autocall interface	Yes–if IR is reset and COS or ACR lead is active No– if IR bit is set	Set No Change
8	By control program	Set	Set	Dial digit from PDF 4–7	No	No
F	By control program	Reset	Reset	Zeros (resets digit buffer in autocall interface)	Yes– when ACR,DLO,COS, and PND leads are all inactive	No



- If an autocall interface has a bit service request when scanned, the following lines from the ACU (Automatic Calling Unit) set the SDF as long as the LCD state is X'3' (autocall interface):

  'Power Indicator'

  'Data Line Occupied'

  'Present Next Digit'

  'Call Originate Status'

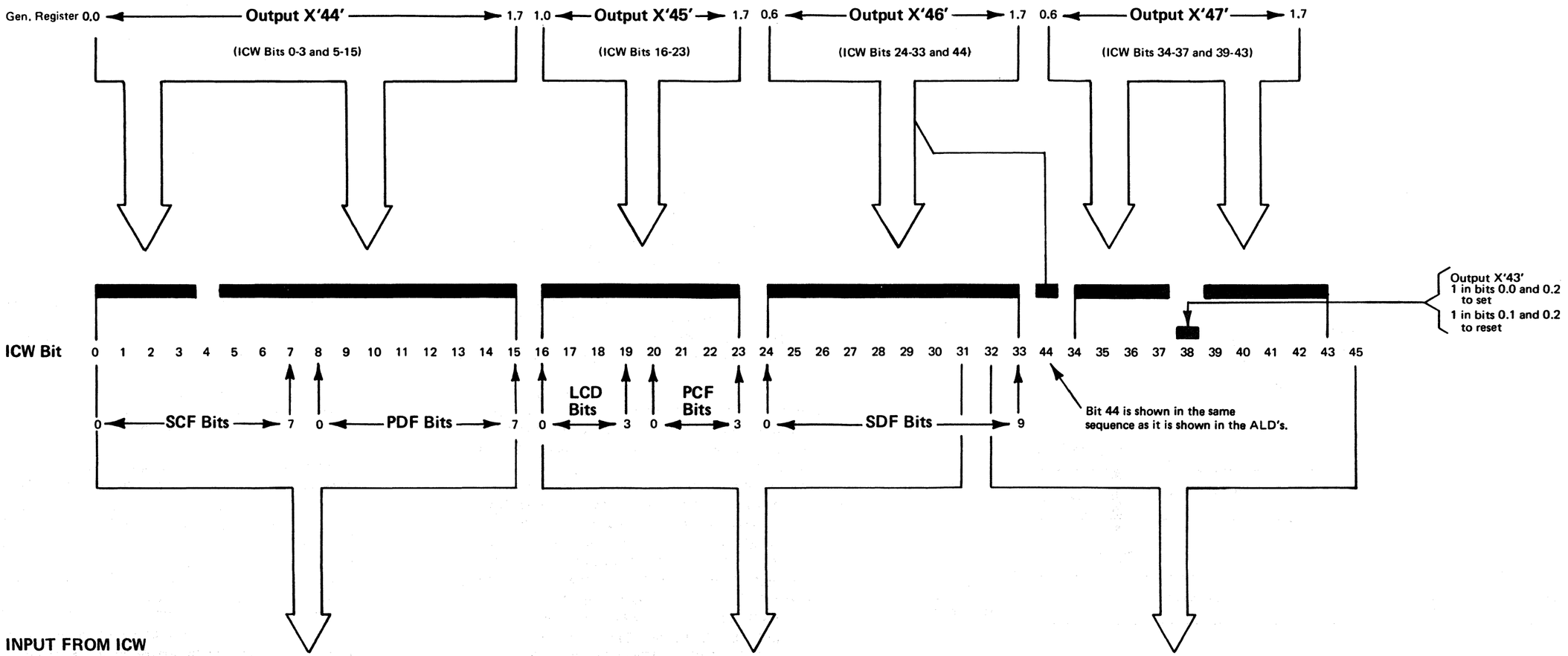
  'Abandon Call and Retry'

- The states of SDF bits 1-9 have no effect on the autocall interface operation.
- SDF 0 (Interrupt Remember) is the only SDF bit that affects the interface operation.
- See B-500 for the use of CRQ and PND.

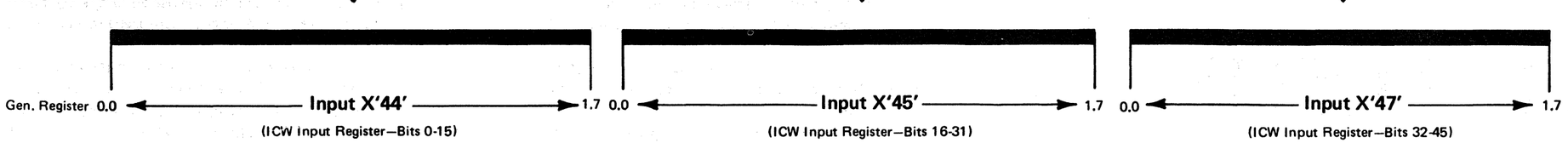
ACCESS OF ICW BY INPUT/OUTPUT INSTRUCTION

X = Hex

OUTPUT TO ICW



INPUT FROM ICW



Note: *The ICW parity bits are not included in the data transferred by the input instruction. The scanner generates parity for the data placed on the CCU inbus.*

INPUT AND OUTPUT INSTRUCTIONS

The type 2 scanner input/output instructions enable the program to communicate with the line interface bases (LIBs), program interrupt levels, interface controls words (ICWs), and type 2 scanner registers.

I/O Programming Considerations

As a general rule, input/output instructions should be issued only when the status of ABAR (attachment buffer address register) and the particular scanner ICW input register is known. An understanding of how those registers are set or loaded is needed for correct execution.

The following chart shows the program levels that can set the ABAR in the attachment base and the ICW input register in the selected scanner.

Program Level	*ABAR*	*ICW Input Register*
1	Output X'40'	Cannot set
2	L2 Interrupt	L2 Interrrupt
3 or 4	Output X'40'	Output X'40'

The following considerations are recommended for executing input/output instructions in the different program levels.

Program Level 1—(Error Routines)

1. Input X'40' can be executed to obtain the interface address in the attachment buffer address register.
2. Output X'40' can be executed to select the scanner if needed. The scanner can decode the input/output instructions only when selected.

Note: *The selected scanner ICW input register is not changed if an Output X'40' is executed at program level 1.*

3. After the scanner is selected, other input and output instructions may be executed as needed. Output instructions may be executed in any order, but all output instructions (Outputs X'43, 44, 45, 46, 47') that set a portion of the ICW *must* be separated by at least one cycle. This is required because the output register in the scanner buffers the data from the general register and requires time to store the data in the ICW.
4. Before exiting from program level 1, Output X'40' may be executed to place the old interface address back in ABAR if it had been saved. However, one instruction cycle must separate Output X'40' from any Output X'43-47'. The scanner ICW input register is not changed as a result of Output X'40'.

Program Level 2—(Character Service)

1. Input X'40' may be executed to obtain the interface address.
2. Inputs X'44, 45, or 47' may be executed whenever necessary to obtain a portion of the ICW from the scanner ICW input register; or Outputs X'43, 44, 45, 46, or 47' may be executed to set a portion of the ICW.
3. Output instructions may be executed in any order, but all subsequent Output X'43, 44, 45, 46, or 47' instructions must be separated by at least one cycle. These outputs must also be separated from an Output X'40' by at least one instruction.

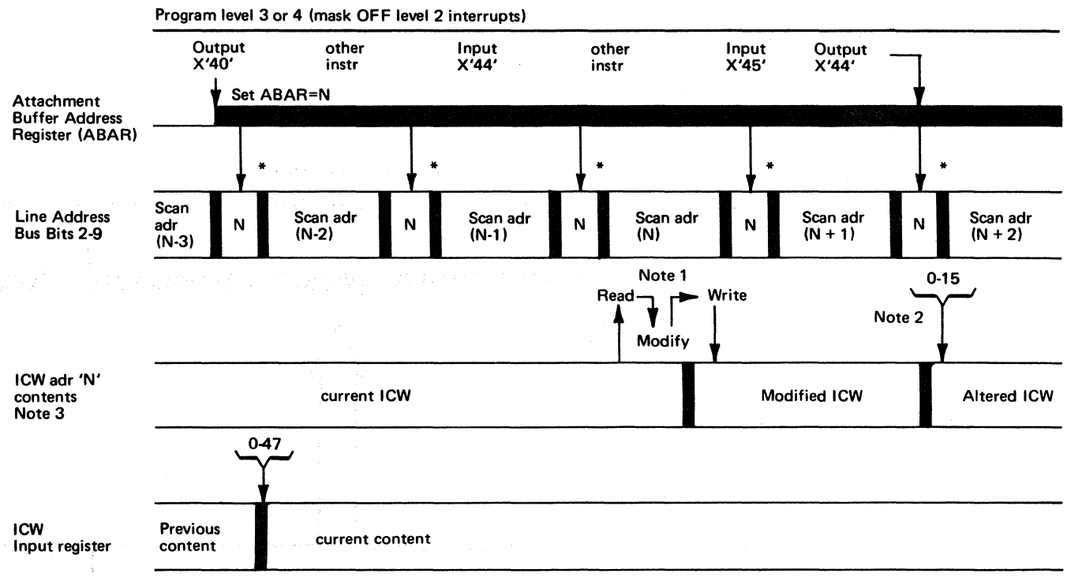
Program Levels 3 and 4—(Lower Level Routines)

1. Output X'7E' may be executed with a 1 in byte 1 bit 2 of the register specified by the R field. This will 'mask off' program level 2 interrupts that could change the contents of ABAR by a character service L2 interrupt.
2. Output X'40' may be executed to load ABAR with the interface address of a line to be acted upon. The scanner places the contents of the ICW associated with this interface address in that scanner's ICW input register.
3. After the scanner is selected, (a) Output X'43, 44, 45, 46, or 47' may be executed (to alter the associated portion of the ICW) followed by some other instruction, or (b) some other instruction must be executed, followed by Input X'44, 45, 46, or 47' (to obtain the associated portion of the ICW that was loaded by the Output X'40' into the ICW input registers).

Note: *If Output X'43, 44, 45, 46, or 47' was executed as in (a) above, the ICW content was altered, but the ICW input register still contains the contents of the ICW as it was before the alteration.*

4. Output instructions may be executed in any order, but all subsequent Output X'43, 44, 45, 46, or 47' instructions must be separated by at least one cycle.
5. All lines in the addressed type 2 scanner should be disabled before executing an Output X'42' to change the scan limit.
6. Output X'7F' may be executed with a 1 in byte 1, bit 2 of the register specified in the R field. This unmasks the program level 2 interrupts.

Example of Input/Output Instruction Sequence During Program Levels 3 and 4.



*Program addressing

0-15
To register R
(Input Register reflects current ICW)

16-23
To register R
(Input Register differs from current ICW

Notes:

1. *Current content of the ICW is read out, examined, and modified if needed, then written back into ICW. Modification example: During PCF state 8, 'clear to send' became active, so the scanner sets PCF state 9. The ICW input register will not reflect this modification.*
2. *Output X'44' alters the ICW content for address N. The ICW input register will not reflect this modification.*
3. *The scan limit for the scanner modifies the interface address on the line address bus to form the ICW address. Scan addressing is modified by the upper scan limit. This example assumes an upper scan limit of 00 (96 addresses), therefore no modification occurs.*

INPUT X'40' (INTERFACE ADDRESS)

Input X'40' is used to obtain the interface address from ABAR (attachment buffer address register) in the attachment base. When Input X'40' is executed, the attachment base gates the interface address in ABAR to the 0.6 through 1.6 bit positions of the general register specified by the R field. The attachment base also gates a 1 to position 0.4 and 0 to each of the remaining positions in the general register.

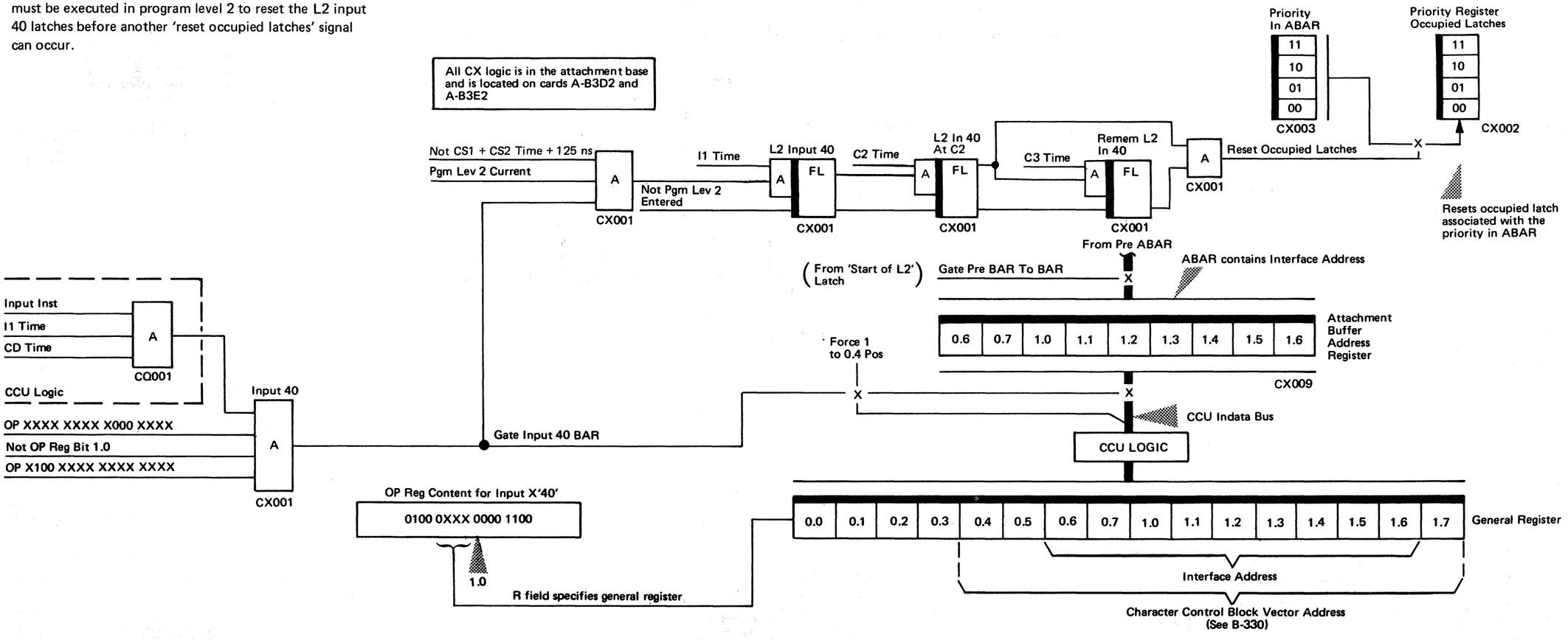
If Input X'40' is executed during program level 2, the attachment base resets the 'priority register occupied' latch associated with the interface address in ABAR. This indicates that (1) the character service request is being serviced by the control program and (2) the 'program level 2 interrupt priority register', from which the ABAR was loaded, is now available for another level 2 interrupt of the same priority. Subsequent Input X'40' instructions within the same character service interrupt do not reset the 'priority register occupied' latches. An exit instruction must be executed in program level 2 to reset the L2 input 40 latches before another 'reset occupied latches' signal can occur.

INPUT X'40' TIMINGS

CCU Clock (*)	A	B	C	D	A	B	C	D	B	C	D	A
I1 Time of Input X'40'					(Next Instruction)				Exit Instr			
Gate Input 40 BAR												
Write LS (in CCU)												
Pgm Lev 2 Entered										Exit		
Pgm Lev 2 Current											Exit	
L2 Input 40 FL												
Attachment Base Clock (*)	C4	C5	C6	C7	C0	C1	C2	C3	X	X	X	X
L2 In 40 AT C2 FL												
Remem L2 In 40 FL												
Reset Occupied Latches												

*The CCU clock and attachment base clock are asynchronous, and the relationship shown is assumed for this example.

All CX logic is in the attachment base and is located on cards A-B3D2 and A-B3E2



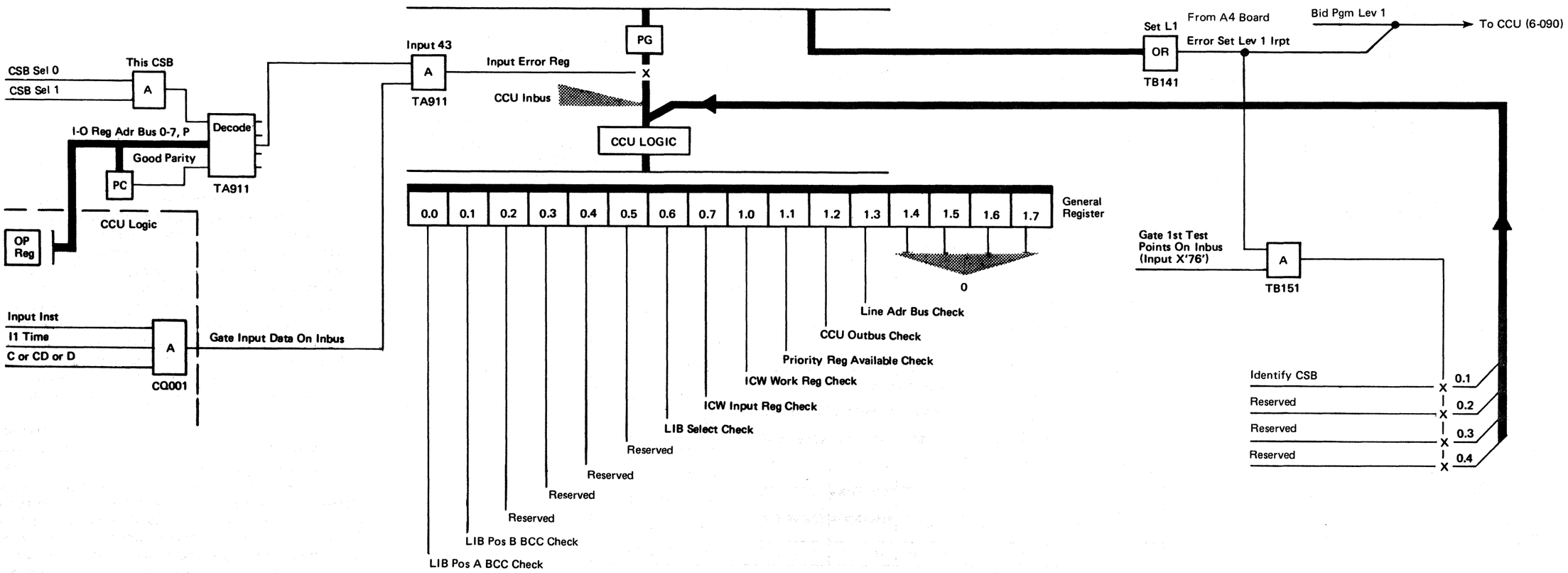
INPUT X'43' (CHECK REGISTER)

Input X'43' is used to obtain the status of the check register in the type 2 scanner. The interface address in the attachment buffer address register selects the scanner that contains the check register.

Level 1 Interrupt

If any of the check register bits in a scanner are set to 1, the scanner sets the level 1 interrupt request that bids for a program level 1 interrupt in the CCU. The level 1 routine determines that the scanner caused the level 1 interrupt by executing Input X'76'. The control program can set ABAR with an interface address associated with that scanner, and then execute Input X'43' to determine the specific cause for the level 1 interrupt.

General Register (R)	*Check Register Position*	*Cause Of Check*	*Reference*
0.0	LIB A BCC Check	Set to 1 if the scanner detects a LIB position A BCC local store parity error during a bit clock selection.	C-020 C-120
0.1	LIB B BCC Check	Same as above for LIB position B.	
0.2	Reserved		
0.3	Reserved		
0.4	Reserved		
0.5	Reserved		
0.6	LIB Select Check	Set to 1 if more than one LIB was selected, or more than one line was accessed on the selected LIB, or no line was accessed on the selected LIB, or a line was accessed on the LIB that was not selected.	
0.7	ICW Input Reg Check	Set to 1 if the scanner detects a parity error (odd) in the ICW input register (46 + 2P).	B-020
1.0	ICW Work Reg Check	Set to 1 if the scanner detects a parity error (odd) in the ICW work register (46 + 2P).	B-020
1.1	Priority Reg Avail Check	Set to 1 if the scanner detects a parity error (even) in the priority register available lines (4 + P).	B-020
1.2	CCU Outbus Check	Set to 1 if the scanner detects a parity error (even) on the Outbus (16 + 2P).	B-020, B-170
1.3	Line Adr Bus Check	The line adr bus parity is used to predict the parity of the address as modified by the scanner's upper scan limits. If this predicted parity does not compare with the actual parity of the modified address, the scanner sets this bit to 1.	B-020 B-(180-210)

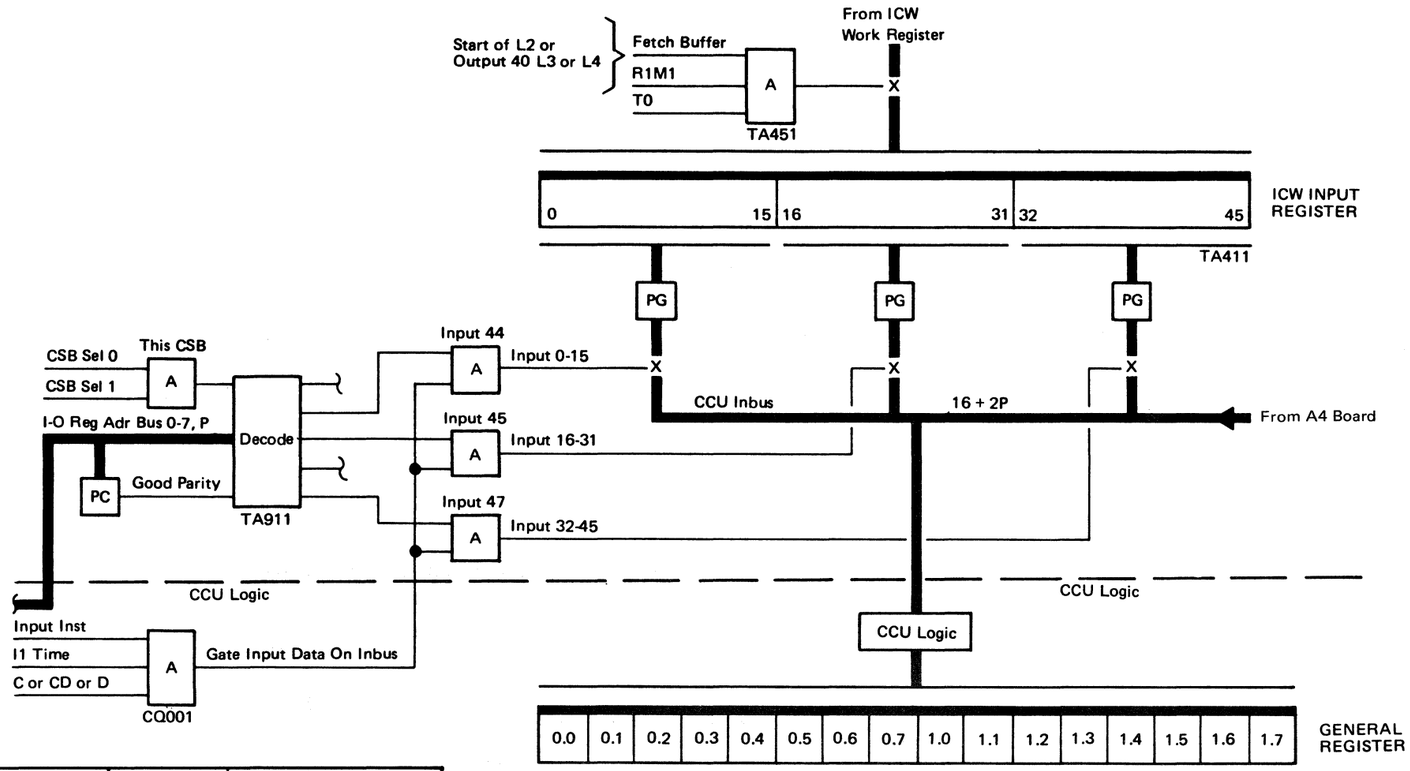


INPUT X'44', X'45' AND X'47'

Input X'44' (ICW Input Register—Bits 0-15). When the scanner decodes Input X'44', the scanner gates the contents of the SCF (secondary control field), and the PDF (parallel data field) to the general register specified by the R field.

Input X'45' (ICW Input Register—Bits 16-31). When the scanner decodes Input X'45', the scanner gates the contents of the LCD (line control definer), PCF (primary control field), and SDF (serial data field) bits 0-7 to the general register specified by the R field.

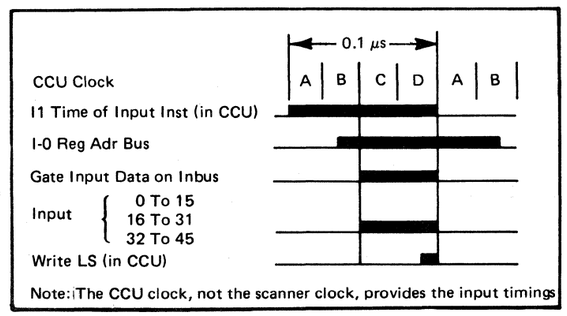
Input X'47' (ICW Input Register—Bits 32-45). When the scanner decodes Input X'47', the scanner gates the contents of SDF bits 8-9, NRZI control bit, ones counter bits 0-2, last line state bit, display request bit, L2 interrupt pending bit, priority bits 1-2, and reserved bits to the general register specified by the R field.



General Register Bit Pos.	Input X'44'	Input X'45'	Input X'47'
0.0	SCF 0 (Stop Bit Check/Receive Break/Abort)	LCD Bit 0	SDF Bit 8
0.1	SCF 1 (Service Request Interlock)	LCD Bit 1	SDF Bit 9
0.2	SCF 2 (Character Overrun/Underrun)	LCD Bit 2	Reserved
0.3	SCF 3 (Modem Check)	LCD Bit 3	Reserved
0.4	SCF 4 (Received Line Signal Detector)	PCF Bit 0	Reserved
0.5	SCF 5 (Flag Detection/Disable Zero-Insert Rem)	PCF Bit 1	Reserved
0.6	SCF 6 (Program Flag)	PCF Bit 2	Display Request
0.7	SCF 7 (Pad Flag/Disable Zero-Insert Control)	PCF Bit 3	Reserved
1.0	PDF Bit 0	SDF Bit 0	Reserved
1.1	PDF Bit 1	SDF Bit 1	L2 Interrupt Pending
1.2	PDF Bit 2	SDF Bit 2	Priority Bit 1
1.3	PDF Bit 3	SDF Bit 3	Priority Bit 2
1.4	PDF Bit 4	SDF Bit 4	NRZI
1.5	PDF Bit 5	SDF Bit 5	Reserved
1.6	PDF Bit 6	SDF Bit 6	Bit is always 0
1.7	PDF Bit 7	SDF Bit 7	Bit is always 0

See B-061 for SCF bit definitions

Storage Input Timing

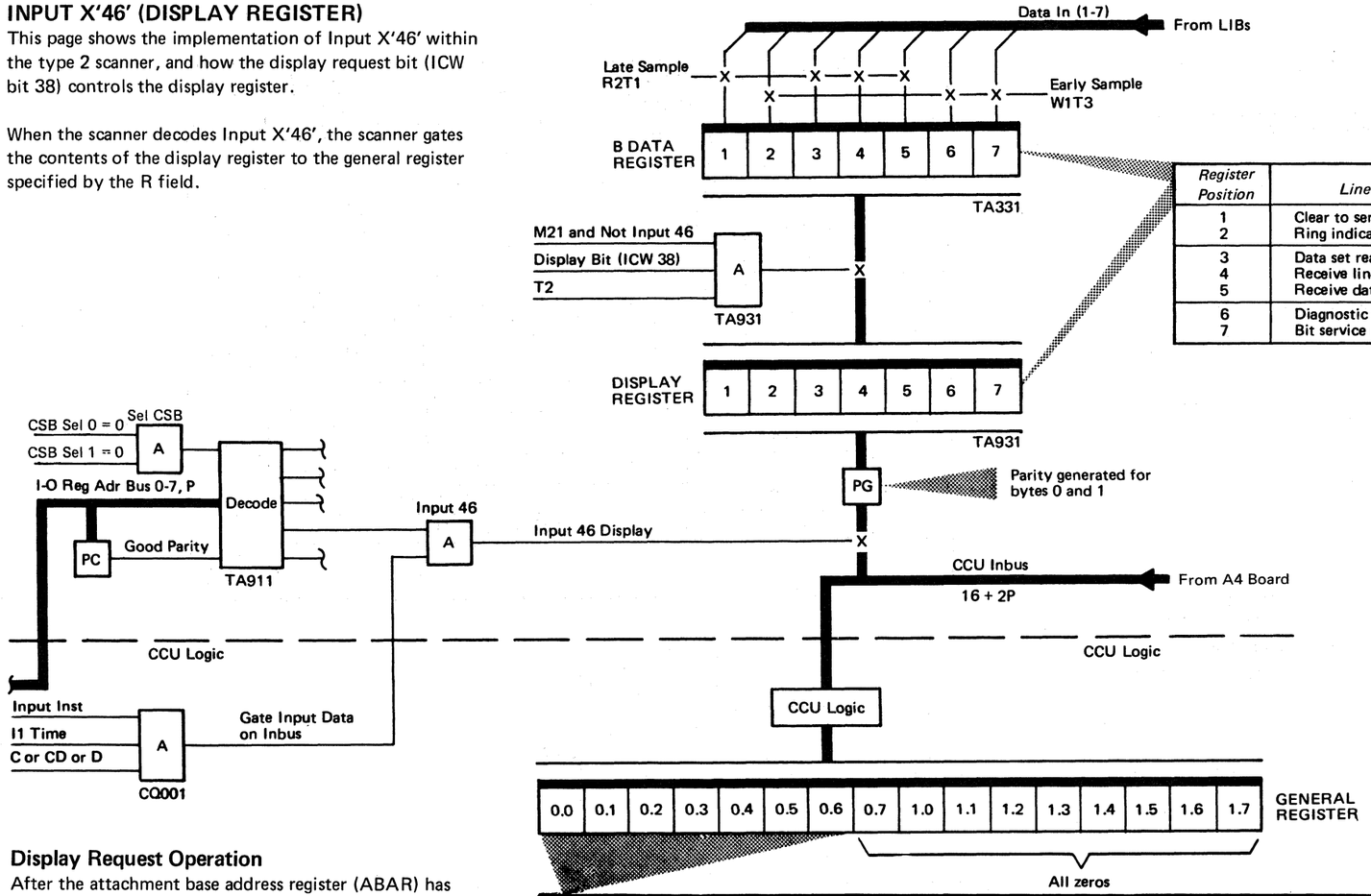


Note: The CCU clock, not the scanner clock, provides the input timings

INPUT X'46' (DISPLAY REGISTER)

This page shows the implementation of Input X'46' within the type 2 scanner, and how the display request bit (ICW bit 38) controls the display register.

When the scanner decodes Input X'46', the scanner gates the contents of the display register to the general register specified by the R field.



Register Position	*Line Interface*	*Auto Call Interface*
1	Clear to send	Abandon call and retry (ACR)
2	Ring indicator	Present next digit (PND)
3	Data set ready	Data line occupied (DLO)
4	Receive line signal detector	Power indicator (PWI)
5	Receive data bit buffer	Unused
6	Diagnostic wrap mode	Call originating status (COS)
7	Bit service request	Bit service request

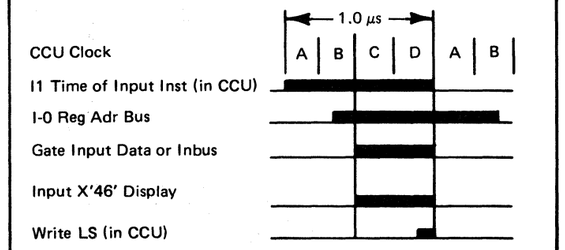
Display Request Operation

After the attachment base address register (ABAR) has been set to the proper interface address, the control program executes an Output X'43' to set the display request bit (ICW bit 38). As long as the display request bit is on, every scan of that interface causes the display register to trap the contents of the B data register. The display register traps the forced states of 'clear to send', 'data set ready', and 'receive line signal detector' when diagnostic wrap mode is on because these bits are not on in the B data register.

For the display register contents to be meaningful, only one display request bit may be on in an ICW associated with the scanner. Input X'46' should not be executed within 192 microseconds of the setting of the display bit. This ensures that the data in the display register is valid for the interface just selected and is not the result of a former display trap operation.

General Register Position	*Line Interface*	*Autocall Interface*
0.0	Clear To Send: 1 if the CTS line from the modem is on, or if diagnostic wrap forces CTS on.	Abandon Call and Retry: 1 if the ACR line from the autocall unit is on.
0.1	Ring Indicator: 1 if the ring indicator line from the modem is on.	Present Next Digit: 1 if the PND line from the autocall unit is on.
0.2	Data Set Ready: 1 if the DSR line from the modem is on, or if diagnostic wrap forces DSR on.	Data Line Occupied: 1 if the DLO line from the autocall unit is on.
0.3	Receive Line Signal Detector: 1 if the RLSD line from the modem is on.	Power Indicator: 1 if the PWI line from the autocall unit is on.
0.4	Receive Data Bit Buffer: 1 if the line interface receive data bit buffer contains a mark (1). This bit is 0 if the bit buffer contains a space (0).	Bit is always 0.
0.5	Diagnostic Wrap Mode: 1 if the line interface is in diagnostic wrap mode.	Call Originating Status: 1 if the COS line from the autocall unit is on.
0.6	Bit Service Request: 1 if the line interface bit service request is on.	Bit Service Request: 1 if the autocall interface bit service request is on.

Storage Input Timing



Note: The CCU clock, not the scanner clock, provides the input timings.

OUTPUT X'40', AND X'41'

Output X'40' loads an interface address in ABAR (attachment buffer address register) to the attachment base. When Output X'40' is executed in program levels 3 or 4, the attachment base gates the contents of the ICW work register to the ICW input register where it is available to the control program by means of Input instructions X'44', '45', and '47'.

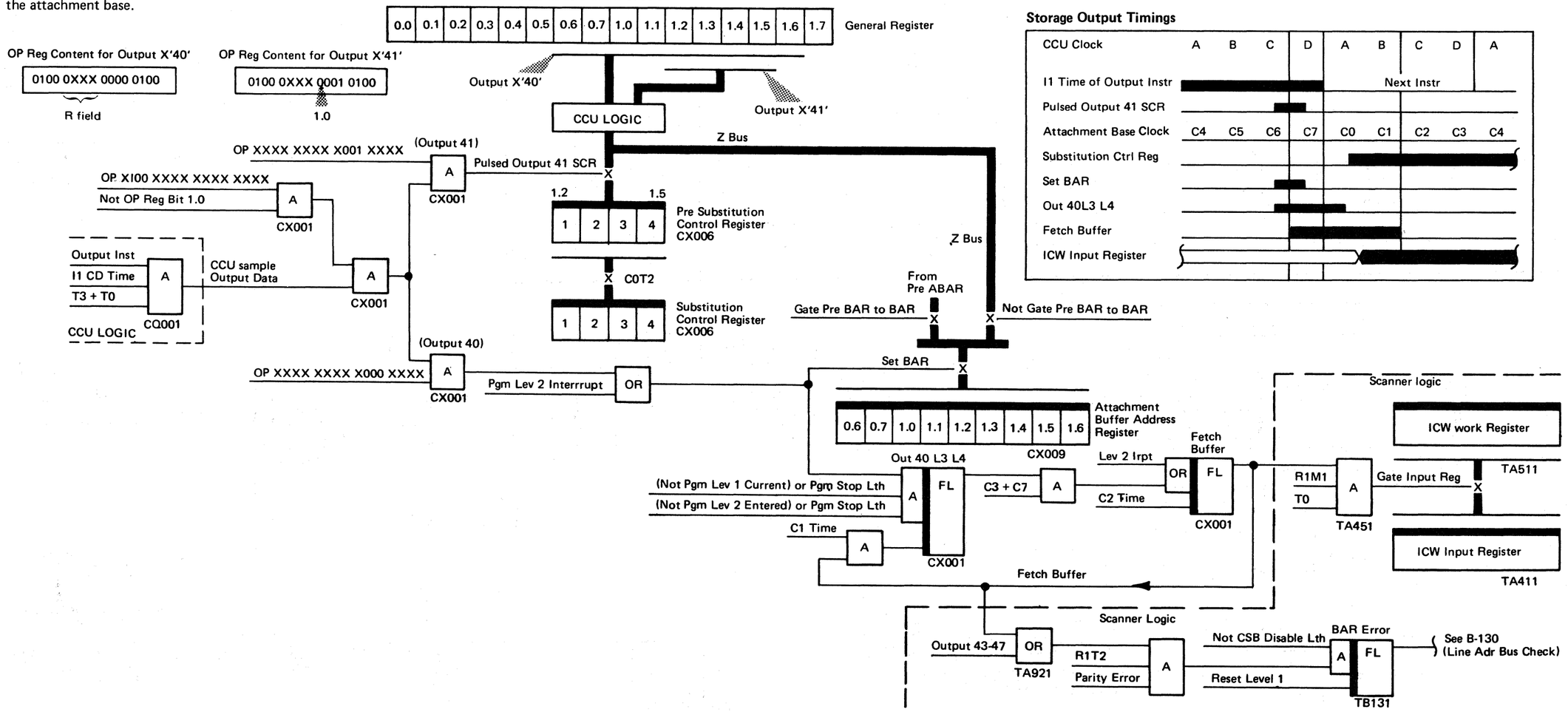
The control program must execute Output X'40' to initialize ABAR with an interface address associated with the installed type 2 scanner after the 3705-80 is powered on and before other inputs and outputs are issued to the scanner. Otherwise, an input/output check may occur.

Output X'41' sets the substitution control register bits in the attachment base.

General Register (R)	*Output X'40'*
0.0 – 0.5	*
0.6** – 0.7**	Interface Address Bit 0 – Bit 1 ⟩ Scanner (00 = 1)
1.0 – 1.2	Bit 2 – Bit 4 ⟩ LIB (010 = LIB A, 011 = LIB B)
1.3 – 1.6	Bit 5 – Bit 8 ⟩ Line (0 - F (hex))
1.7	*

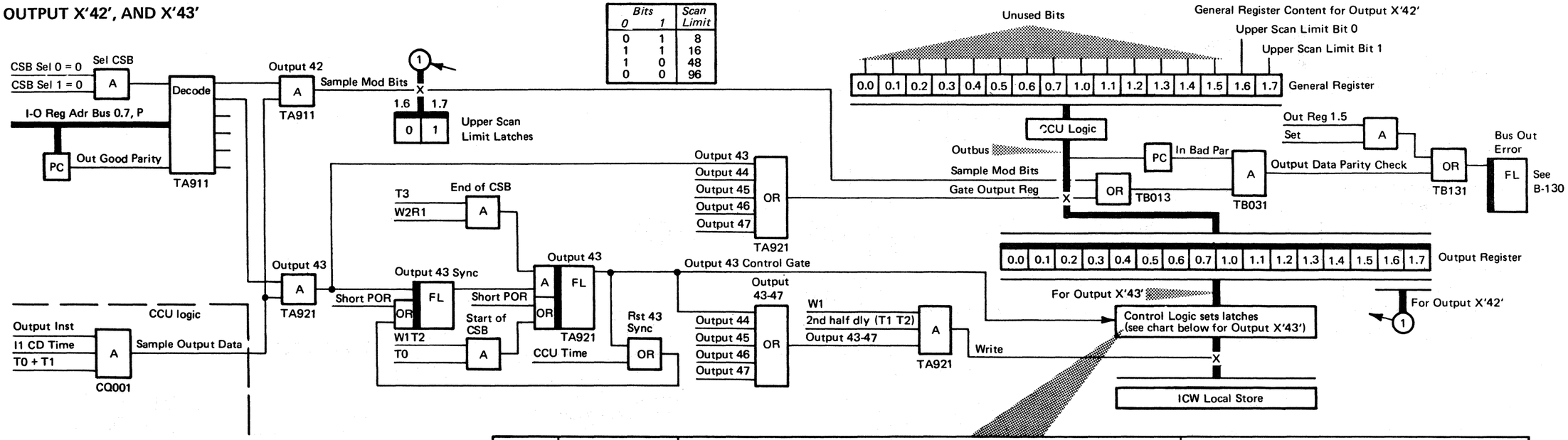
General Register (R)	*Output X'41'*
0.0 – 1.1	*
1.2 – 1.5	Substitution Ctrl Reg Bit 1 – Bit 4
1.6 – 1.7	*

*Bit Position Unused
**This bit must be zero in the 3705-80



Storage Output Timings

OUTPUT X'42', AND X'43'



Output Reg Pos	Position Name	Set Function (0.0 = 1)	Reset Function (0.1 = 1)
0.0	Set Function	A 1 causes the set function for output positions 0.2 through 1.6 when the corresponding bit is 1. This bit should not be 1 if 0.1 is 1.	Must be a 0 if the reset function is on (bit 0.1 = 1).
0.1	Reset Function	A 1 causes the reset function for output positions 0.2 through 1.6 when the corresponding bit is 1. This bit should not be 1 if 0.0 is 1.	Must be a 0 if the set function is on (bit 0.0 = 1).
0.2	Display Request	A 1 sets ICW bit 38. A 0 does not change ICW bit 38.	A 1 resets the ICW bit 38. A 0—no change.
0.3 | 0.6	Not used	No effect.	No effect.
0.7	Disable LIB pos A	A 1 disables LIB A. To do this, the scanner: ● Forces 'control out A' and 'control in A'. ● Forces 'control out B' and 'control in C'. ● Holds CSB data out lines 1-7 to 0. ● Resets PCF 0-3 to X'0' (N0-op). ● Inhibits 'CSB wants a priority register'. ● Resets ICW bit 41 (L2 interrupt pending). ● Inhibits the set of the 'work register error' latch in the check register. ● Forces 'write' at W2 (T3 + T0) to write into ICW local store. ● Masks BCC 1-6 errors from setting corresponding check register latches. (This resets the line/autocall interface latches in all line sets when LIB A is selected) A 0 has no effect.	A 1 *enables* LIB A. A 0 has no effect.
1.0	Disable LIB pos B	Same as 0.7 for LIB B.	Same as 0.7 for LIB B.
1.1	Not used	Not used	Not used
1.2	Not used	Not used	Not used
1.3	Not used	Not used	Not used
1.4	Not used	Not used	Not used
1.5	Type 2 Scanner N L1 Request	A 1 sets all 12 latches in the check register and causes a level 1 interrupt. A 0 has no effect.	A 1 resets the check register latches and the level 1 interrupt. A 0 has no effect.
1.6	Disable Interrupt Requests	A 1: ● Sets the 'CSB disable' latch that forces the same disable actions as described in 0.7 for all LIBS. ● Resets the upper scan limits. ● Resets the display request bit (ICW bit 38). ● Masks the setting of BCC 1-6 latches in the check register. ● Inhibits the setting of 'line sel error', 'in reg', 'work reg error', 'avail error', and 'BAR error' latches in the check register. Note: *Output X'43' can still set the 'line sel error' latch.* A 0 has no effect.	A 1 resets the 'CSB disable' latch to *enable the scanner.* A 0 has no effect. Note: *The 'CSB disable' latch may also be set during a power on, during IPL 1, or by a reset switch operation. The program must reset this latch in the scanner before the scanner can be initialized.*
1.7	Not Used	No effect.	No effect

Output X'42' sets the upper scan limit in the scanner. The interface address in the attachment buffer address register selects the scanner.

Output X'43' is executed to set or reset various control functions in the type 2 scanner. The interface address in the attachment buffer address register selects the scanner. When Output X'43' is executed, the bit configuration in the general register specified by the R field determines which control functions are set or reset.

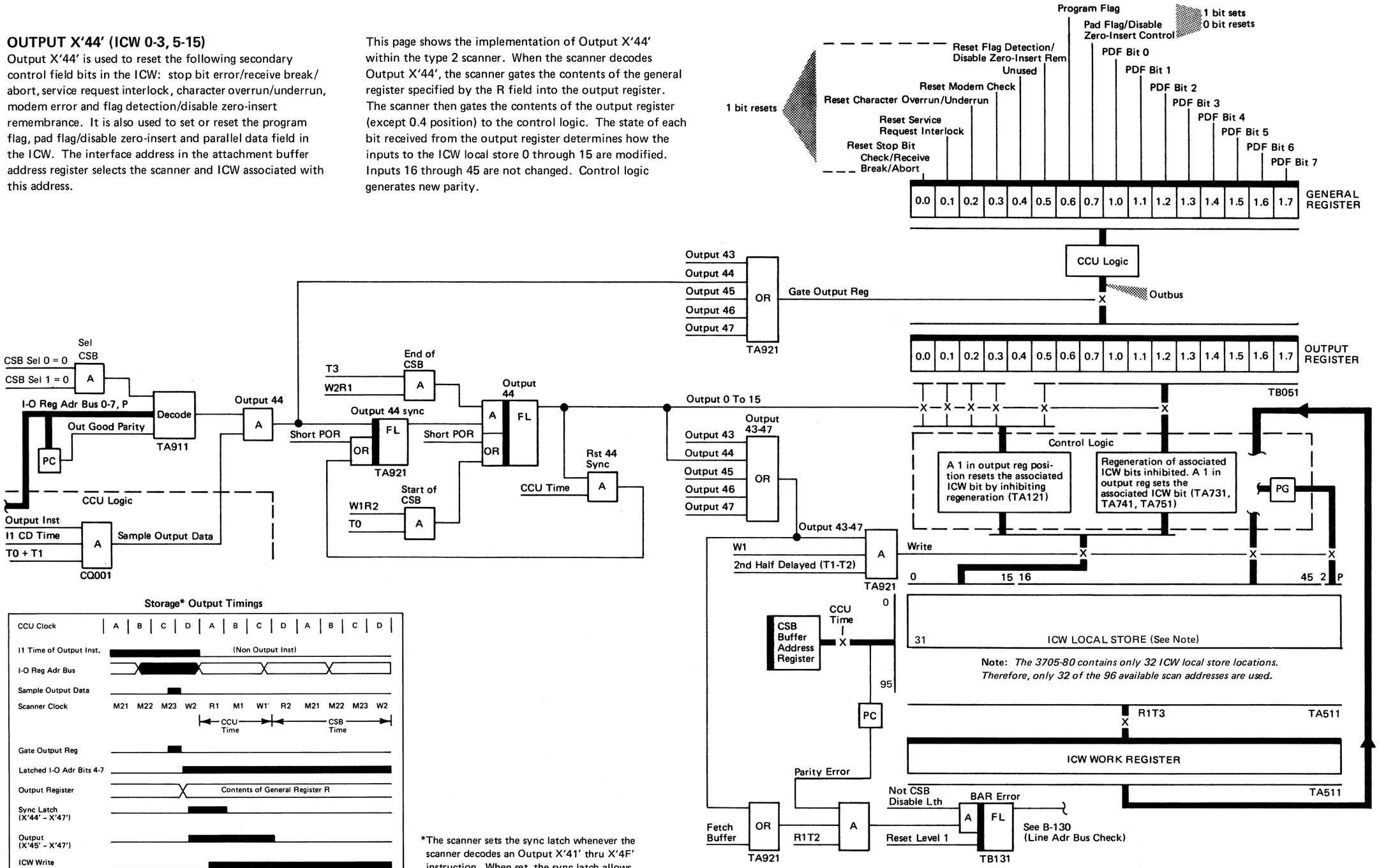
Selective LIB reset is caused by the set function. The scanner sets the 'mask LIB X errors' latch that causes the functions specified in the LIB pos 1 row (see chart). The scanner resets each line at the line's bit service request. The reset continues until the 'mask LIB X errors' latch is reset by the reset function (0.1 = 1 and a 1 in the associated disable LIB position) leaving LIB X *enabled.*

A minimum of one scan period (192 microseconds) is required between the time the 'CSB disable' latch is turned on to cause a reset (1.6 = 1 when 0.0 = 1), and when the 'CSB disable' latch is turned off to end the reset (1.6 = 1 when 0.1 = 1). The scanner is *enabled* when the 'CSB disable' latch is off.

OUTPUT X'44' (ICW 0-3, 5-15)

Output X'44' is used to reset the following secondary control field bits in the ICW: stop bit error/receive break/abort, service request interlock, character overrun/underrun, modem error and flag detection/disable zero-insert remembrance. It is also used to set or reset the program flag, pad flag/disable zero-insert and parallel data field in the ICW. The interface address in the attachment buffer address register selects the scanner and ICW associated with this address.

This page shows the implementation of Output X'44' within the type 2 scanner. When the scanner decodes Output X'44', the scanner gates the contents of the general register specified by the R field into the output register. The scanner then gates the contents of the output register (except 0.4 position) to the control logic. The state of each bit received from the output register determines how the inputs to the ICW local store 0 through 15 are modified. Inputs 16 through 45 are not changed. Control logic generates new parity.



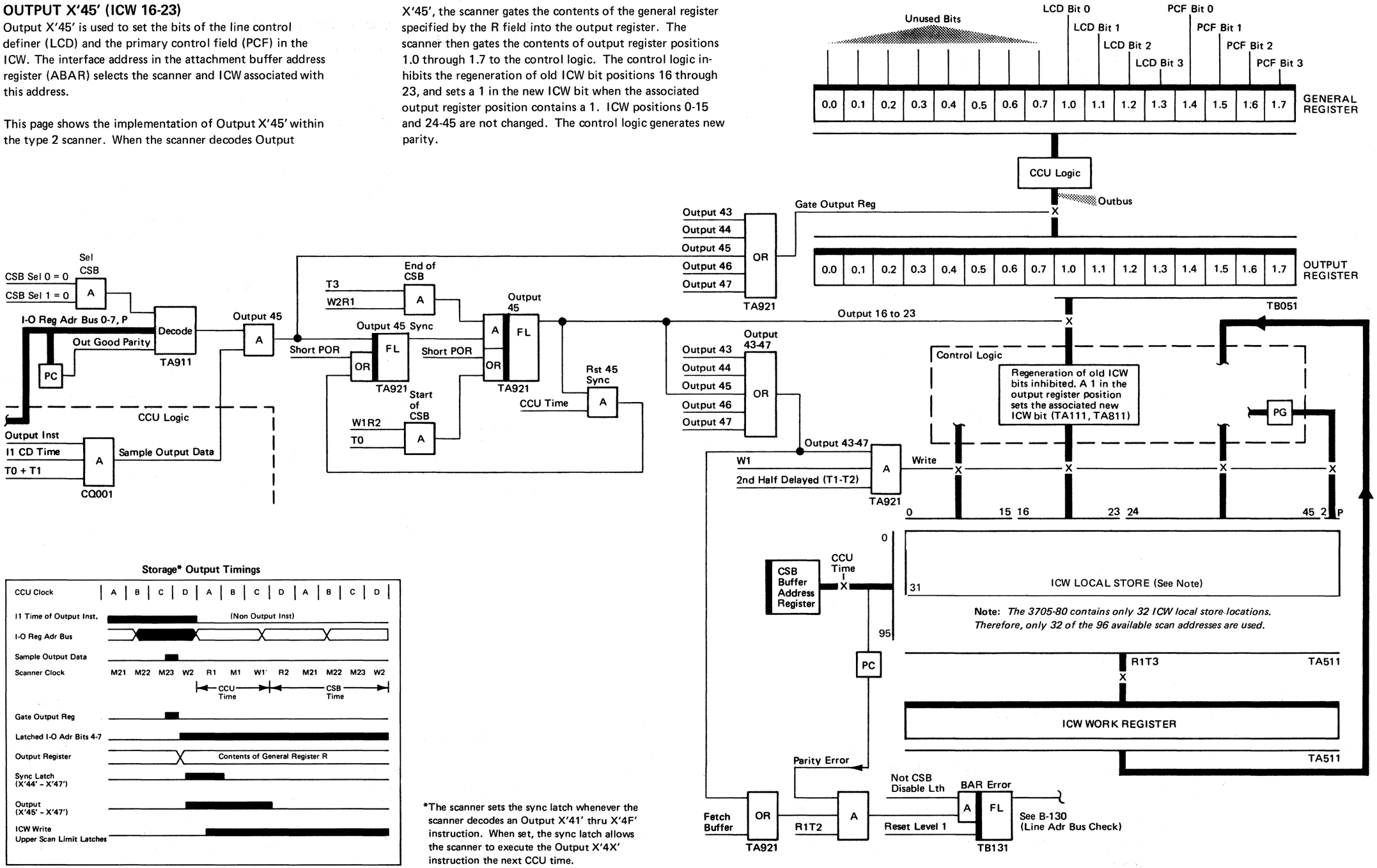
Storage* Output Timings

*The scanner sets the sync latch whenever the scanner decodes an Output X'41' thru X'4F' instruction. When set, the sync latch allows the scanner to execute the Output X'4X' instruction the next CCU time.

OUTPUT X'45' (ICW 16-23)

Output X'45' is used to set the bits of the line control definer (LCD) and the primary control field (PCF) in the ICW. The interface address in the attachment buffer address register (ABAR) selects the scanner and ICW associated with this address.

This page shows the implementation of Output X'45' within the type 2 scanner. When the scanner decodes Output X'45', the scanner gates the contents of the general register specified by the R field into the output register. The scanner then gates the contents of output register positions 1.0 through 1.7 to the control logic. The control logic inhibits the regeneration of old ICW bit positions 16 through 23, and sets a 1 in the new ICW bit when the associated output register position contains a 1. ICW positions 0-15 and 24-45 are not changed. The control logic generates new parity.



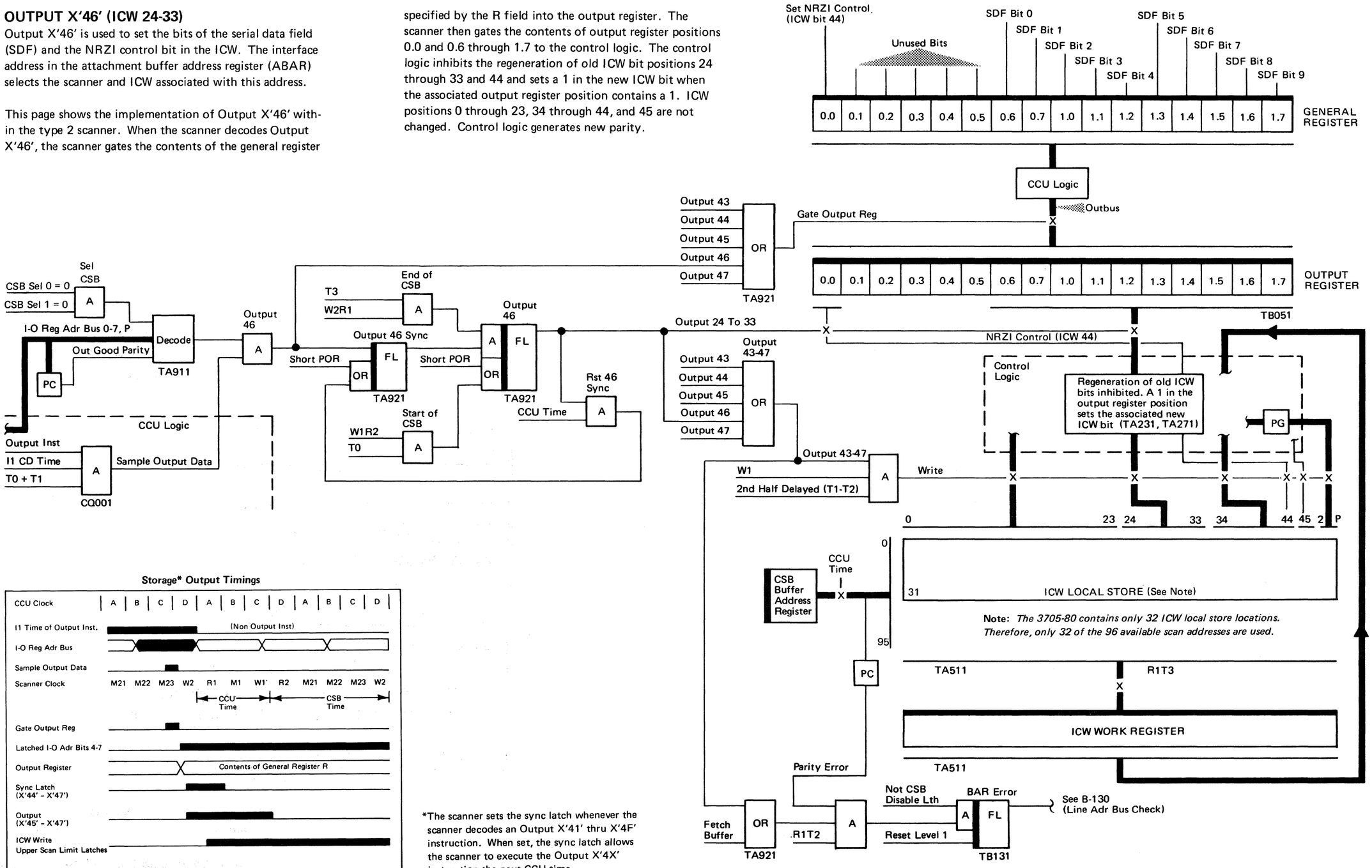
Storage* Output Timings

*The scanner sets the sync latch whenever the scanner decodes an Output X'41' thru X'4F' instruction. When set, the sync latch allows the scanner to execute the Output X'4X' instruction the next CCU time.

OUTPUT X'46' (ICW 24-33)

Output X'46' is used to set the bits of the serial data field (SDF) and the NRZI control bit in the ICW. The interface address in the attachment buffer address register (ABAR) selects the scanner and ICW associated with this address.

This page shows the implementation of Output X'46' within the type 2 scanner. When the scanner decodes Output X'46', the scanner gates the contents of the general register specified by the R field into the output register. The scanner then gates the contents of output register positions 0.0 and 0.6 through 1.7 to the control logic. The control logic inhibits the regeneration of old ICW bit positions 24 through 33 and 44 and sets a 1 in the new ICW bit when the associated output register position contains a 1. ICW positions 0 through 23, 34 through 44, and 45 are not changed. Control logic generates new parity.



Note: *The 3705-80 contains only 32 ICW local store locations. Therefore, only 32 of the 96 available scan addresses are used.*

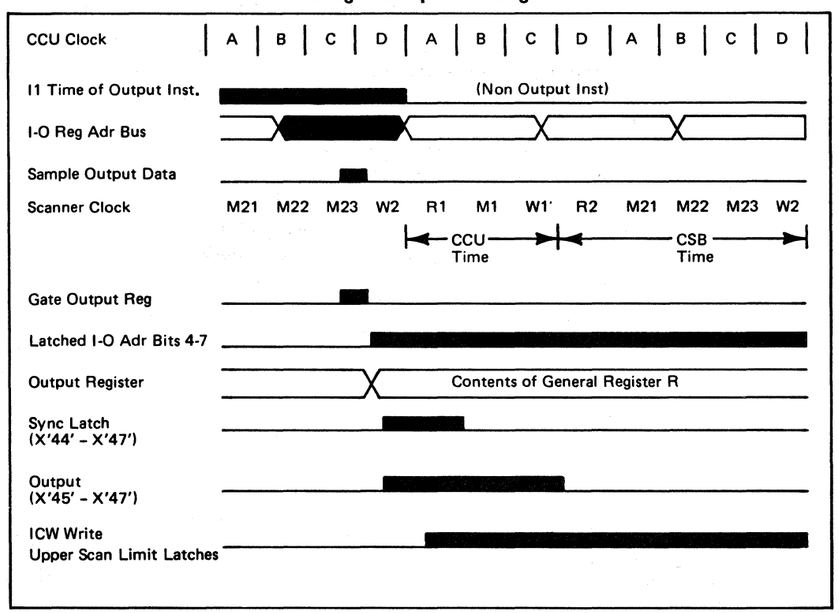
Storage* Output Timings

*The scanner sets the sync latch whenever the scanner decodes an Output X'41' thru X'4F' instruction. When set, the sync latch allows the scanner to execute the Output X'4X' instruction the next CCU time.

STORAGE TIMING OUTPUT X'44', X'45', X'46', and X'47'

Storage timings for Output instructions X'44' through X'47' are shown on this page.

Storage* Output Timings



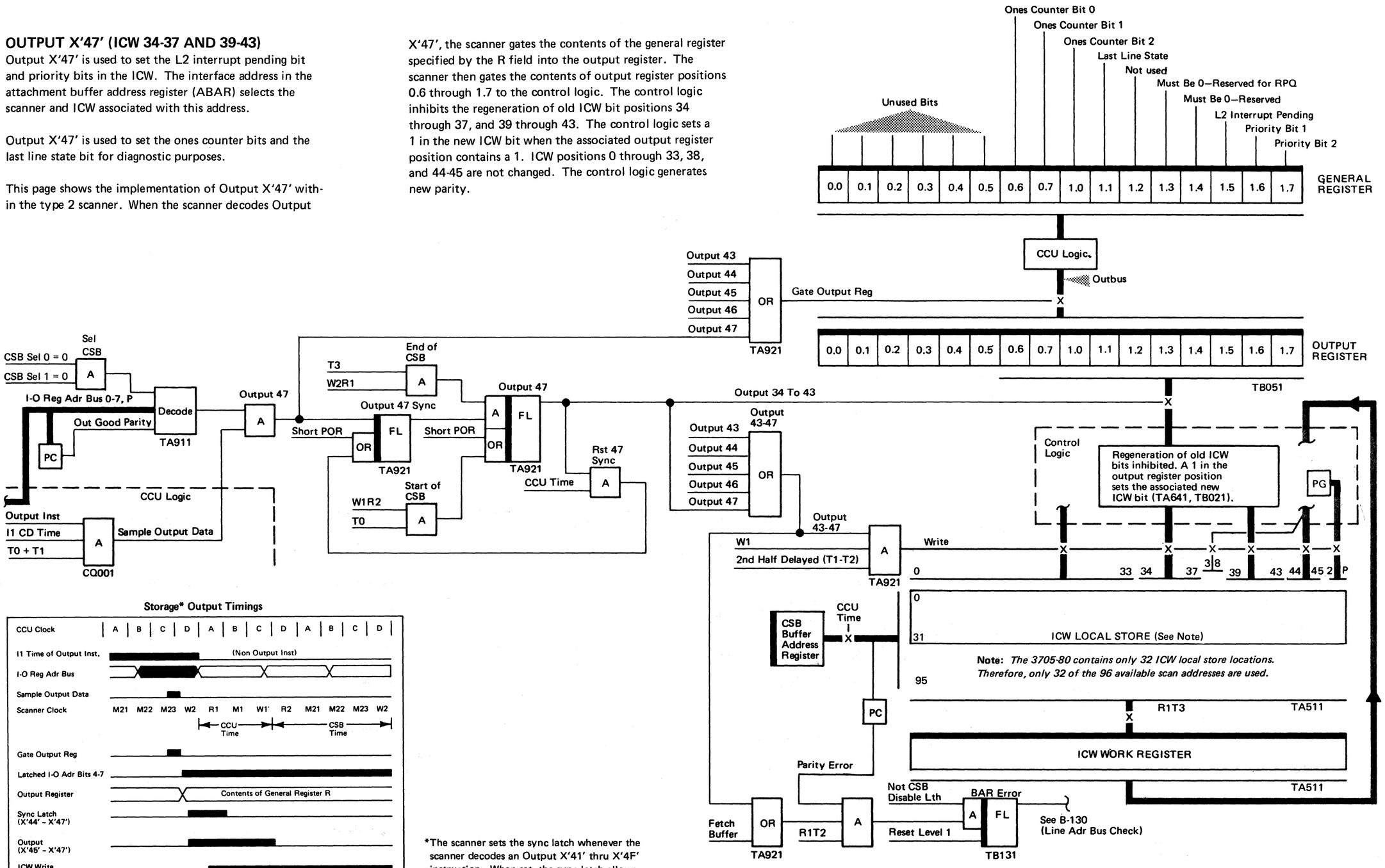
*The scanner sets the sync latch whenever the scanner decodes an Output X'41' thru X'4F' instruction. When set, the sync latch allows the scanner to execute the Output X'4X' instruction the next CCU time.

OUTPUT X'47' (ICW 34-37 AND 39-43)

Output X'47' is used to set the L2 interrupt pending bit and priority bits in the ICW. The interface address in the attachment buffer address register (ABAR) selects the scanner and ICW associated with this address.

Output X'47' is used to set the ones counter bits and the last line state bit for diagnostic purposes.

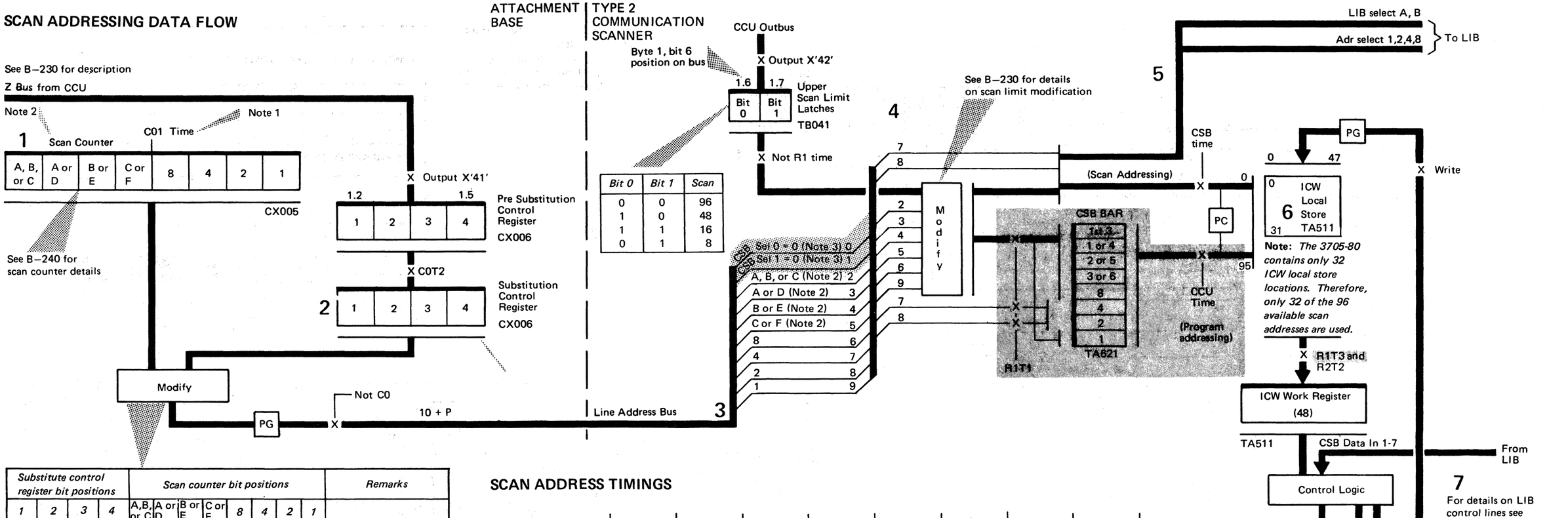
This page shows the implementation of Output X'47' within the type 2 scanner. When the scanner decodes Output X'47', the scanner gates the contents of the general register specified by the R field into the output register. The scanner then gates the contents of output register positions 0.6 through 1.7 to the control logic. The control logic inhibits the regeneration of old ICW bit positions 34 through 37, and 39 through 43. The control logic sets a 1 in the new ICW bit when the associated output register position contains a 1. ICW positions 0 through 33, 38, and 44-45 are not changed. The control logic generates new parity.



Storage* Output Timings

*The scanner sets the sync latch whenever the scanner decodes an Output X'41' thru X'4F' instruction. When set, the sync latch allows the scanner to execute the Output X'4X' instruction the next CCU time.

SCAN ADDRESSING DATA FLOW

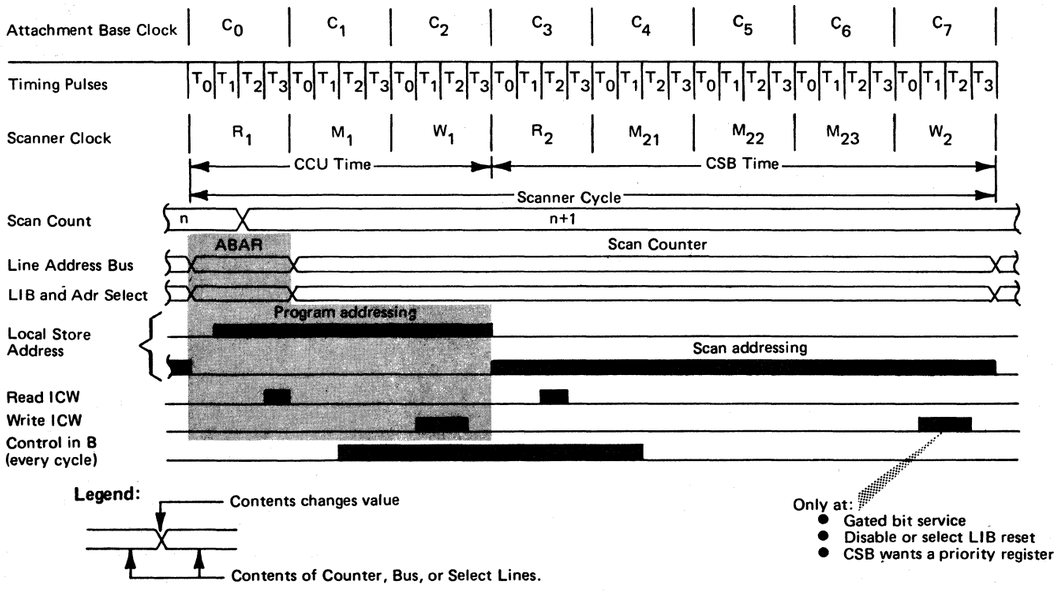


Substitute control register bit positions				*Scan counter bit positions*								*Remarks*
1	*2*	*3*	*4*	A,B, or C	A or D	B or E	C or F	*8*	*4*	*2*	*1*	
				LIB				*Interface Address*				
Sub cntl Reg 1 = 1 If Scan Counter interface adr = E or F, force bit positions as shown.				X	X	X	X	1	1	1	X	Substitution Configuration (intf adr = E or F
				1	1	0	0	0	0	0	0	Modified adr = 020
Sub cntl Reg 2 = 1 If Scan Counter intf adr. = C or D, force bit positions as shown.				X	X	X	X	1	1	0	X	Substitution Configuration (intf adr = C or D
				1	1	0	0	0	0	1	0	Modified adr = 022
Sub Cntl Reg 3 = 1 If Scan Counter intf adr. = A or B, force bit positions as shown.				X	X	X	X	1	0	1	X	Substitution Configuration (intf adr = A or B
				1	1	0	0	0	1	0	0	Modified adr = 024
Sub Cntl Reg 4 = 1 If Scan Counter intf adr. = 8 or 9, force bit positions as shown.				X	X	X	X	1	0	0	X	Substitution Configuration (intf adr = 8 or 9)
				1	1	0	0	0	1	1	0	Modified adr = 026

X = don't care bit

Any scan counter output that does not match the substitution configuration for the associated substitution control register is not modified.

SCAN ADDRESS TIMINGS



Notes:

1. *C01 steps every 2.0 microseconds.*
2. *A and B select respective LIBs. C, D, E, and F do not select LIBs or ICWs.*
3. *This bit must always be zero for the 3705-80.*

SCAN ADDRESSING

Description for B-220. The numbers refer to corresponding numbers on the data flow.

1 Scan Counter

The scan counter runs continuously, stepping through 96 different states. See B-240 for details on the scan counter positions and sequence of interface address outputs.

If the scan counter output is not modified, the type 2 scanner scans 96 different interface addresses in a period of 192 microseconds. Without modification, the scanner can not handle line speeds higher than 4,800 bps without the possibility of undetected bit overrun/underrun conditions.

Two modifications can be made to the scan counter output to allow the scanner to handle line speeds of up to 57,600 bps. These modifications are made in conjunction with the substitution control register and the upper scan limit latches.

2 Address Substitution

The bit configuration in the substitution control register determines how the scan counter output is modified. The chart on B-220 shows which scan counter bit positions are modified for each substitution control register position. This modification causes certain fixed interface addresses assigned to line interface base (LIB) position A to be substituted on the line address bus for certain normal scan counter output states. When operating in this manner, the type 2 scanner is forced to scan the fixed address, or addresses, with an effective scan period of 16.0 microseconds. This is because address substitution occurs every eighth time the scan counter changes state (see B-240 for the scan counter sequence). This allows the fixed address, or addresses, in each scanner to handle line speeds up to 57,600 bps, independent of the state of the upper scan limit latches in the scanner.

The following table shows which addresses are substituted, and which addresses are not scanned as a result of that substitution when the different substitution control register bits are on.

Substitution Ctrl Reg Bit	*Fixed Address Substituted in the Type 2 Scanner If Substitution Ctrl Reg Bit is ON*	*Addresses Not Scanned in the Type 2 Scanner If Substitution Ctrl Reg Bit is ON*
1	Adr 0 in LIB position A	Adr E and F in LIB positions A-F (See Note)
2	Adr 2 in LIB position A	Adr C and D in LIB positions A-F (See Note)
3	Adr 4 in LIB position A	Adr A and B in LIB positions A-F (See Note)
4	Adr 6 in LIB position A	Adr 8 and 9 in LIB positions A-F (See Note)

Note: *A and B select respective LIBs. C, D, E, and F do not select LIBs or ICWs.*

3 Line Address Bus

Ten address bits plus a parity bit are on the line address bus, but for scan addressing, CSB sel 0 and CSB sel 1 are ignored. Parity is generated over the eight bit address on line address bus positions 2-9.

4 Upper Scan Limit Modification

The type 2 scanner has two upper scan limit latches. The scanner modifies the address on the line address bus according to the state of its upper scan limit latches. See the chart to the right for the actual line address bit positions modified by the four states of the upper scan limit latches. The line address bus output may be modified in some form as shown in the chart.

If the scan counter output is not modified by address substitution, the four states of the upper scan limit latches create the following effective scan periods:

3705-80

Upper Scan Limit State	*Actual Scan Counter Period*	*Number of Interfaces actually scanned by Scanner*	*Number of times each Interface is scanned in Scan Counter Period*	*1.0 usec Cycle Time Effective Scan Period*
00	192 usec	96	1	*192 usec
10	192 usec	48	2	96 usec
11	192 usec	16	6	32 usec
01	192 usec	8	12	16 usec

*The effective scan period is for 96 addresses since the attachment base steps through 96 addresses.

5 LIB Select and Address Select

Every 2.0 microseconds, the scanner selects a line interface, or auto call interface, by sending the modified line address bus output to the LIB and interface by means of the LIB select and address select lines.

6 ICW Local Store

The type 2 scanner contains a local store array that contains 32 addressable interface control words (ICW). Each ICW contains 46 bits plus 2 parity bits. A distinct ICW is associated with each line interface, or autocall unit interface, attached to the scanner through a LIB. See chart on B-250 for the relationships between the modified line address bus output, ICW array selection, and interface address selected for the scanner.

See B-220 for scan address timings to read out and write into the ICW associated with the selected interface address. CSB time gates the address to the local store, and the contents of the selected ICW are placed in the ICW work register at R2T2 time. The scanner control logic examines the contents of this ICW and the 'control in B' status.

When a hardware interface bit service or a program service level 2 interrupt is required, the ICW contents are modified and written back into the local store at W2T1T2 time. If the ICW contents are not modified, they normally are not written into the local store array because the original contents are not destroyed during read-out.

7 LIB Control

The scanner control logic sends a 'control in B' signal to the selected interface which gates the status of certain data communications equipment lines and certain latches in the interface hardware back to the scanner. See B-260 for details.

UPPER SCAN LIMIT MODIFICATION OF LINE ADDRESS BUS

Upper Scan Limit	*Position*	*(Note) Address Bit Positions* A, B, or C	A or D	B or E	C or F	8	4	2	1	*Interface Lines Selected (See Note)*	*Modification Performed (See Note)*
00 (96 lines)	Line adr bus	1	↓	↓	↓	↓	↓	↓	↓	Sel A, B, or C	Invert 'A, B, or C' bit
	Local store adr	0								Adr sel y	
	Line addr bus	0	↓	↓	↓	↓	↓	↓	↓	Sel D, E, or F	Invert 'A, B, or C' bit
	Local store adr	1								Adr sel y	
10 (48 lines)	Line adr bus	X	↓	↓	↓	↓	↓	↓	↓	A, B, or C	Force 'A, B, or C' bit to 0
	Local store adr	0								Adr sel y	
11 (16 lines)	Line adr bus	X	X	X	X	↓	↓	↓	↓	Sel A	Force bit 'A or D' to 1 and 'A, B, or C', 'B or E', 'C or F' to 0.
	Local store adr	0	1	0	0					Adr sel y	
01 (8 lines)	Line adr bus	X	X	X	X	1	↓	↓	X	Sel A	If bit 8 = 1, force it to 0 and force bit 1 to 1. If bit 8 = 0, do not modify it, but force bit 1 to 0. In both cases, force bit 'A or D' to 1 and 'A, B, or C', 'B or E', 'C or F' to 0.
	Local store adr	0	1	0	0	0			1	Adr sel y	
	Line adr bus	X	X	X	X	0	↓	↓	X	Sel A	
	Local store adr	0	1	0	0	0			0	Adr sel y	

↓ indicates no modification

X indicates don't care

Upper scan limit = 01 forces this interface line selection sequence if address substitution has not modified the scan counter sequence.

Modified Line Adr Bus Position 8	4	2	1	*Line Selected within LIB A*
0	0	0	0	0
0	0	1	0	2
0	1	0	0	4
0	1	1	0	6
0	0	0	1	1
0	0	1	1	3
0	1	0	1	5
0	1	1	1	7

SCAN COUNTER

- Stepped every 2.0 microseconds at C01 time (see B-220).
- There are 96 different states—one for each interface address in the communication scanner. Although 96 addresses are scanned, only the first 32 addresses (00-31) are used in the 3705-80.
- The relationship of the output state of the scan counter with respect to the line address bus bit positions is shown in the chart.

  Position 'A, B, or C' — A one indicates A, B, or C is selected.

  A zero indicates D, E, or F is selected.

  Position 'A or D' — A one selects A if position 'A, B, or C' is a one, or D if position 'A, B, or C' is a zero.

  Position 'B or E' — A one selects B if position 'A, B, or C' is a one, or E if position 'A, B, or C' is a zero.

  Position 'C or F' — A one selects C if position 'A, B, or C' is a one, or F if position 'A, B, or C' is a zero.

  Only one position from among 'A or D', 'B or E', and 'C or F', can be active at a time.

  These four positions define the selection of A through F. C, D, E, and F do not select LIBs or ICWs. However, A and B do select respective LIBs.

  Positions 8, 4, 2, 1 form the hex representation for the line address within the selected LIB.
- The scan counter generates interface addresses in the sequence shown in the chart. The LIBs are selected in sequence—however, the even interface addresses within each LIB are generated consecutively, followed by the odd interface addresses.

SEQUENCE OF INTERFACE ADDRESSES GENERATED BY SCAN COUNTER

Interface Address (Hex)	*Scan Counter Bit Positions*								*LIB Selected*	*Interface Line Selected*
	A, B, or C	*A or D*	*B or E*	*C or F*	*8*	*4*	*2*	*1*		
	← LIB Address →				← Interface line within selected LIB →					
020	1	1	0	0	0	0	0	0	A	0
022	1	1	0	0	0	0	1	0		2
024	1	1	0	0	0	1	0	0		4
026	1	1	0	0	0	1	1	0		6
028	1	1	0	0	1	0	0	0		8
02A	1	1	0	0	1	0	1	0		A
02C	1	1	0	0	1	1	0	0		C
02E	1	1	0	0	1	1	1	0		E
021	1	1	0	0	0	0	0	1		1
023	1	1	0	0	0	0	1	1		3
025	1	1	0	0	0	1	0	1		5
027	1	1	0	0	0	1	1	1		7
029	1	1	0	0	1	0	0	1		9
02B	1	1	0	0	1	0	1	1		B
02D	1	1	0	0	1	1	0	1		D
02F	1	1	0	0	1	1	1	1	A	F
030	1	0	1	0	0	0	0	0	B	0
↓	↓	↓	↓	↓	Even lines then odd lines				↓	↓
03F	1	0	1	0	1	1	1	1	B	F
040	1	0	0	1	0	0	0	0		
↓	↓	↓	↓	↓	Even lines then odd lines					
04F	1	0	0	1	1	1	1	1		
050	0	1	0	0	0	0	0	0		
↓	↓	↓	↓	↓	Even lines then odd lines					
05F	0	1	0	0	1	1	1	1		
060	0	0	1	0	0	0	0	0		
↓	↓	↓	↓	↓	Even lines then odd lines					
06F	0	0	1	0	1	1	1	1		
070	0	0	0	1	0	0	0	0		
↓	↓	↓	↓	↓	Even lines then odd lines					
07F	0	0	0	1	1	1	1	1		

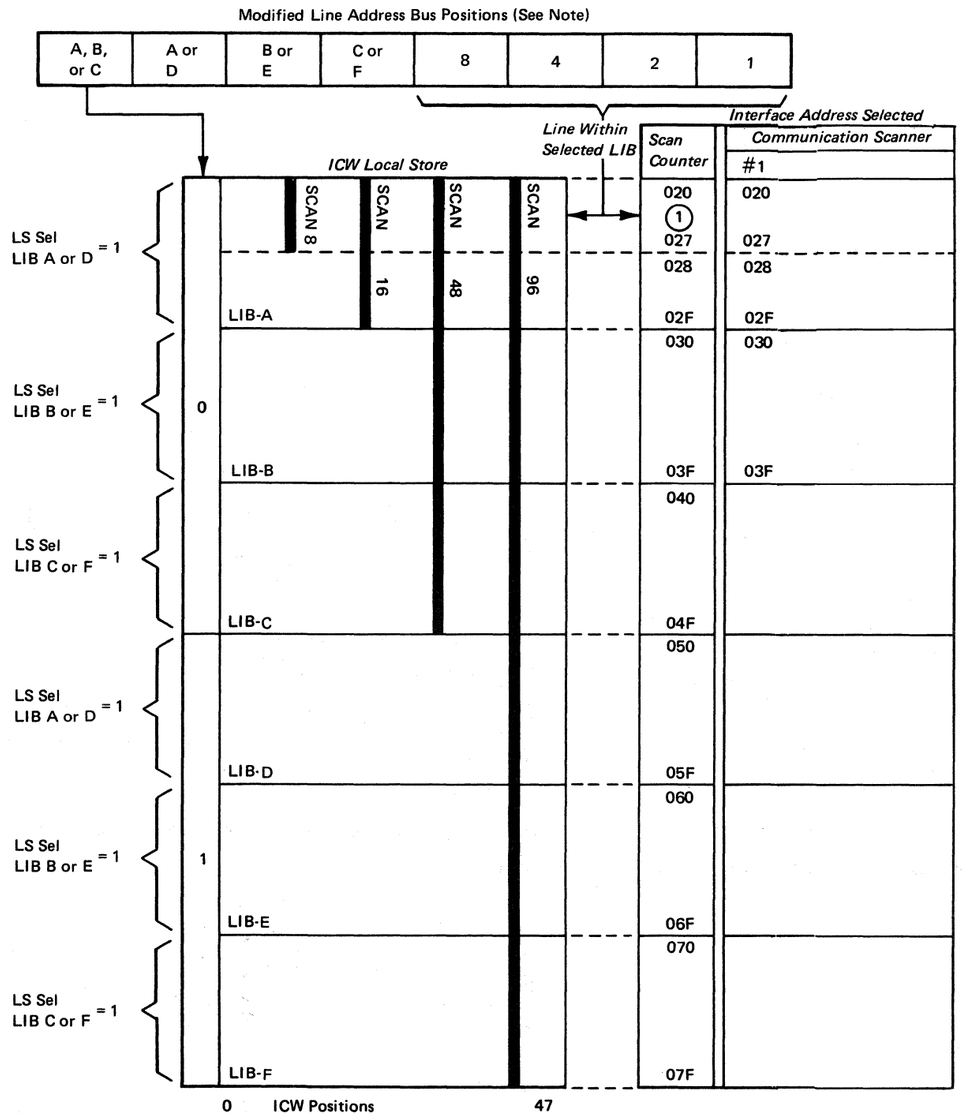
SCAN ADDRESSING EXAMPLES

Position	Address Positions (See Note)								Interface Lines Selected	ICW Local Store Adr Selected	Modification Performed
	A, B, or C	A or D	B or E	C or F	8	4	2	1			
EXAMPLE 1: All Substitution Ctrl Registers = 0, Upper Scan Limit = 00 (96 lines)											
Scan Counter	1	1	0	0	0	1	1	1			See B-240
Line Address Bus	1	1	0	0	0	1	1	1			No Adr Substitution
Modified Local Store Adr	0	1	0	0	0	1	1	1	Sel LIB A Adr sel 7	027 (1)	Upper Scan Limit
EXAMPLE 2: Substitution Ctrl Reg Bit 1 = 1, Upper Scan Limit = 11 (16 lines)											
Scan Counter	1	1	0	0	1	1	1	0			See B-240
Line Address Bus	1	1	0	0	0	0	0	0			Adr Substitution
Modified Local Store Adr	0	1	0	0	0	0	0	0	Sel LIB A Adr sel 0	020	Upper Scan Limit
EXAMPLE 3: Substitution Ctrl Reg Bit 4 = 1, Upper Scan Limit = 00 (96 lines)											
Scan Counter	0	0	0	1	1	0	0	1			See B-240
Line Address Bus	1	1	0	0	0	1	1	0			Adr Substitution
Modified Local Store Adr	0	1	0	0	0	1	1	0	LIB sel 1-intf 1 Adr sel 6-intf 1 & 2	026 (2)	Upper Scan Limit
EXAMPLE 4: Substitution Ctrl Reg Bit 2 = 1, Upper Scan Limit = 01 (8 lines)											
Scan Counter	1	1	0	0	1	0	0	0			See B-240
Line Address Bus	1	1	0	0	1	0	0	0			No Adr Substitution
Modified Local Store Adr	0	1	0	0	0	0	0	1	Sel LIB A Adr sel 1	021	Upper Scan Limit
EXAMPLE 5: Substitution Ctrl Reg Bit 3 = 1, Upper Scan Limit = 10 (48 lines)											
Scan Counter	0	1	0	0	1	1	1	0			See B-240
Line Address Bus	0	1	0	0	1	1	1	0			No Adr Substitution
Modified Local Store Adr	0	1	0	0	1	1	1	0	Sel LIB A Adr sel E	02E	No Upper Scan Limit
EXAMPLE 6: All Substitution Ctrl Registers = 0, Upper Scan Limits = 01 (8 lines)											
Scan Counter	0	0	0	1	0	1	1	1			See B-240
Line Address Bus	0	0	0	1	0	1	1	1			No Adr Substitution
Modified Local Store Adr	0	1	0	0	0	1	1	0	Sel LIB A Adr sel 6	026 (3)	Upper Scan Limit

Note: *A and B selective respective LIBs. C, D, E, and F do not select LIBs or ICWs.*

These addresses do not appear as such during scan addressing, but are seen in ABAR during a program level 2 interrupt as shown on B-330.

ICW LOCAL STORE/SELECTED INTERFACE ADDRESS RELATIONSHIP TO SCAN ADDRESSING



DATA IN/OUT–LIB TO SCANNER (PART 1 OF 2)

See B-270 for description of numbered control circuits

- Set Mode
- Disable (PCF X'F')
- CSB Disable (see B-170)
- Select LIB Reset (See B-170)

- Transmit Bit SVC
- Dial Bit SVC
- CSB Disable
- Select LIB Reset (see B-170)
- Disable (PCF X'F') (see B-170)

SCANNER | LIB

LIBs A or B — A — Control In A — (Interface string) — 4

LIBs A or B — A — Control Out A — (Interface String) — 3

Serial Data Field Positions: 3 4 5 6 7 8 9 (1 2 3 4 5 6 7)

Data Out (1-7) — (1)

Sel Line X — A

A Register

1	Diag Mode
2	Data Terminal Ready
3	Sync Mode
4	External Clock
5	Data Rate Select
6	OSC Sel Bit 1
7	OSC Sel Bit 2

Feedback Test

Logic Pages for Line Set

A/B Registers	*Logic Page*
LS1	VB160
LS2	VB140
LS3 (HDX)	VB100
LS3X (Duplex)	VB120
LS4	VB080
LS5	VB150
LS8	VB200
LS9	VB200

Data In (1–7) — Data In (1–7)

Late Sample R2T1 — 2 — Early Sample W1T3

B Data Register TA331: 1 2 3 4 5 6 7

B data register contains only the status gated by control in B

All 7 Data In lines checked for feedback error — (1) — OE TA341 — OR

Gated Bit Svc — A TA111 — Feedback Error — 5

- Force X'F' in LCD
- Inhibit Set of SCF 1 (svc req)

FEEDBACK TEST

SCANNER

Sel Line X — A

1	Clear To Send
2	Ring Indicator
3	Data Set Ready
4	Rcv Line Signal Detector
5	Rec Data Buffer
6	Diag Mode
7	Bit Svc Request

LINE INTERFACE

AUTOCALL INTERFACE

Sel Line Y — Control In B — A — (3)

1	Abandon Call and Retry
2	Present Next Digit
3	Data Line Occupied
4	Power Indicator
5	Unused
6	Call Originating Status
7	Bit Service Request

Sets SDF 2

Sets SDF 5

Sel Line Z — Control Out B — A — (2)

B Register

2	Call Request (CRQ)
3	Digit Present (DPR)
4	Digit Number 8
5	Digit Number 4
6	Digit Number 2
7	Digit Number 1

Feedback Test

LIBs A or B — A — Control In B — (Interface string) — 1

Control In B LTH (every scan cycle) — TA331

LIBs A or B — A — Control Out B (Interface String) — 6

Sel Line X — A

B Register

3	Rcv Data Space
4	Xmit Mode
5	New Sync
6	Request To Send
7	Send Data Buffer

Feedback Test

Data Out (1–7) — (1)

4	Xmit Mode [Transmit PCF 8,9,A,B, C, or D (Not Tag or SDLC)]
5	New Sync (When in BSC or SDLC and PCF State A) Note
6	Request To Send (Transmit PCF 8,9,A,B,D, or (C and Not Tag)
7	Send Data
2	SDF 2 Call Request (When in Dial PCF States 4,5, or 8)
3	SDF 5 Digit Present (When in Dial PCF State 8)
4	PDF 4 Digit Number 8 (When in Dial PCF State 8)
5	PDF 5 Digit Number 4 (When in Dial PCF State 8)
6	PDF 6 Digit Number 2 (When in Dial PCF State 8)
7	PDF 7 Digit Number 1 (When in Dial PCF State 8)

LIBs A or B — A — Control In C — (Interface String) — 7

1 Sets SCF 0 (Receive Break) for start-stop

Note: *BSC state A should not be used if the new sync latch is not present in the line interface; otherwise, a feedback check may occur.*

SCANNER | LIB

DATA IN/OUT LIB INTERFACE (PART 2 OF 2)

Description for B-260. The numbers refer to control circuits shown on B-260.

1 Every 2.0 microseconds during scan addressing, the type 2 scanner selects a line interface, or auto call interface, by sending that interface address to the LIB and interface over the 'LIB select' and 'address select' lines (See Note). The scanner sends a 'control in B' signal to the interface that gates the status of certain data communication equipment lines and certain latches in the interface hardware back to the scanner.

2 This status is stored in the B data register and is available to the control logic and the display register. See B-150 for the status bits buffered in the B data register.

3 PCF state X'1' (set mode) gates the set mode SDF bit configuration over the data out lines and gates this data into the 'A register' of the scanned interface by sending the 'control out A' signal. Bit service request is not required to set the 'A register'.

4 The scanner ensures the latches are set to the correct value by sending 'control in A' to the interface hardware which gates feedback signals (from those latches just set) over the data-in lines to the scanner.

5 At gated bit service, if any latch does not agree with the value to which it was to have been set, a feedback error results which sets the LCD field to hex 'F'. This temporarily suspends scanner-to-interface action for that line. Level-2 interrupts for the faulty interface are also suppressed except for set mode. These errors must be recognized by a periodic scan of the LCD fields for all interfaces. The 3705-80 interval timer is used to provide this periodic scan of the LCD fields. Line and autocall interface feedback error detection is at the interface level; but if failures are detected in a group of interfaces, the interface hardware, type 2 scanner hardware or program logic may be at fault.

6 With 'bit service' on, a transmit or autocall operation sends 'control out B' to the interface and control logic places the appropriate bits on the data out lines.

7 The 'control in C' signal, sent to the interface, causes a feedback test.

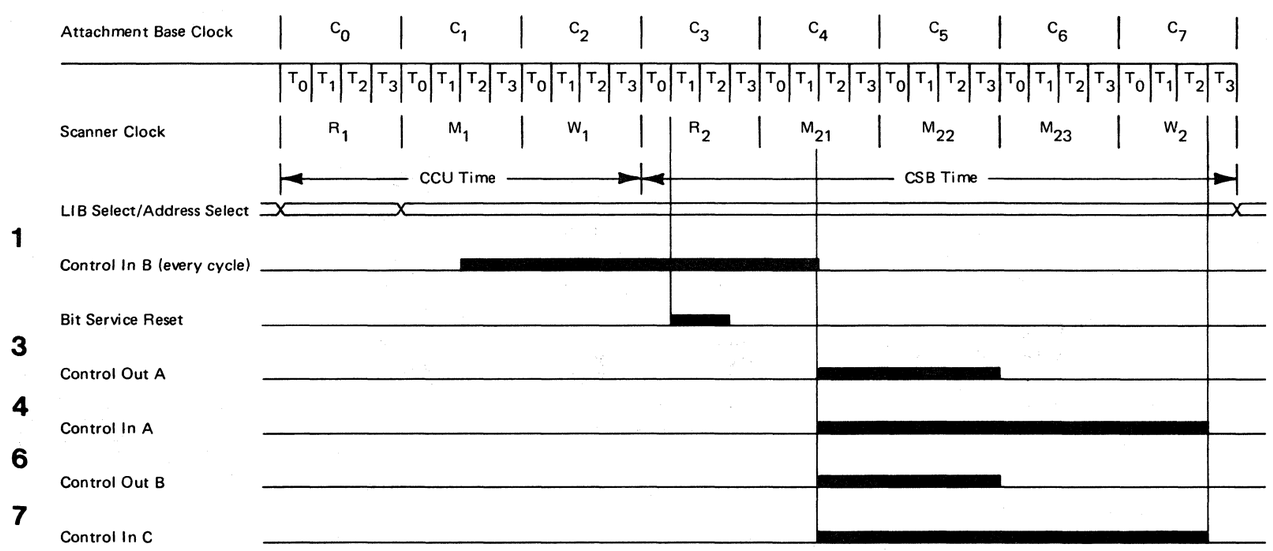
3 & 6 The CSB disable latch turns on by executing Output X'43' (1 in byte 0, bit 0 and 1 in byte 1, bit 6), by an IPL reset, by the control panel Reset pushbutton, or by power on/off reset. When the CSB disable latch is on, the data out lines are held off while 'control out A' and 'control out B' are sent to the interface to reset the hardware latches. A feedback test then occurs. (See B-170.)

3 With bit service on, a disable (PCF state F) sends 'control out A' and 'control out B', to the interface with data out lines held off to reset the control latches in the LIB. The fall of 'data terminal ready' signals the data communications equipment that the interface is disabled and for the data communications equipment to terminate that connection. A feedback test then occurs. (See B-460.)

3 & 6 When Output X'43' is executed with the set function on (1 in 0.0) and any 'disable LIB position 1-6' on (1 in corresponding byte and bit position), the line 'select LIB reset' is active while scanning the interface/autocall lines on the disabled LIB. At this time the data out lines are held off while 'control out A' and 'control out B' are sent to the interface to reset the hardware latches. A feedback test then occurs. (See B-170.)

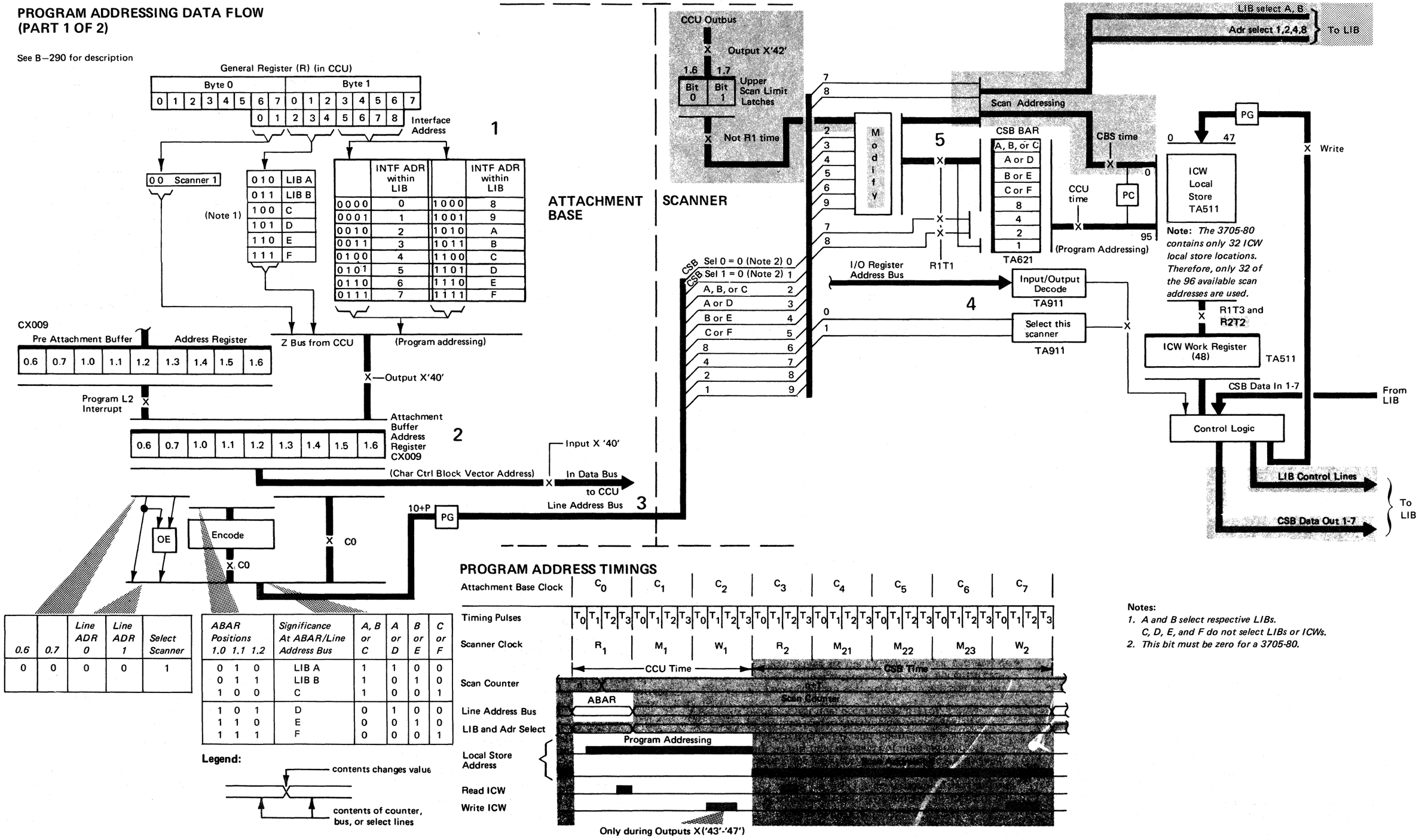
- Two signals are sent from the type 2 scanner to the interface without any control signals to gate them. These are the 'reset bit service' and 'test data' lines.
  - The 'reset bit service' line resets the 'bit service' latch in the interface hardware on the cycle in which it is sensed. This notifies the interface hardware that the service request has just been honored. A feedback check then occurs.
  - When diagnostic wrap mode is used, the scanner places the transmitted data of the diagnostic transmit line in a 'test data' latch in the type 2 scanner hardware. The receive lines sample the state of this 'test data' latch and use it as received data.
- Bit Overrun Reset
  Grounded in the scanner
- LIB Active In
  Held at the down level in the scanner

SCANNER INTERFACE TIMING TO LIBS



PROGRAM ADDRESSING DATA FLOW (PART 1 OF 2)

See B–290 for description



0.6	0.7	Line ADR 0	Line ADR 1	Select Scanner
0	0	0	0	1

ABAR Positions 1.0 1.1 1.2	Significance At ABAR/Line Address Bus	A, B or C	A or D	B or E	C or F
0 1 0	LIB A	1	1	0	0
0 1 1	LIB B	1	0	1	0
1 0 0	C	1	0	0	1
1 0 1	D	0	1	0	0
1 1 0	E	0	0	1	0
1 1 1	F	0	0	0	1

Legend:

PROGRAM ADDRESS TIMINGS

Notes:

1. *A and B select respective LIBs. C, D, E, and F do not select LIBs or ICWs.*
2. *This bit must be zero for a 3705-80.*

Note: *The 3705-80 contains only 32 ICW local store locations. Therefore, only 32 of the 96 available scan addresses are used.*

PROGRAM ADDRESSING DATA FLOW (PART 2 OF 2)

Description for B-280. The numbers refer to corresponding numbers on part 1 of the data flow.

The control program handles the service requirements of the line interfaces—one at a time. The control program does this by executing input and output instructions. Program addressing refers to the period of the scanner cycle during which the input and output instructions are implemented in the attachment base and scanner. This occurs during CCU time of the scanner cycle.

Before the program can examine or modify fields in an interface control word (ICW) associated with a particular interface, the address of that interface must be placed in the attachment buffer address register (ABAR) of the type 2 attachment base. Similarly, before the program can access certain registers in the type 2 scanner, or perform control functions in the scanner, the interface address in the ABAR must be one of those assigned to that scanner. Two distinct events cause the contents of the ABAR to change:

(1) When a program level 2 interrupt occurs, the ABAR contents are automatically set by the attachment base with the interface address from the highest priority register occupied. The interrupt program executes Input X'40' to determine the interface address in ABAR. The program can then examine and/or modify fields in the ICW associated with this interface.

(2) In program levels 1, 3, and 4, the program may have to examine certain registers in the scanner or perform miscellaneous control functions in the scanner. Furthermore, in program level 3 or 4, the program may need to access the ICW associated with a specific interface. By executing Output X'40' under such circumstances, the program can cause the ABAR to be set according to the interface address in the general register specified by R.

Note: *To avoid conflicts with the automatic mechanism which sets ABAR when a program level 2 interrupt occurs, programs executing at program level 3 or 4 should mask program level 2 interrupts before executing Output X'40'. If more than one program level is likely to execute Output X'40', additional program interlocks should be established between those levels by the user.*

The following numbered items pertain to the program addressing data flow on B-280.

1 Interface Addresses

The lines attached to the 3705-80 are assigned interface addresses at installation time. The interface address assigned to a given line is determined by the physical position of the line interface hardware in the LIB through which the line is attached. The control program identifies each line by means of the nine-position interface address. The nine bits define the scanner position, LIB position, and the line within the LIB as shown in the charts on B-280.

2 ABAR (Attachment Buffer Address Register)

ABAR buffers the nine interface address bits for program addressing the scanner.

3 Line Address Bus

Three ABAR positions (1.0-1.2) are encoded to four bits and then gated to the line address bus for 250 nanoseconds (C0 time). C0 time also gates ABAR positions 1.3-1.6 to the line address bus. ABAR positions 0.6-0.7 (interface address bits 0-1) are placed on the line address bus continuously. Since they can be changed by an Output X'40', or a program level 2 interrupt during the scanner cycle, they are not included in the line address bus partiy.

4 Scanner Select

Line address bus positions 0-1 select the scanner. The scanner decodes the input and output instructions and performs the required function. The accompanying diagram shows the conditions under which a feedback error can occur during scanner selection.

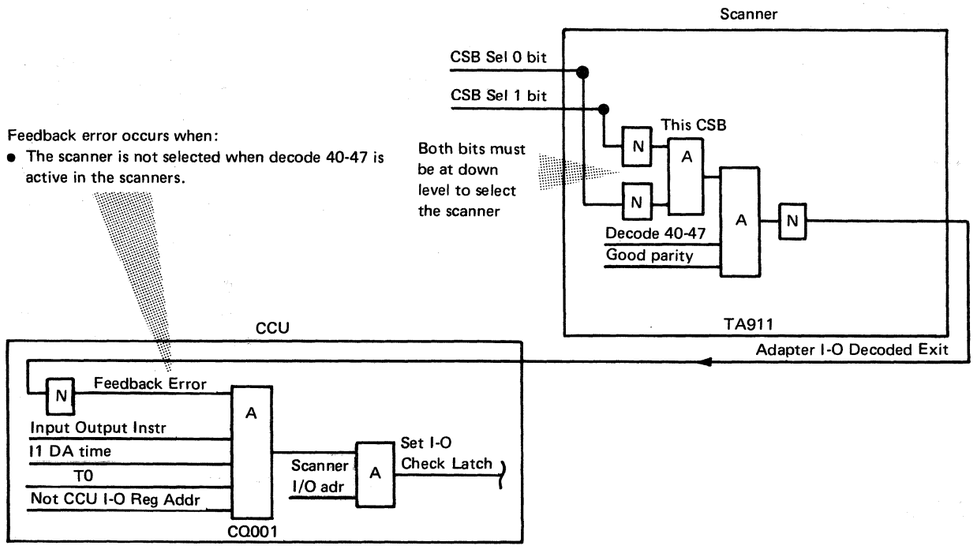
5 CSB BAR (Buffer Address Register)

The line address bus is gated into the CSB BAR at R1T1 time. The line address passes through the upper scan limit modify logic but the upper scan limit latch output is degated at R1 time, and no modification occurs.

6 ICW Local Store

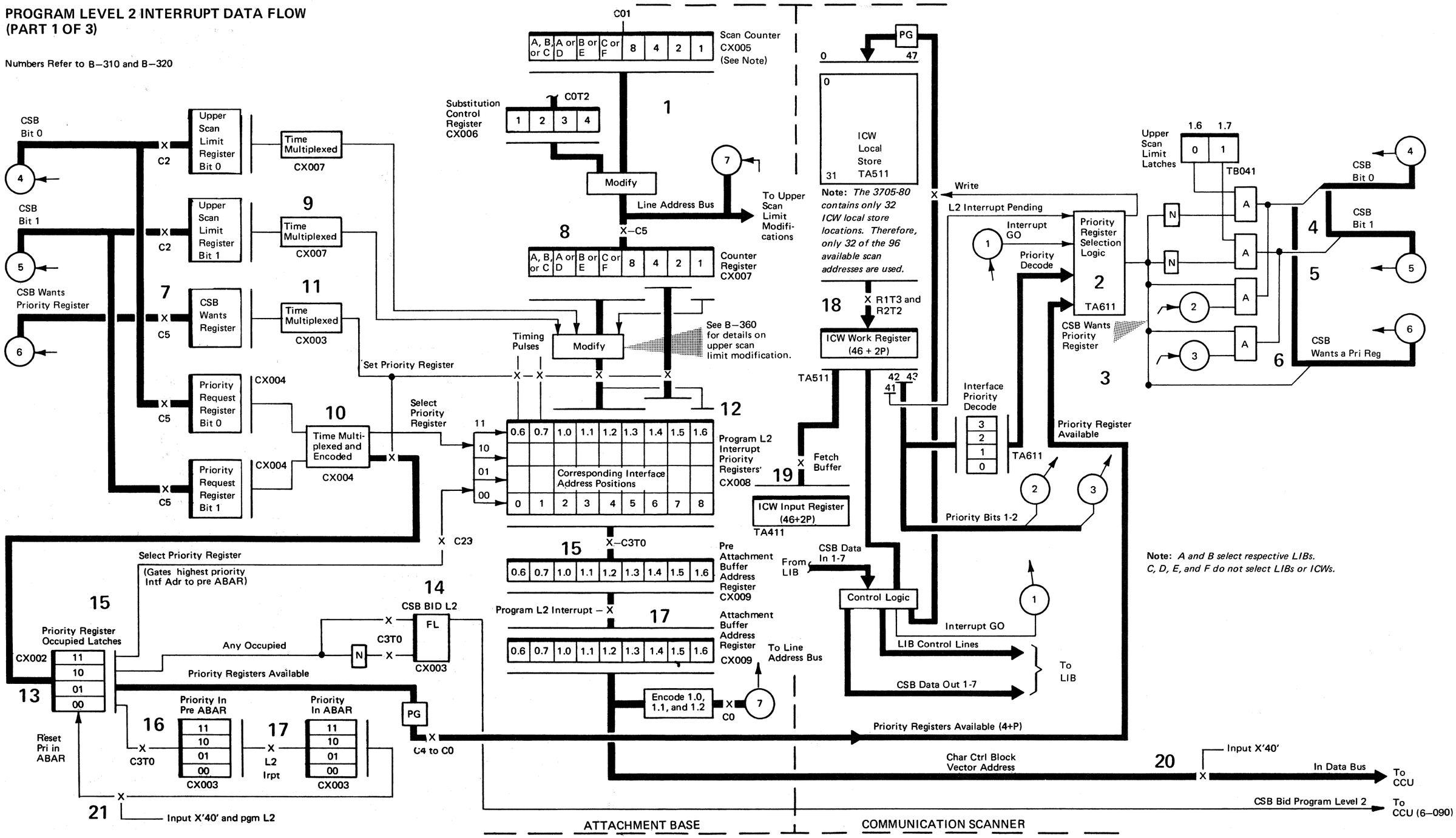
At CCU time, the line address in the CSB BAR selects the associated ICW from the ICW local store. The content of the ICW is read into the ICW work register at R1T3 time. The scanner is addressed and the contents of the ICW read out during CCU time. New data is written into the ICW associated with the line address when OUTPUT X'43-47' instructions are decoded.

Scanner Select And I/O Check Detection



PROGRAM LEVEL 2 INTERRUPT DATA FLOW (PART 1 OF 3)

Numbers Refer to B–310 and B–320



Note: *A and B select respective LIBs. C, D, E, and F do not select LIBs or ICWs.*

PROGRAM LEVEL 2 INTERRUPT DATA FLOW (PART 2 OF 3)

Numbers refer to B-300

1 During scan addressing, the scan counter output, modified as required by the substitution control register, selects an interface address and a LIB in the type 2 scanner. The ICW associated with the interface address is read into the scanner ICW work register.

2 The availability of the priority registers in the type 2 attachment base are sent to the scanner. If control logic determines that a condition requiring a level 2 interrupt is present (A), it signals 'interrupt go' to the priority register selection logic. Likewise, if a level 2 interrupt is pending from a previously sensed 'interrupt go' condition, this is signaled to the priority register selection logic.

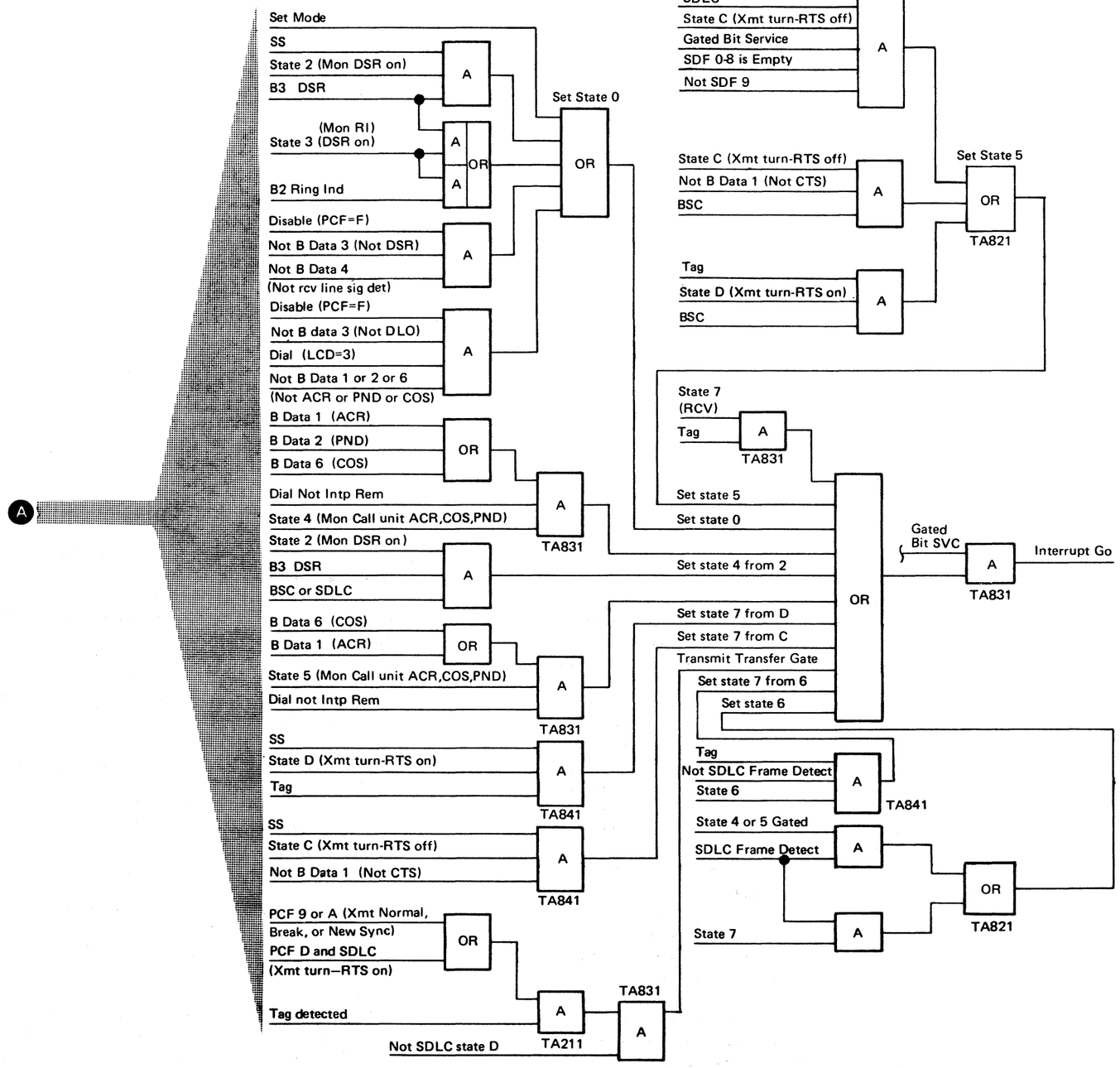
3 The interface priority is decoded from ICW bits 42 and 43. This priority selects the corresponding register from the 'priority registers available' from the attachment base when 'interrupt go' or 'level 2 interrupt pending' is signaled, and activates the line 'CSB wants a priority register' with the following results:

- Write gate causes the unmodified ICW work register contents and all modified bit positions to write into the ICW local store address selected during this CSB time.
  - 'Interrupt go' sets SCF 1 (service request) if there were no feedback errors and if SCF 0 (stop bit check/rcv break), SCF 2 (char overrun/underrun), and SCF 3 (modem check) are not set.
  - L2 interrupt pending bit (ICW bit 41) is set if the priority register wanted is not available from the attachment base.
  - ICW parity bits are changed accordingly.

4 • The state of the upper scan limit bits 0 and 1 were returned to the attachment base over the bit 0 and 1 buses at C2 time, before the 'CSB wants a priority register' signal. The scanner places the 0 and 1 bits associated with its upper scan limit on the scanner bit 0 and bit 1 buses. The upper scan limit state from the scanner is placed in the upper scan limit bit 0 and 1 register at C2 time.

Note: *The relationship of the conditions that cause 'interrupt go' and the PCF states is shown on B-080.*

Conditions that cause Level 2 Interrupt
(located in control logic on B–300)



Note: *The relationship of the conditions that cause 'interrupt go' and the PCF states is shown on B-080*

PROGRAM LEVEL 2 INTERRUPT DATA FLOW (PART 3 OF 3)

5 The scanner may select a priority register from the remaining 'priority registers available' lines coming into the scanner from the attachment base.

See B-340 for the following example. All priority registers are available to the scanner which wants priority register 3 (11). If priority register 3 is not available, the scanner sets L2 interrupt pending bit 41 in the ICW and waits for priority register 3 to
6 become available on a future scan. When priority register 3 becomes available, the scanner gates its priority bits to the bit 0 and bit 1 buses. The priority
7 bits for the scanner are gated into the priority request bit 0 and priority request bit 1 register at C5 time.

8 The scan counter output (modified as required by the substitution control register) is placed into the counter register and buffered. It is modified by the upper scan limits from the scanner according to the corresponding chart on B-360. This modification is required since the scanner's upper-scan limits modified the scan counter output in selecting the interface address and associated ICW. The same modification must be made in the attachment base for the scanner to return to the program interface address that caused the level 2 interrupt.

9 The upper scan limit register bits 0 and 1 are time-multiplexed as shown on B-340. The scanner modification occurs at C01 time.

10 The priority request register bits 0 and 1 are time-multiplexed in the same way (see B-340). The 0 and 1 bits are encoded to select one of the associated priority registers at each time.

11 The 'CSB wants register' output is likewise time-multiplexed to generate the set priority register pulses. These pulses set the modified counter register contents (interface address) into the priority register selected by the associated select priority pulses. In addition, the scanner identification code is gated into priority register positions 0.6 and 0.7. This code is formed as shown on B-340 and identified as 'bits 0.6 and 0.7 to priority reg'.

12 Four program level 2 interrupt priority registers are in the type 2 attachment base. Each priority register has a different priority, with priority 11 (3) the highest. Each interface address is assigned to one of these four priorities via the priority select bits 1-2 (ICW bits 42-43). The higher speed lines should be assigned a higher priority than the lower speed lines to avoid a character overrun (receiving), or underrun (transmitting).

13 At the same time the interface address is set into the selected priority register, the selecting priority is set into the associated 'priority register occupied' latch. This results in the following:

14 • As long as any occupied latch is set, the CSB bid level 2 latch is set. This causes the type 2 attachment base to bid for a program level 2 interrupt in the CCU. The State of the CSB bid L2 latch may be inspected by the program executing Input X'77'.

15 • The highest priority in the occupied latches selects that priority register and causes its contents to read into the pre ABAR (attachment buffer address register).

16 • The highest priority value is also set in the corresponding 'priority in pre ABAR' latch.

17 When the CCU accepts the program level 2 bid, the line 'prog lev 2 next' gates the interface address that caused the interrupt from the pre ABAR to the ABAR, and gates the priority value from the 'priority in pre ABAR' latch into the corresponding 'priority in ABAR' latch.

18 The 10-bit interface address in ABAR is gated to the line address bus at C0 time; then program addressing occurs as explained on B-290. The scanner gates the ICW associated with this interface address into its ICW work register at R1T3 time. The 'gate pre-ABAR to ABAR' pulse causes the line 'fetch buffer' to gate the ICW working registers into their respective ICW
19 input registers at R1M1T0 time. The CSB select bits determine which ICW input register contents are used when the control program executes the appropriate input instructions.

20 When Input X'40' is executed in program level 2, the character control block (CCB) vector address associated with the interface address that caused the interrupt is sent to the general register. Then the interrupt handling program can identify which interface wants service. B-330 contains a summary of all the character control block vector assignments.

21 Input X'40' executed in program level 2 also resets the 'priority register occupied' latch associated with the priority in the 'priority in ABAR' latch. This makes that priority register available to the scanners.

CHARACTER CONTROL BLOCK VECTOR ADDRESS

During a program level 2 interrupt, when the program executes an Input X'40', the interface address that caused the program level 2 interrupt is gated from the ABAR to a general register in the CCU. The relationship between the ABAR positions and the general register is shown at **1**.

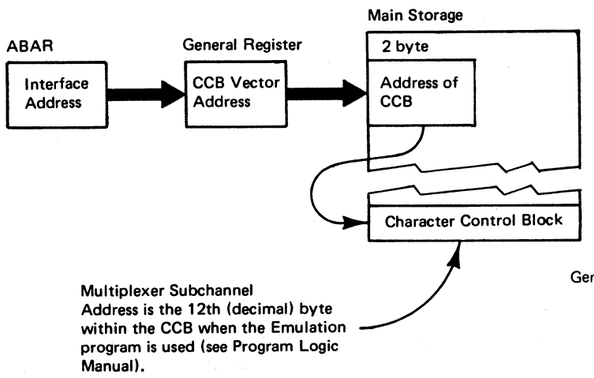
The output of ABAR forms the 'interface address'; for this example it is interface address 020 (hex). The contents of the general register form the character control block (CCB) vector address—in this example, 840 (hex).

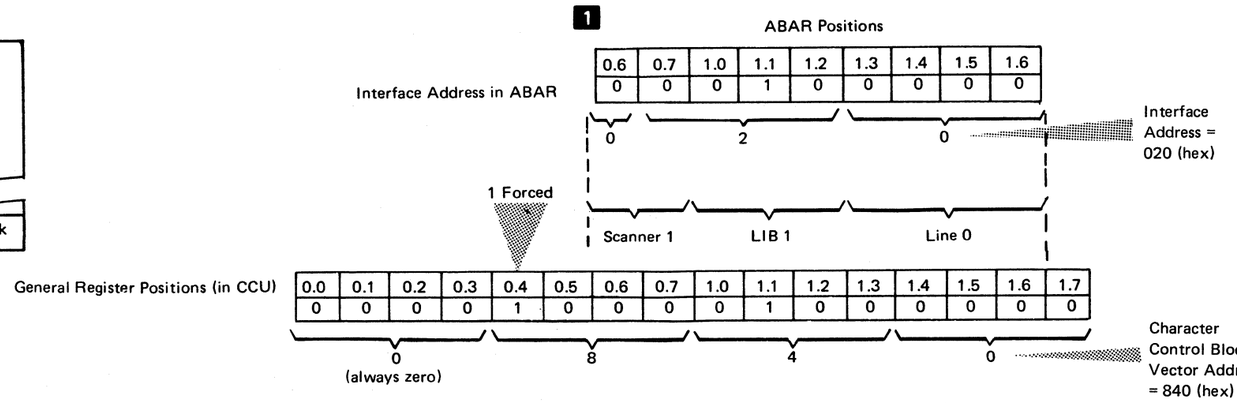
Each interface address has a two-byte permanent storage location that is addressed by its associated character control block vector address. See the accompanying chart for the CCB vector address assigned to each interface address.

The two-byte storage location contains an address pointing to status information concerning that line. This information is used by the routine that handles the program level 2 interrupt. The status information depends upon the program used, such as an emulation program, network control program, or customer-written program. This status information resides in the character control block when the network control program is used.

Type 2 Communication Scanner — LIB Position Interface Address Assignments and CCB Vector Storage Addresses

Frame and LIB Position		INTERFACE ADDRESS ASSIGNMENTS (HEX)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		Character Control Block Vector Storage Addresses (Hex)															
3705-80 LIB position	A	0 2 —	840	842	844	846	848	84A	84C	84E	850	852	854	856	858	85A	85C	85E
	B	0 3 —	860	862	864	866	868	86A	86C	86E	870	872	874	876	878	87A	87C	87E



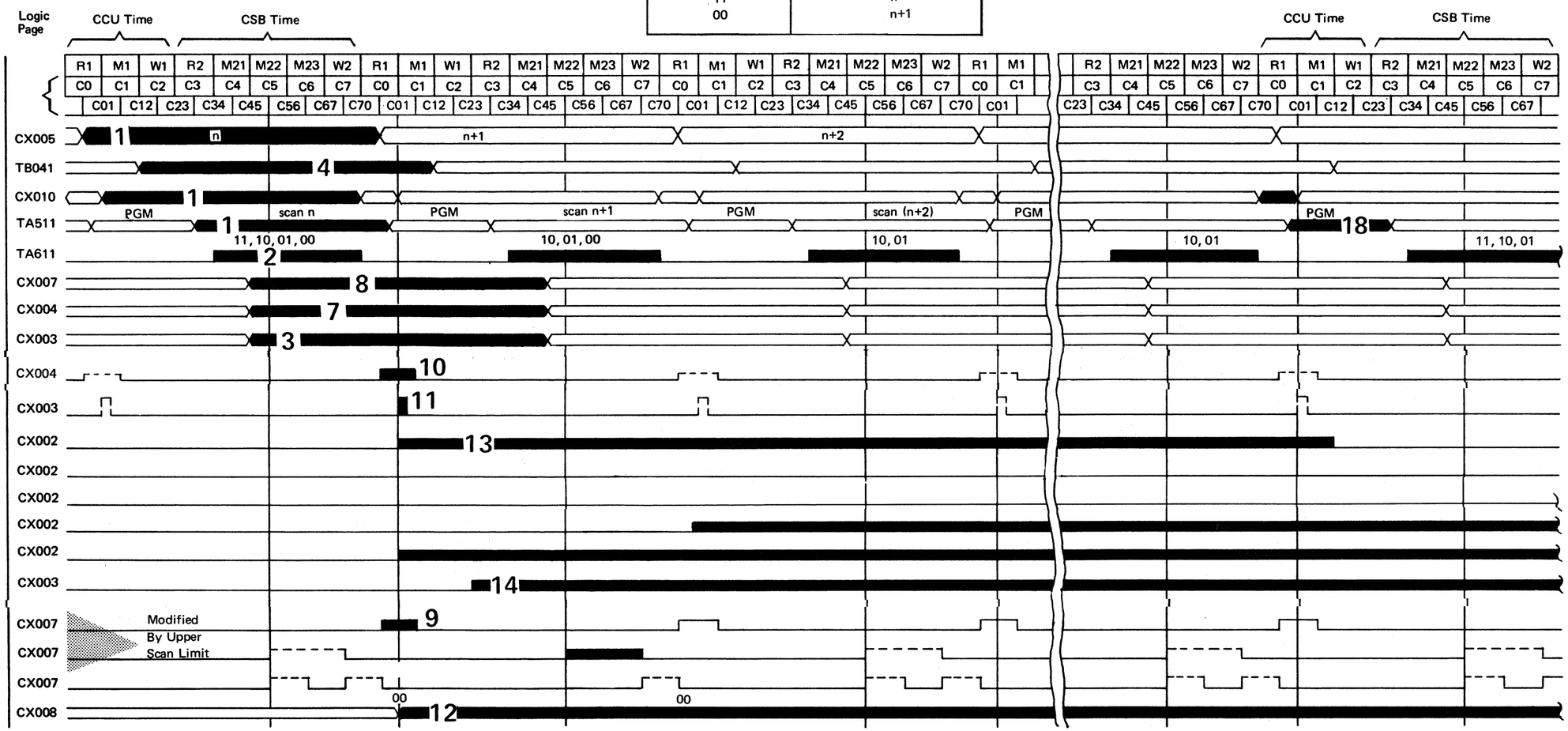


PROGRAM LEVEL 2 INTERRUPT TIMINGS (PART 1 OF 2)

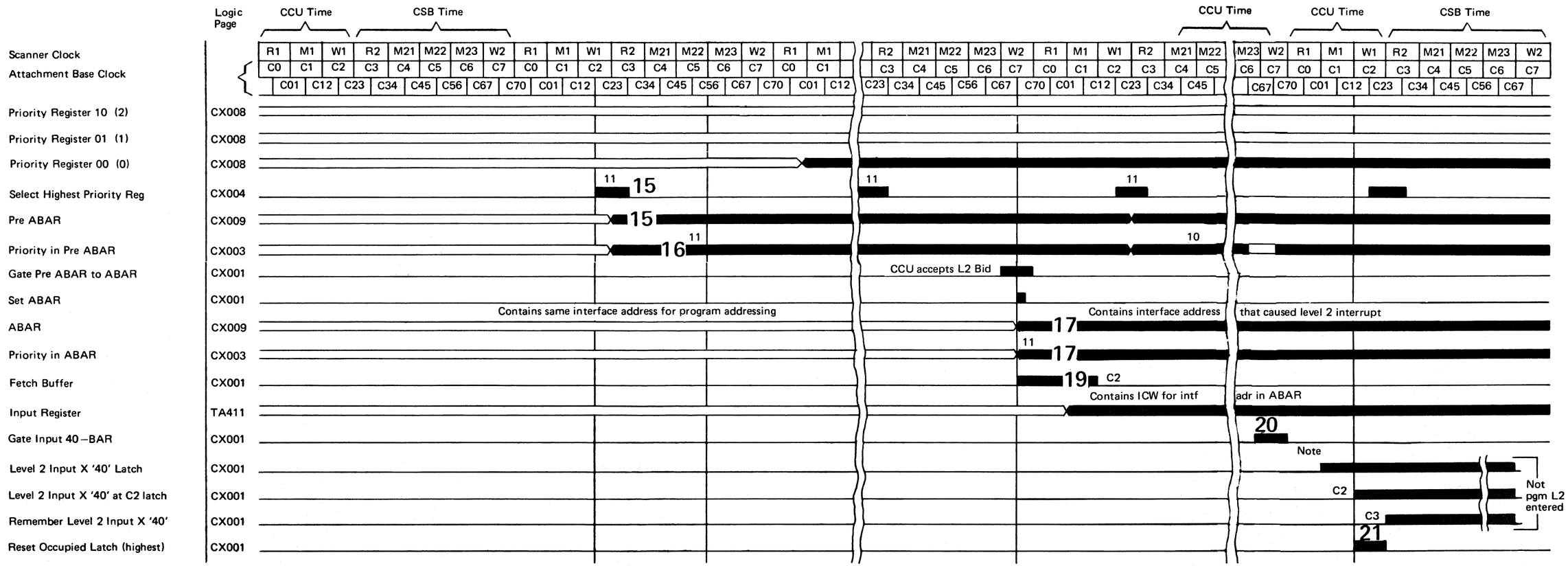
Numbers refer to B–300 and B–310

EXAMPLE ILLUSTRATED

Priority in ICW When Scanned	*Scan Counter Value When 'Interrupt Go' Is Sensed*
11	n
00	n+1

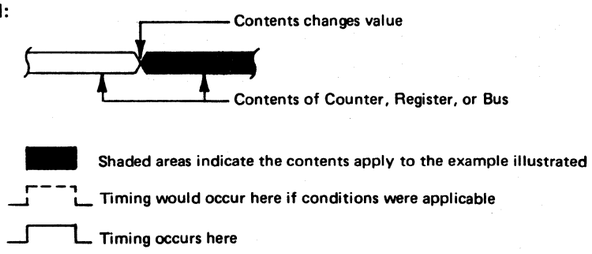


PROGRAM LEVEL 2 INTERRUPT TIMINGS (PART 2 OF 2)



Note: *Gate Input 40 is independent of the attachment base clock—gated by the CCU clock at CD time.*

Legend:



PROGRAM LEVEL 2 INTERRUPT EXAMPLES

EXAMPLE 1: Substitution ctrl reg 1 = 1, Scanner upper scan limit = 11 (16 lines)

	Position	A, B or C	A or D	B or E	C or F	8	4	2	1	Action Performed — comments
1	Scan Counter	1	0	1	0	1	1	1	0	
	Counter Register/Line Address Bus	1	1	0	0	0	0	0	0	Adr substitution—(See B–220) Interface Address 020
	ICW Local Store Address	0	1	0	0	0	0	0	0	Modified by upper scan limit = 11 (See B–230) Selected—LIB A, adr = 0, ICW = 020

Interface address 020 requests level 2 interrupt (priority = 11)

	Position	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	
12	Priority Register 11	0	0	0	1	0	0	0	0	0	Modify counter reg according to accompanying charts 1 and 2.
17	ABAR	0	0	0	1	0	0	0	0	0	ABAR loaded by pgm lev 2 interrupt

Force 1 — 2 Scanner 1 — 3 LIB 1 — (Hex) Line Adr 0 → Interface address = 020 on In Data Bus

	In Data Bus position	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	
20	General Reg. in CCU	1	0	0	0	0	1	0	0	0	0	0	0	Character Control Block Vector

8 4 0 — Address = 840 (See B–330)

EXAMPLE 2: Substitution ctrl reg 1 = 1, Scanner upper scan limit = 01 (8 lines)

	Position	A, B, or C	A or D	B or E	C or F	8	4	2	1	Comment
1	Scan Counter	1	0	1	0	1	1	0	1	
	Counter Register/Line Address Bus	1	0	1	0	1	1	0	1	No adr substitution—(See B–220) Interface Address 03D
	ICW Local Store Address	0	1	0	0	0	1	0	1	Modified by upper scan limit = 01 (See B–230) Selected—LIB A, adr 5, ICW = 025

Interface address 025 requests level 2 interrupt (priority = 10)

	Position	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	
12	Priority Register 10	1	0	0	1	0	0	1	0	1	Modify counter reg according to accompanying charts 1 and 2.
17	ABAR	1	0	0	1	0	0	1	0	1	ABAR loaded by pgm lev 2 interrupt

Force 1 — 2 Scanner 1 — 3 LIB 1 — (Hex) Line Adr 5 → Interface address = 025 on In Data Bus

	In Data Bus position	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	
20	General Reg in CCU	1	0	0	0	0	1	0	0	1	0	1	0	Character Control Block Vector

A 4 A — Address = 84A (See B–330)

Numbers to the left of the examples refer to B–300, B–310 and B–320.

1 UPPER SCAN LIMIT MODIFICATION OF THE COUNTER REGISTER

Upper Scan Limits Bit 0	Upper Scan Limits Bit 1	Counter Register bit positions A, B, or C	A or D	B or E	C or F	8	4	2	1	Priority Register bit positions 1.0	1.1	1.2	1.3	1.4	1.5	1.6	Significance (Note 1)
0	0 (96 lines)	1	1	0	0	X	X	X	X	0	1	0	X	X	X	X	LIB A
		1	0	1	0	X	X	X	X	0	1	1	X	X	X	X	LIB B
		1	0	0	1	X	X	X	X	1	0	0	X	X	X	X	LIB C
		0	1	0	0	X	X	X	X	1	0	1	X	X	X	X	LIB D
		0	0	1	0	X	X	X	X	1	1	0	X	X	X	X	LIB E
		0	0	0	1	X	X	X	X	1	1	1	X	X	X	X	LIB F
1	0 (48 lines)	1	1	0	0	X	X	X	X	0	1	0	X	X	X	X	LIB A
		1	0	1	0	X	X	X	X	0	1	1	X	X	X	X	LIB B
		1	0	0	1	X	X	X	X	1	0	0	X	X	X	X	LIB C
		0	1	0	0	X	X	X	X	0	1	0	X	X	X	X	LIB A
		0	0	1	0	X	X	X	X	0	1	1	X	X	X	X	LIB B
		0	0	0	1	X	X	X	X	1	0	0	X	X	X	X	LIB C
1	1 (16 lines)	1	1	0	0	X	X	X	X	0	1	0	X	X	X	X	LIB A
		1	0	1	0	X	X	X	X	0	1	0	X	X	X	X	LIB A
		1	0	0	1	X	X	X	X	0	1	0	X	X	X	X	LIB A
		0	1	0	0	X	X	X	X	0	1	0	X	X	X	X	LIB A
		0	0	1	0	X	X	X	X	0	1	0	X	X	X	X	LIB A
		0	0	0	1	X	X	X	X	0	1	0	X	X	X	X	LIB A
0	1 (8 lines)	1	1	0	0	0	X	X	0	0	1	0	0	X	X	0	LIB A even lines
		1	0	1	0	1	X	X	0	0	1	0	0	X	X	1	LIB A odd lines
		1	0	0	1	1	X	X	1	0	1	0	0	X	X	1	LIB A odd lines
		0	1	0	0	0	X	X	0	0	1	0	0	X	X	0	LIB A even lines
		0	0	1	0	0	X	X	1	0	1	0	0	X	X	0	LIB A even lines
		0	0	0	1	1	X	X	1	0	1	0	0	X	X	1	LIB A odd lines

2 SCANNER CODE SET IN PRIORITY REGISTERS

	Pri Reg bit pos.	
Scanner	0.6	0.7
1	0	0

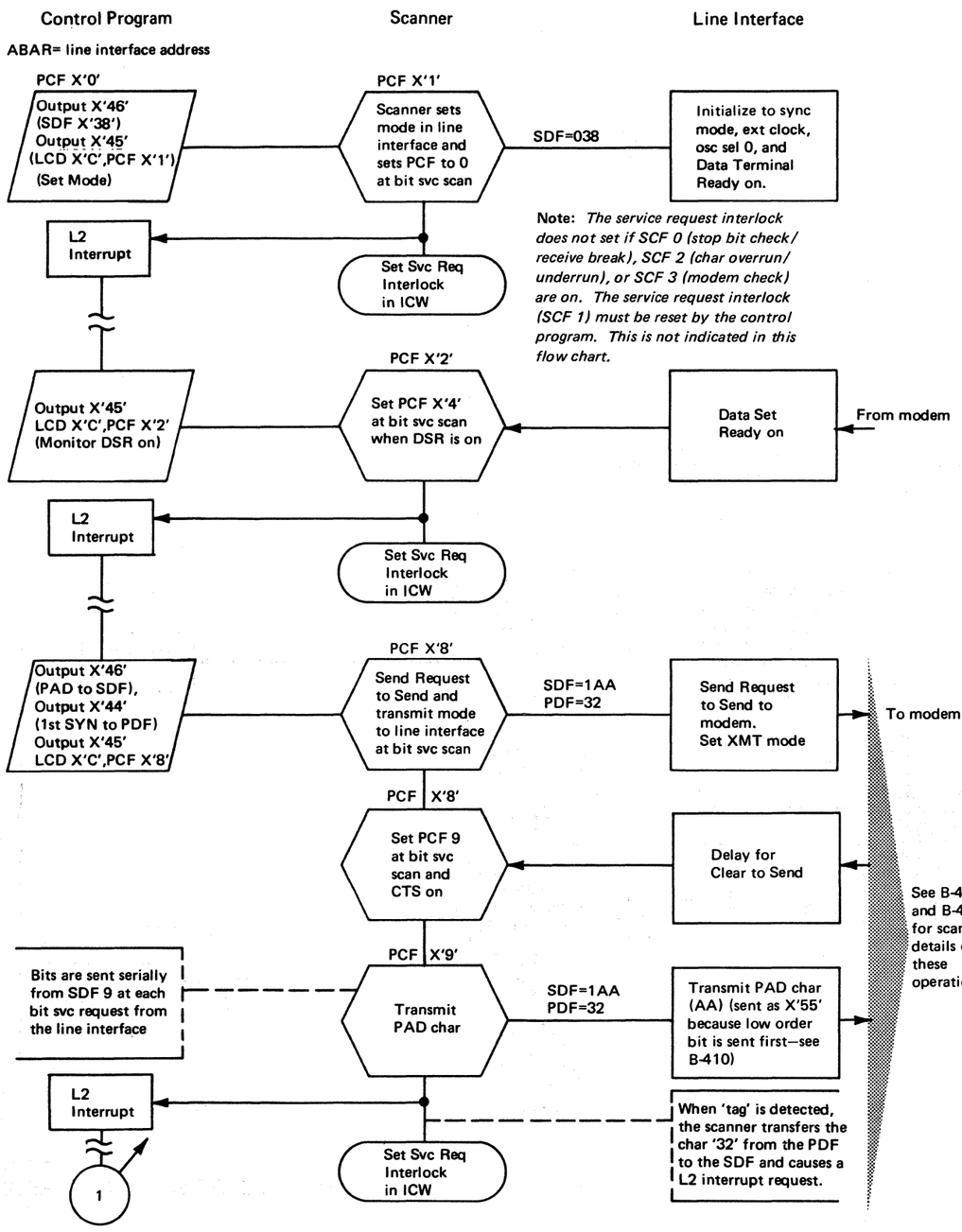
3 LIB IDENTIFICATION

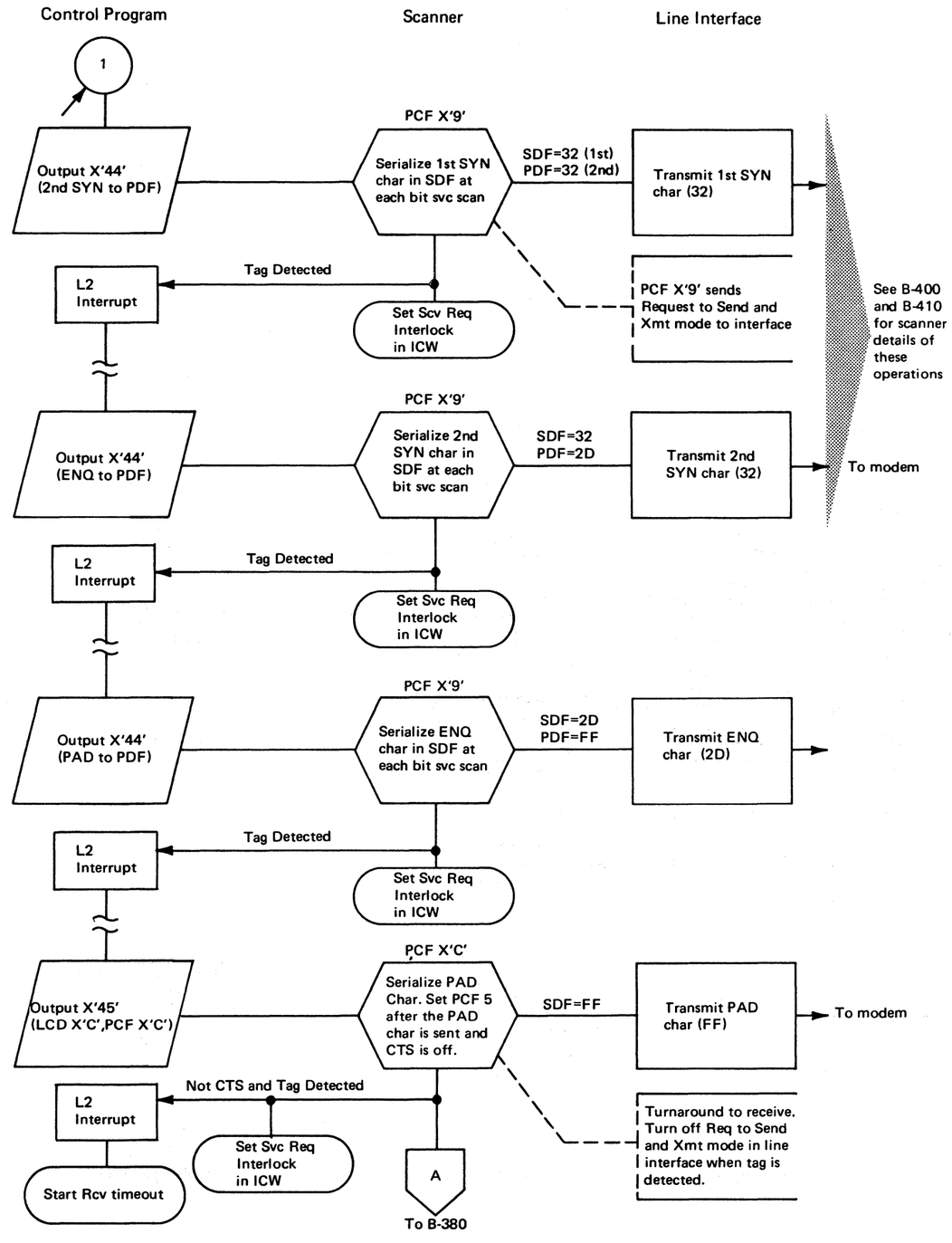
ABAR Positions 1.0	1.1	1.2	Significance of ABAR content (Note 1)
0	1	0	LIB A
0	1	1	LIB B
1	0	0	C
1	0	1	D
1	1	0	E
1	1	1	F

Note 1: *A and B select respective LIBs. C, D, E, and F do not select LIBs or ICWs.*

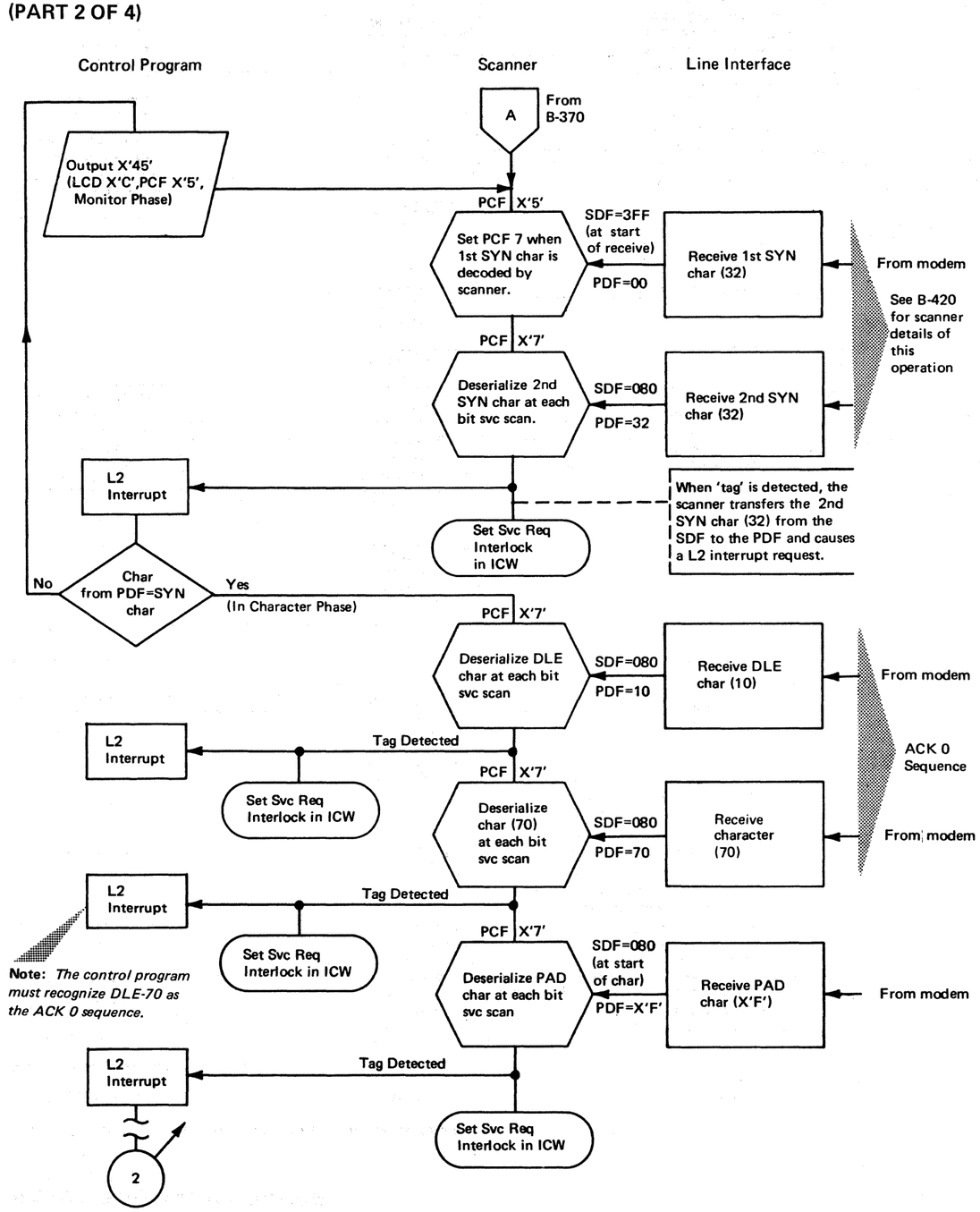
BI-SYNC TERMINAL OPERATION (PART 1 OF 4)

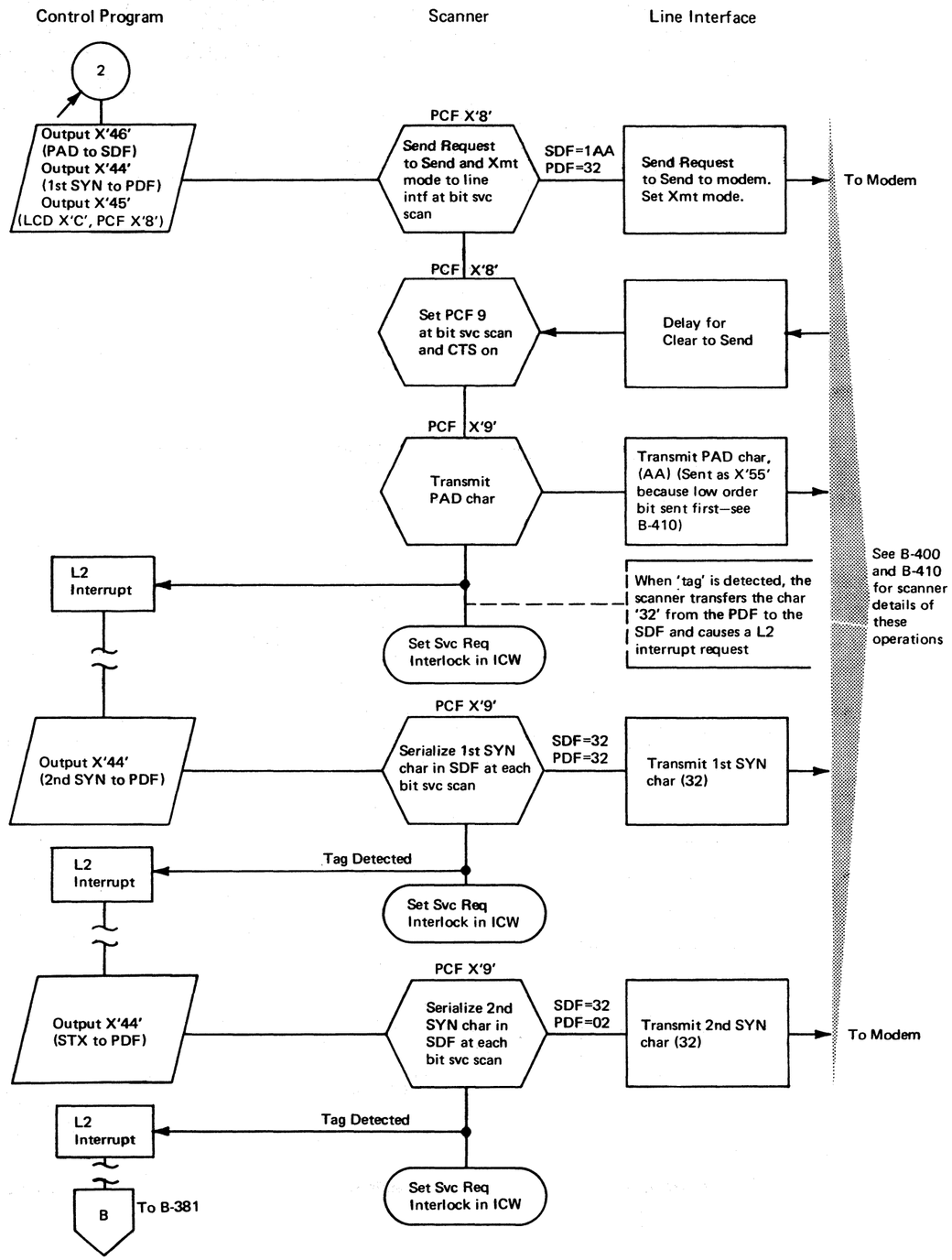
Note: *This operation uses EBCDIC code over a half duplex switched line.*



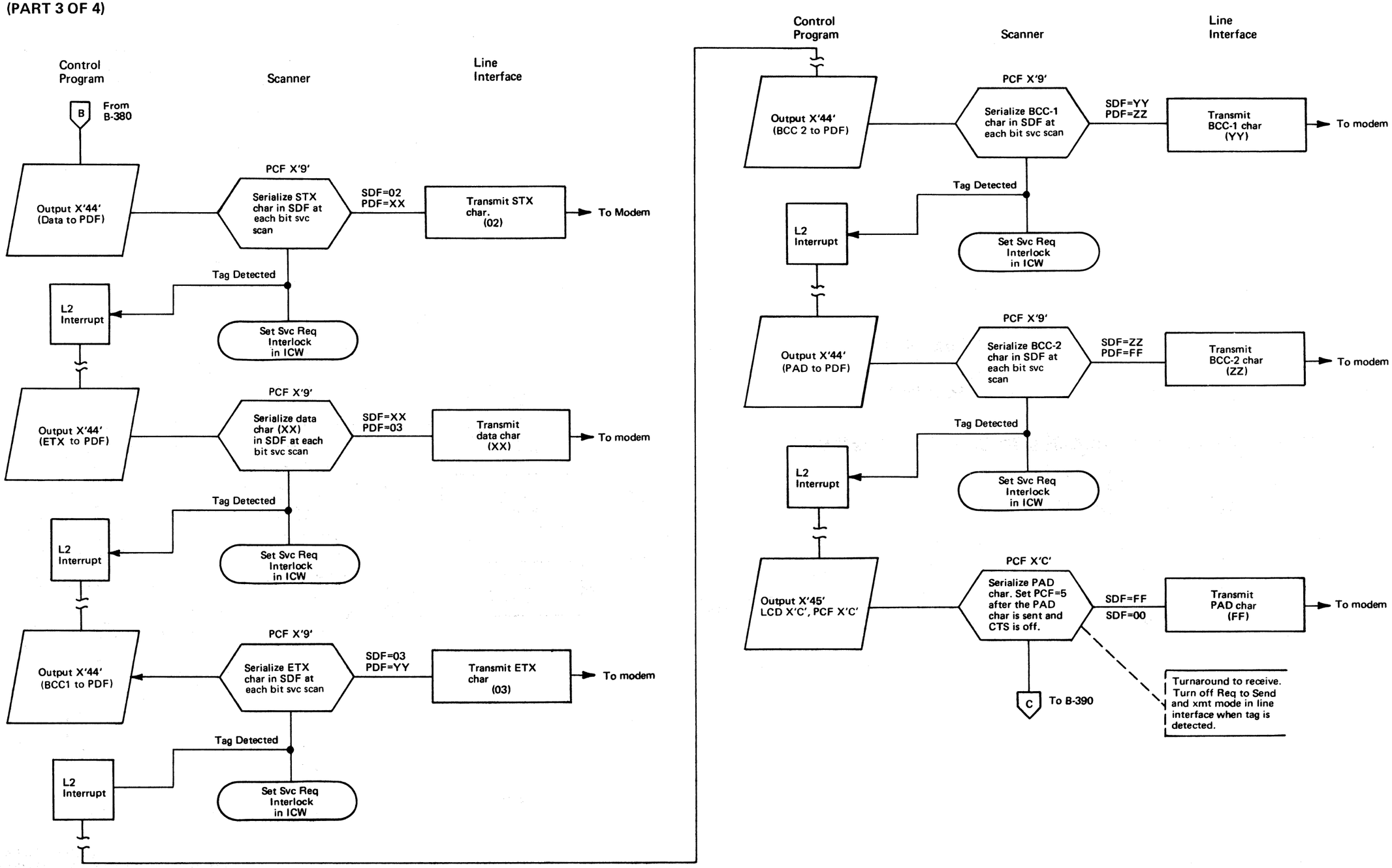


BI-SYNC TERMINAL OPERATION (PART 2 OF 4)

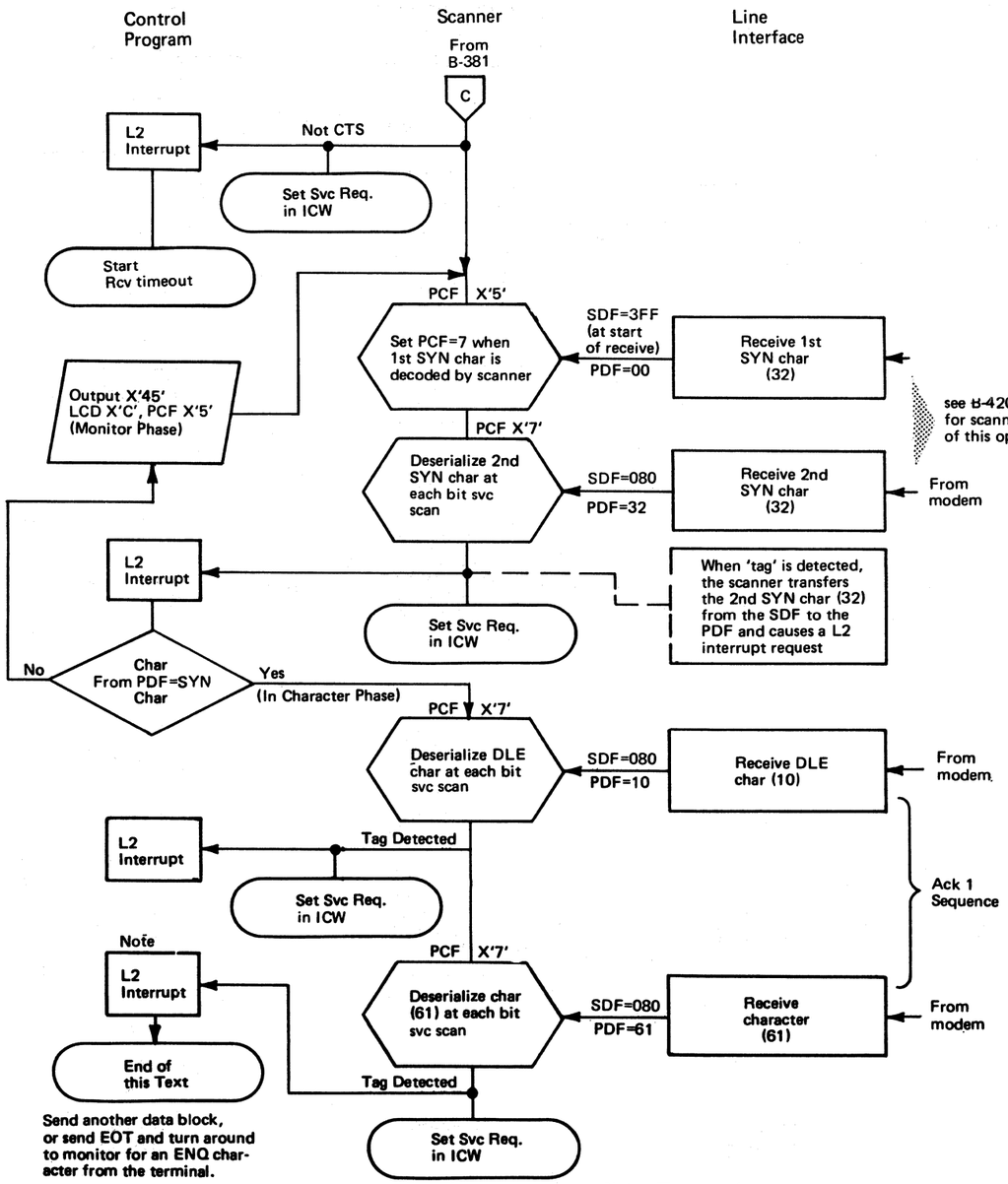




BI-SYNC TERMINAL OPERATION (PART 3 OF 4)

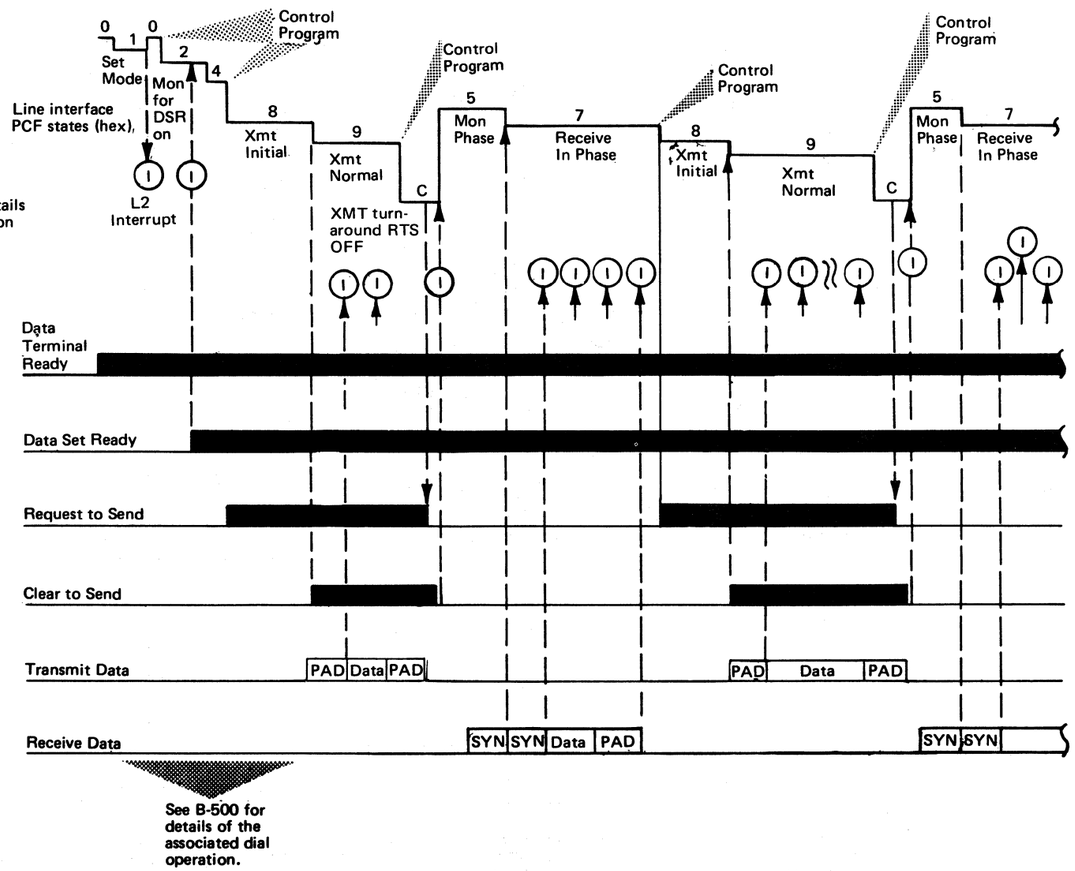


BI-SYNC TERMINAL OPERATION (PART 4 OF 4)



Note: *The control program must recognize DLE-61 as the ACK 1 sequence.*

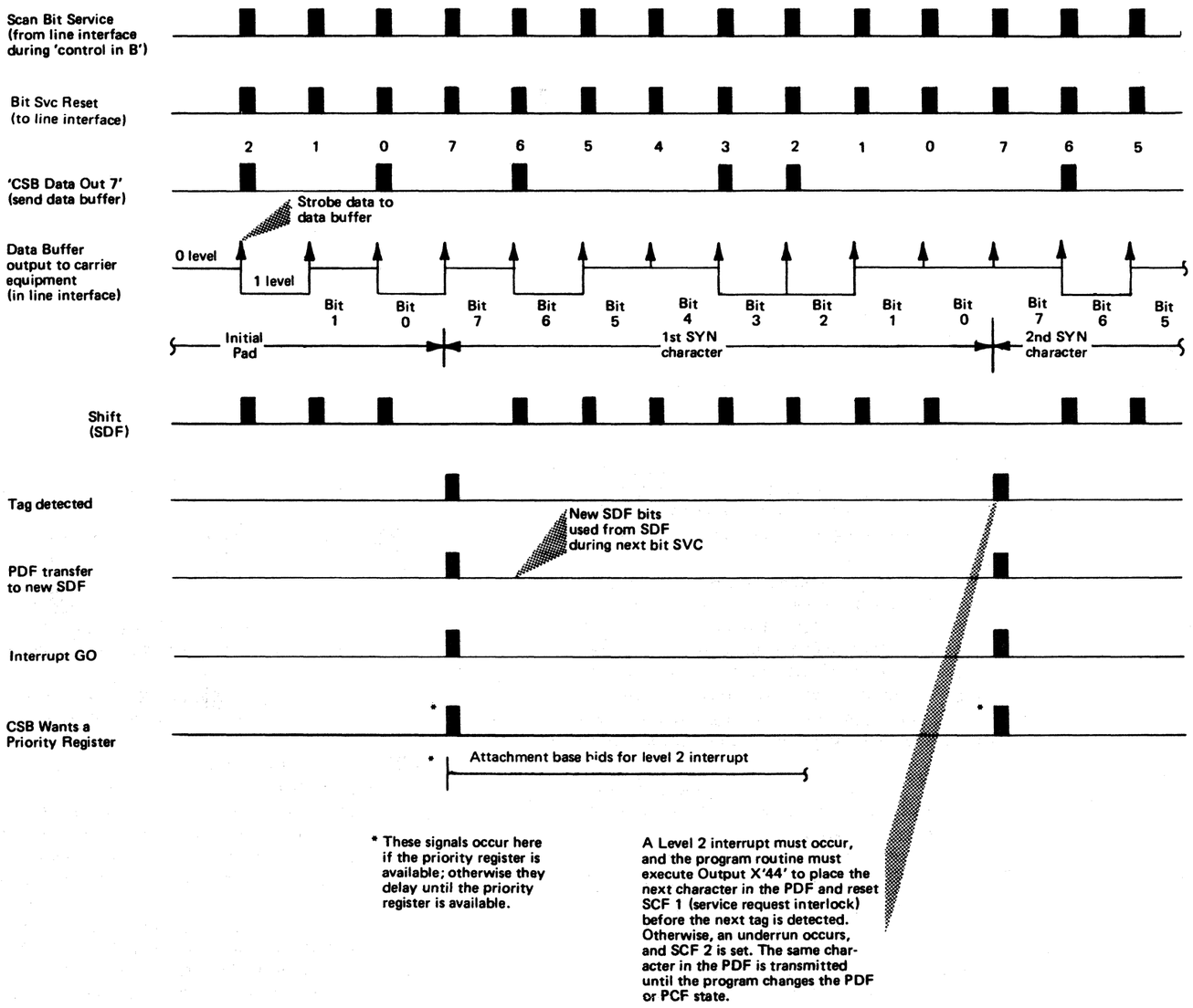
Sequence of Operation For a Half-Duplex Switched Line



See B-500 for details of the associated dial operation.

BSC TRANSMIT SEQUENCE

See B-410 for details associated with this sequence.



* These signals occur here if the priority register is available; otherwise they delay until the priority register is available.

A Level 2 interrupt must occur, and the program routine must execute Output X'44' to place the next character in the PDF and reset SCF 1 (service request interlock) before the next tag is detected. Otherwise, an underrun occurs, and SCF 2 is set. The same character in the PDF is transmitted until the program changes the PDF or PCF state.

BSC TRANSMIT DETAILS

Note: *This example uses LCD = C (EBCDIC code).*

The scanner holds 'CSB data out 7' (send data buffer) at the mark level while CTS (clear to send) is off (TA311). 1 While CTS is off, 'SDF direct' regenerates the data in the SDF and 'shift' is inhibited (TA211).

When CTS turns on, the scanner sets PCF=9 (TA831). 2 State 9 becomes the active PCF state at the next 'bit service request' for that interface. The scanner then:

- Removes the mark hold and sends the bit in SDF 9 to the LIB at 'bit service request' time (TA311). 3
- Shifts SDF 0-9 under control of 'bit service request'. 4
  During this shift, the scanner:
  – Inhibits 'SDF direct'.
  – Places a zero in SDF 0. 5

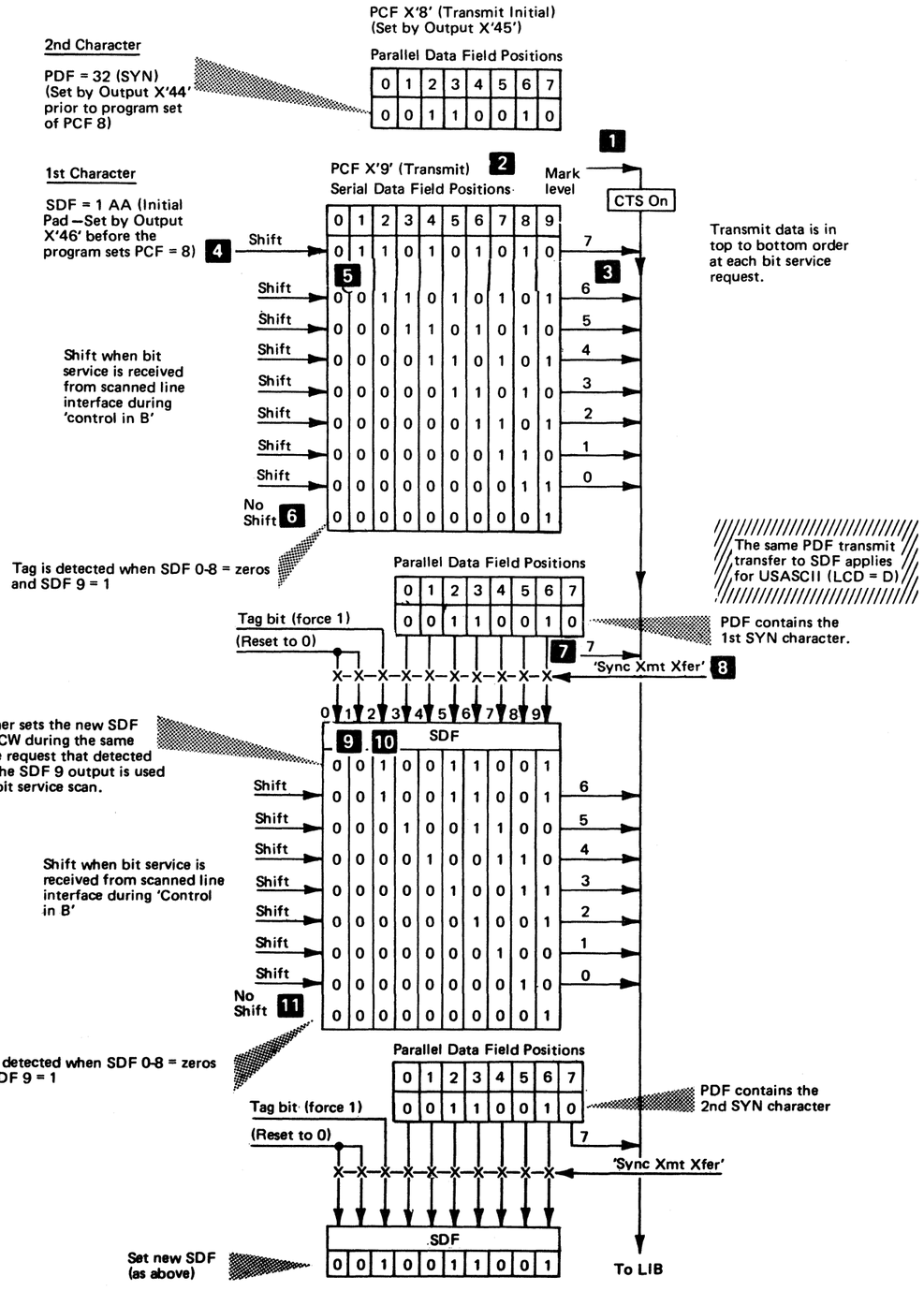
The scanner detects the transmit tag during 'gated bit service' when SDF 0-8 contains all zeros and SDF 9 is 1 (TA261). 6

The scanner:

- Sends the next bit from PDF 7 instead of SDF 9. 7
- Brings up 'sync xmt xfer' that gates PDF 0-6 contents to the SDF (TA231). 8 During this PDF to SDF transfer, the scanner:
  – Sets SDF 2 for the transmit tag. 9 The LCD state determines that this bit is set into SDF 2. This applies to LCD = D (USASCII) also.
  – Forces SDF bits 0-1 to zeros 10 (also under control of LCD C or D).
- Inhibits 'shift' to prevent shifting the new character in the SDF (TA211).
- Brings up 'interrupt go' (TA831) that:
  – Sets SCF 1 (service request interlock) if SCF 0, SCF 2, or SCF 3 are not set (TA121).
  – Causes a L2 interrupt request (TA831).
  – Brings up 'fetch buffer' that gates the ICW content to the input register when the CCU accepts the L2 interrupt (CX001).

The control program executes an Output X'44' to place the next character in the PDF, and to reset SCF 1 (service request interlock). The scanner detects transmit tag (SDF 0-8 = zeros and SDF 9 = 1) for each character sent to the LIB. 11 In addition to the action previously described, the scanner checks to ensure that SCF 1 is off. If on, an underrun has occurred and the scanner sets SCF 2 (overrun/underrun), and resets SCF 1 (TA121).

The scanner sends characters to the LIB using the above sequence until the control program changes the PCF state to C (transmit turnaround-RTS off), or D (transmit turnaround-RTS on).



BSC RECEIVE DETAILS

Note: *Example uses LCD = C (EBCDIC code).*

The scanner shifts the received data through the SDF (serial data field) at each bit service request looking for the sync configuration. Once the scanner recognizes the sync configuration (TA841), **1** the scanner:

- Sets PCF = 7 (TA811). **2**
- Inhibits 'gate direct' that prevents regenerating the old PCF 0-3 bits (TA831).
- Generates 'initiate sync 8 rcv tag' (TA841) that:
  - Sets the tag bit in the 'new SDF 2' (TA261) **3**
  - Inhibits 'shift' (TA211). **4**

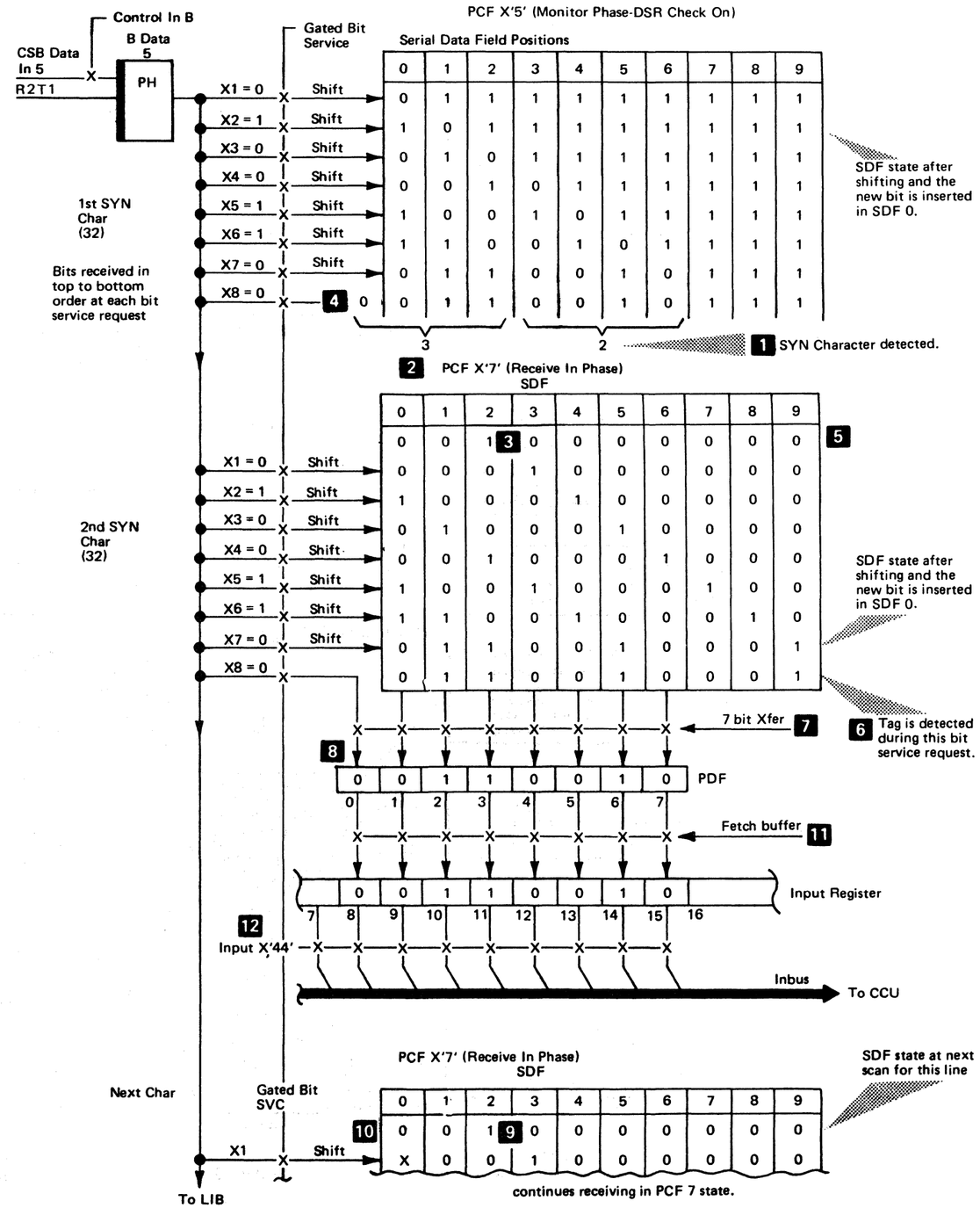
    With 'gate direct' and 'shift' inhibited, the scanner places zeros in new SDF 0-1 and SDF 3-9 positions. **5**

The scanner shifts the received data through the SDF at each bit service request until the tag bit is detected in SDF 9 (TA261) **6** . When the receive tag is detected, the scanner:

- Initiates 'rcv xfer' (TA711) that:
  - Causes '7 bit xfer' of the SDF contents to the new PDF (TA711) **7** .
  - Gates the new bit to PDF 0 **8** .
  - Inhibits 'PDF direct' (0-7). This prevents the regeneration of the old PDF (TA211).
  - Sets a tag bit in new SDF 2 (TA261) **9** .
  - Inhibits 'shift' and 'SDF direct' (TA211). This resets SDF 0-1 and SDF 3-9 by preventing the regeneration of the old SDF **10** .
  - Checks for overrun (TA121). If SCF 1 (service request interlock) is on, an overrun has occurred. The scanner sets SCF 2 (overrun/underrun), and resets SCF 1.
  - Brings up 'interrupt go' (TA831) that:
    1. Causes a L2 interrupt request (CX003).
    2. Brings up 'fetch buffer' when the CCU accepts the L2 interrupt (CX001) **11** .

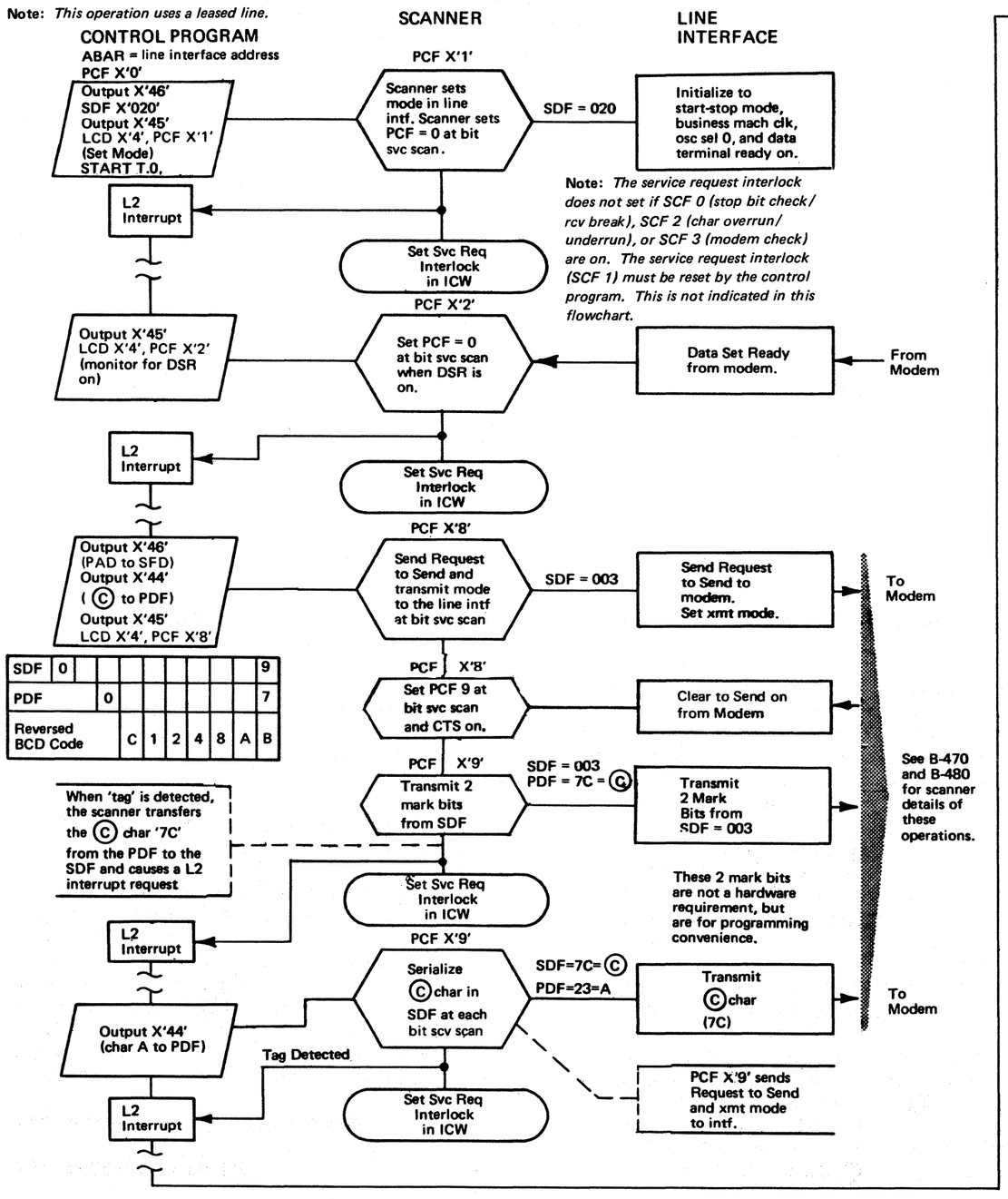
The control program executes Input X'44' to obtain the receive character **12** . If the second character is the SYN character while in PCF X'7', character phase has been established and the program keeps the PCF in state 7. If the second character is not the SYN character, the program sets PCF = 5 (for this example) to resume monitoring for phase.

The same sequence occurs for each character received.

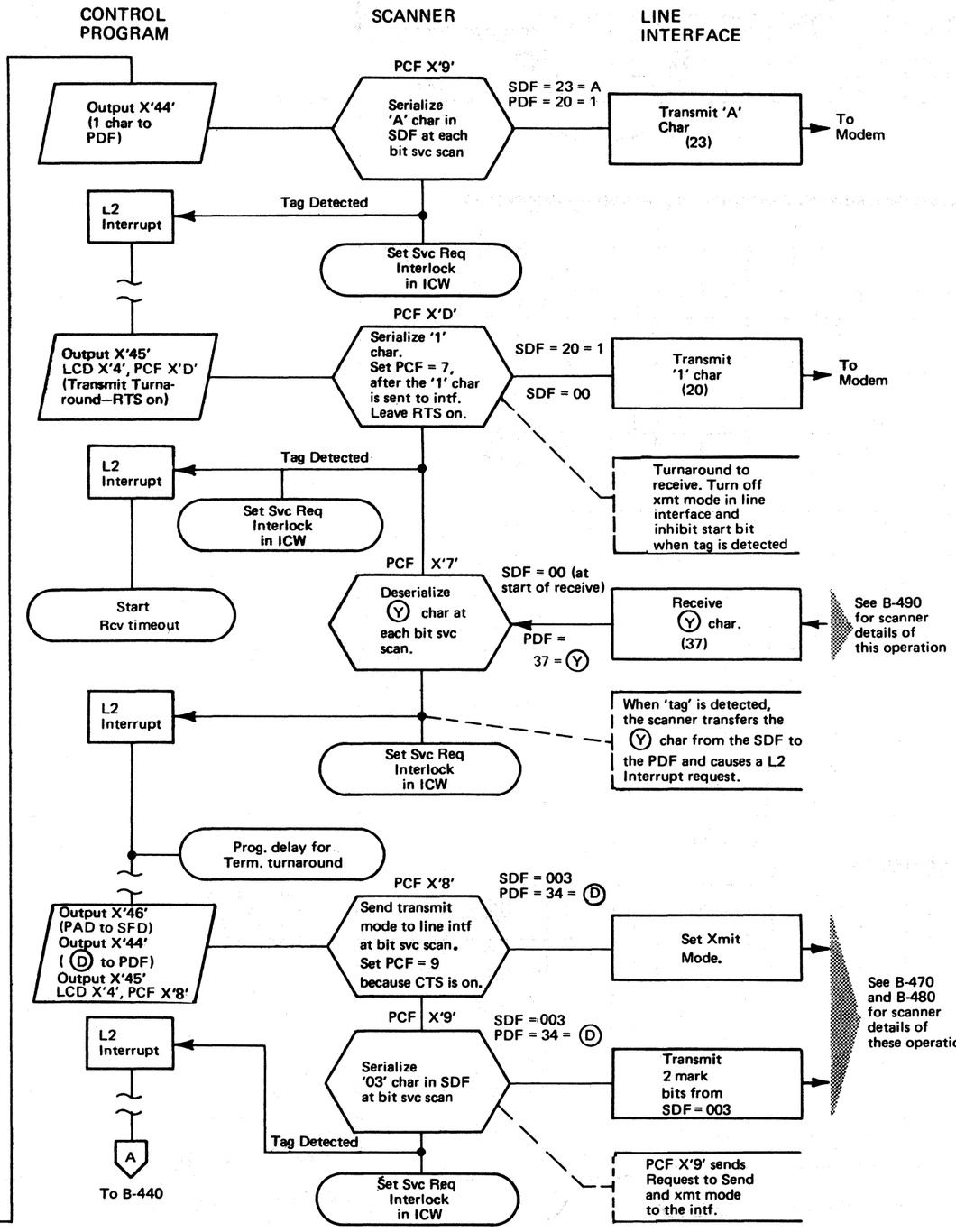


1050 TYPE TERMINAL OPERATION (PART 1 OF 2)

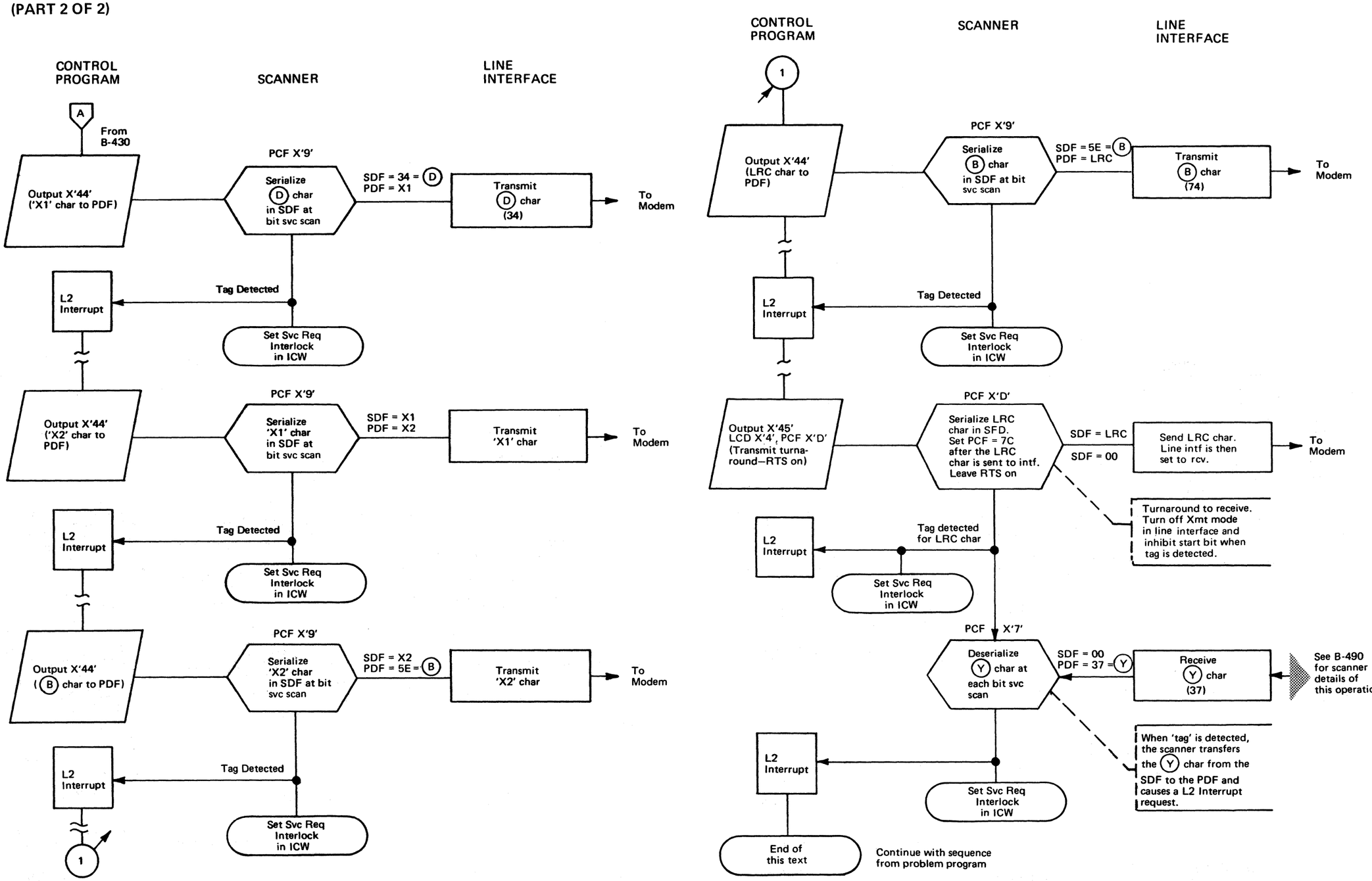
Note: *This operation uses a leased line.*



SDF	0							9
PDF	0							7
Reversed BCD Code	C	1	2	4	8	A	B	

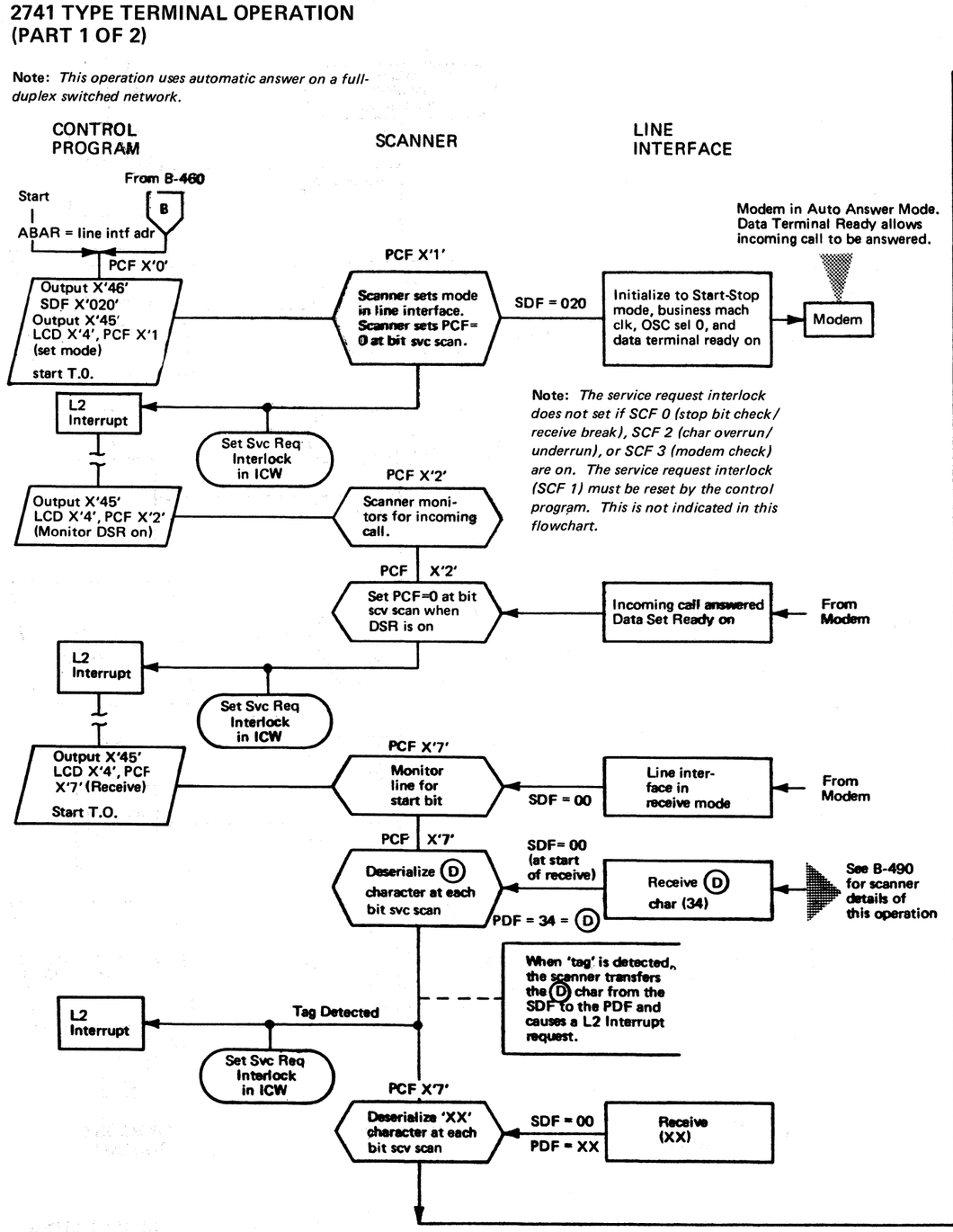


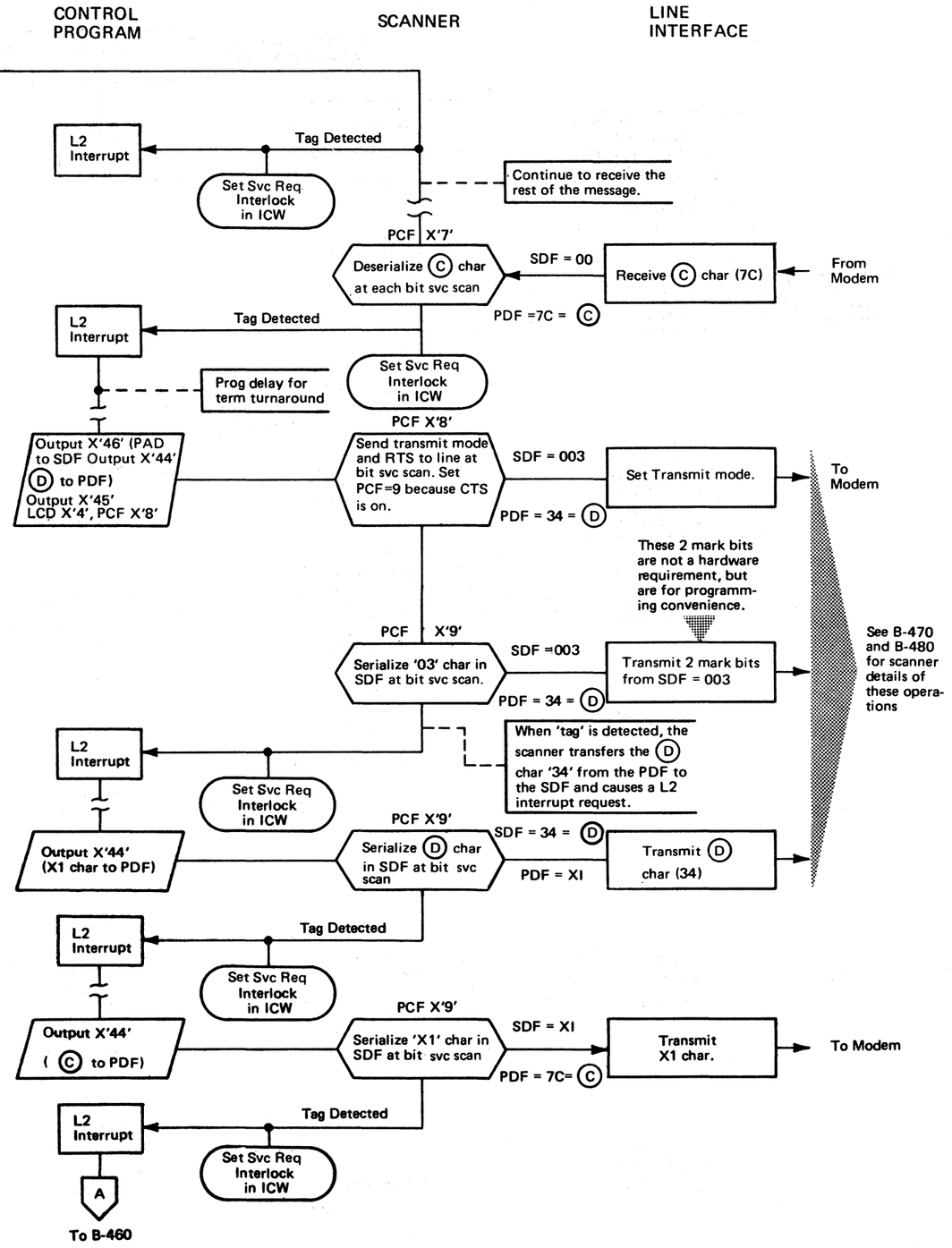
1050 TYPE TERMINAL OPERATION (PART 2 OF 2)



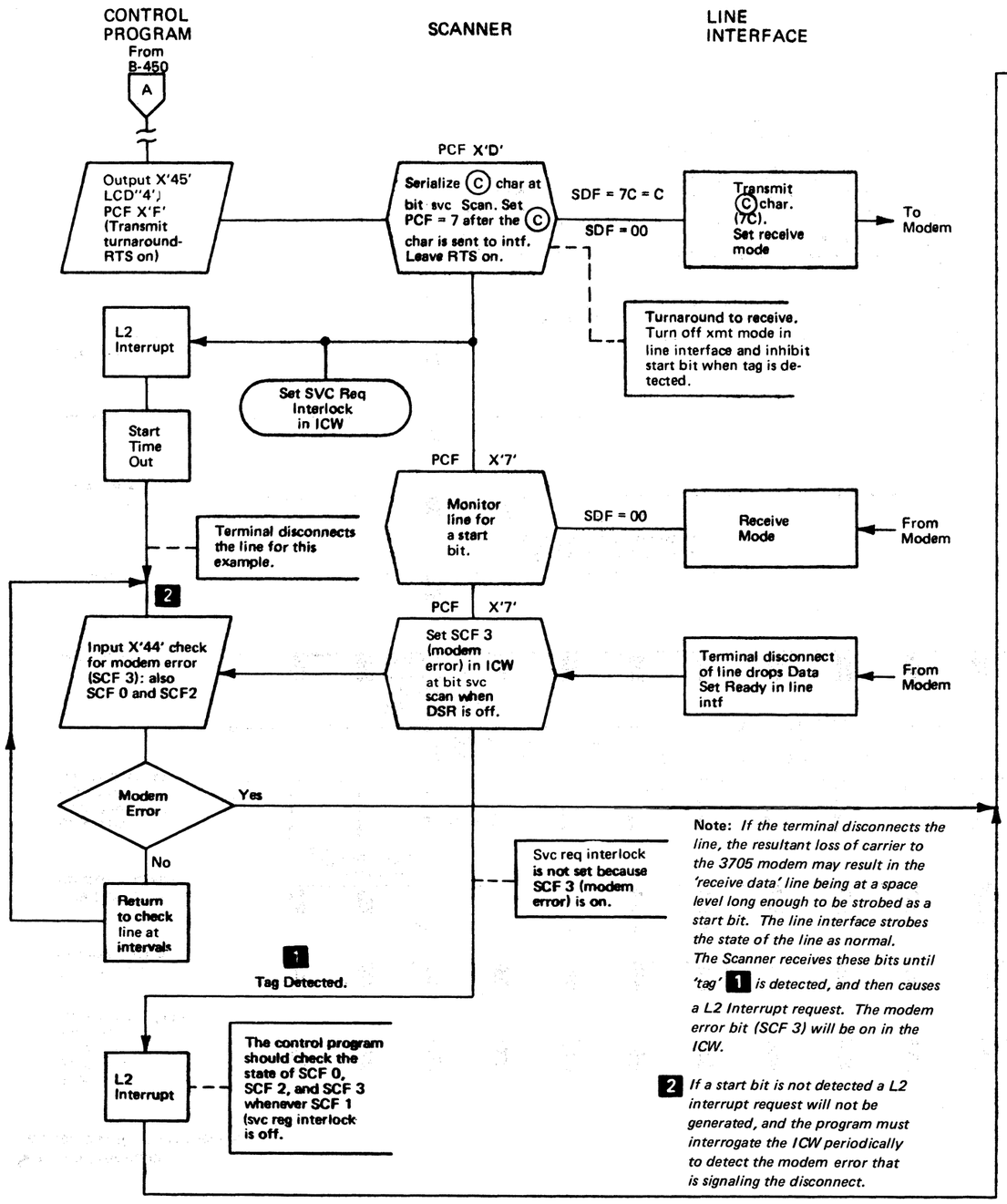
2741 TYPE TERMINAL OPERATION (PART 1 OF 2)

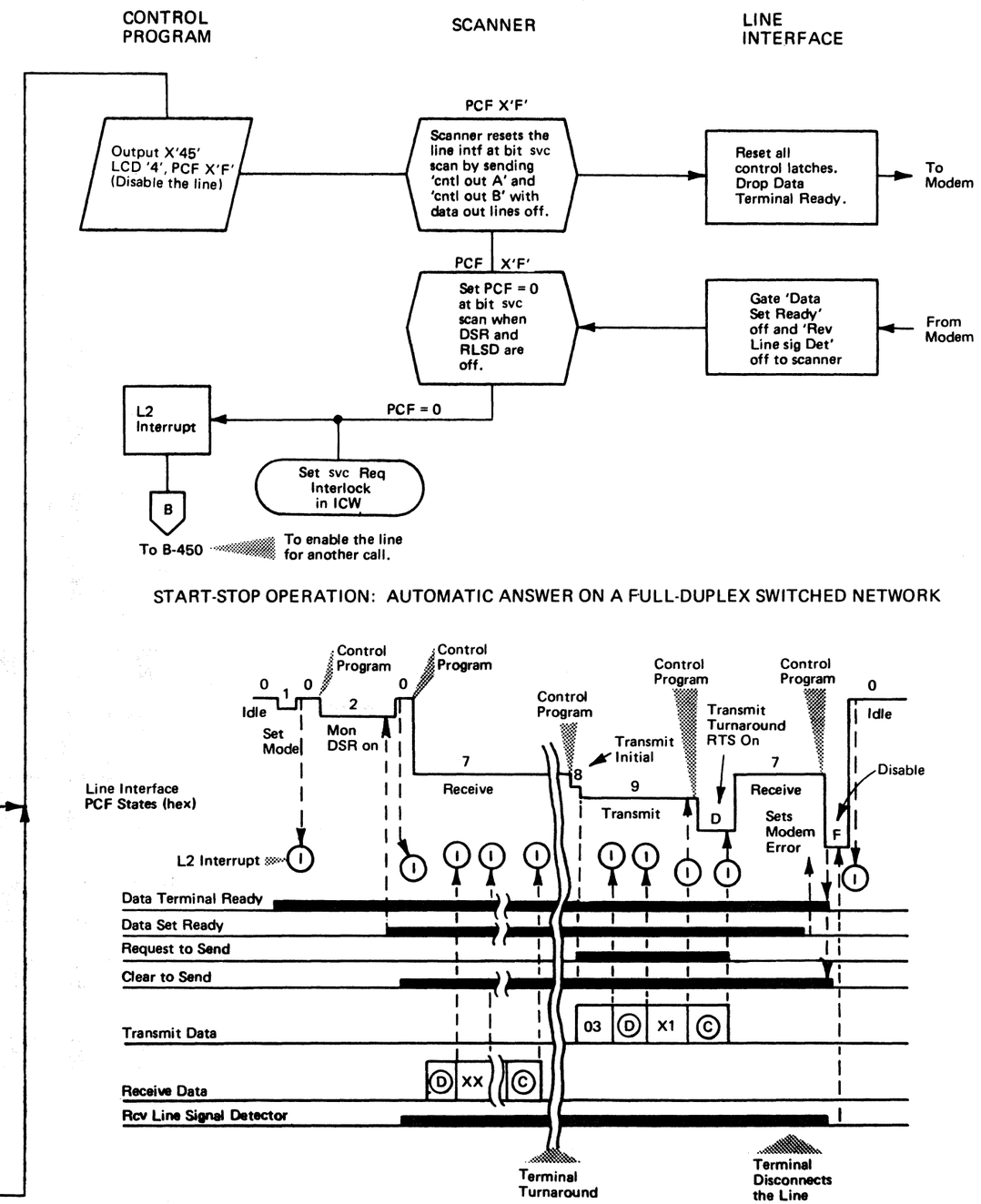
Note: *This operation uses automatic answer on a full-duplex switched network.*





2741 TYPE TERMINAL OPERATION (PART 2 OF 2)

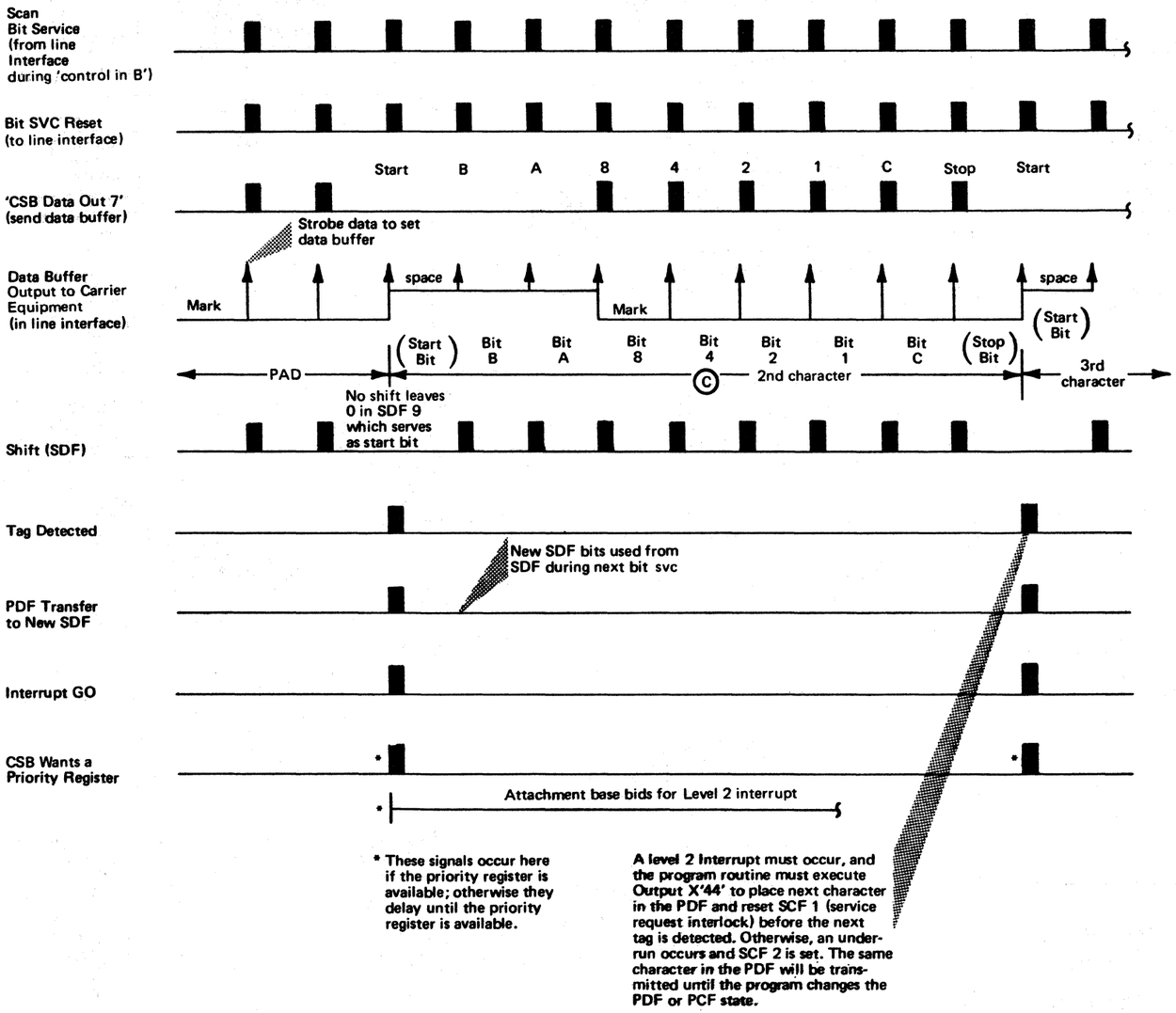




START-STOP OPERATION: AUTOMATIC ANSWER ON A FULL-DUPLEX SWITCHED NETWORK

START-STOP TRANSMIT SEQUENCE

See B-480 for details associated with this sequence.



* These signals occur here if the priority register is available; otherwise they delay until the priority register is available.

A level 2 interrupt must occur, and the program routine must execute Output X'44' to place next character in the PDF and reset SCF 1 (service request interlock) before the next tag is detected. Otherwise, an underrun occurs and SCF 2 is set. The same character in the PDF will be transmitted until the program changes the PDF or PCF state.

START-STOP TRANSMIT DETAILS

This example uses LCD = 4 (start-stop 9/7—7 data bits, 1 start bit, and 1 stop bit).

The scanner holds 'CSB data out 7' (send data buffer) at the mark level while CTS (clear to send) is off (TA311). **1** While CTS is off, 'SDF direct' regenerates the data in the SDF and 'shift' is inhibited (TA211).

When CTS turns on, the scanner sets PCF = 9 (TA831). **2** State 9 becomes the active PCF state at the next bit service request for that interface address. The scanner then:

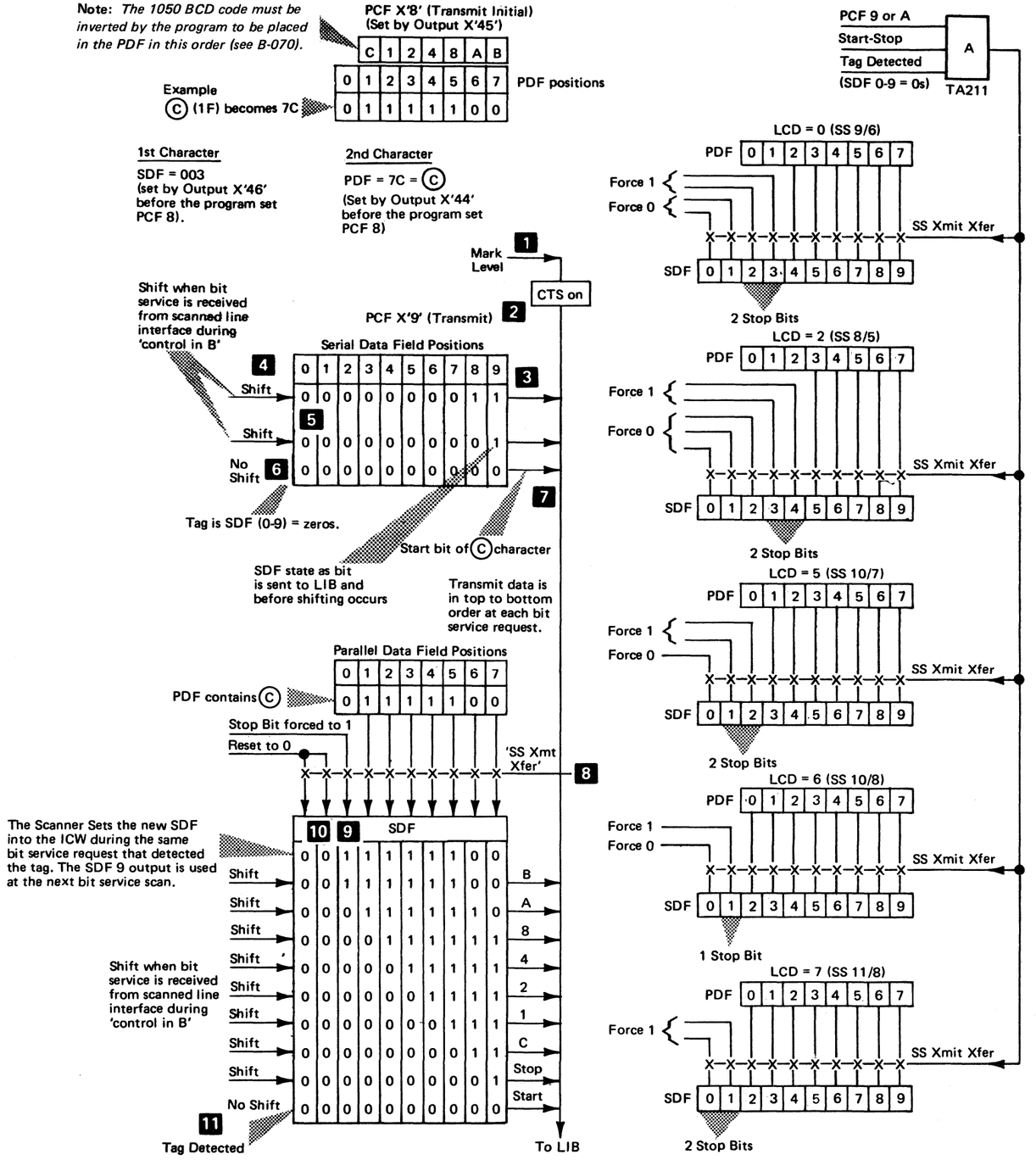
- Removes the mark hold and sends the bit in SDF 9 to the LIB at 'bit service request' time (TA311). **3**
- Shifts SDF 0-9 under control of 'bit service request'. **4** During this shift, the scanner:
  - Inhibits 'SDF direct'.
  - Places a zero in SDF 0. **5**

The scanner detects the transmit tag during 'gated bit service' when SDF 0-9 contains all zeros (TA261). **6** The scanner:

- Checks the 'modem receive space' line during 'control in C' for an active level. If the line is active, the scanner sets SCF 0 (receive break). SCF 0 on prevents setting SCF 1 (service request interlock) (TA121). This check occurs for every character transmitted.
- Sends the start bit for the (C) to the LIB. **7**
- Brings up "SS xmt xfer' that gates the PDF contents to the SDF (TA231). **8** During this PDF to SDF transfer, the scanner:
  - Sets SDF 2 for the transmit tag (also supplies the mark for the stop bit). The LCD state determines where and how many stop bits are set in the SDF (see the accompanying diagrams). **9**
  - Forces SDF 0-1 to zero (also under control of the LCD state). **10**
- Inhibits 'shift' to prevent shifting the new character in the SDF (TA211).
- Brings up 'interrupt go' (TA831) that:
  - Sets SCF 1 (service request interlock) if SCF 0, SCF 2, or SCF 3 are not set (TA121).
  - Causes a L2 interrupt request (TA831).
  - Brings up 'fetch buffer' that gates the ICW content to the input register when the CCU accepts the L2 interrupt (CX001).

The control program executes an Output X'44' to place the next character in the PDF, and to reset SCF 1 (service request interlock). The scanner detects transmit tag (SDF 0-9 = zeros) for each character sent to the LIB. **11** In addition to the action previously described, the scanner checks to ensure that SCF 1 is off. If on, an underrun has occurred and the scanner sets SCF 2 (overrun/underrun), and resets SCF 1 (TA121).

The scanner sends characters to the LIB using the above sequence until the control program changes the PCF state to (1) B (prepare to turn), (2) C (transmit turnaround-RTS off), or (3) D (transmit turnaround-RTS on)—assuming normal operation.



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START-STOP RECEIVE DETAILS

Note: *Example uses LCD = 4 (start-stop 9/7–7 data bits, 1 start bit, and 1 stop bit).*

The scanner monitors the received data for a start bit (space) at bit service request time when the PCF state is 'receive' and the SDF is empty. The scanner inhibits 'shift' until the start bit is detected. At this time, the scanner inserts a tag bit in SDF 2 **1** .

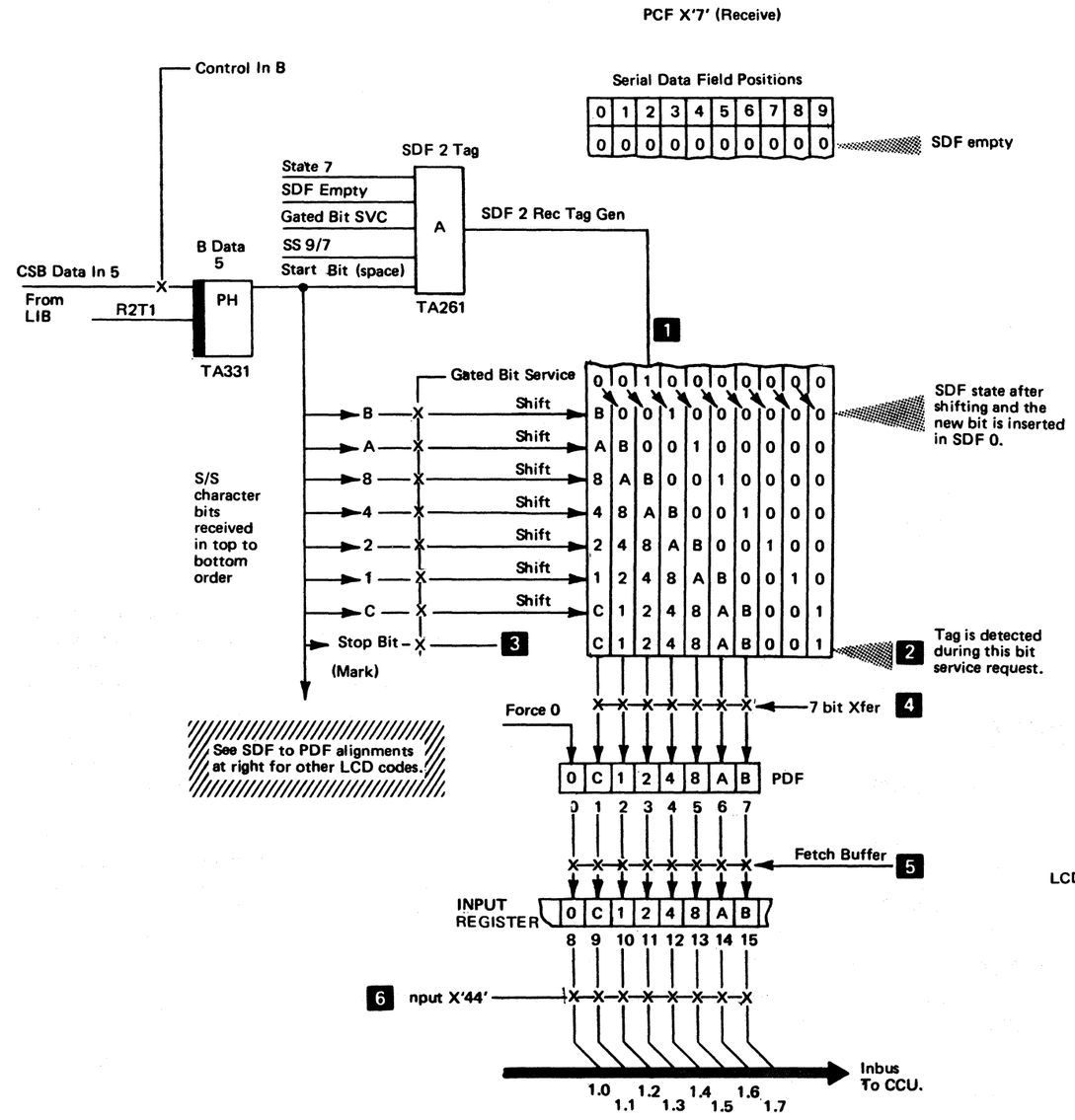
The scanner detects tag when SDF 9 = 1 at bit service scan **2** .

When tag is detected, the scanner:

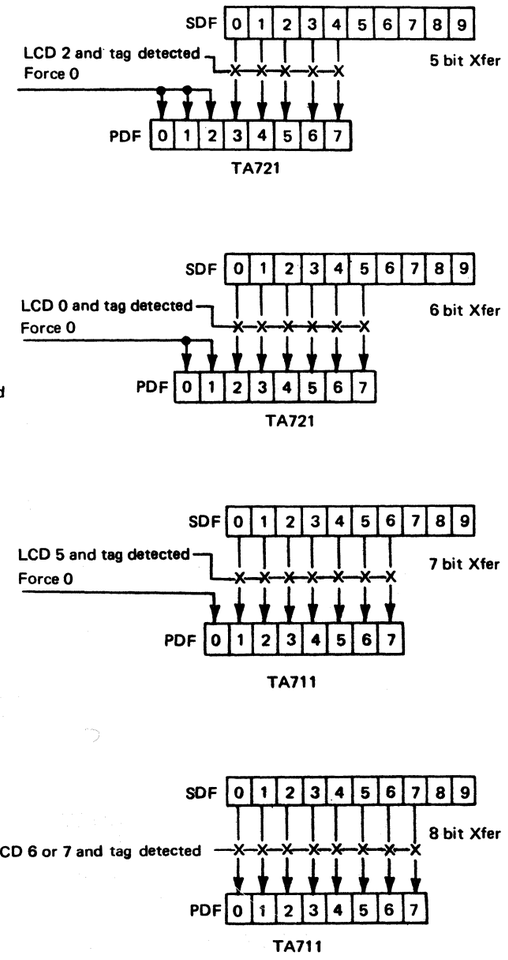
- Inhibits shift (TA211) **3** .
- Checks the stop bit in the B data 5 position for a mark level (TA121).
  - If stop bit is at a space level, the scanner sets SCF 0 to 1 (stop bit error).
- Checks for overrun (TA121).
  - If SCF 1 (service request interlock) is on, the scanner sets SCF 2 (overrun), and resets SCF 1.
- Generates 'receive transfer' that:
  - Causes '7 bit xfer' of SDF contents to the PDF (TA711) **4** .
  - Inhibits 'PDF direct' (0-7). This forces PDF 0 to zero, and inhibits the regeneration of the old PDF (TA731).
- Brings up 'interrupt go'. This causes:
  - A L2 interrupt request (TA831).
  - 'Fetch buffer' that gates the ICW content to the input register (CX001) **5** .

The control program executes Input X'44' to obtain ICW bits 0-15.

The same sequence occurs for each character received.



START-STOP SDF TO PDF TRANSFERS BY LCD CODES.



DIAL OPERATION
(PART 1 OF 2)

See B-510 for a flow chart of this dial operation.

The following sequence outlines a suggested procedure which may be taken to perform a dialing function.

Lower Level Disabled Code (L2 Masked)

Address the *autocall interface* and execute Input X'45' to input SDF bits 0-7. DLO must be inactive to proceed with the dial operation. (If DLO is active either a dial operation has already been started, the line interface has not been disabled and has auto answered an incoming call, or a failure has occurred). If the IR bit is on, reset it by executing Output X'46'. Set the PCF state to X'4'. (Monitor Call ACR, COS, PND) to cause the CRQ latch to set in the autocall interface, and initiate a timeout.

Address the associated *line interface*. Set the PCF to X'0' (NO-OP), set SDF to turn DTR on, and set the PCF to X'1' (Set Mode).

1. L2 interrupt for associated *Line Interface* Reset service request (ICW Bit 1), and set PCF to X'2' (Monitor DSR).
2. First L2 interrupt for *autocall interface* (assuming the timeout did not complete).

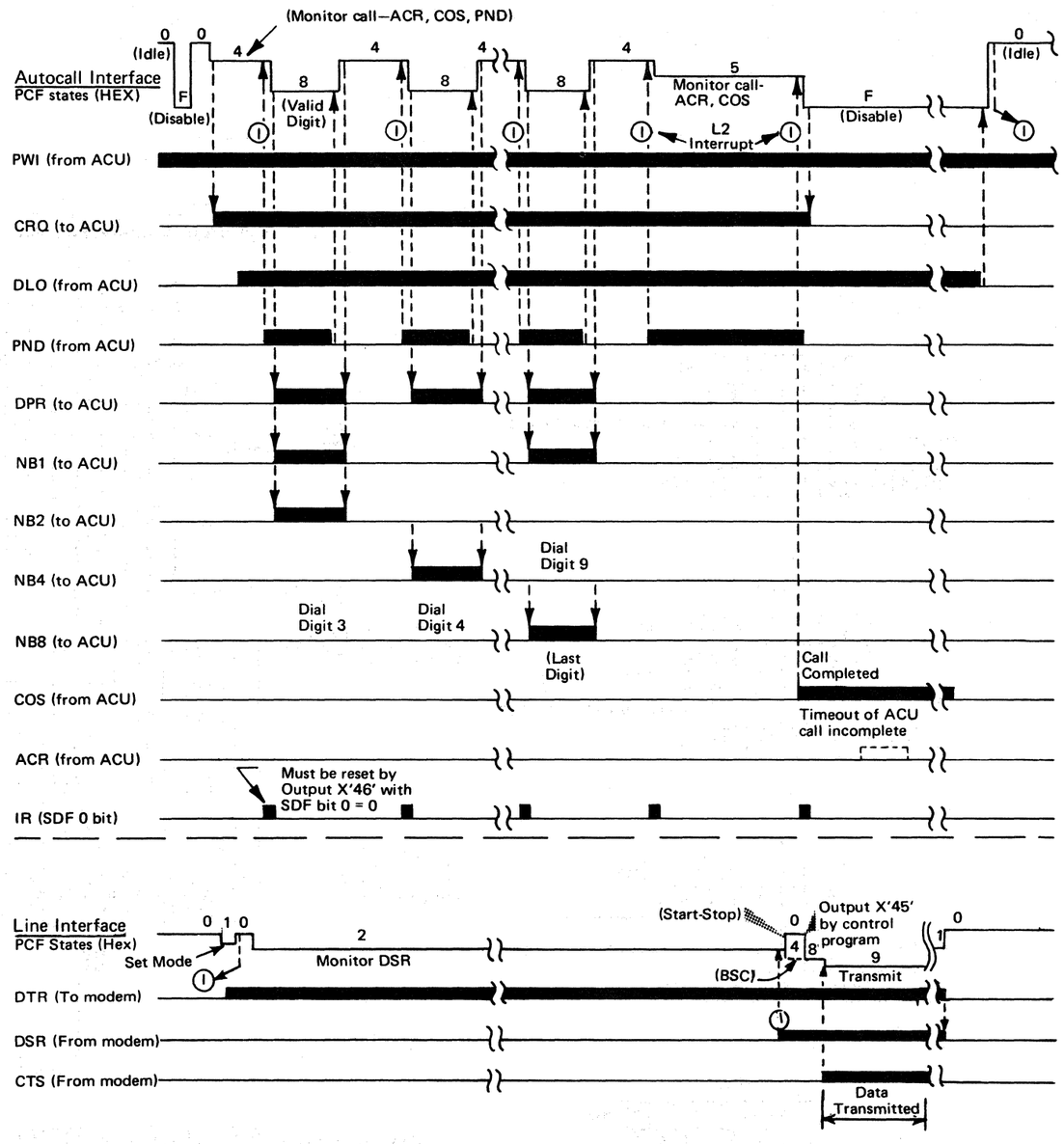
   The PCF state should be X'4' (Monitor Call ACR, COS, PND). Input SDF Bits 0-7. Check to see that ACR and COS are OFF and PND is on. Place the proper dial digit in PDF Bits 4-7, and after resetting ICW Bit 1, place the PCF in state X'8' (Valid Digit) to cause the DPR latch to be set in the autocall interface. Reset the IR bit by executing Output X'46', and initiate a timeout.
3. L2 interrupts for *autocall interface* for all but the last digit (assuming the timeout did not complete). Same action as in 2.
4. Last digit L2 interrupt for *autocall interface* (assuming timeout did not complete).

   The PCF state should be X'4'. Check to see if COS is on.

If COS is off, check to see if ACR is on. If ACR is on, the connection has not been established before ACR time-out and retry is suggested. If ACR and COS are off, reset ICW bit 1, place the PCF in state X'5' (Monitor ACR, COS), reset the IR bit by executing Output X'46', and initiate a timeout. When the next interrupt occurs, either ACR or COS, or both, should be on. If COS is off, appropriate retry action should be taken. If COS is on, the same action should be taken as described in the following paragraph.

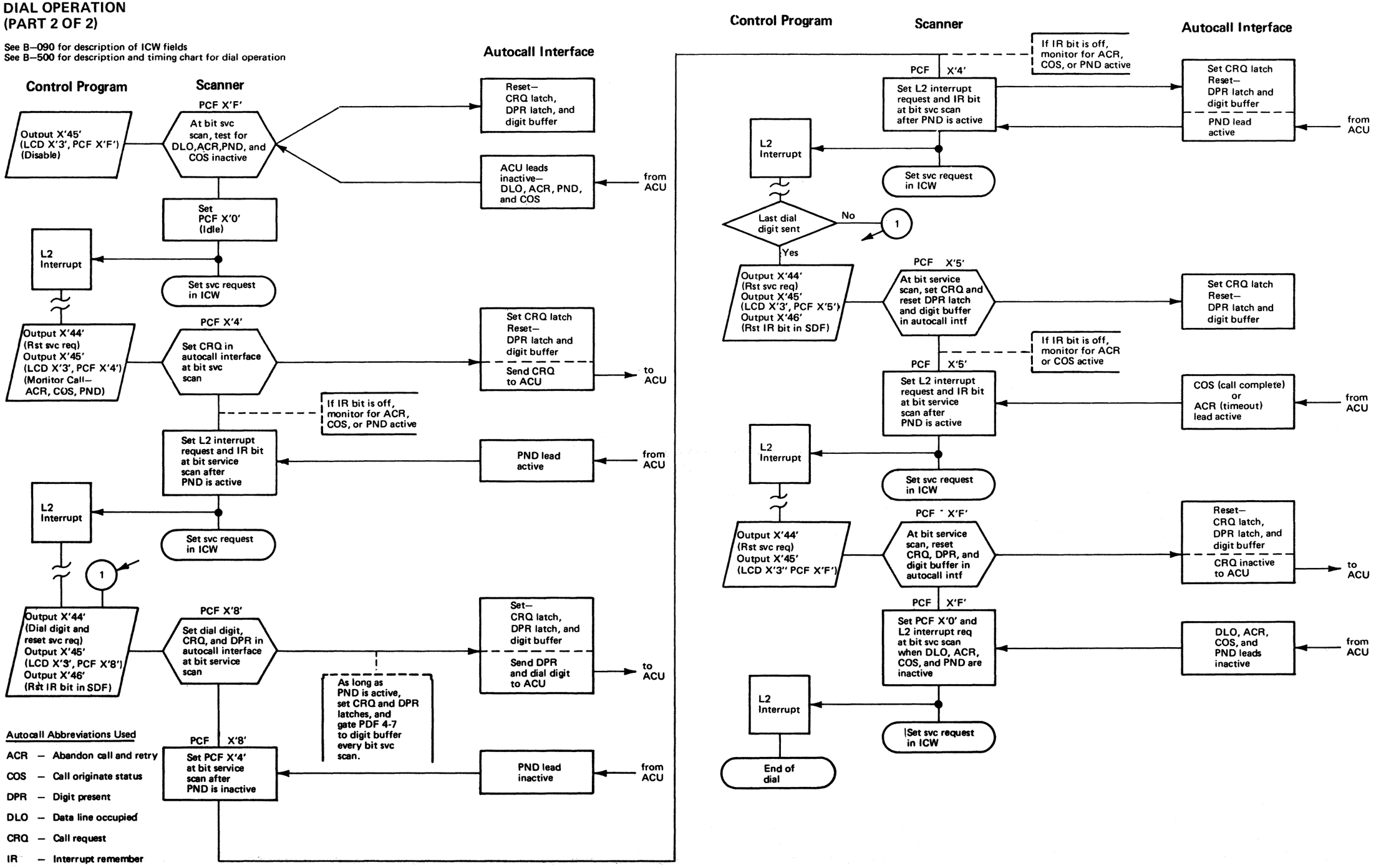
If COS is on, the connection has been established. After resetting ICW Bit 1, place the PCF in state X'F' (Disable) and reset the IR bit by executing Output '46'. When the call completes, a timeout should be initiated on the autocall interface. If DLO, COS, PND and ACR all become inactive, causing the interface to request a L2 interrupt, the timeout should not complete. If the timeout completes before the L2 interrupt, appropriate error recovery procedures should be invoked.

SEQUENCE CHART FOR DIAL OPERATION



DIAL OPERATION (PART 2 OF 2)

See B–090 for description of ICW fields
See B–500 for description and timing chart for dial operation



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DIAGNOSTIC WRAP

Diagnostic Wrap

- Provides a means of testing and locating troubles in the type 2 scanner line control logic and line-interface receive logic.
- Provides a method of on-line program testing.
- Can be performed on-line without affecting the operation of lines *not* in diagnostic mode.

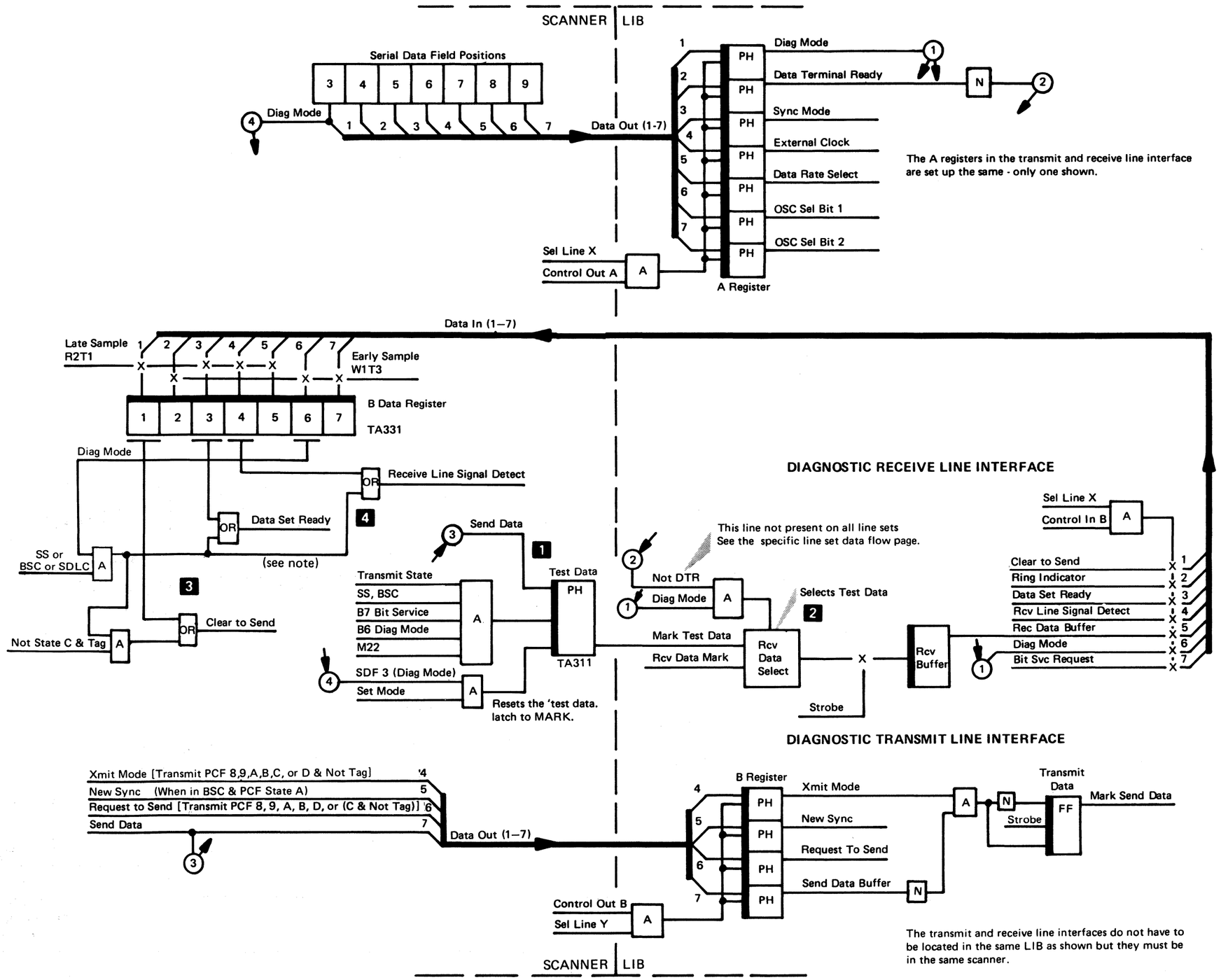
Setup

- Set any one line interface per type 2 scanner to act as a transmit line and any one or more line interfaces in the same scanner to act as receive lines.
- Set Mode is issued to all diagnostic receive line interfaces first, then to the diagnostic transmit line. The SDF field must be set as follows:
  - SDF 3 (Diagnostic Mode) – set to 1.
  - SDF 4 (Data Terminal Ready) – reset to 0.
  - SDF 5 (Sync Mode) – set to 1 for BSC.
    – reset to 0 for start-stop.
  - SDF 6 (External Clock) – reset to 0.
  - SDF 7 (Data Rate Select) – May be 1 or 0 for all line sets.
  - SDF 8 and 9 (Oscillator Select 1,2) – Select an available internal oscillator bit rate. The rate must be the same for the transmit and receive line interfaces.

Operation

1. After the Set Modes are issued, the affected line interfaces can be exercised through any sequence of point-to-point or multipoint operations.
2. Data bits clocked to the transmit line interface 'send data buffer' are also clocked into the 'test data' latch in the type 2 scanner. **1**
3. As each receive line interface (in diagnostic mode) is scanned, the 'test data' bit is strobed into the 'receive buffer' instead of the 'receive data mark'. **2**
4. When the 'diagnostic mode' bit is a 1 in the B data register (B6) during scan time, the type 2 scanner simulates the active states of:
   - 'Data Set Ready' and 'Clear to Send'. Clear to Send is not simulated **3** active if PCF=X'C' and the 'tag' is on (scanner has completely serialized the character in the SDF).
   - 'Receive Line Signal Detect' to turn on ICW bit 4. **4**

Note: *Diagnostic mode does not force RLSD to a 1.*



SDLC TRANSMISSION FRAME FORMAT

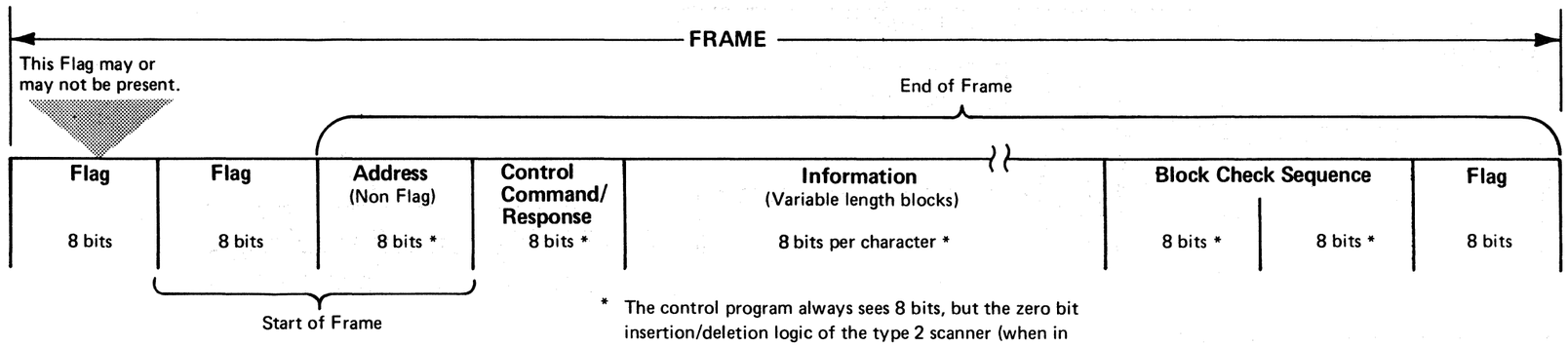
Flag

The Flag is a unique sequence of bits that cannot inadvertently be duplicated in the data stream that is used to signal the start and end of each frame.

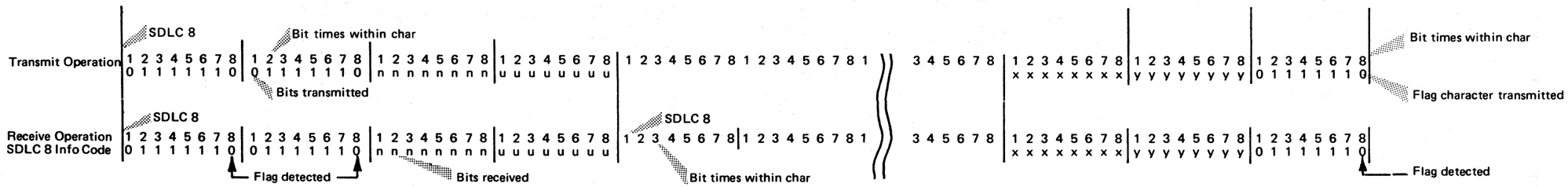
- The bit sequence is 0111 1110.
- A minimum of one Flag precedes each frame.
- The End Flag may serve as the Start Flag of the next frame.
- When in receive mode, the scanner continuously monitors the line for the appearance of a Flag.

Abort

The scanner interprets a binary zero followed by a sequence of seven binary ones (0111 1111) as Abort and sets SCF 0 to a 1 and resets SCF 1 to 0.



* The control program always sees 8 bits, but the zero bit insertion/deletion logic of the type 2 scanner (when in NRZI mode) may transmit/receive more than 8 bits over the communications facility.



SDLC MODES OF OPERATION

NRZI Mode

When receive timing is derived from bit transitions in the data, the transmission technique is inherently sensitive to transitionless data; a series of consecutive binary one bits or binary zero bits. The zero bit insertion technique, to preclude the appearance of Flag sequences within the frame, assures that sequences of consecutive one bits longer than 5 will not occur in the transmission, except for the transmission of the Flag (6 ones) or the Abort (7 ones). In order to prevent the occurrence of extended periods of transitionless data due to consecutive zero bits, zero complemented differential coding (NRZI) is used when SDLC transmission utilizes non-synchronous type modems, equivalent free standing modems, or synchronous modems with data derived clocks.

The control program sets ICW bit 44 (NRZI control) when transmission is to occur in NRZI mode.

Transmit Operation

When transmitting in NRZI mode, the scanner:

- Complements the state of the 'send data' ('CSB data out 7') line to the 'send data' buffer in the selected line interface to transmit a zero bit.
- Does not change the state of the 'send data' line to transmit a 1 bit. This results in continuous transitions (one per bit service request) in the event of consecutive zero bits and no transitions for the case of consecutive one bits.
- Holds the 'send data' line to a steady binary on (Mark) level when PCF state X'8' (initial transmit) is active.
- Sets PCF X'9' (transmit normal) when Clear To Send becomes active and begins transmitting the bit synchronizing pattern, Flag sequences, data, and so forth.

Receive Operation

When receiving in NRZI mode, the scanner:

- Makes the new bit a complement of the 'last line state' if the 'receive data buffer' receives a 1 (Mark).
- Makes the new bit the same as the 'last line state' if the 'receive data buffer' receives a 0 (Space).

When a 6th binary one is received, the scanner inspects the next data bit and if it is a binary zero, the total combination (0111 1110) is the Flag. The scanner recognizes the Flag character and automatically changes from PCF X'5' (monitor Flag) to PCF X'6' (receive info-inhibit data interrupts) to monitor for a non-Flag character. The scanner recognizes the 'start of frame' when a Flag character is followed by an eight-bit non-Flag character and automatically changes the PCF state from X'6' to X'7'.

The Flag should be detected on the normal boundary. The following chart shows the predicted position of the Flag bits in the SDF at the time the Flag should be detected. If the Flag is detected at other than this configuration of the tag bit, the scanner sets SCF 2 bit to 1.

The bits in the shaded area are the remaining Flag bits when the Flag should be detected (see B-520) with the last 0 bit received in the new bit position. The 1* is the receive Tag bit shifted right.

Flag Detect Predicted Position

	SDLC Code	*New Bit Pos.*	*SDF Positions 0 1 2 3 4 5 6 7 8 9*
Normal boundary	8	0	1 1 1 1 1 1 0 0 0 1*

*Receive Tag bit

When 'end of frame' is sensed by the control program, the control program performs a block check.

Non-Synchronous Communication Channel Bit Synchronous Requirements

When business machine clocking is being used and the remote clock is not in phase (for example — half duplex operation or the first transmission following a line turnaround) the first two characters must be X'100' and X'00' respectively. The first two characters transmitted are X'00'; the 1 bit in the initial character X'100' is not transmitted but is used as the tag bit. These two characters, in conjunction with the NRZI encoder, provide the remote business machine 16 transitions for clock synchronization. When using modem clocking or the remote clock is in bit phase, these two leading characters are not required.

Zero Bit Insertion/Display

Transmit Mode

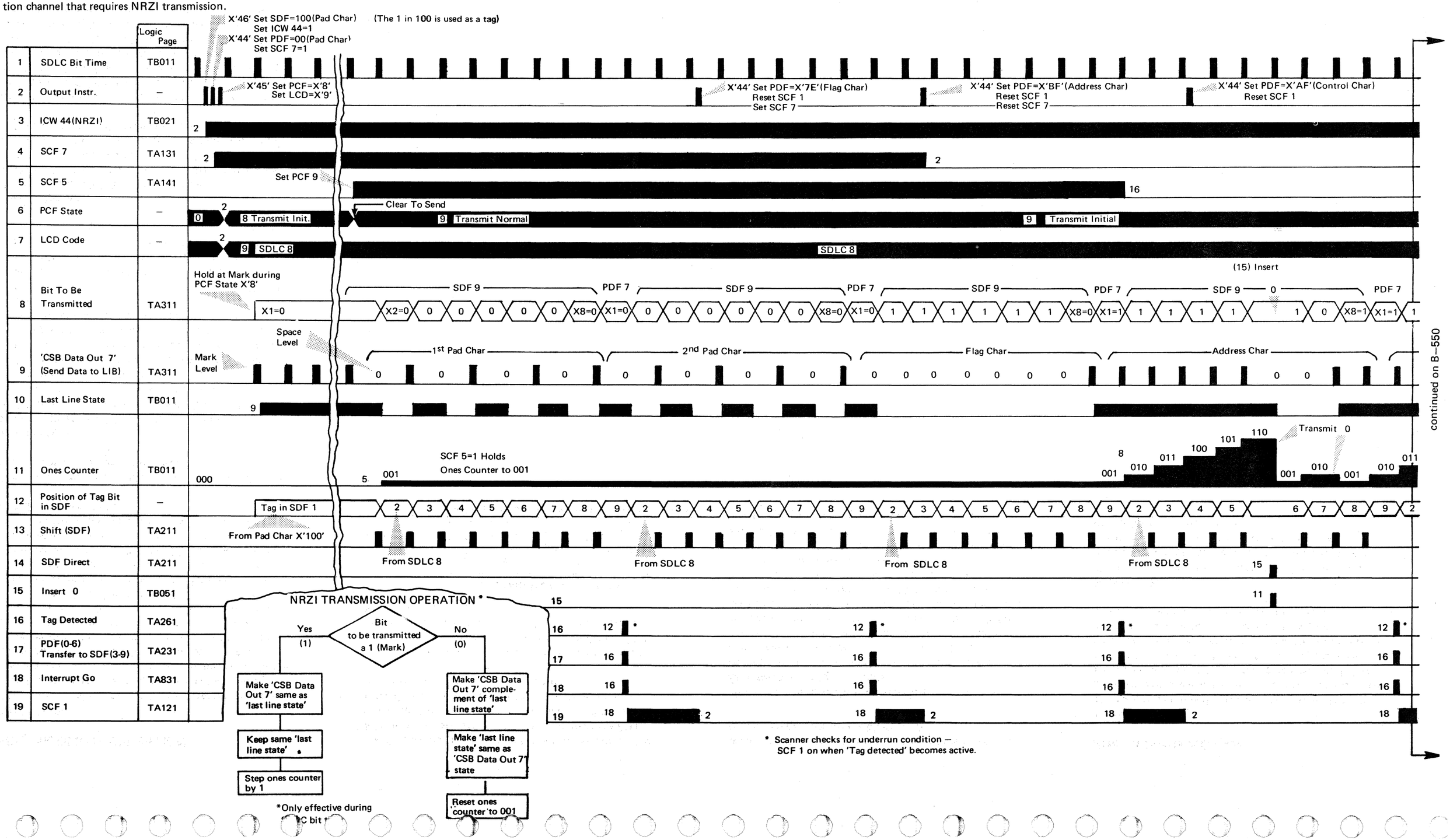
The scanner monitors the sequence of transmit data bits and when a consecutive sequence of 5 binary ones is noted, the scanner automatically inserts a binary zero bit before transmitting the next data bit. This includes the transmission of block check characters. Thus there will never be a consecutive sequence of transmitted binary one digits exceeding 5 within the frame except the Flag or Abort.

Receiving Mode

The scanner monitors the stream of received data bits and inspects the bit following any consecutive sequence of 5 binary one bits. If this bit is a binary zero, the scanner deletes it from the data stream.

SDLC TRANSMIT SEQUENCE (PART 1 OF 2)

This example is for a non-synchronous type communication channel that requires NRZI transmission.

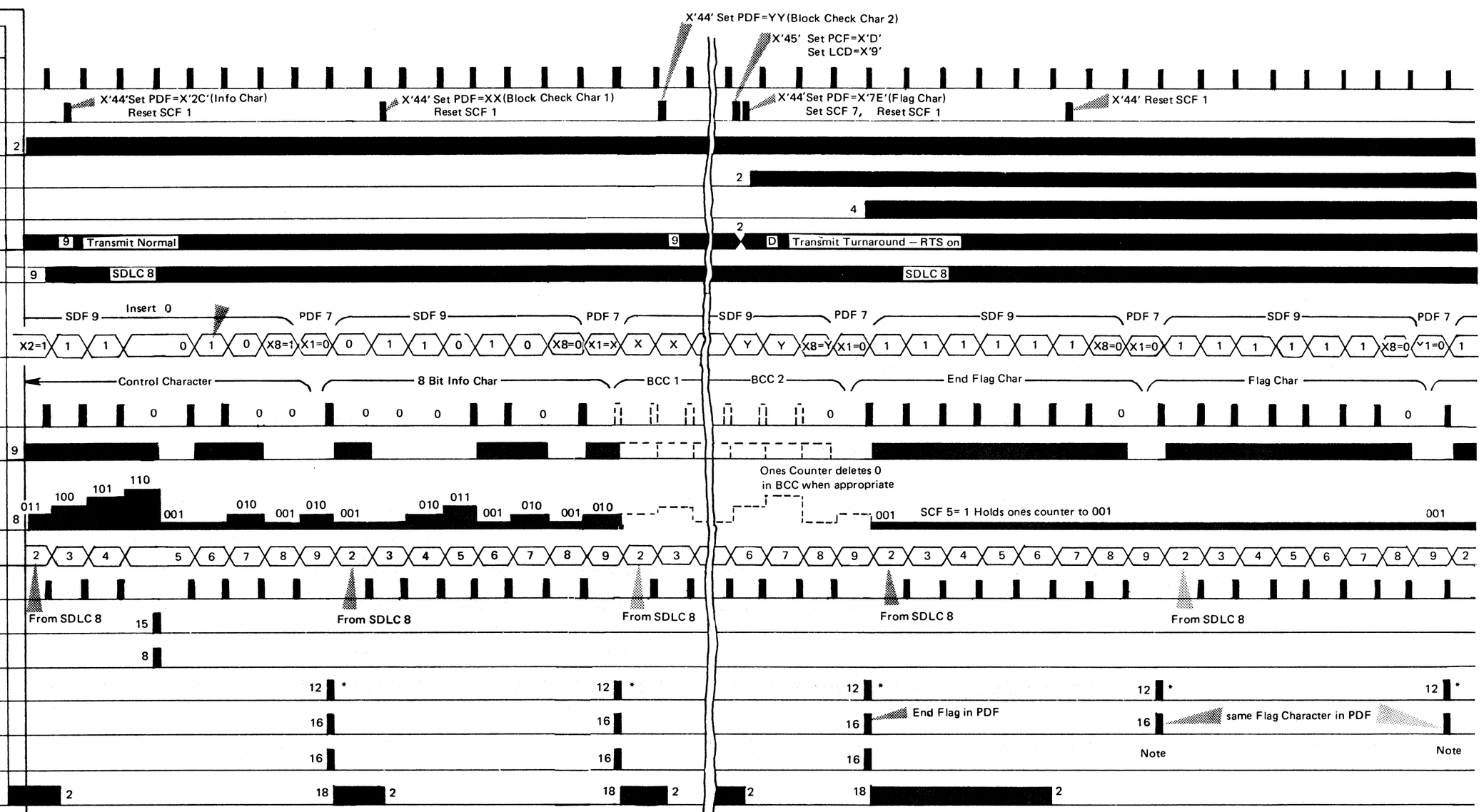


continued on B–550

SDLC TRANSMIT SEQUENCE (PART 2 OF 2)

continued from B-540

		Logic Page
1	SDLC Bit Time	TB011
2	Output Instruction	–
3	ICW 44(NRZI)	TB021
4	SCF 7	TA131
5	SCF 5	TA141
6	PCF State	–
7	LCD Code	–
8	Bit To Be Transmitted	TA311
9	'CSB Data Out 7' (Send Data to LIB)	TA311
10	Last Line State	TB011
11	Ones Counter	TB011
12	Position of Tag Bit in SDF	–
13	Shift (SDF)	TA211
14	SDF Direct	TA211
15	Insert 0	TB051
16	Tag Detected	TA261
17	PDF (0-6) Transfer To SDF (3-9)	TA231
18	Interrupt Go	TA831
19	SDF 1	TA121

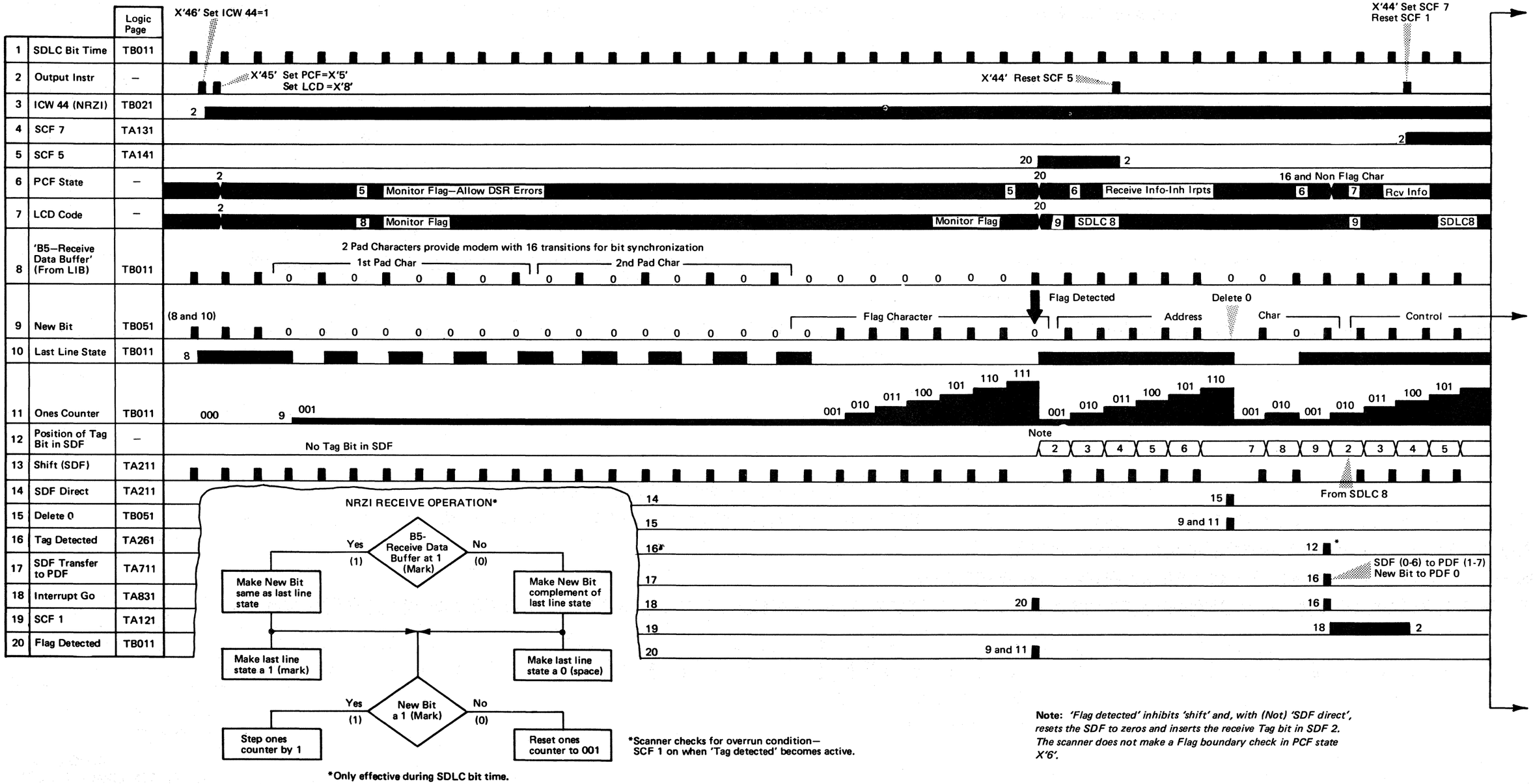


* Scanner checks for underrun condition— SCF 1 on when 'Tag detected' becomes active.

Note: *When in PCF state X'D', the scanner continuously serializes the Flag Character to the line interface without further interrupts until the service routine ends it — normally by setting PCF X'9'. This PCF state sequence is used for duplex operation where this SDLC transmit operation occurs on a low order line interface address while the corresponding receive operation occurs on a high order line interface address.*

SDLC RECEIVE SEQUENCE (PART 1 OF 2)

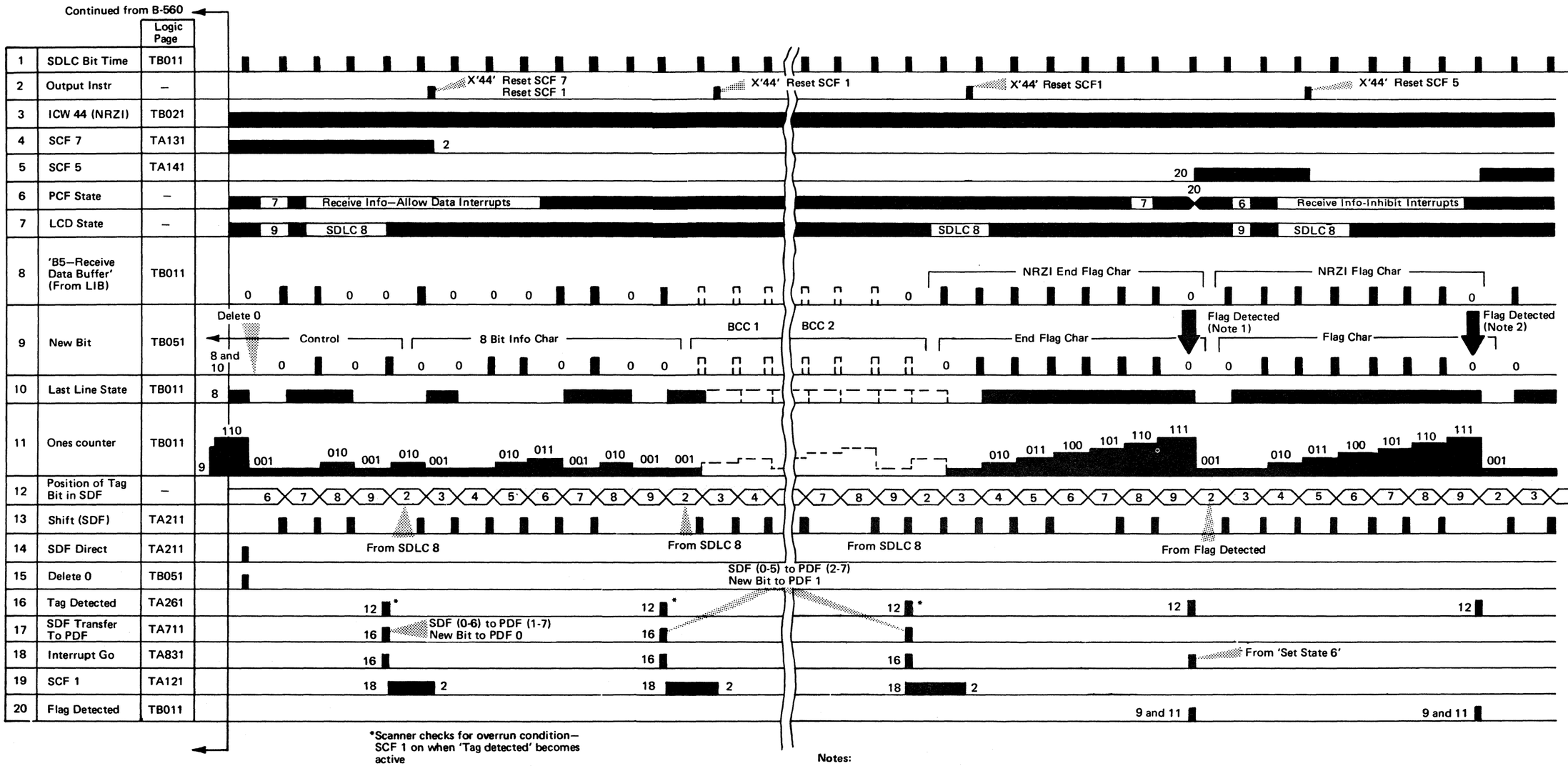
This example is for a non-synchronous type communication channel that requires NRZI receiving. The characters received are those transmitted in the sequence shown on B-540.



Note: *'Flag detected' inhibits 'shift' and, with (Not) 'SDF direct', resets the SDF to zeros and inserts the receive Tag bit in SDF 2. The scanner does not make a Flag boundary check in PCF state X'6'.*

SDLC RECEIVE SEQUENCE (PART 2 OF 2)

Continued from B-560



*Scanner checks for overrun condition–SCF 1 on when 'Tag detected' becomes active

Notes:

1. *When 'flag detected' occurs simultaneously with 'tag detected', the scanner makes a Flag boundary check in PCF state X'7' but does not check the overrun condition, therefore, SCF 2 on would indicate a Flag boundary check-not an overrun condition. The SDF does not transfer the Flag char to the PDF.*

   'Flag detected' inhibits 'shift' and, with (Not) 'SDF direct', resets the SDF to zeros and inserts the receive Tag bit in SDF 2.

2. *When 'Flag detected' occurs simultaneously with 'Tag detected', the overrun condition is not checked. The scanner does not make a Flag boundary check in the PCF state X'6'. The SDF does not transfer the Flag char to the PDF.*

INTRODUCTION (PART 1 OF 2)

Partition Within LIB (Note 1)	Line Interface Address On LIB	Mode of Operation	Line Set Type *														
			LS1					LS2 (Note 2)		LS3 (Note 2)		LS4 (Note 2)	LS5 (Note 2)	LS8 (Note 3)		LS9 (Note 2)	
			EIA Start/Stop External Modem	EIA Synchronous Half-Duplex External Modem	EIA Synchronous Duplex External Modem	EIA Start/Stop Local Attachment	EIA Synchronous SNA Local Attachment	V.35 Interface Half-Duplex	V.35 Interface Duplex	Digital Synchronous Half-Duplex	Digital Synchronous Duplex	Autocall Line	V.35 Interface Local Attachment Half-Duplex	CCITT X.21 Line Half-Duplex Medium Speed	CCITT X.21 Line Duplex Medium Speed	CCITT X.21 Line Half-Duplex High Speed	CCITT X.21 Line Duplex High Speed
1	0	X	X	T	X	X	X	T	X	T	A	X	X	T	Y	T	
	1	–	–	R	–	–	*	*	*	*	A	*	–	R	*	*	
	2	X	X	T	X	X	X	R	X	R	A	X	X	T	*	R	
	3	–	–	R	–	–	*	*	*	*	A	*	–	R	*	*	
2	4	X	X	T	X	X							X	T			
	5	–	–	R	–	–	NA	NA	NA	NA	NA	NA	–	R	NA	NA	
	6	X	X	T	X	X							X	T			
	7	–	–	R	–	–	NA	NA	NA	NA	NA	NA	–	R	NA	NA	
3	8	X	X	T	X	X							X	T			
	9	–	–	R	–	–	NA	NA	NA	NA	NA	NA	–	R	NA	NA	
	A	X	X	T	X	X							X	T			
	B	–	–	R	–	–	NA	NA	NA	NA	NA	NA	–	R	NA	NA	
4	C	X	X	T	X	X											
	D	–	–	R	–	–	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	
	E	X	X	T	X	X											
	F	–	–	R	–	–	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	

Notes:

1. *Partition designations for LIB B are 5, 6, 7, and 8.*
2. *Only available in Partition 1.*
3. *Only available in Partitions 1, 5, 6, and 7.*

Legend

X –	Denotes an address used for a single line interface line set. – is an unused address.
X *	Denotes a pair of addresses required for this line set and mode of operation. * is an unused address.
T R	Denotes a pair of addresses required for this line set and mode of operation. Low order address of pair is transmit. High order address is receive.
T * R *	Denotes four addresses required for this line set. These line sets use two interfaces cabled into a single modem. The line sets must have adjacent addresses. The transmit address must be the low order address. The receive address must be the high order address. * is an unused address.
Y * * *	Denotes an address required for this line set and mode of operation. * is an unused address.
A A	Denotes a pair of addresses used for a two autocall interface if installed.

*The IBM 3705-80 Communications Controller contains the following standard line set configurations.

M81: partitions 2 and 3 each contain an LS1 line set (4 lines).
M82: partitions 2, 3, 5, 6, and 7 each contain an LS1 line set (10 lines).
M83: partitions 1 through 8 each contain an LS1 line set (16 lines).
M84: partitions 2 and 3 each contain an LS1 line set (4 lines), and partitions 5, 6, and 7 each contain an LS8 line set (6 lines).

INTRODUCTION (PART 2 OF 2)

Lines are attached to the 3705-80 through LIBs (Line Interface Bases). The 3705-80 can contain a maximum of two LIBs (LIB A and LIB B). The number of installed LIBs is model dependent. Each LIB is identical and can handle a variety of line and terminal types.

Lines are attached to the LIB through line sets. Each LIB is divided into physical locations corresponding to line addresses. Four line address locations make up a partition, and four partitions make up a LIB. Each partition of the LIB can contain a single line set only.

The LIB consists of one MST board, a BCC (bit clock control) card, and an isolation card. The LIB provides the following general functions.

Drives and terminates all signals from the scanner to the line set interface

Terminates, logically ORs, and redrives all feedback signals from the line set interfaces to the scanner

Provides bit clocking
- Controls bit sampling for lines driven by business machine clocks
- Causes pseudo bit-service requests for lines driven by external data set clocks during periods when the data set clock is not running
- Provides signals to monitor the autocall operation for autocall interfaces.

Note: *In this manual, INTERNAL CLOCK means business machine provided clock, and EXTERNAL CLOCK means modem provided clock.*

The 3705-80 LIB provides for the attachment of up to four line sets. Line set configuration is determined by the 3705-80 model. The following line sets are available.

Line Set LS1 (19.2K bps Attachment)
The LS1 line set provides for the attachment of two half-duplex or duplex, switched or nonswitched lines that can operate at speeds up to 9600 bps. The mode of operation can be either start/stop (S/S), binary synchronous (BSC), or synchronous data link control (SDLC). Limiting the total number of lines scanned to eight (upper scan limit), permits synchronous operation of the lines at a speed of 19.2K bps. Both lines of the LS1 must be attached directly to terminals, or attached using an EIA RS-232C/CCITT V.24 interface to an external modem. The control program may condition these line interfaces for either external clock or business machine clock control (if the speed does not exceed 2400 bps).

Line Set LS2 (56,000 bps CCITT V.35 Attachment)
The LS2 line set provides for the attachment of one duplex or two half-duplex synchronous lines that have a CCITT V.35 interface to an external modem (see Note) for use at line speeds up to 56,000 bps. The control program must condition this line interface for external clock control.

Note: *The LS2 line set in a 3705-80 can be directly attached to a Line Set 1W in a 3705-II for half-duplex operation at 14.4K bps or 57.6K bps.*

Line Set LS3 (50,000 bps Digital Attachment)
The LS3 line set provides for the attachment of one duplex synchronous line for operation at speeds up to 50,000 bps. This line set has a high-speed digital interface for attaching switched or nonswitched lines to a wideband external modem (see Note). The control program must condition this line interface for external clock control.

Note: *IBM control programs do not contain programming for switched line operation of the LS3 line set.*

Line Set LS4 (Auto Call Attachment)
The LS4 line set provides four independent RS-366A/CCITT V.25 interfaces for attachment to external automatic calling units (ACUs). Each interface and attached ACU can be associated by external cabling within any of the line interfaces provided by line sets LS1.

Line Set SI.5 (57.6K bps Direct Attachment CCITT V.35)
The LS5 line set provides for local attachment of two half-duplex synchronous devices which have a CCITT V.35 interface. Clocking is provided by the line set at either 57.6K bps or 14.4K bps. The attached devices must be set for external clock control.

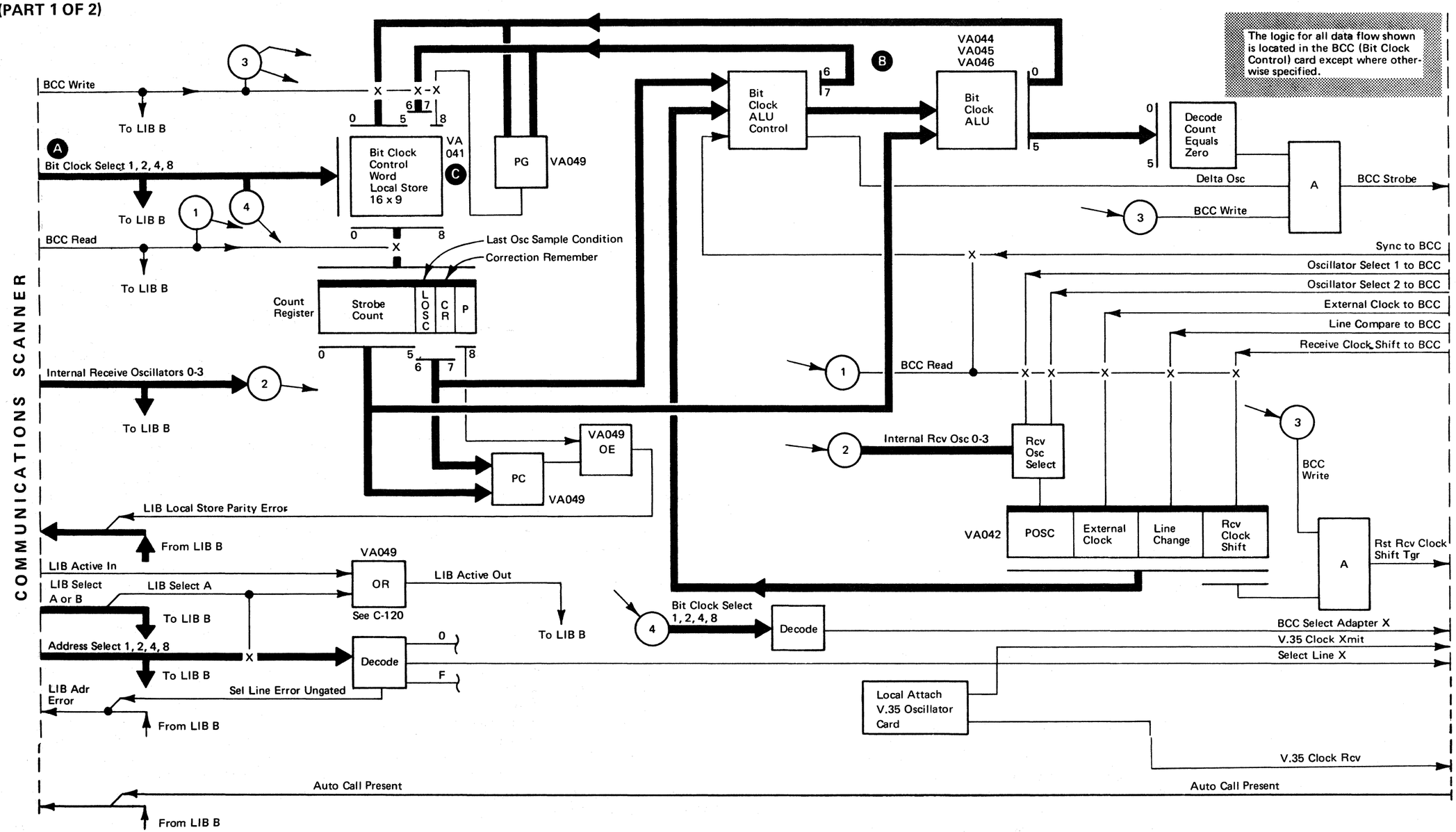
Line Set LS8 (9600 bps CCITT X.21 Attachment)
The LS8 line set provides for the attachment of either two duplex switched or nonswitched synchronous lines, or two half-duplex nonswitched synchronous lines for operation at line speeds of 2400, 4800, or 9600 bps.

For switched line operation, the LS8 line set requires; (1) the latest release of ACF/NCP/VS, (2) a business machine clock that operates at a frequency that is less than 1/24 of the operating speed of the line, and (3) a 2400 bps business machine clock for testing purposes.

Line Set LS9 (48,000 bps CCITT X.21 Attachment)
The LS9 line set provides for the attachment of either a single duplex switched or nonswitched synchronous line, or a single half-duplex switched or nonswitched synchronous line for operation at 48,000 bps.

For switched line operation, the LS9 line set requires; (1) the latest release of ACF/NCP/VS, (2) a business machine clock that operates at a frequency that is less than 1/24 of the operating speed of the line, and (3) a 2400 bps business machine clock for testing purposes.

LIB DATA FLOW (PART 1 OF 2)



LIB DATA FLOW (PART 2 OF 2)

Ⓐ Interface Bit Clock Addressing

In addition to line scanning for servicing requests, the scanner controls the sequential selection of the 16 BCC (bit clock control) words in each LIB. During each selection, one BCC word is addressed, read out, updated, and written back into the LIB BCC local store.

Ⓑ LIB Recieve—Bit Clock Control

The BCC provides bit strobing pulses to the associated line interface to sample the received data if that line is business machine clocked. Controls are provided to strobe start-stop data and/or binary synchronous (or equivalent) business machine clocked data. Corrections are continuously made for synchronous data clocking to assure that strobing occurs in the center of the data bit. When external clocking is provided by the modem, the internal clocking of the bit control is used to determine if the modem clock is providing receive clocking pulses. If clocking pulses are not received from the modem, the bit clock control provides the strobe pulses for both the received data and for pseudo bit service requests so the receive operation can continue. The bit clock control uses a program selectable internal clock that runs at less than one half the line speed. Because strobing occurs at a slower rate than the transmission of data, some data bits are lost and the control program would not recognize the characters received. The control program must detect this condition.

Each LIB has a bit clock control that controls the bit clocking and strobing function for up to 8 interfaces.

Ⓒ Bit Clock Control Word Local Store

Within the BCC card in each LIB is a bit clock control word local store. There is a nine bit BCC word for each interface. The format of the BCC word is:

- Bits 0-5 contain a count field that buffers the count of the internal clock oscillator transitions.
- Bit 6 contains the LOSC (last oscillator sample condition) from the previous interface scan.
- Bit 7 contains a correction remember bit. The correction remember bit on indicates:
  - The count has been forced to 32 at a bit boundary for start-stop receive operations.
  - The count has been adjusted at a line transition for synchronous receive operation with business machine clocking.

    In both cases, the count can only be incremented by one (no additional corrections) until BCC strobe, at which time the correction remember bit is reset.
- Bit 8 is a parity bit.
- Bit Clock Select
  - Output of the bit clock select counter which runs continuously in the attached scanner.
  - Each bit clock selection cycle is 400 ns during which one line interface address in each LIB and the associated BCC word are selected.
  - Sequentially selects 1 of 16 BCC words in each LIB.
  - The same BCC word is selected every 6.4 microseconds.

BUSINESS MACHINE CLOCKS

Up to four business machine clocks (1 standard and 3 optional) may be installed in the communication scanner. The business machine clocks for the scanner may be selected from the following list. Also shown is the power-on warm-up period associated with each business machine clock.

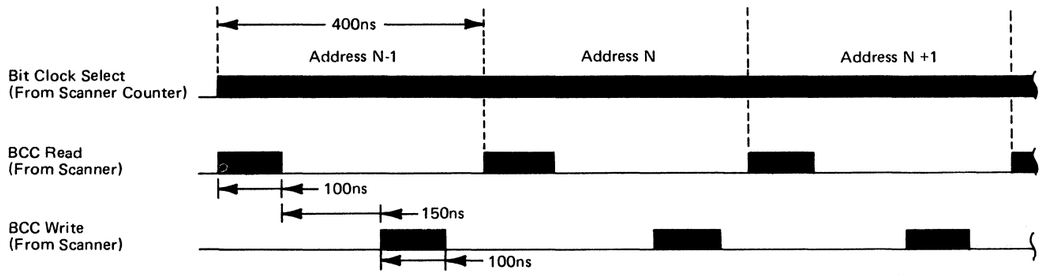
V.35 LOCAL ATTACHMENT CLOCK

If a type LS5 line set is installed in the 3705-80, a special oscillator (located on the LIB A board) provides the required 14,400 or 57,600 bps clock pulses to operate the line set. A jumper on the LIB A board provides the means to select the desired oscillator speed. The V.35 Local Attachment Clock also provides pulses for use by the distant locally attached device.

Power-on warm up time for the V.35 Local Attachment Clock is one second.

- BCC Read
  - Gates the contents of the BCC word to the count register.
  - Gates the status of line interface lines to BCC latches for use by the bit clock ALU control.

BIT CLOCK CONTROL TIMINGS



- BCC Write
  - Gates the updated contents of the strobe count, LOSC, correction remember, and parity bit to the selected BCC word in local store.

Business Machine Clock	*Power-on Warm Up Period (seconds)*
50.0 bps	4
110.0 bps	3
134.5 bps (Basic)	2
200.0 bps	<1
300.0 bps	<1
600.0 bps	<1
1200.0 bps	<1
2400.0 bps	<1

At least one of the above business machine clocks whose speed is less than one half the speed of the lowest speed external clocked line interface must be installed in the scanner. Which installed business machine clock is used for a given line interface is set under program control. For line attachment at speeds greater than above, the external modem or V.35 Local Attachment Clock must provide the clock pulses.

LIB BCC SEQUENCE OF OPERATION (PART 1 OF 3)

The bit clock select lines from the attached scanner sequentially select each BCC word in the BCC local store of each LIB. Four bit-clock select lines (1, 2, 4, 8) are decoded to address the BCC word in the local store (located in the BCC card).

The BCC word is read out of BCC local storage and placed in the clock register at BCC read time.

Since a BCC word is read into the clock register in each LIB every 400 nanoseconds, each bit is sampled at least 64 times for each of the 16 lines operating at 2400 bps—the highest bit rate for business machine clocking. Received data is sampled at a higher rate as the bit rate decreases (see C-050).

At the same time the LIB selects a BCC word from the BCC local store, the associated interface is also selected.

BCC select adapter X gates the following applicable lines from the selected line adapter (see individual line set pages).

'Sync to BCC'
'External clock to BCC'
'Oscillator select bits 1 and 2 to BCC'
'Line compare to BCC'
'Receive clock shift to BCC'

Up to 4 business machine oscillators may be in the attached scanner. For a given bit rate, the same physical oscillator generates the internal receive oscillator and the internal transmit oscillator, but the internal receive oscillator rate is 32 times as fast as the internal transmit oscillator. The receive oscillator gives 64 oscillator changes for every bit time. The internal receive oscillator chart gives the time-per-cycle for each internal clock bit rate. A cycle is the time between consecutive positive going pulses as shown on C-050.

Internal Transmit Osc

Bit Rate BPS	*MS/cycle*
50.0	20.000
110.0	9.091
134.5	7.435
200.0	5.000
300.0	3.333
600.0	1.667
1200.0	0.833
2400.0	0.416

Internal Receive Osc

Bit Rate BPS	*MS/cycle*
50	0.625
110	0.284
134.5	0.232
200	0.156
300.0	0.104
600	0.052
1200	0.026
2400	0.013

One of the four internal receive oscillators is selected according to the state of the oscillator select bits 1 and 2. The state of that selected receive oscillator is placed in the POSC (present oscillator sample condition) latch at BCC read gate time. The states of the external clock, line compare, and receive clock shift are also gated into their respective latches at BCC read gate time.

The bit clock ALU control logic determines whether there has been an oscillator transition since the last BCC scan of that interface. This is done by comparing the present state of the oscillator (POSC) to the last oscillator sample condition from the bit clock control word for that interface. If the oscillator has not changed state since the last bit clock control scan, the bit clock control word is restored to the bit clock control word local store and the bit clock controls wait until the next BCC scan. If the oscillator has changed state, the POSC state is written into the LOSC position of the BCC word in local store. A sequence of decisions is then made to determine what action is to be taken (see Bit Clock ALU Control Flow Chart on C-050).

Start-Stop Operation

If the line interface is attached to a start-stop line, and if a transition has occurred on the receive data line, and if the correction remember bit is off, then the count field in the BCC word is set to a pseudo reset value of 32. The correction remember bit is also set on, and the BCC word is restored to the BCC local store.

If a transition has not occurred, or if a transition has occurred but the correction remember bit is on, a one is added to the count by means of the bit clock ALU; the ALU count is then tested. If the count is zero, the BCC strobe is signaled to the line interface, the correction remember bit is reset, and the updated BCC word returns to the BCC local store. If the count is not zero, the only action taken is the updated BCC word returns to the BCC local store.

The count field in the BCC word is six bits (bits 0-5) and can contain a count ranging from 0 to 63. The count starts at 32 on a bit boundary. The count is then incremented by one every 1/64 of a bit time as determined by the change in the internal receive oscillator. The count eventually increments past 63 to 0. A count of zero causes a BCC strobe to be signaled to the interface where a strobe occurs. The strobe is positioned in the virtual center of the bit.

Synchronous Operation (Business Machine Clocking)

If the selected interface is a line interface attached to a synchronous line that requires business machine clocking, a clock correction technique is used. A test is made to determine if a transition has occurred on the receive data line. If a transition has not occurred, the action is the same as for the start-stop operation—no correction takes place.

If a transition has occurred, the correction remember bit is tested. If the correction remember bit is on, a correction has already been made for that strobe period and the transition of the line is ignored. (**Note:** *A transition occurring with the correction remember bit on indicates a noisy or erratic action on the receive data line.*) Under normal conditions, the correction remember bit in the BCC word is off when the receive data line transition occurs. The two high-order bits of the count field, bits 0 and 1, are examined to determine what correction to make to the count field. The farther the count is from 32 the larger the correction, as indicated in the following chart:

Count Bits 0	*1*	*Corrective Action*	*Count Between*
0	0	Add 5 to count	0-15
0	1	Add 3 to count	16-31
1	0	Subt 2 from count	32-47
1	1	Subt 4 from count	48-63

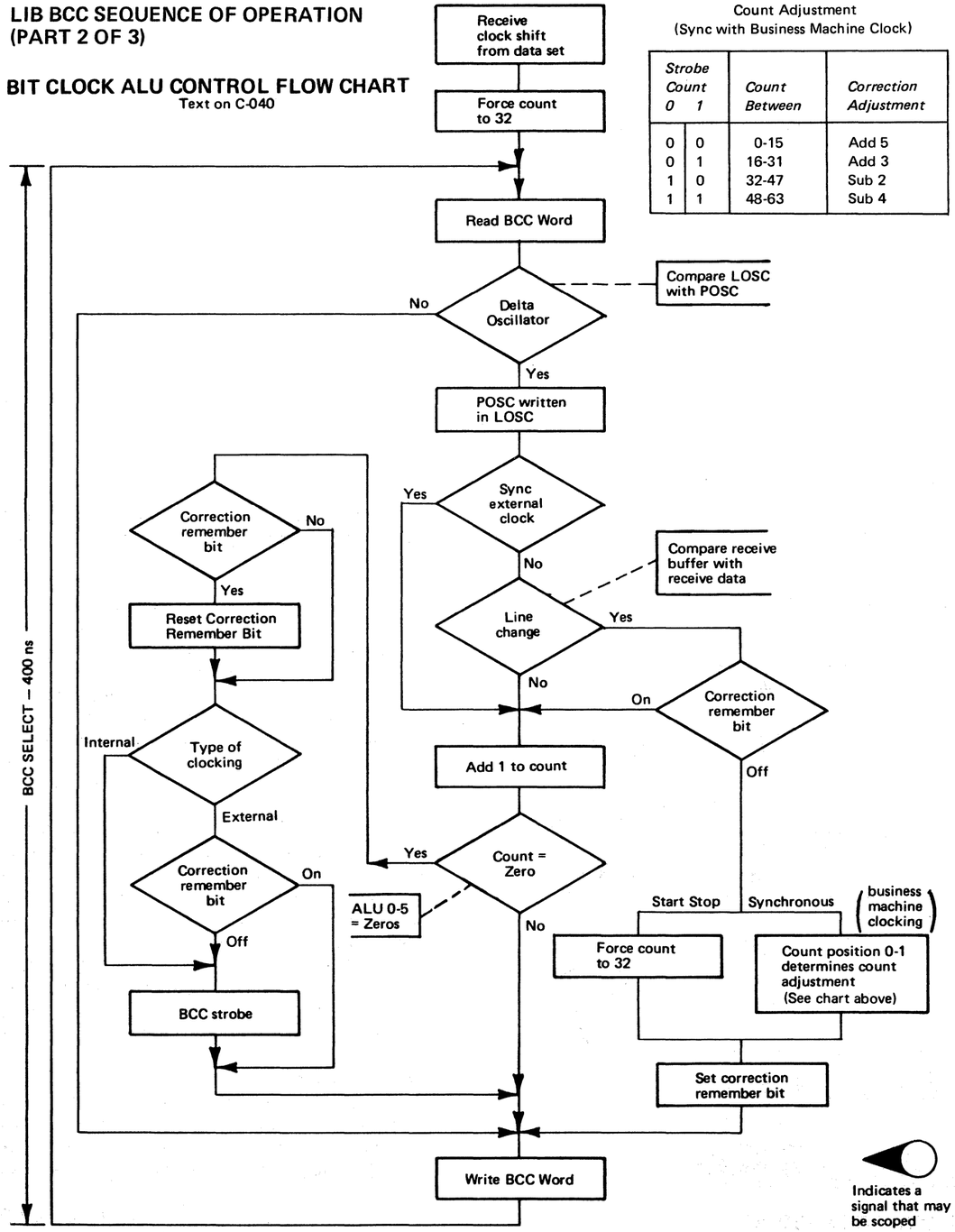
Ideally, the count should be exactly 32 at each data transition. If low, the count is increased in order to advance the strobe time. If high, the count is decreased to delay the strobe time.

The correction is made at the first change in oscillator that occurs when the correction remember bit is off, and when a transition occurs on the receive data line. Corrections are not made when consecutive bits are at the same data level. The count continues to increment by one until it becomes zero at which time the BCC strobe is signaled to the line interface.

LIB BCC SEQUENCE OF OPERATION (PART 2 OF 3)

BIT CLOCK ALU CONTROL FLOW CHART

Text on C-040

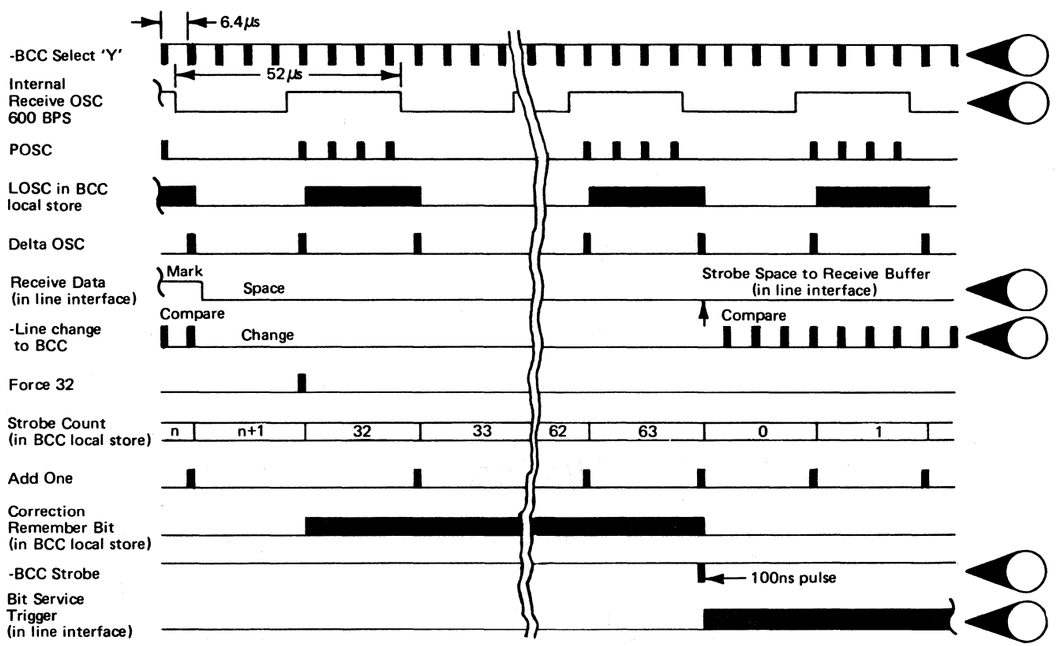


Count Adjustment
(Sync with Business Machine Clock)

Strobe Count 0	1	*Count Between*	*Correction Adjustment*
0	0	0-15	Add 5
0	1	16-31	Add 3
1	0	32-47	Sub 2
1	1	48-63	Sub 4

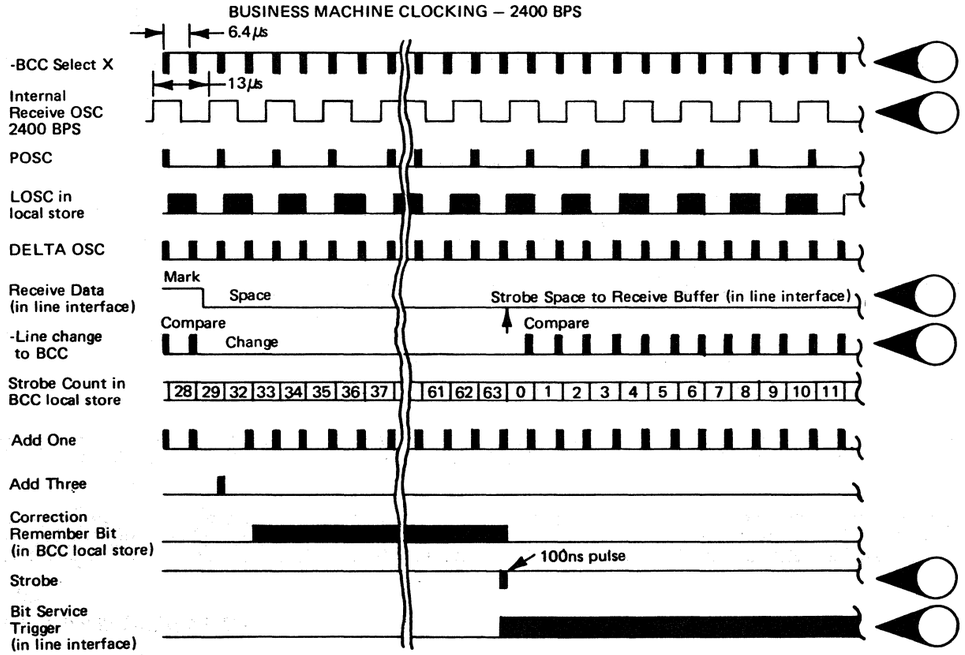
BIT CLOCK CONTROL SEQUENCE FOR START-STOP OPERATION

BUSINESS MACHINE CLOCKING – 600 BPS



BIT CLOCK CONTROL SEQUENCE FOR SYNCHRONOUS OPERATION

BUSINESS MACHINE CLOCKING – 2400 BPS



LIB BCC SEQUENCE OF OPERATION (PART 3 OF 3)

Synchronous Operation (Modem Clocking)

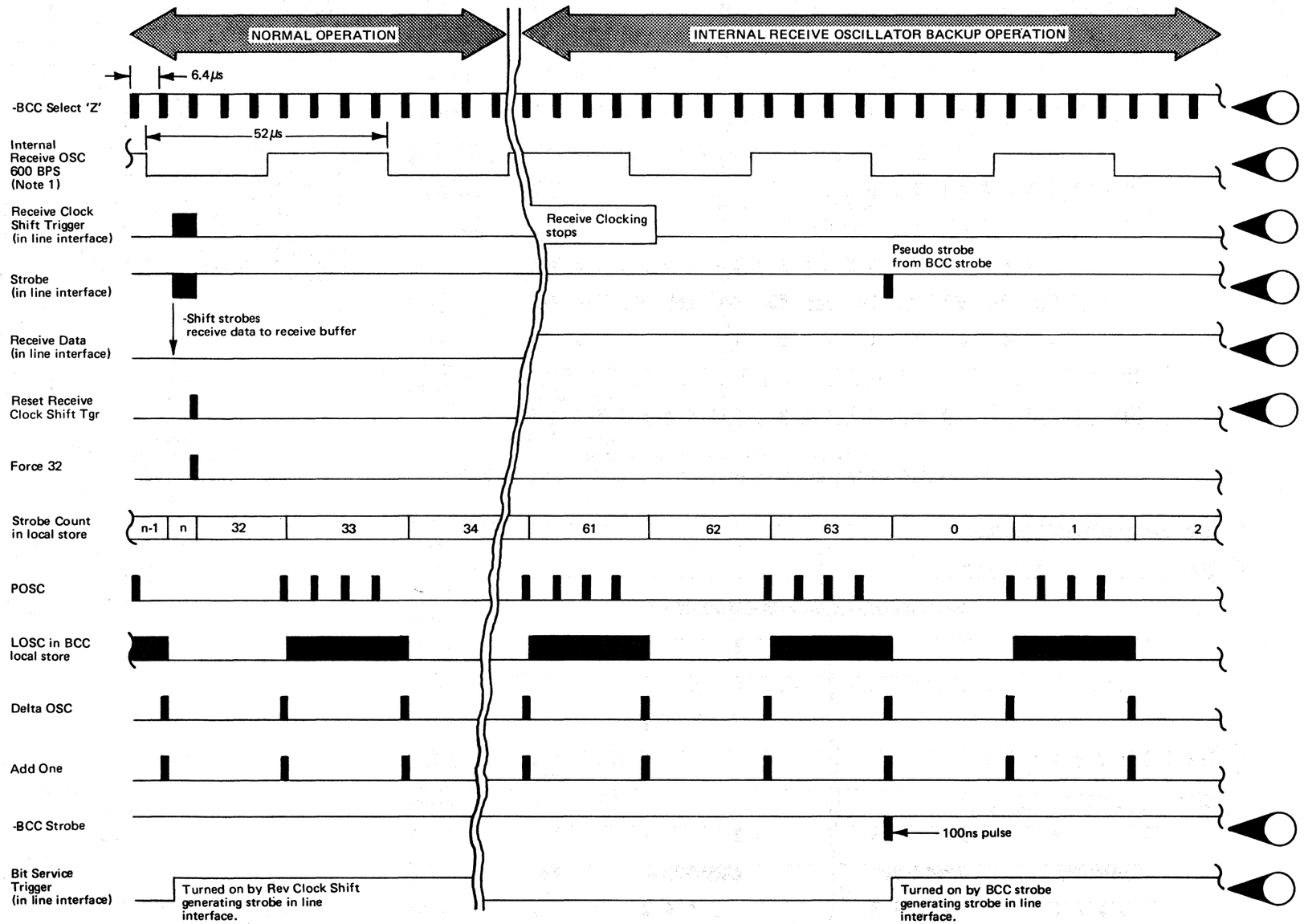
The count is forced to 32 during the BCC select cycle that senses the receive clock shift from the associated line interface. This receive clock shift originated from the negative going transition on the receive clock line from the modem.

A change in oscillator is not required to force the count to 32—however, a delay may exist between the negative transition of the receive clock from the modem and the BCC select cycle. The count is then incremented by one at every change in internal receive oscillator. The internal receive oscillator must run at less than one-half the line bit rate, so that the count will never reach 63 before the next negative transition of the receive clock from the modem repeats the above cycle by forcing the count to 32. The receive data is thus strobed from the modem receive clocking.

If the receive clock from the modem stops, the count eventually increments past 63 to 0. A BCC strobe is signaled to the interface where a pseudo strobe will sample the receive data and cause a bit service request. Because the internal receive oscillator runs at less than half the rate at which the data was transmitted, some data bits are missed. The assembled character is not the character that was transmitted, and as a result, the control characters are not recognized. The control program must detect this condition and take appropriate action.

This internal receive oscillator backup operation is needed to generate pseudo bit service requests to prevent the interface from getting into a 'hung' condition.

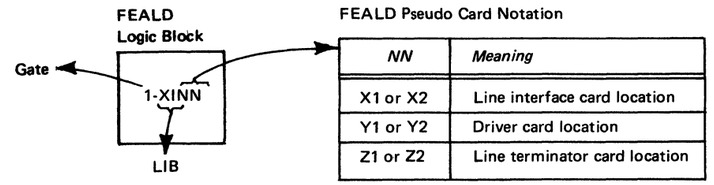
BIT CLOCK CONTROL SEQUENCE FOR SYNCHRONOUS OPERATION MODEM CLOCKING—2400 bps



Note: *The internal receive oscillator must run at less than one half the line baud rate.*

Indicates a signal that may be scoped.

LIB CARD POSITIONS



FEALD Pseudo Card Notation

NN	*Meaning*
X1 or X2	Line interface card location
Y1 or Y2	Driver card location
Z1 or Z2	Line terminator card location

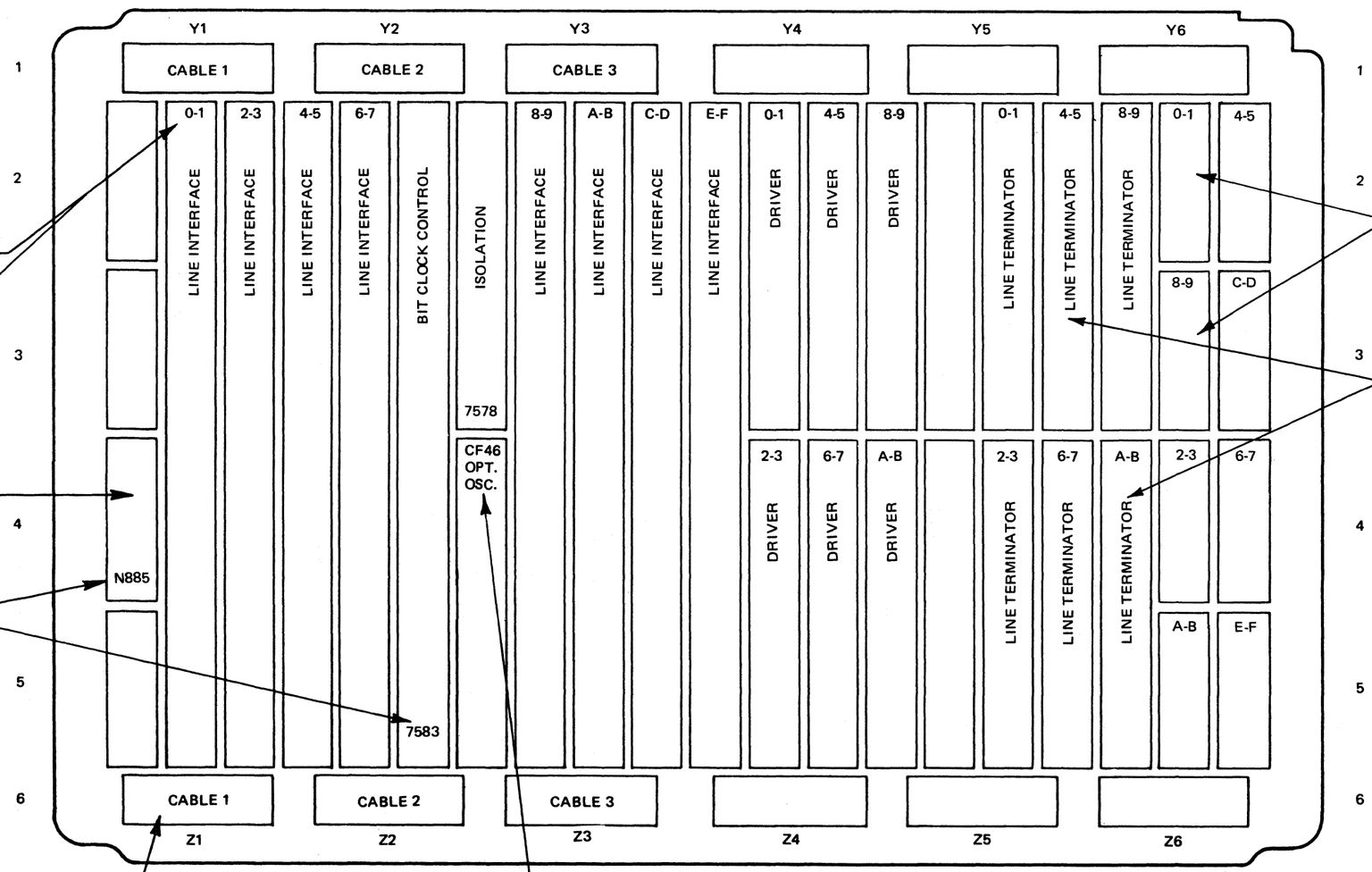
See logic page VA000 for card part numbers and card codes for the line set types that may be installed in this LIB.

Line addresses within this LIB.

The driver and line terminator for LS1 line sets are integrated on the LS1 line interface card. Driver terminator cards are not present for LS1.

Termination card if this is the last board on the interface string

Card Code



The I/O gate cables for LS1 line sets are plugged directly to the board.

The I/O gate cables for LS2, LS3, LS4, LS5, LS8, and LS9 line sets are plugged in the top card connectors of the line terminator cards.

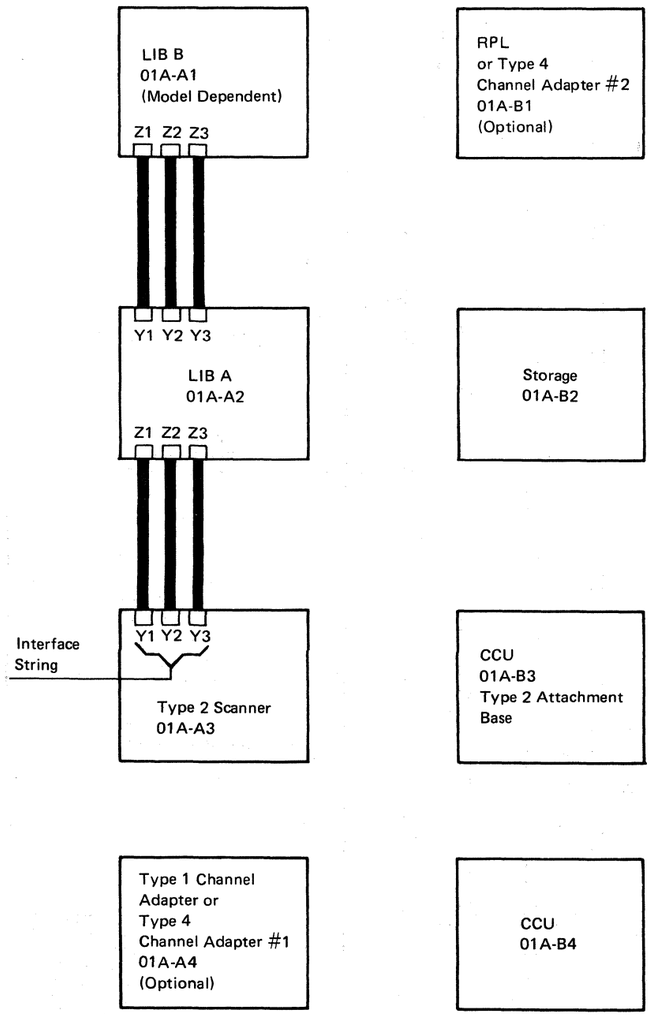
See LIB cabling on C-110

14,400 or 57,600 Hz local attachment oscillator (Used with line set LS5 only.)

1-X1 BOARD
(CARD SIDE)

LIB CABLING

TYPE 2 SCANNER

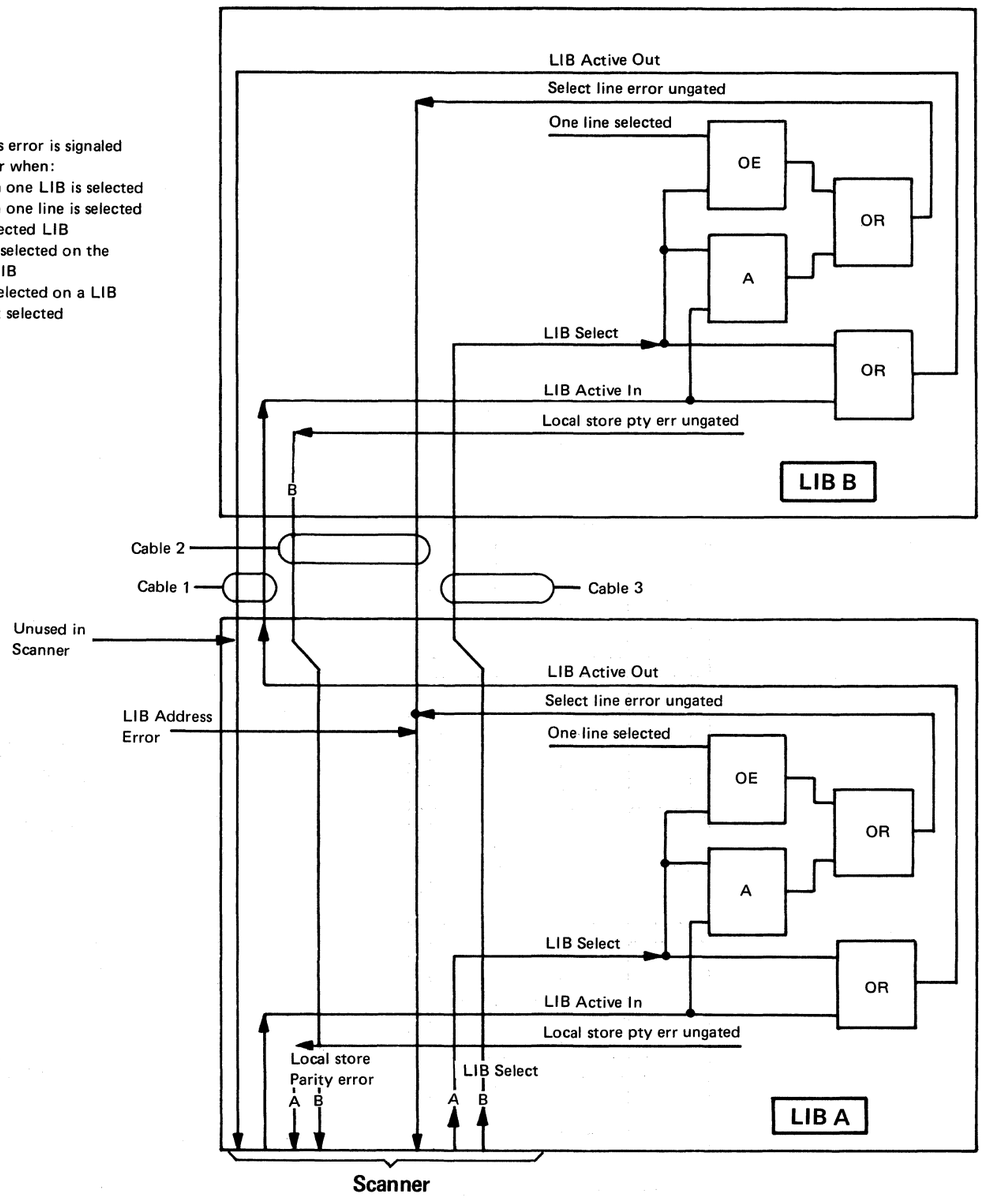


Facing card side of boards.

LIB ADDRESS ERROR AND LOCAL STORE PARITY ERROR

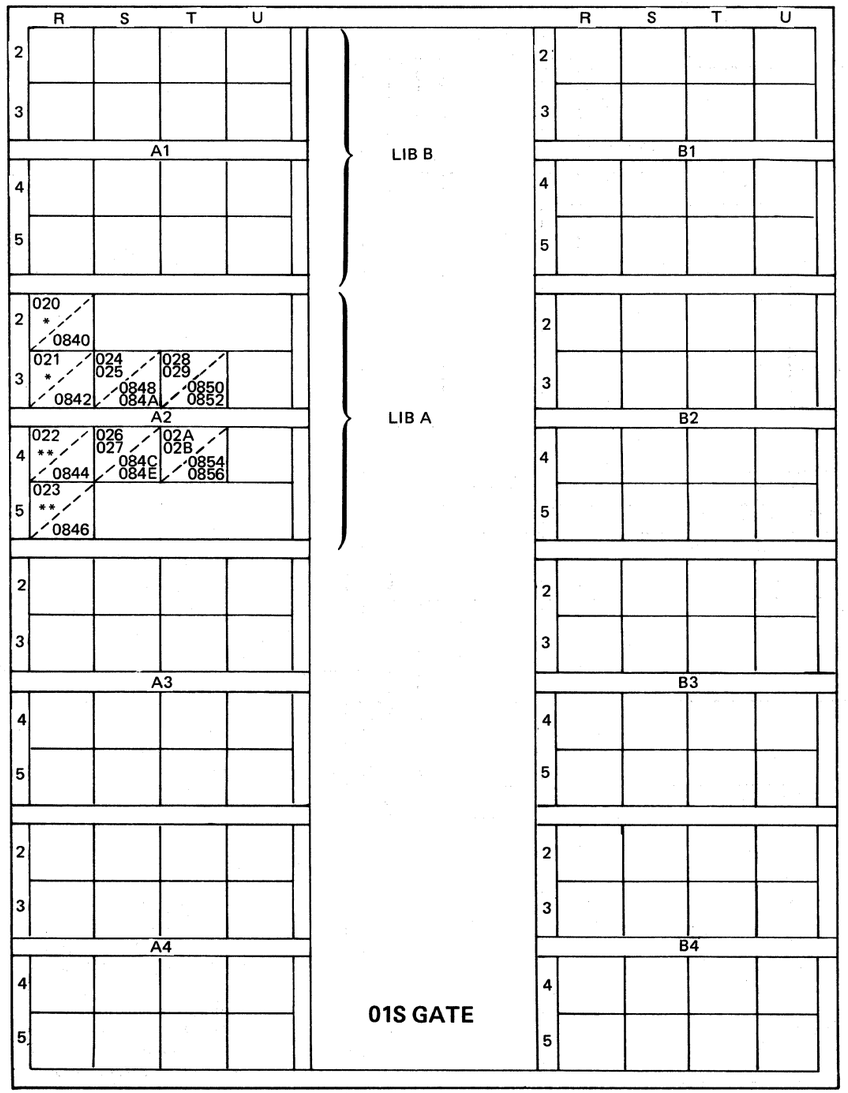
A line address error is signaled to the scanner when:

- More than one LIB is selected
- More than one line is selected on the selected LIB
- No line is selected on the selected LIB
- A line is selected on a LIB that is not selected



I/O GATE--INTERFACE CONNECTOR POSITIONS (PART 1 OF 2)

Type 2 Scanner



Line Interface Address (Hex)

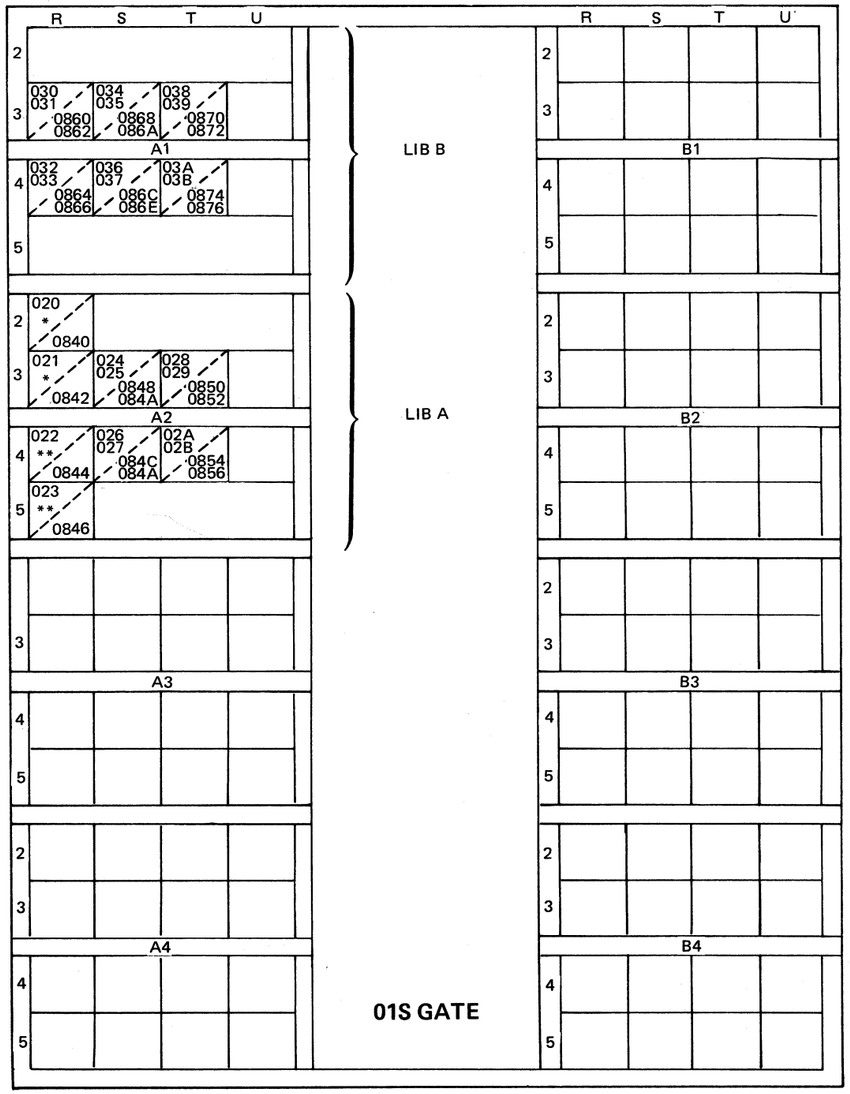
XXX / YYYY

Character Control Block Vector Storage Address (Hex)

See B-330 for relationship of Interface Address and Character Control Block Vector Storage Address.

* PRESENT ONLY IF LINE SET 2 , 3 , 4 , 5 , 8 OR 9 IS INSTALLED IN PARTITION 1
** PRESENT ONLY IF LINE SET 2 (HDX) , 3 (HDX) , 4 , 5 OR 8 IS INSTALLED IN PARTITION 1

View From Outside of Frame
MODEL 81

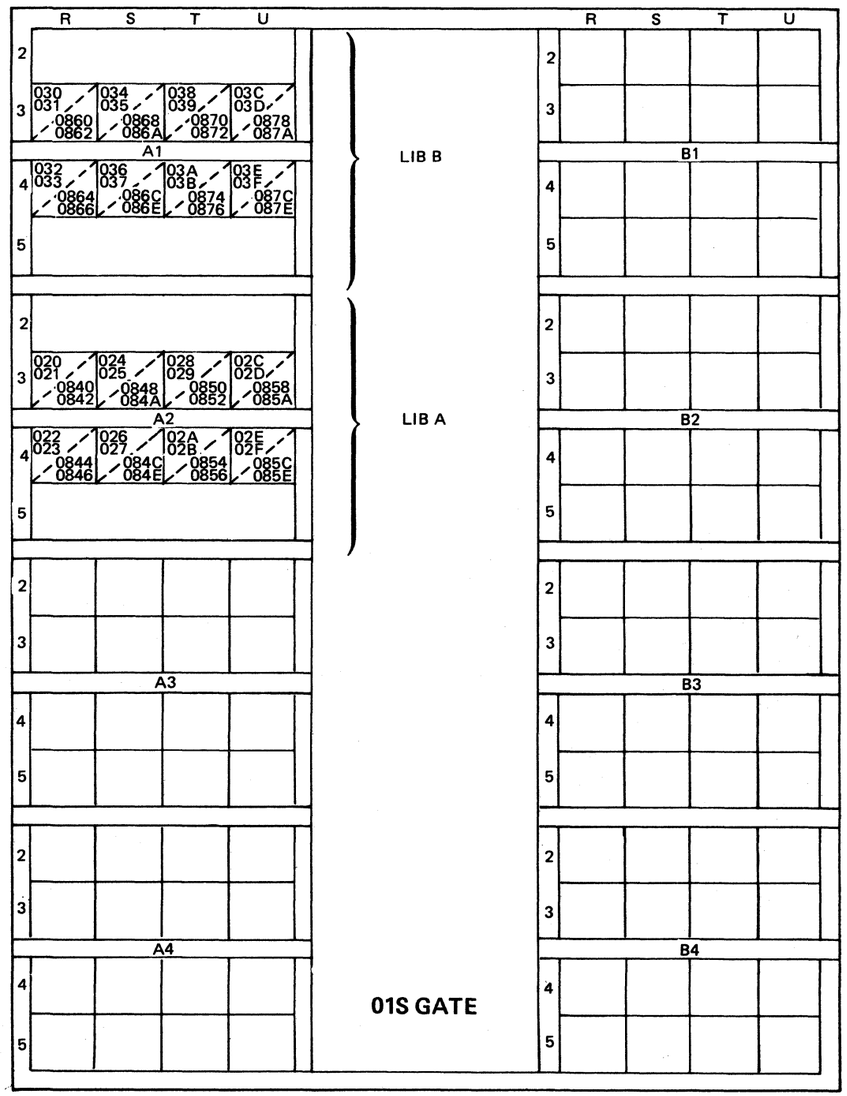


** Present only if line set 2, 3, 4, 5, 8, or 9 is installed in Partition 1
** Present only if line set 2 (HDX), 3 (HDX), 4, 5, or 8 is installed in Partition 1

View From Outside of Frame
MODEL 82

I/O GATE—INTERFACE CONNECTOR POSITIONS (PART 2 OF 2)

Type 2 Scanner



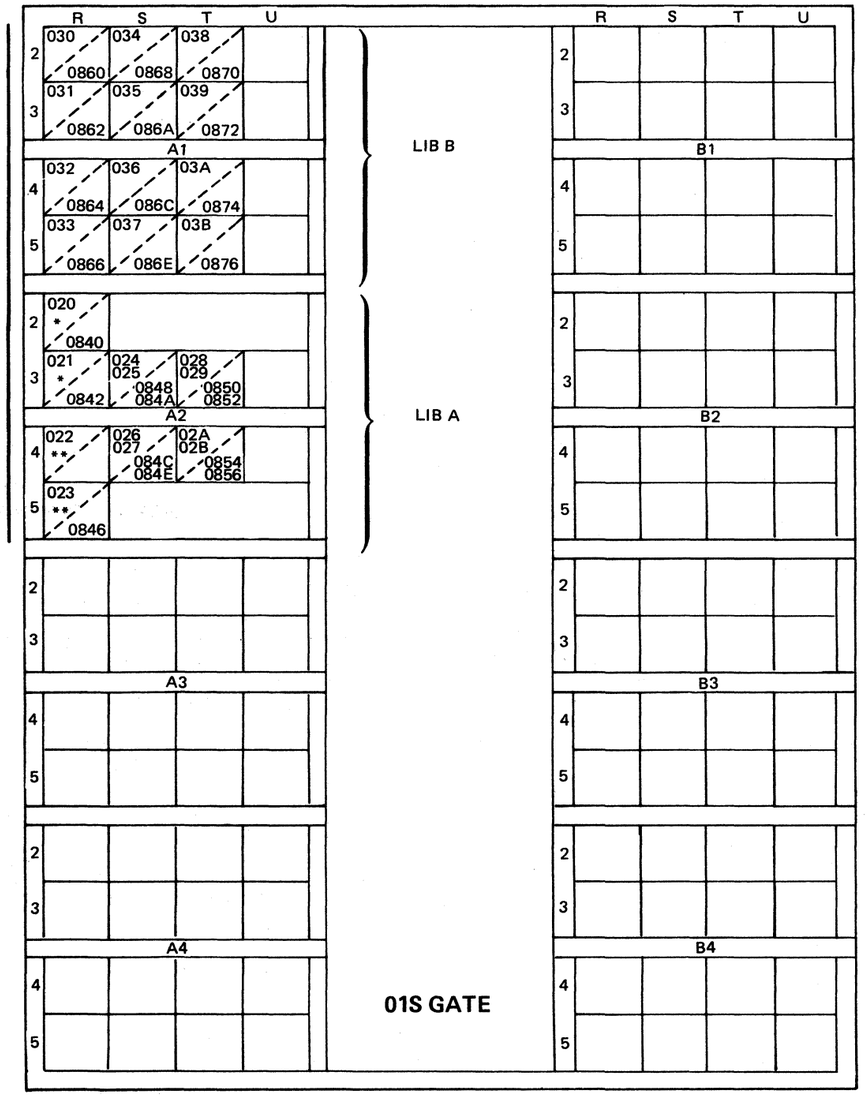
View From Outside of Frame
MODEL 83

Line Interface Address (Hex)

XXX
YYYY

Character Control Block Vector Storage Address (Hex)

See B-330 for relationship of Interface Address and Character Control Block Vector Storage Address.



* Present only if line set 2, 3, 4, 5, 8, or 9 is installed in Partition 1
** Present only if line set 2 (HDX), 3 (HDX), 4, 5, or 8 is installed in Partition 1

View From Outside of Frame
MODEL 84

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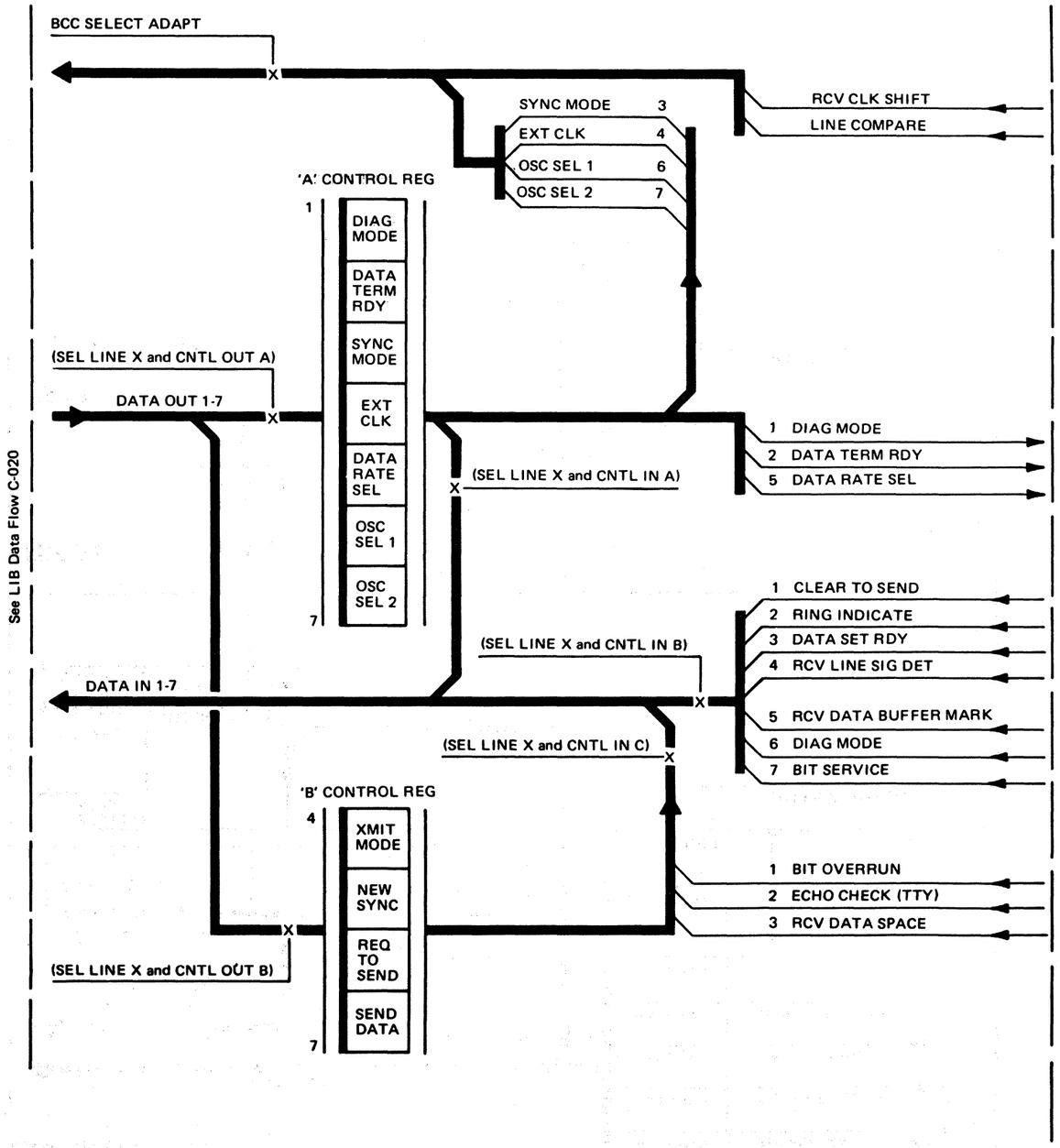
LINE SET INDEX

LINE SET PAGE REFERENCES ALD REFERENCES

Line Set	*Operating Mode*	*Line Interface Data Flow*	*Modem/Line Adapter Data Flow*	*ALD Page*	*Card Location Chart*	*Pin Location Chart*	*Jumper Options*
LS1	EIA Start/Stop External Mode	C-170	——	VB060	VA000	VA003	VA003 & VA004
LS1	EIA Synchronous Half-Duplex External Modem	C-200	——	VB060	VA000	VA003	VA003 & VA004
LS1	EIA Synchronous Duplex External Modem	C-200	——	VB060	VA000	VA012	VA004 & VA012
LS1	Start/Stop Local Attachment	C-170	C-190	VB060	VA000	VA009	VA004 & VA009
LS1	EIA Synchronous/SNA Local Attachment	C-200	C-190	VB060	VA000	VA010	VA004 & VA016
LS2	Half-Duplex CCITT V.35 Interface	C-220	——	VB140	VA000	VA008	——
LS2	Duplex CCITT V.35 Interface	C-220	——	VB140	VA000	VA014	——
LS3	Digital Synchronous Half-Duplex	C-240	——	VB100	VA000	VA006	——
LS3	Digital Synchronous Duplex	C-240	——	VB100	VA000	VA013	VA013
LS4	Auto Call Line	C-260	——	VB080	VA000	VA005	VA005 (cap. asm.)
LS5	Local Attachment Half-Duplex CCITT V.35 Interface	C-270	——	VB150	VA000	VA015	VA015
LS8	Nonswitched CCITT X.21 Interface Half-Duplex/Duplex	C-290	——	VB200	VA000	VA017	VA017
LS8	Switched CCITT X.21 Interface Half-Duplex/Duplex	C-310	——	VB200	VA000	VA017	VA017
LS9	Nonswitched CCITT X.21 Interface Half-Duplex/Duplex	C-290	——	VB200	VA000	VA017	VA017
LS9	Switched CCITT X.21 Interface Half-Duplex/Duplex	C-310	——	VB200	VA000	VA017	VA017

LINE SET GENERAL DATA FLOW



LINE SET LS1–START/STOP (PART 1 OF 2)

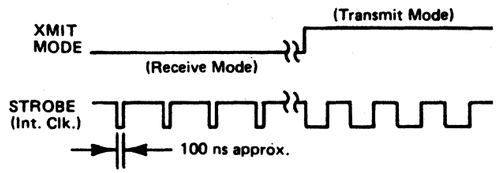
Line Interface

The line interface is a buffer for status and data, transferred between the scanner and the communication line adapter (modem, IBM Line Adapter, telegraph adapter).

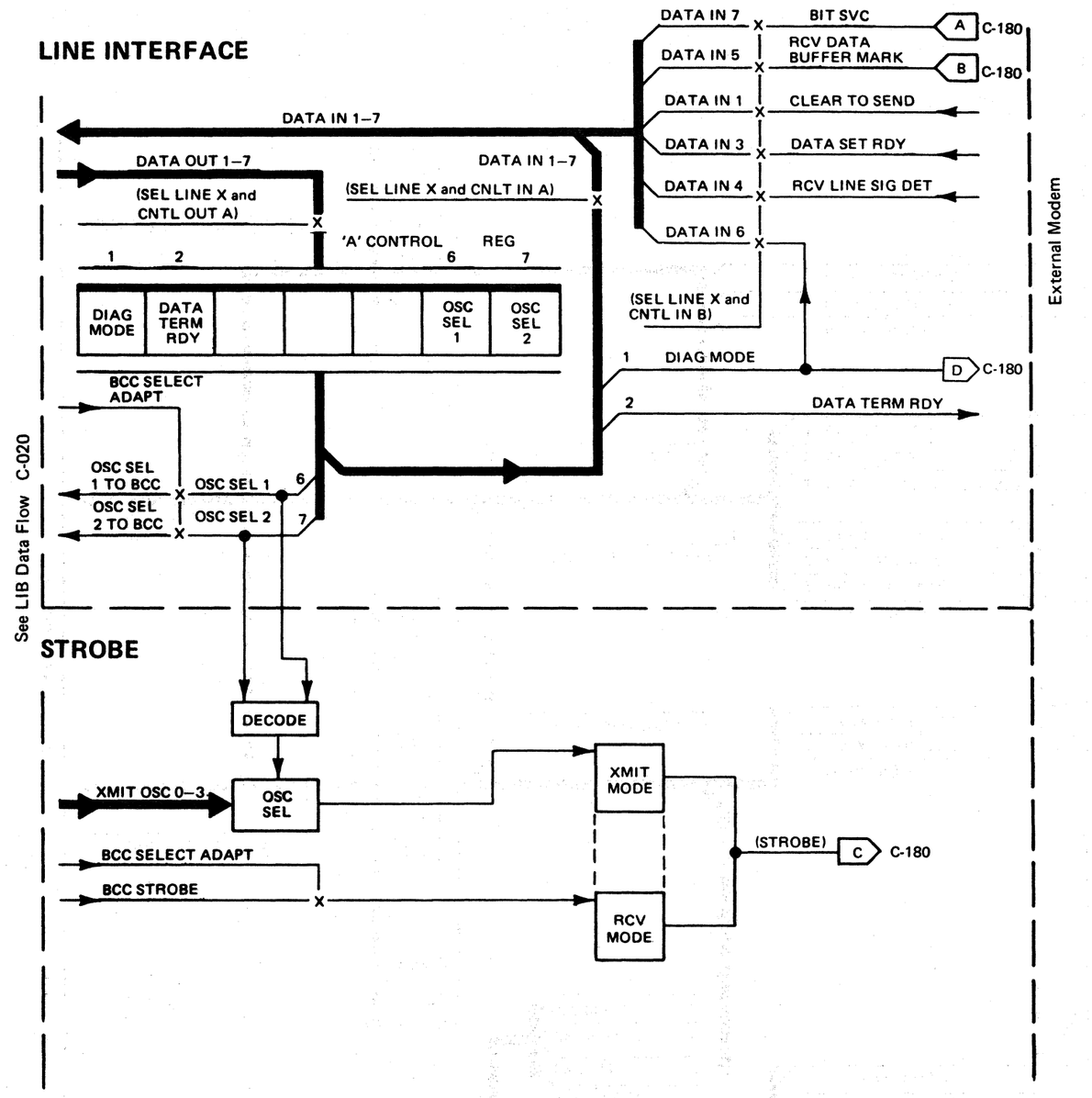
1. The communication line adapter status, RCV buffer status, and 'bit service trigger' status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the communication adapter during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the communication line adapter, and 'xmit data' bits to the 'send data buffer' during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner during a CNTL IN C.

Strobe

1. When Xmit Mode is not set, receive mode is assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator.



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*



LINE SET LS1—START/STOP (PART 2 OF 2)

Bit Service

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

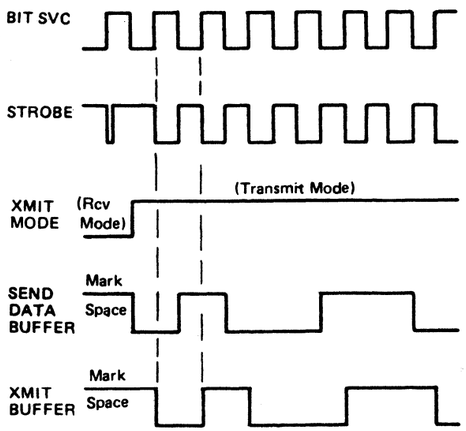
1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

Transmit

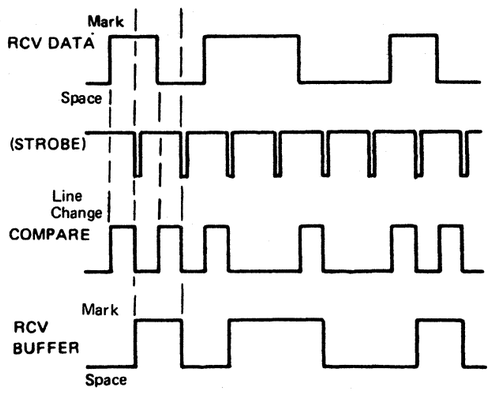
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the EIA level of the communication line.

Receive

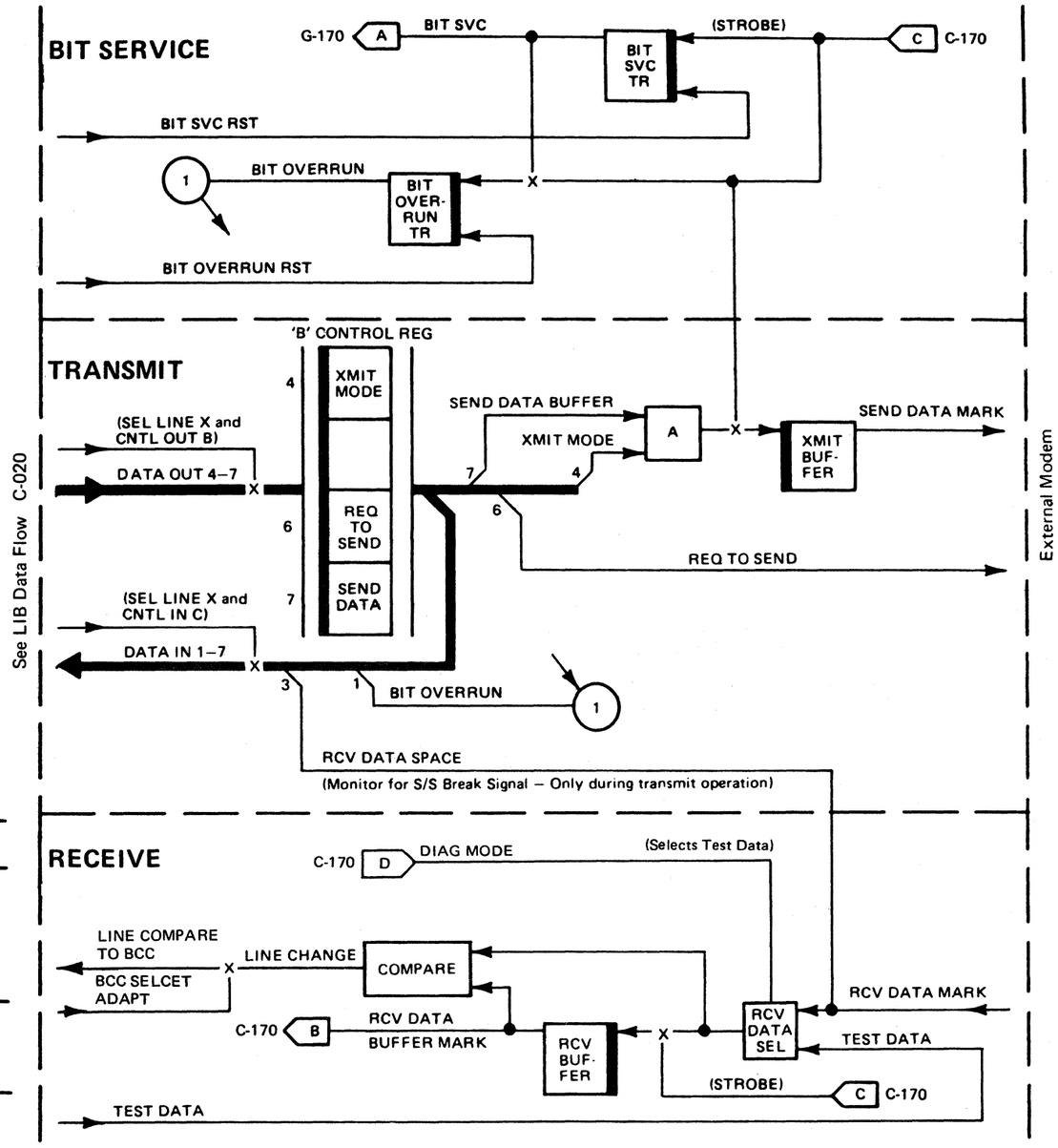
1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*



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LINE SET LS1—LOCAL ATTACHMENT INTERFACE

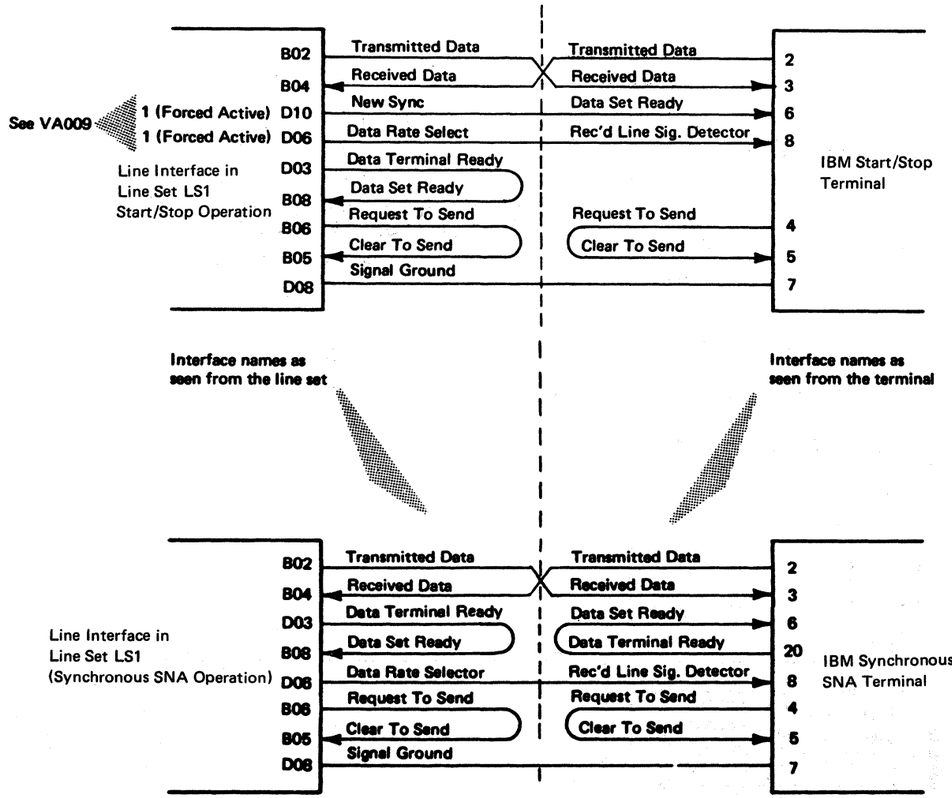
Line Set LS1 (Start/Stop Terminals)

Data flow for local attachment start/stop operation is the same as EIA start/stop operation.

Line Set LS1 (Synchronous SNA Terminals)

Data flow for local attachment synchronous operation is the same as EIA synchronous operation.

The control program must activate Data Rate Select since this signal drives the terminal's Received Line Signal Detector circuit.



LINE SET LS1–SYNCHRONOUS (PART 1 OF 2)

Line Interface

The line interface is a buffer for status and data, transferred between the scanner and the communication adapter (external modem, or the local attachment).

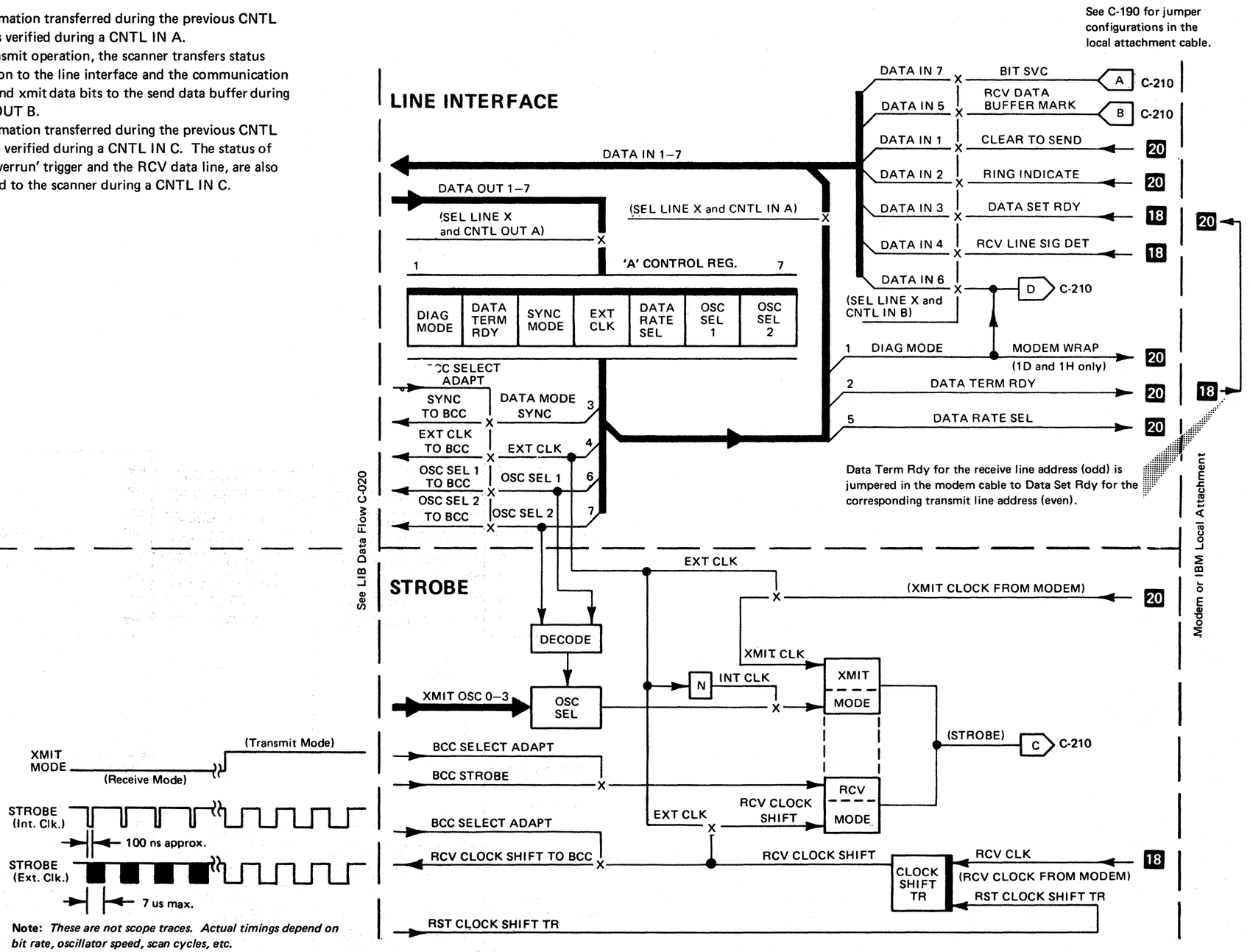
Line Set LS1 (Duplex with an External Modem)

This line set consists of a transmit line interface on an even address and a receive line interface on an odd address. Hardware is present in this line set for the transmit address where the modem interface lines are marked with 20 . Hardware is present in this line set for the receive address where the modem interface lines are marked with 18 .

1. The communication line adapter status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the communication adapter, during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A, is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the communication adapter, and xmit data bits to the send data buffer during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B, is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line, are also transferred to the scanner during a CNTL IN C.

Strobe

1. When Xmit Mode and Ext Clk are not set, receive mode and internal clock are assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Ext Clk is set, 'strobe' pulses are obtained from the modem clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator (internal clocking) or from the modem clock (external clocking).



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*

LINE SET LS1—SYNCHRONOUS (PART 2 OF 2)

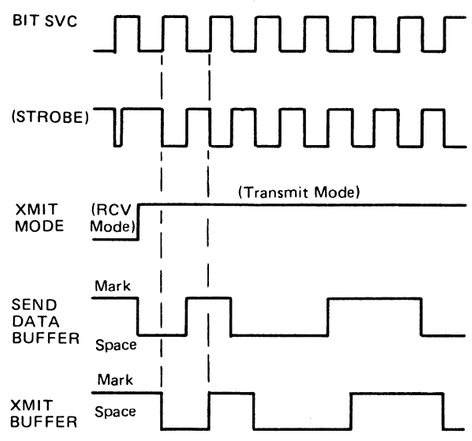
Bit Service

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

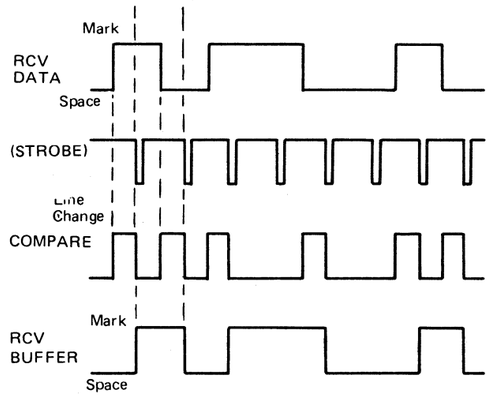
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, New Sync, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the EIA level of the communication line.



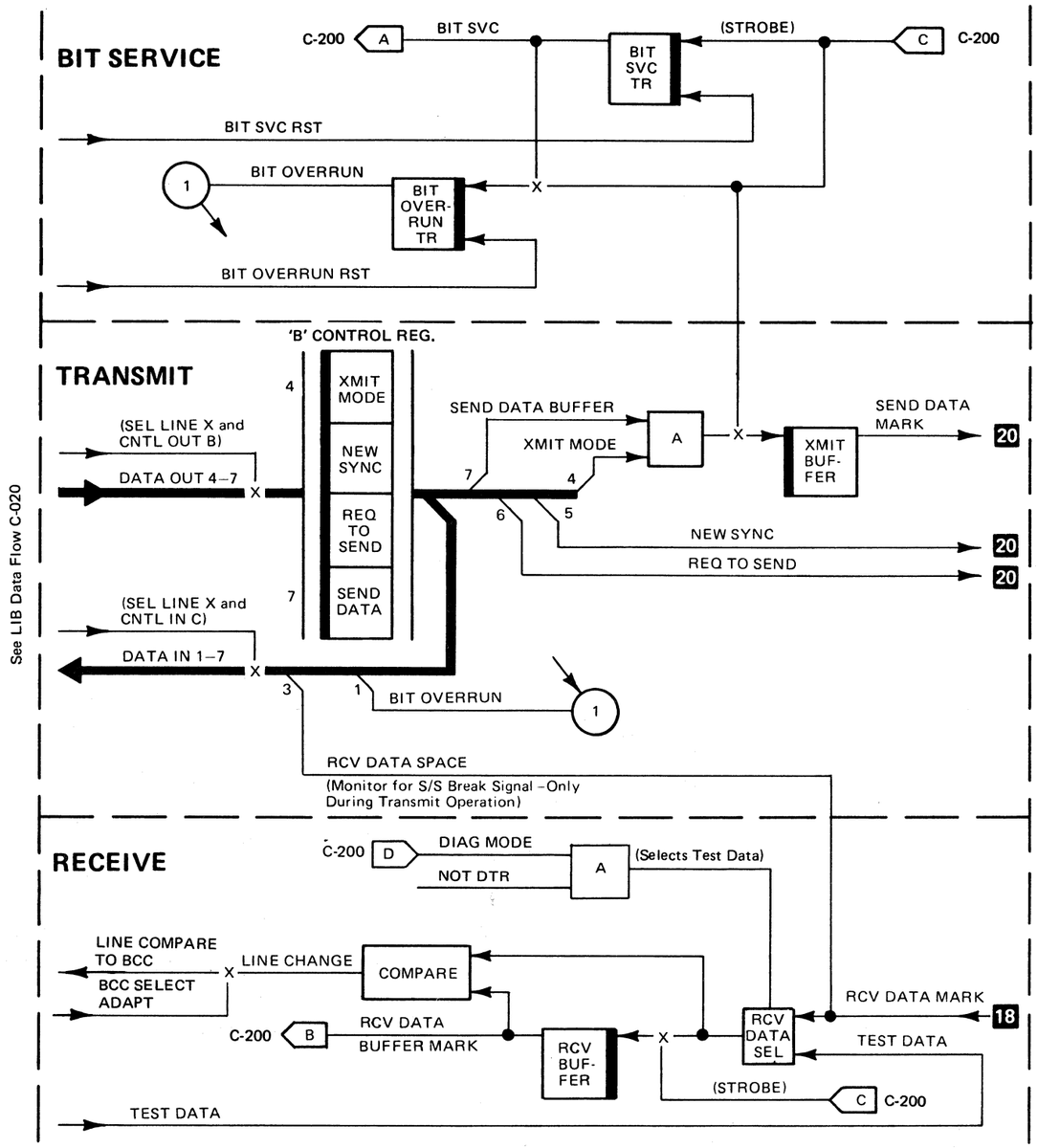
Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*

RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*



LINE SET LS2 HALF-DUPLEX/DUPLEX (CCITT V.35 INTERFACE) (PART 1 OF 2)

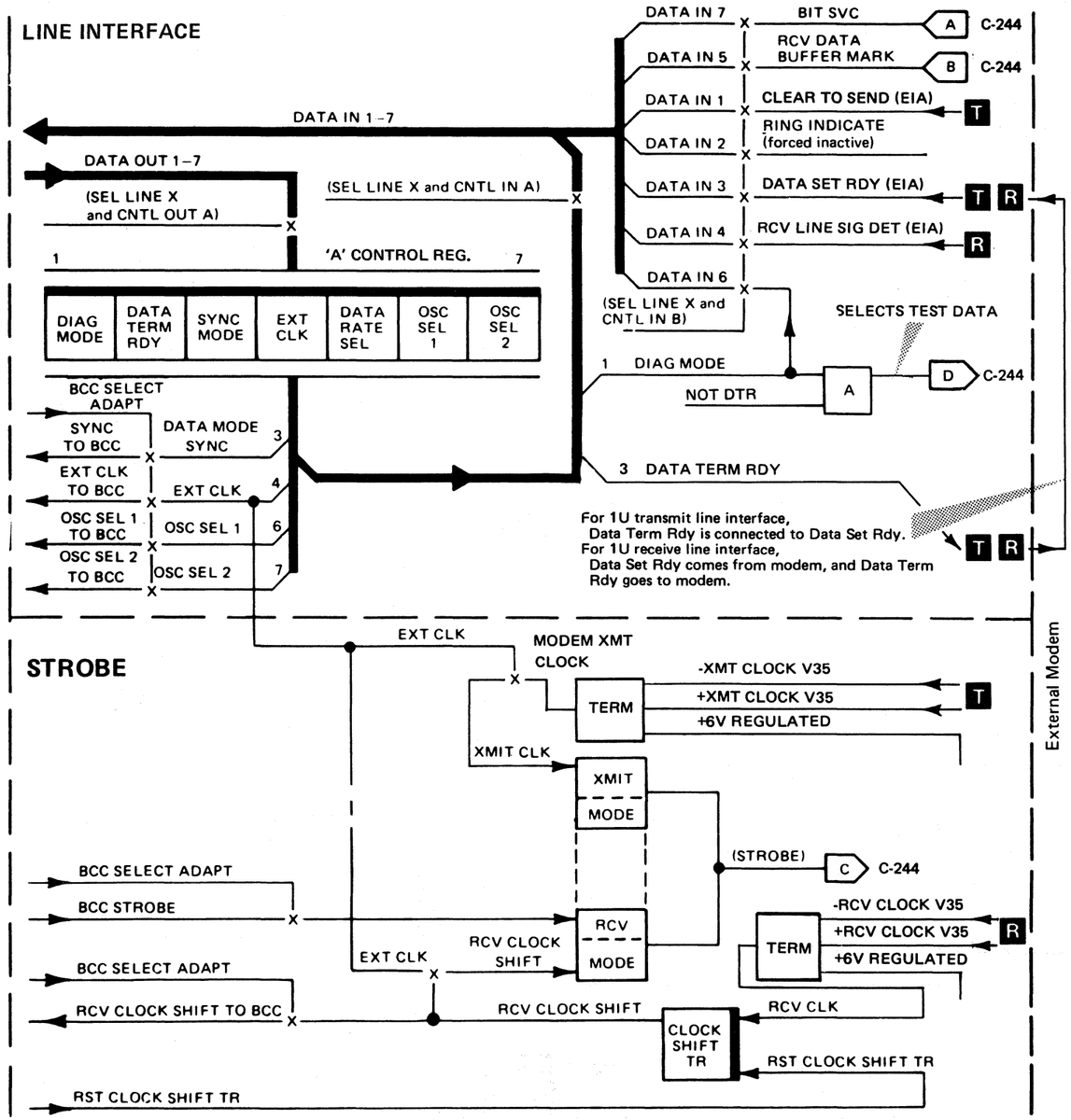
For duplex operation, both line interfaces of the LS2 line set are cabled to a single external modem. Partitions must have adjacent addresses. (0 and 2, 4 and 6, 8 and A, C and E). The transmit address must be the low order address (0, 4, 8, or C) and the receive address must be the high order address (2, 6, A or E).

The hardware for transmit and hardware for receive are identical and for this illustration they are shown combined, but actually they are independent of each other, both in hardware and operation. Hardware used for transmit operations is marked with T, and hardware used for receive operations is marked with R. See VA014 for how the modem signal lines are connected to the line-interfaces.

Line Interface

The line interface is a buffer for status and data, transferred between the scanner and the modem.

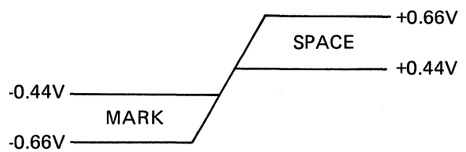
1. The modem status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL in B.
2. The scanner transfers status information to the line interface during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and transmits a data bit to the 'send data buffer' during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner during a CNTL IN C. (The type 2 scanner ignores 'bit overrun' and holds 'bit overrun reset' on solid.)



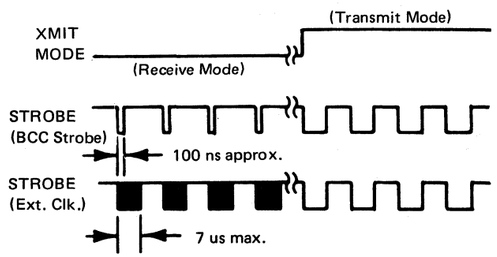
Strobe

1. If the receive clock shift is not received from the modem when in receive mode, the backup 'strobe' pulses are obtained from the 'BCC strobe' pulses (see C-060).
2. During receive mode, when Ext Clk is set, 'strobe' pulses are obtained from the modem clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the modem clock (external clocking).

The modem clock pulses (Xmt clock and RCV clock) are received at the CCITT V35 levels. The range of levels is as follows:



These levels *are differential* voltage levels measured between each side of the balanced line.



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*

LINE SET LS2 – DUPLEX (CCIT V.35 INTERFACE (PART 2 OF 2)

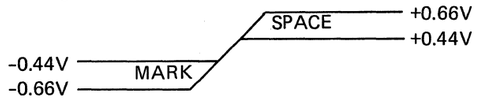
Bit Service

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

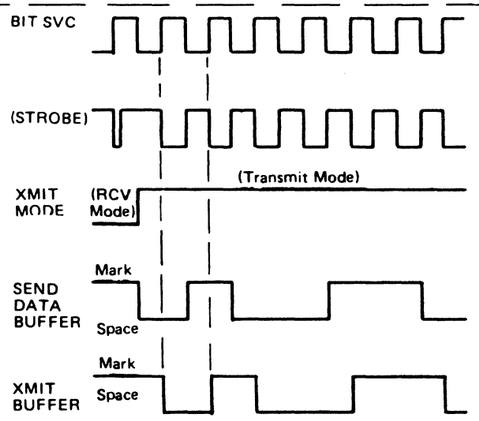
1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

Transmit

1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, New Sync, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the CCITT V.35 level of the communication line. The range of levels is as follows:



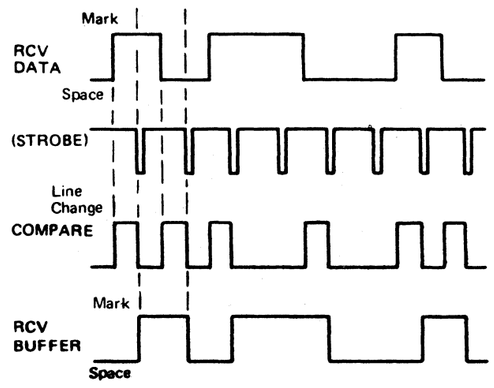
These levels are *differential* voltage levels measured between each side of the balanced time.



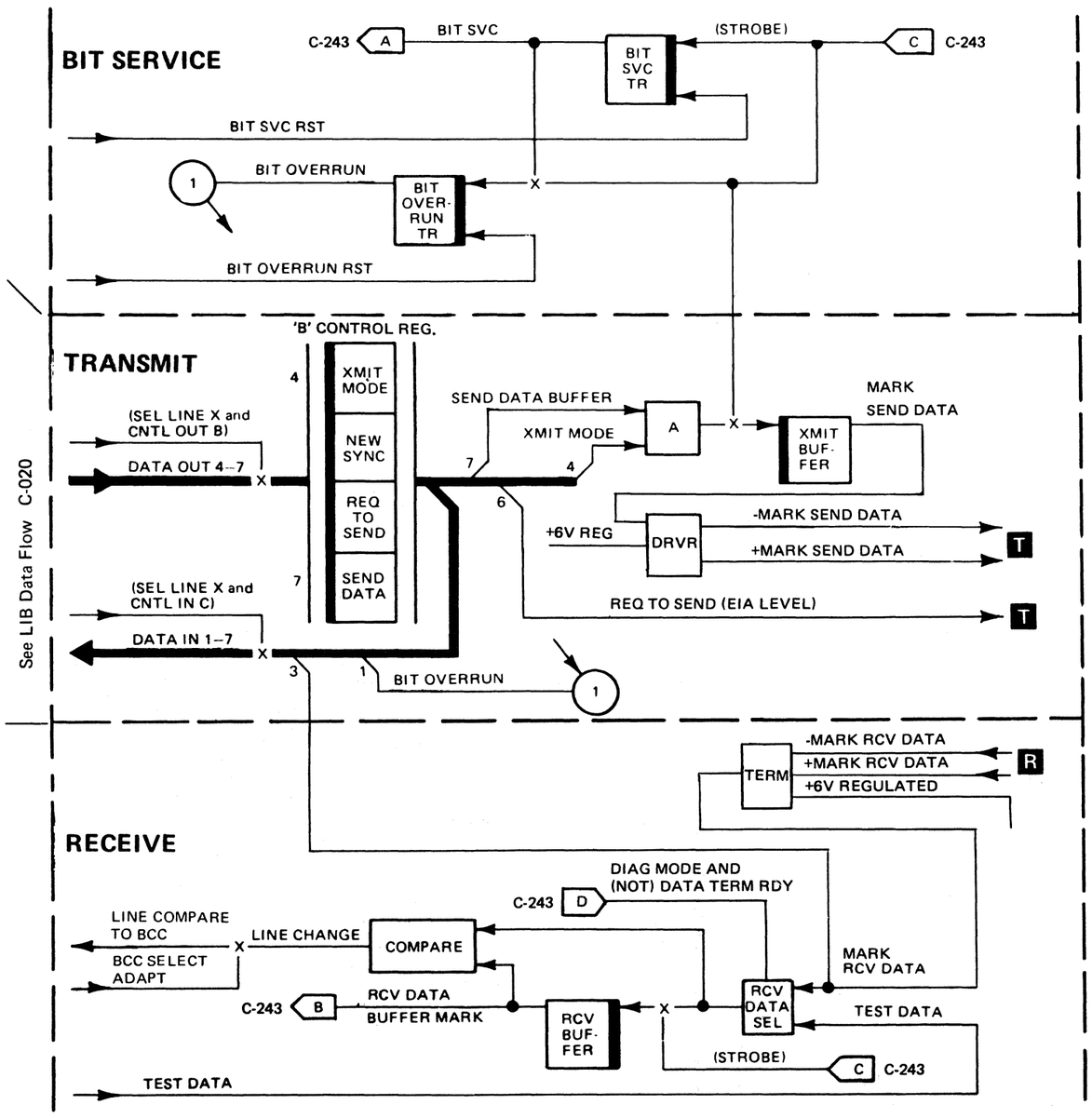
Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*

Receive

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit. The received data is at the CCITT V.35 levels as described above.



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*



LINE SET LS3 – DIGITAL SYNCHRONOUS HIGH SPEED DUPLEX EXTERNAL MODEM (PART 1 OF 2)

For digital duplex operation, both line interfaces of the LS3 line set are cabled to a single external modem. Partitions must have adjacent addresses (0 and 2, 4 and 6, 8 and A, C and E). The transmit address must be the low order address (0, 4, 8 or C) and the receive address must be the high order address (2, 6, A or E).

The hardware for transmit and hardware for receive are identical, and for this illustration they are shown combined, but actually they are independent of each other, both in hardware and operation. Hardware used for transmit operations is marked with **T**, and hardware used for receive operations is marked with **R**.

See VA013 for how the modem signal lines are connected to the line interfaces.

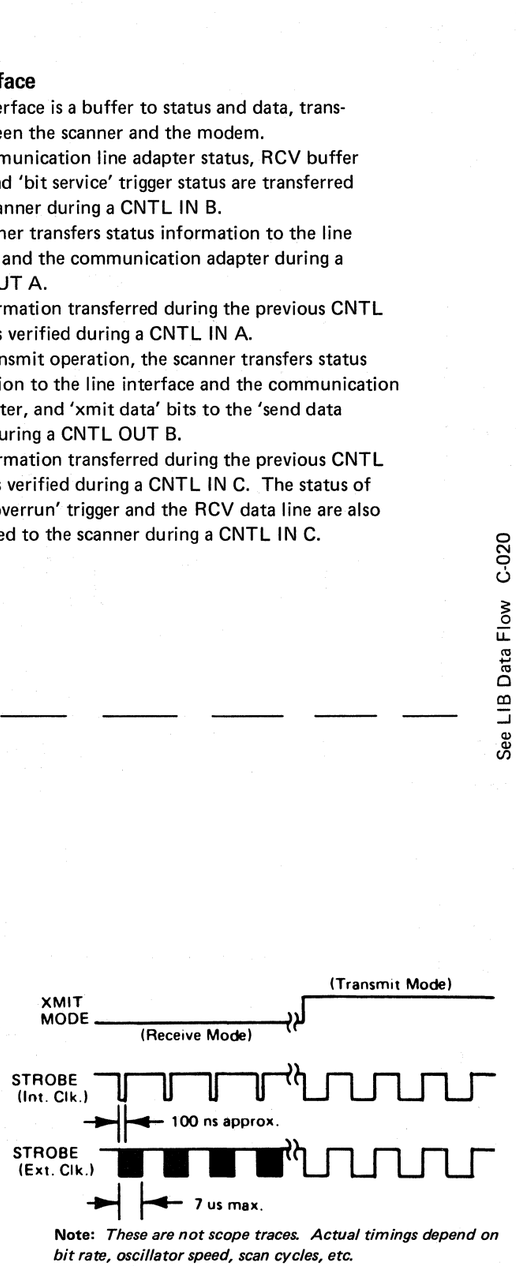
Line Interface

The line interface is a buffer to status and data, transferred between the scanner and the modem.

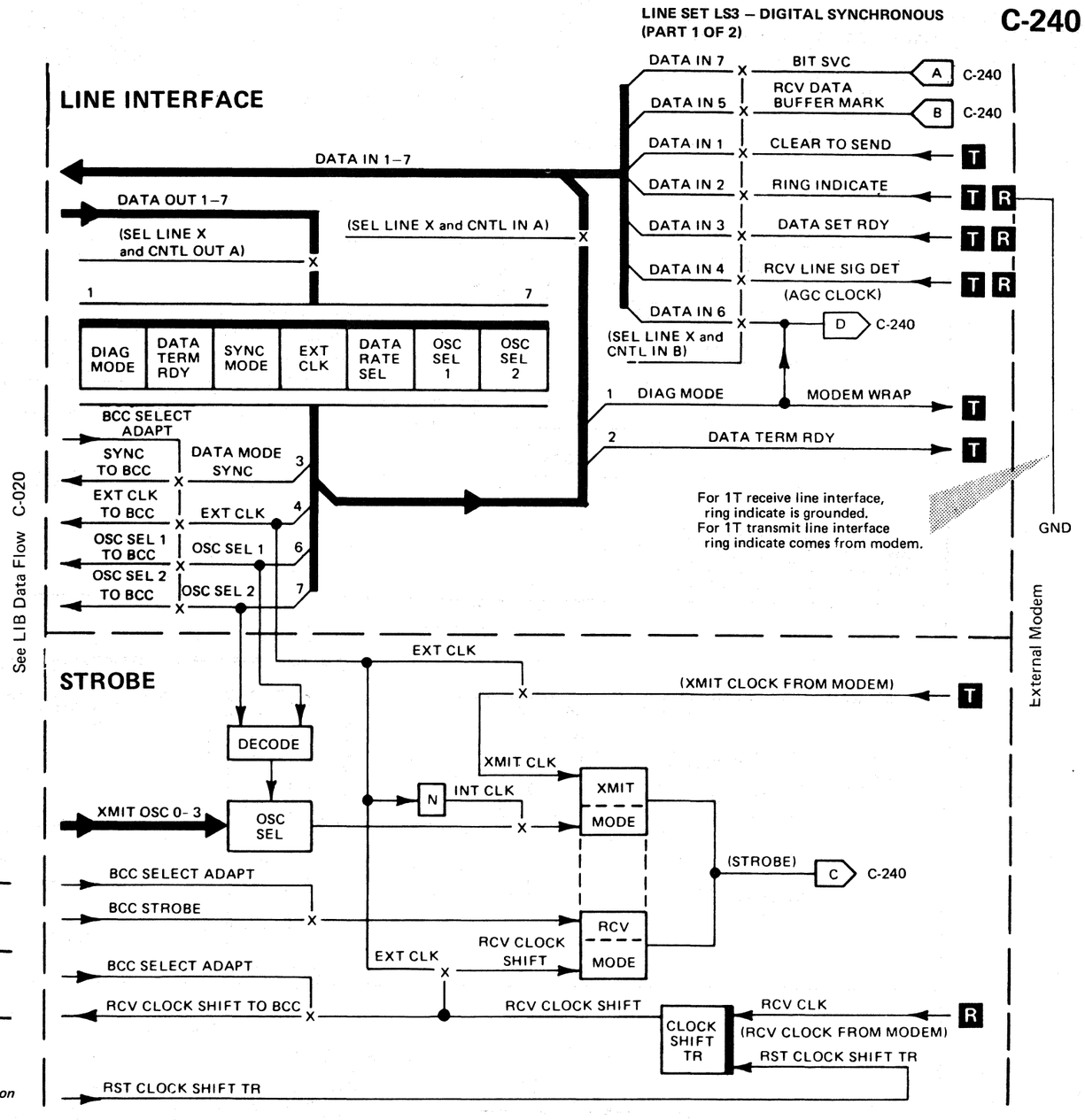
1. The communication line adapter status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the communication adapter during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the communication line adapter, and 'xmit data' bits to the 'send data buffer' during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner during a CNTL IN C.

Strobe

1. When Xmit Mode and Ext Clk are not set, receive mode and internal clock are assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Ext Clk is set, 'strobe' pulses are obtained from the modem clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator (internal clocking) or from the modem clock (external clocking).



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*



LINE SET LS3 – DIGITAL SYNCHRONOUS HIGH SPEED DUPLEX EXTERNAL MODEM (PART 2 OF 2)

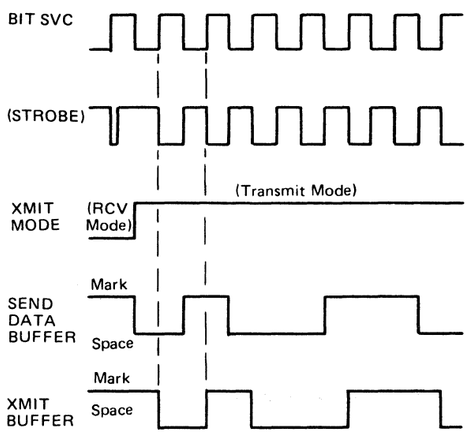
Bit Service

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowlegement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

Transmit

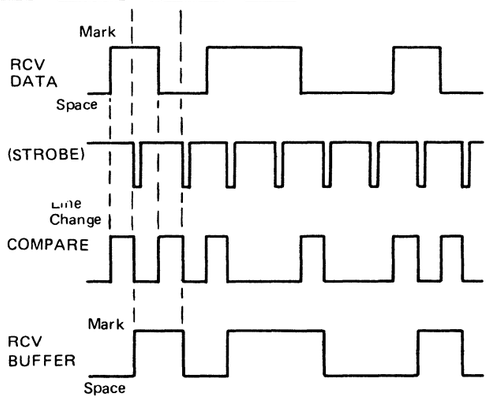
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, New Sync, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the Digital level of the communication line.



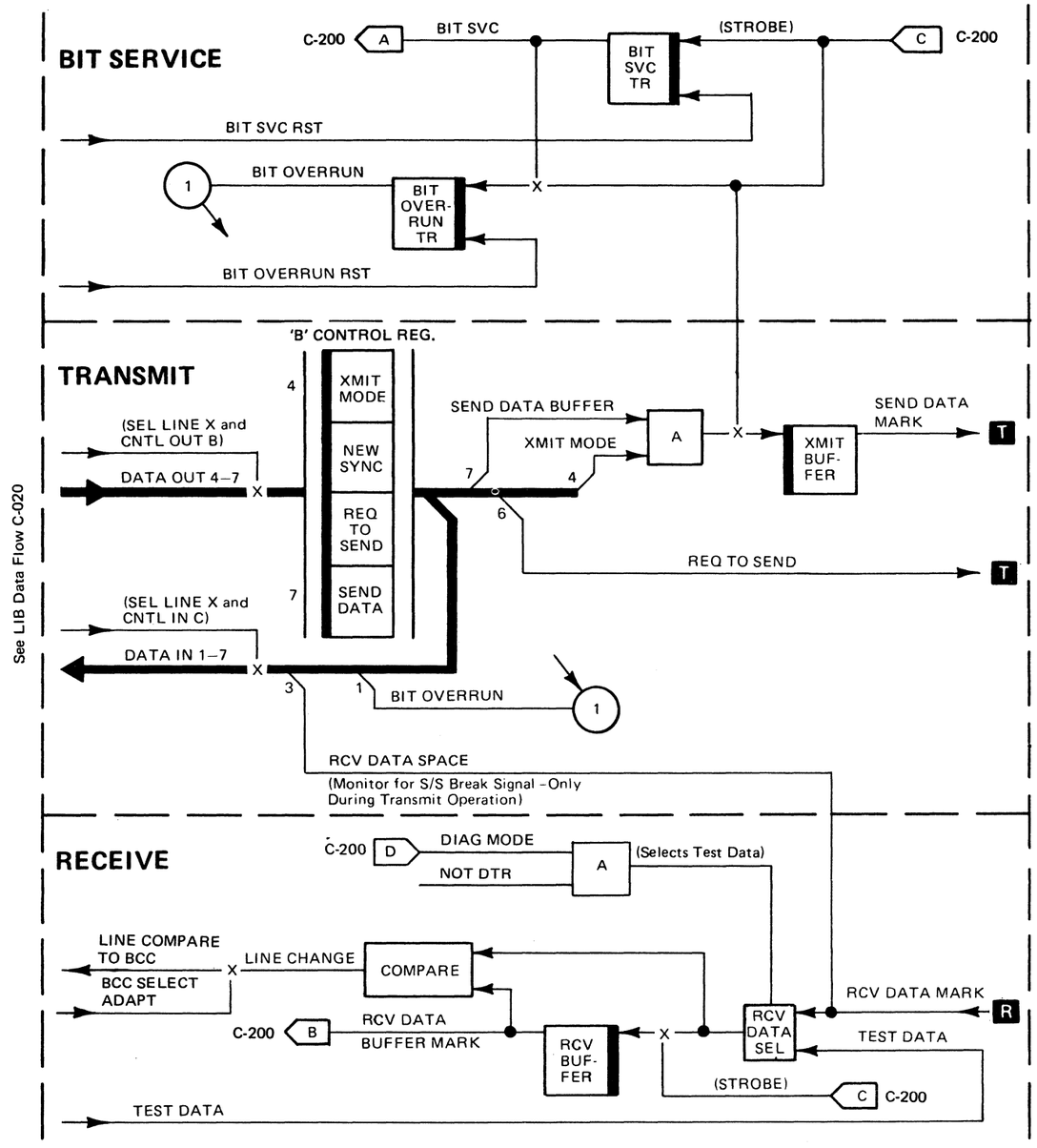
Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*

Receive

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*



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LINE SET LS4 – AUTOCALL INTERFACE

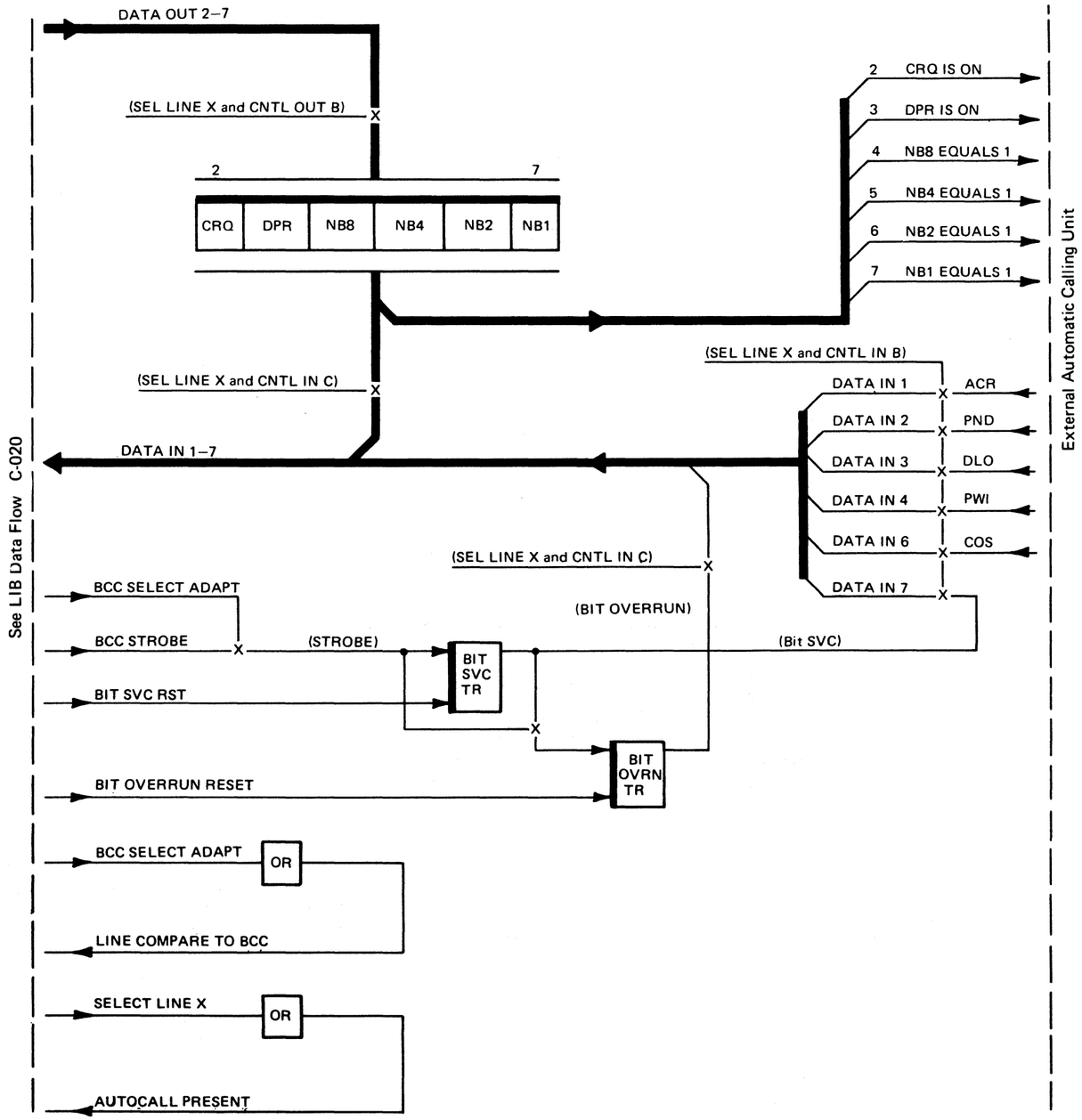
The Auto Call interface is a buffer for status and data transferred between the scanner and the external Automatic Calling Unit (ACU).

1. ACU status is transferred to the scanner during a CNTL IN B.
2. The scanner transfers information to the ACU during a CNTL OUT B (after a 'bit service' request).
3. The information, transferred during the previous CNTL OUT B, is verified during a CNTL IN C.

Bit Service

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the Auto Call interface. 'Bit service' is the Auto Call interface request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request .

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger. 'Strobe' pulses are obtained from the 'BCC strobe' pulses (derived from internal oscillator 0).
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.



LINE SET LS5 – HIGH SPEED DUPLEX (CCITT V.35 INTERFACE) (PART 1 OF 2)

The hardware for transmit and hardware for receive are identical and for this illustration they are shown combined, but actually they are independent of each other, both in hardware and operation. Hardware used for transmit operations is marked with **T**, and hardware used for receive operations is marked with **R**. See VA016 for how the local attachment signal lines are connected to the line-interfaces.

Line Interface

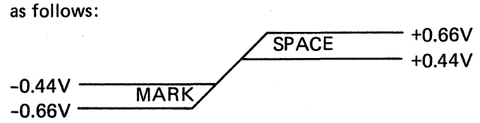
The line interface is a buffer for status and data, transferred between the scanner and the modem.

1. The modem status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and transmits a data bit to the 'send data buffer' during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner during a CNTL IN C. (The type 2 scanner ignores 'bit overrun' and holds 'bit overrun reset' on solid.)

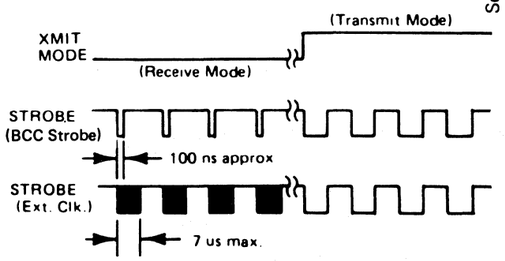
Strobe

1. If the receive clock shift is not received from the V.35 local oscillator, when in receive mode, the backup 'strobe' pulses are obtained from the 'BCC strobe' pulses (see C-060).
2. During receive mode, when Ext Clk is set, 'strobe' pulses are obtained from the V.35 local oscillator, (through the 'clock shift' trigger).
3. When XMIT Mode is set, 'strobe' pulses are obtained from the V.35 XMIT clock (external clocking).

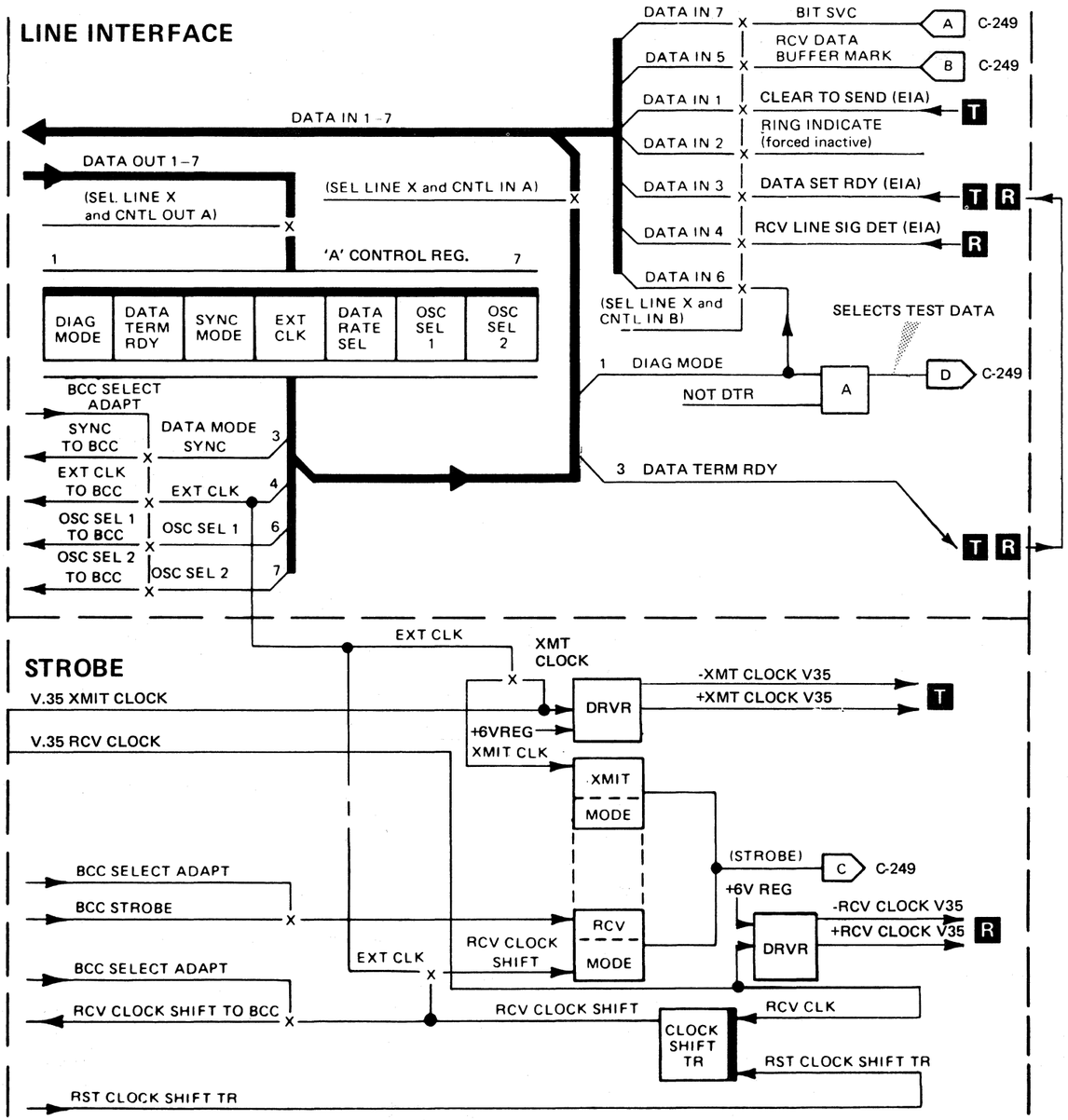
The clock pulses for a distant terminal or 3705-80 are transmitted at CCITT V35 levels. The range of levels is as follows:



These levels are *differential* voltage levels measured between each side of the balanced line.



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*



LINE SET LS5 — HIGH SPEED DUPLEX (CCITT V.35 INTERFACE) (PART 2 OF 2)

Bit Service

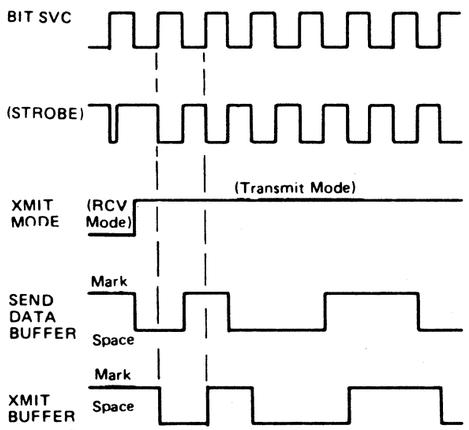
'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

Transmit

1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, New Sync, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the CCITT V.35 level of the communication line. The range of levels is as follows:

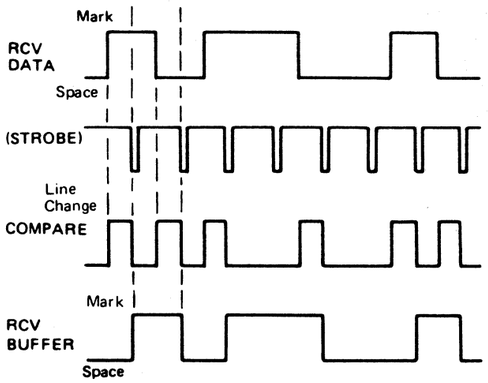
These levels are *differential* voltage levels measured between each side of the balanced time.



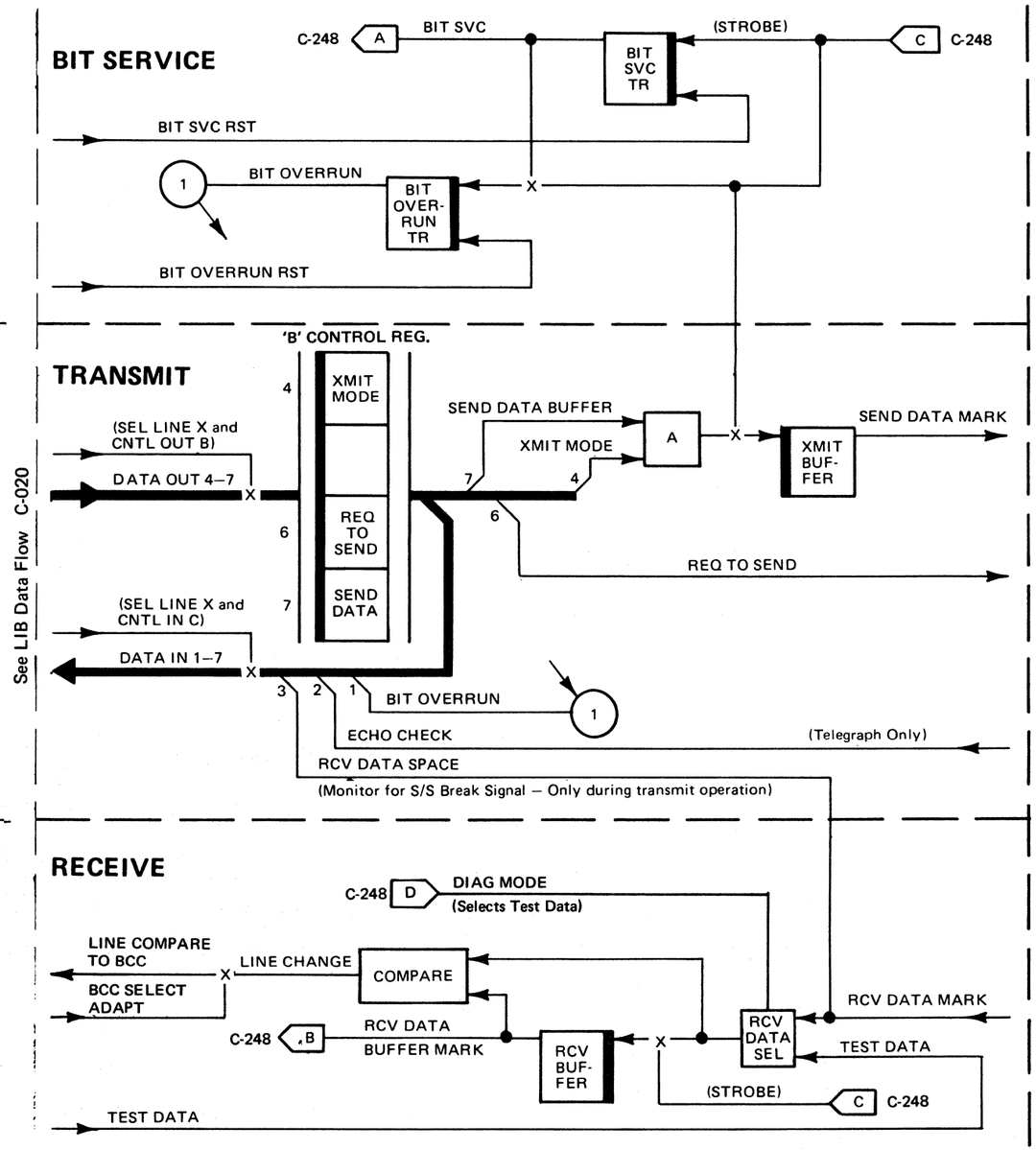
Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*

Receive

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit. The received data is at the CCITT V.35 levels as described above.



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*



LINE SET LS8 OR LS9 – DUPLEX OR HALF-DUPLEX – NONSWITCHED (CCITT X.21 INTERFACE) (PART 1 OF 2)

Line Interface

The line interface is a buffer for status and data, transferred between the scanner and the communication adapter (data circuit-terminating equipment-DCE).

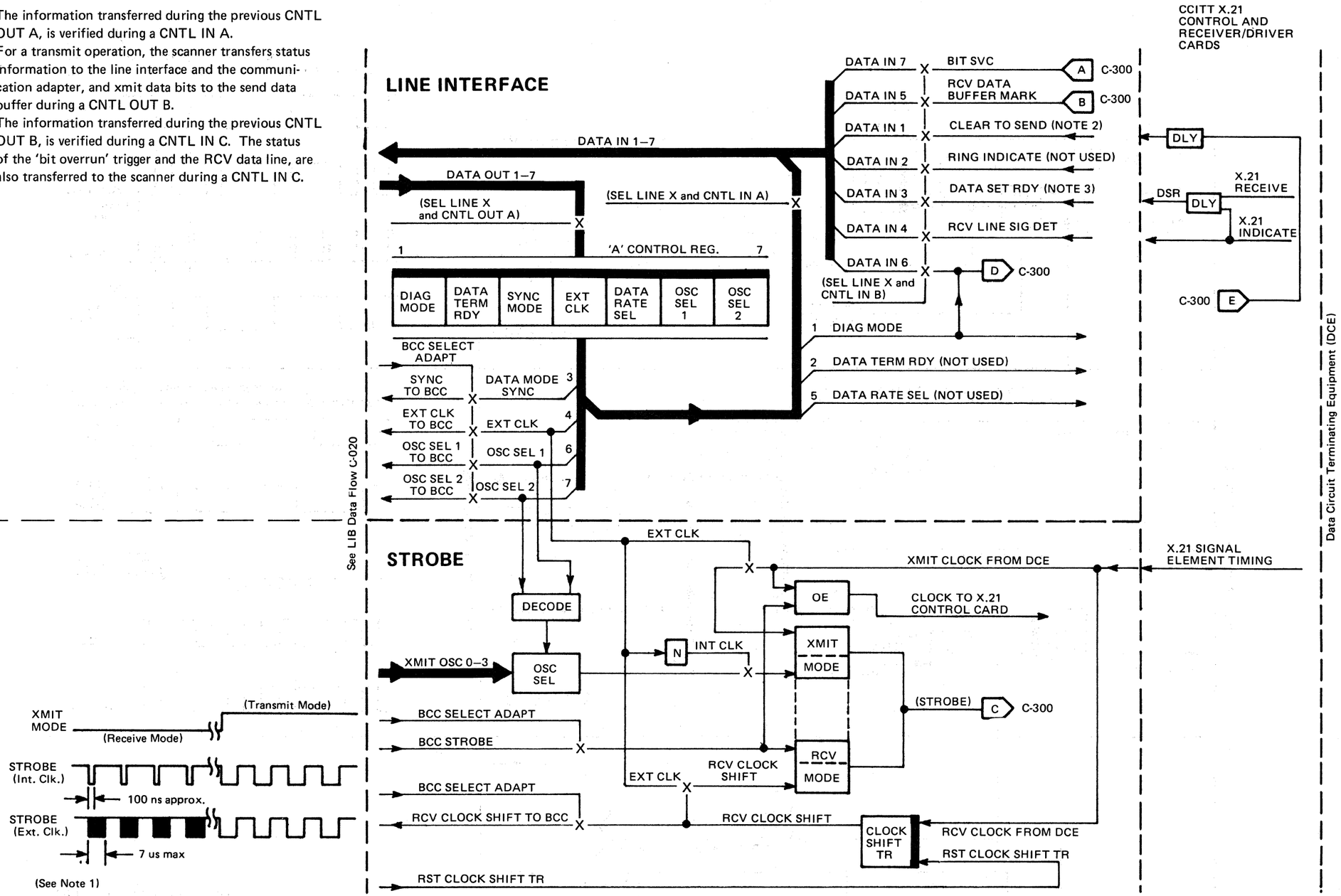
1. The communication line adapter status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the communication adapter, during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A, is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the communication adapter, and xmit data bits to the send data buffer during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B, is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line, are also transferred to the scanner during a CNTL IN C.

Strobe

1. When Xmit Mode and Ext Clk are not set, receive mode and internal clock are assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Ext Clk is set, 'strobe' pulses are obtained from the DCE clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator (internal clocking) or from the DCE clock (external clocking).

Notes:

1. *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*
2. *Approximately 26 bit times after it is activated, CLEAR TO SEND becomes effective.*
3. *Approximately 17 bit times after RECEIVE drops to '0' and INDICATE turns OFF, DATA SET READY becomes inactive.*



LINE SET LS8 OR LS9 — DUPLEX OR HALF-DUPLEX — NONSWITCHED (CCITT X.21 INTERFACE) (PART 2 OF 2)

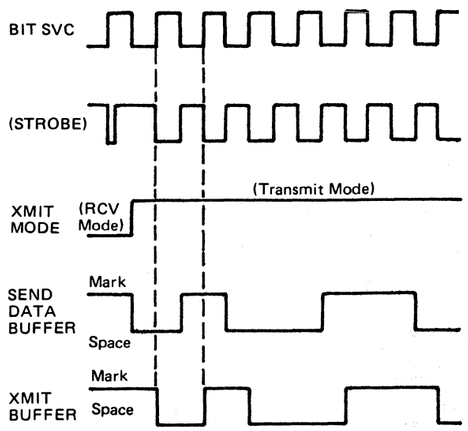
Bit Service

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

Transmit

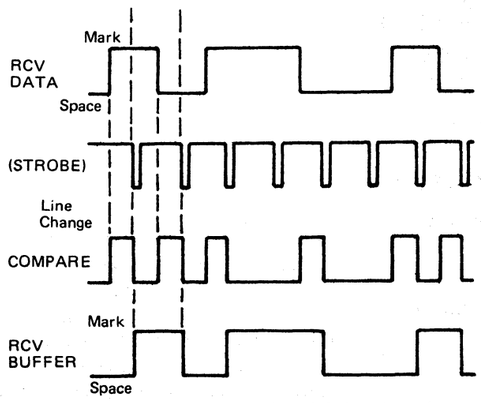
1. 'Bit service' is set by the negative going shift of the 'strobe ' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the CCITT level of the communication line.



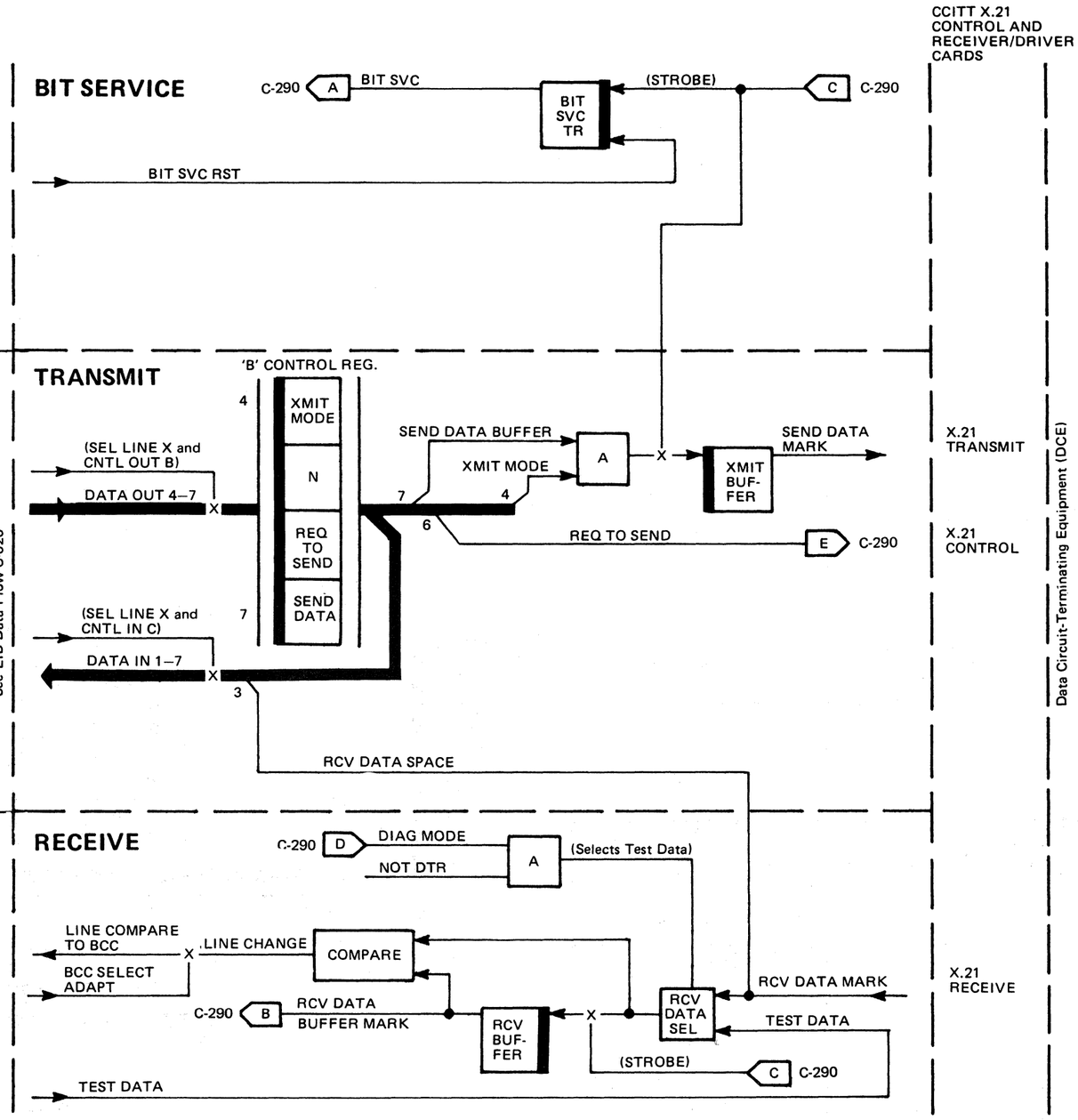
Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*

Receive

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*



LINE SET LS8 OR LS9 – DUPLEX – SWITCHED (CCITT X.21 INTERFACE) (PART 1 OF 3)

Line Interface

The line interface is a buffer for status and data, transferred between the scanner and the communication adapter (data circuit-terminating equipment-DCE).

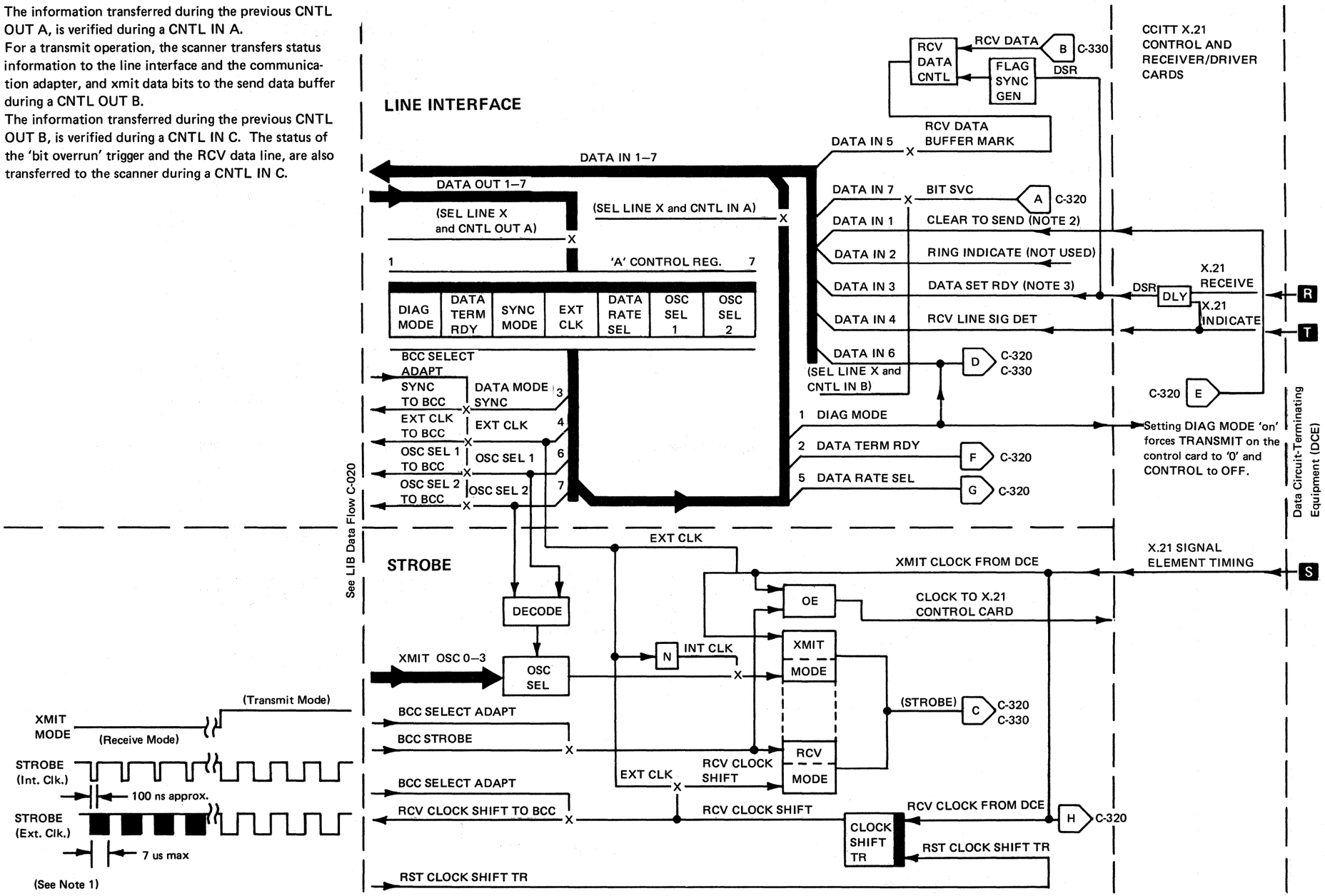
1. The communication line adapter status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the communication adapter, during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A, is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the communication adapter, and xmit data bits to the send data buffer during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B, is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line, are also transferred to the scanner during a CNTL IN C.

Strobe

1. When Xmit Mode and Ext Clk are not set, receive mode and internal clock are assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Ext Clk is set, 'strobe' pulses are obtained from the DCE clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator (internal clocking or from the DCE clock (external clocking).

Notes:

1. *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*
2. *With this line set, the NCP and basic machine timing use an internal clock (operating at 1/24 or less of the data rate) to delay a change in state of the CLEAR TO SEND line. The CLEAR TO SEND line changes state approximately 24 bit times after REQUEST TO SEND is activated.*
3. *Approximately 17 bit times after RECEIVE drops to '0' and INDICATE turns OFF, DATA SET READY becomes inactive.*



LINE SET LS8 OR LS9 – DUPLEX – SWITCHED (CCITT X'21 INTERFACE) (PART 2 OF 3)

Bit Service

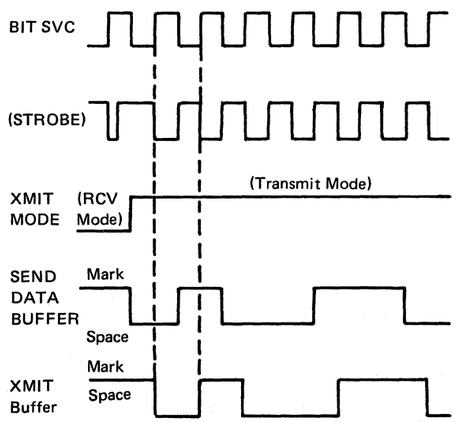
'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

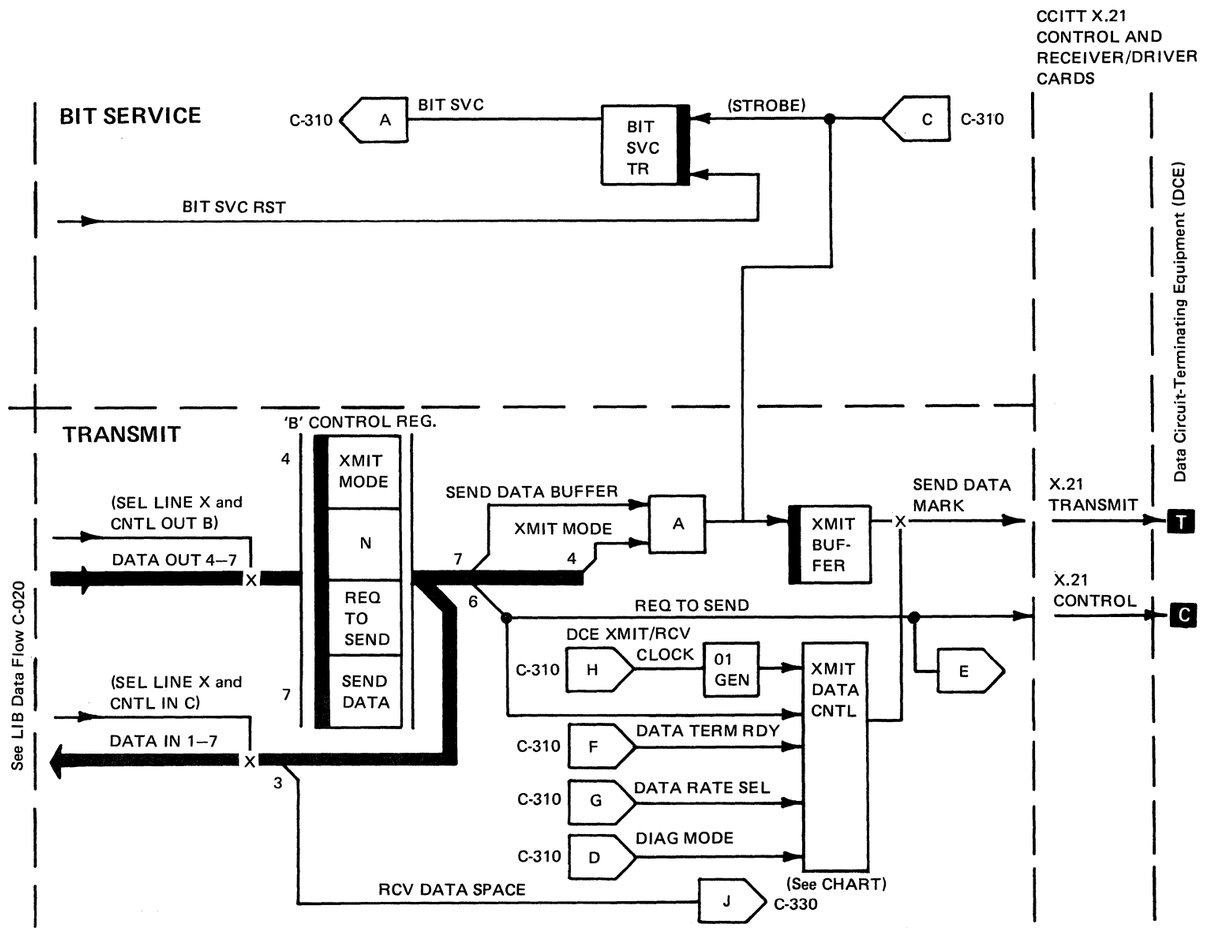
Transmit

1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the CCITT level of the communication line.

With an LS8 or LS9 line set in switched mode, the *on* or *off* state of several latches determines the status of the CCITT X.21 interface and the condition of the transmit and control signal lines. The following chart shows how to use the latch conditions to determine the status of the interface.



Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.*



Latch Conditions				Interface Signals		
Diag Mode	*Data Term Rdy*	*Data Rate Sel*	*Req To Send*	*Control (C)*	*Transmit (T)*	*CCITT X.21 Status*
Off	Off	**	Off	Off	0101...	DTE Controlled Not Ready
On	**	**	**	Off	0000...	DTE Uncontrolled Not Ready
Off	On	**	Off	Off	1111...	DTE Ready
Off	On	On	On	On	0000...	Call Request
Off	On	Off	On	On	*	Call Accepted or Data Transfer

*Data is transmitted from the Send Data Buffer.
**Of no concern

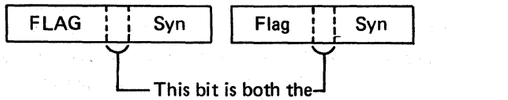
LINE SET LS8 OR LS9 – DUPLEX – SWITCHED (CCITT X.21 INTERFACE) (PART 3 OF 3)

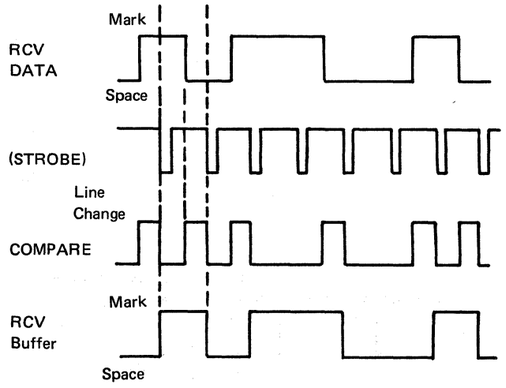
Receive

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.

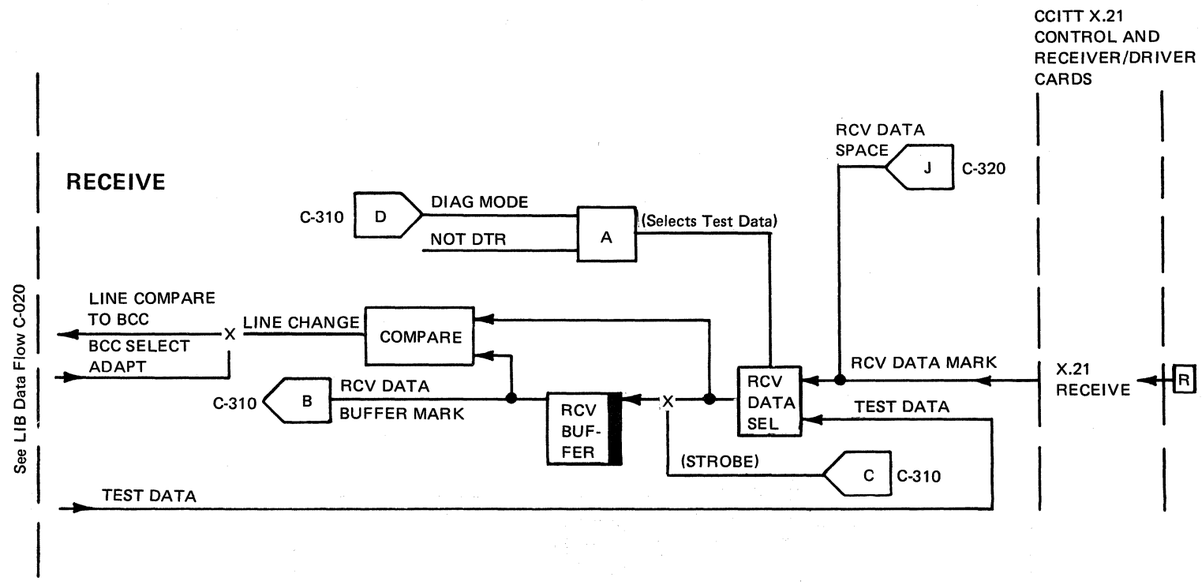
If a DCE not ready condition occurs (data set ready becomes inactive), a continuous pattern of fixed data appears on the addressed receive data lead. This fixed data pattern consists of an SDLC flag character and a USASCII syn character. If the scanner associated with the CCITT X.21 interface is in a monitor flag or monitor phase state, the continuously generated data pattern produces a level 2 interrupt with a modem check indication. This level 2 interrupt indicates to the controller that a DCE not ready condition exists. The data pattern that appears on the receive data lead is shown below.

X011111101101000X011111101101000. . . . . .

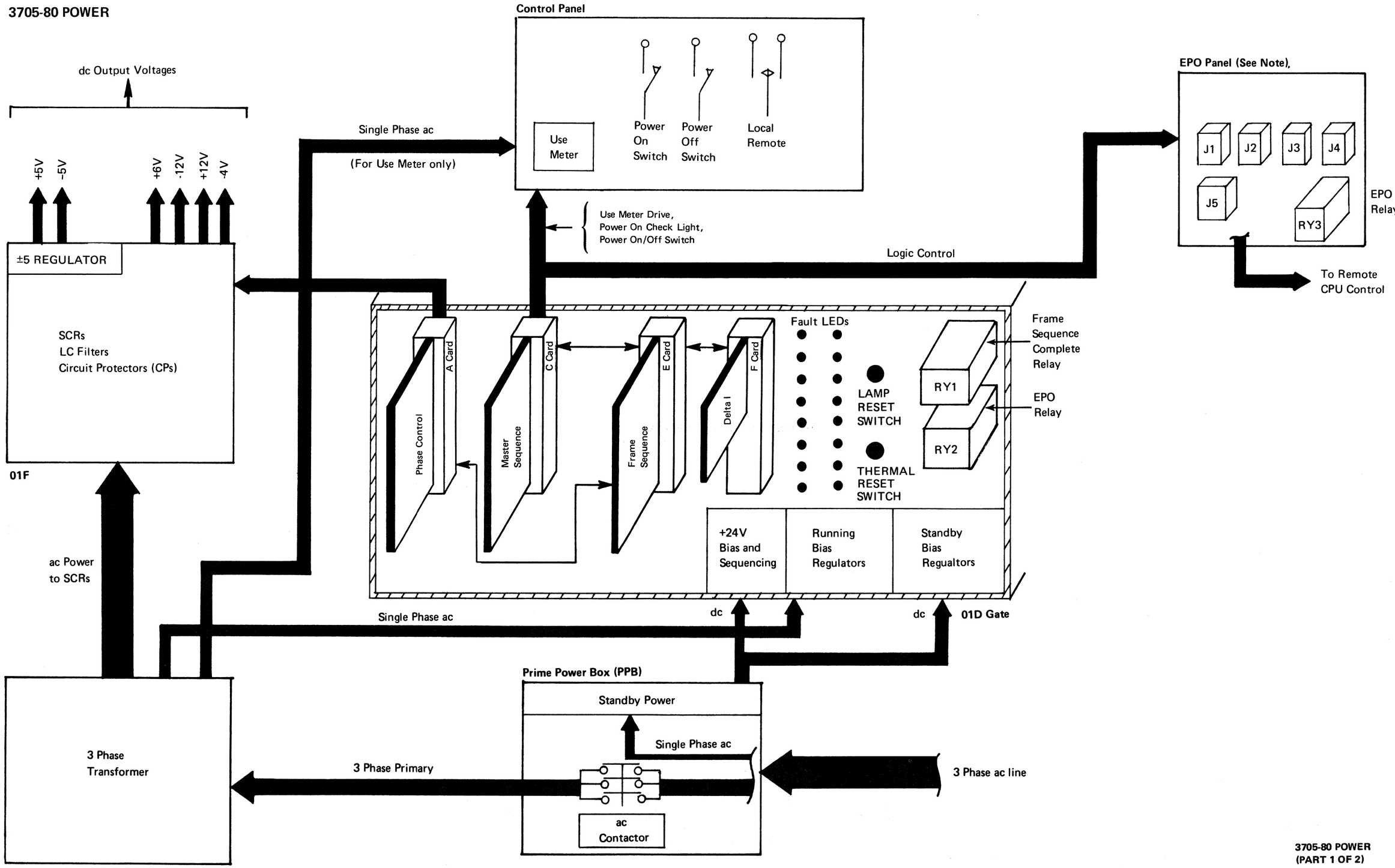




Note: *These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycle, etc.*



3705-80 POWER



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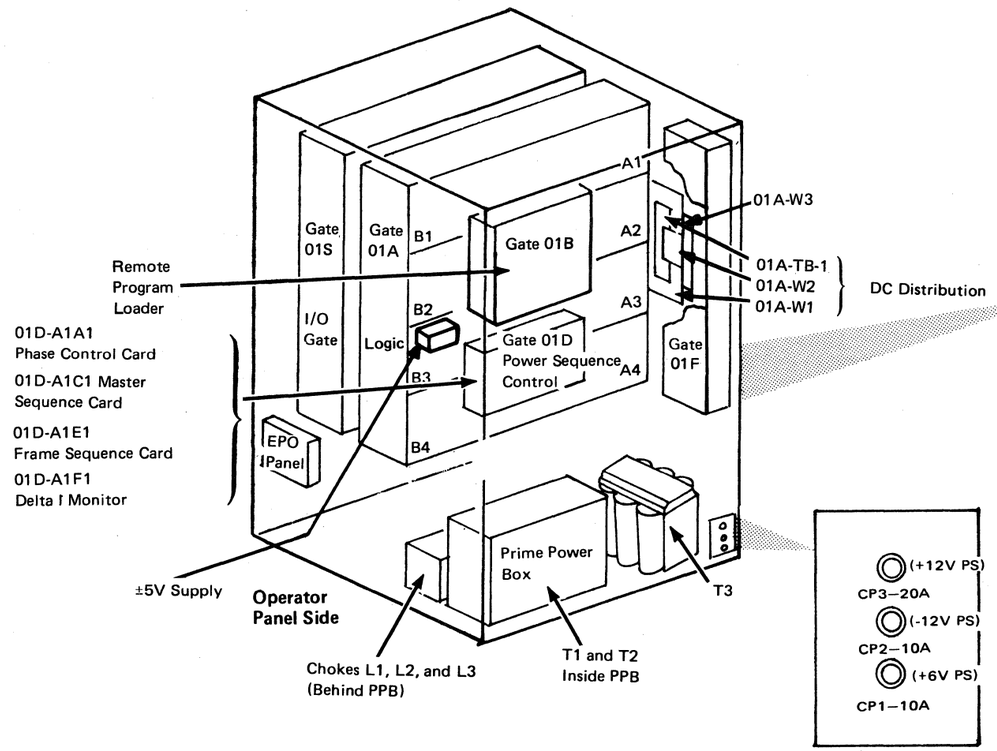
3705-80 POWER

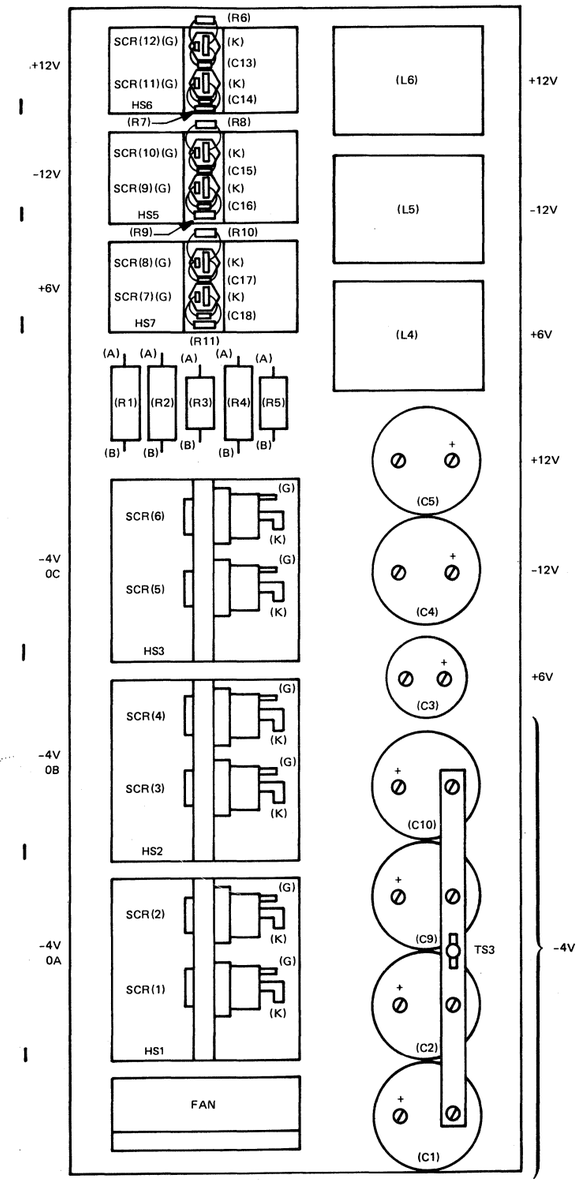
Component Locations

Unit	*Layout Reference*
Prime power box	YZ866 sheets 1, 2, 11
01D	YZ886 sheet 4
EPO panel	YZ886 sheet 8
RPL	YZ886 sheet 11
I/O Gate (01S)	YZ886 sheet 7
01F	YZ886 sheet 5

Note: *The Power Sequence Control gate 01D has no actual logic board. Pseudo board designator "A1" is used in card location references to maintain the format: frame, gate, board, card. For example: 01D-A1C1 for the Master Sequence Card.*



Gate 01F
Power Supply Mounting Asm.
-4V, +6V and ±12V



3705-80 POWER CHECK

Note: *Refer to Volume 1 (SY27-0208) of FETMM for 3705-80 Power Maintenance Analysis Procedures (MAPs).*

- The Power Check light turns on during a normal power-on sequence and turns off when the sequence has successfully completed.
- A power-off sequence occurs, and the Power Check light turns on for any of the following check conditions:
  1. Overvoltage on any logic voltage
  2. Undervoltage on any logic voltage
  3. Thermal sense on the logic *gates and power supplies.*
- If the power check resulted from conditions 1-2, reset the Power Check light by pressing the Power Off switch. Power can now be turned on.
- If the power check resulted from a thermal condition, reset the power check light by pressing the THERMAL RESET switch (located on the power sequence control gate-01D after the thermal contact that detected the thermal condition has cooled off and closed its contact (usually about a half hour). Power can now be turned on.

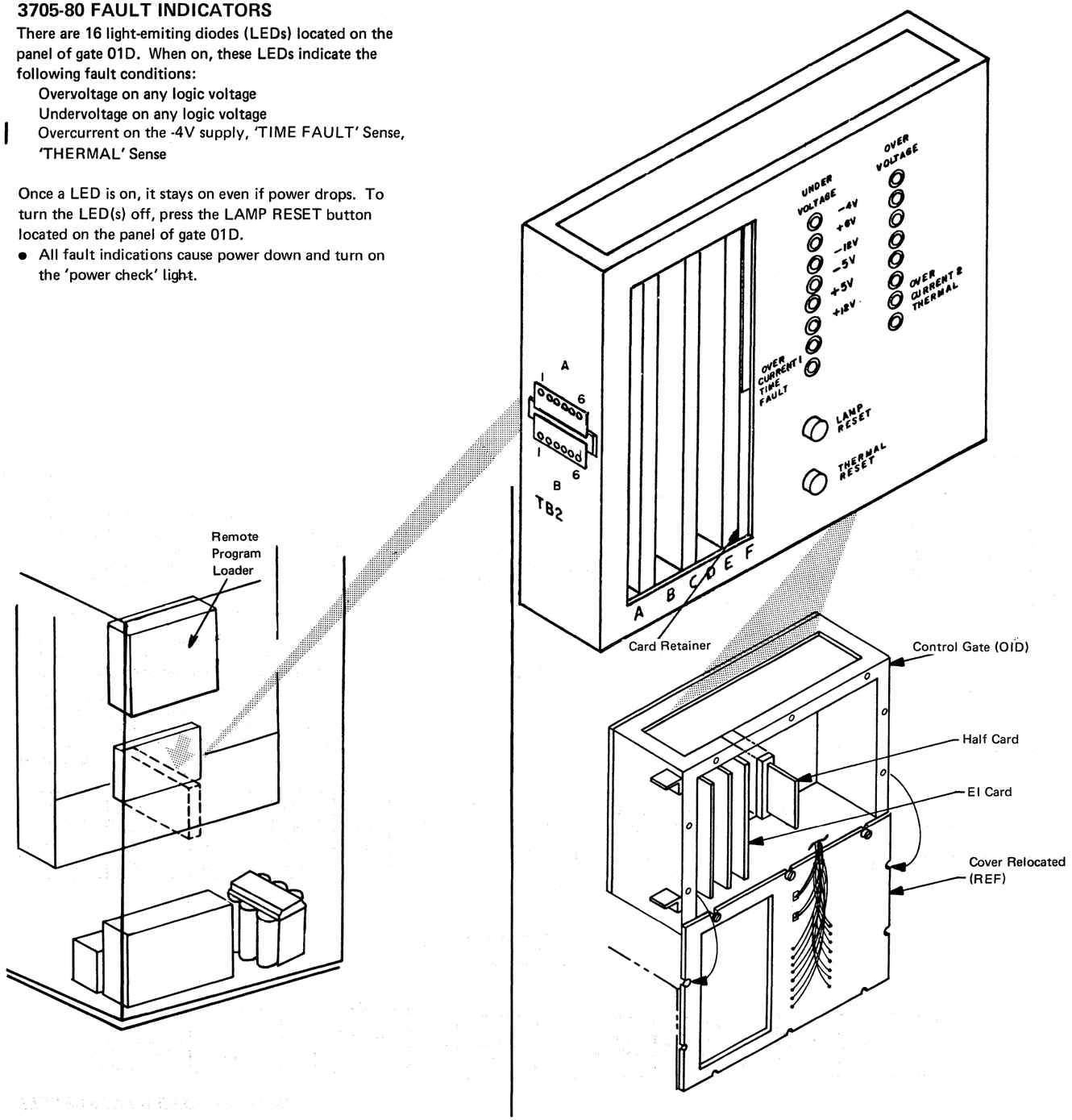
3705-80 FAULT INDICATORS

There are 16 light-emitting diodes (LEDs) located on the panel of gate 01D. When on, these LEDs indicate the following fault conditions:

Overvoltage on any logic voltage
Undervoltage on any logic voltage
Overcurrent on the -4V supply, 'TIME FAULT' Sense, 'THERMAL' Sense

Once a LED is on, it stays on even if power drops. To turn the LED(s) off, press the LAMP RESET button located on the panel of gate 01D.

- All fault indications cause power down and turn on the 'power check' light.



Power On Voltage Sequence:

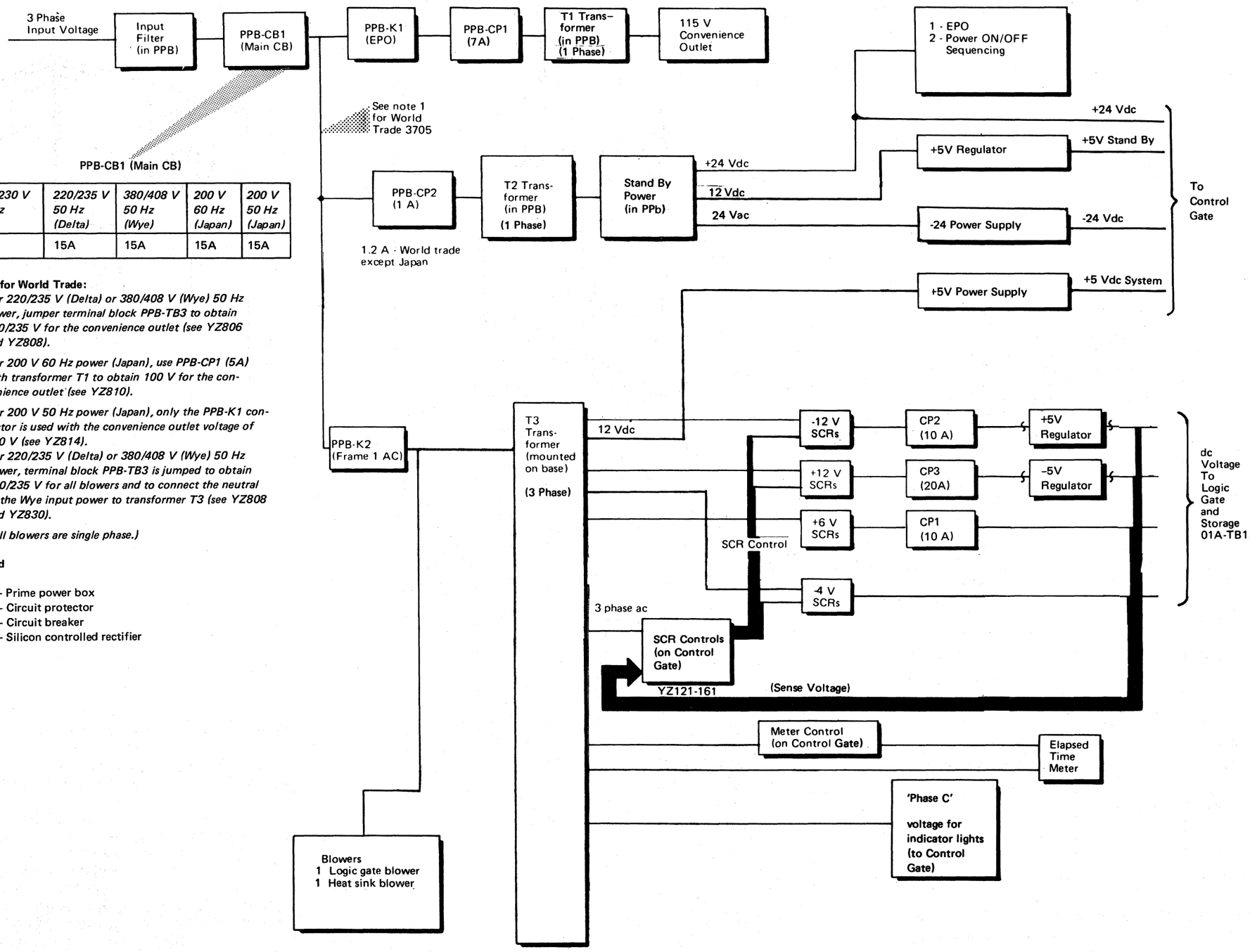
-4V ⟶ +6V and -12V ⟶ +12V and -5V ⟶ +5V

LED Fault Indication	*Causes Power Down*	*Duration of Fault Before Power Down*	*Approximate level at which LED turns on. UNDER-VOLTAGE, OVER-VOLTAGE, or OVER-CURRENT (-4V) causes power down*	*Action To Be Taken If Respective LED is On*
-4V OVERVOLTAGE	Yes	Immediate	-4.9V	See Note 1 and refer to power MAPs in Volume 1 (SY27-0208) of FETMM.
-5V OVERVOLTAGE	Yes	Immediate	-5.4V	
+5V OVERVOLTAGE	Yes	Immediate	+5.6V	
+6V OVERVOLTAGE	Yes	Immediate	+6.6V	
-12V OVERVOLTAGE	Yes	Immediate	-13.6V	
+12V OVERVOLTAGE	Yes	Immediate	+13.8V	
-4V UNDERVOLTAGE	Yes	Immediate	-3.5V	
-5V UNDERVOLTAGE	Yes	Immediate	-4.4V	
+5V UNDERVOLTAGE	Yes	Immediate	+2.8V	
+6V UNDERVOLTAGE	Yes	Immediate	+5.0V	
-12V UNDERVOLTAGE	Yes	Immediate	-9.6V	
+12V UNDERVOLTAGE	Yes	Immediate	+10.2V	
THERMAL	Yes	Immediate	+VTL Logic Level	See Note 3
OVERCURRENT 1 (-4V)	Yes	See Note 2	175A (See Note 2)	N/A
OVERCURRENT 2	Not Used	N/A	N/A	N/A
TIME FAULT	Yes	1 second	+VTL Logic Level	See Note 4

Notes:

1. *Follow procedure for checking SCRs as shown on D-560.*
2. *OVERCURRENT 1 (-4V) will interrupt the system when an excessive change in current is detected. A short delay (0 to 8 seconds) may occur before the system is interrupted.*
3. *Check filters and blowers. Power on the 3705-80 and observe the 'THERMAL CHECK' light. If the light turns on again, check thermistors and wiring.*
4. *Check the -5V and +5V power supplies if a TIME FAULT is the only fault indication.*

3705-80 POWER DISTRIBUTION



208/230 V 60 Hz	*220/235 V 50 Hz (Delta)*	*380/408 V 50 Hz (Wye)*	*200 V 60 Hz (Japan)*	*200 V 50 Hz (Japan)*
15A	15A	15A	15A	15A

Notes for World Trade:

1. *For 220/235 V (Delta) or 380/408 V (Wye) 50 Hz power, jumper terminal block PPB-TB3 to obtain 220/235 V for the convenience outlet (see YZ806 and YZ808).*

   For 200 V 60 Hz power (Japan), use PPB-CP1 (5A) with transformer T1 to obtain 100 V for the convenience outlet (see YZ810).

   For 200 V 50 Hz power (Japan), only the PPB-K1 contactor is used with the convenience outlet voltage of 200 V (see YZ814).
2. *For 220/235 V (Delta) or 380/408 V (Wye) 50 Hz power, terminal block PPB-TB3 is jumped to obtain 220/235 V for all blowers and to connect the neutral of the Wye input power to transformer T3 (see YZ808 and YZ830).*

   (All blowers are single phase.)

Legend

PPB — Prime power box
CP — Circuit protector
CB — Circuit breaker
SCR — Silicon controlled rectifier

3705-80 POWER-ON SEQUENCE

- Shows the sequence of events that occur during normal power-on operation (1) when the Local/Remote Power switch is set to the LOCAL position, and the Power On switch is depressed, or (2) when the Local/Remote Power switch is set to the REMOTE position, and the host processor brings power up.

Contact or action causing pickup	*Power Supply Components or Action*	*Timing Relationships*
EPO-J (1, 2, 3, or 4)	PPB-K1 (EPO)	(+24 Vdc For Relays)
PPB-K1 #1 point		Remote position of Local/Remote Power Switch
Press Power On Switch	Power On switch or processor Power On	Local position of Local/Remote Power Switch
Local Power On Switch or processor Power On		
Local Power On Switch or processor Power On	Power Check Light	
Local Power On Switch or processor Power On	Power On Reset	
01D-C1 Transistor picks K2	PPB-K2 (ac to 3705-80)	
01D-C1	+5V 'Start Sequencing' signal sent to frame sequence card	
01D-C1 transistor	12-second timer started	
-4V up in frame	–12V, –5V, and +6V sequence begins when-4V up	
–12V and +6V up in frame	+12V sequence begins when +6V and –12V up	
+5V and +12V up	Sequence complete	
Power-On sequence complete	Power ON Light	+24 Vdc

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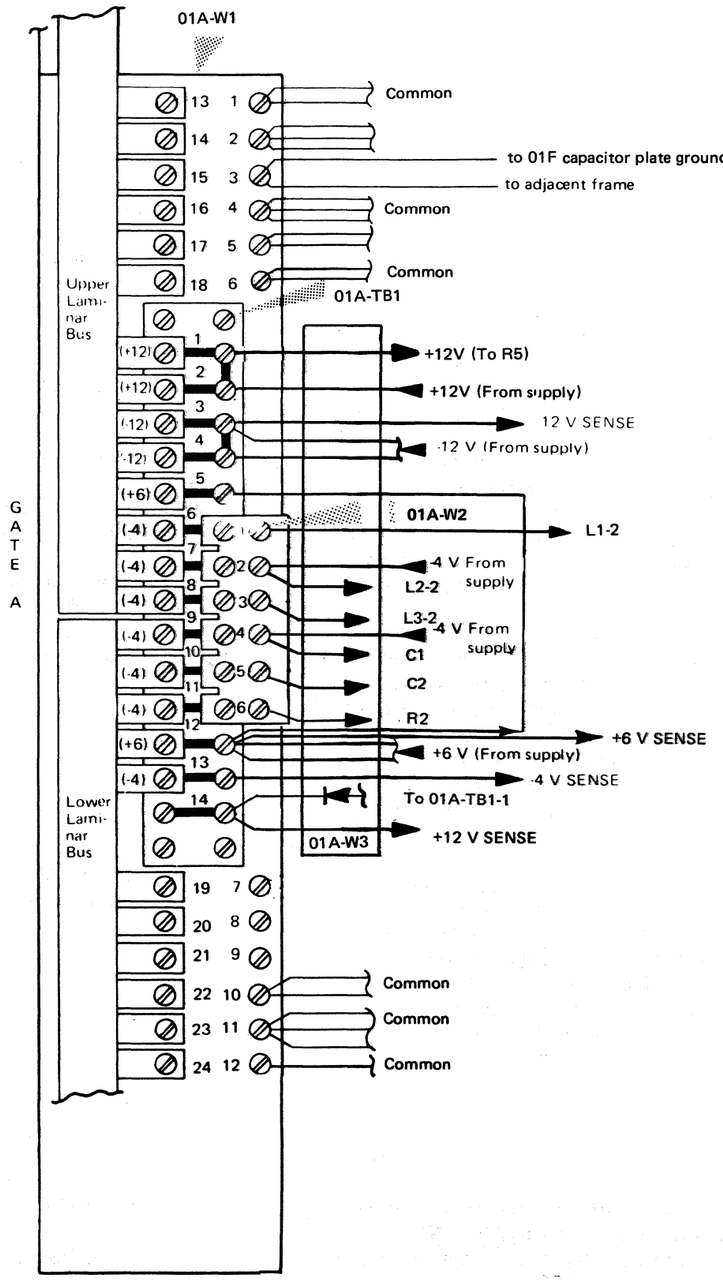
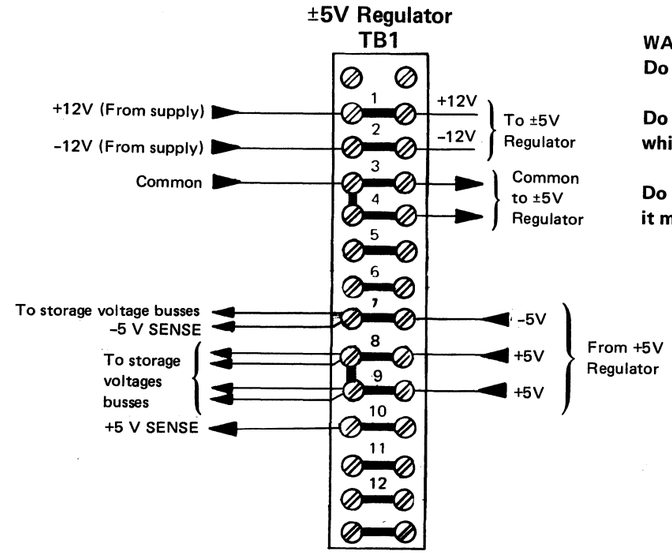
3705-80 DC VOLTAGE DISTRIBUTION (ALD Page YZ836)





WARNING

Do not remove any of the wires labeled SENSE.

Do not remove any of the terminal board (TB) jumpers which connect a voltage with its sense lead.

Do not bend the laminar bus tab too sharply because it may crack upon straightening.

CHECKING +6V, ±12V AND -4V SCRs (PART 1 OF 2)

Because the wave shapes for the -4V, +6V, and ±12V SCRs are similar, only representative samples are shown.

Note: *The +6V and ±12V supplies are each associated with an individual pair of SCRs. The -4V supply is associated with three pairs of SCRs.*

Scope Setup Procedures

1. Setup the scope as follows:
   a. Sync the scope on LINE.
   b. Set horizontal sweep at 5ms/divn.
   c. Set the vertical sweep appropriate to voltage.
2. Put the scope probe on the heat sink for the voltage being tested (see chart below). See **1** for the location of the heat sink.

Voltage	*Heat Sink*
-4V	1, 2, and 3
-12V	5
+12V	6
+6V	7

3. There should be two pulses within 16.7 ms as shown in **2** (20.0 ms for 50Hz).
   a. If one pulse is missing as shown in **3** , the problem is most likely an 'open SCR' or control card.

   Note: *A single SCR, firing alone for voltages other than -4V, does not sustain the output voltage and allow the 3705-80 power to remain on. During the power-on sequence, however, you will see the traces shown in* **3** *for a few seconds.*

   b. To locate an 'open SCR', follow either Procedure A or Procedure B.

Procedure A

1. Use two scope probes with the Vert-Volt/divn for the A and B traces at the same setting (Vert/Mode on Chopped).
2. Attach the A probe to the heat sink associated with the SCRs you are checking **1** .
3. Attach the B probe to the cathode of either SCR.
4. The wave shape displayed on the scope should resemble either **4** or **5** (vertical adjustment of the traces may be necessary to obtain the proper display).

See Note

Procedure B

1. Turn off PPB-CB1.
2. Remove (unsolder) lead from the gate of either SCR associated with the supply being tested.
3. Turn on PPB-CB1 and power-on the 3705 while observing for the waveform shown at **3** .
4. If the waveform at **3** appears, you have removed the gate connection from the open SCR. If no SCR fires, you have removed the gate from the good SCR.
5. Turn off PPB-CB1 and replace the open SCR.

See Note

Note: *Three pairs of SCRs are associated with -4V. Each pair of SCRs operates from one phase of the 3-phase input (refer to YZ530). The 3705-80 may operate with one or two phases missing, therefore, it is essential that each pair of SCRs be checked for an 'open' condition. Do not conclude that -4V SCRs are operating properly until each phase has been checked individually.*

Locating a Shorted SCR

A shorted SCR is the principal cause of a tripped circuit breaker or circuit protector in a 3705-80.

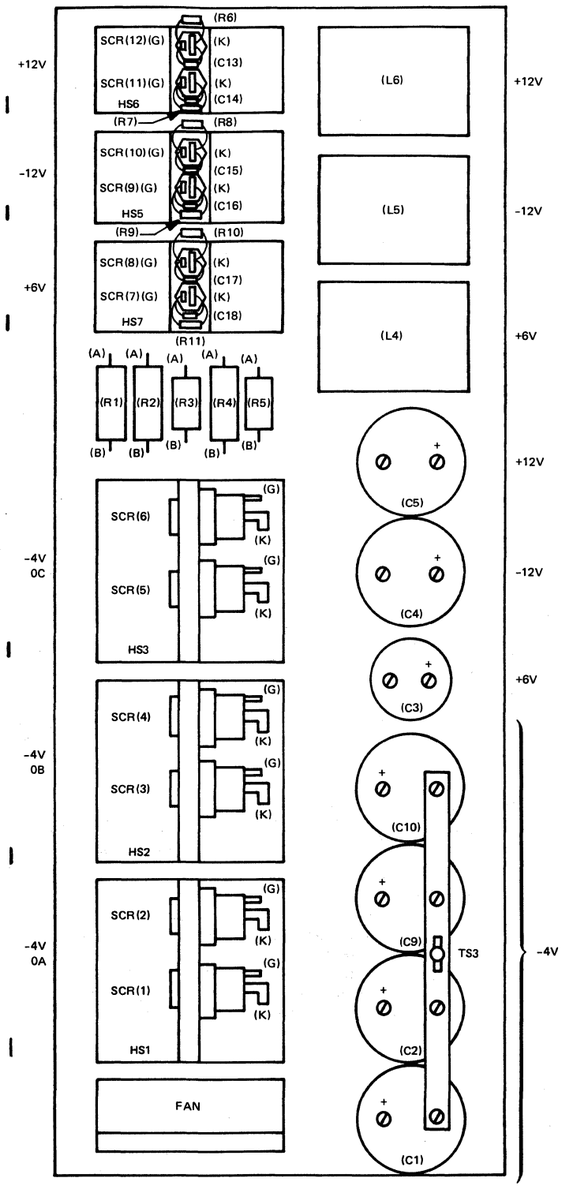
1. If PPB-CB1 (main CB) trips during power-on of a 3705-80, the probable cause is a shorted SCR in the -4V dc power supply.
2. A shorted SCR in the +6V or ±12V dc power supply either acts like a fuse and opens the associated circuit, or causes one of the following conditions:
   a. Overheats transformer wires.
   b. Trips PPB-CB1 (main CB).
   c. Trips CP1, CP2, CP3, or CP4.

Testing the SCR for Shorts

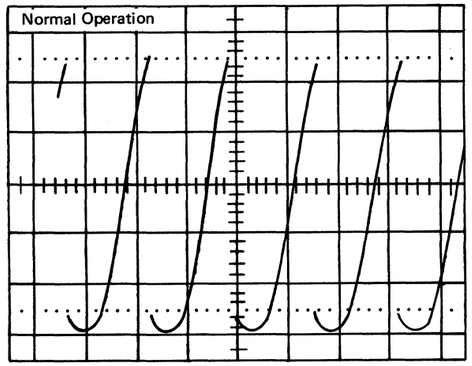
1. Turn off PPB-CB1.
2. Isolate the SCR to be tested.
   a. Remove the phase control card from 01D-A1A1.
   b. Remove the cathode connection from the SCR Note. For an SCR in the -4V supply, remove the cathode connection at the cathode. For SCRs in power supplies other than -4V, remove the cathode connection at T3-TB2 (refer to YZ830).
3. Test for 'anode' to 'cathode' shorts. Use an ohmmeter to determine which SCR is shorted. A shorted SCR may appear as a direct short with a low resistance between the cathode and anode, or may appear as a diode, with a high resistance in one direction and a low resistance in the other. A good SCR has a high reading between the cathode and anode in both directions. Check all SCRs associated with the failing power supply.
4. Test for 'gate' to 'cathode' shorts. Use an ohmmeter to measure the resistance between the gate and cathode of each SCR (see **6**). Readings of 50 ohms or greater in both forward and reversed directions indicate no short. A reading of only a few ohms indicates a short.
5. Unsolder the leads to the bad SCR.
6. Remove the nut and lockwasher that hold the SCR to the heat sink and remove SCR.
7. Mount the new SCR on heat sink.
8. Resolder leads to proper SCR terminals. Turn on PPB-CB1 and power up to verify the repair.

CHECKING +6V, ±12V, AND -4V SCRs (PART 2 OF 2)

Power Supply Mounting Assembly (01F)
-4V, +6V, and ±12V

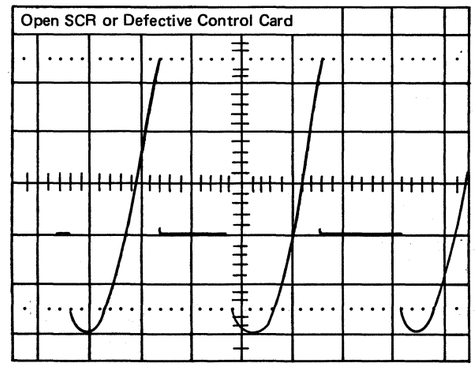


2

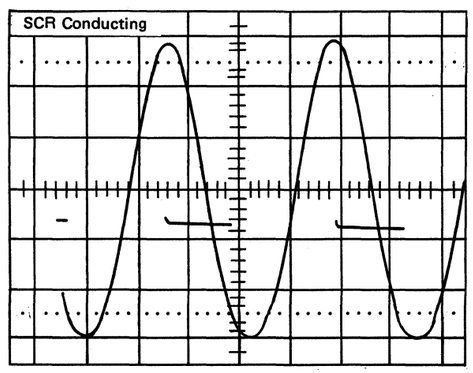


Horz – 2 ms/divn
Vert – Appropriate to Voltage Under Test
Sync – Line

3

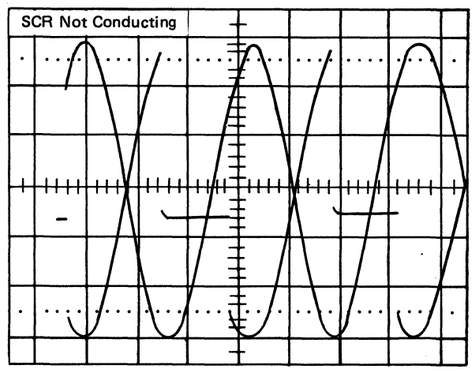


4



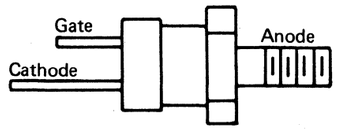
(Scope probe B on cathode of conducting SCR)

5



(Scope probe B on cathode of "open" SCR)

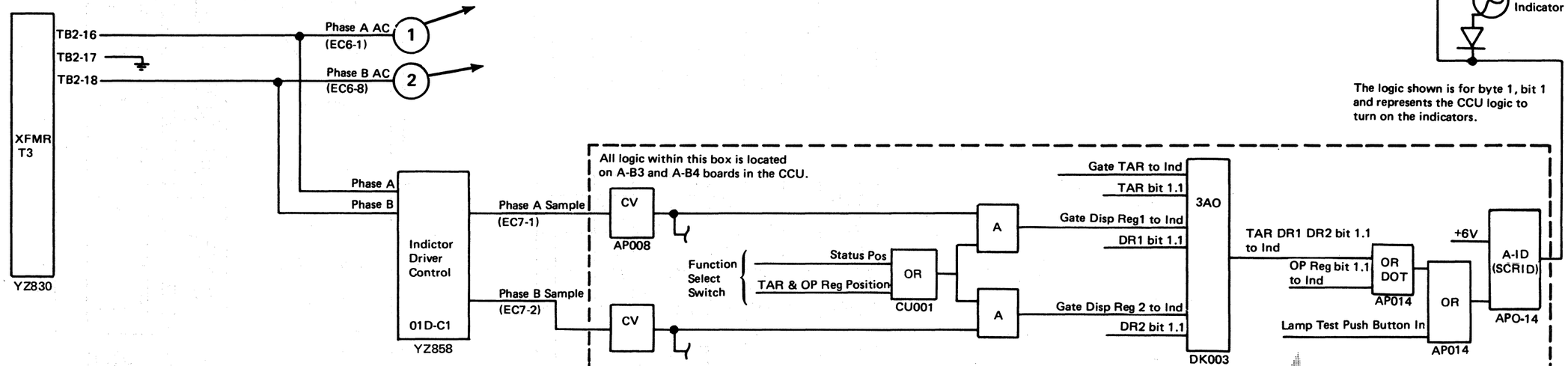
6

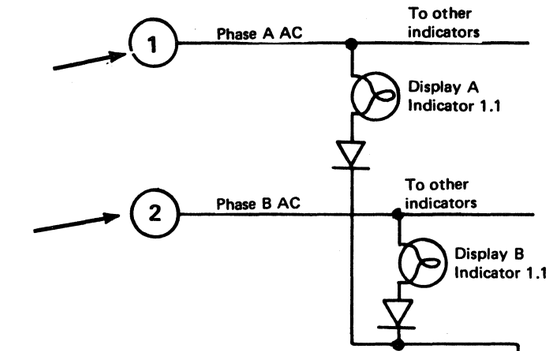


SCR

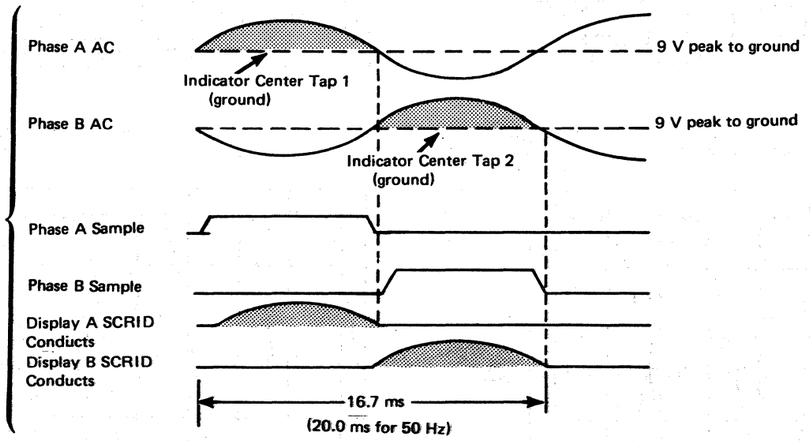
INDICATOR LIGHTS – SUPPLY/CONTROL

One center-tapped winding of T3 is used for the indicator lights. The center-tapped winding is divided into phase A (when TB2-16 is positive with respect to TB2-17) and phase B (when TB2-18 is positive with respect to TB2-17)





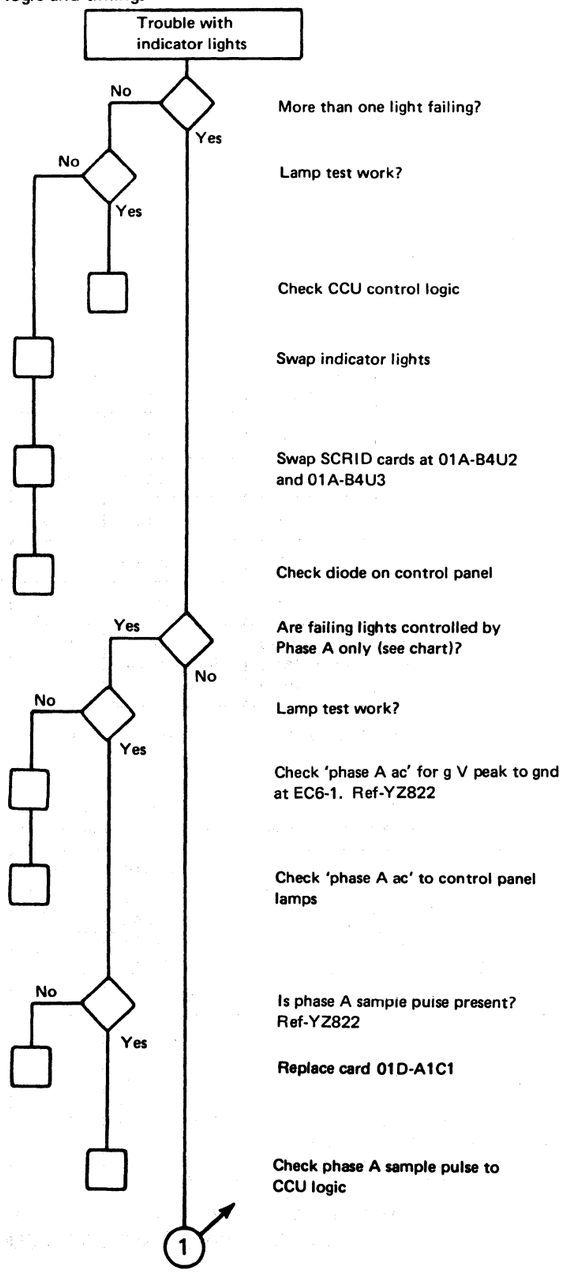
The logic shown is for byte 1, bit 1 and represents the CCU logic to turn on the indicators.

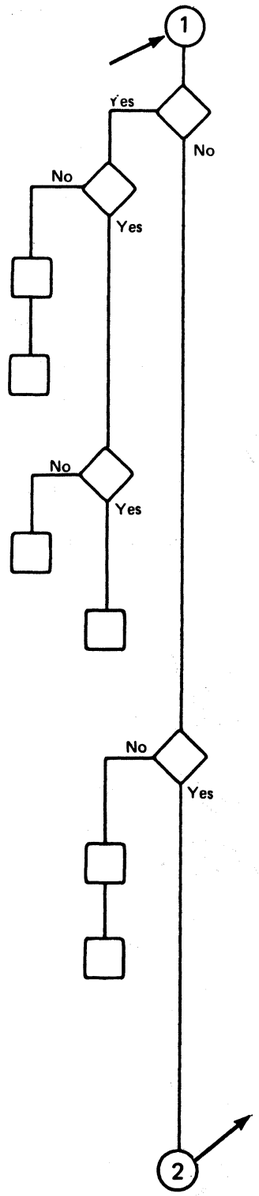


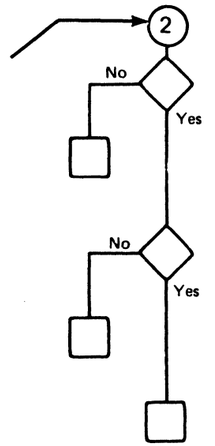
Note: *When the Lamp Test pushbutton is pressed, the intensity of the indicator lights will decrease.*

INDICATOR LIGHTS – CHARTS AND PROCEDURES

Refer to D-570 for logic and timings







Indicator Driver Card (SCRID)	Phase A ac Indicator Display A	Phase B ac Indicator Display B	Logic page
01A-B4U2	0.0 0.1 0.2 0.3	0.0 0.1 0.2 0.3	AP012 AP012
	0.4 0.5 0.6 0.7	0.4 0.5 0.6 0.7	AP013 AP013
	1.0 1.1 1.2 1.3	1.0 1.1 1.2 1.3	AP014 AP014
01A-B4U2	1.4 1.5 1.6 1.7	1.4 1.5 1.6 1.7	AP015 AP015
01A-B4U3	Chan 1 Intf A Enbl	Chan 1 Intf B Enbl	AP009
	Chan 2 Intf A Enbl	Chan 2 Intf B Enbl	
	Panel Active		
		CCU Check	AP009
	Spare Spare Hard Stop Wait	Spare Pgm Display Test Pgm Stop	AP010 AP010
01A-B4U3	Load X.4 X.5 X.6 X.7	 X.4 X.5 X.6 X.7	AP011 AP011

DC VOLTAGE MEASUREMENT

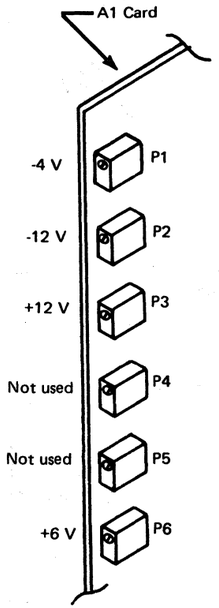
- Voltages should be set using a digital voltmeter.

Voltage	*Voltage Measurement**	*Location of Voltage Adjustment Potentiometer on Card 01D-A1A1*	*Maximum Ripple (peak to peak)*
-4V	B06 on any board	P1	80mV
-12V	01A-TB1-3	P2	480mV
+12V	01A-TB1-1	P3	480mV
+5V	5V Regulator TB1-9	Adjustment potentiometer is on ±5V regulator card	50mV
-5V	5V Regulator TB1-7	Not Adjustable	50mV
+6V	01A-TB1-12	P6	240mV

*Measure individual voltages between frame and the points shown on this chart

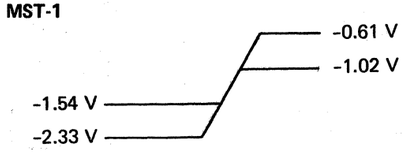
Power Supply Regulation And Maximum Current

Voltage	*Power Supply Regulation*	*Maximum Rated Output Current*
-12V	+0.84V	8.5A
-4V	+0.16V	145A
+6V	0.24V	8A
+12V	+0.84V	10A
+5V	±0.25V	4A
-5V	±0.25V	0.8A

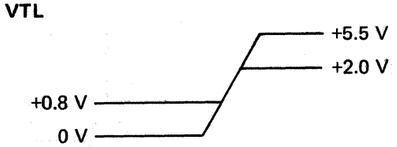


Logic Voltage Levels

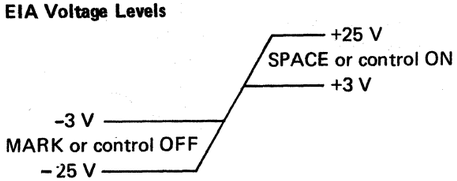
MST-1



VTL

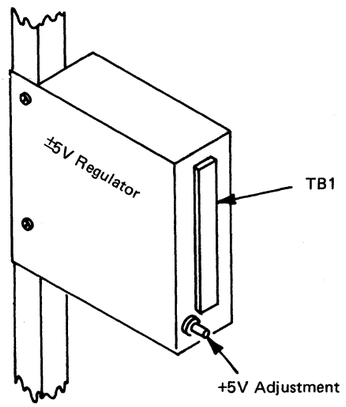


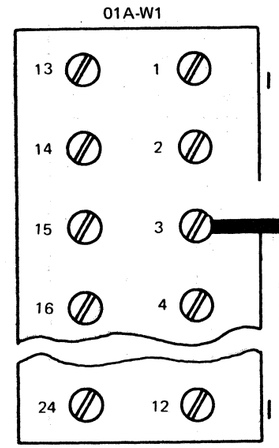
EIA Voltage Levels



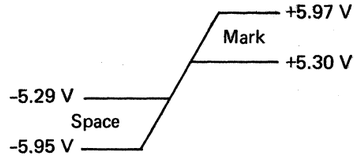
DC Common—Frame Ground Condition

- dc common and frame ground are tied together in by a wire that connects jumper bus 01A-W1-3 to the plate base. See YZ536.
- Eight jumper assemblies (P/N 1770813) are mounted between frame ground (at board mounting screws) and the dc signal ground pin positions for each logic board located on gate(s) 01A.

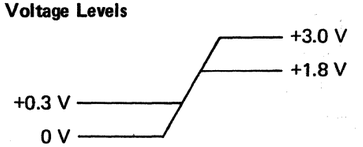




Mil 188 Voltage Levels

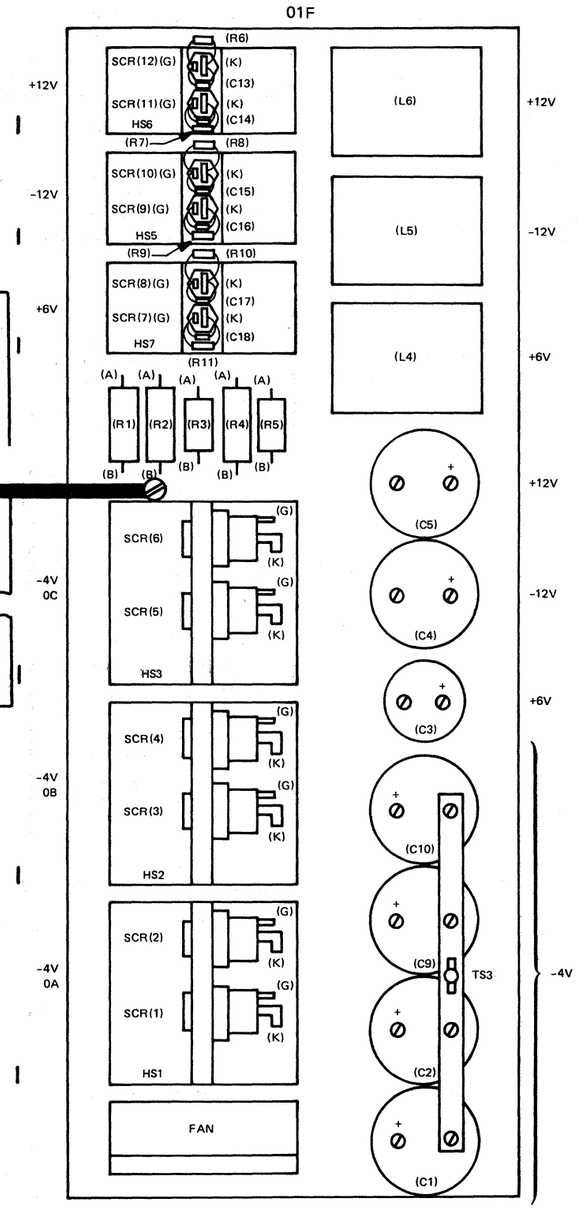


SLT Voltage Levels



Digital Levels

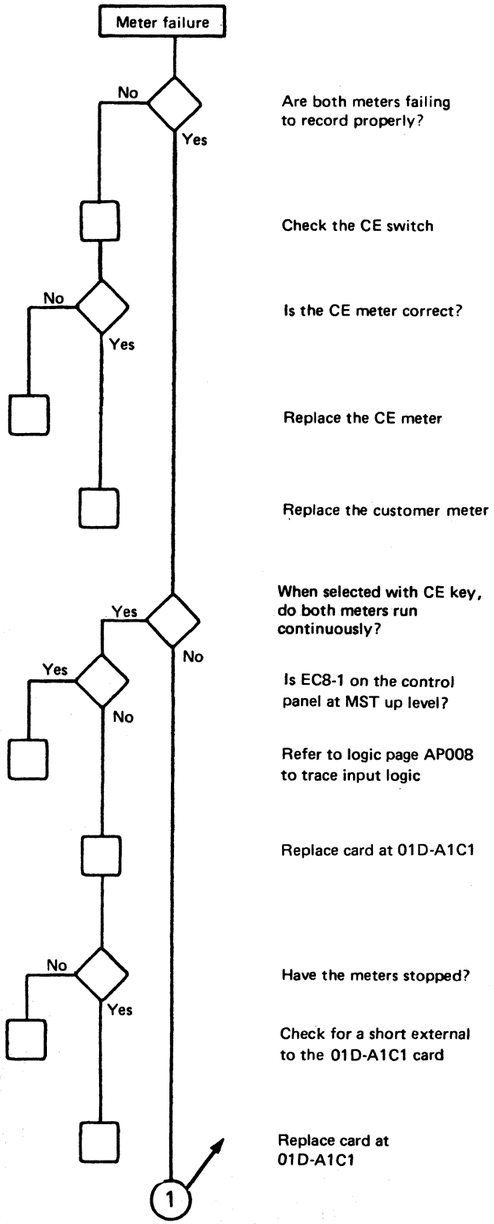
SPACE or control ON – 23 ma (+1 V)
MARK or control OFF – 5 ma (-0.7 V)
Open circuit – control OFF

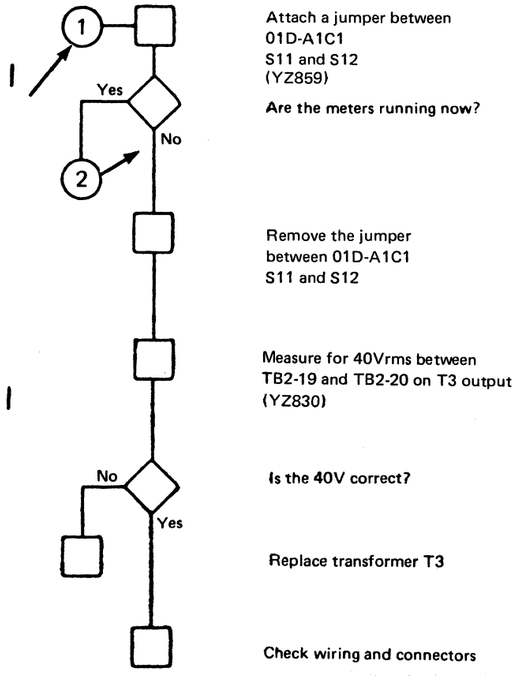


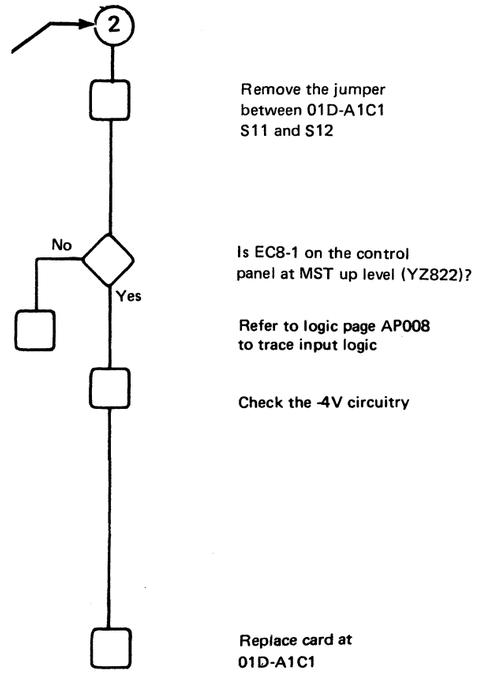
Power Supply Mounting Asm.

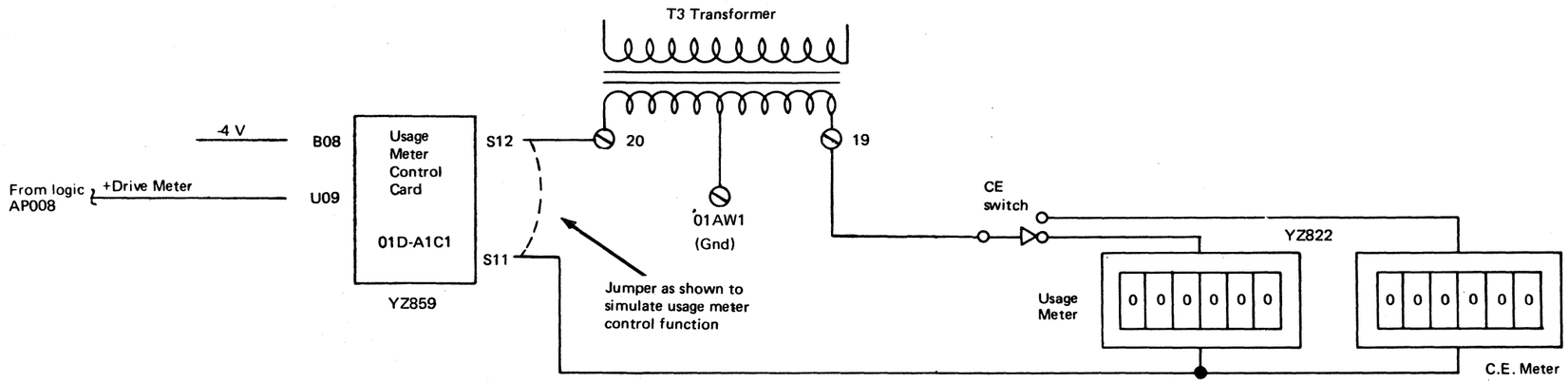
USAGE METER

See 1-030 for the conditions that cause the usage meter to run.









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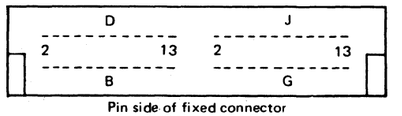
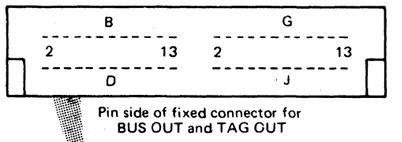
3705-80 Physical Locations

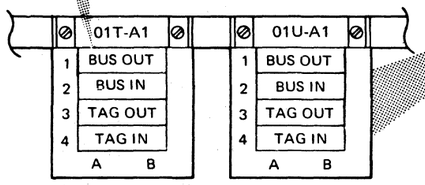
See logic page YZ801 sheets 1–17 for physical location details not shown on this page.



Pin side of fixed connector for BUS IN and TAG IN



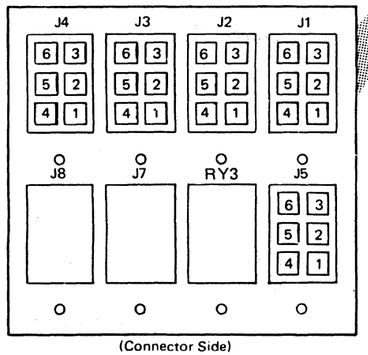
Pin side of fixed connector for BUS OUT and TAG OUT



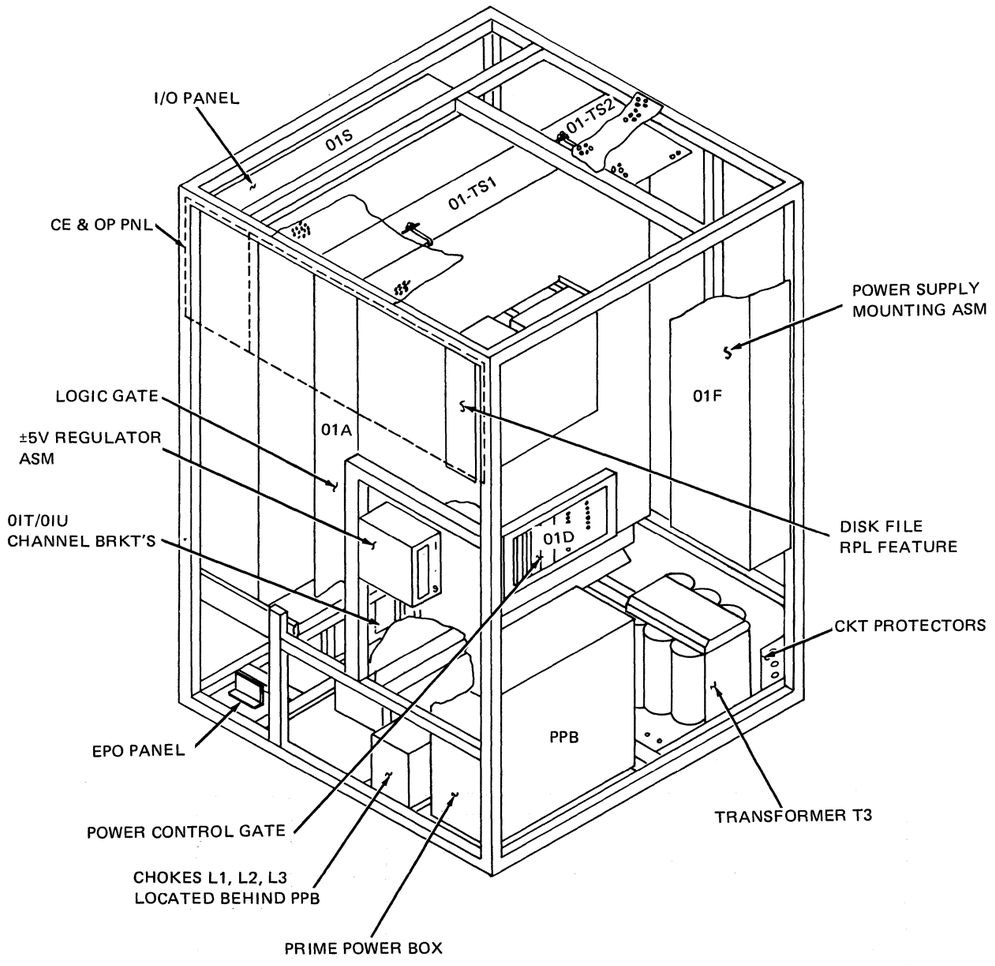
CHANNEL INTERFACE A (Connector Side)

CHANNEL INTERFACE B

EPO PANEL

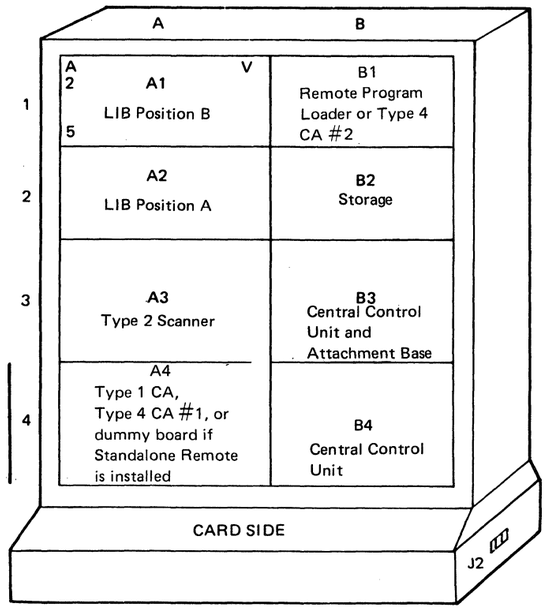


(Connector Side)

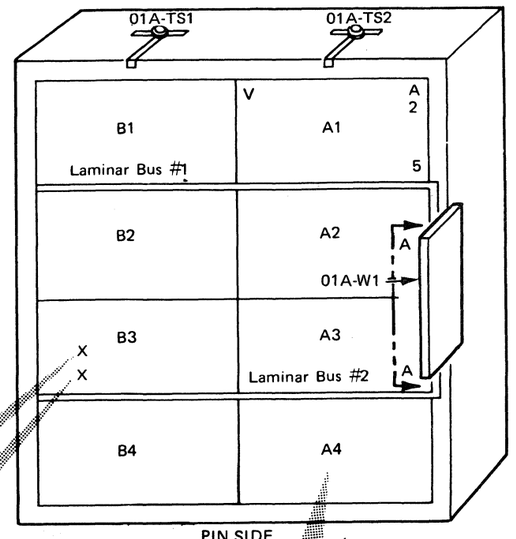


	BUS	TAG	CABLE
S/360	P/N 5440649	P/N 5440650	P/N 5353920
S/370	P/N 2282675	P/N 2282676	P/N 5466456

LOGIC GATE–01A

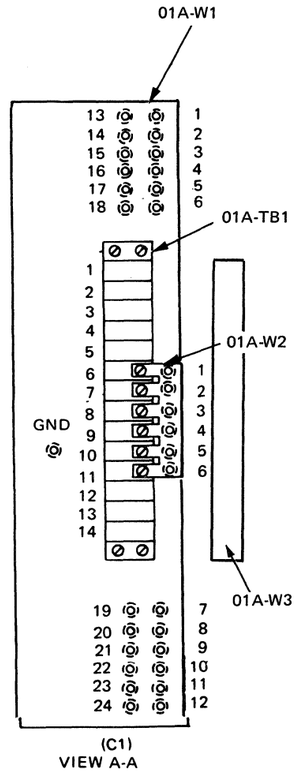


LOGIC GATE – 01A



Scope Synchronization Pin No. 1 (01A-B3M2P10)
Scope Synchronization Pin No. 2 (01A-B3M2P13)
Address Compare (01A-B3 P2 S09)

Type 1 CA, Type 4 CA #1, or dummy board if Standalone Remote is installed.



(C1)
VIEW A-A

TOOLS AND TEST EQUIPMENT

A. Special tools, test equipment, and maintenance supplies to be shipped with the 3705-80.

Description	*P/N*
"Y" Jumper	1770810
Jumper	1770811
Test Block	6835406 (LS1 only)
Test Block	1770812 (LS2, LS3, LS4, LS5, LS8, LS9)

B. Test equipment and non-technology related tools required for the 3705:

1. Test equipment

P/N	*Description*	*Quantity*
454550 or	454 Tektronix* Scope	1
453047	453 Tektronix* Scope	1
453585	Digitec **251 or 266 Meter	1
453545	db Meter	1
5851882	MST 1 CE Indicator Latch Card	1

2. Tools

P/N	*Description*	*Quantity*
453631	Microfiche Viewer	1
5801645	Back Panel Indicator Card	1

C. Technology related tools

Refer to Tools and Test Equipment TSL No. 43 and to the *Monolithic System Technology, Packaging, Tools, Wiring Change Procedure, SY22-6739* for tool requirements of the IBM 3705. Some of these tools may not be part of the normal maintenance package and should not be ordered by the Branch Office.

* Trademark of Tektronix, Inc.
** Trademark of United Systems Corporation

PREVENTIVE MAINTENANCE

Unit	*Freq*	*Check*	*When Checked*
		1. Check all voltages	At installation
		2. Tighten all screw type connections of power system	At installation and 6 months after installation
		3. Check indicators	On each call
1	6	4. Check cooling fans	Determined by the operating environment
		5. Check air filters	
2	12	6. Check line cord, plug, terminals, and grounding	Every 12 months
		7. Scope all SCRs	Every 12 months

Remote Program Loader

INTRODUCTION

Remote Program Loader

This feature provides the capability of loading the ACF/NCP/VS (Advanced Communication Function/Network Control Program/Virtual System) into the 3705-80 over the following:

- The communication facility when:
  - There is no channel adapter on the remote 3705-80.
  - The channel adapter enable/disable switch is in the "disabled" position and the channel adapter is not enabled.
  - The remote 3705-80 ACF/NCP/VS requests an IPL by executing an Output X'79' if the ACF/NCP/VS had requested that the IPL occur over the communication facility (by executing an Output X'6B' with bit 0.4 = 1).
- The channel adapter when:
  - The channel adapter has an 'initial selection level 3 interrupt' pending when a Write IPL command X'05' is in its command register.
  - The enable/disable switch for the channel adapter is in the "enabled" position.
  - The channel adapter is enabled and the NCP has requested that the IPL occur over a channel adapter (by executing an Output X'6B' with bit 1.4 = 0) [see 2-160].

When the 3705-80 contains a Remote Program Loader-II and a channel adapter, the 3705-80 can be IPLed as a local (using the channel adapter with one host processor or be re-IPLed as a remote (using the RPL with another host processor if the first processor becomes inoperative. The 3705-80 must be operating with ACF/NCP/VS.

Both features also provide for diagnosing the appropriate remote 3705-80 without the aid of the host processor. The remote 3705-80 is capable of diagnostic checkout, line selection to the host processor, connection with the host processor via the local 3705-80, and receiving the remote network control program that was transmitted from the host processor.

Remote Program Loader Hardware

The remote program loader contains the hardware units required to load the remote network control program from the host processor via a local 3705-80. These hardware units are:

- A Diskette drive and a Diskette
- A Diskette controller
- A ROS (read-only-storage) with a bootstrap program to operate the Diskette drive via the Diskette controller.

The Diskette contains the loader, dump, and diagnostic programs. Normally, the Diskette is used only for read-only-storage. Writing is enabled when the remote 3705-80 is not initialized or when a wire jumper is installed.

The wire jumper is to be used only for Diskette program update. Writing when the remote 3705-80 is not initialized is used to dump (write) the upper 8K of storage onto Diskette tracks 15 and 16 when a program dump is requested.

The Diskette controller controls the Diskette operations via input and output instructions from the control program.

The ROS bootstrap program used with the remote program loader is loaded into 3705-80 main storage during the IPL sequence in the same manner as the bootstrap program for a channel adapter. The ROS bootstrap program tests the instructions needed to load the loader programs into storage from the Diskette, checks the Diskette operations, and controls loading the loader program from the Diskette into the remote 3705-80 main storage.

Synchronous Data Link Control (SDLC) Operation

Communication between local and remote 3704/3705 controllers is by SDLC — a discipline for the management of information transferred over a data communication facility. The type 2 communication scanner is used in the local 3705-80 and the remote 3705-80 for the SDLC operation. The type 2 scanner is the only scanner available for 3705 Model 80 SDLC operation.

Communication Facillty Between the Local and Remote 3705-80

The primary communication facility must be a point-to-point or multipoint non-switched facility. The following chart lists the line sets (by line speed) that may be used on the primary communication facility.

Primary Facility

Speed	*3705-80 Line Set*	*Data Mode*
1200 bps	LS1	HDX or Duplex
2000 bps	LS1	HDX or Duplex
2400 bps	LS8, LS1	HDX or Duplex
4800 bps	LS1, LS8	HDX or Duplex
9600 bps	LS9	HDX or Duplex
19.2 kbps	LS3	HDX or Duplex
40.8 kbps	LS2, LS3	HDX or Duplex
48.0 kbps	LS2	HDX or Duplex
50.0 kbps	LS3	HDX or Duplex
56.0 kbps	LS2	HDX or Duplex

A secondary communication facility may be used as an alternate path for communication when the primary path is not operational. The secondary facility is point-to-point and may be switched or non-switched. The following chart lists the line sets (by line speed) that may be used on the secondary communication facility.

Secondary Facility

Speed	*Facility**	*3705-80 Line Set*	*Data Mode*
600 bps	S	LS1	HDX
1200 bps	S		HDX
	N	LS1	HDX or Duplex
2000 bps	S	LS1	HDX
	N	LS1	HDX or Duplex
2400 bps	S	LS1	HDX
	N	LS1	HDX or Duplex
4800 bps	N	LS1, LS8, LS9	HDX or Duplex
	S	LS1	HDX
9600 bps	N	LS1, LS8, LS9	HDX or Duplex
19.2 kbps	N or S N	LS3	HDX or Duplex
40.8 kbps	N	LS2, LS3	HDX or Duplex
48.0 kbps	N	LS2, LS8, LS9	HDX or Duplex
50.0 kbps	N or S N	LS3	HDX or Duplex
56.0 kbps	N	LS2	HDX or Duplex

*N = Non-switched S = Switched

CONTROL PROGRAM LOAD DATA FLOW

1 A control program load can be initated by:
- Normal power on at the remote controller.
- Pressing the LOAD pushbutton on the remote 3705-80 control panel.
- The remote control program detecting a hardware failure in the remote controller.
- The host processor issuing a Load Initial which causes the local NCP to issue a 'Set Initialization Mode' command to the remote controller.

Each method starts the IPL (initial program load) sequence (A) that loads the ROS bootstrap program (B) into main storage.

2 The Diskette drive, under control of the ROS bootstrap program, reads LP1 (load program 1) (C) into main storage. LP1 then controls the reading of LP2 (D) from the Diskette drive into the main storage.

3 LP2 activates the scanner and the SDLC line interface address in the LIB to set up communications with the local controller.

4 The host processor issues a Load Initial to cause the local NCP to issue a SIM command to condition LP2 in the remote controller to receive the remote NCP (network control program). Then the host processor sends the remote NCP to the local channel adapter.

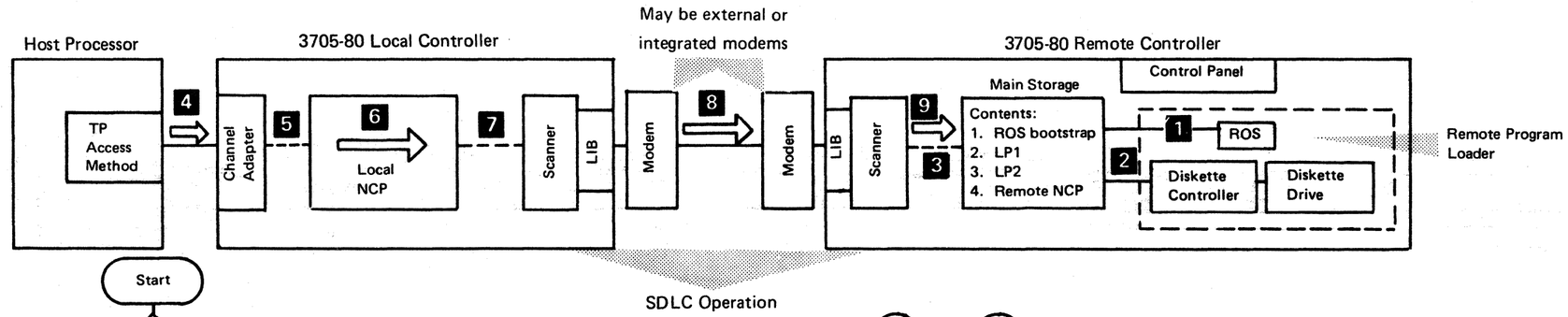
5 The channel adapter notifies the local NCP (by interrupts) as the remote NCP data arrives.

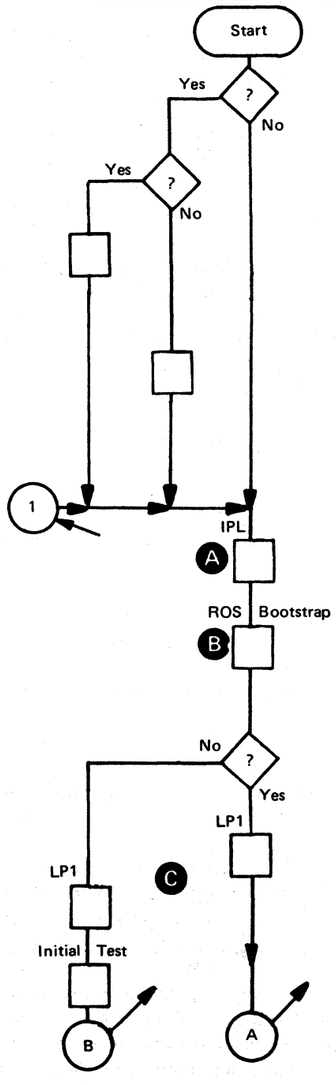
6 The local NCP processes the remote NCP data to be sent to the remote controller.

7 The local NCP had activated the scanner and the SDLC (synchronous data link control) line interface address in the LIB before issuing the SIM command to the remote controller (see **4**).

8 The remote NCP data is transmitted over the communication facilities using SDLC.

9 The scanner notifies LP2 (by interrupts) as the remote NCP data arrives and is loaded into main storage. LP2 then turns control of the remote controller over to the remote NCP. (E)





Is a dump or IFT load required?

Dump required?

Manual intervention is required to prevent executing the initial test and to cause the high 8K of storage to write on the Diskette.
1. Set '0BBBB' in the STORAGE ADDRESS/REGISTER DATA switches.
2. Press the LOAD button.
3. Press the INTERRUPT button.

Manual intervention is required to load IFTs.
1. Set the FUNCTION SELECT switch to the STORAGE ADDRESS position.
2. Set '0DDDD' in the STORAGE ADDRESS/REGISTER DATA switches.
3. Press RESET, press LOAD' and then press the INTERRUPT button.

Initiate the IPL sequence. This loads the ROS bootstrap program into main storage (see Page F-050 for the IPL sequence).

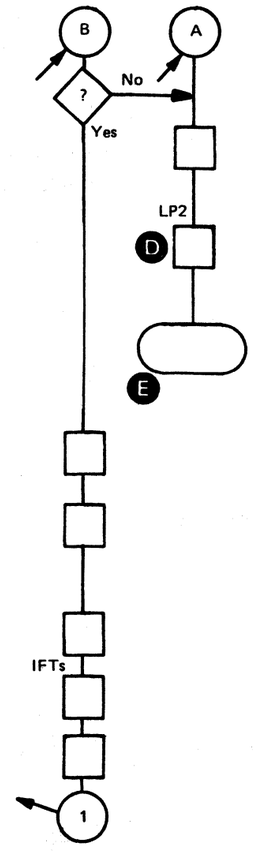
The ROS bootstrap:
1. Tests the instructions used in loading from the Diskette.
2. Checks the Diskette controller.
3. Reads LP1 from track 0 of the Diskette.

Is the "dump bit" (Register X'68' bit 0.0) on?

Read the dump subroutine from track 17 and write the high 8K of main storage onto Diskette tracks 15 and 16.

Read the initial test into main storage from Diskette tracks 1 through 5.

Execute "initial test".



Are the IFTs to be loaded?

Read LP2 from Diskette tracks 6 and 7.

LP2 controls:
1. Transmitting the "dump" to the controlling CPU.
2. Loading the remote NCP from the host CPU.

LP2 turns control over to the remote NCP.

Read the IFT loader from Diskette track 8.

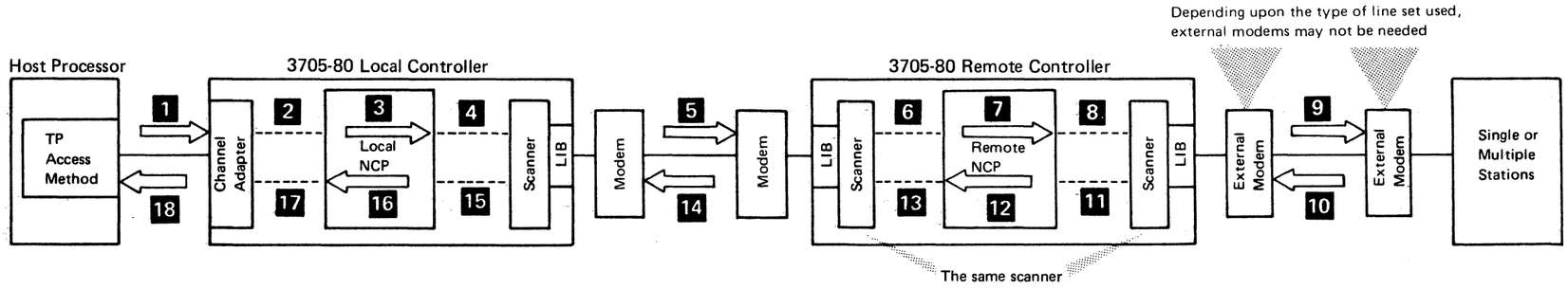
Read the diagnostic control monitor (DCM) from Diskette track 9 and the hardware configuration data set CDS) from Diskette track 10.

Read the IFTs from Diskette tracks 18 through 76.

Execute the IFTs.

Re-IPL for normal operation.

DATA TRANSFER BETWEEN HOST PROCESSOR AND REMOTE STATION USING A LOCAL AND REMOTE CONTROLLER



Host Processor to Station

1 The host processor sends data to the local controller.

2 The channel adapter notifies the local NCP (Network Control Program) (by interrupts) as data arrives.

3 The local NCP determines that the destination of the data is a station connected to the remote controller.

4 The local NCP activates the scanner and remote controller line interface address in the LIB when data is ready to be sent to the remote controller.

5 Data is transmitted over the communication facility to the remote controller.

6 The communication scanner notifies the remote NCP (by interrupts) as data arrives.

7 The remote NCP processes the data and prepares it for the station.

8 The remote NCP activates the scanner and station's line interface address in the LIB when data is ready to be sent to the station.

9 Data is transmitted over the communication facility to the station.

Station to Host Processor

10 The station sends the data to the remote controller.

11 The scanner notifies the remote NCP (by interrupts) as the data arrives.

12 The remote NCP processes the data and prepares it for the host processor.

13 The remote NCP activates the scanner and local controller line interface address in the LIB when data is ready to be sent to the local controller.

14 Data is transmitted over the communication facility to the local controller.

15 The scanner notifies the local NCP (by interrupts) as the data arrives.

16 The local NCP prepares the data for the host processor.

17 The local NCP activates the channel adapter when data is ready to be sent to the host processor.

18 The channel adapter transfers the data to the host processor.

REMOTE 3705-80 CONTROL PANEL

3705-80 Used Only as a Remote

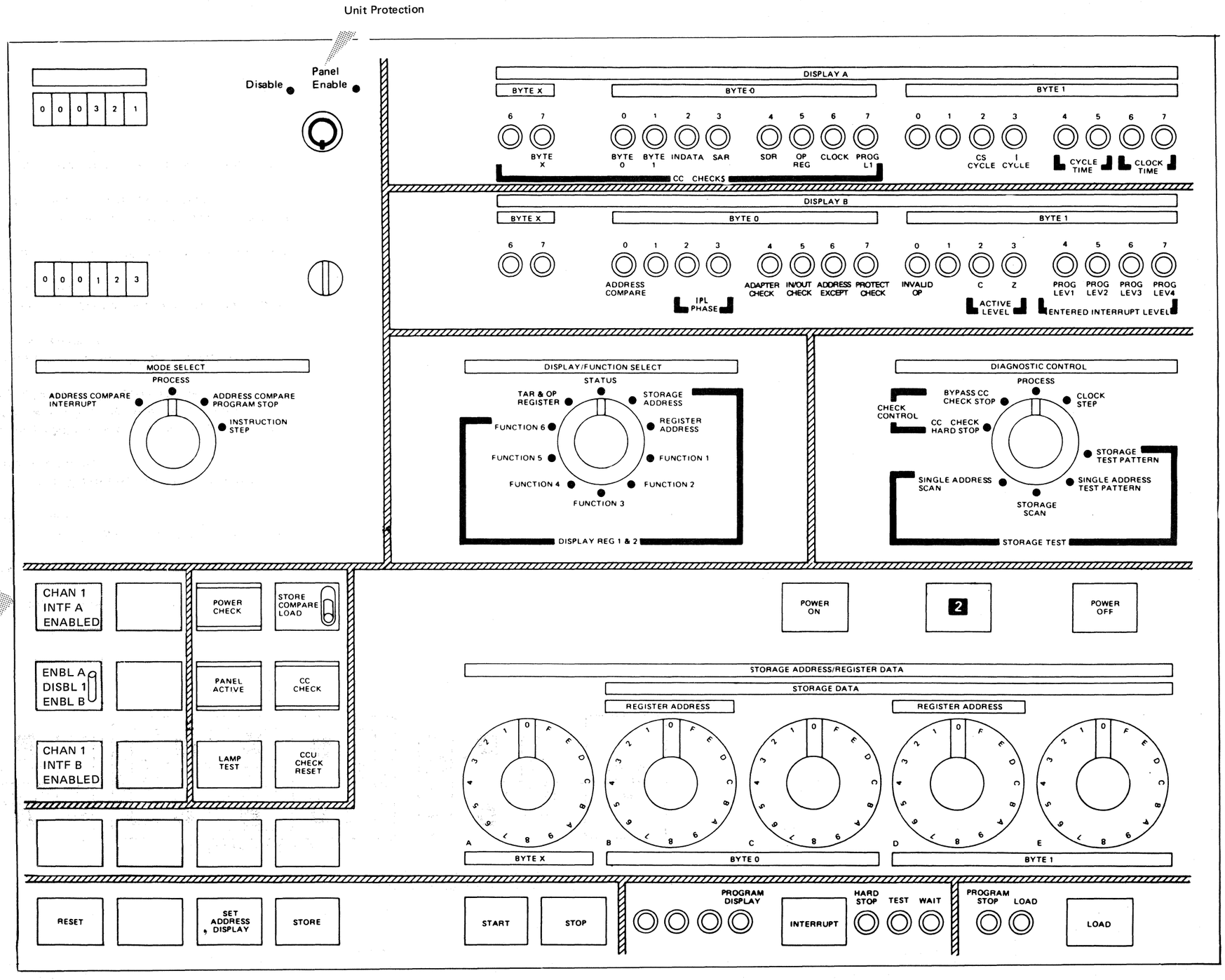
The remote 3705-80 control panel is identical to the Local 3705-80 control panel except that all the channel enable/disable switches (and the associated enable indicators) and the local/remote power switch have been removed and replaced with blanks (see **1** and **2**).

3705-80 Used as Either a Remote or a Local

The control panel for this 3705-80 is identical to the Local 3705-80 control panel.

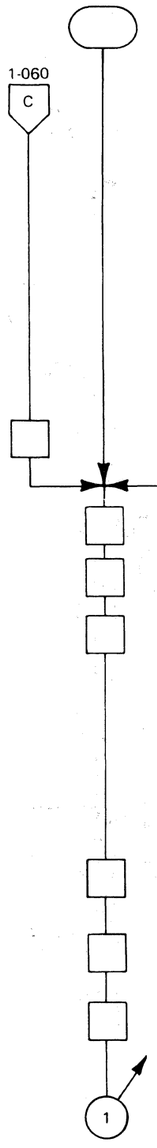
See the control panel section at page 1-000 in Volume 2 of this manual for a description of the function and use of the control panel.

CA switches and indicators are present only if the CA feature is installed. CA switches and indicators are not present if the 3705-80 is a standalone remote controller.



REMOTE IPL SEQUENCE (PART 1 OF 3)

This is a high level overview of remote IPL. Use the flowchart in the IBM Remote Loader Diagnostic section of this FETMM (Volume I, SY27-0208) for troubleshooting.



Start IPL

The DIAGNOSTIC CONTROL switch must be in the PROCESS position and either:

1. The LOAD push button is pressed.
2. The POWER ON push button is pressed.
3. A CCU check occurs.
4. The host processor issues a Load Initial command. This causes the local NCP or ACF/NCP/VS to issue a SIM (set initialization mode) SDLC instruction that causes the remote NCP or ACF/NCP/VS to execute an Output X'79' with bit 0.2 on to start the IPL. This Output X'79' also selects the RPL ROS on a remote 3705-80 with channel adapters if the ACF/NCP/VS has set the 'select RPL ROS' latch with an Output X'6B' with bit 0.4=1 (see F-080).

A remote 3705-80 with channel adapters also selects the RPL ROS if all the channel adapters are disabled and all the channel adapter enable/disable switches are in the "disable" position.

Note: *See pages 6-960 through 6-963 in Volume 2 of this FETMM for more details about phase 1 and 2.*

Press LOAD.

IPL Phase 1

Turn on LOAD indicator.

Turn on IPL PHASE 1 indicator

Initiate a general CCU reset.

During the general reset:

1. The storage key for the first 2k bytes of main storage is set to zero.
2. The TEST indicator is turned on.
3. Interrupt levels 2 through 5 are masked.
4. Interrupt level 1 is unmasked.
5. The interrupt entered latches are reset.
6. All interrupt requests are reset.
7. The 'program stop' and 'hard stop' latches are reset.
8. Main storage references are inhibited.

Turn off IPL PHASE 1 indicator.

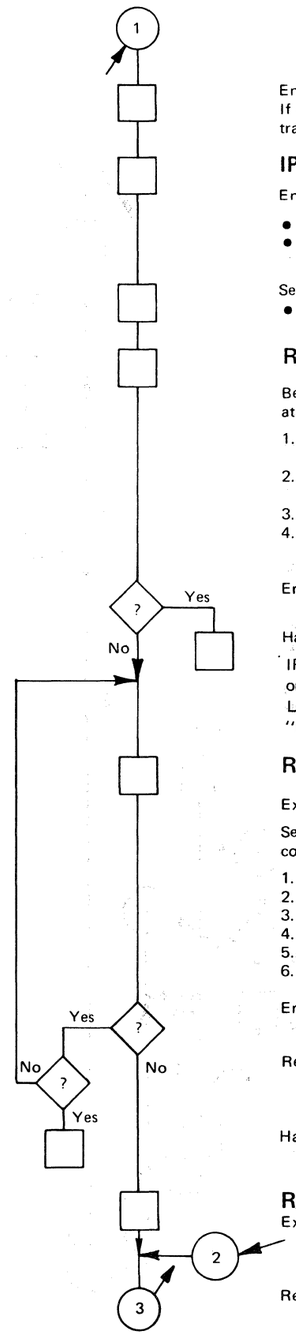
If the IPL PHASE 1 indicator remains on, a hardware reset error occurred.

IPL Phase 2

Enter IPL phase 2, turn on IPL PHASE 2 indicator.

Load ROS bootstrap program from ROS to main storage.

- Load 1024 bytes into main storage beginning at address X'00000'.
- The data transfer from ROS to main storage is via cycle steal at 1 byte per cycle.



End IPL phase 2, turn off IPL PHASE 2 indicator.
If the IPL PHASE 2 indicator remains on, the ROS to main storage transfer is not complete.

IPL Phase 3

Enter IPL phase 3. Turn on IPL PHASE indicators 1 and 2.

- 3705-80 begins ROS bootstrap program execution.
- The bootstrap program is divided into three sections.

Set IPL L1 interrupt request

- The bootstrap program executes at program level 1.

ROS Section 1

Begin executing the first section of the ROS bootstrap program at address X'0010'.

1. Saves general registers of group 0 (program level 1 and 2) starting at storage location X'0780'.
2. Verifies the operation of the instructions to be used in sections 2 and 3 of the ROS bootstrap program.
3. Saves external registers X'76', X'7D', and X'7E'.
4. Uses Input X'79', bit 1.7 to check for a branch to the bootstrap escape address (X'06FC').

Error detected?

Hard stop and display the error code.

IPL PHASE indicators 1 and 2 and the TEST indicator will be on with an error code displayed in TAR. See the IBM Remote Loader Diagnostic section of this FETMM (Volume I, SY27-0208) "IPL Procedures" for detailed error analysis.

ROS Section 2

Execute the second section of the ROS bootstrap program.

Section 2 of the ROS bootstrap program tests the Diskette controller data path. The tests include the following:

1. CRC register test.
2. PDR test.
3. Adapter reset test.
4. Diskette speed verification test.
5. Access test.
6. Head engage/disengage test.

Error detected?

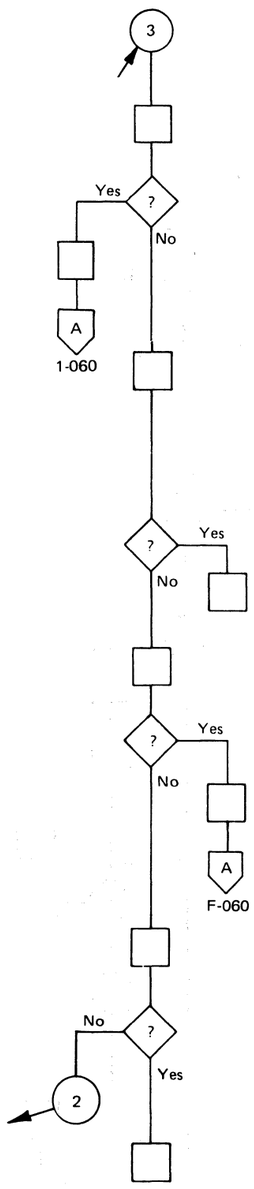
Retry count = 0?

Hardstop, see Note.

ROS Section 3

Execute section 3 of the ROS bootstrap program.

Read load program 1 from Diskette track 0.



Read load program 1 from Diskette track 0.

Load successful?

Reset IPL PHASE indicators and the IPL L1 interrupt request.

Generate an OBR record. See Page F-070 for the OBR field definitions.
Read error can be caused by:

- Track identification error.
- Data bit comparison failure.
- CRC error.
- No data received after a read command was issued to the Diskette controller.

Retry count = 0?

Hardstop with IPL PHASE 1 and 2 and the LOAD indicators on. See Note.

Read load program 1 from Diskette track 11

Load successful?

Reset IPL PHASE indicators and the IPL L1 interrupt request.

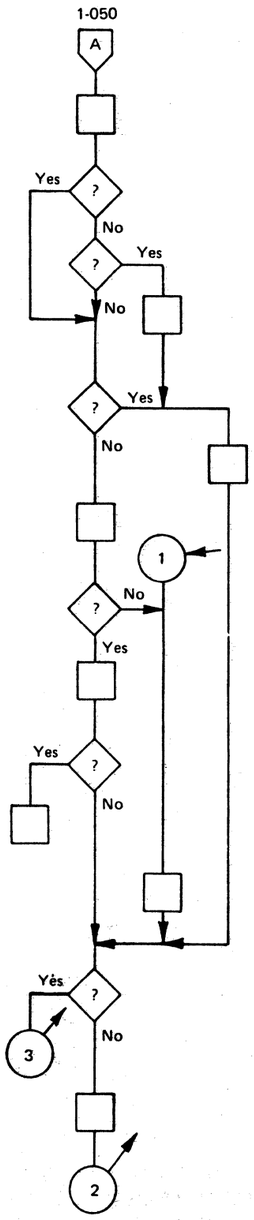
Decrement retry count by 1.

Retry count = 0?

Hardstop with IPL PHASE 1 and 2 and LOAD indicators on. See Note.

Note: *Remote Loader Diagnostic information for the 3705-80 is contained in the RPL section of this FETMM (Volume I, SY27-0280).*

REMOTE IPL SEQUENCE (PART 2 OF 3)



Load Program 1

Begin execution of load program 1

Did host processor initiate the IPL?

Do the Address/Data switches "B" through "E" = 'BBBB'?

Register X'6B' bit 0.0 (dump bit) is turned on. When this bit is on, the high 8k bytes of storage is preserved. This bit on does not cause a dump unless the host system requests one.

Is Register X'6B' Bit 0.0 on?

Write the high 8k bytes of storage onto Diskette tracks 15 and 16.

Initial Test

Read the Initial Test from Diskette tracks 1 through 4.

Was the load successful?

Execute the Initial Test program.

Were any errors detected?

Hard stop. See Note.

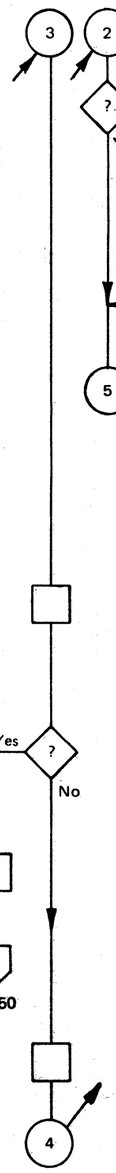
Generate an OBR record, See Page 1-070 for the OBR field definitions.

Do the Address/Data switches "B" through "E" = 'DDDD'? This indicates a request to run the IFTs.

Note: *To get out of a continuous retry loop, set the Address/Data switches "B" through "E" to 'DDDD' and press INTERRUPT.*

Read load program 2 from Diskette tracks 6-7.

Note: *Remote Loader Diagnostic information for the 3705-80 is contained in the RPL section of this FETMM (Volume 1, SY27-0208).*



Was the load successful?

Read load program 2 from Diskette tracks 12-13.

Was the reload successful?

Decrement retry count by 1.

Retry count = 0?

Read the "IFT Diskette Loader" and the "CDS Writer" from Diskette track 8.

Note: *The INTERRUPT key must have been pressed after the LOAD key to read the IFTs.*

Are changes to be made to the CDS?
If yes, the Function Select switch will be at the Register Address position.
If no, the Function Select switch will be at the Storage Address position.

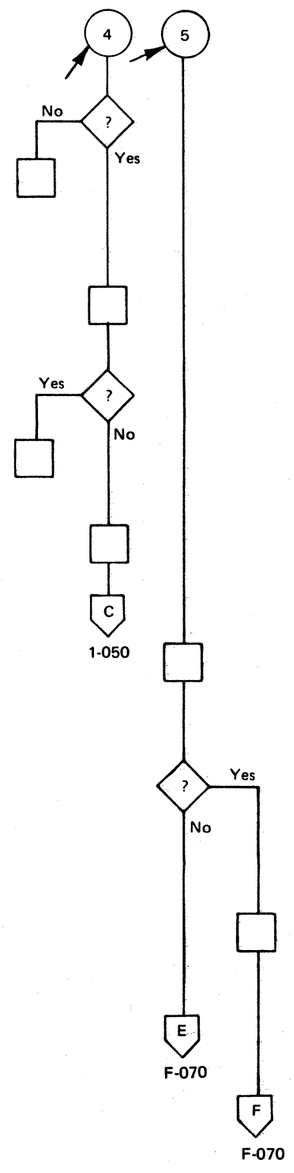
Modify the CDS as directed by the CDS Writer

Set up:

1. Address/Data switches "B" – "E" = DDDD.
2. Function Select switch = Register Address
3. CE jumper installed – see the CDS description in the RPL section of this FETMM (Volume I, SY27-0208).

Read the DCM from Diskette track 9.

See the IFT descriptions in the RPL section of this FETMM (Volume I, SY27-0208).



Was the load successful?

Hard stop with sequence number in the display register. See Note.

Execute the IFTs as directed from the control panel.

Any errors?

See Note.

End the IFTs and re-IPL for normal operation.

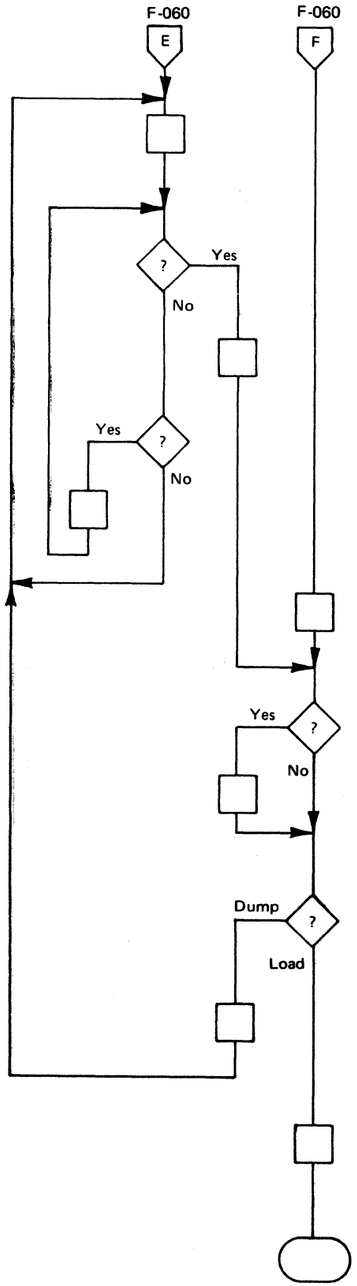
Load Program 2

Begin execution of load program 2.

Did the local controller (Host CPU) initiate the IPL? (Register X'6B' bit 0.3 will be on)

Condition the SDLC line set to communicate with the local controller.

REMOTE IPL SEQUENCE (PART 3 OF 3)



Condition the SDLC line set to monitor for a SIM SDLC instruction from the local controller. (The local NCP issues the SIM to the remote NCP after the host processor issues a Load Initial.)

Was a SIM SDLC instruction received?

Disable all other lines.

Does the received SDLC message require a response?

Respond with 'IPL required' (RQI) to local controller.

Receive the SIM SDLC instruction from the local controller.

Does the remote controller have OBR records to send to the host processor?

Send the OBR records to the local controller which passes them to the host processor.

Should load program 2 execute a "dump" or a "load"?

Dumper

The "dumper" handles the transfer of dump data from the remote controller to the local controller. The local NCP sends the "dump data" to the host processor.

Loader

The "loader" handles the transfer of the remote NCP from the local controller to the remote controller.

Load program 2 turns control over to the remote NCP once the remote NCP is loaded.

OBR (Out board Recorder)

The OBR is an error message that load program 1 stores in remote-controller storage locations 'X0020' – X'0034'. Load program 2 transmits the OBR message to the host processor (via the local controller) before the host CPU transmits the remote-NCP (via the local controller) to the remote controller.

Remote Storage Locations	*Field Definitions*
00020-00021	All zeros
00022-00023	OBR Type: X'2105'=3705-80
00024-00025	Input X'7D' (CCU Check Register) bit 1.3=1 (IPL Diskette controller error) bit 1.4=1 (Diskette media error—replace the Diskette)
00026-00027	Input X'76' (Adapter Level 1 Interrupt Request)
00028-00029	Input X'7E' (CCU Level 1 Interrupt Request)
0002A-0002B	Input X'79' (Utility Register)
0002C-0002F	Input X'74' (Lagging Address Register)
00030-00034	Level 0 Instruction Address Register

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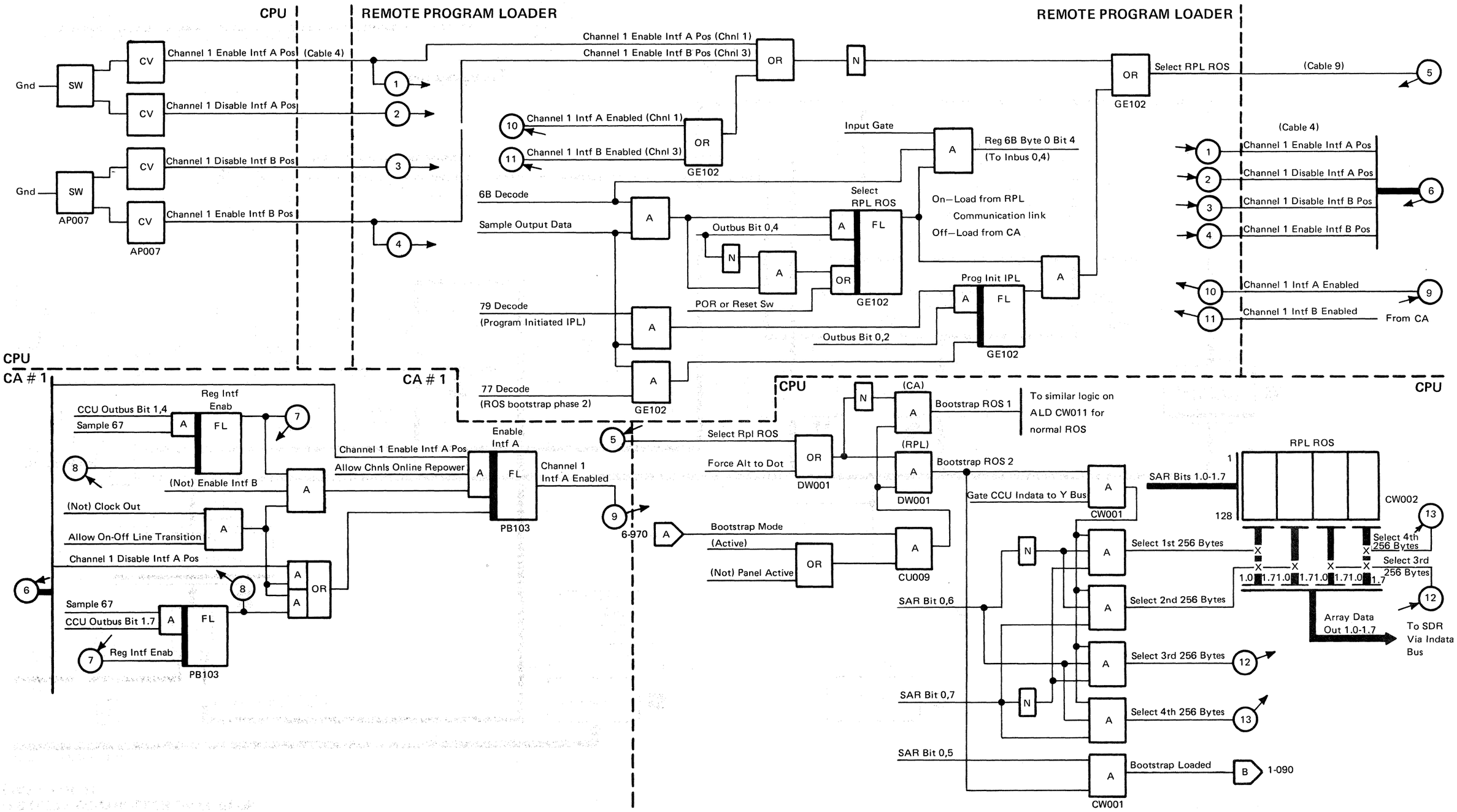
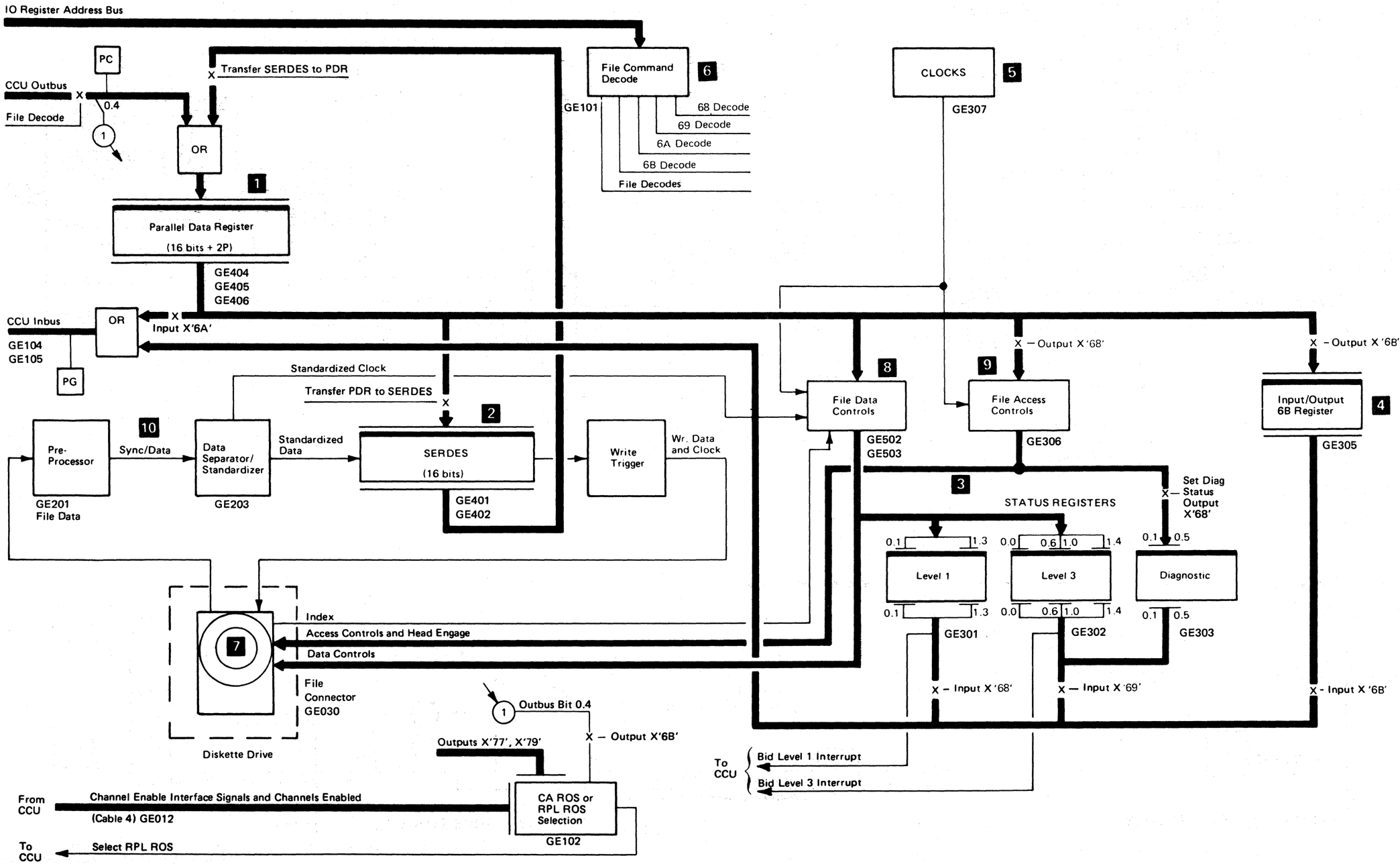
RPL ROS SELECTION

FOR RPL WITH A CA TYPE 1 OR 4



DISKETTE CONTROLLER DATA FLOW (PART 1 OF 2)



DISKETTE CONTROLLER DATA FLOW (PART 2 OF 2)

1 Parallel Data Register

The parallel data register (PDR) is an 18 bit register (16 data bits and 2 parity bits) that is used for all data going to or coming from the CCU. The PDR is checked for odd parity only when the CCU Outbus is gated into it.

When any file command is decoded, the data on the CCU Outbus is set into the PDR. The data is then gated to the proper logic according to the particular file command that was decoded.

During read or write operations, the PDR is used to buffer data between the CCU and the SERDES.

2 SERDES

The SERDES provides bit serialization/deserialization operations on the file read or write data. SERDES is a group of 16 'flip-flops' that receive data from the Diskette to be sent to the CCU via the PDR or it receives data from the CCU via the PDR to be written onto the Diskette.

3 Status Registers

The status registers store information pertinent to the controller operations. These registers are:

A. Level 1 Status Register
   These two conditions cause a Level 1 Interrupt.
   1. Outbus parity error
   2. Write operation and Write not enabled

B. Level 3 Status Register
   These four conditions cause a Level 3 Interrupt.
   1. Interrupt on Index
   2. Data Service
   3. Motor/Media Protect
   4. I/O Overrun

C. Diagnostic Status Register
   1. In Sync
   2. Access 0 status
   3. Access 1 status
   4. Access 2 status
   5. Access 3 status
   6. Head Engage Latch

4 Input/Output X'6B' Register

The Input/Output X'6B' register is used to store information required during IPL and program load phases. This information is:

A. Dump requested
B. Control program initiated IPL
C. Host initiated IPL

5 Clock

For the 3705-80 clocking for the Diskette controller is derived from the CCU clock 62.5ns pulses.

6 File Command Decode

The file command decode circuitry decodes data placed on the I/O Register Address Bus by the CCU into input or output commands. These commands are used by the Diskette controller to move information between the controller and the CCU. This information may be data or control information.

7 Diskette

The Diskette is a read only storage medium used by the remote 3705-80. The IPL loader and diagnostic programs are stored on the Diskette.

8 File Data Controls

The file data controls permit data to be read from or written on the Diskette (i.e. head engage latch, index recognition, and read and write clocking).

9 File Access Controls

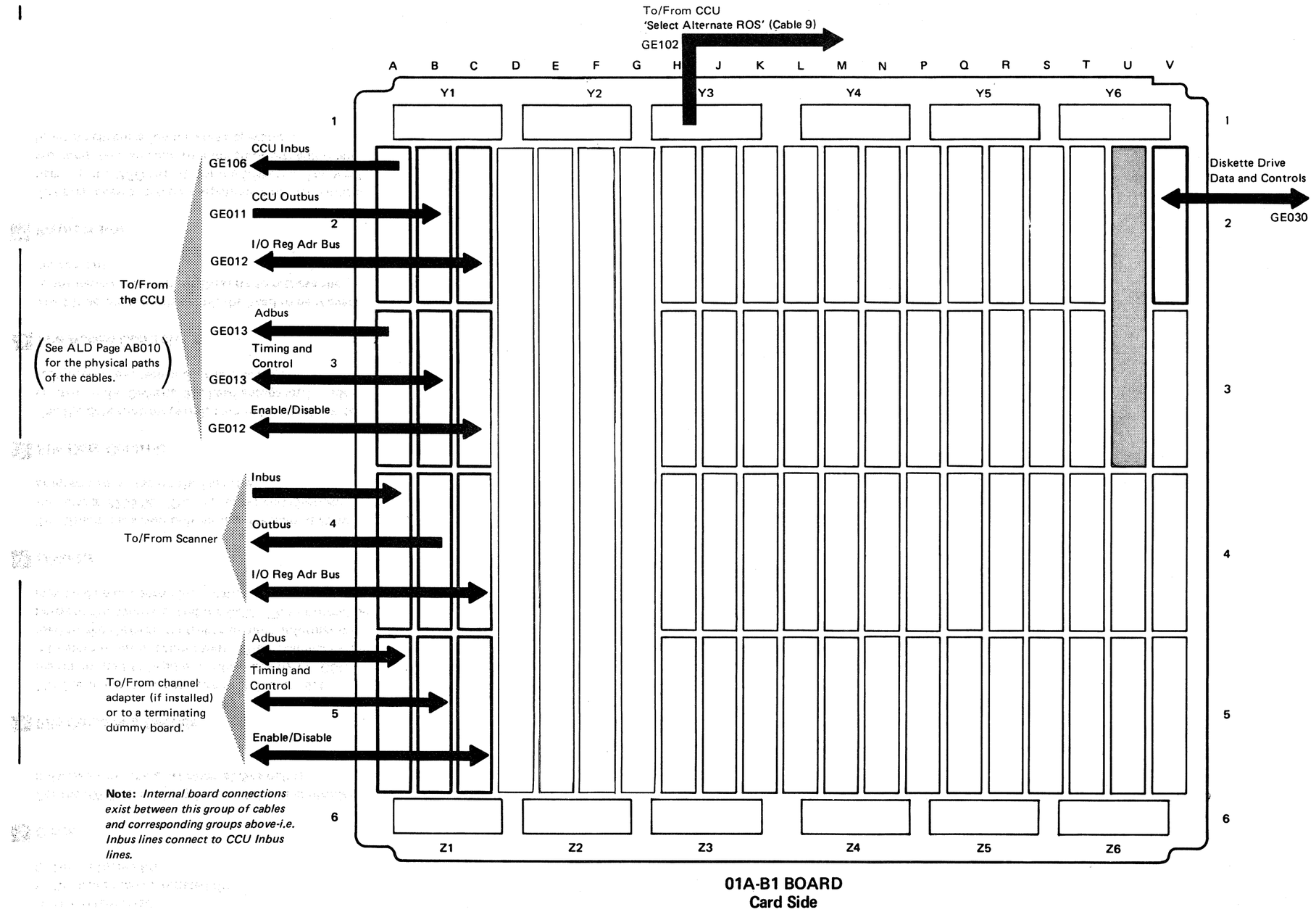
The file access controls permit the head to be moved to the desired track on the Diskette to retrieve the desired data.

10 Preprocessor

The preprocessor and data separator/data standardizer make up the VFO circuits for the Diskette. The VFO separates the read data from the clock bits and establishes synchronization on a read operation.

3505-80 DISKETTE CONTROLLER CARD LOCATIONS AND FUNCTIONS

Card Location	*Card Code*	*Card Function*	*ALD Page*
01A-B1D2	CE51	Instruction decode Alternate IPL selection 62.5ns clocking for 3705-80 Models M80–M84 Inbus Dot and powering	GE101 GE102 GE103 GE104-7
01A-B1E2	4997	SERDES Sync decode Outbus parity checking Buffer Byte 0 Buffer Byte 1	GE401-2 GE402 GE403 GE404-5 GE405-6
01A-B1F2	CE50	Level 1 status register Level 3 status register Diagnostic status register Status reset-I/O overrun Input and Output X'6B' Access drive Timing clocks	GE301 GE302 GE303 GE304 GE305 GE306 GE307
01A-B1G2	4998	I/O common controls Pulse gating and timing Diskette controls Count and SERDES tag Motor and Media Protection Output sample	GE501 GE502 GE503 GE504 GE505 GE506
01A-B1U2	3994	Pre-processor Phase discriminator Data separator and standardizer	GE201 GE202



Note: *Internal board connections exist between this group of cables and corresponding groups above-i.e. Inbus lines connect to CCU Inbus lines.*

01A-B1 BOARD
Card Side

DISKETTE FORMAT

Track Assignments

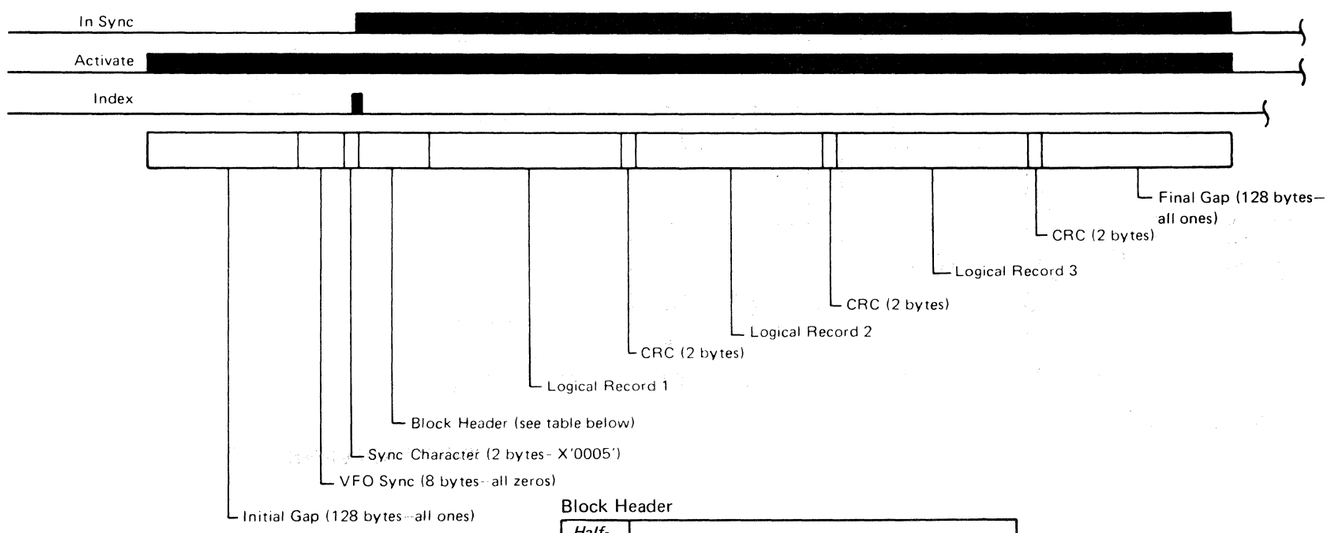
The Diskette tracks are assigned for use as specified in the following table.

3705-80

Track	*Assignment*
0	Load Program 1 — controls IPL execution.
1-5	Initial Test — sections 1-2
6-7	Load Program 2 — controls the communication to load the control program or dump the 3705-80 to the host processor.
8	IFT loader/CDS writer.
9	DCM (diagnostic control module).
10	CDS (configuration data set) — defines the machine configuration executing the IFT.
11	Load Program 1 (duplicate of track 0).
12-13	Load Program 2 (duplicate of tracks 6 and 7).
14	Reserved.
15-16	Dump data (Load Program 1 store the upper 8K of main storage onto these tracks if a dump is requested via the control panel switches).
17	Dump subroutine.
18	Reserved.
19-25	CCU IFT — sections 1-3
26-27	Storage IFT — sections 1-2
28	Reserved
29-42	Type 2 scanner IFT — sections 1-7
64	Reserved
65-66	Panel line test — sections 1-2
67	Type 1 CA IFT Type 4 CA IFT — sections 1-2
76	Reserved

Track Format

Each track contains one record which may be subdivided into three smaller logical records. Each logical record has its own CRC character. These CRC characters are accumulated into the final CRC at the end of the track record.



Block Header

Half-word	*Description*
1	Track ID (X'0000' through X'004C')
2	Control Information
3	Reserved
4	Reserved
5	Logical Record 1 (storage address)
6	Logical Record 1 (storage address)
7	Logical Record 1 (byte count—twos complement)
8	Program version level (EBCDIC)
9	Logical Record 2 (storage address)
10	Logical Record 2 (storage address)
11	Logical Record 2 (byte count—twos complement)
12	Program ZAP number
13	Logical Record 3 (storage address)
14	Logical Record 3 (storage address)
15	Logical Record 3 (byte count—twos complement)
16	Block header CRC

ACCESS DRIVE

A counter that can be stepped either forward or backward controls the access drive. Output X'68' with bits 1.1 and 1.2 on steps the counter forward; bit 1.1 on and 1.2 off steps the counter backward. Each Output X'68' causes the counter to step one count either forward or backward.

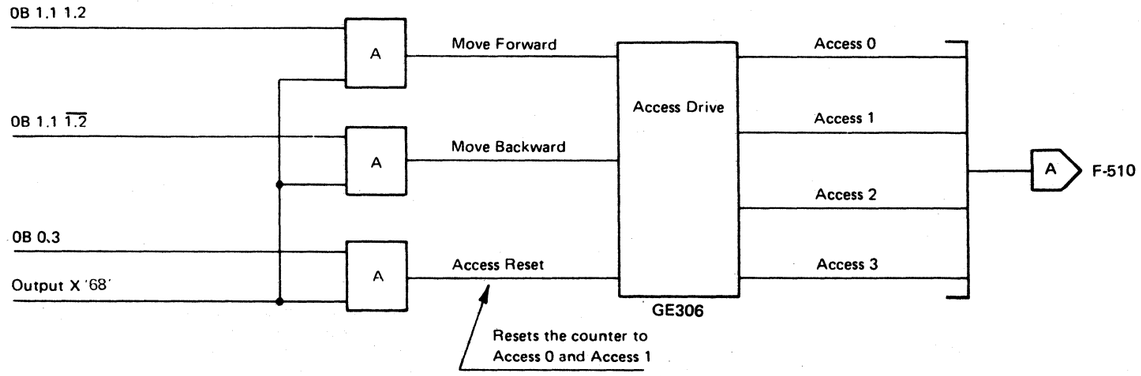
The output lines from the counter drive the stepper motor. Two adjacent output lines are active for each access operation.

The stepper motor is protected by dropping the current to it if the access is held active longer than the time required to detect two index pulses. Because of this protection, the control program should energize the motor after index time and hold it energized for approximately 150 ms.

The head should not be engaged or disengaged during accessing operations, but can be engaged before or after the access. The head automatically disengages within three revolutions (498 ms) after a read, write, access, or head engage operation unless the operation is re-initiated. Because of the automatic head disengaging, the head should be reengaged before each read or write operation.

Recalibration

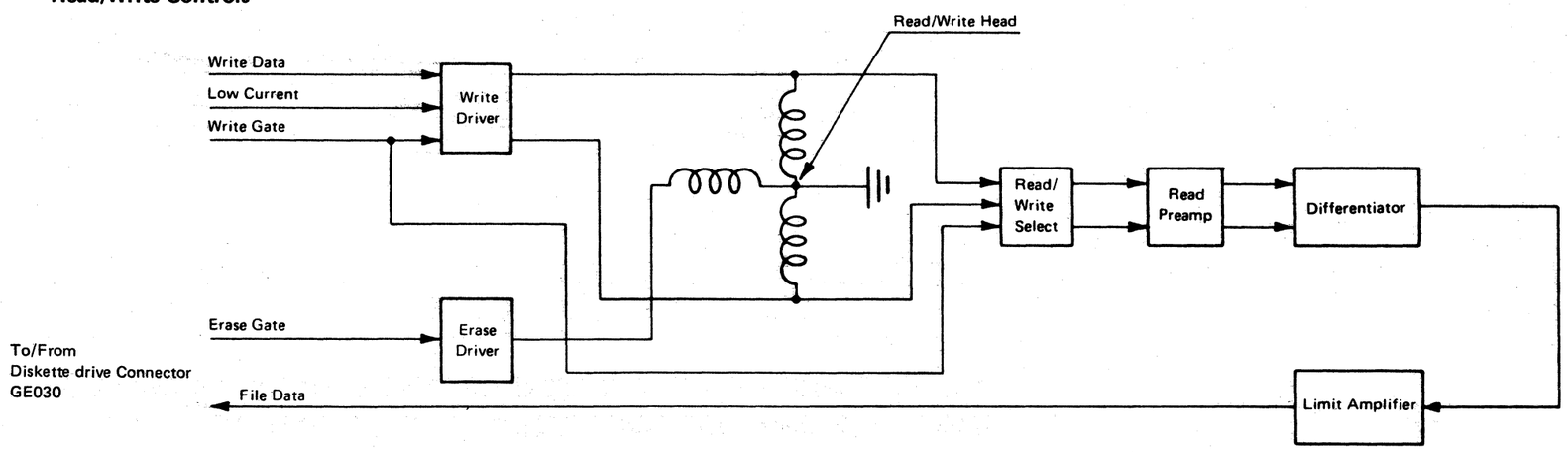
The control program recalibrates the access by executing an Output 'X68' instruction with bit 0.3 on. Bit 0.3 resets the counter to condition output lines 'access 0' and 'access 1'. After the reset X'68', the control program executes eighty X'68' instructions with bit 1.1 on and 1.2 off (reverse). This sets the head back to track 0 (home position).



Track	0	1	2	3	4	5	6	74	75	76
Lines Energized: Access 0	X			X	X				X	X
Access 1	X	X			X	X				X
Access 2		X	X			X	X	X		
Access 3			X	X			X	X	X	

The motor is at phase 0 when the read/write head is at track 0 or at any track evenly divisible by four.

Read/Write Controls



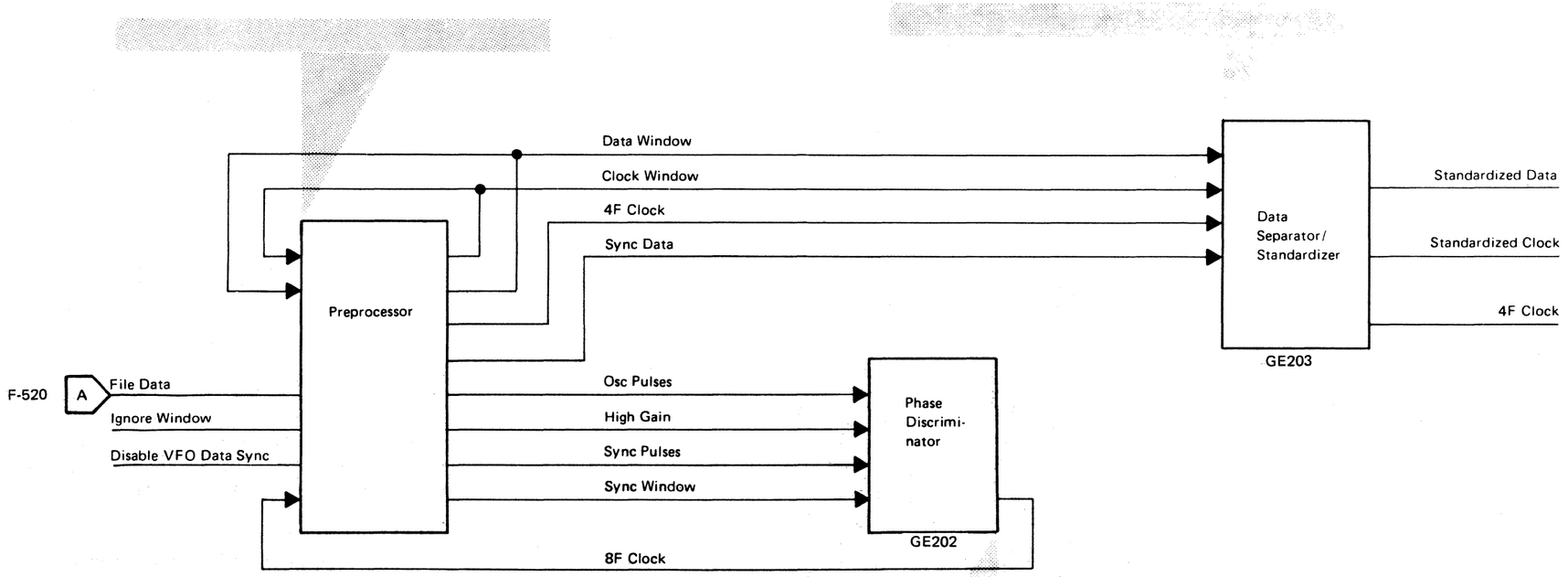
VARIABLE FREQUENCY OSCILLATOR OPERATION AND TIMING

Operation

Data is recorded on the Diskette using frequency modulation (double frequency) coding that makes the data self clocking. The data read from the Diskette contains the data bits with a clock bit between the data bits. The variable frequency oscillator (VFO) separates the data bits and clock bits and standardizes the data stream with a uniform time period between the data pulses.

This group of logic circuits generates control signals for the phase discriminator and data separator/standardizer. The input signals, commands, and phase discriminator outputs are combined to ensure proper VFO operation.

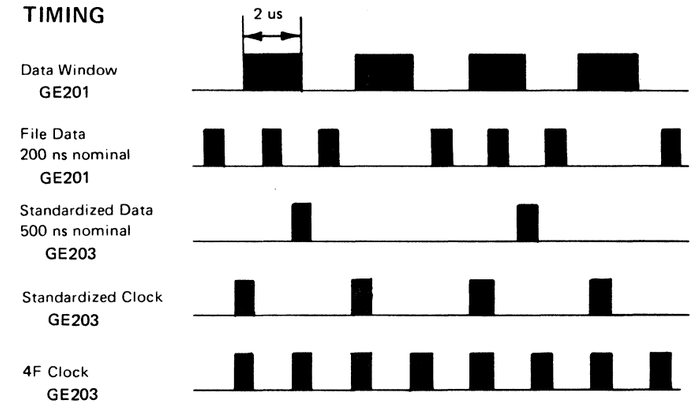
The data separator separates the data stream of clock and data bits ('sync data' line) into a stream of clock bits and a stream of data bits. SERDES deserializes the data bits before they are gated into the parallel data register (PDR).



VFO CARD LOCATION: B1U2 (3705-80)

A feedback loop controls the phase discriminator frequency so that the phase discriminator frequency matches the frequency of the clock bits on the 'sync data' line.

TIMING



Data Synchronization

The data record (one per track) is formatted so that it begins with 128 bytes of all one bits followed by eight bytes of all zero bits followed by a two byte sync character (X'0005'). When the index pulse causes 'activate' to become active, 'ignore window' also becomes active. At least 16 of the 64 standardized clock pulses must be read (in a continuous string without one bits) before the 'ignore window' line can become inactive.

When the two byte sync character is read, the 'in sync' latch is set and remains set until 'activate' becomes inactive.

See Page F-300 for a description of the track record format.

INPUT AND OUTPUT INSTRUCTIONS

The 3705-80 remote program loader uses input and output instructions to transfer data to and from the Diskette and to control the Diskette controller.

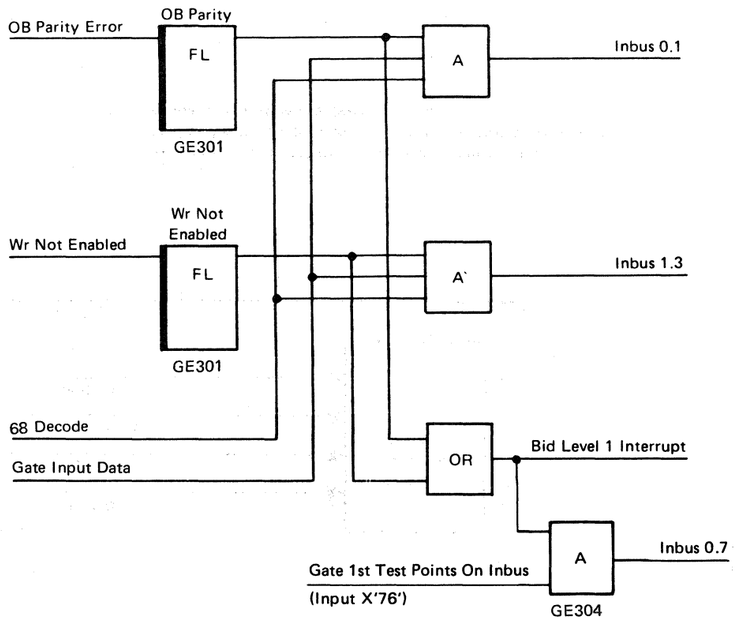
The remote program loader uses the following instructions:

- Input X'68' (Level 1 Status)
- Input X'69' (Level 2 Status)
- Output X'68' (Control)
- Output X'69' (Read/Write)
- Input X'6A' (Parallel Data Register)
- Output X'6A' (Parallel Data Register)
- Input X'6B' (Control Program Load Register)
- Output X'6B' (Control Program Load Register)

Input X'68' (Level 1 Status)

Input X'68' transfers the condition of the 'level 1 status' latches into a CCU general register. The 3705-80 control program determines the cause of a Diskette controller level one interrupt with this instruction.

	3705-80		
Bit	*Card Location*	*ALD Page*	*Function*
0.1	B1F2	GE301	Indicates an outbus parity error.
1.3	B1F2	GE301	Indicates that a write command was received by the file adapter when write was not enabled.



Error Detection

The control program detects read, write, and CRC errors in the CCU.

Outbus Parity Error: Each time the PDR (parallel data register) is loaded from the CCU Outbus, the parity is checked. If even parity is detected, a level 1 status latch is set. When the control program executes an Input X'68' in response to the level one interrupt caused by the error, bit 0.1 is transferred to the CCU general register.

Write Not Enabled: This error is detected when a Write command (Output X'68') is decoded while the write capability is disabled.

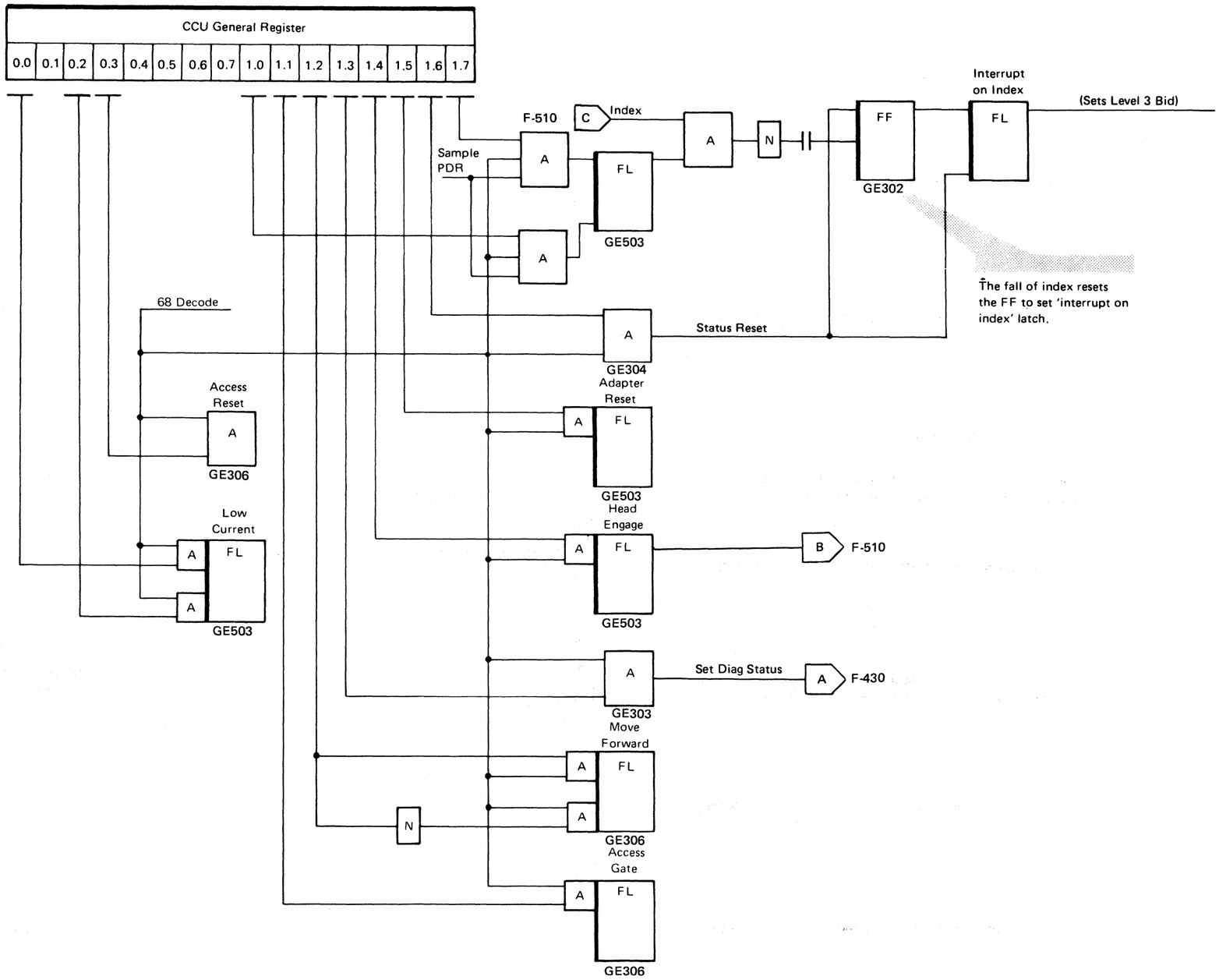
To enable the write capability, the 3705-80 must not be initialized or the wire jumper must be installed, see ALD Page GE501.

Output X'68' (Control)

Output X'68' (Control) prepares the Diskette for subsequent read and write operations. The 3705-80 control program uses this instruction to control the access mechanism, engage the head, set the write current, and reset the Diskette controller.

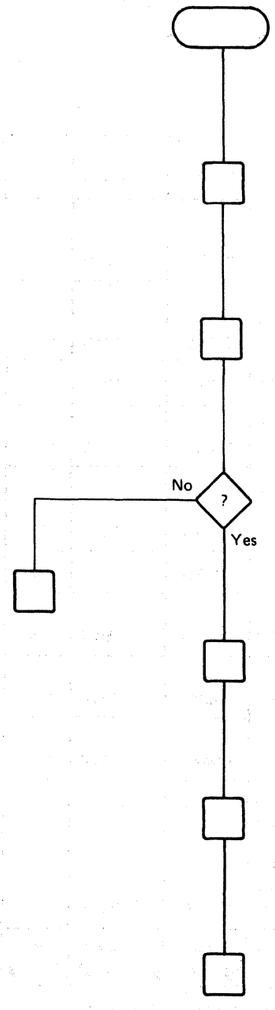
Summary of Output X'68' Control Functions

Bit	*Card Location*	*ALD Page*	*Function*
0.0	B1G2	GE503	Sets low current latch for writing. This bit must be on when writing tracks 44 through 76. This bit must be off when writing tracks 0 through 42, and may be at either level for track 43.
0.2	B1G2	GE503	Resets low current latch for writing.
0.3	B1F2	GE306	Resets the head access counter to 'access 0'.
1.0	B1G2	GE503	Resets the 'interrupt on index' latch.
1.1	B1F2	GE306	Moves the head one track.
1.2	B1F2	GE306	On causes the head to move forward; off causes the head to move backwards.
1.3	B1F2	GE303	Sets the 'diagnostic status' latches.
1.4	B1G2	GE503	Sets the 'head engage' latch.
1.5	B1G2	GE503	Resets all registers, latches, and counters except the head access counter.
1.6	B1F2	GE304	Resets the level 1 and level 3 interrupt latches and all status latches.
1.7	B1G2	GE503	Allows a level 3 interrupt when the index pulse is detected.



Use of Input/Output Instructions During Interrupts

Level 1 Interrupt



The Diskette controller causes a 'bid level 1 interrupt' upon detection of a hardware error.

The control program branches to the level 1 handler.

The control program executes Input X'76' to determine which adapter, scanner, or controller has requested the level 1 interrupt.

Is bit 0.7 on? If on, the failure is in the Diskette controller.

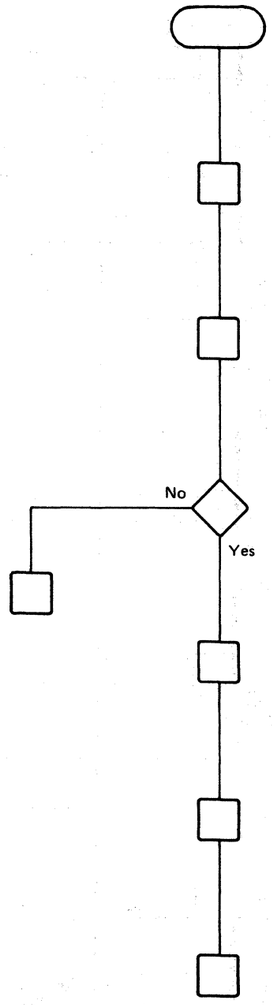
If off, the control program identifies the adapter or scanner bidding for the level 1 interrupt and then executes the proper input code.

The control program executes Input X'68' to get the Diskette controller level 1 status.

The control program executes Output X'68' with bit 1.6 on to reset the level 1 status registers and the level 1 bid.

The control program executes the error recovery procedure.

Level 3 Interrupt



The Diskette controller causes a 'bid level 3 interrupt'.

The control program branches to the level 3 handler.

The control program executes Input X'77' to determine the cause of the level 3 interrupt request (adapter, scanner, or CCU).

Is bit 1.1 on? If on, the interrupt request is from the Diskette controller.

If off, the control program identifies the adapter or scanner bidding for the level 3 interrupt and then executes the proper input code.

The control program executes Input X'69' to get the Diskette controller level 3 status.

The control program executes Output X'68' with bit 1.6 on to reset the level 3 status registers and the level 3 bid.

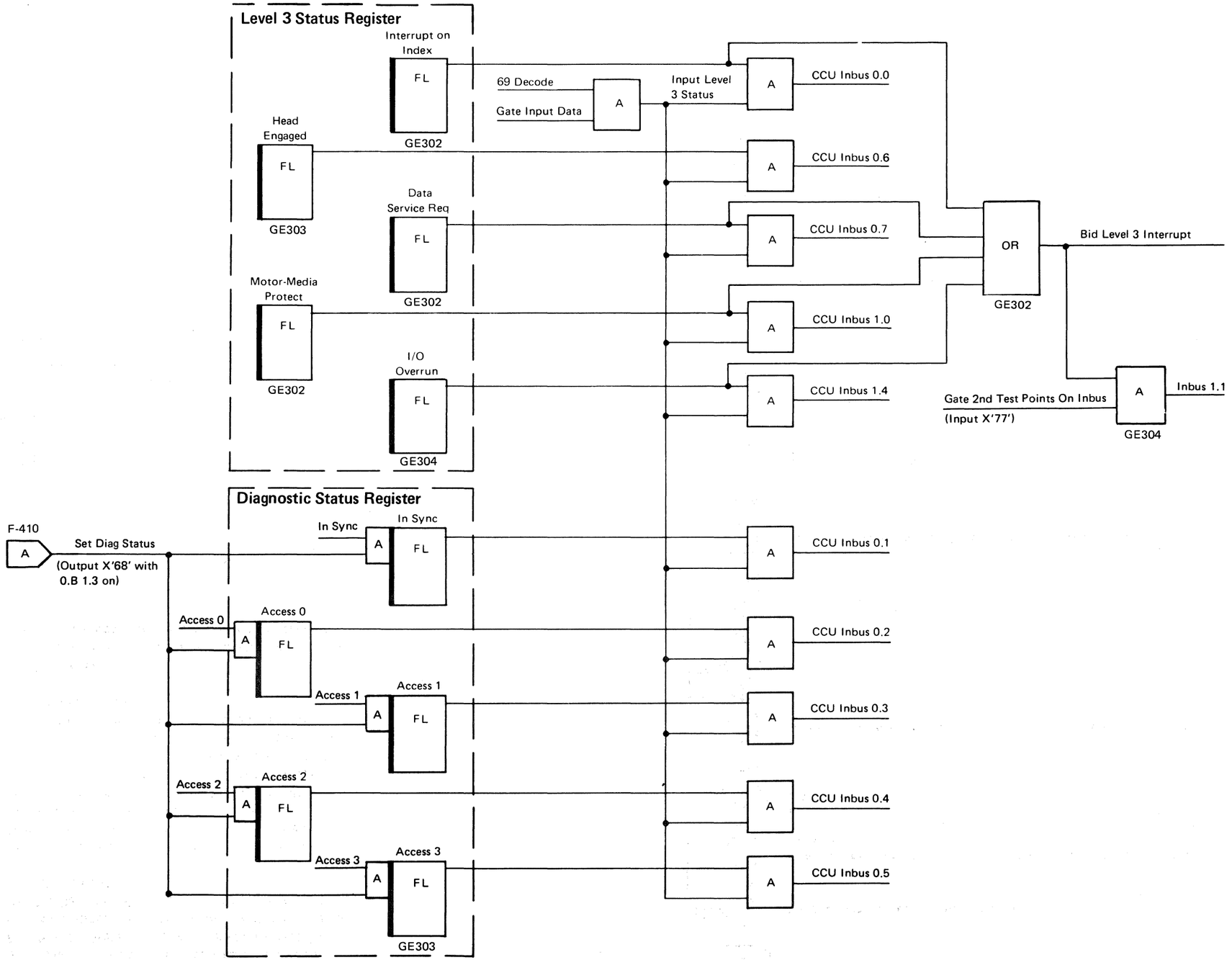
The control program executes the appropriate service routine.

Input X'69' (Level 3 Status)

This instruction transfers the contents of the level 3 status register and the diagnostic status register into a CCU general register. The 3705-80 control program uses this instruction to determine the cause of level 3 interrupts caused by the Diskette.

Summary of Input X'69' Bit Indications

Bit	*Card Location*	*ALD Page*	*Indication*
0.0	B1F2	GE302	The 'interrupt on index' latch is on.
0.1	B1F2	GE303	The controller is in sync on a read operation, (diagnostic).
0.2	B1F2	GE303	Access counter 'access 0' output active (diagnostic).
0.3	B1F2	GE303	Access counter 'access 1' output active (diagnostic).
0.4	B1F2	GE303	Access counter 'access 2' output active (diagnostic).
0.5	B1F2	GE303	Access counter 'access 3' output active (diagnostic).
0.6	B1F2	GE303	The 'head engaged' latch is on.
0.7	B1F2	GE302	'Data service request' is active.
1.0	B1F2	GE302	The head has been automatically disengaged or the current has been dropped from the access motor.
1.4	B1F2	GE304	'Character service request' has been presented twice without an intervening X'6A' instruction.



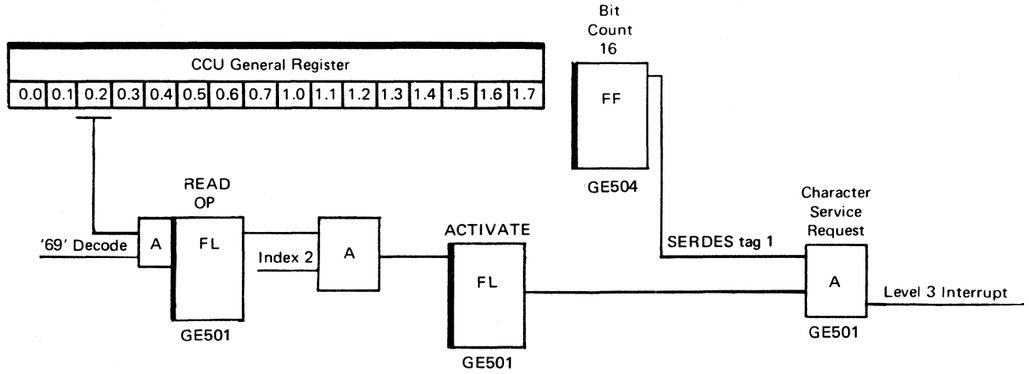
Output X'69' (Read/Write) (Part 1 of 2)

Output X'69' (Read/Write) is used to initiate either a read (bit 0.2 on), or a write (bit 0.1 on) operation. The head must be positioned to the correct track and engaged prior to the read or write operation initiation.

Diskette Read

Before executing the Output X'69' instruction, the control program must ensure that the head is positioned at the proper track (Output X'68') and that the head is engaged (Output X'68').

After a 60 ms head settling delay, the Output X'69' (Read) instruction is executed to initiate the read operation. When the index pulse following the Output X'69' is detected, 'activate' becomes active and data from the disk is shifted through SERDES until the 'bit count 16' flip-flop is turned on (SERDES counted 16 bits). A character service level 3 interrupt is requested and the halfword in SERDES is loaded into the PDR. The control program transfers the data in the PDR into a CCU general register via an Input X'6A' (Parallel Data Register) instruction.

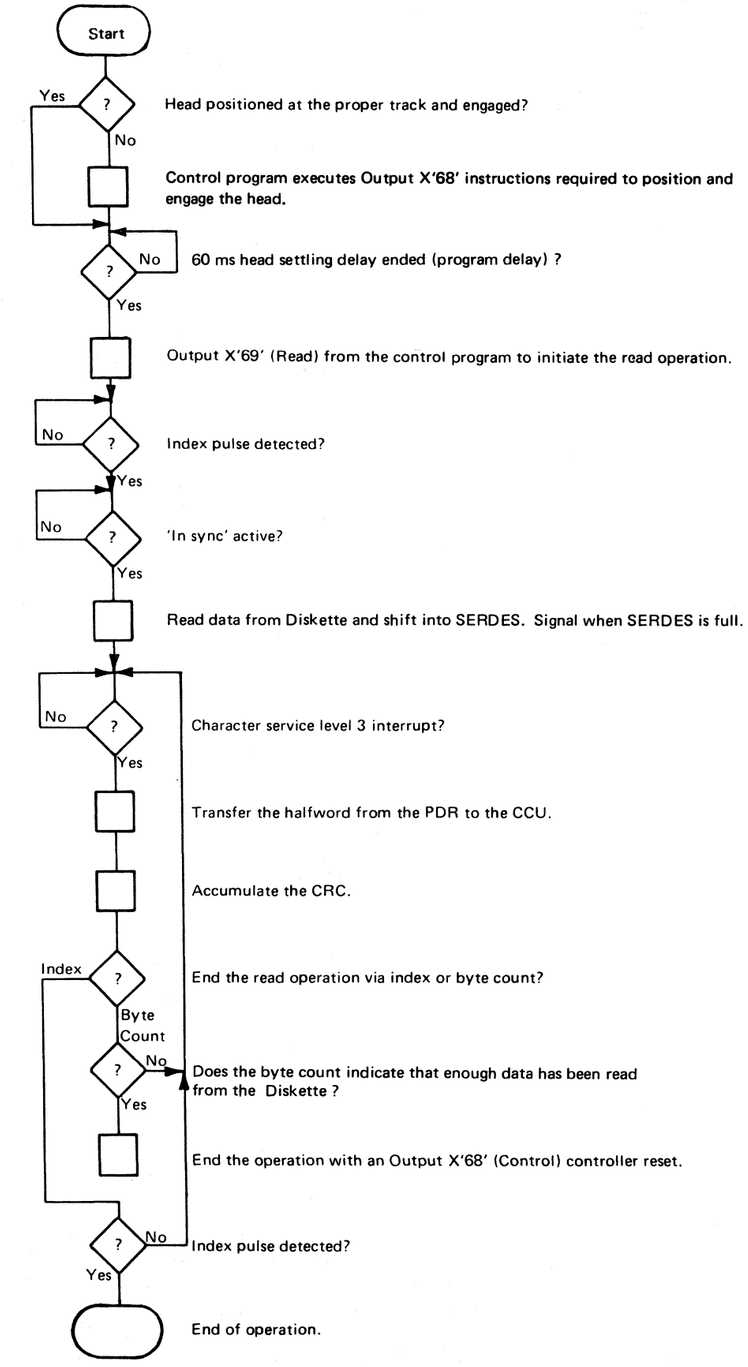


The control program accumulates a CRC character for the data using the CRC accumulation circuits described on Page 6-840 in Volume 2 of the 3705-80 the *3705-80 Communications Controller Theory-Maintenance* manual, SY27-0209. The CRC is accumulated in the same way as an SDLC CRC.

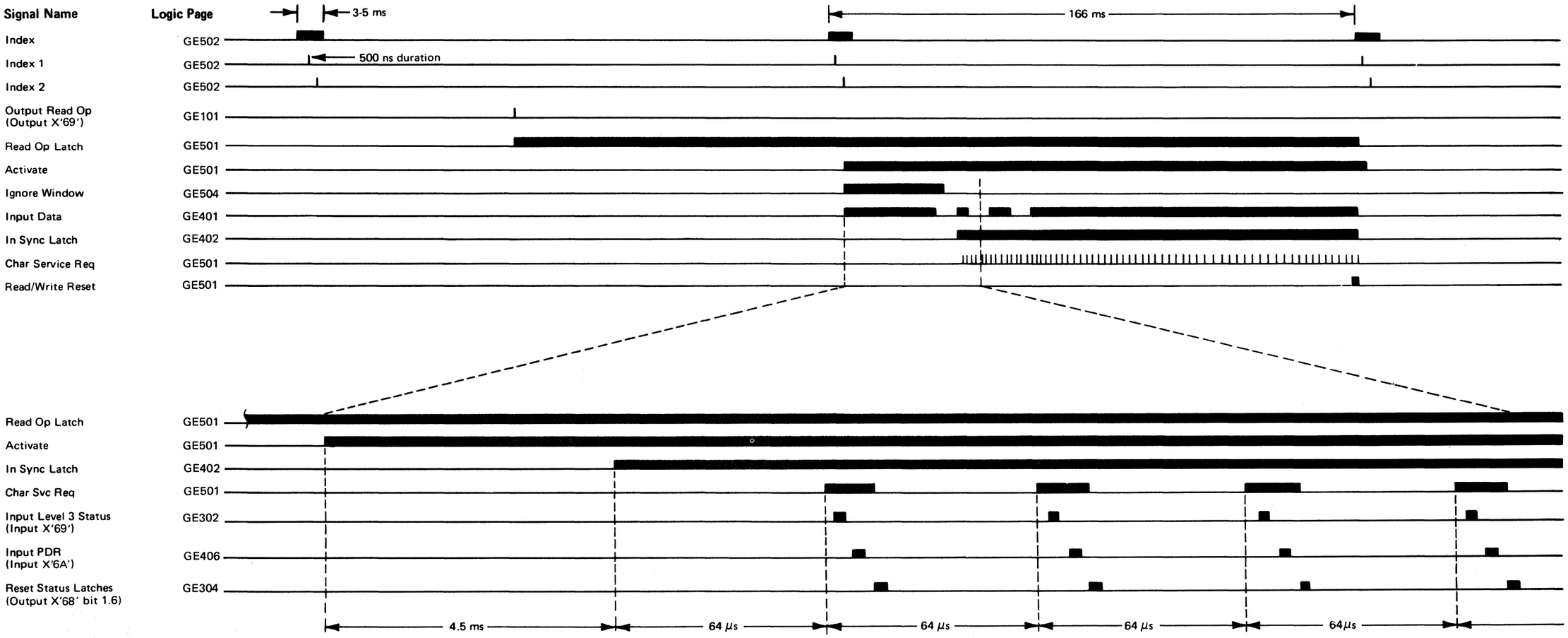
The read operation is ended with the next index pulse. However, ending the read operation this way transfers the GF (final gap) into storage. An alternate method to end the read operation after transferrring the CRC is to keep a current byte count to compare with the byte count(s) in the block header. When the desired number of bytes has been transferred, the control program ends the read operation with an adapter reset, Output X'68' (Control) bit 1.5 on.

Read Example

The flow chart contains a logical representation of the read operation and does not represent the actual operation.



Output X'69' (Read Operation)
(Part 2 of 2)



Diskette Write (Part 1 of 2)

The diskette is protected from inadvertent writing by blocking Diskette write operations unless (1) a CE jumper is installed between B1G2S02 and B1G2D08 (GE501), or (2) the 3705-80 is not initialized (IPL phase one, two, or three). An attempt to write when one of these conditions is not satisfied results in a program level 1 interrupt to signal the 'write not enabled' error to the control program.

When data is to be written, the control program must ensure that the read/write head is at the proper track and engaged. After engaging the head, the controlling program must delay for 60 ms to allow the head to settle before executing the Output X'69' (Write) instruction with bit 0.1 on to initiate the write operation.

The Diskette controller requests a character service level 3 interrupt immediately upon receiving the Output X'69'. The control program should respond to this interrupt by placing the first halfword (all ones) into the PDR via an Output X'6A' (Parallel Data Register) instruction. The Diskette controller transfers the halfword from the PDR into SERDES.

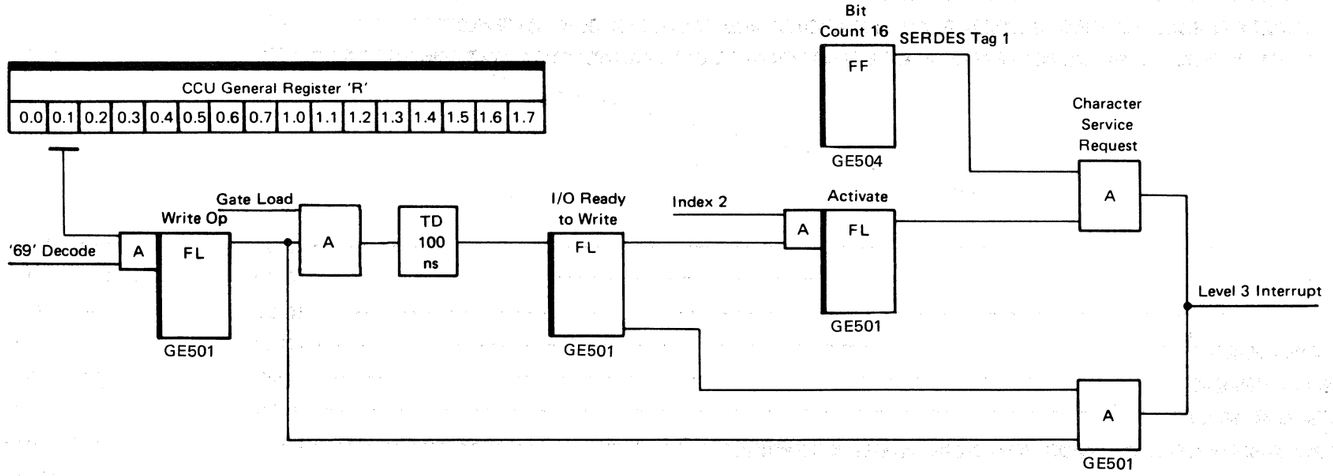
The index pulse signals the beginning of the track so that the data in SERDES is written serially on the Diskette. When 'bit count 16' turns on, a level 3 interrupt is requested so that the control program can transfer another halfword into the PDR.

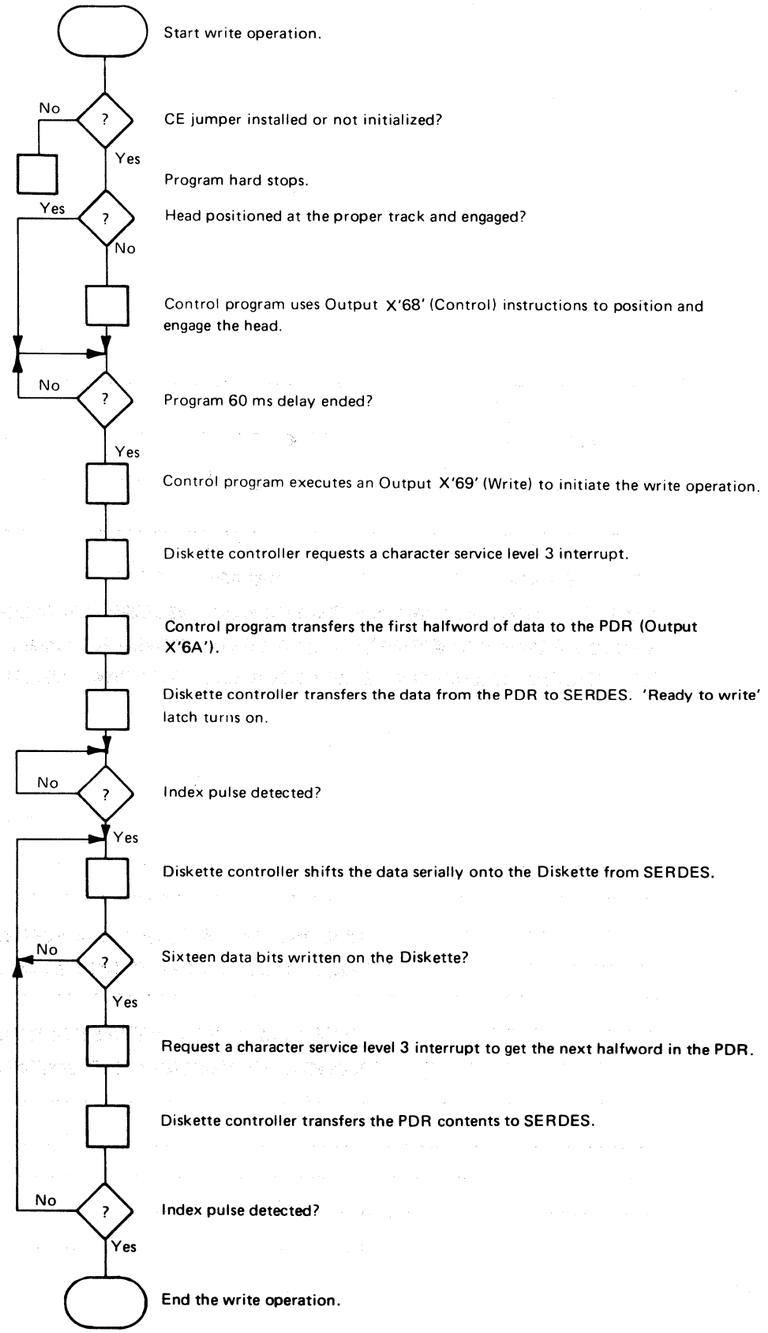
The control program must transfer data to the PDR in the correct track format.

GI (initial gap — 128 bytes, all ones)
VFO Sync (8 bytes, all zeros)
Sync Character (X'0005')
Block Header (32 bytes)
Data and CRC (data length varies not to exceed 4668 bytes, CRC is 2 bytes)
GF (final gap — minimum 128 bytes, all ones)

Write Operation Example

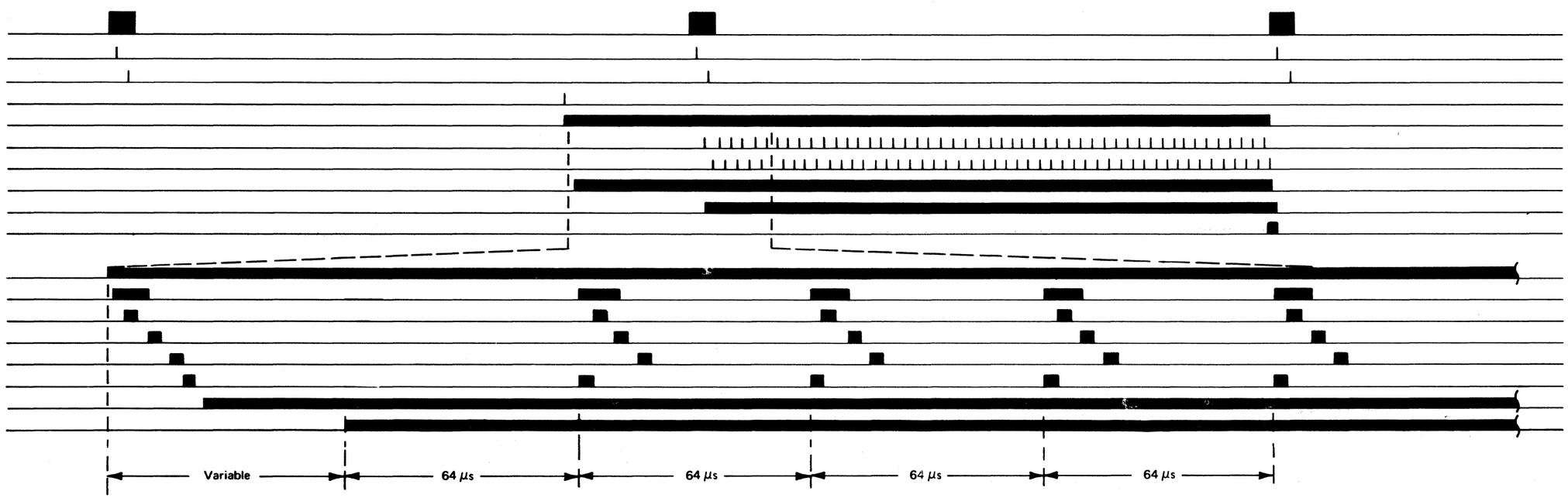
The flowchart contains a logical representation of the write operation and is not the actual method of writing on the Diskette.



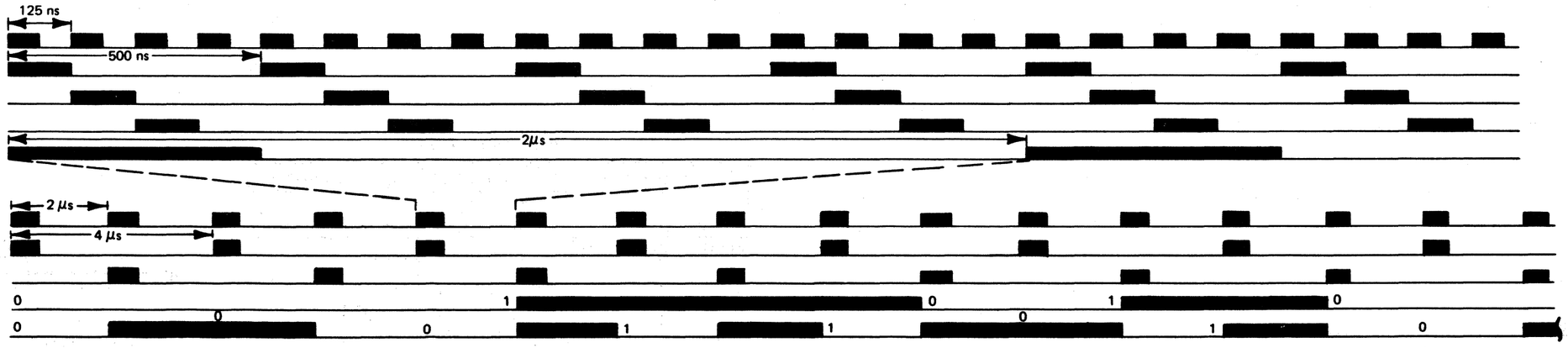


Output X'69' (Write Operation) (Part 2 of 2)

Signal Name	Logic Page
Index	GE502
Index 1	GE502
Index 2	GE502
Output write op (Output X'69')	GE101
Write Op Latch	GE501
Data Service Req	GE501
Output data (Output X'6A')	GE406
Ready to Write	GE501
Activate	GE501
Read/Write Reset	GE501
Write Op Latch	GE501
Char Sv Req	GE501
Input Lvl 3 Status (Input X'69')	GE302
Reset Status Latches	GE304
Output to PDR (Output X'6A')	GE406
Xfer PDR to SERDES	GE404
Ready to Write	GE501
Activate	GE501



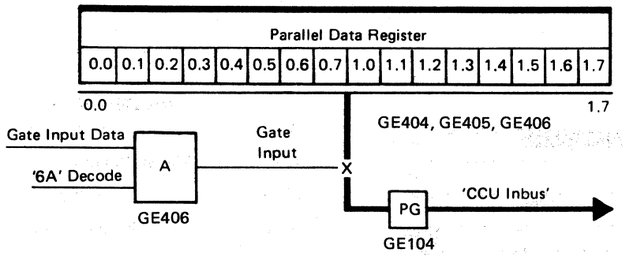
File 62.5 ns Clock	GE307
T1	GE307
T3	GE307
T4	GE307
WRP1 (Write Pulse 1)	GE307
WRP1	GE307
WR Data Pulse	GE307
WR Clock	GE307
(Data from SERDES 0)	GE402
Write Data (to Diskette drive)	GE402



For each transition in 'write data', current is switched in the read/write head causing a flux change on the diskette. Transitions every 4 µs (125 kHz) are zeros while transitions every 2 µs (250 kHz) are ones (see Page F-520).

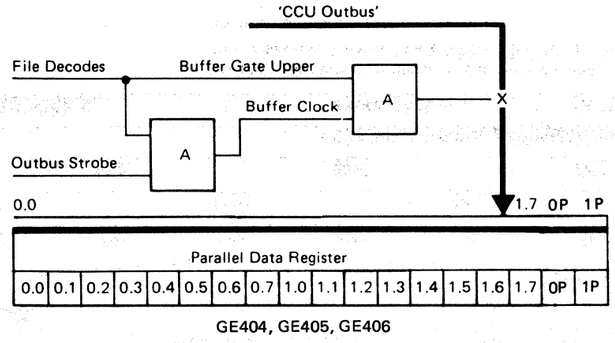
Input X'6A' (Parallel Data Register)

This instruction transfers the data read from the Diskette into a CCU general register.



Output X'6A' (Parallel Data Register)

This instruction transfers data from a CCU general register to the parallel data register. The control program transfers data to be written onto the Diskette controller via this instruction.



Output X'6B' (Input/Output Register)

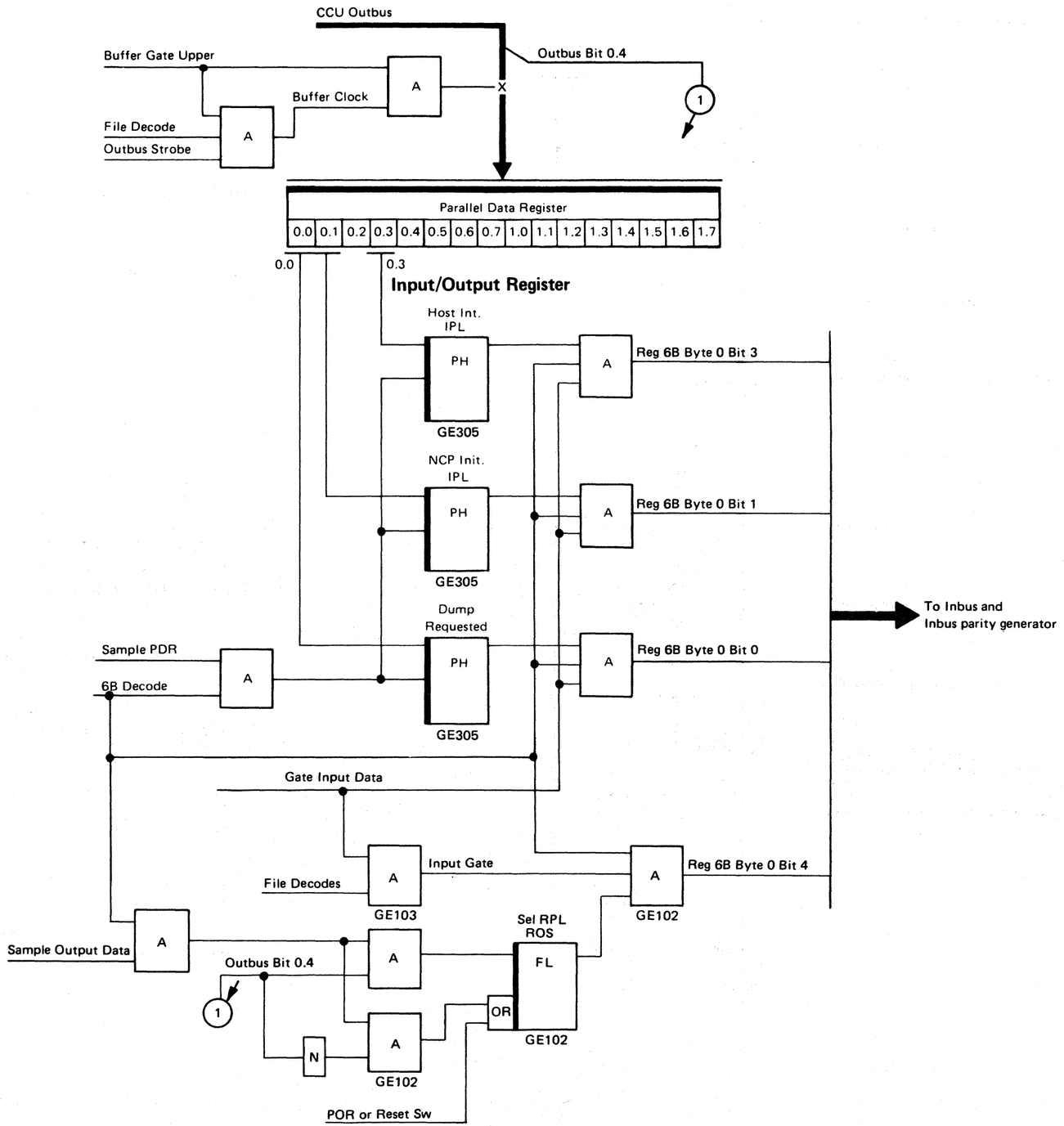
This instruction transfers bits 0.0 through 0.3 of a CCU general register to the input/output register. The data is loaded into the PDR and gated into the input/output register. This instruction also sets or resets the 'select RPL ROS' latch. This latch enables the control program to select the RPL ROS in the CCU when the control program initiates an IPL by executing an Output X'79' with bit 0.2 on.

The input/output register stores information used during IPL and control program load.

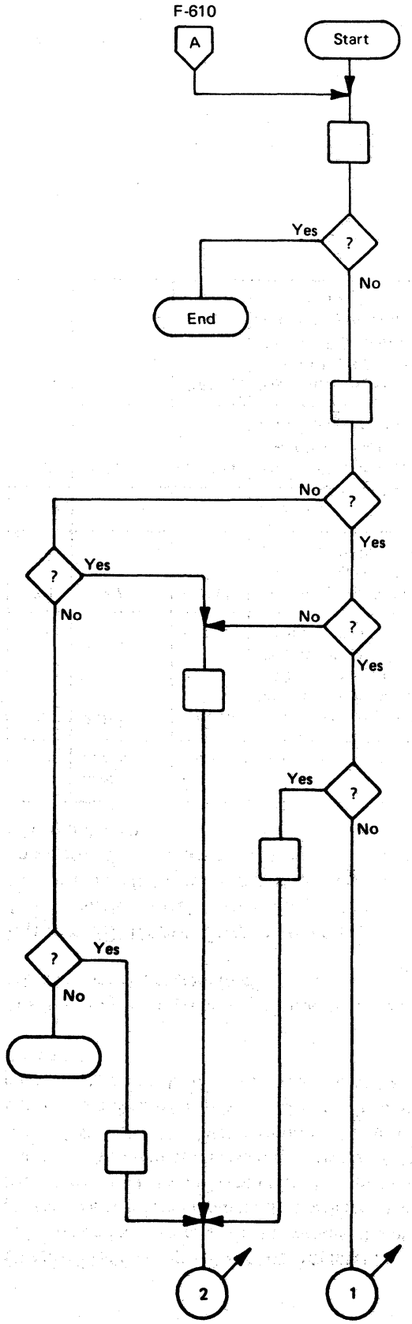
Input X'6B' (Input/Output Register)

This instruction transfers the contents of the input/output register to bits 0.0 through 0.3 of a CCU general register. This instruction also transfers the state of the 'select RPL ROS' latch.

Bit	*Card Location*	*ALD Page*	*Indication*
0.0	B1F2	GE305	The contents of storage should be preserved for a dump. This bit does not trigger the dump, the host or Load Program 1 retains control.
0.1	B1F2	GE305	The re-IPL was initiated by the control program. This bit is set by the controlling program.
0.2	–	–	Reserved.
0.3	B1F2	GE305	The re-IPL was initiated by the host CPU. This bit is set by the controlling program.
0.4	B1D2	GE102	The control program has set the 'select RPL ROS' latch to select the RPL ROS when an IPL is initiated by an output X'79' with bit 0.2=1.



Diskette Controller Diagnostic Approach for Read Failures



Use the RPL section in Volume 1 (SY27-0208) of this FETMM for detailed error analysis.

Failure fixed?

End of call.

Set up a continuous read — see the RPL section in Volume 1 (SY27-0208) of this FETMM.

Is '+ reset ignore window' present? Scope at B1E2P11 — logic GE402.

Does '+ standardized data' go up and down? Scope at B1E2P07 — logic GE407.

Is '— in sync' active? Scope at B1E2M05 — logic GE402.

Replace card at B1E2.

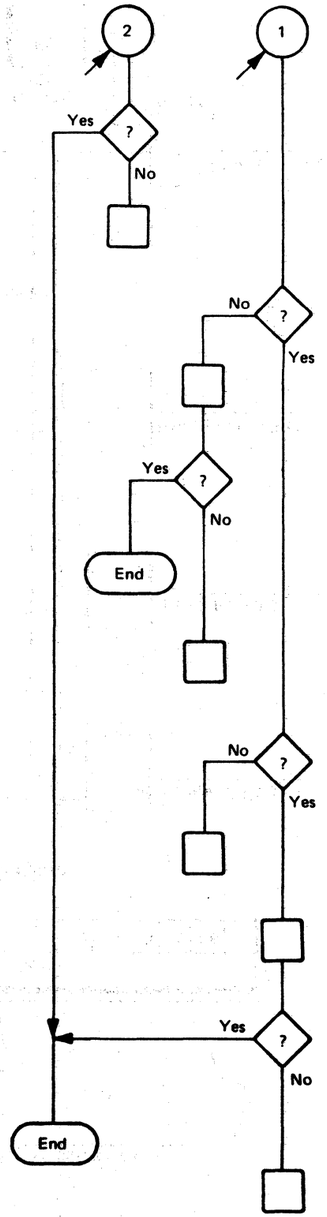
Is trouble a track identify failure?

Replace card at B1F2.

Does '+ file data' go up and down? Scope at B1U2B12 — logic GE201.

Check the driver card in the Diskette Drive (see Page F-520 and Page F-575).

Replace card at B1U2.



Failure fixed?

Check the Diskette drive adjustments.

Is '— SERDES tag 1' active? It should go minus every 64 μs. Scope B1G2B02 — logic GE504.

Replace card at B1G2.

Failure fixed?

End of call

Replace card at B1E2.

Is the read data incorrect as specified in the RPL section of Volume 1 (SY27-0208).

Failure is most likely a BCC error. Replace the Diskette.

Replace card at B1E2.

Failure fixed?

End of call.

Check Diskette drive adjustments.

DISKETTE DRIVE

Components

Diskette Drive Cover 1
The Diskette drive cover permits the insertion and removal of the Diskette.

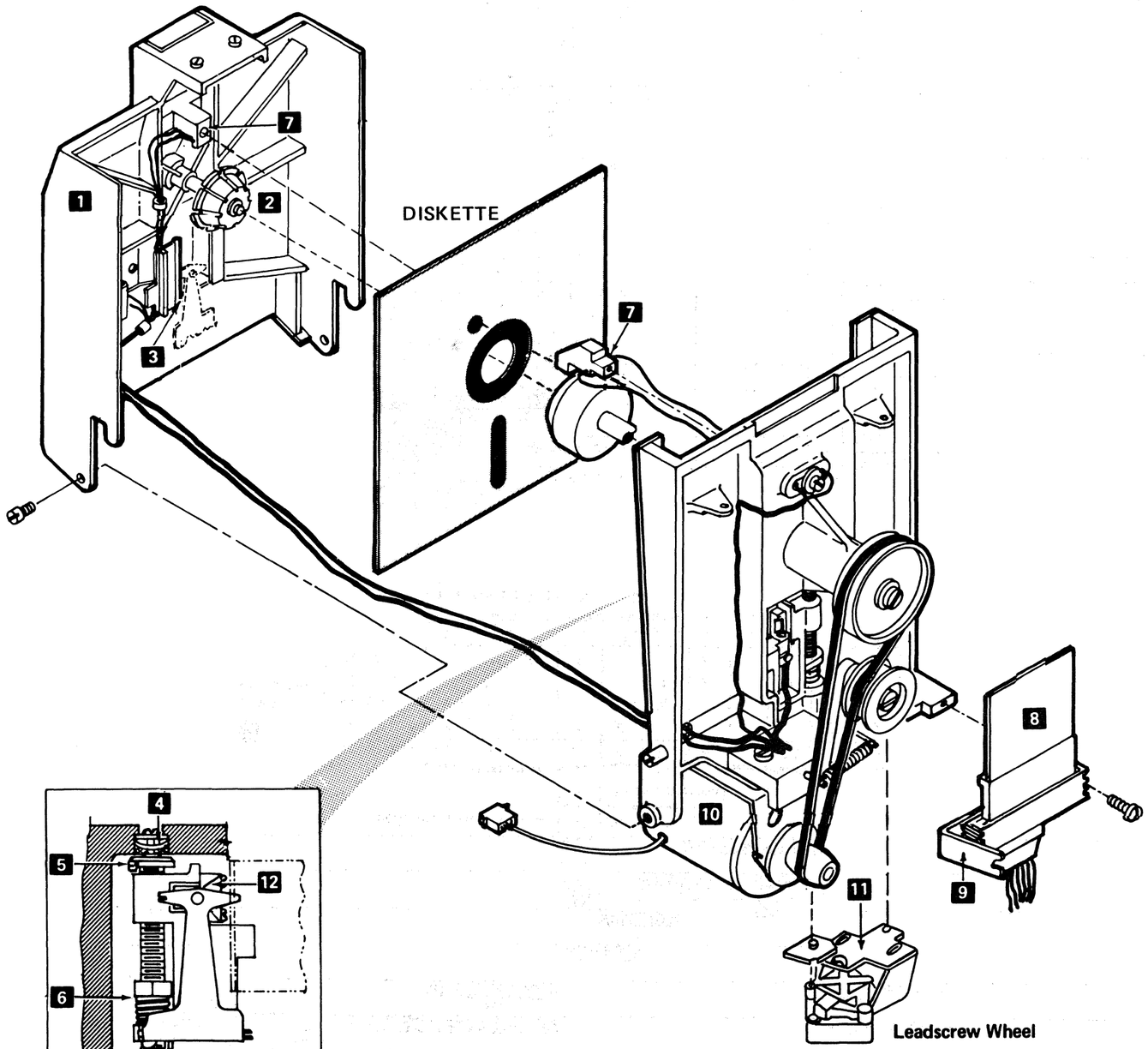
Diskette Collet Assembly 2
When the Diskette drive cover is closed, the spring-loaded collet centers and clamps the Diskette to the Diskette hub.

Head Load Actuator Assembly 3
The head load actuator assembly consists of a magnet and an armature. During a read or write operation, the head load actuator is energized and allows the head pressure pad arm to push the Diskette against the read/write head. At the same time, the head load actuator armature compresses the Diskette to locate and clean the disk against the inside surface of the Diskette envelope. While not reading or writing, the head load actuator is de-energized and holds the pressure pad assembly away from the Diskette to reduce wear on the Diskette surface and the read/write head.

Preload Spring 4
The preload spring loads the leadscrew to ensure head alignment with the Diskette.

Limit Stops 5
The upper and lower limit stops restrict head/carriage motion on the leadscrew.

Leadscrew Nut and Spring 6
The leadscrew nut and spring load the head/carriage assembly to ensure head alignment with the Diskette.



Light Emitting Diode (LED) and Phototransistor 7
When the Diskette cover is closed, the continuous light (the light from the LED is invisible) emitted from the LED is directed towards the phototransistor. Once every revolution, the index hole in the Diskette allows light from the LED to reach the phototransistor. The phototransistor sends index pulses to the Diskette controller.

File Control Card 8
The file control card provides drive circuits for the stepper motor, head load actuator, and the write and erase coils in the head. It also provides the amplifiers for the phototransistor and the read head.

The file control card is oriented so that the components and test pins face out for servicing. Early model drive units provide a bracket to hold the file control card for servicing. Diskette drive units with SN 22000 and above do not have this bracket. 9

Motor and Drive 10
The motor rotates the Diskette at a speed of 360 rpm.

Stepper Motor Assembly 11
The stepper motor wheel is permanently mounted on the end of the stepper motor shaft. The stepper motor shaft turns in increments of 90 degrees in either direction under the control of access pulses. The stepper motor wheel engages the leadscrew wheel. When the stepper motor rotates 90 degrees, it causes the leadscrew to rotate 90 degrees. The head carriage assembly then moves up or down one track on the Diskette.

Read/Write Head 12
The read/write head provides the read, write, and erase functions.

Operating Sequence

The control program activates the motor control. The Diskette can be inserted or removed with power up.

Insert the Diskette and close the cover. Closing the cover engages the Diskette collet assembly 8 in the drive hub 7 clamping the Diskette in place. With power up, the Diskette is now turning.

After a ten second delay from power on, index pulses 14 are read every 166.6 ms.

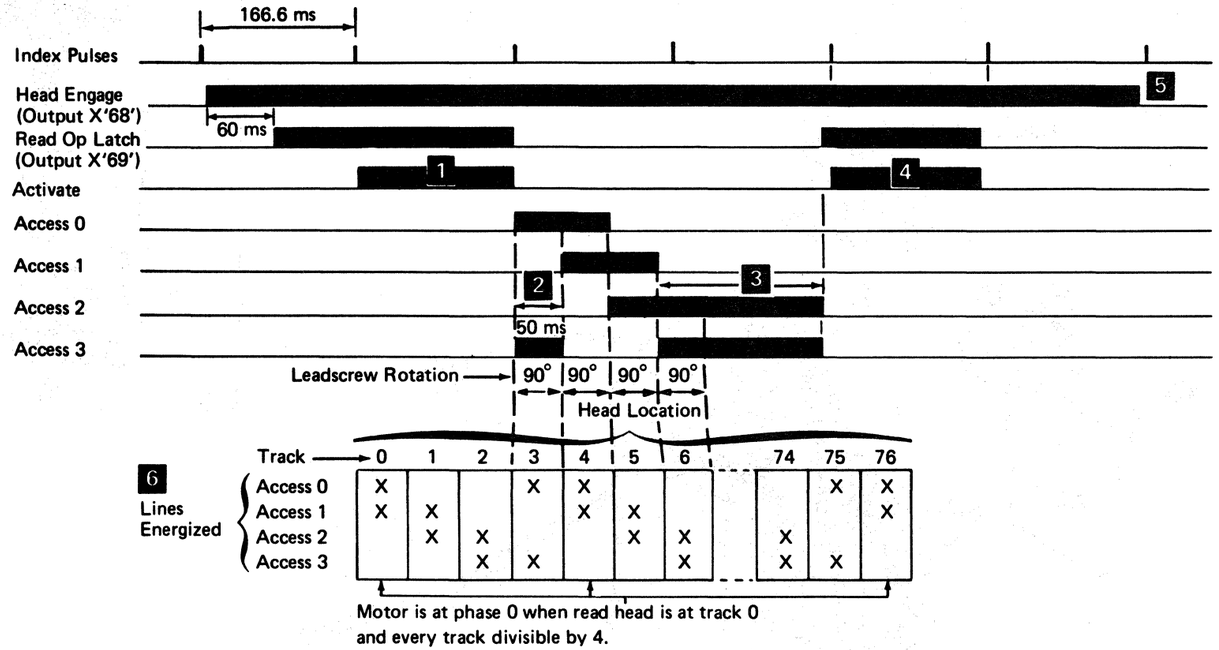
Output X'68' with bit 1.4 set activates the 'head engage' line 13 . This causes the head pressure pad 10 to push the flexible Diskette against the read head 9 . Once 'activate' becomes active, data is valid. Head location is determined by reading the track 1 or by returning the read head to track 0.

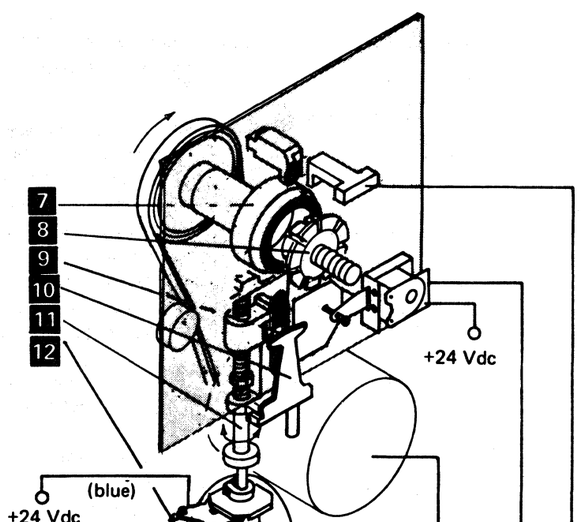
For each Output X'68', the stepper motor 12 rotates the leadscrew 11 90 degrees clockwise or counterclockwise depending on the state of bits 1.1 and 1.2. This moves the read head one track position. (Clockwise rotation of leadscrew, looking down on unit, moves the carriage up.) Two adjacent signal lines must be energized simultaneously when accessing 6 . Overlapping must be no less than 50 ms 2 . Prior to read or write operations, the two lines for the selected track must be energized for 150 ms minimum 3 (50 ms for travel and 100 ms to stabilize).

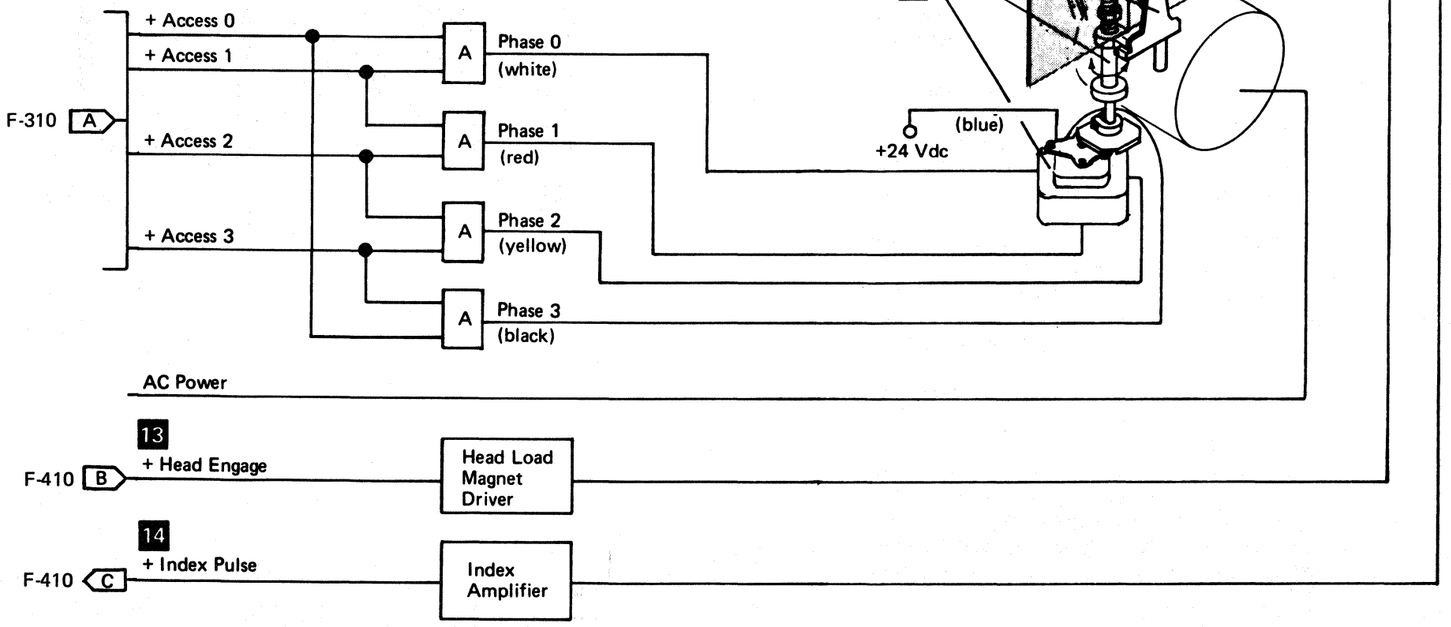
Reading occurs 4 .

Pressure pad may be lifted as soon as possible after completion of last read, write, or access operation to reduce Diskette and head wear 5 .

Typical Timing Sequence







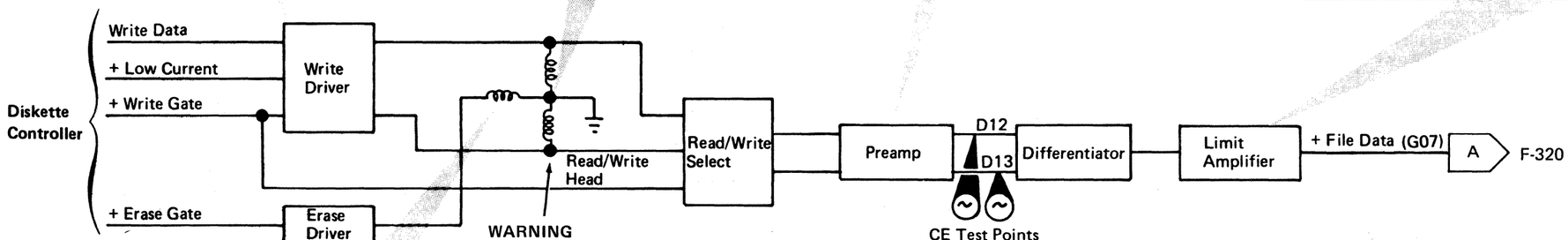
Read/Write Circuit Principles

Write Data
For each transition in the 'write data' line, current is switched in the read/write head casuing a flux change on the Diskette.

Raw Read Data
- Sine wave signal:
  125 kHz (all 0's)
  250 kHz (all 1's)
- Higher voltage at outer track because of higher disk speed and lower bit density.
- All 0's pattern gives higher voltage amplitude than all 1's.

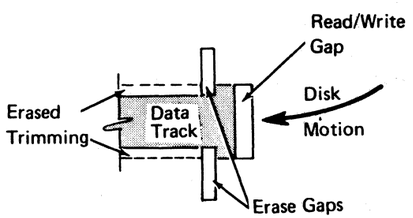
Read Amplifier
Preamp and differentiator input:
1.0 to 20 mV (all 0's)
0.5 to 15 mV (all 1's)

Limit Amplifier
- High gain differential amplifier amplifies signal so one of amplifier transistors is cut off. Outputs of limiter are two out-of-phase square waves.
- Differential rectifier RC network differentiates square waves. Resulting positive- and negative-going pulses (180° out of phase) are input to an OR circuit. Output is a train of positive pulses. Positive leading edges of output pulses correspond to peaks in read signal delayed by a constant amount.
- File data is a string of 150 ns pulses ('+file data') which are fed to the VFO in the Diskette controller.

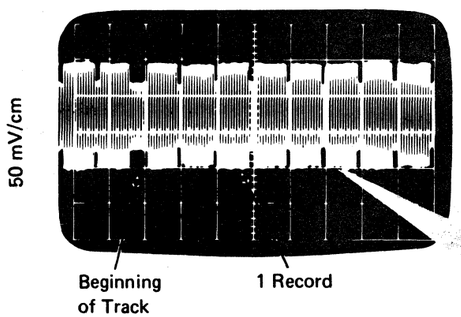


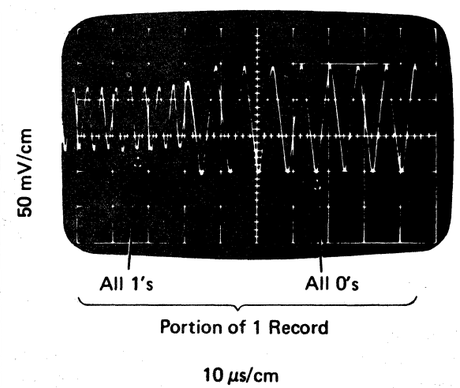
ERASE

The edges of the data track are erased to prevent reading adjacent tracks during Diskette interchange.



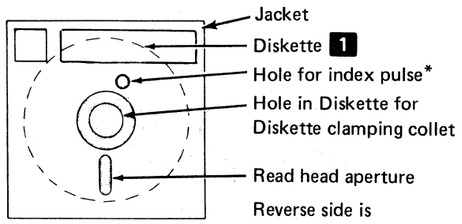
Full Track Differential Read Signal at CE Test Points

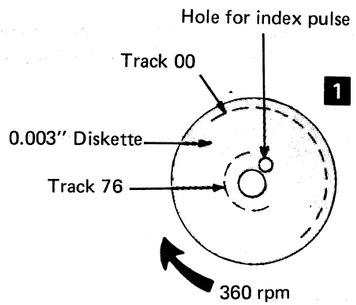




Diskette
(Part 1 of 2)

Characteristics





- The Diskette rotates within the sealed Diskette jacket.
- The Diskette is interchangeable with any other Diskette having the same format.
- The Diskette is mailable.
- Data areas on the Diskette may be reached in random sequence.

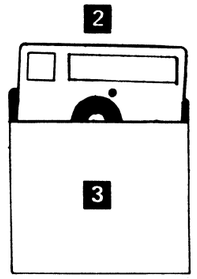
*The hole is off-centered to prevent an index pulse if the Diskette is placed backwards in the Diskette drive.

Handling

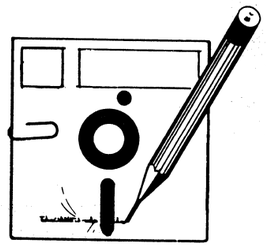
Damaged Diskettes should not be inserted into the Diskette drive. Diskettes which are physically damaged (torn, creased, warped) or contaminated with foreign materials (eraser dust, fingerprints, cleaning fluid, etc.) may cause the Diskette to lift from the head resulting in operation errors, equipment errors, or head damage.

Placing heavy objects on the Diskettes may damage the Diskette.

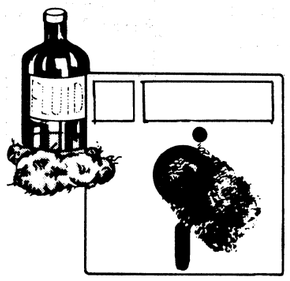
- Return the Diskette 2 to the envelope 3 whenever it is removed from the Diskette drive.



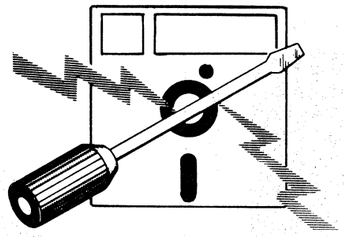
- Do not use clips. Never write on the Diskette with an erasable pencil.



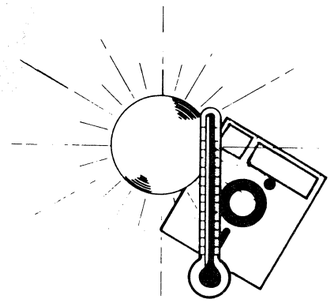
- Do not touch or clean the Diskette surface. Contaminated Diskettes must be discarded.



- Keep the Diskette away from magnetic fields and from materials which might be magnetized. Any Diskette exposed to a magnetic field may lose information.



- Do not expose the Diskette to excessive heat (over 125°F or 51.5°C) or direct sunlight.



Long Term Storage

Place Diskettes in their envelopes and store in the following environment:
- Temperature: 50° to 125°F (10.0° to 51.5°C)
- Relative humidity: 8% to 80%
- Maximum wet bulb: 85°F (29.4°C)

If a Diskette has been exposed to temperatures outside of the machine's environmental range, allow five minutes acclimation time before use. The Diskette should be removed from its shipping container during this time, but should be kept in its envelope.

Diskette
(Part 2 of 2)

Shipping and Receiving
Ship the Diskette inside the original shipping carton.
An ordinary mailing envelope does not provide sufficient protection.

Be sure to label the package: DO NOT EXPOSE TO EXCESSIVE HEAT (over 125°F or 51.5°C) OR DIRECT SUNLIGHT.

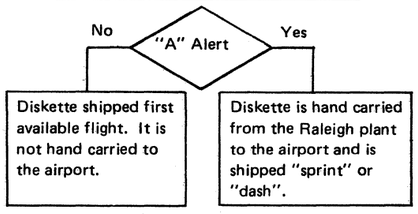
Upon receiving Diskettes, check for carton and Diskette damage. Save the carton for storing the Diskette and for shipment later.

Replacement Diskette Ordering Procedure

CE records the:
- Machine type serial number
- BM number
- GID number.
- EC number.

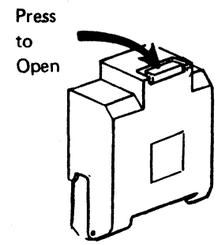
From Diskette label

CE calls Mechanicsburg specifying code "A" or Code "A" Alert.

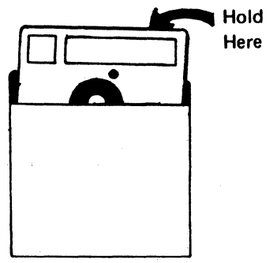


Insertion

1 Open the cover.



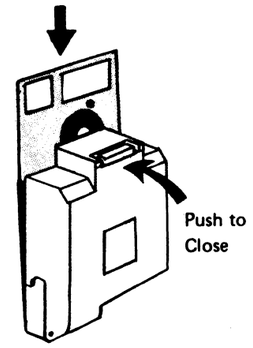
2 Remove the Diskette from the envelope. Grasp the Diskette by the upper edge.



3 Lower the Diskette squarely into the file.

WARNING
Do not insert damaged diskettes.

4 Close the cover after the Diskette is fully inserted.



5 Place the empty envelope in a clean storage area.

Removal
Reverse above procedure.

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Removal, Adjustment and Replacement Procedures (Part 1 of 8)

Latch Assembly
Removal and Replacement

1 Open the cover.

2 Remove the two latch mounting screws 1 .

3 Pull the latch out toward the front of the cover.

4 To replace, reverse the above procedure.

Cover Assembly
Removal and Replacement

WARNING
Do not allow the pressure pad arm to snap against the head.

1 Hold the cover while removing the two screws (one on each side).

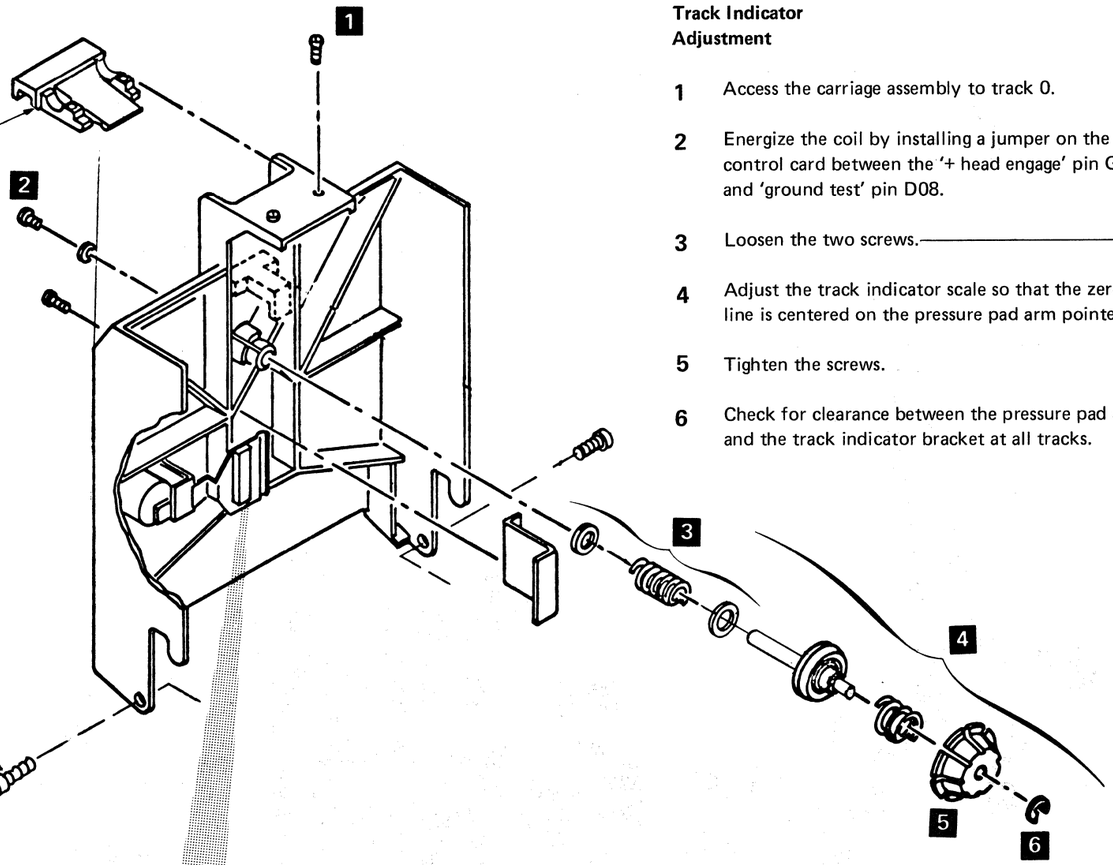
2 Remove the cover carefully to avoid damage to wires.

3 Remove the wires from the LED and the actuator. (Yellow wire goes to LED terminal marked Y.)

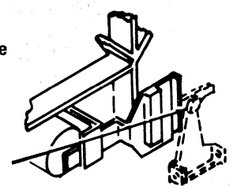
4 Remove the wires from the clips on the cover.

WARNING
Before replacing the cover screws, position the actuator bail under the pressure pad arm.

5 To replace, reverse the above procedure.



WARNING
Before replacing the cover screws, position the actuator bail under the pressure pad arm.



Track Indicator
Adjustment

1 Access the carriage assembly to track 0.

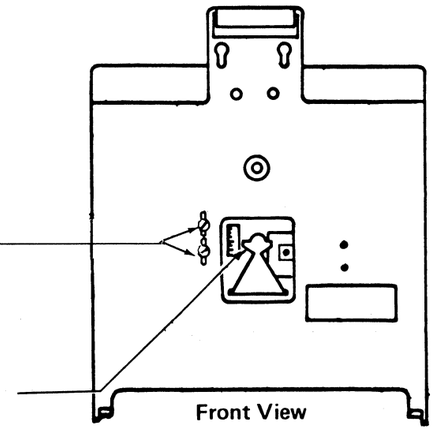
2 Energize the coil by installing a jumper on the file control card between the '+ head engage' pin G10 and 'ground test' pin D08.

3 Loosen the two screws.

4 Adjust the track indicator scale so that the zero line is centered on the pressure pad arm pointer.

5 Tighten the screws.

6 Check for clearance between the pressure pad arm and the track indicator bracket at all tracks.



Collet
Removal and Replacement

1 Remove the cover.

2 Remove mounting screw 2 .

3 Remove collet assembly 4 , spring, and washers 3 .

4 Remove collet 5 by removing clip 6 .

5 To replace, reverse the above procedure.

Removal, Adjustment and Replacement Procedures (Part 2 of 8)

Drive Motor
Removal

DANGER
Remove primary power from the 3705-80.

1 Unplug the drive motor cable 1 .

2 Remove the belt.

DANGER
Motor case temperature may exceed safe handling limits.

3 Loosen the two motor mounting clamps and remove the drive motor 2 .

4 Remove the drive pulley 4 .

Drive Motor
Replacement

1 Replace the drive pulley. (Align the setscrew with the flat surface on the shaft.)

2 Clamp the motor to the mounting bracket.

DANGER
(60 Hz motors) To prevent personal injury, position the two large holes in the motor frame to the top and under the bracket 10 .

3 Replace the belt.

4 Plug in the drive motor cable. Restore primary power to the 3705-80.

5 Check the belt tracking and adjust if necessary.

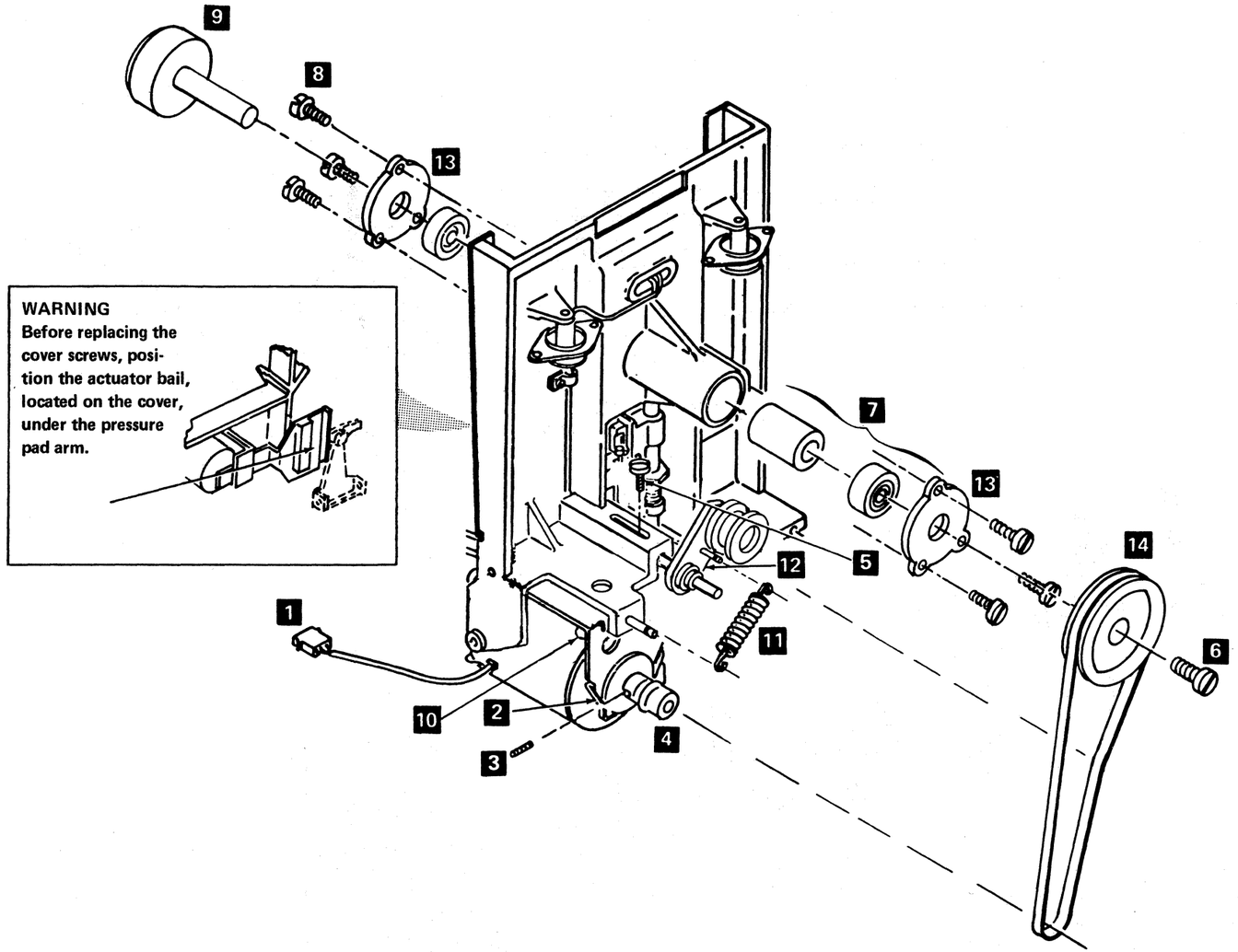
Belt Tracking
Adjustment

The belt must be riding in the center of the drive pulley 4 and hub pulley 14 when the drive pully is rotated counterclockwise (viewed from the pulley side).

WARNING
The drive pulley setscrew 3 must be aligned with the flat on the motor shaft.

Adjust the position of the drive pulley and the idler so the belt rides on the center of the drive pulley and the hub pulley. Froming of the idler pulley arm 12 may be required.

Note: *Late level Diskette drives have an idler pulley with a narrow groove. To adjust belt tracking, loosen screw 5 and slide the idler until the belt rides in the center of the drive pulley and the hub pulley.*



WARNING
Before replacing the cover screws, position the actuator bail, located on the cover, under the pressure pad arm.

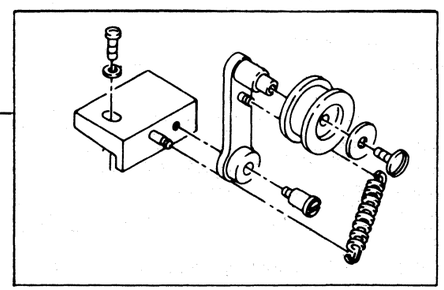
Idler Assembly
Removal

Note: *Diskette drive units with serial number below 22000 have this type idler assembly.*

1 Remove the belt and spring 11 .

2 Remove the idler assembly 12 .

3 To replace, reverse the above procedure and check belt tracking.



Hub Assembly
Removal and Replacement

1 Remove the cover.

2 Remove the drive belt.

3 Remove the screw 6 and remove the pulley 14 .

4 Remove the hub 9 .

5 Remove the bearing retaining screws and bearing 8 .

Note: *Late level Diskette drives have bearing retainer plates 13 between the bearing retaining screws and the bearings.*

6 Remove the bearing retaining screws, bearing, and spacers 7 .

7 To replace, reverse the above procedure. Check the belt tracking and adjust if necessary.

WARNING
The front bearing must be flush with the front surface of the baseplate; tighten the front bearing retaining screws first. The bearing seals should face outward.

Drive Pulley
Removal

1 Remove the belt.

2 Loosen setscrew 3 and remove pulley 4 .

Drive Pulley
Replacement

1 Position the pulley on the shaft.

2 Align the setscrew with the flat surface of the shaft and tighten.

3 Replace the belt.

4 Check the belt tracking and adjust if necessary.

Removal, Adjustment and Replacement Procedures (Part 3 of 8)

Pressure Pad Actuator Removal and Replacement

1 Remove the cover.

2 Remove these two screws.

3 Remove the leads.

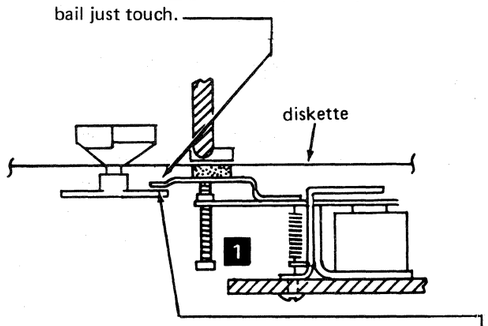
4 To replace, reverse above procedure and do adjustment.

Pressure Pad Actuator Adjustment

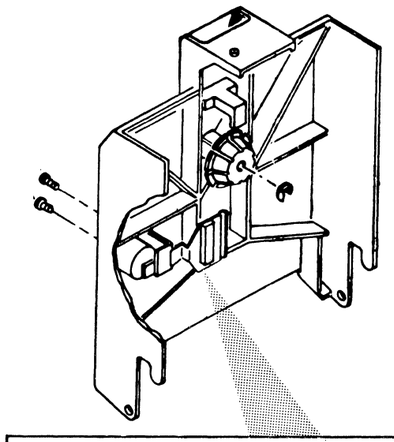
1 Install a Diskette.

2 Energize the coil by installing a jumper on the file control card between the '+ head engage' pin G10 and 'ground test' pin D08.

3 Adjust screw 1 until the pressure pad arm and bail just touch.



4 Rotate the adjusting screw clockwise 1/2 to 3/4 turn and check for clearance between the arm and bail at all tracks.

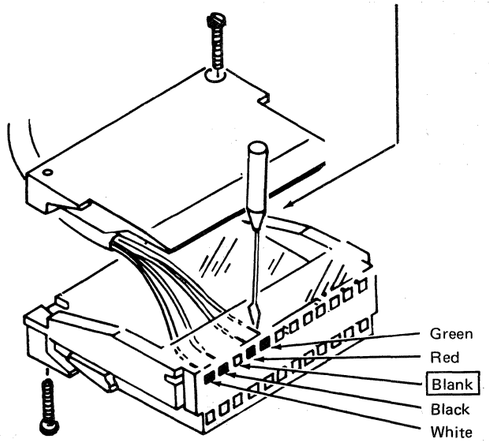


WARNING
Before replacing cover screws, position actuator bail, located on cover, under pressure pad arm.

Leadscrew and Head Carriage Assembly Removal

1 Note the routing of the head cable.

2 Remove the wires from the connector by pushing down with a small screwdriver as shown.



3 Center the carriage on the leadscrew by turning the stepper motor wheel.

4 Remove the stepper motor 4 and the leadscrew wheel 3.

5 Remove the cover.

6 Loosen the clamping screws on the upper and lower stops.

7 Remove the bottom bearing.

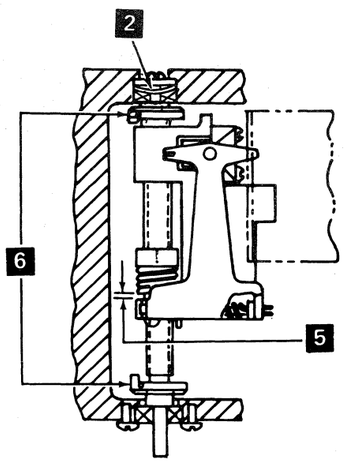
WARNING
Watch for the preloaded spring 2 when removing the shaft.

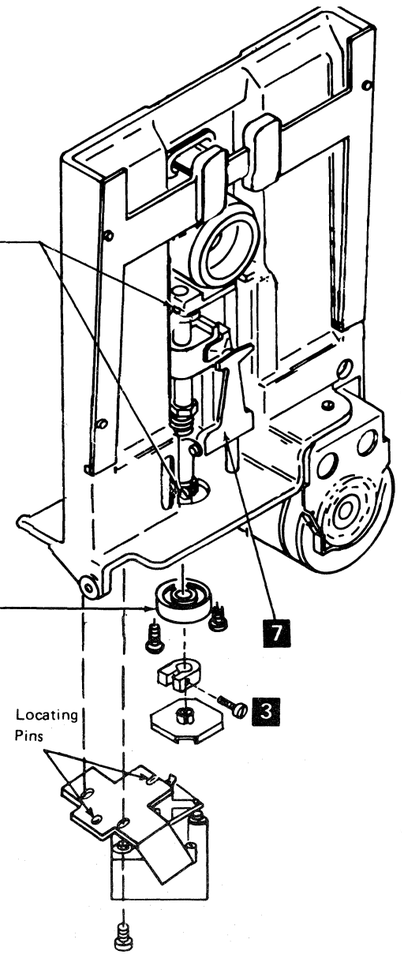
8 Slide the leadscrew assembly down until the top clears the baseplate, then slide the assembly out.

WARNING
Do not allow the pressure pad arm to snap against the head. 7

9 Remove the top bearing, preload spring, and both stops from the leadscrew.

WARNING
Early model drive units do not have a spacer to retain the preload spring; therefore, care should be taken not to lose the preload spring. 2





Replacement

Note: *If the leadscrew and the carriage are disassembled, replace by threading the leadscrew into the bottom portion of the carriage assembly and into the carriage nut and spring. There should be approximately 0.51 mm (0.020") here.* 5

1 Center the carriage assembly on the leadscrew and install the upper and lower limit stops orientated as shown. 6

2 Replace the top bearing and preloaded spring 2 (concave side up).

3 Replace the assembly into the baseplate, bottom end first.

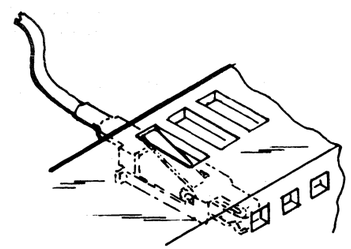
4 Replace the bottom bearing and check for about 0.76 mm (0.030") up and down movement of the leadscrew against the preloaded spring.

5 Replace the leadscrew wheel, the leadscrew wheel clamp, and the stepper motor.

Note: *Reroute head cable as noted under removal.*

6 Connect wires (see removal for wire locations). Check that the wire terminals are properly seated and securely fastened in the connector.

WARNING
Ensure that the locking tabs on the terminals engage in the connector slots to prevent the leads from pushing out when plugged in.



7 Do the stepper motor adjustment (F-565) and the read/write head adjustment (F-555).

8 Replace the cover.

Removal, Adjustment and Replacement Procedures (Part 4 of 8)

Read/Write Head Adjustment

To properly make the head adjustment, you must obtain three simultaneous conditions:

- Correct head to CE tool clearance.
- Correct relationship between the stepper motor and leadscrew wheels.
- Correct clearance between the stepper motor and leadscrew wheels.

1 Access head to track 0 (stepper wheels should line up as in view 13).

2 Remove the cover.

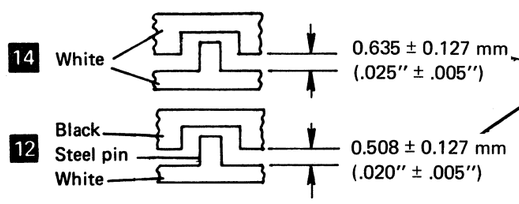
3 Loosen the mounting screw and move phototransistor assembly 1 to the left.

WARNING
If phototransistor assembly is not moved, the accuracy of the head adjustment may be affected.

4 Loosen clamping screws on lower limit stop 8 and leadscrew wheel 9 .

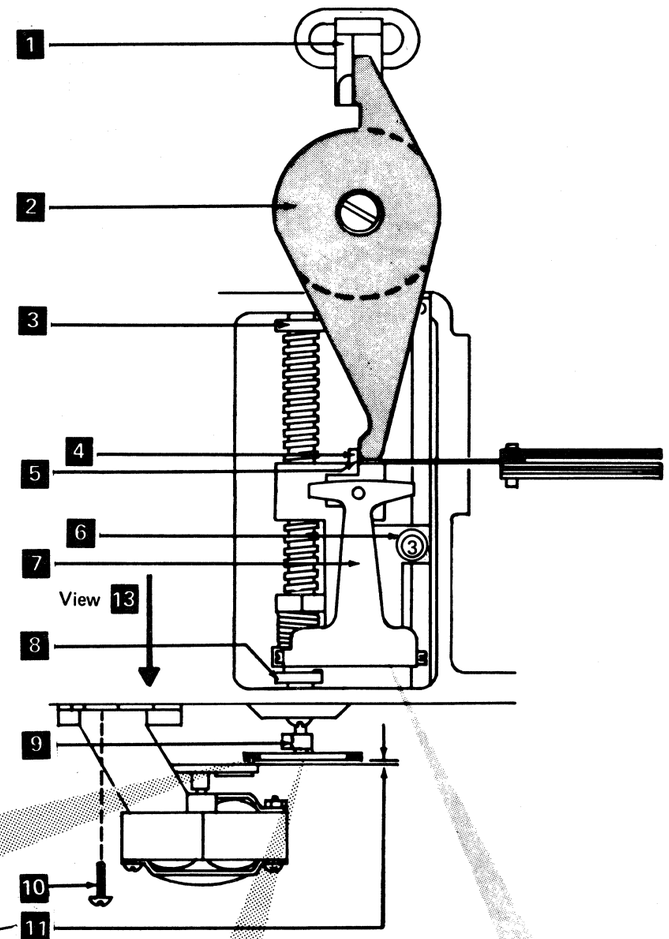
Steps 5 and 6 provide maximum stepper motor to leadscrew wheel pin penetration with no binds.

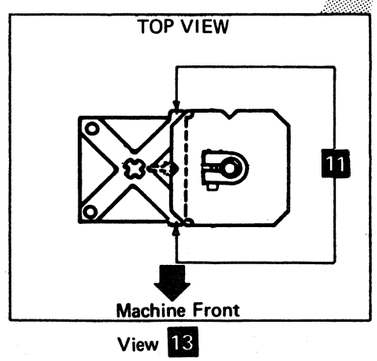
5 Determine type of stepper assembly, below:



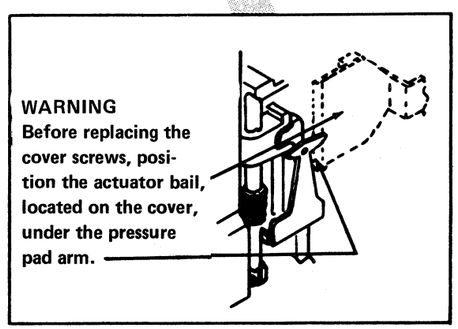
6 With stepper motor and leadscrew wheel oriented as in view 13 insert a feeler gage corresponding to the gap setting in 14 or 12 above, between the wheels as shown by 11 in view 13 . Gage may be left in place.

7 Locate the white dot label or identation on the outer circumference of the Diskette drive hub. If the hub has both, always use the white dot. Rotate the hub to position this mark up.





View 13



This ensures that any hub eccentricity is located in the same spot and that all head adjustments use the same reference point.

WARNING
Avoid any contact of the CE tool with the highly polished face of the head.

8 Install the CE tool (P/N 2200698) on hub 2 . Clamp into place with the thumbscrew.

9 Rotate the CE tool so it contacts surface 4 .

10 Rotate leadscrew by gripping upper limit stop 3 adjust for gap 5 . This gap is a number found on the front of the read head assembly 6 . This number represents thousandths. Example: 3 equals 0.076 mm (0.003"). Adjust for a very light drag on a 0.076 mm (0.003") gage. A 0.051 mm (0.002") gage must be free.

WARNING
Ensure stepper motor and leadscrew wheel remain oriented as in 13 .

11 Securely tighten leadscrew wheel clamping screw 9 . The top of the clamping collar should be approximately even with the top of the metal clamping surface of leadscrew wheel.

WARNING
If the clamping collar is not securely tightened, machine operation will tend to cause head to go out of adjustment.

12 Adjust the phototransistor so the raised edge is in contact with tool 2 and tighten the mounting screw.

13 Remove the CE tool and perform the lower limit stop adjustment (F-560).

14 Recheck gap 11 setting.

15 Rotate the stepper motor at least one full revolution and check for binds.

16 Do the upper limit stop adjustment (F-560).

17 If a new leadscrew wheel has been replaced in step 5, the slot should be 25—40 percent full with IBM #23 grease.

18 Replace the cover and adjust track indicator (F-540).

Leadscrew Wheel Removal and Replacement

1 Remove the stepper motor 10 (F-565).

2 Loosen clamping screw and remove leadscrew wheel 9 .

3 To replace, reverse above procedure. Do stepper motor adjustment (F-565), head adjustment (this page).

Head and Pressure Pad Cleaning

WARNING
Use only the materials listed below to clean the head and the pressure pad.

1 With the cover open, manually rotate the stepper motor wheel until the carriage assembly is at the upper limit stop.

WARNING
Do not allow pressure pad arm to snap against head.

2 Pivot pressure pad arm 7 away from head and check pad for contamination. If contaminated, use dry brush (P/N 2200106) to remove caked deposits and to fluff pad.

WARNING
Fluid treated cloth should not contact pressure pad.

3 While holding pressure pad arm out, clean polished head surface with isopropyl alcohol (P/N 2200200) applied to a clean cloth (P/N 2108930).

Removal, Adjustment and Replacement Procedures (Part 5 of 8)

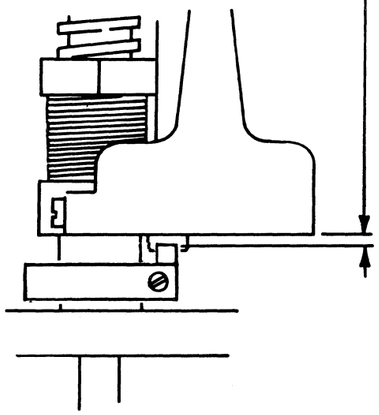
Lower Limit Stop Adjustment (With Cover Removed)

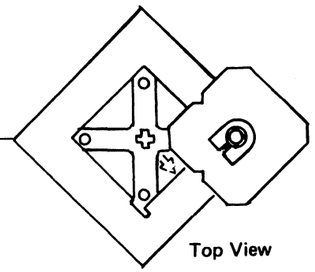
1 Loosen clamp screw **1** . Make sure that the lead-screw is 45° ± 15° beyond track 0 in the downward direction. Wheels must be in the position shown.

2 Position the limit stop so the projection on the limit stop is in front of and against the projection on the carriage.

3 Adjust for 0.3 mm to 0.46 mm (0.012" to 0.018") between top of the projection on the limit stop and bottom of the carriage.

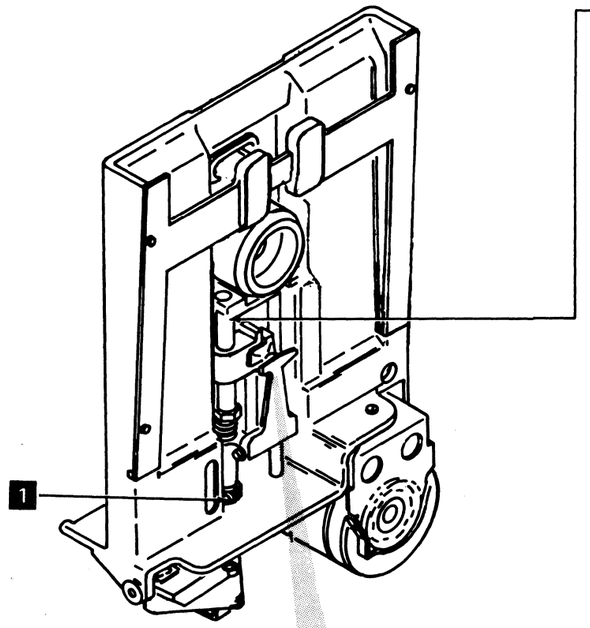
4 Tighten screw **1** .



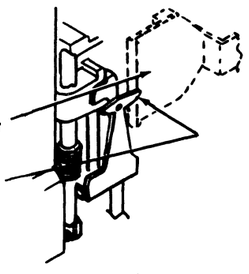


Top View

Front of Machine



WARNING
Before replacing the cover screws, position the actuator bail, located on the cover, under the pressure pad arm.



Upper Limit Stop Adjustment

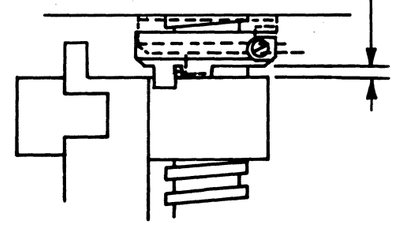
1 Loosen the clamp screw and slide the stop up as far as possible.

2 Starting at track 0, rotate the stepper motor wheel 19 full revolutions to move the carriage assembly up to track 76. Rotate the stepper motor wheel approximately 45 degrees further.

3 With the projection on the limit stop against the carriage, adjust the stop for 0.64 mm to 0.89 mm (0.025" to 0.035").

4 Tighten the clamp screw.

WARNING
Do not overtighten.



Back View

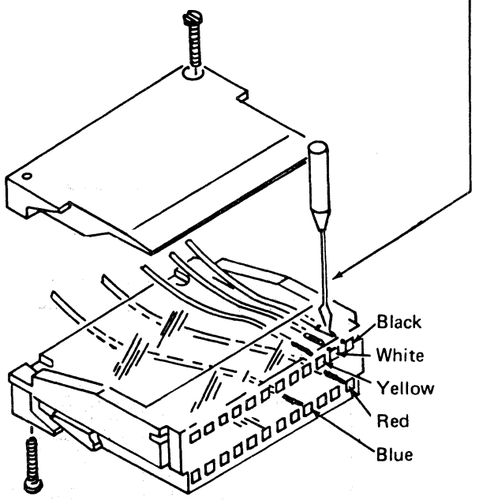
The lower and upper limit stop adjustment ensures that the carriage can always be accessed to tracks 0 and 76 without over-travel, thus damaging the mechanism.

Removal, Adjustment and Replacement Procedures (Part 6 of 8)

Stepper Motor
Removal and Replacement

1 Remove the five leads from the connector.

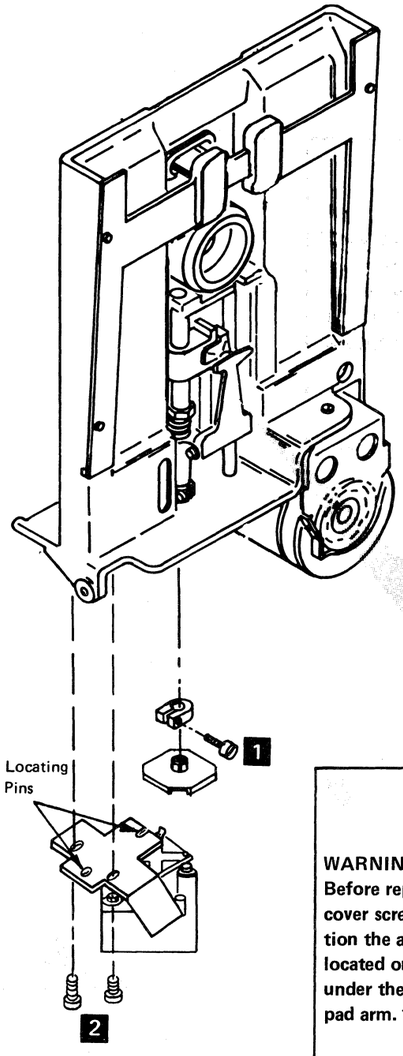
2 Remove two screws 2 .

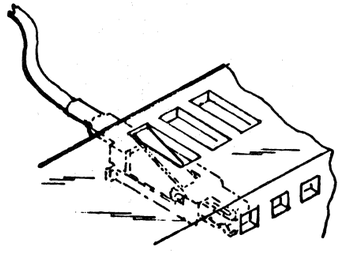


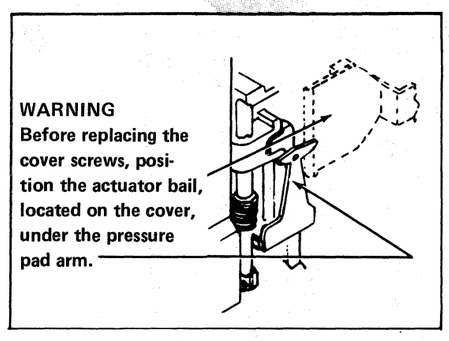
WARNING
Make sure the pins are in the slots of the leadscrew wheel when replacing the stepper motor to avoid breaking parts.

3 To replace, reverse above procedure and do the stepper motor adjustment.

WARNING
Ensure that the locking tabs on the terminals engage in the connector slot to prevent the leads from pushing out when plugged in.







Stepper Motor
Adjustment

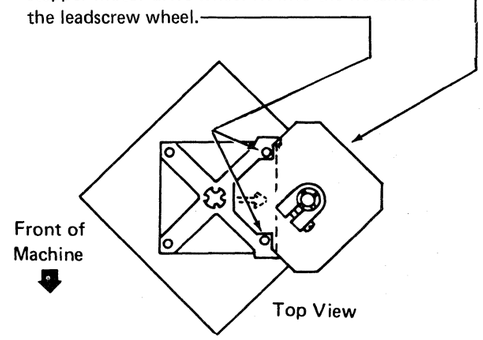
1 Loosen two screws 2 .

2 Move the stepper motor away from the leadscrew.

3 Loosen clamping screw 1 and move the leadscrew wheel up so it rotates freely.

4 Position the wheel as shown.

5 Pull the leadscrew wheel down until the pins on the stepper motor drive wheel fit into the notches on the leadscrew wheel.

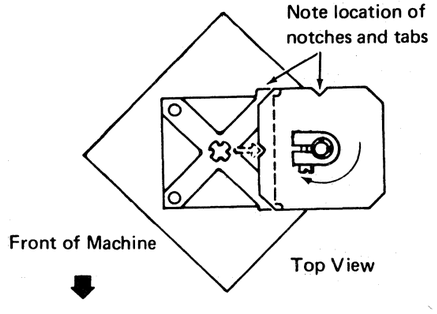


6 Slide the stepper motor toward the leadscrew until the pins contact the notches. No clearance is allowable. Do not force stepper motor into leadscrew wheel.

7 Tighten the two stepper motor mounting screws 2 .

8 Move the leadscrew wheel up until it rotates freely.

9 Rotate the leadscrew wheel and slide it down on the drive pins in the position shown below.



10 Do the head adjustment (F-555).

Removal, Adjustment and Replacement Procedures (Part 7 of 8)

Phototransistor
Service Check

Note: *Always perform the following procedure with the Diskette loaded; otherwise, ambient light will be present causing an improper reading on the VOM.*

DANGER
Remove primary power from the 3705-80.

1 Unplug the Diskette drive motor plug. Restore primary power to the 3705-80.

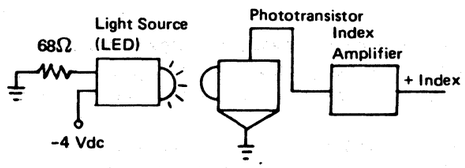
2 Attach the positive probe of a VOM (15 Vdc scale) to +6.0 Vdc, test point G11 on the file control card.

3 Attach the negative probe to amplifier input B08.

4 Insert Diskette and close the cover.

5 With the head unloaded, rotate hub until the index hole causes the phototransistor to switch on or off. (Rotating the hub back and forth causes a continuous switching in the phototransistor.

6 A shift in excess of 0.5 Vdc should be noted on the VOM under normal circumstances.



Note: *This LED emits invisible light.*

DANGER
Remove primary power from the 3705-80.

7 Replug the Diskette drive motor plug. Restore primary power to the 3705-80. Set up an oscilloscope as indicated to the right and check for an index pulse width of 0.5 ms minimum.

Phototransistor
Removal

1 Access the read head to track 0.

2 Power down.

3 Remove the cover.

4 Remove mounting screw 3 .

5 Remove the leads.

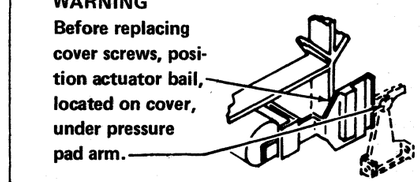
Phototransistor
Replacement

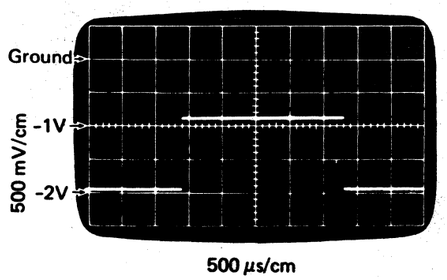
1 Replace the leads. (Yellow wire goes to terminal marked Y.)

2 Replace the mounting screw, but do not tighten.

3 Do adjustment starting at step 4.

WARNING
Before replacing cover screws, position actuator bail, located on cover, under pressure pad arm.





Phototransistor
Adjustment

1 Access the read head to track 0.

2 Remove cover.

3 Loosen mounting screw 3 , and move the phototransistor to the left.

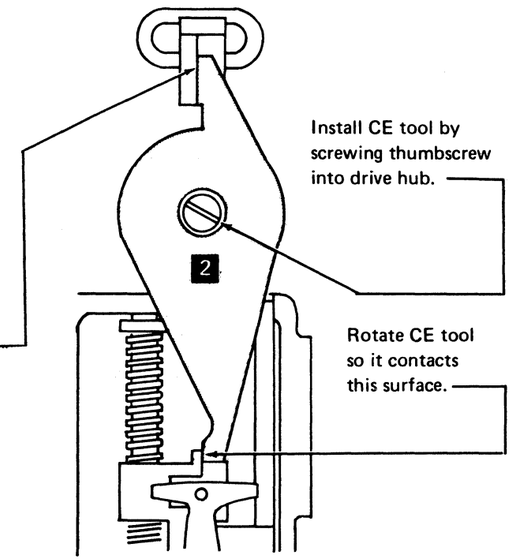
4 Install the CE tool 2 as shown at right.

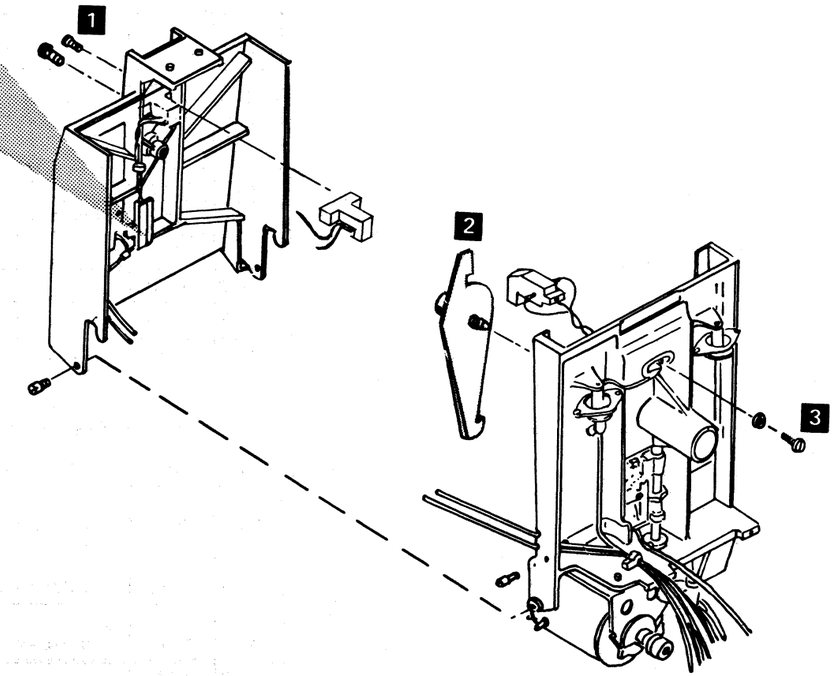
5 Adjust the phototransistor so the raised edge is in contact with tool.

6 Tighten the mounting screw.

7 Remove the CE tool.

8 Replace the cover.





Light Emitting Diode (LED)
Service Check

Attach the positive probe of a VOM to LED current test pin, D07 on the file control card and the negative probe to -4.0 Vdc test pin, G06 on the file control card. The voltage should be +1.0 Vdc to +1.6 Vdc.

Light Emitting Diode (LED)
Removal and Replacement

1 Remove the cover.

2 Remove the two mounting screws 1 .

3 Remove the leads. (Yellow wire goes to terminal marked Y.)

4 To replace, reverse above procedure.

Note: *This LED emits invisible light.*

Removal, Adjustment and Replacement Procedures (Part 8 of 8)

MST File Control Card
Removal and Replacement
The MST file control card is oriented with the components and test pins face out. The card does not have to be moved for servicing.*

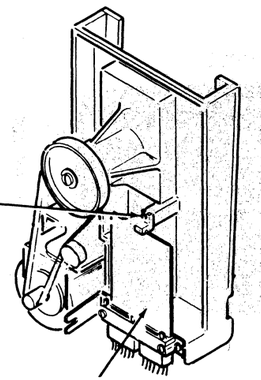
1 Power off.

2 Loosen the screw and turn bracket; then tighten screw.

3 Remove card.

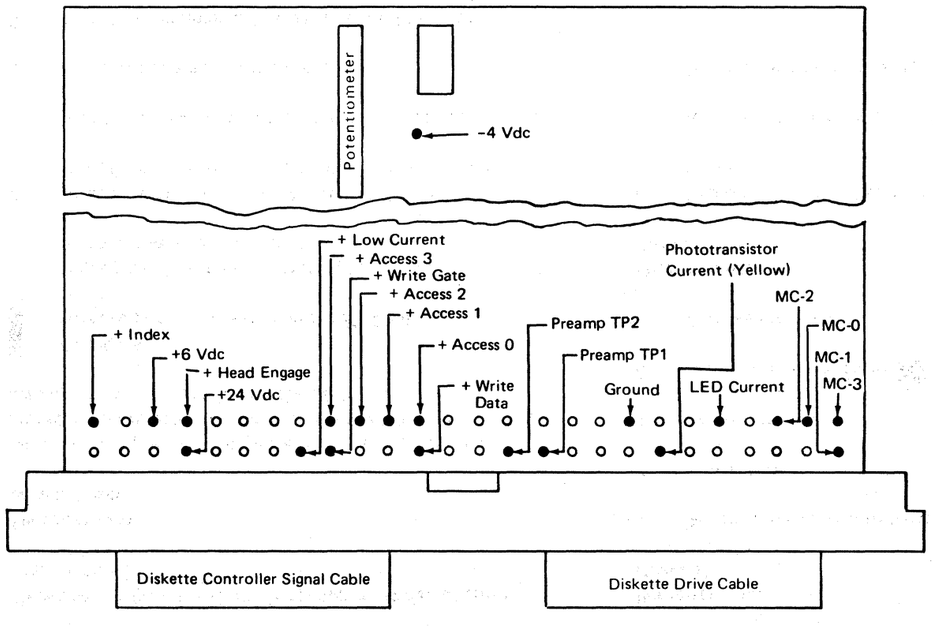
4 To replace, reverse above procedure. Be sure card is properly seated in socket and retaining bracket.

*Early model Diskette drives provide a bracket to hold the file control card for servicing. Diskette drives with serial number 22000 and above do not have this bracket.



MST File Control Card

MST Test Points

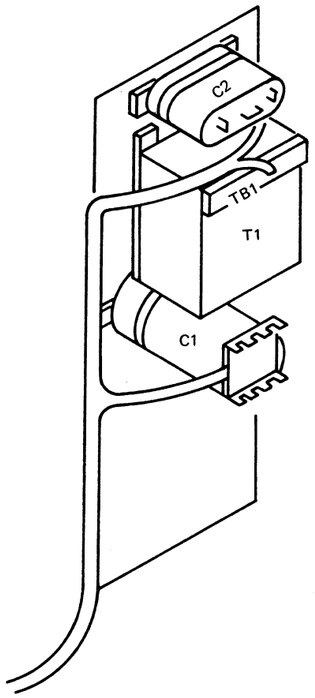


Card Pin Assignment

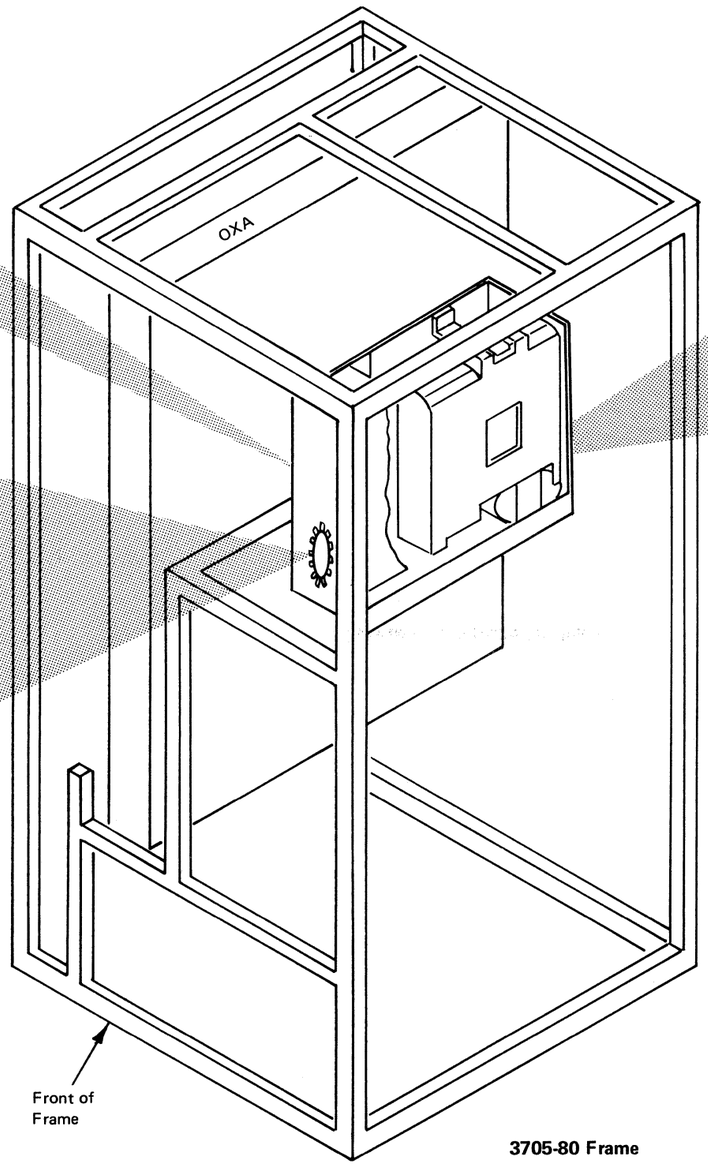
Name	Color	MST
Stepper Motor MC-0 (Phase 0)	White	B03
Stepper Motor MC-1 (Phase 1)	Red	D02
Stepper Motor MC-2 (Phase 2)	Yellow	B04
Stepper Motor MC-3 (Phase 3)	Black	B02
Stepper Common +24 Vdc	Blue	D05
Head Magnet +24 Vdc	Yellow	D04
- Head Load	Black	B05
LED Return	Black	D06
LED Current	Yellow	D07
Phototransistor Return	Black	D09
Phototransistor Current	Yellow	B08
Head Input	Black	B12
Head Input	White	B13
Erase Current	Red	B10
Head Ground and Shield	Green	B09
Preamp TP1		D12
Preamp TP2		D13
Ground	Black	D08
+ Access 0		G02
+ Access 1		G03
+ Access 2		G04
+ Access 3		G05
+ File Data		G07
+ Head Engage		G10
+ Write Data		J02
+ Erase Gate		J04
+ Write Gate		J05
+ Low Current		J06
+ Index		G13
+24 Vdc		J10
+6 Vdc		G11
+5 Vdc		
-4 Vdc		G06
-5 Vdc		
Ground		J08

REMOTE 3705-80 DISKETTE DRIVE AND POWER SUPPLY LOCATIONS

F1—0.3A
F2—2A
Located on the rear cover of the Diskette Drive

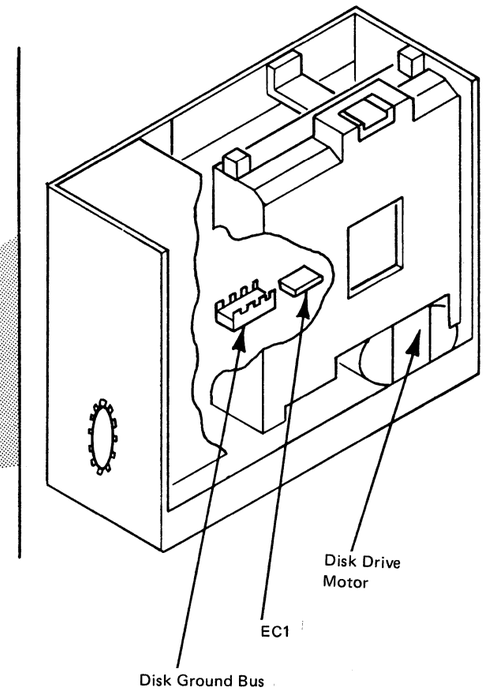


PS1



3705-80 Frame

Diskette Drive



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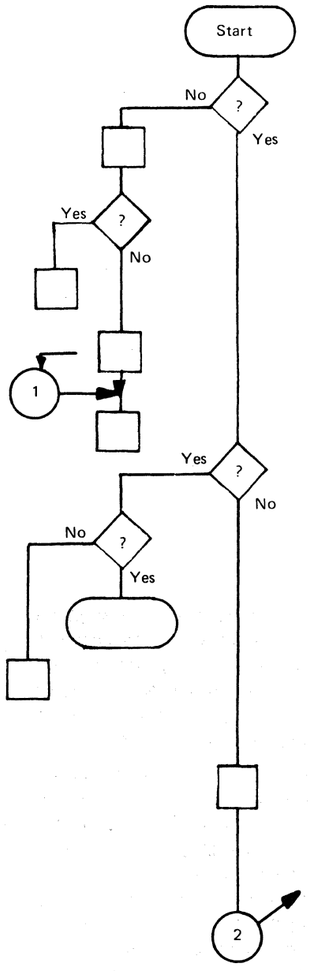
REMOTE 3705-80 DISKETTE DRIVE POWER SUPPLY MAINTENANCE PROCEDURE



Does the drive motor run?

Make sure the remote 3705-80 is powered up.

DANGER
Is *200 Vac* between TB1-1 and TB1-3 of PS1 (for location see Page F-600)? Check the connector between PS1 and the Diskette drive motor. If ok, suspect the motor.

Check the PS1 cables

Refer to the 3705-80 power-on sequence charts on D-540 of this volume.

Can the Diskette drive access, load head, read or write?

Is Re-IPL possible?

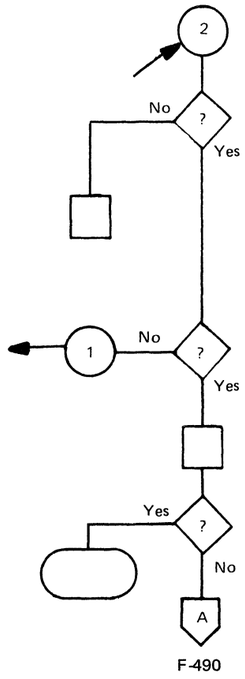
Return to the Customer

See Note.

Check input fuse F1 (0.3 amp) and Output fuse F1 (2 amp) on PS1 (for location see Page F-600).

Note: *Refer to the RPL section in Volume 1 (SY27-0208) of this FETMM for RPL diagnostic information.*

P/N 1757889
P/N 1757880
P/N 1757881
P/N 1757882
P/N 1757883
P/N 1757884



F-490

Fuses ok?

Determine why the fuse(s) blew then replace the fuse(s). Use YZ logic pages.

Are the 0XF-HD2-2 points made?

Replace the file control card on the Diskette drive.

Does the Diskette drive operate ok?

Return to the customer

TOOLS AND TEST EQUIPMENT

A. Special branch office tools and maintenance supplies for a remote 3705-80 for the Diskette drive include:

Part Number	*Description*	*Quantity*
2200698	CE Alignment Tool Kit	1
2200106	Brush	1
2200200	Isopropyl Alcohol	1
2108930	Cloth	1

The CE alignment tool is used for the following:

- Alignment of the read head by adjusting the read head to track 0. See Page F-555.
- Adjustment of the phototransistor assembly by mechanical alignment. See Page F-570.

B. Test equipment and non-technology related tools required for the remote 3705-80 Diskette controller — same as the local 3705-80.

C. Technology related tools
Refer to Tools and Test Equipment TSL No. 43 for MST tool requirements, with the following change:

The tools and procedures outlined in Chapter 4 ("Emergency Card Repair") of the MST FETOM (Order No. SY22-6739) are not recommended for use by Field Engineering. These tools are not part of the normal maintenance package and should not be ordered by the CE or the Branch Office.

PREVENTIVE MAINTENANCE

The Diskette drive requires no scheduled maintenance. The success of this concept depends upon the proper care of the Diskettes and the head/carriage assemblies.

WARNING
The Diskette drive contains plastic materials that are subject to damage by a wide variety of chemicals, including IBM cleaning fluids.

To avoid serious damage to the leadscrew and the carriage, lubricate the leadscrew only with IBM No. 6 oil when the head carriage is replaced.

To avoid serious damage to the head, clean it only with isopropyl alcohol (PN 2200200) and a clean cloth (PN 2108930) after removing the Diskette (see Page F-555).

CE SERVICE HINTS

Read Errors Due to Speed Changes: Run the index timing pulse diagnostic to verify the Diskette speed. Check the collet and the main bearings for correct lubrication.

Intermittent Read Errors: Check specially for creased or cracked Diskette jacket specially at the bottom of the read window.

Intermittent or Solid 'Not Ready' or Device Errors: Check for shorted or broken LED or solenoid cables. Care should be taken when assembling the Diskette device. All clamp screws, etc., must be tight.

Head Adjustment Procedure: Do not start a head adjustment procedure without first checking for dust or dirt in the leadscrew.

Any time you do a head adjustment, always start from the beginning and check the stepper motor wheel, leadscrew wheel, leadscrew, etc. Do not start in the middle of the head adjustment procedures.

TYPE 4 CHANNEL ADAPTER

INTRODUCTION

The type 4 CA is a type 1 CA that has been modified to operate in EB (extended buffer) mode and CS (cycle steal) mode as well as in the type 1 CA mode (non-EB mode). Since the type 4 CA is a modified type 1 CA, the description of the type 1 CA in Section 8 is applicable to the type 4 CA and is not repeated in this section. This section covers the differences between the type 4 CA and the type 1 CA.

EP/NCP Burst Size Options

The emulation program and non-licensed NCP programs have no generation option to control the amount of data passed to the channel adapter; these programs always transfer four bytes or less in non-EB/CS mode. The maximum cycle steal transfer for licensed IBM NCP programs (ACF/NCP/VS) will be the sysgened buffer size. See the NCP sysgen manual GC30-3008 for buffer-size options.

Main Differences Between Type 4 CA and Type 1 CA

- EB mode

  The type 4 CA uses a separate 9 X 32 EB local-store data-buffer array for EB inbound and outbound data transfers.

  When in EB mode, the type 4 CA can transfer a maximum of 32 bytes of data across the channel during each data transfer burst with program intervention required only before and after each burst.

  Good parity is not set into the EB local store by a power-on reset or the RESET pushbutton. The 3705-80 control program must assure good parity is set in the EB local store before it is accessed.

  EB mode is reset by a power-on reset, the RESET pushbutton, a CA diagnostic reset, a system reset, an Output X'62' with bit 0.7=1, an Output X'6C' with bit 0.0=0, or when the not-initialized state is entered. It is *not* reset by a selective reset.

- CS mode

  When in cycle steal mode, the first two bytes (addresses 0 and 1) of the 9 X 32 EB local-store data-buffer array are used as the cycle-steal buffer register for CS inbound and outbound data transfers.

  When in CS mode, the type 4 CA can transfer a maximum of 256 bytes of data across the channel during each data transfer burst with program intervention required only before and after each burst.

  EB and CS modes are mutually exclusive. An Output X'6C' with bits 0.0 (EB mode) and 0.1 (CS mode) on will default to EB mode.

- Expanded BSC Control Character Recognition

  The type 4 CA, when in EB or CS mode and the ESC (emulator subchannel) mode is enabled, recognizes the following BSC control characters when they are in the inbound data stream from the host processor:

  - ETB and ETX-CA stops the inbound data transfer and requests a level 3 interrupt.
  - DLE-STX sequence—CA stops monitoring the transparent data.
  - SYN—when the CA detects (n)* consecutive SYN characters, the CA stops the inbound data transfer and requests a level 3 interrupt.

- Non-EB/CS mode

  The type 4 CA uses the same 4 X 18 non-EB/CS local store array as the type 1 CA. The type 4 CA uses it for non-EB inbound/outbound-data transfers and for Address In and emulator subchannel Status In presentation to the channel.

- Initial Selection 'short control unit busy' status

  Any start I/O to the ESC address when the type 4 CA has disconnected from the channel because of the 4, 8, or 16 byte burst jumpering receives a Status In of X'70' (control unit busy). See H-220 or H-270.

- Two Type 4 CAs

  When two type 4 CAs are installed in a 3705-80, they share the same input/output codes so the 3705-80 control program must select the desired CA. See Output X'67' on page H-120.

- Automatic selection between two type 4 CAs by level 3 interrupt priority

  The priority selection circuits in each CA assign a priority level to each type 4 CA level 3 interrupt, compare the priorities in the two CAs, and then select the CA with the highest priority for servicing. The 3705-80 control program has control over when to 'prime' this priority select circuit and when the CA selection is made (see H-230).

- IPL and ROS implementation

  – One type 4 CA

  Uses the type 1 CA ROS and IPL sequencing.

  – Two Type 4 CAs

  Use N-Channel ROS.

  Either type 4 CA in a configuration containing two type 4-CAs can accept an IPL command. A special Sense command status is used to break contention if two or more host processors simultaneously try to IPL the 3705-80.

*Value of (n) is determined by the 3705-80 control program.

An IPL attempt by a host processor must consist of a Sense command, command-chained to a Write IPL command. If an IPL is in progress from either type 4 CA when a host processor attempts an IPL, the 3705-80 N-channel ROS returns an ending status of 'CE, DE, UE' to the Sense command. The unit exception breaks the command chaining and the Write IPL command is not executed by the host processor channel. This host processor program enters a timeout period waiting for an asynchronous device-end from the 3705-80 to indicate that the IPL operation has been completed. If the asynchronous device-end does not occur prior to the timeout completion, this host processor program assumes the IPL in progress was not successful and executes a Write IPL command that is not chained from a Sense command.

When an IPL operation is successfully completed, the control program just loaded returns an asynchronous device-end to all channels attached to the 3705-80 except the channel over which the IPL occurred. This 'DE' signals the host processor programs associated with these channels that the 3705-80 has just completed the transition from a not-ready state to a ready state.

– Remote Program Loader (RPL)

One type 4 CA can be located in the 3705-80 with the RPL. See E-000 for board locations. The RPL requires a RPL ROS while the channel adapter, requires a different ROS as previously defined. The RPL logic selects which ROS is loaded at IPL phase 2 time.

WARNING

When operating with a type 4 CA in an NCP (PEP included) environment, do not attempt to disable a channel interface unless the 3705-80 network has been quiesced or a system reset has occurred. If this procedure is not followed, the NCP may, while disabled, attempt to send asynchronous status which inhibits the CA4 from becoming enabled again.

Note: *With N-Channel ROS both enabled type 4 CAs will accept commands over their NSC addresses.*

Type 4 CA Configurations

Up to two type 4 CAs can be installed in a 3705-80; one in the A4 board position and one in the B1 board position of the A-gate. Two type 4 CAs can be used in a PEP System with the enabled NSC(s) handling the NCP data transfers and the ESC addresses handling the EP data transfers. The channel adapters in a PEP system can be attached to the same or different host processors. A type 4 CA cannot be combined with a type 1 CA.

Type 4 CAs can have a two-channel switch but whenever two channel adapters are installed in the 3705-80, neither adapter can have a two-channel switch. Only one type 4 CA can be combined with the remote program loader.

The type 4 CA can be attached to a selector, byte multiplexer, or block multiplexer channel of a system/370, a 43XX Processor, a 303X Processor, or a 3081 Processor Complex or to a byte multiplexer channel of a system/360.

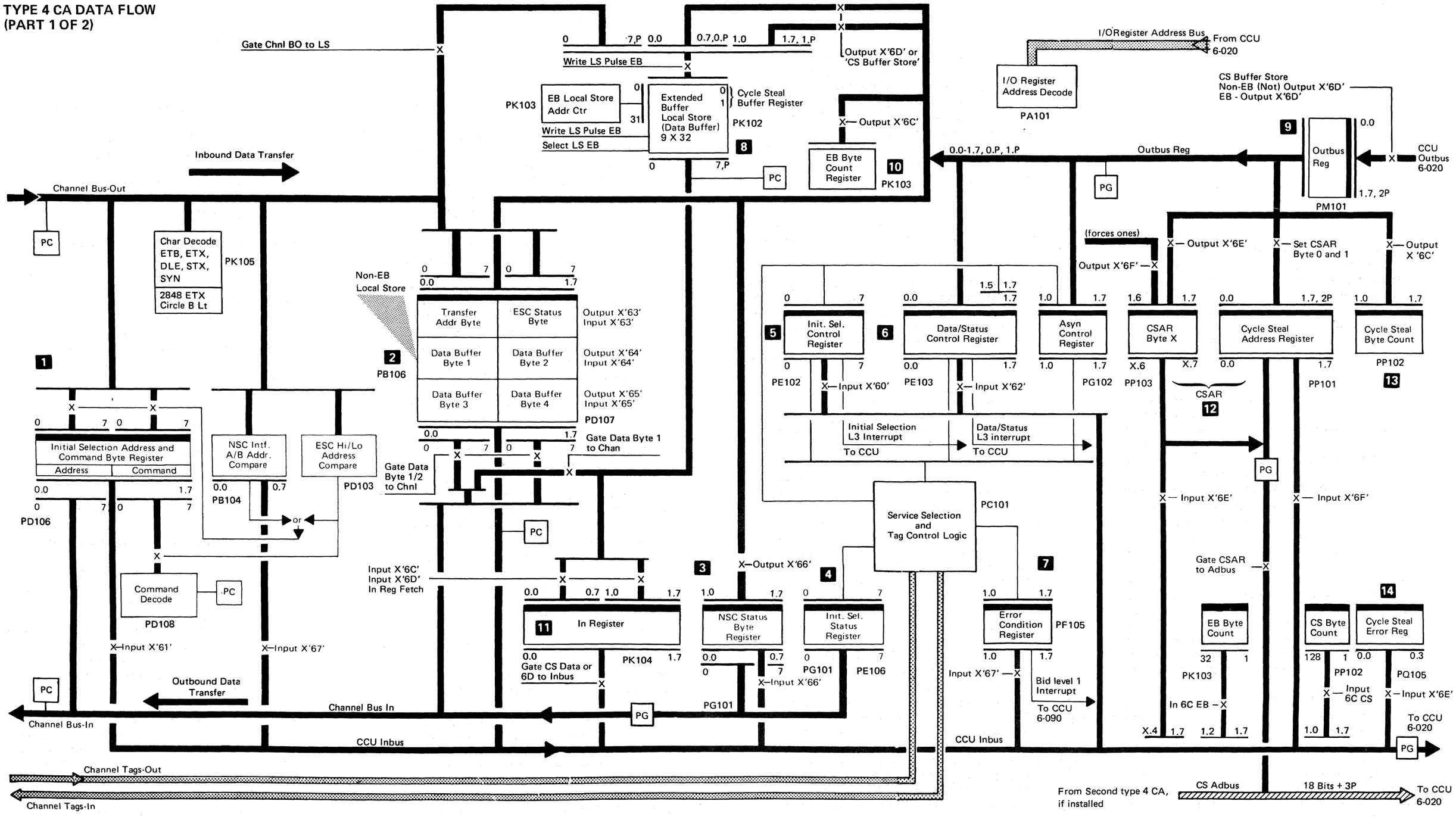
CE Burst Length Jumper Option

Depending on which host processor the CA4 is attached to, the CE installs jumpers to select a burst size of 4, 8, or 16 bytes. If no jumpers are installed, the burst will be the byte count set up by the control program, up to 32 bytes in EB mode and up to 256 bytes in CS mode. If a burst size of 4, 8 or 16 bytes is chosen the CA4 will transfer the number of bytes specified by the plugging option, disconnect from the channel to allow other channel activity to occur then reconnect to transfer another burst of data. This disconnecting and reconnecting will continue until the full byte count has been transferred.

EXAMPLE: (Assume the CA4 is plugged for 8 byte burst length)

1. The control program sets up a 32 byte EB mode transfer.
2. The CA4 transfers 8 bytes, then disconnects from the channel interface.
3. The CA4 reconnects to the channel, transfers 8 more bytes, then disconnects.
4. Step 3 is repeated two more times.
5. The CA4 interrupts the control program indicating all 32 bytes have been transferred. The interrupt occurs only after the full byte count (32 in this example) has been transferred. The burst length jumpering option is transparent to the control program. The duration that the CA4 will disconnect from the channel is also a plugging option see CA4 logic page PA049 for burst-length and duration of delay between bursts plugging information.

TYPE 4 CA DATA FLOW (PART 1 OF 2)



TYPE 4 CA DATA FLOW (PART 2 OF 2)

1 Initial Selection Address and Command Register

This register contains the I/O device address byte and command byte presented to the channel adapter during initial selection. The register can be accessed by Input X'61' which should be executed only if the type 4 channel adapter initial or data/status level 3 interrupt request is set. See H-050 for Input X'61' description. This register is referred to as the SIO register in the ALD's.

2 Local Store (Non-EB Mode)

The local store provides buffering for the I/O address byte used in all data and status transfer sequences initiated by the 3705-80. Buffering for up to four bytes of data for inbound and outbound data transfers in non-EB mode is provided here also.

The control program loads or accesses the I/O device address and the emulation status byte with Output X'63' and Input X'63' respectively. The data bytes are transferred with X'64' or X'65' instructions, see chart below.

NON-EB MODE

Data Byte	Data Transfer	
	Out	In
1	X'64'	X'64'
2	X'64'	X'64'
3	X'65'	X'65'
4	X'65'	X'65'

3 NSC Status Byte Register

The current status of the NSC is maintained in this register and gated over the channel interface during NSC status transfer sequences. The control program should set the NSC status by executing an Output X'66' instruction. The control program has access to this register with the Input X'66' instruction.

4 Initial Selection Status Register

The status byte is generated and presented to the channel from this register during initial selection sequences except under the following conditions.

- An initial selection sequence occurs for the native mode subchannel before the NSC status byte provided by the control program has been accepted. The NSC status byte from the NSC status register is presented instead of the hardware generated status.
- An initial selection sequence occurs for an emulation address when the control program has signaled that an ESC status transfer sequence is required and has signaled that ESC Test I/O status is available. The ESC status byte provided by the program is presented instead of hardware generated status.

5 Initial Selection Control Register

The information in this register identifies the event causing the type 4 channel adapter initial level 3 interrupt request to be set. The register can be accessed by Input X'60', which should be executed only if the interrupt request is set.

6 Data/Status Control Register

The information in this register controls and identifies events that cause the type 4 channel adapter data/status level 3 interrupt request to be set. The register can be accessed by Input X'62', which should be executed only if the interrupt request is set. The control program can perform various control functions by setting or resetting bits in this register with an Output X'62' instruction. The instruction should be executed only when the control program is servicing a type 4 CA level 3 interrupt request.

7 Error/Condition Register

The error/condition register is a collection of latches that are set when the CA detects an error or an occurrence of specific asynchronous conditions. The 3705-80 control program has access to this register with an Input X'67' instruction, (see page H-110). The errors indicated by the error/condition register cause type 4 CA error interrupts (see page H-380).

8 Extended Buffer Local Store

The extended buffer local store provides for buffering up to 32 bytes of data for inbound and outbound data transfers when in extended-buffer mode. The first two data bytes are transferred to the In register by an Input X'6C'. The Input X'6D' instruction transfers the two bytes in the In register to a CCU general register before loading the In register with the next two bytes from the EB local store. Sixteen Input X'6D' instructions are required to transfer the data in the entire extended buffer. All 32 bytes of data for an outbound data transfer are loaded into the EB local store, two per instruction, by Output X'6D' instructions.

9 Outbus Register

The outbus register buffers two data bytes for loading into the EB local store. The even data byte is loaded from the outbus register to the EB local store, followed by the odd data byte to the next sequential EB local store address.

10 EB Byte Count Register

This register buffers the requested byte count (up to 32) for inbound or outbound data transfers when in EB mode.

11 EB In Register

This register receives the even, then odd, data bytes from the EB local store for transfer to the CCU.

12 Cycle Steal Address Register

The byte X register and the cycle steal address register contain the address bits of the storage data buffer location for the first data byte to be transferred to or from storage by cycle stealing. The byte X register contains the two high order address bits and the cycle steal address register contains the 16 low order address bits. The two registers combined form the CSAR. The CCU updates CSAR to the next sequential half-word storage address at the completion of a cycle steal transfer.

13 Cycle Steal Byte Count

This register buffers the requested CS byte count (up to 256 bytes) for inbound or outbound data transfers when in CS mode.

14 Cycle Steal Error Register

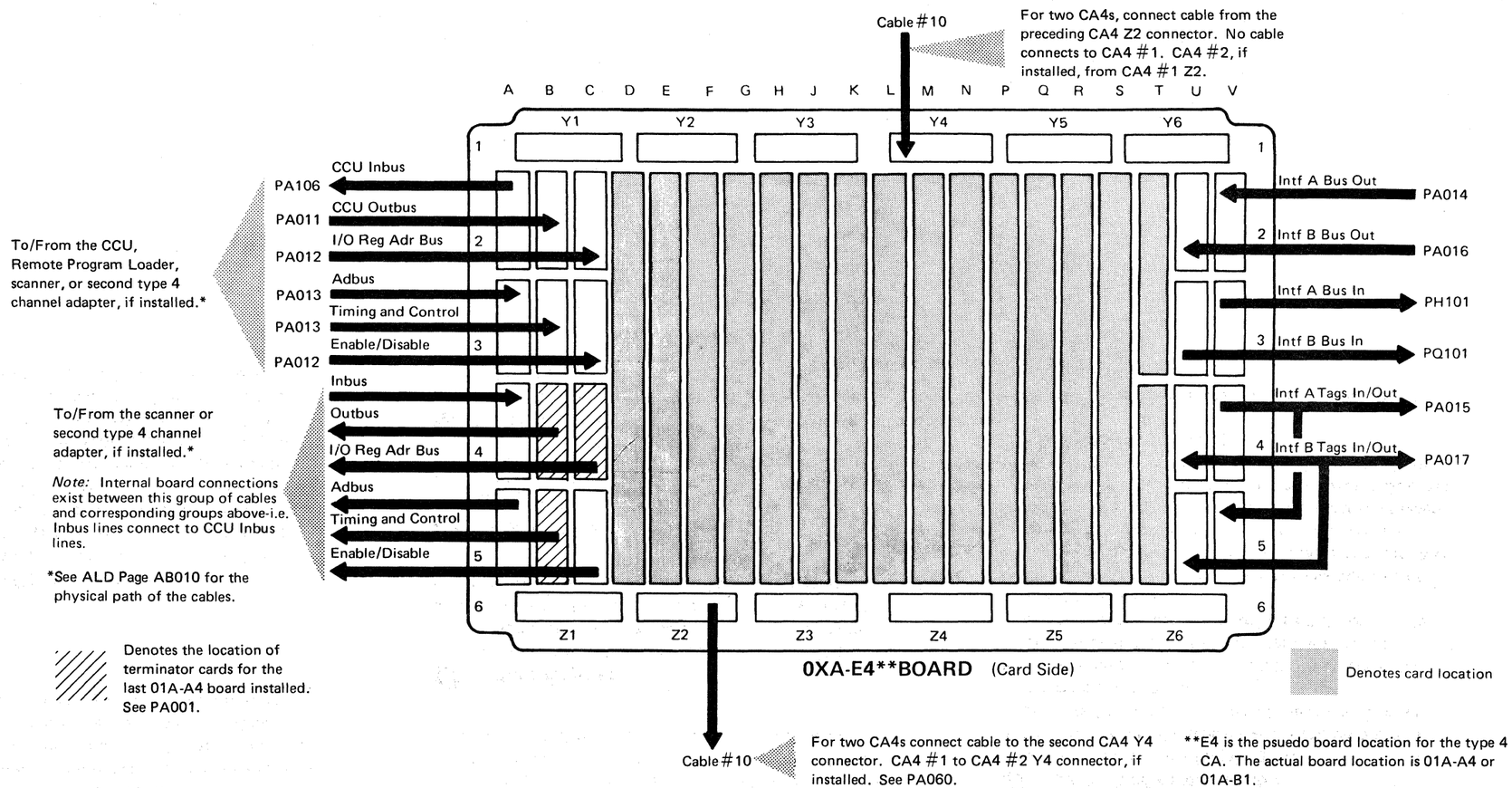
This register is set by the following errors:

- CS outbus error—the type 4 CA sets this bit during a cycle steal operation when data from storage contains incorrect (even) parity.
- CS inbus error—the type 4 CA sets this bit when the CCU raises 'bad data' to signal that the CCU has received bad data (even parity) from the type 4 CA on a cycle-steal data transfer.
- CS address bus error—the type 4 CA sets this bit when the CCU raises 'SAR even parity' to signal that the CCU has received incorrect parity on the CS address bus.
- CS address exception—the type 4 CA sets this bit when the CCU raises 'address error' to signal that the CCU has received an address from the type 4 CA that is within a protected section of storage.

The type 4 CA requests a level 1 interrupt when any of these bits are set.

CARD FUNCTIONS AND LOCATIONS

Card Loc	ALD Page	Function
E4F2	PA101	I/O Decodes
	PA102	I/O Feedback-Level 1 Bid
	PA103	Basic Clocking
	PA104	Inbus Dot Byte 0
	PA105	Inbus Dot Byte 1
	PA106	Inbus Byte 0
	PA107	Inbus Byte 1
	PA108	Selected Latch and L3 Bids
E4P2	PB101	Channel Intf Tags and Controls
	PB102	Channel Intf A Receivers
	PB103	Interface A Control
	PB104	Channel Address Jumpering and Channel Parity Check
	PB105	Non-EB/CS Local Store Byte 0 Assembler
	PB106	Non-EB/CS Local Store Byte 0
	PB107	Interface B Address
E4N2	PC101	Channel Tags Control and Tag Clock
	PC 102	Channel Tags Control-Start I/O, and Operational In
	PC103	Channel Tags Control and Tag In Latches
	PC104	Channel Tags Control-Stack, Chaining, Stop, or Halt I/O
	PC105	Channel Tags Control, Enable, and Selective System Reset
	PC106	Channel Tag Control Powering
E4M2	PD101	Channel Bus-Out Repower
	PD102	Low Address Jumpers
	PD103	Low Address Logic
	PD104	High Address Jumpers
	PD105	High Address Logic
	PD106	Start I/O Adr Reg and Command Reg
	PD107	Non-EB/CS Local Store Byte 1
	PD108	Command Decode
	PD109	CCU Outbus Inversion
E4L2	PE101	CCU Outbus Termination
	PE102	Initial Selection Control
	PE103	Service Transfer Control
	PE104	Byte Transfer Count (Non-EB/CS)
	PE105	Service Transfer
	PE106	Initial Status Generation
	PE107	OR Dots Byte 0
E4K2	PF101	Input/Output Control
	PF102	Assembler and Non-EB/CS Local Store Cntl
	PF103	NSC Control
	PF104	RN Asynchronous Information
	PF105	Error Latches
E4T2	PG101	NSC Status Register
	PG102	Asynchronous Interrupt Control
E4Q2	PH101	Intf A Bus-In Drivers Bits 0,1,2
	PH102	Intf A Bus-In Drivers Bits 3,4,5
	PH103	Intf A Bus-In Drivers Bits 6,7,P
	PH104	Intf A Tag-In Drivers Op In, Adr In, and Service In
	PH105	Intf A Tag-In Drivers Sel In, Req In, and Status In
	PH106	Select Out Relay Driver and Control Gating
	PH107	Bus-In Error Latch and Reset Generation
E4T4	PJ101	Intf A Select Out Relays
	PJ102	Intf B Select Out Relays



Card Loc	ALD Page	Function
E4J2	PK101	CCU Outbus Register Byte 0 and Channel Bus Out Repowering
	PK102	Extended Buffer Local Store and Assembler
	PK103	EB Local Store Address Counter and Count Control
	PK104	EB Local Store to Inbus
	PK105	BSC Control Character Recognition and Detect all zeros on CCU Outbus Byte 0
	PK106	Burst Length Jumpering
	PK107	EB Local Store to Drivers
E4H2	PL101	BSC Character Recognition Control
	PL102	I/O Decodes and Extended Buffer Mode Lt
	PL103	Extended Buffer Controls
	PL104	Burst Length Controls and Force Short CU Busy
	PL105	Both Local Store Gate Controls and Local Store Cycle Reset

Card Loc	ALD Page	Function
E4G2	PM101	CCU Outbus Byte 1 Repower, Zero Detect, and Priority Sample Generation
	PM102	CA L3 Priority Determination and Gating Priority to CA4 #2, if installed.
	PM103	Priority Control Logic
	PM104	Repowering
E4D2	PP101	CS Address Register
	PP102	CS Counter and Count Compare
	PP103	CS Byte X and Adbus Gating
	PP104	CS Byte 0 and 1 Gating to Inbus
	PP105	Force 1 to Byte X and Repowering
	PP106	Initial Sel Rst Control and Svc Sel Rst Control
E4E2	PQ101	CS Sequencing Control
	PQ102	CS Buffer Control and Odd Byte Transfer Control
	PQ103	CS Decodes and Inbus Gating
	PQ104	CS Mode Latch Counter and Byte X Control
	PQ105	CS Check Latches
	PQ106	Repowering

Card Loc	ALD Page	Function
E4R2	PR101	Intf B Bus Out Receivers Bits 0-3
	PR102	Intf B Bus Out Receivers Bits 4-7
	PR103	Intf B Bus Out Rcvr Bit P and Tags Out Rcvr Op Out, Select Out
	PR104	Intf B Tags Out Rcvr Adr Out, Cmd Out, Svc Out, and Supp Out
	PR105	Enable B Latch
	PR106	Intf B NSC Address Valid
E4S2	PS101	Intf B Bus-In Drivers Bits 0,1,2
	PS102	Intf B Bus-In Drivers Bits 3,4,5
	PS103	Intf B Bus-In Drivers Bits 6,7,P
	PS104	Intf B Tag-In Drivers Op In, Adr In and Service In
	PS105	Intf B Tag-In Drivers Sel In, Req In, and Status In
	PS106	Select Out Relay Driver and Control Gating
	PS107	Bus-In Error Latch and Reset Generation

INPUT AND OUTPUT INSTRUCTIONS

The type 4 channel adapter relies on the 3705-80 control program to use input and output instructions to control data transfers. The control program initiates channel data and status transfers, and transfers data between the CA and the CCU with input and output instructions.

Each input or output instruction addresses an external register. The input instructions gate the external register to CCU general registers via the CCU Inbus. Output instructions gate CCU general registers to CA registers via the CCU Outbus. The 'I/O register address bus' is decoded in the type 4 CA.

Executing an Input or Output X'60', X'61', X'62', X'63', X'64', X'65', X'66', X'6C', X'6D', X'6E', or X'6F' when the CA is actively handling a data or status transfer sequence causes an in/out check to occur; see H-380.

Control Panel Access to CA Registers

Type 4 CA registers X'60' through X'66' should be accessed from the control panel with Input or Output instructions only when either of the type 4 CA level 3 interrupts are pending.

To ensure that this interrupt remains pending, the 3705-80 should be in either Program Stop or Hard Stop mode before these instructions are executed from the control panel.

If these conditions are not met, the following occurs:

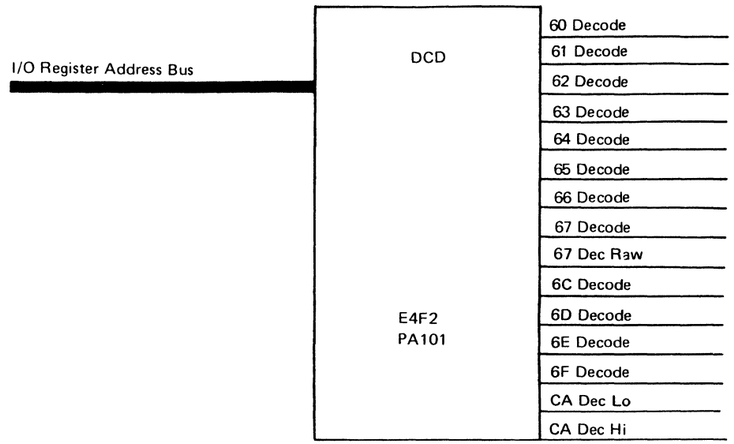
1. If the type 4 CA is in the process of a data or status transfer sequence and an Input or Output X'60' through X'66' or X'6C' through X'6F' is initiated from the control panel, the type 4 CA hardware:
   a. Causes a type 4 CA level 1 interrupt request.
   b. Sets the type 4 CA In/Out instruction accept latch.
   c. Gates X'0000' onto the CCU Inbus to be displayed in display B if the instruction is an Input.
   d. Does not recognize Output instructions.
2. If the type 4 CA is not transferring data or status and a type 4 CA level 3 interrupt request is not pending, one of the following occurs:
   a. For Input X'60', X'61', or X'66' instructions, either the instruction is executed without error or, if at the same time the instruction is being executed, the CA is being selected by the host processor channel, the CCU may sample invalid data from the type 4 CA. The data in display B should be considered invalid.
   b. For Output X'66' instructions, either the instruction is executed without error or, if at the same time the instruction is being executed, the type 4 CA is being selected by the host processor channel, a type 4 CA channel bus in check and a type 4 CA level 1 interrupt request may be set or a processor data check may be detected at the host processor.
3. If the type 4 CA is in the process of presenting ESC status to a Test I/O issued to an ESC address, and an Input X'60' through X'66' or an Output X'62' through X'66' is executed, one of the following occur:
   a. The instruction executes without error.
   b. If at the same time any of these instructions are being executed, the type 4 CA is being selected by the host processor channel, either a type 4 channel bus in check, a type 4 CA local store, a level 1 interrupt request, or a processor data check may occur.

Input and Output X'67' can be executed from the 3705-80 control panel without causing an error.

Loading Data Into the Extended Buffer From the Control Panel

Simulate the following instructions from the control panel using the procedures on Page 1-140:

Input X'6C'	
Output X'6C'	8000 (data in ADDRESS/DATA switches A-E)
Input X'6D'	This steps the EB byte counter by 2.
Output X'6D'	XXXX (data in ADDRESS/DATA switches A-E). This data is loaded into EB LS data buffers 2 and 3.
Output X'6D'	Repeat the Output X'6D' for each two data bytes desired. The data in the ADDRESS/DATA switches may be changed. *Do not* perform another Input X'6D' until you have loaded the number of bytes desired. The 31st and 32nd data bytes are loaded into EB LS data buffers 0 and 1 (the EB byte counter goes from 11111 to 00000).
Output X'6D'	
Input X'6C'	Resets EB byte counter.
Input X'6D'	The first Input X'6D' transfers the 31st and 32nd data bytes loaded from the control panel to the inbus.
Input X'6D'	The second Input X'6D' transfers the first two data bytes loaded. Consecutive Input X'6D's transfer the data bytes in the same sequence as they were loaded by consecutive
Input X'6D'	Output X'6D's.



I/O Reg Bus Bits								Decode
0	1	2	3	4	5	6	7	
OP Reg Bits								
1.4	0.1	0.2	0.3	1.0	1.1	1.2	1.3	
X	1	1	0	0	0	0	0	60
X	1	1	0	0	0	0	1	61
X	1	1	0	0	0	1	0	62
X	1	1	0	0	0	1	1	63
X	1	1	0	0	1	0	0	64
X	1	1	0	0	1	0	1	65
X	1	1	0	0	1	1	0	66
X	1	1	0	0	1	1	1	67
X	1	1	0	1	1	0	0	6C
X	1	1	0	1	1	0	1	6D
X	1	1	0	1	1	1	0	6E
X	1	1	0	1	1	1	1	6F

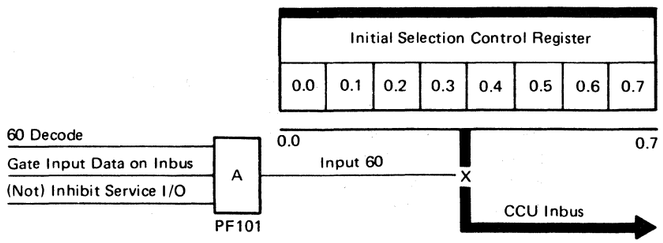
Op Reg bit 1.4 = { 1 for Input / 0 for Output

Input X'60' Instruction

Input X'60' transfers the contents of the initial selection control register into a CCU general register. The 3705-80 control program uses this instruction to determine the exact cause of a type 4 CA initial selection level 3 interrupt.

An Output X'60' resets the initial selection control register and the L3 interrupt request resulting from the initial selection.

The type 4 CA and type 1 CA Input X'60' instructions are identical.



Bit	Logic Page	Function
0.0	PE102	Input Initial Selection State*
0.1	PC105	Input Initial Interface Disconnect
0.2	PC105	Input Initial Selective Reset
0.3	PE102	Input Initial Chan Bus Out Check
0.4		0
0.5	PE102	Input Stack Initial
0.6	PF103	NSC Status Cleared
0.7	PC105	Input System Reset

*Normal Initial Selective

E4M2 PD106

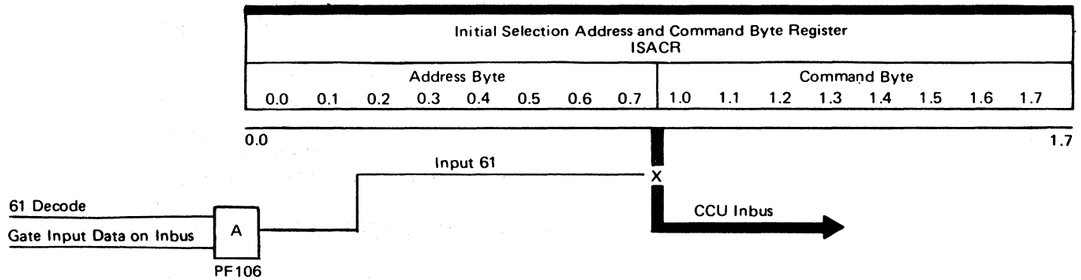
Input X'61' Instruction

Input X'61' transfers the contents of the initial selection address and command byte register into a CCU general register. During an initial selection sequence, a type 4 CA initial selection level 3 interrupt is requested, and the 3705-80 control program must investigate the subchannel address and command causing the interrupt. Byte 0 is the address to which the command in byte 1 was issued.

The 3705-80 control program must store the address and command because the host processor can send the CA a new command before the 3705-80 control program has completed the previous one when in ESC mode. The 3705-80 control program must also control the CA action for each command.

An Output X'61' instruction has no effect on the channel adapter.

The type 4 CA and type 1 CA Input X'61' instructions are identical.



Output X'62' Instruction

This instruction initiates inbound and outbound data transfers and status presentations. The 3705-80 control program uses this instruction to control CA4 action and, when not in EB or CS mode, to specify the number of bytes of data to transfer across the channel interface on a channel data transfer.

Non-EB/CS Mode

Byte Count	Bits 1.5	1.6	1.7
1	0	0	1
2	0	1	0
3	0	1	1
4	X	0	0

EB or CS Mode

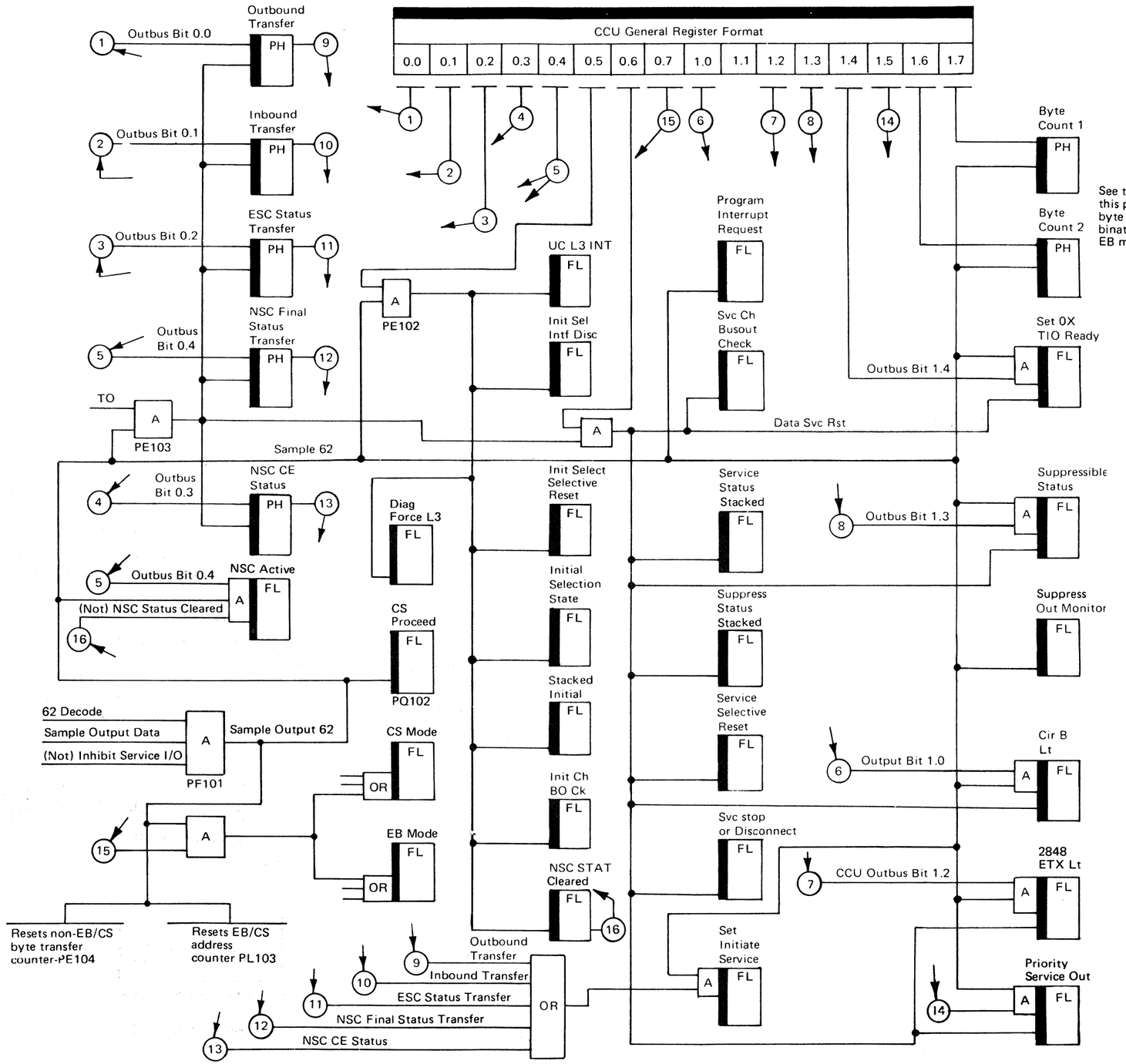
SYN Chars	Bits 1.6	1.7
1	0	1
2	1	0
3	1	1
4	0	0

X This bit may be on or off for a byte count of four.

Summary of Output X'62' bit definitions and ALD locations

Bit	Card LOC	ALD Page	Function
0.0*	E4L2	PE103	1 = set; 0 = rst outbound transfer
0.1*	E4L2	PE103	1 = set; 0 = rst inbound transfer
0.2*	E4L2	PE103	1 = set; 0 = rst ESC status transfer
0.3*	E4L2	PE103	1 = set; 0 = rst NSC channel end status
0.4*	E4L2	PE103	1 = set; 0 = rst NSC final status transfer
	E4K2	PF103	Set NSC active
0.5	E4K2	PF103	Reset NSC status cleared
	E4G2	PM103	Reset force initial selection L3 interrupt
	E4L2	PE102	Reset initial channel bus out check
	E4L2	PE102	Reset stacked initial
	E4L2	PE102	Reset initial selection state
	E4L2	PE102	Reset Unit Check L3 interrupt
	E4N2	PC105	Reset initial selection interface disconnect
	E4N2	PC105	Reset initial selection selective reset
0.6	E4K2	PF104	Reset monitor for 2848 ETX
	E4K2	PF104	Reset monitor for circle B
	E4L2	PE106	Reset 0X TIO ready
	E4L2	PE105	Reset service channel bus-out check
	E4L2	PE105	Reset service status stack
	E4N2	PC104	Reset suppressible status
	E4N2	PC105	Reset service selective reset
	E4N2	PC105	Reset svc stop or disconnect
	E4N2	PC104	Reset suppress status stack
0.7	E4H2	PL102	Resets EB Mode
	E4E2	PQ104	Resets CS Mode
1.0	E4K2	PF104	Set monitor for circle B
1.1	– –	– –	This bit ignored
1.2	E4K2	PF104	Set Monitor for 2848 ETX
1.3	E4N2	PC104	Set suppressible status
1.4	E4L2	PE106	Set 0X TIO ready
1.5	E4G2	PM102	Set Priority Outbound Data Xfer Seq
1.6	E4L2	PE104	Byte count 2 } Non-EB/CS Mode } EB or CS Mode—number of SYN characters
1.7	E4L2	PE104	Byte count 1 }

*Any of these bits with 'Sample 62' set Initiate Service, E4L2, PE014



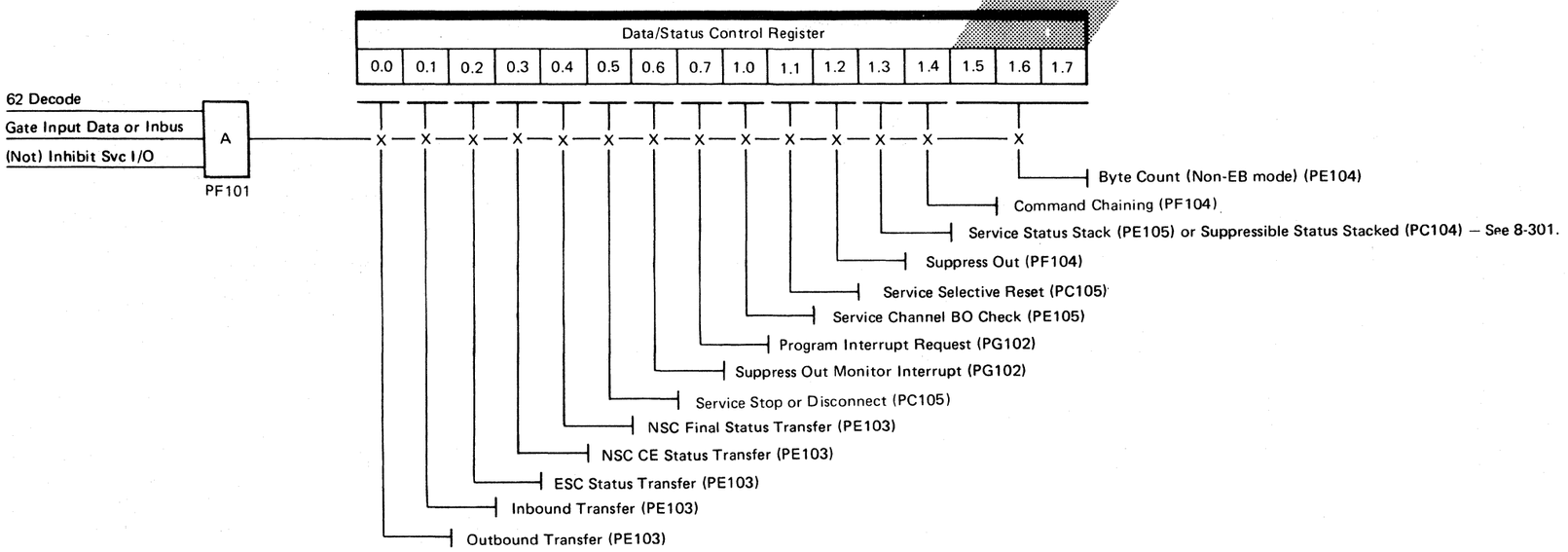
Input X'62' Instruction

This instruction transfers the contents of the data/status control register into a CCU general register. The 3705-80 control program uses this instruction to determine the exact cause of a type 4 CA data/status level 3 interrupt. The type 4 CA and type 1 CA Input X'62' instructions are identical.

Non-EB/CS mode

Count transferred to the CCU

Count	Bits		
	1.5	1.6	1.7
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0



Output and Input X'63' Instructions

The 3705-80 control program uses the Output X'63' instruction to load the subchannel address (byte 0) and ESC status byte (byte 1) into the non-EB/CS local store buffer. The CA identifies itself to the channel by gating byte 0 onto the channel bus in, during the address transfer and gates byte 1 onto the channel bus in to transfer the ESC status to the host processor. (NSC address and status take a different path, see page 8-170.)

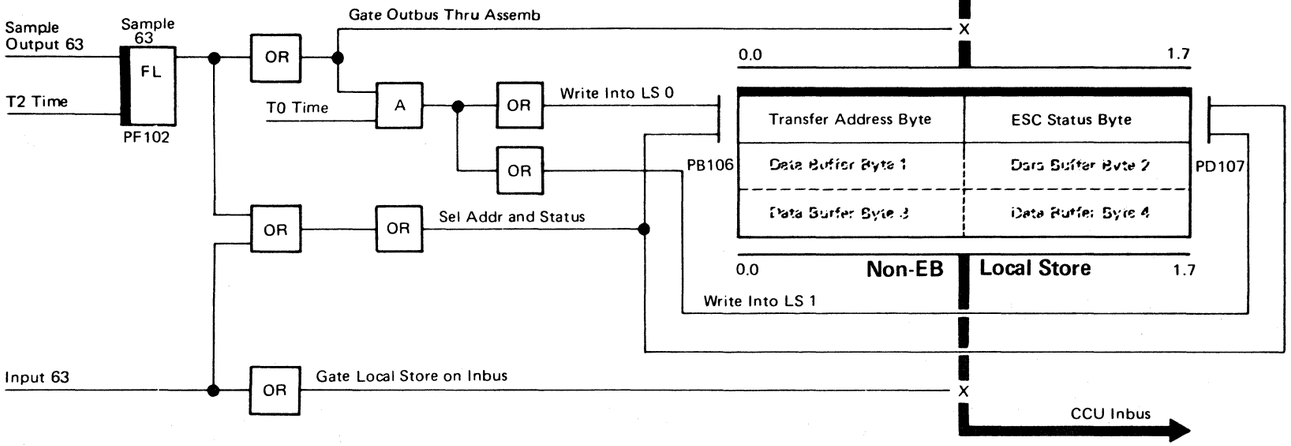
The 3705-80 control program must ensure that the correct address and status bytes are stored in the register. Otherwise, incorrect channel operation occurs.

With the Input X'63' instruction, the 3705-80 control program can determine the last subchannel address provided to the host processor. The level 3 interrupt request latch should be set for this instruction to execute.

The type 4 CA and type 1 CA Output X'63' and Input X'63' instructions are identical.

CCU Outbus Bit Definitions

Bits	Definition
0.0-0.7	Subchannel address
1.0	Attention
1.1	Status modifier (SM)
1.2	Control unit end (CUE)
1.3	Busy
1.4	Channel end (CE)
1.5	Device end (DE)
1.6	Unit check (UC)
1.7	Unit exception (UE)



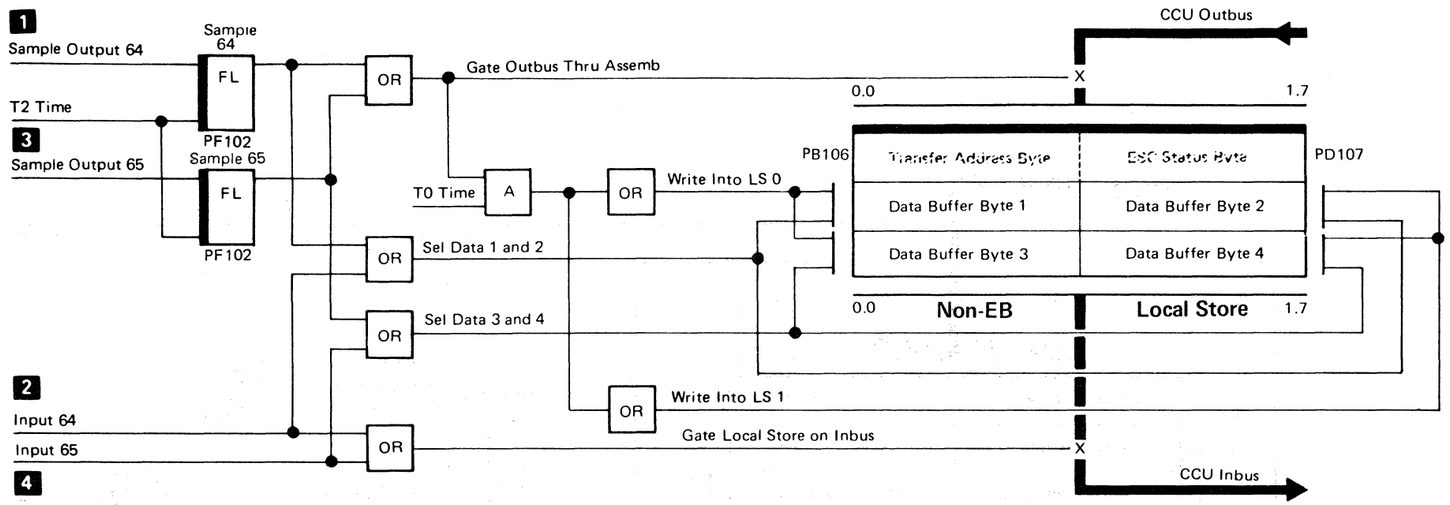
Output and Input X'64' Instruction

1
Output X'64' instruction loads non-EB/CS data buffer byte 1 and non-EB/CS data buffer byte 2 with the first two data bytes to be transferred across the channel to the host processor. These two data bytes are transferred to the host processor one byte at a time during an outbound data transfer.

The type 4 CA and type 1 CA Output X'64' instructions are identical.

2
Input X'64' transfers into a CCU general register the two data bytes that were received from the channel and stored in non-EB/CS data buffer byte 1 and non-EB/CS data buffer byte 2.

The type 4 CA and type 1 CA Input X'64' instructions are identical.



Output and Input X'65' Instruction

3
Output X'65' instruction loads non-EB/CS data buffer byte 3 and non-EB/CS data buffer byte 4 with the second two bytes to be transferred across the channel to the host processor. These two data bytes are transferred to the host processor one byte at a time during an outbound data transfer.

The type 4 CA and type 1 CA Output X'65' instructions are identical.

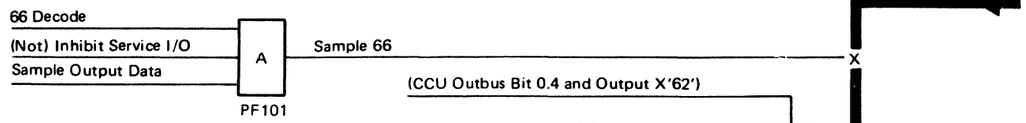
4
Input X'65' transfers into a CCU general register and the two data bytes that were received from the channel and stored in non-EB/CS data buffer byte 3 and non-EB/CS data buffer byte 4.

The type 4 CA and type 1 CA Input X'65' instructions are identical.

Output X'66' Instruction

The Output X'66' instruction loads the final status byte to be presented to the channel into the NSC Status Byte Register. Output X'66' bit 0.4=1 sets NSC Long Busy. (See PF103).

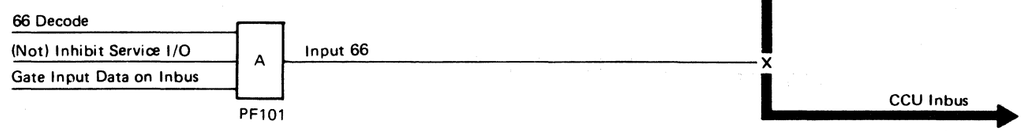
LOGIC REFERENCE PG101, PD108



Input X'66' Instruction

The Input X'66' instruction transfers the contents of the NSC status byte register into a CCU general register and forces byte 1, bits 0-7 to zeros. This instruction should be used only for diagnostic purposes and should not be used when the CA is on-line with an interface enabled.

The type 4 CA and type 1 CA Input X'66' instructions are identical.



The type 4 CA and the type 1 CA Output X'66' instructions are identical.

NSC STATUS BYTE REGISTER BIT DEFINITIONS

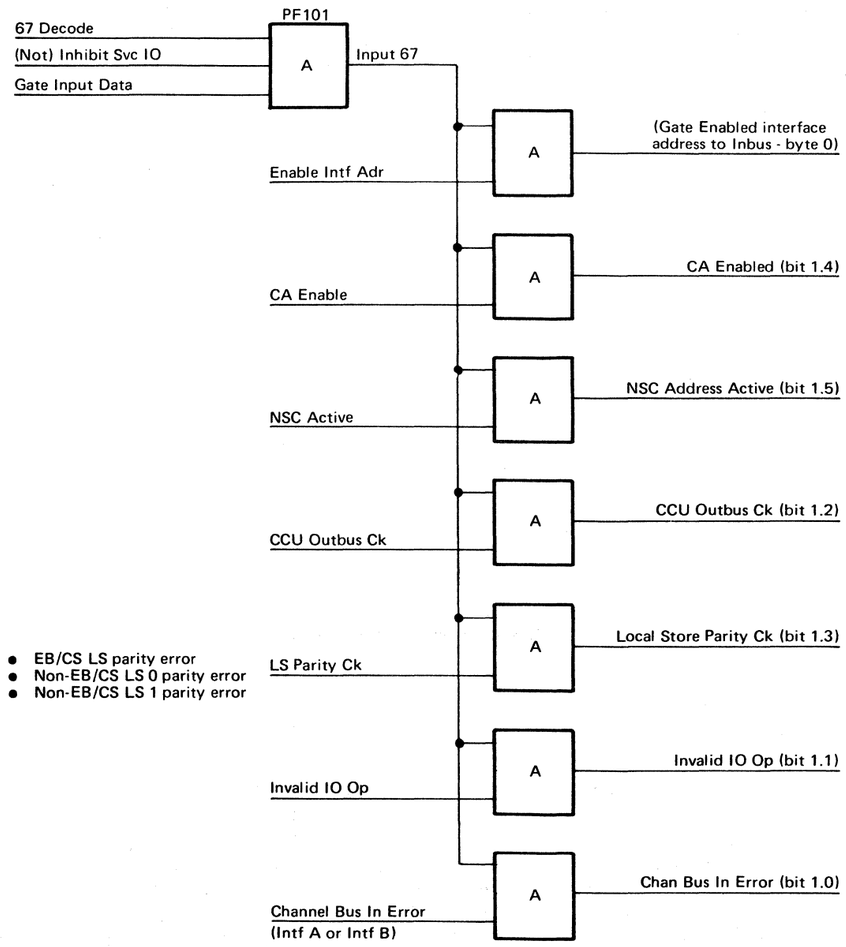
Bit 0.0 – Attention
Bit 0.1 – Status Modifier
Bit 0.2 – 0
Bit 0.3 – 0
Bit 0.4 – Channel End (CE)
Bit 0.5 – Device End (DE)
Bit 0.6 – Unit Check (UC)
Bit 0.7 – Unit Exception (UE)

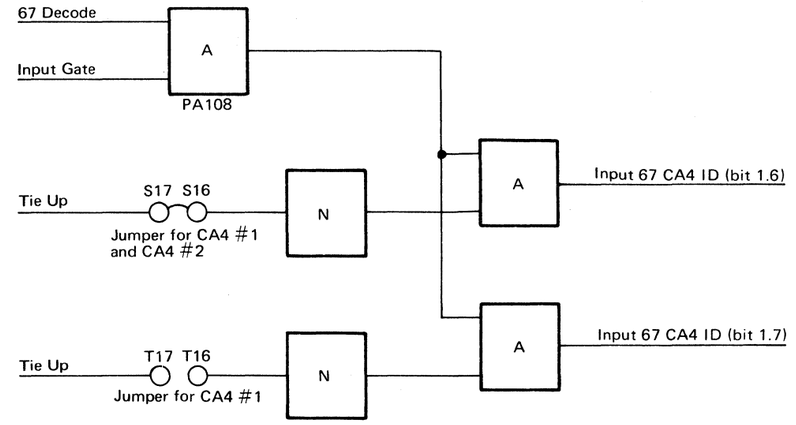
Input X'67' Instruction

The Input X'67' transfers the error condition register (H-380) and the hardware address of the NSC channel interface address to the CCU.

Summary of Inbus bits during Input X'67':

Bit	Card Loc.	Logic Page	Function
0.0-0.7	E4P2	PB104	NSC hardware address intf A
0.0-0.7	E4P2	PB107	NSC hardware address intf B
1.0	E4Q2	PH107	Chan bus in error
1.1	E4K2	PF105	Invalid I/O Op
1.2	E4K2	PF105	CCU outbus check
1.3	E4K2	PF105	Local store parity check
1.4	E4K2	PF104	CA enabled
1.5	E4K2	PF104	NSC address active
1.6-1.7	E4K2	PA108	00 – Type 4 CA #1 selected 01 – Type 4 CA #2 selected





Output X'67' Instruction

The Output X'67' instruction sets or resets the various control latches. The 3705-80 control program must execute an Output X'67' instruction to enable the CA interface before the CA can transfer data to or from the channel.

Selection Between Multiple Type 4 CAs

This instruction selects the CA4 specified by CCU outbus bits 0.5, 0.6, and 0.7 and resets the 'selected latch' on the CA4 not specified; therefore both CA4s cannot be selected at the same time. This instruction is then performed in the selected CA4. Outbus bit 0.5 must not be a one for subsequent Output X'67' instructions unless the non-selected CA4 is to be selected.

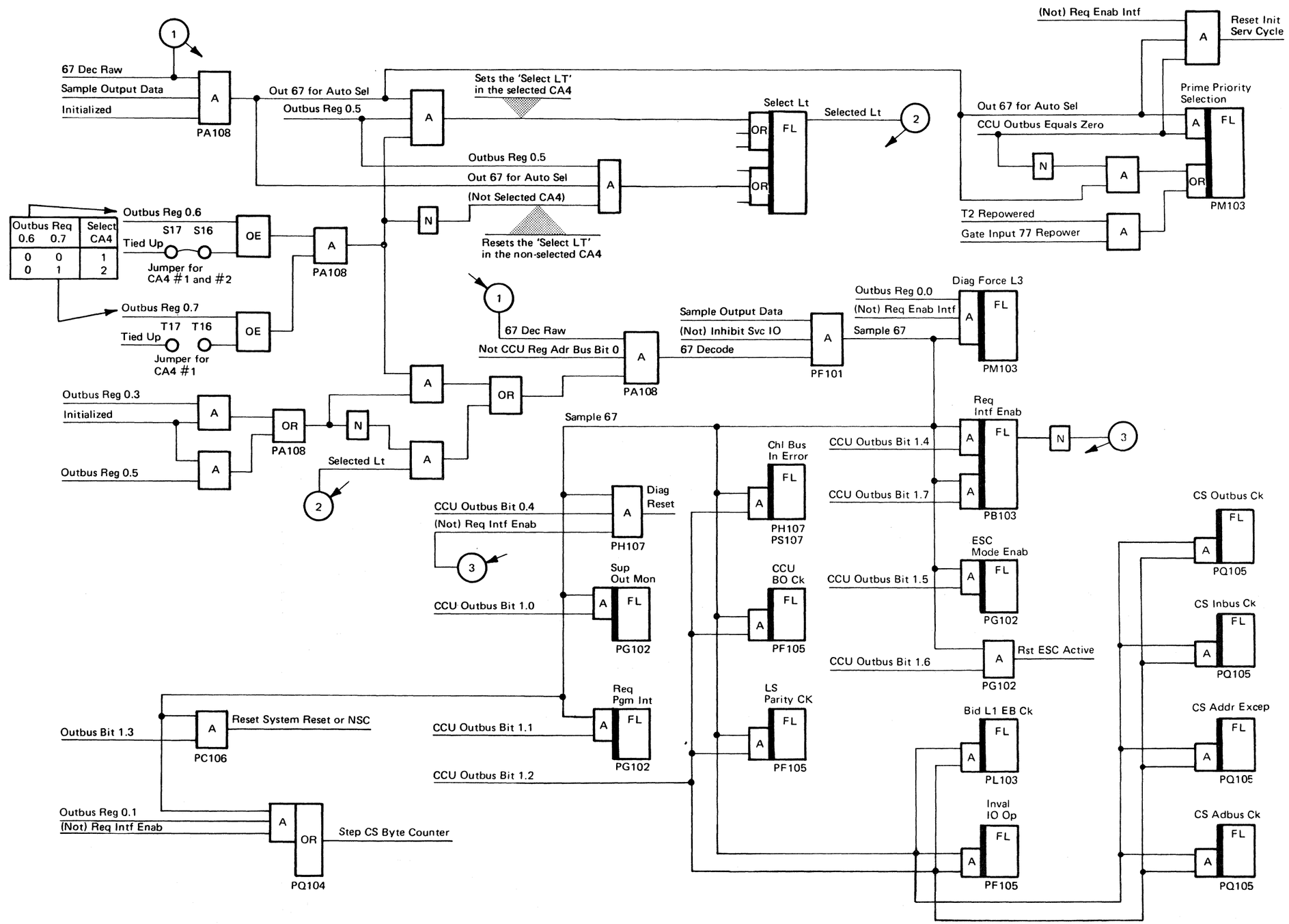
The control program can execute this instruction to the non-selected CA4 (bits 0.6, 0.7) by setting outbus bit 0.3 to one. The status of each CA4's 'selected latch' is not changed but the Output X'67' instruction is performed in the non-selected CA4 (to request a "program requested interrupt" for example). Bits 0.3 and 0.5 are mutually exclusive and both should never be on during the same output X'67' instruction.

Priming L3 Interrupt Priority Selection

An Output X'67' instruction, with all outbus bits zero, primes the CA4 priority selection circuit in the selected CA4 and forces a diagnostic data/status interrupt if appropriate.

Summary of Outbus bits during Output X'67'

Bit	Card Loc.	ALD Page	Function
0.0	E4G2	PM103	Diagnostic force initial selection interrupt
0.1	E4E2	PQ104	Diagnostic force byte transfer cycle steal mode
0.2	——	——	Not Used
0.3	E4F2	PA108	Perform Output X'67' on CA4 specified by bits 0.6 and 0.7
0.4	E402	PH107	Diagnostic reset
0.5	E4F2	PA108	0=Leave current CA4 selected 1=Select CA4 specified by bits 0.6 and 0.7
0.6, 0.7	E4F2	PA108	00 = Select CA4 #1 01 = Select CA4 #2
1.0	E4T2	PG102	Set suppress out monitor int
1.1	E4T2	PG102	Set request program interrupt
1.2	E4K2	PF105	Reset invalid I/O Op
		PF105	Reset local store parity check
		PF105	Reset CCU outbus check
		PH107	Reset channel bus in error (interface A)
		PS107	Reset channel bus in error (interface B)
		PL103	Reset bid level 1 EB check
	E4E2	PQ105	Reset CS outbus check
		PQ105	Reset CS inbus check
		PQ105	Reset CS address exception
		PQ105	Reset CS adbus check
1.3	E4N2	PC106	Reset 'system reset' or 'NSC'
1.4	E4P2	PB103	Request interface enable
1.5	E4T2	PG102	Set ESC mode enable
1.6	E4T2	PG102	Reset ESC active
1.7	E4P2	PG103	Reset interface enable



Input X'6C' Instruction

(Type 4 CA Extended Buffer/Cycle Steal Mode Control Register)

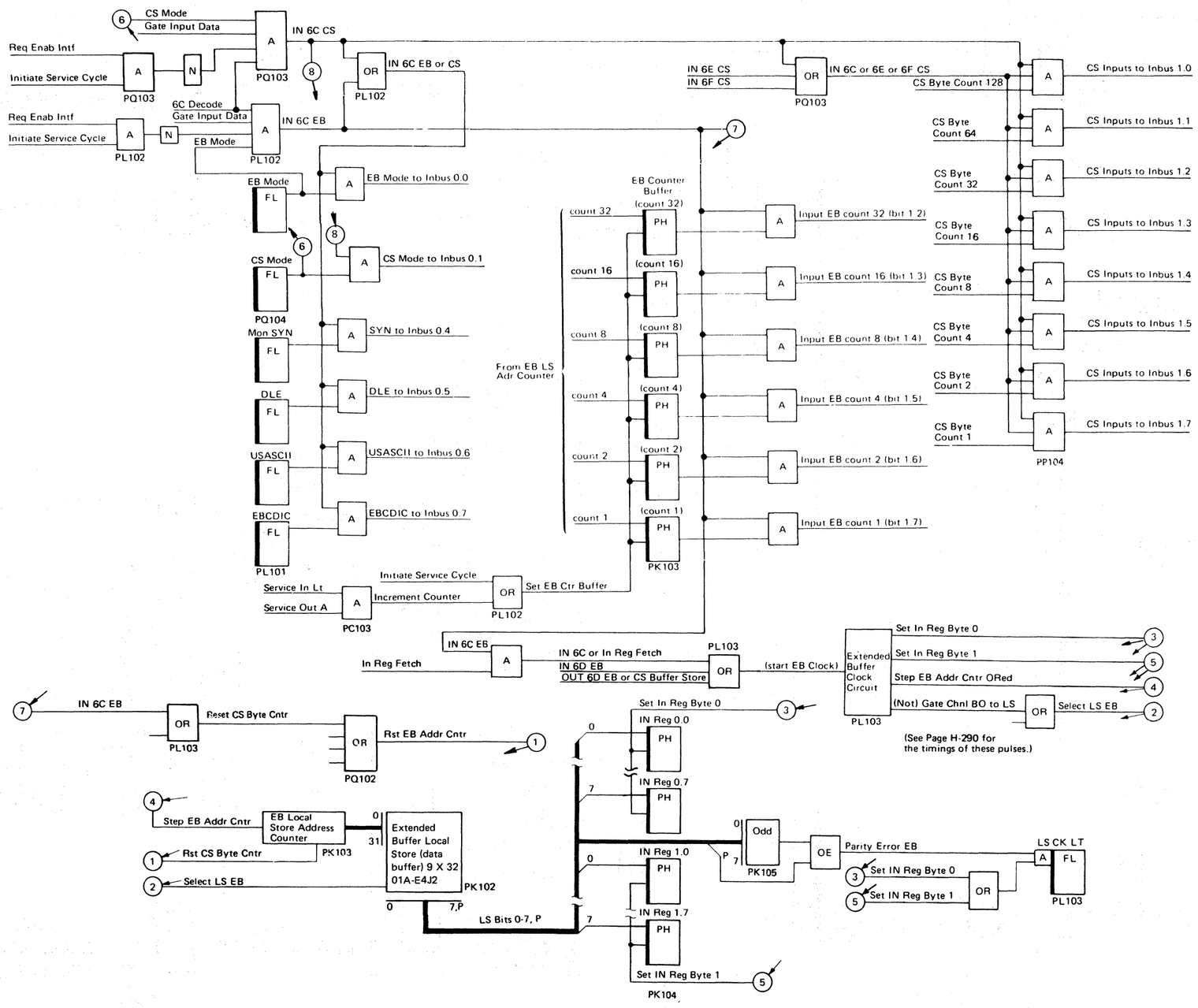
The Input X'6C' instruction transfers to a specified CCU general register the states of the 'extended buffer mode' latch, 'cycle steal mode' latch, 'character-monitor control' latches, 'DLE remember' latch, and the byte count of the data transferred in extended byte or cycle steal mode.

The Input X'6C' instruction resets the EB/CS local store address counter to address 0, then loads In register byte 0 with data byte 0 from EB/CS local store address 0. The 'step EB address counter' pulse advances the EB/CS local store address counter to 1 and then loads In register byte 1 with data byte 1 from that address. The EB/CS local store address counter then advances to address 2 so that the first Input X'6D' can continue loading the In register from sequential addresses. The data is buffered in the In register until the next Input X'6D' transfers it to a specified CCU general register.

Each byte of data from the EB/CS local store is parity checked and a parity error forces a level 1 interrupt.

Summary of CCU Inbus bits during Input X'6C'

Bit	Card Loc	ALD Page	Function	
0.0	E4H2	PL102	Extended Buffer Mode	
0.1	E4E2	PQ104	Cycle Steal Mode	
0.2			0	
0.3			0	
0.4	E4H2	PL105	SYN monitor control latch	
0.5	E4H2	PL101	DLE remember latch	
0.6	E4H2	PL101	USASCII monitor control latch	
0.7	E4H2	PL101	EBCDIC monitor control latch	
1.0			0	
1.1			0	
1.2	E4J2	PK103	Transferred byte count-bit 32	EB Mode
1.3	E4J2	PK103	Transferred byte count-bit 16	EB Mode
1.4	E4J2	PK103	Transferred byte count-bit 8	EB Mode
1.5	E4J2	PK103	Transferred byte count-bit 4	EB Mode
1.6	E4J2	PK103	Transferred byte count-bit 2	EB Mode
1.7	E4J2	PK103	Transferred byte count-bit 1	EB Mode
1.0	E4D2	PP104	Transferred byte count-bit 128	CS Mode (All zeros = 256)
1.1	E4D2	PP104	Transferred byte count-bit 64	CS Mode (All zeros = 256)
1.2	E4D2	PP104	Transferred byte count-bit 32	CS Mode (All zeros = 256)
1.3	E4D2	PP104	Transferred byte count-bit 16	CS Mode (All zeros = 256)
1.4	E4D2	PP104	Transferred byte count-bit 8	CS Mode (All zeros = 256)
1.5	E4D2	PP104	Transferred byte count-bit 4	CS Mode (All zeros = 256)
1.6	E4D2	PP104	Transferred byte count-bit 2	CS Mode (All zeros = 256)
1.7	E4D2	PP104	Transferred byte count-bit 1	CS Mode (All zeros = 256)



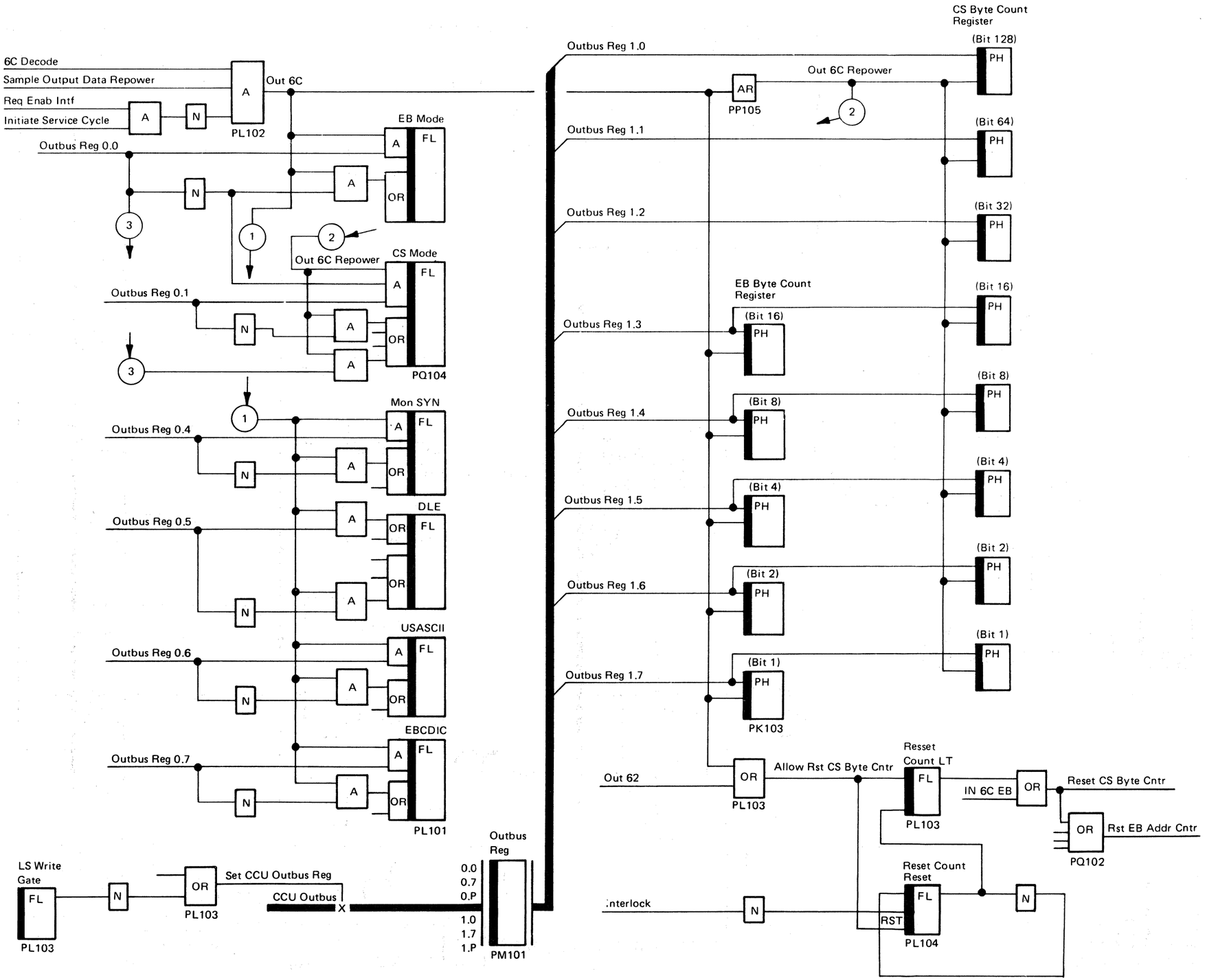
Output X'6C' Instruction

(Type 4 CA Extended Buffer/Cycle Steal Mode Control Register)

The Output X'6C' instruction sets or resets the 'EB mode' latch, the 'CS mode' latch, and various character-monitor or remember control latches. When outbus bit 0.0 is a one, the CA4 sets the 'EB mode' latch, inhibits any set of the 'CS mode' latch, and resets the 'CS mode' latch if it was on. This instruction also sets the EB and CS byte count registers with the number of bytes to be transferred during a data transfer and resets the EB local store address counter and CS byte counter to 0.

Summary of CCU Outbus bits during Output X'6C'

Bit	Card Loc	ALD Page	Function	
0.0	E4H2	PL102	1 = Set, 0 = Reset-extended buffer mode	
0.1	E4E2	PQ104	1 = Set, 0 = Reset-cycle steal mode	
0.2			0	
0.3			0	
0.4	E4H2	PL105	1 = Set, 0 = Reset SYN monitor control latch	
0.5	E4H2	PL101	1 = Set, 0 = Reset DLE remember latch	
0.6	E4H2	PL101	1 = Set, 0 = Reset USASCII monitor control latch	
0.7	E4H2	PL101	1 = Set, 0 = Reset EBCDIC monitor control latch	
1.0			0	
1.1			0	
1.2			0	
1.3	E4J2	PK103	Requested byte count-bit 16	EB Mode
1.4	E4J2	PK103	Requested byte count-biy 8	
1.5	E4J2	PK103	Requested byte count-bit 4	
1.6	E4J2	PK103	Requested byte count-bit 2	
1.7	E4J2	PK103	Requested byte count-bit 1	
1.0	E4D2	PP102	Requested byte count-bit 128	CS Mode
1.1	E4D2	PP102	Requested byte count-bit 64	
1.2	E4D2	PP102	Requested byte count-bit 32	
1.3	E4D2	PP102	Requested byte count-bit 16	
1.4	E4D2	PP102	Requested byte count-bit 8	
1.5	E4D2	PP102	Requested byte count-bit 4	
1.6	E4D2	PP102	Requested byte count-bit 2	
1.7	E4D2	PP102	Requested byte count-bit 1	



Input X'6D' Instruction

(Type 4 CA Extended Buffer/Cycle Steal Mode Data Buffer Bytes)

The 3705-80 control program uses the Input X'6D' instruction to transfer data to a specified CCU general register from the In register and then to reload the In register with data from the EB/CS local store data buffer.

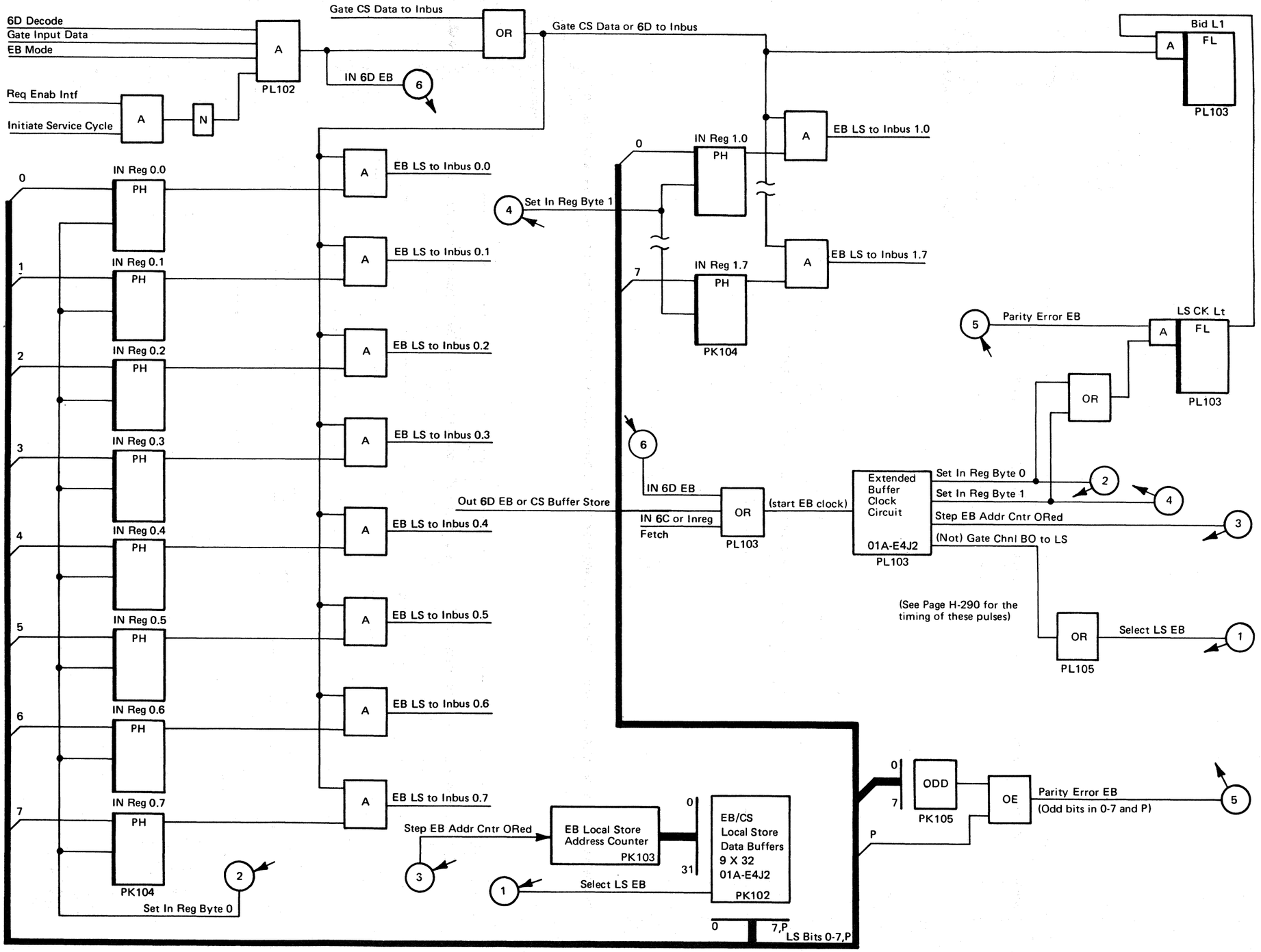
The Input X'6C' instruction loads the In register with two data bytes from EB/CS local store data buffer addresses 0 and 1. After a one cycle delay, the first Input X'6D' instruction transfers these to a specified CCU general register. The EB clock then loads In register byte 0 with data byte 0 from the next sequential EB/CS local store address. The EB clock increments the EB/CS local store address and then loads In register byte 1 with data byte 1 from the incremented address. The EB clock increments the address to the next sequential address. The In register buffers these two data bytes until the next Input X'6D' transfers them to the CCU. Sixteen Input X'6D' instructions are required to transfer the entire EB/CS local store data buffer. The 3705-80 control program must allow a delay of at least one cycle between successive Input X'6D' instructions to give the CA4 hardware enough time to load the In register (see H-290).

Each Input X'6D' loads the In register with two data bytes. If an inbound-data transfer sends an odd number of bytes, the last data character and the contents of the next EB/CS local store address will be loaded into the In register. The 3705-80 control program uses the transferred byte count to know that the last data byte was not part of this data transfer.

Each byte of data from the EB/CS local store is parity checked and a parity error forces a level 1 interrupt.

Summary of CCU Inbus bits during Input X'6D'

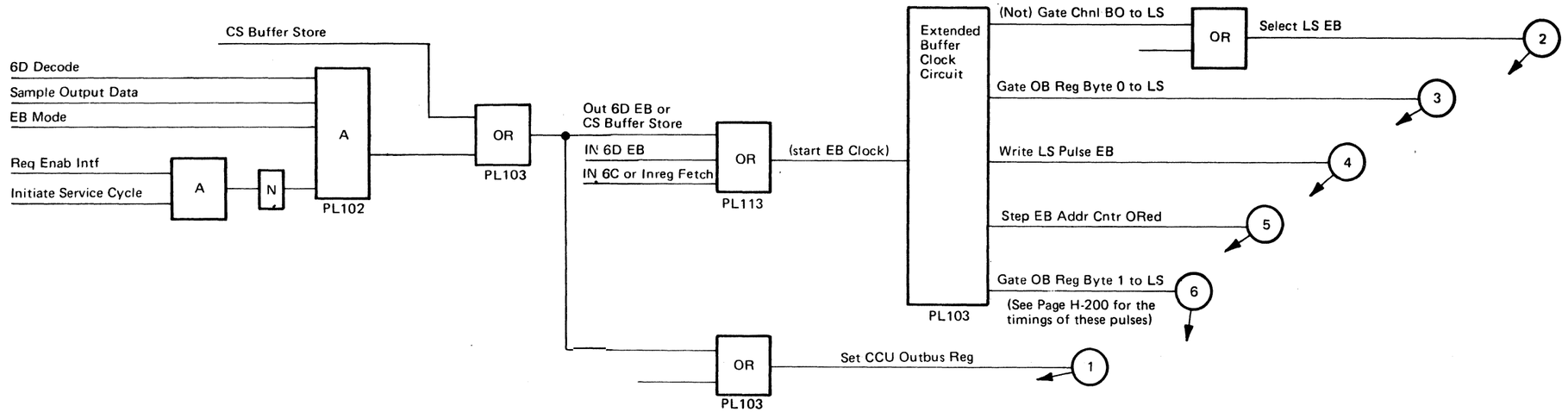
Bit	Card Loc	ALD Page	Function
0.0	E4J2	PK104	EB data buffer even byte-bit 0
0.1	E4J2	PK104	EB data buffer even byte-bit 1
0.2	E4J2	PK104	EB data buffer even byte-bit 2
0.3	E4J2	PK104	EB data buffer even byte-bit 3
0.4	E4J2	PK104	EB data buffer even byte-bit 4
0.5	E4J2	PK104	EB data buffer even byte-bit 5
0.6	E4J2	PK104	EB data buffer even byte-bit 6
0.7	E4J2	PK104	EB data buffer even byte-bit 7
1.0	E4J2	PK104	EB data buffer odd byte-bit 0
1.1	E4J2	PK104	EB data buffer odd byte-bit 1
1.2	E4J2	PK104	EB data buffer odd byte-bit 2
1.3	E4J2	PK104	EB data buffer odd byte-bit 3
1.4	E4J2	PK104	EB data buffer odd byte-bit 4
1.5	E4J2	PK104	EB data buffer odd byte-bit 5
1.6	E4J2	PK104	EB data buffer odd byte-bit 6
1.7	E4J2	PK104	EB data buffer odd byte-bit 7



Output X'6D' Instruction

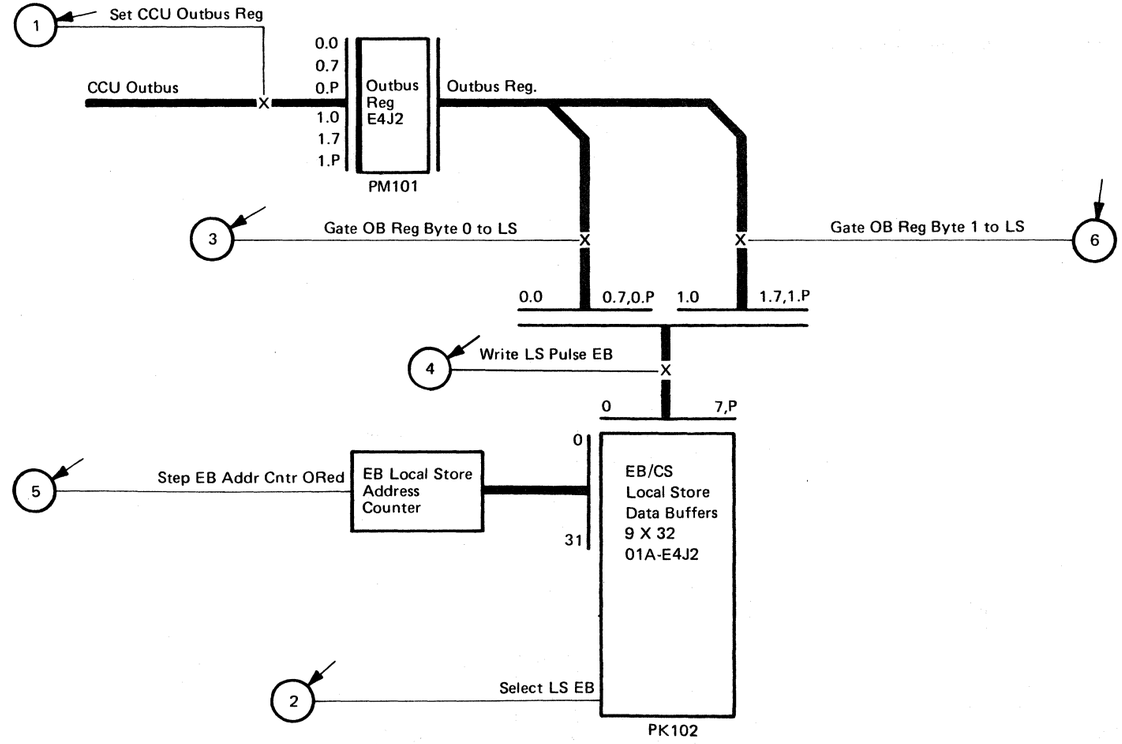
(Type 4 CA Extended Buffer/Cycle Steal Mode Data Buffer Bytes)
The control program uses the Output X'6D' instruction to load the EB/CS local store data buffers with data for an outbound data transfer.

The data is buffered in the outbus register until it can be written into the EB/CS local store data buffer. A previous Output X'6C' instruction had reset the EB/CS local store address counter to 0 so that the data may be loaded sequentially beginning with address 0. The EB clock generates the gating and write pulses to load data byte 0 into the EB/CS local store, increment the EB/CS local store address counter by 1, then load data byte 1. Each Output X'6D' instruction thus loads two data bytes in sequential addresses. Sixteen Output X'6D' instructions are required to fill the EB/CS local store. The 3705-80 control program must allow a delay of at least one cycle between successive Output X'6D' instructions to give the CA4 hardware enough time to load the EB/CS local store data buffers (see H-200).



Summary of CCU Outbus bits during Output X'6D'

Bit	Card LOC	ALD Page	Function
0.0	E4J2	PK102	EB data buffer even byte–bit 0
0.1	E4J2	PK102	EB data buffer even byte–bit 1
0.2	E4J2	PK102	EB data buffer even byte–bit 2
0.3	E4J2	PK102	EB data buffer even byte–bit 3
0.4	E4J2	PK102	EB data buffer even byte–bit 4
0.5	E4J2	PK102	EB data buffer even byte–bit 5
0.6	E4J2	PK102	EB data buffer even byte–bit 6
0.7	E4J2	PK102	EB data buffer even byte–bit 7
1.0	E4J2	PK102	EB data buffer odd byte–bit 0
1.1	E4J2	PK102	EB data buffer odd byte–bit 1
1.2	E4J2	PK102	EB data buffer odd byte–bit 2
1.3	E4J2	PK102	EB data buffer odd byte–bit 3
1.4	E4J2	PK102	EB data buffer odd byte–bit 4
1.5	E4J2	PK102	EB data buffer odd byte–bit 5
1.6	E4J2	PK102	EB data buffer odd byte–bit 6
1.7	E4J2	PK102	EB data buffer odd byte–bit 7



Input X'6E' and X'6F' Instructions

Input X'6E' (CS Error Register and CS Byte X)

The 3705-80 control program uses the Input X'6E' instruction to transfer the contents of the 'cycle steal error register' (see H-380) and the 'CSAR byte X register' to a specified CCU general register.

Summary of CCU Inbus bits during Input X'6E'

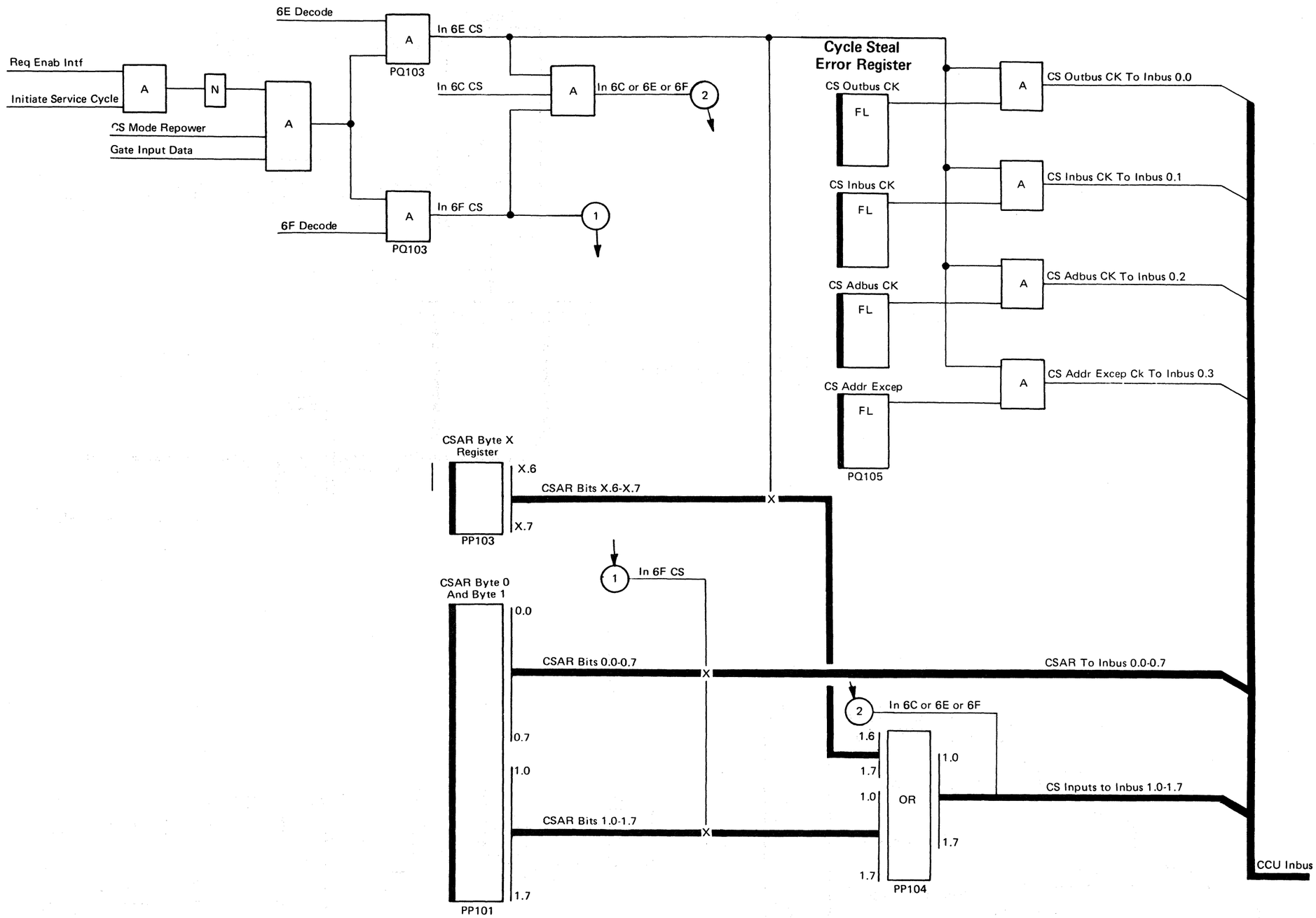
Bit	Card Loc	ALD Page	Function
0.0	E4E2	PQ105	Cycle Steal Outbus Error
0.1	E4E2	PQ105	Cycle Steal Inbus Error
0.2	E4E2	PQ105	Cycle Steal Adbus Error
0.3			0
0.4			0
0.5			0
0.6			0
0.7			0
1.0			0
1.1			0
1.2			0
1.3			0
1.4			0
1.5			0
1.6	E4D2	PP103	CSAR Bit X.6
1.7	E4D2	PP103	CSAR Bit X.7

Input X'6F' (CSAR Byte 0 and Byte 1)

The 3705-80 control program uses the Input X'6F' instruction to transfer the contents of CSAR byte 0 and 1 to a specified CCU general register.

Summary of CCU Inbus bits during Input X'6F'

Bit	Card Loc	ALD Page	Function
0.0	E4D2	PP104	CSAR Bit 0.0
0.1	E4D2	PP104	CSAR Bit 0.1
0.2	E4D2	PP104	CSAR Bit 0.2
0.3	E4D2	PP104	CSAR Bit 0.3
0.4	E4D2	PP104	CSAR Bit 0.4
0.5	E4D2	PP104	CSAR Bit 0.5
0.6	E4D2	PP104	CSAR Bit 0.6
0.7	E4D2	PP104	CSAR Bit 0.7
1.0	E4D2	PP104	CSAR Bit 1.0
1.1	E4D2	PP104	CSAR Bit 1.1
1.2	E4D2	PP104	CSAR Bit 1.2
1.3	E4D2	PP104	CSAR Bit 1.3
1.4	E4D2	PP104	CSAR Bit 1.4
1.5	E4D2	PP104	CSAR Bit 1.5
1.6	E4D2	PP104	CSAR Bit 1.6
1.7	E4D2	PP104	CSAR Bit 1.7



Output X'6E' and X'6F' Instructions

Output X'6E' (CSAR Byte X)
The 3705-80 control program uses the Output X'6E' instruction to set the extended address bits in the CSAR byte X register. Output X'6F' must first be executed to set CSAR bytes 0 and 1 since it also resets CSAR byte X. Output X'6E' is then executed if the storage address is above 64 K (CSAR bits X.6 or X.7=1).

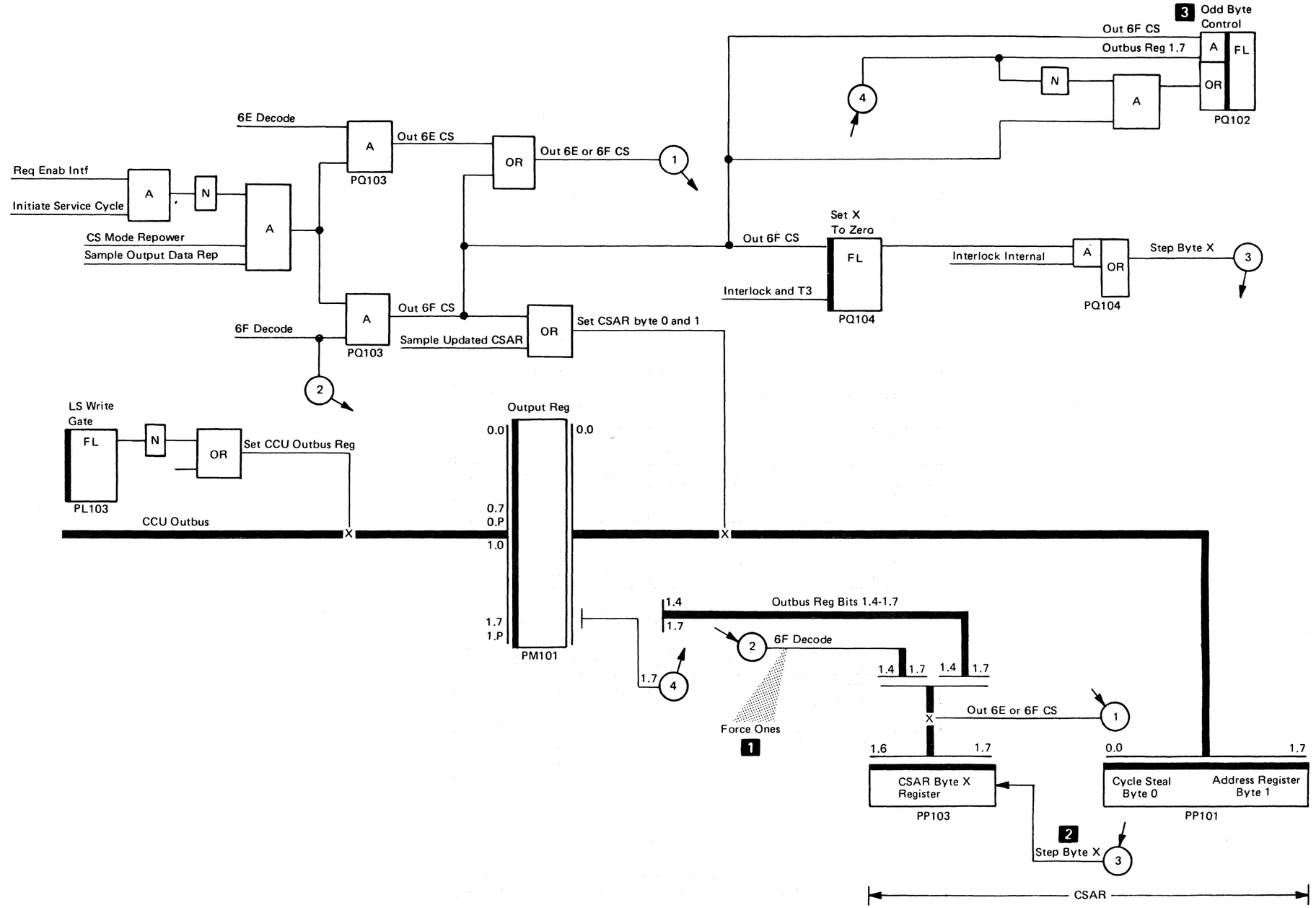
Summary of CCU Outbus bits during Output X'6E'

Bit	Card Loc	ALD Page	Function
0.0			0
0.1			0
0.2			0
0.3			0
0.4			0
0.5			0
0.6			0
0.7			0
1.0			0
1.1			0
1.2			0
1.3			0
1.4			0
1.5			0
1.6	E4D2	PP103	CSAR Bit X.6
1.7	E4D2	PP103	CSAR Bit X.7

Output X'6F' (CSAR Byte 0 and Byte 1)
The 3705-80 control program uses the Output X'6F' instruction to set the storage address (for the first data buffer byte involved in a cycle-steal data transfer) in CSAR bytes 0 and 1. Output X'6F' resets CSAR byte X by (1) forcing ones into CSAR bits X.6-X.7 **1** and (2) stepping CSAR byte X from X'F' to X'0' **2** . Resetting CSAR byte X enables the control program to set up CSAR using only Output X'6F' if the storage address is not above 64 K. Output X'6F' also sets/resets the 'odd byte control' latch **3** depending upon the state of outbus reg bit 1.7 (CSAR bit 1.7).

Summary of CCU Outbus bits during Output X'6F'

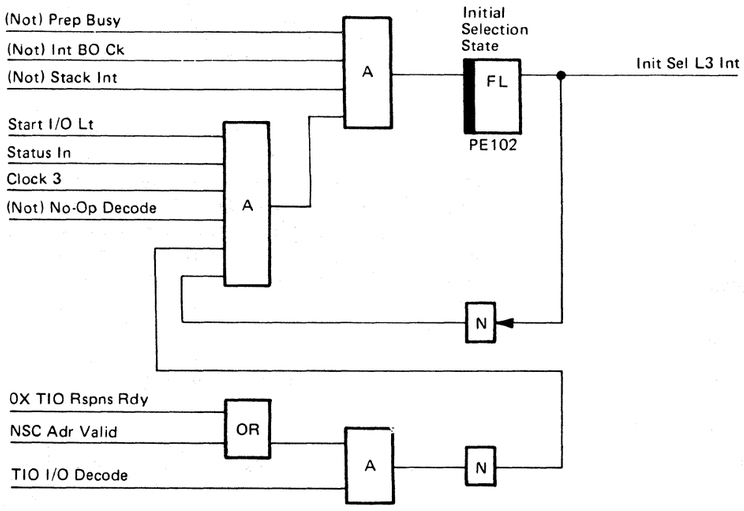
Bit	Card Loc	ALD Page	Function
0.0	E4D2	PP101	CSAR Bit 0.0
0.1	E4D2	PP101	CSAR Bit 0.1
0.2	E4D2	PP101	CSAR Bit 0.2
0.3	E4D2	PP101	CSAR Bit 0.3
0.4	E4D2	PP101	CSAR Bit 0.4
0.5	E4D2	PP101	CSAR Bit 0.5
0.6	E4D2	PP101	CSAR Bit 0.6
0.7	E4D2	PP101	CSAR Bit 0.7
1.0	E4D2	PP101	CSAR Bit 1.0
1.1	E4D2	PP101	CSAR Bit 1.1
1.2	E4D2	PP101	CSAR Bit 1.2
1.3	E4D2	PP101	CSAR Bit 1.3
1.4	E4D2	PP101	CSAR Bit 1.4
1.5	E4D2	PP101	CSAR Bit 1.5
1.6	E4D2	PP101	CSAR Bit 1.6
1.7	E4D2	PP101	CSAR Bit 1.7



OUTBOUND DATA TRANSFERS–EB MODE (PART 1 OF 6)

Outbound data transfers result from channel Read commands that direct the transfer of data from 3705-80 storage to the host processor. When the CA4 is in EB mode, the 3705-80 control program must execute an Output X'6D' for each two data bytes that are to be transferred to the channel whether the CA4 is in ESC or NSC mode.

CA Decodes the Command and Requests an Interrupt



The 3705-80 control program responds to the initial select level 3 interrupt with the following instructions:

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	1000 10X0	1.0 = type 4 CA level 3 interrupt 1.4 = selected type 4 CA initial selection level 3 interrupt 1.6 = 0 type 4 CA #1 selected = 1 type 4 CA #2 selected
Input X'61'	address	command	Byte 0 = address Byte 1 = command
Input X'60'	1000 0000	0000 0000	Normal initial selection (Note 1)
At this point the control program queues the control block for this line on the priority data-service-out queue. After all control blocks ahead of this one are serviced, the following sequence is performed.			
Output X'63'	address	xxxx xxxx	Byte 0 = transfer address Byte 1 = all zeros
Output X'6C'	1000 0000	1000 0111	0.0 = set extended buffer mode 1.3-1.7 = 0111 to transfer seven data bytes out (Note 2) Resets EB adr counter to adr 00
Output X'6D'	data	data	Byte 0 = data for EB LS adr 00 Byte 1 = data for EB LS adr 01
Minimum of one cycle delay between successive Output X'6D's			
Output X'6D'	data	data	Byte 0 = data for EB LS adr 02 Byte 1 = data for EB LS adr 03
Minimum of one cycle delay between successive Output X'6D's			
Output X'6D'	data	data	Byte 0 = data for EB LS adr 04 Byte 1 = data for EB LS adr 05
Minimum of one cycle delay between successive Output X'6D's			
Output X'6D'	data	xxxx xxxx No data	Byte 0 = data for EB LS adr 06 Byte 1 = Contents are loaded into EB LS adr 07
Minimum of one cycle delay between Output X'6D' and Output X'62'			
Output X'62'	1000 0010	0000 0100	0.0 = outbound data transfer 0.6 = reset data/status interrupt 1.5 = set priority outbound-data transfer sequence EB
Output X'67'	0000 0000	0100 0000	1.1 = set program interrupt (to block initial select interrupts)

Loads seven data bytes into the EB local store (data buffer) starting at address 00 plus the "no data" contents of general register byte 1 into address 07. See H-200 for a sequence chart for this operation.

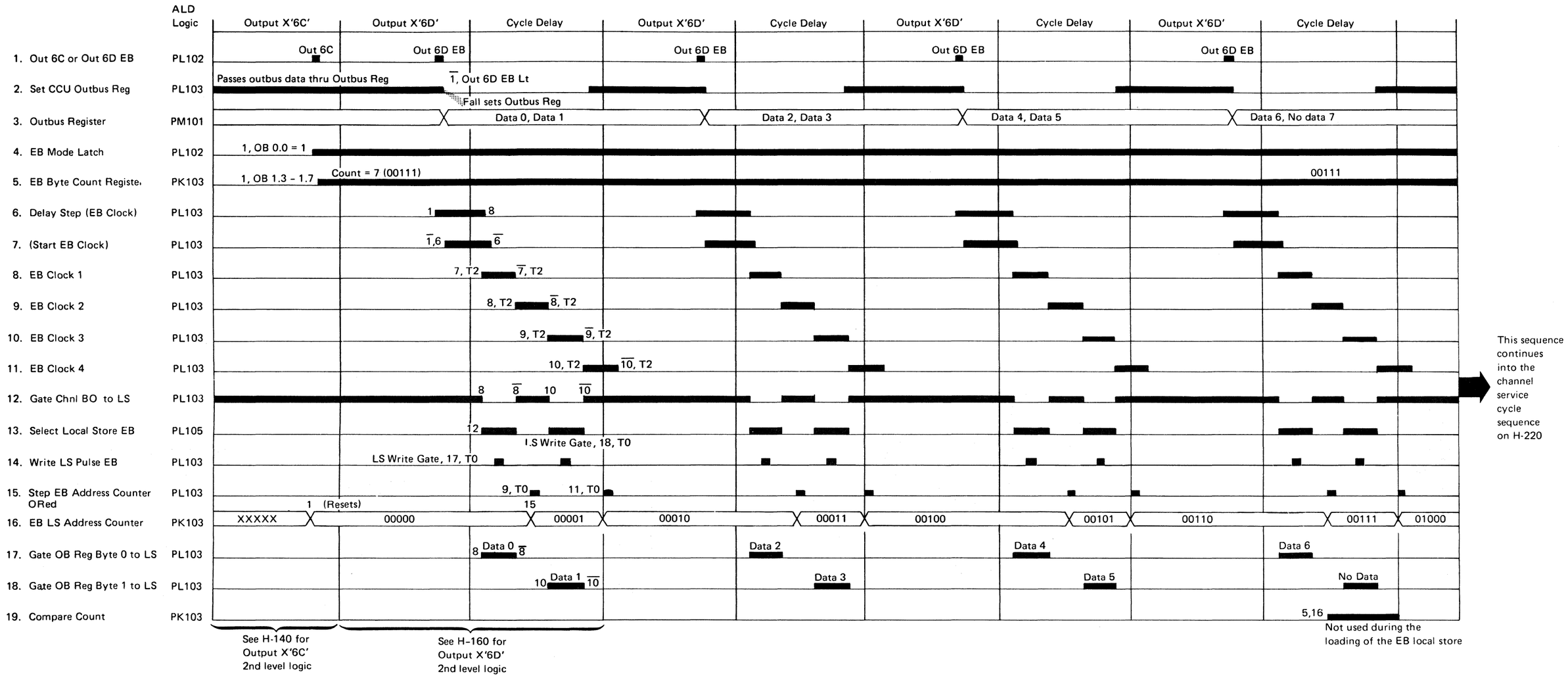
Outbound transfer initiates a channel data service cycle. See H-220 for a sequence chart for this operation and the channel service cycle.

Notes:

1. *Other bits may be transferred to the CCU during this input. If other bits are on, the 3705-80 control program must take action differently from the normal initial selection.*
2. *From one to thirty-two bytes of data may be transferred to the channel. The number of Output X'6D's depends on the number of bytes of data to be transferred.*

OUTBOUND DATA TRANSFERS—EB MODE (PART 2 OF 6)

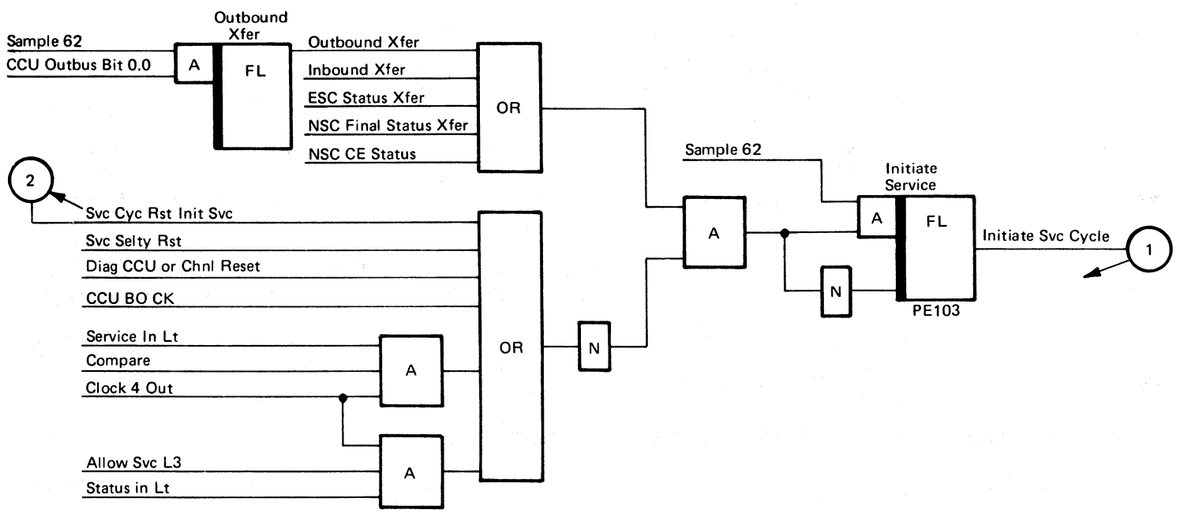
Sequence Chart for Loading the EB Local Store (Data Buffer)



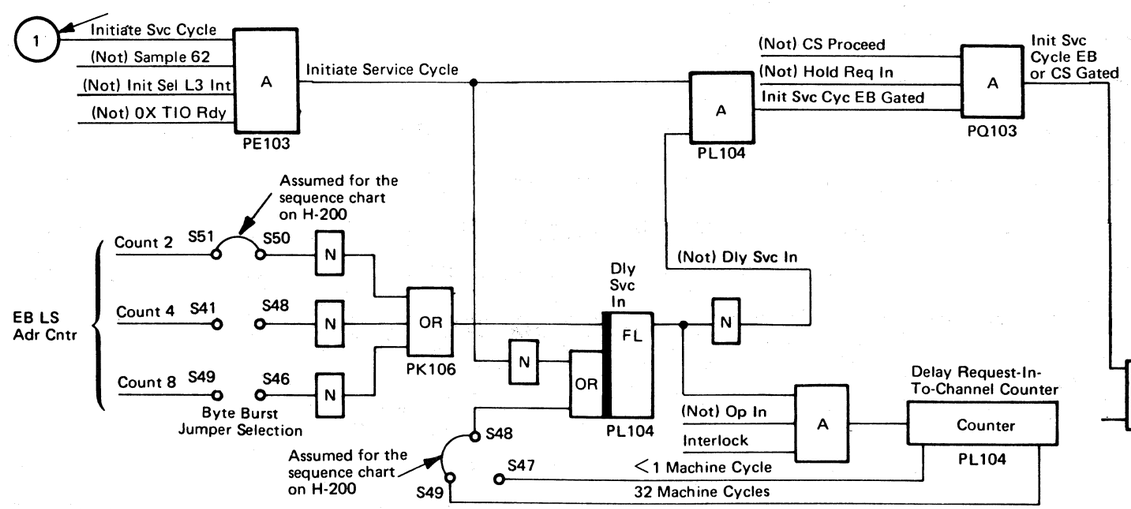
OUTBOUND DATA TRANSFERS—EB MODE
(PART 3 OF 6)

CA to Channel Data Transfer—See H-220 for Sequence Chart

The Output X'62' instruction starts a channel service cycle so that the data loaded into the EB/CS local store can be transferred to the channel.

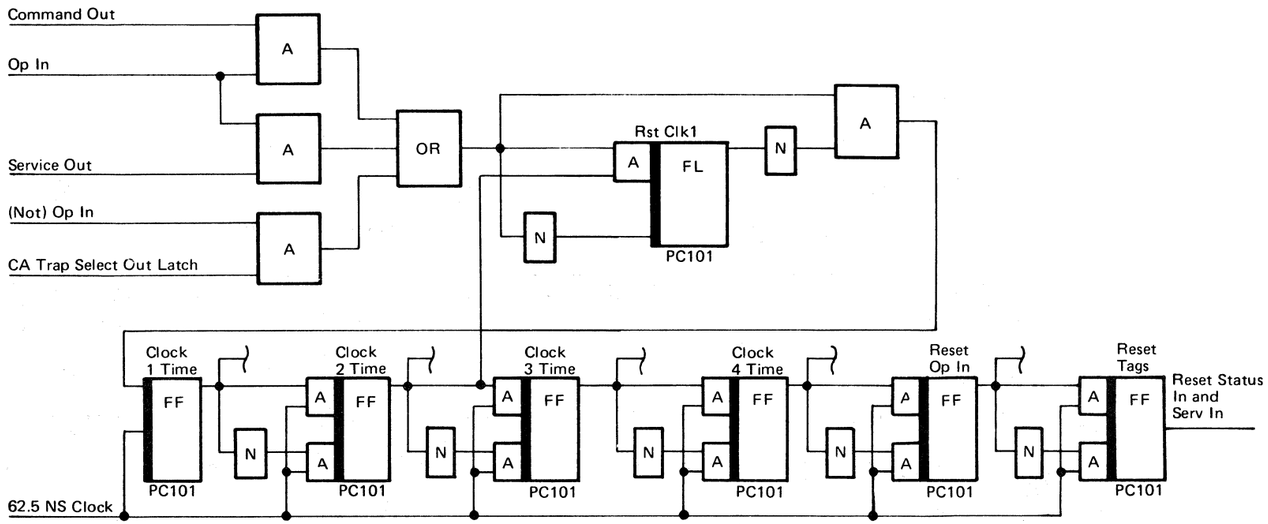


The CA4 sends Request In to the channel to start the service cycle.

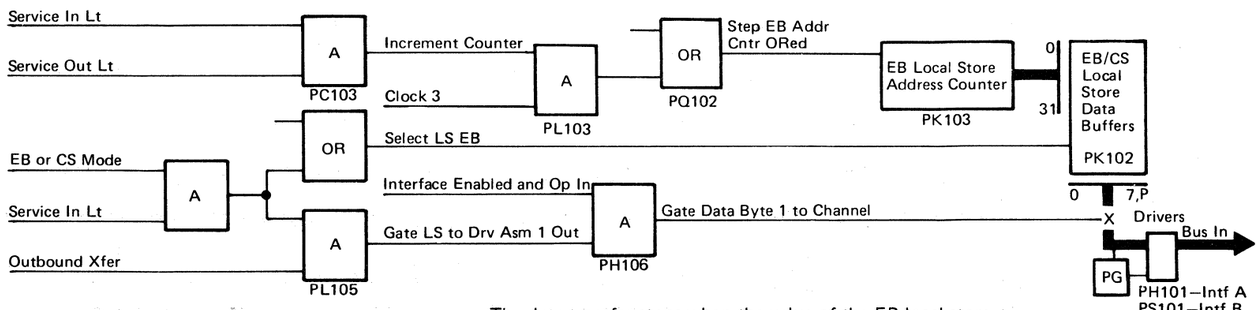


The type 4 CA provides the capability of transferring 4, 8, 16, or 32 byte bursts of data—the selection made by a CE-installed jumper. The EB address counter steps as each data byte transfers to the channel. 'Count 2' falls after four data bytes have been transferred ('count 4' after eight, 'count 8' after sixteen) to set the 'delay service in' latch. This latch is not set for a thirty-two byte burst. Op In resets to drop the CA off the channel and a delay counter starts. A CE-installed jumper selects how much delay occurs before the CA raises Request In to continue transferring data to the EB channel.

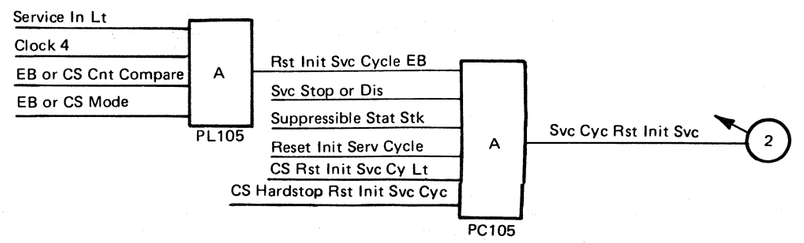
The channel tag clock operates each time the channel and the CA start a data transfer. The clock synchronizes the CA and the channel to handle the data transfer.

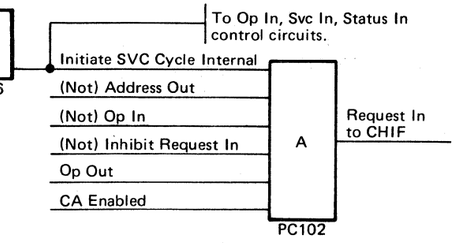


Service In causes the next data byte to be read out of the EB/CS LS data buffer to the channel and then increments the EB address counter.



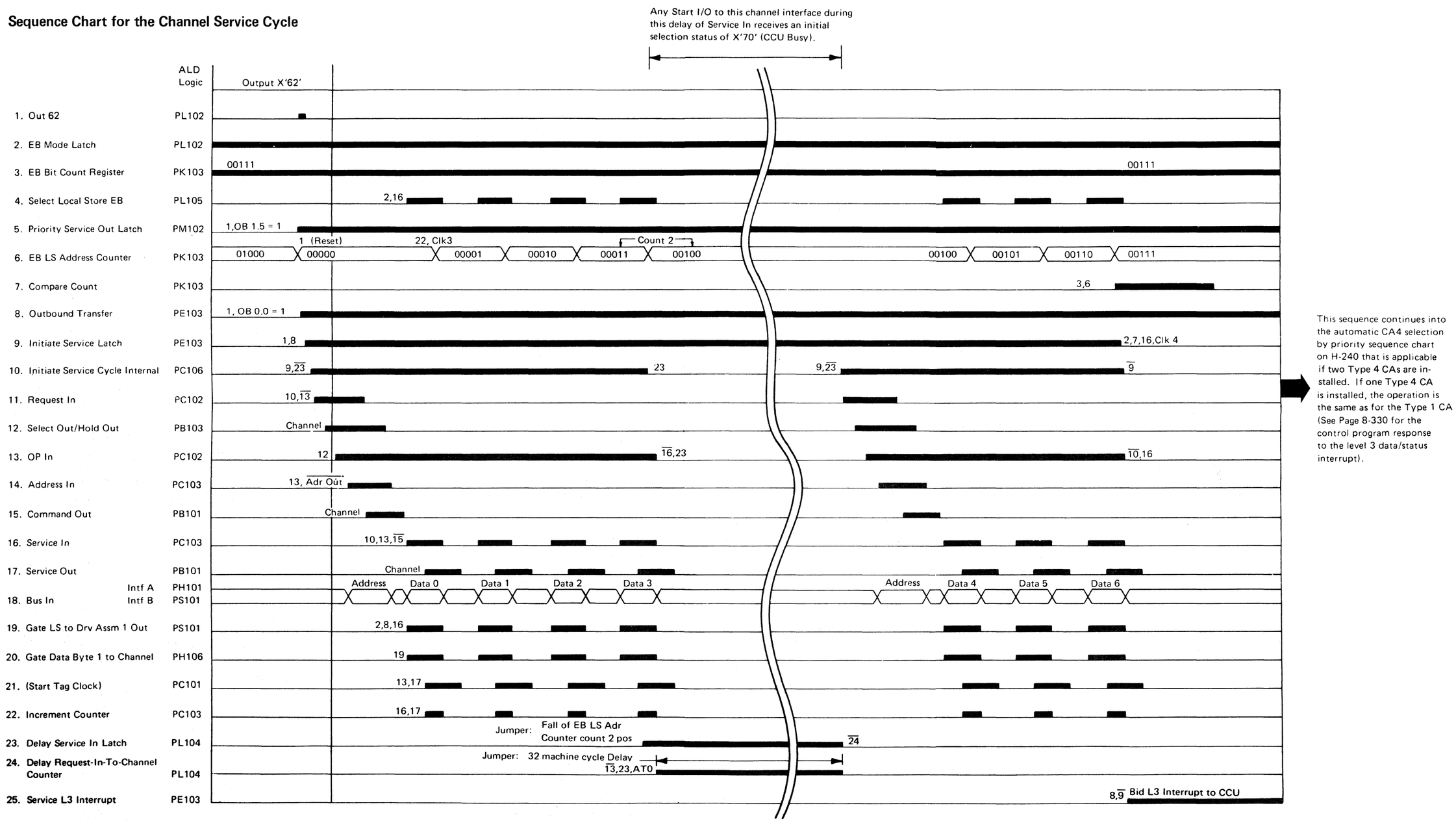
The data transfer stops when the value of the EB local store address counter equals the byte count to be transferred in the EB count register.





OUTBOUND DATA TRANSFERS–EB MODE (PART 4 OF 6)

Sequence Chart for the Channel Service Cycle



This sequence continues into the automatic CA4 selection by priority sequence chart on H-240 that is applicable if two Type 4 CAs are installed. If one Type 4 CA is installed, the operation is the same as for the Type 1 CA (See Page 8-330 for the control program response to the level 3 data/status interrupt).

OUTBOUND DATA TRANSFERS—EB MODE (PART 5 OF 6)

Automatic CA4 Selection by Priority—Two Type 4 CAs

When two type 4 CAs are installed, the automatic-selection circuit automatically selects the CA4 with the highest priority interrupt request. The control program must execute an Output X'67' with all zeros in the specified general register to set the 'prime priority select' latch **1** . When the next Input X'77' is executed, the highest priority CA is selected **2** . If the priorities were equal, the automatic-selection circuit selects the first CA4 with an equal priority that receives the 'selected from previous CA' signal **3** .

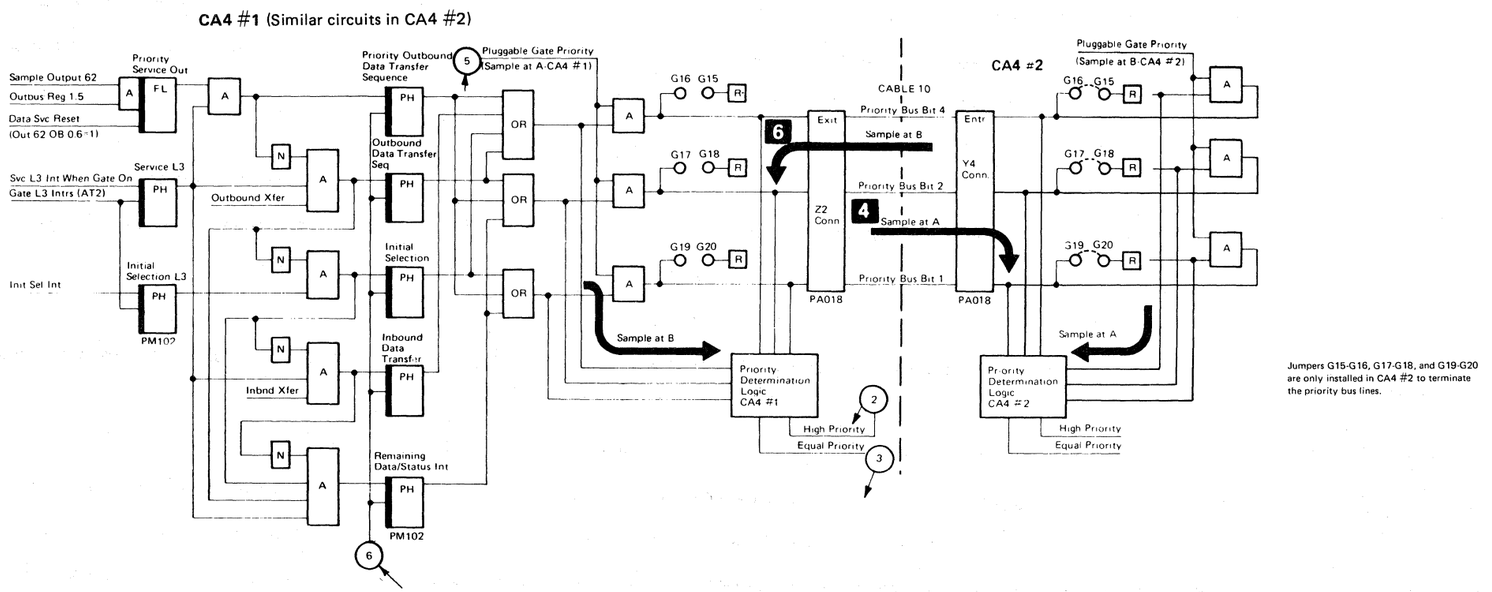
The control program can assign a higher level priority to an Outbound Data Transfer Sequence by setting bit 1.5 to 1 when executing Output X'62' to set the Outbound Sequence.

The automatic-selection circuit assigns priority bits to all L3 interrupts according to this table:

L3 Interrupt	Priority 4	Bus 2	Bits 1
Priority Outbound Data Transfer Seq.	1	1	1
Outbound Data Transfer Seq.	1	1	0
Initial Selection Interrupt	1	0	1
Inbound Data Transfer Seq.	1	0	0
Remaining Data Status Interrupts	0	1	1

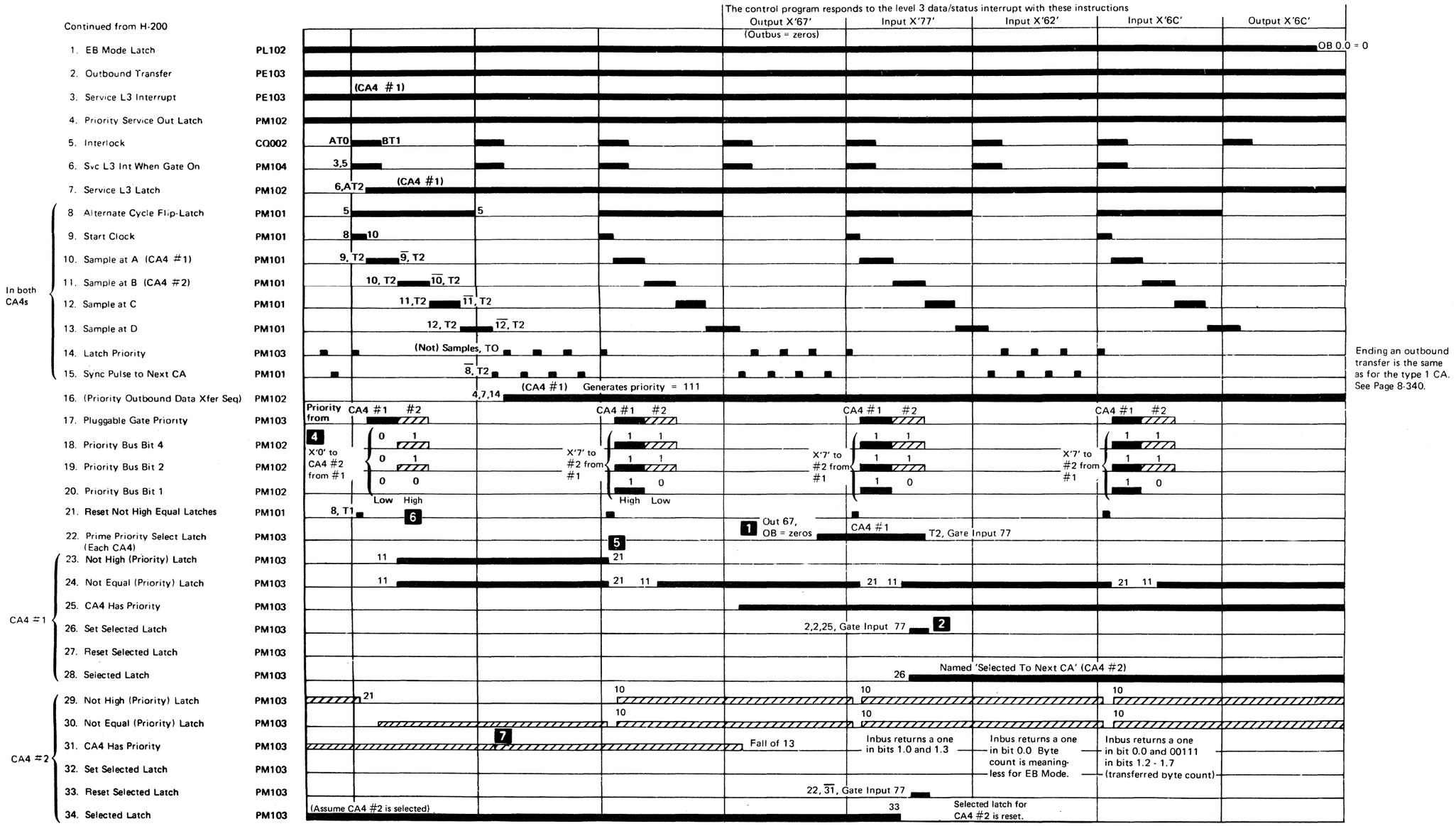
At 'sample at A' time, CA4 #1 sends its L3 interrupt state to CA4 #2 via the priority bus **4** . CA4 #2 compares its priority with the CA4 #1 priority and sets its appropriate 'not high' and/or 'not equal' priority latches. Once set, these latches remain on until reset by the 'reset not high equal latches' pulse **5** . At 'sample at B' time, CA4 #2 sends its L3 interrupt state to CA4 #1 **6** . CA4 #1 compares its priority with the CA4 #2 priority and sets its appropriate 'not high' and/or 'not equal' priority latches. Some of these 'not high' and/or 'not equal' priority latches may have been set at 'sample at A' time.

At the fall of 'sample at D' time, each CA4 interrogates the states of its 'not high' and 'not equal' priority latches as well as the state of the 'selected from previous CA' line to determine whether to set its 'CA4 has priority' latch **7** . This sampling occurs continuously but the select latches are set or reset by this circuit only by the next Input X'77' instruction.



OUTBOUND DATA TRANSFERS—EB MODE (PART 6 OF 6)

Sequence Chart for the Automatic CA4 Selection by Priority—Two Type 4 CAs



Ending an outbound transfer is the same as for the type 1 CA. See Page 8-340.

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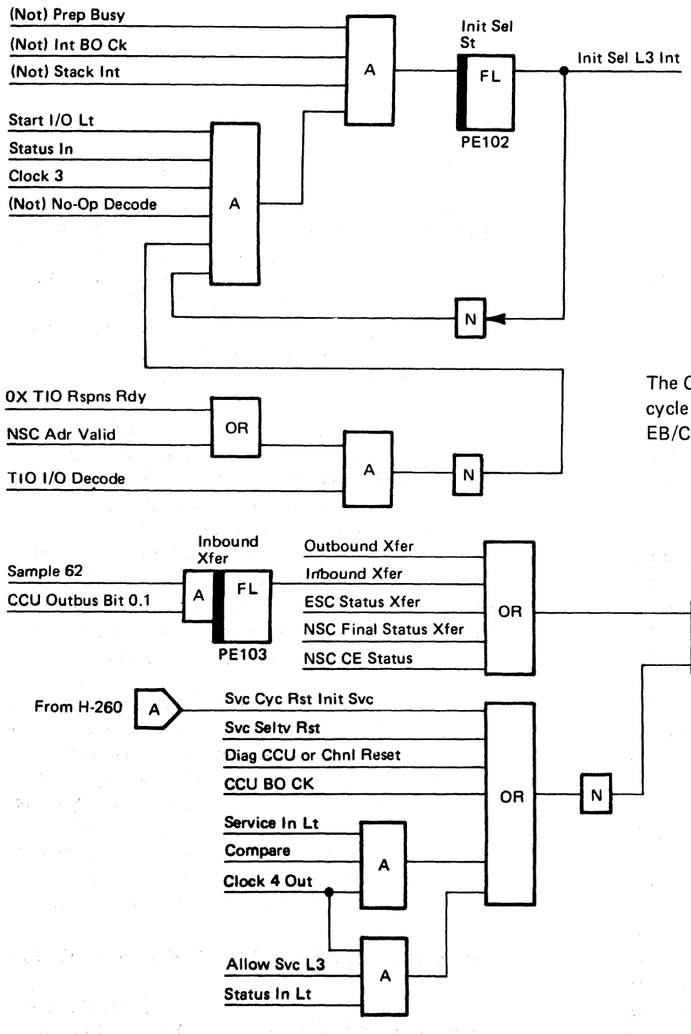
INBOUND DATA TRANSFERS—EB MODE (PART 1 OF 5)

Inbound data transfers result from commands that require the passing of data from the host processor to 3705-80 storage.

When the commands are decoded, they request an initial selection level 3 interrupt so that the 3705-80 control program can determine what action to take to service the command. The commands start an initial selection sequence as shown on 8-170.

CA Requests an Initial Selection Level 3 Interrupt



The Output X'62' instruction initiates a channel service cycle to transfer the data from the host processor to the CA EB/CS local store.

Control Program Responds to the Interrupt

The 3705-80 control program responds to the initial selection level 3 interrupt with the following sequence of instructions.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	1000 10x0	1.0 = type 4 CA level 3 interrupt 1.4 = selected type 4 CA initial selection level 3 interrupt 1.6 = 0 type 4 CA #1 selected = 1 type 4 CA #2 selected
Input X'60'	1000 0000	0000 0000	0.0 = Normal initial selection (Note)
Input X'61'	Address	Command	Byte 0 = subchannel address Byte 1 = command
Output X'60'	xxxx xxxx	xxxx xxxx	Resets initial selection level 3 interrupt.
At this point the control program queues the control block for this line on the data-service-in queue. After all the control blocks ahead of this one, on the queue, are serviced the following sequence is performed.			
Output X'63'	Address	xxxx xxxx	Byte 0 = address Byte 1 = all zeros
Output X'6C'	1000 1001	0000 1000	0.0 = set extended buffer mode 0.4 = set SYN monitor control latch 0.7 = set EBCDIC monitor control latch 1.3-1.7 = 1000 to transfer eight data bytes Resets EB adr counter to adr 00
Output X'62'	0100 0010	0000 0000	0.1 = inbound data transfer 0.6 = reset data/status control 1.6-1.7 = request byte count limit for consecutive SYNs. 01 = 1; 10 = 2; 11 = 3; 00 = 4.

See H-270 for a sequence chart for this operation and the channel service cycle.

Note: *If other bits are on during this input, the 3705 control program must take appropriate action to service the condition indicated by the bit.*

The type 4 CA provides the capability of transferring 4, 8, 16, or 32 byte bursts of data—the selection made by a CE-installed jumper. The EB address counter steps as each data byte transfers to the EB local store. 'Count 2' falls after four data bytes have been transferred ('count 4' after eight, 'count 8' after sixteen) to set the 'delay service in' latch. This latch is not set for a thirty-two byte burst. Op In resets to drop the CA off the channel and a delay counter starts. A CE-installed jumper selects how much delay occurs before the CA raises Request In to continue transferring data to the EB local store.

INBOUND DATA TRANSFERS–EB/CS MODE (PART 2 OF 5)

BSC Control Character Recognition in ESC Mode

ETB and ETX (EBCDIC or USASCII)

The type 4 CA, when in EB/CS mode and the ESC (emulator sub-channel) mode is enabled, recognizes BSC control characters ETB and ETX and sets the 'svc stop or disc' latch **1** . This resets the 'initiate service cycle' latch and causes a CA4 data/status L3 interrupt. An Input X'62', executed when the level 3 interrupt is serviced, transfers bit 0.5 (service stop) to a specified CCU general register for 3705-80 control program use.

DLE-STX (EBCDIC or USASCII)

The type 4 CA, when in EB/CS mode and the ESC mode is enabled, recognizes the DLE-STX control-character sequence (indicating the start of transparent data) and resets the EBCDIC, USASCII, and DLE monitor latches **2** to prevent monitoring the transparent data. An Input X'6C', executed when the level 3 interrupt is serviced, transfers zeros for USASCII and EBCDIC monitor control bits 0.6 and 0.7 to a specified CCU general register for 3705-80 control program use.

If the DLE control character is the last character of one inbound-data transfer sequence, bit 0.5 ('DLE remember' latch) will be on in a specified CCU general register after the Input X'6C' instruction is performed. The 3705-80 control program must set the 'DLE remember' latch (bit 0.5=1) when the Output X'6C' instruction is executed for the next inbound-data transfer sequence for the subject address. If an STX control character is the first character of the next inbound-data transfer sequence, the EBCDIC, USASCII, and DLE monitor latches are reset to prevent monitoring the transparent data for ending characters.

SYN (EBCDIC or USASCII)

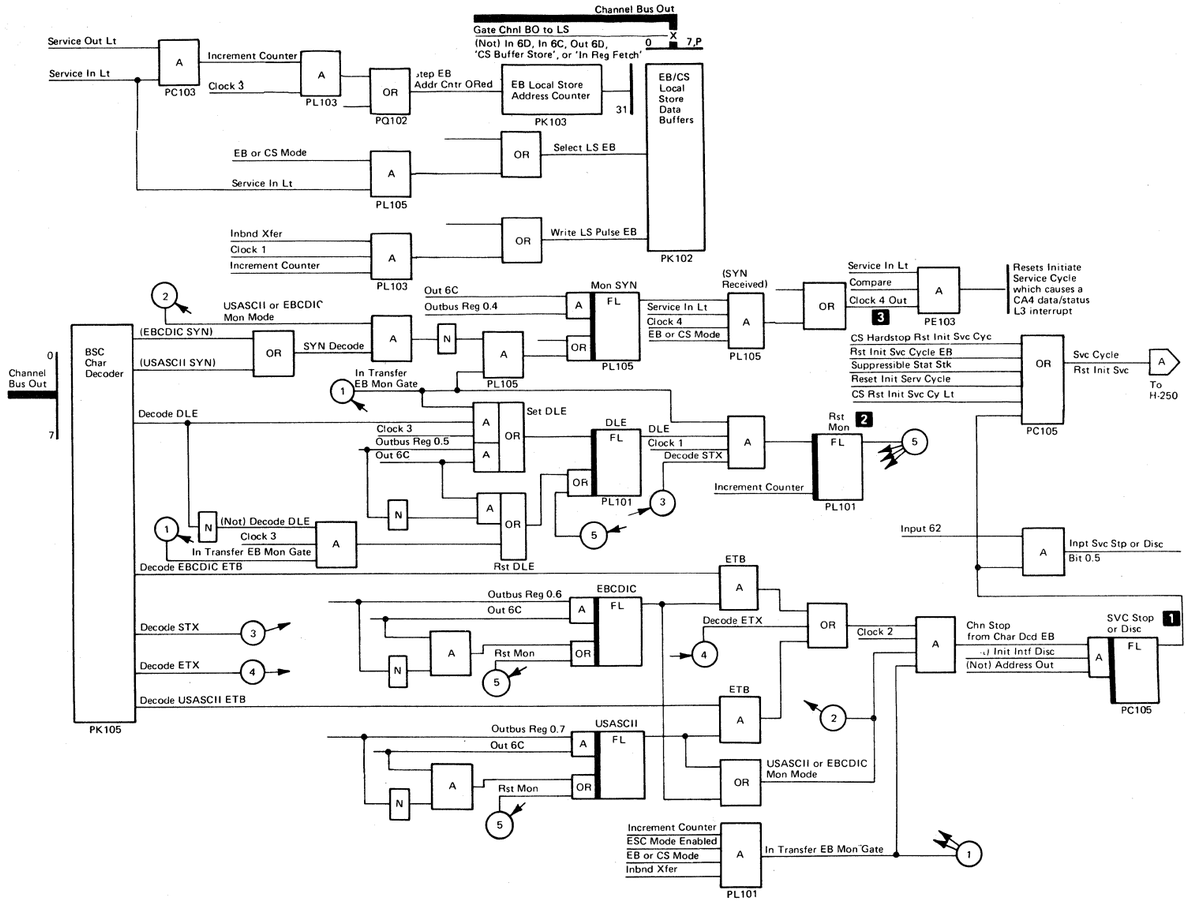
Some programs use SYN characters as time fill characters. The type 4 CA recognizes these consecutive SYN characters as "fill" characters and frees the channel to service other devices.

The type 4 CA, when in EB/CS mode and the ESC mode is enabled, monitors for SYN characters if the 'monitor SYN' latch is on. The Output X'62' that requested the inbound-data transfer sequence also sets the non-EB/CS byte-transfer count with the number of consecutive SYN characters that are to be received before the CA4 disconnects from the channel. When the number of consecutive SYN characters received from the channel equals the number in the non-EB/CS byte-transfer count, the CA4 resets the 'initiate service cycle' latch and causes a CA4 Data/status L3 interrupt **3** . An Input X'6C', executed when the level 3 interrupt is serviced, transfers bit 0.4 ('SYN monitor control' latch) to a specified CCU general register for 3705-80 control program use.

A non-SYN character resets the 'monitor SYN' latch and monitoring of SYN characters ceases and normal controls for terminating the sequence take over.

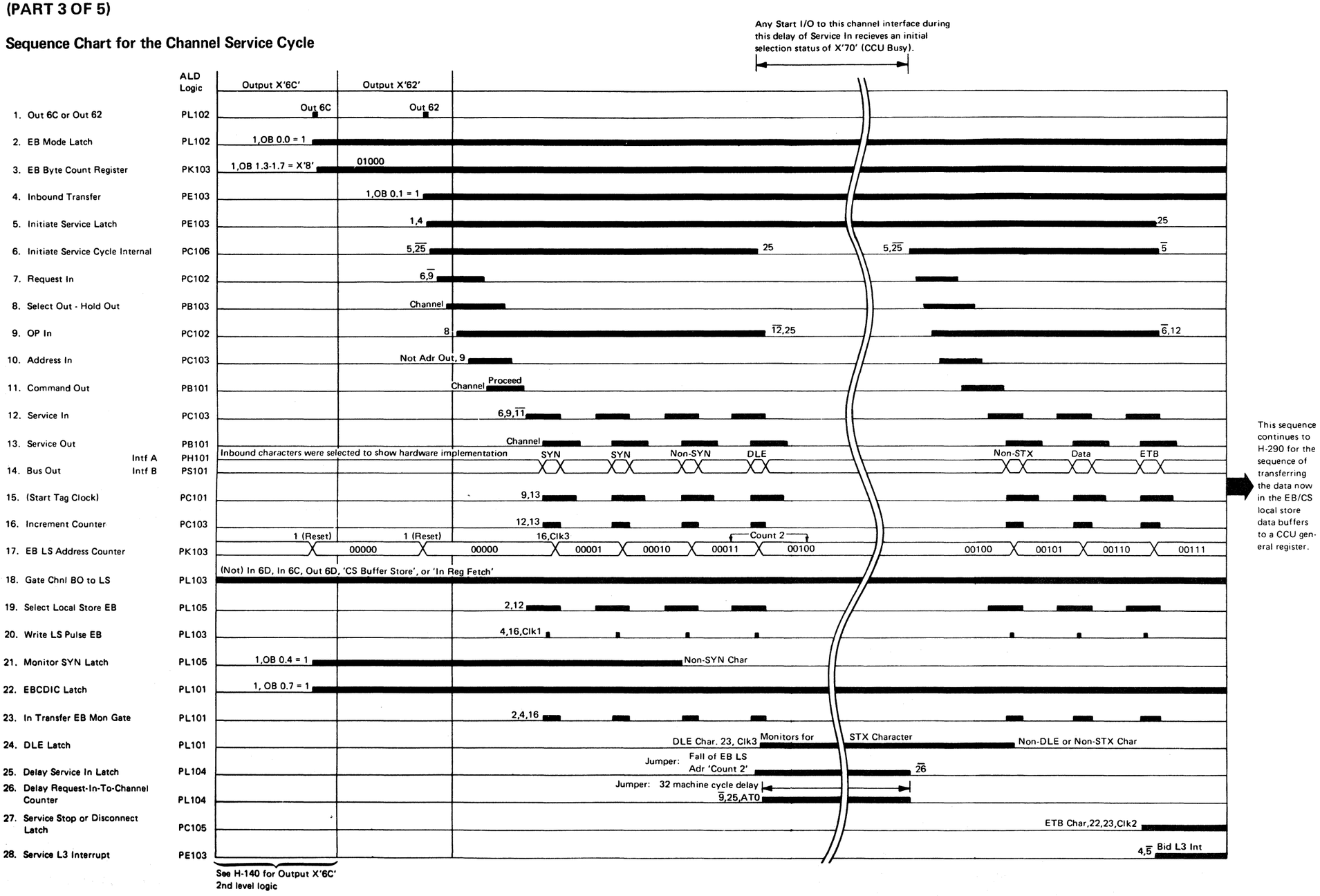
BSC Control Character	EBCDIC Hex	USASCII Hex
STX	02	02
ETX	03	03
DLE	10	10
SYN	32	16
ETB	26	17

USASCII monitor mode ignores channel bus out bit 0 when decoding the control characters.



INBOUND DATA TRANSFERS—EB MODE (PART 3 OF 5)

Sequence Chart for the Channel Service Cycle



This sequence continues to H-290 for the sequence of transferring the data now in the EB/CS local store data buffers to a CCU general register.

INBOUND DATA TRANSFERS—EB MODE (PART 4 OF 5)

Transferring Data From the EB/CS Local Store to the CCU General Register

In response to the type 4 CA data/status level 3 interrupt, the 3705-80 control program must execute the following instructions. The 3705-80 control program uses the transferred byte count from the Input X'6C' instruction to determine how many Input X'60' instructions are required to input all the data. (Four Input X'60' instructions are required in this example.)

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	1001 0000	1.0 = type 4 CA L3 Interrupt 1.3 = selected type 4 CA data/status interrupt 1.6 = 0 type 4 CA #1 selected
Input X'63'	Address	0000 0000	Byte 0 = subchannel address Byte 1 = all zeros
Input X'62'	0100 0100	0000 0XXX	0.1 = inbound data transfer 0.5 = service stop condition—the control program should end the channel command 1.5-1.7 not used for EB mode
Input X'6C'	1000 0001	0000 0111	0.0 = extended buffer mode 0.7 = EBCDIC monitor control latch 1.2-1.7 = 7 transferred byte count—EB mode
Minimum of one cycle delay after Input X'6C'			
Input X'6D'	0011 0010	0011 0010	Byte 0 = SYN character Byte 1 = SYN character
Minimum of one cycle delay after Input X'6D'			
Input X'6D'	XXXX XXXX	0001 0000	Byte 0 = non-SYN character Byte 1 = DLE character
Minimum of one cycle delay after Input X'6D'			
Input X'6D'	YYYY YYYY	ZZZZ ZZZZ	Byte 0 = non-STX character Byte 1 = data character
Minimum of one cycle delay after Input X'6D'			
Input X'6D'	0010 0110	WWWW WWWW	Byte 0 = ETB character Byte 1 = non-data
Minimum of one cycle delay after Input X'6D'			
Output X'6C'	0000 0000	0000 0000	0.0 = reset extended buffer mode 0.7 = 0 reset EBCDIC monitor control latch.

See H-290 for a sequence chart for this operation.

If the ETB character had not ended the data transfer (as in our example) by a service stop, the 3705-80 control program would continue the data transfer after the eight data bytes were transferred to a CCU general register by repeating the sequence starting on H-270.

Ending an Inbound-Data Transfer—EB Mode

The ending of an inbound-data transfer in EB mode is identical to that of the type 1 CA except for the type 4 CA recognition of the BSC control characters as described on page H-260.

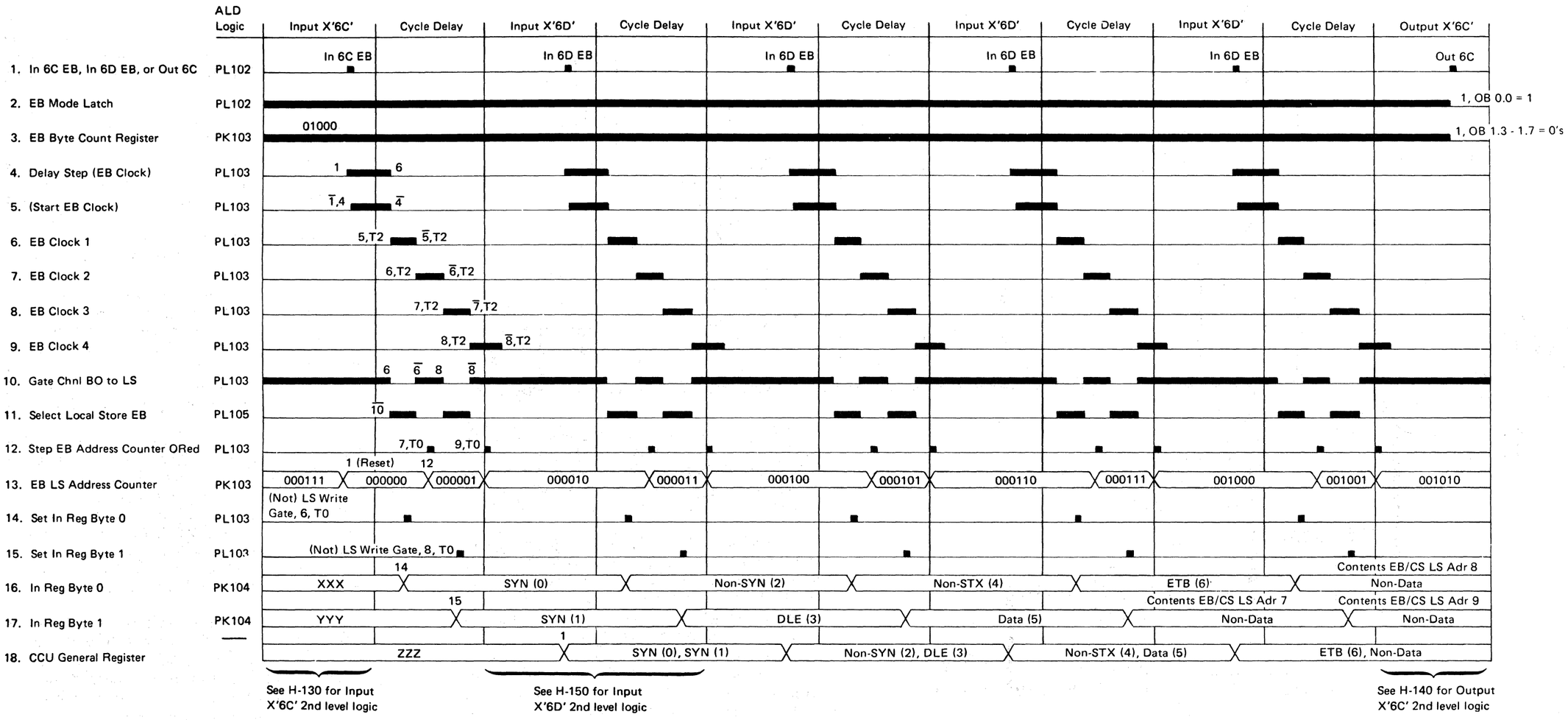
See page 8-280 for endings other than the recognition of the BSC control characters.

See page 8-290 (ESC) for endings caused by the recognition of the BSC control characters (as in the example).

INBOUND DATA TRANSFERS—EB MODE (PART 5 OF 5)

Sequence Chart for Inputting the EB/CS Local Store (Data Buffer)

Continued from H-270



See H-130 for Input X'6C' 2nd level logic

See H-150 for Input X'6D' 2nd level logic

See H-140 for Output X'6C' 2nd level logic

CYCLE STEAL OPERATION–OUTBOUND DATA TRANSFERS (PART 1 OF 4)

Introduction

During an outbound data transfer, the CA4 transfers data from CCU storage to the EB/CS local-store data buffers by cycle stealing. Only EB/CS local-store data buffer addresses 0 and 1 are used during cycle stealing. Cycle stealing always transfers the two data bytes obtained from storage to the EB/CS local-store data buffers. However, if the starting address in CSAR is an odd address, the CA4 only transfers byte 1 to the channel. All subsequent data is transferred two bytes at a time unless the outbound data transfer ends by only transferring byte 0.

The CA4 cycle steals two data bytes to EB/CS local-store data buffers 0 and 1 then raises 'Request In' to request a channel service cycle to transfer these two bytes to the channel. The CA4 then blocks 'Service In' while the CA4 cycle steals two more data bytes. The CA4 then allows 'Service In' to transfer these two data bytes to the channel. This operation continues until the number of bytes transferred equals the specified CS byte count and a data/status level 3 interrupt is requested.

Initializing the Cycle Steal Operation

The 3705-80 control program executes an:

- Output X'6C' to load the 'CS byte count' register with the desired number of data bytes to be passed during the channel transfer and to set 'CS mode'.
- Output X'6F' to load CSAR byte 0 and 1 with the storage address of the location containing the first byte of data to be transferred by cycle stealing **1** . CSAR byte X is forced to ones and then stepped to zeros to save executing Output X'6E' if the extended address bits are zeros. **2**
- Output X'6E' to load CSAR byte X if the extended address bits X.6-X.7 are not zeros. **3**
- Output X'62' to set (1) outbound data transfer, (2) the 'priority outbound-data transfer sequence' (if desired) and (3) the 'CS proceed' latch to start the cycle steal operation.

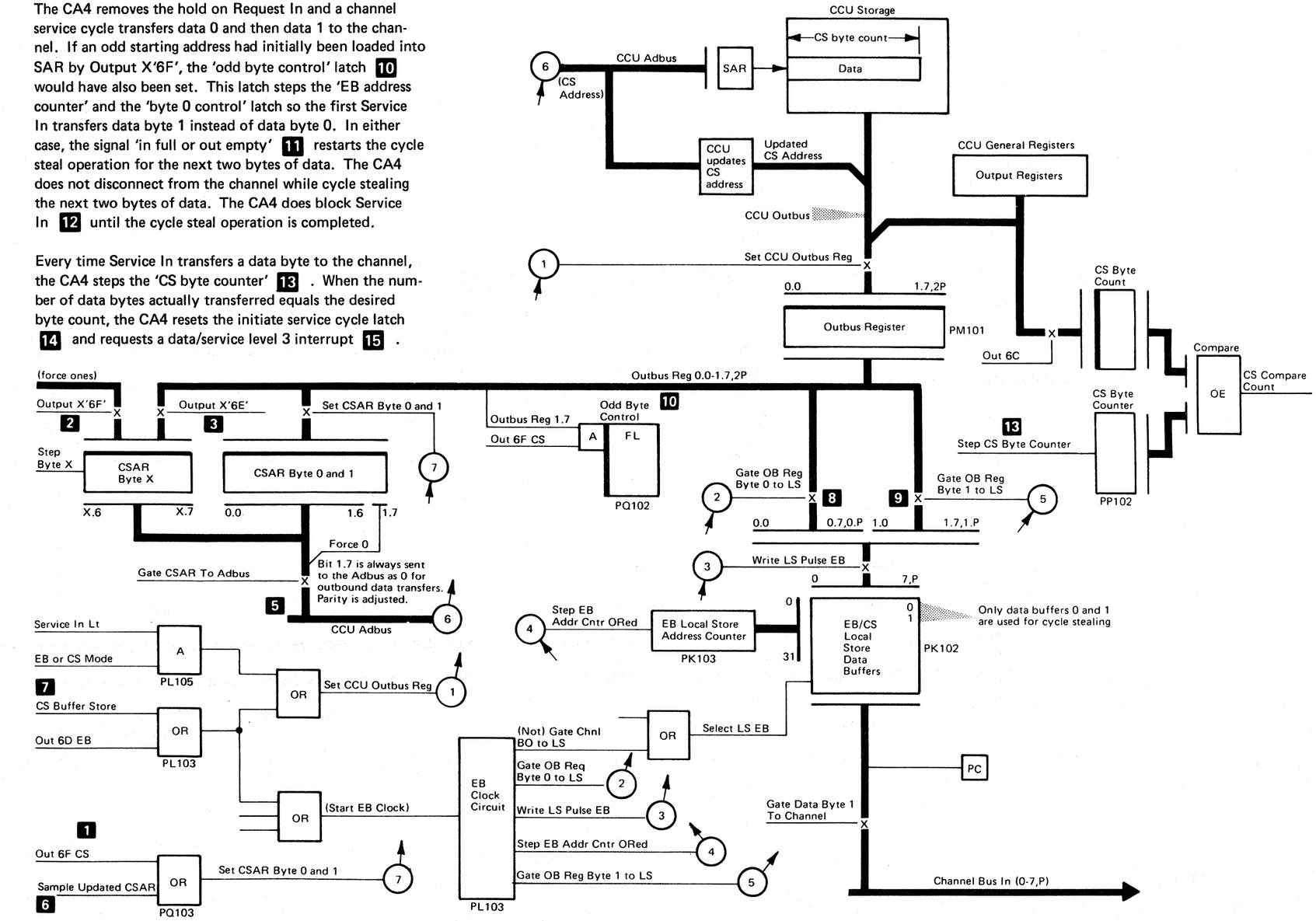
Details of Cycle Stealing Operation

The key numbers in the paragraphs below refer to the data flow diagram on this page and/or the CS sequence chart on H-320.

Once 'CS proceed' is active, the CA4 blocks Request In **4** . After the CA4 has bid for a cycle-steal machine cycle and the CCU responds with 'go channel 1', the CA4 gates the address in CSAR **5** (on a half-word boundary) to SAR so the CCU can obtain the half word of data during the cycle steal machine storage read. The CCU increments the address by two and places it on the 'CCU outbus'. The CA4 reloads CSAR with the updated address from the CCU **6** . 'CS buffer store' **7** signals the CA4 to load data byte 0 into EB/CS LS buffer address 0 **8** and data byte 1 into buffer address 1 **9** and then reset the 'EB LS address counter'.

The CA4 removes the hold on Request In and a channel service cycle transfers data 0 and then data 1 to the channel. If an odd starting address had initially been loaded into SAR by Output X'6F', the 'odd byte control' latch **10** would have also been set. This latch steps the 'EB address counter' and the 'byte 0 control' latch so the first Service In transfers data byte 1 instead of data byte 0. In either case, the signal 'in full or out empty' **11** restarts the cycle steal operation for the next two bytes of data. The CA4 does not disconnect from the channel while cycle stealing the next two bytes of data. The CA4 does block Service In **12** until the cycle steal operation is completed.

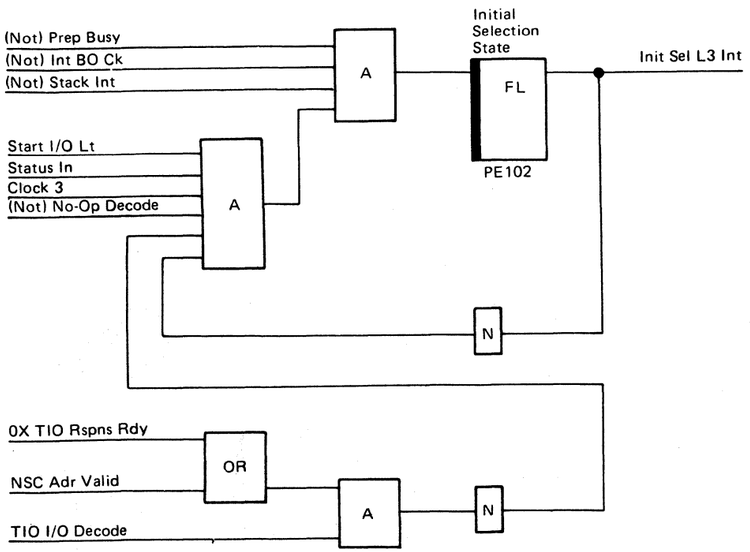
Every time Service In transfers a data byte to the channel, the CA4 steps the 'CS byte counter' **13** . When the number of data bytes actually transferred equals the desired byte count, the CA4 resets the initiate service cycle latch **14** and requests a data/service level 3 interrupt **15** .



OUTBOUND DATA TRANSFERS—CS MODE (PART 2 OF 4)

Outbound data transfers result from channel Read commands that direct the transfer of data from 3705-80 storage to the host processor. When the CA is in cycle steal mode, the CA4 does not require control program intervention (once cycle stealing has been initialized) until the channel data transfer has been completed and the CA4 requests a level 3 interrupt. The fetching of data from CCU storage is automatically done by the cycle steal hardware whether the CA4 is in ESC or NSC mode.

CA Decodes the Command and Requests an Interrupt



The 3705-80 control program responds to the initial select level 3 interrupt with the following instructions.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	1000 10X0	1.0 = type 4 CA level 3 interrupt 1.4 = selected type 4 CA initial selection level 3 interrupt 1.6 = 0 type 4 CA #1 selected = 1 type 4 CA #2 selected
Input X'60'	1000 0000	0000 0000	Normal initial selection (Note 1)
Input X'61'	address	command	Byte 0 = address Byte 1 = command
Output X'63'	address	0000 0000	Byte 0 = transfer address Byte 1 = all zeros
Output X'6C'	0100 0000	0000 0111	0.1 = set cycle steal mode 1.0-1.7 = X'03' to transfer three data bytes out (Note 2) Resets EB adr counter to adr 00
Output X'6F'	address	address	Byte 0 = CSAR byte 0 Byte 1 = CSAR byte 1 Resets CSAR byte X Sets 'odd byte control' latch if CSAR bit 1.7=1
Output X'6E'	0000 0000	0000 XXXX	Byte 0 = all zeros Byte 1 bits 6-7 = extended address bits for CSAR byte X
Output X'62'	1000 0100	0000 0100	0.0 = outbound data transfer 0.5 = reset 'initial select state' 1.5 = set priority outbound-data transfer sequence Sets 'CS proceed' latch to start the cycle steal operation

Initial Selection Address In and Status In Response

This instruction is not needed if the extended address bits X.6 and X.7 are zeros.

Outbound transfer initiates a channel data service cycle. See H-330 for a sequence chart for this operation and the channel service cycle.

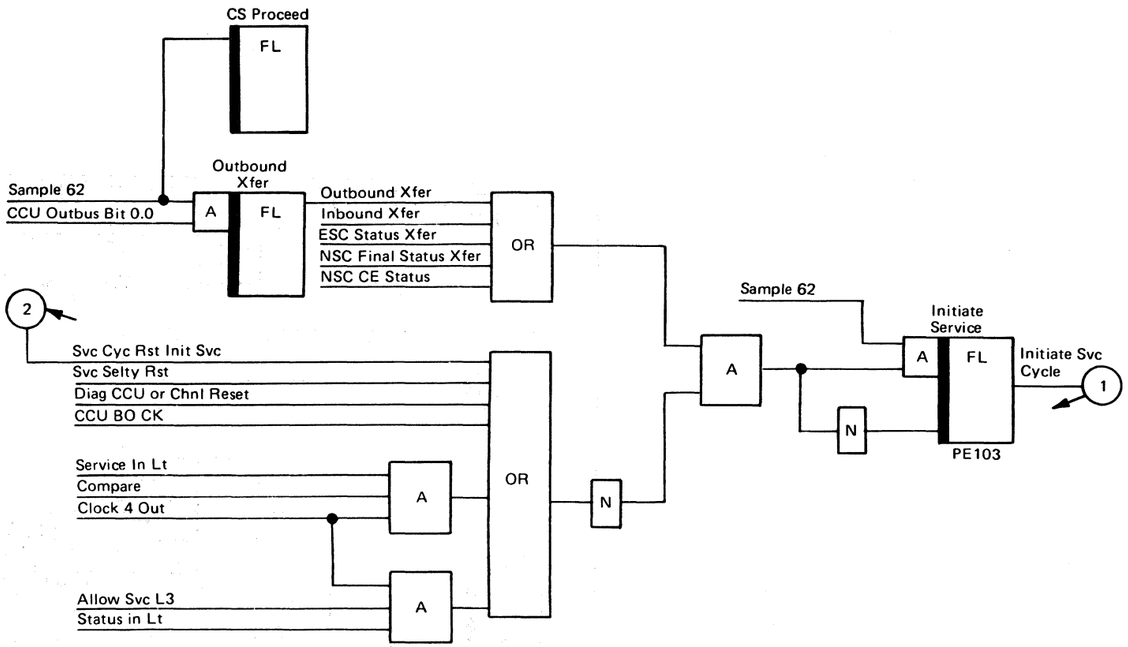
Notes:

1. *Other bits may be transferred to the CCU during this input. If other bits are on, the 3705-80 control program must take action differently from the normal initial selection.*
2. *From 1 to 256 bytes of data may be transferred to the channel.*

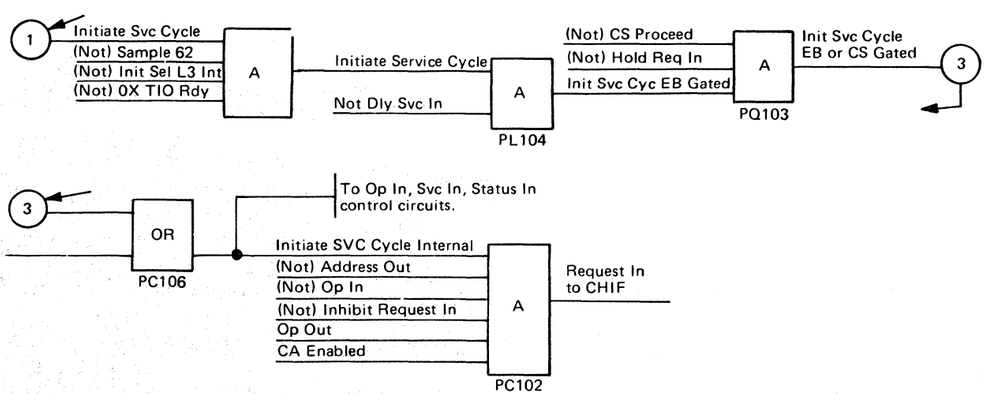
OUTBOUND DATA TRANSFERS—CS MODE (PART 3 OF 4)

CA to Channel Data Transfer—See H-300 for Sequence Chart

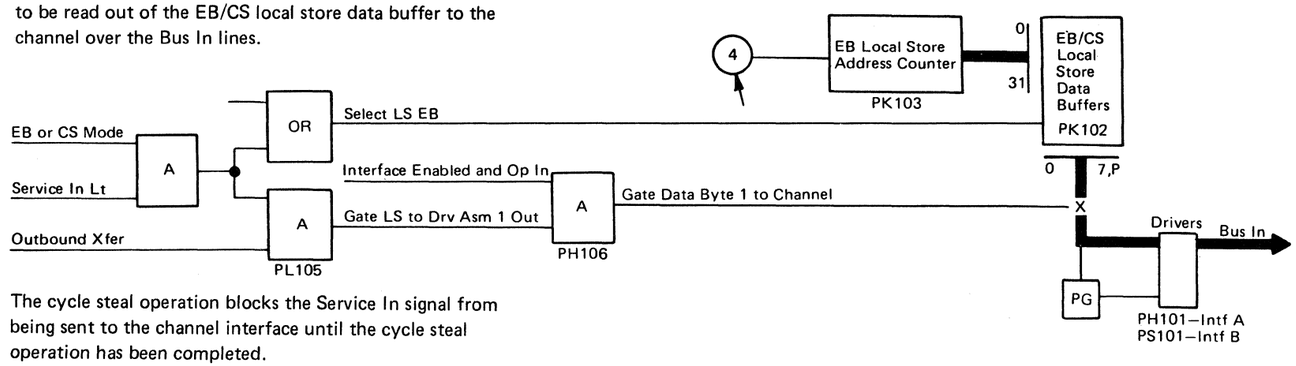
The Output X'62' instruction starts (1) a cycle steal operation that loads two bytes of data into the EB/CS local store and (2) a channel service cycle so that the data loaded into the EB/CS local store can be transferred to the channel.



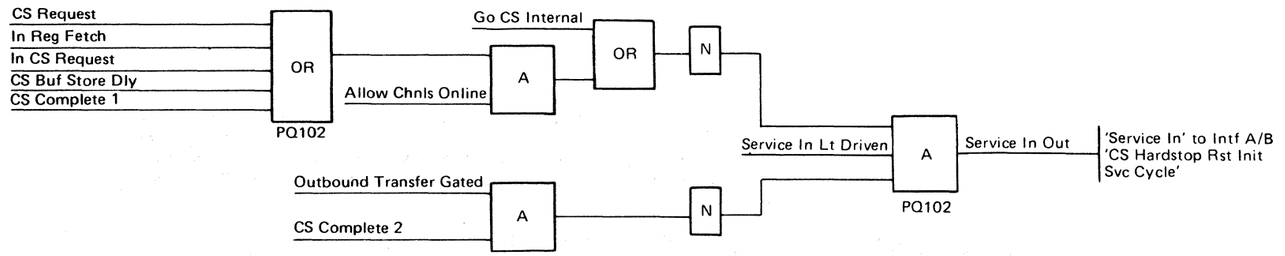
The CA4 sends Request In to the channel to start the service cycle.



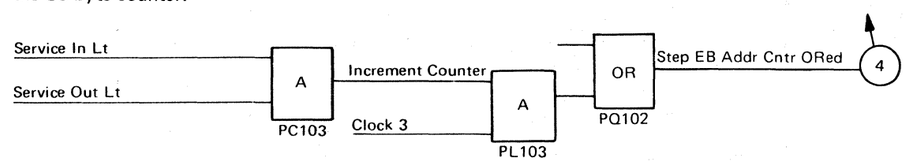
When the Service In latch is set, it causes the next data byte to be read out of the EB/CS local store data buffer to the channel over the Bus In lines.



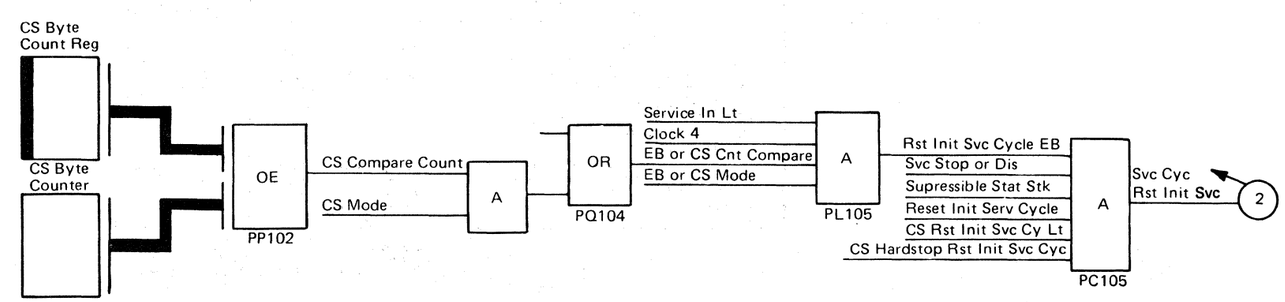
The cycle steal operation blocks the Service In signal from being sent to the channel interface until the cycle steal operation has been completed.



When the channel returns Service Out, the channel tag clock operates to synchronize the CA and channel. Service Out also increments the EB local store address counter and steps the CS byte counter.

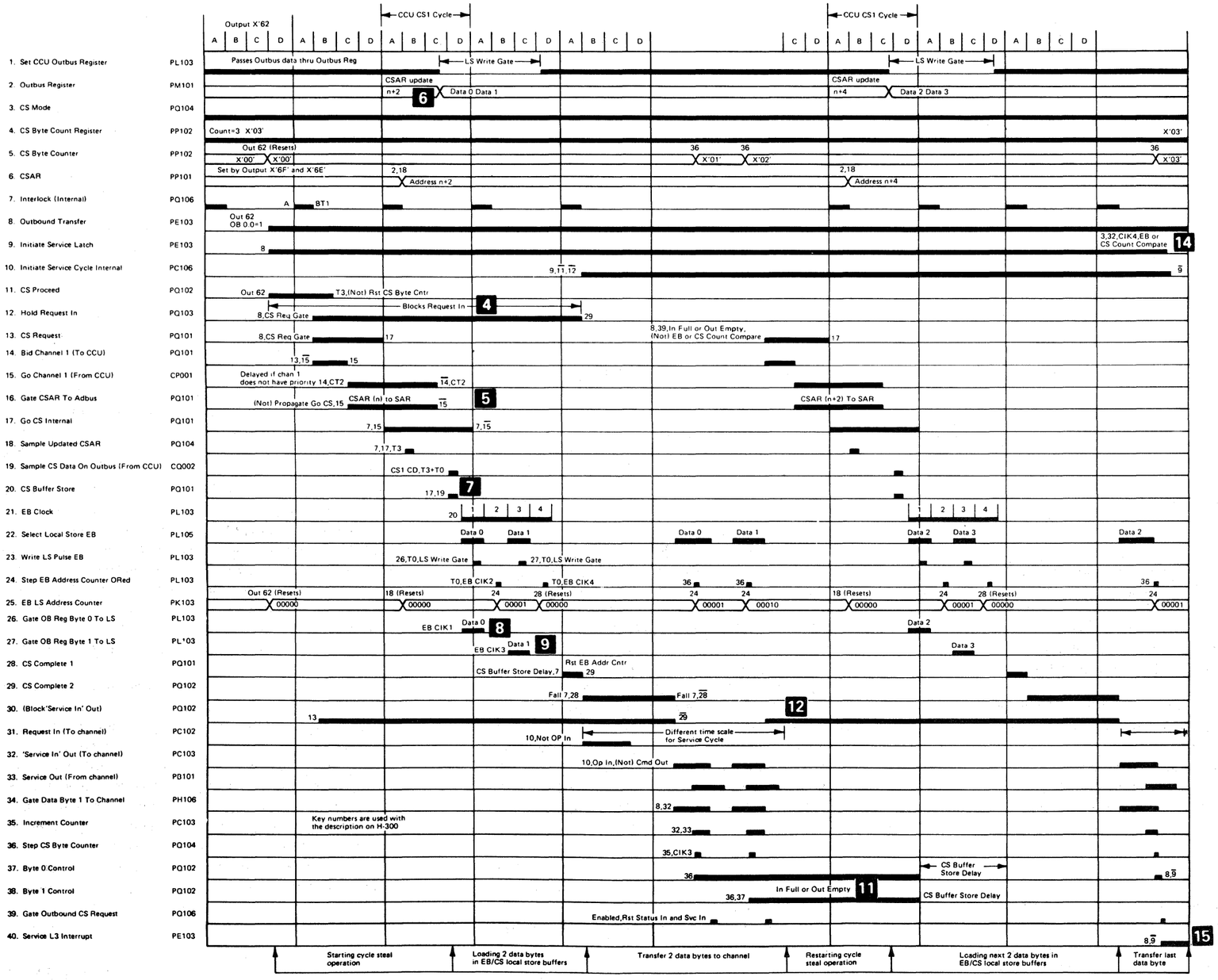


The data transfer stops when the value of the CS byte counter equals the byte count to be transferred in the CS byte count register.



OUTBOUND DATA TRANSFERS—CS MODE (PART 4 OF 4)

CS Sequence Chart—Outbound



This sequence continues into the automatic CA4 selection by priority sequence chart on H-240 that is applicable if two type 4 CAs are installed. If only one type 4 CA is installed, the operation is the same as for the type 1 CA (See page 8-330 for the control program response to the level 3 data/status interrupt).

CYCLE STEAL OPERATION—INBOUND DATA TRANSFERS (PART 1 OF 4)

Introduction

During an inbound data transfer, the CA4 transfers data from the EB/CS local-store data buffers to CCU storage by cycle stealing. Only EB/CS local-store data buffer addresses 0 and 1 are used during cycle stealing. Cycle stealing always transfers the two data bytes obtained from the EB/CS LS data buffers to storage. However, if the starting address in CSAR is an odd address, the CCU stores data byte 1 (from the channel) and rewrites storage byte 0 in storage. All subsequent data is transferred two bytes at a time unless the inbound-data transfer ends by only transferring data byte 0. In this case, the CCU stores data byte 0 (from the channel) and rewrites storage byte 1 in storage.

The CA4 raises 'Request In' to start a data service cycle so that the channel can transfer one or two data bytes to the EB/CS LS data buffer. The CA4 then starts a cycle steal operation that loads the In register with the contents of the EB/CS LS data buffers 0 and 1. The CA4 requests that the CCU take a cycle-steal machine cycle to store the data in the In register at the address sent to the CCU over the Adbus and whether to store byte 0, byte 1 or bytes 0 and 1. The CCU updates the address and sends it back to the CA4 where it is loaded into CSAR. During the cycle steal operation, the CA4 blocks the 'Service In' signal from being sent to the channel. Once the cycle steal operation is completed, 'Service In' is sent "out" to the channel and the channel resumes transferring two more data bytes to the EB/CS LS data buffer. This operation continues until a BSC ending control character is detected in the data from the channel or the number of data bytes received equals the specified CS byte count and then the CA4 requests a level 3 interrupt.

Initializing the Cycle Steal Operation

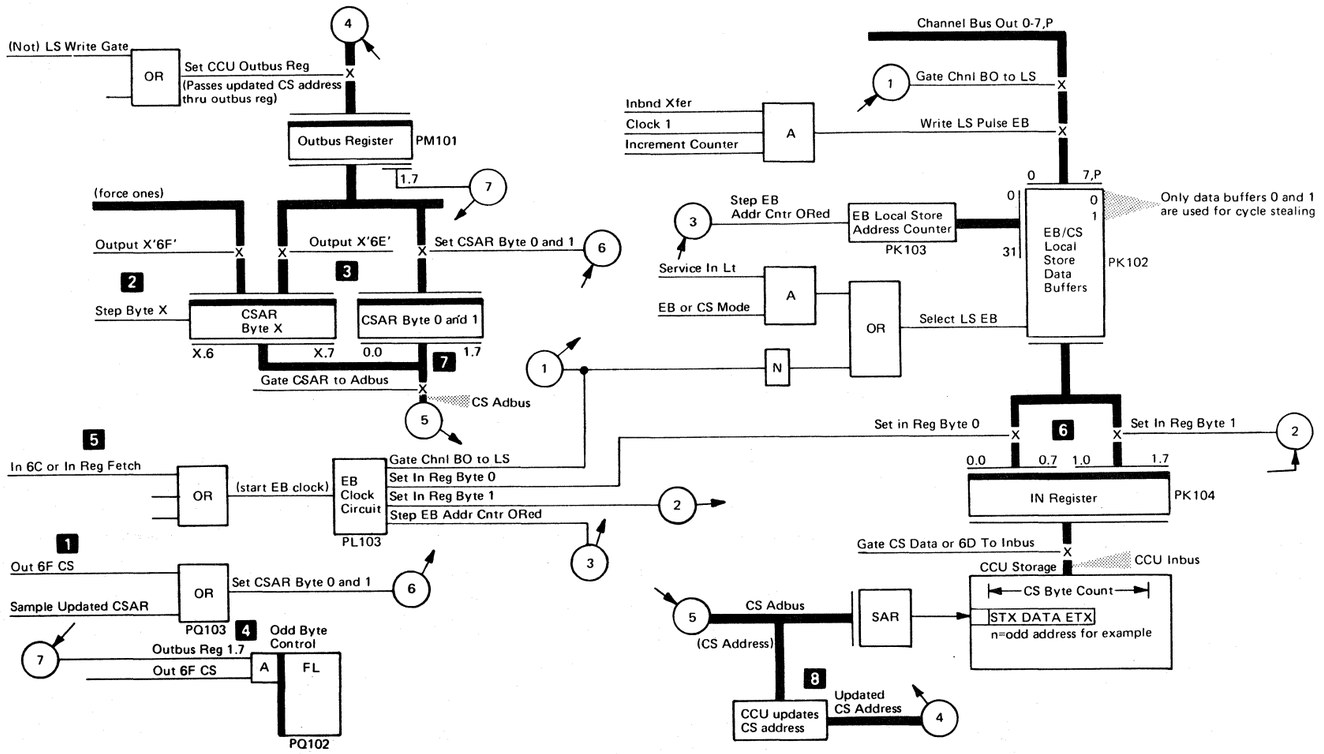
The 3705-80 control program executes an:

- Output X'6C' to load the 'CS byte count' register with (1) the expected number of data bytes to be received during the channel transfer or (2) a byte count in excess of the expected number of data bytes where a BSC ending control character normally ends the data transfer. Output X'6C' sets 'CS mode' and also sets the BSC monitor control latches if they are desired.
- Output X'6F' to load CSAR bytes 0 and 1 with the storage address location in which the first byte of data is to be stored by cycle stealing **1** . CSAR byte X is forced to ones and then stepped to zeros to save executing Output X'6E' if the extended address bits are zeros **2** .
- Output X'6E' to load CSAR byte X if the extended address bits X.6 and X.7 are not zeros **3** .
- Output X'62' to set (1) inbound data transfer and (2) the 'CS proceed' latch to start the cycle steal operation.

Details of the Cycle Stealing Operation

The key numbers in the paragraphs below refer to the data-flow diagram on this page and/or the CS sequence chart on H-360.

The CA4 raises 'Request In' to start a data service cycle. The example illustrated in the CS sequence chart on H-360 assumes that the address in CSAR points to an odd boundary, therefore Output X'6F' sets the 'odd byte control' latch **4** . This latch steps the EB address counter to 1 and sets 'byte 0 control' so that the first data byte transferred by the channel is loaded in EB/CS LS data buffer 1. The CA4 (1) steps the CS byte counter to one (2) turns on 'byte 1 control' to indicate that the buffer is full, (3) turns on 'CS request' to bid for a CS1 machine cycle, and (4) blocks sending 'Service In' to the channel. 'In reg fetch' **5** resets the EB LS address counter to 0 and starts the EB clock. This loads the contents of buffer 0 (old data) into In register byte 0 and data byte 1 (STX) from buffer 1 into In register byte 1 **6** .



The CCU returns 'go chan 1' when the next machine cycle will be a CS1 machine cycle. The CA4 then sends all 18 bits of the address from CSAR to SAR over the CS adbus **7** and sends 'store byte 1' to signal the CCU that only data byte 1 is to be stored. The CA4 gates the In register contents to SDR (storage data register) byte 1 from which data byte 1 is stored. The CCU updates the address to an even address by incrementing by one or two **8** (depending on how many bytes were stored) and returns the address (16 bits) over the CCU outbus. The CA4 then loads the updated address into CSAR bytes 0 and 1. Since byte X of the updated address is not returned, the CA4 must update CSAR byte X if a carry from bit 0.0 to X.7 occurred during the CCU update. The CA4 knows a carry occurred if the updated address on the CCU outbus equals zero when sampling the updated CSAR and steps CSAR byte X.

The CA4 sends 'Service In' to the channel **9** when the cycle steal operation has been completed. The data service cycle resumes and the channel transfers the next two data bytes to EB/CS LS data buffers 0 and 1. This service cycle operation is the same operation that occurs when the starting CS address is even and the 'odd byte control' latch is off. Aside from loading two data bytes instead of one, this service cycle and cycle steal operation is identical to that described above except that 'store byte 0' and 'store byte 1' signals are both sent to the CCU when the CSAR address is sent to SAR **10** .

The CA4 monitors the data transferred from the channel for BSC ending control characters ETB or ETX when in ESC mode and the monitor control latches are set. If either of these ending characters is detected **11** on the channel Bus Out, the CA4 sets the 'service stop or disconnect' latch that resets the 'initiate service' latch stopping the service cycle and requests a level 3 interrupt. (See H-260). **12**

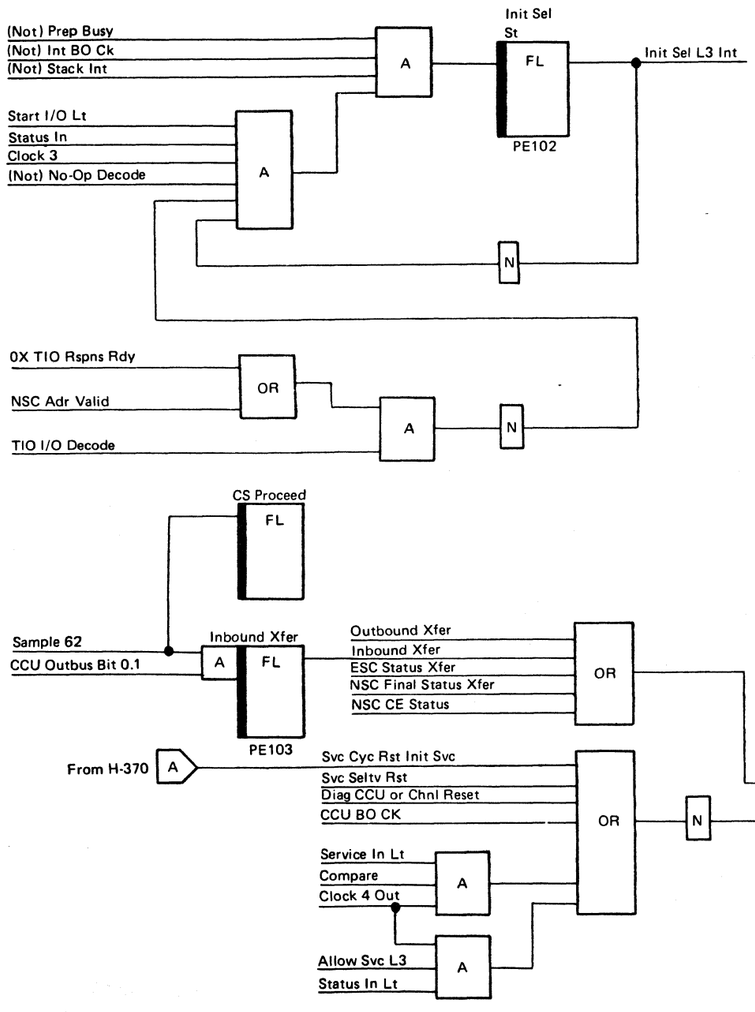
Every time Service Out transfers a data byte from the channel, the CA4 steps the 'CS byte counter'. When the number of data bytes received equals the desired count in the 'CS byte count' register, the CA4 raises 'reset initiate service cycle EB' that resets the 'initiate service cycle' latch stopping the service cycle and requests a level 3 interrupt.

INBOUND DATA TRANSFERS–CS MODE (PART 2 OF 4)

Inbound data transfers result from commands that require the passing of data from the host processor to 3705-80 storage.

When the commands are decoded, they request an initial selection level 3 interrupt so that the 3705-80 control program can determine what action to take to service the command. The commands start an initial selection sequence as shown on 8-170.

CA Requests an Initial Selection Level 3 Interrupt



Control Program Responds to the Interrupt

The 3705-80 control program responds to the initial selection level 3 interrupt with the following sequence of instructions.

Instruction	General Register Bits Byte 0	Byte 1	Indication or Function
Input X'77'	0000 0000	1000 1000	1.0 = type 4 CA level 3 interrupt 1.4 = selected type 4 CA initial selection level 3 interrupt 1.6 = 0 type 4 CA #1 selected
Input X'60'	1000 0000	0000 0000	Normal initial selection*
Input X'61'	Address	Command	Byte 0 = subchannel address Byte 1 = command
Output X'63'	Address	0000 0000	Byte 0 = address Byte 1 = all zeros
Output X'6C'	0100 1001	0000 1000	0.1 = set cycle steal mode 0.4 = set SYN monitor control latch 0.7 = set EBCDIC monitor control latch 1.0-1.7 = X'08' to transfer eight data bytes Resets EB adr counter to adr 00
Output X'6F'	Address	Address	Byte 0 = CSAR byte 0 Byte 1 = CSAR byte 1 Resets CSAR byte X Sets 'odd byte control' latch if CSAR bit 1.7=1
Output X'6E'	0000 0000	0000 XXXX	Byte 0 = all zeros Byte 1 bits 6-7 = address bits for CSAR byte X
Output X'62'	0100 0110	0000 0000	0.1 = inbound data transfer 0.5 = reset initial selection 0.6 = reset data/status control 1.6-.17 = 0; check for 4 SYN chars Sets 'CS proceed' latch to start the cycle steal operation

Initial selection Address In and Status In response

This instruction is not needed if the extended address bits X.6 and X.7 are zeros.

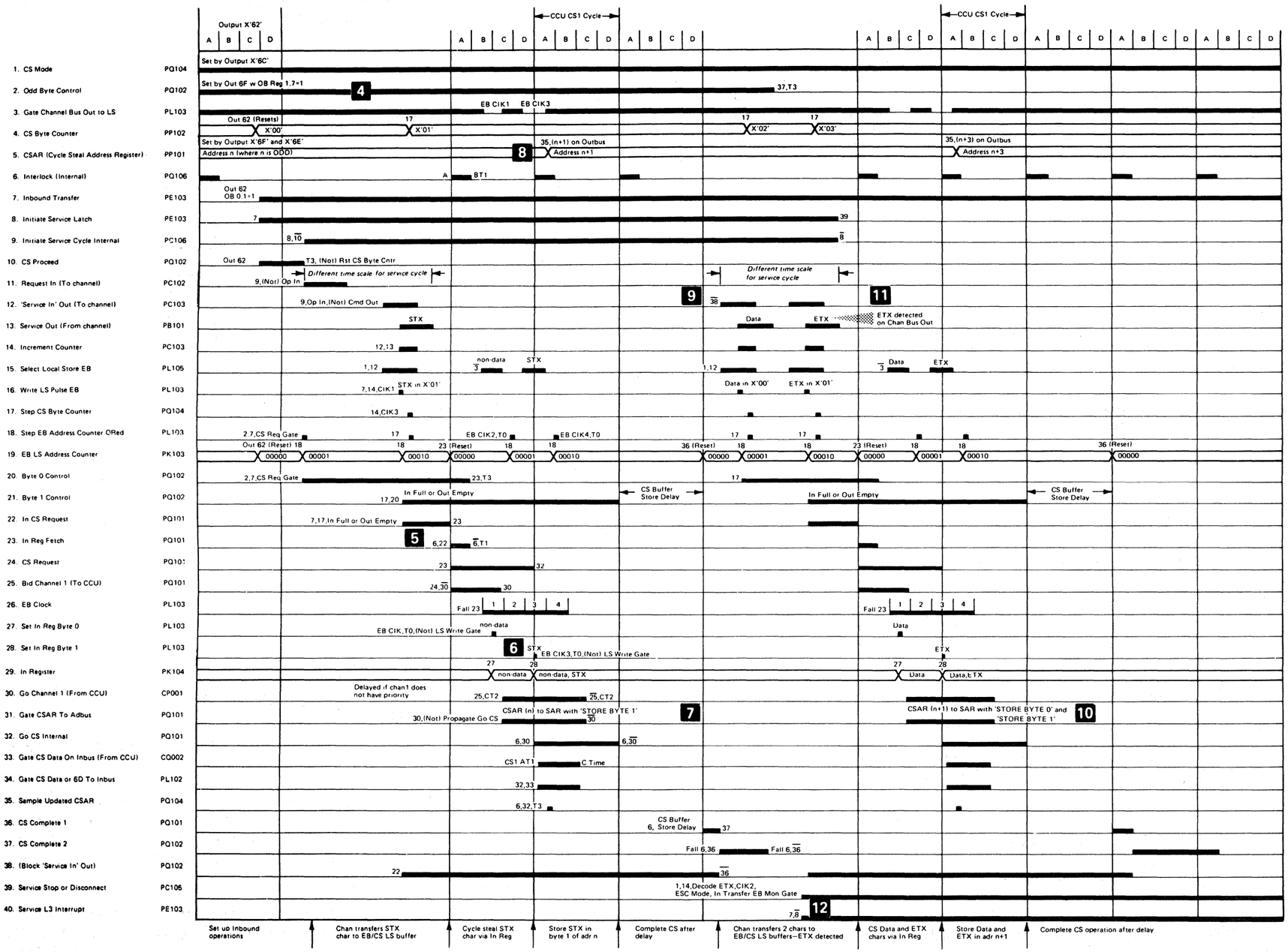
Inbound transfer initiates a channel data service cycle 'CS proceed' initiates a cycle steal operation. See H-360 for the combined sequence of operation assuming the CS begins on an odd byte address.

*If other bits are on during this input, the 3705-80 control program must take appropriate action to service the condition indicated by the bit.

The Output X'62' instruction initiates a channel service cycle to transfer the data from the host processor to the CA EB/CS local store.

INBOUND DATA TRANSFERS–CS MODE (PART 3 OF 4)

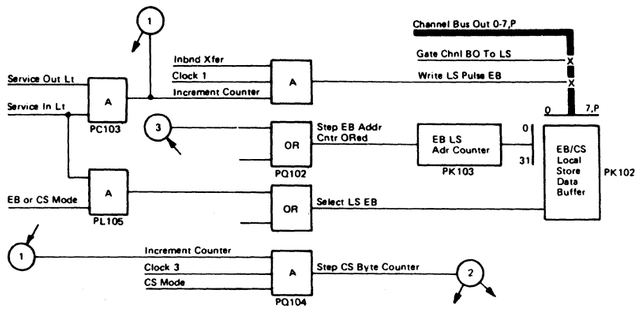
CS Sequence Chart–Inbound



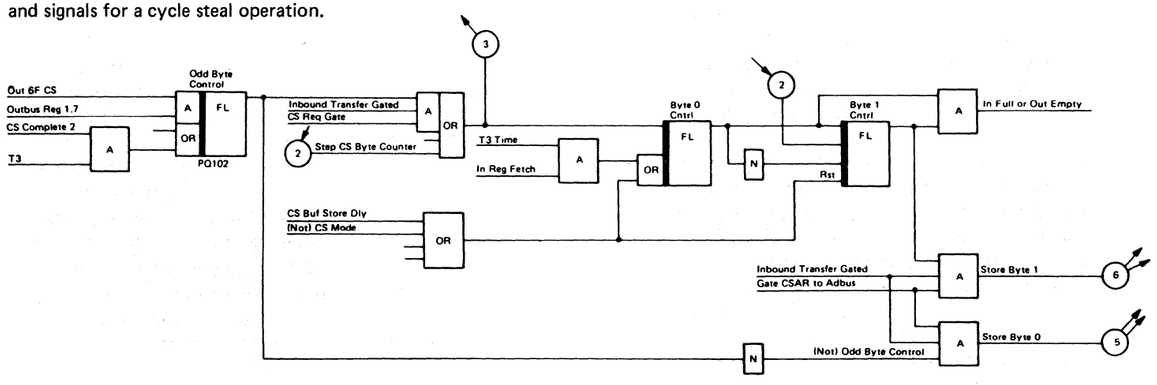
INBOUND DATA TRANSFERS–CS MODE (PART 4 OF 4)

See H-360 Sequence Chart

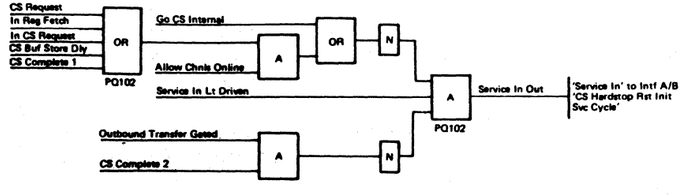
When the channel returns Service Out in response to Service In, the channel tag clock operates to synchronize the CA4 and channel. The CA4 writes the data byte on channel Bus Out into the EB/CS LS data buffer and then steps the EB local-store address counter.



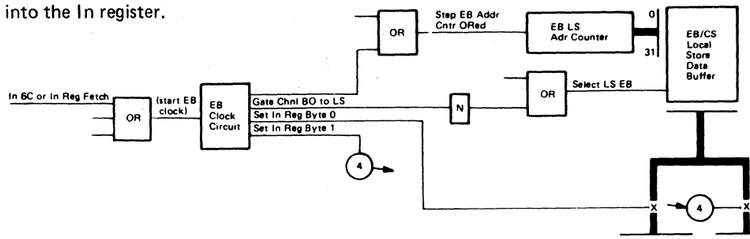
In our example the starting address in CSAR is odd, therefore the 'odd byte control' latch had set the 'byte 0 control' latch and had stepped the EB address counter to 1. When the first data byte is written into the EB/CS LS data buffer, the CA4 steps the CS byte counter and sets the 'byte 1 control' latch. This indicates that the data buffers are filled and signals for a cycle steal operation.



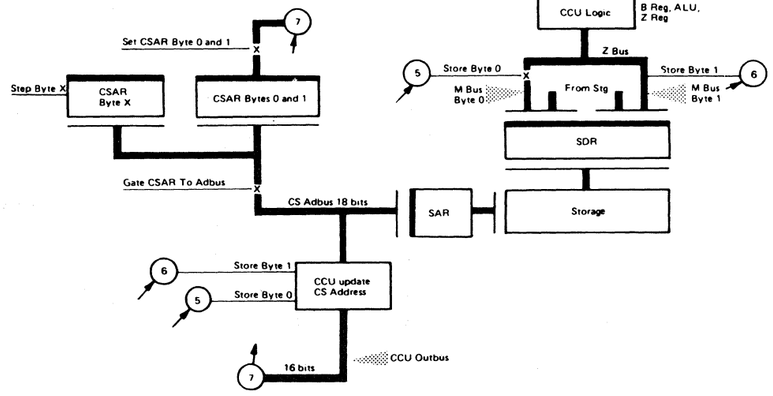
The cycle steal operation blocks the Service In signal from being sent to the channel interface until the cycle steal operation has been completed.



'In reg fetch' starts the EB clock that provides the timing pulses to load the data bytes from buffer 0 then buffer 1 into the In register.

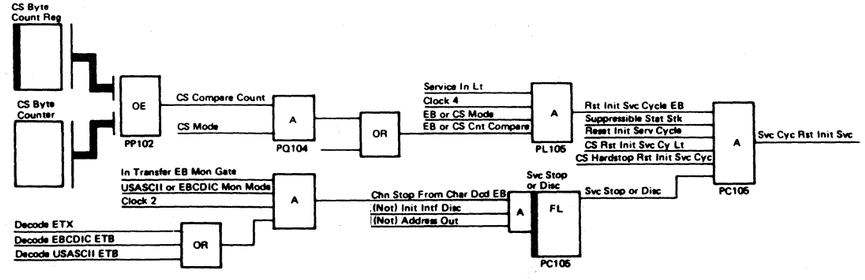


When the CCU takes a CS1 machine cycle, the CCU loads the SDR depending on which "store byte" lines are active then stores the SDR contents into the storage location addressed by the CSAR address.



The CCU updates the address and returns it to CSAR.

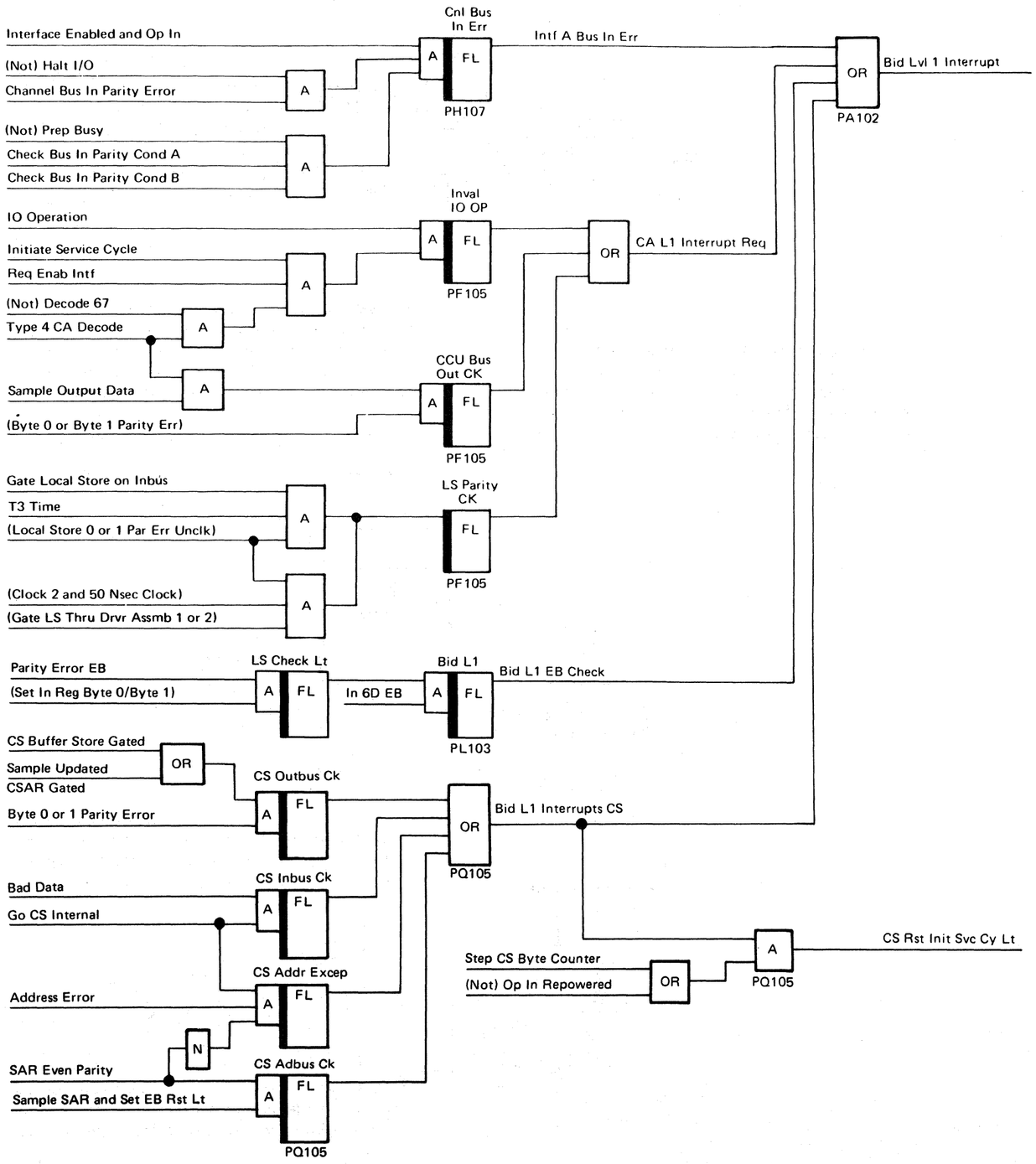
The service cycle operation resumes after the cycle steal operation is completed. This service-cycle cycle-steal routine keeps repeating (without any normal program interrupts) until (1) the CA4 detects an ETX or ETB character in the data transferred from the channel provided the CA4 is in ESC mode and the monitor control latches are set (see H-260), or (2) the CA4 has received the number of data bytes equal to the desired count in the 'CS byte count' register. Either condition resets the initiate service latch that stops the service cycle operation and requests a level 3 interrupt.



CA4 ERROR INTERRUPTS

The type 4 channel adapter requests a level 1 interrupt whenever:

- A channel 'Bus-In' check occurs.
  The channel adapter hardware detects bad parity in the data byte being sent across the channel to the CPU.
  The control program should respond to the interrupt with an Input X'67' instruction to transfer the contents of the error condition register to the CCU. Bit 1.0 should be transferred if a channel 'Bus-In' check occurred.
- An in/out instruction accept check occurs.
  An in/out instruction accept check (invalid I/O op) occurs if the control program executes an Input or Output X'60' through X'66' or X'6C' through X'6F' instruction while the CA is actively handling any data or status transfer sequence. When the control program responds to the level 1 interrupt with an Input X'67', bit 1.1 is transferred to the CCU.
- A 'CCU Outbus' check occurs.
  When bad parity is detected on the 'CCU Outbus', the CA requests a level 1 interrupt. Bit 1.2 is returned to the CCU from the error condition register when the control program executes an Input X'67' instruction in response to the interrupt.
- A local store check occurs.
  Bad parity being gated from the local store registers causes a level 1 interrupt request. Bit 1.3 is returned to the CCU from the error condition register when the control program executes an Input X'67' instruction in response to the interrupt.
- An EB local store check occurs.
  Bad parity being gated from the EB local store during Input X'6C' or Input X'6D' sets the 'local store check' latch. The next Input X'6D' instruction causes a level 1 interrupt request. Bit 1.3 is returned to the CCU from the error condition register when the control program executes an Input X'67' instruction in response to the interrupt.
- CS outbus check occurs.
  When bad parity is detected on the 'CCU Outbus' during a cycle steal data transfer, the CA requests a level 1 interrupt. Bit 0.0 is returned to the CCU from the 'CS error register' when the control program executes an Input X'6E' instruction in response to the interrupt.
- CS inbus check occurs.
  When the CCU raises 'bad data' to signal that the CCU has detected even parity on the 'CCU inbus' during a cycle-steal data transfer, the CA requests a level 1 interrupt. Bit 0.1 is returned to the CCU from the 'CS error register' when the control program executes an Input X'6E' instruction in response to the interrupt.
- CS address bus check occurs.
  When the CCU raises 'SAR even parity' to signal that the CCU has detected incorrect parity (even) on the 'CS adbus' during a cycle-data transfer, the CA requests a level 1 interrupt. Bit 0.2 is returned to the CCU from the 'CS error register' when the control program executes an Input X'6E' instruction in response to the interrupt.
- CS address exception occurs.
  When the CCU raises 'address error' without 'SAR even parity' to signal that the CCU has received an address from a type 4 CA that is within a protected section of storage.



INITIAL SELECTIVE RESET, INITIAL INTERFACE DISCONNECT AND SERVICE SELECTIVE RESET—SELECTOR CHANNEL CONTROLS

The 'gate 60 or reset' FL is to prevent losing a second interrupt while the CA4 is handling a previous interrupt.

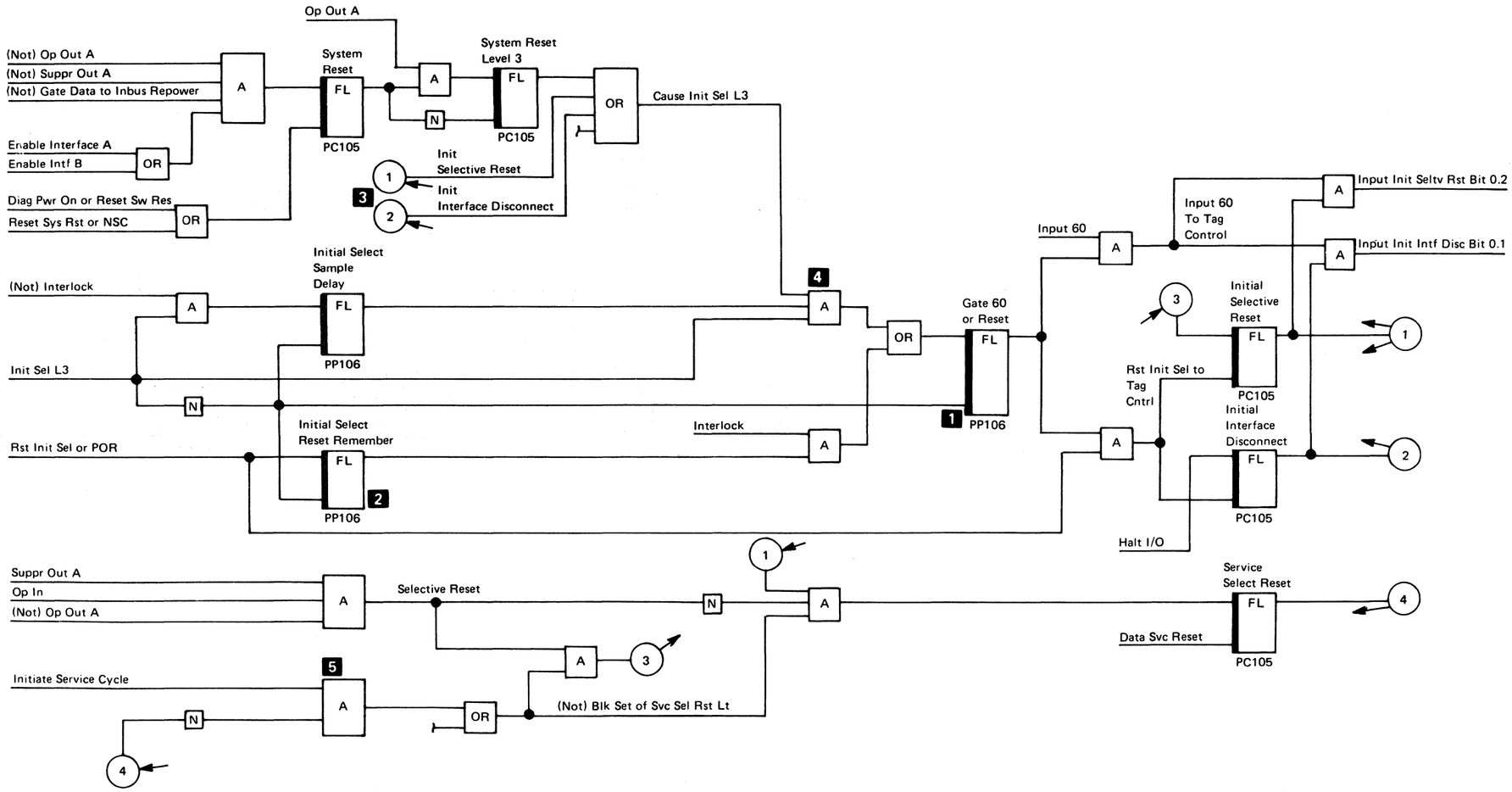
During a normal initial select L3 interrupt (not caused by selective reset or halt I/O), the 'gate 60 or reset' FL **1** is reset, which:

- Prevents either inputting or resetting the 'initial selective reset' FL or 'initial interface disconnect' FL.
- Prevents the 'service selective reset' FL from being set.

If selective reset or halt I/O occurs during a normal initial select L3 interrupt, their respective latch will be set and after the original initial select is reset **2** , the two latches can be inputted and/or reset.

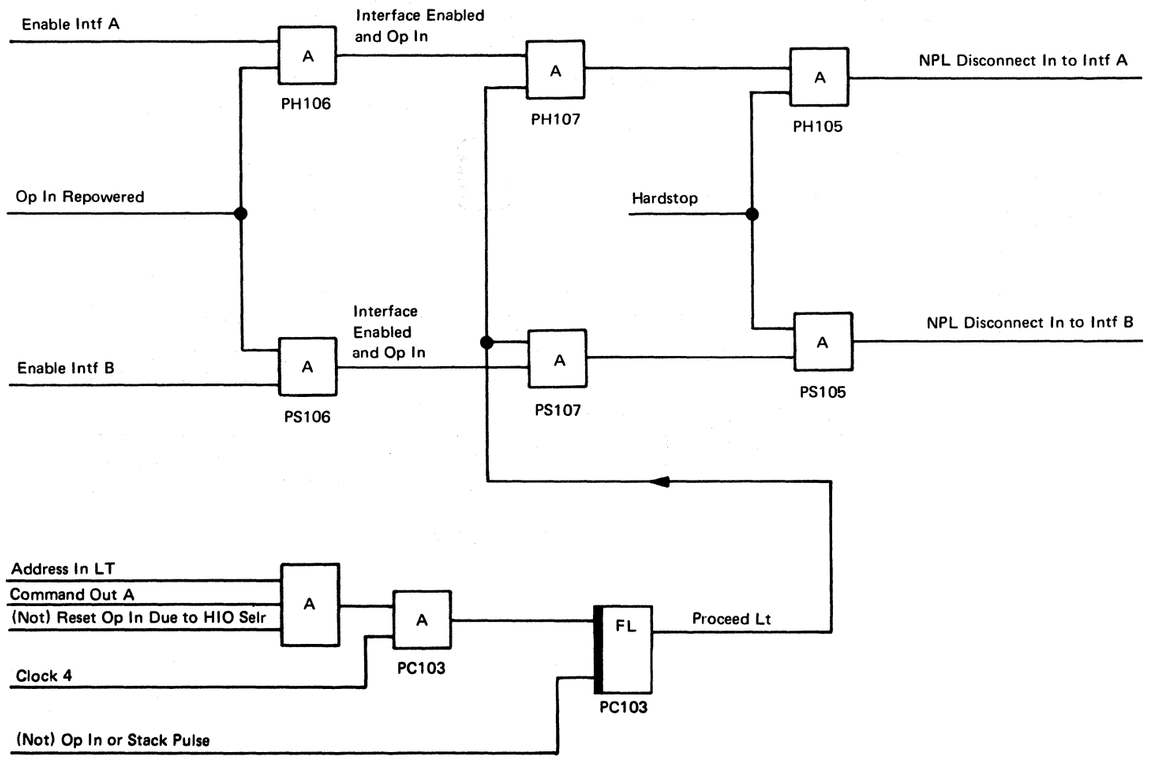
If the initial select L3 interrupt is caused by a selective reset or Halt I/O **3** (no initial select L3 interrupt was in progress), the two latches can be inputted or reset **4** .

The service selective reset can only be set when the CA4 is transferring data over the channel (initiate service cycle active) **5**



DISCONNECT IN–SELECTOR CHANNEL

Disconnect In is gated to the channel interface (A or B when a hardstop condition occurs and the CA4 is actively operating with the channel.



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