IBM Maintenance Library

3705-80 Communications Controller
Theory-Maintenance
Volume I

(D99-3705F-01)

SY27-0208-1

Preface

This publication is directed to the Customer Engineer assigned to maintain the IBM 3705-80 Communications Controller. He is assumed to be trained on either a System/360, System/370, 4300 Processor, or 3031, 3032, 3033, or 3081 Processor Complex and to have a teleprocessing background.

This publication should be used to locate and replace failing field replaceable units within the controller. Pictures are combined with text to convey basic operational concepts. No attempt is made to provide detailed theory information. Each page contains one topic (although some topics may require more than one page).

The CE should always begin at the "start" section of Volume I when trying to locate a failure. This section contains a flowchart that points to the correct part of the manual for locating the failure.

The 3705-80 FETMM consists of three volumes which are identified by two form numbers. The volumes may be placed in separate binders for ease of use.

Volume I (SY27-0208) contains comphrensive "how to fix information." Information is provided on: (1) maintenance philosophy, (2) internal functional tests (IFTs), (3) diagnostic control module (DCM), (4) power map procedures, and (5) panel line test. The purpose of Volume I is to help the CE test the 3705-80, locate failing hardware components, and repair and return the controller to the user as quickly as possible. Divider tabs provide quick access to the individual sections.

Volume II (SY27-0209, part 1 of 2) contains an abbreviation list, legend, the composite table of contents, introduction to the 3705-80, a description of the control panel switches and lights and procedures for using them, diagnostic aids, IPL, and the theory-maintenance sections on the central control unit, and storage. A composite index of all three volumes is at the back of each volume.

Volume III (SY27-0209, part 2 of 2) contains an abbreviation list, legend, a volume table of contents, and the theory-maintenance sections on the type 1 channel adapter, the type 2 communication scanner, the line interface base, the line sets, the power system, and the remote program loader (RPL). It also contains information on test tools and equipment, preventive maintenance, and physical locations. A composite index of all volumes is at the back of each volume.

Second Edition (January 1982)

This edition has important changes. Information on the Type 4 Channel Adapter has been added to the manual.

Prerequisite Publication

Introduction to the 3705-80 Communications Controller, GA27-3304.

Related Publications

IBM 3705-80 Communications Controller Principles of Operation, GC30-3074
IBM 3704 and 3705 Communications Controllers Original Equipment Manufacturer's Information, GA27-3053
IBM 3705 Parts Catalog, S131-0077
IBM 3704-05 Program Reference Handbook, GY30-3012
IBM 3705 Advance Communication Functions for NCP, SY30-3029
System/360 Operating System Online Test Executive Program, GC28-5086
DOS OLTEP SRL, GC24-5086
System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturer's Information, GA22-6974
Guide to Using the IBM 3705 Communications Controller Control Panel, GA27-3087

Summary of Changes for SY27-0208-1

This revision contains:

- new pages with type 4 CA information and existing pages with integrated type 4 CA information.
- minor updates to the PWR MAPs section.
- other minor editorial changes and clarifications.

Abbreviations

A	And circuit or ampere
AA	automatic answering
ABAR	attachment buffer address register
ABO	adapter bus out (register)
ac	alternating current
ACO	automatic call originate
ACF/NCP/ VS	Advanced Communications Function for Network Control Program/Virtual Storage
ACR	abandm call and retry
ACU	automatic calling unit
adr	address
AEQ	automatic equalizer
AHR	add halfword register (instruction)
ALD	automated logic diagram
ALU	arithmetic logic unit
AMP	amplifier
APAR	authorized program analysis report
AR	add register (instruction)
ARI	add register immediate (instruction)
B	branch (instruction)
BAL	branch and link (instruction)
BALR	branch and link register (instruction)
BAR	buffer address register
BB	branch on bit (instruction)
BC	bit clock
BCB	bit control block
BCC	bit clock control
BCL	branch on C latch (instruction)
BCT	branch on count (instruction)
BO	bus out
BP	break point
bps	bit per second
BSC	binary synchronous communication
BSM	bridge storage module
BZL	branch on Z latch (instruction)
CA	channel adapter
CACHKR	channel adapter check register
CACR	channel adapter control register
CADB	channel adapter data buffer
CAMR	channel adapter mode register
CASNSR	channel adapter sense register
CASTR	channel adapter status register
CB	circuit breaker
CBAR	CSB buffer address register
CCB	character control block
CCR	compare character register (instruction)
CCT	coupler cut through (modem)
CCU	central control unit
CD	carrier detect
CDS	configuration data set
CE	Channel End (status)
chan	channel
char	character
CHR	compare halfword register (instruction)
ck	check
clk	clock
cm	centimeter
CMDR	channel adapter command register
CMND	command
com	common
COS	Call Originate Status
CP	circuit protector
CPU	central processing unit
CR	compare register (instruction)
CRC	cyclic redundancy check
CRI	compare register immediate (instruction)
CRQ	Call Request
CS	cycle steal
CSAR	cycle steal address register
CSB	communication scanner base
CSCD	clear to send, carrier detect
CSMC	cycle steal message counter
ctrl	control
CTS	Clear To Send
CUE	Control Unit End (status)
CW	control word
CWAR	control word address register
CWCNTR	control word byte count register
DAA	data access arrangement
DA	data modem ready
dB	decibel
DBAR	diagnostic buffer address register
dc	direct current
DCE	data circuit-terminating equipment
DCM	diagnostic control monitor
DCR	data channel ready
DE	Device End (status)
DET	detector
diag	diagnostic
dist	distance
DLO	data line occupied
DOS	Disk Operating System
DPR	digit present
DR	display register or data ring (modem)
DCS	distant station connect (ACO only)
DSR	data set ready
DT	data tip (modem)
DTE	data terminal equipment
DTR	data terminal ready
EC	edge connector
EB	extended buffer
ECP	emulation control program
EIA	Electronic Industries Association
enbl	enable
EON	end of number (ACO only)
EPO	emergency power off
ESC	emulation subchannel
EXT	external
FCS	final control sequence
FET	field effect transistor modem card
FETOM	Field Engineering Theory of Operation Manual
FF	flip flop
FL	flip latch
FRU	field replaceable unit
GB	ground bus
gnd	ground
grp	group
hex	hexadecimal
Hlfwd	halfword
horz	horizontal
HS	heat sink
Hz	Hertz
I	instruction (cycle)
IAR	instruction address register
IC	insert character (instruction)
ICS	initial control sequence
ICT	insert character and count (instruction)
ICW	interface control word
IFT	internal functional test
IN	input (instruction)
INCWAR	inbound control word address register
Init	initial
int	internal
intf	interface
I/O	input/output
IPL	initial program load
IR	interrupt remember
irpt	interrupt
ISACR	initial selection address and command register
L	load (instruction)
LA	load address (instruction)
LAR	lagging address register
LCD	line code definer
LCOR	load character with offset register (instruction)
LCR	load character register (instruction)
LED	light emitting diode
LGF	leading graphics flag
LH	load halfword (instruction)
LHOR	load halfword with offset register (instruction)
LHR	load halfword register (instruction)
LIB	line interface base
lim	limiter
LOR	load with offset register (instruction)
LOSC	last oscillator sample condition
LR	load register (instruction)
LRI	load register immediate (instruction)
LS or ls	local store
lt	latch
L1	level 1
L2	level 2
L3	level 3
L4	level 4
L5	level 5
mA	milliampere
Mem TB	memory terminal board
modem	modulator/demodulator
ms/divn	milliseconds per division
MST	monolithic system technology
mV	millivolt
NB	Digit Signal
N/C	normally closed
NCP	network control program
NCR	and character register (instruction)
NHR	and halfword register (instruction)
N/O	normally open
NR	and register (instruction)
NRI	and register immediate (instruction)
NRZI	non-return-to-zero inverted
ns	nanoseconds
NSC	native subchannel
OBR	outboard recorder
O/C	overcurrent
OCR	or character register (instruction)
OE	exclusive or
OH	off hook (modem)
OHR	or halfword register (instruction)
OLT	on line test
OLTEP	on line test executive program
OLTLIB	on line test library
OLTSEP	on line test standalone executive program
op	operation
op reg	operation register
OR	or register (instruction)
ORI	or register immediate (instruction)
OS	Operating System
OSC	oscillator
OUT	output (instruction)
OUTCWAR	outbound control word address register
OVRN	overrun
O/V	overvoltage
P	parity
PC	parity check
PCF	primary control field
PCI	program controlled interrupt
PDF	parallel data field
PEP	partitioned emulation programming
PG	parity generation
pgm	program
PH	polarity hold
PND	Present Next Digit
P/N	part number
POR	power on reset
pos	position

POSC	present oscillator sample condition
pot	potentiometer
P-P	post processor modem card
PPB	prime power box
PUT	programmable unijunction transistor
PWI	power indicator
R	resistance or resistor
rcv	receive
rd	read
rdy	ready
RE	register and external register (instructions)
ref	reference
reg	register
regen	regenerative
req	request
RI	register immediate (instruction) or ring indicator (modem)
RLSD	receive line signal detector
RMS	root mean square
ROS	read-only storage
RPL	remote program loader
RR	register to register (instructions)
RS	register to storage (instructions)
RSA	register and storage with addition (instructions)
RT	register branch or register and branch (instructions)
RTS	Request To Send
rly	relay
SAR	storage address register
SCF	secondary control field
SCR	silicon controlled rectifier or subtract character register (instruction)
SCRID	silicon controlled rectifier indicator driver
SDF	serial data field
SDLC	synchronous data link control
SDR	storage data register
sec	second
sel	selection
SEP	separator (ACO only)
seq	sequence
SG	signal ground
SH	switch hook (modem)
SHR	subtract halfword register (instruction)
SIG	signal
SIO	start I/O
SMS	standard modular system
SR	subtract register (instruction)
SRI	subtract register immediate (instruction)
SRL	Systems Reference Library
S/S	start/stop
ST	store (instruction)
STC	store character (instruction)
STCT	store character and count (instruction)
STH	store halfword (instruction)
stk	stacked
svc	service
sw	switch
SYN	synchronous idle
sync	synchronization or synchronous
TAR	temporary address register
TB	terminal board
TIC	Transfer In Channel
tr	trigger
TRM	test register under mask (instruction)
TSL	Technical Service Letter
T2	test 2
T3	test 3
T4	test 4
UC	Unit Check (status)
UE	Unit Exception (status)
V	volts
V/divn	volts per division
wd	word
wr	write
XCR	exclusive-or character register (instruction)
xfer	transfer
xfmr	transformer
XHR	exclusive-or halfword register (instruction)
xmt	transmit
XR	exclusive-or register (instruction)
XRI	exclusive-or register immediate (instruction)
2W	two-wire line connection (implies half-duplex)
4W	four-wire line connection (implies duplex, but actual duplex depends on the line set type and telephone company equipment).

Contents

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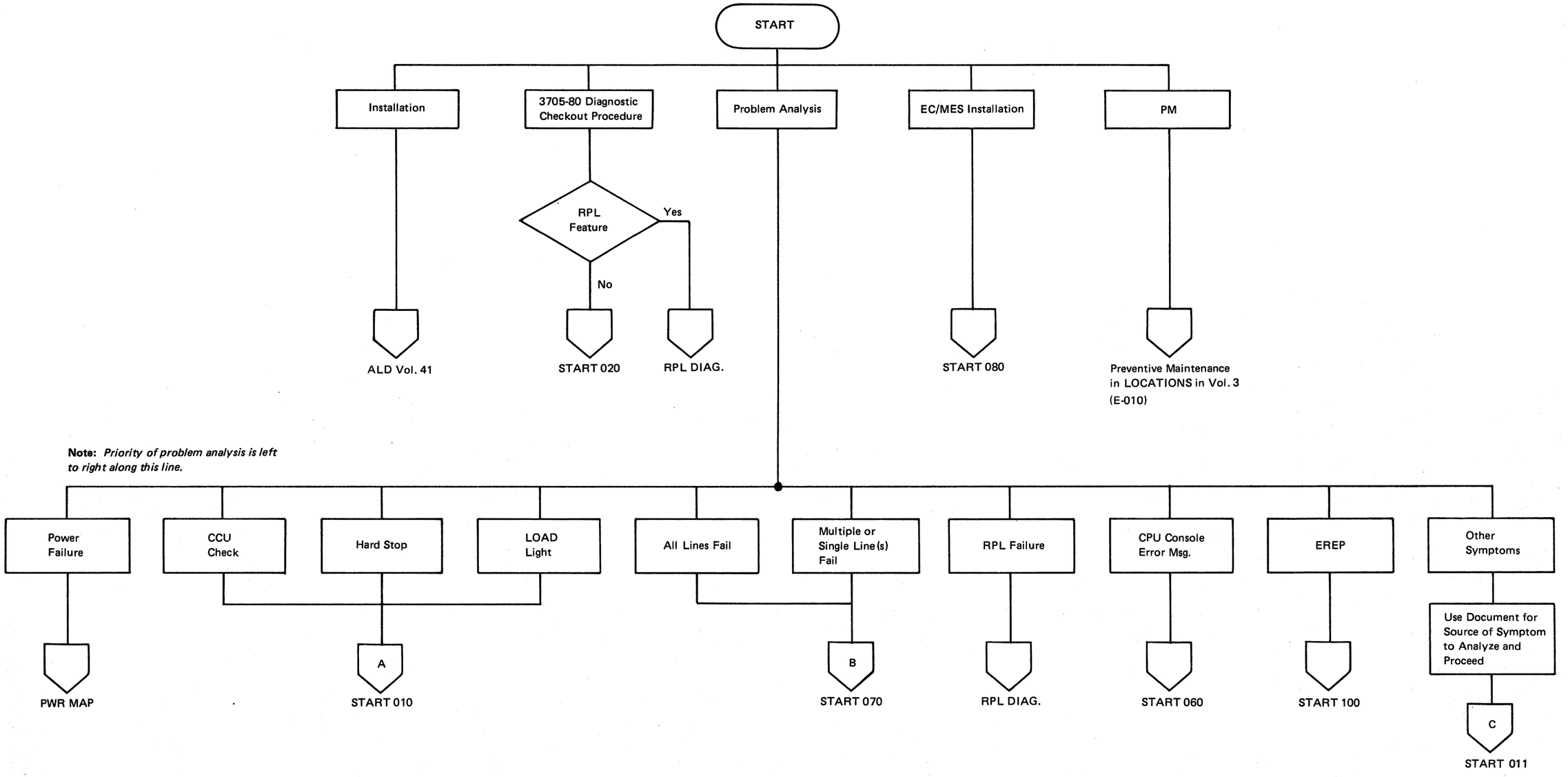

START
Installation
3705-80 Diagnostic Checkout Procedure
Problem Analysis
EC/MES Installation
PM
RPL Feature
Yes
No
ALD Vol. 41
START 020
RPL DIAG.
START 080
Preventive Maintenance in LOCATIONS in Vol. 3 (E-010)
Note: Priority of problem analysis is left to right along this line.
Power Failure
CCU Check
Hard Stop
LOAD Light
All Lines Fail
Multiple or Single Line(s) Fail
RPL Failure
CPU Console Error Msg.
EREP
Other Symptoms
Use Document for Source of Symptom to Analyze and Proceed
A
B
C
PWR MAP
START 010
START 070
RPL DIAG.
START 060
START 100
START 011

CCU/CHECK/HARDSTOP/LOAD LIGHT

From START 005 → A

On Operators Panel:
1. Lamp Test
2. Record CCU status lights DISPLAY A and B
3. Record TAR & OP REGISTER DISPLAY A and B

Execute Input 7D
Record Value
Check for any CCU checks

INPUT X'7D' — CCU CHECK REGISTER

Gen Reg (R)		*Reg/Function (E)*			
BYTE 0,	BIT 0	Byte X Check	BYTE 1,	BIT 0	Cycle Counter Check
	BIT 1	Byte 0 Check		BIT 1	0
	BIT 2	Byte 1 Check		BIT 2	0
	BIT 3	Program Check in Level 1		BIT 3	0
	BIT 4	SAR Check		BIT 4	0
	BIT 5	SDR Check		BIT 5	0 = No CCU Checks; 1-CCU Check(s)
	BIT 6	OP Reg Check		BIT 6	TYPE 2 Attach Base Clock Check
	BIT 7	INDATA Bus Check		BIT 7	CCU Clock Check

Execute Input 7E
Record Value
Check for any CCU Level 1 Interrupts

INPUT X'7E' — CCU LEVEL 1 INTERRUPT REQUESTS

Gen Reg (R)		*Reg/Function (E)*			
BYTE 0,	BIT 0	0	BYTE 1,	BIT 0	Address Compare Interrupt L1
	BIT 1	0		BIT 1	Address Exception (note)
	BIT 2	0		BIT 2	In/Out Check (note)
	BIT 3	0		BIT 3	Protection Check (note)
	BIT 4	0		BIT 4	Invalid Op Check (note)
	BIT 5	0		BIT 5	0
	BIT 6	0		BIT 6	IPL L1
	BIT 7	0		BIT 7	0

Note: Prog Check

Execute Input 76
Record Value
Check for any Adapter Level 1 Interrupts

INPUT X'76' — ADAPTER LEVEL 1 INTERRUPT REQUESTS

Gen Reg (R)		*Reg/Function (E)*			
BYTE 0,	BIT 0	Type 4 CA L1	BYTE 1,	BIT 0	0
	BIT 1	Type 2 Scan-1 L1		BIT 1	0
	BIT 2	0		BIT 2	0
	BIT 3	0		BIT 3	0
	BIT 4	0		BIT 4	0
	BIT 5	Type 1 CA, or Selected Type 4 CA L1		BIT 5	0
	BIT 6	0		BIT 6	0
	BIT 7	Remote Program Loader L1 Request		BIT 7	0

1 →

1 →

Execute Input 74
Record LAR

INPUT X'74' — LAGGING ADDRESS REGISTER (LAR)

Gen Reg (R)		*Reg/Function (E)*				
BYTE X,	BIT 4	LAR BYTE X,	BIT 4 }	with 20-bit EA only		
	BIT 5		BIT 5 }			
	BIT 6		BIT 6 }	with 18 or 20-bit EA		
	BIT 7		BIT 7 }			
BYTE 0,	BIT 0	LAR BYTE 0,	BIT 0	BYTE 1,	BIT 0	LAR BYTE 1, BIT 0
	BIT 1		BIT 1		BIT 1	BIT 1
	BIT 2		BIT 2		BIT 2	BIT 2
	BIT 3		BIT 3		BIT 3	BIT 3
	BIT 4		BIT 4		BIT 4	BIT 4
	BIT 5		BIT 5		BIT 5	BIT 5
	BIT 6		BIT 6		BIT 6	BIT 6
	BIT 7		BIT 7		BIT 7	BIT 7

EA = Extended Addressing

Execute Input 79
Record Value
Check for Program Level Interrupted

INPUT X'79' — UTILITY

Gen Reg (R)		*Reg/Function (E)*			
BYTE 0	BIT 0	0	BYTE 1,	BIT 0	Program Level 2 Interrupted (note)
	BIT 1	0		BIT 1	Prog Level 3 Interrupted (note)
	BIT 2	0		BIT 2	Prog Level 4 Interrupted (note)
	BIT 3	0		BIT 3	Prog Level 5 Interrupted (note)
	BIT 4	0		BIT 4	FET memory
	BIT 5	0		BIT 5	0
	BIT 6	Prog Level 5 C Condition		BIT 6	Type 1 or 4 CA installed
	BIT 7	Prog Level 5 Z Condition		BIT 7	IPL Escape Control

Note: This bit=0 if not Level 1 or if entered immediately after exiting Level 1.

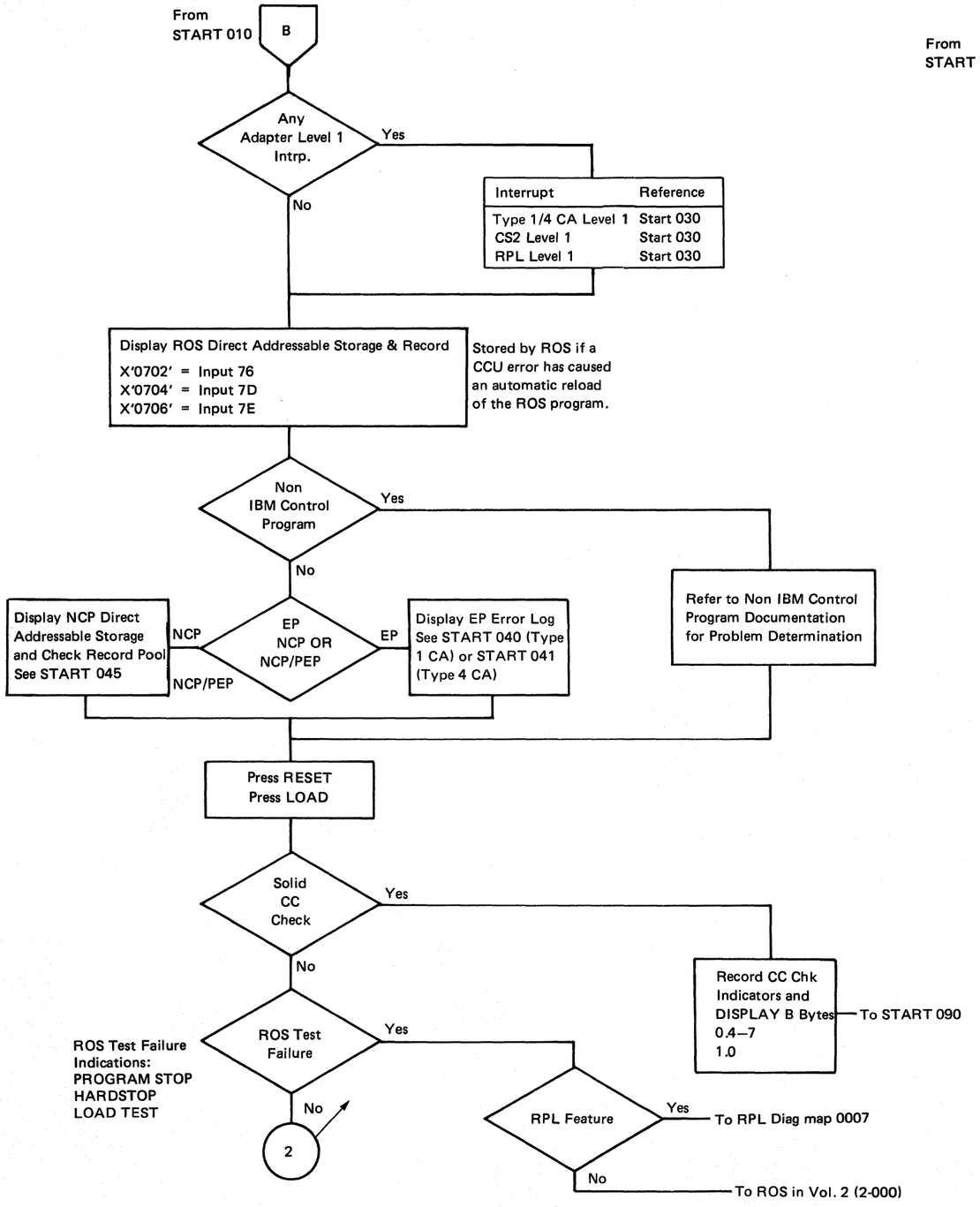
Execute Input 77
Record Value
Check for and Record Level 2 and 3 Interrupts

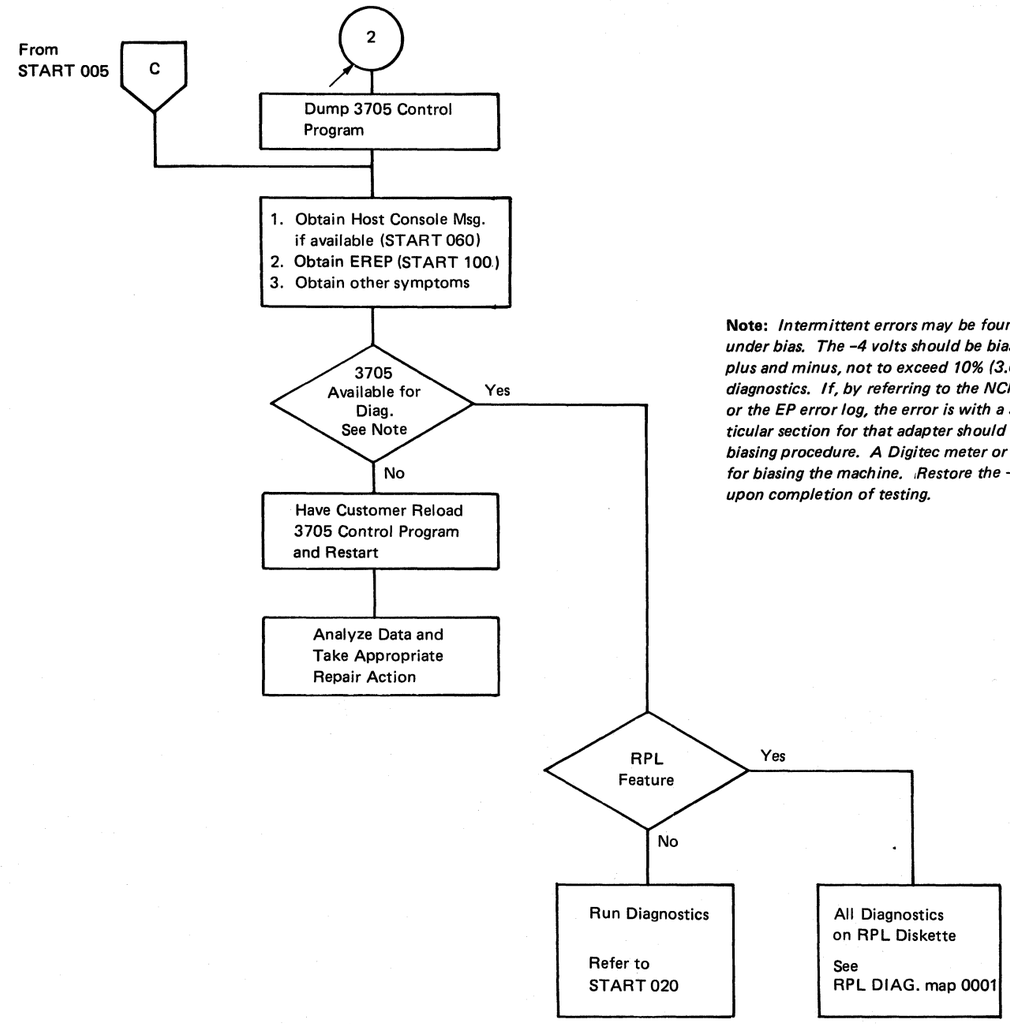
INPUT '77' — ADAPTER LEVEL 2 or 3 INTERRUPT REQUESTS (See Note 1)

Gen Reg (R)		*Reg/Function (E)*			
BYTE 0,	BIT 0	0	BYTE 1,	BIT 0	Type 4 CA L3
	BIT 1	Type 2 Scan L2		BIT 1	Remote Program Loader L3 Request
	BIT 2	0		BIT 2	0
	BIT 3	0		BIT 3	Type 1 or Selected Type 4 CA Data/Status L3
	BIT 4	0		BIT 4	Type 1 CA-1 or Selected Type 4 CA L3
	BIT 5	0		BIT 5 }	Type 4 CA Selected
	BIT 6	0		BIT 6 }	
	BIT 7	0		BIT 7	0

Note 1: *Executing this instruction following an Output X'67 instruction in which all bits=0 automatically selects the Type 4 CA having highest L3 priority.*

B → START 011





Note: *Intermittent errors may be found by running diagnostics under bias. The -4 volts should be biased in increments of .1 volts plus and minus, not to exceed 10% (3.6–4.4), while running all diagnostics. If, by referring to the NCP check record pool (CRP), or the EP error log, the error is with a specific adapter, the particular section for that adapter should be looped using the above biasing procedure. A Digitec meter or equivalent should be used for biasing the machine. Restore the -4 volts to its proper setting upon completion of testing.*

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3705-80 CHECKOUT PROCEDURE

The 3705 is tested by:

1. ROS Test: Started when LOAD key is pressed.
2. Panel Test: Manual operations performed by the Customer Engineer.
3. OLT Diagnostics: Started by the Customer Engineer.

ROS Test

Initiated when the LOAD key is pressed (local and RPL). Provides the following functions:

IPL Phase 1	-	General reset.
IPL Phase 2	-	ROS code loads into storage beginning at location X'0000'.
IPL Phase 3	-	Checks function and instructions required to complete the IPL.

Note: Remote IPL phase 3 also tests the diskette controller data path.

Refer to the ROS section in Volume 2 for detailed operating procedure.

Panel Test

Tests, via the control panel, the basic control and CCU data flow necessary to load ROS.

Refer to the CTRL PNL section in Volume 2 for detailed operating procedure.

Note: 3705 must be available to run diagnostics. That is, the customer cannot run the 3705 while the diagnostics are in process.

Channel Adapter 1 or 4 OLTS 3705 AA-AI

Tests the common channel adapter controls and interface and performs a data wrap from the NSC to the ESC.

Run procedure:

At 3705	-	Enable channel interface Press the RESET and LOAD switches
At Host	-	Start OLTEP or OLTSEP Enter- NSC,ESC/3705AA-AI/NFE/

Refer to the CA OLT section for detailed operating procedure.

Initial Test (INIT)

Provides basic functional testing of some registers and storage. Tests the instruction set in each of the 5 program levels.

At the 3705:

1. Switch the 3705 power on.
2. Set both the MODE SELECT and DIAGNOSTIC CONTROL switches to the PROCESS position.
3. Enable the appropriate channel interface.
4. To load the DCM, set the DISPLAY/FUNCTION SELECT switch to the STATUS position. For information on using the other positions, see "How to Use the DISPLAY/FUNCTION SELECT Switch" in the DCM section.
5. Press the RESET pushbutton, then the LOAD pushbutton.
6. DISPLAY B bits 0.2 and 0.3 should be on indicating that ROS has reached IPL phase 3. The LOAD light is on; the following lights are off: HARD STOP, TEST, WAIT, and PROGRAM STOP.

If the above conditions are not present, refer to the CE Panel Test in the CNTL PNL section and the ROS Test in the ROS test section (Volume 2).

At the Host:

Start the OLTEP or OLTSEP in the host processor. When OLTEP or OLTSEP causes a console printer message of:

r ID 'ENTER DEV/TEST/OPT/'

you enter:

r ID,'xxx,yyy/3705A/nfe,ext=ABCD/'

where:

XXX = the channel address of the 3705 (native subchannel address (NSC))

yyy = an emulation subchannel address (ESC)

ABCD = four operating options provided by the OLT and type 1 CA loaders. The correct entries are Y (for YES) or N (for NO). The options are defined as follows:

- A = OLT bypass printing channel errors
- B = Run Initial Test (INIT)
- C = Run type 1 CA loader with error checking
- D = Bypass hard stop on type 1 CA loader error in 3705 and retry

For failure indicators and how to use the INIT symptom index see INIT 30.

Refer to INIT section or the RPL OP section (Volume 3) for detailed operating procedures.

Diagnostic Control Monitor - (DCM)

The DCM provides functions for requesting, loading and controlling the internal functional tests (IFTS), displaying error information, and setting up scope loops.

Load Procedure (3705-80 With Channel Adapter)

At the 3705:

1. Switch the 3705 power on.
2. Set both the MODE SELECT and DIAGNOSTIC CONTROL switches to the PROCESS position.
3. Enable the appropriate channel interface.
4. Set the DISPLAY/FUNCTION SELECT switch to the STATUS position to load the DCM. For information on using the other positions, see "How to Use the DISPLAY/FUNCTION SELECT Switch" in the DCM section.
5. Press the RESET pushbutton, then the LOAD pushbutton.
6. DISPLAY B bits 0.2 and 0.3 should be on indicating that ROS has reached IPL phase 3. The LOAD light is on; the following lights are off: HARD STOP, TEST, WAIT and PROGRAM STOP.

If the above conditions are not present, refer to the CE Panel Test in the CP section and the ROS Test in the ROS Test section.

At the Host:

Start the OLTEP or OLTSEP in the host processor. When OLTEP or OLTSEP causes a console printer message of:

r ID 'ENTER DEV/TEST/OPT/'

you enter:

r ID,'XXX/3705A/nfe,ext=ABCD/'

where:

XXX = the channel address of the 3705 (native subchannel address (NSC))

ABCD = four operating options provided by the OLT and type 1 CA loaders. The correct entries are Y (for YES) or N (for NO). The options are defined as follows:

- A = OLT bypass printing channel errors
- B = Run Initial Test (INIT)
- C = Run type 1 CA loader with error checking
- D = Bypass hard stop on type 1 CA loader error in 3705 and retry

For example, if you enter:

r ID,'007/3705A/EXT=NYNN/'

Test T3705A to address 007 with Initial Test (INIT) requested is invoked.

Load Procedure (3705-80 with RPL feature)

1. Place the Initial Test/IFT diskette in the 3705-80 reader.
2. Set the DISPLAY/FUNCTION SELECT switch to the STORAGE ADDRESS positior
3. Set STORAGE ADDRESS/REGISTER DATA switches A-E to 0DDDD.
4. Set the channel enable/disable switch to disable.
5. Press RESET, LOAD then INTERRUPT.
6. Initial Test will load (it cannot be optioned out) and step through the 5 program levels (1-5) back to level 1 and then load the Diagnostic Control Monitor (DCM).
7. DCM loaded - DISPLAY A = FFFF, DISPLAY B = FFFF. HARD STOP and PROGRAM DISPLAY lights on.

Follow Initial Test run procedure (RPL Feature).

Summary of DISPLAY/FUNCTION SELECT Switches and CE Sense Switches

The DISPLAY/FUNCTION SELECT switch is tested by the DCM when the INTERRUPT pushbutton is pressed and every time the START pushbutton is pressed after a stop code is displayed. The following summarizes the functions that can be selected (a dash indicates that the switch is not used):

DISPLAY/FUNCTION SELECT Position	ADDRESS/DATA switches A B C D E	FUNCTION
STORAGE ADDRESS	Y Y Y Y Y	Display location YYYYY
REGISTER ADDRESS	- R - R -	Display register RR
FUNCTION 1	- 0 - - -	Refresh last DCM display
	- 1 - - -	Stop panel utilities
	- 2 - - -	Set up continuous display without test
	- 3 - - -	Set up continuous display with test
	- 4 - - -	Set up address compare display without test
	- 5 - - -	Set up address compare display with test
	- 6 - H H	Set repeat count to HH
	- 7 - - -	Display repeat count
	- 9 S M M	Set CE sense switches
	A S M M	Reset sense switches
	A S 0 0	Display CE sense switches (S=0 for byte 0 of switches; S=1 for byte 1 of switches; MM=selected bits to set or reset.)
	- D X X X	Dynamic communications to routines
FUNCTION 2	X X X X X	Display storage contents at XXXXX.
FUNCTION 3	- R - R -	Display register contents of register RR
FUNCTION 4	- P I R R	Part 1 of request
	- M M M M	Part 2 of request P=Adapter Number I=IFT Number R=Routine Number MMMM=CE sense switches
	- F 0 X X	Terminate T3705A Loader at host.
FUNCTION 5	V W X Y Z	Continue from the error stop or manual intervention stop. (If it is an error stop, VWXYZ is not used. If it is a manual intervention stop, VWXYZ is used by the routine as specified in the symptom index.)
FUNCTION 6	- F F F F F - - - - -	Abort total request Abort current routine
FUNCTION 1,2,3		Panel utility display positions
FUNCTION 4,5,6		DCM displays routine codes. Stop codes are displayed when the switch is set to one of the FUNCTION positions (1 to 6).

CE Sense Switch	ADDRESS/DATA Switches B C D E
Problem Definition Mode	1
Restart Routine on First Error	2
Loop on First Error	4
Bypass Error Stop	8
Cycle on Request	1
Include Manual Intervention Routines	2
Repeat Each Routine X Times	4
Halt Before Execution	8
Bypass New Error Stops	1
Wait Before Continuing	8

Note: To loop on an IFT error requires combined CE Sense Switch settings. To restart routine on first error or to loop on firs error, the bypass error stop sense switch must also be set.

Example: Set STORAGE ADDRESS/REGISTER DATA switch E to:

A - To restart routine on first error or

C - To loop routine on first error.

Scope Sync Points

+ Sync Point 1	-	01A-B3M2P10 (ALD page CU015) Beginning of each routine on the hardware setup block when the DCM is in a scoping loop.
+ Sync Point 2	-	01A-B3M2P13 (ALD page CU004)
+ Address Compare	-	01A-B3P2S09 (ALD page CU004). Use to sync on the test function of a test routine. Storage address compare to STORAGE ADDRESS/REGISTER DATA switches.

DCM Symptom Index

The DCM symptom index is located at the back of the DCM section. Operator codes are identified by either DISPLAY A = X''0000' or X'FFFF'.

See the DCM section for detailed information.

Internal Function Tests (IFTs)

IFTs are a set of diagnostic programs, under the control of the DCM, that are designed to aid in detecting 3705 hardware failures. The IFTs available for the 3705-80 are:

CCU
Storage
Type 1 or 4 Channel Adapter
Type 2 Communication Scanner

Run Procedure (all routines of all IFTs on all adapters)

1. DCM must be loaded in the 3705 and ready for part 1 of an IFT request. DISPLAY A and B = X'FFFF'. HARD STOP and PROGRAM DISPLAY lights are on (see DCM load procedure).
2. Host message: ENTER IFT REQUEST AT 3705.
3. Set DISPLAY/FUNCTION SELECT switch to FUNCTION 4.
4. Set STORAGE ADDRESS/REGISTER DATA switches to X'0000' and press START. DISPLAY B should be X'8002' with the HARD STOP and PROGRAM DISPLAY lights on.
5. Press START again. All tests will run on all adapters.
6. Host message: WAITING FOR IFT COMPLETION. Successful completion of the IFTs is indicated as follows: DISPLAY A = X'FFFF', DISPLAY B = X'80F0', HARD STOP and PROGRAM DISPLAY lights on.
7. To terminate testing, set X'F0XX in STORAGE ADDRESS/REGISTER DATA switches and press START.

Note: RPL Feature IFTs are on the RPL Diskette.

Error Indications and Symptom Index

1. PROGRAM DISPLAY, TEST and HARD STOP lights on.
2. Symptom index display format:

   DISPLAY A = PIRR

   DISPLAY B = TSKK

   Where:

   P = Number (ID) of adapter being tested.

   I = Number (ID) of active IFT.

   RR= Number (ID) of active routine.

   T = Type of display code.

   S = Scoping indicator and error counter.

   KK= Code reference to symptom index.
3. Symptom index for IFTs are in the back of the IFT section.

For failure indications and how to use he IFT symptom index, see IFT 012.

Manual Intervention Routines

Manual intervention routines test single bit storage errors, storage protect key, usage meter, storage, and type 2 communication scanner. The symptom index is at the back of the IFT section (IFT CSB 800).

See the IFT section for detailed operating procedures.

Panel Line Test (T3705L)

This test is a standalone version of the NCP-4 line test function and can be used when neither NCP or EP is available to test the communication line using the 3705-80 control panel.

The test requires a dedicated 3705. The customer cannot run the 3705 while the diagnostics are in progress.
The test can be loaded with the type 1 channel adapter, the type 4 channel adapter, or the RPL diskette.

CDS requirements:

RPL - No CDS is required.
CA1 - Only channel data is required.
CA4 - Only channel data is required.
(See the CDS section.)

Run procedure:

See the PNL LN section for operating procedures.

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CHANNEL ADAPTER TYPE 1 or 4 (INPUT 67)

Level 1 Interrupt Request

Execute Input 67
Record Value
Check for Any Errors:

The Input X'67' transfers the error condition register and the hardware address of the NSC channel interface address to the CCU.

Summary of Inbus bits during input X'67':

Bit	*Card Loc.*	*Logic Page*	*Function*
0.0-0.7	A4P2	RC104	NSC hardware address intf A
0.0-0.7	A4P2	RC017	NCS hardware address intf B
1.0	A4Q2	RC707	Chan bus in error
1.1	A4K2	RC507	Invalid I/O Op
1.2	A4K2	RC507	CCU outbus check
1.3	A4K2	RC507	Local store parity check
1.4	A4K2	RC504	CA enabled
1.5	A4K2	RC504	NSC address active
1.6	—	—	00 = Type 4 CA #1 selected
1.7	—	—	01 = Type 4 CA #2 selected

BYTE 1.0 Channel Bus In Check — Incorrect parity detected on channel bus in. Hardware generates good parity and causes L1 interrupt.

1.1 In/Out Instruction Accept Check — Indicates that control program executed an input or output X'60' through '66' instruction when CA1 was handling a data or status transfer.

1.2 CCU Outbus Check — The CA hardware detected incorrect parity on CCU outbus.

1.3 Local Store Check — The CA hardware detected incorrect parity on data bytes gated out of local storage. The control program should place good parity in LS by executing an output '63-65' instruction.

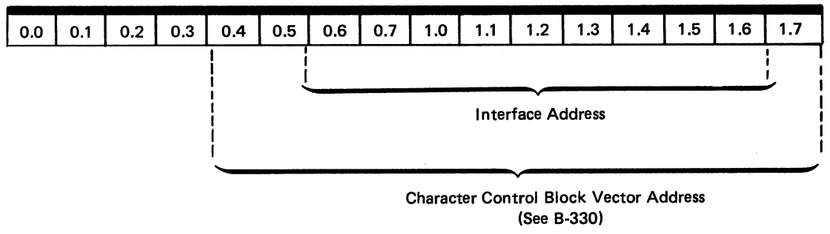
1.4 Channel Interface Enabled — Indicates either Inf A or B is enabled.

1.5 NSC Address Active — Indicates that the NSC has been selected and is active. Bit is reset when host accepts final status.

COMMUNICATION SCANNER TYPE 2 (INPUT 40 AND 43)

Execute Input 40

Record Interface Address:



Execute Input 43
Record Value
Check for any Errors:

General Register (R)	*Check Register Position*	*Cause of Check*	*Reference*
0.0	LIB A BCC Check	Set to 1 if the scanner detects a LIB A BCC local store parity error during a bit clock selection.	C-020 C-120
0.1	LIB B BCC Check	Same as above for LIB position B.	
0.6	LIB Select Clock	Set to 1 if more than one LIB was selected, or more than one line was accessed on the selected LIB, or no line was accessed on the selected LIB, or a line was accessed on a LIB that was not selected.	
0.7	ICW Input Reg Check	Set to 1 if the scanner detects a parity error (odd) in the ICW input register (46 + 2P).	B-020
1.0	ICW Work Reg Check	Set to 1 if the scanner detects a parity error (odd) in the ICW work register (46 + 2P).	B-020
1.1	Priority Reg Avail Check	Set to 1 if the scanner detects a parity error (even) in the priority register available lines (4 + P).	B-020
1.2	CCU Outbus Check	Set to 1 if the scanner detects a parity error (even) on the Outbus (16 + 2P).	B-020, B-170
1.3	Line Adr Bus Check	The line adr bus parity is used to predict the parity of the address as modified by the scanner's upper scan limits. If this predicted parity does not compare with the actual parity of the modified address, the scanner sets this bit to 1.	B-020 B-(180-210)

REMOTE PROGRAM LOADER (INPUT 68)

Execute Input 68
Record Value
Check for any Errors:

INPUT X'68' — REMOTE PROGRAM LOADER LEVEL 1 STATUS

Gen Reg (R)		*Reg/Function (E)*
BYTE 0	BIT 0	*
	BIT 1	Outbus Parity Error
	BIT 2	*
	BIT 3	*
	BIT 4	*
	BIT 5	*
	BIT 6	*
	BIT 7	*
BYTE 1	BIT 0	*
	BIT 1	*
	BIT 2	*
	BIT 3	Write Command Issued When Write Not Enabled
	BIT 4	*
	BIT 5	*
	BIT 6	*
	BIT 7	*

Error Recording

Recoverable and nonrecoverable errors are recorded in 3705 storage. The Emulation Program can log up to 15 halfword error indications. The log entry identifies the type of error (program check level 4, scanner check, etc.) and the hardware unit affected. Entries are made on a wrap-around basis with the most recent events being retained and each entry beyond the recording limit overlaying the oldest entry.

Register Save Area and Log Table

The level 1 interrupt handler uses two segments of the fullword direct addressable area.

1. Fullwords from address X'07A0' up to but not including X'07DE' are used to store the group 0 general registers.
2. Fullwords from address X'07E0' up to but not including X'0800' are used for the 16 halfword log table. This table contains the various one or two halfword error messages accumulated during processing. One entry is made for hardware errors and two entries are made for program errors.

Log Table Format: A halfword at address X'07DE' contains the address of the last entry made in the table. If there have been no entries in the table, X'07DE' contains X'07DE'. After the halfwords are all used, the logging process wraps to the beginning of the table and overlays the first entry or entries, beginning at X'07E0', with the entry or entries for the next level 1 interrupt and so on.

The two hardstop conditions (program check and channel adapter check) have two entries in the log table:

1. The log message. This entry contains the exact cause for failure, the interrupt level and an identifier.
2. The contents of the lagging address register (LAR).

The Log Message: The halfword log message may contain two or three segments of information, depending on the type of error.

In the case of a program check or channel adapter check, three segments are used.

1. The high-order byte contains the cause of the check.
2. The last four bits of the low-order byte contain the interrupt level at which the error occurred.
3. The four remaining bits contain an identifier. For a program check the identifier is zero, and for a channel adapter check it is one.

The scanner checks have only two types of information in the log message.

1. The cause of the check, which is located in the 12 high-order bits.
2. The identifier, which is located in the four low-order bits.

The recorded events may be inspected by using the dump program or by displaying the entries on the 3705 control panel. The dump must be made prior to re-IPL, or the error log table and the register save area are lost, and the information in them is meaningless.

Error Log Format

Byte 0	*Byte 1*	*Byte 2*	*Byte 3*	*Error Type*
x x	x 0	LAR *		Program Check
x x	x 1	LAR *		Chann Adapt Chk.
x x	x 3	Not Used		Type 2CS Chk.

* See LAR Contents

I.D. Bits

Error Type: Program Check (IN X'7E')

	Byte 0	*Byte 1*	
Bit 0	Address Compare	Level 2	
Bit 1	Address Exception	Level 3	
Bit 2	In/Out	Level 4	
Bit 3	Storage Protection	Level 5	
Bit 4	Invalid Op	ID Bit = 0	0
Bit 5	Zero	ID Bit = 0	
Bit 6	Zero	ID Bit = 0	
Bit 7	Zero	ID Bit = 0	

Bytes 2 and 3 contain the contents of the LAR.

Error Type: Channel Adapter Check (IN X'67')

	Byte 0	*Byte 1*	
Bit 0	Channel Bus in Parity	Level 2	
Bit 1	I/O Instr. Exception	Level 3	
Bit 2	CCU Outbus Parity	Level 4	
Bit 3	Local Store Parity	Level 5	
Bit 4	Zero	ID Bit = 0	1
Bit 5	Zero	ID Bit = 0	
Bit 6	Zero	ID Bit = 0	
Bit 7	Zero	ID Bit = 1	

Bytes 2 and 3 contain the contents of the LAR.

Error Type: Type 2 Scanner (1) Check (IN X'43')

	Byte 0	*Byte 1*	
Bit 0	LIB A	ICW Work Register	
Bit 1	LIB B	Priority Register	
Bit 2	Zero	CCU Outbus Parity	
Bit 3	Zero	Line Address Bus	
Bit 4	Zero	ID Bit = 0	
Bit 5	Zero	ID Bit = 0	
Bit 6	LIB Select	ID Bit = 1	3
Bit 7	ICW IN Register	ID Bit = 1	

CONDITION	*LAR CONTENTS*
Invalid Op Code Check	Address of last instruction executed before the one that caused the check (see note)
Protection Check or Address Exception Check	Address of last instruction executed before the one that caused the check (see note) -or- Address of the instruction that caused the check
In/Out Check at Level 2, 3, or 4	Address of the input or output instruction that caused the check
In/Out Check at Level 5	Address of last instruction executed before the one that caused the check (see note)
IPL (including CCU check)	Address of last instruction executed before IPL phase 1
Adapter Check	Unpredictable
— Control Panel Operations —	
LOAD ADDRESS COMPARE, PROGRAM STOP or INTERRUPT	Address of last instruction executed before the one whose address is set in switches A to E (3705) (see note)
LOAD or STORE, ADDRESS COMPARE, PROGRAM STOP or INTERRUPT	Address of instruction that was loaded from or stored into the location set in switches A to E (3705)
INSTRUCTION STEP	Address of last instruction executed
STOP Push Button	Address of last instruction executed

Note: *The last instruction may have been an Exit instruction executing at a higher priority program level than the level executing at the time the condition occurred. Therefore, LAR contains the address of that Exit instruction.*

ERROR LOG EXAMPLE:

```
007C0    B8400022  00000000  00000000  00000000  00000000  00000000  00000000  000007E6
007E0    40030023  404003E8  00000000  00000000  00000000  00000000  00000000  00000000
00800    00000000  00000000  00000000  00000000  00000000  00000000  00000000  00000000
```

Using the above listing of storage extracted from a 3705 storage dump, note that address X'07DE' contains X'07E6' which means the last entry was made into address X'07E6'. This means that the oldest entry is located at X'07E8', but since that location is all zeroes the table hasn't wrapped around yet, so the oldest entry is at location X'07E0'. In the first entry (X'4003), the I.D. field is B'0011' so this entry is for a type 2 scanner check. Byte 0, bit 1 being on indicates a LIB B BCC check occurred. The second entry (X'0023') indicates a CCU OUTBUS parity check occurred on the TYPE 2CS. The third and last entry is a program check entry and is therefore two halfwords long. This entry (X'404003E8') indicates an address exception check occurred in program level 3 and the contents of LAR was X'03E8'.

TYPE 4 CHANNEL ADAPTER

Error Recording

Recoverable and nonrecoverable errors are recorded in 3705 storage. The emulation program can log up to 16 halfword error indicators. The log entry identifies the type of error (program check level 4, scanner check, etc.) and the hardware unit affected. Entries are made on a wrap-around basis with the most recent events being retained and each entry beyond the recording limit overlaying the oldest entry.

Register Save Area and Log Table

The level 1 interrupt handler uses two segments of the direct addressable areas.

1. Fullword addresses X'07A0' up to but not including X'07C4' are used to store the group 0 general registers.
2. The halfword at X'071C' contains the address of the log table pointer (LOGPOINT), followed immediately by the 16 halfword log table (LOGITEMS). These 17 halfwords are located in the CYESVC module.

Log Table Format: LOGPOINT contains the address of the last entry made in the table. If there have been no entries in the table, LOGPOINT contains its own address. After the 16 halfwords are all used, the logging process wraps to the beginning of the table and overlays the first entry or entries, beginning at LOGITEMS, with the entry or entries for the next level 1 interrupt and so on.

The recorded events may be inspected by using the Dump program or by displaying the entries on the 3705 control panel. The Dump must be made prior to re-IPL, or the error log table and the register save area are lost, and the information in them is meaningless.

BYTE 0	BYTE 1	BYTE 2	BYTE 3	ERROR TYPE
x x	x 0	* LAR		LEVEL 1 CCU ERROR
x x	x 1	* LAR		LEVEL 1 CHAN. ADAPT. CHECK
x x	x 3	* LAR NOTE 1		LEVEL 1 TYPE 2 SCANNER CHECK
x x	x 7	NOT USED		LEVEL 3 ERROR

* SEE LAR CONTENTS
NOTE 1. - APPEARS ONLY IF AN OUTBUS CHK OCCURS.

The Log Message: The halfword log message may contain one, two, or three halfwords of information, depending on the type of error.

The four low-order bits of the first halfword indicate the type of error as follows:

1. X'0' Level 1 CCU error
2. X'1' Level 1 channel adapter check
3. X'3' Level 1 scanner check
4. X'7' Level 3 error

1. Level 1 CCU error, first halfword:

   Byte 0
   - Bit 0 not used
   - Bit 1 address exception
   - Bit 2 IN/OUT check
   - Bit 3 protection check
   - Bit 4 invalid OP check
   - Bits 5-6 not used
   - Bit 7 ALC support error

   Byte 1
   - Bit 0 program level 2 interrupted
   - Bit 1 program level 3 interrupted
   - Bit 2 program level 4 interrupted
   - Bit 3 program level 5 interrupted
   - Bits 4-7 X'0'

   Level 1 CCU error, second halfword:

   Bytes 0 and 1: lagging address register

2. Level 1 channel adapter check, first halfword:

   Byte 0
   - Bit 0 channel bus-in check
   - Bit 1 IN/OUT instruction accept check
   - Bit 2 CCU out bus check
   - Bit 3 local store check
   - Bit 4 channel interface enabled
   - Bit 5 native subchannel address active
   - Bit 7 0 = #1 type 4 channel adapter selected; 1 = #2 type 4 channel adapter selected

   Byte 1
   - Bit 0 program level 2 interrupted
   - Bit 1 program level 3 interrupted
   - Bit 2 program level 4 interrupted
   - Bit 3 program level 5 interrupted
   - Bits 4-7 X'1'

   Level 1 channel adapter check, second halfword:

   Bytes 0 and 1: lagging address register

3. Level 1 type 2 scanner check, first halfword:

   Byte 0
   - Bit 0 LIB position A bit clock check
   - Bit 1 LIB position B bit clock check
   - Bit 2 not used
   - Bit 3 not used
   - Bit 4 not used
   - Bit 5 not used
   - Bit 6 LIB select check
   - Bit 7 ICW input register check

   Byte 1
   - Bit 0 ICW work register 1 check
   - Bit 1 priority register available check
   - Bit 2 CCU outbus check
   - Bit 3 line address bus check
   - Bits 4-7 X'3'

   Level 1 type 2 scanner check, second halfword (appears only if an outbus check occurs)

   Bytes 0 and 1: lagging address register

4. Level 3 initial select where INPUT X'60', byte 0 is zero, first halfword: X'0047'

   Level 3 interrupt for a channel adapter that is not sysgened, first halfword: X'0147'

Note: *When a hard stop occurs, all 18 bits of the LAR are saved in storage at label SAVELAR in the CYENUC module.*

CONDITION	*LAR CONTENTS*
Invalid Op Code Check	Address of last instruction executed before the one that caused the check (see note)
Protection Check or Address Exception Check	Address of last instruction executed before the one that caused the check (see note) -or- Address of the instruction that caused the check
In/Out Check at Level 2, 3, or 4	Address of the input or output instruction that caused the check
In/Out Check at Level 5	Address of last instruction executed before the one that caused the check (see note)
IPL (including CCU check)	Address of last instruction executed before IPL phase 1
Adapter Check	Unpredictable
— Control Panel Operations —	
LOAD ADDRESS COMPARE, PROGRAM STOP or INTERRUPT	Address of last instruction executed before the one whose address is set in switches A to E (3705) (see note)
LOAD or STORE, ADDRESS COMPARE, PROGRAM STOP or INTERRUPT	Address of instruction that was loaded from or stored into the location set in switches A to E (3705)
INSTRUCTION STEP	Address of last instruction executed
STOP Push Button	Address of last instruction executed

Note: *The last instruction may have been an Exit instruction executing at a higher priority program level than the level executing at the time the condition occurred. Therefore, LAR contains the address of that Exit instruction.*

ERROR LOG EXAMPLE:

```
00700   XXXXXXXX  XXXXXXXX  XXXXXXXX  XXXXXXXX  00000000  00000000  00000000  7F0E0000
07F00   00000000  00000000  00000000  00007F16  40030023  404003E8  00000000  00000000
07F20   00000000  00000000  00000000  00000000
```

Using the above listing of storage extracted from a 3705 storage dump, note that address X'071C' contains X'7F0E', which is the address of the log table pointer. X'7F0E' contains X'7F16' which means the last entry was made into address X'7F16'. This means that the oldest entry is located at X'7F18', but since that location is all zeroes, the table has not wrapped around yet, so the oldest entry is at location X'7F10'. In the first entry (X'4003), the I.D. field is B'0011' so this entry is for a type 2 scanner check. Byte 0, bit 1 being on indicates a LIB B BCC check occurred. The second entry (X'0023') indicates a CCU OUTBUS parity check occurred on the TYPE 2CS. The third and last entry is a program check entry and is therefore two halfwords long. This entry (X'404003E8') indicates an address exception check occurred in program level 3 and the contents of LAR was X'03E8'.

NCP DIRECT ADDRESSABLE STORAGE

Display and Record:

X'0760' = ABEND Code. Posted by Supervisor for an error which causes an ABEND. Refer to START 051 for ABEND codes.

X'07BC' = Input 74 (LAR). Stored if ABEND is detected in level 1. (See START 040.)

X'0688' = Input 79 (Byte 1). Stored if ABEND is detected in level 1.

X'06B7' = Communication Scanner #1 Mask for LIB disable functions

Note: Mask = 'FF' if scanner is disabled.

NCP CHECK RECORD POOL

The NCP builds some MDR's to be sent to the host in an area in storage called the Check Record Pool (CRP). When a channel adapter failure or a NCP ABEND prevents transferring the MDR to the host, the check information must be obtained from the entry in the CRP. The CRP can contain three level 1 records and three level 3 records.

To locate CRP:

1. Display fullword (xxxx xxxx) at X'07D8' (pointer to HWE)
2. Add 6 to the fullword at X'07D8' (xxxx xxxx + 6 = yyyy yyyy)
3. Display the halfword (zzzz) at yyyy yyyy. This is the CRP pointer.

Example: Assume that NCP has abended with an ABEND code of X'0503', a non-recoverable channel adapter check occurred. To find what the error was, you must find the MDR. First you must find the CRP.

1. Assume the contents of X'07D8' is X'00018384'.
2. X'18384'+6=X'1838A'.
3. Assume the contents of X'1838A' is X'BBA8'.
4. Therefore the address of the CRP is X'BBA8'.

Storage starting at X'BBA8' is:

BC1ABC00 BBB2BBB2 80000400

This is the CRP header. Bytes 2 and 3 of the CRP header contain the address of the next level 1 unit to be serviced (BC00 in this example).

0BC00 12010503 10058400 00000000 00000000 00000A8C

Bytes 2 and 3 contain the ABEND code and is the start of MDR data.

Mode byte is X'10' and the error record byte is X'84'. This indicates that a type 1 channel adapter check occurred. Also note that the ABEND/malfunction code X'0503' is stored. See the chart that follows (from the *3704 and 3705 Program Reference Handbook),* GY30-3012-5 for the MDR record format for type 1 or type 4 channel adapter errors. Note that register X'67' is stored at X'BC12' (actual record begins at X'BC02' since each entry has a two byte header). Therefore, register X'67' contained X'0A8C'. See START 030 to find that the error was a channel bus-in check.

CHECK RECORD POOL

Program: NCP

Size in bytes: Variable (header = 10 bytes; each entry = 18-35 bytes).

Created by: NCP generation

Pointer to CRP: SYSCKRP field in HWE.

Function: Contains check records that have not yet been processed. These records are generated by program level 1 and 3 error handling routines and are processed by a program level 5 routine (CXDIERT) that prepares buffers for transfer to the host as unsolicited MDR (miscellaneous data recorder) records.

Header

0(0) CRPL1PTR Pointer to next record unit to be used by level 1.	2(2) CRPT1PTR Pointer to the next level 1 unit to be serviced by CXDIERT.
4(4) CRPL3PTR Pointer to next record unit to be used by level 3.	6(6) CRPT3PTR Pointer to the next level 3 unit to be serviced by CXDIERT.
8(8) CRPSTAT1* Trigger control byte.	9(9) CRPSTAT2 (Reserved)

Entry Format

0(0) CRPCTL CRP control bytes.	
CRPLNG* Length of the MDR data.	CRPFLG* CRP flag byte.

Start of MDR Data (CRPDATA)

		2(2) CRPABMAL Abend malfunction code. (Refer to Start 051 and 052)	
4(4) CRPREC* The recording mode byte. (For values see table.)	5(5) CRPID MDR record ID field. The 3705 MDR record is always X'05'.	6(6) CRPBERT* Box error record type code.	7(7) CRPLCRT Lost check record counter.
8(8) Up to 29 bytes of formatted information. Remainder of MDR data. (Refer to Start 053-056)			

*Indicates a byte expansion follows.

Byte Expansions

Offset/Field Name	*Bit Pattern/ Hex Value*	*Contents*
8(8) (Header) CRPSTAT1		Trigger control byte.
	X'00'	Trigger of CXDIERT is required.
	X'80'	Trigger of CXDIERT is not required.
0(0) CRPLNG (Entry Format)		Length of MDR data.
	X'04'	Invalid record.
	X'12'	Type 1/4 channel adapter.
	X'12'	Type 1 scanner.
	X'12'	Type 2 scanner-1.
	X'12'	Type 2 scanner-2.
	X'12'	Type 2 scanner-3.
	X'12'	Type 2 scanner-4.
	X'12'	Invalid operation code.
	X'12'	Input/Output instruction exception.
	X'14'	Type 3 scanner-1.
	X'14'	Type 3 scanner-2.
	X'14'	Type 3 scanner-3.
	X'14'	Type 3 scanner-4.
	X'14'	Unresolved program level 1 interrupt.
	X'14'	Unresolved program level 3 interrupt.
	X'18'	Type 2 channel adapter-1.
	X'18'	Type 2 channel adapter-2.
	X'19'	Permanent line errors.
	X'19'	Line statistics.
1(1) CRPFLG		CRP flag byte.
	1...	End of check record pool. (Bits 1-5 reserved).
	.... ..1.	Record is being serviced by CXDIERT.
	1	Check record unit has been used (filled) requires service.
4(4) CRPREC (MDR Data)		Recording mode.
	X'00'	Permanent line errors.
	X'01'	Line statistics.
	X'10'	Type 1/4 channel adapter.
	X'10'	Type 2 channel adapter-1.
	X'10'	Type 2 channel adapter-3.
	X'11'	Type 1 scanner.
	X'11'	Type 2 scanner-1.
	X'11'	Type 2 scanner-2.
	X'11'	Type 2 scanner-3.
	X'11'	Type 2 scanner-4.
	X'12'	Invalid operation code.
	X'12'	Input/Output instruction exception.
	X'13'	Unresolved program level 1 interrupt.
	X'13'	Unresolved program level 3 interrupt.
	X'FF'	Invalid record.

Offset/Field Name	*Bit Pattern/ Hex Value*	*Contents*
6(6) CRPBERT		Box error record type code.
	X'01'	Unresolved program level 1 interrupt.
	X'02'	Type 2 channel adapter-2.
	X'03'	Unresolved program level 3 interrupt.
	X'04'	Type 2 channel adapter-1.
	X'08'	Type 2 scanner-4.
	X'08'	Invalid operation code.
	X'09'	Type 3 scanner-4.
	X'10'	Type 2 scanner-3.
	X'11'	Type 3 scanner-3.
	X'20'	Type 2 scanner-2.
	X'21'	Type 3 scanner-2.
	X'40'	Type 2 scanner-1.
	X'41'	Type 3 scanner-1.
	X'84'	Type 1/4 channel adapter.
	X'C0'	Type 1 scanner.

NCP AND PEP ABEND AND EP HARDSTOP CODES

The abend codes for NCP and PEP systems are defined in the XSYSABNS mode.

When an error that causes an abend (abnormal termination) occurs, the supervisor's abend processor (CXAABND) posts an abend code in halfword direct addressable storage location X'760'. Locating the abend code in the dump gives some insight into the reason for the abnormal termination. The abend code appears in Display A on the panel if it is set to Function 6.

If the condition causing the abend is detected in level 1, the contents of external register X'74' (LAR) are stored at location X'7BC' and the contents of external register X'79' are stored at location X'6AB'. These two registers indicate the address of the failing instruction and the program level that was executing when level 1 was entered.

The first byte of the abend code indicates which portion of the NCP detected the error. The second byte indicates the specific error that was detected.

Errors Detected by Hardware

X'0000' CCU check (automatic abend). A CCU hardware error has caused an automatic reload of the ROS program. ROS saves the following external registers in these halfword direct addressable storage locations.
XR'76' at X'0702'
* XR'7D' at X'0704'
XR'7E' at X'0706'
* Bits on in this register indicate the type of CCU hardware error. For more information, see *IBM 3704 and 3705 Communications Controllers Principle of Operation,* GC30-3004.

Errors Detected by I/O Initiation Request, SVC Decoding or a Level 1 Interrupt Handling Routine (Byte 0 = X'00').

X'0001' An invalid SVC code was executed.
X'0002' A protection exception occurred.
X'0003' An XIO macro to a communication line specified an invalid QCB address.
X'0004' An XIO macro to the channel specified a BCU containing invalid chain pointers.
X'0005' An XIO macro to the channel specified a BCU containing too much text (more than can ever be transferred with a single host read operation).
X'0006' An XIO macro to the channel specified a BCU enqueued to a system queue.
X'0007' An XIO macro to the channel was used while a task was still waiting on the ECB in the first buffer of the BCU.
X'0008' An XIO macro to the channel specified a BCU in which at least one buffer had too large a text count field in the buffer prefix.
X'0009' An addressing exception occurred.
X'000A' An input/output instruction exception occurred, and retry was not possible.
X'000D' An instruction attempted to branch to storage location X'0000'.
X'000E' A program check occurred in level 1.
X'000F' An XIO macro to the link specified an invalid address.
X'0010' A level 3 channel adapter interrupt occurred while the channel adapter was active, but the command register (X'56') did not indicate a Read, Write, or Write Break command (type 2 CA only).
X'0011' A level 3 channel adapter interrupt for a host Write or Write Break occurred, and neither zero count override nor channel stop was indicated. One of these conditions should be present for every host Write operation.
X'0012' An initial selection sequence on a type 1/4 channel adapter was undefined.
X'0013' An outbound BTU had an invalid chain field.
X'0014' A data/status sequence on a type 1/4 channel adapter was undefined.
X'0015' An XIO to the channel specified a BCU address outside the buffer pool.
X'0016' An XPORT macro specified an invalid buffer address.
X'0017' An unrecoverable level 1 channel adapter check has occured.
X'0018' Zero count override was detected on a host read operation.
X'0019' An initial IN CW did not have the zero count override flag set for channel I/O.
X'001A' The retry limit for an input or output instruction was exceeded.
X'001B' The program attempted to execute an invalid operation code.
X'001C' The program attempted to switch channel adapters via an XIO macro when the logic is not generated into the NCP.
X'001D' The program attempted to use an XIO macro for a busy communication line.
X'001E' More than one XIO macro was outstanding for the same BCU.
X'001F' An XIO macro to the channel specified an invalid BTU text count.
X'0020' The INCWAR in a type 2/3 channel adapter was incorrect (hardware error).
X'0021' The access method pad size is larger than the host buffer unit size.
X'0022' Outbound data pointers incorrect program error.
X'0023' Invalid PIU address issued to channel.
X'0024' Out CW execution failure, hardware error.
X'0025' Level 3 is not in initial selection of data status for type 1/4 channel adapter.
X'0026' Attention delay PIU counter overflow or under flow.
X'0027' Attention presented bit is on but intermediate queue is empty.
X'0028' UIBLBBA is equal to zero. (Program error)
X'0029' Channel interface is disabled while the NCP is active.
X'002A' During initialization a level 3 was not pending on the channel adapter that is being loaded across.
X'002B' During initialization a level 3 is pending on a channel adapter which is SYSGENd inactive.
X'002C' During initialization, a channel adapter which has been SYSGENd inactive can not be interface disabled within a reasonable time. Manual intervention may be required.
X'002D' Invalid CAB address.
X'002E' Channel initialization error.
X'002F' Level 1 CCU I/O exception occurred. The address at LAR 2 was not equal to the address in LAR.

EP Hardstop/PEP Abend Codes (Located in group 0 register 1)

X'0030' Scanner address exception (EP only).
X'0031' L1 scanner ERP. Scanner error occurred during ERP.
X'0032' L1 scanner ERP. Unable to recover from CCU outbus check. Unable to locate the failing Output X'4X' instruction.
X'0033' L1 CA ERP. Unable to select the failing channel adapter.
X'0034' L1 CA ERP. I/O exception check. (EP only)
X'0035' L1 CA ERP. Channel Adapter error occurred during ERP.
X'0036' L1 CA ERP. Unable to recover from CCU outbus check. Unable to locate the failing Output X'6X' instruction.
X'0037' L1 CA ERP. CCU outbus check did not occur on L2 or L3.
X'0038' Initialization CCU interrupt request detected.
X'0039' L1 CCU ERP. L5 issued an in or out instruction.
X'003A' Initialization. Adapter check detected.
X'003B' L1 CCU ERP. Unable to recover from inbus parity check. Unable to locate retry point for Input X'6C'.
X'003C' L1 CA ERP. Unable to recover from CCU outbus check. Unable to locate retry point for Output X'6C'.
X'003D' L1 ERP. L1 error rate threshold exceeded.
X'003E' L1 CCU ERP. Program check. (EP only).
X'003F' L1 ERP. Unable to determine interrupted level.
X'0040' L3 interrupt from PEP and CA not system generated.
X'0041' L1 ALC ERP. Unable to recover from Airlines Line Control support L1 error. Unable to locate the failing input X'78' instruction.
X'0042' L1 ALC ERP. Unable to recover from Airlines Line Control support L1 error. Unable to locate the retry point.
X'0050' CXCAANS got control with abort pending off.
X'0051' CXCAANS got control with SNP mask = 0.
X'0053' CA active with write, write break or read but channel inoperative bit is on.

Errors Detected by Task Management (Byte 0 = X'01')

X'0102' A TRIGGER macro specified an invalid QCB.
X'0104' A reentrant CALL macro specified a non-reentrant subroutine, or a level 5 task issued a reentrant CALL macro to code that is not a subroutine.
X'0105' A level 5 task used a non-reentrant CALL macro when either the calling task or the called subroutine was reentrant.
X'0107' A BHR attempted to use a QPOST macro.
X'0108' A SETIME macro specified an interval greater than 43,200 seconds.
X'0109' A BHR attempted to use the QPOST operand on a SYSXIT macro.
X'010C' A task attempted to use a SYSXIT macro while save area(s) were still allocated to its queue control block.
X'010D' A COPYPIU macro specified an RU count too high.
X'010E' A QPOST macro specified an invalid QCB address.
X'010F' A TPPOST macro specified a BCU with an invalid resource ID.
X'0111' A TPPOST macro specified an invalid BCU address (address low).
X'0112' A TPPOST macro specified an invalid BCU address (address high).
X'0113' A COPYPIU macro specified an invalid old buffer address (address low).
X'0114' A COPYBCU macro specified an invalid old buffer address.
X'0115' A COPYPIU macro specified an invalid new buffer address (address low).
X'0116' A COPYBCU macro specified an invalid new buffer address (address high).
X'0117' A task attempted to use an EXECBHR macro when the point 3 BHR queue was empty.
X'0118' A user BHR dequeued a BCU and failed to return it to the queue (via an INSERT macro) prior to the execution of an IBM BHR.
X'0119' A BHR attempted to use an EXECBHR macro.
X'0120' A dynamic save area pool was incorrectly structured.
X'0121' A SETIME macro specified an ECB address outside the buffer pool.
X'0122' A SETIME macro specified an invalid QCB address.
X'0129' A CHAP macro specified an invalid QCB address.
X'012D' A task attempted a reentrant return when no save area was currently allocated to the task.
X'0130' A POST macro specified an ECB whose status was already "event complete".
X'0131' A task attempted to change the dispatching priority of a waiting QCB to APPNDG.
X'0132' COPYPIU — LEASE = YES invalid—new register value too large.
X'0133' COPYPIU — LEASE = YES—old PIU is too long. (over 255 buffers).
X'0134' COPYPIU — LEASE = YES—new buffer chain is too long. New chain is longer than the old.

Errors Detected by Queue Management (Byte 0 = X'02')

X'0201' An ENQUE macro specified an element that was already enqueued.
X'0202' An INSERT macro specified an element that was already enqueued.
X'0203' An EXTRACT macro specified the same address for the QCB and the positional element.
X'0204' Unassigned.
X'0205' An INSERT macro specified an element at the end of a queue.
X'0206' An INSERT macro specified the same address for the element to be inserted and the element after which it was to be inserted.
X'0207' An INSERT macro specified the same address for the element to be inserted and the QCB governing the queue.
X'0208' An ENQUEUE macro specified the same address for the element to be enqueued and the QCB governing the queue.
X'0209' A BHR attempted to use an ENQUE macro specifying an active queue control block.
X'0210' An ENQUE macro specified an element outside the buffer pool.
X'0211' An INSERT macro specified an element outside the buffer pool (positional element).
X'0212' An INSERT macro specified an element outside the buffer pool (insertion element).
X'0213' An EXTRACT macro specified an element outside the buffer pool (positional element).
X'0214' Unassigned.
X'0215' An ADVAN macro specified an element outside the buffer pool (positional element).
X'0216' A DEQUE macro specified an invalid QCB address.
X'0217' An ENQUE macro specified an invalid QCB address.
X'0218' A POINT macro specified an invalid QCB address.
X'0219' An INSERT macro specified an invalid QCB address.
X'021A' An INSERT macro specified the active QCB.
X'021B' An ENQUE macro attempted to enqueue the active QCB.
X'021C' Head/tail not both zero.

Errors Detected by Buffer Management (Byte 0 = X'03')

X'0301' A CHAIN macro specified a buffer that was already chained.
X'0302' A CHAIN macro specified the same address for the buffer to be chained and the buffer to which it was to be chained.
X'0303' Request too large.
X'0304' A RELEASE macro specified a BCU containing more buffers than the system limit on buffers per BCU.

X'0306' A RELEASE macro specified a BCU enqueued to a system queue.
X'0307' The BCU specified in a RELEASE macro had a task still waiting on its event control block.
X'030A' A LEASE macro specified a buffer count too high.
X'030F' A RELEASE macro specified a buffer outside the buffer pool (buffer address low).
X'0310' A CHAIN macro specified a positional buffer outside the buffer pool.
X'0311' A CHAIN macro specified that a buffer outside the buffer pool be chained.
X'0312' An UNCHAIN macro specified a positional buffer outside the buffer pool.
X'0314' A SCAN macro specified a buffer outside the buffer pool (positional buffer address).
X'0315' A RELEASE macro specified a buffer outside the buffer pool (buffer address high).
X'0316' Initialization routines were unable to allocate buffers.
X'0318' A LEASE macro specified an ECB address outside the buffer pool.
X'0319' A LEASE macro specified a buffer count of 0.
X'0320' The buffer pool size and the buffer availability count were in conflict.
X'0321' Less than 20 buffers were formatted during initialization of the NCP.
X'0322' A RELEASE macro specified a buffer already in the free buffer pool.

Errors Detected by Supervisory Services (Byte 0 = X'04')
X'0401' A GETBYTE macro specified a BCU address outside the buffer pool.
X'0403' A PUTBYTE macro specified a BCU address outside the buffer pool.
X'0405' A GETBYTE macro specified a BCU with an incorrect text length.
X'0406' A PUTBYTE macro specified a BCU with an incorrect test offset (in one or more of the buffer prefix fields), or a PUTBYTE macro with the operand UPDATE = YES specified a BCU with an incorrect text length.
X'0407' A GETIME macro specified invalid options.

Hardware Related and Miscellaneous Errors (Bytes X'05', X'07', X'08')
X'0501' The retry limit for unresolved level 1 interrupts was exceeded.
X'0502' The retry limit for unresolved level 3 channel adapter interrupts was exceeded.
X'0503' A nonrecoverable channel adapter check occurred.
X'0504' A nonrecoverable communication scanner check occurred.
X'0505' A type 2 channel adapter cycle steal protection exception occurred.
X'0506' A type 2 channel adapter cycle steal addressing exception occurred.
X'0507' The retry limit for recoverable channel adapter checks was exceeded.
X'0508' The retry limit for recoverable communication scanner checks was exceeded.
X'050A' A channel adapter check could not be resolved.
X'050B' A communication scanner check could not be resolved.
X'050C' A program level 1 interrupt could not be resolved.
X'050D' A machine check or IPL request was not serviced by hardware.
X'050E' A program level 3 interrupt could not be resolved.
X'050F' A program level 4 timer interrupt request expired and the timer interval was not scheduled.
X'0510' NCP generation conflict—the NCP was not configured for the type of communication scanner installed.
X'0521' NCP generation conflict program level 1 was not configured for the type of channel adapter installed.
X'0522' NCP generation conflict—an interrupt occurred from an inactive or undefined channel adapter. The channel adapter, if installed, should have been switched offline by the operator at the 3705 and should have remained disabled.
X'0523' Type 3 scanner addressing exception.
X'0524' Type 3 scanner storage protection exception.
X'0525' Load module is too large. Code and/or blocks that must reside below 64K are above 64K.
X'0701' ANS initiated by the remote NCP.
X'0702' ANS initiated at the remote controller's panel.
X'0703' SIM received by the secondary NCP.
X'0800' The link used by load program 2 was not defined at NCP generation.

Errors Detected in Level 5 (Byte 0 = X'10, X'30)
X'1001' A BCU with a Restart command contained an error in the text length field.
X'1002' The line control block (LCB) contained an invalid resource ID.
X'1003' The subtask sequence pointer in the LCB was not initialized.
X'1004' The BTU contained an invalid command modifier.
X'1005' After BHR execution, the device input queue was empty (point 1).
X'1006' After BHR execution, the line I/O queue was empty (point 2).
X'1007' After BHR execution, the point 3 BHR queue was empty.
X'1008' A task associated with the point 3 BHR queue was dispatched.
X'1009' The backspace BHR was dispatched, but the queue was empty.
X'100A' A data manipulation error occurred in the backspace BHR.
X'100B' The date/time BHR was dispatched, but the queue was empty.
X'100C' All 'skip' flags were set in the service order table (SOT).
X'100D' The number of dial digits passed from the host was not equal to the BTU text length.
X'100E' No Reset command was found at the end of an operation that was being reset.
X'100F' The device base (DVB) contained an invalid resource ID.
X'1010' An invalid system resource ID was specified in the BCU.
X'1011' An invalid checkpoint data length was specified in the BCU.
X'1012' The BH set pointer (DVIBHSET) in the DVB did not match any entry in the system BH set table (BST).
X'10EE' IOBPOLL points outside SOT.
X'10FF' Pending sessions count is negative.
X'3000' A task was dispatched with an empty QCB.
X'3001' Invalid UIB status in PIU.
X'3002' Invalid XIO return code.
X'3003' Invalid XPORT return code.
X'3001' Module CXDESSA entered when Deactivate Line halt is in progress.
X'3005' CXDCPSI unable to route PIU to SSCP.
X'3006' Reset Immediate XIO failed.
X'3007' Invalid PIU Format.
X'3008' Segmentation parameter N — zero.
X'3009' Segmentation parameters conflict.
X'300A' Run Terminator triggered with invalid status.
X'300B' Invalid Network Address in LKB.
X'300C' Invalid input passed to routine.
X'300D' LCB contains no PIU.
X'300E' CXDKFMR passed a request code to a routine which does not handle that request code.
X'300F' XIO Link failed on validated PIU.
X'3010' XPORT failed on validated PIU.
X'3011' XIO SETMODE failed.
X'3012' Invalid UIB type field.
X'3013' Invalid network address in CCU.
X'3014' Remote NCP received SNRM from local NCP.
X'3015' Remote NCP received DISC from local NCP.
X'3016' Remote detected permanent error in path to local and ANS is not in system.
X'3017' Inbound flow in SSCP PU session of a type 1 PU.
X'3018' Begin bracket PIU not on queue.

SDLC/BSC Path Function Abend Codes
X'3019' A DEQUE macro was issued by SPF CPM in and there was no error PIU on the APPL process QCB.
X'301A' An ADVAN macro was issued by SPF CPM in and there was no error PIU on the APPL process QCB.
X'301B' An EXPORT macro, issued by SPF CPM in, failed for unknown reason.
X'301C' An XPORT macro, issued by SPF CPM in, failed for an unknown reason during FID1 to FID0 conversion.
X'301D' An XPORT macro, issued by SPF CPM in, failed for an unknown reason during the export of a FID1 PIU.
X'301E' An XPORT macro was issued by an IBM point 3 BHR before the PIU was converted.
X'301F' A DEQUE macro was issued by SPF CPM out and there was no error PIU on the APPL process QCB.
X'3020' An XPORT macro, issued by the build error module (CXDSERR), failed for an unknown reason.
X'3021' A POINT macro was issued by the build error module (CXDSERR) and there was no PIU on the APPL process QCB.
X'3025' Lines or links not quiesced count went negative.
X'3026' Auto network shutdown RVT scan error. (SNA)
X'3027' An undefined Contact Poll command was detected during SNA auto network shutdown.
X'3028' The remote NCP detected a condition on the active link to the local NCP which requires backup link monitoring. Although there are backup links to the local controller, there is no backup monitor code.

Load Program 2 (LPG2) Error Codes (conditions causing an unconditional hardstop).
X'30F0' No local/remote communication link defined as active in the remote ILP configuration data set (CDS).
X'30F1' Type 1 Scanner failed to enable, hardware error on CDS definition error.
X'30F2' CDS invalid.

Load Program 2 (LPG2) Abend Codes (conditions causing a conditional hardstop).
X'3F01' No local/remote communication link active (enable failed or transmittal failed).
X'3F02' DISC (disconnect) received while monitoring one line. LPG2 to IPLs to monitor all CDS lines.
X'3F03' SNRM (set normal response mode) received while monitoring one line and load final not yet received. LPG2 to IPLs to monitor all lines.
X'3F04' Timer expiration. User specified inactive interval has expired.
X'3F05' Level 1 error.
X'3F10' SIM (set initialization mode) received during the load or dump state.

MDR RECORD FORMATS

The records for permanent line errors and line statistics are created by the line error recorder routine (CXDILER).

Record Format for Permanent Line Errors

			0(0) Line Interface Address		2(2) Recording*** Mode = X'00'	3(3) Record ID X'05'
4(4) BTU Command (BCHCMD)*	5(5) BTU Modifier (BCHMOD)*	6(6) BTU Flags (BCHSFLAG)*	8(8) IOB Command (IOBCMAND)*	9(9) IOB Modifiers (IOBCMODS)*		11(B) IOB Immediate Control Command (IOBIMCTL)*
12(C) IOB Status (IOBSTAT)*		14(E) IOB Extended Status (IOBEXTST)*	15(F) IOB Initial Error Status (IOBERST)*		17(11) IOB Initial Error Extended Status (IOBEREST)*	18(12) I/O-Counter (DVBSDRT)*
20(14) Temporary Error Counter (DVBSDRE)*	21(15) 2740 Graphic Response Byte**	22(16) Device Features (DVBFEAT1)*	(DVBFEAT2)*	24(18) Device Type (DVBTYPE)*		

*Indicates the control block field from which this MDR record field is loaded. (See Note.)
**2740 graphic response byte is zeroed if not applicable.
***Applies to BSC/SS devices as well as lines.

Record Format for Station Statistics

		0(0) Line Interface Address	2(2) Recording Mode = X'01'	3(3) Record ID = X'05'
4(4) Hex Zeros				
				18(12) I/O Counter (DVBSDRT)* / or SCB transmission counter (SCBTCNT) if SDLC. I-Format
20(14) Temporary Error Counter (DVBSDRE)* / or SCB retry count (SCBTRTCT) if SDLC	22(16) Device Features (reserved if SDLC) (DVBFEAT1)*	(DVBFEAT2)*	24(18) Device Type (DVBTYPE)* / or SCB station type (SCBTYPE) if SDLC	

*Indicates the control block field from which the MDR record field is loaded. (See Note.)

Note: *For field definitions refer to either IBM 3704-05 Program Reference Handbook, GY30-3012 or IBM 3705 Advance Communication Functions for NCP, SY30-3029.*

Record Format for Permanent SDLC Errors

			0(0) Line Interface Address		2(2) Recording Mode X'03' = Station Error X'02' = Link Error	3(3) Record ID X'05'
4(4) * SCB Service Seeking Command Flags (SCBSSCF)	6(6) * Output Control Flag (SCBOCF)	7(7) Reserved	8(8) LXB Command (LXBCMAND)	9(9) LXB Modifiers (LXBCMODS)		11(B) LXB Immediate Control Command (LXBIMCTL)
12(C) LXB Final Error Status *2* (LXBSTAT) LXBSTAT / LXBSTATC	14(E) LXB Final Error Extended Status (LXBEXTST)	15(F) LXB Initial Error Status *3* (LXBERST) (LXBERST / LXBHSTAT)		17(11) LXB Initial Error Extended Status (LXBEREST)	18(12) * SCB Transmission Counter (SCBTCNT) I-Format	
20(14) * SCB Retry Count (SCBTRTCT)	21(15) Received BLU Command Field (LXBRBLUC)	22(16) Reserved	24(18) * SCB Status Type (SCBTYPE)	25(19) ** Transmit BLU Command Field (CCBCFLD)	26(1A) * SCB Current Outstanding Count (SCBCOC)	27(1B) * SCP Pass Count (SCBPCNT)
28(1C) * SCB Receive Count (SCBNR) (Bits 4,5,6)	29(1D) * SCB Send Count (SCBNS) (Bits 4,5,6)	30(1E) CCB Control Flags and Line Type (CCBCTL) CCBRSPON Control Flag / CCBTYPE Line Type	32(20) *** Command Field Received from Secondary Station SECCFR	33(21) *** N(R) and N(S) Received from Secondary Station	34(22) *** Command Reject Reason X'08' = Invalid N(R) X'04' = Frame too Long X'02' = Data Received in S or NS Format X'01' = Invalid Command	

*This field is present only if this record is for a station (for a link, field contains all zeros).
**This field stored only for duplex links.
***This field stored only if Command Reject was the cause of the MDR record being formatted.
*2*Last error recognized.
*3*First error recognized.

Note: *For field definitions refer to either IBM 3704-05 Program Reference Handbook, GY30-3012 or IBM 3705 Advance Communication Functions for NCP, SY30-3029.*

The records on this and the following pages are created by level 1 error processing routines. They are prepared for transfer to the host by the error record transfer routine (CXDIERT).

Record Format for Type 1 or Type 4 Channel Adapter Errors

4(4) Error Record Type X'84' (Type 1 CA)	5(5) Lost Check Record Count (CRPLCRCT)	6(6)	0(0) Abend/Malfunction Code	2(2) Recording Mode = X'10'	3(3) Record ID = X'05'
		Hex Zeros			
			16(10) External Register X'67' Type 1 CA Controls		

Record Format for Type 2 Communication Scanner Errors

4(4) Error Record Type*	5(5) Lost Check Record Count (CRPLCRCT)	6(6) External Register X'43' Check Register 1	0(0) Abend/Malfunction Code	2(2) Recording Mode = X'11'	3(3) Record ID = X'05'
			8(8) External Register X'74' Lagging Address Register		
12(C) Interrupted Program Level's Instruction Address Register (Register 0)			16(10) External Register X'79' Program Level Interrupted '		

*Type 2 Scanner = X'40'

Record Format for:

- Invalid Instruction Operation Code Check. (Abend = X'001B')
- Address Exception. (Abend = X'0009')
- Protection Check. (Abend = X'0002')
- Branch to zero by Level 5. (Abend X'000D')

4(4) Error Record Type = X'08'	5(5) Lost Check Record Count (CRPLCRCT)	6(6) Halfword from Interrupted Program Levels IAR-2 or zero	0(0) Abend/Malfunction Code	2(2) Recording Mode = X'12'	3(3) Record ID = X'05'
			8(8) External Register X'74' Lagging Address Register		
12(C) Interrupted Program Level's Instruction Address Register (Register 0)			16(10) External Register X'79' Program Level Interrupted		

Record Format for Input/Output Instruction Exceptions

4(4) Error Record Type = X'20'	5(5) Lost Check Record Count (CRPLCRCT)	6(6) Instruction on which the Error Occurred	0(0) Abend/Malfunction Code	2(2) Recording Mode = X'12'	3(3) Record ID = X'05'
			8(8) External Register X'74' Lagging Address Register		
12(C) Interrupted Program Level's Instruction Address Register (Register 0)			16(10) External Register X'79' Program Level Interrupted		

Note: *For field definitions refer to either IBM 3704-05 Program Reference Handbook, GY30-3012 or IBM 3705 Advance Communication Functions for NCP, SY30-3029.*

Record Format for Unresolved Program Level 1 Interrupt Requests

			0(0) Abend/Malfunctions Code	2(2) Recording Mode = X'13'	3(3) Record ID = X'05'
4(4) Error Record Type = X'01'	5(5) Lost Check Record Count (CRPLCRCT)	6(6) External Register X'76' Adapter Interrupt Requests Group 1	8(8) External Register X'74' Lagging Address Register		
12(C) Interrupted Program Level's Instruction Address Register (Register 0)			16(10) External Register X'79' Program Level Interrupted	18(12) External Register X'7E' CCU Interrupt Requests Group 1	

Record Format for Unresolved Program Level 3 Interrupt Requests
This record is created by the level 3 router (CXCCRTR)

			0(0) Abend/Malfunction Code	2(2) Recording Mode = X'13'	3(3) Record ID = X'05'
4(4) Error Record Type = X'03'	5(5) Lost Check Record Count (CRPLCRCT)	6(6) External Register X'77' Adapter Interrupt Requests Group 2	8(8)		
Hex Zeros				18(12) External Register X'7F' CCU Interrupt Requests Group 2	

Note: *For field definitions refer to either IBM 3705-80 Program Reference Handbook, GY30-3012 or IBM 3705 Advance Communication Function for NCP, SY30-3029.*

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HOST PROCESSOR CONSOLE ERROR MESSAGES

Host Processor Console Error Messages may be helpful in time stamping and determining the cause of a suspected failure in the 3705.

Analyze the error message to determine:

1. If the address reported is on the suspected 3705.
2. To determine the status, sense or other error data associated with the error.
3. If a trend is present in multiple addresses.

The console error messages should be correlated with EREP records and customer reports to pinpoint failure times and causes.

Examples of error messages:

TCAM

```
IEA000I 56E,DCK,01,0600,080006000001,,,TCAM ,08.35.30
        (A) (B) (C) (D)      (E)              (F)
```

VTAM

```
IEA000I 035,TOT,02,0E40,0100,0A**4040,,DPPOODPP ,08.00.13
        (A) (B) (C) (D)  (E)                     (F)
```

HASP - JES2

```
02.48.22     $HASP094  I/O ERROR ON LINE 8   657,02,0E00,0161,A661
 (F)                        (B)               (A) (C) (D)  (E)
```

where:

- (A) = Control Unit Address
- (B) = Error Description
- (C) = Command Code
- (D) = CSW Status
- (E) = Sense Byte
- (F) = Time

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COMMAND CODES

NSC Commands

Command Codes	*Command*	*Description*
00	Test I/O	Hardware Presents the current status of the NSC.
03	I/O NO-OP	Immediate initial status of CE/DE is presented by the hardware if the CA is free of commands.
05	Write IPL	Hardware accepts the command, returns status of '00' and causes a CA L3 interrupt. Control program is loaded into storage.

EP Command Codes

S/360 and S/370	*Command*
00	Test I/O
01	Write
02	Read
03	I/O No-Op
12	Diagnostic Read
05	Diagnostic Write
13	Set Address Zero
17	Set Address One
1B	Set Address Two
1F	Set Address Three
1D	Diagnostic Poll
04	Sense
15	Wrap
06	Prepare
41	Write Break
09	Poll
0A	Inhibit
19	Poll SOH
42	Read Clear
0D	Break
0E	Search
2F	Disable
27	Enable
29	Dial
1E	Address Prepare
23	Set Mode

NCP Channel Commands

Command Code	*Command*	*Description*
X'01'	Write	The Write command is initiated to the NCP. Data in the CPU main storage is transferred to the NCP.
X'02'	Read	The Read command is initiated at the NCP. Data at controller storage is transferred to CPU main storage.
X'03'	No-Op	This command is required as the last CCW in a Read or Write CCW chain.
X'04'	Sense	The host initiates this command. One byte of sense data is transferred to the host.
X'09'	Write Break	The Write Break command is identical to the Write command except that it is used to indicate that it is the last or only Write command in a chain of Write CCWs.
X'31'	Write Start 0	This is the first command expected in Write Channel program after IPL of the NCP. It is also expected after each successful Write Start 1 command.
X'32'	Read Start 0	This is the first command expected in the Read Channel program after IPL of the NCP. It is also expected after each successful Read Start 1 command.
X'51'	Write Start 1	This is the second command expected in the Write Channel program after IPL of the NCP. It is also expected after each successful Write Start 0 command.
X'52'	Read Start 1	This is the second command expected in the Read Channel program after IPL of the NCP. It is also expected after each successful Read Start 0 command.
X'93'	Reset Restart	This command causes the NCP to reset its switches to indicate that the last Write Start and Read Start commands were Write Start 1 and Read Start 1.

Notes:

1. *Data transfer does not occur on Read Start and Write Start commands.*
2. *See IBM 3705-80 Communications Controller Principles of Operation, GC30-3074, for a description of the operation of the Test I/O X'00' and Write IPL X'05' channel commands.*

Sense Bit Definitions

Bit 0 — Command Reject. This bit indicated that the channel command presented to the channel adapter is not a valid command for a particluar subchannel address or not valid for the NSC address.

Bit 1 — Intervention Required. This bit indicated that programming errors were detected by either the CA, the CCU, or the 3705 control program. CA hardware sets this bit when the CA is executing a channel Read, Write, or Write Break command.

Bit 2 — Bus Out Check. This bit indicated a parity check was detected on the I/O channel bus out during the initial selection command byte transfer or during host processor to 3705 data transfer.

Bit 3 — Equipment Check. This bit indicates that an internal hardware check or a parity check is detected during a data transfer between the CCU and the channel adapter.

Bit 4 — Data check.

Bit 5 — Not used.

Bit 6 — This bit indicated that the CCU is not initialized. The host CPU is expected to respond to this bit with a Write IPL command.

Bit 7 — Abort. This bit indicated that the 3705 control program has terminated its channel operation in and abnormal manner.

Note: *Refer to START 062-064 for the sense bit definitions that are program independent.*

Sense Command Ending Status

Ending status can be presented to the channel in one of three combinations:

1. CE, DE presented together - normal operation.
2. Split CE, DE, (that is, not together).
3. CE, DE, and UC, - occurs when interface disconnect is received during a Sense command.

SENSE INFORMATION

The following tables summarize sense information that the Emulation Program can present to the host processor. The Emulation Program maintains this information for each line in the CCBSENSE byte of the CCB.

Table 1 lists sense information by bit for start-stop terminals. Start-stop terminals are broken down into four general classifications: 1) all start-stop terminals except, 2) 1030, 3) TTY 33/35, and 4) TTY 83B2/B3 and WU115A. Table 2 lists sense information by bit for BSC terminals, all of which are treated alike.

The sense-byte bit designation are:

CCBSENSE Bit 0 Command Reject
1 Intervention Required
2 Bus Out Parity Check
3 Equipment Check
4 Data Check
5 Overrun
6 Lost Data
7 Time-out Complete

For further details on sense information, see *IBM 3705-80 Communications Controller Principles of Operation, GC30-3074.*

Command	*All Start-Stop Terminals except*	*1030*	*TTY 33/35*	*TTY 83B2/B3 and WU115A*
Bit 0-Command Reject				
SEARCH	Command invalid for all start-stop terminals.			
BREAK		Command invalid for these terminals.		
POLL	Command invalid for these terminals.			
DIAL	No auto call feature installed.	Command invalid for this terminal.	No auto call feature installed.	Command invalid for this terminal.
ADPREP SET MODE	Commands invalid for all start-stop terminals.			
INVALID COMMAND	Command invalid for all start-stop terminals.			
WRAP	1. Line in transparent wait mode. 2. Previous WRAP still in progress. 3. Line is defined as wrap line.			
All commands except TIO, I/O, NO-OP and SENSE	1. Panel test is active on the line. 2. MSLA line is currently being used by another subchannel.			
Bit 1-Intervention Required				
WRITE* PREPARE	1. Data set power off. 2. Data set ON HOOK.**** 3. Data set not in data mode. 4. Line not enabled. 5. Break signal received (applicable for all start-stop devices except 2848/2845).		Line not enabled.	
READ** INHIBIT**	1. Same as Write 1, 2, 3, & 4. 2. Space for over 1 character time.		1. Line not enabled. 2. Space for over 1 character time.	
POLL*	1. Same as Write 1, 2, 3, & 4 2. Space for over 1 character time.	N/A		

Table 1. Sense Bit Information—Start-Stop Terminals (Part 1 of 3)

Command	*All Start-Stop Terminals except*	*1030*	*TTY 33/35*	*TTY 83B2/B3 and WU115A*
DIAL	1. Auto call unit power off. 2. No auto call unit attached.	N/A	1. Auto call unit power off. 2. No auto call unit attached.	N/A
SEARCH**	N/A		1. Line not enabled. 2. Space for over 1 character time.	
BREAK*	2741 with break: Same as Write 1, 2, 3, & 4. Line not enabled: same as Write 1, 2, 3, & 4.			
ENABLE	For non-switched lines, Data Set Ready does not rise after a one-second time-out.			
Bit 2-Bus-Out Parity Check				
Any command associated with this transfer of data	Wrong bus-out parity when output data (from the channel) is being presented.			
Any valid or invalid command	Wrong bus-out parity during initial selection.			
Bit 3-Equipment Check				
All commands	1. An active command is being executed, and a new command is issued for that line. 2. A check condition that does not cause a hard stop (I/O check, adapter check, or address exception) is detected in the controller and is associated with a particular line or line group.			
ENABLE DISABLE	A feedback check occurs.			
DIAL	1. A call request fails to turn on or off. 2. An auto call or feedback check occurs.			
Bit 4-Data Check				
WRITE	1. VRC check. 2. Echo checks, if telegraph feature is installed.	VRC check.	N/A	Echo check.
READ INHIBIT	1. VRC check. 2. LRC check. 3. (N) response to a text message 4. Line at space at stop-bit time.	1. VRC check. 2. (N) response to a text message 3. Line at space at stop-bit time.	Line space at stop-bit time.	
POLL	1. VRC check. 2. Line at space at stop-bit time. 3. Response received is other than (N) or (D) 4. Echo check, if telegraph feature is installed.	1. VRC check. 2. Line space at stop-bit time. 3. Response received is other than (N) or (D)	N/A	
WRAP DIAG WRITE	VRC check	VRC check	N/A	
SEARCH	N/A			Line at space at bit time.
BREAK	N/A			Echo check.
DIAG READ	Same as Read 1 & 4	Same as Read 1 & 3	Same as Read	

Table 1. Sense Bit Information—Start-Stop Terminals (Part 2 of 3)

Command	*All Start-Stop Terminals except*	*1030*	*TTY 33/35*	*TTY 83B2/B3 and WU115A*
Bit 5-Overrun				
READ INHIBIT	Set during a receive operation if data service for one buffer is not honored by the ICP before the next buffer has been filled.			
Bit 6-Lost Data				
READ INHIBIT DIAG READ	1. Data service request is on when Read is issued. 2. Receiving bit is on when Halt I/O is issued. 3. Data service request is on when Halt I/O is issued. 4. Channel issues Stop during read service operations.			
SEARCH	N/A			1. Receiving bit is on when Halt I/O is issued. 2. Receiving bit is on when search command is issued. 3. Data Service request is on when Halt I/O is issued. 4. Channel issues Stop during a read service operation.
DIAL	The data set is OFF HOOK*** Data Set Ready or Present Next Digit is on before Call Request is set.	N/A	The data set is OFF HOOK*** Data Set Ready or Present Next Digit is on before Call Request is set.	N/A
PREPARE POLL	Receiving bit is on when Halt I/O is issued.		N/A	
Bit 7-Time-out				
READ	1. No character is received within 3 seconds in control mode (awaiting response to selection or polling). 2. No character is received for 25.6 seconds when in text mode.		A 25.6 second time lapse occurs between characters.	1. First character is not received within 2 seconds when the Receiving bit is off. 2. A 25.6 second time lapse occurs between characters when the Receiving bit is on.
DIAL	Abandon Call and Retry is returned from an auto call unit.	N/A	Abandon Call and Retry is returned from an auto call unit.	N/A
PREPARE	Open line (continuous space) for 25.6 seconds			
SEARCH	N/A			Same as Read
POLL	No characters received within three seconds in poll mode (awaiting response to polling)		N/A	
DISABLE	On a switched network, Data Set Ready does not go off within 25.6 seconds after Disable is issued.	N/A	On a switched network, Data Set Ready does not go off within 25.6 seconds after Disable is issued.	N/A
INHIBIT	No response within three seconds for an initial character.			
Any Transmit except WRAP	Line does not become transmit operational within 25.5 seconds.			

*Line does not become Transmit Operational within 25.5 seconds.
**Line does not become Receive Operational within time-out period specified.
***OFF HOOK means that Data Set Ready is set before all dial digits are presented.
****Communication line connection is broken on a dial line.

Table 1. Sense Bit Information—Start-Stop Terminals (Part 3 of 3)

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Command	*Binary Synchronous Lines*
	Bit 0 - Command REJECT
READ POLL PREPARE	Line in transparent wait mode or disabled
ENABLE DISABLE SET MODE	Line in transparent wait mode.
DIAL	Line in transparent wait mode, or no auto call feature installed.
BREAK CLEAR INHIBIT DIAG READ DIAG WRITE	Command invalid for BSC.
SEARCH AD PREP	1. Line in transparent wait mode. 2. No station selection capabilities on this line. 3. Line disabled.
Any other command	Command invalid for BSC.
WRITE	Line disabled.
WRAP	1. Line in transparent wait mode. 2. Previous WRAP still in progress. 3. Line is defined as wrap line.
All commands except TIO, I/O, NO-OP and SENSE	1. Panel test is active on the line. 2. MSLA line is currently being used by another subchannel.
	Bit 1 - Intervention Required
WRITE* POLL* READ** SEARCH** ADD PREP** PREPARE	1. Data set power off. 2. Data set ON HOOK.**** 3. Data set not in data mode. 4. Data set not attached to Emulation Program. 5. Set immediately upon fall of clear to send.
DIAL	1. Auto call unit power off. 2. No auto call unit attached. 3. Data Line Occupied when Dial command is issued.
	Bit 2 - Bus-Out Parity Check
Any valid or invalid command	Wrong bus-out parity during initial selection, data transfers, or status presentation.
	Bit 3 - Equipment Check
All Commands	A scanner check occurs. Equipment check is presented on all affected lines.
ENABLE DISABLE	A set mode operation (PCF set to X'1') did not complete because of an oscillator failure.
DIAL	1. Call request fails to turn on or off. 2. An auto call or line interface transfer check occurs.
	Bit 4 - Data Check
READ	1. CRC or LRC non-compare. 2. VRC error for USASCII code. 3. Incorrect control character sequence in transparent mode (DLE followed by other than DLE, SYN, ETX, ETB, ENQ, or ITB).
SEARCH AD PREP POLL (rcv)	VRC error for USASCII code.

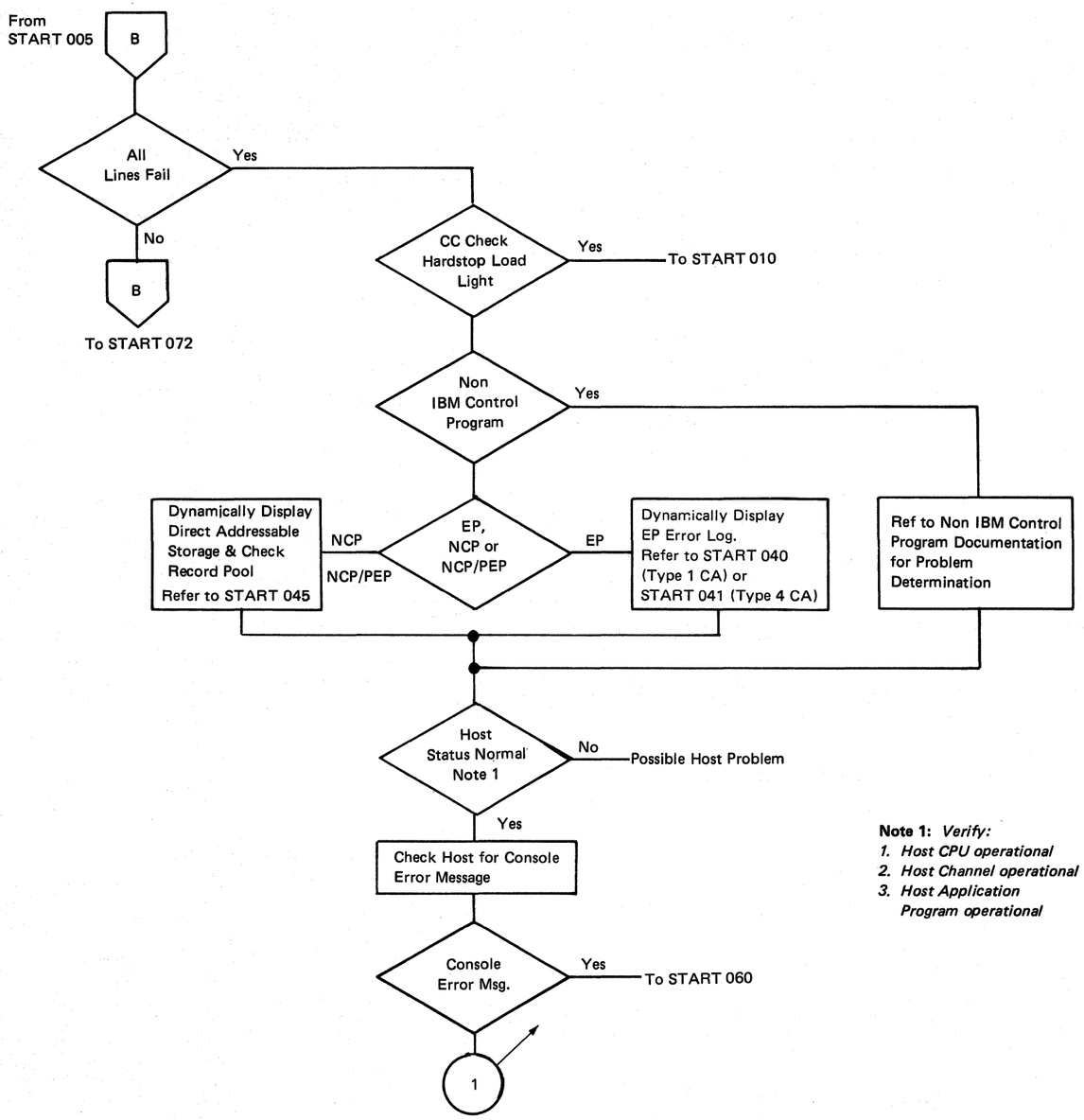
Table 2. Sense Bit Information-BSC Terminals (Part 1 of 2)

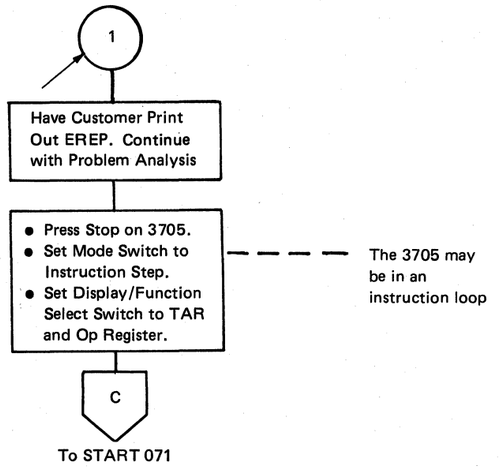
Command	*Binary Synchronous Lines*
	Bit 5 - Overrun
READ, SEARCH, or POLL (receive	Data service is not honored by the Emulation Program before the next character is received. Set during a receive operation if data service for one buffer is not honored by the ICP before the next buffer has been filled.
	Bit 6 - Lost Data
READ SEARCH	1. The command is issued to a line which has already received more characters than can be contained in the CCB data buffers and PDF. 2. The Emulation Program is still receiving from a terminal when Halt I/O is issued to that line. 3. All buffered characters have not been sent to the host processor when Halt I/O is received for that line. 4. A channel stop is indicated by the channel before all characters have been transmitted to the host processor.
DIAL	The data set is OFF HOOK*** on the addressed line.
	Bit 7 - Timeout Complete
WRITE	No Write is received within three seconds when in transparent wait mode.
READ	1. Read follows Poll, and Poll command receives no response within 3 seconds. 2. None of the following characters or character sequences is received within three seconds: *Characters* ENQ, ACK, NAK, EOT, SOH, or STX. *Character Sequences* DLE-STX, DLE-STX. SYN, SYN, NON-SYN (if not in transparent mode) DLE-SYN, NON-DLE (if in transparent mode)
SEARCH	1. Search follows Poll, and Poll command receives no response within three seconds. 2. None of the following characters or character sequences is received within one second while in control mode or within 3 seconds while in text mode or transparent mode. *Characters* ENQ, ACK, NAK, EOT, SOH, or STX. *Character Sequences* DLE-STX, DLE-STX SYN, SYN, NON-SYN (if not in transparent mode) DLE-SYN, NON-DLE (if in transparent mode)
DIAL	The auto call unit returns ACR (Abandon Call and Retry).
DISABLE	The switched network data set does not go OFF HOOK*** within three seconds.

*Line does not become Transmit Operational within 25.5 seconds.
**Line does not become Receive Operational within three seconds.
***OFF HOOK means that Data Set Ready is set before all dial digits are presented.
****Communication line connection is broken on a dial line.

Table 2. Sense Bit Information-BSC Terminals (Part 2 of 2)

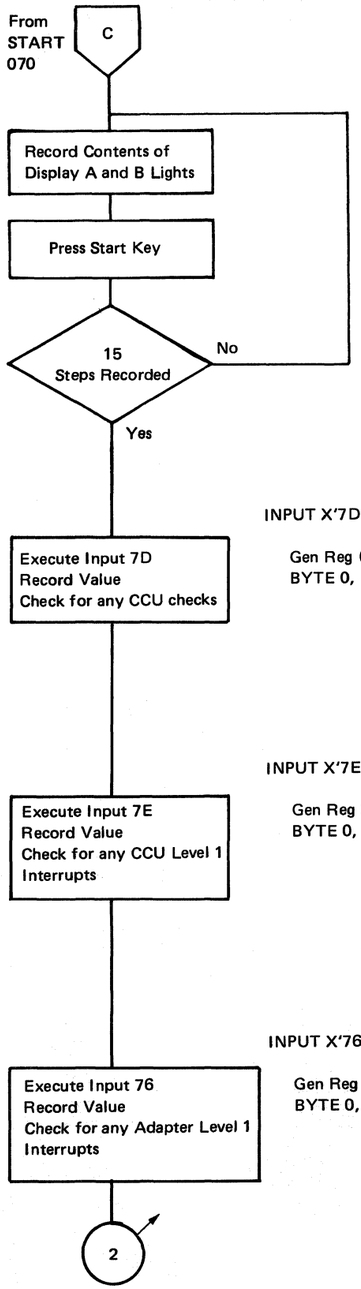
LINE FAILURE ANALYSIS





Note 1: *Verify:*

1. *Host CPU operational*
2. *Host Channel operational*
3. *Host Application Program operational*



INPUT X'7D' — CCU CHECK REGISTER

Gen Reg (R)		Reg/Function (E)
BYTE 0,	BIT 0	Byte X Check
	BIT 1	Byte 0 Check
	BIT 2	Byte 1 Check
	BIT 3	Program Check in Level 1
	BIT 4	SAR Check
	BIT 5	SDR Check
	BIT 6	OP Reg Check
	BIT 7	INDATA Bus Check

BYTE 1,	BIT 0	Cycle Counter Check
	BIT 1	0
	BIT 2	0
	BIT 3	0
	BIT 4	0
	BIT 5	0 = No CCU Checks; 1-CCU Check(s)
	BIT 6	TYPE 2 Attach Base Clock Check
	BIT 7	CCU Clock Check

INPUT X'7E' — CCU LEVEL 1 INTERRUPT REQUESTS

Gen Reg (R)		Reg/Function (E)
BYTE 0,	BIT 0	0
	BIT 1	0
	BIT 2	0
	BIT 3	0
	BIT 4	0
	BIT 5	0
	BIT 6	0
	BIT 7	0

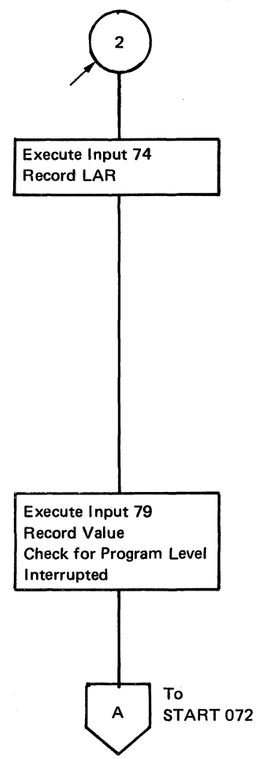
BYTE 1,	BIT 0	Address Compare Interrupt L1
	BIT 1	Address Exception (note)
	BIT 2	In/Out Check (note)
	BIT 3	Protection Check (note)
	BIT 4	Invalid Op Check (note)
	BIT 5	0
	BIT 6	IPL L1
	BIT 7	0

Note: *Prog Check*

INPUT X'76' — ADAPTER LEVEL 1 INTERRUPT REQUESTS

Gen Reg (R)		Reg/Function (E)
BYTE 0,	BIT 0	Type 4 CA L1
	BIT 1	Type 2 Scan-1 L1
	BIT 2	0
	BIT 3	0
	BIT 4	0
	BIT 5	Type 1 CA, or Selected Type 4 CA L1
	BIT 6	0
	BIT 7	Remote Program Loader L1 Request

BYTE 1,	BIT 0	0
	BIT 1	0
	BIT 2	0
	BIT 3	0
	BIT 4	0
	BIT 5	0
	BIT 6	0
	BIT 7	0



INPUT X'74' — LAGGING ADDRESS REGISTER (LAR)

Gen Reg (R)		Reg/Function (E)					
BYTE X,	BIT 4	LAR BYTE X,	BIT 4 }	with 20-bit EA only			
	BIT 5		BIT 5 }				
	BIT 6		BIT 6 }	with 18 or 20-bit EA			
	BIT 7		BIT 7 }				
BYTE 0,	BIT 0	LAR BYTE 0,	BIT 0		BYTE 1,	BIT 0	LAR BYTE 1, BIT 0
	BIT 1		BIT 1			BIT 1	BIT 1
	BIT 2		BIT 2			BIT 2	BIT 2
	BIT 3		BIT 3			BIT 3	BIT 3
	BIT 4		BIT 4			BIT 4	BIT 4
	BIT 5		BIT 5			BIT 5	BIT 5
	BIT 6		BIT 6			BIT 6	BIT 6
	BIT 7		BIT 7			BIT 7	BIT 7

EA = Extended Addressing

INPUT X'79' — UTILITY

Gen Reg (R)		Reg /Function (E)			
BYTE 0,	BIT 0	0	BYTE 1,	BIT 0	Program Level 2 Interrupted (note)
	BIT 1	0		BIT 1	Prog Level 3 Interrupted (note)
	BIT 2	0		BIT 2	Prog Level 4 Interrupted (note)
	BIT 3	0		BIT 3	Prog Level 5 Interrupted (note)
	BIT 4	0		BIT 4	FET memory
	BIT 5	0		BIT 5	0
	BIT 6	Prog Level 5 C Condition		BIT 6	0
	BIT 7	Prog Level 5 Z Condition		BIT 7	IPL Escape Control

Note: *This bit=0 if not Level 1 or if entered immediately after exiting Level 1.*

LINE FAILURE ANALYSIS (Cont.)

From START 071

A

Any Adapters Level 1 Intrp.

Yes

Interrupt	Reference
Type 1/4 CA Level 1	START 030
CS2 Level 1	START 030
RPL Level 1	START 030

No

Display ROS Direct Addressable Storage
X'0702' = Input 76
X'0704' = Input 7D
X'0706' = Input 7E

Stored By ROS If a CCU Error Has Caused an Automatic Reload of the ROS Program

Press Reset
Press Load

Dump 3705 Control Program

3705 Available for Diagnostics (Note 1)

Yes

No

Have Customer RELOAD 3705 Control Program and Restart

Check Erep for Error Messages

START 100

Analyze all Data and Take Appropriate Repair Action

RPL Feature

Yes

No

Run Diagnostics Refer to START 020

All Diagnostics are on RPL Diskette Refer to: RPL Diag.

From START 070

B

Multiple or Single Line Failures (Note 2)

Non-IBM Control Program

Yes

Refer to Non-IBM Control Program Documentation for Problem Determination

EP or NCP NCP/PEP

NCP

NCF/PEP

Dynamically Display Direct Addressable Storage & Check Record Pool. Refer To Start 045.

EP

Dynamically Display EP Error Log. Refer to START 040 (Type 1 CA) or START 041 (Type 4 CA)

EP Error Log or NCP Chk. Record Pool Entry

Yes

Analyze Data

Schedule 3705 for Diagnostics or Repair Action

No

Check Host for Console Error Msg.

Console Error Msg.

Yes

To START 060

No

Check Erep for Error Message(s)

Error Message(s)

Yes

To START 100

3

3

Verify Host Application Pgm Utilizing the Failing Line(s) Is Running

Is Application Program Running

Yes

Refer Problem to Customer Tech. Support Group

No

Host Application Program Problem

Note 1: *Intermittent errors may be found by running diagnostics under bias. The -4 volts should be biased in increments of .1 volts plus and minus, not to exceed 10% (3.6—4.4), while running all diagnostics. If by referring to the NCP check record pool (CRP) or the EP error log, the error is with a specific adapter, the particular section for that adapter should be looped using the above biasing procedure. A Digitec meter or equivalent should be used for biasing the machine. Restore the -4 volts to its proper setting upon completion of testing.*

Note 2: *Single line failures— probable 3705 hardware causes:*

1. *Line set card*
2. *3705 to modem cable*

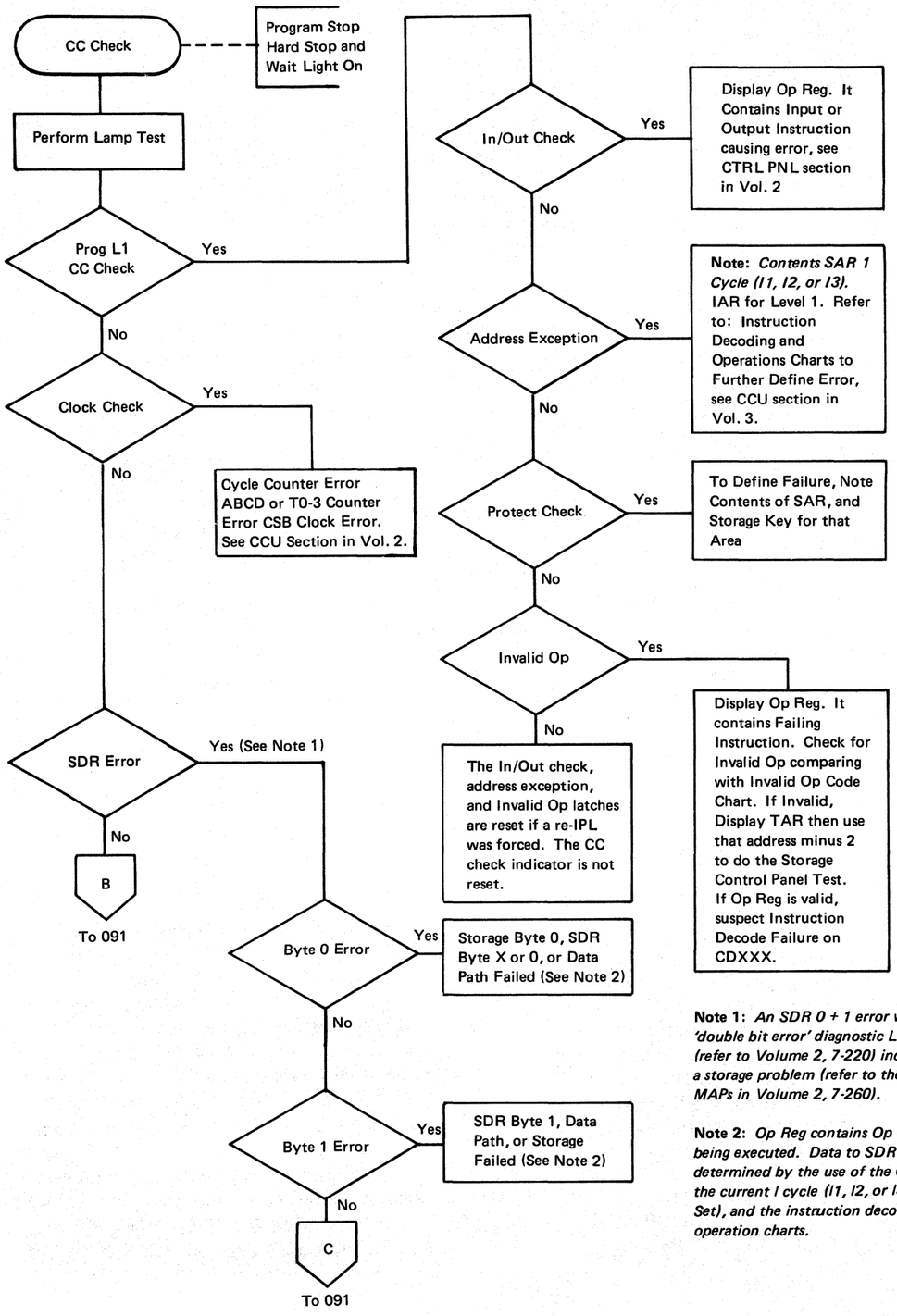
EC AND MES INSTALLATION

The installation of ECs and MESs must be coordinated with the customer to minimize impact on the network environment.

Use the steps that follow:

1. Read the instructions.
2. Inventory the EC/MES to ensure all parts have been received.
3. Check early warning microfiche for:
   A. B/M tips
   B. Hardware tips
   C. OLTs tips
4. Check prereqs and concurrents for:
   A. Hardware configuration and EC levels
   B. Diagnostic level
   C. 3705 NCP or EP program PTF/APAR level
   D. Operating system level
5. Review EC/MES with customer.
6. Schedule time for installation.
7. Ensure CDS is proper and run all diagnostics prior to installing EC/MES.
8. Install EC/MES.
9. Reconfigure CDS (if required) and run all diagnostics to verify correct operation.
10. Have customer load his control program and verify correct operation.

CC CHECK ANALYSIS FLOWCHART (See Note 3)



Note 1: *An SDR 0 + 1 error with the 'double bit error' diagnostic LED on (refer to Volume 2, 7-220) indicates a storage problem (refer to the Memory MAPs in Volume 2, 7-260).*

Note 2: *Op Reg contains Op Code being executed. Data to SDR can be determined by the use of the Op Code, the current I cycle (I1, I2, or I3 Latch Set), and the instruction decode and operation charts.*

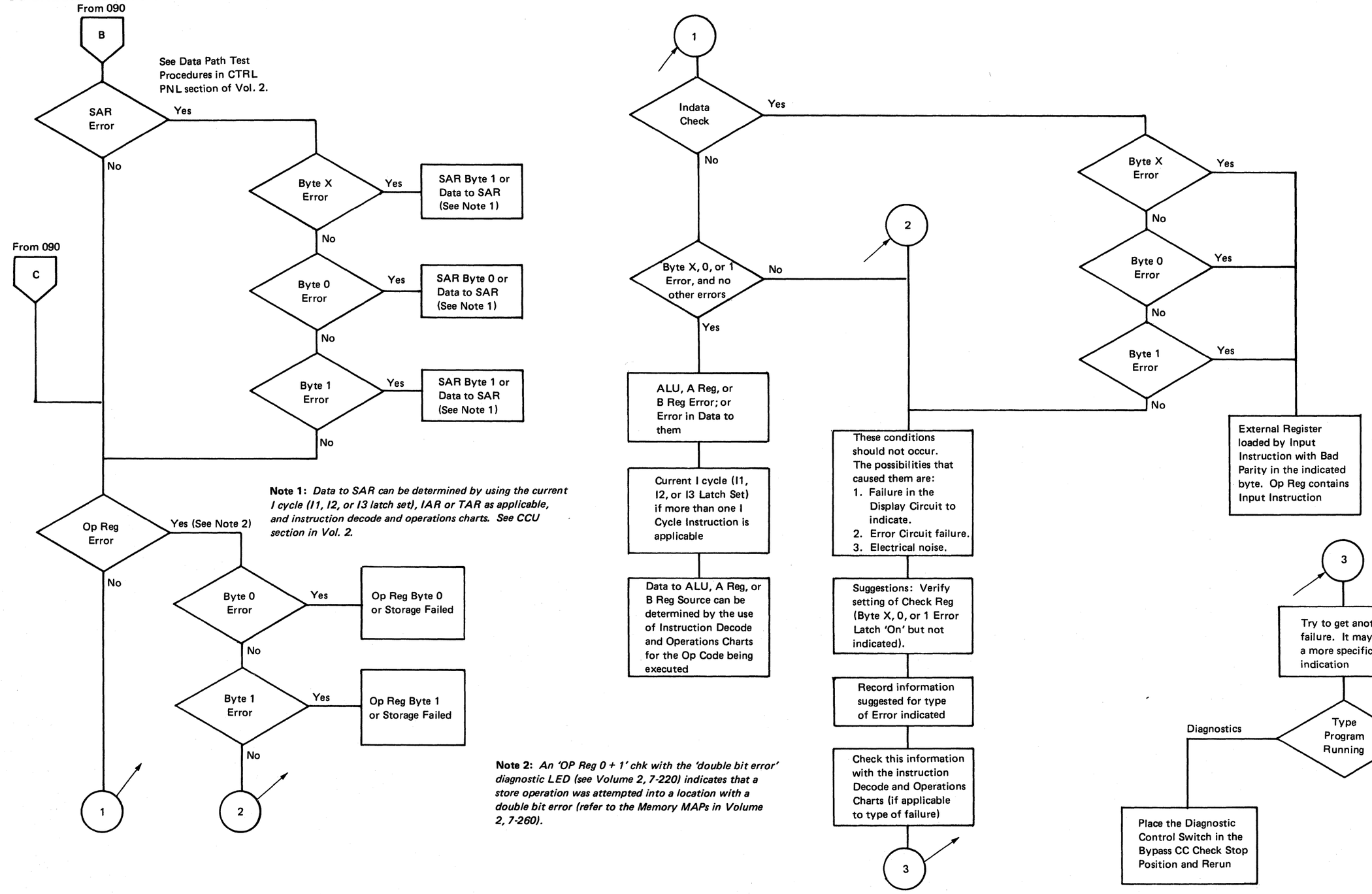
Invalid Operation Codes

Operation Register																
Byte 0								*Byte 1*								
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
0	X	X	X	0	X	X	X	0	0	X	0	0	0	0	0	
0	X	X	X	0	X	X	X	0	1	0	1	0	0	0	0	
0	X	X	X	0	X	X	X	0	1	1	X	0	0	0	0	
1	0	1	1	1	0	0	1	0	1	0	0	0	0	0	0	
1	0	1	1	1	0	1	X	0	1	0	0	0	0	0	0	
1	0	1	1	1	1	X	X	0	1	0	0	0	0	0	0	
1	0	1	1	1	X	X	X	0	1	0	0	0	0	0	1	
1	0	1	1	1	X	X	X	0	1	0	0	0	0	1	X	
1	0	1	1	1	X	X	X	0	1	1	0	0	0	X	X	
1	0	1	1	1	X	X	X	0	X	X	1	X	X	X	X	
1	0	1	1	1	X	X	X	0	X	X	0	1	0	X	X	3705-I
1	0	1	1	1	X	X	X	0	X	X	0	X	1	X	X	
1	0	1	1	1	X	X	X	0	1	X	0	X	1	X	X	3705-II
1	0	1	1	1	X	X	X	0	1	X	0	1	X	X	X	

X = Don't Care

Note 3: *If errors occurred during a power on sequence, verify that ROS has loaded properly, using the ROS listings in Vol. A42. If ROS has not loaded, refer to 6-960 for IPL problem determination.*

CC CHECK ANALYSIS FLOWCHART (PART 2)



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EREP

The EREP on-line utility program performs three basic functions for the 3705 controller:

1. EREP prints detailed, time-stamped error records of:
   A. Channel errors (NCP and EP)
   B. Unit check records (NCP and EP)
   C. MDR records (NCP)
2. EREP summarizes the statistical data generated by the subsystem.
3. EREP provides trend reporting to aid in network maintenance.

EREP should be analyzed:

1. At the time of a reported failure
2. When intermittent failures occur
3. When reviewing account data for network management

Procedures for obtaining EREP printouts vary by account.

Refer to *S370 FE EREP Reference Guide* (S229-3224) and Account Procedures to obtain EREP data.

The EREP 3705 records should be correlated with console error messages and customer reports to pinpoint failure times and causes.

The following pages in this section contain sample records:

START	101	-	Unit check record
START	102	-	BSC/SS Permanent Line Error
START	103-105	-	BSC/SS Permanent Line Error MDR decoding
START	106	-	Station Statistics
START	107	-	Permanent SDLC Link Error
START	108-110	-	Permanent SDLC Line Error MDR decoding
START	111	-	Permanent SDLC Station Error
START	112	-	Type 2 Communication Scanner Error
START	113-114	-	MDR Summary

Note: All record types are not shown.

Additional edited MDR records will contain data similar to that shown in the examples.

For unedited EREP records or additional information on MDR records not shown, see the MDR record formats on page START 053.

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EREP – UNIT CHECK RECORD

```
---RECORD ENTRY TYPE - UNIT CHECK     SOURCE - OUTBOARD            MODEL- 145       SERIAL NO.    123456

   OS/VS REL X
                          DAY YEAR          HH MM SS.TH       JOB IDENTITY ABCDEFGH
                    DATE- 103  XX      TIME- 08 09 10 11                  C1C2C3C4 C5C6C7C8

  DEVICE TYPE                        2703 (B)
  PRIMARY   CHANNEL UNIT ADDRESS     000B8 (A)
  ALTERNATE CHANNEL UNIT ADDRESS     0000008
  COMMUNICATION ADAPTER TYPE         IBM TERM I
  TERMINAL TYPE                      1050  (G)

                  (C)  CC   CA    FL     C1                K    CA   US CS  CT
    FAILING CCW        02 004000 40 00 0088            CSW F0 03EFF8 0E 00 0008


    UNIT STATUS (E)            CHANNEL STATUS (D)          STATISTICAL DATA (H)      STATISTICAL DATA

  ATTENTION          0        PRGM-CTLD TRPT   0          TEMPY READS      000      TEMPY WRITES     015
  STATUS MODIFIER    0        INCORRECT LENGTH 0          INTRVN REQD      000      BUS OUT CHK      015
  CONTROL UNIT END   0        PROGRAM CHECK    0          EQUIP CHK        000      OVERRUN          015
  BUSY               0        PROTECTION CHECK 0          LOST DATA        000      TIME OUT         015
  CHANNEL END        1        CHAN DATA CHECK  0          NOT USED         000      NOT USED         006
  DEVICE END         1        CHAN CTL CHECK   0          NOT USED         000      NOT USED         006
  UNIT CHECK         1        I/F CTL CHECK    0          NOT USED         000      NOT USED         006
  UNIT EXCEPTION     0        CHAINING CHECK   0          NOT USED         000      CHAN DATA CHK    006

  SENSE BYTE DATA (F)

BYTE 0    06

CMND REJ  0
INTV REQD 0
BUS C CHK 0
EQUIP CHK 0
DATA CHK  0
OVERRUN   1
RECEIVING 1
TIME OUT  0


   HEX DUMP OF RECORD
   HEADER     30550800   00000000   0071103F   08091011        00123456   01300000

       0018   01020304   05060708   09004000   40000088        F003EFF8   DEB00008   00000103   01004013
       0038   00000003   0F0F0F0F   0F0F0F0F   06060606        06060606   06060606
```

EREP UNIT CHECK RECORD

The EREP unit check records should be correlated with console error messages and customer reports to pinpoint failure times and causes.

To analyze a unit check record:

1. Determine if the channel unit address (A) is the NSC (native subchannel) or ESC (emulation subchannel) address.
2. Determine the device type (B) (3705 or emulated device)
3. Check the CCW for the command code (C) (see page START 061).
4. Check the channel status (D) and/or unit status (E) for error indications.
5. Check the sense byte (F):

NSC = Use Type 1/4 CA sense bit definition (see page START 061)

ESC = Determine terminal type (G)

For Start/Stop (see page START 062)
For BSC (see page START 064)

Note 1: Statistical data (H) is accumulated in the access method (program counters).

EREP – PERMANENT LINE ERROR MDR

Recording Mode '00'

The EREP MDR records should be correlated with console error messages and customer reports to pinpoint failure times and causes.

To analyze an MDR record with a recording mode of '00'

1. Verify the resource I.D. (A).
2. Verify the 3705 channel unit address (B).
3. Verify the LIB address (C).
4. Check the IOB command (D).

1(1) IOBCMAND	X'00'	I/O command field.
	X'10'	No I/O occurred.
	X'12'	Write initial.
	X'16'	Write continue.
	X'17'	Write recover.
	X'19'	Write delay.
	X'25'	Write.
	X'27'	Read.
	X'28'	Read delay.
	X'2A'	Read initial.
	X'83'	Read continue.
	X'8D'	Disable.
	X'8F'	Enable.
	X'94'	Dial.
	X'9B'	Write EOT.
	X'AC'	Write control.
		Read status.

5. Utilize MDR data (E) and MDR decoding flow chart (ref. START 103) to define error.

Note: *If no match is found, or if further byte/bit definition is required, refer to "Data Area Layouts" in the IBM 3704 and 3705 Program Reference Handbook (GY30-3012).*

```
---RECORD ENTRY TYPE - 3705 MDR    SOURCE - OUTBOARD                MODEL- 0168      SERIAL NO.   060009
   VS 2 REL.   03
                        DAY YEAR                      HH MM SS.TH
                  DATE- 027   78                TIME 04 54 14 58

 DEVICE TYPE          3705 (B)
 CHANNEL UNIT ADDRESS 001B
 RESOURCE I.D.        8801 (A)


 LIB ADDR.            022 (C)
 TERMINAL NAME        LLEAS71K

  BASIC TRANSMISSION UNIT
   BTU COMMAND  00              IOB COMMAND          8D (D)     IOB INITIAL ERROR STATUS   0000
   BTU MODIFIER 00              IOB MODIFIERS        0000       IOB INITIAL ERR EXT STAT   00 (E)
   BTU FLAGS    0000            IOB IMMED CTL CMMND 00          IOB STATUS                 06F4
                                                                IOB EXTENDED STATUS        00

   INITIAL ERROR STATUS 00    INITIAL ERR EXT STAT 00    LAST ERROR STATUS    06    LAST ERR EXT STAT    00
      FIRST BYTE                                             FIRST BYTE
   EXTENDED ERR STAT FLG 0    OVERRUN/UNDERRUN FLAG 0    EXTENDED ERR STAT FLG 0    OVERRUN/UNDERRUN FLAG 0
   FORMAT EXCEPTION FLAG 0    LINE QUIET TIMEOUT FG 0    FORMAT EXCEPTION FLAG 0    LINE QUIET TIMEOUT FG 0
   SYNC CHECK FLAG       0    LEADING DLE FORMAT CH 0    SYNC CHECK FLAG       0    LEADING DLE FORMAT CH 0
   DATA CHECK FLAG       0    SUB BLOCK ERROR FLAG  0    DATA CHECK FLAG       0    SUB BLOCK ERROR FLAG  0
   PH    ER              0    UNUSED                0    PH    ER              0    UNUSED                0
     AS    RO            0    UNUSED                0      AS    RO            1    UNUSED                0
       E     R           0    UNUSED                0        E     R           1    UNUSED                0
   LENGTH CHECK FLAG     0    UNUSED                0    LENGTH CHECK FLAG     0    UNUSED                0

  SIO COUNTER 0000  TEMPORARY ERROR COUNTER 00

  2770                                    00
   HEX DUMP OF RECORD
   HEADER    91830800    058A0000    0078027F    04541458        01060009    01680588

       0018  001BD3D3    C5C1E2F7    F1D28801    00A00005        00000000    8D000000    06F40000    00000000
       0038  00000000    00000000    00000000    00
```

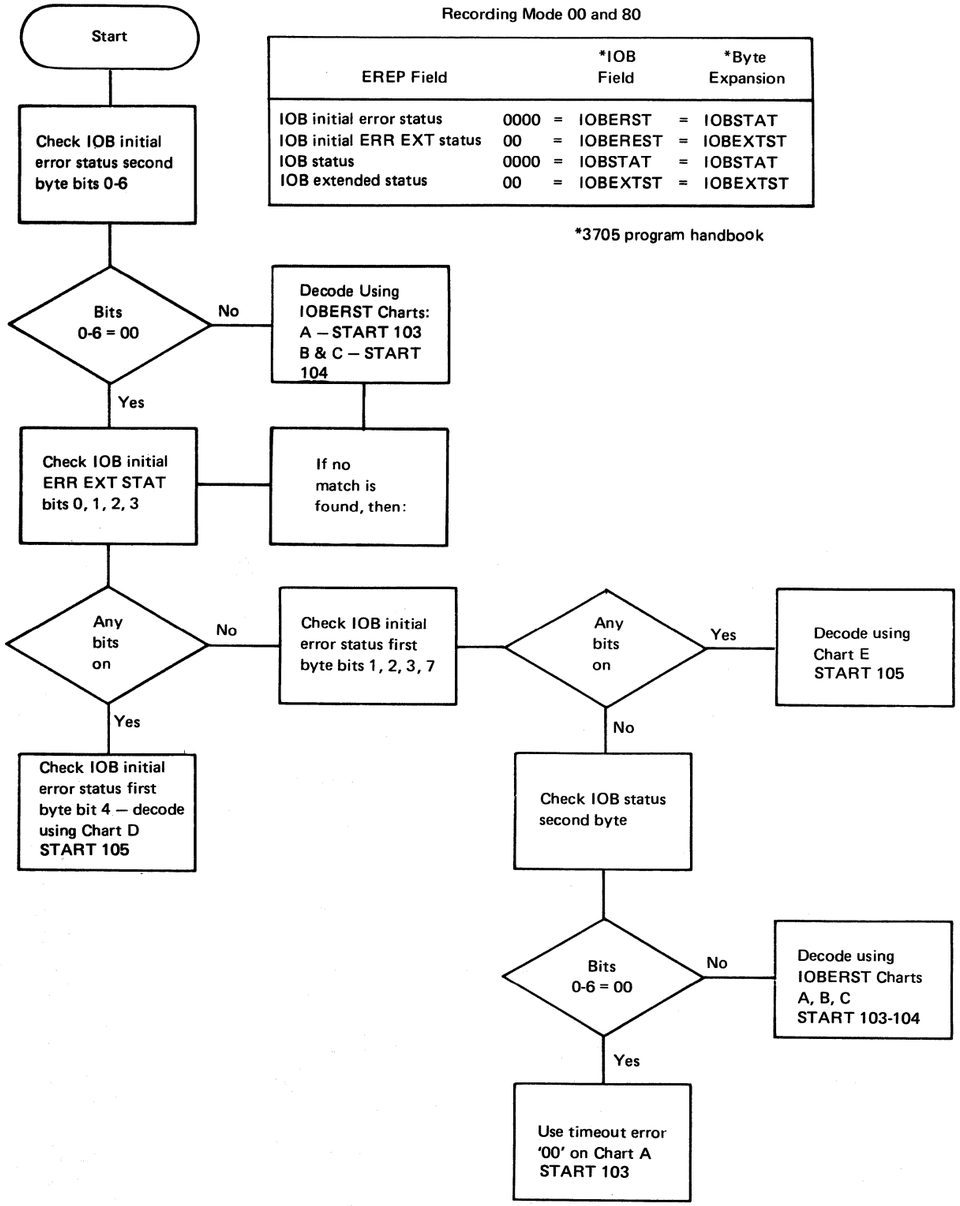
MDR

Record Format for Permanent Line Errors

		0(0) LINE Interface Address			2(2) Recording *** Mode = X'00'	3(3) Record ID = X'05'
4(4) BTU Command (BCHCMD)*	5(5) BTU Modifier (BCHMOD)*	6(6) BTU Flags (BCHSFLAG)*		8(8) IOB Command (IOBCMAND)*	9(9) IOB Modifiers (IOBCMODS)*	11(B) IOB Immediate Control Command (IOBIMCTL)*
12(C) IOB Status (IOBSTAT)*		14(E) IOB Extended Status (IOBEXTST)*	15(F) IOB Initial Error Status (IOBERST)*		17(11) IOB Initial Error Extended Status (IOBEREST)*	18(12) I/O Counter (DVBSDRT)*
20(14) Temporary Error Counter (DVBSDRC)*	21(15) 2740 Graphic Response Byte**	22(16) Device Features (DVBFEAT1)	(DVBFEAT2)	24(18) Device Type (DVBTYPE)*		

*Indicates the control block field from which this MDR record field is loaded. (See "Data Area Layout" section for field definitions.)
**2740 graphic response byte is zeroed if not applicable.
***Applies to BSC/SS devices as well as lines.

PERMANENT BSC/SS LINE ERROR—MDR DECODING



Recording Mode 00 and 80

EREP Field		*IOB Field		*Byte Expansion
IOB initial error status	0000 =	IOBERST	=	IOBSTAT
IOB initial ERR EXT status	00 =	IOBEREST	=	IOBEXTST
IOB status	0000 =	IOBSTAT	=	IOBSTAT
IOB extended status	00 =	IOBEXTST	=	IOBEXTST

*3705 program handbook

Chart A

IOBERST Second Byte Bits 0-6	Error	Probable Cause	Error Description
00,20 40,60	Timeout	Communications/ Secondary Failure	Timeout -Some character(s) have been received.
04,24 44,64	Cutoff	Communications/ Secondary Failure	Cutoff - Control length field was too long.
06,26 46,66	Abort	Communications/ Secondary Failure	Abort-Reply to transmitted data was an ENQ.
08,28 48,68	Text in Control Mode	Communications/ Secondary Failure	Text received in control mode. (No SOH, STX, or Circle D)
0A,2A 4A,6A	DLE Control End	Communications/ Secondary Failure	DLE Control End -Undefined or DLE and character sequence was received.
0C,2C 4C,6C	Wrong ACK	Secondary Failure	Wrong ACK -Received wrong ACK.
0E,2E 4E,6E	Negative Ack	Communications/ Secondary Failure	Negative ACK - Negative ACK was received.
10,30 50,70	Received Sub-Block	Secondary Failure	Received Sub-Block End - Received sub-block has ended before the end of the transmission block.
1E,3E 5E,7E	Wack	Secondary Failure	Wack - Received wack.
80	Timeout	Communications/ Secondary Failure	Timeout - nothing received.
82	Command Reject	Program Failure	Command Reject - Command could not be carried out because of specification error.
84	Buffer Depleted	Program Failure	Buffer Depleted - Level 2 and 3 buffer pools depleted.
88	DLE/EOT	Secondary Failure	DLE/EOT - Received disconnect signal.

Chart B

IOBERST Second Byte Bits 0-6	Error	Probable Cause	Error Description
8A	Data Not Expected	Communications/ Secondary Failure	Data Not Expected - Data was received when it was not expected.
8C	Reset	Program Failure	Reset - Immediate XIO command has caused the current command to end prematurely.
90	Transmit Sub-block End	Program Failure	Transmit Sub-Block End - Sub-block being sent has ended before the end of the transmission block.
92	EOT Sent After Wack	Secondary Failure	EOT Sent After Wack - The command ended when EOT was sent, after the Wack reply was received.
94	Break In Text	Communications/ Secondary Failure	Break in Text - Break was received while receiving text.
96	Poll Stop	Secondary Failure	Poll Stop-Dev. was polled to the polling limit and responded negatively.
9A	Break In Transmit	Secondary Failure	Break in transmit - Break was received while in the process of transmitting. (normal operation)
9C	Discon-nected	Host Program Failure	Disconnected - Command issued to a line that is disabled.
E0	User Error	Program Failure	User Error - Normally indicates an incorrect NCP generation. (MTA)
E4	Scanner Check	Hardware Failure	Scanner Failure-Indicates Level 1 Communication Scanner Check occurred.
E8	Adapter Check	Hardware Failure	Adapter Check - Communications line adapter check occurs when level 2 interrupt not received.

Chart C

IOBERST Second Byte Bits 0-6	Error	Probable Cause	Error Description
EA	Adapter Feedback Check	Hardware Failure	Adapter Feedback Check - Communication adpt. feed-back check has occurred.
EC	Equipment Check	Hardware Failure	Equipment Check - Operation ended because of a 370X hardware failure.
F0	Modem Error	Modem Interface Failure	Modem Error - DSR or CTS drops during command operation.
F2	Modem Clock Error	Modem Interface Failure	Modem Clock Error - When in transmit mode and the first character cannot be transmitted.
F4	DSR - On Check	Modem Interface Failure	DRS-On Check - For leased lines, indicates DSR did not come up within 3 seconds after DTR.
F8	DSC - Off Check	Modem Interface Failure	DSR-Off Check - Indicates DSR did not drop within 3 seconds of DTR dropping.
FC	ACU Check	Modem Interface Failure	ACU Check - No response from ACU.
FE	Program Failure	Program Failure	Program Failure - A negative data length was computed.

Chart D

IOBEREST Bit	Error	IOBERST first Byte	Probable Cause	Error Description
0=1	Underrun	4=1	Program/Hardware Failure	Underrun - Character transmitted more than once.
	Overrun	4=0	Program/Hardware Failure	Overrun - Receive character overlayed.
1=1	Line Quiet Timeout	N/A	Communications Failure	Line quiet Timeout - Data still being received after block ends.
2=1	DLE Format Exception	N/A	Secondary Failure	DLE Format Exception - Invalid DLE line control sequence.
3=1	Sub-Block Error Flag	N/A	Communications/ Secondary Failure	Sub-block Error Flag - Error recovery failed to retry a recoverable error.

Chart E

IOBERST First Byte	Error	Probable Cause	Error Description
3=1	Data Check	Communications Failure	Data Check - Block check character error.
1=1	Format Exception	Secondary Failure	Format Exception - bad line control sequence.
2=1	Sync Check	Communications Failure	Sync Check-Stop bit error (start/stop only).
7=1	Length Check	Host Program	Length Check - Ending character detected before count exhausted. (Transmit)

EREP – STATION STATISTICS MDR

Recording Mode '01'

```
---RECORD ENTRY TYPE - 3705 MDR    SOURCE - OUTBOARD                MODEL- 0168      SERIAL NO.   060009
   VS 2 REL.   03
                        DAY YEAR                          HH MM SS.TH
                  DATE- 033   78                    TIME 19 01 28 77
                        (B)
 DEVICE TYPE          3705
 CHANNEL UNIT ADDRESS 013
 RESOURCE I.D.        A004 (A)


 LIB ADDR.            0020 (C)
 TERMINAL NAME        DE2

  BASIC TRANSMISSION UNIT                    (D)                                              (E)
   BTU COMMAND  00              IOB COMMAND          00        IOB INITIAL ERROR STATUS   0000
   BTU MODIFIER 00              IOB MODIFIERS        0000      IOB INITIAL ERR EXT STAT   00
   BTU FLAGS    0000            IOB IMMED CTL CMMND  00        IOB STATUS                 0000
                                                               IOB EXTENDED STATUS        00

   INITIAL ERROR STATUS 00    INITIAL ERR EXT STAT 00    LAST ERROR STATUS    00    LAST ERR EXT STAT    00
      FIRST BYTE                                            FIRST BYTE
   EXTENDED ERR STAT FLG 0    OVERRUN/UNDERRUN FLAG 0    EXTENDED ERR STAT FLG 0    OVERRUN/UNDERRUN FLAG 0
   FORMAT EXCEPTION FLAG 0    LINE QUIET TIMEOUT FG 0    FORMAT EXCEPTION FLAG 0    LINE QUIET TIMEOUT FG 0
   SYNC CHECK FLAG       0    LEADING DLE FORMAT CH 0    SYNC CHECK FLAG       0    LEADING DLE FORMAT CH 0
   DATA CHECK FLAG       0    SUB BLOCK ERROR FLAG  0    DATA CHECK FLAG       0    SUB BLOCK ERROR FLAG  0
   PH    ER              0    UNUSED                0    PH    ER              0    UNUSED                0
     AS    RO            0    UNUSED                0      AS    RO            0    UNUSED                0
       E     R           0    UNUSED                0         E     R          0    UNUSED                0
   LENGTH CHECK FLAG     0    UNUSED                0    LENGTH CHECK FLAG     0    UNUSED                0

  SIO COUNTER 03C6  TEMPORARY ERROR COUNTER 00 (F)

  2770                                      00
   HEX DUMP OF RECORD
   HEADER    91830800    058A0000    0078033F    19012877        01060009    01680588

       0018  001BC4C5    F2404040    4040A004    00200105        00000000    00000000    00000000    000003C6
       0038  00001007    4C3C407E    601DE8C3    D6

****************END OF SAMPLE REPORT*************
```

The EREP MDR Records should be correlated with console error messages and customer reports to pinpoint failure times and causes.

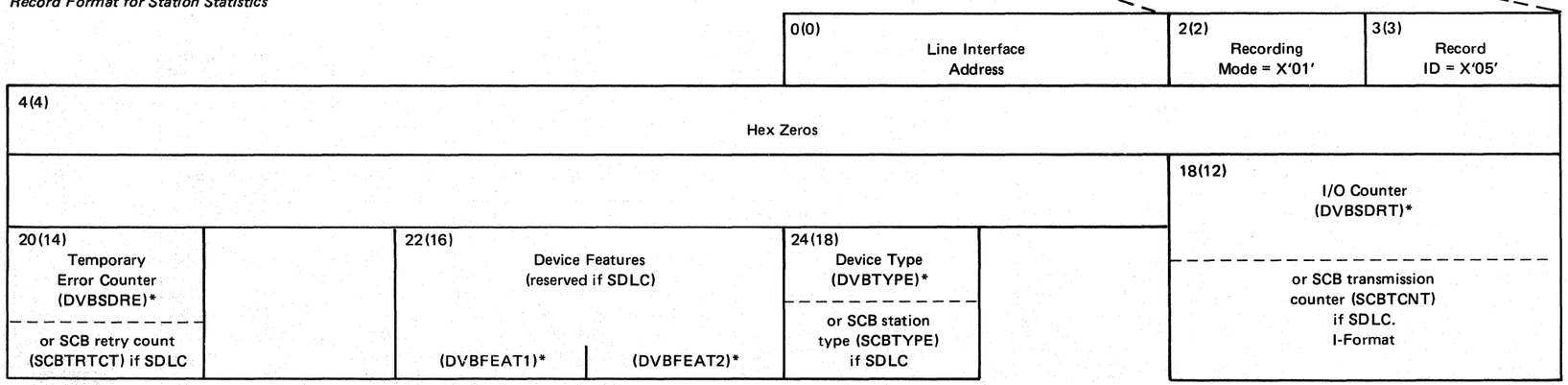
To analyze an MDR record with a recording mode of '01':

1. Verify the resource ID (A).
2. Verify the channel unit address (B).
3. Verify the LIB address (C).
4. Note that the command field (D) and status fields (E) are 'zeroes'.
5. Review counter fields (F) for station statistics.

Note: If further byte/bit definition is required, refer to "Data Area Layouts" in the *IBM 3704 and 3705 Program Reference Handbook,* GY30-3012.

MDR

Record Format for Station Statistics



*Indicates the control block field from which the MDR record field is loaded. (See "Data Area Layouts" section for field definitions.)

EREP – PERMANENT SDLC LINK ERROR MDR

Recording Mode '02'

```
---RECORD ENTRY TYPE - NCP MDR     SOURCE - OUTBOARD                MODEL- 0168      SERIAL NO.   060157
   VS 1 REL.   07
                      DAY YEAR                        HH MM SS.TH
                  DATE- 144   80                TIME 07 58 06 64

 DEVICE TYPE          3705 (B)
 CHANNEL UNIT ADDRESS 0021
 RESOURCE I.D.        303C (A)

 NETWORK ADDRESS      303C      NETWORK NAME AMBSDLC2

 RECORD TYPE - PERMANENT SDLC LINK ERROR

 SUSPECTED MODEM INTERFACE ERROR

 LIB ADDR             0024 (C)

  LINK INFORMATION

   CCB CONTROL FLG            00       LXB COMMAND                30 (D)  LXB FINAL ERROR STATUS    (E)  12F0
   CCB LINE TYPE              41       LXB MODIFIERS              0000    LXB FINAL ERR EXT STATUS       00
                                       LXB IMMED. CTL CMD         00      LXB INITIAL ERROR STATUS       0000
                                                                          LXB INITIAL ERR EXT STATUS     00

   FINAL ERR BIT DECODE       FINAL ERR EXT STAT        INITIAL ERR BIT DECODE     INITIAL ERR EXT STAT

   EXTENDED ERR STAT FLG 0    OVERRUN/UNDERRUN FLAG 0   EXTENDED ERR STAT FLG 0    OVERRUN/UNDERRUN FLAG 0
   FORMAT EXCEPTION FLG  0    BLOCK OVERRUN         0   FORMAT EXCEPTION FLG  0    BLOCK OVERRUN         0
                         0    ABORT                 0                         0    ABORT                 0
   DATA CHECK            1    MONITOR COUNT OVERFLO 0   DATA CHECK            0    MONITOR COUNT OVERFLO 0
   SDLC POLL FINAL BIT   0                              SDLC POLL FINAL BIT   0


   HEX DUMP OF RECORD
   HEADER    91470800    15000000    008C144F    07580664        01060157    01680588

       0018  0021C1D4    C2E2C4D3    C3F23C3C    00240205        01000000    00000000    30000000    12F00000
       0038  00000000    00000000    00D10000    00000041        00000000    00000000    00000000    00000000
       0058  02C1C3C6    D5C3D7F0    F10C0000    00000000        00000000    00000000    00
```

Record Format for Permanent SDLC Errors

The EREP MDR records should be correlated with console error messages and customer reports to pinpoint failure times and causes.

To analyze an MDR record with a recording mode of '02':

1. Verify the Resource ID (A).
2. verify the channel unit address (B).
3. Verify the LIB address (C).
4. Check the LXB command (D).

1(1) LXBCMAND	X	LXB command:
	X'00'	No I/O occurred
	X'83'	Disable.
	X'8D'	Enable
	X'8F'	Dial
	X'30'	Run SDLC Link
	X'32'	Run Initial

5. Utilize MDR data (E) and MDR decoding flow chart (see page START 108) to define the error.

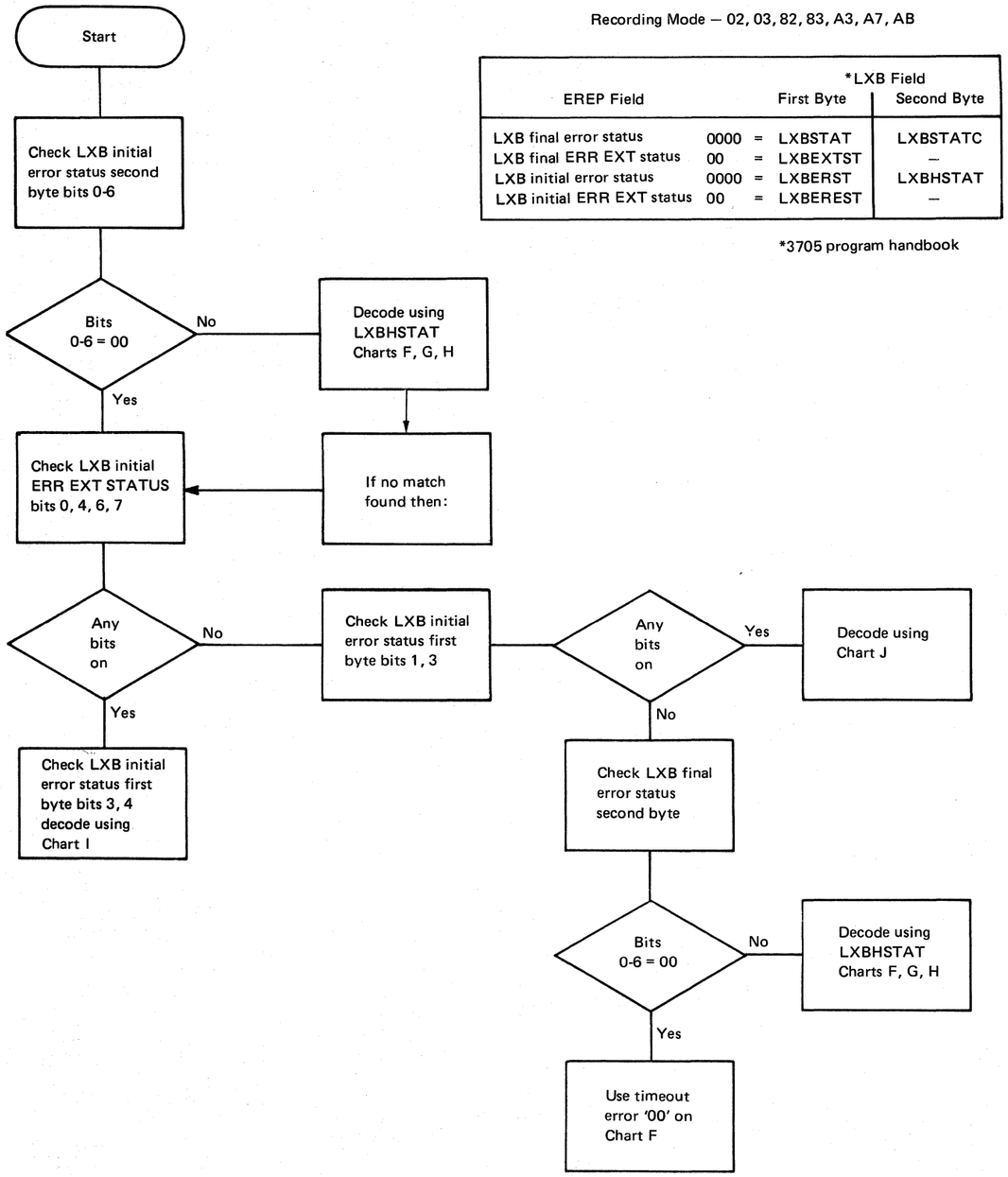
Note: If no match is found, or if further byte/bit definition is required, refer to "Data Area Layouts" in the *IBM 3704 and 3705 Program Reference Handbook,* GY30-3012.

0(0) Line Interface Address		2(2) Recording Mode X'03' = Station Error X'02' = Link Error	3(3) Record ID X'05'

4(4) * SCB Service Seeking Command Flags (SCBSSCF)	6(6) * Output Control Flag (SCBOCF)	7(7) Reserved	8(8) LXB Command (LXBCMAND)	9(9) LXB Modifiers (LXBCMODS)		11(B) LXB Immediate Control Cmd. (LXBIMCTL)
12(C) LXB Final Error Status *2* (LXBSTAT) LXBSTAT / LXBSTATC	14(E) LXB Final Error Extended Status (LXBEXTST)	15(F) LXB Initial Error Status *3* (LXBERST) LXBERST / LXBHSTAT		17(11) LXB Initial Error Extended Status (LXBEREST)	18(12) * SCB Transmission Counter (SCBTCNT) I-Format	
20(14) * SCB Retry Count (SCBTRTCT)	21(15) Received BLU Command Field (LXBRBLUC)	22(16) Reserved	24(18) * SCB Station Type (SCBTYPE)	25(19) ** Transmit BLU Command Field (CCBCFLD)	26(1A) * SCB Current Outstanding Count (SCBCOC)	27(1B) * SCP Pass Count (SCBPCNT)
28(1C) * SCB Receive Count (SCBNR) (Bits 4,5,6)	29(1D) * SCB Send Count (SCBNS) (Bits 4,5,6)	30(1E) CCB Control Flags and Line Type CCBCTL) CCBRSPON Control Flags / CCBTYPE Line Type	32(20) *** Command Field Received From Secondary Station. SECCFR	33(21) *** N(R) and N(S) Received From Secondary Station.	34(22) *** Command Reject Reason: X'08' = Invalid N(R). X'04' = Frame too long. X'02' = Data received in S or NS format. X'01' = Invalid command.	

*This field is present only if this record is for a station (for a link, field contains all zeros).
**This field stored only for duplex links.
***This field stored only if Command Reject was the cause of the MDR record being formatted.
*2*Last error recognized.
*3*First error recognized.

PERMANENT SDLC LINE ERROR—MDR DECODING



Recording Mode — 02, 03, 82, 83, A3, A7, AB

EREP Field			*LXB Field First Byte	*LXB Field Second Byte
LXB final error status	0000	=	LXBSTAT	LXBSTATC
LXB final ERR EXT status	00	=	LXBEXTST	—
LXB initial error status	0000	=	LXBERST	LXBHSTAT
LXB initial ERR EXT status	00	=	LXBEREST	—

*3705 program handbook

Chart F

LXBHSTAT Bits 0-6	Error	Probable Cause	Error Description
00	Timeout	Communications/ Secondary Failure	Timeout - Received RR, RNH or REJ.
0C	Partial or Negative Acknowl- edgement	Communications/ Secondary Failure	Partial or Negative Acknowl- edgement - Sequence number did or did not change.
0E	SDLC REJ. Received	Secondary Failure	SDLC REJ Received - Line is not duplex-format exception
1C	SDLC RR Received	Secondary Failure	SDLC RR Received - Received RR in NS phase - format exception.
1E	SDLC XID Received	Secondary Failure	SDLC XID Received -Received XID in RR or RNR phase - format exception.
20	Timeout	Communications/ Secondary Failure	Timeout - Received address and control fields.
24	Buffer Cutoff	Program Failure	Buffer Cutoff - Exceeded buffer limit.
2C	Partial or Negative Acknowl- edgement	Communications/ Secondary Failure	Partial or Negative Acknowl- egement - Sequence number did or did not change.
60	Timeout	Communications/ Secondary Failure	Timeout - Flag received.
62	SDLC Com- mand Reject Received	Communications/ Failure	SDLC Command Reject Re- ceived displacement: X'YY'=08 Invalid N(R) 04 Frame too long 02 Data in S or NS Format 01 Invalid command

Chart G

LXBHSTAT Bits 0-6	Error	Probable Cause	Error Description
64	Buffer Cutoff	Program Failure	Buffer Cutoff - Exceeded buffer limit.
80	Timeout	Communications/ Secondary Failure	Timeout - Nothing received.
84	Buffer pool Depleted	Program Failure	Buffer Pool Depleted -No more buffers available.
8C	Reset	Program Failure	Reset - End Run Command.
8E	Invalid Address	Secondary Failure	Invalid Address - received from secondary.
96	Poll Stop	Secondary Failure	Poll Stop- Device was polled to the polling limit and responded negatively.
9C	Disabled	Host Program Failure	Disabled -Command issued to a line that is disabled.
A0	Timeout	Communications/ Secondary Failure	Timeout - Received flag.
A2 and LXBERST Byte 0.1 =1	Received Invalid SDLC Command	Secondary Failure	Received Invalid SDLC Command - Format Exception
A4	Invalid N(R) Count	Program/Secondary Failure	Invalid N(R) Count -Received invalid (incongruous N(R) in I or S format.
A6	Link Activity Timeout	Primary Communications Failure	Link Activity Timeout - No flags received (remote NCP only).
A8 and LXBERST Byte 0.1 =1	Received SDLC DISC	Secondary Failure	Received SDLC DISC - Format exception.

Chart H

LXBHSTAT Bits 0-6	Error	Probable Cause	Error Description
AC and LXBERST Byte 0.1 =1	Received SDLC SNRM	Secondary Failure	Received SDLC SNRM - Format exception.
B6 and LXBERST Byte 0.1 =1	Received SDLC ROL	Secondary Failure	Received SDLC ROL - Format exception. Can be caused by system reset at the secondary.
BC and LXBERST Byte 0.1 =1	Received SDLC NSA	Secondary Failure	Received SDLC NSA in RR or RNR Phase - format exception.
E8	Adapter Check	Hardware Failure	Adapter Check - Communications line adapter check occurs when level 2 interrupt not received.
EA	Adapter Feedback Check	Hardware Failure	Adapter Feedback Check - Communication adapter feedback check has occurred.
F0	Modem Error	Modem Interface Failure	Modem Error-DSR or CTS drops during command operation.
F2	Transmit Clock or CTS Failure	Modem Interface Failure	Transmit Clock or CTS failure
F4	DSR - On Check	Modem Interface Failure	DSR - On Check - For leased lines indicates DSR does not come up within 3 seconds after DTR.
F8	DSR - Off Check	Modem Interface Failure	DSR - Off Check - DSR fails to drop during a disable operation.
FC	ACU Check	Modem Interface Failure	ACU Check - Incorrect Auto Call Interface sequence.
FE	Program Failure	Program Failure	Program Failure - Negative data length was computed.

Chart I

LXBEREST bit	Error	LXBERST bit	Probable Cause	Error Description
0=1	Underrun	4=1	Program/ Hardware Failure	Underrun-Character transmitted more than once.
0=1	Overrun	4=0 3=0	Program/ Hardware Failure	Overrun - Received character overlayed
0=1	Frame Check Sequence Error	4=0 3=1	Communications Failure	Frame Check Sequence Error - (Data Check)
4=1	Block Overrun		Program Failure	Block Overrun-Level 3 block processing in progress when another block available from level 2.
6=1	Abort Received		Communications/ Secondary Failure	Abort Received - Eight consecutive 1 bits received.
7=1	Monitor Count Overflow		Communications/ Secondary Failure	Monitor Count Overflow - 64 temporary I-format receive errors have occurred.

Chart J

LXBERST	Error	Probable Cause	Error Description
3=1	Frame Check Sequence Error	Communications Failure	Frame Check Sequence Error- (Data Check).
1=1	Format Exception	Secondary Failure	Format Exception - Invalid SDLC format.

EREP — PERMANENT SDLC STATION ERROR MDR

Recording Mode '03'

The EREP MDR records should be correlated with console error messages and customer reports to pinpoint failure times and causes.

To analyze an MDR record with a recording mode of '03'

1. Verify the resource I.D. (A).
2. Verify the channel unit address (B).
3. Verify the LIB address (C).
4. Check the LXB command (D).

1(1)		LXB command:
LXBCMAND	X'00'	No I/O occurred.
	X'83'	Disable.
	X'8D'	Enable.
	X'8F'	Dial.
	X'30'	Run SDLC link.
	X'32'	Run Initial.

5. Utilize MDR data (E) and MDR decoding flow chart (ref. START 108) to define error.

Note: *If no match is found, or if further byte/bit definition is required, refer to "Data Area Layouts" in the IBM 3704 and 3705 Program Reference Handbook (GY30-3012).*

```
---RECORD ENTRY TYPE - 3705 MDR    SOURCE - OUTBOARD                  MODEL- 0168      SERIAL NO.   060009
   VS 2 REL.   03
                        DAY YEAR                    HH MM SS.TH
                  DATE- 031   78              TIME 13 06 13 92

 DEVICE TYPE          3705 (B)
 CHANNEL UNIT ADDRESS 011C
 RESOURCE I.D.        9895 (A)

 NETWORK ADDRESS      9895      NETWORK NAME PUSW1E

 RECORD TYPE - PERMANENT SDLC LINE ERROR

 LIB ADDR             002C (C)

  LINK INFORMATION

   CCB TYPE CONNECTION FLG    00       LXB COMMAND          (D) 30       LXB LAST ERROR STATUS      (E) 06F0
   CCB TYPE FLAGS             21       LXB MODIFIERS            0000     LXB LAST ERR EXT STATUS        00
                                       LXB IMMED. CTL CND.      00       LXB FIRST ERROR STATUS         0000
                                                                         LXB FIRST ERR EXT STATUS       00

   LAST ERR BIT DECODE        LAST ERR EXT STAT          FIRST ERR BIT DECODE       FIRST ERR EXT STAT

   EXTENDED ERR STAT FLG 0    OVERRUN/UNDERRUN FLAG 0    EXTENDED ERR STAT FLG 0    OVERRUN/UNDERRUN FLAG 0
   FORMAT EXCEPTION FLG  0    BLOCK OVERRUN         0    FORMAT EXCEPTION FLG  0    BLOCK OVERRUN         0
   CHAR SYNC CHECK       0    ABORT                 0    CHAR SYNC CHECK       0    ABORT                 0
   DATA CHECK            0    MONITOR COUNT OVERFLO 0    DATA CHECK            0    MONITOR COUNT OVERFLO 0
   SDLC POLL FINAL BIT   0                               SDLC POLL FINAL BIT   0

 LOCAL PRI STATION INFORMATION

   SCB DEVICE TYPE            22
   SCB LINK SCHEDULING FLGS   0001
   SCB OUTPUT CONTROL FLAGS   81
   IMTD BLU CMD FLD           00
   RCVD BLU CMD FLD           00
   N (R)                      01
   N (S)                      01
   SCB BLKS OUTSTANDING CNT   000
   SCB PASS COUNT             007
   SCB I-FORMAT TRANSMIT CNT  000017
   SCB IMIT TEMP ERR COUNT    002

   HEX DUMP OF RECORD
   HEADER    91830800    058A0040    0078031F    13061392          01060009    01680588

       0018  011CD7E4    E2E6F1C5    40409895    002C0305          00018100    30000000    06F00000    00000011
       0038  02000000    22000007    22220021    00000000          00000000    000000
***************END OF SAMPLE REPORT***************
```

Record Format for Permanent SDLC Errors

0(0) Line Interface Address					2(2) Recording Mode. X'03' = Station Error X'02' = Link Error	3(3) Record ID. X'05'
4(4) * SCB Service Seeking Command Flags (SCBSSCF)	6(6) * Output Control Flag (SCBOCF)	7(7) Reserved	8(8) LXB Command (LXBCMAND)	9(9) LXB Modifiers (LXBCMODS)		11(B) LXB Immediate Control Cmd. (LXBIMCTL)
12(C) LXB Final Error Status *2* (LXBSTAT) LXBSTAT / LXBSTATC	14(E) LXB Final Error Extended Status (LXBEXTST)	15(F) LXB Initial Error Status *3* (LXBERST) LXBERST / LXBHSTAT		17(11) LXB Initial Error Extended Status (LXBEREST)	18(12) * SCB Transmission Counter (SCBTCNT) I-Format	
20(14) * SCB Retry Count (SCBTRTCT)	21(15) Received BLU Command Field (LXBRBLUC)	22(16) Reserved		24(18) * SCB Station Type (SCBTYPE)	25(19) ** Transmit BLU Command Field (CCBCFLD)	26(1A) * SCB Current Outstanding Count (SCBCOC)	27(1B) * SCP Pass Count (SCBPCNT)
28(1C) * SCB Receive Count (SCBNR) (Bits 4,5,6)	29(1D) * SCB Send Count (SCBNS) (Bits 4,5,6)	30(1E) CCB Control Flags and Line Type CCBCTL) CCBRSPON Control Flags / CCBTYPE Line Type		32(20) *** Command Field Received From Secondary Station SECCFR	33(21) *** N(R) and N(S) Received From Secondary Station	34(22) *** Command Reject Reason: X'08' = Invalid N(R). X'04' = Frame too long. X'02' = Data received in S or NS format. X'01' = Invalid command.	

*This field is present only if this record is for a station (for a link, field contains all zeros).
**This field stored only for duplex links.
***This field stored only if Command Reject was the cause of the MDR record being formatted.
*2*Last error recognized.
*3*First error recognized.

EREP – TYPE 2 COMMUNICATION SCANNER ERROR MDR

Recording Mode '11'

```
---RECORD ENTRY TYPE - 3705 MDR    SOURCE - OUTBOARD                  MODEL- 0168      SERIAL NO.   060009
   VS 2 REL.   03

                        DAY YEAR                    HH MM SS.TH
                  DATE- 002   78                TIME 08 13 52 39

 DEVICE TYPE          3705  (B)
 CHANNEL UNIT ADDRESS 001A
 RESOURCE I.D.        9000  (A)

 TYPE 2 CRECORD TYPE - UNKNOWN - IFCETRN1
 RECORD TYPE - COMMUNICATION SCANNER TYPE 2 CSB1 (C)  ABEND CODE 0000

    LAGGING ADDRESS REG 74     000011DE          INTERRUPTED LEVEL IAR         000011E2
    EXTERNAL REGISTER 79       0043        (D)

        COMMUNICATIONS SCANNER STATUS 43=       0200

          LIB POS 1 BIT CLOCK CHECK          0
          LIB POS 2 BIT CLOCK CHECK          0
          LIB POS 3 BIT CLOCK CHECK          0
          LIB POS 4 BIT CLOCK CHECK          0
          LIB POS 5 BIT CLOCK CHECK          0
          LIB POS 6 BIT CLOCK CHECK          0
          LIB SELECT CHECK                   1  (E)
          ICW IN REGISTER CHECK              0
          ICW WORK REGISTER CHECK            0
          PRIORITY REGISTER AVAILABLE CHECK  0
          CCU OUTBUS CHECK                   0
          LINE ADBUS CHECK                   0
          UNUSED                             0
          UNUSED                             0

 HEX DUMP OF RECORD

 HEADER    91830800     058A0000     0060002F     08135239       01060009     01680588
     0018  001AD5C3     D7C14040     40409000     00001105       40000200     000011DE     000011E2     00430000
```

MDR

Record Format for Type 2 Communication Scanner Errors

			0(0) Abend/Malfunction Code	2(2) Recording Mode = X'11'	3(3) Record ID = X'05'
4(4) Error Record Type*	5(5) Lost Check Record Count (CRPLCRCT)	6(6) External Register X'43' Check Register 1	8(8) External Register X'74' Lagging Address Register		
12(C) Interrupted Program Level's Instruction Address Register (Register 0)			16(10) External Register X'79' Program Level Interrupted		

*Type 2 Scanner 1 = X'40'
Type 2 Scanner 2 = X'20'
Type 2 Scanner 3 = X'10'
Type 2 Scanner 4 = X'08'

The ERP MDR records should be correlated with console error messages and customer reports to pinpoint failure times and causes.

To analyze any MDR record with a recording mode of 11:

1. Verify the resource ID (A).
2. Verify the channel address (B).
3. Note that the record type (C) describes the adapter failure.
4. Note that the following data (D) is recorded:
   - Input 74 - Lagging address register
   - Input 79 - Program level interrupted
   - Reg 0 - Interrupted level IAR
   - Input 43 - Check register 1
5. Verify which bit is set to indicate the error condition (E).

Note: Refer to the *3705 Principles of Operation* for detailed error description.

EREP – MDR SUMMARY

```
---SUMMARY OF ENTRY TYPE - 3705 MDR        DEVICE TYPE 3705        MODEL- 3031       SERIAL NO.  037961

              DAY YEAR     DAY YEAR
   DATE RANGE- 063   80 TO  063   80

    CHANNEL UNIT ADDRESS 00001D                  TOTAL NUMBER OF RECORDS  0021

                                                 - - - - - - - - - - PERMANENT ERROR TYPES - - - - - - - - - -
                    LIB                  TEMP     PERM                                                    MODEM/
TERM NAME   RID     ADDR   #I/O OPS      ERRORS   ERRORS     HDWR    TM OUT   DATA CK    RCV     ITV RQD   MISC    INTFC
A025        F854    002C   00000000     000000   000003     00000   00003    00000      00000   00000     00000   00000
B020        F801    002C   00000000     000000   000002     00000   00002    00000      00000   00000     00000   00000
B021        F80B    002C   00000000     000000   000001     00000   00001    00000      00000   00000     00000   00000
B022        F819    002C   00000000     000000   000001     00000   00001    00000      00000   00000     00000   00000
B023        F827    002C   00000000     000000   000001     00000   00001    00000      00000   00000     00000   00000
B024        F835    002C   00000000     000000   000001     00000   00001    00000      00000   00000     00000   00000
B025        F843    002C   00000000     000000   000001     00000   00001    00000      00000   00000     00000   00000
B101        F84E    002C   00000000     000000   000005     00000   00005    00000      00000   00000     00000   00000
D003        F84F    002C   00000000     000000   000003     00000   00003    00000      00000   00000     00000   00000
D004        F850    002C   00000000     000000   000003     00000   00003    00000      00000   00000     00000   00000
```

ERR/MDR SUMMARY

Field	*Description*
TERM NAME	Terminal name as assigned in NCP Gen.
RID	Resource ID as assigned in NCP Gen.
LIB ADDR	3705 line interface address for this line ('0000' if this error is not associated with a line).
# I/O OPS	For BSC/SS lines. A count of test blocks transmitted (including retries). The count is taken from he DVBSDRT field in the DVB (device base control block). For SDLC stations, a count of I-frames transmitted (including retries). The count is taken from the SCBTCNT field in the SCB (station control block). For SDLC Links, the count is always set to zero.
TEMP ERRORS	For BSC/SS lines, a count of error retires. The count is taken from the DVBSDRE field in the DVB (device base control block). For SDLC stations, a count of error retries. The count is taken from the SCBTRTCT field in the SCB (station control block.) For SDLC links, the count is always set to zero.
PERM ERRORS	1. Errors which have exhausted their retry error count 2. Errors which NCP considers permanent and no error recovery is attempted. A. Received SDLC frame reject response B. Received invalid SDLC command C. Adapter check D. Adapter feedback check E. Modem error F. Transmit clock or clear to send failure G. Data set ready turn on or off check H. Auto call check I. Program failure.
Permanent Error Types:	
HDWR	1. 3705 hardware failures: A. Scanner failure B. Adapter check C. Adapter feedback check D. Equipment check
TM OUT	1. No data was received from a terminal when it was expected 2. No response from the ACU (auto-call unit)
DATA CK	Block check character error (BSC); Frame check sequence error (SDLC) (errors most likely associated with line problems)
RCV	Terminal answers with incorrect response, out of sequence response or ends the operation permaturely (errors most likely associated with terminal problems)
ITV RQD	Negative acknowledgement received from terminal in control phase.
MISC	1. Program errors 2. User errors 3. "Should not occur" errors 4. Errors not categorized
MODEM/INTFC	Modem interface errors: 1. DSR or CTS drops during command operation 2. Transmit clock failure 3. DSR fails to reach an up level within 3 seconds of DTR (leased line) 4. DSR fails to drop during a disable operation. 5. Incorrect auto-call interface sequence.

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INTERNAL FUNCTIONAL TEST (IFT)

WHAT IFT DOES

IFTs are a set of diagnostic programs that help detect 3705 hardware failures. There are separate IFTs for each of the following major components of the 3705:

- Central Control Unit (CCU)
- Storage
- Type 1 or Type 4 Channel Adapter
- Type 2 Communication Scanner Base (CSB)

Note: The type 2 CSB IFT also tests the Line Interface Base (LIB) and Line Sets.

IFT consists of the following sections:

Section	CE Request and Description (see note 1)	
Z3705AAA	-	Type 1 CA Load Module (see note 2)
Z3705ACA	-	DCM
Z3705ADA	-	INIT, Section 1
Z3705AEA	-	INIT, Section 2
Z3705BAA	11RR	CCU IFT, Section 1
Z3705BBA	-	CCU IFT, Section 2
Z3705BCA	-	CCU IFT, Section 3
Z3705CAA	P2RR	Storage
Z3705DAA	P3RR	Type 1 CA IFT, Section 1
Z3705JAA	P9RR	Type 4 CA IFT, Section 1
Z3705JBA	P9RR	Type 4 CA IFT, Section 1
Z3705GBA	-	Type 2 CSB IFT, Section 2
Z3705GCA	-	Type 2 CSB IFT, Section 3
Z3705GDA	-	Type 2 CSB IFT, Section 4
Z3705GEA	-	Type 2 CSB IFT, Section 5

Note 1: CE request is the information that you must enter to run a particular IFT. See "How to Request an IFT" later in this section.

Note 2: Type 1 CA Load Module is used for both the type 1 and type 4 CA.

REQUIREMENTS

You must have the proper configuration data set (CDS) cataloged with the remainder of the system (for additional information, see the CDS section). Before IFT routines can run properly, the functional areas in the CCU hardware must be operational. These functional areas are tested by the ROS bootstrap program each time the LOAD pushbutton is pressed.

HOW IFTS ARE STRUCTURED

An IFT consists of a preface, one or more routines, subroutines, a preface for each routine, and interrupt handlers.

IFTs are loaded into 10K byte areas of storage. If an IFT is larger than 10K bytes, the IFT is divided into sequentially numbered self-contained modules called sections. Each section contains an IFT preface. Subroutines and interrupt handlers are duplicated in each section.

IFT Preface

The IFT preface is located at the beginning of each IFT section and contains: (1) the IFT number, (2) the section number, (3) the address of the preface for the first routine in the IFT, and (4) the addresses of the level I, 2, 3, and 4 interrupt handlers.

IFT Routine Preface

The routine preface is located at the beginning of each routine and contains: (1) the routine number, (2) flags that identify manual intervention and problem definition routines (3) the address of the abort subroutine, and (4) the address of the preface for the next routine in the section. For the last routine in a section, the next routine address field is X'FFFE'. For the last routine in an IFT, the next routine address field is X'FFFF'.

IFT Routines

IFT routines consist of blocks of code that provide the various test functions. The basic routine blocks are:

- Initialize Block: The initialize block is entered on the first pass through the routine and it initializes addresses, pointers, and other parameters. The initialize block also performs certain hardware operations such as adapter reset. The initialize block can be modified to alter the initial addresses, pointers, and parameters for subsequent passes.
- Program Setup Block: The program setup block prepares the other blocks of the routine for execution by setting up or modifying parameters and addresses.
- Hardware Setup Block: The hardware setup block prepares the hardware for testing by setting registers and latches according to the initial parameters.
- Pretest Block: The pretest block tests for correct hardware setup. Error codes displayed by this block indicate other routines should be run to test the hardware setup conditions.
- Set Scope Sync 2 Block: The set scope sync 2 block causes a pulse to be emitted from scope sync point 2 (01A-B3M2P13, ALD page CU015) at the beginning of each test function.
- Test Block: The test block completes the steps necessary to test the hardware. Test block causes the hardware to execute the functions being tested.
- Analysis Block: The analysis block checks the results of the test block and if an error was detected, causes the DCM to display error codes.
- Test for More Parameters Block: The test for more parameters block determines if additional test iterations are to be taken.
- Modify Block: The modify block modifies pointers and addresses for any additional iterations of the test.
- End Block: The end block terminates the routine and returns control to the DCM.

IFT EXECUTION

3705 Setup Procedures

1. Switch the 3705 power on.
2. Set both the MODE SELECT and DIAGNOSTIC CONTROL switches to the PROCESS position.
3. Enable the appropriate channel interface.
4. To load the DCM, set the DISPLAY/FUNCTION SELECT switch to the STATUS position. For information on using the other positions, see "How to Use the DISPLAY/FUNCTION SELECT Switch" later in this section.
5. Press the RESET pushbutton, then the LOAD pushbutton.
6. DISPLAY B bits 0.2 and 0.3 should be on indicating that ROS has reached IPL phase 3. The LOAD light is on; the following lights are off: HARDSTOP, TEST, WAIT, and PROGRAM STOP.

   If the above conditions are not present, refer to the CE Panel Test in the CTRL PNL section and the ROS Test in the ROS section (both sections are in Volume 2).

Host Procedures

Start the OLTEP or OLTSEP in the host processor. When OLTEP or OLTSEP causes a console printer message of:
r ID 'ENTER DEV/TEST/OPT/'

you enter:

r ID,'XXX/3705A/nfe,ext=ABCD/'

where:

XXX = the channel and unit address of the 3705 (native attachment address).

ABCD = four operating options provided by the OLT and type 1/4 CA loaders. The correct entries are Y (for YES) or N (for NO). The options are defined as follows:

- A = OLT bypass printing channel errors
- B = Run INIT
- C = Run type 1 CA loader with error checking
- D = Bypass hard stop on type 1 CA loader error in 3705 and retry

If your response to the DEV/TEST/OPT/ message does not include the ext= parameter, the default value assumed is ext=nyyy (that is, ext=NO,YES,YES,YES).

Delay of INIT Execution: Before INIT begins executing, the 3705/host interface must be disabled. The type 1 CA loader attempts to disable the 3705 interface by issuing a diagnostic DISABLE command when INIT is loaded. The host 'clock out' line must drop before the 3705 can go offline. The host 'clock out' line will drop when either the host processor STOP pushbutton is pressed or when the host processor enters the wait state.

Operating situations under OS or DOS can result in maximum use of the processor that will delay the host from entering the wait state. During this delay, the OLT prints a message indicating that it is waiting for the 3705 to disable its channel interface. Also, at the 3705, an equivalent message code is displayed in the control panel lights.

TYPE 1 LOADER ERROR PRINTOUTS

Error printouts occur if the Type 1 CA loader detects an error. The printout contains all the pertinent information about the type 1/4 CA error that can be obtained by the type 1 CA loader. The bypass printing channel errors option inhibits the error printout. For a description of the error printouts, refer to *DOS OLTEP SRL* (GC24-5086), *IBM System/360 Operating System On-line Test Executive Program* (GC28-6650), or *OLTSEP Operator's Guide* (D99-SEPDT).

MESSAGES

Messages occur during operation of the type 1 CA loader that indicate: (1) the loader has detected an error or (2) an action is needed to load the diagnostic programs into 3705 storage. The messages, message explanations, and responses are as follows:

THE STATUS OF THE 3705 CANNOT BE DETERMINED. **WARNING** CONTINUATION WILL CAUSE THE ENTIRE 3705 TO BECOME UNAVAILABLE. ENTER 'C' TO CANCEL OR 'P' TO PROCEED.

Explanation: The OLT cannot determine the status (offline or stopped) of the 3705. If the OLT is allowed to continue, the program in 3705 storage will be destroyed.

Response: Continue by entering a C or P, as follows:

r id,'C' (for cancel)
or
r id,'P' (for proceed)

Any other response results in the program repeating the last line of the above message. After five invalid responses, the message INVALID RESPONSE AFTER 5 REQUESTS is printed.

ALL 3705 ADDRESSES ARE NOT STOPPED OR OFFLINE. **WARNING** CONTINUATION WILL CAUSE THE ENTIRE 3705 TO BECOME UNAVAILABLE. ENTER 'C' TO CANCEL OR 'P' TO PROCEED, OR 'R' TO RETRY.

Explanation: The OLT has been notified by the executive driver that all 3705 addresses are not offline or stopped. If the OLT is allowed to continue, the program in 3705 storage will be destroyed.

Response: You have the opportunity to make all addresses available to the OLT using standard system facilities. Continue by entering a C, P, or R, as follows:

r id,'C' (for cancel)
or
r id,'P' (for proceed)
or
r id,'R' (for retry)

The difference between a 'P' and "R" response is (1) P means to proceed, regardless of the offline or online status of the 3705 address and (2) R means that the operator has been taking addresses offline and wants the program to verify that all units are now available to the OLT.

Any other response results in the program repeating the last line of the above message. After five invalid responses, the message INVALID RESPONSE AFTER 5 REQUESTS is printed.

INVALID RESPONSE AFTER 5 REQUESTS

Explanation: The program assumed the response of 'C' and terminated the OLT.

Response: None.

BAD RC YY FROM XXXXXXX

Explanation: The type 1 CA loader has requested a function of the executive driver which the driver is incapable of performing. This may be because of an invalid parameter or an error that occurred while the executive driver was performing the request. XXXXXXX is the name of the function being requested, and YY is the code returned by the executive program. The XXXXXXX field is filled by the type 1 CA loader.

Response: This message is a diagnostic programming aid. If it occurs, a dump and other available information should be submitted with an APAR (Authorized Program Analysis Report).

The following messages are printed on the system output printer to describe failures and the operation that was being attempted when an error occurred:

BAD CC SIO

FAILED TO INTRPT

BAD STATUS ON SIO

NOP CMD FOR 3705 LOAD BUTTON

RD CMD FOR IFT REQ

WRT CMD TO WRITE DATA

WRT CMD FOR LAST BLOCK

WRT IPL CMD SENDING LOADER

WRT CMD SENDING CONTROL WORD

Explanation: If the DCM has already been loaded, the program indicates that you can make a request at the 3705. If the DCM has not been loaded, the program starts over by requesting you to press the LOAD pushbutton on the 3705.

Response: If DCM has been loaded, enter a request; otherwise press LOAD.

PRESS LOAD ON 3705

Explanation: This message occurs when the type 1 CA loader is initially started or if loss of control occurs. It constitutes the beginning of the type 1 CA loader and provides the synchronization between the 3705 and the host processor.

Response: Press the LOAD pushbutton on the 3705. This message repeats every 30 seconds until the LOAD pushbutton is pressed.

AWAITING 3705 INTERFACE DISABLE

Explanation: The type 1 CA loader has loaded INIT in the 3705 and is waiting for the 3705 to go offline. This message is repeated every 20 seconds until the 3705 channel interface is disabled and the 3705 begins executing the IFT.

If this message occurs continuously, the 3705 is either unable to go offline after the INIT has been loaded, or unable to get back online after the INIT has completed execution. A processor-bound system can cause this problem.

Response: Pressing the STOP and then the START pushbuttons on the processor console drops the 'clock out' line long enough for the 3705 to go offline. Entering the wait state accomplishes this also.

ENTER IFT REQUEST AT 3705

Explanation: This message indicates that a request to load an IFT module can be entered.

Response: Enter an IFT request. See "How to Request an IFT" in this section.

3705 LOADED WITH IFT Z3705AAA

3705 LOADED WITH IFT Z3705ADA

3705 LOADED WITH IFT Z3705AEA

Explanation: These messages indicate that INIT or IFT modules have been successfully loaded in the 3705 without any errors being detected. Z3705AAA is the type 1 CA loader, Z3705ADA is the INIT section 1, and Z3705AEA is the INIT section 2.

Response: None.

ERP USED ON MOD Z3705XXX

Explanation: This message warns you that errors occurred while loading the INIT or IFT modules. Each output operation to the 3705 is attempted up to ten times if an error occurs (unless the OLT option EL (N) has been modified). If the operation being attempted is performed before the error count is exhausted, the OLT considers the data transfer successful and continues loading the INIT or IFT modules.

Response: Verify that the INIT or IFT modules are at the proper level.

Z3705XXX IN ERROR, ABORT LOAD

Explanation: The retry count (normally 10) is exhausted and the error is still occurring. The type 1 CA loader assumes that loss of control has occurred and restarts at the beginning.

Response: Refer to the message "ERP USED ON MOD Z3705XXX".

WAITING FOR IFT COMPLETION

Explanation: This message occurs every 20 seconds after an IFT has been loaded in the 3705. Most of the IFTs disable the 3705. The type 1 CA loader is in a loop issuing NOP

commands to the 3705. If it receives condition code 03, the 3705 interface is not enabled, it prints this message, and waits another 20 seconds. When the 3705 is enabled, the type 1 CA loader continues running.

Response: None.

INVALID PLINK MOD

Explanation: The type 1 CA loader has detected an error in the requested module (an address in the module was on an odd boundary). The type 1 CA loader returns to the Read command to allow you to enter another request at the 3705.

Response: Enter another request.

MOD Z3705XXX NOT IN OLTLIB

Explanation: The type 1 CA loader has received an IFT request (through a Read command), for a module that is not in OLTLIB. The type 1 CA loader returns to the Read command to allow you to enter another request at the 3705.

Response: Enter another request. However, if the request was valid, the IFT module name must be added to the OLTEP/OLTSEP library before the IFT can be loaded.

HOW TO USE THE DISPLAY/FUNCTION SELECT SWITCH (SEE FIGURE IFT-1)

With the DISPLAY/FUNCTION SELECT switch set to any position except TAR & OP REGISTER or STATUS, the following functions will be performed when: (1) the INTERRUPT pushbutton is pressed or (2) the START pushbutton is pressed after a stop code is displayed:

DISPLAY/FUNCTION SELECT Switch Position	STORAGE ADDRESS/ REGISTER DATA Switches A B C D E	FUNCTION
STORAGE ADDRESS	Y Y Y Y Y	Display location YYYYY.
REGISTER ADDRESS	- R - R -	Display register RR.
FUNCTION 1	- 0 - - -	Refresh the last DCM display.
	- 1 - - -	Stop the panel utilities.
	- 2 - - -	Set up continuous display without test.
	- 3 - - -	Set up continuous display with test.
	- 4 - - -	Set up address compare display without test.
	- 5 - - -	Set up address compare display with test.
	- 6 - H H	Set repeat count to HH.
	- 7 - - -	Display repeat count.
	- 9 S M M	Set CE sense switches (S=0 for byte 0 of switches, S=1 for byte 1 of switches, and MM= selected bits to be set or reset.
	- A S M M	Reset CE sense switches.
	- A S 0 0	Display CE sense switches.
	- D X X X	Dynamic communications to routines.
FUNCTION 2	X X X X X	Display storage contents at XXXXX.
FUNCTION 3	- R - R -	Display contents of register RR.
FUNCTION 4	- P I R R	Part 1 of IFT request (see "How to Request an IFT" later in this section).
	- M M M M	Part 2 of IFT request (see "How to Request an IFT" later in this section).
	- F 0 X X	Terminate OLTEP or OLTSEP at the host (see "How to Terminate an IFT" later in this section).
FUNCTION 5	V W X Y Z	Continue from the error stop or manual intervention stop. If it is an error stop, VWXYZ is not used. If it is a manual intervention stop, VWXYZ is used by the routine as specified in the IFT Symptom Index at the back of this section.
FUNCTION 6	- F F F F	Terminate the total request.
	- - - - -	Terminate the current routine.
FUNCTION 1,2, or 3	- - - - -	Panel utility display positions
FUNCTION 4,5, or 6		DCM displays of routine codes. Stop codes are displayed when the switch is set to any of the FUNCTION positions.

Note: - means that the switch is not used.

Figure IFT-1. How to Use the DISPLAY/FUNCTION SELECT Switch

HOW TO REQUEST AN IFT

An IFT request is divided into two parts: part 1 selects an adapter, IFT, and specific routines and part 2 selects the CE sense switch options desired. See the DCM section for the DCM stop codes, description, and required intervention.

Before an IFT request can be made:

1. OLTEP or OLTSEP must be running in the host CPU.
2. The DCM must be loaded and ready for an IFT request. Prior to the *initial request,* DISPLAY A and DISPLAY B will each contain X'FFFF'.

To perform part 1 of an IFT request:

1. Terminate active IFT request before entering a new request. See "How to Terminate an IFT or OLTEP/OLTSEP" later in this section.
2. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 4.
3. Set the STORAGE ADDRESS/REGISTER DATA switches to select the desired adapter, IFT, and routine (see Figure IFT-2). The IFT number is set in switch C, and the routine number is set in switches D and E. If the appropriate switch is set to 0, then all adapters, IFTs, or routines will be run.

   To run the CCU IFTs, set switches B and C to 11. To run the storage IFTs, set switch C to 2. To run the type 1 CA IFTs, set switch C to 3. To run the communication scanner IFTs, set switch C to 6. To run the type 4 CA IFTs, set switch C to 9. (See CE Request in "What IFT Does" earlier in this section.)

Adapter, IFT, and routine to be selected	STORAGE ADDRESS/ REGISTER DATA Switches B C D E
Run all routines of all IFTs on all all adapters.	0 0 0 0
Run all routines of one IFT on all adapters tested by this IFT (I is the IFT number).	0 I 0 0
Run all routines of one IFT on one adapter (I is the IFT number and P is the adapter ID)	P I 0 0
Run one routine of one IFT on all adapters tested by the IFT (I is IFT number and RR is the routine number).	0 I R R
Run one routine of one IFT on one adapter (P is the adapter ID, I is IFT number, and RR is the routine number).	P I R R

Figure IFT-2. How to Select an Adapter, IFT, and Routine

4. Press the START pushbutton. If the PROGRAM STOP and HARD STOP lights come on, DISPLAY A contains X'FFFF' and DISPLAY B contains X'8002' the DCM is ready for part 2 of the IFT request.

   If the PROGRAM STOP and HARD STOP lights do not come on, see "Why the PROGRAM DISPLAY Light Is Not On" in the DCM Section. See the IFT Symptom Index at the back of this section and perform the corrective action that is indicated.

To perform part 2 of an IFT request:

1. Set the STORAGE ADDRESS/REGISTER DATA switches to select the desired CE option as shown Figure IFT-3. (CE test options can be combined). For example, to loop on the first error (switch E = X'4'), you must also bypass error stop (switch E = X'8'). To combine both options, you would set switch E to X'C'.

   If no options for a particular switch are desired, set that switch to zero.

   See the DCM section for a detailed description of the CE sense switch settings.

CE Test Options	STORAGE ADDRESS/ REGISTER DATA Switch B	C	D	E
Problem definition mode				1
Restart routine on first error				2
Loop on first error				4
Bypass error stop				8
Cycle on request			1	
Include manual intervention routines (see the manual routines that follow)			2	
Repeat each routine X times			4	
Halt before execution			8	
Bypass new error stops		1		
Wait before continuing	8			

Figure IFT-3. CE Sense Switch Settings

2. Press the START pushbutton. The PROGRAM DISPLAY light should come on. If it does not, see "Determining Why the PROGRAM DISPLAY Light Is Not On" in the DCM section.
3. See the IFT Symptom Index at the back of this section for a description of the code in DISPLAY B.

HOW TO TERMINATE AN IFT OR OLTEP/OLTSEP

To terminate an entire IFT request, perform the following steps:

1. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 6.
2. Set STORAGE ADDRESS/REGISTER DATA switches BCDE to X'FFFF'.
3. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.

To terminate an IFT routine, perform the following steps:

1. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 6.
2. Set at least one of the STORAGE ADDRESS/REGISTER DATA switches BCDE to a value other than X'F'
3. If the program is running, press the INTERRUPT pushbutton. If the HARD STOP light is on, press the START pushbutton.
4. Press INTERRUPT.

To terminate an IFT request and also OLTEP or OLTSEP, perform the following steps:

1. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 4.
2. Set STORAGE ADDRESS/REGISTER DATA switches B and C to X'F0'. OLTEP or OLTSEP at the host and the IFT request will be terminated.

IFT Manual Intervention Routines

CCU Manual Intervention IFT

1156 Storage protect keys.
1190 Customer usage meter.

Storage Manual Intervention IFTs

1215 Storage worst card analysis routine. This routine requires approximately 12 minutes to run.

Type 2 CSB Manual Intervention IFTs

1694	PCF state X'F' disable
1698	Transmit test for PCF state X'B'
1699	Transmit test for PCF state X'C'
169C	Modem interface
16F0	SDLC link test
16F2	Wrap data test (BSC and SDLC)
16F4	X.21 line set test (world trade only)
16F5	High speed local attachment oscillator speed test

IFT SYMPTOM INDEX MASK FIELD AND REGISTER USAGE

The "mask" field specifies the bits being tested. A "0" in the mask field indicates that a bit position is not tested. If the IFT symptom index lists a "mask" field for registers 4, 5, and 6 (program level 4, hexadecimal X'14', X'15', and X'16'), the following contents are standard for the registers:

Register 4 (X'14') contains the "mask" bits being tested.
Register 5 (X'15') contains the bits in register X'14' that are in error.
Register 6 (X'16') contains the bit pattern expected in register X'14'.

EXAMPLE OF AN IFT RUN

Following is an example of running an IBM 3705-80 INIT and IFT. This example assumes that the channel adapter OLTs have previously been run successfully (see the CAOLT section).

In this example, all routines (except manual intervention and external wrap) of all IFTs are run for all adapters. Information is provided on how to run individual tests using different parameters such as error loops and test loops. The example also shows a starting point if an unexpected error stop occur.

It is assumed that OLTEP or OLTSEP is running in the host CPU and the CDS is correct for all adapters. It is also assumed that the MODE SELECT and DIAGNOSTIC CONTROL switches are set to PROCESS, and the DISPLAY/FUNCTION SELECT switch is set to STATUS.

This example does not completely test the LIBs and Line Sets. More in-depth testing can be done using the manual intervention routines (see "Manual Intervention Routines" earlier in this section). Manual intervention routines can be used to further test storage and the customer usage meter.

To specifically check line sets, the external wrap manual intervention routines can be used. Interaction between the communication scanner, LIBs, and/or line sets can cause scanner error stops that are caused by the line sets.

In this example, messages from the system are shown in upper case and information that you must enter is shown in lower case.

ENTER DEV/TEST/OPT	
xxx/3705A/nfe,ext=nyyy/'	This response requests that IFTs be loaded across the channel to the 3705. The ext parameter shown requests (1) print channel errors, (2) run INIT, (3) run type 1 CA loader with error checking, and (4) bypass hard stop on a type 1 CA loader error.
S T3705A	
THE STATUS OF THE 3705 CANNOT BE DETERMINED.** WARNING ** CONTINUATION WILL CAUSE THE ENTIRE 3705 TO BECOME UNAVAILABLE. ENTER 'C' TO CANCEL OR 'P' TO PROCEED.	This message may or may not be printed depending on the operating system.
'p'	
PRESS LOAD ON 3705	Press LOAD on the 3705. The IFTs will load across the channel after INIT runs.
3705 LOADED WITH IFT Z3705AAA	Z3705AAA is the type 1 CA loader.
3705 LOADED WITH IFT Z3705ADA	INIT section 1 is now running. See the INIT section of this manual if an error occurs.
WAITING FOR IFT COMPLETION	This message occurs every 20 seconds while the tests are running in the 3705. No action is required.
3705 LOADED WITH IFT Z3705AEA	INIT section 2 is now running. See the INIT section of this manual if an error occurs.
3705 LOADED WITH IFT Z3705ACA	The DCM is now in control of the 3705.
ENTER IFT REQUEST AT 3705	See "How to Request an IFT" in this section. Set the FUNCTION/DISPLAY SELECT switch to FUNCTION 4. DISPLAY A and DISPLAY B should both be X'FFFF'. The HARD-STOP and PROGRAM DISPLAY lamps should be on. Set the STORAGE ADDRESS/REGISTER DATA switches to X'0000' and press START. DISPLAY B should be X'8002'. The HARD-STOP and PROGRAM DISPLAY lamps should be on. Press START. All tests will run on all adapters.
3705 LOADED WITH IFT Z3705BAA	For a list of the IFT sections, see "What IFT Does" earlier in this section.
3705 LOADED WITH IFT Z3705BBA	
3705 LOADED WITH IFT Z3705BCA	
3705 LOADED WITH IFT Z3705CAA	After this point, the actual modules that are run depend on the hardware CDS. The list in this example only shows the CCU and storage IFT sections. If an unexpected error stop occurs, see the IFT Symptom Index at the back of this section.
WAITING FOR IFT COMPLETION	DISPLAY A = X'FFFF' and DISPLAY B = X'80F0' indicates that the IFTs have completed and no errors were detected. Terminate testing by setting X'F0XX' in STORAGE ADDRESS/ REGISTER DATA switches BCDE respectively. Then press START.
T T3705A	

Figure IFT-4. Example of an IFT Run

FAILURE INDICATIONS

If an error is detected during execution of IFT and the following conditions are met, use the information displayed in DISPLAY A and DISPLAY B to find a code in the IFT Symptom Index.

1. The LOAD light is off. If the LOAD light is on, see the error displays for the ROS, INIT, or IFT loader.
2. The TEST light must be on. If the TEST light is off and the LOAD light is on, see the error displays for the ROS, INIT, or IFT loader. If both the TEST light and the LOAD light are off, see the error displays for the IFT loader.
3. The DISPLAY/FUNCTION SELECT switch is set to FUNCTION 4, 5, or 6. If it is not, see "Refresh Last DCM Display Code" in the DCM section.
4. The PROGRAM DISPLAY light is on. If the PROGRAM DISPLAY light is off, see "Determining Why PROGRAM DISPLAY Light Is Not On" in the DCM section.

How to Use the IFT Symptom Index

If an IFT error occurs, use the data displayed in DISPLAY A and DISPLAY B to find a code in the IFT Symptom Index which will show one or more cards suspected of causing the failure.

A troubleshooting technique to use is:

1. When an error occurs, record the suspected failing card location (or locations).
2. Continue the IFT with the next routine (using FUNCTION 6).
3. If another error occurs, again record the suspected failing card location (or locations).
4. Repeat the previous step several more times.
5. After several IFT routines have been run that caused errors, the probable cause of the error is the card in the location with highest number of error indications.

   The list of suspected cards is not exhaustive and it may not indicate the exact failing card. If after replacing a suspected card, the failure persists, scoping the signals into and out of the card may help you determine the cause of the failure.

How to Find an IFT Symptom Index Error Code

If an IFT error occurs, the data displayed in DISPLAY A and DISPLAY B is in the following format:

```
DISPLAY A   =   P I R R
DISPLAY B   =   T S K K
```

Where:

P = The ID of the adapter being tested when the failure occurred
I = The IFT number being run when the failure occurred
RR = The routine number being run when failure occurred
T = The type of display code
S = Scoping indicator and error counter
KK = Code reference in symptom index

Each of the above characters represents a 4-bit hexadecimal digit. Note also that byte X is not used.

Use the following procedure to find a code in the IFT symptom index:

001
Is T equal to 8 (DISPLAY B first hex digit)?
Y N

002
Is T equal to 0 (DISPLAY B first hex digit)?
Y N

003
Is T equal to 1 or 2 (DISPLAY B first hex digit)?
Y N

004
Is T equal to E (DISPLAY B first hex digit)?
Y N

005
Is T equal to F (DISPLAY B first hex digit)?
Y N

006
Is T equal to 6 or 7 (DISPLAY B first hex digit)?
Y N

007
Is T equal to 9 or A (DISPLAY B first hex digit)?
Y N

008
Is T equal to B or D (DISPLAY B first hex digit)?
Y N

009
Ensure that the DCM and IFT loaded properly and that the required conditions described prior to this procedure were met.

010
See the section 'Dynamic Communication To Routines' (DCM section). This display is from that DCM panel utility.

011
See 'Set, Reset, Display CE Sense Switches' (DCM section). This display is from that DCM panel utility.

012
See 'Set or Display Repeat Count' (DCM section). This display is from that DCM panel utility.

013
A manual intervention stop code is being displayed.

T	I	
F	1	CCU
F	6	CSB type 2

014
Information is being displayed. The display indicates either errors or correct operation.

T	I	
E	1	CCU
E	6	CSB type 2

015
A pretest error or an error common to the IFT routines has been detected: 1 indicates pretest, 2 indicates common error.
The I field (DISPLAY A second hex digit) indicates the IFT Symptom Index to use.

T	I	
1/2	1	CCU
1/2	2	Storage
1/2	3	CA type 1
1/2	6	CSB type 2
1/2	9	CA type 4

016
The IFT has detected an error and an error code is displayed.
The I field (DISPLAY A second hex digit) indicates the IFT Symptom Index to use.

T	I	
0	1	CCU
0	2	Storage
0	3	CA type 1
0	6	CSB type 2
0	9	CA type 4

017
See the DCM symptom index (DCM Section) for a description of the display. DISPLAY A indicates which adapter, which IFT, and which routine is active. DISPLAY A equal to X'FFFF' indicates the DCM is ready to accept a new request.

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3705-80 CCU IFT SYMPTOM INDEX

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1102	0X01	The interval timer L3 irpt should occur every 100 milliseconds. This routine tests for an accuracy of ± 3 percent. Did L3 timer irpt occur prior to 97 ms?	The timer L3 irpt occurred in less than 97 ms.	A-B3L2 A-B3U5	00FF	CP007 CC007	6-090	Reg X'15' indicates percent of error. If reg X'15' equals X'0004', the error is 4 percent which means the timer irpt occurred at 96 ms.
	0X02	Did L3 timer irpt occur after 103 ms?	The timer L3 irpt occurred later than 103 ms.	A-B3L2 A-B3U5	00FF	CP007 CC007	6-090	Reg X'15' indicates percent of error. X'0004' indicates 4 percent error. The irpt occurred at 104 ms.
	0X03	Default test. If an irpt does not occur within 110 ms, this routine will halt.	A timer L3 irpt did not occur within 110 ms.	A-B3L2 A-B3U5	N/A	CP007 CC007	6-090	Standard DCM display does not apply.
1103	0X01	Memory size test. Input X'70' is compared with the BSM count (contained in the Configuration Data Set (CDS) to verify that the two agree.	Input X'70' and CDS BSM count did not compare.	A-B4E2 (If CDS count is correct.)	N/A	CM002	4-070 6-770	Reg X'14' = CDS BSM count. Reg X'15' = Input X'70' converted to BSM count. Reg X'16' = Input X'70'.
1104	0X01	Z bus parity checker. Bit 7 of bytes X, 0, and 1 is complemented to forced bad parity. The CCU ck reg is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.	The actual CCU ck reg data is in error. The Z parity checker failed to detect bad parity. CCU ck reg is input X'7D'.	See Note 5. A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-050	See Note 1.
	0X02	Did the force error function produce the correct data?	The actual data produced by the force error function did not compare with the expected data.	A-B3S2 A-B3G2	3FFFF	CK001 CQ005	6-050	
1105	0X01	Z bus parity checker. Bit 6 of bytes X, 0, and 1 is complemented to force bad parity. The CCU ck reg is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.	The actual CCU ck reg data is in error.	See Note 5. A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-050	See Note 1.
	0X02	Did the force error function produce the correct data?	The actual data produced by the force error function did not compare with the expected data.	A-B3S2 A-B3G2	3FFFF	CK001 CQ005	6-050	
1106	0X01	Z bus parity checker. Bit 5 of bytes 0 and 1 is complemented to force bad parity. The CCU ck reg is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.	The actual CCU ck reg data is in error.	See Note 5 A-B3N2 A-B3G2	3FFFF	CK003 CQ005	6-050	See Note 1.
	0X02	Did the force error function produce the correct data?	The actual data produced by the force error function did not compare with the expected data	A-B3S2 A-B3G2	3FFFF	CK001-2 CQ005		
1107	0X01	Z bus parity checker. Bit 4 of bytes 0 and 1 is complemented to force bad parity. The CCU ck reg is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.	The actual CCU ck reg data is in error.	See Note 5. A-B3N2 A-B3G2	FFFF	CK003-7 CQ005		See Note 1.
	0X02	Did the force error function produce the correct data?	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2	3FFFF	CK001 CQ005	6-050	
1108	0X01	Z bus parity checker. Bit 3 of bytes 0 and 1 is complemented to force bad parity. The CCU ck reg is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.	The actual CCU ck reg data is in error	See Note 5. A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-050	See Note 1.
	0X02	Did the force error function produce the correct data?	The actual data produced by the force error function did not compare with the expected data.	A-B3S2 A-B3G2	3FFFF	CK001 CQ005		

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1109	0X01	Z bus parity checker. Bit 2 of bytes 0 an 1 is complemented to force bad parity. The CCU ck reg is tested for expected data. Routine makes 256 passes starting with data 0000 using an update value of X'10101'.	The actual CCU ck reg data is in error.	See note 5. A-B3N2 A-B3G2	FFFF	GK003 CQ005	6-050	See Note 1.
	0X02	Did the force error function produce the correct data?	The actual data produced by the force error function did not compare with the expected data.	A-B3S2 A-B3G2	3FFFF	CK001 CQ005		
110A		Z bus parity checker. Bit 1 of bytes 0 and 1 is complemented to force bad parity.						
	0X01	The CCU ck reg is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.	The actual CCU ck reg data is in error.	See Note 5. A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-050	See Note 1.
	0X02	Did the force error function produce the correct data?	The actual data produced by the force error function did not compare with the expected data.	A-B3S2 A-B3G2	3FFFF	CK001 CQ005	6-050	
110B		Z bus parity checker. Bit 0 of bytes 0 and 1 is complemented to force bad parity.						
	0X01	The CCU ck reg is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.	The actual CCU ck reg data is in error.	See Note 5. A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-050	See Note 1.
	0X02	Did the force error function produce the correct data?	The actual data produced by the force error function did not compare with the expected data.	A-B352 A-B3G2	3FFFF	CK001 CQ005	6-050	
110C		A reg parity checker. Output X'78' (force CCU checks) with mask X'0020' is used to force bad parity.						
	0X01	The CCU reg is tested for the expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.	The A reg parity checker failed to detect bad parity	See Note 5. A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-920	See Note 1.
	0X02	Did the force error function produce the correct data?	The actual data produced by the force error function did not compare with the expected data.	A-B3S2 A-B3G2	3FFFF	CK001 CQ005	6-920	
110D	0X01	B reg parity checker. Output X'78' with mask X'0040' is used to force bad parity. The CCU ck reg is tested for the expected data.	The B reg parity checker failed to detect bad parity.	See Note 5. A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-920	See Note 1.
	0X02	Did the force error function produce the correct data?	The actual data produced by the force error function did not compare with the expected data.	A-B3S2 A-B3G2	3FFFF	CK001 CQ005	6-920	
110E		SDR reg parity checker test. Output 'X78', (force CCU checks) with mask X'0040' is used in conjunction with an output instruction to force SDR errors. The output instruction that forces the error is reg X'15' output to reg X'1A'. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.						
	0X01	The CCU ck reg is tested for the expected error bits.	The actual CCU ck reg data is in error.	See Note 6. A-B3N2 A-B3S2	FFFF	CK001 CU013 CU013	6-920	Reg X'16' will contain the test data that was used to output to reg X'1A'.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
110F		Indata parity checker test. Output X'78' (Force CCU checks) with mask X'0010' is used in conjunction with an input instruction to force indata parity errors. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.						
	0X01	The CCU ck reg is tested for the expected error bits.	The actual CCU check reg data is in error.	A-B3S2 A-B3N2	FFFF	CK001 CU013	6-920	Reg X'16' will contain the test data that was in reg X'1A' when the input from reg X'1A' was executed.
1110	0X01	SAR parity checker test. Output X'78' (force CCU checks) with mask X'0040' is used to force bad parity. The CCU ck reg is tested for the expected error bits.	The SAR parity checker failed to detect bad parity.	See Note 7. A-B3N2 A-B4G2 A-B4H2	FFFF	CK003 DP993 DR993	6-920	See Note 1.
	0X02	Did the force error function produce the correct data?	The actual data produced by the force error function did not compare with the expected data.	A-B3S2 A-B3G2 A-B3H2	FFFF	CK001 DP993 DR993	6-920	
1113	0X01	L4 is interrupted by L3 via a PCI L3 irpt. Irpt req grp 2 (X'7F') is tested for a PCI L3 bit.	The PCI L3 irpt failed to occur.	A-B3G2 A-B3M2 A-B3J2	FDFB	CQ005 CD001 CU015 CP002 CA003	6-920 6-860	
	0X02	Before forcing the L3 irpt, the L4 CZ latches are set to CZ = 10. On return to L4 the CZ latches are tested to ensure that L3 did not alter the preset L4 CZ latches.	The L4 CZ latches were altered by the PCI L3 irpt.	A-B3G2	0003	CZXXX	6-090	
1114	0X01	L4 is interrupted by L3 via a PCI L3 irpt. Irpt req grp 2 (X'7F') is tested for a PCI L4 bit.	The PCI L3 irpt failed to occur.	A-B3G2 A-B3M2 A-B3J2	FDFB	CQ005 CD001 CU015 CP002 CA003	6-090 6-860	See routine 1113.
	0X02	Before forcing the L3 irpt, the L4 CZ latches are set to CZ = 01. On return to L4 the CZ latches are tested to ensure that L3 did not alter the preset L4 XZ latches.	The L4 CZ latches were altered by the PCI L3 irpt.	A-B3G2	0003	CZXXX	6-090	
1115	0X01	L2 masking and unmasking functions are tested. L2 is masked and then an attempt to force an L2 irpt, via diag L2 function, is performed.	The L2 mask function failed to prevent an L2 irpt.	A-B3M2	FDFB	CP002 CD001 CQ001	6-090 6-940	
	0X02	L2 is unmasked and an L2 irpt is forced via diag L2 function.	The L2 unmask function failed.	A-B3M2	FDFB	CP002 CD001 CQ001	6-090 6-950	
1116		L4 is interrupted by L2 via the diag L2 function.						
	0X01	Irpt req grp 2 (X'7F') is tested for a diag L2 bit.	The diag L2 irpt failed to occur.	A-B3M2	FDFB	CP002	6-860	
	0X02	Before forcing the L2 irpt, the L4 CZ latches are set to CZ = 01. On return to L4 the CZ latches are tested to ensure that the L2 irpt did not alter the preset L4 CZ latches.	The L4 CZ = 10 latches were altered by the diag L2 irpt.	A-B3G2	0003	CZXXX	6-090	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1117	0X01	L4 is interrupted by L2 via the diag L2 function.	The diag L2 irpt failed to occur.	A-B3G2	FDFB	CP002	6-090	See routine 1116.
	0X02	Before forcing the L2 irpt, the L4 CZ latches are set to CZ = 01. On return to L4 the CZ latches are tested to ensure that the L2 irpt did not alter the preset L4 CZ latches.	The L4 CZ = 10 latches were altered by the diag L2 irpt.	A-B3G2	0003	CZXXX	6-090	
1118	0X01	L4 is interrupted by a L1 irpt via a I/O check. The utility reg X'79' is tested to verify that L4 was interrupted.	The utility reg did not contain the prog L4 interrupted bit. (L1 failed to irpt.)	A-B3M2	00F0	CP004	6-830	Bypass troubleshooting this error until error code 0X02 of this routine has run without an error.
	0X02	Irpt req grp 1 X'7E' is tested for the I/O check L1 bit.	The I/O check L1 bit did not set. An L1 irpt did not occur.	N/A	FFFF	CU014	6-850	
	0X03	Before forcing the L1 irpt, the L4 CZ latches are set to CZ = 10. On return to L4 the CZ latches are tested to ensure that the L1 did not alter the preset L4 CZ latches.	The L4 CZ = 10 latches were altered by the L1 irpt.	A-B3G2	0003	CZXXX	6-090	
1119		L4 is interrupted by an L1 irpt via an I/O check.						
	0X01	The utility reg X'79' is tested to verify if L4 was interrupted.	L1 failed to irpt.	A-B3L2 A-B3G2	00F0	CU014 CP002	6-803	See routine 1118.
	0X02	Irpt req grp 1 X'7E' is tested for the I/O check L1 bit.	The I/O check L1 bit did not set.		FFFF		6-050	
	0X03	Before forcing the L1 irpt, the L4 CZ latches are set to CZ = 01.	The L4 CZ = 01 latches were altered by the L1 irpt.	A-B3G2	0003	CZXXX	6-090	
111A		L3 is interrupted by a diag L2 function.						See routine 1113.
	1X01	Since the DCM runs under L4, an L3 irpt is forced via PCI L3 to allow this routine to test while in L3.	Pretest error.				6-940	
	0X01	An L2 irpt is forced via diag L2. The irpt req grp 2 X'7E' is tested to verify that diag L2 bit was set.	The diag L2 irpt failed to occur when running under L3.		FDFB		6-830	See routine 1116.
	0X02	Before forcing the L2 irpt, the L3 CZ latches are set to CZ = 10.	The L3 CZ = 10 latches were altered by the L2 irpt.		0003		6-090	
111B	1X01	Since the DCM runs under L4, an L3 irpt is forced via PCI L3 to allow this routine to test while in L3.	Pretest error.				6-940	
	0X02	Before forcing the L2 irpt, the L3 CZ latches are set to CZ = 01.	The L3 CZ = 01 latches were altered by the L2 irpt.		0003		6-830	
111C		L3 is interrupted by L1 via an I/O check L1.						See routine 1113.
	1X01	Since the DCM runs under L4, and L3 irpt is forced via PCI L3 to allow this routine to test while in L3.	Pretest error.				6-940	
	0X01	The utility reg X'79' is tested to verify that L3 was interrupted.	The utility reg did not contain the prog L3 interrupted bit.	A-B3M2	00F0	CP004	6-830	Bypass troubleshooting this error until error code 0X02 of this routine has run without failure.
	0X02	The L1 irpt is forced via I/O check L1.	The I/O check bit did not set. An L1 irpt did not occur when running under L3.		FFFF		6-050	See routine 1118.
	0X03	Before forcing the L1 irpt, the L3 CZ latches are set to CZ = 10. On return to L3 the CZ latches are tested to ensure that the L1 irpt did not alter the preset L3 CZ latches.	The L3 CZ = 10 latches were altered by the L1 irpt.		0003		6-090	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
111D	1X01	Since the DCM runs under L4, an L3 irpt is forced via PCI L3 to allow this routine to test while in L3.	Pretest error.				6-940	
	0X01	The utility reg X'79' is tested to verify that L3 was interrupted.	The utility reg did not contain the prog L3 interrupted bit.	A-B3M2	00F0	CP004	6-830	Bypass troubleshooting this error until error code 0X02 of this routine has run without failure.
	0X02	The L1 irpt is forced via I/O check L1.	The I/O check bit did not set. An L1 irpt did not occur when running under L3.		FFFF		6-050	See routine 1118.
	0X03	Before forcing the L1 irpt, the L3 CZ latches are set to CZ = 01.	The L3 CZ = 01 latches were altered by the L1 irpt.		0003		6-090	
111E		L2 is interrupted by L1 via an I/O check L1.					6-050	See routine 1116.
	1X02	Since the DCM runs under L4, an L2 irpt is forced via diag L2 irpt. This will allow the routine to test while in L2.	Pretest error.				6-090	
	0X01	The utility reg X'79' is tested to verify that L2 was interrupted.	The utility reg did not contain the prog L2 interrupted bit.	A-B3M2	00F0	CP004	6-830	Bypass troubleshooting this error until error code 0X02 of this routine has run without failure.
	0X02	The L1 irpt is forced via an I/O check L1. Irpt req grp 1 X'7E' is tested to verify.	The I/O check L1 bit did not set. An L1 irpt did not occur when running under L2.		FFFF		6-850	See routine 1118.
	0X03	Before forcing the L1 irpt, the L2 CZ latches are set to CZ = 10. On return to L2, the CZ latches are tested to ensure that the L1 irpt did not alter the preset L2 CZ latches.	The L2 CZ = 10 latches were altered by the L1 irpt.		0002		6-090	
111F	1X02	Since the DCM runs under L4, an L2 irpt is forced via diag L2 irpt. This will allow the routine to test while in L2.	Pretest error.				6-090	See routine 1117.
	0X01	The utility reg X'79' is tested to verify that L2 was interrupted.	The utility reg did not contain the prog L2 interrupted bit.	A-B3M2	00F0	CP004	6-830	See routine 1119.
	0X02	The L1 irpt is forced via an I/O check L1. Irpt req grp 1 X'7E' is tested to verify.	The I/O check L1 bit did not set. An L1 irpt did not occur when running under L2.		FFFF		6-850	See routine 1118.
	0X03	Before forcing the L1 irpt, the L2 CZ latches are set to CZ = 01. On return to L2, the CZ latches are tested.	The L3 CZ = 01 latches were altered by the L1 irpt.		0003		6-090	
1120		This routine does an irpt display-chain from L4 to L3 to L2 to L1 to L3 to L4. The CZ latches for L4, L3, and L2 are preset to a known state before forcing the next irpt. Each is checked on return to its level.					6-080	See routines 1113-111F.
	1X01	L4 is interrupted by L3 via PCI L3.	Pretest error.				6-090	
	1X02	L3 is interrupted by L2 via diag L2.	Diag L2 irpt failed to occur.		N/A		6-090	
	0X01	Before forcing the L3 irpt, the L4 CZ latches are set to CZ = 10. On return to L4, the CZ latches are tested to ensure that the L3, L2, and L1 irpt did not alter the preset L4 CZ latches.	The L4 CZ = 10 latches were altered by the L3, L2, and L1 irpt daisy-chain.		0003		6-090	
	0X02	Before forcing the L2 irpt, the L3 CZ latches are set to CZ = 01. On return to L3, the CZ latches are tested.	The L3 CZ = 10 latches were altered by the L2 and L1 irpt daisy chain.		0003		6-090	
	0X03	Before forcing the L1 irpt, the L2 CZ latches are set to CZ = 10. On return to L2, the CZ latches are tested.	The L2 CZ = 10 latches were altered by the L1 irpt.		0003		6-090	
1121	0X01	L4 masking and unmasking functions are tested. Since the DCM runs under PCI L4, this routine resets PCI L4 and waits for an L3 interval timer L3 irpt. L4 is then masked and tested. On the next timer L3 irpt, L4 is unmasked and tested.	The L4 mask function failed to prevent a PCI L4 irpt from occurring.	A-B3M2 A-B3L2	N/A	CP002 CP006	6-090 6-940	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1121	0X02	L4 is unmasked and a PCI L4 irpt is set while in L5. An exit from L3 is performed and L4 should irpt via PCI L4.	The L4 unmask function failed. A PCI L4 irpt did not occur.	A-B3M2	N/A	CP002	6-090 6-950	
1122	0X01	L3 masking and unmasking functions are tested. L3 is masked; an attempt is made to force an L3 irpt via a set PCI L3 irpt.	The L3 mask function failed to prevent a PCI L3 irpt from occurring. If the L5 mask function is not active, false errors may occur. If so, run routine 1124 to test the L5 mask function.	A-B3M2	N/A	CP002	6-940 6-950 6-940	
	0X02	L3 is unmasked, an attempt is made to force a L3 irpt via a set PCI L3 irpt.	The L3 unmask function failed. A PCI L3 irpt did not occur.	A-B3M2	N/A	CP002	6-940	
1123		This routine tests for an L4 service irpt (svc L4) when an exit from L5 is performed.						
	0X01	In order to reach L5, the PCI L4 irpt must be reset and an exit from L4 is performed.	L5 failed to become active or L4 failed to exit (previously tested).	A-B3M2	N/A	CP003	6-090	
	0X02	The exit from L5 should set svc L4 irpt. The irpt reg grp 2 X'7F' will be tested to verify this.	The L5 exit failed to set svc L4 irpt bit.	A-B3M2	0001	CU015	6-860	
	0X03	The L4 svc L4 irpt will be reset to verify that it can be reset.	Svc L4 irpt failed to reset.	A-B3M2	0001	CU015	6-090	
	0X05	An L5 exit is performed.	L5 failed to exit.		N/A		6-750	
1124		This routine tests that L5 can be interrupted by L1.						
	0X01	L5 is interrupted by L1 via an I/O check. Irpt reg grp 1 X'7E' is tested to verify that a L1 irpt did occur.	The I/O check L1 bit did not set. L1 irpt failed to occur.		FFFF	CU014	6-850	
	0X02	The utility reg X'79' is tested for a prog L5 interrupted bit. The L1 irpt should cause the utility reg to set the above bit.	The prog L5 interrupted bit failed to set.	A-B3M2	0010	CP004	6-830	
	0X03	Before forcing the L1 irpt, the L5 CZ latches are set to CZ = 01. On return to L5, the CZ latches are tested.	The L5 CZ = 01 latches were altered by the L1 irpt.		0003		6-090	
	0X04	On return to L4, the saved utility reg is tested to verify that the L5 CZ condition bits are correct.	The CZ = 01 bits in the utility reg are in error.	A-B3M2	0300	CP004	6-090	
	0X05	Upon return to L4 and after the above tests have been run, the utility reg is tested to verify that the exit from L2, L5, and the L4 irpt did not affect the L5 CZ = 01 latch.	The CZ = 01 bits of the utility reg are in error. The L5 exit or svc 14 irpt affected the L5 CZ latch.		0300	CP004	6-090	
1125	0X01	The masking and unmasking of L5 is tested. L5 is masked and instruction execution is halted on L4 and an exit from L4 is performed. This should allow L5 to become active if the masking function failed.	The L5 masking function failed.	A-B3M2	N/A	CP002	6-940 6-950	
	0X02	L5 is unmasked to allow L5 to become active.	The L5 unmask function failed.		N/A		6-950	
112A	0X01	Invalid input reg decode testing. An attempt is made to input to an invalid reg. An I/O check L1 irpt should result. Invalid reg values are in a table. Irpt req grp 1 X'7E' is tested for an I/O check L1 bit.	The invalid input reg failed to set I/O check.	A-B3L2 A-B3K2 A-B3H2	FFFF	CK007 CU014 CQ001 CD001	6-120 6-120 6-850	Reg X'16' will contain the value of the input reg that produced the error. Errors in this routine could be external to the CCU. (CSBs, CAs). Byte 0 bit 0-3 and byte 1 bits 0-3 are the two hex values that define the reg.
	0X02	The LAR reg is tested to verify that the L1 irpt occurred at the invalid test slot.	LAR reg failed to track or the L1 irpt occurred at the wrong adr.	A-B3M2	3FFFF	CS001	6-800	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
112B	0X01	Invalid output reg decode testing. An attempt is made to output an invalid reg. An I/O check L1 irpt should result. Invalid reg values are in a table. Irpt reg grp 1 X'7E' is tested for an I/O check.	The invalid output reg failed to set I/O check.	A-B3L2 A-B3K2 A-B3H2	FFFF	CK007 CU014 CQ007 CD001	6-120 6-850	Reg X'16' will contain the value of the output reg that produced the error. Byte 0 bits 0-3 and byte 1 bits 0-3 are the two hex values that define the reg.
	0X02	The LAR is tested to verify that the L1 irpt occurred at the invalid test slot.	LAR failed to track or the L1 irpt occurred at the wrong adr.	A-B3M2	3FFFF	CS001	6-800	
112C		Invalid op (instruction) testing.						
	0X01	An attempt is made to execute a half-word of code that is invalid. Invalid operations are in a table. Irpt req grp 1 X'7E' is tested for a op check L1 bit.	The invalid op failed to set op check L1.	A-B3L2	FFFF	CU014	6-050 6-850	Reg X'16' will contain the value of the op that caused the error.
	0X02	The LAR is tested to verify that the L1 irpt occurred at the invalid test slot.	LAR failed to track or the L1 irpt occurred at the wrong adr.	A-B3M2	3FFFF			
112D	0X01	Invalid op (instruction) testing. An attempt is made to execute a half-word of code that is invalid. The invalid ops are formed from table data ORed with a varying data field. This routine makes over 300 passes. Irpt reg grp 1 X'7E' is tested for a op check L1 bit.	The invalid op failed to set op check L1.	A-B3L2	FFFF	CU014	6-050 6-850	Reg X'16' will contain the value of the invalid op that caused the error.
	0X02	The LAR is tested.	LAR failed to track or the L1 irpt occurred at the wrong adr.	A-B3M2	FFFF	CS001	6-800	
112E	0X01	Invalid op (instruction) testing. An attempt is made to execute a halfword of code that is invalid. The invalid ops are formed from data table data ORed with a varying data field. This routine makes over 600 passes.	The invalid op failed to set up check L1.	A-B3L2	FFFF	CU014	6-050 6-850	Reg X'16' will contain the value of the invalid op that caused the error.
	0X02	The LAR is tested under routine 112D.						
112F	0X01	Invalid op (instruction) testing. An attempt is made to execute a half-word of code that is invalid. The invalid ops are formed from table data ORed with a varying data field. This routine makes over 180 passes.	The invalid op failed to set op check L1.	A-B3L2	FFFF	CU014	6-050 6-850	Reg X'16' will contain the value of the invalid op that caused the error.
	0X02	The LAR is tested under routine 112D.	LAR failed to track or the L1 irpt occurred at the wrong adr.	A-B3M2	FFFF	CS001	6-800	
1130	0X01	Invalid op (instruction) testing. An attempt is made to execute a half-word code that is invalid. The invalid ops are formed from table data ORed with a varying data field. This routine makes over 50 passes.	The invalid op failed to set op check L1.	A-B3L2	FFFF	CU014	6-050 6-850	Reg X'16' will contain the value of the invalid op that caused the error.
	0X02	The LAR is tested under routine 112D.	LAR failed to track or the L1 irpt occurred at the wrong adr.	A-B3M2	FFFF	CS001	6-800	
1131	1X03	Tests for an L1 program check when an invalid op is detected while in L1. Since the DCM runs in L4, an invalid I/O check will be used to force this routine to run in L1.	I/O check failed to force a L1 irpt (pretest error).		N/A		6-050	
	0X01	Once L1 is active, an invalid op check is forced. Irpt req grp 1 X'7E' is tested for an invalid op check.	The invalid op failed to force an error when operating under L1.	A-B3H2	FFFF	CD004	6-050 6-850	See routine 112C or 112D.
	0X02	The invalid op in L1 should set L1 prog check and CCU check. CCU check reg X'7D' is tested.	The L1 invalid op failed to set the expected check bits.	A-B3N2	FFFF	CK007		

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1132	1X03	Tests for an L1 program check when an invalid I/O check is detected while in L1. Since the DCM runs in L4, an invalid check will be used to force this routine to run in L1.	Initial I/O check failed to force and L1 irpt (pretest error).		N/A		6-050	
	0X01	Once L1 is active, an I/O check is forced. Irpt req grp 1 X'7E' is tested for an I/O check.	The I/O check failed to force an error when operating under L1.		FFFF	CU014		
	0X02	The I/O check in L1 should set L1 prog check and CCU check. CCU check reg X'7D' is tested.	The L1 I/O check failed to set the expected check bits.	A-B3N2	FFFF	CK007	6-050 6-840	
1133		Address exception test. This routine attempts to load data from the first invalid adr and expects an adr exception check to occur. The adr under test is then increased in increments of 4K until the maximum adr is reached.						
	0X01	Test for adr exception. Irpt req grp X'7E' is tested for adr exception check L1 bit.	Adr exception failed to occur.	A-B4E2 A-B3F2	0040	CS002 CM003	6-050 6-850	Register X'13' will contain the adr under test.
	0X02	LAR is tested to verify that it tracks and that the adr exception occurred at the expected instruction.	LAR failed to track or adr exception check above failed to occur.		FFFF		6-800	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1134	0X01	PCI L3 irpt reg unused bit testing. The data in reg X'11' is varied from 0000 to FFFF to verify that the value of the data does not matter. Instruction out reg X'11', PCI L3.	PCI L3 irpt failed to occur (don't care bits do care).		FDFB			Reg X'16' will contain the value of reg X'11' when the error occurred.
1135	0X01	L4 instruction interaction test. A given half-word instruction is inserted into an arithmetic sequence at three different points to test for any interaction. The test loop is repeated 48 times with different half-word instructions.	Data expected did not agree. Test instruction was between an LHR and an OHR.		FFFF		6-220	Reg X'16' contains the half-word instruction that caused the interaction.

Special Note: The purpose of this test is to produce a random sequence of instructions to verify any interaction that may exist. The following code is listed to illustrate the technique used to detect interaction.

```
     LA   R2,X'8421'          R2=  1000  0100  0010  0001
     LA   R4,X'1248'          R4=  0001  0010  0100  1000
     LHR  R4,R4               R4=  0001  0010  0100  1000
**---------- *
 *TEST SLOT*                  The Instruction Under Test Is Stored In This Slot
**---------- *
     OHR  R2,R4               R2=  1001  0110  0110  1001
     STH  R2,SAVE1            Save R2 For Error Code 0X01 Analysis
     LA   R6,X'FFFF'          R6=  1111  1111  1111  1111
**---------- *
 *TEST SLOT*                  The Instruction Under Test Is Stored In This Slot
     XHR  R2,R6               R2=  0110  1001  1001  0110
**---------- *
 *TEST SLOT*                  The Instruction Under Test Is Stored In This Slot
**---------- *
     LA   R5,X'9669'          R5=  1001  0110  0110  1001
     NHR  R2,R5               R2=  0000  0000  0000  0000
     STH  R2,SAVE2            Save R2 For Error Code 0X02 Analysis
```

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Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1135	0X02	The final sum of the arithmetic sequence is tested.	Data expected did not agree. The test instruction was between an LA and an XHR.		FFFF		6-220 6-600	Same as 0X01 above.
1136		L3 instruction interaction test. This routine is the same as 1135 above except the test is run under program L3.						
	1X01	A PCI L3 irpt is used to force an L3 irpt.	PCI L3 irpt failed (pretest error).		N/A		6-090	
	0X01	Same as 0X01 above under routine 1135.						
	0X02	Same as 0X02 above under routine 1135.						
1137		L2 instruction interaction test. This routine is the same as 1135 above except the test is run under program L2.						
	1X02	Diag L2 irpt is used to force an L2 irpt.	Diag L2 irpt failed (pretest error).		N/A		6-090	
	0X01	Same as 0X01 above under routine 1135.						
	0X02	Same as 0X02 above under routine 1135.						
1138		L1 instruction interaction test. This routine is the same as 1135 above except the test is run under program L1.						
	1X03	An invalid output reg is used to force an L1 irpt.	Invalid output reg failed to produce an L1 irpt (pretest error).		N/A		6-090	
	0X01	Same as 0X01 above under routine 1135.						
	0X02	Same as 0X02 above under routine 1135.						
1139	0X01	L5 instruction interaction test. This routine is the same as 1135 above except the test is run under program L5. Error is same as 0X01 above under routine 1135.					6-090	
	0X02	Same as 0X02 above under routine 1135.						
113C		Verify correct indication and operation of reg X'7A'.						
	0X01	Input X'7A' byte 0 bit 0 on (cycle utilization counter (CUC) instruction).	CDS definition indicates CUC installed, but hardware indicator bit is off.	A-B4T2				Verify that CDS definition in model/flag byte.
	0X02	Input X'7A' byte 0 bit 0 is on (no CUC instruction).	CDS indicates CUC not installed, but hardware bit is on.	A-B4T2				Verify model/flag byte of CDS.
	0X03	Cycle utilization counter value is not correct. Several passes are made using different values.		A-B4T2				Reg X'14' contains actual CUC value. Reg X'15' contains bits in error. Reg X'16' contains expected CUC value.
113F		BSC CRC polynomial test. This routine will test the hardware CRC circuitry to verify that the correct CRC character is developed.						
	0X01	Using input reg X'7B'.	The developed and expected CRC characters did not compare.	A-B3S2	FFFF	CR001-3		See comment below for Routine 1140.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1140	0X01	8-Bit CRC polynomial test.	The developed and expected CRC characters did not compare.	A-B3S2	FFFF	CR001-3		Register X'13' will contain an adr pointer to the data table. To determine the old CRC, data character, and expected new CRC display the following storage adrs: Reg X'13' adr = old CRC. Reg X'13' adr plus 2 = data. Reg X'13' adr plus 4 = new CRC. **Note:** Reg X'13' above implies the adr is contained in reg X'13'.
1142	0X01	CRC Polynomial Test for Airline Line Control (ALC) RPQ #858655 This routine should run only when RPQ 858655 is installed. If the failing 3705-80 does not have RPQ 858655 installed, check the CDS data.	The developed and expected CRC characters did not compare.	A-B3C2	FFFF			See comments for routine 1140.
1143	0X01	ALC CS3 reg test. This routine should run only when RPQ 858911 is installed. If RPQ 858911 is not installed, check the CDS data. Test bits for rcv/xmt direction and all CCC bits in input and output X'75'.	I/O regs X'75' do not compare.					R14 = data read from input reg X'75'. R15 = bits in error. R16 = data stored in output reg X'75'.
1144		ALC xmt test. This routine should run only when RPQ 858911 is installed. If RPQ 858911 is not installed, check the CDS data.						
	0X01	Tests ALC L1 hardware by altering one instruction in the data processing sequence.	Altered instruction failed to produce an L1 irpt.					Input reg X'7E' byte 1, bit 7 should be on to indicate ALC support L1 err.
	0X02	Tests EOM remember part 1. Test if expected.	EOM remember was expected but was not detected. Bit tested is byte 0, bit 1.					R14 = actual data. R16 = expected data.
	0X03	Tests EOM remember part 2. Test if detected.	EOM remember was detected but was not expected. Bit tested is byte 0, bit 1.					R14 = actual data. R16 = expected data.
	0X04	Tests EOM expected.	EOM was expected but was not detected. Bit tested is byte 0, bit 2.					R14 = actual data. R16 = expected data.
	0X05	Tests EOM detected.	EOM was detected but was not expected. Bit tested is byte 0, bit 2.					R14 = actual data. R16 = expected data.
	0X06	Tests end character counter.	The actual end character counter does not compare with the expected. Bits tested are byte 0, bits 5, 6, and 7.					R14 = actual data R15 = bits in error. R16 = expected data.
	0X07	Tests CCC.	The actual CCC does not compare with the expected. Bits tested are byte 1, bits 2, 3, 4, 5, 6, and 7.					R14 = actual data. R15 = bits in error. R16 = expected data.
	0X08	Tests first 2 bytes of buffer.	First 2 bytes of buffer are in error.					R13 = adr of buffer. R14 = actual data from buffer. R15 = bits in error. R16 = expected data.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1144	0X09	Tests second 2 bytes of buffer.	Second 2 bytes of buffer are in error.					R13 = adr of buffer. R14 = actual data from buffer. R15 = bits in error. R16 = expected data.
	0X0A	Tests third 2 bytes of buffer.	Third 2 bytes of buffer are in error					R13 = adr of buffer. R14 = actual data from buffer. R15 = bits in error. R16 = expected data.
	0X0C	Tests ALC L1 request bit.	ALC L1 request bit not set. Bit tested is byte 1, bit 7 of input reg X'7E'.					Reg X'03' = contents of input reg X'7E'.
	0X0D	Tests for correct L1 irpt adr.	Actual irpt adr does not compare with expected irpt adr.					LAR should point to irpt adr but does not. Reg X'04' = contents of LAR. Reg X'05' = bits in error. Reg X'06' = expected irpt adr.
	0X0E	Tests reset of ALC L1 request bit.	ALC L1 request bit did not reset. Bit tested is byte 1, bit 7.					Reg X'05' = contents of input reg X'7E'.
1145		ALC receive test. This routine should run only when RPQ 858911 is installed. If RPQ 858911 is not installed, check the CDS data.						
	0X01	Tests ALC L1 hardware by altering one instruction in the data processing sequence.	Altered instruction failed to produce an L1 interrupt.					Input reg X'7E' byte 1, bit 7 should be on to indicate ALC support L1 error.
	0X02	Tests EOM remember part 1. Test if expected.	EOM remember was expected but was not detected. Bit tested is byte 0, bit 1.					R14 = actual data. R16 = expected data.
	0X03	Tests EOM remember part 2. Test if detected.	EOM remember detected but not expected. Bit tested is byte 0, bit 1.					R14 = actual data. R16 = expected data.
	0X04	Tests GA part 1. Test if expected.	GA expected but not detected. Bit tested is byte 0, bit 2.					R14 = actual data. R16 = expected data.
	0X05	Tests GA part 2. Test if detected.	GA detected but not expected. Bit tested is byte 0, bit 2.					R14 = actual data. R16 = expected data.
	0X06	Tests CCC remember expected.	CCC remember expected but not detected. Bit tested is byte 0, bit 4.					R14 = actual data. R16 = expected data.
	0X07	Tests CCC remember detected.	CCC remember detected but not expected. Bit tested is byte 0, bit 4.					R14 = actual data. R16 = expected data.
	0X08	Tests end character counter.	The actual end character counter does not compare with the expected data. Bits tested are byte 1, bits 5, 6, and 7.					R14 = actual data. R15 = bits in error. R16 = expected data.
	0X09	Tests CCC.	The actual CCC does not compare with the expected data. Bits tested are byte 1, bits 2, 3, 4, 5, 6, and 7.					R14 = actual data. R15 = bits in error. R16 = expected data.
	0X0A	Tests first 2 bytes of buffer.	First two bytes of buffer are in error.					R13 = adr of buffer. R14 = actual data from buffer. R15 = bits in error. R16 = expected data.
	0X0B	Tests second 2 bytes of buffer.	Second 2 bytes of buffer are in error.					R13 = adr of buffer. R14 = actual data from buffer. R15 = bits in error. R16 = expected data.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1145	0X0C	Tests third 2 bytes of buffer.	Third two bytes of buffer are in error.					R13 = adr of buffer. R14 = actual data from buffer. R15 = bits in error. R16 = expected data.
	0X0D	Tests fourth 2 bytes of buffer.	Fourth 2 bytes of buffer are in error.					R13 = adr of buffer. R14 = actual data from buffer. R15 = bits in error. R16 = expected data.
	0X0E	Tests ALC L1 request bit.	ALC L1 request bit did not set. Bit tested is byte 1, bit 7 of input reg X'7E'.					Reg X'03' = contents of input reg X'7E'.
	0X0F	Tests for correct L1 irpt addr.	Actual irpt adr does not compare with expected irpt adr.					LAR should point to irp adr but does not. Reg X'04' = contents of LAR. Reg X'05' = bits in error. Reg X'06' = expected data.
	0X10	Tests reset of ALC L1 request bit.	ALC L1 request bit did not reset. Bit tested is byte 1, bit 7.					Reg X'05' = contents of input reg X'7E'.
1146	0X01	Storage protect test. Sets all storage keys to 000. The storage keys are first set and then read and compared for the correct key value. The setting and reading of keys is performed by a major subroutine.	One of the storage block keys failed to set to 000.	A-B4D2	0007	CVXXX	6-040	See Note 2.
1147	0X01	Sets all storage keys to 001.	One of the storage block keys failed to set to 001.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
1148	0X01	Sets all storage keys to 010.	One of the storage block keys failed to set to 010.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
1149	0X01	Sets all storage keys to 011.	One of the storage block keys failed to set to 011.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
114A	0X01	Sets all storage keys to 100.	One of the storage block keys failed to set to 100.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
114B	0X01	Sets all storage keys to 101.	One of the storage block keys failed to set to 101.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
114C	0X01	Sets all storage keys to 110.	One of the storage block keys failed to set to 110.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
114D	0X01	Sets all storage keys to 111.	One of the storage block keys failed to set to 111.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
114E	0X01	Storage protect test. Set all protect keys to 000.	One of the protect keys failed to set to 000.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
114F	0X01	Sets all protect keys to 001.	One of the protect keys failed to set to 001.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1150	0X01	Sets all protect keys to 010.	One of the protect keys failed to set to 010.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1151	0X01	Sets all protect keys to 011.	One of the protect keys failed to set to 011.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1152	0X01	Sets all protect keys to 100.	One of the protect keys failed to set to 100.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1153	0X01	Sets all protect keys to 101.	One of the protect keys failed to set to 101.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1154	0X01	Sets all protect keys to 110.	One of the protect keys failed to set to 110.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1155	0X01	Sets all protect keys to 111.	One of the protect keys failed to set to 111.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1156		Special storage protect routine for problem definition mode. This routine will run only if the problem definition mode and the manual intervention CE sense switches are set or if a single routine is requested and the routine requested is 1156. If the PDM CE sense switch is on, a manual intervention code will be displayed. You should then enter the desired key data into switches B, C, D, and E (see Note 2 for format of out set key data. Also note that byte 0, bits 0-3 should be entered into switch B, etc.). The data entered will determine if a storage key or protect key is set and/or read. This test runs under program L4. **Note:** Ensure that the block under test (for setting storage key) does not prevent this routine or the DCM from executing instructions.					
	FX0F	Manual intervention code. You should enter the desired data into switches B, C, D, and E.	N/A		N/A		4-080	For looping on error, the DCM CE sense switch should be set. If not, the routine will make only one pass.
	0X01	The key set is tested to verify that it agrees with the expected data.	Key failed to set to the desired value.		0007		6-040	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
		Storage Protection Mechanism Testing at Program L5. Section 1. The following seven routines test to verify that, if the protect key and storage key match, the user (L5 is the user) is allowed to access storage for instruction execution. Since the protect keys for program levels 1, 2, 3, and 4 are fixed equal to 0, program L5 is set up for the appropriate protect key and the actual test section of each routine is tested at program L5.						
1158		Test that when the storage key is equal to 001 and the protect key (L5) is equal to 001, no storage protect errors occur when an instruction execution is performed.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11 1X21	Pretest error. Pretest error.						
1159		When the storage key is equal to 010 and the protect key (L5) is equal to 010, tests that no storage protect errors occur when an instruction execution is performed.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X12 1X22	Pretest error. Pretest error.						
115A		When the storage key is equal to 011 and the protect key (L5) is equal to 011, test that no storage protect errors occur when an instruction execution is performed.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X13 1X23	Pretest error. Pretest error.						
115B		When the storage key is equal to 100 and the protect key (L5) is equal to 100, tests that no storage protect errors occur when an instruction execution is performed.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X14 1X24	Pretest error. Pretest error.						
115C		Test that when the storage key is equal to 101 and the protect key (L5) is equal to 101, no storage protect errors occur when an instruction execution is performed.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X15 1X25	Pretest error. Pretest error.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
115D		When the storage key is equal to 110 and the protect key (L5) is equal to 110, tests that no storage protect errors occur when an instruction execution is performed.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X16	Pretest error.						
	1X26	Pretest error.						
115E		When the storage key is equal to 111 and the protect key (L5) is equal to 111, tests that no storage protect errors occur when an instruction execution is performed.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X17	Pretest error.						
	1X27	Pretest error.						
		Storage Protection Mechanism Testing at Program L5. Section 2. The following eight routines test to verify that, if protect key and storage key match or if the storage key is 111 (unprotected storage), the user (L5 is the user) is allowed to modify storage without causing protection checks.						
115F		When the storage key is equal to 001 and the protect key (L5) is equal to 001, tests that no storage protect errors occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11	Pretest error.						
	1X21	Pretest error.						
1160		When the storage key is equal to 001 and the protect key (L5) is equal to 010, tests that no storage protect errors occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X12	Pretest error.						
	1X22	Pretest error.						
1161		When the storage key is equal to 011 and the protect key (L5) is equal to 011, tests that no storage protect errors occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X13	Pretest error.						
	1X23	Pretest error.						

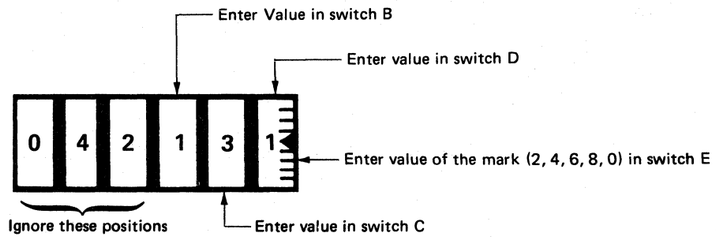
Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1162		When the storage key is equal to 100 and the protect key (L5) is equal to 100, tests that no storage protect errors occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X14 1X24	Pretest error. Pretest error.						
1163		When the storage key is equal to 101 and the protect key (L5) is equal to 101, tests that no storage protect errors occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X15 1X25	Pretest error. Pretest error.						
1164		Test that when the storage key is equal to 110 and the protect key (L5) is equal to 110, no storage protect errors occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X16 1X26	Pretest error. Pretest error.						
1165		When the storage key is equal to 111 and the protect key (L5) is equal to 111, tests that no storage protect errors occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X17 1X27	Pretest error. Pretest error.						
1166		When the storage key is equal to 111 (unprotected storage) and the protect key (L5) is some value other than 111 ((101 for this test)), tests that no storage protect errors occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X15 1X17 1X25	Pretest error. Pretest error. Pretest error.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
		Storage Protection Mechanism Testing at Program L5. Section 3. The following five routines test to verify that if the protect key and the storage key are not equal, the user (L5 is the user) is not allowed to execute an instruction. In addition, protection check should be set.						
116A		When the storage key is equal to 001 and the protect key (L5) is equal to 110, tests that storage protection checks will occur when an attempt is made to execute an instruction.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11	Pretest error.						
	1X16	Pretest error.						
	1X26	Pretest error.						
116F		When the storage key is equal to 110 and the protect key (L5) is equal to 001, tests that storage protection checks will occur when an attempt is made to execute an instruction.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11	Pretest error.						
	1X16	Pretest error.						
	1X21	Pretest error.						
1170		When the storage key is equal to 000 and the protect key (L5) is equal to 111, tests that storage protection checks will occur when an attempt is made to execute an instruction.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X10	Pretest error.						
	1X17	Pretest error.						
	1X27	Pretest error.						
1171		When the storage key is equal to 111 and the protect key (L5) is equal to 000, tests that storage protection checks will occur when an attempt is made to execute an instruction.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X10	Pretest error.						
	1X17	Pretest error.						
	1X20	Pretest error.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1172		When the storage key is equal to 110 and the protect key (L5) is equal to 111, tests that storage protection checks will occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X16	Pretest error.						
	1X17	Pretest error.						
	1X27	Pretest error.						
		Storage Protection Mechanism Testing at Program L5. Section 4. The following six routines test to verify that, if the protect key and the storage key are not equal and if the protect key is not equal to zero, the user (L5) is not allowed to modify storage. In addition, protection check should be set.						
1173		Test that when the storage key is equal to 100 and the protect key (L5) is equal to 110, storage protection checks will occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X14	Pretest error.						
	1X16	Pretest error.						
	1X26	Pretest error.						
1174		When the storage key is equal to 001 and the protect key (L5) is equal to 101, tests that storage protection checks will occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11	Pretest error.						
	1X15	Pretest error.						
	1X25	Pretest error.						
1175		When the storage key is equal to 000 and the protect key (L5) is equal to 100, tests that storage protection checks will occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X10	Pretest error.						
	1X14	Pretest error.						
	1X24	Pretest error.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1177		When the storage key is equal to 011 and the protect key (L5) is equal to 010, tests that storage protection checks will occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X12	Pretest error.						
	1X13	Pretest error.						
	1X22	Pretest error.						
1178		When the storage key is equal to 101 and the protect key (L5) is equal to 001, tests that storage protection checks will occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11	Pretest error.						
	1X15	Pretest error.						
	1X21	Pretest error.						
1179		When the storage key is equal to 100 and the protect key (L5) is equal to 111, tests that storage protection checks will occur when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did occur.	A protection check did not occur	A-B4D2	FFFF	CVXXX	6-040 1-040	
	1X14	Pretest error.						
	1X17	Pretest error.						
	1X27	Pretest error.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1190	The customer usage meter should run when an instruction is executed at program levels 1, 2, 4, 5, and L3 if 8 ms has elapsed since the interval timer irpt occurred or if an instruction is executed at L3 and a non-interval timer irpt has occurred. A series of instructions totaling 24 seconds will be executed on each level for a total run time of 2 minutes (0.034 run time on meter). You will be requested to read and enter the meter at the start of the test and at the end. As a result, this routine will run only if the manual intervention CE sense switch is set. **Customer Usage Meter Test 1** Enter the meter reading as follows (see Figure 1190): 1. When code FX01 is displayed in DISPLAY B, set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5. 2. Ignoring the three leftmost meter positions, enter the remaining positions in STORAGE ADDRESS/REGISTER DATA switches B, C, D, and E. Note that the value entered in switch E represents the marks on the rightmost meter wheel (thousands position). Always round the thousands position to the nearest even number (2, 4, 6, 8, 0). 3. Press the START pushbutton. 4. When code FX02 is displayed in DISPLAY B, enter the new meter reading in the STORAGE ADDRESS/REGISTER DATA switches B, C, D, and E as described in step 2. 5. Press the START pushbutton.				1-040	



For this example you would enter 1 3 1 0 in switches B, C, D, and E

Figure 1190. How to Read the Meter for Test Routine 1190.

	EX01	Display code to indicate that this routine is running (2 min.).		N/A	N/A	N/A		
	FX02	Manual intervention code. Enter the meter value observed in step 4 above.			N/A			1-040
	0X01	The first meter reading is updated by 0.034 and compared with the second reading to verify that the run time is two minutes (0.034 in terms of meter reading).	The meter fail to run correctly or meter reading were not consistent.	A-B3 L2 A-B3 M2	FFFF	CP006 CP007	1-040	Warning: If the meter reading entered under FX01 was between 9.966 and 9.999 inclusive a false error will be reported. Rerun the test again.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1191		Customer usage meter test 2. If no other program levels are active and an L3 interval timer irpt occurs, the customer usage meter should not run until after 8 ms has elapsed. This routine will mask off all execution except the interval timer and update a real time type of count. The customer usage meter should not run during this routine.					1-040	
		Run time is 1 minute.						
	FX01	Same as FX01 above.						
	EX02	Displays code to indicate this routine is running.		N/A	N/A	N/A		
	FX02	Same as FX02 above.						
	0X01	The first meter reading is saved and compared with the second. Since the meter should not run, the two meter readings should be equal.	The meter either ran or meter readings were not consistent.	A-B3 L2 A-B3 M2	FFFF	CP006 CP007	1-040	
Pretest Error Codes The following error codes define failures of functions previously tested by other routines. For each error code a cross reference will be given to point to the routine that originally tested the given function.								
11XX	1X01	Forces an L3 irpt via an output X'7C' to set PCI L3.	L3 irpt failed to occur		N/A		6-940	Routine 1113 previously tested this function. Request routine 1113 and verify that PCI L3 will force an L3 irpt.
11XX	1X02	Forces an L2 irpt via an output to set diag L2 irpt.	L2 irpt failed to occur.		N/A		6-900	The DCM set the L2 mask before loading a given IFT. As a result, L2 must be unmasked before focusing an L2 irpt. Routine 1115 test both the unmasking of L2 irpt and masking of L2 irpt via an output to set diag L2.
11XX	1X03	Forces an irpt via an invalid output reg X'2F'.	L1 irpt failed to occur.		N/A		6-050	Routine 1118 previously tested this function. Request routine 1118 and verify if an L1 irpt can be forced via an I/O check.
11XX	1X10	Sets a given storage key to 000.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 1146 previously tested this function. Run routine 1146 or 1156.
11XX	1X11	Sets a given storage key to 001.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 1147 previously tested this function. Run routine 1147 or 1156.
11XX	1X12	Sets a given storage key to 010.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 1148 tested this function. Run routine 1148 or 1156.
11XX	1X13	Sets a given storage key to 011.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 1149 previously tested this function. Run routine 1149 or 1156.
11XX	1X14	Sets a given storage key to 100.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 114A previously tested this function. Run routine 114A or 1156.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
11XX	1X15	Sets a given storage key to 101.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 114B previously tested this function. Run routine 114B or 1156.
11XX	1X16	Sets a given storage key to 110.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 114C previously tested this function. Run routine 114C or 1156.
11XX	1X17	Sets a given storage key to 111.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 114D previously tested this function. Run routine 114D or 1156.
11XX	1X20	Sets a given protect key to 000.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 114E tested this function. Run routine 114E or 1156.
11XX	1X21	Sets a given protect key to 001.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 114F previously tested this function. Run routine 114F or 1156.
11XX	1X22	Sets a given protect key to 010.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 1150 previously tested this function. Run routine 1150 or 1156.
11XX	1X23	Sets a given protect key to 011.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 1151 previously tested this function. Run routine 1151 or 1156.
11XX	1X24	Sets a given protect key to 100.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 1152 previously tested this function. Run routine 1152 or 1156.
11XX	1X25	Sets a given protect key to 101.	Key failed to set.		N/A		6-040 6-880	See Notes 2 and 5. Routine 1153 previously tested this function. Run routine 1153 or 1156.
11XX	1X26	Sets a given protect key to 110.	Key failed to set.		N/A		6-040	See Notes 2 and 5. Routine 1154 previously tested this function. Run routine 1154 or 1156.
11XX	1X27	Sets a given protect key to 111.	Key failed to set.		N/A		6-880	See Notes 2 and 5. Routine 1155 previously tested this function. Run routine 1155 or 1156.
11XX	2X11	Subroutine to handle L1 irpts.	An L1 irpt has occurred and there are no CCU bits on in either X'7D' CCU check reg or X'7E' irpt req grp 1. All L1 irpts should occur as a result of a CCU type error.	N/A	N/A	N/A	6-840 6-850	Reg X'05' has a dummy bits in error data X'9999'.
11XX	2X12	Subroutine to handle L1 irpts.	An L1 irpt has occurred due to some bit in either irpt req grp 1 X'7E' and/or adapter irpt req grp 1 & 2 X'76' & X'77'. The CCUIFT L1 subroutine resets all forced CCU irpt conditions and determines that all bits cannot be reset.	N/A	N/A		6-810 6-820 6-860	Reg X'05' will contain bits that cannot be reset. If any adapter 21 bits are on, they must be manually reset before pressing START to continue.
11XX	2X13	Subroutine to handle L1 irpts.	An L1 irpt has occurred due to a CCU L1 irpt. The CCUIFT L1 subroutine attempts to reset the L1 interrupt conditions and determines that all bits cannot be reset.	A-B3L2 A-B4D2	N/A	CP005	6-090	Reg X'05' will contain the OR of the CCU ck req X'7D' and irpt req grp 1 X'7E'.
11XX	2X14	Subroutine to handle L1 irpts.	An L1 irpt has occurred and the routine under test did not expect to force an L1 irpt. The irpt occurred due to a CCU error.	N/A	N/A	CK006	6-090	Reg X'05' will contain the OR of the CCU ck req X'7D' and irpt req grp 1 X'7E'.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
11XX	2X15	Subroutine to handle L1 irpts.	An L1 irpt has occurred and the routine under test did not expect to force an L1 irpt. There are not any CCU error bits on; as a result, the irpt must be due to either a CA or CSB request.	N/A	N/A	N/A	6-090 6-810 6-820 6-860	Reg X'05' has a dummy bits in error data X'9999'. Display the following regs to determine the cause of the L1 irpt: X'7F' irpt req grp 2, X'76' adpt req grp 1 and X'77' adpt req grp 2. If any adapter bits are on, they must be manually reset before pressing START to continue.
11XX	2X21	Subroutine to handle L2 irpts.	Diag L2 irpt req bit failed to reset.	A-B3M2	N/A	CU014	6-050	
11XX	2X22	Subroutine to handle L2 irpts.	An L2 irpt has occurred and the diag L2 bit is not on in the irpt req grp 2 X'7F'. When running the CCUIFTs all L2 interrupts should result from Diag L2 bit.	N/A	N/A	N/A	6-850	Reg X'05' will contain irpt req grp 2 X'7F'.
11XX	2X23	Subroutine to handle L2 irpts.	An L2 irpt had occurred and either the type 1 CSB L2 and/or type 2 CSB L2 bits are on in adapter req grp 2 X'77'. The CCUIFT L2 subroutine has attempted to reset by resetting all forced CCU error conditions.	N/A	N/A	CX003	6-820	Reg X'05' will contain adpt req grp 2 X'77'.
11XX	2X24	Subroutine to handle L2 irpts.	An L2 irpt has occurred and the routine under test did not expect to force an L2 irpt.	N/A	N/A	N/A	6-090	Reg X'05' has a dummy bits in error data X'9999'. Display regs: X'77' adpt req grp 2 and X'7F' irpt req grp 2 to determine the cause of the L2 irpt.
11XX	2X31	Subroutine to handle L3 irpts.	An L3 irpt has occurred via a PCI L3 irpt X'7C'. The level sub-routine attempts to reset the PCI L3 irpt, but fails.	A-B3M2	N/A	CU015	6-940	
11XX	2X32	Subroutine to handle L3 irpts.	An L3 irpt has occurred and neither the PCI L3, timer L3, nor pushbutton L3 bits are on. All L3 interrupts that occur should result from one of the above conditions.	N/A	N/A			Reg X'0D' has a dummy bits in error data X'9999'. Reg X'0E' contains adpt req grp 2 X'77'.
11XX	2X33	Subroutine to handle L3 irpts.	An L3 irpt has occurred and either the Type I CAn L3 and/or Type 2 CAn L3 bits are on in adapter req grp 2 X'77'. The CCUIFT L3 subroutine has attempted to reset by resetting all forced CCU errors conditions.	N/A	N/A	CP005	6-820	Reg X'05' will contain adpt req grp 2 X'77'. If any adapter bits are on, they must be manually reset before pressing START to continue.
11XX	2X34	Subroutine to handle L3 irpts.	An L3 irpt has occurred and the routine under test did not expect to force an L3 irpt. The timer L3 and pushbutton L3 interrupts are expected at all times.	N/A	N/A	N/A	6-090	Reg X'0D' has CCU irpt req grp X'7E' loaded. In addition display reg X'77' adpt req grp 2 to determine if a CA L3 irpt req occurred.
11XX	2X41	Subroutine to handle L4 irpts.	A PCI L4 or svc L4 irpt has occurred. The L4 attempts to reset either or both but determines that one or both cannot be reset.	A-B3M2	N/A	CU015	6-090	Reg X'15' contain the irpt req that cannot be reset. Byte 0, bit 7 = PCI L4 and Byte 1, bit 7 = svc L4.
11XX	2X42	Subroutine to handle L4 irpts.	An L4 irpt has occurred and neither the PCI L4 or svc L4 bits are on in X'7F'.	N/A	N/A	CU015 CP005	6-860	Reg X'15' has a dummy bits in error data X'9999'. If any adapter bits are on, they must be manually reset before pressing START to continue.
11XX	2X43	Subroutine to handle L4 irpts.	An L4 irpt has occurred and the routine under test did not expect to force an L4 irpt.	N/A	N/A	N/A	6-090	Reg X'15' has a dummy bits in error data X'0001'. Display req X'7F' CCU IRPT req grp 1. Byte 0, bit 7 = PCI L4 and Byte 1, bit 7 = svc L4.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments

NOTES FOR CCU IFT SYMPTOM INDEX

Note 1: Since the error forcing circuitry has not been previously tested, bypass this error code until error code 0002 of the same routine has been run without failure.

Note 2: For all of the above storage protect testing routines, reg X'16' for error display has special meaning. Req X'16' will contain the data that was sent output to req X'73' (set key). This will allow the block address to be displayed as shown below. See routine 1156 for setting a loop on a given storage or protect key.

Output X'73'	Set Key
Byte 0, 0	SKA Bit 0 ---------- (G)
1	SKA Bit 1 ---------- (H)
2	SKA Bit 2 ---------- (J)
3	SKA Bit 3 ---------- (K)
4	SKA Bit 4 or PKA Bit 0-- (L)
5	SKA Bit 5 or PKA Bit 1-- (M)
6	SKA Bit 6 or PKA Bit 2-- (N)
7	*
Byte 1, 0	*
1	*
2	*
3	Select Key Adr 1=SKA 0=PKA
4	Set Key 1=SET
5	Key – Bit 0
6	Key – Bit 1
7	Key – Bit 2

SAR

Byte	Byte								Byte							
X	0								1							
67	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
GH	J	K	L	M	N	-	-	-	-	-	-	-	-	-	-	-

. . . Use this chart to convert block number into adr range and vice versa.

Exp: If no key adr bits are on, then the block number in question is zero and covers the adr range of 0-4097 bytes.

Note 3: The first two storage block keys are not changed but are allowed to remain set to 000. This will allow direct addressable areas, the DCM control module, and the CCU IFT irpt and subroutine areas to be addressed without protection checks.

Note 4: Only three of the available settable protect keys are currently used.

Note 5: Use the following chart to determine the first suspected card or cards. The table should be keyed off of the failing bits in reg X'15' (bits in error).

Bit in Error Reg X'15'	Failure	Function (Z-Bus)	Card	Logic Page
Byte 0, bit 0	Byte X	ALU, AREG, BREG	A-B4J2	DF976
bit 1	Byte 0	ALU, AREG, BREG	A-B4K2	DG976
bi1 2	Byte 1	ALU, AREG, BREG	A-B4N2	DK976

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments

Note 6: Use the following chart to determine the first suspected card or cards. Key off the failing bits in reg X'15' (bits in error).

Bit in Error Reg X'15'	Failure	Function	Card	Logic Page
Byte 0, bit 1	Byte 0	SDR	A-B4G2	DP993
bit 2	Byte 1	SDR	A-B4A2	DR993

Note 7: Use the following chart to determine the first suspected card or cards. Key off the failing bits in reg X'15' (bits in error).

Bits in Error Reg X'15'	Failure	Function	Card	Logic Page
Byte 0, bit 0	Byte X	SAR	A-B4D2	CV001
bit 1	Byte 0	SAR	A-B4D2	CV001
bit 2	Byte 1	SAR	A-B4C2	DS001

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3705-80 STORAGE IFT SYMPTOM INDEX

ADAPTER CONSIDERATIONS

The entire storage array is considered as one adapter. Errors are detected and displayed by the DCM as established by DCM-IFT conventions.

FAILURE ANALYSIS

Errors in storage control circuits can appear as array card errors when the diagnostics are run. If an array card error is indicated by diagnostics, the suggested procedure is to swap the indicated card with another one and run the same diagnostics again. If the error indications remain the same, panel procedures should be used to test the control circuitry (FETMM, SY27-0209, page 7-260). Error indications are as follows unless noted otherwise in the storage symptom index:

Reg X'13' = failing address
Reg X'14' = actual data received
Reg X'15' = failing data bits ON
Reg X'16' = expected data

All routines except the worst case routine set bybass CCU check stop mode during the test to allow an error display instead of a hardstop. The worst case routine does not set bypass CCU check stop because parity errors must be detected by a CCU check rather than data verification. Set the DIAGNOSTIC CONTROL switch to BYPASS CC CHECK STOP position for an error display of the data bits if desired.

NOTES

Referenced notes are in the back of the storage IFT symptom index.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X2XX	2X01	L1 irpt handler subroutine. Error 1 verifies that a L1 irpt has been caused by address exception condition in the address exception routine.	Unexpected L1 irpt encountered. Address exception expected. Other irpt bit(s) also on. Flag stored by the address exception routine should equal input reg X'7E'. (Irpt Req) Definition of unexpected bits: 1.0 — Address compare 1.2 — In/out check 1.3 — Protection check 1.4 — Invalid op 1.6 — IPL level 1 request				6-090	Reg X'04' = interrupt request bits from input reg X'7E'. Bit 1.1 expected. Reg X'06' = expected data.
X2XX	2X02	L1 irpt handler subroutine: Error 2	An L1 address exception did not occur at expected instruction in address exception routine.				6-050	Reg X'04' = adr of inst following the one causing the L1 interrupt. Reg X'06' = adr of inst following the one that should have caused interrupt.
X2XX	2X03	L1 irpt handler subroutine. Error 3 verifies that address exception condition can be reset.	Address exception bit failed to reset after the expected address exception condition.				6-050	Reg X'7E' bit 0 was set by address exception but could not be reset.
X210		Single bit error correction test. This routine tests the ability to detect and correct a single bit or check bit error in storage. An error is forced via the diagnostic register for each of the data bits in both the on and off condition. The results are tested to verify that the bit was corrected and there is not an existing error already in storage. An error in this routine could be caused by storage support circuitry. Refer to the STORAGE section in Volume 2.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X210	0X01	Single bit error correction.	Failed to correct single bit error. Error was forced via the diagnostic register.				7-220	R14 = actual data. R15 = bit in error.
	0X02	Single bit error correction.	Failed to correct single bit error in complement pattern. Error was forced via the diagnostic register.				7-220	R14 = actual data. R15 = bit in error.
	0X03	Data bit error. Errors already exist in storage.	Unable to verify single bit error correction due to error(s) already existing in storage at several addresses.				7-220	R14 = actual data. R15 = bit in error.
	0X04	Check bit error. Errors already exist in storage.	Unable to verify single bit error correction due to error(s) already existing in storage at several addresses.				7-220	R14 = actual data. R15 = bit in error.
X211		Double bit error detection test. This routine tests the ability to detect a double bit error and provide the correct error indications. Double bit errors are forced via the diagnostic register.						
	0X01	Double bit error detection. Problem may be ECC card or other storage support logic.	Failed to detect a double bit error. CCU check register X'7D' should indicate SDR check.				7-220	R13 = data address R14 = actual bits from CCU check reg X'7D'. R15 = CCU check reg bits in error. R16 = data stored.
X212		Bus out parity test. This routine forces bad parity on CCU bus out via output reg X'78'. If a bus out check occurs, a double bit error condition is indicated to the CCU when that address is read.						
	0X01	Bus out parity.	Op reg check not indicated				7-220	R13 = test address. R14 = data read from test address (should = X'0000'). R15 = CCU check reg bits received (should contain op reg check).
X213		Address exception test. This routine tests ability to generate an address exception L1 interrupt or fold condition in which the data is stored in address zero. Flags are set to indicate to the L1 interrupt that an address exception L1 Interrupt is expected. The interrupt or fold should occur during an attempt to store into an invalid address.						
	0X01	CDS, input X'70' compare.	Number of 32K increments derived from CDS and input X'70' do not compare.					R14 = number of 32 increments taken from CDS data, after one shift left and should compare with input X'70'. Example: 256K in CDS = 8800, after one shift left = 1000. 256K in input req X'70' = 1000. R15 = bits in error. R16 = input X'70'.
	0X02	Address exception or fold. For 256K the maximum address +2 = address 0 or fold.	Failed to indicate address exception or fold. The address should fold to zero.					R13 = maximum valid address determined from input req X'70'. R14 = Data read from address zero. Should be zero due to fold condition.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X214		Double bit error pattern test. This routine stores, loads and tests a pattern, its complement and its recomplement. Two patterns are used to provide bit variation. No errors are forced via the diagnostic register. If a double bit error occurs, a test is made to determine which card the bits are on, in which case the card is identified. If the bits in error are on both cards of a pair, information is saved from worst card analysis (routine #15). Pattern 1 = 5555/AAAA Pattern 2 = 8001/7FFE						
	0X01	Double bit error.	Double bit errors have occurred and the errors have been determined to be in a single array card as identified by reg X'15' displacement value.				7-220	R13 = failing adr. R15 = displacement into worst card table. (See note 1.)
	0X02	Double bit error. If routine 14 was run as single routine request continue to termination and request routine 15. If problem definition SSW was set at IFT select, continue. If it was not, set 9101 in data switches, function 1, and continue.	Double bit errors have occurred, but cannot be isolated to a single array card. Suggested procedure is to set DCM sense switch for problem definition to cause routine #15 to be run, or run the routine as a single routine. A flag is set to cause routine #15 to test only the failing array cards.				7-220	R13 = failing adr at which the double bit error occurred.
X215		Single bit error pattern test. **Note:** This routine runs in problem definition mode. Either the DCM sense switch should be set for problem definition or the routine should be run as a single routine request. This routine stores, loads, and tests a pattern, its complement and its recomplement. Two patterns are used to provide bit variation. ***Single Bit error Forced*** Pattern 1 = 5555/AAAA Pattern 2 = 8001/7FFE						
	0X01	Worst card analysis.	The worst card has been determined.				7-220	R15 byte 1 = displacement into worst card table. See Note 1. If reg 15 = X'10', worst card = position U2.
	0X02	Worst card analysis — the worst card is the card with the greatest number of single bit errors.	Double bit error detected in routine 14 has determined worst card within the range of addresses where the double bit error exists.				7-220	R15 byte 1 = displacement into worst card table. See Note 1. If reg 15 = X'10', position U2.
	E0XX	This code is displayed because routine 15 takes longer than 20 seconds to run. It indicates only that the routine is running and is not in a loop.						

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Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X216		Address Failure Analysis. This Routine attempts to analyze a solid addressing failure by storing each address in its own location as data. Failures are saved for a composite error display, from which consistent address bits can be analyzed. Failing pattern can be determined by combining bits consistently ON from error code 0X01 and bits consistently OFF from error code 0X02. Bit definitions are as follows: BYTE X X 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 X X X X X X X X X X X X X X X X CSY CSX SAR Bits Unused Card Select off = T2, on = U2						
	0X01	Address failure analysis.	Addressing failure. Replace bits in address layout with a 1 for each bit ON in reg X'15'. Continue to error code 0X02 to complete failing pattern.				7-220	R15 = bits consistently ON in all failures.
	0X02	Address failure analysis.	Addressing failure. Replace bits in address layout with a 0 for each bit ON in reg X'15'. Bits remaining as X after error code 0X01 and 0X02 were not consistent in the failures.				7-220	R15 = bits consistently OFF in all failures.
X217		Addressing capability. This routine checks addressing capability by storing each location with its own address as data and testing that the data was stored correctly.						
	0001	Addressing capability.	Addressing failure. Compare expected and actual data to determine address bits in error.				7-230	R13 = failing address. R14 = actual data. R15 = bits in error. R16 = expected data.

NOTE 1: ARRAY CARD IDENTIFICATION

R15 Displacement	Card Location	Address Range
00 or 02	T2	00000-07FFE
04 or 06	T2	08000-0FFFE
08 or 0A	T2	10000-17FFE
0C or 0E	T2	18000-1FFFE
10 or 12	U2	20000-27FFE
14 or 16	U2	28000-2FFFE
18 or 1A	U2	30000-37FFE
1C or 1E	U2	38000-3FFFE

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3705-80 TYPE 1 CA IFT SYMPTOM INDEX

3705-80 Type 1 Channel Adapter (CA) Symptom Index

The type 1 CA IFT symptom index is a listing of error codes relating to failures occurring during the operation of the IFT. All bits of the CA registers which have both input and output capability are tested with several patterns, including all ones, zeros, every other bit, growing ones, and floating zeros patterns. Interaction between the registers is also checked. In addition to verification of register operation, the function of program requested and suppress-out monitor level 3 interrupts are verified. Error codes are also given for unexpected and/or unknown level 1 (L1) and level 3 (L3) interrupts and if the CA interface was not disabled.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1301	0X01	Disable CA type 1 interface.	Channel interface was not disabled.	A4P2	0008	RC103		
1302	0X02	CA diagnostic reset.	Did not clear reg X'60'.	A4L2	FFFF	RC402	8-130	
	0X04	CA diagnostic reset.	Did not clear reg X'62'.	A4L2	FFFF	RC403	8-130	
	0X08	CA diagnostic reset.	Did not clear reg X'66'.	A4T2	FFFF	RC601	8-130	
	0X09	CA diagnostic reset.	Did not clear reg X'67'.	A4K2	00FF	RC505	8-130	
1303	0X0A	Set reg X'63' to X'0000'.	Unable to set reg X'63' to X'0000'.	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
1304	0X0B	Set reg X'63 to X'FFFF'.	Unable to set reg X'63' to X'FFFF'.	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
1305	0X0C	Set reg X'63' to X'5555'.	Unable to set reg X'63' to X'5555'.	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
	0X0D	Set reg X'63' to X'AAAA'.	Unable to set reg X'63' to X'AAAA'.	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
1306	0X0E	Set reg X'63' using floating zeros pattern.	Unable to set reg X'63' using floating zeros pattern.	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
1307	0X0F	Set reg X'63' using growing ones pattern.	Unable to set reg X'63' using growing ones pattern.	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
1308	0X0A	Set reg X'64' to X'0000'.	Unable to set reg X'64' to X'0000'.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
1309	0X0B	Set reg X'64' to X'FFFF'.	Unable to set reg X'64' to X'FFFF'.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130A	0X0C	Set reg X'64' to X'5555'.	Unable to set reg X'64' to X'5555'.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
	0X0D	Set reg X'64' to X'AAAA'.	Unable to set reg X'64' to X'AAAA'.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130B	0X0E	Set reg X'64' using floating zeros pattern.	Unable to set reg X'64' using floating zeros pattern.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
130C	0X0F	Set reg X'64' using growing ones pattern.	Unable to set reg X'64' using growing ones pattern.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130D	0X0A	Set reg X'65' to X'0000'.	Unable to set reg X'65' to X'0000'.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130E	0X0B	Set reg X'65' to X'FFFF'.	Unable to set reg X'65' to X'FFFF'.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130F	0X0C	Set reg X'65' to X'5555'.	Unable to set reg X'65' to X'5555'.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
	0X0D	Set reg X'65' to X'AAAA'.	Unable to set reg X'65' to X'AAAA'.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
1310	0X0E	Set reg X'65' using floating zeros pattern.	Unable to set reg X'65' using floating zeros pattern.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
1311	0X0F	Set reg X'65' using growing ones pattern.	Unable to set reg X'65' using growing ones pattern.	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
1312	0X0B	Set reg X'66' to X'CF00' by output of X'40CF' to reg X'66'.	Unable to set reg X'66' to X'CF00'.	A4T2	FFFF	RC601	8-120	
1313	0X0C	Set reg X'66' to X'4500' by output of X'0045' to reg X'66'.	Unable to set reg X'66' to X'4500'.	A4T2	FFFF	RC601	8-120	
	0X0D	Set reg X'66' to X'8A00' by output of X'008A' to reg X'66'.	Unable to set reg X'66' to X'8A00'.	A4T2	FFFF	RC601	8-120	
1314	0X0E	Set reg X'66' using floating zeros pattern.	Unable to set reg X'66' using floating zeros pattern.	A4T2	CF00	RC601	8-120	
1315	0X0F	Set reg X'66' using growing zeros pattern.	Unable to set reg X'66' using growing zeros pattern.	A4T2	CF00	RC601	8-120	
1316	0X0A	Set reg X'62' to X'0000'.	Unable to set reg X'62' to X'0000'.	A4L2	FFFF	RC403	8-080	
1317	0X10	Set reg X'62' to X'8000' outbound transfer sequence.	Unable to set reg X'62' to X'8000'.	A4L2	FFFF	RC403	8-080	
1318	0X11	Set reg X'62' to X'4000' inbound transfer sequence.	Unable to set reg X'62' to X'4000'.	A4L2	FFFF	RC403	8-080	
1319	0X12	Set reg X'62' to X'2000' ESC final status transfer sequence.	Unable to set reg X'62' to X'2000'.	A4L2	FFFF	RC403	8-080	
131A	0X13	Set reg X'62' to X'1000' NSC channel end transfer sequence.	Unable to set reg X'62' to X'1000'.	A4L2	FFFF	RC403	8-080	
	0X14	Set Channel End status when setting reg X'62' to X'1000'.	Unable to set reg X'66' to X'0800'.	A4L2	FFFF	RC601	8-080	
131B	0X15	Set reg X'62' to X'0800' NSC final status transfer sequence.	Unable to set reg X'62' to X'0800'.	A4L2	FFFF	RC403	8-080	
	0X16	No bits are set in reg X'66' when setting reg X'62' to X'0800'.	Reg X'66' not all zeros.	A4T2	FFFF	RC601	8-080	
131C	0X0A	Pretest. Set reg X'62' to X'0000'.	Unable to set reg X'62' to X'0000'.	A4L2	FFFF	RC403		Reg X'65' set incorrectly.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
131C	0X20	Set L3 program requested irpt.	L3 irpt did not occur.	A4T2	0006	RC601	8-080	
131D	0X0A	Pretest. Set reg X'62' to X'0000'.	Unable to set reg X'62 to X'0000'.	A4L2	FFFF	RC403		Rerun routine 1303.
	0X21	Set suppress out monitor.	L3 irpt did not occur.	A4T2	000A	RC602	8-080	
131E	0X0A	Pretest. Set reg X'63' to X'0000'.	Unable to set reg X'63' to X'0000'.	A4M2	FFFF	RC403		
	0X40	When X'0000' is set in reg X'63' it does not set reg X'64'.	Reg X'64' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-100 8-110	
	0X41	When X'0000' is set in reg X'63' it does not set reg X'65'.	Reg X'65' set incorrectly.	A4D2, A4K2	FFFF	RC402	8-100 8-110	
	0X42	When X'0000' is set in reg X'63' it does not set reg X'66'.	Reg X'66' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-100 8-120	
131F	0X0A	Pretest. Set reg X'64' to X'0000'.	Unable to set reg X'64' to X'0000'.	A4M2	FFFF	RC502		Rerun routine 1308.
	0X43	When X'0000' is set in reg X'64' it does not set reg X'65'.	Reg X'65' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-110 8-120	
	0X44	When X'0000' is set in reg X'64' it does not set reg X'66'.	Reg X'66' set incorrectly.	A4D2, A4K2	FFFF	RC601	8-110 8-120	
	0X45	When X'0000' is set in reg X'64' it does not set reg X'63'.	Reg X'63' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-100 8-110	
1320	0X0A	Pretest. Set reg X'65' to X'0000'.	Unable to set reg X'65' to X'0000'.	A4M2	FFFF	RC502		Rerun routine 130D.
	0X46	When X'0000' is set in reg X'65' it does not set reg X'66'.	Reg X'66' set incorrectly.	A4D2, A4K2	FFFF	RC601	8-110	
	0X47	When X'0000' is set in reg X'65' it does not set reg X'63'.	Reg X'63' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-110 8-100	
	0X48	When X'0000' is set in reg X'65' it does not set reg X'64'.	Reg X'64' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-110	
1321	0X0B	Pretest. Set reg X'63' to X'FFFF'.	Unable to set reg X'63' to X'FFFF'.	A4M2	FFFF	RC502		Rerun routine 1304.
	0X4C	When X'FFFF' is set in reg X'63' it does not set reg X'64'.	Reg X'64' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-100 8-110	
	0X4D	When X'FFFF' is set in reg X'63' it does not set reg X'65'.	Reg X'65' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-100 8-110	
	0X4E	When X'FFFF' is set in reg X'63' it does not set reg X'66'.	Reg X'66' set incorrectly.	A4D2, A4K2	FFFF	RC601	8-100 8-120	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1321	0X4F	When X'FFFF' is set in reg X'63' it does not set reg X'60'.	Reg X'60' set incorrectly.	A4D2, A4K2	FFFF	RC402	8-100 8-120	
	0X51	When X'FFFF' is set in reg X'63' it does not set reg X'62'.	Reg X'62' set incorrectly.	A4D2, A4K2	FFFF	RC403	8-100 8-080	
1322	0X0B	Pretest. Set reg X'64 to X'FFFF'.	Unable to set reg X'64' to X'FFFF'.	A4M2	FFFF	RC502		Rerun routine 1309.
	0X52	When X'FFFF' is set in reg X'64' it does not set reg X'65'.	Reg X'65' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-110	
	0X53	When X'FFFF' is set in reg X'64' it does not set reg X'66'.	Reg X'66' set incorrectly.	A4D2, A4K2	FFFF	RC601	8-110 8-120	
	0X54	When X'FFFF' is set in reg X'64' it does not set reg X'60'.	Reg X'60' set incorrectly.	A4D2, A4K2	FFFF	RC402	8-110 8-070	
	0X56	When X'FFFF' is set in reg X'64' it does not set reg X'62'.	Reg X'62' set incorrectly.	A4D2, A4K2	FFFF	RC403	8-080 8-110	
	0X57	When X'FFFF' is set in reg X'64' it does not set reg X'63'.	Reg X'63' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-100 8-110	
1323	0X0B	Pretest. Set reg X'65' to X'FFFF'.	Unable to set reg X'65' to X'FFFF'.	A4M2	FFFF	RC502		Rerun routine 130E.
	0X58	When X'FFFF' is set in reg X'65' it does not set reg X'66'.	Reg X'66' set incorrectly.	A4D2, A4K2	FFFF	RC601	8-120 8-110	
	0X59	When X'FFFF' is set in reg X'65' it does not set reg X'60'.	Reg X'60' set incorrectly.	A4D2, A4K2	FFFF	RC402	8-070 8-110	
	0X5B	When X'FFFF' is set in reg X'65' it does not set reg X'62'.	Reg X'62' set incorrectly.	A4D2, A4K2	FFFF	RC403	8-080 8-110	
	0X5C	When X'FFFF' is set in reg X'65' it does not set reg X'63'.	Reg X'62' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-100 8-110	
	0X5D	When X'FFFF' is set in reg X'65' it does not set reg X'64'.	Reg X'64' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-110	
	0X5E	When X'00CF' is set in reg X'66' it does not set reg X'60'.	Reg X'60' set incorrectly.	A4D2, A4K2	FFFF	RC402	8-120 8-070	
1324	0X0B	Pretest. Output X'00CF' to reg X'66'.	Input from reg X'66' not X'CF00'.	A4T2	FFFF	RC601		Rerun routine 1312.
	0X60	When X'00CF' is set in reg X'66' it does not set reg X'62'.	Reg X'62' set incorrectly.	A4D2, A4K2	FFFF	RC403	8-120 8-080	

3705-80 TYPE 1 CA IFT SYMPTOM INDEX - Cont.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
1324	0X61	When X'00CF' is set in reg X'66' it does not set reg X'63'.	Reg X'63' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-120 8-120	
	0X62	When X'00CF' is set in reg X'66' it does not set reg X'64'.	Reg X'64' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-120 8-110	
	0X63	When X'00CF' is set in reg X'66' it does not set reg X'65'.	Reg X'65' set incorrectly.	A4D2, A4K2	FFFF	RC502	8-120 8-110	
13XX	1X01	Disable CA type 1 interface.	Channel interface was not disabled.	A4P2	0008	RC103	8-130	
	1X0A	Set regs to X'0000'.	Unable to set regs to X'0000'.	A4M2, A4P2	FFFF	RC501	8-100 8-110	
	1X0B	Set all used bit positions to ones.	Unable to set ones to all used bit positions.	A4M2, A4P2	FFFF	RC501	8-100 8-110	
	2X00	Unexpected L1 irpt.	L1 irpt with no request bits on.	A4K2	XXXX	RC505	8-340	
	2X01	Unexpected L3 irpt.	Initial selection L3 irpt bit on in reg X'77' (bit 1.4).	A4L2	XXXX	RC402		
	2X02	Reset initial selection L3 irpt.	Failed to reset initial selection L3 irpt.	A4L2	XXXX	RC402	8-080	
	2X03	Unexpected L3 irpt.	Data/status L3 irpt bit on in reg X'77' (bit 1.3) without suppress out monitor or program requested irpt bits on in reg X'67'.	A4L2	XXXX	RC403	8-090	Reg X'62' should indicate cause irpt.
	2X04	Reset data/status L3 irpt.	Failed to reset data/status L3 irpt.	A4L2	XXXX	RC602	8-080	
	2X05	Unexpected suppress out L3 irpt.	Suppress out L3 irpt bit on in reg X'77' (bit 0.6).	A4T2	XXXX	RC602		
	2X06	Reset suppress out monitor L3 irpt.	Failed to reset suppress out monitor.	A4T2	XXXX	RC602	8-080	
	2X07	Unexpected L3 irpt.	Unexpected program reg irpt.	A4T2	XXXX	RC602	8-090	
	2X08	Reset program requested L3 irpt.	Failed to reset program requested L3 irpt.	A4T2	XXXX	RC602	8-080	
	2X09	Unexpected L3 irpt from type 1 CA.	No request bits on in reg X'62'.	A4L2, A4T2	XXXX	RC407	8-090	
	2X1X	Unexpected L1 irpt.	Local store check.	A4K2	XXXX	RC505	8-340	See Note 1.
	2X2X	Unexpected L1 irpt.	CCU outbus check.	A4K2	XXXX	RC505	8-340	See Note 1.
	2X4X	Unexpected L1 irpt.	I/O inst accept check.	A4K2	XXXX	RC505	8-340	See Note 1.
	2X8X	Unexpected L1 irpt.	Channel bus-in check.	A4K2	XXXX	RC505	8-340	See Note 1.
	2XFF	Reset unexpected L1 irpt.	Failed to reset L1 irpt.	A4K2	XXXX	RC505	8-130	See Note 1.

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3705-80 TYPE 1 CA IFT SYMPTOM INDEX - Cont.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments

NOTES:

Note 1: Combinations of more than one L 1 irpt cause will be indicated by Y in error code X'2XYX' and these causes can be separated into codes X'2X1X' – X'2X8X'.

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3705-80 TYPE 4 CA IFT SYMPTOM INDEX

The type 4 CA IFT symptom index is a listing of error codes relating to failures occurring during the operation of the IFT. All bits of the CA registers which have both input and output capability are tested with several patterns, including all ones, zeros, every other bit, growing ones, and floating zeros patterns. Interaction between the registers is also checked. In addition to verification of register operation, the function of program requested and suppress-out monitor level 3 interrupts are verified. Error codes are also given for unexpected and/or unknown level 1 (L1) and level 3 (L3) interrupts and if the CA interface was not disabled.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X901		Select type 4 CA.						
	0X01		Unable to select type 4 CA.	E4F2		PA108	H-120	Reg X'14' contains the results of an IN X'67' instruction executed after the selection failed.
	0X02		Unable to select type 4 CA.	E4F2		PA108	H-120	Reg X'14' contains the results of an IN X'77' instruction executed after the selection failed.
X902	0X01	Disable type 4 CA interface.	Type 4 CA interface was not disabled.	E4P2		PB103	H-120	
X903		Type 4 CA diagnostic reset.						
	0X02		Did not clear reg X'60'.	E4Q2 E4K2 E4N2 E4L2		PH107 PF103 PC105 PE102	H-120 H-050	Any bits. Bit 0.6. Bit 0.1, 0.2, 0.7. Bit 0.1, 0.3, 0.5.
	0X04		Did not clear reg X'62'.	E4Q2 E4L2 E4T2 E4N2 E4K2		PH107 PE103 PG102 PC104 PF104	H-120 H-070	Any bits. Bits 0.0-0.4, 1.0, 1.5-1.7. Bits 0.6, 0.7. Bits 0.5, 1.1, 1.3. Bits 1.2, 1.4.
	0X08		Did not clear reg X'66'.	E4Q2 E4M2 E4T2		PH107 PD108 PG102	H-120 H-100	Any bits. Bits 0.0, 0.1, 0.4, 0.5. Bits 0.6, 0.7.
	0X09		Did not clear reg X'67'.	E4Q2 E4K2 E4F2		PH107 PF104 PA108	H-120 H-110	Any bits. Bits 1.1-1.5. Bits 1.6-1.7.
	0X0A		Did not clear reg X'6C'.	E4Q2 E4H2 E4E2		PH107 PL102 PQ104	H-120 H-130	Any bits. Bit 0.0. Bit 0.1.
X904	0X0A	Set reg X'63' (SSAR) to X'0000' (all zeros).	Unable to set reg X'63' to X'0000'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-080	
X905	0X0B	Set reg X'63' (SSAR) to X'FFFF' (all ones).	Unable to set reg X'63' to X'FFFF'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-080	
X906	0X0C	Set reg X'63' to X'5555'.	Unable to set reg X'63' to X'5555'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-080	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X906 (cont.)	0X0D	Set reg X'63' to X'AAAA'.	Unable to set reg X'63' to X'AAAA'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-080	
X907	0X0E	Set reg X'63' (SSAR) using growing ones pattern.	Unable to set reg X'63' using growing ones pattern.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-080	
X908	0X0F	Set reg X'63' using floating zeros pattern.	Unable to set reg X'63' using floating zeros pattern.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-080	
X909	0X0A	Set reg X'64' (data reg 1 and 2) to X'0000' (all zeros).	Unable to set reg X'64' to X'0000'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	
X90A	0X0B	Set reg X'64' to X'FFFF' (all ones).	Unable to set reg X'64' to X'FFFF'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	
X90B	0X0C	Set reg X'64' to X'5555'.	Unable to set reg X'64' to X'5555'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	
	0X0D	Set reg X'64' to X'AAAA'.	Unable to set reg X'64' to X'AAAA'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	
X90C	0X0E	Set reg X'64' using floating zeros pattern.	Unable to set reg X'64' using floating zeros pattern.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	
X90D	0X0F	Set reg X'64' using growing ones pattern.	Unable to set reg X'64' using growing ones pattern.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	
X90E	0X0A	Set reg X'65' to X'0000' (all zeros).	Unable to set reg X'65' to X'0000'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	
X90F	0X0B	Set reg X'65' to X'FFFF'.	Unable to set reg X'65' to X'FFFF'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X910	0X0C	Set reg X'65' to X'5555'.	Unable to set reg X'65' to X'5555'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	
	0X0D	Set reg X'65' to X'AAAA'.	Unable to set reg X'65' to X'AAAA'.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	
X911	0X0E	Set reg X'65' using floating zeros pattern.	Unable to set reg X'65' using floating zeros pattern.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	
X912	0X0F	Set reg X'65' using growing ones pattern.	Unable to set reg X'65' using growing ones pattern.	E4M2 E4P2 E4K2		PD107 PB106 PF102	H-090	
X913	0X0B	Set reg X'66' to X'CF00' by output of X'40CF' to reg X'66'.	Unable to set reg X'66' to X'CF00'.	E4T2		PG101	H-100	
X914	0X0C	Set reg X'66' to X'4500' by output of X'0045' to reg X'66'.	Unable to set reg X'66' to X'4500'.	E4T2		PG101	H-100	
	0X0D	Set reg X'66' to X'8A00' by output of X'008A' to reg X'66'.	Unable to set reg X'66' to X'8A00'.	E4T2		PG101	H-100	
X915	0X0E	Set reg X'66' using floating zeros pattern.	Unable to set reg X'66' using floating zeros pattern.	E4T2		PG101	H-100	
X916	0X0F	Set reg X'66' using growing ones pattern.	Unable to set reg X'66' using growing ones pattern.	E4T2		PG101	H-100	
X917	0X0A	Set reg X'62' to X'0000'.	Unable to set reg X'62' to X'0000'.	E4L2 E4T2 E4N2		PE103 PG102 PC104	H-060	
X918	0X10	Set reg X'62' to X'8000' outbound transfer sequence.	Unable to set reg X'62' to X'8000'.	E4L2		PE103	H-060	
X919	0X11	Set reg X'62' to X'4000' inbound transfer sequence.	Unable to set reg X'62' to X'4000'.	E4L2		PE103	H-060	
X91A	0X12	Set reg X'62' to X'2000' ESC final status transfer sequence.	Unable to set reg X'62' to X'2000'.	E4L2		PE103	H-060	
X91B	0X13	Set reg X'62' to X'1000', NCS channel end transfer sequence.	Unable to set reg X'62' to X'1000'.	E4L2		PE103	H-060	
	0X14	Set reg X'66' to X'0800', channel end status.	Unable to set reg X'66' to X'0800'.	E4L2 E4T2		PE103 PG101	H-060	
X91C	0X15	Set reg X'62' to X'0800' NCS final status transfer sequence.	Unable to set reg X'62' to X'0800'.	E4L2		PE103	H-060	
	0X16	No bits are set in reg X'66' when setting reg X'62' to X'0800'.	Reg X'66' not all zeros.	E4T2 E4L2		PG101 PE103	H-060	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X91D	0X0A	Set Reg X'62' to X'0000' during pretest.	Unable to set reg X'62' to X'0000'.	E4L2		PE103	H-060	Rerun routine X917.
	0X20	Set L3 program-requested irpt.	Irpt did not occur.	E4T2		PG102	H-120	
X91E	0X0A	Set reg X'62' to X'0000' during pretest.	Unable to set reg X'62' to X'0000'.	E4L2		PE103	H-060	Rerun routine X917.
	0X21	Set suppress out monitor.	L3 irpt did not occur.	E4T2		PG102	H-120	
X91F	0X0A	Status service and adr reg address test. Set all bits off in reg X'63' and verify that regs X'64', X'65', and X'66' are set correctly.	Unable to set reg X'63' to X'0000'.	E4M2		PD107	H-080	Rerun routine X904.
	0X40		Reg X'64' set incorrectly.	E4F2 E4K2		PA101 PF101	H-080 H-090	
	0X41		Reg X'65' set incorrectly.	E4F2 E4K2		PA101 PF101	H-080 H-090	
	0X42		Reg X'66' set incorrectly.	E4F2 E4K2		PA101 PF101	H-080 H-090	
X920	0X0A	Data regs 1 and 2 address test. Set all bits off in reg X'64' and verify that regs X'63', X'65' and X'66' are set correctly.	Unable to set reg X'64' to X'0000'.	E4M2		PD107	H-090	Rerun routine X909.
	0X43		Reg X'65' set incorrectly.	E4F2 E4K2		PA101 PF101	H-090 H-090	
	0X44		Reg X'66' set incorrectly.	E4F2 E4K2		PA101 PF101	H-090 H-090	
	0X45		Reg X'63' set incorrectly.	E4F2 E4K2		PA101 PF101	H-080 H-090	
X921	0X0A	Data regs 3 and 4 address test. Set all bits off in reg X'65' and verify that regs X'63', and X'64' and X'66' are set correctly.	Unable to set reg X'65' to X'0000'.	E4M2 E4P2		PD107 PB106	H-090	
	0X46		Reg X'66' set incorrectly.	E4F2 E4K2		PA101 PF101	H-090 H-100	
	0X47		Reg X'63' set incorrectly.	E4F2 E4K2		PA101 PF101	H-080 H-090	
	0X48		Reg X'64' set incorrectly.	E4F2 E4K2		PA101 PT101	H-090	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X922	0X0B	Status service and adr reg address test. Set all bits on in reg X'63' and verify that regs X'60', X'62', X'64', X'65' and X'66' are set correctly.	Unable to set reg X'63' to X'FFFF'.	E4M2 E4P2		PD107 PB106	H-080	
	0X4C		Reg X'64' set incorrectly.	E4F2 E4K2		PA101 PF101	H-080 H-090	
	0X4D		Reg X'65' set incorrectly.	E4F2 E4K2		PA101 PF101	H-080 H-090	
	0X4E		Reg X'66' set incorrectly.	E4F2 E4K2		PA101 PF101	H-080 H-100	
	0X4F		Reg X'60' set incorrectly.	E4F2 E4K2		PA101 PF101	H-080 H-050	
	0X51		Reg X'62' set incorrectly.	E4F2 E4K2		PA101 PF101	H-060 H-080	
X923	0X0B	Data regs 1 and 2 address test. Set all bits on in reg X'64' and verify that regs X'60', X'62', X'63', X'65' and X'66' are set correctly.	Unable to set reg X'64' to X'FFFF'.	E4M2 E4P2		PD107 PB106	H-090	
	0X52		Reg X'65' set incorrectly.	E4F2 E4K2		PA101 PF101	H-090	
	0X53		Reg X'66' set incorrectly.	E4F2 E4K2		PA101 PF101	H-090 H-100	
	0X54		Reg X'60' set incorrectly.	E4F2 E4K2		PA101 PF101	H-090 H-050	
	0X56		Reg X'62' set incorrectly.	E4F2 E4K2		PA101 PF101	H-060 H-090	
	0X57		Reg X'63' set incorrectly.	E4F2 E4K2		PA101 PF101	H-080 H-090	
X924	0X0B	Data regs 3 and 4 address test. Set all bits on in reg X'65' and verify that regs X'60', X'62', X'63', X'64', and X'66' are set correctly.	Unable to set reg X'65' to X'FFFF'.	E4M2 E4P2		PD107 PB106	H-090	
	0X58		Reg X'66' set incorrectly.	E4F2 E4K2		PA101 PF101	H-090 H-100	
	0X59		Reg X'60' set incorrectly.	E4F2 E4K2		PA101 PF101	H-050 H-090	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X924 (cont.)	0X5B		Reg X'62' set incorrectly.	E4F2 E4K2		PA101 PF101	H-060 H-090	
	0X5C		Reg X'63' set incorrectly.	E4F2 E4K2		PA101 PF101	H-080 H-090	
	0X5D		Reg X'64' set incorrectly.	E4F2 E4K2		PA101 PF101	H-090	
X925	0X0B	NSC status reg address test. Set reg X'66' to X'00CF' and verify that no bits are set on in regs X'60', X'62', X'63', X'64' and X'65'.	Reg X'66' set incorrectly.	E4T2		PG101	H-100	
	0X5E		Reg X'60' set incorrectly.	E4F2 E4K2		PA101 PF101	H-100 H-050	
	0X60		Reg X'62' set incorrectly.	E4F2 E4K2		PA101 PF101	H-060 H-100	
	0X61		Reg X'63' set incorrectly.	E4F2 E4K2		PA101 PF101	H-100 H-080	
	0X62		Reg X'64' set incorrectly.	E4F2 E4K2		PA101 PF101	H-100 H-090	
	0X63		Reg X'65' set incorrectly.	E4F2 E4K2		PA101 PF101	H-090 H-100	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X92E		Reset EB mode and CS mode with an OUT X'62': 1. CS mode is set with an output of X'4000' to reg X'6C'. 2. CS mode is reset with an output of X'0100' to reg X'62'. 3. An IN reg X'6C' is performed to verify that mode bits 0.0 and 0.1 are 0. 4. EB mode is set with an output of X'8000' to reg X'6C'. 5. EB mode is reset with an output of X'0100' to reg X'62'. 6. An IN reg X'6C' is performed to verify that mode bits 0.0 and 0.1 are 0.						
	0X01		Unable to reset CS mode.	E4H2		PL102	H-140	
	0X02		Unable to reset EB mode.	E4J2		PL103	H-130	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X930		EB mode control reg – all zeros. The CA4 is disabled and reset. Certain EB mode control reg bits are set with an OUT X'6C', reset with an OUT X'6C' and the results verified with an IN X'6C'. Two passes of the routine are made. The bits tested and the expected results are shown in the "Comments" column.						Reg X'15' contains the results of the IN X'6C' instruction. The EB mode control reg bits tested and the expected results are: Pass Bit Description 1 2 0.0 EB mode 1 0 0.1 CS mode 0 1 0.4 Syn monitor ctrl lt 0 0 0.5 DLE remember lt 0 0 0.6 ASCII monitor ctrl lt 0 0 0.7 EBCDIC monitor ctrl lt 0 0
	0X01		Failure occurred on first pass.	E4H2		PL102	H-140	
	0X02		Failure occurred on second pass.	E4E2		PL104	H-140	
X932		EB mode control reg – all ones. The CA4 is disabled and reset. Certain EB mode control reg bits are reset with an OUT X'6C', set with an OUT X'6C', and the results verified with an IN X'6C'. Two passes of the routine are made. The bits tested and the expected results are shown in the "Comments" column.						Reg X'15' contains the results of the IN X'6C' instruction. The EB mode control reg bits tested and the expected results are: Pass Bit Description 1 2 0.0 EB mode 1 0 0.1 CS mode 0 1 0.4 Syn monitor ctrl lt 0 0 0.5 DLE remember lt 0 0 0.6 ASCII monitor ctrl lt 0 0 0.7 EBCDIC monitor ctrl lt 0 0
	0X01		Failure occurred on first pass.	E4H2		PL102	H-140	
	0X02		Failure occurred on second pass.	E4E2 E4H2 E4H2 E4H2 E4H2		PQ104 PL105 PL101 PL101 PL101	H-140 H-140 H-140 H-140 H-140	
X934		EB mode adr reg reset. After the CA4 is disabled and reset, EB mode is set and an OUT X'62' is executed to reset the EB mode adr reg.						
	0X01		An IN X'6C' indicated EB mode was not reset.	E4H2		PL102	H-140	Reg X'14' contains the results of the IN X'6C'.
	0X02		An IN X'6C' indicated the adr reg was not reset.	E4H2 E4J2		PL103 PK103	H-140 H-130	Reg X'14' contains the results of the IN X'6C'. A value other than 0 was in the transferred byte count. Reg X'15' indicates which of the adr reg bits were not 0. Reg X'14' contains the results of the IN X'6C'.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X935		EB mode adr reg sequencing. After disabling and resetting the CA4, EB mode is set and an OUT X'62' is issued to reset the EB mode adr reg and to initiate a service cycle. Sequential OUT X'6D' instructions are issued to step the EB mode adr reg. A diagnostic reset (OUT X'67') is issued to reset service cycle, EB mode is again set, and an IN X'6C' is issued to obtain the transferred byte count. The transferred byte count provides the value in the EB mode adr reg and is equal to twice the number of output X'6C' instructions issued plus 2. During the first pass, through this routine, one OUT X'6D' is executed. On each succeeding pass, the number of OUT X'6D' instructions is increased by 1 until on the 16th pass, 16 OUT X'6D' instructions are executed.						
	0X01		An IN X'6C' indicated either EB mode was reset or the transferred byte count was not 0.	E4H2 E4J2		PL102 PK103	H-140 H-130	If bit 0.0 of reg X'15' is on, EB mode was reset. If any other bits are on, the EB mode adr reg was not reset. Pretest error. Rerun routine X934.
	0X02		After a diagnostic reset to reset service cycle, EB mode could not be set.	E4H2		PL102	H140	Setting EB mode was previously tested in routine X932. Rerun routine X932.
	0X04		Transferred byte count obtained with X'6C' instruction indicated that EB adr reg did not step correctly.	E4H2		PL103	H-160	Reg X'14' contains the results of the IN X'6C'. Reg X'13' contains the expected value. This value is twice the number of OUT X'6D' instructions issued +2. (The adr reg wraps around at a value of 32 so if 16 X'6D' instructions were issued, a value of 2 will be expected.)
X936	0X01-0X10	EB mode local store all zero test. After disabling and resetting the CA4, EB mode is set and 16 OUT X'6D' instructions are executed, turning on all bits in the EB mode local store array. Then, X'6D's are executed to turn off all the bits.	A position of the array was found to be nonzero. The error code indicates (in hex) which halfword was found to be nonzero. For example, error code 0X01 indicates the first halfword (bytes 0 and 1), error code 0X02 indicates the second (bytes 2 and 3), etc., up to error code 0X10, which indicates the 16th halfword (bytes 30 and 31).	E4J2 E4G2		PK102 PM101	H-160 H-160	Reg X'14' contains the results of the IN X'6D' that obtained the halfword in error. All bits should be off. (Continuing from the error stop causes the remaining positions of the array to be verified.)
X938	0X01-0X10	EB mode local store interference test. After disabling and resetting the CA4, the EM mode local store array is set to 0. Then, 16 OUT X'6D' instructions are executed to set each halfword of the EM mode array to selected bit patterns. Following an IN X'6D' to prime the array in-buffer, 16 IN X'6D's are executed to verify that each halfword was properly set. The first pass through the routine attempts to set all bits in the array on. Next, each halfword is set to X'AAAA', X'5555', X'7A7A', X'8585', X'C3C3', X'3C3C', X'EFEF' and X'1010'. Each pattern is written in all array locations and read back for verification one pattern at a time.	An IN X'6D' instruction indicated that a halfword was set as expected. The error code indicates (in hex) which halfword failed. For example, 0X11 indicates the first halfword (bytes 0 and 1), 0X12 indicates the second (bytes 2 and 3), etc., up to 0X20 which indicates the 16th (bytes 30 and 31) halfword failed.	E4J2 E4G2		PK102 PM101	H-160 H-160	Reg X'14' contains the results of the IN X'6D', and reg X'15' indicates which bits were in error. Continuing from this error stop causes the remaining positions of the array to be checked and other data patterns to be used.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X939	0X01-0X10	EB mode local store variable data. After disabling and resetting the CA, the EB mode local store array is set to 0. Then, 16 OUT X'6D' instructions are executed to set each halfword of the EB mode array to a certain bit pattern. Following an IN X'6D' to prime the array in-buffer, 16 IN X'6D's are executed to verify that each halfword was properly set. The first pass through the routine sets the array to X'FFFE' and verifies this. A zero is then floated through the array until X'7FFF' is reached. Each pattern is written in all locations, read back, and verified. Next, growing ones patterns starting with X'0001' and ending with X'FFFF' are stored. Each pattern is written in all locations, read back, and verified.	An IN X'6D' instruction indicated that a halfword was not set as expected. The error code indicates (in hex) which halfword failed. For example, 0X11 indicates the first halfword (bytes 0 and 1), 0X12 indicates the second halfword (bytes 2 and 3), etc., up to 0X20, which indicates the 16th (bytes 30 and 31) halfword failed.	E4J2 E4G2		PK102 PM101	H-160 H-160	Reg X'14' contains the results of the IN X'6D', and reg X'15' indicates which bits were in error. Continuing from this error stop causes the remaining positions of the array to be checked and other data patterns to be used, remaining positions of the array to be checked, and other data patterns to be used.
X93A	0X01-0X10	EB mode addressing — reset with IN X'6C'. After disabling and resetting the CA4, the EB mode local store array is set to zeros and 16 consecutive OUT X'6D's executed. Each OUT X'6D' sets the number of the local store array byte into that byte of the EB mode local store array. Thus, bytes 0 and 1 of the array should contain X'00' and X'01', bytes 2 and 3 should contain X'02' and X'03', etc. After all the bytes are set, an IN X'6D' primes the array in-buffer and each halfword is read to determine that it is set to its respective number.	One of the bytes stored in the local store array was incorrect. The error code indicates (in hex) which halfword failed. For example, 0X11 indicates the first halfword (bytes 0 and 1), 0X12 indicates the second (bytes 2 and 3), etc., up to 0X20, which indicates the 16th (bytes 30 and 31) halfword failed.	E4J2		PK103 PK102	H-160	Reg X'11' contains the expected contents of the local store bytes, reg X'14' contains the results of the IN X'6D', and reg X'15' indicates the bits in error. (Continuing from this error stop causes the remaining local store bytes to be checked.)
X93C		EB mode addressing — reset with IN X'6C'. After disabling and resetting the CA4, the EB mode local store array is set to zeros and 'n' (see below) OUT X'6D' instructions are executed to store byte's number into the byte being set. An IN X'6C' is then executed to reset the EB mode adr reg and a X'FFFF' stored with OUT X'6D'. X'FFFF' should be stored into bytes 2 and 3 of the array, since an IN X'6C' was used to reset the adr reg. Sixteen passes are made through this routine, the first pass executes one OUT X'6D' instruction, the second pass executes two OUT X'6D' instructions, etc.						
	0X01		After storing X'FFFF' into bytes 2 and 3 of the EB mode local store array, an OUT X'62' is executed to reset the adr reg (the reset function was previously tested by routine X934) and an IN X'6D' reads the first halfword (bytes 0 and 1) of the array. This halfword should contain X'0001' but did not.	E4J2 E4H2		PK102 PL103	H-150 H-140	Reg X'14' contains the results of the IN X'6D'. The byte located at the adr in reg X'12' plus X'64' indicates the number of bytes stored in the array before the IN X'6C' reset was executed.
	0X02		If the first two bytes of the array were not changed, another X'6D' obtains the second halfword of the array, which should contain X'FFFF' stored following the IN X'6C' to reset the adr register. The data was incorrect.	E4J2 E4H2		PK102 PL103	H-150 H-140	Reg X'14' contains the actual results of the IN X'6D'. The byte located at the adr in reg X'12' plus X'64' indicates the number of bytes stored in the array before the IN X'6C' reset was issued.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X93D	0X01	EB mode adr reset and print with IN X'6C'. This routine verifies that an IN X'6C' instruction primes the EB mode local store array in-buffer with the first 2 bytes of the array. After disabling and resetting the CA4, the EB mode local store array is cleared and X'0001' is stored in bytes 0 and 1 of the array. An IN X'6C' is executed followed by an IN X'6D' to verify that the first 2 bytes have been fetched.	The IN X'6D' which was executed to verify that the first 2 bytes of the array have been fetched, contained other than the X'0001' stored in the first 2 bytes.	E4H2		PL102	H-130	Reg X'14' contains the results of the IN X'6D'.
X93E		EB mode adr reg reset with OUT X'62' and OUT X'6C'. This routine verifies that the EB mode adr reg is reset with an OUT X'62' or an OUT X'6C'. After disabling and resetting the CA4, the EB mode local store array is cleared and 'n' (see below), X'6D's executed, storing each bytes number into the byte being set. An OUT X'62' or X'6C' is then executed to reset the EB mode adr reg and a X'FFFF' is stored with an OUT X'6D' into the first 2 bytes of the array. Sixteen passes are made through this routine using an OUT X'62' to reset the adr reg and then 16 more using an OUT X'6C'. For each output instruction, the first pass does one OUT X'6D' instruction; the second pass does 2 OUT X'6D' instructions, etc.					
	0X24		Following an OUT X'62' to reset the adr reg and an OUT X'6D' to store X'FFFF', an IN X'6C' was executed to reset the adr reg and an IN X'6D' to read the first 2 bytes of the array. The bytes did not contain X'FFFF'.	E4H2		PL103	H-140	Reg X'14' contains the results of the IN X'6D'. The byte located at the adr in reg X'12' plus X'64' indicates the number of bytes stored before the OUT X'62' reset was executed.
	0XC4		After an OUT X'6C' instruction to reset the adr reg and an OUT X'6D' instruction to store X'FFFF', an IN X'6C' was executed to reset the adr reg and an IN X'6D' was executed to get the first 2 bytes of the array. They did not contain X'FFFF'.	E4H2		PL103	H-140	Reg X'14' contains the results of the IN X'6D'. The byte located at the adr in reg X'12' plus X'64' indicates the number of bytes stored before the OUT X'6C' reset was executed.
X940		Data/status irpts. After disabling and resetting the CA4, a test is made to ensure that each of the data/status L3 irpts can be forced. A separate pass through the routine is made for each type data/status transfer sequence. At any of the error stops within this routine, reg X'11' indicates the type of data/status irpt being tested. They are tested in the following order: Bit 0.4: NSC Final Status Indicator Bit 0.3: NSC Channel End Transfer Bit 0.2: ESC Final Status Transfer Bit 0.1: Inbound Data Transfer Bit 0.0: Outbound Data Transfer (If byte 1, bit 5 is on, a Priority Outbound Data Transfer)					

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X940 (cont.)	0X01		After an OUT X'62' has been issued to set the tested type of transfer sequence, an OUT X'67' with data of all zeros is issued to force the selected type of irpt. After unmasking L3 irpts, no irpt occurred. (The OUT X'67' should have caused the diagnostic hardware to force the selected type irpt.)	E4G2		PM103	H-230	Reg X'11' indicates the type of transfer sequence being tested.
	0X02		Following the forced L3 irpt, an IN X'62' indicated that the irpt received was not the data/status L3 irpt expected.	E4L2		PE103	H-070	Reg X'14' contains the results of the IN X'62'. Reg X'11' indicates the type of transfer sequence being tested.
X942		Data/status irpts reset. After forcing each of the data/status L3 irpts, a check is made to ensure that each can be reset with an OUT X'62'. A separate pass through the routine is made for each type data/status transfer sequence. At any of the error stops in this routine, reg X'11' indicates the type of data/status irpt being tested. They are tested in the following order: Bit 0.4: NSC final status transfer Bit 0.3: NSC channel end transfer Bit 0.2: ESC final status transfer Bit 0.1: Inbound data transfer Bit 0.0: Outbound data transfer (If byte 1, bit 5 is on, a priority outbound data transfer)					
	0X01		After issuing an OUT X'62' to set the tested type of transfer sequence, an OUT X'67' with data of all zeros is issued to force the selected type of irpt. After unmasking L3 irpts, no irpt occurred. (The OUT X'67' should have caused the diagnostic hardware to force selected type irpt.)	E4G2		PM103	H-230	Reg X'11' indicates the types of transfer sequence being tested. Pretest Error. Rerun routine X940.
	0X02		Following the forced L3 irpt, an IN X'62' indicated that the L3 irpt received was not the data/status L3 irpt expected.	E4L2		PE103	H-070	Reg X'14' contains the results of the IN X'62'. Reg X'11' indicates the type of transfer sequence being tested. Pretest Error. Rerun routine X940.
	0X03		After forcing the tested type, data/status L3 irpt, an OUT X'62' with byte 1, bit 6 on was issued to reset the data/status L3 irpt request. L3 irpts were then unmasked and a check made to ensure that no L3 irpt condition was still pending. A L3 irpt did occur.	E4G2		PM103	H-230	Reg X'14' contains the results of the IN X'77' issued when the irpt occurred. Continuing from this error stop will cause an IN X'62' to be issued and a check made to ensure none of the transfer sequence bits are still set. (See error code 0X04.) If error 0X04 does not occur after continuing from this stop, none of those bits were set. Reg X'11' indicates the type of transfer sequence being tested.
	0X04		After ensuring that no L3 irpt occurs after resetting the tested type transfer sequence, another check is made to ensure that none of the sequence bits remain on. An IN X'62' indicated that at least 1 bit remained on.	E4L2		PE103	H-070	Reg X'14' contains the results of the IN X'62'. Reg X'11' indicates the type of transfer sequence being tested.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X944		Force initial select irpt. This test ensures that an initial select L3 irpt can be forced with an OUT X'67'.						
	0X01		After issuing an OUT X'67' with bit 0.0 on, another OUT X'67' with no bits on was issued to force an initial select irpt. No L3 irpt occurred.	E4G2		PM103	H-120	
	0X02		Incorrect initial select irpt from the adapter under test was received.	E4G2 E4L2		PM103 PE102	H-120	Reg X'14' contains the results of the IN X'77' issued when the irpt was received. Reg X'15' indicates the bits in error: Bit 1.0: CA-4 L3 irpt bit not set Bit 1.3: Selected type 4 channel adapter data/status L3 set in error Bit 1.4: Selected type 4 channel adapter L3 initial select not set
X945		Reset forced initial select irpt. An initial select L3 irpt is forced and a check was made to ensure that it can be reset.						
	0X01		After issuing an OUT X'67' with bit 0.0 on, another OUT X'67' with no bits on is issued to force an initial select irpt. The irpt did not occur.	E4G2		PM103	H-120	Pretest Error. Rerun Routine X944.
	0X02		After the L3 irpt is received, a check is made to ensure that it was an initial select irpt from the adapter under test.	E4G2 E4L2		PM103 PE102	H-120	Reg X'14' contains the results of the IN X'77' issued when the irpt was received. Reg X'15' indicates the bits in error: Bit 1.0: CA-4 L3 irpt bit not set Bit 1.3: Selected type 4 channel adapter data/status L3 in error Bit 1.4: Selected type 4 channel adapter L3 initial select not set. Pretest Error. Rerun routine X944.
	0X03		After having forced an initial select L3 irpt, an OUT X'62' with bit 0.5 on is issued to reset the initial select irpt. After unmasking L3 irpts, another irpt occurred.	E4G2 E4L2		PM103 PE102	H-060 H-060	Reg X'14' contains the results of an IN X'77' issued when the irpt occurred: Bit 1.3: A data/status L3 irpt was present. Bit 1.4: An initial select irpt was still present.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X946		Dual type 4 CA immediate select CA4-1. This test ensures that with the second CA4 selected an OUT X'67' can be issued to the first CA4 without changing the CA4 selection. Program-requested irpt is used as the test vehicle. This routine will run only on machines with a second CA4 defined in the CDS. The overall operation of this routine is: 1. After selecting and disabling the first CA-4, ensures that program-requested irpt is off. 2. After selecting and disabling the second CA-4, ensures that program-requested irpt is off. 3. Causes a program-requested irpt on the first CA-4 and leaves the second one selected. 4. Allows irpts and ensures that an irpt occurs but that IN X'77' indicates the second CA4 is still selected and program-requested irpt has not been set. 5. Selects the first CA4 and verifies that program-requested irpt has been set.						
	0X01		Following an OUT X'67' with bit 0.5 on to select CA4-1, an IN X'67' indicated that CA4-1 was not selected.	E4F2		PA108	H-120	Reg X'14' contains the results of the IN X'67'. Pretest error. Rerun routine 1901.
	0X02		After selecting the first CA4, the first CA4 was disabled and a check made to ensure that no program-requested irpt was pending. However, an irpt was pending.	E4T2		PG102	H-070	Reg X'14' contains the results of the IN X'62' issued after the reset. Pretest error. Rerun routine 1903.
	0X03		Following an OUT X'67' with bits 0.5 and 0.7 on to select CA4-2, an IN X'67' indicated that CA-2 was not selected.	E4F2		PA108	H-120	Reg X'14' contains the results of the IN X'67'. Pretest error. Rerun routine X901.
	0X04		After having selected the second CA4, it was disabled and a check made to ensure that no programmed-requested irpt was pending. An irpt was pending.	E4T2		PG102	H-070	Reg X'14' contains the results of the IN X'62'. issued after the reset. Pretest error. Rerun routine X903.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X946 (cont.)	0X05		With CA4-2 selected, an OUT X'67' with bits 0.3 and 1.1 on was issued to set program-requested irpt on the first CA4 without changing CA4 selection. L3 irpts were unmasked and a check made to ensure that a L3 irpt did occur but that CA4-2 was still selected.	E4G2		PM102	H-230	If bit 0.0 of reg X'15' is on, no L3 irpt occurred. If bit 0.0 is off, a L3 irpt occurred and reg X'14' contains the results of an IN X'77' issued when the irpt occurred. Reg X'15' contains the bits in error: Bit 1.0: Although a L3 irpt occurred, IN X'77' did not indicate a CA4 L3 irpt. Bit 1.3: A data/status L3 irpt is indicated. With CA4-2 still selected and the irpt condition set on CA4-1, no data/status irpt should be indicated. Bit 1.4: An initial select irpt is indicated. Bit 1.6: CA4-2 is no longer selected.
	0X06		While CA4-2 is still selected, a check is made to ensure that an IN X'62' does not indicate a program-requested irpt. (The program-requested irpt should have been set on CA4-1.)	E4G2		PM102	H-230	Reg X'14' contains the results of the IN X'62'.
	0X07		Select CA4-1. An OUT X'67' with bit 0.5 on is issued to select CA4-1 again. An IN X'67' that followed indicated CA4-1 had not been selected.	E4G2		PM102	H-230	Reg X'14' contains the results of the IN X'67'. Though not a pretest error, this function has previously been tested. Try rerunning routine 1901.
	0X08			E4G2		PM102	H-230	After reselecting CA4-1, irpts are again unmasked and a check made to ensure that a data/status L3 irpt from CA4-1 now occurs. (The program-requested irpt previously set has not been reset and should still be pending.) If bit 0.0 or reg X'15 is on, no L3 irpt occurred. If bit 0.0 is off, an irpt did occur and reg X'14' contains the results of the IN X'77' issued following the irpt. Reg X'15' contains the error bits: Bit 0.0: No L3 irpt occurred. (Ignore remaining error bits.) Bit 1.0: IN X'77' did not indicate a CA4 L3 irpt. Bit 1.3: A data/status irpt is not indicated. Bit 1.4: An initial select irpt is indicated. Bit 1.6: CA4-2 is still selected.
	0X09		Following the data/status irpt from CA4-1, an IN X'62' did not indicate a program-requested irpt.	E4T2		PG102	H-070	Reg X'14' contains the results of the IN X'62'.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X949		Dual CA4 immediate select. This test ensures that when the first CA4 is selected, an OUT X'67' can be issued to the second CA4 without changing the CA4 selection. Program-requested irpt is used as the test vehicle. This routine is run only on machines with multiple CA4s and only if the second CA4 is defined in the CDS. The overall operation of this routine is: 1. After selecting and disabling the second CA4, it ensures that program-requested irpt is off. 2. After selecting and disabling the first CA4, it ensures that program-requested irpt is off. 3. It causes a program-requested irpt on the second CA4, leaving the first CA4 selected. 4. It allows irpts and ensures an irpt occurs but that IN X'77' indicates the first CA4 is still selected and program-requested irpt has not been set. 5. It selects the second CA4 and verifies that program-requested irpt has been set.					
	0X01		Following an OUT X'67' with bits 0.5 and 0.7 on to select CA4-2, an IN X'67' indicated that CA4-2 was not selected.	E4F2		PA108	H-120	Reg X'14' contains the results of the IN X'67'. Pretest error. Return routine X901.
	0X02		After selecting the second CA4, the second CA4 is disabled and a check made to ensure that program-requested irpt is pending. An irpt was pending.	E4T2		PG102	H-070	Reg X'14' contains the results of the IN X'62' issued after the disable. Pretest error. Rerun routine X903.
	0X03		Following an OUT X'67' with bit 0.5 on to select CA4-1 an IN X'67' indicated that CA4-1 was not selected.	E4F2		PA108	H-120	Reg X'14' contains the results of the IN X'67'. Pretest error. Rerun routine X901.
	0X04		After having selected the first CA4, the CA4 was disabled and a check made to ensure that no programmed requested irpt was pending. However, an irpt was pending.	E4T2		PG102	H-070	Reg C'14' contains the results of the IN X'62' issued after the reset. Pretest error. Rerun routine X903.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X949 (cont.)	0X05		With CA4-1 selected, an OUT X'67' with bits 0.3, 0.7 and 1.1 on was issued to set program-requested irpt on the second CA4 without changing the CA4 selection. L3 irpts were unmasked and a check made to ensure that a L3 irpt did occur but that CA4-1 was still selected.	E4G2		PM102	H-230	If bit 0.0 of reg X'15' is on, no L3 irpt occurred. If bit 0.0 is off, a L3 irpt occurred and reg X'14' contains the results of an IN X'77' issued when the irpt occurred. Reg X'15' contains the bits in error: Bit 0.0: No L3 irpt occurred. (Ignore remaining error bits.) Bit 1.0: Although a L3 irpt occurred, IN X'77' did not indicate a CA4 L3 irpt. Bit 1.3: A data/status L3 irpt is indicated. (With CA4-1 still selected and the irpt condition set on CA4-2, no data/status irpt should be indicated.) Bit 1.4: An initial select irpt is indicated. Bit 1.6: CA4-1 is no longer selected.
	0X06		While CA4-1 is still selected, a check is made to ensure that an IN X'62' does not indicate a program-requested irpt. (The program-requested irpt should have been set on CA4-2.)	E4G2		PM102	H-230	Reg X'14' contains the results of the IN X'62'.
	0X07		Select CA4-2. An OUT X'67' with bits 0.5 and 0.7 on is issued to select CA4-2 again. An IN X'67' that followed indicated CA4-2 had not been selected.	E4G2		PM102	H-230	Reg X'14'contains the results of the IN X'67'. Though not a pretest error, this function has previously been tested. Try rerunning routine X901.
	0X08		After reselecting CA4-2, irpts are unmasked and a check made to ensure that a data/status L3 irpt from CA4-2 now occurs. (The program-requested irpt previously set has not been reset and should still be pending.)	E4G2		PM102	H-230	If the irpt bit 0.0 of reg X'15' is on, no L3 irpt occurred. If bit 0.0 is off, an irpt did occur and reg X'14' contains the results of the IN X'77' issued following the irpt. Reg X'15' contains the error bits: Bit 0.0: No L3 irpt occurred. (Ignore remaining error bits.) Bit 1.0: IN X'77' did not indicate a CA4 L3. Bit 1.3: A data/status irpt is not indicated. Bit 1.4: An initial select irpt is indicated. Bit 1.6: CA4-1 is still selected.
	0X09		Following the data/status irpt from CA4-2, an IN X'62' did not indicate a program-requested irpt.	E4T2		PG102	H-070	Reg X'14' contains the results of the IN X'62'.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X94C and X94E		Dual CA4 priority selection test 1 and test 2. These routines verify that the automatic priority selection circuity selects the CA4 with the highest pending priority irpt. The routines make multiple passes; each pass forces one of nine possible irpt conditions (shown following) for a CA4 until all possible combinations of irpt conditions and CA4 sequence have been tested. Note that the only difference between the routines is the sequence in which the CA4s are selected. The tests performed and the resulting error codes, if any, are identical. If interrupts of the same priority are forced, the routine ensures that the nonselected CA4 is selected when the automatic selection takes place. These routines function as follows: Set up both CA4s for the first priority sequence (priority outbound) shown following. 1. Select and disable CA4-1. 2. Set a test irpt condition. 3. Select and disable CA4-2. 4. Set a test irpt condition. 5. Issue an OUT X'67' to allow auto CA4 selection. 6. Allow irpts and verify that an irpt occurs and that CA4 selection has occurred. 7. Determine which CA4 interrupted and verify that the type of irpt received was the type of irpt forced. 8. Reset the irpt condition. 9. Repeat steps 5 thru 8 for the second irpt. 10. If difference priority irpts were forced, verify that the CA4 with the highest pending-priority irpt, interrupts prior to the other CA4. 11. If equal priority irpts are forced, verify that the next logical CA4 interrupts when expected. 12. Advance CA4 sequence and return to step 1. On the first pass, the priority sequence is tested on both CA4s defined in the CDS. After each pass the first CA4 is advanced to the next sequence. When the first CA4 has been advanced and been tested on the last sequence, it is reset to the first sequence and the second CA4 is advanced. In this manner, both CA4s are advanced through the nine sequences. On each pass, E0xx is displayed in DISPLAY B; where xx is the pass count reset at X'FF'. If the panel request is 0900, this routine is run one time for each CA4 defined in the CDS.					

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X94C and X94E (cont.)								

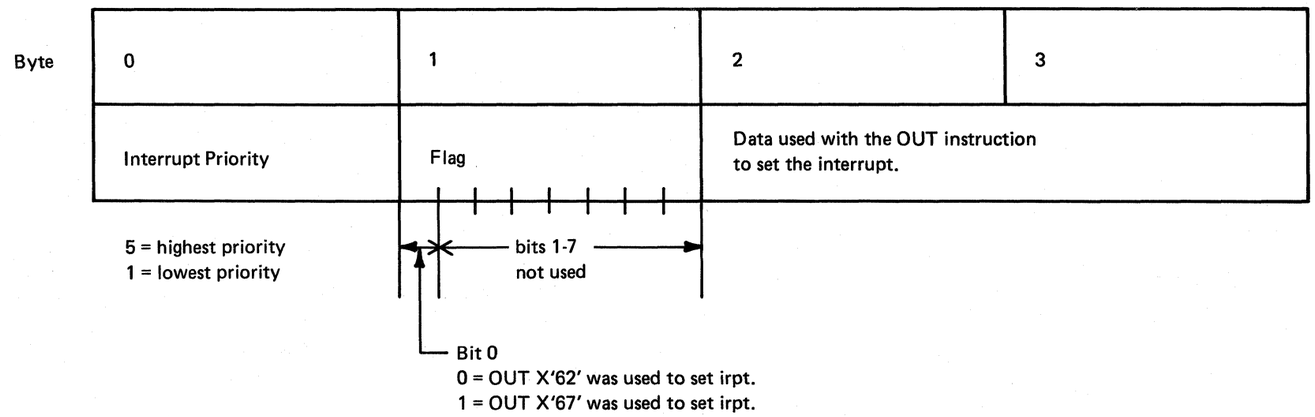
Irpt Priority Table

Type of Irpt Sequence	*Priority Byte 0*	*Flags Byte 1*	*Output Data Bytes 2-3*	*Expected Input Data Bytes 4-5*
Priority outbound sequence	X'05'	X'00'	X'8004'	X'8000'
Outbound data transfer sequence	X'04'	X'00'	X'8000'	X'8000'
Initial selection sequence	X'03'	X'E0'	X'8000'	X'0000'
Inbound data sequence	X'02'	X'00'	X'4000'	X'4000'
ESC status transfer sequence	X'01'	X'00'	X'2000'	X'2000'
NSC channel end status transfer sequence	X'01'	X'00'	X'1000'	X'1000'
NSC final status transfer sequence	X'01'	X'00'	X'0800'	X'0800'
Program requested irpt	X'01'	X'80'	X'0040'	X'0400'
Suppress out monitor irpt	X'01'	X'90'	X'0080'	X'0200'

Flag Byte Format

Bit	*Content*	*Definition*
0	0	OUT X'62' used to set condition
	1	OUT X'67' used to set condition
1	0	Check reg X'62'
	1	Do not check reg X'62'
2	0	Data/Status irpt expected
	1	Initial selection irpt expected
3	1	Last table entry
4-7		Not used.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X94C and X94E (cont.)		For routines X94C and X94E, reg X'12' contains the address of a save area in storage. The halfword at X'54' plus this address, is the address of a field describing the type of irpt forced on the first CA4. The halfword at X'56' plus this address, is the address of a field describing the type of irpt forced on the second CA4. The format is:						



Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X94C and X94E (cont.)	0X01		Following an OUT X'67' with bit 0.5 on to select CA4-1, an IN X'67' indicated that CA4-1 was not selected.	E4F2		PA108	H-120	Reg X'14' contains the results of the IN X'67'. Pretest error. Rerun routine X901.
	0X02		Following an OUT X'67' with bits 0.5 and 0.7 on to select CA4-2, an IN X'67' indicates that CA4-2 was not selected.	E4F2		PA108	H-120	Reg X'14' contains the results of the IN X'67'. Pretest error. Rerun routine X901.
	0X05 0X09		After setting a pending irpt condition on both CA4s, an OUT X'67' of all zeros was issued to cause auto-CA selection to occur. After unmasking level 3 irpts, no irpt occurred. (Refer to the routine description to determine what type irpt was forced on each CA.)	E4L2 E4G2		PE102 PM103	H-070 H-120	0X05 is for the first irpt expected. 0X09 is for the second irpt expected.
	0X06 0X10		Although an irpt occurred (see error code 0X05), neither bit 1.3 nor 1.4 was on in IN X'77'. This indicates that auto-selection has not taken place. (Refer to the routine description to determine the type irpt forced on each adapter.)	E4G2		PM103	H-230	0X06 is for the first irpt expected. 0X10 is for the second irpt expected.
	0X07 0X11 0X15		After verifying that the irpt received was the one expected, an OUT X'62' with bits 0.5 and 0.6 is executed to reset the irpt condition. An IN X'62' then indicated that a data/status transfer sequence was still set.	E4L2		PE108	H-070	Reg X'14' contains the results of the IN X'62'. Bits 0.4 through 0.7 should not have been on. The halfword located at X'5C' plus the adr in reg X'12' contains the results of the IN X'77' executed when the irpt was received. This can be used to determine which adapter is selected.
	0X08 0X12 0X16		After verifying that the OUT X'62' reset any data/status transfer sequence bits (see error codes 0X07, 0X11, or 0X15), an IN X'77' is executed to verify that the received irpt condition has been reset and that a type 4 channel adapter L3 irpt is still pending from the other CA.	E4G2		PM103	H-230	Reg X'14' contains the results of the IN X'77'. Either bit 1.3 or 1.4 was still on, indicating the present irpt condition has not been reset, or bit 1.0 is no longer on indicating no other type 4 channel adapter L3 irpt is pending. Refer to the routine description to determine the type irpt forced on each CA. Reg X'14' contains the results of the IN X'77'.
	0X09		See error code 0X05.					
	0X10		See error code 0X06.					
	0X11		See error code 0X07.					
	0X12		See error code 0X08.					
	0X15		See error code 0X07.					
	0X16		See error code 0X08.					
	0X19 0X21		The irpt occurring after auto-channel adapter selection was not the type of irpt expected.	E4L2 E4G2		PE103 PM103	H-070 H-120	Reg X'14' contains the results of the IN X'77' executed at the time of the irpt. Reg X'15' indicates the bits in error in reg X'14'.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X94C and X94E (cont.)	0X20 0X22 0X24 0X26		If the irpt expected in codes 0X19 and 0X21 was a data/status irpt, an IN X'62' verifies that the irpt was the expected type data/status irpt.	E4L2		PE103	H-070	Reg X'14' contains the results of the IN X'62'. Reg X'15' indicates the bits in error in reg X'14'. The halfword located at X'5C' plus the adr in reg X'12' contains the results of the IN X'77' executed when the irpt occurred. This can be used to determine the selected adapter.
X950		Cycle-steal reg X'6F' test. This routine ensures that bits 1.4, 1.5, 1.6, and 1.7 of reg X'6E' and all bits of reg X'6F' can be set to ones. The value of X'000F' is output to reg X'6E'. Reg X'6E' is read to verify that it contains X'000F'. The value of X'FFFF' is output to reg X'6F'. Reg X'6F' is read to verify that it contains X'FFFF'.						
	0X01		Error indication on input of cycle-steal reg X'6E'.	E4E2		PP103	H-180	Bits expected to be set are 1.4, 1.5, 1.6, and 1.7. Results of input should be in reg X'14'. Bits in error should be in reg X'15'.
	0X02		Error indication upon input of cycle-steal reg X'6F'.	E4D2		PP101	H-180	Results of the input are in Reg X'14'. All bits are expected to be set. Bits in error should be in reg X'15'.
X952		Cycle-steal adr and outbound data transfer test. This routine tests for the proper functioning of the cycle-steal adr regs, X'6E' and X'6F' and for the transfer of data from storage to the data buffer reg X'6D'. On successive passes, cycle-steal operation is executed in diagnostic mode. Starting with a 2-byte cycle steal, each cycle steal is incremented by 2 until 256 bytes are transferred in the last pass. On each pass, the cycle-steal operation is requested with an output to reg X'6C'; the data out adr is output to reg X'6E' and reg X'6F'. Outbound transfer is requested with OUT X'62' and the cycle-steal is initiated by outputs to reg X'67'. Output X'67' is executed on each pass, once for each byte in the count in reg X'6C'. The resulting cycle-steal adr in registers X'6E' and X'6F', when in cycle-steal mode, is 2 bytes higher than when in normal cycle-steal mode. With this in mind, the cycle steal adr is checked on each pass to be 2 bytes higher than normal, and the data in register 6D is compared with data that is 2 bytes beyond that data normally expected.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X952 (cont.)	0X01		Cycle-steal adr error.	E4E2 E4D2		PP103 PP101	H-180 H-180	Value obtained from reg X'6F' is in reg X'14'. Adr expected is in reg X'13'. Bits in error in reg X'15'.
	0X02		Cycle-steal data error.	E4J2		PK102	H-160	The value obtained from reg X'6D' is in reg X'14'. The value expected from reg X'6D' is in reg X'13'. The bits in error are in reg X'15'.
X954		Cycle-steal adr and inbound data transfer test. This routine tests for the proper functioning of the cycle-steal adr reg X'6E' and X'6F' and for the transfer of data from the buffer reg X'6D' to storage. On successive passes, cycle-steal operations are executed. The byte count of each cycle steal is incremented by 2, from 2 to 256 bytes. On each pass, the cycle steal operation is requested with an output to reg X'6C'; the data in adr is output to reg X'6F' and reg X'6E'. Inbound transfer is requested with IN X'62' and the cycle steal is initiated by outputs to reg X'67'. Reg output X'67' is executed the number of times equal to the cycle steal count. After each operation, the cycle-steal adr is verified to have incremented by the same value of the cycle-steal count, and the data in storage is verified to be that from the buffer reg X'6D'.						
	0X01		Cycle-steal adr error.	E4E2 E4D2		PP103 PP101	H-180 H-180	Value obtained from reg X'6F' is in reg X'14'. Adr expected is in reg X'13'. Bits in error are in reg X'15'.
	0X02		Cycle-steal data error.	E4J2		PK102	H-180	Value obtained from storage is in reg X'14'. Value expected in storage is in reg X'13'. The bits in error are in reg X'15'.
X956		Cycle-steal outbound odd-even count and adr test. This test verifies proper performance of the cycle-steal operation, whether count or storage adr is odd or even. This test makes four passes. The first is an outbound transfer of 3 bytes from an even adr. On the second pass, the adr is made odd. On the third pass, the count is made even, and on the fourth pass the adr is made even.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X956 (cont.)		On each pass, cycle-steal registers X'6E' and X'6F' are verified to be incremented as expected. The anticipated data from storage is verified to be in reg X'6D'.						
	0X01		The cycle-steal adr from reg X'6F' in error on a 3-byte transfer.	E4D2		PP104	H-170	Reg X'14' contains the data from reg X'6F'. Reg X'15' contains the bits of reg X'14' that are in error.
	0X02		The cycle-steal adr from reg X'6F' in error on a 4-byte transfer.	E4D2		PP104	H-170	Reg X'14' contains the data from reg X'6F'. Reg X'15' contains the bits of register X'14' that are in error.
	0X03		Data error on outbound 3-byte cycle-steal transfer.	E4D2		PP104	H-170	Data expected is in reg X'14'. Bits in error are in reg X'15'.
	0X04		Data error on outbound 4-byte cycle-steal transfer.	E4D2		PP104	H-170	Data expected is in reg X'14'. Bits in error are in reg X'15'.
X957		Cycle utilization counter (CUC) test. This test verifies proper incrementing of the CUC from cycle-steal cycles by the adapter under test. CUC value represents a combination of cycle-steal and instruction cycles. CUC operation of the CUC for I1, I2 and I3 cycles has been verified in the CUC diagnostic routines.						
	0X01		CUC value is not correct after cycle-steal operation.	1AB4-T2		CN001		Reg X'14' = actual CUC value Reg X'15' = bits in error Reg X'16' = expected CUC value

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X958, X959, X95A, X95B, and X95C	F001 (Manual inter-vention stop, see step 2 on this page.)							

Extended buffer mode (EBM) local store data interference tests.

The interference test routines perform additional testing on the EBM local storage buffer. You should run all the other CA4 test routines before running the interference test routines.

The interference test routines:

- Write various data patterns into the local storage buffer.
- Read the local storage buffer.
- Compare the read data with the expected data.

The information on this page is common to routines X958 through X95C. The information on the following page describes each routine specifically.

General Procedures for Running the EBM Interference Test Routines

When running the interference test routines, use the following procedure.

1. When requesting a routine, set the 'include manual intervention routine' CE sense switch. (Set X'10' in the STORAGE ADDRESS/REGISTER DATA switches D and E to cause the routine to cycle). (For detailed information on how to run an IFT, see "How to Request an IFT" in the IFT section.)

2. When the manual intervention stop occurs (DISPLAY B indicates X'F001'), adjust the -4 Vdc voltage to -3.6 volts. (Refer to page D-580 in Volume 3 of *IBM 3705-80 Communications Controller Theory Maintenance* SY27-0209.)

   If an error stop occurs before X'F001' is displayed, replace the CA4 card at E4J2 and rerun the interference test routines.

   Note: Do not select the 'loop on first error' CE sense switch setting. The interference test routines are not designed to loop on an error.

3. Set STORAGE ADDRESS/REGISTER DATA switches D and E to X'CC'.

4. Set DISPLAY/FUNCTION SELECT switch to FUNCTION 5.

5. Press the START pushbutton. The routine will start running.

6. After the routine has run several times (see approximate run times for each routine on the following page), set the STORAGE ADDRESS/REGISTER DATA switches D and E to a value other than X'CC'. (X'CC' causes the routine to bypass manual intervention stops. The routine will not stop until the current run is completed.)

7. Another X'F001' manual intervention stop will occur. Adjust the -4 Vdc voltage to -4.4 volts (see step 2).

8. Set STORAGE ADDRESS/REGISTER DATA switches D and E to X'CC'.

9. Set DISPLAY/FUNCTION SELECT switch to FUNCTION 5.

10. Press the START pushbutton. The routine will start running.

11. After the routine has run several times (see approximate run times for each routine on the following page) set the STORAGE ADDRESS/REGISTER DATA switches D and E to a value other than X'CC'. (X'CC' causes the routine to bypass manual intervention stops. The routine will not stop until the current run is completed.)

12. Adjust the -4 Vdc to -4.0 (see step 2).

13. Repeat these steps for the next interference test routine or return the 3705-80 to the customer.

    To end the current routine, set the DISPLAY/FUNCTION SELECT switch to FUNCTION 6, and set STORAGE ADDRESS/REGISTER DATA switches B-E to X'FFFF'. If the machine is running, press the INTERRUPT push button. If the machine is stopped, press the START push button.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X958	0X58	EBM local storage buffer interference test 1. Routine X958: (1) Writes into 1 position of the EBM local storage buffer, (2) reads the local storage buffer, and (3) compares the data read to the expected data. Routine X958 runs approximately 1/2 second.	Data read did not agree with expected data.	E4J2		PK102	H-130 through H-160	Reg X'14' contains the read data (obtained with IN X'6D' instruction). Reg X'15' indicates the bits in error. Reg X'16' contains the expected data.
X959	0X59	EBM local storage buffer interference test 2. Routine 959: (1) Writes into 15 positions of the IBM local storage buffer, (2) reads the local storage buffer, and (3) compares the data read to the expected data. Routine X959 runs approximately 1.5 minutes.	Data read did not agree with expected data.	E4J2		PK102	H-130 through H-160	Reg X'14' contains the read data (obtained with IN X'6D' instruction). Reg X'15' indicates the bits in error. Reg X'16' contains the expected data.
X95A	0X5A	EBM local storage buffer interference test 3. Routine X95A: Writes X'0000' through X'FFFC' into consecutive positions of the EBM local storage buffer. Positions 1 of the local storage buffer is written into and the remaining positions are read and compared to the expected data. The position written into is advanced on each pass of the routine. Routine X95A runs approximately 5 minutes.	Data read did not agree with expected data.	E4J2		PK102	H-130 through H-160	Reg X'14' contains the read data (obtained with IN X'6D' instruction). Reg X'15' indicates the bits in error. Reg X'16' contains the expected data.
X95B	0X01	EBM local storage buffer interference test 4 (Ping Pong test 1). Routine X95B: Writes various data patterns into various positions of the EBM local storage buffer. Routine X95B runs approximately 1/2 second.	An unexpected L1 irpt occurred.	U4J2		PK102	H-130 through H-160	
	0X5B		Data read did not agree with expected data.	U4J2		PK102	H-130 through H-160	Reg X'14' contains the read data (obtained with IN X'6D' instruction). Reg X'15' indicates the bits in error. Reg X'16' contains the expected data.
X95C	0X01	EBM local storage buffer interference test 5 (Ping Pong test 2). Routine X95C: Writes various data patterns into various positions of the EBM local storage buffer. Routine X95C runs approximately 1/2 second.	An unexpected L1 irpt occurred.	E4J2		PK102	H-130 through H-160	
	0X5C		Data read did not agree with expected data.	E4J2		PK102	H-130 through H-160	Reg X'14' contains the read data (obtained with IN X'6D' instruction). Reg X'15' indicates the bits in error. Reg X'16' contains the expected data.

3705-80 TYPE 4 CA IFT COMMON ERROR STOPS

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X9XX	1X01	Disable CA1.	CA1 was not disabled.	E4P2		PB103	H-120	Rerun routine X902.
	1X02	Select CA4.	CA4 was not selected.	E4F2		PA108	H-120	Reg X'14' contains results of an IN X'67'. Rerun routine X901.
	1X03	Select CA4.	CA4 was not selected.	E4F2		PA108	H-120	Reg X'14' contains results of an IN X'77'. Rerun routine X901.
	1X0A	Set regs to X'0000'.	Unable to set regs to X'0000'.					Rerun routines X904 through X925.
	1X0B	Set regs to X'FFFF'.	Unable to set regs to X'FFFF'.					Rerun routines X904 through X925.
	1X10	Set various bit patterns in regs.	Unable to set bit patterns in regs.					Rerun routines X904 through X925.
	1X11	Set EB mode with OUT X'6C' instruction (Bit 0.0 = 1)	Unable to set EB mode.	E4H2		PL102	H-140	Reg X'14' contains results of an IN X'6C'. Rerun routine X932.
	1X21 1X30	Set all positions of EB local storage array to 0.	Unable to set one or more positions to 0.	E4J2 E4G2		PK102 PK101	H-160 H-160	Reg X'14' contains the results of IN X'6D'. The error code indicates the failing halfword (1X21 is first halfword). Rerun routine X936.
	2X00		Received unexpected L1 irpt with no request bits on.	E4K2		PF107	H-110	
	2X01		Received unexpected L3 irpt.	E4L2		PM103	H-230	Bit 1.4 in reg X'77' was on.
	2X02		Unable to reset L3 irpt.	E4L2		PE102	H-060	
	2X03		Received unexpected L3 irpt.	E4L2		PE103	H-070	Bit 1.3 in reg X'77' was on. Neither 'suppress out monitor' nor 'program request irpt' were on in reg X'77'. Reg X'62' indicates the cause of the irpt.
	2X04		Unable to reset L3 data/status irpt.	E4L2			H-060	
	2X05		Unexpected 'suppress out monitor' L3 irpt.	E4T2		PG102	H-070	Bit 0.6 in reg X'77' is on.
	2X06		Unable to reset 'suppress out monitor' L3 irpt.	E4T2		PG102	H-070	
	2X07		Unexpected 'program request' L3 irpt.	E4T2		PG102	H-070	
	2X08			E4T2		PG102	H-070	
	2X09		Unexpected L3 irpt from CA1.	E4L2 E4T2			H-060	No request bits were on in reg X'62'.
	2X0A		Unknown L3 irpt occurred.					Neither IN X'77' nor IN X'7F' indicated the source of the irpt.
	2X1X		Unexpected L1 irpt occurred.	E4K2		PF101	H-100	Bit 1.3, 'local store check' was on in reg X'67'.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X9XX (cont.)	2X2X		Unexpected L1 irpt occurred.	E4K2		PF101	H-100	Bit 1.2, 'CCU outbus check' was on in reg X'67'.
	2X4X		Unexpected L1 irpt occurred.	E4K2		PF101	H-100	Bit 1.1 'I/O instruction accept check' was on in reg X'67'.
	2X8X		Unexpected L1 irpt occurred.	E4K2		PF101	H-100	Bit 1.0 'bus-in check' was on in reg X'67'.
	2XFF		Unable to reset L1 irpt.	E4K2		PF101	H-100	
				E4H2		PL105	H-140	Bit 0.4 Syn monitor control lt.
				E4H2		PL101	H-140	Bit 0.5 DLE remember lt.
				E4H2		PL101	H-140	Bit 0.6 ASCII monitor control lt.
				E4H2		PL101	H-140	Bit 0.7 EBCDIC monitor control lt.

3705-80 CSB IFT SYMPTOM INDEX

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X602	XXXX	CDS (configuration data set) checking rtn. This rtn checks that certain necessary control data within the CDS is valid. You should refer to the CDS section in this manual for a complete CDS definition. The CDS is loaded into storage starting at X'0F00' when the DCM (diagnostic control module) is loaded. Within the CDS is a control block for the type 2 communication scanner. This control block defines the scanner type, scanner RPQs, scanner features, oscillator types, LIB types, and line set types. Some of this data is validated in this rtn. If you get errors in this rtn and the configuration data is correct, it could be that the version/level of the diagnostics that you are running does not support that feature. While this rtn is running, you may get some DISPLAY B error codes starting with 1. These are pretest errors, which cannot be bypassed except by aborting this rtn. These pretest errors are defined in "Common Error Stops" following this CSB symptom index. See "Common Error Stops" for details on these pretest error codes if they occur. A summary of the error codes is listed here: *DISPLAY B* *Meaning* 1X01 Scanner is not configured as a type 2 scanner. 1X06 An invalid LIB type code found in CDS. 1X07 An invalid line set type code found in CDS.						
	0X01	Configuration data set (CDS)	Scanner not configured as a type 2 communication scanner. Reg X'16' = storage adr of data block within the CDS for the adapter (scanner number) under test.					Reg X'11' = line adr of scanner LIB line intf adr.
	0X02	Configuration data set (CDS)	Oscillator 0 not installed according to CDS data. Reg X'16' = storage adr of data block within the CDS for the adapter (scanner number) under test. Reg X'11' = line adr as used to set ABAR.					This error will also occur if an invalid oscillator type code was found in the CDS for oscillator 0 (1st oscillator position).
	0X03	Configuration data set (CDS)	Oscillator 0 not lowest speed according to CDS data. Reg X'16' = storage adr of data block within the CDS for the adapter (scanner number) under test. Reg X'11' = line adr as used to set ABAR.					This error will also occur if an invalid oscillator code is in the CDS for oscillators 1, 2, or 3 (2nd, 3rd, or 4th oscillator positions).
	0X04	Configuration data set (CDS)	No LIBs configured according to CDS data. Reg X'16' = storage adr of data block within the CDS for the adapter under test. Reg X'11' = line adr.					
	0X05	Configuration data set (CDS)	No line sets installed according to CDS data. Reg X'16' = storage adr of data block within the CDS for the adapter (scanner number) under test.					Reg X'11' = line adr of scanner-LIB-line intf adr.
X603	0X01	Test all valid inputs and outputs for type 2 scanner.	Input or output caused I/O check. Display reg X'14' has been loaded with the actual failing input/output instruction. Reg X'16' contains storage adr of instruction loaded into reg X'14'. Reg X'11' = line adr.	A3D2 B3E2		TA921 CK001	B-120 B-210	
	0X02	Test all valid inputs and outputs for type 2 scanner.	Adapter L1 irpt occurred. Reg X'14' contains error bits stored in L1 rtn from reg X'43'. Reg X'16' has adr of input/output instruction. Reg X'11' = line adr.	A3C2		TB131	9-500 8-460	L1 inputs are to the card at location A3C2.
X605	0X01	Attachment buffer adr reg. ABAR is reg X'40'	Unable to write or read valid adr to or from ABAR. Display reg X'14' for failing adr input from ABAR. Reg X'11' is adr that was output to ABAR.	B3E2 B3D2		CX001 CX009	B-030	All valid adr are written to and read from the ABAR with output and input X'40'.
X607	0X01	'CSB disable' on – turned on by output X'43' with byte 0 bit 0 and byte 1 bit 6 on. Should clear PCF and display request bits in ICW.	'CSB disable' failed to force primary control field (PCF) to 0. Reg X'11' = failing line adr.	A3F2		TA811	B-170	Check that 'CSB disable' holds the PCF to 0 and resets ICW bit 38, Reg X'47' byte 0 bit 6. Also checks that output X'43' with byte 0 bit 1 and byte 1 bit 5 clears reg X'43'.
	0X02	'CSB disable' on – turned on by output X'43' with byte 0 bit 0 and byte 1 bit 6 on. Should clear PCF and display request bits in ICW.	'CSB disable' failed to force PCF to 0 when output X'45' is done to set PCF = 7.	A3F2		TA811	B-190	Reg X'11' = line adr set in ABAR.

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X607	0X03	'CSB disable' on – turned on by output X'43' with byte 0 bit 0 and byte 1 bit 6 on. Should clear PCF and display request bits in ICW.	Error reg bits remain on in reg X'43'. Display reg X'15' for error bits.	A3C2		TB131	B-130	Reg X'11' = line adr set in ABAR.
	0X04	'CSB disable' on – turned on by output X'43' with byte 0 bit 0 and byte 1 bit 6 on. Should clear PCF and display request bits in ICW.	'CSB disable' did not reset display request ICW bit 38. Reg X'11' = line adr.	A3G2		TB061	B-140	ICW bit 38 (display bit) is input reg X'47' byte 0 bit 6.
X60A	XXXX	ICW adr test. This test checks for interaction between ICWs by storing a different pattern in the SDF of each ICW that is used. It then checks each ICW to ensure that it contains the correct pattern in its SDF. The pattern used in the SDF of each ICW is byte 0 bits 6-7 and byte 1 bits 0-7 of the line adr (as used to set ABAR) of that ICW. If the SDF portion of the ICW local storage is bad, you should use rtn X61D to help locate the problem.						
	0X01	Check that all ICWs (intf control words) can be adr by the pgm.	Incorrect bits in serial data field. Reg X'16' contains expected SDF. Reg X'14' byte 0 bits 6-7 = actual SDF bits 0 and 1 (ICW bits 24 and 25); byte 0 bits 0-7 = actual SDF bits 2-9 (ICW bits 26-33). Reg X'11' = line adr with invalid SDF.	A3L2 A3J2 A3H2		TA621 TA545 TA221	B-190	Each ICW is adr, and a different bit pattern is stored in the SDF bits of each ICW. Then each ICW is adr, and the SDF is checked to ensure that the correct bits are on for that ICW. **Note:** The pgm does output X'46' to set up the SDFs of all ICWs; then the rtn sets scope sync 2 before checking each ICW with input X'45' and X'47'.
X60C	0X01	'CSB disable' off (scanner enabled)	Primary control field (PCF) did not remain at 0. Reg X'11' contains line adr, which should be in ABAR. ABAR is reg X'40'.	A3F2		TA811	B-170	'CSB disable' latch is turned off, and the PCF is checked to see if it is 0.
	0X02	'CSB disable' off (scanner enabled)	PCF did not set or remain at state 7 with scanner enabled. Reg X'45' has PCF; reg X'11' has line adr.	A3F2		TA811	B-190	The 'CSB disable' bit being off allows the PCF to be changed to 7. The display bit (ICW bit 38) should still be off.
	0X03	'CSB disable' off (scanner enabled)	Bits are on in the error reg after 'CSB disable' turned off. See reg X'43'. Reg X'11' has line adr.	A3C2		TB131	B-130	No error bits are caused or expected.
	0X04	'CSB disable' off (scanner enabled)	Display bit on after 'CSB disable' off. Reg X'47' byte 0 bit 6 should not be on. Reg X'11' = line adr.	A3G2		TB061	B-140	
X610	0X01	Unexpected L1 irpt–test 1	Unexpected L1 irpt occurred. Reg X'16' = scanner check reg (saved from reg X'43' in the L1 irpt handler). Reg X'14' contains adr input from ABAR when the L1 occurred. Reg X'11' = line adr. Reg X'43' should be all 0's at this time unless another L1 error condition has occurred.	A3C2		TB131	B-130	Scanner is reset by an output to set 'CSB disable' latch. The pgm waits for any unexpected L1 irpt.
X611	0X01	Unexpected L1 irpt–test 2	Unexpected L1 irpt occurred. Reg X'16' = scanner check reg X'43' (saved by the L1 irpt handler). Reg X'14' = line adr obtained from ABAR when the L1 occurred. **Note:** Reg X'43' should be all 0's at this time unless another L1 error condition has occurred.	A3C2		TB131	B-130	Reset scanners by setting 'CSB disable' latch on. Enable scanner by turning the latch off. Pgm waits for unexpected L1 or L2 irpt.
X613	0X01	Unexpected L2 irpt–test 1	Unexpected L1 irpt. Reg X'16' = scanner check reg X'43' (saved by the L1 irpt handler). Reg X'14' = adr obtained from ABAR when the L1 occurred. **Note:** Reg X'43' should be all 0's at this time unless another error occurred.	A3C2		TB131	B-130	When 'CSB disable' is on, pgm checks for unexpected level 1 and L2 irpt.

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X613	0X02	Unexpected L2 irpt—test 1	Unexpected L1 and L2 irpt. Reg same as error X613 0X01.	A3C2 A3L2		TB131 TA611	B-130	See X613 0X01 comments.
	0X03	Unexpected L2 irpt—test 1	Unexpected L2 irpt. Reg X'14' contains adr obtained from ABAR by an input X'40' when the L2 occurred.	A3L2		TA611	B-300	See X613 0X01 comments.
X614	0X01	Unexpected L2 irpt—test 2	Unexpected L1 irpt. Reg X'16' = scanner check reg (saved from reg X'43' in the L1 irpt handler). Reg X'14' = ABAR (obtained by input X'40' when the L1 occurred). Reg X'43' was reset when the L1 occurred and should now be all 0's unless another L1 error is pending.	A3C2		TB131	B-130	After 'CSB disable' is reset, the pgm checks for unexpected L1 and L2 irpt. No action is initiated in the scanner after it is enabled, and no L1 or L2 irpt should occur.
	0X02	Unexpected L2 irpt—test 2	Unexpected L1 and L2 irpt. Reg Same as error X614 0X01.	A3C2 A3L2		TA131 TA611	B-130	See X614 0X01 comments.
	0X03	Unexpected L2 irpt—test 2	Unexpected L2 irpt. Reg X'14' = ABAR when unexpected L2 occurred.	A3L2		TA611	B-300	See X614 0X01 comments.
X616	0X01	Disable line intf base (LIB)	Primary control field (PCF) not set to 0 on disable. Reg X'11' = line adr.	A3F2		TA811	B-170	Each LIB is disabled and checked to see that PCF is forced to remain at 0. The LIB is disabled if its mask bit is set on by an output X'43'. **Note:** Only LIBs indicated as being installed by the CDS are tested.
	0X02	Disable line intf base (LIB)	Disable LIB did not force PCF to 0. Reg X'11' = line adr. An output X'45' was done to set PCF to 7. The PCF should have been forced to 0 since the LIB is disabled.	A3F2		TA811	B-170	See X616 0X01 comments.
X617	0X01	Enable line intf base (LIB)	Primary control field (PCF) not 0 after the LIB is enabled. Reg X'11' = line adr.	A3F2		TA811	B-170	The pgm disabled each LIB.
	0X02	Enable line intf base (LIB)	Could not set PCF after enabling LIB. Reg X'11' = line adr. Output X'45' was done to set LCD = 0 and PCF = 7. PCF should remain at 7.	A3F2		TA811	B-170	See X617 0X01 comments.
X61B	0X01	Intf control word bits 6-15 test	ICW bits 6-15 not set to X'2AA'. Reg X'11' = line adr.	A3P2 A3M2		TA131 TA741	B-180	Pgm sets ICW bits 6-15 to X'000', sets scope sync 2, sets ICW bits 6-15 to X'2AA', and checks that they = X'2AA'.
	0X02	Intf control word bits 6-15 test	ICW bits 6-15 not set to X'155'. Reg X'11' = line adr.	A3P2 A3M2		TA131 TA741	B-180	Pgm sets ICW bits 6-15 to X'000', sets scope sync 2, sets ICW bits 6-15 to X'155', and checks that they = X'155'.
	0X03	Intf control word bits 6-15 test	ICW bits 6-15 not set to X'3FF'. Reg X'11' = line adr.	A3P2 A3M2		TA131 TA741	B-180	Pgm sets ICW bits 6-15 to X'000', sets scope sync 2, sets ICW bits 6-15 to X'3FF', and checks that they = X'3FF'.
	0X04	Intf control word bits 6-15 test	ICW bits 6-15 not set to X'000'. Reg X'11' = line adr.	A3P2 A3M2		TA131 TA741	B-180	Pgm sets ICW bits 6-15 to X'3FF', sets scope sync 2, sets ICW bits 6-15 to X'000', and checks that they = X'000'.

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X61C	0X01	Intf control word bits 16-19 (LCD check)	ICW bits 16-19 not set to X'A'. Reg X'11' = line adr.	A3P2		TA111	B-190	Bit patterns X'A', '5', 'F', and '0' are set in and read from ICW bits 16-19 (LCD) in this test. ICW bits 20-23 (PCF) are not tested and are always set to 0's in this test to prevent any scanner hardware action that may occur if these bits are not 0. For this error stop (0X01), the pgm sets LCD to 0, sets scope sync 2, sets LCD to A, and checks that LCD = 'A'.
	0X02	Intf control word bits 16-19 (LCD check)	ICW bits 16-19 not set to X'5'. Reg X'11' = line adr.	A3P2		TA111	B-190	Pgm sets LCD = 0, sets scope sync 2, sets LCD to 5, and checks that LCD = X'5'.
	0X03	Intf control word bits 16-19 (LCD check)	ICW bits 16-19 not set to X'F'. Reg X'11' = line adr.	A3P2		TA111	B-190	Pgm sets LCD = 0, sets scope sync 2, sets LCD = F, and checks that LCD = X'F'.
	0X04	Intf control word bits 16-19 (LCD check)	ICW bits 16-19 not set to X'0'. Reg X'11' = line adr.	A3P2		TA111	B-190	Pgm sets LCD to F, sets scope sync 2, sets LCD to 0, and checks that LCD = X'0'.
X61D	0X01	Intf control word bits 24-33; out = reg X'46'; in = reg X'45' and X'47' (serial data field).	ICW bits 24-33 not set to X'2AA'. Reg X'11' = line adr.	A3H2		TA221	B-200	Pgm sets SDF to X'000', sets scope sync 2, sets SDF to X'2AA', and checks that SDF = X'2AA'.
	0X02	Intf control word bits 24-33; out = reg X'46'; in = reg X'45' and X'47' (serial data field).	ICW bits 24-33 not set to X'155'. Reg X'11' = line adr.	A3H2		TA221	B-220	Pgm sets SDF to X'000', sets scope sync 2, sets SDF to X'155', and checks that SDF = X'155'.
	0X03	Intf control word bits 24-33; out = reg X'46'; in = reg X'45' and X'47' (serial data field).	ICW bits 24-33 not set to X'3FF'. Reg X'11' = line adr.	A3H2		TA221	B-200	Pgm sets SDF to X'000', sets scope sync 2, sets SDF to X'3FF', and checks that SDF = X'3FF'.
	0X04	Intf control word bits 24-33; out = reg X'46'; in = reg X'45' and X'47' (serial data field).	ICW bits 24-33 not set to X'000'. Reg X'11' = line adr.	A3H2		TA221	B-200	Pgm sets SDF to X'3FF', sets scope sync 2, sets SDF to X'000', and checks that SDF = X'000'.
X61E	0X01	Display request bit (ICW bit 38); out = reg X'43'; in = reg X'47'	ICW bit 38 not turned on. Reg X'11' = line adr.	A3G2		TB061	B-170 B-140	Set ICW bit 38 on and reset it by an output X'43'. Bit is tested by an input from reg X'47'.
	0X02	Display request bit (ICW bit 38); out = reg X'43'; in = reg X'47'	ICW bit 38 not reset. Reg X'11' = line adr.	A3G2		TB061	B-170	See X61E 0X01 comments.
X61F	0X01	'CSB disable' resets display request bit (ICW bit 38)	ICW bit 38 not turnned on when scanner and LIB are enabled. Reg X'11' = line adr under test.	A3G2		TB061	B-170	Pgm attempts to set ICW bit 38 and 'CSB disable' to turn it off. Bit is set by output reg X'43' and tested by input reg X'47'.
	0X02	'CSB disable' resets display request bit (ICW bit 38)	'CSB disable' did not reset ICW bit 38. Reg X'11' = line adr.	A3G2		TB061	B-170	
X625	0X01	Primary control field (PCF) (NOP test) reg X'45'	PCF not set to X'0'. Reg X'11' = line adr. Reg X'40' should be same as reg X'11'.	A3F2		TA811		The pgm sets the PCF = 0 and expects no scanner action and no irpt during a 25-ms period for each line adr. The scanner and LIBs are enabled during this test.
	0X02	Primary control field (NOP test) reg X'45'	PCF did not remain at X'0' during a 25-ms wait.	A3F2		TA811		See X625 0X01 comments.
	0X03	Primary control field (NOP test) reg X'45'	L2 irpt occurred with line set to NOP. Reg X'14' = ABAR (obtained by input X'40' when the unexpected L2 occurred). Reg X'40' should = reg X'14'. Reg X'11' is last line adr set in ABAR (output X'40') just prior to output X'45' to set LCD and PCF = 0. No L2 irpt are expected in this rtn.	A3L2		TA611	B-310	See X625 0X01 comments.
X626	0X01	Upper scan limit X'00'.	Did not get L2 irpt from line when ICW 41 was set on. Reg X'11' = line adr. Reg X'40' should = reg X'11'.	A3L2		TA621	B-300	Set ICW bit 41 on.

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X626	0X02	Upper scan limit X'00'.	L2 from wrong line adr. Reg X'11' = expected line adr. Reg X'14' = line adr that caused the L2.	A3L2		TA611	B-300	Adr in each scanner is checked.
X627	XXXX	Set mode and scanner test. This is the first rtn in the type 2 scanner internal functional tests that requires that the line sets and some LIB circuits be operational. There are many possibilities for errors being detected in this rtn, but the most likely source of problems is in the line sets rcv strobe circuits or in the bit clock control card circuits in the LIB. See note 7 at the end of this CSB symptom index for some aid in determining if failures are in only one line set, in the LIB, or in the scanner.						
	0X01	Set mode and scanner test	L2 irpt did not occur for set mode. Display reg X'45'. If byte 0 bits 0-3 (LCD) are on, a feedback check occurred. Check oscillator 0 in the scanner. Check for bit svc or a missing line set card for the failing adr. The most likely source of failure is in the line set card(s) for the failing line adr. Reg X'11' = line adr under test. Reg X'40' should = reg X'11'. If no feedback check (LCD = F) occurred, the LCD should be 7 if the line runs in start/stop mode; the LCD should be 'C' if the line runs in BSC mode. If PCF = 1, the set mode never completed for start/stop or BSC lines. If PCF = 0, the set mode completed normally, but the L2 irpt expected did not occur within 25-ms after it was issued. Reg X'77' byte 0 bit 1 will be on if a L2 pending occurred after the 25-ms. The SDF contains the bits used for set mode. The card called is only a starting point to look for bit svc.	A3E2		TA331	B-310	All S/S and B-260 BSC line sets (some RPQ line sets) are tested by a set-mode operation, which checks some of the scanner, oscillator, LIB, line set circuits. A likely source of error is the line set card in the failing line adr. Display bit is set while line adr is under test so that the display reg (reg X'46') is valid for line adr under test. The PCF is checked for 0 after a set mode. A set mode may cause a L2 irpt even if the oscillator is not working properly. See note 7 at the end of this CSB symptom index for aid in isolating the problem.
	0X02	Set mode and scanner test	L2 irpt from wrong adr. Check the line that caused the irpt for faults. Reg X'11' = line adr under test. Reg X'40' should = reg X'11'. Reg X'14' has line adr obtained from ABAR by input X'40' when the L2 occurred.	A3L2		TA621	B-310 B-260	See X627 0X01 for details.
	0X03	Set mode and scanner test	PCF field did not set to 0 on set mode. Reg X'11' and X'14' set up same as X627 0X01 and X627 0X02.	A3F2		TA811	B-310 B-260	See X627 0X01 for details.
X628	XXXX	Feedback check test. All installed line line sets are tested to ensure that a feedback check will occur if an invalid bit is used during set mode and that a feedback check does *not* occur if a valid bit is used during a set mode. This rtn will most likely produce error stops if the CDS (configuration data set) defining the LIB and line set types is not set up properly for the hardware that is installed. If the CDS is correct, the most likely source of the error is in the line set card(s) for the failing line adr. See note 7 at the end of this CSB symptom index for an aid to problem determination. Each installed line set is tested in the following steps: a. Reset and then enable the scanner. b. Set the display bit on in the line adr under test. c. Set the SDF by an output X'46' with the bits in reg X'13'. d. Set scope sync 2. e. Set LCD = 0 and PCF = 1 to initiate the set-mode operation. f. Unmask L2 irpt and wait until either a L2 occurs or 25-ms have elapsed. g. Verify that the LCD was set to F by the scanner if a feedback check occurred due to an invalid bit being used in the SDF during the set mode, or verify that LCD was not set to F if a valid bit was used during the set mode. h. Repeat steps a through g until all set-mode bit positions have been tested.						

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X628	XXXX	On all error stops in this rtn, the following regs are set up: Reg X'11' = line adr of line under test (as used to set ABAR). Reg X'13' = bit pattern being output to the SDF for this step of the test. The bit position that is a 1 is the bit being tested. Each bit of byte 1 is defined in more detail as: *Bit* *ICW bit* *SDF bit* *Normal use if this bit is a 1 during set mode* 0 26 2 Not used. 1 27 3 Set diagnostic wrap mode. 2 28 4 Set data terminal ready. 3 29 5 Set sync bit clock (syn clock correction). 4 30 6 Set external clock selected. 5 31 7 Set data rate select (select high rate). 6 32 8 Set oscillator select bit 1. 7 33 9 Set oscillator select bit 2.						
	0X01	Check that an invalid bit in the SDF during a set mode operation causes a feedback check.	Error if a feedback check did not occur setting the LCD to F. See reg X'13' bit definitions in X628 XXXX for more information.	A3E2		TA341	B-260	A feedback check should have occurred since CDS indicates a line set is installed without a latch for the bit position under test in the SDF.
	0X02	Check that a valid bit in the SDF during a set mode operation does not cause a feedback check.	Error if a feedback check occurred setting LCD to F. See reg X'13' bit definitions in X628 XXXX for failing bit.	A3E2		TA341	B-260	A feedback check should not occur since CDS indicates a line set is installed with a latch that could be set on for this SDF bit position during a set mode operation.
X629	XXXX	Diag mode test. Each installed S/S or sync line adr is set into diag mode with a set-mode operation. Then a check is made to ensure that 'CTS' 'DSR', and 'diag mode' bits are on. Auto-call line sets are not checked. Each adr is tested in the following sequence: (1) Reset and then enable the communication scanner. (2) Set display bit (ICW bit 38). (3) Set SDF bit on for diag mode and set bit on for sync bit clock if line will run in sync mode only. (4) Set scope sync 2. (5) Set PCF = 1 and LCD = 7 for S/S lines or LCD = C for sync lines. (6) Wait for L2 irpt from the set mode and check the results. The most likely source of hardware failures detected in this rtn are the line set card(s) for the line adr under test. See note 7 at the end of this symptom index T2CS-NoteS for aid in determining a failing pattern.						
	0X01	Diag mode	L2 irpt did not occur. See X627 0X01 for reg. Card called is only a starting point to look for bit svc.	A3E2		TA331	B-310 B-260	See X629 XXXX for more information.
	0X02	Diag mode	L2 irpt from wrong line adr. Check the line adr for faults.	A3L2		TA621	B-310 B-260	See X627 0X02 for reg. See X629 XXXX for more information.
	0X03	Diag mode	PCF did not change to 0 on set-mode completion. See X627 0X03 for reg.	A3F2		TA811	B-310 B-260	See X629 XXXX for more information.
	0X04	Diag mode	Proper latches did not set. Display reg X'46' byte 0 bits 0, 2, and 5 should be on. Reg X'14' contains input from reg X'46' at the time failure was detected. Reg X'15' has a bit on for each bit position in reg X'14' that is in error. Reg X'11' = line adr under test.	A3E2		TA331	B-150	Reg X'46' bit 3 (RLSD) is ignored in this test; it may be on or off. Errors may be detected if an incoming call on a switched line brings up 'ring indicator' (reg X'46' bit 0.1).
X62D	0X01	Svc req (ICW bit 1) and L2 irpt	L2 irpt did not occur for set mode. See 0X27 0X01 for reg and checks.	A3E2		TA331	B-130 B-260	Each installed S/S or BSC line set into diagnostic rcv mode and SDF bit 9 set on. A L2 irpt should occur and 'svc req' bit (ICW bit 1) should turn on. The reset of the 'svc req' bit is then checked.
	0X02	Svc req (ICW bit 1) and L2 irpt	L2 irpt was from the wrong line adr. Check the line adr that causes the irpt for faults. Reg X'11' = line adr under test. Reg X'40' should = reg X'11'. Reg X'14' has line adr obtained from ABAR by input X'40' when the L2 occurred.	A3L2		TA621	B-300	See comments in X62D 0X01.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X62D	0X03	SDF bit 9 was turned on and should cause a character svc L2 irpt.	L2 irpt did not occur. Check oscillator or scanner or missing line set card for that line. Reg X'11' = line adr of line under test. Reg X'40' should = reg X'11'.	A3E2		TA331	B-310 B-260	See comments in X62D 0X01.
	0X04	SDF bit 9 was turned on and should cause a char-svc L2 irpt.	L2 irpt occurred from wrong line adr. Reg X'14' = line adr that caused the L2. Reg X'11' = line adr L2 was expected from.	A3E2		TA331	B-490 B-420	See comments in X62D 0X01.
	0X05	SDF bit 9 was turned on and should cause a char-svc L2 irpt with ICW bit 1 on.	ICW bit 1 ('svc-request') is not on or ICW bits 0, 2, 3, 5, 6, or 7 are on. Reg X'44' byte 0 = ICW bits 0-7 in bits 0-7.	A3P2		TA121	B-140	ICW bit 4 is ignored in this test since it may be on or off.
	0X06	SDF bit 9 was turned on and should cause a char-svc L2 irpt.	Svc request did not reset (ICW bit 1). Reg X'44' byte 0 bit 1.	A3P2		TA121	B-180	
X62E	0X01	Priority bits 1 and 2. Reg X'47'	Priority bit 2 failed to set. Reg X'11' = line adr of line under test. Reg X'40' should = reg X'11'.	A3G2		TB021	B-210	All combinations of the priority bits are checked to ensure they can be set and reset.
	0X02	Priority bits 1 and 2. Reg X'47'	Priority bit 1 failed to set. Reg X'11' = line adr under test. Reg X'40' should = reg X'11'.	A3G2		TB021	B-210	
	0X03	Priority bits 1 and 2. Reg X'47'	Priority bits 1 and 2 failed to set. Reg X'11' = line adr under test.	A3G2		TB021	B-210	
	0X04	Priority bits 1 and 2. Reg X'47'	Priority bits 1 and 2 failed to turn off. Reg X'11' = line adr under test.	A3G2		TB021	B-210	
X632	0X01	'Irpt req pending' bit (ICW 41). Reg X'47'	L2 'irpt req pending' bit did not set in ICW 41, or reg X'47'. Check that 1st set mode caused the priority reg to be occupied. Reg X'13' = line adr that should be in priority reg 3. Reg X'16' = line adr that should have 'irpt req pending' bit on. Reg X'40' should = reg X'16'.	A3L2	0040	TA641	B-300	L2 irpt are masked off and a set mode puts a line adr (ICW) in diag mode with priority select set to 3. A 2nd line adr is put into diag mode; priority select set to 3 by another set-mode operation. Then the on state of the 'irpt pending' bit is tested in the 2nd line. L2 irpt are unmasked and checked that they occur in correct order.
	0X02	'Irpt req pending' bit (ICW 41). Reg X'47'	No L2 irpt. Should have had a L2 from line adr in reg X'13'. Reg X'16' = line adr of the next expected L2 irpt.	A3L2		TA611	B-300	See X632 0X01.
	0X03	'Irpt req pending' bit (ICW 41). Reg X'47'	1st L2 irpt occurred but not from the expected line. Reg X'13' = line adr expected to irpt first. Reg X'14' = line adr that caused the L2 irpt. Reg X'16' = line adr expected to irpt next.	A3L2		TA611	B-300	See X632 0X01.
	0X04	'Irpt req pending' bit (ICW 41). Reg X'47'	No L2 irpt from 2nd line that had 'irpt pending' bit on. Reg X'13' = line adr of line that should have irpt previously. Reg X'16' = line adr expected to cause the L2 irpt.	A3L2		TA611	B-300	Check scanner, oscillator, and LIB clock if no L2 irpt occurred. See comments in X632 0X01.
	0X05	Irpt req pending bit (ICW 41). Reg X'47'	2nd L2 irpt occurred but from wrong adr. Reg X'13' = line adr of previous line that should have irpt on previous error check. Reg X'14' = line adr of line causing L2 irpt. Reg X'16' = line adr expected to cause L2 irpt.	A3L2		TA611	B-300	See X632 0X01.
X634	0X01	Upper scan limit X'01' test (8 lines)	Did not get L2 irpt from one of the 1st 8 lines when ICW bit 41 was set on. Reg X'11' = line adr L2 expected to L2 irpt. Reg X'40' should = reg X'11'.	A3L2		TA621	B-220	Only 8 lines should irpt when ICW bit 41 is set on; upper scan limits are set up to scan 8 line adr.
	0X02	Upper scan limit X'01' test (8 lines)	L2 from wrong adr. Reg X'11' = line adr expected to L2 irpt. Reg X'14' = line adr causing the L2 irpt.	A3L2		TA621	B-300	

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X634	0X03	Upper scan limit X'01' test (8 lines)	Got an unexpected L2 irpt when ICW bit 41 was set in one of the ICWs beyond the 1st 8 lines. This irpt ICW should not have been scanned to cause a L2 irpt even though its L2 'irpt pending' bit was set. Reg X'11' = line adr in which the ICW bit 41 was set. Reg X'14' is the line adr causing the L2 irpt. If reg X'11' = reg X'14', the upper scan limit 01 is not working properly.	A3L2		TA621	B-220	If reg X'11' is not = reg X'14', the unexpected L2 may be caused by a scan problem not related to the upper scan limit controls.
X635	0X01	Upper scan limit X'11' test (16 lines)	Did not get L2 irpt from one of the 1st 16 lines when ICW bit 41 was set on. Reg X'11' = line adr expecting a L2 irpt.	A3L2		TA621	B-220	Only 16 line adr should irpt when ICW bit 41 set on with scan limit set for 16 lines.
	0X02	Upper scan limit X'11' test (16 lines)	L2 irpt from wrong adr. Reg X'11' = expected adr; reg X'14' = line adr causing the L2 irpt.	A3L2		TA611	B-300	
	0X03	Upper scan limit X'11' test (16 lines)	Got an unexpected L2 irpt when ICW bit 41 was set in one of the ICW's beyond the 1st 16. This line adr should not be scanned with scan limit bits = 11, so a L2 should not occur. Reg X'11' = line adr of ICW in which bit 41 was set. Reg X'14' = line adr causing the L2. If reg X'11' = reg X'14', the upper scan limit 01 is not working properly.	A3L2		TA621	B-220	If reg X'11' is not = reg X'14', the unexpected L2 irpt may be caused by a scanner problem not related to the upper scan limit controls.
X636	0X01	Upper scan limit X'10' test (48 lines)	Did not get L2 from one of the 1st 48 lines when ICW bit 41 was set. Reg X'11' = line adr expected to L2 irpt.	A3L2		TA621	B-220	Only 48 line adr should irpt when ICW bit 41 is set on when upper scan limit is set for 48 lines.
	0X02	Upper scan limit X'10' test (48 lines)	L2 from wrong adr. Reg X'11' = line adr expected to L2 irpt. Reg X'14' = line adr on which the L2 irpt occurred.	A3L2		TA611	B-300	
	0X03	Upper scan limit X'10' test (48 lines)	Unexpected L2 irpt when ICW bit 41 was set in one of the ICWs beyond the 1st 48 line adr. With scan limit 10 set, this line should not be scanned, so no L2 should occur. Reg X'11' = line adr of ICW in which ICW bit 41 was set on. Reg X'14' = line adr that caused the L2. If reg X'11' = reg X'14', upper scan limit 01 is not working properly.	A3L2		TA621	B-220	If reg X'11' is not = reg X'14', the unexpected L2 irpt may be caused by a scanner problem not related to the scan limit controls.
X63B	0X01	Irpt priority reg	L2 irpt did not occur after unmasking L2. Reg X'13' = line adr L2 expected from.	A3L2		TA611	B-300	The 1st 4 ICWs are set up with priority settings of 3, 2, 1, and 0 in that order. ICW bit 41 ('irpt request pending') is set in the 1st four ICWs. L2 is unmasked and the ICWs are checked to ensure they irpt in proper order (1st, 2nd, 3rd, and 4th ICW).
	0X02	Irpt priority reg	L2 irpt is not from the expected adr. Reg X'13' = line adr L2 expected from. Reg X'14' = line adr that caused L2.	A3L2		TA611	B-300	
X63D	0X01	Substitution ctrl reg bit 1	Unexpected L2 irpt occurred. Reg X'14' = line adr of line causing the L2 irpt. Reg X'11' = line adr that had ICW bit 41 (L2 pending) set. If reg X'11' does not = reg X'14', there may be a LIB or scanner failure. If reg X'14' = reg X'11', substitution ctrl reg bit 1 is not working; reg X'14' is the line adr that should not have been scanned and, therefore, should not have caused a L2 irpt.	B3E2 B3D2		CX001 CX009	B-220	Substitution ctrl reg bit 1 is set on, and an attempt is made to cause a L2 irpt on lines E and F of all LIBs. These adr should not be scanned.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X63E	0X01	Substitution ctrl reg bit 2	Unexpected L2 irpt. Reg X'14' = line adr of line causing the L2. Reg X'11' = line adr of line that had ICW bit 41 (L2 pending) set. If reg X'11' does not = reg X'14' there may not be a LIB or scanner failure. If reg X'14' = reg X'11', substitution ctrl reg bit 2 is not working, reg X'14' is the line adr that should not have been scanned and, therefore, should not have caused a L2 irpt.	B3E2 B3D2		CX001 CX009	B-220	Substitution ctrl reg bit 2 is set, and an attempt is made to cause a L2 irpt on lines C and D of all LIBs. These adr should not be scanned.
X63F	0X01	Substitution ctrl reg bit 3	Unexpected L2 irpt. Reg X'14' = line adr causing the L2 irpt. Reg X'11' = line adr that had ICW bit 41 (L2 pending) set on. If reg X'11' does not = reg X'14', there may be a LIB or scanner failure. If reg X'14' = reg X'11', the substitution ctrl reg bit 3 is not working properly, and reg X'11' = the line adr that should not have been scanner and should not have caused a L2 irpt.	B3E2 B3D2		CX001 CX009	B-220	Substitution ctrl reg bit 3 is set, and an attempt is made to cause a L2 irpt on lines A and B of all LIBs. These adr should not be scanned with the scan substitution ctrl bit 3 on.
X640	0X01	Substitution ctrl reg bit 4	Unexpected L2 irpt. Reg X'14' = line adr causing the L2 irpt. Reg X'11' = line adr that had ICW bit 41 (L2 pending) set. If reg X'11' does not = reg X'14', there may be a LIB or scanner failure. If reg X'14' = reg X'11', the substitution ctrl reg bit 4 is not working, in which case reg X'14' is the line adr that should not have been scanned and, therefore, should not have caused a L2 irpt.	B3E2 B3D2		CS001 CX009	B-220	Substitution ctrl reg bit 4 is set, and an attempt is made to cause a L2 irpt on lines 8 and 9 of all LIBs. These adr should not be scanned.
X645	XXXX	Diag xmt test for S/S line sets. All installed line adr that will run in S/S mode are tested, one at a time. The test goes through xmt initial (PCF = 8) to xmt data (PCF = 9) through xmt turn-around (PCF = 9 to PCF = 7). The char xmt are a PAD char of X'FF' followed by two data characters of X'AA'. The S/S LCD of 7 (start bit, 8 data bits, 2 stop bits) is used in this test. You should refer to notes 4 and 7 at the end of this CSB symptom index for aid in problem determination if this rtn detects any errors. Prior to setting xmt initial, the pgm does a set mode with the 'diagnostic mode' bit on. If this set mode fails, you will get pretest error stop codes in DISPLAY B beginning with 1. These codes may be found in "Common Error Stops" following this CSB symptom index. With 'diag mode' set properly, the scanner should force on the 'CTS' condition so that when xmt initial is set, the next bit time should result in PCF changing from 8 to 9 (xmt initial to xmt data). The most likely source of hardware failure for this rtn is in the line set card(s) for the line adr that is under test.						
	0X01	Diag xmt test for S/S.	L2 irpt did not occur after xmt initial was set. Display reg X'45' and check byte 0 bits 0-3 for feedback check (all bits on). LCD should = 7; PCF should = 9. (PCF was set to 8 by pgm.) Reg X'11' = line adr under test. See X645 XXXX for more info.	A3L2		TA611	B-310 B-260	The scanner hardware should change the PCF from 8 to 9 when it detects 'CTS'. CTS should be forced on by the scanner if 'diagnostic mode' latch was set on properly when the set mode was done. After scanner changes PCF to 9, it should serialize and xmt a bit every bit svc time and cause a char-svc L2 irpt when the PAD char has been sent.
	0X02	Diag xmt test for S/S	L2 irpt was not from expected line adr. Reg X'14' = line adr that caused the L2 irpt. Reg X'11' = line adr that L2 was expected from.	A3L2		TA611	B-300	Check scanner, oscillator, and LIB clock if no L2 irpt occurred or L2 was from the wrong line adr. See X645 XXXX for more info.
	0X03	Diag xmt test for S/S	Primary control field (PCF) did not change to X'9'. Reg X'11' = line adr under test. See X645 XXXX for more info.	A3F2		TA811	B-080	Scanner should change PCF to 9 from 8 when it detects 'CTS' which should be forced by the scanner if diag mode set properly.
	0X04	Diag xmt test for S/S	No L2 irpt after 2nd xmt char. Reg X'11' = line adr under test. If LCD = F, a feedback check has occurred. LCD should = 7; PCF should = 9.	A3L2		TA611	B-310	
	0X05	Diag xmt test for S/S	2nd L2 irpt from wrong line adr. See X645 0X02 for reg.	A3L2		TA611	B-300	See X645 XXXX for more info.
	0X06	Diag xmt test for S/S	No L2 for xmt turnaround. Reg X'11' = line adr under test. Check reg X'45' for LCD. If LCD = F, a feedback check occurred. LCD should = 7; PCF should = 7 since PCF was set to 'D' (xmt turn-around) on the previous char-svc L2 irpt.	A3L2		TA611	B-310 B-080	See X645 XXXX for more info.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X645	0X07	Diag xmt test for S/S	3rd L2 irpt from wrong line adr. See X645 0X02 for reg.	A3L2		TA611	B-310	See X645 XXXX for more info.
	0X08	Diag xmt test for S/S	PCF did not change to X'7' (rcv mode) after turnaround or LCD changed. Reg X'11' = line adr under test.	A3F2		TA811	B-080	Scanner should change PCF to 7 on normal turn-around completion. LCD should be 7.
	0X09	Diag xmt test for S/S	SDF did not set to 0.	A3H2		TA221	B-480	SDF should be changed to 0 by scanner hardware on xmt turnaround. Reg X'15' byte 0 bits 6 and 7 contain SDF bits 0 and 1. Byte 1 contains SDF bits 2-9.
X64A	XXXX	Diag rcv mode bit svc and tag detection test. All line sets that will run in S/S or sync mode are tested. After the set mode is completed, a bit pattern of X'0301' for S/S line sets or X'0201' for sync line sets is output to SDF by an output to reg X'46'. Then the PCF is set to 7 (rcv mode) with a LCD = 7 for S/S line sets or LCD = C for sync line sets. For S/S line sets, this should cause a char-svc L2 irpt on the first scan cycle after the next bit svc occurs in the line set. For a sync line set (due to LCD = C), the char-svc L2 irpt should occur after the second bit svc and should strobe a 1 bit into PDF bit 0 from the 'test data' latch. In either case, the result should be a char of X'C0' in the PDF when the char-svc occurs.						
	0X01	Diag rcv mode bit deserializing and bit svc for all installed line adr in rcv mode (PCF = 7).	PCF did not set to X'7' (rcv mode) or LCD has changed. Reg X'11' = line adr of line set under test.	A3F2		TA811	B-190	Pgm did an output to reg X'45' to set LCD and PCF. Then an input X'45' is done to check LCD and PCF.
	0X02	Diag rcv mode, bit deserializing, and bit svc for all lines in rcv mode.	L2 irpt did not occur. Check oscillator, scanner limits, or LIB clock. Reg X'11' = line adr expected to cause L2 irpt.	A3L2		TA611	B-490	See X64A XXXX.
	0X03	Diag rcv mode, bit deserializing, and bit svc for all lines in rcv mode.	L2 irpt from wrong adr. Reg X'14' = line adr that caused L2 irpt. Reg X'11' = line adr expected to cause L2 irpt.	A3L2		TA611	B-300	See X64A XXXX.
	0X04	Diag rcv mode, bit deserializing, and bit svc for all lines in rcv mode.	Data byte in PDF (parallel data field) not expected data, or check flag on in ICW bits 0-3. Reg X'11' = line adr. Reg X'14' = flags and PDF input from reg X'44'. Reg X'16' = expected bits that should be on in reg X'14'.	A3E2 A3P2		TA311 TA131	B-490 B-420	See X64A XXXX.
X64C	XXXX	Diag xmt test for sync lines. All installed line sets that will run in sync mode are tested from xmt initial (PCF = 8) through xmt data (PCF = 9) to xmt turnaround (PCF = D to PCF = 5). Char xmt are two pad char of X'AA' and the char X'32'. Prior to setting xmt initial, the pgm does a set mode with the 'diag mode' and 'sync bit clock' bits both on. If this set mode fails, you will get pretest error stop codes in DISPLAY B beginning with 1. These codes may be found in "Common Error Stops" following this CSB symptom index. With 'diag mode' set properly, the scanner should force on the 'CTS' condition so that when xmt initial is set, the next bit time should result in PCF changing from 8 to 9 (xmt initial to xmt data).						
	0X01	Diag xmt test for BSC line sets.	L2 did not occur after xmt initial. LCD should = C. If LCD = F, a feedback check occurred so line set or LIB is probably in error. If LCD = C, check PCF. PCF was set to 8 but should have changed to 9 as the 1st char was xmt. If the char was not xmt, check for oscil-lator/LIB clock error or scanner failure.	A3L2		TA611	B-310 B-260	See X64C XXXX and notes 4 and 7 at the end of this CSB symptom index for checks to make to aid problem determination. Reg X'11' = line adr of line set under test.
	0X02	Diag xmt test for BSC	L2 from wrong line adr. Display reg X'14' for line adr that caused the L2 irpt and reg X'11' for the line adr expected to cause the L2 irpt.	A3L2		TA611	B-300	See notes 4 and 7 at the end of this CSB symptom index for problem determination aids.
	0X03	Diag xmt test for BSC	PCF did not change to X'9' (xmt data). Reg X'11' = line adr. LCD and PCF same as X64C 0X01.	A3F2		TA811	B-080	See X64C XXXX.
	0X04	Diag xmt test for BSC	2nd L2 irpt did not occur. See X64C 0X01 for LCD and PCF.	A3L2		TA611	B-310 B-260	See X64C XXXX.
	0X05	Diag xmt test for BSC	2nd L2 irpt from wrong line adr. Check failing line adr for cause of of error. See X64C XXXX.	A3L2		TA611	B-300	Reg X'14' = line adr that caused the L2 in error. Reg X'11' = line adr expected to cause L2.
	0X06	Diag xmt test for BSC	L2 irpt did not occur after setting PCF to X'D' for xmt turnaround. Check if LCD = F (feedback check). PCF should = 5, since on last char svc, it was set to 'D'. If PCF is not 5, then turnaround did not work. Reg X'11' = line adr under test.	A3L2		TA611	B-080	See X64C XXXX. LCD should = C. PCF should have changed to 5.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X64C	0X07	Diag xmt test for BSC	3rd L2 irpt from wrong line adr. Check failing line adr for cause of error. See X64C XXXX.	A3L2		TA611	B-300	Reg X'14' = line adr that caused the L2 in error. Reg X'11' = line adr expected to cause L2.
	0X08	Diag xmt test for BSC	PCF did not change to 5 on xmt turnaround, or LCD is not = C. Reg X'11' = line adr under test.	A3F2		TA811	B-080	PCF should have changed to 5, and LCD should have remained at C.
X650	XXXX	Wrap data test for S/S line sets using LCD = 7. All lines that run is S/S mode (except telegraph line sets) are wrapped two at a time. The first installed S/S line is made the rcv line and the next installed S/S line is made a xmt line. As each pair of lines completes its wrap, the lines are reset. The line that was the xmt line is now made the rcv line and the next installed S/S line is made the xmt line. This is continued until the last installed S/S line has been used as a xmt line. The last installed S/S line is then made a rcv line and the first installed line is made the xmt line for the last wrap performed in this rtn. Data sent on the xmt line will be the PAD character (X'FF') and the characters X'AA', X'01' and X'FE'. The test is run with LCD = 7 so the hardware should add a start bit and two stop bits to the character being xmt. The rcv line should rcv the xmt characters except for the PAD character. NOTES: **Note 1:** See notes 4, 5 and 7 in section T2CS-NoteS for more information and for aid in problem determination and isolation. **Note 2:** For all error stops in this rtn, the following reg are set up: Reg X'11' = xmt line adr (as used to set ABAR) Reg X'13' = rcv line adr (as used to set ABAR) Reg X'14' (for errors that indicate L2 irpt occurred from wrong adr) contains the line adr that caused the L2 irpt. Reg X'14' (for errors that indicate the rcv data is bad or ICW bits 0-7 are in error) contains ICW bits 0-15 from the rcv line ICW obtained by executing input X'44'. ICW bits 8-15 (the PDF) contain the rcv data. ICW bits 0-7 are check and control flags and are always expected to be set as follows: ICW bit 0 = stop bit check; should be off. ICW bit 1 = svc req; should be on. ICW bit 2 = char overrun/underrun; should be off. ICW bit 3 = modem check; should be off. ICW bit 4 = rcv line signal detect; this bit is ignored in this test. ICW bit 5 = reserved bit; this bit is ignored in this test. ICW bit 6 = pgm flag; this bit is ignored in this test. ICW bit 7 = pad flag; this bit is ignored in this test. Reg X'16' (for errors that indicate the rcv data is bad) contains the expected ICW bits 0-15 that are being tested against the contents of reg X'14'. The rcv line always has the display bit on in its ICW, so reg X'46' is valid for the rcv line under test. All lines are set to priority 3 and oscillator select 0. The following error codes are listed in the sequence in which the actual test is run.						
	0X01	First L2 irpt for xmt line adr (not counting the set mode)	No L2 irpt occurred. Reg X'11' = xmt line adr. Reg X'13' = rcv line adr.	A3L2		TA611	B-310 B-260	Should have char-svc L2 irpt from the xmt line adr after the PAD char was xmt. See notes 4, 5, and 7 at the end of this CSB symptom index for checks to make and aids in problem determination.
	0X02	First L2 irpt for xmt line adr	L2 irpt from wrong line adr. Reg X'11' = xmt line adr and the line adr expected to cause the L2 irpt. Reg X'13' = rcv line adr. Reg X'14' = line adr that caused the L2 irpt.	A3L2		TA611	B-300	See checks and comments in X650 XXXX.
	0X03	Xmt line PCF changed to 9 as the PAD char of X'FF' is xmt.	Xmt line PCF did not change to 9, or LCD not = 7. Reg X'11' = xmt line adr.	A3F2		TA811	B-080	See checks and comments in X650 XXXX. Character X'01' is output to the PDF of xmt line after this error display. Previous PDF char of X'AA' should now be in process of transmission from SDF.
	0X04	Rcv line rcv char X'AA' (first rcv line L2 irpt after set mode)	No L2 irpt occurred. Reg X'11' = xmt line adr. Reg X'13' = rcv line adr and line adr expected to cause the L2 irpt.	A3L2		TA611	B-490	See checks and comments in X650 XXXX. This should be the 2nd L2 irpt after pgm set scope sync 2.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X650	0X05	Rcv line rcv character X'AA'	L2 irpt from wrong adr. Reg X'11' = xmt line adr. Reg X'13' = rcv line adr and the line expected to cause the L2 irpt. Reg X'14' = line adr causing the L2.	A3L2		TA611	B-300	See checks and comments in the X650 XXXX.
	0X06	Rcv line rcv character X'AA'	Rcv line PCF not = 7, or LCD not = 7. Reg X'13' = rcv line adr.	A3F2		TA811	B-080	Rcv PCF was set to 7-(rcv mode) by the pgm and should not have changed. See checks and comments in X650 XXXX.
	0X07	Rcv line rcv character X'AA'	Rcv data in rcv line PDF not X'AA', or ICW bits 0-3 in error.	A3E2 A3P2		TA311 TA131	B-490	See X650 XXXX for reg and checks.
	0X08	Xmt of X'AA' completed	No L2 irpt occurred. Reg X'11' = xmt line adr expected to cause a L2.	A3L2		TA611	B-310 B-260	Should have completed the transmission of X'AA'. The X'01' that was in the PDF should have transferred to the SDF and be in the process of being xmt. This is the 3rd L2 irpt after pgm set scope sync 2. See checks and comments in X650 XXXX.
	0X09	Xmt of X'AA' completed	L2 irpt from wrong adr. Reg X'11' = xmt line adr and the adr expected to cause the L2. Reg X'13' = rcv line adr. Reg X'14' = line adr that caused the L2.	A3L2		TA611	B-300	See checks and comments in X650 XXXX. After this error display, the xmt line's PDF is set to X'FE' for the next xmt char.
	0X0A	Rcv char X'01'	No L2 irpt occurred. Reg. X'13' = rcv line adr expected to cause a char-svc L2 irpt.	A3L2		TA611	B-490	Should rcv char X'01' in PDF and char-svc L2 irpt. This should be 4th L2 (2nd from rcv line adr) after pgm set scope sync 2. See X650 XXXX for reg and checks.
	0X0B	Rcv char X'01'	L2 irpt from wrong adr. Reg X'11' = xmt line adr. Reg X'13' = rcv line adr and the adr expected to cause L2 irpt. Reg X'14' = line adr causing L2 irpt.	A3L2		TA611	B-300	See checks and comments in X650 XXXX.
	0X0C	Rcv char X'01'	Data rcv not X'01', or ICW bits 0-3 in error.	A3E2 A3P2		TA311 TA131	B-490	See checks and comments in X650 XXXX.
	0X0D	Xmt of X'01' completed	No L2 irpt occurred. Reg X'11' = xmt line adr expected to cause the L2 char-svc irpt.	A3L2		TA611	B-310 B-260	Should have just completed transmission of char X'01'. X'FE' should have been transferred from the PDF to the SDF and be in the process of being xmt. This is the 5th L2 (3rd from xmt line adr) after pgm set scope sync 2. See checks and comments in X650 XXXX.
	0X0E	Xmt of X'01' completed	L2 irpt from wrong line adr. Reg X'11' = xmt line adr and adr expected to cause the L2. Reg X'13' = rcv line adr. Reg X'14' = line adr that caused the L2 irpt.	A3L2		TA611	B-300	See checks and comments in X650 XXXX. After this error check is made, the xmt line's PCF is set to X'D' to cause xmt turnaround.
	0X0F	Rcv char X'FE'	No L2 irpt occurred.	A3L2		TA611	B-490	This is the 6th L2 (3rd from rcv line adr). Last L2 expected for rcv line. See checks and comments in X650 XXXX.
	0X10	Rcv char X'FE'	L2 irpt from wrong adr. Reg X'11' = xmt line adr. Reg X'13' = rcv line adr and adr expected to cause L2 irpt. Reg X'14' = line adr causing the L2 irpt.	A3L2		TA611	B-300	See checks and comments in X650 XXXX.

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Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X650	0X11	Rcv char X'FE'	Rcv data not X'FE', or ICW bits 0-3 in error.	A3E2 A3P2		TA311 TA131	B-490	See comments in X650 XXXX.
	0X12	Xmt of X'FE' completed and xmt turnaround.	No L2 irpt occurred. Reg X'11' = xmt line adr and adr expected to cause L2.	A3L2		TA611	B-310 B-260	7th L2 (4th from rcv line adr) after pgm set scope sync 2. Xmt turnaround (PCF = D) was set after the previous L2 irpt for xmt line, so xmt line should now be turned around to rcv mode (PCF = 7).
	0X13	Xmt of X'FE' completed and xmt turnaround.	L2 irpt from wrong adr. Reg X'11' = xmt line adr and adr expected to cause the L2. Reg X'13' = rcv line adr. Reg X'14' = line adr that caused the L2 irpt.	A3L2		TA611	B-300	See checks and comments in X650 XXXX.
	0X14	Xmt turnaround.	Xmt line PCF did not change to 7 on turnaround; or xmt SDF did not set to 0, or LCD not = 7.	A3F2 A3H2		TA811 TA211	B-080	When xmt turnaround is completed, the SDF should be X'000', PCF should be 7, and LCD should be 7. See checks and comments in X650 XXXX.

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Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X652	XXXX							

Wrap data test S/S line sets with LCDs of 0, 2, 4, 5, and 6. All installed S/S line adr, except telegraph, are wrapped two at a time. The first installed S/S line is made the rcv line, and the next installed S/S line is made a xmt line. As each pair of lines completes its wrap, the lines are reset. The line that was the xmt line is made the rcv line, and the next installed S/S line is made the new xmt line. Then the test is run on this pair of lines. This is continued until the last installed S/S line has been used as a xmt line. At this time, the last installed S/S line is made a rcv line, and the first installed line is made the xmt line; and the test is run. After the above is done with LCD = 0, the whole process is repeated for LCD = 2, for LCD = 4, for LCD = 5, and then for LCD = 6.

Note: LCD = 7 is tested in rtn X650. This test is not run if the 1st installed oscillator exceeds 1200 bits per second.

Date to be xmt and rcv for each LCD should be:

LCD = 0; data = X'2A', X'01', and X'3E'
LCD = 2; data = X'0A', X'01', and X'1E'
LCD = 4; data = X'2A', X'01', and X'7E'
LCD = 5; data = X'2A', X'01', and X'7E'
LCD = 6; data = X'AA', X'01', and X'FE'

The hardware should add a start bit and one or two stop bits to the xmt char according to LCD type. A PAD char (X'FF') is always xmt before the data char are xmt. The rcv line should rcv the xmt char except for the PAD char.

Note: For all error stops in this rtn, the following regs are set up:

Reg X'11' = xmt line adr (as used to set ABAR)
Reg X'13' = rcv line adr (as used to set ABAR)
Reg X'14' (for errors that indicate L2 irpt occurred from wrong adr) contains the line adr that caused the L2 irpt.

Reg X'14' (for errors that indicate the rcv data is bad or ICW bits 0-7 are in error) contains ICW bits 0-15 from the rcv line ICW obtained by executing input X'44'. ICW bits 8-15 (the PDF) contain the rcv data. ICW bits 0-7 are check and control flags and are always expected to be set as follows:

ICW bit 0 = stop bit check; should be off.
ICW bit 1 = svc req; should be on.
ICW bit 2 = char overrun/underrun; should be off.
ICW bit 3 = modem check; should be off.
ICW bit 4 = rcv line signal detector; this bit is ignored in this test.
ICW bit 5 = reserved bit; this bit is ignored in this test.
ICW bit 6 = pgm flag; this bit is ignored in this test.
ICW bit 7 = pad flag; this bit is ignored in this test.

Reg X'16' (for errors that indicate the rcv data is bad) contains the expected ICW bits 0-15 that are being tested against the contents of reg X'14'.
Reg X'16' (for errors that indicate LCD changed or PCF is bad) contains expected LCD and PCF in byte 0.

The rcv line always has the display bit on in its ICW, so reg X'46' is valid for the rcv line under test. All lines are set to priority 3 and oscillator select 0. Refer to notes 4, 5, and 7 at the end of this symptom index for aid in problem determination. The following error codes are listed in the sequence in which the actual test is run.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X652	0X01	First L2 irpt for xmt line (not counting set mode)	No L2 irpt occurred. Reg X'11' = xmt line adr. Reg X'13' = rcv line adr.	A3L2		TA611	B-310 B-260	Should have char-svc L2 irpt after the PAD char was xmt. Check LCD for feedback check. You may use the continue function to determine if only this line set, this LIB, or all lines in the scanner are failing. If all lines are failing, the first oscillator card or the scanner cards are probably bad. If all lines in one LIB are failing, check the bit clock control card. If only 1 line or a pair of lines is failing, the problem is probably the line set card(s) for the failing line adr.
	0X02	First L2 irpt for xmt	L2 irpt from wrong adr. Reg X'11' = xmt line adr and the adr expected to cause L2 irpt. Reg X'13' = rcv line adr. Reg X'14' = line adr that caused the L2.	A3L2		TA611	B-300	See checks and comments under X652 0X01.
	0X03	Xmt line PCF changed to 9 as the PAD char X'FF' is xmt	Xmt line PCF did not change to 9 or LCD changed. Reg X'11' = xmt line adr.	A3F2		TA811	B-080	See checks and comments under X652 0X01. Set X'01' in xmt PDF after this error display. Previous PDF char of X'AA' should be in process of transmission from SDF now.
	0X04	Rcv first char	No L2 irpt occurred. Reg X'13' = rcv line adr and line adr expected to cause the L2. Reg X'11' = the xmt line adr.	A3L2		TA611	B-490	See checks and comments under X652 0X01. This is the 2nd L2 after pgm set scope sync 2.
	0X05	Rcv first char	L2 irpt from wrong line adr. Reg X'13' = rcv line adr and the line expected to cause L2 irpt. Reg X'11' = xmt line adr. Reg X'14' = line adr that caused L2.	A3L2		TA611	B-300	See checks and comments under X652 0X01.
	0X06	Rcv first char	Rcv line PCF not = 7 or LCD changed. Reg X'13' = rcv line adr.	A3F2		TA811	B-080	Rcv PCF set to 7 (rcv mode) during initial setup and should have remained at 7. See X652 XXXX for reg and checks.
	0X07	Rcv first char	Rcv data in PDF not = expected rcv data, or ICW bits 0-3 in error.	A3E2 A3P2		TA311 TA131	B-490	See X652 XXXX for reg. See comments under X652 0X01 for aid in determining the failing pattern.
	0X08	Xmt of X'AA' completed	No L2 irpt occurred. Reg X'11' = xmt line adr expected to cause the L2 irpt.	A3L2		TA611	B-310 B-260	Should have just completed the transmission of X'AA'. The X'01' that was in the PDF should have transferred to the SDF and be in the process of being xmt. This is the 3rd L2 irpt after pgm set scope sync 2. See checks and comments under X652 0X01.
	0X09	Xmt of X'AA' completed	L2 irpt from wrong adr. Reg X'11' = xmt line adr and the adr expected to cause L2 irpt. Reg X'13' = rcv line adr. Reg X'14' = line adr that caused the L2 irpt.	A3L2		TA611	B-300	See checks and comments under X652 0X01. After this error display, the xmt lines PDF is set to X'FE'.
	0X0A	Rcv char X'01'	No L2 irpt occurred. Reg X'13' = rcv line adr expected to cause L2.	A3L2		TA611	B-490	Should have rcv the char X'01' in the PDF and had a char-svc L2 irpt. This should be the 4th L2 irpt (2nd from the rcv line) pgm set scope sync 2. See checks and comments under X652 0X01.
	0X0B	Rcv char X'01'	L2 irpt from wrong adr. Reg X'11' = xmt line adr. Reg X'13' = rcv line adr and the adr expected to cause L2 irpt. Reg X'14' = adr of line causing L2 irpt.	A3L2		TA611	B-300	See checks and comments under X652 0X01.
	0X0C	Rcv char X'01'	Data rcv not X'01', or ICW bits 0-3 in error.	A3E2 A3P2		TA311 TA131	B-490	See comments under X652 0X07.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X652	0X0D	Xmt of X'01' completed	No L2 irpt occurred. Reg X'11' = xmt line adr expected to cause the L2 irpt.	A3L2		TA611	B-310 B-260	Should have just completed xmt char X'01'. Char X'FE' should have transferred from the PDF to the SDF and be in the process of being xmt. This is the 5th L2 (3rd from xmt line adr) after setting scope sync 2. See checks and comments under X652 0X01.
	0X0E	Xmt of X'01' completed	L2 irpt from wrong adr. Reg X'11' = xmt line adr the L2 was expected from. Reg X'13' = rcv line adr. Reg X'14' = line adr that caused L2 irpt.	A3L2		TA611	B-300	See checks and comments under X652 0X01. After this error, the xmt PCF is set to 'D' for turnaround.
	0X0F	Rcv 3rd char	No L2 irpt occurred.	A3L2		TA611	B-490	This is the 6th L2 (3rd from rcv line adr) and last L2 irpt for rcv line. See checks and comments under X652 0X01.
	0X10	Rcv 3rd char	L2 irpt from wrong adr. Reg X'11' = xmt line adr. Reg X'13' = rcv line adr and the line expected to cause L2 irpt. Reg X'14' = line adr causing the L2 irpt.	A3L2		TA611	B-300	See checks and comments under X652 0X01.
	0X11	Rcv 3rd char	Rcv data in PDF not = to expected data, or ICW bits 0-3 in error.	A3E2 A3P2		TA311 TA131	B-490	See comments under X652 0X07 for ICW bits.
	0X12	Xmt of X'FE' completed and xmt turnaround.	No L2 irpt occurred. Reg X'11' = xmt line adr expected to cause the L2 irpt.	A3L2		TA611	B-310 B-260	This is the 7th L2 (4th from the xmt line adr) after pgm set scope sync 2. Xmt turnaround (PCF = D) was set after previous L2 for xmt line, so xmt line should now be turned around to rcv mode. (PCF = 7).
	0X13	Xmt of X'FE' completed and xmt turnaround.	L2 irpt from wrong adr. Reg X'11' = xmt line adr and the adr expected to cause L2 irpt. Reg X'13' = rcv line adr. Reg X'14' = line adr that caused the L2 irpt.	A3L2		TA611	B-300	See checks and comments under X652 0X01.
	0X14	Xmt turnaround	Xmt line PCF did not change to 7 on turnaround; or xmt SDF did not set to 0, or LCD is not = 7.	A3F2 A3H2		TA811 TA211	B-080	When xmt turnaround is completed, the SDF should = 000, PCF should = 7, and LCD should = 7. See comments in X652 0X01.
X656	XXXX	Sync line sets wrap data test. All installed line adr that run in sync mode (even though they also run in S/S mode and have been already tested in rtn X650) are wrapped two at a time. The first installed sync line adr is made the rcv line, and the next installed sync line adr is made the xmt line adr. The test is performed on this pair of lines. When the test is completed on this pair of lines, the lines are reset; the line that was the xmt line is now made the rcv line, and the next installed sync line adr is made the new xmt line. This pair of lines is then wrapped. This stepping through the lines is continued until the last installed sync line has been the xmt line. Then the first installed line is made the xmt line, and the last installed sync line is made the rcv line; this pair of lines is wrapped. All the installed sync line sets are wrapped with LCD = C, and then the above procedure is repeated using LCD = D. A set mode is executed for both the xmt and rcv line adr with ICW bit 27 (diag wrap mode) and ICW bit 29 (sync bit clock) on. Oscillator select bits are 0's to select the first oscillator. The priority bits are set to 3. The set mode is executed before the setting of scope sync 2 as each pair of lines is wrapped. The set mode must complete successfully for the wrap to function; any errors detected during the set mode are pretest errors, and all start with error code 1XXX. These error codes are located in "Common Error Stops" following this CSB symptom index. References to L2 irpt in the following error code displays are the char-svc L2 irpt that occur after scope sync 2 is set; they do not include the L2 irpt that occurred for the set modes that occur before scope sync 2.					

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X656	XXXX	NOTES: **Note 1:** For all error stops in this rtn, the following regs are set up: Reg X'11' = xmt line adr (as used to set ABAR) Reg X'13' = rcv line adr (as used to set ABAR) Reg X'14' (for errors that indicate L2 irpt occurred from wrong adr) contains the line adr that caused the L2 irpt. Reg X'14' (for errors that indicate the rcv data is bad or ICW bits 0-7 are in error) contains ICW bits 0-15 from the rcv line ICW obtained by executing input X'44'. ICW bits 8-15 (the PDF) contain the rcv data. ICW bits 0-7 are check and control flags and are always expected to be set as follows: ICW bit 0 = stop bit check; should be off. ICW bit 1 = svc req; should be on. ICW bit 2 = char overrun/underrun; should be off. ICW bit 3 = modem check; should be off. ICW bit 4 = rcv line signal detector; this bit is ignored in this test. ICW bit 5 = reserved bit; this bit is ignored in this test. ICW bit 6 = pgm flag; this bit is ignored in this test. ICW bit 7 = pad flag; this bit is ignored in this test. Reg X'16' (for errors that indicate the rcv data is bad) contains the expected ICW bits 0-15 that are being tested against the contents of reg X'14'. **Note 2:** Checks to be made on all error stops: A. Check LCD of failing line adr. If LCD = F, a feedback check has occurred. If the configuration data set (CDS) erroneously indicates a line set is installed that will run in sync mode, a feedback check will occur. B. You may use the continue function (except on pretest errors starting with 1) to continue from this error to (1) see if just this line adr is failing, (2) see if all line adr in this LIB are failing, or (3) see if all sync lines are failing. You may get additional error stops on the same line pair being wrapped, so you may have to use the continue function multiple times. If only one line set is failing or a pair of even/odd adr, the line set card is probably bad. If all adr fail in one LIB, the LIB's bit clock control card may be bad, or the terminators may be bad. If all sync line adr fail, the scanner cards may be bad. If the line adr are the type that run in both sync and S/S mode and if they run successfully in rtn X652, then suspect LCD = C or LCD = D circuitry or the sync bit clock control line. Refer to the LIB section in Volume 3 (LIBs and line sets) because card locations vary in location according to LIB types. The xmt data char are shifted by one data bit position from the rcv data char to generate a predictable irpt sequence. See notes 4 and 6 at the end of this CSB symptom index for more info about this shifting of xmt data char. Xmt data - 55 55 19 19 50 7F 80 00 (when using EBCDIC LCD of C) Rcv data - 32 A0 FE 00 01 (when using EBCDIC LCD of C) Xmt data - 55 55 0B 0B 50 7F 80 00 (when using ASCII LCD of D) Rcv data - 16 A0 FE 00 01 (when using ASCII LCD of D). The rtn is run in the same sequence as that of the following error codes.							
	0X01	Xmt of 1st PAD completed	No L2 irpt occurred from xmt line adr.	A3L2		TA611	B-310 B-260	1st char-svc L2 irpt after scope sync 2. See X656 XXXX notes 1 and 2 for reg and checks.
	0X02	Xmt of 1st PAD completed	L2 irpt not from xmt line adr.	A3L2		TA611	B-300	See X656 XXXX notes 1 and 2 for reg and checks.
	0X03	Xmt PCF changes from 8 to 9.	Xmt PCF not = 9, or LCD changed.	A3F2		TA811	B-080	Xmt PCF was set to 8 by pgm during hardware setup. The scanner hardware should have changed the PCF to 9 and should now be in process of xmt 2nd pad char. The xmt PDF is set to the 1st SYN char after this error display. See X656 XXXX notes 1 and 2 for reg and checks.
	0X04	Xmt of 2nd PAD completed	No L2 irpt occurred from xmt line adr.	A3L2		TA611	B-310 B-260	2nd L2 irpt after scope sync 2. See X656 XXXX notes for reg and checks.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X656	0X05	Xmt of 2nd PAD completed	L2 irpt not from xmt line adr.	A3L2		TA611	B-300	See X656 XXXX notes 1 and 2 for reg and checks. After this error display, the xmt PDF is set with the 2nd SYN char.
	0X06	Xmt of 1st SYN completed	No L2 irpt occurred from xmt line adr.	A3L2		TA611	B-310 B-260	3rd L2 irpt after scope sync 2. See notes 1 and 2 in X656 XXXX for reg and checks.
	0X07	Xmt of 1st SYN completed	L2 irpt not from xmt line adr.	A3L2		TA611	B-300	See X656 XXXX notes 1 and 2 for reg and checks. After this error display, the xmt PDF is set to char X'A0' to be xmt next. Should now be in process of xmt 2nd SYN char.
	0X08	Rcv 1st SYN	Rcv line PCF not = 7, or LCD changed.	A3F2		TA811	B-080	Rcv line PCF was set to 5. When the 1st SYN character is rcv and recognized, the hardware should set the rcv PCF = 7. **Note:** This setting of PCF = 7 from PCF = 5 does not cause a L2 irpt. See notes 1 and 2 in X656 XXXX for reg checks.
	0X09	Rcv 2nd SYN	No L2 irpt occurred from rcv line adr.	A3L2		TA611	B-310 B-420	4th L2 (1st from the rcv line adr) after scope sync 2. See notes 1 and 2 in X656 XXXX for reg and checks.
	0X0A	Rcv 2nd SYN	L2 irpt not from rcv line adr.	A3L2		TA611	B-300	See X656 XXXX notes 1 and 2 for reg and checks.
	0X0B	Rcv 2nd SYN	Rcv data in PDF not a SYN char, or ICW bits 0-3 in error.	A3E2 A3P2		TA311 TA131	B-420	Rcv data in PDF should = X'32' SYN if LCD = C or X'16' SYN char if LCD = D. See notes 1 and 2 in X656 XXXX for reg, ICW bits 0-7, and checks to make.
	0X0C	Xmt of 2nd SYN completed	No L2 irpt occurred for xmt line adr.	A3L2		TA611	B-310 B-260	5th L2 (4th from the xmt line adr) after pgm set scope sync 2. See notes 1 and 2 in X656 XXXX for reg and checks.
	0X0D	Xmt of 2nd SYN completed	L2 irpt not from xmt line adr.	A3L2		TA611	B-300	See X656 XXXX notes 1 and 2 for reg and checks. After this error display, the xmt PDF is set to char X'7F' as the next char to xmt. The char X'50' should now be in the process of being xmt.
	0X0E	Rcv char X'A0'	No L2 irpt occurred from the rcv line adr.	A3L2		TA611	B-310 B-420	6th L2 (2nd from the rcv line adr) after scope sync 2. See notes 1 and 2 in X656 XXXX for reg and checks.
	0X0F	Rcv char X'A0'	L2 irpt not from rcv line adr.	A3L2		TA611	B-300	See X656 XXXX notes 1 and 2 for reg and checks.
	0X10	Rcv char X'A0'	Rcv data in PDF not = X'A0', or ICW bits 0-3 in error.	A3E2 A3P2		TA311 TA131	B-420	See X656 XXXX notes 1 and 2 for reg, ICW bits 0-7, and checks to make.
	0X11	Xmt of X'50' completed	No L2 occurred for xmt line adr.	A3L2		TA611		7th L2 (5th from the xmt line adr). See notes 1 and 2 in X656 XXXX for reg and checks.
	0X12	Xmt of X'50' completed	L2 not from xmt line adr.	A3L2		TA611		See X656 XXXX notes 1 and 2 for reg and checks. After this error display, the xmt PDF is set to X'80' as the next char to xmt. Should now be in process of xmt the char X'7F'.
	0X13	Rcv char X'FE'	No L2 irpt occurred for rcv line adr.	A3L2		TA611	B-310 B-420	8th L2 (3rd from the rcv line adr). See notes 1 and 2 in X656 XXXX for reg and checks to make.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X656	0X14	Rcv char X'FE'	L2 irpt not from rcv line adr.	A3L2		TA611	B-300	See X656 XXXX notes 1 and 2 for reg and checks.
	0X15	Rcv char X'FE'	Rcv data in PDF not = X'FE', or ICW bits 0-3 in error.	A3E2 A3P2		TA311 TA131	B-420	See X656 XXXX notes 1 and 2 for reg, ICW bits 0-7, and checks to make.
	0X16	Xmt of X'7F' completed	No L2 occurred for xmt line adr.	A3L2		TA611		9th L2 (6th from the xmt line adr). See notes 1 and 2 in X656 XXXX for reg and checks.
	0X17	Xmt of X'7F' completed	L2 not from xmt line adr.	A3L2		TA611		See X656 XXXX notes 1 and 2 for reg and checks. After this error display, the xmt PDF is set to X'00' as the next char to xmt. Should now be in the process of xmt X'80'.
	0X18	Rcv char X'00'	No L2 irpt occurred from rcv line adr.	A3L2		TA611	B-310 B-420	10th L2 (4th from the rcv line adr). See notes 1 and 2 in X656 XXXX for reg and checks to make.
	0X19	Rcv char X'00'	L2 irpt not from rcv line adr.	A3L2		TA611	B-300	See X656 XXXX notes 1 and 2 for reg and checks.
	0X1A	Rcv char X'00'	Rcv data in PDF not = X'00', or ICW bits 0-3 in error.	A3E2 A3P2		TA311 TA131	B-420	See X656 XXXX notes 1 and 2 for reg, ICW bits 0-7, and checks.
	0X25	Xmt of X'80' completed	No L2 occurred from xmt line adr.	A3L2		TA611		12th L2 (7th from xmt). See notes 1 and 2 in X656 XXXX for reg and checks.
	0X26	Xmt of X'80' completed	L2 not from xmt line adr.	A3L2		TA611		See X656 XXXX notes 1 and 2 for reg and checks. After this error display, the xmt PCF is set to X'D' for xmt turnaround. Should now be in process of xmt X'00' as last char to xmt.
	0X27	Rcv char X'01'	No L2 occurred from rcv line adr.	A3L2		TA611		12th L2 (7th from rcv). See notes 1 and 2 in X656 XXXX for reg and checks. Last L2 for rcv.
	0X28	Rcv char X'01'	L2 not from rcv line adr.	A3L2		TA611		See X656 XXXX notes 1 and 2 for reg and checks.
	0X29	Rcv char X'01'	Rcv data in PDF not = X'11', or ICW bits 0-3 in error.	A3E2 A3P2		TA311 TA131		See X656 XXXX notes 1 and 2 for reg, ICW bits 0-7, and checks. After this error display, the rcv PCF is set to 0, so no further L2 irpt should occur from the rcv line adr.
	0X2A	Xmt of X'00' completed and xmt turnaround	No L2 occurred from xmt line adr.	A3L2		TA611		13th L2 (10th from xmt) and should be the last L2. See notes 1 and 2 in X656 XXXX for reg and checks. At this time, the xmt PCF should have turned around to PCF = 5.
	0X2B	Xmt of X'00' completed and xmt turnaround	L2 not from xmt line adr.	A3L2		TA611		See X656 XXXX notes 1 and 2 for reg and checks. PCF should be turned around to PCF = 5.
	0X2C	Xmt turnaround	Xmt PCF did not turn around to PCF = 5, or LCD changed.	A3F2		TA811		After previous xmt L2 (see X656 0X26), xmt PCF was set to X'D' to cause a turnaround. The hardware should have completed the transmission of the char X'00' and then set PCF = 5. See notes 1 and 2 in X656 XXXX for reg and checks.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X65A	XXXX	DLC line sets wrap data test. All installed line sets that will run in DLC mode are wrapped two at a time. The first installed DLC line set is made the rcv line, and the next installed DLC line set is made the xmt line. The test is then performed on this pair of lines. When the test is completed on this pair of lines, the lines are reset; the line that was the xmt line is now made the rcv line, and the next installed DLC line set is made the new xmt line. Then this pair of lines is wrapped. This stepping up through the lines is continued until the last installed DLC line has been made the xmt line. The first installed line is then made the xmt line, and the last installed DLC line is made the rcv line; this pair of lines is wrapped. A set mode is done on both the xmt and rcv lines with ICW bit 27 (diag wrap mode) and ICW bit 29 (sync bit clock) both on. Oscillator select bits are 0 so the first oscillator is selected. The priority bits are set to 3. The set mode is done before the setting of scope sync 2 as each pair of lines is wrapped. The set mode must be completed successfully for the wrap to function; any errors detected during set mode are pretest errors and start with error code 1XXX. These error codes are in "Common Error Stops" following this CSB symptom index. References to L2 irpt in the following error codes are the char-svc L2 irpt that occur after scope sync 2 is set; they do not include L2 irpt that occurred for set mode before scope sync 2. **NOTES:** **Note 1:** On all error stops in this rtn, the following reg are set up: Reg X'11' = xmt line set adr (as used to set ABAR) Reg X'13' = rcv line set adr (as used to set ABAR) Reg X'14' (for errors that indicate no L2 occurred or L2 from wrong adr) = line adr that caused the L2, or = 0000 if no L2 occurred. Reg X'14' (for errors that indicate rcv data is bad or ICW bits 0-3 or 5 are in error) = what was obtained by an input X'44' from the rcv line ICW (bits 0-15). ICW bits 8-15 are the PDF and should contain the rcv data. ICW bits 0-7 are error and control flags and are expected to be set as follows: ICW bit 0 = stop bit check; should be off. ICW bit 1 = svc req; should be on. ICW bit 2 = char overrun; should be off except when misaligned flag char is detected. ICW bit 3 = modem check; should be off. ICW bit 4 = rcv line signal detect; this bit is ignored in this test. ICW bit 5 = DLC flag detect/disable stuffer remember; on when a flag char is detected. ICW bit 6 = pgm flag; this bit is ignored. ICW bit 7 = PAD flag/disable stuffer bit; on only when a flag or pad char is set into the PDF for the xmt line adr. This bit is ignored on the rcv line adr. Reg X'14' (for errors that indicate the LCD or PCF is bad) contains the LCD in byte 0 bits 0-3 and the PCF in byte 0 bits 4-7. Reg X'16' (for errors that indicate rcv data is bad) contains the expected ICW bits 0-15 that are being tested against the contents of reg X'14', except bits 4, 6, and 7 are ignored. **Note 2:** Checks to be made on all error stops: A. Check LCD of failing line set. If LCD = F, a feedback check has occurred. If the CDS indicates a line set that will run in sync mode is installed but this is not the case, a feedback check will occur. B. Use the continue function (except on pretest errors starting with 1) to continue from the error to see if just this line set is failing, if all line sets in this LIB are failing, or if all DLC lines are failing. Multiple error stops on the same pair of wrapped lines may occur so the continue function may have to be used many times. If only one line set is failing or a pair of even/odd adr, the line set card is probably bad. If all adr fail in one LIB, the LIB's bit clock control card or terminators may be bad. If all DLC line sets fail, the communication scanner cards may be bad. If the line sets are the type that will run also in sync and S/S mode and if they run successfully in rtn X652 and X656, then suspect the LCD or DLC circuitry or sync bit clock control. **Note 3:** The xmt char are offset by 1 data bit to cause rcv data char to be offset by 1 data bit from xmt char. See notes 4 and 6 following this CSB symptom index for more info. Xmt data - AA 2A 3F 50 7F 00 7F Rcv data - flag A0 FE 00 idle All installed DLC line sets are tested in 8-bit mode (LCD = 9). The rtn is run in the same sequence as that of the following error codes.							
	0X01	Xmt of 1st PAD char (X'AA') completed	No L2, or L2 not from xmt line adr.	A3L2		TA611		1st L2 char-svc irpt after pgm set scope sync 2. See X65A XXXX notes 1 and 2 for reg and checks.
	0X02	Xmt of 1st PAD char (X'AA') completed	Xmt PCF not = 9, or LCD changed.	A3F2		TA811		Xmt PCF was set to 8 by pgm in hardware setup. Communication scanner hardware should have changed it to 9. Should not be in process of xmt 2nd PAD. The xmt PDF is set to an offset flag char after this error. See X65A XXXX notes.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X65A	0X03	Xmt of 2nd PAD char (X'2A') completed	No L2, or L2 not from xmt line adr.	A3L2		TA611		2nd L2 after scope sync 2. See X65A XXXX for reg and checks. After this error display, the xmt PDF is set with X'3F' flag char.
	0X04	Rcv flag char X'7E'	No L2, or L2 not from xmt line adr.	A3L2		TA611		3rd L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X05	Rcv flag char X'7E'	Rcv LCD not = 9, or PCF not = 6.	A3G2		TB021		Receiving a flag char should change PCF to 6.
	0X06	Rcv flag char	ICW bits 0-3 or 5 are in error.	A3G2		TB021		ICW bit 5 should be on; bits 0-3 should be off. Reg X'14' = ICW bits 0-15.
	0X07	Xmt of flag char (X'3F') completed	No L2, or L2 not from xmt line adr.	A3L2		TA611		4th L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X08	Rcv data char 'A0'	No L2, or L2 not from rcv line adr.	A3L2		TA611		5th L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X09	Rcv data char 'A0'	The rcv LCD was not = 9, or PCF not = 7.	A3F2		TA811		Reg X'14' contains LCD in bits 0-3 and PCF in bits 4-7.
	0X0A	Rcv data char 'A0'	The rcv data not = X'A0', or ICW bits 0-3 or 5 are in error.	A3E2 A3P2		TA311 TA121		ICW bit 1 should be on. ICW bits 0, 2, 3, and 5 should be off.
	0X0B	Xmt of data char '50' completed	No L2, or L2 not from xmt line adr.	A3L2		TA611		6th L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X0C	Rcv data char 'FE'	No L2, or L2 not from rcv line adr.	A3L2		TA611		7th L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X0D	Rcv data char 'FE'	The rcv data not = X'FE', or ICW bits 0-3 or 5 are in error.	A3E2 A3P2		TA311 TA121		See X65A XXXX for regs.
	0X0E	Xmt of data char '7F' completed	No L2, or L2 not from xmt line adr.	A3L2		TA611		8th L2. See X65A XXXX for reg and checks.
	0X0F	Rcv data char '00'	No L2, or L2 not from rcv line adr.	A3L2		TA611		9th L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X10	Rcv data char X'00'	The rcv data not = X'00', or ICW bits 0-3 or 5 are in error.	A3E2 A3P2		TA311 TA121		See X65A XXXX for regs.
	0X11	Rcv idle char	No L2, or L2 not from rcv line adr.	A3L2		TA611		10th L2 after scope sync 2.
	0X12	Rcv idle char	The rcv LCD not = 9, or PCF not = 7.	A3F2		TA811		Reg X'14' byte 0 = LCD in bits 0-3 and PCF in bits 4-7.
	0X13	Rcv idle char	ICW bits 0-3 or 5 are in error.	A3G2		TB011		ICW bit 0 should be on. ICW bits 1, 2, 3, and 5 should be off.
X65B	XXXX	DLC LCD B, A, 8 Test. The first two installed lines that will run in DLC mode will be wrapped and tested using the LCDs for 5, 6, and 7-bit char. The error stop checks to be made and the reg contents to check are as indicated in X65A XXXX. The xmt char are offset by 1 bit position to cause rcv data char to be offset by 1 data bit position from the xmt char. See notes 4 and 6 following this symptom CSB index for more info. Xmt Data - 5 bit (LCD = B): AA 2A 3F 00 0F 3F 3F Rcv Data - 5 bit (LCD = B): flag 00 1E 1E flag Xmt Data - 6 bit (LCD = A): AA 2A 3F 00 1F 3F 3F Rcv Data - 6 bit (LCD = A): flag 00 3E 3E flag Xmt Data - 7 bit (LCD = 8): AA 2A 3F 00 3F 3F 3F Rcv Data - 7 bit (LCD = 8): flag 00 7E 7E flag The rtn is run in the same sequence as that of the following error codes—first in 5-bit mode, then in 6-bit mode, and finally in 7-bit mode.							

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X65B	0X01	Xmt of 1st PAD char completed	No L2, or L2 not from xmt line adr.	A3L2		TA611		1st L2 char-svc irpt after setting scope sync 2. See X65A XXXX for reg and checks.
	0X02	Xmt of 1st PAD char completed	The xmt PCF not = 9.	A3F2		TA811		Xmt PCF was set to 8 by pgm in hardware setup. The communication scanner hardware should have changed it to 9.
	0X03	Xmt of 2nd PAD char completed	No L2, or L2 was not from xmt line adr.	A3L2		TA611		2nd L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X04	Rcv flag char	No L2, or L2 not from rcv line adr.	A3L2		TA611		3rd L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X05	Rcv flag char	Rcv LCD not = 9, or PCF not = 6 for rcv line adr.	A3G2 A3P2		TA111 TA121		See X65A XXXX for reg and checks.
	0X06	Rcv flag char	ICW bits 0-3 or 5 are in error.	A3G2		TB021		ICW bit 2 should be on (flag detect). ICW bits 0, 1, 3, and 5 should be off.
	0X07	Xmt of flag char completed	No L2, or L2 not from xmt line adr.	A3L2		TA611		4th L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X08	Rcv data char X'00'	No L2, or L2 not from rcv line adr.	A3L2		TA611		5th L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X09	Rcv data char X'00'	The LCD changed, or the PCF is not = 7.	A3F2		TA811		See X65A XXXX note 1 for reg and checks. The LCD was previously set for either 5, 6, or 7-bit mode. Reg X'16' byte 0 contains expected LCD and PCF.
	0X0A	Rcv data char X'00'	The rcv data is not = X'00', or ICW bits 0-3 or 5 are in error.	A3E2 A3P2		TA311 TA121		ICW bit 1 should be on. ICW bits 0, 2, 3, and 5 should be off. See X65A XXXX for reg and checks.
	0X0B	Xmt data char X'00' completely xmt	No L2, or L2 not from xmt line adr.	A3L2		TA611		6th L2 after scope sync 2. See X65A XXXX for reg and checks. After this error display, the PDF is set with data char X'3F', the 'disable stuffer' bit is set on, the LCD is set to 9, and the PCF is set to D. This should cause the xmt line to send constant DLC idle char without causing any more L2 irpt.
	0X0C	Rcv data char X'1E', X'3E', or X'7E'	L2 irpt did not occur, or L2 not from the rcv line adr.	A3L2		TA611		7th L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X0D	Rcv data char X'1E', X'3E', or X'7E'	The rcv data char not as expected (X'1F', X'3F', or X'7F'), or ICW bits 0-3 or 5 are in error.	A3P2 A3N2		TA111 TA511		See X65A XXXX note 1 for reg and checks. Reg X'16' = the expected ICW bits 0 through 15. ICW bit 1 should be on; bits 0, 2, 3, and 5 should be off.
	0X0E	Rcv data char X'1E', X'3E', or X'7E'	No L2, or L2 not from the rcv line adr.	A3L2		TA611		8th L2. This is the 2nd time this char is rcv. This is actually a flag char, but due to char boundary alignment on the 5, 6, or 7-bit chars, this is detected as a data char.
	0X0F	Rcv data char X'1E', X'3E', or X'7E'	Rcv PCF not = 7, or the LCD changed.	A3F2		TA811		LCD and PCF should not have changed. See X65A XXXX for reg and checks.
	0X10	Rcv data char X'1E', X'3E', or X'7E'	The rcv data char not as expected (X'1F', X'3F', or X'7F'), or ICW bits 0-3 or 5 are in error.	A3P2 A3N2		TA111 TA511		See X65A XXXX note 1 for reg and checks. Reg X'16' contains the expected ICW bits 0 through 15. ICW bit 1 should be on; bits 0, 2, 3, and 5 should be off.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X65B	0X11	Rcv flag char	L2 irpt did not occur, or L2 was not from the rcv line adr.	A3L2		TA611		9th L2 after scope sync 2. See X65A XXXX for reg and checks.
	0X12	Rcv flag char	The LCD not = 9, or PCF not = 6 for rcv line adr.	A3F2		TA811		See X65A XXXX for reg and checks.
	0X13	Rcv flag char	ICW bits 0-3 or 5 are in error.	A3G2		TB011		ICW bits 0, 1, and 3 should be off. ICW bits 2 and 5 (DLC flag detect) should be on. See X65A XXXX.
X660	XXXX	DLC data wrap in NRZI mode. X65A XXXX is valid for this rtn except for note 3. All DLC lines in this rtn are tested in 8-bit mode. Xmt data: AA For clock correction. 2A For clock correction. 3F A shifted flag char sent with the 'disable stuffer' bit on. 01 After the low order bit (a 1 bit) is sent from this char, the xmt SDF is cleared to 0's, and the NRZI bit is set in the xmt ICW by doing an output X'46' with data of X'8000'. The 'last line state' bit is also set on when the 1 bit is being xmt. From this point, all 0 bits are serialized out of the SDF; but due to the NRZI circuits, alternate data bits should be xmt. 00 See comments under the 01 character. 00 See comments under the 01 character. 00 See comments under the 01 character. Rcv data: Flag recognized from the xmt X'3F' plus the extra 1 bit. AA Alternate data bits rcv. Note that the NRZI bit is not set on for the rcv line adr. AA Alternate data bits rcv. AA Alternate data bits rcv. AA Alternate data bits rcv. AA Alternate data bits rcv. This rtn tests ability of communication scanner to xmt data in NRZI mode. The xmt and rcv char are offset to generate a predictable irpt sequence. See notes 4 and 6 following this CSB symptom index for reason for this offset.					
	0X01	Xmt of 1st char completed	No L2 character svc irpt occurred or L2 was not from the xmt line adr.	A3L2		TA611		First character svc L2 after pgm set scope sync 2. See X65A XXXX for reg and other checks.
	0X02	Xmt of 1st char completed	The xmt PCF not = 9 or LCD not = 9.	A3F2		TA811		The PCF was set to 8 by the pgm during setup and should have been changed to 9 by CS.
	0X03	Xmt of 2nd char completed	No L2 or L2 not from xmt line adr.	A3L2		TA611		2nd L2 char-svc irpt after pgm set scope sync 2. See X65A XXXX for reg and checks.
	0X04	Rcv flag char	No L2 or L2 not from rcv line adr.	A3L2		TA611		3rd L2 char-svc irpt after pgm set scope sync 2. See X65A XXXX for reg and checks.
	0X05	Rcv flag char	Rcv LCD not = 9 or PCF not = 6.	A3P2 A3F2		TA111 TA811		Reg X'14' byte 0 = LCD and PCF.
	0X06	Rcv flag char	ICW bits 0-3 or 5 are in error.	A3G2		TB011		ICW bits 2 (char overrun) and ICW bit 5 (flag detect) should be on. Bits 0, 1, and 3 should be off.
	0X07	Xmt of char X'3F' completed	No L2 irpt occurred, or L2 was not from the xmt line adr.	A3L2		TA611		4th L2 char-svc irpt after pgm set scope sync 2. See X65A XXXX for reg and checks.
	0X08	Wait for xmt or rcv line adr to cause a L2 irpt	No L2 irpt occurred from either xmt or rcv line adr.	A3L2		TA611		
	0X09	Rcv data char X'AA'	L2 irpt not from rcv line adr.	A3L2		TA611		Reg X'14' = irpt line adr.
	0X0A	Rcv data char X'AA'	Rcv LCD not = 9, or PCF not = 7.	A3P2 A3F2		TA111 TA811		Reg X'14' byte 0 = LCD and PCF.
	0X0B	Rcv data char X'AA'	Rcv data not = X'AA', or ICW bits 0-3 or 5 are in error.	A3G2 A3N2		TB021 TA511		Reg X'14' byte 1 = PDF data; byte 0 = ICW bits 0-7. ICW bit 1 should be on. ICW bits 0, 2, 3, and 5 should be off.

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Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X660	0X0C	Wait for xmt or rcv line adr to cause a L2 irpt.	No L2 irpt occurred from either xmt or rcv line adr.	A3L2		TA611		
	0X0D	Rcv data char X'AA'	The L2 irpt not from rcv line adr.	A3L2		TA611		Reg X'14' = irpt line adr.
	0X0E	Rcv data char X'AA'	Rcv LCD not = 9, or PCF not = 7.	A3P2 A3F2		TA111 TA811		Reg X'14' byte 0 = LCD and PCF.
	0X0F	Rcv data char X'AA'	Rcv data not = X'AA', or ICW bits 0-3 or 5 are in error.	A3G2 A3E2 A3P2		TB021 TA311 TA511		Reg X'14' byte 1 = PDF data; byte 0 = ICW bits 0-7. ICW bit 1 should be on. ICW bits 0, 2, 3, and 5 should be off.
	0X10	Wait for xmt or rcv line adr to cause a L2 irpt.	No L2 irpt occurred from either xmt or rcv line adr.	A3L2		TA611		
	0X11	Rcv data char X'AA'	L2 not from rcv line adr.	A3L2		TA611		Reg X'14' = irpt line adr.
	0X12	Rcv data char X'AA'	Rcv LCD not = 9, or PCF not = 7.	A3P2 A3F2		TA111 TA811		Reg X'14' byte 0 = LCD and PCF.
	0X13	Rcv data char X'AA'	Rcv data not = X'AA', or ICW bits 0-3 or 5 are in error.	A3E2 A3P2		TA511 TA121		Reg X'14' byte 1 = rcv data from PDF; byte 0 = ICW bits 0-7. ICW bit 1 should be on. ICW bits 0, 2, 3, and 5 should be off.
	0X14	Wait for xmt or rcv line adr to cause a L2 irpt.	No L2 irpt occurred from either the xmt or rcv line adr.	A3L2		TA611		
	0X15	Rcv data char X'AA'	L2 not from rcv line adr.	A3L2		TA611		Reg X'14' = irpt line adr.
	0X16	Rcv data char X'AA'	Rcv LCD not = 9, or PCF not = 7.	A3P2 A3F2		TA111 TA811		Reg X'14' byte 0 = LCD and PCF.
	0X17	Rcv data char X'AA'	Rcv data not = X'AA', or ICW bits 0-3 or 5 are in error.	A3E2 A3P2		TA511 TA121		Reg X'14' byte 1 = PDF data. ICW bit 1 should be on. ICW bits 0, 2, 3, and 5 should not be on.
	0X18	Wait for xmt or rcv line adr to cause L2 irpt.	No L2 irpt occurred from either the xmt or rcv line adr.	A3L2		TA611		See X660 XXXX for reg and checks to be made.
	0X19	Rcv data char X'AA'	L2 not from rcv line adr.	A3L2		TA611		Reg X'14' = irpt line adr.
	0X1A	Rcv data char X'AA'	Rcv data not = 9, or PCF not = 7.	A3P2 A3F2		TA111 TA811		Reg X'14' byte 0 = LCD and PCF.
	0X1B	Rcv data char X'AA'	Rcv data not = X'AA', or ICW bits 0-3 or 5 are in error.	A3G2 A3N2		TB021 TA511		Reg X'14' byte 1 = rcv data (from PDF). ICW bit 1 (svc-req) should be on. Bits 0, 2, 3, and 5 should be off.
	0X30	Xmt of data char X'00' complete.	The xmt LCD not = 9, or PCF not = 9.	A3F2		TA811		Reg X'14' byte 0 = LCD and PCF. This error is in a subrtn common to all xmt irpt after initial xmt of X'00'.
X662	XXXX	Sync monitor test – When in sync monitor state (LCD = 9, PCF = 4 or 5), the scanner is sampling for an EBCDIC SYN char, an ASCII SYN char, or a DLC flag char. This rtn tests to ensure (1) that when an EBCDIC SYN char is detected in the rcv data stream, the scanner sets the LCD to X'C' and the PCF to X'7' and (2) that when an ASCII SYN char is detected in the rcv data steam, the scanner sets the LCD to X'D' and the PCF to X'7'. The first installed line set pair that will run in DLC mode is wrapped. The set mode is done before setting the scope sync 2 as the pair of lines is wrapped. Any errors detected during set mode are pretest errors and start with error code 1XXX. These error codes are in "Common Error Stops" following this CSB symptom index.							

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X662		NOTES: **Note 1:** On all error stops in this rtn, the following reg are set up: Reg X'11' = xmt line set adr Reg X'13' = rcv line set adr Reg X'14' (for errors that indicate rcv data is bad or ICW bits 0-3 or 5 are in error) = what was obtained by an input X'44' from the rcv line ICW bits 8-15 are the PDF and contain the rcv data. ICW bits 0-7 are error and control flags and are defined as follows: ICW bit 0 = stop bit check/DLC idle detect. ICW bit 1 = svc req. ICW bit 2 = char overrun. ICW bit 3 = modem check. ICW bit 4 = rcv line signal detect; this bit is ignored in this test. ICW bit 5 = DLC flag detect/disable stuffer remember. ICW bit 6 = pgm flag; this bit is ignored in this test. ICW bit 7 = PAD flag/disable stuffer; this bit is ignored on the rcv data ICW bits 0-15 testing. Reg X'14' (for errors that indicate the LCD or PCF is bad) = the LCD in byte 0 bits 0-3, and PCF in byte 0 bits 4-7. The line is tested in 8-bit mode. The xmt char are offset from the rcv char. See notes 4 and 6 following this CSB symptom index for the reason for this offset. Xmt data AA 2A 19 19 0B 0B Rcv data 32 16					
	0X01	Xmt of 1st char X'AA' completed	No L2 char-svc irpt occurred from xmt line, or L2 irpt occurred but not from xmt line adr.	A3L2		TA611		1st L2 irpt after scope sync 2. Reg X'14' = 00 if no L2 occurred; Reg X'14' = irpt adr in error. Reg Reg X'11' = xmt line adr.
	0X02	Xmt of 1st char X'AA' completed	Xmt PCF not = 9, or LCD not = 9.	A3F2		TA811		After xmt initial, the scanner should have changed PCF to 9.
	0X03	Xmt of 2nd char X'2A' completed	No L2 char-svc irpt occurred from xmt line, or L2 irpt occurred but not from xmt line.	A3L2		TA611		2nd L2 irpt after scope sync 2. See comments for X662 0X01.
	0X04	Xmt of 1st EBCDIC SYN char X'19' completed	No L2 irpt, or L2 irpt not from xmt adr.	A3L2		TA611		3rd L2 irpt after scope sync 2. See comments for X662 0X01.
	0X05	Xmt of 1st EBCDIC SYN char X'19' completed	Xmt PCF not = 9, or LCD not = 9.	A3F2		TA811		Reg X'14' byte 0 = actual xmt LCD and PCF.
	0X06	Rcv EBCDIC SYN char X'32'	No L2 irpt from rcv line adr, or irpt occurred from wrong line adr.	A3L2		TA611		Reg X'14' = 0000 if no L2 occurred; else reg X'14' = line adr of ICW irpt in error. Reg X'13' = rcv line adr.
	0X07	Rcv EBCDIC SYN char X'32'	Rcv LCD not = C, or PCF not = 7.	A3F2		TA261		Reg X'14' byte 0 = LCD and PCF. The communication scanner hardware should change LCD to X'C' when a EBCDIC SYN char is rcv.
	0X08	Rcv EBCDIC SYN char X'32'	ICW bits 0-3 are in error, or data rcv in PDF is not = to X'32'.	A3E2 A3P2		TA511 TA121		ICW bit 1 (svc-req) should be on; and ICW bits 0, 2, and 3 should be off. See X662 XXXX note 1.
	0X09	Xmt of 2nd EBCDIC SYN char X'19' completed	No L2 irpt occurred from xmt line, or irpt occurred from wrong line adr.	A3L2		TA611		See comment for X662 0X01.
	0X0A	Xmt of 1st ASCII SYN char X'0B' completed	No L2 irpt occurred from xmt line, or irpt occurred from wrong line adr.	A3L2		TA611		See comment for X662 0X01.
	0X0B	Xmt of 1st ASCII SYN char X'0B' completed.	Xmt LCD not = 9, or PCF not = 9.	A3F2		TA811		Reg X'14' byte 0 contains actual LCD and PCF.
	0X0C	Rcv ASCII SYN char X'16'	No L2 irpt occurred from rcv line, or irpt occurred from wrong line adr.	A3L2		TA611		See comment for X662 0X06.

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Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X662	0X0D	Rcv ASCII SYN char X'16'	Rcv LCD not = D, or PCF not = 7.	A3F2		TA261		Reg X'14' byte 0 = LCD and PCF. The communication scanner hardware should change LCD to D when ASCII SYN char is rcv.
	0X0E	Rcv ASCII SYN char X'16'	Rcv line ICW bits 0-3 are in error, or the rcv data char in the PDF is not = to X'16'.	A3N2		TA511		ICW bit 1 (svc-req) should be on. ICW bits 0, 2, and 3 should be off. See X662 XXXX note 1.

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Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X666	XXXX	Stop bit error test for all S/S lines. All S/S line adr are tested to see if a stop bit check can be detected. The lines are used in pairs with one line made the rcv line. This is the line that should detect the stop bit check. The rcv line is tested with LCDs of 0, 2, 4, 5, 6, and 7. The xmt line always is set up with LCD = 7. A PAD char of X'03' is xmt, followed by the char X'02'. When the X'02' is being xmt, the pgm loops, checking xmt SDF bits 8 and 9 for 00; then the xmt SDF is set to X'180'. This should cause the xmt line to send extra bits of 0 and cause the rcv line to get a stop bit check. The sequence of operation in this rtn is: a. Reset scanner. b. Enable scanner. c. Set display bit in the rcv line's ICW. d. Set rcv line adr in rcv mode. e. Set mode on the xmt line adr. f. Set xmt line SDF = X'03' (2 bit times of PAD). g. Set xmt line PDF = X'02'. h. Set xmt PCF = 8. i. Set scope sync 2. j. Wait for L2 irpt on xmt PAD char completed. k. Wait for xmt SDF bits 8-9 = 0. l. Set xmt SDF = X'180'. m. Wait for rcv line adr char-svc L2 irpt. n. Check that 'stop bit check' bit is on in rcv line's ICW. o. Reset the 'stop bit check' bit. p. Check that the bit is reset. The above sequence is done for LCDs 0, 2, 3, 4, 6, and 7 on the rcv line adr; then the next S/S line is set up, and the whole test is run again. All lines use priority 3 and oscillator select 0. **NOTES:** **Note 1:** The following reg are set up for all errors displayed in this rtn: Reg X'11' = xmt line adr Reg X'13' = rcv line adr; the adr that should detect the stop bit errors Reg X'16' = the LCD being tested on the rcv line (in byte 1, bits 0-3) **Note 2:** On all error stops, the LCDs should be checked for LCD = F (feedback check). You can use the continue function (except for pretest errors during the set modes) to continue from the error stop to see if (1) only one line set, the whole LIB, or all S/S line sets in the scanner are failing, and (2) if the failure is for one LCD setting or all LCD settings. If only one line or one pair of lines is failing, suspect the line set card as being bad. If all lines on a LIB fail, check LIB cards and terminators. If all lines on a scanner fail or if only one LCD setting fails, suspect the scanner cards. Refer to LIB card positions in the LIB section in Volume 3 (LIBs and line sets) because card locations vary according to LIB type. Other possible failures are that oscillator 0 is failing or oscillator select is not working.							
	0X01	Xmt of PAD completed	No L2 irpt occurred.	A3L2		TA611		Reg X'11' = xmt line adr expected to cause L2 irpt. See X666 XXXX notes 1 and 2 for other reg and checks to be made.
	0X02	Xmt of PAD completed	L2 irpt not from xmt line adr.	A3L2		TA611		Reg X'11' = xmt line adr expected to cause L2 irpt. Reg X'14' = line adr that caused the L2 irpt. See X666 XXXX notes 1 and 2 for other reg and checks to be made.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X666	0X03	Shifting of xmt SDF	Xmt SDF bits 8 and 9 did not get 0's shifted into them within 200 ms.	A3L2		TA611	B-480	See X666 XXXX notes 1 and 2 for reg and checks. If this failure occurs, suggest you run rtn X650 and X652 to test diag wrap.
	0X04	Rcv char	No L2 irpt occurred.	A3L2		TA611	B-310 B-260	Reg X'13' = rcv line adr expected to cause L2 irpt. See X666 XXXX notes 1 and 2 for other reg and checks.
	0X05	Rcv char	L2 irpt not from rcv line adr.	A3L2		TA611	B-300	Reg X'13' = rcv line adr expected to cause the L2 irpt. Reg X'14' = line adr that caused the L2 irpt. See X666 XXXX notes 1 and 2 for other reg and checks.
	0X06	'Stop bit check' bit on	Stop bit check (ICW bit 0) not on.	A3P2		TA121	B-140	Stop bit check should be on in the rcv line ICW. See X666 XXXX notes 1 and 2 for reg and checks.
	0X07	'Stop bit check' bit off	Stop bit check did not reset.	A3P2		TA121	B-180	Pgm attempted to reset the stop bit check, but it did not reset. See X666 XXXX notes 1 and 2 for reg and checks.
X668	XXXX	Pad flag test for S/S lines. Check that while the PAD flag (ICW bit 7) is on and the xmt PDF = X'FF', no char are rcv. Then turn the PAD flag off and check that char can be rcv. A pair of lines are used in each run of the test, with one line being the rcv line and the other the xmt line. All S/S lines are tested with LCD = 2, priority 3, and oscillator select 0. A set mode is executed for both the rcv and the xmt lines. The rcv line is set in rcv mode, the xmt SDF is set to X'FF', the xmt PDF is set to X'05', the xmt PCF is set to X'8', and scope sync 2 is set. The rest of the test runs in the same sequence as that of the following error codes. As each test is finished, the next S/S line adr is used with the previous xmt line, and the test is run again. This continues until all installed S/S lines in the scanner under test are run in both xmt and rcv modes. NOTES: **Note 1:** The following reg are set up for error displays: Reg X'11' = xmt line (ICW) adr as used to set ABAR. Reg X'13' = rcv line (ICW) adr as used to set ABAR. Reg X'14' (for errors indicating L2 irpt is from wrong adr) = the line adr of the line that caused the L2 irpt. Reg X'14' (for unexpected rcv data in the PDF or for errors that indicate ICW bits 0-7 are in error) contains ICW bits 0-15 from the rcv line ICW obtained by an input X'44'. Reg X'16' = expected rcv lines ICW bits 0-15 for rcv data PDF errors, or ICW bits 0-7 error. The rcv ICW bits 8-15 are the PDF; byte 1 of both reg X'14' and reg X'16' should always be equal on all rcv data tests. ICW bits 0-7 are normally expected to = X'4n' in reg X'14', where *n* = 0-F ('svc req' bit on, 'rcv line signal detect' bit ignored, all other bits off). For telegraph LIBs, ICW bits 0-7 are not checked since an echo check may occur, setting modem check if no external current loop is present. **Note 2:** For all error stops, the LCDs should be examined for a feedback check: LCD = X'F'. You can use the continue function (except for set mode pretest errors) to see if only this line adr, a pair of line adr, all lines in a LIB, or all lines in the scanner are failing. If only one line or a pair of lines is failing, suspect the line set card. If all lines in a LIB are failing, suspect the LIB bit clock control card or line terminators. If all lines in the scanner fail, suspect scanner cards or first oscillator card. See LIB card positions in the LIB section in Volume 3 (LIBs and line sets) because they vary according to LIB type.							
	0X01	First PAD char completely xmt	No L2 irpt occurred. L2 irpt expected from xmt line adr.	A3L2		TA611	B-310 B-260	See X668 XXXX notes 1 and 2 for reg and checks. This should be 1st L2 irpt after scope sync 2.
	0X02	1st PAD completely xmt	L2 irpt not from xmt line adr.	A3L2		TA611	B-300	See X668 XXXX notes 1 and 2 for reg and checks. After this error display, the xmt line's PAD flag is turned on, and the PDF is set to X'FF'. X'05' is being xmt.
	0X03	Rcv 1st char of X'05'	No L2 irpt occurred. L2 irpt expected from rcv line adr.	A3L2		TA611	B-310 B-420	See X668 XXXX notes 1 and 2 for reg and checks. This should be the 2nd L2 irpt (1st from rcv line adr) after scope sync 2.
	0X04	Rcv 1st char of X'05'	L2 irpt not from rcv line adr.	A3L2		TA611	B-300	See X668 XXXX notes 1 and 2 for reg and checks.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X668	0X05	Rcv 1st char of X'05'	Rcv data in PDF not = X'05', or ICW bits 0-7 in error.	A3E2 A3P2		TA311 TA131	B-420	See X668 XXXX notes 1 and 2 for reg, ICW bits 0-7, and checks.
	0X06	Xmt of X'05' completed	No L2 irpt occurred.	A3L2		TA611	B-310 B-260	See X668 XXXX notes 1 and 2 for reg and checks. This should be 3rd L2 irpt, 2nd from xmt line adr.
	0X07	Xmt of X'05' completed	L2 irpt not from xmt line adr.	A3L2		TA611	B-300	See X668 XXXX notes 1 and 2 for reg and checks. After this error display, the xmt line's PAD flag is turned on, and the PDF is set to X'FF'. Should now be xmt the PAD char set up after X668 0X02. Rcv line should not be rcv any data bits.
	0X08	Xmt of 2nd PAD char completed	No L2 irpt occurred.	A3L2		TA611	B-310 B-260	See X668 XXXX notes 1 and 2 for reg and checks. This is the 4th L2 (3rd from xmt line adr).
	0X09	Xmt of 2nd PAD char completed	L2 irpt not from xmt line adr.	A3L2		TA611	B-300 B-420	See X668 XXXX notes 1 and 2 for reg and checks. If the L2 irpt was caused by the rcv line adr, suspect that the rcv line was rcv data instead of the PAD char that was supposed to be xmt. After this error display, the pad flag is turned off, and the xmt PDF is set to X'0E' as the next char to xmt. A PAD char should now be in the process of xmt.
	0X0A	PAD flag reset	PAD flag did not reset in xmt ICW.	A3E2		TA311	B-180	See X668 XXXX notes 1 and 2 for reg and checks.
	0X0B	Xmt of 3rd PAD char completed	No L2 irpt occurred.	A3L2		TA611	B-310 B-260	See X668 XXXX notes 1 and 2 for reg and checks. This should be the 5th L2 irpt (4th from xmt line adr).
	0X0C	Xmt of 3rd PAD char completed	L2 irpt from wrong adr. Expected a L2 from xmt line adr.	A3L2		TA611	B-300	See X668 XXXX notes 1 and 2 for reg and checks. After this error display, the xmt PAD flag is turned on, and the PDF is set to X'FF'. Should now be xmt char X'0E'.
	0X0F	Rcv char X'0E'	No L2 irpt occurred. Should have L2 irpt from rcv line adr.	A3L2		TA611	B-310 B-420	See X668 XXXX notes 1 and 2 for reg and checks. This should be the 6th L2 irpt (the 2nd from rcv line adr).
	0X10	Rcv char X'0E'	L2 irpt not from rcv line adr.	A3L2		TA611	B-300	See X668 XXXX notes 1 and 2 for reg and checks. If the L2 irpt was caused by the xmt line adr, the xmt line's ICW may have failed to recognize the reset of the PAD flag after X668 0X09.
	0X11	Rcv char X'0E'	Rcv data in PDF not X'0E', or ICW bits 0-7 in error.	A3E2 A3P2		TA311 TA131	B-420	See X668 XXXX notes 1 and 2 for reg, ICW bits 0-7, and checks.
X669	XXXX	Scanner priority test. This rtn tests that the priority between multiple scanners is correct. If L2 irpt are pending from multiple scanners at the same time, the 1st scanner should have the highest priority, the 2nd scanner the next priority, etc. In this test, the 1st ICW of each installed scanner is set up to have a L2 irpt pending by setting ICW bit 41. Then the pgm checks that the scanners irpt in the correct sequence. The test is run using priority select 3 for all tested scanners. This test is not run if only one scanner is installed. If this test detects failures, you should make sure that all previous test rtn have run on all scanners before you use this rtn to try to isolate the problem.						
	0X01	Scanner priority test	Did not get L2 irpt after all scanners were set to cause a L2 irpt.	A3L2		TA611	B-300	See X669 XXXX. Reg X'13' = line adr L2 is expected from.
	0X02	Scanner priority test. Scanner 1 has highest priority, scanner 2 next, scanner 3 next, and scanner 4 the lowest priority.	L2 irpt occurred from wrong adr. Reg X'13' = line adr expected to cause L2 irpt. Reg X'14' = line adr causing L2.	A3L2		TA611	B-300	See X669 XXXX.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X66E	XXXX	Char overrun and underrun test for S/S lines. Check that char overruns on the rcv line and char underruns on the xmt line can be detected and reset. All S/S lines are tested except for telegraph lines, which cause an echo check if no external current source is connected to the line. The echo check sets a modem check that suppresses the setting of svc req. Overrun cannot be set when the 'svc req' bit is off. A pair of S/S lines are used in each run of the test, with one line made the rcv line and one the xmt line. As each test finishes, the next S/S line is made the xmt line, and the last xmt line is made the rcv line. This continues until all S/S lines have been both a xmt and a rcv line in the scanner under test. All lines are tested with LCD = 2, priority = 3, and oscillator select = 0. A set mode is executed for the rcv line and then the xmt line. The rcv line is set in rcv mode. The xmt line's SDF is set to X'FF', PDF to X'0A', and PCF to X'8'. Scope sync 2 is set; then the rtn runs in the same sequence as that of the following error display codes. The scanner is reset and then enabled, and the above test is run on the next line. This continues until all S/S lines except telegraph lines have been tested. **NOTES:** **Note 1:** The following reg are set up for error displays: Reg X'11' = xmt line (ICW) adr as used to set ABAR. Reg X'13' = rcv line (ICW) adr as used to set ABAR. Reg X'14' (for errors indicating L2 irpt from wrong adr) contains the adr of the line that caused the L2 irpt. Reg X'14' (for unexpected rcv data in the PDF or for errors that indicate ICW bits 0-7 are in error) contains ICW bits 0-15 from the rcv line ICW obtained by an input X'44'. Reg X'16' = expected rcv line's ICW bits 0-15 for rcv data, PDF errors, or ICW bits 0-7 error. The rcv ICW bits 8-15 are the PDF. Byte 1 of both reg X'14' and reg X'16' should always be equal on all rcv data tests. ICW bits 0-7 are expected to be = to X'4n' in reg X'14' ('svc req' on, where *n* = 0-F, 'rcv line signal detect' ignored, all other bits off). The exception to ICW bits 0-7 occurs when an overrun is created. The 'svc req' bit (ICW bit 1) should be off, and char overrun bit (ICW bit 2) should be on. **Note 2:** For all error stops, the LCDs should be examined for a feedback check: LCD = X'F'. You can use the continue function (except for set mode pretest errors) to see if only this line adr, a pair of line adr, all lines in a LIB, or all lines in the scanner are failing. If only one line or a pair of lines is failing, suspect the line set card. If all lines in a LIB are failing, suspect the LIB bit clock control card or line terminators. If all lines in the scanner fail, suspect the scanner cards or first oscillator card. See LIB card positions in the LIB section in Volume 3 (LIBs and line sets) because they vary according to LIB type.						
	0X01	Completed xmt of PAD char	No L2 irpt occurred. Should have had a L2 irpt from the xmt line adr.	A3L2		TA611	B-310 B-260	See X66E XXXX notes 1 and 2 for reg and checks. This should be the 1st L2 irpt after pgm set scope sync 2.
	0X02	Completed xmt of PAD char	L2 irpt not from xmt line adr.	A3L2		TA611	B-300	See X66E XXXX notes 1 and 2 for reg and checks.
	0X03	Completed xmt of PAD char	Xmt line PCF did not change to 9.	A3F2		TA811	B-080	See X66E XXXX notes 1 and 2 for reg and checks. Pgm sets xmt PCF = 8 during hardware setup. Hardware should have changed the PCF to 9 as 1st char is xmt. After this error display, the xmt PDF is set to X'01' as the next char to be xmt. Should now be in process of xmt char X'0A'.
	0X04	Rcv char X'0A'	No L2 irpt occurred.	A3L2		TA611	B-490	See X66E XXXX notes 1 and 2 for reg and checks. This should be the 2nd L2 irpt (1st from rcv line adr).
	0X05	Rcv char X'0A'	L2 irpt not from rcv line adr.	A3L2		TA611	B-300	See X66E XXXX notes 1 and 2 for reg and checks.
	0X06	Rcv char X'0A'	Rcv data in PDF not = X'0A', or ICW bits 0-7 in error.	A3E2 A3P2		TA311 TA131	B-490	See X66E XXXX notes 1 and 2 for reg and checks. 'Svc-req' bit is not reset after this error display, so next rcv char should cause a char overrun.
	0X07	Completed xmt of X'0A'	No L2 irpt occurred. Should have had a L2 irpt from xmt line adr.	A3L2		TA611	B-310 B-260	See X66E XXXX notes 1 and 2 for reg and checks. This should be the 3rd L2 irpt (2nd from xmt line adr).

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X66E	0X08	Completed xmt of X'0A'	L2 irpt not from xmt line adr.	A3L2		TA611	B-300	See X66E XXXX notes 1 and 2 for reg and checks. After this error display, the xmt PDF is set to X'0E' as the next char to be xmt. 'Svc-req' bit is not reset, so the next xmt L2 irpt should set the char underrun bit. Should now be in the process of xmt the char X'01'.
	0X09	Rcv char X'01' and get char overrun	No L2 irpt occurred. Should have a L2 irpt from rcv line adr.	A3L2		TA611	B-490	See X66E XXXX notes 1 and 2 for reg and checks. This should be 4th L2 (2nd from rcv line adr). Check reg X'44'; ICW bit 2 (char overrun bit) should be on in rcv line, ICW bit 1 (svc req) should be off, and PDF should contain X'01'. If you display reg X'40', store the rcv line adr and display reg X'44' (ICW bits 0-15), the PDF should now = X'0E', since the xmt line is still sending char X'0E'. The rcv line should be rcv the char and setting overrun.
	0X0A	Rcv char X'01' and get char overrun	L2 irpt not from rcv line adr.	A3L2		TA611	B-300	See comments on X66E 0X09.
	0X0B	Rcv char X'01' and get char overrun	Char overrun (ICW bit 2) not on, svc req (ICW bit 1) is on, or PDF (ICW bits 8-15) not = X'01'.	A3P2		TA611	B-490 B-140	Rec ICW bit 2 should be on. See X66E 0X09. Reg X'14' = the rcv ICW bits 0-15 obtained by an input X'44'.
	0X0C	Reset of ICW bit 2	ICW bit 2 (char overrun) did not reset.	A3P2		TA611	B-180	See X66E XXXX notes 1 and 2 for reg and checks.
	0X0D	Xmt of X'01' completed and xmt underrun	No L2 irpt occurred. Should have had a L2 irpt from xmt line adr.	A3L2		TA611	B-310 B-260	See X66E XXXX notes 1 and 2 for reg and checks. This should be 5th L2 irpt (3rd from xmt line adr).
	0X0E	Xmt of X'01' completed and xmt underrun	L2 irpt not from xmt line adr.	A3L2		TA611	B-300	See X66E XXXX notes 1 and 2 for reg and checks.
	0X0F	Xmt underrun	Underrun (ICW bit 2) not on in xmt line's ICW (Should be on).	A3P2		TA121	B-310 B-140	See X66E XXXX notes 1 and 2 for reg and checks. After X66E 0X08 on last xmt char-svc L2, the 'svc req' bit was not reset, so when this xmt L2 irpt occurred, the char underrun bit should have been set on by hardware.
	0X10	Reset of xmt underrun	Underrun bit (ICW bit 2) did not reset in xmt line's ICW.	A3P2		TA121	B-180	
X672	XXXX	Char overrun and underrun test for sync lines. All sync lines are checked to ensure that char overrun can be detected on rcv lines and char underrun can be detected on xmt lines. All lines are tested with LCD = C, priority = 3, and oscillator select = 0. Each pair of lines is set up by (1) setting the display bit in the rcv line, (2) executing set mode on the rcv line, (3) setting the rcv line PCF = 5, (4) executing set mode on the xmt line, (5) setting xmt SDF and PDF to X'55', (6) setting xmt PCF = 8, and (7) setting scope sync 2. The rest of the test is run in the same sequence as that of the error codes that follow. When the test is finished on a pair of lines, the scanner is disabled and then enabled. The next sync line adr is made the new xmt line, the last xmt line is made the new rcv line, and the whole test is run again. This is continued until all sync lines have been tested both as xmt and rcv lines.							

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X672	XXXX	NOTES: **Note 1:** The following reg are set up for error displays: Reg X'11' = xmt line (ICW) adr as used to set ABAR. Reg X'13' = rcv line (ICW) adr as used to set ABAR. Reg X'14' (for errors indicating L2 irpt from wrong adr) contains the adr of the line that caused the L2 irpt. Reg X'14' (for unexpected rcv data in the PDF or for errors that indicate that ICW bits 0-7 are in error) contains ICW bits 0-15 from the rcv line ICW obtained by an input X'44'. Reg X'16' = expected rcv line's ICW bits 0-15 for rcv data, PDF errors, or ICW bits 0-7 error. The rcv ICW bits 8-15 are the PDF. Byte 1 of both reg X'14' and reg X'16' should always be equal on all rcv data tests. ICW bits 0-7 are expected to be: bit 1 (svc-req) on; bits 0, 2, 3, 5, 6, and 7 off; bit 4 ignored. The exception to ICW bits 0-7 being as above is when an overrun is created. The 'svc req' bit (ICW bit 1) should be off, and char overrun bit (ICW bit 2) should be on. **Note 2:** For all error stops, the LCDs should be examined for a feedback check: LCD = X'F'. You can use the continue function (except for set mode pretest errors) to see if only this line adr, a pair of line adr, all lines in a LIB, or all lines in the scanner are failing. If only one line or a pair of lines is failing, suspect the line set card. If all lines in a LIB are failing, suspect the LIB bit clock control card or line terminators. If all lines in the scanner fail, suspect the scanner cards or first oscillator card. See LIB card positions in the LIB section in Volume 3 (LIBs and line sets) because they vary according to LIB type. **Note 3:** See note 6 following this CSB symptom index for the shifted SYN and data char.						
	0X01	Xmt 1st PAD (X'55') completed	No L2 irpt occurred.	A3L2		TA611		See X672 XXXX notes 1 and 2 for reg and checks. 1st L2 (from xmt) after scope sync 2.
	0X02	Xmt 1st PAD (X'55') completed	L2 not from xmt line adr.	A3L2		TA611		See X672 XXXX for reg and checks.
	0X03	Xmt PCF went to 9.	Xmt PCF did not go to 9.	A3F2		TA811		See X672 XXXX for reg and checks. Pgm set PCF = 8 in hardware setup, and hardware should have changed the PCF to 9. After this error display, the xmt PDF is set to X'19' (shifted SYN char), and svc req is reset.
	0X04	Xmt 2nd PAD (X'55') completed	No L2 irpt occurred.	A3L2		TA611		See X672 XXXX for reg and checks. 2nd L2 (2nd from xmt) after scope sync 2.
	0X05	Xmt 2nd PAD (X'55') completed	L2 not from xmt line adr.	A3L2		TA611		See X672 XXXX notes 1 and 2 for reg and checks. After this error display, the xmt PDF is set with the 2nd shifted SYN char (X'19'), and svc req is reset. Should now be in process of xmt the 1st SYN char.
	0X06	Xmt 1st SYN (X'19') completed	No L2 irpt occurred.	A3L2		TA611		See X672 XXXX for reg and checks. 3rd L2 (3rd from xmt).
	0X07	Xmt 1st SYN (X'19') completed	L2 not from xmt line adr.	A3L2		TA611		See X672 XXXX notes 1 and 2 for reg and checks. After this error display, the xmt lines PDF is set to character X'50' and svc request is reset. Should now be in process of xmt the 2nd SYN char.
	0X08	Rcv line detected 1st SYN	Rcv line's PCF not = 7.	A3F2		TA811	B-080	The rcv adr PCF was set to 5 by the pgm during hardware setup, but the 1st SYN char should have been rcv and detected by the hardware and caused the PCF to be changed to 7. **Note:** No L2 irpt should result from changing PCF = 5 to PCF = 7. See X672 XXXX notes 1 and 2 for reg and checks.
	0X09	Rcv line rcv 2nd SYN	No L2 irpt occurred.	A3L2		TA611	B-310 B-420	See X672 XXXX for reg and checks. 4th L2 irpt (1st from rcv).
	0X0A	Rcv line rcv 2nd SYN	L2 irpt not from rcv line adr.	A3L2		TA611	B-300	See X672 XXXX for reg and checks.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X672	0X0B	Rcv line rcv 2nd SYN.	Rcv data in rcv line PDF not a SYN char (X'32'), or ICW bits 0-7 in error.	A3E2 A3P2		TA311 TA131	B-240	See X672 XXXX notes 1 and 2 for reg, ICW bits 0-7, and checks to make. 'Svc-req' bit is not set off in the rcv line ICW, so the next rcv line L2 irpt should indicate char overrun.
	0X0C	Xmt of 2nd SYN completed	No L2 irpt occurred.	A3L2		TA611	B-310 B-260	See X672 XXXX for reg and checks. 5th L2 irpt (4th from xmt).
	0X0D	Xmt of 2nd SYN completed	L2 irpt not from xmt line adr.	A3L2		TA611	B-300	See X672 XXXX for reg and checks. After this error display, the xmt line's PDF is set to X'00'. The 'svc req' bit is not reset. On the next L2 irpt for the xmt line adr, a char underrun error should be indicated. Should now be in the process of xmt the char X'50'.
	0X0E	Rcv char X'A0' and get char overrun.	No L2 irpt occurred.	A3L2		TA611	B-310 B-420	See X672 XXXX for reg and checks. Reg X'44' contains the rcv line's ICW bits 0-15. ICW bits 8-15 are the PDF and should = X'A0'. ICW bit 2 (char overrun) should be on since svc req (ICW bit 1) was not reset on the last rcv line L2 irpt. ICW bit 1 (svc req) should be off, since hardware should turn it off when it turns on ICW bit 2. This is the 6th L2 irpt (2nd from rcv).
	0X0F	Rcv char X'A0' and get char overrun.	L2 irpt not from rcv line adr.	A3L2		TA611	B-300	See X672 XXXX notes 1 and 2 for reg and checks. Reg X'44' contains the rcv line's ICW bits 0-15. ICW bits 8-15 are the PDF and should = X'A0'. ICW bit 2 (char overrun) should be on since svc req (ICW bit 1) was not reset on the last rcv line L2 irpt. ICW bit 1 (svc req) should be off, since hardware should turn it off when it turns on ICW bit 2.
	0X10	Rcv char X'A0' and get char overrun.	Char overrun (ICW bit 2) is not on, svc req (ICW bit 1) is on, or PDF not = X'A0' in rcv line's ICW.	A3P2		TA121	B-420 B-140	See comments under X672 0X0F.
	0X11	Char overrun reset	Char overrun (ICW bit 2) did not reset.	A3P2		TA121	B-180	Pgm attempted to reset char overrun and then checked to make sure it was off. See X672 XXXX notes 1 and 2 for reg and checks.
	0X12	Xmt of X'50' complete and char underrun	No L2 irpt occurred.	A3L2		TA611		See X672 XXXX notes 1 and 2 for reg and checks. Should have xmt line's ICW bit 2 on (underrun), since the 'svc req' bit was not reset on the last xmt L2 irpt. 7th L2 (5th from xmt).
	0X13	Xmt of X'50' completed and char underrun	L2 not from xmt line adr.	A3L2		TA611		See X672 XXXX notes 1 and 2 for reg and checks. The xmt line's ICW should have the 'char underrun' bit on (ICW bit 2), since the 'svc req' bit was not reset on the last xmt L2 irpt.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X672	0X14	Xmt of X'50' completed and char underrun	The 'char underrun' bit (ICW bit 2) is not on but should be.	A3P2		TA121		See X672 XXXX notes 1 and 2 for reg and checks. The xmt line's ICW should have the 'char underrun' bit on (ICW bit 1), since the 'svc req' bit was not reset on the last xmt L2 irpt.
	0X15	Reset underrun	The char underrun bit did not reset.	A3P2		TA121	B-180	See X672 XXXX notes 1 and 2 for reg and checks. The pgm attempted to reset the char underrun bit in the xmt ICW and then checked and found the bit was still on.
X675	XXXX	Force L1 check test. Checks that an output X'43' with byte 0 bit 0 and byte 1 bit 5 on forces the check bits on in the scanner check reg (input X'43'). Then checks that an output X'43' with byte 0 bit 1 and byte 1 bit 5 on resets the check bits. The scanner is disabled ('CSB disable' latch is set) and then enabled ('CSB disable' latch turned off). ABAR is set with an output X'40', scope sync 2 is set, and an output X'43' is done with byte 0 bit 0 and byte 1 bit 5 on. The rest of the test is run in the same sequence as that of the following error codes.						
	0X01	Scanner check reg bits on	All check bits not on.	A3C2		TB131	B-170 B-130	Reg X'14' = the scanner check reg bits obtained by an input X'43'. Byte 0 bit 0-7 and byte 1 bits 0-3 should all be on. **Note:** L1 adapter checks were masked off so the normal L1 adapter check that should occur is blocked at this time. Reg X'11' = line adr of scanner under test as used to set ABAR. After this error display, ABAR is set again and another output X'43' is executed with byte 0 bit 1 and byte 1 bit 5 on to reset the scanner check reg bits.
	0X02	Scanner check reg reset	All check bits not reset.	A3C2		TB131	B-140 B-130	All scanner check reg bits should be reset. Reg X'14' contains the scanner check reg obtained by an input X'43'. Reg X'11' = line adr of scanner under test set in ABAR. After this error display, output X'43' is executed again to set the scanner check reg bits on. Then adapter L1 irpt are unmasked, and a check is made that a L1 actually occurred.
	0X03	Scanner check reg causes L1 irpt.	No L1 irpt occurred.	A3C2		TB131	B-130	A L1 irpt should have occurred for scanner under test. Reg X'11' = line adr set in ABAR.
	0X04	Scanner under test caused the L1 irpt.	The scanner under test was not the scanner that caused the L1 irpt.	A3C2		TB131	B-300	Reg X'14' = line adr causing the L1 irpt. Reg X'11' = line adr of scanner under test.
X678	XXXX	Modem error bit test. This rtn tests that the modem error bit (ICW bit 3) is set according to the modem intf lines of data set ready (DSR) and/or clear to send (CTS). Only one error stop can occur in this rtn, with reg X'15' indicating the failure. If reg X'15' = 0001, the error is that the modem check bit did not come on with DSR off and a PCF of 5, 7, 8, 9, A, B, C, or D. If reg X'15' = 0002, the error is that the modem error bit is not on with CTS off and a PCF of 9, A, B, or D. Reg X'13' contains the contents of the display reg obtained by an input X'46', with bit 0.0 being CTS and 0.2 = DSR. Reg X'11' contains line (ICW) adr of line under test. Reg X'14' contains ICW bits 0-15, with bit 0.3 being the 'modem check' bit. Reg X'45' contains LCD and PCF, with bits 0.4 – 0.7 being PCF now in ICW. Reg X'16' bits 1.0 – 1.3 = LCD in use, and bits 1.4 – 1.7 = PCF that was used. PCF now in ICW may be different than PCF that was used, and this may be normal. Example: if PCF was set to D with an LCD of C, then the PCF would change to 5.						
	0X01	Modem error bit	Modem error bit (ICW bit 3) is at wrong value.	A3P2		TA131	B-140	Reg defined in X678 XXXX.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X67A	XXXX	Oscillator speed test. Each installed oscillator in the scanner under test is checked. The oscillator frequency is checked to ensure that there is no more than a plus or minus 0.25 percent variation from its expected frequency. The first installed line in the scanner is used to run the test. The test: 1. Resets and then enables the scanner. 2. Sets up the best possible upper scan limit for the line being used for the test. 3. Sets priority = 3. 4. Sets the 'display req' bit so reg X'46' will be valid for the line in use. 5. Executes set mode with oscillator select 0 to ensure the line operates. (Pretest errors are indicated if set mode fails.) 6. Sets scope sync 2. 7. Executes a set mode with oscillator select bits for the oscillator position under test. 8. Masks off L1, L2, and L3 irpt. 9. Sets PDF to X'55' and the SDF to X'1D5'. 10. Sets PCF = 8 (xmt initial). 11. Loops until SDF bit 3 = 0 (the 1st 3 bit times are not included in the speed test because the 1st 3 bit times are unpredictable. Examples: the 1st bit svc is caused by the rcv clock because xmt state is not active yet. Also when xmt state is set, it may cause an extra strobe pulse if the oscillator is in a negative state at this time). 12. Reports an error if the SDF did not shift 3 times to set SDF bit 3 to 0 within 180 ms. 13. Sets SDF = X'54'. 14. Loops for 1 second plus enough time to round bits-per-second count to a whole number, counts the number of bits that occur while in the loop, saves the loop count when and if the number of bits to be counted is actually counted, and alternately sets the SDF to X'54' and X'55' after each bit time to cause the 'test data' latch (xmt data) to have alternate bits for a possible trouble-shooting aid. 15. Calculates, from the number of bits counted, the loop count and the tolerance to determine whether the oscillator is running at the correct frequency. 16. Reports an error if the detected frequency is not within tolerance. The above is done for each of the 4 possible oscillators if the CDS entry for that oscillator position contains a valid oscillator type. **Notes:** This rtn is dependent on the proper operation of the first installed line since the rtn is designed to test the oscillators rather than the line sets. Also the oscillator type fields in the configuration data set (CDS) must be right. If this rtn fails, the oscillator card for the oscillator under test could be bad, the oscillator select bits could be bad, or the gating controls for the oscillators could be bad. Another possible failure is getting extra or missing strobe pulses not caused by the oscillator. The following reg are set up for all rtn error displays except the set mode pretest errors beginning with 1: Reg X'11' = line adr of line used in test (adr as used to set ABAR). Reg X'14' = number of bits counted during the test. Reg X'15' = relative oscillator position under test in byte 0 bits 0-7 with X'0' being 1st oscillator, 1 being 2nd oscillator, 2 being 3rd oscillator, and 3 being the 4th oscillator. Reg X'15' = oscillator type in byte 1 bits 0-7. This type is as obtained from the CDS. Reg X'16' = number of bits per second expected to be counted (rounded off to a whole number).						
	0X01	Set mode with oscillator under test	No L2 irpt occurred.	A3L2 A3T2 A3T4 A3U2 A3U4 B3U5		TA611 TB411 TB412 TB413 TB414 CC007	C-020 C-160	See X67A XXXX notes for reg and checks.
	0X02	SDF shifting	SDF bit 3 did not set to 0 in the 180 ms wait time.	A3L2 A3T2 A3T4 A3U2 A3U4 B3U5		TA611 TB411 TB412 TB413 TB414 CC007	C-020 B-480 B-410	SDF bits 1, 2, and 3 were set by an output X'46' with X'01D5'. The SDF should have been shifted right, setting SDF bit 3 to a 0. See X67A XXXX notes for reg and checks.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X67A	0X03	Oscillator frequency	Oscillator under test running too fast.	A3L2 A3T2 A3T4 A3U2 A3U4 B3U5		TA611 TB411 TB412 TB413 TB414 CC007	C-020 C-040	Reg X'14' contains the number of bits actually counted. Reg X'16' contains the number of bits expected to be counted. If reg X'14' = reg X'16', the oscillator is getting less than 1 bit time extra in the 1 second run but is still too fast (not within 0.25 percent of expected frequency). See X67A XXXX notes for other reg and checks to be made.
	0X04	Oscillator frequency	Oscillator under test running too slowly. Not enough bits counted in 1 second.	A3L2 A3T2 A3T4 A3U2 A3U4 B3U5		TA611 TB411 TB412 TB413 TB414 CC007	C-020 C-040	Reg X'14' contains the number of bits actually counted and is less than reg X'16', which contains number of bits expected to be counted. See X67A XXXX notes for other reg and checks to make.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X694	XXXX	PCF state F disable test. This rtn, which is a manual intervention rtn, will not be run unless you set the CE sense switch to run manual intervention rtn or unless you requested a single rtn to be run. This rtn will stop with manual intervention codes of F0 in DISPLAY B, asking you to enter the info required to run this rtn. These F0-codes may be found following this CSB symptom index. This test rtn does a PCF = F switch line intf disable to the line(s) you entered. The rtn: 1. Disables ('CSB disabled' latch turned on) and then enables the scanner under test. 2. Sets the display request bit in the line (ICW) under test. 3. Sets scope sync 2. 4. Sets the diag mode bit and, if the line is only sync, sets the sync clock bit in the SDF. 5. Sets PCF = 1 and LCD = 7 for S/S lines, or LCD = C for sync lines. 6. Waits for and validates that a L2 irpt occurred for the line under test. 7. Checks that the PCF went from 1 to 0. (Set mode completed okay.) 8. Sets PCF = F. 9. Waits for and validates that a L2 irpt occurred for the line under test. 10. Checks that the PCF went to 0. 11. Checks that the scanner display reg (X'46') byte 0 bits 0, 1, 2, 3, and 5 are all off which indicates the line intf has been reset. **Notes:** This rtn indicates failures on any line intf that has modem intf lines, 'ring indicator', or 'rcv line signal detect' tied up to active levels. For some modems, data sets, and line set types, it is normal for some of these intf lines to be tied up to an active (on) level. If you requested all lines to be run, this rtn will bypass LIB types 2, 3, and 4 since they always have some intf line active. If the test indicates failures due to modem intf lines being on when they should not be, you could have a bad intf converter on the line set for the line that failed, or there could be a bad modem or data set connected to the line. If none of the lines completed the PCF = F portion of the test, the scanner cards may be bad. It is assumed that the other internal test rtn have been run and that set modes and internal data wraps work properly. If this is not true, there could be a bad oscillator, a bad line set, a bad LIB, or some scanner failure. The following reg are valid for all error displays in this rtn: Reg X'11' = line adr that is under test (as used to set ABAR) Reg X'46' = the scanner display reg for the line under test.						
	0X01	Set mode	No L2 irpt occurred.	A3E2		TA331	B-310 B-260	This error should not occur if rtn X627 and X629 ran successfully. Suggest you run those rtn again. Should have had a L2 irpt from the set mode, and PCF should now = 0. See X694 XXXX notes for reg and more info.
	0X02	Set mode	L2 irpt not from the line under test.	A3E2		TA331	B-300	This error should not occur if rtn X627 and X629 ran successfully. Suggest you run those rtn again. Should have had a L2 irpt from the set mode, and PCF should now = 0. See X694 XXXX notes for reg and more info. Reg X'14' = line adr that caused the L2 irpt.
	0X03	Set mode	PCF did not go to 0 after set mode.	A3E2		TA331	B-080	See comments in X694 0X01. Reg X'14' byte 0 = LCD and PCF obtained by an input X'45' at the time of failure.
	0X04	PCF = F completed	No L2 irpt occurred after PCF was set to F.	A3F2		TA811	B-310	No L2 irpt will occur if some modem intf lines did not reset. See X694 XXXX notes for reg and more info.
	0X05	PCF = F completed	L2 irpt from the line under test.	A3E2		TA331	B-300	This error may have nothing to do with the PCF = F test, since no other line should cause a L2. See X694 XXXX notes for reg and more info. Reg X'14' contains the line adr that caused the L2 irpt.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X694	0X06	PCF = F completed	PCF did not change to 0.	A3F2		TA811	B-080 B-260	Hardware should have changed PCF to 0 from PCF = F after the modem interface is reset. If 'DSR' and 'rcv line signal detect' intf lines did not reset properly, PCF may still = F. See X694 XXXX notes for more info.
	0X07	Modem intf reset	All modem intf lines that should be reset are not reset.	A3E2		TA331	B-150	Reg X'14' = reg X'46' at the time of failure. **Note:** Reg X'46' is loaded every scan cycle, so it may not be = to reg X'14' at this time. Reg X'15' has a bit on for each bit position that is bad in reg X'14'. See X694 XXXX notes for more info.
X698	XXXX	Diag xmt test for PCF = B. This rtn, which is a manual intervention rtn, will not be run unless you set the CE sense switch to run manual intervention rtn or unless you request a single rtn to be run. This rtn will stop with manual intervention codes of F0 in DISPLAY B, asking you to enter the info required to run this rtn. These F0 codes can be found following this CSB symptom index. This rtn xmt a PAD char (X'FF') and 2 data char (X'AA'). The rtn sets PCF = B to xmt the second data char; then the scanner sets PCF = C and checks that the xmt line turned around. This is a manual intervention rtn because PCF = C turnaround requires the 'CTS' modem intf line to drop; this does not occur on some modem intf that have this line tied up to an active (on) level. This rtn runs on S/S lines only and uses LCD = 7. **Note:** This rtn indicates a failure on any line intf that does not drop the 'CTS' modem intf line. If 'CTS' should not be on for this intf, you should suspect the line set card for the failing line. If all lines fail, there may be a bad scanner card. Errors X698 0X01 through 0X05 should not occur; if they do, you should run rtn X645 to try to find the failure. The following reg are set up for all error displays: Reg X'11' = line adr of line under test (as used to set ABAR). Reg X'46' = scanner display reg, which is valid for the line under test. Reg X'14' = line that caused the L2 irpt for errors in which the L2 irpt is not from the line under test.					
	0X01	Xmt of PAD completed	No L2 irpt occurred.	A3L2		TA611	B-310 B-260	
	0X02	Xmt of PAD completed	L2 irpt not from the line under test.	A3L2		TA611	B-300	
	0X03	Xmt of PAD completed	PCF did not go to 9.	A3F2		TA811	B-080	PCF set to 8 by pgm for xmt initial. The scanner hardware should have changed it to 9. See the X698 XXXX note.
	0X04	Xmt of 1st data (X'AA') completed	No L2 irpt occurred.	A3L2		TA611	B-310 B-260	
	0X05	Xmt of 1st data (X'AA') completed	L2 irpt not from the line under test.	A3L2		TA611	B-300	See the X698 XXXX note. After this error display, the PCF is set to B.
	0X06	Xmt of 2nd data (X'AA') completed	No L2 irpt occurred.	A3L2		TA611	B-080 B-310 B-260	If 'CTS' did not drop, this irpt will not occur. PCF should have been changed to C if the last data char was xmt okay. See the X698 XXXX note for more info.
	0X07	Xmt of 2nd data (X'AA') completed	L2 irpt not from the line under test.	A3L2		TA611	B-300	
	0X08	PCF went to 7.	PCF did not set to 7 after xmt turn-around.	A3F2		TA811	B-080	PCF was changed to C by the hardware, and an additional bit time should occur. If 'CTS' is off, PCF should be changed to 7 by the scanner hardware. See the X698 XXXX note for more info.
	0X09	SDF = 0	SDF bits 0-7 did not = 0.	A3H2		TA221	B-480	Turnaround should leave SDF = 0. See the X698 XXXX note for more info.
	0X0A	SDF = 0	SDF bits 8-9 did not = 0.	A3H2		TA221	B-480	Turnaround should leave SDF = 0. See the X698 XXXX note for more info.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X699	XXXX	Diag xmt test for PCF = C. This rtn, which is a manual intervention rtn, will not be run unless you set the CE sense switch to run manual intervention rtn or unless you request a single rtn to be run. This rtn will stop with manual intervention codes of F0 in DISPLAY B, asking you to enter the info required to run this rtn. These F0 codes can be found following this CSB symptom index. This rtn xmt a PAD char (X'FF') and 2 data char (X'AA'). The rtn xmt the second data character, then sets PCF = C and checks that the xmt line turned around. This is a manual intervention rtn because PCF = C turnaround requires the 'CTS' modem intf line to drop; this does not occur on some modem intf that have this line tied up to an active (on) level. This rtn runs on DLC lines only and uses LCD = 9. **Note:** This rtn indicates a failure on any line intf that does not drop the 'CTS' modem intf line. If 'CTS' should not be on for this intf, you should suspect the line set card for the failing line. If all lines fail, there may be a bad scanner card. Errors X699 0X01 through 0X05 should not occur; if they do, you should run rtn X645 to try to find the failure. The following reg are set up for all error displays: Reg X'11' = line adr of line under test (as used to set ABAR). Reg X'46' = scanner display reg, which is valid for the line under test. Reg X'14' = line that caused the L2 irpt for errors in which the L2 irpt is not from the line under test.						
	0X01	Xmt of 1st data (X'AA') completed	No L2 irpt occurred.	A3L2		TA611	B-310 B-260	See the X699 XXXX note.
	0X02	Xmt of 1st data (X'AA') completed	L2 irpt not from the line under test.	A3L2		TA611	B-300	See the X699 XXXX note.
	0X03	Xmt of 1st data (X'AA') completed	PCF did not go to 9.	A3F2		TA811	B-080	PCF was set to 8 by pgm for xmt initial. The scanner hardware should have changed it to 9. See the X699 XXXX note.
	0X04	Xmt of 2nd data (X'AA') completed	No L2 irpt occurred.	A3L2		TA611	B-310 B-260	See the X699 XXXX note.
	0X05	Xmt of 2nd data (X'AA') completed	L2 irpt not from the line under test.	A3L2		TA611	B-300	See the X699 XXXX note. After this error display, the PCF is set to B.
	0X06	Xmt turn completed	No L2 irpt occurred.	A3L2		TA611	B-080 B-310 B-260	If 'CTS' did not drop, this irpt will not occur. PCF should have changed to 5 if the last data char was xmt okay. See the X699 XXXX note for more info.
	0X07	Xmt turn completed	L2 irpt not from the line under test.	A3L2		TA611	B-300	See the X699 XXXX note.
	0X08	PCF went to 5.	PCF did not set to 5 after xmt turnaround.	A3F2		TA811	B-080	After PCF was set to C, an additional bit time should occur. If CTS is off, PCF should be changed to 5 by the scanner hardware. See the X699 XXXX note for more info.
X69C	XXXX	Modem intf check. This rtn, which is a manual intervention rtn, will not run unless you set the CE sense switch to run manual intervention rtn or unless you request a single rtn to be run. This rtn stops with manual intervention codes of F0 in DISPLAY B, asking you to enter the info required to run this rtn. These F0 codes can be found following this 'CSB' symptom index. This rtn checks that the modem intf line's 'CTS' and 'rcv line signal detect' are not on and that the 'rcv data bit buffer' is on. This test is run with 'RTS' off and 'diag wrap mode' off. **Note:** This rtn will indicate failures on all modem intf and/or line sets that have 'CTS' and 'rcv line signal detect' ties up to active (on) levels. For example, all LIB type 2 telegraph line sets should have 'rcv line signal detect' active all the time and should cause failures. If failures occur and the intf line in error should not have lines tied to active levels, suspect a bad line set card or a modem intf problem. The following reg are set up for error displays: Reg X'11' = line adr (as used to set ABAR) of the line under test. Reg X'46' = the scanner display reg, which should be loaded by the scanner every scan cycle for the line under test. Reg X'14' = what was in the display reg X'46' at the time the failure was detected. Reg X'14' may not = reg X'46' if you display reg X'46', because reg X'46' may be changed on each scan cycle. Reg X'15' contains bits in error, with each bit position that is on representing the bit position in reg X'14' that is in error.						
	0X01	Modem intf	Intf lines not in expected condition.				B-150	Reg X'14' byte 0 bit 0 is the 'CTS' bit, which should be off; bit 3 is the 'rcv line signal detect' bit, which should be off; bit 4 is the 'rcv data bit buffer' bit, which should be on.

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Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X6F0	XXXX	SDLC link test. This rtn, which is a manual intervention rtn, will not be run unless you set the CE sense switch to run manual intervention rtn or unless you request a single rtn to be run. This rtn will stop with manual intervention stop code F020 through F02C, asking you to enter options needed to run this rtn. These stop code definitions are listed in "Manual Intervention" following this CSB symptom index. This rtn may be used for SDLC data link problem determination and repair verification when on-line tests (under host system control) are not available. This SDLC link test is basically an echo test, with the primary SDLC station sending an SDLC Link Test command frame down the link. The primary station expects to get the same test frame back if the remote end of the link rcv the test frame without errors. Some SDLC terminals respond only with a nonsequenced acknowledgment response rather than sending back the link test frame it rcv. Options are provided to run as an SDLC primary station or as an SDLC secondary station. The primary station option initiates the Link Test commands and expects to rcv responses. The secondary SDLC station responds to test frames rcv; if the test frame was rcv without errors, the same test frame is sent back as a response. If a test frame was rcv without block check errors and had either more data than could be buffered or did not have the poll bit on in the control field, the secondary station responds with a test frame without optional data. All frames rcv with block check errors or with abort detect conditions are counted as errors, and no response is provided. All frames rcv with an SDLC station adr other than the SDLC station adr selected in the F028 manual intervention stop code are counted as an unexpected or nonsupported frame, and no response is provided. No response is provided for frames with anything but a Link Test command field. The structure of the Link Test command enables this test to also run a local external duplex modem wrap if you select the primary station option and connect the xmt and rcv lines together properly. A remote wrap can be done if the remote end of the link can tie the xmt and rcv duplex lines together with proper loading, etc. Because the remote end of the link must store the test frame and send it back, the wrap option does not work on half-duplex lines. This rtn always stops on xmt errors such as modem check, time-out, or overrun; but it does not stop on rcv errors except for modem check errors unless an option is selected to stop on frames in error or stop on any frame. Continuation (select FUNCTION 5 and press START pushbutton) from the X6F0 0X20, 0X60, or 0X61 error codes stops the rtn, clears all error counts and summary statistics, and restarts the test from the xmt/rcv data portions. This allows continuing the test on a manual switched-line connection without making a new connection. The same restart is used for the D000 dynamic restart option or the D000 restart option at manual intervention stop code F02C. Any manual switched-line connection will not be broken until you abort the rtn or use a restart option that goes through total hardware setup such as the D002 restart code. The format of all transmissions from this SDLC link test are: PAD PAD F A C dd FC FC F ee where: PAD = alternate data xmt char for clock correction; will be X'AA' if NRZI mode is not being used or X'00' if NRZI mode is being used. F = SDLC flag char composed of a 0 bit, followed by six 1 bits and another 0 bit (X'7E'). A = SDLC station adr. C = SDLC control field; will always be X'F3' if a Link Test command/response is being sent, or X'97' if a frame reject response is being sent. dd = optional xmt/rcv data field when the Link Test command is being used. When the frame reject response is being sent, the first byte of this field is the command field of the rcv frame that is being rejected; the second byte is set to 0's (it is defined as the send and rcv sequence counts); and the third byte is set to X'04' if more data was rcv than could be buffered, or to X'01' if the Link Test command was rcv without the poll bit on. FC = frame check sequence. Two frame check char are always sent. Their bit configuration varies according tot he SDLC station adr, control field, and optional data fields. ee = an ending transmission of X'FF' to make the lines go to an idle state and to allow time for bits to be sent before dropping the 'RTS' lead on xmt turnarounds. All the data defined above between the two flag char is defined as a frame. All references in this document to the frame refer to this portion of each xmt or rcv segment of data. Note that if a frame is being sent/rcv in NRZI mode, the actual bit configuration on the line will differ from that shown above. Also, SDLC 0 bit insertion/deletion applies to all char except the flags and ending sequence defined under *ee*.					

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X6F0	XXXX							

Test statistics and error count are available while the test is running and at the manual intervention F02C test completion code. In addition, certain reg are used for current status indicators and may be displayed while the test is running or at the manual intervention F02C stop code. Following is the definition of the status indicators:

X'1E' reg contains the current xmt and rcv line status.

Byte 0 of reg X'1E' = last rcv frame type indicator; may contain one of the following indications:

- X'00' Time-out occurred on last rcv completion.
- X'80' A good link test frame was rcv with no errors.
- X'40' A frame reject response was rcv as the last frame rcv at this primary station.
- X'20' An unnumbered acknowledgment was rcv as the last frame at this primary station.
- X'10' A frame-check-sequence error was detected in the last rcv frame.
- X'08' An invalid or nonsupported frame was rcv as the last rcv frame. This link test only supports the link test response, the unnumbered acknowledgment response, and the frame reject response, if running as a primary station. The secondary station option will accept only a Link Test command, but it may respond with a link test response or a frame reject response. This type indicator is also set if a partial frame was rcv followed by an 'abort detect' sequence of seven or more consecutive 1 bits.
- X'04' A valid link test frame was rcv, but it contained more data than could be buffered. If this is a secondary station, a command reject response is sent for this frame. The maximum length of the rcv (and xmt) data buffer is 1024 char if the 3705 has more than 16K storage, or 10 char if the 3705 has only 16K of storage.
- X'02' Invalid SDLC station adr rcv or, for primary station option with optional xmt data, the rcv data did not compare with the SDLC station adr or optional xmt data that was sent. The SDLC station adr that you provide in the manual intervention F028 stop code is used to make this comparison. If the secondary station option was selected, this frame will not be responded to.
- X'01' A hardware-detected error such as modem check or overrun has been detected. No response is made to any frames rcv with this type of error.

Byte 1 of reg X'1E' = xmt line status and other info bits. Multiple bits may be on in this byte as opposed to byte 0, which never will have more than 1 bit on. The bits within this byte are defined as:

- X'80' A reply is pending to be sent to the last frame rcv at this secondary station.
- X'40' A command reject reply is now being sent or was the last frame xmt from this secondary station.
- X'20' A Link Test command (from primary station) or response (from secondary station) was the last frame sent or is being sent at this time.
- X'10' A xmt initial operation is being done or was the last xmt operation done. This xmt initial is done to set 'RTS' and to wait for 'CTS' from the modem intf for the first xmt operation of all primary station options and for secondary station options when 'RTS' should be on at all times. See manual intervention stop code F020 for this option.
- X'08' Xmt line is busy if this bit is on.
- X'04' Rcv line is busy if this bit is on.
- X'02' Bit not defined. May be used as added indicator at later time.
- X'01' Bit not defined. May be used as added indicator at later time.

X'1F' reg contains the accumulated xmt and rcv line status indicators. The bits in this reg have the same meaning as the bits defined for reg X'1E' except once these bits are set on, they are not reset until the test is restarted. These bits serve as a summary of all the xmt and rcv operations that have been done up to the time this reg is displayed.

X'1D' reg is used to control the E0 display code that is put out to the panel DISPLAY B lights (if DISPLAY/FUNCTION SELECT switch is in POSITION 4, 5, or 6). This reg is cleared to 0's at approximately 2-second intervals and, in between this clearing to 0's, it is used as an accumulator of all the bits defined in the reg X'1E' bits.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X6F0	XXXX	*X'46' reg* is the scanner display reg. Rtn X6F0 sets the display bit in the ICW for the rcv line used in this test. For half-duplex lines, this reg gives you the current line intf conditions for both the xmt and rcv operations. For duplex lines, this reg contains the rcv line intf conditions. Following are bit definitions for byte 0 of this reg: *Bit* *Hex* *Meaning if bit is on* 0 80 'CTS' is active; should be on while in xmt mode and may be on while in rcv mode. For duplex lines, this bit probably will not be on because it reflects the status of the rcv half of the duplex pair. 1 40 'Ring indicator' is active. 2 20 'DSR' is active; should be on for nonswitched lines and should come on after line is connected for switched lines. 3 10 'Rcv line signal detect' (carrier detect) is active, should be on while rcv and may be on while xmt. 4 08 'Rcv data bit buffer' is a 1 bit; should vary as rcv data varies. 5 04 'Diag mode' bit is on; but it should not be on in this test. 6 02 'Bit svc req' bit is on; should be on once each bit svc. *E0nn display codes.* While the link test is running, various display codes (except E06F) are displayed in DISPLAY B if you have the DISPLAY/FUNCTION SELECT switch in function POSITION 4, 5, or 6. These display codes are displayed approximately once every other second, with the DISPLAY B lights cleared to 0 between each E0 display. These E0 display codes are defined as: E000 (alternating with E0FF) Waiting for 'DSR' to come on before doing any xmt or rcv operations. These codes will be continuously displayed until 'DSR' comes on by completing a manual switched connection or by connecting (or jumpering) the proper modem intf leads. On a nonswitched-line connection, you will not see this display code if 'DSR' is always on (as expected). E060 A good test frame was rcv within the last 2 seconds, and no other error was detected (except a possible time-out). E061 Nothing was rcv (time-outs) during the last 2 seconds. E062 A frame-check sequence error was detected in some frame during the last 2 seconds. E063 A nonsupported or invalid frame was rcv during the last 2 seconds. E064 More data was rcv than could be buffered during the last 2 seconds. E065 A frame reject response was rcv at this primary station during the last 2 seconds. E066 An unnumbered acknowledgment was rcv at this primary station during the last 2 seconds. E067 Either of 3 conditions may exist: 1- SDLC station adr did not compare. 2- Rcv data did not compare with xmt data. 3- Secondary station rcv more data than could be buffered. In all cases, display code E067 indicates that the data rcv does not compare with data xmt. E068 A hardware-detected error such as modem check or overrun has been detected during the last 2 seconds. E06F This code is displayed if you are using the dynamic communication option (FUNCTION 1 and switches B-E set to D0nn) and have entered a D0nn code that is not defined. No action is taken if this code is displayed. *D0nn dynamic communication codes.* These dynamic communication codes allow you to terminate or restart the link test at various points within the test. You enter these codes while the pgm is running by setting the DISPLAY/FUNCTION SELECT switch to FUNCTION 1, by setting the selected code in switches B-E, and then pressing the INTERRUPT key on the control panel. These dynamic communication options are the same as those defined in the F02C manual intervention stop code definition. They are repeated here in a summary form. For more details, see the F02C stop code definition. D000 Restart link test at xmt/rcv data point (no line resets). D001 Restart rtn from beginning, including asking for options. D002 Restart link test, including hardware resets and enables. D003 Stop rtn at F02C stop code and display statistics. D004 Terminate rtn after hardware resets.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X6F0	XXXX	*Statistics at link test termination.* *X'1C' reg* contains the adr of a statistics table in storage. At all times while the test is running and at the manual intervention F02C and X6F0 0Xnn stop codes, you can get the storage adr of the statistics table from this reg and can display the storage locations for the following half-word counters. Following is a list of what is available in these statistics: *Hex displacement within statistics pointed to by reg X'1C'* 00 Number of SDLC link test frames xmt successfully. This count does not include frame reject responses sent from a secondary station. 02 Number of SDLC link test frames rcv with no errors. If this is a primary station, the rcv SDLC station adr and, (if used), the optional data must compare in order to have 1 added to this count. On a normal manual intervention F02C completion at a primary station, this count should match the number of test-frames-xmt count if no errors have been detected. An exception is when the secondary station responds with unnumbered acknowledgments to test frames; then this count should be 0, and the rcv unnumbered-acknowledgments count should match the number of test-frames-xmt count. 04 Number of frames rcv with frame-check-sequence errors. 06 Number of frame reject responses rcv at this secondary station. 08 Number of unnumbered acknowledgments rcv at this secondary station. 0A Number of frames rcv that were not included in other rcv counts. This count includes frames rcv with invalid SDLC station adr, nonsupported commands/responses, nondata compares with optional xmt data and frames terminated by an abort detection condition. Note that some of these conditions may have caused a frame-check-sequence error and be included in the frame-check error count rather than in this count. 0C For a primary station, this field contains number of test frames requested to be sent manual intervention. If this field is all 0's and a primary station option was selected, test frames will be sent continuously, allowing for rcv, etc., without ever terminating the test. 0E Number of hardware errors detected, such as modem check or overruns, on the xmt and rcv operations. 10 Number of frame reject responses xmt by this secondary station. Following are the error stop codes that may occur in this test. Note that any error stop codes beginning with 1 or 2 in DISPLAY B byte 0 bits 0-3 are defined in "Common Error Stops" following this CSB symptom index. The DISPLAY B codes starting with F are defined in "Manual Intervention following this CSB symptom index.					
	0X07	Auto-call failed to complete	An auto-call error has been detected. Reg. X'15' byte 0 contains an error indicator number. Determine error indicator and see the following description: *Error Indicator* 1 Error in auto-call connection. Reg. X'15' byte 1 contains SDF bits in error. SDF bits 0-4 are on; 5-7 are off. Also it indicates an error if LCD is not = 3 and PCF not = 4 (reg. X'45' byte 0). 2 Error in dialing. See error indicator 1 description. 4, 5, and 6 If last digit dialed was not an EON digit, PND may come on and cause a L2 irpt if the distant station does not answer immediately. The same thing will occur with EON, as last digit, on some OEM (non-IBM) and on IBM auto-call units that do not have the EON feature strapped on. On some OEM auto-call units, the EON will cause the auto-call unit to transfer control to the modem/data set with 'DSR' on immediately, even though no distant station has been connected and given an answer tone. 4 Error indicating PWI, CRQ or DLO not on. Reg X'15' byte 1 bits 1, 2, and 3 should be on. 5 No auto-call completion (time-out). Reg X'15' byte 1 bit 6 (COS) should be on. 6 Abandon-call and retry came on. Reg X'15' byte 1 bit 7 came on.					Reg X'15' byte 1 = SDF bits 0-7. SDF bit definitions for auto-call are: Bit 0 = (IR) intrpt remember. Bit 1 = (PWI) power indicator. Bit 2 = (CRQ) call request. Bit 3 = (DLO) data line occupied. Bit 4 = (PND) present next digit. Bit 5 = (DPR) digit present. Bit 6 = (COS) call originate status. Bit 7 = abandon call and retry.

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Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X6F0	0X20	Xmt line operations	A xmt line error has been detected. Reg X'13' = accumulated ICW bits 0-15 during this xmt operation. On each L2 irpt, ICW bits 0-7 are stored together and saved for this error display. If reg X'15' byte 0 bit 3 (X'10') is on, the xmt line has timed out due to 'CTS' not coming on or due to some other xmt failure such as loss of xmt clock.					See X6F0 XXXX for more reg and error states. If continuing from this error stop by selecting FUNCTION 5 and pressing START, the test restarts at the xmt/rcv portion without hardware reset and enable. This error may be found more easily in rtn X6CE.
	0X60	Rcv error completion	This error stop occurs if a modem check has been detected (ICW bit 3 on) while in rcv mode. This stop also occurs if you select the options to stop on any frame or any frame in error. Reg X'13' = ICW bits accumulated during this rcv operation by storing ICW bits 0-7 together and saving them on each L2 irpt. Note that pgm does not stop on rcv time-outs but sets up to xmt again if a primary station or to rcv again if a secondary station. Reg X'16' = adr of rcv data buffer in storage, and reg X'19' = adr + 1 of last rcv char. Note that reg defined in X6F0 XXXX provide more info.					See X6F0 XXXX notes for test run details, reg, and test statistics. To continue from this stop, select FUNCTION 5 and press START. The test restarts at the xmt/rcv portion of the test without hardware resets and enables.
	0X61	Rcv frames	This stop code occurred because you selected an option to stop on the type of frame just rcv. Reg X'1E' defines type of frame rcv and is defined in X6F0 XXXX. Reg X'16' = adr of start of rcv data buffer. Reg X'19' = adr + 1 of last char rcv (less frame-check char). Reg X'14' = accumulated frame-check char accumulated by this pgm and should = X'F0B8' if no errors occurred. Reg X'13' = last 2 rcv char (prior to flag char) and should be the actual rcv frame check sequence.					See X6F0 XXXX for reg and test statistics. To continue, select FUNCTION 5 and press START. The pgm restarts at the xmt/rcv data portion of the test without hardware reset and enable operations but the pgm clears the stat counters.

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Routine	Error Code	Function Tested
X6F2	X.XXX	Wrap data test – BSC and SDLC. This is a manual intervention wrap rtn, which runs only if you set the CE sense switch to run manual intervention rtn or request a single rtn to be run. At the first manual intervention stop F049 enter the desired options: SWITCH B C D E 0 - - - First oscillator 1 - - - Second oscillator 2 - - - Third oscillator 3 - - - Fourth oscillator 4 - - - Data rate select 8 - - - External clock - 0 0 0 No request - 4 0 0 Auto-call request (for manual intervention stops F029, F02A, and F02B, see pages CSB 804 and CSB 806)* - 0 0 1 Xmt without a rcv line (no wrap) - 0 0 2 Xmt and rcv; swap lines and repeat - 0 0 3 Xmt and rcv same pair At manual intervention stop F050, enter a valid xmt line adr and wrap type operator (does not apply to auto-call requests). *BSC SWITCHES* *B C D E* — *SDLC SWITCHES* *B C D E* 5 X X X — D X X X Normal (DTR/not diag mode). An external wrap facility must be provided to wrap data with this option. 6 X X X — E X X X Line set wrap (diag mode/not DTR) 7 X X X — F X X X Modem wrap (diag mode/DTR) for modems that use the modem wrap signal At manual intervention stop F052, enter a valid rcv line adr and wrap type operator in the same format as in stop F050.

*Auto-call operation only (data link will not be established).

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X6F2	0X01	A set mode was executed on the rcv line (adr in reg X'13').	Either the expected L2 did not occur or the wrong line irpt. Reg X'14' contains the irpt line adr.					The reference data for this test is variable and is not given.
	0X02	The LCD of the rcv line was checked for a feedback check.	A feedback check occurred in the set mode to the rcv line.					
	0X03	A set mode was executed on the xmt line (adr in reg X'11').	Either the expected L2 did not occur or the wrong line irpt. Reg X'14' contains the irpt line adr.					
	0X04	The LCD of the xmt line was checked for a feedback check.	A feedback check occurred in the set mode to the xmt line.					
	0X06	The modem should cause 'CTS' to come up on the xmt line after approximately 300ms.	The xmt line display reg did not contain the 'CTS' bit.					
	0X07	The modem should cause 'DSR' to come up on the xmt line.	The xmt line display reg did not contain the 'DSR' bit.					
	0X10	An irpt was expected from either the xmt or the rcv line. The test is xmt and rcv (if rcv is selected).	No irpt received (rcv line, xmt line or unexpected).					
	0X13	The xmt and rcv should irpt for svc each char time.	The rcv line has not irpt after at least 20 xmt line irpt.					
	0X15	Checking input X'44' for correct flags set	Flags set in SCF during the rcv were not set properly. Reg X'15' contains the adr of the flags and data rcv.					
	0X16	Checking data rcv against the data expected	The data rcv is not equal to that expected. Reg X'15' byte 1 is the data rcv, byte 2 is the data rcv. Reg X'17' points to the expected byte; reg X'16' points to the rcv data; SCF flags in byte 1 are at adr pointed to by reg X'16'.					
	0XD8	Auto-call failed to complete	An auto-call error has been detected. Reg. X'15' byte 0 contains an error indicator number. Determine error indicator and see the following description: *Error Indicator* 1 Error in auto-call connection. Reg. X'15' byte 1 contains SDF bits in error. SDF bits 0-4 are on; 5-7 are off. Also it indicates an error if LCD is not = 3 and PCF not = 4 (reg. X'45' byte 0). 2 Error in dialing. See error indicator 1 description. 3 Error indicating PWI, CRQ or DLO not on. Reg. X'15' byte 1 bits 1, 2, and 3 should be on.					Reg X'15' byte 1 = SDF bits 0-7. SDF bit definitions for auto-call are: Bit 0 = (IR) intrpt remember. Bit 1 = (PWI) power indicator. Bit 2 = (CRQ) call request. Bit 3 = (DLO) data line occupied. Bit 4 = (PND) present next digit. Bit 5 = (DPR) digit present. Bit 6 = (COS) call originate status. Bit 7 = abandon call and retry.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X6F4	XXXX	X.21 line set test. This is a manual intervention rtn, which runs only if directly selected or the CE sense switch is set to run manual intervention rtn. This rtn tests the X.21 line sets' unique handling of 'DSR' and 'CTS'. If the switch option is specified, the bit-pattern generator and state-generation circuits are also tested. The xmt and rcv lines must be wrapped (transmit T and C signals connected to the receive R and I signals respectively) by an external facility. Refer to CTRL PNL Section in Volume 2 for wrap test block info. Most of the tests are performed on the xmt line, with the results being checked on the xmt and/or rcv lines. This rtn should be run twice on a half-duplex pair, reversing the adr specified as the xmt and rcv lines the second time. Data is not explicitly wrapped by this rtn. Use rtn X6F2 for this purpose and to further verify the line set and external wrap connection. Refer to logic page VA017 for the jumper information. The following manual intervention stops occur. At manual intervention stop F055, enter the rtn options as follows: *Switch* *B C D E* X Y Z 2 2400 bps Jumpers are in delay position. X Y Z 3 2400 bps Jumpers are in no delay position. X 8 Z 4 4800 bps Jumpers are in delay position. X 8 Z 5 4800 bps Jumpers are in no delay position. X 8 Z 6 9600 bps Jumpers are in delay position. X 8 Z 7 9600 bps Jumpers are in no delay position. X 8 Z 8 48K bps Jumpers are in delay position. X 8 Z 9 48K bps Jumpers are in no delay position.					

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Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X6F4	XXXX	where x = 0 If the rtn is not to be looped without respecifying the manual input. x = 1 If the rtn is to be looped without respecifying the manual input. y = 0 If internal 2400 bps clock is to be used. **Note:** This option is valid only for 2400 bps. y = 8 If external clock is to be used. z = 0 If the line set is jumpered for nonswitched half-duplex operation. z = 1 If the line set is jumpered for switched operation. z = 2 If the line set is jumpered for nonswitched full-duplex operation. At stop F056, enter the xmt line adr. *Switch* *B C D E* 0 X X X XXX is the xmt line adr as defined in the F001 manual intervention stop code. At stop F057, enter the rcv line adr. *Switch* *B C D E* 0 X X X XXX is the rcv line adr as defined in the F001 manual intervention stop code. At manual intervention stop F059, disconnect the external wrap facility. This stop code will be bypassed if the loop option was specified in response to manual intervention stop code F055. Error stops in this rtn, except for the set mode pretest errors (1X03 and 1X04), are most likely caused by failures in the line set cards if the other type 2 scanner rtn have run successfully. Refer to logic page VA000 for line set card locations. Any one of the three cards of the line set could be causing the error as no attempt is made by this rtn to isolate failures any further.					
	0X05	DTE controlled not ready state	12 bit times after the rcv line was initialized an alternating bit pattern was not detected in the SDF.					
		Note: Error 0X05 will occur only if switched and external clock options are specified.						
	0X07	DTE ready state	10 bit times after DTR was set on the xmt line, all 1's were not detected in the SDF of the rcv line.					
	0X08	DSR active on the xmt side.	DSR on the xmt side was not active.					
		Note: Error 0X08 will occur only if nonswitched duplex or switched option is specified.						
	0X09	'DSR' active on the rcv side.	'DSR' on the rcv side was not active.					
	0X0B	'DSR' on the rcv line stays active at least 12 bit times after diag mode is set on the xmt line.	'DSR' became inactive on the rcv line too soon after 'diag mode' was set on the xmt line.					
	0X0C	'DSR' on the rcv line becomes inactive 22 bit times after diag mode is set on the xmt line.	'DSR' on the rcv line was still active 22 bit times after diag mode on the xmt line should have forced 'ctrl' and 'xmt' and, therefore, 'indicate' and 'rcv' on the rcv side to 0's.					
	0X0D	A bit pattern for a SDLC flag is generated on the rcv line after 'DSR' becomes inactive.	A SDLC flag bit pattern was not detected in the SDF within 20 bit times after 'DSR' became inactive.					
		Note: Error 0X0D will occur only if the switched option was specified.						
	0X0E	A bit pattern for an ASCII SYN is generated on the rcv line after 'DSR' became inactive.	An ASCII SYN bit pattern was not detected in the SDF within at least 20 bit times after the SDLC flag bit pattern was detected.					
		Note: Error 0X0E will occur only if the switch option was specified.						
	0X12	All marks generated by the xmt line and rcv when diag mode is reset and 'DTR' is set on the xmt line. Data rate select is also set at this time, but it should have no effect because 'RTS' is off.	All marks were not detected in the rcv line's SDF 10 bit times after the set mode irpt from the xmt line.					

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X6F4	0X13	'Indicate' is inactive on the rcv line when 'RTS' is inactive on the xmt line.	'Indicate' is active on the line before 'RTS' has been activated on the xmt line.					
	0X15	'CTS' is inactive on the xmt line when 'RTS' is inactive on the xmt line.	'CTS' is active on the xmt line before 'RTS' has been activated on the xmt line.					
	0X18	'Indicate' becomes active on the rcv line when 'CTS' is activated on the xmt line.	'Indicate' did not become active on the rcv line after 'RTS' was activated on the xmt line.					
	0X19	'CTS' delay **Note:** Error 0X19 will occur only if the delay option was specified.	'CTS' became active less than 21 bit times after 'RTS' was set in the line set ('Indicate' detected on the rcv line).					
	0X20	'CTS' becomes active after 'RTS' is activated	'CTS' did not become active within one scan time with no delay, 31 bit times with delay after 'RTS' was set in the line set ('Indicate' detected on the rcv side).					
	0X21	Call request state **Note:** Error 0X21 will occur only if the switched option is specified.	All 0's were not detected in the rcv line's SDF when 'RTS', data rate select, and 'DTR' are on in the xmt line.					
	0X22	'DSR' stays active on the xmt line when 'Indicate' is active and the rcv data line is held at space for at least 20 bit times. **Note:** Error 0X22 will occur only if the nonswitched duplex or switched option is specified.	'DSR' became inactive on the xmt line while a continuous space was being rcv when 'Indicate' was active ('RTS' active on the xmt line).					
	0X23	'DSR' stays active on the rcv line when 'Indicate' is active and the rcv data line is held at space for at least 20 bit times.	'DSR' becomes inactive on the rcv line while a continuous space was being rcv when 'Indicate' was active ('RTS' active on the xmt line).					
	0X25	'DSR' stays active on the xmt line at least 12 bit times after 'diag mode' is set on the xmt line. **Note:** Error 0X25 will occur only if the nonswitched duplex or switched option is specified.	'DSR' became inactive on the xmt line too soon after 'diag mode' was set on the xmt line.					
	0X26	'DSR' becomes inactive on the xmt line 22 bit times after 'diag mode' is set on the xmt line. **Note:** Error 0X26 will occur only if the nonswitched duplex or switched option is specified.	'DSR' on the xmt line was still active 22 bit times after 'diag mode' on the xmt line should have forced C and T and, therefore, I and R on the rcv side to 0's.					
	0X27	'DSR' becomes inactive on the xmt line when the external connection is broken. **Note:** Error 0X27 will occur only if the nonswitched duplex or switched option is specified.	'DSR' did not become inactive on the xmt line when the external connection was unplugged.					
	0X28	'DSR' becomes inactive on the rcv line when the external connection is broken.	'DSR' did not become inactive on the rcv line when the external connection was unplugged.					
X6F5	XXXX	High-speed local attachment oscillator speed test. This manual intervention rtn checks the 14.4KHZ/57.6KHZ high-speed oscillator that is supplied for the High-Speed Local Attachment Line features. The frequency to be checked must be jumpered on the LIB type 1 board in which the oscillator is installed. See the following switch entry specifications for the jumper info. The oscillator frequency is checked to ensure that there is not more than a plus or minus 0.1 percent variation from its expected frequency. The oscillator frequency and the line that it is to be checked on are entered in the ADDRESS/DATA switches at manual intervention stop code F058 as follows: *Switch* *B C D E* 0 X X X 14.4KHZ test on line XXX (jumper on pin side A2G4B07 to A2G4B05) 1 X X X 57.6KHZ test on line XXX (jumper on bin side A2G4B07 to A2G4B09) Where XXX is the line adr as defined in the F001 manual intervention stop code.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments
X6F5	XXXX	The oscillator frequency is determined by the number of bits shifted in the SDF versus the number of times through a pgm loop. The SDF is set to X'01FE', and a bit count and pgm loop count are initialized. Each time through the loop, the loop count is decremented by 1, and the low order SDF bit is checked. When the low-order SDF bit is 1, the SDF is reinitialized to X'01FE', and the bit count is decremented by 1. If the loop count is decremented to 0 before the bit count, the residual bit count is compared to 0.1 percent of its initial value. If the bit count is decremented to 0 before the pgm loop count, the residual pgm loop count is compared to 0.1 percent of its initial value. This rtn indicates failures if: 1. The frequency selected in ADDRESS/DATA switch B does not agree with the frequency selected by the jumper on A2G4. 2. The oscillator card is defective. 3. 'External oscillator select' bit in the line set fails to set. 4. Oscillator gating controls are defective.						
	0X01	Set mode to set external clock	No L2 irpt occurred.	A3L2 A3T2 A3T4 A3U2 A3U4		TA611 TB411 TB412 TB413 TB414	C-020 C-160	Reg X'11' contains the line adr the L2 irpt was expected from.
	0X02	SDF shifting	SDF bit 9 did not set to 1 in the approximate 180 ms wait time.	A3L2 A2G4		TA611 VA070	C-020	SDF bits 1, 2, 3, 4, and 5 were set by an output X'46' with X'01F0'. Regs X'14' and X'13' contain the state of the ICW bits 2.0-5.7 at the end of the wait time. Reg X'14' contains the SDF bits 0-7 in byte 1. Reg X'13' contains SDF bits 8 and 9 in 0.0-0.1 and external clock bit in 1.7.
	0X03	Oscillator frequency	Oscillator under test running too fast. The bit count decremented to 0 before the pgm loop count was decremented below 0.1 percent of its initial value.	A3L2 A2G4		TA611 VA070	C-020	Reg X'14' contains the residual loop count. Reg X'16' contains the initial loop count.
	0X04	Oscillator frequency	Oscillator under test running too slowly. The pgm loop count decremented to 0 before the bit count was decremented below 0.1 percent of its initial value.	A3L2 A2G4		TA611 VA070	C-020	Reg X'14' contains the residual bit count. Reg X'16' contains the initial bit count.

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Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments

NOTES:

The following notes, which are referred to in either the error code description or the error code comments, provide reg contents and other info for that error code.

Note 1: The expected char-svc L2 irpt either did not occur, or the char-svc L2 irpt was from the wrong line adr. The contents of the following reg indicate the type of error and the expected data:

Reg X'11' = line adr the char-svc L2 irpt was expected from. This line adr in in the format used to set ABAR.
Reg X'14' = either the line adr obtained from ABAR of the line that caused the char-svc L2 irpt; or, if reg X'14' = 0000, the expected char-svc L2 irpt did *not* occur.

Note 2: The expected xmt line char-svc L2 irpt either did not occur, or the char-svc L2 irpt was from the wrong line adr. The char-svc L2 irpt should be from the xmt line adr. The following reg indicate the type of error and the expected data:

Reg X'11' = xmt line adr the char-svc L2 irpt was expected from. This line adr in in the format used to set ABAR.
Reg X'14' = either the line adr obtained from ABAR of the line that caused the char-svc L2 irpt; or, if reg X'14' = 0000, the expected char-svc L2 irpt did *not* occur.
Reg X'13' = rcv line adr. There should be no rcv line char-svc L2 irpt at this time. Error could be caused by a feedback check setting LCD to F on the xmt line, by the xmt or rcv line selecting the wrong oscillator, by a clock correction failure in the BCC card of the LIB, or by some other line set, LIB, or scanner problem.

Note 3: The expected rcv line char-svc L2 irpt either did not occur, or the char-svc L2 irpt was from the wrong line adr. The char-svc L2 irpt should be from the rcv line adr. The following reg indicate the type of error and the expected data:

Reg X'13' = rcv line adr the char-svc L2 irpt was expected from. This line adr in in the format used to set ABAR.
Reg X'14' = either the line adr obtained from ABAR of the line that caused the char-svc L2 irpt; or, if reg X'14' = 0000, the expected char-svc L2 irpt did *not* occur.
Reg X'11' = xmt line adr. There should be no xmt line char-svc L2 irpt at this time. Error could be caused by a feedback check setting LCD to F on the rcv line, by the xmt or rcv line selecting the wrong oscillator, by a clock correction failure in the BCC card of the LIB, or by some other line set, LIB, or scanner problem.

Note 4: The 'test data' latch and its function in the diag wrap tests is a major tool in problem determination for the type 2 communication scanner internal functional tests. Most of the rtn that xmt and/or rcv data depend on the proper setting of the 'test data' latch in the communication scanner. The test data latch is set to a mark condition when an ICW is scanned and that ICW is for a line adr that is in diag mode, has a bit svc pending, and any of the following conditions apply:

a. Xmt state and next bit to be xmt is a 1.
b. A set mode (PCF = 1) is being done.
c. Disable communication scanner (power on reset) is active.

In step a, the next bit to be xmt may be from SDF bit 9, PDF bit 7, or a 1 bit forced by some other conditions, such as xmt initial.

The 'test data' latch may be set to a space condition when an ICW is scanned and that ICW is for a line adr that is in diag, has a bit svc pending, is in xmt state, and the next bit to be xmt is a 0. The 0 bit to be xmt may be from SDF bit 9, PDF bit 7, a forced start bit, 0 bit insert, or 0 bit break signal.

Line adr in rcv mode strobe data into the rcv data bit buffer from the 'test data' latch if, when the ICW is scanned the line is in diag mode, a bit svc is pending, and 'DTR' is not on.

During diag mode transmissions, the transitions between mark and space in the 'test data' latch should follow the bit svc requests caused by the xmt clock (oscillator). The ICW for the diag xmt line must be scanned before the 'test data' latch can be set or reset, so there may be a delay of up to one full scan period before the 'test data' latch is set or reset after the bit svc request is made. The period differences between the scan cycles and bit svc requests usually result in an average delay of one-half of a scan period between the bit svc and the setting or resetting of the 'test data' latch. An unstable trace appears on the 'test data' latch during diag xmt operation caused by this delay. This unstable trace also occurs at the send data bit buffers during normal line xmt; unstable trace does not occur on the actual xmt line because the bit to be xmt is not set into the xmt trigger until the next bit svc request time.

There is an average delay of one-half of a scan period between the time when the rcv line bit svc occurs and the rcv data bit is gated into the SDF or PDF of the rcv line's ICW.

The above two delays on the diag xmt and rcv operations normally account for less than one-half of a bit time. This delay usually will have no affect on a diag wrap operation except that the rcv clock correction circuits will be forced into action to correct for the jitter on the 'test data' latch. With the higher speed oscillators, this delay, along with rcv clock correction, may add up to more than half of a bit time. When this delay exceeds half of a bit time, the sequence of xmt and rcv line char-svc L2 irpt may be affected. This sequence of irpt is explained in more detail in notes 5 and 6.

Note 5: The rtn did a diag wrap data using S/S LCDs. The rcv line adr is expected to cause its char-svc L2 irpt with a char being rcv before the char is completely xmt on the xmt line adr. This occurs only in diag mode when the 'test data' latch is in use (see note 4). During the manual intervention external data wrap test and during normal line operation, this does not occur because there is an extra bit time delay between the send data bit buffer and the xmt trigger. The rcv irpt occurs before the xmt irpt because the rcv line strobes the rcv data bit and requests its char-svc L2 irpt near the middle of the first or only stop bit at the end of the rcv data char. The xmt line does not request its char-svc L2 irpt until the end of the last or only stop bit at the end of the char being

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	Program Mask	FEALD Page	FETMM Page	Comments

xmt. This does not apply to the xmt of a PAD char (all 1 bits with no start bit) since the rcv line, in S/S mode, should not cause a char-svc L2 irpt when rcv pad char. If the line adr are irpt out of sequence and if neither line has had a feedback check (LCD = F), there are many possibilities that can cause the error. Some of them are:

a. Oscillator select bits are not selecting the correct oscillator or blocking the other oscillators causing extra or missing strobes.
b. Start, stop, or tag bit recognition is not working.
c. LCD is not being recognized as a S/S type.
d. Rcv clock correction is working incorrectly.

See note 7 for aids in isolating problems to the communication scanner, LIB, or line sets. Another possible failure is that the oscillator is running much too fast or that an oscillator above 1200 is installed but is configured as a slower speed oscillator in the CDS. If the oscillator is much too fast (or too many strobes are occurring from some other source), the irpt can occur out of sequence due to the 'test data' latch delays explained in note 4. This condition can be tested by running rtn X67A, which is the oscillator speed test. If the CDS indicates that the first installed oscillator exceeds 1200 bps, some portions of a few rtn are bypassed due to the delay times explained in note 4.

Note 6: The rtn did a diag wrap data using sync LCDs. The rcv line adr is expected to cause its char-svc L2 irpt with the char being rcv before the char is actually fully xmt. The rcv line should not irpt until it detects a rcv data bit pattern that is recognized as a SYN char for the particular line control (LCD) in use. Therefore, the xmt line adr normally has several char-svc L2 irpt to xmt PAD and SYN characters before the rcv line has any. The rtn shift the xmt line's data char by one or more bit positions to cause the rcv line to recognize the SYN char bit pattern one or more bit times before the end of the xmt char. This is done to ensure that the sequence of irpt would be predictable so that the line sets could be tested for clock correction or selection errors. Without this xmt char shifting, out-of-sequence irpt could occur on high-speed oscillators due to the 'test data' latch jitter explained in note 4 and the different type clock correction done in sync mode over S/S mode. If the line adr are irpt out of sequence and if neither line has had a feedback check (LCD = F), there are many possibilities that can cause the error. Some of them are:

a. Oscillator select bits are not selecting the correct oscillator or blocking the other oscillators, causing extra or missing strobe pulses.
b. Tag bit recognition is not working.
c. LCD is not recognized as a synchronous LCD.
d. Rcv clock correction is not working properly.

See note 7 for aids in isolating problems in the communication scanner, LIB or line sets. Another possibility is that the oscillator is running much too fast or some other failure is causing too many strobe pulses. In this case, the irpt could occur out of sequence due to the 'test data' latch jitter and delays explained in note 4.

Note 7: This note is referred to by those rtn that run on more than one line adr (not necessarily at the same time) and allow you to use the continue function. This rtn allows using the continue function after an error stop to help isolate a problem to the communication scanner, LIB, or line sets. When an error stop occurs, record the line adr and other info about that error; then select FUNCTION 5 and press the pushbutton to continue from that error stop. Other error stops for the same line adr will probably occur, but they should be ignored since they were probably caused by the previous error or by over/under run. When the rtn has finished testing one line adr or a pair of line adr, it does a reset to the scanner and then starts the test on the next line or pair of line adr. Because of this, the first error stop for each line adr should be recorded to develop a failure pattern to use to isolate the failure to one line adr, a pair of line adr, all the line adr in a LIB, or all line adr in the scanner. If only one line adr or a pair of even-odd line adr fail, the problem is probably with the line set card for that position. If all line adr fail, the problem could be with LIB or communication scanner adr failures or bad cable connections between the scanner and LIB. A bad bit clock control card in the LIB could also cause all line adr in a LIB to cause failures that look like line set failures.

3705-80 CSB IFT COMMON ERROR STOPS

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
X6XX	1X01	Configuration data set	CDS indicates it is not for the type 2 communication scanner or that it has an invalid scanner number in its scanner type and number field.				Reg X'16' = storage adr of the scanner control block that is in error within the CDS.
	1X03	Set mode	The L2 irpt that occurred during set mode was not from the expected line adr. This is a pretest error so if you use the continue function (FUNCTION 5), the set mode will be tried again.		TA611	B-260	Reg X'14' = line adr (as used to set ABAR) of the ICW that irpt in error. Reg X'11' = the line adr that the L2 was expected from. If reg X'14' = 0000, no L2 occurred.
	1X04	Set mode	A feedback check occurred, setting the LCD field of the ICW to X'F'. This is a pretest error so if you use the continue function (FUNCTION 5), the set mode will be tried again.	A3E2	TA341	B-260	Reg X'11' = line adr (as used to set ABAR) of the scanner/LIB/line intf adr that the set mode is being done on at this time.
	1X05	Set mode	Missing the L2 irpt expected within 1 bit time after doing the set mode. This is a pretest error so if you use the continue function (FUNCTION 5), the set mode will be tried again.	A3L2	TA611	B-310	Reg X'11' = line adr (as used to set ABAR) of the line set that the set mode is being done on.
	1X06	Configuration data set	An invalid LIB type is defined for the scanner being tested.				Reg X'15' byte 0 = the invalid LIB type found in the CDS. Reg X'11' = adr (as used to set ABAR) for the scanner/LIB/intf adr.
	1X07	Configuration data set	An invalid line set type is defined for the line being tested. Refer to the CDS section.				Reg X'15' byte 1 = the invalid line set type found in the CDS. Reg X'11' = line adr being checked.
	2X01	All functions not expecting or causing L1 irpt	Unexpected L1 irpt occurred with no CCU or adapter L1 error bits on.	A3C2	TB131	6-082	
	2X02	All functions not expecting a L1 irpt or causing a L1 irpt	Unexpected L1 irpt occurred, indicating a type 2 scanner L1 error.	A3C2	TB131	B-130	Reg X'76' contains adapter L1 irpt error bits.
	2X03	All functions not expecting or causing a L1 irpt	L1 adapter (type 2 scanner) irpt occurred with no scanner error reg X'43' bits on for the scanner causing this error.	A3C2	TB131	B-130	
	2X04	All functions allowing adapter L1 irpt	Cannot reset type 2 scanner adapter L1 irpt bits.	A3C2	TB131	B-130	Reg X'76' contains adapter irpt error bits.
	2X05	All functions	An input/output check caused by a valid input or output inst.	A3C2	TB131	B-290	Reg X'74' contains adr of the valid input or output inst.
	2X21	All functions not expecting L2 irpt but allowing L2 irpt to occur	Unexpected L2 irpt occurred.	A3L2	TA611	6-082	
	2X33	All functions	An unexpected L3 irpt occurred with no L3 irpt request bits on.			6-082	
	2X44	All functions	L4 unexpected reentrance. The DCM gives control to all rtn with L4 PCI bit on (reg 7F byte 0 bit 7 on). This bit should never be turned off and should never exit L4 except to L1, L2, and L3, which are higher priority.			6-082	
	E0nn	Display info	This display is for info only. The nn after the E0 is the LIB and line adr now under test unless otherwise specified in the rtn write up.				This E0nn display is to let you know that the rtn is running.

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3705-80 CSB IFT MANUAL INTERVENTION STOPS

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
F001	Enter the line adr to be tested. Set switches B, C, D, and E to 0000 to test all adr, and set to FFFF to bypass all testing. Otherwise, enter the line adr as used to set ABAR. Refer to CS2 section in Volume 3 for a chart on all valid line adr. Some rtn will not accept the 0000 switch settings to test all installed line adr; and, in that case, you will get another manual stop code saying an invalid line adr was selected. To continue from manual intervention stops, set the required info into the STORAGE ADDRESS/REGISTER DATA switches B, C, D and E: set the DISPLAY/FUNCTION SELECT switch to function and press the START pushbutton. Following is the format to use when entering the line adr: *Hex* Switch B 0 Switch C 0 for 1st scanner adr bits Switch D 4 for 1st LIB, lines 0-7 5 for 1st LIB, lines 8-F 6 for 2nd LIB, lines 0-7 7 for 2nd LIB, lines 8-F Switch E 0 for lines 0 or 8 2 for lines 1 or 9 4 for lines 2 or A 6 for lines 3 or B 8 for lines 4 or C A for lines 5 or D C for lines 6 or E E for lines 7 or F						
F002	Invalid scanner adr bits were entered in switch C. Re-enter the line adr as in stop code F001.						
F003	The selected scanner is not installed or not configured properly in CDS. Reg X'16' contains the adr of the scanner block for the requested scanner. If reg X'16' = X'0000', the scanner is not configured. Re-enter the request as in stop code F001.						
F004	Invalid LIB adr selected. Re-enter the request as in stop code F001. (Only 4 LIBs are allowed in the first scanner.)						
F007	The selected line adr is not installed according to data in the CDS. This manual intervention rtn requires a line adapter to be installed to run tests. Re-enter the line adr as in stop code F001.						
F008	The manual intervention rtn cannot run tests on the LIB or type of line adapter for the line adr selected. Re-enter the line adr as in stop code F001.						
F020	Enter the link test line type and control options. Primary station option initiates link test; secondary station option responds only to link test command rcv from a remote primary station. 'RTS' = ON means that 'RTS' is to be left on at all times (even during rcv operations); 'RTS' is normally used for point-to-point 4-wire half-duplex and duplex nonswitched lines for both primary and secondary stations. For multipoint primary stations, the 'RTS' = ON option is usually used for 4-wire half-duplex and duplex lines. Two-wire nonswitched lines, switched lines and multipoint secondary stations usually use the 'RTS' = OFF option to drop 'RTS' while not in xmt mode. The 'external clock', 'data rate select' = ON and 'oscillator select' options are dependent on the type of modem connected and the type of internal and/or external clocks installed. If you select the 'external clock' option (with or without 'data rate select' = ON), the pgm will not use NRZI mode of transmission. If you select internal oscillators number 0, 1, 2, or 3, the pgm uses NRZI mode. NRZI mode means (as implemented in the 3705) that if a 0 bit is to be xmt, the xmt line trigger is complemented; if a 1 bit is to be sent, the state of the xmt line trigger is not changed. The combination of NRZI mode and SDLC 0-bit-insertion operations always results in at least one data transition every six bit times so that modem or internal clocks can be kept in phase. NRZI mode is not used when external clock is selected from the modem since it is then the modem's responsibility to provide clock correction and bit synchronization. This automatic selection of NRZI mode according to type of line clocking is compatible with frame check sequence 3705 NCP utilization. The optional xmt data option can be used only with the primary station options to provide data char to be sent within the SDLC link test frames being xmt. This optional data is sent after the SDLC station adr and control fields and before the frame check sequence. If the optional xmt data option is not selected as a primary station option, the minimum test frame of 4 char (SDLC station adr, SDLC link test control field and two frame check char) preceded and followed by flag char are xmt. Note that 16 alternate bit transmissions are xmt before the first flag char of a frame so that the rcv clock can be corrected. To continue, set the STORAGE ADDRESS/REGISTER DATA switches B, C, D, and E to the required settings, set DISPLAY/FUNCTION SELECT switch to FUNCTION 5, and press the START pushbutton.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
F020							

Following are switch B-E settings for entering line type and control options for F020 stop code:

Switch B = line type options. Enter one of the following in switch B:

- 0 Primary station, half-duplex 2-wire nonswitched line with 'RTS' = OFF option.
- 1 Secondary station, half-duplex 2-wire nonswitched line with 'RTS' = OFF option.
- 2 Primary station, half-duplex 4-wire nonswitched line with 'RTS' = ON option (normally point-to-point).
- 3 Secondary station, half-duplex 4-wire nonswitched line with 'RTS' = ON option (normally point-to-point).
- 4 Secondary station, half-duplex 4-wire nonswitched line with 'RTS' = OFF option (normally multipoint secondary).
- 5 Primary station, duplex 4-wire nonswitched line with 'RTS' = ON option.
  Note: Requires duplex line set intf.
- 6 Secondary station, duplex 4-wire nonswitched line with 'RTS' = ON option.
  Note: Requires duplex line set intf.
- 7 Secondary station, duplex 4-wire nonswitched line with 'RTS' = OFF option (normally multipoint secondary).
  Note: Requires duplex line set intf.
- 8 Primary station, switched line with manual call, manual answer, or auto-answer with 'RTS' = OFF option.
  Note: Half-duplex only for switched lines.
- 9 Secondary station, switched line with manual call, manual answer, or auto-answer with 'RTS' = OFF option.
  Note: Half-duplex only for switched lines.
- A Primary station, switched line with auto-call.
  Note: Half-duplex only for switched lines.
- B Secondary station, switched line with auto-call.
  Note: Half-duplex only, for switched lines.

Switch C = clock control options. Enter one of the following in switch C:

- 0 Internal oscillator select 0 to use first internal oscillator
- 1 Internal oscillator select 1 to use second internal oscillator
- 2 Internal oscillator select 2 to use third internal oscillator
- 3 Internal oscillator select 3 to use fourth internal oscillator
- 4 Select external clock but do not select 'data rate select'
- 5 Select external clock and also set 'data rate select' to use the higher of the two external clocking rates

Switch D = NRZI control with external clock. Enter one of the following in switch D:

- 0 External clock, non-NRZI, or internal clock NRZI
- 1 External clock NRZI
- 2 External clock, new sync, non-NRZI mode
  Note: New sync is normally used with 4-wire multipoint nonswitched line modem equipment where the associated intf is designated as the master station (primary).
- 3 External clock, new sync, and NRZI mode. See the note under 2 above.

Switch E = xmt and rcv data options. Enter one of the following in switch E:

- 0 No optional xmt data and not stopping on rcv frames.
- 1 Stop on any frame rcv with a bad frame check char.
- 2 Stop on any frame rcv other than a normal link test command or response.
- 3 Stop on any frame rcv (good or bad).

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
F020	4 Optional xmt data is required and will be requested in the F024 and F025 stop codes. This option is restricted to primary stations. This option does not include any stops on rcv frames. 5 Optional xmt data is required and will be requested in the F024 and F025 stop codes. This option is restricted to primary stations. This option includes a 'stop on any frame rcv with a frame check error' option. 6 Optional xmt data is required and will be requested in the F024 and F025 stop codes. This option is restricted to primary stations. This option includes the 'stop on any frame rcv other than a normal test frame' option. 7 Optional xmt data is required and will be requested in the F024 and F025 stop codes. This option is restricted to primary stations. This option includes the 'stop on any frame rcv' option.						
F021	Invalid option or invalid combination of options entered for the link test. Enter options again as defined in the F020 stop code.						
F022	Enter number of test frames to be xmt at this primary station for the link test. Set switches B–E to number (in hex) of times you want the test frame xmt before the pgm terminates with the F02C completion code. If you enter 0000, the test will not terminate unless you use the dynamic communication options or abort the test.						
F024	Enter first optional xmt data char for the primary station link test option. Set switches D and E to the hex char to be xmt. If only one optional data char is to be xmt, set switches B or C to any nonzero value. If more than one optional xmt data char is to be sent, set switches B and C to 00.						
F025	Enter next optional xmt data char to be sent from this primary station of the SDLC link test. Set switches D and E to the hex char that you want to use as the next data char to be xmt. If this is the last optional xmt data char you want to send, set switches B or C to any nonzero value. If you want to enter more optional xmt data, set switches B and C to 00; the current data char in switches D and E will be stored when you select FUNCTION 5 and press START. Then you will get this stop code again unless end of xmt buffer has been reached. You may enter up to 1022 char to be xmt with the F024 and F025 stop codes.						
F026	Enter xmt line intf adr. Enter line adr in same format as defined in the F001 manual intervention stop code. If you have selected an option using duplex lines, enter the xmt line intf adr of the duplex line intf par. **Note:** Duplex xmt line intf is always the first line intf adr of the even/odd line intf pair, with the even line intf adr being used as the xmt line and the odd line intf adr being used as the rcv line. Note also that this line intf adr to be entered does not use the low-order bit of byte 1 to set/input ABAR so that line adr such as 0842 and 0846 are considered to be odd line intf adr, and line adr such as 0840 and 0848 are even line intf adr. The line intf adr you enter is used to get line set type and options according to what is found in the configuration data set (CDS). If you have selected a not-installed or invalid line adr, you will get stop code F027 asking for the line intf adr again. If you have selected a duplex line option, the line set type must be a type that can run in duplex mode; the same applies for half-duplex, switched line, and internal/external clock selection. If you enter FF in switches B and C and continue, the pgm will go back to the F020 stop code to ask for initial options again.						
F027	Xmt line intf adr entered in stop code F026 was invalid line set type for running with options selected. Enter xmt line intf adr again as defined in stop code F026. If you enter FF in switches B and C and then continue, the pgm will go back to the F020 stop code to ask for initial options again.						
F028	Enter SDLC station adr in switches D and E. This is the SDLC station adr put into all test frames xmt on the line and the SDLC station adr that this station expects to rcv from the remote secondary station if the primary station option was selected. If you have selected the secondary station option, this will be the SDLC station adr searched for in all incoming frames and the SDLC station adr put into the response test frames or frame reject response sent back to the remote primary station. If the secondary station rcv a frame that has a different SDLC station adr than the one you are entering, it will not respond to that frame but will count it in the statistics counters defined in the rtn X6F0 write-up in the "CSB Symptom Index." After you continue from this code, the pgm will reset and enable the scanner and start the link test. See the appropriate rtn write-up in "CSB Symptom Index" for display codes you will get while the test is running.						
F029	Enter the line adr of the auto-call originate the line intf to be used in this test. See manual intervention stop code F001 for format to be used for entering the line adr. **Note:** If the line adr entered is either invalid or not configured as an auto-call originated line, this stop code will be displayed again. Enter line adr again as defined for this stop code.						
F02A	Enter the first digit to be dialed on the auto-call originate line. Set switch D to 0 and switch E to the next digit to be dialed. Press START.						

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments

F02B

Enter the next digit to be dialed. Set switch D to 0 and switch E to the next digit to be dialed. Press START. Continue entering digits in this manner; after the last digit has been entered, set switches D and E to FF and press START.

The pgm will not reset, enable the scanner, and start the link test. Wait for normal connection or time-out (20 sec) to occur. If normal connection occurs, each dial digit will be displayed in DISPLAY B, byte 1, as it is dialed.

F02C

Link test has terminated. If necessary, check statistics and reg indicators defined in the heading of the appropriate rtn in "CSB Symptom Index". Then enter a link test restart or termination option.

The following list of options are acceptable with switches B and C set to D0 or 00 for this F02C stop code. The same options may be used with the D0 settings when using the dynamic communications options defined in the appropriate rtn write-up in "CSB Symptom Index". Following is a list of the restart/termination options:

Set switches B C, D, and E to	*For this restart/terminate option*
D000	Restart the link test at point where it set up initial xmt and rcv operations without doing a scanner reset and enable operation. This option allows you to restart the test on a switched line without making a new dialed connection, but this option may be used on any type of restart except a scanner or LIB failure. If you use this restart option, all the statistics counters will be cleared (except the number of frames to xmt), and run indicators will be reset to starting options.
D001	Restart rtn at stop code F020 asking for the link test options. This restart option will mask L2 irpt and mess up xmt and rcv buffer pointers but will not modify any of the other link test statistics; it will not reset the lines currently in use until after you have entered your new options. Therefore, this option may be used to terminate the current test but you will still be able to look at test statistics or be able to respecify options.
D002	Restart the link test from hardware reset and enable in the scanner. This option will clear all run indicators and statistics as in option D000; but, in addition, it will disconnect any switched-line connection due to the scanner reset and enable. This restart option should be used if a scanner or LIB failure occurred or if you did any outputs from the control panel that changed the current line conditions.
D003	Go to stop code F02C and wait for next selection of options. This stop code is used for dynamic communications (function select FUNCTION 1 and D003 in switches B-E). If used at F02C stop code, it will result in stop F02C again. This dynamic communications may be used to terminate the test before the xmt frame count is reached for the primary station or to terminate the secondary station when nothing is being rcv (indicated by E061 display code being displayed continuously).
D004	Terminate rtn after resetting scanner. This option should be used when you have finished testing with the link test. This will terminate the link test rtn and if you have not set the CE sense switches to cycle on request or if you are not running multiple IFTs or adapters, the DCM will produce a DISPLAY B stop code of 80nn asking for your next test request.

F030

Enter xmt, rcv, wrap, or dial option.

Enter in switches B-E your selected option. Options are:

0001	Xmt test on a nonswitched line or local attachment.
0002	Rcv test on a nonswitched line or local attachment.
0003	Wrap a pair of nonswitched or local lines.
0004	Xmt test on a switched line using manual dialing and line connection.
0005	Rcv test on a switched line using manual dialing and line connection.
0006	Wrap a pair of switched lines using manual and line connection.
0007	Dial numbers on an auto-call originate line intf and then xmt on the attached switched line intf.
0008	Wrap data on switched lines. This option will: • Dial numbers on an auto-call originate intf. • Answer the call on a switched line intf. • Go into rcv mode on the line intf that answered the call. • Xmt on the line intf attached to the auto-call originate line intf to the rcv line.
0009	Dial numbers continuously on an auto-call originate line intf.
000A	Dial numbers on an auto-call originate line intf; xmt an alternate all-0's and all-1's char pattern for 128 char; and then disconnect the line adr.

F031

Enter the line adr of the auto-call originate line intf to be used in this test. See manual intervention stop code F001 for the format to be used for entering the line adr.

F032

The line adr entered is either invalid or not configured as an auto-call originate line. Enter the line adr again as defined in stop code manual intervention F031.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments

F033

Enter the first digit to be dialed on the auto-call originate line.

Set switch D to 0 and switch E to the digit to be dialed. The digit to be dialed may be 0 through 9 for dial digits, C for the end-of-numbers char, or D for the separator char. Because the end-of-numbers and separator char are not supported by most IBM and non-IBM auto-call units in the U.S.A., they should be used with caution. At this time, reg X'13' points to a location in storage where you (as an option) may store up to 32 bytes of dial digits; you can then set switches C and D to FF and press the START pushbutton to continue. If you select this option to store the dial digits, the first 4 bits of each byte should be 0 and the last 4 bits should be the dial digit, and you should store a X'FF' char after the last digit to be dialed. If you make any errors in entering any dial digits, you will be asked to enter the first dial digit again. If you used the end-of-numbers char, it must be the last digit entered.

F034

Enter the next digit to be dialed.

Set switch D to 0 and switch E to the digit to dial, or set switches D and E to FF if the last digit to dial was entered previously. See manual intervention stop code F033 for caution on dial digits and optional use of reg X'13' storage adr, which you may still use as an option. After you have entered the dial digits, the digits will be validated; if any digit is invalid, you will be asked to enter the first dial digit again. This manual intervention code may be repeated up to 31 times to get a total of 32 digits.

F035

Enter the xmt line adr to be used in this test. See manual intervention stop code F001 for format to use.

F036

The xmt line adr entered is invalid or not configured as a line that can run in xmt mode. Enter the xmt line adr again as defined in manual intervention stop code F035.

F037

The xmt line adr entered cannot be used with the switched line and/or auto-call originate test option you selected. Enter the xmt line adr again as defined in manual intervention stop code F035.

F038

Enter LCD and set mode bits for xmt line. Set switch B to the line control definer (LCD) wanted.

Set hex:

0	For S/S 9/6 line control which has one start bit, 6 data bits and 2 stop bits
2	For S/S 8/5 line control
4	For S/S 9/7 line control
5	For S/S 10/7 line control
6	For S/S 10/8 line control
7	For S/S 11/8 line control
8	For DLC 7-bit char line control
9	For DLC 8-bit char line control
A	For DLC 6-bit char line control
B	For DLC 5-bit char line control
C	For BSC EBCDIC line control
D	For BSC ASCII line control

Note: Do not use LCD = 0, 2, 5, or 7 when xmt and rcv (wrap) all 0's is selected because an error may occur, indicating more char were rcv than were xmt. Do not use LCD = 4 or 6 when xmt on a line set that can detect a rcv break by the 'stop bit check' because you may get error stops, indicating ICW bits 0-3 are in error with the 'stop bit check' bit being on.

Set switch C to 0.

Set switches D and E to the hexadecimal sum of the following bit definitions. The 8 bits obtained are used to set SDF bits 2-9 (ICW bits 26-33) during the set mode operation.

Switch D:

Hex

8	This bit is reserved and should be 0.
4	Diagnostic mode latch is set if this bit is a 1. This bit should normally be a 0 to test normal modem operation. If this bit is a 1 and the set 'DTR' bit is a 1, the modem test lead will be activated in IBM integrated modems. When the 'diagnostic mode' bit is set on, that CS hardware forces on a 'DSR' and may force 'CTS' indication according to the line status. This bit should be 0 for all auto-call originate and switched line test options.
2	Set 'DTR' if this bit is a 1. This bit should normally be a 1 to test modems. If you select to do an internal xmt or wrap operation, this bit should be a 0, and the 'diagnostic mode' bit should be a 1.
1	'Sync bit clock latch' is set if this bit is a 1. This bit should normally be a 0 for S/S line control and a 1 for sync and BSC line control. With some special features, this bit may control other than the clocking method.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments

F038

Switch E:

Hex

8 'External clock' latch is set if this bit is a 1. If this bit is 0, an internal clock is used. For proper modem operation, some modems require that external clock be used. If you set this bit to 1 to select external clock, you should set the two 'oscillator select' bits to 0. If you set the 'diagnostic mode' bit to a 1, this bit should be a 0 except for the case where IBM integrated modems that provide external clock are put in test mode by having both the 'diagnostic mode' and 'DTR' bits set to 1.

4 'Data rate select' latch is set on if this bit is a 1. On modems that provide operational speeds, this bit being on should select the higher of the two speeds. The 'data rate select' latch may be used for other purposes on some line sets. An example is the EIA local line set type 1F where it drives the local attachments 'rcv line signal detect' lead.

2 and 1 Oscillator select bits used to select one of 4 possible oscillators. These bits may be set to 00, 01, 10, or 11 to select the 1st, 2nd, 3rd, or 4th oscillator position. The 1st oscillator is required to be the lowest speed oscillator. You should use caution in selecting the 2nd, 3rd, or 4th oscillator since that oscillator may not be installed or may exceed the maximum allowable operating speed of the line set under test. The 'oscillator select' bits should be set to 00 if you have the 'external clock' bit set to 1.

F039 LCD entered for xmt line is invalid or the xmt line set type cannot run with the LCD type selected. Enter LCD and set mode bits again as in manual intervention stop code F038.

F03A Enter the rcv line adr to be used in this test. See manual intervention stop code F001 for format to be used for entering adr.

F03B The rcv line adr entered is invalid or not configured as a line set type that can run in rcv mode. Enter the rcv line adr again as in manual intervention stop code F03A.

F03C The rcv line adr entered cannot be used with the switched line and/or auto-call originate test option selected. Enter the rcv line adr again as in manual intervention stop code F03A. This error will also occur if a wrap option was selected and the rcv line cannot run with the xmt line LCD or set mode options.

F03D Enter LCD and set mode bits for rcv line. See manual intervention stop code F038 for format to enter LCD and set mode bits.

F03E LCD entered for rcv line is invalid; the rcv line set type cannot run with the LCD type selected; or, for wrap options, the LCD selected is not the same as the xmt LCD. Enter the LCD and set mode bits for the rcv line again. See manual intervention stop code F038 for format.

F040 Enter xmt data options and/or first data char to xmt. All data char are xmt as entered with bit 7 xmt first, then bit 6, then bit 5, etc. The char are xmt from the first entered to the last entered, and then the same char pattern is repeated continuously until the test is terminated. If you select the option to xmt all marks (1 bits) or all spaces (0 bits), any data char entered are ignored.

Set switch B to the hexadecimal sum of the following options:

Hex

8 Xmt in NRZI mode if a DLC LCD is selected.

4 All 1 bits (marks) are xmt if this bit is a 1. For S/S the pad flag will be set on to suppress the start bit, and data char of all 1 bits will be xmt. For DLC, the 'disable stuffer' bit will be set on to suppress the 0 bit insert function, and data char of all 1 bits will be xmt. Note that this xmt-all-1's options is intended for modem equalization functions and cannot detect a failure such as an open xmt data lead. You should wrap data using some char with both 0 and 1 bits for a better exercise of the modem or telecommunication line.

2 Xmt all 0's. For S/S LCDs, two pad char of all 1 bits are xmt and then the xmt line's PCF is set to 'A' to suppress stop bits, and all 0 bits are xmt. For other LCDs, all 0 bits are xmt without any SYN or flag char.

1 Xmt all 1's in DLC mode without setting the 'disable stuffer' bit so 0-bit insertion will operate. This option will work only if a DLC LCD is selected.

Set Switch C to the hexadecimal sum of the following options:

Hex

8 Ignore ICW 0-3 if this bit is a 1. Otherwise, after every xmt, line char-svc ICW bits 0-3 are checked; and, if any of these bits are in error, an error code is displayed.

4 Reserved. Set to 0.

2 Xmt DLC link test. This bit is ignored unless you selected a DLC LCD or the xmt-all-1's, the xmt-all-0's or the xmt-DLC-all-1's options.

3705-80 CSB IFT MANUAL INTERVENTION STOPS - Cont.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments

F040

Hex

1 Alternate data input option if this bit is a 1. If you set this bit to 0, set switches D and E to the 1st char to be xmt, select FUNCTION 5, and press the START pushbutton; you will get manual intervention stop code F041 asking for next data char to xmt. If you want to use the alternate data input option, do the following:

a. Get storage adr from reg X'13'

b. Store the count of the number of char to be xmt as the first char. The highest valid count is X'78' to xmt 120 char. The pgm will xmt this number of char, go back to the first char, and repeat the same number of char continuously until the test is terminated.

c. Store up to 120 consecutive char after the count byte. The char to be xmt are put in the PDF in the same format in which you store them except that bit 0, bits 0 and 1, or bits 0, 1, and 2 may be cleared. If you selected LCD4, 5, or 8, the char you store will all have the 0 bit set to 0 since these are all 7-bit char LCDs. If you selected LCD 0 or A, bits 0 and 1 will be set to 00. If you selected LCD 2 or B, bits 0, 1, and 2 will be set to 000.

d. Set switch B to 0.

e. Set switch C to 1 or 9 (according to the ignore-ICW-bits 0-3 option) to indicate this alternate data input is being used.

f. Select FUNCTION 5 and press the START pushbutton.

Set switches D and E to the first char to be xmt unless you selected the alternate data input format or the xmt-all-1's or the xmt-all-0's option in that case, switches D and E are ignored.

F041

Enter next char to be xmt.

Set switches B and C to 00 and switches D and E to the next char to be xmt, or set switch B or C to any nonzero position if the last char has been entered previously. At this time, reg X'13' contains an adr pointing to a storage location that contains a byte that has the number of char you have previously entered, followed by the char you have entered. You may (as an option) use the alternate data input steps a, b, and c defined in manual intervention stop code F040. Then set switch B to C to a nonzero position, select FUNCTION 5, and press the START pushbutton.

F042

Enter rcv data options. If you are wrapping data, the rcv data char are compared with the xmt char selected unless you selected the rcv-all-1's, rcv-all-0's, DLC-link-test, or ignore-rcv-irpt options. If you are doing a rcv-only test and have not selected one of the above options, the rcv data char are ignored, but you may display the last data char rcv by displaying reg X'44' (byte 1) while the pgm is running. If you selected a sync LCD (8, 9, A, B, C, or D) and did not select one of the above options, there will be no indication of any data being rcv unless a valid synchronizing char for the LCD in use is rcv.

Note: When using a wrap option for either xmt all 1's, xmt all 0's, DLC all 1's, or DLC link test, you should select the same rcv data option or error stops may occur.

Set switch B to the hexadecimal sum of the following options:

Hex

8 Rcv in NRZI mode if this bit is a 1 and if you selected a DLC LCD.

4 All 1 bits are expected to be rcv if this bit is a 1. If this bit is a 1 and all 1 bits are not rcv, an error will be reported. Note that this rcv-all-1's option, which is intended to be used for modem equalization, cannot detect a failure such as an 'open rcv data' lead or a 'rcv data' lead clamping problem. You should wrap some data char containing both 0 and 1 bits for a complete exercise of the modems or telecommunication line.

2 All 0 bits are expected to be rcv. If this bit is a 1 and all 0 bits are not rcv, an error is reported.

1 Ignore all rcv char-svc irpt. If this bit is a 0 and you have selected one of the wrap options and all 1's and all 0's options are 0, a check is made that char rcv are the same as char xmt.

Set switch C to the hexadecimal sum of the following options:

Hex

8 Ignore ICW bits 0-4 if this bit is a 1. If this bit is a 0 and the 'ignore all rcv char svc irpt' bit is a 0, ICW bits 0-4 are checked on every rcv char-svc irpt and an error is reported if they are in error.

4 Reserved. Set to 0.

2 Rcv DLC link test. This bit is ignored unless you selected a DLC LCD or if selected the rcv all 1's or the rcv all 0's options. If you select this option, rcv data errors are counted and displayed in the DISPLAY B indicator lights as an X'E0nn' code, where *nn* is the low-order byte of the rcv data error count. The total error count is always available in reg X'1B'. Note that it is common to get one or two errors when the rtn first starts rcv due to clock correction time and the DLC 1 bit counter circuit.

1 Reserved. Set to 0.

Set switches D and E to 00.

F049

Enter options for rtn X6F2; see X6F2 XXXX in "CSB Symptom Index' for selections.

3705-80 CSB IFT MANUAL INTERVENTION STOPS - Cont.

Routine	Error Code	Function Tested	Error Description	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
F050	Enter xmt line adr for rtn X6F2; see X6F2 XXXX in "CSB Symptom Index" for selections.						
F052	Enter the rcv line adr for rtn X6F2; see X6F2 XXXX in "CSB Symptom Index" for selections.						
F055	Enter options for rtn X6F4; see X6F4 XXXX in "CSB Symptom Index" for selections.						
F056	Enter the xmt line adr for rtn X6F4; see manual intervention stop code F001 for format.						
F057	Enter the rcv line adr for rtn X6F4; see stop code F001 for format.						
F058	Enter the high-speed local attachment oscillator frequency and line adr for rtn X6F5; see X6F5 XXXX in "CSB Symptom Index" for selections.						
F059	Disconnect the external wrap facility for rtn X6F4; see X6F4 XXXX in "CSB Symptom Index".						

Diagnostic Control Monitor (DCM)

The diagnostic control monitor (DCM) provides functions for:

- Routine selection
- Manual intervention routines
- Abort control
- Control panel interface
- Routine execution
- Error control information
- Scope synchronization
- Continuing from an error stop or a manual intervention stop

REQUIREMENTS

You must have the proper configuration data set (CDS) cataloged with the remainder of the system (for additional information, see the CDS section). Before IFT routines can run properly, the functional areas in the CCU hardware must be operational. These functional areas are tested by the ROS bootstrap program each time the LOAD pushbutton is pressed.

DCM EXECUTION

3705 Setup Procedures

1. Switch the 3705 power on.
2. Set both the MODE SELECT and DIAGNOSTIC CONTROL switches to the PROCESS position.
3. Enable the appropriate channel interface.
4. Set the DISPLAY/FUNCTION SELECT switch to the STATUS position to load the DCM. For information on using the other positions, see "How to Use the DISPLAY/FUNCTION SELECT Switch" later in this section.
5. Press the RESET pushbutton, then the LOAD pushbutton.
6. DISPLAY B bits 0.2 and 0.3 should be on indicating that ROS has reached IPL phase 3. The LOAD light is on; the following lights are off: HARDSTOP, TEST, WAIT, and PROGRAM STOP.

If the above conditions are not present, refer to the CE Panel Test in the CP section and the ROS Test in the ROS test section.

Host Procedures

Start the OLTEP or OLTSEP in the host processor. When OLTEP or OLTSEP causes a console printer message of:

r ID 'ENTER DEV/TEST/OPT/'

you enter:

r ID,'XXX/3705A/nfe,ext=ABCD/'

where:

XXX = the channel and unit address of the 3705 (native attachment address).

ABCD = four operating options provided by the OLT and type 1 CA loaders. The correct entries are Y (for YES) or N (for NO). The options are defined as follows:

A = OLT bypass printing channel errors
B = Run INIT
C = Run type 1 CA loader with error checking
D = Bypass hard stop on type 1 CA loader error in 3705 and retry

If your response to the DEV/TEST/OPT/ message does not include the ext= parameter, the default value assumed is ext=nyyy (that is, ext=NO,YES,YES,YES).

Delay of INIT Execution: Before INIT begins executing, the 3705/host interface must be disabled. The type 1 CA loader attempts to disable the 3705 interface by issuing a diagnostic DISABLE command when INIT is loaded. The host 'clock out' line must drop before the 3705 can go offline. The host 'clock out' line will drop when either the host processor STOP pushbutton is pressed or when the host processor enters the wait state.

Operating situations under OS or DOS can result in maximum use of the processor that will delay the host from entering the wait state. During this delay, the OLT prints a message indicating that it is waiting for the 3705 to disable its channel interface. Also, at the 3705, an equivalent message code is displayed in the control panel lights.

TYPE 1 CA LOADER ERROR PRINTOUTS

Error printouts occur if the type 1 CA loader detects an error. The printout contains all the pertinent information about the error that can be obtained by the type 1 CA loader. The bypass printing channel errors option inhibits the error printout. For a description of the error printouts, refer to *DOS OLTEP SRL,* (GC24-5086), *IBM System/360 Operating System On-line Test Executive Program,* (GC28-6650), or *OLTSEP Operator's Guide,* (D99-SEPDT).

MESSAGES

Messages occur during operation of the type 1 CA loader that indicate: (1) the loader has detected an error or (2) an action is needed to load the diagnostic programs into 3705 storage. The messages, message explanations, and responses are as follows:

THE STATUS OF THE 3705 CANNOT BE DETERMINED. **WARNING** CONTINUATION WILL CAUSE THE ENTIRE 3705 TO BECOME UNAVAILABLE. ENTER 'C' TO CANCEL OR 'P' TO PROCEED.

Explanation: The OLT cannot determine the status (offline or stopped) of the 3705. If the OLT is allowed to continue, the program in 3705 storage will be destroyed.

Response: Continue by entering a C or P, as follows:

r id,'C' (for cancel)
or
r id,'P' (for proceed)

Any other response results in the program's repeating the last line of the above message. After five invalid responses, the message INVALID RESPONSE AFTER 5 REQUESTS is printed.

ALL 3705 ADDRESSES ARE NOT STOPPED OR OFFLINE. **WARNING** CONTINUATION WILL CAUSE THE ENTIRE 3705 TO BECOME UNAVAILABLE. ENTER 'C' TO CANCEL OR 'P' TO PROCEED, OR 'R' TO RETRY.

Explanation: The OLT has been notified by the executive driver that all 3705 addresses are not offline or stopped. If the OLT is allowed to continue, the program in 3705 storage will be destroyed.

Response: You have the opportunity to make all addresses available to the OLT using standard system facilities. Continue by entering a C, P, or R, as follows:

r id,'C' (for cancel)
or
r id,'P' (for proceed)
or
r id,'R' (for retry)

The difference between a P and an R response is (1) P means to proceed, regardless of the offline or online status of the 3705 address and (2) R means that the operator has been taking addresses offline and wants the program to verify that all units are now available to the OLT.

Any other response results in the program's repeating the last line of the above message. After five invalid responses, the message INVALID RESPONSE AFTER 5 REQUESTS is printed.

INVALID RESPONSE AFTER 5 REQUESTS

Explanation: The program assumed the response of 'C' and terminated the OLT.

Response: None.

BAD RC YY FROM XXXXXXX

Explanation: The type 1 CA loader has requested of the executive driver a function that the driver is incapable of performing. This may be because of an invalid parameter or an error that has occurred while the executive driver is performing the request. XXXXXXX is the name of the function being requested, and YY is the code returned by the executive program. The XXXXXXX field is filled by the type 1 CA loader.

Response: This message is a diagnostic programming aid. If the message occurs, a dump and other available information should be submitted with an APAR (Authorized Program Analysis Report).

The following messages are printed on the system output printer to describe failures and the operation that is being attempted when an error occurs:

BAD CC SIO

FAILED TO INTRPT

BAD STATUS ON SIO

NOP CMD FOR 3705 LOAD BUTTON
RD CMD FOR IFT REQ
WRT CMD TO WRITE DATA
WRT CMD FOR LAST BLOCK
WRT IPL CMD SENDING LOADER

WRT CMD SENDING CONTROL WORD

Explanation: If the DCM has already been loaded, the program indicates that you can make a request at the 3705. If the DCM has not been loaded, the program starts over by requesting you to press the LOAD pushbutton on the 3705.

Response: If DCM has been loaded, enter a request; otherwise press LOAD.

PRESS LOAD ON 3705

Explanation: This message occurs when the type 1 CA loader is initially started or if loss of control occurs. It constitutes the beginning of the type 1 CA loader and provides the synchronization between the 3705 and the host processor.

Response: Press the LOAD pushbutton on the 3705. This message repeats every 30 seconds until the LOAD pushbutton is pressed.

AWAITING 3705 INTERFACE DISABLE

Explanation: The type 1 CA loader has loaded INIT in the 3705 and is waiting for the 3705 to go offline. This message is repeated every 20 seconds until the 3705 channel interface is disabled and the 3705 begins executing the IFT.

If this message occurs continuously, the 3705 is either unable to go offline after the INIT has been loaded or unable to get back online after the INIT has completed execution. A processor-bound system can cause this problem.

Response: Pressing the STOP and then the START pushbuttons on the processor console drops the 'clock out' line long enough for the 3705 to go offline. Entering the wait state accomplishes this also.

ENTER IFT REQUEST AT 3705

Explanation: This message indicates that a request to load an IFT module can be entered.

Response: Enter an IFT request. See "How to Request an IFT" in this section.

3705 LOADED WITH IFT Z3705AAA
3705 LOADED WITH IFT Z3705ADA
3705 LOADED WITH IFT Z3705AEA

Explanation: These messages indicate that INIT or IFT modules have been successfully loaded in the 3705 without any errors being detected. Z3705AAA is the type 1 CA loader, Z3705ADA is the INIT section 1, and Z3705AEA is the INIT section 2.

Response: None.

ERP USED ON MOD Z3705XXX

Explanation: This message warns you that errors have occurred while loading the INIT or IFT modules. Each output operation to the 3705 is attempted up to 10 times if an error occurs (unless the OLT option EL [N] has been modified). If the operation being attempted is performed before the error count is exhausted, the OLT considers the data transfer successful and continues loading the INIT or IFT modules.

Response: Verify that the INIT or IFT modules are at the proper level.

Z3705XXX IN ERROR, ABORT LOAD

Explanation: The retry count (normally 10) is exhausted, and the error is still occurring. The type 1 CA loader assumes that loss of control has occurred and restarts at the beginning.

Response: Refer to the message "ERP USED ON MOD Z3705XXX".

WAITING FOR IFT COMPLETION

Explanation: This message occurs every 20 seconds after an IFT has been loaded in the 3705. Most of the IFTs disable the 3705. The type 1 CA loader is in a loop issuing NOP commands to the 3705. If it receives condition code 03, the 3705 interface is not enabled; it prints this message and waits another 20 seconds. When the 3705 is enabled, the type 1 CA loader continues executing.

Response: None.

INVALID PLINK MOD

Explanation: The type 1 CA loader has detected an error in the requested module. (An address in the module is on an odd boundary.) The type 1 CA loader returns to the Read command to allow you to enter another request at the 3705.

Response: Enter another request.

MOD Z3705XXX NOT IN OLTLIB

Explanation: The type 1 CA loader has received an IFT request (through a Read command) for a module that is not in OLTLIB. The type 1 CA loader returns to the Read command to allow you to enter another request at the 3705.

Response: Enter another request. However, if the original request was valid, the IFT module name must be added to the OLTEP/OLTSEP library before the IFT can be loaded.

DESCRIPTION OF DCM FUNCTIONS

Routine Selection

The routine selection facility allows you to select:

- One routine of one IFT for either one adapter or all of the adapters tested by the IFT.
- All of the routines of all IFTs for either one adapter or all of the adapters tested by the IFT.
- All of the routines of all the IFTs for all of the adapters.
- Manual intervention routines. The CE sense switch, "include manual intervention routines", controls this option.
- Problem definition routines. The CE sense switch, "problem definition mode", controls this option.
- Repeating a routine up to 256 times before the next routine is executed. The CE sense switch, "repeat each routine X times", controls this option. If this option is not selected, the routines are executed one time sequentially. X can be displayed and set from the panel and is specified as a decimal number in the range 1-256. If X is not specified, the default value assumed is 128. (See "Set or Display Repeat Count" later in this section.)
- Continuously cycling the entire IFT request, either for one routine or for all the routines. The CE sense switch, "cycle on request", controls this option.
- Stopping before the execution of each routine in order to prepare for the execution of the routine. For example, this option allows you to set up an address compare stop for a location within the routine. Panel utilities can also be used at this time. The CE sense switch, "halt before execution", controls this option.

Manual Intervention Routines

You can include manual intervention routines in an IFT request by setting the CE sense switch "include manual intervention routines" (see "How to Perform an IFT Request" in the IFT section).

After a manual intervention stop occurs:

- DISPLAY A will contain: (1) the adapter number in byte 0, bits 0-3, (2) the IFT number in byte 0, bits 4-7, and (3) the routine number in byte 1, bits 0-7.
- DISPLAY B will contain a manual intervention stop code (X'FXXX') which you use to look up an entry in the appropriate IFT symptom index. (X'F' in byte 0, bits 0-3 indicates a manual intervention stop occurred.) The appropriate IFT symptom index entry will tell you what action to take. (XXX indicates the manual intervention stop to reference.)

Abort Control

The abort control facility is used to abort or terminate the current routine or the entire IFT request.

To abort a request or routine:

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see "Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 6.
3. Set STORAGE ADDRESS/REGISTER DATA switches B, C, D, and E as follows:
   a. To abort a routine: set any one of the switches to a value other than X'F'.

b. To abort a request: set all of the switches to X'F'.

4. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.

Control Panel Interface

The DCM uses the DISPLAY A and DISPLAY B indicators on the control panel to display:

Adapter, IFT, and routine numbers
IFT symptom index routine and error codes
IFT routine manual intervention codes
DCM operator codes
DCM error codes
Panel utility displays

Note: Unless byte X is specified in the symptom index for a specific error, references to DISPLAY A and DISPLAY B are for bytes 0 and 1 only.

The DCM routines allow you to select the panel utilities and to also enter manual intervention data (for example, set, reset, or display the CE sense switches).

- After an error stop or manual intervention stop, DISPLAY A will display:
  - the adapter number in byte 0, bits 0-3
  - the IFT number in byte 0, bits 4-7
  - the routine number in byte 1, bits 0-7
- After a manual intervention stop, DISPLAY B will display:
  - X'F' in byte 0, bits 0-3, indicating that manual intervention is required. Byte 1, bits 0-7 will indicate the manual intervention stop that you should reference.
- After an error stop, DISPLAY B will display:
  - Either X'0', X'1', X'2', or X'3' in byte 0, bits 0-3 (0 indicates an error stop unique to one routine, 1, 2, or 3 indicates an error stop common to many routines)
  - a loop count in byte 0, bits 4-7
  - the error code in byte 1, bits 0-7
- For DCM operator or error codes:
  - DISPLAY A will display either X'0000' or X'FFFF'.
  - DISPLAY B will display X'8' in byte 0, bits 0-3 and the error code in byte 1, bits 0-7.

Panel utility displays are variable depending upon the control panel switch settings.

Routine Execution

The routines are executed sequentially, by section. For example, if IFT 6 has two sections and tests two adapters, the sequence is:

Adapter 1, IFT 6, Section 1
Adapter 2, IFT 6, Section 1
Adapter 1, IFT 6, Section 2
Adapter 2, IFT 6, Section 2

At the beginning of each routine, the DCM displays the following information:

DISPLAY A Byte 0,
Bits 0-3 = Number of the adapter being tested
Bits 4-7 = Number of the IFT being executed

DISPLAY A Byte 1,
Bits 0-7 = Number of the routine being executed

DISPLAY B Byte 0,
Bits 0-4 = 0
Bits 5-7 = Low order three bits of the error counter

DISPLAY B Byte 1,
Bits 0-7 = Zeros

At the completion of a request, the display indicates that the request was either completed with no errors detected, completed with errors detected, or aborted.

Error Control Information

The DCM stops and displays error codes for detected errors. The error codes are listed in the appropriate symptom index (DCM, IFT, etc.) Other error information, which may be available in registers or storage locations, is also shown in the appropriate symptom index.

The DCM allows you to bypass an error stop when a failure is detected by setting the "bypass error stop" CE sense switch. The error code is displayed even if the stop is bypassed.

The DCM allows you to select a particular error on which to loop. Two loop options are available: (1) the "loop on first error" option causes the smallest possible loop internal to the routine and (2) the "restart routine on first error" option restarts the current routine when the first error occurs. The scoping loop continues whether or not the error occurs again. The CE sense switches, "loop on first error" and "restart routine on first error", control these options.

The DCM stops and displays error codes for any new failure while it is in a scoping loop. However, the DCM allows you to bypass the error stop when a new failure is detected while the DCM is in a loop. The error code for the new error is not displayed because it would interfere with the original error code display. The CE Sense switch, "bypass new error stops", controls this option.

Failures detected in a pretest routine block automatically cause looping in the pretest block. This prevents execution of the routine without the proper setup; therefore, the scope picture for the test function of the routine is traced only when the setup is proper.

The DCM increments an error counter when a failure is detected. The counter range is from 0 to 127, with an overflow indicator. The low-order three bits of this counter are shown in the error count display in DISPLAY B. The counter is reset to zero for each new request.

Scope Synchronization

The DCM controls scope sync pulses on three test pins.

- Scope sync point 1 (01A-B3M2P10, ALD page CU015): a pulse is emitted from sync point 1 at (1) the beginning of each routine or (2) when the hardware setup block is entered, if the DCM is in a scoping loop.
- Scope sync point 2 (01A-B3M2P13, ALD page CU015): A pulse is emitted from sync point 2 at the beginning of the test function within a test routine.
- Address compare scope sync point (01A-B3P2S09, ALD page CU004): A pulse is emitted from the address compare sync point when an address used for a fetch or store (controlled by the STORE COMPARE LOAD switch) matches the address set in the STORAGE ADDRESS/REGISTER DATA switches. This pulse is used to sync on any storage location in any IFT routine or the DCM. Set the address of an instruction used in the routine (or function) in the STORAGE ADDRESS/REGISTER DATA switches. When the instruction is executed, the address compare sync pulse is emitted.

Test pins 1 and 2 can be used together to count the number of test functions performed. Test point 1 is used to trigger the scope using delayed sweep. Each pulse emitted from test point 2 then represents one test function.

For information on setting up a scoping loop, see "Setting Up a Scoping Loop" in this section.

Continuing From an Error Stop or Manual Intervention Stop

The continue function allows you continue a routine from the point of an error stop or manual intervention stop. It also allows you to enter input data to the test routine (if required). Before you can use this function, DISPLAY A and DISPLAY B must indicate either a DCM stop code, an error stop code, or a manual intervention stop code.

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see "Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. If the code in the displays is for manual intervention (DISPLAY B byte 0=X'FX'), set the STORAGE ADDRESS/REGISTER DATA switches as specified in the appropriate symptom index for the IFT being run.
3. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5.
4. Press the START pushbutton.
5. DISPLAY B is set to zeros however, it may not display the zeros long enough for you to see them.

HOW TO USE PANEL UTILITIES

The panel utilities allow you to perform various DCM utility functions such as setting or resetting CE switches, displaying storage, and displaying the contents of registers. You can use the panel utilities only if the DCM is executing in the 3705.

The DCM overrides panel utility displays if a routine that is being executed requires a display. (for example displays required for manual intervention routines and error stops override panel utility displays).

The sections that follow describe the panel utilities and how to run them.

Refresh the Last DCM Display Code

This panel utility restores DISPLAY A and DISPLAY B to the last code displayed by the DCM (excluding displays made by panel utilities).

If another panel utility is active, this panel utility cannot be executed. See "Stop Panel Utility" later in this section.

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see "Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. Set the DISPLAY/FUNCTION switch to FUNCTION 1.
3. Set STORAGE ADDRESS/REGISTER DATA switch B to X'0'.
4. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
5. DISPLAY A and DISPLAY B will contain the codes last displayed by the DCM.

Continuous Display Without Test

This panel utility displays the contents of a specified storage location or register. The data displayed is not tested for any special conditions. The data display occurs at each timer interrupt (approximately 10 times per second).

The data display is bypassed if the DCM is stopped for an error stop, manual intervention stop, or DCM code, or if the DISPLAY/FUNCTION SELECT switch is not set to FUNCTION 1, 2, or 3.

If another panel utility is active, this panel utility cannot be executed. See "Stop Panel Utility" later in this section.

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see "Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1.
3. Set the STORAGE ADDRESS/REGISTER DATA switch B to X'2'.
4. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
5. DISPLAY A should be X'0000' and DISPLAY B should be X'8066'. For other values, see the appropriate IFT symptom index in the IFT section.
6. Select the type of display:
   a. For a storage display, set the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.
   b. For a register display, set the DISPLAY/FUNCTION SELECT switch to REGISTER ADDRESS.
7. Select the address or register to display:
   a. For a storage display, set the storage address in STORAGE ADDRESS/REGISTER DATA switches A, B, C, D, and E.
   b. For a register display, set the register number in STORAGE ADDRESS/REGISTER DATA switches B and D.
8. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
9. DISPLAY A should be X'0000' and DISPLAY B should be X'8068'. For other values, see the appropriate IFT symptom index.
10. If the HARD STOP light is on, set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5 and press the START pushbutton to continue. Otherwise, do as requested for the original stop code.
11. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1, 2, or 3. The data will be displayed during each timer interrupt until the utility is stopped (see "Stop Panel Utility" later in this section).

Continuous Display With Test

This panel utility displays the contents of a specified storage location or register. The data displayed will be tested for special conditions which you select. The data display occurs at each timer interrupt (approximately 10 times per second).

The displayed data is tested with a mask and an expected bit pattern. A single bit or any number of the displayed data bits can be tested. For each bit position that is to be tested, the corresponding bit position in the mask is set to a 1. The mask is ANDed with the data and the result is exclusive ORed with the expected data. If the result is not zero, a hard stop occurs. (To continue after such a hard stop, see "Continuing from an Error Stop or Manual Intervention Stop" earlier in this section.)

Although the display function can be bypassed because of the DISPLAY/FUNCTION SELECT switch position or a stop code display, the test data function is performed as long as the utility is active.

The display is bypassed if the DCM is stopped for an error stop, manual intervention stop, or DCM code, or if the DISPLAY/FUNCTION SELECT switch is not set to FUNCTION 1, 2, or 3.

If another panel utility is active, this panel utility cannot be executed. See "Stop Panel Utility" later in this section.

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see "Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1.
3. Set the STORAGE ADDRESS/REGISTER DATA switch B to X'3'.
4. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
5. DISPLAY A should be X'0000' and DISPLAY B should be X'8064'. For other values, see the appropriate IFT symptom index.
6. Enter the mask to be used to test the data in STORAGE ADDRESS/REGISTER DATA switches B,C,D, and E.
7. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
8. DISPLAY A should be X'0000' and DISPLAY B should be '8065'. For other values, see the appropriate IFT symptom index.
9. Enter the expected data in the STORAGE ADDRESS/REGISTER DATA switches B,C,D, and E.
10. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
11. DISPLAY A should be X'0000' and DISPLAY B should be X'8066'. For other values, see the appropriate IFT symptom index.
12. Select the type of display:
    a. For a storage display, set the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.
    b. For a register display, set the DISPLAY/FUNCTION SELECT switch to REGISTER ADDRESS.
13. Select the address or register to display:
    a. For a storage display, set the storage address in STORAGE ADDRESS/REGISTER DATA switches A, B, C, D, and E.
    b. For a register display, set the register number in STORAGE ADDRESS/REGISTER DATA switches B and D.
14. If the HARD STOP light is on, press the START push button otherwise press the INTERRUPT push button.
15. If the HARD STOP light is on, set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5 and press the START pushbutton to continue. Otherwise, do as requested for the original stop code.
16. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1, 2, or 3. The data will be displayed during each timer interrupt until the panel utility is stopped (see "Stop Panel Utility" later in this section).

For example: Assume that you want to continuously display the contents of storage location X'1888' and you want to hard stop if byte 0 bit 0 at storage location X'1888' is a 1.

1. For step 6 above, you would set X'8000' (mask= 1000 0000 0000 0000) in STORAGE ADDRESS/REGISTER DATA switches B,C,D, and E. This is the mask; the 1 bit indicates which position of the data that will be tested for a 1 bit.
2. For step 9 above, you would set the bit position that you want tested to zero. In this example, set STORAGE ADDRESS/REGISTER DATA switches B,C,D, and E to X'0000' (0000 0000 0000 0000). (Note that setting switches B, C, D, and E to any value in which bit 0 of switch B is a zero will work; for example X'7FFF' (0111 1111 1111 1111.)
3. For step 12 above, you would set the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.
4. For step 13 above, you would set the STORAGE ADDRESS/REGISTER DATA switches to X'1888' (the address of the storage location).

Address Compare Display Without Test

This panel utility displays the contents of a specified storage location or register address when an address compare interrupt occurs. The data displayed is not tested for any special conditions. (Refer to "LOAD/STORE ADDRESS COMPARE Switch" in the CTRL PNL section of Volume 2.

The display is bypassed if the DCM is stopped for an error stop, manual intervention stop, DCM code, or if the DISPLAY/FUNCTION SELECT switch is not in FUNCTION 1, 2, or 3.

If another panel utility is active, this panel utility cannot be executed. See "Stop Panel Utility" later in this section.

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see "Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1.
3. Set the STORAGE ADDRESS/REGISTER DATA switch B to X'4'.
4. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
5. DISPLAY A should be X'0000' and DISPLAY B should be X'8066'. For other values, see the appropriate IFT symptom index in the IFT section.
6. Select the type of display:
   a. For a storage display, set the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.
   b. For a register display, set the DISPLAY/FUNCTION SELECT switch to REGISTER ADDRESS.
7. Select the address or register to display:
   a. For a storage display, set the storage address in STORAGE ADDRESS/REGISTER DATA switches A, B, C, D, and E.
   b. For a register display, set the register number in STORAGE ADDRESS/REGISTER DATA switches B and D.
8. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
9. DISPLAY A should be X'0000' and DISPLAY B should be X'8068'. For other values, see the appropriate IFT symptom indexes in the IFT section.
10. If the HARD STOP light is on, set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5 and press the START pushbutton to continue. Otherwise, do as requested for the original stop code.
11. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1, 2, or 3. The data will be displayed during each timer interrupt until the panel utility is stopped (see "Stop Panel Utility" later in this section).
12. Set up for either a LOAD or a STORE address compare operation (set the STORE COMPARE LOAD switch to either STORE or LOAD).
13. Set the STORAGE ADDRESS/REGISTER DATA switches to the storage address where the compare is to be made.
14. Set the MODE SELECT switch to ADDRESS COMPARE INTERRUPT. When an address compare interrupt occurs, the data stored at that address or register will be displayed. The display can be stopped and started with the MODE SELECT switch.

Address Compare Display With Test

This panel utility displays the contents of a specified storage location or register address when an address compare interrupt occurs.

The data that is displayed is tested with a "mask and expected bit" pattern (a single bit or a number of bits of data may be tested). If the data is not equal to the expected data, the DCM makes a hard stop. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5 and press the START pushbutton to continue.

The display is bypassed if the DCM is stopped for either an error stop, manual intervention stop, a DCM code, or if the DISPLAY/FUNCTION SELECT switch is not set to FUNCTION 1, 2, or 3.

If another panel utility is active, this panel utility cannot be executed. See "Stop Panel Utility" later in this section.

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see "Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1.
3. Set the STORAGE ADDRESS/REGISTER DATA switch B to X'5'.
4. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
5. DISPLAY A should be X'0000' and DISPLAY B should be X'8064'. For other values, see the appropriate IFT symptom index.
6. Enter the mask to be used to test the data in STORAGE ADDRESS/REGISTER DATA switches B,C,D, and E.
7. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
8. DISPLAY A should be X'0000' and DISPLAY B should be '8065'. For other values, see the appropriate IFT symptom index.
9. Enter the expected data in the STORAGE ADDRESS/REGISTER DATA switches B,C,D, and E.
10. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
11. DISPLAY A should be X'0000' and DISPLAY B should be X'8066'. For other values, see the appropriate IFT symptom index.
12. Select the type of display:
    a. For a storage display, set the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.
    b. For a register display, set the DISPLAY/FUNCTION SELECT switch to REGISTER ADDRESS.
13. Select the address or register to display:
    a. For a storage display, set the storage address in STORAGE ADDRESS/REGISTER DATA switches A, B, C, D, and E.
    b. For a register display, set the register number in STORAGE ADDRESS/REGISTER DATA switches B and D.
14. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
15. DISPLAY A should be X'0000' and DISPLAY B should be X'8068'. For other values, see the appropriate IFT symptom indexes in the IFT section.
16. If the HARD STOP light is on, set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5 and press the START pushbutton to continue; otherwise do as requested for the original stop code.
17. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1, 2, or 3 to make the display active during each timer interrupt until the panel utility is stopped (see "Stop Panel Utility" later in this section).
18. Set up for either a LOAD or a STORE address compare operation (set the STORE COMPARE LOAD switch to either STORE or LOAD).
19. Set the STORAGE ADDRESS/REGISTER DATA switches to the storage address where the compare is to be made.
20. Set the MODE SELECT switch to ADDRESS COMPARE INTERRUPT. When an address compare interrupt occurs, the data stored at that address or register will be displayed. The display can be stopped and started with the MODE SELECT switch.

For example: Assume that you want to display the contents of register X'15' after the instruction X'1924' has been executed and to make a hard stop if bits 1.1 and 1.2 of register X'15' are zero.

1. For step 6 above, you would set X'0060' (mask= 0000 0000 0110 0000) in STORAGE ADDRESS/REGISTER DATA switches B,C,D, and E. This is the mask; the 1 bit indicates which position of the displayed data that will be tested for a 1 bit
2. For step 9 above, you would set the bit positions that you want tested to ones. In this example, set STORAGE ADDRESS/REGISTER DATA switches B,C,D, and E to X'0060' (0000 0000 0110 0000). (Note that setting switches B, C, D, and E to any value in which bits 1 and 2 of switch C is a one will work; for example X'FFFF' (1111 1111 1111 1111.))
3. For step 12 above, you would set the DISPLAY/FUNCTION switch to REGISTER ADDRESS.
4. For step 13 above, you would set the STORAGE ADDRESS/REGISTER DATA switches to X'1050' (register X'15').
5. Set up for either a LOAD or a STORE address compare operation (set the STORE COMPARE LOAD switch to either STORE or LOAD).
6. Set the STORAGE ADDRESS/REGISTER DATA switches to the storage address where the compare is to be made.
7. Set the MODE SELECT switch to ADDRESS COMPARE INTERRUPT. When an address compare interrupt occurs, the data stored in register X'15' will be displayed after the instruction at address X'1924' has been executed. The display can be stopped and started with the MODE SELECT switch.

Note: If the address compare interrupt is used, either in the 3705 DCM utilities or while running the 3705 Initial Test IFTs, unexpected errors may occur. Some of the tests cause intentional parity errors and CCU checks by means of an Output X'78' which affects the next

instruction cycle. Some of the tests are time dependent and the extra time needed to handle the address compare interrupt causes errors. The level 1 interrupt that occurs for the address interrupt may be reported as an error by some tests and may not cause errors in other tests depending upon when the address compare interrupt occurs.

Set or Display Repeat Count

This panel utility displays or changes the repeat count. The repeat count determines the number of times each routine is executed before proceeding to the next routine when the CE sense switch "repeat each routine X times" is set. Repeat count is entered in hex in the range X'00-FF' (decimal 0-255). 00 is treated as 256.

If another panel utility is active, this panel utility cannot be executed. See "Stop Panel Utility" later in this section.

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see "Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1.
3. Set the STORAGE ADDRESS/REGISTER DATA switches A, B, C, D, and E to the following positions:

```
                A B C D E

Set Count       - 6 - H H
Display Count   - 7 - - -

where:
 HH is the repeat count in hex.
```

- means the switch can be set to any position.

1. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
2. DISPLAY A should be X'0000' and DISPLAY B should be X'60HH' or X'70HH', where HH is the value of the repeat count. For other values, see the appropriate IFT symptom index.
3. To continue if the HARD STOP light is on, set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5 and press the START pushbutton.

Set, Reset, or Display CE Sense Switches

This panel utility allows you to set and reset the CE sense switches, which control execution of the IFTs, using the STORAGE ADDRESS/REGISTER DATA SWITCHES. The CE sense switches can also be set when you perform part 2 of an IFT request (see "How to Request an IFT" in the IFT section of this volume).

Sense Switch Description

Bypass New Error Stops CE Sense Switch
This CE sense switch causes the DCM to bypass new error stops while looping on a selected error code. If this switch is not set, the DCM stops for new errors detected during the loop.

Wait Before Continuing CE Sense Switch
This CE sense switch causes the DCM to wait after the INTERRUPT or START pushbuttons are pressed (with DISPLAY B containing X'806F'). The wait allows you to alter the STORAGE ADDRESS/REGISTER DATA switches for address compare or other uses. The DCM continues from the wait when the DISPLAY/FUNCTION SELECT switch is changed to FUNCTION 5 and the START pushbutton is pressed.

Problem Definition Mode CE Sense Switch
This CE sense switch causes a manual intervention code to be displayed in DISPLAY B. You must look in the appropriate IFT symptom index to determine what to do when the stop occurs. This mode gives you control over running long CCU storage protect IFT routines.

Restart Routine on First Error CE Sense Switch
This CE sense switch causes the DCM to restart the current routine when the first error is detected. Once this sense switch is set, the DCM restarts the routine at the point of the first error detected even though the error may not occur on subsequent restarts. This switch can be set when the routine is stopped to display an error code and must be reset to exit the routine.

Loop on First Error CE Sense Switch
This CE switch causes the DCM to loop the routine in which the first error was detected. The loop taken by this option is the smallest possible loop within the routine. Once this CE sense switch is set, the DCM loops the routine at the point of the first error detected even though the error is not detected on subsequent loops. This switch can be set when the routine is stopped to display an error code and must be reset to exit the routine.

Bypass Error Stop CE Sense Switch
This switch causes the DCM to not stop for an error display unless it is a new error display. This switch must be set with the restart routine on first error and the loop on first error to cause continuous looping. If this switch is not set with the restart and loop switches, the DCM stops with the error displayed each time the error is detected. For intermittent errors, this switch can be used to determine the relative time between failures.

Cycle on Request CE Sense Switch
This CE sense switch causes the DCM to repeat the requested IFT routine or group of routines until the switch is reset.

Include Manual Intervention Routines CE Sense Switch
This switch causes the manual intervention routines to be included in the requested IFT.

Repeat Each Routine CE Sense Switch
This CE sense switch causes the DCM to repeat each routine the number of times specified by a repeat count. The requested routine will repeat 128 times unless you change the repeat count (see "Set or Display Repeat Count" earlier in this section).

Halt Before Execution of CE Sense Switch
This CE sense switch causes the DCM to halt before executing each test routine.

Setting CE Sense Switches

Any of the switches can be set or reset separately. The switches can be displayed, one byte at a time.

If another panel utility is active, this panel utility cannot be executed. See "Stop Panel Utility" later in this section.

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see "Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1.
3. Set the STORAGE ADDRESS/REGISTER DATA switches to the following positions:

```
                STORAGE ADDRESS/REGISTER
                     DATA Switches
                                A B C D E
Set switches in byte S          - 9 S M M
Reset switches in byte S        - A S M M
```

Where:

- S = 0 or 1 for the desired byte
- MM = the bit position of the switches to be set or reset. (if MM = 00, the selected byte of the switches will be displayed, but not changed.)
- X = set to 0 when multiple CE sense switches are not used.

- means the switch can be set to any position.

Byte 0	M	M
Bypass New Error Stops	X	1
Wait Before Continuing.	8	X
Byte 1		
Problem Definition Mode	X	1
Restart Routine on First Error	X	2
Loop on First Error	X	4
Bypass Error Stop	X	8
Cycle on Request	1	X
Include Manual Intervention Routines	2	X
Repeat Each Routine N Times	4	X
Halt Before Execution	8	X

CE test switch options can be combined. For example, to loop on the first error (switch E = X'4'), you must also bypass error stop (switch E = X'8'). To combine both options, you would set switch E to X'C'.

1. Press the START pushbutton if the HARD STOP light is on. Otherwise press the INTERRUPT pushbutton.
2. DISPLAY A should be X'0000' and DISPLAY B should be '9SMM' or 'ASMM', where S is the byte of the switches and MM is the value of the switches. If the HARD STOP light is on, set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5 and press the START pushbutton to continue or respond as requested by the last stop code.

Stop Panel Utility

This utility stops the setup of a utility or stops an active utility.

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see

"Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1.
3. Set the STORAGE ADDRESS/REGISTER DATA switch B to X'1'.
4. Press the START pushbutton if the HARD STOP light is on. Otherwise press the INTERRUPT pushbutton.
5. DISPLAY A should be X'0000' and DISPLAY B should be X'8060'. For other values, see the appropriate IFT symptom index.
6. If the HARD STOP light is on, set the DISPLAY/FUNCTION SELECT switch to 5 and press the START pushbutton to continue or do what was requested from previous stop code.

Dynamic Communications to Routines

This panel utility allows communication with executing routines. The data entered by this panel utility is stored in the DCM control table and may be referred to by any executing routine. Each routine that uses this facility has a description in the appropriate IFT symptom index for the data to be entered and its use.

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see "Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1.
3. Set the STORAGE ADDRESS/REGISTER DATA switches as follows:

```
A B C D E
- D X X X
```

Where:

XXX is the data that is to be passed to the routine
- means that the switch can be set to any position

1. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton. DISPLAY B will be set to the data entered.
2. If the START pushbutton was pressed after a hard stop display, the HARD STOP light should be on, and the DCM is ready for your next input.

Display Storage or Register Contents

This panel utility displays a selected storage location or register via a program display. The maintenance cycle steal is not used. Because the pushbutton interrupt handler uses the registers, register displays in the program level at which this panel utility was requested may not agree with the display obtained by the maintenance cycle steal panel display. Also, requested display locations are not checked for validity and can cause input/output checks or address exception checks.

1. The PROGRAM DISPLAY light should be on during this procedure; if it is not on, see "Determining Why the PROGRAM DISPLAY Light is Not On" later in this section.
2. Select the type of display:
   a. For a storage display, set the DISPLAY/FUNCTION SELECT switch to FUNCTION 2.
   b. For a register display, set the DISPLAY/FUNCTION SELECT switch to FUNCTION 3.
3. Select the address to display:
   a. For a storage display, set the storage address in STORAGE ADDRESS/REGISTER DATA switches A, B, C, D, and E.
   b. For a register display, set the register number in STORAGE ADDRESS/REGISTER DATA switches B and D.
4. If the HARD STOP light is on, press the START pushbutton otherwise press the INTERRUPT pushbutton.
5. DISPLAY A should contain the requested storage or register address. DISPLAY B should contain the contents of the requested address. If other values are displayed, see the appropriate IFT symptom index.

HOW TO USE THE DISPLAY/FUNCTION SELECT SWITCH

With the DISPLAY/FUNCTION SELECT switch set to any position except TAR & OP REGISTER or STATUS, the following functions will be performed when: (1) the INTERRUPT pushbutton is pressed or (2) the START pushbutton is pressed after a stop code is displayed:

DISPLAY/FUNCTION SELECT Switch Position	STORAGE ADDRESS/ REGISTER DATA Switches A B C D E	FUNCTION
STORAGE ADDRESS	Y Y Y Y Y	Display location YYYYY.
REGISTER ADDRESS	- R - R -	Display register RR.
FUNCTION 1	- 0 - - -	Refresh the last DCM display.
	- 1 - - -	Stop the panel utilities.
	- 2 - - -	Set up continuous display without test.
	- 3 - - -	Set up continuous display with test.
	- 4 - - -	Set up address compare display without test.
	- 5 - - -	Set up address compare display with test.
	- 6 - H H	Set repeat count to HH.
	- 7 - - -	Display repeat count.
	- 9 S M M	Set CE sense switches (S=0 for byte 0 of switches, S=1 for byte 1 of switches, and MM= selected bits to be set or reset.
	- A S M M	Reset CE sense switches.
	- A S 0 0	Display CE sense switches.
	- D X X X	Dynamic communications to routines.
FUNCTION 2	X X X X X	Display storage contents at XXXXX.
FUNCTION 3	- R - R -	Display contents of register RR.
FUNCTION 4	- P I R R	Part 1 of IFT request (see "How to Request an IFT" later in this section). P=adapter number, I=IFT number and RR=routine number.
	- M M M M	Part 2 of IFT request (see "How to Request an IFT" later in this section). MMMM=CE sense switches
	- F 0 X X	Terminate OLTEP or OLTSEP at the host (see "How to Terminate an IFT" later in this section).
FUNCTION 5	V W X Y Z	Continue from the error stop or manual intervention stop. If it is an error stop, VWXYZ is not used. If it is a manual intervention stop, VWXYZ is used by the routine as specified in the appropriate IFT symptom index.
FUNCTION 6	- F F F F	Abort the total request.
	- - - - -	Abort the current routine.
FUNCTION 1,2, or 3		Panel utility display positions
FUNCTION 4,5, or 6		DCM displays of routine codes. Stop codes are displayed when the switch is set to any of the FUNCTION positions.

Note: - means that the switch is not used.

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Setting up a Scoping Loop

The DCM and IFTs provide two looping options for detected failures.

- Loop on first error selects the smallest possible loop within the IFT. The loop includes the hardware setup, pretest, set scope sync point 2, test, analysis, and error display. The loop for this option normally takes less time to execute than the restart routine on the first error option. The loop continues, whether or not the error occurs again.
- Restart routine on the first error selects a loop that starts at the beginning of a routine, continues the routine to the point where the error is first detected, and restarts the routine again. The loop for this option requires more time; however, it may be required for sequence-sensitive failures. The loop continues, whether or not the error occurs again.

Use the continue function to continue from the error stop after selecting the looping option. The time required to stop on the error code again indicates the length of the loop. Repeat this process several times using the longest length of time.

To obtain continuous running loops, the "bypass error stop" CE sense switch must also be set.

If an error other than the one selected for looping occurs, the DCM stops to display the new error code. To bypass stops for other errors, set the "bypass new error stop" CE sense switch.

When the scoping loop is running correctly, the scoping indicator (DISPLAY B, bit 0.4) blinks at the rate of 3.2 seconds (1.6 seconds on and 1.6 seconds off). DISPLAY B (byte 0, bits 5, 6, 7) is incremented by one, for each error detected. This error counter (together with the loop time) indicates whether the failure is solid or intermittent. Other information is also displayed. DISPLAY A shows the adapter, IFT, and routine number. DISPLAY B (byte 0, bits 0-3 and byte 1) shows the error code being looped on.

Determining Why The Program Display Light is Not On

When the DCM displays data in displays A and B, the PROGRAM DISPLAY light is turned on. Failure of the PROGRAM DISPLAY light to turn on may be diagnosed by the following:

1. Press the LAMP TEST switch. Does the PROGRAM DISPLAY lamp come on? If not, replace the PROGRAM DISPLAY lamp.
2. Is the HARD STOP light on?
   a. If yes, is the CCU CHECK light also on?
   - If not on, the 'hard stop' latch was set by the DCM or IFT. Determine the active program level, the IAR value of the level, and the program that the IAR relates to. Reload the program and try again.

   b. If the CCU CHECK light is on and if the LEVEL 1 PROGRAM CHECK light is also on, reload the program and retry.
   - If it is not on, determine the cause of the hardware check that caused the hard stop. Check DISPLAY A, byte 0 with the DISPLAY/FUNCTION switch set to STATUS.

3. If the PROGRAM STOP light is on, press the START pushbutton and check the other panel switches.
4. Other possible causes:
   a. Level 3 interrupt level has been masked. To unmask:
   - Stop the program
   - Display register X'7F', store X'00010' in register X'7F'
   - Start the program

   b. The request bit for the INTERRUPT pushbutton is failing. To test:
   - Stop the program.
   - Press the INTERRUPT pushbutton.
   - Display register X'7F'. Bit 0.6 should be on.
   - Start the program.

   c. Displaying data in displays A and B does not turn on the PROGRAM DISPLAY light. To test:
   - Display a storage location.
   - Turn the DISPLAY/FUNCTION SELECT switch to FUNCTION 1.
   - Press the INTERRUPT pushbutton if the program is running, or the START pushbutton if the program is stopped.
   - DISPLAY A should display the address entered. DISPLAY B should display the contents of the storage location addressed.
   - The PROGRAM DISPLAY lights should be on and the HARD STOP light should be on if the DCM was previously stopped on a display code.

   d. If the above techniques fail, reload the DCM. The initial display of X'FFFF' should cause the PROGRAM DISPLAY light to turn on. If it does, the problem is a program failure; if not, the problem is a hardware problem.

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Display A Code	Display B Code	Description of the DISPLAY Code	Manual Intervention Required
FFFF	8000	Enter part 1 of an IFT request.	Set DISPLAY/FUNCTION SELECT switch to FUNCTION 4. Set STORAGE ADDRESS/REGISTER DATA switches. *Switch* — *Description* B — Adapter number Example: Switch B = 1 for channel adapter 1; = 0 for all of the adapters tested by the IFT requested. C — IFT number = 0 for all IFTs = 1 for CCU IFT = 2 for storage IFT = 3 for type 1 channel adapter IFT = 6 for type 2 communication scanner IFT. = 9 for type 4 channel adapter 1FT. D and E — Routine Number = 00 for all routines of the selected IFT = XX for only routine XX (where XX = routine number) Press control panel START pushbutton.
	8001	Error on entering part 1 of request.	DISPLAY/FUNCTION SELECT switch not in FUNCTION 4. Re-enter part 1.
	8002	Enter part 2 of an IFT request.	Set DISPLAY/FUNCTION SELECT switch to FUNCTION 4. Select CE sense switches according to the following (combine for actual switch values): *Switch* B C D E Problem definition mode. . . . 1 Restart routine on first error. . . . 2 Loop on first error. . . . 4 Bypass error stop. . . . 8 Cycle on request. . . 1 . Include manual intervention routines. . . 2 . Repeat each routine X times . . 4 . Halt before execution. . . 8 . Bypass new error stops. . 1 . . Wait before continuing. 8 . . . Press control panel START pushbutton.
	8003	Error on entering part 2 of request.	DISPLAY/FUNCTION SELECT switch not in FUNCTION 4. Re-enter part 2. See stop 8002 for procedure to enter part 2.
	8004	Requested IFT number is not defined in the configuration data set (CDS).	Reg X'15' bits 0.4-0.7 = requested IFT number. Enter part 1 again. See stop 8000 for procedure to enter part 1 of request.
	8005	Requested IFT number was found but the requested adapter number is not defined in the Configuration Data Set.	Reg X'15' bits 0.0-0.3 = requested adapter number. Enter part 1 of request again. See stop 8000 for procedure to enter part 1.
	8006	IFT number or section number in the preface of the IFT loaded is not correct.	The wrong IFT was loaded or the numbers in the preface are wrong. Reg X'13' = loaded IFT/section number: byte 0 = IFT number and byte 1 = section number. Reg X'15' = IFT/section number desired (in IFT preface of IFT loaded): byte 0 = IFT number and byte 1 = section number. Check the messages at host processor console for further error messages concerning this IFT load request. Re-enter part 1 of request. See stop 8000 for procedure to enter part 1.

Display A Code	Display B Code	Description of the DISPLAY Code	Manual Intervention Required
FFFF	8007	The requested routine number was not found in any of the routine prefaces of the requested IFT.	Reg X'15' (byte 1) = requested routine number. Enter part 1 of request again. See stop 8000 for procedure to enter part 1.
XXXX	8008	The DCM has halted before executing the routine number in DISPLAY A.	To execute the routine, set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5 (continue) and press the control panel START pushbutton. Note — this stop occurred because CE Sense switch "halt before execution" is on.
	8009	DISPLAY/FUNCTION SELECT switch was not in FUNCTION 5 (continue) to continue from a halt before execution.	Set the switch and try again.
	800A	DISPLAY/FUNCTION SELECT switch was not in FUNCTION 5 (continue) or FUNCTION 6 (abort) when a request was made to continue from an error stop or a manual intervention stop.	Set the switch and try again.
	8X11	Group 0 IAR is not the active IAR.	Set the DISPLAY/FUNCTION SELECT switch to the STATUS position. If L1 is not entered, a program error has occurred on the highest level entered that has caused a branch to the DCM L1 interrupt handler. If L1 is entered, there is a failure in the hardware that selects Group 0 registers when L1 is active. To recover, reload.
	8X12	An L1 interrupt has occurred for an adapter not being tested by the IFT routine.	Reg X'05' = X = address of error data. X to X + 6 is valid. Reset the error condition, then select FUNCTION 5 (continue) or FUNCTION 6 (abort) and press the START pushbutton. *Address* — *Data* X — L1 interrupt request bits tested: byte 0 bit 1 = Type 2 CS number 1 L1 bit 5 = Type 1 CA number 1 L1 X+2 — Interrupted level byte 1 bit 0 = L2 bit 1 = L3 bit 2 = L4 bit 3 = L5 X+4/X+6 — Lagging address register. Address of instruction when interrupt occurred or address of last valid instruction before interrupt occurred. X+8/X+A — Data in local store register (R field) address by the input or output instruction. X+C — Input/output instruction that failed. Bits 0.1 to 0.3 and bits 1.0 to 1.3 = external register. Bits 1.4 to 1.5 = C for input, = 4 for output.
	8X13	An L1 interrupt has occurred for an input/output check.	Reg X'05' = X = address of error data. X to X+C is valid. See definition in 8X12. Select FUNCTION 5 (continue) or FUNCTION 6 (abort); then press the START pushbutton.
	8X14	The DCM L1 interrupt handler attempted to reset the input/output check defined in 8X13 and the input/output check request bit (Reg X'7E', bit 1.2) did not reset.	Select FUNCTION 5 (continue) or 6 (abort) and press the START pushbutton to retry the reset.
	8X15	An L1 interrupt has occurred for a protection check.	Reg X'05' = X = address of error data. X to X+6 is valid. See definition in 8X12. Select FUNCTION 5 (continue) or FUNCTION 6 (abort) and press the START pushbutton.
	8X16	An L1 interrupt has occurred for an address exception check.	Reg X'05' = X = address of error data. X to X+6 valid. See definition in 8X12. Select FUNCTIONS 5 (continue) or FUNCTION 6 (abort) and press the START pushbutton.
	8X17	An L1 interrupt has occurred for an invalid op check.	Reg X'05' = X = address of error data. X to X+6 is valid. See definition in 8X12. Select FUNCTION 5 (continue) or FUNCTION 6 (abort) and press the START pushbutton.
	8X18	The DCM L1 interrupt handler attempted to reset the protection check, address exception, or invalid op check defined above and the request bit (reg X'7E', bit 1.1, 1.3, or 1.4) did not reset.	Select FUNCTION 5 (continue) and press the START pushbutton to retry the reset.
	8X19	An L1 interrupt has occurred for an IPL request. An IPL request should cause a ROS load.	Reg X'05' = X = address of error data. X is valid. See definition in 8X12. Select FUNCTION 5 (continue) and press the START pushbutton.

Display A Code	Display B Code	Description of the DISPLAY Code	Manual Intervention Required
XXXX	8X1A	The DCM L1 interrupt handler attempted to reset the IPL request defined in 8X19 and the request bit (reg X'7E', bit 1.6) did not reset.	Select FUNCTION 5 (continue) and press the START pushbutton to exit L1 if "loop on first error" CE sense switch is not on. If "loop on first error" switch is on, the program will try to reset again.
	8X1B	The DCM is unable to exit interrupt L1 after being loaded and given control (for the first time) on L1.	Run the initial test that checks instruction execution at each level.
	8X20	An unexpected L2 interrupt has occurred.	Use the control panel to determine cause and to reset the cause. Then set select FUNCTION 5 (continue) or 6 (abort) and press the START pushbutton. Reg X'76' and reg X'7E' request bits.
	8X31	An L3 interrupt has occurred for an adapter not being tested by the IFT routine (INTERRUPT pushbutton and timer interrupts are expected and do not cause this error).	Reg X'0D' = X = address of error data. *Address* *Data* X L3 interrupt request bits tested bit 1.2 = Type 2 or 3 CA number 2 bit 0.3 = Type 1 or 4 CA data/status bit 1.4 = Type 1, 2, 3, or 4 CA number 1 initial Reset the L3 adapter interrupt condition. Select FUNCTION 5 (continue) or FUNCTION 6 (abort) and press the START pushbutton.
	8X32	An L3 interrupt has occurred for an unexpected PCI L3 interrupt.	Reg X'0D' = X = address of error data. See stop 8031 for data meaning. Select FUNCTION 5 (continue) and press the START pushbutton to allow program to attempt to reset the PCI L3.
	8X33	The DCM L3 interrupt Handler attempted to reset the PCI L3 defined above and the PCI L3 request bit (reg X'7F', bit 1.6) did not reset.	Select FUNCTION 5 (continue) and press the START pushbutton to allow the program to try to reset the PCI L3 again.
	8X34	The DCM L3 interrupt handler attempted to reset the interval timer interrupt request bit and the request bit (reg X'7F', bit 1.5) did not reset.	Select FUNCTION 5 (continue) and press the START pushbutton to cause the DCM to try to reset again.
	8X35	The DCM L3 interrupt handler attempted to reset the INTERRUPT pushbutton request and the request bit (reg X'7F', bit 0.6) did not reset.	Press the START pushbutton to cause DCM to try to reset again.
	8X40	An unexpected L4 interrupt has occurred.	**Note:** PCI L4 is set by the DCM and should be on all the time except while some CCU IFT routines are running. Use the control panel to determine cause and to reset the cause before using continue function. Reg X'7F' defines the request bits.
0000	8060	Requested utility function performed.	If HARD STOP light is on, set up other utility functions or select FUNCTION 5 (continue) or FUNCTION 6 (abort) and press the START pushbutton. (If previous stop was code 8000 through 8007, select FUNCTION 4 (request) and complete your request). If the INTERRUPT pushbutton was used to do the utility function, this display code is for information only and the program should still be running.
	8061	The request for a panel utility is not correct.	Check switch positions and try again. Possibilities: Switch B is not set for a valid utility request code. Switch C is not set to 0 or 1 for Byte 0 or 1 on a CE switch request.
	8062	The test condition specified has not been met.	The following registers of the active level contain these parameters: Register – X'01' R1 = address tested R3 = contents of address R5 = error bits If the status indicates that L1 is active, register 1, register 3, and register 5 = registers X'01', X'03', and X'05'. If the status indicates that L3 is active, register 1, register 3, and register 5 = registers X'09', X'0B', and X'0D'. Select function to terminate utility, to continue, etc. Press the START pushbutton.
	8064	Enter the mask in the STORAGE ADDRESS/REGISTER DATA switches for testing the contents of the address to display, press the START pushbutton if the HARD STOP light is on.	Press the INTERRUPT pushbutton if the program is running.

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3705-80 DCM SYMPTOM INDEX - Cont.

Display A Code	Display B Code	Description of the DISPLAY Code	Manual Intervention Required
0000	8065	Enter the expected data in the STORAGE ADDRESS/REGISTER DATA switches for testing the contents of the address to display, then press the START push-button if the HARD STOP light is on.	Press the INTERRUPT pushbutton if the program is running.
	8066	Enter the address to display.	Set the DISPLAY/FUNCTION SELECT switch to: A = storage address to display contents of storage location. * = register address to display contents of register. Set the STORAGE ADDRESS/REGISTER DATA switches to: ABCDE = storage address B/D = register address Press the START pushbutton if the HARD STOP light is on. Press the INTERRUPT pushbutton if the program is running.
	8067	DISPLAY/FUNCTION SELECT switch not set to STORAGE ADDRESS or REGISTER ADDRESS for code 8066.	Retry with initial utility request.
	8068	Set up for display is complete.	If the HARD STOP light is on, select FUNCTION 5 (continue) and press the START pushbutton to continue. (If previous stop code was 8000 through 8007 select FUNCTION 4 (request) and complete the request. If the program is running, this display code is for information only.
XXXX	806F	The DCM has halted due to CE sense switch "wait before continuing" being on.	This pause may be used to execute the utility functions or to change the STORAGE ADDRESS/REGISTER DATA switches for address compare use. Select FUNCTION 5 (continue) and press the START pushbutton to continue.
FFFF	80F0	Test request is finished and no errors were detected. The DCM is ready to accept a new request.	See stop 8000 for procedure to enter request.
	80F1	Test request is finished and errors were detected. The DCM is ready to accept a new request.	See stop 8000 for procedure to enter request.
	80F2	Test was aborted by the operator.	Ready to accept a new request. See stop 8000 for procedure to enter request.
XXXX	80FF	A program or hardware failure has caused a branch to storage location zero.	See interrupt entered indicator to determine interrupt level. DISPLAY A is the address of the instruction that caused the branch to location zero if L1 is not active. (The address also is in register 5 of the active level.) Analyze the program registers, etc. to determine why the branch occurred. Reload the DCM to recover from this error.
FFFF	FFFF	DCM is loaded and ready for first IFT request.	See FFFF 8000 for request procedure. Both bits of byte X in DISPLAY B should be on.

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INITIAL TEST (INIT)

WHAT INIT DOES

Initial Test (INIT) is loaded by the type 1 channel adapter (CA) loader (Z3705AAA) and is executed before the control program (CP) or the diagnostic control monitor (DCM) (Z3705ACA) is loaded. INIT verifies that basic registers, storage areas, storage functions, and the 3705-80 instruction set operate correctly. INIT has two sections:

- Z3705ADA
  - Tests the functions of some registers
  - Tests basic storage functions
  - Tests a limited amount of storage
- Z3705AEA
  - Tests the instruction set in each of the five program levels, starting at program level 1, then program level 2, and so on through program level 5. INIT then returns to program level 1 before returning control to the loader. Each instruction is tested for proper: (1) instruction decode, (2) CZ latch setting and resetting, and (3) ALU function.
  - Tests storage addressing by storing a unique pattern at each storage location. Storing begins at the end of INIT and continues to the last storage location. INIT then reads storage to see that none of the storage locations have been modified after being stored into.

This section of the manual describes loading and running INIT using a host channel; if you are using the remote program load (RPL) feature, see the RPL DIAG section.

The INIT symptom index, at the back of this section, lists the functions tested by the INIT routines. The symptom index also shows critical register values, expected CZ latch settings, and locations of suspected failing cards.

REQUIREMENTS

You must have the proper configuration data set (CDS) cataloged with the remainder of the system (for additional information, see the CDS section). Before INIT routines can be executed properly, the functional areas in the CCU hardware must be operational. These functional areas are tested by the ROS bootstrap program each time the LOAD pushbutton is pressed.

INIT EXECUTION

3705 Setup Procedures

1. Switch the 3705 power on.
2. Set both the MODE SELECT and DIAGNOSTIC CONTROL switches to the PROCESS position.
3. Enable the appropriate channel interface.
4. Set the DISPLAY/FUNCTION SELECT switch to any position other than a FUNCTION position to load the DCM at the completion of INIT. For information on using the FUNCTION positions, see "CE Options" later in this section.
5. Press the RESET pushbutton and then the LOAD pushbutton.
6. DISPLAY B bits 0.2 and 0.3 should be on, indicating that ROS has reached IPL phase 3. The LOAD light is on; the following lights are off: HARDSTOP, TEST, WAIT, and PROGRAM STOP.

If the above conditions are not present, refer to the "CE Panel Test" in the CTRL PNL section and the "ROS Test" in the ROS section (Volume 2).

Running the Host Loader

Start the OLTEP or the OLTSEP program in the host processor. When OLTEP or OLTSEP causes a console printer message of:

r ID 'ENTER DEV/TEST/OPT/'

you enter:

r ID,'XXX/3705A/nfe,ext=ABCD/'

where:

XXX = the channel and unit address of the 3705 (native attachment address).

ABCD = four operating options provided by the OLT and type 1 CA loaders. The correct entries are Y (for YES) or N (for NO). The options are defined as follows:

A = OLT bypass printing channel errors
B = Run INIT
C = Run type 1 CA loader with error checking
D = Bypass hard stop on type 1 CA loader error in 3705 and retry

If your response to the DEV/TEST/OPT/ message does not include the ext= parameter, the default value assumed is ext=nyyy (that is, ext=NO,YES,YES,YES).

Delay of INIT Execution: Before INIT begins executing, the 3705/host interface must be disabled. The type 1 CA loader attempts to disable the 3705 interface by issuing a diagnostic DISABLE command when INIT is loaded. The host 'clock out' line must drop before the 3705 can go offline. The host 'clock out' line drops when either the host processor STOP pushbutton is pressed or when the host processor enters the wait state.

Operating situations under OS or DOS can result in maximum use of the processor that will delay the host from entering the wait state. During this delay, the OLT prints a message indicating that it is waiting for the 3705 to disable its channel interface. Also, at the 3705, an equivalent message code is displayed in the control panel lights. See "Interpreting Display Lights during Loading" later in this section.

MESSAGES

Messages occur during operation of the type 1 CA loader that indicate: (1) the loader has detected an error or (2) an action is needed to load the diagnostic programs into 3705 storage. The messages, message explanations, and responses are as follows:

THE STATUS OF THE 3705 CANNOT BE DETERMINED. **WARNING** CONTINUATION WILL CAUSE THE ENTIRE 3705 TO BECOME UNAVAILABLE. ENTER 'C' TO CANCEL OR 'P' TO PROCEED.

Explanation: The OLT cannot determine the status (offline or stopped) of the 3705. If the OLT is allowed to continue, the program in 3705 storage will be destroyed.

Response: Continue by entering a C or P, as follows:

r id,'C' (for cancel)
or
r id,'P' (for proceed)

Any other response results in the program's repeating the last line of the above message. After five invalid responses, the message INVALID RESPONSE AFTER 5 REQUESTS is printed.

ALL 3705 ADDRESSES ARE NOT STOPPED OR OFFLINE. **WARNING** CONTINUATION WILL CAUSE THE ENTIRE 3705 TO BECOME UNAVAILABLE. ENTER 'C' TO CANCEL OR 'P' TO PROCEED, OR 'R' TO RETRY.

Explanation: The OLT has been notified by the executive driver that all 3705 addresses are not offline or stopped. If the OLT is allowed to continue, the program in 3705 storage will be destroyed.

Response: You have the opportunity to make all addresses available to the OLT using standard system facilities. Continue by entering a C, P, or R, as follows:

r id,'C' (for cancel)
or
r id,'P' (for proceed)
or
r id,'R' (for retry)

The difference between a P and an R response is (1) P means to proceed, regardless of the offline or online status of the 3705 address and (2) R means that the operator has been taking addresses offline and wants the program to verify that all units are now available to the OLT.

Any other response results in the program's repeating the last line of the above message. After five invalid responses, the message INVALID RESPONSE AFTER 5 REQUESTS is printed.

INVALID RESPONSE AFTER 5 REQUESTS

Explanation: The program assumed the response of 'C' and terminated the OLT.

Response: None.

BAD RC YY FROM XXXXXXX

Explanation: The type 1 CA loader has requested of the executive driver a function that the driver is incapable of performing. This may be because of an invalid parameter or an error that has occurred while the executive driver is performing the request. XXXXXXX is the name of the function being requested, and YY is the code returned by the executive program. The XXXXXXX field is filled by the type 1 CA loader.

Response: This message is a diagnostic programming aid. If the message occurs, a dump and other available information should be submitted with an APAR (Authorized Program Analysis Report).

The following messages are printed on the system output printer to describe failures and the operation that is being attempted when an error occurs:

BAD CC SIO

FAILED TO INTRPT

BAD STATUS ON SIO

NOP CMD FOR 3705 LOAD BUTTON

RD CMD FOR IFT REQ

WRT CMD TO WRITE DATA

WRT CMD FOR LAST BLOCK

WRT IPL CMD SENDING LOADER

WRT CMD SENDING CONTROL WORD

Explanation: If the DCM has already been loaded, the program indicates that you can make a request at the 3705. If the DCM has not been loaded, the program starts over by requesting you to press the LOAD pushbutton on the 3705.

Response: If DCM has been loaded, enter a request; otherwise press LOAD.

PRESS LOAD ON 3705

Explanation: This message occurs when the type 1 CA loader is initially started or if loss of control occurs. It constitutes the beginning of the type 1 CA loader and provides the synchronization between the 3705 and the host processor.

Response: Press the LOAD pushbutton on the 3705. This message repeats every 30 seconds until the LOAD pushbutton is pressed.

AWAITING 3705 INTERFACE DISABLE

Explanation: The type 1 CA loader has loaded INIT in the 3705 and is waiting for the 3705 to go offline. This message is repeated every 20 seconds until the 3705 channel interface is disabled and the 3705 begins executing the IFT.

If this message occurs continuously, the 3705 is either unable to go offline after the INIT has been loaded or unable to get back online after the INIT has completed execution. A processor-bound system can cause this problem.

Response: Pressing the STOP and then the START pushbuttons on the processor console drops the 'clock out' line long enough for the 3705 to go offline. Entering the wait state accomplishes this also.

3705 LOADED WITH IFT Z3705AAA
3705 LOADED WITH IFT Z3705ADA
3705 LOADED WITH IFT Z3705AEA

Explanation: These messages indicate that INIT or IFT modules have been successfully loaded in the 3705 without any errors being detected. Z3705AAA is the type 1 CA loader, Z3705ADA is the INIT section 1, and Z3705AEA is the INIT section 2.

Response: None.

ERP USED ON MOD Z3705XXX

Explanation: This message warns you that errors have occurred while loading the INIT or IFT modules. Each output operation to the 3705 is attempted up to 10 times if an error occurs (unless the OLT option EL [N] has been modified). If the operation being attempted is performed before the error count is exhausted, the OLT considers the data transfer successful and continues loading the INIT or IFT modules.

Response: Verify that the INIT or IFT modules are at the proper level.

Z3705XXX IN ERROR, ABORT LOAD

Explanation: The retry count (normally 10) is exhausted, and the error is still occurring. The type 1 CA loader assumes that loss of control has occurred and restarts at the beginning.

Response: Refer to the message "ERP USED ON MOD Z3705XXX".

WAITING FOR IFT COMPLETION

Explanation: This message occurs every 20 seconds after an IFT has been loaded in the 3705. Most of the IFTs disable the 3705. The type 1 CA loader is in a loop issuing NOP commands to the 3705. If it receives condition code 03, the 3705 interface is not enabled; it prints this message and waits another 20 seconds. When the 3705 is enabled, the type 1 CA loader continues executing.

Response: None.

INVALID PLINK MOD

Explanation: The type 1 CA loader has detected an error in the requested module. (An address in the module is on an odd boundary.) The type 1 CA loader returns to the Read command to allow you to enter another request at the 3705.

Response: Enter another request.

MOD Z3705XXX NOT IN OLTLIB

Explanation: The type 1 CA loader has received an IFT request (through a Read command) for a module that is not in OLTLIB. The type 1 CA loader returns to the Read command to allow you to enter another request at the 3705.

Response: Enter another request. However, if the original request was valid, the IFT module name must be added to the OLTEP/OLTSEP library before the IFT can be loaded.

INTERPRETING DISPLAY LIGHTS DURING LOADING

DISPLAY A shows the number of valid channel commands (Read, Write, IPL, Write, Break, or Sense) that has occurred during the loading of a module. This count is dynamically updated each time a device end (DE) is presented to end a successful channel transfer. DISPLAY B shows various errors or execution indications, as follows:

DISPLAY B	*Definition*
00FE	Awaiting type 1 channel interface disable
00FF	Awaiting type 1 channel interface enable
FF00	Awaiting type 1 channel level 3 interrupt
0000	All other times

A hard stop at location TAR=06D6 indicates that the wrong loader is being used for the channel; register X'79', bit 1.6 must be on if a type 1 CA is installed. (A CDS error can also cause this stop.) A hard stop at location TAR=0668 indicates an error has been detected during a type 1 CA loader operation.

COMMUNICATIONS CONTROLLER LOADER UTILITY

This utility allows the customer to execute the INIT routines prior to loading NCP or EP.

1. The loader program must be initiated in the host processor. Refer to the appropriate NCP or Emulation Program (EP) publications.
2. Switch the 3705 power on.
3. Set both the MODE SELECT and DIAGNOSTIC CONTROL switches in the PROCESS position.
4. Enable the appropriate channel interface.
5. Set the DISPLAY/FUNCTION SELECT switch to any position other than a FUNCTION position. However, the STATUS position is suggested.
6. Press the RESET pushbutton and then the LOAD pushbutton.

REMOTE PROGRAM LOADER (RPL)

To use the remote program loader:

1. The RPL feature must be installed.
2. A correctly written disk media must be available.

Refer to the RPL DIAG section for IPL procedures.

NORMAL INIT RUN INDICATIONS

During a normal control program load or DCM load, the following indications signal correct operation:

1. The ENTERED INTERRUPT LEVEL lights switch sequentially from PROG LEV1 (which indicates program level 1) to no lights on (which indicates program level 5) as the INIT routines are executed in that level. PROG LEV1 is switched on again prior to loading the control program or DCM.

2. These panel indicators are on during INIT:

   PROGRAM DISPLAY
   TEST
   LOAD

CE OPTIONS

The following options are available for troubleshooting failures.

Loop On Program Level

Loop on program level allows you to loop in INIT under control of the DISPLAY/FUNCTION SELECT switch.

DISPLAY/FUNCTION SELECT Switch Position	*Loop Description*
FUNCTION 1	Loop on program level 1
FUNCTION 2	Loop on program level 2
FUNCTION 3	Loop on program level 3
FUNCTION 4	Loop on program level 4
FUNCTION 5	Loop on program level 5
FUNCTION 6	Loop on all program levels
Any other position	Run each test once, then request the next program.

When the DISPLAY/FUNCTION SELECT switch is set to any of the FUNCTION positions, the routine number is displayed in DISPLAY B, byte 0; and the active program level is displayed in byte 1, bits 4-7.

Note: Because the INIT routines are executed very quickly, the routine number displayed may not be visible.

Loop On Error

Loop on error allows you to loop in a routine from the location where the error was detected back to the start of the routine. If on the next pass through the routine the error does not occur, the program loops from the end of the routine back to the start. This method tests for intermittent errors.

To loop on an error after the program stops so that you can display the second error display data:

1. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5.
2. Place the address of the output X'70' instruction, which indicates the error, in the STORAGE ADDRESS/REGISTER DATA switches. (See "Failure Indications" in this section to determine the address of the output X'70' instruction).
3. Press START.

The program takes the address entered in the STORAGE ADDRESS/REGISTER DATA switches and overlays that halfword with a NOP instruction to prevent additional hard stops and allow looping.

To exit from the loop, momentarily move the DISPLAY/FUNCTION SELECT switch to a position other than FUNCTION 5. The overlaid output X'70' instruction is restored.

Display Routine Starting Address

This option allows you to display, in DISPLAY A, the starting address of the routine in which the error occurred.

When the program stops to display the second error display data:

1. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 5.
2. Place the address of the output X'70' instruction in the STORAGE ADDRESS/REGISTER DATA switches.
3. Add X'0001' to the STORAGE ADDRESS/REGISTER DATA switch setting.
4. Press START.

This turns on a flag which causes the program to stop again with the starting address displayed in DISPLAY A.

DISPLAY A, bit 1.3 is on at this time to indicate that this option is active.

Once you have recorded the starting address, you have two options: (1) press START to execute the loop-on-error program again, or (2) continue testing by setting the DISPLAY/FUNCTION SELECT switch to a position other than FUNCTION 5 and pressing START.

Abort the Current Routine and Continue Testing

If a program stop occurs and you do not want to loop on error or display the routine starting address, set the DISPLAY/FUNCTION SELECT switch to any position except FUNCTION 5 and press START. This aborts the current routine and continues testing.

FAILURE INDICATIONS

If an error is detected during execution of INIT, the WAIT, HARD STOP, and PROGRAM STOP lights will be on. The error is one of two types:

1. CCU CHECK: CCU checks are hardware-detected errors that are seen in DISPLAY A by setting the DISPLAY/FUNCTION SELECT switch to the STATUS position.

   If a CCU check is detected, it can be the result of the function being tested or it can be a failure of the hardware doing the testing. See the CCU Check Analysis Flowchart in the Start section for information and procedure concerning failure.
2. PROGRAM STOP (no CCU check): INIT does an output X'70' (hard stop) to report an error.

   If a program stop occurs, set the DISPLAY/FUNCTION SELECT switch to any position other than TAR & OP REGISTER or STATUS. DISPLAY B will contain, in byte 0, the current routine number and, in byte 1, bits 4-7, the current program level.

   Record: (1) the value of register 0 (R0) (IAR) for the current program level, (2) the setting of the CZ latches, and (3) if appropriate, the value of register 5 (R5) and/or register 7 (R7) (see Figure INIT-1 in "DISPLAY B"). To see if R5 or R7 is used, see the expected results column in the INIT symptom index for the current routine (DISPLAY B, byte 0).

   Subtract 2 from the R0 (IAR) value to get the address of the out stop instruction that indicates the error. This address value is needed for the loop-on-error option and display-starting-address option.

   Press START to display the error codes in DISPLAY A (see "How to Use the INIT Symptom Index").

   Select the desired CE option (FUNCTION 1-6).

Note: If an asynchronous program stop occurs (a level 1 interrupt from a section of the 3705-80 not presently being tested), set the DISPLAY/FUNCTION SELECT switch to STATUS and record DISPLAY B, bytes 0.4-7 and 1.0. See the problem analysis chart in the START section.

How to Use the INIT Symptom Index

The DISPLAY/FUNCTION switch must be in a FUNCTION position (1-6).

DISPLAY A

Data displayed in DISPLAY A defines either the error code and loop count or the routine starting address. If the PROGRAM STOP light is not on, the data in DISPLAY A is the loop count. If the PROGRAM STOP light is on and DISPLAY B byte 1, bit 3 is not on, the data in DISPLAY A is the error code.

BYTE 0 Bits								*BYTE 1 Bits*							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	X	X	0	0	0	0	0	0	X	X	X	X	X	X

If DISPLAY A byte 0, bit 2 or 3 is on, the error code is common to many routines and is listed in the back of the INIT symptom index.

The majority of the INIT routines are straight line code (no looping or subroutines). As a result, by taking the address of a given output X'70' instruction and displaying the starting address of that routine, you can use the address-compare-interrupt capability to pinpoint the failing instruction.

The symptom index supplies the critical data and expected setting of the CZ latches.

DISPLAY B

Data displayed in DISPLAY B indicates (1) the routine number, (2) the type of error data that is displayed in DISPLAY A, and (3) the current program level under test.

BYTE 0 Bits								*BYTE 1 Bits*							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
R	R	R	R	R	R	R	R	0	0	0	T	N	N	N	N

Where:

RRRR RRRR = The routine number.
T = The type of data displayed in DISPLAY A
0000 = The error code or loop count.
0001 = The starting address of the routine.
NNNN = The program level in which the error occurred.

1000 = program level 1
0100 = program level 2
0010 = program level 3

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0001 = program level 4
0000 = program level 5

Because the majority of the INIT routines are executed under all 5 program levels, the symptom index refers to a general register for a program level without listing its hexadecimal value, depending on the value of NNNN as previously defined.

NNNN	PROG LEVEL	(IAR) R0	R1	R2	R3	R4	R5	R6	R7
1000	1	X'00'	X'01'	X'02'	X'03'	X'04'	X'05'	X'06'	X'07'
0100	2	X'00'	X'01'	X'02'	X'03'	X'04'	X'05'	X'06'	X'07'
0010	3	X'08'	X'09'	X'0A'	X'0B'	X'0C'	X'0D'	X'0E'	X'0F'
0001	4	X'10'	X'11'	X'12'	X'13'	X'14'	X'15'	X'16'	X'17'
0000	5	X'18'	X'19'	X'1A'	X'1B'	X'1C'	X'1D'	X'1E'	X'1F'

Figure INIT-1. Hexadecimal Values for Registers Based on Program Level

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Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
0108	XXXX	Registers X'02', X'04', and X'06' are tested to verify data patterns FF, 00, AA, and 55.							
	0001	XR R2, R2 failed to clear byte 0.	R2(0) = XX	R2(0) = 00	01	See Note 2.			
	0002	XR R2, R2 failed to clear byte 1.	R2(0) = XX	R2(1) = 00	01	See Note 2.			
	0003	LH R2, SAVE failed to load R2 byte 0 with all ones.	R2(0) = 00	R2(0) = FF	11	See Note 2.			
	0004	LH R2, SAVE failed to load R2 byte 1 with all ones.	R2(1) = 00	R2(1) = FF	11	See Note 2.			
	0005	LH R2, SAVE2 failed to load R2 byte 0 with X'55'.	R2(0) = FF	R2(0) = 55	11	See Note 2.			
	0006	LH R2, SAVE2 failed to load R2 byte 1 with X'55'.	R2(1) = FF	R2(1) = 55	11	See Note 2.			
	0007	LH R2, SAVE3 failed to load R2 byte 0 with X'AA'.	R2(0) = 55	R2(0) = AA	11	See Note 2.			
	0008	LH R2, SAVE3 failed to load R2 byte 0 with X'AA'.	R2(1) = 55	R2(1) = AA	11	See Note 2.			
	0009	Register X'04' Byte 0 failed to load the correct data.		R4(0) = Actual. R5(0) = Expected.	11	See Note 2.			
	000A	Register X'04' Byte 1 failed to load the correct data.		R4(1) = Actual. R5(0) = Expected.	11	See Note 2.			
	000B	Register X'06' Byte 0 failed to load the correct data.		R6(0) = Actual. R5(0) = Expected.	11	See Note 2.			
	000C	Register X'06' Byte 1 failed to load the correct data.		R6(1) = Actual. R6(0) = Expected.	11	See Note 2.			
0208	XXXX	Test to verify that input X'70' defines a valid maximum address. Test last valid storage address (max. 64K). Storage size indicated in Reg X'70' is incorrect.		R6 = Maximum address as calulated from input X'70'.					If actual storage size is greater than 64K, X'FFFE' will be used instead of actual max. address.
0308	XXXX	Error correction routine—Ability to correct single bit errors, detect double bit errors, diagnostic reg reset.							
	0001	Error correction failed to reset data bit forced to 1 via diagnostic reg.		R6 = Expected data. R4 = Bits in error.	01				
	0002	Error correction failed to set data bit forced to 0 via diagnostic reg.		R6 = Expected data. R3 = Bits in error.	01				
	0003	Failed to detect double bit error.		R3 = Expected. R6 = Actual.					
	0004	Diagnostic reg did not reset or test mode did not set. Reset of test mode should reset the diagnostic reg.		R1 = Expected. R3 = Actual.	01				
0408	XXXX	Addressing test—Address is stored as data and verified to be correct address.							
	0001	Data at address does not match address.		R1 = Expected. R5 = Actual.	01				Problem may be CDS, check CDS data defining storage.
0708	XXXX	Storage test—Store zeros in background of ones.							
	0001	Background pattern was destroyed. Addressing problem suspected.		R1 = Test address. R2 = Exp. (backgnd.) R5 = Bits in error.					If this error occurs, bypass the running of INIT and load the storage IFT.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
0708	0002	Store and then load a test pattern.		R1 = Test address. R4 = Expected. R5 = Bits in error.					If this error occurs, bypass the running of INIT and load the storage IFT.
	0003	Load test pattern again to test restore capability.		R1 = Test address. R4 = Expected. R3 = Bits in error.					If this error occurs, bypass the running of INIT and load the storage IFT.
	0004	Parity bit failed.		R1 = Test address.					If this error occurs, bypass the running of INIT and load the storage IFT.
0808	XXXX	Storage test—Store ones in background of zeros.							
	0001	Background pattern was destroyed. Addressing problem suspected.		R1 = Test address. R2 = Exp. (backgnd.) R5 = Bits in error.					
	0002	Store and then load a test pattern.		R1 = Test address. R4 = Expected. R5 = Bits in error.					
	0003	Load test pattern again to test restore capability.		R1 = Test address. R4 = Expected. R3 = Bits in error.					
0908	XXXX	Program relocation—This routine is used to relocate test to address X'2000'. No error stops should occur.							
0A08	XXXX	Storage test 0-2K. Store zeros in background of ones.							
	0001	Background pattern was destroyed. Addressing problem suspected.		R1 = Test address. R2 = Exp. (backgnd.) R5 = Bits in error.					
	0002	Store and then load a test pattern.		R1 = Test address. R4 = Expected. R5 = Bits in error.					
	0003	Load test pattern again to test restore capability.		R1 = Test address. R4 = Expected. R3 = Bits in error.					
	0004	Parity bit failed.		R1 = Test address.					
0B08	XXXX	Storage test 0-2K. Store ones in background of zeros.							
	0001	Background pattern was destroyed. Addressing problem suspected.		R1 = Test address. R2 = Exp. (backgnd.) R5 = Bits in error.					
	0002	Store and then load a test pattern.		R1 = Test address. R4 = Expected. R5 = Bits in error.					
	0003	Load test pattern again to test restore capability.		R1 = Test address. R4 = Expected. R3 = Bits in error.					

3705-80 INIT SYMPTOM INDEX - Cont.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
0C08	XXXX	Program relocation—All data relocated by Routine 0908 will be relocated back to '0000-0FFE' and control will be passed to the C. E. Loop Option subroutine. No error stops should occur.							

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
100N	XXXX	Branch instruction test.							
	0001	Branch with a displacement of 2 failed to branch around error stop.	N/A	N/A	01	AB3H2	CD002	6-640	Decode failure.
	0002	Prior to issuing the branch, R1 was loaded with zeros to set the CZ latches. After branching, the CZ latches are tested to verify that the branch did not alter the CZ latches.	R1(1) = 00	R1(1) = 00	01	AB3G2	CZxxx	6-640	CZ latch failure.
	0003	Same as 0001 above.	N/A	N/A	10	AB3H2	CD002	6-640	Decode failure.
	0004	Same as 0002 above except R1(1) is loaded with all ones to set the CZ latches to 10.				AB3G2	CZxxx	6-640	CZ latch failure.
110N	XXXX	LRI and BB pattern test.							
	0001	R1(1) is loaded with X'05' using LRI, then R1(1) is XOR with X'05'.	R1(1) = 05	R1(1) = 00	01	AB3H2	CD002	6-170	Decode failure.
	0002	R1(1) is loaded with all ones and the CZ latches are tested.	R1(1) = 00	R1(1) = FF	10	AB3G2	CZxxx	6-170	CZ latch failure.
	0003	A series of BB instructions is performed on R1(1). One of the eight BB failed to branch.	R1(1) = FF	R1(1) = FF	10	AB3H2	CD002	6-660	Decode failure.
	0004	BB instruction(s) altered the CZ latches.	R1(1) = FF	R1(1) = FF	10	AB3G2	CZxxx	6-660	CZ latch failure.
	0005	R1(0) is loaded with X'00' and then the CZ latches are tested for 01.	R1(0) = XX	R1(0) = 00	01	AB3H2 AB3G2	CD002 CZxxx	6-170	Decode failure. CZ latch failure.
	0006	A series of BB instructions is performed on R1(0). One of the eight BB branched on a zero or previous LRI failed.	R1(0) = 00	R1(0) = 00	01	AB3H2	CD002	6-660 6-170	Decode failure.
	0007	BB instruction altered the CZ latches.	R1(0) = 00	R1(0) = 00	01	AB3G2	CZxxx	6-660	CZ latch failure.
	0008	R1(0) is loaded with X'FF' and then the CZ latches are tested for 10.	R1(0) = 00	R1(0) = FF	10	AB3H2	CD002	6-170	Decode failure.
	0009	A series of BB instructions is performed on R1(0). One of the eight BB failed to branch.	R1(0) = FF	R1(0) = FF	10	AB3H2	CD002	6-660	Decode failure.
	000A	BB instruction altered the CZ latches.	R1(0) = FF	R1(0) = FF	10	AB3G2	CZxxx	6-660	CZ latch failure.
	000B	R1(1) is loaded with all zeros and the CZ latches are tested for 01.	R1(1) = FF	R1(1) = 00	01	AB3G2	CZxxx	6-170	CZ latch failure.
	000C	A series of BB instructions is performed on R1(1). One of the eight BB branched on a zero or previous LRI failed.	R1(1) = 00	R1(1) = 00	01	AB3H2	CD002	6-660 6-170	Decode failure.
	000D	BB instruction altered the CZ latches.	R1(1) = 00	R1(1) = 00	01	AB3G2	CZxxx	6-660	CZ latch failure.
120N	XXXX	XRI instruction test.							
	0001	XRI or Z latch failed.	R1(1) = 0C	R1(1) = 00	01	AB3H2 AB3J2 AB3G2	CDxxx CA003 CZxxx	6-170	
	0002	XRI or C latch failed when R1(1) is XOR with all ones.	R1(1) = 00	R1(1) = FF	10	AB3J2 AB3H2 AB3G2	CA003 CDxxx CZxxx	6-170	ALU control failure. Decode failure. CZ latch failure.
	0003	XRI above failed to produce the correct data. Testing is with BB instructions.		R1(1) = FF		See Note 2.		6-170 6-660	See Note 2 for bit failures.
	0004	XRI failed to set Z latch.	R1(1) = FF	R1(1) = 00	01	See Note 2.		6-170	See Note 2 for bit failures.
	0005	XRI above failed to produce correct data. Testing is with BB instructions.		R1(1) = 00	01	See Note 2.		6-170	See Note 2 for bit failures.
	0006	XRI or C Latch failed.	R1(0) = FF	R1(0) = FF	10	See Note 2.		6-170	See Note 2 for bit failures.
	0007	XRI above failed to produce correct data. Testing is with BB instructions.		R1(0) = FF	10	See Note 2.		6-170	See Note 2 for bit failures.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
120N	0008	XRI failed to set Z latch.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-170	See Note 2.
	0009	Above XRI failed to produce correct data.		R1(1) = 00	01	See Note 2.		6-170	See Note 2.
130N	XXXX	ARI Instruction Test.							
	0001	ARI decode or CZ failure.	R1(1) = 0E	R1(1) = 00	10	AB3G2 AB3J2	CZ002 CA002	6-170	Decode failure. ALU CTL failure.
	0002	ARI or CZ latch failure adding zeros.	R1(0) = FF	R1(0) = FF	00	AB3G2 AB3J2	CZxxx CA002	6-170	CZ latch failure.
	0003	Above ARI modified high byte. Testing by XRI.	R1(0) = FF	R1(0) = 00	01	See Note 2.		6-170	See Note 2 for bit failures.
	0004	ARI or C latch failure adding zeros.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-170	
	0005	Above ARI modified low byte. Testing by XRI.	–	R1(1) = 00	01	See Note 2.		6-170	
	0006	CZ latch failure adding all ones.	R1(1) = 00	R1(1) = FF	00	See Note 2.		6-170	
	0007	ARI above, failed to produce correct result. Testing is with XRI instructions.	–	R1(1) = 00	01	See Note 2.		6-170	
	0008	ARI CZ latch failure adding all ones to all ones.	R1(1) = FF	R1(1) = FE	10	See Note 2.		6-170	
	0009	Above ARI failed to produce correct result. Testing is with XRI instructions.	–	R1(1) = 00	01	See Note 2.		6-170	
150N	XXXX	Data flow path: byte 1, Zeros Pattern Sensitivity.							XRI, BB, BCL and BZL instructions are used to verify bit sensitivity.
	0001	XRI or CZ latch failure.	R1(1) = 00	R1(1) = 01	10	See Note 2.		6-170	
	0002	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(1) = 01	10	See Note 2.		6-170 6-660	Any failure in this routine, see Note 2.
	0003	XRI failed to set Z latch.	R1(1) = 01	R1(1) = 00	01	See Note 2.		6-170	
	0004	XRI or CZ latch failure.	R1(1) = 00	R1(1) = 02	10	See Note 2.		6-170	
	0005	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(1) = 02	10	See Note 2.		6-170 6-660	
	0006	XRI failed to set Z latch.	R1(1) = 02	R1(1) = 00	01	See Note 2.		6-170	
	0007	XRI or CZ latch failure.	R1(1) = 00	R1(1) = 04	10	See Note 2.		6-170	
	0008	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(1) = 04	10	See Note 2.		6-170	
	0009	XRI failed to set Z latch.	R1(1) = 04	R1(1) = 00	01	See Note 2.		6-170	
	000A	XRI or CZ latch failure.	R1(1) = 00	R1(1) = 08	10	See Note 2.		6-170	
	000B	Above XRI failed to produce correct results. Testing is with BB instructions.	–	R1(1) = 08	10	See Note 2.		6-170	
	000C	XRI failed to zet Z latch.	R1(1) = 08	R1(1) = 00	01	See Note 2.		6-170	
	000D	XRI or CZ latch failure.	R1(1) = 00	R1(1) = 10	10	See Note 2.		6-170	
	000E	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(1) = 10	10	See Note 2.		6-170	
	000F	XRI failed to set Z latch.	R1(1) = 10	R1(1) = 00	01	See Note 2.		6-170	
	0010	XRI or CZ latch failure.	R1(1) = 00	R1(1) = 20	10	See Note 2.		6-170	
	0011	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(1) = 20	10	See Note 2.		6-170	
	0012	XRI failed to set Z latch.	R1(1) = 20	R1(1) = 00	01	See Note 2.		6-170	
	0013	XRI or CZ latch failure.	R1(1) = 00	R1(1) = 40	10	See Note 2.		6-170	

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
150N	0014	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(1) = 40	10	See Note 2.		6-170	
	0015	XRI failed to set Z latch.	R1(1) = 40	R1(1) = 00	01	See Note 2.		6-170	
	0016	XRI or CZ latch failure.	R1(1) = 00	R1(1) = 80	10	See Note 2.		6-170	
	0017	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(1) = 80	10	See Note 2.		6-170	
	0018	XRI failed to set Z latch.	R1(1) = 80	R1(1) = 00	01	See Note 2.		6-170	
	0019	XRI or CZ latch failure.	R1(1) = 00	R1(1) = AA	10	See Note 2.		6-170	
	001A	Above XRI failed to produce correct result. Testing is with B and BB instructions.	–	R1(1) = AA	10	See Note 2.		6-170	
	001B	XRI failed to set Z latch.	R1(1) = AA	R1(1) = 00	01	See Note 2.		6-170	
160N	XXXX	Data flow path: byte 1, Ones Pattern Sensitivity.							XRI, BB, BCL and BZL instructions are used to verify bit sensitivity.
	0001	XRI or CZ latch failure.	R1(1) = 00	R1(1) = FE	10	See Note 2.		6-170	
	0002	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(1) = FE	10	See Note 2.		6-170	Any failure in this routine, see Note 2.
	0003	XRI failed to set Z latch.	R1(1) = FE	R1(1) = 00	01	See Note 2.		6-170	
	0004	XRI or CZ latch failure.	R1(1) = 00	R1(1) = FD	10	See Note 2.		6-170	
	0005	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(1) = FD	10	See Note 2.		6-170	
	0006	XRI failed to zet Z latch.	R1(1) = FD	R1(1) = 00	01	See Note 2.		6-170	
	0007	XRI or CZ latch failure.	R1(1) = 00	R1(1) = FB	10	See Note 2.		6-170	
	0008	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(1) = FB	10	See Note 2.		6-170	
	0009	XRI failed to set Z latch.	R1(1) = FB	R1(1) = 00	01	See Note 2.		6-170	
	000A	XRI or CZ latch failure.	R1(1) = 00	R1(1) = F7	10	See Note 2.		6-170	
	000B	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(1) = F7	10	See Note 2.		6-170	
	000C	XRI failed to set Z latch.	R1(1) = F7	R1(1) = 00	01	See Note 2.		6-170	
180N	XXXX	Data flow path: byte 0, Ones pattern sensitivity.							XRI, BB, BCL and BZL instructions are used to verify bit sensitivity.
	0001	XRI or CZ latch failure.	R1(0) = 00	R1(0) = EF	10	See Note 2.		6-170	
	0002	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(0) = EF	10	See Note 2.		6-170	Any failure in this routine, see Note 2.
	0003	XRI failed to set Z latch.	R1(0) = EF	R1(0) = 00	01	See Note 2.		6-170	
	0004	XRI or CZ latch failure.	R1(0) = 00	R1(0) = DF	10	See Note 2.		6-170	
	0005	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(0) = DF	10	See Note 2.		6-170	
	0006	XRI failed to set Z latch.	R1(0) = DF	R1(0) = 00	01	See Note 2.		6-170	
	0007	XRI or CZ latch failure.	R1(0) = 00	R1(0) = BF	10	See Note 2.		6-170	
	0008	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(0) = BF	10	See Note 2.		6-170	
	0009	XRI failed to set Z latch.	R1(0) = BF	R1(0) = 00	01	See Note 2.		6-170	
	000A	XRI or CZ latch failure.	R1(0) = 00	R1(0) = 7F	10	See Note 2.		6-170	
	000B	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(0) = 7F	10	See Note 2.		6-170	

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
180N	000C	XRI failed to set Z latch.	R1(0) = 7F	R1(0) = 00	01	See Note 2.		6-170	
190N	XXXX	Data flow path: Byte 0, Zeros Pattern Sensitivity.							XRI, BB, BCL and BZL instructions are used to verify bit sensitivity.
	0001	XRI or CZ latch failure.	R1(0) = 00	R1(0) = 01	10				
	0002	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(0) = 01	10	See Note 2.		6-170	
	0003	XRI failed to set Z latch.	R1(0) = 01	R1(0) = 00	01	See Note 2.		6-170	
	0004	XRI or CZ latch failure.	R1(0) = 00	R1(0) = 02	10	See Note 2.		6-170	
	0005	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(0) = 02	10	See Note 2.		6-170	
	0006	XRI failed to set Z latch.	R1(0) = 02	R1(0) = 00	01	See Note 2.		6-170	
	0007	XRI or CZ latch failure.	R1(0) = 00	R1(0) = 04	10	See Note 2.		6-170	
	0008	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(0) = 04	10	See Note 2.		6-170	
	0009	XRI failed to set Z latch.	R1(0) = 04	R1(0) = 00	01	See Note 2.		6-170	
	000A	XRI or CZ latch failure.	R1(0) = 00	R1(0) = 08	10	See Note 2.		6-170	
	000B	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(0) = 08	10	See Note 2.		6-170	
	000C	XRI failed to set Z latch.	R1(0) = 08	R1(0) = 00	01	See Note 2.		6-170	
	000D	XRI or CZ latch failure.	R1(0) = 00	R1(0) = 55	10	See Note 2.		6-170	
	000E	Above XRI failed to produce correct result. Testing is with BB instructions.	–	R1(0) = 55	10	See Note 2.		6-170	
	000F	XRI failed to set Z latch.	R1(0) = 55	R1(0) = 00	01	See Note 2.		6-170	
1B0N	XXXX	ORI instruction test.							
	0001	ORI decode failure. Low byte containing 09 was ORI with 05. Result tested by XRI.	R1(1) = 09	R1(1) = 00	01	AB3H2 AB3J2	CD002 CA003	6-170	Decode failure. ALU control failure.
	0002	ORI or CZ latch failure.	R1(1) = 00	R1(1) = FF	10	AB3G2	CZxxx	6-170	CZ latch failure.
	0003	Above ORI failed to produce correct result. Testing is with XRI instructions.	R1(1) = FF	R1(1) = 00	01	See Note 2.		6-170	See Note 2 for bit failures in this routine.
	0004	ORI or CZ latch failure.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-170	
	0005	Above ORI failed to produce correct result. Testing is with XRI instructions.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-170	
	0006	ORI or CZ latch failure.	R1(0) = FF	R1(0) = FF	10	See Note 2.		6-170	
	0007	Above ORI failed to produce correct result. Testing is with XRI instructions.	R1(0) = FF	R1(0) = 00	01	See Note 2.		6-170	
	0008	ORI or CZ latch failure FF was ORI with FF.	R1(0) = 00	R1(0) = FF	10	See Note 2.		6-170	
	0009	ORI above failed to produce correct result. Testing is with XRI instructions.	R1(0) = FF	R1(0) = 00	01	See Note 2.		6-170	
1C0N	XXXX	NRI instruction test.							
	0001	NRI decode failure. 09 was NRI with 05. Result was tested with XRI instruction.	R1(1) = 09 R1(1) = 05 R1(1) = 01	R1(1) = 00	01	AB3H2 AB3J2	CD002 CA002	6-170	Decode failure. ALU control failure.
	0002	NRI or CZ latch failure. 00 was NRI with 00.	R1(1) = 00	R1(1) = 00	01	AB3G2	CZxxx	6-170	CZ latch failure.
	0003	Above NRI failed to produce correct result. Tested by XRI instruction.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-170	
	0004	NRI or CZ latch failure. FF was NRI with FF.	R1(0) = FF	R1(0) = FF	10	See Note 2.		6-170	

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
1C0N	0005	Above NRI failed to produce correct result. Tested by XRI instruction.	R1(0) = FF	R1(0) = 00	01	See Note 2.		6-170	
	0006	NRI or CZ latch failure. FF was NRI with 00.	R1(1) = FF	R1(1) = 00	01	See Note 2.		6-170	
	0007	NRI above failed to produce correct result.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-170	
	0008	NRI or CZ latch failure. FF was NRI with 00.	R1(0) = 00	R1(0) = 00	01	See Note 2.		6-170	
	0009	Above NRI failed to produce correct result. Tested by XRI instruction.	R1(0) = 00	R1(0) = 00	01	See Note 2.		6-170	
1D0N	XXXX	TRM instruction test.							
	0001	TRM decode failure. Tested by XRI. TRM mask was 05.	R1(1) = 09	R1(1) = 00	01	AB3H2 AB3J2	CDxxx CA002	6-170	Decode failure. ALU control failure.
	0002	TRM or CZ latch failure. TRM Mask was FF.	R1(1) = FF	R1(1) = FF	10	AB3K2 AB3G2	CL003 CZxxx	6-170	LS control failure. CZ latch failure.
	0003	Above TRM modified R1 low. Tested by XRI instruction.	R1(1) = FF	R1(1) = 00	01	See Note 2.		6-170	See Note 2 for bit failure.
	0004	TRM or CZ latch failure. TRM Mask was 00.	R1(0) = FF	R1(0) = FF	01	See Note 2.		6-170	
	0005	Above TRM modified R1 high. Tested by XRI instruction.	R1(0) = FF	R1(0) = 00	01	See Note 2.		6-170	
	0006	TRM or CZ latch failure. TRM Mask was FF.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-170	
	0007	Above TRM modified R1 low.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-170	
1E0N	XXXX	SRI instruction test.				AB3H2	CD002	6-170	Decode failure.
	0001	SRI Decode failure. SRI 05 from 09. Result tested by XRI instruction.	R1(1) = 09 R1(1) = 05 R1(1) = 04	R1(1) = 00	01	AB3J2 AB3G2	CA003 CZxxx	6-170	ALU control failure. CZ latch failure
	0002	SRI or CZ latch failure. SRI 00 from FF.	R1(0) = FF	R1(0) = FF	00	See Note 2.		6-170	
	0003	SRI above failed to produce correct result. Tested by XRI instruction.	R1(0) = FF	R1(0) = 00	01	See Note 2.		6-170	
	0004	SRI or CZ latch failure. SRI Mask was 00.	R1(0) = 00	R1(0) = 00	01	See Note 2.		6-170	
	0005	Above SRI failed to produce correct result. Tested by XRI instruction.	R1(0) = 00	R1(0) = 00	01	See Note 2.		6-170	
	0006	SRI or CZ latch failure.	R1(1) = FF	R1(1) = 00	01	See Note 2.		6-170	
	0007	Above SRI failed to produce correct result. Tested by XRI instruction.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-170	
	0008	SRI or CZ latch failure. SRI Mask was FF.	R1(1) = 00	R1 = FF01	10	See Note 2.		6-170	
	0009	Above SRI failed to produce correct result. Tested by XRI instruction.	R1 = FF01	R1 = 0000	01	See Note 2.		6-170	
1F0N	XXXX	CRI instruction test.							
	0001	CRI decode failure. CRI Mask was 05. Tested by XRI instruction.	R1(1) = 09 R1(1) = 09	R1(1) = 00	01	AB3H2 AB3J2 AB3K2	CD002 CA003 CL003	6-170	Decode failure. ALU control failure. LS control failure.
	0002	CRI or CZ latch failure. CRI Mask was FF.	R1(1) = FF	R1(1) = FF	01	AB3G2	CZxxx	6-170	CZ latch failure.
	0003	Above CRI modified R1 low. Tested by XRI instruction.	R1(1) = FF	R1(1) = 00	01	See Note 2.		6-170	
	0004	CRI or CZ latch failure. CRI Mask was FF.	R1(1) = 00	R1(1) = 00	10	See Note 2.		6-170	
	0005	Above CRI modified R1 low. Tested by XRI instruction.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-170	
	0006	CRI or CZ latch failure. CRI Mask was FE.	R1(1) = FF	R1(0) = FF	00	See Note 2.		6-170	
	0007	Above CRI modified R1 high. Tested by XRI instruction.	R1(0) = FF	R1(0) = 00	01	See Note 2.		6-170	

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Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
200N	XXXX	LCR instruction test.							
	0001	LCR decode failure. Tested by XRI instruction.	R1(1) = 09	R3(1) = 05		AB3H2	CD002	6-220	Decode failure.
			R1(1) = 05	R1(1) = 00	01	AB3J2	CAxxx	6-170	ALU controls failure.
	0002	Above LCR modified R3 low. Tested by XRI instruction.	R3(1) = 05			AB3G2	CZxxx	6-220	CZ latch failure.
			R3(1) = FF	R3(1) = 00	01			6-170	See Note 2 for bit failures.
	0003	LCR or CZ latch failure.	R3(0) = XX			See Note 2.		6-220	
			R3(1) = 01	R3(0) = 01	00				
	0004	LCR above failed to produce correct result. Tested by XRI instruction.	R3(0) = 01	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0005	LCR or CZ latch failure.	R3(1) = 02			See Note 2.		6-220	
			R3(0) = 00	R3(0) = 02	00				
	0006	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = 02	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0007	LCR or CZ latch failure.	R3(1) = 04			See Note 2.		6-220	
			R3(0) = 00	R3(0) = 04	00				
	0008	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = 04	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0009	LCR or CZ latch failure.	R3(1) = 08			See Note 2.		6-220	
			R3(0) = 00	R3(0) = 08	00				
	000A	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = 08	R3(0) = 00	01	See Note 2.		6-220 6-170	
	000B	LCR or CZ latch failure.	R3(1) = 10			See Note 2.		6-220	
			R3(0) = 00	R3(0) = 10	00				
	000C	Above LCR failed to produce correct results. Tested by XRI instruction.	R3(0) = 10	R3(0) = 00	01	See Note 2.		6-220 6-170	
	000D	LCR or CZ latch failure.	R3(1) = 20			See Note 2.		6-220	
			R3(0) = 00	R3(0) = 20	00				
	000E	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = 20	R3(0) = 00	01	See Note 2.		6-220 6-170	
	000F	LCR or CZ latch failure.	R3(1) = 40			See Note 2.		6-220	
			R3(0) = 00	R3(0) = 40	00				
	0010	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = 40	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0011	LCR or CZ latch failure.	R3(1) = 80			See Note 2.		6-220	
			R3(0) = 00	R3(0) = 80	00				
	0012	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = 80	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0013	LCR or CZ latch failure.	R3(1) = 7F			See Note 2.		6-220	
			R3(0) = 00	R3(0) = 7F	00				
	0014	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = 7F	R3(0) = 00	01	See Note 2.		6-220 6-170	

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
200N	0015	LCR or CZ latch failure.	R3(1) = BF R3(0) = 00	R3(0) = BF	00	See Note 2.		6-220	
	0016	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = BF	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0017	LCR or CZ latch failure.	R3(1) = DF R3(0) = 00	R3(0) = DF	00	See Note 2.		6-220	
	0018	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = DF	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0019	LCR or CZ latch failure.	R3(1) = EF R3(0) = 00	R3(0) = EF	00	See Note 2.		6-220	
	001A	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = EF	R3(0) = 00	01	See Note 2.		6-220 6-170	
	001B	LCR or CZ latch failure.	R3(1) = F7 R3(0) = 00	R3(0) = F7	00	See Note 2.		6-220	
	001C	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = F7	R3(0) = 00	01	See Note 2.		6-220 6-170	
	001D	LCR or CZ latch failure.	R3(1) = FB R3(0) = 00	R3(0) = FB	00	See Note 2.		6-220	
	001E	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = FB	R3(0) = 00	01	See Note 2.		6-220 6-170	
	001F	LCR or CZ latch failure.	R3(1) = FD R3(0) = 00	R3(0) = FD	00	See Note 2.		6-220	
	0020	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = FD	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0021	LCR or CZ latch failure.	R3(1) = FE R3(0) = 00	R3(0) = FE	00	See Note 2.		6-220	
	0022	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = FE	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0023	LCR or CZ latch failure. 2 LCR instructions used. R3 high to R3 high sets CZ = 00. R3 low to R3 high sets CZ = 11.	R3(1) = 00 R3(0) = FE	R3(0) = 00	11	See Note 2.		6-220	
	0024	Above LCRs failed to produce correct result. Tested by XRI instruction.	R3(0) = 00	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0025	LCR or CZ latch failure.	R3(1) = FF R3(0) = 00	R3(0) = FF	10	See Note 2.		6-220	
	0026	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = FF	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0027	LCR or CZ latch failure.	R3(1) = AA R3(0) = 00	R3(0) = AA	10	See Note 2.		6-220	
	0028	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = AA	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0029	LCR or CZ latch failure.	R3(1) = 55 R3(0) = 00	R3(0) = 55	10	See Note 2.		6-220	

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Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
200N	002A	Above LCR failed to produce correct result. Tested by XRI instruction.	R3(0) = 55	R3(0) = 00	01	See Note 2.		6-220 6-170	
	002B	LCR or CZ latch failure. Tested by XRI instruction.	R3(1) = FE R1(1) = 00	R1(1) = FE R1(1) = 00	01	See Note 2.		6-220 6-170	
	002C	LCR failure. Tested by XRI instruction.	R3(0) = 00 R1(0) = FF	R1(0) = 00 R1(0) = 00	01	See Note 2.		6-220 6-170	
	002D	LCR failure. Tested by XRI instruction.	R3(0) = 00 R1(0) = FF	R1(0) = 00	01	See Note 2.		6-220 6-170	
220N	XXXX	Branching test.							
	0001	BZL, pos. displacement – ALU failure.			11	AB3G2	CZxxx	6-640	CZ latch failure.
	0002	B, neg. displacement–ALU failure.			11	AB3J2	CAxxx	6-640	ALU controls failure.
	0003	BCL, neg. displacement – ALU failure.			11	See Note 2.		6-640	See Note 2 for bit failures.
	0004	BZL, neg displacement.			11	See Note 2.		6-640	
	0005	BCL, BZL, B, BB failure.			11	See Note 2.		6-640 6-660	
230N	XXXX	ACR instruction test.							
	0001	ACR decode failure. Result 0E is tested by XRI instruction.	R3(1) = 05 R1(1) = 09	R1(1) = 0E R1(1) = 00	01	AB3H2 AB3J2	CDxxx CAxxx	6-220 6-170	Decode failure. ALU controls failure. See Note 2 for bit failures.
	0002	ACR or CZ latch failure.	R3(1) = 01 R1(0) = F7	R1(0) = F8	00	AB3G2	CZxxx	6-220	CZ latch failure.
	0003	Above ACR did not produce correct result. Tested by XRI instruction.	R1(0) = F8	R1(0) = 00	01	See Note 2.		6-220 6-170	
	0004	ACR or C latch failure. ACR R3 high with R3 low, CZ = 00. ACR R1 low with R3 high, CZ = 11.	R1(1) = 81 R3 = 7F01	R3 = 7F80 R3 = 0080	11	See Note 2.		6-220	
	0005	Above ACR, Z latch failure.				See Note 2.		6-220	
	0006	Above ACR, failed to produce correct data in R3 low. Tested by XRI instruction.	R3(1) = 80	R3(1) = 00	01	See Note 2.		6-220 6-170	
	0007	Above ACR failed to produce correct data in R3 high. Tested by XRI instruction.	R3(0) = 00	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0008	Above ACR modified contents of R1(1). Tested by XRI instruction.	R1(1) = 81	R1(1) = 00	01	See Note 2.		6-220 6-170	
	0009	Above ACR modified contents of R1(0). Tested by XRI instruction.	R1(0) = FF	R1(0) = 00	01	See Note 2.		6-220 6-170	
	000A	ACR or CZ latch failure. ACR R1 high with R1 high.	R1(0) = FF	R1(0) = FE	10	See Note 2.		6-220	
	000B	Above ACR failed to produce correct result. Tested by XRI instruction.	R1(0) = FE	R1(0) = 00	01	See Note 2.		6-220 6-170	

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
230N	000C	ACR failed to produce correct result when ACR R1 low with R3 low. Tested by XRI instruction.	R1(1) = 00 R3(1) = FF	R3(1) = FF	00	See Note 2.		6-220 6-170	
240N	XXXX	OCR instruction test.							
	0001	OCR decode failure. Tested by XRI instruction.	R3(1) = 05 R1(1) = 00	R1(1) = 00 R1(1) = 00	01	AB3H2 AB3J2	CDxxx CA003	6-220 6-170	Decode failure. ALU controls failure. See Note 2 for bit failures.
	0002	OCR or CZ latch failure.	R3(1) = CC R1(0) = 33	R1(0) = FF	10	AB3G2	CZxxx	6-220	CZ latch failure.
	0003	Above OCR failed to produce correct result. Tested by CRI instruction.	R1(0) = FF	R1(0) = FF	01	See Note 2.		6-220 6-170	
	0004	OCR or CZ latch failure.	R3(0) = 00 R1(1) = 00	R1(1) = 00	01	See Note 2.		6-220	
	0005	Above OCR failed to produce correct result. Tested by CRI instruction.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-220 6-170	
	0006	OCR or CZ latch failure. Tested by CRI instruction.	R1(0) = FF	R1(0) = FF	01	See Note 2.		6-220 6-170	
250N	XXXX	NCR instruction test.							
	0001	NCR decode failure. Tested by XRI instruction.	R3(1) = 05 R1(1) = 09	R1(1) = 01 R1(1) = 00	01	AB3H2 AB3J2	CD002 CAxxx	6-220 6-170	Decode failure. ALU controls failure. See Note 2 for bit failures.
	0002	NCR or CZ latch failure.	R3(0) = FF R1(1) = FF	R1(1) = FF	10	AB3G2	CZxxx	6-220	CZ latch failure.
	0003	NCR above failed to produce correct result. Tested by CRI instruction.	R1(1) = FF	R1(1) = FF	01	See Note 2.		6-220 6-170	
	0004	NCR or CZ latch failure.	R1(1) = FF R1(0) = 00	R1(0) = 00	01	See Note 2.		6-220	
	0005	Above NCR failed to produce correct result. Tested by CRI instruction.	R1(0) = 00	R1(0) = 00	01	See Note 2.		6-220 6-170	
260N	XXXX	XCR instruction test.							
	0001	XCR instruction decode tested by XRI instruction.	R3(1) = 05 R1(1) = 09	R1(1) = 0C R1(1) = 00	01	AB3H2 AB3J2	CD002 CA003	6-220 6-170	Decode failure. ALU controls failure. See Note 2 for bit failures.
	0002	XCR or CZ latch failure.	R1(0) = FF R1(1) = 00	R1(1) = FF	10	AB3G2	CZxxx	6-220	CZ latch failure.
	0003	Above XCR failed to produce correct result. Tested by CRI instruction.	R1(1) = FF	R1(1) = FF	01	See Note 2.		6-220 6-170	
	0004	XCR or CZ latch failure.	R1(1) = FF R3(0) = FF	R3(0) = 00	01	See Note 2.		6-220	
	0005	XCR above failed to produce correct result.	R3(0) = 00	R3(0) = 00	01	See Note 2.		6-220	

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Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
270N	XXXX	SCR instruction test.							
	0001	SCR decode failure. Tested by XRI instruction.	R3(1) = 05 R1(1) = 09	 R1(1) = 04 R1(1) = 00	 01	AB3H2 AB3J2	CD002 CA003	6-220 6-170	Decode failure. ALU controls failure.
	0002	SCR or CZ latch failure.	R1(0) = FF R3(0) = 00	 R3(0) = 01	 10	AB3G2	CZxxx	6-220	CZ latch failure.
	0003	Above SCR failed to produce correct result. Tested by XRI instruction.	R3(0) = 01	R3(0) = 00		See Note 2.		6-220 6-170	
	0004	SCR or CZ latch failure.	R1(0) = FF R3(0) = FF	 R3(0) = 00	 01	See Note 2.		6-220	
	0005	Above SCR failed to produce correct result. Tested by XRI instruction.	R3(0) = 00	R3(0) = 00	01	See Note 2.		6-220 6-170	
280N	XXXX	CCR instruction test.	R3(1) = 05						
	0001	CCR decode failure. Tested by XRI instruction.	R1(1) = 09	R1(1) = 09 R1(1) = 00	 01	AB3H2 AB3J2	CD002 CA003	6-220 6-170	Decode failure. ALU controls failure.
	0002	CCR or CZ latch failure.	R3(1) = FF R3(0) = 00	 R3(0) = 00	 10	AB3G2	CZxxx	6-220	CZ latch failure.
	0003	Above CCR modified R3 high. Tested by XRI instruction.	R3(0) = 00	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0004	CCR or CZ latch failure.	R1(0) = FF R3(1) = FF	 R3(1) = FF	 01	See Note 2.		6-220	
	0005	Above CCR modified R3 low. Tested by XRI instruction.	R3(1) = FF	R3(1) = 00	01	See Note 2.		6-220 6-170	
	0006	CCR or C latch failure.	R1(0) = 01 R3(0) = 02		10	See Note 2.		6-220 6-170	
	0007	CCR or Z latch failure.	R1(0) = 01 R3(0) = 02		10	See Note 2.		6-220 6-170	
290N	XXXX	LCOR instruction test.							
	0001	LCOR decode failure. Tested by XRI instruction.	R3(1) = 05 R1(1) = 09	 R1(1) = 02 R1(1) = 00	 01	AB3H2 AB3J2	CD002 CAxxx	6-220 6-170	Decode failure. ALU controls failure.
	0002	LCOR or CZ latch failure. LCOR R3 high into R3 high.	R3(0) = FF	R3(0) = 7F	10	See Note 2.		6-220	
	0003	Above LCOR failed to produce correct result. Tested by XRI instruction.	R3(0) = 7F	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0004	LCOR or CZ latch failure. LCOR R1 low into R1 low.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-220	
	0005	Above LCOR failed to produce correct result. Tested by CRI instruction.	R1(1) = 00	R1(1) = 00	01	See Note 2.		6-220	
2A0N	XXXX	LHR instruction test.							
	0001	LHR decode failure. Tested by XRI instruction.	R3(1) = 05 R1(1) = 09	 R1(1) = 05 R1(1) = 00	 01	AB3H2 AB3J2	CD003 CA001	6-220 6-170	Decode failure. ALU controls failure.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
2B0N	XXXX	SHR instruction test.							
	0001	SHR decode failure. Tested by XRI instruction.	R3(1) = 05 R1(1) = 09	R1(1) = 04 R1(1) = 00	 01	AB3H2 AB3H2	CD003 CA003	6-220 6-170	Decode failure. ALU controls failure.
	0002	SHR or CZ latch failure.	R1 = 0100 R3 = 0000	R3 = FF00	10	AB3G2	CZxxx	6-220	CZ latch.
	0003	Above SHR failed to produce correct result. Tested by XRI instruction.	R3(0) = FF	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0004	Above SHR failed to produce correct result. Tested by XRI instruction.	R3(1) = 00	R3(1) = 00	01	See Note 2.		6-220 6-170	
	0005	SHR or CZ latch failure.	R3 = FF00 R1 = FF00	 R1 = 0000	01	See Note 2.		6-220	
	0006	SHR or CZ latch failure.	R1 = 01FF R3 = FF00	 R3 = FD01	 00	See Note 2.		6-220	
	0007	SHR above failed to produce correct result. Tested by XRI instruction.	R3(0) = FD	R3(0) = 00	01	See Note 2.		6-220 6-170	
	0008	SHR above failed to produce correct result. Tested by XRI instruction.	R3(1) = 01	R3(1) = 00	01	See Note 2.		6-220 6-170	
2C0N	XXXX	CHR instruction test.							
	0001	CHR decode failure. Tested by XRI instruction.	R3(1) = 05 R1(1) = 09	R1(1) = 09 R1(1) = 00	 01	AB3H2 AB3J2	CD003 CAxxx	6-220 6-170	Decode failure. ALU control failure.
2E0N	XXXX	Byte 0 and 1 data flow pattern sensitivity test. This routine loops 256 times. The first test pattern is FF00 and each successive pass adds one to byte 1 and subtracts one from byte 0 so that the last test pattern is 00FF.							See Note 2 for bit failures.
	0001	LHR instruction is used to move R3 data into R1. The CZ latches are tested for 10.	R3 = NOT 0	R1 = R3	10	See Note 2.		6-220	
	0002	LHR data transfer is tested by XORing data in R1 and R3 byte 0. Byte 0 data failed to transfer.	R1 = R3	R3(0) = 00	01	See Note 2.		6-220	R3(0) = Bits that failed.
	0003	LHR data transfer is tested by XORing data in R1 and R3 byte 1. Byte 1 data failed to transfer.	R1(1) = R3(1)	R3(1) = 00	01	See Note 2.		6-220	R3(1) = Bits that failed.
	0004	CHR instruction is tested by comparing R1 and R3.	R1 = R3	R1 = R3 R3 = Test Pattern	01	See Note 2.		6-220	
2F0N	XXXX	Byte 0 and 1 data flow pattern sensitivity test: 2 of 2.							
	0001	LHR instruction is used to move R1 data into R3. The CZ latches are tested for 01.	R1 = 0000 R3 = FFFF	 R3 = 0000	01	See Note 2.		6-220	
	0002	CHR instruction is used to test data transfer.	R1 = 0000 R3 = 0000	R1 = 0000 R3 = 0000	01	See Note 2.		6-220	
	0003	CHR instruction is tested for correct CZ latches when data is unequal.	R1 = 0000 R5 = FFFF	R1 = 0000	10	See Note 2.		6-220	Note 1

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
2F0N	0004	The data in R3(1) is tested to verify error codes 0001 and 0002 above.	R3 = 0000	R3(1) = 00	01	See Note 2.		6-220	R3(1) = Bits in error.
	0005	The data in R3(0) is tested to verify codes 0001 and 0002 above.	R3 = 0000	R3(0) = 00	01	See Note 2.		6-220	R3(0) = Bits in error.
310N	XXXX	AHR instruction test.							
	001	AHR R1, R3. A basic AHR instruction is executed and the results are tested by XORING.	R1(1) = 09 R3(1) = 05 R1(1) = 0E	R1(1) = 00	01	AB3H2 AB3J2	CDxx CAxxx	6-220 6-220	R1(1) = Bits in error. Decode. ALU controls.
	0002	R1 is added to R1. The CZ latches are tested for 01.	R1 = 0000	R1 = 0000	01	AB3G2	CZxxx	6-220	CZ latches.
	0003	AHR should have caused an overflow. The Z latch is tested.	R3 = FF00 R5 = 0100	R3 = 0000	11	See Note 2.		6-220	Note 1.
	0004	Same instruction as 0003. The C latch is tested.		R3 = 0000	11	See Note 2.		6-220	
	0005	CHR is used to verify the data in R3.	R1 = 0000 R3 = 0000	R1 = 0000 R3 = 0000	01	See Note 2.		6-220	
	0006	AHR instruction is tested for CZ latches 00.	R3 = 0001 R1 = FFFE	R1 = FFFF	00	See Note 2.		6-220	
	0007	The data in R1 is verified by using XRI. Byte 1 failed.	R1 = FFFF	R1(1) = 00	01	See Note 2.		6-220 6-170	R1(1) = Bits in error.
	0008	Same as 0007 except Byte 0 failed.	R1 = FF00	R1(0) = 00	01	See Note 2.		6-220 6-170	R1(0) = Bits in error.
320N	XXXX	OHR instruction test.							
	0001	OHR R1, R3. R1 data is tested by XRI. Instruction failed.	R1(1) = 09 R3(1) = 05 R1(1) = 0D	R1(1) = 00	01	AB3H2 AB3J2	CD003 CA003	6-220 6-170	Decode failure. ALU controls failure. See Note 2 for bit failures.
	0002	OHR R5, R5. CZ latches are tested for 10.	R5 = 55AA	R5 = 55AA	10	AB3G2	CZxxx	6-220	Note 1 CZ latches.
	0003	The data in R5 is verified by comparing R5 with R1 using CHR instruction.	R1 = 55AA R3 = 55AA	same same	01	See Note 2.		6-220	
	0004	OHR R5, R3. CZ latches are tested for 10.	R3 = AA55 R5 = 55AA	R5 = FFFF	10	See Note 2.		6-220 6-170	Note 1.
	0005	The data in R5 is verified by comparing using CRI. Byte 0 data failed.	R5 = FFFF	R5 = FFFF	01	See Note 2.		6-220 6-170	Note 1.
	0006	Same as 0005 above except byte 1 data failed.	R5 = FFFF	R5 = FFFF	01	See Note 2.		6-220 6-170	Note 1.
	0007	OHR R1, R1. CZ latches are tested for 01.	R1 = 0000	R1 = 0000	01	See Note 2.		6-220	
	0008	Using CRI, the data in R1 is verified. Byte 0 data failed.	R1 = 0000	R1 = 0000	01	See Note 2.		6-220	
	0009	Using CRI, the data in R1 is verified. Byte 1 data failed.	R1 = 0000	R1 = 0000	01	See Note 2.		6-220	
330N	XXXX	NHR instruction test.							
	0001	NHR R1, R3. R1 data is tested by XRI. Instruction failed.	R1(1) = 09 R3(1) = 05 R1(1) = 01	R1(1) = 00	01	AB3H2 AB3J2	CD003 CA002	6-220 6-170	Decode failure. ALU controls failure.
	0002	NHR R1, R5. CZ latches are tested for 10.	R1 = AA55 R5 = FFFF	R1 = AA55	10	AB3G2	CZxxx	6-220	CZ latches.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
330N	0003	Using CRI, the data in R1 is verified. Byte 0 data failed.		R1 = AA55	01	See Note 2.		6-220 6-170	
	0004	Using CRI, the data in R1 is verified. Byte 1 data failed.		R1 = AA55	01	See Note 2.		6-220	
	0005	NHR R1, R5. CZ latches are tested for 01.	R1 = AA55 R5 = 55AA	R1 = 0000	01	See Note 2.		6-220	Note 1.
	0006	Using CRI, the data in R1 is verified. Byte 0 data failed.		R1 = 0000	01	See Note 2.		6-220 6-170	
	0007	Using CRI, the data in R1 is verified. Byte 1 data failed.		R1 = 0000	01	See Note 2.		6-220 6-170	
	0008	NHR R3, R5. CZ latches are tested for 10.	R3 = FFFF R5 = 55AA	R3 = 55AA	10	See Note 2.		6-220 6-170	Note 1.
	0009	Using CRI, the data in R3 is verified. Byte 0 data failed.		R3 = 55AA	01	See Note 2.		6-220 6-170	
	000A	Using CRI, the data in R3 is verified. Byte 1 data failed.		R3 = 55AA	01	See Note 2.		6-220 6-170	
340N	XXXX	XHR instruction test.							
	0001	XHR R1, R3. R1 data is tested by XRI. Instruction failed.	R1(1) = 09 R3(1) = 05 R1(1) = 00	R1(1) = 00	01	AB3H2 AB3J2	CD003 CA003	6-220 6-170	Decode failure. ALU controls failure.
	0002	XHR R1, R3. CZ latches are tested for 10.	R1 = 0000 R3 = AA55	R1=AA55	10	AB3G2	CZxxx	6-220	CZ latches.
	0003	Using CRI, the data in R1 is verified. Byte 0 data failed.		R1 = AA55	01	See Note 2.		6-220 6-170	
	0004	Using CRI, the data in R1 is verified. Byte 1 data failed.		R1 = AA55	01	See Note 2.		6-220	
	0005	XHR R1, R5. CZ latches are tested for 10.	R1 = AA55 R5 = FFFF	R1 = 55AA	10	See Note 2.		6-220	
	0006	Using CRI, the data in R1 is verified. Byte 0 data failed.		R1 = 55AA	01	See Note 2.		6-220 6-170	
	0007	Using CRI, the data in R1 is verified. Byte 1 data failed.		R1 = 55AA	01	See Note 2.		6-220 6-170	
	0008	XHR R1, R1. CZ latches are tested for 01.	R1 = 55AA	R1 = 0000	01	See Note 2.		6-220	
	0009	Using CRI, the data in R1 is verified. Byte 0 data failed.		R1 = 0000	01	See Note 2.		6-220 6-170	
	000A	Using CRI, the data in R1 is verified. Byte 1 data failed.		R1 = 0000	01	See Note 2.		6-220 6-170	
	000B	XHR R3, R3. CZ latches are tested for 01.	R3 = AA55	R3 = 0000	01	See Note 2.		6-220	
	000C	Using CHR, the data in R3 is verified. Data failed.		R3 = 0000	01	See Note 2.		6-220	
350N	XXXX	LHOR instruction test.							
	0001	LHOR R1, R3. R1 data is tested by XRI. Instruction failed.	R1 = XX09 R3 = 0005 R1 = 0002	R1(1) = 02	01	AB3H2 AB3J2	CD003 CAxxx	6-220 6-170	Decode failure. ALU controls failure.

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Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
350N	0002	LHOR R1, R1. The CZ latches are tested for 00.	R1 = 0102	R1 = 0881	00	AB3G2	CZxxx	6-220	CZ latches
	0003	Using CRI, the data in R1 is verified. Byte 0 data failed.		R1 = 0081	01	See Note 2.		6-220 6-170	
	0004	Using CRI, the data in R1 is verified. Byte 1 data failed.		R1 = 0081	01	See Note 2.		6-220 6-170	
	0005	LHOR R1, R1. The CZ latches are tested for 10.	R1 = 0081	R1 = 0040	10	See Note 2.		6-220	
	0006	Same as 0003 above.		R1 = 0040	01	See Note 2.		6-220	
	0007	Same as 0004 above.		R1 = 0040	01	See Note 2.		6-220	
	0008	LHOR R1, R1. C latch failed to set.	R1 = 0001	R1 = 0000	11	See Note 2.		6-220	
	0009	Same instruction as 0008. Z latch failed to set.		R1 = 0000	11	See Note 2.		6-220	
	000A	R1 data is verified for all zeros. Data failed.		R1 = 0000	01	See Note 2.		6-220	
360N	XXXX	LOR instruction test.							
	0001	LOR R1, R3. R1 data is tested by XRI. Instruction failed.	R1 = XX09 R3 = XX05 R1 = XX02	R1(1) = 00	01	AB3H2 AB3J2	CD003 CAxxx	6-220 6-170	Decode failure. ALU controls failure.
370N	XXXX	AR instruction test.							
	0001	AR R1, R3. R1 data is tested by XRI. Instruction failed.	R1 = XX09 R3 = XX05 R1 = XX0E	R1(1) = 00	01	AB3H2 AB3J2	CD003 CAxxx	6-220 6-170	Decode failure. ALU controls failure.
380N	XXXX	Byte X data flow pattern sensitivity test using the LOR and AR instructions.						6-220	See Note 2 for bit failure.
	0001	LOR R1, R1. C latch is tested for an active state.	R1 = 00001	R1 = 00000	11	See Note 2.		6-220	
	0002	Same instruction. Z latch is tested for an active state.		R1 = 00000	11	See Note 2.		6-220	
	0003	R1 is tested for all zeros. OHR R1, R1.	R1 = 00000	R1 = 00000	01	See Note 2.		6-220	
	0004	AR R1, R1. CZ latches are tested for 00.	R1 = 0C000	R1 = 18000	00	See Note 2.		6-220	
	0005	R1 byte 0 is tested to verify the data.		R1(0) = 80	01	See Note 2.		6-220	
	0006	R1 byte 1 is tested to verify the data.		R1(1) = 00	01	See Note 2.		6-220	
	0007	R1 byte X is tested to verify the data. R1 is shifted right one position to move byte X bit 7 into R1(0). CZ latches are tested for 00.	R1 = 18000 R3 = 00000	R3 = 0C000	00	See Note 2.		6-220	
	0008	R3 byte 0 is tested to verify the data.		R3(0) = C0	01	See Note 2.		6-220	
	0009	R3 byte 1 is tested to verify the data.		R3(1) = 00	01	See Note 2.		6-220	
	000A	AR R1, R1. CZ latches are tested for 00.	R1 = 18000	R1 = 30000	00	See Note 2.		6-220	
	000B	R1 byte 0 and byte 1 is tested to verify the data.		R1 = 30000	01	See Note 2.		6-220	
	000C	R1 is shifted into R3 and R3 is shifted once. This will move byte X data into byte 0. CZ latches are tested for 00.	R1 = 30000	R3 = 0C000	00	See Note 2.		6-220	
	000D	AR R3, R3/AR R3, R3. CZ latches are tested for 00.	R3 = 0AA00	R3 = 2A800	00	See Note 2.		6-220	
	000E	LOR R1, R3. CZ latches are tested for 00.	R3 = 2A800	R1 = 15400	00	See Note 2.		6-220	
	000F	R1 byte 0 is tested to verify the data.		R1(0) = 54	01	See Note 2.		6-220	
	0010	LOR R1, R1. R1 byte 0 is tested to verify the data.	R1 = 15400	R1 = 0AA00	01	See Note 2.		6-220	

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
380N	0011	LOR R1, R1/LOR R1, R1. R1 byte 0 is tested to verify the data.	R1 = 0AA00	R1 = 02A80 R1(0) = 2A	01	See Note 2.		6-220	
	0012	R1 byte 1 is tested to verify the data.		R1(1) = 80	01	See Note 2.		6-220	
3A0N	XXXX	LA instruction test.							
	0001	Using the LA instruction, R1 is loaded with 00509. The XRI instruction is used to verify the data in byte 0. Instruction failed.	R1 = 00000 R1 = 00509 R1 = 00509	R1 = 00009	01	AB3H2	CD0001	6-660	Decode failure.
	0002	LA R3, X'00000'. LA altered the CZ latches.	R3 = XXXXX	R3 = 00000	10	AB3G2	CZxxx	6-660	CZ latches.
	0003	R3 is tested to verify the data.		R3 = 00000	01	See Note 2.		6-660	Subroutine test correct byte X data.
	0004	LA R1, X'3FFFF'. LA altered the CZ latches.	R1 = 00000	R1 = 3FFFF	01	See Note 2.		6-660	
	0005	R1 is tested to verify the data.		R1 = 3FFFF	01	See Note 2.		6-660	Subroutine test correct byte X data.
	0006	LA R1, X'255AA'. R1 is tested to verify the data.	R1 = 3FFFF	R1 = 255AA	01	See Note 2.		6-660	Subroutine test correct byte X data.
	0007	LA R1, X'1AA55'. R1 is tested to verify the data.	R1 = 255AA	R1 = 1AA55	01	See Note 2.		6-660	Subroutine test correct byte X data.
3B0N	XXXX	Data flow path byte X, 0 and 1 data sensitivity test using the LA Instruction. This routine loops forty times with the LA instruction being updated on each pass.							See Note 2 for bit failures.
	0001	LA R1, test pattern. The data in R1 is tested to verify the LA instruction. The actual test of data is CHR R1, R3 where R3 is loaded via test table.		R1 = R3	01	See Note 2.		6-660 6-220	Subroutine test. Correct byte X data.
3C0N	XXXX	LR instruction test.							
	0001	LR R1, R3. R1 data is tested by XRI. Instruction failed.	R1(1) = 09 R3(1) = 05 R1(1) = 05	R1(1) = 00	01	AB3H2	CD003	6-220	Decode Failures. See Note 2 for bit failures.
	0002	LR R1, R7. The CZ latches are tested for 01.	R1 = 3FFFF R7 = 00000	R1 = 00000	01	AB3G2	CZxxx	6-220	Note 1. CZ latches.
	0003	The data in R1 is tested to verify the LR instruction.		R1 = 00000	01	See Note 2.		6-220	
	0004	LR R1, R7. The CZ latches are tested for 10.	R1 = 00000 R7 = 2AA55	R1 = 2AA55	10	See Note 2.		6-220	Note 1.
	0005	R1 is tested to verify the data.		R1 = 2AA55	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0006	LR R1, R7. The CZ latches are tested for 10.	R1 = 2AA55 R7 = 155AA	R1 = 155AA	10	See Note 2.		6-220	Note 1.
	0007	R1 is tested to verify the data.		R1 = 155AA	01	See Note 2.		6-220	Subroutine test correct byte X data.
3D0N	XXXX	Local store register 3 and 5 byte X testing.							
	0001	R7 is loaded with 30000 via LA instruction. R7 is moved into R3 and the R3 data is shifted right two positions to move byte X data into byte 0. Using CRI, the data in R3 byte 0 is tested.	R7 = 30000 R3 = 00000	R3 = 0C000	01	See Note 2.		6-600 6-220	Note 1.
	0002	Same as above except R7 is moved into R5.	R7 = 30000 R5 = 00000	R5 = 0C000	01	See Note 2.		6-660 6-220	Note 1.
	0003	Same as 0001 above except R7 is loaded with all zeros.	R7 = 00000 R3 = 0C000	R3 = 00000	01	See Note 2.		6-600 6-220	Note 1.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
3D0N	0004	Same as 0003 above except R7 is moved into R5.	R7 = 00000 R5 = 0C000	R5 = 00000	01	See Note 2.		6-660 6-220	Note 1.
	0005	Same as 0001 above except R7 is loaded with 20000.	R7 = 20000 R3 = 00000	R3 = 08000	01	See Note 2.		6-660 6-220	See Note 1.
	0006	Same as 0005 above except R7 is moved into R5.	R7 = 20000 R5 = 00000	R5 = 08000	01	See Note 2.		6-660 6-220	See Note 1.
	0007	Same as 0001 above except R7 is loaded with 10000.	R7 = 10000 R3 = 08000	R3 = 04000	01	See Note 2.		6-660 6-220	See Note 1.
	0008	Same as 0007 above except R7 is moved into R5.	R7 = 10000 R5 = 08000	R5 = 04000	01	See Note 2.		6-660 6-220	See Note 1.
3E0N	XXXX	OR instruction test.							
	0001	OR R1, R3. R1 data is tested by XRI. Instruction failed.	R1 = XXX09 R3 = XXX05 R1 = XXX0D	R1(1) = 00	01	AB3H2 AB3J2	CD003 CA003	6-220	Decode failure. ALU controls failure. See Note 2 for bit failures.
	0002	OR R1, R3. The CZ latches are tested for 01.	R1 = 00000 R3 = 00000	R1 = 00000	01	AB3G2	CZxxx	6-220	CZ latches.
	0003	The data in R1 is tested to verify byte 0 and 1.		R1 = 00000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0004	OR R1, R3. The CZ latches are tested for 10.	R1 = 255AA R3 = 1AA55	R1 = 3FFFF	10	See Note 2.		6-220	
	0005	The data in R1 is tested to verify byte 0 and 1.		R1 = 3FFFF	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0006	OR R1, R3. The CZ latches are tested for 10.	R1 = 1FFFF R3 = 2FFFF	R1 = 3FFFF	10	See Note 2.		6-220	
	0007	The data in R1 is tested to verify byte 0 and 1.		R1 = 3FFFF	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0009	OR R1, R3. The CZ latches are tested for 10.	R1 = 30000 R3 = 30000	R1 = 30000	10	See Note 2.		6-220	
	000A	The data in R1 is tested to verify byte 0 and 1.		R1 = 30000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	000B	OR R1, R3. The CZ latches are tested for 10.	R1 = 0AA55 R3 = 055AA	R1 = 0FFFF	10	See Note 2.		6-220	
	000C	The data in R1 is tested to verify byte 0 and 1.		R1 = 0FFFF	01	See Note 2.		6-220	Subroutine test correct byte X data.
3F0N	XXXX	NR instruction test.							
	0001	NR R1, R3. R1 data is tested by XRI. Instruction failed.	R1 = XXX09 R3 = XXX05 R1 = XXX01	R1(1) = 00	01	AB3H2 AB3J2	CD003 CA002	6-220	Decode failure. ALU controls failure.
	0003	OR R1, R3. The CZ latches are tested for 10.	R1 = 30000 R3 = 30000	R1 = 30000	10	See Note 2.		6-220	
	0004	The data in R1 is tested to verify byte 0 and 1.		R1 = 30000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0005	NR R1, R3. The CZ latches are tested for 01.	R1 = 2AA55 R3 = 155AA	R1 = 00000	01	See Note 2.		6-220	
	0006	The data in R1 is tested to verify byte 0 and 1.		R1 = 00000	01	See Note 2.		6-220	Subroutine test correct byte X data.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
3F0N	0007	NR R1, R3. The CZ latches are tested for 01.	R1 = 155AA R3 = 2AA55	R1 = 00000	01	See Note 2.		6-220	
	0008	The data in R1 is tested to verify byte 0 and 1.		R1 = 00000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0009	NR R1, R3. The CZ latches are tested for 10.	R1 = 0FFFF R3 = 0FFFF	R1 = 0FFFF	10	See Note 2.		6-220	
	000A	The data in R1 is tested to verify byte 0 and 1.		R1 = 0FFFF	01	See Note 2.		6-220	Subroutine test correct byte X data.
400N	XXXX	XR instruction test.							
	0001	XR R1, R3. R1 data is tested by XRI. Instruction failed.	R1 = XXX09 R3 = XXX05 R1 = XXX0C	R1(1) = 00	01	AB3H2 AB3J2	CD003 CA003	6-220 6-170	Decode failure. ALU controls failure.
	0002	XR R1, R3. The CZ latches are tested for 01.	R1 = 3AA55 R3 = 3AA55	R1 = 00000	01	AB3G2	CZxxx	6-220	CZ latches.
	0003	The data in R1 is tested to verify byte 0 and 1.		R1 = 00000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0005	XR R1, R3. The CZ latches failed.	R1 = 255AA R3 = 155AA	R1 = 30000	10	See Note 2.		6-220	
	0006	The data in R1 is tested to verify byte 0 and 1.		R1 = 30000	01	See Note 2.		6-220	Subroutine test correct byte X data
	0008	XR R1, R3. The CZ latches failed.	R1 = 1AA55 R3 = 2AA55	R1 = 30000	10	See Note 2.		6-220	
	0009	The data in R1 is tested to verify byte 0 and 1.		R1 = 30000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	000A	XR R1, R3. The CZ latches failed.	R1 = 0AA55 R3 = 055AA	R1 = 0FFFF	10	See Note 2.		6-220	
	000B	The data in R1 is tested to verify byte 0 and 1.		R1 = 0FFFF	01	See Note 2.		6-220	Subroutine test correct byte X data.
410N	XXXX	AR instruction test.							
	0001	AR R1, R3. The CZ latches failed.	R1 = 2AA55 R3 = 355AA	R1 = 1FFFF	10	AB3H2 AB3J2 AB3G2	CD003 CA002 CZxxx	6-220	Decode failure. ALU controls failure. CZ latch.
	0003	The data in R1 is tested to verify byte 0 and 1.		R1 = 10000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0004	AR R1, R3. C latch failed.	R1 = 155AA R3 = 2AA56	R1 = 00000	11	See Note 2.		6-220	
	0005	Z latch failed.		R1 = 00000	11	See Note 2.		6-220	
	0006	The data in R1 is tested to verify byte 0 and 1.		R1 = 00000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0008	AR R1, R3. The CZ latches failed.		R1 = 3FFFE	00	See Note 2.		6-220	
	0009	The data in R1 is tested to verify byte 0 and 1.	R1 = 3FFFE	R1 = 30000	01	See Note 2.		6-220	Subroutine test correct byte X data.
420N	XXXX	SR instruction test.							
	0001	SR R1, R3. R1 data is tested by XRI. Instruction failed.	R1 = 00009 R3 = 00005 R1 = 00004	R1(1) = 00	01	AB3H2 AB3J2	CD003 CA003	6-220	Decode failure. ALU controls failure.
	0002	SR R1, R3. CZ failed.	R1 = 155AA R3 = 2AA55	R1 = 2AB55	10	AB3G2	CZxxx	6-220	CZ latch.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
420N	0003	The data in R1 is tested to verify byte 0 and 1.	R1 = 2AB55	R1 = 20000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0004	SR R1, R3. CZ latches failed.	R1 = 3FFFF R3 = 3FFFF	R1 = 00000	01	See Note 2.		6-220	
	0005	The data in R1 is tested to verify byte 0 and 1.	R1 = 00000	R1 = 00000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0006	SR R1, R3. CZ latches failed.	R1 = 055AA R3 = 1AA55	R1 = 2AB55	10	See Note 2.		6-220	
	0007	The data in R1 is tested to verify byte 0 and 1.	R1 = 2AB55	R1 = 20000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0008	SR R1, R3. CZ latches failed.	R1 = 0AA55 R3 = 055AA	R1 = 054AB	00	See Note 2.		6-220	
	0009	The data in R1 is tested to verify byte 0 and 1.	R1 = 054AB	R1 = 00000	01	See Note 2.		6-220	Subroutine test correct byte X data.
430N	XXXX	CR instruction test.							
	0001	CR R1, R3. R1 data is tested by XRI. Instruction failed.	R1 = 00009 R3 = 00005	R1(1) = 00	01	AB3H2 AB3J2	CD003 CAxxx	6-220	Decode failure; ALU controls failure.
	0002	CR R1, R3. CZ latches failed.	R1 = 15555 R3 = 2AAAA	R1 = 15555	10	AB3G2	CZxxx	6-220	CZ latch.
	0003	The data in R1 is tested to verify byte 0 and 1.	R1 = 15555	R1 = 10000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0004	CR R1, R3. CZ latches failed.	R1 = 355AA R3 = 355AA	R1 = 355AA	01	See Note 2.		6-220	
	0005	The data in R1 is tested to verify byte 0 and 1.	R1 = 355AA	R1 = 30000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	0007	CR R1, R3. The CZ latches failed.		R1 = 25555	00	See Note 2.		6-220	
	0008	The data in R1 is tested to verify byte 0 and 1.	R1 = 25555	R1 = 20000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	000A	CR R1, R3. The CZ latches failed.		R1 = 0AAAA	10	See Note 2.		6-220	
	000B	The data in R1 is tested to verify byte 0 and 1.	R1 = 0AAAA	R1 = 0000	01	See Note 2.		6-220	Subroutine test correct byte X data.
	000C	CR R1, R3. CZ latches failed.	R1 = 0AA55 R3 = 0AA55	R1 = 0AA55	01	See Note 2.		6-220	
	000D	The data in R1 is tested to verify byte 0 and 1.	R1 = 0AA55	R1 = 0000	01	See Note 2.		6-220	Subroutine test correct byte X data.
440N	XXXX	L instruction test.							
	0001	Load R1 with R7 as the base register. CZ failed or load instruction failed.	R1 = 25AA5 R7 = Base Register	R1 = 1A55A	10	AB3H2 AB3J2	CDxxx CAxxx	6-390	See Note 1. Decode failure. ALU controls failure.
	0002	The data in R1 is tested to verify the L instruction.		R1 = 1A55A	01	See Note 2.		6-390	See Note 2 for bit failures.
	0003	Load R1 with R7 as the base register. CZ failed.	R1 = 1A55A	R1 = 25AA5	10	AB3G2	CZxxx	6-390	CZ latch.
	0004	The data in R1 is tested to verify the L instruction.		R1 = 25AA5	01	See Note 2.		6-390	
	0005	Load R1 and R7 as the base register.	R1 = 3FFFF	R1 = 00000	01	See Note 2.		6-390	
	0006	The data in R1 is tested to verify the L instruction.		R1 = 00000	01	See Note 2.		6-390	
450N	XXXX	LH instruction test.							
	0001	Load halfword R1 with R7 as the base register. CZ latches failed.	R1 = 2A55A	R1 = 05AA5	10	AB3H2 AB3J2	CD003 CA001	6-290	Decode failure. ALU controls failure.

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450N	0002	The data in R1 is tested to verify the LH instruction.		R1 = 05AA5	01	See Note 2.		6-290	See Note 2 for bit failures.
	0003	LH R1 with R7 as the base register failed.	R1 = 15AA5	R1 = 0A55A	10	See Note 2.		6-290	
	0004	The data in R1 is tested to verify the LH.		R1 = 0A55A	01	See Note 2.		6-290	
	0005	LH—R1 with R7 as the base register. CZ failed.	R1 = 3FFFF	R1 = 00000	01	See Note 2.		6-290	
	0006	The data in R1 is tested to verify the LH.		R1 = 00000	01	See Note 2.		6-290	
460N	XXXX	STH instruction test. R7 is used as the base register.							See Note 1.
	0001	STH instruction modified the CZ latches.		R1 = 0A55A	01	AB3H2 AB3J2 AB3G2	CD003 CAxxx CZxxx	6-360	Decode failure. ALU controls failure. CZ latch.
	0002	The data stored above is loaded via an L instruction and compared. STH failed.	R1 = 3A55A R3 = 3A55A	R3 = 3A55A	01	See Note 2.		6-360	
	0003	STH instruction modified the CZ latches.		R1 = 05AA5	10	See Note 2.		6-360	
	0004	The data stored above is loaded via an L instruction and compared. STH failed.	R1 = 35AA5 R3 = 35AA5	R1 = 35AA5 R3 = 35AA5	01	See Note 2.		6-360 6-390	
470N	XXXX	L using R0 as Operand 1.							
	0001	Load R0 with R3 as the base register. Failed to load R0.	N/A	N/A	01	AB3H2 AB3J2	CDxxx CAxxx	6-390	Decode failure. ALU control.
	0002	Load instruction with R0 as Operand 1 altered the CZ latches.	N/A	N/A	01	N/A	CZxxx	6-390	CZ latches.
480N	XXXX	L instruction test from the fullword direct addressable area.							
	0001	Load R1 from direct addressable area. CZ failed or instruction failed.	R1 = 00000	R1 = 3FFFF	10	AB3H2 AB3J2	CDxxx CAxxx	6-390	Decode failure. ALU control.
	0002	The data in R1 is tested to verify the load.		R1 = 3FFFF	01	See Note 2.		6-390	
490N	XXXX	LR (Load Register) using R0 as operand one to ensure that the CZ latches are not affected.							
	0001	LR R0, R5 when R0 is specified as operand one, a branch should occur. LR R0, R5 failed to branch to the address contained in R5.	N/A	N/A	01	AB3H2 AB3J2	CDxxx		
	0002	When R0 is specified as operand one, the CZ latches should not be altered. This error stop indicates that the CZ latches were altered.	N/A	N/A	01	AB3G2	CZxxx		
4A0N	XXXX	IC (insert character) Instruction Test.				AB3H2 AB3J2	CD003 CAxxx	6-290	Decode failure. ALU controls failure. See Note 2 for bit failure.
	0001	IC R1(1), Test Area 1 CZ failed. R3 is the base register.	R1 = 300FF	R1 = 30055	10	See Note 2.		6-290	
	0002	The data in R1 is tested to verify the IC instruction.		R1 = 30055	01	See Note 2.		6-290	
	0003	IC R1(0), Test Area 2, Z Latch failed. R3 = base register.	R1 = 3FFFF	R1 = 300FF	11	See Note 2.		6-290	
	0004	Same as 0003 except C latch failed.		R1 = 300FF	11	See Note 2.		6-290	
	0005	The data in R1 is tested to verify the IC instruction.		R1 = 300FF	01	See Note 2.		6-290	
	0006	IC R1(0), Test Area 3 CZ failed. R0 = base register.	R1 = 3FEFE	R1 = 301FE	00	See Note 2.		6-290	

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
4A0N	0007	The data in R1 is tested to verify the IC instruction.		R1 = 301FE	01	See Note 2.		6-290	
	0008	IC R1(1), Test Area 4 CZ failed. R0 = base register.	R1 = 00000	R1 = 000AA	10	See Note 2.		6-290	
	0009	The data in R1 is tested to verify the IC instruction.		R1 = 000AA	01	See Note 2.		6-290	
4B0N	XXXX	ICT (insert character and count) Instruction Test. R3 is the base register for this routine.							
	0001	ICT R1(1), R3 CZ latches were altered by the ICT instruction.	R1 = 200AA R3 = Base	R1 = 20055 R3 = Base + 1. R2 = Value of Base.	01	AB3H2 AB3J2	CDxxx CAxxx	6-480	Decode failure. ALU controls failure. See Note 2 for bit failures.
	0002	The data in R1 is tested to verify the ICT instruction.		R1 = 20055	01	See Note 2.		6-480	
	0003	The address in R3 is tested to verify if the ICT updated the base.	R3 = Base + 1	R3 = Base + 1. R2 = Base.	01	See Note 2.		6-480	
	0004	ICT R1(0), R3. CZ latches were altered by ICT instruction.	R1 = 155FF	R1 = 1AAFF R3 = Base + 2. R2 = Base.	10	See Note 2.		6-480	
	0005	The data in R1 is tested to verify the ICT instruction.		R1 = 1AAFF	01	See Note 2.		6-480	
	0006	The address in R3 is tested to verify if the ICT updated the base.		R3 = Base + 2. R2 = Base.	01	See Note 2.		6-480	
	0007	ICT R1(0), R3. CZ latches were altered by ICT instruction.	R1 = 00000	R1 = 0FF00 R3 = Base + 3. R2 = Base.	10	See Note 2.		6-480	
	0008	The data in R1 is tested.		R1 = 0FF00	01	See Note 2.		6-480	
	0009	The address in R3 is tested.		R3 = Base + 3. R2 = Base.	01	See Note 2.		6-480	
	000A	ICT R1(1), R3. CZ latches were altered by ICT Instruction.	R1 = 3FFFF	R1 = 3FF00 R3 = Base + 4. R2 = Base.	01	See Note 2.		6-480	
	000B	The data in R1 is tested.		R1 = 3FF00	01	See Note 2.		6-480	
	000C	The address in R3 is tested.		R3 = Base + 4. R2 = Base.	01	See Note 2.		6-480	
4C0N	XXXX	ST (store fullword) instruction testing.							
	0001	ST R1, Test Area R3 is the base reg for this test. The CZ latches were altered by the ST instruction.		R1 = 1A55A R3 = Base.	01	AB3H2	CD003	6-430	Decode failure. See Note 2 for bit failures.
	0002	The data stored above is loaded and tested.	R7 = 25AA5	R1 = R7 R1 = 1A55A	01				Note 1.
	0003	ST R1, test area. R3 is the base reg for this test. The CZ latches were altered by the ST instruction.		R1 = 25AA5 R3 = Base.	10	N/A	CZxxx	6-430	CZ latches.
	0004	Same as 0002 above.	R7 = 1A55A	R1 = R7 R1 = 25AA5	01	See Note 2.		6-430	See Note 1.
	0005	ST R1, direct addressable. R0 is the base reg for this test. The CZ latches were altered by the ST.		R1 = 3FFFF	01	N/A	CZxxx	6-430	CZ latches.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
4C0N	0006	The data stored above is loaded and tested.	R7 = 00000	R1 = R7 R1 = 3FFFF	01	See Note 2.		6-430	See Note 1.
	0007	Same as 0005 except different data is used.		R1 = 00000	10	See Note 2.		6-430	
	0008	Same as 0006.	R7 = 3FFFF	R1 = R7 R1 = 00000	01	See Note 2.		6-430	See Note 1.
4D0N	XXXX	STH instruction test.							
	0001	STH R1, direct addressable. R0 is the base reg. for this test. The CZ latches were altered by the STH.		R1 = FFFF	01	AB3H2	CD003	6-360	Decode failure.
	0002	The data stored above is read out via a L R3 instruction and compared.	R3 = 0000	R1 = R3 R1 = FFFF	01	See Note 2.		6-360	
	0003	Same as 0001 except different data is used.		R1 = 0000	10	See Note 2.		6-360	
	0004	Same as 0002 except different data is used.	R3 = FFFF	R1 = R3 R1 = 0000	01	See Note 2.		6-360	
4E0N	XXXX	STC Instruction Test.							
	0001	STC R1(0), test area. R3 is the base reg for this test. The CZ latches were altered by the STC.		R1 = 3AAFF	01	AB3H2	CDxxx	6-330	Decode failure.
	0002	The data stored above is read out and compared.	R7 = 300FF	R1 = R7 R1 = 0FFAA	01	See Note 2.		6-330	See Note 1.
	0003	STC R1(1), test area. R3 is the base reg for this test. The CZ latches were altered by the STC.		R1 = 3FF55	01	See Note 2.		6-330	
	0004	The data stored above is read out and compared.	R7 = 3AAFF	R1 = R7	01	See Note 2.		6-330	See Note 1.
	0005	STC R1(1), direct addressable. R0 is the base reg for this test. CZ latches were altered.		R1 = 2AAFF	10	See Note 2.		6-330	
	0006	The data stored above is read out and compared.	R7 = 30000	R1 = R7 R1 = 0FFFF	01	See Note 2.		6-330	See Note 1.
	0007	STC R1(0), direct addressable. R0 is the base reg for this test. CZ latches were altered.		R1 = 300AA	10	See Note 2.		6-330	
	0008	The data stored above is read out and compared.	R7 = 30000	R1 = R7	01	See Note 2.		6-330	See Note 1.
4F0N	XXXX	STCT (Store Character and Count) Instruction Test.							
	0001	STCT R1(0), R3. The CZ latches were altered by the STCT.	R3 = Base	R1 = 0FFAA R3 = Base + 1. R2 = Value of base.	01	AB3H2 AB3J2	CDxxx CAxxx	6-520	Decode failure. ALU control failure.
	0002	The data stored above is read out and compared.	R7 = 30055	R1 = R7 R1 = 3FF55	01	See 0001 Above.		6-520	See Note 1.
	0003	The address in R3 is tested to verify the count function.		R3 = Base + 1. R2 = Base.	01	See 0001 Above.		6-520	
	0004	STCT R1(1), R3. The CZ latches were altered by the STCT.		R1 = 3FF00 R3 = Base + 2. R2 = Base.	10	See Note 2.		6-520	

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Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
4F0N	0005	The data stored above is read out and compared.	R7 = 300FF	R1 = R7 R1 = 0FF00	01	See Note 2.		6-520	See Note 1.
	0006	The address in R3 is tested to verify the count function.		R3 = Base + 2. R2 = Base.	01	See Note 2.		6-520	
500N	XXXX	LOR instruction test for correct CZ latches. A previous routine tested the instruction decode.							
	0001	LOR R1, R1. The CZ latches failed.	R1 = 2AAAA	R1 = 15555	00	AB3H2 AB3J2 AB4R2	CDxxx CAxxx CF004	6-220	Decode failure. ALU control failure. Shift right failure.
	0002	The data in R1 is tested to verify the LOR.		R1 = 15555	01	See 0001 Above.		6-220	
	0003	LOR R1, R1. The CZ latches failed.	R1 = 15555	R1 = 0AAAA	10	See Note 2.		6-220	
	0004	The data in R1 is tested to verify the LOR.		R1 = 0AAAA	01	See Note 2.		6-220	
	0005	LOR R1, R1. CZ latches failed.	R1 = 0AAAA	R1 = 05555	00	See Note 2.		6-220	
	0006	The data in R1 is tested to verify the LOR.		R1 = 05555	01	See Note 2.		6-220	
	0007	LOR R1, R1. CZ latches failed.	R1 = 05555	R1 = 02AAA	10	See Note 2.		6-220	
	0008	The data in R1 is tested to verify the LOR.		R1 = 02AAA	01	See Note 2.		6-220	
510N	XXXX	LOR instruction test for correct CZ latches, 2 of 2.							
	0001	LOR R1, R1. CZ latches failed.	R1 = 00001	R1 = 00000	11	AB3H2 AB3J2 AB4R2	CDxxx CAxxx CF004	6-220	Decode failure. ALU control failure. Shift right failure.
	0002	The data in R1 is tested to verify the LOR.		R1 = 00000	01	See Note 2.		6-220	
530N	XXXX	ARI instruction test.							
	0001	Failure in byte X.	R1 = 1FFFF	R1 = 20000	10	AB4J2	DF009	6-170	
540N	XXXX	SRI instruction test.							
	0001	Failure in byte X.	R1 = 00000	R1 = 3FFFF	10	AB4J2	DF009	6-170	
550N	XXXX	ACR instruction test.							
	0001	Failure in byte X.	R3(0) = 03 R1 = 2FEFF	R1 = 301FF	10	AB4J2	DF009	6-220	
560N	XXXX	SCR instruction test.							
	0001	Failure in byte X.	R3(1) = 01 R1 = 30000	R1 = 2FFFF	01	AB4J2	DFxxx	6-220	Byte X.
570N	XXXX	BAL and BALR instruction test.							
	0001	BAL failed to branch. Decode failure.	N/A	N/A	01	AB3H2	CD001 thru CD004	6-570	

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
570N	0002	Above BAL altered CZ latch. CZ was 01.	N/A	N/A	01	AB3G2		6-570	
	0003	Above BAL failed to store correct value in R3.		R3 = IAR link.	N/A			6-570	
	0004	BALR failed to branch. Decode failure.		R3 = IAR link.	N/A			6-240	
	0005	Above BALR modified CZ latches.		N/A	N/A	AB3G2	CZxxx	6-240	
	0006	Above BALR failed to load Reg 1 with correct link address.		R1 = IAR link.				6-240	
	0007	An invalid register decode occurred.	N/A	N/A	N/A	N/A	N/A	6-240	A wild branch occurred or a local store register decode failure.
580N	XXXX	BCT instruction test.							
	0001	BCT did not branch. Decode failure.	R3 = 30000	R3 = 3FFFF	01	AB3H2	CD001 thru CD004	6-680	Count in low byte.
	0002	Above BCT did not decrement count.		R3 = 3FFFF		AB3J2	CAxxx	6-680	ALU control
	0003	BCT above modified the CZ latch.		R3 = 3FFFF	01	AB3G2	CZxxx	6-680	CZ latches.
	0004	BCT above failed to decrement count.		R3 = 3FFFF				6-680	Count in high byte.
	0005	BCT did not decrement properly.	R3 = 3FFFF	R3 = 3FEFF	10	AB3J2	CAxxx	6-680	
	0006	Above BCT failed to branch		R3 = 3FEFF	10	AB3H2	CDxxx	6-680	Decode.
	0007	Above BCT modified CZ latch.		R3 = 3FEFF	10	AB3G2	CZxxx	6-680	CZ latches.
	0008	Above BCT did not decrement.		R3 = 3FEFF	10	AB3J2	CAxxx	6-680	ALU
	0009	BCT modified CZ latch.	R1 = 30001	R1 = 30000	10	AB3G2	CZxxx	6-680	Count in low byte CZ latches.
	000A	Above BCT failed to decrement count.	R1 = 30001	R1 = 30000	10	AB3J2	CAxxx	6-680	Count in low byte ALU.
	000B	Above BCT decremented count to zero but branched.		R1 = 30000	N/A	AB3H2	CDxxx	6-680	Decode.
	000C	BCT modified CZ latch.	R1 = 301FF	R1 = 300FF	10	AB3G2	CZxxx	6-680	Count in high byte.
	000D	Above BCT failed to decrement count.		R1 = 300FF	N/A	AB3J2	CAxxx	6-680	ALU.
	000E	Above BCT branched when count was zero.		R1 = 300FF	N/A	AB3H2	CDxxx	6-680	Decode.
	000F	Above BCT failed to decrement count.		R1 = 300FF	N/A	AB3J2	CAxxx	6-680	ALU.
5A0N	XXXX	Register decode test for current level reg. group. The following tests will load one of the current level 'N' general register with data. Then the other six registers are 'ORed' together to test for register decode errors. Each of the remaining six should have data = 00000.							
	0001	Register decode failure. Group regs = 00000 except R1.	R1 = 00001	Same.	N/A	AB3K2	CLxxx		Decode failure for all error codes in this routine.
	0002	LR R1, R1 failed.		R1 = 00001	N/A	AB3K2	CLxxx	6-220 6-120	
	0003	Register decode failure. Group regs = 00000 except R1.	R1 = 30101	Same.	N/A	AB3K2	CLxxx	6-220 6-120	
	0004	LRI R1(1) failed.		R1 = 30101	N/A	AB3K2	CLxxx	6-170 6-120	
	0005	LCR R1(0), R1(1) failed.		R1 = 30101	N/A	AB3K2	CLxxx	6-220 6-120	

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
5A0N	0006	Register decode failure. Group regs = 00000 except R2.	R2 = 00002	Same.	N/A	AB3K2	CLxxx	6-220 6-120	
	0007	LR R1, R2 failed.		R1 = R2 R2 = 00002	N/A	AB3K2	CLxxx	6-220 6-120	
	0008	Register decode failure. Group regs = 00000 except R3.	R3 = 00003	Same.	N/A	AB3K2	CLxxx	6-120	
	0009	LR R3, R3 failed.		R3 = 00003	N/A	AB3K2	CLxxx	6-220 6-120	
	000A	Register decode failure. Group regs = 00000 except R3.	R3 = 30303	Same.	N/A	AB3K2	CLxxx	6-120	
	000B	LR1 R3(1) failed.		R3 = 30303		AB3K2	CLxxx	6-120 6-120	
	000C	LCR R3(0), R1(1) failed.		R3 = 30303		AB3K2	CLxxx	6-220 6-120	
	000D	Register decode failure. Group regs = 00000 except R4.	R4 = 00004	Same.	N/A	AB3K2	CLxxx	6-120	
	000E	LR R1, R4 failed.		R1 = R4 R4 = 00004		AB3K2	CLxxx	6-220 6-120	
5B0N	XXXX	Register decode test for current level reg group. See routine 470N above.							All error codes routine signify a decode failure.
	0001	Register decode failure. Group reg = 00000, except R5.	R5 = 00005	Same.		AB3K2	CLxxx	6-120	See Note 1.
	0002	LR R5, R5 failed.		R5 = 00005		AB3K2	CLxxx	6-220 6-120	See Note 1.
	0003	Register decode failure. Group regs = 00000, except R5.	R5 = 20505	Same.		AB3K2	CLxxx	6-120	See Note 1.
	0004	LRI R5(1) failed.		R5 = 20505		AB3K2	CLxxx	6-170 6-120	See Note 1.
	0005	LCR R5(0), R5(1) failed.		R5 = 20505		AB3K2	CLxxx	6-220 6-120	See Note 1.
	0006	Register decode failure. Group regs = 00000, except R6.	R6 = 00006	Same.		AB3K2	CLxxx	6-120	
	0007	LR R1, R6 failed.		R1 = R6 R6 = 00006		AB3K2 AB3K2	CLxxx CLxxx	6-220 6-120	
	0008	Register decode failure group regs = 00000, except R7.	R7 = 00007	Same.		AB3K2	CLxxx	6-120	See Note 1.
	0009	LR R7, R7 failed.		R7 = 00007		AB3K2	CLxxx	6-220 6-120	
	000A	Register decode failure. Group regs = 00000, except R7.	R7 = 00707	Same.		AB3K2	CLxxx	6-120	See Note 1.
	000B	LRI R7(1) failed.		R7 = 00707		AB3K2	CLxxx	6-170 6-120	See Note 1.
	000C	LCR R7(0), R7(1) failed.		R7 = 00707		AB3K2	CLxxx	6-220 6-120	See Note 1.
5C0N	XXXX	Add and subtract pattern sensitivity test; this routine loops.							BCT count in R3(1). SRI count in R7.
	0001	BCT failed to branch or altered CZ latches.	N/A	N/A	00	AB3J2	CAxxx	6-680	ARI count in R1.
	0002	BCT altered CZ latches.	N/A	N/A	00	AB3G2	CZxxx	6-680	CZ latches.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
5C0N	0003	The ARI and BCT counts are not equal. ALU failure.				See Note 2.		6-170 6-680	
	0004	The ARI and SRI counts are not equal. ALU failure.				See Note 2.		6-170 6-680	
	0005	The C latch set after an SRI instruction when result was not less than zero.			00	AB3H2 AB3G2	CDxxx CAxxx	6-170	
	0006	SRI failed to set C latch.			00	See Note 2.		6-170	
	0007	Z latch set on a non-zero SRI result.			00	See Note 2.		6-170	
	0008	Z latch failed to set on overflow ARI result.			11	See Note 2.		6-170	
	0009	C latch failed to set on overflow ARI result.			11	See Note 2.		6-170	
	000A	ARI and BCT counts not equal. ALU failure.			N/A	See Note 2.		6-170 6-680	
	000B	SRI failed to set C latch.			10	See Note 2.		6-170	
	000C	ARI did not set Byte X on overflow condition.			01	See Note 2.		6-170	
5F0N	XXXX	Input/output instruction decode test.							All input-output to Reg X '79'.
	0001	Output instruction modified CZ latch.	R7 = 30300		01	AB3H2	CDxx	6-730	See Note 1. All failures in this routine are of decode type.
	0002	Input instruction modified CZ latch.			01	AB3H2	CDxxx	6-170	
	0003	Input or output X'79' decode failure.		R3 = 00300	N/A	AB3H2	CDxxx	6-120	
	0004	Output modified CZ latch.	R7 = 00000		10	AB3H2	CDxxx	6-730	See Note 1.
	0005	Input modified CZ latch.			10	AB3H2	CDxxx	6-710	
	0006	Input or output decode failure.		R1 = 00000	N/A	AB3H2	CDxxx	6-710 6-730	
600N	XXXX	Input test for CCU LAR reg.				AB3H2 AB3M2	CD003 CS001	6-800	
	0001	Input failure R1 = R3 the address previous to inputing LAR.							
620N	XXXX	I/O register decode test. Level 1 testing only. Each general register, starting with Level 1 Reg 6 through Level 5 Reg 7, is tested. Testing is done by a subroutine.				AB3K2	CLxxx	6-120	Local store register selection failure. See Note 2 for bit failures.
	0001	OUT R1, test reg, IN R2, test reg. Either the "output" or "input" register decode failure.	R1 = Output reg data.	R1 = R2 R1 = Output reg data.	N/A	AB3K2	CLxxx	6-120	The failing register can be determined by the data in R1. Bytes 0 and 1 bits 0-3 will define the register in hex. For example, 0164 = output to X'06' (Level 1 Reg 6) 11F4 = output to X'1F' (Level 5 Reg 7)
630N	XXXX	I/O register pattern: sensitivity testing. Level 1 testing only. Each of the general registers tested above in routine 620N is tested again with 28 different patterns.				AB3K2	CLxxx	6-120	Local store register selection failure. See Note 2 for bit failures.
	0001	OUT R1, test reg, IN R4, test reg. The data in R2 and R4 failed to compare.		R1 = R4 R2 = Test pattern. R3 = Test reg data.	N/A	AB3K2	CLxxx	6-120	R3 bytes 0 and 1 bits 0-3 defines the register, in hex.

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Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
650N	XXXX	Level 1 to Level 2 setup test. A subroutine is used to unmask Level, set Diag L2 interrupt and prepares to exit Level 1.				AB3M2	CPxxx		Program level failure.
	0001	Interrupt requests group 1 has outstanding bits on. Reg X'7E'.		R1 = Reg X'7E'.	01	AB3M2	CPxxx	6-850	
	0002	Diag L2 interrupt request interrupt bit is not on interrupt request group 2. Reg X'7F'.		R1 = Reg X'7F'. R1 = 8004	01	AB3M2	CPxxx	6-850	
660N	XXXX	General register setup. Exit Level 1.							
	0001	Same test and error data as that listed in routine 620N.							
	0002	Exit instruction failed to exit Level 1.		N/A	N/A	AB3M2	CPxxx	6-750	Program level failure.
	0003	The Level 1 exit did not exit to Level 2 but returned to Level 1.	N/A	N/A	N/A	AB3M2	CPxxx	6-750	See Note 3.
	0004	Level 1 exited to Level 3 instead of Level 2.	N/A	N/A	N/A	AB3M2	CPxxx	6-750	See Note 3.
	0005	Level 1 exited to Level 4 instead of Level 2.	N/A	N/A	N/A	AB3M2	CPxxx	6-750	See Note 3.
	0006	Level 1 exited to Level 5 instead of Level 2.	N/A	N/A	N/A	AB3M2	CPxxx	6-750	See Note 3.
670N	XXXX	General register interaction testing. Once the basic routines have been run under program Level 2, the general registers for Level 3 R0 through Level 5 R7 are tested to verify that the Level 2 programs did not alter the data previously stored by routine 630N.				AB3K2 AB3M2	CLxxx CPxxx		Register selection. Program level failure.
	0001	Interaction between Level 2 and some other general register.	R4 = Expected data. R2 = Actual data. R1 = Input reg data.		N/A			6-120	The failing register can be determined by the data in R1. Bytes 0 and 1 bits 0-3 will define the register, in hex.
690N	XXXX	I/O register decode testing. Level 2 testing only.							
	0001	OUT R1, test reg, IN R2, test reg. Register decode failed. Previously tested under program Level 1, must be level sensitive.	R1 = Output reg data.	R1 = R2 R1 = Output reg data.	N/A	AB3K2	CLxxx	6-120	R1 bytes 0 and 1 bits 0-3 defines the register, in hex. Register selection see Note 2 for bit failures.
6A0N	XXXX	I/O register pattern sensitivity testing. Level 2 testing only.				AB3K2	CLxxx		Register selection. See Note 2 for bit failures.
	0001	OUT R2, test reg, IN R4, test reg. Previously tested under program Level 1, must be level sensitive.		R2 = R4 R2 = Test pattern. R3 = Test reg data.	N/A	AB3K2	CLxxx		R3 bytes 0 and 1 bit 0-3 defines the register in hex.
6C0N	XXXX	Level 2 to Level 3 setup test. A subroutine is used to mask Level 2, unmask Level 3, reset diag L2 request interrupt, and prepares to exit Level 2.				AB3M2	CPxxx		Program level failure.
	0001	Diag L2 interrupt request bit failed to reset.		R1 = Reg X'7F'.	N/A	AB3M2	CPxxx	6-070	Reg X'7F' byte 0 bit 0 equals Diag L2 request.
	0002	PCI L3 interrupt request bit failed to set. Reg X'7F'. Byte 1 Bit 6.		R1 = Reg X'7F'.	N/A	AB3M2	CPxxx	6-070 6-860	
	0003	PCI L3 interrupt request bit fialed to reset or other interrupt bits are on. Reg X'7F'. Byte 1 Bit 6.		R1 = Reg X'7F'.	N/A	AB3M2	CPxxx	6-070 6-860	Reg X'7F' byte 0 equals PCI L3 interrupt.
6D0N	XXXX	General register setup. Exit Level 2.							
	0001	Same test and error data as listed above under routine 690N.						6-120	

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
6D0N	0002	Exit instruction failed to exit L2.	N/A	N/A	N/A	AB3M2 AB3K2	CPxxx CLxxx	6-070 6-750	Program level failure. Register selection.
	0003	Level 2 exited to Level 1 instead of Level 3.	N/A	N/A	N/A	AB3M2 AB3K2	CPxxx CLxxx	6-070 6-750	See Note 3.
	0004	Level 2 exited to Level 2 instead of Level 3.	N/A	N/A	N/A	AB3M2 AB3K2	CPxxx CLxxx	6-070 6-750	See Note 3.
	0005	Level 2 exited to Level 4 instead of Level 3.	N/A	N/A	N/A	AB3M2 AB3K2	CPxxx CLxxx	6-070 6-750	See Note 3.
	0006	Level 2 exited to Level 5 instead of Level 3.	N/A	N/A	N/A	AB3M2 AB3K2	CPxxx CLxxx	6-070 6-750	See Note 3.
6F0N	XXXX	General register interaction test. Once the basic routines have been run under program Level 3, the general registers for Level 4 Reg 0 through Level 1 Reg 7 are tested to verify that the Level 3 programs did not alter the data previously stored by routine 6D0N.				AB3K2 AB3M2	CLxxx CPxxx		Register selection. Program level failure.
	0001	Interaction between Level 3 and some other general register.		R4 = Expected data. R2 = Actual. R1 = Input reg data.	N/A	AB3K2 AB3M2	CLxxx CPxxx	6-120	R1 bytes 0 and 1 bits 0-3 defines register in hex.
700N	XXXX	I/O register decode test. Level 3 testing only.		R1 = R2		AB3K2	CLxxx		Register selection.
	0001	OUT R1, test reg, IN R2, test reg. Register decode failed. Previously tested under program Levels 1 & 2.		R1 = Output reg data.	N/A	AB3K2	CLxxx	6-120	R1 bytes 0 and 1 bits 0-3 defines the register in hex.
710N	XXXX	I/O register pattern sensitivity test. Level 3 testing only.				AB3K2	CLxxx		Register selection. See Note 2 for bit failure.
	0001	OUT R2, test reg, IN R4, test reg. Previously tested under program Level 1 and 2 (must be Level sensitive).		R2 = R4 R2 = Test pattern. R3 = Test reg data.	N/A	AB3K2	CLxxx		R3 bytes 0 and 1 bits 0-3 define the register in hex.
730N	XXXX	Level 3 to Level 4 setup test. A subroutine is used to mask Level 3, unmask Level 4, reset PCI L3 request, set PCI L4 request, and prepares to exit Level 3.				AB3M2	CPxxx		Program level failure.
	0001	PCI L3 interrupt request bit failed to reset. Reg X'7F' Byte 1 Bit 6.		R1 = Reg X'7F'	N/A	AB3M2	CPxxx	6-860	
	0002	PCI L4 interrupt request bit failed to set. Reg X'7F' Byte 0 Bit 7.		R1 = Reg X'7F'	N/A	AB3M2	CPxxx	6-860	
	0003	Outstanding bits on in Reg X'7F'.		R1 = 0000	01	AB3M2	CPxxx	8-870	
740N	XXXX	General register setup. Exit Level 3.							
	0001	Same test and error data as listed above under routine 700N.						6-120	
	0002	Exit instruction failed to exit L3.	N/A	N/A	N/A	AB3K2 AB3M2	CLxxx CPxxx	6-070 6-750	Register selection. Program level failure.
	0003	Level 3 exited to Level 1 instead of Level 4.		N/A	N/A	AB3K2 AB3M2	CLxxx CPxxx	6-070 6-750	See Note 3.
	0004	Level 3 exited to Level 2 instead of Level 4.		N/A	N/A	AB3K2 AB3M2	CLxxx CPxxx	6-070 6-750	See Note 3.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
740N	0005	Level 3 exited to Level 3 instead of Level 4.		N/A	N/A	AB3K2 AB3M2	CLxxx CPxxx	6-070 6-750	See Note 3.
	0006	Level 3 exited to Level 5 instead of Level 4.		N/A	N/A	AB3K2 AB3M2	CLxxx CPxxx	6-070 6-750	See Note 3.
760N	XXXX	I/O register interaction testing. Once the basic routines have been run under program Level 4, the general registers for Level 5 Reg 0 through Level 3 Reg 7 are tested to verify that the Level 4 programs did not alter the data previously stored by routine 740N.				AB3K2 AB3M2	CLxxx CPxxx		Register selection. Program level failure. See Note 2 for bit failures.
	0001	Interaction between Level 4 and some other general register.		R4 = Expected data. R2 = Actual. R1 = Input reg data.	N/A	AB3K2 AB3M2	CLxxx CPxxx	6-070	R1 bytes 0 and 1 bits 0-3 define the register in hex.
770N	XXXX	I/O register decode testing Level 4 testing only.				AB3K2	CLxxx		Register selection.
	0001	OUT R1, test reg, IN R2, test reg. Register decode failed. Previously tested under program Levels 1, 2 and 3.		R1 = R2 R1 = Output reg data.	N/A	AB3K2	CLxxx	6-120	R1 byte 0 bits 0. Bits 0-3 defines the register in hex.
780N	XXXX	I/O register pattern sensitivity testing. Level 4 testing only.				AB3K2	CLxxx		Register selection. See Note 2 for bit failures.
	0001	OUT R2, test reg, IN R4, test reg. Previously tested under program Levels 1, 2, and 3.		R2 = R4 R2 = Test pattern. R3 = Test reg data.	N/A	AB3K2	CLxxx		R3 bytes 0 and 1 bits 0-3 defines the register in hex. See Note 2.
7A0N	XXXX	Memory addressing test runs only under program Level 4.				AB3K2 AB4E2	CLxxx CMxxx		Register selection. Address exception failure.
	0001	Invalid fold occurred at address in R1. Fold occurs when maximum address of 64K or 256K is incremented and wraps back to address zero, and is therefore valid only if storage size = 64K or 256K.		R1 = Address of fold.	N/A	AB3K2 AB4E2	CLxxx CMxxx		
	0002	Fold failed to occur. Address determined by input X'70' did not cause fold to address X'0000'. Fold should occur if 64K or 256K.		R1 = Address. R3 = Max address per X'70'.		AB3K2 AB4E2	CLxxx CMxxx		
	0003	Storage size input, Reg X'70' appears to be in error. Address exception was set prior to reaching the maximum address derived from data in Reg X'70'.		R1 = Address of error. R3 = Max address derived from X'70'.	N/A	AB3K2 AB4E2	CLxxx CMxxx	6-770 6-005	
	0004	Unexpected Level 1 request bits in Reg X'7E'.		R7 = X'7E'	N/A	AB3K2 AB4E2	CLxxx CMxxx	6-850	
	0005	Failed to set address exception.		R1 = Address of error.	N/A	AB3K2 AB4E2	CLxxx CMxxx	6-005	
	0006	Level 1 interrupt but address exception bit is not on. Byte 1 Bit 1 Reg X'7E'.		R3 = X'7E'	N/A	AB3K2 AB4E2	CLxxx CMxxx	6-850	
	0007	Address exception bit failed to reset. Output to Reg X'77'.		R3 = X'7E'	N/A	AB3K2	CLxxx	6-900	
	0008	Data failure. The data stored at each location is its own address value. As a result, R3 equals both the expected data and the address that failed.		R3 = Expected. R5 = Actual.	01	AB3K2 AB4E2	CLxxx CMxxx	7-020 7-030	
	0009	Address exception failed to set when attempting to load a halfword from an invalid address.		R3 = Address of error.	01	AB3K2 AB4E2	CLxxx CMxxx	6-050	

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
7A0N	000A	Address exception error occurred while attempting to load a halfword from a valid address.		R3 = Address.	N/A	AB3K2 AB4E2	CLxxx CMxxx	6-050	
	000B	An address exception error occurred but failed to trap to Level 1.		R5 = Reg X'7E'	N/A	AB3K2 AB4E2	CLxxx CMxxx	6-050	
7B0N	XXXX	Level 4 to Level 5 setup test. A subroutine is used to mask Level 4, unmask Level 5, reset PCI L4 request, and prepares to exit Level 4.				AB3M2	CPxxx		Program level failure.
	0001	Outstanding bits are on in either interrupt request Group 1 or 2 (X'76', X'77'), excluding the timer L3 bit.		R1 = the 'OR' of regs X'7E' and X'7F'.	N/A	AB3M2	CPxxx	6-810 6-820	
7C0N	XXXX	General register setup exit Level 4.							
	0001	Same test and error data as listed above under routine 770N.							
	0002	Exit instruction failed to exit L4.		N/A	N/A	AB3M2 AB3K2	CPxxx CLxxx	6-070 6-750	Program level. Failure register selection.
	0003	Level 4 exited to Level 1 instead of Level 5.		N/A	N/A	AB3M2 AB3K2	CPxxx CLxxx	6-070 6-750	See Note 3.
	0004	Level 4 exited to Level 2 instead of Level 5.		N/A	N/A	AB3M2 AB3K2	CPxxx CLxxx	6-070 6-750	See Note 3.
	0005	Level 4 exited to Level 3 instead of Level 5.		N/A	N/A	AB3M2 AB3K2	CPxxx CLxxx	6-070 6-750	See Note 3.
	0006	Level 4 exited to Level 4 instead of Level 5.		N/A	N/A	AB3M2 AB3K2	CPxxx CLxxx	6-070 6-750	See Note 3.
7F0N	XXXX	Level 5 to Level 1 setup test. A subroutine is used to mask Level 5 and prepares to return to Level 1.				AB3M2	CPxxx		Program level failure.
	0001	An "output" instruction is executed under program Level 5 in order to force a Level 1 interrupt. The output failed to set I/O check Level 1 or mask Level 5 failed.		N/A	N/A	AB3M2	CPxxx	6-050	
	0002	The I/O check above trapped to Level 2 instead of Level 1.		N/A	N/A	AB3M2	CPxxx	6-070	
	0003	The I/O check above trapped to Level 3 instead of Level 1.		N/A	N/A	AB3M2	CPxxx	6-070	
	0004	The I/O check above trapped to Level 4 instead of Level 1.		N/A	N/A	AB3M2	CPxxx	6-070	
800N	XXXX	I/O register interaction testing. Once the basic routines have been run under program Levels 2, 3, 4, and 5, the program makes an additional pass under program Level 1. Then the general registers for Level 3 Reg 0 through Level 5 Reg 7 are tested for any interaction.				AB3K2	CLxxx		Register selection. See Note 2 for bit failures.
	0001	Interaction did occur.		R4 = Expected Data. R2 = Actual. R1 = Input reg data.	N/A	AB3K2	CLxxx		R1 bytes 0 and 1 bits 0-3 define the register in hex.
810N	XXXX	Reset Level 1 in/out check L1 test.							
	0001	Output to Reg X'77' with data X'0004' failed to reset check.		R1 = X'7E'	N/A	AB3G2 AB3L2	CQ004 CU014	6-900	Output X'77' failure. I/O check latch failure.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments
XX0N	1001	Routine continuity error. At the start of a given routine R1 is loaded with a value equal to the given routine number, this value is then compared to a "current routine number" which is read from a table. As a result, should a wild branch(s) occur, this trap should catch it.	N/A	R1 should equal R3. R1 = Actual. R3 = Expected.	N/A	N/A	N/A		
	1002	Subroutine to test Byte X. Since the fullword instructions have not been tested during the first two passes through this subroutine, the data in R1 is shifted right two places and then tested using XOR halfword.	R1 = Actual. R3 = Expected.	R1 should equal R3.	01	AB4J2	DFxxx	6-220	'X' Byte failure.
	2001	Level 5 to Level 1 interrupt handler. Unable to reset Level 1 request bits. Output to Reg X'77' with data X'C00C'.		R1 = Reg X'7E'	01	AB3G2 AB3M2	CQ004 CPxxx	6-900	Output X'77' failure. Program level failure.
	2002	Exit from Level 1 handler failed. Previously tested.		N/A	N/A	N/A		6-070	
	2003	While running under program Level 2, an unexpected Level 1 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2004	While running under program Level 2, an unexpected Level 2 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2005	While running under program Level 2, an unexpected Level 3 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2006	While running under program Level 2, an unexpected Level 4 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2008	While running under Level 3, an unexpected Level 1 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2009	While running under program Level 3, an unexpected Level 2 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	200A	While running under program Level 3, an unexpected Level 3 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	200B	While running under program Level 3, an unexpected Level 4 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	200D	While running under program Level 4, an unexpected Level 1 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	200E	While running under program Level 4, an unexpected Level 2 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	200F	While running under program Level 4, an unexpected Level 3 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2010	While running under program Level 4, an unexpected Level 4 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2012	While running under program Level 5, an unexpected Level 2 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2013	While running under program Level 5, an unexpected Level 3 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2014	While running under program Level 5, an unexpected Level 4 interrupt occurred. Second pass through Level 1 after running test under program Levels 2, 3, 4, and 5.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2015	Unexpected Level 1 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2016	Unexpected Level 2 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2017	Unexpected Level 3 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2018	Unexpected Level 4 interrupt occurred.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2019	Program Level 5 became the active program level while attempting to run under either program Level 1, 2, 3, or 4. To determine which level should be active, look at the data in display register B. Bits 1.4 through 1.7 define the program level under test (see page 3-010).		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2020	While running under program Level 5, a Level 1 interrupt occurred and the I/O check bit was not on.		N/A	N/A	N/A	N/A	6-070	See Note 3.
	2021	Subroutine to handle timer Level 3 interrupts. An attempt to reset the timer Bit (X'7F' 1.5) failed. Output X'77' with data X'0040' was used to attempt the reset.	N/A	R7 = EXT Reg X'7F'.	N/A	A-B3L2	CP007		See Note 3.

Routine	Error Code	Function Tested and Error Description	PROG LEV 'N' Prior to Test Inst. Execution	Expected and Actual Results in PROG LEV 'N' Req.	CZ Latch Results	Suspected Card Location(s)	FEALD Page	FETMM Page	Comments

NOTES:

Note 1. The error reporting subroutine uses registers R5 and R7. As a result, if you want to observe the data values expressed for a given error code, record the data in R5 and R7 at the initial out stop.

Note 2. Use the following chart to determine the suspected card or cards for all ALU or data sensitive errors. The card should be identified from the failing bits in the register as defined under "expected results". Once a given instruction is tested for a basic ALU and CZ Latch setting, then any errors that follow are due to data sensitivity.

BITS IN ERROR	CARD	LOGIC PAGE
Byte X, Bits P, 6, 7	A-B4J2	DFXXX
Byte 0, Bits P, 0, 1	A-B4K2	DGXXX
Byte 0, Bits 2, 3, 4	A-B4L2	DHXXX
Byte 0, Bits 5, 6, 7	A-B4M2	DJXXX
Byte 1, Bits P, 0, 1	A-B4N2	DKXXX
Byte 1, Bits 2, 3, 4	A-B4P2	DLXXX
Byte 1, Bits 5, 6, 7	A-B4Q2	DMXXX

Note 3. This error cannot be looped using the INIT loop on error option.

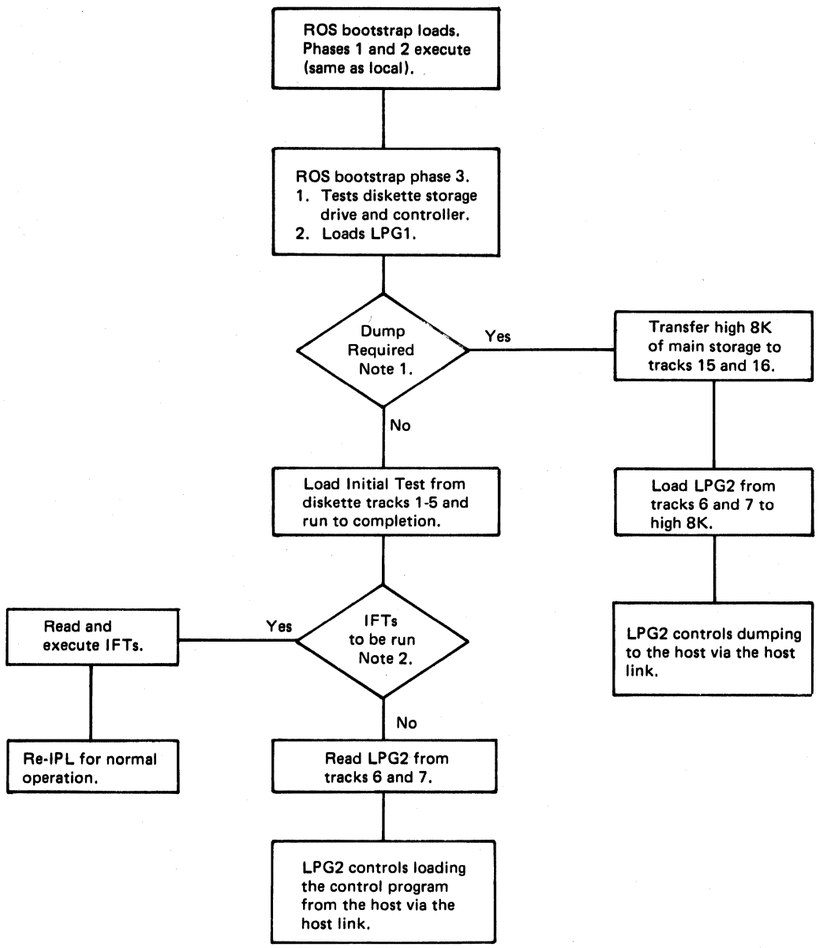
REMOTE PROGRAM LOADER

The 3705-80 includes either a remote program loader (RPL) alone or a remote program loader and either a type 1 or a type 4 channel adapter (CA). The RPL consists of a ROS bootstrap program, an IBM diskette storage device, and a diskette controller that together provide a remote IPL capability for the 3705-80.

The contents of the RPL diskette is shown in the following chart. Note that while using the RPL, the ability to write on the diskette is disabled.

Track	*Content*	*Description*
0	Load Program 1	(1) Program that is transferred to main storage by the ROS boot-strap to control further loading of programs. (2) Defines the local/ remote communication link for LPG2 (IPL configuration data set).
1-4	(3705-80) Initial Test	A CCU diagnostic exerciser.
5	(3705-80) (Reserved)	
6-7	Load Program 2 (LPG2)	Controls the local/remote communication link for loading and dumping.
8	IFT Loader/CDS Writer	
9	Diagnostic Control Monitor	
10	Hardware Configuration Data Internal Functional Tests (IFT)	Defines the hardware configuration for the internal functional tests.
11	Load Program 1	Duplicate of track 0.
12-13	Load Program 2	Duplicate of tracks 6 and 7.
14-16	(Reserved)	
17	Subroutine (LPG1 Dump)	
18	Reserved	
19-76	IFT	Internal Functional Tests.

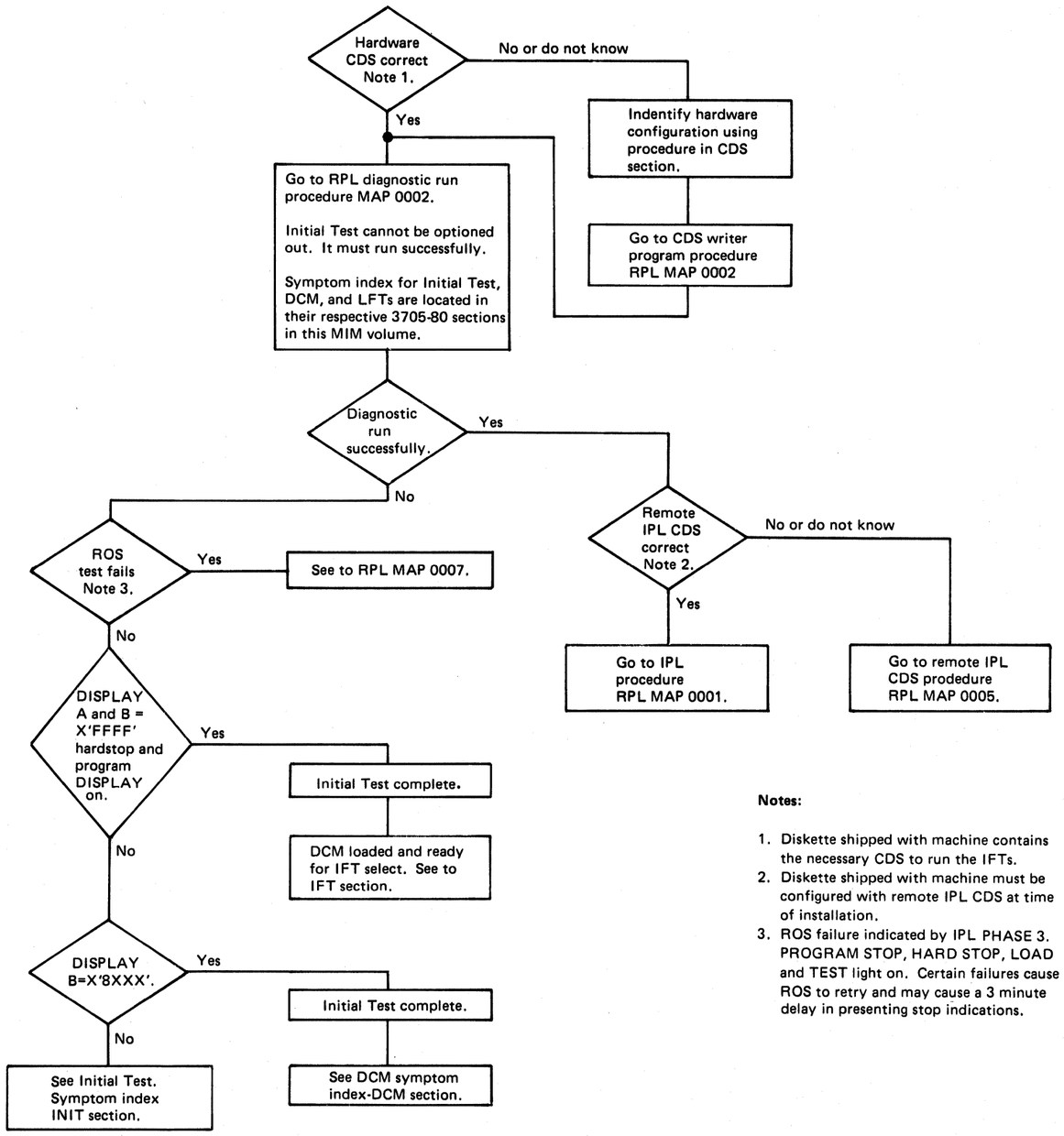
IPL 3705-80 (RPL Feature)



Notes:

1. Set the STORAGE ADDRESS/REGISTER DATA switches to X'0BBBB'.
2. Set the STORAGE ADDRESS/REGISTER DATA switches to X'0DDDD' and the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.

RPL Diagnostic Checkout and Remote IPL



Notes:

1. Diskette shipped with machine contains the necessary CDS to run the IFTs.
2. Diskette shipped with machine must be configured with remote IPL CDS at time of installation.
3. ROS failure indicated by IPL PHASE 3, PROGRAM STOP, HARD STOP, LOAD and TEST light on. Certain failures cause ROS to retry and may cause a 3 minute delay in presenting stop indications.

PAGE 1 OF 3

ENTRY POINTS

FROM	ENTER THIS MAP		
MAP NUMBER	ENTRY POINT	PAGE NUMBER	STEP NUMBER

No entries in this table

EXIT POINTS

EXIT THIS MAP		TO	
PAGE NUMBER	STEP NUMBER	MAP NUMBER	ENTRY POINT
3	031	0002	A
1	004	0003	A
2	020	0003	A
3	030	0004	A
1	003	0005	A

001
(Entry Point A)

The remote IPL CDS and the hardware CDS must be configured properly to use the diskette media successfully.
HAVE THE CONFIGURATION DATA SETS (CDS) BEEN CONFIGURED PROPERLY?
Y N

002
DO YOU WISH TO UPDATE THE HARDWARE CDS?
Y N

003
To update Remote IPL CDS -
Go To Map 0005, Entry Point A.

004
Go To Map 0003, Entry Point A.

005
ARE THE DIAGNOSTICS TO BE RUN?
Y N

006
DO YOU WISH TO UPDATE OR ZAP A PROGRAM?
Y N

3 3 2
A B C

C
1

PAGE 2 OF 3

007
DO YOU WISH TO RUN THE PANEL LINE TEST?
Y N

008
DO YOU ANTICIPATE OR DESIRE A STORAGE DUMP?
Y N

009
(Entry Point B)

1. Set ENABLE/DISABLE switch(s) to DISABLE.
2. Set the DISPLAY/FUNCTION SELECT switch to REGISTER ADDRESS.
3. Press RESET.
4. Press LOAD.

The normal run time for ROS, LPG1, Initial test, and LPG2 is approximately 30 seconds. ROS tries to recover from errors that may cause a 3-minute delay before an error stop occurs.

DOES DISPLAY A CONTAIN X'FCXX'?
Y N

010
DOES DISPLAY A CONTAIN X'CCXX'?
Y N

011
IS THE 3705 LOOPING?
Y N

3 3 3 3 3
D E F G H

J

012
IS THE IPL PHASE 1, 2, OR 3 LIGHTS ACTIVE?
Y N

013
DOES DISPLAY A CONTAIN X'0CXX'?
Y N

014
DOES DISPLAY A CONTAIN X'ECXX'?
Y N

015
DOES DISPLAY A AND B CONTAIN X'FFFF'?
Y N

016
DOES DISPLAY B CONTAIN X'8XXX'?
Y N

017
See Initial Test Symptom Index, INIT Section.
If the DISPLAY B data does not compare with any of the initial test routines, refer to Volume 2 and check out the CE panel.

018
See DCM Symptom Index, DCM Section.

019
The DCM is the active program. Go to the DCM Section.

020
CDS Writer Program is the active program.
Go To Map 0003, Entry Point A.

021
DOES DISPLAY B CONTAIN X'80XX'?
Y N

022
IFT Diskette Loader is the active program.
See the IFT Diskette Loader Symptom Index, this section.

3 3
K L

E 2 F 2 G 2 H 2 K 2 L 2 **IPL PROCEDURE**

PAGE 3 OF 3

023
See the DCM Symptom Index, DCM Section.

024
See ROS Symptom Index.

025
Go to Load Program 2 (LPG2) Symptom Index, this section.

026
Load Program (LPG1) is the Active Program.
Go to LPG1 Symptom Index, MAP 0008.

027
Load Program 2 is active. See LPG2 Symptom Index in this section to determine meaning of display codes.

028
Set the STORAGE ADDRESS REGISTER DATA switches to X'0BBBB'.
Go to Page 2, Step 009, Entry Point B.

A 1 B 1 D 2 MAP 0001-3

029
Go to the panel line test procedure, PNL LN TEST Section.

030
Go To Map 0004, Entry Point A.

031
Go To Map 0002, Entry Point A.

PAGE 1 OF 1

001
Set ENABLE/DISABLE switch(s) to DISABLE.

Set the DISPLAY/FUNCTION SELECT switch to the STORAGE ADDRESS position.

Set the STORAGE ADDRESS/REGISTER DATA switches to X'0DDDD'.

Press RESET. Press LOAD, and then press the panel INTERRUPT pushbutton.

The IPL sequence should be active at this point. During IPL Phase 3, ROS reads load program 1 from diskette and passes control to LPG1. LPG1 determines the type of load (NCP, with or without dump option, or diagnostics) being requested via either the CE panel or IPL register X'6B'. LPG1 will attempt to read the appropriate program from diskette and pass control to it. If errors occur, while attempting to read either initial test or the IFT diskette loader from diskette or while the dump option is active, LPG1 defaults to a LPG2 load.

Normal run time for a ROS/LPG1/Initial Test/IFT diskette loader is approximately 30 seconds.

Note: Under abnormal conditions, such as no index pulses or diskette media in the diskette drive, ROS attempts to retry. This may cause a 3-minute delay before an error stop occurs.

DISPLAY REGISTER A AND B = X'FFFF'?
Y N

002
DISPLAY REGISTER B = X'8XXX'?
Y N

003
See Initial test symptom index. If the DISPLAY B data does not compare with any of the initial test routines, refer to Volume 2 and check out the CE Panel (CTRL PNL Section).

004
See DCM Symptom Index (DCM Section).

005
Control has been passed to the DCM and it is ready for an IFT request. See IFT Section.

CDS WRITER PROGRAM PROCEDURE

PAGE 1 OF 2

001
(Entry Point A)

Install the write enable jumper.

3705-80 - Pin 01A-B1G2S02 to ground.

Set ENABLE/DISABLE switch(s) to DISABLE.

Set the DISPLAY/FUNCTION SELECT switch to the REGISTER ADDRESS position.

Set the STORAGE ADDRESS/REGISTER DATA switches to X'0DDDD'.

1. Press RESET.
2. Press LOAD.
3. Press the panel INTERRUPT button.

The IPL sequence should be active at this point. During IPL Phase 3, ROS will read load program 1 from diskette and pass control to LPG1. LPG1's determines the type of load (NCP, with or without dump option, or diagnostics) being requested via either the CE panel or IPL register X'6B'. LPG1 attempts to read the appropriate program from diskette and pass control to it. If errors occur, while attempting to read either initial test or the IFT diskette loader from diskette or while the dump option is active, LPG1 will default to a LPG2 load.

Normal run time for a ROS/LPG1/initial test/IFT diskette loader is approximately 30 seconds.
NOTE: Under abnormal conditions, such as no index pulses or diskette media in the diskette drive, ROS will attempt to retry. This may cause a 3-minute delay before an error stop occurs.

DISPLAY REGISTER A = X'ECXX'?
Y N

002
See CDS Writer Symptom Index (this section).

A

A

003
The CDS Writer is the active program.
DISPLAY REGISTER B = X'3001'?
Y N

004
The first function of the CDS writer program is to test the write capability of the remote loader adapter. A test pattern is written onto track X'0F' and then read back to verify the write. The code X'3001' in DISPLAY B indicates that the write test was good. The CDS Writer is waiting a command.
See CDS Writer Symptom Index (this section).

005
Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 2.

Set the STORAGE ADDRESS/REGISTER DATA switches to X'00002'.

Press START.

(Entry Point B)

The hardware CDS will be read into storage from track X'0A'.
DISPLAY REGISTER B = X'3024'?
Y N

006
See CDS Writer Symptom Index (this section).

2
B

B
1

CDS WRITER PROGRAM

PAGE 2 OF 2

007
Change the hardware CDS by altering storage as required. Only those bytes that are affected need be changed.

Refer to CDS Section for definition.
The CDS are located at X'F00' plus (+) the value of the byte location that is specified on the individual CDS cards.

It is possible to transfer the current hardware CDS from one diskette to another by changing the diskette medias at this point.

When ready to write the new CDS, set the STORAGE ADDRESS/ REGISTER DATA switches to X'0EEEE'.
Press START.
DISPLAY REGISTER B = X'302F'?
Y N

008
See CDS Writer Symptom Index (this section).

009
Indicates that the hardware CDS has been written on track X'0A' without errors.
ANY MORE HARDWARE CDS TO BE CHANGED?
Y N

010
Remove the write enable jumper.
Re-IPL.

011
Press START.
Go to Page 1, Step 005, Entry Point B.

PROGRAM ZAPPER PROCEDURE

PAGE 1 OF 2

001
(Entry Point A)

Install the write enable jumper.

3705-80 - Pin 01A-B1G2S02 to ground.

Set ENABLE/DISABLE switch(s) to DISABLE.

Set the DISPLAY/FUNCTION SELECT switch to the REGISTER ADDRESS position.

Set the STORAGE ADDRESS/REGISTER DATA switches to X'0DDDD'.

Press RESET. Press LOAD, and then press the panel INTERRUPT button.

The IPL sequence should be active at this point. During IPL Phase 3, ROS will read load program 1 from diskette and pass control to LPG1. It is LPG1's function to determine the type of load (NCP, with or without dump option, or diagnostics) being requested via either the CE panel or IPL register X'6B'. LPG1 will attempt to read the appropriate program from diskette and pass control to it. If errors occur, while attempting to read either initial test or the IFT diskette loader from diskette or while the dump option is active, LPG1 will default to a LPG2 load.

Normal run time for a ROS/LPG1/Initial Test/IFT diskette loader is approximately 30 seconds.
Note: Under abnormal conditions, such as no index pulses or diskette media in the diskette drive, ROS will attempt to retry. This may cause a 3-minute delay before an error stop occurs.

DISPLAY REGISTER A = X'ECXX'?
Y N

002
See CDS Writer Symptom Index (this section).

A

A MAP 0004-1

003
The CDS Writer is the active program.
DISPLAY REGISTER B = X'3001'?
Y N

004
The first function of the CDS writer program is to test the write capability of the remote loader adapter. A test pattern is written onto track X'0F' and then read back to verify the write. The code X'3001' in DISPLAY B indicates that the write test was good. The CDS Writer is waiting a command.
See CDS Writer Symptom Index (this section).

005
Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 2.
Set the STORAGE ADDRESS/REGISTER DATA switches to X'0003'.
Press START.

(Entry Point B)

DISPLAY REGISTER B = X'3031'?
Y N

006
See CDS Writer Symptom Index (this section).

007
The Program Zapper is active.

Enter the program ID into the STORAGE ADDRESS/REGISTER DATA switches
Note: The program ID will be supplied with the Zap instructions.

Set the DISPLAY/FUNCTION SELECT switch to position 2.
Press START.
DISPLAY REGISTER B = X'3034'?
Y N

008
See CDS Writer Symptom Index (this section).

2
B

B MAP 0004-1

1

PROGRAM ZAPPER PROCEDURE

MAP 0004-2

PAGE 2 OF 2

009
The given program has been read into storage. Apply the program Zap (by altering storage) per given instructions. When ready to write the given program back onto diskette, set the STORAGE ADDRESS/REGISTER DATA switches to X'0EEEE'.
Press START.
DISPLAY REGISTER B = X'303F'?
Y N

010
See CDS Writer Symptom Index (this section).

011
Indicates that the given program has been written onto diskette without errors.
ANY MORE PROGRAM ZAP'S TO BE APPLIED?
Y N

012
Remove the write enable jumper.
Re-IPL.

013
Press START.
Go to Page 1, Step 005, Entry Point B.

MAP 0004-2

REMOTE IPL CDS PROCEDURE

PAGE 1 OF 2

001
(Entry Point A)

Install the write enable jumper.

3705-80 - Pin 01A-B1G2S02 to ground.

Set ENABLE/DISABLE switch(s) to DISABLE.

Set the DISPLAY/FUNCTION SELECT switch to the REGISTER ADDRESS position.

Set the STORAGE ADDRESS/REGISTER DATA switches (keys) to X'0DDDD'.

Press RESET. Press LOAD, and then press the panel INTERRUPT button.

The IPL sequence should be active at this point. During IPL Phase 3, ROS will read load program 1 from diskette and pass control to LPG1. LPG1 determines the type of load (NCP, with or without dump option, or diagnostics) being requested via either the CE panel or IPL register X'6B'. LPG1 attempts to read the appropriate program from diskette and pass control to it. If errors occur, while attempting to read either initial test or the IFT diskette loader from diskette or while the dump option is active, LPG1 will default to a LPG2 load.

Normal run time for a ROS/LPG1/initial test/IFT diskette loader is approximately 30 seconds.
Note: Under abnormal conditions, such as no index pulses or diskette media in the disk drive, ROS attempts to retry. This may cause a 3-minute delay before an error stop occurs.

DISPLAY REGISTER A = X'ECXX'?
Y N

002
See CDS Writer Symptom Index (this section).

A

A MAP 0005-1

003
The CDS Writer is the active program.
DISPLAY REGISTER B = X'3001'?
Y N

004
The first function of the CDS writer program is to test the write capability of the remote loader adapter. A test pattern is written onto track X'0F' and then read back to verify the write. The code X'3001' in DISPLAY B indicates that the write test was good. The CDS Writer is waiting a command.
See CDS Writer Symptom Index (this section).

005
Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 2.
Set the STORAGE ADDRESS/REGISTER DATA switches to X'0003'.
Press START.

(Entry Point B)

DISPLAY REGISTER B = X'3031'?
Y N

006
See CDS Writer Symptom Index (this section).

007
The Program Zapper is active.

Set the STORAGE ADDRESS/REGISTER DATA switches to X'00C07'.

Set the DISPLAY/FUNCTION SELECT switch to position 2.
Press start.
DISPLAY REGISTER B = X'3034'?
Y N

008
See CDS Writer Symptom Index in this section.

2
B

MAP 0005-1

B
1

REMOTE IPL CDS PROCEDURE

MAP 0005-2

PAGE 2 OF 2

009
The program LPG1 has been read into storage.
See Table 2 of LPG2 Symptom Index and Remote IPL CDS for definition and storage MAP of the 'Remote IPL CDS' (this section). Remote IPL CDS information can be added or changed by altering storage.
When ready to write the given program back onto diskette, set the STORAGE ADDRESS/REGISTER DATA switches to X'0EEEE'.
Press START.
DISPLAY REGISTER B = X'303F'?
Y N

010
See CDS Writer Symptom Index (this section).

011
Indicates that the given program has been written onto diskette without errors.
ANY MORE PROGRAM ZAP'S TO BE APPLIED?
Y N

012
Remove the write enable jumper.
Re-IPL.

013
Press START.
Go to Page 1, Step 005, Entry Point B.

REMOTE LOADER ROS INDEX

PAGE 1 OF 4

001
(Entry Point A)

C.E. aids

Use the following to get to the correct procedure or documentation:
DESCRIPTION?
Y N

002
SUPPORTING DOCUMENTATION?
Y N

003
CONTROL PANEL SETUP?
Y N

004
ERROR HANDLING PROCEDURES?
Y N

005
LOOP ON REMOTE LOADER ADAPTER TEST?
Y N

4 4 4 3 3 3
A B C D E F

F

006
CONTINUOUS READ OF LOAD PROGRAM 1 FROM TRACK ZERO?
Y N

007
CONTINUOUS READ OF LOAD PROGRAM 1 FROM ALTERNATE TRACK?
Y N

008
CONTINUOUS READ OF ANY GIVEN TRACK, EXCEPT X'06', X'09' OR X'0C'?
Y N

009
DETERMINE THE VERSION LEVEL OF PROGRAMS ON ANY GIVEN TRACK?
Y N

010
CONTINUOUS READ OF EITHER TRACK X'06', X'09' OR TRACK X'0C'?
Y N

011
There are no more CE Aids listed in this MAP.

012
CONTINUOUS READ OF EITHER TRACK X'06' OR X'0C'.

A. The above listed tracks contain programs which would normally be loaded into storage starting at location X'0000' and would destroy the ROS code. In order to allow a continuous read, the load point will be modified to start at X'1000'.

B. Refer to the ROS program listing. Set up for a load address compare stop at location X'03EC'. Press LOAD and wait for address compare stop.

C. Store a load halfword instruction X'2101' (Step 012 continues)

3 2 2 2
G H J K

K
1

PAGE 2 OF 4

(Step 012 continued)
into storage location X'036E'.

D. Store address X'1000' into storage location X'0600'.

E. Store a branch instruction X'A809' into storage location X'03F2'.

F. Store a NOP instruction X'A800' into storage locations X'03DA' and X'03F0'.

G. Store the desired track number X'0000' - X'004C' (with the above exceptions) into storage location X'0616'.

H. Set up for a load address compare stop at location X'03D6'. This will cause an address compare stop if any errors occur. --FOR CONTINUOUS LOOP--bypass this step.

I. Press START. Program should continuously read given track.

013
DETERMINE THE VERSION/LEVEL OF PROGRAMS ON ANY GIVEN DISKETTE.

A. Refer to the ROS program listing. Set up for a load address compare stop at location X'03EC'. Press LOAD and wait for address compare stop.

B. Store the desired track number (X'0000' - X'004C') into storage location X'0616'.

C. Store a branch instruction X'885B' into storage location X'03B6'. This patch will terminate the read after the track record block is read from diskette.

D. Set up for a load address compare stop at location X'0368'. Press START. When address compare stop occurs, display storage location X'066E'. It will contain the version/level in EBCDIC. e.g., V/L=01 would equal X'F0F1'. In addition the program ZAP count can be determined by displaying the storage location X'0676'.

Note: If the given track did not have a valid V/L at creation time, the V/L will equal X'FFF1'.

H J
1 1

014
CONTINUOUS READ OF ANY TRACK EXCEPT X'06' OR X'0C'.

A. Refer to the ROS loader program listing. Set up for a load address compare stop at location X'03EC'. Press LOAD and wait for the address compare stop.

B. Store a branch instruction X'A809' into storage location X'03F2'.

C. Store a NOP instruction X'A800' into storage locations X'03DA' and X'03F0'.

D. Store the desired track number X'0000' - X'004C' (with the above exceptions) into storage location X'0616'.

E. Set up for a load address compare stop at location X'03D6'. This will cause an address compare stop if any errors occur. --FOR CONTINUOUS LOOP--bypass this step.

F. Press START. Program should continuously read given track.

015
(Entry Point BC)
CONTINUOUS READ OF LOAD PROGRAM 1 FROM ALTERNATE TRACKS

A. Refer to the ROS program listing. If the ROS code is not already loaded in storage, setup for a load address compare stop at location X'01DE' and press LOAD. If ROS is already in storage, set the L1 IAR to X'01DE'.

B. Store a NOP instruction X'A800' into storage location X'03F2'.

C. Store a clear REG instruction X'11C8' into storage location X'03E8'. This will set the track seek number to zero on alternate passes.

D. Store a branch instruction X'A813' into storage location X'03F8'.

(Step 015 continues)

G 1 **REMOTE LOADER ROS INDEX**

PAGE 3 OF 4

(Step 015 continued)

E. Set up for a load address compare stop at location X'03D6'. This will cause an address compare stop if any errors occur.

F. Press START. Program should continuously read load program 1 from first track zero and then track 11. Refer to the ROS flowchart on previous pages.

016

CONTINUOUS READ OF LOAD PROGRAM 1 FROM TRACK ZERO.

A. Refer to the ROS program listing. If the ROS code is not already loaded in storage, setup for a load address compare stop at location X'01DE' and press LOAD. If ROS is already in storage, set the L1 IAR to X'01DE'.

B. Store a branch instruction (X'A809') into storage location X'03F2'.

C. Store a NOP instruction (X'A800') into storage location X'03DA'.

D. Store a NOP instruction (X'A800') into storage location X'03F0'.

E. Setup for a load address compare stop at location X'03D6'. This will cause an address compare stop if any errors occur. --FOR CONTINUOUS LOOP--bypass this step.

F. PRESS START. Program should continuously read LOAD PROGRAM 1 from track zero. If the program stops, refer to the ROS MAPS on other pages.

D 1 E 1 MAP 0006-3

017

LOOP ON REMOTE PROGRAM LOADER TEST.

A. Refer to the ROS loader program listing. If the ROS code is already loaded in storage, setup for a load address compare stop at location X'00EC' and press LOAD. If ROS is already in storage, set the L1 IAR to X'00EC'.

B. Store a (IN R4,IAR) instruction X'041C' into storage location X'01E2'.

Special Note: Assuming that all the adapter tests run without error, the above patch will allow the ROS code to move the head out to track 77 and then loop back to run the adapter test again.

C. Store a clear register instruction X'66C8' into storage location X'01EE'.

D. Store a branch instruction X'A8ED'into storage location X'01F0'.

E. Setup for an address compare stop at location X'03D6'. This will cause an address compare stop if any errors occur.

F. Press START. Program should loop without stopping, unless errors occur. If program stops, refer to the ROS flowcharts on other pages.

018

ERROR HANDLING PROCEDURES

1. If an error is detected during the instruction testing or the Remote Loader adapter initialization code, a hardstop will be invoked via an output X'70'.

2. If an error is detected during the Remote Loader Adapter test, a branch to 'Retry' will occur. If the retry count is not exhausted, a branch to 'IGAR141' will invoke a retry.

3. If an error is detected while attempting to read LPG1 from the diskette and the retry count is not exhausted, the track assignment will be changed and a read retry will occur.

(Step 018 continues)

A 1 B 1 C 1 **REMOTE LOADER ROS INDEX**

PAGE 4 OF 4

(Step 018 continued)

4. The initial retry count is 18. If the total number of retries of B and/or C exceeds 18, a hardstop will be invoked via an output X'70'. Reg 4 (X'04') and reg 6 (X'06') are used to help trace progress thru ROS.

019

CONTROL PANEL SETUP

1. During a normal IPL, the control panel MODE SELECT switch and the DIAGNOSTIC CONTROL switch must both be set to PROCESS.

020

SUPPORTING DOCUMENTATION

1. PROGRAM LISTING -A listing of the ROS code is in the ALD's beginning on page GE800 (3705-80).

2. FLOW CHART - A general flowchart, showing the logical flow of the ROS Remote Loader adapter testing and read functions is in the beginning of the ALDs on page GE860 (3705-80).

3. SIMULATION RUN - A ROS simulation run is in the ALD's on page GE860 (3705-80). The simulation run is a listing, in instruction execution order, showing the contents of the general registers used during the instruction test portion of the ROS. This simulation run may be used in conjunction with instruction step procedures as a check for correct operation.

021

DESCRIPTION

The ROS code is a 1024 byte program that is used to read LPG1 from the Remote Loader Diskette. Before the ROS program attempts to read LPG1, it checks the functions and instructions it needs to complete the read.

The functions tested are:

1. INSTRUCTIONS - Only the portion of the instruction set needed to complete the read of LPG1 from diskette is tested. The instructions tested are:

(Step 021 continues)

(Step 021 continued)

ARI	ST*	* = used but not thoroughly tested
LRI	BB	
ORI	BCL	
THM	BZL	
LH	B	
STH	XR	

IN* X'68, 69, 6A, 76, 79, 7C, 7D, 7E' and the Level 1 Local store Reg X'00-07'

OUT* X'68, 69, 6A, 77' and the level 1 Local Store Regs X'00-07'

2. Data Path

3. The SDLC CRC hardware assist register X'7C'.

4. Remote Loader adapter functions tested are:

   A. PDR register
   B. Adapter reset
   C. Diskette speed
   D. Head access and motor protect
   E. Head Engage/Disengage & Media Protection.

5. Read Data - The actual Read testing is accomplished while reading LPG1 from Diskette.

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ENTRY POINTS

FROM	ENTER THIS MAP		
MAP NUMBER	ENTRY POINT	PAGE NUMBER	STEP NUMBER
No entries in this table			

EXIT POINTS

EXIT THIS MAP		TO	
PAGE NUMBER	STEP NUMBER	MAP NUMBER	ENTRY POINT
3	012	0008	BA

001
(Entry Point A)

ROS ERROR ANALYSIS
The ROS code presents error indications by hardstopping via output X'70'. Observe the value of TAR (SAR) displayed on the control panel and follow the indicated procedures following:

TAR (SAR) = X'0002'?
Y N

002
TAR (SAR) = X'0032'?
Y N

003
TAR (SAR) = X'0034'?
Y N

004
TAR (SAR) = X'00BE'?
Y N

005
TAR (SAR) = X'00E8'?
Y N

6A 5B 5C 4D 4E 2F

F1

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006
TAR (SAR) = X'00F6'?
Y N

007
TAR (SAR) = X'0106'?
Y N

008
TAR (SAR) = X'0400'?
Y N

009
IPL PHASE 3 ACTIVE?
Y N

010
IPL Controls not working; refer to the ROS section in MLM Volume 2.

011
A ROS Program Load or Execution failure probably occurred.
Refer to the following:

ROS DATA TRANSFER TEST.

Display Main Storage Address

1. Location X'0010'
   All bits should be off in byte 0 in DISPLAY B. Suspect any bit that is on in byte 0 as being continuously on from storage. The bit can also be on continuously from ROS.

2. Location X'0032'
   All bits should be off in byte 1 in DISPLAY B. Suspect any bit that is on in byte 1 as being continuously on from storage. The bit can also be on continuously from ROS.

3. Location X'0056'
   All bits should be on in DISPLAY B. Suspect any bit that is not on as being continuously off from storage. The bit can also be off continuously from ROS.

(Step 011 continues)

3G 3H 3J

(Step 011 continued)

ROS ADDRESS GENERATION TEST

Display main storage addresses.
X'0000' should contain X'7004'.

IF LOCATION (X) 0000 CONTAINS	SUSPECT SAR BIT	SEE ALD 3705-80
(X) F6FF	15 ON	MM206-207
98B8	14 ON	MM206-207
810B	13 ON	MM206-207
0082	12 ON	MM206-207
0492	11 ON	MM206-207
F1FF	10 ON	MM206-207
1305	9 ON	MM206-207
65C8	8 ON	MM206-207
3587	7 ON	MM206-207

These charts are valid only for intermittent errors. ROS must load into storage correctly at least one time correctly out of a number of LOAD pushbutton operations for these charts to be valid. Otherwise use manual store and display procedures.
Location X'03FE' should contain X'7004'.

IF LOCATION X'03FE' CONTAINS	SUSPECT SAR BIT	See ALD 3705-80
(X) A815	15 OFF	MM206-207
810B	14 OFF	MM206-207
8802	13 OFF	MM206-207
A8D7	12 OFF	MM206-207
014C	11 OFF	MM206-207
2795	10 OFF	MM206-207
A823	9 OFF	MM206-207
9704	8 OFF	MM206-207
8491	7 OFF	MM206-207

NOTE: Only SAR bits 7 through 15 are used to address low
(Step 011 continues)

G H J
2 2 2

ERROR ANALYSIS PROCEDURES

MAP 0007-3

PAGE 3 OF 6

(Step 011 continued)
storage.

If no discrepancy has been found in the ROS data transfer test or the address generation test, verify that the control panel is set up properly and retry the IPL.

012
Remote Loader Adapter error, or diskette error or diskette media error.
A possible error would be CCU oscillator running at wrong speed. Verify input X'79' 0.5 for correct oscillator.
Go To Map 0008, Entry Point BA.

013
Reg X'06' used as a CE trace register, cannot be zeroed out.

Determine why reg X'06' cannot be cleared.

To set up a scoping loop, refer to the ROS listing.

1. Set the Level 1 IAR to X'00FC'.
2. Store a X'55C8'into location X'00FC'. This will clear reg X'05'.
3. Store a branch instruction X'A80B' into location X'0104'.
4. Press START.

014
Reg X'02' which is used as a base register, cannot be set to X'0600'.

Determine why reg X'02' cannot be set to X'0600'.

To set up a scoping loop, refer to the ROS listing.

1. Set the L1 IAR to X'00EA'.
2. Store a X'55C8'into location X'00EA'. This will clear reg X'05'.
3. Store a branch instruction X'A80D' into location X'00F4'.
4. Press START.

D E
1 1

ERROR ANALYSIS PROCEDURES

MAP 0007-4

PAGE 4 OF 6

015
An IPL sequence has been invoked, but the IPL bit 0.2 of input Reg X'79', is not ON.

016
A branch on bit instruction or BZL instruction has failed.

Setup for a load address compare stop at the starting address of the branch on bit test (X'00A4').

Re-IPL

When the load address compare stop occurs, store a branch instruction X'A81B' into location X'00BC'. This will set up a scoping loop.

Using the ROS listing, simulation run, the instruction step procedure and the following table, determine the failing instruction (bit).

Register 1 contains the instruction and indicates what is being tested. Bit 0.7 (ON) indicates that byte 1 is being tested, and bit 0.7 (OFF) indicates that byte 0 is being tested. Bits 0.2, 0.3, and 1.0 are a binary indication of the bit that is being tested within the byte. The bits are being tested for (solid) ON and OFF conditions.			
REGISTER 1		BITS BEING TESTED	
BYTE 0 01234567	BYTE 1 01234567	BYTE 0 01234567	BYTE 1 01234567
XX00XXX0	0XXXXXXX	10000000	00000000
XX00XXX0	1XXXXXXX	01000000	00000000
XX01XXX0	0XXXXXXX	00100000	00000000
XX01XXX0	1XXXXXXX	00010000	00000000
XX10XXX0	0XXXXXXX	00001000	00000000
XX10XXX0	1XXXXXXX	00000100	00000000
XX11XXX0	0XXXXXXX	00000010	00000000
XX11XXX0	1XXXXXXX	00000001	00000000
XX00XXX1	0XXXXXXX	00000000	10000000
XX00XXX1	1XXXXXXX	00000000	01000000
XX01XXX1	0XXXXXXX	00000000	00100000

(Step 016 continues)

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(Step 016 continued)

XX01XXX1	1XXXXXXX	00000000	00010000
XX10XXX1	0XXXXXXX	00000000	00001000
XX10XXX1	1XXXXXXX	00000000	00000100
XX11XXX1	0XXXXXXX	00000000	00000010
XX11XXX1	1XXXXXXX	00000000	00000001

To loop, set the MODE SELECT switch to PROCESS, ensure that the above mentioned branch instruction has been stored and then press START.

017
Output instruction X'70' hardstop failed.
Disregard the CCU check, Invalid OP lights. Determine why output X'70' failed to stop the machine.

018
An instruction failure or data flow failure.
Using the following table, use the load address compare procedure to determine the failing routine.
If the same hardstop is encountered prior to reaching the listed program stop, change the address of the next table entry and re-IPL.

SUGGESTED PGM STOP	SUSPECTED FAILURE	STARTING ADDRESS OF ROUTINE	BRANCH INST FOR LOOPING
(X) 00A4	STH,ST,LH,XR	(X) 007C	(X) A848
(X) 007C	XR,IN,OUT,LH	(X) 0062	(X) A82E
(X) 0062	DATA FLOW ORI,ARI,TRM BCL,BZL	(X) 0034	(X) A800
(X) 0034	BRANCH	(X) 002E	(X) A807

When the load address compare occurs, refer to the table to determine the starting address of the failing routine.

Store a NOP instruction X'A800' into location X'0030' . Refer to the table and store the appropriate branch instruction into location X'0032'.

Using the ROS listing, simulation run and the instruction
(Step 018 continues)

PAGE 6 OF 6

(Step 018 continued)
step procedure, determine the exact failing instruction.

To loop the failing routine, set the MODE SELECT switch to PROCESS, ensure that the above mentioned branch instruction has been stored and then press START.

019
An invalid branch to zero has occurred. Refer to the following to determine if ROS was loaded correctly.

ROS DATA TRANSFER TEST.

Display Main Storage Address

1. Location X'0010'
   All bits should be off in byte 0 in DISPLAY B. Suspect any bit that is on in byte 0 as being continuously on from storage. The bit can also be on continuously from ROS.

2. Location X'0032'
   All bits should be off in byte 1 in DISPLAY B. Suspect any bit that is on in byte 1 as being continuously on from storage. The bit can also be on continuously from ROS.

1. Location X'0056'
   All bits should be on in DISPLAY B. Suspect any bit that is not on as being continuously off from storage. The bit can also be off continuously from ROS.

Using the ROS listing and the Load Address Compare procedure, stop at various points in the program to determine what instruction is branching to zero.

This page intentionally left blank

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ENTRY POINTS

FROM	ENTER THIS MAP		
MAP NUMBER	ENTRY POINT	PAGE NUMBER	STEP NUMBER
No entries in this table			

EXIT POINTS

EXIT THIS MAP		TO	
PAGE NUMBER	STEP NUMBER	MAP NUMBER	ENTRY POINT
10	075	0006	BC

001
(Entry Point A)

LPG1 SYMPTOM INDEX
DISPLAY REG B = X'C006'?
Y N

002
DISPLAY REG B = X'C007'?
Y N

003
DISPLAY REG B = X'C009'?
Y N

004
DISPLAY REG B = X'C047'?
Y N

005
DISPLAY REG B = X'C048'?
Y N

1 1 1 1 1 1
1 1 1 1 1 2
A B C D E F

F
1

PAGE 2 OF 11

006
DISPLAY REG B = X'C0CE'?
Y N

007
DISPLAY REG B = X'C0FA'?
Y N

008
No other register display should occur.
Refer to MLM Volume 2 and verify the panel display register.
RE-IPL

009
X'C0FA' has occured. Track ID or CRC errors are occurring while trying to read LPG2 from diskette. If the retry is exhausted prior to obtaining a good load, LPG1 will initiate an automatic re-IPL.

010
X'C0CE' indicates that an adapter hardware type of error has occured.
(Entry Point UU)
(Entry Point RR)

REG X'06' = X'0234'?
Y N

011
REG X'06' = X'0276'?
Y N

012
REG X'06' = X'0288'?
Y N

013
REG X'06' = X'03B4'?
Y N

014
REG X'06' = X'030C'?
Y N

1 1 1 1 1
1 1 0 0 0
G H J K L M

M

015
(Entry Point HH)

SUSPECTED CARDS FOR THIS CHART ARE:	
3705-80	FUNCTION
01A-B1U2 ALD GE20X	VFO/DATA SEPERATORS
01A-B1F2 ALD GE30X	LEVEL 3 STATUS, ACCESS DRIVE AND CLOCK
01A-B1E2 ALD GE40X	FILE SERDES, SYNC DECODE, & PDR REGISTER.
01A-B1G2 ALD GE50X	DISKETTE CONTROLS, PULSE GATING, & TIMINGS.

Note: The errors on this chart are in the READ subroutine.
REG X'06' = X'0352'?
Y N

016
REG X'06' = X'035E'?
Y N

017
REG X'06' = X'037E'?
Y N

018
Display storage location X'062E' (program flag).
DOES IT CONTAIN X'F088'?
Y N

019
IS THE CONTROL PANEL 'CC CHECK' LIGHT ON?
Y N

9 8 8 8 3 3
N P Q R S T

S T
2 2

LPG1 SYMPTOM INDEX

PAGE 3 OF 11

020
This should not occur. Use the ROS listing to determine the problem.

021
Use the ROS listing to determine if the trouble is a failing instruction or input/output error.
IS THE TROUBLE AN INPUT/OUTPUT ERROR?
Y N

022
Use the ROS listing to determine the failing instruction.

023
(Entry Point BA)
Input/output error.

The Remote Loader adapter Input/Output Register decodes (X'68,69,6A') are contained on the following cards.
3705-80
01A-B1D2 ALD GE101

REG X'04' = X'0000'?
Y N

024
REG X'04' = X'0108'?
Y N

025
REG X'04' = X'0142'?
Y N

026
REG X'04' = X'0164'?
Y N

027
REG X'04' = X'017A'?
Y N

8 8 7 7 5
U V W X Y Z

Z

MAP 0008-3

028
REG X'04' = X'01A0'?
Y N

029
REG X'04' = X'01c0'?
Y N

030
REG X'04' = X'01E4'?
Y N

031
No other error should occur. Use the ROS listing to determine the problem.

032
An error occurred while moving the head out to track 77.
This error should occur only if CE aid number 1 is active. (continuous loop set up by CE)
Go to Page 2, Step 010, Entry Point RR.

033
REG X'06' = X'0000'?
Y N

034
Head engage, head disengage or media protect error.
REG X'07' = X'01CA'?
Y N

035
REG X'07' = X'01CE'?
Y N

036
REG X'07' = X'01D4'?
Y N

5 5 5 4 4 4
A A A A A A
A B C D E F

A A
E F
3 3

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037
REG X'07' = X'01DC'?
Y N

038
Should not occur. Use ROS listing to determine problem.

039
An adapter L3 interrupt did occur, but the media protect bit failed to set.

Reg X'05' contains the adapter level status, input X'69'. Media protect bit 1.0.

SUSPECTED CARD
3705-80
01A-B1F2 ALD GE302

Go to Step 040, Entry Point SS.

040
Media protection failed to occur. The head is engaged and ROS goes into a 10 sec. wait. However, media protect should occur on the third revolution after the head is engaged.

SUSPECTED CARD
3705-80
01A-B1G2 ALD GE505

(Entry Point SS)
To set up a scoping loop, refer to the ROS listing:

1. Set the L1 IAR to X'01C0'.

2. Store a branch instruction X'A817' into storage location
(Step 040 continues)

A
D
3

MAP 0008-4

(Step 040 continued)
X'01D4'.

3. Store a (LRI R3H,X'6F') instruction X'826F' into storage location X'02BC'. This will provide a 510-600 ms timeout loop in lieu of the standard 10 sec.

4. Press START.

041
Head engage latch failed to set.

SUSPECTED CARDS	
3705-80	FUNCTION
01A-B1G2 ALD GE503	DISKETTE CONTROLS
01A-B1F2 ALD GE303	DIAGNOSTIC STATUS LATCHES

To set up a scoping loop, refer to the ROS listing:

1. Set the L1 IAR to X'01C0'.

2. Store a branch instruction X'A811' into storage location X'01CE'.

3. Press START.

042
An unexpected interrupt occured when an output to engage the head was issued.
Reg X'05' contains the adapter level 3 status (input X'69'). Refer to ALD GE30X for 3705-80.
To set up a scoping loop, refer to the ROS listing:

1. Set the L1 IAR to X'01C0'.
2. Store a branch instruction X'A80C' into storage location X'01CA'.
3. Store a branch instruction X'A81F' into storage location X'01DC'.
4. Press START.

043
A subroutine error occurred while testing the head controls and media protect circuitry.
Go to Page 2, Step 010, Entry Point RR.

044
REG X'06' = X'0000'?
Y N

045
A subroutine error occurred while testing the access controls.
Note: This is the first pass thru the following ROS TAR(SAR) stops:
REG X'06' = X'0234'
REG X'06' = X'0276'
REG X'06' = X'0288'
REG X'06' = X'02B4'
Go to Page 2, Step 010, Entry Point RR.

046
Motor protection failed to occur. The adapter is issued a head move command. ROS waits for a motor protect interrupt (input X'69' 1.0). A 10-second timeout will occur if motor protect fails.

SUSPECTED CARDS	
3705-80	FUNCTION
01A-B1G2 ALD GE505	MOTOR PROTECT
01A-B1F2 ALD GE303	LEVEL 3 STATUS REG

To set up a scoping loop, refer to the ROS listing:

1. Set the L1 IAR to X'01A6'.
2. Store a branch instruction X'A819' into storage location X'01BC'.
3. Press START.

047
Verify diskette speed. The expected diskette speed of 166.6 milliseconds per revolution is tested for a +10 percent tolerence. The test method used is to get in-sync with the diskette index and time the elapse period to the next index. Refer to the chart below for this next section of the MAP.

SUSPECTED CARDS FOR THIS CHART ARE	
3705-80	FUNCTION
01A-B1F2 ALD GE302	STATUS & INTERRUPT CONTROLS
01A-B1E2	BASIC

(Step 047 continues)

(Step 047 continued)

ALD GE402	TIMINGS
01A-B1G2 ALD GE501	DISKETTE CONTROLS

REG X'07' = X'0182'?
Y N

048
REG X'07' = X'0188'?
Y N

049
REG X'07' = X'0190'?
Y N

050
REG X'07' = X'019C'?
Y N

051
Should not occur. Use ROS listing to determine problem.

052
The allow interrupt on index latch failed to reset output. X'68' with 1.0 on should reset the above mentioned latch. Refer to the following chart.

SUSPECTED CARDS FOR THIS CHART ARE	
3705-80	FUNCTION
01A-B1F2 ALD GE302	STATUS & INTERRUPT CONTROLS

053
Either the diskette speed is too fast or extra index pulses are occurring.
Go to Step 054, Entry Point B.

054
Diskette speed too slow or interrupt on index did not occur on the next revolution.
(Entry Point B)
To verify the diskette speed for 3705-80 refer to ALD GE502. Scope (+) index. It should occur every 166 MS +5, -5 percent. If it does not, refer to RPL Section of FETMM.
For scoping, refer to the following:

TO SCOPE FOR MISSING PULSES:

1. For 3705-80, refer to ALD GE030. Scope (+) index.
2. Set the scope on a slow sweep range and display three (+) index pulses. If the middle pulse is not a solid pulse, refer to RPL Section of FETMM.

TO SCOPE FOR EXTRA INDEXES:

1. For 3705-80, refer to ALD GE502. Scope (+) index.
2. Expand the scope sweep to provide a full screen index pulse (2 to 3 ms). If the (+) index pulse breaks up, it will generate extra index pulses. Refer to RPL OP section of MLM Volume 3.
3. If the (+) index pulse does not break up, replace the suspect card. (see list below)

SUSPECTED CARDS FOR THIS CHART ARE	
3705-80	FUNCTION
01A-B1F2 ALD GE302	STATUS & INTERRUPT CONTROLS
01A-B1E2 ALD GE402	BASIC TIMINGS
01A-B1G2 ALD GE501	DISKETTE CONTROLS

X3 AH6

LPG1 SYMPTOM INDEX

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055
Failed to get an interrupt on index L3 status.

1. Check for diskette media in reader.

2. Check cable between remote cable loader adapter and the diskette.

Refer to the following chart for scoping:

To scope 3705-80, refer to ALD GE030. Scope the signal (+) index. If it does not occur, refer to RPL OP section of MLM Volume 3. If it does occur, refer to the ROS listing:

1. Set the L1 IAR to X'17A'.

2. Store a branch instruction X'A80B' into storage location X'182'.

3. Press START.

For 3705-80, refer to ALD GE030. Scope for the signal *-int on index*. If it does not occur, replace the diskette control card. If it does occur, continue to scope to determine the failing card.

056
Remote loader adapter reset test, an output X'68' with 1, 5 & 1.6 on is issued to reset the adapter. The two status registers (input X'68' and '69') are tested for all zeros.

There is no assurance that the adapter had any outstanding status prior to issuing the reset. As a result, status reset errors may occur at other points in ROS.

This routine is the first code to issue an output X'68', and the input X'69'. If the card in the following chart does not correct the error, verify the previous decodes.

The suspected card is as follows:

```
+--------------+
|SUSPECTED CARD|
+--------------+
|   3705-80    |
```

(Step 056 continues)

W3

MAP 0008-7

(Step 056 continued)

```
+--------------+
|   01A-B1F2   |
|   ALD GE30X  |
+--------------+
```

Display registers X'68' and '69' via the control panel to determine the 'HOT' status bits(s).
For scoping, refer to the following:

To set up a scoping loop, refer to the ROS listing:

1. Set the L1 IAR to X'0164'.

2. Store a branch instruction X'A80D' into storage location X'016E'.

3. Store a branch instruction X'A815' into storage location X'0176'.

4. Press START.

057
PDR register test (input/output X'6A') error. The remote loader PDR REG is tested to verify correct data transfer.
REG X'03' = X'0000'?
Y N

058
(Entry Point VV)
Refer to the following chart:

```
+----------------+
| SUSPECTED CARD |
+----------------+
|    3705-80     |
+----------------+
|    01A-B1E2    |
|    ALD GE40X   |
+----------------+
```

For scoping, use the following:

To set up a scoping loop, refer to the ROS listing:

1. Set the L1 IAR to X'0142'.

(Step 058 continues)

8AK

U3 V3 AK7

LPG1 SYMPTOM INDEX

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(Step 058 continued)
2. Store a branch instruction X'A809' into storage location X'0150'.

3. Press START.

This loop will start with the first test pattern and continue to update the test pattern until an error occurs. It will then branch back in a tight loop on the failing pattern.

059
The first suspected card failure is in the decode of in/out X'6A'.
Go to Page 7, Step 058, Entry Point VV.

060
CRC register test (input X'7C') error. The 8 bit DLC hardware assist register is tested to verify correct CRC calculation.
The suspected card is as follows:

```
+--------------+
|SUSPECTED CARD|
+--------------+
|   3705-80    |
+--------------+
|   01A-B3S2   |
|   ALD CR001  |
+--------------+
```

Refer to the following for scoping:

To set up a scoping loop, refer to the ROS listing:

1. Set the L1 IAR to X'0108'.

2. Store a branch instruction X'A815' into storage location X'011A'.

3. Press START.

061
Error occurred while attempting to read LPG1 from diskette.
Go to Page 2, Step 010, Entry Point UU.

P2 Q2 R2

MAP 0008-8

062
A CRC CHECK OCCURED.
Replace the diskette media, re-IPL. If the same error occurs, continue the following procedure.
Display storage location X'0654', (program flag).
DOES IT CONTAIN X'0000'?
Y N

063
The first 32 bytes of data (track header and its CRC) was read without error.
Go to Step 066, Entry Point QQ.

064
The CRC error occured on the track header block.
Go to Step 066, Entry Point QQ.

065
CHARACTER SERVICE FAILED TO OCCUR.
Go to Step 066, Entry Point QQ.

066
TRACK ID ERROR.
The track number read from the diskette did not match the expected value.
Reg X'03' = actual track number read from the diskette media. Reg X'05' = bits in error.
Replace the diskette media and re-IPL. If the same error re-occurs, continue with the following procedure.

(Entry Point QQ)

To set up a scoping loop, refer to the ROS listing:

1. For track ID errors, refer to chart 1 below. Set up for the 'continuous read of LPG1 from the alternate tracks'. Observe the diskette head movement. It should be alternating between track 0 and 11. If not, change the access drive and the diskette control cards. (refer to chart 2 below). If the same error reoccurs, refer to the RPL OP Section of MLM Volume 3.

2. For character service errors, refer to chart 3 below and set up for continuous read of LPG1 from track 0. Using chart 2 at the right, and the RPL OP section of MLM Volume 3 for appropriate timing charts, scope for failure.

(Step 066 continues)

(Step 066 continued)

CHART 1
CONTINUOUS READ OF LOAD PROGRAM 1 FROM ALTERNATE TRACKS

A. Refer to the ROS program listing. If the ROS code is not already loaded in storage, set up for a load address compare stop at location X'01DE' and press load. If ROS is already in storage, set the L1 IAR to X'01DE'.

B. Store a NOP instruction X'A800' into storage location X'03F2'.

C. Store a clear reg instruction X'01' into storage location X'03E8'. This will set the track seek number to zero on alternate passes.

D. Store a branch instruction X'A813' into storage location X'03FB'.

E. Set up for a load address compare stop at location X'03D6'. This will cause an address compare stop if any errors occur.

F. Press START. Program should continuously read load program 1 from first track zero and then track 11. Refer to the ROS flowchart on previous pages.

SUSPECTED CARDS FOR THIS CHART ARE	
3705-80	FUNCTION
01A-B1U2 ALD GE20X	VFO/DATA SEPERATORS
01A-B1F2 ALD GE30X	LEVEL 3 STATUS, ACCESS DRIVE AND CLOCK
01A-B1E2 ALD GE40X	FILE SERDES, SYNC DECODE, & PDR REGISTER.

(Step 066 continues)

N2

(Step 066 continued)

01A-B1G2 ALD GE50X	DISKETTE CONTROLS, PULSE GATING, & TIMINGS.

CONTINUOUS READ OF LOAD PROGRAM 1 FROM TRACK ZERO.

A. Refer to the ROS program listing. If the ROS code is not already loaded in storage, set up for a load address compare stop at location X'01DE' and press LOAD. If ROS is already in storage, set the L1 IAR to X'01DE'.

B. Store a branch instruction (X'A809') into storage location X'03F2'.

C. Store a NOP instruction (X'A800') into storage location X'03DA'.

D. Store a NOP instruction (X'A800') into storage location X'03F0'.

E. Set up for a load address compare stop at location X'03D6'. This will cause an address compare stop if any errors occur. --FOR CONTINUOUS LOOP--bypass this step.

F. PRESS START. Program should continuously read LOAD PROGRAM 1 from track zero. If the program stops, refer to the ROS MAPS on other pages.

067
The initial character service failed to occur during an attempt to read.
Replace the diskette media and re-IPL.
DOES THE SAME ERROR OCCUR?
Y N

068
(Entry Point TT)
IS THE DISKETTE PRESSURE PAD LOADING?
Y N

10ALN 10AMN

ALN9 AMN9 ANN9

069
IS THE DISKETTE HEAD MOVING?
Y N

070
Check the remote program loader adapter's 24VAC power supply and fuses.
IS IT OK?
Y N

071
Refer to PWR MAP section and trouble shoot the power supply.

072
Refer to the RPL OP Section of MLM Volume 3 and trouble shoot the pressure pad movement.

073
For 3705-80, refer to ALD GE502. Scope for '+ head engage'. If signal is present, refer to the RPL OP Section of MLM Volume 3, if signal '+ head engage' is not present. Replace the diskette control as indicated below:

SUSPECTED CARDS FOR THIS CHART ARE	
3705-80	FUNCTION
01A-B1G2 ALD GE50X	DISKETTE CONTROLS PULSE GATING & TIMING

074
Go to Page 8, Step 066, Entry Point QQ.

075
Go To Map 0006, Entry Point BC.

JK22L2

076
An adapter L1 interrupt has occurred. Use the control panel to display reg X'68', the adapter level 1 status register. Determine the type of error.

3705-80	FUNCTION
01A-B1E2 ALD GE403	OUTBUS PARITY
01A-B1G2 ALD GE501	WRITE CONTROLS
01A-B1F2 ALD GE301	LEVEL 1 STATUS REG

077
Failed to get an interrupt on index (input X'69' Bit 0.0).
Go to Page 11, Step 080, Entry Point II.

078
Table of possible gray codes
(input X'69' bits 0,2,3,4 and 5)

IF REVERSE MOVE	CURRENT GRAY COUNT	IF FORWARD MOVE
1001	1100	0110
1100	0110	0011
0110	0011	0110
0011	0110	1100

GRAY COUNTER ERROR OR ACCESS CONTROL ERROR.
Reg X'05' contains the bits-in-error(mask = X'3C00').
Reg X'03' contains the actual gray code (input X'69').

If 3705-80, the suspected card is 01A-B1F2 (ALD GE305).

(Step 078 continues)

G 2 H 2 **LPG1 SYMPTOM INDEX**

A 1 B 1 C 1 D 1 E 1 MAP 0008-11

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(Step 078 continued)
NOTE: To do a Manual Reset Test, use the control panel to:
1. Output X'68' with data X'0006'.
2. Input should equal X'3000'.

SPECIAL NOTE: There is NO positive feedback from the motor. As a result, this test does not prove that the head actually moved.

079
An unexpected interrupt occurred during a head move sequence. Reg X'05' contains the adapter level 3 status (input X'69').
Go to Step 080, Entry Point II.

080
X'0234' failed to get an interrupt on index (INPUT X'69' BIT 0.0).
(Entry Point II)
The suspected function failure is the STATUS AND INTERRUPT CONTROLS and the BASIC TIMINGS.

If 3705-80, the suspected cards are 01A-B1F2 (ALD GE302) for a failure of the STATUS and INTERRUPT CONTROLS and 01A-B1E2 (ALD GE40X) if BASIC TIMINGS.

CONTINUOUS READ OF LOAD PROGRAM 1 FROM Track zero.

A. Refer to the ROS program listing. If the ROS code is not already loaded in storage, set up for a load address compare stop at location X'01DE' and press LOAD. If ROS is already in storage, set the L1 IAR to X'01DE'.

B. Store a branch instruction (X'A809') into storage location X'03F2'.

C. Store a NOP instruction (X'A800') into storage location X'03DA'.

D. Store a NOP instruction (X'A800') into storage location X'03F0'.

E. Set up for a load address compare stop at location X'03D6'. This will cause an address compare stop if any errors occur. --FOR CONTINUOUS LOOP--bypass this

(Step 080 continues)

(Step 080 continued)
step.

F. PRESS START. Program should continuously read LOAD PROGRAM 1 from track zero. If the program stops, refer to the ROS MAPS on other pages.

081
X'C048' indicates that the IFT DISK LOADER cannot be read from diskette.
Go to Step 082, Entry Point GG.

082
X'C047' indicates that INITIAL TEST can not be read from the diskette.
(Entry Point GG)
Change the diskette media and RE-IPL.

083
Storage mechanism failure.

If 3705-80, the suspected card is 01A-B4D2 (ALD CVXXX).

084
Cold SAR bits(s) are causing addressing failures.
Reg X'05' contains the test address. Storage location X'3FE' has been disturbed by the address in Reg X'05'.
Note: To scope the loop,
set the DISPLAY/FUNCTION SELECT switch to FUNCTION 3.
Press START.

085
IPL register X'6B' failure.
Reg X'03' contains expected data and reg X'05' contains the bit in error.
If 3705-80, the suspected card is 01A-B1F2 (ALD GE305)
Note: To scope the loop,
set the DISPLAY/FUNCTION SELECT switch to FUNCTION 3.
Press START.

LPG1 FLOWCHART

PAGE 1 OF 2

001
(Entry Point A)

LPG1 FLOWCHART

LPG1 is passed control at storage location X'0080'.

Set DISPLAY A = X'CCTT' and DISPLAY B X'0000'.

Test for intermittent errors that may have occurred in ROS. If any errors did occur, set the appropriate bit in the OBR record.

Complete the ORB record. Save the CE trace registers X'04' and X'05' used in ROS.

Determine what type of load is to follow diagnostic or LPG2.

Based on the type of load and storage size, set the appropriate flags and initial test. Flag location X'0414'.

Test IPL reg '6B'.

Test for cold SAR bits 0.0, 1, 2, 3, and 4.

DID THE HOST REQUEST A STORAGE DUMP?
Y N

002
DID THE OPERATOR REQUEST A STORAGE DUMP?
Y N

003
Move the 32 bytes of L0 general regs data or BTU data from X'079F' to location X'0040' - X'005F'.

Perform a READ. Read initial test from diskette.

WAS READ SUCCESSFUL?
Y N

2 2 2
A B C D

D MAP 0009-1

004
DID DIAGNOSTICS LOAD?
Y N

005
(Entry Point AB)
DID NCP/R REQUEST IPL?
Y N

006
DID OPERATOR/C.E. REQUEST A DIAGNOSTICS LOAD?
Y N

007
(Entry Point ZZ)
Restore the 32 bytes of L0 general regs data or BTU data back to X'0780' - '079F' from the temporary save area X'0040' - '005F'.

(Entry Point WW)
Perform a READ. Read LPG2 from track X'06'.

WAS READ SUCCESSFUL?
Y N

008
Perform a READ. Read LPG2 from track X'0C'.

WAS READ SUCCESSFUL?
Y N

2 2 2 2 2 2
E F G H J K

MAP 0009-1

E F G H J K
1 1 1 1 1 1

LPG1 FLOWCHART

PAGE 2 OF 2

009
RETRY EXHAUSTED?
Y N

010
Go to Page 1, Step 007, Entry Point WW.

011
Automatic RE-IPL

012
Go to Step 013, Entry Point XX.

013
(Entry Point XX)
Reset 'Test Mode' and 'IPL Phase 3' Mode.

Pass control to LPG2 at location L-8K where L=Last Valid Machine address.
See LPG2 Symptom Index and Remote IPLCDS.

014
Operator panel data switches = X'0DDDD' and panel level 3 interrupt active (input X'7F' bit 0.6).

Perform a READ. Read the 'IFT Disk Loader' from diskette.

WAS READ SUCCESSFUL?
Y N

015
Report an error via the panel and hardstop.

016
Pass control to the 'IFT Disk Loader' at location X'3C04'. Refer to the 'IFT Disk Loader'.

017
IPL reg X'6B' byte 0, bits 0, 1 or 3 equals a logical one.
Go to Page 1, Step 007, Entry Point ZZ.

018
Report an error via the operator panel and hardstop.

A B C
1 1 1

MAP 0009-2

019
Reset 'IPL phase 3' Mode.
Pass control to initial test at location X'0800'.
Assuming no error stops, initial test will re-enter LPG1 without manual intervention required.
Go to Page 1, Step 005, Entry Point AB.

020
Operator panel data switches = X'0BBBB'.
Go to Step 021, Entry Point YY.

021
IFT reg X'6B' bit 0.0 equals a logical one.

(Entry Point YY)
Perform a READ. Read the 'Dump Subroutine' from track X'11'.
WAS READ SUCCESSFUL?
Y N

022
Go to Step 024, Entry Point AC.

023
Perform a DUMP. Save the upper 8K of storage by writing it into tracks X'0F' and X'10'.
DUMP OK?
Y N

024
(Entry Point AC)
Set flag to indicate that the DUMP data is BAD.
Go to Page 1, Step 007, Entry Point WW.

025
Fetch and save the storage protect keys for the upper 8K. Store at location X'0180'.
Go to Page 1, Step 007, Entry Point WW.

MAP 0009-2

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Load Program 2 (LPG2) Symptom Index and Remote IPL CDS

LPG2 consists of an SDLC handler, an NCP loader, and a dump handler. The SDLC handler controls the SDLC trunk or trunks and is shared by the other two routines. The NCP loader controls the loading of the NCP-R from the host to the remote. The dump handler controls the transfer of storage and the contents of tracks X'0F' and X'10' to the host.

When LPG2 is given control, a basic validity check is performed on the "remote IPL CDS" data. Based on the "remote IPL CDS" data, LPG2 monitors a given SDLC trunk or trunks for control information from the host. The host retains control over the type of request (for example load or dump) and must inform the remote (LPG2) of the action to be taken. The "dump required" bit being ON only indicates that the upper 8K of storage contents have been saved when the IPL sequence was initiated. A continuous re-IPL occurs if "data set ready" is not active for any of the defined lines.

Remote LPG 2 (X3705NEA) supports the SDLC test command and up to X'10' bytes of data.

Remote IPL CDS Format

In order to establish contact with the host, LPG2 must know which SDLC trunk or trunks to use and the type of communication scanner installed in the remote loader machine. Because this information is subject to changes, a 64 byte area is reserved in LPG1 and is defined as the "remote IPL CDS" Refer to the following tables for bit definition of the CDS field. See MAP 5 "remote IPL CDS procedure" (in this section) for the procedure to modify the CDS.

The host link may be assigned to any line pair, but line pair 1 is recommended.

Obtain the following information from the host site prior to writing the remote RPL CDS:

1. Upper scan limit
2. Scanner substitution control bits
3. Number of minutes wait time during dump or load
4. SDLC host link poll character
5. NRZI transmission method
6. Host link leased or switched line
7. If switched line, manual or auto answer
8. Modem or internal clock
9. Data rate select if two speed modem
10. Oscillator select bits

Error Reporting

If LPG2 incurs an unrecoverable error, it posts an error code in DISPLAY B and hard stops via an output X'70' instruction. The following list can be used to help determine the error:

DISPLAY B	Description of Error
30F0	No active SDLC trunks
30F1	No scanner
30F2	CDS invalid

LPG2 hard stops with no error code posted if L1 checks occur due to program error. STATUS position of DISPLAY/FUNCTION SELECT switch shows the reason. L1 1 reg 1 (X'01') contains the combined input X'76' and X'7E'. L4 IAR (IN X'10') contains the saved L2 IAR. L3 IAR is intact.

Abend

LPG2 encounters some conditions which cause the LPG2 to re-IPL itself. After re-IPLing, FUNCTION 1 of the DISPLAY/FUNCTION SELECT switch will display the abend (re-IPL) code if applicable. Re-IPL during an abend will be prevented by FUNCTION 6 being set prior to abend. DISPLAY B would then contain the abend code.

LPG2 Codes	Description of Condition
3F01	No trunks up - either enable failed or transmit initial failed
3F02	SDRM received while monitoring one line
3F03	SNRM received while monitoring one line
3F04	Automatic re-IPL due to user specified time interval expiration
3F05	L1 CSB interrupt
3F06	Incorrect LPG2 active for 3705 MOD I (should not get this message on 3705-80)
3F10	SIM received while loading or dumping

Byte and Bit Definitions for the Remote IPL CDS

Scanner and Line Pair 1 CDS

STORAGE LOCATION	*Byte.Bit*	*Description*
X'0040'	0.0-3	= 0000
	0.4-1.7	= Transmit leg address for line pair 1 (see Note 1)
X'0042'	0.0-3	= 0000
	0.4-1.7	= Receive leg address for line pair 1 (see Note 1)
X'0044'	0.3	= 1 (Communication scanner type 2)
	0.7	= 1 (The IPL trunks are attached to scanner 1)
	1.0-7	= SDLC address for line pair 1 (see Note 7)
X'0046'	0.0	= 0 if line pair 1 does not require NRZI transmission method (see Note 5)
	0.1	= 0 if line pair 1 is to be monitored (see Note 2)
		= 1 if line pair 1 is inactive
	0.2	= 0 (Reserved)
	0.3	= 0 if line defined is leased
		= 1 if line defined is switched (see Note 4)
	0.4	= 0 if switched line is manual answer
		= 1 if switched line uses 'ring indicator' auto answer mode
	0.5	= 0 (Reserved)
	0.6-1.7	= Line definition for line pair (needed at set mode time for output X'46') for type 2 scanner (see Note 6)

Scanner and Line Pair 2 CDS

STORAGE LOCATION	*Byte.Bit*	*Description*
X'0048'	0.0-3	= 0000
	0.4-1.7	= Transmit leg address for line pair 2 (see Note 1)
X'004A'	0.0-3	= 0000
	0.4-1.7	= Receive leg address for line pair 2 (see Note 1)
X'004C'	0.6-.7	= Upper scan limit (refer to CS2 section in Volume 3)
	1.0-7	= SDLC address for line pair 2 (see Note 7)
X'004E'	0.0	= 0 if line pair 2 does not require NRZI transmission method (see Note 5)
	0.1	= 0 if line pair 2 is to be monitored (see Note 2)
		= 1 if line pair 2 is inactive
	0.2	= 0 (Reserved)
	0.3	= 0 if line defined is leased
		= 1 if line defined is switched (see Note 4)
	0.4	= 0 if switched line is manual answer
		= 1 if switched line uses 'ring indicator' auto answer mode
	0.5	= 0 (Reserved)
	0.6-1.7	= Line definition for line pair (needed at set mode time for output X'46') for type 2 scanner (see Note 6)

Scanner and Line Pair 3 CDS

STORAGE LOCATION	*Byte.Bit*	*Description*
X'0050'	0.0-3	= 0000
	0.4-1.7	= Transmit leg address for line pair 3 (see Note 1)
X'0052'	0.0-3	= 0000
	0.4-1.7	= Receive leg address for line pair 3 (see Note 1)
X'0054'	0.0-3	= Scanner substitution control 1 bits 1-4 respectively (refer to CS2 section in Volume 3)
	0.4-7	= 0000 for unlimited wait time during load or dump process = number of minutes of inactivity (timeout) during load or dump before an automatic re-IPL occurs (see Note 4)
	1.0-7	= SDLC address for line pair 3 (see Note 7)
X'0056'	0.0	= 0 if line pair 3 does not require NRZI transmission method (see Note 5)
	0.1	= 0 if line pair 3 is to be monitored (see Note 2) = 1 if line pair 3 is inactive
	0.2	= 0 (Reserved)
	0.3	= 0 if line defined is leased = 1 if line defined is switched (see Note 4)
	0.4	= 0 if switched line is manual answer = 1 if switched line uses 'ring indicator' auto answer mode
	0.5	= 0 (Reserved)
	0.6-1.7	= Line definition for line pair (needed at set mode time for output X'46') for type 2 scanner (see Note 6)

Line Pair 4 CDS

STORAGE LOCATION	*Byte.Bit*	*Description*
X'0058'	0.0-3	= 0000
	0.4-1.7	= Transmit leg address for line pair 4 (see Note 1)
X'005A'	0.0-3	= 0000
	0.4-1.7	= Receive leg address for line pair 4 (see Note 1)
X'005C'	1.0-7	= SDLC address for line pair 4 (see Note 7)
X'005E'	0.0	= 0 if line pair 4 does not require NRZI transmission method (see Note 5)
	0.1	= 0 if line pair 4 is to be monitored (see Note 2) = 1 if line pair 4 is inactive
	0.2	= 0 (Reserved)
	0.3	= 0 if line defined is leased = 1 if line defined is switched (see Note 4)
	0.4	= 0 if switched line is manual answer = 1 if switched line uses 'ring indicator' auto answer mode
	0.5	= 0 (Reserved)
	0.6-1.7	= Line definition for line pair (needed at set mode time for output X'46') for type 2 scanner (see Note 6)

Line Pair 5 CDS

STORAGE LOCATION	*Byte.Bit*	*Description*
X'0060'	0.0-3	= 0000
	0.4-1.7	= Transmit leg address for line pair 5 (see Note 1)
X'0062'	0.0-3	= 0000
	0.4-1.7	= Receive leg address for line pair 5 (see Note 1)
X'0064'	1.0-7	= SDLC address for line pair 5 (see Note 7)
X'0066'	0.0	= 0 if line pair 5 does not require NRZI transmission method (see Note 5)
	0.1	= 0 if line pair 5 is to be monitored (see Note 2) = 1 if line pair 5 is inactive
	0.2	= 0 (Reserved)
	0.3	= 0 if line defined is leased = 1 if line defined is switched (see Note 4)
	0.4	= 0 if switched line is manual answer = 1 if switched line uses 'ring indicator' auto answer mode
	0.5	= 0 (Reserved)
	0.6-1.7	= Line definition for line pair (needed at set mode time for output X'46') for type 2 scanner (see Note 6)

Line Pair 6 CDS

STORAGE LOCATION	*Byte.Bit*	*Description*
X'0068'	0.0-3	= 0000
	0.4-1.7	= Transmit leg address for line pair 6 (see Note 1)
X'006A'	0.0-3	= 0000
	0.4-1.7	= Receive leg address for line pair 6 (see Note 1)
X'006C'	1.0-7	= SDLC address for line pair 6 (see Note 7)
X'006E'	0.0	= 0 if line pair 6 does not require NRZI transmission method (see Note 5)
	0.1	= 0 if line pair 6 is to be monitored (see Note 2)
		= 1 if line pair 6 is inactive
	0.2	= 0 (Reserved)
	0.3	= 0 if line defined is leased
		= 1 if line defined is switched (see Note 4)
	0.4	= 0 if switched line is manual answer
		= 1 if switched line uses 'ring indicator' auto answer mode
	0.5	= 0 (Reserved)
	0.6-1.7	= Line definition for line pair (needed at set mode time for output X'46') for type 2 scanner (see Note 6)

Line Pair 7 CDS

STORAGE LOCATION	*Byte.Bit*	*Description*
X'0070'	0.0-3	= 0000
	0.4-1.7	= Transmit leg address for line pair 7 (see Note 1)
X'0072'	0.0-3	= 0000
	0.4-1.7	= Receive leg address for line pair 7 (see Note 1)
X'0074'	1.0-7	= SDLC address for line pair 7 (see Note 7)
X'0076'	0.0	= 0 if line pair 7 does not require NRZI transmission method (see Note 5)
	0.1	= 0 if line pair 7 is to be monitored (see Note 2)
		= 1 if line pair 7 is inactive
	0.2	= 0 (Reserved)
	0.3	= 0 if line defined is leased
		= 1 if line defined is switched (see Note 4)
	0.4	= 0 if switched line is manual answer
		= 1 if switched line uses 'ring indicator' auto answer mode
	0.5	= 0 (Reserved)
	0.6-1.7	= Line definition for line pair (needed at set mode time for output X'46') for type 2 scanner (see Note 6)

Line Pair 8 CDS

STORAGE LOCATION	*Byte.Bit*	*Description*
X'0078'	0.0-3	= 0000
	0.4-1.7	= Transmit leg address for line pair 8 (see Note 1)
X'007A'	0.0-3	= 0000
	0.4-1.7	= Receive leg address for line pair 8 (see Note 1)
X'007C'	1.0-7	= SDLC address for line pair 8 (see Note 7)
X'007D'	0.0	= 0 if line pair 8 does not require NRZI transmission method (see Note 5)
	0.1	= 0 if line pair 8 is to be monitored (see Note 2)
		= 1 if line pair 8 is inactive
	0.2	= 0 (Reserved)
	0.3	= 0 if line defined is leased
		= 1 if line defined is switched (see Note 4)
	0.4	= 0 if switched line is manual answer
		= 1 if switched line uses 'ring indicator' auto answer mode
	0.5	= 0 (Reserved)
	0.6-1.7	= Line definition for line pair (needed at set mode time for output X'46') for type 2 scanner (see Note 6)

Notes:

1. Trunk address(es) - The transmit and receive leg addresses must be the "character control block" (CCB) for a type-2 scanner. Refer to LIB section in Volume 2. If the trunk is a half duplex line, the transmit and receive lines must contain identical addresses.
2. If a given line pair is not used or defined, the appropriate bit must be set on to suppress using it.
3. When it is possible to load/dump over multiple line pairs, LPG2 locks onto a line when an SDLC SIM command is received. This time limit allows LPG2 to re-IPL itself if the trunk "goes down" during the load/dump process. The re-IPL will allow LPG2 to scan all lines (SDLC trunks) again. Insert hex values X'1' to X'F' for 1 to 15 minutes timeout.
4. Switched line support requires a type 2 scanner and the line must be half duplex. No check is made that scanner and mode are correct. Unpredictable results may occur if defined incorrectly.
5. NRZI mode of operation is required if business machine clock is in use.
6. Set mode values.

Byte *Bit*	Type 2 CSB *Output X'46'*	
0.6	0	
0.7	0	
1.0	0	
1.1	Diagnostic wrap mode.	This bit should normally be 0.
1.2	Data terminal ready.	This bit should normally be 1.
1.3	Synchronous bit clock.	This bit should normally be 1 with internal clock.
1.4	Modem provided clock.	This bit should normally be 1 if modem clock is to be used.
1.5	Data rate select.	If 1 on modems with two speeds this will select the highest of the two available speeds.
1.6	Oscillator select.	These two oscillator select bits, in combination, are used to select internal oscillator (business machine clock) to be used.
1.7	Oscillator select.	

7. This is a software address (poll character) defined by the Host NCP with the ADDR operand on the INNODE macro.

CONTROL PANEL DISPLAY TECHNIQUES

LPG2 uses the following method to display status and to report on the progress of the load/dump portion of the IPL sequence of a remote 3705.

The display is controlled by the DISPLAY/FUNCTION SELECT switch and it is updated every 100 milliseconds. Console switches are read only at the time the INTERRUPT pushbutton is pressed.

Contents of the display registers are as follows except when the DISPLAY/FUNCTION SELECT switch is in either the STATUS or TAR & OP REGISTER position.

Normal Display

Normal Display (when functions in B, C, and D (which follow) are not invoked):

DISPLAY REG A = FCss
DISPLAY REG B = last line with interrupt

where: FC = remote loader program present (LPG2)
ss = state of IPL sequence
- 80 = Monitor for IPL State
- 40 = Load State
- 20 = Dump State
- 10 = Entry Point Received (for Load)
- 08 = PIU received, not yet returned
- 04 = Reserved
- 02 = High 8K of storage from 33FD Disk in.
- 01 = Type 2 Scanner Indicator

Storage Address

Storage address displays the storage contents at the address defined by the STORAGE/ADDRESS/DATAn REGISTER switches.

DISPLAY REG A = storage address
DISPLAY REG B = contents at that storage address

Register Address

Register address displays the contents of general program registers 00 through 1F and external/hardware registers 40 through 7F.

STORAGE ADDRESS/DATA switches = xrxrx
DISPLAY REG A = 0r0r0
DISPLAY REG B = register rr contents

Note: For the following displays, it is assumed you are familiar with: 1) SDLC line control and 2) NCP 3.0.

FUNCTION 1: Displays reason for IPL, CDS line(s) being scanned

DISPLAY REG A = REG '6B' first 4 Bits, 8 bits of 0, 4 bits for 1st, 2nd, 3rd, and/or 4th CDS line set being used
DISPLAY REG B = NCP Abend Code if NCP invoked IPL, LPG2 abend code if LPG2 re-IPLed itself (see ABEND later in this section).

FUNCTION 2: ICW display. The interface address or the line address is specified by the C, D, and E switches. Only lines defined in the CDS can be displayed.

DISPLAY REG A = SCF,PDF
DISPLAY REG B = LCD/PCF, data set leads

FUNCTION 3: The current position in storage pointer when load/dump in progress and the last request code received (from PIU) is displayed along with the state of the IPL sequence.

DISPLAY REG A = Last request code received; state of IPL sequence (see normal display above)
DISPLAY REG B = Storage Pointer

FUNCTION 4: Displays latest SDLC address and control fields. The interface address or the line address is specified by the C, D, and E panel switches (keys). Only those lines defined in the "remote IPL CDS" can be displayed.

DISPLAY REG A = Receive SDLC station address and control field
DISPLAY REG B = Transmit SDLC station address and control field

FUNCTION 5: Display latest PIU received. Low order switches (D and E) are used for displacement into PIU displayed. Zeros in B & C switches indicate work/transmit PIU. Non-zeros indicate receive PIU.

DISPLAY REG A = X'00' or X'FF' followed by displacement.
DISPLAY REG B = PIU contents at that displacement.

FUNCTION 6: Displays zeros for 100 ms, then resets to normal display. If LPG2 detects position 6 while abending, it hard stops instead of re-IPLing.

Note: Zeros are displayed if invalid addresses are set in switches.

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3705-80 Configuration Data Set Writer

The configuration data set (CDS) writer verifies the write circuitry of the Remote Loader Adapter, allows the operator or CE to modify either the 'Remote IPL CDS' or the hardware CDS, and allows the CE to apply program fixes to the various programs.

ERROR HANDLING

The CDS writer uses the following displays for communication with the operator or CE.

DISPLAY A = ECtt where EC defines the CDS writer and tt defines the track number that the head is currently over or tried to read.

DISPLAY B = 30xx - for information displays or software errors
= C0Fx - indicates a write/read subroutine error
= C0xx - indicates a hardware error

The CDS writer does not use a retry procedure; all errors are posted immediately.

Error and information displays are shown on pages RPL 255 and 260.

DISPLAY A	DISPLAY B	Explanation
ECtt	3001	The CDS writer is awaiting a command to (1) modify the remote IPL CDS, (2) modify the hardware CDS, or (3) modify a program on the disk media. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 2, set the STORAGE ADDRESS/REGISTER DATA switches to X'0002' to modify hardware CDS, or X'0003' to modify remote IPL CDS or to modify a program (remote IPL CDS is contained in LPG1, Z3705MGA). Press the START pushbutton.
ECtt	3002	The DISPLAY/FUNCTION SELECT switch was not in FUNCTION 2 position when the command was issued. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 2 and press START.
ECtt	3005	After modifying the CDS or program, the STORAGE ADDRESS/REGISTER DATA switches should have been set to X'EEEE'. Set the switches properly and press START.
ECtt	3024	The hardware CDS is loaded into storage and ready for modification. Refer to the hardware CDS description to configure the CDS properly. It is possible to transfer the CDS from one disk media to another by bringing the media with the CDS to this point and changing disk media.
ECtt	3026	The track header has been modified. Press START to return to stop code X'3001' or re-IPL.
ECtt	302F	The hardware CDS has been successfully written onto the disk. Press START to return to stop code X'3001' if additional commands are required.
ECtt	3031	The program is awaiting the ID of the program to be modified. Enter the program ID.
ECtt	3032	The requested program could not be found on the disk media. Press START to return to the stop code X'3031'.
ECtt	3034	The requested program has been read into storage for modifying. Apply the zap as per instructions. When the zap is applied, set the STORAGE ADDRESS/REGISTER DATA switches to X'EEEE' and press START.
ECtt	3036	Priviledged areas of storage have been modified. Press START to return to stop X'3031' for restart.
ECtt	303F	The requested program has been successfully written onto the disk media. Press START to return to stop code X'3031'.

DISPLAY A	DISPLAY B	Explanation
ECtt	C021	Either no interrupt on index occurred or an unexpected interrupt occurred. X'05' contains the L3 status obtained via input X'69', (bit 0.0) (see Note 1). Card location is 01A-B1G2. Refer to FEALD page GE50x.
ECtt	C022	An unexpected interrupt occurred during a head move sequence. X'05' contains the L3 status obtained via an input X'69' (see Note 1).
ECtt	C023	Either an access control or a gray counter error occurred. X'05' contains the bits in error masked by X'3C00'. X'03' contains the actual gray code obtained via input X'69'. A table of possible gray code values is located in the IPL procedure MAP (see Note 1). Card location is 01A-B1F2. Refer to FEALD Page GE30x.
ECtt	C024	An interrupt on index failed to occur within the alloted time. The time alloted for a 3705-80 is 177.5 ms (see Note 1).
ECtt	C026	An L1 interrupt occurred from the remote adapter. X'05' contains the L1 status obtained via input X'68' (see Note 1). Card location is 01A-B1E2. Rerer to FEALD page GE403.
ECtt	C03B	The head failed to engage. X'05' contains the L3 status obtained via input X'69' (see Note 1). Card location is 01A-B1G2. Refer to FEALD page GE503.
ECtt	C081	The initial character service interrupt on a read operation failed to occur. Change the disk media and re-IPL (see Note 1 and Note 2).
ECtt	C082	An access error occurred; the track ID did not match the expected ID (see Note 1 and Note 2).
ECtt	C083	A character service interrupt after the first one failed to occur on read operation. This is probably a remote adapter timing error (see Note 1 and Note 2).
ECtt	C084	A CRC error occurred on one of the track records. Change the disk media and re-IPL (see Note 1 and Note 2).
ECtt	C0F1	The head failed to engage during a write operation. Register X'05' contains the level 3 status obtained via an input X'69' (see Note 1)
ECtt	C0F2	An unexpected L3 interrupt occurred on a write operation. X'05' containes the level 3 status obtained via input X'69'. Reg X'05' bits are defined as: bit 1.0 (motor/media error), bit 1.4 (overflow), bit 0.0 (index), and bit 0.7 (character service) (see Note 1).

DISPLAY A	DISPLAY B	Explanation
ECtt	C0F3	An overrun error occurred during a write operation. X'05' containes the L3 status obtained via an input X'69' (see Note 1).
ECtt	C0F4	A motor/media error occurred during a write operation. X'05' contains the L3 status obtained via input X'69' (see Note 1).
ECtt	C0F6	Head engage failed to set during a read operation that was to verify the previous write operation. X'05' contains the level 3 status obtained via input X'69' (see Note 3).
ECtt	C0F7	An unexpected L3 interrupt occurred during a read operation that was to verify the previous write operation. X'05' contains the L3 status obtained via input X'69' (see Note 3).
ECtt	C0F8	An overrun error occurred during a read operation that was to verify the previous write operation. X'03' contains the L3 status obtained via input X'69' (see Note 3).
ECtt	C0FA	Write/Read error(s) occurred. It is assumed that cause of this read error is that the write operation failed. Reg X'06' contains the number of errors that occurred. Reg X'05' contains an address pointer to the expected data for the first error. To determine the actual data read back from disk, add X'1500' to the address pointer contained in Reg X'05'. Reg X'04' contains the starting address of the write buffer. The difference between Reg X'04' and Reg X'05' will indicate at what point of the track record the first error occurred (see Note 3). Refer to (1) FEALD page GE30X, card location 01A-B1F2, (2) FEALD page GE50X, and (3) FEALD page GE20X.

Note 1: To set up a scoping loop, set the control panel FUNCTION SELECT SWITCH to FUNCTION 3. Press START. The program will continue to loop as long as FUNCTION 3 is active. See Note 2 for an additional scoping procedure.

Note 2: Display storage location X'1302' to determine the track number on which the read failure is occurring. Using this track number, refer to MAP 8 and the ROS program listing to set up a scoping loop.

Note 3: To set up a scoping loop, set the control panel FUNCTION switch to FUNCTION 4. Press START. The program will continue to loop (write/verify) as long as FUNCTION 4 is active. All errors that refer to this Note are assumed to be caused by failures in the write circuitry.

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3705-80 IFT Diskette Loader Description

The IFT Diskette Loader (Z3705NCA 3705-80) resides on a 33FD diskette media with the Internal Functional Tests (IFTs). The loader provides an interface between the Diagnostic Control Monitor (DCM) and the Remote Loader Adapter.

Load Program 1 (LPGM1) controls loading of the IFT Diskette Loader. The IFT Diskette Loader is loaded into the 3705 storage after Initial Test (INIT) has been executed if a diagnostic load is requested.

A diagnostic load is requested by setting the DISPLAY/FUNCTION SELECT switch to the STORAGE ADDRESS position, setting STORAGE ADDRESS/REGISTER DATA switches B through E to X'DDDD', and pressing LOAD and INTERRUPT. The IFTs load from the diskette media and execute exactly the same as if loaded via the channel adapter. Loading the Panel Line Test requires that STORAGE ADDRESS/REGISTER DATA switches B through E be set to X'AADD'.

The IFT Diskette Loader executes in program level 1 and is located in storage at addresses X'3C00' - X'3FFF'. In addition to the IFT Diskette Loader, a linkage handler and program ID/track number table (track allocation table) is loaded at location X'1100'. A control table is loaded at X'1300'.

Error Handling

The IFT Diskette Loader reports errors with the following displays.

DISPLAY A = DCtt
where:
DC indicates the IFT Loader and tt is the current track ID

DISPLAY B = 30xx or C0xx
where:
30xx indicates a program error stop code or information display

C0xx indicates a hardware error stop code

The IFT Diskette Loader improves the availability of a given IFT with a retry procedure. The retry count is set to 4 each time a track read begins. If a X'C0xx' error occurs, the loader resets the Remote Loader Adapter and attempts to read the diskette again. When the retry count is exhausted, the loader posts an error code and hard stops.

Error and information displays are shown on the following page (RPL DIAG 310).

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DISPLAY A	DISPLAY B	Explanation
DCtt	3031	The IFT Diskette Loader could not find the DCMs ID (X''0003'') in the diskette track table which starts at location X''1200''. The diskette track table may have been changed; change diskette media and re-IPL.
DCtt	3032	An invalid program ID was requested. Display register X''05'' to determine what program was requested. Refer to the table below to determine the program ID. The most likely cause for this error is an invalid adapter defined in the hardware CDS. After verifying the CDS, press START to return to the DCM; the DCM should post an additional error. Z 3 7 0 5 n n A A Translates to 00 — A Translates to 01 B Translates to 01 — B Translates to 02 C Translates to 02 — C Translates to 03 D Translates to 03 — D Translates to 04 E Translates to 04 — E Translates to 05 F Translates to 05 — F Translates to 06 G Translates to 06 — G Translates to 07 H Translates to 07 — H Translates to 08 I Translates to 08 — I Translates to 09 J Translates to 09 — J Translates to 0A K Translates to 0A — K Translates to 0B L Translates to 0B — L Translates to 0C M Translates to 0C — M Translates to 0D N Translates t0 0D — N Translates to 0E O Translates to 0E — O Translates to 0F P Translates to 0F
DCtt	3039	The DCM requested test termination. Press START to restart the DCM or re-IPL.
DCtt	303F	This is an information type stop to indicate that intermittent errors occurred in either ROS and/or LPGM1. Display storage location X''1330'' to determine the number of errors that occurred. The starting count was X''EFFF'', byte 0 is the complement of 18 decimal. For each error, byte 0 will be one greater; X''F3FF'' represents five errors. Storage locations X''063C'' and X''063E'' represent the CE trace reg X''04'' and X''06'' respectively. These locations will be X''0000'' if no error occurred in ROS. Refer to the IPL procedure MAPs and use the trace data to determine the type of error. If reg X''06'' is not X''0000'', the last error occurred in LPGM1. Refer to the IPL procedure MAPs and use the trace data to determine the type of error. Storage location X''062F'' will be X''0000'' if intermittent track ID errors occurred, X''062F'' will be X''F0B8'' if intermittent CRC errors occurred.

DISPLAY A	DISPLAY B	Explanation
DCtt	C021	Either no interrupt on index or an unexpected interrupt occurred. Reg X''05'' contains the L3 status obtained via input X''69'' (see Note 1). Card location is 01A-B1G2. Refer to FEALD page GE50X.
DCtt	C022	An unexpected interrupt occurred during the head move sequence. Reg X''05'' contains the L3 status obtained via input X''69'' (see Note 1).
DCtt	C023	Either an access error or a gray counter error occurred. Reg X''05'' contains the bits in error masked by X''3C00''. Reg X''03'' contains the actual gray code obtained via X''69''. A table of possible gray counter codes is located in the IPL procedure MAPs (see Note 1). Card location is 01A-B1F2. Refer to FEALD page GE30X.
DCtt	C024	No interrupt on index signal occurred within the alloted time after a head access sequence. The alloted time is 172.9 ms on a 3705-80 (see Note 1).
DCtt	C026	A level 1 interrupt occurred from the remote adapter. Reg X''05'' contains the L1 status obtained via input X''68'' (see Note 1).
DCtt	C03B	The head engage bit failed to come on in register X''69''. Reg X''05'' contains the L3 status obtained via input X''69'' (see Note 1).
DCtt	C081	The initial character service interrupt failed to occur on a read operation. Change the diskette media and re-IPL. Storage location X''1302'' contains the track number of the failing track (see Note 1 and Note 2).
DCtt	C082	The track ID read from the track did not match the expected track ID. Storage location X''1302'' contains the track number of the failing track (see Note 1 and Note 2).
DCtt	C083	No character service interrupt occurred on a data byte after the first one. This is a probable remote adapter timing error. Storage location X''1302'' contains the track number of the failing track (see Note 1 and Note 2).
DCtt	C084	A CRC error occurred on one of the track records. Change the diskette media and re-IPL. Storage location X''1302'' contains the track number of the failing track (see Note 1 and Note 2).

Note 1: To set up a scoping loop, set the control panel DISPLAY/FUNCTION SELECT SWITCH to FUNCTION 3. Press start. The program will continue to loop as long as FUNCTION 3 is active. See Note 2 for an additional scoping procedure.

Note 2: Display storage location X'1302' to determine the track number on which the read failure is occuring. Using this track number, refer to MAP 8 (in this section) and the ROS program listing to set up a scoping loop.

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Channel Adapter Online Test (CA OLT)

WHAT CA OLT DOES

CA OLT attempts to identify card faults that have the following failure symptoms. All the cards listed below are on gate 01A, board position A4 or B1:

Failure Symptom	*Card*	*Location*
Command decode	2325	A4M2
Status	2325	A4M2
	2326	A4T2
	7602	A4L2
Sense	7601	A4P2
Residual byte count	7602	A4L2
Traps ESC address when ESC lines not enabled	2325	A4M2
	2326	A4T2
Widespread errors	2342	A4N2
Interface A	6836	A4Q2
Interface B	6836	A4S2
	6837	A4R2
Extended buffer*		
control circuits	AC05	**J2
data flow	AC06	**H2
Cycle Steal*		
control circuits	CE25	**E2
data flow	CE24	**D2

* type 4 CA only ** A4 or B1

Note: If the CUTEST questions receive a C (cancel) response just before the test is run, all test sections print out a diagnostic message indicating the section did not run.

REQUIREMENTS

You must have the proper configuration data set (CDS) cataloged with the remainder of the system. (For additional information, see the CDS section.) Note that T3705AE wraps the ESC address and terminates if the ESC address is missing in the test request message (DEV/TEST/OPT) or in the native subchannel (NSC) CDS.

HOW CA OLT IS STRUCTURED

The CA OLT consists of the following test sections:

T3705AA
T3705AB
T3705AC
T3705AD
T3705AE
T3705AF (type 4 CA only)
T3705AG (type 4 CA only)
T3705AH (type 4 CA only)
T3705AI (type 4 CA only)

T3705AA, T3705AB, and T3705AC CA OLT Description

Test sections T3705AA, T3705AB, and T3705AC primarily test the common controls and interface. The 3705-80 ROS bootstrap program responds to the functions of these three sections.

T3705AB, routines 3 and 4, test Halt I/O (HIO) and Test I/O (TIO) commands. These routines do not check the results of the tests if the CDS for the line being tested defines it as shared; Online Test Standalone Executive Program (OLTSEP) does not process the command requested if the line is shared.

T3705AD and T3705AE CA OLT Description

Test sections T3705AD and T3705AE issue I/O commands to the NSC and ESC addresses.

Before T3705AD or T3705AE is started, a responder program (U3705A), which responds to their commands, is loaded into the 3705-80. When the responder is successfully loaded in the 3705-80, the ROS bootstrap program turns control over to the responder program. Failure to load successfully results in an error printout similar to that resulting from errors in normal test functions.

T3705AF AND T3705AH DESCRIPTION

T3705AF and T3705AH are 3705 type 4 channel adapter test sections and will not run on a type 1 channel adapter.

T3705AF and T3705AH use responder modules U3705I and U3705J. U3705I is loaded into the 3705 with an IPL command. Chained to the IPL is a write command to load U3705J.

U3705I loads U3705J at X'800' in the 3705 storage and gives ending status to the I/O operation that loaded them; then transfers control to U3705J. U3705J sets various mode states according to the routine being run.

T3705AF and T3705AH each consist of eight routines. Each routine sends a 4 byte signal prior to a test. The signal identifies the routine and gives the responder a count with which to regulate the read byte count.

At the end of this test the routine requests and receives a count of the data written. An error message results if the count is wrong.

Routine 05 can be made to loop 256 times by entering EXT = L in the options field of the test request message to employ a longer wrap operation. The extra looping increases the run time for T3705AF or T3705AH from about 10-15 seconds to about 3 1/2 minutes.

T3705AG AND T3705AI DESCRIPTION

T3705AG and T3705AI are 3705 type 4 channel adapter test sections and will not run on a type 1 channel adapter.

T3705AG and T3705AI use responder modules, U3705I and U3705K. U3705I is loaded into the 3705 with an IPL command. Chained to the IPL is a write command to load U3705K.

U3705I loads U3705K at X'800' in the 3705 storage and gives ending status to the I/O operation that loaded them; then transfers control to U3705K. U3705K sets various mode states according to the routine being run.

T3705AG and T3705AI each consist of four routines. Each routine sends a 4 byte signal prior to a test. The signal identifies the routine and gives the responder a 3705 storage address where the test message is to be written and read. This section tests the type 4 channel adapter cycle steal mode.

At the end of these tests the routine requests and receives a count of the data written. An error message results if count is wrong.

IFT EXECUTION

3705 Setup Procedures

1. Switch the 3705 power on.
2. Set both the MODE SELECT and DIAGNOSTIC CONTROL switches to the PROCESS position.
3. Enable the appropriate channel interface.
4. To load the DCM, set the DISPLAY/FUNCTION SELECT switch to the STATUS position. For information on using the other positions, see "How to Use the DISPLAY/FUNCTION SELECT Switch" in the DCM section.
5. Press the RESET pushbutton and then the LOAD pushbutton.
6. DISPLAY B bits 0.2 and 0.3 should be on, indicating that ROS has reached IPL phase 3. The LOAD light should be on; the following lights should be off: HARD STOP, TEST, WAIT, and PROGRAM STOP.

If the above conditions are not present, refer to the CE panel test in the CTRL PNL section and the ROS test in the ROS section (Volume 2).

Host Procedures

Start the OLTEP or OLTSEP in the host processor. When OLTEP or OLTSEP causes a console printer message of:

r ID 'ENTER DEV/TEST/OPT/'

you enter:

r ID,'xxx,yyy/3705AA-AE/NFE/'

where:

xxx = the channel address of the 3705 (native subchannel address (NSC))
yyy = an emulation subchannel address (ESC)

The test request message for the CA OLT must include the 3705 native subchannel address followed by the emulation subchannel address.

T3705AA and T3705AE test the NSC and ESC addresses. If only the NSC address is entered in the device field of the test request message, T3705AA bypasses that part of the test using the second address (the last half of routines 1 and 2).

T3705AE looks for a second address in the test request message and for an emulation line definition in the NSC CDS. If either is missing, a message (NO ESC ADDRESS DEFINED IN NSC

CDS OR TEST REQUEST) is printed out and the test section is terminated.

For example, assume that you entered:

R 01,'005,020/3705AA-AE/NFE/'

When an emulation line address is entered in the device field of DEV/TEST/OPT/, DOS/OLTEP prints a DVC NOT OP message for that address. OLTEP performs a data protection function when the emulation line address is not available. Condition code 3 results and the printout occurs.

Routine 2 of T3705AC requires manual intervention. The option *MI* must be included in the test request message for this routine to be run.

If any of these OLT sections are run by reading them in from the card reader, U3705C must follow the first section called for in the test request message. Test sections T3705AD and T3705AE also require the 3705 responder program, U3705A, to follow each deck.

On termination, T3705AD and T3705AE issue an invalid channel Write IPL command (4 bytes of zeros) to leave the 3705 in a ROS-loaded state.

Routines 3 and 4 of T3705AB test the Halt I/O and Test I/O commands. These routines are run only under OLTSEP and are bypassed if the executive program is not OLTSEP. If these routines are requested and the executive is other than OLTSEP, the start and terminate messages appear but the routines are not run.

MESSAGES

Messages occur during operation of the CA OLT that indicate: (1) an error has been detected or (2) an action is needed to either cancel, proceed, or retry the requested CA OLT procedure. The messages, message explanations, and responses are as follows:

THE STATUS OF THE 3705 CANNOT BE DETERMINED. **WARNING** CONTINUATION WILL CAUSE THE ENTIRE 3705 TO BECOME UNAVAILABLE. ENTER 'C' TO CANCEL OR 'P' TO PROCEED.

Explanation: The OLT cannot determine the status (offline or stopped) of the 3705. If the OLT is allowed to continue, the program in 3705 storage will be destroyed.

Response: Continue by entering a C or P, as follows:

r id,'C' (for cancel)
or
r id,'P' (for proceed)

Any other response results in the program's repeating the last line of the above message. After five invalid responses, the message INVALID RESPONSE AFTER 5 REQUESTS is printed.

ALL 3705 ADDRESSES ARE NOT STOPPED OR OFFLINE. **WARNING** CONTINUATION WILL CAUSE THE ENTIRE 3705 TO BECOME UNAVAILABLE. ENTER 'C' TO CANCEL OR 'P' TO PROCEED, OR 'R' TO RETRY.

Explanation: The OLT has been notified by the executive driver that all 3705 addresses are not offline or stopped. If the OLT is allowed to continue, the program in 3705 storage will be destroyed.

Response: You have the opportunity to make all addresses available to the OLT using standard system facilities. Continue by entering a *C, P,* or *R,* as follows:

r id,'C' (for cancel)
or
r id,'P' (for proceed)
or
r id,'R' (for retry)

The P response means to proceed regardless of the offline or online status of the 3705 address; the R response means that the operator has been taking addresses offline and wants the program to verify that all units are now available to the OLT.

Any other response results in the program's repeating the last line of the above message. After five invalid responses, the message INVALID RESPONSE AFTER 5 REQUESTS is printed.

INVALID RESPONSE AFTER 5 REQUESTS

Explanation: The program assumed the response of C and terminated the OLT.

Response: None.

CA OLT ERROR INFORMATION

When the CA OLT detects an error (bad CSW, CC, sense, data, etc.), an error printout occurs at the host processor printer. All pertinent information about the error that can be obtained by the OLT appears in the printout.

If the error printout reports that no interrupt occurred from the 3705, see "Responder Error Displays" later in this section.

When an interface control check causes a machine check, OLTSEP enters its WAIT state with an error code displayed in the instruction counter of the host processor. The wait state error codes are defined in the *OLTSEP Operator's Guide,* D99-SEPDT. Such a machine check is catastrophic to OLTEP under OS or DOS. Running SEREP is the next logical step if such a failure occurs.

The message ID number for the failing section of the online test is printed in the first 3 digits of the test description (second line) of the DPRINT message. The test section numbers and the corresponding message ID numbers follow:

Test Section Number	*Message ID Number*
T3705AA	30-41
T3705AB	42-53
T3705AC	54-62
T3705AD	63-76
T3705AE	77-88
T3705AF*	1-19
T3705AG*	1-9 and 20-29
T3705AH*	1-19
T3705AI*	1-9 and 20-29

*type 4 CA only

For a description of the error printout format, refer to *DOS OLTEP SRL,* GC24-5086; *IBM System/360 Operating System On-Line Test Executive Program,* GC28-6650; and *OLTSEP Operator's Guide,* D99-SEPDT.

Responder Error Displays

The following is a description of the responder error codes. The DISPLAY/FUNCTION SELECT switch must not be in either the STATUS or the TAR & OP REGISTER positions. These error codes do not isolate errors but indicate that an error has occurred. The program sets one of the codes below in DISPLAY B and sets HARD STOP. To continue, press the START pushbutton. If the DISPLAY/FUNCTION SELECT switch is in FUNCTION 5, the program will not stop on type 1 CA level 1 interrupts.

U3705I Responder Display Codes (DISPLAY B)

CODE	*MEANING*
C200	Non CA L1 (CCU, CSB, etc.)
C202	CA2 selected for IPL, but L3 not set
C203	CA1 selected for IPL, but L3 not set
C204	Unexpected CA L1
C20A	Unknown L3 (not timer, PCI, panel or CAS)
C20E	Unknown CA L3 interrupt
C210	Inbound transfer when not expected
C211	Inbound transfer with count of zero
C212	Unexpected command received
C2FF	Normal display code

U3705J and U3705K Responder Display Codes (DISPLAY B)

CODE	*MEANING*
C200	Non channel adapter L1 (CCU, CSB, etc.)
C202	CA2 selected for IPL, but L3 not set
C203	CA1 selected for IPL, but L3 not set
C204	Unexpected CA L1
C20A	Unknown L3 (Not timer, PCI, panel or CAS)
C20C	Branch to zero detected
C20E	Unknown CA L3 interrupt
C210	Inbound transfer when not expected
C211	Inbound transfer with count of zero
C212	Unexpected command received
C2FF	Normal display code.

Test Section Description

Test Section T3705AA

Routine 01: Checks No-op command.

(Issues a No-op command to the NSC address.)

01001 Expected results:

Condition code	01
First CSW status	0C00
Expected sense	00

(Issues a No-op command to the ESC address.)

01002 Expected results:

Condition code	03

Routine 02: Checks Write IPL command.

(Issues a Write IPL command with an invalid byte count of 1 to the NSC address.)

02001 Expected results:

Condition code	00
Ending status	0F00
Expected sense	02

(Issues a Write IPL command with an invalid byte count of 1 to the ESC address, which has not been enabled.)

02002 Expected results:

Condition code	03

Routine 03: Checks illegal commands.

(Issues all illegal commands to the NSC address on consecutive passes.)

03001 Expected results:

Condition code	00
Ending status	0E00
Expected sense	82

Routine 04: Checks Write command.

(Issues the Write command to the NSC address, which has not been initialized.)

04001 Expected results:

Condition code	00
Ending status	0E00
Expected sense	02

Test Section T3705AB

Routine 01: Checks Read command.

(Issues the Read command to the NSC address, which has not been initialized.)

01001 Expected results:

Condition code	00
Ending status	0E00
Expected sense	02

Routine 02: Checks Write Break command.

(Issues the Write Break command to the NSC address, which has not been initialized.)

02001 Expected results:

Condition code	00
Ending status	0E00
Expected sense	02

Routine 03: Checks Halt I/O operation. This routine runs under OLTSEP only.

(Issues a Halt I/O command.)

03001 Expected results:

Condition code	01
Initial status	0000
Expected sense	00

Routine 04: Checks the resulting status of Test I/O command. This routine runs under OLTSEP only.

(Issues a Test I/O command.)

04001 Expected results:

Condition code	00
First CSW status	0000
Expected sense	00

Test Section T3705AC

Routine 01: Checks the transfer of data using Write IPL command.

(Writes 18 bytes of data with the Write IPL command.)

The ending status presented because of an invalid Write IPL command is channel end, device end, unit check, and unit exception. This status is presented by ROS. The second 2 bytes of data transferred do not contain a count of 18.

01001 Expected results:

Condition code	00
First CSW status	0F00
Expected sense	02

Routine 02: Tests the ROS-generated asynchronous status.

(Sets attention equals YES, and issues a No-op command.)

This is a manual intervention routine. The manual intervention option must be specified in the request for test, or this routine is bypassed. A message to the operator requests 'PRESS THE LOAD PUSHBUTTON ON THE 3705 CONTROL PANEL'.

If the LOAD pushbutton is not pressed within 60 seconds after the operator message, a time-out results. An error message presents the first CSW status as shown below, but the ending or second CSW status is zeros:

02001 Expected results:

Condition code	01
First CSW status	0C00
Ending status	0600
Expected sense	00

Test Section T3705AD

T3705AD requires the responder program U3705A (see "T3705AD and T3705 AE CA OLT Description" earlier in this section). All commands in T3705AD are issued to the NSC address.

Routine 01: Checks data transfer with the Write command.

(Writes 4 bytes of data.)

01001 Expected results:

Condition code	00
First CSW status	0800
Second CSW status	0400
Expected sense	00

Routine 02: Checks data wrap with the Write and Read commands.

(Writes and reads 4 bytes of data. Data read is compared for accuracy.)

02001 Expected results:

Condition Code	00
Initial status	0800
Ending status	0400
Expected sense	00

02002 Expected results:

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

Routine 03: Checks 1-byte data wrap.

(Writes 1 byte of data.)

03001 Expected results:

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

(Issues a Read command with a byte count of 4. Data is compared to verify 1 byte read.)

03002 Expected results:

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

Routine 04: Checks 3-byte wrap.

(Writes 3 bytes of data.)

04001 Expected results:

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

(Issues a Read command with a byte count of 4. Data is compared to verify bytes read.)

04002 Expected results:

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

Routine 05: Checks data wrap with the Write and Read commands using command chaining.

(Issues a Write command of 4 bytes chained to a Read command of 4 bytes.)

05001 Expected results:

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

A failure in this routine and not in other routines might be due to chaining failure; suspect card 2342 at A4N2.

Routine 06: Checks NSC status byte.

(Issues a Write Break command with a byte count of 4.)

The status presented here is not a valid presentation of status, but a test of the ability to set status bits.

06001 Expected results:

Condition code	00
First status	CC00
Second status	0000
Expected sense	00

Routine 07: Checks for status modifier, control unit end, and busy.

(Issues a No-op command.)

The responder sets up to present the initial and ending status as indicated below. As in the previous routine, this is a test for the ability to set status bits.

07001 Expected results:

Condition code	01
Initial status	7000
Ending status	8400
Residual Count	00
Expected sense	00

Test Section T3705AE

T3705AE requires the responder program U3705A (see "see T3705AD and T3705AE CA OLT Description" earlier in this section).

Routine 01: Checks that a No-op command causes channel and device end.

(Issues a No-op command to the NSC address.)

01002 Expected results:

Condition code	01
First CSW status	0C00

(Issues a No-op command to the ESC address.)

01003 Expected results:

Condition code	01
First CSW status	0C00

Routine 02: Checks data wrap with the Read and Wrap commands.

(Issues a Read command to the NSC address [18 bytes]. Issues a Wrap command to the ESC address [18 bytes].)

02001 Expected results (NSC address):

Condition code	00
First CSW status	0800
Second CSW status	0400
Expected sense	00

02001 Expected results (ESC address):

Condition code	00
First CSW status	0C00
Expected sense	00

CANCEL/PROCEED messages for each pass

Test Section T3705AF

Routine 01: Checks Normal Mode Wrap Test

This routine writes a 16 byte message on the first test address and reads the message back on the second address. The wrap is made in normal mode (not extended buffer mode) and inbound data/status interrupts occur each time a 4 byte buffer is filled.

01002 *Expected results from the Write*

Condition code	00
First CSW status	0800
Second CSW status	0400
Expected sense	00

01002 *Expected results from the Read*

Condition code	00
First CSW status	00C0
Second CSW status	0000
Expected Sense	00

Routine 02: Checks 36 Byte Data Wrap in Extended Buffer Mode

This routine writes a 36 byte message on the first test address and reads the message back on the second address. This wrap is made in extended buffer mode. The first inbound data/status interrupt occurs when the 32 byte buffer is filled. The second data/status interrupt occurs with the remaining 4 bytes written and the occurrence of channel stop.

02002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

02002 *Expected results from the Read*

Condition code	00
Initial status	0C00
Ending status	0000
Expected sense	00

Routine 03: Checks Recognition of ETB and ETX in EBCDIC Mode

This routine writes a 36 byte message on the first test address and reads the message back on the second address. This wrap is made in extended buffer mode. The first inbound data/status interrupt occurs when the 32 byte buffer is filled. The second data/status interrupt occurs with the remaining 4 bytes written and the occurrence of channel stop.

The 34th character in the message is an ETB. This causes the CA to present channel stop to the responder. The write ends with a residual count of 2. The read command receives only 34 bytes and ends with a residual byte count of 2. On the second pass, the ETB is replaced with an ETX.

03002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Expected status	00

03002 *Expected results from the Read*

Condition code	00
Initial status	0C00
Ending status	0000
Expected sense	00

Routine 04: Checks Recognition of ETB and ETX in ASCII Mode

This routine writes a 36 byte message on the first test address and reads the message back on the second address. This wrap is made in extended buffer mode. The first inbound data/status interrupt occurs when the 32 byte buffer is filled. The second data/status interrupt occurs with the remaining 4 bytes written and the occurrence of channel stop.

The 34th character in the message is an ETB and causes the CA to present channel stop to the responder. The write command ends with a residual count of 2. The read command receives only 34 bytes and ends with a residual byte count of 2. On a second pass, the ETB is replaces with the ETX.

04002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

04002 *Expected results from the Read*

Condition code	00
Initial status	0C00
Ending status	0000
Expected sense	00

Routine 05: Checks the Recognition of DLE-STX

A 72 byte message with the DLE-STX character sequence inserted after 36 Bytes is written. ETB

and ETX characters are also inserted in the data following the DLE-STX sequence. The DLE-STX sequence causes the CA hardware to stop monitoring for control characters. The ETB and ETX characters should not cause an end to the write. All data written is read back on the ESC address.

This routine is performed first in EBCDIC mode, and then in ASCII mode.

If EXT = L is entered in the test request message, this routine will loop 256 times.

05002 *Expected results from the write*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

05002 *Expected results from the Read*

Condition code	00
Initial status	0C00
Ending status	0000
Expected sense	00

Routine 06: Checks DLE Remember
Two 36 byte messages are written on the native sub-channel address. The DLE is the last character of the first message. The STX is the first character of the second message. The responder, sees the DLE remember latch bit set because of the DLE. When the second Write is recognized the responder sets this bit in register X'6C'. The arrival of the STX character then causes the hardware to stop monitoring for control characters. Subsequent control characters, not being recognized by hardware, should not cause the write to end.

A 72 byte read command is issued to the ESC address. All 72 bytes written by the 2 write commands are read back.

This routine is performed first in EBCDIC mode then in ASCII mode.

06002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

06002 *Expected results from the Read*

Condition code	00
First status	0C00
Second status	0000
Expected sense	00

Routine 07: Checks SYN Character Monitor Test (Positive)
This routine writes a 16 byte message. The first pass has 4 EBCDIC SYN characters as the first 4 characters. The hardware is set to EBCDIC mode, disconnects from the channel, and presents a level 3 interrupt to the responder. The responder presents ending status to the write if it sees the SYN Monitor bit set. On a second pass, the SYN characters and mode are changed to ASCII mode.

Because the write command is terminated after 4 bytes, a residual byte count of 12 results. The 4 bytes written are read and verified. The read command is also a 16 byte read and ends with a residual byte count of 12.

07002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Residual count	0C
Expected sense	00

07002 *Expected results from the Read*

Condition code	00
First status	0C00
Second status	0000
Residual count	0C
Expected sense	00

Routine 08: Checks SYN Character Monitor Test (Negative)
This routine writes a 16 byte message. On the first pass, the 3705 is placed in EBCDIC mode. The first 4 bytes of the message are ASCII SYN characters.

The channel adapter hardware should not recognize a SYN character sequence. On the second pass of the test, the mode and the SYN characters are reversed. The results should be the same.

08002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Residual count	00
Expected sense	00

08002 *Expected results from the Read*

Condition code	00
First status	0C00
Second status	0000
Residual count	00
Expected sense	00

Routine 01: 250 Byte Wrap Test
This routine writes a 250 byte message on the first test address and reads the message back on the second address. The responder sets the channel adapter to the cycle steal mode.

01002 *Expected results from the Write*

Condition code	00
First CSW status	0800
Second CSW status	0400
Expected sense	00

01002 *Expected results from the Read*

Condition Code	00
First CSW status	0C00
Second CSW status	0000
Expected sense	00

Routine 02: Checks 255 Byte Data Wrap
This routine writes a 255 byte message on the first test address and reads the message back on the second address. The responder sets up the channel adapter for cycle steal mode.

02002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

02002 *Expected results from the Read*

Condition code	00
Initial status	0C00
Ending status	0000
Expected sense	00

Routine 03: Checks the 512 Byte Wrap Test
This routine writes a 520 byte message on the first test address and reads the message back on the second address. The responder sets the channel adapter to cycle steal mode. The count of 520 causes the channel adapter to require servicing three times from the responder. The first and second service is for 256 bytes each and the third is for the remaining 8 bytes.

This test makes two passes. On the second pass, the 3705 storage address where the test message is written and read is changed from X'1000' to X'1001'.

03002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

03002 *Expected results from the Read*

Condition code	00
Initial status	0C00
Ending status	0000
Expected sense	00

Routine 04: Checks the 520 Byte Wrap Test (to and from high storage)
This routine is similar to routine 03. The differences are the responder receives and transmits back the test message from high storage, starting at address X'FF00'. This test

verifies setting the byte X address bits in the cycle steal address register X'6E'. Prior to this test a 4 byte Write Break command sends the routine identification to the responder. The first 2 bytes identify the routine and the second 2 bytes define the 3705 storage address of the test message.

This routine makes three passes altering the test message address in the 3705 from X'FF00' to X'1FF00' to X'2FF00' respectively. If the 3705 storage is too small for these addresses, the responder defaults to an acceptable address.

04002	*Expected results from the Write*
Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

04002	*Expected results from the Read*
Condition code	00
Initial status	0C00
Ending status	0000
Expected sense	00

Test Section T3705AH

Routine 01: Checks Normal Mode Wrap Test
This routine writes a 16 byte message on the NSC test address and reads the message back on the same address. The wrap is made in normal mode (not extended buffer mode) and inbound data/status interrupts occur each time a four byte buffer is filled.

01002	*Expected results from the Write*
Condition code	00
First CSW status	0800
Second CSW status	0400
Expected sense	00

01002	*Expected results from the Read*
Condition code	00
First CSW status	0800
Second CSW status	0400
Expected sense	00

Routine 02: Checks 36 Byte Data Wrap in Extended Buffer Mode
This routine writes a 36 byte message on the NSC test address and reads the message back on the same address. This wrap is made in extended buffer mode. The first inbound data/status interrupt occurs when the 32 byte buffer is filled. The second data/status interrupt occurs with the remaining 4 bytes written and the occurrence of channel stop.

02002	*Expected results from the Write*
Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

02002	*Expected results from the Read*
Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

Routine 03: Checks Recognition of ETB and ETX in EBCDIC Mode
This routine writes a 36 byte message on the NSC test address and reads the message back on the same address. This wrap is made in extended buffer mode. The first inbound data/status interrupt occurs when the 32 byte buffer is filled. The second data/status interrupt occurs with the remaining 4 bytes written and the occurrence of channel stop.

The 34th character in the message is an ETB. This causes the channel adapter to present channel stop to the responder. The write ends with a residual count of 2. The read command receives only 34 bytes and ends with a residual byte count of 2. On the second pass, the ETB is replaced with an ETX.

03002	*Expected results from the Write*
Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

03002	*Expected results from the Read*
Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

Routine 04: Checks Recognition of ETB and ETX in ASCII Mode
This routine writes a 36 byte message on the NSC test address and reads the message back on the same address. This wrap is made in extended buffer mode. The first inbound data/status interrupt occurs when the 32 byte buffer is filled. The second data/status interrupt occurs with the remaining 4 bytes written and the occurrence of channel stop.

The 34th character in the message is an ETB and causes the channel adapter to present channel stop to the responder. The write command ends with a residual count of 2. The read command receives only 34 bytes and ends with a residual byte count of 2. On a second pass, the ETB is replaced with an ETX.

04002	*Expected results from the Write*
Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

04002	*Expected results from the Read*
Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

Routine 05: Checks the Recognition of DLE-STX
The 72 byte message with the DLE-STX character sequence inserted after 36 Bytes is written. ETB and ETX characters are also inserted in the data following the DLE-STX sequence. The DLE-STX sequence causes channel adapter hardware to discontinue monitoring for control characters.

The ETB and ETX characters should not cause an end to the write. All data written is read back on the same address.

The above is performed first in EBCDIC mode, and then in ASCII mode.

If EXT = L is entered in the test request message, this routine will loop 256 times.

05002	*Expected results from the Write*
Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

05002	*Expected results from the Read*
Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

Routine 06: Checks DLE Remember
Two 36 byte messages are written on the native sub-channel address. The DLE is the last characters of the first message. The STX is the first character of the second message. The responder, sees the DLE remember latch bit set because of the DLE. When the second write is recognized the responder sets this bit in register X'6C'. The arrival of the STX character then causes the hardware to discontinue monitoring for control characters. Subsequent control characters, not being recognized by hardware, should not cause the write to end.

A 72 byte read command is issued to the NSC address. All 72 bytes written by the 2 write commands are read back.

This test is performed first in EBCDIC mode then in ASCII mode.

06002	*Expected results from the Write*
Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

06002 *Expected results from the Read*

Condition code	00
First status	0800
Second status	0400
Expected sense	00

Routine 07: Checks SYN Character Monitor Test (Positive)
This routine writes a 16 byte message. The first pass has 4 EBCDIC SYN characters as the first 4 characters. The hardware is set to EBCDIC mode, disconnects from the channel, and presents a level 3 interrupt to the responder. The responder presents ending status to the write if it sees the SYN Monitor bit set. On a second pass, the SYN characters and mode are changed to ASCII mode.

Because the write command is terminated after 4 bytes, a residual byte count of 12 results. The 4 bytes written are read and verified. The read command is also a 16 byte read and ends with a residual byte count of 12.

07002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Residual count	0C
Expected sense	00

07002 *Expected results from the Read*

Condition code	00
First status	0800
Second status	0400
Residual count	0C
Expected sense	00

Routine 08: Checks SYN Character Monitor Test (Negative)
This routine writes a 16 byte message. On the first pass, the 3705 is placed in EBCDIC mode. The first 4 bytes of the message are ASCII SYN characters.

The CA hardware should not recognize a SYN character sequence. On a second pass of the test, the mode and the SYN characters are reversed. The results should be the same.

08002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Residual count	00
Expected sense	00

08002 *Expected results from the Read*

Condition code	00
First status	0800
Second status	0400
Residual count	00
Expected sense	00

Test Section T3705AI

Routine 01: 250 Byte Wrap Test
This routine writes a 250 byte message on the NSC test address and reads the message back on the same address. The responder sets the channel adapter to the cycle steal mode.

01002 *Expected results from the Write*

Condition code	00
First CSW status	0800
Second CSW status	0400
Expected sense	00

01002 *Expected results from the Read*

Condition code	00
First CSW status	0800
Second CSW status	0400
Expected sense	00

Routine 02: Checks 255 Byte Data Wrap
This routine writes a 255 byte message on the NSC test address and reads the message back on the same address. The responder sets up the channel adapter for cycle steal mode.

02002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

02002 *Expected results from the Read*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

Routine 03: Checks the 512 Byte Wrap Test
This routine writes a 520 byte message on the first NSC address and reads the message back on the same address. The responder sets the channel adapter to cycle steal mode. The count of 520 causes the channel adapter to require servicing three times from the responder. The first and second service is for 256 bytes each and the third is for the remaining 8 bytes.

This test makes two passes. On the second pass, the 3705 storage address where the test message is written and read is changed from X'1000' to X'1001'.

03002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

03002 *Expected results from the Read*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

Routine 04: Checks the 520 Byte Wrap Test (to and from high storage)
This routine is similar to routine 03. The differences are the responder receives and transmits back the test message from high storage, starting at address X'FF00'. This test verifies setting the byte X address bits in the cycle steal address register X'6E'. Prior to this test a four byte Write Break command sends the routine identification to the responder. The first 2 bytes identify the routine and the second 2 bytes define the 3705 storage address of the test message.

This routine makes three passes altering the test message address in the 3705 from X'FF00' to X'1FF00' to X'2FF00' respectively. If the 3705 storage is too small for these addresses, the responder defaults to an acceptable address.

04002 *Expected results from the Write*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

04002 *Expected results from the Read*

Condition code	00
Initial status	0800
Ending status	0400
Expected sense	00

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Configuration Data Set (CDS) for the 3705-80

WHAT THE CDS DOES

The CDS defines the 3705 hardware and is required by the diagnostic programs. The CDS, which is punched on cards, must accurately describe the exact configuration of the 3705-80. This section describes the CDS punched card format for the 3705-80.

The 3705-80 definition is provided in the On-Line-Test (OLT) CDS. The IFT loader appends the CDS to the Diagnostic Control Monitor (DCM) when the DCM is loaded into the 3705. The DCM refers to the CDS as required by the requested IFT. To determine the storage location of CDS information in the 3705-80, add the CDS byte location (shown in the card formats that follow) to X'F00'.

CDS REQUIREMENTS FOR THE 3705-80

The number and type of CDS cards that must be punched for the 3705-80 depend on (1) the hardware configuration of the 3705-80 and (2) whether a 3705 model other than 3705-80 is present on the host system. Figure CDS-1 shows the number and types of CDS cards required for specific configurations. An explanation and description of each CDS card type follows.

Host System 3705-80 Configuration	Dummy CDS Card	Channel Data Card	Index and CDS Cards	Range Definition Cards
3705-80 only with one CA and no RPL diskette feature	1	1	3	See Note
3705-80 with one type 1 CA and RPL	1	1	3	See Note
3705-80 with one type 4 CA and RPL	1	1	3	See Note
3705-80 with two type 4 CAs	1	1	3	See Note
3705-80 only with RPL diskette feature and no CA	N/A	N/A	N/A	N/A
Both a 3705-80 and a 3705 model other than model 80	N/A	1	3	See Note

Note: See "Range Definition Cards" later in this section.

Figure CDS-1. CDS Card Requirements for the 3705-80.

PREREQUISITE CDS INFORMATION

Fill out Figure CDS-2. This information will be required when punching CDS cards.

1. Check the 3705-80 features present.

RPL diskette feature (board B1)	____
Storage (board B2)	___*
CCU (boards B3 and B4)	___*
LIB position B (board A1)	____
LIB position A (board A2)	___*
CSB type 2 (board A3)	___*
Type 1 CA (board A4)	____
Type 4 CA (board A4)	____
Type 4 CA (board B1)	____
Two channel switch	____

* =always present for 3705-80

2. Enter the appropriate addresses in hex.

	Interface A (CA #1)	Interface B (CA #2)
Native subchannel (NSC) address	____	____
Low emulation subchannel (ESC)	____	____
High emulation subchannel (ESC)	____	____

3. Enter the appropriate oscillator speeds.

Osc 00 (01AA3T2)	____
Osc 01 (01AA3T4)	____
Osc 02 (01AA3U2)	____
Osc 03 (01AA3U4)	____

Note: The oscillator part numbers are shown on CS2 ALD pages TB411 through TB414.

4. Enter the appropriate line set types.

LIB Position A		LIB Position B	
Line Interface Address		Line Interface Address	
020-023	____	030-033	____
024-027	____	034-037	____
028-02B	____	038-03B	____
02C-02F	____	03C-03F	____

Figure CDS-2. Check List for 3705-80 Prerequiste CDS Information

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3705-80 DUMMY CDS CARD

A dummy CDS card is required for a 3705-80 unless either (1) a 3705 model other than the 3705-80 is present or (2) the 3705-80 has the RPL diskette feature installed and a type 1 CA or a type 4 CA is not installed.

The following format is used for the dummy CDS card.

Notes:

1. Columns not specified must be left blank.
2. The dummy CDS card information is not stored in the CDS.
3. The dummy CDS card is required for SOSPC to perform a sub-family selection using the auto-edit function.

Column	1	2 4		10 17	18 19	20 21	22 23	24 25		32	80
Description		CDS	Blank	Unused Subchannel Unit Address	08	80	40	06	Blank	/	

- End of 3705-80 Dummy CDS Card
- 3705-80 Unit or Type Code
- Terminal Control Unit Class Code
- 3705-80 Feature Code
- 3705 Dummy Feature Code
- Any available (unused) subchannel unit address in hex (right justified). For example: 0000000A.

CHANNEL DATA CDS CARD (CARD 1 OF 4)

A channel data CDS card is required for a 3705-80 unless the RPL diskette feature is installed and a type 1 or a type 4 CA is not installed.

The following format is used for the channel data CDS card:

Note: Columns not specified must be left blank.

F00

CDS Byte Location				00 03	04	05	06	07	08		09	0A 0B	0C 0D	0E		14 1B	1C 1D		72	73 80
Column	1	2 4		10 17	18 19	20 21	22 23	24 25			30 31		36 39	40 41		52 67			72	73 80
Description		CDS		Native Subchannel Unit Address	08		40	06					ESC Unit Adr			Symbolic name of the NCP CDS				Optional: Comments or card ID

Address must be in hex (right justified—for example, 000000F6). The initial tests (INIT), IFTs, and CA OLTs load across this channel address.

3705-80 Model Code

20 if 3705-80 has a type 4 channel adapter installed; otherwise 00.

Terminal Control Unit Class Code

3705-80 Unit or Type Code

4 if 3705-80 has 2-channel switch installed; otherwise 0.

4 if 3705-80 is shared with another system CPU; otherwise 0.

The emulation subchannel (ESC) unit address, in hex, of the lowest 2701, 02, or 03 emulation line address (determined by CA jumper options). See "Range Definitions" later in this section. If type 1/type 4 CA is in NCP mode only, leave columns 36-41 Blank.

The number of continuous emulation line addresses in hex. Each address used in testing requires a 2701, 02, or 03 CDS entry. See "Range Definitions" in this section.

The symbolic NCP CDS name is assigned by the user at SYSGEN time. It is punched in EBCDIC hex with a X'C3' (EBCDIC C) appended. This is required by the OLTT. Unused positions in this field are filled with X'40'. For example, assume that the symbolic name is "RTP". You would punch the EBCDIC code for RTPC in hex in columns 52-59. You would punch X'40' in columns 60-67 (D9E3D7C340404040).

Any character except /

INDEX AND DATA CDS CARDS

In addition to the channel data card, three index and data cards are required for a 3705-80. The index identifies the 3705-80 hardware configuration and points to the data bytes that contain a detailed description of the hardware.

The following format is used for the index and data CDS cards. If an entry is not applicable, leave it blank or punch it with zeros. However, the assigned card columns must be maintained.

006 (40-47)

Index and Data Card (2 of 4) (Columns not specified must be left blank)

CDS Byte Location		1E 1F		2E 2F	30 31	32 33		38 39		
Column	1	16 19		48 51	52 55	56 59		68 71	72 73	80
Description		1123		1223				1627		Optional: Comments or card ID

CCU Index

Storage Index

1322 for Type 1 CA Index
1922 for First Type 4 CA Index

2924 for Second Type 4 CA Index

Type 2 Communication Scanner Index

Any Character Except /

Index and Data Card (3 of 4)

CDS Byte Location		3A 41	42 43	44	45	46	47	48	49		4E		51	52	53	54	55			
Column	1	16	32 35	36 37	38 39	40 41	42 43	44 45	46 47		56 57		62 63	64 65	66 67	68 69	70 71	72 73		80
Description			FFFF		01	88	00		01		40		00						Optional: Comments or card ID	

End of CDS Index

First NSC Unit Address — Interface A

Frame Designation for First CA

256K Storage (Standard Size for 3705-80)

Reserved

Second NSC Unit Address — Interface A

Type 2 CSB

Frame Designation for Second CA4

Reserved

Speed of Oscillator Position 1 (OSC 00) (See Note 1)

Speed of Oscillator Position 2 (OSC 01) (See Note 1)

Speed of Oscillator Position 3 (OSC 02) (See Note 1)

Speed of Oscillator Position 4 (OSC 03) (See Note 1)

Any Character Except /

Note 1: Codes for Oscillator Speeds

Speed	Code
50.0	03
110.0	0D
134.5	0F
200.0	13
300.00	14
600.00	15
1200.00	17
2400.00	1B

Index and Data Card (4 of 4)

CDS Byte Location		56	57		5A 5B	5C 5D	5E 5F	60 61	62 63	64 65	66 67	68 69	6A 71			
Column	1	16 17	18 19		24 27	28 31	32 35	36 39	40 43	44 47	48 51	52 55	56 71	72	73	80
Description		13			Lines 0-1	Lines 2-3	Lines 4-5	Lines 6-7	Lines 0-1	Lines 2-3	Lines 4-5	Lines 6-7	/		Optional: Comments or Card ID	

LIB A Line Set Types (See Note 2)

LIB B Line Set Types (See Note 2)

LIB A Type X

13 for LIB B Type X or Blank if LIB is Not Present

M81	*	LS1	LS1	—	—	—	—	—
M82	*	LS1	LS1	—	LS1	LS1	LS1	—
M83	LS1	LS1	LS1	LS1	LS1	LS1	LS1	LS1
M84	*	LS1	LS1	—	LS8	LS8	LS8	—

*Feature Line Set (One LS2, LS3, LS4, LS5, LS8, or LS9)

Note 2: Codes for Line Set Types

Line Set Type	Code
Type 1 Half Duplex	0404
Type 1 Duplex	0808
Type 2 Half Duplex	0D0D
Type 2 Duplex	0F0F
Type 3 Half Duplex	0707
Type 3 Duplex	0E0E
Type 4 ACU Interface	0505
Type 5 High Speed Local Attach	1010
Type 8 Medium Speed (9600 bps or Less)	3939
Type 9 High Speed (Greater Than 9600 bps)	3A3A

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RANGE DEFINITION CARDS

Each emulation line address in the range defined by the channel data CDS card (columns 36-41) must be defined by an appropriate CDS entry or the message 'NO CDS ENTRY' will print for *each* undefined address. To prevent these messages from printing for unused lines (those lines not defined as an IBM 2701, 2702, or 2703 by a CDS entry), punch a dummy CDS entry for *each* unused address using the format that follows.

Notes:

1. Range definition dummy CDS cards are not required if either (1) the RPL diskette feature is not installed on the 3705-80 or (2) the type 1 CA or type 4 CA is in NCP mode only.
2. Card columns not specified must be left blank.

Column	1	2 4		10 17		22 25		52	80
Description		CDS		Unused ESC Unit Adr		4001		/	

The emulation subchannel (ESC) unit address, in hex, of an undefined emulation line address. The address range is defined by the channel data CDS card.

End of range definition card.

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POWER PROBLEM ISOLATION

PAGE 1 OF 2

ENTRY POINTS

FROM	ENTER THIS MAP		
MAP NUMBER	ENTRY POINT	PAGE NUMBER	STEP NUMBER

No entries in this table

EXIT POINTS

EXIT THIS MAP		TO	
PAGE NUMBER	STEP NUMBER	MAP NUMBER	ENTRY POINT
1	003	2130	A
2	011	2130	A
2	012	2130	A

001
Note: Verify that all 3 phases of A.C. input voltage are correct. The A.C. voltage can be checked at SCRs 1, 2, and 3 (ALD YZ830).
Is the POWER CHECK light on?
Y N

002
Is the 3705 powered up but can not be powered down?
Y N

003
Go To Map 2130, Entry Point A.

004
- Meter 01D-A1C1M02 while pressing the POWER OFF switch.

Is +24 Vdc present at 01D-A1C1M02?
Y N

005
- Check the POWER OFF switch and verify that +24 Vdc is present at the switch.

006
Is approximately 0 Vdc present at 01D-A1C1M09? (Picks PPB-K2)
Y N

007
- Check the PPB-K2 relay for a stuck-on condition.

2 2
A B

A B
1 1

POWER PROBLEMS

PAGE 2 OF 2

008
- Replace the master sequence card at 01D-A1C1.
- Check the cabling from 01D-A1C1U02 to the PPB-K2 coil.

009
Is the THERMAL light on at the 01D gate?
Y N

010
Did the power check occur during the initial power-on sequence?
Y N

011
- Check the LEDs on the 01D gate in the order listed below and go to the appropriate MAP (refer to 'Checking SCRs' on D-560):

LED Indicator	MAP
Any O/V	2147
-4V OC1	2148
-4V U/V	2141
+6V U/V	2144
-12V U/V	2145
+12V U/V	2146
+5V U/V	2142
-5V U/V	2143

If no LEDs are on,
Go To Map 2130, Entry Point A.

012
- Press POWER OFF.

Go To Map 2130, Entry Point A.

013
- Press the THERMAL RESET switch on the 01D gate.

Does the THERMAL light turn off?
Y N

014
- Power down and turn off main CB. Remove master sequence card 01D-A1C1 and use ohmmeter to check continuity from card side pins C1G08 to C1J04.

Does meter read 0 ohms?
Y N

C D E

C D E
1 1

015
- Use ohmmeter to isolate defective thermal switch (YZ822).
- Check air filters and blowers.

016
- Replace master sequence card at 01D-A1C1.
- Check air filters and blowers.

017
*The thermal condition is gone (thermal switch has dropped).
- Check all air filters and blowers.

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POWER-ON PROBLEMS

PAGE 1 OF 5

ENTRY POINTS

FROM	ENTER THIS MAP		
MAP NUMBER	ENTRY POINT	PAGE NUMBER	STEP NUMBER
2100	A	1	001

001
(Entry Point A)
NOTE: When servicing inside the 01D gate, the indicator panel should be placed in the maintenance position (see D-520).
Is +24 Vdc present at 01D-TB1-6? (YZ824)
Y N

002
•If more than 2.4V ripple is present at 01D-TB1-6, replace the capacitor PPB-C1.
Is +24 Vdc present at 01D-TB1-8?
Y N

003
•Use an ac meter to measure the PPB-T2 output voltages.
Expected voltage from 24.2 to 33.3 Vac rms between:
PPB-T2-TB5-1 and PPB-T2-TB5-6
PPB-T2-TB5-2 and PPB-T2-TB5-6
Are these voltages within the specified range?
Y N

004
•Check PPB-CP2, PPB-CB2, PPB-CB1 and the input voltage (YZ802 and YZ804).

005
•Check the diodes at PPB-T2-TB5-1 and at PPB-T2-TB5-2.

006
•Replace the diode between 01D-TB1-6 and 01D-TB1-8.

A

007
Is +5 Vdc Standby present at 01D-A1C1P03? (YZ859)
Y N

008
•If more than 200mV ripple is present at 01D-A1C1P03, replace the capacitor 01D-C2.
Is approximately +12 Vdc present at 01D-TB1-2? (YZ824)
Y N

009
•Use an ac meter to measure the PPB-T2 output voltages.
Expected voltage from 11 to 27 Vac rms between:
01D-TB1-1 and 01D-Gnd TB
01D-TB1-3 and 01D-Gnd TB
Are these voltages within the specified range?
Y N

010
•Check the PPB-T2 transformer and cabling to 01D-TB1.

011
•Check the diodes at 01D-TB1-2.

012
•Remove the cards at 01D-A1C1 and 01D-A1E1.
Is +5 Vdc Standby present at 01D-A1C1P03 now? (YZ859)
Y N

013
•Replace the +5 V Standby regulator at 01D-Q3 (YZ824).
•Reinstall the cards at 01D-A1C1 and 01D-A1E1.

014
*One of these two cards is shorting the +5 V standby supply.
•Replace the defective card.

2 B

B 1

015
•Press POWER ON.
Does PPB-K2 pick (even if only momentarily)? (YZ822)
Y N

016
Is PPB-K1 picked?
Y N

017
Is 01D-RY2 picked? (EPO relay)
Y N

018
Is the EPO cable plugged in the appropriate connector?
Y N

019
•Plug the EPO cable into the appropriate connector.

020
•Temporarily jumper EPO-JX pins 1 to 2.
Does 01D-RY2 pick?
Y N

021
•Remove the EPO-JX jumper.
Is +24 Vdc present at EPO-JX pin 1?
Y N

022
•Check the cabling from 01D-TB1-8 to EPO-JX-1.

023
•Check the 01D-RY2 coil.

024
•Remove the EPO-JX jumper.
•Check the EPO cable and associated CPU.

025
•Check the 01D-RY2-3 points.

3 C D

D

026
Is approximately 0 Vdc present at 01D-A1C1M09? (-Pick PPB-K2, YZ855)
Y N

027
Is the LOCAL/REMOTE switch in the local position? (YZ822)
Y N

028
Is 0 Vdc present at LOCAL/REMOTE switch terminal 3 (N/C)?
Y N

029
•Check the LOCAL/REMOTE switch.

030
Is at least +2.5 Vdc present at LOCAL/REMOTE switch terminal 1 (N/O)?
Y N

031
•Check the LOCAL/REMOTE switch.
•Check the master sequence card at 01D-A1C1 (YZ860).
•Check cabling from LOCAL/REMOTE switch terminal 1 (N/O) to 01D-A1C1J09.

032
*A CPU or channel power on must be initiated to provide a contact closure within the CPU. This closure returns +24 Vdc to the EPO panel (EPO-J1).
Is +24 Vdc present at EPO-J1-6?
Y N

033
•Check the CPU cable and associated CPU.

034
•Replace the master sequence card at 01D-A1C1.
•Check cabling from EPO-J1-6 to 01D-A1C1G12 (+Pick).
•Check cabling from LOCAL/REMOTE switch terminal 3 (N/C) to 01D-A1C1G09 (+Remote On).

3 E 3 F

F 2

POWER-ON PROBLEMS

PAGE 3 OF 5

035
Is 0 Vdc present at LOCAL/REMOTE switch terminal 1 (N/O)?
Y N

036
- Check the LOCAL/REMOTE switch.

037
Is at least +2.5 Vdc present at LOCAL/REMOTE terminal switch 3 (N/C)?
Y N

038
- Check the LOCAL/REMOTE switch and cabling (YZ822).
- Check the master sequence card at 01D-A1C1 (YZ860).
- Check cabling from LOCAL/REMOTE switch terminal 3 (N/C) to 01D-A1C1G09.

039
- Meter 01D-A1C1P02 while pressing the POWER ON switch.

Is +24 Vdc present at 01D-A1C1P02? (YZ854)
Y N

040
Is +24 Vdc present at 01D-TB1-9? (YZ822)
Y N

041
- Check the 01D-RY2-1 points.

042
- Check the POWER ON switch and verify that +24 Vdc is present at the switch.
- Check cabling from POWER ON switch to 01D-A1C1J02.

043
- Replace the master sequence card at 01D-A1C1.
- Check cabling from LOCAL/REMOTE switch (terminal 1 N/O) to 01D-A1C1J09 (+Local On).

C 2 E 2

MAP 2130-3

044
- Check the PPB-K2 coil and wiring (YZ822).

045
- Press POWER OFF.
- Place a jumper between pins 01D-A1C1M07 and 01D-A1C1P08 (disables the 12 second time out, master seq., YZ829).
- Place a jumper between pins 01D-A1E1G12 and 01D-A1E1J08. (Disables the 12 second timeout, frame seq., YZ827.)
- Press POWER ON.

Does PPB-K2 pick and remain picked?
Y N

046
Is 0 Vdc present at 01D-TB1-10? (-Crash, YZ824)
Y N

047
Is 24 Vdc present at Op Panel Power Off Switch, Common? (YZ822)
Y N

048
- Press POWER OFF.
- Check the -24 V standby supply at 01D-C1(-) and replace the capacitor 01D-C1 if more than 2.4V ripple is present (YZ824).
- Check the +24 V standby supply at PPB-C1(+) and replace the capacitor PPB-C1 if more than 2.4V ripple is present.
- Replace the master sequence card at 01D-A1C1.
- If the problem still exists, check 01D-C3 instead.
- Check cabling from Power Off Switch to 01D-A1C1G02 (+24V Pwr Off Sw, YZ822).
- See Notes 1 and 6.

049
- Check for a shorted POWER OFF switch.
- See Notes 1 and 6.

4 4
G H

MAP 2130-3

G 3 H 3

POWER-ON PROBLEMS

PAGE 4 OF 5

050
- Replace the frame sequence card at 01D-A1E1.
- If the problem still exists, replace the master sequence card at 01D-A1C1 instead.
- Check for a short at 01D-TB1-10 and cabling.
- See Notes 1 and 6.

051
Is between +4.5 Vdc and +5.5 Vdc present at 01D-Q2-2? (YZ824, YZ886, sheet 4 of 11)
Y N

052
- If more than 200mV ripple is present at 01D-Q2-3, replace the capacitor 01D-C3.

Is approximately +30 Vdc present at 01D-TB1-13? (YZ824)
Y N

053
- Use an AC meter to measure the T3 output voltages between 01D-TB1-12 and 01D-TB1-14.

Is approximately +30 Vac rms present between 01D-TB1-12 and 01D-TB1-14?
Y N

054
- Check the T3 transformer and the PPB-K2-2 points (YZ830).
- See Notes 1 and 6.

055
- Check the diodes at 01D-TB1-13.
- See Notes 1 and 6.

056
- Replace the +5 V regulator at 01D-Q2.
- Check 01D-R4.
- See Notes 1 and 6.

057
Is 01D-RY1 picked? (YZ822)
Y N

5 5
J K

K

MAP 2130-4

058
Is between +4.5 Vdc and +5.5 Vdc present at 01D-A1E1J03? (YZ827)
Y N

059
- Replace the +5 V regulator at 01D-Q1 (YZ824).
- See Notes 1 and 6.

060
Are any of the LEDs on the 01D gate on?
Y N

061
Is at least +2.5 Vdc present at 01D-TB1-7?
Y N

062
- Replace the master sequence card at 01D-A1C1.
- Check the cabling from 01D-A1C1U05 to 01D-TB1-7.
- See Notes 1 and 6.

063
Is 0 Vdc present at 01D-RY1-B? (YZ822)
Y N

064
- Replace the frame sequence card at 01D-A1E1.
- Check cabling from 01D-E1B02 to 01D-RY1-B.
- Check cabling from 01D-TB7 to 01D-A1E1B13 (YZ822).
- See Notes 1 and 6.

065
- Check the 01D-RY1 coil (YZ822).
- See Notes 1 and 6.

5
L

MAP 2130-4

POWER-ON PROBLEMS

066

- Check the LEDs on the 01D gate in the order listed below and go to the appropriate MAP (refer to the 'Checking SCRs' on D-560):

LED Indicator	MAP
Any O/V	2147
-4V OC1	2148
-4V U/V	2141
+6V U/V	2144
-12V U/V	2145
+12V U/V	2146
+5V U/V	2142
-5V U/V	2143

067

Is +24 Vdc present at 01D-A1C1P05? (sequence complete new, YZ829)

Y N

068

- Check the 01D-RY1-1 points.
- See Notes 1 and 6.

069

Is approximately 0 Vdc present at Op Panel Power ON Indicator 1-B? (YZ822)

Y N

070

- Replace the master sequence card at 01D-A1C1.
- Check cabling from 01D-A1C1S03 to Power On Indicator 1-B.
- See Notes 1 and 6.

071

- Check the POWER ON light.
- See Notes 1 and 6.

****

Note 1: Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.

Note 6: Remove the jumper between pins 01D-A1E1G12 and 01D-A1E1J08.

-4 V UNDER-VOLTAGE

PAGE 1 OF 3

001
(Entry Point A)

CAUTION

A shorted SCR can damage the phase control card (01D-A1A1), also a defective phase control card can damage an SCR. Refer to the 'Checking SCRs' on D-560 to check for shorted SCRs.

- Press POWER OFF.
- Place a jumper between pins 01D-A1C1M07 and 01D-A1C1P08 (disables the 12-second timeout, master seq., YZ829).
- Place a jumper between pins 01D-A1E1G12 and 01D-A1E1J08 (disables the 12-second time out) if not already present. (Frame sequence, YZ827)
- Press POWER ON.

Is 0 Vdc present at 01A-TB1-13? (-4 V sense, YZ836)
Y N

002
Is -4 Vdc present at 01A-TB1-13?
Y N

003
- Scope the -4 V SCRs at 01F-HS1 (YZ886, sheet 5).

Are both SCRs firing? (Refer to 'Checking SCRs' on D-560.)
Y N

004
- Scope the gate pulses at 01D-A1A1B09. (YZ866)

Are the gate pulses present? (Refer to 'Checking SCRs' on D-560.)
Y N

005
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1 if applicable.
- See Note 6.

2 2
A B C D

C D MAP 2141-1

006
- Press POWER OFF.
- Measure the resistance of the pulse transformer secondary coils between the following pins:
  01D-A1A1G11 and 01D-A1A1J11
  01D-A1A1G13 and 01D-A1A1J13

Is less than 20 ohms present? (YZ866)
Y N

007
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1 if applicable.
- See Note 6.

008
- Check for AC at cathode of failing SCR(s).
- Check the failing SCR(s) and cabling from the phase control card.
- See Note 1 if applicable.
- See Note 6.

009
- Scope the -4 V SCRs at 01F-HS2 (YZ886, sheet 5).

Are both SCRs firing? (Refer to 'Checking SCRs' on D-560.)
Y N

010
- Scope the gate pulses at 01D-A1A1B07. (YZ866)

Are the gate pulses present? (Refer to 'Checking SCRs' on D-560.)
Y N

011
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1 if applicable.
- See Note 6.

2 2
E F

MAP 2141-1

E F
1 1

-4 V UNDER-VOLTAGE

PAGE 2 OF 3

012
- Press POWER OFF.
- Measure the resistance of the pulse transformer secondary coil between the following pins:
  01D-A1A1G06 and 01D-A1A1J06
  01D-A1A1G09 and 01D-A1A1J09

Is less than 20 ohms present? (YZ866)
Y N

013
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1 if applicable.
- See Note 6.

014
- Check for AC at cathode of failing SCR(s).
- Check the failing SCR(s) and cabling from the phase control card.
- See Note 1 if applicable.
- See Note 6.

015
- Scope the -4 V SCRs at 01F-HS3 (YZ886, sheet 5).

Are both SCRs firing? (Refer to 'Checking SCRs' on D-560.)
Y N

016
- Scope the gate pulses at 01D-A1A1B11. (YZ866)

Are the gate pulses present? (Refer to 'Checking SCRs' on D-560.)
Y N

017
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1 if applicable.
- See Note 6.

G H

A B G H
1 1

MAP 2141-2

018
- Press POWER OFF.
- Measure the resistance of the pulse transformer secondary coil between the following pins:
  01D-A1A1G02 and 01D-A1A1J02
  01D-A1A1G04 and 01D-A1A1J04

Is less than 20 ohms present? (YZ866)
Y N

019
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1 if applicable.
- See Note 6.

020
- Check for AC at cathode of failing SCR(s).
- Check the failing SCR(s) and cabling from the phase control card.
- See Note 1 if applicable.
- See Note 6.

021
- Adjust the -4 V pot on the phase control card at 01D-A1A1 to increase the voltage (see D-580).
- Replace the phase control card if adjusting the pot does not fix it. (Refer to 'DC Voltage Measurement' on D-580.)
- Check for open 01F-L1, 01F-L2 and 01F-L3 chokes (YZ886, sheet 6).
- See Note 1 if applicable.
- See Note 6.

022
- Replace the frame sequence card at 01D-A1E1.
- Check cabling from 01A-TB1-13 to 01D-A1E1M08 (YZ827).
- See Note 1 if applicable.
- See Note 6.

023
Is -24 Vdc present at 01D-C1(-terminal)? (-24 V bulk supply, YZ824)
Y N

3 3
J K

MAP 2141-2

J K
2 2

-4 V UNDER-VOLTAGE

PAGE 3 OF 3

024
- If more than 2.4V ripple is present, replace the capacitor 01D-C1.
- Check the diode at PPB-T2-TB5-4.

025
Is at least +1.0 Vdc present at 01D-A1E2P04? (drive signal for -4 V supply, YZ851 use CAUTION in probing this point)
Y N

026
- Replace the frame sequence card at 01D-A1E1.
- If the problem still exists, replace the phase control card at 01D-A1A1 instead. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1 if applicable.
- See Note 6.

027
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- If the problem still exists, check 01F-L1,L2,L3 choke and SCRs instead (YZ886, sheet 6).
- See Note 1 if applicable.
- See Note 6.

****

Note 1: Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
Note 6: Remove the jumper between pins 01D-A1E1G12 and 01D-A1E1J08.

+5 VDC UNDER-VOLTAGE (STORAGE)

MAP 2142-1

PAGE 1 OF 2

ENTRY POINTS

FROM	ENTER THIS MAP		
MAP NUMBER	ENTRY POINT	PAGE NUMBER	STEP NUMBER
No entries in this table			

EXIT POINTS

EXIT THIS MAP		TO	
PAGE NUMBER	STEP NUMBER	MAP NUMBER	ENTRY POINT
1	003	2146	A

001
(Entry Point A)
- Press Power Off
- Place a jumper between pins 01D-A1C1M07 and 01D-A1C1P08 (disables the 12-second timeout, master sequence, YZ829).
- Place a jumper between pins 01D-A1E1G12 and 01D-A1E1J08 (disables the 12-second timeout, frame sequence, YZ827).
- Press power on.

Is +12 Vdc present at 5V REG TB1-1? (YZ836)
Y N

002
Is +12 Vdc present at 01A-TB1-2? (YZ836)
Y N

003
Go To Map 2146, Entry Point A.

004
- Check cables from 01A-TB1-2 (YZ836)

005
Is 0 Vdc present at 5V REG TB1 8 & 9?
Y N

006
Is +5 Vdc present at 5V REG TB1 8 & 9?
Y N

007
Is 6 AMP F1 on -5/+5 regulator asm. blown?
Y N

2 A 2 B 2 C 2 D

A 1 B 1 C 1 D 1

+5 VDC UNDER-VOLTAGE

PAGE 2 OF 2

008
- Adj +5VDC POT on -5/+5 regulator asm. (see D-580).
- Replace -5/+5 regulator asm, if +5VDC adjustment does not correct problem. (Refer to 'Checking SCRs' on D-560.)
- See Note 1.
- See Note 6.

009
Go to Step 015, Entry Point B.

010
Is +5VDC present at 5V REG TB1-10?
Y N

011
- Replace diode 1.
- See Note 1.
- See Note 6.

012
- Check cabling to 01D-A1E1M06.
- Replace the frame sequence card at 01D-A1E1.
- See Note 1.
- See Note 6.

013
Is 6 AMP fuse 1 on -5/+5 regulator asm. blown?
Y N

014
- Replace -5/+5 Regulator Asm. and adjust +5 Vdc.
- See Note 1.
- See Note 6.

015
(Entry Point B)
- Press Power Off.
- Remove storage cards at 01A-B2T2 & U2.
- Replace 6 AMP F1.
- Press Power On.

Does 6 AMP F1 blow again?
Y N

E F

E F

MAP 2142-2

016
- To isolate the storage card which may be drawing excessive current, replace cards at 01A-B2T2 & U2 one at a time while monitoring +5 VDC at 01D-A1E1M06.
- To isolate 01A-B2 board, remove leads at 5V REG TB1-8 & 9 (YZ836).
- Replace -5/+5 regulator Asm. and adjust +5VDC if problem still exists.
- See Note 1.
- See Note 3.
- See Note 6.

017
- To isolate 01A-B2 board, remove leads at 5V REG TB1-8 & 9 (YZ836).
- Replace -5/+5 regulator Asm. and adjust +5 VDC if problem still exists.
- See Note 1.
- See Note 3.
- See Note 6.

****

Note 1: Remove jumper between pins 01D-A1E1G12 and 01D-A1E1J08.

Note 3: Reinstall the removed storage cards in their original position.

Note 6: Remove jumper between pins 01D-A1C1M07 and 01D-A1C1P08 (if installed).

-5 VOLT UNDER-VOLTAGE (STORAGE)

ENTRY POINTS

FROM	ENTER THIS MAP		
MAP NUMBER	ENTRY POINT	PAGE NUMBER	STEP NUMBER
No entries in this table			

EXIT POINTS

EXIT THIS MAP		TO	
PAGE NUMBER	STEP NUMBER	MAP NUMBER	ENTRY POINT
1	003	2145	A

001
- Press power off.
- Place a jumper between pins 01D-A1C1M07 and 01D-A1C1P08 (disables the 12 second timeout, master sequence, YZ829).
- Place a jumper between pins 01D-A1E1G12 and 01D-A1E1J08 (disables the 12 second timeout, frame sequence, YZ817).

Press power on.

Is -12 Vdc present at 5V REG TB1-2? (YZ836)

Y N

002

Is -12 Vdc present at 01A-TB1-3? (YZ836)

Y N

003

Go To Map 2145, Entry Point A.

004
- Check cables from 01A-TB1-3 (YZ836).

005

Is 0 Vdc present at 5V REG TB1-7?

Y N

006

Is -5 Vdc present at 5V REG TB1-7?

Y N

2 2 2
A B C

C
1

-5 VOLT UNDER-VOLTAGE

007

(Entry Point A)
- Press power off.
- Remove storage cards at 01A-B2T2 & U2.
- Press Power on.

Is -5 Vdc present at 5V REG TB1-7?

Y N

008

Press power off.
- Disconnect, at 5V REG TB1-7 (YZ836), the two -5VDC cables to the 01AB2 board.
- Press power on.

Is -5 Vdc present at 5V REG TB1-7?

Y N

009
- Replace -5/+5 regulator asm and adjust +5 Vdc. (See D-580.)
- See Note 1.
- See Note 3.
- See Note 6.

010
- Short in -5VDC cables or 01A-B2 board.
- See Note 1.
- See Note 3.
- See Note 6.

011
- Isolate the storage card which may be drawing excessive current by replacing cards one at a time while monitoring -5VDC at 5V REG TB1-7.
- See Note 1.
- See Note 3.
- See Note 6.

A B
1 1

012
- Check cabling from 5V REG TB1-7 to 01D-A1E1M05.
- Replace frame sequence card at 01D-A1E1.
- See Note 1.
- See Note 3.
- See Note 6.

****

Note 1: Remove jumper between pins 01D-A1E1G12 and 01D-A1E1J08.

Note 3: Reinstall the removed storage cards in their original positions.

Note 6: Remove jumper between pins 01D-A1C1M07 and 01D-A1C1P08 (if installed).

013

Go to Step 007, Entry Point A.

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+6 V UNDER-VOLTAGE

PAGE 1 OF 2

001
(Entry Point A)

CAUTION

A shorted SCR can damage the phase control card (01D-A1A1), also a defective phase control card can damage an SCR. Refer to 'Checking SCRs' on D-560 to check for shorted SCRs.

Is 01F-CP1 tripped? (YZ886, sheet 3)
Y N

002
- Press POWER OFF.
- Place a jumper between pins 01D-A1C1M07 and 01D-A1C1P08 (disables the 12 second timeout, master seq., YZ829).
- Place a jumper between pins 01D-A1E1G12 and 01D-A1E1J08 (disables the 12 second time out) if not already present. (Frame seq. YZ827)
- Press POWER ON.

Is 0 Vdc present at 01A-TB1-12? (+6 V sense, YZ836)
Y N

003
Is +6 Vdc present at 01A-TB1-12?
Y N

004
- Scope the +6 V SCRs at the base of 01F-HS7 (YZ886, sheet 5)

Are both SCRs firing? (Refer to 'Checking SCRs' on D-560.)
Y N

005
- Press POWER OFF.
- Measure the resistance of the pulse transformer secondary coils between the following pins:
  01D-A1A1G07 and 01D-A1A1J07
  01D-A1A1G08 and 01D-A1A1J08

Is less than 20 ohms present? (YZ866)
Y N

2
A B C D E F

B C D E F MAP 2144-1

006
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1.
- See Note 6.

007
- Press power on.
- Check for AC at cathode of failing SCR.
- Check the failing SCR and cabling from the phase control card.
- See Note 1.
- See Note 6.

008
- Adjust the +6 V pot on the phase control card at 01D-A1A1 to increase the voltage (see D-580).
- Replace the phase control card if adjusting the pot does not fix it. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1.
- See Note 6.

009
- Replace the frame sequence card at 01D-A1E1.
- Check cabling from 01A-TB1-12 to 01D-A1E1P02 (YZ827).
- See Note 1.
- See Note 6.

010
Is at least +2.5 VDC present at 01D-A1E1M04? (drive signal for +6V supply, YZ827, use CAUTION in probing this point)
Y N

011
- Replace the frame sequence card at 01D-A1E1.
- If the problem still exists, replace the phase control card at 01D-A1A1 instead. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1.
- See Note 6.

2
G MAP 2144-1

A G
1 1 **+6 V UNDER-VOLTAGE**

PAGE 2 OF 2

012
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- If the problem still exists, check 01F-CP1, 01F-L4 choke and SCRs instead (YZ886, sheet 5).
- Check circuit.
- See Note 1.
- See Note 6.

013
- Press POWER OFF.
- Disconnect the laminar bus lugs at 01A-TB1-5 and 01A-TB1-12 (YZ836).
- Reset 01F-CP1.
- Press POWER ON.

Does 01F-CP1 trip again?
Y N

014
- Determine which lead causes the circuit protector to trip by powering up after replacing the laminar bus lugs one at a time.

CAUTION

- Isolate the short to a logic board by removing the laminar bus jumpers to each board. Before removing or reinstalling the laminar bus jumpers from/to a board, power must be off until the jumpers are all off/on. Otherwise, the current required by the board assembly could exceed the capacity of the board pins and burn them off.
- Isolate to a card by removing cards.
- See Notes 1 and 6.

H

H MAP 2144-2

015
- Press POWER OFF.
- Reconnect the laminar bus lugs at 01A-TB1-5 and 01A-TB1-12.
- Replace capacitor, 01F-C3 (YZ886, sheet 5).
  WARNING: Circuit damage may occur if power is applied with the capacitor disconnected.
- Reset 01F-CP1.
- Press POWER ON.

Does 01F-CP1 trip again?
Y N

016
- Return to normal operation.

017
- Check for a bad circuit protector, 01F-CP1.
- See Notes 1 and 6.

****

Note 1: Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
Note 6: Remove the jumper between pins 01D-A1E1G12 and 01D-A1E1J08.

MAP 2144-2

-12 V UNDER-VOLTAGE

PAGE 1 OF 2

001
(Entry Point A)

CAUTION

A shorted SCR can damage the phase control card (01D-A1A1), also a defective phase control card can damage an SCR. Refer to 'Checking SCRs' on D-560 to check for shorted SCRs.

Is 01F-CP2 tripped? (YZ886, sheet 3)
Y N

002
- Press POWER OFF.
- Place a jumper between pins 01D-A1C1M07 and 01D-A1C1P08 (disables the 12 second timeout, master seq., YZ829).
- Place a jumper between pins 01D-A1E1G12 and 01D-A1E1J08 (disables the 12 second time out) if not already present. (Frame seq. YZ827)
- Press POWER ON.

Is 0 Vdc present at 01A-TB1-3? (-12 V sense, YZ836)
Y N

003
Is -12 Vdc present at 01A-TB1-3?
Y N

004
- Scope the -12 V SCRs at the base of 01F-HS5 (YZ886, sheet 5).

Are both SCRs firing? (Refer to 'Checking SCRs' on D-560.)
Y N

005
- Press POWER OFF.
- Measure the resistance of the pulse transformer secondary coils between the following pins:
  01D-A1A1G03 and 01D-A1A1J03
  01D-A1A1G05 and 01D-A1A1J05

Is less than 20 ohms present? (YZ866)
Y N

2 A B C D E F

B C D E F MAP 2145-1

006
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1.
- See Note 6.

007
- Press power on.
- Check for AC at cathode of failing SCR.
- Check the failing SCR and cabling from the phase control card.
- See Note 1.
- See Note 6.

008
- Adjust the -12 V pot on the phase control card at 01D-A1A1 to increase the voltage (refer to 'Checking SCRs' on D-560).
- Replace the phase control card if adjusting the pot does not fix it. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1.
- See Note 6.

009
- Replace the frame sequence card at 01D-A1E1.
- Check cabling from 01A-TB1-3 to 01D-A1E1P07 (YZ827).
- See Note 1.
- See Note 6.

010
Is at least +2.5 Vdc present at 01D-A1E1M13? (Drive signal for -12V supply, YZ827, use CAUTION in probing this point.)
Y N

011
- Replace the frame sequence card at 01D-A1E1.
- If the problem still exists, replace the phase control card at 01D-A1A1 instead. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1.
- See Note 6.

2 G MAP 2145-1

A G
1 1

-12 V UNDER-VOLTAGE

PAGE 2 OF 2

012
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- If the problem still exists, check 01F-CP2, 01F-L5 choke and SCRs instead (YZ886, sheet 5).
- Check circuit.
- See Note 1.
- See Note 6.

013
- Press POWER OFF.
- Disconnect the laminar bus lugs at 01A-TB1-3 and 01A-TB1-4 (YZ836).
- Reset 01F-CP2.
- Press POWER ON.

Does 01F-CP2 trip again?
Y N

014
- Determine which lead causes the circuit protector to trip by powering up after replacing the laminar bus lugs one at a time.

CAUTION

- Isolate the short to a logic board by removing the laminar bus jumpers to each board. Before removing or reinstalling the laminar bus jumpers from/to a board, power must be off until the jumpers are all off/on. Otherwise, the current required by the board assembly could exceed the capacity of the board pins and burn them off.
- Isolate to a card by removing cards.
- See Notes 1 and 6.

H MAP 2145-2

015
- Press POWER OFF.
- Reconnect the laminar bus lugs at 01A-TB1-3 and 01A-TB1-4.
- Replace capacitor, 01F-C4. (YZ886, sheet 5)
  WARNING: Circuit damage may occur if power is applied with the capacitor disconnected.
- Reset 01F-CP2.
- Press POWER ON.

Does 01F-CP2 trip again? (YZ886, sheet 6)
Y N

016
- Return to normal operation.

017
- Check for a bad circuit protector, 01F-CP2.
- See Notes 1 and 6.

****

Note 1: Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
Note 6: Remove the jumper between pins 01D-A1E1G12 and 01D-A1E1J08.

H MAP 2145-2

+12 V UNDER-VOLTAGE

PAGE 1 OF 2

001
(Entry Point A)

CAUTION

A shorted SCR can damage the phase control card (01D-A1A1), also a defective phase control card can damage an SCR. Refer to 'Checking SCRs' on D-560 to check for shorted SCRs.

Is 01F-CP3 tripped? (YZ886, sheet 3)
Y N

002
- Press POWER OFF.
- Place a jumper between pins 01D-A1C1M07 and 01D-A1C1P08 (disables the 12 second timeout, master seq., YZ829).
- Place a jumper between pins 01D-A1E1G12 and 01D-A1E1J08 (disables the 12 second time out) if not already present. (Frame seq. YZ827)
- Press POWER ON.

Is 0 Vdc present at 01A-TB1-1? (+12 Vdc output, YZ836)
Y N

003
Is +12 Vdc present at 01A-TB1-1?
Y N

004
- Scope the +12 V SCRs at the base of 01F-HS6 (YZ886, sheet 5)

Are both SCRs firing? (Refer to 'Checking SCRs' on D-560.)
Y N

005
- Press POWER OFF.
- Measure the resistance of the pulse transformer secondary coils between the following pins:
  01D-A1A1G10 and 01D-A1A1J10
  01D-A1A1G12 and 01D-A1A1J12

Is less than 20 ohms present? (YZ866)
Y N

2 A B C D E F

006
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1.
- See Note 6.

007
- Press power on.
- Check for AC at cathode of failing SCR.
- Check the failing SCR and cabling from the phase control card.
- See Note 1.
- See Note 6.

008
- Adjust the +12 V pot on the phase control card at 01D-A1A1 to increase the voltage (see D-580).
- Replace the phase control card if adjusting the pot does not fix it. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1.
- See Note 6.

009
Is +12VDC present at 01A-TB1-14? (+12 V sense)
Y N

010
- Replace diode 1 between 01A-TB1-1 and 14.
- See Note 1.
- See Note 6.

011
- Replace the frame sequence card at 01D-A1E1.
- Check cabling from 01A-TB1-1 to 01D-A1E1M03 (YZ827).
- See Note 1.
- See Note 6.

012
Is approximately 40 Vac peak-to-peak (15 Vac rms) present at cathode of SCR 5? (YZ886, sheet 5 of 11)
Y N

2 2
G H

+12 V UNDER-VOLTAGE

PAGE 2 OF 2

013
- Check T3 and cabling to SCR 5.
- See Note 1.
- See Note 6.

014
Is at least +2.5 Vdc present at 01D-A1E1P11? (Drive signal for +12 V supply, YZ827, use CAUTION in probing this point.)
Y N

015
- Replace the frame sequence card at 01D-A1E1.
- If the problem still exists, replace the phase control card at 01D-A1A1 instead. (Refer to 'DC Voltage Measurement' on D-580.)
- See Note 1.
- See Note 6.

016
- Check diode 1 between 01A-TB1-1 and 14.
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- If the problem still exists, check 01F-CP3, 01F-L6 choke and SCRs instead (YZ886, sheet 5).
- Check circuit.
- See Note 1.
- See Note 6.

017
- Press POWER OFF.
- Disconnect the laminar bus lugs at 01A-TB1-1 and 01A-TB1-2 (YZ836).
- Reset 01F-CP3.
- Press POWER ON.

Does 01F-CP3 trip again?
Y N

J K

018
- Determine which lead causes the circuit protector to trip by powering up after replacing the laminar bus lugs one at a time.

CAUTION

- Isolate the short to a logic board by removing the laminar bus jumpers to each board. Before removing or reinstalling the laminar bus jumpers from/to a board, power must be off until the jumpers are all off/on. Otherwise, the current required by the board assembly could exceed the capacity of the board pins and burn them off.
- Isolate to a card by removing cards.
- See Notes 1 and 6.

019
- Press POWER OFF.
- Reconnect the laminar bus lugs at 01A-TB1-1 and 01A-TB1-2.
- Replace capacitor, 01F-C5 (YZ886, sheet 5).
  WARNING: Circuit damage may occur if power is applied with the capacitor disconnected.
- Reset 01F-CP3.
- Press POWER ON.

Does 01F-CP3 trip again?
Y N

020
- Return to normal operation.

021
- Check for a bad circuit protector, 01F-CP3.
- See Notes 1 and 6.

****

Note 1: Remove the jumper between pins 01D-A1C1M07 and 01D-A1C1P08.
Note 6: Remove the jumper between pins 01D-A1E1G12 and 01D-A1E1J08.

OVER-VOLTAGE

PAGE 1 OF 2

001
(Entry Point A)
- Press POWER OFF.
- Check the CBs for the failing power supply (YZ886, sheet 3 and 16).

Are any CBs tripped?
Y N

002
- Press POWER ON.

Does the 3705 power on now?
Y N

003
- Adjust the pot(s) on the phase control card at 01D-A1A1 to decrease the voltage on the supply(s) with the over-voltage (Refer to 'Checking SCRs' on D-560).
- Continue with MAPs if adjusting pot(s) does not fix the problem.
- Replace the frame sequence card at 01D-A1E1.
- Press POWER ON.

Does the 3705 power on now?
Y N

004
The frame sequence card was not the faulty component.

Are any over-voltage lights on at the 01D gate?
Y N

005
The over-voltage condition has disappeared.
- Check the LEDs on the 01D gate in the order listed below and go to the appropriate MAP:

(Refer to 'Checking SCRs' on D-560.)

LED Indicator	MAP
-4V OC1	2148
-4V U/V	2141
+6V U/V	2144
-12V U/V	2145
+12V U/V	2146
+5V U/V	2142
-5V U/V	2143

2 2
A B C D

C D MAP 2147-1

006
Is -5VDC or +5VDC over voltage light on?
Y N

007
- Replace the phase control card at 01D-A1A1. (Refer to 'DC Voltage Measurement' on D-580.)
- Press POWER ON.

Does the 3705 power on now?
Y N

008
The phase control card was not the faulty component.

Are any over-voltage lights on at the 01D gate?
Y N

009
The over-voltage condition has disappeared.
- Check the LEDs on the 01D gate in the order listed below and go to the appropriate MAP:

(Refer to 'Checking SCRs' on D-560.)

LED Indicator	MAP
-4V OC1	2148
-4V U/V	2141
+6V U/V	2144
-12V U/V	2145
+12V U/V	2146
+5V U/V	2142
-5V U/V	2143

010
- Check the voltage distribution for an intermittent loss of load (loose screws or connections).

011
The problem has been corrected by replacing the phase control card.

012
- Replace -5/+5 VDC regulator assembly.

013
The problem has been corrected by replacing the frame sequence card.

A B
1 1

OVER-VOLTAGE

PAGE 2 OF 2

014
The over-voltage condition has disappeared.
- Check the voltage distribution for an intermittent loss of load (loose screws or connections).

015
- Check the voltage distribution for an intermittent short.
- Check for faulty CBs.

OC1 INDICATOR

(-4VDC OVER CURRENT)

PAGE 1 OF 2

001
(Entry Point A)
- Press POWER OFF.
- Place a jumper between pins 01D-A1C1M07 and 01D-A1C1P08 (disables the 12 second timeout, master seq., YZ829).
- Place jumper between pins 01D-A1E1G12 and 01D-A1E1J08 (disables the 12 sec. Frame seq. T.O.) if not already present.
- Disconnect the Laminar Bus lugs at 01A-TB1-6, 7 and 8 (YZ836).
- Press POWER ON.

Does OC1 indicator turn on?
Y N

002
- Determine which lead causes the OC1 indication on the -4V supply by powering up after replacing the Laminar Bus lugs one at a time.

| CAUTION

- Isolate the short to a logic board by removing the Laminar Bus to each board. Before removing or reinstalling the Laminar Bus jumpers from/to a board, power must be off until the jumpers are all off/on. Otherwise, the current required by the board assembly could exceed the capacity of the board pins and burn them off.
- Isolate to a card by removing cards. Visually inspect the card for damage.
- Remove jumper between pins 01D-A1E1G12 and 01D-A1E1J08.
- Remove jumper between pins 01D-A1C1M07 and 01D-A1C1P08.

A

003
- Press POWER OFF.
- Reconnect the Laminar Bus lugs at 01A-TB1-6, 7 and 8 (YZ836).
- Disconnect the Laminar Bus lugs at 01A-TB1-9, 10, 11 and 13.
- Move yellow wire #60 from 01A-TB1-13 to 01A-W2-6 (temporary -4 volt sense connection).
- Press POWER ON.

Does OC1 indicator turn on?
Y N

004
- Determine which lead causes the OC1 indication on the -4V supply by powering up after replacing the Laminar Bus lugs one at a time.

| CAUTION

- Isolate the short to a logic board by removing the Laminar Bus to each board. Before removing or reinstalling the Laminar Bus jumpers from/to a board, power must be off until the jumpers are all off/on. Otherwise, the current required by the board assembly could exceed the capacity of the board pins and burn them off.
- Isolate to a card by removing cards. Visually inspect the card for damage.
- At completion of service procedure, move yellow wire #60 back to 01A-TB1-13 from its temporary connection at 01A-W2-6.
- Remove jumper between pins 01D-A1E1G12 and 01D-A1E1J08.
- Remove jumper between pins 01D-A1C1M07 and 01D-A1C1P08.

2
B

B
1

OC1 INDICATOR

(-4VDC OVER CURRENT)

PAGE 2 OF 2

005
- Replace Delta I card at 01D-A1F1.
- Replace frame sequence card at 01D-A1E1.
- Check that wire 122 goes to 01D-F1G03 and wire 115 goes to 01D-F1G08.
- Reconnect the Laminar Bus lugs at 01A-TB1-9, 10, 11 and 13 (YZ836).
- At completion of service procedure, move yellow wire #60 back to 01A-TB1-13 from its temporary connection at 01A-W2-6.
- Remove jumper between pins 01D-A1E1G12 and 01D-A1E1J08.
- Remove jumper between pins 01D-A1C1M07 and 01D-A1C1P08.

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Panel Line Test T3705L

WHAT IT DOES

Panel line test T3705L is a stand-alone version of the Network Control Program 4 (NCP4) line test function. This test is similar to the Emulation Program (EP) panel line test. This routine may be used when neither NCP nor EP is available to test the communication line using the IBM 3705 control panel. This test supports start-stop and BSC lines attached to the type 2 communication scanner. T3705L may be run using the 3705-80 RPL diskette or using OLTEP/OLTSEP and the type 1 or type 4 channel adapter.

This test is capable of:

- Sending characters continuously
- Addressing a terminal and looking for a valid response
- Polling a terminal and receiving data
- Originating an auto-call operation
- Handling an auto-answer operation

You have the responsibility for entering a line address, entering the set mode data, building a selection/polling control character scheme, and building a data stream for the test.

REQUIREMENTS

This test requires a dedicated IBM 3705-80 Communications Controller.

Configuration Data Set (CDS) Requirements:

RPL—No CDS required
CA1—Only channel data required (see the CDS section)

This test does not run under control of the diagnostic control monitor (DCM). Valid addresses must be entered for line testing.

CHANNEL ADAPTER LOAD PROCEDURE

1. Press RESET and then LOAD on the 3705.
2. Respond to the DEV/TEST/OPT request message at the host processor console with:

   r 01,'NSC/T3705L/NFE,EXT=nnny/'

DISPLAY registers A and B should equal X'FFFF' and the WAIT light should be on. Go to the run procedures below.

RPL DISKETTE LOAD PROCEDURE

1. Set the DISPLAY/FUNCTION SELECT switch to the STORAGE ADDRESS position. Set the STORAGE ADDRESS/REGISTER DATA switches to X'0AADD'.
2. Press RESET.
3. Press LOAD.
4. Press the panel INTERRUPT pushbutton.

Note: The IPL sequence should be active at this point. During IPL phase 3, ROS reads load program 1 (LPG1) from disk and passes control to LPG1. It is LPG1s function to determine the type of load being requested by way of the CE panel. LPG1 attempts to read the appropriate program from disk and to pass control to it. If errors occur while attempting to read either initial test or the IFT loader from disk, LPG1 defaults to a LPG2 load.

Normal run time for a ROS/LPG1/initial test/IFT disk loader is approximately 30 seconds. Because of error retries, there may be a 3-minute delay before an error stop occurs.

5. Are the DISPLAY registers A and B equal to X'FFFF'? If not, see the initial test symptom index. If the DISPLAY B data does not compare with any of the initial test routines, refer to the CTRL PNL section in Volume 2 and check out the CE panel test.

The TEST light should come on when the test is loaded and ready to be executed. Go to the run procedures below.

RUN PROCEDURES

1. Set the DISPLAY/FUNCTION SELECT switch to FUNCTION 1 to enter the test options.
2. Set STORAGE ADDRESS/REGISTER DATA switch B to 1 and press the INTERRUPT pushbutton. DISPLAY A should contain X'00F1'. Enter the line address to be tested as 0yyy (where *yyy* represents the desired line ABAR address), and press the START pushbutton.
3. DISPLAY A should contain X'00F2'. Enter the set mode data, LCD, and PCF turn character as follows, then press the START pushbutton.

STORAGE ADDRESS/REGISTER DATA SWITCHES

```
B   C     D    E
|   |     |    |
|   |     |    |-- PCF (turn character)
|   |     |       C = transmit turn RTS off
|   |     |       D = transmit turn RTS on
|   |     |--- LCD (see table)
|   |-------- Set mode data (see table)
```

Switches

B	*C*	*Description*
0	0	Select oscillator 0
0	1	Select oscillator 1
0	2	Select oscillator 2
0	3	Select oscillator 3
0	4	Data rate select
0	8	External clock
1	0	Synchronous clock
2	0	Data terminal ready
4	0	Diagnostic

Table of Set Mode Data:

Switch D	*Definition*
0	SS 9/6
1	Reserved
2	SS 8/5
3	Auto-call
4	SS 9/7
5	SS 10/7
6	SS 10/8
7	SS 11/8
8	Reserved
9	Reserved
A	Reserved
B	Reserved
C	BSC EBCDIC
D	BSC ASCII
E	Reserved
F	Feedback check

Table of LCDs: (type 2 communication scanner)

4. DISPLAY A should contain X'00F3'. Enter the control and SYN characters as follows:

	Switches B	C	D	E
Auto-call	2	0	x	x
Monitor RI	1	0	x	x
Duplex	0	8	x	x
Half-duplex	0	0	x	x

where *xx* represents a SYN character for BSC operation. DISPLAY A and DISPLAY B should display X'FFFF' if auto-call or duplex has not been specified.

Press the START pushbutton.

5. Do this step only if auto-call or duplex is specified in step 4. DISPLAY A should contain X'00F4'. Enter the auto-call line address. Press the START pushbutton.
6. Do this step only if auto-call or duplex is specified in step 4. DISPLAY A should contain X'00F5'. Enter the duplex receive line address. Press the START pushbutton.
7. DISPLAY A and DISPLAY B should contain X'FFFF'. Set the switches as follows:

```
          Switches
          B C D E

Init line 2 x x x
```

where *x* represents unused data.

Press the INTERRUPT pushbutton.

8. Set the switches as follows:

```
Switches
B C D E
4 0 x x  (Executes a set mode
          operation with data
          specified in step 3)
```

where *x* represents scan limit bits.

Press the INTERRUPT pushbutton.

9. Enter the test functions desired according to the following Test Functioncharts. If DISPLAY A and DISPLAY B contain X'0000', an invalid entry occurred.

TEST FUNCTION CHARTS

TEST FUNCTION CHART 1

Functions	ADDRESS/DATA Switches B and C	ADDRESS/DATA Switches D and E Input Data Byte	Descriptions
Transmit initial	42	None	Places the PAD/SYN character into the lines SDF and PDF and sets the PCF state to X'8'. When the PCF state goes to X'9', the PAD/SYN character is transmitted repeatedly.
Transmit test character and fill	43	Test character	Reads the test character from ADDRESS/DATA switches D and E and places it in the lines PDF. The line must be in transmit mode already (PCF state X'9'). The test character is transmitted once and the PAD/SYN character repeatedly thereafter.
Transmit test character and repeat	44	Test character	Reads the test character from ADDRESS/DATA switches D and places it in the lines PCF. The line must be in transmit mode already (PDF state X'9'). The test character is transmitted repeatedly.
Transmit test character and turn to receive	45	Test character	Reads the test character from ADDRESS/DATA switches D and E and places it in the lines PDF. The line must be in transmit mode already (PCF state X'9'). The test character is transmitted; then the line is turned around to the receive state. When the line begins to receive characters, the first 15 characters are stored in the LTS data buffers beginning with the second byte. The first byte contains the last character transmitted (the test character). If more than 15 characters are received, subsequent characters are overlapped into the last byte position of the data buffer.
Auto-answer (buffer 0/1 if reply)	46	0X digit	Performs set mode operation with 'data terminal ready' on. When someone dials in, a test is made for start-stop or BSC operation. For start-stop, PCF state X'7'(receive) is set. For BSC, state X'5' (monitor for phase) is set. When character phase is detected, state X'7' (receive) is set. If byte 1, bit 7 is 0 and the received compare character compares with one of the compare characters, the line is set to transmit mode and buffer 0 is transmitted. If bit 7 is 1, buffer 1 is transmitted.

Note: Display the LTS to see the data received. See "LTS Description" later in this section for the LTS format.

TEST FUNCTION CHART 2

Functions	ADDRESS/DATA Switches B and C	ADDRESS/DATA Switches D and E Input Data Byte	Descriptions
Dial digit	47	0X digit	Loads the dial digit from ADDRESS/DATA switch E into a 16-position buffer. The last digit loaded must be X'F'. X'F' indicates the end of the dial digits.
Dial operate (buffer 0/1 if reply)	48	YX digit	Transmits dial digits previously loaded to the auto-call unit. If switch position E is 0, the dial digits are transmitted to the auto-call unit; if nonzero, the sequence ends after the number of dial digits specified in E has been transmitted. When the dial is completed, the line is put in receive mode. If byte 1, bit 3 is 0 and a received character compares with one of the compare characters, the line is set to transmit mode and buffer 0 is transmitted. If bit 3 is 1, buffer 1 is transmitted.
Data rate	49	FF=high rate 00=low rate	Selects the high or low data rate for a line previously defined in test.
Receive mode	4A	None	Places the line in receive mode and places the first character received in the first position of the data buffer. If more than 16 characters are received, subsequent characters overlap into the last byte position of the data buffer.
Change PCF turn character	4B	Turn character	Changes the PCF turn character to the value set in ADDRESS/DATA switch E. Switch D should be set to 0.
Display LTS	4C	Displacement into LTS	Displays 2 half-words of the line test control block (LTS) beginning at the displacement specified in ADDRESS/DATA switches D and E. See "LTS Description" later in this section for the the LTS format.
Transmit buffer 0 or 1	4F	E - 0 (buffer 0) E - 1 (buffer 1)	The line is set to transmit mode (PCF state X'8'). When PCF state X'8' goes to PCF state X'9', buffer 0 is transmitted if byte 1, bit 7 is 0. If bit 7 is 1, buffer 1 is transmitted. When the corresponding transmit end compare character is detected, the line is turned around to receive mode.
End test	50	0x digit	If byte 1, bit 7 is 0, the test is ended, the line test control block (LTS) is cleared, and the line is placed in a no-op state (drops DTR and resets options selected by set mode). If bit 7 is 1, the line remains enabled (DTR active).

TEST FUNCTION CHART 3

Functions	ADDRESS/DATA Switches B and C	ADDRESS/DATA Switches D and E Input Data Byte	Descriptions
Load buffer 0	51	XX digit	The character in switches D and E is stored in a 40-character buffer. Leading PADs and SYNs must be inserted for the type 3 communication scanner (T3CS) also, due to the use of PCF state 'E' during the transmit operation.
Load buffer 1	52	XX digit	Same as Load buffer 0 except the character is stored in buffer 1.
Load receive compare character 1	53	XX digit	The character in switches D and E is stored as the first receive compare character.
Load receive compare character 2	54	XX digit	Same as Load receive compare character 1 except the character is stored as the second receive compare character.
Load receive compare character 3	55	XX digit	Same as Load receive compare character 1 except the character is stored as the third receive compare character.
Load swap transmit buffer 0 compare character	56	XX digit	The character in switches D and E (XX) is stored as the swap transmit buffer 0 compare character.
Load swap transmit buffer 1 compare character	57	XX digit	Same as Load swap transmit buffer 0 compare character except the character is stored as the swap transmit buffer 1 compare character.
Initialize buffer 0 offset	58	XX digit	Sets in the LTS the displacement (normally X'00') into the appropriate buffer at which the storing of data entered through the panel is to begin. As the data is subsequently entered, a count of the data characters is accrued; this count is then used by the transmit routine to determine when the line should be placed into receive mode.

TEST FUNCTION CHART 4

Functions	ADDRESS/DATA Switches B and C	ADDRESS/DATA Switches D and E Input Data Byte	Descriptions
Initialize buffer 1 offset	59	XX digit	Same as function 58 except the displacement is for buffer 1.
BSC cyclic redundancy check (CRC) accumulation buffer 0/1	5A	00 (for buffer 0) 01 (for buffer 1)	Accumulates the CRC characters for BSC data (to be transmitted) as it is entered into either buffer 0 or buffer 1.
Set receive mode byte	5C	Setting dependent on option selected (see Descriptions column)	Allows the selection of certain options by setting a control byte in the LTS (line test control block). Bit 3 indicates that the option of checking for 2 special characters (set by subfunctions 53 and 54) in sequence in a received data stream is to be used by the panel line test function to determine when the line being tested should be placed into transmit mode. Bit 6 of the control byte indicates that CRC character accumulation is to be performed on BSC data during receive operations. Bit 7 gives the same indication for SDLC data.

DEFINITION OF DISPLAY A AND DISPLAY B DURING TEST

Control Panel Display Output

Bits	Byte X 6	7	Byte 0 0123 4567	Byte 1 0123 4567
DISPLAY A	0	0	xxxx xxxx	xxxx xxxx
ICW Bits	0	0	0-7	8-15
ICW Fields	0	0	SCF	PDF
DISPLAY B	0	0	xxxx xxxx	xxxx xxxx
ICW Bits	0	0	16-23	
ICW Fields			LCD PCF	DS Leads

Data Set Leads Display

BYTE 1 Bit	Data Line	BYTE 1 Bit	*Auto-call
0	Clear to send	0	Abandon call and retry
1	Ring indicator	1	Present next digit
2	Data set ready	2	Data line occupied
3	Receive line signal	3	Digit present
4	Receive data bit buffer	4	Call request
5	Diagnostic wrap mode	5	Call originating status
6	Bit service request	6	Bit service request
7	Zero (not used)	7	Interrupt remember

* The LCD displays a X'3' (auto-dial) when the DS leads display dial line information.

LTS Description (Hex is LTS displacement value)

HEX	FIELD DESCRIPTIONS	
00	LTSCTL: Control byte.	LTSPDSYN: PAD or SYN character for this line.
02	LTSSTMD: The system-generated set mode SDF.	LTSLCD: The system-generated LCD value.
04	LTSXLAD: The line address of the line being tested.	
06	LTSRLAD: Duplex receive line address.	
08 0A 0C 0E 10 12 14 16	LTSDIALL: Buffer for receive data characters or auto-call dial digits. This is the receive buffer for a type 2 communication scanner and the address of the receive buffer for a type 3 communication scanner.	
18	LTSNFCNT: Counter for non-X'FF' data characters when receiving.	
1A	LTSN0CNT: Counter for non-X'00' data characters when receiving.	
1E	LTSDCNT: Counter for auto-call dial digits and receive data characters.	LTSTURN: Transmit turn LCD/PCF.
20	LTSACLN: Auto-call line address.	
22	LTSXL2: Transmit level 2 pointer.	
24	LTSRL2: Receive level 2 pointer.	
26	LTSDATAP: Transmit buffer pointer.	
28	LTSRCC1: Receive compare character 1.	LTSRCC2: Receive compare character 2.
2A	LTSRRC3: Receive compare character 3.	LTSWAP1: Swap transmit buffer 0 compare character.
2C	LTSWAP2: Swap transmit buffer 1 compare character.	LTSXEND0: Buffer 0 transmit end compare character.

TEST EXAMPLES

Write Data to IBM 2770 (BSC Lines)

Step	Functions	ADDRESS/ DATA Switches B C D E	Action Required	Descriptions
1	Initialize buffer 0	5 8 0 0	Press INTERRUPT	Sets initial buffer 0 offset.
2	Initialize buffer 1	5 9 0 0	Press INTERRUPT	Sets initial buffer 1 offset.
3	Load buffer 0	5 1 x x*	Press INTERRUPT	Loads buffer 0 with address sequence.
4	Load buffer 1	5 2 x x**	Press INTERRUPT	Loads buffer 1 with address sequence.
5	Accumulate CRC	5 A 0 1	Press INTERRUPT	Accumulates and stores CRC in buffer 1.
6	Set compare character 1	5 3 3 D	Press INTERRUPT	Sets receive compare character 1.
7	Set swap character 1	5 6 6 1	Press INTERRUPT	Sets first swap character.
8	Set swap character 2	5 7 7 0	Press INTERRUPT	Sets second swap character.
9	Transmit initial	4 2 0 0	Press INTERRUPT	Sets transmit state.
10	Transmit buffer 0	4 F 0 0***	Press INTERRUPT	Transmits from buffer 0.
11	End test	5 0 0 1	Press INTERRUPT	Ends the test.

* xx= X'FF', X'AA', X'32', X'32, X'37', X'FF', X'FF', X'AA', X'32', X'32', addr, X'2D', X'FF'.

** xx= X'FF', X'FF', X'AA', X'32', X'32', X'02', X'E3', X'C5', X'E2', X'E3', X'40', X'C2', X'D3', X'D6', X'C3', X'D2', X'15', X'03'.

*** TEST BLOCK should print out repeatedly on the terminal until step 11 ends the test.

Read from an IBM 2770 and Accumulate Cyclic Redundancy Check (CRC)

Step	Functions	ADDRESS/ DATA Switches B C D E	Action Required	Descriptions
1			Enter data at the terminal and press the REQUEST key.	
2	Initialize buffer 0	5 8 0 0	Press INTERRUPT	Sets offset for buffer 0.
3	Load buffer 0	5 1 x x*	Press INTERRUPT	Loads buffer 0 with the polling sequence.
4	Set receive mode	5 C 0 2	Press INTERRUPT	Sets receive mode byte to BSC accumulation on receive.
5	Transmit initial	4 2 0 0	Press INTERRUPT	Sets transmit state.
6	Transmit buffer 0	4 F 0 0**	Press INTERRUPT	Transmits from buffer 0.
7	End test	5 0 0 0	Press INTERRUPT	

* xx = X'FF', X'AA', X'32', X'32', X'FF', X'FF', X'AA', X'32', X'32', addr, addr, X'F0', X'2D', X'FF'

** If data is received properly and the CRC is correct, the line turns around, transmits buffer 0 again, and goes into receive mode. The terminal times out.

Read Data with a Two-Character Compare

Step	Functions	ADDRESS/ DATA Switches B C D E	Action Required	Descriptions
1			Enter ABCD1234 at the terminal and press the REQUEST key.	
2	Initialize buffer 0	5 8 0 0	Press INTERRUPT	Sets buffer 0 offset.
3	Load buffer 0	5 1 x x*	Press INTERRUPT	Loads buffer 0 with the poll sequence.
4	Set receive mode	5 C 1 0	Press INTERRUPT	Sets two-character compare on receive.
5	Set first compare character	5 3 C 4	Press INTERRUPT	Stores first receive compare character.
6	Set second compare character	5 4 F 1	Press INTERRUPT	Stores second receive compare character.
7	Transmit initial	4 2 0 0	Press INTERRUPT	Sets transmit mode.
8	Transmit buffer 0	4 F 0 0**	Press INTERRUPT	Transmits from buffer 0.
9	Display LTS	4 C 0 8 4 C 1 2***	Press INTERRUPT	Displays received data.
10	End test	5 0 0 0	Press INTERRUPT	Ends the test.

* xx = X'AA', X'32', X'32', X'37', X'FF', X'FF', X'AA', X'32', X'32', addr, addr, X'F0', X'2D' X'FF'.

** If the data is received properly, the line turns around, transmits buffer 0 again, and goes into receive mode. The terminal times out.

*** The last received data character should be X'F1'.

Address an IBM 1050 (S/S Terminal) Using Buffers 0 and 1

Step	Functions	ADDRESS/ DATA Switches B C D E	Action Required	Descriptions
1	Initialize buffer 0	5 8 0 0	Press INTERRUPT	Sets initial buffer 0 offset.
2	Initialize buffer 1	5 9 0 0	Press INTERRUPT	Sets initial buffer 1 offset.
3	Load buffer 0	5 1 F F	Press INTERRUPT	Loads the PAD character X'FF' in buffer 0.
4	Load buffer 0	5 1 F F	Press INTERRUPT	Loads the second PAD character X'FF' in buffer 0.
5	Load buffer 0	5 1 7 C	Press INTERRUPT	Loads a circle C character into buffer 0.
6	Load buffer 0	5 1 A 3	Press INTERRUPT	Loads the terminal address X'A3' into buffer 0.
7	Load buffer	5 1 2 0	Press INTERRUPT	Loads the component select address X'20' into buffer 0.
8	Load buffer 1	5 2 F F	Press INTERRUPT	Loads the PAD character X'FF' into buffer 1.
9	Load buffer 1	5 2 3 4	Press INTERRUPT	Loads the end-of-address character X'34' into buffer 1.
10	Load buffer 1	5 2 X X	Press INTERRUPT	Loads data character X'xx' into buffer 1.
11	Load buffer 1	5 2 5 E	Press INTERRUPT	Loads a circle B character X'5E' into buffer 1.
12	Load buffer 1	5 2 y y	Press INTERRUPT	Loads longitudinal redundancy check (LRC) character X'yy' into buffer 1. If the same data character is entered an even number of times in step 10, the LRC is a circle B, which can be entered for X'yy'.
13	Load buffer 1 swap compare character	5 7 3 7	Press INTERRUPT	Loads the swap compare character for buffer 1. If the response from the terminal is X'37', after buffer 0 is transmitted, the line is turned around and buffer 1 is transmitted.
14	Transmit	4 F 0 0	Press INTERRUPT	Transmits buffer 0.

Notes:

1. After step 11 is executed, buffer 0 is transmitted to the address of the IBM 1050 terminal. The line is set to receive mode. If the terminal responds with a circle Y (X'37'), the line is set to transmit mode and buffer 1 is transmitted.
2. ADDRESS/DATA switch A is always set to X'0'.

Send to and Receive from a S/S Terminal (IBM 2741 or IBM 3767)

Step	Functions	ADDRESS/ DATA Switches B C D E	Action Required	Descriptions
1	Initialize buffer 0	5 8 0 0	Press INTERRUPT	Sets initial buffer 0 offset.
2	Load buffer 0	5 1 x x*	Press INTERRUPT	Loads data into buffer 0.
3	Set compare character 1	5 3 7 C	Press INTERRUPT	Sets receive compare character 1.
4	Transmit buffer 0	4 F 0 0	Press INTERRUPT	Transmits buffer 0.

* xx = X'FF', X'AA', X'34', X'1F', X'54', X'20', X'10', X'70', X'08', X'68', X'58', X'38', X'04', X'64', X'6D', X'7C', X'FF'.

0123456789 should print out on the terminal and the terminal go into transmit mode. Key a message into the IBM 2741 and send it to the IBM 3705. The IBM 3705 should send 0123456789. This sequence can be repeated until the test is terminated.

ERROR STOPS

Error stops that may occur in the panel line test are indicated in DISPLAY A and DISPLAY B. See the following list for a description of the stops and recovery actions required:

DISPLAY A	*DISPLAY B*	*Description*
80FC	80FC	An unexpected level 4 interrupt occurred; only PCI-level interrupts are expected. register X'15' contains the results of an input X'7F' instruction executed when the interrupt occurred. To recover from this stop, the program must be reloaded.
80FE	80FE	An unexpected level 1 interrupt occurred. Register X'01' contains the ORed results of an input X'7E' and an input X'76' instruction executed when the interrupt occurred. If bits 0.1, 0.2, 0.3, or 0.4 are on, a communication scanner level 1 interrupt occurred; pressing the START pushbutton causes the program to attempt a scanner reset and to restart. If none of these bits are on, another type of level 1 interrupt occurred, and the program must be reloaded.
80FF	xxxx	A program or hardware failure caused a branch to storage location X'00000'. DISPLAY B contains the address of the instruction causing the branch. To recover, the program must be reloaded.

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