Enterprise Systems Architecture/390
COMPARE AND SWAP AND PURGE Instruction

┌─── Note: ──┐
│   │
│ Before using this information and the product it supports, be sure to read the general information under "Notices" on page iii. │
│   │
└──┘

April 2000

The facility discussed in this publication is available on the IBM S/390 Parallel Enterprise Server. The information published herein should not be construed as implying any intention by IBM to provide these facilities on models other than those described herein.

This publication is provided for use in conjunction with other relevant IBM publications, and IBM makes no warranty, express or implied, relative to its completeness or accuracy. The information in this publication is current as of its publication date but is subject to change without notice.

Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product is not intended to state or imply that only IBM's product may be used. Any functionally equivalent product may be used; however, this does not constitute a waiver in any way of IBM's intellectual property rights.

IBM may have patents or pending patent applications covering subject matter described herein. Furnishing this publication does not constitute or imply a grant of any license under any patents, patent applications, trademarks, copyrights, or other rights of IBM or of any third party, or any right to refer to IBM in any advertising or other promotional or marketing activities. IBM assumes no responsibility for any infringement of patents or other rights that may result from the use of this publication or from the manufacture, use, lease, or sale of apparatus described herein.

Licenses under IBM's utility patents are available on reasonable and nondiscriminatory terms and conditions. Inquiries relative to licensing should be directed, in writing, to:

International Business Machines Corporation
IBM Director of Licensing
500 Columbus Avenue
Thornwood, New York 10594
U.S.A.

Trademarks

The following terms used in this publication are trademarks of the International Business Machines Corporation in the United States or other countries:

Enterprise Systems Architecture/390
ESA/390
IBM
S/390 Parallel Enterprise Server

Preface

This publication describes the COMPARE AND SWAP AND PURGE instruction, also known as the broadcasted-purging facility, of the Enterprise Systems Architecture/390 (ESA/390).[1]

This publication is informal and not orderable through PUBORDER. The publication contains information that will be placed in the next version, version -07, of *Enterprise Systems Architecture/390 Principles of Operation,* SA22-7201.

Terms and concepts referred to in this publication but explained in the aforementioned publication are not explained again in this publication.

---

[1] Enterprise Systems Architecture/390 and ESA/390 are trademarks of the International Business Machines Corporation.

COMPARE AND SWAP AND PURGE Instruction

Name	Mne-monic	Characteristics						Op Code
COMPARE AND SWAP AND PURGE	CSP	RRE C	P A¹ SP	$		R ST	R₂	B250

Explanation:

$	Causes serialization.
A¹	Access exceptions; not all access exceptions may occur; see instruction description for details.
C	Condition code is set.
P	Privileged-operation exception.
R	PER general-register-alteration event.
R₂	R₂ field designates an access register in the access-register mode.
RRE	RRE instruction format.
SP	Specification exception.
ST	PER storage-alteration event.

Figure 1. Summary of Control Instructions

COMPARE AND SWAP AND PURGE

CSP   R₁,R₂   [RRE]

'B250'	////////	R₁	R₂
0	16	24	28 31
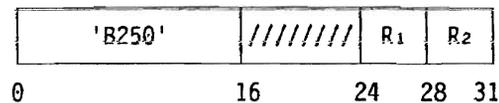
The first and second operands are compared. If they are equal, the contents of general register R₁ + 1 are stored at the second-operand location, and a purging operation is performed. If they are unequal, the second operand is loaded into the first-operand location. The result of the comparison is indicated in the condition code.

Bits 16-23 of the instruction are ignored.

The first operand is the contents of general register R₁. The second operand is a word in storage. The location of the leftmost byte of the second operand is designated by the contents of general register R₂.

The purging operation applies to ART-lookaside buffers (ALBs) and translation-lookaside buffers

(TLBs) in all CPUs in the configuration. Either ALBs or TLBs, or both ALBs and TLBs, may be selected for purging. All entries are cleared from the selected buffers.

The purging operation is specified by means of bits 30 and 31 of general register R₂. When bit 30 is one, entries are cleared from ALBs. When bit 31 is one, entries are cleared from TLBs. When bits 30 and 31 both are ones, entries are cleared from ALBs and TLBs. When bits 30 and 31 both are zeros, no entries are cleared.

The handling of the address in general register R₂ is dependent on the addressing mode. In the 24-bit addressing mode, the contents of bit positions 8-29 of general register R₂, with two zeros appended on the right, constitute the address, and the contents of bit positions 0-7 are ignored. In the 31-bit addressing mode, the contents of bit positions 1-29 of general register R₂, with two zeros appended on the right, constitute the address, and the contents of bit position 0 are ignored.

The contents of the registers just described are shown in Figure 2 on page 2.

```
R₁    ┌──────────────────────────────────────┐
      │           First Operand              │
      └──────────────────────────────────────┘
      0                                    31


R₁ + 1 ┌──────────────────────────────────────┐
       │             Swap Value              │
       └──────────────────────────────────────┘
       0                                    31

       24-Bit Addressing Mode

R₂    ┌──────────┬───────────────────┬───┬───┐
      │ //////// │ Second-Operand Adr.│ A │ T │
      └──────────┴───────────────────┴───┴───┘
      0          8                  30  31

       31-Bit Addressing Mode

R₂    ┌──┬───────────────────────────┬───┬───┐
      │ /│  Second-Operand Address   │ A │ T │
      └──┴───────────────────────────┴───┴───┘
      0  1                          30  31
```
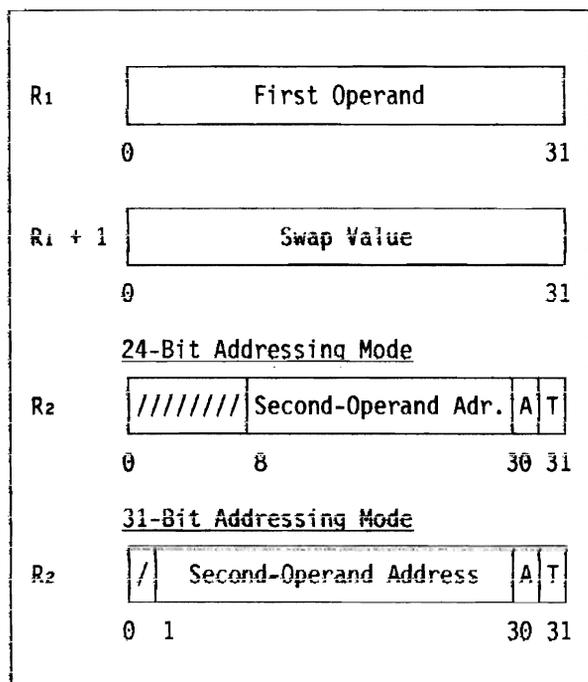
Figure 2. Register Contents for COMPARE AND SWAP AND PURGE

When an equal comparison occurs, the contents of general register $R_1 + 1$ are stored at the second-operand location. The fetch of the second operand for purposes of comparison and the store into the second-operand location appear to be a block-concurrent interlocked-update reference as observed by other CPUs.

When the result of the comparison is unequal, the second-operand location remains unchanged. However, on some models, the value may be fetched and subsequently stored back unchanged at the second-operand location. This update appears to be a block-concurrent interlocked-update reference as observed by other CPUs.

A serialization function is performed before the operand is fetched and again after the operation is completed.

When an equal comparison occurs, this CPU clears entries from its ALB and TLB, as specified

by bits 30 and 31 of general register R_2, and signals all CPUs in the configuration to clear the same specified entries from their ALBs and TLBs. The ALB entries that are cleared are all ALB access-list designations, access-list entries, ASN-second-table entries, and authority-table entries. The TLB entries that are cleared are all TLB segment-table entries and page-table entries.

The execution of COMPARE AND SWAP AND PURGE is not completed on the CPU which executes it until (1) all specified entries have been cleared from the ALB and TLB on this CPU and (2) all other CPUs in the configuration have completed any storage accesses, including the updating of the change and reference bits, by using the specified ALB and TLB entries.

Special Conditions

The R_1 field must designate an even register; otherwise, a specification exception is recognized.

Resulting Condition Code:

0   First and second operands equal, second operand replaced by contents of general register $R_1 + 1$

1   First and second operands unequal, first operand replaced by second operand

2   --

3   --

Program Exceptions:

* Access (fetch and store, operand 2)
* Privileged operation
* Specification

Programming Note: COMPARE AND SWAP AND PURGE provides a broadcast form of the PURGE ALB and PURGE TLB instructions, thus making it possible to avoid uses of SIGNAL PROCESSOR.

End of Document