IBM Customer Engineering

Manual of Instruction

1620 Data Processing System

Floating Point Feature

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IBM

Customer Engineering Manual of Instruction
1620 Data Processing System
Floating Point Feature

This edition, Form 227-5630-1, incorporates major changes to Form R27-5630-0. The latter form is made obsolete by these changes.

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Contents

Preface

This manual is intended to be used in conjunction with the *Customer Engineering Manual of Instruction, 1620 Data Processing System* (Form 227-5647), and the *Customer Engineering Instructional System Diagrams, 1620 Data Processing System* (Form 227-5631). Complete explanations of the basic 1620 operation code functions are given in the Instruction Manual. Function charts and system diagrams for the basic 1620 as well as for the Floating Point feature are included in the Instructional System Diagrams.

Automatic Floating Point Operations (Special Feature)

The Automatic Floating Point Operations special feature provides the IBM 1620 Data Processing System with the ability to do floating point arithmetic by using floating point instructions, instead of the subroutines heretofore necessary.

The addition of automatic floating point operations can increase the computing power of the 1620 System 50 to 100 per cent, depending on the amount of floating point computations required. Up to 15 per cent of the basic 1620 core storage capacity can be saved through the elimination of subroutines and call sequence instructions associated with floating add, floating subtract, floating multiply, and floating divide.

Automatic Division (special feature) is a prerequisite to the installation of floating point operations.

Description

Floating Point Arithmetic

Scientific and engineering computations frequently involve lengthy and complex calculations in which it is necessary to manipulate numbers that may vary widely in magnitude. To obtain a meaningful answer, problems of this type usually require that as many significant digits as possible be retained during calculation and that the decimal point always be properly located. When applying such problems to a computer, several factors must be taken into consideration, the most important of which is the decimal point location.

Generally speaking, a computer does not recognize the decimal point present in any quantity used during the calculation. Thus, a product of 414154 will result regardless of whether the factors are 9.37×44.2, $93.7 \times .442$, or 937×4.42, etc. It is the programmer's responsibility to be cognizant of the decimal point location during and after the calculation and to arrange the program accordingly. In the operation of addition, for example, the decimal point of all numbers must be lined up to obtain the correct sum. To facilitate this arrangement, the programmer must shift the quantities as they are added. In the manipulation of numbers that vary greatly in magnitude, the resulting quantity could conceivably exceed allowable working limits.

The processing of numbers expressed in ordinary form, for example, 427.93456, 0.0009762, 5382, —623.147, 3.1415927, etc., can be accomplished on a computer only by extensive analysis to determine the size and range of intermediate and final results. This analysis and subsequent number scaling frequently takes longer than the actual calculation. Furthermore, number scaling requires complete and accurate information concerning the boundaries of all numbers that come into the computation (input, intermediate, output). Since it is not always possible to predict the size of all numbers in a given calculation, analysis and number scaling is sometimes impractical.

To alleviate this programming problem, a system must be employed in which information regarding the magnitude of all numbers accompanies the quantities in the calculation. Thus, if all numbers are represented in some standard, predetermined format which instructs the computer in an orderly and simple fashion concerning the location of the decimal point, and if this representation is acceptable to the routine doing the calculation, then quantities which range from minute fractions having many decimal places to large whole numbers having many integer places can be handled. The arithmetic system most commonly used, in which all numbers are expressed in a format having the feature just described, is called "floating point arithmetic."

The notation used in floating point arithmetic is basically an adaptation of the scientific notation widely used today. In scientific work, very large or very small numbers are expressed as a number, between one and ten, times a power of ten. Thus 427.93456 is written as 4.2793456×10^{2} and 0.0009762 as 9.762×10^{-4}. In the 1620 floating point arithmetic system, the range of numbers is modified to extend between .1 and .99999999, that is, the decimal point of all numbers is placed to the left of the high-order (leftmost) nonzero digit. Hence, all quantities may be thought of as a decimal fraction times a power of ten, for example, 427.93456 as $.42793456 \times 10^{3}$ and 0.0009762 as $.97620000 \times 10^{-3}$. In addition to the advantages inherent in scientific notation, the use of floating point numbers during processing eliminates the necessity of analyzing the operations to determine the positioning of the decimal point in intermediate and final results since the decimal point is always immediately to the left of the high-order nonzero digit in the fraction.

1620 Automatic Floating Point Operations

In 1620 automatic floating point operations, a floating point number is a field consisting of a variable length fraction (F) and a 2-digit exponent (E). The exponent is in the two low-order positions of the field, and the fraction is in the remaining high-order positions, as shown:

$$\bar{F} \ldots . F\bar{E}E$$

The fraction must have a minimum of two digits and can have any number to a maximum of 100 digits. However, when two fields are operands, that is, quantities being added, subtracted, multiplied, or divided, they must have fractions of the same length. The extremity of the field is marked by a flag over the high-order digit.

NOTE: The term "mantissa" is often used instead of the term "fraction." Both terms are used synonymously to differentiate between significant digits and their associated exponent.

The exponent is established on the premise that the fraction is less than 1.0 and equal to or greater than 0.1. The exponent is always two digits and has a range of −99 to +99. It is defined by a flag over the high-order (tens) digit.

The fraction and the exponent each have an algebraic sign represented by a flag in the units position if negative, and by the absence of a flag in the units position if positive. A floating point number with a negative fraction and a negative exponent is represented as follows:

$$\bar{F} \ldots . \bar{F}\bar{E}\bar{E}$$

Sign control of the results of all computations is maintained according to the standard rules of arithmetic operations.

Operation

In descriptions of instructions and operations, the following symbols are used for clarity and brevity:

PF	=	fraction in the field at the P address
QF	=	fraction in the field at the Q address
PE	=	exponent in the field at the P address
QE	=	exponent in the field at the Q address
L	=	number of digits in the fraction
d	=	PE − QE

In all floating point numbers, the decimal point is assumed to be at the left of the high-order digit, which must not be zero. Such a number is "normalized." When a number has one or more high-order zeros, it is considered to be "unnormalized." An unnormalized number that results from a floating point computation is normalized automatically, but unnormalized terms are not recognized as such when entered as data. They will be processed, but correct results cannot be assured. Therefore, it is necessary to enter all data in normalized form. For example, the number $\bar{0}682349\bar{4}05$ should be entered as $\bar{6}823494\bar{0}04$, assuming the fixed point number is 6823.494, and an 8-digit fraction is required.

Instructions

Eight floating point instructions are provided (Figure 1-1). Four are for arithmetic computations; floating add, floating subtract, floating multiply, and floating divide; three control the field size and location: floating shift right, floating shift left, and transmit floating. The eighth instruction provides for branch and transmit in floating point operations. All instructions are in the 1620 format and contain a 2-digit op code, a 5-digit P address, and a 5-digit Q address.

With the exception of floating shift right and floating shift left, the P address and Q address of floating point fields are the addresses of the low-order positions of the exponents.

Within the description of each instruction, the operation of the computer in aligning decimal points, normalizing results, etc., is described as an aid for the Customer Engineer in checking program logic and trouble shooting. These operations are automatic and need not be programmed. Notice particularly that floating divide requires only one instruction: the dividend is positioned, division is accomplished, and the quotient is transmitted to the P field without further command.

Floating point operations conform to the basic 1620 operating concepts regarding the execution of a multiply or divide operation following a save key operation, in that a floating multiply or divide operation executed after a save key operation will destroy the address saved in PR-1.

Zero Fraction

When a floating point computation results in a zero fraction, or if an exponent, <−99, is developed, a special floating point zero (machine zero) is created in the form $\bar{0}0 \ldots . 0\bar{9}\bar{9}$, which is the smallest positive

Floating Add	FADD	01
Floating Subtract	FSUB	02
Floating Multiply	FMUL	03
Floating Divide	FDIV	09
Floating Shift Left	FSL	05
Transmit Floating	TFL	06
Branch and Transmit Floating	BTFL	07
Floating Shift Right	FSR	08

Figure 1-1. Floating Point Operation Codes and Mnemonics

quantity that can be represented. A zero fraction or exponent, <-99, causes the equal/zero indicator (12) to be turned on. Zeros entered as data should be in the floating point zero form. Zero quantities in other forms, for example, $\bar{0}0 \ldots 0\bar{0}0$, will be processed but results cannot be assured.

Indicators

The four indicators associated with automatic floating point operations are represented by lights on the 1620 console. The light for each indicator is turned on when the corresponding indicator is turned on. The high/plus and equal/zero lights are located in the Control Gates section of the console, and the arithmetic overflow check and exponent check lights and switch are in the Indicator Displays and Switches section.

HIGH/PLUS (INDICATOR CODE 11)

The high/plus indicator and light are turned on when the fraction resulting from a floating point computation is greater than zero.

EQUAL/ZERO (INDICATOR CODE 12)

The equal/zero indicator and light are turned on to indicate a zero fraction resulting from a floating point computation.

ARITHMETIC OVERFLOW CHECK (INDICATOR CODE 14)

During floating point operations, the overflow check indicator is turned on when division by zero is attempted. Division by an unnormalized number may result in an incorrect quotient because of an incorrectly positioned divisor.

EXPONENT CHECK (INDICATOR CODE 15)

The exponent check indicator is turned on by an exponent overflow or underflow.

Exponent Overflow. When an exponent greater than +99 is generated, the fraction is set to 9s. The sign is determined by the computed result that caused the overflow. The exponent is set to +99, which is the largest floating point number ($\bar{9}9 \ldots 9\bar{9}9$) that can be represented in the floating point format. If the generated fraction is positive, the H/P indicator (11) is also turned on.

Exponent Underflow. When an exponent less than −99 is generated, the fraction is set to +0s and the exponent is set to −99 (machine zero). This is the smallest floating point number ($\bar{0}0 \ldots 0\bar{9}\bar{9}$) that can be represented in the floating point format. The E/Z indicator (12) is also turned on.

An exponent underflow is not indicated when one or both operands are zero.

When the exponent check indicator (15) is turned on, program operation is controlled by the console overflow check switch, which is also connected to the overflow check indicator (14). Functions of the console switches are described in the CE Manual of Instruction (Form 227-5647). The exponent check indicator (15) is turned off by programmed interrogation or by depression of the 1620 reset key.

Mode Latches

The floating point feature makes use of the basic operations of the 1620, for example, add, subtract, compare, multiply, load dividend, divide, and transmit. Various combinations of these basic 1620 operations are obtained with the use of "mode latches" which perform essentially the same control functions as the op lines from the operation register. At the end of a given mode operation, the mode latch for the next operation is turned on, thus passing the control of one operation on to the next until the entire floating point function is completed.

I Cycle Entry Modification

The output of the I cycle entry point OR (01.15.05.1) is ANDed with *−S 0 DEC OPR TENS*. As long as the operation register tens position contains a zero, most of the I cycle entry points are prevented from initiating an I cycle. The exceptions which can initiate an I cycle are: FP exit, divide overflow, or the I/O exit trigger ON.

1620 Central Processing Unit (CPU)

Basic Console

Two new lights were added to the Control Gates section of the basic console to indicate the status of the underflow/equal zero (UNFLO/ZERO) and the floating point exit (FP EXIT) latches.

The exponent check (EXP CHK) status light was added to the O'FLOW check switch. When the exponent check latch is turned on, the computer continues to operate or stops, depending on the setting of the console check switch associated with the exponent check latch. See Figure 1-2.

Auxiliary CE Console

An auxiliary console (Figure 1-3) is provided with the floating point feature. The console contains thirty lights to display the on/off status of various mode and auxiliary latches associated with floating point operations.

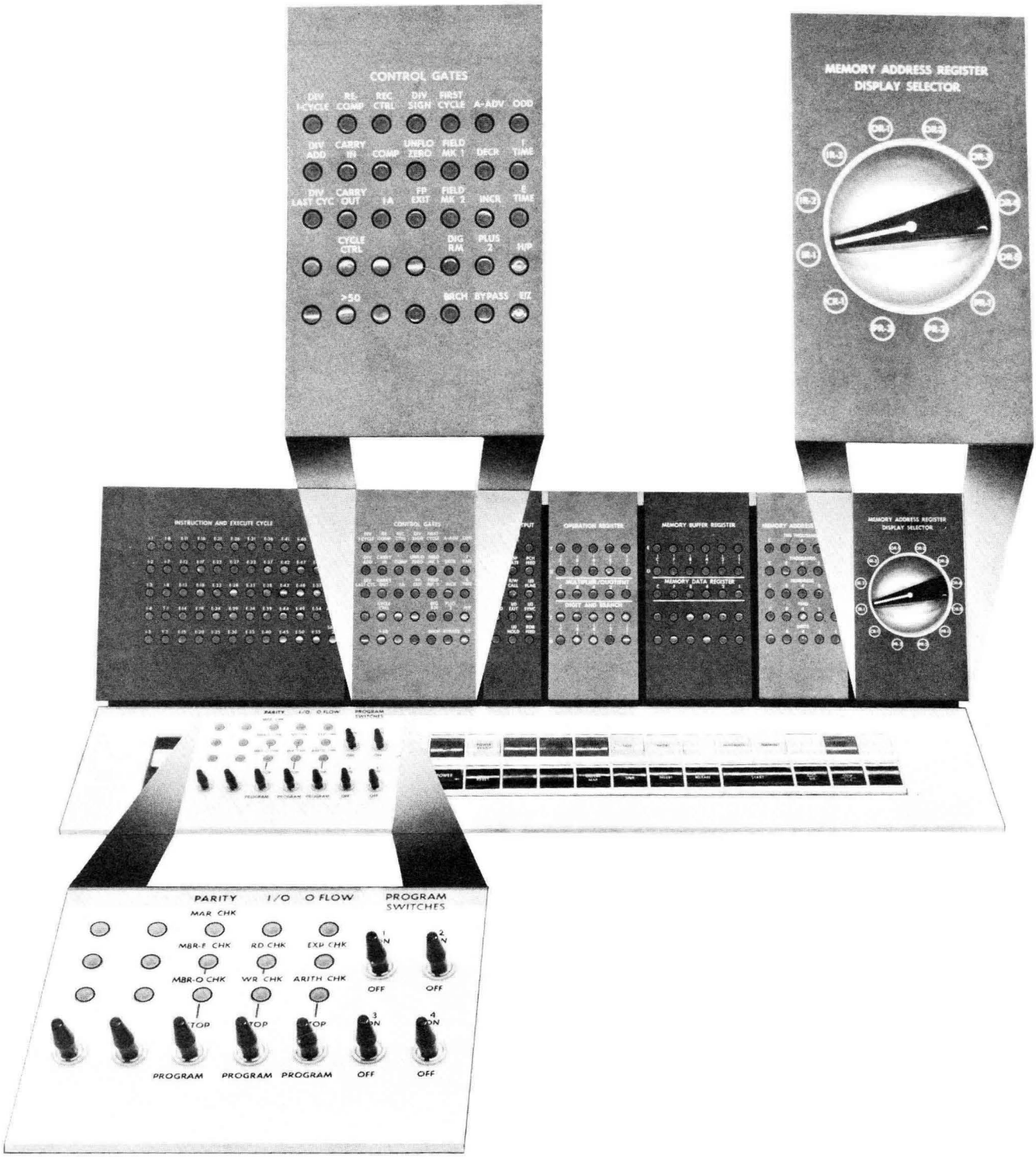


Figure 1-2. 1620 Console

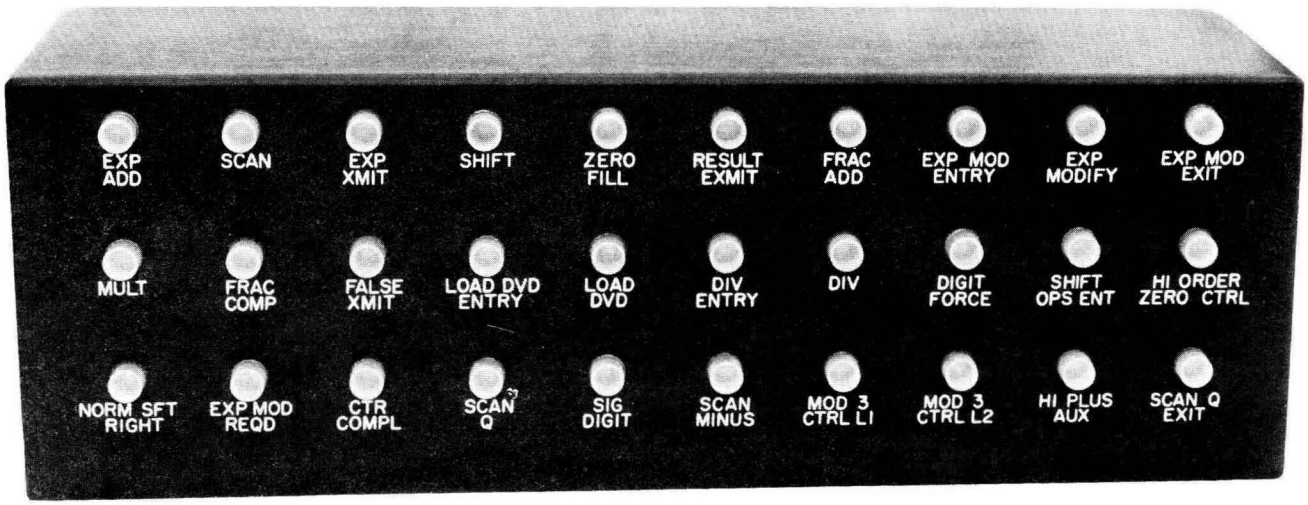


Figure 1-3. Auxiliary CE Console

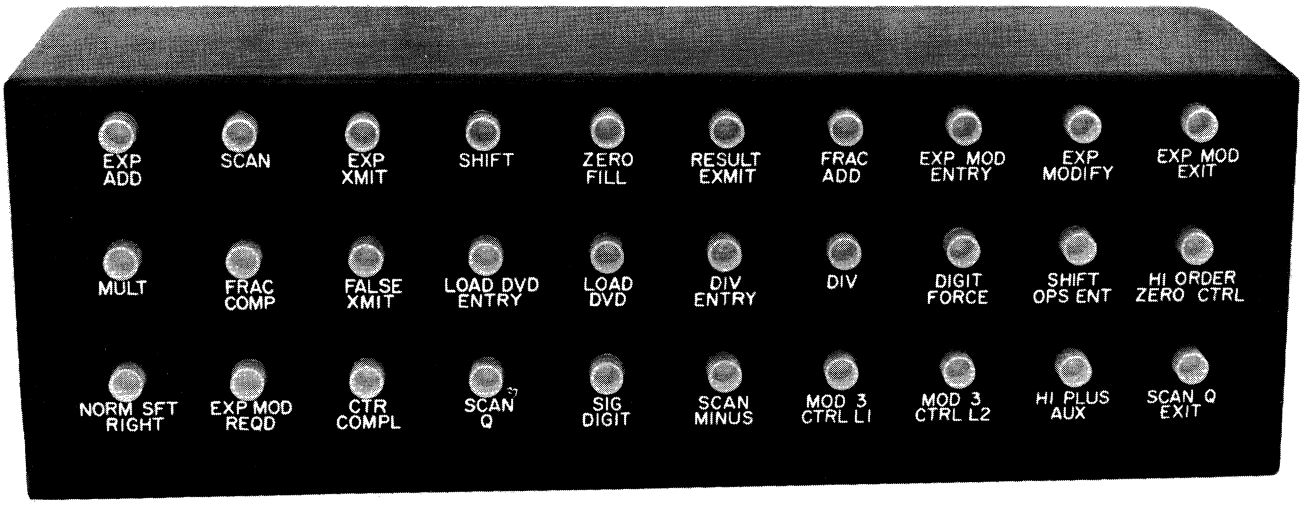
This console can be stored inside the 1620 CPU when not in use or it may be placed outside in any desired location, restricted only by the length of the cable that connects the auxiliary console to the CPU. Two magnets are built into the base of the auxiliary console box. These magnets will hold the console in the desired position.

Appendix A is a drawing of the auxiliary console showing the system diagram page number on which the latch, associated with the light, may be found. The drawing also shows page numbers of the function chart or charts on which the latches are found. The system diagram and function chart page numbers refer to the Instructional System Diagrams (Form 227-5631).

Appendix B is a list of the latches associated with floating point operations and includes the basic 1620 triggers (15, 16, 24, 25, 26, and 27). The list gives the system diagram and function chart page numbers on which the latches are located and shows if a console light is associated with the latch and indicates on which console the light is located.

Memory Address Register Storage (MARS)

Three new registers have been added to the MARS array: OR-4, OR-5, and CR-1. These three new registers appear on the memory address register display selector switch (Figure 1-2). The OR-4 and OR-5 registers are used for storing addresses in the same manner as OR-1, OR-2, etc. The CR-1 register is used somewhat differently. During an exponent compare operation, the algebraic difference between PE and QE, developed during trigger 13 time of the compare operation, is placed in CR-1. During the following scan mode (P or Q), CR-1 is read out and decremented or incremented by one and written back into CR-1. At each readout, the output of the increment/decrement switch is interrogated for a "zero" condition (MAR=0/CR-1=0). The presence or absence of a zero, before the field mark flag of the field being scanned is reached, determines what operation will follow. For a normalizing shift left, the CR-1 register is used with scan mode (0) to count the number of zeros encountered during the scan. The resulting count of zeros in CR-1 is then subtracted from the result exponent during the exponent modify mode.



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General

The four nonarithmetic floating point operations are given in this section. Two of the operations, floating shift right and floating shift left, are used to adjust field size. One operation, transmit floating, is used to relocate fields, and one operation, floating branch and transmit, provides the same branch and transmit facilities for floating point operations as is available for the basic 1620 operations.

Transmit Floating (TFL-06)

A function chart of this operation is on page 68 of the Instructional System Diagrams, (Form 227-5631). Transmit floating is essentially the same as the basic 1620 transmit field, code 26 operation. The difference is in the control exercised by the modulo 3 counter over the turn off time of the 1st cycle trigger. See the description of the modulo 3 counter for an explanation of its functions.

OBJECTIVE AND FUNCTION

Transmit the QF and QE field at the Q address per OR-1 to the location designated by the P address per OR-2.

The Q address is normally the low-order position of QE and the operation is the same as the basic transmit field instruction (TF-26), except that flag bits in the three low-order positions are ignored as indications to terminate the transmittal. Beginning with the fourth low-order digit, a flag bit (field mark of QF) terminates the operation. All flag bits in the field are transmitted.

TRIGGER FUNCTIONS

Trigger 26 (01.60.57.1).

1. Impulse the modulo 3 counter. For all other trigger 26 functions, see the basic transmit field operation.

Trigger 27 (01.60.57.1).

1. Turn off the 1st cycle trigger at W2 time of the third transmit cycle under control of the modulo 3 counter. For all other functions of trigger 27, see the basic transmit field operation.

Modulo 3 Counter

A function chart of the modulo 3 counter is on page 56 of the Instructional System Diagrams (Form 227-5631).

Three floating point operations use the modulo 3 counter:

1. Transmit floating (TFL-06).
2. Branch and transmit floating (BTFL-07)
3. Digit force mode which may be used depending upon the result of a floating add, subtract, multiply, or divide operation.

OBJECTIVE

The modulo 3 counter blocks the turn off (reset) of the 1st cycle trigger until the end of the third digit transmission cycle. This is done to prevent the field mark no. 1 trigger from recognizing a flag bit other than the field mark of the fraction (PF or QF) being transmitted. It is possible for three flag bits to be encountered before the field mark flag of the fraction is read out. These are:

1. The sign flag bit of the exponent (PE or QE).
2. The field mark flag bit of the exponent (PE or QE).
3. The sign flag bit of the fraction (PF or QF).

FUNCTIONS

First Trigger 24 or 26 Time.

1. Turns on the L1 and L2 modulo 3 latches. The L2 latch ON blocks the turn off of the 1st cycle trigger.

First Trigger 25 or 27 Time.

1. Turns on the L3 latch. Triggers 25 or 27 do not control this turn on. The L3 latch is turned on when the L1 latch is on at the next R3 time, which occurs during trigger 25 or 27 time. The L3 latch stays on until the next FP reset occurs.

Second Trigger 24 or 26 Time.

1. Turns off the L1 latch at W1 time.

Second Trigger 25 or 27 Time.

1. No action.

Third Trigger 24 or 26 Time.

1. Turns off the L2 latch at R3 time.

Third Trigger 25 or 27 Time.

1. Turns off the 1st cycle trigger at W2 time.

Branch and Transmit Floating (BTFL-07)

A function chart of this operation is on page 69 of the Instructional System Diagrams (Form 227-5631). Branch and transmit floating is essentially the same as the basic 1620 branch and transmit instruction (BT-27).

The difference is in the control exercised by the modulo 3 counter over the turn off time of the 1st cycle trigger. See the description under MODULO 3 COUNTER.

OBJECTIVE AND FUNCTION

Save the address of the next instruction in sequence by transferring the address in IR-1 to IR-2. Transmit the field at the Q address (QF and QE) to the P address minus one. Branch to the instruction at the P address now in IR-1.

The Q address is normally the low-order position of the exponent (QE). The operation is the same as the basic branch and transmit instruction (BT-27), except that in the transmit function the three low-order position flags are ignored as indications to terminate the transmittal. Beginning with the fourth low-order position, a flag bit (field mark of QF) terminates the operation. All flag bits are transmitted.

TRIGGER FUNCTIONS

Triggers 15 and 16 (01.60.45.1).
See the basic branch and transmit operation.

Trigger 26 (01.60.57.1).
1. Impulses the modulo 3 counter. For all other trigger 26 functions, see the basic branch and transmit operation.

Trigger 27 (01.60.57.1).
1. Turns off the 1st cycle trigger after the third transmit cycle under control of the modulo 3 counter. For all other trigger 27 functions, see the basic branch and transmit operation.

Floating Shift Right (FSR-08)

Function charts for this operation are on pages 71, 72, and 49 of the Instructional System Diagrams (Form 227-5631). Figure 2-1 is a data flow diagram for this operation. This instruction is used to shorten or shrink a fraction field. It is essentially a transmit field operation in which the field specified by the Q address is transmitted to the field specified by the P address. The P address is normally the units position of the fraction; the Q address is normally the address of a higher-order digit of the same fraction. Hence, in transmitting from the Q address to the P address, a higher-order fraction digit is transmitted to a lower-order position of the same fraction starting with the units fraction digit position and continuing into higher-order positions (lower-numbered memory locations). The transmission continues until the field mark flag bit of the Q field is encountered. This flag bit is transmitted with the last (high-order) Q field digit and becomes the field mark of the shortened fraction field. Vacated positions are filled with zeros. If the original units digit of the fraction (P address per OR-2) contains a sign flag bit prior to receiving the new units digit (Q address per OR-1) the sign flag is preserved. The exponent of the fraction is not moved or altered.

The operations described in the preceding paragraph are carried out in three steps:
1. Shift ops entry (Function chart on page 71*).
2. Shift mode (Function chart on page 72*).
3. Zero fill (Function chart on page 49*).

Shift Ops Entry (Code 08)

Shift ops entry is a control and address set up operation during which the P address per OR-2 is transferred to PR-3, and the Q address per OR-1 is transferred to PR-2. The units digit of the P address per OR-2 is interrogated for a sign flag bit. If a sign flag bit is present, the scan minus latch is turned on to preserve the sign condition so it will be placed back into the units position when the new (Q address) units position digit is transmitted to the P address, thus destroying the P address units digit.

TRIGGER FUNCTIONS

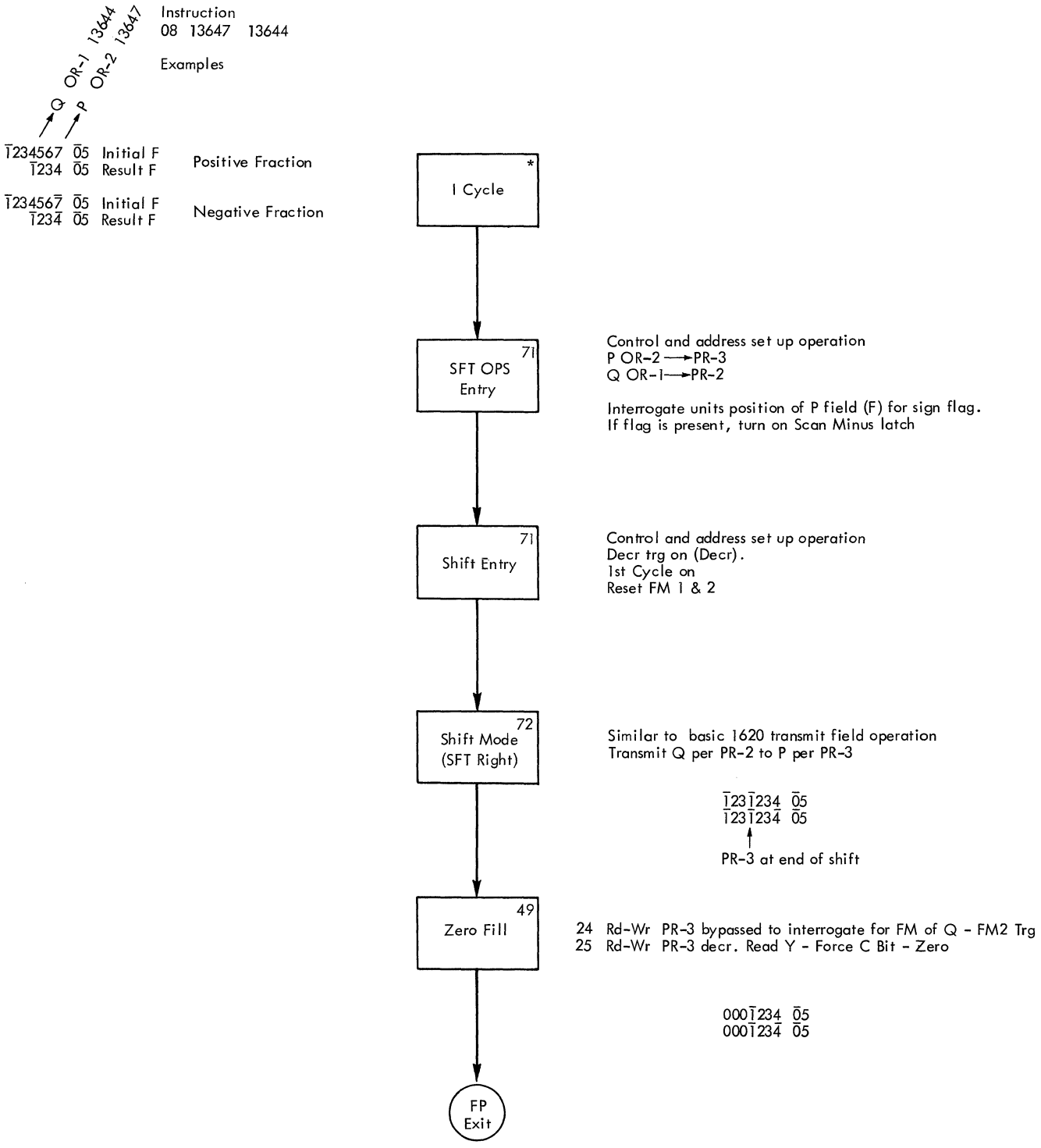
Shift Ops Entry Latch (01.67.50.1).
1. Turned on by I cycle trigger 8 and operation code 08.
2. Provides a *bypass* function for writing into MARS register during trigger 24 and 25 time.
3. Provides a gate for various trigger 24 and trigger 25 functions.
4. Turns on trigger 24.
5. Turned off by the shift mode latch.

Trigger 24 (01.68.24.1).
1. Reads out of memory per OR-2 (units digit of original fraction) and places the digit in MDR.
2. Resets (clears) PR-2 and PR-3.
3. Writes from MAR into PR-3 bypassed.
4. Turns on the scan minus latch if an MDR F bit is present (sign of the fraction).
5. Turns on trigger 25.

Trigger 25 (01.68.24.1).
1. Reads OR-1 into MAR (Q address – address of digit to be moved right).
2. Writes from MAR into PR-2 bypassed.
3. Turns on the shift entry latch.

*The function charts are in the *Customer Engineering Instructional System Diagrams, 1620 Data Processing System* (Form 227-5631).

One of two op codes in which the P & Q addresses addresses are not address of the exponents



-*- See Basic Function Charts

Figure 2-1. Data Flow – Floating Shift Right

Shift Entry Latch (01.66.50.1).

1. Turns on the decrement trigger (decrement).
2. Turns on the 1st cycle trigger.
3. Turns off field mark no. 1 and no. 2 triggers.
4. Exit to the shift mode (right) operation.

Shift Mode (Right)

Shift mode right accomplishes the transmission of the Q field per PR-2 to the P field per PR-3. The transmission or shift right operation stops when the field mark flag bit of the Q field is reached.

OBJECTIVE

Transmit the Q field per PR-2 to the location designated by the P address per PR-3 and successively lower memory positions. End the operation and exit to the zero fill operation when the field mark flag bit in the Q field is encountered.

FUNCTIONS

Triggers 24, 25, and the shift mode latch accomplish the shift operation. The Q field to be moved is read out of memory, one digit at a time per PR-2 during trigger 24 time, and written back into memory at the P address per PR-3 during trigger 25 time. If the scan minus latch is on during the first trigger 25 cycle, a sign flag bit is set.

TRIGGER FUNCTIONS

Shift Mode Latch (01.66.50.1).

1. Turned on by the shift entry latch of the shift ops entry operation.
2. Turns off the shift ops entry latch.
3. Provides a gate for various functions with triggers 24 and 25.
4. Turns on trigger 24.

Trigger 24 (01.68.24.1).

1. Reads out of memory per PR-2 and stores the digit in MDR.
2. Turns on field mark no. 1 trigger if an MDR F bit is present in MDR.
3. Writes back PR-2 decremented.
4. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Blocks reset of MDR (*Read Y*).
2. Reads out of memory per PR-3 with either the odd or the even sense amplifiers blocked (*Read Y*), depending upon whether PR-3 is odd or even, to clear the memory location.
3. Sets a sign flag bit in MDR if it is *first cycle* and the scan minus latch is on.
4. Turns off the 1st cycle trigger.
5. Transfers MDR to MBR (*Read Y*) and writes the contents of MBR into memory per PR-3.
6. Writes back PR-3 decremented.
7. Exit to zero fill mode if field mark no. 1 trigger is on.

Zero Fill Mode

Zero fill mode is entered from the shift mode during trigger 25 time with field mark no. 1 trigger on.

OBJECTIVES

Write zeros into the positions vacated by the preceding shift mode (right) operation.

FUNCTIONS

Starting with the position just left of the high-order digit of the fraction shifted right by the preceding shift mode (right) operation, force C bits (zeros) into the vacated positions. The operation exits to I cycle entry when field mark no. 2 trigger is on. Field mark no. 2 trigger is turned on when the field mark flag bit of the original Q address fraction is encountered.

TRIGGER FUNCTIONS

Zero Fill Mode Latch (01.66.60.1).

1. Turned on during trigger 25 time of the preceding shift mode (right) operation when field mark no. 1 trigger is on.
2. Provides gates for various functions with triggers 24 and 25.
3. Turns on trigger 24.

Trigger 24 (01.68.24.1).

1. Reads out of memory per PR-3 and stores the digit in MDR.
2. Turns on field mark no. 2 trigger if an MDR F bit is present (field mark of the original fraction).
3. Writes back PR-3 bypassed.
4. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Forces a reset of MDR regardless of *Read Y*.
2. Reads out of memory per PR-3 with either the odd or even sense amplifiers blocked (*Read Y*), depending on whether the PR-2 address is odd or even, to clear the memory location.
3. Turns on the MDR C bit latch (force zero).
4. Transfers MDR to MBR and writes the contents of MBR into memory per PR-3.
5. Writes back PR-3 decremented.
6. Exit to I cycle entry when field mark no. 2 trigger is on.

Floating Shift Left (FSL-05)

Function charts for this operation are given on pages 65, 66, 67, and 49 of the Instructional System Diagrams (Form 227-5631). Figure 2-2 is a data flow chart for this operation.

One of two op codes in which the P & Q addresses are not addresses of the exponents.

Instruction
05 01364 01371

Examples

Positive F
0000$\bar{1}$234 $\bar{0}$5
$\bar{1}$2340000 $\bar{0}$5

Negative F
0000$\bar{1}$23$\bar{4}$ $\bar{0}$5
$\bar{1}$234000$\bar{0}$ $\bar{0}$5

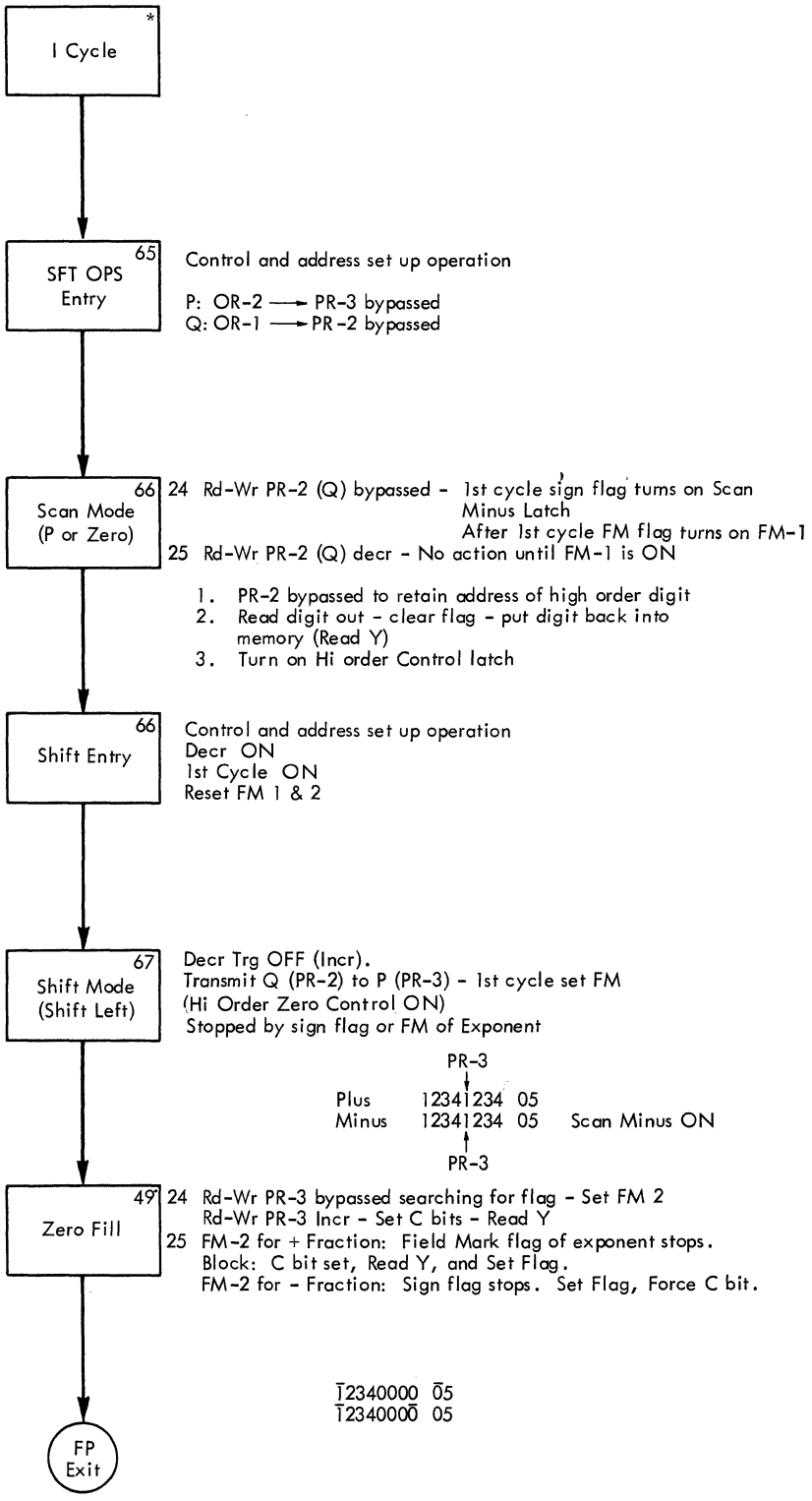
P OR-2 01364
Q OR-1 01371

OR-2 & PR-3 Flag cleared
PR-2
OR-1

00001234 $\bar{0}$5
Turns on Scan Minus latch
00001234 $\bar{0}$5
Hi Order Zero Control latch turned ON when FM flag detected to Force set of FM flag on 1st transmit (shift) cycle

P: OR-2 -PR-3 01360
Must be cleared prior to operation
PR-2
Q: OR-1 01371

0000$\bar{0}$000$\bar{1}$234 $\bar{0}$7
$\bar{1}$2340$\bar{0}$001234 $\bar{0}$7
Make certain that field is clear of flags before expanding F more than 2L



-*- See Basic Function Charts

Figure 2-2. Data Flow — Floating Shift Left

The field designated by the Q address, which is the address of the *low-order* position of the fraction, is shifted left so that the *high-order* digit is moved to the location specified by the P address. The exponent is not moved or altered.

The effect of this instruction is to expand the fraction by shifting it to the left and filling the vacated positions with zeros. It is important to note that the Q address is the address of the low-order position of the field moved, and the P address is the address of the high-order position of the resulting field. An existing sign flag bit at the Q address is retained for algebraic sign; the field flag bit is transmitted with the high-order digit of the Q field.

If the fraction is expanded to a length greater than 2L, any extraneous flag bits in core storage positions between the original high-order digit position of the Q address, and the new position of the low-order digit of the original fraction must be cleared before the FSL instruction is given. Therefore, if the address of Q minus the address of P is equal to or greater than 2L, locations between the P address plus L and the Q address minus L must be free of flags.

Unlike other instructions in the floating point series, FSL is executed in the transmit record manner of transmitting individual digits in the high-order to low-order sequence. After the units digit has been transmitted, the remaining positions of the fraction are set to zero in ascending core storage location sequence. After each position is set to zero, the succeeding position is checked for a flag bit. If the fraction is positive, the flag bit is assumed to be the high-order position of the exponent and the operation stops without altering the flag bit position. If the fraction is negative, the flag bit is assumed to be the sign flag of the fraction, and a negative zero is inserted in that position before the operation stops. Thus, a flag bit detected in a position prior to the previous high-order position of the original fraction stops the operation and results in an incorrect fraction.

For example, if P=01590, Q=01601, and L=4, core storage locations 01590 through 01603, with an extraneous flag bit in 01596, appear as follows:

XXXXXXX̄XF̄FFFĒE

After transfer of the fraction, but before the zero fill operation, the core storage locations appear as follows (note that the flag bit in 01598 has been cleared):

F̄FFFXXX̄XFFFFĒE

Upon completion of the operation, the fraction is incorrect, as follows:

F̄FFF00X̄XFFFFĒE

If 01596 had not contained a flag bit, the fraction would have been expanded correctly, as follows:

F̄FFF00000000ĒE

The operations described in the preceding paragraphs are carried out in four steps:

1. Shift ops entry (Function chart on page 65*).
2. Scan mode (Function chart on page 66*).
3. Shift mode (left) (Function chart on page 67*).
4. Zero fill mode (Function chart on page 49*).

Shift Ops Entry (Code 05)

Shift ops entry is a control and address set up operation.

OBJECTIVES

1. Transfer the P address per OR-2 into PR-3. The address in OR-2 designates the position to which the high-order digit of the fraction is to be shifted.
2. Transfer the Q address per OR-1 into PR-2. The address in OR-1 designates the units digit of the fraction to be shifted. This is also the address of the units position of the expanded fraction after the shift takes place and will always be a zero or flag zero, depending upon the original sign of the fraction to be expanded.

FUNCTIONS

Triggers 24, 25, and the shift ops entry latch accomplish the transfer of addresses. Trigger 24 transfers OR-2 to PR-3 and trigger 25 transfers OR-1 to PR-2. The shift ops entry latch causes a *bypass* during each of the transfers.

TRIGGER FUNCTIONS

Shift Ops Entry Latch (01.67.50.1).

1. Turned on by I cycle trigger 8 and operation code 05.
2. Causes a bypass function.
3. Turns on trigger 24.

Trigger 24 (01.68.24.1).

1. Reads OR-2 into MAR.
2. Resets (clears) PR-2 and PR-3.
3. Writes from MAR into PR-3 bypassed.
4. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Reads OR-1 into MAR.
2. Writes from MAR into PR-2 bypassed.
3. Exit to scan mode (op 05).

*The Function charts are in the *Customer Engineering Instructional System Diagrams, 1620 Data Processing System* (Form 227-5631).

Scan Mode (Code 05)

The scan mode (code 05) is entered from shift ops entry during trigger 25 time.

OBJECTIVES

Scan through the Q field per PR-2 to test the units digit for a sign flag on the first cycle and to test the remaining digits for the field mark flag. If a sign flag is present, the scan minus latch is turned on. Note that the sign flag is not cleared from memory. Field mark no. 1 trigger is turned on by the field mark flag to signal the end of the scan operation, and the field mark flag is cleared from the memory location.

FUNCTIONS

The scan mode latch controls the read and write functions of PR-2 during triggers 24 and 25 time. Trigger 24 tests the digits for sign and field mark flag bits. Trigger 25 clears the field mark flag bit, decrements PR-2 when trigger 25 is followed by trigger 24, and controls the function to follow.

TRIGGER FUNCTIONS

Scan Entry Latch (01.66.20.1).

1. Turned on by trigger 25 of the shift ops entry operation.
2. Turns on the 1st cycle trigger.
3. Turns off field mark no. 1 and no. 2 triggers.
4. Turns on the scan mode latch.
5. Turned off by entry reset.

Scan Mode Latch (01.66.20.1).

1. Causes read and write of PR-2 on every trigger 24 and 25 cycle.
2. Inhibits turn on of triggers 11, 21, 23, and 42.
3. Provides gates for various trigger 24 and 25 time functions.
4. Turns on trigger 24.
5. Turned off by the shift mode latch.

Trigger 24 (01.68.24.1).

1. Reads out of memory per PR-2 (function of the scan mode latch) and places the digit in MDR.
2. Turns on the scan minus latch if an MDR F bit (sign) is present on the first cycle.
3. Turns on field mark no. 1 trigger when an MDR F bit (field mark of Q) is present after the first cycle.
4. Turns on the decrement trigger (decrement).
5. Writes back PR-2 (function of the scan mode latch) bypassed.
6. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Reads out of memory per PR-2 (function of the scan mode latch) and places the digit in MDR.
2. Turns off the 1st cycle trigger.
3. Writes back PR-2 (function of the scan mode latch) decremented if field mark no. 1 trigger is off.

For cycle in which field mark no. 1 trigger is on:

4. Clears the field mark flag in MDR.
5. Transfers MDR to MBR *(Read Y)* and writes the contents of MBR into memory per PR-2.
6. Turns on the high-order zero control latch for use in setting the field mark flag in the high-order P address position.
7. Writes back PR-2 (function of the scan mode latch) bypassed. PR-2 contains the address of the high-order Q field digit to be transmitted.
8. Turns on the shift entry latch.

Shift Entry Latch (01.66.50.1).

1. Turns on the decrement trigger (decrement).
2. Turns on the 1st cycle trigger.
3. Turns off field mark no. 1 and no. 2 triggers.
4. Exit to the shift mode operation.

Shift Mode (Code 05)

The shift mode operation is entered from the shift entry operation which follows the scan mode (op 05) operation.

OBJECTIVE

Transmit the Q field per PR-2 to the P field per PR-3 starting with the high-order digit position and proceeding to lower-order digit positions (higher-numbered memory locations) until the operation is terminated by:

1. The field mark flag bit of the exponent associated with the Q field if the Q field is positive (no Q field sign flag).
2. The sign flag bit of the Q field if the Q field is negative.

FUNCTIONS

Triggers 24, 25, and the shift mode latch accomplish the left shift operation. During trigger 24 time, the Q address digits per PR-2 (starting with the high-order position) are read out to MDR and tested for a flag bit. During trigger 25 time, the Q address digit in MDR is written into memory per PR-3 (P address). The functions that occur when field mark no. 1 trigger is on depends upon the status of the scan minus latch. The scan minus latch is ON if the original Q field contains a sign flag bit, and is OFF if no sign flag bit is present. When a flag bit is encountered during the transmission, it may either be the sign flag of the original Q field or the field mark flag of the exponent associated with the Q field. If the scan minus latch is on (minus Q field), field mark no. 1 trigger is turned on by the flag in the

units position of the Q address. The *Read Y* function takes place, the flag is cleared as the units digit is transmitted to the new location, and PR-3 is decremented. PR-3 then contains the address immediately to the right of the last digit (units) transmitted to the new location. PR-3 is then set so it can be used to fill in zeros between the last digit transmitted and the exponent. If the scan minus latch is off, field mark no. 1 trigger is turned on by the field mark flag bit of the exponent immediately right of the Q address field. The *Read Y* function is inhibited, and PR-3 is written back bypassed. PR-3 then contains the same address as explained previously.

TRIGGER FUNCTIONS

Shift Mode Latch (01.66.50.1).

1. Turned on by the shift entry latch at the end of the scan mode operation.
2. Turns off the scan mode latch.
3. Provides gates for various functions with triggers 24 and 25.
4. Turns on trigger 24.
5. Turned off by the zero fill mode latch.

Trigger 24 (01.68.24.1).

1. Reads out of memory per PR-2 and places the digit in MDR.
2. Turns off the decrement trigger (increment).
3. Turns on field mark no. 1 trigger if an MDR F bit is present (sign of QF or field mark of QE).
4. Writes back PR-2 incremented.
5. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Blocks the reset of MDR *(Read Y)* if field mark no. 1 trigger is off or the scan minus latch is on.
2. Blocks the *Read Y* function if the field mark no. 1 trigger is on and the scan minus latch is off.
3. Reads out of memory per PR-3 with either the odd or even sense amplifiers blocked *(Read Y)*, depending on whether the PR-3 address is odd or even, to clear the memory location. Note that item 3 depends upon item 2.
4. Sets a field mark flag bit in MDR on first cycle (function of *high-order zero control*).
5. Clears the flag in all locations per PR-3 after first cycle.
6. Transfers MDR to MBR *(Read Y)* and writes the contents of MBR into memory per PR-3.
7. Writes back PR-3 incremented unless field mark no. 1 trigger is on and the scan minus latch is off, in which case write back PR-3 bypassed.
8. Turns off 1st cycle trigger.
9. Exit to zero fill mode when field mark no. 1 trigger is on.

Zero Fill Mode

The zero fill mode is entered from the shift mode (left) during trigger 25 time when field mark no. 1 trigger is on.

OBJECTIVE

Fill in zeros between the location to which the last digit was transmitted and the exponent associated with the Q address.

FUNCTIONS

Starting with the position just right of the last digit transmitted, the positions are read out and tested for a flag bit. If no flag bit is present, a zero (C bit) is forced into the position. If a flag bit is present it may be one of the following:

1. The sign flag bit of the original Q address field.
2. The field mark flag bit of the exponent associated with the Q address field.

If the scan minus latch is on, the first flag bit encountered is the sign flag of the original Q field, if the latch is off; the flag bit is the field mark of the exponent associated with the Q field. If the sign flag is encountered (scan minus latch on), a flag zero is forced into memory at that location. If the field mark flag bit of the exponent is encountered, the digit read out is returned to memory unaltered. The operation exits to I cycle entry when field mark no. 2 trigger is on.

TRIGGER FUNCTIONS

Zero Fill Mode Latch (01.66.60.1).

1. Turned on during trigger 25 time of the last shift mode cycle.
2. Provides gates for various functions with triggers 24 and 25.
3. Turns on trigger 24.

Trigger 24 (01.68.24.1).

1. Reads out of memory per PR-3 and places the digit in MDR.
2. Turns on field mark no. 2 trigger if an MDR F bit is present. Notice that the 1st cycle trigger is off at this time.
3. Writes back PR-3 bypassed.
4. Turns on trigger 25.

Trigger 25 (01.68.24.1).

For cycles prior to field mark no. 2 trigger being on:

1. Resets MDR regardless of *Read Y.*
2. Reads out of memory per PR-3 with either the odd or even sense amplifiers blocked *(Read Y)*, depending upon whether the PR-3 address is odd or even, to clear the memory location.
3. Turns on the MDR C bit latch (force zero).

4. Transfers MDR to MBR *(Read Y)* and writes the contents of MBR into memory per PR-3.
5. Writes back PR-3 incremented.

For the cycle in which field mark no. 2 trigger is on because of a sign flag bit in the units position of the original Q field (scan minus latch on):

6. Items 1 through 5 previously given, remain the same.
7. Turns on the MDR F bit latch to set the sign flag bit.
8. Exits to I cycle entry.

For the cycle in which field mark no. 1 trigger is on because of a field mark flag bit for the exponent associated with the Q address (scan minus latch off):

9. Blocks the *Read Y*, forces MDR C bit, resets MDR, and sets flag functions.
10. Reads out of memory per PR-3 and places the digit in MDR.
11. Writes the contents of MBR into memory per PR-3. This writes back the high-order exponent digit without alteration.
12. Exit to I cycle entry.

General

An exponent add, subtract, or compare operation is initiated following the I cycle in which any floating arithmetic operation code is placed in the operation register.

When a floating add or subtract operation (op code 01-FADD and 02-FSUB) is specified, an algebraic comparison of PE and QE is made. When a floating multiply operation (op code 03-FMUL) is specified, PE and QE are added algebraically. When a floating divide operation (op code 09-FDIV) is specified, QE is subtracted from PE algebraically.

Exponent add, subtract, or compare functions are accomplished by using triggers 11, 12, 13, 14, and 21, also the recomplement control trigger, recomplement trigger, and trigger 23 are used if a recomplement function is required. The functions of these circuits remain virtually the same as when used with the standard operation codes. The functions of the basic auxiliary triggers associated with the standard add, subtract, and compare operation codes remain the same. However, some new functions and auxiliary latches have been added to implement the floating point arithmetic operations. Because PE and QE consist of two digits each, only two complete add, subtract, or compare cycles are performed unless recomplement is required, in which case two recomplement cycles take place after an add or subtract operation. A compare operation is never recomplemented.

The floating point arithmetic function that follows the exponent add, subtract, or compare function is determined by the operation code used and/or by the status of various auxiliary triggers that are turned on or off during the exponent add, subtract, or compare function. The following are five functions to which the exponent add, subtract, or compare function can exit.

For floating add or subtract (operation codes 01 or 02):

1. Exit to fraction add if the equal/zero trigger is on, denoting that PE is equal to QE (PE=QE)
2. Exit to scan mode (Q) if the high/plus trigger is on and the equal/zero trigger is off, denoting that PE is greater than QE(PE>QE).
3. Exit to exponent transmit if the high/plus and equal/zero triggers are both off, denoting that PE is less than QE(PE<QE).

For floating multiply (operation code 03):

4. Exit to multiply mode, determined by the operation code (03).

For floating divide (operation code 09):

5. Exit to fraction compare mode, determined by the operation code (09).

A more complete description of exponent add, subtract, or compare and the conditions that determine which floating point arithmetic function will follow is given under FLOATING MULTIPLY and FLOATING ADD OR SUBTRACT.

For a description of the basic 1620 add, subtract, compare, operation see the CE Manual of Instruction (Form 227-5647). For Function charts of these operations, see pages 11 and 12 of the CE Instructional System Diagrams (Form 227-5631).

Floating Multiply

For a floating multiply operation, QE is added to PE and the sum replaces PE. PF is multiplied by QF and the product replaces PF. PF is normalized and PE is modified, as required, after multiplication.

The operations described in the preceding paragraph are carried out in six steps:

1. Exponent add or subtract (Function chart on page 45*).
2. Multiply mode (Function chart on page 58*, pages 14* through 19* for basic operation).
3. Exponent modify entry (Function chart on page 51*).
4. Exponent modify mode (03/09) (Function chart on page 52*).
5. Exponent modify exit (03/09) (Function chart on page 53*).
6. Result transmit mode (03/09) or digit force, depending upon whether a zero product is developed or if the resulting exponent exceeds +99 or is less than −99 (Function charts on pages 63* or 55*).

Section 4, EXAMPLES, contains a data flow chart (Figure 4-1) for multiply operations and examples of multiplication problems with various representative F and E values and signs.

*These function charts are in the *Customer Engineering Instructional System Diagrams, 1620 Data Processing System* (Form 227-5631).

Exponent Add or Subtract

Exponent add or subtract is essentially a basic add operation for operation code 03 floating multiply, or a subtract operation for operation code 09 floating divide.

OBJECTIVE

Add or subtract, algebraically, the exponents PE (OR-2) and QE (OR-1) and store the sum or difference at the PE address in memory.

FUNCTIONS

Exponent add or subtract functions are accomplished by using triggers 11, 12, 13, 14, and 21, also the recomplement control trigger, recomplement trigger, and trigger 23 are used if a recomplement function is required. The functions of these circuits remain virtually the same as when used with the standard operation codes. The functions of the auxiliary triggers associated with the standard add or subtract operation codes remain the same. However, several new functions and auxiliary latches have been added to implement the floating point arithmetic operations: exponent add mode latch, overflow/underflow latch, underflow/equal zero latch, and the overflow correct latch. The functions of these latches are explained under TRIGGER FUNCTIONS. Because PE and QE consist of two digits each, only two complete add or subtract cycles are performed unless recomplement is required, in which case two recomplement cycles also take place.

TRIGGER FUNCTIONS

Exponent Add Mode Latch (01.66.10.1).

1. Turned on by trigger 8.
2. Turns on trigger 11 for first memory cycle of the add or subtract operation.
3. Turned off by the multiply mode latch or the fraction compare mode latch.

The following functions are in addition to the basic trigger 11, 12, 13, and 14 functions for add or subtract.

Trigger 11 (01.60.11.1). NOTE: If the operation code is 09, the T/C trigger is turned off (complement) by trigger 8.

1. Resets OR-4 to clear it for receiving the address of the units digit of QF for use during the divide entry operation.
2. Resets OR-5 to clear it for receiving the address of the units digit of PE during trigger 12 time.
3. Resets PR-2 and PR-3 to clear them for receiving the address of the units digit of PF during trigger 14 time of the *last add cycle.*

Trigger 12 (01.60.12.1).

1. Writes from MAR (per OR-2) into OR-5 bypassed to retain the address of the units digit of PE for later use during the exponent modify entry mode.

Trigger 13 (01.60.13.1).

1. No additional functions.

Trigger 14 (01.60.14.1). The following functions occur on the *last add cycle.*

1. Resets OR-3 to clear it for receiving the address of the units position of the PF.
2. Writes from MAR (per OR-2) into OR-3, PR-3, and PR-2 decremented to preserve the units position address of the PF.
3. Turns on the overflow/underflow latch if the operation is *true* with a carry out. This occurs if the sum of two positive exponents exceeds +99.
4. Turns on the overflow/underflow latch and the underflow/equal zero latch if the operation is *true* with a carry out and the high/plus trigger is not on. This occurs if the sum of the negative exponents is more minus than −99.
5. Turns on the overflow correct latch in parallel with the overflow/underflow latch if the sum of the exponents is +100 with a multiply operation, or −100 with a divide operation.

   If an exponent of ±100 is modified to ±99 during the exponent modify mode, the overflow/underflow and/or the underflow/equal zero latches are turned off because an exponent of 99 is valid.
6. Exit to multiply mode if the operation code is 03, floating multiply.
7. Exit to fraction compare mode if the operation code is 09, floating divide.

Multiply Mode

The multiply mode is entered from the exponent add mode operation.

OBJECTIVE

Multiply the PF field (OR-2) by the QF field (OR-1), and store the algebraic product at location 00099 and successively lower memory locations.

FUNCTIONS

Triggers 32 through 41 and trigger 19 perform a basic multiply operation in which PF is the multiplicand and QF is the multiplier. To implement the floating multiply operation two new auxiliary latches are added; the exponent modify required latch and the multiply correct flag latch. One new function is added to trigger 19, three new functions are added to trigger 38, and one is added to trigger 39.

An explanation of each of the new functions is given with the associated trigger or latch under trigger functions.

Multiply Mode Entry Latch (01.67.00.1).

1. Turned on during the *last add cycle* by trigger 14.
2. Causes an *I cycle reset.*
3. Turns on the E cycle entry trigger.
4. Turns on the T/C trigger *(true).*
5. Turns on the multiply mode latch.

Multiply Mode Latch (01.67.00.1).

1. Blocks the turn on of triggers 11, 21, 23, and 42.
2. Turns off the exponent add mode latch.
3. Forces an operation code 23, which is a basic multiply operation.
4. Provides a gate for functions with triggers 19 and 38.
5. Turned off by the exponent modify entry latch.

Trigger 19 (01.60.49.1).

1. Exit to exponent modify entry when field mark no. 1 has been reached and there is no carry out.

Trigger 38 (01.62.38.1).

1. Turns on the exponent modify required latch on the last multiply cycle if the high-order digit of the product is a zero.

NOTE: During the last multiply cycle trigger 35 time, the product of the high-order multiplier (QF) digit and the high-order multiplicand (PF) digit is read out of the multiply table and stored in the D/B reg units and tens position. During the following trigger 37 time, the product digit in the D/B reg tens position is transferred to the D/B reg units position. The foregoing are basic 1620 multiply operations. The following applies to floating multiply only. During trigger 38 time, the D/B reg units is interrogated for a zero or not zero condition. If a zero is present, the exponent modify required latch is turned on. The presence of a zero at this time indicates that the high-order digit of the product is a zero. (See trigger 39 following for exception.)

2. Clear a flag bit (carry) after the first cycle if it is not the last multiply cycle, and if the high-order digit is not a zero.
3. Set the high-order field mark flag bit if the high-order digit of the product is a zero. This in effect places the field mark of the product one place to the right of the position that would normally be the high-order digit position. Because of this condition, the PE must be decreased by one during the exponent modify operation. The exponent modify required latch ON controls the "subtract one" function. See Example 2, FLOATING MULTIPLY, Section 4.

   It should be noted that a field mark flag bit is placed in the normal high-order position of the product by trigger 41. Thus two field mark flag bits are present with the product. However, when the product is transferred to the PF address, the first field mark encountered stops the transmit operation (for the exception, see Trigger 39) and the high-order flag zero is not transmitted.

Trigger 39 (01.62.39.1).

1. Turns on the multiply correct flag latch if the exponent modify correct latch is on and the high-order position of the product is not a zero.

   A special case exists when multiplying PF and QF fields containing digits such as 99901 × 19901 (see Example 5, FLOATING MULTIPLY, Section 4). These particular operands cause an 09 to be read out of the multiply table and set in D/B reg tens and units during trigger 35 time of the last multiply cycle. Trigger 37 resets D/B reg units and transfers D/B reg tens (the zero) to D/B reg units. The zero in D/B reg units during trigger 38 time satisfies the conditions necessary for turning on the exponent modify required latch and for setting a field mark flag bit with the digit that is immediately right of the high-order position of the product. However, during the previous trigger 40 time a carry was developed so that a one was placed in the high-order position of the product. During the next trigger 41 time, a field mark flag bit is set in the high-order position of the product. There are now two field mark flag bits in the product, one with the proper high-order digit and one with the digit immediately to the right of the high-order digit. It is necessary to do the following:

   a. Turn off the exponent modify required latch during the last trigger 39 time before exiting to the exponent modify mode to prevent changing the exponent (PE). This is accomplished by turning on the floating multiply correct latch during trigger 39 time.
   b. Clear the flag from the next to high-order position during the result transmit mode and block *FP exit* to allow the high-order digit to be transferred.
   c. Turn off the multiply correct flag latch to allow the normal set flag for field definition and FP exit to take place during the result transmit mode operation.

NOTE: During the basic multiply operation, PR-1 is used (after the product area clearing operation) to retain the location in the product area to which the first product digit is added, as each new multiplier digit is obtained. PR-1 initially contains 00099 and is decremented (−1) each time a new multiplier digit is obtained. Thus, at the end of the basic multiply operation, PR-1 contains the address of 99 minus the number of

digits in the multiplier, or 99—L in terms of floating multiply. The address in PR-1 (99—L) is transferred to OR-1 during the exponent modify exit operation, for use during the result transmit mode. The address in PR-1 (99—L) is transferred to OR-1 bypassed if no exponent modify is required, and is transferred to OR-1 incremented (100—L) if an exponent modify is required. See EXPONENT MODIFY EXIT (03/09), Section 3.

Exponent Modify Entry (03/09)

OBJECTIVE AND FUNCTIONS

The exponent modify entry function is a control and address set up operation to prepare for the exponent modify operation that follows. The address in OR-5 is transferred into OR-2 and OR-3 bypassed. OR-2, OR-3, and OR-5 then contain the address of the units position of the result exponent (PE). The high/plus, equal/zero, and 1st cycle triggers are turned on as in a basic add operation E cycle entry because the exponent modify operation is essentially an add or subtract operation involving the result exponent (PE).

TRIGGER FUNCTIONS

Exponent Modify Entry Latch (01.66.80.1).

1. Turned on by an exit from a multiply mode or divide mode operation.
2. Turns off the multiply or divide mode latch.
3. Provides gates for accomplishing various functions during trigger 24 and 25 time.
4. Turns on trigger 25.
5. Turned off by the exponent modify mode latch.

Trigger 24 (01.68.24.1).

1. Reads OR-5 into MAR (PE units).
2. Resets (clear) OR-1, OR-2, and OR-3.
3. Writes from MAR into OR-2, OR-3, and OR-5 bypassed.
4. Causes a *change mode* function which:
   a. Forces an I cycle reset.
   b. Turns on the T/C trigger *(true).*
   c. Turns on the E cycle entry trigger.
   d. Turns off the zero fill mode latch.
5. Turns on the high/plus auxiliary latch if the basic high/plus trigger is on. The sign of PF is preserved in the auxiliary latch. The basic high/plus trigger is thereby freed for use during the exponent modify mode operation.
6. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Blocks MAR reset to prevent a VRC (vertical redundancy check) error.
2. Turns on the high/plus trigger.
3. Turns on the equal/zero trigger.
4. Turns on the 1st cycle trigger.
5. Exit to exponent modify mode by turning on the exponent modify mode latch.

Exponent Modify Mode (03/09)

The exponent modify mode is entered from the exponent modify entry operation. The exponent modify operation is essentially an add or subtract operation. If the exponent modify required latch is off, zeros are added to or subtracted from the result exponent (PE) which causes no actual modification of the exponent. If the exponent modify required latch is on, a one is subtracted from the exponent for a multiply operation, or a one is added to the exponent for a divide operation.

OBJECTIVES

1. Make no changes in the exponent (PE) if the exponent modify required latch is off.
2. Subtract a one from the result exponent (PE) for a multiply operation if the exponent modify required latch is on.
3. Add one to the result exponent (PE) for a divide operation if the exponent modify required latch is on.

FUNCTIONS

The add or subtract functions are carried out by triggers 21, 12, 13, 14, and the recomplement triggers, if required. Note that trigger 21 is used in place of trigger 11. Eight memory cycles, four per digit, are required to modify the result exponent. Eight additional memory cycles will take place if a recomplement operation is required.

TRIGGER FUNCTIONS

Exponent Modify Mode Latch (01.66.80.1).

1. Turned on during trigger 25 time of the exponent modify entry mode operation.
2. Turns on the decrement trigger (decrement).
3. Turns off trigger 11.
4. Blocks trigger 11 being turned on by trigger 14.
5. Turns on trigger 21.
6. Turned off by the exponent modify exit latch.

Trigger 21 (01.60.31.1).

No exponent modify required – Multiply

1. Resets D/B reg units.
2. Sets a C bit in D/B reg units on first cycle.
3. Turns on field mark no. 1 trigger and sets a C in D/B reg units on second cycle.
4. Turns off the T/C trigger (complement) on first cycle.

Exponent modify required – Multiply

5. Resets D/B reg units.

6. Sets a 1 bit in D/R reg units.
7. Turns on field mark no. 1 trigger and sets a C bit in D/B reg units on second cycle.
8. Turns off the T/C trigger (complement) on first cycle.

No exponent modify required – Divide

9. Same as items 1, 2, and 3.

Exponent modify required – Divide

10. Same as items 5, 6, and 7.

Triggers 12 and 13 (01.60.12.1 and 01.60.13.1). For the functions of triggers 12, 13, and the other basic functions of trigger 14, the recomplement triggers, if needed, and the auxiliary triggers associated with a basic add or subtract operation, see pages 11 and 12 in the Function charts, Instructional System Diagrams (Form 227-5631). Also see the CE Manual of Instruction (Form 227-5647), Section 10, ARITHMETIC OPERATIONS.

Trigger 14 (01.60.14.1).
For last add cycle:

1. Exits to exponent modify exit by turning on the exponent modify exit latch.
2. Turns on the overflow/underflow latch if the operation is performed in the true mode, a carry out occurs, and the high/plus trigger is on ($>+99$).
3. Turns on the overflow/underflow latch and the underflow/equal zero latch if the operation is performed in the true mode, a carry out occurs, and the high/plus trigger is off (<-99).

Exponent Modify Exit (03/09)

OBJECTIVES

The exponent modify exit function is a control and address set up operation which prepares for the digit force mode or result transmit mode function that follows, and determines which function is to follow.

FUNCTIONS

The address in OR-2 is placed in PR-3 bypassed. PR-3 then contains the address of the units digit of PF. The address in PR-1 (99—L) is placed in OR-1 incremented (100—L) if the operation is multiply and exponent modify is required. The address in PR-1 (99—L) is placed in OR-1 bypassed (99—L) if the operation is divide, or if the operation is multiply and no exponent modify is required. The operation then exits to the function determined by the status of the overflow/underflow or underflow/equal zero latches. For details on how PR-1 is initially set to 99—L see MULTIPLY MODE under FLOATING MULTIPLY and DIVIDE ENTRY under FLOATING DIVIDE, Section 3.

TRIGGER FUNCTIONS

Exponent Modify Exit Latch (01.66.81.1).

1. Turned on during trigger 14 time of the last exponent modify cycle *(last add cycle).*
2. Turns off the exponent modify mode latch.
3. Provides gates for various functions during trigger 24 and 25 time.
4. Turns on trigger 24.

Trigger 24 (01.68.24.1).

1. Reads OR-2 into MAR. OR-2 contains the address of the units digit of PF.
2. Writes back OR-2 bypassed.
3. Writes into PR-3 from MAR bypassed.
4. Turns off the high/plus trigger.
5. Turns off field mark no. 1 and no. 2 triggers.
6. Turns on 1st cycle trigger.
7. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Reads PR-1 into MAR (99—L).
2. Writes into OR-1 from MAR incremented if the operation is multiply and an exponent modify is required. OR-1 now contains the address of the lowest-order product digit (100—L) to be transmitted from the product area to the PF address.
3. Writes into OR-1 from MAR bypassed if the operation is divide, or if the operation is multiply and no exponent modify is required. OR-1 now contains the address of the lowest-order product or quotient digit (99—L) to be transmitted from the product area to the PF address.
4. Turns on the high/plus trigger if the high/plus auxiliary latch is on. The sign of PF was saved in the high/plus auxiliary latch during the exponent modify entry operation.
5. Exit to result transmit mode if neither the overflow/underflow or the underflow/equal zero latch is on.
6. Exit to digit force mode if either the overflow/underflow or the underflow/equal zero latch is on.

Result Transmit Mode (03/09)

The result transmit mode (03/09) is entered during trigger 25 time of the exponent modify exit operation if neither the overflow/underflow or underflow/equal zero triggers are on thus indicating that the result exponent (PE) is not greater than +99 or less than —99.

OBJECTIVE

1. Transmit the resulting product or quotient in the product area per OR-1 to the PF field per OR-2.
2. Exit to I cycle entry for the next instruction in sequence when the entire field has been transmitted.

FUNCTIONS

Triggers 26, 27, and the result transmit mode latch perform a transmit field operation. In the case of divide, the quotient is always located at address 99—L and this address per OR-1 is used for the result transmit operation. If the operation is multiply, the result transmit will either be from address 99—L (per OR-1) in the case where no exponent modify was required, or from 100—L (per OR-1) in the case where exponent modify was required because of a high-order zero in the product. Also in the case of multiply, a sign flag bit is placed in the units position of the PF field in accordance with the status of the high/plus trigger. In a divide operation the sign will already be with the units position of the quotient in the product area and will be transmitted with it.

For an explanation of the special case multiply ($\bar{9}99\bar{0}1 \times \bar{1}99\bar{0}1$), see Trigger 27 following.

TRIGGER FUNCTIONS

Result Transmit Mode Latch (01.66.40.1).

1. Turned on during trigger 25 time of the exponent modify exit operation.
2. Turns on the decrement trigger (decrement).
3. Turns on the 1st cycle trigger.
4. Turns off field mark no. 1 and no. 2 triggers.
5. Turns on trigger 26.
6. Turned off by *FP reset.*

Trigger 26 (01.60.57.1).

1. Reads out of memory per OR-1 (product area) and stores the digit in MDR.
2. After the first cycle, turns on field mark no. 1 trigger when the end of the product or quotient field in the product area is reached.
3. Writes back OR-1 decremented.
4. Turns off the multiply correct flag latch on the extra trigger 26 cycle caused by the multiply correct flag latch being on.
5. Turns on trigger 27.

Trigger 27 (01.60.57.1).

1. Blocks reset of MDR *(Read Y).*
2. Reads out of memory per OR-2 with either the odd or even sense ampliers blocked *(Read Y),* depending on whether the OR-2 address is odd or even, to clear the memory location.
3. Sets or clears a flag bit (sign) in MDR depending upon the status of the high/plus trigger.
4. Transfers the contents of MDR to MBR *(Read Y)* and writes the contents of MBR into memory per OR-2.
5. Turns off the 1st cycle trigger (W2-D3).
6. Exit to I cycle entry if field mark no. 1 is on and the multiply correct flag latch is off.

In the special multiply case condition ($\bar{9}99\bar{0}1 \times \bar{1}99\bar{0}1$), the first field mark encountered by trigger 26 is associated with the digit immediately right of the high-order digit and is not the actual field mark flag bit. With the multiply correct flag latch on, the flag is cleared by trigger 27, the exit to I cycles is blocked, and trigger 26 is turned on to read out the actual high-order digit with its associated field mark flag bit. The high-order digit with its flag bit is transmitted to the PF field per OR-2. The operation then exits to I cycle entry for the next operation in sequence.

Digit Force

See FLOATING ADD, OR SUBTRACT, Section 3.

Multiplying by Zero ($\bar{0}0 \ldots 0\bar{9}\bar{9}$)

Multiplying by zero is a legal arithmetic operation. However, a special case exists when multiplication by zero is attempted in the floating point mode and the exponent of the multiplicand (PE) is $\bar{0}0$ or $\bar{0}\bar{0}$.

The following example describes what occurs when PF and PE=$\bar{2}46\bar{0}0$ and QF and QE=$\bar{0}0\bar{0}\bar{9}\bar{9}$. The example further describes a circuit that is not shown in the CE Instructional System Diagrams (Form 227-5631).

NOTE: An exponent check should not occur at *FP exit* time when a multiplication by zero is accomplished.

Given, a multiplicand (PF and PE) such as $\bar{2}46\bar{0}0$ and a multiplier (QF and QE) of machine zero, $\bar{0}0\bar{0}\bar{9}\bar{9}$.

1. The exponent add mode operation results in a PE of -99 ($\bar{9}\bar{9}$) which is a valid exponent.
2. The basic multiply operation does not turn off the basic equal/zero trigger (turned on by trigger 32) because the product digits are zeros.
3. The floating multiply mode operation turns on the exponent modify required latch during trigger 38 time (high-order zero) and, during the last trigger 19 time, accomplishes three functions.
   a. Turns on the underflow/equal zero latch to signal that a digit force (machine zero) operation is to take place following the exponent modify exit operation. This sets the product (PF and PE) to machine zero.
   b. Turns off the overflow/underflow latch. This latch is not on for this specific example. However, for any negative PE other than $\bar{0}\bar{0}$ the overflow/underflow latch would have been turned on during the exponent add mode and this function would turn it off to prevent the exponent check latch from being turned on at *FP exit* time, thus indicating an erroneous exponent check error.

c. NEW CIRCUIT. Turns off the exponent modify required latch to prevent a modification of PE (−99) during the exponent modify mode operation. This in turn prevents the overflow/underflow latch from being turned on because, if PE (−99) is modified [−99−(+1) = −100] a carry out during the exponent modify mode operation will turn on the overflow/underflow latch and in turn cause the exponent check latch to be turned on at *FP exit* time thereby indicating an erroneous exponent check.

It should be noted that, with a PE other than $\bar{0}0$ or $\bar{0}\bar{0}$, an overflow would not normally occur during the exponent modify mode. Any negative PE other than $\bar{0}\bar{0}$ will cause an overflow condition during the exponent add mode operation. However, during the last trigger 19 time of the multiply mode operation, the overflow/underflow latch is turned off, thereby preventing an erroneous exponent check. See item b. given previously.

Floating Divide

For a floating divide operation, QE is algebraically subtracted from PE. The resulting difference replaces PE. PF is divided by QF and the quotient, developed in the product area, is transmitted to the PF field thus replacing PF. PF is normalized and PE is modified, as required, after division.

The operations described in the preceding paragraph are carried out in eleven steps:

1. Exponent add or subtract mode (Function chart on page 45*).
2. Fraction compare mode (Function chart on page 59*).
3. False transmit mode (Function chart on page 60*).
4. Load dividend entry (Function chart on page 61*).
5. Load dividend (Function chart on page 20*. Basic operation).
6. Divide entry (Function chart on page 62*).
7. Divide mode (Function chart on pages 22* through 25*. Basic operation).
8. Exponent modify entry (03/09) (Function chart on page 51*).
9. Exponent modify mode (03/09) (Function chart on page 52*).
10. Exponent modify exit (03/09) (Function chart on page 53*).
11. Result transmit mode (03/09) or digit force, depending upon whether a zero quotient is developed or if the resulting exponent is greater than +99 or less than −99 (Function charts on pages 63* or 55*).

Section 4, EXAMPLES, contains a data flow chart for the divide operation and examples of divide problems with various representative F and E values and signs.

Exponent Add or Subtract Mode

See FLOATING MULTIPLY

Fraction Compare Mode

Fraction compare mode is entered from exponent add or subtract mode when the operation code is 09-divide.

OBJECTIVE

Compare the absolute** value of PF per OR-2 to the absolute value of QF per OR-1 to determine if PF is greater than or equal to QF, or if PF is less than QF. This comparison determines whether the dividend is loaded into 100—L or 99—L.

FUNCTIONS

The fraction compare operation is accomplished using triggers 11, 12, 13, 14, and the associated auxiliary triggers to perform essentially a basic comparison operation. The only difference is that the comparison is not performed algebraically but is performed on the absolute values of PF and QF. To cause a comparison of absolute values, the control of the T/C trigger by the signs of PF and/or QF is inhibited. Thus a complement operation is always performed. The status of the high/plus trigger at the end of the compare operation is used to determine the product area location into which the dividend is placed by the load dividend operation. It should be noted that the high/plus trigger is turned on at the beginning of the compare operation and when field mark no. 2 is reached, the status of the high/plus trigger is determined by a *carry out* or *no carry out* condition during trigger 13 time. If PF is greater than or equal to QF (H/P on) the load dividend operation will load the dividend into the product area at location 100—L. If PF is less than QF (H/P off), the dividend will be loaded into the product area at location 99—L.

*These function charts are in the *Customer Engineering Instructional System Diagrams, 1620 Data Processing System* (Form 227-5631).

**Numerical value disregarding algebraic signs.

TRIGGER FUNCTIONS

Fraction Compare Entry Latch (01.67.10.1).

1. Turned on by trigger 14 *last add cycle* of the exponent add or subtract mode operation.
2. Turns off the T/C trigger (complement).
3. Causes a *change mode* function which:
   a. Forces an I cycle reset.
   b. Turns on the E cycle entry trigger.
   c. Attempts to turn on the T/C trigger (true), however, the timing is such that item 2 holds the T/C trigger in the OFF status.
4. Turns on the fraction compare mode latch.

Fraction Compare Mode Latch (01.67.10.1).

1. Turns off the exponent add mode latch.
2. Blocks any change in the status of the T/C trigger. A fraction (PF or QF) sign flag bit, if present, cannot change the status of the T/C trigger during trigger 11 or 12 time.
3. Forces a basic code 24 compare operation by turning on trigger 11.
4. Exit to false transmit mode on the *last add cycle* of the compare operation.

False Transmit Mode

The false transmit mode is entered from the fraction compare mode during trigger 14 time of the *last add cycle.*

OBJECTIVES AND FUNCTIONS

Scan the PF field per OR-3 (PF units) for the presence of an MDR F bit (field mark of PF) and count the number of digit positions in PF by setting 00100 in MAR, decrementing the address in MAR into PR-2 on the first cycle, and then decrementing PR-2 for every digit cycle until the field mark is encountered. The exponent modify required latch is turned on if the H/P trigger is ON (from the preceding fraction compare mode). The exponent modify required latch then controls which address (100—L or 99—L) is used by the load dividend operation for loading the dividend into the product area. Exit to load dividend entry when field mark no. 1 trigger is on. At the end of the operation, PR-2 contains the address of 100—L.

Trigger 24 performs the scan of PF per OR-3 and trigger 25 sets 00100 in MAR, decrementing MAR into PR-2, and decrementing PR-2 until the field mark is encountered.

TRIGGER FUNCTIONS

False Transmit Mode Latch (01.67.20.1).

1. Turned on by trigger 14 of the last compare cycle of the fraction compare operation.
2. Turns off the fraction compare mode latch.
3. Blocks the turn on of triggers 11, 21, 23, and 42.
4. Turns on the exponent modify required latch if the high/plus trigger is on. The exponent modify latch controls two functions when on:
   a. During the load dividend operation, the address (100—L) in PR-2 is written into OR-2 bypassed, thus OR-2 contains the address 100—L. If the latch is off, the address in PR-2 is written into OR-2 decremented, thus OR-2 contains the address 99—L.
   b. During the exponent modify mode operation, a "one" is added to the exponent. If the latch is off, a "zero" is added, thus the exponent is not modified.
5. Turns on the 1st cycle trigger.
6. Turns off field mark no. 1 and no. 2 triggers.
7. Turns on trigger 24.

Trigger 24 (01.68.24.1)

1. Reads out of memory per OR-3 (starting with PF units) and stores the digit in MDR.
2. After first cycle, turn on field mark no. 1 trigger if an MDR F bit is present.
3. Writes back OR-3 decremented.
4. Turns on trigger 25.

Trigger 25 (01.68.24.1).

First cycle:

1. Resets (clears) PR-2.
2. Sets 00100 in MAR.
3. Writes from MAR into PR-2 decremented.
4. Turns off 1st cycle trigger (W2-D3).

Second and subsequent cycles:

5. Reads PR-2 into MAR.
6. Writes back PR-2 decremented.
7. Exits to load dividend entry if field mark no. 1 trigger is on.

Load Dividend Entry

The load dividend entry mode is entered during trigger 25 time of the false transmit mode if field mark no. 1 trigger is on. The load dividend entry is a control and address set up operation.

OBJECTIVES

1. Set OR-2 to the product area address to which the units digit of the dividend is to be transmitted during the load dividend operation.
2. Set OR-1 to the address of the units digit of PF (dividend) which is to be transmitted to the product area per OR-2.

FUNCTIONS

Triggers 24, 25, and the load dividend mode latch are used in performing the control and address set up operations. Trigger 24 clears various MARS registers and

sets the product area address (100—L or 99—L) into OR-2. PR-2 retains the 100—L address. Trigger 25 sets the address of the units digit of the dividend (PF) into OR-1.

TRIGGER FUNCTIONS

Load Dividend Entry Latch (01.67.30.1).

1. Turned on during trigger 25 time of the false transmit mode when field mark no. 1 trigger is on.
2. Causes a *change mode* function which:
   a. Forces an I cycle reset.
   b. Turns on the T/C trigger (true).
   c. Turns on the E cycle entry trigger.
   d. Turns off the zero fill mode latch.
3. Provides gates for accomplishing various functions during trigger 24 and 25 time.
4. Turns on trigger 24.
5. Turned off by the load dividend mode latch.

Trigger 24 (01.68.24.1).

1. Reads PR-2 into MAR (100—L).
2. Resets (clears) OR-1, OR-2, OR-3 and PR-1.
3. Writes back PR-2 bypassed (100—L).
4. Writes from MAR into OR-2 decremented (99—L) if the exponent modify required latch is off.
5. Writes from MAR into OR-2 bypassed (100—L) if the exponent modify required latch is on.
6. Turns on 1st cycle trigger.
7. Turns off field mark no. 1 and no. 2 triggers.
8. Turns off the false transmit mode latch.
9. Developes the additional *MARS address entry* gate (R5-D8) making a total gate of T4-D15.
10. Turns on trigger 25.

Trigger 25 (01.68.24.1)

1. Reads PR-3 into MAR (PF units).
2. Writes from MAR into OR-1 bypassed.
3. Turns on the load dividend mode latch.

Load Dividend

The load dividend mode is entered from the load dividend entry operation and forces a basic code 28 load dividend operation.

Load Dividend Mode Latch (01.67.30.1).

1. Forces a basic code 28 load dividend operation.

For details of the basic code 28 operation, see the CE Manual of Instruction (Form 227-5647).

Divide Entry

Divide entry is entered from the load dividend operation and is a control and address set up operation.

OBJECTIVES AND FUNCTIONS

The divide entry latch causes an I cycle reset and turns on the T/C trigger *(true)*. Trigger 24 places, in OR-2 and OR-3, the address (100-L) of the dividend digit from which the units digit of the divisor is subtracted. Trigger 25 places the address of the units digit of the divisor (QF units) in OR-1 and PR-1 and turns on the divide mode latch. The divide mode latch initiates a basic code 29 divide operation.

TRIGGER FUNCTIONS

Divide Entry Latch (01.67.40.1).

1. Turned on during trigger 29 time of the load dividend operation.
2. Causes a *change mode* function which:
   a. Forces an *I-cycle reset*
   b. Turns on the T/C trigger *(true).*
   c. Turns on the E cycle entry trigger.
   d. Turns off the zero fill mode latch.
3. Provides a gate for various functions with triggers 24 and 25.
4. Turns on trigger 24.
5. Turned off by the divide mode latch.

Trigger 24 (01.68.24.1).

1. Reads PR-2 into MAR (100—L).
2. Resets (clears) OR-1, OR-2, OR-3, and PR-1.
3. Writes from MAR into PR-2 bypassed.
4. Writes from MAR into OR-2 and OR-3 bypassed. OR-2 and OR-3 contain the address (100—L) of the dividend digit from which the first divisor digit (QF units) is to be subtracted.
5. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Reads OR-4 into MAR (units digit of the divisor: QF units).
2. Writes from MAR into OR-1 bypassed.
3. Writes from MAR into PR-1 bypassed.
4. Turns on the divide mode latch.

Divide Mode

The divide mode is entered from the divide entry operation and forces a basic code 29 divide operation.

Divide Mode Latch (01.67.40.1).

1. Forces a basic code 29 divide operation.
2. Turned off by the exponent modify entry latch.

NOTE: The first quotient digit developed during the divide operation is stored one position to the left of the dividend position from which the high-order digit of the divisor is subtracted.

NOTE: During trigger 14 time of the last divide add cycle *(last divide cycle* AND *divide add),* the address written back into OR-2 is the address of the units quotient digit. During this same trigger 14 time, PR-1 is cleared and the address of the units quotient digit per OR-2 is written into PR-1. PR-1 thus contains the address (99—L) of the units digit of the quotient. See

Function chart p. 62 (Form 227-5631). The address in PR-1 is transferred to OR-1 during the exponent modify exit operation for use during the result transmit operation.

For details of the basic code 29 operation, see the CE Manual of Instruction (Form 227-5647).

Exponent Modify Entry (03/09)

See FLOATING MULTIPLY

Exponent Modify Mode (03/09)

See FLOATING MULTIPLY

Exponent Modify Exit (03/09)

See FLOATING MULTIPLY

Result Transmit Mode (03/09)

See FLOATING MULTIPLY

Digit Force

See FLOATING ADD OR SUBTRACT

Floating Add or Subtract

For a floating add or subtract operation, PE is compared with QE to determine if the exponents are of equal value or if one is greater (algebraically) than the other. The algebraic difference between PE and QE is designated "d."

Depending on L (length of the operands) and the value of d, the appropriate field is shifted to align decimal points before the addition of PF and QF is performed.

If d=0 (PE = QE), no shift is made.

If d > 0 (PE > QE) and the difference (d) is less than the length (L) of the operands, QF is, in effect, shifted d positions to the right before being added to PF. The number of low-order digits in QF equal to d are lost as the shift is made.

If d < 0 (PE < QE) and the absolute value of d is less than L, PF is shifted d positions to the right before QF is added to it. The number of low-order digits in PF equal to the absolute value of d are lost when PF is shifted.

If d > 0 or d < 0 and in both cases if d or |d| (absolute value of d) is greater than L, the shift of PF or QF causes PF or QF to be shifted beyond the available result field which is L digits in length. In this case, the fraction being shifted is considered insignificant in relation to the remaining fraction and the remaining fraction is declared the result without alteration (except for a possible sign change).

Following the alignment of decimals, the fraction add (or subtract) takes place.

If there is no carry out from the high-order position, or if the high-order result digit is not a zero, the fraction does not need to be normalized and the floating add or subtract operation is complete.

If a carry out from the high-order position occurs, the fraction must be normalized by shifting it to the right so that the carry position fits into the available result field length, and the exponent must be modified (+1) so that it reflects the increased positional value of the fraction caused by the carry out.

If the result fraction contains a high-order zero (and possibly more than one) but does not contain all zeros, the fraction must be normalized by shifting it to the left a number of places equal to the number of high-order zeros. The exponent must be decreased by an amount equal to the number of high-order zeros so that the exponent reflects the decreased positional value of the fraction caused by the high-order zero or zeros.

If the result fraction contains all zeros, machine zero is forced into the result fraction field immediately after the fraction add (or subtract) operation.

Functions charts for floating add or subtract are in the Instructional System Diagrams (Form 227-5631). The Function chart page numbers in the following list are not necessarily in the order in which they are used because the varied paths available depend upon the numerical values and signs of the fractions and exponents involved and upon the operation (add or subtract) being performed.

Section 4, EXAMPLES, contains a data flow chart for the floating add or subtract operation and examples of addition problems with various representative F and E values and signs.

Exponent Compare Mode (Op Code 01 or 02)

OBJECTIVES

Compare QE specified by the Q address (OR-1) to PE specified by the P address (OR-2) to determine if PE is higher than, equal to, or less than QE with signs taken into consideration.

FUNCTIONS

The high, equal, or low condition of the 2-digit PE field, specified by OR-2, relative to the two-digit QE field, specified by OR-1, is established, considering signs. Both fields remain unchanged after the comparison has been completed.

Four memory cycles are required to compare each position of the two fields as follows:

1. One digit from the Q field (QE) is read from memory per OR-1 to the units position of the digit branch register.
2. The corresponding digit of the P (PE) field is read from memory per OR-2 to MDR.
3. The P field digit is transferred from MDR to the tens position of MAR and the digit stored in the digit/branch register is complemented (tens complement in units position, nines complement in other positions) and placed in the units position of MAR. This manufactured address with a 3 placed in the hundreds position of MAR is used to read the one digit difference from the add table in memory to MDR.
4. The difference digit in MDR is not written back into memory but is written into CR-1 for later use as a counter to determine how far PF or QF must be shifted to align the decimal points if alignment is needed. The fourth cycle decrements the P address (OR-2) in preparation for the next compare cycle.

The comparison proceeds serially, one digit at a time, from low-order to high-order digits of the compared fields until the operation is terminated by a flag bit (field mark no. 2) in the high-order position of the P field (PE). The comparison is performed internally by subtraction of the Q field (QE) from the P field (PE).

RESULTING AUXILIARY TRIGGER (INDICATOR) STATUS

Condition (Algebraic)	Indicators	
	High/Plus	Equal/Zero
PE greater than QE (PE>QE)	ON	OFF
PE less than QE (PE<QE)	OFF	OFF
PE equal to QE (PE=QE)	OFF	ON

PE = Two-digit exponent in field at P address
QE = Two-digit exponent in field at Q address

If the comparison of PE and QE results in an algebraic difference greater than 99, the D>99 latch is turned on to control the scan operation that follows.

If the comparison (algebraic subtraction) of PE and QE results in a complement figure stored in CR-1 (counter), the counter complement latch is turned on to control whether CR-1 is incremented or decremented in the scan operation that follows.

TRIGGER FUNCTIONS

The exponent compare function is initiated when trigger 8 of the I cycle turns on the exponent add mode latch.

Exponent Add Mode Latch (01.66.10.1).

1. Turned on by trigger 8.
2. Forces a basic compare operation (code 24).
3. Turns on trigger 11 for first memory cycle of the compare operation.
4. Turned off by the mode or entry latch of the following operation.
5. Turned off by floating point reset.

Trigger 11 (01.60.11.1).

1. Turns on first cycle trigger.
2. Reads out of memory per OR-1 (QE) and stores the digit in D/B reg units.
3. Resets OR-4 to clear it for receiving the address of the units digit of QE later in the memory cycle.
4. Resets OR-5 to clear it for receiving the address of the units digit of PE during trigger 12 time.
5. Resets CR-1 (counter) to clear it for receiving the difference digits (PE—QE) during the two trigger 13 times.
6. Resets PR-2 and PR-3 to clear them for receiving the address of the units digit of PF during trigger 14 time of the last add cycle.
7. Writes from MAR into OR-4 bypassed on first MARS write time (R3-D2) to retain the address of the units digit of QE for later use if needed.
8. Writes back OR-1 decremented on second MARS write time (W3-D2) for addressing the tens digit of QE on the next trigger 11 time.
9. Turns on the T/C trigger if QE is negative.

For second cycle:

10. Turn on field mark no. 1 trigger.

Trigger 12 (01.60.12.1).

1. Reads out of memory per OR-2 (PE) and stores the digit in MDR.
2. Writes back OR-2 bypassed to retain the address of the units digit of PE for later use if needed.

For first cycle:

3. Writes from MAR into OR-5 bypassed to retain the address of the units digit of PE for later use if needed.
4. Changes the status of the T/C trigger if PE is negative.
5. Turns off the high/plus trigger if PE is negative.
6. Turns on the carry in trigger to obtain 10s complement in units position if a complement operation is indicated (T/C trigger OFF).

For second cycle:

7. Turns on field mark no. 2 trigger (field mark of PE).

Trigger 13 (01.60.13.1).

1. Develops and sets add table address in MAR.
2. Reads out of memory per add table address and stores the digit in MDR.
3. Turns on the carry out trigger if MDR contains an F bit (carry).
4. Resets D/B reg units and transfers the digit in MDR to D/B reg units.

For first cycle:

5. Writes the digit stored in D/B reg units into CR-1 units. This stores the algebraic difference of the unit digits (PE—QE) for later use if needed.

For second cycle:

6. Resets D/B reg tens and transfers the digit in MBR-odd or MBR-even to D/B reg tens depending upon whether the address in MAR is odd or even.
7. Writes the digit stored in D/B reg tens into CR-1 tens. This stores the algebraic difference of the tens digit (PE—QE) for later use if needed.
8. Sets a C bit (zero) into CR-1 hundreds, thousands, and ten-thousands positions (to prevent a VRC error when CR-1 is read out to MAR).
9. Changes the status of the high/plus trigger if there is no carry out on the cycle in which field mark no. 2 is reached and it is a complement operation (T/C trigger OFF).
10. Turns off the equal/zero trigger if the add table digit (in MDR) is not a zero.

Trigger 14 (01.60.14.1).

1. Reads into MAR from OR-2 (PE) and writes back OR-2 decremented.
2. Turns on carry in trigger if the carry out trigger is on (due to an add table carry or a carry due to T/C switch 9 out, and the carry in trigger on).

For first cycle:

3. Turns on trigger 11 and turns off 1st cycle trigger if neither field mark no. 1 nor field mark no. 2 has been reached, and repeats the four memory cycles (triggers 11, 12, 13, and 14) for the tens position of PE and QE.

For second cycle *(last add cycle)*:

NOTE: A recomplement operation is not performed at the end of a compare operation. It is possible for CR-1 (counter) to contain the complement of the algebraic difference of PE and QE depending upon their respective signs. If this condition exists, the counter complement latch is turned on and, when CR-1 is scanned, it is incremented instead of decremented.

4. Resets OR-3 to clear it for receiving the address of the units position of PF for later use if needed.
5. Writes from MAR into OR-3, PR-2, and PR-3 to preserve the units position address of PF for later use if needed.
6. Turns on the counter comp latch if there is no carry out on a complement operation (CR-1 contains a complement figure).
7. Turns on the D>99 (d greater than 99) trigger if there is a carry out on a true (T/C trigger on) operation. This condition occurs if the algebraic difference of PE—QE is greater than 99. If the D>99 trigger is on and:
   a. PE>QE (high/plus on — equal/zero off), the normal exit to scan (Q) will take place. However, the MAR=0/CR-1=0 (CR-1 counter reaching zero) line is blocked and the scan will continue until the field mark flag bit of QF is detected and turns on the scan Q exit latch. With the scan Q exit latch on, the next trigger 25 time will cause the scan operation to exit to I cycle entry for the next instruction in sequence. No fraction add operation takes place, and the PF and PE fields remain unaltered in memory. PF is used as the sum or difference because the value of QF is considered to be insignificant in relation to PF.
   b. PE<QE (high/plus and equal/zero triggers off), the normal exit to exponent transmit will take place. Exponent transmit replaces PE with QE and then exits to scan mode (P). The MAR=0/CR-1=0 line is blocked and the scan of PF continues until the field mark F bit of PF is detected and turns on field mark no. 1 trigger. With field mark no. 1 trigger on, the next trigger 25 time will cause the scan operation to exit to result transmit. The result transmit mode replaces PF with QF and then exits to I cycle entry for the next instruction in sequence. No fraction add operation takes place because PE and PF have been replaced by QE and QF in memory. QF is now used as the sum or difference because the value of PF is considered to be insignificant in relation to QF.
8. Exits to fraction add mode if the equal/zero trigger is on (PE = QE or d = 0), indicating that the decimal positions of PF and QF are aligned.
9. Exits to scan mode (Q) if the high/plus trigger is on and the equal/zero trigger is off (PE > QE), indicating that the decimal positions of PF and QF are not aligned. The QF address (OR-1) is adjusted to align the decimals.

10. Exits to exponent transmit mode if the high/plus and equal/zero triggers are both off (PE < QE), indicating that the decimal positions are not aligned. PE is replaced by QE (exponent transmit) and PF is shifted to the right to align the decimals. The high-order positions of PF, vacated by the right shift, are filled with zeros (zero fill mode).

Scan Mode (Q)

The scan mode (Q) is entered from exponent add mode (compare) when PE>QE, indicated by the high/plus trigger being on, and when the comparison does not result in a zero difference, indicated by the equal/zero trigger being off. These conditions indicate that PF is more significant than QF and only the high-order digits of QF are to be added to PF.

OBJECTIVES

1. Adjust OR-1 so that it contains the address of the QF digit that is equivalent in significance to the lowest-order digit of PF. This, in effect, shifts QF to the right to align the PF and QF decimals.
2. End the operation by exiting to I cycle entry if the algebraic difference between PE and QE is greater than 99 or greater than the length of the QF field. In either case PF is considered to be the result.

FUNCTIONS

Scan mode (Q) scans through the Q field (QF), two memory cycles per digit using triggers 24 and 25, decrementing CR-1 and looking for the CR-1 counter being zero (MAR=0/CR-1=0), or for the presence of a flag bit (field mark of QF). If CR-1 contains a complement figure (counter complement latch on), the scan will increment CR-1 while looking for the counter being zero.

OR-1 is used to scan through the QF field. If the field mark flag bit of QF is encountered during the scan before the CR-1 counter reaches zero, there will be no digits in QF with equivalent significance to those in PF. Therefore, the result of the add or subtract operation is PF itself, and the operation can be terminated (exit to I cycle entry) after changing the status of the high/plus trigger, if necessary, to indicate the sign of the P field which is now the result.

NOTE: The high/plus trigger is ON at the end of the fraction compare operation. This ON status is determined by the comparison of the exponents. The ON status of the high/plus trigger directs the entry into the scan mode (Q) operation. If it is determined that there are no QF digits with equivalent significance to those in PF (see preceding paragraph), the status of the high/plus trigger must be set to reflect the sign of PF. If the sign of PF is plus, the ON status of the high/plus trigger is not changed. If the sign of PF is negative, the high/plus trigger is turned off (see trigger 25, item 3, under TRIGGER FUNCTIONS following).

There are two possible causes for exiting to I cycle entry:

1. If the algebraic differences between PE and QE is greater than 99 (PE—QE = d>99), the D>99 trigger is turned on. The D>99 trigger ON, blocks the MAR=0/CR-1=0 line which, when up, indicates that the CR-1 counter reached zero. Therefore, the scan continues until the field mark of QF is encountered, causing the operation to be terminated as previously explained regardless of the counter reaching zero.
2. If the algebraic difference between PE and QE is greater than the length of the QF field, for example, if the field of QF is five digits long and the algebraic difference of PE and QE is six, shifting QF six places to the right will shift QF beyond the significance of PF and the field mark of QF will be encountered before the counter (CR-1) goes to zero. In this case, PF and PE are considered to be the result, and the operation is terminated as previously explained.

In the event that the counter reaches zero before the QF field mark flag bit is detected, the scan operation exits to fraction add. The address now in OR-1 is the address of the QF digit which is equivalent in significance to the lowest-order digit of PF. The addition or subtraction of the fractions can now proceed in the normal 1620 manner.

TRIGGER FUNCTIONS

The scan mode (Q) is initiated when trigger 14 of the *last add cycle* of the exponent compare operation turns on the scan entry latch and the scan Q latch.

Scan Entry Latch (01.66.20.1).

1. Turned on during trigger 14 time of the *last add cycle* of the exponent compare operation.
2. Turns on the scan mode latch.
3. Turns on 1st cycle trigger.
4. Turns off field mark no. 1 and no. 2 triggers.
5. Turned off during the following memory cycle.

Scan Q Latch (01.66.21.1).

1. Turned on by trigger 14 of the last add cycle of the exponent compare operation.
2. Provides a gate for reading and writing OR-1 and for turning on the scan Q exit latch if an MDR F bit (field mark of QF) is detected.
3. Provides a gate for exiting to fraction add.

It should be noted that the scan Q latch remains ON for use during the fraction add operation. At the end of the fraction add mode operation, either exiting to I cycle entry or turning on the high-order zero control latch will turn off the scan Q latch.

Scan Mode Latch (01.66.20.1).

1. Turned on by the scan entry latch and remains on throughout the scan operation.
2. Provides gates for performing various scan functions.
3. Turns on trigger 24.
4. Turned off by the mode latch of the following function or by a floating point exit reset (FP reset).

Trigger 24 (01.68.24.1).

1. Turns on the decrement trigger (decrement).

First cycle:

2. Reads out of memory per OR-1 and tests for an MDR F bit (sign of QF). If an MDR F bit is present, turns on the scan minus latch to preserve the sign of QF for use during fraction add. At the end of the fraction add mode operation, either an exit to I cycle entry or an exit to scan mode (0) will turn off the scan minus latch.
3. Writes back OR-1 decremented.

Second and subsequent cycles:

4. Reads out of memory per OR-1 and tests for an MDR F bit (field mark of QF). If an MDR F bit is present, turns on the scan Q exit latch for use during the next trigger 25 time to cause an exit to I cycle entry.
5. Writes back OR-1 decremented.

Trigger 25 (01.68.24.1).

1. Turns off the decrement trigger (increment) if the counter complement latch is on.
2. Turns off the 1st cycle trigger.
3. If the scan Q exit latch is on, reads out of memory per OR-2 (units position of PF) and checks for the sign of PF (MDR F bit). If an MDR F bit is present (minus sign) turns off the high/plus trigger. The high/plus trigger ON (plus) or OFF (minus) indicates the sign of PF.
4. Reads CR-1 into MAR and checks for MAR=0/CR-1=0 which is taken from the output of the increment/decrement switch (MAR address ±1 depending upon status of counter complement trigger). If the output of the increment/decrement switch is zero (MAR=0/CR-1=0), exit to fraction add.
5. Writes back CR-1 incremented or decremented, depending upon the status of the counter complement trigger.
6. If the scan Q exit latch is on, exit to I cycle entry.

Exponent Transmit Mode

The exponent transmit mode is entered from exponent compare when PE<QE, indicated by the high/plus trigger being off and the comparison not resulting in a zero difference, indicated by the equal/zero trigger being off. These conditions indicate that QF is more significant than PF and only the high-order digits of PF are to be added to QF. QE is taken as the exponent of the sum or difference, therefore, QE is transmitted to the location of PE and replaces PE.

OBJECTIVE

Transmit QE units and tens per OR-4 to the location of PE units and tens per OR-5. QE replaces PE which is lost.

FUNCTIONS

The transmittal of QE to PE requires four memory cycles, two for each digit. The flag bits for the sign, if any, and the field mark are transmitted with the digits. Triggers 24 and 25 accomplish the operation.

TRIGGER FUNCTIONS

Exponent Transmit Entry Latch (01.66.30.1).

1. Turned on by trigger 14 of the *last exponent add* cycle.
2. Blocks turn on of trigger 11.
3. Turns off the exponent add mode latch.
4. Turns on the 1st cycle trigger.
5. Turns off field mark no. 1 and no. 2 triggers.
6. Turns on the exponent transmit mode latch.
7. Turned off by *entry reset* from the floating point arithmetic function that follows.

Exponent Transmit Mode Latch (01.66.30.1).

1. Turned on by the exponent transmit entry latch.
2. Provides gates for various functions with triggers 24 and 25.
3. Turns on trigger 24.
4. Turned off by the scan mode latch.

Trigger 24 (01.68.24.1).

1. Reads out of memory per OR-4 (units position of QE on first cycle, tens position on second cycle) and stores the digit in MDR.
2. Writes back OR-4 decremented.

Trigger 25 (01.68.24.1)

1. Blocks reset of MDR *(Read Y).*
2. Reads out of memory per OR-5 (units position of PE on first cycle, tens position on second cycle) with either the odd or even sense amplifiers blocked *(Read Y)*, depending on whether the OR-5 address is odd or even, to clear the memory location.
3. Writes back OR-5 decremented.
4. Transfers MDR to MBR *(Read Y).*

5. Writes into memory per OR-5 from MBR.
6. Turns off 1st cycle trigger at W2-D3 time.

   NOTE: The turn off of the 1st cycle trigger occurs late (W2-D3) in the first trigger 25 time. The turn on of the scan mode trigger in the floating point arithmetic function that follows is gated by R3-D4 time which occurs before the turn off of the 1st cycle trigger by trigger 25. The scan mode therefore cannot be entered during the first trigger 25 time but must wait until the second trigger 25 time when the 1st cycle trigger is off at R3-D4 time.

7. Exits to scan mode (P) on second cycle.

Scan Mode (P)

The scan mode (P) is entered from exponent transmit. Because the exponent compare operation indicated that PE<QE, the exponent transmit operation has replaced PE with QE. It is further required that PF be shifted to the right because it is of less significance than QF and therefore only the high-order digits of PF are to be added to QF.

OBJECTIVES

1. Adjust PR-2 so that it contains the address of the PF digit that is equivalent in significance to the lowest-order digit of QF. This operation establishes the address of the low-order PF digit to which the low-order QF digit is to be added.
2. Exit to the result transmit mode if the field mark of PF is reached before the CR-1 counter goes to zero and brings up the MAR=0/CR-1=0 line.
3. Exit to the fraction add mode if the CR-1 counter reaches zero (MAR=0/CR-1=0) before the field mark of PF is reached.

FUNCTIONS

Scan mode (P) scans through the P field (PF), two memory cycles per digit, using triggers 24 and 25. The CR-1 counter is incremented and decremented, depending upon the status of the counter complement latch, while looking for CR-1 to reach zero (MAR=0/CR-1=0), or for the presence of a flag bit, (field mark no. 1 trigger ON due to reaching the field mark of PF). If the CR-1 counter contains a complement figure, the counter complement latch is on, causing the scan to increment CR-1.

PR-2 is used to scan through the PF field. If the CR-1 counter reaches zero prior to reaching the field mark flag bit of PF, the scan operation exits to fraction add. The address in PR-2 at this time is the address of the PF digit which is equivalent in significance to the lowest-order digit of QF. The addition or subtraction of the P and Q fractions can now proceed in the normal 1620 manner.

If the field mark flag bit of PF is encountered prior to CR-1 reaching zero, this indicates there are no digits in PF with equivalent significance to those in QF. Therefore, QF is declared to be the result of the floating point add or subtract operation. The QF field must be transmitted to the PF field, thus replacing PF with QF which becomes the result. The result transmit mode accomplishes the transmission of the QF field to the PF field.

There are two possible causes for exiting to result transmit mode:

1. The algebraic difference between PE and QE is greater than the length of PF. For example, if the field of PF is five digits long and the algebraic difference of PE and QE is six, shifting PF six places to the right will shift PF beyond the significance of QF, and the field mark of PF will be encountered before the counter (CR-1) goes to zero.
2. The algebraic difference between PE and QE is greater than 99. In this case the D>99 latch is turned on, which in turn blocks the MAR=0/CR-1=0 line. With MAR=0/CR-1=0 blocked, the scan proceeds until the field mark of PF is encountered (field mark no. 1 trigger on).

TRIGGER FUNCTIONS

The scan mode (P) is initiated when trigger 25 of the exponent transmit operation turns on the scan entry latch.

Scan Entry Latch (01.66.20.1).

1. Turned on during trigger 25 time of the second exponent transmit cycle.
2. Turns on the scan mode latch.
3. Turns on the 1st cycle trigger.
4. Turns off field mark no. 1 and no. 2 triggers.
5. Turned off during the following memory cycle.

Scan Mode Latch (01.66.20.1).

1. Turned on by the scan entry latch and remains on throughout the scan operation.
2. Provides gates for performing various scan functions.
3. Turns on trigger 24.
4. Turned off by the mode latch of the following function.

Trigger 24 (01.68.24.1).

1. Turns on the decrement trigger (decrement).

First cycle:

2. Reads out of memory per PR-2 (PF units) and tests for an MDR F bit (sign of PF). If an MDR F bit is present, turns on the scan minus latch to preserve the sign of PF for use during the shift mode (right) operation.
3. Writes back PR-2 decremented.

Second and subsequent cycles:

4. Reads out of memory per PR-2 and tests for an MDR F bit (field mark of PF). If an MDR F bit is present, turns on field mark no. 1 trigger for use during the next trigger 25 time to cause an exit to the result transmit mode.
5. Writes back PR-2 decremented.

Trigger 25 (01.68.24.1).

1. Turns off the decrement trigger (increment) if the counter complement latch is on.
2. Turns off the 1st cycle trigger.
3. If field mark no. 1 trigger is on, exit to the result transmit mode.
4. Reads CR-1 into MAR and checks for MAR=0/CR-1=0 which is taken from the output of the increment/decrement switch (MAR address ±1 depending upon status of counter complement latch). If the output of the increment/decrement switch is zero (MAR=0/CR-1=0), exit to shift mode (right).

NOTE: Only the output of the units and tens position of MAR, through the incr/decr switch, is checked.

5. Write back CR-1 incremented or decremented depending upon the status of the counter complement latch.

Result Transmit Mode (01/02)

The result transmit mode (01/02) is entered from scan mode (P) during trigger 25 time when field mark no. 1 trigger is on (field mark of PF), thus indicating that PF is not significant in relation to QF.

OBJECTIVES

1. Transmit the QF field to the PF field including sign, if any, and field mark.
2. Exit to I cycle entry when the entire QF field has been transmitted to the PF field address.

FUNCTIONS

The QF field is transmitted to the PF field, two memory cycles per digit, using triggers 26 and 27. The sign of QF is checked and, if an operation code 01 floating add is being performed, the sign of QF becomes the sign of PF. If an operation code 02 floating subtract is being performed, the sign of QF is changed when QF is transmitted to the PF field.

When the result transmit mode is entered, the high/plus trigger is off (result of exponent compare). During trigger 26 time of the result transmit operation the high/plus trigger is turned on if QF is negative and remains off if QF is positive.

For Operation 01 Floating Add. The sign of QF becomes the result sign. During trigger 27 time, the status of the high/plus trigger is changed. For example, if QF is positive, the high/plus trigger (off during trigger 26 time) is turned on. The ON status is then used to clear the flag bit (if any) in MDR. If QF is negative, the high/plus trigger (turned on during trigger 26 time) is turned off. The OFF status is then used to set a flag bit in MDR (sign of result fraction).

For Operation Code 02 Floating Subtract. The sign of QF must be changed before it becomes the result sign. During trigger 27 time, the status of the high/plus trigger, set during trigger 26 time, is used to determine the sign of the result fraction. If QF is negative, the ON status of the high/plus trigger is used to clear the flag bit (if any) in MDR. If QF is positive, the OFF status of the high/plus trigger is used to set a sign flag bit in MDR. This accomplishes the reversal of signs required by an algebraic subtraction. For example, if QF is negative and is subtracted from zero (PF insignificant), the sign of the subtrahend (QF) must be changed to positive (clear flag). Likewise, if QF is positive and is subtracted from zero (PF insignificant), the sign of the subtrahend (QF) must be changed to negative (set flag).

TRIGGER FUNCTIONS

Result Transmit Mode Latch (01.66.40.1).

1. Turned on during trigger 25 time of the last scan of the previous scan mode operation and remains on throughout the transmit operation.
2. Turns on the decrement trigger (decrement).
3. Turns on the 1st cycle trigger.
4. Turns off field mark no. 1 and no. 2 triggers.
5. Turns off the scan mode latch.
6. Turns on trigger 26.
7. Turned off by *FP reset.*

Trigger 26 (01.60.57.1).

1. Reads out of memory per OR-1 (QF) and stores the digit in MDR.

First cycle:

2. Turns on the high/plus trigger if an MDR F bit is present (sign of QF).

Second and subsequent cycles:

3. Turns on field mark no. 1 trigger when the end of the QF field is reached.
4. Writes back OR-1 decremented.

Trigger 27 (01.60.57.1).

1. Blocks reset of MDR *(Read Y).*
2. Reads out of memory per OR-2 (PF) with either the odd or even sense amplifiers blocked *(Read Y),* depending on whether the OR-2 address is odd or even, to clear the memory location.

First cycle:

3. For op code 01 (FADD), changes the status of the high/plus trigger.
4. Sets or clears a flag bit (sign) in MDR depending upon the status of the high/plus trigger.
5. Transfers MDR to MBR *(Read Y)* and writes the contents of MBR into memory per OR-2.
6. Turns off the 1st cycle trigger.

NOTE: *NOT M3 = CTR L2* is at +S.

Second and subsequent cycles:

7. Turns on FP exit latch and exits to I cycle entry when field mark no. 1 (QF) is reached during the previous trigger 26 time.

Shift Mode (Right) Op Codes 01/02

The shift mode (right) is entered from scan mode (P) during trigger 25 time when the CR-1 counter reaches zero (MAR=0/CR-1=0) prior to the scan reaching the field mark of PF. This condition indicates that PF must be shifted to the right to align the low-order significant digit of PF to the lowest-order digit of QF.

OBJECTIVES

1. Transmit the significant digits of PF per PR-2 to the location specified by PR-3. The address in PR-2 was decremented to the address of the first low-order significant digit in PF during the preceding scan mode (P) operation. PR-3 contains the address of the original units position digit of PF. This address was placed in PR-3 during the exponent compare operation.
2. Exit to zero fill mode when the end of the PF field is reached.

FUNCTIONS

The PF digits per PR-2 are transmitted to the location designated by PR-3, two memory cycles per digit, using triggers 24 and 25. The sign of PF is determined by the status of the scan minus latch which was set during scan mode (P). If the scan minus latch is on, a flag bit will be set with the first digit transmitted to the PR-3 address. If the scan minus latch is off, a clear flag function occurs.

It should be noted that the scan mode (P) operation may have left only one significant PF digit to be transmitted. In this case, this single digit is the high-order digit of the original PF field; it has the field mark flag bit associated with it and only this one digit is shifted. The fact that field mark no. 1 trigger is turned on is used to signal the exit to the zero fill mode. The sign of PF is set with the single digit depending upon the status of the scan minus trigger. If PF is positive, the field mark associated with the single digit is cleared by the clear flag function.

TRIGGER FUNCTIONS

Shift Entry Latch (01.66.50.1).

1. Turned on during trigger 25 time of the last scan mode (P) operation.
2. Turns on the decrement trigger (decrement).
3. Turns on the 1st cycle trigger.
4. Turns off field mark no. 1 and no. 2 triggers.
5. Turns on the shift mode latch.

Shift Mode Latch (01.66.50.1).

1. Turns off the scan mode latch.
2. Provides gates for various trigger 24 and trigger 25 functions.
3. Turns on trigger 24.
4. Turned off by the zero fill mode latch.

Trigger 24 (01.68.24.1)

1. Reads out of memory per PR-2 and stores the digit in MDR.
2. Turns on field mark no. 1 trigger if an MDR F bit is present (field mark of PF).
3. Turns off the shift entry latch.
4. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Blocks reset of MDR *(Read Y).*
2. Reads out of memory per PR-3 with either the odd or even sense amplifiers blocked *(Read Y),* depending on whether the PR-3 address is odd or even, to clear the memory location.
3. Writes back PR-3 decremented.
4. Turns on the flag bit trigger in MDR to set the sign of PF during the 1st cycle if the scan minus latch is on.
5. Turns off the flag bit trigger (if on) in MDR if the scan minus latch is off (positive PF), or if it is not the first cycle.
6. Transfers MDR to MBR *(Read Y)* and writes the digit into memory per PR-3.
7. Turns off the 1st cycle trigger (W2-D3).
8. Exit to zero fill mode if the field mark of PF was detected (field mark no. 1 trigger on) during the previous trigger 24 time.

Zero Fill Mode

Zero fill mode is entered from shift mode (right) during trigger 25 time when field mark no. 1 trigger is on (field mark of PF) at the end of the operation that shifted PF to the right to align the lowest-order significant digits of PF and QF.

OBJECTIVE

1. Place zeros (C bits) in the PF positions vacated by the previous shift mode (right) operation.

FUNCTIONS

Two cycles per digit are required, using triggers 24 and 25. During trigger 24 cycles, the PF digit to be replaced is read out of memory per PR-3 and investigated for the presence of a field mark. PR-3 is written back bypassed. During trigger 25 cycles, the digit is again read out of memory per PR-3, MDR is reset (regardless of *Read Y*), and a C bit is placed in MDR to be written into memory per PR-3. When the field mark of PF is encountered, a flag is set to mark the high-order position of PF. This location is the same as the original PF high-order digit location except that the location is now filled with a flag zero (flag bit alone) instead of the original significant digit.

The address in PR-3 at the beginning of the zero fill mode operation is the address of the first position to the left of the high-order digit of the shifted PF, after PF is shifted to the right. This address is placed in PR-3 during the last trigger 25 time of the shift mode.

TRIGGER FUNCTIONS

Zero Fill Mode Latch (01.66.60.1).

1. Turned on by trigger 25 of the shift mode (right) operation.
2. Turns off shift mode latch.
3. Provides a gate to accomplish various functions during trigger 24 and 25 time.
4. Turns on trigger 24.
5. Turned off by the fraction add entry trigger.

Trigger 24 (01.68.24.1).

1. Reads out of memory per PR-3 and stores the digit in MDR.
2. Turns on field mark no. 2 trigger if an MDR F bit is present (field mark of PF).
3. Writes back PR-3 bypassed to retain the same address for filling in a zero during trigger 25 time.
4. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Resets MDR regardless of *Read Y*.
2. Reads out of memory per PR-3 with either the odd or the even sense amplifiers blocked *(Read Y)*, depending on whether the PR-3 address is odd or even, to clear the memory location.
3. Turns on the C bit trigger in MDR.
4. Turns on the flag bit trigger in MDR if field mark no. 2 trigger is on (field mark of PF).
5. Transfers MDR to MBR *(Read Y)*. If both a C bit and a flag bit are set in MDR, the C bit corrector will clear the C bit and only the flag bit will reach MBR.
6. Writes into memory per PR-3 from MBR.
7. Writes back PR-3 decremented.
8. Exit to fraction add mode if field mark no. 2 trigger is on (field mark of PF).

Fraction Add Mode

Fraction add mode is entered from one of three floating point arithmetic functions:

1. Exponent compare where d = 0 (PE − QE = d).
2. Scan mode (Q) where PE>QE and where at least one digit in QF is significant in relation to the digits in PF.
3. Zero fill mode where PE<QE and where at least one digit in PF is significant in relation to the digits in QF.

When the fraction add mode is entered, all initial adjustments to the exponents have been made, as required. The fractions have been shifted, as required, to align the decimal points (that is, the fractions have been shifted so that digits of equal significance are aligned).

At the beginning of fraction add, OR-1 contains the address of the units position of QF. OR-2 and OR-3 contain the address of the units position of PF. Addition or subtraction of the fractions (PF and QF) can now take place in the normal 1620 manner.

OBJECTIVES

1. Depending upon the operation code, add or subtract the fractions designated by OR-1 for QF and OR-2 for PF.
2. Exit to I cycle entry if no normalizing shift left or right is indicated. The exit to I cycle entry is made when:
   a. The high-order digit of the sum or difference is not a zero.
   b. The sum or difference of the high-order digits does not produce a carry.
3. Exit to exponent modify entry mode if a normalizing shift right is indicated by the fraction add taking place in the true mode and there is a carry out from the high-order position during the add.
4. Exit to scan mode (zero) if a normalizing shift left is indicated by the fraction add taking place in the complement mode, and the result contains a high-order zero.
5. Exit to digit force mode if the entire result field (PF) is zero, which is indicated by the equal/zero trigger being on.

FUNCTIONS

The fraction add operation is essentially a basic 1620 add or subtract operation and makes use of triggers 11, 12, 13, and 14. Recomplement takes place normally, if necessary. The resulting indicator status directs the computer to one of four operations:

1. No normalizing is required as defined in item 2 under OBJECTIVES.
2. A normalizing shift right is required as defined in item 3 under OBJECTIVES.
3. A normalizing shift left is required as defined in item 4 under OBJECTIVES.
4. A digit force operation is required as defined in item 5 under OBJECTIVES.

TRIGGER FUNCTIONS

Fraction Add Entry Latch (01.66.70.1).

1. Turned on by exit to fraction add mode from zero fill mode, exponent compare mode, or scan mode (Q).
2. Turns off the scan mode trigger.
3. Causes a *change mode* function which:
   a. Forces an *I cycle reset.*
   b. Turns on the T/C trigger (true).
   c. Turns on the E cycle entry trigger.
   d. Turns off the zero fill mode latch.
4. Turns off the T/C trigger (complement) if the operation code is 02-FSUB.
5. Turns on the fraction add mode latch.
6. Turned off when the next exit to I cycle entry takes place.

Fraction Add Mode Latch (01.66.70.1).

1. Turns off the exponent add mode latch.
2. Forces a basic add operation code 21 which turns on trigger 11.
3. Provides a gate *(fraction add mode* AND *scan Q)* for accomplishing certain functions during trigger 11 time.
4. Provides a gate for use with various functions during trigger 14 time.

Trigger 11 (01.60.11.1).

1. Reads out of memory per OR-1 and stores the digit in D/B reg units (basic op).
2. Writes back OR-1 decremented (basic op).

If fraction add is preceded by scan mode (Q):

3. Turns on field mark no. 1 trigger if an MDR F bit (field mark of QF) is present. It should be noted that during the scan mode (Q) operation, OR-1 is decremented and may have had the address of the high-order QF digit stored in it on the last scan cycle during which the scan mode exited to fraction add mode. Thus an MDR F bit being present when OR-1 is read out during the first trigger 11 time, indicates that the first digit read out is the high-order digit of the QF field and the MDR F bit is the field mark of QF. Trigger 21 is used to supply "make-up" zeros for the remainder of the fraction add operation.
4. Changes the status of the T/C trigger if the scan minus latch is on. The scan minus latch is used to preserve the sign of QF during the scan mode (Q) operation.
5. Blocks the basic trigger 11 function that changes the status of the T/C trigger if an MDR F bit (basic sign function) is present *(fraction add Q sign inhibit).*

If fraction add is not preceded by scan mode (Q):

6. Turns on field mark no. 1 trigger after first cycle when end of QF field is reached.
7. Changes status of T/C trigger during 1st cycle if QF field is negative.

Triggers 12 and 13 (01.60.12.1 and 01.60.13.1). For other functions of triggers 11 and 14, and for functions of triggers 12, 13, 21, 23, and the auxiliary triggers associated with the basic add and subtract operations, see the CE Manual of Instruction (Form 227-5647). Function charts for the basic add, subtract, compare operations are on pages 11 and 12 of the Instructional System Diagrams (Form 227-5631).

Trigger 14 (01.60.14.1). Additional floating point functions on last trigger 14 cycle *(last add cycle):*

1. Resets PR-2 and PR-3.
2. Turns on the high-order zero control latch if the high-order sum or difference digit in MDR is a zero.
3. Exit to I cycle entry if:
   a. The add operation is accomplished in the true mode, there is no carry out from the high-order position and the equal/zero trigger is off.
   b. The add operation is accomplished in the complement mode and the high-order zero control latch is off (no zero in high-order position of the result field).
4. Turns on the normalizing shift right latch and exits to exponent modify entry if the add or subtract operation is accomplished in the true mode and there is a carry out from the high-order position.

NOTE: The basic overflow trigger is turned on by a true and a carry out condition. If the O'Flow check switch is set to STOP, the computer will stop at the next I cycle entry time.

5. If the add or subtract operation is complement, the high-order zero control latch is on, and the equal/zero trigger is off:
   a. Exits to scan mode (zero).
   b. Writes back PR-2 and PR-3 bypassed to preserve the address of the high-order digit of the result field (PF) for use by the scan mode (zero) operation.
   c. Turns off the decrement trigger (increment).

6. Exit to digit force mode and turns on the underflow/equal zero latch if the equal/zero trigger is on.

Exponent Modify Entry (01/02)

OBJECTIVES AND FUNCTIONS

The exponent modify entry function is a control and address set up operation to prepare for the exponent modify operation that follows. The address in OR-5 is transferred into OR-2 and OR-3 bypassed. OR-2, OR-3, and OR-5 then contain the address of the units position of the result exponent (PE). The high/plus, equal/zero, and 1st cycle triggers are turned on as in a basic add operation E cycle entry because the exponent modify operation is essentially an add or subtract operation involving the result exponent (PE).

TRIGGER FUNCTIONS

Exponent Modify Entry Latch (01.66.80.1).

1. Turned on by an exit from:
   a. A fraction add operation when a carry out results from the addition or subtraction of the high-order PF and QF digits in the true mode.
   b. A zero fill operation when the high-order zero control latch is on.
2. Turns off the fraction add mode latch.
3. Provides gates for accomplishing various functions during trigger 24 and 25 time.
4. Turns on trigger 25.
5. Turned off by the exponent modify mode latch.

Trigger 24 (01.68.24.1).

1. Reads OR-5 into MAR (PE units).
2. Resets (clears) OR-1, OR-2, and OR-3.
3. Writes from MAR into OR-2, OR-3, and OR-5 bypassed.
4. Causes a *change mode* function which
   a. Forces an *I cycle reset.*
   b. Turns on the T/C trigger (true).
   c. Turns on the E cycle entry trigger.
   d. Turns off the zero fill mode latch.
5. Turns on the high/plus auxiliary latch if the basic high/plus trigger is on. The sign of PF is preserved in the auxiliary latch. The basic high/plus trigger is thereby freed for use during the exponent modify mode operation.
6. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Blocks MAR reset to prevent a VRC error.
2. Turns on the high/plus trigger.
3. Turns on the equal/zero trigger.
4. Turns on the 1st cycle trigger.
5. Exits to exponent modify mode by turning on the exponent modify mode latch.

Exponent Modify Mode (01/02)

The exponent modify mode is entered from the exponent modify entry operation. The exponent modify operation is essentially a basic 1620 add or subtract operation wherein the result exponent (PE) has a one added in the case of a normalizing shift right; in the case of a normalizing shift left, a number is subtracted from the result exponent (PE) equal to the number of left shifts, per CR-1, required to place a significant digit in the high-order position of the result fraction field (PE).

OBJECTIVES

1. Add one to the result exponent (PE) if a normalizing shift right is required as indicated by a carry out from a fraction add or subtract operation accomplished in the true mode.
2. Subtract the contents of CR-1 from the result exponent (PE), if a normalizing shift left operation was performed previously.
3. Exit to exponent modify exit.

FUNCTIONS

The add or subtract functions are carried out by triggers 21, 12, 13, 14, and the recomplement triggers, if required. Note that trigger 21 is used in place of trigger 11. Normally, eight memory cycles, four per digit, are required to modify the result exponent. Eight more memory cycles are required if a recomplement operation is required.

For a normalizing shift right operation, a one is placed in the D/B reg units on the first cycle for addition to the units position of PE per OR-2. On the second cycle, a C bit (zero) is set in the D/B reg units for addition to the tens position of PE. Any carries generated during the first add cycle are added to PE tens position on the second add cycle. If a carry out occurs on the second add cycle, the overflow/underflow latch is turned on to signal that the result exponent (PE) exceeds +99.

For a normalizing shift left operation, CR-1 is read out to MAR and the digit in MAR units is gated to the D/B reg units on the first cycle for subtraction from the units position of PE per OR-2. CR-1 is written back bypassed to retain the same value for use on the second cycle. On the second cycle, CR-1 is read out to MAR and the digit in MAR tens is gated to the D/B reg units for subtraction from the tens position of PE per OR-2. If subtracting the contents of CR-1 from PE results in an exponent of less than −99, the overflow/underflow and underflow/equal zero latches are turned on to signal an underflow condition. Note that subtracting CR-1 from a minus signed result exponent will cause a true operation, that is, the two minus figures are added without complementing. Therefore, if the addition of CR-1

and PE exceeds —99, a carry out in the true mode turns on the overflow/underflow and underflow/equal zero latches. The high/plus trigger is off because of the minus exponent.

TRIGGER FUNCTIONS

Exponent Modify Mode Latch (01.66.80.1).

1. Turned on during trigger 25 time of the exponent modify entry mode operation.
2. Turns on the decrement trigger (decrement).
3. Turns off trigger 11.
4. Blocks trigger 11 being turned on by trigger 14.
5. Turns on trigger 21.
6. Turned off by the exponent modify exit latch.

Trigger 21 (01.60.31.1). For a normalizing shift right operation (high-order zero control latch off and normalizing shift right latch on).

First cycle:

1. Resets D/B reg units.
2. Turns on the 1 bit latch in D/B reg units *(set 1 bit).*

Second cycle:

3. Resets D/B reg units.
4. Turns on C bit latch in D/B reg units *(set C bit).*
5. Turns on field mark no. 1 trigger to force an "end of field" indication.

For a normalizing shift left operation (high-order zero control latch on and normalizing shift right latch off).

First cycle:

6. Resets D/B reg units.
7. Forces a reset of MAR (trigger 21 basic function).
8. Reads CR-1 into MAR.
9. Turns off T/C trigger (complement).
10. Transfers (gates) MAR units to D/B reg units.
11. Writes back CR-1 bypassed.

Second cycle:

12. Resets D/B reg units.
13. Forces a reset of MAR.
14. Reads CR-1 into MAR.
15. Transfers (gates) MAR tens to D/B reg units.
16. Turns on field mark no. 1 trigger.
17. Writes back CR-1 bypassed.
18. Turns on trigger 12.

For the functions of triggers 12, 13 and other functions of trigger 14, the recomplement triggers, if needed, and the auxiliary triggers associated with a basic add or subtract operation, see the Manual of Instruction (Form 227-5647). For Function charts of the basic operations, see the Instructional System Diagrams (Form 227-5631).

Trigger 14 (01.60.14.1). For last add cycle:

1. Exits to exponent modify exit by turning on the exponent modify exit latch.
2. Turns on the overflow/underflow latch if the operation is in the true mode, a carry out occurs (PE > +99), and the high/plus trigger is on (plus exponent).
3. Turns on the overflow/underflow and underflow/equal zero latches if the operation is in the true mode, a carry out occurs (PE < —99), and the high plus trigger is off (minus exponent).

Exponent Modify Exit (01/02)

OBJECTIVES

The exponent modify exit function is a control and address set up operation which prepares for the shift mode (right and $\bar{1}$ fill) function that follows and also determines which function is to follow. The following function can be a digit force mode operation, a shift mode (right and $\bar{1}$ fill) operation or an exit to I cycle entry.

FUNCTIONS

The address in OR-2 is placed in PR-3 bypassed. PR-3 then contains the address of the units digit of PF. The address in OR-2 is placed in PR-2 decremented. PR-2 then contains the address of the tens digit of PF. The operation then exits to the function determined by the status of the overflow/underflow, underflow/equal zero, and normalizing shift right latches.

TRIGGER FUNCTIONS

Exponent Modify Exit Latch (01.66.81.1).

1. Turned on during trigger 14 time of the last exponent modify cycle *(last add cycle).*
2. Turns off the exponent modify mode latch.
3. Provides gates for various functions during trigger 24 and 25 time.
4. Turns on trigger 24.

Trigger 24 (01.68.24.1).

1. Reads OR-2 into MAR (PF units).
2. Writes back OR-2 bypassed.
3. Writes into PR-3 from MAR, bypassed (PF units).
4. Turns off the high/plus trigger.
5. Turns off field mark no. 1 and no. 2 triggers.
6. Turns on the 1st cycle trigger.
7. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Reads OR-2 into MAR (PF units).
2. Writes into PR-2 from MAR decremented. This places the address of the tens position of PF in PR-2 for use in the shift mode (right and $\bar{1}$ fill) operation.
3. Turns on the high/plus trigger if the high/plus auxiliary latch is on. The sign of PF was saved in the high/plus auxiliary latch during the exponent modify entry operation.

For a normalizing shift right operation:

4. Exits to shift mode (right and $\bar{1}$ fill) if neither the overflow/underflow nor the underflow/equal zero latch is on and the normalizing shift right latch is on.
5. Exits to digit force mode if either the overflow/underflow or the underflow/equal zero latch is on.

For a normalizing shift left operation:

6. Exits to I cycle entry if neither the overflow/underflow or the underflow/equal zero latch is on and the normalizing shift right latch is off.
7. Same as item 5.

Shift Mode (Right and $\bar{1}$ Fill)

OBJECTIVES

1. Shift the PF one position to the right.
2. Place a $\bar{1}$ in the high-order position of the PF field.

FUNCTIONS

This is essentially a transmit field operation in which the tens position digit in the PF field per PR-2 is transmitted to the units position of the PF field, the hundreds position digit is transmitted to the tens position just vacated, etc., until the end of the field is reached. When the original high-order position digit is transmitted, the field mark flag bit is removed. A $\bar{1}$ (for the carry) is forced into the high-order position vacated on the previous digit transmission cycle. The operation exits to I cycle entry following the $\bar{1}$ force operation.

TRIGGER FUNCTIONS

Shift Entry Latch (01.66.50.1).

1. Turned on during trigger 25 time of the exponent modify exit operation.
2. Turns on the decrement trigger (decrement).
3. Turns on the 1st cycle trigger.
4. Turns off field mark no. 1 and no. 2 triggers.
5. Turns on the shift mode latch.
6. Turned off by trigger 24.

Shift Mode Latch (01.66.50.1).

1. Provides gates for performing various functions during triggers 24 and 25 time.
2. Turns on trigger 24.
3. Turned off by *FP reset.*

Trigger 24 (01.68.24.1).

1. Reads out of memory per PR-2 and stores the digit in MDR.
2. Turns on field mark no. 1 trigger if an MDR F bit is present. Notice that PF could be a two digit field.
3. Turns off field mark no. 1 trigger if the force flag one latch is on.
4. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Blocks the reset of MBR *(Read Y).*
2. Reads out of memory per PR-3 with either the odd or even sense amplifiers blocked *(Read Y),* depending on whether the PR-3 address is odd or even, to clear the memory location.
3. On first cycle set or reset the F bit latch in MDR (set flag – clear flag) depends upon the status of the high/plus trigger, for sign designation of PF.
4. Clears (resets) an MDR F bit (clear flag) on every cycle after the first cycle.
5. Turns on the force flag one latch if field mark no. 1 is on.
6. Transfers the contents of MDR to MBR *(Read Y)* and writes the contents of MBR into memory per PR-3.
7. Writes back PR-3 decremented.
8. Turns off the 1st cycle trigger (W2-D3).
9. If the force flag one latch is on and the field mark no. 1 trigger is off:
   a. Forces a reset of MDR regardless of *Read Y.*
   b. Turns on the 1 bit and flag bit latches in MDR.
   c. Transfers the contents of MDR to MBR *(Read Y)* and writes the contents of MBR ($\bar{1}$) into memory per PR-3.
   d. Writes back PR-3 decremented.
   e. Exits to I cycle entry.

Digit Force Mode

The digit force mode is entered from a fraction add mode operation or an exponent modify mode exit operation.

OBJECTIVES

This mode accomplishes one of two functions depending upon the status of various triggers and latches when the mode is entered.

1. Machine zero ($\bar{0}00 - - - 0\bar{9}\bar{9}$) is forced if:
   a. During a floating arithmetic add or subtract operation, the resulting sum or difference of the fraction is zero (underflow/equal zero latch on).
   b. During a floating multiply or divide operation, the resulting product or quotient is zero (underflow/equal zero latch on).
   c. During add, subtract, multiply, or divide operation an exponent underflow occurs (overflow/underflow and underflow/equal zero latches on).

2. Machine infinity ($\bar{9}9 - - - - 9\bar{9}9$) is forced if:
   a. An exponent overflow occurs (PE > +99) during the exponent add or subtract function of a floating multiply or divide operation.
   b. An exponent overflow occurs (PE > +99) during the exponent modify function of a floating add, subtract, or divide operation.

Notice that multiply is not included in item 2b. This is because the exponent modify function, if required for a multiply operation, subtracts one from the exponent. Subtracting one from an exponent cannot make the exponent exceed +99. Therefore, if an exponent overflow exists for a multiply operation, it will be detected during the exponent add operation. If, during the exponent add operation, the sum of the exponents (PE + QE) equals exactly 100, the exponent modify mode will, if modification is required, subtract one, thereby making the exponent 99 which is valid. The previously detected overflow condition is ignored and the digit force operation is not performed. For more information on this operation, see FLOATING MULTIPLY, EXPONENT ADD OR SUBTRACT, Trigger 14, item 5.

FUNCTIONS

The resulting PE and PF field is cleared and machine infinity or machine zero replaces the result digits. Notice that the PF field of machine infinity is signed plus or minus depending upon the status of the high/plus trigger. Machine zero always has a negative exponent and a positive fraction.

The modulo 3 counter latches and circuits used during the digit force mode operation prevent the turn off (reset) of the 1st cycle trigger until the two exponent digits (PE) and the units digit of the fraction (PF) have been set to the required value. This is primarily to prevent field mark no. 1 trigger from recognizing a flag bit other than the field mark of PF. It is possible for the following three flag bits to be encountered before the field mark of PF is read out: sign of PE, field mark of PE, and sign of PF.

TRIGGER FUNCTIONS

Digit Force Entry Latch (01.66.90.1).

1. Turned on by:
   a. Trigger 14 on the *last add cycle* of a fraction add mode operation if the equal/zero trigger is on *(zero result)* and it is not a true mode operation with a *carry out.*
   b. Trigger 25 of the exponent modify exit operation if the overflow/underflow or the underflow/equal zero latch is on.
2. Blocks the turn on of triggers 11, 21, 23, and 42.
3. Blocks the turn off (reset) of the 1st cycle trigger.
4. Turns on the 1st cycle trigger.
5. Turns off field mark no. 1 and no. 2 triggers.
6. Turns on the digit force mode latch.

Digit Force Mode Latch (01.66.90.1).

1. Provides gates for various functions with triggers 24 and 25.
2. Reads out of memory per OR-5 (PE units) and during:
   a. Trigger 24 time, stores the digit in MDR.
   b. Trigger 25 time, a *Read Y* function blocks the sense amplifiers, odd or even, therefore the digit read out of memory is lost.
3. Writes back OR-5 bypassed during trigger 24 time and decremented during trigger 25 time.

   NOTE: A read and write per OR-5 occurs during both trigger 24 and trigger 25 time.

4. Turns on trigger 24.
5. Turned off by FP reset.

Trigger 24 (01.68.24.1).

1. Reads out of memory per OR-5 (function of the digit force mode latch).
2. Turns on L1 and L2 modulo counter latches. The ON status of the L2 modulo counter latch blocks the reset of the 1st cycle trigger until R3 time of the third trigger 25 cycle.
3. Turns on the decrement trigger (decrement).
4. Turns on field mark no. 1 trigger if an MDR F bit is present during the fourth or subsequent trigger 24 cycles. The address in MAR on the fourth cycle is the address of the tens digit of PF.
5. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Reads out of memory per OR-5 (function of the digit force mode latch) with either the odd or even sense amplifiers blocked *(Read Y)*, depending on whether the OR-5 address is odd or even, to clear the memory location.
2. Resets MDR regardless of *Read Y.*

Forcing Machine Zero

First trigger 25 time:

3. Turns on the MDR F, C, 8, and 1 bit latches. This generates a −9 ($\overline{9}$) for the units digit of PE.
4. Transfers MDR to MBR *(Read Y)* and writes the contents of MBR into memory per OR-5.
5. Turns on the equal/zero trigger.

Second trigger 25 time:

6. Turns on the MDR F, C, 8, and 1 bit latches. This generates a field mark flag 9 ($\overline{9}$) for the tens position of PE.
7. Transfers MDR to MBR *(Read Y)* and writes the contents of MBR into memory per OR-5.

Third and subsequent trigger 25 times:

8. Turns on the MBR C bit latch. This generates zeros for the PF field.
9. Transfers MDR to MBR *(Read Y)* and writes the contents of MBR into memory per OR-5.
10. Turns off the 1st cycle trigger (W2 time).
11. On the *last digit force cycle* (field mark of PF reached during the previous trigger 24 time) turns on the MDR flag bit and C bit latches. This generates a field mark zero ($\overline{0}$) for the high-order position of PF. The C bit corrector will remove the C bit and place only the flag bit in memory.
12. Exit to I cycle entry.

Forcing Machine Infinity

First trigger 25 time:

13. Turns on the MDR C, 8, and 1 bit latches. This generates a +9 for the units position of PE.
14. Transfers MDR to MBR *(Read Y)*, and writes the contents of MBR into memory per OR-5.

Second trigger 25 time:

15. Turns on the MDR F, C, 8, and 1 bit latches. This generates a field mark 9 ($\overline{9}$) for the tens position of PE.
16. Transfers MDR to MBR *(Read Y)*, and writes the contents of MBR into memory per OR-5.

Third trigger 25 time:

17. Turns on the MDR C, 8, and 1 bit latches. This generates a 9 for the units position of PE.
18. Turns on the MDR F bit latch if the high/plus trigger (sign of PF) is off. This generates a flag bit to be added to the C, 8, and 1 bits for designating the sign of PF as being minus.
19. Transfers MDR to MBR *(Read Y)*, and writes the contents of MBR into memory per OR-5.
20. Turns off the 1st cycle trigger (W2 time).

Fourth and subsequent trigger 25 time:

21. The remainder of the PF field is filled with 9s with a field mark 9 ($\overline{9}$) placed in the high-order position of PF on the *last digit force cycle.*
22. Exit to I cycle entry if field mark no. 1 is on. If the overflow/underflow latch is on (forcing machine infinity) the exponent check latch (indicator code 15) is turned on to signal the overflow condition when the exit to I cycle entry takes place. If the console check switch is set to STOP, the computer is stopped. See the Exponent overflow and underflow latch Function chart, p. 54 (Form 227-5631).

Scan Mode (0)

Scan mode (0) is entered from fraction add mode when the operation is accomplished in the complement mode, the high-order zero control latch is on, and the equal/zero trigger is off. These conditions indicate that the high-order digit of PF (and possibly others) is a zero (high-order zero control latch on) but that not all of the digits are zeros (equal/zero trigger off).

OBJECTIVES

1. Scan the PF field per PR-2, searching for the first significant digit (not a zero).
2. Count the number of zeros encountered using CR-1 as a counter.

It should be noted that the CR-1 counter, units and tens, is reset to zero by being incremented or decremented during the scan mode (P or Q) that precedes the fraction add operation. It should be further noted that, if during the scan mode (P or Q), the field mark of PF or QF is encountered before CR-1 reaches zero, the operation exits to I cycle entry and does not proceed to fraction add and scan mode (0). CR-1 will then be reset on the first trigger 11 time of the next exponent add, subtract, or compare operation.

3. Retain the sign of PF in the scan minus latch, the status of which is controlled by the high/plus trigger. If PF is positive (high/plus on) the scan minus latch is turned off. If PF is negative (high/plus off) the scan minus latch is turned on.
4. Exit to shift mode (left).

FUNCTIONS

Scan mode (0) uses triggers 24 and 25. Trigger 24 reads out of memory per PR-2 and interrogates the character for a significant digit (not zero). Trigger 25 counts, by causing CR-1 to be incremented +1 on each cycle, the number of characters interrogated before the first significant digit is encountered.

TRIGGER FUNCTIONS

Scan Entry Latch (01.66.20.1).

1. Turned on by trigger 14 of the *last add cycle* when the fraction add operation is accomplished in the complement mode, the equal/zero trigger is off, and the high-order control latch is on.
2. Turns off field mark no. 1 and no. 2 triggers.
3. Turns on the 1st cycle trigger.
4. Turns on the scan mode latch.

Scan Mode Latch (01.66.20.1).

1. Turned on by the scan entry latch.
2. Provides gates for various functions with triggers 24 and 25.
3. Turns on trigger 24.
4. Turned off by the mode latch of the following operation.

NOTE: At the same time that the scan mode entry latch is turned on, the decrement trigger is turned off (increment), and the address in MAR per OR-2 is written into PR-2 and PR-3 incremented. Thus PR-2 and PR-3 contain the address of the high-order digit of PF at the end of trigger 14 time of the *last add cycle.*

1. Reads out of memory per PR-2 and stores the digit in MDR.
2. Turns on the scan minus latch if the high/plus trigger is off (negative PF). If the high/plus trigger is on (positive PF), the scan minus latch will be off at the end of trigger 24 time regardless of the presence of the MDR F bit (field mark of PF). The status of the scan minus latch is used during the shift left operation.
3. Turns on the significant digit latch if the character in MDR is not a zero.
4. Writes back PR-2 incremented.
5. Turns on trigger 25.

Trigger 25 (01.68.24.1).

For all cycles except last zero scan:

1. Reads CR-1 into MAR (00000 on first cycle).
2. Writes back CR-1 incremented. CR-1 is used as a counter to count the number of zeros encountered during the scan mode (zero) operation. The resulting count in CR-1 is subtracted from PE during the exponent modify mode.
3. Turns off the 1st cycle trigger.

For the *Last Zero Scan* cycle:

4. Turns on the decrement trigger (decrement) if the significant digit latch is on.

Last Zero Scan is developed by the AND that turns on the decrement trigger.

5. Reads PR-2 into MAR.
6. Writes back PR-2 decremented. At the end of this cycle the address in PR-2 is the address of the first significant digit (not a zero) encountered during the scan operation.
7. Exit to shift mode (left).

Shift Mode (Left) Operation Codes 01/02

Shift mode (left) is entered from the scan mode (0) when a significant digit is encountered (significant digit latch on) during the scan operation.

OBJECTIVES

1. Starting with the first significant PF digit per PR-2, shift it and the remaining lower-order digits in PF to the high-order and subsequent lower-order positions of the result PF field per PR-3.
2. Set a field mark flag bit on the first cycle.
3. Exit to zero fill mode when the end of the PF field per PR-2 is reached.

FUNCTIONS

Starting with the first significant digit, the digits are read out of memory per PR-2 during trigger 24 time. The digits are written back into memory per PR-3 starting with the high-order position of the result PF field. This read out per PR-2 and write back per PR-3 of the PF digits accomplishes a left shift of the PF digits.

The method by which the computer determines when it has reached the low-order (units) position of the PF field differs depending upon the sign of the PF field. The sign flag bit of a negative PF is used to end the shift operation. The field mark flag bit of the PE field is used to end the left shift of a positive PF. A positive PF field results in an *extra shift cycle* because the tens digit of the PE must be read out and interrogated for its field mark flag bit before the left shift is terminated. The details of functions for ending the shift operation involving positive and negative PF fields is given under trigger 25.

TRIGGER FUNCTIONS

Shift Entry Latch (01.66.50.1).

1. Turned on by trigger 25 during the *last zero scan* cycle.
2. Turns on the decrement trigger (decrement).
3. Turns on the 1st cycle trigger.
4. Turns off field mark no. 1 and no. 2 triggers.
5. Turns on the shift mode latch.

Shift Mode Latch (01.66.50.1)

1. Turns off the scan mode latch.
2. Provides gates for various functions with triggers 24 and 25.
3. Turns on trigger 24.

Trigger 24 (01.68.24.1). When the shift mode (left) is entered, PR-2 contains the address of the first significant digit encountered by the preceding scan operation. PR-3 contains the address of the high-order position of PF.

1. Reads out of memory per PR-2 and stores the digit in MDR.
2. Turns off the decrement trigger (increment).
3. Turns on field mark no. 1 trigger if an MDR F bit is present. It should be noted that the first significant digit encountered during the scan operation could be the PF units position digit, and if the PF is negative a flag bit is associated with it. Therefore field mark no. 1 trigger can be turned on during the first trigger 24 time. In this case, the units digit will be transmitted (left shift) to the high-order position of PF.
4. Turns on trigger 25.

Trigger 25 (01.68.24.1).

For a negative PF:

1. Blocks the reset of MDR *(Read Y).*
2. Reads out of memory per PR-3 with either the odd or even sense amplifiers blocked *(Read Y),* depending on whether the PR-3 address is odd or even, to clear the memory location.
3. Turns on the MDR F bit latch to set the field mark flag bit for the PF on first cycle only.
4. Clears the MDR flag bit on all cycles after the first.
5. Transfers MDR to MBR *(Read Y)* and writes the contents of MBR into memory per PR-3.
6. Writes back PR-3 incremented.
7. Turns off the 1st cycle trigger (W2-D3).
8. Exit to zero fill mode if field mark no. 1 trigger is on.

With a negative PF, field mark no. 1 trigger is turned on by the sign flag bit of PF. The flag bit is removed when the units digit is transmitted (shifted left). The sign flag bit will be placed in the units position of PF by the zero fill operation that follows the shift (left) operation.

For a positive PF:

There is no flag bit in the units position of a positively signed PF field. Therefore, during a left shift operation there is no way for the PF field to signal the computer that the end of the PF field has been reached. However, the exponent (PE) does have a field mark flag bit associated with its tens position digit. This tens position digit is the next digit immediately to the right of the units digit of the PF field. This PE field mark is used to control the last shift cycle. When *Read Y* is blocked, the sense amplifiers are not blocked, and this allows the normal write back of MBR into memory per PR-3. The address in MAR is written back into PR-3 bypassed thus retaining the address of the next digit to the right of the last digit transmitted (shifted left). PR-3 is used with the zero fill operation that follows. The operation then exits to the zero fill mode. Trigger 25, functions 1 through 8, given under negative PF apply to a positive PF with the exception of the last left shift cycle which is explained previously in this paragraph.

Zero Fill Mode

Zero fill mode is entered from the shift mode left operation when the required number of digits have been shifted.

OBJECTIVE

1. Place a zero (C bit) in PF locations vacated by the shift left operation.
2. Place a flag zero in the units position of the PF field, if the original PF field is negative.
3. Exit to the exponent modify entry mode when all vacated positions are filled with zeros.

FUNCTIONS

The PF field is read out one digit at a time per PR-3 during trigger 24 time and interrogated for the presence of an MDR F bit. During trigger 25 time, the PF field is read out one digit at a time per PR-3, and a zero (C bit) is written back into memory replacing the digit. A flag zero is placed in the units position of a negative PF field.

TRIGGER FUNCTIONS

Zero Fill Mode Latch (01.66.60.1).

1. Turned on during trigger 25 time of the shift mode (left) operation when field mark no. 1 trigger is on.
2. Provides gates to accomplish various functions during trigger 24 and 25 time.
3. Turns on trigger 24.
4. Turned off by trigger 24 ANDed with the exponent modify entry latch.

Trigger 24 (01.68.24.1).

1. Reads out of memory per PR-3 and stores the digit in MDR. At the start of this operation, PR-3 contains the address of the next digit to the right of the last digit transmitted (shifted left) during the shift mode operation.
2. Turns on field mark no. 2 trigger if an MDR F bit is present. The MDR F bit will be present when the tens digit of the PE is read out for a positive PF field. Note that the 1st cycle trigger is off as a result of the preceding shift mode (left) operation and is not turned on when entering the zero fill mode. Thus, if the first digit read out is the units digit of a negative PF, field mark no. 2 trigger can be turned on.

3. Writes back PR-3 bypassed to retain the address for use by trigger 25 in replacing the digit with a zero (C bit).
4. Turns on trigger 25.

Trigger 25 (01.68.24.1).

1. Reads out of memory per PR-3.

For a negative PF result:

2. The *Read Y* causes either the odd or even sense amplifiers to be blocked, depending upon whether the address in PR-3 is odd or even, to clear the memory address.
3. Forces a reset of MDR regardless of *Read Y*.
4. Turns on the MDR C bit latch.
5. Turns on the MDR F bit latch for sign designation of PF if field mark no. 2 trigger is on.
6. Transfers MDR to MBR *(Read Y)* and writes the contents of MBR into memory per PR-3. If both the MDR C bit and MDR F bit latches are on, the C bit correction circuits will strip out the C bit allowing only the F bit to reach MBR.
7. Writes back PR-3 incremented.
8. Exits to exponent modify entry mode if field mark no. 2 trigger is on.

For a positive PF result:

9. If field mark no. 2 trigger is off:
   a. Reads out of memory per PR-3 with either the odd or the even sense amplifiers blocked *(Read Y)*, depending on whether the PR-3 address is odd or even, to clear the memory location.
   b. Forces a reset of MDR regardless of *Read Y*.
   c. Turns on the MDR C bit latch.
   d. Transfers MDR to MBR *(Read Y)* and writes the contents of MBR into memory per PR-3.
   e. Writes back PR-3 incremented.
10. If field mark no. 2 trigger is on:
   a. Blocks: *Read Y*, the MDR C bit latch turn on, the MDR reset, and the set flag functions.
   b. Reads PR-3 into MAR.
   c. Writes back into PR-3 from MAR incremented.
   d. Exits to exponent modify mode.

The tens position of PE is written back into memory per PR-3 and therefore is not lost.

Section 4 Floating Point Arithmetic Examples

This section contains data flow charts and examples for floating point arithmetic. The examples are representative of various floating point arithmetic problems and are intended to show the fundamental operations required by various value and sign configurations of fractions and exponents.

Figure 4-1 is a data flow diagram for floating multiply and divide. The dashed lines indicate the path(s) taken by specific examples. The numbers (1, 2, etc.) inside the circles, or oblongs, and inserted in the dashed lines are keyed to the same numbered examples in the text.

Floating Multiply Examples

Example 1. No Exponent Modify Required

$\bar{3}45\ \bar{0}7$	P	L = 3
$\bar{4}32\ \bar{0}4$	Q	L = 3
690		2L = 6
1035		
1380		
$\bar{1}49040\ \bar{1}1$	=6 product area positions =2L	
	No exponent modify required	
$\bar{1}49\ \bar{1}1$	Final Result	

Exponent Add. Add QE per OR-1 to PE per OR-2, replacing PE with the result sum. At the end of this operation, OR-1 contains the address of QF units (multiplier) and OR-2, OR-3, PR-2, and PR-3 contain the address of PE units (multiplicand).

Multiply Mode. Basic multiply function (PF × QF).

Exponent Modify Entry (03/09). Control and address set up operation. For details see EXPONENT MODIFY ENTRY (03/09) in Section 3.

Exponent Modify Mode (03/09). For this example, zeros (C bits) are subtracted from the result exponent (PE) because the exponent modify required latch is off. Adding zeros does not alter the result exponent (PE). No exponent overflow occurs.

Exponent Modify Exit (03/09). Control and address set up operation. Write address 99 — L into OR-1 because the exponent modify required latch is off. For details see EXPONENT MODIFY EXIT (03/09) in Section 3.

Result Transmit. Transmit the product from the product area per OR-1 starting with position 99 — L which is position 00096, the 9 in this example, and continuing until the field mark flag of the high-order product digit in the product area ($\bar{1}$ in 00094 for this example) stops the operation.

Exit to I cycle entry for the next instruction in sequence.

Example 2. Exponent Modify Required

$\bar{1}23\ \bar{0}2$	P	L = 3
$\bar{2}46\ \bar{0}4$	Q	L = 3
738		2L = 6
492		
246		
$\bar{0}\bar{0}30258\ \bar{0}6$	=5 product area positions ≠2L (high-order zero). Exponent modify required (high-order zero)	
$\bar{3}02\ \bar{0}5$	Final Result	

Exponent Add. Add QE per OR-1 to PE per OR-2 replacing PE with the result sum. At the end of this operation, OR-1 contains the address of QF units (multiplier) and OR-2, OR-3, PR-2, and PR-3 contain the address of PF units (multiplicand).

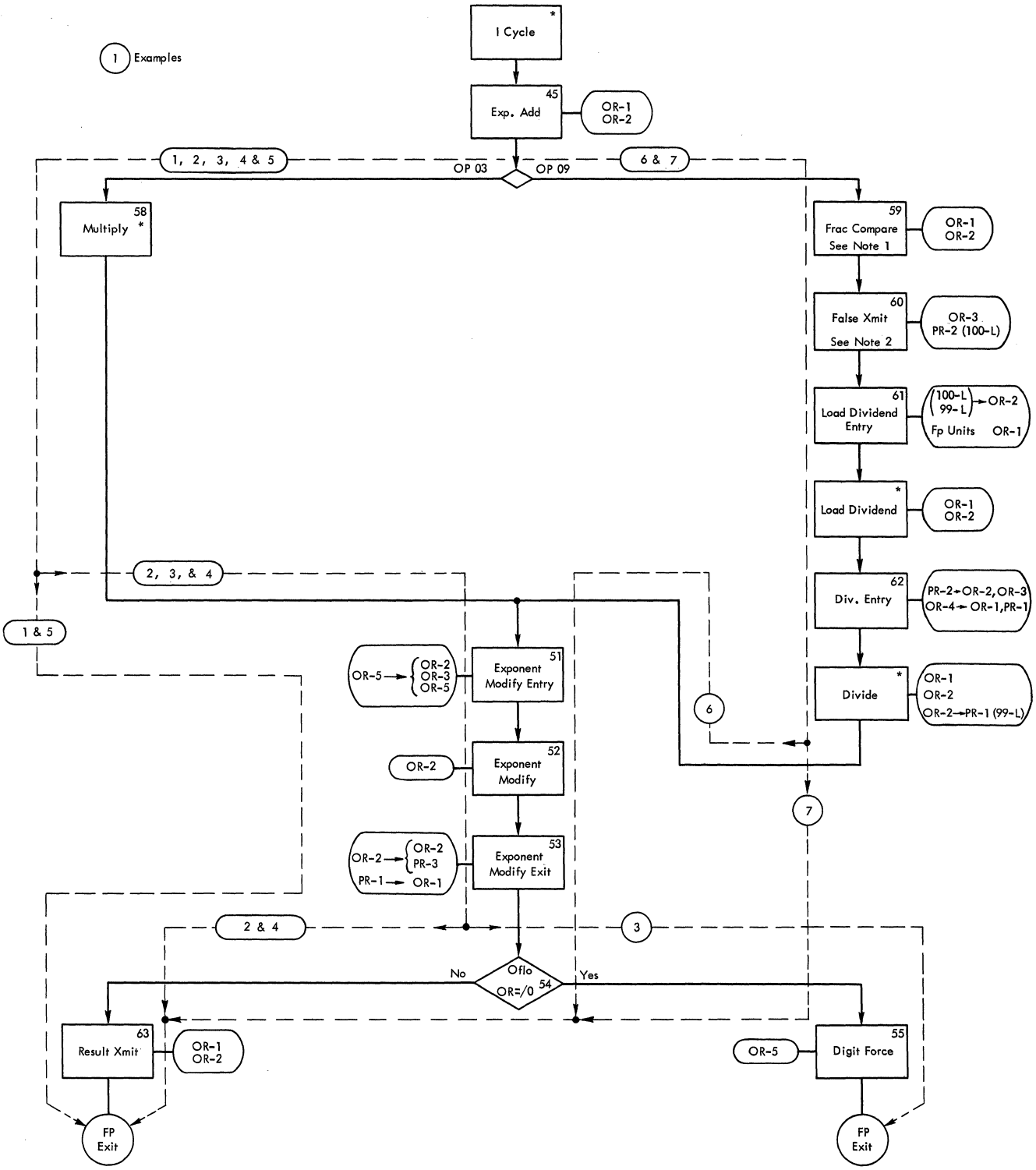
Multiply Mode. Basic multiply function (PF× QF). Turn on exponent modify required latch.

Exponent Modify Entry. Control and address set up operation. For details see EXPONENT MODIFY ENTRY (03/09) in Section 3.

Exponent Modify Mode (03/09). Subtract "one" from the result exponent (PE) because the exponent modify required latch is on. No exponent overflow occurs.

Exponent Modify Exit (03/09). Control and address set up operation. Write address 100 — L in OR-1 because the exponent modify required latch is on. For details see EXPONENT MODIFY EXIT (03/09) in Section 3.

Result Transmit. Transmit the product from the product area per OR-1 to the result fraction (PF) address per OR-2, starting with position 100 — L which is position 00097, the 2 in this example, and continuing



-*- See Basic Function Charts

Note 1. Fraction compare determines the address for load dividend
if P > Q (HP On) 100-L
P < Q 99-L

Note 2. False Xmit sets up the address
100-L In PR2

Figure 4-1. Data Flow – Multiply and Divide

until the field mark flag bit of the high-order product digit in the product area ($\overline{3}$ in 00095 for this example) stops the operation. It should be noted that a field mark flag bit is placed with the zero($\overline{0}$) next left of the flag three ($\overline{3}$). Because the first flag encountered stops the operation, the second flag has no effect but does remain in the product area.

Exit to I cycle entry for the next instruction in sequence.

Example 3. Digit Force — Machine Infinity

$\overline{3}45\ \overline{4}3$	P	L = 3
$\overline{4}32\ \overline{6}4$	Q	L = 3
690 $\overline{0}7$	CO = Exponent overflow	2L = 6
1035		
1380		
$\overline{1}49040\ \overline{0}7$	= 6 product area positions = 2L	
	No exponent modify required	
$\overline{9}99\ \overline{9}9$	Final Result	

Exponent Add. Add QE per OR-1 to PE per OR-2, replacing PE with the result sum. At the end of this operation, OR-1 contains the address of QF units (multiplier) and OR-2, OR-3, PR-2, and PR-3 contain the address of PF units (multiplicand). The overflow/underflow latch is turned on to indicate the exponent overflow.

Multiply Mode. Basic multiply function (PF × QF).

Exponent Modify Entry (03/09). Control and address set up operation. For details see EXPONENT MODIFY ENTRY (03/09) in Section 3.

Exponent Modify Mode (03/09). For this example, zeros (C bits) are subtracted from the result exponent (PE) because the exponent modify required latch is off. Adding zeros does not alter the result exponent (PE). No exponent overflow occurs during the exponent modify mode.

Exponent Modify Exit (03/09). Control and address set up operation. Write address 99 — L into OR-1 because the exponent modify required latch is off. For details see EXPONENT MODIFY EXIT (03/09) in Section 3.

Digit Force Mode. Force machine infinity ($\overline{9}99\ \overline{9}9$) because of the exponent overflow detected during the exponent add operation.

Exit to I cycle entry for the next instruction in sequence.

Example 4. Exponent Overflow — Modify PE to 99

$\overline{1}23\ \overline{3}8$	P	L = 3
$\overline{2}46\ \overline{6}2$	Q	L = 3
738 $\overline{0}0$		2L = 6
492	Overflow/underflow latch and	
246	overflow correct latch turned on	
$\overline{0}\overline{3}0258\ \overline{0}0$	during exponent add because of	
	the carry out from exponent add.	
	= 5 product area positions ≠ 2L	
	Exponent modify required	
	(high-order zero)	
$\overline{3}02\ \overline{9}9$	Final Result	

Exponent Add. Add QE per OR-1 to PE per OR-2, replacing PE with the result sum ($\overline{0}0$ in this example). The overflow/underflow latch is turned on because of the carry out. The overflow correct latch is turned on because the sum is exactly 100 and its sign is positive (high/plus on).

Multiply Mode. Basic multiply function (PF × QF).

Exponent Modify Entry (03/09). Control and address set up operation. For details see EXPONENT MODIFY ENTRY (03/09) in Section 3.

Exponent Modify Mode (03/09). For this example, a one is subtracted from the result exponent (PE = $\overline{0}0$) because the exponent modify required latch is on. The exponent thus becomes 99 (100 — 1 = 99) which is a valid exponent, and the overflow/underflow latch is turned off (see the exponent overflow and underflow latch Function chart p. 54 of Form 227-5631).

Exponent Modify Exit (03/09). Control and address set up operation. Write address 100 — L in OR-1 because the exponent modify required latch is on. For details see EXPONENT MODIFY EXIT (03/09) in Section 3.

Result Transmit. Transmit the product from the product area per OR-1 to the result fraction (PF) address per OR-2, starting with position 100 — L which is position 00097, the 2 in this example, and continuing until the field mark flag bit of the high-order product digit in the product area ($\overline{3}$ in 00095 for this example) stops the operation.

Exit to I cycle entry for the next instruction in sequence.

Example 5. Special Case 999 × 199

$\overline{9}99\ \overline{0}1$	P	L = 3
$\overline{1}99\ \overline{0}1$	Q	L = 3
8991		2L = 6
8991		
999		
$\overline{1}\overline{9}8801\ \overline{0}2$		
$\overline{1}98\ \overline{0}2$	Final Result	
00000000		
81	9 × 9	
00081		
81	9 × 9	
000891		
81	9 × 9	
0008991		
81	9 × 9	
0009801		
81	9 × 9	
00017901		
81	9 × 9	
00098901		
09	1 × 9	
00099801		
09	1 × 9	
000108801		
09	1 × 9	Last Multiply Cycle
$\overline{1}\overline{9}8801$	Product	

Note the carry

This zero is in D/B reg units during trigger 38 time

Exponent Add. Add QE per OR-1 to PE per OR-2 replacing PE with the result sum. At the end of this operation OR-1 contains the address of QF units (multiplier) and OR-2, OR-3, PR-2, and PR-3 contain the address of PF units (multiplicand).

Multiply Mode. These particular operands cause an 09 to be read out (of the multiply table) and set in D/B reg tens and units during trigger 35 time of the last multiply cycle. Trigger 37 resets D/B reg units and transfers D/B reg tens to D/B reg units. This zero in D/B reg units during trigger 38 time satisfies the conditions necessary for turning on the exponent modify required latch and for setting a field mark flag bit with the digit that is immediately right of the high-order position of the product. However, during the previous trigger 40 time, a carry was developed so that a one was placed in the high-order position of the product. During the next trigger 41 time, a field mark flag bit is set in the high-order position of the product. There are now two field mark flag bits in the product, one with the high-order digit and one with the digit immediately to the right of the high-order digit. It is necessary to do the following:

1. Turn off the exponent modify required latch during the last trigger 39 time before exiting to the exponent modify mode to prevent changing the exponent PE. This is accomplished by turning on the floating multiply correct flag latch during trigger 39 time.
2. Clear the flag from the next to high-order position during the result transmit mode, and block *FP exit* to allow the high-order digit to be transferred.
3. Turn off the multiply correct flag latch to allow the normal set flag for field definition and FP exit to take place during the result transmit mode operation.

Exponent Modify Entry (03/09). Control and address set up operation. For details see EXPONENT MODIFY ENTRY (03/09) in Section 3.

Exponent Modify Mode (03/09). For this example, zeros (C bits) are subtracted from the result exponent (PE) because the exponent modify required latch is off (see item 1 under MULTIPLY MODE). Adding zeros does not alter the result exponent (PE). No exponent overflow occurs.

Exponent Modify Exit (03/09). Control and address set up operation. Write address 99 — L into OR-1 because the exponent modify required latch is off. For details see EXPONENT MODIFY EXIT (03/09) in Section 3.

Result Transmit. In this example, the first field mark flag bit encountered by trigger 26 during the transmit operation is associated with the digit immediately right of the high-order digit, and is not the actual field mark flag bit of the correct product. This flag is cleared by trigger 27 because the multiply correct flag latch is on. Because the floating multiply correct flag latch is on, the *FP exit* to I cycle during trigger 27 time is blocked and trigger 26 is turned on for an extra transmit cycle to read out the actual high-order product digit with its associated field mark flag bit. The floating multiply correct flag latch is turned off during this extra trigger 26 cycle. The actual high-order digit is transmitted to the PF field per OR-2. The operation then exits to I cycle entry for the next operation in sequence.

Floating Divide Examples

Example 1. Exponent Modify Required

$\bar{1}46\ \bar{0}4$	P	Dividend
$\div\ \bar{1}20\ \bar{0}2$	Q	Divisor
$\bar{1}21\ \bar{0}3$	Final Result	

Exponent Subtract. $\bar{0}4 - \bar{0}2 = \bar{0}2$

Fraction Compare. Compare the absolute values of PF and QF (PF — QF).

$\bar{1}46$	$\bar{1}46$	High/plus remains on
$-\bar{1}20$	$\bar{8}70$	Exponent modify required
26	CO 026	

False Transmit. PR-2 set to 100 — L. In this example, 100 — L = 00097. The exponent modify required latch is turned on because the high/plus trigger is on.

97	98	99	100	PR-2
1	4	6		OR-3

Load Dividend Entry. Control and address set up operation. Transfer the address in PR-2 (100 — L = 00097) to OR-2 bypassed. Transfer the address in PR-3 (PF units) to OR-1.

Load Dividend. Basic load dividend operation, transmits PF per OR-1 to the product area (100—L=00097) per OR-2.

95	96	97	98	99	Product Area per OR-2
1	4	6	0	0	PF per OR-1

Divide Entry. Control and address set up operation. Transfer the address in PR-2 (100 — L = 00097) to OR-2 and OR-3 for use during the divide operation. Transfer the address in OR-4(QF units) to OR-1 and PR-1 for use during the divide operation.

Divide. Basic divide operation. Start division by subtracting the units digit of QF per OR-1 from the product area per OR-2 (100 — L = 00097).

First divide cycle:

95	96	97	98	99	Product Area per OR-2
1	4	6	0	0	
1	2	0			QF per OR-1
0	2	6			

Last divide cycle:

94	95	96	97	98	99	Product Area
$\bar{1}$	2	1	0	8	0	Quotient and Remainder

Transfer the address in OR-2 (100 — L) to PR-1 decremented (99 — L = 00096).

Exponent Modify Entry (03/09). Control and address set up operation. Transfer the address in OR-5 (PE units) to OR-2 and OR-3.

Exponent Modify Mode (03/09). Add one to PE ($\bar{0}2 + \bar{0}1 = \bar{0}3$) because the exponent modify required latch is on. No exponent overflow occurs.

Exponent Modify Exit (03/09). Control and address set up operation. The address in OR-2 at the end of the exponent modify mode operation is the address of PF units. Transfer the address in PR-1 to OR-1. The address in PR-1 (99 — L) was placed there during trigger 14 time of the *last divide add* cycle of the basic divide operation. OR-1 is thus set for transmitting the units quotient digit from the product area to the PF field during the result transmit operation.

Result Transmit. Transmit the quotient from the product area per OR-1 to the fraction P (PF) address per OR-2. Exit to I cycle entry for the next instruction in sequence.

Example 2. No Exponent Modify Required

$\bar{1}16\ \bar{0}4$	P	Dividend
$\div\bar{1}20\ \bar{0}2$	Q	Divisor
$\bar{9}66\ \bar{0}2$	Final Result	

Exponent Subtract. $\bar{0}4 - \bar{0}2 = \bar{0}2$

Fraction Compare. Compare the absolute values of PF and QF (PF — QF).

$\bar{1}16$	$\bar{1}16$	High/plus off
$-\bar{1}20$	$\bar{8}70$	No exponent modify required
$\bar{9}96$	No CO $\bar{9}96$	

False Transmit. PR-2 set to 100 — L. In this example 100 — L = 00097. The exponent modify required latch is not turned on because the high/plus trigger is off.

97	98	99	100	PR-2
$\bar{1}$	4	6		OR-3

Load Dividend Entry. Control and address set up operation. Transfer the address in PR-2 (100 — L = 00097) to OR-2 decremented (99 — L = 00096). Transfer the address in PR-3 (PF units) to OR-1.

Load Dividend. Basic load dividend operation, transmits PF per OR-1 to the product area (99—L=00096) per OR-2.

94	95	96	97	98	99	Product area per OR-2
$\bar{1}$	1	6	0	0	0	PF per OR-1

Divide Entry. Control and address set up operation. Transfer the address in PR-2 (100 — L = 00097) to OR-2 and OR-3 for use during the divide operation. Transfer the address in OR-4 (QF units) to OR-1 and PR-1 for use during the divide operation.

Divide. Basic divide operation. Start division by subtracting the units digit of QF per OR-1 from the product area per OR-2 (100 — L = 00097).

First divide cycle:

94	95	96	97	98	99	
1	1	6	0	0	0	Product Area per OR-2
	1	2	0			QF per OR-1
	9	4				

Last divide cycle:

94	95	96	97	98	99	
$\bar{9}$	6	6	0	8	0	Quotient and Remainder

Transfer the address in OR-2 (100 — L) to PR-1 decremented (99 — L = 00096).

Exponent Modify Entry (03/09). Control and address set up operation. Transfer the address in OR-5 (PE units) to OR-2 and OR-3.

Exponent Modify Mode (03/09). The exponent is not altered because the exponent modify required latch is off. No exponent overflow occurs.

Exponent Modify Exit (03/09). Control and address set up operation. The address in OR-2 at the end of the exponent modify mode operation is the address of PF units. Transfer the address in PR-1 to OR-1. The address in PR-1 (99 — L) was placed there during trigger 14 time of the *last divide add* cycle of the basic divide operation. OR-1 is thus set for use during the result transmit operation.

Result Transmit. Transmit the quotient from the product area per OR-1 to the PF address per OR-2.

Exit to I cycle entry for the next instruction in sequence.

Floating Add Examples

Figure 4-2 is a data flow diagram for floating add and subtract. The dashed lines indicate the path(s) taken by specific examples. The numbers (1, 2, etc.) inside the circles, or oblongs, and inserted in the dashed lines are keyed to the same numbered examples in the text.

Examples 1 through 5 are typical problems showing the various data flow paths taken because of the exponent configuration (value and sign).

Examples 6 through 11 are typical problems showing the various data flow paths taken because of the fraction configuration (value and sign).

Example 1. PE = QE/d = 0

$\bar{1}23\ \bar{0}4$	P	1230
$\bar{2}46\ \bar{0}4$	Q	2460
$\bar{3}69\ \bar{0}4$	Result	3690 ← Available result field

Exponent Compare. PE = QE or d = 0, high/plus off, equal/zero on (no decimal alignment needed).

Fraction Add. True, no carry out, equal/zero off (no normalizing required). Exit to I cycle entry for the next instruction in sequence.

Example 2. (PE > QE) Scan Q — Fraction Add

$\bar{1}23\ \bar{0}6$	P	123000
$\bar{2}46\ \bar{0}4$	Q	2000
$\bar{1}25\ \bar{0}6$	Result	125000 ← Available result field

Exponent Compare. PE > QE, high/plus on, equal/zero off (QF must be shifted right to align decimals).

Scan Mode(Q). CR-1 contains the algebraic difference between PE and QE, a 2 in this example. The QF field must be shifted right two positions to align the decimal points. This shift is accomplished by decrementing OR-1 the number of places indicated by CR-1 (2). In this example, OR-1 will, after the scan, contain the address of the $\bar{2}$ in QF which is added to the 3 in PF during fraction add.

Fraction Add. True, no carry out, equal/zero off (no normalizing required). Exit to I cycle entry for the next instruction in sequence.

Example 3. (PE > QE) Scan Q — FP Exit

$\bar{1}23\ \bar{0}8$	P	12300000
$\bar{2}46\ \bar{0}3$	Q	246
$\bar{1}23\ \bar{0}8$	Result	12300246 ← Available result field

Exponent Compare. PE > QE, high/plus on, equal/zero off (QF must be shifted right to align decimals).

Scan Mode (Q). CR-1 contains the algebraic difference between PE and QE, a 5 in this example. The QF field must be shifted right five positions to align the decimal points. The shift is started by decrementing OR-1, however the field mark of QF is reached prior to CR-1 reaching zero (MAR = 0/CR-1 = 0). This indicates

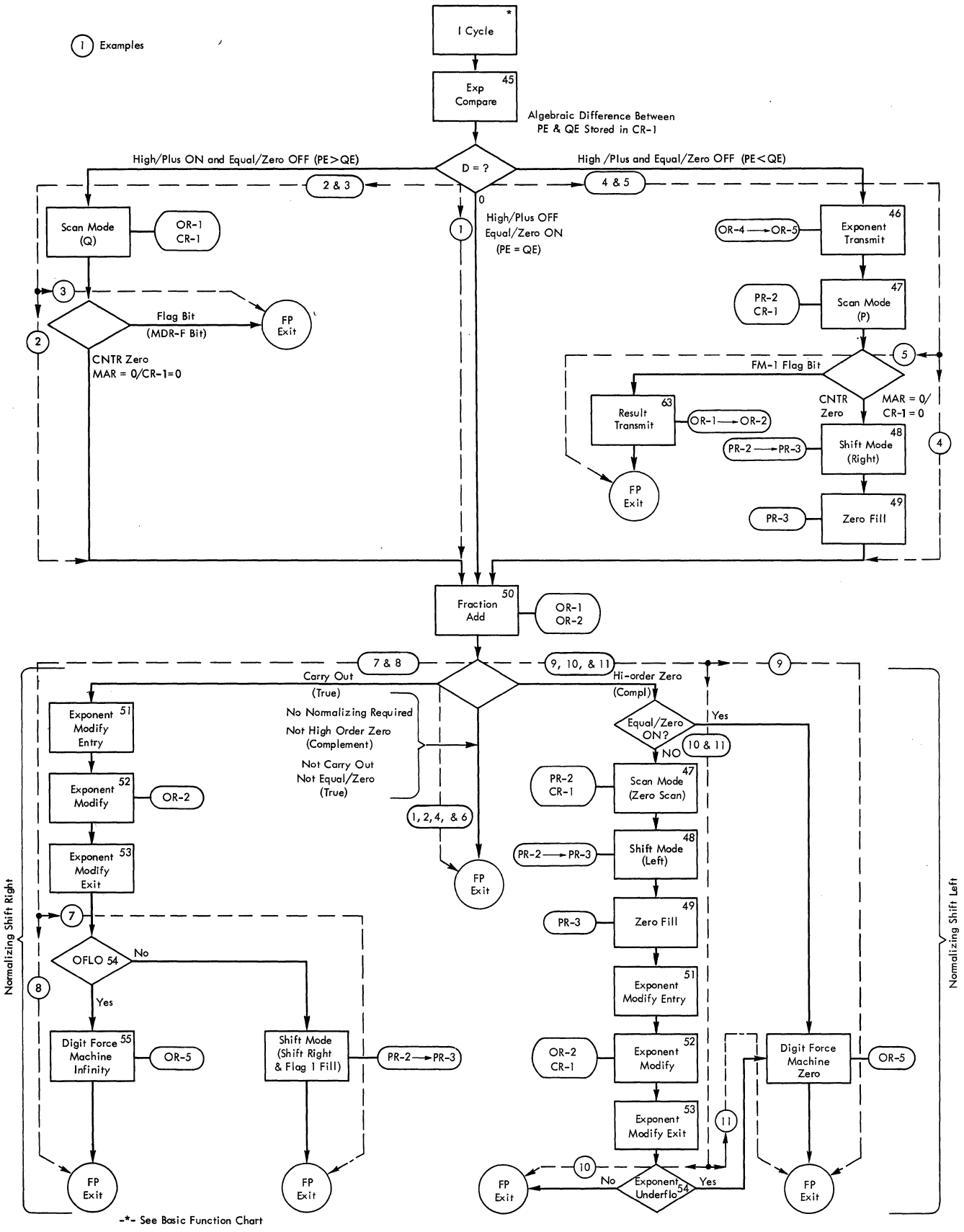


Figure 4-2. Data Flow – Add and Subtract

that QF is shifted completely out of the available 3-position result field and is therefore insignificant in relation to PF. PF and PE are declared the result and are left at the P address with no alteration. Exit to I-cycle entry for the next instruction in sequence.

Example 4. (PE < QE) Exponent Transmit — Scan P — Fraction Add

123 02	P	12.3
246 04	Q	2460.0
247 04	Result	2472.3

←Available result field

Exponent Compare. PE<QE, high/plus off, equal/zero off (PF must be shifted right to align decimals).

Exponent Transmit. QE is declared to be the result exponent, and therefore QE per OR-4 is transmitted to the PE field per OR-5.

Scan Mode (P). CR-1 contains the algebraic difference between PE and QE, a complement 2 (00098) in this example. The PF field must be shifted right two positions to align the decimal points. The PF field is scanned by decrementing PR-2 the number of places indicated by CR-1 (2). In this example, PR-2 will, after the scan, contain the address of the high-order digit (1) of the PF. This is the address of the first position to be shifted right to align the 1 in PF with the 6 in QF.

Shift Mode (Right). The 1 per PR-2 is transmitted to the position originally occupied by the 3 per PR-3. The flag bit with the 1 stops the transmittal operation. PR-2 and PR-3 are decremented during the shift mode operation.

Zero Fill Mode. The positions occupied by the 1 and 2 in the PF field in the example must be set to zero because, in the transmit operations, the location from which digits are transmitted is not cleared during the transmission. PR-3 contains the address of the 2 in the PF field at the end of the shift mode operation and is used to fill in zeros until stopped by the original (1) field mark.

Fraction Add. True, no carry out, equal/zero off, (no normalizing required). Exit to I cycle entry for the next instruction in sequence.

Example 5. (PE < QE) Exponent Transmit — Scan P — FP Exit

123 03	P	123
246 08	Q	24600000
246 08	Result	24600123

←Available result field

Exponent Compare. PE < QE, high/plus off, equal/zero off (PF must be shifted right to align decimals).

Exponent Transmit. QE is declared the result exponent and therefore is transmitted to the result exponent location (PE at the P address). The digits of QE are read out per OR-4 and placed in the PE location, per OR-5, replacing the original PE. The address of the units digit of QE is placed in OR-4 during the first trigger 11 time of the exponent compare operation. The address of the units digit of PE is placed in OR-5 during the first trigger 12 time of the exponent compare operation.

Scan Mode (P). CR-1 contains the algebraic difference between PE and QE, a complement 5 (00095) in this example. The PF field must be shifted right five positions to align the decimal points. The PF field is scanned by decrementing PR-2 the number of places indicated by CR-1 (5). In this example, the field mark flag bit of PF is encountered before CR-1 reaches zero (MAR = 0/CR-1 = 0). This condition indicates that the PF must be shifted completely out of the available 3-position result field and is therefore insignificant in relation to the QF. QF is declared the result fraction with no alteration. QF must therefore be transmitted to the PF location replacing PF. Notice that QE replaced PE during the exponent transmit operation. Also note that if this operation had been a code 02-FSUB, the sign of QF would be changed during the result transmit mode.

Result Transmit. Transmit QF per OR-1 to the PF address per OR-2. PF is destroyed during the transmit operation. Exit to I cycle entry for the next instruction in sequence.

Example 6. No Normalizing Required

	123 04	P
	246 04	Q
	369 04	Result

Fraction Add. No normalizing required, true, no carry out, not equal/zero. Exit to I cycle entry for the next instruction in sequence.

Example 7. Normalizing Shift Right Required — 1 Fill

	423 04	P
	745 04	Q
CO	168 04	Result at end of Fraction Add
	116 05	Final Result

Normalizing shift right required: true, carry out.

Exponent Modify Entry (01/02). Control and address set up operation. For details, see EXPONENT MODIFY ENTRY (01/02) in Section 3.

Exponent Modify Mode (01/02). Add 1 to the result exponent. There is no carry out, therefore, there is no exponent overflow. For details, see EXPONENT MODIFY MODE (01/02) in Section 3.

Exponent Modify Exit (01/02). Control and address set up operation. For details, see EXPONENT MODIFY EXIT in Section 3.

Shift Mode (Shift Right and $\bar{1}$ Fill). Shift PF to the right one position (PR-2 to PR-3) and place a $\bar{1}$ (for the carry) in the high-order position. Exit to I cycle entry for the next instruction in sequence.

Example 8. Normalizing Shift Right Required — Digit Force (∞)

	$\bar{4}23\ \bar{9}9$	P
	$\underline{\bar{7}45\ \bar{9}9}$	Q
CO	$\bar{1}78\ \bar{9}9$	Result at end of Fraction Add
	$\bar{9}99\ \bar{9}9$	Final Result (Machine infinity)

Normalizing shift right required: true, carry out.

Exponent Modify Entry (01/02). Control and address set up operation. See EXPONENT MODIFY ENTRY (01/02) in Section 3 for details.

Exponent Modify Mode (01/02). Add 1 to the result exponent. Carry out occurs (99 + 1 = 100), therefore there is an exponent overflow. The overflow/underflow latch is turned on.

Exponent Modify Exit (01/02). Control and address set up operation. For details, see EXPONENT MODIFY EXIT (01/02) in Section 3.

Digit Force Mode (∞). Starting with the units position of the result exponent, place 9s in both exponent positions and in the three positions (for this example) of the result fraction field. The operation is stopped when the high-order position of the result fraction (PF) is reached. The high-order position is flagged for the field mark.

NOTE: If the result fraction had been signed minus, a flag 9 ($\bar{9}$) would be placed in the units position of the result fraction field.

Example 9. Zero Fraction Result — Digit Force (0)

	$\bar{3}45\ \bar{0}4$	P
	$\underline{\bar{3}4\bar{5}\ \bar{0}4}$	Q
	$\bar{0}00\ \bar{0}4$	Result after Fraction Add
	$\bar{0}00\ \bar{9}\bar{9}$	Final Result (Machine zero)

Complement operation, high-order zero control on, equal/zero on.

Digit Force Mode (0). Starting with the units position of the result exponent (PE), place a negative 9 ($\bar{9}$) in the units position and a field mark 9 ($\bar{9}$) in the tens position. Place zeros in all result fraction (PF) positions (three positions for this example) in the result fraction field.

Example 10. Normalizing Shift Left — Shift Left — Zero Fill

	$\bar{3}45\ \bar{0}4$	P
	$\underline{\bar{3}2\bar{1}\ \bar{0}4}$	Q
	$\bar{0}24\ \bar{0}4$	Result after Fraction Add
	$\bar{2}40\ \bar{0}3$	Final Result

Normalizing shift left required: complement, high-order zero control on, equal/zero off.

Scan Mode (Zero). Scan the result fraction field (PF) starting with the high-order digit per PR-2 and test each position for a significant digit (other than zero). Count, by incrementing CR-1, the number of zeros (one in this example) encountered prior to reaching the first significant digit. At the end of the scan (first significant digit encountered) PR-2 contains the address of this first significant digit.

Shift Mode (Left). Transmit the first significant digit per PR-2 to the original high-order digit position per PR-3. PR-3 was set to the address of the original high-order position digit at the end of the fraction add operation.

Zero-Fill Mode. Place a zero in the position(s) vacated by the previous left shift operation. In the example given, the result fraction field contains $\bar{2}44$ at the end of the left shift (transmit) operation. The 4 in the units position was not destroyed when it was transmitted to the next position to the left. At the end of the left shift operation PR-3 contains the address of the digit immediately to the right of the last digit transmitted. PR-3 can thus be used to set zeros in the positions to the right of the last digit transmitted by incrementing through the fraction field until stopped by a flag bit. For the example given, the first flag bit encountered will be the field mark of the result exponent (PE). This flagged digit is returned to memory unaltered.

NOTE: In the case of a field signed minus, the first flag encountered is the sign flag of the result fraction (PF). For details of this operation see the detailed writeup for Zero Fill Mode under FLOATING ADD OR SUBTRACT.

Exponent Modify Entry (01/02). Control and address set up operation. For details, see EXPONENT MODIFY ENTRY (01/02) in Section 3.

Exponent Modify Mode (01/02). Subtract the contents of CR-1 from the result exponent (PE). In the example, CR-1 contains a one because, during the scan zero, just one zero was counted prior to encountering the first significant digit. No underflow occurs ($\bar{0}4 - \bar{0}1 = \bar{0}3$).

Exponent Modify Exit (01/02). Control and address set up operation. For details see EXPONENT MODIFY EXIT. Exit to I cycle entry for the next instruction in sequence.

Example 11. Normalizing Shift Left — Exp O'Flo — Digit Force (0)

$\bar{3}45\ \bar{9}\bar{9}$	P
$\underline{\bar{3}21\ \bar{9}9}$	Q
$\bar{0}24\ \bar{9}\bar{9}$	Result after Fraction Add
$\bar{2}40\ \bar{0}\bar{0}$	Result after Exponent Modify
$\bar{0}00\ \bar{9}\bar{9}$	Final Result (Machine zero).

This example has the same functions as example 10 until it reaches the exponent modify mode.

Exponent Modify Mode (01/02). Subtract the contents of CR-1 from the result exponent (PE). In the example, CR-1 contains a 1 because, during scan zero, just one zero was counted prior to encountering the first significant digit. An underflow occurs

$$[(-99) - (+01) = -100]$$

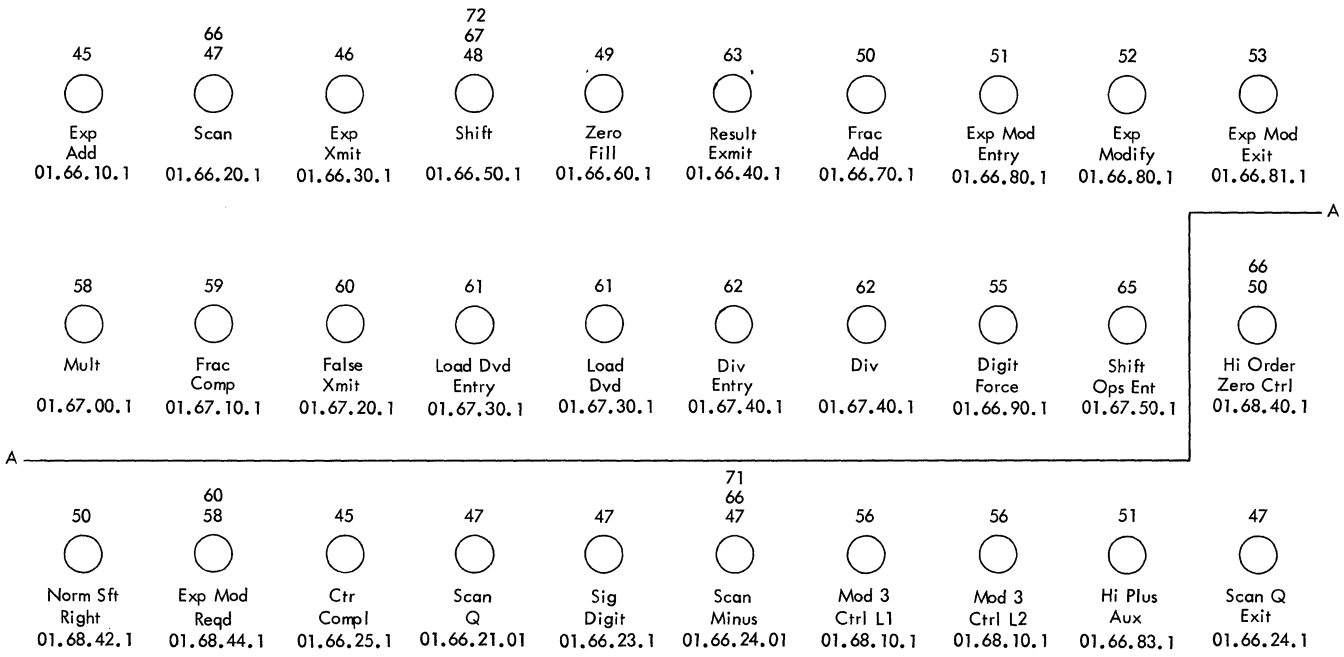
The overflow/underflow and underflow/equal zero latches are turned on.

Exponent Modify Exit (01/02). Control and address set up operation. For details, see EXPONENT MODIFY EXIT (01/02) in Section 3.

Digit Force Mode. Starting with the units position of the result exponent (PE), place a negative 9 ($\bar{9}$) in the units position and a field mark 9 ($\bar{9}$) in the tens position. Place zeros in the result fraction (PF) positions (three positions for this example). Exit to I cycle for the next instruction in sequence.

Appendix A

Auxiliary CE Console Keyed to Function Charts and System Diagrams



The lamps above A-A are associated with Mode latches
The lamps below A-A are associated with Auxilliary latches
The numbers above the lamps indicate function chart page numbers (Form 227-5631) on which the latch is shown

Appendix B

Floating Point Latches

Latch Name or Number See Syst Diag 01.05.60.1 (Form 227-5631)	Syst Diagram Page # (Form 227-5631)		Function Chart Page # (Form 227-5631)
Counter Comp (Complement)	01.66.25.1	*	45
D > 99	01.66.19.1		45
Digit Force Entry	01.66.90.1		53,55
Digit Force Mode	01.66.90.1	*	55
Divide Entry	01.67.40.1	*	62
Divide Mode	01.67.40.1	*	62
Exponent Add Mode	01.66.10.1	*	45
Exponent Check	01.68.90.1	ǂ	54
Exponent Modify Entry	01.66.80.1	*	51
Exponent Modify Exit	01.66.81.1	*	53
Exponent Modify Mode	01.66.80.1	*	52
Exponent Modify Required	01.68.44.1	*	58,60
Exponent Xmit Entry	01.66.30.1		46
Exponent Xmit Mode	01.66.30.1	*	46
False Xmit Mode	01.67.20.1	*	60
F Mul Correct Flag	01.45.50.1		58
Force Flag One	01.66.51.1		48
FP Exit	01.67.90.1	ǂ	48,49,50,53,55,63 68,69
Frac Add Entry	01.66.70.1		50
Frac Add Mode	01.66.70.1	*	50
Frac Compare Entry	01.67.10.1		59
Frac Compare Mode	01.67.10.1	*	59
Hi Order Zero Ctrl	01.68.40.1	*	50,66
Hi Plus (H/P) Aux	01.66.83.1	*	51
Load Dvd Entry	01.67.30.1	*	61
Load Dvd Mode	01.67.30.1	*	61
Modulo 3 Ctr. L1 & L2	01.68.10.1	*	56
Modulo 3 Ctr. L3	01.68.10.1		
Mult Mode	01.67.00.1	*	58
Mult Mode Entry	01.67.00.1		58
Norm Sft Right	01.68.42.1	*	50
O'flo Correct	01.66.83.1		54
Overflow/Underflow	01.68.85.1		54
Result Xmit Mode	01.66.40.1	*	63
Scan Entry	01.66.20.1		47,66
Scan Minus	01.66.24.1	*	47,66,71
Scan Mode	01.66.20.1	*	47,66
Scan Q	01.66.21.1	*	47
Scan Q Exit	01.66.24.1	*	47
Shift Entry	01.66.50.1		48,66,71
Shift Mode	01.66.50.1	*	48,67,72
Shift Ops Entry	01.67.50.1	*	65
Sig Digit	01.66.23.1	*	47
Triggers 15 & 16	01.60.45.1	ǂ	69
Triggers 24 & 25	01.68.24.1	ǂ	46,47,48,49,51,53 55,60,61,62,65,66, 67,71,72
Triggers 26 & 27	01.60.57.1	ǂ	63,68,69
Underflow/Equal Zero	01.68.85.1	ǂ	54
Zero Fill Mode	01.66.60.1	+	49

* Light on Auxilliary Console

ǂ Light on Basic Console

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