LOGIC NO	DESCRIPTION	PART NO	EC NO	SEC #	REA	SF 9/M
SYSTEMS DIAGRAMS						
SD011	BLOCK DIAGRAM - STORAGE ADJ	2196980	731676	E0013		2510220
SD012	PERSPECTIVE DIAGRAM	2196981	414308	E0001		2510220
SD013	SJ4 STORAGE ADJUSTMENT *5 PAGES*	2500256	731503A	E0006		2510220
SD021	REF PLUG CHART	2196982	414308	E0001		2510220
SD031	TIMING	2196983	731503	E0003		2510220
SD041	8K ARRAY ADDRESSING	2196984	414308	E0001		2510220
SD042	4K ARRAY ADDRESSING	2196985	414308	E0001		2510220
SD043	X-Y DRIVE READ	2196986	414308	E0001		2510220
SD044	X-Y DRIVE WRITE	2196987	414308	E0001		2510220
SD051	INHIBIT SENSE 4K	2196988	414308	E0001		2510220
SD061	SENSE CONNECTIONS 8K	2196989	414308	E0001		2510220
SD062	SENSE CONNECTIONS 4K	2196990	414308	E0001		2510220
SD071	8K BOTTOM BOARD SCHEMATIC *2 PAGE	2196991	731676	E0013		2510220
SD072	4K BOTTOM BOARD SCHEMATIC *2 PAGE	2196992	731676	E0013		2510220
SD081	8K DIODE BOARD SCHEMATIC *2 PAGES	2196993	731676	E0013		2510220
SD082	4K DIODE BOARD SCHEMATIC *2 PAGES	2196994	731676	E0013		2510220
SD101	SLDA SOCKET LISTING	2196645	731503	E0003		2510220
SD111	CONTROL CLOCK	2196650	731503	E0003		2510220
SD121	XY CURRENT CONTROL	2196651	731503	E0003		2510220
SD221	VOLTAGE DISTRIBUTION	2196653	731503	E0003		2510220
SD311	MAR INVERTERS 1 OF 3	2196654	731503	E0003		2510220
SD311 010	MAR INVERTERS 1 OF 3	2510216	731504	E0004		2510220
SD321	MAR INVERTERS 2 OF 3	2196655	731503	E0003		2510220
SD331	MAR INVERTERS 3 OF 3	2196656	731503	E0003		2510220
SD331 010	MAR INVERTERS 3 OF 3	2510217	731504	E0004		2510220
SD411	Y READ GATE WRITE DRIVER	2196657	731503	E0003		2510220
SD421	Y READ GATE WRITE DRIVER	2196658	731503	E0003		2510220
SD431	Y READ GATE WRITE DRIVER	2196659	731503	E0003		2510220
SD441	Y READ GATE WRITE DRIVER	2196660	731503	E0003		2510220
SD451	X WRITE GATE READ DRIVER	2196661	731503	E0003		2510220
SD461	Y WRITE GATE READ DRIVER	2196662	731503	E0003		2510220
SD471	X Y DRIVE ARRAY CONN Y DIM	2196668	414308	E0001		2510220
SD511	X READ GATE WRITE DRIVER	2196663	731503	E0003		2510220
SD521	X READ GATE WRITE DRIVER	2196664	731503	E0003		2510220
SD531	X WRITE GATE READ DRIVER	2196665	731503	E0003		2510220
SD541	X WRITE GATE READ DRIVER	2196666	731503	E0003		2510220
SD551	X AUX WRITE GATE READ DRIVER	2196667	731503	E0003		2510220
SD561	XY DRIVE ARRAY CONN X DIM	2196669	414308	E0001		2510220
SD611	DATA INPUT	2196670	731503	E0003		2510220
SD621	DATA INPUT	2196671	731503	E0003		2510220
SD621 010	DATA INPUT	2510218	731504	E0004		2510220
SD631	INHIBIT INPUT LESS THAN 4K	2196672	414308	E0001		2510220
SD641	INHIBIT INPUT MORE THAN 4K	2196673	414308	E0001		2510220
SD651	INHIBIT INPUT LESS THAN 4K	2196674	414308	E0001		2510220
SD661	INHIBIT INPUT MORE THAN 4K	2196675	414308	E0001		2510220
SD711	INHIBIT SENSE BIT 0 AND 1	2196676	731503	E0003		2510220
SD721	INHIBIT SENSE BIT 2 AND 3	2196677	731503	E0003		2510220
SD731	INHIBIT SENSE BIT 4 AND 5	2196678	731503	E0003		2510220
SD741	INHIBIT SENSE BIT 6 AND 7	2196679	731503	E0003		2510220
SD751	INHIBIT SENSE BIT 8 AND 9	2196680	731503	E0003		2510220
SD761	INHIBIT SENSE BIT 10 AND 11	2196681	731503	E0003		2510220
SD771	INHIBIT SENSE BIT 12 AND 13	2196682	731503	E0003		2510220
SD781	INHIBIT SENSE BIT 14 AND 15	2196683	731503	E0003		2510220
SD791	INHIBIT SENSE BIT 16 AND 1M	2196684	731503	E0003		2510220
SD791 010	INHIBIT SENSE BIT 16 AND 17	2510219	731504	E0004		2510220

2196980

READ CYCLE
WRITE CYCLE

CLOCK & TIMING SD111

TIMING PULSES

TO INHIBIT DRIVERS, SENSE AMPLIFIER & SENSE CONTROL

CURRENT CONTROL SD121

TO GATES & DRIVERS

ARRAY CAPACITIES

4K
MAIN = 4096 - 18 BIT WORDS
AUX = 256 - 18 BIT WORDS

8K
MAIN = 8192 - 18 BIT WORDS
AUX = 512 - 18 BIT WORDS

ADDR REG BITS 3 TO 15, AUX

SJ-4 CPU INTERFACE

(8)

ADDR REG BITS 3, 4, 5, AUX SD321-331

X WRITE GATES SD531-551

X READ DRIVERS SD531-551

X

SIDE A

DIODE BOARD SD081-082

SIDE D ARRAY SD471, 561

SIDE B

Y

(8)

Y WRITE GATES SD451-461

Y READ DRIVERS SD451-461

ADDR REG BITS 9, 10, 11 SD311-321

SIDE C

AIR FLOW

(16)

ADDR REG BITS 12, 13, 14, 15 SD311

Y RD GT - WR DR SD411-441

Y

BOTTOM BOARD SD071-072

SENSE CONNECTIONS SD061-062

Z

X

(8)

X RD GT - WR DR SD511-521

ADDR REG BITS 6, 7, 8 SD321

INHIBIT BIT DATA

INHIBIT DRIVERS SD711-791

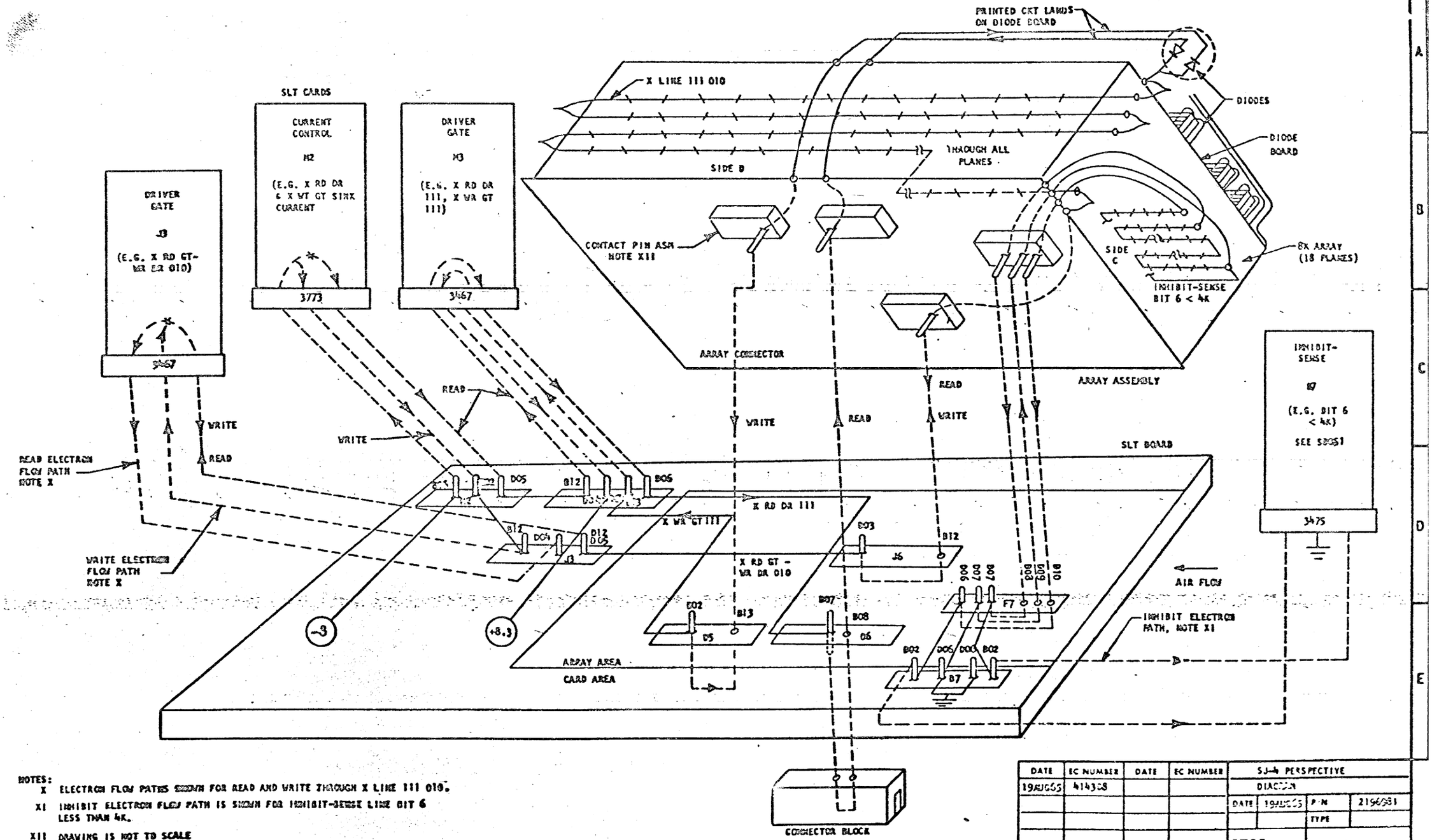
SENSE AMPLIFIERS SD711-791

SENSE CONTROL SD211

SENSE BIT DATA
(TO CPU)

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME SJ-4 BLOCK DIAGRAM				19 AUG 65	414308			X PRINT TO ENG. SPEC. NO.	
				[illegible]	260302				
DESIGN		MODEL SD011		[illegible]	731503				
DETAIL				1 FEB 68	731676				
CHECK		DRAW KE							
APPRO		CHECK [illegible]							

2196980



NOTES:

X ELECTRON FLOW PATHS SHOWN FOR READ AND WRITE THROUGH X LINE 111 010.

XI INHIBIT ELECTRON FLOW PATH IS SHOWN FOR INHIBIT-SENSE LINE BIT 6 LESS THAN 4K.

XII DRAWING IS NOT TO SCALE

XIII ONLY 4 OF 18 CONTACT PIN ASM ARE SHOWN.

* SD043 & SD044 FOR CIRCUITRY IN J3, M2, AND M3.

DATE	EC NUMBER	DATE	EC NUMBER	SJ-4 PERSPECTIVE			
19AUG65	414308			DIAGRAM			
				DATE	19AUG65	P/N	2196981
						TYPE	
				IBM		SD012	

SJ-4 STORAGE ADJUSTMENT (SUMMARY)

I VOLTAGE ADJUSTMENT

1. SET STORAGE BOARD LOGIC VOLTAGES TO WITHIN 1% OF NOMINAL.
2. SPECIAL VOLTAGE (+12V) SHOULD BE WITHIN 11.16V TO 12.84V (A2D09).
3. THE "+8.3V GATE VOLTAGE" SHOULD BE WITHIN 8.0 TO 8.8V(A2D13).
4. MEASURE INTAKE TEMPERATURE AND RECORD TEMPERATURE ON THE LABEL.
5. SET V-REF TO WITHIN ±0.03V OF THE VALUE GIVEN IN FIGURE 1 (G2B02 REFERENCED TO G2B06). V-REF IS OPTIMIZED FOR THE SPECIFIC UNIT UNDER THE "V-REF ADJUSTMENT" SECTION.

II SENSE CONTROL ADJUSTMENT

1. STOP CLOCK. "EMITTER STROBE" SHOULD BE AT ITS -3V LEVEL.
2. ADJUST -3V TO GIVE -2.70V BETWEEN "EMITTER STROBE" AND GROUND: (G2B12 TO G2D08).
3. ADJUST "SENSE CONTROL VOLTAGE" TO 2.14V REFERENCED TO THE "OFFSET VOLTAGE (G2B07 TO G2B09).
4. RESTORE -3V TO NORMAL (G2B06 TO G2D08).
5. "SENSE CONTROL VOLTAGE" RANGE IS 2.24V ± 0.05V (G2B07 TO G2B09). RECORD ON LABEL.

III STROBE ADJUSTMENT

1. OBSERVE ONES ENVELOPE (E.G. BIT 6 LESS THAN 4K: B7B02 & B7D02).
2. SHORT N2B05 TO N2D08 AND PLACE PEAK OF READ ONES ENVELOPE ON CENTER VERTICAL LINE.
3. REMOVE SHORT AND COMPARE "+ STROBE LESS THAN 4K (H2B09) WITH "+ STROBE MORE THAN 4K" (H2B08).
4. SET LEADING EDGE OF STROBE AT THE 0.5V LEVEL 10 NANOSECONDS AFTER PEAK OF ONES ENVELOPE (H2B09).*
5. RECORD ON LABEL THE INTERVAL BETWEEN THE PEAK OF THE ONES ENVELOPE AND THE LEADING EDGE OF THE STROBE. (B7B02 & B7D02 TO H2B09).
6. RECORD ACCESS TIME ON LABEL (E1E11 TO C1C11 OR B7B04).

IV V-REF ADJUSTMENT

1. SET V-Z TO 6.36V OR 6.24V IF CPU CANNOT OPERATE OUTSIDE ±4% (G2B11 TO G2D08).
2. DETERMINE THE UPPER AND LOWER OPERATING LIMITS OF V-REF (G2B02 TO G2B06).
3. SET V-Z TO 5.64V OR 5.76V IF CPU CANNOT OPERATE OUTSIDE ±4% (G2B11 TO G2D08).
4. DETERMINE THE UPPER AND LOWER OPERATING LIMITS OF V-REF (G2B02 TO G2B06).
5. SET V-REF TO THE OPTIMUM OPERATING POINT. (SEE FIGURE 5), AND RECORD V-REF VALUE.
6. DETERMINE V-REF OPERATING RANGE (%) AND INSURE THAT THE REQUIREMENTS LISTED IN THE TABLE ARE MET. RECORD V-REF LIMITS AND PERCENTAGE ON LABEL.

SUMMARY OF TEST POINTS, VOLTAGE REFERENCE POINTS AND POTENTIOMETER LOCATIONS

NET NAME	LOCATION OR PIN	COMMENTS OR LEVEL
-3V LOGIC VOLTAGE	G2B06	-3.00V, ±0.03V (A), ±0.12V (B).
+3V LOGIC VOLTAGE	G2D03	+3.00V, ±0.03V (A), ±0.12V (B).
+6V LOGIC VOLTAGE	G2B11	+6.00V, ±0.06V (A), ±0.24V (B), ±0.36V (C).
BOARD LOGIC GROUND	G2D08	GROUND
+12V SPECIAL VOLTAGE	A2D09	+12.00 ±0.84V
+8.3V GATE VOLTAGE	A2D13	+8.3V -0.3V, +0.5V
VREF POTENTIOMETER	G2	(UPPER POT)
VREF	G2B02	(REFERENCE TO -3V)
-3V (0.7V) EMITTER STROBE	G2B12	(REFERENCE TO GND)
SENSE CONTROL POTENTIOMETER	G2	(LOWER POT)
SENSE CONTROL VOLTAGE (VSA)	G2B07	(REFERENCE TO OFFSET VOLTAGE)
OFFSET VOLTAGE	G2B09	0.8V±0.2V
+ READ CYCLE	E1E11	(TO SYNCHRONIZE SCOPE)
+ STROBE LESS THAN 4K	H2B09	(REFERENCE POINT)
+ STROBE MORE THAN 4K	H2B08	(REFERENCE POINT)
STROBE POTENTIOMETER	N2	(ONLY POT)
X CURRENT REFERENCE VOLTAGE	M2B09	(TEST POINT)
Y CURRENT REFERENCE VOLTAGE	B2B09	(TEST POINT)
- SENSE BIT 6	C1C11 OR B7B04	(ACCESS REFERENCE)
+ SHORT TIME	N2B13	(REFERENCE POINT)

A WESTON 901 (1/4%) OR EQUIVALENT METER IS REQUIRED FOR ALL VOLTAGE ADJUSTMENTS. TIME MEASUREMENTS ARE TO BE WITHIN ± 10 NS. ABSOLUTE TIME MEASUREMENTS SHALL BE MADE WITH A CALIBRATED SCOPE. IN THE FIELD THIS CALIBRATION CAN BE DONE WITH THE CRYSTAL OSCILLATOR TIMING OUTPUT OF THE HOST MACHINE. GROUNDED PROBES MUST BE USED FOR MAKING TIME MEASUREMENTS.

TOLERANCE NOTES

(A) - ADJUSTMENT SETTING TOLERANCE - APPLIES TO THE ADJUSTMENT PROCEDURE ONLY
(B) - NORMAL OPERATING SUPPLY VARIATION MEASURED AT THE STORAGE UNIT BOARD PINS LISTED ABOVE.
(C) - STORAGE OPERATING LIMITS HOWEVER, THE CPU MAY NOT OPERATE OUTSIDE OF ±4%, ie.6.00V±0.24V.
* - THESE ARE TO BE WITHIN 10 NS OF EACH OTHER.

INTERNATIONAL BUSINESS MACHINES CORP.		DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SJ-4 STORAGE ADJUSTMENT	21FEB67	256302			X PRINT TO ENG. SPEC. NO.	
DESIGN	LER ... MODEL H11	11JUN67	731503A				
DETAIL							
CHECK	DRAW KE 11JUN67						SD013
APPRO	CHECK						2500256

SJ-4 STORAGE ADJUSTMENT (DETAILED)

STORAGE ADJUSTMENT SHOULD NOT BE MADE UNLESS A CARD IN A2, B2, G2, M2, OR N2 IS REPLACED OR THERE IS A CLEAR INDICATION THAT THE STORAGE IS NOT ADJUSTED PROPERLY. A COMPLETE ADJUSTMENT INCLUDES 1) VOLTAGE ADJUSTMENT, 2) SENSE CONTROL ADJUSTMENT, 3) STROBE ADJUSTMENT, AND 4) VREF ADJUSTMENT.

IF THE CARD IN LOCATION N2 IS REPLACED, THE "STROBE ADJUSTMENT" SECTION MUST BE FOLLOWED. IF A CARD IN A2, B2, G2, OR M2 IS REPLACED, A COMPLETE ADJUSTMENT MUST BE MADE.

UPDATE "ADJUSTMENT SETTINGS" LABEL WHENEVER THE STORAGE IS READJUSTED.

I. VOLTAGE ADJUSTMENT

ALL VOLTAGES ARE MEASURED WITH RESPECT TO STORAGE UNIT GROUND EXCEPT WHERE NOTED OTHERWISE. A WESTON 901 (2/4%) OR EQUIVALENT METER IS REQUIRED FOR ALL VOLTAGE ADJUSTMENTS.

1. SET STORAGE BOARD LOGIC VOLTAGES AS FOLLOWS, MEASURED WITH RESPECT TO BOARD GROUND.

-3.00V ±0.03V	G2B06
+3.00V ±0.03V	G2D03
*+6.00V ±0.06V	G2B11
GROUND	C2D08

*NOTE: +6 IS ALSO V_Z

2. SPECIAL VOLTAGE (+12V), MEASURED AT A2D09, SHOULD BE WITHIN 11.16V TO 12.84V

+12.0V±0.84V A2D09

3. THE "+8.3V GATE VOLTAGE" SHOULD BE WITHIN 8.0V TO 8.8V.

+8.3V GATE VOLTAGE: A2D13
(+8.3V-0.3V, +0.5V)

4. MEASURE THE TEMPERATURE OF THE INCOMING AIR AND RECORD THE TEMPERATURE ON THE LABEL.

THERMOMETER: P/N 5392366 (OR EQUIVALENT)

5. SET V-REF (MEASURED WITH RESPECT TO -3V) TO WITHIN ±0.03V OF THE VALUE GIVEN IN FIGURE 1. THIS IS AN INITIAL ADJUSTMENT. V-REF IS A TEMPERATURE TRACKING VOLTAGE. ONCE V-REF HAS BEEN SET IT WILL TRACK A LINE PARALLEL TO THAT SHOWN IN FIGURE 1. THIS LINE REPRESENTS THOSE SETTINGS OF V-REF AT WHICH THE STORAGE CAN BE EXPECTED TO OPERATE WITHOUT ERROR. IT DOES NOT REPRESENT OPTIMUM SETTINGS OF V-REF FOR A SPECIFIC STORAGE UNIT. THE ACTUAL TRACKING LINE MAY HAVE A SLOPE OF (-0.013V±0.002V)/°C

VREF POT: G2(UPPER POT)
VREF: G2B02
-3V: G2B06

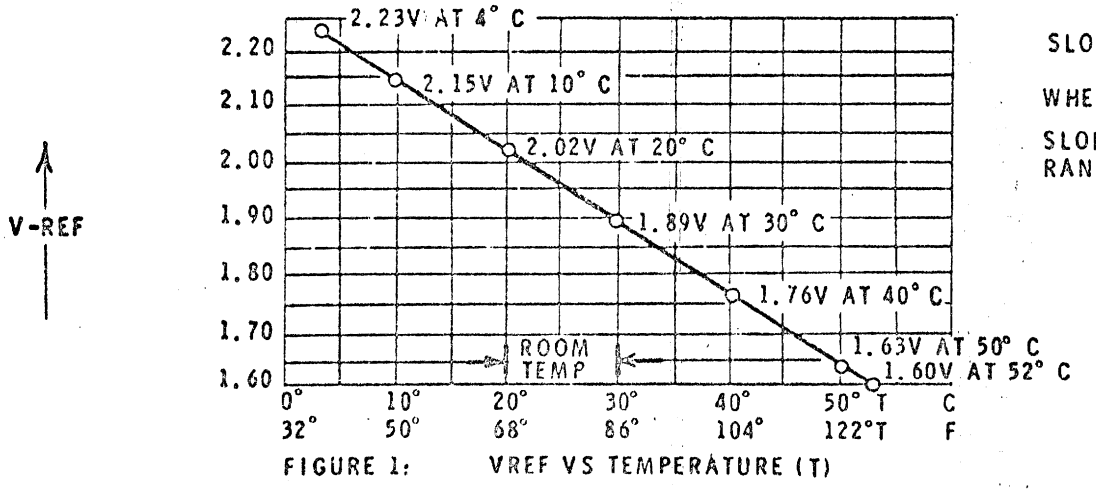


FIGURE 1: VREF VS TEMPERATURE (T)

$$\text{SLOPE} = \frac{\text{V-REF AT } T_1 - \text{V-REF AT } T_2}{\text{TEMPERATURE } T_1 - \text{TEMPERATURE } T_2}$$

WHERE: $T_1 - T_2$ MUST BE AT LEAST 10° C.

SLOPE RANGE: -0.011V/°C TO -0.015V/°C.

II. SENSE CONTROL ADJUSTMENT

1. STOP THE CLOCK. THE "-3V (0.7V) EMITTER STROBE" SHOULD BE AT ITS -3V LEVEL. THE TWO VOLTAGES (-3V & 0.7V) DEFINE THE SIGNAL LEVELS OF THIS NET.

2. ADJUST -3V TO GIVE -2.70V BETWEEN "-3V (0.7V) EMITTER STROBE" AND GROUND.

-3V (0.7V) EMITTER STROBE: G2B12
GROUND: G2D08

3. ADJUST THE LOWER POTENTIOMETER ON CARD G2 TO SET THE "SENSE CONTROL VOLTAGE" TO 2.14V REFERENCED TO THE "OFFSET VOLTAGE"

SENSE CONTROL POT: G2(LOWER POT)
SENSE CONTROL VOLTAGE: G2B07
OFFSET VOLTAGE: G2B09

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME SJ-4 STORAGE ADJUSTMENT				21FEB67	256302			X PRINT TO ENG. SPEC. NO.	
DESIGN LER 20JUN67	MODEL			12JUN67	731503A				
DETAIL									
CHECK		DRAW	KE 12JUN67						SD013
APPRO		CHECK							

4. RESTORE -3V TO NOMINAL.

-3V G2B06

5. RESTORING -3V TO NOMINAL WILL CAUSE THE "SENSE CONTROL VOLTAGE" REFERENCED TO THE "OFFSET VOLTAGE" TO RISE TO 2.24V ±0.05V AT ROOM TEMPERATURE. THIS VOLTAGE CHANGES AT THE RATE OF +0.01V/10°C. NOTICE THE 2.24V±0.05V IS THE RANGE, BUT THAT THE CORRECT SETTING IS OBTAINED BY FOLLOWING STEPS 1 TO 4. RECORD THE FINAL VALUE OF "SENSE CONTROL VOLTAGE" REFERENCED TO THE OFFSET VOLTAGE" ON THE LABEL. TOLERANCE FROM FINAL VALUE IS ±0.02V-0.01V/ °C.

III. STROBE ADJUSTMENT

SYNCHRONIZE ON TO OR "+ READ CYCLE" (E1E11). THE BASIC REQUIREMENT TO BE MET IS THAT THE LEADING EDGE OF THE STROBE, H2B09 (MEASURED AT THE 0.5V LEVEL WITH RESPECT TO ITS BASELINE) MUST BE WITHIN 0 TO 30 NANOSECONDS (WITH A NOMINAL SETTING OF 10 NS) AFTER THE PEAK OF THE ONES ENVELOPE. THE UNIT SHOULD OPERATE AT NOMINAL VOLTAGES ON ALL PATTERNS WHEN THE STROBE IS DELAYED AT LEAST 30 NANOSECONDS FROM ITS FINAL SETTING.

NOTE: THE CLOCK CARD (5804683) IN N2 MAY BE OF A, B, OR C LEVEL, ie. HAVE A 1K POTENTIOMETER. IN THIS CASE, IT MAY NOT BE POSSIBLE TO DELAY THE STROBE SUFFICIENTLY. IF THE STROBE CANNOT BE DELAYED AT LEAST 20 NS LATER THAN THE "FINAL" SETTING, THE CARD SHOULD BE REPLACED BY ONE HAVING A 2K POTENTIOMETER, ie. A D (OR LATER) LEVEL CARD. THE FINAL SETTING MUST BE AT LEAST ONE FULL TURN FROM ITS MAXIMUM DELAYED POSITION.

1. WHILE RUNNING AN ALL ONES PATTERN IN ALL ADDRESSES, OBSERVE THE ONES ENVELOPE FOR A LESS THAN 4K BIT, e.g. BIT 6<4K, B7B02 AND B7D02, USING DIFFERENTIAL SCOPE LEADS (OR ALTERNATE) TO DIFFERENTIAL INPUTS OF SCOPE SUCH AS A 561S, 647, OR 453. A SCOPE HAVING A BANDWIDTH OF AT LEAST 20 MC IS REQUIRED, AND SCOPE SETTINGS OF 50 NS AND 20 MV PER CM ARE RECOMMENDED.

CABLE ASSEMBLY--DIFFERENTIAL SCOPE LEADS (PN 2182907).

ALTERNATE: DIRECT TWISTED PAIR TERMINATED ON EACH LINE BY A 150 OHM RESISTOR TO SCOPE GROUND.

e.g. - BIT 6<4K: B7B02 AND B7D02

2. SHORT N2B05 TO N2D08 TO REMOVE STROBE REFLECTION, THEN ADJUST THE CENTER OF THE ONES ENVELOPE AT READ TIME TO THE CENTER VERTICAL LINE. CENTER MAY BE DETERMINED BY ADJUSTING THE SCOPE TO PLACE THE RISE AND FALL OF THE ONES ENVELOPE AT ±50 NS ON THE SAME HORIZONTAL LINE. SEE FIGURE 2. AT LEAST TWO BITS SHOULD BE OBSERVED TO DETERMINE THE AVERAGE TIME FOR THE CENTERS, e. g. BIT 6 < 4K: B7B02 AND B7D02 (4K), BIT 6>4K: A7B02 AND A7D02 (8K) OR BIT 14<4K: M7B02 AND M7D02 (4K) AND BOTH POSITIVE AND NEGATIVE CENTERS SHOULD BE OBSERVED.

BIT 6<4K: B7B02 AND B7D02
BIT 6>4K: A7B02 AND A7D02
BIT 14<4K: M7B02 AND M7D02.

N2B05 SHORTED TO N2D08

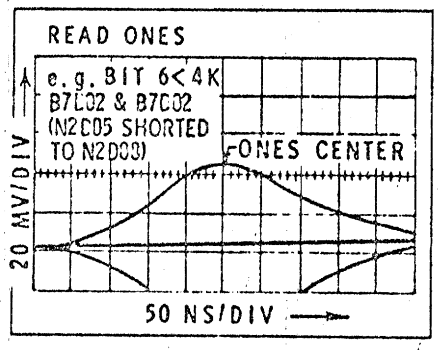


FIGURE 2

3. REMOVE THE SHORT OF STEP 2 AND COMPARE (ON 8K UNITS) "+ STROBE LESS THAN 4K." WITH "+ STROBE MORE THAN 4K." THE LEADING EDGES OF THE STROBES (MEASURED AT THE 0.5V LEVEL) MUST BE WITHIN 10 NANOSECONDS. A 10-TO-1 PROBE SHOULD BE USED FOR THESE MEASUREMENTS.

+ STROBE LESS THAN 4K: H2B09
+ STROBE MORE THAN 4K: H2B08

4. ADJUST THE POTENTIOMETER ON CARD N2 TO PLACE THE LEADING EDGE OF THE "+ STROBE LESS THAN 4K" (MEASURED AT THE 0.5V LEVEL WITH RESPECT TO ITS BASELINE) 10 NANOSECONDS LATER THAN THE THE ONES ENVELOPE. SEE FIGURE 3.

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME SV-4 STORAGE ADJUSTMENTS					12JUN67	731503A			X PRINT TO ENG. SPEC. NO.	2500256
DESIGN LER 20JUN67	MODEL									
DETAIL										
CHECK		DRAW KE 12JUN67								SD103
APPRO		CHECK								

STROBE POT: N2

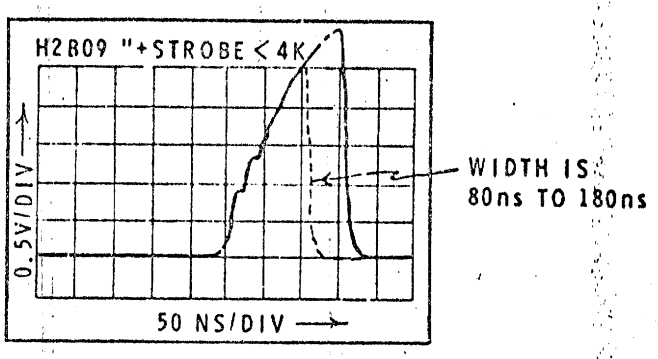


FIGURE 3

5. RECORD ON THE LABEL THE INTERVAL BETWEEN THE CENTERS OF THE ONES ENVELOPE (FIGURE 2) AND THE LEADING EDGE OF THE STROBE (MEASURED AT THE 0.5V LEVEL WITH RESPECT TO ITS BASELINE - FIGURE 3).

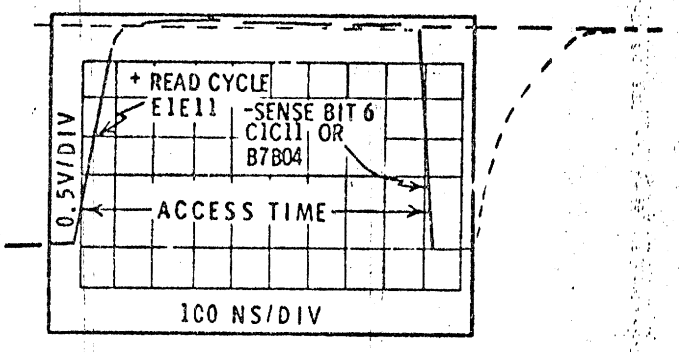
6. MEASURE THE INTERVAL BETWEEN THE RISE OF "+ READ CYCLE" (E1E11) AND THE FALL OF "-SENSE BIT 6" (C1C11 OR B7B04) AT THE 0.5V LEVEL WITH RESPECT TO BASELINES. SEE FIGURE 4. RECORD THIS INTERVAL AS "ACCESS TIME" ON THE LABEL.

+ READ CYCLE: E1E11

- SENSE BIT 6: C1C11 OR B7B04

ACCESS TIME: 700 NS TO 950 NS (SPECIFICATION)
910 NS±30 NS (TYPICAL 8K) 880 NS±30 NS (TYPICAL 4K)

FIGURE 4



IV. VREF ADJUSTMENT

VREF OPERATING LIMITS ARE DETERMINED BY RUNNING WORST CASE PATTERNS THROUGH ALL ADDRESSES. THESE PATTERNS ARE SET UP BY A TESTER OR BY STORAGE ADJUSTMENT PROGRAMS PROVIDED BY THE USING SYSTEM. FAILURE POINTS WILL BE DETECTED BY COMPARISON CIRCUITRY OR PARITY ERROR INDICATION. A VREF $-V_Z$ OPERATING RECTANGLE IS FORMED BY DEFINING THE UPPER AND LOWER BOUNDARIES AS $+6\pm0.36V$ (V_Z). THE LEFT AND RIGHT BOUNDARIES ARE DETERMINED BY THE TWO INNERMOST V-REF LIMITS V_A AND V_B ON THE $+6V\pm0.36V$ (V-Z) LINES. THE OPTIMUM (V-REF) OPERATING POINT IS THE POINT WHERE THE DIAGONALS OF THE RECTANGLE INTERSECT.

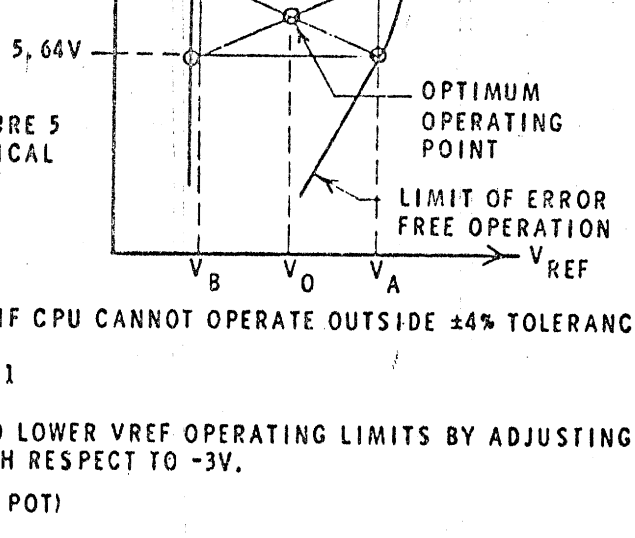


FIGURE 5
TYPICAL
PLOT

1. SET V_Z TO 6.36V. (6.24V IF CPU CANNOT OPERATE OUTSIDE ±4% TOLERANCE ON +6V SUPPLY)

V_Z (LOGIC +6V): G2B11

2. DETERMINE THE UPPER AND LOWER VREF OPERATING LIMITS BY ADJUSTING THE UPPER POTENTIOMFTER ON CARD G2. MEASURE VREF WITH RESPECT TO -3V.

VREF POT: G2(UPPER POT)
VREF: G2B02
-3V: G2B06

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME SJ-4 STORAGE ADJUSTMENT				12JUN67	731503A			X PRINT TO ENG. SPEC. NO.	
DESIGN LER 20JUN67		MODEL							
DETAIL									
CHECK		DRAW KF 12JUN67							SD013
APPRO		CHECK							

3. SET V_Z TO 5.64 V. (5.76V IF CPU CANNOT OPERATE OUTSIDE ±4% TOLERANCE ON +6V SUPPLY)

V_Z (LOGIC +6V): G2B11

4. DETERMINE THE UPPER AND LOWER VREF OPERATING LIMITS BY ADJUSTING THE UPPER POTENTIOMETER ON CARD G2. MEASURE VREF WITH RESPECT TO -3V.

VREF POT: G2(UPPER POT)
VREF: G2B02
-3V: G2B06

5. SET VREF TO OPTIMUM OPERATING POINT, SEE FIGURE 5 ABOVE, AND RECORD THE VALUE DETERMINED ON THE LABEL.

VREF: OPTIMUM OPERATING POINT

6. DETERMINE THE V-REF OPERATING RANGE (%). THE REQUIREMENTS ARE LISTED IN THE TABLE BELOW AND THE RANGE IS FOUND FROM:

a) FOR "OPTIMUM" CONDITION:- $\pm R_O = \pm \left\{ \frac{V_A - V_B}{V_A - V_B} \right\} \times 100.$ (R_o IS THE LIMIT PERCENTAGE FROM OPTIMUM OPERATING POINT.)

SEE FIGURE 5 FOR DEFINITIONS OF V_A AND V_B

b) FOR "TRACKING" CONDITION:- $\pm R_T = \pm \left\{ \frac{|V_N - V_T|}{V_T} \times 100 \right\}$. ($R_T$ IS THE PERCENTAGE FROM V-REF TRACKING POINT)

VT IS THE VREF TRACKING POINT AND VN IS THE VALUE OF V_A OR V_B NEAREST TO V_T. RECORD THE V-REF LIMITS AND PERCENTAGE ON LABEL.

ENVIRONMENT		REQUIRED LIMITS OF ERROR FREE OPERATION	
CLASSIFICATION	TEMPERATURE RANGE	VREF	Vz
ROOM TEMP	20°C TO 30°C	OPTIMUM VALUE ±10%	NOMINAL ± 6%
CLASS C	10°C TO 43.3°C	TRACKING POINT VALUE ±6%	NOMINAL ± 6%
ABOVE AND BELOW CLASS C	4°C TO 10°C AND 43.3°C TO 52°C	TRACKING POINT VALUE ±4%	NOMINAL ± 6%

* NOTE: FOR "CLASS C" AND "ABOVE AND BELOW CLASS C" THE LIMITS APPLY OVER THE TEMPERATURE RANGE SHOWN FOR ANY COMBINATION OF V-REF AND V_Z (ie. - VREF +6% & V_Z -6%).

THE ± 10% VREF VALUE APPLIES ONLY FOR THE SPECIFIC ROOM TEMPERATURE AT WHICH V-REF IS OPTIMIZED. THUS, IF THE UNIT IS ADJUSTED AND TESTED AT A ROOM TEMPERATURE ONLY (ie. A TEMPERATURE WITHIN 20° C TO 30° C) THE UNIT MUST OPERATE ERROR FREE WHEN V-REF IS VARIED ±10% FROM ITS OPTIMUM OPERATING POINT AND WHEN V_Z IS VARIED IN ANY COMBINATION (e.g. -V-REF +10% AND V_Z -6%).

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SJ-4 STORAGE ADJUSTMENT				21FEB67	256302			X PRINT TO ENG. SPEC. NO.	
DESIGN	LER	20JUN67	MODEL		9JUN67	731503A				
DETAIL										
CHECK			DRAW	KE 9JUN67						SD013
APPRO			CHECK							

SJ-4 REFERENCE PLUGGING CHART

P/N	DATE	TYPE
2196982	19AUG65	SD021

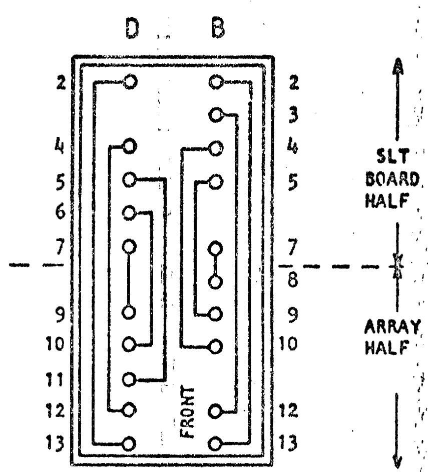
IBM

DATE	EC NUMBER
19AUG65	414308

STORAGE ADDRESS REGISTER

X HIGH ORDER			X LOW ORDER			Y HIGH ORDER			Y LOW ORDER			
3	4	5	6	7	8	9	10	11	12	13	14	15
RD DR, WR GT			RD GT - WR DR			RD DR, WR GT			RD GT - WR DR			

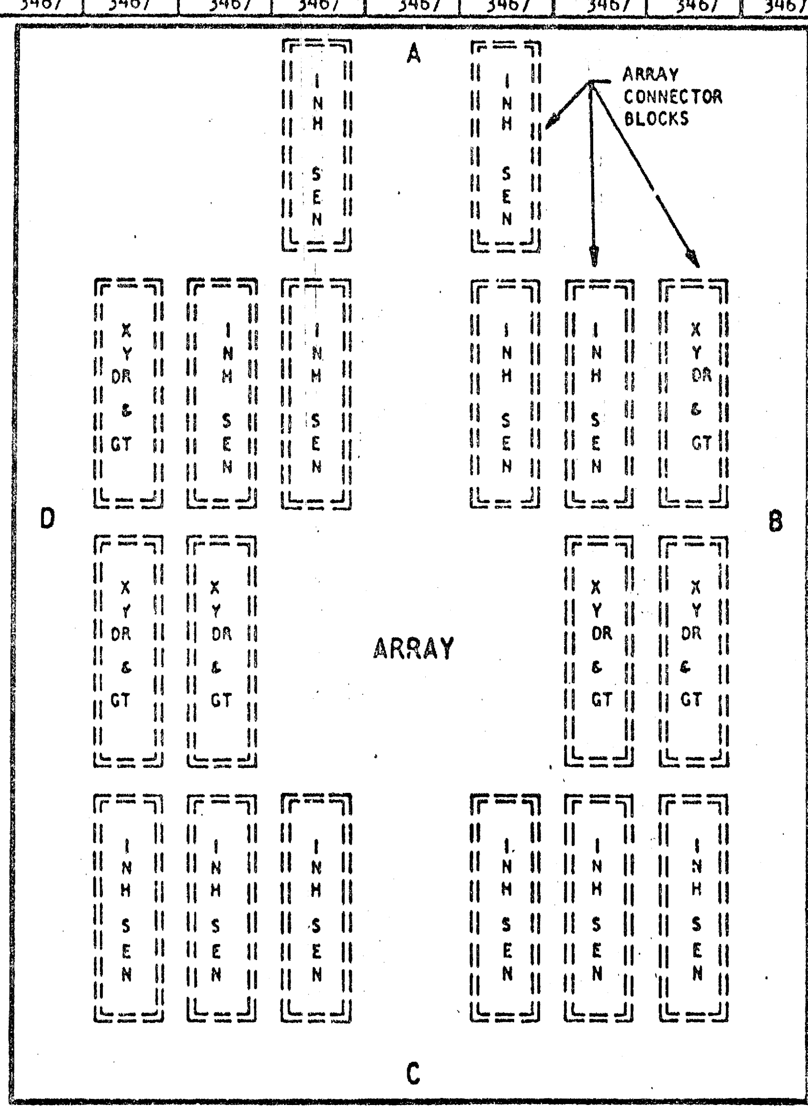
ARRAY CONNECTOR BLOCK



SLT BOARD (CARD SIDE)

	A	B	C	D	E	F	G	H	J	K	L	M	N
1	CONNECTOR 1			CONNECTOR 2				CONNECTOR 3			CONNECTOR 4		
2	VOLTAGE REGULATOR 3404	Y CURRENT CONTROL 3773	API & 9 AI INH BITS 0-8 * 3466	API & 9 AI INH BITS 0-8 3466	(hatched)	ADDR REG BITS INV 6-15 3132	POT V REF & SEN CTRL 3491 POT	LOGIC & ADDR REG BITS INV 3,4,5 0525	AUX RD DR & WR GT ** 3467	API & 9 AI INH BITS 9-17 3466	API & 9 AI INH BITS 9-17 * 3466	X CURRENT CONTROL 3773	POT CLOCK STROBE
3	INH SEN BITS 7&9 * 3475	INH SEN BITS 7&9 3475	Y RD GT - WR DR 0000 0001 0010 0011 3467	0100 0101 0110 0111 3467	1000 1001 1010 1011 3467	1100 1101 1110 1111 3467	Y RD DR, WR GT 000 001 010 011 3467	100 101 110 111 3467	X RD GT-WR DR 000 001 010 011 3467	100 101 110 111 3467	X RD DR, WR GT 000 001 010 011 3467	100 101 110 111 * 3467	4683

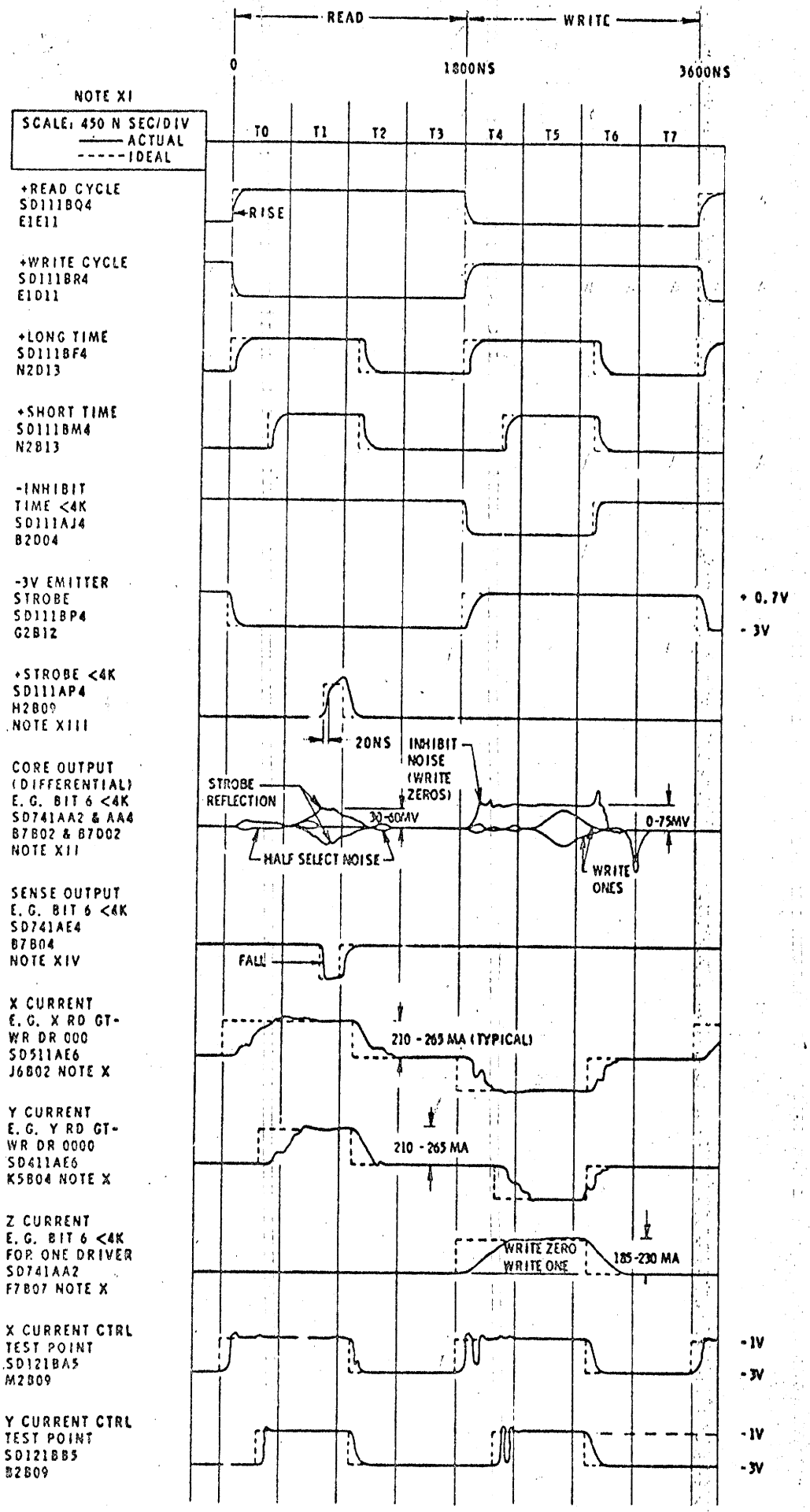
	A	B	M	N
4	INH SEN BITS 1&5 * 3475	INH SEN BITS 1&5 3475	INH SEN BITS 11&17 3475	INH SEN BITS 11&17 * 3475
5	INH SEN BITS 2&3 * 3475	INH SEN BITS 2&3 3475	INH SEN BITS 13&15 3475	INH SEN BITS 13&15 * 3475
6	INH SEN BITS 4&8 * 3475	INH SEN BITS 4&8 3475	INH SEN BITS 10&12 3475	INH SEN BITS 10&12 * 3475
7	INH SEN BITS 0&6 * 3475	INH SEN BITS 0&6 3475	INH SEN BITS 14&16 3475	INH SEN BITS 14&16 * 3475
8				



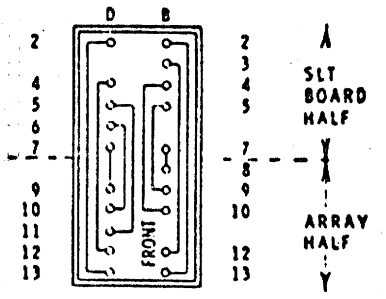
AIR FLOW

* 8K ONLY

** AUX FEATURE ONLY



ARRAY CONNECTOR BLOCK



NOTES

X CURRENTS MAY BE MEASURED BY REPLACING THE APPROPRIATE ARRAY CONNECTOR BLOCK WITH A JUMPER ASSEMBLY P/N 2182906 OR A CARD OFFSET P/N 452530. TEN 4.00 (101.6) JUMPERS P/N 452655 SHOULD BE USED ON THE CARD OFFSET IN A LAYOUT MATCHING THE CONNECTOR BLOCK LAYOUT ARRAY CONNECTOR BLOCKS SHOULD BE REMOVED WITH BLOCK TOOL ASM P/N 2108860

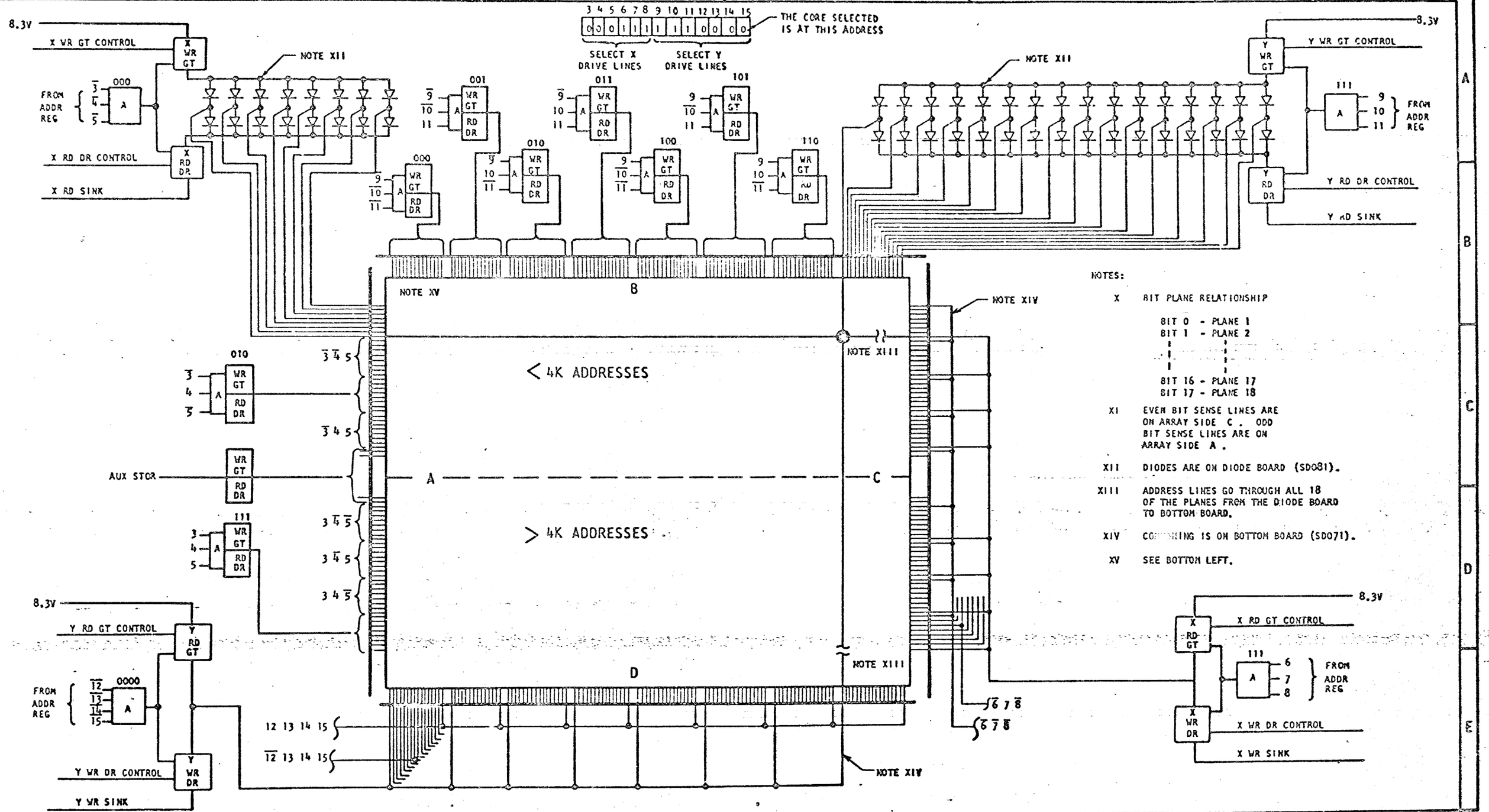
XI SYNC POINT +READ CYCLE (N2J06)

XII USE DIRECT TWISTED PAIR TERMINATING EACH LINE BY 150 OHM RESISTOR TO GROUND AT SCOPE OR CABLE DIFFERENTIAL ASM-SCOPE LEADS P/N 2182907

XIII STROBE OPTIMUM OCCURS WITH KNEE OF STROBE 20 NANOSECONDS PAST PEAK OF ONES PACK

XIV TYPICAL "ACCESS" TIME FROM READ CYCLE RISE (POSITIVE GOING) AND SENSE OUTPUT FALL (NEGATIVE GOING) IS 860 NS FOR 4K AND 900 NS FOR 8K MEASURED AT THE 1 VOLT LEVEL.

IBM			DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SJ-4 TIMING AND WAVEFORMS		19 AUG 65	414308			X PRINT TO ENG. SPEC. NO.	
DESIGN		MODEL	21 FEB 67	256302				
DETAIL	LD 21FEB67		11MAY67	731503				
CHECK		DRAW						SD031
APPRO		CHECK						



NOTES:

X BIT PLANE RELATIONSHIP

BIT 0 - PLANE 1
BIT 1 - PLANE 2
BIT 16 - PLANE 17
BIT 17 - PLANE 18

X1 EVEN BIT SENSE LINES ARE ON ARRAY SIDE C. ODD BIT SENSE LINES ARE ON ARRAY SIDE A.

XII DIODES ARE ON DIODE BOARD (SD081).

XIII ADDRESS LINES GO THROUGH ALL 18 OF THE PLANES FROM THE DIODE BOARD TO BOTTOM BOARD.

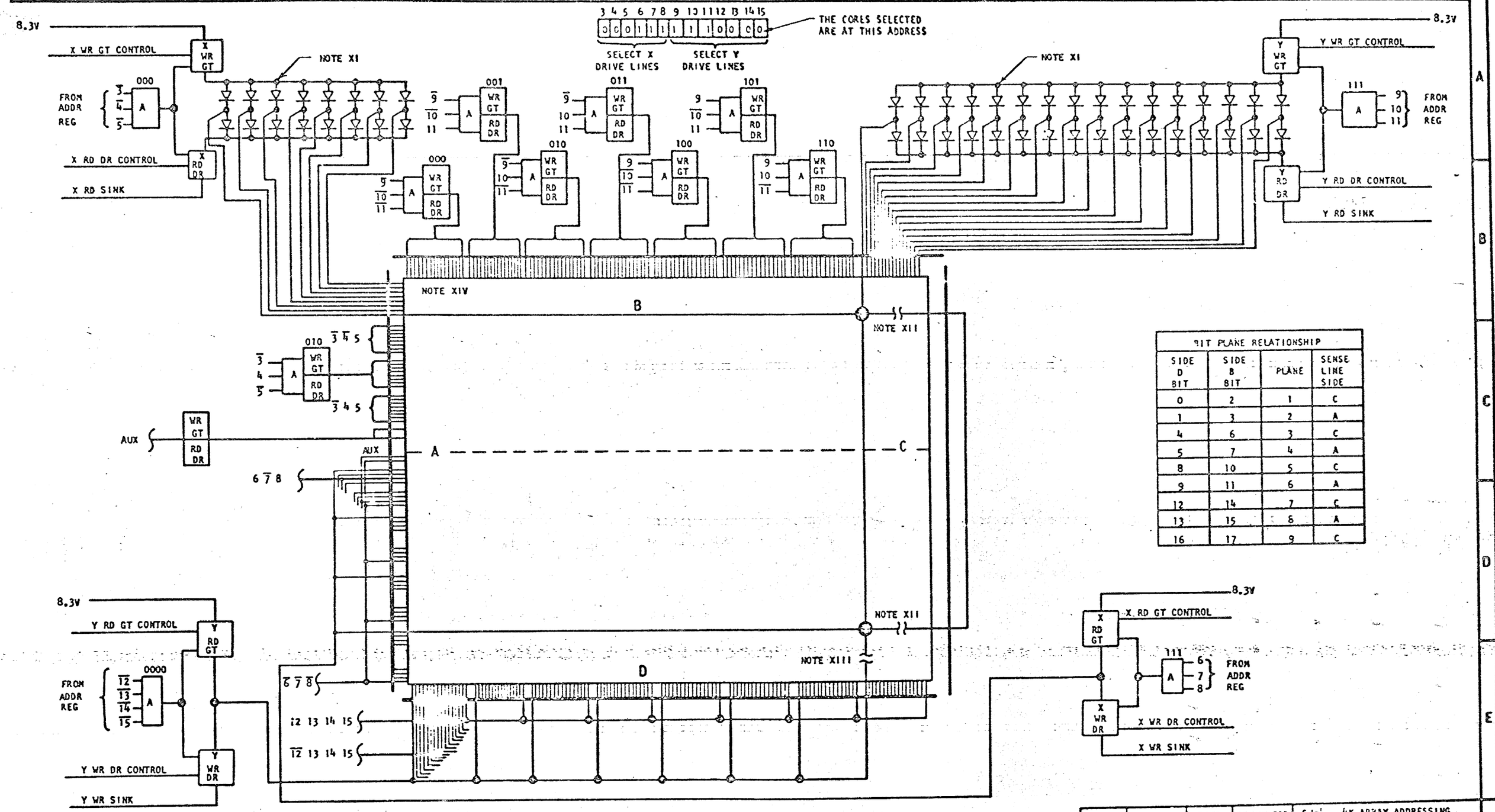
XIV CONNECTING IS ON BOTTOM BOARD (SD071).

XV SEE BOTTOM LEFT.

NOTES (CONTINUED):

XV THE CONNECTIONS BETWEEN DIODE BOARD AND ARRAY (OR ARRAY AND BOTTOM BOARD) ARE ACTUALLY ON ALTERNATE SIDES FOR ANY TWO ADJACENT ARRAY LINES.

DATE	EC NUMBER	DATE	EC NUMBER	SJ-4 8K ARRAY ADDRESSING			
19AUG65	414308						
				DATE	19AUG65	P/N	2196984
						TYPE	
				IBM		SD041	



BIT PLANE RELATIONSHIP			
SIDE D BIT	SIDE B BIT	PLANE	SENSE LINE SIDE
0	2	1	C
1	3	2	A
4	6	3	C
5	7	4	A
8	10	5	C
9	11	6	A
12	14	7	C
13	15	8	A
16	17	9	C

NOTES:

XI DIODES ARE ON DIODE BOARD (SD082).

XII X ADDRESS LINES FROM DIODE BOARD GO THROUGH THE ARRAY ON SIDE B, JUMPER ACROSS AT BOTTOM BOARD (SD072), AND RETURN VIA SIDE D TO DIODE BOARD FOR X COMMONING (SD082).

XIII Y ADDRESS LINES GO THROUGH THE ARRAY FROM DIODE BOARD AND ARE COMMONED ON THE BOTTOM BOARD (SD072).

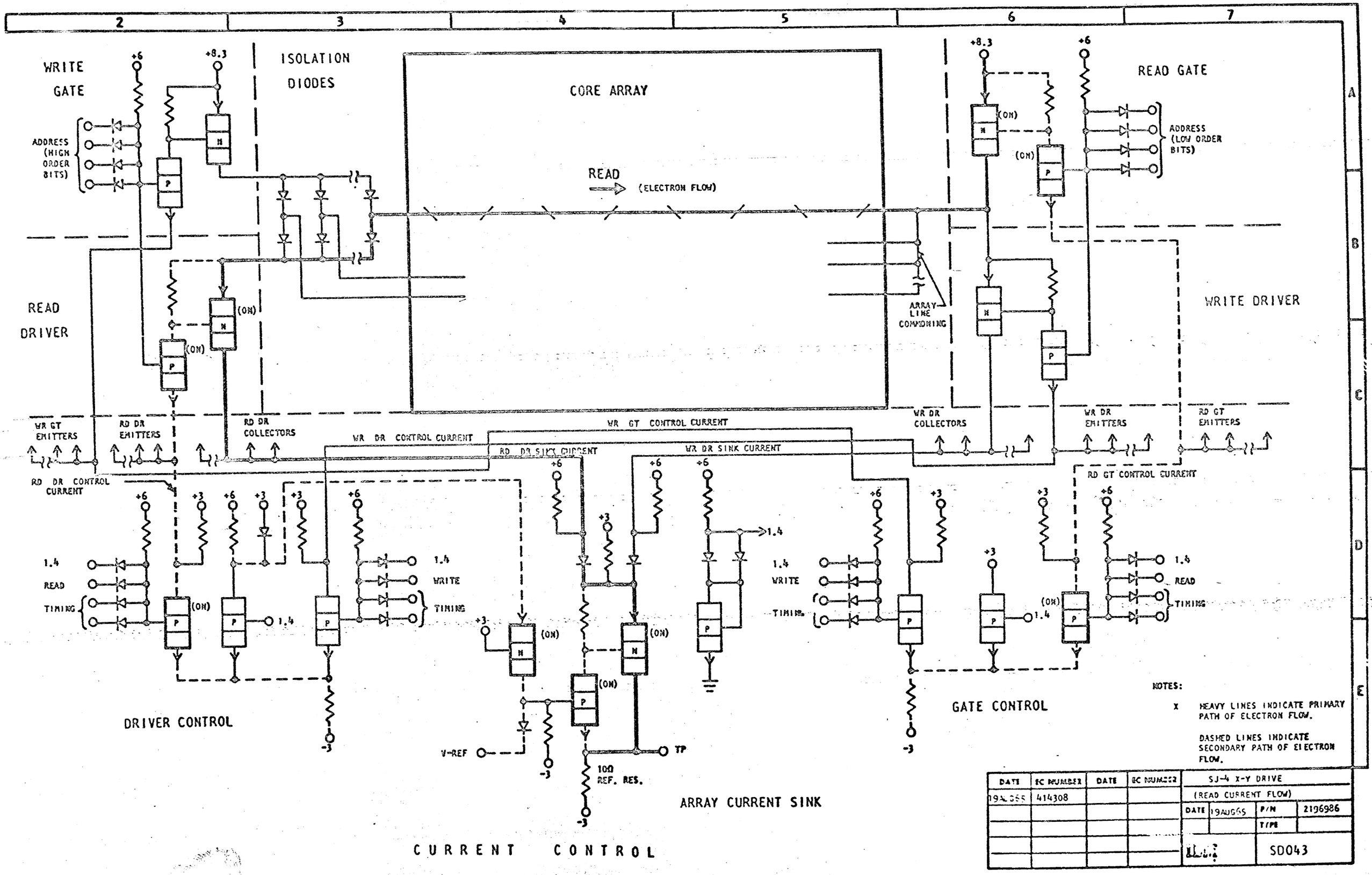
XIV THE CONNECTIONS BETWEEN DIODE BOARD AND ARRAY (OR ARRAY AND BOTTOM BOARD) ARE ACTUALLY ON ALTERNATE SIDES FOR ANY TWO ADJACENT ARRAY LINES.

DATE	EC NUMBER	DATE	EC NUMBER
23AUG65	414308		

SJ-4 4K ARRAY ADDRESSING

DATE 19AUG65 P/N 2196985

TYPE SD042



NOTES:

X HEAVY LINES INDICATE PRIMARY PATH OF ELECTRON FLOW.

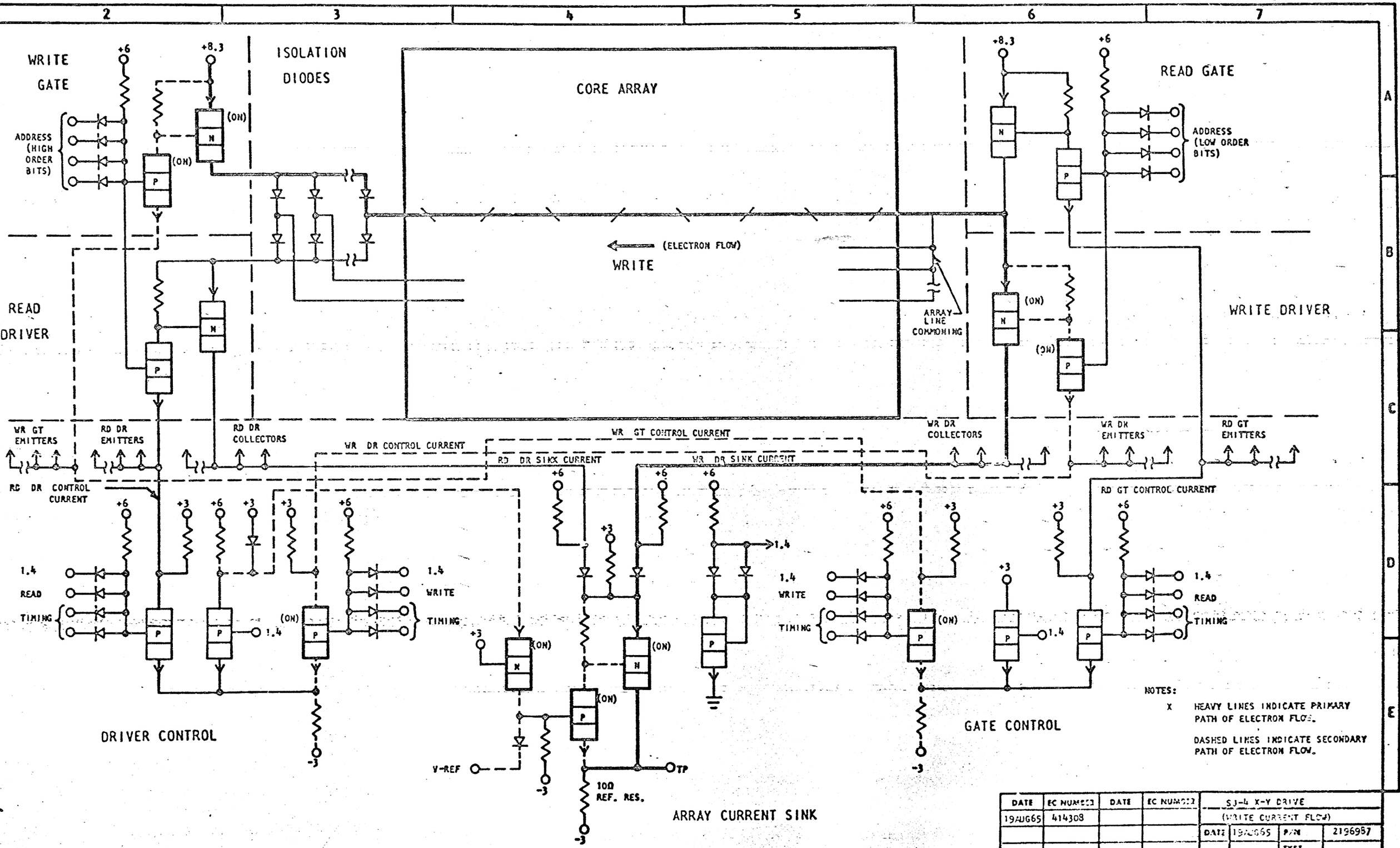
DASHED LINES INDICATE SECONDARY PATH OF ELECTRON FLOW.

DATE	EC NUMBER	DATE	EC NUMBER
19AUG65	414308		

SJ-4 X-Y DRIVE
(READ CURRENT FLOW)

DATE	19AUG65	P/N	2196986
		TYPE	

SD043



NOTES:

X HEAVY LINES INDICATE PRIMARY PATH OF ELECTRON FLOW.

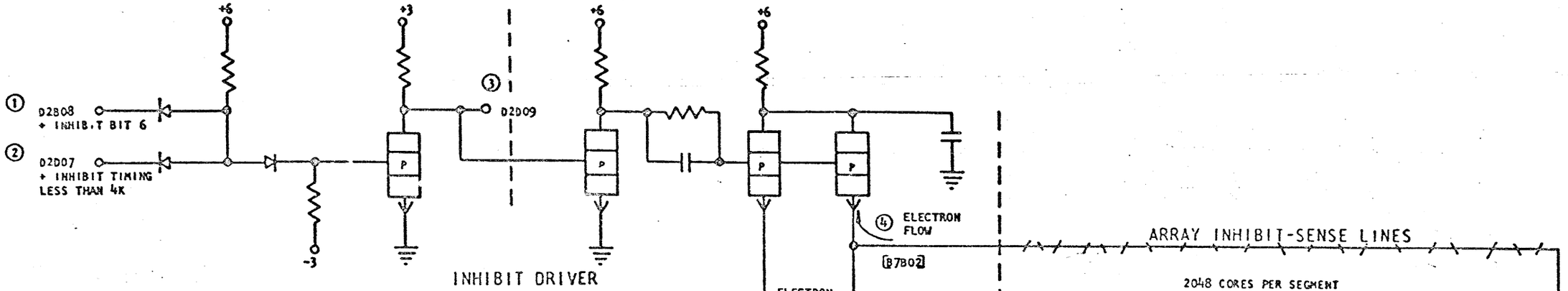
DASHED LINES INDICATE SECONDARY PATH OF ELECTRON FLOW.

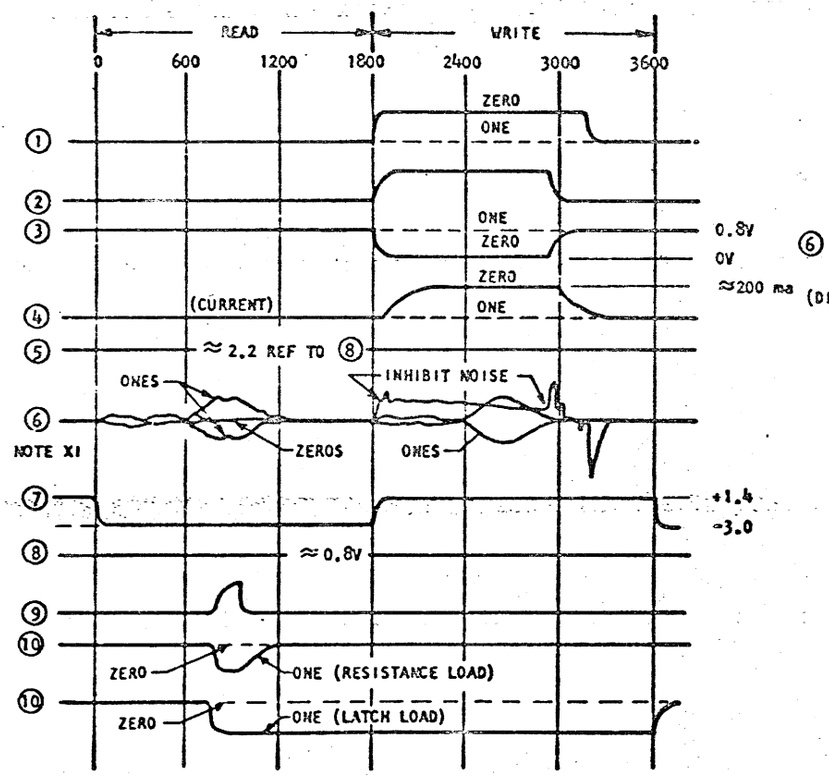
DATE	EC NUMBER	DATE	EC NUMBER
19AUG65	414308		

SJ-4 X-Y DRIVE
(WRITE CURRENT FLOW)

DATE 19AUG65 P/N 2196987
TYPE

IBM S0044





NOTE:
X SYNC POINT: + READ CYCLE (H2J05).
X1 SEE SD031.

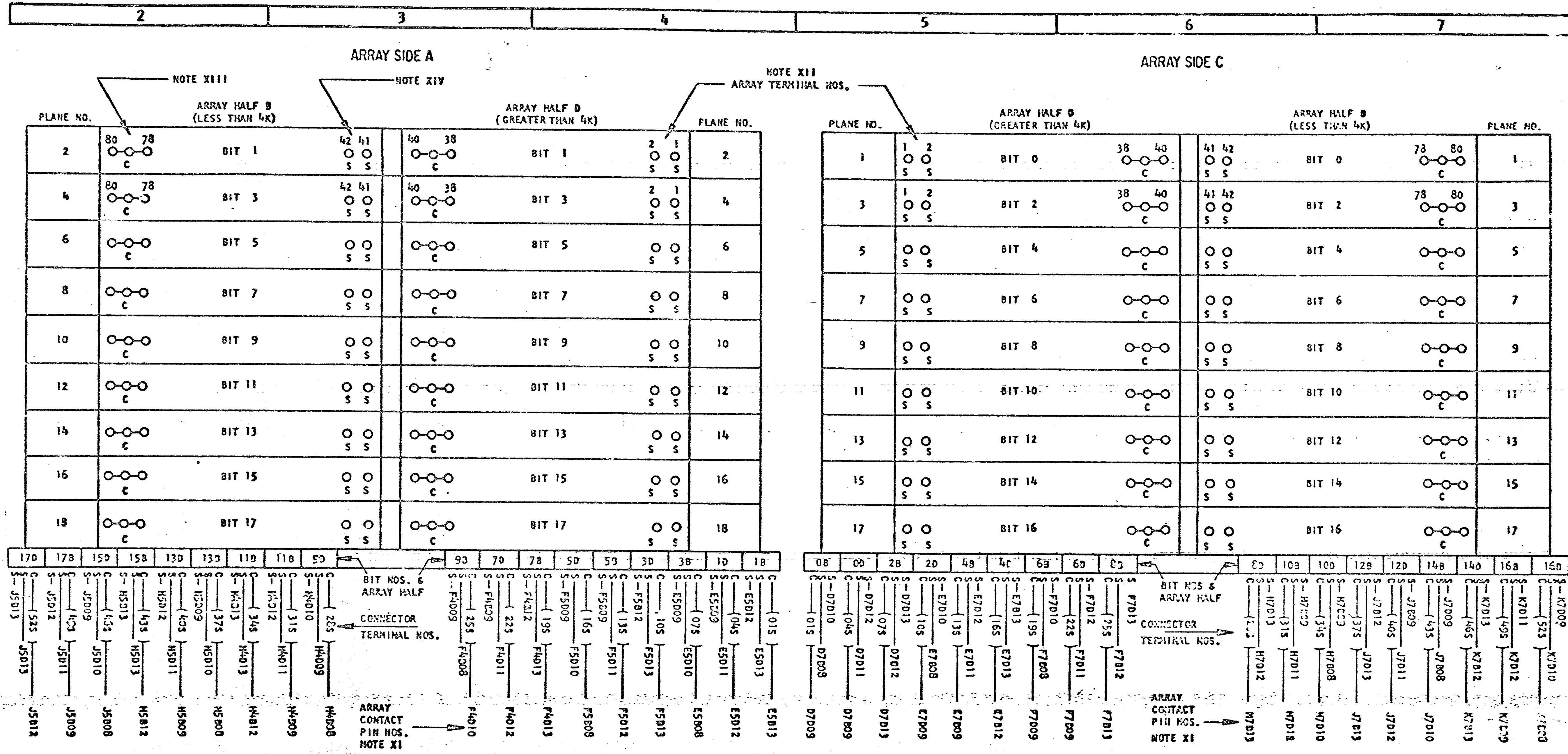
SENSE AMPLIFIER

DATE	EC NUMBER	DATE	EC NUMBER
19AUG65	414308		

SJ-4 INHIBIT SENSE (BIT 6 <4K)

DATE	19AUG65	P/N	2196988
		TYPE	

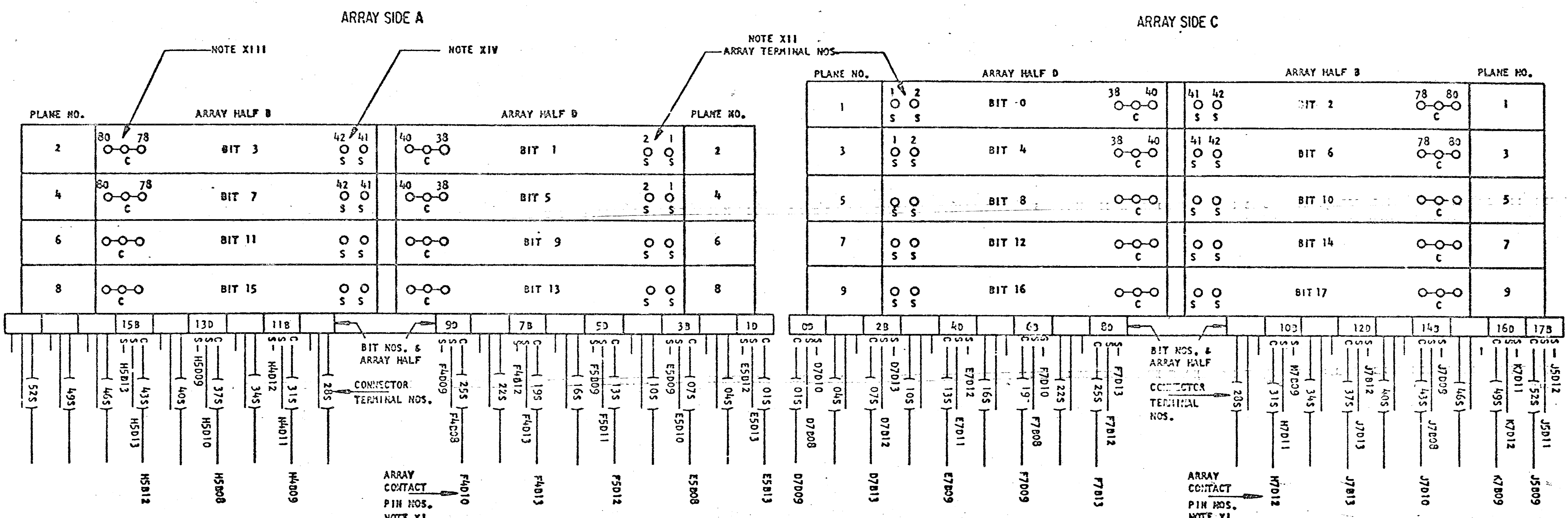
IBM SD051



NOTES:

- XI EACH ARRAY CONTACT PIN IS JUMPERED TO A CONNECTOR TERMINAL VIA A PRINTED CIRCUIT (SEE SD012)
- XII EACH CONNECTOR TERMINAL IS JUMPERED TO AN ARRAY TERMINAL VIA A DISCRETE WIRE (SEE SD012.)THE WIRES ARE GOUPED IN TWISTED TRIPLETS.
- XIII ARRAY TERMINALS MARKED C ARE COMMONED, E.G. 38-40 OR 78-80
- XIV ARRAY TERMINAL MARKED S IS JUMPERED TO EITHER CONNECTOR TERMINAL MARKED S FOR A GIVEN BIT AND ARRAY HALF.

DATE	EC NUMBER	DATE	EC NUMBER	SJ-4 8K
AUG 65	414303			SENSE CONNECTIONS
				DATE AUG 65 P/N 2196933
				TYPE
				IBM SD061



NOTES:

XI EACH ARRAY CONTACT PIN IS JUMPERED TO A CONNECTOR TERMINAL VIA A PRINTED CIRCUIT (SEE SD012).

XII EACH CONNECTOR TERMINAL IS JUMPERED TO AN ARRAY TERMINAL VIA A DISCRETE WIRE (SEE SD012.) THE WIRES ARE GROUPED IN TWISTED TRIPLETS.

XIII ARRAY TERMINALS MARKED C ARE COMMONED, E.G. 38-40 OR 78-80.

XIV ARRAY TERMINAL MARKED S IS JUMPERED TO EITHER CONNECTOR TERMINAL MARKED S FOR A GIVEN BIT AND ARRAY HALF.

DATE	EC NUMBER	DATE	EC NUMBER
AUG 65	414305		

SJ-4 4K

SENSE CONNECTIONS

DATE	AUG 65	P/N	2196997
		TYPE	

IBM SD062

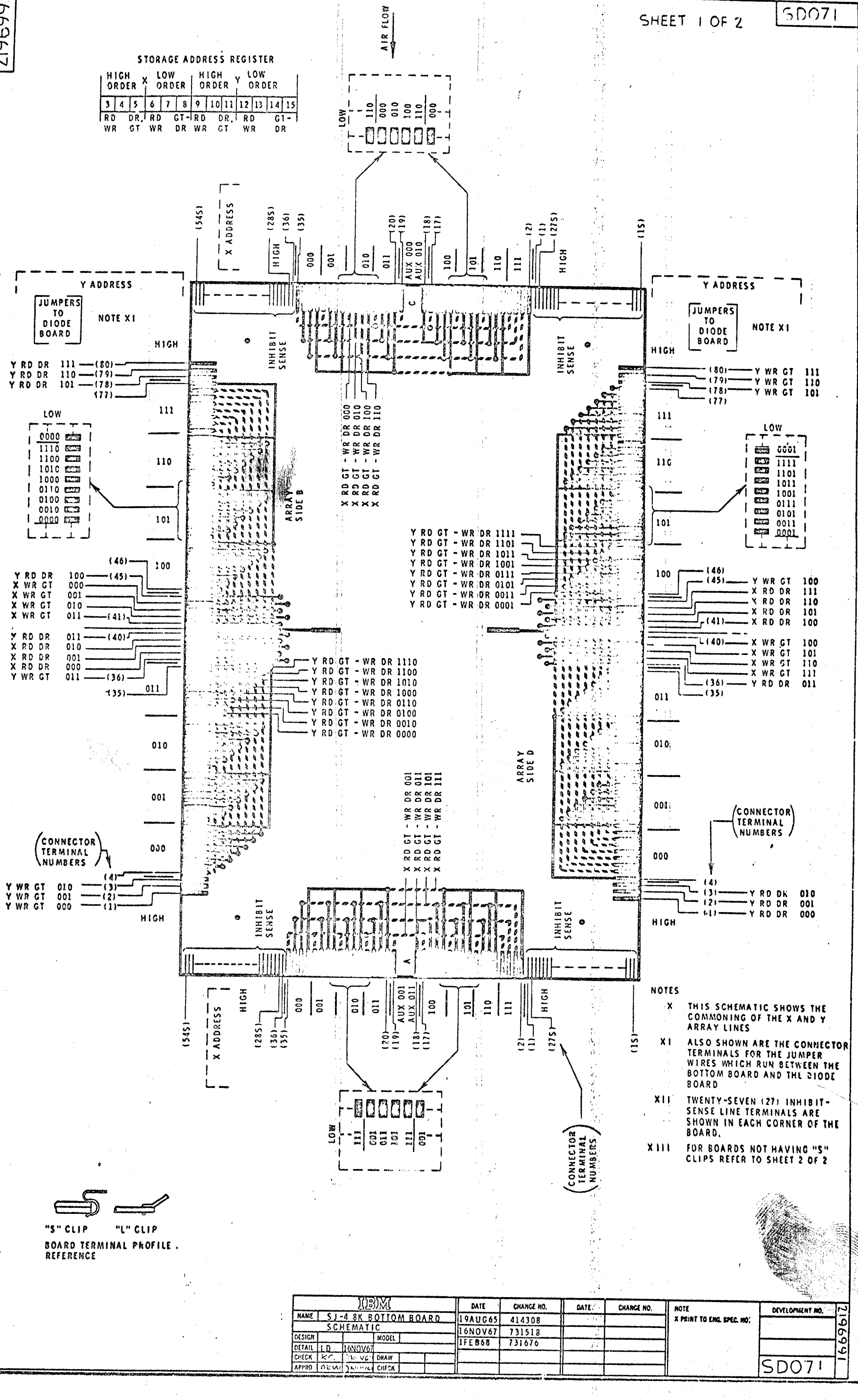
2196991

SHEET 1 OF 2

SD071

STORAGE ADDRESS REGISTER

HIGH ORDER X			LOW ORDER			HIGH ORDER Y			LOW ORDER			
3	4	5	6	7	8	9	10	11	12	13	14	15
RD WR		DR GT	RD WR		GT DR	RD WR		DR GT	RD WR		GT DR	



NOTES

X THIS SCHEMATIC SHOWS THE COMMONING OF THE X AND Y ARRAY LINES

X1 ALSO SHOWN ARE THE CONNECTOR TERMINALS FOR THE JUMPER WIRES WHICH RUN BETWEEN THE BOTTOM BOARD AND THE DIODE BOARD

X11 TWENTY-SEVEN (27) INHIBIT-SENSE LINE TERMINALS ARE SHOWN IN EACH CORNER OF THE BOARD.

X111 FOR BOARDS NOT HAVING "S" CLIPS REFER TO SHEET 2 OF 2

"S" CLIP "L" CLIP

BOARD TERMINAL PROFILE REFERENCE

IBM				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SJ-4 8K BOTTOM BOARD			19AUG65	414308			X PRINT TO ENG. SPEC. NO.	2196991
	SCHEMATIC			16NOV67	731518				
DESIGN		MODEL		1FEB68	731676				
DETAIL	LD 16NOV67								SD071
CHECK	KC	DRAW							
APPRO	AEW	CHECK							

2196991

SHEET 2 OF 2

SD071

STORAGE ADDRESS REGISTER

X HIGH ORDER			X LOW ORDER			Y HIGH ORDER			Y LOW ORDER			
3	4	5	6	7	8	9	10	11	12	13	14	15
RD WR		DR GT	RD WR		GT DR	RD WR		DR GT	RD WR		GT DR	

AIR FLOW

NUMBERING SEQUENCE FOR SENSE CONNECTIONS

DETAIL B

DETAIL A

LOW 110 000 010 100 110 000

X ADDRESS (54S) (28S) HIGH (36) (35) 000 001 010 011 (20) (19) AUX 000 AUX 010 (18) (17) 100 101 110 111 (2) (1) HIGH (27S) (15)

Y ADDRESS — JUMPERS TO DIODE BOARD — NOTE X1 — HIGH

AUX RD DR (81)
Y RD DR 111 (80)
Y RD DR 110 (79)
Y RD DR 101 (78)
(77)

LOW: 0000, 1110, 1100, 1010, 1000, 0110, 0100, 0010, 0000

111 / 110 / 101

(46) 100
Y RD DR 100 (45)
X WR GT 000
X WR GT 001
X WR GT 010
X WR GT 011 (41)

X RD DR 011 (40)
X RD DR 010
X RD DR 001
X RD DR 000
Y WR GT 011 (36)
(35) 011

010

001

000

(CONNECTOR TERMINAL NUMBERS)
(4)
Y WR GT 010 (3)
Y WR GT 001 (2)
Y WR GT 000 (1)
HIGH

INHIBIT SENSE DETAIL B

ARRAY SIDE B

X RD GT-WR DR 000
X RD GT-WR DR 010
X RD GT-WR DR 100
X RD GT-WR DR 110

Y RD GT-WR DR 1110
Y RD GT-WR DR 1100
Y RD GT-WR DR 1010
Y RD GT-WR DR 1000
Y RD GT-WR DR 0110
Y RD GT-WR DR 0100
Y RD GT-WR DR 0010
Y RD GT-WR DR 0000

X RD GT-WR DR 001
X RD GT-WR DR 011
X RD GT-WR DR 101
X RD GT-WR DR 111

INHIBIT SENSE DETAIL A

ARRAY SIDE D

Y DR GT-WR DR 1111
Y RD GT-WR DR 1101
Y RD GT-WR DR 1011
Y RD GT-WR DR 1001
Y RD GT-WR DR 0111
Y RD GT-WR DR 0101
Y RD GT-WR DR 0011
Y RD GT-WR DR 0001

Y ADDRESS — JUMPERS TO DIODE BOARD — NOTE X1 — HIGH

(81) — Y WR GT 111
(80) — Y WR GT 110
(79) — Y WR GT 101
(78)

111 / 110 / 101

LOW: 0001, 1111, 1101, 1011, 1001, 0111, 0101, 0011, 0001

100
(47)
(46) — Y WR GT 100
X RD DR 111
X RD DR 110
X RD DR 101
(42) — X RD DR 100

(41) — X WR GT 100
X WR GT 101
X WR GT 110
X WR GT 111
(37) Y RD DR 011
(36)

011 / 010 / 001 / 000

(CONNECTOR TERMINAL NUMBERS)
(5)
(4) — Y RD DR 010
(3) — Y RD DR 001
(2) — Y RD DR 000
(1) — AUX WR GT
HIGH

X ADDRESS (54S) HIGH (28S) (36) (35) 000 001 010 011 (20) (19) AUX 001 AUX 011 (18) (17) 100 101 110 111 (2) (1) HIGH (27S) (15)

LOW 111 001 011 101 111 001

(CONNECTOR TERMINAL NUMBERS)

IBM				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SJ-4 8K BOTTOM BOARD			19AUG65	414308			X PRINT TO ENG. SPEC. NO.	
SCHEMATIC				16NOV67	731518				
DESIGN			MODEL	2FEB68	731676				
DETAIL	LD	8NOV67							
CHECK	RG	9 Nov 67	DRAW						SD071
APPRO	ACW	9 Nov 67	CHECK						

1666L.77

2196992

SD072

SHEET 1 OF 2

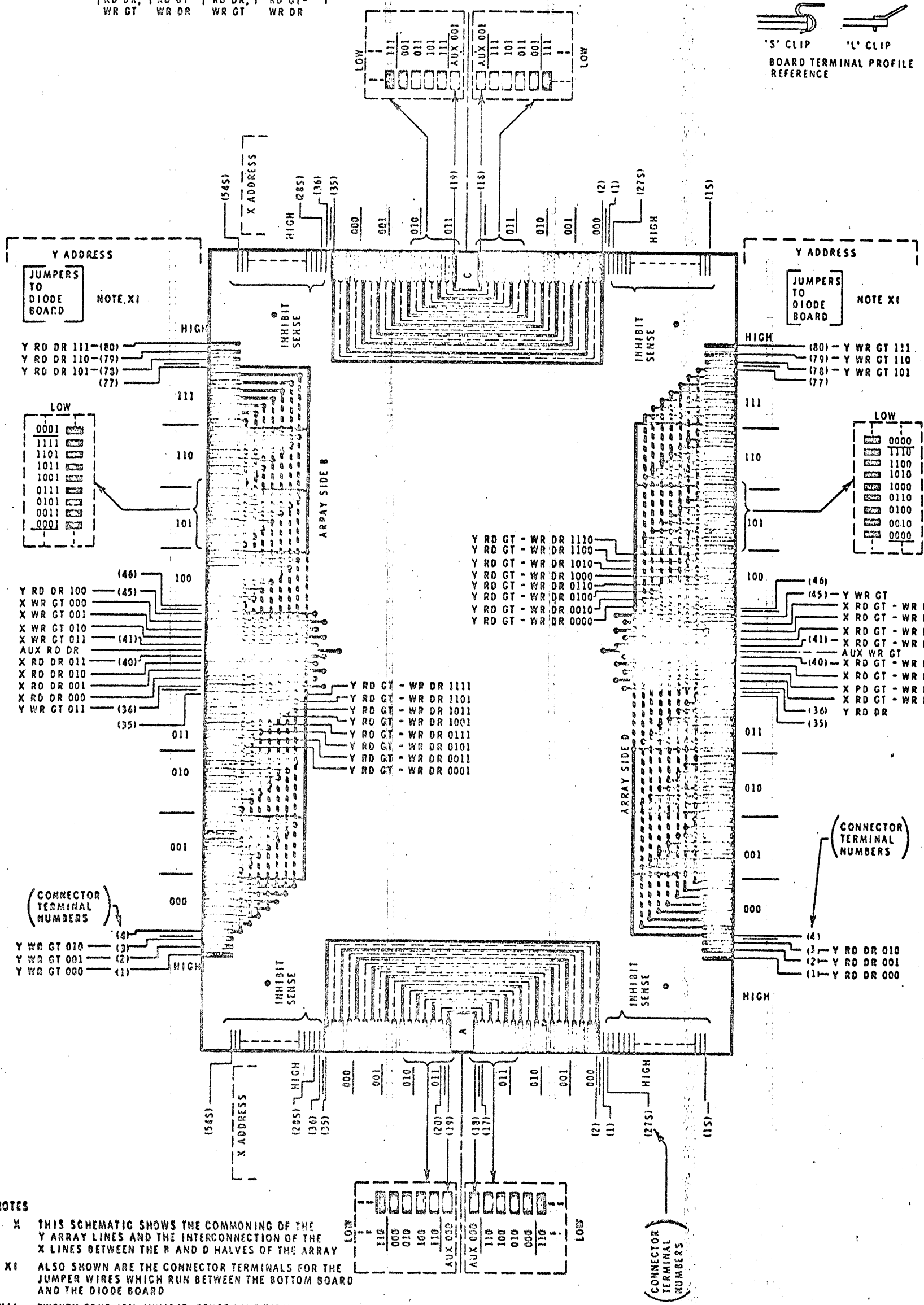
AIR FLOW

STORAGE ADDRESS REGISTER

X						Y				
HIGH ORDER			LOW ORDER			HIGH ORDER			LOW ORDER		
3	4	5	6	7	8	9	10	11	12	13	14	15
RD DR, WR GT			RD GT- WR DR			RD DR, WR GT			RD GT- WR DR			

'S' CLIP 'L' CLIP

BOARD TERMINAL PROFILE REFERENCE



NOTES

X THIS SCHEMATIC SHOWS THE COMMONING OF THE Y ARRAY LINES AND THE INTERCONNECTION OF THE X LINES BETWEEN THE B AND D HALVES OF THE ARRAY

XI ALSO SHOWN ARE THE CONNECTOR TERMINALS FOR THE JUMPER WIRES WHICH RUN BETWEEN THE BOTTOM BOARD AND THE DIODE BOARD

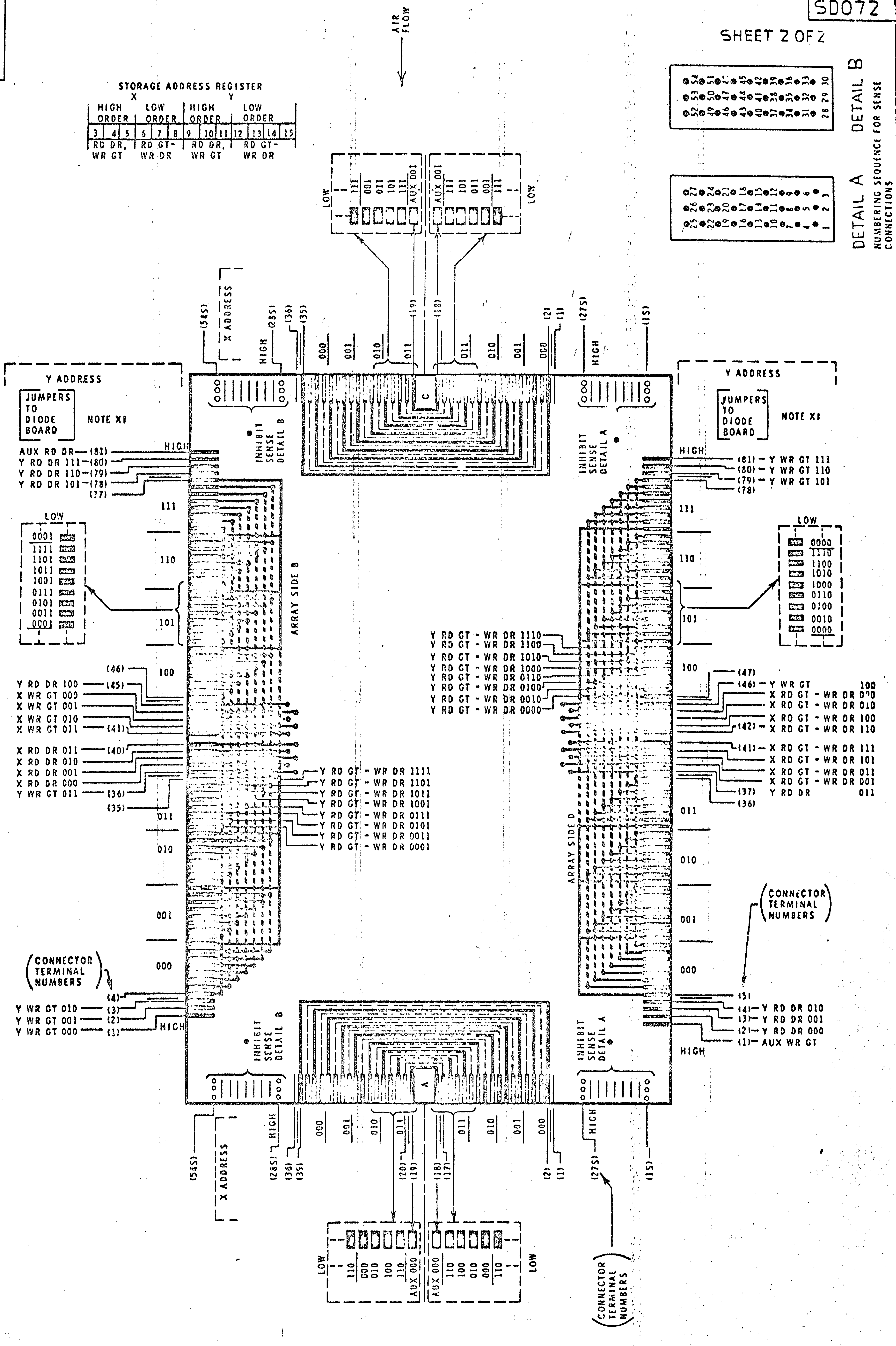
XII TWENTY FOUR (24) INHIBIT-SENSE LINE TERMINALS ARE ACTIVE ON SIDE A AND 30 ON SIDE C

XIII REFER TO SHEET 2 OF 2 FOR BOARDS NOT HAVING 'S' CLIPS

IBM	DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME SJ-4 4K BOTTOM BOARD	19AUG65	414308			X PRINT TO ENG. SPEC. NO.	
SCHEMATIC	2FEB68	731676				
DESIGN MODEL						
DETAIL KTS 2FEB68						
CHECK DRAW						
APPRO CHECK						SD072

2196992

2196992


STORAGE ADDRESS REGISTER
X
Y
HIGH ORDER
LOW ORDER
HIGH ORDER
LOW ORDER
3 4 5 6 7 8 9 10 11 12 13 14 15
RD DR, WR GT
RD GT- WR DR
RD DR, WR GT
RD GT- WR DR
AIR FLOW
DETAIL A
DETAIL B
NUMBERING SEQUENCE FOR SENSE CONNECTIONS
Y ADDRESS
JUMPERS TO DIODE BOARD
NOTE X1
X ADDRESS
HIGH
LOW
INHIBIT SENSE DETAIL B
INHIBIT SENSE DETAIL A
ARRAY SIDE B
ARRAY SIDE D
AUX RD DR—(81)
Y RD DR 111—(80)
Y RD DR 110—(79)
Y RD DR 101—(78)
(77)
(81)— Y WR GT 111
(80)— Y WR GT 110
(79)— Y WR GT 101
(78)
Y RD DR 100
X WR GT 000
X WR GT 001
X WR GT 010
X WR GT 011
X RD DR 011
X RD DR 010
X RD DR 001
X RD DR 000
Y WR GT 011
Y WR GT 100
X RD GT - WR DR 000
X RD GT - WR DR 010
X RD GT - WR DR 100
X RD GT - WR DR 110
X RD GT - WR DR 111
X RD GT - WR DR 101
X RD GT - WR DR 011
X RD GT - WR DR 001
Y RD DR 011
Y RD GT - WR DR 1110
Y RD GT - WR DR 1100
Y RD GT - WR DR 1010
Y RD GT - WR DR 1000
Y RD GT - WR DR 0110
Y RD GT - WR DR 0100
Y RD GT - WR DR 0010
Y RD GT - WR DR 0000
Y RD GT - WR DR 1111
Y RD GT - WR DR 1101
Y RD GT - WR DR 1011
Y RD GT - WR DR 1001
Y RD GT - WR DR 0111
Y RD GT - WR DR 0101
Y RD GT - WR DR 0011
Y RD GT - WR DR 0001
CONNECTOR TERMINAL NUMBERS
Y WR GT 010
Y WR GT 001
Y WR GT 000
Y RD DR 010
Y RD DR 001
Y RD DR 000
AUX WR GT
AUX 001
AUX 000

IBM				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SJ-4 4K BOTTOM BOARD			19AUG65	414308			X PRINT TO ENG. SPEC. NO.	
	SCHEMATIC			2FFB68	731676				
DESIGN		MODEL							
DETAIL	KTS 2FEB68								
CHECK		DRAW							
APPRO		CHECK							SD072

2196992

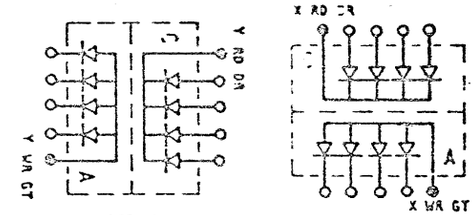
SHEET 1 OF 2

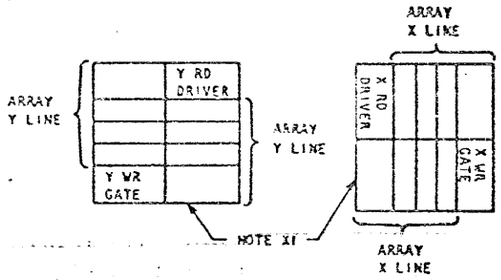
STORAGE ADDRESS REGISTER

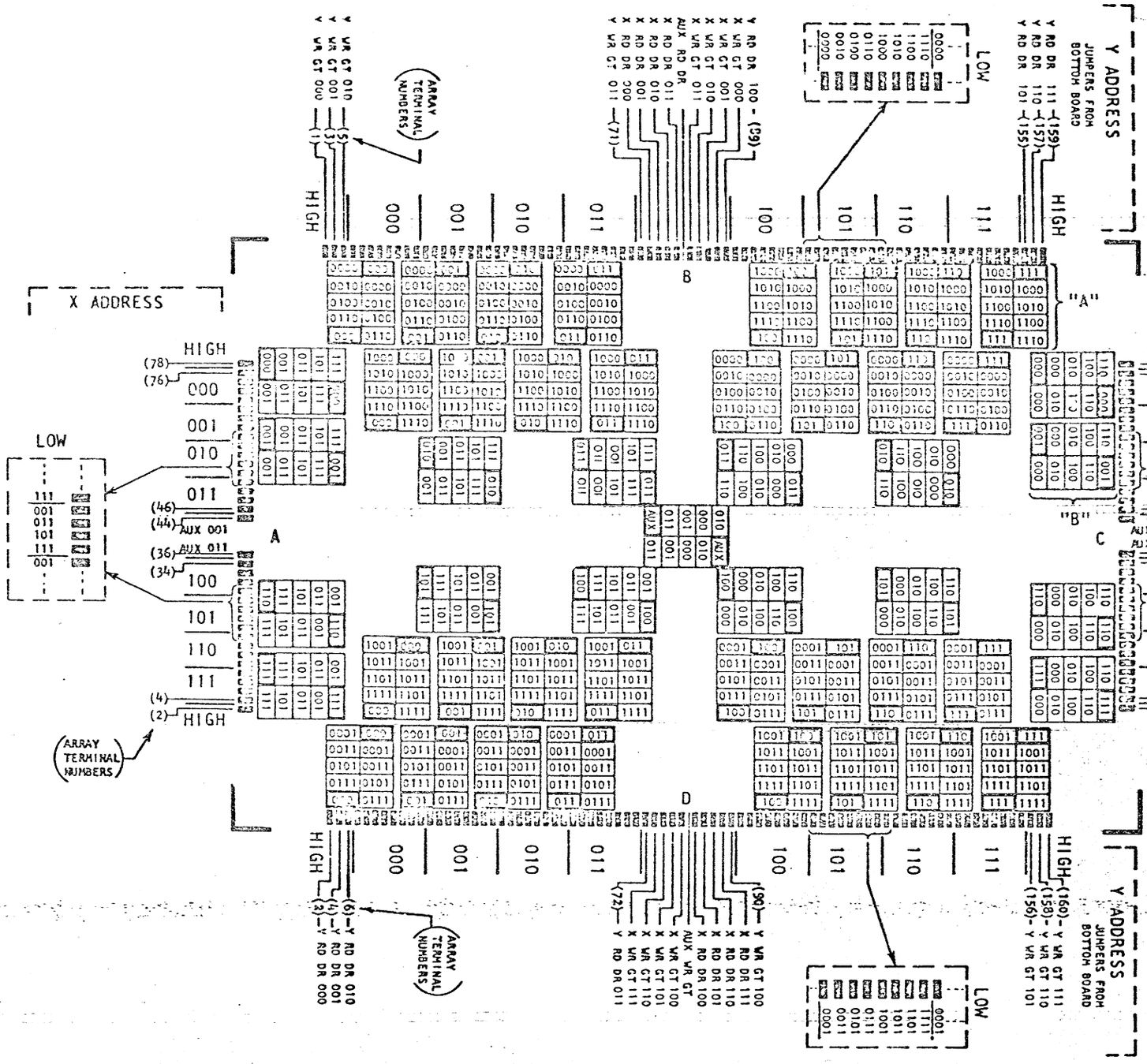
X						Y					
HIGH ORDER			LOW ORDER			HIGH ORDER			LOW ORDER		
3	4	5	6	7	8	9	10	11	12	13	14	15
RD WR		DR, GT	RD WR		GT-DR	RD WR		DR, GT	RD WR		GT-DR

NOTE X

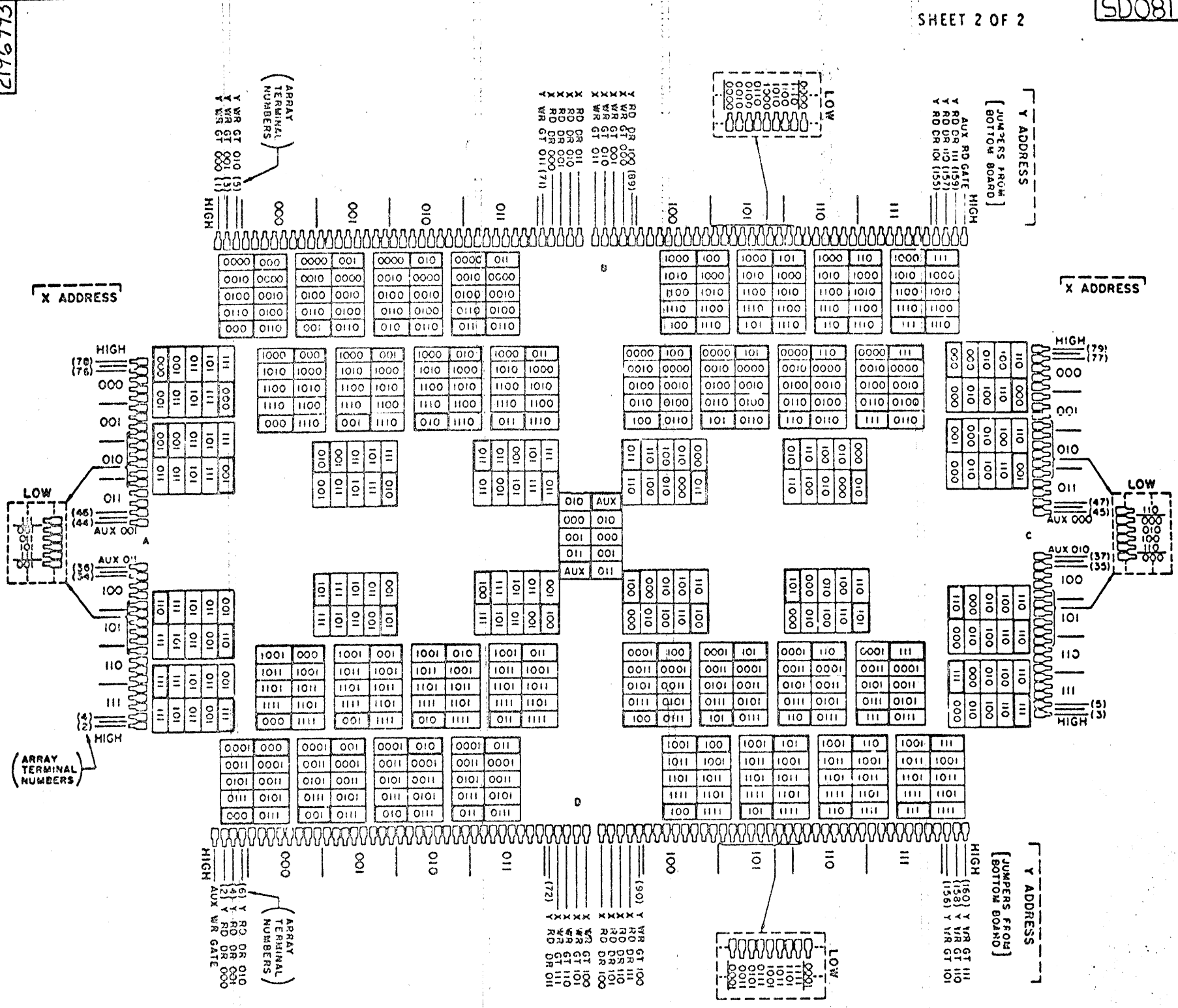
DIODE PACS







DATE	EC NUMBER	DA E	EC NUMBER	SJ-4 8K DIODE BOARD			
19AUG65	414308			SCHEMATIC			
17 FEB67	256302			DATE	19AUG65	P N	2196993
11MAY67	731503					TYPE	
25SEP67	730728			IBM		SD081	
1FEB68	731670						

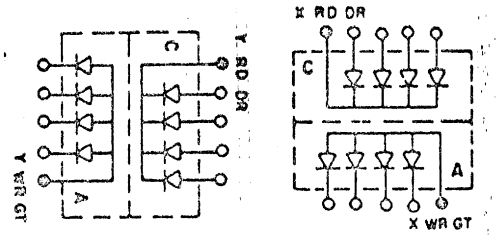


STORAGE ADDRESS REGISTER

HIGH ORDER X			LOW ORDER X			HIGH ORDER Y			LOW ORDER Y			
3	4	5	6	7	8	9	10	11	12	13	14	15
RD DR, WR GT			RD GT-WR DR			RD DR, WR GT			RD GT-WR DR			

(NOTE X)

DIODE PACS

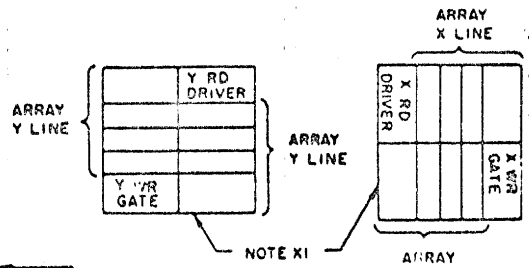


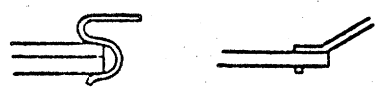
NOTES

X USE SHEET 1 OF 2 FOR DIODE BOARDS HAVING "S" TYPE TERMINALS

XI TO LOCATE AN ARRAY LINE USE THE HIGH AND LOW BINARY NOTATION OF THE STORAGE ADDRESS REGISTER AS SHOWN ON THIS PAGE

XII LEAST SIGNIFICANT ADDRESS BIT IS ON RIGHT OR Y AND BOTTOM FOR X



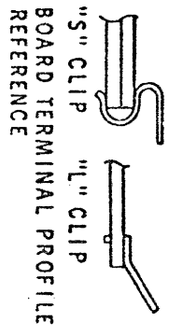


BOARD TERMINAL PROFILES-REF

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SJ-4 8K DIODE BOARD			19AUG65	414308			X PRINT TO ENG. SPEC. NO.	
	SCHEMATIC			17FEB67	256302				
DESIGN	KE		MODEL	11MAY67	731503				
DETAIL				21SEP67	730728				
CHECK	[illegible]	DRAW	KE 29MAR67	1FEB 68	731676				SD081
APPRO		CHECK							

2196993

SHEET 1 OF 2



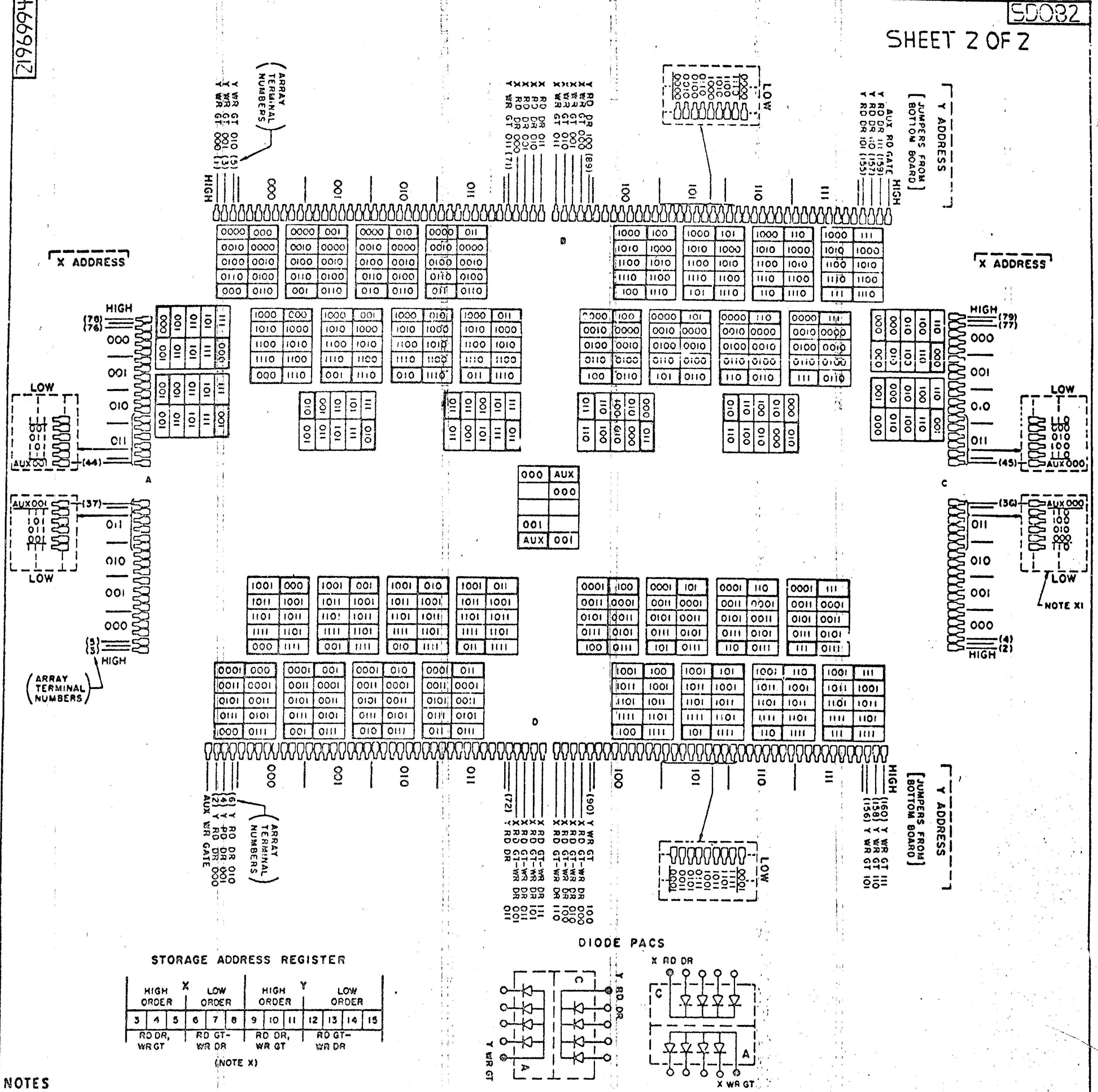
STORAGE ADDRESS REGISTER

X						Y					
HIGH ORDER			LOW ORDER			HIGH ORDER			LOW ORDER		
3	4	5	6	7	8	9	10	11	12	13	14	15
RD DR, WR GT			RD GT-WR DR			RD DR, WR GT			RD GT-WR DR		

NOTE X

DATE	EC NUMBER	DATE	EC NUMBER	SJ-4 4K DIODE BOARD			
19AUG65	414308			SCHEMATIC			
17 FEB 67	256302			DATE	19AUG65	P N	2196994
11MAY67	731503					TYPE	
2FEB68	731676			IBM		S0082	

2169617 4669994



NOTES

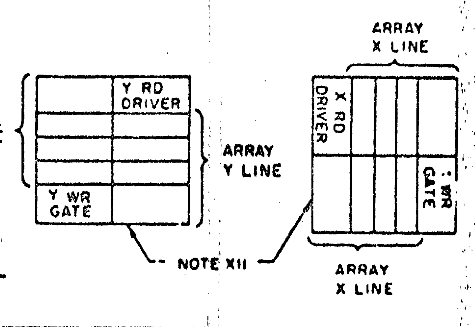
X TO LOCATE AN ARRAY LINE, USE THE HIGH AND LOW BINARY NOTATION OF THE STORAGE ADDRESS REGISTER AS SHOWN ON THIS PAGE

XI THE X RD GT-WR DR (LOW ORDER X) COMMONING IS ON THE D HALF OF THE A AND C SIDES OF THE DIODE BOARD

XII LEAST SIGNIFICANT ADDRESS BIT IS ON RIGHT FOR Y AND BOTTOM FOR X

XIII USE SHEET 1 OF 2 FOR DIODE BOARDS HAVING "S" TYPE TERMINALS

XIV USE SHEET 2 OF 2 FOR DIODE BOARDS HAVING "L" TYPE TERMINALS



INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO	DATE	CHANGE NO	NOTE	DEVELOPMENT NO.
NAME SJ-4 4K DIODE BOARD SCHEMATIC	65	414303			X PRINT TO ENG. SPEC. NO.	
DESIGN / MODEL	17FEB67	257302				
DETAIL	11MAY67	7 503				
CHECK / DRAW KE 29MAY	2FEB73	735676				SD082
APPRO / CHECK						4669994

A1 CONNECTOR
E09 SD611AA4
E11 SD721AK4

A2 SINGLE CARD
5803484 3484
SD221 A4

A3 SINGLE CARD 8K
5803475 3475
SD751 A1 A2
SD741 A3 A4

A4 SINGLE CARD 8K
5803475 3475
SD731 A1 A2
SD711 A3 A4

A5 SINGLE CARD 8K
5803475 3475
SD721 A1 A2 A3 A4

A6 SINGLE CARD 8K
5803475 3475
SD751 A1 A2
SD731 A3 A4

A7 SINGLE CARD 8K
5803475 3475
SD711 A1 A2
SD741 A3 A4

B1 CONNECTOR
A09 SD611AA4
A11 SD711AJ4
B09 SD611AB4
B1* SD711AK4
C09 SD611AC4
C11 SD721AJ4
D09 SD611AD4
D11 SD721AK4
E09 SD611AE4
E11 SD731AJ4

B2 SINGLE CARD
5803773 3773
SD121 AA AB AC AD AE AF
AG AH AJ AK AL AM
SD111 BA

B3 SINGLE CARD
5803475 3475
SD751 A1 A2
SD741 A3 A4

B4 SINGLE CARD
5803475 3475
SD731 A1 A2
SD711 A3 A4

B5 SINGLE CARD
5803475 3475
SD721 A1 A2 A3 A4

B6 SINGLE CARD
5803475 3475
SD751 A1 A2
SD731 A3 A4

B7 SINGLE CARD
5803475 3475
SD711 A1 A2
SD741 A3 A4

C1 CONNECTOR
A11 SD741AK4
B09 SD611AF4
B11 SD731AK4
C09 SD611AG4
C11 SD741AJ4
D09 SD611AH4
D11 SD741AK4
E09 SD611AJ4
E11 SD751AJ4

C2 SINGLE CARD 8K
5803466 3466
SD641 AA AB AC AD AE AF
AG AH AJ AK

C3 SINGLE CARD
5803467 3467
SD411 AA AB AC AD AE AF
AG AH AJ AK AL AM

D1 CONNECTOR
A09 SD621AA4
A11 SD751AK4
E09 SD331AA4
E11 SD111BA4

D2 SINGLE CARD
5803466 3466
SD631 AA AB AC AD AE AF
AG AH AJ AK

D3 SINGLE CARD
5803467 3467
SD421 AA AB AC AD AE AF
AG AH AJ AK AL AM

D5 SINGLE CARD
CORE
SD561

D6 SINGLE CARD
CORE
SD561

D7 SINGLE CARD
CORE
SD721

E1 CONNECTOR
A09 SD331AA4
A11 SD331AP4
B09 SD321AJ4
B11 SD321AL4
C09 SD321AE4
C11 SD321AG4
D09 SD331AF4
D11 SD111BR4
E11 SD111BQ4

E3 SINGLE CARD
5803467 3467
SD431 AA AB AC AD AE AF
AG AH AJ AK AL AM

E5 SINGLE CARD
CORE
SD721

E6 SINGLE CARD
CORE
SD561

E7 SINGLE CARD
CORE
SD731

F1 CONNECTOR
A11 SD311AL4
B11 SD111BS4
C09 SD321AA4
C11 SD321AC4
D09 SD311AJ4
D11 SD311AL4
E09 SD311AE4
E11 SD311AG4

F2 SINGLE CARD
5803132 3132
SD311 A1 B1 C1 D1 E1 F1
SD321 G1 H1 J1 K1

F3 SINGLE CARD
5803467 3467
SD441 AA AB AC AD AE AF
AG AH AJ AK AL AM

F4 SINGLE CARD
CORE
SD751

F5 SINGLE CARD
CORE
SD731

F7 SINGLE CARD
CORE
SD731

G1 CONNECTOR
A09 SD311AA4
A11 SD311AC4
E09 SD331AQ4
E11 SD111BR4

G2 SINGLE CARD
5803491 3491
SD221 A1
SD121 B1
SD111 C1 C2

G3 SINGLE CARD
5803467 3467
SD431 AA AB AC AD AE AF
AG AH AJ AK AL AM

H1 CONNECTOR
A09 SD331AA4
A11 SD331AP4
B09 SD321AJ4
B11 SD321AL4
C09 SD321AE4
C11 SD321AG4
D09 SD331AF4
D11 SD111BR4
E11 SD111BQ4

H2 SINGLE CARD
5800525 0525
SD111 A1 A2 A3 B1 B2 B3
C1
SD331 D1 E1
SD321 F1 G1

H3 SINGLE CARD
5803467 3467
SD461 AA AB AC AD AE AF
AG AH AJ AK AL AM

H4 SINGLE CARD
CORE
SD761

H5 SINGLE CARD
CORE
SD781

H7 SINGLE CARD
CORE
SD761

J1 CONNECTOR
A11 SD311AL4
B11 SD111BS4
C09 SD321AA4
C11 SD321AC4
D09 SD311AJ4
D11 SD311AL4
E09 SD311AE4
E11 SD311AG4

J2 SINGLE CARD AUX
5803467 3467
SD551 AA AB AC AD AE AF
AG AH AJ AK AL AM

J3 SINGLE CARD
5803467 3467
SD511 AA AB AC AD AE AF
AG AH AJ AK AL AM

J5 SINGLE CARD
CORE
SD791

J6 SINGLE CARD
CORE
SD561

J7 SINGLE CARD
CORE
SD781

K1 CONNECTOR
A09 SD311AA4
A11 SD311AC4
E09 SD621AB4
E11 SD771AK4

K2 SINGLE CARD
5803466 3466
SD651 AA AB AC AD AE AF
AG AH AJ AK

K3 SINGLE CARD
5803467 3467
SD521 AA AB AC AD AE AF
AG AH AJ AK AL AM

K5 SINGLE CARD
CORE
SD561

K6 SINGLE CARD
CORE
SD561

K7 SINGLE CARD
CORE
SD791

L1 CONNECTOR
A09 SD621AB4
A11 SD761AJ4
B09 SD621AC4
B11 SD761AK4
C09 SD621AD4
C11 SD771AJ4
D09 SD621AE4
D11 SD771AK4
E09 SD621AF4
E11 SD761AJ4

L2 SINGLE CARD 8K
5803466 3466
SD661 AA AB AC AD AE AF
AG AH AJ AK

L3 SINGLE CARD
5803467 3467
SD531 AA AB AC AD AE AF
AG AH AJ AK AL AM

M1 CONNECTOR
A11 SD791AK4
B09 SD621AG4
B11 SD781AK4
C09 SD621AH4
C11 SD791AJ4
D09 SD621AJ4
D11 SD791AK4
E09 SD331AH4
E11 SD331AQ4

M2 SINGLE CARD
5803773 3773
SD121 AA AB AC AD AE AF
AG AH AJ AK AL AM
SD111 BA

M3 SINGLE CARD 8K
5803467 3467
SD541 AA AB AC AD AE AF
AG AH AJ AK AL AM

M4 SINGLE CARD
5803475 3475
SD791 A1 A2
SD761 A3 A4

M5 SINGLE CARD
5803475 3475
SD771 A1 A2
SD781 A3 A4

M6 SINGLE CARD
5803475 3475
SD771 A1 A2
SD761 A3 A4

M7 SINGLE CARD
5803475 3475
SD791 A1 A2
SD781 A3 A4

N1 CONNECTOR
A09 SD331AK4
A11 SD331AR4

N2
N3 DOUBLE CARD
5804683 4683
SD111 A1 A2 A3 A4 A5 A6
A7 A8 A9 AA AB AC
AD AE B1 B2 B3

N4 SINGLE CARD 8K
5803475 3475
SD791 A1 A2
SD761 A3 A4

N5 SINGLE CARD 8K
5803475 3475
SD771 A1 A2
SD781 A3 A4

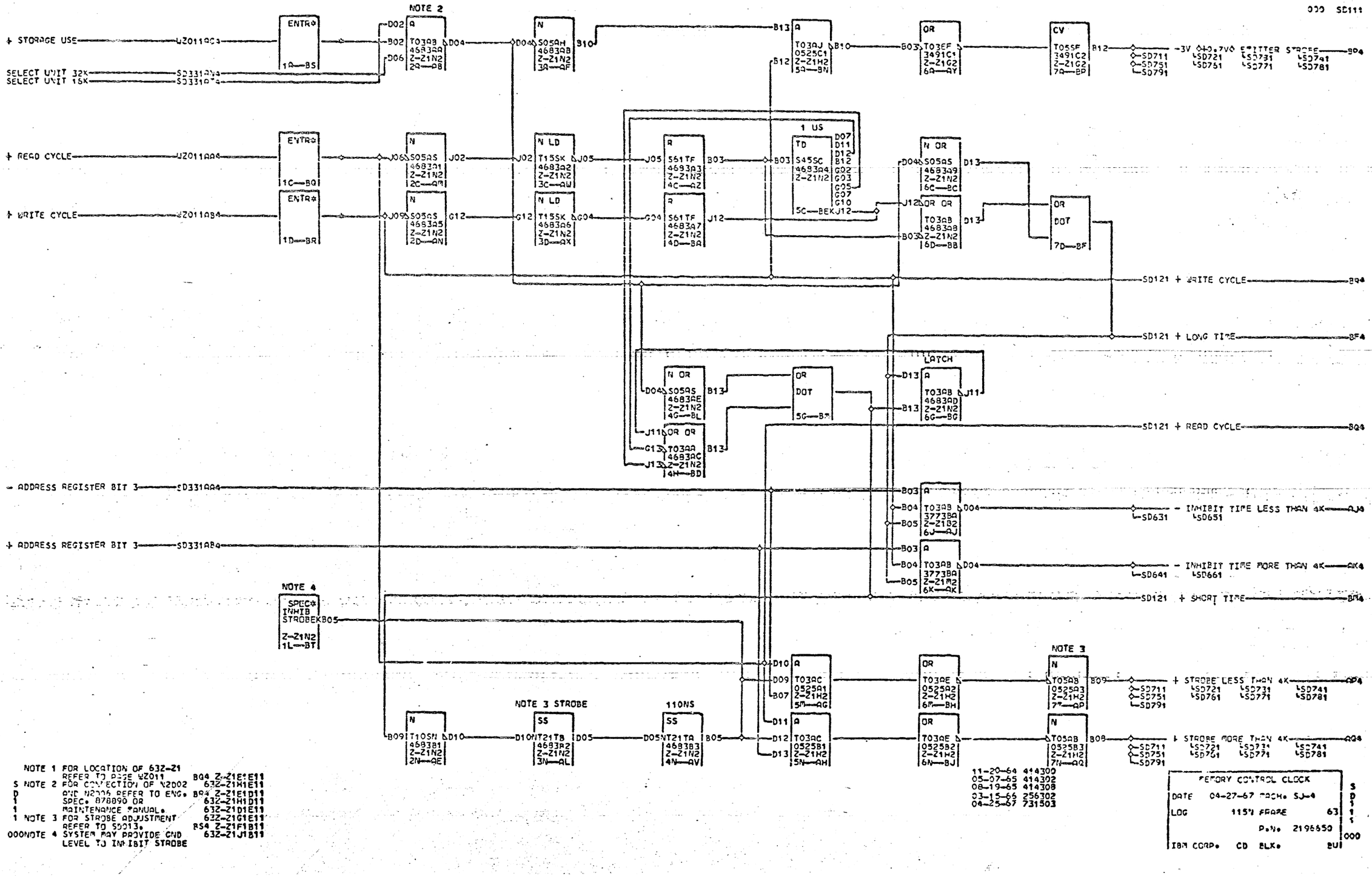
N6 SINGLE CARD 8K
5803475 3475
SD771 A1 A2
SD761 A3 A4

N7 SINGLE CARD 8K
5803475 3475
SD791 A1 A2
SD781 A3 A4

PLUG LIST

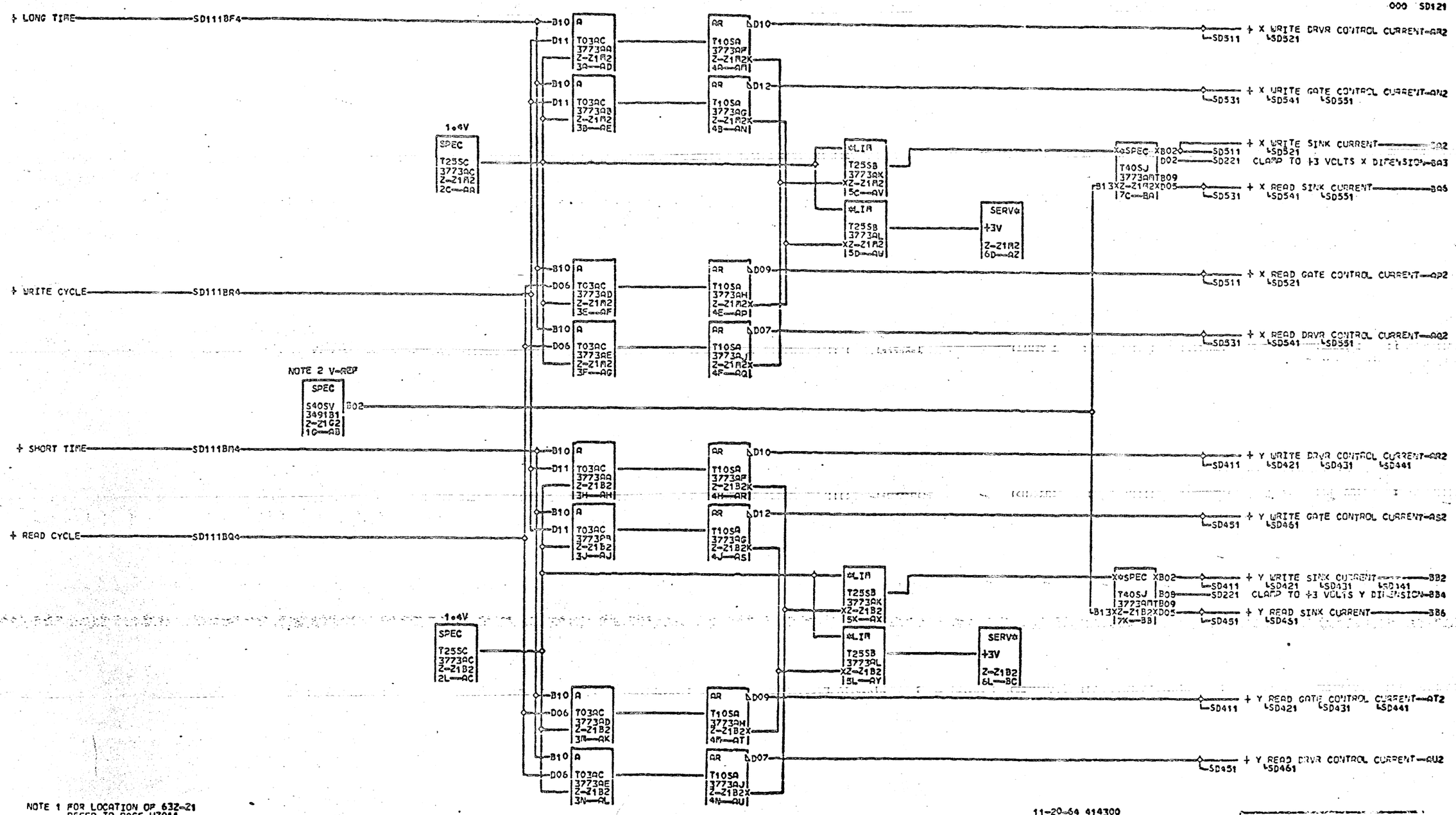
PART NO	ACC	TYPE	SOCKETS	TOTAL
5800525		0525	H2	01
5803132		3132	F2	01
5803466		3466	D2 K2	02
5803466	8K	3466	C2 L2	02
5803467		3467	C3 D3 E3 F3 G3 H3 J3 K3 L3	09
5803467	8K	3467	M3	01
5803467	AUX	3467	J2	01
5803475		3475	B3 B4 B5 B6 B7 M4 M5 M6 M7	09
5803475	8K	3475	A3 A4 A5 A6 A7 N4 N5 N6 N7	09
5803484		3484	A2	01
5803491		3491	G2	01
5803773		3773	B2 M2	02
5804683		4683	N2	01
		CONN	A1 B1 C1 D1 E1 F1 G1 H1 J1 K1 L1 M1 N1	13
		CORE	D5 D6 D7 E5 E6 E7 F4 F5 F7 H4 H5 H7 J5 J6 J7 K5 K6 K7	18

SOCKET LISTING
DATE 04-26-67 MACH. SJ-4
LOG 1169 BOARD 632-21
PREV. ENGR. 03-15-67 256302
PRES. ENGR. 04-25-67 731503
P.N. 2195695 SDD
IBM CORP. SDD BLK.



NOTE 1 FOR LOCATION OF 63Z-Z1 REFER TO PAGE WZ011
S NOTE 2 FOR CONNECTION OF N2D02 ONE N2D06 REFER TO ENG. SPEC. 878890 OR MAINTENANCE MANUAL.
1 NOTE 3 FOR STROBE ADJUSTMENT REFER TO SD013.
000NOTE 4 SYSTEM MAY PROVIDE GND LEVEL TO INHIBIT STROBE

BQ4	Z-Z1E1E11
	63Z-Z1H1E11
BR4	Z-Z1E1D11
	63Z-Z1H1D11
	63Z-Z1D1E11
	62Z-Z1G1E11
BS4	Z-Z1F1B11
	63Z-Z1J1B11



NOTE 1 FOR LOCATION OF 63Z-21
REFER TO PAGE WZ011
NOTE 2 FOR V-REF ADJUSTMENT
REFER TO SD013.

S D 2 1 000

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

X Y CURRENT CONTROL

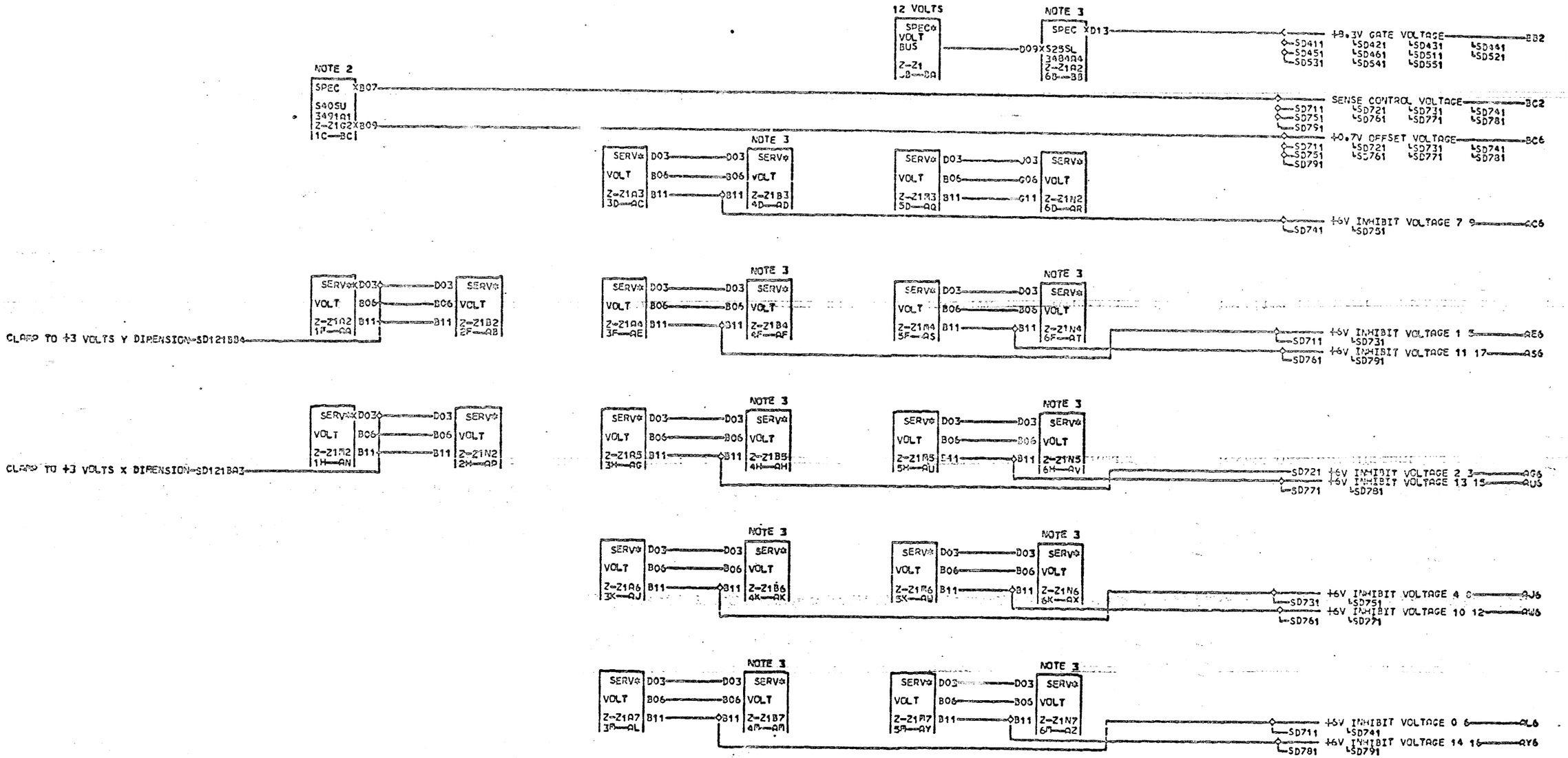
DATE 04-27-67 PROG. SJ-4

LOG 115N PAGE 63

P.N. 2195651

IBM CORP. CD BLK.

S D 2 1 000



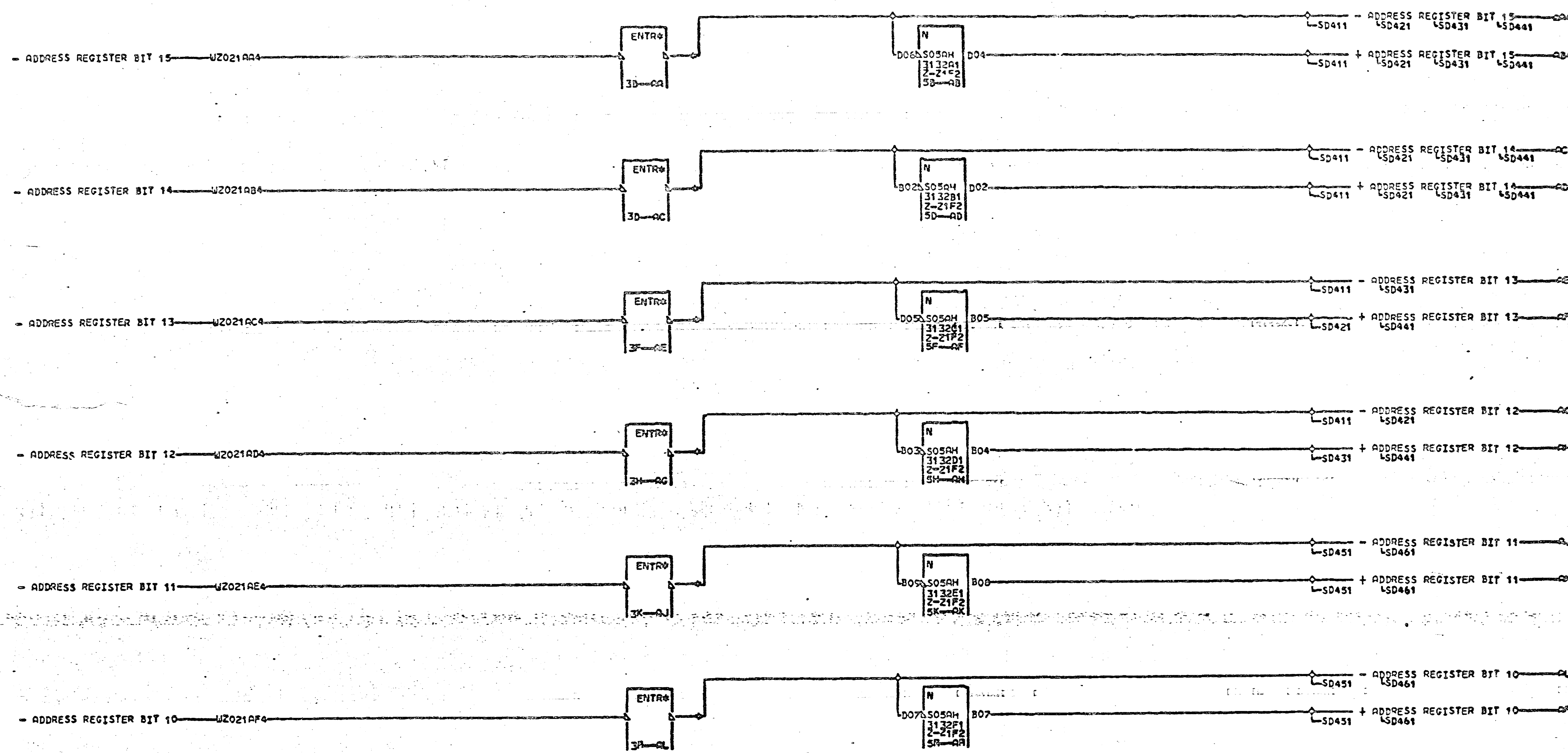
NOTE 1 FOR LOCATION OF 63Z-Z1 REFER TO PAGE UZ011

NOTE 2 FOR SENSE CONTROL VOLTAGE ADJUSTMENT REFER TO SD013

NOTE 3 DISTRIBUTION MAY BE BY MINI-BUS OR BY PRINTED OR YELLOW WIRE ON THE BOARD.

11-20-64 414300
05-07-65 414302
03-15-66 256302
04-15-67 731503

LOGIC VOLTAGE DISTRIBUTION				SD221 000
DATE 04-27-67	MACH. SJ-4			
LOG 117W	FRAME	63		
	P.N. 2196633			
IBM CORP. CD	BLK.	BD		



NOTE 1 FOR LOCATION OF 63Z-Z1
REFER TO PAGE WZ011

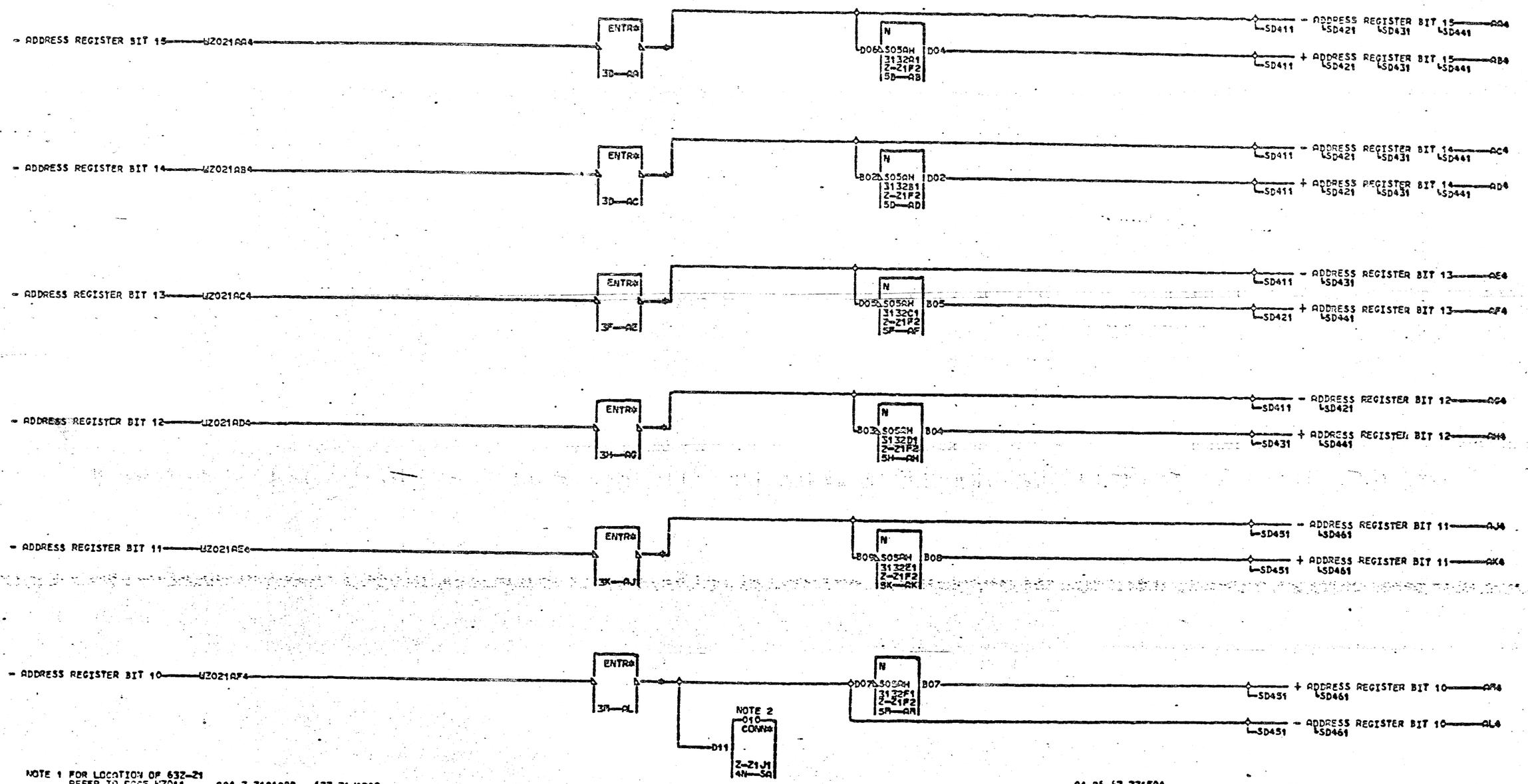
S
D
3
1
1
000

AA4 Z-Z1G1A09
63Z-Z1K1A09
AC4 Z-Z1G1A11
63Z-Z1K1A11
AE4 Z-Z1F1E09
63Z-Z1J1E09
AG4 Z-Z1F1E11
63Z-Z1J1E11
AJ4 Z-Z1F1D09
63Z-Z1J1D09
AL4 Z-Z1F1D11
63Z-Z1J1D11
63Z-Z1F1A11
63Z-Z1J1A11

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256702
04-25-67 731503

MAR INVERTERS 1 OF 3		
DATE	04-27-67	MACH. SJ-4
LOG	115N	FRAME 63
		P.N. 2196654
IBM CORP.	CD	BLK. AP

S
D
3
1
1
000



NOTE 1 FOR LOCATION OF 63Z-Z1 REFER TO PAGE UZ011

NOTE 2 SYSTEM MAY REMOVE M3D09 TO J1D11 REFER TO UZ021

AA4 Z-Z1D1A09	63Z-Z1K1A07	63Z-Z1J1D09
AC4 Z-Z1C1A11	AL4 Z-Z1F1D11	63Z-Z1J1D11
RE4 Z-Z1F1E09	63Z-Z1K1A11	63Z-Z1F1A11
AG4 Z-Z1F1E11	63Z-Z1J1E09	63Z-Z1J1A11
AJ4 Z-Z1F1D09	63Z-Z1J1E11	

010
SIM TO PN 2196654 EC 731503

04-26-67 731504

FOR INVERTERS 1 OF 3

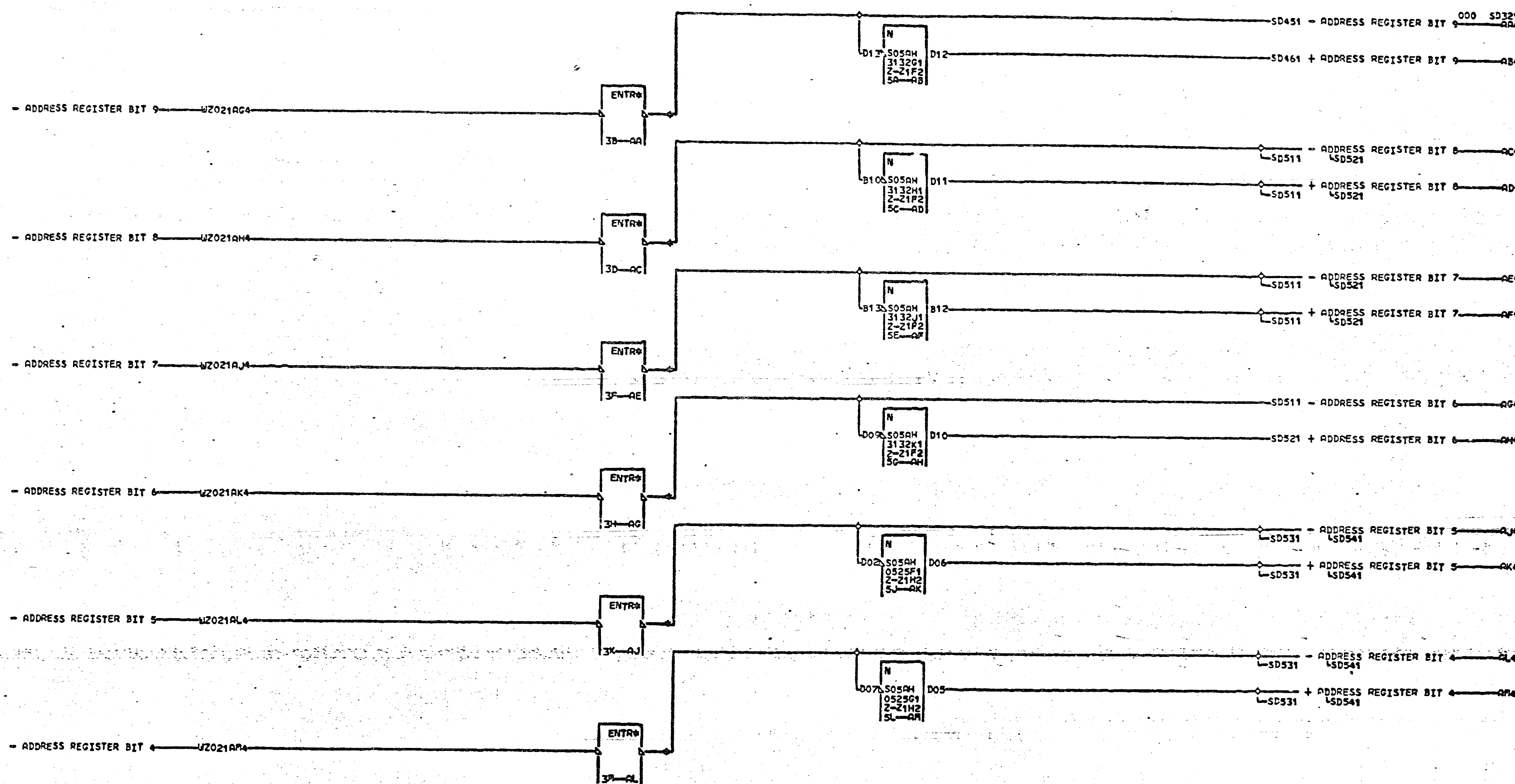
DATE 04-26-67 PROG. SJ-4

LOG 117J FRAME 63

PeNo 2510216

IBM CORP. CD BLK. SB

010



NOTE 1 FOR LOCATION OF 632-Z1
REFER TO PAGE WZ011

S
D
3
2
1

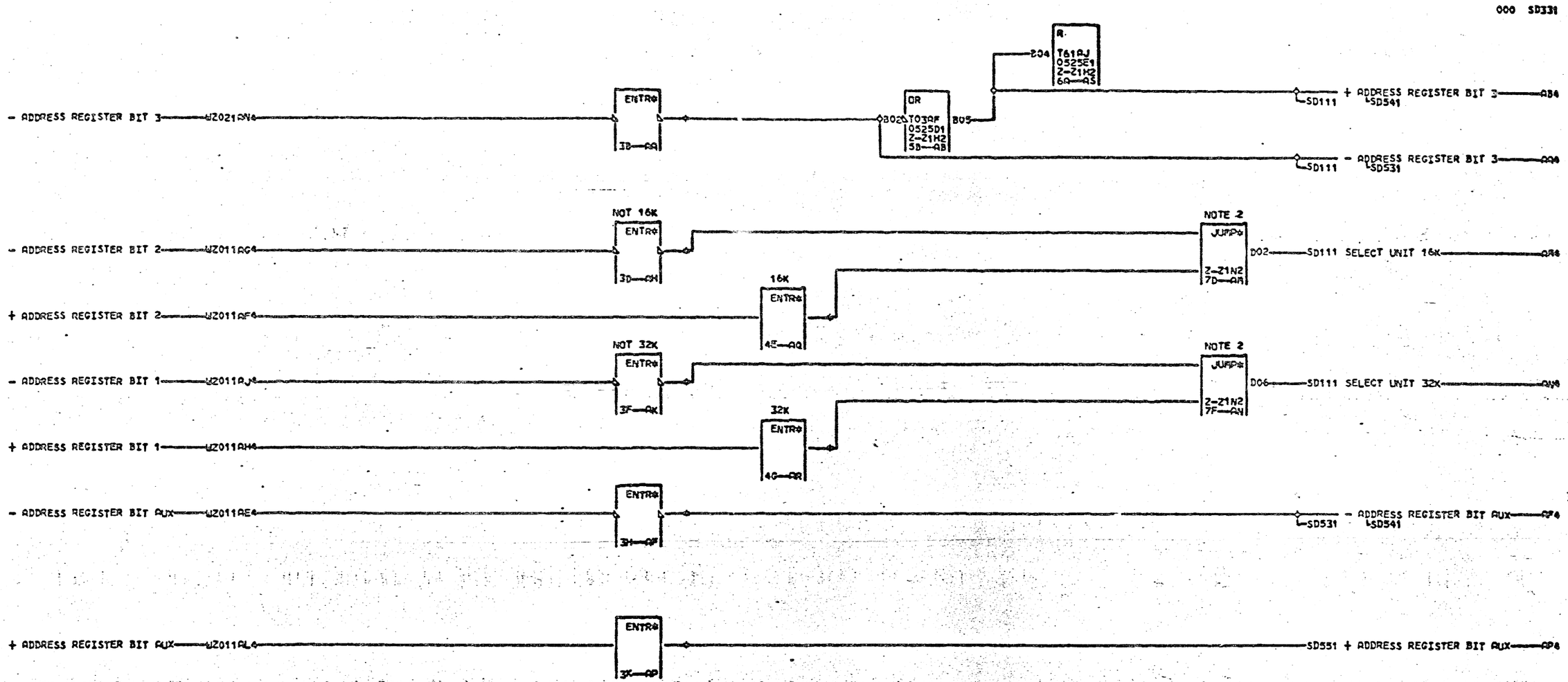
000

AA4 Z-Z1F1C09 632-Z1H1B09
632-Z1J1C09 AL4 Z-Z1E1B11
AC4 Z-Z1F1C11 632-Z1H1B11
632-Z1J1C11
AE4 Z-Z1E1C09
632-Z1H1C09
AG4 Z-Z1E1C11
632-Z1H1C11
AJ4 Z-Z1E1B09

11-20-64 414300
05-07-65 414302
03-15-66 256302
04-25-67 731503

MAR INVERTERS 2 OF 3		
DATE	04-27-67	MACH. SJ-4
LOG	115N	FRAME 63
		P.N. 2196655
IBM CORP.	CD	BLK. AN

S
D
3
2
1
000



NOTE 1 FOR LOCATION OF 632-Z1 REFER TO PAGE WZ011

S NOTE 2 FOR CONNECTIONS REFER TO PAGE WZ011.

AA4 Z-Z1E1A09 632-Z1M1A11
632-Z1M1A09 AQ4 Z-Z1M1E11
632-Z1D1E09 AR4 Z-Z1M1A11
632-Z1G1E09
AF4 Z-Z1E1D09
632-Z1H1D09
AH4 Z-Z1M1E09
AK4 Z-Z1M1A09
AP4 Z-Z1E1A11

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

MAR INVERTERS 3 OF 3

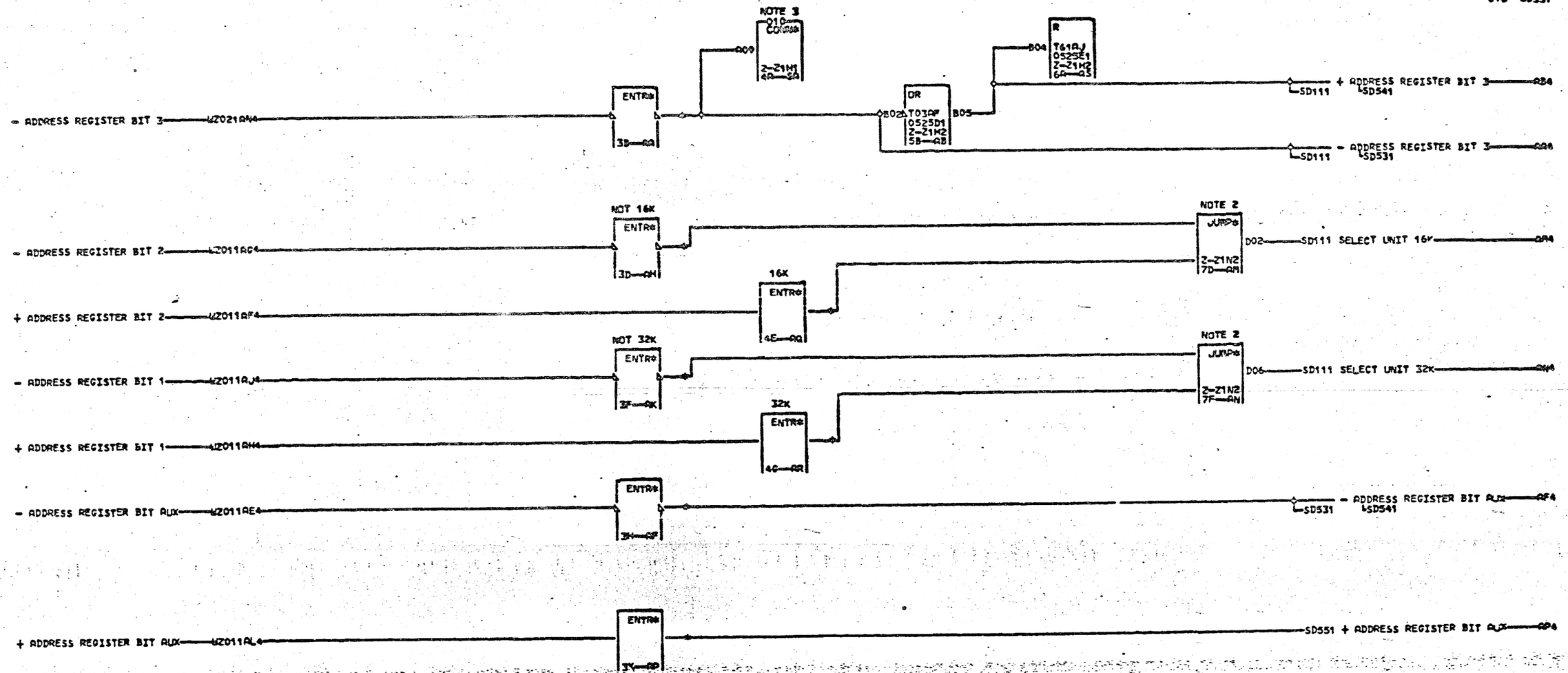
DATE 04-27-67 PROM. SJ-4

LOG 115N FRAME 63

P.N. 2196656

IBM CORP. CD BLK. AT

000



NOTE 1 FOR LOCATION OF 632-Z1 REFER TO PAGE WZ011
NOTE 2 FOR CONNECTIONS REFER TO PAGE WZ011.
NOTE 3 SYSTEM MAY REMOVE M2502 TO M1A09 REFER TO WZ021

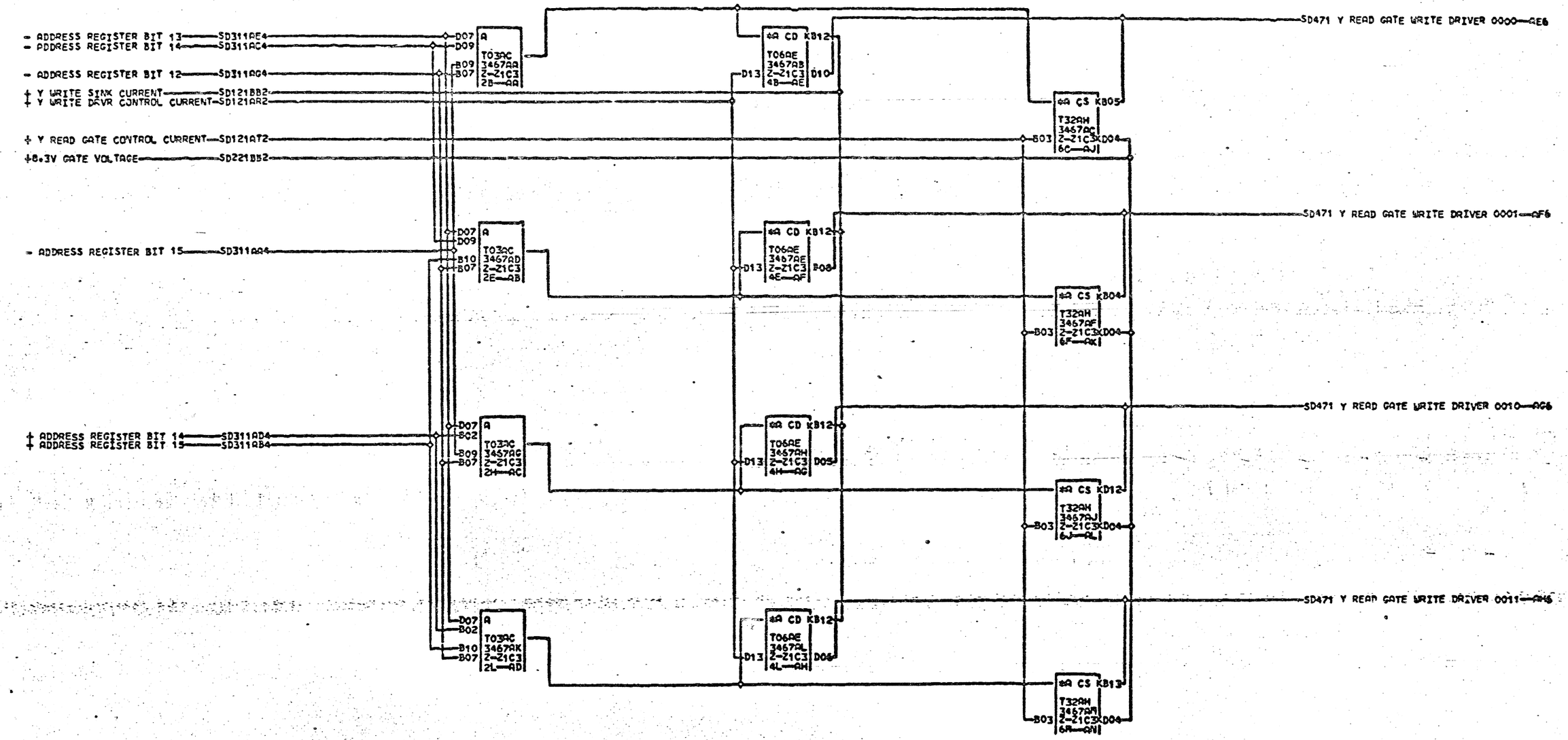
AA4	Z-Z1E1A09	632-Z1M1A11	
	632-Z1M1A09	AQ4	Z-Z1R1E11
	632-Z1D1E09	AR4	Z-Z1N1A11
	632-Z1G1E09		
AF4	Z-Z1E1D09		
	632-Z1M1D09		
AH4	Z-Z1M1E09		
AK4	Z-Z1N1A09		
AP4	Z-Z1E1A11		

SIR TO PN 2196656 EC 731503

04-26-67 731504

FOR INVERTERS 3 OF 3
DATE 04-26-67 TECH. SJ-4
LOG 117J FRAME 63
P.N. 2310217
IBM CORP. CD BLK. SB

SD131 010

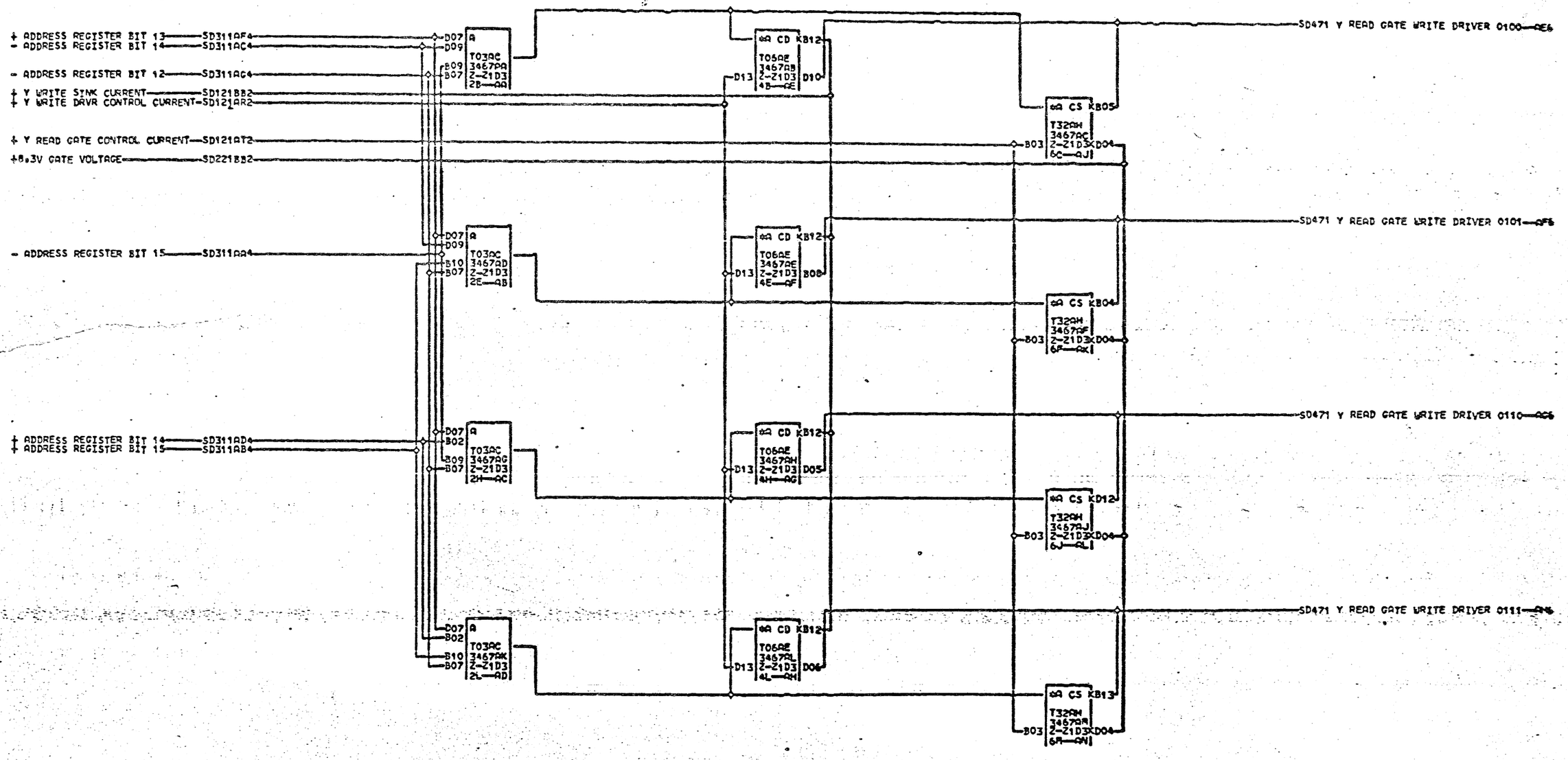


NOTE 1 FOR LOCATION OF 632-21
REFER TO PAGE W2011
$ NOTE 2 Y LOW 0000 TO 0011

11-20-64 414300
05-07-65 414302
08-16-65 414308
03-15-66 256302
04-25-67 731503

Y READ GATE WRITE DRIVER
LOW ORDER 1 OF 4
DATE 04-27-67 MACH. SJ-4
LOG 115N FRAME $3
P.N. 2196657
IBM CORP. CD BLK. MP

$ SD411 000

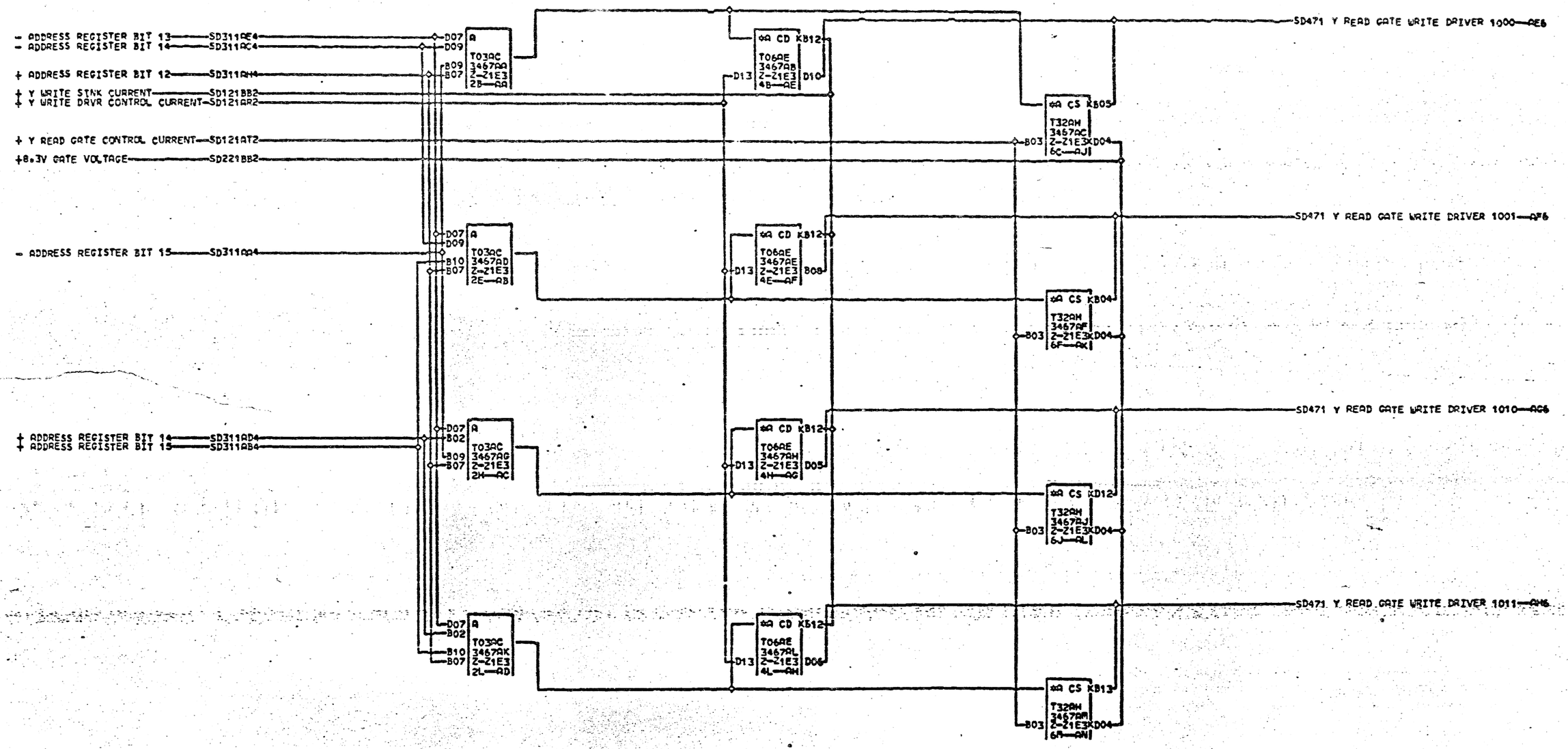


NOTE 1 FOR LOCATION OF 632-29
REFER TO PAGE WZ011
NOTE 2 Y LOW 0100 TO 0111

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

Y READ GATE WRITE DRIVER
LOW ORDER 2 OF 4
DATE 04-27-67 MACH. SJ-8
LOG 115N FRAME 63
P.N. 2196658
IBM CORP. CD BLK. AD

SD421 000

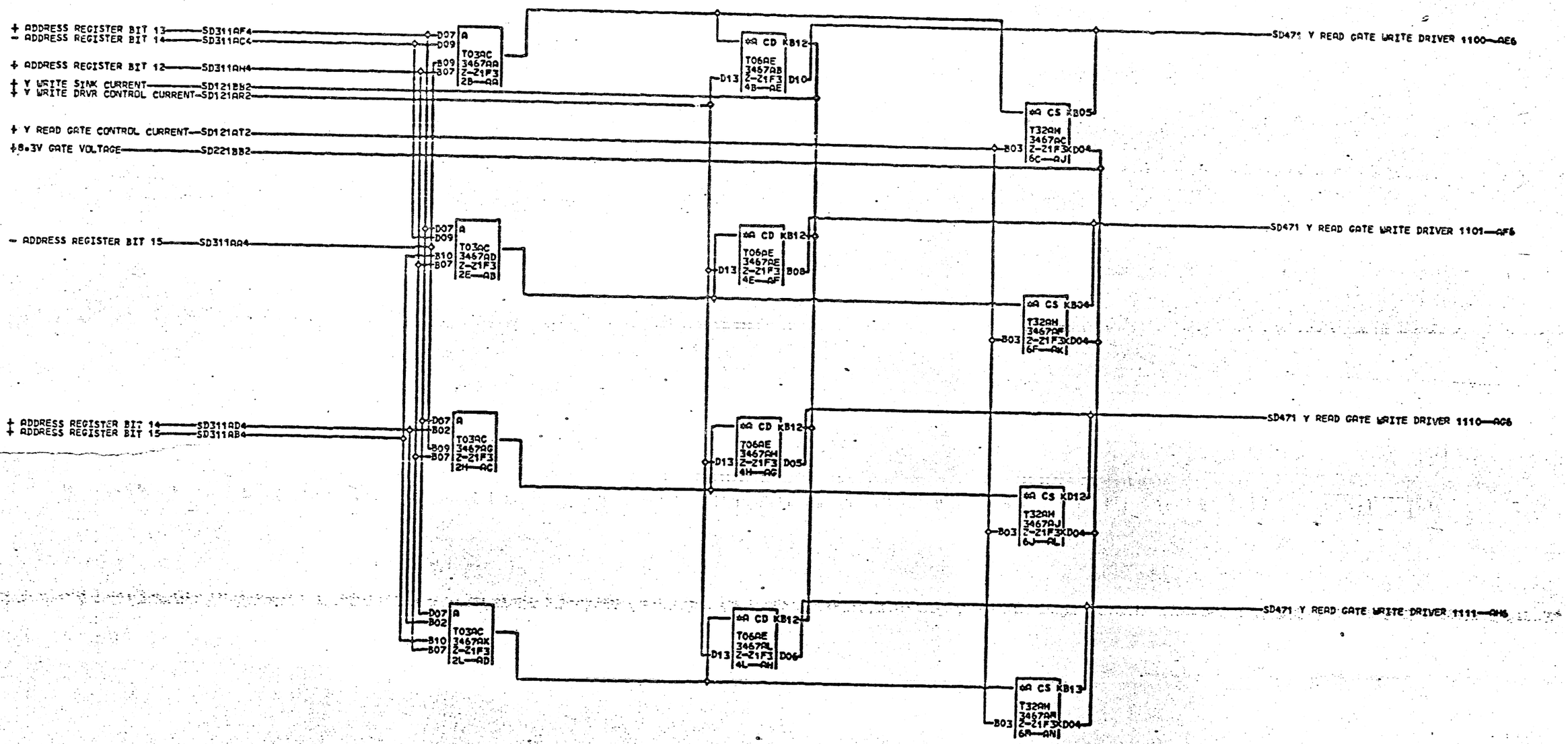


NOTE 1 FOR LOCATION OF 532-21
REFER TO PAGE W2011
NOTE 2 Y LOW 1000 TO 1011

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

Y READ GATE WRITE DRIVER
LOW ORDER 3 OF 4
DATE 04-27-67 PACH. SJ-6
LOG 115N FRAME 63
P.N. 2196659
IBM CORP. CD BLK. AP

SD431 1 000

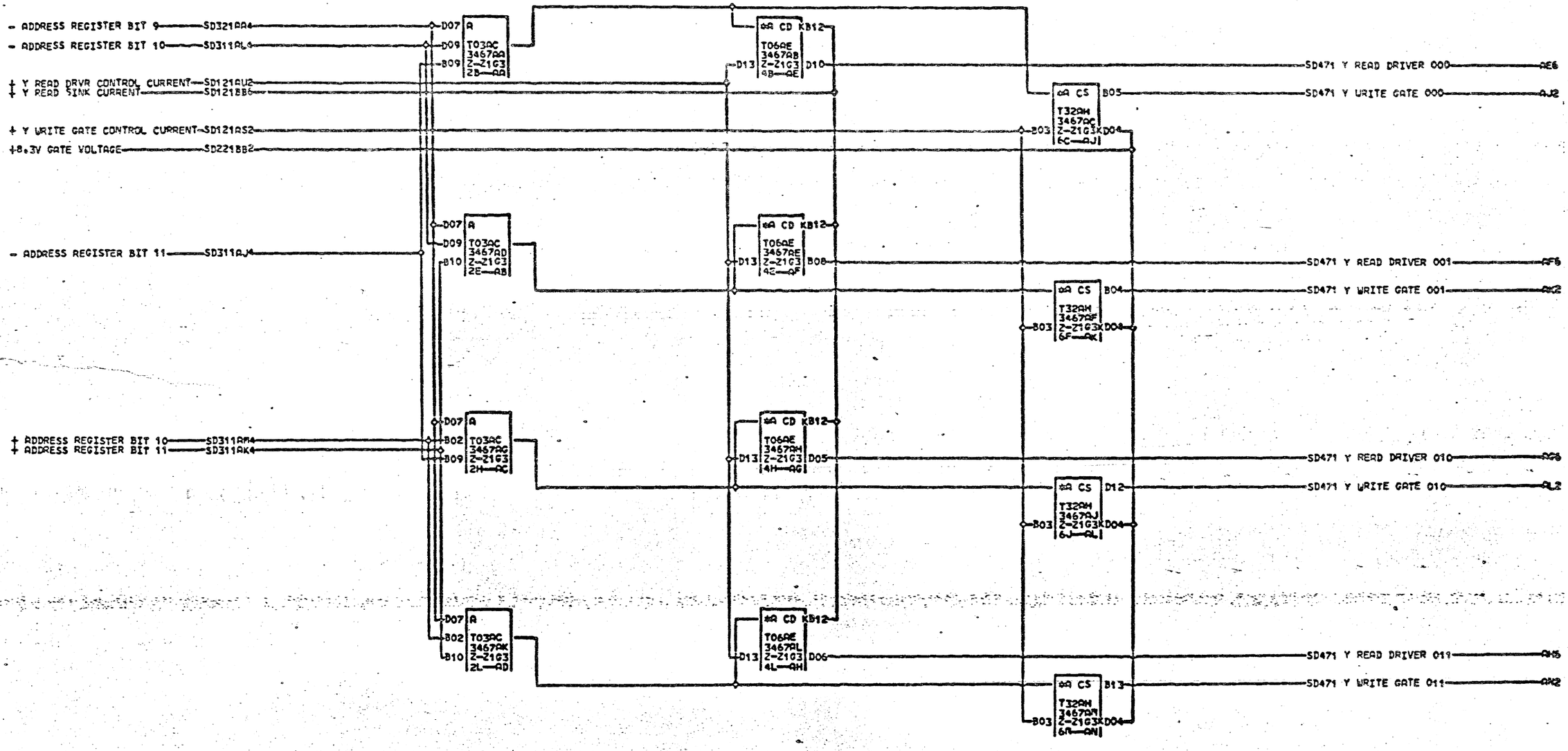


NOTE 1 FOR LOCATION OF 632-21 REFER TO PAGE W2011
NOTE 2 Y LOW 1100 TO 1111

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

Y READ GATE WRITE DRIVER
LOW ORDER 4 OF 4
DATE 04-27-67 PACH. SJ-6
LOG 115N FRAME 63
PeNo 2196660
IBM CORP. CD BLK. AP

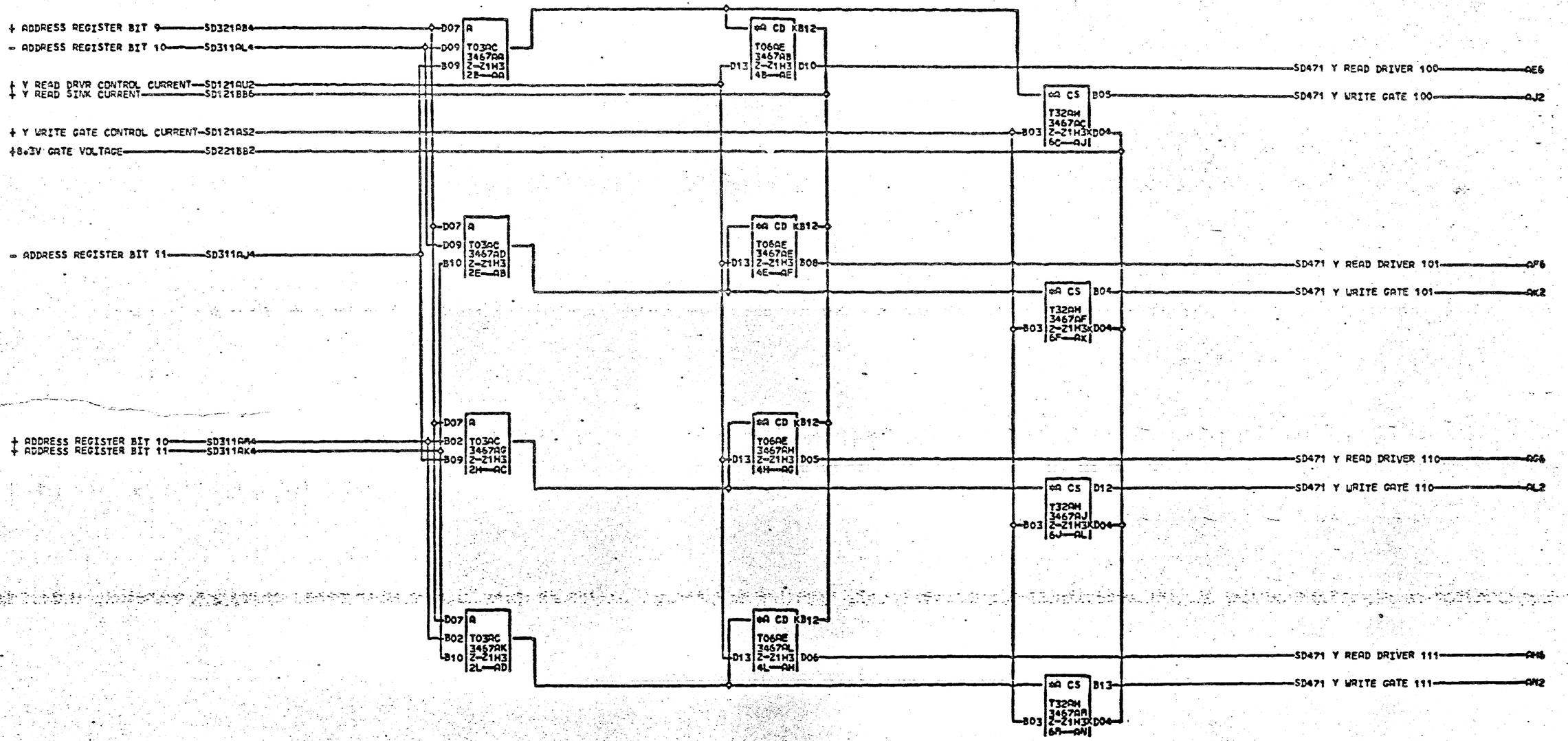
S 8 4 4 1 000



NOTE 1 FOR LOCATION OF 632-21
REFER TO PAGE WZ011
NOTE 2 Y MI 000 TO 011

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

Y WRITE GATE AND READ DRIVER
HIGH ORDER 1 OF 2
DATE 04-27-67 MACH. SJ-6
LOG 115N FRAME 63
P.N. 2196661
IBM CORP. CD BLK. AP



NOTE 1 FOR LOCATION OF 632-21 REFER TO PAGE WZ011

$ NOTE 2 Y MI 100 TO 111

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

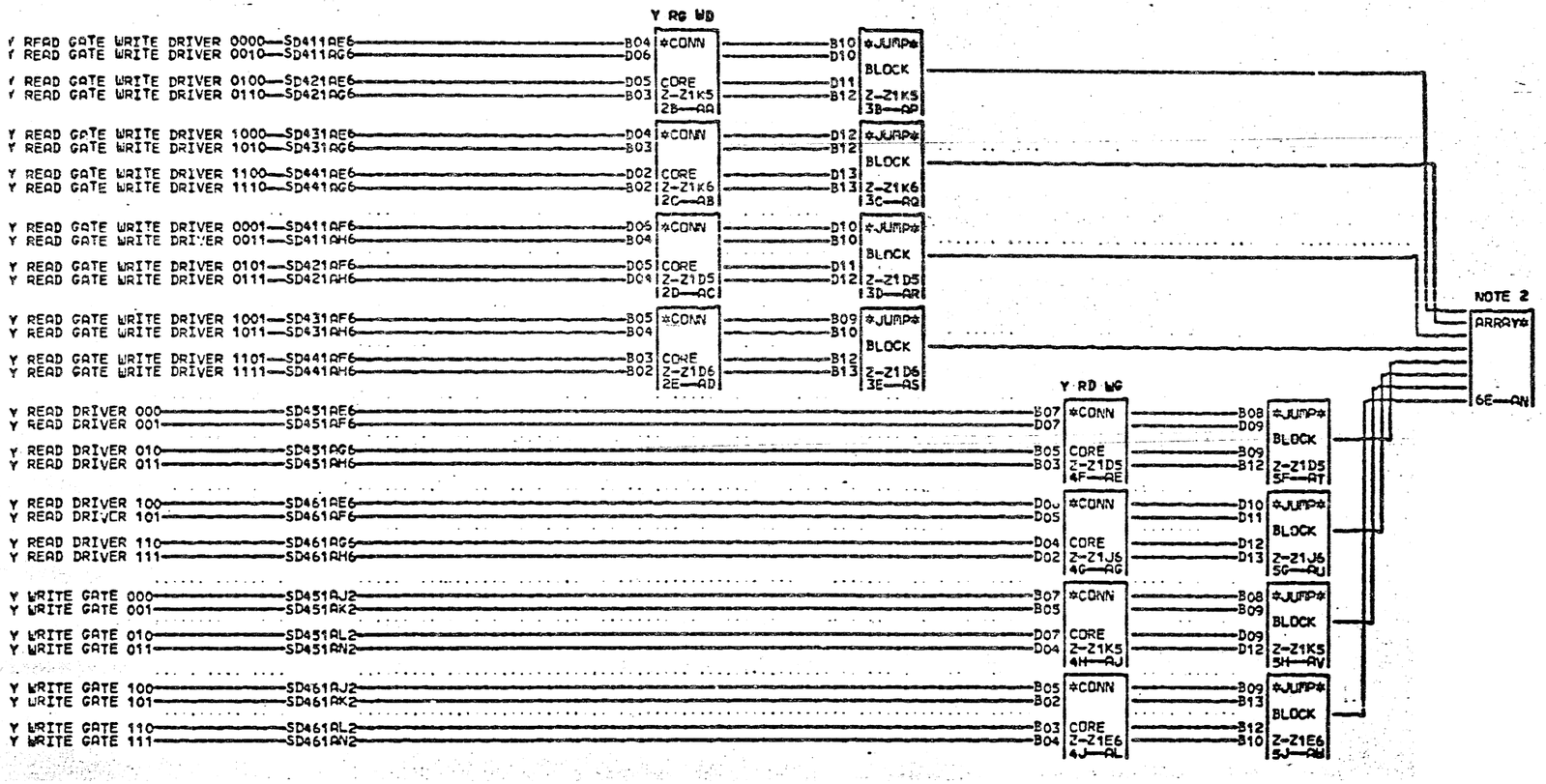
Y WRITE GATE AND READ DRIVER HIGH ORDER 2 OF 2

DATE 04-27-67 MACH. SJ-4

LOG 115N FRAME 63

P.N. 2196662

IBM CORP. CD BLK. AP



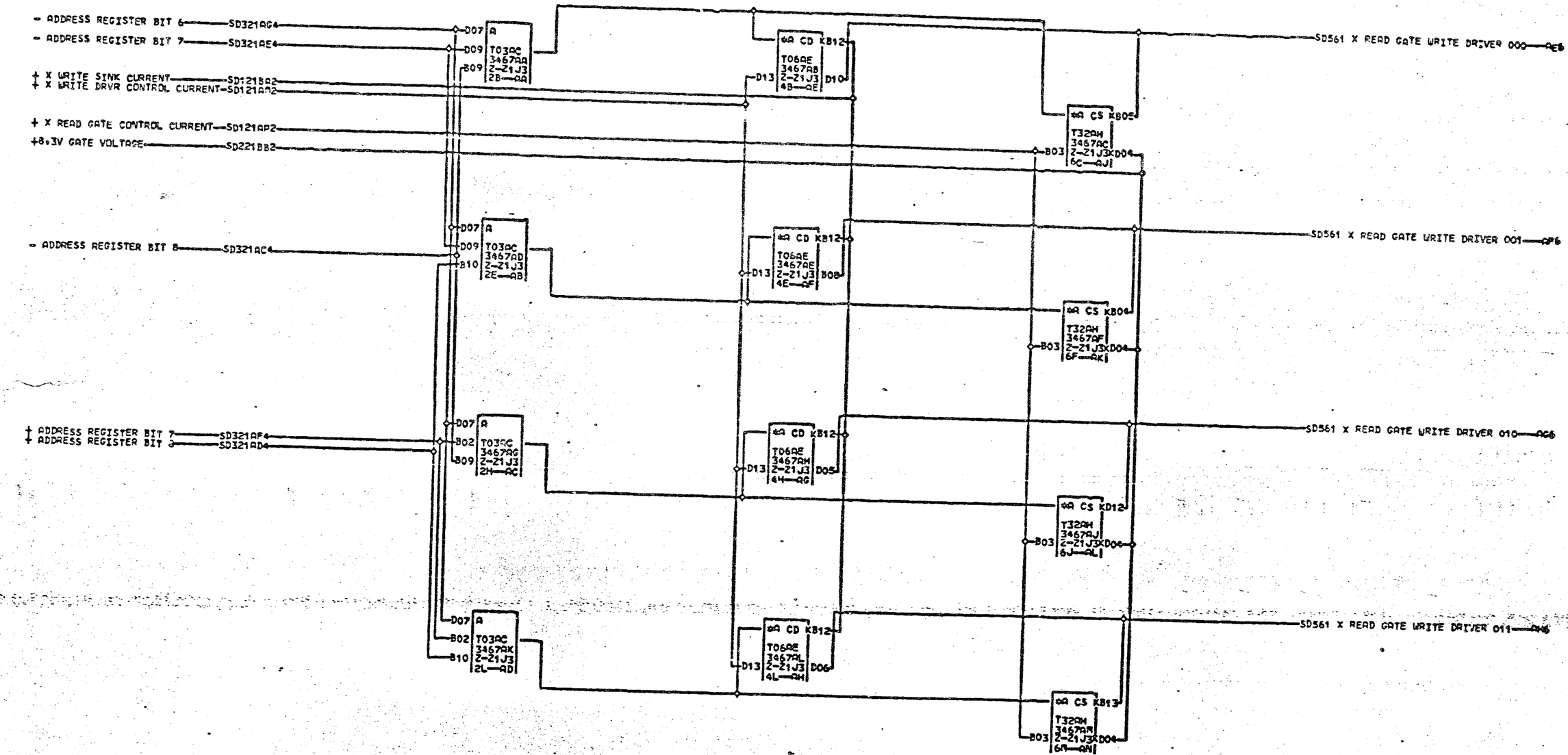
NOTE 1 FOR LOCATION OF 632-21
REFER TO PAGE W2011
S NOTE 2 REFER TO SD0710 SD0720
D SD0810 AND SD082 FOR
4 CONNECTIONS TO ARRAY
7 BOTTOM AND DIODE BOARDS
9

000

11-20-64 414300
05-07-65 414302
08-19-65 414308

X Y DRIVE ARRAY CONNECTOR
Y DIMENSION
DATE 07-12-66 MACH. SJ-4
LOG 277F FRAME 63
P.N. 2196668
IBM CORP. CD BLK. AX

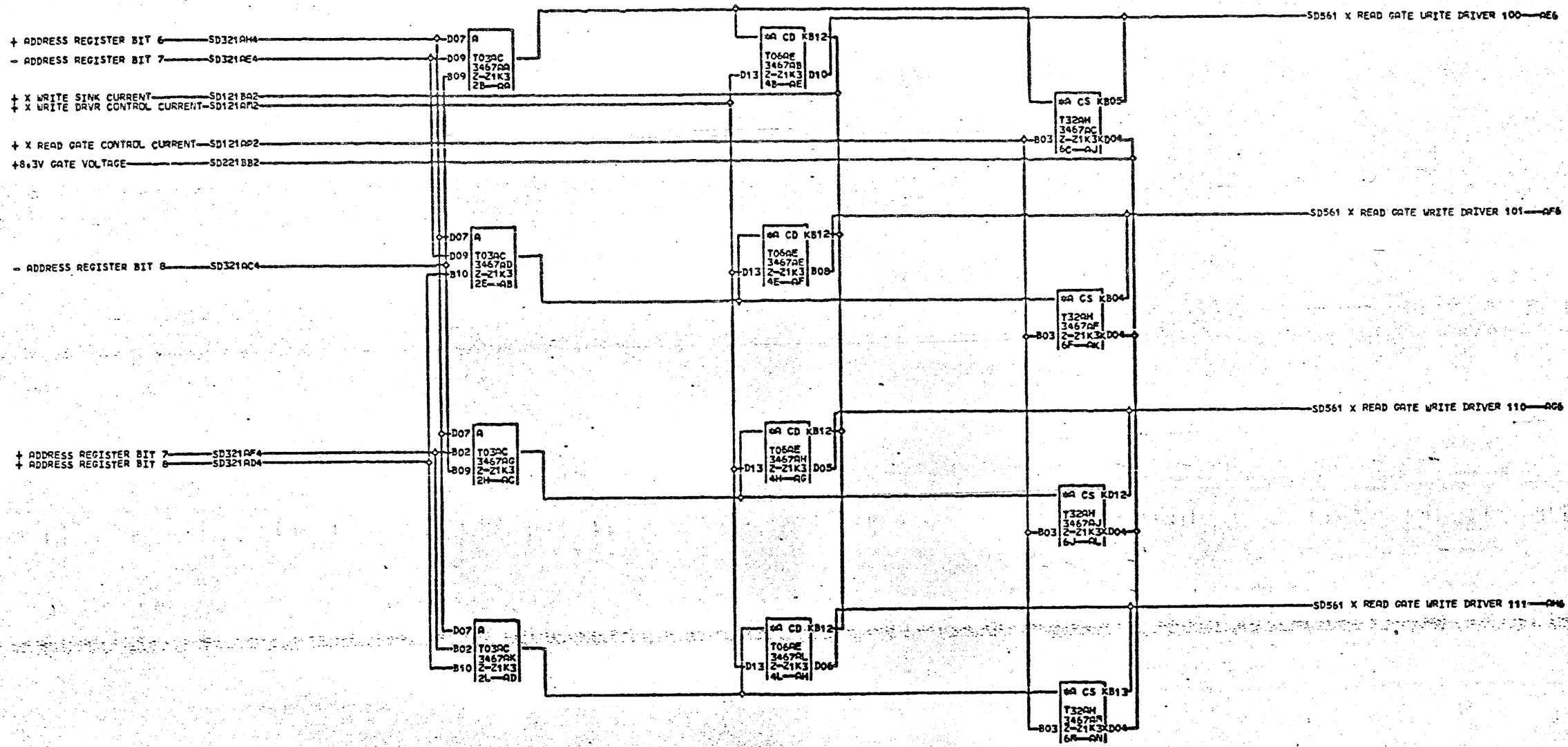
SD471 9 000



NOTE 1 FOR LOCATION OF 632-21
REFER TO PAGE W2011
NOTE 2 X LOW 000 011

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

X READ GATE WRITE DRIVER
LOW ORDER 1 OF 2
DATE 04-27-67 PACH. SJ-4
LOG 115N FRAME 63
P.No. 2196663
IBM CORP. CD BLK. AP
SD311 000

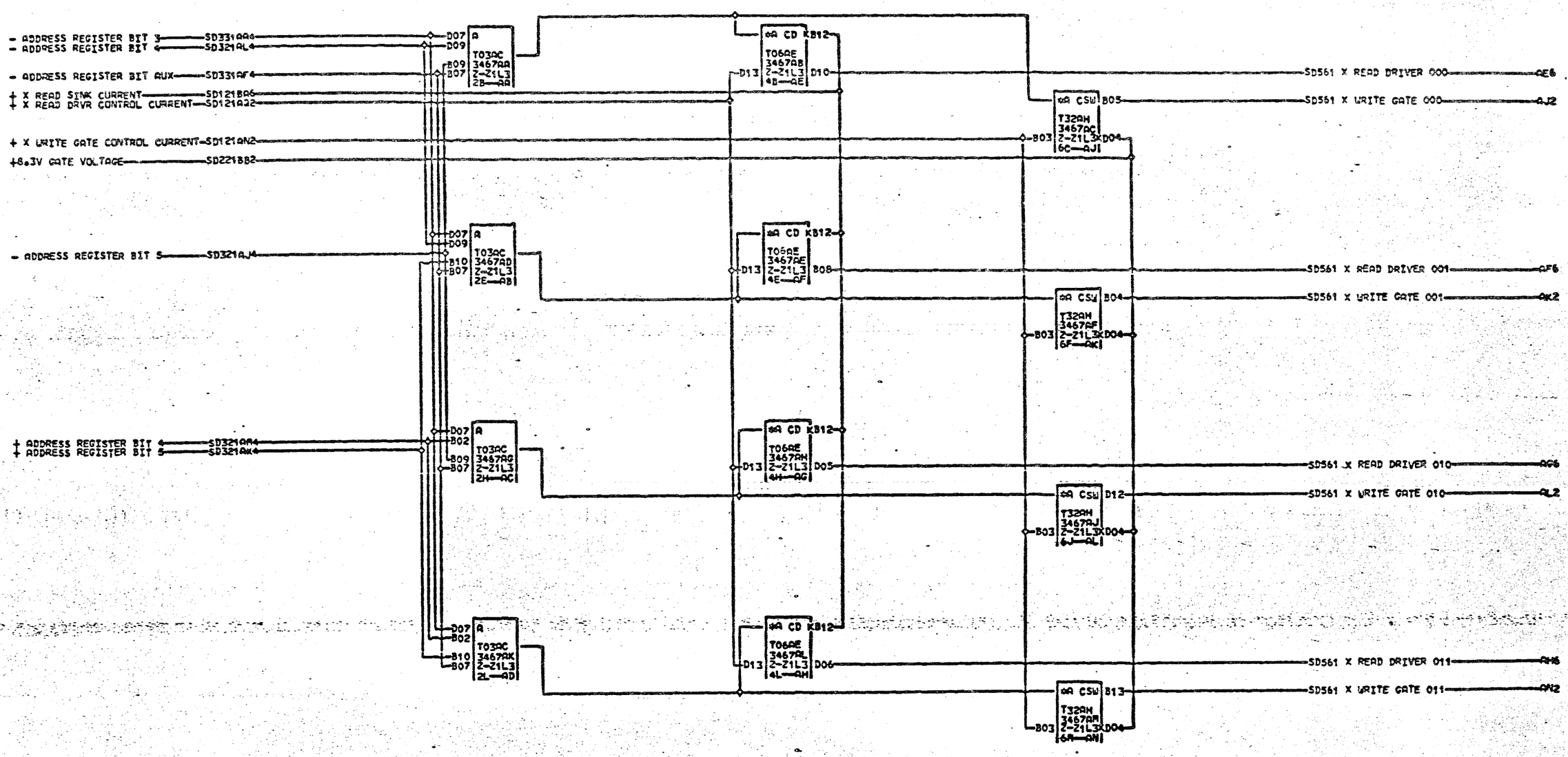


NOTE 1 FOR LOCATION GF 632-Z1
REFER TO PAGE WZ011
NOTE 2 X LOW 100 TO 111

1-20-64 414300
03-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731303

X READ GATE WRITE DRIVER
LOW ORDER 2 OF 2
DATE 04-27-67 RACH. SJ-6
LOG 115N FRAME 63
P.No. 2196564
IBM CORP. CD BLK. AP

SD521 1 2 000

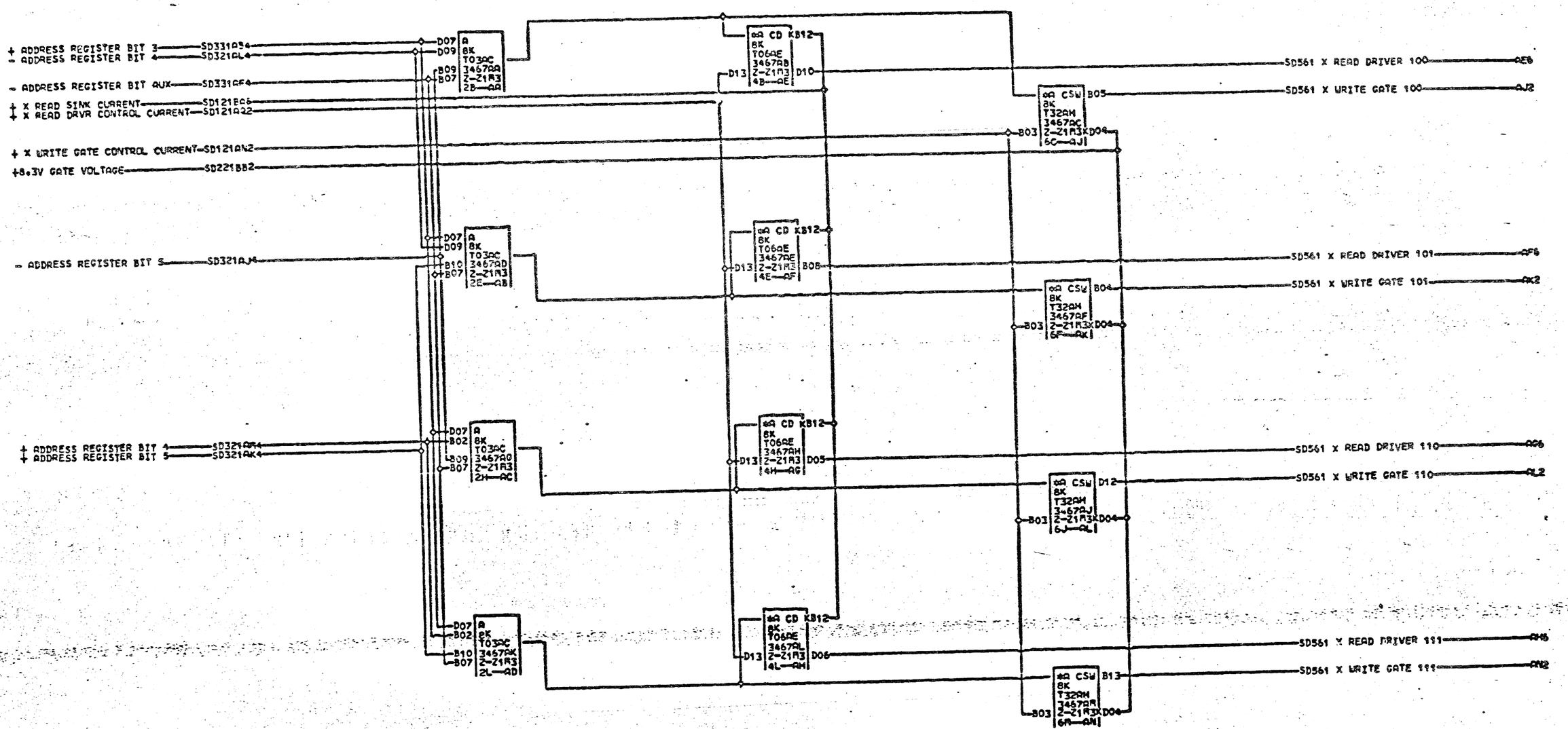


NOTE 1 FOR LOCATION OF 632-21 REFER TO PAGE WZ011
NOTE 2 X HI 000 TO 019

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

X WRITE GATE AND READ DRIVER HIGH ORDER 1 OF 2
DATE 04-27-67 PACH. SJ-4
LOC 115N FRAME 63
P.N. 2196665
IBM CORP. CD BLK.

SD531 000



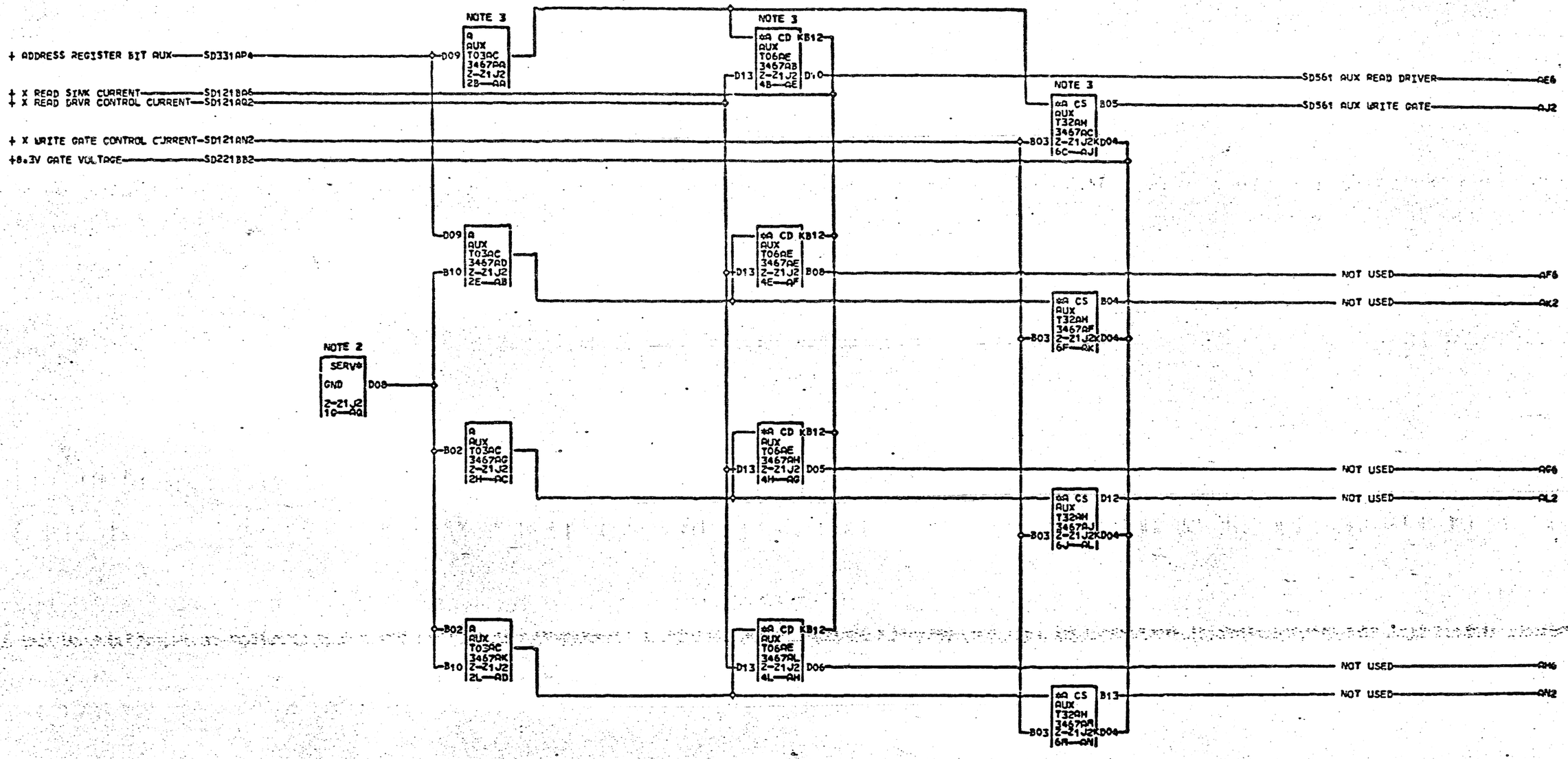
NOTE 1 FOR LOCATION OF 632-21 REFER TO PAGE WZ011
S NOTE 2 X HI 100 TO 111

000

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

X WRITE GATE AND READ DRIVER
HIGH ORDER 2 OF 2
DATE 04-27-67 PROM: SJ-4
LOG 115N FRAME 63
P.No. 2196666
IBM CORP. CD BLK. AP

S 000



NOTE 1 FOR LOCATION 632-21
REFER TO PAGE W2019
S NOTE 2 UNUSED CIRCUIT TIE DOWN
D NOTE 3 THIS CARD PRESENT FOR
S AUX STORAGE ONLY
S NOTE 4 AUX IS X HI ORDER
1

000

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

X AUX WRITE GATE READ DRIVER

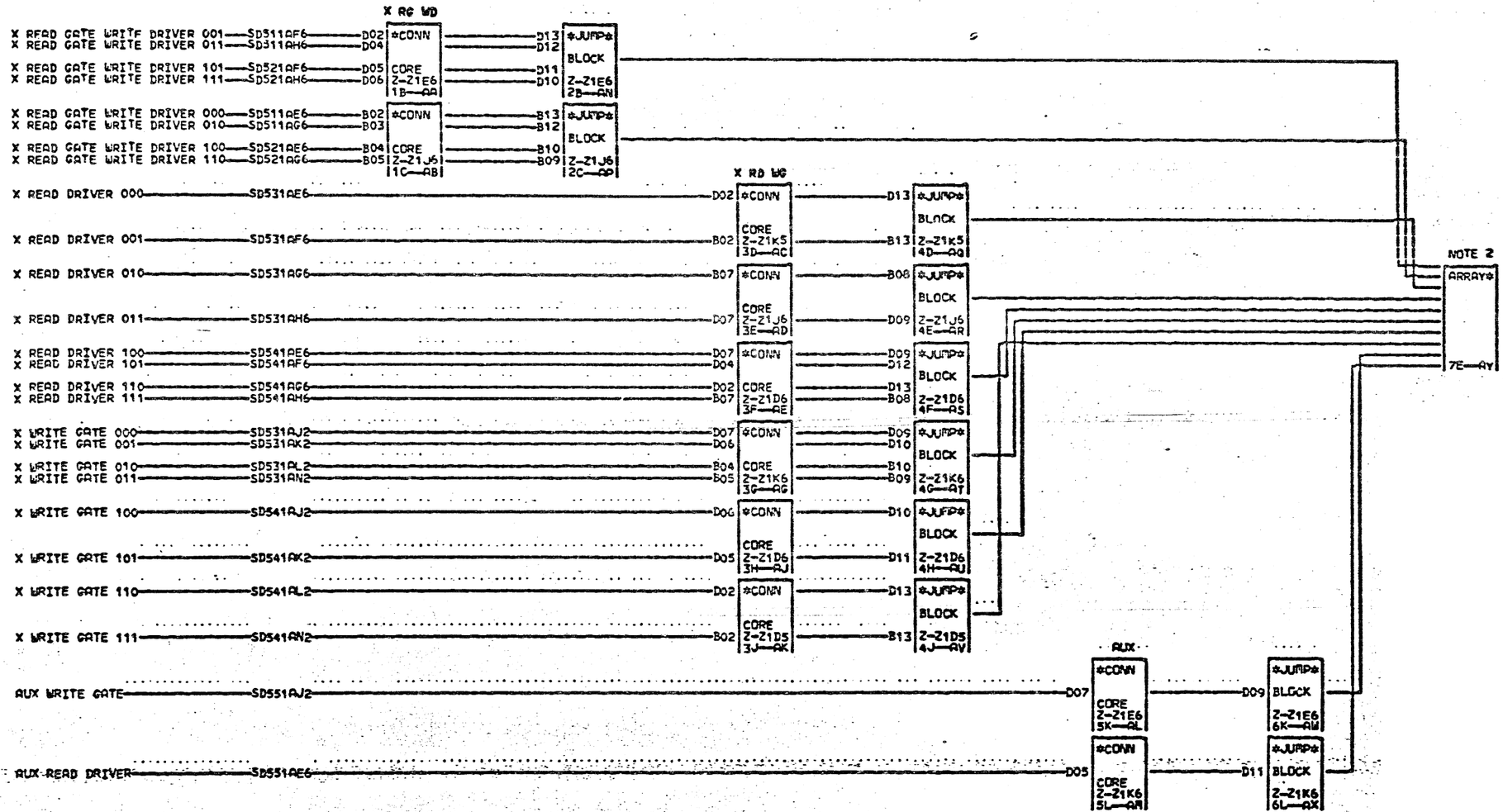
DATE 04-27-67 RACM* SJ-4

LOG 115N FRAME 63

P.N* 2196667

IBM CORP* CD BLK* AR

S S S S 1 000



NOTE 1 FOR LOCATION OF 632-21
REFER TO PAGE 62011

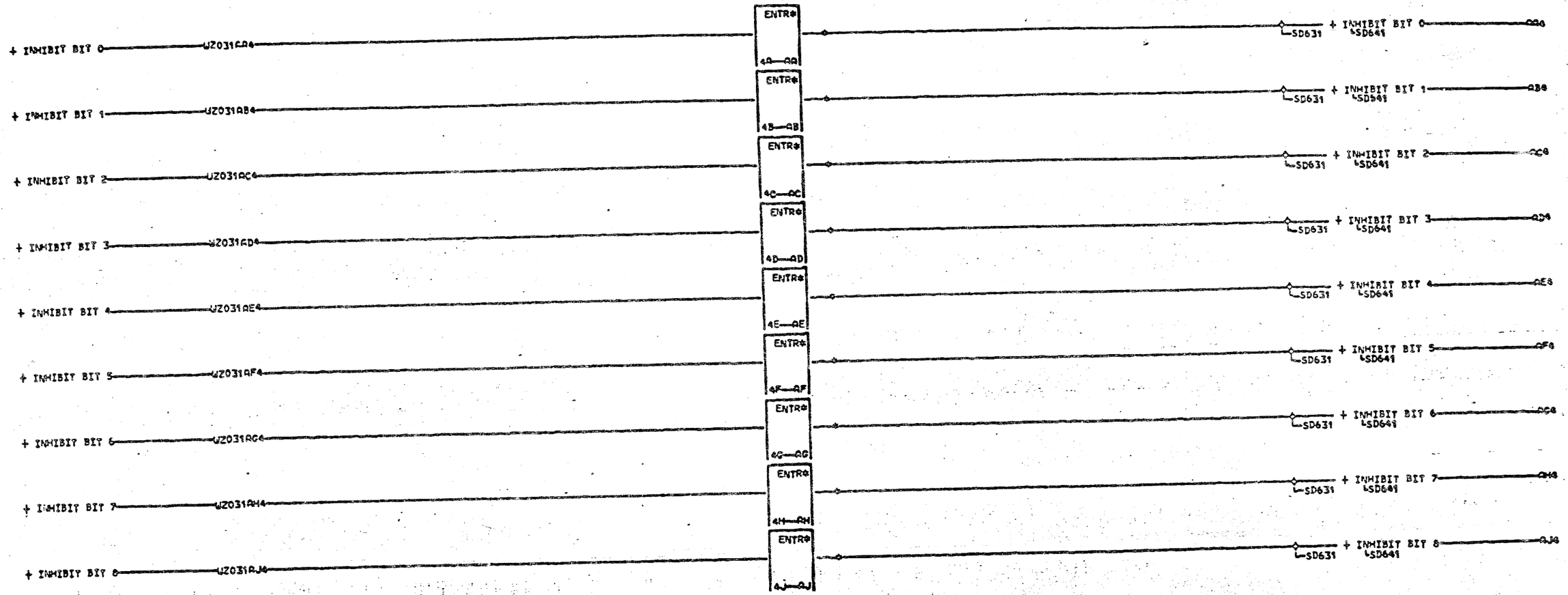
$ NOTE 2 REFER TO SD0710 SD0720
D SD0810 AND SD082 FOR
5 CONNECTIONS TO ARRAY
6 BOTTOM AND DIODE BOARDS
1

000

11-20-64 414300
05-07-65 414302
08-19-65 414308

X Y DRIVE ARRAY CONNECTOR
X DIMENSION
DATE 07-12-66 EACH. SJ-4
LOC 277F FRAME 63
P.No. 2196669
IBM CORP. CD BLK. AZ

SD561 1 000



NOTE 1 FOR LOCATION OF 632-Z1 REFER TO PAGE WZ011

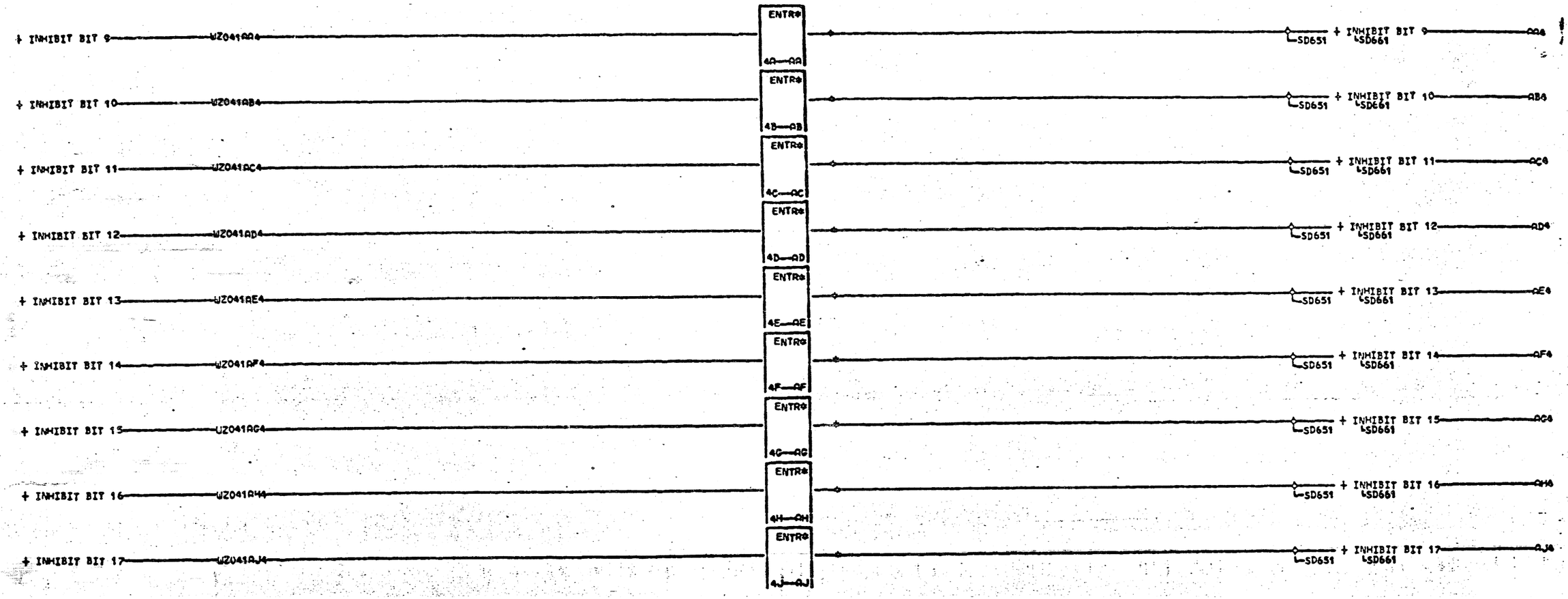
$ NOTE 2 + TO WRITE ZERO

AA4 Z-Z1B1A09 AJ4 Z-Z1C1E09
S32-Z1A1E09
AB4 Z-Z1B1B09
AC4 Z-Z1B1C09
AD4 Z-Z1B1D09
AE4 Z-Z1B1E09
AF4 Z-Z1C1B09
AG4 Z-Z1C1C09
AH4 Z-Z1C1D09

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

DATA INPUT
1 OF 2
DATE 04-27-67 PACH⊕ SJ-0
LOG 115N FRAME 63
P⊕N⊕ 2196679
IBM CORP⊕ CD BLK⊕ AX

SD611 009



NOTE 1 FOR LOCATION OF 632-Z1
REFER TO PAGE WZ011
$ NOTE 2 + TO WRITE ZERO

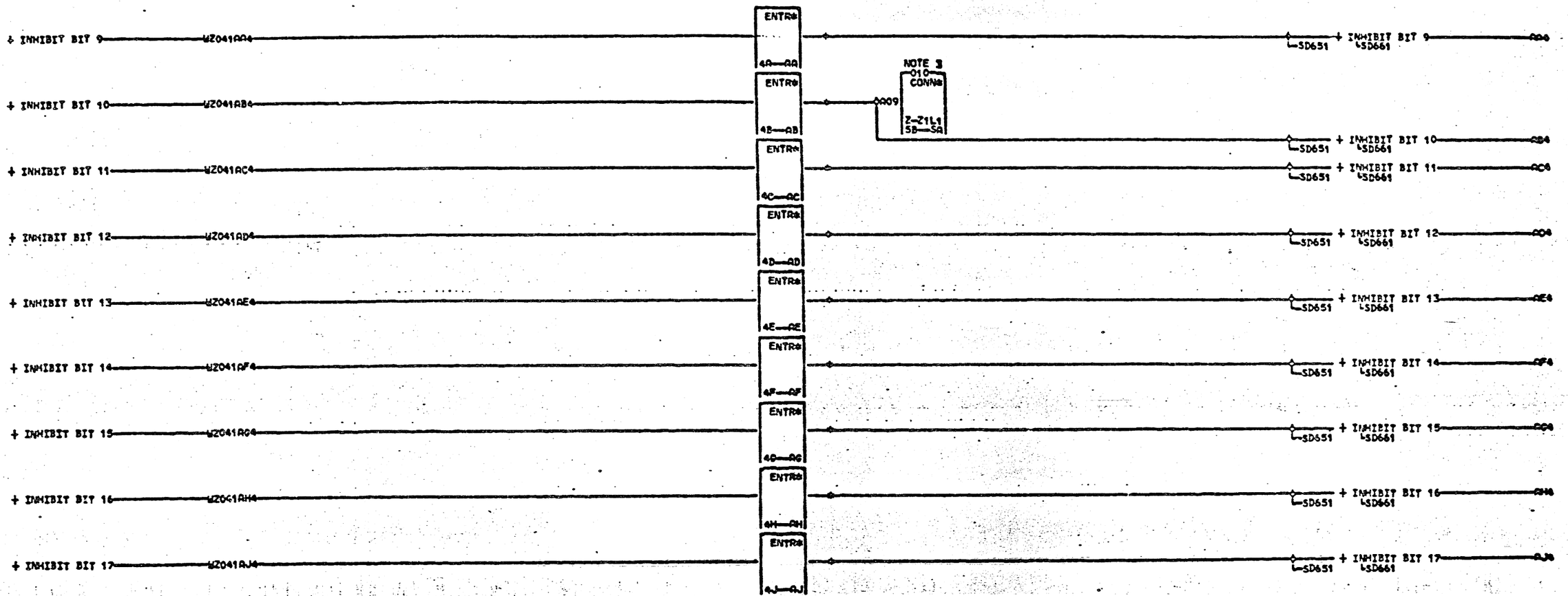
SD621
1
009

AA4 Z-Z1D1A09 AJ4 Z-Z1M1D09
AB4 Z-Z1L1A09
632-Z1K1E09
AC4 Z-Z1L1B09
AD4 Z-Z1L1C09
AE4 Z-Z1L1D09
AF4 Z-Z1L1E09
AG4 Z-Z1M1B09
AH4 Z-Z1M1C09

1-20-64 414300
5-07-65 414302
8-19-65 414308
3-15-66 256302
4-25-67 731503

DATA INPUT
2 OF 2
DATE 04-27-67 MACH. SJ-8
LOG 115N FRAME 63
P.N. 2196671
IBM CORP. CD SLK. AL

SD621
1
009



NOTE 1 FOR LOCATION OF 632-Z1 REFER TO PAGE WZ011
S NOTE 2 + TO WRITE ZERO
D NOTE 3 SYSTEM MAY REMOVE L2804 TO L1A09 REFER TO WZ041
8
2
1
010
SIM TO PN 2196671 EC 731503

AA4 Z-Z1D1A09 AJ4 Z-Z1R1D09
AB4 Z-Z1L1A09
632-Z1K1E09
AC4 Z-Z1L1B09
AD4 Z-Z1L1C09
AE4 Z-Z1L1D09
AF4 Z-Z1L1E09
AG4 Z-Z1R1B09
AH4 Z-Z1R1C09

04-26-67 731504

DATA INPUT
2 OF 2
DATE 04-26-67 MACH⊕ SJ-4
LOG 117J PROBE 63
P⊕N⊕ 2510218
IBM CORP⊕ CB BLK⊕ SB
S D 8 2 1 010

NOTE 2

+ INHIBIT BIT 0 — SD611AA4 — D02 A T03AB 3466AA Z-Z1D2 4B — AB — D03 — SD711 -INHIBIT BIT 0 4K — AB4

+ INHIBIT BIT 1 — SD611AB4 — B04 A T03AB 3466AB Z-Z1D2 4C — AC — B05 — SD711 -INHIBIT BIT 1 4K — AC4

+ INHIBIT BIT 2 — SD611AC4 — D05 A T03AB 3466AC Z-Z1D2 4D — AD — D04 — SD721 -INHIBIT BIT 2 4K — AD4

+ INHIBIT BIT 3 — SD611AD4 — B02 A T03AB 3466AD Z-Z1D2 4E — AE — B10 — SD721 -INHIBIT BIT 3 4K — AE4

+ INHIBIT BIT 4 — SD611AE4 — B09 A T03AB 3466AE Z-Z1D2 4F — AF — D06 — SD731 -INHIBIT BIT 4 4K — AF4

+ INHIBIT BIT 5 — SD611AF4 — D10 A T03AB 3466AF Z-Z1D2 4G — AG — B07 — SD731 -INHIBIT BIT 5 4K — AG4

+ INHIBIT BIT 6 — SD611AG4 — B08 A T03AB 3466AG Z-Z1D2 4H — AH — D09 — SD741 -INHIBIT BIT 6 4K — AH4

+ INHIBIT BIT 7 — SD611AH4 — B13 A T03AB 3466AH Z-Z1D2 4J — AJ — B12 — SD741 -INHIBIT BIT 7 4K — AJ4

+ INHIBIT BIT 8 — SD611AJ4 — D13 A T03AB 3466AJ Z-Z1D2 4K — AK — D11 — SD751 -INHIBIT BIT 8 4K — AK4

- INHIBIT TIME LESS THAN 4K — SD111AJ4 — D12 OR T03AJ 3466AK Z-Z1D2 2A — AA — D07

NOTE 1 FOR LOCATION OF 632-21 REFER TO PAGE W2011

NOTE 2 THE -INHIBIT BIT LEVELS ARE APPROX. 0 AND +0.7V

SD631 000

11-20-64 414300
05-27-65 414302
08-19-65 414308

INHIBIT INPUT BIT 0-8 LESS THAN 4K

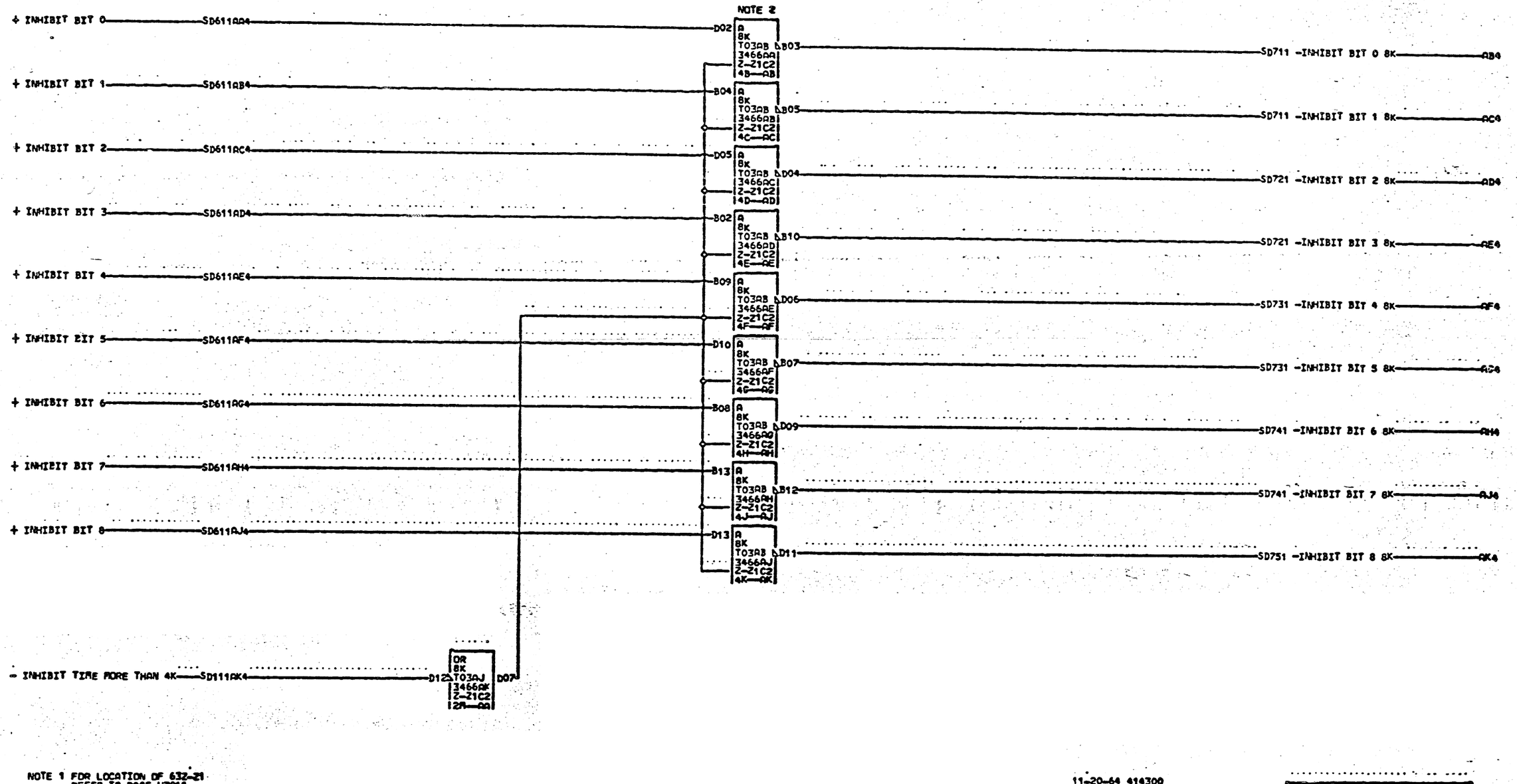
DATE 07-12-66 MACH. SJ-0

LOC 277F FRAME 63

P.N. 2196672

IBM CORP. CD BLK. AL

SD631 000



NOTE 1 FOR LOCATION OF 632-21 REFER TO PAGE WZ011

S NOTE 2 THE -INHIBIT BIT LEVELS ARE APPROX. 0 AND +0.7V

D
6
4
1

000

11-20-64 414300
05-07-65 414302
08-19-65 414308

INHIBIT INPUT BIT 0-8
MORE THAN 4K

DATE 07-12-66 MACH. SJ-6

LOG 277F FRAME 63

P.N. 2196673

IBM CORP. CD BLK. AL

S D 6 4 1 000

NOTE 2

+ INHIBIT BIT 9 — SD621AA4 — D02 — T03AB 3466AA Z-Z1K2 4B — AB — B03 — SD751 -INHIBIT BIT 9 4K — AB4

+ INHIBIT BIT 10 — SD621AB4 — B04 — T03AB 3466AB Z-Z1K2 4C — AC — B05 — SD761 -INHIBIT BIT 10 4K — AC4

+ INHIBIT BIT 11 — SD621AC4 — D05 — T03AB 3466AC Z-Z1K2 4D — AD — D04 — SD761 -INHIBIT BIT 11 4K — AD4

+ INHIBIT BIT 12 — SD621AD4 — B02 — T03AB 3466AD Z-Z1K2 4E — AE — B10 — SD771 -INHIBIT BIT 12 4K — AE4

+ INHIBIT BIT 13 — SD621AE4 — B09 — T03AB 3466AE Z-Z1K2 4F — AF — D06 — SD771 -INHIBIT BIT 13 4K — AF4

+ INHIBIT BIT 14 — SD621AF4 — D10 — T03AB 3466AF Z-Z1K2 4G — AG — B07 — SD781 -INHIBIT BIT 14 4K — AG4

+ INHIBIT BIT 15 — SD621AG4 — B08 — T03AB 3466AG Z-Z1K2 4H — AH — D09 — SD781 -INHIBIT BIT 15 4K — AH4

+ INHIBIT BIT 16 — SD621AH4 — B13 — T03AB 3466AH Z-Z1K2 4J — AJ — B12 — SD791 -INHIBIT BIT 16 4K — AJ4

+ INHIBIT BIT 17 — SD621AJ4 — D13 — T03AB 3466AJ Z-Z1K2 4K — AK — D11 — SD791 -INHIBIT BIT 17 4K — AK4

- INHIBIT TIME LESS THAN 4K — SD111AJ4 — D12 — OR T03AJ 3466AK Z-Z1K2 12A — AA — D07

NOTE 1 FOR LOCATION OF 632-Z1 REFER TO PAGE WZ011

NOTE 2 THE -INHIBIT BIT LEVELS ARE APPROX. 0 AND +0.7V

11-20-64 414300
05-07-65 414302
08-19-65 414308

INHIBIT INPUT BIT 9-17 LESS THAN 4K

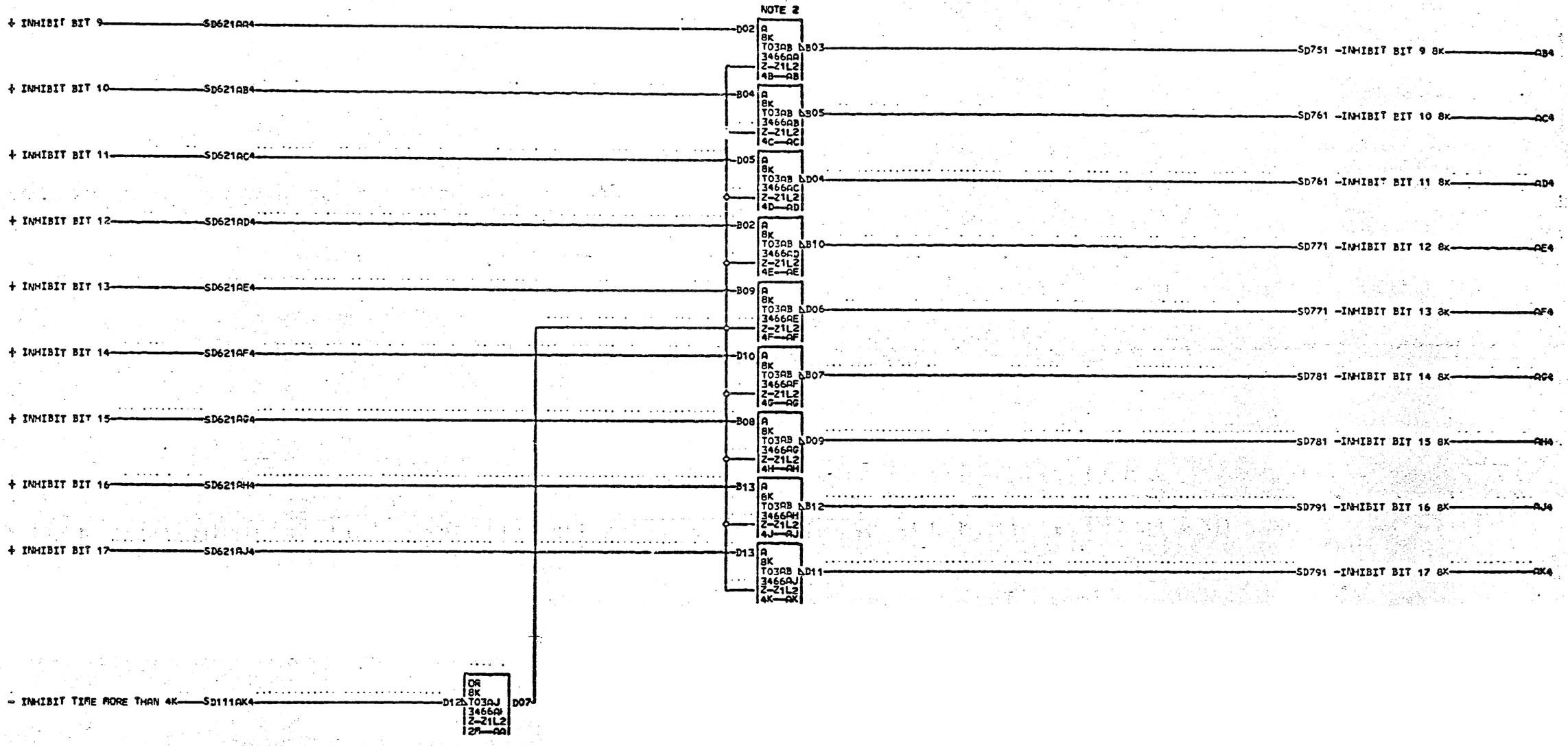
DATE 07-12-66 PACH. SJ-4

LOG 277F FRAME 63

P.No. 2196674

IBM CORP. CD BLK. AL

SD651 1 000



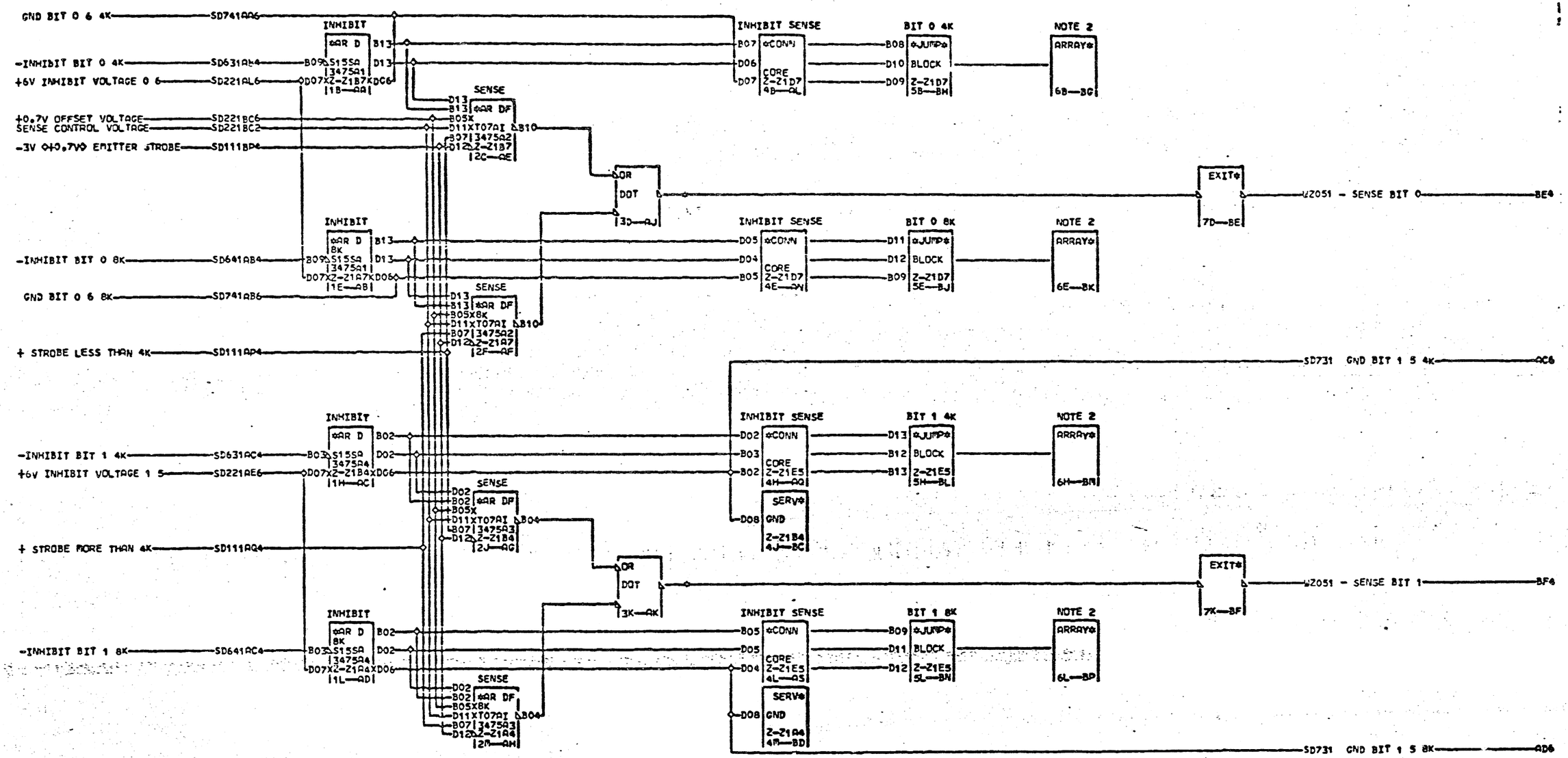
NOTE 1 FOR LOCATION OF 632-21
REFER TO PAGE W2011
NOTE 2 THE -INHIBIT BIT LEVELS
ARE APPROX. 0 AND +0.7V

SD661
009

11-20-64	414300
01-07-65	414302
08-19-65	414308

INHIBIT INPUT BIT 9-17
MORE THAN 4K
DATE 07-12-66 MACH. SJ-4
LOG 277F FRAME 63
P.N. 2196675
IBM CORP. CD BLK. AL

SD661 009



NOTE 1 FOR LOCATION OF 632-Z1 REFER TO PAGE WZ011 . AJ4 Z-Z1B1A11
$ NOTE 2 REFER TO SD061 AND SD062 FOR LOGIC TO ARRAY CONNECTIONS. AK4 Z-Z1B1B11

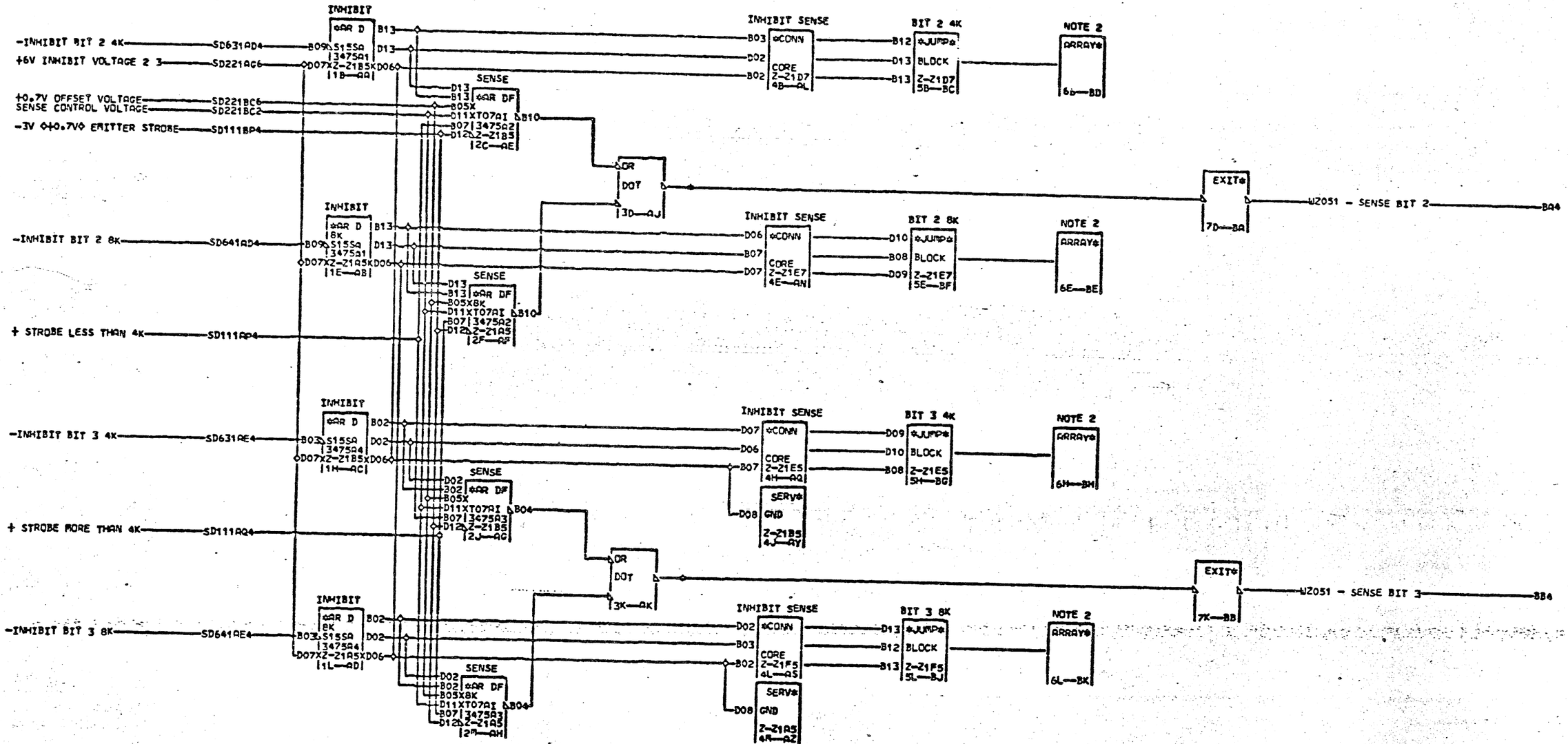
000

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

INHIBIT SENSE BIT 0 AND 1

DATE 04-27-67 PROG. SJ-4
LOG 115N FRAME 63
P.N. 2196676
IBM CORP. CD BLK. BQ

000



NOTE 1 FOR LOCATION OF 63Z-Z1
REFER TO PAGE WZ011

S NOTE 2 REFER TO SD061 AND SD062 FOR LOGIC TO ARRAY CONNECTIONS.

AJ4 Z-Z1B1C19
AK4 Z-Z1B1D19
63Z-Z1A1E19

11-20-64	414300
05-07-65	414302
08-19-65	414308
03-15-66	256302
04-25-67	731503

INHIBIT SENSE BIT 2 AND 3

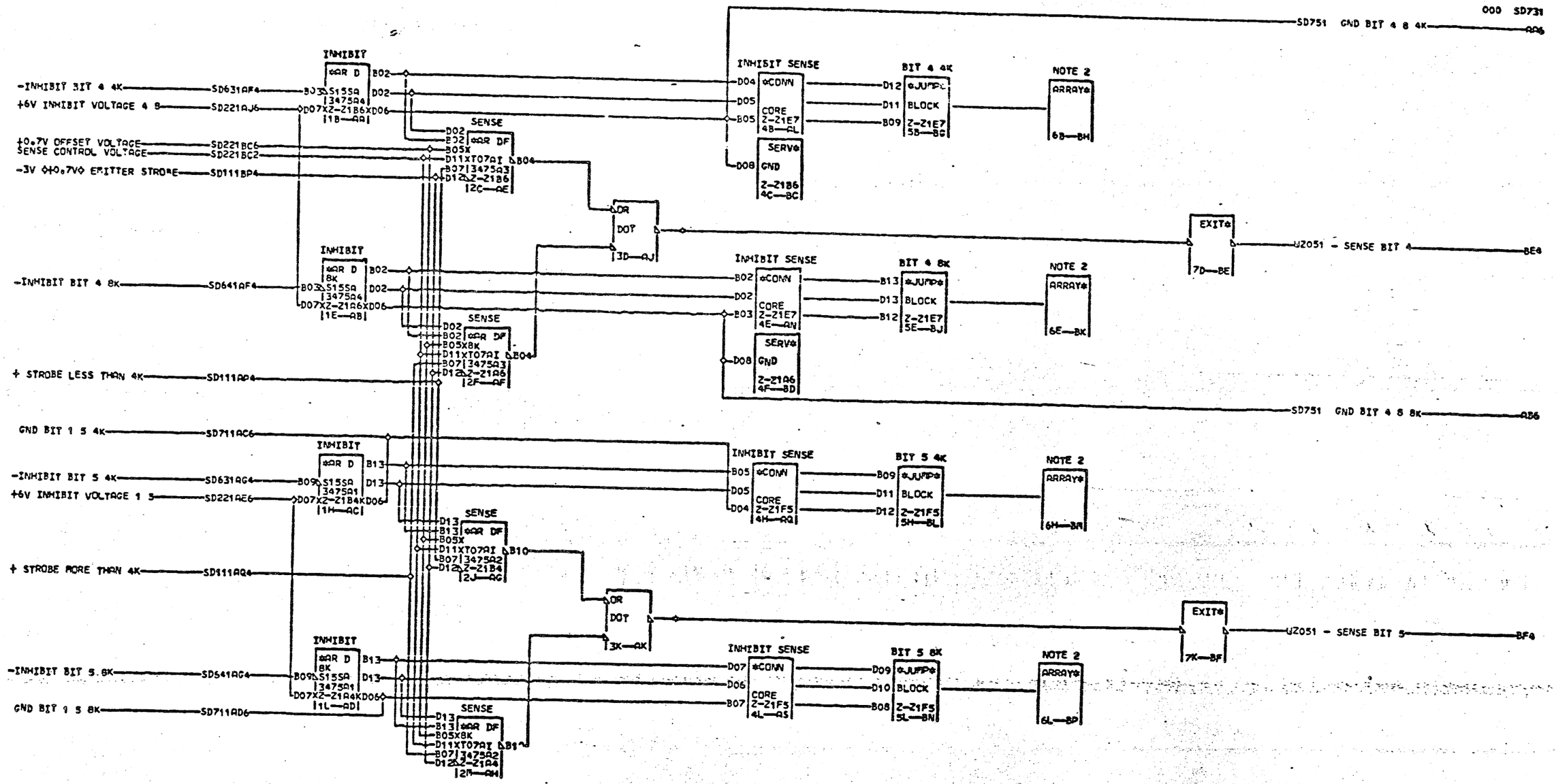
DATE 04-27-67 PACH: SJ-4

LOG 115N FRAME 63

P.N. 2196677

IBM CORP. CD BLK. BL

SD721 000



NOTE 1 FOR LOCATION OF 6X2-Z1 REFER TO PAGE WZ011

NOTE 2 REFER TO SD061 AND SD062 FOR LOGIC TO ARRAY CONNECTIONS.

AJ4 Z-Z1B1E11
AK4 Z-Z1C1B11

11-20-64	414300
05-07-65	414302
08-19-65	414308
03-15-66	256302
04-25-67	731503

INHIBIT SENSE BIT 4 AND 5

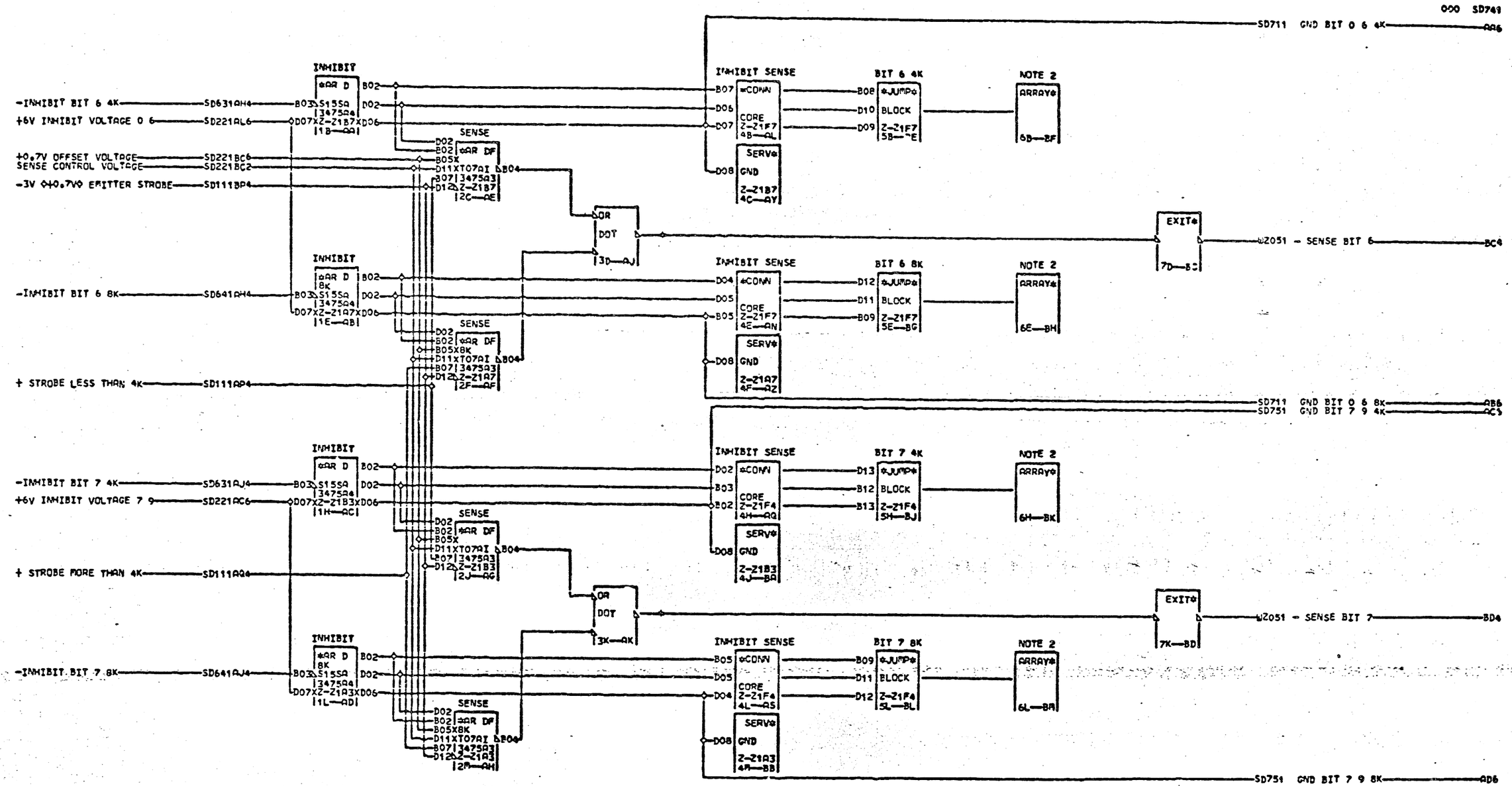
DATE 04-27-67 PROM. SJ-4

LOG 115N FRAME 63

P.N. 2196878

IBM CORP. CD BLK. 80

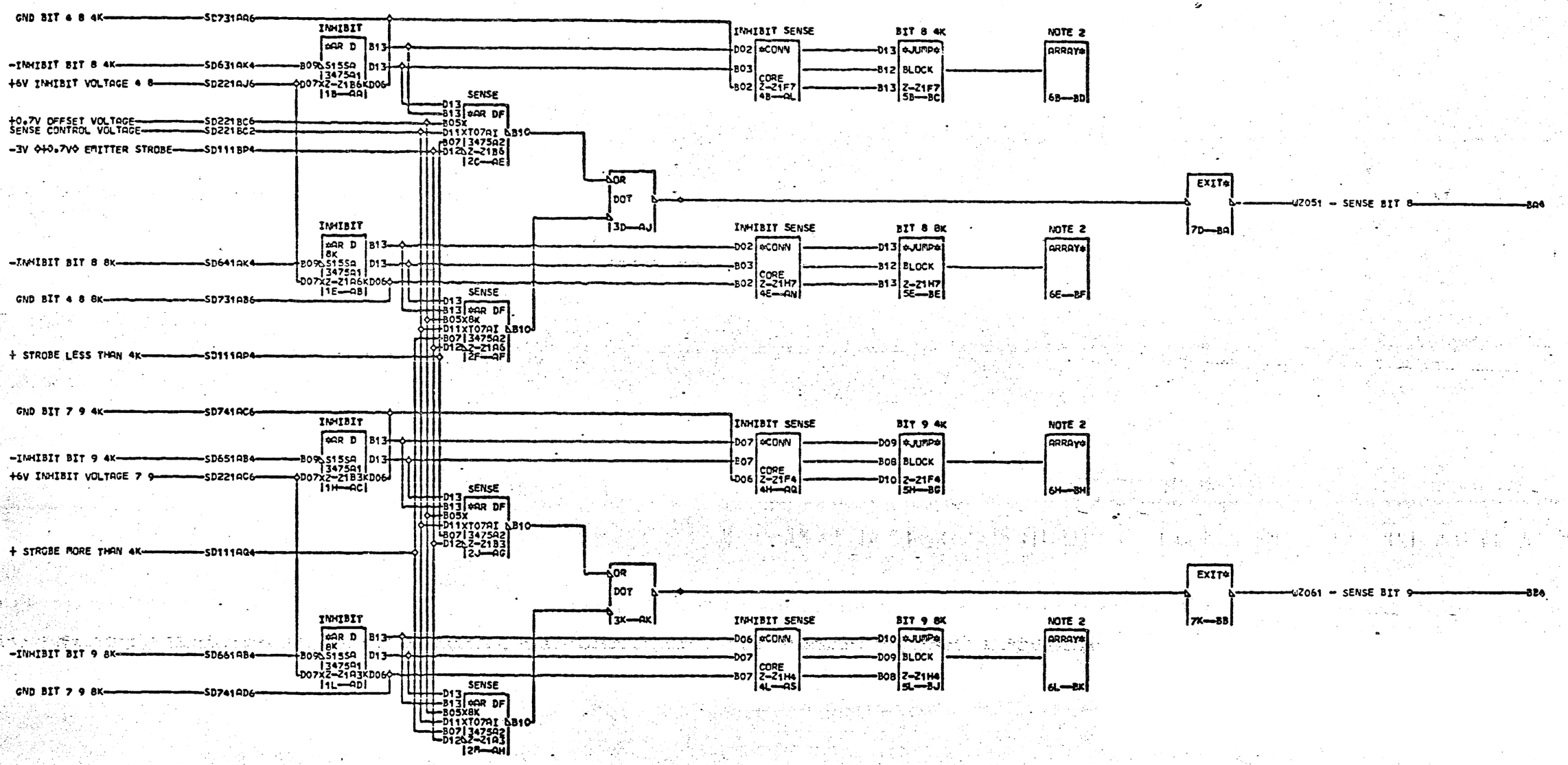
SD23191 009



NOTE 1 FOR LOCATION OF 632-Z1
REFER TO PAGE WZ011 — AJ4 Z-Z1C1C11
NOTE 2 REFER TO SD061 AND SD062 FOR LOGIC TO ARRAY CONNECTIONS. — AK4 Z-Z1C1D11; 632-Z1C1A11

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

INHIBIT SENSE BIT 6 AND 7
DATE 04-27-67 MACH. SJ-4
LOG 115N FRAME 63
P.N. 2196679
IBM CORP. CD BLK. BN



NOTE 1 FOR LOCATION OF 632-21
REFER TO PAGE WZ011 AJ4 Z-Z1C1E11
S NOTE 2 REFER TO SD061 AND AK4 Z-Z1D1A11
D SD062 FOR LOGIC TO
7 ARRAY CONNECTIONS.
5
1
000

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

INHIBIT SENSE BIT 8 AND 9

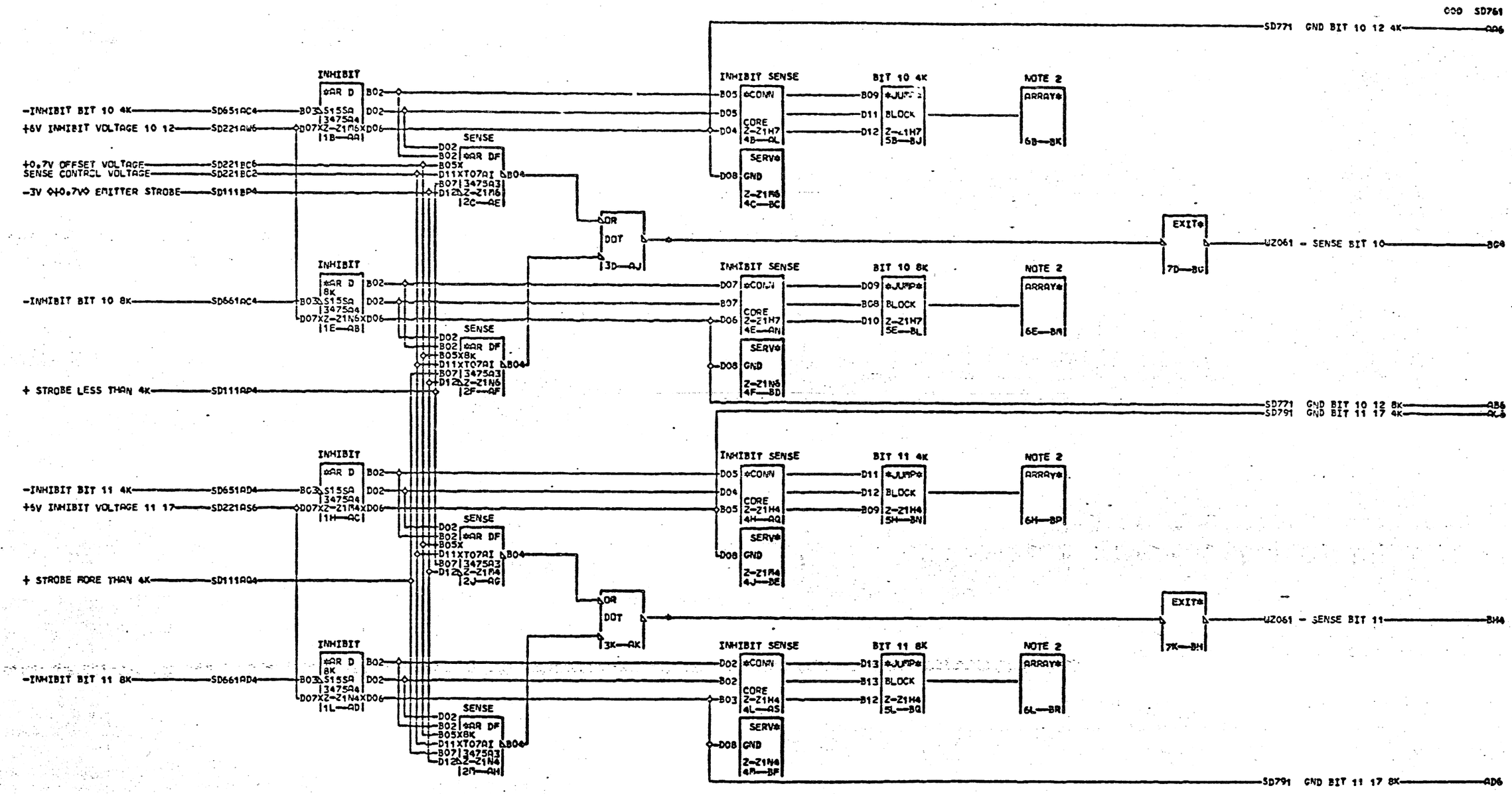
DATE 04-27-67 PROM. SJ-4

LOG 115N FRAME 63

P.No. 2196880

IBM CORP. CD BLK. BL

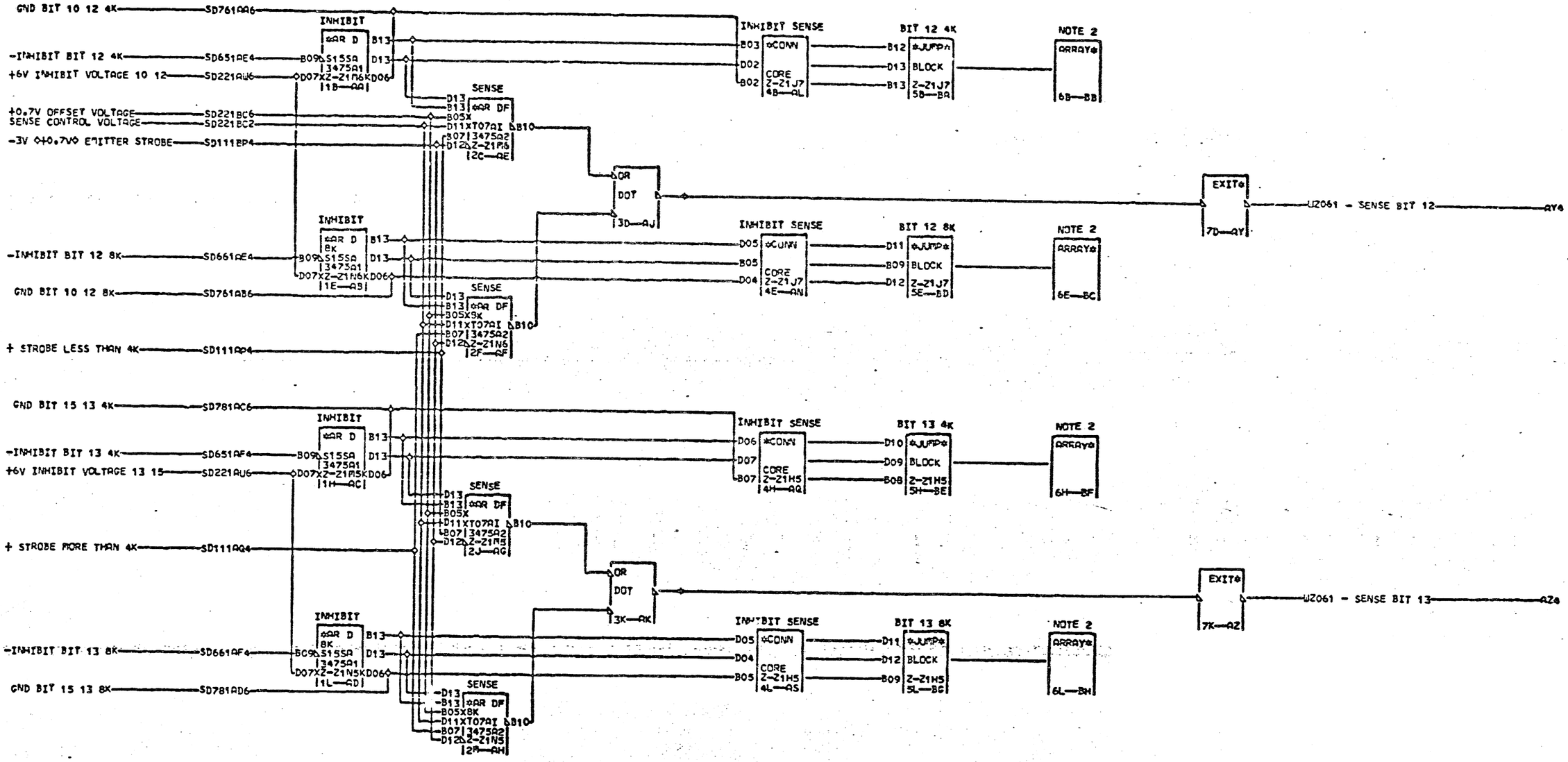
S D 7 5 1 000



NOTE 1 FOR LOCATION OF 63Z-Z1 REFER TO PAGE WZ011 AJ4 Z-Z1L1A11
NOTE 2 REFER TO SD061 AND SD062 FOR LOGIC TO ARRAY CONNECTIONS. AK4 Z-Z1L1E11

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

INHIBIT SENSE BIT 10 AND 11
DATE 04-27-67 MACH. SJ-0
LOG 115N FRAME 63
P.N. 2196681
IBM CORP. CD BLK. BS



NOTE 1 FOR LOCATION OF 63Z-Z1
REFER TO PAGE WZ011 AJ4 Z-Z1L1C11
NOTE 2 REFER TO SD061 AND AK4 Z-Z1L1D11
SD062 FOR LOGIC TO 63Z-Z1K1E11
ARRAY CONNECTIONS.

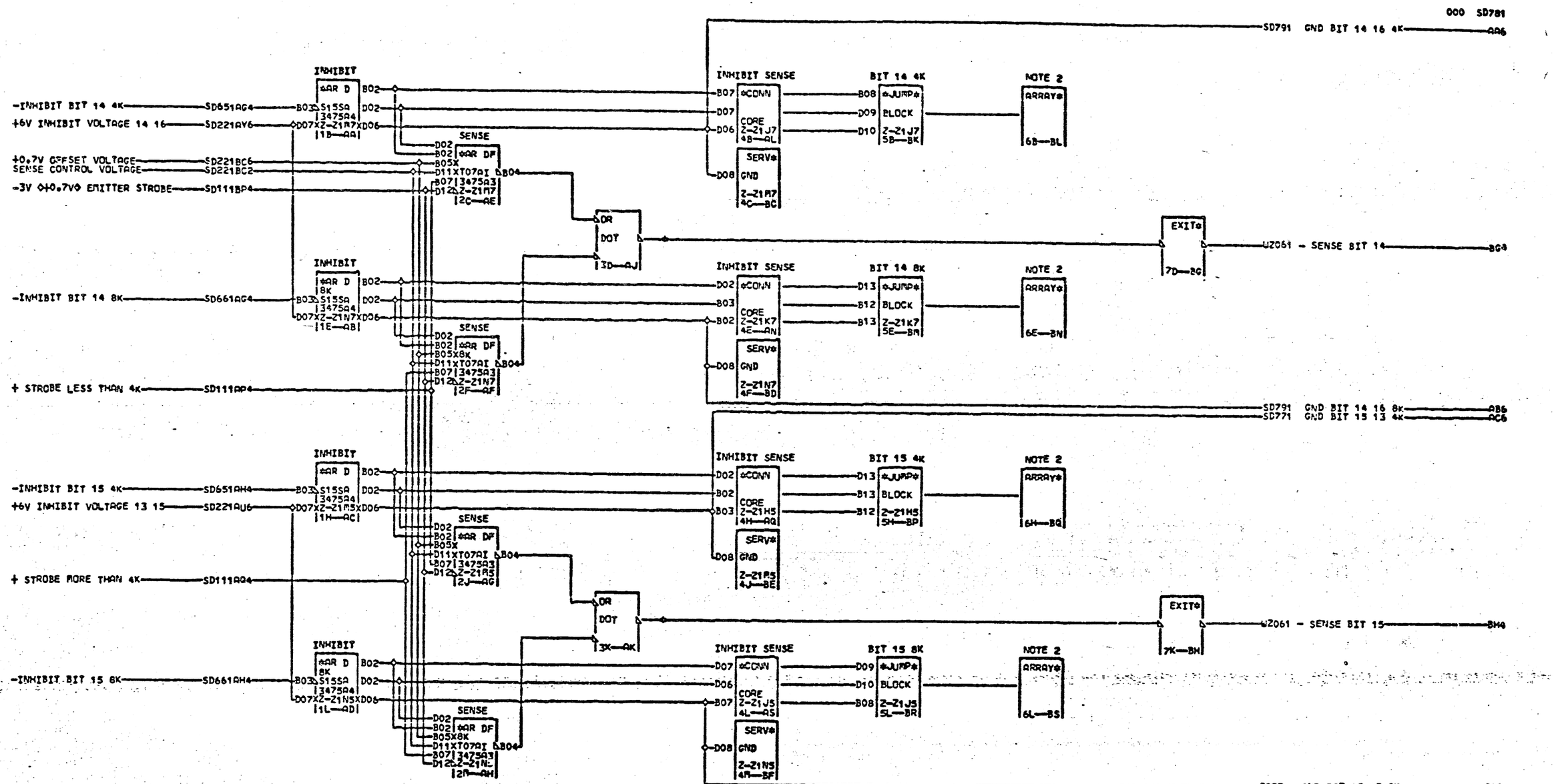
S 9 7 1 1 000

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

INHIBIT SENSE BIT 12 AND 13

DATE 04-27-67 MACH. SJ-4
LOG 115N FRAME 63
P.N. 2196882
IBM CORP. CD BLK. BJ

S 9 7 1 1 000



NOTE 1 FOR LOCATION OF 632-Z1 REFER TO PAGE WZ011

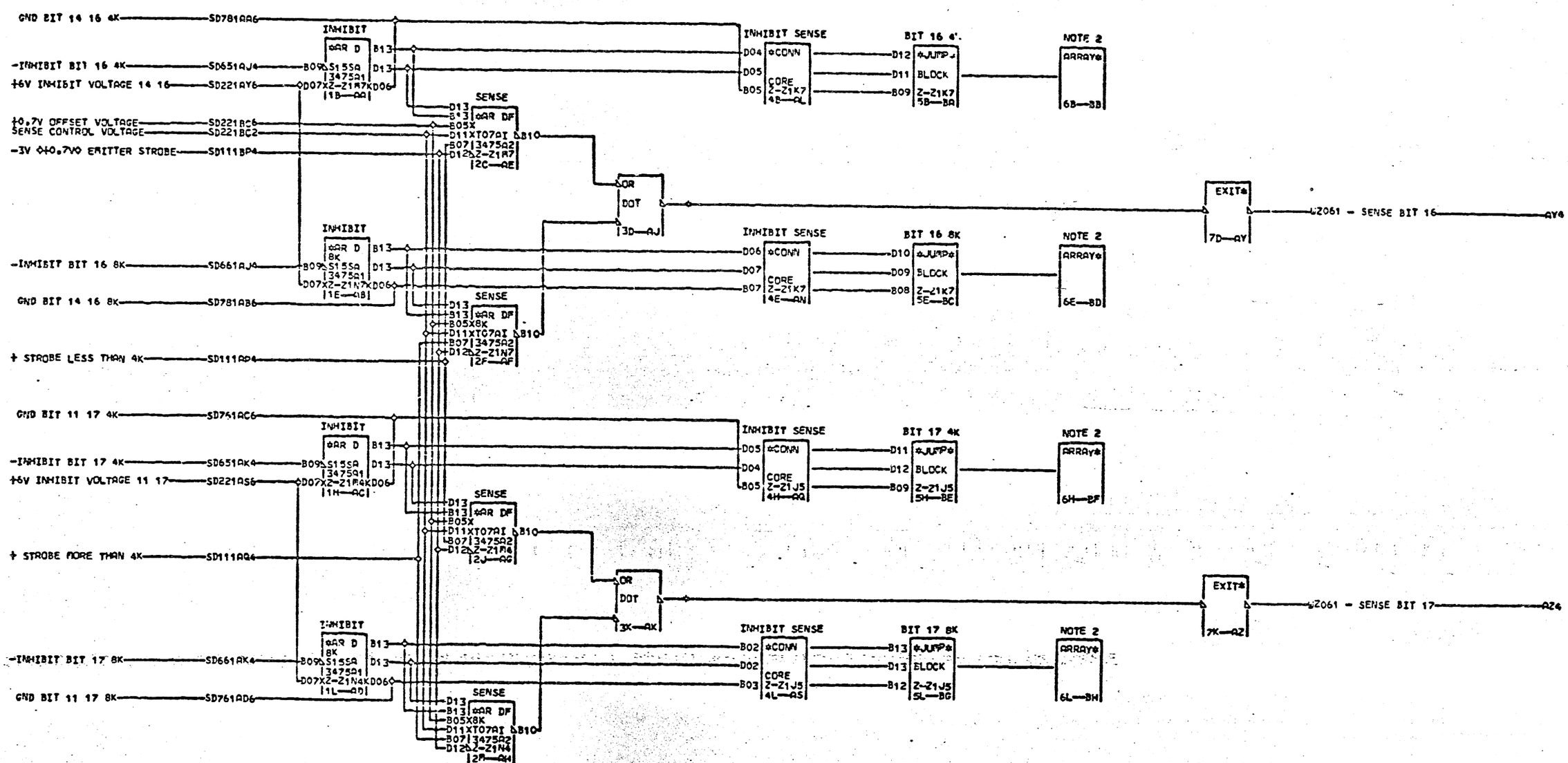
NOTE 2 REFER TO SD061 AND SD062 FOR LOGIC TO ARRAY CONNECTIONS.

AJ4 Z-Z1L1E11
AK4 Z-Z1M1B11

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

INHIBIT SENSE BIT 14 AND 15	
DATE 04-27-67 MACH. SJ-4	
LOG 115N FRAME 63	
P.No. 2196683	
IBM CORP. CD BLK. BT	

S 9 8 1 000



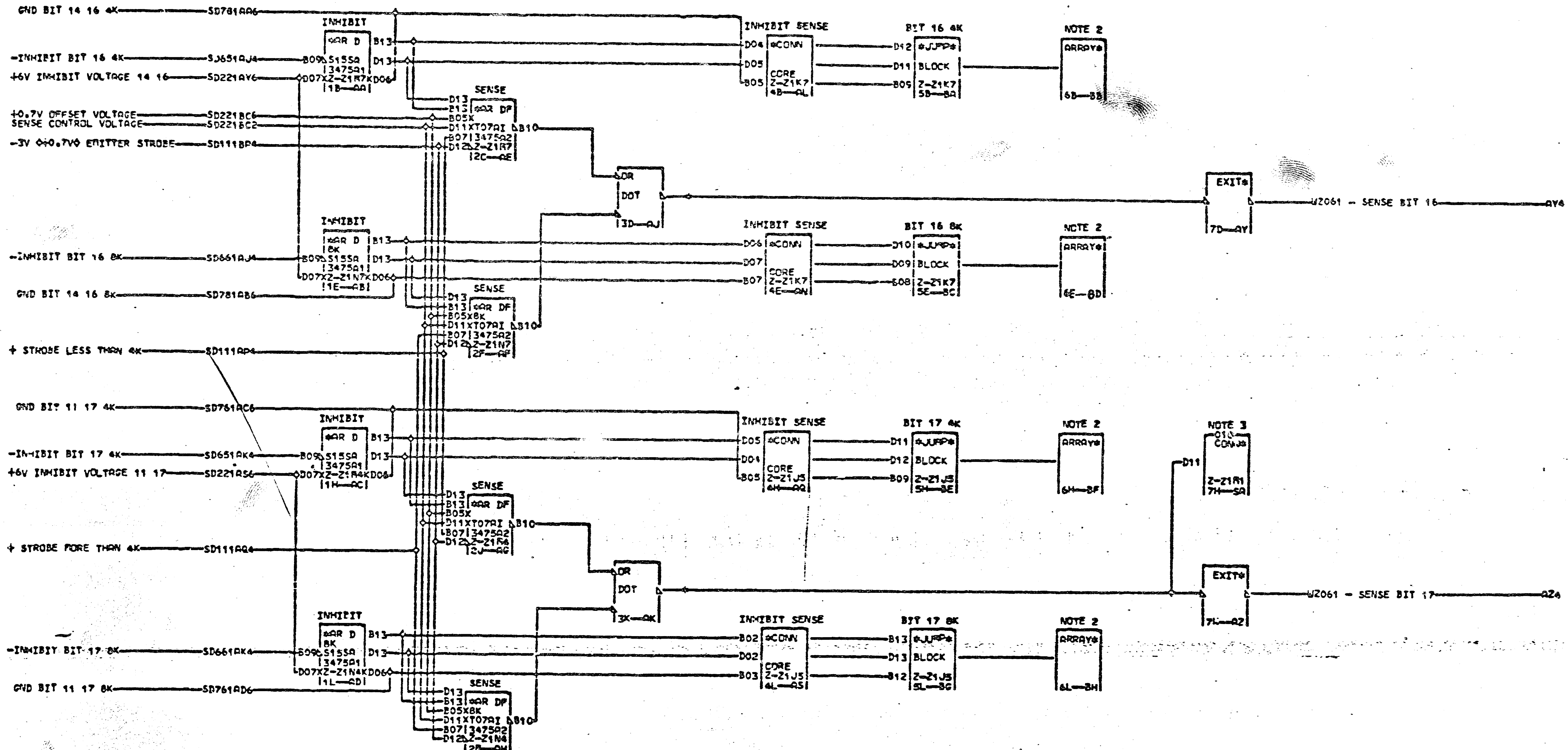
NOTE 1 FOR LOCATION OF 63Z-Z1
REFER TO PAGE WZ011 — AJ4 Z-Z1A1C11
$ NOTE 2 REFER TO SD061 AND — AK4 Z-Z1A1D11
SD062 FOR LOGIC TO — 63Z-Z1A1A11
ARRAY CONNECTIONS.
9 NOTE 3 SYSTEM MAY REMOVE N4B10
1 TO M1D11.REFER TO WZ061

009

11-20-64 414300
05-07-65 414302
08-19-65 414308
03-15-66 256302
04-25-67 731503

INHIBIT SENSE BIT 16 AND 17
DATE 04-27-67 PROM. SJ-4
LOG 115N FRAME 63
P.N. 2196684
IBM CORP. CD BLK. BJ

$ 9 9 1 009



NOTE 1 FOR LOCATION OF 63Z-Z1 REFER TO PAGE WZ011
NOTE 2 REFER TO SD061 AND SD062 FOR LOGIC TO ARRAY CONNECTIONS.
NOTE 3 SYSTER RAY REMOVE N4B10 TO M1D11.REFER TO WZ061

AJ4 Z-Z1M1C11
AK4 Z-Z1M1D11
63Z-Z1M1A11

SD791

010
SIM TO PN 2196684 EC 731503

04-26-67 731504

INHIBIT SENSE BIT 16 AND 17			
DATE	04-26-67	MACH.	SJ-4
LOG	117J	FRAME	63
		P.N.	2510219
IBM CORP.	CD	BLK.	SB

SD791
010