HP 3000 Computer System

Preface To The HP 30341A HP-IB Interface Module

Diagnostic Manual Set

HEWLETT PACKARD

COMPUTER SYSTEMS DIVISION, 19447 PRUNERIDGE AVE., CUPERTINO, CALIF. 95014

Part No. 30341-90003
Index No. 3HDWR.30341-90003

Printed in U.S.A 5/81

LIST OF EFFECTIVE PAGES

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. Changes are marked with a vertical bar in the margin. If an update is incorporated when an edition is reprinted, these bars are removed but the dates remain.

PRINTING HISTORY

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The date of the title page of the manual changes only when a new edition is published. When an edition is reprinted, all the prior updates to the edition are incorporated.

The HP 30341A Interface Module Hardware Self-Test is a CPU ROM-resident, microcode diagnostic that verifies correct operation of the Interface Module's hardware. The self-test can be initiated either by issuing the the Initiate Selftest (SLFT) instruction from software to the Interface Module's Intermodule Bus Adapter (IMBA) PCA or by manually actuating the Bus Interface Controller (BIC) PCA's CPU TEST Switch S1. Switch S1 is located at center left on the front edge of the BIC PCA.

The results of the self-test are stored in the computer system's SLFT "mailbox" memory location MB2 and displayed by 10 LED's (A thru I and "*") located on the left-front edge of the BIC PCA. Termination of the self-test is indicated by the BIC PCA's "*" LED being cleared (off) and the busy/wait flag (bit 0) in "mail-box" memory location MB4 being set. The octal value (error code) contained in MB2 or indicated by A thru I LED's indentify which portion of the self-test that failed as listed in the following tables. It should be noted that the error codes contained in the second table pertain to specific Control Store ROM chips located on the Processor PCA.

If the self-test is initiated with no peripheral devices attached to the HP-IB, successful test completion is indicated by %74 in memory location MB2 and %740 indicated by the A thru I LED's. If the self-test is initiated with no cold-load device attached to the HP-IB (e.g., HP 2680A only), successful test completion is indicated by %75 in MB2 and %750 indicated by the LED's. If the self-test is initiated with a cold-load device attached to the HP-IB (e.g., HP7976A), successful test completion is indicated by %00 in MB2 and %000 indicated by the LED's.

Note

The BIC LED's will momentarily flash error codes %740 and %750 before remaining lit to indicate that a hard error does not exist and to serve as a warning that a particular device is not attached to the HP-IB.

Table 1. Hardware Self-Test Summary

Hardware Under Test	Octal Error Code		Test
	MB2	BIC LEDs	
Processor PCA			
PCU	10	100	TAV, IBV, Stackbit
	11	110	Skip On Immediate, DBUS, INDR; LINK
	12	120	AV, BV, SAVEA, SAVB; JMP, JMPL, JSB, RSB
	13	130	CIR, Mapper, ATTN
RALU	14	140	Registers
	15	150	Extended Registers
	16	160	ALU
	17	170	Shift Logic, Link Logic
RASS Unit	20	200	Counter, STA0, 3 (PRV, ROP), F1
	21	210	Comparators, BV Logic, ISR10-13, ATTN
	22	220	PADD Logic, CIR
	23	230	Registers
	24	240	STA-7 (Overflow, Carry, Condition Code)
BIC PCA and IMB	25	250	ISR, Skip-On-Test, Int Sync Reg, ATTN
	26	260	CPUDOIT, CPUDONE, Timeout, Float State of IMB
	27	270	Freeze Logic
Processor PCA ROMs	30-47	300-470	CRC for each Processor PCA ROM. Refer to table 2.
Memory Verify	60	600	Verify reads and writes to %777
Memory Verify	61	610	Verify reads and writes to %777
Memory Verify	62	620	Bandwidth verification of reads
Memory Verify	63	630	Bandwidth verification of reads
GIC PCA and IMBA PCA	65	650	Verify GIC configuration Channel = channel with lowest channel number " 1
	66	660	MI to GIC register communication
	67	670	Verify DNV (data not valid) operation

Table 1. Hardware Self-Test Summary (Continued)

Hardware Under Test	Octal Error Code		Test
	MB2	BIC LEDs	
GIC PCA and IMBA PCA (Con't)	70	700	CSRQ due to SIOP test
	71	710	CSRQ due to PHI interrupt for all devices
	72	720	Verify GIC interrupt logic and IRQ operation
	73	730	Verify CSRQ from DMA circuitry, PHI and FIFOs. Also verifies IMBA's ability to execute memory operations.
HP-IB Interface	74	740	Verifies that HP-IB device exists on channel. Device numbers 0 - 7 are tried on GIC from step 65
I.D. Verify	75	750	Verifies that HP-IB load device exists on channel. Device numbers 0 - 7 are tried on GIC from step 65
Write/Read	76	760	Write/Read loop back to device # of step 75, assumed cold load device

Table 2. Processor PCA ROM Error Codes

Octal Error Code		Defective ROM Reference Designator	Octal Error Code		Defective ROM Reference Designator
MB2	BIC LEDs		MB2	BIC LEDs	
30	300	U-131	40	400	U-133
31	310	U-141	41	410	U-143
32	320	U-151	42	420	U-153
33	330	U-161	43	430	U-163
34	340	U-132	44	440	U-134
35	350	U-142	45	450	U-144
36	360	U-152	46	460	U-154
37	370	U-162	47	470	U-164

NOTES

NOTES