Hewlett-Packard
98041A Disc Interface
Installation and Service Manual

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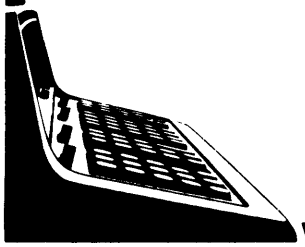

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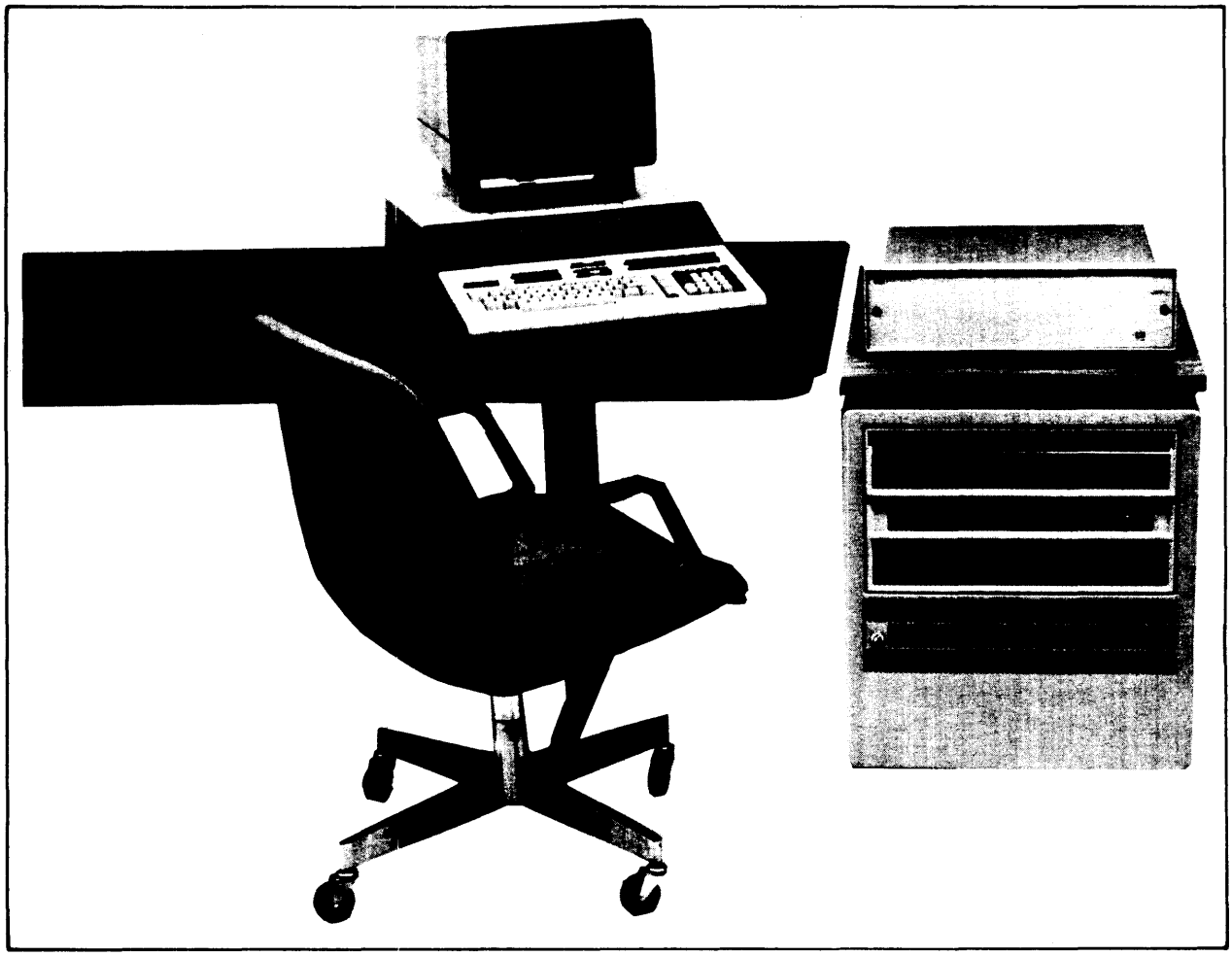

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Figures

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Chapter 1
General Information

Introduction

The HP 98041A Disc Interface connects an HP System 45 Desktop Computer to a wide variety of high speed, mass storage peripherals.

This manual provides you with 98041A equipment specifications, installation procedures and general mass storage system information. In addition, service information including the theory of operation for the interface, replaceable parts lists, component locators and schematics is provided.

Equipment Supplied

The following items are supplied with each disc interface.

Description	Quantity	Part Number
Installation Manual	1	98041-90000
Power Cord	1	8120-1378*
Spare Fuse		
.75A,250V,NB	1	2110-0033
1.5A,250V,NB	1	2110-0043
Rack Mount Hardware		
Screws	4	2680-0103
Washer	4	3050-0257

* Part number for the standard power cord is shown. Refer to "Power Cords" in Chapter 2 for options.

Specifications

The following specifications are for the 98041A Disc Interface only. Refer to the Installation and Service Manuals for each mass storage unit in the system for its specifications and operating limitations.

Technical Specifications

Environmental

Operating Temp: 0° C to 55° C

Non-Operating Temp: −40° C to 65° C

Relative Humidity: 0 to 95% at 25° to 40° C (77° to 104° F)
thout condensation

Physical Dimensions

Height: 13.34 cm (5.25 in)

Width: 40.64 cm (16 in)

Length: 30.48 cm (12 in)

Weight: 9.34 kg (20 lbs 12 oz)

Chapter 2
Installation

Power Requirements

The disc interface operates from power line voltages of 100, 120, 220 or 240 volts ac. The range of operation is within +5% and −10% of each nominal voltage. Two switches on the disc interface back panel permit selection of any one of the four nominal voltages (see Figure 2-1). The line frequency must be within 48 to 66 Hz. The disc interface requires a maximum of 120 voltamps.

CAUTION

THE DISC INTERFACE MAY BE DAMAGED IF THE LINE VOLTAGE SWITCH SETTINGS ARE INCORRECT. CHECK THE SWITCH SETTINGS BEFORE APPLYING POWER.

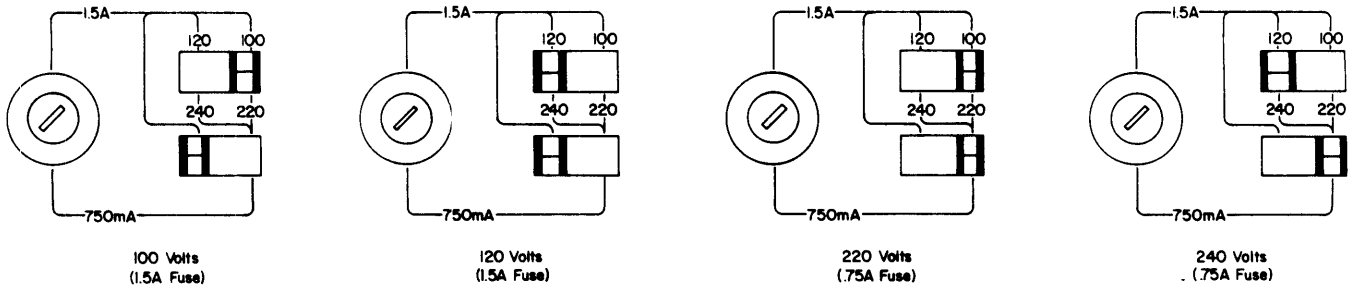


Figure 2-1: Line Voltage Switches

Grounding Requirements

The National Electrical Manufacturers' Association (NEMA) recommends that the disc interface be grounded to protect operating personnel from electrical shock. The disc interface is equipped with a three-conductor power cable which, when connected to an appropriate receptacle, grounds the cabinet of the interface.

Fuses

The disc interface must be fitted with a 1.5 amp normal blow fuse for 100-120 volt operation or a .75 amp normal blow fuse for 220-240 volt operation. Fuse part numbers are listed in the Equipment Supplied Table in Chapter 1.

WARNING

BEFORE CHANGING THE FUSE, BE SURE THAT THE DISC INTERFACE IS DISCONNECTED FROM ANY POWER SOURCE.

To remove a fuse, press in on the cap of the fuse holder and twist the cap in the direction indicated by the arrow on the cap. Pull the cap free and remove the fuse.

To install a fuse, place either end of the fuse into the pocket in the cap and reinstall the cap by pressing in on the cap and twisting it in the opposite direction from the arrow.

Always be sure that the correct fuse is used. The wrong fuse could result in damage to the disc interface if a malfunction or unusual line voltage occurs.

Power Cords

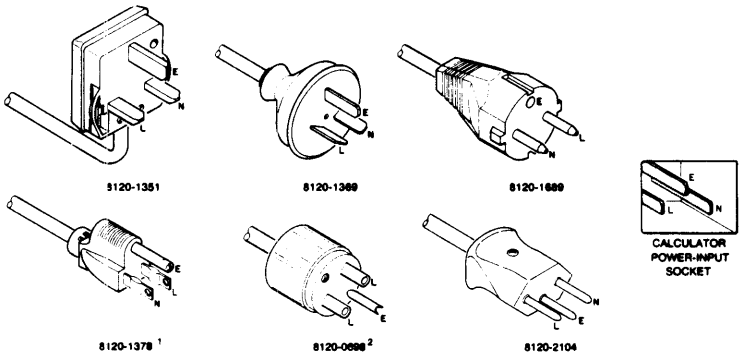
Power cords supplied by HP will have polarities matched to the power-input socket on the equipment, as shown below:

- L = Line or Active Conductor (also called 'live' or 'hot')
- N = Neutral or Identified Conductor
- E = Earth or Safety Ground

WARNING

IF IT IS NECESSARY TO REPLACE THE POWER CORD, THE REPLACEMENT CORD MUST HAVE THE SAME POLARITY AS THE ORIGINAL, OTHERWISE A SAFETY HAZARD FROM ELECTRICAL SHOCK TO PERSONNEL, WHICH COULD RESULT IN INJURY OR DEATH, MIGHT EXIST. IN ADDITION, THE EQUIPMENT COULD BE SEVERELY DAMAGED IF EVEN A RELATIVELY MINOR INTERNAL FAILURE OCCURRED.

Power cords with different plugs are available for the equipment; the part number of each cord is shown in Figure 2-2. Each plug has a ground connector. The cord packaged with the equipment depends upon where the equipment is to be delivered.



[1]UL and CSA approved for use in the United States of America and Canada with equipment set for either 100 or 120 Vac operation.

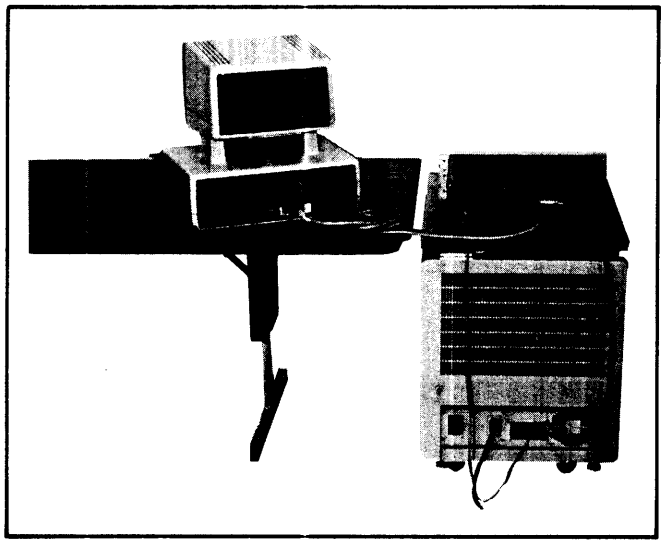
[2]UL and CSA approved for use in the United States of America and Canada with equipment set for either 200 or 240 Vac operation.

Figure 2-2: Power Cords

Installing the Disc Interface

The disc interface should be installed between the computer and the mass storage units in the system. Be sure that the computer and the disc interface are both off before connecting any cables to either instrument.

Plug the disc interface I/O card into any one of the I/O slots in the back of the computer. The mass storage controller unit (or units) connect to the HP-IB connector located on the back of the 98041A central data unit. Figure 2-3 shows a 98041A Disc Interface connected to a System 45 computer and an HP 13037B Disc Controller with a 7906A Disc Drive.



Figue 2-3: Connecting the HP 98041A Disc Interface

Interface Select Code

The 98041A is preset at the factory to select code 12. Select code 12 is the computer's default select code whenever a MASS STORAGE IS statement is executed specifying a mass storage unit that is connected to a 98041. Refer to "Mass Storage Operations" in the computer Operating and Programming manual for details concerning mass storage program statements.

If you need to change the select code setting on the disc interface, it can be set to any value from 1 to 12. The select code switch is accessible through a small hole on the top of the I/O card case (Figure 2-4). To change the setting, rotate the switch using a small screwdriver until the small arrow on the switch points to the desired select code number.

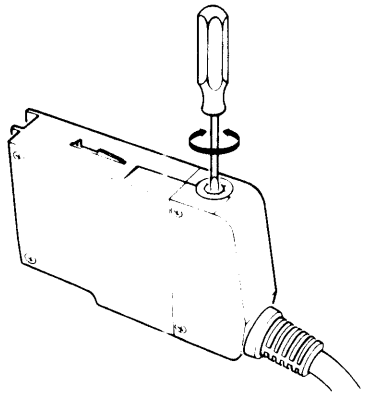


Figure 2-4: Interface Select Code Switch

HP-IB Capabilities

Although the 98041A Disc Interface is a valid implementation of the HP-IB IEEE standard 488-1975, the special use of specific secondary commands that are unique to specific mass storage controllers does not permit using other HP-IB peripherals (such as Plotters, Printers, Tape Drives, etc.) with the 98041. All other HP-IB peripherals should be connected to the computer via a 98034A HP-IB Interface.

NOTE

Although both interfaces use the same type of connector, only properly designed mass storage controllers should be connected to the 98041A Disc Interface and general HP-IB peripherls should be connected to the 98034A HP-IB Interface.

Refer to Supplement A to this manual for a complete list of the HP mass storage units that are compatible with the 98041A.

Connecting Mass Storage Controllers

A maximum of two mass storage controller units may be connected to an HP 98041A Disc Interface. These controllers can be separate units that can each control several disc drives, or a controller and a disc drive built into one unit.

Interconnecting Cables

Standard HP-IB cables are used to connect the mass storage controller units in your system to the disc interface. Listed in Figure 2-5 are the accessory numbers of the various cables that are available.

Length	Accessory Number
1 metre	10631A
2 metres	10631B
4 metres	10631C

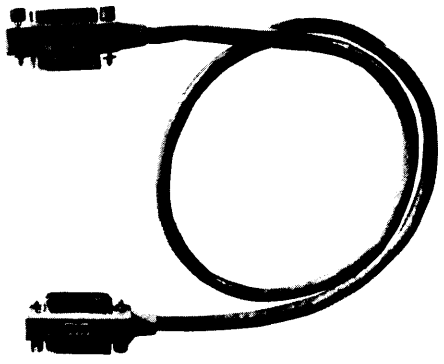


Figure 2-5: Standard HP-IB Cables

Cable Length Restrictions

The total cable length connecting the disc interface with the mass storage controllers connected to it must be less than or equal to 6 metres. The cable may be distributed between the disc interface and the mass storage controllers in any manner that is practical, as long as the total length does not exceed 6 metres. This cable length restriction does not, however, include any cables used to connect a controller to its various disc drives. Refer to the installation manual for each disc drive and disc controller unit in your system for information concerning the cables and connections between those units. Figure 2-6 shows example system configurations using the allowable cable length of 6 metres between the disc interface and various disc controller units.

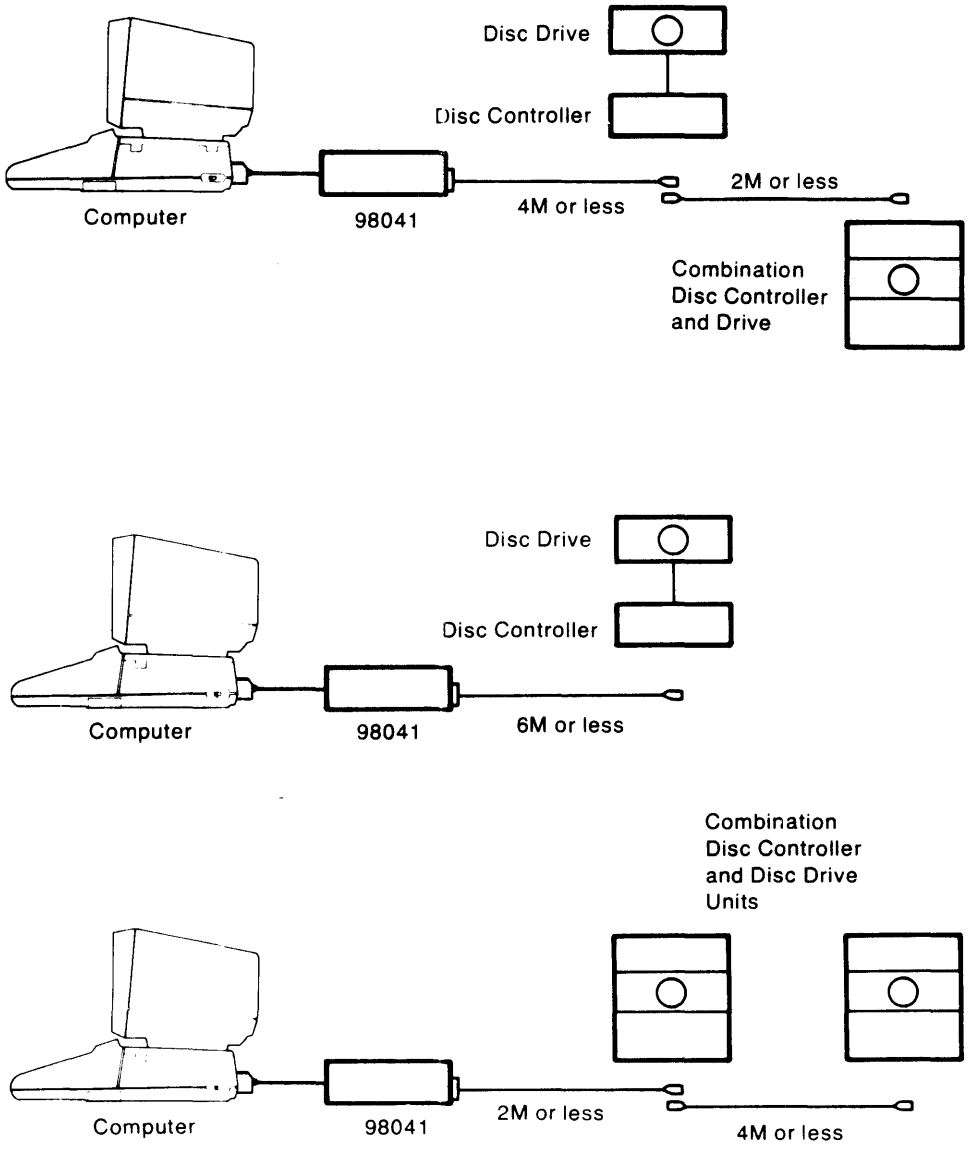


Figure 2-6: Example System Configurations

ROM Requirements

The disc interface requires that the Mass Storage ROM be properly installed in the computer to provide the statements necessary to store data on the mass storage units. Refer to the Mass Storage Techniques Manual for ROM installation and programming information.

Mass Storage Unit Installation

The installation procedure for the various mass storage units that are compatible with the disc interface are contained in their respective Installation and Service Manuals. Refer to Supplement A for a listing of the manual part number of each compatible unit.

Rack Mounting

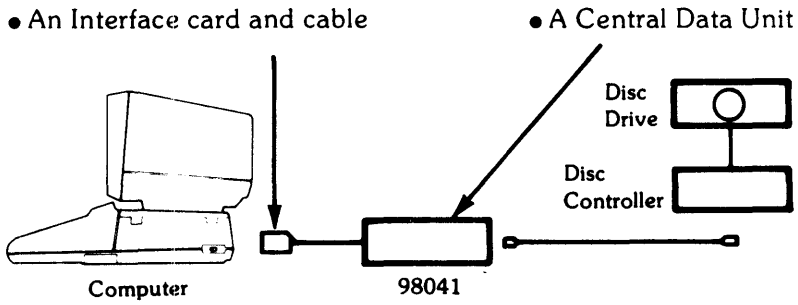
Rack Mounting

The 98041A Disc Interface can be mounted in an instrument rack by fastening the front panel casting to the rack with the four mounting supplied with the interface. Remove the interface's front panel by turning the two screws located on either side of the front panel. These screws release the front panel when they are turned 90° in either direction. Lift off the front panel to expose the two mounting holes on each side of the front casting. After securing the unit to the rack, replace the front panel.

Chapter 3
Theory of Operation and Service

Disc Interface General Description

The 98041A Disc Interface consists of two physical components as shown in the typical system block diagram below.



The Interface card connects to any of the computer's I/O slots. The central data unit is attached to the interface card's 3 metre cable. Up to two disc controllers can be connected to the central data unit via standard HP-IB cables with a total cable length of 6 metres or less. Each disc controller is then connected to the disc drives according to its specific installation requirements.

Diagnostic Test Program

A Diagnostic Test Program is availiable on the 98041A Test Cartridge (P/N 98041-90010) for use with the System 45 Desktop Computer. This test can be used to verify the operation of the disc interface and the mass storage units in the system.

The 98041A Disc Interface Diagnostic Program Manual (P/N 98041-90031) contains the necessary information for loading and running the diagnostic test.

The diagnostic program along with the information in this chapter should help you isolate and repair failures in a 98041A mass storage system.

System Operation Overview

The general function of the disc interface is to transfer data to and from various mass storage devices consisting of disc controllers and disc drives. The disc interface converts the computer's mass storage instructions into HP-IB disc controller commands. Additionally, the interface converts the computer's 16-bit data into two 8-bit bytes that are useable by the discs and also compensates for the input/output speed differences between the computer and the disc controllers.

A block diagram of the disc interface is on page . Unfold the diagram for reference as you read this section. Following the block diagram is an operational explanation of the various components of the disc interface. Complete schematic diagrams, component locators and replaceable parts lists are given for each assembly. A glossary of signal abbreviations is included with the schematics.

Interface Logic Levels

The Disc Interface uses TTL logic levels. Throughout this manual, all logic levels and signal levels will be referred to as either **"high"** ($\geq$ 2V) or **'low'** ($\leq$ 0.8V)

Theory of the Interface Card Operation

The interface card contains two printed circuit assemblies: the A1 I/O Control Board and the A2 Data Logic Board. These assemblies consist of driver, receiver and terminator components for the 16 data lines, 5 status lines and 6 control lines as well as part of the I/O control logic.

The A1 I/O Control Board

The I/O control board assembly (P/N 98041-66501) contains the drivers for the 6 control lines. These lines and their functions are defined as follows.

The $\overline{\text{IC1}}$ and $\overline{\text{IC2}}$ lines from the computer's I/O control specify the type of I/O operation that is to be executed. The following table shows the line level for each operation –

$\overline{\text{IC2}}$	$\overline{\text{IC1}}$	Operation
high	high	DMA Data transfer
low	high	DMA Data transfer last word.
low	low	Non-DMA data transfer
high	low	Input status information or send control information.

The $\overline{\text{INIT}}$ line specifies that the computer has just been switched on or has been reset. This line leaves the A1 board as the $\overline{\text{GINIT}}$ line.

The **$\overline{\text{IOSB}}$** line carries the handshake strobe pulse from the computer I/O control. The strobe driver is enabled only if the select code on lines PA0 thru PA3 specify a value that is the same as the value set on the select code switch (S1). This line leaves the A1 board as the $\overline{\text{GQIOSB}}$ line.

The **$\overline{\text{DOUT}}$** line specifies the transfer direction for the operation being executed by the computer (either input or output). The $\overline{\text{DOUT}}$ driver is enabled only when the select code value on lines PA0 thru PA3 is the same as the value set on the select code switch (S1). The $\overline{\text{DOUT}}$ line leaves the A1 board as the GQDOUT line.

The **$\overline{\text{INT}}$** line causes the I/O card to respond to an interrupt poll performed by the computer's I/O control.

The A1 board also contains the select code decoding logic and the poll response decoding logic.

The A2 Data Logic Board

The Data Logic assembly (P/N 98041-66502) contains the drivers and receivers for the 16 data lines and the receivers for the 5 disc interface status lines. The status lines are defined as follows.

The **$\overline{\text{GIRQ}}$** line sends an interrupt request signal from the central data unit to the computer I/O control as either a low priority interrupt $\overline{\text{IRL}}$ (for select code settings of 2 thru 7) or a high priority interrupt $\overline{\text{IRH}}$ (for select code settings of 8 thru 12). The $\overline{\text{GIRQ}}$ line also enables the poll response logic to respond to a poll operation conducted by the computer's I/O control.

The $\overline{\text{GDMAR}}$ line is used by the central data unit to request a DMA operation from the computer.

The $\overline{\text{GSTS}}$ line specifies whether or not the central data unit is powered on and whether or not a DMA transfer is enabled.

The **$\overline{\text{GFLG}}$** line carries the central data unit's part of the non-DMA transfer handshake in response to the $\overline{\text{GQIOSB}}$ pulse from the computer I/O control.

The **$\overline{\text{GPOP}}$** line indicates that either the central data unit has just powered up (via the $\overline{\text{GPOPP}}$ line from the disc interface power supply) or the computer has just been powered up or reset (via the $\overline{\text{GINIT}}$ line from the computer).

Theory of the Central Data Unit Operation

The central data unit contains four printed circuit assemblies: the A3 Support Board, the A4 HP-IB Board, the A5 HP-IB Connector Board and the A6 Power Supply Board.

The A3 Support Board

The support board assembly (P/N 98041-66504) contains the components that complement the signal lines coming from or going to the A1 and A2 boards. These components include receivers and terminators for the 6 control lines, drivers for the 5 status lines, and transceivers and terminators for the 16 bidirectional data lines. This board also receives the +5 Volt, +12 Volt and ground lines from the A6 power supply assembly. All of the lines are then connected to the A4 HP-IB board.

The A4 HP-IB Board

The HP-IB board assembly (P/N 98041-66507) contains the circuits necessary to convert the computer's strobed, 16-bit data words into two 8-bit data bytes. This data is transfered into the PHI chip (A4 U1) using a two wire type handshake with the computer. The PHI chip also transfers the data bytes to and from the selected mass storage controller units using the HP-IB disc controller commands and the HP-IB three wire handshake.

The basic hardware components of the HP-IB board are as follows –

- I/O Registers
- PHI Chip
- Sixteen Byte FIFO Buffer
- PHI Access Control State Machine
- Byte Packing Control State Machine
- FIFO Fullness Counter
- DMA Request Logic
- Interrupt Request Logic
- HP-IB Transceivers

The I/O Registers

There are two types of I/O registers on the HP-IB board: the bidirectional 16-bit data registers and the 6-bit instruction register.

The data registers consist of four 4-bit latches. These latches make the computer's 16-bit data structure compatible with the HP-IB discs' 8-bit data structure. These registers can be clocked to transfer each 16-bit word from the computer as two 8-bit bytes useable by the disc drives or to combine two 8-bit bytes from a disc into a 16-bit word usable by the computer.

The instruction register is a 6-bit latch that accepts instructions from the computer on data lines $\overline{\text{IOD 0}}$ thru $\overline{\text{IOD 5}}$ when the $\overline{\text{IC1}}$ and $\overline{\text{IC2}}$ lines select an instruction operation. Three bits of the data ($\overline{\text{IOD 5}}$ thru $\overline{\text{IOD 3}}$) form the PHI chip register address and three bits ($\overline{\text{IOD 2}}$ thru $\overline{\text{IOD 0}}$) specify the type of operation to be performed. The bit values for the PHI chip register address and the operation codes are shown next.

Register No.	$\overline{\text{DIO 5}}$	$\overline{\text{DIO 4}}$	$\overline{\text{DIO 3}}$
Reg 0 –	low	low	low
Reg 1 –	low	low	high
Reg 2 –	low	high	low
Reg 3 –	low	high	high
Reg 4 –	high	low	low
Reg 5 –	high	low	high
Reg 6 –	high	high	low
Reg 7 –	high	high	high

$\overline{\text{DIO 3}}$	$\overline{\text{DIO 1}}$	$\overline{\text{DIO 0}}$	Type of Operation
high	high	high	Non-DMA write to specified PHI Register
high	high	low	Non-DMA read from specified PHI Register
high	low	high	Don't Care
high	low	low	Reset
low	high	high	DMA Output – Computer memory to disc controller/drive
low	high	low	DMA input – disc controller/drive to computer memory
low	low	high	Don't Care
low	low	low	No-op

The PHI Chip

The PHI chip (A4 U1) controls the bi-directional tri-state transceivers which send and receive information at speeds compatible with HP-IB disc controllers and drives. The PHI chip sends disc addresses and commands according to the HP-IB disc-controller command protocol. This protocol is a valid implementation of the IEEE Std. 488-1975 but makes special use of some "don't care" states in certain HP-IB messages. This control protocol also utilizes certain secondary address characters as commands that are used to select various disc controller operations.

Refer to Supplement A to this manual for a list of the HP disc controllers that utilize the HP-IB disc controller protocol.

The PHI is structured on the computer side of the interface as a group of eight 10-bit registers, with various control lines to the Control State Machines and a two wire handshake.

The 3-bit address from the instruction register is used to select the specific PHI register for the operation to be performed. The registers are defined as follows:

Register 0: Contains the values of 9 status conditions that are capable of interrupting the computer's I/O. These values are masked by the values in Register 1. If any of the nine status conditions are masked and true, the 10th bit of the register is set true which enables the interrupt request logic.

Register 1: Contains the mask values for the 9 interrupt status conditions in register 0. A true value of 1 for a bit, unmasks or selects the corresponding bit in register 0 as being capable of initiating an interrupt request.

Register 2: Used to transfer data to or from the HP-IB side of the system. It is structured as two 8 byte FIFO buffers; an inbound FIFO and an outbound FIFO.

Register 3: Contains the values of the non-interrupting status conditions.

Register 4: Contains the 8 control bits used to set up operational conditions within the PHI chip.

Register 5: Contains the HP-IB address of the PHI chip.

Register 6: Masks the 8 incoming responses to a parallel poll operation conducted by the disc interface to detect service requests from mass storage units in the system.

Register 7: Normalizes the 8 incoming parallel poll responses from the mass storage units in the system.

NOTE

The data transfers and programming cycles discussed in this section are generated by the computer as a result of the execution of appropriate Mass Storage ROM statements.

Non-DMA I/O Transfers

The non-DMA I/O operations are used to transfer mask, command and status bytes to and from the PHI registers. Each of these operations requires two computer I/O cycles: one cycle to send the PHI register number and the operation code to the instruction latch and one cycle to transfer the data byte to or from the addressed PHI register.

Typical uses of non-DMA data transfers are sending HP-IB addresses or commands, programming the interrupt mask, obtaining interface status, setting PHI chip control bits, setting up DMA data transfers, and obtaining a parallel poll response.

DMA I/O Transfers

High speed data transfers to and from mass storage devices take place under computer DMA control. The disc interface must be programmed before the DMA transfer occurs. This programming process requires three computer I/O cycles. The first cycle specifies a write operation to PHI register 4. The next cycle sends the proper bit pattern to register 4 to set the DMA FIFO select bit which enables the DMAR line out of the PHI chip. The third I/O cycle specifies either a DMA input or output operation and selects PHI register 2 to transfer the data.

Once these cycles have programmed the interface, the DMA data transfer takes place.

The FIFO Buffer

The FIFO (First-In, First-Out) buffer is used only when a DMA data transfer takes place. This buffer is by passed during all non-DMA operations.

The FIFO transfers data in 8-bit bytes, to and from register 2 of the PHI chip and the I/O data registers. It can hold up to sixteen bytes.

Sixteen bit data is transferred to and from the I/O data registers and the FIFO in two 8-bit bytes, with the most significant byte ($\overline{\text{IOD8}}$ thru $\overline{\text{IOD15}}$) transfered first followed by the least significant byte ($\overline{\text{IOD0}}$ thru $\overline{\text{IOD7}}$). The FIFO buffer can hold up to sixteen bytes of data to allow for speed variations that may occur between the computer's DMA transfer rate and the data transfer rate of the disc controller.

The PHI Access Control

This circuit provides the control signals for all data transfers between the PHI chip and either the FIFO buffer or the I/O latches. The PHI access control is programmed by data from the instruction latch/decoder that specifies the type of transfer to be performed and the PHI register to be used for the transfer.

Using the timing signal from the interface clock circuit, the PHI access control provides the handshake signals necessary to transfer data between the FIFO buffer and the PHI chip for DMA transfers and between the I/O latches and the PHI chip for non-DMA transfers.

The Byte Packing Control

This circuit controls the packing of bytes into words and the unpacking of words into bytes between the I/O latches and the FIFO buffer during DMA operations. It also controls the DMA request logic. The byte packing control receives its control signals from the PHI access control and the FIFO fullness counter.

A more detailed description of the operation of the PHI Access and the Byte Packing Control machines as well as a state diagram is provided on page 21.

The FIFO Fullness Counter
and
The DMA Request Logic

The fullness of the FIFO buffer is monitored by the FIFO fullness counter. This circuit monitors both the PHI access control and the byte packing control to prevent either an overflow or underflow of data during DMA transfers.

During DMA output transfers, the fullness counter prevents data overflow in the FIFO buffer by signalling the byte packing control whenever the FIFO buffer is close to being full. The byte packing control then causes the DMA request logic to halt the computer DMA output until the FIFO has room for more data.

During DMA input transfers, the fullness counter prevents data underflow in the FIFO buffer by signalling the byte packing control whenever the FIFO buffer is close to being empty. The byte packing control then causes the DMA request logic to halt the computer's DMA input until the FIFO contains more data.

The Interrupt Request Logic

The interrupt request logic monitors the interrupt line of the PHI chip to determine when the PHI chip requests an interrupt. When a DMA transfer is complete (indicated by $\overline{IC1}$ high and $\overline{IC2}$ low), this circuit asserts the interrupt line ($\overline{INT}$). When PHI register 0 is read by the computer, the logic clears the interrupt line.

The HP-IB Transceivers

These high speed transceivers are capable of transferring data to and from the PHI chip and the HP-IB disc controllers at a rate of up to 1M bytes/sec.

The A5 HP-IB Connector Board

The HP-IB connector board assembly (P/N 98041-66505) connects the transceivers on the HP-IB board to the standard HP-IB connector on the central data unit's back panel.

The A6 Power Supply Board

The power supply board (P/N 98041-66503) provides +5 volts at a maximum current of 5 amps, +12 volts at a maximum current of 1 amp and the power on signal to the A3 and A4 boards. The computer provides the power for the A1 and A2 boards.

+5 Volt Supply

The +5 volt supply is a series-pass voltage regulator with current limiting and current foldback. The diode bridge (CR2, CR6, CR7, CR8) and filter capacitor (C1) develop raw +10 (nominal) volts from the power transformer. Q1 is the pass element for the +5 volt supply. The base of Q1 is controlled by the drive transistor (pins 6 and 7) in U1, which supplies Q1 with a regulated drive. This internal drive transistor is controlled by a differential amplifier in U1. The differential amplifer compares the output voltage on the +5S line with a reference voltage. The reference voltage is obtained from U1 pin 4 and may be adjusted with R17.

R11 is in the voltage sense circuit to allow the A6 board to operate when disconnected from the rest of the system (e.g., in a test fixture) by providing a feed back path to the differential amplifier. R11 is shorted out when the pc board is connected in the system.

R1 and one of the internal transistors (pins 1 and 10) of U1 form the current limiter for the +5 volt supply. If the current through R1 becomes greater than 5 amps, the internal transistor turns on due to the voltage differential across its base-emitter junction. This sinks base current away from the internal drive transistor reducing the base current supplied to the pass transistor, Q1, thus reducing the output voltage and limiting the current. C2 prevents the current limiting circuit from oscillating.

A6Q5, R7 and R8 form the current foldback portion of the regulator. If the output current should become excessive (e.g., a short circuit on the +5 volt line) a large voltage differential becomes present between the base of Q1 and the emitter of Q5. This draws current away from the base of the internal drive transistor in a manner similar to the current limiting circuit. Since the current foldback occurs after current limiting takes effect, the Q1 base drive is reduced even more. This causes a reduction of the output voltage beyond that caused by the current limiter alone. The effect is to reduce greatly both the output current and the output voltage. Under short circuit load condition, the output current is 800mA.

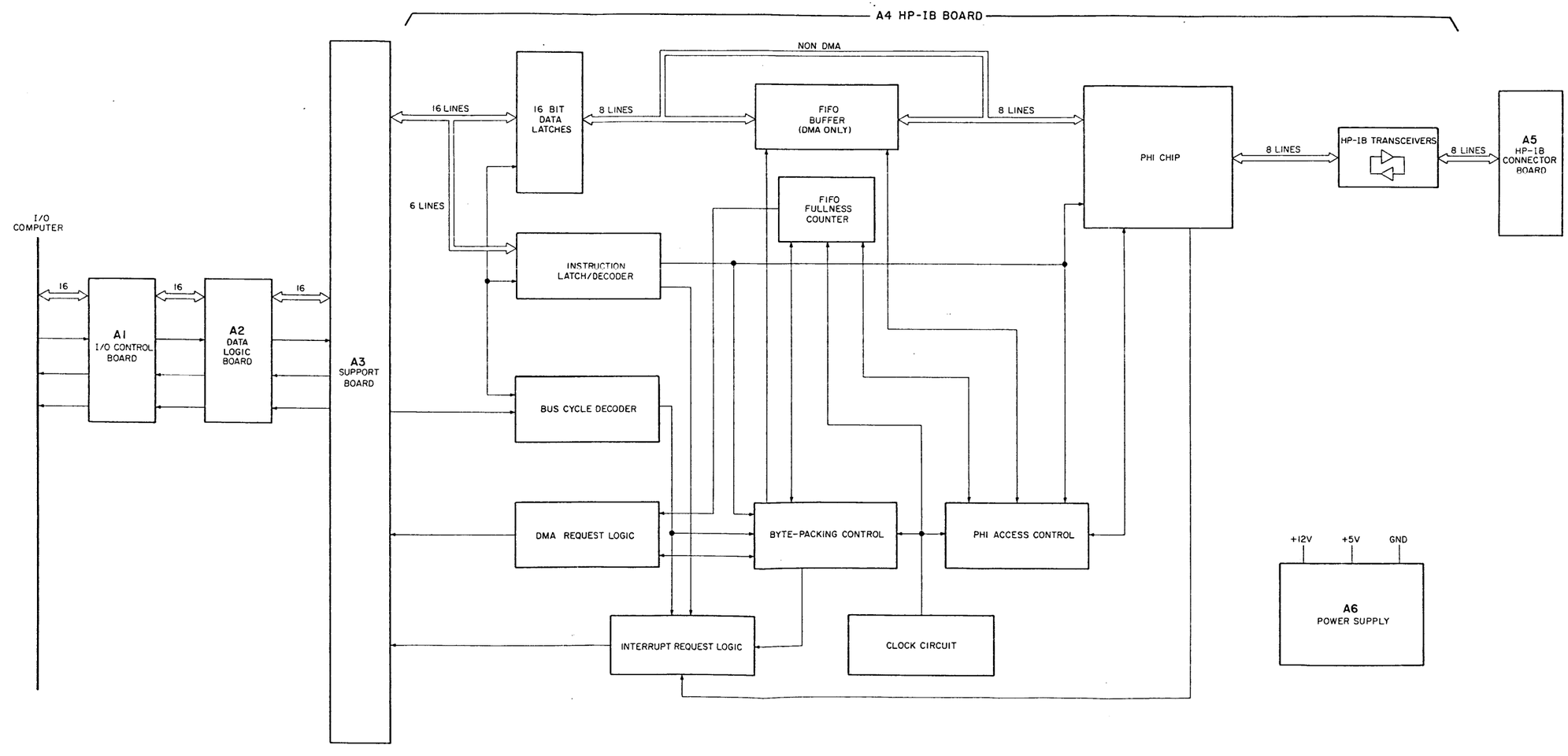
If the pass transistor (Q1) shorts out, the output voltage of the +5 volt supply could become excessive. To prevent the destruction of the TTL components, a crowbar circuit is provided to short the +5 volt supply to ground. If the output voltage exceeds 5.6 volts, the thyristor (Q2) conducts, clamping the output voltage to .8 volts. This can be reset only by switching the unit's power off and then on again.

+12 Volt Supply

CR5 and C10 provide the unregulated voltage for the +12 volt supply. U2 is a self-contained 12 volt regulator which provides current limiting at 1 amp and thermal overload protection for this supply. This supply powers the PHI chip on the A4 board.

The Power-On Signal

The $\overline{\text{GPOPP}}$ signal specifies whether or not both the +5 volt and +12 volt supplies are operating at their rated voltages. The +5 volt and +12 volt monitoring circuits will activate the $\overline{\text{GPOPP}}$ signal whenever the +5 supply falls below 4.7 volts or whenever the +12 supply falls below 11.4 volts. This is accomplished by pulling the respective zener diodes, CR3 or CR4, out of the reverse breakdown region and into the off region. This causes the appropriate transistor, Q3 or Q6, to turn off, thus causing the respective output transistor, Q4 or Q7, to turn on which makes $\overline{\text{GPOPP}}$ low. The $\overline{\text{GPOPP}}$ signal along with the $\overline{\text{GINIT}}$ signal are used to inform the computer (via $\overline{\text{POP}}$ and the $\overline{\text{ONLINE}}$ flip-flop on A1) whenever the PHI chip receives a "power on reset" or whenever the disc interface is first powered on or the computer is powered on or reset.



Disc Interface Block Diagram

Sequential Operation Description

The following descriptions detail the sequential operation of the various HP-IB circuits during both non-DMA and DMA output and input operations.

Non-DMA Output Operation

A instruction I/O cycle ($\overline{IC1}$ = low; $\overline{IC2}$ = high) is carried out with the following bit pattern being latched into the instruction register:

$\overline{IOD5}$	$\overline{IOD4}$	$\overline{IOD3}$	$\overline{IOD2}$	$\overline{IOD1}$	$\overline{IOD0}$
PHI register			high	high	high

This sets $\overline{WPHI}$ true which opens the data path from the I/O data latches to the PHI chip, and also sets $\overline{PAC}$ true and advances the PHI access control to state 02. The $\overline{IOD0}$ bit set to 1 indicates a write operation, (i.e. data transfer from the calculator memory to the disc drive via the disc interface). Thus, $\overline{WRITE}$ is true and the access control waits in state 36 until STBF goes true to indicate that the non-DMA I/O cycle containing the data byte has been completed. The STBF qualifier is the output of a D flip-flop which is clocked on the trailing edge of the IOSB pulse which results from the non-DMA I/O cycle.

The PHI access control is now certain that the data is contained in the I/O latches and the data path to the PHI chip is enabled. Now, the handshake of the data into the PHI chip can be carried out. Bits 5, 4 and 3 of the instruction latch contain the coding for the PHI register address. The handshake of the data into the PHI consists of the PHI access control first asserting $\overline{IOGO}$ to indicate to the PHI chip that the data is ready and then waiting for the PHI to respond with $\overline{IOEND}$ to indicate that the data has been accepted. With this handshake complete, $\overline{CPAC}$ is asserted to reset the instruction register to the NO-OP state. The PHI access control then returns to state 00 to await the next operation.

Non-DMA Input Operation

An instruction I/O cycle ($\overline{IC1}$ = low; $\overline{IC2}$ = high) is carried out with the following bit pattern being latched into the instruction register:

$\overline{IOD5}$	$\overline{IOD4}$	$\overline{IOD3}$	$\overline{IOD2}$	$\overline{IOD1}$	$\overline{IOD0}$
PHI register			high	high	low

This bit pattern is decoded by the instruction decoder to set $\overline{\text{RPHI}}$ true which enables the data path from the PHI chip to the I/O data latches and also sets $\overline{\text{PAC}}$ true. Since $\overline{\text{IOD0}}$ is low, $\overline{\text{WRITE}}$ will be false and thus state 32 is reached. The data must now be transferred from the PHI chip into the I/O data latches. The PHI access control handshakes with the PHI to pass the data into the I/O latches. These latches are clocked on the trailing edge of $\overline{\text{LOAD}}$ which occurs only after the PHI assertes $\overline{\text{IOEND}}$ indicating that the data is valid on its output lines. The PHI access control then waits in state 26 for the computer I/O cycle which reads the data from the I/O latches via a non-DMA input. When this occurs $\overline{\text{STBF}}$ goes true and the instruction latch is cleared by $\overline{\text{CPAC}}$ and the PHI access control reset to handle the next operation.

Computer DMA Output Operation

This description is for a data transferred from the computer's memory to a disc controller and drive.

The data transfer is preceeded by three computer I/O cycles.

- An instruction cycle ($\overline{\text{IC1}}$ = low; $\overline{\text{IC2}}$ = high) that loads the following bits into the instruction latch:

$\overline{\text{IOD5}}$	$\overline{\text{IOD4}}$	$\overline{\text{IOD3}}$	$\overline{\text{IOD2}}$	$\overline{\text{IOD1}}$	$\overline{\text{IOD0}}$
high	low	low	high	high	high
PHI Register 4			write to PHI register		

- A non-DMA data transfer ($\overline{\text{IC1}}$ = low; $\overline{\text{IC2}}$ = low) programs the appropriate control bit in PHI register 4 to specify that the direction of the transfer is to be from computer memory to the disc controller/drive (IOD1 set to low).

- An instruction cycle ($\overline{\text{IC1}}$ = low; $\overline{\text{IC2}}$ = high) then loads the following bits into the instruction latch:

$\overline{\text{IOD5}}$	$\overline{\text{IOD4}}$	$\overline{\text{IOD3}}$	$\overline{\text{IOD2}}$	$\overline{\text{IOD1}}$	$\overline{\text{IOD0}}$
low	high	low	low	high	high
PHI register 2			DMA output operation		

The PHI register 2 is selected because all DMA cycles travel through that particular register due to its unique FIFO structure. In addition to this FIFO within the PHI chip itself, there is the sixteen by 8-bit FIFO circuitry on the HP-IB board. These two FIFO's provide buffering between the data rates of the various disc drives and the fixed data rate of the computer's IOC during DMA transfers.

The instruction register bits are decoded to set up the data path through the FIFO and to point to PHI register 2. The DMA qualifier is true and the PHI access control waits in state 05 until the FIFO indicates that it has received a data byte from the I/O latches, by setting $\overline{\text{ORE}}$ low. Now, the data byte can be transferred out of the FIFO by clocking the transfer out line of the FIFO chip with $\overline{\text{TOPF}}$ and simultaneously handshaking with the PHI chip by issuing the $\overline{\text{IOGO}}$ signal. The PHI's DMA Request line is also used to inhibit each handshake until the PHI is ready to accept the byte of data.

The tasks performed by the byte packing control during a DMA transfer from the calculator memory to the disc drive are:

1) Unpack the 16 bit word into two eight bit bytes
2) Clock the data from the I/O data latches into the FIFO buffer
3) Turn the DMA request on and off as determined by the FIFO fullness counter.

The $\overline{\text{STRD}}$ (Start Read) qualifier allows the DMA request to be turned on as soon as there is one word of room available in the FIFO buffer. The byte packing control then waits for the I/O cycle to be completed and opens the data path to transfer the high order 8-bits into the FIFO and then the low order 8-bits. In this fashion, the 16-bit word is separated into two 8-bit bytes and stacked into the FIFO buffer.

The packing control checks the qualifier $\overline{\text{LW}}$ (Last Word) to determine if the computer has completed the entire DMA transfer as indicated by a DMA cycle with the $\overline{\text{IC1}}$ (high) and $\overline{\text{IC2}}$ (low) control lines specifying the last word of a transfer. If not, the packing control must then decide if there is room in the FIFO for another word or if DMA should be turned off to allow the slower transfer rate of the disc drive to catch up. The packing control will stay in the fast loop (states 36 to 25) as long as there are less than six words in the FIFO and in the longer loop of states 10 to 37 if there are greater than or equal to six words in the buffer.

The DMA output operation is turned on whenever there is room for one word (two bytes) in the FIFO. If the packing control is in the slow loop, the DMA will be turned off after this single word transfer. If the packing control is in the fast loop, DMA turn off is initiated when there are only two words of room available since the hardware in this case is not be able to turn off DMA without allowing at least one more computer I/O cycle to occur.

The byte packing control notifies the PHI access control that it has loaded the last byte into the FIFO by generating the signal $\overline{\text{LWIN}}$.

When the last word has been loaded into the FIFO the packing control waits in state 26 for the PHI access control to complete its mission of transferring the data out of the FIFO and into the PHI chip. The $\overline{\text{DMARIP}}$ (DMA Read-In-Progress) signal generated by the PHI access control is the qualifier which implements this intramachine handshake.

When all the bytes are in the PHI chip, the hardware then requests an interrupt to notify the calculator of the completion of the DMA at the interface. The packing control then waits in state 12 for the driver to clear the interrupt by reading PHI register zero which is the interrupt register. The $\overline{\text{CLDF}}$ signal resets the last word latch and the $\overline{\text{LBT}}$ flip flop and the computer DMA output is completed.

Computer DMA Input Operation

This sequence of events is followed for a DMA data transfer from a disc controller/drive to the computer's memory.

The DMA data transfer is preceeded by three computer I/O cycles that set up the interface for the transfer.

- An instruction I/O cycle ($\overline{\text{IC1}}$ = low; $\overline{\text{IC2}}$ = high) loads the bits into the instruction register that specify a non-DMA transfer to PHI register 4.

$\overline{\text{IOD5}}$	$\overline{\text{IOD4}}$	$\overline{\text{IOD3}}$	$\overline{\text{IOD2}}$	$\overline{\text{IOD1}}$	$\overline{\text{IOD0}}$
high	low	low	high	high	high
PHI Register 4			Non-DMA write		

- A non-DMA data transfer ($\overline{\text{IC1}}$ = low; $\overline{\text{IC2}}$ = high) then programs the appropriate control bits into PHI register 4 that specifies that the direction of the data transfer is to be from the disc controller/drive to the computer's memory ($\overline{\text{IOD1}}$ set high).
- An instruction cycle ($\overline{\text{IC1}}$ = low; $\overline{\text{IC2}}$ = high) that loads the bits into the instruction register to select PHI register 2 for a DMA input data transfer from the disc controller/drive to the computer's memory.

$\overline{\text{IOD5}}$	$\overline{\text{IOD4}}$	$\overline{\text{IOD3}}$	$\overline{\text{IOD2}}$	$\overline{\text{IOD1}}$	$\overline{\text{IOD0}}$
low	high	low	low	high	low
PHI Register 2			DMA Input Operation		

During a DMA input to the calculator memory, the byte packing control is opening the data path between the data latches and FIFO, and is responsible for packing the bytes in the FIFO buffer into words in the data latches. It also requests sufficient DMA cycles to enable the computer to achieve the data transfer rate of the disc drive.

The $\overline{\text{STWR}}$ (Start Write) qualifier goes low when five bytes have been loaded into the FIFO by the PHI access control and this automatically sets the DMA request line ($\overline{\text{DMAR}}$) low. The FIFO is given the $\overline{\text{TOP}}$ signal (Transfer Out Parallel) and the data byte is clocked into the high order byte of the data latches. Next, the low order byte is loaded and the packing control waits in state 22 for the I/O cycle to occur which will transfer the data word into the computer.

If the number of bytes in the FIFO is now less than five the DMA shuts off and the packing control waits in state 01 for more data to be loaded into the FIFO. If there are still five or more bytes available, the access control waits for the present I/O cycle to complete and then returns to the five-state high speed loop from state 03 to state 02.

There are two mechanisms for termination of a DMA input operation. The normal sequence of events is that the computer IOC takes the last DMA byte with $\overline{IC1}$ = high and $\overline{IC2}$ = low. The interface hardware senses this and sets $\overline{LW}$ (Last Word) high which causes the access control to stop the high speed data transfer and request an interrupt from the computer. The second mechanism for DMA input termination is when the transfer must be terminated before the expected number of bytes have been transferred. This is the case when errors have been detected on the HP-IB, the disc controller or the disc drive. The HP-IB indicates this condition by tagging the last data byte with EOI. That bit sets the $\overline{END}$ latch and $\overline{END}$, which in turn forces $\overline{STWR}$ to be low. This allows the last four bytes of data to be clocked out of the FIFO buffer. When the last byte is placed into the data latch, the qualifier $\overline{MT}$ (empty) becomes low indicating that no more bytes are in the FIFO. Then the access control stops data transfer and begins to request an interrupt signaling the end of the DMA input.

Additional Theory of Operation

The PHI Access and Byte Packing Control State Machines

The PHI access control and byte packing control machines are ROM-based, state oriented logic circuits which receive input signals called qualifiers from the other HP-IB board circuits and generate control signals called outputs. This structure is depicted in Figure 3-1.

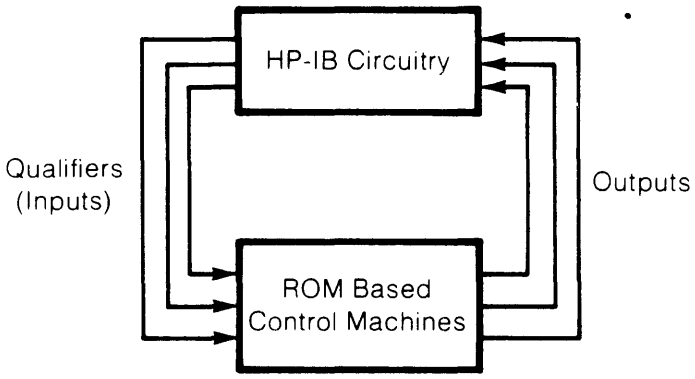


Figure 3-1: Basic Control Machine Structure

The inputs, or qualifiers, give the control machines information about the present state of the hardware.

The control machines decide what action should be taken and then what outputs should be given to stimulate the hardware to perform the necessary task.

The controllers are designed to make decisions by programming the bit patterns stored in ROMs. Two bits of the present state and three alternate/direct bits determine the five bit ROM address. The alternate/direct bits are also stored in ROM but are selected based on the status of the input qualifiers. Thus, the ROM address is determined by the present state and the input qualifiers. The state of the ROM is updated on the leading edge of a six megahertz clock signal called CK1. That is, new states or new addresses become valid and a ROM memory location is accessed on CK1.

The ROM output words contain four parts: 1). Four bits are used to select the appropriate input qualifier to be used in determining three bits of the next state. Three of these four select bits are also used as the alternate address bits; 2). Seven (PHI acess) or ten (byte packer) bits are used as outputs; 3). Three bits are used as the direct address; 4). Two bits are used as next state bits. These outputs become valid on the leading edge of a six megahertz clock signal called CK2. The CK2 signal is essentially an inverted CK1 signal.

The structure of the controller circuitry used to implement this scheme is depicted in Figure 3-2.

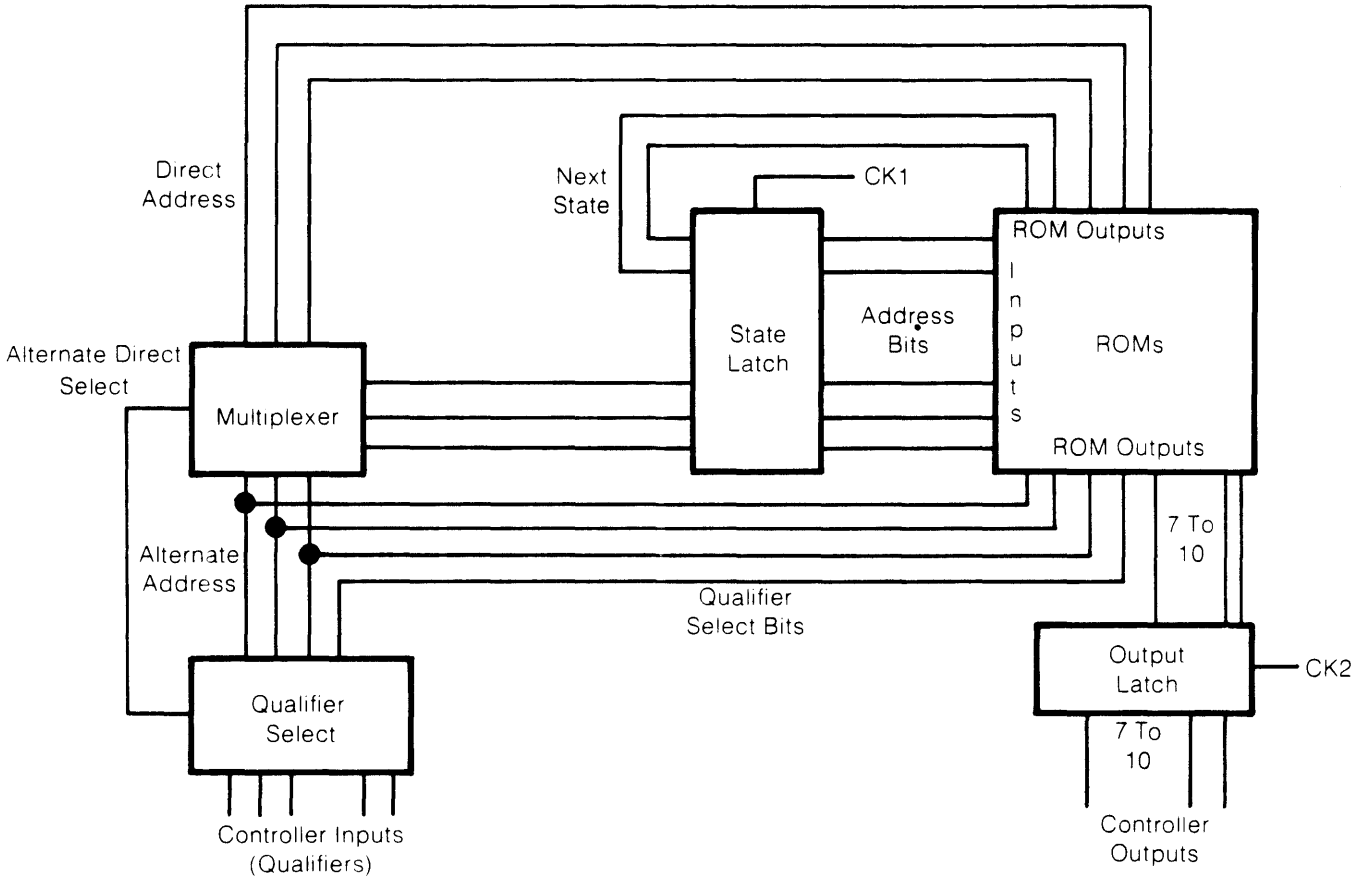
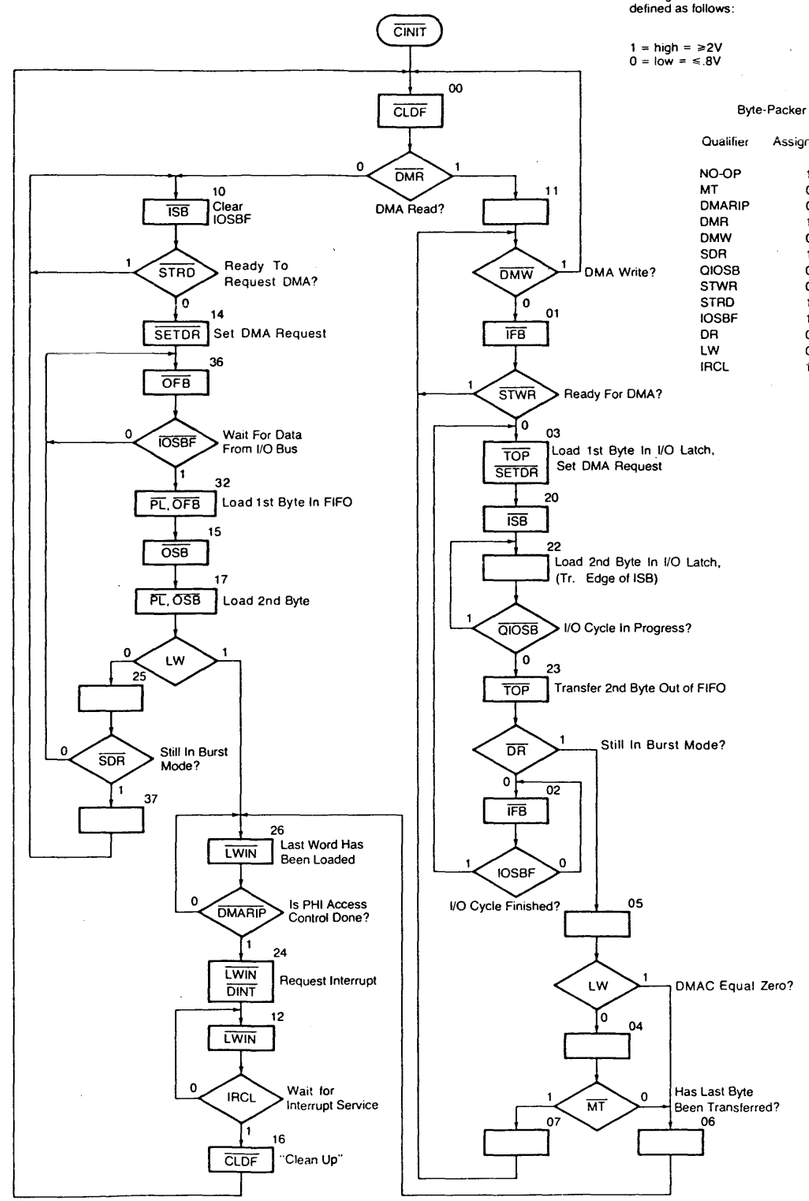


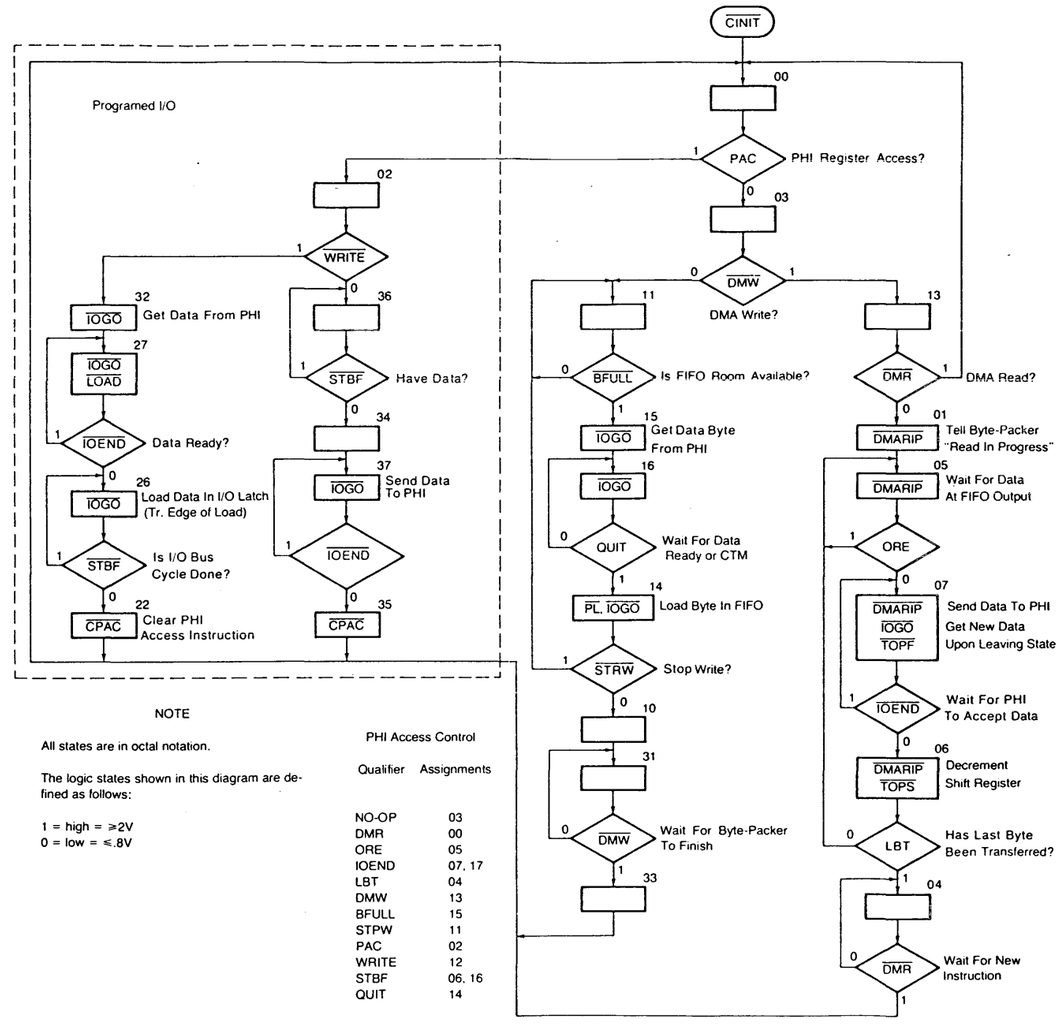
Figure 3-2: Structure of the Controller Circuitry

Decisions are executed in the state machines by selecting either the alternate or the direct address as the next state. Whether the direct or alternate address is selected is determined by the state of the ALTERNATE/DIRECT SELECT pin on the multiplexer. A logic one level selects the direct address and logic zero level selects the alternate address bits. This line is driven by the input qualifier which is selected by the four Qualifier Select Bits. Notice that three of these bits also serve as the alternate address bits. Thus, in the present state, a particular qualifier is selected and its logical value controls whether the next state is the one pointed to by the direct address or the alternate address. In this manner branching is implemented in the controller algorithm.

The controller algorithm is depicted in Figure 3-3: 98041A HP-IB Interface ASM where ASM stands for Algorithmic State Machine. Each box represents a state and the signal(s) listed in each repesents the output(s) valid during that state. The triangular blocks represent decisions and the qualifier which controls the outcome of the decision is listed therein. The states are listed in octal and these states correspond to the five bit ROM address.



Byte Packing Control State Diagram



NOTE

All states are in octal notation.

The logic states shown in this diagram are defined as follows:

1 = high = ⩾2V
0 = low = ⩽.8V

PHI Access Control

Qualifier	Assignments
NO-OP	03
DMR	00
ORE	05
IOEND	07, 17
LBT	04
DMW	13
BFULL	15
STPW	11
PAC	02
WRITE	12
STBF	06, 16
QUIT	14

PHI Access Control State Diagram

Servicing the Disc Interface

Disc Interface Disassembly Procedures

The following proceedures outline steps that can be used to remove each of the assemblies in the disc interface for service.

WARNING

DISCONNECT THE AC POWER CORD BEFORE ATTEMPTING TO DISASSEMBLE THE DISC INTERFACE.

Disconnect the disc interface from both the computer and the disc controllers in the system.

Tools Required for Disassembly

The following tools are needed to disassemble the disc interface:

- Large pozi screwdriver
- Small pozi srewdriver
- Small flat blade screwdriver
- Diagonal wire cutter
- 7mm open or box end wrench
- ¼ inch open or box end wrench

A1 and A2 Assembly Access

The A1 and A2 assemblies are contained in the interface card case. Follow these steps to remove the A1 and A2 circuit boards from the case.

1. Remove only the four screws shown in photo A of Figure 3-3. Then flip the interface over and remove the four screws as shown in photo B of 3-3.
2. Pull the rear housing from the front housing and separate the two halves of the front housing case as shown in photo C of Figure 3-3. The A1 and A2 boards are held together by three connectors. Carefully separate the circuit boards by pulling them apart.

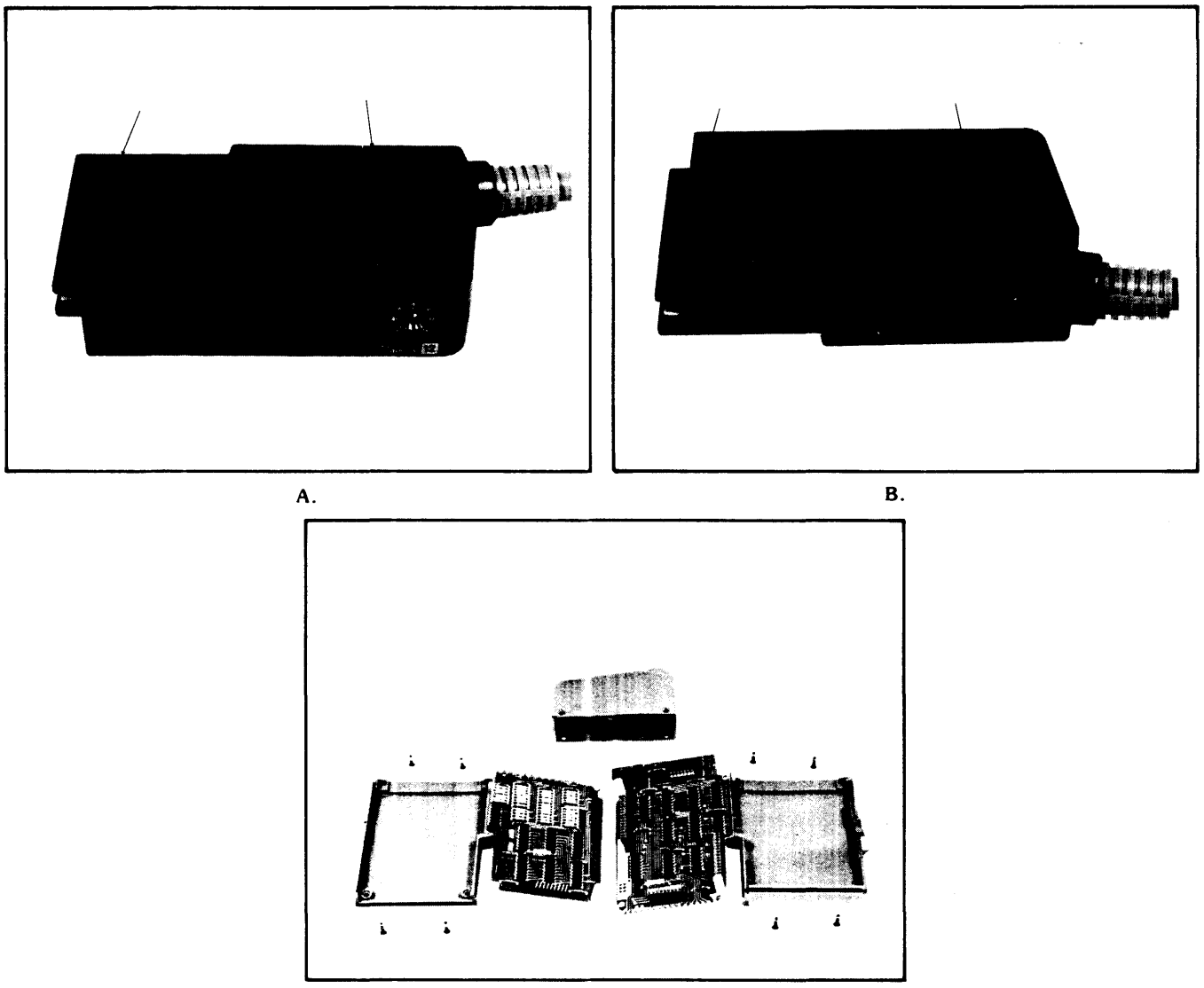


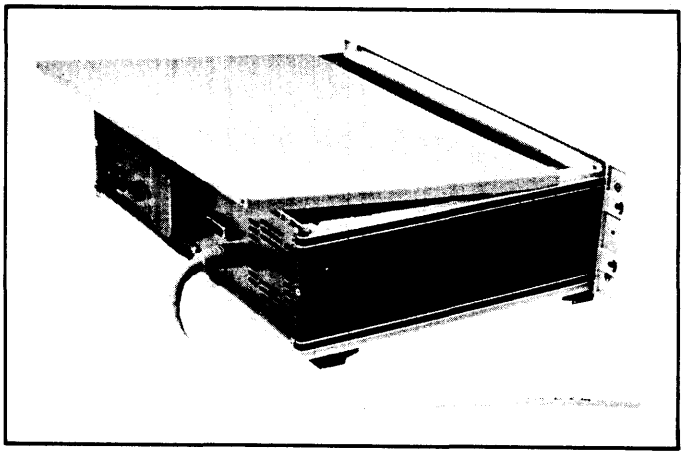
Figure 3-3: Interface Card Disassembly

A3 thru A7 Assembly Access

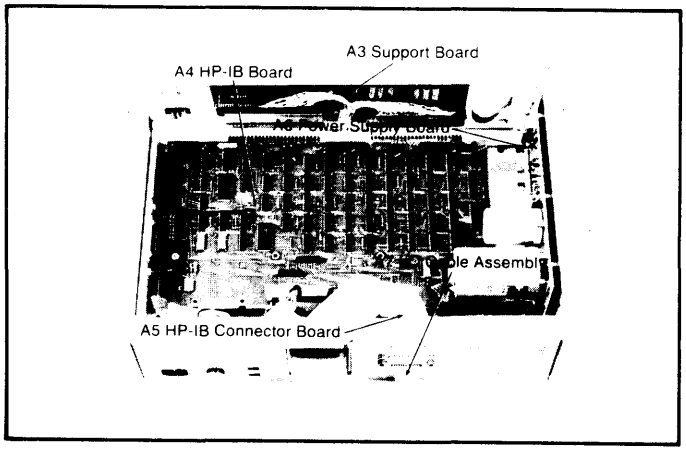
The A3 thru A7 assemblies are located in the central data unit. The following steps can be used to access these assemblies.

1. Unfasten the screw located at the rear of the top cover (photo A of Figure 3-4) with a large pozi-drive screwdriver. This screw does not come out of the cover.
2. Slide the cover to the rear of the unit and remove it as shown in photo A of Figure 3-4.

The location of the various assemblies is shown in photo B of Figure 3-4.



A. Top Cover Removal

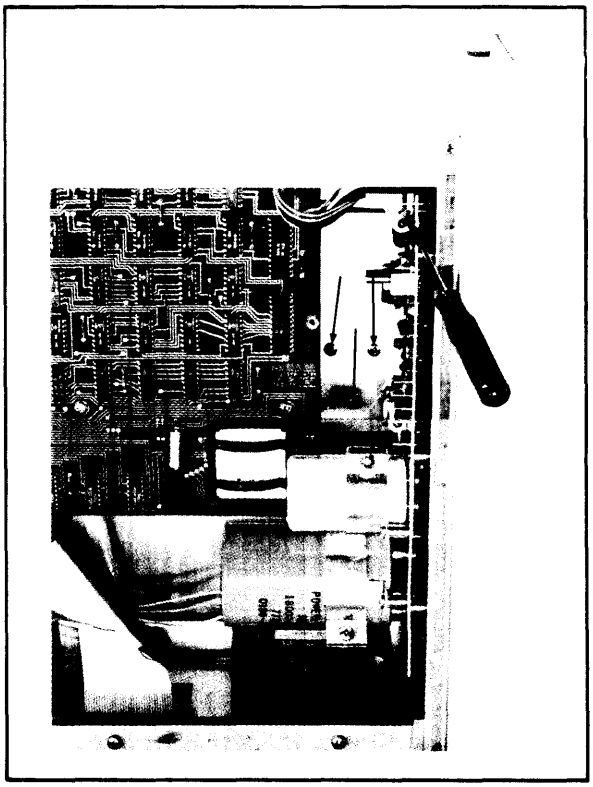


B. Assembly Locations

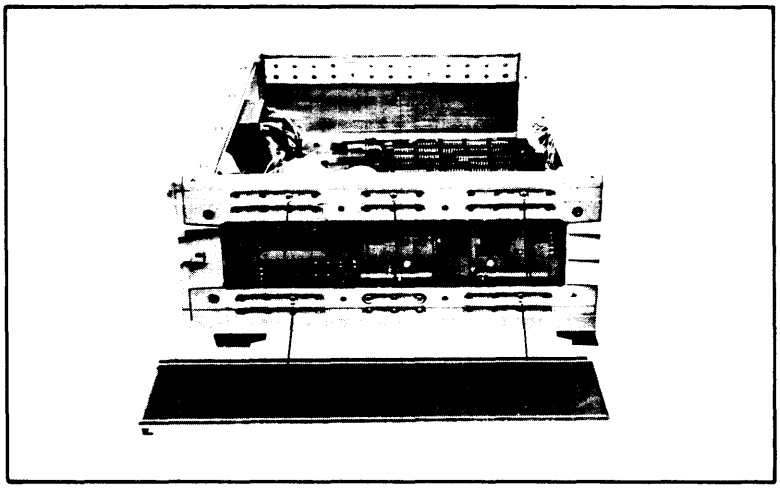
Figure 3-4: A3 thru A7 Assembly Access

NOTE

All references to right and left in the following procedures assume that you are facing the central data unit's back panel.

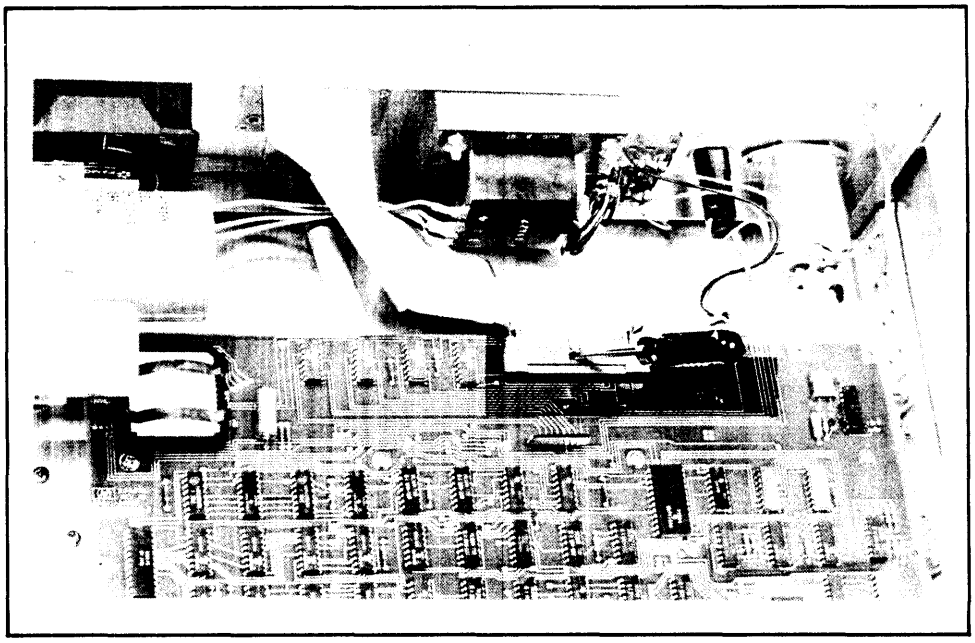


A. Removing the A6W1 cable and the location of the three heat sink mounting screws.

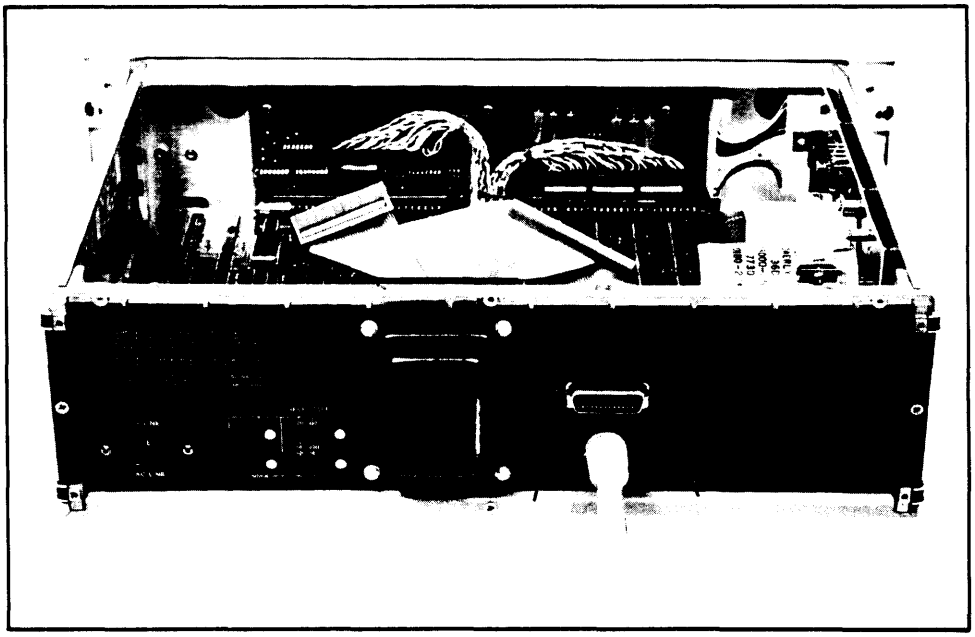


B. Removing the right side panel and the location of the five board mounting screws.

Figure 3-6: Removing the A6 Power Supply Board

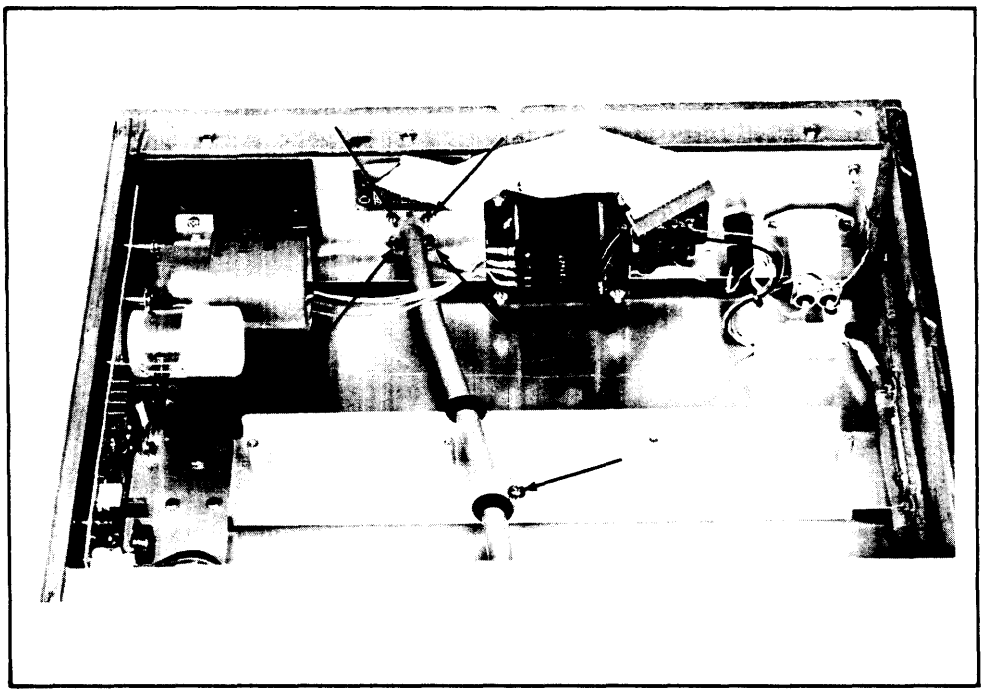


A. Unplug the ribbon cable.

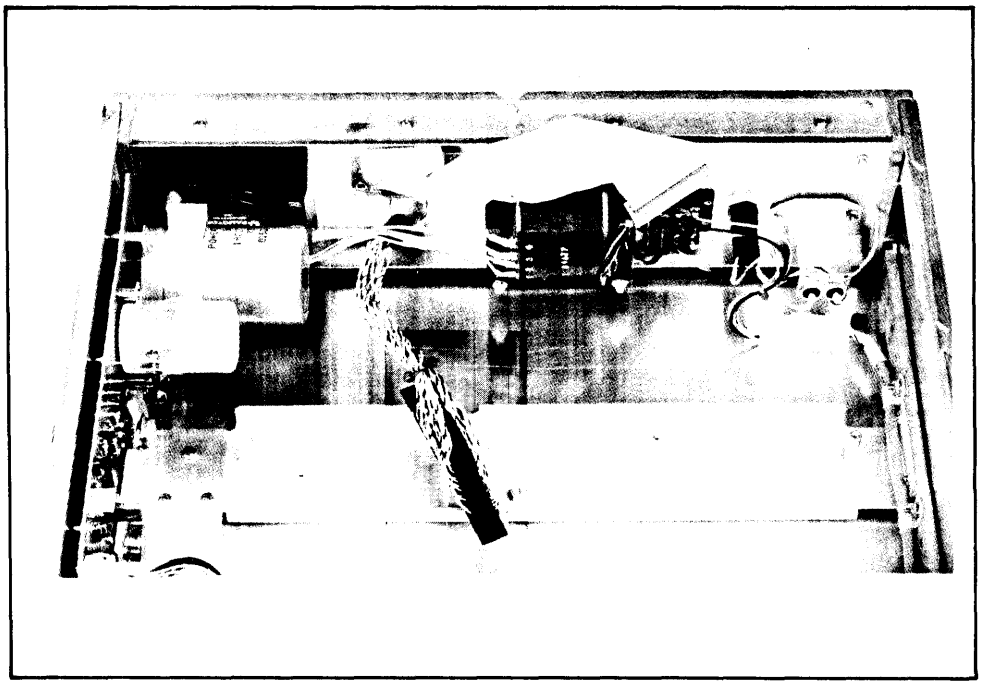


B. Remove these metric screws.

Figure 3-8: Removing the A5 HP-IB Connector Board



B. Remove these ¼ inch nuts.



C. Carefully pull the cable through the hole.

Figure 3-9: Removing the A7 I/O Cable Assembly

6. Remove the six screws from the interface and rear housing and separate the halves as shown in Figure 3-10. Remove the two screws and locknuts that attach the cable connector to the rear housing.

Adjusting the PHI Internal Timing

Whenever the PHI chip is changed, the internal timing delays must be adjusted. Potentiometer R2 on the A4 HP-IB board is used to adjust this timing delay. An oscilloscope (or some other type of test equipment that is capable of measuring a pulse width independent of frequency) is required for the adjustment.

Procedure

WARNING

This procedure requires that power be applied to the disc interface. Lethal voltages exist throught the primary circuits of the power supply. DO NOT TOUCH any of the primary circuitry.

Connect the 98041A I/O card to a System 45 computer. All cables from the mass storage controllers should be disconnected from the 98041.

Connect the oscilloscope probe to the test point marked "HSE/PUE", located near the PHI chip on the A4 board (see Figure 3-12). Connect the probe ground lead to the nearby test point marked "GROUND".

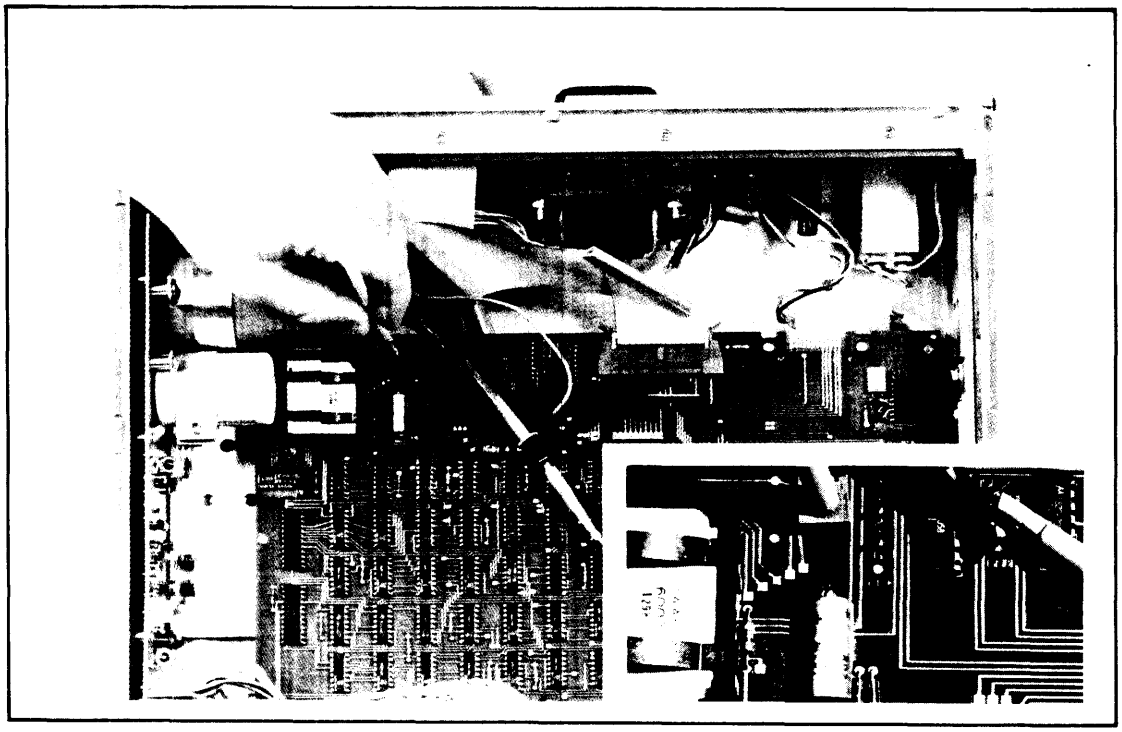


Figure 3-12: Adjusting the PHI Chip

Availiable Field Service Inventory Items

Assembly Reference	HP Part No.	Qty	Description
A1	98041-66501	1	I/O Control Board
A2	98041-66502	1	I-6)O Data Logic Board
A3	98041-66504	1	Support Board
A4	98041-66507	1	HP-IB Board
A5	98041-66505	1	HP-IB Connector Board
A6	98041-66503	1	Power Supply Board
A7	98041-61602	1	I/O Cable Assembly
A4U1	1AA6-61606	1	PHI Chip
A5W1	98041-61606	1	D.C. Power Cable
	98041-61603	1	Power Switch Assembly
	10631B	1	2 Metre HP-IB Cable
	98431A	1	Mass Storage ROM

Figure 3-13 shows the Product Support Package and the location of each of the components.

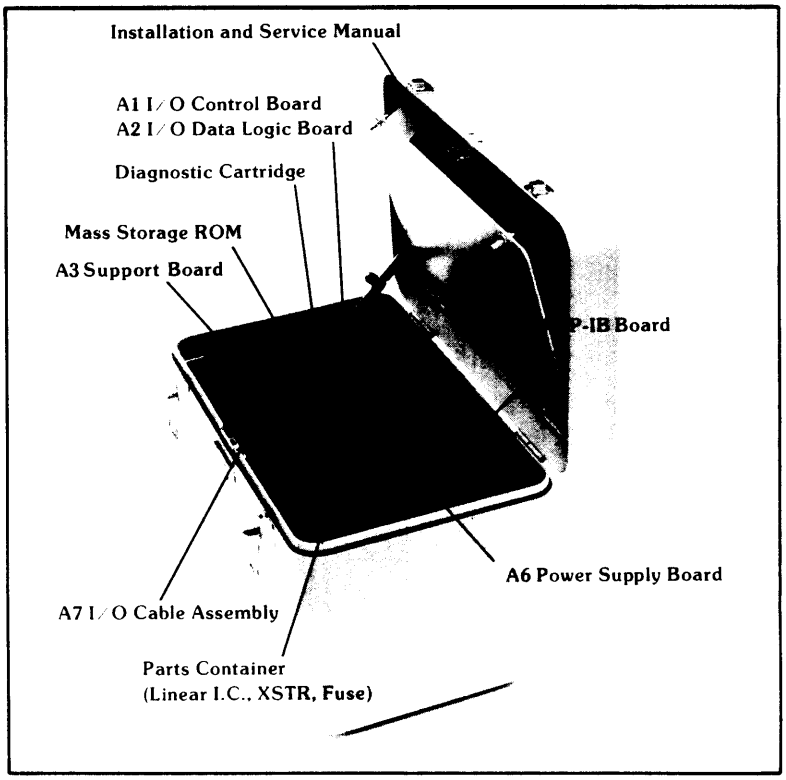


Figure 3-13: Service Kit Component Locations

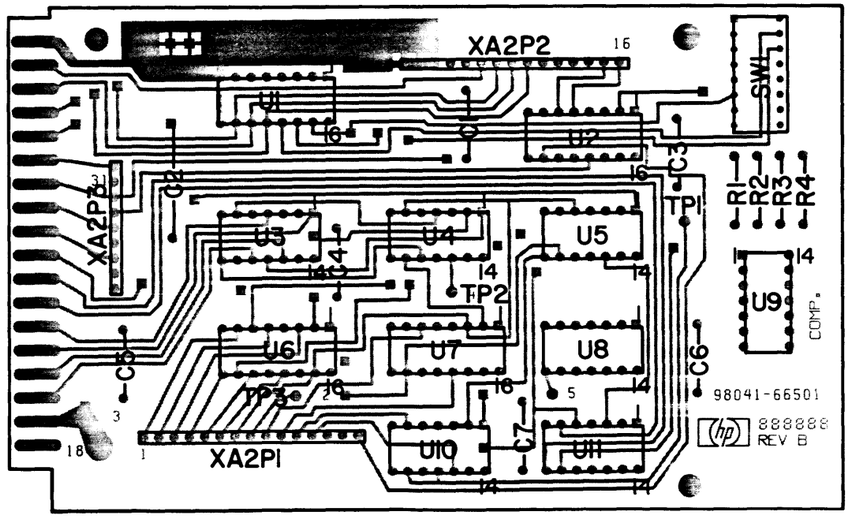
Signal Line Name Abbreviations

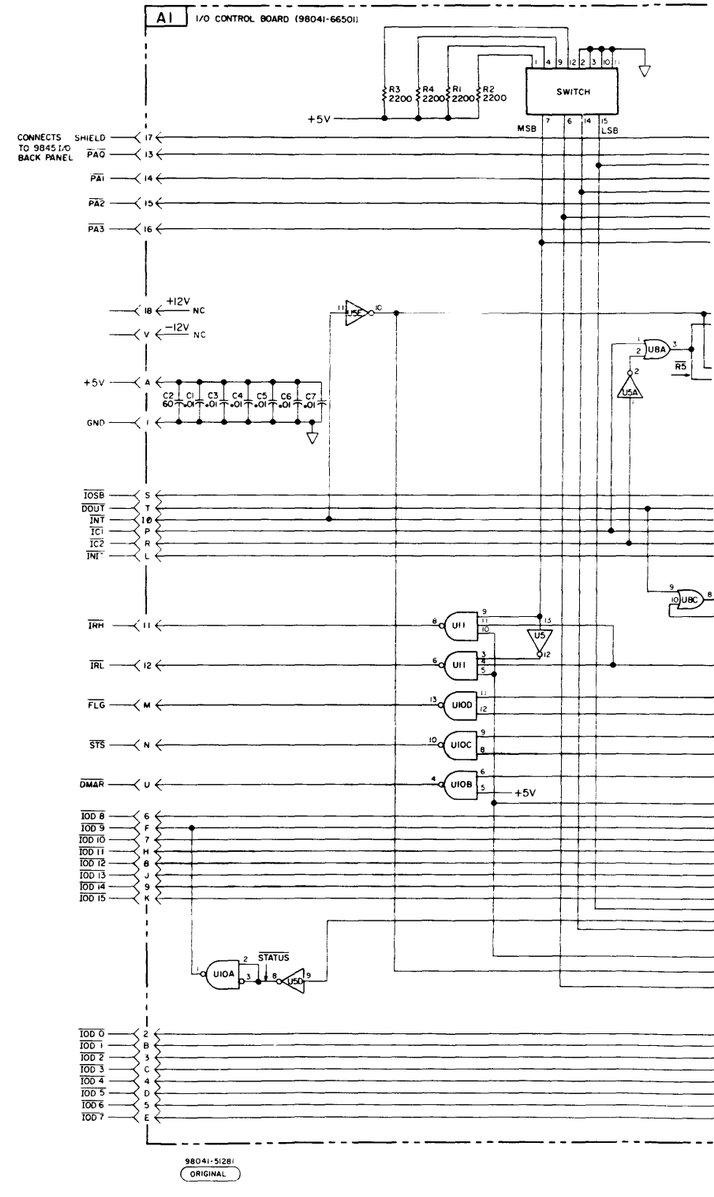
Abbreviation	Meaning
IRCL	Interrupt is Cleared
IRL	Low level Interrupt Line
ISB	Input Second Byte
LBR(N)	Last Byte Ready
LBT	Last Byte Transferred
LOAD	Load I/O Latches
LTE1	Less Than or Equal to 1
LTE11	Less Than or Equal to 11
LW(N)	Last Word
LWIN	Last Word In
MT	FIFOs Empty
OFB	Output First Byte
ORE	Output Register Empty
OSB	Output Second Byte
PAC	PHI Access
PA0-PA3	Peripheral Address Select Lines
PL	Parallel Load (into FIFOs)
POP	Power On Pulse
QIOSB	IOSB qualified with PA
QUIT	IOEND "ORed" with LW
RPRO	Read PHI Register Zero
RST	Reset
SDR	Sampled Data Request
SETDR	Set DMA Request
STBF	Strobe Finished
STPW	STOP Write
STRD	START Read
STS	Status (IOC signal)
STWR	START Write
WRITE(N)	Write PHI Chip Registers
WIR5	Write Instruction Register due to W5
TOP	Transfer Out Parallel
TOPF	Transfer Out Parallel (FIFO)
TOPS	Transfer Out Parallel (Shift Register)

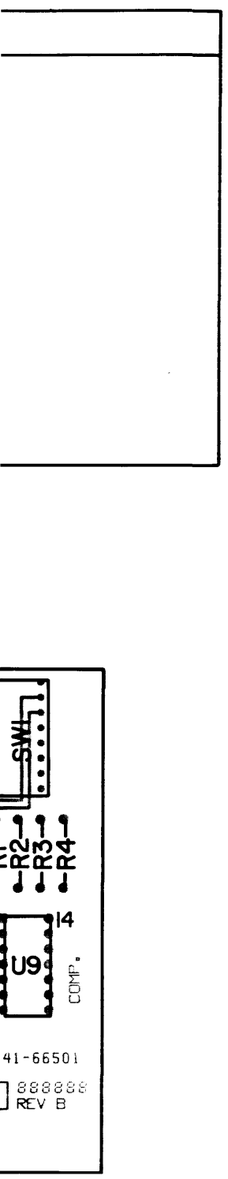
A1 Replaceable Parts

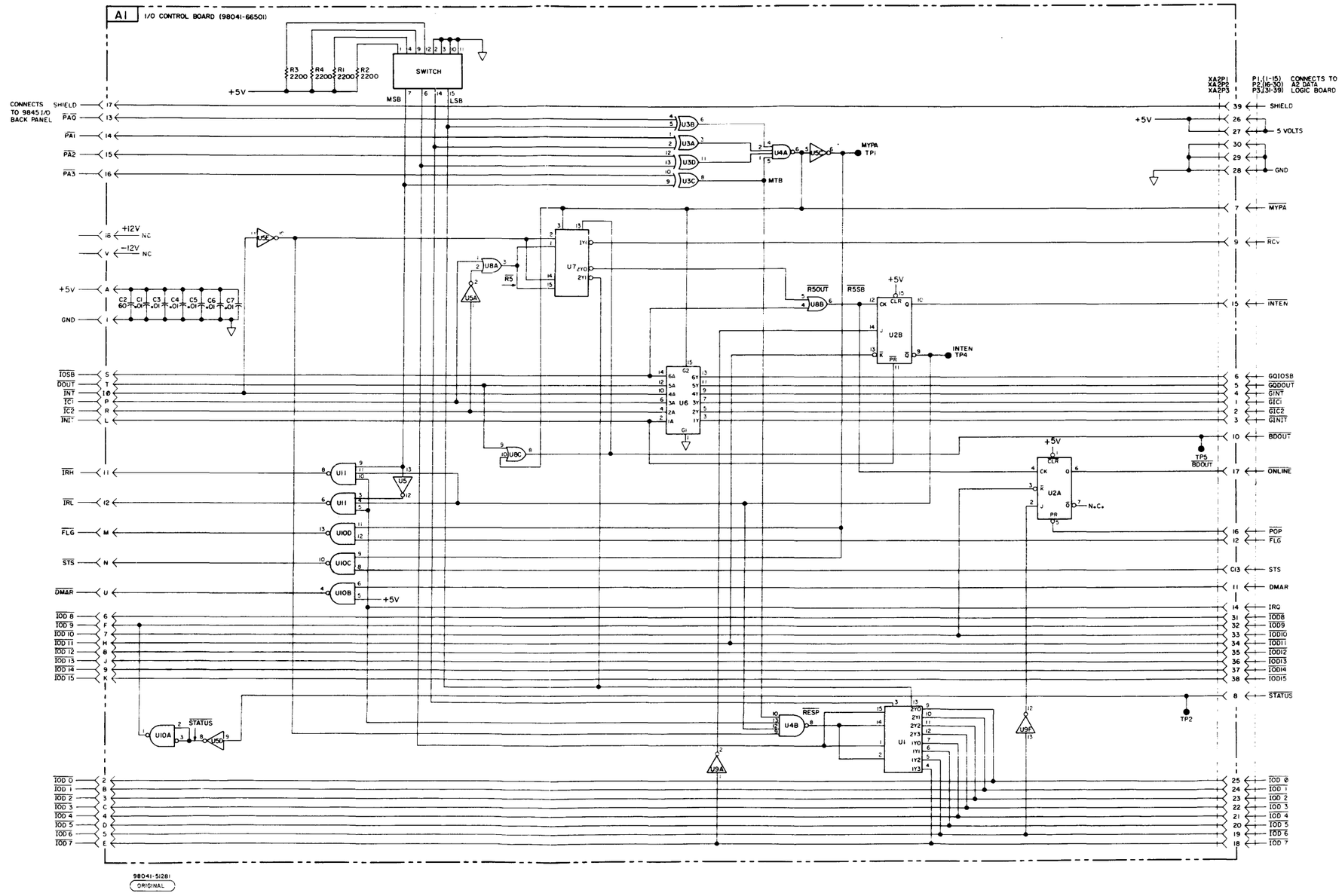
REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
A1	**98041-66501**		**I/O Control Assembly**
C1	0160-3847	6	C-F .01μf 50V
C2	0180-0106	1	C-F 60μf 6V
C3-C7	0160-3847		C-F .01μf 50V
R1-R4	0683-2225	4	R-F 2200Ω 5%
S1	3100-3364	1	Select Code Switch
U11	820-1427	1	IC SN74LS156
U2	1820-1282	1	IC SN74LS109
U3	1820-1211	1	IC SN74LS86N
U4	1820-1204	1	IC SN74LS20N
U5	1820-1199	2	IC 74LS04N
U6	1820-1491	1	IC SN74LS367N
U7	1820-1245	1	IC 74LS155
U8	1820-1208	1	IC SN74LS32
U9	1820-1199		IC 74LS04N
U10	1820-0327	1	IC SN7401N
U11	1820-1414	1	IC 74LS12N
U11	1820-1199		IC 74LS04N
XA2P1,XA2P2		2	Connector 15 socket
XA2P3		1	Connector 9 socket

A1 Component Locator







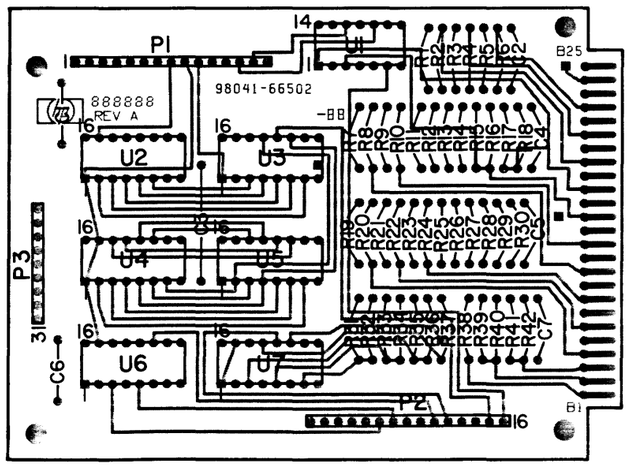


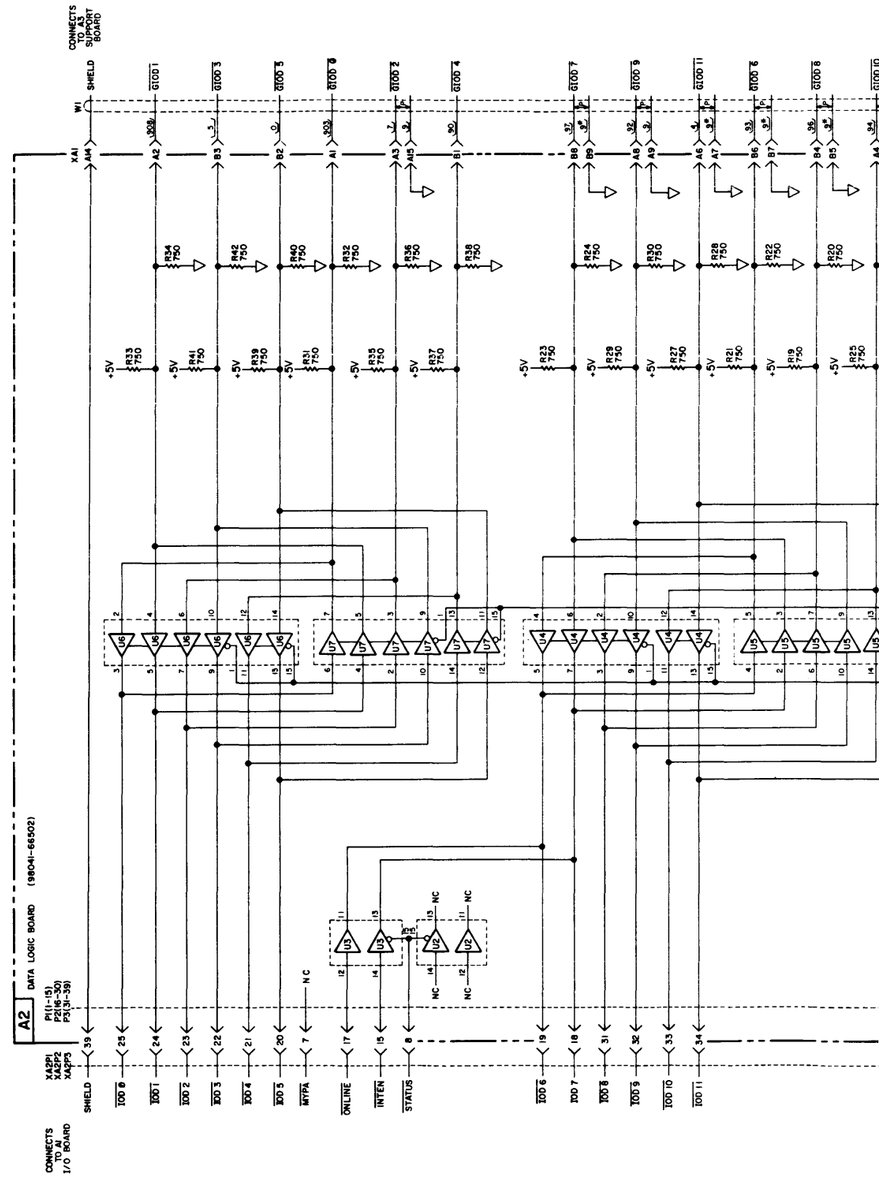
A1 Schematic Diagram

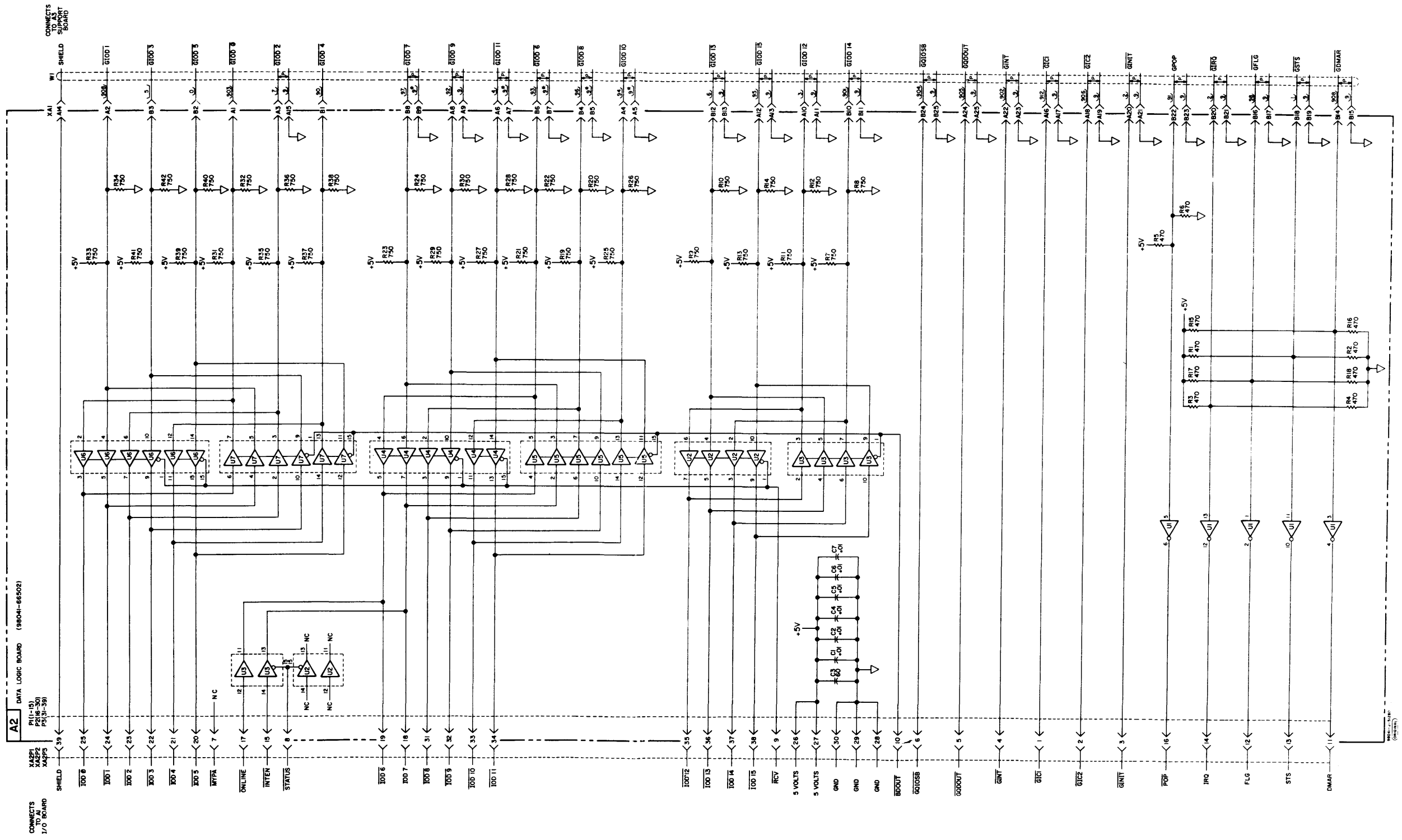
A2 Replaceable Parts

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
A2	**98041-66502**	**1**	**I/O Data Assembly**
C1,C2	0160-3847	6	C-F .01μf 50V
C3	0180-0160	1	C-F 60μf 6V
C4-C7	0160-3847		C-F .01μf 50V
P1,P2		2	Connector 15 P/N
P3		1	Connector 9 P/N
R1-R6	0683-4715	10	R-F 470Ω 5%
R7-R14	0683-7515	3	R-F 750Ω 5%
R15-R18	0683-4715		R-F 470Ω 5%
R19-R42	0683-7515	24	R-F 750Ω 5%
U1	1820-1416	1	IC 74LS14
U2-U7	1820-1491	6	IC SN74LS367N

A2 Component Locator





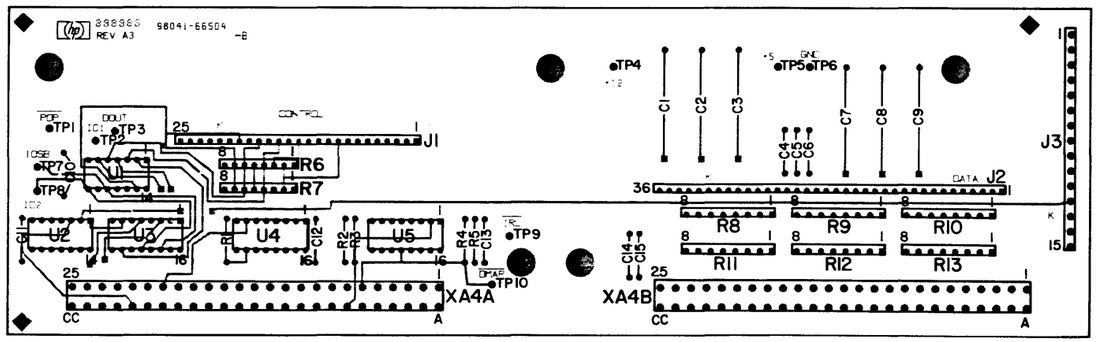


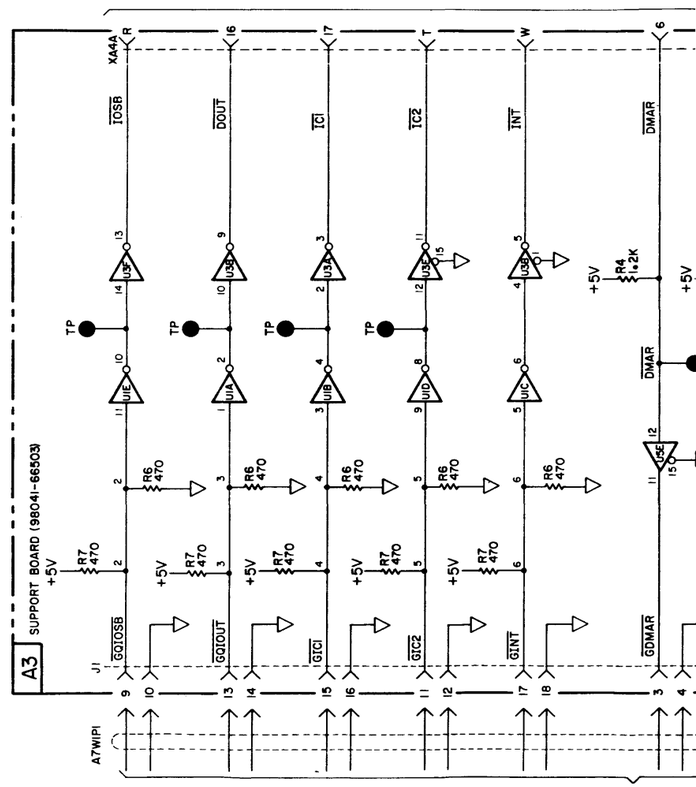
A2 Schematic Diagram

A3 Replaceable Parts

REFERENCE DESIGNATOR	-⚡- PART NO.	TQ	DESCRIPTION
A3	**98041**		**Support Assembly**
C1-C3	0180-0098	3	C-F 100µf 20V
C4-C6	0160-3847	9	C-F .01µf 50V
C7-C9	0180-0097	3	C-F 47µf 35V
C10-C15	0160-3847		C-F .01µf 50V
J1,J2	1251-3691	2	Connector 36 socket
P1	1251-3901	1	Connector 15 P/N
R1	0683-4725	1	R-F 4700Ω 5%
R2-R5	0683-1225	4	R-F 1200Ω 5%
RP1,RP2	1810-0203	2	R-Network
RP3,RP4	1810-0075	2	R-Network
U1	1820-1416	1	IC 74LS14
U2	1820-1201	1	IC SN74LS08N
U3,U4	1820-1492	2	IC SN74LS368N
U5	1820-1491	1	IC SN74LS367N
XA4A,XA4B	1251-2915	2	PC Connector 2x25

A3 Component Locator

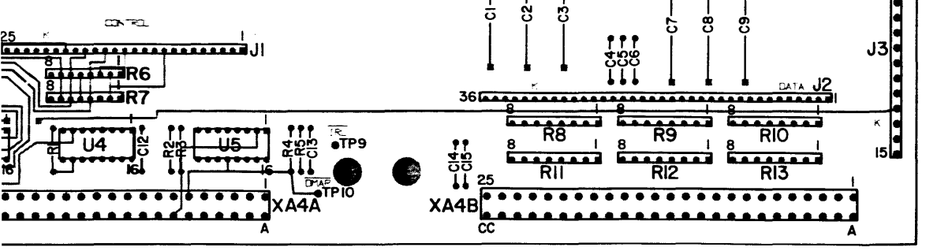


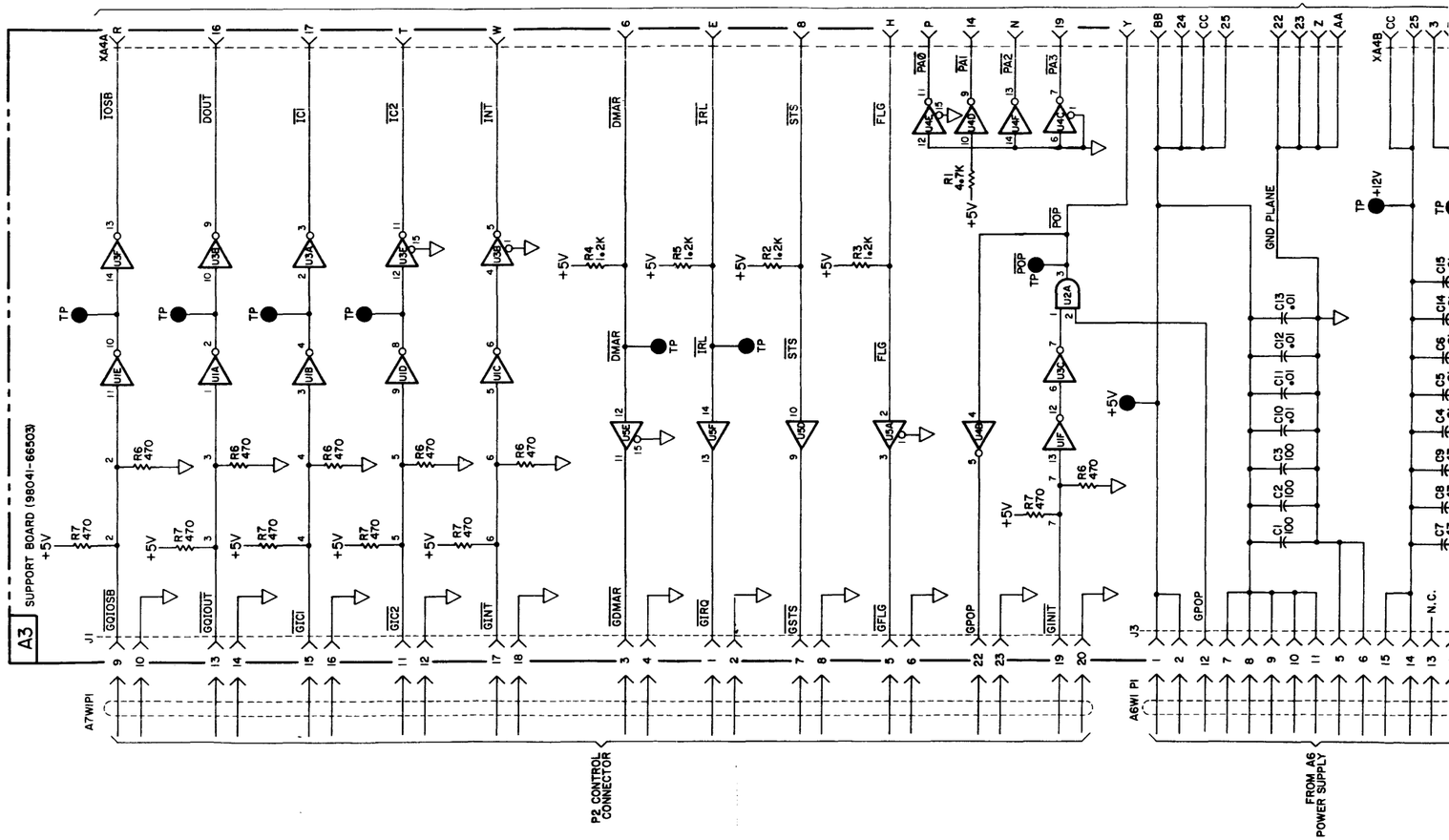


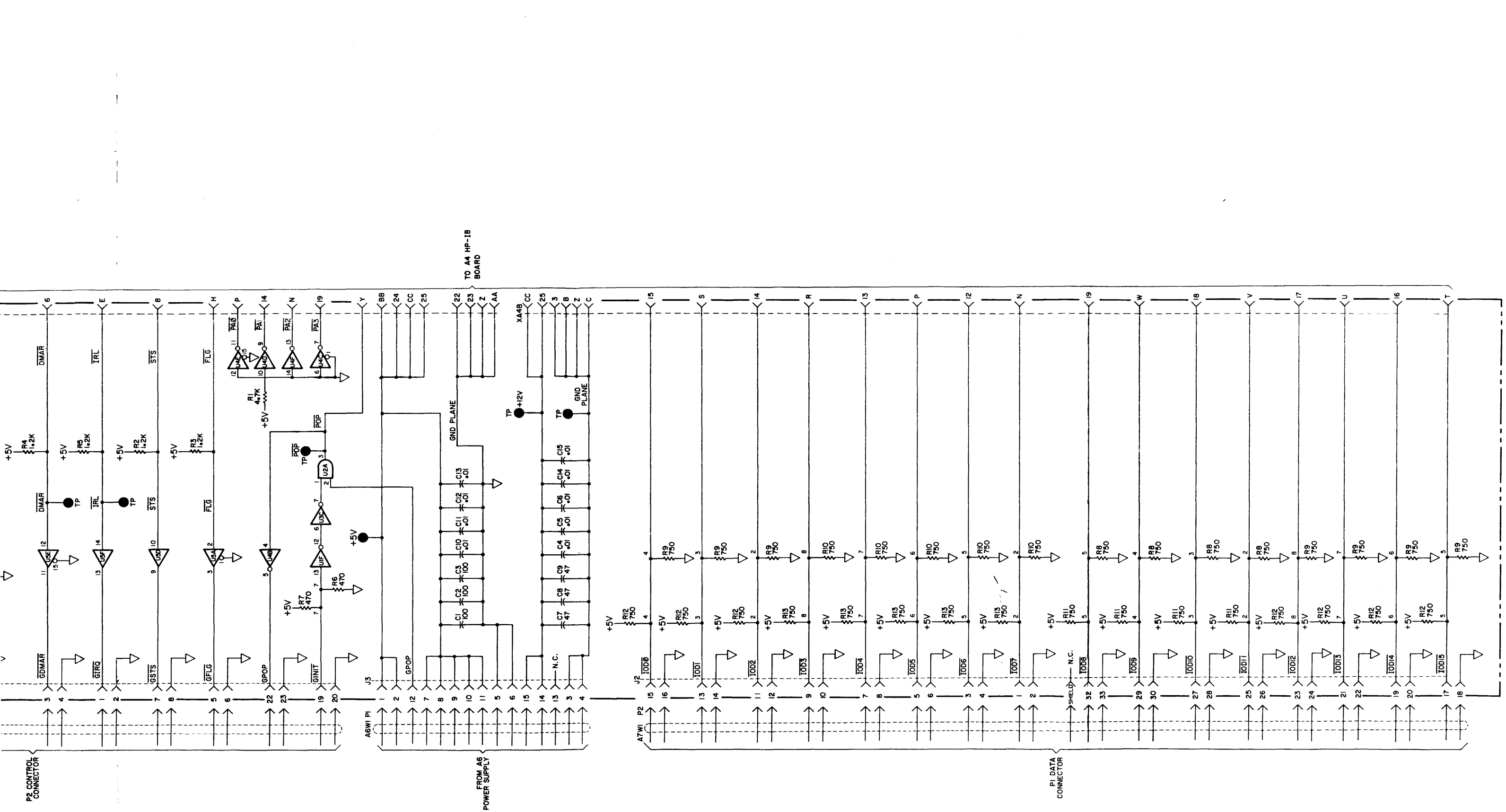
A3 Replaceable Parts

	PART NO.	TQ	DESCRIPTION
	98041		**Support Assembly**
	0180-0098	3	C-F 100μf 20V
	0160-3847	9	C-F .01μf 50V
	0180-0097	3	C-F 47μf 35V
	0160-3847		C-F .01μf 50V
	1251-3691	2	Connector 36 socket
	1251-3901	1	Connector 15 P/N
	0683-4725	1	R-F 4700Ω 5%
	0683-1225	4	R-F 1200Ω 5%
	1810-0203	2	R-Network
	1810-0075	2	R-Network
	1820-1416	1	IC 74LS14
	1820-1201	1	IC SN74LS08N
	1820-1492	2	IC SN74LS368N
	1820-1491	1	IC SN74LS367N
	1251-2915	2	PC Connector 2x25

A3 Component Locator





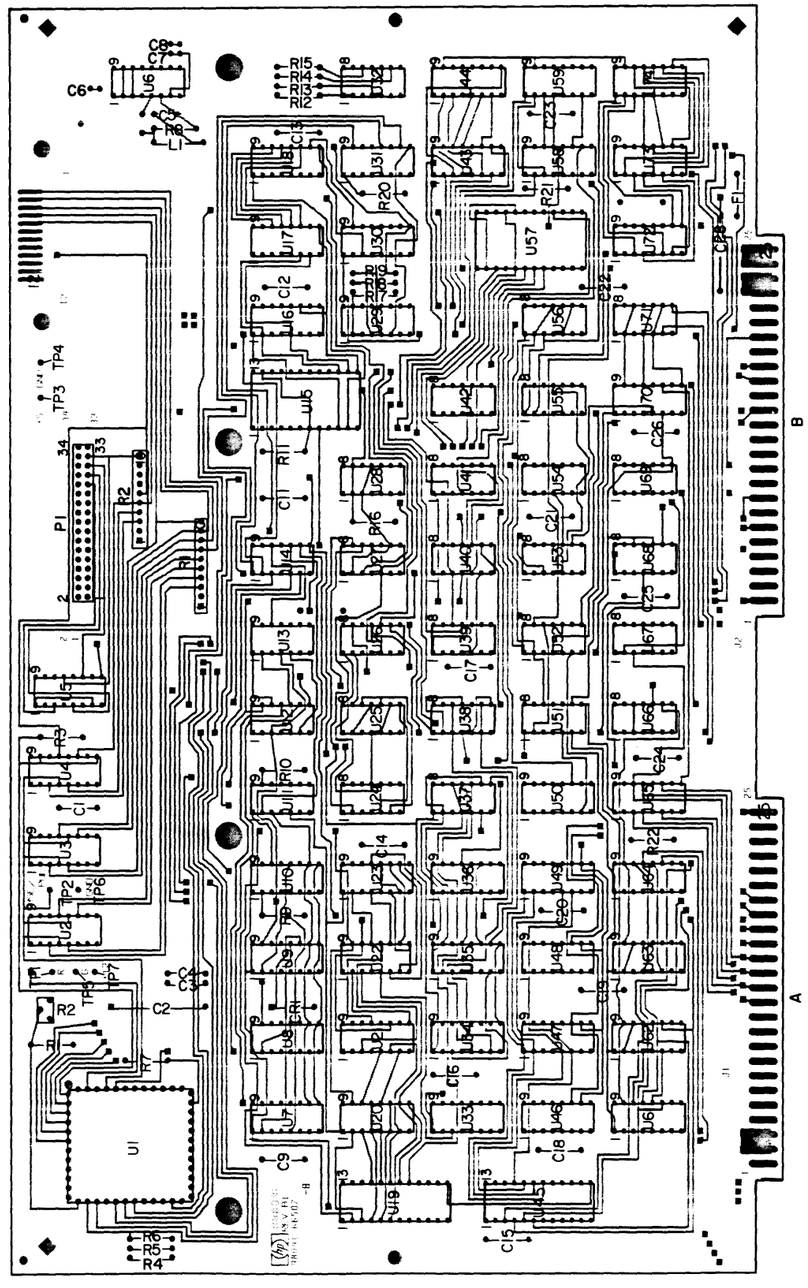


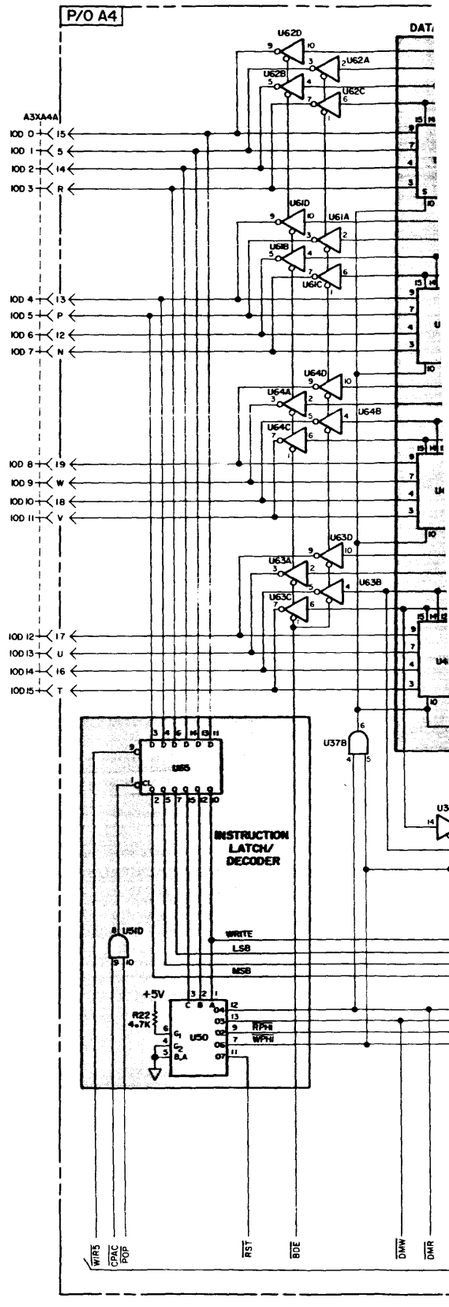
A3 Schematic Diagram

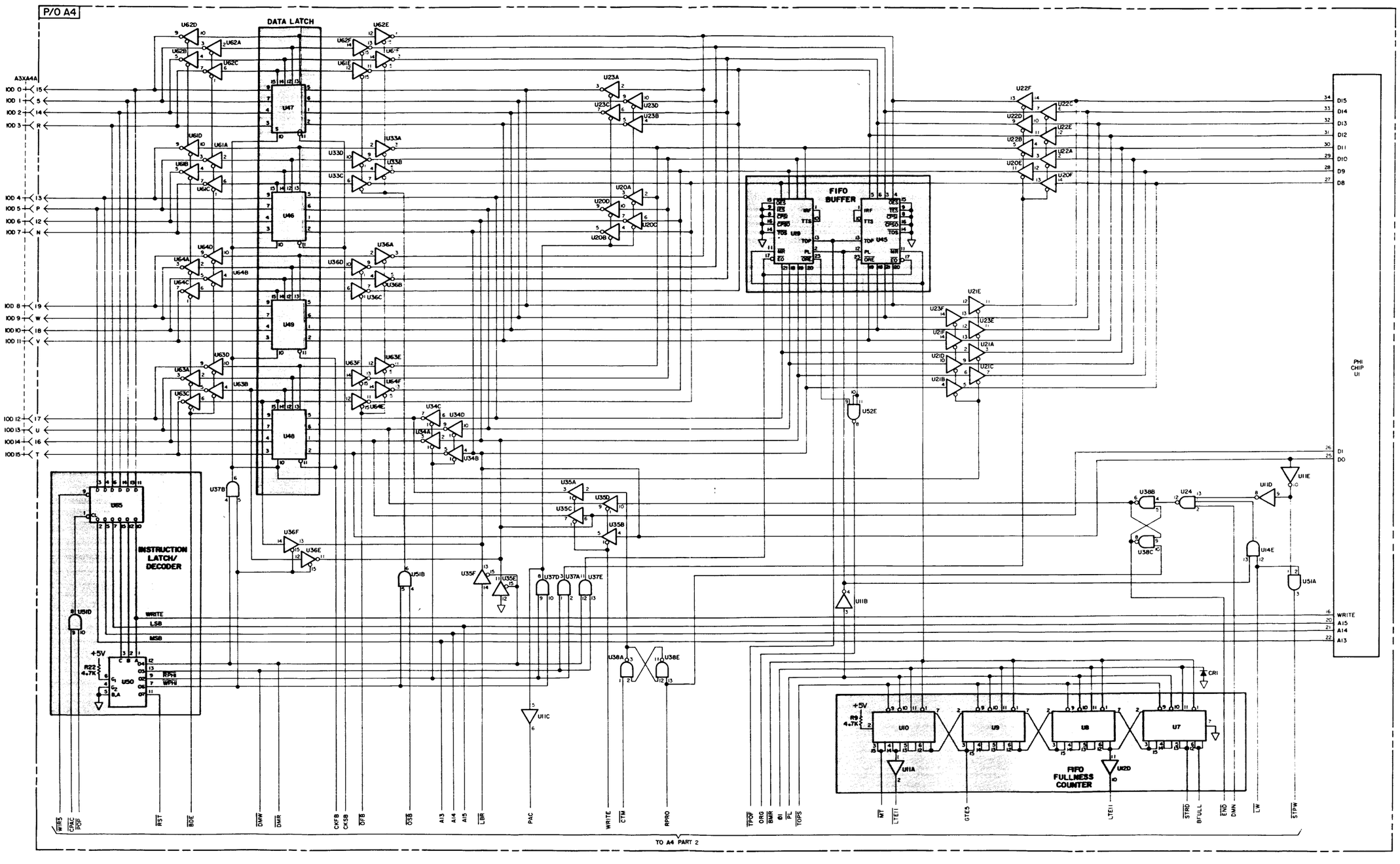
A4 Replaceable Parts

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION	REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
A4	**98041-66507**	**1**	**HP-IB Assembly**				
C1	0160-3847	22	C-F .01μf 50V	U58	1820-1076		IC SN745174N
C2	0180-0098	1	C-F 100μf 20V	U59	1816-1244		IC Memory (ROM)
C3,C4	0160-3847		C-f .01μf 50V				
C5	0140-0190	1	C-F 39pf 300V	U61-U64	1820-1492		IC SN74LS368N
C6-C8	0160-0576	3	C-f .1μf 50V	U65	1820-1196	1	IC SN74LS174N
C9-C27	0160-3847		C-F .01μf 50V	U66	1820-1208		IC SN74LS32
C28	0180-0159	1	C-F 220μf 10V	U67,U68	1820-1209	2	IC 74LS38
				U69	1820-1205	1	IC SN74LS21
CR1	1901-0347	1	Diode – hot carrier	U70	1820-1216		IC SN74LS138
				U71	1820-1204	1	IC SN74LS20N
F1	2110-0568	1	Fuse 4A 125V	U72	1820-2194		IC 74LS257
L1	9140-0112	1	Coil 4.7μh	U73	1820-1076		IC SN74S174N
P1	1251-5068	1	Connector 2x17	U74	1816-1245		IC Memory (ROM)
R1,R2	1810-0328	2	R-Network		1200-0650	1	Socket for U1
R3	0683-4725	15	R-F 4700Ω 5%				
R4-R6	0698-4425	3	R-F 1540Ω 1%				
R7	0683-4725		R-F 4700Ω 5%				
R8	0698-4195	1	R-F 1020Ω 1%				
R9-R18	0683-4725		R-F 4700Ω 5%				
R19	0698-3263	1	R-F 40.2Ω 1%				
R20-R22	0683-4725		R-F 4700Ω 5%				
R	2100-0558	1	R-Variable 20K 10%				
U1	1AA6-6002	1	PHI Chip				
U2-U5	1820-2058	4	IC MC3448				
U6	1820-1977	1	IC MC12061P				
U7-U10	1820-1276	4	IC SN74LS194N				
U11,U12	1820-1199	4	IC 74LS04N				
U13,U14	1820-1201	7	IC SN74LS08N				
U15	1820-0640	2	IC SN74150N				
U16	1820-2194	2	IC 74LS257				
U17	1816-1247	1	IC Memory (ROM)				
U18	1816-1246	1	IC Memory (ROM)				
U19	1816-0934	2	IC FIFO				
U20-U23	1820-1491	6	IC SN74LS367N				
U24	1820-1202	2	IC 74LS10N				
U25	1820-1197	5	IC 74LS00N				
U26	1820-1199		IC 74LS04N				
U27	1820-1197		IC 74LS00N				
U28	1820-1112	3	IC 74LS74				
U29	1820-0629	1	IC 74S112N				
U30,U31	1820-1076	5	IC SN745174N				
U32	1820-1197		IC 74LS00N				
U33	1820-1492	6	IC SN74LS368N				
U34,U35	1820-1491		IC SN74LS367N				
36	1820-1492		IC SN74LS368N				
U37	1820-1201		IC SN74LS08N				
U38,U39	1820-1197		IC 74LS00N				
U40	1820-1201		IC SN74LS08N				
U41,U42	1820-1112		IC 74LS74				
U43	1820-1076		IC SN74S174N				
U44	1816-1243		IC Memory (ROM)				
U45	1816-0934		IC FIFO				
U46-U49	1820-1444	4	IC 74LS298				
U50	1820-1216	2	IC SN74LS138				
U51	1820-1201		IC SN74LS08N				
U52	1820-1202		IC 74LS10N				
U53	1820-1208	2	IC SN74LS32				
U54	1820-1199		IC 74LS04N				
U55,U56	1820-1201		IC SN74LS08N				
U57	1820-0640		IC SN74150N				

A4 Component Locator





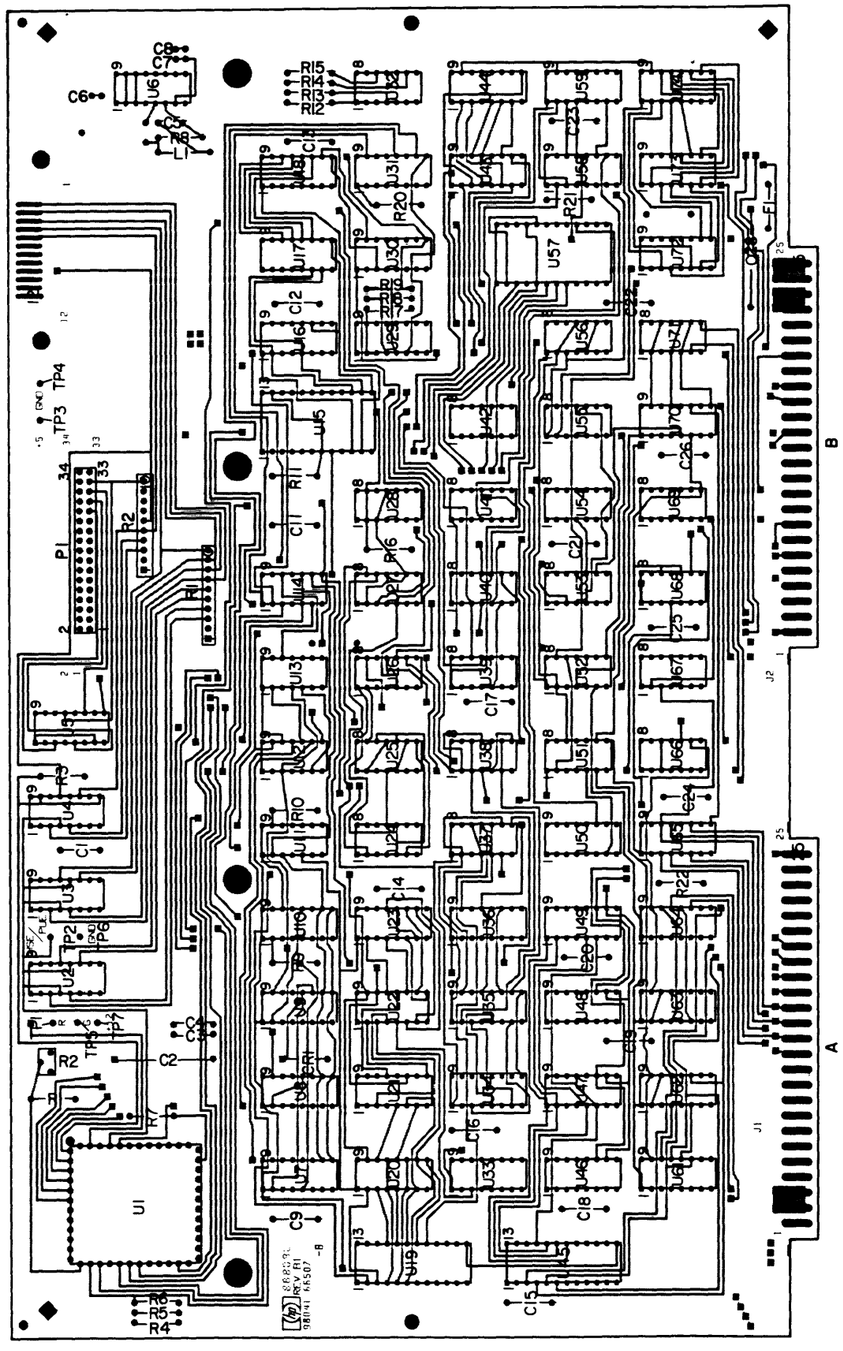


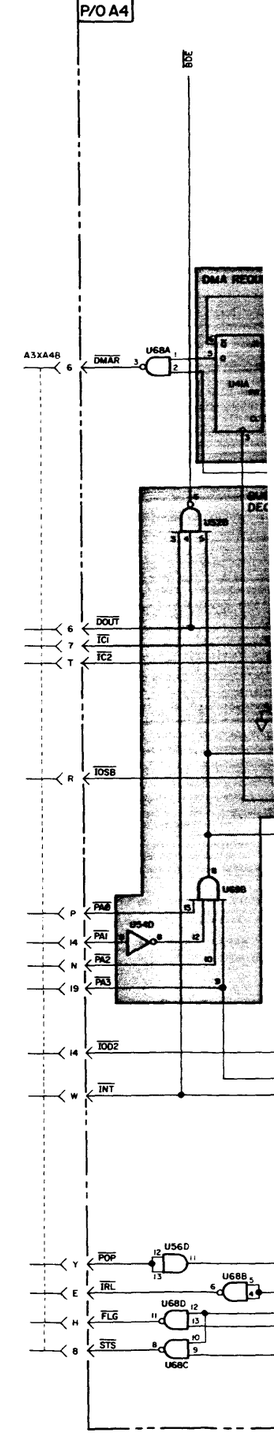
A4 Schematic Diagram Part 1

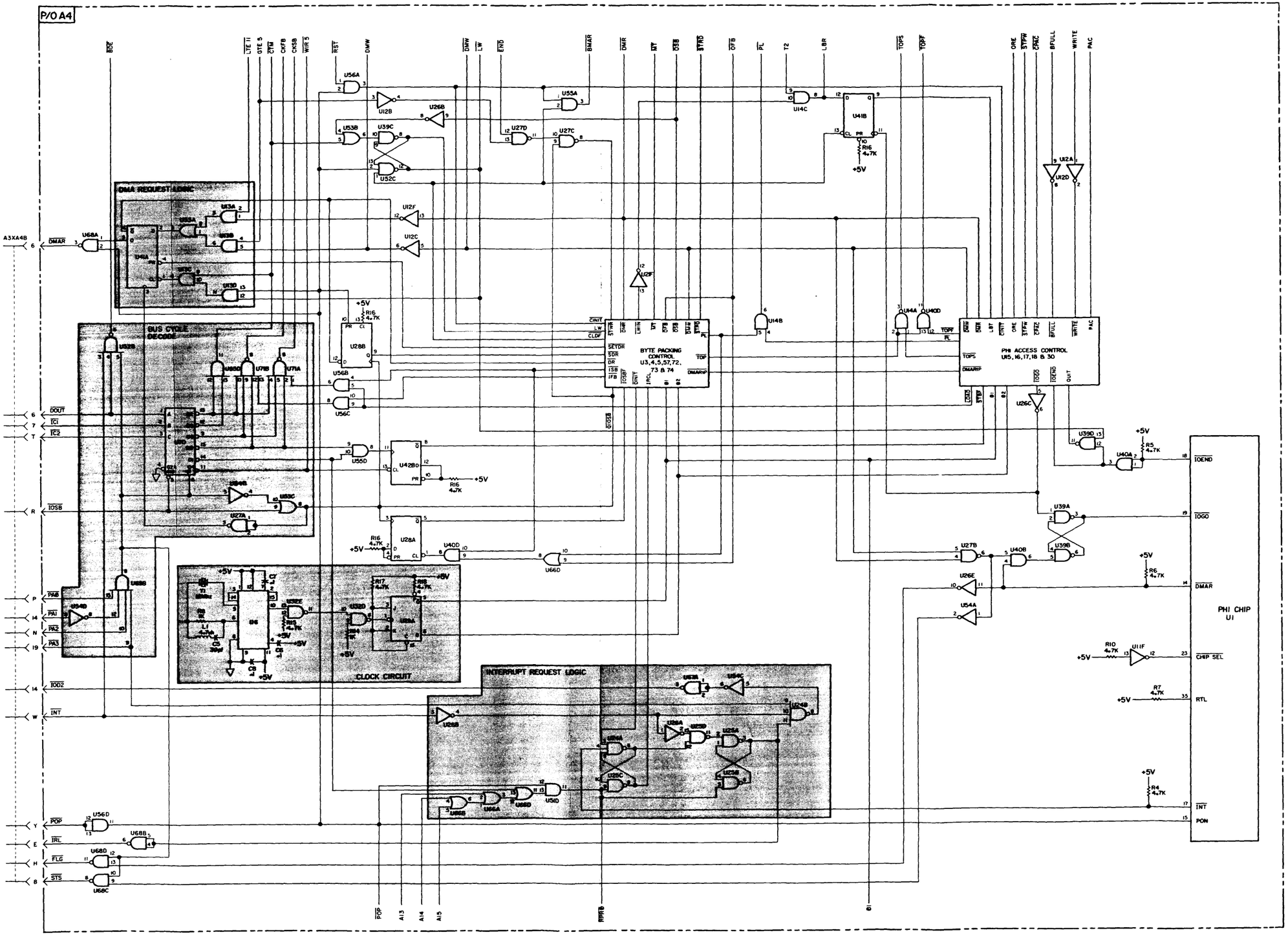
A4 Replaceable Parts

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION	REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
A4	**98041-66507**	**1**	**HP-IB Assembly**				
C1	0160-3847	22	C-F .01μf 50V	U58	1820-1076		IC SN745174N
C2	0180-0098	1	C-F 100μf 20V	U59	1816-1244		IC Memory (ROM)
C3,C4	0160-3847		C-f .01μf 50V				
C5	0140-0190	1	C-F 39pf 300V	U61-U64	1820-1492		IC SN74LS368N
C6-C8	0160-0576	3	C-f .1μf 50V	U65	1820-1196	1	IC SN74LS174N
C9-C27	0160-3847		C-F .01μf 50V	U66	1820-1208		IC SN74LS32
C28	0180-0159	1	C-F 220μf 10V	U67,U68	1820-1209	2	IC 74LS38
				U69	1820-1205	1	IC SN74LS21
CR1	1901-0347	1	Diode – hot carrier	U70	1820-1216		IC SN74LS138
				U71	1820-1204	1	IC SN74LS20N
F1	2110-0568	1	Fuse 4A 125V	U72	1820-2194		IC 74LS257
L1	9140-0112	1	Coil 4.7μh	U73	1820-1076		IC SN74S174N
P1	1251-5068	1	Connector 2x17	U74	1816-1245		IC Memory (ROM)
R1,R2	1810-0328	2	R-Network		1200-0650	1	Socket for U1
R3	0683-4725	15	R-F 4700Ω 5%				
R4-R6	0698-4425	3	R-F 1540Ω 1%				
R7	0683-4725		R-F 4700Ω 5%				
R8	0698-4195	1	R-F 1020Ω 1%				
R9-R18	0683-4725		R-F 4700Ω 5%				
R19	0698-3263	1	R-F 40.2Ω 1%				
R20-R22	0683-4725		R-F 4700Ω 5%				
R	2100-0558	1	R-Variable 20K 10%				
U1	1AA6-6002	1	PHI Chip				
U2-U5	1820-2058	4	IC MC3448				
U6	1820-1977	1	IC MC12061P				
U7-U10	1820-1276	4	IC SN74LS194N				
U11,U12	1820-1199	4	IC 74LS04N				
U13,U14	1820-1201	7	IC SN74LS08N				
U15	1820-0640	2	IC SN74150N				
U16	1820-2194	2	IC 74LS257				
U17	1816-1247	1	IC Memory (ROM)				
U18	1816-1246	1	IC Memory (ROM)				
U19	1816-0934	2	IC FIFO				
U20-U23	1820-1491	6	IC SN74LS367N				
U24	1820-1202	2	IC 74LS10N				
U25	1820-1197	5	IC 74LS00N				
U26	1820-1199		IC 74LS04N				
U27	1820-1197		IC 74LS00N				
U28	1820-1112	3	IC 74LS74				
U29	1820-0629	1	IC 74S112N				
U30,U31	1820-1076	5	IC SN745174N				
U32	1820-1197		IC 74LS00N				
U33	1820-1492	6	IC SN74LS368N				
U34,U35	1820-1491		IC SN74LS367N				
36	1820-1492		IC SN74LS368N				
U37	1820-1201		IC SN74LS08N				
U38,U39	1820-1197		IC 74LS00N				
U40	1820-1201		IC SN74LS08N				
U41,U42	1820-1112		IC 74LS74				
U43	1820-1076		IC SN74S174N				
U44	1816-1243		IC Memory (ROM)				
U45	1816-0934		IC FIFO				
U46-U49	1820-1444	4	IC 74LS298				
U50	1820-1216	2	IC SN74LS138				
U51	1820-1201		IC SN74LS08N				
U52	1820-1202		IC 74LS10N				
U53	1820-1208	2	IC SN74LS32				
U54	1820-1199		IC 74LS04N				
U55,U56	1820-1201		IC SN74LS08N				
U57	1820-0640		IC SN74150N				

A4 Component Locator





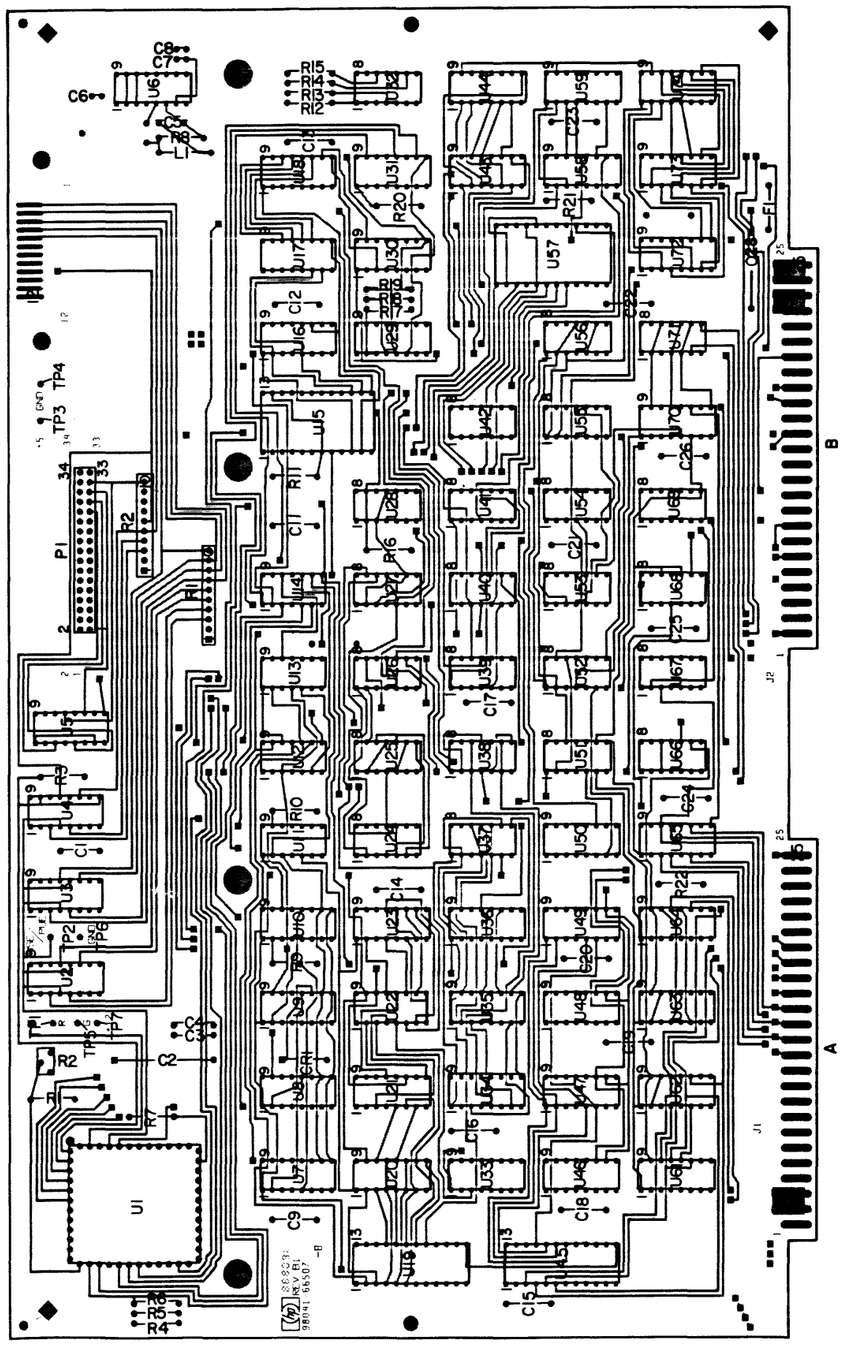


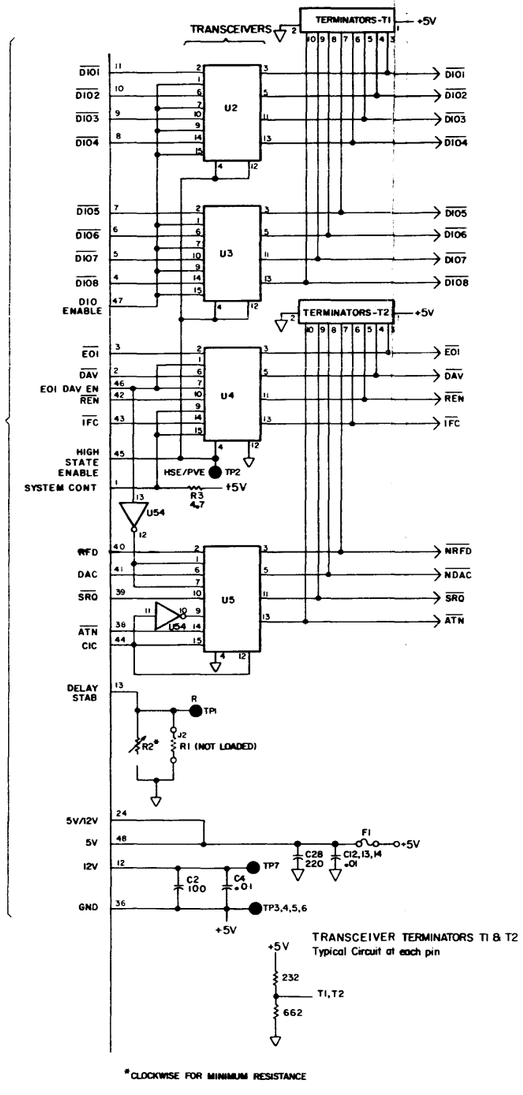
A4 Schematic Diagram Part 2

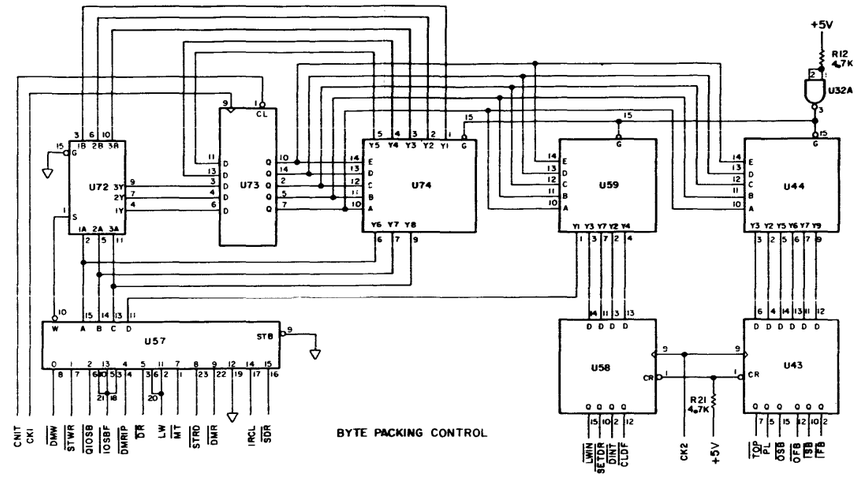
A4 Replaceable Parts

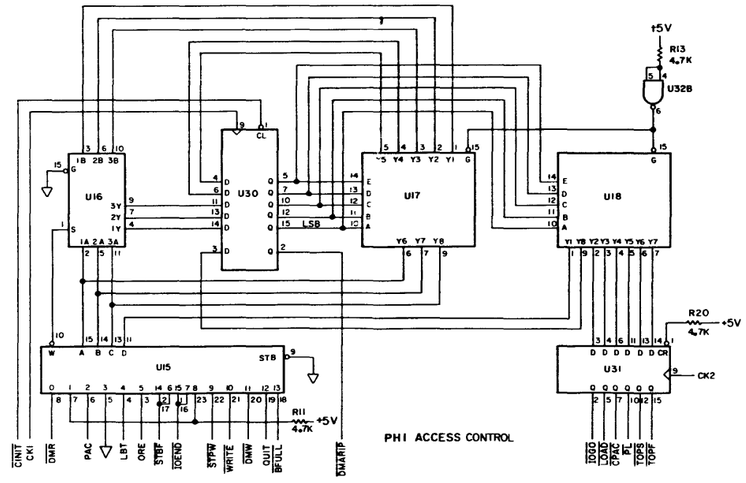
REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION	REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
A4	**98041-66507**	**1**	**HP-IB Assembly**				
C1	0160-3847	22	C-F .01µf 50V	U58	1820-1076		IC SN745174N
C2	0180-0098	1	C-F 100µf 20V	U59	1816-1244		IC Memory (ROM)
C3,C4	0160-3847		C-f .01µf 50V				
C5	0140-0190	1	C-F 39pf 300V	U61-U64	1820-1492		IC SN74LS368N
C6-C8	0160-0576	3	C-f .1µf 50V	U65	1820-1196	1	IC SN74LS174N
C9-C27	0160-3847		C-F .01µf 50V	U66	1820-1208		IC SN74LS32
C28	0180-0159	1	C-F 220µf 10V	U67,U68	1820-1209	2	IC 74LS38
				U69	1820-1205	1	IC SN74LS21
CR1	1901-0347	1	Diode – hot carrier	U70	1820-1216		IC SN74LS138
				U71	1820-1204	1	IC SN74LS20N
F1	2110-0568	1	Fuse 4A 125V	U72	1820-2194		IC 74LS257
L1	9140-0112	1	Coil 4.7µh	U73	1820-1076		IC SN74S174N
P1	1251-5068	1	Connector 2x17	U74	1816-1245		IC Memory (ROM)
R1,R2	1810-0328	2	R-Network		1200-0650	1	Socket for U1
R3	0683-4725	15	R-F 4700Ω 5%				
R4-R6	0698-4425	3	R-F 1540Ω 1%				
R7	0683-4725		R-F 4700Ω 5%				
R8	0698-4195	1	R-F 1020Ω 1%				
R9-R18	0683-4725		R-F 4700Ω 5%				
R19	0698-3263	1	R-F 40.2Ω 1%				
R20-R22	0683-4725		R-F 4700Ω 5%				
R	2100-0558	1	R-Variable 20K 10%				
U1	1AA6-6002	1	PHI Chip				
U2-U5	1820-2058	4	IC MC3448				
U6	1820-1977	1	IC MC12061P				
U7-U10	1820-1276	4	IC SN74LS194N				
U11,U12	1820-1199	4	IC 74LS04N				
U13,U14	1820-1201	7	IC SN74LS08N				
U15	1820-0640	2	IC SN74150N				
U16	1820-2194	2	IC 74LS257				
U17	1816-1247	1	IC Memory (ROM)				
U18	1816-1246	1	IC Memory (ROM)				
U19	1816-0934	2	IC FIFO				
U20-U23	1820-1491	6	IC SN74LS367N				
U24	1820-1202	2	IC 74LS10N				
U25	1820-1197	5	IC 74LS00N				
U26	1820-1199		IC 74LS04N				
U27	1820-1197		IC 74LS00N				
U28	1820-1112	3	IC 74LS74				
U29	1820-0629	1	IC 74S112N				
U30,U31	1820-1076	5	IC SN745174N				
U32	1820-1197		IC 74LS00N				
U33	1820-1492	6	IC SN74LS368N				
U34,U35	1820-1491		IC SN74LS367N				
36	1820-1492		IC SN74LS368N				
U37	1820-1201		IC SN74LS08N				
U38,U39	1820-1197		IC 74LS00N				
U40	1820-1201		IC SN74LS08N				
U41,U42	1820-1112		IC 74LS74				
U43	1820-1076		IC SN74S174N				
U44	1816-1243		IC Memory (ROM)				
U45	1816-0934		IC FIFO				
U46-U49	1820-1444	4	IC 74LS298				
U50	1820-1216	2	IC SN74LS138				
U51	1820-1201		IC SN74LS08N				
U52	1820-1202		IC 74LS10N				
U53	1820-1208	2	IC SN74LS32				
U54	1820-1199		IC 74LS04N				
U55,U56	1820-1201		IC SN74LS08N				
U57	1820-0640		IC SN74150N				

A4 Component Locator









A4 Schematic Diagram Part 3

A5 Replaceable Parts

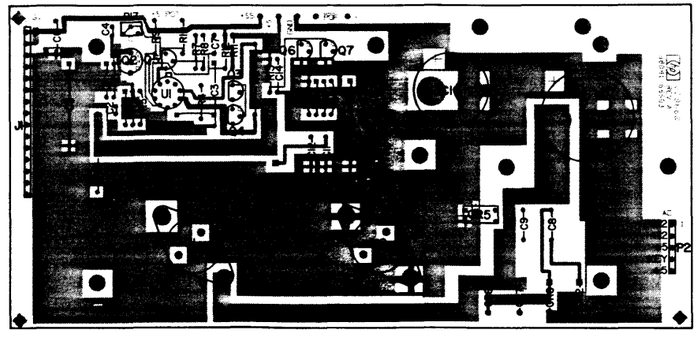
REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
A5	**98041-66505**	**1**	**HP-IB Connector Assembly**
J2	1251-4040	1	Connector HP-IB
W1	98041-61605		HP-IB Cable Assembly
	0360-1636	1	Ribbon Cable
	1251-5165	1	Connector

A6 Replaceable Parts

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
A6	**98041-66503**	**1**	**Power Supply Assembly**
C1	0180-2397	1	C-F 18000μf 25V
C2	0160-0575	2	C-F .047μf 20V
C3	0180-0100	1	C-F 4.7μf 35V
C4	0160-0575		C-F .047μf 20V
C5	0180-0097	2	C-F 47μf 35V
C6	0160-3847	2	C-F .01μf 50V
C7	0160-0362	1	C-F 510pf 300V
C8,C9	0169-0128	2	C-F 2.2μf 50V
C10	0180-2181	1	C-F 1300μf 50V
C11,C12	0160-0170	2	C-f .22μf 25V
C13	0180-0097		C-F 47μf 35V
C14	0160-3847		C-F .01μf 50V
CR1	1902-0041	1	Diode Breakdown 5.11V
CR2	1901-0662	4	Diode Power Rectifier
CR3	1902-3073	1	Diode Breakdown 4.32V
CR4	1902-3165	1	Diode Zener 10.5V
CR5	1901-0364	1	Diode Assembly
CR6,CR7,CR8	1901-0662		Diode Power Rectifier
Q1	1854-0566	1	XSTR NPN SI
Q2	1854-0068	1	Thyristor
Q3-Q7	1854-0071	5	XSTR NPN
U1	1820-0196	1	IC U5R7723393
U2	1826-0117	1	IC Linear
R1	0811-2490	1	R-F 0.1Ω 5W
R2	0683-1515	3	R-F 150Ω 5%
R3	0757-0280	1	R-F 1000Ω 1%
R4	0683-3925	3	R-F 3900Ω 5%
R5	0683-1515		R-F 150Ω 5%
R6	0698-3696	1	R-F 39Ω 5%
R7	0757-0277	1	R-F 49.9Ω 1%
R8	0698-4453	1	R-F 402Ω 1%
R9	0757-0427	1	R-F 1500Ω 1%
R10	0698-3279	1	R-F 4.99KΩ
R11,R12	0757-1094	2	R-F 1.47KΩ 1%
R13	0683-4715	1	R-f 470Ω 5%
R14,R15	0683-3925		R-F 3900Ω 5%
R16	0683-1515		R-f 150Ω 5%
R17	2100-3273	1	R-Var. 2KΩ 10%
	98041-01101	1	Heat Sink

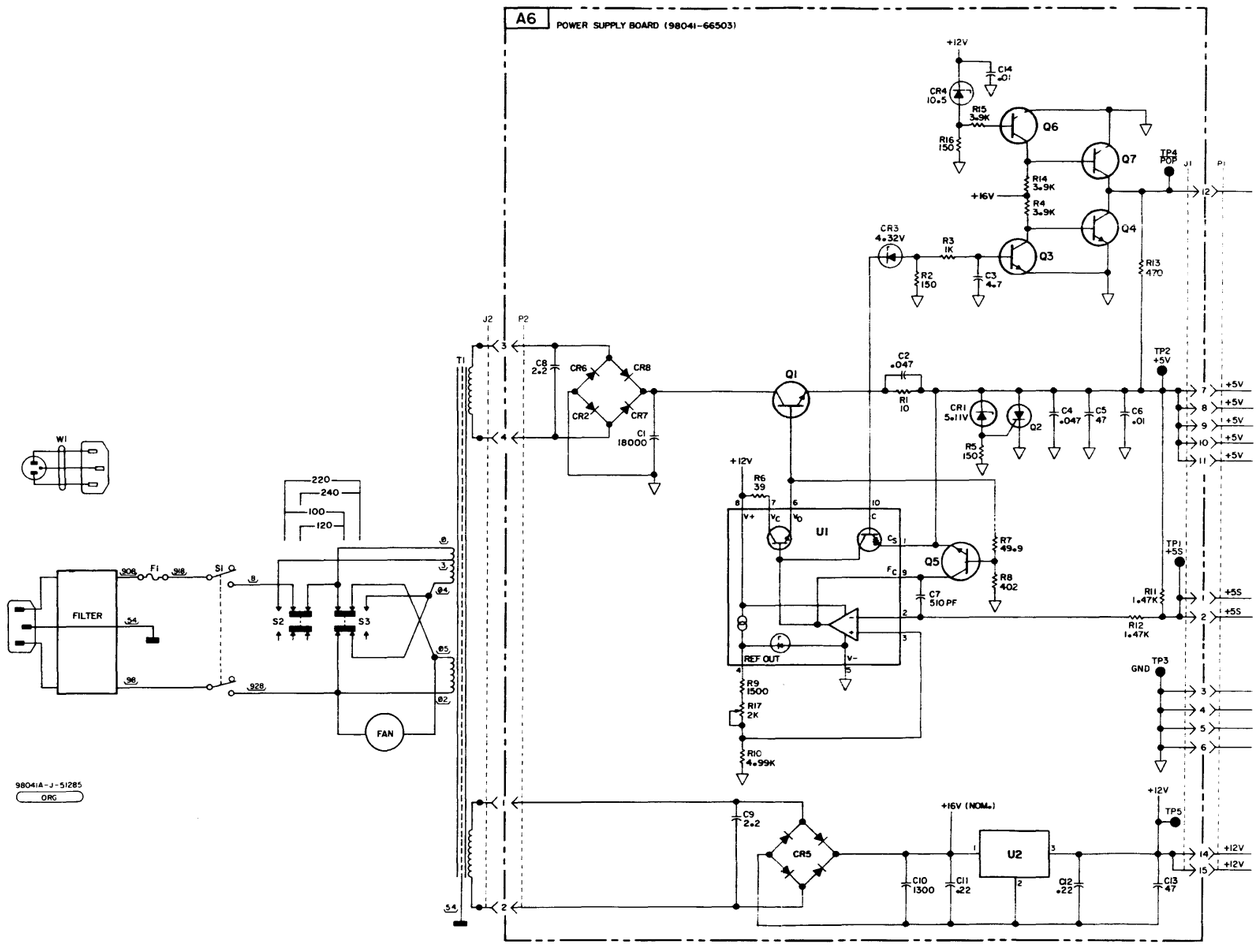
REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
Chassis Mounted	**Power Supply**		**Components**
F1	2110-0043	1	1.5 Amp N.B.
	2110-0543	1	Fuse Holder
	2110-0545	1	Fuse Holder Cap
	3160-0209	1	Fan
	9135-0038	1	Line Filter
S1	3101-2080	1	Rocker Switch (on/off)
S2	3101-2042	2	Slide Switch
T1	9100-4040	1	Transformer
	98041-61607	1	**Transformer Cable**
	98041-61606	1	**D.C. Power Cable**
	1251-0627	2	Polarizing Key Connector
	1251-3223	2	Connector Block
W1	**98041-61603**	1	**Primary Power Cable**
	1251-3170		Connector Plug Body

A6 Component Locator



DESCRIPTION
Components
1.5 Amp N.B.
Fuse Holder
Fuse Holder Cap
Fan
Line Filter
Rocker Switch (on/off)
Slide Switch
Transformer
Transformer Cable
D.C. Power Cable
Polarizing Key Connector
Connector Block
Primary Power Cable
Connector Plug Body

ocator



A6 Schematic Diagram

A7 I/O Cable Assembly Replaceable Parts

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
A7	**98041-61601**	**1**	**I/O Cable Assembly**
A7W1	98041-61602	1	I/O Cable
P1,P2	1251-0688	54	Connector Terminals
P1,P2	1251-3808	2	Polarizing Plug
P1	1251-4506	1	Connector Housing 25 pin
P2	1251-5162	1	Connector Housing 36 pin
XA2	1251-4147	1	Connector P.C. 2x25

A7 Connector Wiring Diagrams

P1 Control Connector

Pin No.	Wire Color	Signal
1	WHT/BLK/VIO	GIRQ
2	WHT	GND-(GIRQ)
3	WHT/BLK/GRA	GDMAR
4	WHT	GND-(GDMAR)
5	WHT/GRA	GFLG
6	WHT	GND-(GFLG)
7	BRN	GSTS
8	WHT	GND-(GSTS)
9	WHT/BLK/YEL	GQIOSB
10	WHT	GND-(GQIOSB)
11	WHT/BLK/BLU	GIC2
12	WHT	GND-(GIC2)
13	WHT/BLK/GRN	GQIOUT
14	WHT	GND-(GQIOUT)
15	WHT/BRN/RED	GIC1
16	WHT	GND-(GIC1)
17	WHT/BLK/RED	GINT
18	WHT	GND-(GINT)
19	RED	GINIT
20	WHT	GND-(GINIT)
21	(KEY)	
22	WHT/BRN	GPOP
23	WHT	GND-(GPOP)

XA2 A2 Boa

Row A Pin No.	Row A Signal	Row A Wire Color
1	IOD0	WHT/BLK/ORN
2	IOD1	GRA
3	IOD2	VIO
4	IOD10	WHT/YEL
5	GND-(IOD0 & 10)	WHT (*)
6	IOD11	YEL
7	GND-(IOD1 & 11)	WHT (*)
8	IOD9	WHT/RED
9	GND-(IOD9)	WHT
10	IOD12	ORN
11	GND-(IOD12)	WHT
12	IOD15	WHT/GRN
13	GND-(IOD15)	WHT
14	–	SHIELD
15	GND-(IOD2)	WHT
16	GIC1	WHT/BRN/RED
17	GND-(GIC1)	WHT
18	GIC2	WHT/BLK/BLU
19	GND-(GIC2)	WHT
20	GINIT	RED
21	GND-(GINIT)	WHT
22	GINT	WHT/BLK/RED
23	GND-(GINT)	WHT
24	GQDOUT	WHT/BLK/GRN
25	GND-(GQDOUT)	WHT

(*) Two wires on each of these pins.

XA2 A2 Board Connector

Row A Pin No.	Row A Signal	Row A Wire Color	Row B Pin No.	Row B Wire Color	Row B Signal
1	IOD0	WHT/BLK/ORN	1	WHT/BLK	IOD4
2	IOD1	GRA	2	BLK	IOD5
3	IOD2	VIO	3	GRN	IOD3
4	IOD10	WHT/YEL	4	WHT/BLU	IOD8
5	GND-(IOD0 & 10)	WHT (*)	5	WHT (*)	GND-(IOD3 & 8)
6	IOD11	YEL	6	WHT/ORN	IOD6
7	GND-(IOD1 & 11)	WHT (*)	7	WHT (*)	GND-(IOD4 & 6)
8	IOD9	WHT/RED	8	WHT/VIO	IOD7
9	GND-(IOD9)	WHT	9	WHT (*)	GND-(IOD5 & 7)
10	IOD12	ORN	10	WHT/BLK/BRN	IOD14
11	GND-(IOD12)	WHT	11	WHT	GND-(IOD14)
12	IOD15	WHT/GRN	12	BLU	IOD13
13	GND-(IOD15)	WHT	13	WHT	GND-(IOD13)
14	–	SHIELD	14	WHT/BLK/GRA	GDMAR
15	GND-(IOD2)	WHT	15	WHT	GND-(GDMAR)
16	GIC1	WHT/BRN/RED	16	WHT/GRA	GFLG
17	GND-(GIC1)	WHT	17	WHT	GND-(GFLG)
18	GIC2	WHT/BLK/BLU	18	BRN	GSTS
19	GND-(GIC2)	WHT	19	WHT	GND-(GSTS)
20	GINIT	RED	20	WHT/BLK/VIO	GIRQ
21	GND-(GINIT)	WHT	21	WHT	GND-(GIRQ)
22	GINT	WHT/BLK/RED	22	WHT/BRN	GPOP
23	GND-(GINT)	WHT	23	WHT	GND-(GPOP)
24	GQDOUT	WHT/BLK/GRN	24	WHT/BLK/YEL	GQIOSB
25	GND-(GQDOUT)	WHT	25	WHT	BND-(GQIOSB)

(*) Two wires on each of these pins.

P2 Data Connector

Pin No.	Wire Color	Signal
1	WHT/VIO	IOD7
2	WHT	GND-(IOD7)
3	WHT/ORN	IOD6
4	WHT	GND-(IOD6)
5	BLK	IOD5
6	WHT	GND-(IOD5)
7	WHT/BLK	IOD4
8	WHT	GND-(IOD4)
9	GRN	IOD3
10	WHT	GND-(IOD3)
11	VIO	IOD2
12	WHT	GND-(IOD2)
13	GRA	IOD1
14	WHT	GND-(IOD1)
15	WHT/BLK/ORN	IOD0
16	WHT	GND-(IOD0)
17	WHT/GRN	IOD15
18	WHT	GND-(IOD15)
19	WHT/BLK/BRN	IOD14
20	WHT	GND-(IOD14)
21	BLU	IOD13
22	WHT	GND-(IOD13)
23	ORN	IOD12
24	WHT	GND-(IOD12)
25	YEL	IOD11
26	WHT	GND-(IOD11)
27	WHT/YEL	IOD10
28	WHT	GND-(IOD10)
29	WHT/RED	IOD9
30	WHT	GND-(IOD9)
31	WHT	GND-(IOD9)
31	(KEY)	
32	WHT/BLU	IOD8
33	WHT/BLU	IOD8
33	WHT	GND-(IOD8)

Chasis and Case Components

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
I/O Card Case	**Components**		
	5040-7801	1	Case,Front Housing,Left
	5040-7802	1	Case,Front Housing,Right
	5040-7803	1	Cover,Rear Housing,Left
	5040-7855	1	Cover,Rear Housing,Right
	5040-7836	1	Spring Latch
Chasis	**Components**		
	5020-7337	1	Front Frame
	5020-8804	1	Rear Frame Casting
	5020-8835	4	Corner Strut
	5040-7201	4	Foot
	5060-9833	1	Top Cover
	5060-9845	1	Bottom Cover
	5060-9855	2	Side Cover
	98041-60201		**Front Panel Assembly**
	1390-0071	2	P/O ¼ Turn Fastener
	1390-0096	2	P/O ¼ Turn Fastener
	1390-0257	2	P/O ¼ Turn Fastener
	1390-0370	2	P/O ¼ Turn Fastener
	98041-00202	1	Front Panel
	7120-1254	1	Identification Plate
	98041-00201	1	Rear Panel
Miscellaneous	**Components**		
	98041-90000	1	Installation Manual
	98041-90030	1	Installation and Service Manual
	98041-90031	1	Diagnostic Test Manual

Appendix

This section contains a reprint of the 12745A-01, the 13037A-06B and the 12037A-06 service notes. These service notes contain the information necessary to add the HP-IB interface to the 13037 Disc Controller.

Service Note 12745A-01

12745A Installation Requirement

Intent:

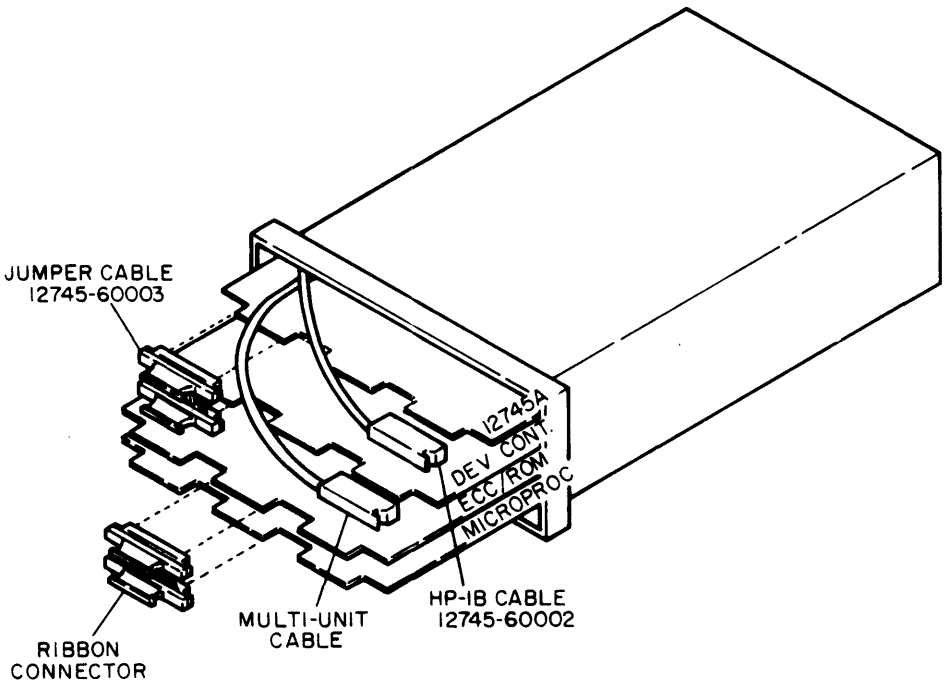
This service note is provided to establish installation requirements for the HP-IB interface to the 13037B Disc Controller.

Content

The 12745A package includes the following:

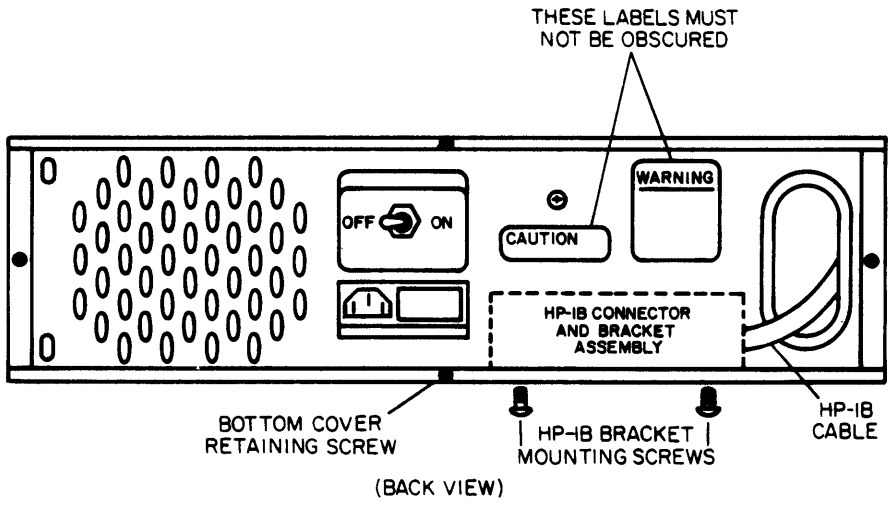
1	12745-60001	Interface PCA
1	12745-60002	HP-IB Interface Cable
1	12745-60003	Ribbon Jumper Cable

A standard cable configuration is shown below:



Note that the 13037B microprocessor and ECC/ROM boards must reside in the lower two card slots of 13037B card cage. The middle (third) slot must contain the 13037B device controller board, with the top (fifth) slot housing the 12745A interface card. Only for such an arrangement will the appropriate cabling be possible.

The 12745A interface cable to the HP-IB bus (part number 12745-60002) requires mounting to the back frame of the 13037B controller cabinet. The HP-IB connector and bracket are attached to the bottom right section of that frame by two screws, as illustrated below (note that the bottom cover of the 13037B must be removed to allow access to the mounting holes).



13037B controllers must be of a 1740 (or greater) date code to be compatable with the 12745A interface card. Controllers having earlier date codes will require varying degrees of modification, depending on the revision of the power subsection. Please refer to Service Note 13037B-01 for power subsection upgrade procedures. Further, 1625 (or later) date code ECC/ROM boards are required for proper operation.

Service Note 13037A-06B

Supersedes:
13037A-06
13037A-06A

13037A Disc Controller Power Subsection Repairs

Problem:
Enhancements to the 13037B power subsection have caused a restructuring of replacements parts that will affect 13037A repairs.

Cause:
The optional 12745A HP-IB interface to the 13037B disc controller required production changes to the 13037 power subsection (see Service Note 13037B-01).

Solution:
A new power regulator assembly (13037-60026) has been put on the exchange program. Although this part is backwards compatible with the 13037-60018 power regulator assembly that it replaces, CSD has chosen to maintain a dual pipeline of these boards. Consequently, the 13037-69018 assembly is still available through CSD as an exchange item.

CPC will stock only the new 13037-60027 power interconnect board. This board is backwards compatible with the older 13037-60020 board, and should be used whenever a replacement is necessary. (Note that the two holes in the board are used only when connecting a 13037-60027 power interconnect board with a 13037-60026 power regulator assembly.)

A new 80,000 μf filter capacitor (part number 0180-2789) has been added to CPC stock. This capacitor provides for increased ripple current, and it is suggested that part number 0180-2789 capacitors be used to replace failed part number 0180-2393 capacitors (the part number 0180-2393 capacitor will still be available, as it is presently used in 7900 power supplies).

48-3/78

Service Note 13037A-06

Supersedes:
None

13037 Power Regulator Assembly and Power Interconnect Board Update

Symptom:

New power supply assembly and power interconnect board in 13037B.

Cause:

The capability to satisfy future increases in power requirements within the 13037B has necessitated an extensive redesign of the 13037-60018 Power Regulator Assemblies with the new 13037-60026 boards. Date Code 1735A 13037B's will replace the old 13037-60020 Power Interconnect Boards with the new 13037-60027 parts. The two stand-offs mounting the 13037-60026 to the 13037-60027 are mounted backwards on 13037-60026 boards having date codes between 1730A and 1735A, but are to be used if the existing 13037-60020 board is to be replaced with a 1307-60027. All new boards are completely compatible with the older ones, so no retrofits will be required. **Note that caution is advised when servicing because the heat sink is at a clearly marked 12-volt potential but the upper standoff is at an unmarked 5-volt potential.**

09/77-48

98041A Disc Interface Installation and Service Manual

Part No. 98041-90030
Microfiche No. 98041-99030

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