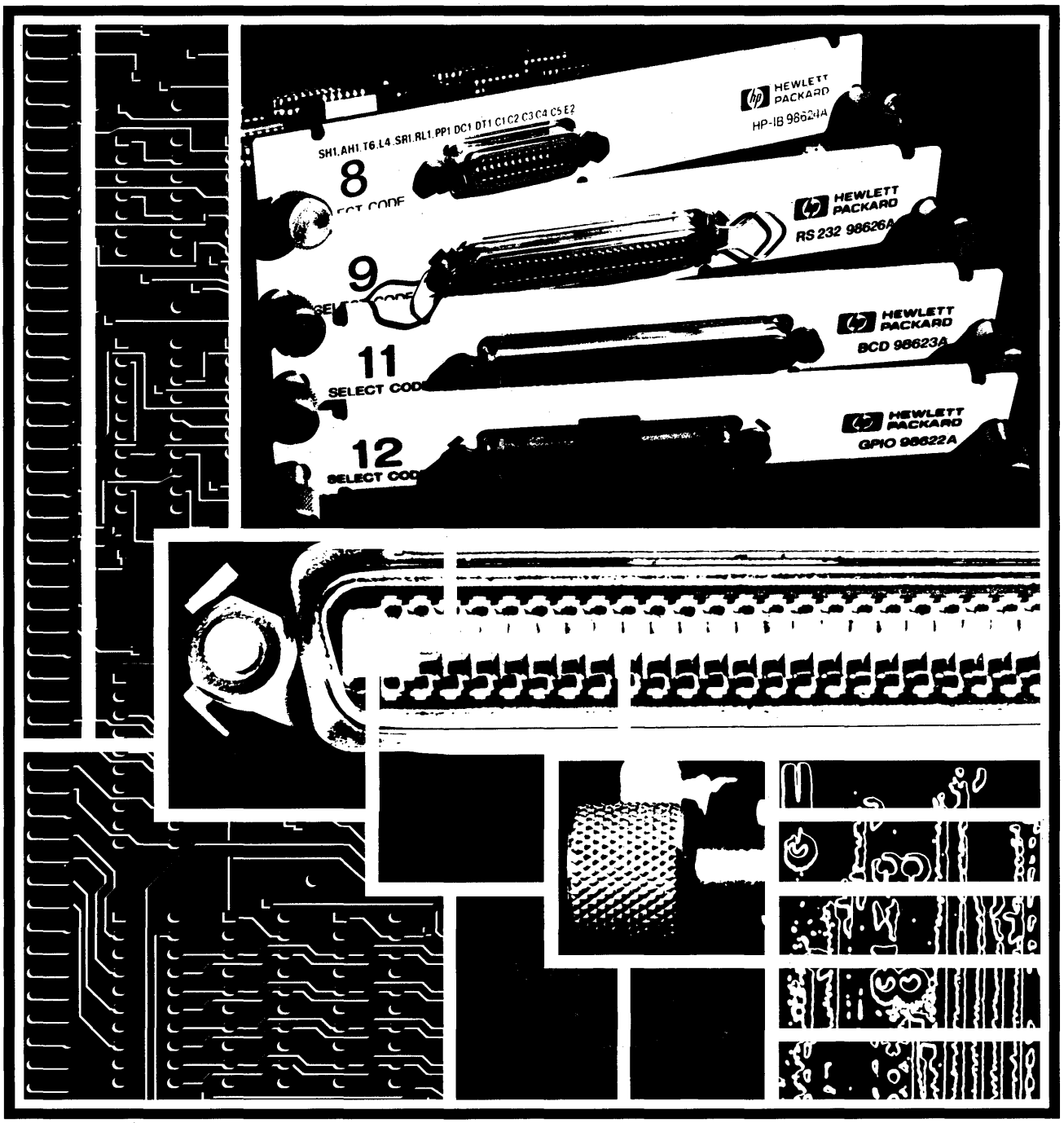
HP Computer Systems

HP 98642A Four-Channel Asynchronous Multiplexer Installation Manual



HEWLETT PACKARD

HEWLETT PACKARD

Warranty Statement

Hewlett-Packard products are warranted against defects in materials and workmanship. For Hewlett-Packard Desktop Computer Division products sold in the U.S.A. and Canada, this warranty applies for ninety (90) days from the date of delivery.* Hewlett-Packard will, at its option, repair or replace equipment which proves to be defective during the warranty period. This warranty includes labor, parts, and surface travel costs, if any. Equipment returned to Hewlett-Packard for repair must be shipped freight prepaid. Repairs necessitated by misuse of the equipment, or by hardware, software, or interfacing not provided by Hewlett-Packard are not covered by this warranty.

HP warrants that its software and firmware designated by HP for use with a CPU will execute its programming instructions when properly installed on that CPU. HP does not warrant that the operation of the CPU, software, or firmware will be uninterrupted or error free.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTIBILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD SHALL NOT BE LIABLE FOR CONSEQUENTIAL DAMAGES.

*For other countries, contact your local Sales and Service Office to determine warranty terms.

HP 9000 Series 300 Computer Systems

HP 98642A
Four-Channel Asynchronous Multiplexer (MUX)

Installation Manual

Card Assembly: 98642-66501

Date Code: B-2535
B-2627

Hewlett-Packard Company
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678

Update 2 (April 1988)
Manual Part Number 98642-90001
E0985
Printed in U.S.A.
September 1985

PRINTING HISTORY

The Printing History below identifies the Edition of this manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same manual with the user-inserted information. New editions of this manual will contain new information, as well.

Manual 98642-90001

First Edition . . . . . September 1985
Update 1 . . . . . August 1986
Update 2 . . . . . April 1988

SAFETY CONSIDERATIONS

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING **The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.**

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged) while the other is electron deficient (positively charged). The level of charge that is developed depends on the type of material. Insulators can easily build up charges in excess of 20,000 volts. A person working at a bench or walking across a floor can build up a charge of many thousands of volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields.

The resulting damage can range from complete destruction to latent degradation. Small geometry semiconductor devices are especially susceptible to damage by static discharge.

The PSI card is shipped in a transparent static shielding bag. The card should be kept in this bag at all times until it is installed in the system. Save this bag for storing or transporting the card. When installing the card in the system, do not touch any components. Hold the card only by the edges or extractor levers.

WARNING

SAFETY EARTH GROUND - The computer on which this product is installed is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety ground must be provided from the main source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and must be secured against any unintended operation.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

CONTENTS

CONTENTS (continued)

Chapter 4
PROGRAMMING

CONTENTS (continued)

Chapter 1
General Information

This manual provides general information, installation, theory of operation, programming information, maintenance instructions, replaceable parts information, and servicing diagrams for the HP 98642A Four-Channel Asynchronous Multiplexer (MUX).

GENERAL DESCRIPTION

The HP 98642A Four-Channel Asynchronous Multiplexer (MUX) is a microprocessor based, asynchronous interface used for controlling EIA RS-232-C/CCITT V.28 terminal-type devices. (EIA stands for the Electronics Industry Association; CCITT is the Consultative Committee for International Telephone and Telegraph, an international standards organization.) The HP 98642A (MUX) provides four full-duplex asynchronous serial I/O ports, one of which is capable of supporting a full-duplex modem.

EQUIPMENT SUPPLIED

The standard HP 98642A Four-Channel Asynchronous Multiplexer consists of the following items:

Printed circuit assembly, part number 98642-66501

Installation manual, part number 98642-90001

15-meter RJ-11 to RJ-11 Direct-Connect Cable for ports 1, 2, or 3. Part number 98642-66505

RJ-11 to RS-232 Adapter. Part number 98642-66508

5-meter U.S. Modem Cable for port 0. Part number 98642-66506

The following cable is available, but not supplied:

15-meter Terminal-Connect Cable for port 0. Part number 98642-66507.

In addition, a Loopback Test Connector, part number 98642-67950, is also available.

The 15-meter cable and loopback test connector can be ordered through the nearest Hewlett-Packard Sales and Support Office. (A list of Hewlett-Packard Sales and Support Offices is contained at the back of this manual.)

IDENTIFICATION

The Product

Up to five digits and a letter (98642A in this case) are used to identify Hewlett-Packard products. The five digits identify the product; the letter indicates the revision level of the product.

Printed Circuit Asembly

The printed circuit assembly supplied with the HP 98642A product is identified by a part number marked on the card. In addition to the part number, the assembly is further identified by a letter and a four-digit date code (e.g., B-2535). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the MUX printed circuit assembly could be:

98642-66501
B-2535

NOTE

For brevity, the "printed circuit assembly" will be referred to merely as "card" in the remainder of this manual.

If the date code stamped on the card does not agree with the date code on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Support Office (a list of Hewlett-Packard Sales and Support Offices is contained at the back of this manual).

Manual

This manual is identified by name and part number. The name, part number, and publication date are printed on the title page. If the manual is revised, the publication date is changed. The "Printing History" page records the reprint dates and manual update record.

SPECIFICATIONS

Table 1-1 lists the specifications of the HP 98642A MUX.

Table 1-1. Specifications

FEATURES

* Four full-duplex asynchronous serial I/O ports (channels)
* One port compatible with full-duplex modem or direct connect
* EIA RS-232-C and CCITT V.28 compatibility
* Programmable baud rates of 110, 134.5, 150, 300, 600, 1200, 2400, 4800, 9600, and 19.2K baud
* Programmable character size of 7 or 8 bits
* Programmable 1 or 2 stop bits
* Programmable parity of odd, even, or none
* Parity, overrun, and framing error detection
* 128-character FIFO receive buffer per channel (port)
* 16-character FIFO transmit buffer per channel (port)
* 16-millisecond timer interrupt interval
* Built-in firmware self-test
* Character recognition via a host-controlled bit map
* Break detection and generation

Table 1-1. Specifications (Continued)

PHYSICAL CHARACTERISTICS

Size:	135 mm by 170 mm (5.3 by 6.6 inches)
Weight:	310 grams (11 ounces)
Backplane Connector:	100-pin edge connector
Device Connectors:	Three 4-conductor modular phone jacks (part number 98642-66505) for ports 1, 2, and 3 (direct-connect ports) One 25-pin RS-232-C connector (part number 98642-66506) for port 0 (modem or direct-connect port)

ENVIRONMENTAL RANGE

Operating:	0 degree C to +55 degrees C 5% to 95% relative humidity
Non-operating:	-40 degrees C to +75 degrees C

POWER REQUIREMENTS

	Current (amps)		Power dissipation (watts)	
Voltage	(typical)	(2-sigma)	(typical)	(2-sigma)
+5V	0.950	1.142	4.75	5.71
+12V	0.057	0.067	0.68	0.80
-12V	0.005	0.007	0.06	0.08

Chapter 2
Installation

This chapter provides information on installing and checking the operation of the MUX.

DETERMINING CURRENT REQUIREMENTS

The MUX circuit card obtains its operating voltages from the host computer. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the card are listed in the power requirements entry of table 1-1. Refer to the appropriate system manual for the power supply capabilities.

FIRMWARE (EPROM) INSTALLATION

CAUTION

SOME OF THE COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD OR REMOVING OR REPLACING COMPONENTS.

The EPROM is installed in a socket on the MUX card as shown in figure 2-1. Ensure that it is installed properly, and that it has not been damaged or loosened from its socket during shipping.

Additionally, when installing or removing the EPROM, guard against bending or breaking the pins on the component. These pins also can be folded between the component and its socket, which would result in intermittent operation of the MUX. To straighten a bent pin, use a lead former such as the Aries® T-516.

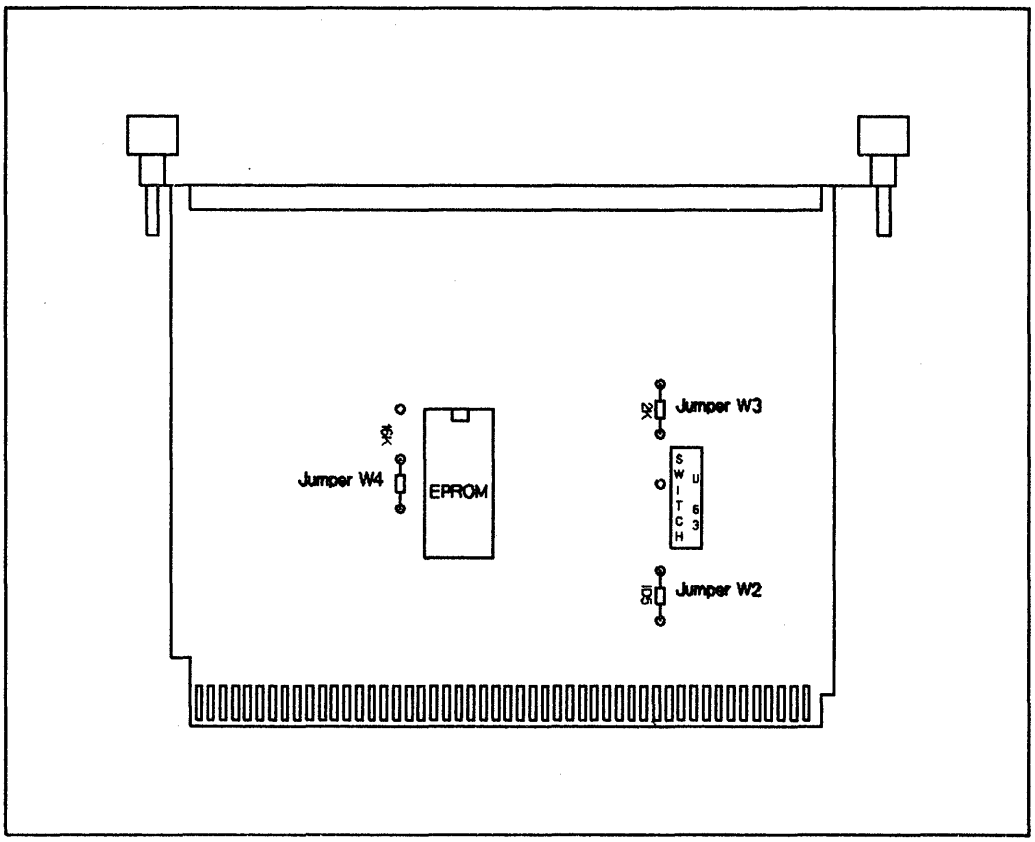


Figure 2-1. Key Component Locations

JUMPERS

Up to three jumpers may be installed on the MUX card. These jumpers are installed at the factory; their locations are shown in figure 2-1 for reference only.

CONFIGURATION SWITCHES

An eight-switch pack on the MUX card is divided into three switch groups. The first group is a single switch (switch 1) which selects the REMOTE or LOCAL mode. This is used to indicate that one of the MUX ports will be used as a system console. The second group consists of switches 2 and 3 and selects the interrupt level of the card. The third group (switches 4 through 8) is used to set the select code of the card.

The default settings of the switches are 0 0 0 0 1 1 0 1. This is indicated in figure 2-2, which shows the switch pack configuration and the switch settings.

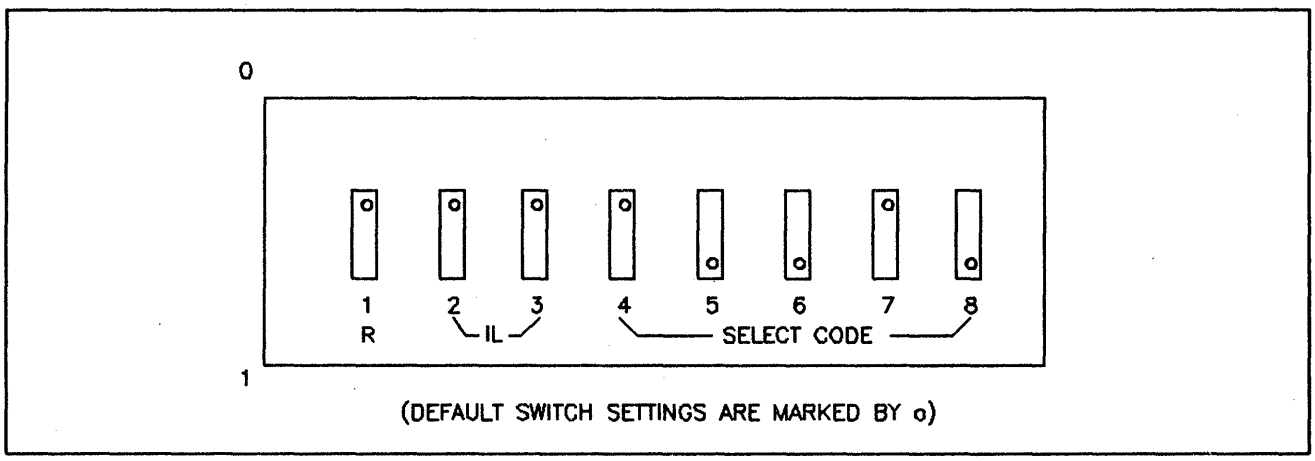


Figure 2-2. Configuration Switches

Select Code Switches

Each interface must have a unique select code so that it can be accessed by the host computer. On the MUX card, the select code is set by switches 4 through 8. The settings of these switches determine the select code of the MUX card and determine the base address in system memory to which the MUX will respond. The settings, memory base addresses, and select codes are shown in table 2-1.

Select codes 0 through 7 should not be used. (Select codes 0 through 6 are reserved for internal peripheral devices such as the keyboard, disc drives, CRT display, etc.; select code 7 is used by the HP-IB interface.) Thus, select codes 8 through 31 are available for the MUX and other interfaces. The default select code setting for the MUX is "13".

Table 2-1. Select Code Settings

Select Code	SWITCH SETTINGS * 4 5 6 7 8	MEMORY ADDRESS	NOTES
0	0 0 0 0 0	600000	Reserved
1	0 0 0 0 1	610000	Codes
2	0 0 0 1 0	620000	.
3	0 0 0 1 1	630000	.
4	0 0 1 0 0	640000	.
5	0 0 1 0 1	650000	.
6	0 0 1 1 0	660000	Do Not
7	0 0 1 1 1	670000	Use
8	0 1 0 0 0	680000	
9	0 1 0 0 1	690000	
10	0 1 0 1 0	6A0000	
11	0 1 0 1 1	6B0000	
12	0 1 1 0 0	6C0000	
13	0 1 1 0 1	6D0000	*Default*
14	0 1 1 1 0	6E0000	
15	0 1 1 1 1	6F0000	
16	1 0 0 0 0	700000	
17	1 0 0 0 1	710000	
18	1 0 0 1 0	720000	
19	1 0 0 1 1	730000	
20	1 0 1 0 0	740000	
21	1 0 1 0 1	750000	
22	1 0 1 1 0	760000	
23	1 0 1 1 1	770000	
24	1 1 0 0 0	780000	
25	1 1 0 0 1	790000	
26	1 1 0 1 0	7A0000	
27	1 1 0 1 1	7B0000	
28	1 1 1 0 0	7C0000	
29	1 1 1 0 1	7D0000	
30	1 1 1 1 0	7E0000	
31	1 1 1 1 1	7F0000	

* See figure 2-2 for the 1 and 0 settings.

Interrupt Level Switches

Switches 2 and 3 determine the level at which the MUX will interrupt. Interrupt levels 1 and 2 are reserved for internal peripheral devices only, leaving interrupt levels 3 through 6 available for the MUX and other interfaces. Interrupt level 3 is lowest priority; 6 is highest priority. If an interrupt request conflict occurs, service is provided by the host computer on the basis of highest priority first. If two devices at the same level interrupt simultaneously, the interrupts are serviced in the order that they are received.

The switch settings and the interrupt levels are shown below. The default interrupt level is 3.

SWITCH SETTINGS 2	3	INTERRUPT LEVEL
0	0	3 (default)
0	1	4
1	0	5
1	1	6

Remote/Local Switch

The Remote/Local Switch (switch #1) determines if MUX port 1 will be used as a system console. When the switch is set to "1", port 1 is to be used as a system console (REMOTE). See below:

SETTING	RESULT
1	REMOTE
0	LOCAL (default)

CABLES

There are several cables, all compatible with EIA RS-232-C and CCITT V.28, for use with the MUX. These cables are available from Hewlett-Packard (see Chapter 1 for part numbers), or they may be fabricated as shown in figures 2-3 and 2-4.

A 5-meter, 4-conductor 28 AWG telephone-type cable is used with ports 1, 2 and 3 (direct-connect ports). A male, 6-position phone jack connector (Amphenol part number AMP 641335-1) is connected to each end of the cable. An adapter is used with this cable for 25-pin connections. The adapter consists of a female RJ-11 phone jack (Amphenol part number AMP 520250-2) interwired to a male DB 25-pin connector.

CAUTION

DO NOT PLUG A TELEPHONE LINE INTO THE RJ-11 JACK ON THE MUX CARD. THIS IS NOT A MODEM JACK. CONNECTING A TELEPHONE LINE TO THIS JACK MAY DAMAGE THE MUX CARD.

For port 0 (modem port), a standard modem cable is used when connecting to a modem (DCE). If port 0 is to be connected to a terminal (DTE), a direct connect cable (which exchanges pins 2 and 3) must be used. This cable is available as HP 92219R through your HP Sales and Support Office.

NOTE

The initials DCE mean "Data Communications Equipment", and are used to refer to modems. Outgoing data is on pin 3, incoming data is on pin 2. DTE are initials for "Data Terminal Equipment", and are used to refer to terminal-type devices. Outgoing data is on pin 2, incoming data is on pin 3.

Figure 2-3 shows the different cables and connectors. Figure 2-4 shows how to wire a connector for ports 1, 2 and 3.

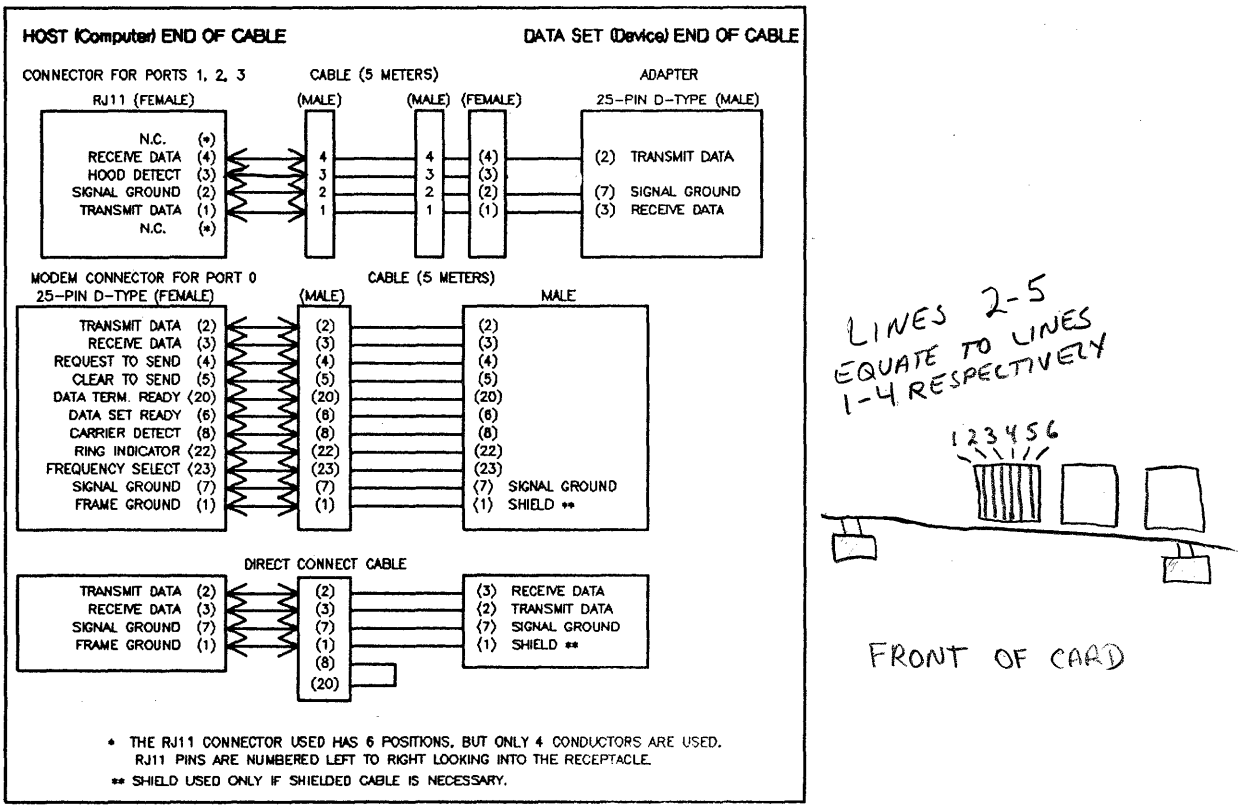


Figure 2-3. Cables used with the MUX

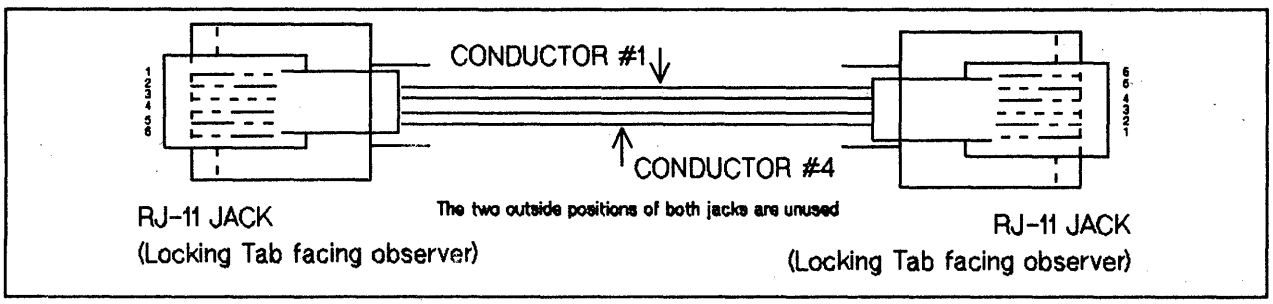


Figure 2-4. Wiring for RJ-11 Connector (Ports 1, 2, 3).

Wiring RJ-11 Jacks for Ports 1, 2 & 3

In wiring this cable, it is important that the conductors be run just as shown in figure 2-4. As an example, if the four (used) conductors are pink, brown, orange, and purple, and the six positions available in the RJ-11 jacks are numbered 1 through 6, then the pink conductor will begin at position 2 (not 1) of jack "A" and terminate at position 5 of jack "B". Likewise, the brown conductor will start at position 3 of jack "A" and end at position 4 of jack "B", the orange at 4 "A" going to 3 "B", and the purple from 5 "A" and ending at 2 "B". Remember: These colors and numbering scheme are for illustration only. Your cable will likely be different, but the principle is the same. Recheck figure 2-4 before wiring.

INSTALLATION

CAUTION

ALWAYS ENSURE THAT THE POWER TO THE COMPUTER IS OFF BEFORE INSERTING OR REMOVING THE MUX CARD OR CABLE. FAILURE TO DO SO MIGHT RESULT IN DAMAGE TO THE MUX.

CAUTION

SOME OF THE COMPONENTS USED ON THE MUX CARD ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD.

Install the MUX as follows:

1. Set the switches on the card for proper operation in your system. See figure 2-1 for the location of the switch bank and the applicable paragraphs in this chapter for the switch settings.

2. Install the card in the appropriate I/O slot in the computer. Refer to the computer system installation manual for further information, if necessary. Components on this card must be on the same side as for other cards in the computer. When installing the card, use care not to damage components or

traces on this or adjacent cards. Tighten the two thumbscrews (one on each side of the card) to seat the card firmly in place in the computer.

3. Connect the appropriate cable(s) to the card.

START UP

To start up and verify correct operation of the MUX, perform the following:

1. Turn on computer system power.

2. A self-test, which is executed at power on, is contained on the card. If the card does not pass self-test, a message will appear on the CRT indicating that the card has failed. The type of failure will be identified and the card will be identified by ID number and select code. If the MUX card fails self-test, refer to Chapter 5 for maintenance instructions using the loop-back test hoods (the loop-back test hoods exercise more of the card's circuitry).

RESHIPMENT

If the MUX is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment. Include the part number of the MUX.

Pack the card in the original factory packing material, if available. If the original material is not available, use the same quality and type materials as originally used. Commercial packing and shipping companies have the facilities and materials to repack the item. BE SURE TO OBSERVE THE ANTI-STATIC PRECAUTIONS FOUND IN THE FRONT OF THIS MANUAL.

Chapter 3

Theory of Operation

The HP 98642A Four-Channel Asynchronous Multiplexer (MUX) is used to interface to up to four peripheral devices, either through direct-connect (ports 1, 2, and 3), or through a modem (port 0) (note that port 0 can also be used to connect directly to a peripheral device if a direct connect cable is used).

FUNCTIONAL THEORY OF OPERATION

A functional block diagram of the MUX card is shown in figure 3-1. Reference also should be made, as necessary, to the schematic logic diagram contained in Chapter 7, figure 7-1.

To simplify locating components on the three sheets of figure 7-1, the following scheme is used: There are ten numbers across the top and bottom border of the schematic's three sheets, going from 10 to 19, 20 to 29, and 30 to 39, respectively. The first digit indicates the sheet number, 1, 2, or 3, and the second digit is the vertical column. A set of five letters, A through E, are on the left and right borders of the schematics. This provides 50 easy to locate areas. To make the coordinates easy to find in the text, they are set off in brackets []. For example, [25C] would be found on the second sheet, column number 5, and horizontal row C.

The MUX card contains the following major components:

- Z-80A CPU (Central Processing Unit)
- Two Z-80A SIO/2s (Serial Input/Output)
- Two Z-80A CTCs (Counter/Timer Circuit)
- Backplane interface circuitry
- 8K by 8 EPROM
- 2K by 8 static RAM
- Shared memory controller
- FIFO input and output registers

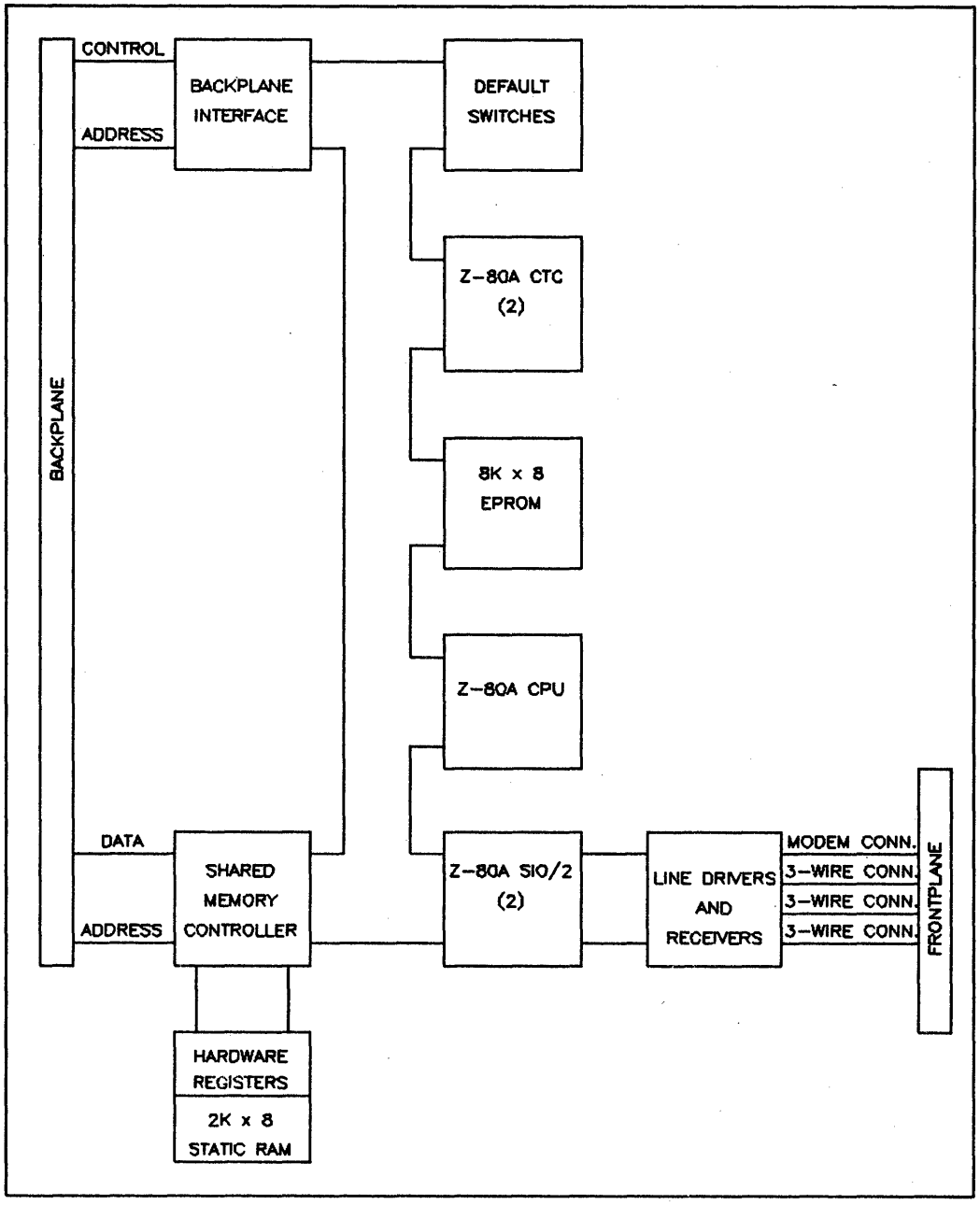


Figure 3-1. MUX Functional Block Diagram

- RS-232-C/V.28 line drivers and receivers
- Three RJ-11 telephone-type connectors (channels 1, 2, and 3)
- 25-pin D-type connector for modem or direct connect (channel 0)
- 100-pin backplane connector

The heart of the MUX is the Z-80A CPU [A25]. The CPU controls the two Z-80A SIO/2s [13A and 13C], the CTCs [12A and 12D], the EPROM [26B], the RAM [27E], and the backplane interface circuitry (sheets 2 and 3, 7-1).

A brief description of the function of each block shown in figure 3-1 is as follows:

The backplane interface circuitry bridges communication between the host computer and the MUX.

The default switches are used to set the select code and the interrupt level of the MUX, and to indicate if one of the devices connected to the MUX (port 1) is to be the system console.

The CTC contains four independent counter/timer channels. Two CTCs are used on the MUX card.

The 8K byte EPROM is used to store the firmware.

The SIO is a programmable serial I/O controller with two independent full-duplex channels with separate control and status lines. The MUX uses two SIOs.

The shared memory controller arbitrates the RAM resources on the card between the Z-80A CPU and the host CPU.

The hardware registers are used to pass information between the card and the host computer.

The 2K byte static RAM is used for I/O buffering and storage of temporary data.

The line drivers and receivers are used to transmit and receive data between the MUX and the peripheral devices.

Overview

The MUX card is "memory mapped" to the host computer. This means that the host communicates with the card via reads and writes to a portion of the host's memory space which is reserved for I/O functions. This memory portion is defined by the select code on the MUX card (see Chapter 2, table 2-1). No two cards on a host backplane can have the same select code.

When the host decides to service (address) the MUX, it sends an address strobe to indicate that the backplane address is valid. If the address of the MUX card matches the upper byte of the 24-bit address, the MUX asserts the IMA (I aM Addressed) line to acknowledge the match. This begins a host memory cycle. For more details on a memory cycle, see the paragraph "*Shared Memory Controller*".

The MUX operating firmware is contained in the 8Kx8 EPROM, U57 [B26]. This firmware can only be accessed by the Z-80A. The 2Kx8 RAM, U55 [27E], along with hardware registers U73, U75, U38, and U16 [28A through 28D], are used to exchange information between the host and the Z-80A. The entire RAM and register contents are in addressing space dedicated to shared memory, thus any location in RAM can be accessed by either the Z-80A or host processors. Most of the RAM space is reserved for FIFO registers that buffer transmit and receive characters. Refer to the paragraph "*Memory Addressing Space*" for information on memory mapping, and the paragraph "*Shared Memory Controller*" for timing details.

The two Z-80A Serial Input/Output circuits [13A and 13C] accept the asynchronous bit streams received from the peripheral devices via RS-232-C receivers U21 and U18 [17A through 17D], and convert these into 8-bit bytes. These bytes are buffered in the FIFO receive buffer space corresponding to the channel. The next consecutive byte in the FIFO will contain status information (parity, framing, or overrun error or break detection overflow).

The MUX issues a time-out interrupt to the host every 16 msec. The host responds to this interrupt by checking each buffer for data. The data is then processed by the host and eventually executed as complete records.

The host transmits data to the MUX only if there is room in the transmit FIFO corresponding to a particular channel. When data appears in the transmit FIFOs, an interrupt is issued by the host to inform the card that buffer needs to be emptied (transmitted).

System Clocks

There are three synchronized system clocks (1.8432 MHz, 3.864 MHz, and 7.3728 MHz) on the MUX. All three clocks are derived from the 7.3728 MHz crystal oscillator [23D]. These clocks are completely independent of the host computer clock. Each of the three clocks is used to drive a different function as follows:

- 1.8432 MHz (PHI2) clock provides output to the CLK/TRG pins on the CTCs which generate baud rates and system timing intervals.
- 3.6864 MHz (PHI, PHI1) is used to provide a system clock to the Z-80A CPU, SIOs, and the CTCs, and is also used in the shared memory circuitry.
- 7.3728 MHz (2PHI) is used in the shared memory circuitry.

Shared Memory Controller

The shared memory controller circuitry (see sheet 3, 7-1) arbitrates the RAM resources on the MUX between the Z-80A CPU and the host CPU. The 2K byte RAM uses shared data and shared address busses; the memory controller decides who has control of the busses at any given time.

If the Z-80A CPU requests a memory cycle when the host is accessing memory, the Z-80A will remain in the wait cycle of its memory fetch until the host has completed its access.

The timing for the memory controller is based on the 7.37 MHz and the 3.68 MHz system clocks and is shown in figure 3-2.

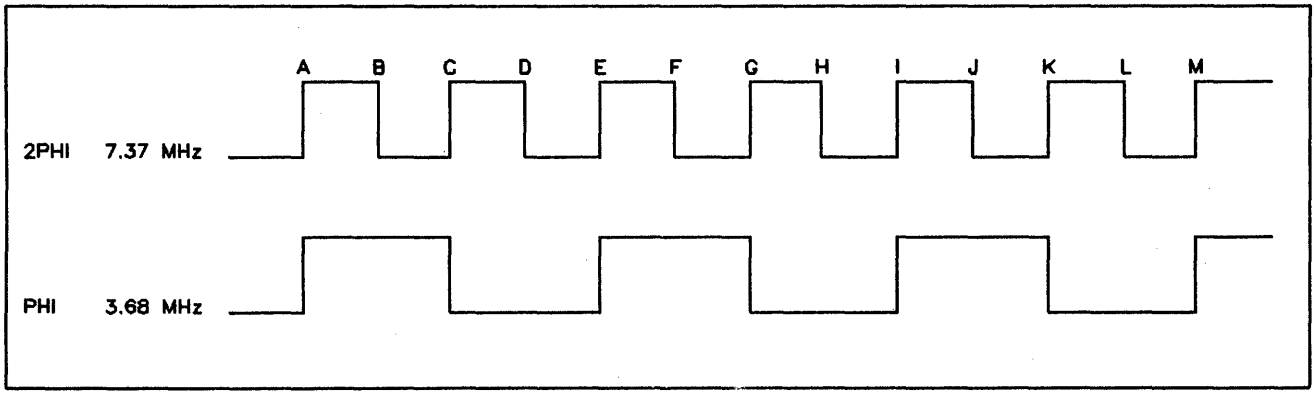


Figure 3-2. Memory Controller Timing

The ACCESS SELECT flip-flop, U15 [36D] samples the host request line on alternate falling edges of the 7.37 MHz clock (edges D, H, and L on figure 3-2). This flip-flop determines who has control of the shared memory busses at a given time. If the host has not requested memory when the access is sampled, the Z-80A CPU will get control by default.

At the falling edge of the 3.68 MHz clock (edges C, G, and K), the address from the selected processor and BW/R signal (from the host) is latched. At the rising edge of the 3.68 MHz clock (edges A, E, and I), the memory request line of the selected processor is sampled by the first flip-flop, U15 [36D] of the shared memory timing chain. If shared memory is requested, this flip-flop will start a shared memory cycle.

The following events will occur during a shared memory cycle:

1. The clocks to the ACCESS SELECT flip-flop and the address latches are disabled to prevent the other processor from interrupting the memory cycle.

2. The shared WRITE line is enabled.

3. The shared memory address decoder is enabled.

4. The data bus transceiver corresponding to the appropriate processor is enabled.

5. If the Z-80A is selected, the Z-80A WAIT- line is selected.

The next positive-going edge of the 3.68 MHz clock will set the second flip-flop [37D] in the shared memory timing chain. This inhibits the shared memory WRITE signal and generates the DTACK- signal if the host requested memory.

When the processor that requested the shared memory cycle releases its shared memory line, its data bus transceiver is disabled. The next positive edge of the 3.68 MHz clock will then set the first flip-flop in the timing chain. This re-enables host requests by setting the mainframe request enable flip-flop, releasing the Z-80A read latch, and clearing the second flip-flop in the timing chain.

A host shared memory write consists of the following events:

1. The host addresses the card (BAS = 0, BA16-BA20 = select code of card). See [31A]. This sequence enables the MYAD- signal. When the host generates its data strobe (BLDS), the host will request shared memory assuming a memory cycle is not already in progress.

2. At the falling edge of the 2 PHI clock, the ACCESS SELECT flip-flop is set. This selects the host address on the shared address bus.

3. At the next falling edge of PHI1, the address will be latched along with the BR/W line. The BR/W line (DIR) will set the direction for the data bus transceiver and enable a write to RAM.

4. At the next falling edge of PHI1, the first flip-flop of the timing chain is cleared, thus starting a shared memory cycle. This causes the SWR- line to go low and the SMREQ line to go high. Assuming a host write to legal shared RAM space (address >= 8000H), the RAM will now be fully enabled for a write cycle. The data bus transceiver will also be enabled.

5. At the next rising edge of PHI1, the second flip-flop in the timing chain will change state, thus inhibiting the SWR- line to RAM, which terminates the write. The DTACK- signal is also enabled to the host.

6. The host will end the cycle by releasing the BLDS- line. This will cause the mainframe shared memory request line (ENMDATA-) to disable the data bus transceiver.

7. At the next positive edge of PHI1, the shared memory timing flip-flops will return to the idle state. The ACCESS SELECT flip-flop and address latches will be re-enabled.

Z-80A Shared Memory Read

The following events occur during a Z-80A shared memory read. Refer to the timing diagram of figure 3-2 for additional information.

1. The Z-80A requests memory in the RAM address space (ZA15 = 0). This generates a shared memory request (SMREQZ = 1).

2. By default, the ACCESS SELECT flip-flop has selected the Z-80A to control the shared busses.

3. At the next negative edge of PHI, the Z-80A address bus is latched, thus creating the shared memory address.

4. At the next rising edge of PHI1, the first flip-flop in the timing chain is cleared, thus starting a shared memory cycle. This enables the Z-80A data bus transceiver between the ZD and SD busses, and releases the WAIT- line to the Z-80A CPU.

5. When the read cycle is complete, signal ZMREQ- goes high, thus disabling the Z-80A data bus transceiver.

6. At the next positive positive edge of PHI1, the shared memory timing flip-flops return to the idle state. The ACCESS SELECT flip-flop and address latches are re-enabled.

If a memory cycle is already in progress when a processor tries to request shared memory, that processor will be held off via WAIT- (Z-80A CPU) or DTACK- (host CPU) until it can get access to shared memory.

Memory Address Space

The 64K byte-portion of host memory assigned to the Z-80A is divided into several sections as shown in figure 3-3. The 2K bytes of RAM located on the card are shown in figure 3-4.

As you can see from figure 3-3, the addressing space is divided into three major areas: EPROM (program space), RAM space, and hardware register space. The contents of the MUX RAM, U55 [27E] and hardware registers (Semaphore register, U16 [24B]; Reset ID register, U38 and U75 [23B]; and Interrupt register, U38 and U73 [23C]) exist in shared memory, thus the host can address them. Note that the Z-80A and host addresses on figure 3-3 are different to access the same location. To convert a Z-80A address to a host address, shift the bits left one location and add one. For example, to address the first location in RAM, the Z-80A address is C000, but the host address is 8001.

Interface Registers

All communication between the host and the MUX card is performed by passing information between several interface registers. These interface registers consist of the three hardware registers (Reset ID, Interrupt, and Semaphore), and RAM locations which are called registers. All of these registers are described in Chapter 4, Programming.

Reset

On power-up, the host pulls (sets to low) the RESET- line to the I/O cards. On the MUX card, this resets the Z-80A, causing its program counter to reset and begin execution of the self-test routine.

The RESET- line also clears the RESET flip-flop, U38 [34A], which is normally used to initiate a software reset. (Clearing this register would normally cause a Z-80A Non-Maskable Interrupt (NMI), but the NMI input is edge sensitive and will not see the edge during a power-on reset.)

See Chapter 4 for information on a programmed reset.

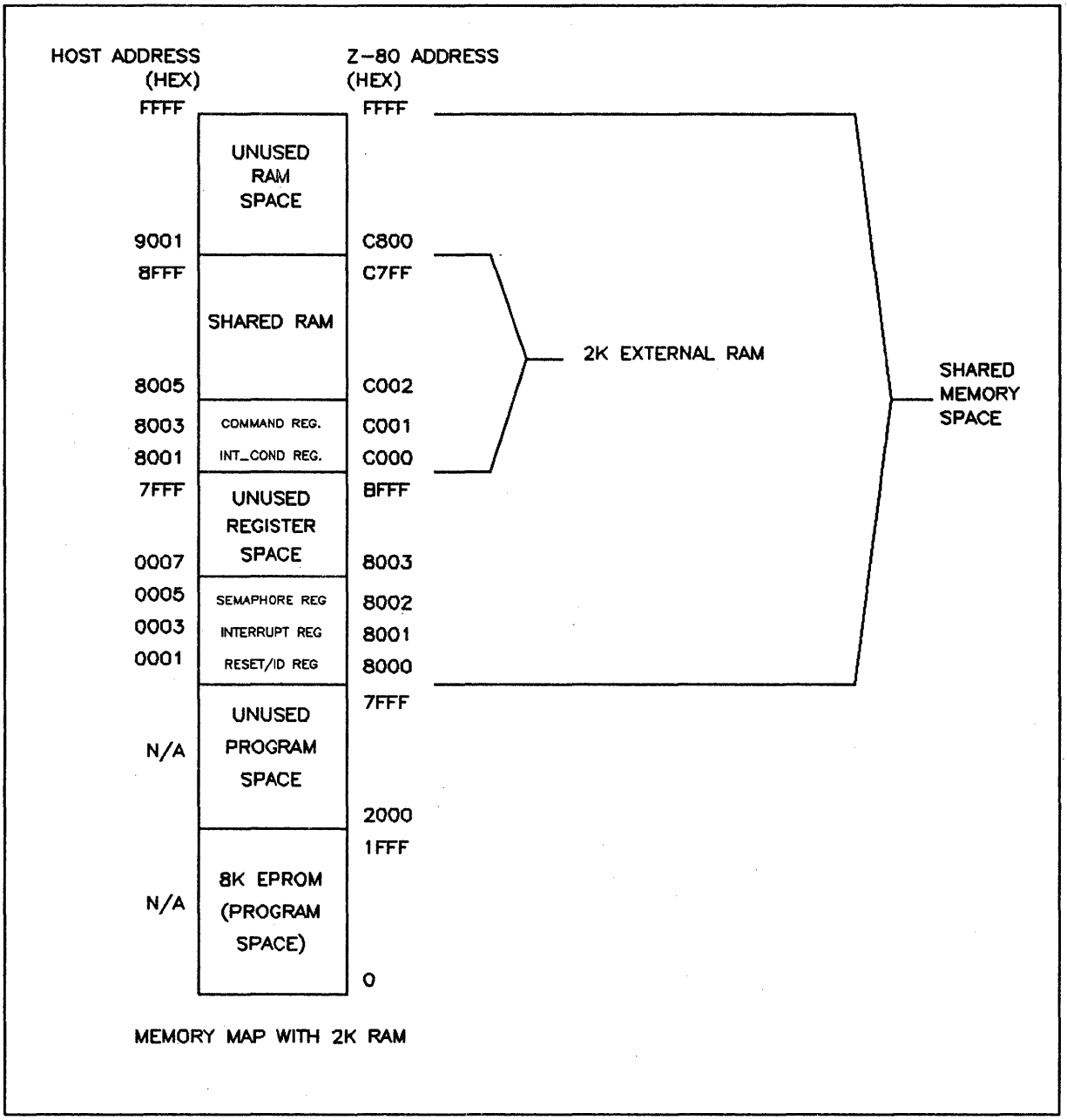


Figure 3-3. 64K Byte Addressable Memory Map

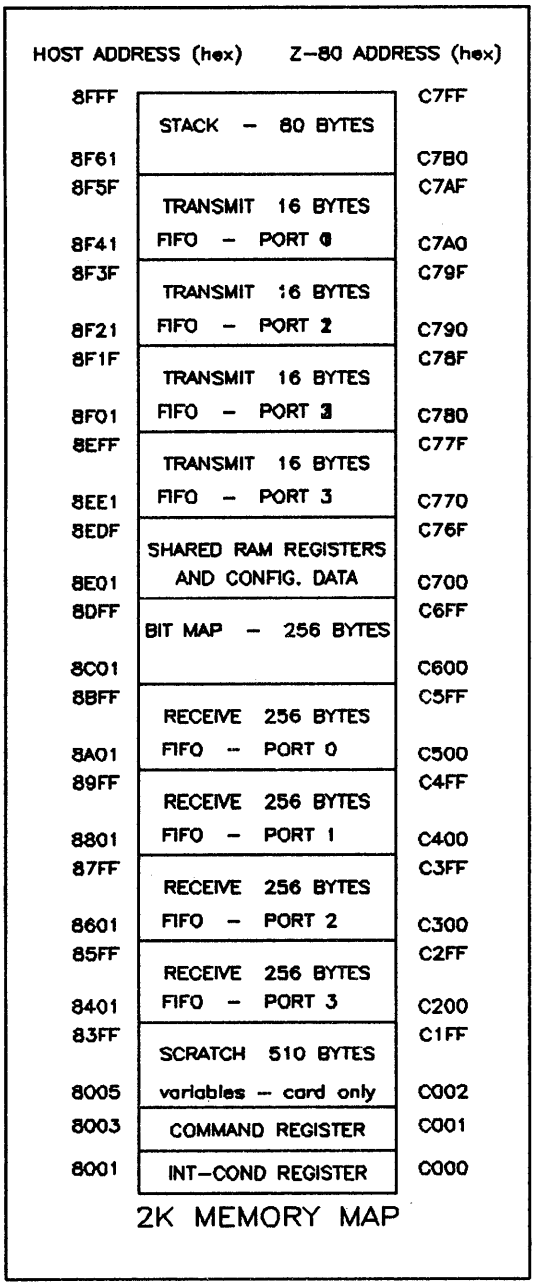


Figure 3-4. 2K Byte RAM Memory Map

Modem Lines

Port 0 on the MUX card supports seven modem control lines, in addition to two data lines (send and receive) and a signal ground. Of the seven control lines, four are input and three are output. Refer to the paragraph "*SIO/2 (Serial I/O Controller)*" for information on the SIO lines that correspond to the modem control lines.

The lines are summarized in table 3-1.

Table 3-1. Modem Lines

TWO CHARACTER MNEMONIC	ALTERNATE MNEMONIC	DESCRIPTION	INPUT/ OUTPUT
RD	Rx	RECEIVED DATA	INPUT
SD	Tx	TRANSMITTED DATA (SEND DATA)	OUTPUT
RS	RTS	REQUEST TO SEND	OUTPUT
TR	DTR	DATA TERMINAL READY	OUTPUT
CS	CTS	CLEAR TO SEND	INPUT
RR	CD	RECEIVED LINE SIGNAL DETECT (RECEIVER READY)	INPUT
DM	DSR	DATA SET READY (DATA MODE)	INPUT
SR	SR	FREQUENCE SELECT (SIGNAL RATE)	OUTPUT
IC	RI	RING INDICATOR (INCOMING CALL)	INPUT
SG	GND	SIGNAL GROUND	

I/O Address Space

The Z-80A provides addressing capability for 256 distinct I/O port registers. The MUX addressin assignments are shown in table 3-2.

SIO/2 (Serial I/O Controller)

The SIO/2 is a programmable serial I/O controller with two independent full-duplex channels with separate control and status lines. Each channel can be independently programmed. The MUX has two SIO/2s, with each channel used as a fully programmable asynchronous terminal controller.

Each SIO channel has two I/O addressable ports. One bi-directional port is for data transfer, and the other is for control information. The assigned SIO lines are described in table 3-3.

CTC (Counter Timer Circuit)

A Z-80A CTC (Counter Timer Circuit) provides four independent counter/timer channels. Three of these timers can supply outputs for other devices, and the fourth channel can only cause an interrupt to the Z-80A CPU. The MUX card uses two CTCs, which supply four timer outputs and four additional interrupt-only timers. The assigned uses of the CTC timer outputs are shown in table 3-4.

Priority Interrupt Structure

All I/O devices connected to the MUX card can interrupt. These interrupts are prioritized using the standard Z-80A priority chain. The MUX card interrupt priority structure is shown below.

```
Highest Priority  -  SIO Number 0, Channel A Receiver
        |         -  SIO Number 0, Channel A Transmitter
        |         -  SIO Number 0, Channel A External/Status
        |         -  SIO Number 0, Channel B Receiver
        |         -  SIO Number 0, Channel B Transmitter
        |         -  SIO Number 0, Channel B External/Status
        |         -  SIO Number 1, Channel A Receiver
        |         -  SIO Number 1, Channel A Transmitter
        |         -  SIO Number 1, Channel A External/Status
        |         -  SIO Number 1, Channel B Receiver
        |         -  SIO Number 1, Channel B Transmitter
        |         -  SIO Number 1, Channel B External/Status
        |         -  CTC Number 1, Counter/Timer Channel 2
Lowest Priority   -  CTC Number 0, Counter/Timer Channel 2
```

Note that the host interrupts to the Z-80A have the priority corresponding to CTC Number 0, Channel 2.

Table 3-2. I/O Address Space

I/O ADDRESS SPACE								
BITS								
7	6	5	4	3	2	1	0	DEVICE
0	1	1	1	X	X	0	0	SIO 0 CHANNEL A DATA
0	1	1	1	X	X	0	1	SIO 0 CHANNEL A CONTROL
0	1	1	1	X	X	1	0	SIO 0 CHANNEL B DATA
0	1	1	1	X	X	1	1	SIO 0 CHANNEL B CONTROL
1	0	1	1	X	X	0	0	SIO 1 CHANNEL A DATA
1	0	1	1	X	X	0	1	SIO 1 CHANNEL A CONTROL
1	0	1	1	X	X	1	0	SIO 1 CHANNEL B DATA
1	0	1	1	X	X	1	1	SIO 1 CHANNEL B CONTROL
1	1	0	1	X	X	0	0	CTC 0 CHANNEL 0
1	1	0	1	X	X	0	1	CTC 0 CHANNEL 1
1	1	0	1	X	X	1	0	CTC 0 CHANNEL 2
1	1	0	1	X	X	1	1	CTC 0 CHANNEL 3
1	1	1	0	X	X	0	0	CTC 1 CHANNEL 0
1	1	1	0	X	X	0	1	CTC 1 CHANNEL 1
1	1	1	0	X	X	1	0	CTC 1 CHANNEL 2
1	1	1	0	X	X	1	1	CTC 1 CHANNEL 3

Table 3-3. SIO Lines

SIO	CHANNEL	SIO LINE	SYMBOL	DESCRIPTION
0	A	RTS-	RS	Request To Send (modem output)
0	A	DTR-	TR	Terminal Ready (modem output)
0	A	CTS-	CS	Clear To Send (modem input)
0	A	DCD-	RR	Data Carrier Detect (modem input)
0	A	SYNC-	DM	Data Mode (modem input)
0	B	RTS-	SR	Signal Rate Generator (modem out)
0	B	CTS-	HD1	Hood Detect - port 1
0	B	DCD-	IC	Ring Indicator (modem input)
1	A	CTS-	HD2	Hood Detect - port 2
1	B	RTS-		Enable Frontplane Drivers
1	B	CTS	HD3	Hood Detect - port 3

Table 3-4. CTC Timer Outputs

CTC NO.	CTC NO.	EXT. CLOCK SOURCE	TIMER OUTPUT MNEMONIC	DESCRIPTION
0	0	PHI2	BRG0	Channel 0 baud rate clock
0	1	PHI2	BRG1	Channel 1 baud rate clock
0	2	PHI	INTERNAL	Host interrupt line
0	3	PHI	INTERNAL	Unused
1	0	PHI2	BRG2	Channel 2 baud rate clock
1	1	PHI2	BRG3	Channel 3 baud rate clock
1	2	PHI	INTERNAL	Time-out timer
1	3	PHI	INTERNAL	Unused

Chapter 4
Programming

Firmware on the MUX card is contained in a 4K byte EPROM. Features of the MUX firmware are as follows:

- Character recognition via a host-controlled bit map
- Break detection
- Break generation via host command
- Receive data 16-millisecond continuous time-out timer
- 128-character Receive buffers and 16-character Transmit buffers for each of the four channels
- Baud rates supported: 110, 134.5, 150, 300, 600, 1200, 2400, 4800, 9600, 19200
- Parity checking: odd, even, or none
- Number of stop bits: 1 or 2
- Number of data bits per character: 7 or 8
- Full-duplex transmission mode

OVERVIEW OF SHARED MEMORY FIRMWARE SCHEME

Data is passed between the MUX card and the host computer in circular FIFO buffers. There are eight of these buffers: four Receive buffers (one for each port), and four Transmit buffers (one for each port). These buffers are not hardware buffers, they are RAM locations which are accessed by both the card and the host. This shared memory scheme thus allows four basic types of memory accesses (see figure 4-1).

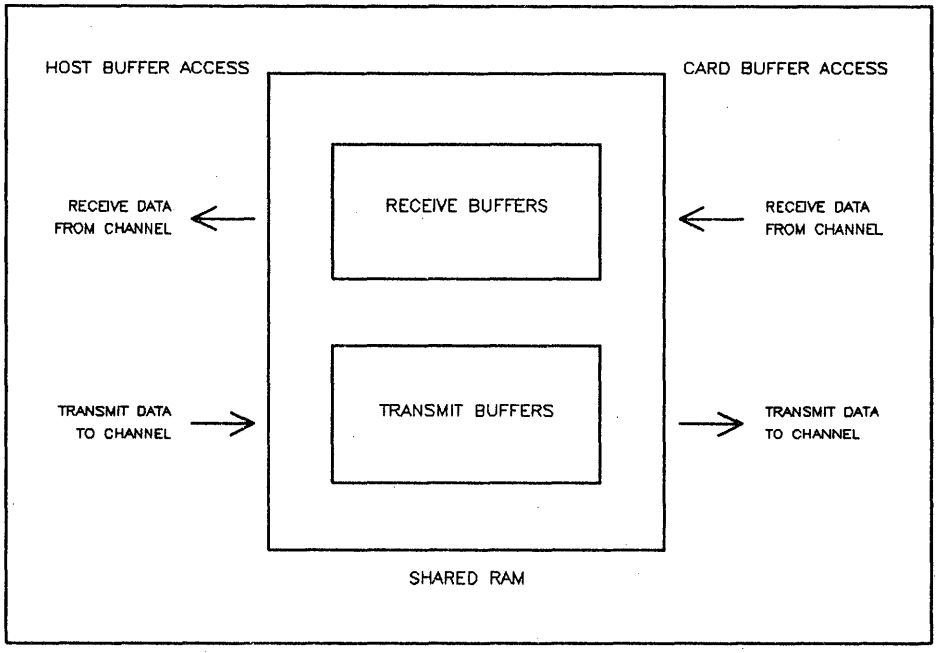


Figure 4-1. RAM Transmit and Receive Buffers

PASSING DATA BETWEEN MUX CARD AND HOST

The following paragraphs contain a general overview of how transmit and receive data is passed between the MUX and the host computer. Note that receive data is defined as data from a peripheral device to the MUX card and from there to the host computer; transmit data is defined as data from the host to the MUX card and from there to the peripheral device.

Receive Data From Channel

There are two basic parts to receive data processing: Putting receive data into the Receive buffers (card processing), and removing the data from the buffers (host processing).

When a character arrives from the peripheral device, the card retrieves it from the line receiver, and checks its bit map to determine if it is to be processed as a special character (see the paragraph "*Bit Map Format and Accessing*" for information on bit map checking). If the character is a special character, the card will send a Special Character interrupt to the host (see the paragraph "*Interrupts*" for information on interrupts). The card then writes the character to the Receive FIFO buffer for the appropriate port.

Each character written to the Receive buffers has an accompanying status byte. The status byte indicates whether a framing error, parity error, transceiver overrun error, buffer overflow error, or break occurred at the character.

The host is notified of data in the Receive buffers by time-out interrupts. During card initialization, the host sends a Start Timer interrupt, and the card begins a timer (time-out length is 16 milliseconds). When the timer goes off, the card sends the host a Time-Out interrupt and resets the timer. The host clears any data in the buffers and waits for the next Time-Out interrupt. (The host, therefore, reads data in the Receive buffers every 16 milliseconds.)

Transmit Data to the Channel

When the host has transmit data to send, it first checks if the Transmit buffer is full. If it is full, the host will wait for a TX Buffer Empty interrupt from the card. If the buffer is not full, the host places characters in the buffer until the buffer is full or the transmission is finished. If the buffer was empty, after the host has put the character in the buffer, the host will send a TX Buffer Not Empty interrupt to the card indicating that now there is data in the buffer.

When the card receives the TX Buffer Not Empty interrupt from the host, it begins to empty the Transmit buffer. When the card finishes emptying the buffer, it sends a TX Buffer Empty interrupt to the host. The host ignores this interrupt if it does not have data to send.

Firmware Priority Scheme

All firmware events are interrupt driven; therefore, the priority of these events is largely dependent on the priority of the SIO and CTC channels and their placement on the interrupt daisy chain. The priority order of the major firmware events are listed below:

1. RECEIVE DATA - PORT 0
2. TRANSMIT DATA - PORT 0
3. MODEM LINE CHANGES - CS, DM, and RR
4. RECEIVE DATA - PORT 1
5. TRANSMIT DATA - PORT 1
6. MODEM LINE CHANGES - IC
7. RECEIVE DATA - PORT 2
8. TRANSMIT DATA - PORT 2
9. RECEIVE DATA - PORT 3
10. TRANSMIT DATA - PORT 3
11. TIMER INTERRUPT
12. HOST INTERRUPTS

INTERFACE REGISTERS

Interface registers consist of both hardware registers and RAM locations (also called registers). The interface registers are accessed by both the card and the host; all information between the card and the host is performed by passing information between these registers. (The FIFO buffers, although they also are RAM locations and are accessed by both the card and host, are not considered to be interface registers because they require special handshaking.)

Refer to Chapter 3, figure 3-4 for a RAM memory map.

NOTE

Technically, all of RAM is accessible by both the card and the host. However, a portion of RAM is reserved for card use only. Because there is no hardware protection mechanism for this portion of RAM, the host computer driver should be written such that these locations are not accessed.

Hardware Registers

Hardware registers on the MUX card are:

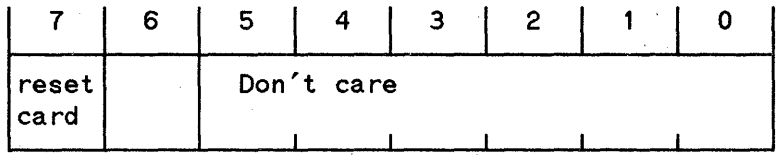
Reset/ID register
Interrupt register
Semaphore register

RESET/ID REGISTER.

Z-80 ADDRESS: 8000H
HOST ADDRESS: 0001H

The Reset/ID register is used to reset the card and to contain the card identification information. On the MUX card, using this register to reset the card causes a Non-Maskable Interrupt (NMI) to the Z-80. The NMI in turn causes a fetch at location 66 in ROM which contains a jump instruction to the Initialize routine. At the end of the initialize code is the wait loop the card performs while waiting for interrupts. In other words, on the MUX card, a card reset using this register will reinitialize the card but will *NOT* return to the code that was being executed at the time the NMI was issued.

In the following diagrams, the first figure shows the definition of the bit locations when a write is issued to this register. The second shows the bit definitions when a read is issued. Both the card and the host will have occasion to write to this register; however, only the host will have need to read it.



Bit 7: When set (1) the card is RESET and a nonmaskable interrupt is generated to the Z-80. This causes a jump to location 066H in ROM which is the beginning of the Z-80 initialization code. This bit must be cleared before another RESET can be issued.

Bits 0-6: Not defined

READ

7	6	5	4	3	2	1	0
Rem Cntl	Secondary ID	00	CARD ID 0	0	1	0	1

Bit 7: This bit is set or reset by the REMOTE/LOCAL switch (see Chapter 2). When this bit is set, it indicates that there is a system console hooked up to this card.

Bits 5,6: These bits constitute the card's Secondary ID. These bits are hardwired to 00.

Bits 0-4: These bits form the unique ID code of the MUX card. The MUX card ID is 5 and so these bits are hardwired as shown in the figure above.

INTERRUPT REGISTER

Z-80 ADDRESS: 8001H
HOST ADDRESS: 0003H

The Interrupt register is used to enable interrupts to the host and to reflect the interrupt priority of the card. After card initialization the card will not access the Interrupt register again. The host will write to bit 7 when it wants to enable or disable interrupts.

WRITE

7	6	5	4	3	2	1	0
Int Enbl	Don't care						

Bit 7: This bit enables and disables card interrupts to the host. When set (1), interrupts are enabled. When reset (0), interrupts to the host are disabled.

Bits 0-6: Not defined

READ

7	6	5	4	3	2	1	0
Int Enbld	Int Rqst	Interrupt Level		Undefined for this card			

Bit 7: This bit indicates the current status of the host Interrupt enable flip flop ('1'=enabled, '0'= disabled).

Bit 6: This bit is set when the card is requesting an interrupt and reset when it's not.

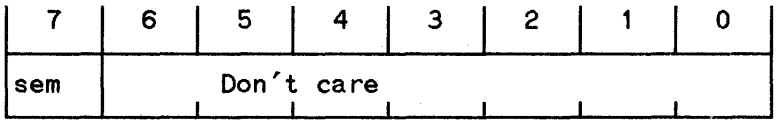
Bits 4-5: These bits indicate the interrupt level of this card. The interrupt level is set by the two interrupt level switches (see Chapter 2)

Bits 0-3: These bits are not defined for the MUX card (not used).

SEMAPHORE REGISTER

Z-80 ADDRESS: 8002H
HOST ADDRESS: 0005H

The Semaphore register is used by both the card and the host while sending and servicing interrupts generated by the interrupt registers (the INT-COND and COMMAND registers). The following is a description of the Semaphore register and an explanation of its use.



Bit 7: This bit gives the status of the semaphore: '0'=not busy, '1'=busy. The semaphore is automatically set after it is read.

Bits 0-6: These bits are not defined.

The Semaphore register is used by the card and the host to determine whether the shared RAM is currently available for access. The Semaphore register performs an indivisible read and set operation. When either the host or the card reads this register, bit 7 is set to indicate that a memory access is in progress. When the access is completed, the Semaphore register can be cleared by writing any value to it. Bits 0 to 6 are meaningless.

It should be noted that the Semaphore register does not perform any hardware lockout function. Its use is part of the backplane protocol. The Semaphore register will only be used when either the card or the host wants to access one of the interrupt registers (see the INT-COND and the COMMAND registers and their associated tables in the following paragraphs).

Registers with Interrupt Capabilities

There are two RAM registers which are capable of generating an interrupt when they are written to. These registers are used to send status and command information between the card and the host. Most of the software interfacing between the card and the host will be initiated through these registers. The following is a description of each. For further information on the interrupts each of these registers can generate, refer to the paragraph "*Interrupts.*"

COMMAND REGISTER

```
Z-80 ADDRESS:  C001H
HOST ADDRESS:  8003H

 WRITE:  HOST ONLY - GENERATES INTERRUPT TO THE Z-80

 READ :  CARD ONLY - TURNS OFF INTERRUPT
```

The COMMAND register is used to send commands and status information from the host to the card. When the host writes to this register, an interrupt to the Z-80 is generated. The interrupt informs the card that there is a command to be read in the COMMAND register. When the card reads the register, the interrupt line is automatically cleared.

The bits in the COMMAND register are used to identify the type of interrupt request. There are two types of interrupts generated by the host; port specific interrupts and non-specific interrupts. If the interrupt is port specific, i.e., it pertains to a particular port, a bit will be set in the COMMAND register to indicate which port. The actual interrupt information will be contained in a 4-byte table called the CMND-TAB. This table is discussed in detail in the paragraph "*Interrupts*".

Since non-specific interrupts do not concern a particular port, there is a bit reserved for them in the COMMAND register. The CMND-TAB is not accessed.

7	6	5	4	3	2	1	0
NOT USED	SELF TEST	TIMER ON/ OFF	MODM	PORT 3	PORT 2	PORT 1	PORT 0

COMMAND REGISTER

Bits 0-3: A '1' in any of these bit positions indicates that there is a port-specific interrupt for that port. The card will check the correct byte in the CMND-TAB to identify the interrupt.

Bit 4: A '1' in this bit position indicates that the host wants to change one of the modem output lines. The card will access the MODM-OUT register to determine which line to change.

Bit 5: A '1' in this bit position indicates that the host wants to turn off or on the 16 millisecond timer.

Bit 6: A '1' in this bit position indicates that the host wants the card to perform its self test.

INT-COND Register

```
Z-80 ADDRESS:  C000H
HOST ADDRESS:  8001H

WRITE: CARD ONLY - GENERATES INTERRUPT TO HOST

READ : HOST ONLY - CLEARS INTERRUPT
```

The INT-COND register is used to send status information and messages from the card to the host. When the card writes to this register, an interrupt to the host is generated. The interrupt informs the host that there is an interrupt to be read in the INT-COND register. When the host reads the register, the interrupt line is automatically cleared. The bits in the INT-COND register are used to identify the type of interrupt request.

As with the COMMAND register, there are two types of interrupts generated by the card; port specific interrupts and non-specific interrupts. If an interrupt is port-specific, a bit will be set in the INT-COND register to indicate which port the interrupt involves. The actual interrupt information is contained in a 4-byte table called the ICR-TAB.

Since non-specific interrupts do not concern a particular port, there is a bit reserved for them in the INT-COND register. The ICR-TAB is not accessed.

7	6	5	4	3	2	1	0
NOT USED	TIME OUT	MODM	ST DONE	PORT 3	PORT 2	PORT 1	PORT 0

INT-COND REGISTER

Bits 0-3: A '1' in any of these bit positions indicates that there is a port-specific interrupt for that port. The card will check the correct byte in the ICR-TAB table to identify the interrupt.

Bit 4: This bit is set after the card has finished self-test and card initialization. This interrupt notifies the host that it may now communicate with the card.

Bit 5: A '1' in this bit position indicates that that a change occurred on one of the input modem lines. The host will access the MODM-IN register to determine which line changed.

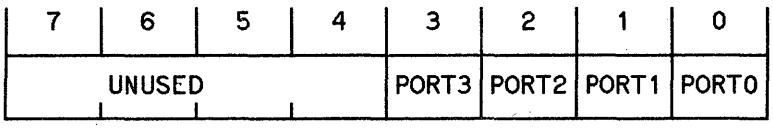
Bit 6: A '1' in this bit position means that the 16 millisecond Receive buffer timer has gone off. The host will respond by retrieving any characters that are in the four Receive buffers.

Special Character Bit Map Table

The bit map consists of 256 RAM locations, each byte representing one character. The first four bits in each byte correspond to the four ports on the card.

The purpose of the bit map is to enable the host to be notified immediately when a "special" character is received. The host defines a character as special by setting (within the byte representing the character) the bit representing the port.

When the card receives a character, it uses the character as an index into the bit map and checks the bit representing the port the character came from. If the bit is set, the card sends the host a Special Character interrupt. The following is an illustration of a bit map location.



NOTE

The host will set bits in the bit map dynamically. There is no handshaking with the card before making a change to the bit map.

Other Shared Memory Registers

There are a number of special purpose RAM locations which will be used to pass information between the host and the card. Table 4-1 contains a list of these shared RAM locations and a description of their usage.

Shared RAM registers

The following paragraphs contain a more detailed explanation of the uses of the shared RAM registers.

RECEIVE FIFO HEAD POINTERS. These pointers contain the index of the current head of the Receive buffers. The Receive buffer head pointers are updated by the host when it removes data from the Receive buffers.

RECEIVE FIFO TAIL POINTERS. These pointers contain the index of the current tail of the Receive buffers. The Receive buffer tail pointers are updated by the card when it places new data into the Receive buffers.

TRANSMIT FIFO HEAD POINTERS. These pointers contain the index of the current head of the Transmit buffers. The Transmit buffer head pointers are updated by the card when it removes data from the Transmit buffers.

Table 4-1. Shared Memory Registers

RAM REGISTER	DESCRIPTION	(IN HEX) Z-80 ADDRESS	(IN HEX) HOST ADDRESS
RHEAD-0	RECEIVE FIFO HEAD POINTER - PORT 0	C700	8E01
RHEAD-1	" - PORT 1	C701	8E03
RHEAD-2	" - PORT 2	C702	8E05
RHEAD-3	" - PORT 3	C703	8E07
RTAIL-0	RECEIVE FIFO TAIL POINTER - PORT 0	C704	8E09
RTAIL-1	" - PORT 1	C705	8E0B
RTAIL-2	" - PORT 2	C706	8E0D
RTAIL-3	" - PORT 3	C707	8E0F
THEAD-0	TRANSMIT FIFO HEAD POINTER - PORT 0	C708	8E11
THEAD-1	" - PORT 1	C709	8E13
THEAD-2	" - PORT 2	C70A	8E15
THEAD-3	" - PORT 3	C70B	8E17
TTAIL-0	TRANSMIT FIFO TAIL POINTER - PORT 0	C70C	8E19
TTAIL-1	" - PORT 1	C70D	8E1B
TTAIL-2	" - PORT 2	C70E	8E1D
TTAIL-3	" - PORT 3	C70F	8E1F
CONFIGURATION DATA REGISTERS:			
CONFG-0	LINE SPECS REGISTER - PORT 0	C710	8E21
BD-0	BAUD RATE INDEX - "	C711	8E23
CONFG-1	LINE SPECS REGISTER - PORT 1	C712	8E25
BD-1	BAUD RATE INDEX - "	C713	8E27
CONFG-2	LINE SPECS REGISTER - PORT 2	C714	8E29
BD-2	BAUD RATE INDEX - "	C715	8E2B
CONFG-3	LINE SPECS REGISTER - PORT 3	C716	8E2D
BD-3	BAUD RATE INDEX - "	C717	8E2F

Table 4-1. Shared Memory Registers (Continued)

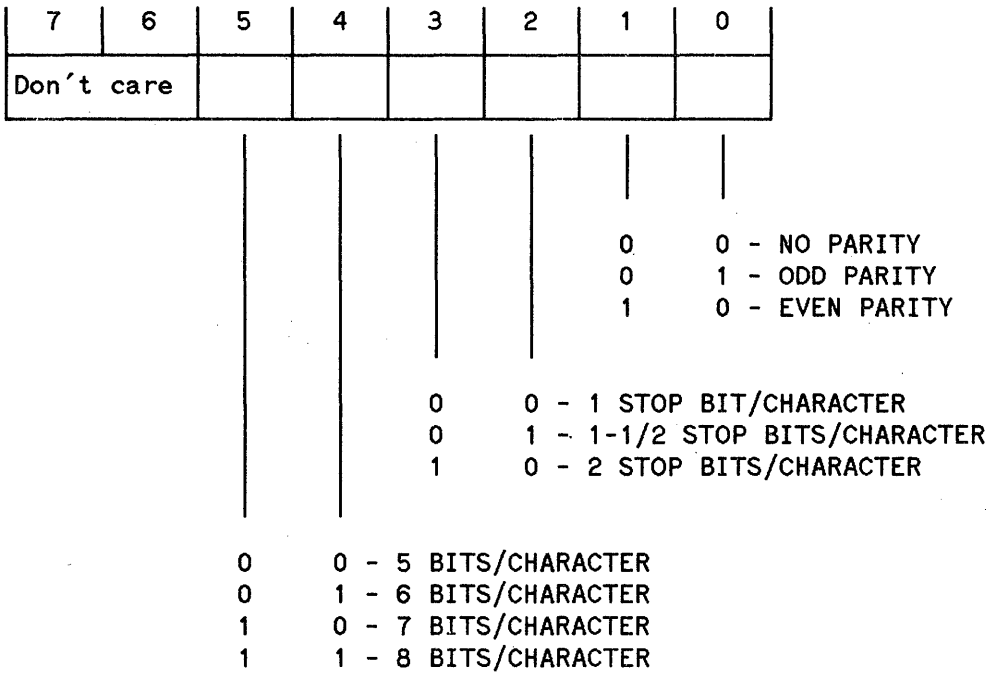
RAM REGISTER	DESCRIPTION	(IN HEX)	
		Z-80 ADDRESS	HOST ADDRESS
MODM-IN	MODEM INPUT LINES	C718	8E31
MODM-OUT	MODEM OUTPUT LINES	C719	8E33
MODM-MASK	MODEM MASK FOR INPUT LINES	C71A	8E35
CMND-TAB	COMMAND REG. INTERRUPT DATA 4 BYTES - 1 PER PORT	C71B	8E37
ICR-TAB	INTCOND REG. INTERRUPT DATA 4 BYTES - 1 PER PORT	C71F	8E3F
ST-COND	SELF TEST RESULT REGISTER	C723	8E47

TRANSMIT FIFO TAIL POINTERS. These pointers contain the index of the current tail of the Transmit buffers. The Transmit buffer tail pointers are updated by the host when it places new data into the Transmit buffers.

Configuration Data Registers

There are two bytes of configuration data for each port. The first byte (CONFG) is used to specify parity, bits per character, and number of stop bits per character for each port. The second byte, BD, contains a value which corresponds to the desired baud rate. Both registers are detailed in the following paragraphs.

CONFG REGISTER. This register is used to specify three pieces of configuration information; parity method, number of bits per character, and the number of stop bits per character. The card is capable of being programmed for the options shown below even though all the options are not supported.



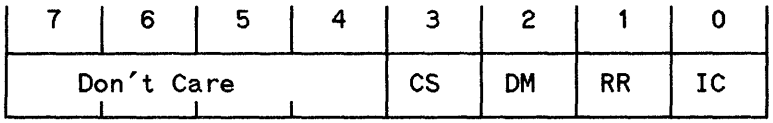
BD REGISTER. This register is used to indicate the baud rate the host wants the port set to. As with the options available in the CONFG register, not all of the available options are supported for the card. The options that are supported are listed at the beginning of this chapter and in table 1-1 in Chapter 1.

BD REGISTER VALUE (HEX)	BAUD RATE (BITS/SEC)
1	50
2	75
3	110
4	134.5
5	150
6	300
7	600
8	900
9	1,200
A	1,800
B	2,400
C	3,600
D	4,800
E	7,200
F	9,600
10	19,200
11	38,400

Modem Input Lines

The first four bits in the MODM-IN register are used to represent the four input modem lines. The remaining four bits are unused. The host will read this register when it wants to know the status of the input modem lines - i.e., which ones are on and which are off. The card will update this register when it receives notification of an input modem line change from the transceiver. If one of these lines change, the card will access the MODM-MASK register to see if the host wants to be interrupted for a change on that particular line. MODM-IN will always contain a copy of the current status of the input modem lines.

MODM-IN REGISTER

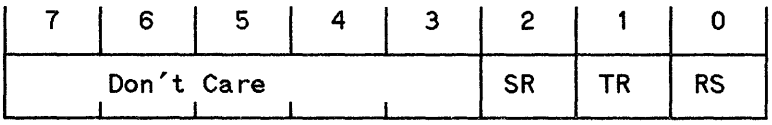


CS - Clear to Send
RR - Receiver Ready
IC - Incoming Call
DM - Data Mode

Modem Output Lines

The first three bits in the MODM-OUT register are used to represent the three output modem lines. The remaining five bits are unused. When the host wants to change a particular output modem line it will first write to this register, setting the appropriate bit position, then generate a Modem Output Change interrupt to the card. The MODM-OUT register will always contain the current status of the modem output lines.

MODM-OUT REGISTER



SR - Signal Rate Selector
TR - Terminal Ready
RS - Request to Send

Modem Mask Register

The first four bits in this register correspond to the first four bits in the MODM-IN register. The other four bits will be set. If there is a change on one of the input modem lines, this register will be used by the card to determine whether the host wants to be interrupted. If the bit in MODM-MASK corresponding to the input line is set, the card will send the host a Modem Input Change interrupt. If the bit is reset (0), the card will not send an interrupt. The format of the Modem Mask register exactly matches that of MODM-IN.

INT-COND Register Interrupt Data (ICR-TAB)

The INT-COND register interrupt data is contained in a 4-byte table which is used to identify port specific interrupts sent by the card to the host. This table is used in conjunction with the INT-COND register. Each of the bytes in the ICR-TAB is reserved for one of the 4 ports. When the card sends the host a port specific interrupt (one of the port bits (0-3) in the INT-COND register is set), the host will read the corresponding byte in ICR-TAB for the actual cause of the interrupt. See the paragraph "*Interrupts*" for more detail on ICR-TAB.

COMMAND Register Interrupt Data (CMND-TAB)

The COMMAND register interrupt data is also contained in a 4-byte table. It is used the same as the ICR-TAB except that it identifies port specific interrupts from the host to the card. The CMND-TAB is used in conjunction with the COMMAND register. See the "*Interrupts*" paragraph for more detail on CMND-TAB.

ST-COND Register

The ST-COND register is used to indicate the result of Self Test. It Self Test passed, ST-COND will contain the value E0H. If Self Test failed, the register contains the value of the IX register (internal to the Z-80) at the time of failure. This value indicates what routine Self-Test was executing when it failed. See Chapter 5 for additional information.

SHARED MEMORY ACCESS AND DATA FORMATS

There are 2K bytes of shared RAM on the MUX card. All of the communication between the card and the host will be via shared RAM (the INT-COND and COMMAND registers are part of the RAM address space). The following paragraphs describe shared memory access protocols, including a description of the FIFO buffers, receive and transmit data formats, FIFO pointer management, Transmit FIFO protocol, and Receive FIFO protocol.

Bus Arbitration

The host and the card will alternate RAM accesses when they both need the bus at the same time. This is accomplished in the hardware. As a result, if both the card and the host try to access RAM at the same time, the host will get the bus for one memory access, then the card. In a worst case situation the host and the card will have to wait one RAM cycle between each memory access.

There is one exception to the above. Both the card and the host will use the Semaphore register to lock each other out when sending or responding to card-to-host or host-to-card interrupts. These interrupt processes are critical regions for both the host and the card and, as such, will be protected by mutual use of the Semaphore register. The use of the Semaphore register in the interrupt processes is described in the paragraph "*Interrupts*".

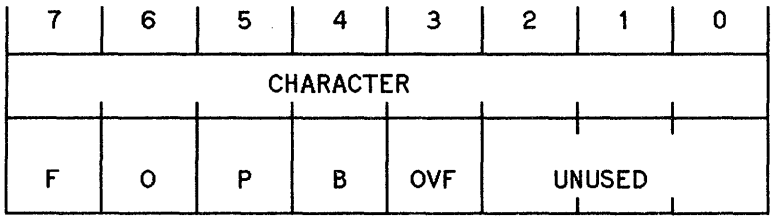
Pointer Management – Receive and Transmit Buffers

Recall that there are a total of eight buffers, each organized as a circular FIFO queue: one Receive buffer and one Transmit buffer for each of the four ports. There are two pointers associated with each of the buffers: a *head* pointer and a *tail* pointer. Both of these pointers are indexes from a base FIFO address. The base address is hard-coded.

The management of the head and tail pointers is the responsibility of both the card and the host. The card will be adding data to the Receive buffers and removing data from the Transmit buffers. Therefore, it will be responsible for updating the Receive buffer Tail pointers and the Transmit buffer Head pointers. Conversely, the host will be removing data from the Receive buffers and adding data to the Transmit buffers. It will be responsible for updating the Receive buffer Head pointers and the Transmit buffer Tail pointers.

Receive Data Format

The receive data format scheme requires two bytes per character. The first byte will be the character and the second byte will be the status byte which contains error information and break detection. The data format is illustrated below:



1. (F) Framing Error - This is to notify the host that a framing error occurred on this character.

2. (O) Overrun Error - This is to notify the host that a UART overrun condition occurred on this character.

3. (P) Parity Error - This is to notify the host that a parity error occurred on this character.

4. (B) Break Detection - This is to notify the host that a Break was received. The character will be null.

5. (OVF) Overflow Error - This is to notify the host that a Receive buffer overflow condition occurred before this character.

Receive FIFO Buffer Management

Recall that there are four receive buffers, one for each port. They are organized as circular FIFO data structures of 256 bytes each. As each character requires 2 bytes, this is enough buffer space for 128 characters per port.

TIME-OUT TIMER FOR RECEIVE CHARACTERS. Recall that the card will interrupt the host every 16 milliseconds. The host will respond to this interrupt by emptying all of the characters in the four Receive buffers. The host turns on the timer during boot-up and the timer will cycle continuously whether there is Receive data in the buffers or not. The host does have the option to turn off the timer if it so desires by sending a Timer Off/On interrupt. This interrupt is discussed in more detail under the paragraph *Interrupts*.

CARD PROCESS FOR RECEIVE BUFFER MANAGEMENT. The card will only access the Receive FIFO buffers when a Receive character has arrived at a port. When a character arrives the following sequence of events is performed by the card.

1. Check if the buffer is full. If so, the card will simply exit this routine without retrieving the character from the transceiver.

NOTE

The transceiver has a 3-byte internal buffer which insures protection in the event the Receive buffer is full. However, if there is still no room in the Receive buffer when the fourth character arrives, the transceiver will overrun. It is the responsibility of the host to service the buffer enough to prevent this occurrence. There will be no overrun prevention done on the card.

2. Retrieve the character from the transceiver.
3. Strip any parity bits.
4. Create the status byte.
5. Check the Bit Map location for the character. If the correct bit is set, it identifies the character as a "special character" and the card sends a Special Character interrupt to the host.
6. Write both the character and the status byte to the FIFO buffer and update the appropriate pointers.

HOST PROCESS FOR RECEIVE BUFFER MANAGEMENT. The host will only access the Receive FIFO buffers after it receives a Time-Out interrupt from the card. The Time-Out interrupt will occur every 16 milliseconds whether there is data in the Receive buffers or not. Upon receipt of the interrupt, the host will begin checking and emptying all four Receive buffers. The host will perform the following sequence of events for each Time-Out interrupt.

For each buffer -

1. If head=tail then exit (buffer empty), else . . .
2. Retrieve data byte and status byte.
3. Update buffer pointers.

4. Begin sequence again.

Transmit Data Format. There is no special transmit data format: because there is no status byte associated with transmit data, the Transmit buffers will simply contain characters to transmit.

Transmit FIFO Buffer Management. Recall that there are four Transmit buffers, one for each port. They are organized as circular FIFO queues of 16 bytes each, one byte per character.

CARD PROCESSING FOR TRANSMIT BUFFER MANAGEMENT. The card begins to send transmit data out the port after it receives a TX Buffer Not Empty interrupt from the host informing it that the transmit buffer for the port is no longer empty. The card starts the transceiver and begins sending out characters. The card performs the following sequence of events.

1. If head=tail then exit (buffer empty) else. . .

2. Retrieve character and send to the UART.

3. Update necessary pointer(s).

HOST PROCESSING FOR TRANSMIT BUFFER MANAGEMENT. The host will add data to the Transmit buffers whenever it has the need unless the intended buffer is full. If the host encounters a full buffer, it will hold off and wait for a TX Buffer Empty interrupt from the card. The TX Buffer Empty interrupt informs the card that there is now room in the Transmit buffer for more characters.

If the buffer is empty when the host wants to put characters in, the host will send the card a TX Buffer Not Empty interrupt. This interrupt tells the card that there are now more characters to send to the transceiver. The following is the sequence of events the host executes for each character it wants to place in a Transmit buffer.

1. Is the Transmit buffer full? If yes, exit routine.

2. Is the Transmit buffer empty? If yes, send a TX Buffer Not Empty interrupt to the card.

3. Do the following until either finished or buffer full

    a. Put character into buffer
    b. Update pointer.

INTERRUPTS

This discussion on interrupts is divided into two general parts: First is an overview of the Interrupt sending and receiving process between the card and the host. Second is an explanation of each of the possible card-to-host and host-to-card interrupts.

NOTE

Both the host and the card will assume that there may be more than one bit set (more than one interrupt) in the Interrupt register when the actual interrupt signal is received. This is the reason that a bit is reserved for each type of interrupt instead of using a value to represent a particular interrupt.

Interrupt Sending and Receiving – Semaphore Register

The interrupt process between the host and the card is critical to both and, as such, cannot tolerate a possible interleaving of memory accesses. As a result, the Semaphore register is used by both the card and the host as notification that a critical process is being performed.

Whenever either the host or the card is sending or receiving an interrupt, both will check the Semaphore register before accessing the Interrupt register. If bit 7 in the Semaphore is "0", the Interrupt registers are not being accessed and the host or the card (whichever is checking the register) may proceed. If bit 7 is "1", the host or the card is in the critical region. The entity wishing to begin must wait. For example, if the host wants to send an interrupt to the card, it will first check the Semaphore register. If bit 7 in the Semaphore register is set, the card is in the process of accessing one of the Interrupt registers. The host will wait for the Semaphore register to be cleared before sending the interrupt.

Host-to-Card Interrupts

Host-to-card interrupts are generated when the host writes to the COMMAND register. As mentioned previously, if the interrupt is port-specific, the bit in the COMMAND register indicating the port will be set, and the bit in CMND-TAB indicating the interrupt will be set. In other words, if the interrupt is port-specific the card will check the corresponding byte in CMND-TAB for the interrupt. If the interrupt is not port-specific, CMND-TAB will not be accessed.

COMMAND REGISTER

{non-specific}{port-specific}

7	6	5	4	3	2	1	0
xxx	ST	TME	MOD	P3	P2	P1	P0

CMND-TAB

7 - 3	2	1	0
UNUSED	BRK	TX	CON
"	BRK	TX	CON
"	BRK	TX	CON
"	BRK	TX	CON

NON-SPECIFIC INTERRUPTS

1. MODEM OUTPUT CHANGE (MOD) - This interrupt is used in conjunction with the MODM-OUT register. The host will generate this interrupt when it wants the card to change one or more of the modem output lines. After receiving this interrupt, the card will read the MODM-OUT register and set the indicated modem lines.

2. TIMER OFF/ON (TME) - This interrupt is used to toggle the timer on and off. If the timer is on when this interrupt is received, the card will turn the timer off. If the timer is off, the card will turn it back on again.

3. SELF TEST ON (ST) - This interrupt tells the card to begin self-test. The purpose of this interrupt is to give the host the capability of dynamically invoking self-test without having to power the system down and back up.

CAUTION

It is critical that the host does not interrupt the card after invoking self-test until the card sends a Self-Test Done interrupt.

PORT-SPECIFIC INTERRUPTS

1. CONFIGURATION DATA CHANGE (CON) - This interrupt informs the card that the host has changed the configuration data for the indicated port. Configuration data includes line characteristics and baud rates for the specified channels. The card will respond to this interrupt by changing the line configuration and baud rate as specified in the CONFG and BD registers.

NOTE

The host waits for the TX buffer to be empty before sending this interrupt so that there is no timing collision.

2. TRANSMIT BUFFER NOT EMPTY (TX) - This interrupt tells the card that the host has put data into a previously empty Transmit buffer. Upon receipt of this interrupt, the card will start the transceiver and begin retrieving characters from the Transmit buffer.

NOTE

This interrupt is identified and processed after the configuration interrupt so that no transmit data is sent until the card has completely finished changing the line configuration for the port.

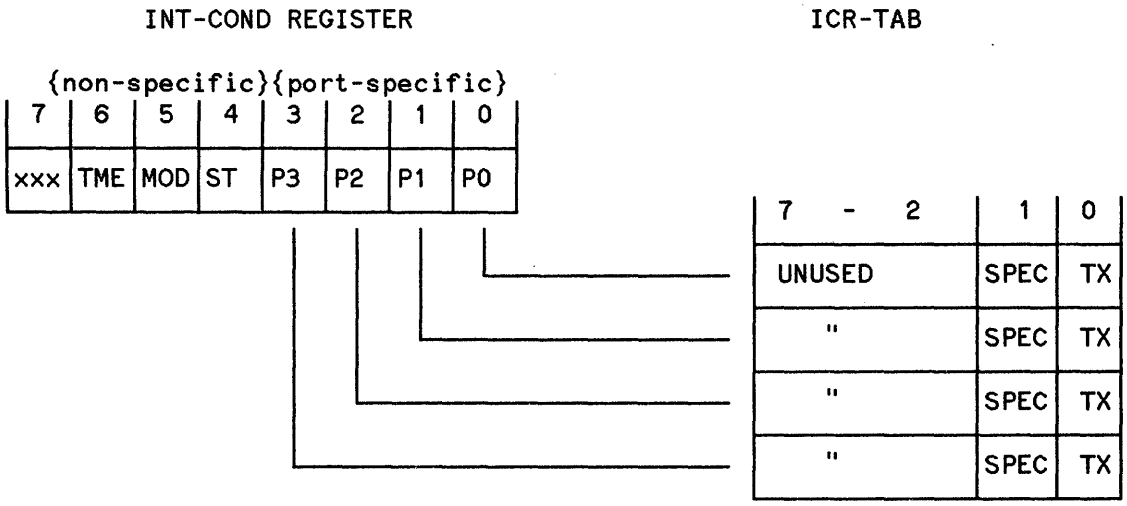
3. SEND BREAK (BRK) - This interrupt works as a toggle. The first time it is sent, it informs the card to send a break on the port specified. The break condition remains until the card receives this interrupt a second time which tells it to stop the break.

NOTE

The host waits for the TX buffer to be empty before sending the interrupt so that there is no timing collision.

Card-to-Host Interrupts

Card-to-host interrupts are generated when the card writes to the INT-COND register. As mentioned previously, if the interrupt is port-specific, the bit in the INT-COND register indicating the port will be set and the bit in ICR-TAB indicating the interrupt will be set. In other words, if the interrupt is port-specific the host will check the corresponding byte in ICR-TAB for the interrupt. If the interrupt is not port-specific, ICR-TAB will not be accessed.



NON-SPECIFIC INTERRUPTS

1. TIMER (TME) - The card will send the host a Time-Out interrupt every 16 milliseconds. This signals the host to come retrieve any characters that might be in the Receive buffers. The host will respond to this interrupt by checking to see if the buffers are empty, then retrieving all characters from the Receive buffers that are not empty.

2. MODEM INPUT CHANGE (MOD) - This interrupt is used in conjunction with the MODM-IN and the MODM-MASK registers. The card will send this interrupt to the host when there has been a change in one of the modem lines indicated by the MODM-MASK register. If there is a change in a modem line whose corresponding bit in the MODM-MASK is not set, the card will not issue this interrupt.

3. SELF TEST COMPLETE (ST) - This interrupt informs the host that the card has completed self-test. The host will check the ST-COND register to determine whether self-test passed or failed. If self-test passed, it also means that the card is initialized and ready for processing.

PORT-SPECIFIC INTERRUPTS

1. SPECIAL CHARACTER RECEIVED (SPEC) - This interrupt is sent when the card receives a character whose bit position in the Bit Map was set. Possible special characters might be XOFF, XON, etc. As mentioned previously, the host is responsible for designating which characters are special.

2. TRANSMIT BUFFER EMPTY (TX) - This interrupt informs the host that the Transmit buffer for the port indicated is now empty. When the host wants to send the card a character but finds the Transmit buffer full, it will back off and wait for this interrupt before attempting to send any more characters.

Chapter 5

Maintenance

If the MUX card did not pass the self-test described in Chapter 2, it is recommended that you return the card to Hewlett-Packard. If further testing is desired, however, test hoods can be installed on the card and the self-test can be rerun (the test hoods test slightly more of the card's circuitry).

The MUX self-test is programmed in ROM and functionally tests portions of the hardware on the card. (If the test hoods are installed, more hardware is tested.)

The self-test includes a ROM test, a RAM test, a CTC test, and an SIO test. There are two ways to invoke self-test: it is automatically invoked during power up when the Auto Reset line is pulled low, or it may be invoked dynamically by a self-test interrupt from the host computer.

CAUTION

The host must *NOT* attempt to interrupt the MUX card until it has received a Self-Test Done interrupt from the card.

The self-test on the MUX card automatically tests for the presence of the loop-back test hoods on each port. For each port that has a test hood connected, a pattern is generated in a section of the self-test that externally loops back through the transceivers. To fully test the transceivers on all four ports in one pass, four test hoods need to be installed. The test hood part numbers are as follows:

Part Number 98642-67950	- This test hood tests ports 1,2, and 3. Note that three of these hoods are necessary to test the transmitters and receivers on ports 1, 2, and 3 in a single pass of the self-test.
Part Number 98644-67950	- This test hood tests the modem channel (port 0).

The wiring for the test hood for ports 1, 2, and 3 is shown in figure 5-1. Figure 5-2 shows the wiring for the modem test hood (port 0).

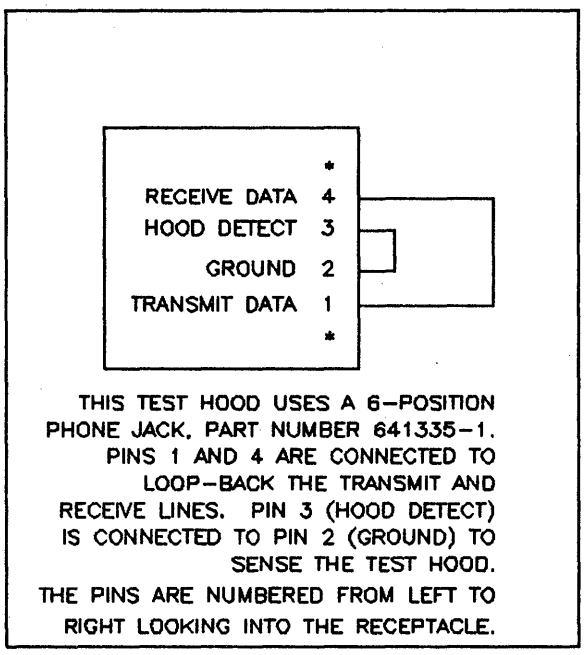


Figure 5-1. Test Hood for Ports 1, 2, and 3

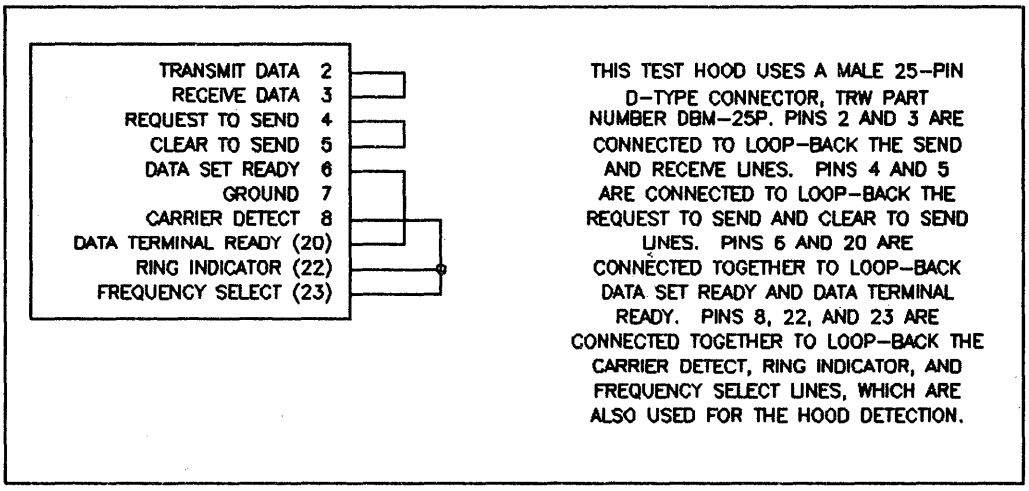


Figure 5-2. Test Hood for Port 0

To test the card using the test hoods, perform the following:

1. Turn computer system power off.
2. Connect test hood part number 98644-67950 to port 0 (modem channel).
3. Connect test hoods part number 98642-67950 to ports 1, 2, and 3.
4. Turn on computer system power. The self-test will execute.

Upon successful completion of self-test, the following will occur:

1. The ST-COND register will contain the value $E0_{hex}$ to indicate that self-test passed.
2. The card will send the host a Self-Test Complete interrupt.
3. The card will execute the initialization routine.

Upon unsuccessful termination of self-test, the following will occur:

1. The ST-COND register receives the value in the IX register. This value indicates where the test failed.
2. The system console will display an error message identifying the card by ID number and select code, and specify a number which indicates the type of failure (the value in the ST_COND register). See the paragraph "*Code Displayed to Console on Self-Test Failure*" for an explanation of the codes.
3. The card sends the host a Self-Test Complete interrupt.
4. The card will execute (or attempt to execute) the initialization routine.

CODE DISPLAYED TO CONSOLE ON SELF-TEST FAILURE

As stated above, when self-test fails, a number representing the section of self-test that failed is written to the ST-COND register. In the event of self-test failure, the host reads the ST-COND register and displays this number on the system console.

The following listing shows individual tests executed in self-test in the order they are executed. The number to the left of each test is the one displayed on the system console if that component of the test fails.

```
ST-COND = 1:  INT-COND/INTERRUPT register test
          2:  NMI/RESET ID register test
          3:  Semaphore register test
          4:  ROM test
          5:  RAM test
          6:  CTC 0 test - algorithm 1
          7:  CTC 0 test - algorithm 2
          8:  CTC 1 test - algorithm 1
          9:  CTC 1 test - algorithm 2
         10:  SIO 0 CH A test (internal loopback)
         11:  SIO 0 CH B test (internal loopback)
         12:  SIO 1 CH A test (internal loopback)
         13:  SIO 1 CH B test (internal loopback)
         14:  SIO 0 CH A test (with test hood - external loopback)
         15:  SIO 0 CH B test (with test hood - external loopback)
         16:  SIO 1 CH A test (with test hood - external loopback)
         17:  SIO 1 CH B test (with test hood - external loopback)
```

NOTE

Self-test executes the component tests in the order shown above and terminates at the first failure encountered. Any components of self-test beyond the one in which the failure occurred are *not* executed.

REPAIR

If desired, isolation to a defective part may be performed. Please be advised, however, that such work is at your discretion and is your responsibility; moreover, NOTE THAT CUSTOMER REPAIR OR MODIFICATION OF THE MUX CARD WILL INVALIDATE WARRANTY AND RENDER THE CARD INELIGIBLE FOR REPAIR BY HEWLETT-PACKARD COMPANY. If such repair service is performed, the replaceable parts information in Chapter 6 and the schematic logic diagrams in Chapter 7 will be of assistance.

Chapter 6
Replaceable Parts

This chapter contains information for ordering replaceable parts for the MUX card. Table 6-1 contains a list of replaceable parts, table 6-2 contains the names and addresses of the manufacturers indexed by the code numbers in table 6-1, and figure 6-1 shows the locations of the parts on the MUX card.

REPLACEABLE PARTS

Table 6-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity.
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to table 6-2 for a cross-reference of the manufacturers.

ORDERING INFORMATION

To order replacement parts or to obtain information on parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will ensure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the kit containing the part (refer to the product identification information supplied in Chapter 1).
2. Description and function of the part.
3. Quantity required.

Table 6-1. HP 98642A Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	98642-66501	1	1	PCA 4CH DIO MUX	28480	98642-66501
C1	0160-3847	9	10	CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C2	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C3	0160-4810	8	7	CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C4	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C5	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C6	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C7	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C8	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C9	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C10	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C11	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C12	0160-4807	3	2	CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
C13	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C14	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C15	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C16	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C17	0160-4807	3		CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
C18	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C19	0180-1746	5	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C20	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
C21	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C22	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
CR1	1901-1098	1	2	DIODE-SWITCHING 1N4150 50V 200MA 4NS	9N171	1N4150
CR2	1901-1098	1		DIODE-SWITCHING 1N4150 50V 200MA 4NS	9N171	1N4150
CR3	1901-0518	8	2	DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR4	1901-0518	8		DIODE-SM SIG SCHOTTKY	28480	1901-0518
J0	1252-0269	9	1	CONN-RECT D-SUBMIN 25-CKT 25-CONT	28480	1252-0269
J1	1251-7532	1	3	MODULAR PHONE RCPT RIGHT ANGLE PC MOUNT	28480	1251-7532
J2	1251-7532	1		MODULAR PHONE RCPT RIGHT ANGLE PC MOUNT	28480	1251-7532
J3	1251-7532	1		MODULAR PHONE RCPT RIGHT ANGLE PC MOUNT	28480	1251-7532
R1	0698-7252	7	5	RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-F
R2	0698-7252	7		RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-F
R3	0698-7252	7		RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-F
R4	0698-0082	7	3	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R5	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R6	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R7	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R8	0757-0405	4	1	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
R9	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R10	0698-7252	7		RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-F
R11	0698-7252	7		RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-F
U1-U10				NOT ASSIGNED		
U11	1820-1427	8	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS156N
U12	1820-1245	8	2	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
U13	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U14	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U15	1820-2488	3	1	IC FF TTL ALS D-TYPE POS-EDGE-TRIG	01295	SN74ALS74N
U16	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U17	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U18	1820-0990	8	2	IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
U19	1820-0509	5	2	IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U20	1820-0509	5		IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U21	1820-0990	8		IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
U22	1820-2300	8	2	IC-Z80A SIO/2	28480	1820-2300
U23	1820-2300	8		IC-Z80A SIO/2	28480	1820-2300
U24-U30				NOT ASSIGNED		
U31	0340-0944	3	1	INSULATOR-IC NYLON BLACK	28480	0340-0944
U31	1813-0225	7	1	CRYSTAL-CLOCK-OSCILLATOR	28480	1813-0225
U32	1820-1245	8		IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
U33	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
U34	1820-1428	9	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
U35	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N

Table 6-1. HP 98642A Replaceable Parts (continued)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U36	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U37	1820-1206	1	1	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U38	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U39	1820-1568	8	1	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
U40	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U41	1820-1470	1	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U42-U54				NOT ASSIGNED		
U55	1818-1611	7	1	IC CMOS 16384 (16K) STAT RAM 150-NS 3-S	S4013	HM6116P-3
U56	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U57	1200-0553	5	1	SOCKET-IC 28-CONT DIP-SLDR	28480	1200-0553
U58				NOT ASSIGNED		
U60				NOT ASSIGNED		
U61	1820-1804	5	1	IC BFR NMOS CLOCK DRVR	04713	MPQ6842
U62	1810-0162	5	1	NETWORK-RES 14-DIP4.7K OHM X 13	11236	760-1-R4.7K
U63	3101-2747	5	1	8-POS AI DIP SW	28480	3101-2747
U64	1820-2740	0	1	IC COMPTR TTL LS MAGTD 2-INP 8-BIT	01295	SN74LS688N
U65	1820-1905	7	1	IC GATE TTL LS NOR DUAL 5-INP	07263	74LS260PC
U66				NOT ASSIGNED		
U67	1820-2298	3	1	IC-Z80A CPU	28480	1820-2298
U68	1820-2301	9	2	IC-Z80A CTC	28480	1820-2301
U69	1820-2301	9		IC-Z80A CTC	28480	1820-2301
U70-U71				NOT ASSIGNED		
U72	1820-2206	3	2	IC MISC TTL LS	01295	SN74LS640N
U73	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U74	1820-2206	3		IC MISC TTL LS	01295	SN74LS640N
U75	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U76	1820-1444	9	4	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U77	1820-1444	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U78	1820-1444	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U79	1820-1444	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
W1	0811-3716	2	4	RESISTOR ZERO OHM	28480	0811-3716
W2	0811-3716	2		RESISTOR ZERO OHM	28480	0811-3716
W3	0811-3716	2		RESISTOR ZERO OHM	28480	0811-3716
W4	0811-3716	2		RESISTOR ZERO OHM	28480	0811-3716
	0515-0076	3	2	SCREW-MACH M3 X 0.5 6MM-LG 90-DEG-FLH-HD	28480	0515-0076
	0590-1445	0	2	THREADED INSERT-NUT M3 X 0.5 CARB-STL	28480	0590-1445
	1818-3384	5	1	IC NMOS 65536 (64K) EPROM 250-NS 3-S	28480	1818-3384
	7121-1010	9	1	LBL-LINE PTR .5-IN-WD X .5-IN-LG	28480	7121-1010
	5180-7226	3	1	PC BOARD	28480	5180-7226
	98642-00001	8	1	COVER PLATE	28480	98642-00001
	98642-81003	6	1	BURNIN DIO MUX	28480	98642-81003

Table 6-2. Code List of Manufacturers

Mfr Code	Manufacturer Name	Address		Zip Code
S4013	HITACHI	TOKYO, JAPAN		
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND COMPNT DIV	DALLAS	TX	75222
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
11236	CTS OF BERNE INC	BERNE	IN	46711
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
9N171	UNITRODE CORP	LEXINGTON	MA	

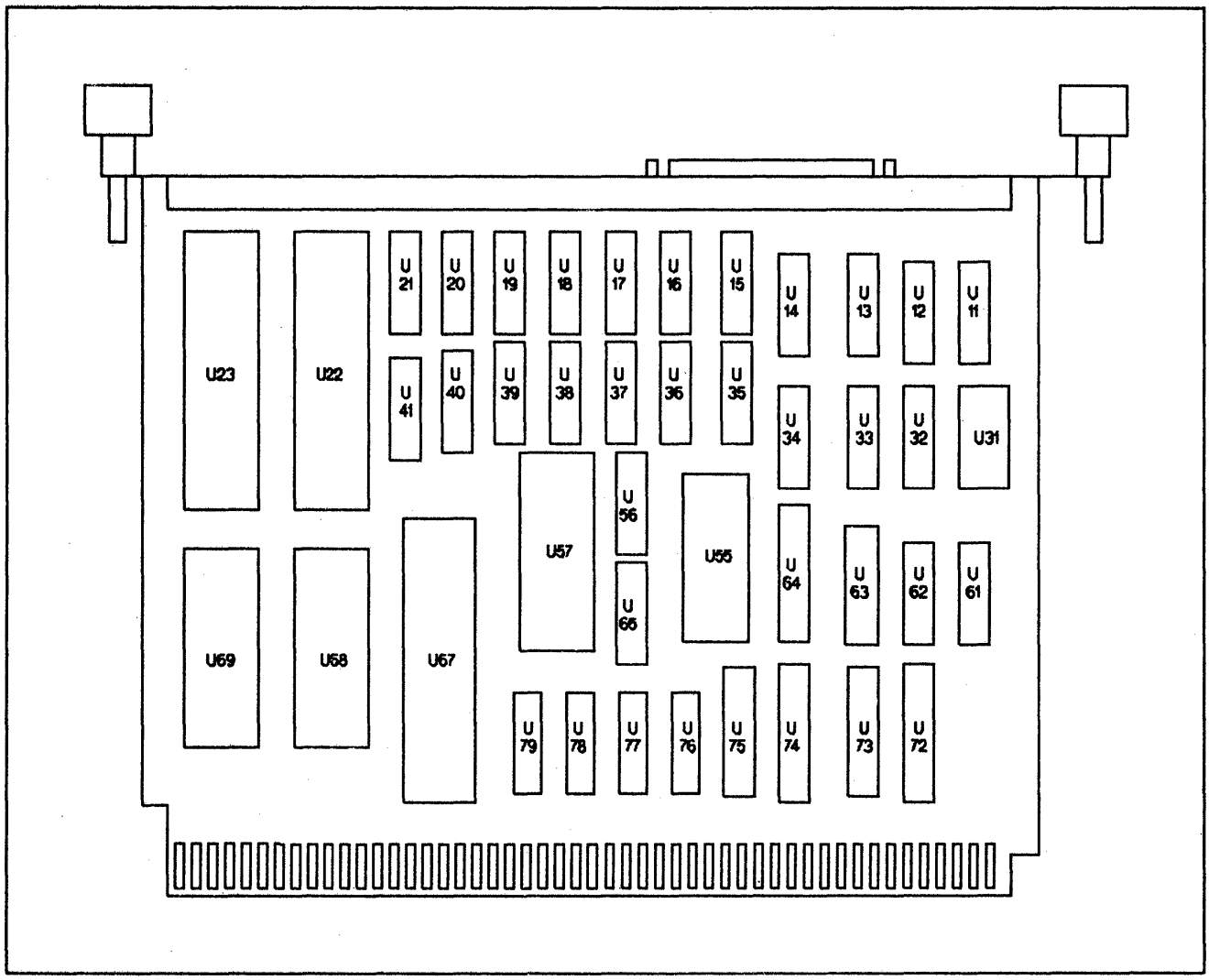


Figure 6-1. HP 98642A Parts Location Diagram

Chapter 7

Schematic Diagrams

This chapter contains schematic logic diagrams for the MUX card.

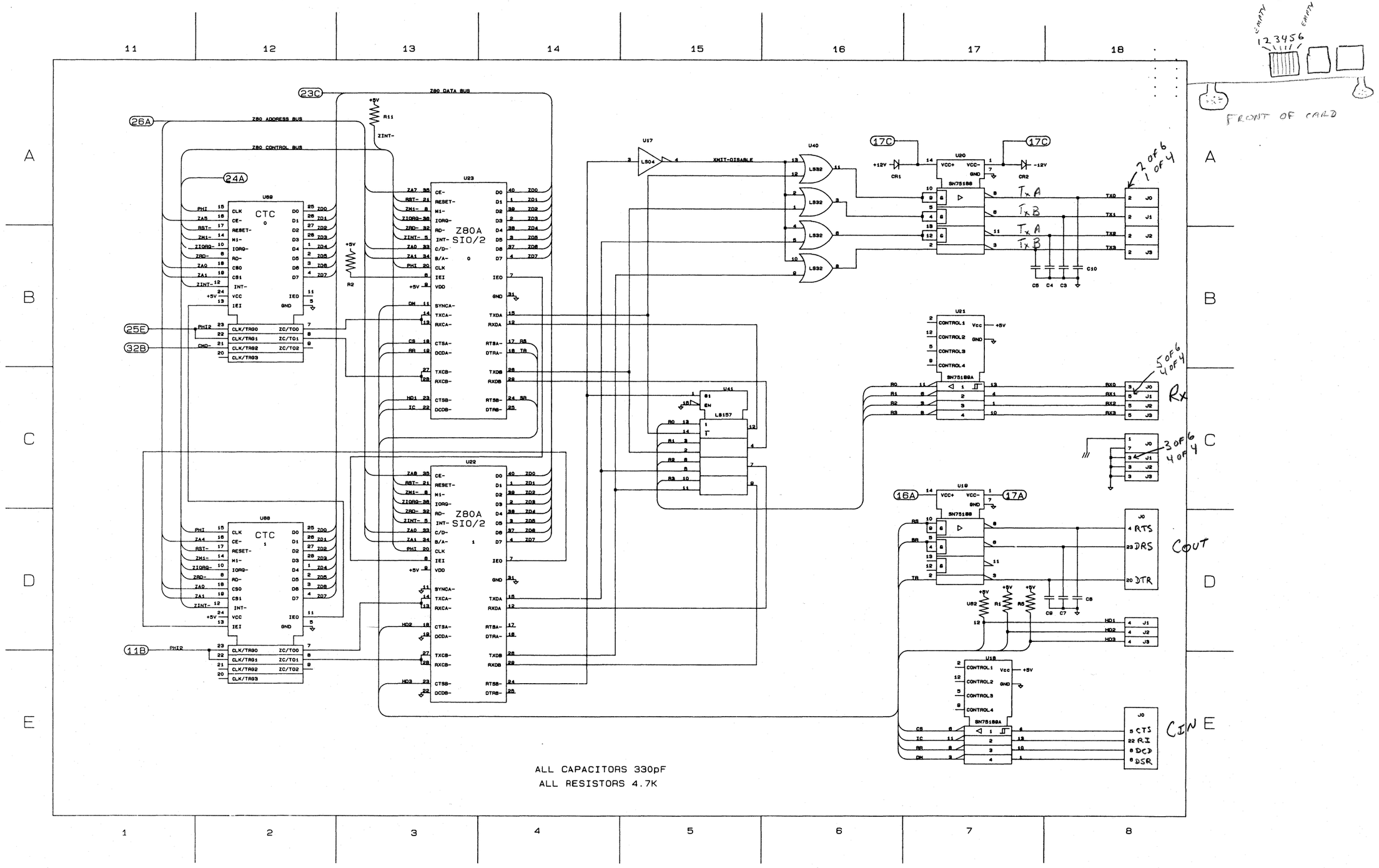


Figure 7-1. MUX Schematic Logic Diagram (Sheet 1 of 3)
Update 2 (April 1988)
7-3/7-4

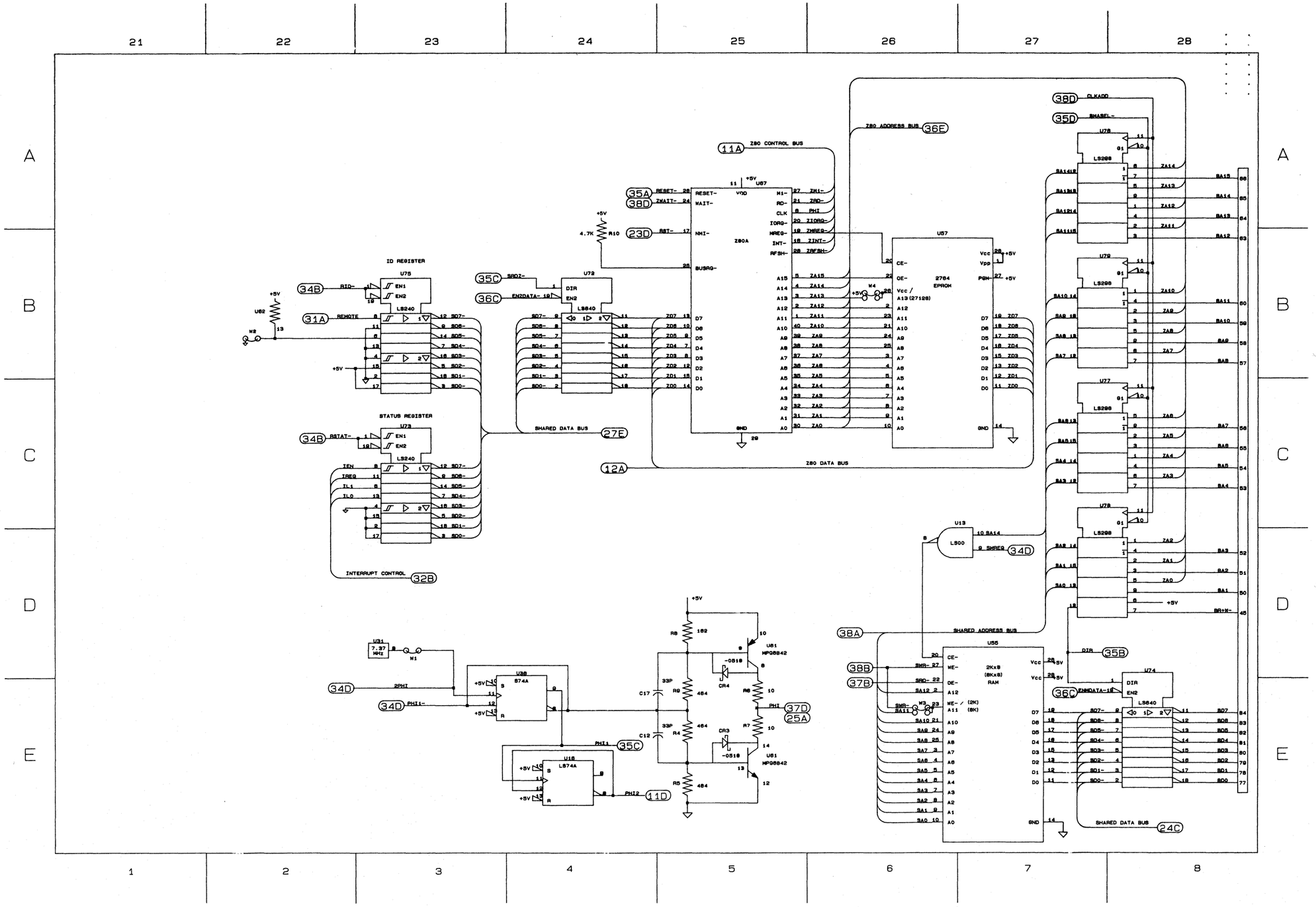


Figure 7-1. MUX Schematic Logic Diagram (Sheet 2 of 3)
Update 2 (April 1988)
7-5/7-6

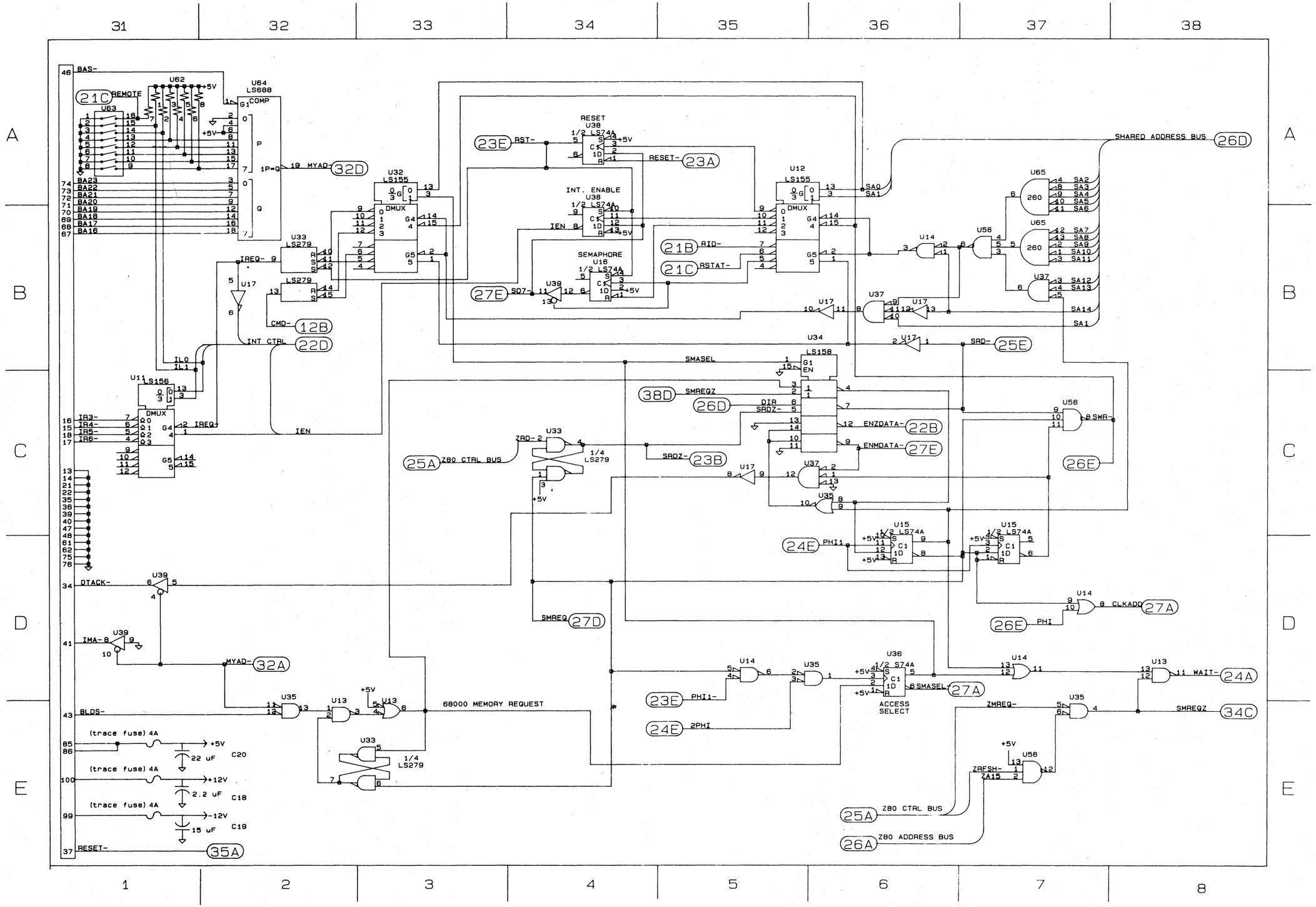


Figure 7-1. MUX Schematic Logic Diagram (Sheet 3 of 3)

Chapter 8
Product History

This chapter lists the changes that have been made to the HP98642A MUX.

Date Code	Remarks
A-2432	Original board.
A-2526	EPROM changed from 98642-81001 to 98642-81002.
A-2530	Pin 1 of U57 jumpered to pin 28 of U57.
B-2535	Previous change incorporated into board layout.
B-2627	EPROM changed from 98642-81002 to 98642-81003.

INDEX

A

B

C

D

E

F

G

H

I

J

M

O

P

R

S

T

Z

MANUAL UPDATE

MANUAL IDENTIFICATION

Title: Four-Channel Asynchronous Multiplexer (MUX)

Part Number: 98642-90001

UPDATE IDENTIFICATION

Update Number: 2 (April 1988)

This update also includes:
Update 1 August 1986

This Update Goes With: First Edition (September 1985)

THE PURPOSE OF THIS MANUAL UPDATE
is to provide new information for your manual to bring it up to date. This is important because it ensures that your manual accurately documents the current version of the product.

THIS UPDATE CONSISTS OF
this cover sheet, a printing history page (if any), any replacement pages, and write-in instructions (if any). Replacement pages are identified by the update number at the bottom of the page. A vertical line (change bar) in the outside margin indicates new or changed text material. The change bar is not used for typographical or editorial changes that do not affect the content of the text.

TO UPDATE YOUR MANUAL
identify the latest update (if any) already contained in your manual by referring to the printing history page. Incorporate only the updates from this packet not already included in your manual. Following the instructions on the back of this page, replace existing pages with the update pages and insert new pages as indicated. If any page is changed in two or more updates, such as the printing history page which is furnished new for each update, only the latest page will be included in the update package. Destroy all replaced pages. If write-in instructions are included they are listed on the back of this page.

HEWLETT-PACKARD COMPANY
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678

98642-90001
U0488
Update 2
April 1988

TECHNICAL MANUAL UPDATE

(98642-90001)

Note that "*" indicates a changed page.

UPDATE	DESCRIPTION
2	A. Replace the following pages with new attached: Title* / ii* 2-5 / 2-6* 7-3* /7-4* 7-5* /7-3*
1	A. Replace the following pages with new attached: vii* / blank 6-3 / 6-4* B. Add new Chapter 8, Product History. C. Replace the following pages with new attached: Index-1 / Index-2* Index-3* / Index-4

READER COMMENT SHEET

Roseville Networks Division

HP 98642A FOUR-CHANNEL ASYNCHRONOUS MULTIPLEXER
Installation Manual

98642-90001 September 1985

We welcome your evaluation of this manual. Your comments and suggestions help us to improve our publications. Please explain your answers under Comments, below, and use additional pages if necessary.

Is this manual technically accurate? ☐ Yes ☐ No

Are the concepts and wording easy to understand? ☐ Yes ☐ No

Is the format of this manual convenient in size, arrangement, and readability? ☐ Yes ☐ No

Comments:

This form requires no postage stamp if mailed in the U.S. For locations outside the U.S., your local HP representative will ensure that your comments are forwarded.

FROM: **Date** _____

Name _____

Company _____

Address _____

_____

_____

FOLD FOLD

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 256 ROSEVILLE, CALIFORNIA

POSTAGE WILL BE PAID BY ADDRESSEE

Publications Manager
Hewlett-Packard Company
Roseville Networks Division
8000 Foothills Boulevard
Roseville, Ca. 95678

FOLD FOLD

MANUAL PART NO. 98642-90001
E0985
Printed in U.S.A.
September 1985

HEWLETT-PACKARD COMPANY
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678