Programmable Serial Interface (PSI)

Hardware Reference Manual

Card Assembly: 5061-4920
Date Code: B-2314

HEWLETT PACKARD

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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with the user-inserted update information. New editions of this manual will contain new information, as well as updates.

First Edition ..... June 1983
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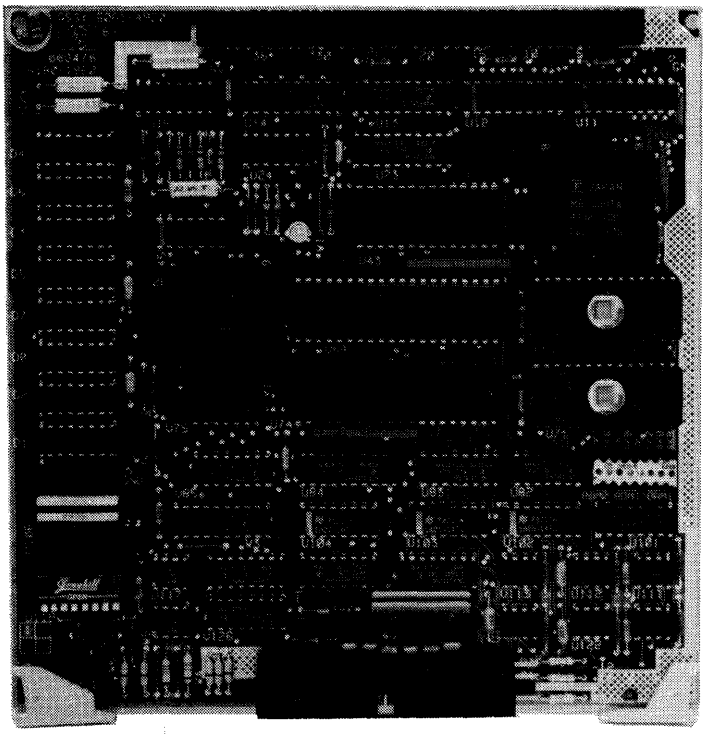


Figure 1-1. PSI Card

GENERAL INFORMATION

SECTION I

This manual provides general information, installation procedures, theory of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the Hewlett-Packard Programmable Serial Interface (PSI) Card. This section contains general information concerning the PSI, and includes a description and specifications.

PHYSICAL DESCRIPTION

The Programmable Serial Interface (PSI) card is shown in figure 1-1. One 80-pin connector connects the card to an Input/Output Adapter and from there to a host computer, and a 50-pin connector connects the card to a peripheral device.

The PSI card can be used in several applications, depending on the firmware ROM/EPROM installed on the card. The ROM firmware is explained in separate manuals, depending on the application. Thus, a product of which the PSI is a part will consist of:

The PSI Printed Circuit Assembly (also referred to as a card in this manual), part number 5061-4920.

One or two ROMs or EPROMS, or one ROM/EPROM and one static RAM.

Up to eight jumper plugs (mounted on the card) depending on the ROM/EPROM/RAM configuration.

A cable, depending on the application.

This manual, part number 27132-90005.

An installation manual for the complete product (the part number will depend on the product).

A firmware manual (the part number will depend on the product).

FUNCTIONAL DESCRIPTION

The PSI provides serial interface capability between a host computer and a remote computer, or a host computer and a peripheral device.

Figure 1-2 shows a Hewlett-Packard computer system using CHANNEL I/O and the PSI. (CHANNEL I/O is a Hewlett-Packard standard defining the physical and electrical characteristics for an I/O system consisting of an I/O channel, an I/O channel adapter, and I/O cards. The PSI is one of the I/O cards.)

Note that the computer system CPU and memory communicate directly along a Memory/Processor Bus (MPB). I/O data to/from peripheral devices reaches the CPU/memory through the I/O channel, the I/O channel adapter, and an I/O card such as the PSI card. The I/O data is received from and transmitted to peripheral devices by the I/O card, which converts device-specific data to a format compatible with the I/O channel, and thus the computer. The I/O channel adapter (see figure 1-2) controls the flow of traffic between the I/O channel and the memory/processor bus.

The PSI uses several of the Z-80 family of microprocessor components to relieve the host computer of much of the overhead.

IDENTIFICATION

The Product

Up to five digits and a letter (27122A, for example) are used to identify Hewlett-Packard products. The five digits identify the product; the letter indicates the revision level of the product. Note that the PSI card is not a product by itself, it is merely one part of an interface product (other parts of the product are the manuals, ROMs or EPROMs, interface cables, etc.). The complete product is described in the firmware manual.

Printed Circuit Card

The printed circuit card is identified by an assembly part number marked on the card. In addition to the part number, the card is further identified by a letter and a four-digit date code (e.g., B-2314). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the PSI card is:

5061-4920
B-2314

If the date code stamped on the card does not agree with the date code on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (a list of Hewlett-Packard Sales and Service Offices is contained at the back of this manual).

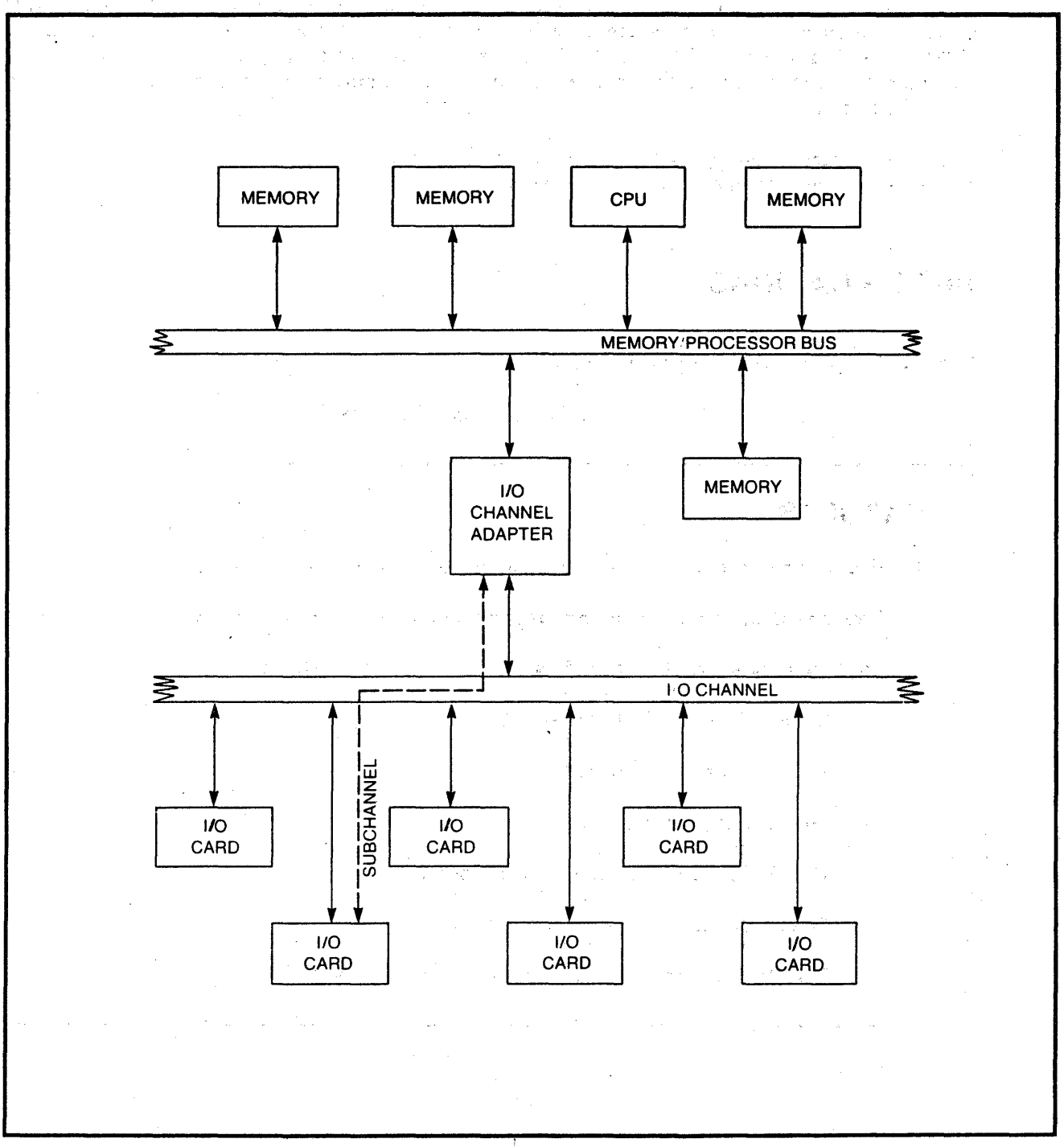


Figure 1-2. PSI in a Typical Hewlett-Packard Computer System

Manuals

This manual, part number 27132-90005, covers the PSI card (part number 5061-4920) only, without any ROMs/EPROMs installed. The PSI card in its complete form with ROMs/EPROMs, cables, etc., is covered in a *firmware* manual which describes the *complete* product. (Note that this manual and the firmware manual are part of the HP 27132 Technical Reference Package.) A third manual, an *installation* manual, is shipped with the complete product and contains information on installing the product in the host computer.

The name, part number, and publication date are printed on the title page of each manual. If the manual is revised, the publication date is changed.

SPECIFICATIONS

Table 1-1 lists the specifications of the PSI.

Table 1-1. Specifications

FEATURES

- One primary full-duplex synchronous/asynchronous serial I/O port
- One secondary full-duplex asynchronous serial I/O port
- Asynchronous baud rates from 50 baud to 115.2K baud

  5, 6, 7, or 8 bits/character

  1, 1.5, or 2 stop bits

  Even, odd, or no parity

  X1, X16, X32, or X64 clock modes

  Break generation and detection

  Parity, overrun, and framing error detection

Table 1-1. Specifications (Continued)

- Synchronous baud rates from 50 baud to 230.4K baud full-duplex internally clocked with secondary channel available

  Baud rates to 460.8K baud full-duplex internally clocked in fast-duplex* mode

  Baud rates to 730K baud full-duplex externally clocked in fast-duplex* mode

    Bisync, HDLC, SDLC operation

    One or two sync characters in two separate sync registers

    Automatic flag or sync character insertion

    Automatic zero insertion and deletion

    Address field recognition

    HDLC information field residue handling

    CRC-16 and CRC-CCITT generation and checking

* -- Fast-duplex is a special mode of operation that uses both channels of the Z-80 SIO for full-duplex data transfer, thus precluding use of the secondary channel. See Section III for more information.

PHYSICAL CHARACTERISTICS

Size:	172.72 mm long by 171.45 mm wide by 16.383 mm thick (6.8 by 6.75 by 0.645 inches)
Weight:	205.4 grams (0.452 pound)
I/O Channel Interconnects:	80-pin connector, J1
Device Interconnects:	50-pin connector, J2

Table 1-1. Specifications (Continued)

POWER REQUIREMENTS

Voltage	Current (typical)	Current (2-sigma)	Power Dissipation (typical)	Power Dissipation (2-sigma)
+5V	1.415A	1.616A	7.077W	8.082W
+12V	0.072A	0.087A	0.864W	1.040W
-12V	0.094A	0.109A	1.128W	1.304W
	TOTAL POWER CONSUMPTION:		9.069W	10.426W (2 sigma value)

INSTALLATION

SECTION II

This section provides information on installing and checking the operation of the PSI.

DETERMINING CURRENT REQUIREMENTS

The PSI circuit card obtains its operating voltages from the host computer power supply through the I/O channel. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the card are listed in the power requirements entry of table 1-1 in Section I. Current requirements for all other I/O cards can be found in the appropriate Technical Reference Manuals.

FIRMWARE INSTALLATION

CAUTION

SOME OF THE COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD OR REMOVING OR REPLACING COMPONENTS.

The EPROMs are installed in the sockets shown in figure 2-1. The types of ROMs/EPROMs that are installed depends on the application and is covered in the firmware manual for that application. You can, however, ensure that the ROM/EPROMs are installed properly, and that they have not been damaged or loosened from their sockets during shipping.

If you ever need to install or remove ROMs/EPROMs, guard against bending or breaking the pins on the component. These pins also can become folded between the component and its socket, which would result in intermittent operation of the PSI. In most cases, a bent or damaged pin can be straightened with careful use of needle-nose pliers.

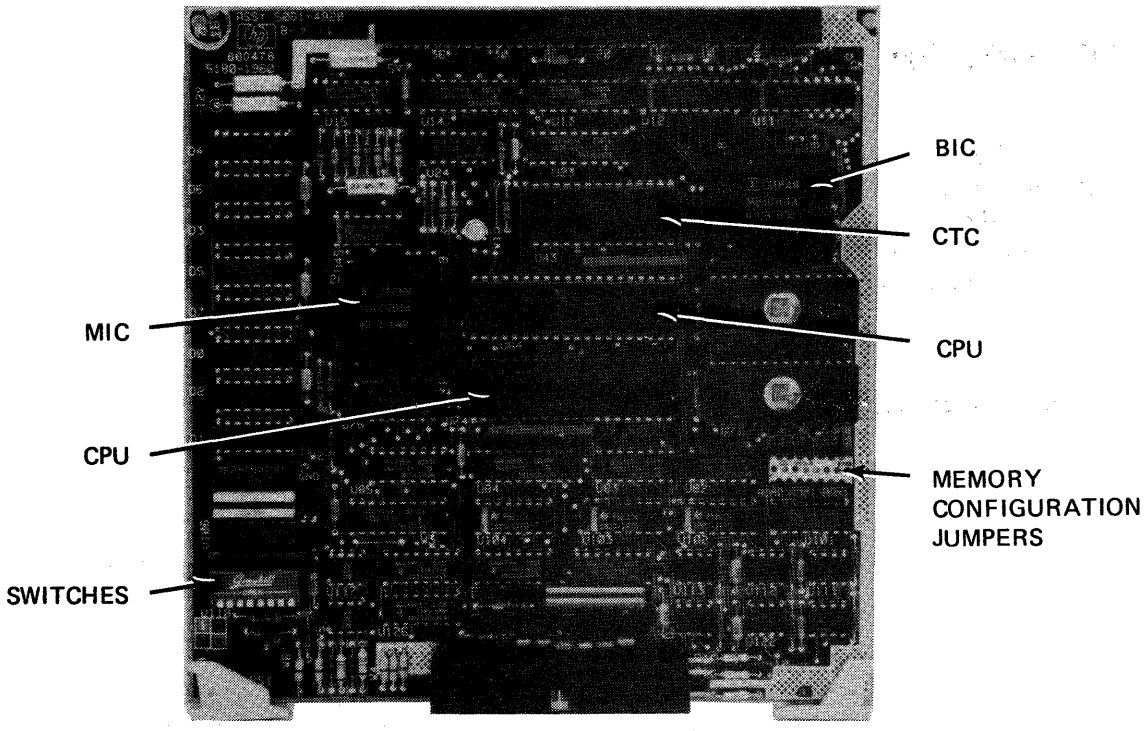


Figure 2-1. Component and Jumper Locations

SWITCHES AND JUMPERS

Switches

A set of eight DIP (Dual In-Line Pack) switches (SW1 through SW8) at location U118 are read into the Z-80B microprocessor during the power-up routine. These switches are used to initially configure the PSI card and are completely dependent on the firmware. Thus, the functions of these switches are defined in the firmware manual and not in this manual.

Memory Configuration Jumpers

The memory configuration jumper, location U81, is a 16-position socket containing eight jumper positions which is used to configure the two memory sockets (U61 and U71) to accomodate different types of ROMs/RAMs.

Memory socket 0 (U61) can use 2K byte, 4K byte, or 8K byte EPROMs such as 2716, 2732, or 2764. Memory socket 1 (U71) can use 2K byte, 4K byte, or 8K byte EPROMs, or can use 1K byte, 2K byte, 4K byte, or 8K byte static RAMs such as 4118, 4802, or 6264. By installing jumpers in the memory select socket (U81), the two memory sockets can be configured for EPROMs/RAMs as shown in table 2-1. Note that table 2-1 is for your information only; the correct EPROMs/RAMs should already be installed.

CAUTION

COMBINATIONS OF JUMPERS OTHER THAN THE ONES SHOWN IN TABLE 2-1 MAY CAUSE DAMAGE TO THE Z-80B. ADDITIONALLY, NO MORE THAN THREE JUMPERS SHOULD BE INSTALLED AT ANY ONE TIME.

Table 2-1. Jumper Positions

EPROM/ RAM PART NUMBER	JUMPER POSITIONS								SELECT SOCKET
	1	2	3	4	5	6	7	8	U81
2716	YES	NO	X	X	X	X	X	X	SOCKET
2732	NO	YES	X	X	X	X	X	X	0
2764	NO	YES	X	X	X	X	X	X	(U61)
2716	X	X	YES	NO	NO	NO	NO	NO	SOCKET
2732	X	X	NO	YES	X	NO	NO	NO	I
2764	X	X	NO	YES	YES	NO	NO	NO	(U71)
4118	X	X	NO	NO	NO	YES	NO	NO	STATIC
4802	X	X	NO	NO	NO	YES	NO	NO	
6264	X	X	NO	NO	NO	NO	YES	YES	RAMS

YES -- Jumper installed
NO -- Jumper not installed
X -- Don't care

ADDITIONAL JUMPERS. Six additional jumpers on the the PSI card are set at the factory and are listed below for information only.

W1 -- Wait Jumper
W2 -- Signature analysis jumper
W3 -- RC jumper
W4 -- Safety jumper
W5 and W6 -- Optical receiver jumpers

I/O CHANNEL INTERFACE

All interface between the PSI and the host computer occurs on the I/O channel. An 80-pin connector (J1) located on the PSI mates with a receptacle on the I/O channel adapter. Connections from the PSI to the I/O channel adapter are shown in table 2-2.

PERIPHERAL DEVICE INTERFACE

A 50-pin connector, J2, on the PSI card provides interface to peripheral devices in accordance with EIA standards RS-232-C, RS-366, and RS-449; and CCITT and ISO standards V.24 and V.25. Pin connections to connector J2, arranged functionally by inputs to the PSI's receivers and outputs from the PSI's transmitters, are shown in tables 2-3 and 2-4.

RS-232-C Cable

Pinouts for an RS-232-C cable are shown in table 2-5. This cable is also compatible with CCITT standard V.28.

RS-449 Cable

Pinouts for an RS-449 cable are shown in table 2-6. For high data rates and long cable lengths, 100-ohm termination resistors (stored on the PSI card near socket U106) should be inserted in sockets R27 and R28. See figure 2-1 for socket locations. Inserting these resistors causes the following signals to be terminated: RD, RT, CS, ST, DM, and RR. In some configurations, it may be desirable to connect signals RT and ST in parallel. This causes the terminating resistors to be paralleled also, resulting in 50-ohm termination. To avoid this and keep the termination impedance at 100 ohms, a 6-pin termination resistor can be used in socket R27. This leaves pins 1 and 2 of the socket unconnected so that only one termination resistor is used.

Direct Connect Cable

Optically isolated receivers are provided on the PSI for read data and receive timing. By using a direct connect cable, computer-to-computer communication can be accomplished up to a distance of 1000 meters. For short cable lengths, or when connected to HP 1000 Series Computers, jumpers W5 and W6 should be removed from the PSI card (socket U81, see figure 2-1). This places a current-limiting resistor in the input circuit to prevent over driving the receivers.

See table 2-7 for the direct connect cable.

NOTE

A "grounding grommet" on the interface cable allows the cable shield to be "grounded" at that point in some applications. Refer to your computer installation manual.

Table 2-2. I/O Channel Connector J1

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
A1	FGND	Frame Ground
A2	DB14	Data Bus, Bit 14
A3	DB12	Data Bus, Bit 12
A4	GND	Ground
A5	DB10	Data Bus, Bit 10
A6	DB8	Data Bus, Bit 8
A7	GND	Ground
A8	DB6	Data Bus, Bit 6
A9	DB4	Data Bus, Bit 4
A10	GND	Ground
A11	DB2	Data Bus, Bit 2
A12	DB0	Data Bus, Bit 0
A13	GND	Ground
A14	AD2	Address Bus, Bit 2
A15	AD0	Address Bus, Bit 0
A16	GND	Ground
A17	DOUT	Data Out
A18	BP0	Bus Primitive Bit 0
A19	CEND	Channel End
A20	SYNC	Synchronize
A21	GND	Ground
A22	CCLK	Common Clock
A23	GND	Ground
A24	BR	Burst Request
A25	DBYT	Device Byte
A26	MYAD	My Address
A27	GND	Ground
A28	---	Not used
A29	---	Not used
A30	---	Not used
A31	RES	Not used
A32	PFW	Power-Fail Warning (Not used)
A33	PPON	Primary Power On
A34	GND	Ground
A35	AC-	Not used
A36	AC+	Not used
A37	-12	-12V
A38	+12	+12V
A39	+5S	Not used
A40	+5P	+5P

Table 2-2. I/O Channel Connector J1 (Continued)

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
B1	FGND	Frame Ground
B2	DB15	Data Bus, Bit 15
B3	DB13	Data Bus, Bit 13
B4	GND	Ground
B5	DB11	Data Bus, Bit 11
B6	DB9	Data Bus, Bit 9
B7	GND	Ground
B8	DB7	Data Bus, Bit 7
B9	DB5	Data Bus, Bit 5
B10	GND	Ground
B11	DB3	Data Bus, Bit 3
B12	DB1	Data Bus, Bit 1
B13	GND	Ground
B14	AD3	Address Bus, Bit 3
B15	AD1	Address Bus, Bit 1
B16	GND	Ground
B17	UAD	Unary Address
B18	BP1	Bus Primitive Bit 1
B19	CBYT	Channel Byte
B20	POLL	Poll
B21	GND	Ground
B22	IOSB	I/O Strobe
B23	GND	Ground
B24	ARQ	Attention Request
B25	DEND	Device End
B26	IFC	Interface Clear
B27	GND	Ground
B28	---	Not used
B29	---	Not used
B30	RES	Not used
B31	ISPU	Not used
B32	NMI	Non-Maskable Interrupt
B33	SPON	Secondary Power On (Not used)
B34	GND	Ground
B35	AC-	Not used
B36	AC+	Not used
B37	-12	-12V
B38	+12	+12V
B39	+5S	Not used
B40	+5P	+5P

Table 2-3. Inputs from the Peripheral to the PSI

J2 PIN	J2 MNEMONIC	RS-449 MNEMONIC	RS-232-C MNEMONIC	V.24 EQUIVALENT	RS-366A/ V.25 ALT	PSI INPUT
A9 B9	RD(A) RD(B)	RD	BB	104		RXDB PRI_RD
A7 B7	ST(A) ST(B)	ST	DB	114		TXCB-
A10 B10	RT(A) RT(B)	RT	DD	115		RXCB-
A8 B8	CS(A) CS(B)	CS	CB	106		CTSB- or CTSA- in Dup Mode
A11 B11 A12	DM(A) DM(B) DM(C)**	DM	 CC	107		DM_DTRB- (DSR) F1-bit 0
A14 B14	RR(A) RR(B)	RR	CF	109		DCDB-
A16 B16 B19	SCS SRR IC	SCS SRR IC	SCB SCF CE	121 122 125	ACR/205 PW1/213	CTSA- DCDA- IC F1-bit 1
A19	TM	TM		142	PND/210	TM- F1-bit 2
A18	SQ	SQ	CG	110	DSC/204	SQ- F1-bit 3

Table 2-3. Inputs from the Peripheral to the PSI (Continued)

J2 PIN	J2 MNEMONIC	RS-449 MNEMONIC	RS-232-C MNEMONIC	V.24 EQUIVALENT	RS-366A/ V.25 ALT	PSI INPUT
B18	SRD	SRD	SBB	119	DLO/203	RXDA SEC_RD F1-bit 4
A23 B23	DCRD(A) DCRD(B)	RD	BB	104		RXDB
A24 B24	DCRT(A) DCRT(B)	RT	DD	115		RXCB-
** DM(C) connects to DM(A) through a 1.96K ohm resistor						

Table 2-4. Outputs from the PSI to a Peripheral Device

J2 PIN	J2 MNEMONIC	RS-449 MNEMONIC	RS-232-C MNEMONIC	V.24 EQUIVALENT	RS-366A/ V.25 ALT	PSI INPUT
A4 B4 A22	SD(A) SD(B) SD	SD	-------- BA	103		TXDB or TXDA (Dup Mode)
A3 B3 A15	TR(A) TR(B) TR	TR	-------- CD	108.2		DTRB-
A5 B5 B15	RS(A) RS(B) RS	RS	-------- CA	105		RTSB- or RTSA- (Dup Mode)
A6 B6 A13	TT(A) TT(B) TT	TT	-------- DA	113		2XDCLK1 ST(SYNC) DCLK1(SYNC)
A17 B17 A21 B20 A20 B2 B21	SRS SSD IS LL RL NS SF/SR	SRS SSD IS LL RL NS SF/SR	SCA SBA CH	120 118 141 140 111	DPR/211 CRQ/202 NB1/206 NB2/207 NB4/208 NB8/209	RTSA- TXDA DTRA- F3-bit 0 F3-bit 1 F2-bit 2 F2-bit 3
A1 A2 B1	+12V +5V -12V					
B13 B12 B22	RC SG SC	RC SG SC	 AB 	102b 102 102a	 AB/201 	REC COMM SIG GND SEND COMM
A25 B25	FRAME GROUND		AA	101	AA	FRAME GROUND

Table 2-5. RS-232-C Cable Connections

J2 PIN	J2 MNEMONIC	RS-232-C PIN	RS-232-C MNEMONIC
*	---	1	AA
A22	SD	2	BA
A9	RD(A)	3	BB
B15	RS	4	CA
A8	CS(A)	5	CB
A12	DM(C)	6	CC
B12**	SG	7	AB
B7**	ST(B)	7	AB
B8**	CS(B)	7	AB
B9**	RD(B)	7	AB
B10**	RT(B)	7	AB
B11**	DM(B)	7	AB
B13**	RC	7	AB
B14**	RR(B)	7	AB
A14	RR(A)	8	CF
B16	SRR(A)	12	SCF
A16	SCS(A)	13	SCB
B17	SSD	14	SBA
A7	ST(A)	15	DB
B18	SRD(A)	16	SBB
A10	RT(A)	17	DD
A17	SRS	19	SCA
A15	TR	20	CD
A18	SQ(A)	21	CG
B19	IC(A)	22	CE
B21	SF/SR	23	CH
A13	TT	24	DA

* The shield is connected to chassis ground through a decoupling capacitor in the connector hood.

** These signals are bussed together at connector J2

Table 2-6. RS-449 Cable

J2 PIN	J2 MNEMONIC	DB-37 PIN	RS-449 MNEMONIC	PAIR NUMBER
B12	SG	19	SG	10
B13	RC	20	RC	16
A3	TR(A)	12	TR(A)	1
B3	TR(B)	30	TR(B)	1
A11	DM(A)	11	DM(A)	9
B11	DM(B)	29	DM(B)	9
A4	SD(A)	4	SD(A)	2
B4	SD(B)	22	SD(B)	2
A9	RD(A)	6	RD(A)	7
B9	RD(B)	24	RD(B)	7
A6	TT(A)	17	TT(A)	4
B6	TT(B)	35	TT(B)	4
A7	ST(A)	5	ST(A)	5
B7	ST(B)	23	ST(B)	5
A10	RT(A)	8	RT(A)	8
B10	RT(B)	26	RT(B)	8
A5	RS(A)	7	RS(A)	3
B5	RS(B)	25	RS(B)	3
A8	CS(A)	9	CS(A)	6
B8	CS(B)	27	CS(B)	6
A14	RR(A)	13	RR(A)	11
B14	RR(B)	31	RR(B)	11
B19	IC	15	IC	13
B20	LL	10	LL	14
A20	RL	14	RL	14
A18	SQ	33	SQ	12
A19	TM	18	TM	13
B22	SC	37	SC	16
A21	IS	28	IS	15
B21	SF/SR	16	SF/SR	15
B2	NS	34	NS	10

Table 2-7. Direct Connect Cable

J2 PIN	J2 MNEMONIC	DIRECT CONNECT PIN	CABLE NUMBER
A4	SD(A)	14	4
B4	SD(B)	16	4
B12	SG	15	4
A6*	TT(A)	1	3
A7*	ST(A)		
B6*	TT(B)	3	3
B7*	ST(B)		
A15*	TR		
A14*	RR(A)		
B14*	RR(B)		
B13*	RC		
B12*	SG		
B22	SC	2	3
A23	DCRD(A)	9	2
B23	DCRD(B)	11	2
A24	DCRT(A)	22	1
B24	DCRT(B)	24	1

* Indicated lines are jumpered together as shown

INSTALLATION

CAUTION

ALWAYS ENSURE THAT THE POWER TO THE COMPUTER IS OFF BEFORE INSERTING OR REMOVING THE PSI CIRCUIT CARD AND CABLE. FAILURE TO DO SO MAY RESULT IN DAMAGE TO THE PSI.

CAUTION

SOME OF THE COMPONENTS USED ON THE PRINTED CIRCUIT CARD ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD.

Install the PSI as follows:

1. Determine if your computer system can supply the power needed for the PSI card. Refer to table 1-1 in Section I for power requirements.

2. Verify that the memory configuration jumpers are configured correctly for the EPROMs/RAMs installed on the card.

3. Install the card in the appropriate slot in the computer. Refer to the computer system installation manual to determine the correct slot. When installing the card, use care not to damage components or traces on the card or on adjacent cards. Press the PSI card firmly into place.

CAUTION

BE SURE TO INSTALL THE DIAGNOSTIC TEST HOOD SO THAT ITS COMPONENT SIDE (THE SIDE WITH THE LED) HAS THE SAME ORIENTATION AS THE COMPONENT SIDE OF THE PSI RJE CARD. DAMAGE TO THE PSI RJE CARD CAN RESULT IF THE TEST HOOD IS INSTALLED INCORRECTLY.

4. Connect the cable supplied with the card from J2 to the peripheral device. If you have the test hood, which exercises more of the card's circuitry during the built-in self-test, and can be ordered (Hewlett-Packard part number 1258-0207), connect it to J2 instead of connecting the cable.

START-UP

To start up and verify correct operation of the PSI, perform the following:

1. Turn on computer system power.

2. A self-test is contained on the card. The host computer system determines if the self-test is run automatically at power-on or must be invoked by the user. Refer to the appropriate manual for your system for a description of self-test initiation.

   a. If the diagnostic test hood is not installed when the self-test executes, the LED located on the card should light briefly and go out. This indicates that the card passed self-test. If the LED does not light at all, the card is defective. If the LED stays on, the card did not pass self-test. For either of these latter two cases, it is recommended that you return the card to Hewlett-Packard; refer to the next paragraph for reshipment information. If you wish to perform maintenance on the card, however, refer to Sections 5, 6, and 7 for maintenance information, replaceable parts lists, and schematic logic diagrams, respectively.

   b. If the diagnostic test hood is installed when the self-test executes, the conditions in step 2.a. should occur, plus the LED located on the diagnostic test hood should light briefly and go out simultaneously with the card's LED. If either LED (the one mounted on the card and the one mounted on the diagnostic test hood) does not light at all, or lights and stays on, the causes are the same as in step 2.a.

3. Refer to your system documentation for information on using the PSI in your system.

RESHIPMENT

If the PSI is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment. Include the part number of the PSI.

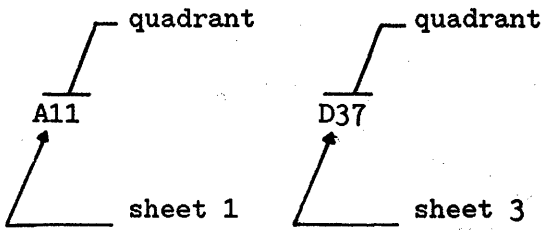
Pack the card in the original factory packing material, if available. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to repack the item. BE SURE TO OBSERVE ANTI-STATIC PRECAUTIONS.

PRINCIPLES OF OPERATION

SECTION III

FUNCTIONAL DESCRIPTION

A functional block diagram of the PSI is shown in figure 3-1. Reference will also be made to the schematic logic diagram contained in Section VI, figure 6-1. Note that figure 7-1 consists of four sheets. References to this figure will be as follows: A11, 6-1; C23, 6-1; D37, 6-1, etc., where the first digit (1, 2, 3, or 4) refers to the sheet number; the combination of letters A through E and numbers 11 through 48 (A11, D37, etc.) refer to the quadrants on the individual sheets; and 6-1 refers to the figure number. For example,



Circuitry on the PSI card consists of a Backplane Interface Circuit (BIC) gate array and its support circuits, a Z-80B microprocessor (CPU), up to 16K bytes of EPROM in two sockets, a Z-80 Counter Timer Circuit (CTC), a Memory Interface Circuit (MIC) gate array, 48K bytes of dynamic RAM, and a Z-80 Serial I/O circuit with associated multiplexer, modem control, and receiver and transmitter circuits.

The heart of the PSI card is the Z-80B CPU (U64, see A22, 6-1), which through a program stored in EPROM controls the functions of the card.

The Backplane Interface Circuit (BIC) (U41, see A14, 6-1) is a custom gate array integrated circuit which controls the communication and handshaking within the I/O channel (backplane). The BIC is accessed by the Z-80B CPU as an I/O device for control information, and through Direct Memory Access (DMA) for data transfer to memory.

The Counter Timer Circuit (CTC, U43, see B24, 6-1) divides the system clock to provide baud rate clocks and other necessary clocks for the PSI. It is accessed by the Z-80B CPU as an I/O device.

The Memory Interface Circuit (MIC, U65, see A32, 6-1) is a custom gate array integrated circuit which handles dynamic refresh and address multiplexing for the 48K dynamic RAM. The MIC also has two channels of DMA control, provides interrupt vectors for backplane interrupts, decodes addresses for EPROM, and provides reset for the rest of the PSI card.

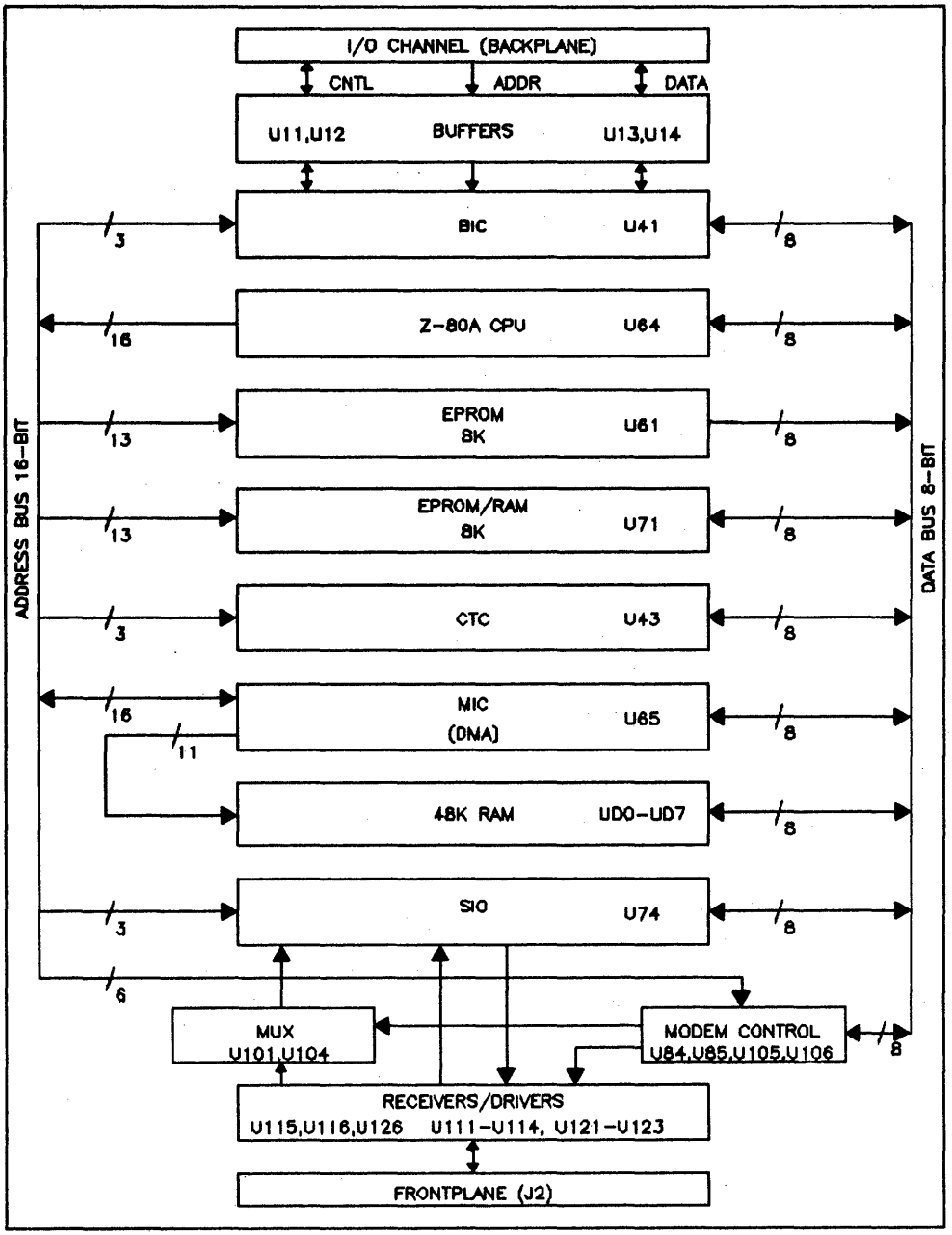


Figure 3-1. PSI Functional Block Diagram

The Serial I/O Circuit (SIO, U74, see A26, 6-1) and its associated multiplexers, modem control, and receivers and drivers, provides serial data communications and control lines to the frontplane connector J2.

System Clocks

Three synchronized system clocks (1.8432 MHz, 3.6864 MHz, and 7.3728 MHz), all derived from the 14.7456 MHz clock signal CCLK+ (see E21, 6-1), perform the following functions:

1.8432 MHz: Provides input to the CLK/TRG pins on the CTC to generate baud rates and system timing intervals.

3.6864 MHz: Used to provide a system clock to the Z-80B CPU, the SIO, MIC, and CTC.

7.3728 MHz: Drives the MIC.

Memory Address Space

The Z-80B CPU address space of 64K bytes is divided into several sections as shown in figure 3-2.

The first 8K bytes of address space is reserved for ROM-based memory. See Section II for details on EPROMs that can be used. The second 8K bytes of address space can also use the same types of ROMs or, alternatively, can use static RAMs.

Eight positions (UD0 through UD7) are provided on the PSI card for 64K by 1 dynamic RAMs. Because the Z-80B can only address 64K bytes of memory, only 48K bytes of dynamic RAM (memory locations 3FFFH through FFFFH) can be accessed by the Z-80 due to overlapping of ROM and dynamic RAM address space. The remaining 16K bytes of dynamic RAM can be accessed by the MIC under DMA control only.

The type of EPROM or static RAM which is used in each of the EPROM sockets on the PSI card must be configured by the 8-position Memory Configuration jumper (U81, see B33, 6-1). See Section II for details.

I/O Address Space

The Z-80B CPU provides addressing capability for 256 distinct I/O port registers. The PSI card uses only 29 I/O port register addresses as shown in table 3-1. Note that the use of any other addresses may cause improper operation.

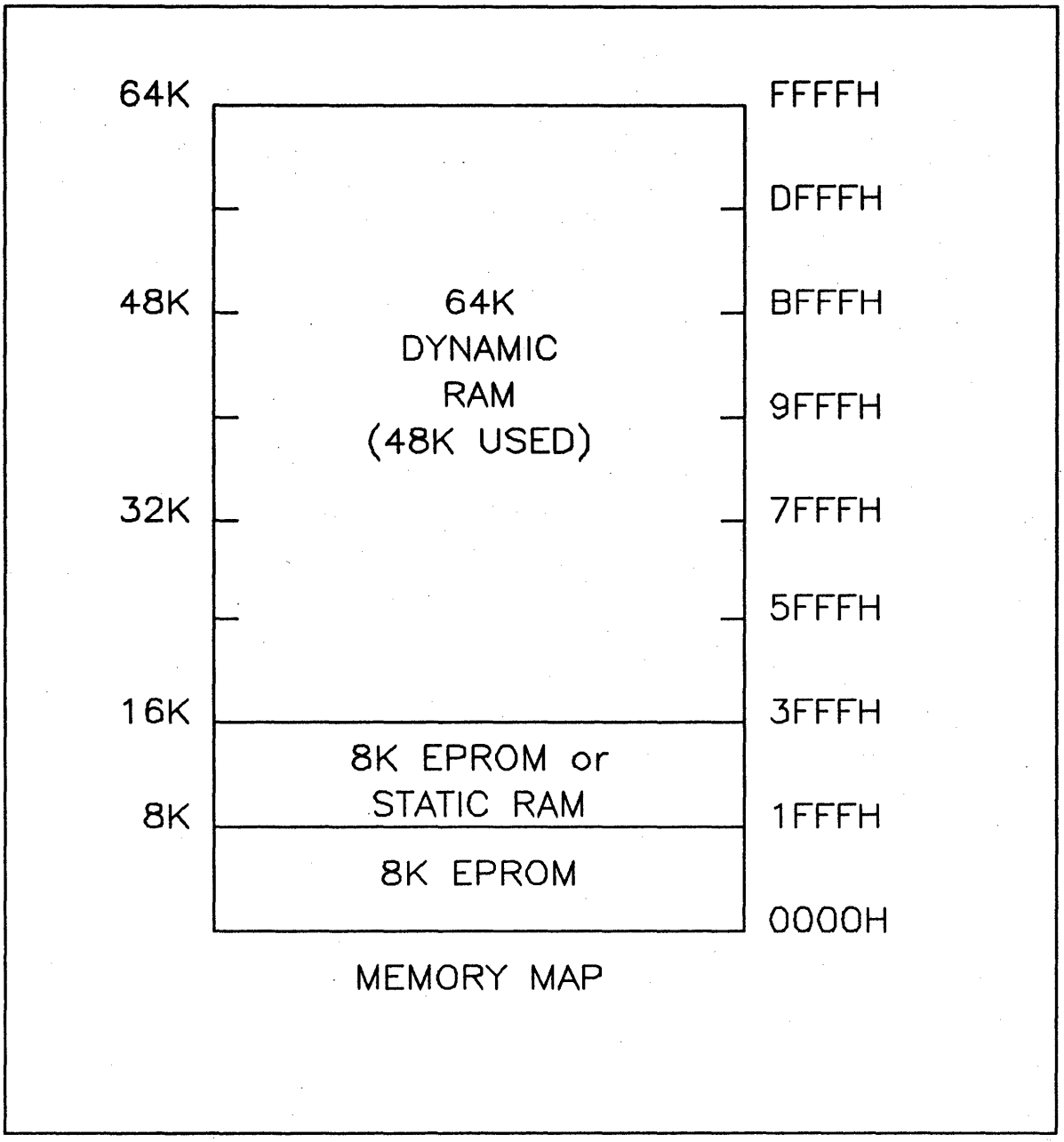


Figure 3-2. Memory Address Space

Table 3-1. I/O Address Space

I/O PORT FUNCTION	I/O ADDRESS LINES 7	6	5	4	3	2	1	0	I/O PORT ADDRESS	READ/WRITE
POWER UP SWITCH	1	1	1	1	X	X	0	0	F0 H	RO
MODEM STATUS INPUT	1	1	1	1	X	X	0	1	F1 H	RO
CONTROL LATCH	1	1	1	1	X	X	1	0	F2 H	WO
MODEM LATCH	1	1	1	1	X	X	1	1	F3 H	WO
MIC REG 0 CONFIG	1	1	1	0	0	0	0	0	E0 H	RW
MIC REG 1 B HI ADDR	1	1	1	0	0	0	0	1	E1 H	WO
MIC REG 2 B LO ADDR	1	1	1	0	0	0	1	0	E2 H	WO
MIC REG 3 B CONFIG	1	1	1	0	0	0	1	1	E3 H	RW
MIC REG 4 B LENGTH	1	1	1	0	0	1	0	0	E4 H	RW
MIC REG 5 B PORT ADDR	1	1	1	0	0	1	0	1	E5 H	RW
MIC REG 6 A HI ADDR	1	1	1	0	0	1	1	0	E6 H	WO
MIC REG 7 A LO ADDR	1	1	1	0	0	1	1	1	E7 H	WO
MIC REG 8 A CONFIG	1	1	1	0	1	0	0	0	E8 H	RW
MIC REG 9 A LENGTH	1	1	1	0	1	0	0	1	E9 H	RW
MIC REG 10 A PORT ADDR	1	1	1	0	1	0	1	0	EA H	RW
MIC REG 11 INT VECTOR	1	1	1	0	1	0	1	1	EB H	RW
CTC CH 0 IRQF	1	1	0	1	X	X	0	0	D0 H	RW
CTC CH 1 2XDCLK1	1	1	0	1	X	X	0	1	D1 H	RW
CTC CH 2 DCLK2	1	1	0	1	X	X	1	0	D2 H	RW
CTC CH 3 GEN PURPOSE	1	1	0	1	X	X	1	1	D3 H	RW
BIC REG 0 DATA	1	0	1	1	X	0	0	0	B0 H	RW
BIC REG 1 COMMAND	1	0	1	1	X	0	0	1	B1 H	RO
BIC REG 1 SUBCH ADDR	1	0	1	1	X	0	0	1	B1 H	WO
BIC REG 2 ORDER	1	0	1	1	X	0	1	0	B2 H	RO
BIC REG 2 STATUS	1	0	1	1	X	0	1	0	B2 H	WO
BIC REG 3 BIC STATUS	1	0	1	1	X	0	1	1	B3 H	RO
BIC REG 3 BIC CONTROL	1	0	1	1	X	0	1	1	B3 H	WO
BIC REG 4 CONFIG	1	0	1	1	X	1	0	0	B4 H	RW
BIC REG 5 INTR LATCH	1	0	1	1	X	1	0	1	B5 H	RW
BIC REG 6 INTR MASK	1	0	1	1	X	1	1	0	B6 H	RW
SIO SEC CH A DATA	0	1	1	1	X	X	0	0	70 H	RW
SIO SEC CH A CONTROL	0	1	1	1	X	X	0	1	71 H	RW
SIO PRI CH B DATA	0	1	1	1	X	X	1	0	72 H	RW
SIO PRI CH B CONTROL	0	1	1	1	X	X	1	1	73 H	RW

Serial I/O Controller (SIO/2)

The Z-80 SIO/2 (U74, A26, 6-1) is a programmable serial I/O controller with two independent full-duplex channels. Each channel has separate control and status lines for modems, and each channel can be independently programmed for synchronous or asynchronous operation. On the PSI card, channel B is the primary channel and can be operated synchronously or asynchronously, while channel A is the secondary channel and can be operated only in asynchronous mode.

SIO REGISTERS. Each SIO channel has an I/O addressable port for data transfer and for control information. For control information there are three read registers and eight write registers available. The functions performed by the registers are shown in table 3-2.

SIO MODEM CONTROL AND STATUS BITS. The modem control and status bits of the SIO are used as defined in table 3-3. In addition, the WAIT/READY lines (W/RDYA- and W/RDYB-) lines should be set to READY for use with the DMA channels of the MIC.

The way that the SIO channels are configured is dependent on the modem control latch U105 (see D27, 6-1), bits 0 through 4. Details are provided in the following paragraphs.

PSI CARD MODES OF OPERATION

The PSI card is capable of ten operational modes of operation and twelve self-test modes. The modes are listed later in tables 3-4 through 3-7.

The following paragraphs describe the signals and conventions used in those tables.

The modes of operation are numbered by using the binary value that is written to the Modem Control register (U85, E27, 6-1) by data bits D0 through D3 (DIR_CON, DUPLEX, SYNC, and INT_TIME). Bit D4 (SELFTEST) is set to 1 (false) for operational modes and 0 (true) for testing modes.

CONTROL LINES. The control lines are defined for use as follows;

INT_TIME: 1 = use internal clocking source (DCLK1) for channel B transmit data.

0 = use external clocking source (ST) for channel B transmit data.

1 or 0 = use external clocking source (RT or DCRT) for channel B receive data, or internal clocking (DCLK1) when in SELFTEST mode.

This control line has affect only when SYNC is true.

SYNC: 1 = synchronous mode. Clocking determined by INT_TIME.

0 = asynchronous mode. Internal clocking source (2XDCLK1) used for transmit and receive data.

Some examples of control line configurations are shown in figures 3-3 through 3-6.

Table 3-2. SIO Register Functions

WRITE REGISTERS	FUNCTION
WR0	Contains register pointers, CRC initialization information, initialization commands for operating modes
WR1	Transmit/receive interrupt and data transfer mode definition
WR2	Interrupt vector (channel B only)
WR3	Receive parameters and controls
WR4	Transmit/receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR6	Synchronization character or SDLC address field
WR7	Synchronization character or SDLC flag
READ REGISTERS	FUNCTION
RR0	Transmit/receive buffer status, interrupt status, and external status
RR1	Special receive condition status
RR2	Modified interrupt vector (channel B only)

Table 3-3. SIO Modem Control and Status Bits

OUTPUTS				
SIO	CONNECTOR J2	NAME	REGISTER AND BIT NO.	I/O ADDR
CONTROL				
RTSA-	SRS	SECONDARY REQUEST TO SEND	WR REG 5 BIT 1	71 H
DTRA-	IS	IN SERVICE	WR REG 5 BIT 7	71 H
RTSB-	RS	REQUEST TO SEND	WR REG 5 BIT 1	73 H
DTRB-	TR	TERMINAL READY	WR REG 5 BIT 7	73 H
		INPUTS		
STATUS				
CTSA-	SCS	SECONDARY CLEAR TO SEND	RD REG 0 BIT 5	71 H
DCDA-	SRR	SECONDARY RECEIVER READY	RD REG 0 BIT 3	71 H
CTSB-	CS	CLEAR TO SEND	RD REG 0 BIT 5	73 H
DCDB-	RR	RECEIVER READY	RD REG BIT 3	73 H

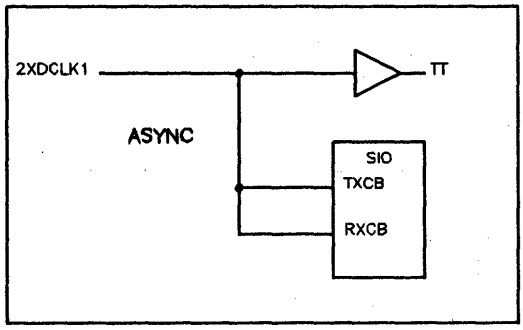


Figure 3-3. ASYNC Control Configuration

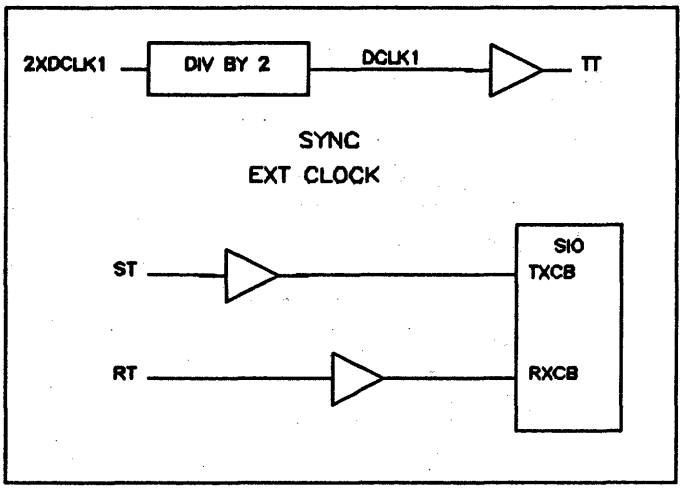


Figure 3-4. SYNC EXT CLOCK Configuration

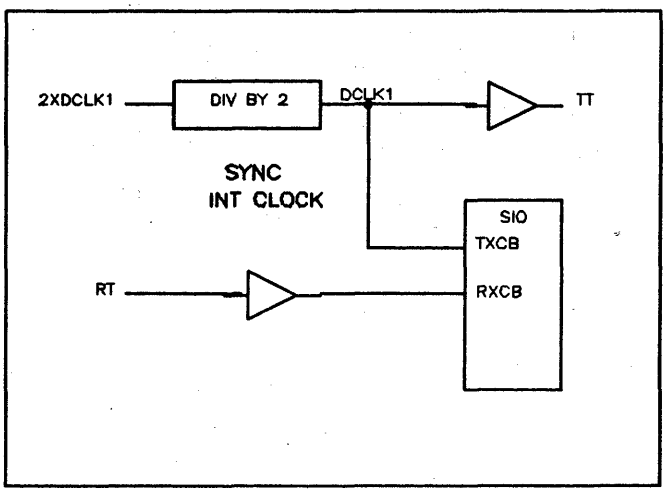


Figure 3-5. SYNC INT CLOCK Configuration

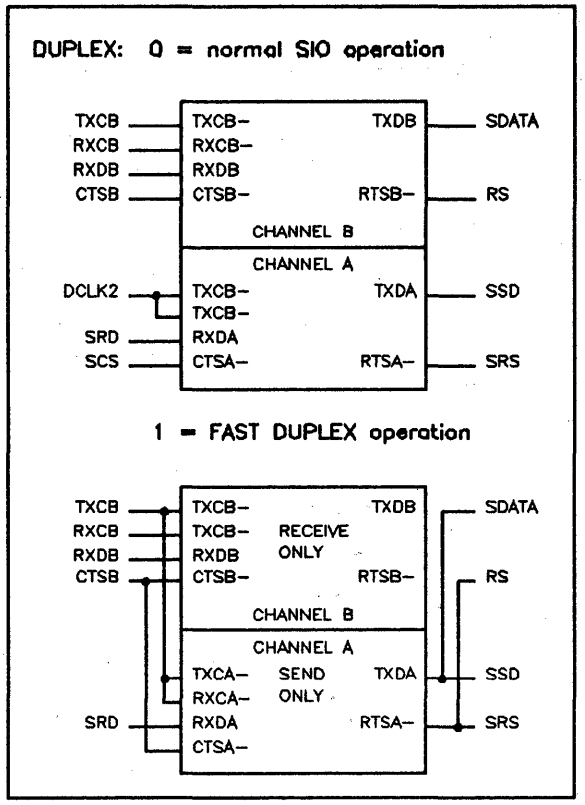


Figure 3-6. DUPLEX Configuration

The following discussion applies to figure 3-6.

DUPLEX: 0 = normal SIO operation 1 = FAST DUPLEX mode

In normal operation, channel B is the Primary send and receive channel, while channel a is the Secondary send and receive channel. In FAST DUPLEX mode, channel B becomes the Primary receive channel, and channel A becomes the Primary transmit channel; the secondary channel is not available. This mode allows both available DMA channels to be used for data transfer in both directions simultaneously in order to attain higher data transfer rates.

DIR_CON: 0 = MODEM operation. In this mode, the normal drivers and receivers are available for use.

1 = Direct Connect operation. This mode is intended for use in direct computer-to-computer connections where optical isolation is desired to prevent ground currents due to ground potential differences between the computers.

In direct connect mode, optically isolated receivers are used for both receive data (DCRD) and receive timing (DCRT). A special cable which only has Send Data (SD), Terminal Timing (TT), Receive Data (DCRD), and Receive Timing (DCRT), is used for this mode. This cable also loops back TT to ST, and TR to RR. The Direct Connect multiplexer (U104, A44, 6-1) loops back DTRB to DM and RS to CTS. These connections allow the same firmware to operate in modem mode or direct connect mode.

SELFTEST: 1 = Normal operation.

0 = Self-Test mode. In this configuration, channel A data is looped back to channel A, and channel B data is looped back to channel B. In addition, DCLK1 is sent to TT and to RXCLK. This allows internal loopback in all asynchronous modes with internal timing. A diagnostic loopback hood allows testing in synchronous modes with external timing.

OPERATIONAL MODE DEFINITIONS. Definitions of the operational modes are as follows:

MODE 0, 1:	Modem Asynchronous. Channel B clocked by 2XDCLK1 and Channel A clocked by DCLK2.
MODE 2:	Modem Synchronous External Clock. Channel B clocked by ST and RT. Channel A clocked by DCLK2.
MODE 3:	Modem Synchronous Internal Clock. Channel B clocked by DCLK1 and RT. Channel A clocked by DCLK2.
MODE 4, 5:	Modem Fast Duplex Asynchronous. Channel B receive channel and Channel A transmit channel. Both clocked by 2XDCLK1.
MODE 6:	Modem Fast Duplex Synchronous External Clock. Channel B receive channel and Channel A transmit channel. Channel B clocked by RT and Channel A clocked by ST.

MODE 7:	Modem Fast Duplex Synchronous Internal Clock. Channel B receive channel and Channel A transmit channel. Channel B clocked by RT and Channel A clocked by DCLK1.
MODE 8, 9:	Direct Connect Asynchronous. Channel B receives DCRD and clocked by 2XDCLK1. Channel A clocked by DCLK2.
MODE 10:	Direct Connect Synchronous External Clock. Channel B receives DCRD and clocked by ST and DCRT. ST has no source so this mode is not usable. Use Mode 11.
MODE 11:	Direct Connect Synchronous Internal Clock. Channel B receives DCRD and clocked by DCLK1 and DCRT. Channel A clocked by DCLK2.
MODE 12, 13:	Direct Connect Fast Duplex Asynchronous. Channel B receives DCRD only and Channel A transmits only. Both clocked by 2XDCLK1.
MODE 14:	Direct Connect Fast Duplex Synchronous External Timing. Channel B receive channel and Channel A transmit channel. Channel B clocked by DCRT and Channel A clocked by ST. ST has no source so this mode is not usable. Use mode 15.
MODE 15:	Direct Connect Fast Duplex Synchronous Internal Timing. Channel B receive channel (DCRD) and Channel A transmit channel. Channel B clocked by DCRT and Channel A clocked by DCLK1.

SELF-TEST MODE DEFINITIONS. Definitions of self-test modes are as follows. In all cases, SDATA is tied to a MARK condition.

MODE ST0, 1:	Modem Asynchronous. Channel B clocked by 2XDCLK1 and Channel A clocked by DCLK2.
MODE ST2:	Modem Synchronous External Clock. Channel B clocked by ST and RT. Channel A clocked by DCLK2. Must use loopback hood.
MODE ST3:	Modem Synchronous Internal Clock. Channel B clocked by DCLK1. Channel A clocked by DCLK2.
MODE ST4, 5:	Modem Fast Duplex Asynchronous. Channel B receive channel and Channel a transmit channel. Both clocked by 2XDCLK1.
MODE ST6:	Modem Fast Duplex Synchronous External Clock. Channel B receive channel and Channel A transmit channel. Channel B clocked by RT and Channel A clocked by ST. Must use loopback hood.
MODE ST7:	Modem Fast Duplex Synchronous Internal Clock. Channel B receive channel and Channel A transmit channel. Channel B clocked by DCLK1 and Channel A clocked by DCLK1.

MODE ST8, 9:	Direct Connect Asynchronous. Channel B clocked by 2XDCLK1. Channel A clocked by DCLK2.
MODE ST10:	Direct Connect Synchronous External Clock. Channel B clocked by ST and DCRT. ST has no source so loopback hood must be used.
MODE ST11:	Direct Connect Synchronous Internal Clock. Channel B clocked by DCLK1. Channel A clocked by DCLK2.
MODE ST12, 13:	Direct Connect Fast Duplex Asynchronous. Channel B and Channel A clocked by 2XDCLK1.
MODE ST14:	Direct Connect Fast Duplex Synchronous External Timing. Channel B receive channel and Channel A transmit channel. Channel B and Channel A clocked by DCLK1 when used with loopback hood.
MODE ST15:	Direct Connect Fast Duplex Synchronous Internal Timing. Channel B receive channel and Channel A transmit channel. Channel B clocked by DCLK1 and Channel A clocked by DCLK1.

MODEM CONTROL. PSI card modes of operation (described in the preceding paragraphs) are controlled by the modem control lines (see D and E28, 6-1). The possible modes and the states of the control lines are shown in tables 3-4 through 3-7.

The control latch (U105, D27, 6-1) provides five control lines to the modem control multiplexers and enables the differential line drivers. The modem latch (U85, E27, 6-) provides four modem control output lines. The modem status register (U84, D22, 6-1) monitors six input lines and the BIC ready line. The modem status register is I/O mapped to port F1 and the modem and control latches are mapped to ports F3 and F2, respectively. See tables 3-8 through 3-10.

Table 3-4. Modem Control Multiplexer -- Modem Mode

MODE	CNTRL	MULTIPLEXER OUTPUTS										
		SDATA	TXCB-	RXDB-	RXCB-	RS-	CTSB-	DM-	RXDA	RXTXCA-	CTSA-	
MODEM ASYNC	1000X MODE 0, 1	TXDB	2X DCLK1	RD	2X DCLK1	RTSB-	CS-	DM-	SRD	DCLK2	SCS-	MUX INPUTS
MODEM SYNC EXT	10010 MODE 2	TXDB	ST	RD	RT	RTSB-	CS-	DM-	SRD	DCLK2	SCS-	
MODEM SYNC INT	10011 MODE 3	TXDB	DCLK1	RD	RT	RTSB-	CS-	DM-	SRD	DCLK2	SCS-	
MODEM DUPLEX ASYNC	1010X MODE 4, 5	TXDA	2X DCLK1	RD	2X DCLK1	RTSA-	CS-	DM-	SRD	2X DCLK1	CS-	
MODEM DUPLEX SYNC EXT	10110 MODE 6	TXDA	ST	RD	RT	RTSA-	CS-	DM-	SRD	ST	CS-	
MODEM DUPLEX SYNC INT	10111 MODE 7	TXDA	DCLK1	RD	RT	RTSA-	CS-	DM-	SRD	DCLK1	CS-	

PRIMARY CHANNEL — SECONDARY CHANNEL

CONTROL LINES = (SELFTEST, DIR_CON, DUPLEX, SYNC, INT_TIME)

NOTE: TT = TXCB

Table 3-5. Modem Control Multiplexer -- Direct Connect Mode

MODE	CNTRL	MULTIPLEXER OUTPUTS								
		SDATA	TXCB-	RXDB	RXCB-	RS- CTSB- DM-	RXDA	RXTXCA-	CTSA-	
DIRECT CONNECT ASYNC	1100X MODE 8, 9	TXDB	2X DCLK1	DCRD	2X DCLK1	RTSB- RTSB- DTRB-	SRD	DCLK2	SCS-	MUX INPUTS
DIRECT CONNECT SYNC EXT	11010 MODE 10	TXDB	ST	DCRD	DCRT	RTSB- RTSB- DTRB-	SRD	DCLK2	SCS-	
		<<<<<DO NOT USE THIS MODE>>>>>								
DIRECT CONNECT SYNC INT	11011 MODE 11	TXDB	DCLK1	DCRD	DCRT	RTSB- RTSB- DTRB-	SRD	DCLK2	SCS-	
DIRECT CONNECT DUPLEX ASYNC	1110X MODE 12,13	TXDA	2X DCLK1	DCRD	2X DCLK1	RTSA- RTSA- DTRB-	SRD	2X DCLK1	RTSA-	
DIRECT CONNECT DUPLEX SYNC EXT	11110 MODE 14	TXDA	ST	DCRD	DCRT	RTSA- RTSA- DTRB-	SRD	ST	RTSA-	
		<<<<<DO NOT USE THIS MODE>>>>>								
DIRECT DUPLEX SYNC INT	11111 MODE 15	TXDA	DCLK1	DCRD	DCRT	RTSA- RTSA- DTRB-	SRD	DCLK1	RTSA-	
		PRIMARY CHANNEL					SECONDARY CHANNEL			

CONTROL LINES = (SELFTEST, DIR_CON, DUPLEX, SYNC, INT_TIME)

NOTE: TT = TXCB

Table 3-6. Modem Control MUX: Modem Self-Test Mode

SELF-TEST MODE	CNTRL	MUX OUTPUTS										
		SDATA	TXCB-	RXDB	RXCB-	RS-	CTSB-	DM-	RXDA	RXTXCA-	CTSA-	
MODEM ASYNC	0000X MODE ST0,1	MARK	2X DCLK1	TXDB	2X DCLK1	RTSB-	CS-	DM-	TXDA	DCLK2	SCS-	
MODEM SYNC EXT	00010 MODE ST 2	MARK	ST <DCLK1>	TXDB	RT <DCLK1>	RTSB-	CS-	DM-	TXDA	DCLK2	SCS-	
		<<<USE ONLY WITH DIAGNOSTIC TEST HOOD>>>										
MODEM SYNC INT	00011 MODE ST 3	MARK	DCLK1	TXDB	DCLK1	RTSB-	CS-	DM-	TXDA	DCLK2	SCS-	MUX INPUTS
MODEM DUPLEX ASYNC	0010X MODE ST4,5	MARK	2X DCLK1	TXDA	2X DCLK1	RTSA-	CS-	DM-	TXDA	2X DCLK1	CS-	
MODEM DUPLEX SYNC EXT	00110 MODE ST 6	MARK	ST <DCLK1>	TXDA	RT <DCLK1>	RTSA-	CS-	DM-	TXDA	ST <DCLK1>	CS-	
		<<<USE ONLY WITH DIAGNOSTIC TEST HOOD>>>										
MODEM DUPLEX SYNC INT	00111 MODE ST 7	MARK	DCLK1	TXDA	DCLK1	RTSA-	CS-	DM-	TXDA	DCLK1	CS-	
			PRIMARY CHANNEL						SECONDARY CHANNEL			

CONTROL LINES = (SELF-TEST, DIR_CON, DUPLEX, SYNC, INT_TIME)

NOTE: TT = DCLK1

Table 3-7. Modem Control MUX: Direct Connect Self-Test Mode

SELF-TEST MODE	CNTRL	MUX OUTPUTS										
		SDATA	TXCB-	RXDB	RXCB-	RS-	CTSB-	DM-	RXDA	RSTXCA-	CTSA	
DIRECT CONNECT ASYNC	0100X MODE ST8,9	MARK	2X DCLK1	TXDB	2X DCLK1	RTSB-	RTSB-	DTRB-	TXDA	DCLK2	SCS-	MUX INPUTS
DIRECT CONNECT SYNC EXT	01010 MODE ST 10	MARK	ST <DCLK1>	TXDB	DCRT <DCLK1>	RTSB-	RTSB-	DTRB-	TXDA	DCLK2	SCS-	
		<<<USE ONLY WITH DIAGNOSTIC TEST HOOD>>>										
DIRECT CONNECT SYNC INT	01011 MODE ST 11	MARK	DCLK1	TXDB	DCLK1	RTSB-	RTSB-	DTRB-	TXDA	DCLK2	SCS-	
DIRECT CONNECT ASYNC	0110X MODE ST 12, ST 13	MARK	2X DCLK1	TXDA	2X DCLK1	RTSA-	RTSA-	DTRB-	TXDA	2X DCLK1	RTSA-	
DIRECT CONNECT DUPLEX SYNC EXT	01110 MODE ST 14	MARK	ST <DCLK1>	TXDA	DCRT <DCLK1>	RTSA-	RTSA-	DTRB-	TXDA	ST <DCLK1>	RTSA-	
		<<<USE ONLY WITH DIAGNOSTIC TEST HOOD>>>										
DIRECT CONNECT DUPLEX SYNC INT	01111 MODE ST 15	MARK	DCLK1	TXDA	DCLK1	RTSA-	RTSA-	DTRB-	TXDA	DCLK1	RTSA-	

PRIMARY CHANNEL — SECONDARY CHANNEL

CONTROL LINES = (SELF-TEST, DIR_CON, DUPLEX, SYNC, INT_TIME)

NOTE: TT = DCLK1

Table 3-8. Modem Status, Port F1 (Input Only)

BIT	MNEMONIC	TRUE	RS-449	RS-232-C	CCITT	RS-366
0	DM_DTRB	1 1	DATA MODE TERMINAL RDY	CC DATA SET READY (DSR) CD DATA TERMINAL RDY	107 108.2	* **
1	IC	1	INCOMING CALL	CE RING INDICATOR	125	
2	TM	1	TEST MODE	CI SIGNAL RATE IND	142/ 112	PND
3	SQ	1	SIG QUALITY	CG SIGNAL QUALITY	110	COS
4	SEC_RD	0	SEC REC DATA	SBB SEC REC DATA	119	DLO(1)
5	RDY	1	READY LINE FROM BIC			
6	PRI_RD	0	RD OR DCRD (USED FOR X.21)			
7	N/C		NO CONNECTION			

* -- Modem mode
** -- Direct connect mode

Table 3-9. Control Latch, Port F2 (Output Only)

BIT	MNEMONIC	TRUE	FUNCTION	RS-366
0	INT_TIME	1	USE INTERNAL CLOCK IN SYNC MODE/NOT EXT CLOCK	---
1	SYNC	1	SYNCHRONOUS MODE/NOT ASYNCHRONOUS MODE	---
2	DUPLEX	1	FAST DUPLEX MODE/NOT NORMAL MODE	---
3	DIR_CON	1	DIRECT CONNECT MODE (OPTO-ISOLATED RECEIVERS)/NOT NORMAL MODE	---
4	SELFTEST	0	CONNECTS TXDA TO RXDA AND TXDB TO RXDB	---
5	LED	0	TURNS ON LED INDICATOR	---
6	XMITEN	1	ENABLE DIFFERENTIAL TRANSMITTERS (SD, TR, ST, TT)	---
7	N/C		NO CONNECTION	

NOTE: All of the above lines are set to 0 at power-up

Table 3-10. Modem Latch, Port F3 (Output Only)

BIT	MNEMONIC	TRUE	FUNCTION	RS-366
0	LL	1	LOCAL LOOP BACK	NB1
1	RL	1	REMOTE LOOP BACK	NB2
3	SF/SR	0	SELECT FREQUENCE/SELECT RATE	NB8
NOTE: All of the above lines are set to 0 at power-up				

Counter Timer Circuit (CTC)

The CTC (U43, A24, 6-1) provides four independent counter/timer channels. In the PSI card, these channels provide the following functions:

Channel 0 -- RQHDF : DMARQ1 (DMA ReQuest channel 1, which is RDY-) hold-off time from ZC/TO0.

Channel 1 -- 2XDCL K1: SIO channel B (primary channel) baud rate generator.

Channel 2 -- DCLK2 : SIO channel A (secondary channel) baud rate timer.

Channel 3: General purpose system timer.

NOTE

Because the output of the CTC consists of pulses, a divide-by-2 circuit is used to divide 2XDCLK1 into DCLK1, in order to provide a 50 percent duty cycle clock which is required for synchronous data transmission

To the Z-80A CPU, the CTC is an I/O addressable port; its addresses are defined in table 3-1, I/O Address Space. Tables 3-11 and 3-12 show how the baud rates are generated.

The CTC has two modes of operation: Counter mode and Timing mode. In Timing mode, an external clock of 1.8432 MHz is used as a clock source. In Counter mode, the system clock of 3.6864 MHz is used with a prescale of either 16 or 256. A programmable divider is used to divide the input clock and is given as the value N.

Table 3-11. Synchronous Baud Rate Generation

TIMER SOURCE	N	2XDCLK1 FREQ	BAUD RATE
1.8432 MHz PHI CTC Input to CTC (Counter mode)	2	921.6 KHz	460.8 KHz
	3	614.4 KHz	307.2 KHz
	4	460.8 KHz	230.4 KHz
	5	368.6 KHz	184.3 KHz
	6	307.2 KHz	153.6 KHz
	16	115.2 KHz	57.6 KHz
	18	102.4 KHz	51.2 KHz
	24	76.8 KHz	38.4 KHz
	32	57.6 KHz	28.8 KHz
	48	38.4 KHz	19.2 KHz
	96	19.2 KHz	9.6 KHz
	192	9.6 KHz	4.8 KHz
3.6864 MHz and DIV 16 Prescale (Timer mode)	32	7200 Hz	3600 Hz
	36	6400 Hz	3200 Hz
	48	4800 Hz	2400 Hz
	64	3600 Hz	1800 Hz
	72	3200 Hz	1600 Hz
	96	2400 Hz	1200 Hz
	128	1800 Hz	900 Hz
3.6864 MHz and DIV 256 prescale (Timer mode)	12	1200 Hz	600 Hz
	24	600 Hz	300 Hz
	36	400 Hz	200 Hz
	48	300 Hz	150 Hz
	65	220 Hz	110 Hz
	72	200 Hz	100 Hz
	96	150 Hz	75 Hz
	144	100 Hz	50 Hz

NOTE: In sync mode, 2XDCLK1 is divided by 2 before going to the SIO in order to create a 50% duty cycle (DCLK1).

Table 3-12. Asynchronous Baud Rate Generation

TIMER SOURCE	N	2XDCLK1 FREQ	BAUD RATE
1.8432 MHz input to CTC (Counter mode)	1	1843.2 KHz	115.2 KHz
	2	921.6 KHz	57.6 KHz
	3	614.4 KHz	38.4 KHz
	6	307.2 KHz	19.2 KHz
	12	153.6 KHz	9.6 KHz
	24	76.8 KHz	4.8 KHz
	32	57.6 KHz	3.6 KHz
	48	38.4 KHz	2.4 KHz
	64	28.8 KHz	1.8 KHz
	96	19.2 KHz	1.2 KHz
	128	14.4 KHz	900 Hz
	192	9.6 KHz	600 Hz
3.6864 MHz System clock divided by 16 prescale (Timer mode)	3	76.8 KHz	4.8 KHz
	4	57.6 KHz	3.6 KHz
	6	38.4 KHz	2.4 KHz
	8	28.8 KHz	1.8 KHz
	12	19.2 KHz	1.2 KHz
	16	14.4 KHz	900 Hz
	24	9.6 KHz	600 Hz
	48	4.8 KHz	300 Hz
	96	2.4 KHz	150 Hz
	107	2153.3 Hz	134.5 Hz (0.06% error)
	131	1758.8 Hz	110 Hz (0.07% error)
	192	1.2 KHz	75 Hz
3.6864 MHz System clock divided by 256 prescale (Timer mode)	1	14.4 KHz	900 Hz
	3	4.8 KHz	300 Hz
	5	2.88 KHz	180 Hz
	6	2.4 KHz	150 Hz
	9	1.6 KHz	100 Hz
	12	1.2 KHz	75 Hz
	18	800 Hz	50 Hz

NOTE: In async mode, th 2XDCLK1 (or DCLK2 for secondary channel) goes to the SIO at 16 times the baud rate.

I/O Channel (Backplane) Interface

The I/O channel, or backplane, interface consists of the Backplane Interface Circuit (BIC, U41, A14, 6-1) and buffers U11 through U14 (A13 and C17, 6-1).

The BIC is an I/O addressable port to the Z-80B CPU and handles byte-to-word conversion and backplane handshaking. To the Z-80B CPU, the BIC appears as a set of ten registers which are read only, write only, and bi-directional. To the I/O bus, the BIC appears as a set of six registers which also are read only, write only, and bi-directional.

The BIC registers available to the Z-80B are I/O mapped to hexadecimal addresses B0 to B6 as shown in table 3-1, I/O address space.

The contents of the BIC registers are shown in figure 3-7.

Memory Interface Circuit (MIC)

The MIC (U65, A32, 6-1) is a custom CMOS gate array which provides the following functions:

Controls up to 64K by 8 of dynamic RAM

Controls up to 16K by 8 of EPROM and/or static RAM

Two programmable DMA channels

Vectors backplane interrupts for Z-80B CPU

The MIC improves the effective bandwidth of the CPU by using DMA for data transfer to and from the SIO and to and from the BIC. This allows data transfers without the overhead of per-character interrupt handling. MIC registers and their contents are shown on the following pages.

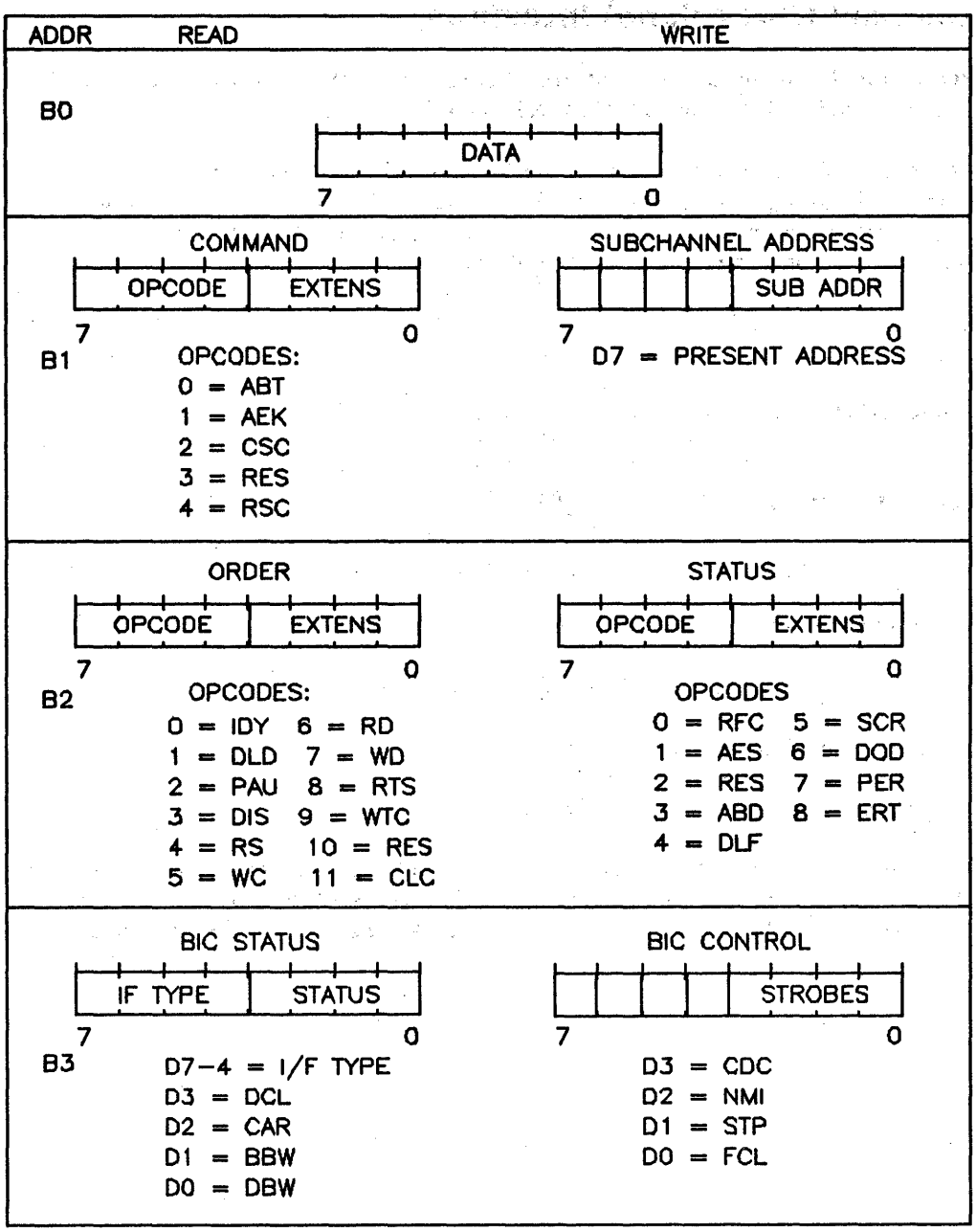


Figure 3-7. BIC Register Reference (Sheet 1 of 2)

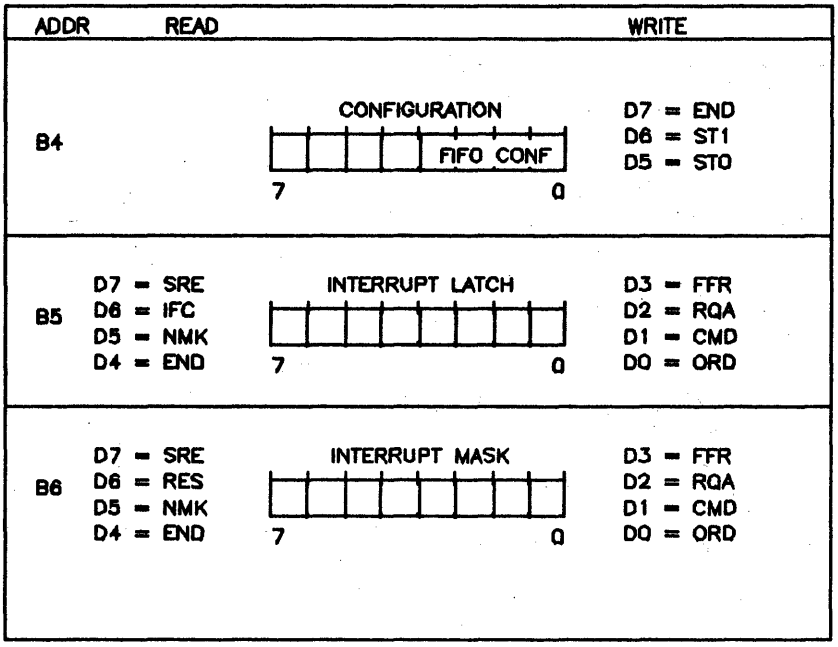
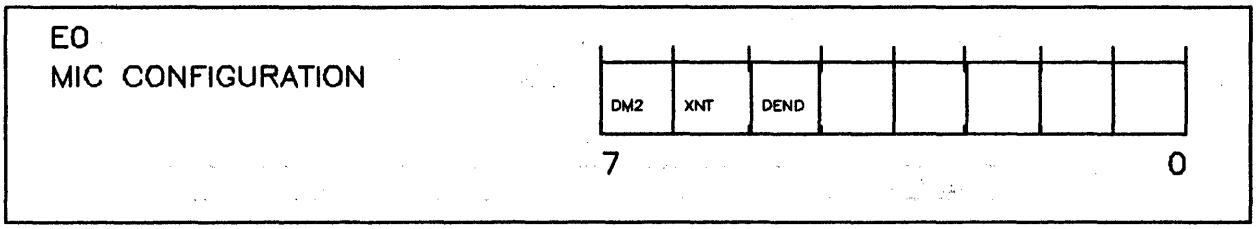


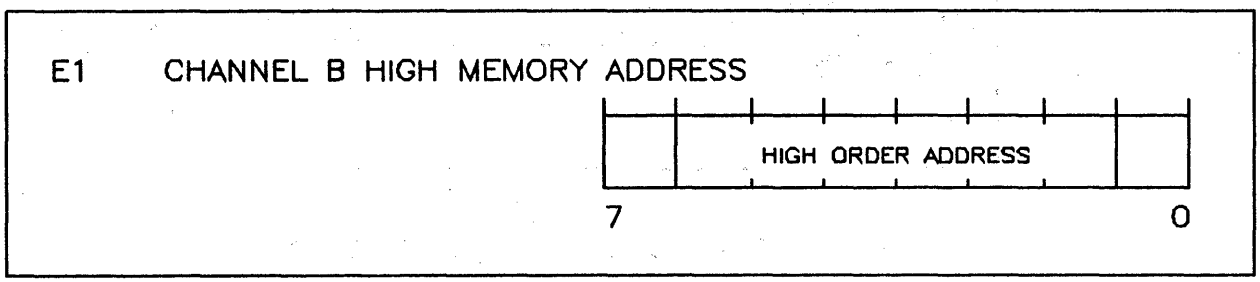
Figure 3-7. BIC Register Reference (Sheet 2 of 2)

MIC REGISTER 0 - CONFIGURATION.



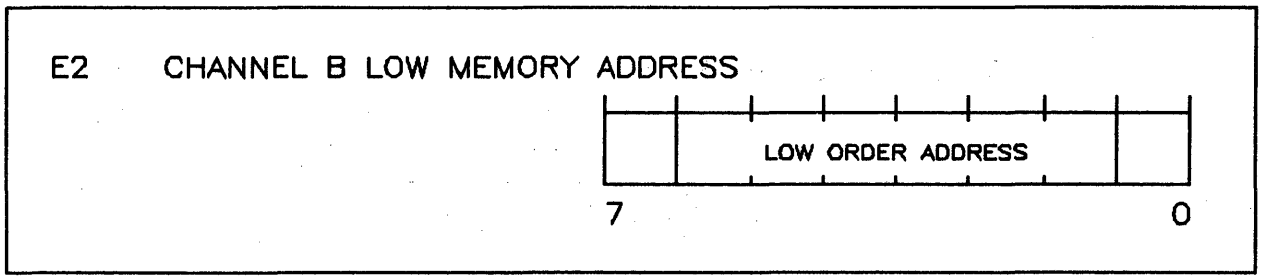
Bit 7 = DM2 DMA B request select (1 = DMAR2, 0 = DMAR1)
Bit 6 = XNT External Interrupt Enable (1 = ENABLE)
Bit 5 = DEND Disable XEND (1 = DISABLE)
Bits 4 - 0 Not used

MIC REGISTER 1 - CHANNEL B HIGH MEMORY ADDRESS.



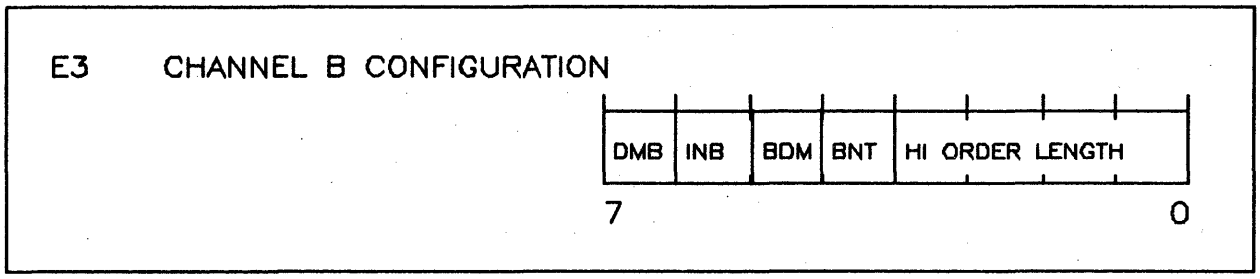
Write only register

MIC REGISTER 2 - CHANNEL B LOW MEMORY ADDRESS.



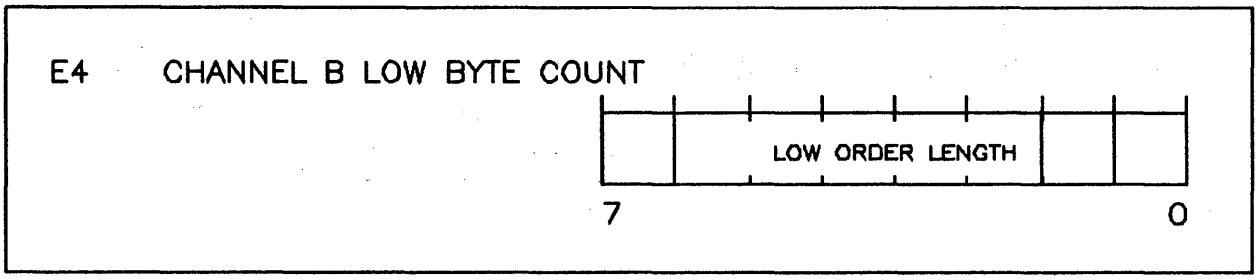
Write only register

MIC REGISTER 3 (HIGH BYTE COUNT) - CHANNEL B CONFIGURATION.

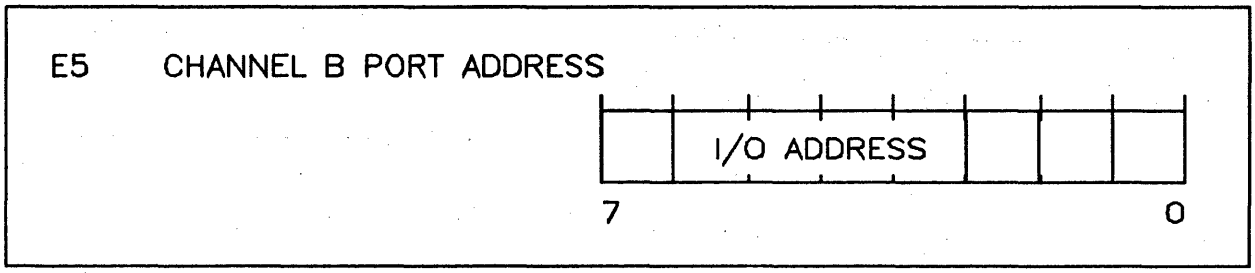


Bit 7 = DMB — DMA Channel B Enable (1 = ENABLE)
Bit 6 = INB — DMA Channel B Transfer Direction (1 = I/O to Memory, 0 = Memory to I/O)
Bit 5 = BDM — DMA B Address Count Direction (1 = Decrement, 0 = Increment)
Bit 4 = BNT — DMA B Interrupt Enable (1 = Enable)
Bit 3 =
Bit 2 =
Bit 1 =
Bit 0 = — Upper four bits of transfer byte count for DMA B

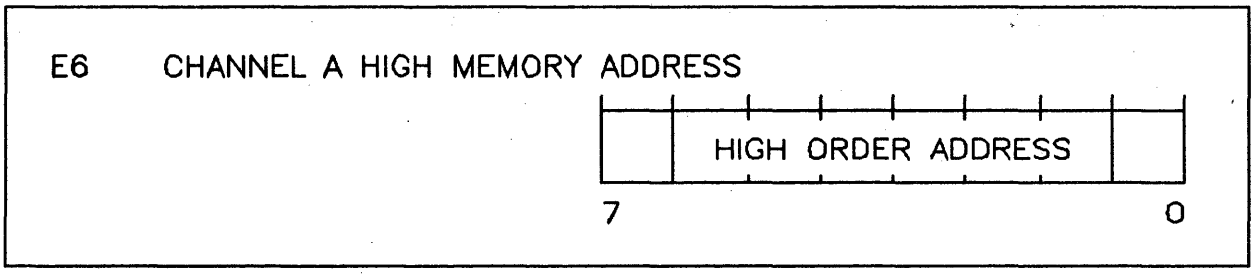
MIC REGISTER 4 - CHANNEL B LOW BYTE COUNT.



MIC REGISTER 5 - CHANNEL B PORT ADDRESS.

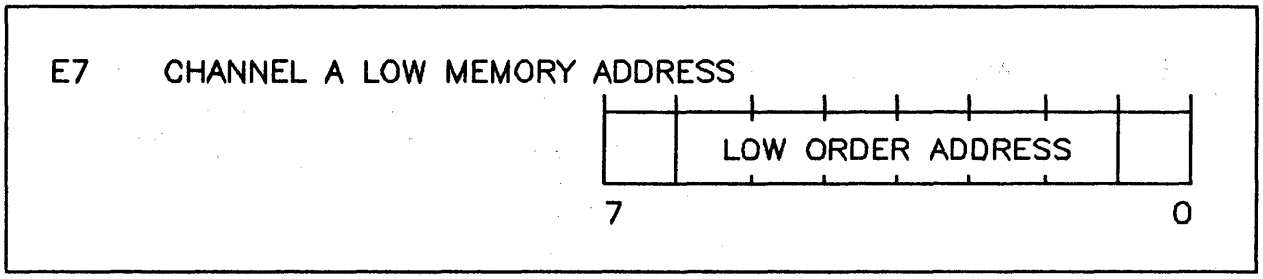


MIC REGISTER 6 - CHANNEL A HIGH MEMORY ADDRESS.



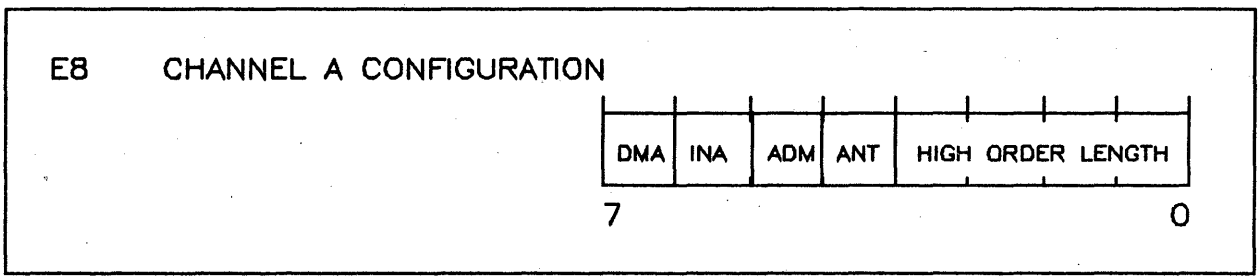
Write only register

MIC REGISTER 7 - CHANNEL A LOW MEMORY ADDRESS.



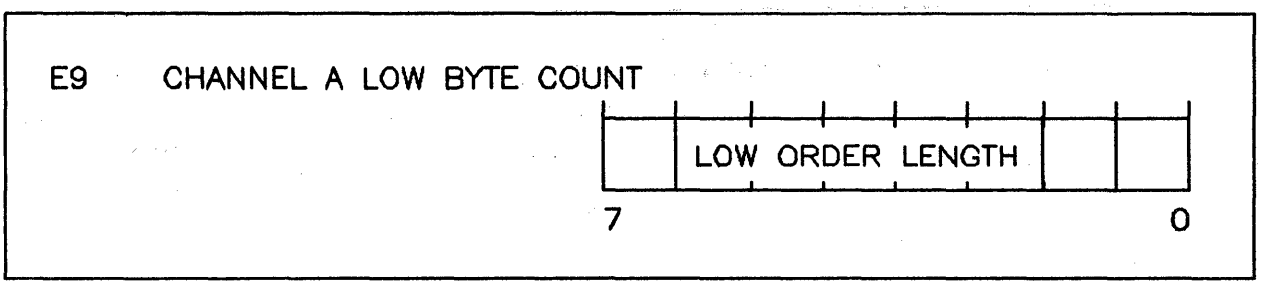
Write only register

MIC REGISTER 8 (HIGH BYTE COUNT) - CHANNEL A CONFIGURATION

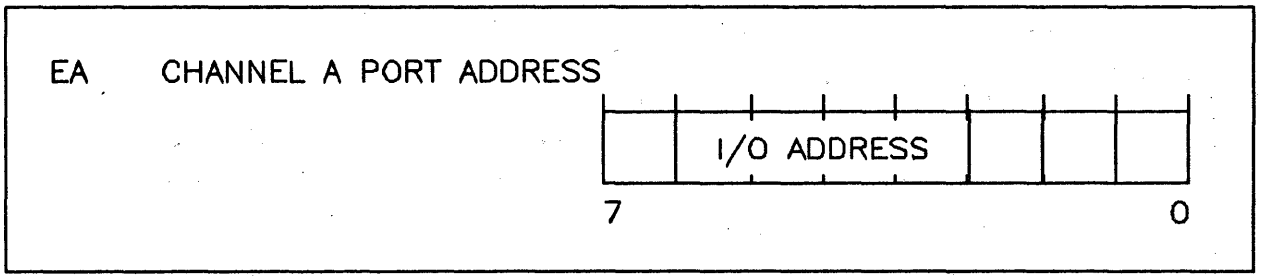



```
Bit 7 = DMA      DMA Channel A Enable (1 = ENABLE)
Bit 6 = INA      DMA Channel A Transfer Direction
                 (1 = I/O to Memory, 0 = Memory to I/O)
Bit 5 = ADM      DMA A Address Count Direction (1 = Decrement, 0 = Increment)
Bit 4 = ANT      DMA A Interrupt Enable (1 = ENABLE)
Bit 3 =
Bit 2 =          Upper four bits of transfer byte count for DMA A
Bit 1 =
Bit 0 =
```

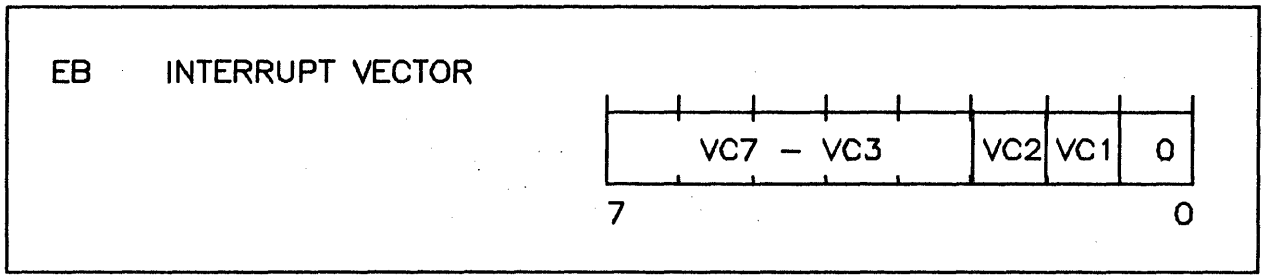
MIC REGISTER 9 - CHANNEL A LOW BYTE COUNT.



MIC REGISTER A - CHANNEL A PORT ADDRESS.



MIC REGISTER B - INTERRUPT VECTOR.




```
Bit 7 =
Bit 6 =    \
Bit 5 =     >---  Programmable portion of Interrupt vector
Bit 4 =    /
Bit 3 = 0
Bit 2 =    \
Bit 1 =     >---  Hardware-generated portion of interrupt vector
Bit 0 = 0       (00 = DMA A; 01 = DMA B; 10 = EXT INT; 11 = not used)
```

Priority Interrupt Structure

The CHANNEL I/O maskable interrupt structure convention is used by the PSI card. This interrupt structure is as follows:

```
Highest Priority  --  SIO/2 Channel A
        |             SIO/2 Channel B
        |             CTC Channel 0
        |             CTC Channel 1
        |             CTC Channel 2
        |             CTC Channel 3
        |             DMA 0
        |             DMA 1
Lowest Priority   --  BIC Interrupt
```

MAINTENANCE

SECTION IV

If the PSI card did not pass the self-test described in Section II, it is recommended that you return the card to Hewlett-Packard. If further testing is desired, however, a diagnostic test hood, which tests more or the card's circuitry during the built-in self-test, can be ordered. The diagnostic test hood part number is 1258-0207.

To test the PSI card using the diagnostic test hood, perform the following:

CAUTION

BE SURE TO INSTALL THE DIAGNOSTIC TEST HOOD SO THAT ITS COMPONENT SIDE (THE SIDE WITH THE LED) HAS THE SAME ORIENTATION AS THE COMPONENT SIDE ON THE PSI RJE CARD. DAMAGE TO THE PSI RJE CARD CAN RESULT IF THE TEST HOOD IS INSTALLED INCORRECTLY.

1. Turn computer system power off.
2. Connect the test hood to connector J2 on the card.
3. Refer to the appropriate computer system manual to determine if the self-test is run automatically at power-on, or only when specifically invoked by you.
4. Turn on computer system power.
5. When the self-test executes, the LED located on the card and the LED located on the test hood should simultaneously light briefly and go out if the card passed self-test. If either LED does not light at all, the card is defective. If either LED stays lit, the card did not pass self-test.

If desired, isolation to a defective part may be performed. Please be advised, however, that such work is at your discretion and is your responsibility; moreover, NOTE THAT CUSTOMER REPAIR OR MODIFICATION OF THE MUX CARD WILL INVALIDATE WARRANTY AND RENDER THE CARD INELIGIBLE FOR EXCHANGE OR REPAIR BY HEWLETT-PACKARD COMPANY. If such service is performed, the replaceable parts information in Section V and the schematic logic diagrams in Section VI will be of assistance.

REPLACEABLE PARTS

SECTION V

This section contains information for ordering replaceable parts for the PSI card. Table 5-1 contains a list of replaceable parts, table 5-2 contains the names and addresses of the manufacturers indexed by the code numbers used in table 5-1, and figure 5-1 shows the locations of the parts on the PSI card.

REPLACEABLE PARTS

Table 5-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY).
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to table 5-2 for a cross-reference of the manufacturers.
7. The manufacturer's part number.

ORDERING INFORMATION

To order replacement parts or to obtain information on parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the kit containing the part (refer to the product identification information supplied in Section II).

2. Description and function of the part.

3. Quantity required.

Table 5-1. PSI Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	5061-4920	6	1	PCA-HPIO PSI	28480	5061-4920
C1	0160-4832	4	12	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C2	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C3	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C4	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
C5	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C6	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C7	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C8	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C9	0160-4807	3	2	CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
C10	0160-4807	3		CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
C11	0160-4835	7	7	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0180-0100	3	1	CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C13	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C18	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C19	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C20	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C21	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C23	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C27	0160-3879	7	6	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
C28	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
C29	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
C30	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
C31	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
C32	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
CR1	1901-0518	8	2	DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR2	1901-0518	8		DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR3	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
CR4	1901-1068	5	2	DIODE-SM SIG SCHOTTKY	28480	1901-1068
CR5	1901-1068	5		DIODE-SM SIG SCHOTTKY	28480	1901-1068
CR6	1990-0486	6	1	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
F1	2110-0301	1	1	FUSE .125A 125V .281X.093	28480	2110-0301
F2	2110-0423	8	2	FUSE 1.5A 125V NTD .281X.093	28480	2110-0423
F3	2110-0423	8		FUSE 1.5A 125V NTD .281X.093	28480	2110-0423
J1	1251-7276	0	1	CONN-POST TYPE .100-PIN-SPCG 80-CONT	28480	1251-7276
J2	1251-7884	6	1	CONN-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7884
Q1	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
Q2	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
R1	0757-0279	0	5	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
R2	0698-0082	7	3	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R3	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R4	0757-0405	4	1	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
R5	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R6	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R7	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
R8	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
R9	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R10	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R11	1810-0278	4	2	NETWORK-RES 10-SIP3.3K OHM X 9	01121	210A332
R12	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
R13	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
R14	1810-0278	4		NETWORK-RES 10-SIP3.3K OHM X 9	01121	210A332
R15	0698-3446	3	2	RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
R16	0757-0199	3	6	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R17	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R18	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R19	1810-0517	4	2	NETWORK-RES 10-SIP6.0K OHM X 9	28480	1810-0517
R20	1810-0552	7	1	NETWORK-RES 6-SIP6.0K OHM X 5	28480	1810-0552
R21	1810-0280	8	1	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R22	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R23	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R24	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R25	1810-0517	4		NETWORK-RES 10-SIP6.0K OHM X 9	28480	1810-0517
R26	0698-4590	0	1	RESISTOR 422 1% .25W F TC=0+-100	24546	C5-1/4-T0-422R-F
R27	1810-0350	3	2	NETWORK-RES 8-SIP100.0 OHM X 4	01121	208B101
R28	1810-0350	3		NETWORK-RES 8-SIP100.0 OHM X 4	01121	208B101
R29	0698-3446	3		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
R30	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-1. PSI Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R31	0698-0083	8	1	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1961-F
R32	0698-3430	5	2	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R33	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
TP1	0360-0474	6	2	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0474
TP2	0360-0474	6		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0474
U11	1820-2862	7	2	IC-DS 3667	28480	1820-2862
U12	1820-2862	7		IC-DS 3667	28480	1820-2862
U13	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U14	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U15	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U23	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U24	1820-0684	7	1	IC INV TTL S HEX 1-INP	01295	SN74S05N
U41	1820-2975	3	1	IC-BIC C2000	28480	1820-2975
U43	1820-2301	9	1	IC-Z80A CTC	28480	1820-2301
U45	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U64	1820-2649	8	1	IC- Z80B-CPU	28480	1820-2649
U65	1820-2995	7	1	IC GATE-ARY CMOS	28480	1820-2995
U74	1820-2300	8	1	IC-Z80A SIO/2	28480	1820-2300
U75	1820-1645	2	1	IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
U81	1810-0661	9	1	NTWK-SHUNT	28480	1810-0661
U82	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U83	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U84	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U85	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U101	1820-1244	7	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U102	1820-1470	1	3	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U103	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U104	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U105	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U106	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U111	1820-2117	5	6	IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U112	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U113	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U114	1820-2831	0	1	ICD 75174 DRIVER	28480	1820-2831
U115	1820-2594	2	3	IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U116	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U117	1990-0655	1	2	OPTO-ISOLATOR LED-IC GATE IF=60MA-MAX	28480	HCPL-2602
U118	3101-2243	6	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
U121	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U122	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U123	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U126	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U127	1990-0655	1		OPTO-ISOLATOR LED-IC GATE IF=60MA-MAX	28480	HCPL-2602
W1	8159-0005	0	4	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W2	1251-2118	9	1	CONNECTOR-SGL CONT SKT .04-IN-BSC-SZ RND	28480	1251-2118
W2	1258-0142	9	1	PLUG-SHORTING 0.200IN CENTERS;INSULATED	71279	461-2872-01-03-10
W4	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W5	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W6	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
X61	1200-0567	1	2	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
X64	1200-0654	7	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
X71	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
XR27	1200-0940	4	2	SOCKET-STRP 8-CONT DIP DIP-SLDR	28480	1200-0940
XR28	1200-0940	4		SOCKET-STRP 8-CONT DIP DIP-SLDR	28480	1200-0940
XU81	1200-0607	0	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	5041-3467	2	1	HPIO EXTR HNDL	28480	5041-3467
	5180-0121	3	1	BURNIN 1818-1425	28480	5180-0121
	5180-0156	4	1	IC-RAM, 64K 75NS	28480	5180-0156
	5180-1960	0	1	PCB-HPIO PSI	28480	5180-1960

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-2. Manufacturer's Code List

MFR. NO.	MANUFACTURER'S NAME	ADDRESS	ZIP CODE
01121	Allen-Bradley Company	Milwaukee, Wi.	53204
01295	Texas Instruments, Inc. Semiconductor Components Div.	Dallas, Tx.	75222
03888	K D I Pyrofilm Corp.	Whippany, N.J.	07981
07263	Fairchild Semiconductor Div.	Mountain View, Ca.	94042
24546	Corning Glass Works (Bradford)	Bradford, Pa.	16701
28480	Hewlett-Packard Co., Corporate HQ.	Palo Alto, Ca.	94304
56289	Sprague Electric Co.	North Adams, Ma.	01247
71279	Cambridge Thermionic Corp.	Cambridge, Ma.	02138

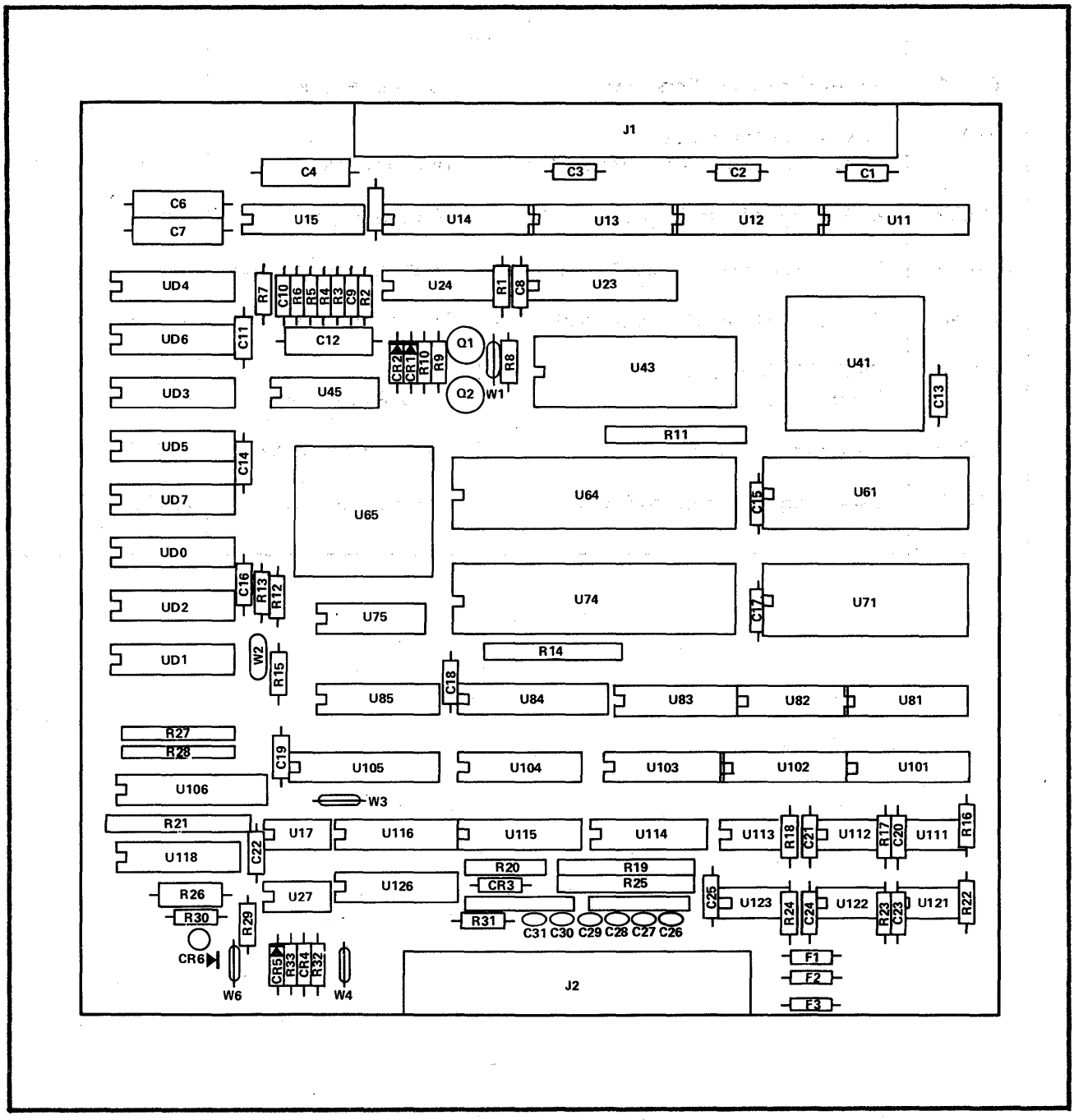


Figure 5-1. PSI Parts Location Diagram

SCHEMATIC DIAGRAMS

SECTION VI

This section contains schematic logic diagrams for the PSI card.

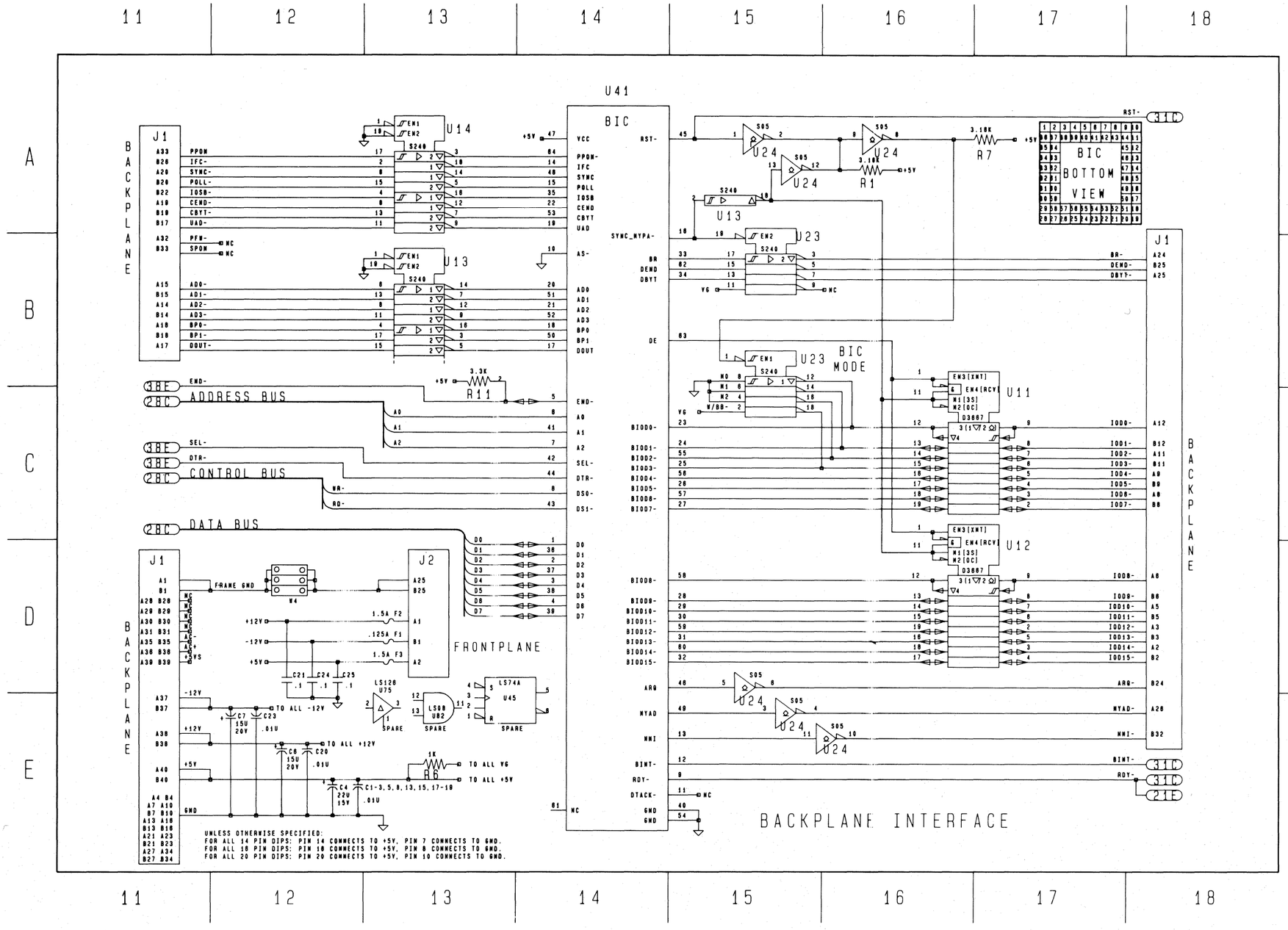


Figure 6-1. PSI Schematic Logic Diagram (Sheet 1 of 4)

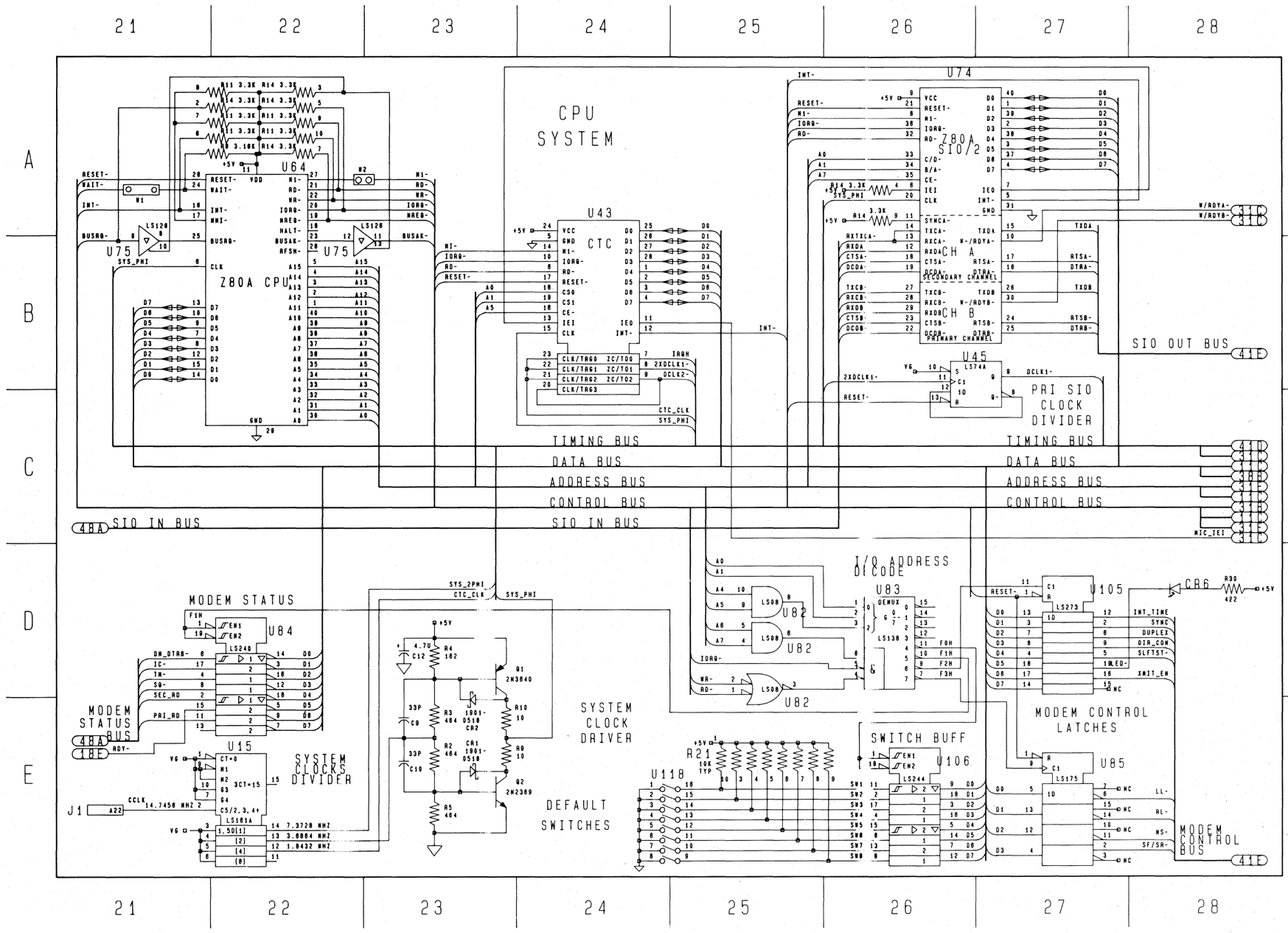


Figure 6-1. PSI Schematic Logic Diagram (Sheet 2 of 4)

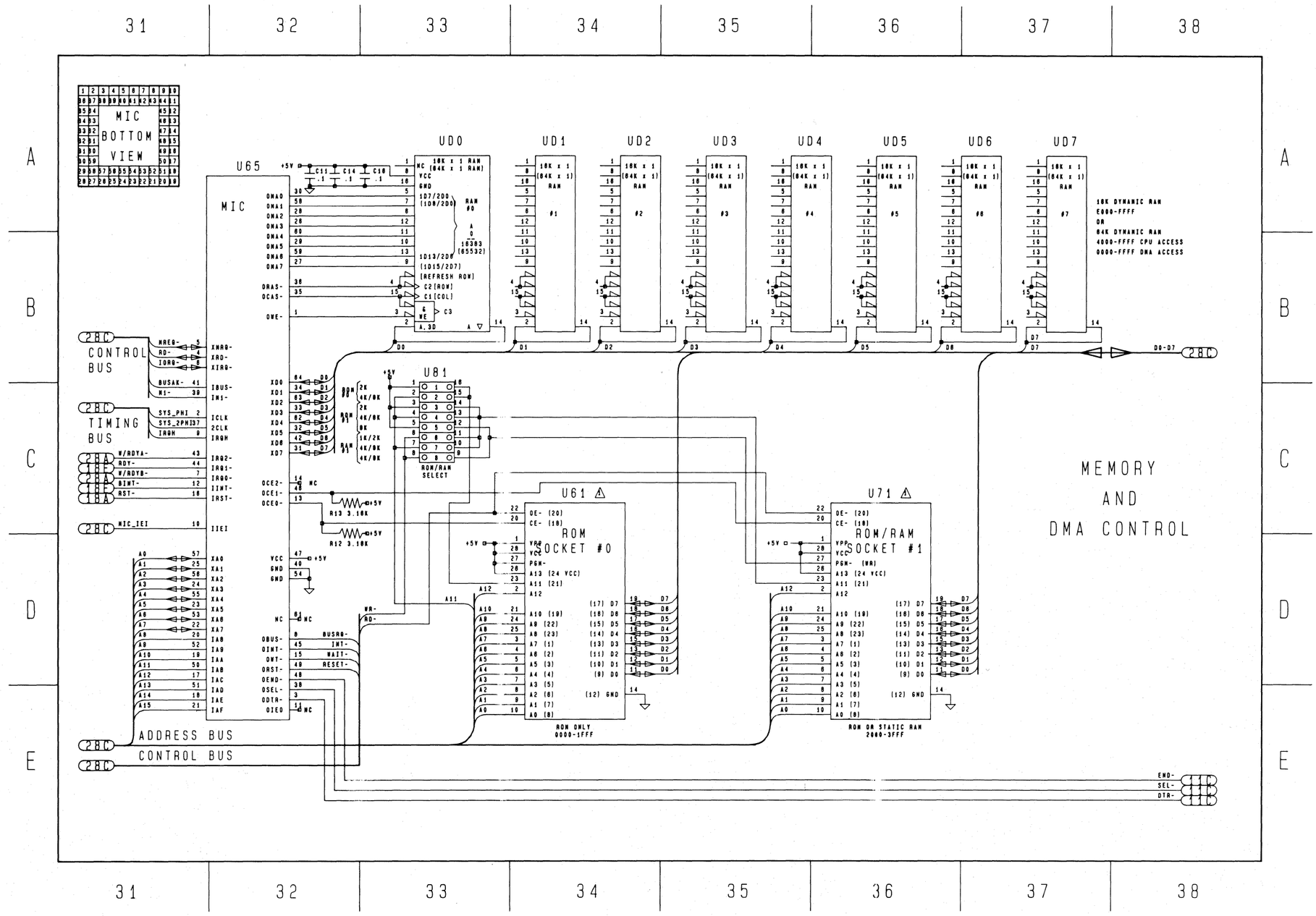


Figure 6-1. PSI Schematic Logic Diagram (Sheet 3 of 4)

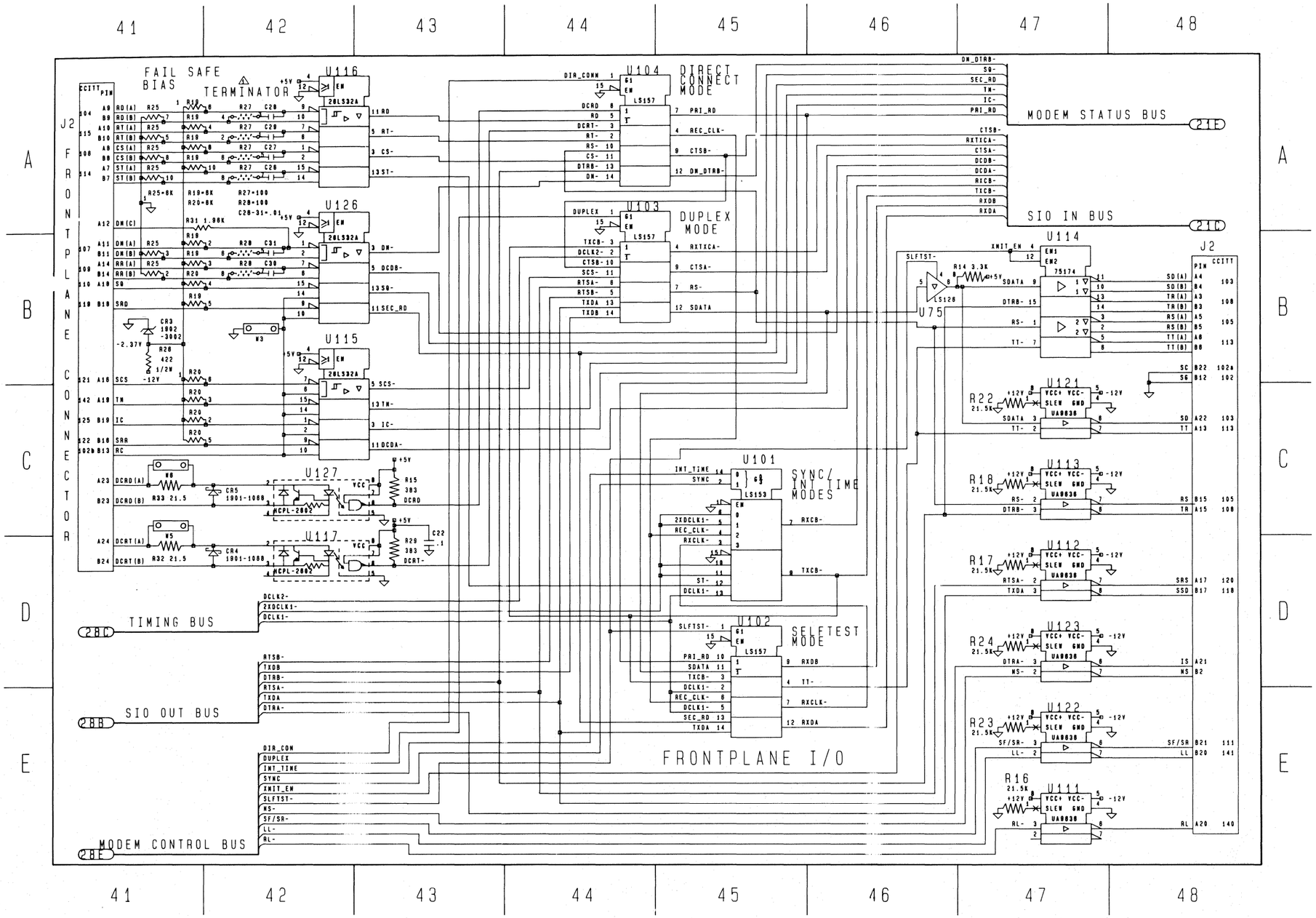


Figure 6-1. PSI Schematic Logic Diagram (Sheet 4 of 4)

ASCII CHARACTERS AND BINARY CODES

APPENDIX A

	0	1	2	3	4	5	6	7
0	NUL	DLE	sp	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3		3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

INDEX

INDEX

MANUAL PART NO. 27132-90005
Printed in U.S.A.
June, 1983

HEWLETT-PACKARD COMPANY
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678