HEWLETT hp PACKARD

OPERATING AND SERVICE MANUAL

12578A
12578A-01

DIRECT MEMORY ACCESS
COMPUTER ACCESSORY KITS

(FOR 2115A, 2116A, 2116B, AND 2116C COMPUTERS)

Note

This manual should be retained with Volume Two of the computer documentation.

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SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This operating and service manual covers general information, installation, programming, theory of operation, and maintenance instructions for the Hewlett-Packard 12578A and 12578A-01 Direct Memory Access Computer Accessory Kits for the HP 2115 and HP 2116 Computers.

1-3. GENERAL DESCRIPTION.

1-4. Direct memory access (DMA) enables the computer to transfer data directly between memory and external devices at a maximum rate of 625,000 16-bit words-per-second in block lengths from 1 to 16,384 words. The DMA system consists of two separate, independent, high-priority control channels. Either or both DMA channels may be switched under program control between computer memory and any device normally serviced through the I/O system of the computer mainframe.

1-5. The DMA option consists of five printed circuit cards that plug directly into the computer mainframe. The cards consist of two DMA register assemblies, a DMA control assembly, a DMA address encoder assembly, and a DMA character packer assembly. The combination of these assemblies permits direct data transfer in either direction between an external device and computer memory using one machine cycle per 16-bit word transfer. Refer to table 1-1 for a complete listing of the plug-in assemblies supplied with the DMA option.

Table 1-1. Plug-In Assemblies Required for Installation and Operation of the DMA Option

HP PART NO.	DESCRIPTION	REFERENCE DESIGNATION			QUANTITY REQUIRED OR SUPPLIED
		HP 2115	HP 2116A/B	HP 2116C	
02116-6203	Printed Circuit Board Assembly: DMA Character Packer	A23	A120	A5	1*
02116-6204	Printed Circuit Board Assembly: DMA Control	A22	A119	A4	1*
02116-6205	Printed Circuit Board Assembly: DMA Address Encoder	A21	A118	A3	1*
02116-6206	Printed Circuit Board Assembly: DMA Register	A122, A123	A116, A117	A1, A2	2*
02115-6044 or 02116-6069	Printed Circuit Board Assembly: Direct Memory Logic	A20	2116A-A113; 2116B-A20	—	1 or 1**
02115-6015	Printed Circuit Board Assembly: I/O Control	A18	—	—	1***
02116-6041	Printed Circuit Board Assembly: I/O Control	—	A201	A201	1***

* Supplied with HP 12578A and HP 12578A-01 Modification Kits.

** Either 02115-6044, board revision B-821, B-904, or later, or 02116-6069, board revision J-905, J-907, or later is required. An 02115-6044 board revision B-904, or later, is supplied with HP 12578A-01 Modification Kit.

*** Board revision 822 or later is required, but not supplied with modification kits.

1-6. To be placed in operation, the two DMA channels must first be initialized for a specific operating mode by instructions and control words in the main program. Data interchange then occurs automatically over DMA channel 1 or DMA channel 2 when a service request command signal is received from an I/O channel programmed to DMA. The DMA channel receiving the service request takes control of the central processor and I/O system, suspends the running program at the end of the current phase, and, during the following machine cycle, generates a special phase 5 memory cycle to read or write a word directly into or out of a predetermined memory location. At the end of the phase 5 memory cycle (one complete machine cycle), control is returned to the central processor and I/O system, and the main program is automatically resumed at the point where it was suspended, without loss of continuity. A new phase 5 cycle is initiated each time the I/O channel signals to DMA that it is ready to input or output another word. When all data in a predetermined block length has been transferred, the DMA channel initiates a normal interrupt to a service subroutine.

1-7. An important feature of DMA is the capability of conserving memory space by packing two 8-bit input characters (bytes) into a 16-bit character word format and storing the word in a single memory location. Character words from memory are divided into two separate eight-bit byte outputs by an unpacking process. Character packing/unpacking is a program option that is turned on or off by a single control bit during DMA channel initialization, and can be used only with external devices that employ eight-bit characters.

1-8. IDENTIFICATION.

1-9. Printed-circuit card revisions are identified by a letter and a date code stamped on the card. The letter code identifies the version of the etched trace pattern on the unloaded card. The date code refers to the electrical characteristics of the loaded card. If the date code stamped on the printed circuit card does not agree with the date code shown on the schematic diagram in section IV of this manual for the DMA card, there are differences between your card and the card described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office.

1-10. CURRENT REQUIRED FROM COMPUTER.

1-11. To operate the logic circuits, the plug-in cards require a total of 6.2 amperes from the +4.5-volt computer power supply and 720 milliamperes from the -2-volt computer power supply.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information on unpacking and inspection, and on field and factory installation of the DMA option.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the equipment is unpacked. Inspect the assemblies for damage (scratches, cracks, loose components, etc.). If the equipment is damaged or fails to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the padding material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged instrument without waiting for any claims against the carrier to be settled.

2-5. FACTORY INSTALLATION.

2-6. If purchased as part of an initial computer order or if added to computers bearing serial number prefixes prior to 746-, the DMA option is installed at the factory and is ready for operation upon receipt of the equipment. When the computer is installed, conduct a performance test of the DMA option in accordance with the test instructions presented in the maintenance section of this manual. If test results are satisfactory, the DMA option is ready for normal use.

2-7. FIELD INSTALLATION.

2-8. Field installation of the DMA option consists of incorporating the plug-in assemblies furnished in the DMA modification kit (refer to table 1-1) into the computer. It may be necessary, however, to make other modifications as specified in table 2-1 before incorporating the DMA kit items, depending on the model and serial number prefix of the computer. Note that Modification Kit HP 12578A-01 includes direct memory logic (DML) assembly 02115-6044, revision B-904 or later, for computers not already equipped with either the 02115-6044 assembly or DML assembly 02116-6069, revision J-907 or later. The I/O control assemblies specified in tables 1-1 and 2-1 are not supplied with either modification kit and must be ordered separately, if required.

2-9. To field install the DMA option, proceed as follows:

a. Check the serial number prefix of the computer in which the DMA option is to be installed. Then carefully review the information presented in table 2-1 that applies to that prefix. Make sure that the necessary modifications have been made, or that the necessary materials and instructions are at hand to make them, before proceeding with the following steps. If further information or assistance is required, consult the nearest Hewlett-Packard Sales and Service Office listed at the back of this manual.

b. Check to ensure that when the DMA option cards are added to the computer the current drain on the power supply will not exceed the limits specified in Volume Three.

c. Set the computer POWER switch to OFF.

d. Using the cards supplied in the modification kit, configure the computer as indicated in table 1-1.

e. Recheck the information presented in table 1-1 and table 2-1 to ensure that the computer is configured as specified.

f. Set the POWER switch to ON and observe whether power turn-on is normal. If normal, conduct a performance test of the DMA option in accordance with the test instructions presented in the maintenance section of this manual. If test results are normal, the DMA option may be programmed for operation.

g. If the plug-in card assemblies in slots A18 or A20 of the HP 2115A Computer, slots A113 or A201 of the HP 2116A Computer, or slots A20 or A201 of the HP 2116B Computer, were replaced with assemblies of a later revision, return the obsolete assemblies to the nearest Hewlett-Packard Sales and Service Office.

h. Run the Diagnostic Program Procedure, part no. 12578-90013, contained in the *Manual of Diagnostics* to verify that the DMA accessory kit is operating properly.

Table 2-1. Field Installation Checklist

MODEL	*SERIAL NUMBER PREFIX	MODIFICATIONS REQUIRED FOR INCORPORATION OF DMA OPTION	SERIAL NUMBER PREFIX AFTER MODIFICATION
		Note For information concerning computers with serial number prefixes other than those specified in this table, consult the nearest Hewlett-Packard Sales and Service Office.	
HP 2115A	744- 817- 818- 819-	1. BACKPLANE. Backplane wiring modifications are required prior to installation and operation of the DMA option. These modifications update the subject computers to the 823- configuration. Consult the nearest Hewlett-Packard Sales and Service Office for assistance in making this change. 2. I/O CONTROL CARD. The I/O control card originally supplied in slot A18 of the subject computers must be replaced with I/O control card 02115-6015, revision 822 or later, to make the I/O system of these computers compatible with the DMA option. 3. INTERRUPT PRIORITY JUMPER. Jumper-wire W1 on front panel coupler card 02115-6011, located in slot A8, must be removed when the DMA option is incorporated into the subject computers. This change connects select codes 06 and 07 into the interrupt system priority structure. Refer to Volume III for detailed information concerning this change. 4. MODIFICATION KIT. Installation of the items supplied in the HP 12578A-01** Modification Kit completes the DMA modification requirements for the subject computers.	823-
	827- 828-	1. BACKPLANE. Backplane wiring modifications are required prior to installation and operation of the DMA option. These modifications update the subject computers to the 831- configuration. Consult the nearest Hewlett-Packard Sales and Service Office for assistance in making this change. 2. INTERRUPT PRIORITY JUMPER. Jumper-wire W1 on front panel coupler card 02115-6011, located in slot A8, must be removed when the DMA option is incorporated into the subject computers. This change connects select codes 06 and 07 into the interrupt system priority structure. Refer to volume III for detailed information concerning this change. 3. MODIFICATION KIT. Installation of the items supplied in the HP 12578A-01** Modification Kit completes the DMA modification requirements for the subject computers.	831-

Table 2-1. Field Installation Checklist (Continued)

MODEL	*SERIAL NUMBER PREFIX	MODIFICATIONS REQUIRED FOR INCORPORATION OF DMA OPTION	SERIAL NUMBER PREFIX AFTER MODIFICATION
	839-	1. BACKPLANE. Backplane wiring modifications are required prior to installation and operation of the DMA option. These modifications update the subject computer to the 904- configuration. Consult the nearest Hewlett-Packard Sales and Service Office for assistance in making this change. 2. INTERRUPT PRIORITY JUMPER. Jumper-wire W1 on front panel coupler card 02115-6011, located in slot A8, must be removed when the DMA option is incorporated into the subject computer. This change connects select codes 06 and 07 into the interrupt system priority structure. Refer to volume III for detailed information concerning this change. 3. MODIFICATION KIT. Installation of the items supplied in the HP 12578A-01** Modification Kit completes the DMA modification required for the subject computer.	904-
	904- and above	1. INTERRUPT PRIORITY JUMPER. Same as item 2 for the 839- configuration. 2. MODIFICATION KIT. Same as item 3 for the 839- configuration.	No Change
HP 2116A	All prior to 746-	1. FACTORY MODIFICATIONS. Computers having serial number prefixes prior to 803- must be returned to the factory for mechanical and electrical modifications before the DMA option can be incorporated. 2. MODIFICATION KIT. The items supplied in the HP 12578A-01** Modification Kit are installed in the subject computers at the factory before reshipment to the user.	803-
	746- 749-	1. BACKPLANE. Backplane wiring modifications are required prior to installation and operation of the DMA option. These modifications update the subject computers to the 803- configuration. Consult the nearest Hewlett-Packard Sales and Service Office for assistance in making this change. 2. I/O CONTROL CARD. The I/O control card originally supplied in slot A201 of the subject computers must be replaced with I/O control card 02116-6041, revision 822 or later, to make the I/O system compatible with the DMA option.	803-

Table 2-1. Field Installation Checklist (Continued)

MODEL	*SERIAL NUMBER PREFIX	MODIFICATIONS REQUIRED FOR INCORPORATION OF DMA OPTIONS	SERIAL NUMBER PREFIX AFTER MODIFICATION
		3. INTERRUPT PRIORITY JUMPERS. If power turn-on card 02116-6095, revision 734- or later, or power-fail interrupt card 02116-6175 is installed in slot A115, a jumper-wire change must be made on either card when the DMA option is installed. This change is required to connect select codes 06 and 07 into the interrupt priority structure. If the power turn-on card resides in slot A115, jumper-wire W9 must be removed from the card. If the power fail interrupt card resides in slot A115, jumper-wire W2 must be removed from the card. Refer to volume III for detailed information concerning this change. 4. MODIFICATION KIT. Installation of the items supplied in the HP 12578A-01** Modification Kit completes the DMA modification requirements for the subject computers.	
	747- 750-	1. BACKPLANE. Backplane wiring modifications are required prior to installation and operation of the DMA option. These modifications update the subject computers to the 807- configuration. Consult the nearest Hewlett-Packard Sales and Service Office for assistance in making this change. 2. I/O CONTROL CARD. The I/O control card originally supplied in slot A201 of the subject computers must be replaced with I/O control card 02116-6041, revision 822 or later, to make the I/O system compatible with the DMA option. 3. INTERRUPT PRIORITY JUMPERS. If power turn-on card 02116-6095, revision 734 or later, or power-fail interrupt card 02116-6175 is installed in slot A115, a jumper-wire change must be made on either card when the DMA option is installed. This change is required to connect select codes 06 and 07 into the interrupt priority structure. If the power fail interrupt card resides in slot A115, jumper-wire W2 must be removed from the card. Refer to volume III for detailed information concerning this change. 4. MODIFICATION KIT. Installation of the items supplied in the HP 12578A-01** Modification Kit completes the DMA modification requirements for the subject computers.	807-

Table 2-1. Field Installation Checklist (Continued)

MODEL	*SERIAL NUMBER PREFIX	MODIFICATIONS REQUIRED FOR INCORPORATION OF DMA OPTION	SERIAL NUMBER PREFIX AFTER MODIFICATION
HP 2116B	823- 824-	1. BACKPLANE. Backplane wiring modifications are required prior to installation and operation of the DMA option. These modifications update the subject computers to the 830- configuration. Consult the nearest Hewlett-Packard Sales and Service Office for assistance in making this change. 2. INTERRUPT PRIORITY JUMPER. Jumper wire W2 on I/O control card 02116-6041, located in slot A201, must be removed when the DMA option is incorporated into the subject computers. This change connects select codes 06 and 07 into the interrupt system priority structure. Refer to volume III for detailed information concerning this change. 3. MODIFICATION KIT. Installation of the items supplied in the HP 12578A Modification Kit completes the DMA modification for the subject computers.	830-
	842-	1. BACKPLANE. Backplane wiring modifications are required prior to installation and operation of the DMA option. These modifications update the subject computer to the 844- configuration. Consult the nearest Hewlett-Packard Sales and Service Office for assistance in making this change. 2. INTERRUPT PRIORITY JUMPER. Jumper-wire W2 on I/O control card 02116-6041, located in slot A201, must be removed when the DMA option is incorporated into the subject computer. This change connects select codes 06 and 07 into the interrupt system priority structure. Refer to volume III for detailed information concerning this change. 3. MODIFICATION KIT. Installation of the items supplied in the HP 12578A Modification Kit completes the DMA modification for the subject computer.	844-
	846-	1. BACKPLANE. Backplane wiring modifications are required prior to installation and operation of the DMA option. These modifications update the subject computer to the 852- configuration. Consult the nearest Hewlett-Packard Sales and Service Office for assistance in making this change. 2. INTERRUPT PRIORITY JUMPER. Jumper-wire W2 on I/O control card 02116-6041, located in slot A201, must be removed when the DMA option is incorporated into the subject computer. This change connects select codes 06 and 07 into the interrupt system priority structure. Refer to volume III for detailed information concerning this change. 3. MODIFICATION KIT. Installation of the items supplied in the HP 12578A Modification Kit completes the DMA modification for the subject computer.	852-

Table 2-1. Field Installation Checklist (Continued)

MODEL	*SERIAL NUMBER PREFIX	MODIFICATIONS REQUIRED FOR INCORPORATION OF DMA OPTION	SERIAL NUMBER PREFIX AFTER MODIFICATION
HP 2116C	850-	1. BACKPLANE. Backplane wiring modifications are required prior to installation and operation of the DMA option. These modifications update the subject computer to the 900- configuration. Consult the nearest Hewlett-Packard Sales and Service Office for assistance in making this change. 2. INTERRUPT PRIORITY JUMPER. Jumper-wire W2 on I/O control card 02116-6041, located in slot A201, must be removed when the DMA option is incorporated into the subject computer. This change connects select codes 06 and 07 into the interrupt system priority structure. Refer to volume III for detailed information concerning this change. 3. MODIFICATION KIT. Installation of the items supplied in the HP 12578A Modification Kit completes the DMA modification for the subject computer.	900-
	845- and 842- and above	1. INTERRUPT PRIORITY JUMPER. Same as item 2 for the 850- configuration. 2. MODIFICATION KIT. Same as item 3 for the 850- configuration.	No Change
	980- and above	1. INTERRUPT PRIORITY JUMPER. Same as item 2 for the HP 2116B 850- configuration. 2. MODIFICATION KIT. Same as item 3 for the HP 2116B 850- configuration.	No Change

* Refers to serial number prefixes assigned at time of manufacture or prefixes assigned as a result of field changes.

** The HP 12578A-01 Modification Kit must be used with computers not equipped with direct memory logic card 02116-6044, revision B-821 or later, or direct memory logic card 02116-6069, revision J-905 or later. If the computer is already equipped with either of these cards, HP 12578A Modification Kit may be used.

*** Computers bearing serial number prefix 850- are used in 2000A System.

SECTION III
PROGRAMMING

3-1. INTRODUCTION.

3-2. This section contains programming information for use with the DMA option, including program word formats and a typical DMA program.

3-3. PROGRAM WORD FORMATS.

3-4. The DMA option is programmed using HP assembler language. The instruction, control, and data word formats used in the operation of DMA are shown in figure 3-1 and are defined below.

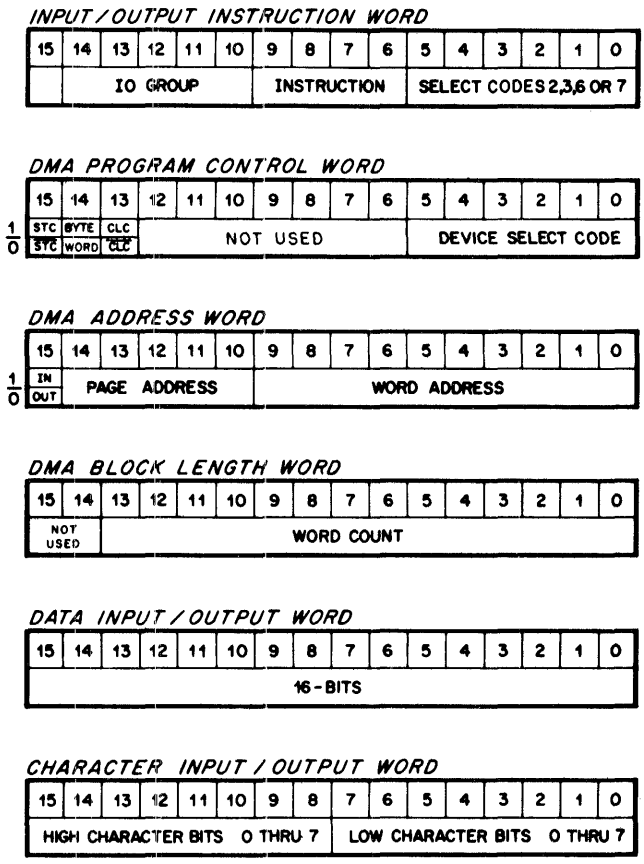


Figure 3-1. DMA Instruction and Control Word Formats

a. Input-output instruction words. I/O group instructions addressed to select codes 2, 3, 6, or 7, that permit the central processor to control the following DMA functions through the I/O select code addresses specified:

(1) Select code 2: permits control FF on DMA channel 1 register assembly to be addressed by CLC and STC instructions.

(2) Select code 2 (preceded by CLC instruction): permits DMA channel 1 memory address register to be addressed by an OTA instruction.

(3) Select code 2 (preceded by STC instruction): permits DMA channel 1 word count register to be addressed by OTA and LIA instructions.

(4) Select code 3: permits control FF on DMA channel 2 register assembly to be addressed by CLC and STC instructions.

(5) Select code 3 (preceded by CLC instruction): permits DMA channel 2 memory address register to be addressed by an OTA instruction.

(6) Select code 3 (preceded by STC instruction): permits DMA channel 2 word count register to be addressed by OTA and LIA instructions.

(7) Select code 6: permits DMA channel 1 switching functions to be addressed by OTA, CLC, STC, CLF, STF, SFC, and SFS instructions.

b. DMA program control words. Program constants that can be programmed to either DMA channel (select codes 6 or 7) to specify the following:

(1) The I/O channel select code address of the device to be serviced by the DMA channel (bits 0 through 5).

(2) Clear (turn off) control on device I/O channel after last word or byte in data block is transferred (bit 13 = 1).

(3) Do not clear control on device I/O channel (bit 13 = 0).

(4) Use character packing mode if memory input transfer or use character unpacking mode if memory output transfer (bit 14 = 1).

(5) Word input/output mode (bit 14 = 0).

(6) Set (turn on) control on device I/O channel after each word or byte in data block is transferred (bit 15 = 1).

(7) Do not set control on device I/O channel (bit 15 = 0).

c. DMA address words. Program constants that can be programmed to either DMA channel (select code 2 or 3) to specify the following:

(1) Starting memory address for first word of input/output data block (bits 0 through 14).

(2) Memory input from device I/O channel (bit 15 = 1).

(3) Memory output to device I/O channel (bit 15 = 0).

d. DMA block length words. Program constants that can be programmed to either DMA channel (select code 2 or 3) to specify the number of words in data block. Word count is a decimal number expressed as the two's complement of its positive binary equivalent.

e. Data input/output words. Conventional data word format used to transfer data directly between the device I/O channel and memory.

f. Character input/output words. A word format used to transfer two character bytes between memory and the DMA packing/unpacking function.

3-5. TYPICAL DMA PROGRAM.

3-6. A typical program example using the DMA option is presented in table 3-1. The first part of this presentation lists a memory input operation where it is desired to read a block of 100 bytes (50_{10} words) from a paper tape reader and store the resulting character words (two bytes per word) in computer memory locations 200_8 through 261_8. The second part of this presentation lists a memory output operation where it is desired to transfer a block of 4096_{10} words from computer memory locations $10{,}000_8$ through 17677_8 to a disc memory unit. This program assumes first that the paper tape reader is assigned to I/O channel select code 10_8 and that DMA channel 1 will be used for the input transfer, and second that the disc memory unit is assigned to I/O channel select codes 22_8 and 23_8 and that DMA channel 2 will be used for the output transfer.

Note

The following program assumes that the interrupt system is enabled (STF0 instruction), and that the DMA channels will initiate an interrupt to a service subroutine when all words in the assigned data block have been transferred. It should be noted, however, that data transfer via the DMA channels can also be accomplished by turning off the interrupt system (CLF0 instruction) and using SFS or SFC instructions programmed to select code addresses 6 and 7 to monitor data transfer between computer memory and the external device.

Table 3-1. Typical DMA Program

LABEL	OP CODE	OPERAND	REMARKS
			INITIALIZE DMA CHANNEL 1:
ASGN1	LDA	CW1	Fetches control word 1 (CW1) from memory and loads it in A-register.
	OTA	6	Outputs CW1 to DMA channel 1.
MAR1	CLC	2	Prepares DMA channel 1 memory address register to receive and store control word 2 (CW2).
	LDA	CW2	Fetches CW2 from memory and loads it in A-register.
	OTA	2	Outputs CW2 to DMA channel 1.
WCR1	STC	2	Prepares DMA channel 1 word count register to receive and store control word 3 (CW3).
	LDA	CW3	Fetches CW3 from memory and loads it in A-register.
	OTA	2	Outputs CW3 to DMA channel 1.
			START (STRT) DEVICE AND CHANNEL:
STRT1	STC	10B,C	Initiate paper tape reader data transfer.
	STC	6B,C	Activate DMA channel 1.
			DATA TRANSFER DMA CHANNEL 1:
⋮	⋮	⋮	Continue program while data transfer takes place.

Table 3-1. Typical DMA Program

LABEL	OP CODE	OPERAND	REMARKS
			INITIALIZE DMA CHANNEL 2:
ASGN2	LDA	CW4	Fetches control word 4 (CW4) from memory and loads it in A-register.
	OTA	7	Outputs CW4 to DMA channel 2.
MAR2	CLC	3	Prepares DMA channel 2 memory address register to receive and store control word 5 (CW5).
	LDA	CW5	Fetches CW5 from memory and loads it in A-register.
	OTA	3	Outputs CW5 to DMA channel 2.
WRC2	STC	3	Prepares DMA channel 2 word count register to receive and store control word 6 (CW6).
	LDA	CW6	Fetches CW6 from memory and loads it in A-register.
	OTA	3	Outputs CW6 to DMA channel 2.
			INITIALIZE DISC MEMORY:
ASGN23	LDA	CW7	Fetches control word 7 (CW7) from memory and loads it in A-register.
	OTA	23B	Outputs CW7 to I/O channel 23_8.
			START CHANNEL AND DEVICE:
STRT2	STC	7,C	Active DMA channel 2.
	STC	22B	Initiate disc memory data transfer.
			DATA TRANSFER DMA CHANNEL 2:
. . .	. . .	. . .	Continue program while data transfer takes place.
			DMA CHANNEL 1 CONTROL WORDS:
CW1	OCT	160010	Assignment for DMA channel 1 (ASGN1); specifies I/O channel select code address (10_8), character byte transfer mode, STC after each byte is transferred, and CLC after final byte is transferred.
CW2	OCT	100200	Memory address register control, DMA channel 1 (MAR1); specifies memory input operation and starting memory address (200_8).
CW3	DEC	-50	Word count register control, DMA channel 1 (WCR1); specifies the 2's complement of the number of character words in the block of data to be transferred (50_{10}).
			DMA CHANNEL 2 CONTROL WORDS:
CW4	OCT	020022	Assignment for DMA channel 2 (ASGN2); specifies I/O channel select code address (22_8), data word transfer mode, and CLC after final word is transferred.
CW5	OCT	010000	Memory address register control, DMA channel 2 (MAR2); specifies memory output operation and starting memory address (10000_8).
CW6	DEC	-4096	Word count register control, DMA channel 2; specifies the 2's complement of the number of words in the block of data to be transferred (4096_{10}).
CW7	OCT	140025	Assignment for disc memory; specifies a write (bit 15 = 1) on track 10_8 (bits 7 thru 13 = 40_8) beginning with sector 25_8 (bits 0 thru 6 = 25_8).

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. This section contains an overall functional description and a detailed circuit description for the DMA option.

4-3. OVERALL FUNCTIONAL DESCRIPTION.

4-4. The following paragraphs provide a functional description of the DMA option. This description is based on the block diagram in figure 4-1 (located at the end of this section) and relates the operation of DMA to the typical program in table 3-1. The operation of DMA channel 1, which is programmed for memory input operations, is described first. This is followed by a description of DMA channel 2, which is programmed for memory output operations. The following descriptions are based on typical applications of the DMA option and may vary slightly when different types of external input/output devices are serviced through DMA. Refer to section III for an explanation of programming terms used in these descriptions.

4-5. The DMA option adds a fifth phase to the four-phase capability of the basic computer. Phase 5 is a special memory cycle that requires one machine timing cycle (T0 through T7). Once initiated by service request signals received from I/O channels programmed to DMA, phase 5 operation is automatic and independent of program control. Each phase 5 cycle permits one input or output word or character byte to be exchanged directly between an external device (tape reader, disc memory, magnetic tape unit, etc.) and computer memory.

4-6. The two high-priority DMA phase 5 control channels are shown functionally by figure 4-1. Both channels are functionally identical and, except for the fact that DMA channel 1 takes priority over channel 2, each operates independently of the other. Three main functions comprise each DMA channel. These are the program control function, the memory control and word count function, and the packing/unpacking function. The program control function is the heart of the DMA channels. It controls all DMA channel switching functions and furnishes the control signals required for phase 5 operation. The memory control and word count function is comprised of registers that give DMA access to the computer memory during phase 5 and provide status and control of data block length. The packing/unpacking function contains registers that permit special processing of 8-bit byte characters.

4-7. After being initialized by instructions and control words in the main program, the DMA channels operate independently of program control. When a service request is received by a DMA channel, it suspends the main program for one machine cycle to achieve data transfer, rather than by interrupting to a service subroutine. While the program is suspended, the computer is in phase 5 and data is transferred to or from the external device. At the end of the phase 5 cycle, the main program, delayed by one machine cycle, continues from the point that it was suspended since the counting registers in the central processor are not stepped during a phase 5 cycle. A DMA interrupt from the program control function occurs only after the word count function signals that all words in a data block have been transferred.

4-8. CHANNEL TIE-IN.

4-9. The DMA channels are tied to the computer I/O addressing scheme through select codes 2, 3, 6, and 7. This is shown functionally by the select code switch in the I/O system in figure 4-1. The select code switch is positioned by the six select code bits (0 through 5) contained in an input/output instruction word format. (See figure 3-1.) The DMA select code assignments permit the DMA channels to be initialized by input/output (I/O group) instructions and control words from the running program in the central processor. As shown by figure 4-1, the channel functions of DMA channel 1 are addressed through select codes 2 and 6 and those of DMA channel 2 are addressed through select codes 3 and 7.

4-10. The DMA channels are also tied directly into the I/O system priority chain through select code addresses 6 and 7. Address 6 has either the second or third highest interrupt priority in the I/O system (depending on computer type and model; refer to volume III) and address 7 has either the third or fourth highest priority. This gives DMA phase 5, and DMA interrupt (FLG and IRQ lines) priority over all I/O channel functions. It follows also that the two DMA channels cannot both operate at the same time since DMA channel 1 takes priority over DMA channel 2. Addresses 2 and 3 are used for addressing purposes only and are not tied into the I/O priority system.

4-11. The DMA channels are tied to the central processor through the I/O bus output (IOBO) lines, I/O bus input (IOBI) lines, T-register (TR) lines, direct memory address (DM) lines, the input/output (I/O group) instruction control lines, and the phase 5 control lines. Initializing control words from memory are routed to the R-bus via the A- or B-registers and are switched to the IOBO bus by the input/output switching function in the central processor. This switch is positioned to out when OTA or OTB instructions are in progress. The control bits on the IOBO lines are then routed to the addressed DMA channel function by the select code switching function in the I/O system. Note that the IOBO lines are also used to output data words to the I/O channels when DMA is not in operation.

4-12. I/O group instruction signals (CLF, STF, etc.) are also routed to the DMA channels and I/O channels through the input/output switching and select code switching functions. When these input/output instructions are processed by the computer, the input/output switch assumes the IOG position. (The I/O group instruction lines are shown merged with the IOBO lines to simplify the presentation of figure 4-1).

4-13. During phase 5 output cycles, the input/output switching and select code switching functions are controlled by the phase 5 control signals and assume the off position. Data words from memory are then routed to the DMA channel directly from the T-register via the TR lines. The data bits on the TR lines are switched to IOBO lines by the service select switching function within the DMA channel and routed to the external device through the interface card located in the I/O channel. The TR lines are routed through the packing/unpacking function when character input/output words (see figure 3-1) from memory are processed. For each character word received from memory, the unpacking function outputs two separate 8-bit character bytes to the external device. Unpacking requires two phase 5 cycles. The first phase 5 cycle reads the character output word from memory, stores the low character bits in the unpacking function register, and outputs the high character bits to the external device. The second phase 5 cycle outputs the low character bits to the external device.

4-14. During phase 5 input cycles, the input/output switching and select code switching functions are also controlled by the phase 5 control signals. The input/output switch is positioned to in and the select code switch is positioned to off. The IOBI lines from the I/O channel are now under control of the service select switch in the DMA channel. The data bits on the IOBI lines are routed either directly to memory via the S-bus, T-bus, and T-register (which are now under phase 5 control) or, in the case of character byte inputs, first through the packing/unpacking function and then read into memory. Packing of input character bytes also requires two phase 5 cycles. The first phase 5 cycle transfers the high character bits into the packing function register where they are stored. The second phase 5 cycle inputs the low character bits and packs them, together with the high character bits, into the character word format and transfers the character input word directly into memory.

4-15. The phase 5 control signals take complete control of the central processor and I/O system during phase 5 input and output cycles. They effectively turn-off the I/O system during phase 5 to prevent the I/O channels from interrupting a DMA phase 5 data transfer. They also control the operating mode of the central processor so that direct data paths (denoted by the heavy lines on figure 4-1) are established between the I/O channels and computer memory. In addition, the phase 5 control signals are gated with the DM lines (for 2115, 2116A, and 2116B computers) from the memory control function register so that during phase 5 the DM lines control memory access in place of the M-register (MR) lines. The phase 5 control signals are referred to as "pseudo" signals because they have the same mnemonic labels and share the same lines in the backplane wiring as similar signals generated in the central processor or the I/O system. Pseudo signals perform essentially the same functions as their counterparts, but originate in the DMA option.

4-15A. For 2116C computer operation, the DM line mnemonics are changed to M and these lines are routed directly to computer memory without being gated with the phase 5 control signals. The phase 5 control signals are used instead to inhibit the M-register (MR) lines during phase 5.

4-16. DMA CHANNEL 1 INITIALIZATION.

4-17. As the first step of the initializing process for DMA channel 1, a DMA program control word, labeled CW1, is fetched from memory and transferred to the A-register by a LDA instruction in the running program. The next instruction, an OTA instruction addressed to select code 6, causes the input/output switching function in the central processor to assume the out position and the select code switching function in the I/O system to assume position 6. This, in turn, causes the CW1 control bits to be transferred from the A-register onto the R-bus, switched from the R-bus to the IOBO bus, and routed to the program control function of DMA channel 1. The CW1 control bits are stored in registers in this function to control the service select, transfer mode, clear control decision, and set control decision switching functions within DMA channel 1. As presented in table 3-1 and figure 4-1, the contents of CW1 switch the set control decision switch to on, the transfer mode switch to pack/unpack, the clear control decision switch to on, and the service select switch to position 10.

4-18. The second step of initialization consists of loading the register associated with the memory control function with the starting address where the first data or character input word is to be stored by DMA. To accomplish this, it is first necessary to clear control on address 2 by addressing a CLC instruction to select code 2. This CLC2 instruction causes the input/output switching function to assume the IOG position, and the select code switching function to assume position 2. A CLC signal is then routed to control FF2, located in the memory control and word count function of DMA channel 1, via the I/O group instruction lines. A LDA instruction then fetches a DMA address word, labeled CW2, from memory and loads it into the A-register. The OTA2 instruction which follows puts the CW2 bits on the IOBO lines and they are routed to the memory control function register where they are stored. The contents of this register are put onto the DM lines and routed to computer memory on command of signals from the program control function during phase 5 cycles that a memory read or write operation takes place.

4-19. The direction bit included in CW2 is stored in a separate register stage within the memory address function. The presence or absence of this bit signals the program control function whether the data transfer is a memory input operation or a memory output operation, respectively. In the case of DMA channel 1, it is assumed that the

channel is programmed for the memory input mode. Therefore, the program control function senses the presence of a direction bit in the register and sets the direction switching function to the in position. The presence or absence of the direction bit, and also the byte/word bit of CW1, has a controlling effect on the generation of register stepping signals, character control signals, and other signals generated within the program control function.

4-20. The third step of initialization consists of loading the register associated with the word count function with a cardinal number that represents the number of words (1 to 16384) in the block of data to be transferred. This number is contained in the DMA block length word labeled CW3 and is expressed as a negative binary integer (two's complement of the positive decimal equivalent). To load the word count function register, it is first necessary to set control on address 2 by addressing a STC instruction to select code address 2. The STC2 instruction, like the CLC instruction, is routed through the IOG position on the input/output switch, through position 2 of the select code switch, and over the I/O group instruction lines to control FF2 located in the memory control and word count function of DMA channel 1. The STC instruction sets control FF2, making it possible to address the word count function register with the bits of CW3. Again, this is accomplished with a LDA instruction that fetches CW3 from memory and loads it into the A-register, followed by an OTA2 instruction that puts the CW3 bits on the IOBO lines for routing to the word count function register where the bits are stored. The word count function register also operates as a down-counter. Just before a word is transferred to or from memory, the count held by this register is increased (less negative) by one. When the count held by the register is zero (word count rollover), a word count status signal transmits this condition to the program control function. As a result of this, the program control function generates flag and interrupt signals that are routed to the I/O address and control function and, depending on the position of the clear control decision switch, generates a CLC signal that clears control on the I/O channel and turns off the external device.

4-21. The final step of the initializing process consists of turning on the external device, and turning on the DMA channel. This is accomplished by programming one STC instruction to the interface card in the I/O channel through which the external device is serviced, and programming a second STC instruction to the program control function of DMA channel 1. Bit 9 of both STC instruction words is a "1" which causes the central processor to also generate a CLF signal when the STC instructions are processed. The first STC instruction is addressed to select code 10. As is the case for all STC instructions, the input/output switch assumes the IOG position. The select code switch is set to position 10 by the select code bits in the instruction word. The STC and CLF signals are then routed via the IOG instruction lines to I/O channnel 10 to set control and clear the flag on the interface card located in I/O channel 10, which causes the external device to turn-on. The second STC instruction is addressed to select code 6. The STC and CLF signals generated by this instruction are routed to the program control function of DMA channel 1 through position 6 of the select code switch. These signals set control and clear the flag of DMA channel 1. This sets the channel 1 control switching function to the on position and the channel 1 interrupt switching function to the on position, and DMA channel 1 is now turned on. With the channel 1 control switch set to the on position, I/O channel 10 is effectively connected between computer memory and the external device through the DMA switching functions. The initialization of DMA channel 1 is now complete. This channel remains static and the main program continues to run until a service request signal is received from the interface card located in I/O channel 10.

4-22. DMA CHANNEL 1 MEMORY INPUT OPERATION.

4-23. When the external device inputs a character byte to the computer, the flag sets on the interface card located in I/O channel 10. The interface card then generates a service request signal that is routed to the program control function of DMA channel 1. The receipt of a service request signal sets a phase 5 operation at the end of the current machine phase. Therefore, at the beginning of the next complete machine cycle, and through the remainder of this cycle (T0 through T7), phase 5 is set by the program control function. During this timing period, a sequence of phase 5 control signals are generated and routed to the central processor and the I/O system (which includes I/O channel 10).

4-24. While phase 5 is set, the central processor and the I/O system are under exclusive control of DMA channel 1. Because byte packing requires two phase 5 cycles (in order to input both the high and low character bytes, pack them into the character word format, and write the character word in computer memory), a memory write cycle will occur only during the even (second, fourth, sixth, etc.) phase 5 cycles that occur for a given character word data block input operation. During the even phase 5 cycles, the low character bytes are processed through I/O channel 10. Therefore, during the course of the first, third, fifth, and all succeeding odd phase 5 cycles (when the high character bytes are processed through I/O channel 10), the phase 5 control signals do the following:

a. Inhibit the M-register bits on the MR lines by inhibiting the operation of all registers in the central processor.

b. Disable the R-, S-, and T-buses in the central processor.

c. Set the input/output switching function to the off position.

d. Set the I/O system select code switching function to the off position.

e. Inhibit the I/O address and control function.

f. Control the operation of the interface card located in I/O channel 10.

g. Inhibit DMA channel 2 through the I/O priority system.

4-25. Due to the conditions described above, the main program in the central processor is suspended and the I/O interrupt system is disabled. The first character byte received from the external device is now stored in the I/O channel 10 interface card register. This byte is designated as the high character because it will occupy high order bits 7 through 15 in the character word format that is written in memory. The phase 5 control signals transfer the high character bits from the interface card register to IOBI lines 0 through 7. These IOBI lines are routed to the packing function via the DMA channel 1 switching functions which were set to the positions shown during the initializing process (see figure 4-1). The high character bits are then strobed into the packing function register by character packing control signals where they are stored until the low character bits are processed through I/O channel 10 during the next phase 5 cycle. Next, STC and CLF signals are generated by the program control function and routed to I/O channel 10 where they set control and clear the flag on the interface card. This prepares the interface card register to accept the next character byte from the external device and removes the service request input from the program control function. At the end of the current machine cycle, the phase 5 cycle ends. The conditions described above are no longer true and control is returned to the central processor and I/O system. During the succeeding machine cycles (the exact number of which is determined by the relative speed of the external device), main program processing resumes from the point where it was suspended until another service request signal is received from I/O channel 10.

4-26. DMA channel 1 remains static while the main program is in progress. The next service request signal received from I/O channel 10 indicates that the low character byte is ready to be processed. Since a character word containing both the high and low bytes will be written in memory during the upcoming phase 5 cycle, the program control function generates a stepping signal (at the end of the current machine cycle in which the service request signal is received) to increment the word count register by one. At the beginning of the next machine cycle, phase 5 is set once again in the same manner described by paragraph 4-23. During the second, fourth, sixth, and all succeeding even phase 5 cycles, the phase 5 control signals do the following:

a. Inhibit the M-register bits on the MR lines and all other registers in the central processor except the T-register.

b. Strobe the memory address bits stored in the memory control function register onto the DM lines (M lines on 2116C).

c. Enable the DM line input gates to give DMA channel 1 control of memory access. (For 2116C computers, the MR line input gates are inhibited to give DMA channel 1 control of memory access.)

d. Set the input/output switching function to the in position.

e. Connect the S-bus to the T-bus by enabling the add function within the central processor.

f. Enable the T-bus input to the T-register.

g. Enable the T-register output to memory.

h. Set the I/O system select code switching function to the off position.

i. Inhibit the I/O address and control function.

j. Control the operation of the interface card located in I/O channel 10.

k. Inhibit DMA channel 2 through the I/O priority system.

4-27. Due to the conditions described above, the main program in the central processor is once again suspended and the I/O interrupt system disabled. The second character byte received from the external device is now stored in the I/O channel 10 interface card register. This byte is designated as a low character because it will occupy low order bits 0 through 7 in the character word format that is written in memory. The phase 5 control signals transfer the low character from the interface card register to IOBI lines 0 through 7. At the same time, the high character bits are strobed from the packing function register onto IOBI lines 8 through 15 by the character control signals. Thus the bits on the IOBI lines comprise the character word which is written into memory via the data path described by the conditions in paragraph 4-26. Next, as during the preceding phase 5 cycle, the STC and CLF signals are generated by the program control function and routed to I/O channel 10 where they set control and clear the flag on the interface card. This prepares the interface card register to accept the next (high character) byte from the external device and removes the service request input from the program control function. At the end of the current machine cycle, the phase 5 cycle ends. At the conclusion of this cycle, the program control function generates a register stepping signal that increments the memory control register count by one. Thus, the next character word transfer from DMA channel 1 will be written into the next higher memory address, and the word counter incremented prior to this phase 5 cycle, indicates that the second character word in the data block is in the process of being packed and transferred. When the current phase 5 cycle ends, the conditions described by paragraph 4-26 are no longer true and control is returned once again to the central processor and I/O control system.

4-28. DMA CHANNEL 1 INTERRUPT.

4-29. The action described by paragraphs 4-22 through 4-27 is repeated for each character word in the data block currently assigned to DMA channel 1. When the service request signal for the final word in the data block is received from I/O channel 10, the word count function

register is incremented as before, and now holds a count of zero. This condition is transmitted to the program control function by the word status signal to indicate that the last character word in the data block will be transferred during the current (final) phase 5 cycle. However, the presence of the word status signal during the final phase 5 cycle does the following:

a. Inhibits the generation of the STC and CLF signals that were generated by the program control function during previous phase 5 cycles.

b. Enables the generation of the CLC signal by the program control function.

c. Effectively inhibits processing of all future service requests from I/O channel 10, unless reinitialized to do so.

d. Returns control of I/O channel 10 data inputs to the I/O system interrupt function.

e. Enables the generation of DMA channel 1 flag and interrupt request signals.

4-30. When the final phase 5 cycle is set, the last byte from I/O channel 10 is processed through DMA channel 1 and the final character word is transferred to memory in the same manner as previously described. However, the STC and CLF signals from the program control function are now inhibited by the word status signal, and the CLC signal is enabled. The CLC signal clears control on the I/O channel interface card and the external device is turned off. The presence of the word status signal during this phase 5 cycle also causes the channel 1 control switching function to return to the off position after the character word has been transferred to memory and the CLC signal has been generated. I/O channel 10 is now under control of the I/O system interrupt function. The flag and interrupt signals, which are enabled by the presence of the word status signal, are sent to the I/O address and control function. One or more machine cycles after the final phase 5 cycle ends, phase 4 is set. One or more machine cycles are required to set phase 4 because the I/O system interrupt function is intentionally inhibited by DMA channel 1 for one machine cycle after phase 5 in order to permit at least one main program instruction to be executed before an interrupt occurs. During phase 4, the flag and interrupt request signals from DMA channel 1 are decoded by the I/O address and control function and the resulting service request address 6 is read into the M-register via the T-bus. At the end of phase 4, an interrupt acknowledge (not shown by figure 4-1) is routed to the program control function, causing the channel 1 interrupt switch to assume the off position. After phase 4 ends, phase 1 is set and the central processor executes the service subroutine programmed for service request address 6. DMA channel 1 is now turned off and must be re-initialized before being placed in operation again.

4-31. DMA DIRECT WORD INPUT.

4-32. If it had been assumed during the preceding description that DMA channel 1 had been initialized for direct word inputs (DMA program control word bit 14 = 0), then the transfer mode switching function would have been programmed to the direct position, rather than to the pack/unpack position. Then the packing/unpacking function would have been by-passed and the character bytes from I/O channel 10 would have been written into memory during each phase 5 cycle, as they were received, rather than during alternate (even) phase 5 cycles, as is the case when the packing function is employed. When the packing function is not used, the character control signals from the program control function are inhibited. Also, the memory control and word count function registers are stepped during each phase 5 cycle rather than only during even phase 5 cycles. For this reason, it would have also been necessary to initialize the word count function register to a count of -100, rather than a count of -50 as shown by table 3-2. Other than the differences noted herein, the operation of DMA channel 1 is the same for a direct input transfer operation as for a packing input transfer operation.

4-33. DMA CHANNEL 2 INITIALIZATION.

4-34. Figure 4-1 shows DMA channel 2 programmed for a memory output operation to a device serviced through I/O channels 22 and 23. In many respects the operation of the DMA channels is the same whether programmed for an input or an output operation. Signal and switching functions described in paragraphs 4-5 through 4-32 that are common to both operations are not covered in detail in the following presentation. Only significant differences are described.

4-35. The DMA program control word, labeled CW4, is read from memory and routed to the program control function of DMA channel 2 by a LDA instruction, followed by an OTA instruction addressed to select code 7. Once stored in the program control function registers, the CW4 control bits set the clear control switch to on, the transfer mode switch to direct, and the service select switch to position 22. Position 22 corresponds to the I/O address of the data channel for the external device. Because the STC bit is assumed to be "0", the set control decision switch remains in the off position.

4-36. After first clearing control on address 3 with a CLC instruction, the DMA address word, labeled CW5, is programmed to the memory control function register by a LDA instruction, followed by an OTA instruction addressed to select code 3. The bits of CW5 provide the starting address from which the first output word in the data block will be read when phase 5 is set for the first time. The direction bit of CW5 is assumed to be "0", which causes the direction switch to be set to the out position.

4-37. Next, control on address 3 is set by an STC instruction. The DMA block length word, labeled CW6, is then programmed to the word count function register by a LDA instruction, followed by an OTA instruction addressed to select code 3. The bits of CW6 represent the number of words in the data block to be transferred from memory to the external device.

4-38. The external device serviced by DMA channel 2 must also be initialized prior to data transfer. This is accomplished under program control by a control word, labeled CW7, that is stored in memory. The device control word is read from memory by a LDA instruction and stored in the A-register as were previous control words. The associated OTA instruction, however, is addressed to select code 23, the I/O address of the control channel for the external device. Therefore, from the A-register, the bits of CW7 are routed through position 23 of the select code switching function and to I/O channel 23 via the IOBO lines. Refer to table 3-2 for a description of CW7.

4-39. The final step of the initializing process for DMA channel 2 consists of turning on the DMA channel, and then turning on the external device, in that order. Note that in the case of DMA channel 1 the external device was turned on first (paragraph 4-21). The turn-on sequence is determined by the relative speed with which the external device is able to accept data from, or provide data to, the DMA channel. In the case of DMA channel 2, the DMA channel is turned on first by programming an STC instruction (bit 9 = 1) to select code 7. The resulting STC and CLF signals set control and clear the flag of DMA channel 2. This sets the channel 2 control switching function to the on position, and the channel 2 interrupt switching function to the on position, and DMA channel 2 is now turned on. A second STC instruction (bit 9 = 0) is programmed to select code 22 to turn on the external device. The initialization process is now complete. DMA channel 2 remains static and the main program continues to run until the flag is set on the interface card in I/O channel 22 causing a service request to be sent to the program control function.

4-40. DMA CHANNEL 2 MEMORY OUTPUT OPERATION.

4-41. When the external device is ready to accept a data word from the computer, it sets the flag on the interface card in I/O channel 22. The interface card then generates a service request signal that is routed to the program control function of DMA channel 2. The receipt of the service request signal sets a phase 5 cycle request condition which prepares DMA channel 2 to go into phase 5 operation at the end of the current machine phase. Just before phase 5 is set, a stepping signal generated by the program control function is applied to the word count function register to increment it by one. At the beginning of the next complete machine cycle (provided DMA channel 1 is not in operation) and through the remainder of this cycle (T0 through T7), phase 5 is set by the program control function. During this timing period, a sequence of phase 5 control signals are generated and routed to the central processor, the I/O system, and I/O channel 22.

4-42. While phase 5 is set, the central processor and the I/O system are under exclusive control of DMA channel 2. Because a direct word transfer requires only one phase 5 cycle (unlike packing and unpacking which require two), and because a memory output operation is in progress, a memory read cycle will occur during every phase 5 cycle generated by the program control function. During each cycle, the phase 5 control signals do the following:

a. Inhibit the M-register bits on the MR lines and all other registers in the central processor except the T-register.

b. Strobe the memory address bits stored in the memory control function register onto the DM lines (M lines on 2116C).

c. Enable the DM line input gates to give DMA channel 2 control of memory access. (For 2116C computers, the MR line input gates are inhibited to give DMA channel 2 control of memory access.)

d. Set the I/O system select code switching function to the off position.

e. Disable the R-, S-, and T-buses in the central processor.

f. Enable the output from memory to the T-register.

g. Enable the T-register output (TR lines) to the switching functions within DMA channel 2.

h. Set the input/output switching function to the off position.

i. Inhibit the I/O address and control function.

j. Control the operation of the interface card in I/O channel 22.

4-43. Under the conditions described above, the main program in the central processor is suspended, and the I/O interrupt system is disabled. The first word in the data block is read from memory, temporarily stored in the T-register, and then routed via the TR lines to the switching functions in DMA channel 2. Because DMA channel 2 has been programmed for a direct output operation, the packing/unpacking function is bypassed, and the bits on the TR lines are switched directly to the IOBO line input to the interface card in I/O channel 22 by the service select switching function. At the same time, the phase 5 control signals enable the register on the interface card. The data word is temporarily stored by I/O channel 22 until accepted by the external device, at which time the I/O channel flag is cleared. At the end of the current machine cycle, the phase 5 cycle ends. At the conclusion of the cycle, the program control function generates a register stepping signal that increments the memory control register count by one. The next data word will, therefore, be read from the next higher memory address when phase 5 is set again. The word counter, which was stepped prior to the current phase 5 cycle, now indicates that the second character word in the data block will be transferred. When the current phase 5 cycle ends, the conditions listed in paragraph 4-42 are no longer true, and control is returned to the central processor and the I/O control system. During the machine cycles which follow (the exact number of which is

determined by the relative speed of the external device), main program processing resumes from the point where it was suspended until another service request signal is received from I/O channel 22.

4-44. DMA CHANNEL 2 INTERRUPT.

4-45. The external device signals when it is ready to accept another word from the computer by once again setting the flag on I/O channel 22. The action described by paragraph 4-40 is then repeated each time a word in the data block currently assigned to DMA channel 2 is transferred to the external device. When the service request signal for the final word in the data block is received from I/O channel 22, the word count function register is incremented to a count of zero. This condition is transmitted to the program control function by the word status signal to indicate that the last word in the data block will be transferred during the current (final) phase 5 cycle. The presence of the word status signal during the final phase 5 cycle does the following:

a. Enables the generation of CLC signal by the program control function.

b. Effectively inhibits processing all future service requests from I/O channel 22.

c. Returns control of I/O channel 22 data inputs to the I/O system interrupt function.

d. Enables the generation of DMA channel 2 flag and interrupt request signals.

4-46. When the final phase 5 cycle is set, the last word in the data block is read from memory and routed to the I/O channel register in the same manner as previously described. After the word is transferred from the I/O channel register to the device, the CLC signal generated by the program control function clears control on I/O channel 22 and turns off the external device. The presence of the word status signal then causes the channel 2 control switching function to return to the off position. Flag and interrupt signals generated within the program control function are then routed to the I/O address and control function of the I/O system. From this point, the interrupt for service request 7 is the same as for service request 6, described in paragraph 4-30.

4-47. DMA CHARACTER BYTE OUTPUTS.

4-48. If it had been assumed during the preceding description that DMA channel 2 has been initialized for byte outputs to an external device employing 8-bit characters, then bit 14 of the DMA program control word (CW5) would have been a 1 instead of a 0, and the transfer mode switch would have been programmed to the pack/unpack position, rather than the direct position. Also, the character control signals would be enabled during each phase 5 cycle. Further, it would be assumed that the output words in the assigned data block are in the character word format shown in figure 3-1. When the stated assumptions are true, the packing and unpacking function is switched into operation during the memory output operation to separate each character word read from memory into two individual 8-bit byte outputs.

4-49. In the unpacking mode, a memory read cycle occurs only during odd (first, third, fifth, etc.) phase 5 cycles generated in the course of transferring a given data block. During even (second, fourth, sixth, etc.) phase 5 cycles, the memory read cycle is inhibited. Odd cycles read the character word from memory, store the low character in the unpacking function register, and output the high character to the external device; even cycles clear the low character from the unpacking function register and output it to the external device. Because two phase 5 cycles are required to output both bytes packed in the character word, the unpacking mode requires twice as many phase 5 cycles as the direct mode to output the same number of words from memory.

4-50. When the external device is ready to accept the first character byte from the computer, it sets the flag on the interface card in the I/O channel through which it is serviced. When the service request signal is sent to the DMA channel, a phase 5 cycle request condition is set within the program control function; and the computer, under control of the phase 5 control signals, goes into phase 5 operation at the beginning of the next machine cycle. During this first (odd) cycle, the phase 5 control signals perform the same functions described in paragraph 4-42, with the exception that the TR lines are now routed to the packing and unpacking function, rather than through the direct position of the transfer mode switch. When the character word is read from memory, the high character bits (so designated because they occupy high order bit positions 8 through 15 in the character word format) are routed to the unpacking function on TR lines 8 through 15. These bits are switched to IOBO lines 8 through 15 and transferred directly to the external device through the pack/unpack position of the transfer mode switch, the out position of the direction switch, position 22 of the service select switch, and the I/O channel register. The low character bits (which occupy low order bits positions 0 through 7 in the character word format) are routed to the unpacking function on TR lines 0 through 7 where they are stored until the next service request is received from the I/O channel. At the end of the current phase 5 cycle, a register stepping signal is generated to increment the memory control register count by one. (The word count function register is not incremented during this cycle.)

4-51. When the external device is ready to accept the second character byte from the computer, it sets the flag on the I/O channel once again. As before, the service request signal sets the phase 5 cycle request condition within the program control function, and the computer goes into phase 5 operation at the beginning of the next machine cycle. During this second (even) cycle, the word count function register is incremented by one, but the memory control function register is not incremented. Because the memory read cycle is inhibited during even cycles, no data is read onto the TR line. However, the low character bits,

which were stored in the unpacking function register during the previous phase 5 cycle, are now read onto IOBO lines 0 through 7 and routed to the external device.

4-52. The character output operations described in paragraphs 4-50 and 4-51 continue alternately, during odd and even phase 5 cycles, until all character words in the data block have been transferred to the external device. During the last even phase 5 cycle, when the final low character byte is transferred, the word count register holds a count of zero. The presence of the word status signal causes the generation of the CLC signal by the program control function and initiates an interrupt from DMA channel 2, under conditions similar to those described by paragraph 4-45.

4-53. DETAILED DESCRIPTION.

4-54. The following paragraphs provide a detailed theory of operation for the DMA option. Logic diagrams are provided at the end of section V for the direct memory logic card (figure 5-1 or 5-2), the DMA character packer card (figure 5-3), the DMA control card (figure 5-4), the DMA address encoder card (figure 5-5), and the DMA register card (figure 5-6). Reference should be made to the logic diagrams whenever the cards are referenced in text. In the following description, only channel 1 of the DMA option is covered since channels 1 and 2 function identically. The parallel operation of the two channels may be seen from the layout of the logic diagrams. All information in the detailed description may be applied to both channels. Also provided at the end of section V are timing diagrams for DMA initialization (figure 5-7), DMA memory input operations (figure 5-8), DMA memory output operations (figure 5-9), and DMA interrupt (figure 5-10). These timing diagrams show the timing relationship between the various DMA signals.

4-55. INITIALIZATION.

4-56. When power is applied to the computer, the power on pulse to I/O (POPIO) signal is applied to the DMA control card. The control reset to I/O (CRS) signal is applied to the DMA control card, the DMA address encoder card, and the DMA register card. The POPIO signal sets the flag 6 buffer flip-flop. The CRS signal clears control FF 6 and transfer enable FF 1 on the DMA control card. At the address encoder card, the CRS signal clears cycle request 1 FF (CR1 FF). The CRS signal also clears the control FF on the DMA register card. The DMA channels must be re-initialized whenever power is turned off and on.

4-57. The first step in initializing DMA after power turn-on is to route the first control word to the DMA address encoder card and the DMA control card. Assuming channel 1 is being used, the lower six bits of this first control word are clocked into service select register FF's SS10 through SS15 by input/output group buffered (IOGB), select code most significant octal digit 0 (SCM0), select code least significant octal digit 6 (SCL6), and I/O output (IOO signals). The service select decoder then decodes these six bits to determine the I/O channel select code address of the device involved in the data transfer. Gates MC31A through MC61B decode SCM and SCL signals for the selected device. Gates MC22A through MC112A decode the SCL signals (for either DMA channel) of the selected device and gates MC54B, MC76A, MC74B, and MC76B decode SCM signals (for either DMA channel).

4-58. The decoded select code enables the service request (SRQ) network (MC33C through MC74A) on the DMA address encoder card. When the selected device sends a service request signal and no higher priority device has interrupted, the CR1 FF can set at T6.

4-59. Bit 14 of the first control word specifies byte packing or unpacking. If bit 14 is a true signal, the character mode 1 FF on the DMA address encoder card is set when IOGB, SCM0, SCL6, and IOO signals cause the clock input on the flip-flop to go true. The set output of the character mode 1 FF enables "and" gates MC16A, MC36A, MC46A, and MC36B to provide input high character to channel 1 (IHC1), output high character to channel 1 (OHC1), output low character to channel 1 (OLC1), and input data word to channel 1 (IDW1) signals. These signals implement character packing and unpacking on the DMA character packer card. The character mode 1 FF also provides an enable signal (CM1) for register stepping.

4-60. On the DMA control card, SCM0, IOGB, and SCL 6 enable "and" gates MC55A and MC57A. The outputs of these gates are used to set the set control decision 1 (STCD1) FF or clear control decision 1 (CLCD1) FF, depending on the state of bits 13 and 15 of the first control word. These decisions will enable transfer signals and send set or clear control signals to the selected I/O device. These signals are optional and the state of the signals depends on the device used with DMA.

4-61. The next step in the initialization process is to load the memory address register with the starting address of the input or output data block and to prepare DMA for either an input or an output operation. The second control word is used to provide this information. On the DMA register card, a CLC signal at select code 2 (SC2) resets the control FF and prepares the memory address register FF's (DM0 through DM14) for loading. The memory address is then loaded into the computer A-register and out onto the I/O bus output (IOBO) lines. All true IOBO bits (0 through 14) are then used to direct set the memory register FF's thus loading the starting address into the memory register. During phase 5 for 2115, 2116A and 2116B computers, the signals from the memory register are gated into memory through the DML card on DM lines 0 through 14. During phase 5 for 2116C computers, the signals from the DMA memory register are routed directly into computer memory on M lines 0 through 14. After each memory transfer, the step memory address register 1 (SMAR1) signal will increment the memory address register by one count until the complete data block is transferred. If bit 15 of the second control word is true, the direction FF is set and a DMA input 1 (DIN1) signal is provided, indicating that the data transfer is to be from an external device to computer memory. If bit 15 is false, the direction FF does not set and a memory output operation is indicated.

4-62. The third step in initializing DMA consists of loading the word count register on the DMA register card with the two's complement of the number of words in the block of data to be transferred. The word count register is enabled by a STC instruction at select code 2. The third control word contains the data block length and is output from the A-register on IOBO lines 0 through 13 into the word count register FF's (WC0 through WC13). Before each word transfer, the word count register is stepped one count by the step word count register 1 (SWCR1) signal. When the counter reaches zero, the overflow (OVFL) FF is set to generate a word count rollover 1 (WCR1) signal. This signal enables flag and interrupt signals to signal DMA that channel operation is complete.

4-63. The final initialization step consists of turning on DMA and the external device. The external device is turned on by a STC,CLF instruction programmed to the device select code. The DMA option is turned on by a STC,CLF instruction to select code 6 for channel 1 or to select code 7 for channel 2. For channel 1, SC6 and STC signals set control FF 6 on the DMA control card to enable DMA interrupt and to set transfer enable FF 1. On the DMA address encoder card, a service request signal can now set cycle request FF 1. The STC6 signal also clears cycle divide 1 FF, initializing the flip-flop to control the register stepping signals.

4-64. DMA INPUT OPERATION.

4-65. DMA may use direct input to the computer memory or byte mode may be selected for eight-bit devices to utilize character packing and conserve memory space. The following description of a DMA input operation points out significant differences between byte operation and direct operation.

4-66. SRQ SIGNALS. Anytime after initialization, the selected device may be ready to transfer information to the computer. At this time, the device flag is set on the interface card and an SRQ signal is generated. At the DMA address encoder card, the SRQ signal is applied to a "nand" gate along with the output of the service select register. The output of the "nand" gate is then applied to either MC14 or MC114, depending on which device originated the SRQ signal. If the priority low (PRL) signal from memory protect and the TE1 signal from transfer enable FF 1 are true, at T6 the SRQ signal sets the CR1 FF. Also, the false output of MC97B disables DMA channel 2.

4-67. PHASE 5. The CR1 FF sends a true CR1 signal to enable character in/out gates MC37D through MC47C and the cycle divide 1 FF. These circuits control the register stepping signals. In the byte mode, the word count register must step only after the second character is available for transfer. The CR1 signal also is applied to the DMA control card where it sets the phase 5 (PH5) FF at T7S of the current machine cycle. The DMA channel then goes into phase 5 operation for the next T0 through T7.

4-68. CENTRAL PROCESSOR UNIT CONTROL SUSPENSION. When the PH5 FF is set, the central processor unit (CPU) and the I/O system are under DMA control, exclusively. Since byte packing requires two phase 5 operations, a memory write cycle occurs on even phase 5 operations, only, for byte mode. On even phase 5 cycles, the lower eight bits are processed; on odd phase 5 cycles, the higher order bits are processed and the phase 5 control signals cause the following:

a. The PH5 signal disables the M-register lines on the DML card through inverter MC75 and enables the DM lines from the memory address register. This provides the memory address register with access to the CPU memory to control the location of the first word transferred.

b. The PH5 signal generates a false enable phase (EPH) signal at the DML card to block phase decoding at the computer timing generator card until phase 5 is complete.

c. The PH5 signal generates a true P123 signal at the DML card to enable memory read and write timing signals and generate a true reset T-register (RST) signal at the computer timing generator card.

d. The PH5 signal generates a false P123G signal at the DML card which disables a gate on the computer shift logic card and prevents possible decoding of the data on the T-bus as an addressable register command by the addressable register and the respective decode network.

e. The PH5 signal prevents the I/O address card from generating an interrupt by clearing the interrupt control FF on the I/O control card to give a false enable service request (ESR) signal. The PH5 signal also disables any I/O select code decoding. During phase 5, the hold interrupt system (HIS) signal from the address encoder card disables all interrupts from I/O devices.

f. The PH5 signal generates a true inhibit instruction register (IIR) signal at the DML card which prevents instructions from being decoded during phase 5 by generating an IIR signal at the computer timing generator card.

g. On the DMA address encoder card, the PH5 signal and the CR1 FF output are "anded" in MC126A and the combined output is used to enable the output of the service select register to generate SCM and SCL signals to the selected device.

4-69. CHARACTER PACKING. If byte mode is being used, the first byte of information will now be in the buffer register of the interface card of the selected I/O device. On the DMA control card, the necessary pseudo control signals are being generated to transfer data into the character packer card and prepare the CPU to accept the data. At T2, the enable flag (ENF) signal at pin 37 of the DMA control card is true to enable flag signals and to enable PH5 and CR1 signals to generate the following DMA control signals: I/O input (IOI), I/O control input (IOCI), inhibit strobe generator (ISG), add function (ADF), and switch store in T-bus (SWST).

4-70. The IOI and IOCI signals gate data out of the

interface card buffer register onto the I/O bus input (IOBI) lines and enable the data on the IOBI lines to get on the S-bus in the CPU. The ISG signal causes a false memory strobe time (MST) signal at the computer timing generator, disabling the reading of core during an input operation. The ADF signal is required to transfer data from the S-bus onto the T-bus. The SWST signal enables the store T-bus in T-register (STBT) signal in the CPU to transfer data into memory. The next step is to store the first character (high-order eight bits) into the input holding register on the DMA character packer card. With data on the IOBI lines to the DMA character packer card, a true IHCl signal is generated at MC17D on the DMA address encoder card. The IHC1 signal gates the first character into the input holding register. The IHC1 signal is brought up as a result of the following signals:

a. Cycle divide 1 FF is reset until CR1 FF is cleared at T6.

b. CR1 FF is set until T6.

c. IOI is true.

d. Character mode 1 FF is set (byte mode operation).

4-71. SET CONTROL AND CLEAR FLAG SIGNALS TO I/O DEVICE. With the WCR1 signal false, the STCD1 FF set, and CR1 true, at time T3T4 a set control (STC) signal is output at pin 58 of the DMA control card to prepare the interface card to receive another character. With WCR1 false and CR1 true, at T4T5 a clear flag (CLF) signal is sent from the DMA control card to clear the flag on the interface card of the selected device. When this flag is cleared, the SRQ signal from the device to the DMA address encoder card is removed. A false SRQ input causes the CR1 FF to be cleared at T6 of the current machine cycle. Clearing the CR1 FF allows cycle divide 1 FF to be set and the phase 5 FF to be reset at T7S of the current cycle. Resetting the phase 5 FF causes all phase 5 pseudo functions to go false and returns control of the CPU and I/O system to the main program.

4-72. The DMA channel remains static while the main program is in progress and until the flag of the selected device is set, indicating that data is again ready to be transferred. At that time another SRQ signal brings up the second phase 5 cycle. Again, the phase 5 FF generates the pseudo control signals that give DMA control of the CPU and I/O system. In the byte mode, this second phase 5 cycle is used to transfer the higher order bits onto the IOBI lines out of the input holding register on the DMA character packer card. This is done when an IDW1 signal is brought up from the DMA address encoder card by true CR1, cycle divide 1, IOI, and CM1 signals. At the same time, the lower order bits are gated onto the IOBI lines directly from the device interface card.

4-73. REGISTER STEPPING. The set cycle divide 1 FF and CR1 FF on the DMA address encoder card provide a character in (CIN) signal to the DMA control card which generates register stepping signals. The M-register in the CPU is inhibited by the PH5 signal. On the DMA control card, CIN, CR1, PH5, and DIN1 signals are combined to generate the step memory address register 1 (SMAR1) signal. The SMAR1 signal is used to gate the address bits from the DMA register card onto the DM lines (leading edge of signal) and to step the register by one (trailing edge of SMAR1). The IOBI lines, gated onto the S-bus by the IOCI signal, are gated through the adder and onto the T-bus by the ADF signal. The SWST signal then stores the T-bus bits in the T-register. The T-register bits are enabled into memory by DMA pseudo signal P123, which enables the generation of memory timing signals on the CPU timing generator card. The 16-bit word is strobed into the address specified by the memory address register. The STC and CLF signals are generated to prepare the device to receive another word.

4-74. On the DMA control card, CR1, CIN, and T7 signals combine to generate a SWCR1 signal to advance the word count register on the DMA register card at T7 of phase 5 (T7 of second phase 5 for byte mode).

4-75. DMA COMPLETION INTERRUPT. The DMA option repeats the register stepping and word transfer process until the service request for the final character word is received from the I/O device. The word count register on the DMA register card is incremented just before the final character is transferred, making the count in the word count register zero. When the word count register is set to zero, the OVFL FF is set, generating a WCR1 signal. The WCR1 signal causes a false output at MC117A on the DMA control card and inhibits the generation of further STC and CLF signals. At T4T5B, a CLC signal is generated by MC83B on the DMA control card to turn off the selected device and thus inhibit any SRQ signals by the device until the initialization process is repeated. With all SRQ lines false on the DMA address encoder card, the CR1 FF is cleared at T6 and the I/O system interrupt control is enabled at the next phase 1.

4-76. With the transfer enable FF on the DMA control card set and the WCR1 signal true, the flag 6 buffer FF is set. (This will reset the transfer enable 1 FF at T4T5B.) At T2, the enable flag (ENF) signal and the flag 6 buffer FF set the flag 6 FF. With the interrupt enable (IEN) signal true and control FF 6 and the flag 6 FF outputing true signals, the interrupt request 6 FF (IRQ6 FF) is set at T5. The flag 0 (FLG0) and IRQ6 signals are routed to the I/O address card in the CPU where the signals try to generate the interrupt signal. The I/O control card disables the interrupt, however, for at least one phase to allow execution of at least one main program instruction phase following a phase 5 operation. At the end of this regular machine phase, DMA interrupts, setting the computer for phase 4 and forcing the DMA trap cell location into the M-register. The jump subroutine (JSB) instruction for DMA completion is then the next fetched instruction. In the DMA completion subroutine, DMA is turned off and must be re-initialized before being placed in operation again.

4-77. DMA OUTPUT OPERATION.

4-78. Many of the DMA output functions are the same as the functions for an input operation described pre-

viously. The initialization process for either operation uses the same basic steps, although the control words differ slightly to prepare DMA to either input a word to computer memory or output a word from memory. (Refer to paragraph 4-55 for information on the initialization process.) Since the two operations are similar, only the essential differences are covered in detail in the following paragraphs.

4-79. An SRQ signal is generated and handled in the same manner as the SRQ for an input operation. (Refer to paragraph 4-65.) Also, PH5 signal generation is the same. (Refer to paragraph 4-66.)

4-80. CENTRAL PROCESSOR UNIT CONTROL SUSPENSION. When phase 5 is set, the CPU and I/O system are under DMA control, exclusively. If byte operation is being used, two phase 5 cycles will be required to transfer a word out of memory to the external device. On each phase 5 cycle (even cycles, only, for byte mode), control signals cause the following:

a. The PH5 signal disables the M-register lines on the DML card through inverter MC75 and enables the DM lines from the memory address register. This provides the memory address register with access to the CPU memory to control the location of the first word transferred.

b. The PH5 signal generates a false enable phase (EPH) signal at the DML card to block phase decoding at the computer timing generator card until phase 5 is complete.

c. The PH5 signal generates a true P123 signal at the DML card to enable memory read and write timing signals and generate a true reset T-register (RST) signal at the computer timing generator card.

d. The PH5 signal generates a false P123G signal at the DML card which disables a gate on the computer shift logic card and prevents possible decoding of the data on the T-bus as an addressable register command by the addressable register and the respective decode network.

e. The PH5 signal prevents the I/O address card from generating an interrupt by clearing the interrupt control FF on the I/O control card to give a false enable service request (ESR) signal. The PH5 signal also disables any I/O select code decoding. During phase 5, the hold interrupt system (HIS) signal from the address encoder card disables all interrupts from I/O devices.

f. The PH5 signal generates a true inhibit instruction register (IIR) signal at the DML card which prevents instructions from being decoded during phase 5 by generating an IIR signal at the computer timing generator card.

g. On the DMA address encoder card, the PH5 signal and the CR1 FF output are "anded" in MC126A and the combined output is used to enable the output of the service select register to generate SCM and SCL signals to the selected device.

h. The memory address bits stored in the memory address register are clocked onto the DM lines by the SMAR signal from the DMA control card.

4-81. CHARACTER UNPACKING. When a 16-bit word is to be output to a device that utilizes byte words, the 16-bit word is first separated into two 8-bit words. This is done by the DMA character packer card and requires two phase 5 cycles. During the first phase 5 cycle, the true signal from the set side of the CR1 FF and the true signal from the reset side of cycle divide 1 FF make MC47C output a false signal on the DMA address encoder card. This makes a true character out (COUT) signal at pin 36. On the DMA control card, the false DIN1 signal is "anded" with CR1, PH5, and COUT to provide the true OUT signal at pin 65. On the DMA address encoder card, the OUT signal is "anded" with CM1, CR1, CD1, and IOO signals to provide the OHC1 signal, which is used to implement character unpacking. The character mode 1 FF is set by bit 14 (byte operation) to provide the CM1 signal; the CR1 FF is set by the SRQ signal to provide the CR1 signal; CD1 is true until CR1 FF is reset at T6; and the OUT and IOO signals are true.

4-82. During the first phase 5, the memory output is put into the T-register when DMA enables read timing with DMA pseudo control signal P123. The lower T-register bits are routed to MC17A through MC47B and the upper bits to MC57A through MC126A on the DMA character packer card. At T4T5, OHC1 gates the upper 8 bits onto IOBO lines 0 through 7 and stores the lower 8 bits in the character packer register until the next phase 5. At that time, these lower bits will be gated onto IOBO lines 0 through 7 by OLC1.

4-83. All other features of a DMA output operation are basically the same as the corresponding input operation features. Refer to paragraph 4-70 for information on STC and CLF signal generation, paragraph 4-72 for register stepping, and paragraph 4-74 for DMA completion interrupt.

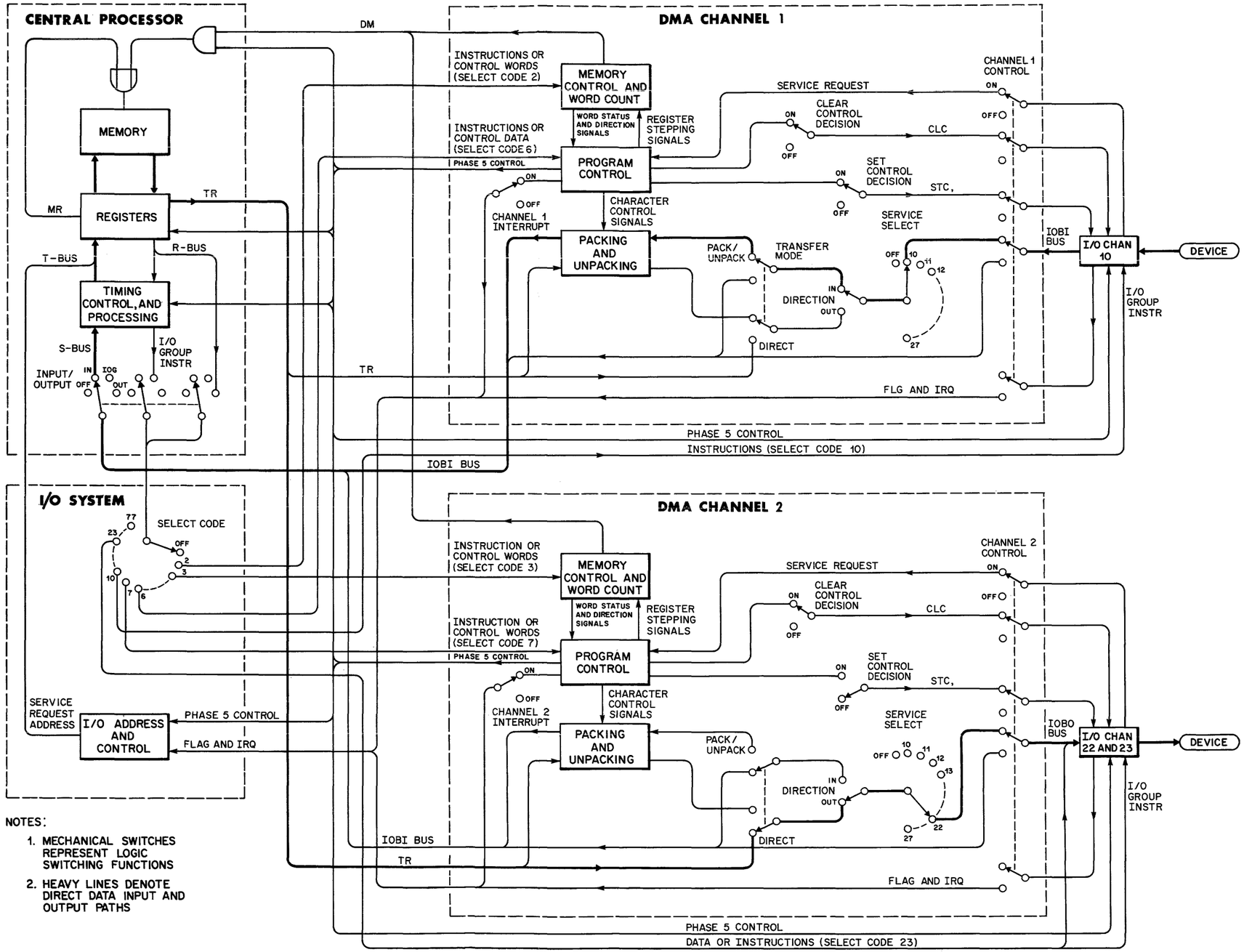


Figure 4-1. DMA Option Functional Block Diagram

SECTION V
MAINTENANCE

5-1. INTRODUCTION.

5-2. This section contains information on diagnostics and troubleshooting for the DMA option.

5-3. PREVENTIVE MAINTENANCE.

5-4. Detailed preventive maintenance procedures and schedules are provided in Volume Two of the Hewlett-Packard computer documentation. There are no separate preventive maintenance procedures to be performed on the interface kit.

5-5. DIAGNOSTICS.

5-6. The DMA accessory kit may be checked using the Diagnostic Program Procedure, part no. 12578-90013, contained in the *Manual of Diagnostics*. This diagnostic tests the DMA registers, memory addressing, data transfer, control, and flag circuit capabilities on a go/no-go basis. The diagnostic requires that the DMA printed-circuit cards be installed in the proper computer slots (refer to table 1-1) and that the following test equipment be available:

a. Microcircuit Interface Card, part no. 12566-6001 or 16-Bit Duplex Register, part no. 12554-60023. Jumper wire configurations for both cards are provided in the diagnostic program procedure.

b. Test Connector, part no. 1251-0332, with the pins shorted as shown in the diagnostic program procedure.

5-7. TROUBLESHOOTING.

5-8. Troubleshooting the DMA option is accomplished by performing the tests in the diagnostic program procedures and analyzing the error halts that occur as the test is run. Error halt codes will appear in the T-register and are listed in table 5-1. To further isolate trouble, the following aids are provided:

Note

The true or high state (logic 1) for signals in this manual is +2.5 ± 0.5 volts. The false or low state (logic 0) is ground or a saturated transistor to ground.

a. DMA I/O signals and equations in table 5-2.

b. Logic and parts location diagrams in figures 5-1 through 5-6.

c. Timing diagrams in figures 5-7 through 5-10.

Note

For 2116C computers, the mnemonic DM is changed to M. In table 5-2 and in logic and timing diagrams, DM0 through DM14 changes to M0 through M14 and DMFF0 through DMFF14 changes to MFF0 through MFF14.

Table 5-1. DMA Performance Test Error Halts

HLT XXB	ERROR
01	FL6 NOT SET
02	FL6 SET
03	SFS 6 BAD
04	SFC 6 BAD
05	FL7 NOT SET
06	SFS 7 BAD
07	FL7 SET
10	SFC 7 BAD
06	NO INT. ON 6
07	NO INT. ON 7
11	ILLEGAL INT. ON 6
12	ILLEGAL INT. ON 7
13	BAD BIT-WDCT REG 1
14	BAD BIT-WDCT REG 2
15	WDCT ROLLOVER 1 BAD
16	BAD TRANSDER CH. 1
17	WDCT ROLLOVER 2 BAD
20	BAD TRANSFER CH. 2
21	SW. REG NOT SET
22	ADDRESS ERROR - DMA 1
23	ADDRESS ERROR - DMA 2
24	FL6 NOT SET
25	FL7 NOT SET
60	SUCCESSFUL TEST
26	BAD DATA FOUND IN COMPRE
31	START OF PACKER TEST
27	OUTPUT PACK-DMA 1 BAD
30	OUTPUT PACK-DMA 2 BAD
31	INPUT PACK-DMA 1 BAD
32	INPUT PACK-DMA 2 BAD
33	CLC-DMA 1 FAILED
34	CLC-DMA 2 FAILED
35	END OF DIAGNOSTIC

Table 5-2. DMA Option Input/Output Signals and Equations

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
ADDR2 = (IOGB)(SCM0)(SCL2)	1. Select code address 2 enabling signals decoded 2. DMA register card 1 3. *Enables DMA channel 1 circuits addressed by select code 2
ADDR3 = (IOGB)(SCM0)(SCL3)	1. Select code address 3 enabling signals decoded 2. DMA register card 2 3. *Enables DMA channel 2 circuits addressed by select code 3
ADDR6 = (IOGB)(SCM0)(SCL6)	1. Select code address 6 enabling signals decoded 2. DMA encoder card and DMA control card 3. *Enables DMA channel 1 circuits addressed by select code 6
ADDR7 = (IOGB)(SCM0)(SCL7)	1. Select code address 7 enabling signals decoded 2. DMA encoder card and DMA control card 3. *Enables DMA channel 2 circuits addressed by select code 7
ADF = (PH5)[(CR1)(DIN1) + (CR2)(DIN2)] (ENF)	1. ADD function 2. DMA control card 3. **Enables ADD function on arithmetic logic card to establish direct path between IOBI lines and T-register during phase 5 data input cycles
CDF1 = (CR1)(PH5) $\overline{CDF1}$ = (ADDR6)(STC) = (CR1)(PH5)	1. Cycle divide FF, DMA channel 1 2. DMA address encoder card 3a. *Set: Enables low character transfer during even (second, fourth, etc.) phase 5 cycles 3b. *Clear: Enables high character data transfer during odd (first, third, etc.) phase 5 cycles
CDF2 = (CR2)(PH5) $\overline{CDF2}$ = (ADDR6)(STC) = (CR2)(PH5)	1. Cycle divide FF, DMA channel 2 2. DMA address encoder card 3a. *Set: Enables low character transfer during even (second, fourth, etc.) phase 5 cycles 3b. *Clear: Enables high character data transfer during odd (first, third, etc.) phase 5 cycles

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
CIN = (CR1)(CDF1) + (CR1)($\overline{CM1}$) = (CR2)(CDF2) + (CR2)($\overline{CM2}$)	1. Character in signal 2. DMA address encoder card 3a. Controls generation of register stepping signals for DMA channel 1 3b. Controls generation of register stepping signals for DMA channel 2
CLC = (IOG)(T4)($\overline{TR11}$)(TR8)(TR7)(TR6) = [(CLCD1)(CR1)(WCR1) + (CLCD2)(CR2)(WCR2)] (T4T5B)	1. Clear control signal 2a. Shift logic card 3a. Clears I/O control FF addressed by program instructions 2b. DMA control card 3b. **Clears I/O control FF addressed by DMA channel 1 or 2
CLCD1 = (ADDR6)(IOO)(IOBO13) $\overline{CLCD1}$ = (ADDR6)(IOO)($\overline{IOBO13}$)	1. Clear control decision FF, DMA channel 1 2. DMA control card 3a. *Set: Enables generation of pseudo CLC signal by DMA channel 1 when word count reaches zero 3b. *Clear: Inhibits generation of pseudo CLC signal by DMA channel 1
CLCD2 = (ADDR7)(IOO)(IOBO13) $\overline{CLCD2}$ = (ADDR7)(IOO)($\overline{IOBO13}$)	1. Clear control decision FF, DMA channel 2 2. DMA control card 3a. *Set: Enables generation of pseudo CLC signal by DMA channel 2 when word count reaches zero 3b. *Clear: Inhibits generation of pseudo CLC signal by DMA channel 2
CLF = (IOG)(T4)(TR9) = [($\overline{WCR1}$)($\overline{DIN1}$)(CR1) + ($\overline{WCR2}$)($\overline{DIN2}$)(CR2)] (T4T5B)	1. Clear flag signal 2a. Shift logic card 3a. Clears flag FF addressed by program instructions 2b. DMA control card 3b. **Clears flag FF addressed by DMA channel 1 or 2
CM1 = (SSI1)(IOBO14) $\overline{CM1}$ = (SSI1)($\overline{IOBO14}$)	1. Character mode FF, DMA channel 1 2. DMA address encoder card 3a. Set: Sets character data transfer mode and enables generation of character packing or unpacking control signals 3b. Clear: Sets word data transfer mode and controls generation of register stepping signals for DMA channel 1 during this mode

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
CM2 = (SSI2)(IOBO14) $\overline{CM2}$ = (SSI2)($\overline{IOBO14}$)	1. Character mode FF, DMA channel 2 2. DMA address encoder card 3a. Set: Sets character data transfer mode and enables generation of character packing or unpacking control signals 3b. Clear: Sets word data transfer mode and controls generation of register stepping signals for DMA channel 2 during this mode
COUT = (CR1)(CDF1) + (CR1)($\overline{CM1}$) = (CR2)(CDF2) + (CR2)($\overline{CM2}$)	1. Character out signal 2. DMA address encoder card 3a. Controls generation of register stepping signals for DMA channel 1 3b. Controls generation of register stepping signals for DMA channel 2
CR1 = CRF1	1. Cycle request, DMA channel 1 2. DMA address encoder card 3. Controls phase 5 FF
CR2 = (CRF2)($\overline{CRF1}$)	1. Cycle request, DMA channel 2 2. DMA address encoder card 3. Controls phase 5 FF
CRE1 = [(SRQ10)(100) + (SRQ11)(101) + (SRQ12)(102) + (SRQ13)(103) + (SRQ14)(104) + (SRQ15)(105) + (SRQ16)(106) + (SRQ17)(107)] (110) + [(SRQ20)(100) + (SRQ21)(101) + (SRQ22)(102) + (SRQ23)(103) + (SRQ24)(104) + (SRQ25)(105) + (SRQ26)(106) + (SRQ27)(107)] (120)	1. Cycle request enable, DMA channel 1 2. DMA address encoder card 3. *Signals presence of service request input signal from I/O channel currently under control of DMA channel 1
CRE2 = [(SRQ10)(200) + (SRQ11)(201) + (SRQ12)(202) + (SRQ13)(203) + (SRQ14)(204) + (SRQ15)(205) + (SRQ16)(206) + (SRQ17)(207)] (210) + [(SRQ20)(200) + (SRQ21)(201) + (SRQ22)(202) + (SRQ13)(203) + (SRQ14)(204) + (SRQ15)(205) + (SRQ16)(206) + (SRQ17)(207)] (220)	1. Cycle request enable, DMA channel 2 2. DMA address encoder card 3. *Signals presence of service request input signal from I/O channel currently under control of DMA channel 2

*Internal card function; not routed through backplane wiring.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
CRF1 = (CRE1)(PRH6)(TE1)(T6T7) $\overline{CRF1}$ = (CRS) + [($\overline{CRE1}$) + ($\overline{PRH6}$) + ($\overline{TE1}$)] (T6T7)	1. Cycle request FF, DMA channel 1 2. DMA address encoder card 3a. *Set: Generates CR1 signal 3b. *Clear: Controls generation of HIS signal
CRF2 = (CRE2) [(CRE1) + (PRH6) + (PRH6) + (TE1)] (TE2)(T6T7) $\overline{CRF2}$ = (CRS) + [(CRE1)(PRH6)(TE1) + ($\overline{CRE2}$) + ($\overline{TE2}$)] (T6T7)	1. Cycle request FF, DMA channel 2 2. DMA address encoder card 3a. *Set: Generates CR2 signal 3b. *Clear: Controls generation of HIS signal
CRS = POPIO (buffered) + CLC0	1. Control reset to I/O registers 2. I/O control card 3. Resets DMA cycle request and all I/O control FF's when power is applied or CLC instruction for select code 0 is executed
CTF2 = (ADDR2)(STC) $\overline{CTF2}$ = (CRS) + (ADDR2)(CLC)	1. DMA register control FF, channel 1 2. DMA register card 1 3a. *Set: Enables DMA word count register loading 3b. *Clear: Enables DMA direct memory address register loading
CTF3 = (ADDR3)(STC) $\overline{CTF3}$ = (CRS) + (ADDR3)(CLC)	1. DMA register control FF, channel 2 2. DMA register card 2 3a. *Set: Enables DMA word count register loading 3b. *Clear: Enables DMA direct memory address loading
CTF6 = (ADDR6)(STC) $\overline{CTF6}$ = (CRS) + (ADDR6)(CLC)	1. DMA I/O control FF, channel 1 2. DMA control card 3a. *Set: Enables DMA channel 1 interrupt 3b. *Clear: Inhibits DMA channel 1 interrupt
CTF7 = (ADDR7)(STC) $\overline{CTF7}$ = (CRS) + (ADDR7)(CLC)	1. DMA I/O control FF, channel 2 2. DMA control card 3a. *Set: Enables DMA channel 2 3b. *Clear: Inhibits DMA channel 2

*Internal card function; not routed through backplane wiring.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
DAWI1 = $\overline{(CTF2)}$(ADDR2)(IOO)(TS)	1. DMA address word input control, channel 1 2. DMA register card 7 3. *Strobes DMA address word bits on IOBO lines 0 thru 15 into direct memory address register FF's and DMA input (direction) FF
DAWI2 = $\overline{(CTF3)}$(ADDR3)(IOO)(TS)	1. DMA address word input control, channel 2 2. DMA register card 2 3. *Strobes DMA address word bits on IOBO lines 0 thru 15 into direct memory address register FF's and DMA input (direction) FF
DAWR1 = $\overline{(CTF2)}$(ADDR2)(IOO)(T3)	1. DMA address word reset control, channel 1 2. DMA register card 1 3. *Clears direct memory address register FF's and DMA input (direction) FF
DAWR2 = $\overline{(CTF3)}$(ADDR3)(IOO)(T3)	1. DMA address word reset control, channel 2 2. DMA register card 2 3. *Clears direct memory address register FF's and DMA input (direction) FF
DIN1 = (DAWI1)(IOBO15) $\overline{DIN1}$ = (DAWR1)	1. DMA input (direction) FF, channel 1 2. DMA register card 1 3a. Set: Sets input data transfer mode 3b. *Clear: Sets output data transfer mode
DIN2 = (DAWI2)(IOBO15) $\overline{DIN2}$ = (DAWR2)	1. DMA input (direction) FF, channel 2 2. DMA register card 2 3a. Set: Sets input data transfer mode 3b. *Clear: Sets output data transfer mode
DM0-14 = (DMFF0-14)(SMAR1) = (DMFF0-14)(SMAR2)	1. Direct memory address, bits 0 thru 14 2. DMA register card 1 or 2 3a. **Direct memory address from DMA channel 1 3b. **Direct memory address from DMA channel 2
DMFF0-14 = (DAWI1)(IOBO0-14) $\overline{DMFF0-14}$ = (DAWR1)	1. Direct memory address register FF's 0 thru 14, DMA channel 1 2. DMA register card 1 3a. *Set: Stores direct memory starting address for DMA channel 1 3b. *Clear: All DMA channel 1 direct memory address register FF's reset

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
DMFF0-14 = (DAWI2)(IOBO0-14) $\overline{\text{DMFF0-14}}$ = (DAWR2)	1. Direct memory address register FF's 0 thru 14, DMA channel 2 2. DMA register card 2 3a. *Set: Stores direct memory starting address for DMA channel 2 3b. *Clear: All DMA channel 2 direct memory address register FF's reset
DWCI1 = (CTF2)(ADDR6)(IOO)(TS)	1. DMA word count input control, channel 1 2. DMA register card 1 3. *Strobes DMA word count bits on IOBO lines 0 thru 13 into word count register FF's
DWCI2 = (CTF3)(ADDR7)(IOO)(TS)	1. DMA word count input control, channel 2 2. DMA register card 2 3. *Strobes DMA word count bits on IOBO lines 0 thru 13 into word count register FF's
DWCR1 = (CTF2)(ADDR2)(IOO)(T3)	1. DMA word count reset control, channel 1 2. DMA register card 1 3. *Clears word count register FF's and overflow (rollover) FF
DWCR2 = (CTF3)(ADDR3)(IOO)(T3)	1. DMA word count reset control, channel 2 2. DMA register card 2 3. *Clears word count register FF's and overflow (rollover) FF
EDT (not used)	
ENF = T2 (buffered)	1. Enable flag signal 2. I/O control card 3. Clocking control signal to DMA control card and DMA address encoder card
EPH = $\overline{\text{PH5}}$	1. Enable phase signal 2. Direct memory logic card 3. **Enables phase FF output gates on timing generator card when present; inhibits phase FF output gates when absent
FBF6 = [(POPIO) + (TE1)(WCR1) + (ADDR6)(STF)] ($\overline{\text{FBF6}}$) $\overline{\text{FBF6}}$ = [(IAK)(IRQ6) + (ADDR7)(CLF)] (FBF6)	1. Flag buffer FF I/O channel 6 2. DMA control card 3a. *Set: Enables flag 6 FF, DMA channel 1 3b. *Clear: Inhibits flag 6 FF, DMA channel 1

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
FBF7 = [(POPIO) + (TE2)(WCR2) + (ADDR7)(STF)] $\overline{(FBF7)}$ $\overline{FBF7}$ = [(IAK)(IRQ7) + (ADDR7)(CLF)] (FBF7)	1. Flag buffer FF I/O channel 7 2. DMA control card 3a. *Set: Enables flag 7 FF, DMA channel 2 3b. *Clear: Inhibits flag 7 FF, DMA channel 2
FLF6 = (FBF6)(ENF) $\overline{FLF6}$ = (ADDR6)(CLF)	1. Flag FF I/O channel 6 2. DMA control card 3a. *Set: Enables interrupt request from DMA channel 1 3b. *Clear: Inhibits interrupt request from DMA channel 1
FLF7 = (FBF7)(ENF) $\overline{FLF7}$ = (ADDR7)(CLF)	1. Flag FF I/O channel 7 2. DMA control card 3a. *Set: Enables interrupt request from DMA channel 2 3b. *Clear: Inhibits interrupt request from DMA channel 2
FLG0 = (IRQ6) + (IRQ7)	1. Flag from I/O channel 6, DMA channel 1 or 2 2. DMA control card 3. Clocks generation of interrupt signal on I/O address card
HIS = (CR1) + (CR2) + (PH5)	1. Hold interrupt system 2. DMA address encoder card 3. Inhibits interrupt system during phase 5 data transfer cycles
IAK = $\overline{(ICF)}$(PH1)(T1)	1. Interrupt acknowledge 2. I/O control card 3. Clocks reset of flag buffer 6 and flag buffer 7 FF's on DMA control card
IDW1 = (CM1)(CR1)(CDF1)(IOI)	1. Input data word from DMA channel 1 2. DMA address encoder 3. Strobes high character data bits stored by input holding register onto IOBI lines 0-7
IEN6 = (ISEF)	1. Interrupt enable, I/O select codes 6 and 7 2. I/O control card 3. Interrupt enable for DMA channels 1 and 2

*Internal card function; not routed through backplane wiring.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
IHC1 = (CM1)(CR1)$\overline{(CDF1)}$(IOI)(ENF)(TS)	1. Input high character to DMA channel 1 2. DMA address encoder 3. Strobes data bits on IOBI lines 0-7 into input holding register for DMA channel 1
IHC2 = (CM2)(CR2)$\overline{(CDF2)}$(IOI)(ENF)(TS)	1. Input high character to DMA channel 2 2. DMA address encoder 3. Strobes data bits on IOBI lines 0-7 into input holding register for DMA channel 2
IHR10-17 = (IOBO0-7)(IHC1) $\overline{IHR10-17}$ = $\overline{(IOBO0-7)}$(IHC1)	1. Input holding register FF's, DMA channel 1 2. DMA character packer card 3a. *Set: Register FF stores binary 1 high character data bit 3b. *Clear: Register FF stores binary 0 high character data bit
IHR20-27 = (IOBO0-7)(IHC2) $\overline{IHR20-27}$ = $\overline{(IOBO0-7)}$(IHC2)	1. Input holding register FF's, DMA channel 2 2. DMA character packer card 3a. *Set: Register FF stores binary 1 high character data bit 3b. *Clear: Register FF stores binary 0 high character data bit
IIR = (PH5)	1. Inhibit instruction register output signal 2. Direct memory logic card 3. **Inhibits generation of instruction register enabling signal on timing generator card
IN (not used)	
IOBI0-7 = (Refer to applicable I/O interface card manual) = (WC0-7)(ADDR2)(IOI) = (WC0-7)(ADDR3)(IOI)	1. I/O bus input, lines 0-7 2a. I/O interface cards 3a. Word or low character input bits 0-7 from I/O channels to S-bus lines 0-7, or high character input bits 0-7 to DMA character packer card 2b. DMA register card 1 3b. Word count bits 0-7, DMA channel 1, to S-bus lines 0-7 2c. DMA register card 2 3c. Word count, bits 0-7, DMA channel 2, to S-bus lines 0-7

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
IOBI8-13 = (Refer to applicable I/O interface card manual) = (IHR10-15)(IDW1) = (IHR20-25)(IDW2) = (WC8-13)(ADDR2)(IOI) = (WC8-13)(ADDR3)(IOI)	1. I/O bus input, lines 8-13 2a. I/O interface card 3a. Word input bits 8-13 from I/O channel to S-bus lines 8-13 2b. DMA character packer card 3b. High character input bits 0-5 from DMA channel 1 to S-bus lines 8-13 2c. DMA character packer card 3c. High character input bits 0-5 from DMA channel 2 to S-bus lines 8-13 2d. DMA register card 1 3d. Word count bits 8-13, DMA channel 1, to S-bus lines 8-13 2e. DMA register card 2 3e. Word count bits 8-13, DMA channel 2, to S-bus lines 8-13
IOBI14,15 = (Refer to applicable I/O Interface Card Manual) = (IHR16,17)(IDW1) = (IHR26,27)(IDW2)	1. I/O bus input, lines 14 and 15 2a. I/O interface cards 3a. Word input bits 14 and 15 from I/O channel to S-bus lines 14 and 15 2b. DMA character packer card 3b. High character input bits 6 and 7 from DMA channel 1 to S-bus lines 14 and 15 2c. DMA character packer card 3c. High character input bit 6 and 7 from DMA channel 2 to S-bus lines 14 and 15
IOBO0-7 = (RB0-7)(IOCO) = (TR0-7)(IODO) = (TR8-15)(OHC1 + OHC2) = (OHR10-17)(OLC1) = (OHR20-27)(OLC2)	1. I/O bus output lines 0-7 2a. Arithmetic logic board 3a. Output from R-bus lines 0-7 2b. DMA character packer card 3b. Word output bits 0-7 from DMA channel 1 or 2 2c. DMA character packer card 3c. High character output bits 0-7 from DMA channel 1 or 2 2d. DMA character packer card 3d. Low character output bits 0-7 from DMA channel 1 2e. DMA character packer card 3e. Low character output bits 0-7 from DMA channel 2

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
IOBO8-15 = (RB8-15)(IOCO) = (TR8-15)(IODO)	1. I/O bus output lines 8-15 2a. Arithmetic logic card 3a. Output from R-bus lines 8-15 2b. DMA character packer card 3b. Word output bits 8-15 from DMA channel 1 or 2
IOCI = (PH5) [(CR1)(DIN1) + (CR2)(DIN2)] (ENF)	1. I/O control input 2. DMA control card 3. **Sames as **IOI
IODO = [$\overline{(CM1)}$(CR1) + $\overline{(CM2)}$(CR2)] (PH5) [(CR1)$\overline{(DIN1)}$ + (CR2)$\overline{(DIN2)}$] (T4T5B)	1. I/O data out (DMA channel 1 or 2) 2. DMA control card 3. Strobes word data bits TR0 thru TR15 onto IOBO lines 0-15
IOGB = (IOG delayed 100 ns) = (CR1)(PH5) + (CR2)(PH5)	1. IOG buffered signal 2a. I/O control card 3a. Select code address enabling signal for I/O channels addressed under program control 2b. DMA address encoder card 3b. **Select code address enabling signal for I/O channels addressed by DMA channel 1 or 2
IOI = (IOG)(T4T5)(TR8)$\overline{(TR7)}$ + (SEO)(T2) = (PH5) [(CR1)(DIN1) + (CR2)(DIN2)] (ENF)	1. I/O input signal 2a. Shift logic card 3a. Enables IOBI lines under program or switch register control 2b. DMA control card 3b. **Enables IOBI lines under control of DMA channel 1 or 2
IOO = (T3T4)(TR8)(TR7)$\overline{(TR6)}$ [(IOG) + (SRG)(T3)] = (T3T4)(PH5) [(CR1)$\overline{(DIN1)}$ + (CR2)$\overline{(DIN2)}$]	1. I/O output signal 2a. Shift logic card 3a. Enables IOBO lines under program control 2b. DMA control card 3b. **Enables IOBO lines under control of DMA channel 1 or 2
IRF6 = (SIR)(PRH6)(FBF6)(IEN6)(FLF6)(CTF6) $\overline{IRF6}$ = (ENF)	1. Interrupt request FF, I/O channel 7 2. DMA control card 3a. *Set: Generates IRQ6 and FLG0 signals for DMA channel 1 3b. *Clear: Inhibits IRQ6 and FLG0 signals for DMA channel 1

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
IRF7 = (SIR)(PRH7)(FBF7)(IEN6)(FLF7)(CTF7) $\overline{IRF7}$ = (ENF)	1. Interrupt request FF, I/O channel 7 2. DMA control card 3a. *Set: Generates IRQ6 and FLG0 signals from DMA channel 2 3b. *Clear: Inhibits IRQ6 and FLG0 signals from DMA channel 2
IRQ6 = IRF6	1. Interrupt request, I/O channel 6 2. DMA control card 3. Interrupt request to I/O address card from DMA channel 1
IRQ7 = IRF7	1. Interrupt request, I/O channel 7 2. DMA control card 3. Interrupt request to I/O address card from DMA channel 2
ISG = (PH5) [(CR1)(DIN1) + (CR2)(DIN2)] (ENF)	1. Inhibit strobe generator 2. DMA control card 3. **Inhibits generation of memory strobe timing (MST) signal on timing generator card
M0-14 = (MR0-14)($\overline{PH5}$) = (DM0-14)(PH5) $\overline{M0\text{-}12}$ = ($\overline{MR0\text{-}14}$)($\overline{PH5}$) = (DM0-14)(PH5)	1. Memory address bits 2. Direct memory logic card 3a. Provides binary 1 memory address bits during program control 3b. **Provides binary 1 memory address bits during DMA channel 1 or 2 control 3c. Provides binary 0 memory address bits during program control 3d. **Provides binary 0 memory address bits during DMA channel 1 or 2 control
OHC1 = (CM1)(CR1)(CDF1)(IOO)(OUT)	1. Output high character from DMA channel 1 2. DMA address encoder 3. Strobes high character data bits from TR8 thru TR15 onto IOBO lines 0-7, respectively; strobes low character data bits from TR0 thru TR7 into channel 1 output holding register
OHC2 = (CM2)(CR2)(CDF2)(IOO)(OUT)	1. Output high character from DMA channel 2 2. DMA address encoder 3. Strobes high character data bits TR8 thru TR15 onto IOBO lines 0-7, respectively; strobes low character data bits from TR0 thru TR7 into channel 2 output holding register

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
OHR10-17 = (TR0-7)(OHC1) $\overline{OHR10\text{-}17}$ = $\overline{(TR0\text{-}7)}$(OHC1)	1. Output holding register FF's, DMA channel 1 2. DMA character packer card 3a. *Set: Register FF stores binary 1 low character data bit 3b. **Clear: Register FF stores binary 0 low character data bit
OHR20-27 = (TR0-7)(OHC2) $\overline{OHR20\text{-}27}$ = $\overline{(TR0\text{-}7)}$(OHC2)	1. Output holding register FF's DMA channel 2 2. DMA character packer card 3a. *Set: Register FF stores binary 1 low character data bit 3b. *Clear: Register FF stores binary 0 low character data bit
OLC1 = (CM1)(CR1)(CDF1)(T4T5 Delayed)	1. Output low character from DMA channel 1 2. DMA address encoder card 3. Strobes low character data bits stored by output holding register onto IOBO lines 0-7
OLC2 = (CM2)(CR2)(CDF2)(T4T5 Delayed)	1. Output low character from DMA channel 2 2. DMA channel 2 3. Strobes low character data bits stored by output holding register onto IOBO lines 0-7
OUT = (COUT)(PH5) [(CR1)$\overline{(DIN1)}$ + (CR2)$\overline{(DIN2)}$]	1. Output high character 2. DMA control card 3. Enables generation of OHC1 and OHC2 signals
P123 = PH5	1. Phase 1, phase 2, or phase 3 2. Direct memory logic card 3. **Simulates P123 output on timing generator card
P123G = $\overline{PH5}$	1. Phase 1, phase 2, or phase 3 2. Direct memory logic card 3. **Inhibits A/B address flip-flop on shift logic card during phase 5 cycles
PH5 = [(CR1) + (CR2)] T7TS $\overline{PH5}$ = T7TS	1. Phase 5 FF, DMA channel 1 or 2 2. DMA control card 3a. Primary DMA control signal; turns-on phase 5 direct memory access cycle and controls pseudo operation of central processor and I/O control system 3b. *Turns-off phase 5

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
POPIO = T5 [(POFP) + (PRS)($\overline{SWC}$)]	1. Power on pulse to I/O 2. Timing generator card 3. Resets flag buffer 6 FF and flag buffer 7 FF when power is applied
PRH6 = PRL5	1. Priority high I/O channel 6; priority low I/O channel 5 2. Power fail control card 3. Enables DMA channel 1 cycle request and interrupt request
PRH7 = PRL6 = (PRH6) [($\overline{FLF6}$) + ($\overline{CTF6}$) + ($\overline{IEN}$)]	1. Priority high I/O channel 7; priority low I/O channel 6 2. DMA control card 3. *Enables DMA channel 2 cycle request and interrupt request
PRL7 = PRH10 = (PRH7) [($\overline{FLF7}$) + ($\overline{CTF7}$) + ($\overline{IEN}$)]	1. Priority low I/O channel 7; priority high I/O channel 10 2. DMA control card 3. Enables I/O channel 10
SCL0 = ($\overline{100}$) + ($\overline{200}$) = ($\overline{TR2}$)($\overline{TR1}$)($\overline{TR0}$)(PH5)	1. Select code least significant octal digit zero 2a. DMA address encoder card 3a. **Address enabling signal to all I/O channels, addressed under control of DMA channel 1 or 2, having select code least significant octal digit zero 2b. I/O address card 3b. Address enabling signal to all I/O channels, addressed under program control, having select code least significant octal digit zero
SCL1 = ($\overline{101}$) + ($\overline{201}$) = ($\overline{TR2}$)($\overline{TR1}$)(TR0)($\overline{PH5}$)	1. Select code least significant octal digit one 2a. DMA address encoder card 3a. **Address enabling signal to all I/O channels, addressed under control of DMA channel 1 or 2, having select code least significant octal digit one 2b. I/O address card 3b. Address enabling signal to all I/O channels, addressed under program control, having select code least significant octal digit one

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
SCL2 = $\overline{(102)}$ + $\overline{(202)}$ = $\overline{(TR2)}\overline{(TR1)}(TR0)\overline{(PH5)}$	1. Select code least significant octal digit two 2a. DMA address encoder card 3a. **Address enabling signal to all I/O channels, addressed under control of DMA channel 1 or 2, having select code least significant octal digit two 2b. I/O address card 3b. Address enabling signal to all I/O channels, addressed under program control, having select code least significant octal digit two
SCL3 = $\overline{(103)}$ + $\overline{(203)}$ = $\overline{(TR2)}(TR1)(TR0)\overline{(PH5)}$	1. Select code least significant octal digit three 2a. DMA address encoder card 3a. **Address enabling signal to all I/O channels, addressed under control of DMA channel 1 or 2, having select code least significant octal digit three 2b. I/O address card 3b. Address enabling signal to all I/O channels, addressed under program control, having select code least significant octal digit three
SCL4 = $\overline{(104)}$ + $\overline{(204)}$ = (TR2)$\overline{(TR1)}\overline{(TR0)}$(PH5)	1. Select code least significant octal digit four 2a. DMA address encoder card 3a. **Address enabling signal to all I/O channels, addressed under control of DMA channel 1 or 2, having select code least significant octal digit four 2b. I/O address card 3b. Address enabling signal to all I/O channels, addressed under program control, having select code least significant octal digit four
SCL5 = $\overline{(105)}$ + $\overline{(205)}$ = (TR2)$\overline{(TR1)}$(TR0)$\overline{(PH5)}$	1. Select code least significant octal digit five 2a. DMA address encoder card 3a. **Address enabling signal to all I/O channels, addressed under control of DMA channel 1 or 2, having select code least significant octal digit five 2b. I/O address card 3b. Address enabling signal to all I/O channels, addressed under program control, having select code least significant octal digit five

**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
SCL6 = $\overline{(106)} + \overline{(206)}$ = (TR2)(TR1)$\overline{(TR0)}$(PH5)	1. Select code least significant octal digit six 2a. DMA address encoder card 3a. **Address enabling signal to all I/O channels, addressed under control of DMA channel 1 or 2, having select code least significant octal digit six 2b. I/O address card 3b. Address enabling signal to all I/O channels, addressed under program control, having select code least significant octal digit six
SCL7 = $\overline{(107)} + \overline{(207)}$ = (TR2)(TR1)(TR0)$\overline{(PH5)}$	1. Select code least significant octal digit seven 2a. DMA address encoder card 3a. **Address enabling signal to all I/O channels, addressed under control of DMA channel 1 or 2, having select code least significant octal digit seven 2b. I/O address card 3b. Address enabling signal to all I/O channels, addressed under program control, having select code least significant octal digit seven
SCM0 = $\overline{(TR5)}\overline{(TR4)}\overline{(TR3)}\overline{(PH5)}$	1. Select code most significant octal digit zero 2. I/O address card 3. **Address enabling signal to all I/O channels, addressed under program control, having select code most significant octal digit zero
SCM1 = $\overline{(TR5)}\overline{(TR4)}$(TR3)$\overline{(PH5)}$ = [(110)(CR1)(PH5) + (210)(CR2)(PH5)] $\overline{(SSFF15)}$	1. Select code most significant octal digit one 2a. I/O address card 3a. Address enabling signal to all I/O channels, addressed under program control, having select code most significant octal digit one 2b. DMA address encoder card 3b. **Address enabling signal to all I/O channels, addressed by DMA channel 1 or 2, having select code most significant octal digit one
SCM2 = $\overline{(TR5)}$(TR4)$\overline{(TR3)}\overline{(PH5)}$ = [(120)(CR1)(PH5) + (220)(CR2)(PH5)] $\overline{(SSFF25)}$	1. Select code most significant octal digit two 2a. I/O address card 3a. Address enabling signal to all I/O channels, addressed under program control, having select code most significant octal digit two 2b. DMA address encoder card 3b. **Address enabling signal to all I/O channels, addressed by DMA channel 1 or 2, having select code most significant octal digit two

**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
SFC = (IOG)($\overline{TR8}$)(TR7)($\overline{TR6}$)	1. Skip if flag clear, decoded 2. Shift logic card 3. Tests flag status on DMA control card under program control
SFS = (IOG)($\overline{TR8}$)(TR7)(TR6)	1. Skip if flag set, decoded 2. Shift logic card 3. Tests flag status on DMA control card under program control
SIR = T5 (buffered)	1. Set interrupt request 2. I/O control card 3. Enables interrupt logic on DMA control card
SKF = (ADDR6)(SFC)($\overline{FLF6}$) + (ADDR6)(SFS)(FLF6) + (ADDR7)(SFC)($\overline{FLF7}$) + (ADDR7)(SFS)(FLF7)	1. Skip on flag signal 2. DMA control card 3. Flag status signal to central processor from DMA channel 1 or 2
SMAR1 = (CR1)(PH5)($\overline{DIN1}$)(COUT) = (CR1)(PH5)(DIN1)(CIN)	1. Step memory address register, DMA channel 1 2. DMA control card 3a. Increments direct memory address register (on DMA register card 1) by one after completion of phase 5 word or high character output transfer 3b. Increments direct memory address register (on DMA register card 1) by 1 after completion of phase 5 word or low character input transfer
SMAR2 = (CR2)(PH5)($\overline{DIN2}$)(COUT) = (CR2)(PH5)(DIN2)(CIN)	1. Step memory address register, DMA channel 2 2. DMA control card 3a. Increments direct memory address register (on DMA register card 2) by 1 after completion of phase 5 word or high character output transfer 3b. Increments direct memory address register (on DMA register card 2) by 1 after completion of phase 5 word or low character input transfer
SRQ10-17,20-27 = FLF	1. Service request signals to DMA 2. Flag FF on interface card in I/O channel 1 3. Sets cycle request FF of DMA channel 1 or 2 on DMA address encoder card

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
SSFF10-15 = (SSI1)(IOBO0-5) $\overline{SSFF10\text{-}25}$ = (SSI1)$\overline{(IOBO0\text{-}5)}$	1. Service select register FF's, DMA channel 1 2. DMA address encoder card 3a. *Set: Register FF stores binary 1 select code bit making up address of I/O channel to be serviced by DMA channel 1 3b. *Clear: Register FF stores binary 0 select code bit making up address of I/O channel to be serviced by DMA channel 2
SSFF20-25 = (SSI2)(IOBO0-5) $\overline{SSFF20\text{-}25}$ = (SSI2)$\overline{(IOBO0\text{-}5)}$	1. Service select register FF's, DMA channel 2 2. DMA address encoder card 3a. *Set: Register FF stores binary 1 select code bit making up address of I/O channel to be serviced by DMA channel 2 3b. *Clear: Register FF stores binary 0 select code bit making up address of I/O channel to be serviced by DMA channel 2
SSI1 = (ADDR6)(IOO)	1. Service select input control, DMA channel 1 2. DMA address encoder card 3. *Strobes select code bits and character mode bits of DMA control word into service select register and character mode FF, respectively, of DMA channel 1
SSI2 = (ADDR7)(IOO)	1. Service select input control, DMA channel 2 2. DMA address encoder card 3. *Strobes select code bit and character mode bit of DMA control word into service select register and character mode FF, respectively, of DMA channel 2
STC = (IOG)(T4)$\overline{(TR11)}$(TR8)(TR7)(TR6) = [(STCD1)(CR1)$\overline{(WCR1)}$$\overline{(DIN1)}$ + (STCD2)(CR2)$\overline{(WCR2)}$$\overline{(DIN2)}$] T3T4	1. Set control signal 2a. Shift logic card 3a. Sets I/O control FF addressed by program instructions 2b. DMA control card 3b. **Sets I/O control FF addressed by DMA channel 1 or 2
STCD1 = (ADDR6)(IOO)(IOBO15) $\overline{STCD1}$ = (ADDR6)(IOO)$\overline{(IOBO15)}$	1. Set control decision FF 2. DMA control card 3a. *Set: Enables generation of STC signal by DMA channel 1 3b. *Clear: Inhibits generation of STC signal by DMA channel 1

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
STCD2 = (ADDR7)(IOO)(IOBO15) $\overline{STCD2}$ = (ADDR7)(IOO)($\overline{IOBO15}$)	1. Set control decision FF 2. DMA control card 3a. *Set: Enables generation of STC signal by DMA channel 2 3b. *Clear: Inhibits generation of STC signal by DMA channel 2
STF = (IOB + SRG) [(T3)($\overline{TR8}$)($\overline{TR7}$)(TR6)]	1. Set flag signal 2. Shift logic card 3. Sets flag FF addressed by program instruction
SWCR1 = (CR1)(CIN)(T7)	1. Step word count register, DMA channel 1 2. DMA control card 3. Increments word count register (on DMA register card 1) after completion of phase 5 word or character transfer by DMA channel 1
SWCR2 = (CR2)(CIN)(T7)	1. Step word count register, DMA channel 2 2. DMA control card 3. Increments word count register (on DMA register card 2) after completion of phase 5 word or character transfer by DMA channel 2
SWST = (PH5) [(CR1)(DIN1) + (CR2)(DIN2)] (ENF)	1. Switch store in T-register 2. DMA control card 3. **Enables store T-bus in T-register signal (STBT) on instruction decoder card
TE1 = (ADDR6)(STC) $\overline{TE1}$ = (CRS) + (FBF6)(T4T5B)	1. Transfer enable FF, DMA channel 1 2. DMA control card 3a. Set: Enables DMA channel 1 to accept service requests from selected I/O channels 3b. Clear: Inhibits service request processing by DMA channel 1
TE2 = (ADDR7)(STC) $\overline{TE2}$ = (CRS) + (FBF7)(T4T5B)	1. Transfer enable FF, DMA channel 2 2. DMA control card 3a. Set: Enables DMA channel 2 to accept service requests from selected I/O channels 3b. Clear: Inhibits service request processing by DMA channel 2
TR0-15 = T-Register FF's 0-15	1. T-register bits 0 through 15 2. Arithmetic logic card 3. Word or character data input to DMA character packer card

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
TR0-15B = TR0-15 (buffered)	1. T-register bits 0 through 15 buffered 2. DMA character packer card 3. *Buffered TR source between TR lines and IOBO lines
WCFF0-13 = (DWCI1)(IOBO0-13) $\overline{\text{WCFF0-13}}$ = (CWCR1)	1. Word count register FF's 0 thru 13 DMA channel 1 2. DMA register card 1 3a. *Set: Stores word count for DMA channel 1 3b. *Clear: All DMA channel 1 word count register FF's reset
WCFF0-13 = (DWCI2)(IOBO0-13) $\overline{\text{WCFF0-13}}$ = (DWCR2)	1. Word count register FF's 0 thru 13 DMA channel 2 2. DMA register card 2 3a. *Set: Stores word count for DMA channel 2 3b. *Clear: All DMA channel 2 word count register FF's reset
WCR1 = WCFF13 $\overline{\text{WCR1}}$ = DWCR1	1. Word count rollover (overflow) FF, DMA channel 1 2. DMA register card 1 3a. Set: Signals completion of block data transfer by DMA channel 1 when word count register content steps to zero 3b. *Clear: Overflow FF reset
WCR2 = WCFF13 $\overline{\text{WCR2}}$ = DWCR2	1. Word count rollover (overflow) FF, DMA channel 2 2. DMA register card 2 3a. Set: Signals completion of block data transfer by DMA channel 2 when word count register content steps to zero 3b. *Clear: Overflow FF reset
100 = $\overline{\text{(SSFF10)}}\overline{\text{(SSFF11)}}\overline{\text{(SSFF12)}}$	1. Detect service request (LSD 0), DMA channel 1 2. DMA address encoder card 3. *Enables SRQ 10 and 20 coincidence gates
$\overline{100}$ = $\overline{\text{(SSFF10)}}\overline{\text{(SSFF11)}}\overline{\text{(SSFF12)}}$(CR1)(PH5)	1. Service select code output (LSD 0), DMA channel 1 2. DMA address encoder card 3. *Generates **SCL0 output
101 = $\overline{\text{(SSFF10)}}\overline{\text{(SSFF11)}}$(SSFF12)	1. Detect service request (LSD 1), DMA channel 1 2. DMA address encoder card 3. *Enables SRQ 11 and 21 coincidence gates

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
$\overline{101} = \overline{(SSFF10)}\overline{(SSFF11)}(SSFF12)(CR1)(PH5)$	1. Service select code output (LSD 1), DMA channel 1 2. DMA address encoder card 3. *Generates **SCL1 output
$102 = \overline{(SSFF10)}(SSFF11)\overline{(SSFF12)}$	1. Detect service request (LSD 2), DMA channel 1 2. DMA address encoder card 3. *Enables SRQ 12 and 22 coincidence gates
$\overline{102} = \overline{(SSFF10)}(SSFF11)\overline{(SSFF12)}(CR1)(PH5)$	1. Service select code output (LSD 2), DMA channel 1 2. DMA address encoder card 3. *Generate **SCL2 output
$103 = \overline{(SSFF10)}(SSFF11)(SSFF12)$	1. Detect service request (LSD 3), DMA channel 1 2. DMA address encoder card 3. *Enables SRQ 13 and 23 coincidence gates
$\overline{103} = \overline{(SSFF10)}(SSFF11)(SSFF12)(CR1)(PH5)$	1. Service select code output (LSD 3), DMA channel 1 2. DMA address encoder card 3. *Generate **SCL3 output
$104 = (SSFF10)\overline{(SSFF11)}\overline{(SSFF12)}$	1. Detect service request (LSD 4), DMA channel 1 2. DMA address encoder card 3. *Enables SRQ 14 and 24 coincidence gates
$\overline{104} = (SSFF10)\overline{(SSFF11)}\overline{(SSFF12)}(CR1)(PH5)$	1. Service select code output (LSD 4), DMA channel 1 2. DMA address encoder card 3. *Generates **SCL 4 output
$105 = (SSFF10)\overline{(SSFF11)}(SSFF12)$	1. Detect service request (LSD 5), DMA channel 1 2. DMA address encoder card 3. *Enables SRQ 15 and 25 coincidence gates
$\overline{105} = (SSFF10)\overline{(SSFF11)}(SSFF12)(CR1)(PH5)$	1. Service select code output (LSD 5), DMA channel 1 2. DMA address encoder card 3. *Generates **SCL 5 output
$106 = (SSFF10)(SSFF11)\overline{(SSFF12)}$	1. Detect service request (LSD 6), DMA channel 1 2. DMA address encoder card 3. *Enables SRQ 16 and 26 coincidence gates
$\overline{106} = (SSFF10)(SSFF11)\overline{(SSFF12)}(CR1)(PH5)$	1. Service select code output (LSD 6), DMA channel 1 2. DMA address encoder card 3. *Generates **SCL 6 output

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
107 = (SSFF10)(SSFF11)(SSFF12)	1. Detect service request (LSD 7), DMA channel 1 2. DMA address encoder card 3. *Enables SRQ 17 and 27 coincidence gates
$\overline{107}$ = (SSFF10)(SSFF11)(SSFF12)(CR1)(PH5)	1. Service select code output (LSD 7), DMA channel 1 2. DMA address encoder card 3. *Generates **SCL 7 output
110 = $\overline{(SSFF13)}\overline{(SSFF14)}\overline{(SSFF15)}$	1. Detect service request (MSD), DMA channel 1 2. DMA address encoder card 3. *Enables SRQ 110 coincidence gates
$\overline{110}$ = $\overline{(SSFF13)}\overline{(SSFF14)}\overline{(SSFF15)}$(CR1)(PH5)	1. Service select code output (MSD 0), DMA channel 1 2. DMA address encoder card 3. *Generates **SCM 0 output
120 = $\overline{(SSFF13)}$(SSFF14)$\overline{(SSFF15)}$	1. Detect service request 2. DMA address encoder card 3. *Enables SRQ 120 coincidence gate
$\overline{120}$ = $\overline{(SSFF13)}$(SSFF14)$\overline{(SSFF15)}$(CR1)(PH5)	1. Detect select code output (MSD 1), DMA channel 1 2. DMA address encoder card 3. *Generates **SCM 1 output
200 = $\overline{(SSFF20)}\overline{(SSFF21)}\overline{(SSFF22)}$	1. Detect service request (LSD 0), DMA channel 2 2. DMA address encoder card 3. *Enables SRQ 10 and 20 coincidence gates
$\overline{200}$ = $\overline{(SSFF20)}\overline{(SSFF21)}\overline{(SSFF22)}$(CR2)(PH5)	1. Service select code output (LSD 0), DMA channel 2 2. DMA address encoder card 3. *Generates **SCL 0 output
201 = $\overline{(SSFF20)}\overline{(SSFF21)}$(SSFF22)	1. Detect service request (LSD 1), DMA channel 2 2. DMA address encoder card 3. *Enables SRQ 11 and 21 coincidence gates
$\overline{201}$ = $\overline{(SSFF20)}\overline{(SSFF21)}$(SSFF22)(CR2)(PH5)	1. Service select code output (LSD 1), DMA channel 2 2. DMA address encoder card 3. *Generates **SCL 1 output
202 = $\overline{(SSFF20)}$(SSFF21)$\overline{(SSFF22)}$	1. Detect service request (LSD 2), DMA channel 2 2. DMA address encoder card 3. *Enables SRQ 12 and 22 coincidence gates

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
$\overline{202} = \overline{(SSFF20)}(SSFF21)\overline{(SSFF22)}(CR2)(PH5)$	1. Service select code output (LSD 2), DMA channel 2 2. DMA address encoder card 3. *Generates **SCL 2 output
$203 = \overline{(SSFF20)}(SSFF21)(SSFF22)$	1. Detect service request (LSD 3), DMA channel 2 2. DMA address encoder card 3. *Enables SRQ 13 and 23 coincidence gates
$\overline{203} = \overline{(SSFF20)}(SSFF21)(SSFF22)(CR2)(PH5)$	1. Service select code output (LSD 3), DMA channel 2 2. DMA address encoder card 3. *Generates **SCL 3 output
$204 = (SSFF20)\overline{(SSFF21)}\overline{(SSFF22)}$	1. Detect service request (LSD 4), DMA channel 2 2. DMA address encoder card 3. *Enables SRQ 14 and 24 coincidence gates
$\overline{204} = (SSFF20)\overline{(SSFF21)}\overline{(SSFF22)}(CR2)(PH5)$	1. Service select code output (LSD 4), DMA channel 2 2. DMA address encoder card 3. *Generates **SCL 4 output
$205 = (SSFF20)\overline{(SSFF21)}(SSFF22)$	1. Detect service request (LSD 5), DMA channel 2 2. DMA address encoder 3. *Enables SRQ 15 and 25 coincidence gates
$\overline{205} = (SSFF20)\overline{(SSFF21)}(SSFF22)(CR2)(PH5)$	1. Service select code output (LSD 5), DMA channel 2 2. DMA address encoder 3. *Generates **SCL 5 output
$206 = (SSFF20)(SSFF21)\overline{(SSFF22)}$	1. Detect service request (LSD 6), DMA channel 2 2. DMA address encoder card 3. *Enables SRQ 16 and 26 coincidence gates
$\overline{206} = (SSFF20)(SSFF21)\overline{(SSFF22)}(CR2)(PH5)$	1. Service select code output (LSD 6), DMA channel 2 2. DMA address encoder card 3. *Generates **SCL 6 output
$207 = (SSFF20)(SSFF21)(SSFF22)$	1. Detect service request (LSD 7), DMA channel 2 2. DMA address encoder card 3. *Enables SRQ 17 and 27 coincidence gate
$\overline{207} = (SSFF20)(SSFF21)(SSFF22)(CR2)(PH5)$	1. Service select code output (LSD 7), DMA channel 2 2. DMA address encoder card 3. *Generates **SCL 7 output

* Internal card function; not routed through backplane wiring.
**DMA control function.

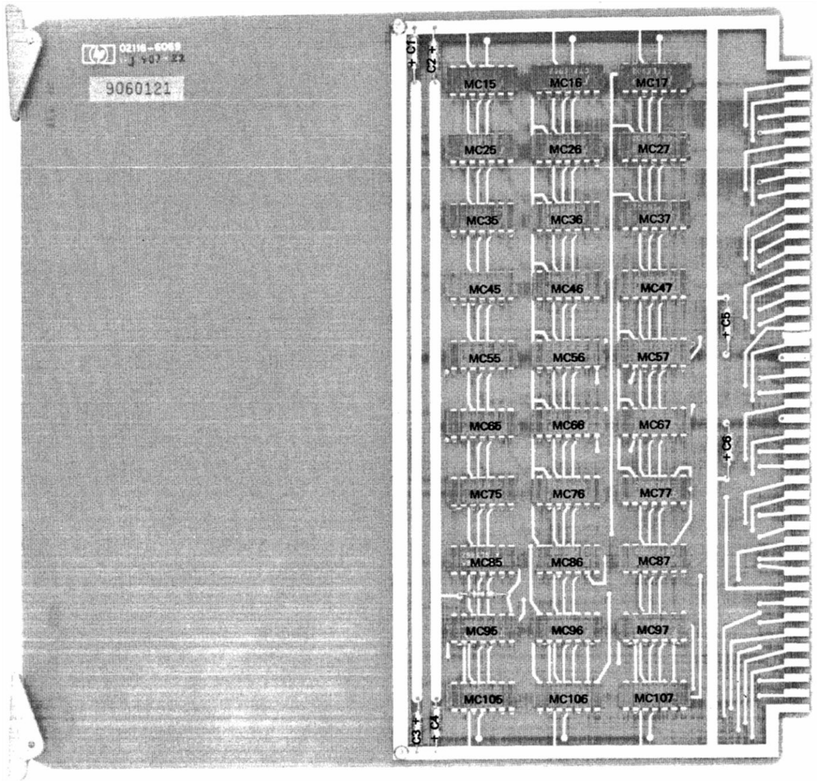
Table 5-2. DMA Option Input/Output Signals and Equations (Continued)

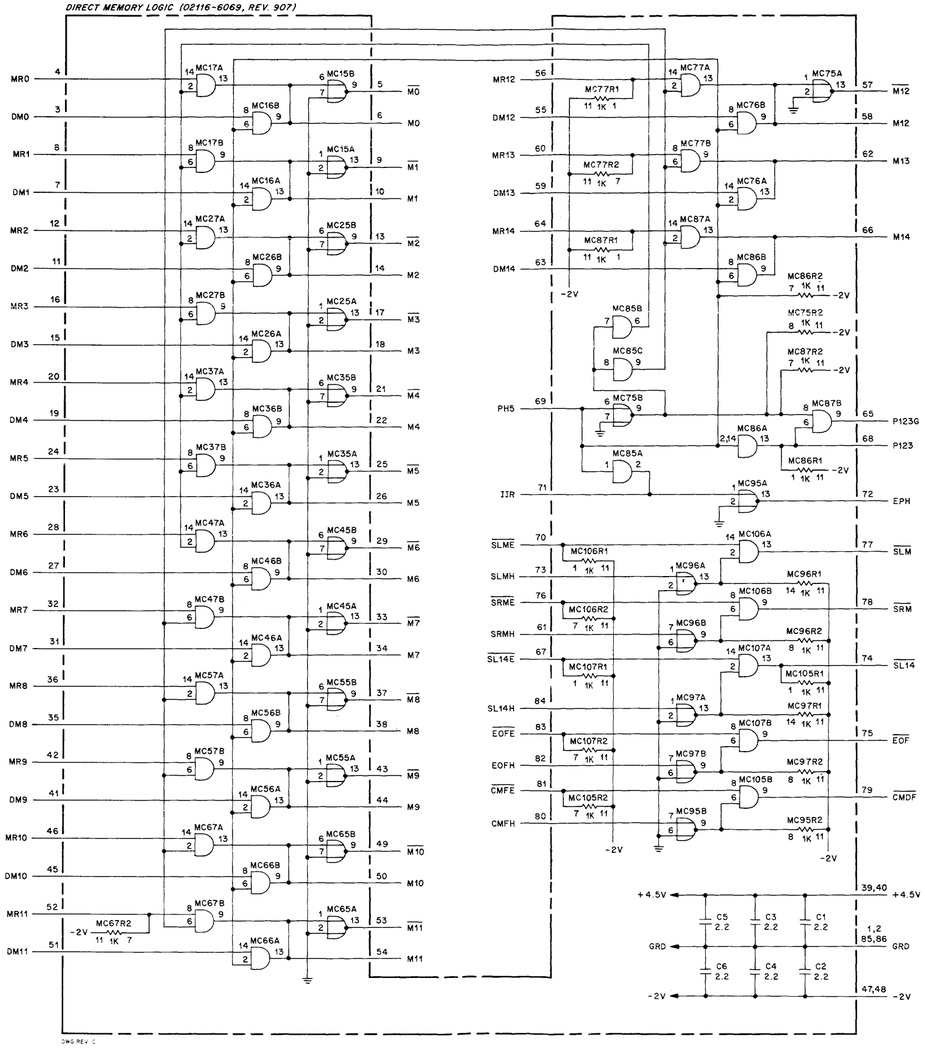
SIGNAL MNEMONIC AND EQUATION	1. DEFINITION 2. SOURCE 3. FUNCTION
210 = (SSFF23)(SSFF24)(SSFF25)	1. Detect service request (MSD 0), DMA channel 2 2. DMA address encoder card 3. *Enables SRQ 210 coincidence gate
$\overline{210}$ = (SSFF23)(SSFF24)(SSFF25)(CR2)(PH5)	1. Service select code output (MSD 0), DMA channel 2 2. DMA address encoder 3. *Generates **SCM 0 output
220 = (SSFF23)(SSFF24)(SSFF25)	1. Detect service request (MSD 1), DMA channel 2 2. DMA address encoder 3. *Enables SRQ 220 coincidence gate
$\overline{220}$ = (SSFF23)(SSFF24)(SSFF25)(CR2)(PH5)	1. Detect select code output (MSD 1), DMA channel 2 2. DMA address encoder 3. *Generates **SCM 1 output

* Internal card function; not routed through backplane wiring.
**DMA control function.

Table 5-3. DML Card (02116-6069) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C6	0180-0197	Capacitor, Fxd, Elect, 2.2µf, 10%, 20VDCW	28480	0180-0197
MC15,25,35,45,55,65,75,95,96,97	1820-0187	Integrated Circuit, CTL	07263	U6A985649X
MC16,17,26,27,36,37,46,47,56, 57,66,67,76,77,86,87,105, 106,107	1820-0186	Integrated Circuit, CTL	07263	U6A985249X
MC85	1820-0965	Integrated Circuit, CTL	07263	SL3462
R1	0698-3443	Resistor, Fxd, Met Flm, 287 ohms, 1%, 1/8w	28480	0698-3443



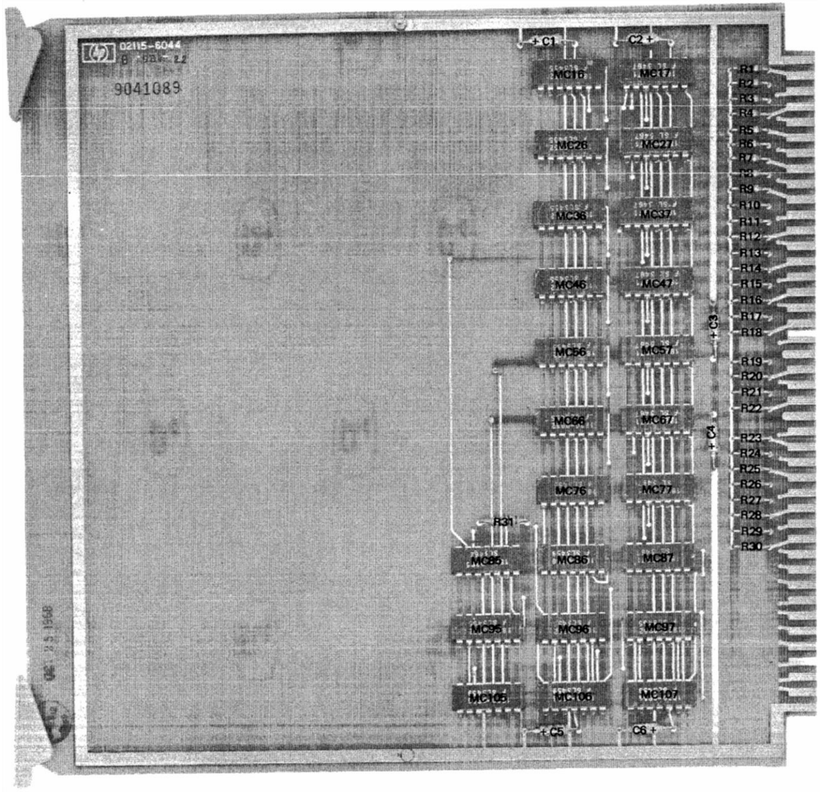


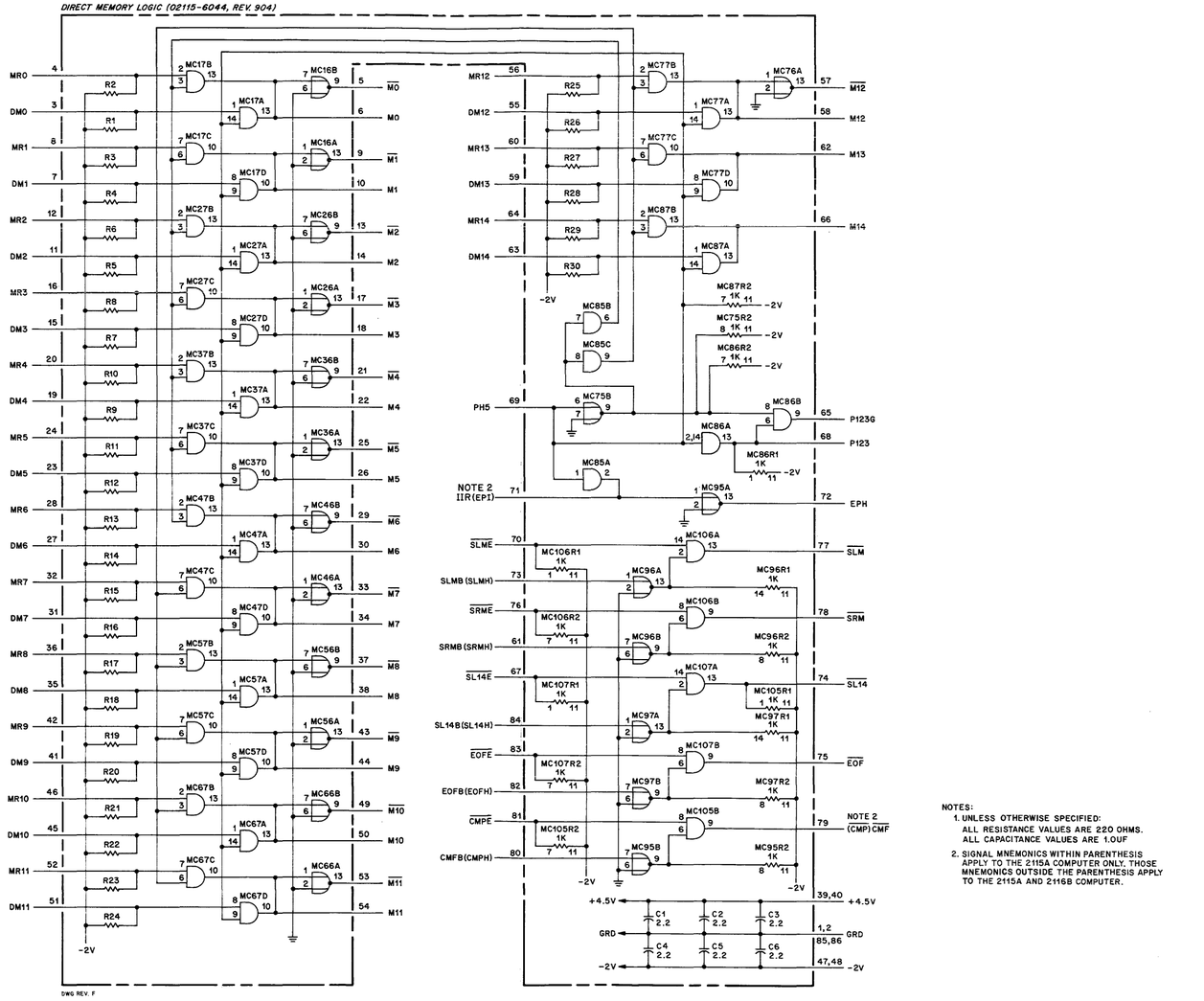
NOTE: UNLESS OTHERWISE SPECIFIED
ALL RESISTANCES ARE IN OHMS.
ALL CAPACITANCES ARE IN MICROFARADS.

Figure 5-1. DML Card (02116-6069) Logic Diagram and Parts Location Diagram

Table 5-4. DML Card (02115-6044) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C6	0180-0291	Capacitor, Elect, 2.2μf, 10%, 35VDCW	28480	0180-0291
MC16,26,36,46,56,66,76,95,96,97	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC17,27,37,47,57,67,77,97	1820-0971	Integrated Circuit, CTL	07263	SL3467
MC85	1820-0965	Integrated Circuit, CTL	07263	SL3462
MC86,105,106,107	1820-0956	Integrated Circuit, CTL	07263	SL3459
R1 thru R30	0683-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/4w	01121	CB2215
R31	0698-3443	Resistor, Met Flm, 287 ohms, 1%, 1/8w	28480	0698-3443



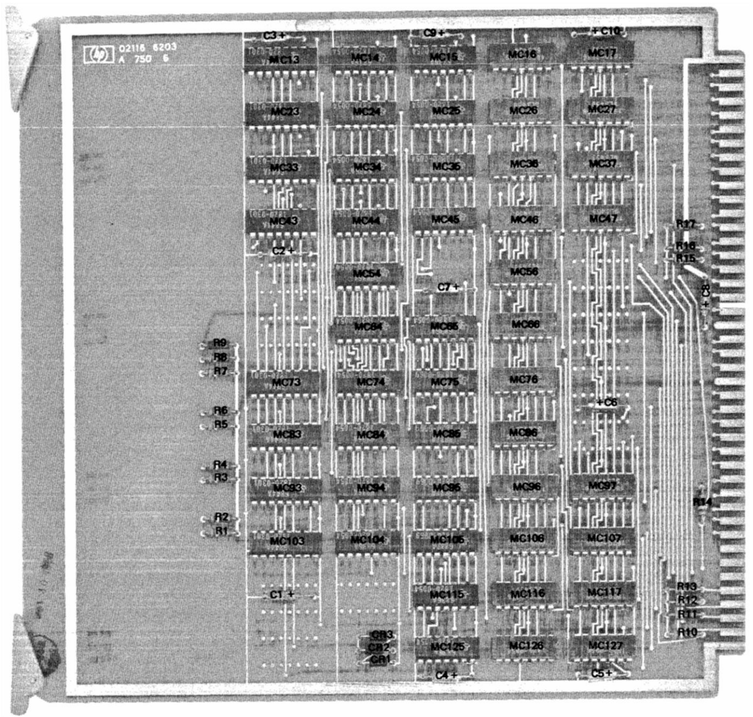


NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE 220 OHMS.
   ALL CAPACITANCE VALUES ARE 1.0UF
2. SIGNAL MNEMONICS WITHIN PARENTHESIS APPLY TO THE 2115A COMPUTER ONLY. THOSE MNEMONICS OUTSIDE THE PARENTHESIS APPLY TO THE 2115A AND 2116B COMPUTER.

Figure 5-2. DML Card (02115-6044) Logic Diagram and Parts Location Diagram

Table 5-5. DMA Character Packer Card (02116-6203) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C10	0180-0291	Capacitor, Fxd, Elect, 1.0µf, 10%, 35VDCW	28480	0180-0291
CR1,2,3	1901-0049	Diode, Si, 50piv	28480	1901-0049
MC13,23,33,43,73,83,93,103	1820-0301	Integrated Circuit, TTL	01295	SL3495
MC14,15,24,25,34,35,44,45,54, 64,65,74,84,94,104,115,125	1820-0054	Integrated Circuit, TTL	01295	SL7400N
MC16,17,26,27,36,37,46,47,56, 66,76,86,96,97,106,107,116, 117,126,127	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC75,85,95,105	1820-0069	Integrated Circuit, TTL	56289	USN7420A
R1 thru R8, R10 thru R17	0683-3915	Resistor, Fxd, Comp, 390 ohms, 5%, 1/4w	01121	CB3915
R9	0683-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/4w	01121	CB2215



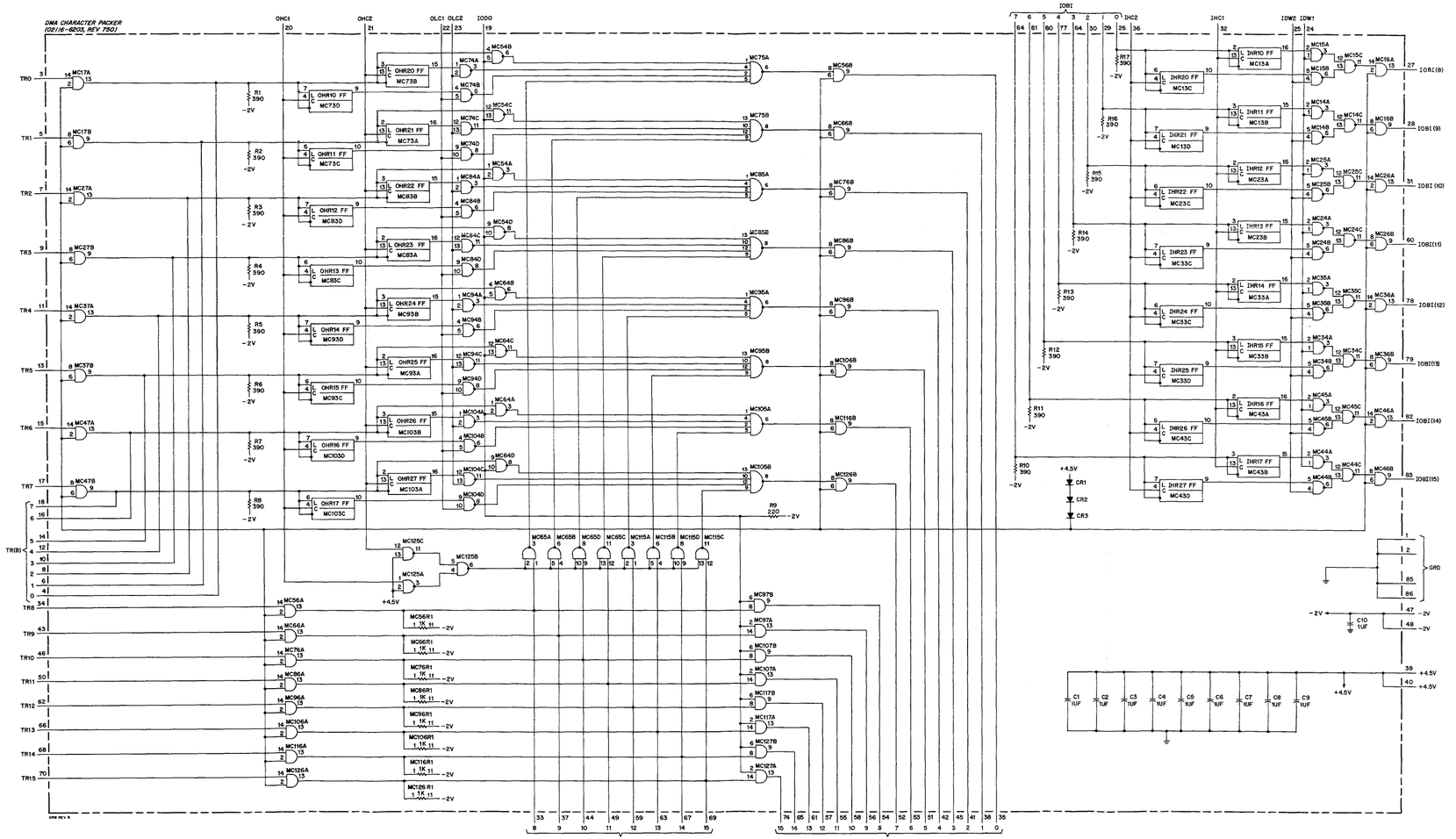
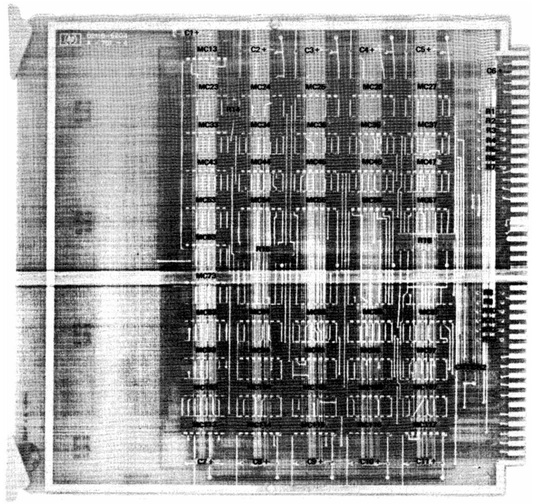


Figure 5-3. DMA Character Packer Card (02116-6203) Logic Diagram and Parts Location Diagram

Table 5-6. DMA Control Card (02116-6204) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C11	0180-0291	Capacitor, Fxd, Elect, 1.0µf, 10%, 35VDCW	28480	0180-0291
CR1,2	1901-0040	Diode, Si, 30mA,30VDCW	07263	FDG1088
MC13,26,27,35,36,44,46,47,54 84 thru 86,94,97,104, 114 thru 117	1820-0054	Integrated Circuit, TTL	01295	SN7400N
MC23	1820-0965	Integrated Circuit,CTL	07263	SL3462
MC24,33,43,53,63,73,83,93,103, 105,113	1820-0956	Integrated Circuit,CTL	07263	SL3459
MC25	1820-0077	Integrated Circuit, TTL	01295	SN7474N
MC34,45,96	1820-0069	Integrated Circuit, TTL	56289	USN7420A
MC37,55 thru 57,95,106,107	1820-0068	Integrated Circuit, TTL	56289	USN7410A
MC87	1820-0301	Integrated Circuit, TTL	01295	SL3495
R1 thru R13	0683-8215	Resistor, Fxd, Comp, 820 ohms, 5%, 1/4w	01121	CB8215
R14	0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4w	01121	CB4715
R15,16	1810-0020	Resistor, Network, Met Flm (7 resistors)	28480	1810-0020



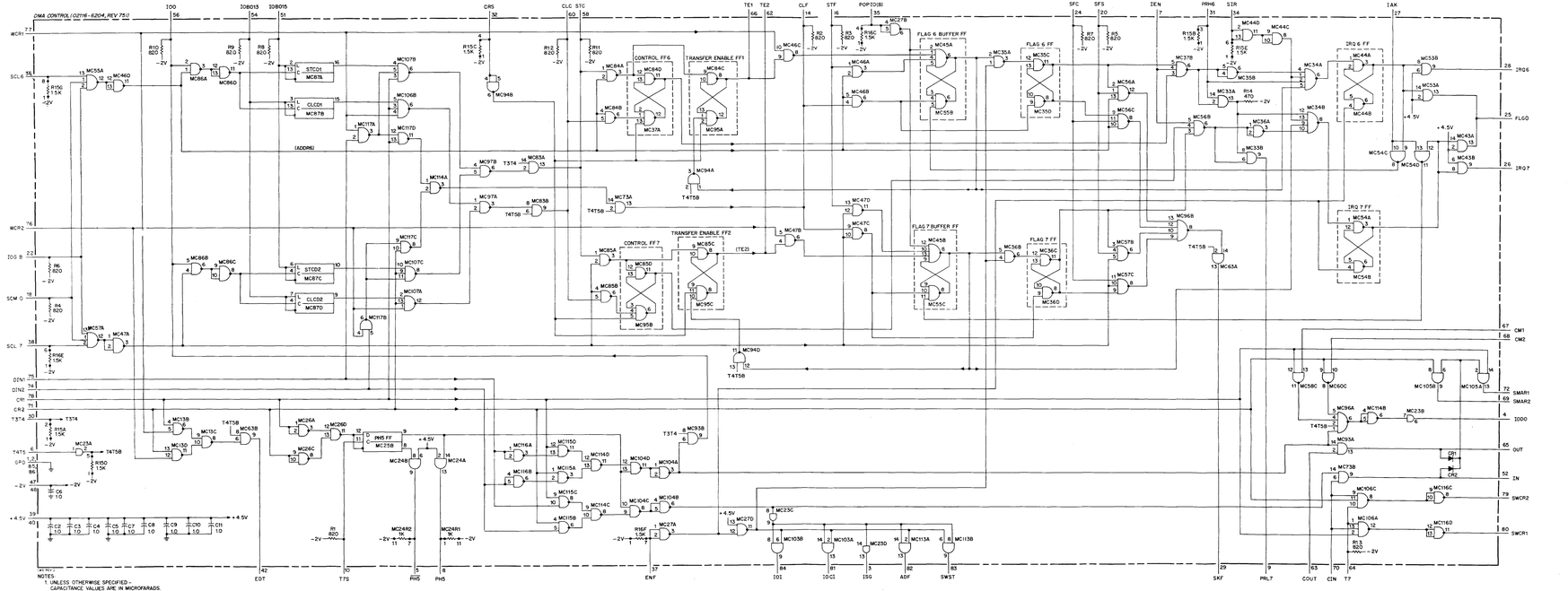
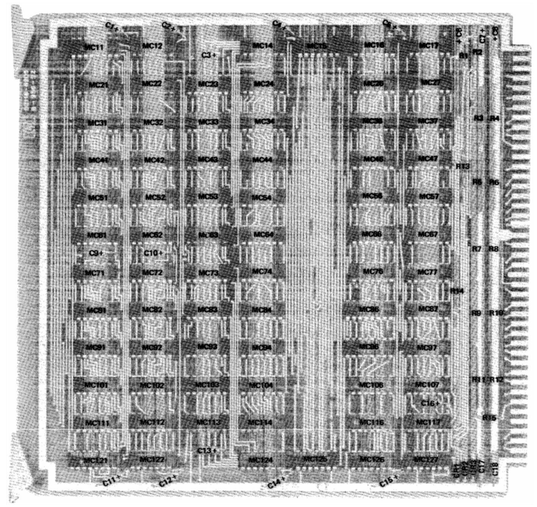


Figure 5-4. DMA Control Card (02116-6204) Logic Diagram and Parts Location Diagram

Table 5-7. DMA Address Encoder Card (02116-6205) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C18	0180-0291	Capacitor, Fxd, Elect, 1.0µf, 10%, 35VDCW	28480	0180-0291
CR1,2,3	1901-0049	Diode, Si, 50piv	28480	1901-0049
MC11,86,96,121	1820-0301	Integrated Circuit, TTL	01295	SL3495
MC12,22,76,112,122,117,127	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC14,24,114,124	1820-0070	Integrated Circuit, TTL	01295	SN7430A
MC15,17,21,23,27,33,34,37,43, 44,47,53,54,56,57,63,64,73,74, 83,84,93,94,103,104,107, 111,113,125,126	1820-0054	Integrated Circuit, TTL	01295	SN7400N
MC16,26,31,36,41,46,51,61,66, 71,81,91,101	1820-0069	Integrated Circuit, TTL	56289	USN7420A
MC32,42,52,62,72,77,82,87,92, 97,102	1820-0068	Integrated Circuit, TTL	56289	USN7410A
MC67	1820-0075	Integrated Circuit, TTL	01295	SN7473N
MC106	1820-0077	Integrated Circuit, TTL	01295	SN7474N
MC116	1820-0071	Integrated Circuit, TTL	01295	SN7440N
R1,2	0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4w	01121	CB4715
R3 thru R12	1810-0020	Resistor, Network, Met Film (7 resistors)	28480	1810-0020
R13,14	0683-1051	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4w	01121	CB1015
R15	0683-3015	Resistor, Comp, 300 ohms, 5%, 1/4w	01121	CB3015



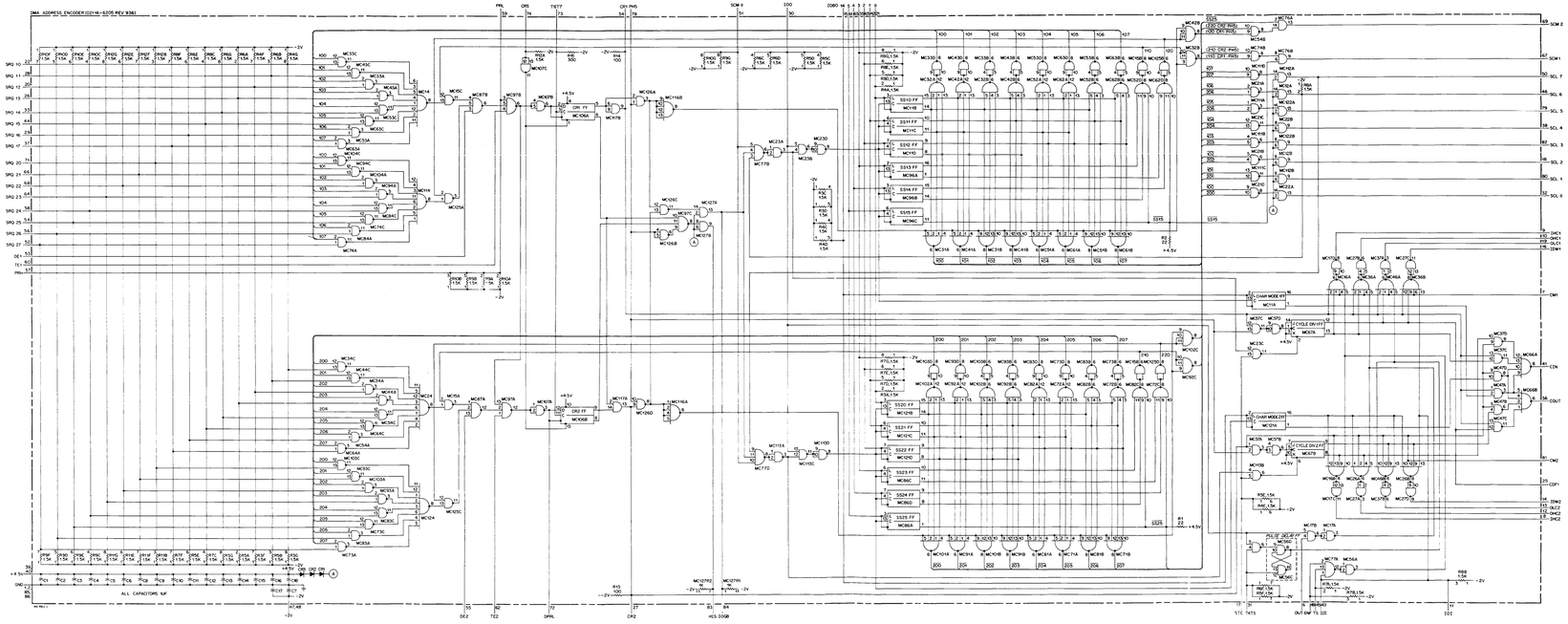
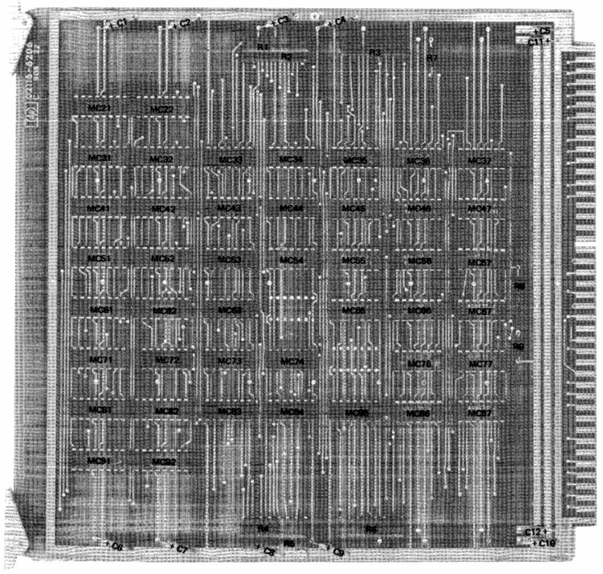
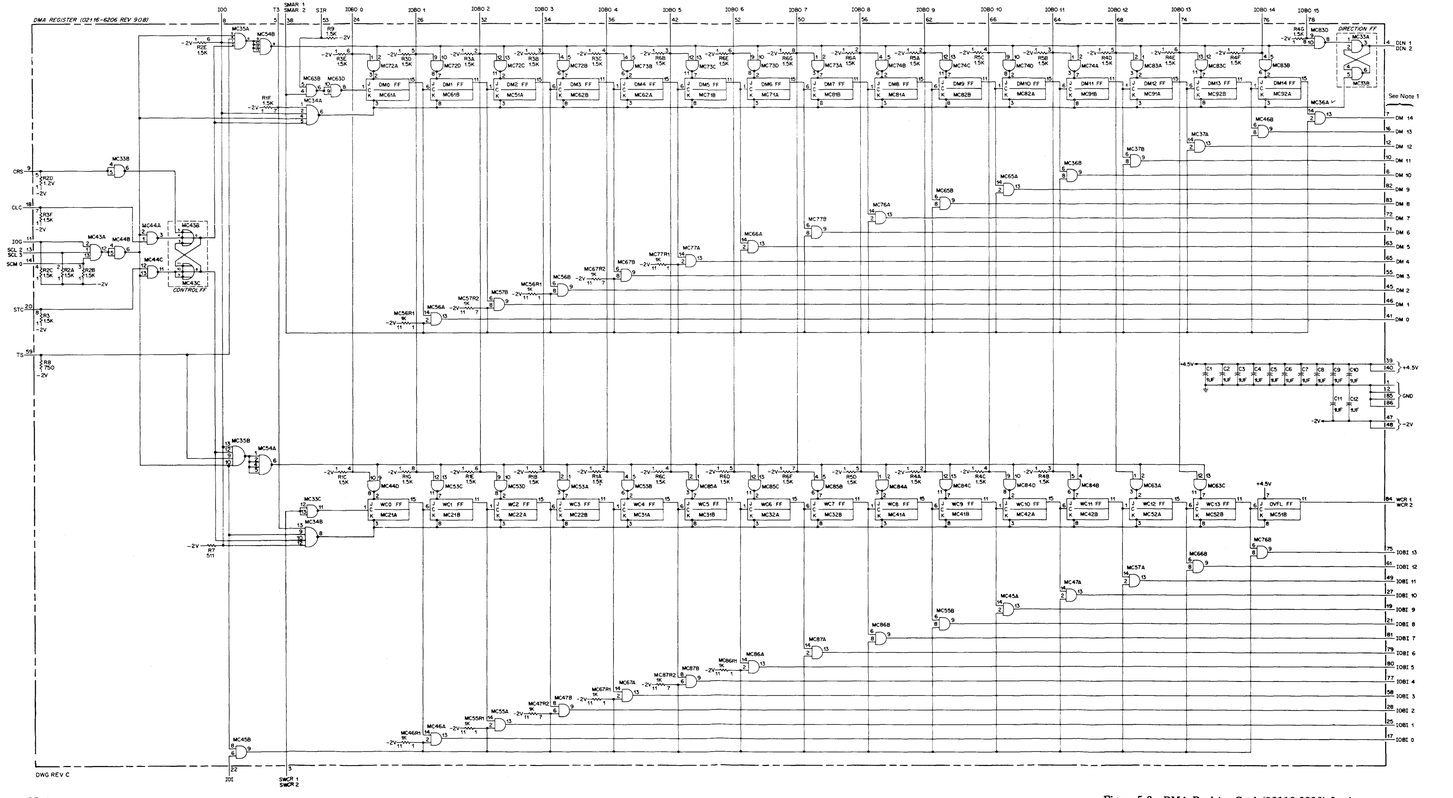


Figure 5-5. DMA Address Encoder Card (02116-6205)
Logic Diagram and Parts Location Diagram

Table 5-8. DMA Register Card (02116-6206) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C12	0180-0291	Capacitor, Fxd, Elect, 1.0µf,10%, 35VDCW	28480	0180-0291
MC21,22,31,32,41,42,51,52,61, 62,71,81,82,91,92	1820-0076	Integrated Circuit, TTL	01295	SN7475N
MC33,44,53,63,72,73,74,83,84,85	1820-0054	Integrated Circuit, TTL	01295	SN7400N
MC34,54	1820-0071	Integrated Circuit, TTL	01295	SN7440N
MC35	1820-0069	Integrated Circuit, TTL	56289	USN7420A
MC36,37,45,46,47,55,56,57,65, 66,67,76,77,86,87	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC43	1820-0068	Integrated Circuit, TTL	56289	USN7420A
R1 thru R6	1810-0020	Resistor, Network, Met Film (7 resistors)	28480	1810-0020
R7	0757-0416	Resistor, Fxd, Met Film, 511 ohms, 1%, 1/8w	28480	0757-0416
R8	0757-0420	Resistor, Fxd, Met Film, 750 ohms, 1%, 1/8w	28480	0757-0420
R9	0683-1525	Resistor, Fxd, Comp, 15K, 5%, 1/4w	01121	CB1525





Note:

1. For 2116C Computers, the mnemonic DM is changed to M.

Figure 5-6. DMA Register Card (02116-6206) Logic Diagram and Parts Location Diagram

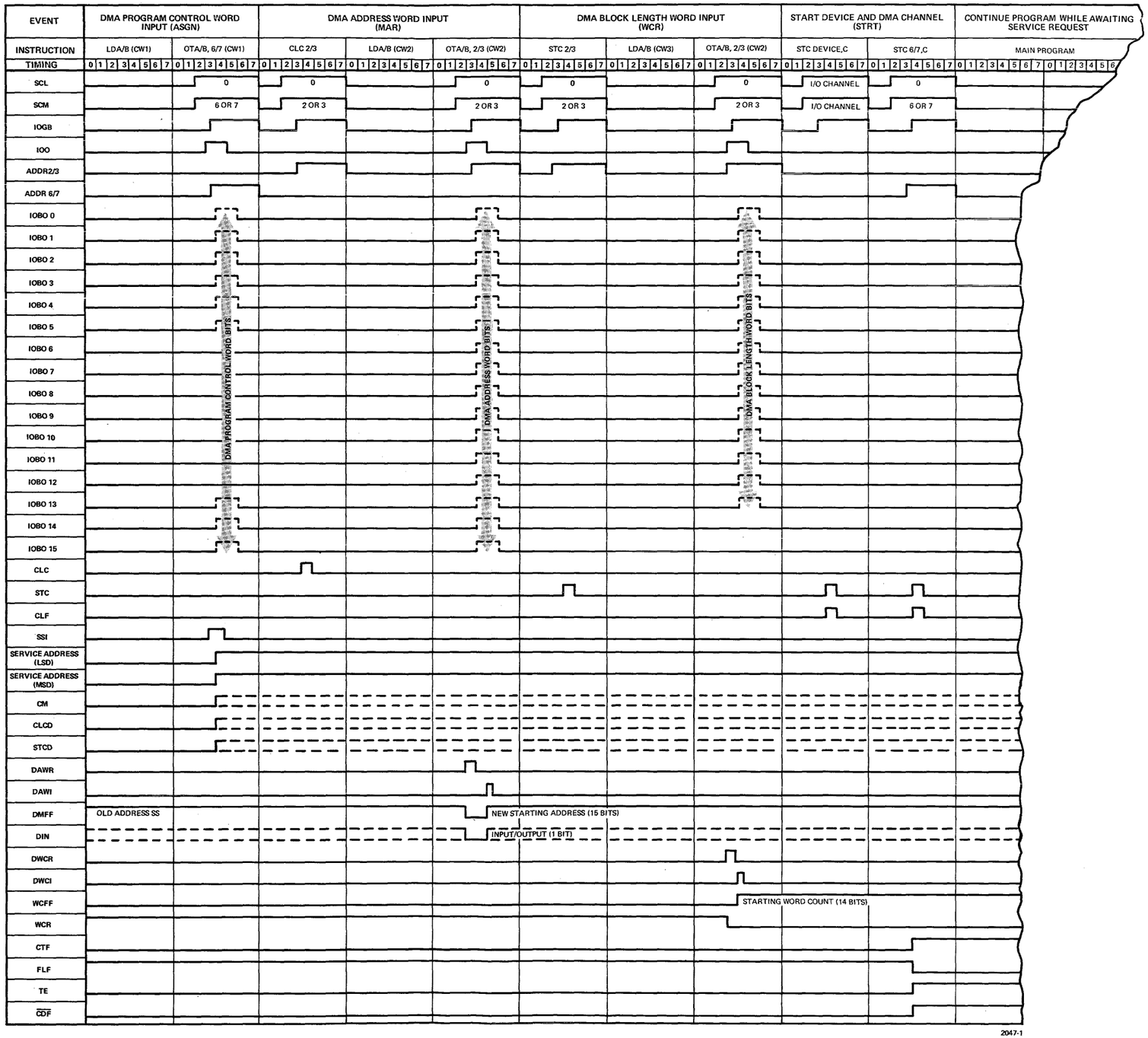


Figure 5-7. DMA Initialization Timing Diagram

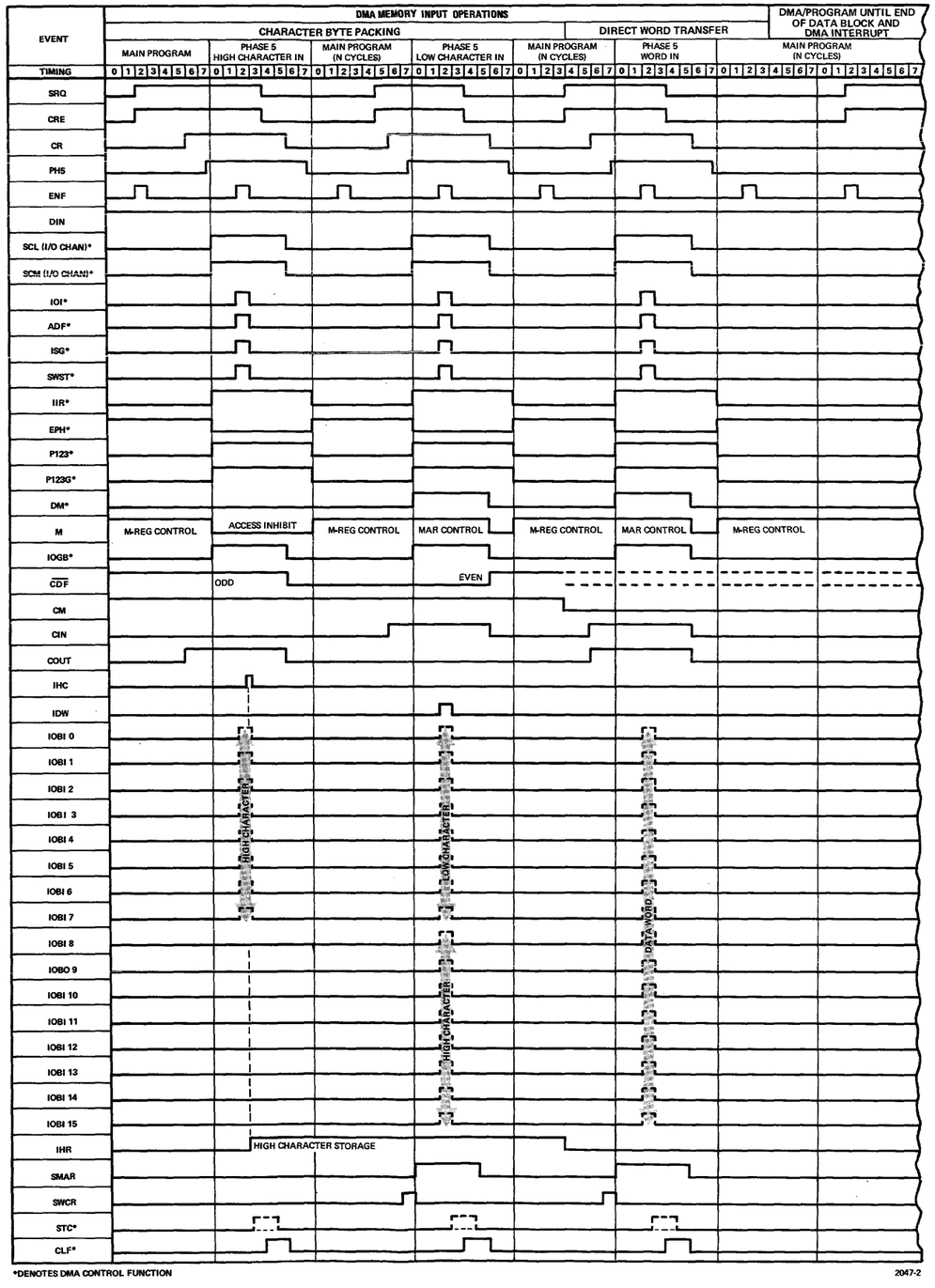


Figure 5-8. DMA Memory Input Operation Timing Diagram

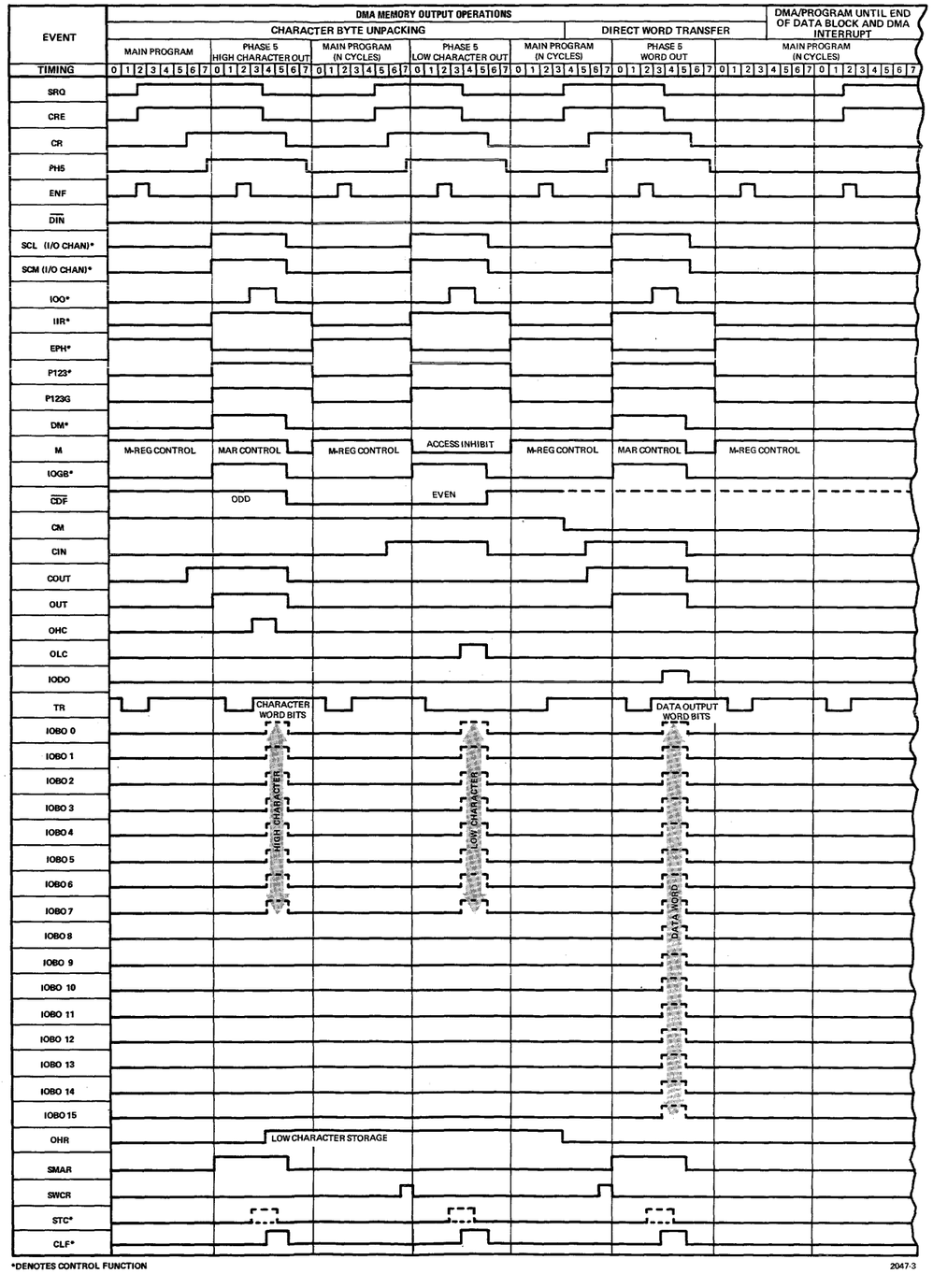
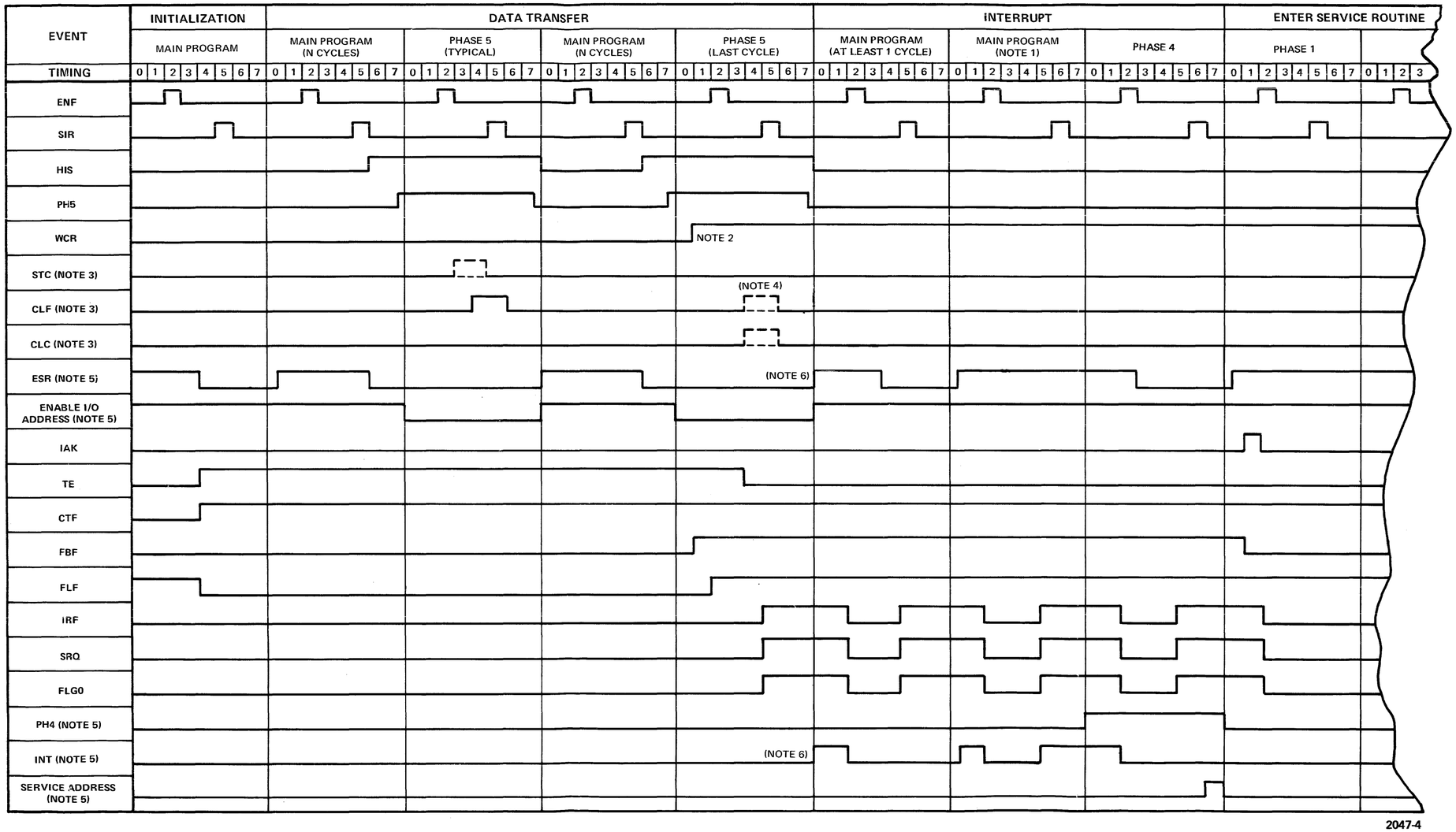


Figure 5-9. DMA Memory Output Operation Timing Diagram



NOTES:

1. Timing shown is based on the assumption that one of the conditions specified in note 6 below was present during the preceding machine cycle. Otherwise phase 4 would have set during this cycle rather than the next.
2. The exact time that the WRC signal goes high depends on inherent circuit delays. However, switching should not occur later than the end of T1.
3. DMA control functions.
4. Generated at this time during data output mode only.
5. Refer to volume III for detailed information concerning the generation and control of signal.
6. This signal assumes the low state during the occurrence of T7Ts if STF, CLF, STF, CLC, JMP,I, or JSB,I instructions are in progress, if phase 5 is set, or if a higher priority interrupt is being serviced. The low state prevents phase 4 from being set.

Figure 5-10. DMA Interrupt Timing Diagram

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering replacement parts for the DMA option. Table 6-1 lists parts in alphanumerical order of the HP stock numbers and lists the following information on each part:

a. Hewlett-Packard part number.

b. Description of the part. (Refer to table 6-2 for an explanation of abbreviations used in DESCRIPTION column.)

c. A five-digit code that corresponds to the manufacturer of the part. (Refer to table 6-3 for a listing of the manufacturers that correspond to the codes.)

d. Manufacturer's part number.

e. Total quantity of each part used in the DMA option.

6-3. Separate parts lists are provided for each printed-circuit card along with parts location diagrams for the cards. These parts lists are located in section V of this manual along with the respective schematic diagrams for the cards.

6-4. ORDERING INFORMATION.

6-5. To order replacement parts, address order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to list at the end of this manual for addresses.) Specify the following information for each part ordered:

a. Instrument model and serial number.

b. Hewlett-Packard stock number for each part.

c. Description of the part.

d. Circuit reference designation.

Table 6-1. Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0180-0197	Capacitor, Fxd, Elect, 2.2uf, 10%, 20VDCW	28480	0180-0197	12
0180-0291	Capacitor, Fxd, Elect, 1.0uf, 10%, 35VDCW	28480	0180-0291	41
0683-1051	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4w	01121	CB1015	2
0683-1525	Resistor, Fxd, Comp, 15k, 5%, 1/4w	01121	CB 1525	1
0683-2205	Resistor, Fxd, Comp, 22 ohms, 5%, 1/4w	01121	CB 2205	2
0683-2215	Resistor, Fxd, Comp, 220 ohms, 5%, 1/4w	01121	CB 2215	30
0683-3015	Resistor, Fxd, Comp, 300 ohms, 5%, 1/4w	01121	CB 3015	1
0683-3915	Resistor, Fxd, Comp, 390 ohms, 5%, 1/4w	01121	CB 3915	16
0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4w	01121	CB 4715	1
0683-8215	Resistor, Fxd, Comp, 820 ohms, 5%, 1/4w	01121	CB 8215	13
0698-3443	Resistor, Fxd, Met Flm, 287 ohms, 1%, 1/8w	28480	0698-3443	2
0757-0416	Resistor, Fxd, Met Flm, 511 ohms, 1%, 1/8w	28480	0757-0416	1
0757-0420	Resistor, Fxd, Met Flm, 750 ohms, 1%, 1/8w	28480	0757-0420	1
1810-0020	Resistor, Network, Met Flm (7 resistors)	28480	1810-0020	18
1820-0054	Integrated Circuit, TTL	01295	SN7400N	75
1820-0068	Integrated Circuit, TTL	56289	USN7410A	19
1820-0069	Integrated Circuit, TTL	56289	USN7420A	21
1820-0070	Integrated Circuit, TTL	01295	SN7430A	4
1820-0071	Integrated Circuit, TTL	01295	SN7440N	3
1820-0075	Integrated Circuit, TTL	01295	SN7473N	1
1820-0076	Integrated Circuit, TTL	01295	SN7475N	15
1820-0077	Integrated Circuit, TTL	01295	SN7474N	2
1820-0186	Integrated Circuit, CTL	07263	U6A985649X	19
1820-0187	Integrated Circuit, CTL	07263	U6A985249X	10
1820-0301	Integrated Circuit, TTL	01295	SL3495	13
1820-0952	Integrated Circuit, CTL	07263	SL3455	10
1820-0956	Integrated Circuit, CTL	07263	SL3459	57
1820-0965	Integrated Circuit, CTL	07263	SL3462	3
1820-0971	Integrated Circuit, CTL	07263	SL3467	8
1901-0040	Diode, Si, 30 mA, 30VDCW	07263	FDG1088	2
1901-0049	Diode, Silicon 50piv	28480	1901-0049	9
02115-6044	Direct Memory Logic Card	28480	02115-6044	1
02116-6203	DMA Character Packer Card	28480	02116-6203	1
02116-6204	DMA Control Card	28480	02116-6204	1
02116-6205	DMA Address Encoder Card	28480	02116-6205	1
02116-6206	DMA Register Card	28480	02116-6206	1
02116-6069	Direct Memory Logic Card	28480	02116-6069	1

Table 6-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A = assembly	J = receptacle connector	TB = terminal board
B = motor	K = relay	TP = test point
BT = battery	L = inductor	U = integrated circuit
C = capacitor	M = meter	V = vacuum tube, neon bulb, photocell, etc.
CP = coupler	MC = microcircuit	
CR = diode	P = plug connector	VR = voltage regulator
DL = delay line	Q = transistor	W = cable, jumper
DS = device signaling (lamp)	R = resistor	X = socket
E = misc hardware	RT = thermistor	Y = crystal
F = fuse	S = switch	Z = tuned cavity, network
FL = filter	T = transformer	

ABBREVIATIONS

A = amperes	IMPG = impregnated	P/O = part of
AC = alternating current	IN. = inch, inches	POLY = polystyrene
AFC = automatic frequency control	INCD = incandescent	PORC = porcelain
ALUM = aluminum	INCL = include(s)	POS = position(s)
AL-ELECT = aluminum electrolytic	INS = insulation(ed)	POT = potentiometer
ASSY = assembly	INT = internal	PP = peak-to-peak
	I/O = input/output	PT = point
BFO = beat frequency oscillator		PWV = peak working voltage
BE CU = beryllium copper	K = kilo = 1000	
BH = binder head		R = resistor
BP = bandpass	LH = left hand	RECT = rectifier
BRS = brass	LIN = linear taper	RF = radio frequency
BWO = backward wave oscillator	LK WASH = lock washer	RH = round head or right hand
	LOG = logarithmic taper	RMO = rack mount only
C = capacitor	LPF = low pass filter	RMS = root-mean square
CCW = counterclockwise		RWV = reverse working voltage
CER = ceramic	M = milli = 10^{-3}	
CMO = cabinet mount only	MEG = mega = 10^{6}	S-B = slow-blow
COEF = coefficient	MET FLM = metal film	SCR = screw
COM = common	MET OX = metal oxide	SE = selenium
COMP = composition	MFR = manufacturer	SECT = section(s)
COMPL = complete	MHz = megahertz	SEMICON = semiconductor
CONN = connector	MINAT = miniature	SI = silicon
CP = cadmium plate	MOM = momentary	SIL = silver
CRT = cathode-ray tube	MTG = mounting	SL = slide
CTL = capacitor-transistor logic	MY = Mylar	SPDT = single-pole, double-throw
CW = clockwise		SPG = spring
	N = nano (10^{-9})	SPL = special
DC = direct current	N/C = normally closed	SPST = single-pole, single-throw
DEPC = deposited carbon	NE = neon	SR = split ring
DPDT = double-pole, double-throw	NI PL = nickel plate	SST = stainless steel
DPST = double-pole, single-throw	NO. = number	STL = steel
DR = drive	N/O = normally open	
	NPN = negative-positive-negative	TA = tantalum
ELECT = electrolytic		TD = time delay
ENCAP = encapsulated	NPO = negative positive zero (zero temperature coefficient)	TGL = toggle
EXT = external		THD = thread
	NRFR = not recommended for field replacement	TI = titanium
F = farads		TOL = tolerance
FH = flat head	NSR = not separately replaceable	TRIM = trimmer
FIL H = fillister head		TTL = transistor-transistor logic
FXD = fixed	OBD = order by description	TWT = traveling wave tube
	OD = outer diameter	
G = giga (10^{9})	OH = oval head	U (μ) = micro = 10^{-6}
GE = germanium	OX = oxide	
GL = glass		VAR = variable
GND/GRD = ground(ed)	P = peak	VDCW = direct current working volts
	PC = printed circuit	
H = henries	PF = picofarads = 10^{-12} farads	W/ = with
HDW = hardware	PH = Phillips head	W = watts
HEX = hexagonal	PH BRZ = phosphor bronze	WIV = working inverse voltage
HG = mercury	PHL = Phillips	WW = wirewound
HR = hour(s)	PIV = peak inverse voltage	W/O = without
HZ = hertz	PNP = positive-negative-positive	
ID = inner diameter		
IF = intermediate frequency		

Table 6-3. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 (Name to Code) and H4-2 (Code to Name) and their latest supplements. The date of revision and the date of the supplements used appear at the bottom of each page. Alphabetical codes have been arbitrarily assigned to suppliers not appearing in the H4 Handbooks.

Code No.	Manufacturer	Address
00000	U.S.A. Common	Any supplier of U.S.
00136	McCoy Electronics	Mount Holly Springs, Pa.
00213	Sage Electronics Corp.	Rochester, N.Y.
00287	Cemco Inc.	Danielson, Conn.
00334	Humidial	Colton, Calif.
00348	Microtron Co., Inc.	Valley Stream, N.Y.
00373	Garlock Inc.	Cherry Hill, N.J.
00656	Aerovox Corp.	New Bedford, Mass.
00779	Amp. Inc.	Harrisburg, Pa.
00781	Aircraft Radio Corp.	Boonton, N.J.
00815	Northern Engineering Laboratories, Inc.	Burlington, Wis.
00853	Sangamo Electric Co., Pickens Div.	Pickens, S.C.
00866	Goe Engineering Co.	City of Industry, Cal.
00891	Carl E. Holmes Corp.	Los Angeles, Calif.
00929	Microlab Inc.	Livingston, N.J.
01002	General Electric Co., Capacitor Dept.	Hudson Falls, N.Y.
01009	Alden Products Co.	Brockton, Mass.
01121	Allen Bradley Co.	Milwaukee, Wis.
01255	Litton Industries, Inc.	Beverly Hills, Calif.
01281	TRW Semiconductors, Inc.	Lawndale, Calif.
01295	Texas Instruments, Inc., Transistor Products Div.	Dallas, Texas
01349	The Alliance Mfg. Co.	Alliance, Ohio
01589	Pacific Relays, Inc.	Van Nuys, Calif.
01670	Gudebrod Bros. Silk Co.	New York, N.Y.
01930	Amerock Corp.	Rockford, Ill.
01961	Pulse Engineering Co.	Santa Clara, Calif.
02114	Ferroxcube Corp. of America	Saugerties, N.Y.
02116	Wheelock Signals, Inc.	Long Branch, N.J.
02286	Cole Rubber and Plastics Inc.	Sunnyvale, Calif.
02660	Amphenol-Borg Electronics Corp.	Broadview, Ill.
02735	Radio Corp. of America, Semiconductor and Materials Div.	Somerville, N.J.
02771	Vocaline Co. of America, Inc.	Old Saybrook, Conn.
02777	Hopkins Engineering Co.	San Fernando, Calif.
02875	Hudson Tool & Die Co.	Newark, N.J.
03508	G.E. Semiconductor Prod. Dept.	Syracuse, N.Y.
03705	Apex Machine & Tool Co.	Dayton, Ohio
03797	Eldema Corp.	Compton, Calif.
03818	Parker Seal Co.	Los Angeles, Calif.
03877	Transitron Electric Corp.	Wakefield, Mass.
03888	Pyrofilm Resistor Co., Inc.	Cedar Knolls, N.J.
03954	Singer Co., Diehl Div. Finderne Plant	Sumerville, N.J.
04009	Arrow, Hart and Hegeman Elect. Co.	Hartford, Conn.
04013	Taurus Corp.	Lambertville, N.J.
04062	Arco Electronic Inc.	Great Neck, N.Y.
04222	Hi-Q Division of Aerovox	Myrtle Beach, S.C.
04354	Precision Paper Tube Co.	Wheeling, Ill.
04404	Dymec Division of Hewlett-Packard Co.	Palo Alto, Calif.
04651	Sylvania Electric Products, Microwave Device Div.	Mountain View, Calif.
04673	Dakota Engr. Inc.	Culver City, Calif.
04713	Motorola, Inc., Semiconductor Prod. Div.	Phoenix, Arizona
04732	Filtron Co., Inc. Western Div.	Culver City, Calif.
04773	Automatic Electric Co.	Northlake, Ill.
04796	Sequoia Wire Co.	Redwood City, Calif.
04811	Precision Coil Spring Co.	El Monte, Calif.
04870	P.M. Motor Company	Westchester, Ill.
04919	Component Mfg. Service Co.	W. Bridgewater, Mass.
05006	Twentieth Century Plastics, Inc.	Los Angeles, Calif.
05245	Components Corp.	Chicago, Ill.
05277	Westinghouse Electric Corp. Semi-Conductor Dept.	Youngwood, Pa.
05347	Ultronix, Inc.	San Mateo, Calif.
05397	Union Carbide Corp., Elect. Div.	New York, N.Y.
05574	Viking Ind. Inc.	Canoga Park, Calif.
05593	Icore Electro-Plastics Inc.	Sunnyvale, Calif.
05616	Cosmo Plastic (c o Electrical Spec. Co.)	Cleveland, Ohio
05624	Barber Colman Co.	Rockford, Ill.
05728	Tiffen Optical Co.	Roslyn Heights, Long Island, N.Y.
05729	Metro-Tel Corp.	Westbury, N.Y.
05783	Stewart Engineering Co.	Santa Cruz, Calif.
05820	Wakefield Engineering Inc.	Wakefield, Mass.
06004	Bassick Co., Div. of Stewart Warner Corp.	Bridgeport, Conn.
06090	Raychem Corp.	Redwood City, Calif.
06175	Bausch and Lomb Optical Co.	Rochester, N.Y.
06402	E.T.A. Products Co. of America	Chicago, Ill.
06540	Amatom Electronic Hardware Co., Inc.	New Rochelle, N.Y.
06555	Beede Electrical Instrument Co., Inc.	Penacook, N.H.
06666	General Devices Co., Inc.	Indianapolis, Ind.
06751	Components Inc., Ariz. Div.	Phoenix, Ariz.
06812	Torrington Mfg. Co., West Div.	Van Nuys, Calif.
06980	Varian Assoc. Eimac Div.	San Carlos, Calif.
07088	Kelvin Electric Co.	Van Nuys, Calif.
07126	Digitran Co.	Pasadena, Calif.
07137	Transistor Electronics Corp.	Minneapolis, Minn.
07138	Westinghouse Electric Corp. Electronic Tube Div.	Elmira, N.Y.
07149	Filmohm Corp.	New York, N.Y.
07233	Cinch-Graphik Co.	City of Industry, Calif.
07256	Silicon Transistor Corp.	Carle Place, N.Y.
07261	Avnet Corp.	Culver City, Calif.
07263	Fairchild Camera & Inst. Corp. Semiconductor Div.	Mountain View, Calif.
07322	Minnesota Rubber Co.	Minneapolis, Minn.
07387	Birtcher Corp., The	Monterey Park, Calif.
07397	Sylvania Elect. Prod. Inc., Mt. View Operations	Mountain View, Calif.
07700	Technical Wire Products Inc.	Cranford, N.J.
07829	Bodine Elect. Co.	Chicago, Ill.
07910	Continental Device Corp.	Hawthorne, Calif.
07933	Raytheon Mfg. Co., Semiconductor Div.	Mountain View, Calif.
07980	Hewlett-Packard Co., Boonton Radio Div.	Rockaway, N.J.
08145	U.S. Engineering Co.	Los Angeles, Calif.
08289	Blinn, Delbert Co.	Pomona, Calif.
08358	Burgess Battery Co.	Niagara Falls, Ontario, Canada
08524	Deutsch Fastener Corp.	Los Angeles, Calif.
08664	Bristol Co., The	Waterbury, Conn.
08717	Sloan Company	Sun Valley, Calif.
08718	ITT Cannon Electric Inc., Phoenix Div.	Phoenix, Arizona
08727	National Radio Lab. Inc.	Paramus, N.J.
08792	CBS Electronics Semiconductor Operations, Div of C.B.S. Inc.	Lowell, Mass.
08806	General Electric Co. Miniat. Lamp Dept.	Cleveland, Ohio
08984	Mel-Rain	Indianapolis, Ind.
09026	Babcock Relays Div.	Costa Mesa, Calif.
09134	Texas Capacitor Co.	Houston, Texas
09145	Tech. Ind. Inc. Atohm Elect.	Burbank, Calif.
09250	Electro Assemblies, Inc.	Chicago, Ill.
09353	C & K Components Inc.	Newton, Mass.
09569	Mallory Battery Co. of Canada, Ltd.	Toronto, Ontario, Canada
09922	Burndy Corp.	Norwalk, Conn.
10214	General Transistor Western Corp.	Los Angeles, Calif.
10411	Ti-Tal, Inc.	Berkeley, Calif.
10646	Carborundum Co.	Niagara Falls, N.Y.
11236	CTS of Berne, Inc.	Berne, Ind.
11237	Chicago Telephone of California, Inc.	So. Pasadena, Calif.
11242	Bay State Electronics Corp.	Waltham, Mass.
11312	Teledyne Inc., Microwave Div.	Palo Alto, Calif.
11314	National Seal	Downey, Calif.
11453	Precision Connector Corp.	Jamaica, N.Y.
11534	Duncan Electronics Inc.	Costa Mesa, Calif.
11711	General Instrument Corp., Semiconductor Div., Products Group	Newark, N.J.
11717	Imperial Electronic, Inc.	Buena Park, Calif.
11870	Melabs, Inc.	Palo Alto, Calif.
12040	National Semiconductor	Danbury, Conn.
12136	Philadelphia Handle Co.	Camden, N.J.
12361	Grove Mfg. Co., Inc.	Shady Grove, Pa.
12574	Gulton Ind. Inc. Data System Div.	Albuquerque, N.M.
12697	Clarostat Mfg. Co.	Dover, N.H.
12728	Elmar Filter Corp.	W. Haven, Conn.
12859	Nippon Electric Co., Ltd.	Tokyo, Japan
12881	Metex Electronics Corp.	Clark, N.J.
12930	Delta Semiconductor Inc.	Newport Beach, Calif.
12954	Dickson Electronics Corp.	Scottsdale, Arizona
13103	Thermolloy	Dallas, Texas
13396	Telefunken (GmbH)	Hanover, Germany
13835	Midland-Wright Div. of Pacific Industries, Inc.	Kansas City, Kansas
14099	Sem-Tech	Newbury Park, Calif.
14193	Calif. Resistor Corp.	Santa Monica, Calif.
14298	American Components, Inc.	Conshohocken, Pa.
14433	ITT Semiconductor, A Div. of Int. Telephone & Telegraph Corp.	West Palm Beach, Fla.
14493	Hewlett-Packard Company	Loveland, Colo.
14655	Cornell Dublier Electric Corp.	Newark, N.J.
14674	Corning Glass Works	Corning, N.Y.
14752	Electro Cube Inc.	San Gabriel, Calif.
14960	Williams Mfg. Co.	San Jose, Calif.
15203	Webster Electronics Co.	New York, N.Y.
15287	Scionics Corp.	Northridge, Calif.
15291	Adjustable Bushing Co.	N. Hollywood, Calif.
15558	Micron Electronics	Garden City, Long Island, N.Y.
15566	Amprobe Inst. Corp.	Lynbrook, N.Y.
15631	Cabletronics	Costa Mesa, Calif.
15772	Twentieth Century Coil Spring Co.	Santa Clara, Calif.
15801	Fenwal Elect. Inc.	Framingham, Mass.
15818	Amelco Inc.	Mt. View, Calif.
16037	Spruce Pine Mica Co.	Spruce Pine, N.C.
16179	Omni-Spectra Inc.	Farmington, Mich.
16352	Computer Diode Corp.	Lodi, N.J.
16585	Boots Aircraft Nut Corp.	Pasadena, Calif.
16688	Ideal Prec. Meter Co., Inc. De Jur Meter Div.	Brooklyn, N.Y.
16758	Delco Radio Div. of G.M. Corp.	Kokoma, Ind.
17109	Thermonetics Inc.	Canoga Park, Calif.
17474	Tranex Company	Mountain View, Calif.
17554	Components Inc.	Biddeford, Ma.
17675	Hamlin Metal Products Corp.	Akron, Ohio
17745	Angstrohm Prec. Inc.	No. Hollywood, Calif.

00015-47
Revised: April, 1969

From: FSC. Handbook Supplements

Table 6-3. Code List of Manufacturers (Continued)

Code No.	Manufacturer	Address
17870	McGraw-Edison Co.	Manchester, N.H.
18042	Power Design Pacific Inc.	Palo Alto, Calif.
18083	Clevite Corp., Semiconductor Div.	Palo Alto, Calif.
18324	Signetics Corp.	Sunnyvale, Calif.
18476	Ty-Car Mfg. Co., Inc.	Holliston, Mass.
18486	TRW Elect. Comp. Div.	Des Plaines, Ill.
18583	Curtis Instrument, Inc.	Mt. Kisco, N.Y.
18612	Vishay Instruments Inc.	Malvern, Pa.
18873	E.I. DuPont and Co., Inc.	Wilmington, Del.
18911	Durant Mfg. Co.	Milwaukee, Wis.
19315	The Bendix Corp., Navigation & Control Div.	Teterboro, N.J.
19500	Thomas A. Edison Industries, Div. of McGraw-Edison Co.	West Orange, N.J.
19589	Concoa	Baldwin Park, Calif.
19644	LRC Electronics	Horseheads, N.Y.
19701	Electra Mfg. Co.	Independence, Kansas
20183	General Atronics Corp.	Philadelphia, Pa.
21226	Executone, Inc.	Long Island City, N.Y.
21335	Fafnir Bearing Co., The	New Britain, Conn.
21520	Fansteel Metallurgical Corp.	N. Chicago, Ill.
23042	Texscan Corp.	Indianapolis, Ind.
23783	British Radio Electronics Ltd.	Washington, D.C.
24455	G.E. Lamp Division	Nela Park, Cleveland, Ohio
24655	General Radio Co.	West Concord, Mass.
24681	Memcor Inc., Comp. Div.	Huntington, Ind.
24796	Parelco Inc.	San Juan Capistrano, Calif.
26365	Gries Reproducer Corp.	New Rochelle, N.Y.
26462	Grobet File Co. of America, Inc.	Carlstadt, N.J.
26851	Compac Hollister Co.	Hollister, Calif.
26992	Hamilton Watch Co.	Lancaster, Pa.
27251	Specialities Mfg. Co., Inc.	Stratford, Conn.
28480	Hewlett-Packard Co.	Palo Alto, Calif.
28520	Heyman Mfg. Co.	Kenilworth, N.J.
30817	Instrument Specialties Co., Inc.	Little Falls, N.J.
33173	G.E. Receiving Tube Dept.	Owensboro, Ky.
35434	Lectrohm Inc.	Chicago, Ill.
36196	Stanwyck Coil Products Ltd.	Hawkesbury, Ontario, Canada
36287	Cunningham, W.H. & Hill, Ltd.	Toronto Ontario, Canada
37942	P.R. Mallory & Co. Inc.	Indianapolis, Ind.
39543	Mechanical Industries Prod. Co.	Akron, Ohio
40920	Miniature Precision Bearings, Inc.	Keene, N.H.
42190	Muter Co.	Chicago, Ill.
43990	C.A. Norgren Co.	Englewood, Colo.
44655	Ohmite Mfg. Co.	Skokie, Ill.
46384	Penn Eng. & Mfg. Corp.	Doylestown, Pa.
47904	Polaroid Corp.	Cambridge, Mass.
48620	Precision Thermometer & Inst. Co.	Southampton, Pa.
49956	Microwave & Power Tube Div.	Waltham, Mass.
52090	Rowan Controller Co.	Westminster, Md.
52983	Sanborn Company	Waltham, Mass.
54294	Shallcross Mfg. Co.	Selma, N.C.
55026	Simpson Electric Co.	Chicago, Ill.
55933	Sonotone Corp.	Elmsford, N.Y.
55938	Raytheon Co. Commercial Apparatus & Systems Div.	So. Norwalk, Conn.
56137	Spaulding Fibre Co., Inc.	Tonawanda, N.Y.
56289	Sprague Electric Co.	North Adams, Mass.
59446	Telex Corp.	Tulsa, Okla.
59730	Thomas & Betts Co.	Elizabeth, N.J.
60741	Triplett Electrical Inst. Co.	Bluffton, Ohio
61775	Union Switch and Signal, Div. of Westinghouse Air Brake Co.	Pittsburgh, Pa.
62119	Universal Electric Co.	Owosso, Mich.
63743	Ward-Leonard Electric Co.	Mt. Vernon, N.Y.
64959	Western Electric Co., Inc.	New York, N.Y.
65092	Weston Inst. Inc. Weston-Newark	Newark, N.J.
66295	Wittek Mfg. Co.	Chicago, Ill.
66346	Minnesota Mining & Mfg. Co. Revere Mincom Div.	St. Paul, Minn.
70276	Allen Mfg. Co.	Hartford, Conn.
70309	Allied Control	New York, N.Y.
70318	Allmetal Screw Product Co., Inc.	Garden City, N.Y.
70417	Amplex, Div. of Chrysler Corp.	Detroit, Mich.
70485	Atlantic India Rubber Works, Inc.	Chicago, Ill.
70563	Amperite Co., Inc.	Union City, N.J.
70674	ADC Products Inc.	Minneapolis, Minn.
70903	Belden Mfg. Co.	Chicago, Ill.
70998	Bird Electronic Corp.	Cleveland, Ohio
71002	Birnbach Radio Co.	New York, N.Y.
71034	Birley Electric Co., Inc.	Erie, Pa.
71041	Boston Gear Works Div. of Murray Co. of Texas	Quincy, Mass.
71218	Bud Radio, Inc.	Willoughby, Ohio
71279	Cambridge Thermionics Corp.	Cambridge, Mass.
71286	Camloc Fastener Corp.	Paramus, N.J.
71313	Cardwell Condenser Corp.	Lindenhurst L.I., N.Y.
71400	Bussmann Mfg. Div. of McGraw-Edison Co.	St. Louis, Mo.
71436	Chicago Condenser Corp.	Chicago, Ill.
71447	Calif. Spring Co., Inc.	Pico-Rivera, Calif.
71450	CTS Corp.	Elkhart, Ind.
71468	ITT Cannon Electric Inc.	Los Angeles, Calif.
71471	Cinema, Div. Aerovox Corp.	Burbank, Calif.
71482	C.P. Clare & Co.	Chicago, Ill.
71590	Centralab Div. of Globe Union Inc.	Milwaukee, Wis.
71616	Commercial Plastics Co.	Chicago, Ill.
71700	Cornish Wire Co., The	New York, N.Y.
71707	Coto Coil Co., Inc.	Providence, R.I.
71744	Chicago Miniature Lamp Works	Chicago, Ill.
71785	Cinch Mfg. Co., Howard B. Jones Div.	Chicago, Ill.
71984	Dow Corning Corp.	Midland, Mich.
72136	Electro Motive Mfg. Co., Inc.	Willimantic, Conn.
72619	Dialight Corp.	Brooklyn, N.Y.
72656	Indiana General Corp., Electronics Div.	Keasby, N.J.
72699	General Instrument Corp., Cap. Div.	Newark, N.J.
72765	Drake Mfg. Co.	Harwood Heights, Ill.
72825	Hugh H. Eby Inc.	Philadelphia, Pa.
72928	Gudeman Co.	Chicago, Ill.
72962	Elastic Stop Nut Corp.	Union, N.J.
72964	Robert M. Hadley Co.	Los Angeles, Calif.
72982	Erie Technological Products, Inc.	Erie, Pa.
73061	Hansen Mfg. Co., Inc.	Princeton, Ind.
73076	H.M. Harper Co.	Chicago, Ill.
73138	Helipot Div. of Beckman Inst., Inc.	Fullerton, Calif.
73293	Hughes Products Division of Hughes Aircraft Co.	Newport Beach, Calif.
73445	Amperex Elect Co.	Hicksville, L.I., N.Y.
73506	Bradley Semiconductor Corp.	New Haven, Conn.
73559	Carling Electric, Inc.	Hartford, Conn.
73586	Circle F Mfg. Co.	Trenton, N.J.
73682	George K. Garrett Co., Div. MSL Industries Inc.	Philadelphia, Pa.
73734	Federal Screw Products Inc.	Chicago, Ill.
73743	Fischer Special Mfg. Co.	Cincinnati, Ohio
73793	General Industries Co., The	Elyria, Ohio
73846	Goshen Stamping & Tool Co.	Goshen, Ind.
73899	JFD Electronics Corp.	Brooklyn, N.Y.
73905	Jennings Radio Mfg. Corp.	San Jose, Calif.
73957	Groov-Pin Corp.	Ridgefield, N.J.
74276	Signalite Inc.	Neptune, N.J.
74455	J.H. Winns, and Sons	Winchester, Mass.
74861	Industrial Condenser Corp.	Chicago, Ill.
74868	R.F. Products Division of Amphenol-Borg Electronics Corp.	Danbury, Conn.
74970	E.F. Johnson Co.	Waseca, Minn.
75042	International Resistance Co.	Philadelphia, Pa.
75263	Keystone Carbon Co., Inc.	St. Marys, Pa.
75378	CTS Knights Inc.	Sandwich, Ill.
75382	Kulka Electric Corporation	Mt. Vernon, N.Y.
75818	Lenz Electric Mfg. Co.	Chicago, Ill.
75915	Littlefuse, Inc.	Des Plaines, Ill.
76005	Lord Mfg. Co.	Erie, Pa.
76210	C.W. Marwedel	San Francisco, Calif.
76433	General Instrument Corp., Micamold Division	Newark, N.J.
76487	James Millen Mfg. Co., Inc.	Malden, Mass.
76493	J.W. Miller Co.	Los Angeles, Calif.
76530	Cinch-Monadnock, Div. of United Carr Fastener Corp.	San Leandro, Calif.
76545	Mueller Electric Co.	Cleveland, Ohio
76703	National Union	Newark, N.J.
76854	Oak Manufacturing Co.	Crystal Lake, Ill.
77068	The Bendix Corp., Electrodynamics Div.	N. Hollywood, Calif.
77075	Pacific Metals Co.	San Francisco, Calif.
77221	Phanostran Instrument and Electronic Co.	South Pasadena, Calif.
77252	Philadelphia Steel and Wire Corp.	Philadelphia, Pa.
77342	American Machine & Foundry Co. Potter & Brumfield Div.	Princeton, Ind.
77630	TRW Electronic Components Div.	Camden, N.J.
77638	General Instrument Corp., Rectifier Div.	Brooklyn, N.Y.
77764	Resistance Products Co.	Harrisburg, Pa.
77969	Rubbercraft Corp. of Calif.	Torrance, Calif.
78189	Shakeproof Division of Illinois Tool Works	Elgin, Ill.
78277	Sigma	So. Braintree, Mass.
78283	Signal Indicator Corp.	New York, N.Y.
78290	Struthers-Dunn Inc.	Pitman, N.J.
78424	Specialty Leather Prod. Co.	Newark, N.J.
78452	Thompson-Bremer & Co.	Chicago, Ill.
78471	Tilley Mfg. Co.	San Francisco, Calif.
78488	Stackpole Carbon Co.	St. Marys, Pa.
78493	Standard Thomson Corp.	Waltham, Mass.
78553	Tinnerman Products, Inc.	Cleveland, Ohio
78790	Transformer Engineers	San Gabriel, Calif.
78947	Ucinite Co.	Newtonville, Mass.
79136	Waldes Kohinoor Inc.	Long Island City, N.Y.
79142	Veeder Root, Inc.	Hartford, Conn.
79251	Wenco Mfg. Co.	Chicago, Ill.
79727	Continental-Wirt Electronics Corp.	Philadelphia, Pa.
79963	Zierick Mfg. Corp.	New Rochelle, N.Y.
80031	Mepco Division of Sessions Clock Co.	Morristown, N.J.
80120	Schnitzer Alloy Products Co.	Elizabeth, N.J.
80131	Electronic Industries Association. Any brand Tube meeting EIA Standards-Washington, DC.	
80207	Unimax Switch, Div. Maxon Electronics Corp.	Wallingford, Conn.
80223	United Transformer Corp.	New York, N.Y.
80248	Oxford Electric Corp.	Chicago, Ill.
80294	Bourns Inc.	Riverside, Calif.
80411	Acro Div. of Robertshaw Controls Co.	Columbus, Ohio

Table 6-3. Code List of Manufacturers (Continued)

Code No.	Manufacturer	Address
80486	All Star Products Inc.	Defiance, Ohio
80509	Avery Label Co.	Monrovia, Calif.
80583	Hammarlund Co., Inc.	Mars Hill, N.C.
80640	Stevens, Arnold, Co., Inc.	Boston, Mass.
80813	Dimco Gray Co.	Dayton, Ohio
81030	International Instruments Inc.	Orange, Conn.
81073	Grayhill Co.	LaGrange, Ill.
81095	Triad Transformer Corp.	Venice, Calif.
81312	Winchester Elec. Div. Litton Ind., Inc.	Oakville, Conn.
81349	Military Specification	
81483	International Rectifier Corp.	El Segundo, Calif.
81541	Airpax Electronics, Inc.	Cambridge, Maryland
81860	Barry Controls, Div. Barry Wright Corp.	Watertown, Mass.
82042	Carter Precision Electric Co.	Skokie, Ill.
82047	Sperti Faraday Inc., Copper Hewitt Electric Div.	Hoboken, N.J.
82116	Electric Regulator Corp.	Norwalk, Conn.
82142	Jeffers Electronics Division of Speer Carbon Co.	Du Bois, Pa.
82170	Fairchild Camera & Inst. Corp. Space & Defense System Div.	Paramus, N.J.
82209	Maguire Industries, Inc.	Greenwich, Conn.
82219	Sylvania Electric Prod. Inc. Electronic Tube Division	Emporium, Pa.
82376	Astron Corp.	East Newark, Harrison, N.J.
82389	Switchcraft, Inc.	Chicago, Ill.
82647	Metals & Controls Inc. Spencer Products	Attleboro, Mass.
82768	Phillips-Advance Control Co.	Joliet, Ill.
82866	Research Products Corp.	Madison, Wis.
82877	Rotron Mfg. Co., Inc.	Woodstock, N.Y.
82893	Vector Electronic Co.	Glendale, Calif.
83014	Hartwell Corp.	Los Angeles, Calif.
83058	Carr Fastener Co.	Cambridge, Mass.
83086	New Hampshire Ball Bearing, Inc.	Peterborough, N.H.
83125	General Instrument Corp., Capacitor Div.	Darlington, S.C.
83148	ITT Wire and Cable Div.	Los Angeles, Calif.
83186	Victory Eng. Corp.	Springfield, N.J.
83298	Bendix Corp., Red Bank Div.	Red Bank, N.J.
83315	Hubbell Corp.	Mundelein, Ill.
83324	Rosan Inc.	Newport Beach, Calif.
83330	Smith, Herman H., Inc.	Brooklyn, N.Y.
83332	Tech Labs	Palisade's Park, N.J.
83385	Central Screw Co.	Chicago, Ill.
83501	Gavitt Wire and Cable Co. Div. of Amerace Corp.	Brookfield, Mass.
83594	Burroughs Corp. Electronic Tube Div.	Plainfield, N.J.
83740	Union Carbide Corp. Consumer Prod. Div.	New York, N.Y.
83777	Model Eng. and Mfg., Inc.	Huntington, Ind.
83821	Loyd Scruggs Co.	Festus, Mo.
83942	Aeronautical Inst. & Radio Co.	Lodi, N.J.
84171	Arco Electronics Inc.	Great Neck, N.Y.
84396	A.J. Glesener Co., Inc.	San Francisco, Calif.
84411	TRW Capacitor Div.	Ogallala, Neb.
84970	Sarkes Tarzian, Inc.	Bloomington, Ind.
85454	Boonton Molding Company	Boonton, N.J.
85471	A.B. Boyd Co.	San Francisco, Calif.
85474	R.M. Bracamonte & Co.	San Francisco, Calif.
85660	Koiled Kords, Inc.	Hamden, Conn.
85911	Seamless Rubber Co.	Chicago, Ill.
86174	Fafnir Bearing Co.	Los Angeles, Calif.
86197	Clifton Precision Products Co., Inc.	Clifton Heights, Pa.
86579	Precision Rubber Products Corp.	Dayton, Ohio
86684	Radio Corp. of America, Electronic Comp. & Devices Div.	Harrison, N.J.
86928	Seastrom Mfg. Co.	Glendale, Calif.
87034	Marco Industries	Anaheim, Calif.
87216	Philco Corporation (Lansdale Division)	Lansdale, Pa.
87473	Western Fibrous Glass Products Co.	San Francisco, Calif.
87664	Van Waters & Rogers Inc.	San Francisco, Calif.
87930	Tower Mfg. Corp.	Providence, R.I.
88140	Cutler-Hammer, Inc.	Lincoln, Ill.
88220	Gould-National Batteries, Inc.	St. Paul, Minn.
88698	General Mills, Inc.	Buffalo, N.Y.
89231	Graybar Electric Co.	Oakland, Calif.
89473	G.E. Distributing Corp.	Schenectady, N.Y.
89665	United Transformer Co.	Chicago, Ill.
90030	United Shoe Machinery Corp.	Beverly, Mass.
90179	US Rubber Co., Consumer Ind. & Plastics Prod. Div.	Passaic, N.J.
90970	Bearing Engineering Co.	San Francisco, Calif.
91146	ITT Cannon Elect, Inc., Salem Div.	Salem, Mass.
91260	Connor Spring Mfg. Co.	San Francisco, Calif.
91345	Miller Dial & Nameplate Co.	El Monte, Calif.
91418	Radio Materials Co.	Chicago, Ill.
91506	Augat Inc.	Attleboro, Mass.
91637	Dale Electronics, Inc.	Columbus, Nebr.
91662	Elco Corp.	Willow Grove, Pa.
91737	Gremar Mfg. Co., Inc.	Wakefield, Mass.
91827	K F Development Co.	Redwood City, Calif.
91886	Malco Mfg. Co., Inc.	Chicago, Ill.
91929	Honeywell Inc., Micro Switch Div.	Freeport, Ill.
91961	Nahm-Bros. Spring Co.	Oakland, Calif.
92180	Tru-Connector Corp.	Peabody, Mass.
92367	Elgeet Optical Co. Inc.	Rochester, N.Y.
92607	Tensolite Insulated Wire Co., Inc.	Tarrytown, N.Y.
92702	IMC Magnetics Corp.	Wesbury Long Island, N.Y.
92966	Hudson Lamp Co.	Kearney, N.J.
93332	Sylvania Electric Prod. Inc. Semiconductor Div.	Woburn, Mass.
93369	Robbins & Myers Inc.	Palisades Park, N.J.
93410	Stemco Controls, Div. of Essex Wire Corp.	Mansfield, Ohio
93632	Waters Mfg. Co.	Culver City, Calif.
93929	G.V. Controls	Livingston, N.J.
94137	General Cable Corp.	Bayonne, N.J.
94142	Phelps Dodge	Yonkers, N.Y.
94144	Raytheon Co., Comp. Div., Ind. Comp. Operations	Quincy, Mass.
94148	Scientific Electronics Products, Inc.	Loveland, Colo.
94154	Wagner Elect. Corp., Tung-Sol Div.	Newark, N.J.
94197	Curtiss-Wright Corp. Electronics Div.	East Paterson, N.J.
94222	South Chester Corp.	Chester, Pa.
94330	Wire Cloth Products, Inc.	Bellwood, Ill.
94375	Automatic Metal Products Co.	Brooklyn, N.Y.
94682	Worcester Pressed Aluminum Corp.	Worcester, Mass.
94696	Magnecraft Electric Co.	Chicago, Ill.
95023	George A. Philbrick Researchers, Inc.	Boston, Mass.
95236	Allies Products Corp.,	Dania, Fla.
95238	Continental Connector Corp.	Woodside, N.Y.
95263	Leecraft Mfg. Co., Inc.	Long Island, N.Y.
95265	National Coil Co.	Sheridan, Wyo.
95275	Vitramon, Inc.	Bridgeport, Conn.
95348	Gordos Corp.	Bloomfield, N.J.
95354	Methode Mfg. Co.	Rolling Meadows, Ill.
95566	Arnold Engineering Co.	Marengo, Ill.
95712	Dage Electric Co., Inc.	Franklin, Ind.
95984	Siemon Mfg. Co.	Wayne, Ill.
95987	Weckesser Co.	Chicago, Ill.
96067	Microwave Assoc., West Inc.	Sunnyvale, Calif.
96095	Hi-Q Div. of Aerovox Corp.	Olean, N.Y.
96256	Thordarson-Meissner Inc.	Mt. Carmel, Ill.
96296	Solar Manufacturing Co.	Los Angeles, Calif.
96306	Microswitch, Div. of Minn.-Honeywell	Freeport, Ill.
96330	Carlton Screw Co.	Chicago, Ill.
96341	Microwave Associates, Inc.	Burlington, Mass.
96501	Excel Transformer Co.	Oakland, Calif.
96733	San Fernando Elect. Mfg. Co.	San Fernando, Calif.
96881	Thomson Ind. Inc.	Long Is., N.Y.
97464	Industrial Retaining Ring Co.	Irvington, N.J.
97539	Automatic & Precision Mfg.	Englewood, N.J.
97979	Reon Resistor Corp.	Yonkers, N.Y.
97983	Litton System Inc., Adler-Westrex Commun. Div.	New Rochelle, N.Y.
98141	R-Troncis, Inc.	Jamaica, N.Y.
98159	Rubber Teck, Inc.	Gardena, Calif.
98220	Hewlett-Packard Co., Moseley Div.	Pasadena, Calif.
98278	Microdot, Inc.	So. Pasadena, Calif.
98291	Sealectro Corp.	Mamaroneck, N.Y.
98376	Zero Mfg. Co.	Burbank, Calif.
98410	Etc Inc.	Cleveland, Ohio
98731	General Mills Inc., Electronics Div.	Minneapolis, Minn.
98734	Paeco Div. of Hewlett-Packard Co.	Palo Alto, Calif.
98821	North Hills Electronics, Inc.	Glen Cove, N.Y.
98978	International Electronic Research Corp.	Burbank, Calif.
99109	Columbia Technical Corp.	New York, N.Y.
99313	Varian Associates	Palo Alto, Calif.
99378	Atlee Corp.	Winchester, Mass.
99515	Marshall Ind., Capacitor Div.	Monrovia, Calif.
99707	Control Switch Division, Controls Co. of America	El Segundo, Calif.
99800	Delevan Electronics Corp.	East Aurora, N.Y.
99848	Wilco Corporation	Indianapolis, Ind.
99928	Branson Corp.	Whippany, N.J.
99934	Renbrandt, Inc.	Boston, Mass.
99942	Hoffman Electronics Corp. Semiconductor Div.	El Monte, Calif.
99957	Technology Instrument Corp. of Calif.	Newbury Park, Calif.

THE FOLLOWING HP VENDORS HAVE NO NUMBER ASSIGNED IN THE LATEST SUPPLEMENT TO THE FEDERAL SUPPLY CODE FOR MANUFACTURERS HANDBOOK.

0000F	Malco Tool and Die	Los Angeles, Calif.
0000Z	Willow Leather Products Corp.	Newark, N.J.
000AB	ETA	England
000BB	Precision Instrument Components Co.	Van Nuys, Calif.
000CS	Hewlett-Packard Co., Colorado Springs	Colorado Springs, Colorado
000MM	Rubber Eng. & Development	Hayward, Calif.
000NN	A "N" D Mfg. Co.	San Jose, Calif.
000QQ	Cooltron	Oakland, Calif.
000WW	California Eastern Lab.	Burlington, Calif.
000YY	S.K. Smith Co.	Los Angeles, Calif.

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