HONEYWELL EDP

HARDWARE BULLETIN

SERIES 200

TYPE 281-2F SINGLE-CHANNEL COMMUNICATION CONTROL

SUBJECT: Equipment Specifications for the Type 281-2F Single-Channel, Broadband Communication Control for Use on Leased, Point-to-Point, Private Broadband Line Service (Telpak A).

SPECIAL INSTRUCTIONS: The references used in this text are the Honeywell Series 200 Models 200/1200/2200 Programmers' Reference Manual, Order No. 139, and the Honeywell Series 200 Model 120 Programmers' Reference Manual, Order No. 141.

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I. GENERAL DESCRIPTION

The Honeywell Type 281-2F Communication Control provides the interconnection of a Series 200 central processor with a remote terminal by means of a Bell DATA-PHONE Dataset 301B on leased, point-to-point, private broadband Telpak A line service. Telpak A has a carrier spectrum equivalent to 12 voice channels. The Bell DATA-PHONE Dataset 301B is required at each end of the transmission link, as shown in Figure 1, page 2.

The Type 281-2F is compatible with all Series 200 central processors; however, the Type 121 must be equipped with Feature 1015 for half-duplex operation or with Feature 1016 for full-duplex operation (Features 1015 and 1016 are described in the Model 120 Programmers' Reference Manual).

The line is characterized by serial bit-stream transmission of eight-level code in the half-duplex (two-way, non-simultaneous) or the full-duplex (two-way, simultaneous) mode. The codes transmitted may be Honeywell code, the American Standard Code for Information Interchange (ASCII), or other codes whose character length is eight bits or less. The rate of transmission over the line is 5100 characters per second.

As shown in Figure 1, page 2, Type 281-2F operation may be rendered compatible with remote station equipment having any one of three configurations. The first configuration consists simply of a Series 200 central processor with a Type 281-2F communication control— this is known as the Honeywell mode of operation. The second configuration is composed of any computer or high-speed device equipped with a Bell DATA-PHONE Dataset 301B and using an eight-bit line code, a Type 281-2F message format, and a continuous bit-stream mode of operation with synchronization established individually for each data block or control block. Such synchronization is accomplished when each data block is preceded by a specified minimum number of synchronization characters; the receiver utilizes these characters to establish synchronization with the transmitter. The third remote station configuration consists of a Univac 1004 having a Model DLT2B Dataline Terminal operating in conjunction with a Bell DATA-PHONE Dataset 301B. This is known as the Univac mode of operation. Special format requirements of the Univac mode are discussed in Appendix A.

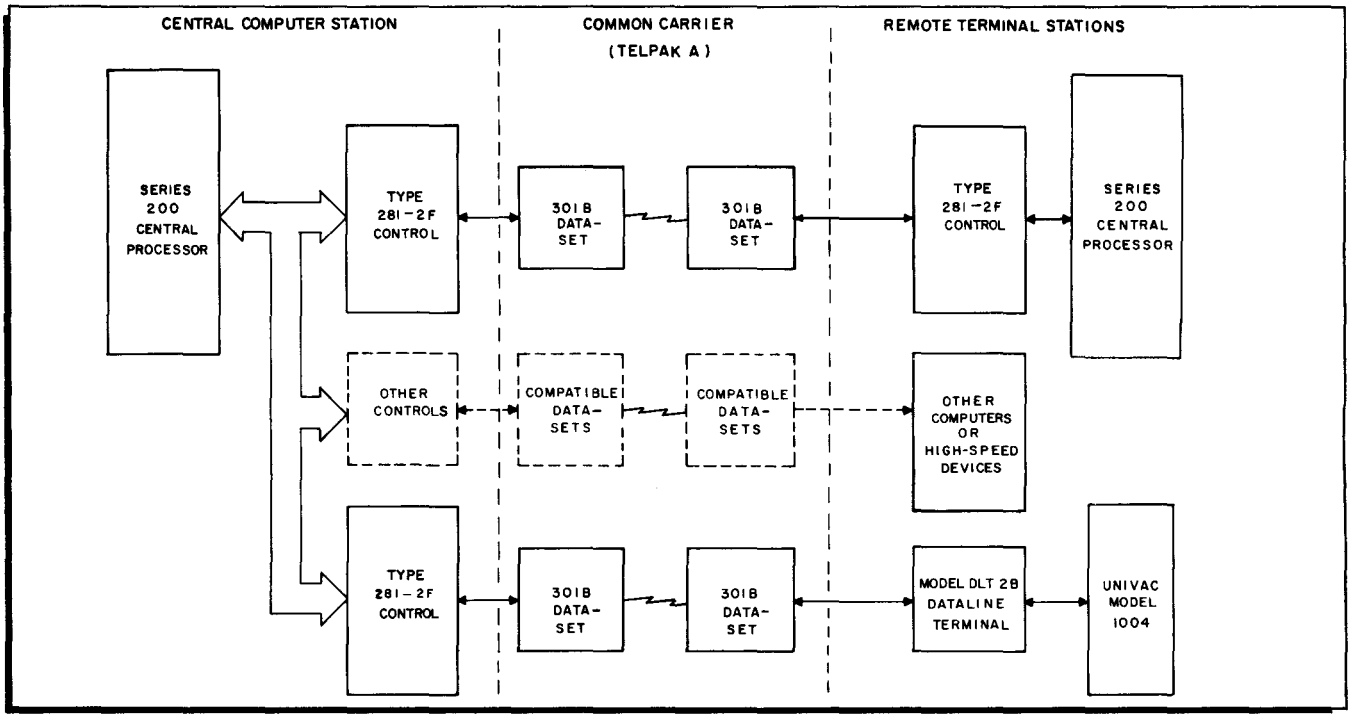


Figure 1. Typical System Applications

The standard Series 200 logic drawer contains one Type 281-2F Communication Control.

II. TYPE 281-2F INTERFACE WITH SERIES 200 CENTRAL PROCESSORS

Standard peripheral interface logic for simultaneous input and output connects the communication control to the standard Series 200 peripheral bus.

III. DATASET/COMMUNICATION CONTROL INTERFACE

The common carrier line terminates in a Bell DATA-PHONE Dataset 301B connected to the Type 281-2F Communication Control by means of a coaxial cable which is limited to a maximum length of 50 feet.

The dataset converts the voltage-level signals of the Type 281-2F into phase-modulated carrier signals for transmission over a Telpak channel as shown in Figure 2, page 3. A voice coordination channel is furnished for the user.

IV. Type 281-2F FUNCTIONAL CHARACTERISTICS

A. Transmission Mode

The Type 281-2F Communication Control is capable of full-duplex or half-duplex operation in the block-by-block transmission mode. Thus — after the initial block — each data block is sent when a response

has indicated the reception of the previous block. Data blocks may be variable in length; maximum block size is limited only by available memory area and data storage capabilities at the terminals.

B. Data Block Format

In conformity with the American Standards Association, the general line format for the data block is as follows:

5 Synchronization Characters	Start-of-Text Character	Data	End-of-Text Character	LRC Character

The general line format for the control block is as follows. In full-duplex operation this block may appear in the middle of a data block.

5 Synchronization Characters	Data-Link-Escape Character	Control	Control (Repeated)

Format requirements for the Univac mode are discussed in Appendix A.

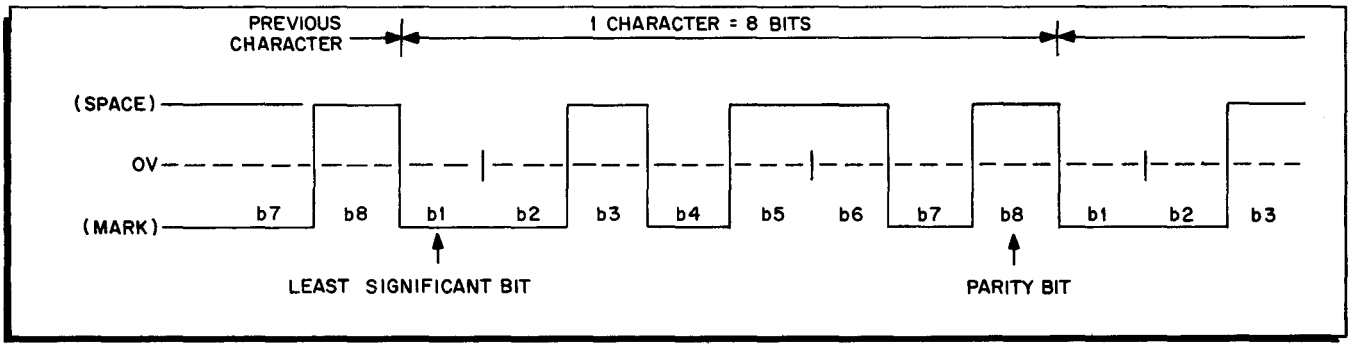


Figure 2. Data Signal at Communication Control/Dataset Interface

1. Character Significance

The following paragraphs define the significance of specific characters in the block format (Table I, page 4). The Honeywell code is illustrated in Table II, page 5, and the American Standard Code for Information Interchange (ASCII) is shown in Table III, page 6.

In the Univac mode of operation the significance of these characters differs, as shown in Table A-I, page A-4.

a. Synchronization Characters

Each block of characters is preceded by at least five synchronization characters. The communication control recognizes two successive characters to achieve synchronization with the remote terminal. The synchronization characters are filtered from the transmitted information; they do not enter memory as data and they are not included in longitudinal-redundancy-check computations.

b. Start-of-Text (STX) Character

The ASCII start-of-text (STX) character signals the beginning of a data block. If synchronization is achieved prior to recognition of the STX character, this character and all subsequent data characters are passed into memory until the end-of-text character is recognized.

Table I. Communication Control Action on Control Characters in Honeywell and ASCII Modes

SYMBOL	NAME	CODE (8-BIT)	NUMBER REQUIRED	ACTION OF CONTROL UNIT
		87654321		
SYNC	Synchronization Character	00010110	5 (min)	Used to achieve sync. Filtered from central processor.
STX	Start-of-Text	00000010	1	This and all data characters that follow are sent to the central processor.
ACK	Acknowledge	10000110	2	Causes interrupt, Filtered.
NAK	Negative Acknowledge	00010101	2	Causes interrupt, Filtered.
ENQ	Enquiry	10000101	2	Interrupt, Filtered.
BEL	Bell (used as TEL REQ.)	00000111	2	Interrupt, Filtered.
WBT	Wait Before Transmit	10011110	2	Interrupt, Filtered.
ETX	End-of-Text	10000011	1	Causes interrupt, Passed into central processor memory.
EOT	End-of-Transmission	00000100	2	Interrupt, Filtered.
LRC	Long Redundancy Check	--------	1	Filtered.

NOTE

This table has been established with odd parity on the eighth bit. It must be modified in the case of even parity.

c. End-of-Text (ETX) Character

The ASCII end-of-text (ETX) character signals the end of a data block; this character is not filtered from the transmitted information but enters main memory. It also signifies that immediately following is a longitudinal-redundancy-check character.

d. Longitudinal-Redundancy-Check (LRC) Character

The longitudinal-redundancy-check (LRC) character is generated or checked by the communication control immediately after the end-of-text character. Its composition and significance are discussed in Section IV, D, 2.

e. Data-Link-Escape (DLE) Character

The ASCII data-link-escape (DLE) character signifies that the two subsequent characters constitute a control sequence.

The communication control thereupon looks for a control character to appear twice in sequence. Upon recognition of this sequence, the communication control loads a status register (Section IV, E, 2) with information pertaining to the nature of the control character received and sets the Interrupt function. The entire control sequence is filtered from the transmitted information so it does not enter main memory.

As mentioned in the opening paragraph of this Section IV, B, 1, the ASCII code bit configurations of the above characters are shown in in Table III, page 6.

For operation with non-ASCII codes, the user may select some of the ASCII characters to suit the remote terminal requirements. The selectable characters are discussed in Section IV, C, 3.

Table II. Honeywell 6-Bit Code

High-Speed Printer	Octal Code	Binary Code	High-Speed Printer	Octal Code	Binary Code
0	00	000000	-	40	100000
1	01	000001	J	41	100001
2	02	000010	K	42	100010
3	03	000011	L	43	100011
4	04	000100	M	44	100100
5	05	000101	N	45	100101
6	06	000110	O	46	100110
7	07	000111	P	47	100111
8	10	001000	Q	50	101000
9	11	001001	R	51	101001
'	12	001010	#	52	101010
=	13	001011	$	53	101011
:	14	001100	*	54	101100
Space	15	001101	"	55	101101
>	16	001110	≠	56	101110
&	17	001111	!	57	101111
+	20	010000	<	60	110000
A	21	010001	/	61	110001
B	22	010010	S	62	110010
C	23	010011	T	63	110011
D	24	010100	U	64	110100
E	25	010101	V	65	110101
F	26	010110	W	66	110110
G	27	010111	X	67	110111
H	30	011000	Y	70	111000
I	31	011001	Z	71	111001
;	32	011010	@	72	111010
.	33	011011	,	73	111011
)	34	011100	(	74	111100
%	35	011101	C_R	75	111101
■	36	011110	□	76	111110
?	37	011111	¢	77	111111

NOTE: Bit 7 must contain a one. Bit 8 is the parity bit.

Table III. American Standard Code for Information Interchange

Bits b_4 b_3 b_2 b_1	Row ↓ Col. →	b_7 b_6 b_5 = 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
		0	1	2	3	4	5	6	7
0 0 0 0	0	NUL	DLE	SP	0	\	P	@	p
0 0 0 1	1	SOH	DC1	!	1	A	Q	a	q
0 0 1 0	2	STX	DC2	"	2	B	R	b	r
0 0 1 1	3	ETX	DC3	#	3	C	S	c	s
0 1 0 0	4	EOT	DC4	$	4	D	T	d	t
0 1 0 1	5	ENQ	NAK	%	5	E	U	e	u
0 1 1 0	6	ACK	SYN	&	6	F	V	f	v
0 1 1 1	7	BEL	ETB	′	7	G	W	g	w
1 0 0 0	8	BS	CAN	(	8	H	X	h	x
1 0 0 1	9	HT	EM	)	9	I	Y	i	y
1 0 1 0	10	LF	SS	*	:	J	Z	j	z
1 0 1 1	11	VT	ESC	+	;	K	[	k	{
1 1 0 0	12	FF	FS	,	<	L	~	l	¬
1 1 0 1	13	CR	GS	-	=	M	]	m	}
1 1 1 0	14	SO	RS	.	>	N	^	n	|
1 1 1 1	15	SI	US	/	?	O	—	o	DEL

Control Characters

NULL	Null/Idle
SOH	Start of Heading (CC)
STX	Start of Text (CC)
ETX	End of Text (CC)
EOT	End of Transmission (CC)
ENQ	Enquiry (CC)
ACK	Acknowledge (CC)
BELL	Audible or attention signal
BS	Backspace (FE)
HT	Horizontal Tabulation (punch card skip) (FE)
LF	Line Feed (FE)
VT	Vertical Tabulation (FE)
FF	Form Feed (FE)
CR	Carriage Return (FE)
SO	Shift Out
SI	Shift In
DLE	Data Link Escape (CC)
DC1, DC2, DC3	Device Controls
DC4	Device Control (stop)
NACK	Negative Acknowledge (CC)
SYNC	Synchronous Idle (CC)
ETB	End of Transmission Block (CC)
CNCL	Cancel
EM	End of Medium
ESC	Escape
FS	File Separator (IS)
GS	Group Separator (IS)
RS	Record Separator (IS)
US	Unit Separator (IS)
DEL	Delete

NOTE

(CC) Communication control
(FE) Format effecter
(IS) Information separator

C. Character Format

1. Line Format

The Type 281-2F is capable of transmitting or receiving any eight-bit character on the communication line. The data character may be in ASCII code with parity in the eighth bit, or it may be in the Honeywell six-bit character code with parity in the eighth bit and a "one" in the seventh bit to differentiate it from a control character, since all control characters remain in ASCII code.

In the Univac mode of operation, the seventh bit is parity (except for the synchronization character), and the eighth bit is a "one."

2. Memory Allocation

When ASCII code is used, each eight-bit character on the line occupies two positions in main memory. However, when Honeywell code is used for data transmission, data may be stored in memory as individual six-bit characters. The communication control can then force the seventh bit to be a "one" and — when transmitting — the eighth bit becomes the parity bit.

If operating in Univac mode, the system may store data in six-bit characters with the communication control generating parity on bit seven and a "one" in bit eight. Details are discussed in Section VI.

3. Variable Character Recognition

The Type 281-2F is capable of recognizing the ten ASCII control characters. To ensure system flexibility the user may select certain of these characters during installation. The characters are selected by means of suitable jumper cards. However, one should note that such selection prohibits change in character recognition by programming; also — in the Honeywell mode of operation — the end-of-text character or its six-bit equivalent must be recognized on transmission.

The following characters can be selected:

a. Synchronization Character

The recognized character is used to achieve synchronization. Only one character is so specified in the system and it can not be used elsewhere in the block as a data or control character. The synchronization character is filtered from the information transmitted to main memory.

b. Framing Characters

"Framing" characters such as STX and ETX are transferred to main memory.

c. Control Characters

The action taken on the control characters ACK, NAK, ENQ, TEL REQ, WBT and EDT is described in Table I, page 4.

D. Error Checking

1. Parity Check

The Type 281-2F is capable of checking for odd or even parity on all received characters with the exception of the longitudinal-redundancy-check character and — in the Univac mode of operation — the synchronization character. Selection of odd or even parity is accomplished by means of jumper cards; it is not under program control. A longitudinal-

redundancy-check error indication is set if the received parity bit does not check with parity generated by the unit.

The communication control can also generate odd or even parity for transmitted characters. Parity generation can be inhibited independently under program control. If parity is inhibited the eighth bit is read from memory and transmitted without change. Parity generation can not be inhibited in the Honeywell mode.

2. Longitudinal Redundancy Check

The communication control generates a parity bit for each of the eight bit positions of a transmitted character. The resultant eight-bit longitudinal-redundancy-check character is transmitted immediately following the end-of-text character. This LRC character guarantees even parity in each bit position over all the characters in the block.

The Type 281-2F generates the longitudinal-redundancy-check character for the incoming block in the same way as for the outgoing block. The communication control compares this generated longitudinal-redundancy-check character against the one transmitted by the remote terminal. It indicates reception of an erroneous block for "unequal compare" or reception of a correct block for "equal compare."

Each bit position in the longitudinal-redundancy-check character is developed as a half-add sum of the same position in all characters within the block. This rule also applies to the parity bit position of the longitudinal-redundancy-check character. Therefore — since the longitudinal-redundancy-check character may have odd or even parity — character parity is not computed nor checked on the LRC character itself.

Synchronization characters, data-link-escape characters and control characters do not enter longitudinal-redundancy-check computation. Framing characters such as start-of-text and end-of-text do enter longitudinal-redundancy-check computation.

3. Overwrite

An overwrite occurs when a PDT instruction is not available for transferring data from the communication control's receive buffer to the central processor. The overwrite causes the Type 281-2F to indicate reception of a block with bad parity, thus overriding the longitudinal redundancy check. An interrupt is set at the end of the block. The program returns a NAK character, forcing retransmission of the block.

E. Communication Between the Series 200 Central Processor and the Type 281-2F

1. Central Processor to Type 281-2F

To a certain extent the program directs and controls Type 281-2F operation. Such program direction and control is effected through Peripheral Data Transfer (PDT) and Peripheral Control and Branch (PCB) instructions. Programming responsibilities and PDT/PCB formats are discussed in Section VI.

2. Type 281-2F to Central Processor

Use of the Type 281-2F requires the central processor interrupt capability, which is standard on all Series 200 processors except the Type 201; the latter must be equipped with Feature 012 (Models 200/1200/2200 Programmers' Reference Manual, pages 1-15 and 1-16). The communication control utilizes this capability to signal a need for central processor action. The Type 281-2F also maintains two status registers — one for reception and one for transmission.

When an interrupt occurs, testing of the appropriate status register determines its cause. Each status register contains six bit positions which store a maximum of six different causes of interrupts.

F. Time-Out

The Type 281-2F is equipped with a timer which "times-out" and interrupts the central processor between 100 and 200 milliseconds after being activated. The timer alerts the central processor to long periods of inactivity or to lack of an expected response on the line. The communication control starts the timer when transmission of a data block is terminated by an end-of-text character or when an end-of-transmission (EOT) signal is sent. "Time-out" may stop the timer, or the Type 281-2F may disable it upon recognition of a legal control character sequence signifying ACK, NAK, or WBT. Two successive, identical control characters must be recognized by the communication control.

A program PCB instruction may also activate or deactivate the timer.

V. OPERATIONAL CHARACTERISTICS

A. General

The Type 281-2F is a broadband communication control capable of full-duplex or half-duplex operation. The efficiency and degree of standardization in the system determine the optimum operating procedure; however — as a guide for operation in ASCII or Honeywell mode — eight basic steps and/or concepts are outlined below. Special requirements for Univac mode operation are discussed in Appendix A.

B. Procedure for Manual Operation in Full-Duplex Communication

1. The communication program is entered into main memory and the peripheral units are readied.
2. Any noncommunication program can be run in the central processor while it is waiting for the start of the communication program.
3. Communication control A, ready to transmit, sends a control sequence of ENQ characters.
4. Communication control B, at the other end of the line, sends an acknowledge sequence of ACK characters.
5. Control A, receiving the acknowledge sequence, recognizes that control B is ready to receive and begins transmission. If control A does not receive the acknowledge sequence, it "times-out." Control A may try again; if it receives no acknowledge sequence from control B its operator may talk over the voice line or make a later attempt to transmit.
6. Regardless of whether or not the other communication control is transmitting, either control may attempt transmission because of the Type 281-2F's full-duplex capability.
7. Transmission and/or reception of a complete block of data is signaled to the central processor by the communication control generating the interrupt. This signal initiates program activity. The action taken by the program depends upon the system requirements.
8. An end-of-transmission message is sent and acknowledged. Each station notifies its operator of the completed transmission and the operators may converse. No line release is necessary.

VI. PROGRAMMING REFERENCE DATA

A. General

Telepak A lines — having an intercharacter time of 192 microseconds — transmit at the rate of 5100 eight-bit characters per second. In order that simultaneous data flow in both directions may be accomplished, the communication control is provided with some degree of independent action.

Programming is the same for full-duplex or half-duplex situations.

B. Characteristics of the System

1. Interrupt

The communication control sets either or both Interrupt functions. When the transmitter requires attention, the transmitter Interrupt function is set. When the receiver requires attention, the receiver Interrupt function is set. Both may be set in a full-duplex operation.

Upon the occurrence of an interrupt, the states of the two Interrupt functions are tested by PCB instructions to determine whether the transmitter or the receiver (or both) requires service. The cause of the Interrupt is determined by testing the corresponding status register.

2. Status Registers

The communication control maintains the two status registers indicating the nature of the interrupts. One register is associated with the transmitter, one with the receiver. Table IV, shows the transmit status register for the Honeywell and ASCII modes; Table V, page 11, shows the receive status register for the same modes. Tables A-II and A-III, pages A-4 and A-5, show these registers for the Univac mode. Each is a six-bit register and the bits are free-flowing. Thus, if a second cause of interrupt occurs before the previous status is cleared, the bit corresponding to this latest interrupt is also set.

Table IV. Transmit Status Register for Honeywell and ASCII Modes

Bit Number	Status	Response
1	Acknowledge	PDT instruction data for the next block to be issued.
2	NAK	PDT instruction data for the same block (retransmit).
3	Wait Before Transmit	Wait for ACK or NAK character.
4	Record Mark	Correct error, wait for NAK character.
5	Time Out	"Control" PDT instruction - ENA or EOT - Terminate if situation persists.

NOTE: All PDT instructions use transmitter read/write channel and logical line address (0t).

The status coming into main memory indicates the latest status of the receiver or transmitter register. If the "transmit" Interrupt function is set, the cause is found by testing the "transmit" status register; if the "receive" Interrupt function is set, the cause is found by testing the "receive" status register. A PDT instruction having a specified C3 control character brings the status of the interrupt into the central processor.

Table V. Receive Status Register for Honeywell and ASCII Modes

Bit Number	Status	Response (in all cases reissue PDT - receive data after response)
1	Received Good Block	"Control" PDT instruction - ACK.
2	Received Bad Block	"Control" PDT instruction - NAK.
3	Enquiry	"Control" PDT instruction - Retransmit last control.
4	Record Mark	"Control" PDT instruction - NAK. TEL REQ if situation persists.
5	Telephone Request	"Control" PDT instruction - ACK and wait for telephone call.
6	End of Transmission	"Control" PDT instruction - ACK.
NOTE: All response PDT instructions use receiver read/write channel and line address (4t).		

3. Control Characters

A control sequence must be inserted in the midst of the data to maintain full-duplex operation. A PDT instruction having a specified C3 control character accomplishes this in the Type 281-2F, as discussed in Section VI, D, 4, b.

4. Single-Frame Demand

Both terminals may be using Honeywell equipment and a Honeywell six-bit character code. In this case it is not necessary to translate the Honeywell character into ASCII code, then retranslate it at the other remote terminal. Instead, the data is stored in Honeywell code (Table II, page 5) in single character positions.

A PDT instruction with a specific C3 control character now may be issued to the communication control, instructing that control to take a data character from one memory location and to force the seventh bit to be a "one." The communication control generates parity on the eighth bit, thus forming an eight-bit character on the line. At the receiving end, if a "Receive" PDT instruction is waiting with an identical C3 control character, the receiver checks for parity, drops bits 8 and 7, and delivers the six-bit character to one memory location.

Similar operation can be performed in the Univac mode, as discussed in Appendix A.

5. Parity Inhibit

A PDT instruction can be used to inhibit the generation and/or checking of parity. However, parity can not be inhibited in the Honeywell mode of operation (single frame demand).

C. System Requirements

1. Read/Write Channel (RWC) Allocation

During full-duplex operation, two read/write channels — capable of simultaneous operation — must be assigned to the communication control for the entire transmission. They may be 12-microsecond read/write channels (for example, 1 and 1' on the Model 200) which are currently available. Only one read/write channel is required for the half-duplex mode of operation.

2. Additional Read/Write Channels

At least one additional read/write channel is required for transfer of received data to storage and for transmission of stored data to main memory.

3. Transfer of Data by the Block Method

A single PDT instruction effects the transmission of each entire block of data. The data block must first be fully assembled in memory, then — upon request — transferred character-by-character to the communication control. Similarly, one PDT instruction effects the reception of each entire block of data. The data block must first be fully assembled in memory, then — when the communication control indicates error-free reception — the data block is transferred to the storage device.

Under no conditions can a data block be transmitted before an acknowledgment of the previous block transmission is received.

If maximum line capacity is to be utilized, the memory area containing data to be transmitted should be buffered; i.e., a block of transmitted data should be present which will be retransmitted if a NAK (negative acknowledge — "please retransmit last block") signal is received. Another block should be present containing the next data to be transmitted if an ACK (acknowledge) signal is received for the block previously transmitted. This latter data block is prepared from storage while the first block is being transmitted.

Buffering should also be adopted for reception to prevent loss of information. A block of data received accurately is transferred to storage while the other communication control is receiving the next block from the line.

D. Programming Procedures

1. General

The programming procedures described in this section apply to operation in the ASCII and Honeywell modes. Special procedural requirements in the Univac mode are discussed in Appendix A.

For ease in programming, the full-duplex Type 281-2F is considered as two units: a transmitter with the logical line address 0t and a receiver with the logical line address 4t (where t is the peripheral address assigned). Programming is the same for full-duplex or half-duplex operation.

If a Type 281-2F Communication Control is used as a transmitter, all comments referring to the transmitter apply and those referring to the receiver are to be ignored. Similarly, when the communication control is used as a receiver, all comments referring to the transmitter are to be ignored.

Even when being used as a receiver, the communication control must transmit control characters. Peripheral Data Transfer instructions accomplish such transmission in the case of the Type 281-2F. The logical line address remains 4t. The direction of data transfer is determined by the entire C3 control character as well as by the sixth bit of the C2 control character. If the proper peripheral address (always 0t for transmitter and 4t for receiver, irregardless of data flow direction) and the proper C3 control character (Table VI, page 25) are not used, the action taken by the communication control is unspecified.

2. Initialization

To prepare the central processor and the Type 281-2F for communication, an "initialization" loop must be effected consisting of the following steps, though not necessarily restricted to them alone:

a. Enter the address of the first instruction of the interrupt loop into the interrupt register;

b. Set the Allow function in the communication control so it can interrupt;

c. Accomplish any miscellaneous "housekeeping" such as establishing necessary constants or fields;

d. Keep a program running in the central processor so it can be interrupted at will.

A prior understanding must exist between the remote terminals and the main computer concerning the code to be utilized so that the issued PDT instructions contain the suitable C3 control character. Coding the PCB and PDT instructions is discussed in Section VI, F and G, respectively. The significance of various C3 control characters in the PDT instruction is described in Section VI, G.

3. Initiating Communication

Either terminal can initiate transmission by means of programming. To determine if remote terminal B is ready to receive, terminal A — wishing to transmit — sends a control block with ENQ characters. Simultaneously, by means of a PCB instruction, terminal A starts the timer. If remote terminal B is capable of responding, it recognizes the ENQ character and responds with an ACK control block. Remote terminal A recognizes the ACK signal, automatically stops the timer, and begins data transmission to terminal B.

On the other hand, if terminal B does not respond to the ENQ character, the timer "times-out" and interrupts the central processor of remote terminal A. Terminal A may repeat the sequence twice more before determining that communication can not be established.

4. Transmission

a. Data

Data is transmitted using the read/write channel and the logical line address associated with the transmitter. The C3 control character used depends upon the code (ASCII, Honeywell, or Univac), the type of frame demand (single or double), and whether or not parity is to be generated.

The length of the transmitted character is always eight bits over the line.

(1) ASCII Code

If the ASCII code is used, the eight bits on the line occupy two six-bit character positions in memory with bits 8 and 7 in bit positions 2 and 1 of the first character location n and bits 6 through 1 in equivalent bit positions at location n + 1. Bit 8 is a "zero"; the communication control inserts the necessary parity. Bits 8 and 7 are entered into bit positions 2 and 1 of location n and bits 6 through 1 are entered into location n + 1 as they are received.

(2) Honeywell Code

If both terminals use Honeywell six-bit code for data, the data characters are stored in memory in individual six-bit character locations. A PDT instruction is issued containing a C3 control character which directs the Type 281-2F to demand only one frame (six bits) per transfer instead of two frames. In addition, this C3 control character causes the Type 281-2F to force bit 7 to be a "one" on all data characters; parity is added on the eighth bit.

On the receiving end of the transfer a PDT instruction with an identical C3 control character is issued to receive the data. This instruction causes the filtering of bits 8 and 7 and the storing of the six data bits in one character position.

NOTE

The synchronization characters, start-of-text (STX) characters, and all control characters remain in eight-bit code.

The Type 281-2F automatically enters the six-bit Honeywell mode of operation after recognizing the start-of-text character. The Honeywell mode of operation ceases when the last character of the block contains the low-order six bits of an ASCII end-of-text (ETX) character with a record mark occurring in the memory location. Upon recognizing this combination, the Type 281-2F forces a "zero" into bit position 7, computes parity, sends out a legal end-of-text character, and follows it with a longitudinal-redundancy-check character.

(3) Univac Code

The single-frame demand can also be effected in the Univac mode, following the same procedure as in (2) above. In this case, however, parity is the seventh bit and the eighth bit is forced to a "one." Switching between Honeywell and Univac modes by program is impossible since the Univac code differs from the ASCII code.

In all three modes of operation the program must supply the necessary synchronization characters and framing (start-of-text and end-of-text) characters. For eight-bit data transfers each of the synchronization characters and the start-of-text and end-of-text characters are eight bits in length, occupying two successive memory locations. In the Univac mode of operation the synchronization character must be supplied with appropriate format. The Type 281-2F neither generates nor checks parity on this last-mentioned character.

The transmitting read/write channel is released when the entire block of data has been sent on the line. However, as defined in Section VI, D, 6, no interrupt occurs until later.

b. Control

The entire control sequence to be transmitted should be stored in memory complete with necessary synchronization characters, data-link-escape character, and two control characters. Since no longitudinal check is generated or performed by a control sequence, no longitudinal-redundancy-check character follows this sequence. The last character position of the control sequence contains a record mark signifying the end of the sequence. When a record mark is sensed within a control sequence, the Type 281-2F draws no more characters from memory and sets no error indications. The setting of this record mark is the programmer's responsibility.

As mentioned earlier, each synchronization character, data-link-escape character, and control character must be eight bits in length, thus occupying two positions in memory. Bits 8 and 7 occupy bit positions 2 and 1 of the first character in location n and the remaining bits are "zeros." If parity is generated by the Type 281-2F, bit 8 is "zero." Bit 7 is "zero" in the ASCII code, but it can be "one" in other codes. Bits 6 through 1 occupy bit positions 6 through 1 of the second character in location n + 1. In the Honeywell operation mode, the eight-bit synchronization character, data-link-escape character, and control character remain in the ASCII code to facilitate their recognition at the receiving end of the line.

Normally the Type 281-2F generates a parity bit on the control characters and introduces it as bit 8. If parity is inhibited on control characters, the parity bit (8) is supplied by the program and transmitted from memory without change.

(1) Receiver

In half-duplex operation, a receiver sends one of three different control characters: the acknowledge (ACK) character, the negative-acknowledge (NAK) character, or the wait-before-transmit (WBT) character.

(a) Acknowledge (ACK)

The acknowledge character signifies that a data block containing no detectable errors is received by the remote terminal and the next data block may be sent. The ACK signal is the normal response when the Type 281-2F interrupts and indicates "received good block of data."

(b) Negative Acknowledge (NAK)

The negative-acknowledge character signifies to the transmitter that a data block is received which displays bad parity or fails the longitudinal redundancy check. The NAK character

request retransmission of the data block. When the communication control interrupts at the termination of a received block and the status register indicates "received bad block of data," the NAK response is transmitted.

(c) Wait Before Transmit (WBT)

The wait-before-transmit control character indicates the development of unexpected troubles at the receiver. These troubles may occur because a storage tape depletion requires the mounting of a new tape or because a temporary mishap has occurred in some part of the system. Under such circumstances the receiver may direct the remote terminal to wait before renewing transmission. It proceeds as follows:

(aa) When reception of the data block is completed and the Type 281-2F has completed and checked the longitudinal-redundancy-check character, indicating to the program whether the data is good or bad, the program sends a WBT sequence instead of the usual ACK or NAK control character.

(bb) Since the length of the interrupt is indeterminate, the WBT control sequence must be repeated at regular intervals, signifying to the other terminal that the line is still active.

(cc) When the Type 281-2F is again ready to receive, it transmits the acknowledge or negative-acknowledge character it has not yet sent, then proceeds in the normal manner.

Thus all three above-mentioned control characters pertain to data received and are known as receiver control characters. One of the three receiver control characters is sent — within the period set by the timer (Section IV, D, 8) — in response to the data block received. The remote terminal does not transmit the next data block unless a control character is sent from the communication control.

The receiver control characters are transmitted by means of PDT instructions using a C3 control character of octal 40 to tell the Type 281-2F that a control sequence is to be transmitted. The read/

write channel allocated to the receiver is used. The C2 control character signifying the logical line address specifies the receiver address (4t).

Upon recognizing the C3 control character of octal 40, the Type 281-2F starts extracting the control characters from memory, executing two frame demands per transfer; it sends these characters over the transmit lines.

Programming steps for full-duplex operation are the same as those used for half-duplex operation; however, when a PDT instruction is issued for transmitting receiver control characters, the communication control operating in the full-duplex mode might be transmitting data. In this case the communication control interrupts the flow of data at the termination of a data character, then starts the control sequence. However, this interruption does not occur between end-of-text and longitudinal-redundancy-check characters or between synchronization characters and the first character to be transmitted.

When it senses the record mark in memory, the communication control recognizes the end-of-control sequence and releases the read/write channel. In full-duplex operation the Type 281-2F returns to transmission of the data it was originally handling.

(2) Transmitter

In half-duplex operation the transmitter sends one of three control characters: the enquiry (ENQ) character, the end-of-transmission (EOT) character, or the telephone request (TEL REQ) character.

(a) Enquiry (ENQ)

The enquiry character issued to a remote terminal signifies that no response has been received for the last transmitted data block. This situation may arise when the remote terminal has not sent the control sequence in time or when noise — or other line interference — has overridden the control sequence. The enquiry control character always asks the remote terminal to "please retransmit your last control sequence." The meaning of this signal is slightly modified in the "initialization" condition, when the transmitter is attempting to establish contact; then it signifies "please transmit an ACK control character if you are ready to receive."

(b) End of Transmit (EOT)

The end-of-transmit control character tells the remote receiver that the transmitter has terminated data transmission. The end-of-transmit character is recognized by the transmitter's communication control, which starts the timer. If the remote terminal does not respond with an ACK or NAK character within 100 milliseconds, the timer indicates it has "timed-out."

The enquiry character is normally sent onto the line in response to a "time-out." In the case of an end-of-transmit character, however, the program retransmits EOT until ACK is received or until the transmitter no longer receives confirmation.

(c) Telephone Request (TEL REQ)

This character is sent after the transmission of a complete data block. It signals for operator intervention in situations which can not be handled by programming. When the telephone request character is sensed and acknowledged, the operators may switch to the talk mode and converse.

Since all three above-mentioned control characters pertain to data transmitted, they are known as transmitter control characters.

Transmitter control characters are transferred to to the communication control by means of a PDT instruction using the same C3 control character as that used for the receiver control characters, that is, octal 40. However, the transmitter control characters use the transmitter read/write channel and the logical line address (0t) of the transmitter. If — in a full-duplex operation — transmitter or receiver control characters are used with improper read/write channels and incorrect line addresses, the results are unspecified. Control character configurations are given in Table I, page 4.

When full-duplex operation is in effect, a precise control sequence and control-character bit configuration is specified by the remote terminal receiver to facilitate insertion of a control sequence in the midst of data (Section VI, D, 4, b, (1). When permanent half-duplex operation is in effect, flexibility may be attained by accomplishing control character recognition through programming. In this latter case, the control sequence can be implemented in any format using the "Control" PDT instruction. A programmer may thus select any suitable format and choose the control characters. Any control characters which may be varied by jumper cards are listed in Section IV, C, 3.

5. Reception

a. Data

When receiving data, a PDT instruction is issued to the receiver using the read/write channel associated with the receiver as the C1 control character and the logical line address (4t) as the C2 control character. The C3 control character depends upon these considerations: Is the code ASCII, Honeywell, or Univac? Is the single-frame demand or the two-frame demand used for storing data? Is there a parity check?

For proper communication, the receiver C3 control character must be the same as that used by the transmitter for the "Transmit Data" PDT instruction.

(1) ASCII Code

When the ASCII code is used, the C3 control character must specify a two-frame demand and a parity check.

(2) Other Eight-Bit Codes

Parity generation must match the conditions at the other terminal and so may be inhibited or permitted.

(3) Honeywell Code

If the same C3 control character is used by both the receiver and transmitter to signify the use of the Honeywell code, the incoming character is checked for parity and bits 8 and 7 are filtered by the communication control. Bits 6 through 1 are sent to memory to fill one character location. The end-of-text character is received as a six-bit character.

(4) Univac Code

The procedure described in step (3) above applies also in the Univac mode of operation.

Regardless of the operational mode, synchronization characters and longitudinal-redundancy-check characters are not transferred to memory.

b. Control

Legal control sequences recognized by the Type 281-2F cause setting of a specific status bit and an Interrupt function. Control sequences are usually not sent into memory.

As described in Section VI, D, 4, b, when a system operates permanently in the half-duplex mode, control information may be sent in the same manner as data, providing the sequence is one which the Type 281-2F "built-in" logic does not recognize and filter from the received information. If not filtered, the control sequence is sent into memory and becomes data to be interrogated by the program.

c. Status

Whenever the transmitter interrupts, the transmitter status register contains the information pertaining to the interrupt. A PDT instruction issued to the transmitter on the associated read/write channel reads the status information. The logical

address of the transmitter (0t) and a C3 control character of octal 20 signifies that status information is requested from the transmit status register. This information is stored in the location specified in the A address of the PDT instruction.

Similarly, to read receiver status information, the PDT instruction is issued with the same C3 control character of octal 20, except that the receive read/write channel and the receiver logical address (4t) are utilized.

The PDT instruction resets the status register tested. The significance of the various bit settings in the status register is discussed in Section VI, D, 6 and shown in Tables IV and V, pages 10 and 11, respectively.

6. Interrupt Processing

In order that the line may be utilized to its maximum capacity, interrupt processing should be as brief as possible. Operations such as character translation and transfer to storage or transfer from storage are accomplished in the noninterrupt mode while the communication lines are busy.

When an interrupt occurs, the "transmit" and "receive" Interrupt functions are tested by Peripheral Control and Branch instructions to determine which is set. In full-duplex operation, both the receiver and transmitter sides of the register may be set; in this case, they must be serviced in turn. Otherwise there is no difference between servicing interrupts in full-duplex or half-duplex operation with the Honeywell or ASCII codes.

a. Transmit Status Register

When the "transmit" Interrupt function is set, a PDT instruction reads the transmit status into memory, as described in Section VI, D, 5, c. This instruction uses the transmitting read/write channel, the logical line address of the transmitter (0t), and the C3 control character of octal 20. Each status bit is questioned.

The bits stored in the transmit status register pertain to the last data block transmitted and are described as follows (Table IV, page 12).

Bit 1: Setting of bit 1 signifies that an acknowledge signal is received in response to the last data block sent. A new PDT instruction must be issued to transmit the next data block.

Bit 2: Setting of bit 2 indicates that a negative-acknowledge character is received in response to the last data block sent. A PDT instruction must be issued requesting retransmission of the same data block.

Bit 3: The Type 281-2F sets bit 3 when a wait-before-transmit signal is sent by the remote receiver. This signal is repeated periodically and the transmitter can not issue any "Transmit" PDT instructions until it receives an ACK or NAK character; then it resumes transmission, as it would upon setting of bit 1 or 2.

Bit 4: Setting of bit 4 indicates that data has overflowed the allocated buffer area and the communication control has sensed a record mark in memory, although it has sensed no end-of-text character. The setting of bit 4 is caused if the program is not certain the last data-block character is a legal end-of-text character (or end-of-text character plus record mark in Honeywell code), or if an insufficient buffer area was allocated. The program must rectify the error before any "Transmit" PDT instructions may be issued.

When the record mark is sensed in memory, the Type 281-2F inhibits a frame demand, forces a legal end-of-text character over the line, and follows it with a bad longitudinal-redundancy-check character. It also sets bit 4 of the transmit status register, releases the read/write channel, and sets the Interrupt function.

The bad longitudinal-redundancy-check character causes the remote terminal to return a negative-acknowledge signal resulting in a retransmission of the block of data.

Bit 5: Bit 5 is set when the timer "times-out" because a response was not received from the remote terminal or was not recognized within a specified time. Normally the response to a "time-out" interrupt is the issuance of an enquiry character to be interpreted by the remote terminal as "please repeat your last control sequence." However, if the "time-out" occurs after the transmitter has sent an end-of-text message, then the end-of-text block must be retransmitted.

In any case, the transmitter program should send the enquiry or end-of-text signal a specific number of times before deciding that the remote terminal has been rendered incapable of responding.

Bit 6: The bit 6 position is currently unassigned.

If the "receiver" Interrupt function is set, a PDT instruction reads the receiver status into memory, using the receiver read/write channel, the logical line address 4t, and the C3 control character octal 20.

b. Receive Status Register

The following status is stored in the receive status register (Table V, page 11).

Bit 1: Bit 1 is set when a data block having no detectable parity error is received. An acknowledge signal responds to such a transmission and a "Receive" PDT instruction must be reissued.

Bit 2: Setting bit 2 indicates the reception of a data block exhibiting bad parity, a bad longitudinal-redundancy-check character, or an overwrite condition. A negative-acknowledge signal must be sent and the "Receive" PDT instruction reissued.

Bit 3: The reception of an enquiry signal sets bit 3. In response, the last transmitted control sequence is repeated. The correct receiver read/write channel and logical line address (4t) must be used.

Bit 4: Setting bit 4 indicates that the received data block has overflowed its allocated area. Having sensed a record mark in memory, the Type 281-2F sets the status bit and the Interrupt function and releases the read/write channel. This error occurs if a valid end-of-text character is sent but goes unrecognized because of noise or if no valid end-of-text message is sent. A negative-acknowledge signal responds to this error. If the error persists, the program may implement a telephone-request signal.

Bit 5: Setting of bit 5 indicates that a telephone request is being made. An acknowledge signal answers and the ensuing telephone call is responded to in the talk mode.

When the "transmit" Interrupt function is set, the transmitter read/write channel is freed for utilization by the PDT instructions. The PDT instructions bringing in the status and sending the response use the transmitter read/write channel and its logical line address (0t).

Bit 6: Bit 6 is set by the reception of an end-of-transmit control sequence. When the program finishes the transmission of data blocks and sends an end-of-transmit signal which is acknowledged, it realizes — unless transmission is returned from the other end — that communication is temporarily completed. The operator may therefore choose to release the read/write channels for other use.

Conversely, when the "receive" Interrupt function is set, the receiver read/write channel is freed. All PDT instructions bringing in status, sending responses, or reissuing "Receive" use the receiver read/write channel and logical line address (4t).

The direction of data flow between the central processor and the Type 281-2F is determined by bit 6 of the C2 control character and by the C3 control character.

7. Record Marks in Memory

a. Transmitter

A transmitter must have record marks in three different locations in memory:

(1) On the last character of a control sequence, indicating its termination;

(2) On the character containing the last six bits of the end-of-text character when transmitting data in the Honeywell six-bit code (here the record mark and the end-of-text character combine to signal a return to the eight-bit mode of operation);

(3) Approximately two characters beyond the last location in the buffer area as protection against transmitting the entire memory because of lack of an end-of-text character or an end-of-text/record mark combination. If a record mark is sensed with no end-of-text character, the Type 281-2F gives the error condition cited in VI, D, 4.

b. Receiver

A receiver must have record marks in two different memory location — either on the last character of a receiver control sequence or approximately two characters beyond the buffer allocated for reception of the largest data block (Section VI, D, 5).

8. Timer

The Type 281-2F timer "times out" between 100 and 200 milliseconds. The Type 281-2F starts the timer automatically upon recognizing a programmed PCB instruction, an end-of-text character, or an end-of-transmission character.

Recognition of a control sequence of two successive, identical control characters specifying acknowledge, negative-acknowledge, or wait-before-transmit stops the timer, as does a PCB instruction or a "time-out."

E. Termination of Communications

When it has completed data transmission, the transmitting terminal sends an end-of-transmission control sequence, which must be acknowledged. If this sequence is not acknowledged, it must be repeated at least three times so that the remote terminal may understand it. When it is acknowledged, no further transmission occurs on the line. In the half-duplex mode of operation, this signals the end of communication. In the full-duplex mode of operation, the end of transmission must likewise be signalled on the other communication line.

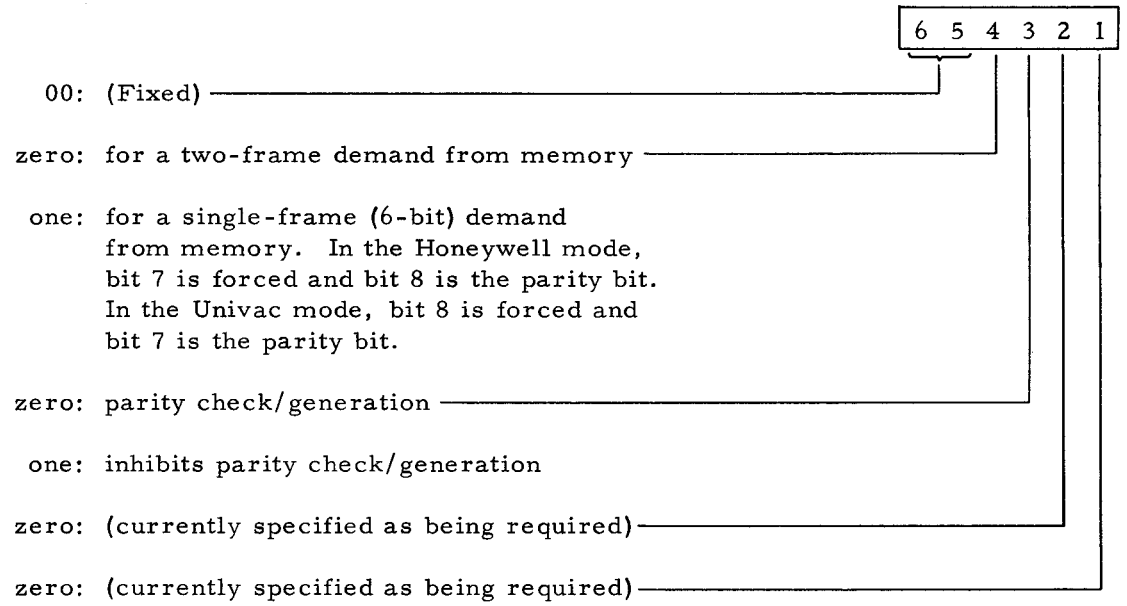
F. Peripheral Control and Branch (PCB) Instruction Format and Coding

The Peripheral Control and Branch instruction format for the Type 281-2F is given in Section 8 of the Models 200/1200/2200 Programmers' Reference Manual. The test and control functions defined by control character C3 are summarized in Table VI, page 25.

G. Peripheral Data Transfer (PDT) Instruction Format and Coding

The Peripheral Data Transfer instruction format for the Type 281-2F is given in Section 8 of the Models 200/1200/2200 Programmers' Reference Manual. The PDT control character coding is given below:

1. To Transmit or Receive Data



2. To Transmit a Control Sequence

   a. To generate parity in the Type 281-2F, the C3 control character is octal 40.

   b. To inhibit parity generation, the C3 control character is octal 44.

3. To Bring in Status Information

   Status information is brought in when the C3 control character equals octal 20. "Transmit" status is brought in if the unit indicator bit of the C2 control character is "zero."

   "Receive" status is brought in if the unit indicator bit of the C2 control character is a "one."

The PDT instruction for receiving data at the receiving end must have the same control character as the PDT instruction for transmitting data at the transmitting terminal.

The action of the Type 281-2F on an illegal or meaningless C3 control character is unspecified.

NOTE

The proper direction of data transfer between central processor and the communication control is not only determined by bit 6 of the C2 control character; it is also dictated by the C3 control character which determines whether this is a "Data," "Control," or "Status" PDT instruction.

VII. TEST MODE

At the user's request, the telephone company provides the Bell DATA-PHONE Dataset 301B with a line and test key. This key turns the data around within the

dataset to allow off-line testing of the unit. Datasets used with the Type 281-2F must be provided with this key for test purposes.

Table VI. PCB C3 Character Coding

INSTRUCTION	DESCRIPTION	C3 (OCTAL)
	Branching	
Device Busy	Is the communication control busy? If "yes," branch to A address. If "no," program continues in sequence.	10
Interrupt	Did unit specified in C2 control character interrupt? If "yes," branch to A address. If "no," program continues in sequence. To check for "transmit" Interrupt, use 0t as line address in C2, for "receive" use 4t (t is peripheral address).	75
	Non-Branching	
Set Allow Function	Allow function in communication control is set; the line is specified in C2.	71
Reset Allow Function	Allow function in communication control is reset; the line is specified in C2.	70
Reset Interrupt Function	Interrupt function in communication control is reset. Line is specified in C2.	74
Start Timer	Starts timer in communication control.	62
Stop Timer	Stops timer in communication control.	63

NOTES:
1. Both Allow and Interrupt funtions in the communication control must be set in order for the central processor to interrupt.
2. If a "Set Allow" PCB instruction is issued and an interrupt condition is set, the Type 281-2F interrupts immediately.
3. The PCB "Set Allow" instruction permits data to be received from the line. All on-line data is ignored until this PCB instruction is issued. For this reason, both transmitter and receiver interrupts are allowed — even in half-duplex operation — so that all control characters must be entered.

APPENDIX A

UNIVAC MODE OF OPERATION

The general characteristics of the Type 281-2F described in the preceding pages also apply for operation in the Univac mode. However, certain special requirements are given below:

A. Message Format

1. Data

5 Synchronization Characters	Data	End-of-Block Character	LRC Character

2. Control

5 Synchronization Characters	Data	End-of-Mode Character

The control character recognition and action generated is shown in Table A-I, page A-3. The control sequence and the action taken upon it by the Type 281-2F is described below under "Control Sequence."

3. Termination

5 Synchronization Characters	End-of-Transmit Character	LRC Character*

In Univac-mode operation, the synchronization character is 10000000, and the end-of-mode character is 10010000. Both the end-of-block character and the end-of-transmit character are selected by jumper cards. Bit 8 is always a "one." Bit 7 is the parity bit generated by the communication control except on the synchronization character.

B. LRC Computation

LRC computation in the Univac mode of operation includes all data characters and the end-of-block character. It does not include the control characters and end-of-mode character. Each bit in the LCR character except the eighth is a half-add sum of all the bits in the same position in all the characters of the message. Bit 8 is a "one."

C. Beginning Communication

The following decisions must be made prior to data transmission.

a. One of the two units (DLT2B or Type 281-2F) must be designated the master unit and the other the slave unit.

b. This relationship remains the same for the installation for all communication transactions.

c. The master unit sends the slave unit a "bid" message instructing it to be the transmitter or receiver for that transmission.

*The program-supplied LRC characters is the same as the EOT character.

d. The slave unit sends back a "connect" message. It instructs the master unit to be the receiver or transmitter depending upon the instruction in the bid message.

e. The units switch to the modes thus determined and start operating.

1. Format of "Bid" Message

5 Synchronization Characters	An "Instruction" Character	End-of-mode Character

The instruction character instructs the slave to be:

a. a transmitter — 1P000100

b. a receiver — 1P000001

2. Format of "Connect" Message

5 Synchronization Characters	Instruction Character	End-of-mode Character

Bid and connect messages do not stop the timer upon reception of a connect message; therefore the program must issue a "Stop Timer" PCB instruction to prevent a "time-out" interrupt.

D. Univac "Non-Reference" Character

If the DLT2B's request to transmit is active and main memory is not being accessed for transmission of synchronization or message characters, then the DLT2B has the automatic ability to generate and transmit a series of "non-reference" characters (10000111). The Type 281-2F takes no action on this character, except to filter it from information sent to main memory. Its presence — having no effect on Type 281-2F operation — is ignored.

E. Parity on Univac Synchronization Character

The Univac synchronization or "reference" character has all "zeros" in bit positions 1 through 7 and a "one" in bit position 8. Therefore, since it does not obey parity rules, a Univac synchronization character should not be checked for parity.

F. Status Indication

The status indication is the same as in the Honeywell mode of operation, Tables A-II and A-III. Some bits are redefined and the WBT bit is not used. TEL and ENQ are not available in the Univac mode with the Type 281-2F. Also, the Univac DLT2B is a half-duplex unit, and the half-duplex mode of operation must be used in referring to programming or operations.

G. Six-Bit Mode

With the proper C3 control character, the data is stored in memory in 6-bit characters. The C3 control character causes the Type 281-2F to draw one frame per transfer following the first non-synchronization character. The programmer must be certain that the first character following the synchronization character is in eight-bit (2-character) mode. This mode also generates parity on bit 7 and forces bit 8 to be a "one" to make eight bits on the line. To leave this mode, the last character must be the last six bits of the Univac end-of-block character with a record mark. Control characters are the full 8-bit Univac control characters (see Table A-I).

NOTE

A communication control can not switch from Honeywell or ASCII mode into Univac mode or vice versa by means of programming. The switch in operational mode is effected by jumper cards.

H. Control Sequence

In the Univac half-duplex mode of operation, a control sequence is established including at least five synchronization characters and a control character, followed in immediate sequence by an end-of-mode character. The end-of-transmit sequence is an exception and is dealt with separately.

Two successive synchronization characters are used by the Type 281-2F to obtain synchronization. Any SYNC character recognized thereafter is filtered. Once the Type 281-2F is in synchronization, the sequence of one control character followed immediately by an end-of-mode character will be recognized by the communication control as a control sequence. The Type 281-2F sets the status corresponding to the control character received, then interrupts. If a "Receive" PDT instruction is active at this time, the control character is transferred to memory at the location indicated by the read/write channel current location counter; the end-of-mode character is filtered.

The control characters recognized by the Type 281-2F are ACK, NAK, Instruction character (transmit), and Instruction character (receive). The last two are used in "bid" messages and "connect" messages as described above. These characters are uniquely defined, as is the end-of-mode character. Note, however, that the design of the Type 281-2F allows the end-of-mode character to be selected by jumper card.

Any of the control characters may be used as a data character as long as it is not followed by an end-of-mode character. The end-of-mode character may also be used as a data character as long as it is not preceded immediately by a control character. The data block must not contain a sequence of two characters that will have the same configuration as one of the above control characters followed by the end-of-mode character. If this should happen, the control status will be set, the unit will interrupt, and the read/write channel will be released. The sequence is therefore considered illegal.

I. End-of-Transmit Sequence

The end-of-transmit control sequence is different from the other control sequences in that the end-of-transmit (EOT) character is followed by an LRC character and not by an end-of-mode (EOM) character. The LRC character in this case is identical to the EOT character since it is a two-character sequence. The Type 281-2F therefore recognizes a sequence of two identical EOT characters as an EOT sequence.

The EOT character can also be used as a data character, providing two EOT characters are not used in immediate succession.

It should be noted that a non-reference character in the middle of the control sequence is ignored. Thus, a sequence of control character, non-reference character, and then an end-of-mode character is still considered a legal control sequence. Similarly, two EOT characters separated by non-reference characters still constitute a legal EOT sequence.

Table A-I. Communication Control Action on Control Characters in Univac Mode

NO.	SYMBOL	NAME	CODE (8 BIT) 87654321	NUMBER REQUIRED	CONTROL UNIT ACTION
1	SYNC	Reference Character	10000000	5	Achieves synchronization. All subsequent characters after synchronization are sent to the central processor.
2	ACK	Acknowledge	10000010	1	Filtered*. Sets interrupt.
3	NAK	Negative Acknowledge	10100000	1	Filtered*. Sets interrupt.
4	EOM	End-of-Mode	10010000	1	Filtered.
5	EOB	End-of-Block	See Notes	1	Sent to CP. Causes interrupt.
6	EOT	End-of-Transmission	See Notes	1	Interrupt, Filtered*.
7	LRC	Longitudinal Record Check	--------	1	Filtered.

NOTES:
1. The end-of-block character is selected by jumper card.
2. The end-of-transmission character is selected by jumper card.
3. Bit 7 is parity.
4. Bit 8 must always be a "one."
5. See also "Format of Bid Message" and "Format of Connect Message" above for two additional characters recognized and filtered by the central processor.

*6. ACK, NAK and EOT may be sent to the central processor if a "Receive" PDT instruction is active at the time these are received.

Table A-II. Transmit Status Register for Univac Mode

BIT NUMBER	STATUS	RESPONSE
1	Acknowledge	PDT instruction data for the next block to be issued
2	NAK	PDT instruction data for the same block (retransmit)
3	Not Used	
4	Record Mark	Correct error, wait for NAK
5	Time-Out	As determined for the installation

NOTE: All PDT's use transmitter RWC and logical line address 0t.

Table A-III. Receive Status Register for Univac Mode

BIT NUMBER	STATUS	RESPONSE
1	Received Good Block	PDT Control — ACK
2	Received Bad Block	PDT Control — NAK
3	Instruction Character — Receiver*	
4	Record Mark	PDT Control — NAK
5	Instruction Character — Transmitter*	
6	End-of-Transmission	PDT Control — ACK

NOTES: 1. In all cases, reissue PDT instruction; receive data after response.

2. All response PDT's use receiver RWC and line address (4t).

*3. See "Format of Bid Message" and "Format of Connect Message" above.

HONEYWELL EDP TECHNICAL PUBLICATIONS
USERS' REMARKS FORM

TITLE: SERIES 200
TYPE 281-2F SINGLE-CHANNEL
COMMUNICATION CONTROL
HARDWARE BULLETIN

DATED: MAY, 1966

FILE NO: 112.0005.1100.0-216

ERRORS NOTED:

Fold

Cut Along Line

SUGGESTIONS FOR IMPROVEMENT:

Fold

FROM: NAME _____ DATE _____

COMPANY _____

TITLE _____

ADDRESS _____

_____

FIRST CLASS
PERMIT NO. 39531
WELLESLEY HILLS
MASS.

BUSINESS REPLY MAIL

No postage stamp necessary if mailed in the United States

POSTAGE WILL BE PAID BY

HONEYWELL
ELECTRONIC DATA PROCESSING DIVISION
60 WALNUT STREET
WELLESLEY HILLS, MASS. 02181

ATT'N: TECHNICAL COMMUNICATIONS DEPARTMENT

Cut Along Line

Honeywell
ELECTRONIC DATA PROCESSING

CRP