HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

PRELIMINARY

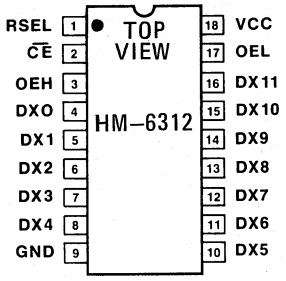
HM-6312/6312A

CMOS ROM
1024 WORD x 12 BIT

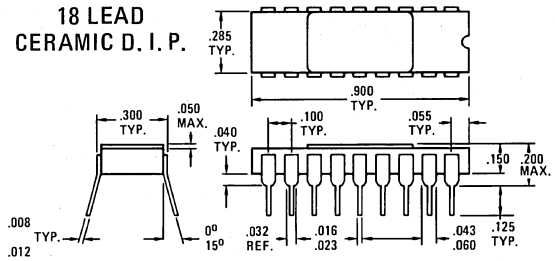
FEATURES

- HM-6100 COMPATIBLE
- LOW POWER - TYP. $<5.0\mu W$ STANDBY
- 4 - 11 VOLT V_{CC} OPERATION
- HIGH SPEED
- STATIC OPERATION

PINOUT/PACKAGE



18 LEAD CERAMIC D. I. P.



NOTE: Board drilling dimensions will equal standard practice for .020 diameter lead.

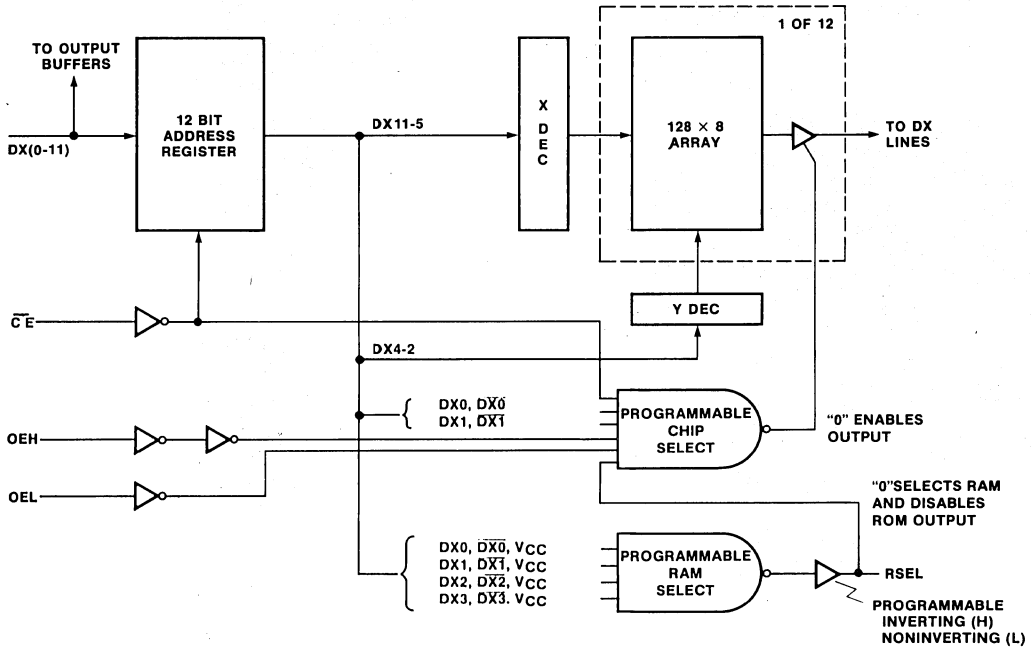
DESCRIPTION

The HM-6312 and HM-6312A are high speed, low power, silicon gate CMOS static ROM's organized 1024 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. The basic part operates at 4 - 7 Volts with a typical 5 Volt 25°C access time of 350 ns. Higher operating voltages, 4 - 11 Volts, are available with the A version. Signal polarities and functions are specified for interfacing with the HM-6100 Microprocessor.

OPERATION

Addresses and data out are multiplexed on 12 lines, DX0 - DX11. Addresses are loaded into an on chip register by the falling edge of $\overline{CE}$. Data out, corresponding to the latched address, is enabled when $\overline{CE}$ and OEL are low and OEH is high and the decoded state of DX0 and DX1 are true. The RSEL output defines an area in the 4096 word addressing space dedicated to RAM. It can be programmed by DX0, DX1, DX2, and DX3. This output eliminates a four bit register and decoder for the high order address bits to select RAM.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Supply Voltage HM-6312	+ 8.0V
Supply Voltage HM-6312A	+ 12.0V
Applied Input or Output Voltage	GND - 0.3V to V_{CC} + 0.3V
Storage Temperature Range	
Industrial HM-6312/6312A-9	- 40°C to + 85°C
Military HM-6312/6312A-2	- 55°C to + 125°C

D. C. CHARACTERISTICS V_{CC} = 4-7V (HM-6312); V_{CC} = 4-11V (HM-6312A)

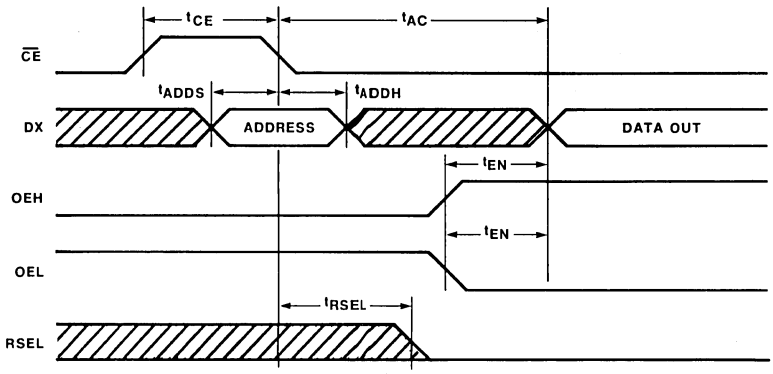
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Logical "1" Input Voltage	V_{IH}	70% V_{CC}			V	
Logical "0" Input Voltage	V_{IL}			20% V_{CC}	V	
Input Leakage	I_{IL}	-1.0		+1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
Logical "1" Output Voltage	V_{OH}	V_{CC}-.01			V	I_{OUT} = 0
Logical "0" Output Voltage	V_{OL}			GND + .01	V	I_{OUT} = 0
Output Leakage	I_O	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
Supply Current	I_{CC}		1.0		μA	V_{IN} = 0 or V_{CC}
Input Capacitance*	C_{IN}		5.0	7.0	pF	
Output Capacitance*	C_{OUT}		6.0	10.0	pF	

*Guaranteed and sampled, but not 100% tested.

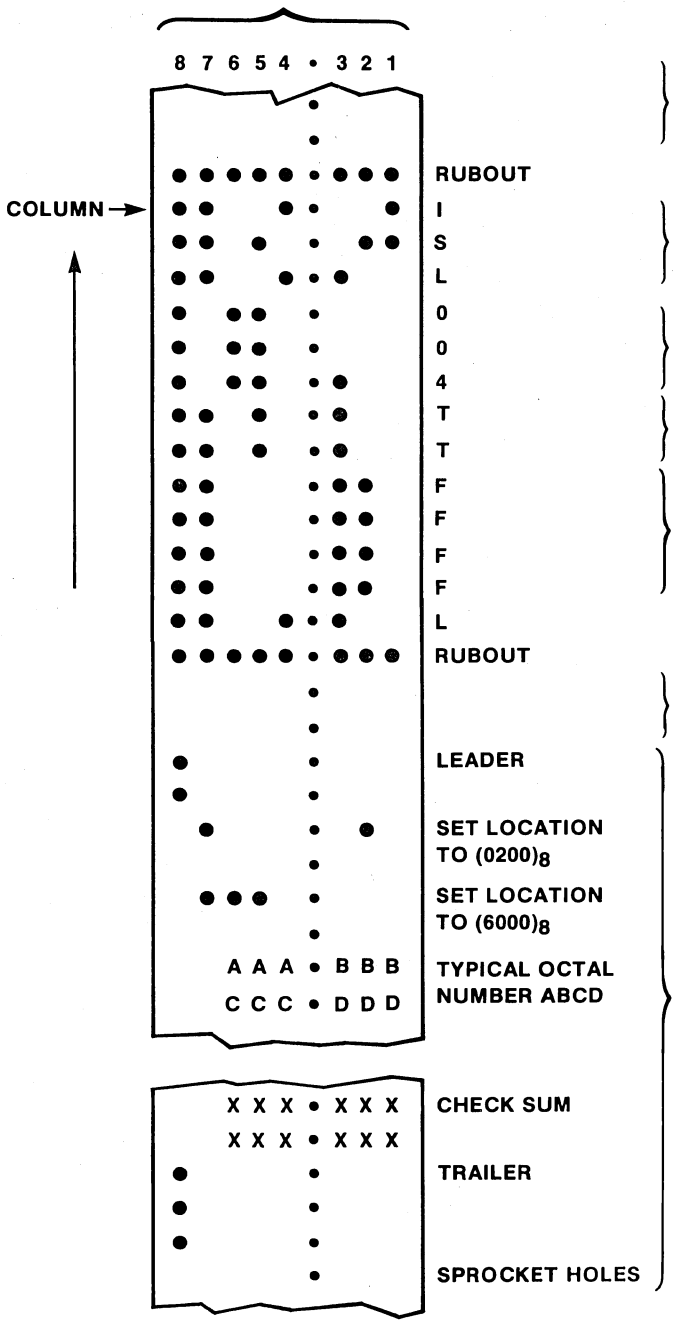
A. C. CHARACTERISTICS T_A = 25°C, C_L = 50pF

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Access Time From CE	(6312)	t_{AC}		500		ns	V_{CC} = 5.0V
	(6312A)			250		ns	V_{CC} = 10.0V
Output Enable Time	(6312)	t_{EN}		250		ns	V_{CC} = 5.0V
	(6312A)			125		ns	V_{CC} = 10.0V
Strobe Positive Pulse Width	(6312)	t_{CE}		220		ns	V_{CC} = 5.0V
	(6312A)			110		ns	V_{CC} = 10.0V
Address Set-Up Time	(6312)	t_{ADDS}		50		ns	V_{CC} = 5.0V
	(6312A)			25		ns	V_{CC} = 10.0V
Address Hold Time	(6312)	t_{ADDH}		50		ns	V_{CC} = 5.0V
	(6312A)			25		ns	V_{CC} = 10.0V
Propagation To RAM Select	(6312)	t_{RS}		250		ns	V_{CC} = 5.0V
	(6312A)			125		ns	V_{CC} = 10.0V

SWITCHING WAVEFORMS



HM-6312/6312A programming information is generated from the PAL III Symbolic Assembler as a "second pass" binary tape. A separate tape is required for each 1024 word ROM pattern, i. e. a separate symbolic should be generated for each 1024 word block of memory used, $(0000\text{-}1777)_8$, $(2000\text{-}3777)_8$, $(4000\text{-}5777)_8$ and $(6000\text{-}7777)_8$. A header is added to the front of each tape giving customer ID, chip select and RAM select programming information. The header consists of 15 ASCII characters generated from a standard teletype. Channel 8 is always punched. The header begins with a rubout followed by 6 alphanumeric characters identifying the customer and the pattern number. Next are 2 letters designating true, false or don't care for inputs DX0 and DX1 to chips select gate A (see functional diagram), and 4 letters designating true, false, don't care for inputs DX0, DX1, DX2, and DX3 to the RAM select gate B (see functional diagram). Next is one letter (H or L) designating RSEL as active high or active low. RSEL function is inhibited when all RSEL inputs are V_{CC} and RSEL is active high. The leader ends with a rubout.



COMMENTS

SPROCKET HOLES

BEGIN HEADER

3 LETTER CUSTOMER ID
(A–Z, 0–9) ARE ALLOWABLE

3 NUMBER CUSTOMER PATTERN NUMBER
(A–Z, 0–9) ARE ALLOWABLE

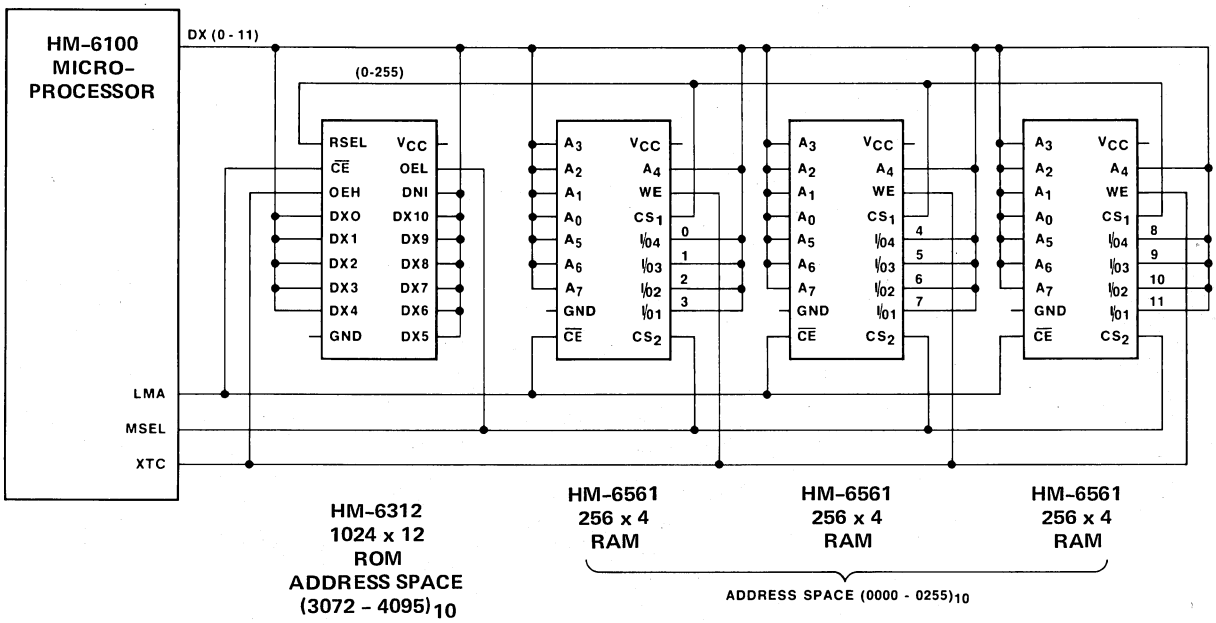
DX0 CHIP SELECT PROGRAMMING
DX1 T–TRUE, F–FALSE
DX0
DX1 RAM SELECT PROGRAMMING
DX2 T–TRUE, F–FALSE, V–DON'T CARE
DX3
RSEL IS ACTIVE LOW
END HEADER

SPROCKET HOLES

PAL III Symbolic Assembler "second pass" output is of this form. Channel 8 only, punches indicate leader or trailer. An address is designated by a punch in channel 7. 12 bits of data are represented by two adjacent columns. DX0-DX5 are represented by channels (6–1) in the first column. DX0–11 are represented by channels (6–1) in the second column.

The example shown above has a customer ID and pattern ISL 004. Chip selects are programmed to recognize addresses $(6000\text{-}7777)_8$ or $(3073\text{-}4095)_{10}$. RAM select is active low for addresses $(0000\text{-}0400)_8$ or $(0000\text{-}0255)_{10}$. For programs using less 1024 words, the unused locations are automatically programmed to a logic one.

A MINIMAL MICROPROCESSOR SYSTEM



ORDERING INFORMATION

HM 1 - 6312 A - 2

HARRIS

DEVICE NUMBER

TEMPERATURE:
2: -55°C to +125°C
9: -40°C to +85°C

PACKAGE CODE

VERSION:
A: 10.0V Nominal
BLANK: 5.0V Nominal

SALES OFFICES –

SUITE 103
4014 LONG BEACH BLVD.
LONG BEACH, CALIF. 90807
(213) 426-7687

SUITE 230
1032 ELWELL COURT
PALO ALTO, CALIF. 94303
(415) 964-6443

SUITE 100
15 SPINNING WHEEL ROAD
HINSDALE, ILL. 60521
(312) 325-4242

SUITE 301
177 WORCESTER STREET
WELLESLEY HILLS, MASS. 02181
(617) 237-5430

SUITE 132
7710 COMPUTER AVENUE
MINNEAPOLIS, MINN. 55435
(612) 835-2505

3215 E. MAIN STREET
ENDWELL, N. Y. 13760
(607) 754-5464

535 BROADHOLLOW ROAD
MELVILLE, L. I., N. Y. 11746
(516) 249-4500

SUITE 220
333 WEST FIRST STREET
DAYTON, OHIO 45402
(513) 226-0636

SUITE 325
650 E. SWEDESFORD ROAD
WAYNE, PENN. 19087
(215) 687-6680

SUITE 7G
777 S. CENTRAL EXPRESSWAY
RICHARDSON, TEXAS 75080
(214) 231-9031

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