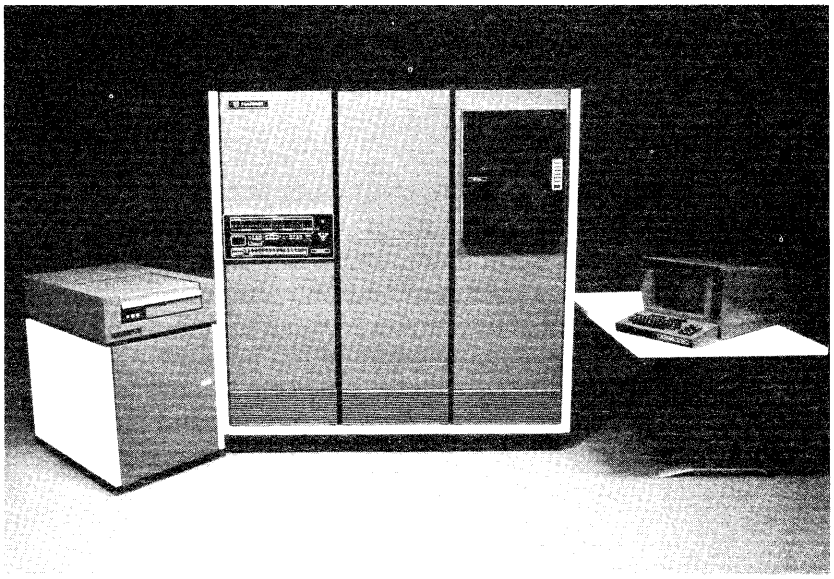
HARRIS 500

Computer System

FEATURES

- **Hardware supported virtual memory system**
- **Over 3 million bytes of main memory**
- **High-speed central system bus**
- **Field-proven hardware and software**
- **Multiple, concurrent functions**
  - **—Interactive time-sharing**
  - **—Multi-stream batch**
  - **—Multiple Remote Job Entry (Host and Workstation)**
  - **—Sensor-based/real-time processing**



HARRIS 500 COMPUTER

The Harris 500 is the middle member of the Harris family of software compatible, virtual memory computers which include the Harris 100 and Harris 800 computer systems.

Features of the Harris 500 include:

- Maximum of 19 million bytes per second system bus transfer rate
- Over 3 million bytes of directly addressable real memory
- Over 12 million bytes of virtual memory space
- Optional, hardware floating point arithmetic
- Hardware supported virtual memory system
- Up to 64 interactive user terminals
- Error correcting main memory
- 6 K bytes high-speed, bipolar cache memory
- Field-proven hardware

The Harris 500 is offered with a complete line of peripherals and maintenance support.

MULTI-USE AND MULTIPLE USERS

The Harris 500 computer system is designed for high performance in a wide range of uses encompassing scientific or engineering applications together with business applications. These processing requirements demand multiple languages, the accommodation of many users, and both local and remote operations. Harris has developed a unique synergy of computer hardware and software to meet these needs.

The Harris 500 computer system supports concurrent users doing interactive program development, time-sharing, multi-stream batch, multiple remote job entry and real-time processing. The Harris operating system, VULCAN, is reentrant, thus permitting one copy to be shared by all users. The VULCAN language processors, (except the overlay versions) are also reentrant and, compiler-generated code optionally can be reentrant.

The Harris 500 multi-use and multiple user system is an ideal solution to the processing requirements of a multi-disciplined organization.

CENTRAL PROCESSOR

The Harris 500 computer is designed around a very fast central system bus for maximum system performance in a multiprogramming environment.

The system bus is capable of an aggregate transfer rate of 19 million bytes per second. The system bus has 48 lines for data transfers and 20 lines for addressing. The address bits allow the full 3072 K bytes of main memory to be accessed by any subsystem using the bus. On writes to main memory, the system bus transfers the memory address together with 24 or 48 data bits in one bus cycle. Typically, input/output operations transfer 48 data bits at one time between main memory and discs or tapes on the Universal Block Channel via the system bus.

The Harris 500 central processor overlaps instruction fetch with execution. While one instruction is being executed, the next sequential instruction is fetched from main memory. The instruction set is compatible with the Harris 100 and Harris 800 computers.

An Operator Console CRT (OPCOM) provides for

communications between the operating system—VULCAN and the system operator.

SCIENTIFIC ARITHMETIC UNIT (SAU)

The Harris 500 features an optional, hardware floating point processor. The Scientific Arithmetic Unit provides concurrent floating point operations independent of the central processing unit. The SAU interface transfers 48 bits to or from main memory on the system bus. Double-precision (48-bit) floating point employs an 8-bit signed exponent and 39-bit signed mantissa, resulting in over 11 decimal digits of precision.

MEMORY SYSTEMS

Virtual Memory

Ease of use is a primary benefit of a virtual memory system. On the Harris 500, users can write programs that are larger than the real memory of the system. Over 12 million bytes of logical address space are available for running application programs regardless of the physical memory available.

The Harris 500 is a demand-paged system supported by the VULCAN virtual memory management operating system. Hardware supporting VULCAN's virtual memory capabilities includes a variety of registers to decrease the burden of housekeeping requirements.

The Harris virtual memory system provides hardware and software memory protection. Every program page in memory is protected against access or inadvertent destruction by another concurrently executing program. In addition, pages containing instructions and constants, as opposed to variable data, are hardware write-protected, even within the same program.

Virtual memory allows programs to execute with only part of the code in real memory. Demand-paging causes the sytem to load blocks or "pages" of code and data into memory as required by a program to continue executing. In the Harris 500 system, a program "page" is 3072 bytes.

Another feature of the the Harris 500 virtual memory system is efficient use of real memory. A program need not occupy contiguous memory pages. Any physical page not occupied by the operating system can hold any logical page. Memory, therefore, never needs reorganizing or compacting.

A combination of hardware and software features serve to minimize the amount of swapping that may occur in a high system usage environment. The Harris virtual memory hardware includes Virtual Usage Registers and Virtual Not-modified Registers. These registers are used by the VULCAN swapping algorithm to identify the most eligible memory pages for swapping.

The Harris sytems have high-speed program loading. Program loading is simply and quickly accomplished by copying program pages directly from disc into memory with no address modification. The Harris virtual memory hardware associates each logical address in the program page with its physical location.

Main Memory

The main memory of the Harris 500 is expandable to over three million bytes (3,145,728 bytes) in 192 K byte modules. Each memory module has its own timing and control logic, and reads or writes 48 bits plus error correcting bits in one memory cycle. The memory cycle time for 48 bits is 400 nanoseconds, and access time is 290 nanoseconds. To achieve high system throughput, each memory module transfers 48 data bits on the system bus to the central processor, cache memory, and some input/output channels.

Cache Memory

The Harris 500 computer includes 6 K bytes of high-speed cache memory. The cache memory cycle time is 150 nanoseconds with an access time of 70 nanoseconds. Although the effectiveness of cache is dependent on the nature of the executing programs, typically, the cache hit ratio will be 90% or better.

The cache memory is partitioned, allocating 3 K bytes for operands and 3 K bytes for instructions. The cache reads or writes 48-bit data fields in one cache memory cycle. Each 48-bit data field has two additional bits to indicate the validity of the stored data. I/O writes to main memory are not written in the cache, however, the cache monitors these write operations and uses the validity bits to indicate a change has occurred in main memory (i.e., the contents of a field in cache are not valid).

Shared Memory

A Shared Memory System is available for multiple processor configurations requiring rapid access to

common data. Up to six ports are available, permitting as many as six processors to be connected to over three million bytes of memory. The combined main and shared memory available to a single computer is three million bytes.

I/O CHANNELS

The Harris 500 has several types of input/output channels which interface the central system bus to the device controllers. The system supports up to 24 logical I/O channels.

Universal Block Channel (UBC)

The Universal Block Channel is a block-mode, direct memory access channel for high-performance peripheral controllers such as those for discs and magnetic tapes. The UBC has two operating modes—the scan mode and the scan-lock mode. In the scan mode, a UBC supports two concurrent input/output operations. In the scan-lock mode, the UBC operates as a single direct memory access channel. In addition to direct memory operations, the UBC also functions as a programmed I/O channel transferring data under CPU/program control between a CPU register and the channel. The UBC contains a 48-bit data buffer for each logical channel.

Integral Block Channel (IBC)

The IBC is a block-mode, direct memory access channel for interfacing the card reader to the system. The card reader controller plugs onto the IBC module.

Programmed I/O Channel (PIOC)

The PIOC is a channel for interfacing slow speed devices to the system. It supports up to four plug-in controllers for devices such as a line printer, operator communications terminal, and user terminals. Input/output to these devices proceeds under program control through a CPU register.

External Block Channel (XBC)

The XBC is a specialized direct memory access channel for user-designed and developed controllers and devices.

Direct Memory Access Communications Processor (DMACP)

The DMACP is a direct memory access communications processor for interfacing various terminals to the system. The DMACP supports both synchronous and asynchronous communications.

SOFTWARE

A comprehensive set of software is available for use with the Harris 500 computer system.

VULCAN Operating System

The Harris Virtual Memory Operating System is a priority structured, demand-paged, multi-programming operating system. VULCAN concurrently supports:

- Multi-stream batch processing
- Interactive time-sharing
- Data base management
- Remote job entry
- Real-time operations

In addition to its operating features, VULCAN works in conjunction with the paging hardware to monitor and direct memory allocation. VULCAN virtual memory operation is totally transparent to the user—while providing the advantage of efficient memory management, extensive user memory space, complete program protection, system security, and a wide selection of system services.

Support Software

The field-proven VULCAN operating system supports nine languages, five support programs, a programmable interactive command language, five remote job entry and two remote batch terminal packages, and TOTAL, a data base management system with T-ask,™ an information retrieval system.

Languages
- Extended BASIC Language Processor
- FORTRAN IV Compiler
- FORTRAN 77 Compiler
- Extended 1974 ANSI COBOL Compiler
- APL Interpreter
- RPG II Compiler
- Harris Macro Assembler

- SNOBOL 4 Interpreter
- FORGO (Load-and-Go FORTRAN Compiler)

Support Programs
- Sort/Merge Package
- VULCAN Indexed Sequential Package (VISP)
- System Accounting (ACUTIL)
- Cross Reference
- VULCAN Symbolic Debugger (VBUG)

Remote Job Entry (RJE) Support Packages
- CDC 200 UT
- IBM 2780
- IBM 3780
- IBM HASP II Multi-leaving
- UNIVAC 1004

Remote Batch Terminal (RBT) Host Packages
- IBM 2780
- IBM HASP II Multi-leaving

Interactive Terminal Package
- IBM 3270

Data Base Management System (DBMS)
- TOTAL Central
- T-ask™ Information Retrieval

Harris Transaction Processor (HTP)

TECHNICAL SPECIFICATIONS

HARRIS 500 CENTRAL PROCESSING UNIT

Type	Microprogrammed, general-purpose, digital computer. Multi-access central system bus.
Arithmetic	Parallel, binary, two's complement fixed and floating point; optional hardware floating point processor.
CPU Microcyle Time	300 nanoseconds

MEMORY SYSTEM

Main Memory

Type	N-Channel MOS with error correction.
Minimum size	196,608 Bytes
Maximum Size	3,145,728 Bytes (with optional Extended Memory)
Increment	192 K Bytes (K=1024)
Word Length	48 bits
Cycle Time	400 nanoseconds (48 bits)
Access Time	290 nanoseconds (48 bits)

(Performance of memory may differ from above when used in Expanded or Shared Memory configurations.)

Cache Memory

Type	Bipolar RAM
Size	6 K Bytes
Word Length	48 bits
Cycle Time	150 nanoseconds (48 bits)
Access Time	70 nanoseconds (48 bits)
Organization	3 KB for operands 3 KB for instructions

Shared Memory (Optional)

Type	Uses Main Memory modules in a Shared memory chasis.
Number of Ports	6
Number of Shared Memories interfaced per CPU (maximum)	4
Port Access	Asynchronous, ring priority

ADDRESSING Direct, indirect, or indexed to 3072 K Bytes

INPUT/OUTPUT

Programmed Transfers	Transfers 8- or 24-bits between a CPU register and the PIOC.
Direct Memory Access Transfers	Transfers 24- or 48-bits between main memory and either the IBC, UBC, DMACP or XBC channels.
Aggregate, Maximum Throughput	Input rate—Up to 19.0 MB per second Output rate—Up to 7.9 MB per second

Single Channel Maximum Transfers Rate (per second)

	Input	Output
IBC	80 KB	80 KB
XBC		
(no CPU contention)	2.4 MB	2.0 MB
(with CPU contention)	1.4 MB	1.2 MB
UBC (with 30 ft. peripheral cable)	3.2 MB	2.5 MB

PRIORITY INTERRUPT STRUCTURE

Internal	Eight executive traps. Multi-level, vectored structure.
External	16 levels, standard. Optionally expandable to 48.
Control	External Priority Interrupts may be individually armed, disarmed, enabled, inhibited or triggered under program control.

POWER FAIL PROTECTION Power fail alarm, standard.

ELECTRICAL REQUIREMENTS

(For CPU, memory and channels contained in a two cabinet configuration.)

Voltage	120/208, 115/230 VAC, 4-wire (standard), or 220/240 VAC, single-phase, 3-wire (optional).
Frequency	60 ± 3 Hz, (50 ± 3 Hz, optional)
Current	24 Amps., maximum.

ENVIRONMENTAL REQUIREMENTS

(For CPU, memory and channels)

Temperature	
Operating	50° F to 113° F (10° C to 45° C), ambient air
Storage	32° F to 122° F (0° C to 50° C), ambient air
Humidity	
Operating	20% to 80%, relative (non-condensing)
Storage	20% to 90%, relative (non-condensing)
Altitude	
Operating	−1,000 to 6,000 ft. (−305 to 1,829 m)
Storage	−1,000 to 15,000 ft. (−305 to 4,572 m)
Cooling	Forced air provided by internal fans on each chassis.

HARRIS
COMMUNICATION AND
INFORMATION PROCESSING

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