RWA-301 Description

The RWA-301 Guzik Technical Enterprises Read Write Analyzer is an integrated tool for the design, analysis and testing of magnetic storage devices and their components. It can be configured for testing disks and heads on a spinstand, drives, head/disk assemblies(HDA's) and head stacks.

With high precision, it performs all traditional measurements such as resolution, PW50, signal-to-noise ratio, overwrite, track average amplitude(TAA) and modulation. To measure the timing accuracy of a recording system, the RWA-301 performs Phase Margin(Bit Shift) Analysis by means of a programmable frequency data separator, accurate to better than 0.5 nanosecond, and a phase margin detector with calibrated window settings, accurate to better than 0.5 nanosecond. Through the use of a software controlled bit mask, the RWA-301 can examine bit shift on any one bit or group of bits in the read back data. This is useful for determining write precompensation and read channel equalization. The RWA-301 includes circuitry to generate RLL encoded data, multiple measurement gates for sectored servo disk drives, optional write pre-compensation and software controlled frequency zones for testing the advanced magnetic recording devices of today.

The RWA-301 is controlled by menu driven software from an IBM PC/AT or compatible computer. Many software application packages are available to extend the use of the product into all areas of magnetic recording.

Features

Track Average Amplitude

Resolution

Signal-to-Noise

Positive and Negative Modulation

Asymmetry

Overwrite

Missing Pulse and Extra Pulse

Pulse Width

Phase Margin(Bit Shift) Analysis

Phase Margin Measurement on Operator Selected Bit(s) in Read Back Data, early and late data

Programmable Write Current

Variable Frequency to 25 Mbit/second

Ability to use drives Servo Clock as the frequency source

Multiple Recording Zones

Result Logging to Disk and/or Printer

Standards(Multiple Correction Factors)

Grading System

Remote Communications and Control for Robotic Integration

Customer Specified Plug-In Filters

Large Variety of Spinstand and Drive Interfaces

Production and Engineering Software

Support for Variety of Preamplifiers

Built-in Calibrator for Bit Shift Analyzer

Any User Specified Transition Pattern up to a 2000 Transition(Bits) Cycle

Detector Thesholds Track Read Envelope

Programmable Peak Detector Time Constant

Software for Head, Disk, HDA and Head Stack Testing

Digital Output Signals for Oscilloscope Connection

Operator Specifiable Curve Fitting and Extrapolation

Programmable Positive and Negative Erase Currents

Extensive Graphics Displays

Multiple Programmable Measurement Gates Suitable for Sectored Servo Skipping

True RLL Recording to 25Mbit/Second by use of a software configurable encoding scheme
Example: MFM = 12.5Mhz,RLL 2/7 = 8.5Mhz,
RLL 1/7 = 12.5Mhz

Specification

Analog Channel

Band Width:	10Khz to 40 Mhz
System Noise:	Less than -55db
Non-Linearity:	Second harmonic less than 1%
Programmable Attenuator:	36db(6db/step)
Filter Matrix:	4 customer specified filters
Preamplifier:	Customer specified
Write Current:	Programmable, 0 to 64 ma(zero to peak)
Programmable Frequency Synthesizer:	.5 Mbit/second to 25 Mbit/second

Parametric Measurement Accuracy

TAA:	+/- 1.5%

Modulation:	+/- 2.0%
Resolution:	+/- 3.0%
Signal-to-Noise Ratio:	+/- 0.5db
Crest Factor:	+/- 2.0%
Overwrite:	+/- 0.3db
Asymmetry:	+/- 0.5%
Pulse Width:	+/- 2.0%

Surface Testing

Missing Pulse:	+/- 2%, 0% to 100% threshold(normalized to 2F envelope)
Extra Pulse:	+/- 2%, 0% to 50% threshold(normalized to 2F envelope)
Individual Recording Zones:	Multiple programmed zones

Digital Test

Data Separator: +/- 0.5 nanosecond, .5 Mbit/second
                                         to 25 Mbit/second

Bit Shift Analyzer with Internal
Calibrator: Consistent window error less than
                                         0.5 Nanosecond

                                         Jitter less than 100 Picoseconds
                                         RMS

                                         Repeatability < / = 100 Picoseconds

Pattern Generator: Any user specified transition pattern
                                         up to a maximum of 2000
                                         transitions in a cycle

                                         Real RLL, up to a maximum of 25
                                         Mbit/second

Precompensation: Optional precompensation in
                                         development