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TECHNICAL PROPOSAL

SYSTEM 473L
DATA PROCESSING EQUIPMENT

SUBMITTED TO

UNITED STATES AIR FORCE
HEADQUARTERS, ELECTRONIC SYSTEMS DIVISION
AIRFORCE SYSTEMS COMMAND
LAURENCE G. HANSCOM FIELD
BEDFORD, MASSACHUSETTS

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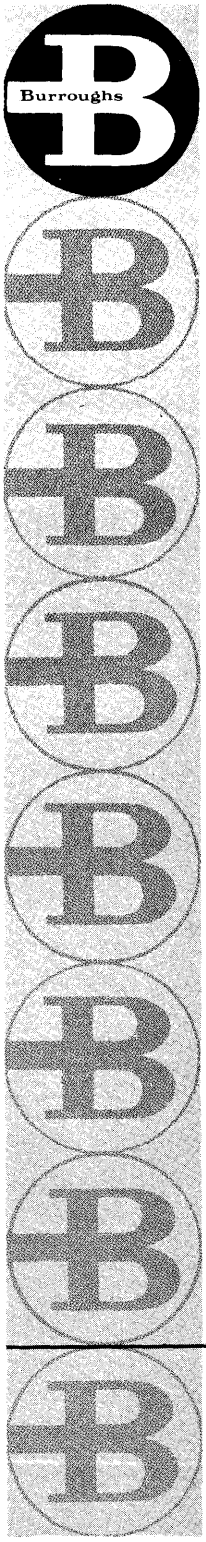

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INTRODUCTION

In response to Electronic Systems Division RFP No. ES-2-473L-2468, the Burroughs Corporation proposes to meet the requirements for the System 473L Data Processing Equipment by furnishing a configuration of the AN/GYK-3(V) Modular Data Processor. AN/GYK-3(V) is the U. S. Navy designation for the Burroughs D825 system. The latter designation will be used throughout this proposal.

The technical portion of this proposal indicates that a D825 fully satisfies and exceeds the detailed IOC requirements of System 473L with respect to:

- Speed -- easily processes the Compare Macro problem in the specified time (0.88 seconds versus 1.0 seconds)
- Real Time Interface -- interface modules which will:

  Simultaneously provide service by the Character Demand Buffer to 512 character-oriented devices (high-speed communication channels, console displays, large board display, or briefing-inquiry stations)

  Provide simultaneous service by Input-Output Modules to 10 block transfer devices (drum store, disc file, magnetic tape, etc.)

  If System 473L requires, provide service to over 300 remote briefing-inquiry stations
- Assurance of system operational continuity as equipments are added to meet the Complete Operational Capability (COC)
- Parallel Processing -- functionally independent modules under the control of an Automatic Operating and Scheduling Program assures dynamic scheduling of simultaneous computing functions

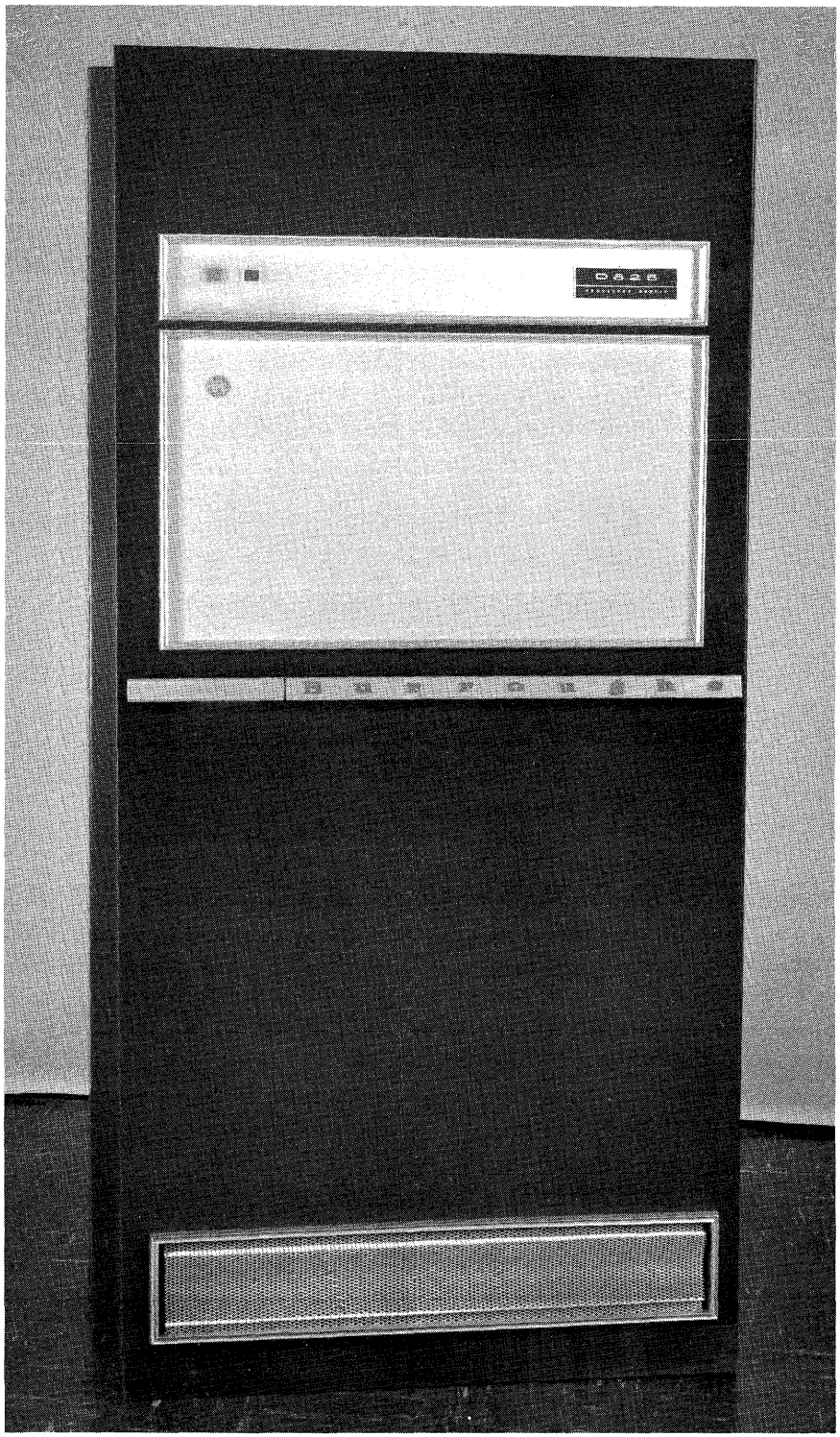


Figure 1. Typical Standard D825 Module

- Reliability -- in the D825 Modular Configuration a single failure does not compromise system performance. The operator or operator-directed program can direct the processor to:

  Continue system operation at a reduced rate

  Operate on a task priority basis

- Growth -- without reprogramming. The IOC installation will be configured for growth, without system shutdown, to a capacity well in excess of that anticipated in the RFQ for System 473L

The project office which will be responsible for the 473L Data Processing Subsystem is in existence and is presently assembling several D825 complexes. One of these will be delivered to the U. S. Navy (NRL); the others are being built for Burroughs inventory.

Product Improvement Program

Corporate funds are being applied to a product improvement program, the results of which are available for incorporation into D825 configurations. Some of the developments of this program are as follows:

The Character Demand Buffer is a unit of hardware which has been added to the D825 equipment complement during the past year. Its design was fostered by the display-communication interface problems associated with the 425L program.

Other results of the product improvement program available to System 473L if future system requirements warrant are:

- Instruction to perform mask compare
- A speed-up in the Data Processing module by a factor of 2
- A 4096-word, 48-bit data memory module with a read-restore cycle of 0.5 μsec
- Capability to add eight additional independent memory access channels (five are presently employed)

These improvements can be incorporated into existing D825 systems as they are made available. They will require little change in the scheduling program, since these considerations have been designed into the Automatic Operating and Scheduling Program (AOSP); just as the AOSP is configured to accommodate any of the possible configuration mixtures of the D825, so it is able to accommodate fundamentally independent modules of mixed rates of processing.

SECTION I
OPERATIONAL PERFORMANCE CHARACTERISTICS

ORGANIZATION

The Burroughs D825 Modular Processor is characterized by its fully shared core memory and concurrent operation of all functional modules. Computer modules and interface modules can simultaneously gain access to separate high-speed core memory modules. In the event of a memory addressing conflict, the conflict is automatically resolved, the lower priority item is delayed the several microseconds it takes to complete the memory transfer of higher priority.

The D825 system is arranged around interconnection networks which permit the various functional modules of the system to simultaneously intercommunicate without restriction. The interconnection networks are distributed among the units they service and physically do not exist except as a part of a functional module.

The operational management of the D825 system is under the control of the Automatic Operating and Scheduling Program (AOSP), a program which analyzes the current system demands and assigns units of the system in such a way as to optimize system performance.

By virtue of this complete freedom of intermodular communication and because of the administration role played by the AOSP, the D825 has inherent multi-thread design. System 473L is assured the efficient maintenance of the data base and the simultaneous retrieval and processing of all necessary data.

RELIABILITY

The assignment doctrine of the AOSP which considers the number of modules of each type available to perform their function also permits automatic

system adjustment for failure of modules. Standby redundant equipments are not required, and failure of one module cannot cause system failure as long as another module of the same type is operating. The only effect of a failure is a reduction of the on-line equipments; system operation continues at a reduced rate or on a task priority basis while repairs are effected.

The D825 has been designed to conform to military specifications. Equipment with a high unit reliability, incorporated in a modular system tolerant of failures of individual modules, and organized for rapid recovery from module failure, assures accomplishments of reliability goals.

GROWTH

The completely modular design of the D825 admits of great flexibility in conforming to expanding and changing operational requirements. As the task mix of System 473L changes to meet new demands, appropriate system modules may be added to the existing system to raise its capability to the requisite level. The IOC configuration will possess the capability necessary to achieve the ultimate growth possible in the system; the installation of additional units reduces to the connection of cables -- no interruption of system activity during growth will be required.

The modular system organization permits two types of growth: addition of identical modules and introduction of totally new or improved equipments. Advantage can thus be taken of the Burroughs D825 product improvement program. As new modules with increased capability are made available as off-the-shelf items, they may be efficiently utilized in existing D825 configurations. The AOSP has been written to accommodate both of these features.

AUTOMATIC OPERATION

Automatic scheduling of problems and dynamic assignment to individual modules is carried out by the Automatic Operating and Scheduling Program (AOSP). The AOSP controls automatic allocation of memory space, automatic assignment of programs based on priority, and automatic transfer of control in separate cross-referenced programs.

An automatic interrupt is an integral part of the D825 system. It provides an additional mode of control and facilitates recognition and diagnosis of

system element failures. All interrupts are recorded, and the AOSP directs the processing of these interrupts. Typical interrupt conditions are:

- External demand for connection
- Run-down of Real Time clocks
- Arrival of a message
- Failure of a functional unit or primary power failure

When primary power fails, the regulated power supplies will maintain service for 500 μs. During this time the computer automatically stores sufficient information in non-volatile memory to restart the program without loss of data.

MANUAL OPERATION

Since responsibility for the management of the data processing system is delegated to the AOSP, the role of the operator is principally that of a monitor. Routinely, then, the system operates with a minimum amount of human intervention. At all times, however, the system is under the overriding control of the operator. Any failures of the system are signaled to the operator either automatically by the equipment or by the AOSP. The operator then takes the appropriate action, be it repairing equipments or instructing the AOSP via console keyboard as to the proper steps to be taken, such as the task priority assignment.

SECURE OPERATION

That computer operation is under control of the AOSP provides a high degree of security; information can be labelled with security classifications and distributed by the AOSP only to authorized output stations. This table of classifications may itself be made accessible only through special procedures so that the integrity of the system against tampering is preserved. In this way, availability of information may be restricted to any degree desirable by declaring certain areas of the digital store to be forbidden to improper requests -- no operator intervention is necessary after such information is initially introduced into the system; and, since no encipherment is required, there is no burden imposed upon the system aside from the adequate labelling of the information by the AOSP.

SECTION II
TECHNICAL CHARACTERISTICS

FUNCTIONAL CONFIGURATION

ORGANIZATION

The Burroughs D825 data processing system is housed in a number of standard cabinets, with at least one functional module to a cabinet. The central processing elements -- the computer module, the core memory module, and the interface modules (the Input-Output Module and the Character Demand Buffer) -- are interconnected by a switching interlock. The central processor services storage and record devices through an interconnection matrix which is controlled by from 1 to 10 Input-Output Modules (IOM). Character demand devices such as displays, communication channels, and inquiry stations are connected to the central processor through an interconnection matrix which is serviced by the Character Demand Buffer (CDB).

In Figure 2 is depicted the functional configuration of the D825 Modular Processing System for application to the 473L Command and Control System. Shown in red are those equipments necessary for the Initial Operating Capability, in green the Complete Operational Capability, and in blue a possible Ultimate Growth Configuration.

The number of modules required for IOC, COC, and the number available for growth of system capability is as follows:

Module	IOC	COC	Growth
Computer	1	2	3
Core Memory	4	7	16
Input Output Module	2	3	10
Character Demand Buffer	1	2	4
Real Time Store	1	2	
Auxiliary Store	2	4	
Bulk Store	1	2	
Card Reader	1	2	
Card Punch	1	2	
Line Printer	2	4	
Operating Console	1	2	
Magnetic Tape	2	4	

The number of storage and record devices (Real Time Store, Auxiliary Store, Bulk Store, Card Reader, Card Punch, etc.) which may be included in the growth system is limited only by the number of channels available at the Input/Output Exchange. There are 64 channels available to service storage and record devices, 36 are used to implement the COC configuration.

The number of character demand devices (Consoles, Displays, Communication Channels) which may be accommodated for growth is limited by the number of channels available at the Communications and Display Exchange. There are a total of 256 channels available to service character demand devices; 86 are used to implement the COC configuration. If required, this number could be increased by an additional 256 channels by implementing the growth Character Demand Buffers as indicated in Figure 2.

Interconnection Networks

Central to the modular operation of the D825 is the Switching Interlock, the matrix at the center of the Functional Organization illustration (Figure 2). Running horizontally are the five major buses of the system: three Computer Buses, one Input/Output Bus, and the Communication Display Bus. Intersecting these buses are the Memory Buses, shown as vertical lines.

The functional modules terminating the five buses are capable of exchanging information with any Memory Module. Provided that each bus is exchanging information with a different Memory Module, all buses can simultaneously exchange information with memory at a rate of one 48-bit word per bus per four microseconds. A priority resolving network located at each memory module resolves any conflict in requests for access to the memory.

An identical situation obtains in both the Input-Output Exchange (shown at the right of the illustration) and the Communication and Display Exchange (shown on the left). In each of these exchanges any of the peripheral devices may communicate with any of the interface modules -- Input-Output Control Modules for the I/O Exchange, Character Demand Buffers for the Communication and Display Exchange. Should one of the interface modules fail, the load is automatically assumed by the remaining modules. When in operation, the Interface Buses are effectively time-shared by the various modules connected to them.

Data Flow

Also depicted in the Functional Organization illustration is a typical instant in time of computer operation. The variously colored lines through the interconnection networks indicate simultaneous transfers of information between functional units; the alternately shaded, broken lines on the two interface buses represent the time sharing which allows simultaneous communication on these lines. As represented in the diagram, the following transfers of information are taking place:

- The IOC Computer Module is communicating with the second growth Memory Module
- The COC Computer Module is communicating with the second COC Memory Module
- The Growth Computer Module is communicating with the first IOC Memory Module

- The Input/Output Bus is being time-shared among:
    - ▲ The IOC Auxiliary Storage Unit, which is loading the fourth IOC Memory Module through the first I/O Control Module;
    - ▲ the COC Bulk Storage Unit, which is being loaded from the third IOC Memory Module through the second I/O Control module; and
    - ▲ The IOC Card Reader, which is loading the first growth Memory Module through the third I/O Control Module.
- The Communication and Display bus is being time-shared among:
    - ▲ an Integrated Console, which is accepting data from the first COC Memory Module via the IOC Character Demand Buffer;
    - ▲ a communications channel, which is loading the third COC Memory Module, also being serviced by the IOC Character Demand Buffer;
    - ▲ A Large Board Display, which is accepting data from the second IOC Memory Module via the COC Character Demand Buffer; and
    - ▲ a growth device, which is loading the fourth growth Memory Module through the first growth Character Demand Buffer.

The interconnection networks do not exist as entities in themselves, but are distributed among the modules they service; that portion of the interconnection network which services a given functional unit is packaged with and is considered a part of that functional unit. If a failure occurs in any of the interconnection networks, only the functional unit which is being serviced by that portion of the interconnection net is lost to the system.

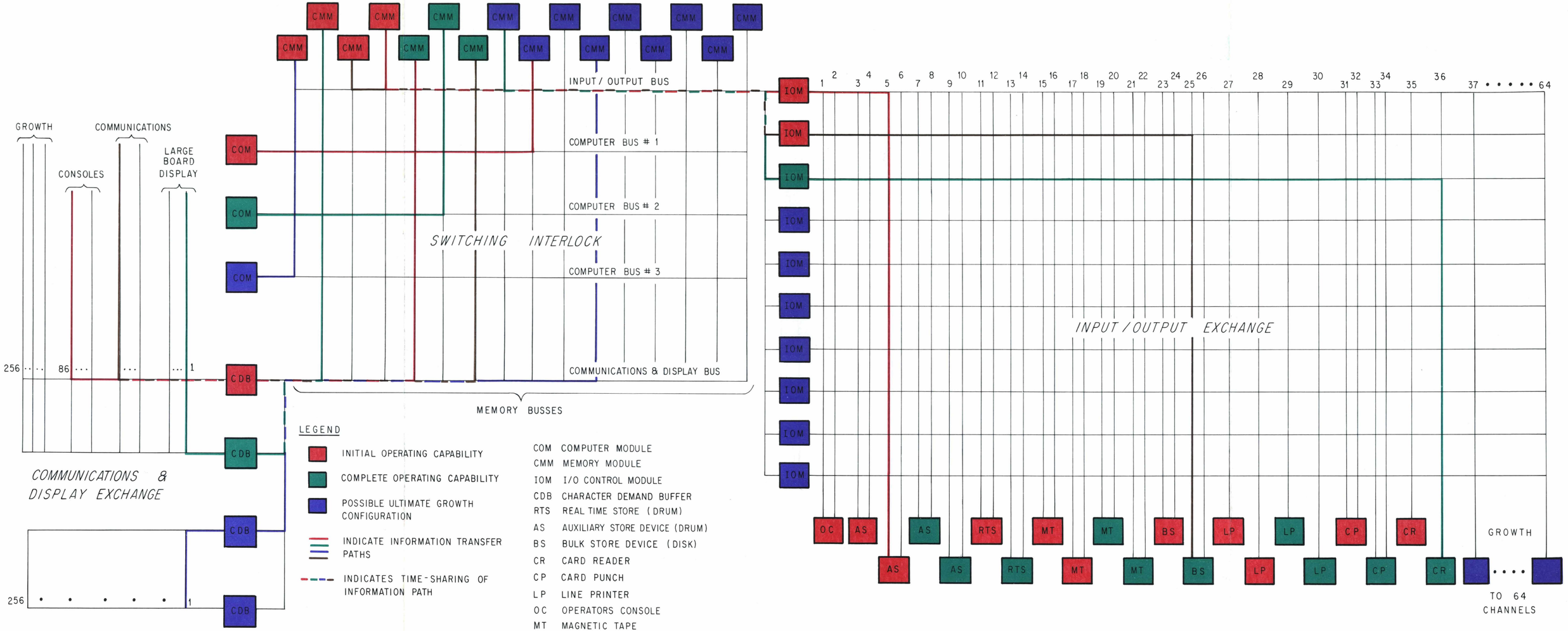


Figure 2. D825 Functional Organization

OPERATING AND SCHEDULING PROGRAM

The functionally independent modules of the Burroughs D825 modular configuration are controlled by a supervisory program which distributes the work load, checks equipment status, and in general supervises system operation. The program is not to be considered supplementary to the hardware system -- it is an integral part of the D825 system, and, indeed, only because of its existence can the system be considered truly modular.

Such a program exists in the Automatic Operating and Scheduling Program (AOSP). The AOSP is a completely general program which operates with any configuration of the D825. The execution of the AOSP, moreover, is not assigned to any specific computer module creating a master-slave arrangement; instead each computer module uses the AOSP as required.

The most important single function of the AOSP is that of the scheduling of work loads. Through this function efficient utilization of equipment is assured with the hardware being used a maximum amount of the time; in case of equipment failure, continuity of processing is ensured. In particular, as new units are added to the system the AOSP , upon recognition of their presence, automatically uses them to best advantage -- no modification of the program is required.

Some of the more important features implemented by the AOSP are:

- The keeping of records of current system configuration
- The ability to receive, decode, and act upon requests from the external world to modify system configuration
- Maintenance of records showing to what items space has been allocated and what memory locations they have been assigned
- Maintenance of records of memory space available for allocation for servicing new run requests
- Regular confidence testing of hardware modules to aid in the timely determination of modules which must be passed over when selection is made for equipment to service new jobs
- Response to external request interrupts
- Administration of the input and output of messages and data between the system and the devices it services

- System of priorities observed in selecting the order in which tasks are serviced
- Master files of system facilities, such as a library of production programs, service programs, standard sub-routine procedures, and permanent data objects
- Administration of the real time clocks in the system

Much of the AOSP operation necessarily occurs "behind the back" of the user's program. The establishment of the correct linkages between programs, subprograms, and data occurs automatically; the scheduling of I/O and the maintenance of system bookkeeping are done without explicit mention in the running programs; and response to interrupt conditions is independent of any foreknowledge on the part of the interrupted program. However, many of the AOSP functions are available to the programmer at his request, via "Control Macros," which are essentially sub-routine-like calls on parts of the AOSP package. Some typical representatives of these functions are: make ready, and then execute, an arbitrary program found on the file; hold up the operation of this program until some specified condition obtains, such as completion of an I/O operation, or termination of some other program.

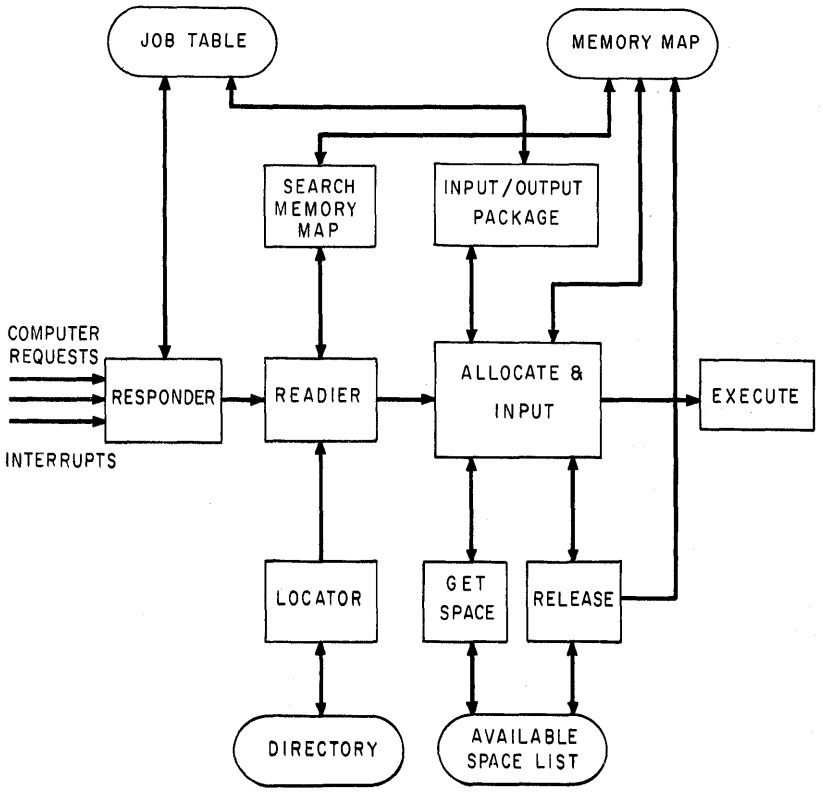


Figure 3. AOSP Flow Diagram

REAL TIME INTERFACE

The bus structure of the D825 is ideally suited to handling of the comparatively severe input-output requirements imposed by the 473L system requirements. To service the multiplicity of devices, the two interface interconnection buses previously described are used -- one for character demand devices and the other for those devices characterized by block transfer of large masses of data.

Two types of interface modules are available for handling real time input-output traffic: the Input-Output Module (IOM), designed for one-at-a-time handling of up to 64 storage and record devices, and the Character Demand Buffer (CDB), designed for simultaneous (interleaved) handling of up to 256 character demand devices. In addition, certain types of devices require Data Synchronizers. The Data Synchronizers are a class of devices which perform the function of matching the input-output device data rate with the CDB or IOM data rate, making the signal levels of the devices compatible with those of the D825 and generating control signals as necessary.

INPUT-OUTPUT MODULE (IOM)

The IOM services the following devices in the 473L system:

2 Magnetic Tapes	1 Card Punch
1 Disc File	1 Card Reader
2 Drum Storage Units	1 Computer Console
2 Line Printers	

The number of these devices required for IOC and COC respectively, as indicated in the specifications for System 473L, is shown in the illustration of the system's functional configuration (Figure 2). Of the 64-channel capacity at the IOM, the number required to perform the COC function is 17 input channels and 19 output channels.

The number of IOM's required to service these storage and record devices is primarily a function of speed and the need for simultaneous service. The data rates of the storage devices specified in the RFQ indicate that two of the IOM modules are required to handle the peak load for the IOC. There is enough growth potential inherent in these two modules in terms of data rate, however, that only one more IOM is necessary to service the COC installation.

Data Flow Analysis

An IOM communicates with the devices in terms of 6-bit characters (plus parity) at up to a 500-kc character rate, while it communicates with the system memory in terms of 12-bit syllables, with groups of 5 syllables (4 data, 1 parity) being transmitted at a 250-kc rate. The communication between an IOM and a device actually proceeds at a rate determined by the device, and the IOM remains connected to the device for the duration of an operation.

The character rates of the devices to be serviced by the IOM for 473L are given below. Also given is the corresponding core memory access rate. In the IOM, data is packed 8 characters per memory word; therefore, an IOM generally requests memory access at one-eighth the character rate of the device it is interconnected with.

I-O Device	Character Rate Per Second*	Memory Access Rate Per Second
Drum Storage Unit	496.0 kc	62.0 kc
Card Punch (binary mode)	136.0 kc	17.0 kc
Card Punch (alpha mode)	68.0 kc	8.5 kc
Magnetic Tape Unit	66.7 kc	8.3 kc
Magnetic Disc Unit	62.5 kc	7.8 kc
Card Reader (binary mode)	6.7 kc	833.0
Card Reader (alpha mode)	3.3 kc	416.0
Line Printer	667.0	83.0
Keyboard - Printer	10.0	1.2

*Actual rate of handling characters within IOM, not an average character rate.

The IOM-memory interconnection time required in reading data from memory is 3.67 microseconds, and 2.67 microseconds in writing data into memory. These figures represent times for reading and writing single isolated words; consecutive references to memory consume a full memory cycle time of 4.0 microseconds per word or 250,000 memory accesses per second.

During system operation, the bulk storage disc unit will be interconnected with an IOM almost continuously, in view of the fact that there will possibly be a continuous queue of 40 requests for records. It necessarily follows that one IOM must be allocated for this service. A second IOM provides sufficient capability for the interleaved handling of all the remaining devices. The two IOM's permit the simultaneous execution of two input-output operations. This capability is adequate, considering the relatively short duration of most of the input-output operations.

Two system limits of interest concerning an input-output exchange are: (a) a single input-output bus can have up to 10 IOM's interconnected with it, and (b) the maximum combined memory access word rate for all IOM's on a single bus is 250 kc. When future requirements call for more simultaneous (not interleaved) input-output operations, up to 8 additional IOM's may be added to the system to permit a total of 10 fully simultaneous operations. The maximum total memory access rate for all of the devices of the system is well within the 250-kc capability.

Operation

The major registers of the IOM (Figure 4) are the command descriptor register, and the information assembly/distributor register.

The execution of a "Transmit to I/O" instruction by a computer module causes the transmission of a 48-bit command descriptor describing the input-output operation to be performed to the lowest-numbered non-busy IOM. The command descriptor register contains the current terminal device number, operation code, record count, word count, and memory starting address.

The assembly/distributor register is utilized by the IOM for:

(a) accepting data from peripheral devices, assembling it into memory words, and transmitting the words to memory, and

(b) reading words from memory, distributing them into 6-bit characters, and transmitting the characters to the peripheral devices.

Each IOM also contains a 2-character buffer to permit high-speed data transfer. On input operations, the 2-character buffer provides temporary storage for the first and second characters of a new input data word while the IOM is storing the previous word in memory; during output operations, the 2-character buffer provides temporary storage for the seventh and eighth characters of the word being transmitted to the peripheral device while the IOM is reading the next word from memory.

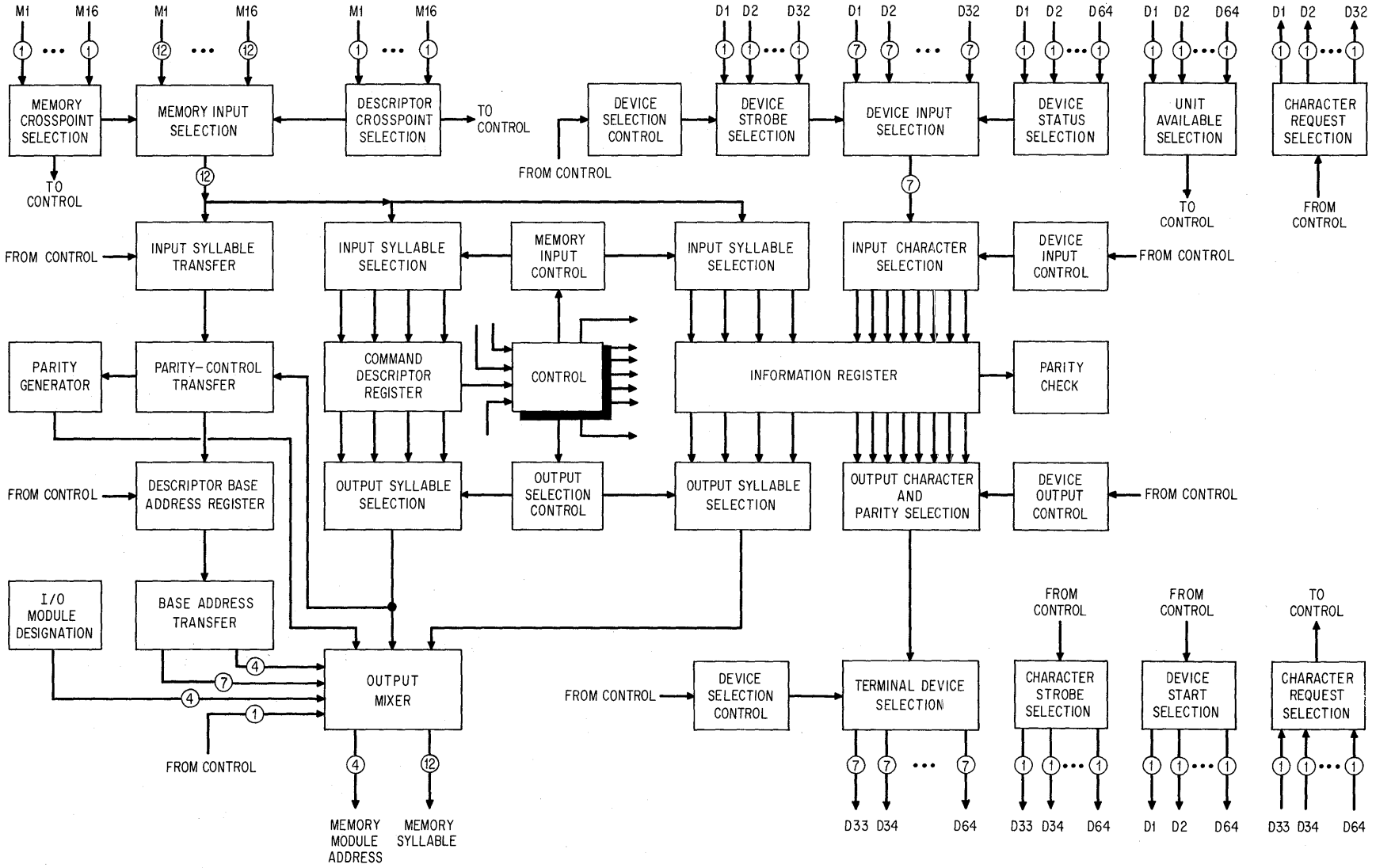


Figure 4. Input-Output Module Block Diagram

Each time a memory location is transferred, the transfer count is stepped down and the memory location count is stepped up. When an I/O operation is terminated, a result descriptor is generated which contains the I/O device designation, the last memory location transferred plus one, the number of locations left to be transferred, the operation being performed, and the reason for the termination. This result descriptor is made available to the system for further action by causing an I/O completion interrupt; appropriate action is then taken by the AOSP.

CHARACTER DEMAND BUFFER (CDB)

The CDB services the following devices in the 473L system:

Consoles	Communications
Displays	Inquiry Stations

The number of these devices required for the COC installation indicated in the specification for the System 473L is shown in the functional configuration illustration (Figure 2). The COC uses 86 of the available 256 channels and the combined character rate is 4650 characters/second.

Time utilization of the Character Demand Buffer is illustrated in Figure 5. On the basis of a 1-second period, the time required to simultaneously service the specified devices at peak rate for the IOC and COC is shown. The CDB handles easily all devices, with 87 percent of its data rate capability available for future use. This corresponds to a growth ability to simultaneously service 256 devices at a data rate of 130 characters per channel. The second CDB indicated in the functional configuration is required to meet the reliability specification for the COC installation.

Advantage of the available growth capacity could be taken through the installation of remote inquiry on display stations. It is recognized that space is limited in the operational area; however, it may be beneficial to locate inquiry or briefing stations in areas other than the immediate vicinity. For the COC installation, it would be possible to install 85 such stations. It is possible to install an additional two CDB's in the system, resulting in an additional 256 free channels utilizable for inquiry-briefing stations.

Transmission Characteristics

Data transmission between the CDB and the devices it serves is effected in serial format to minimize the extent and complexity of system interconnection cabling. Each input or output data channel requires that a shift register buffer of the requisite character length for that particular

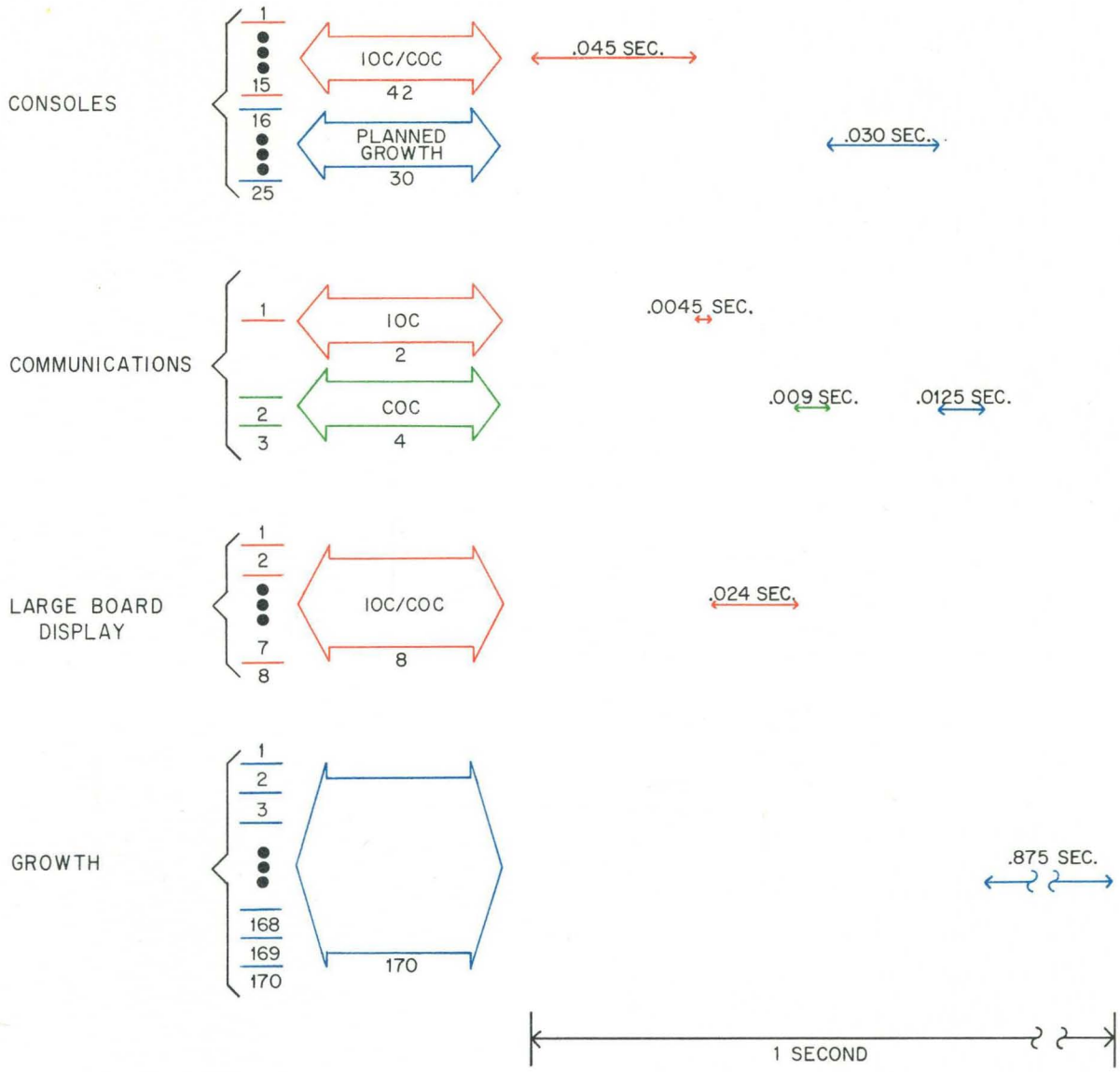
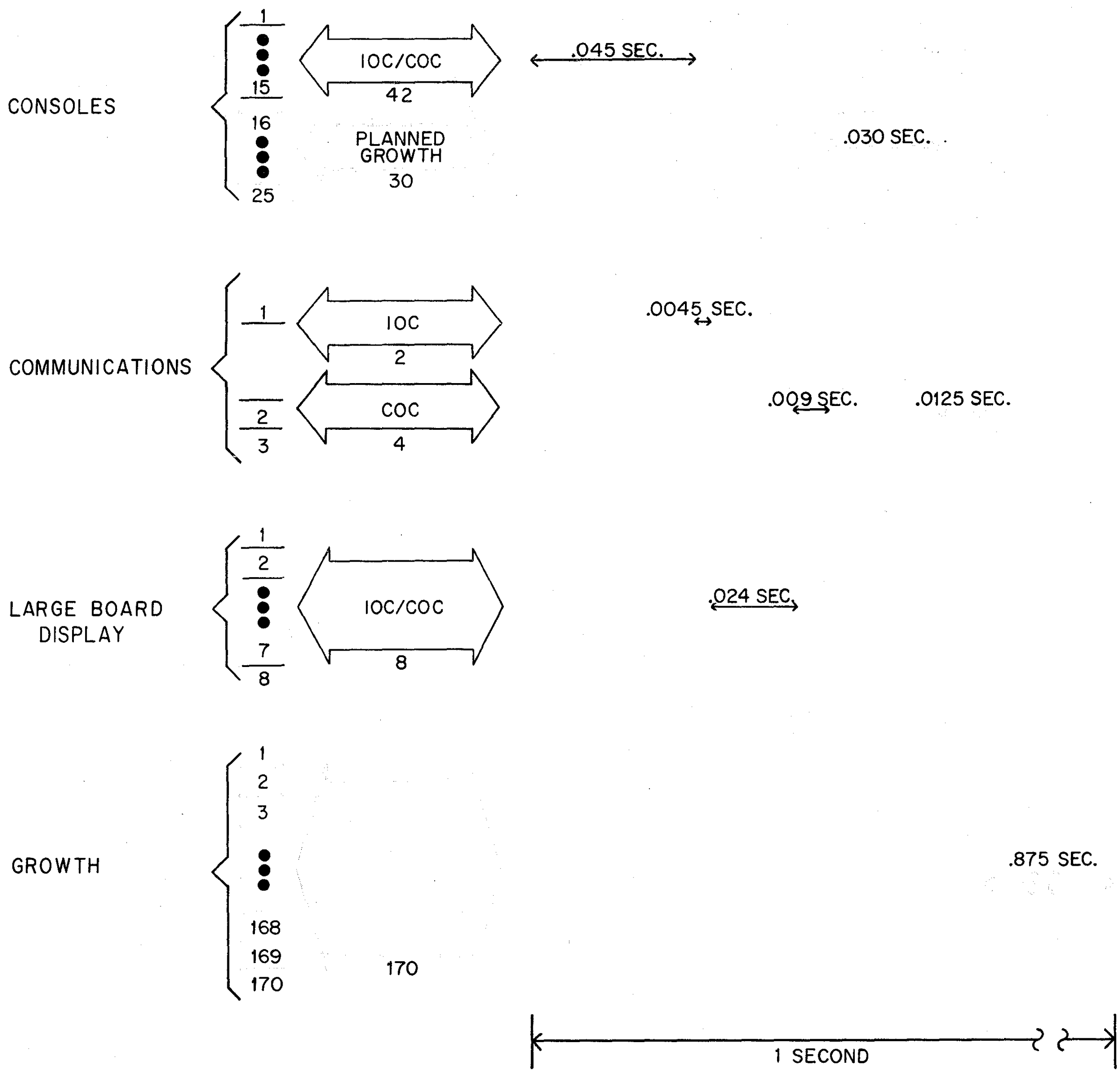


Figure 5. Time Utilization of CDB

channel be associated with the respective device. Data transfers to or from the device buffer are on a character-at-a-time basis on demand by the device. In addition to the serial data and shift lines, each data channel has an associated character request line that enables the device to control the channel character rate.

Input channels present a data line and a "character ready" line to the CDB; the CDB transmits shift pulses over one line to the input channel buffer register to effect data read-in.

Output channels present a "character request" line to the CDB; the CDB transmits data signals and shift pulses to the ouput channel over a pair of lines to effect data read-out.



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Although the character rate is established by the device, the bit rate of the CDB-terminal equipment buffer data transfer is established by the shift clock timing of the CDB. The service time per device, which includes the transmission of the character and the processing of this character, consumes 30 microseconds. It is thus possible for the CDB to service all 256 channels in a total time of 7.68 milliseconds, which corresponds to simultaneous service for 256 devices at a data rate per channel of 130 characters per second.

Operation

The CDB (Figure 6) contains a 512-word memory, devoting two storage words to each input-output channel. The address of each pair of words corresponds to the input-output channel number. One of the two locations provides storage for the applicable command descriptor, while the second location provides buffer storage for the information word being transmitted (distributed) or received (assembled). The command descriptor is identical in format and effect to that used by the IOM. Each CDB accepts only descriptors for channels which it is servicing.

Under program control, the complete list of command descriptors is loaded initially into the CDB; thereafter, command descriptors are reloaded, or modified and reloaded, or new descriptors loaded individually as the program requires them. Generally, the program will be arranged so that new descriptors are loaded while the system is processing an end-of-message interrupt.

A typical input operation for servicing a communication channel of 8-bit characters is executed as follows:

- While scanning, a character ready signal is sensed on an input channel. Scanning stops.
- The command descriptor and partial data word assembled so far are extracted from CDB memory. Scanning is resumed.
- An appropriate number of shift pulses is transmitted to the input channel and the incoming character is accepted serially into the CDB assembly register.
- The character received is appropriately inserted into the data assembled previously (if any).
- The command descriptor and re-assembled data word are re-stored in memory.

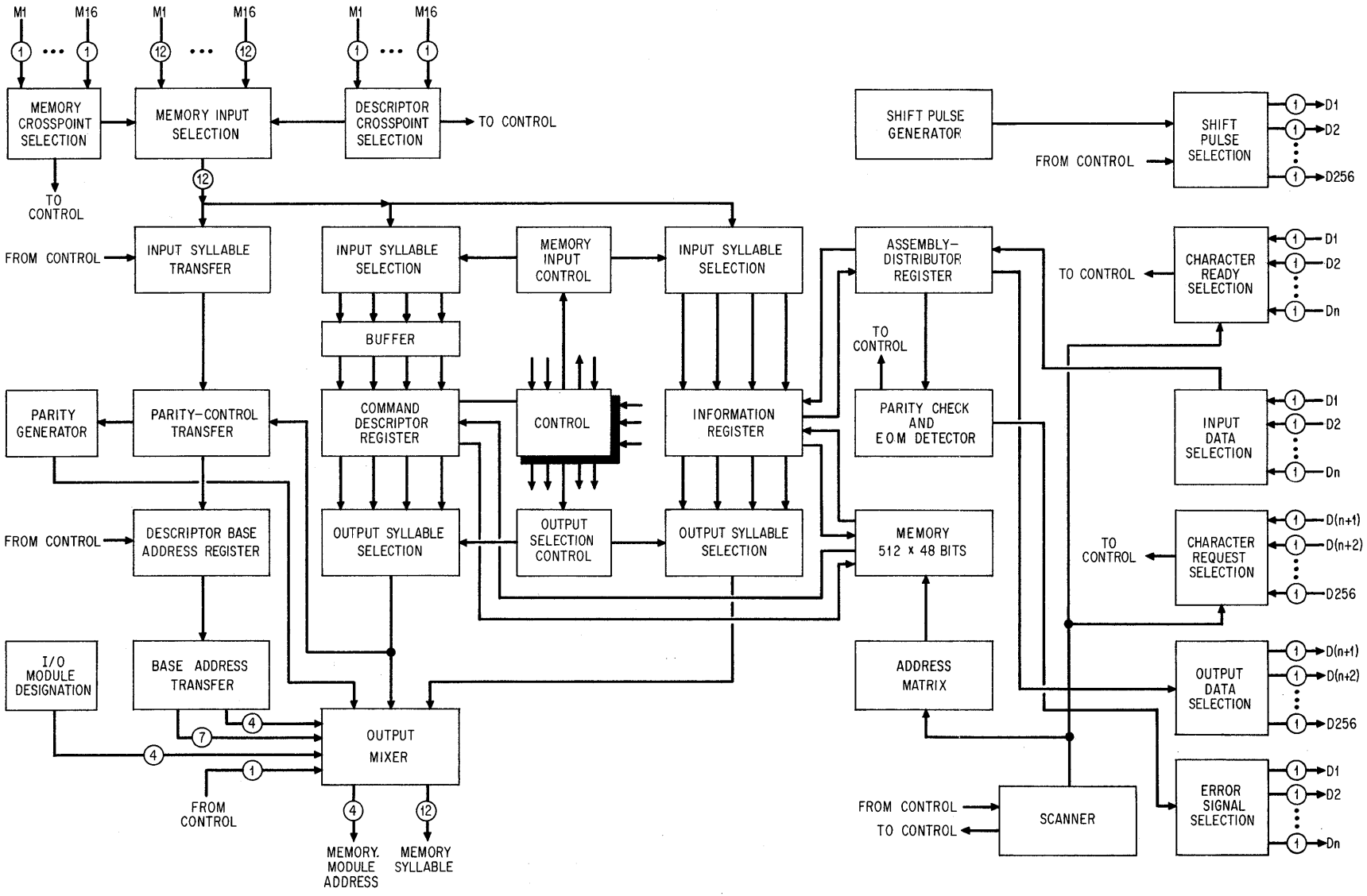


Figure 6. Character Demand Buffer Module Block Diagram

- If the scanner has not already stopped at the next service request channel, the CDB idles until a request is acknowledged.

Whenever a sufficient number of characters are received and assembled to form a full 48-bit word, the CDB stores the word in the system memory without interrupting the computer. The computer is interrupted only at the start of a message, the end of a message, or when more storage space is required in core memory. If the device being serviced has a character length of 48 bits, the word is automatically transmitted to system memory before that device needs servicing again.

The receipt of an end-of-message character initiates storage of the final data word, storage of the result descriptor (a modified version of the command descriptor) which informs the system of what operation has just been completed, and an interrupt of the computer system, indicating that an operation has just been completed and that a result descriptor has just been stored.

A typical output operation for servicing a communication channel of 8-bit characters is executed as follows:

- While scanning, a character request signal is sensed on an output channel. Scanning stops.
- The command descriptor and partial data word distributed so far are extracted from CDB memory. Scanning is resumed.
- The character to be transmitted is separated from the partial data word.
- The separated character is transmitted serially, with accompanying shift pulses, to the buffer register of the output channel.
- The command descriptor and the remainder of the partial data word are re-stored in memory.
- If the scanner has not already stopped at the next service request channel, the CDB idles until a request is received.

MANUAL SWITCHING

Although all of the communication and display data is able to be handled by one CDB unit, the use of two units for the COC installation is proposed in the interest of reliability. Data, however, will not be handled redundantly; instead, a manual switching capability is provided

whereby each data channel may individually be switched to either CDB, and in the event of a CDB failure, a master switchover of all channels to the operational CDB is provided, either under program control or manually.

Capability

Each CDB contains its own control panel of appropriate switches and indicators. A portion of the CDB control panel is devoted to an array of 256 switches for switching the flag signals (character ready and character request) of each of the 256 channels. Each of these switches determines whether or not the corresponding flag signal will be admitted into that CDB. Only the flag signal need be switched, since the corresponding data and shift pulse lines are active only when the flag signal is active.

If a CDB is to be taken off line for service or repair, the master switch may be employed. Each CDB contains such a switch, a 3-pole switch indicating "Service All Channels," "Service No Channels," and "Service Those Channels Whose Individual Flag Switches are Set."

Indication

Visual indication of the switching is provided on the CDB control panels. Internal indication to the data processing system is not required. The data processing system never requires to know which pair of CDB's is servicing any particular input-output channel. Regardless of how the 256 control switches are set on each of the paired CDB's, each of the CDB's will have accepted each of the command descriptors applicable to the 256 input-output channels of interest. A common command descriptor will be executed identically by either of the paired CDB's. However, periodic programmed confidence tests will be executed by the system to insure that each active input-output channel is being properly serviced.

PARITY CHECK

Character Oriented Device to CDB

Data received by the CDB from character oriented devices is parity-checked on a character basis, if the incoming data character contains a parity bit within its format. The CDB, on detecting an error, executes the following: (a) transmits an error-indicating signal directly to the device which presented the faulty data to the CDB, and (b) sets the appropriate bit in the status field of the applicable Descriptor. Thus

when the Descriptor is stored in the Processor's memory on completion of the input operation, the Processor is notified that an error exists in the particular message.

Cumulative checks, such as the longitudinal bit check required for comlognet messages, are performed by the Processor after the complete message has been stored in the Processor's memory. The Processor, on detecting such an error, will transmit a special Descriptor to the CDB, to cause the CDB to transmit an error-indicating signal directly to the device as in the parity error case.

Interface Modules to Core Memory

All data received via the CDB or the IOM for storage in Core Memory is assembled into 48-bit words, to which is added a 49th bit, indicating odd parity. This format represents the standard 49-bit format of the D825 core storage system. If an error is detected in transmission, an interrupt is initiated for diagnostic action.

Core Memory to Interface Modules

All data read-out from core storage is parity checked by the module receiving the data. The module (IOM or CDB), on detecting a parity error of this type, initiates an interrupt to the processor system for immediate diagnostic action.

Interface Modules to Devices

The CDB and IOM generates and formats parity bits with all data as required by the specific devices to which it transmits these data.

INTERRUPT

Beside the interrupts initiated because of errors in parity, each message received or transmitted via the CDB normally has associated with it two interrupts; (a) at message start, one interrupt directs the processor to cause the appropriate input-output descriptor to be transferred to the CDB for execution; (b) a second interrupt, at message termination, causes the CDB to store a notated version of the input-output descriptor into the appropriate field in core memory, in order that the processor may be informed of the complete status of the message. Another interrupt which may be initiated by the CDB occurs when an input-output descriptor word count field has been reduced to zero before receipt of any end-of-message indication. This notifies the processor that more

storage area must be allocated for the incoming message. The processor follows this up by generating a new descriptor and causing it to be transmitted to the CDB before the arrival of the next incoming character.

DIGITAL DATA COMMUNICATIONS LINKS

Digital communications links are serviced by the Character Demand Buffers. In the IOC configuration, provision is made for a single full duplex communications link (two channels, one input and one output); in the COC configuration, three full duplex channels may be used. Growth capability is limited only by the maximum number of channels available at the CDB and data rate. A CDB for example can simultaneously service 128 full duplex 600-bit-per-second channels or 55 1200-bit-per-second channels.

At each communication link, input or output, is a Data Synchronizer capable of buffering two 8-bit Fieldata characters -- for the output case, the one currently being transmitted and the next one to be transmitted; for the input case, the one currently being received, and the one previously received. The output Data Synchronizer also generates idle line code when transmission is not taking place. The input Data Synchronizer is capable of recognizing idle line code, and upon detecting the absence of the code, signals the CDB which in turn interrupts the computer. The Data Synchronizer also provides the necessary signal exchange characteristics to comply with EIA Standard RS232 and hence establishes electrical compatibility for data communication with the remote crypto and actual signal modulation equipment involved in the comlognet trunk connection.

The sequence of illustrations in Figure 7 shows the method of processing a typical communications input. In Part 1, a character has been accepted by the Data Synchronizer which transmits a Character Ready signal to the Character Demand Buffer. The CDB recognizes the flag and accepts and checks parity of the character in Part 2. In Part 3, the CDB interrupts a Computer which transmits to the CDB a Descriptor appropriate to the channel, which then loads the specified area in system core memory in Part 4. Part 5 shows the computer processing the message and transmitting an acknowledge signal to the CDB. In the last part, the processed message is sent to a disc file while the CDB sends the acknowledge signal to the output communications channel.

CONSOLE-DISPLAY INTERFACE

The integrated console subsystem is the major processor interface in the 473L system in terms of data rate. The Character Demand Buffer provides the means for this data interchange and enables simultaneous operation of the consoles with each other and with other real-time system elements.

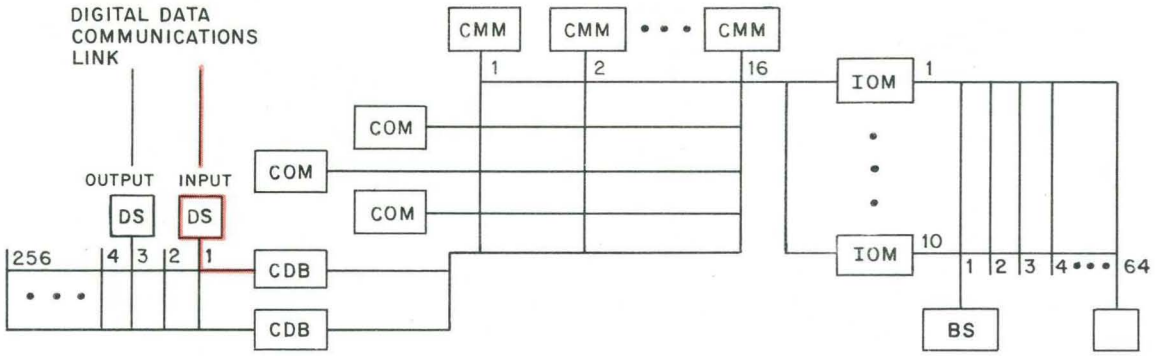
The specific data channels required are determined by the individual devices and related encoder-decoders within each console. There are three physically distinct data channels associated with the type A and C consoles, two channels for the Type B consoles which do not have console printers, and a single output channel for the large board display.

The data transmission requirements for each of the channels are as follows:

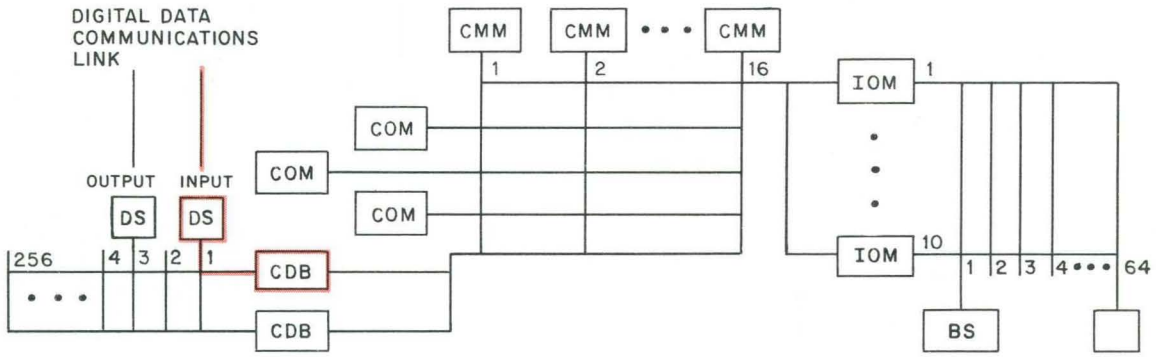
Channel	Character Size, Bits	Characters Per Second
CDB to MC/ET	32 (MC) 8 (ET)	100
CDB to Printer	8	10
ET Input to CDB	8	10
CDB to Large Board Display	32	100

The indicated character sizes include parity and control bits. Collectively, the 15 consoles and 8 large board displays which comprise the initial complement require 15 input channels and 35 output channels. The constraints on the number of consoles which the proposed D825 system could accommodate are that the number of input and output channels per CDB does not exceed 256 or that the maximum single channel character rate -- number of channels product shall not exceed 33, 000 per second. A single CDB can simultaneously service 85 of the 473L Type A consoles.

1. MESSAGE ARRIVES; DATA SYNCHRONIZER FLAG IS RAISED.



2. FLAG IS RECOGNIZED; FIRST CHARACTER IS ACCEPTED.



3. COMPUTER IS INTERRUPTED; INPUT DESCRIPTOR IS ACCEPTED.

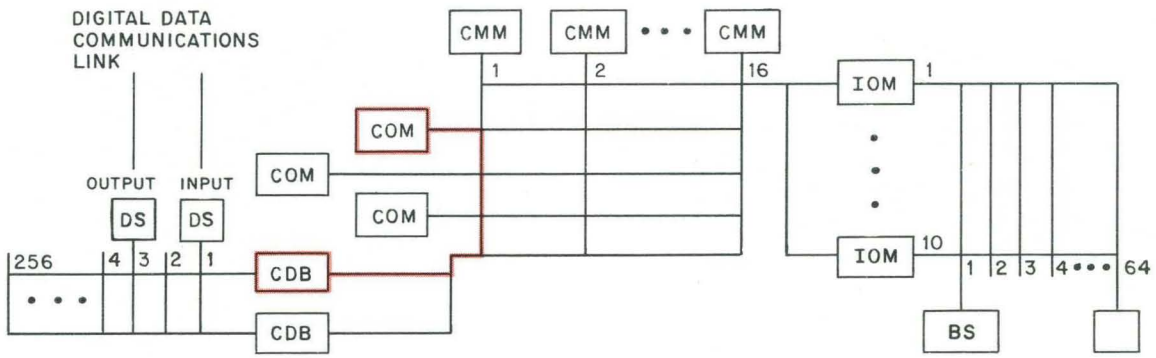
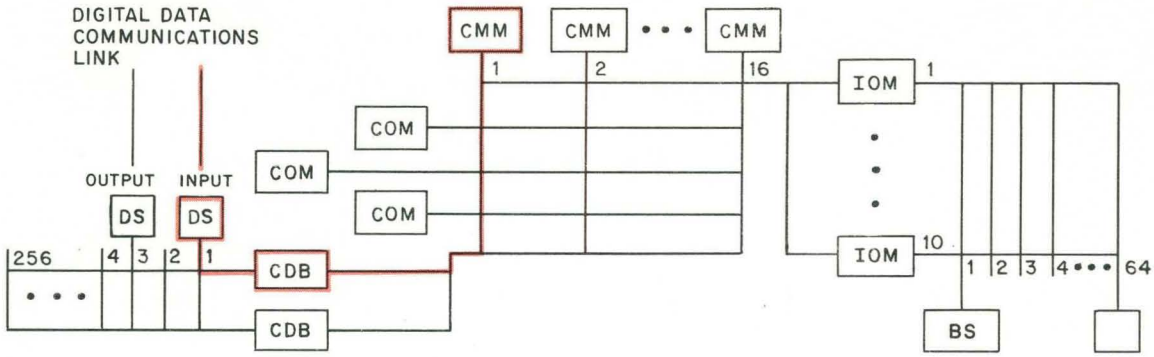
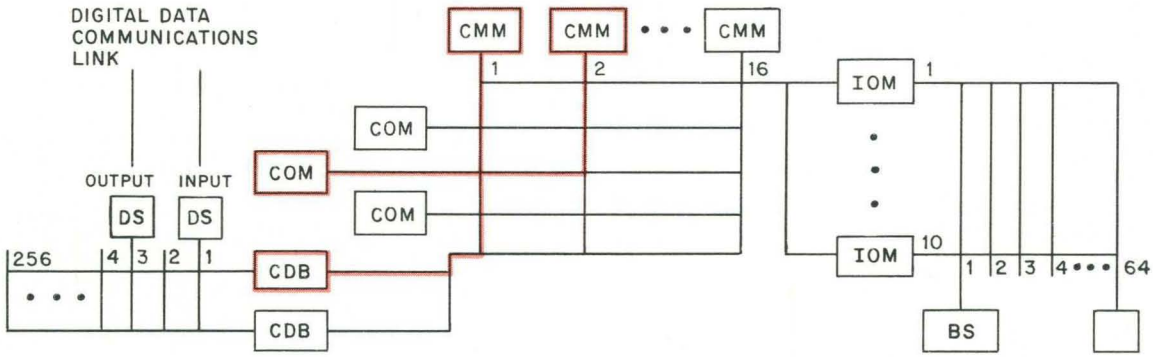


Figure 7. Message Flow Pattern
(Sheet 1 of 2)

4. MESSAGE IS FORMED IN MEMORY.



5. COMPUTER PROCESSES MESSAGE; SENDS "ACKNOWLEDGE" TO CDB.



6. FILES ARE UPDATED; "ACKNOWLEDGE" IS TRANSMITTED.

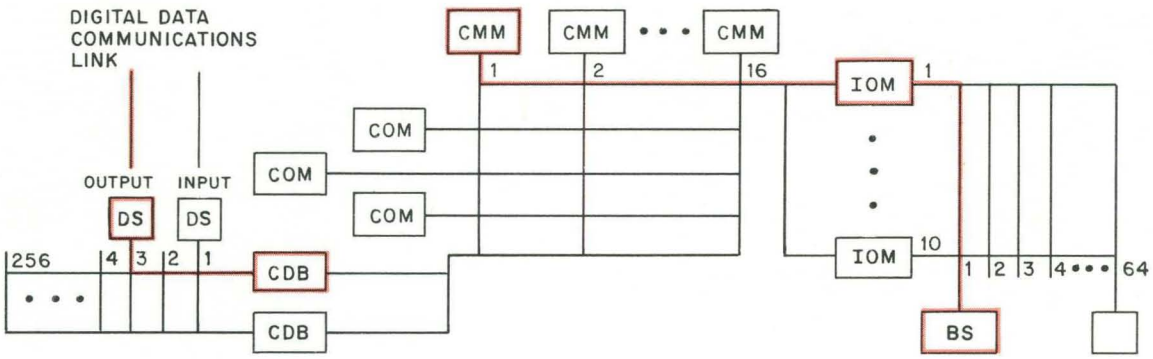


Figure 7. Message Flow Pattern
(Sheet 2 of 2)

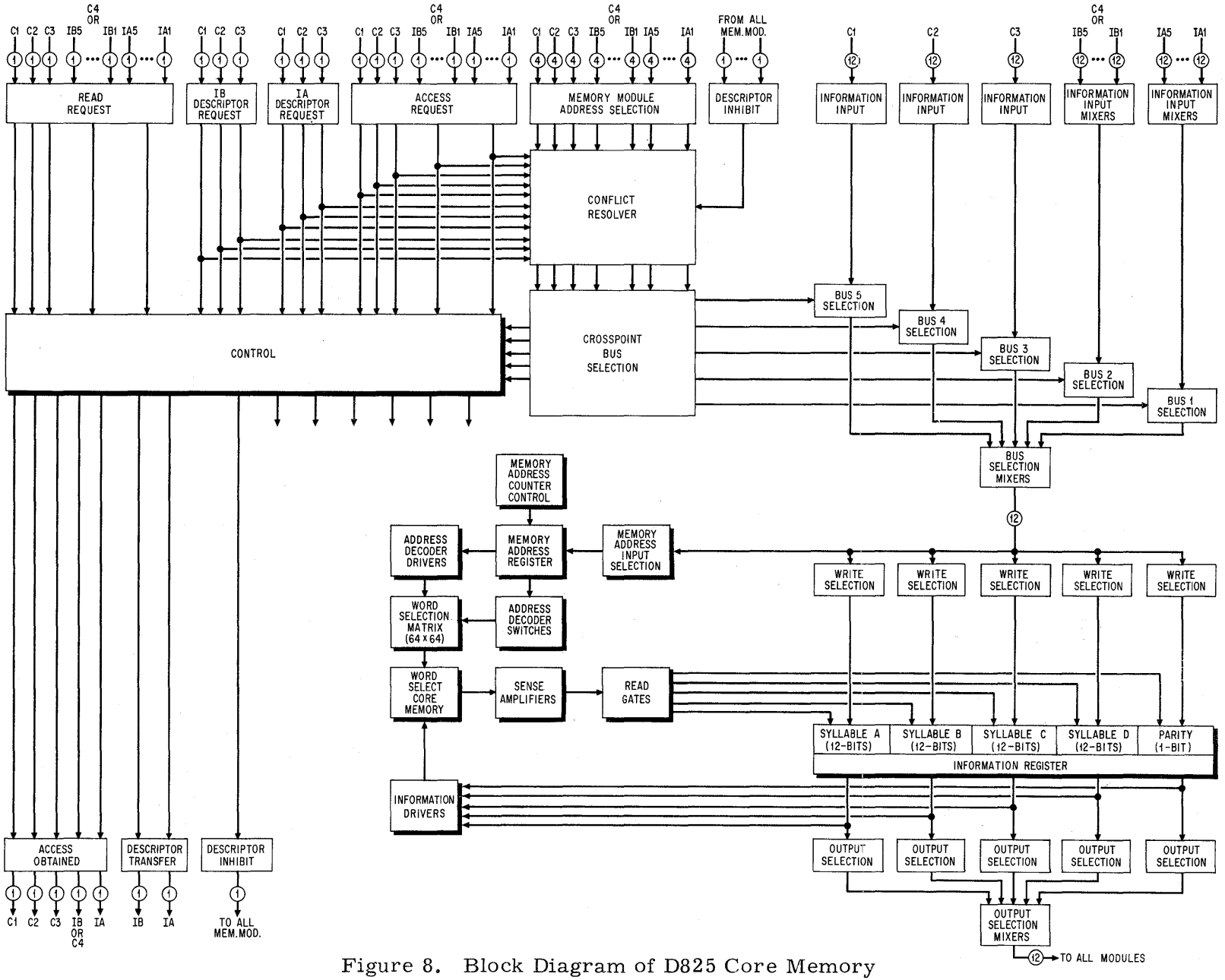


Figure 8. Block Diagram of D825 Core Memory

RECORD EQUIPMENT

The unit record equipment to be used in the 473L system has been selected from standard highly reliable equipment. In all units the electronic circuitry is solid state.

Card Reader

The card reader to be used is the Burroughs B122 model; cards are read by column photoelectrically at a rate of 250 cards per minute. One I/O input channel is required per unit.

Card Punch

The Burroughs D825-41 card punch feeds, punches, checks, and stacks 80-column cards in both standard and postcard thicknesses at a rate of 100 cards per minute. The punch requires one input-output pair of buses per unit.

Line Printer

The high-speed line printer requirement is met by the Analex Model 300. With a repertoire of 96 characters, it prints 300 120-position lines per minute, twice the required rate. One I/O channel is required per unit. An Analex printer is also being used in the D825 installation for NRL.

DIGITAL STORE

CORE MEMORY

The IOC installation of the 473L system will require four of the D825 memory modules. This will provide an interim excess of close to 100,000 bits. If the COC requirement of double the IOC requirement remains firm, only three additional memory modules need to be added to the system. The full D825 system can accommodate 16 memory modules or 3.15×10^6 bits, a growth capability above COC of 400 percent.

Organization

Each D825 Memory Module (Figure 8) contains a random access, linear select, ferrite core memory of 4096 words. Each word contains 48 information bits and one parity bit The modules also contain independent

read, write, and addressing circuitry, a data register and control and storage circuitry for resolving conflicts.

Operation

Memory Operation

Read requests are made to a particular Memory Module by transmitting the 12-bit address of the desired word to the module. Less than one microsecond after the completion of this transmission, the desired word is in the module's data register, and word regeneration and transmission of the word to the requesting module then begins in parallel. The complete cycle requires four microseconds. Likewise, the complete cycle for writing new information into memory, including the transmission to memory of both the word address and the data, also requires four microseconds.

Conflict Operation

In the event that two or more buses (or the devices terminating them) wish to be connected to the same Memory Module, the conflict is resolved by a priority scheme with the highest priority request being immediately granted and the lower priority requests being held in abeyance and being serviced immediately on completion of the higher priority request. Even in the event of the simultaneous occurrence of a number of conflicts, conflict resolution is performed in parallel with no lost time to any of the Memory Modules involved in the conflicts.

RTI - AUXILIARY STORE

The IOC configuration will require two of the D825 drum cabinets to meet the specified requirements for the read time and the auxiliary store. A single D825 drum cabinet contains two drum modules of 1,000,000 data bits each.

The RTI drum cabinet will be implemented with only one drum module for IOC. An additional drum cabinet is indicated for COC. This configuration will meet the requirement in the COC that the RTI store be physically separated from each other and will provide a growth capacity of 100 percent in each of the cabinets. Two of the total of 64 input-output channels of the IOM is required per drum cabinet.

The Auxiliary Store requirement for IOC is met with a single drum cabinet implemented with two drum modules. The COC requirement is met with an additional drum cabinet. For growth, additional drum cabinets may be connected to the input-output bus.

The D825 drum is organized into 45 7-bit bands, each band containing 512 48-bit data words. The drum rotates at a speed of 7200 rpm, and a 6-bit character plus parity is read every 2.04 microseconds. Three hundred thousand bits may be read into core storage in less than 1.5 seconds.

BULK STORE

The IOC configuration requirements for bulk store will be met by a Telex 1A disc file. The use of this disc file will permit the servicing of eight 1,000-bit records in less than 0.5 seconds on the average.

There are over 155 million bits of storage available in the Telex 1A, with an addressable record length between 250 and 12,650 bits. The transfer rates are approximately 250 kc for the inner zone and 500 kc for the outer zone; the average access time is 53 milliseconds.

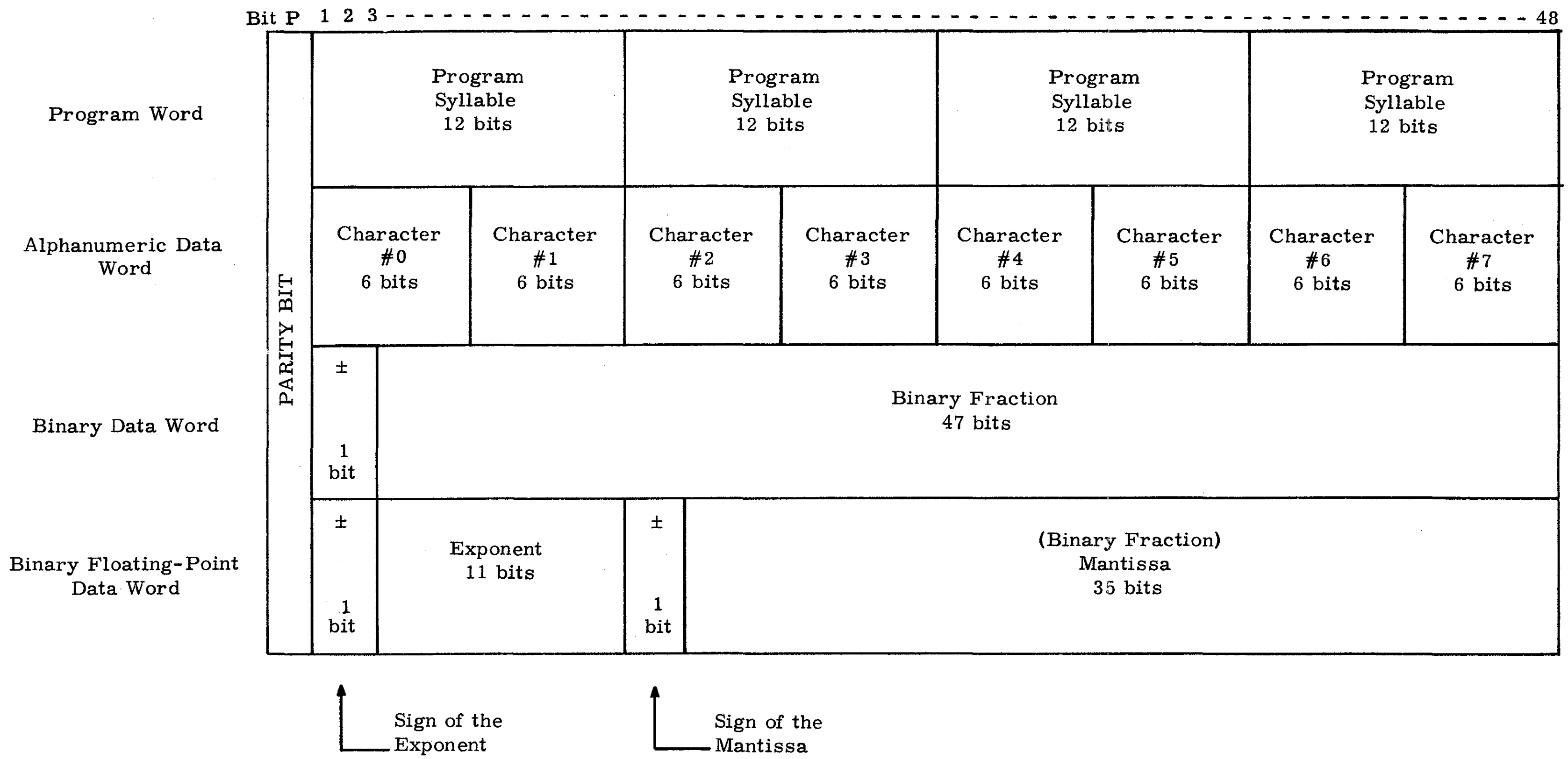
The COC and growth requirement can be met by the addition of more of these units. Each additional unit requires a pair of channels through the Input-Output exchange to the IOM's.

A disc file is at present under development by Burroughs which should be available as an off-the-shelf item in time for the COC installation. This D825 disc file will have a capacity of close to 400 million bits on a total of 13 discs, with an average access time of 16.65 milliseconds. The design utilizes a head per track; therefore, parallel bit readout is possible.

MAGNETIC TAPE

The D825 Magnetic Tape unit is compatible with the requirements for the 473L system.

Data may be stored in the Magnetic Tape unit in two densities, either 200 or 555.5 frames per inch. One frame contains either 6 binary bits or one 6-bit alpha-numeric character. Tape speed is 120 inches per second, giving a transfer rate of 24,000 characters per second for a density of 200 frames per inch, and 66,660 characters per second for a density of 555.5 frames per inch. Packing density is selected by a switch on the unit.



The conventions used in the above data words are:

"1" = minus
"0" = plus

Numbers are represented in signed magnitude form.

Figure 9. D825 Word Formats

Tape format consists of 7 recorded channels across the tape. The 6 information tracks represent either a single alpha-numeric character per frame or 6 bits of binary information per frame, and the seventh track provides a parity check for each frame.

The D825-40 Magnetic Tape Module accepts data in either binary or single-frame alphanumeric form and tape format is compatible with IBM Model 729-II and 729-IV magnetic tape units.

DATA PROCESSOR

The programming of the Compare Macro utilizing the D825 Computer Module yields a processing time of 0.885 seconds. Thus, with a single computer module the D825 system more than meets the 473L IOC processing requirement; with two modules the COC requirement is met with approximately 20 percent spare capability; and with the full three computer complement the growth requirement is met with more than 30 percent spare capability.

CHARACTERISTICS

The D825 Computer Module operates upon 48-bit fixed-point binary numbers, binary floating point numbers of 36 bits mantissa and 12 bits exponent, or alphanumeric words of 8 6-bit characters. The Word Format is given in Figure 9.

The basic clock rate of the D825 Computer Module is 3 megacycles, resulting in:

- Fixed point add — 2.00 μsec
- Fixed point multiply — 42.00 μsec
- Floating point add — 10.67 μsec
- Floating point multiply — 32.33 μsec
- Average equivalent single-address instruction rate — 125,000/sec

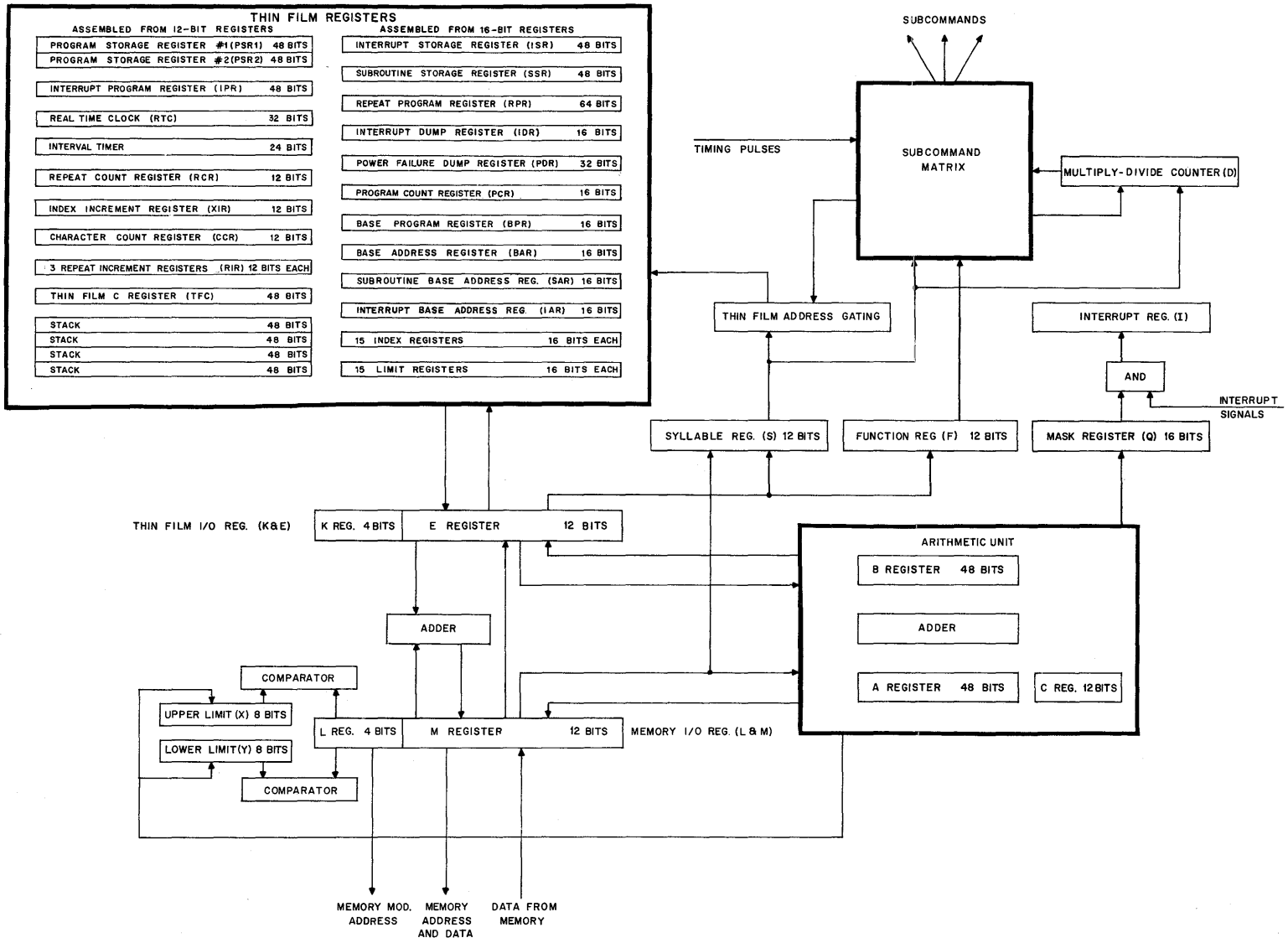


Figure 10. Block Diagram of D825 Computer Module

The D825 is characterized by:

- 12-bit syllable instruction format -- independent of word boundaries
- Operand stack for intermediate high-speed storage permits 0, 1, 2, 3 address operation
- Direct, or infinite-level indirect addressing
- Thin film magnetic storage replaces flip-flop registers
- Retention of data upon primary power failure

There are 15 index registers and 15 comparison limit registers in the D825 Computer Module. Any 3 of the index registers may be addressed by each index address syllable and used to modify each operand address. The index registers may be incremented, decremented, and compared in six different ways with the comparison limit registers.

ORGANIZATION

The Computer Module (Figure 10) consists of three functional areas: the arithmetic unit, the local storage section, and the control section. The first area, the arithmetic unit, is made up of three registers, A, B, and C, with associated controls. The second area is a set of 53 registers contained in a small thin-film magnetic storage. The third area is the control section which includes capability for indexing, address accumulation, indirect addressing, and the command and subcommand matrices.

The Memory-I/O register (L and M) is a multipurpose register. To initiate a memory transfer, the memory address is transferred to the Memory-I/O register. The portion of this address is the L register which designates a specific Memory Module and is sent as dc levels to the switching interlock circuitry of the memory trunk. Address data for the Memory Module and information words entering the Computer Module from the memory module are transmitted through the M register 12 bits at a time.

The A register, B register and C register are the working arithmetic registers of the Computer Module. A register is capable of shifting in optimum combinations of 12, 6, and 1 places to the right and iteratively 1 place to the left.

The function register (F) is a 12-bit register that holds the operator syllable being executed and provides the dc levels for driving the command and subcommand matrices.

The five operand registers include four operand stack registers which make up the thin-film operand stack, and the thin-film C (TFC) register which is used to store the least significant half of a double-length product and the remainder for division.

The two program-storage registers (PSR1 and PSR2) provide storage for eight instruction syllables and permit overlapped instruction fetch during long instructions.

The base address register (BAR) holds the base address of the data direct-address area. The base program register (BPR) holds the base address of the program address area. The program count register (PCR) holds the address of the next instruction to be fetched from memory. The subroutine base address register (SAR) contains the base address of a list of subroutine addresses. When a subroutine is executed, the subroutine storage register (SSR) holds subroutine return information, i.e., the former contents of the BAR, BPR, and PCR.

INTERRUPT

Each Computer Module has an interrupt register which can be set through the interrupt mask register. When a particular condition has set a one at some bit position in the interrupt register, a program interrupt occurs. This interrupt stops the program being executed, stores sufficient registers to allow continuation of the interrupted program at a later time, and transfers control to a routine in an AOSP to service the interrupt.

The interrupt system registers provide storage for data in the operational registers in the event of an interrupt. The interrupt base address register (IAR) contains the base address of the interrupt routines; the contents of this thin film register are protected during the normal operation mode. The interrupt storage register (SR) holds interrupt return information, i.e., the former contents of the BAR, BPR, and PCR. The interrupt program register (IPR) provides storage for the contents of the presently addressed PSR during interrupt. The interrupt dump register (IDR) holds the PSR and repeat controls for interrupt return. The power failure dump register (PDR) holds the contents of the control flip-flops and the flip-flop interrupt register in the event of a power failure.

Primary Power Failure

There is an over-under voltage detector which detects and signals excursions of primary power beyond fixed voltage limits. The out-of-tolerance signal causes the computer module to store sufficient information to restart the program without loss of data. Provision is made for automatic program restart by automatically reloading stored data back into the flip-flop registers. The power supplies themselves have a sufficiently long

time constant to protect the hardware, program, and data from all primary power transients and failures, allowing continuation of the program when stable primary power is restored.

SPEED (COMPARE MACRO)

A single D825 computer module performs the prescribed 40,000 compare operations in 885,227 microseconds. Of this total, 576,515 microseconds are spent doing the 32,029 cases which do not involve crossing word boundaries (exclusive of time for shifting of characters and executing branching). 265,424 microseconds are similarly spent doing the 7971 cases involving split fields. Shifting consumes 20,000 microseconds and branching consumes 23,288 microseconds.

Table I presents the distribution of the 40,000 cases in the Compare Macro problem, the detailed distribution of cases involving crossing D825 word boundaries, and the detailed distribution of computer time necessary to execute the Compare Macro problem.

The D825 order code and basic design features aid in performing field operations as well as word operations. Foremost among these design features are the fast-access thin film memory and the implicit indexing which is provided by the automatic relative addressing characteristic of the D825. The thin film memory is used to hold one memory field being examined for equality with other fields. The base address register of the machine is set to the base address of the packed array of fields in main memory with which the first field is being compared.

The simple case, not involving the crossing of word boundaries, is handled with the single instruction:

```
A:      CEF 222     WORD     F     EQ
NEQ:    ... ...     ....
```

The key field lies left-justified in implicit thin film memory address zero. The CEF instruction compares a partial field of the word in implicit thin film memory address zero with an equal length field in the word taken from the main memory location (WORD plus contents of implicit index register zero). The position and length of the field to be extracted is specified in syllable F. F also specifies how many character positions to shift the extracted field to line it up for comparison with the word in thin film memory address zero. EQ tells what program address to branch to if equality is found.

TABLE I

Distribution for Compare Macro

Distribution of 40, 000 Field Positions

FIELD LENGTH (# CHARACTERS)	START POSITION (CHARACTER NUMBER) 1	2	3	4	5	6	7	8	MARGINAL FIELD LENGTH DISTRIBUTION
1	1, 000	143	143	143	143	143	143	143	2, 000
2	2, 200	314	314	314	314	314	314	314	4, 400
3	4, 800	686	686	686	686	686	686	686	9, 600
4	6, 600	943	943	943	943	943	943	943	13, 200
5	3, 600	514	514	514	514	514	514	514	7, 200
6	1, 000	143	143	143	143	143	143	143	2, 000
7	800	114	114	114	114	114	114	114	1, 600
TOTAL	20, 000	2, 857	2, 857	2, 857	2, 857	2, 857	2, 857	2, 857	40, 000

Distribution of Compare Times

	COMPARISON FIELD NOT SPLIT				COMPARISON FIELD SPLIT		
	FIELDS LINED UP		FIELDS NOT LINED UP		EQ	NOT EQ	
	EQ	NOT EQ	EQ	NOT EQ		FIRST PART EQ	FIRST PART NOT EQ
SHIFTING μS	0	0	1.00	1.00	1.00	1.00	1.00
BRANCHING μS	0.33	0.67	0.33	0.67	0.67	1.33	0.67
REMAINDER μS	18.00	18.00	18.00	18.00	44.92	45.00	18.00
NO. CASES	8, 000	12, 000	4, 811	7, 217	3, 188	1, 338	3, 445
TOTAL SHIFT TIME	0	0	4, 811	7, 217	3, 188	1, 338	3, 445
TOTAL BRANCH TIME	2, 667	8, 000	1, 604	4, 811	2, 126	1, 784	2, 297
REMAINDER	144, 000	216, 000	86, 605	129, 910	143, 212	60, 196	62, 015
TOTAL	146, 667	224, 000	93, 020	141, 938	148, 526	63, 318	67, 757

TABLE I

(continued)

Detailed Distribution of Cases Involving Crossing of Word Boundaries

A	Start Position (Character Number)	3	4	5	6	7	8	Total
B	Number of cases involving crossing of word boundaries	114	257	771	1,714	2,400	2,714	7,971
C	Number which test for not-equal (60% of B above)	69	154	463	1,029	1,440	1,629	4,783
D	Number of C above for which inequality shows up on first part comparison	68	149	434	900	1,080	814	3,445
E	Number requiring two comparisons (C - D)	1	5	29	129	360	814	1,338

For the split field case, the following coding is used:

B:	CEF 222	WORD	F1	TEQ
NEQ:	... ...	....	..	...
TEQ:	SSD	CEF 222	WORD+1	F2
	EQ	SSU	UCT	NEQ
EQ:	SSU	... ...	.....	...

The key field in this case lies in two consecutive thin film memory positions. The field is split in the same way as the comparison field. The two parts of the key field are each left-justified, one in each of the two thin film locations.

Code line B compares the first of the two separate parts of the key word with the first part of the comparison field. Since these parts are not lined up, the shift syllable F1 will call for a shift prior to comparison. F1 also provides for and specifies the extraction to be performed on the memory word containing the first part of the comparison field.

All cases of equality (3188 in number) plus all cases of inequality for which the first portions happen to be equal (1338 in number -- see detailed distribution of cases involving crossing of word boundaries (Table I)) will take the branch to TEQ (tentatively equal). Here the thin film memory pointer

becomes stepped (SSD) to point to the second part of the key field. A second comparison is then made, this time using WORD + 1, which contains the second part of the comparison field in the most significant position. The syllable F2 specifies the necessary masking but does not call for any shifting, since the two parts being compared are already lined up in the most significant ends of their respective words.

Both exits from this comparison (1338 to NEQ, 3188 to EQ -- see Table III) will lead first to an instruction (SSU) which restores the thin film memory pointer to its original position.

Figure 11 is a flow chart corresponding to the above coding for the split field case.

Table I classifies the 40,000 cases by starting character position and field length. The lower right hand triangle of Figure 11 contains the 7971 cases involving crossing of word boundaries.

Half of the packed comparison fields are assumed to be left-justified like the key field. The other half are assumed to begin in character position 2 through 8 with equal frequency. Shifting thus applies to half of the 40,000 cases. From the discussion above, it is to be noted that when shifting

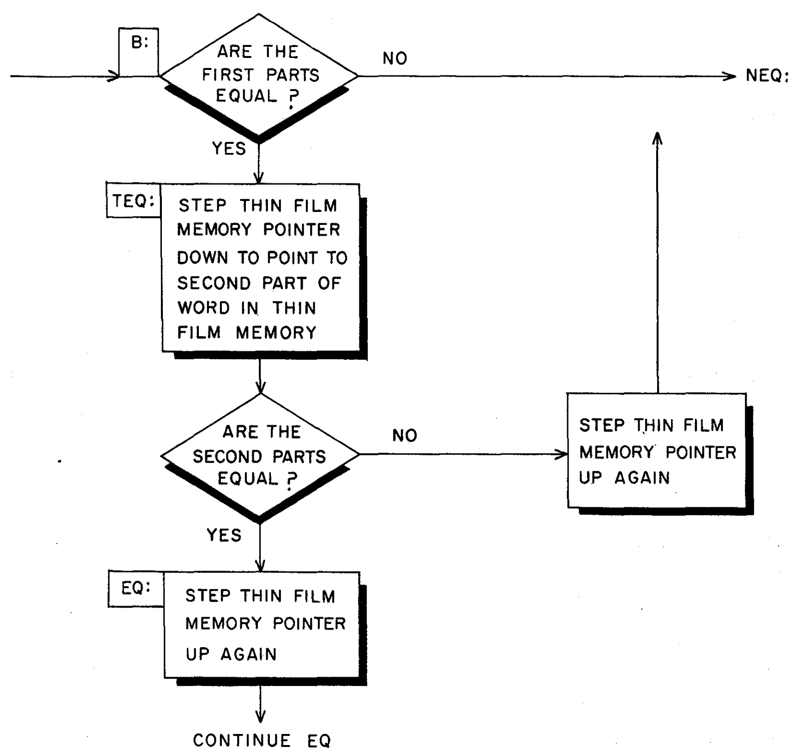


Figure 11. Compare Macro Flow Chart for Split Field Case

occurs, only one shift operation is required. The average amount of shift required for these 20,000 cases is 4 character positions. Whenever N character positions of adjustment are made, 0.33 microseconds each of additional execution time are required for N - 1 of these adjustments. Taking N = 4 for each of the 20,000 cases requiring shifting; 20,000 X 3 X 0.33 = 20,000 microseconds to suffice to take care of the shifting.

It was assumed that 40,000 of the comparisons found equality to hold. Branch syllables (EQ, TEQ, NEQ) give rise to either 0.33 or 0.67 microseconds of execution time according, respectively, as the branch is executed (equality holds) or is not executed (inequality holds).

The distribution of compare times in Table I shows how much branch time is involved in each of the seven cases into which the present problem divides. This table shows that 32,029 cases did not involve the crossing of word boundaries. Of these, 20,000 were those 50 percent of the cases where comparison field was assumed to be left-justified and thus already lined up with the key field. No shifting is required for these 20,000 cases.

For all 32,029 of the NOT SPLIT cases, the comparison is resolved with the expenditure of 18 microseconds plus shifting and branching time (about 19 microseconds total on the average).

The 7971 cases involving the crossing of word boundaries require an average of 35 microseconds to yield resolution of whether the two words being compared are equal or not. When the two words are, in fact, equal, it takes two major steps costing 46.58 microseconds to establish the equality. This applies to 40 percent of the 7971, or 3188 cases.

Of the 4783 cases of non-equality among the split-field cases, most (3445) can be resolved in one comparison costing 19.67 microseconds. The determination of how many of the 4783 cases would manifest the equality on the first part comparison only was made using the assumption that if two N-character fields are unequal, the probability is $1 - (1/2)^k$ that the inequality will show up on consideration of the first k characters alone ($k < n$).

REAL TIME INDICATORS

Each computer module has provision in its thin-film storage for real time clocks. The existing D825 design implements one 24-bit clock register, whose contents are automatically read out and decremented once every 10 milliseconds. This real-time clock may be sampled under program control or, through use of a control flip-flop, can be counted down and used to initiate an interrupt when the count reads zero. The clock range is zero to approximately 46.6 hours in 10-millisecond increments.

To meet the 473L specifications for real time indicators, the following changes will be made:

Real Time Clock

A new 32-bit field (presently spare) of thin-film storage will be provided for the real time clock. The contents of this 32-bit register are automatically read out and decremented once every millisecond. This real-time clock may be sampled (read out or loaded) under program control or, through use of a control flip-flop, can be counted down and used to initiate an interrupt when the count reads zero. The clock range is zero to approximately 49.7 days in one millisecond increments.

Interval Timer

With the decrementing rate increased from once every 10 milliseconds to once every millisecond, the presently available 24-bit clock will fully satisfy the requirements of the interval timer. This interval timer will have the added advantage of being capable of being sampled under program control, while meeting the basic requirement of being preset, then counted down and used to initiate an interrupt on reaching zero. Its clock range is zero to approximately 4.66 hours in one-millisecond increments.

PROCESSOR INTERRUPT CAPABILITY

A comprehensive and flexible interrupt system is a part of the D825 system; its function is principally that of notifying the AOSP of exceptional conditions -- input-output request, parity errors, etc.

The D825 interrupt system is the built-in electronic facility by which the entire D825 system complement can signal the AOSP that some element of the system is not operating properly or that control of some type is needed. Each computer module contains a 12-bit interrupt register, including 2 spare bits and a 22-bit register. There are 13 conditions which can cause an interrupt:

	1.	Primary power failure
	2.	Increment real time clock
	3.	Increment interval timer
X	4.	Restart after primary power failure
	5.	16 external requests
	6.	I/O termination
X	7.	Interrupt computer N
	8.	Real time clock overflow
	9.	Write out of bounds
	10.	Illegal instruction
	11.	Internal parity error
	12.	Arithmetic overflow
X	13.	Normal Mode halt instruction

Three of the bits in the interrupt register are set directly by the occurrence of an interrupt condition. These conditions are 4, 7, and 13 (indicated by "X").

Six others are set only if the corresponding mask bit is a ONE when an interrupt occurs. These conditions are 6, 8, 9, 10, 11, and 12 of the preceding table. One bit is set during normal mode operation by any or all of the sixteen "external request" interrupt conditions in coincidence with their individual mask bits. The remaining interrupt conditions (items 1, 2, and 3) require neither mask nor interrupt register bits. These two conditions are of the highest priority and lead to the automatic processing of the interrupt, while the other interrupt conditions lead to the AOSP processing of the interrupt.

Mask register bits are assigned to the computers by the AOSP in order that:

- local interrupt conditions can either be ignored or processed by the computer in which they occur, and
- system interrupt conditions can be assigned to any computer in the system, depending on the work load and urgency of the request.

A bit in the interrupt register is reset only when the interrupt which set it has been processed. At the end of each instruction or completed iteration of a repeated instruction, the computer is available to process an interrupt condition. If either of the two highest priority conditions exist, the higher one will be processed immediately. If neither of these conditions exists but some bit in the interrupt register is set, the computer will process the existing interrupt condition of highest priority, provided it is not already processing one.

Processing of the Interrupt Conditions

The three highest priority interrupts, primary power failure, count down of the real-time clock, and count down of the interval timer, are processed automatically, i.e., do not involve an AOSP or ordinary control mode operation, and are therefore classified as pseudo interrupts.

The count real-time clock and interval timer signal occurs approximately every millisecond. This interrupt condition is processed by the hardware; it cannot upset the running of any program and can delay it only briefly (7.34 μsec). The processing is a matter of reading the contents of the RTC (or interval timer) from thin film, incrementing it, writing it back into thin film, and setting the RTC (or interval timer) overflow interrupt bit if the overflow condition occurred.

Handling of the 10 interrupt conditions recorded by the interrupt register involves transfer to the control mode of operation, wherein the appropriate AOSP routine will service the interrupt. Transfer from the control mode back to the normal mode is the responsibility of AOSP and is accomplished by using the IRR instruction.

ERROR CHECKING

Two primary means for error checking are employed in the D825: (a) special error checking facilities in the hardware system, and (b) special error checking facilities in the programming system. The hardware system monitors the system operation in several fixed pre-determined ways; the programming system allows checking in an unlimited number of ways within the constraints of program storage capacity. All detected errors are manifested as interrupt conditions, and are brought to the attention of the operator for corrective action.

Automatic Indication

Error indications are made via special printer output messages as well as via the indicators on the control panels associated with the system modules. Specific checks, both hardware type and programmed, on processor and storage operations, are further described.

Processor Operations

Error checks made by hardware within each computer module are as follows:

- Detection of illegal computer instructions
- Parity checks on all data received from the memory modules
- Detection of the lack of response of an addressed memory module
- Detection of attempts by the computer module to write data into a pre-designated "out-of-bounds" memory area
- Detection of arithmetic overflow.

All of these checks are made unconditionally and continuously during computer operation.

Programmed error checks take many forms: a common check is a programmed interrupt of the computer operation at conveniently spaced intervals for the execution of simple confidence tests. Successful completion of such tests will cause an appropriate printout on the supervisory printer. An incorrect output, or the lack of an expected output at the pre-specified intervals, indicates error.

Storage Operations

Although all storage operations are continuously and unconditionally monitored, all the hardware involved in the on-line monitoring is located within the modules which communicate directly with memory, namely, the computer and interface modules. For this reason all hardware error checks are listed as Processor Checks.

Programmed error checks on storage operations are based on periodic confidence tests similar to those used for checking processor operations, and are, in fact, integrated into the programmed processor checks. Each memory module is routinely addressed in the course of these checks.

RELIABILITY

The basic reliability criterion for the 473L Data Processing Subsystem is "availiability" or expected percentage of up time. The factors affecting subsystem availability, namely, equipment failure rates and the effect of down time due to scheduled and unscheduled maintenance, have been minimized by conservative design and optimum machine organization. The estimated availability for the IOC phase is 0.875, based on a system failure rate of 0.095 failures per hour, an average recovery time of 1 hour, and down time of 1 hour per day for preventive maintenance.

A marked improvement in availability is estimated for the COC and Growth phases, 0.99951 and 0.999989, respectively. This is directly attributable to the modular system configuration which permits individual module failures without affecting overall system performance. It also permits individual modules to be serviced for preventive maintenance without incapacitating the entire system.

The electronic part failure rates used in the above estimates were obtained from the RADC Reliability Handbook and are conservative for present-day high-reliability component parts. The failure rates of the mechanical and electromechanical equipment are a function of preventive maintenance and can be kept appropriately low by a vigorous maintenance program.

The calculation of availability for the COC and growth phases, in which spare modules of each type are available, is based on a queuing model

in which the subsystem is considered available unless there are insufficient modules of each type required to maintain basic system performance.

MAINTAINABILITY

Whenever the system error checking facilities reveal a malfunctioning or suspicious module, that module will functionally be disconnected from the operating system, and further exercises and tests will be performed on it to isolate the trouble. When a module is isolated the checkout is conducted under control of the module's own control panel.

Periodic dynamic tests and inspections are employed in maintenance of the storage, record, and the character demand devices. Automatic error indicators, self-checking features, and systems tests can be performed to determine the existence and location of faults.

An outline of the tests which may be performed on each of the major modules follows.

Module Test

The suspect module is isolated from the operating system and tested completely locally, with the module logic being exercised dynamically and statically by the operator.

Channel Test

The interface module is tested with an input-output device to test interface module-device intercommunication and operation.

The memory module is tested with an isolated computer module or interface module to test memory — computer or memory-interface module intercommunication and operation.

Memory Test

The failed interface module is tested with an isolated memory module to test the interface module-memory intercommunication and operation.

A failed computer module, isolated from the operating system, is exercised together with a similarly isolated but operational memory module.

Subsystem Test

An interface module, a memory module, and an input-output device, isolated from the operating system, can be dynamically exercised in an envitonment approaching the normal operational environment. The operator will manually set up the exercises by operating the interface module control panel.

PROGRAMABILITY

In-House Programming Capability

The Burroughs Laboratories maintains a staff of approximately 40 senior programmers who are involved in program research activities and the development of state-of-the-art program concepts such as the Automatic Operating and Scheduling Program.

Fifteen of these programmers are presently involved in finalizing the design of the programming package for the D825 data processor system.

The programming personnel of both the Computational facility at the Research Center and the staff maintained by the ElectroData Division of the Burroughs Corporation also are available to the Great Valley Laboratory personnel.

Number and Type Instructions

The fact that the D825 Modular Processor was designed specifically for use in command control systems is strongly reflected in its order code. In addition to the standard arithmetic operations, there are included a variety of logical operations, branch operations, comparison operations, and field defined operations, the last particularly useful in processing of alphanumeric data. A complete description of the D825 instruction repertoire is presented in Table II; the D825 Instruction Execution Times are given in Table III.

TABLE II

D825 Instruction Repertoire

MNEMONIC AND OCTAL	INSTRUCTION NAME	SYLLABLE LAYOUT A_1 A_2 A_3				SYMBOLIC DESCRIPTION
ACE-72	Alphanumeric Compare Equal	0	(M)	(M)	B	$(A_1) = (A_2) : A_3$ (alphanumeric)
ACG-71	Alphanumeric Compare Greater	0	(M)	(M)	B	$(A_1) > (A_2) : A_3$ (alphanumeric)
ACL-70	Alphanumeric Compare Less	0	(M)	(M)	B	$(A_1) < (A_2) : A_3$ (alphanumeric)
AIF -40	Adjust and Insert, Field	0	(M)	F	(M)	—
BAD-65	Binary Add	0	(M)	(M)	(M)	$(A_1) + (A_2) \longrightarrow A_3$
BAF-43	Binary Add, Field	0	(M)	F	(M)	—
BDV-60	Binary Divide	0	(M)	(M)	(M)	$(A_1) \div (A_2) \longrightarrow A_3$
BMU-61	Binary Multiply	0	(M)	(M)	(M)	$(A_1) \times (A_2) \longrightarrow A_3$
BRB-26	Branch on Bit	0	(M)	(M)	B	—
BRC-11	Branch on Condition	0	L	B		$A_1 : A_2$
BSF-42	Binary Subtract, Field	0	(M)	F	(M)	—
BSU-64	Binary Subtract	0	(M)	(M)	(M)	$(A_1) - (A_2) \longrightarrow A_3$
CBF-25	Convert Binary to Floating Point	0	(M)	(M)		$(A_1) \longrightarrow A_2$, floating
CEF-52	Compare Equal, Field	0	(M)	F	B	—
CEQ-76	Compare Equal	0	(M)	(M)	B	$(A_1) = (A_2) : A_3$ (algebraic)
CGF-51	Compare Greater, Field	0	(M)	F	B	—
CGR-75	Compare Greater	0	(M)	(M)	B	$(A_1) > (A_2) : A_3$ (algebraic)
CLA-20	Clear	0	(M)			zeroes $\longrightarrow A_1$
CLF-50	Compare Less, Field	0	(M)	F	B	—
CLS-74	Compare Less	0	(M)	(M)	B	$(A_1) < (A_2) : A_3$ (algebraic)
CSE-32	Character Search	0	(M)	C	B	$(A) = A_2 : A_3$
FAD-67	Floating Add	0	(M)	(M)	(M)	floating, $(A_1) + (A_2) \longrightarrow A_3$
FDV-62	Floating Divide	0	(M)	(M)	(M)	floating, $(A_1) \div (A_2) \longrightarrow A_3$
FMU-63	Floating Multiply	0	(M)	(M)	(M)	floating, $(A_1) \times (A_2) \longrightarrow A_3$
FSU-66	Floating Subtract	0	(M)	(M)	(M)	floating, $(A_1) - (A_2) \longrightarrow A_3$
HLT-01	Halt	0				—
IRR -05	Interrupt Return	0				—
LAF-47	Logical AND, Field	0	(M)	F	(M)	—
LAN-56	Logical AND	0	(M)	(M)	(M)	$(A_1) \cdot (A_2) \longrightarrow A_3$
LCF-46	Logical COMPLEMENT, Field	0	(M)	F	(M)	—
LCM-24	Logical COMPLEMENT	0	(M)	(M)		$(A_1) \longrightarrow A_2$
LOF-44	Logical OR, Field	0	(M)	F	(M)	—
LOR-55	Logical OR	0	(M)	(M)	(M)	$(A_1) \vee (A_2) \longrightarrow A_3$
LSR-31	Load Special Register	0	(M)	Vs		—
LTF-30	Load Thin Film	0	(M)	T		$(A_1) \longrightarrow A_2$, thin film
LXF-45	Logical EXCLUSIVE OR, Field	0	(M)	F	(M)	—
LXR-54	Logical EXCLUSIVE OR	0	(M)	(M)	(M)	$(A_1) \oplus (A_2) \longrightarrow A_3$
NOP-00	No Operation	0				—
RPT-10	Repeat	0	Rc	Ri	B	Repeat (A_3), by A_2, A_1 times
RVS-06	Reverse Stack	0				—
SAF-41	Strip and Adjust, Field	0	(M)	F	(M)	—
SER-21	Store External Requests	0	(M)			—
SHF-36	Shift	0	(M)	S	(M)	(A_2) shifted, by A_1, $\longrightarrow A_3$
SRJ -14	Subroutine Jump	0	Ja	Ji		—
SRR-04	Subroutine Return	0				—
STF-15	Store Thin Film	0	T	(M)		Thin film, $(A_1) \longrightarrow A_2$
SSD -03	Step Stack Down	0				$s - 1 \longrightarrow s$
SSU -02	Step Stack Up	0				$s + 1 \longrightarrow s$
TIO -16	Transmit to Input/Output	0	IO	M	B	—
TRM-34	Transmit Modified	0	(M)	Vt	(M)	(A_1), by A_2, $\longrightarrow A_3$
TRS-35	Transmit	0	(M)	(M)		$(A_1) \longrightarrow A_2$
UCT-22	Unconditional Transfer	0	B			$: A_1$
XLC-12	Index, Limit - Compare	0	Ia	Iv	B	—

Accurate times for programs execution may be found by adding to the execution times of Table III the following:

+ 2.00 μsec per stack read*
+ 1.67 μsec per stack write
+ 4.00 μsec per level of indirect addressing**
+ 1.67 μsec per repeated instruction***
+ the individual processing time for each type of syllable used:
  - 1.33 μsec per program operator syllable
  - 5.33 μsec per memory syllable (read)
  - 4.33 μsec per memory syllable (write)
  - 0.33 μsec per branch (if executed)
  - 0.67 μsec per branch (if not executed)
  - 1.67 μsec per index syllable
  - 1.67 μsec per any other type of syllable
+ 5.00 μsec per program word - fetch**
- 5.00 μsec per program word - fetch overlap

*0.33 μsec for a stack if it immediately follows a stack write of the preceding instruction.
**Counted only the first time if repeated.
***Not counted the first time.

(Thin film storage provides enough space for 2 full program words; if 1 word is empty and the present instruction is lengthy in execution, the second word can be filled during the execution. This overlap saves 5.00 μsec. All floating point instructions, as well as BDV and BMU, allow overlap.)

TABLE III

D825 Instruction Times
(in μsec)

ACE:	0.33	first bit different
	2.33	first bit alike
ACG:	0.33	first bit different
	2.33	first bit alike
ACL:	0.33	first bit different
	2.33	first bit alike
AIF:	3.00 + 0.33 (n-1)	n = number of adjustments (1 through 7)
	3.00	if n = 0
AUTOMATIC INTERRUPT JUMP:		7.00
BAD:	1.33	signs alike
	2.00	signs different
BAF:	8.33 + 0.33 (n-1)	n = number of adjustments (1 through 7)
	8.33	if n = 0
BVD:	69.67	
BMU:	24.00 + n	n = number of 1's in the multiplier (A_1), excluding 1's in bit positions 1, 12, 24, 36, 48.
BRB:	0.33	
BRC:	0.33	

TABLE III

(continued)

BSF:	8.33 + 0.33 (n-1)	n = number of adjustments (1 through 7)
	8.33	if n = 0
BSU:	1.33	signs different
	2.00	signs alike
CBF:	1.33 + 0.33n	n = number of shifts-left needed to normalize
	0.33	if the number is zero
CEF:	4.67 + 0.33 (n-1)	n = number of adjustments (1 through 7)
	4.67	if n = 0
CEQ:	0.33	signs different
	2.33	signs alike
CGF:	4.67 + 0.33 (n-1)	n = number of adjustments (1 through 7)
	4.67	if n = 0
CGR:	0.33	signs different
	2.33	signs alike
CLA:	0.00	
CLF:	4.67 + 0.33 (n-1)	n = number of adjustments (1 through 7)
	4.67	if n = 0
CLS:	0.33	signs different
	2.33	signs alike

TABLE III

(continued)

CSE:	1.33 + 0.33n	n = number of character positions examined (1 through 8)
FAD:	6.67 + 0.33 (n+m)	n = number of shifts-right needed (in units of 1, 6, & 12 bits) for lining up the operands, and m = number of shifts-left needed to normalize the result. n = 0 if the absolute value of [the (A_1) exponent minus the (A_2) exponent] is $\geq$ 35.
	2.33	The signs of the exponents of the 2 operands are different, and the absolute value of the sum of the two exponents is greater than 2,047.
FDV:	55.67	No quotient overflow
	56.00	Quotient overflow of 1 position has occurred and been corrected.
	1.33	Exponent overflow or underflow has occurred.
FMU:	21.00 + n + 1.33 (if normalization of 1 position is necessary)	n = number of 1's in the mantissa of the multiplier (A_1), excluding 1's in bit positions 1-13, 24, 36, 48.
	1.67	Exponent overflow or underflow has occurred.
FSU:	6.67 + 0.33 (n+m)	n = number of shifts-right needed (in units of 1, 6, & 12 bits) for lining up the operands, and m = number of shifts-left needed to normalize the result. n = 0 if the absolute value of [the (A_1) exponent minus the (A_2) exponent] is $\geq$ 35.
	2.33	The signs of the exponents of the 2 operands are different, and the absolute value of the sum of the two exponents is greater than 2,047.

TABLE III

(continued)

HLT:	0.00	
IRR:	5.67	
LAF:	7.00 + 0.33 (n-1)	n = number of adjustments (1 through 7)
	7.00	if n = 0
LAN:	0.33	
LCF:	5.00 + 0.33 (n-1)	n = number of adjustments (1 through 7)
	5.00	if n = 0
LCM:	0.33	
LOF:	7.00 + 0.33 (n-1)	n = number of adjustments (1 through 7)
	7.00	if n = 0
LOR:	0.33	
LSR:	0.33	
LTF:	0.67	1 register addressed
	2.00	4 12-bit registers addressed
	4.00	3 16-bit registers addressed
LXF:	7.00 + 0.33 (n-1)	n = number of adjustments (1 through 7)
	7.00	if n = 0
LXR:	0.33	
NOP:	0.00	

TABLE III

(continued)

RPT:	1.00	
RVS:	0.00	
SAF:	1.33 + 0.33 (n-1)	n = number of adjustments (1 through 7)
	1.33	if n = 0
SER:	0.00	
SHF:	0.67 + 0.33n (Single)	n = number of shifts-left, or the number of shifts-right in units of 1, 6, and 12 bits.
	5.33 + 0.67 (n-1) (Double)	n = number of shifts; n is limited to 11 for the 2 left arithmetic shifts and to 12 for the other 6 double shifts.
	0.67	shift of zero
SRJ:	5.33	no overlap of program word fetch had occurred
	6.00	overlap of program word fetch had occurred
SRR:	4.00	
STF:	2.00	12-bit register(s) addressed
	4.33	1 16-bit register addressed
	7.33	3 16-bit registers addressed
SSD:	0.00	
SSU:	0.00	
TIO:	0.00	

TABLE III

(continued)

TRM:	0.33	sign modification
	2.67	round, with or without sign modification
TRS:	0.00	
UCT:	0.00	
XLC:	3.33	

Programming Package

A complete software package is included as deliverable equipment with the D325. This package includes not only standard service routines (memory dump routines, debugging routines, etc.) but also diagnostic routines, the AOSP, and a set of compilers.

The diagnostic routines consist of confidence routines, which are run periodically by the AOSP, and localization routines to pin point any failure discovered by a confidence check. In most cases the diagnostic routines can localize a failure to within two to three circuit cards, and in many cases to a particular card. These routines can be initiated either by the AOSP or manually. Results are printed on the console typewriter.

The compiler set consists of a Symbolic Assembler, a Fortran compiler, a JOVIAL III compiler, and an extended ALGOL '60 compiler. The assembler provides the standard memory allocation function and has built in many useful pseudo-codes. the JOVIAL III compiler is standard, save that many of the COMPOOL functions are assumed by the AOSP. The ALGOL compiler includes as a subset standard ALGOL '60, but has been extended by adding provisions for input/output processing and several new declarations and operations to facilitate list processing and to make available to the programmer the advantages provided by the AOSP.

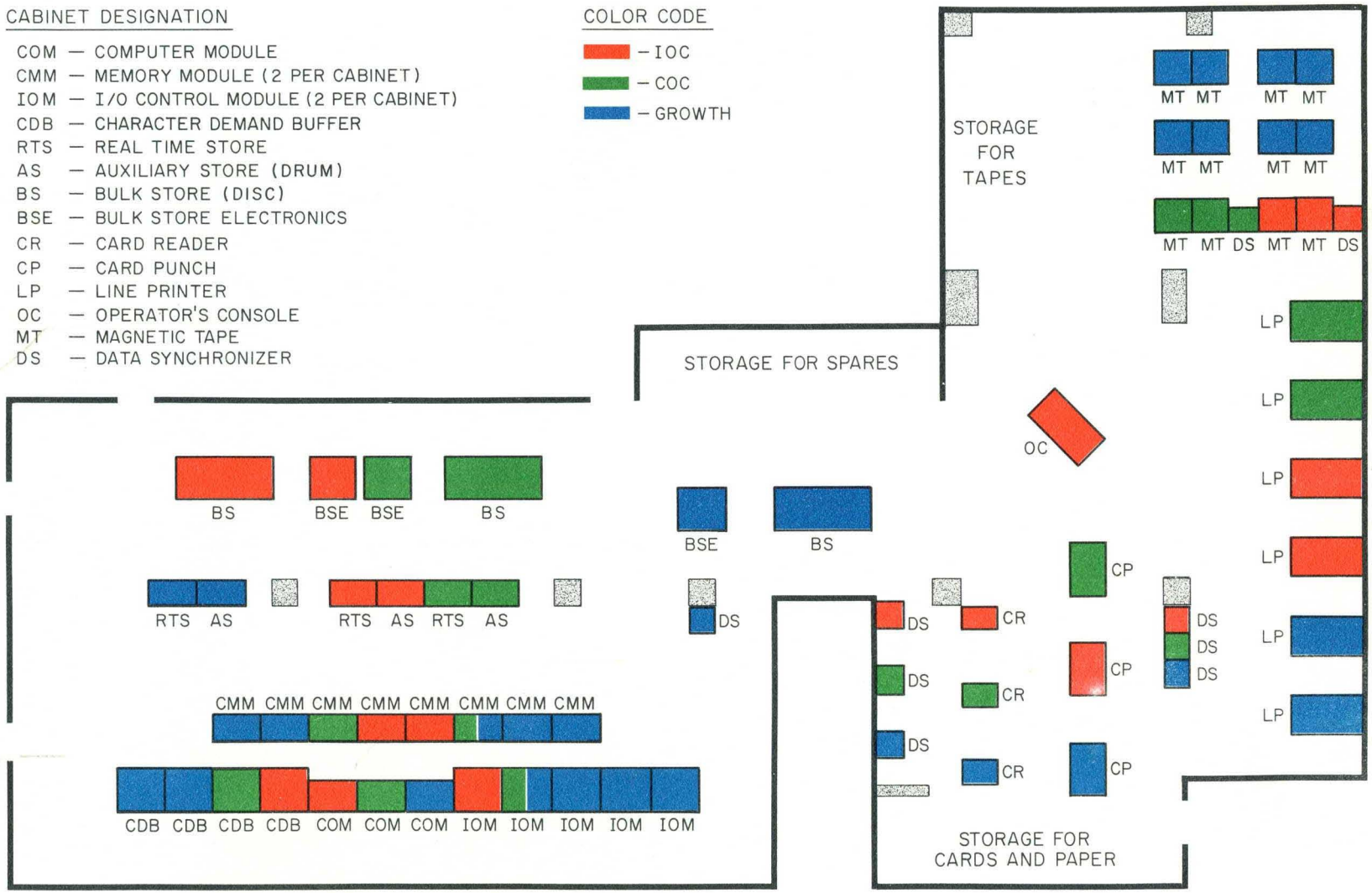


Figure 12. System 473L Physical Layout

SECTION III
PHYSICAL CHARACTERISTICS

OPTIMUM INTEGRAL INCREMENTAL EXPANSION

The D825 Modular Processor system has been designed to permit incremental growth as desired without interruption of system operation. This philosophy of expansion has been applied both to the growth of the data processor itself as well as to the incremental addition of communication modems, displays, record devices, storage devices, etc.

In considering system growth it is necessary to consider the problem in terms of functional compatibility and physical compatibility. The scheduling program (AOSP) which permits efficient functional growth is described under the section Functional Configuration. A floor plan of the proposed physical layout of the 473L system is illustrated in Figure 12. Shown in red are the cabinets necessary for the Initial Operational Capability, in green the Complete Operational Capability, and in blue a possible Ultimate Growth Configuration. This optimum layout will permit growth of all functions of at least 50 percent more than presently required in the COC.

Growth is achievable without interruption of the system operation. Addition of a cabinet involves putting it in place, running the necessary power and signal cables, turning it on, and informing the AOSP of its increased capability by console input keyboard.

The key to the physical expansion of the D825 system is its three interconnection networks, the switching interlock, the input-output exchange, and the display-communications exchange. It is from these networks that the system expands and gains its great advantage of modularity. Ease of growth from a minimum system to a maximum configuration is inherent in the design.

In the D825 system signals are transmitted over coaxial cables; as the cable passes by a unit to which it is to be connected it is tapped and

TABLE IV

Physical Characteristics

MODULE	MANUFACTURER	MODEL	CABINET QUANTITY (Total Required)			SIZE			CLEARANCE				WEIGHT (LBS.)
			IOC	COC	GROWTH	D	W	H	REAR	FRONT	LEFT	RIGHT	
Computer	Burroughs	D825	1	2	3	24"	39"	80"	3'	4'	0	0	1200
Core Memory	Burroughs	D825*	2	4	8	24"	39"	80"	3'	4'	0	0	1200
Input-Output Module	Burroughs	D825*	1	2	5	36"	39"	80"	2'	4'	0	0	1200
Character Demand Buffer	Burroughs	D825	1	2	4	36"	39"	80"	2'	4'	0	0	1200
Real Time Store (Drum)	Burroughs	D825	1	2	3	22"	45"	68"	2'	3'	0	0	1200
Auxiliary Store (Drum)	Burroughs	D825*	1	2	3	22"	45"	68"	2'	3'	0	0	1200
Bulk Store (Disc File)	Telex	1A	1	2	3	36"	84"	60"	4'	4'	2'	2'	2500
Disc File Electronics	Telex		1	2	3	38"	40"	81"	6"	3'	3"	3"	600
Card Reader	Burroughs	B122	1	2	3	18"	30"	14"	2'	3'	3'	2'	150
Card Punch	Burroughs	B303	1	2	3	28"	44"	53"	2'	2'	2'	1'	655
Line Printer	Analex	300	2	4	6	31'	58"	56"	2'	3'	1'	0	1900
Console	Burroughs	D825	1	1	1	30"	60"	45"	2'	2'	0	0	600
Magnetic Tape	Burroughs	BC422	2	4	12	28"	30"	74"	3'	2.5'	0	0	950
Data Synchronizer	Burroughs	D825	3	6	8	22"	23"	48"	2.5'	2.5'	0	0	150

*Two modules per cabinet

entered into the interconnection logic associated with the unit. The driver capability of the signal source is designed to the capacity required of the full system. When a new functional unit is added to the complex, this coaxial interconnecting cable is merely extended.

In terms of physical arrangement the interconnection net of the Data Processing Central is best implemented with two rows of cabinets, one containing all the memories and the other all the computers, CDB's, and IOM's grouped by type. Cabling and expansion are greatly simplified with this layout; for example the output of a computer is carried by two coaxial lines across the aisle between the rows. One cable passes through the cabinets to the left and the other to the right, with each cabinet having a T connector through which the cable passes. At the last T the line is terminated in its characteristic impedance.

Cabinets are designed to be placed side by side so that a row forms a continuous RF tight shield for the cables which pass through it. If growth is planned space should be left in initial floor plans to facilitate cabling of intercomputer control signals. Between nonadjacent cabinets RF shielding is provided by removable cable ducts such as are used to cross the aisle between the rows.

TRANSISTORIZED EQUIPMENT

The D825 modular computer system utilizes advanced circuit and packaging techniques developed and proved by Burroughs in military computing systems for ground-based, mobile, airborne, and shipborne applications.

The physical characteristics of the various D825 modules proposed for the 473L system data processing are indicated in Table IV. The D825 is unique in its orientation toward military related applications. Both the concept and design are products of Burroughs' extensive military equipment experience and detail design criteria for materials, parts, and processes transcend those usually associated with "best commercial practices" and generally parallel the military specification requirements. Component selection has been based upon military standard parts where practical.

ELECTRONIC DESIGN

All modules of the computer system have high reliability circuitry implemented with solid state devices. The logic circuitry of the D825 system employs Burroughs proprietary hybrid transistor-diode logic (HTDL) technique. This circuitry has been proved in a wide variety of severe military applications. Implementation of high speed logic circuitry with the HTDL technique offers important advantages in terms of economy and reliability because of the permitted freedom from rigid component specifications,

large fan-in, fan-out cability, component count reduction, and optimum use of transistor gain-bandwidth product.

Linear select memory techniques which offer the capability of high speed memory operation while allowing greater circuit tolerances and a much greater temperature range are used in both the core memory modules and the thin-film memory of the computer module.

MECHANICAL DESIGN

The computer, memory, interface, and drum modules are housed in identical standard cabinets. Each cabinet has its own power supply. The basic cabinet used for these modules is a front opening steel weldment designed for maximum RFI shielding and optimum component accessibility and cooling. An internally modularized design is achieved by the use of printed circuit cards in the logic circuits, voltage regulation plates in the power supply, and by arrangement of these components on three subassembled racks per cabinet. Two of these racks contain the logic circuitry and the third is the power supply subassembly. The logic racks are essentially identical and are pivoted on a common hinge line to permit switching either one or both racks out for easy access to both the card insertion face and the backplane wiring face. Further modularization is obtained by arranging the thin-film memory as a complete subassembly in the computer module and making the ferrite core stack a subassembly within the memory module.

Controls and indicators appropriate to each functional module are mounted on a cabinet door sub-panel which may be rotated to optionally provide display exposure from either the external or internal face of the door without violating the RFI integrity of the cabinet with the door closed. This feature provides maximum accessibility and visibility with the door either closed normally or open for test and servicing.

Self contained cooling of the cabinets is provided. Front and rear air intakes with RFI protection and dust filtering are located in the lower portion of the cabinet and an exhaust blower exits air at the top rear; separate internal cooling paths are provided for the power supplies and the card racks. Each rack has integral blowers such that adequate cooling air flow is maintained through the card racks even when the racks are pivoted out for test purposes.

WEIGHT AND FLOOR LOADING

The individual weights of the various modular units of the processor and peripheral equipments are indicated in the tabulation of Physical Characteristics (Table IV). Total weights of significant groupings of equipment

as well as total system weights for the various system complement levels are as follows:

SYSTEM LEVEL	GROUP AND SYSTEM WEIGHTS				
	Central Processor	Bulk and Drum Memory	Magnetic Tape Storage	Unit Record	Total System
IOC	6,000	5,800	2,500	6,400	20,700
COC	12,000	11,300	5,000	12,200	40,500
Ultimate	24,000	16,800	15,000	18,000	~~173,800~~ 73,300

The weights for the various equipment categories result in the following maximum floor loadings based on typical configurations and standard 20-foot building bays:

	IOC	COC	Ultimate
Central Processor Group	8	15	30 pounds per square foot
Bulk and Drum Storage Group	10	19	28 pounds per square foot
Magnetic Tape Storage Group	6	13	38 pounds per square foot
Unit Record	8	16	24 pounds per square foot

SERVICE CONDITIONS

TEMPERATURE & HUMIDITY

The rated temperature and humidity ranges for operation and storage of the D825 modular elements and the proposed peripheral equipments are specified in Service Conditions (Table V). The more restricted ranges indicated for the peripheral equipments reflects the fact that these standard, in-being devices -- generally human-computer interface elements -- were directed toward application in environments typical of office buildings and storage areas where a minimum acceptable control over environment for human comfort is exercised. All current service condition ratings are considered highly conservative.

ELECTRICAL

The prime power requirements of the various system elements is also indicated in Table V. All equipments except the card reader require three-phase, four wire prime power inputs. Acceptable tolerances on the 60-cycle power supply for the D825 system is ±10 percent on voltage and ±5 percent on frequency. Over-under voltage detection circuitry is incorporated for protection against line transients. Prime power failure control circuits are capable of detecting and signaling over-under voltage excursions beyond fixed limits. The detecting and signalling of over-under voltages occurs at limits that allow the power supply voltage regulators

TABLE V

Service Conditions

MODULE	MANUFACTURER	MODEL	KVA	POWER			TEMPERATURE (OPERATING)		TEMPERATURE (STORE)		HUMIDITY (OPERATING)		HUMIDITY (STORE)		COOLING AIR	HEAT DISSIPATION
				φ Phase	Voltage	CPS	Low	High	Low	High	Low	High	Low	High	ENTERING CFM	(BTU/HR)
COMPUTER	BURR	D825	2	3	120/208	50/60	0	50	0	75	0	85	0	85	400	6800
MEMORY	BURR	D825	1.5	3	120/208	50/60	0	50	0	75	0	85	0	85	300	5100
I/O CONTROL	BURR	D825	1.5	3	120/208	50/60	0	50	0	75	0	85	0	85	300	5100
CDB	BURR	D825	1.5	3	120/208	50/60	0	50	0	75	0	85	0	85	300	5100
DRUM (REAL)	BURR	D825	1.2	3	120/208	60	0	50	0	70	0	85	0	85	400	4000
DRUM (AUXILIARY)	BURR	D825	1.2	3	120/208	60	0	50	0	70	0	85	0	85	400	4000
DISC FILE	TELEX	1A	5	3	208	60	10	40	-30	65	0	80	0	98	NONE	17500
DISC FILE ELECTRONICS	TELEX	1A	INCLUDED IN FIGURES FOR DISC FILE													
CARD READER	BURR	B122	.35	1	120/208	60	15	38	-45	70	10	90	5	95	NONE	1200
CARD PUNCH	BURR	B303	2.75	1	120/208	60	15	38	-45	70	10	90	5	95	300	9350
LINE PRINTER	ANALEX	300	1.5	3	120/208	60	20	37	0	70	10	80	10	80	500	5100
CONSOLE	BURR	D825	1.2	1	120	50/60	0	50	0	75	0	85	0	85	400	4200
TAPE UNIT	BURR	BC422	3.7	1	115/208	60	19	27	-40	50	40	60	10	90	600	11000
DATA SYNCHRONIZER	BURR	D825	.20	1	120	50/60	0	50	0	75	0	85	0	85	150	700

to supply rated voltages and currents for 500 microseconds after signalling a fault.

SPACE REQUIREMENTS

The basic dimensions of each element of the proposed D825 data processing system are presented in the table of Physical Characteristics (Table IV). As indicated, system space requirements must also account for additional clearances for normal operator or maintenance access as well as those related to nondestruction of normal air flow paths, etc. All of these factors have been considered in the floor layout (Figure 12).

AIR CONDITIONING REQUIREMENT

Each modular equipment cabinet of the D825 system has a self contained blower cooling system with carefully organized circulation paths for the control and removal of internally generated heat. Therefore, the supply of specifically conditioned air to the D825 computer system elements is not required as long as the ambient air temperature is within the ranges specified in Service Conditions (Table V). The cooling air flow rates and the heat dissipation of the various units are also indicated in Table V. The total heat dissipation burdens for full equipment complement operation at the various anticipated system levels is predicted as follows:

IOC	116,200 BTU/Hr
COC	232,000 BTU/Hr
Ultimate Growth	455,700 BTU/Hr

NOISE LEVEL

The primary sources of noise identified with the data processing equipments are primarily mechanism generated noise in the case of some of the input-output devices such as the line printers, card punches, etc., and airborne blower noise from the cooling air exhaust systems of the other units. Each of the proposed equipments reflects normal design attention to the minimization of acoustic noise from these sources. The cowling design of the printer and punch mechanisms offers maximum enclosure and soundproofing consistent with function. All of the D825 module cabinets use low speed (1800 rpm) impeller type exhaust fans especially selected for low noise operation. Although some of the equipments might produce noise levels approaching 60-70 db a few feet from the primary noise source, the use of acoustic ceiling tiling will be adequate to maintain average noise levels in normally occupied areas of the facility in the order of 50-55 db normally associated with average office environments.

ELECTROMAGNETIC INTERFERENCE CE

The D825 Data Processor is designed to meet the Electromagnetic Interference specifications of MIL-I-6051. The features which have been designed into the system to meet this objective include the following:

- Solid welded steel cabinet.
- Two-ply electronic weather stripping completely lining doors and control panels.
- Conductive, maintenance-free coatings to maintain shielding integrity.
- Reversible control panels which permit access to indicators and control switches during maintenance and repair periods and which provide complete interference shielding during normal operational periods.
- External signal interconnections of coaxial cable.
- Power line filtering conforming to MIL-F-15733.
- Waveguide-type filters for air intake and exhaust.

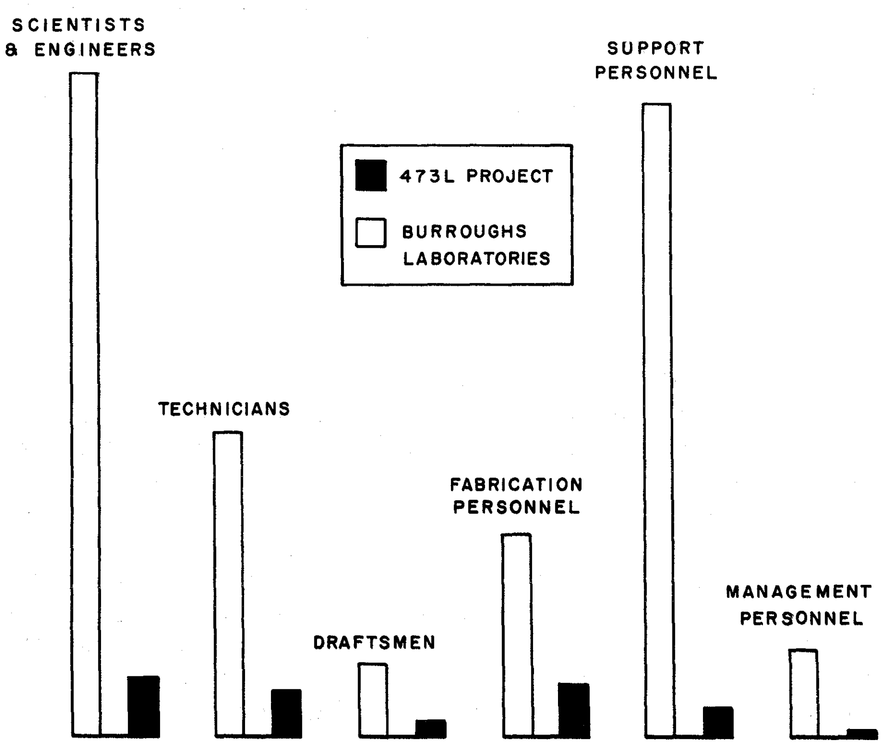


Figure 13. Estimated Manpower Requirements for System 473L Data Processing Equipment Project Compared with Burroughs Laboratories Manpower

SECTION IV
MANAGEMENT

ORGANIZATION

The 473L Data Processing Subsystem Project will be conducted at the Great Valley Laboratory of the Burroughs Laboratories complex at Paoli, Pa. The project will be placed under the technical management of Mr. Robert Williams, who will report to Mr. Norman Skinner, manager of the Great Valley Laboratory. Mr. Williams is presently directing the final stage of development of the D825 Modular Data Processing System for the Naval Research Laboratory. Since the NRL AN/GYK-3 (D825) begun in July 1961, already is in the final system debugging stage, Mr. Williams presently will be able to devote his attention to preliminary planning for the 473L Project. His staff will have been established and ready for action by the 1 May 1962 starting date.

POSITION OF PROJECT

Burroughs is intensely interested in the 473L Project; it offers an excellent opportunity to demonstrate the unusual capabilities of its D825 System. This project has the full endorsement of the Corporation's top management for the employment of whatever measures become necessary toward its successful completion.

Manpower will be ample. Only a portion of the engineering team now on D825 will be needed, since no development effort, as such, will be necessary to convert D825 to 473L system requirements. The relationship of estimated 473L personnel requirements to overall manpower availability at Burroughs Laboratories is indicated in Figure 13.

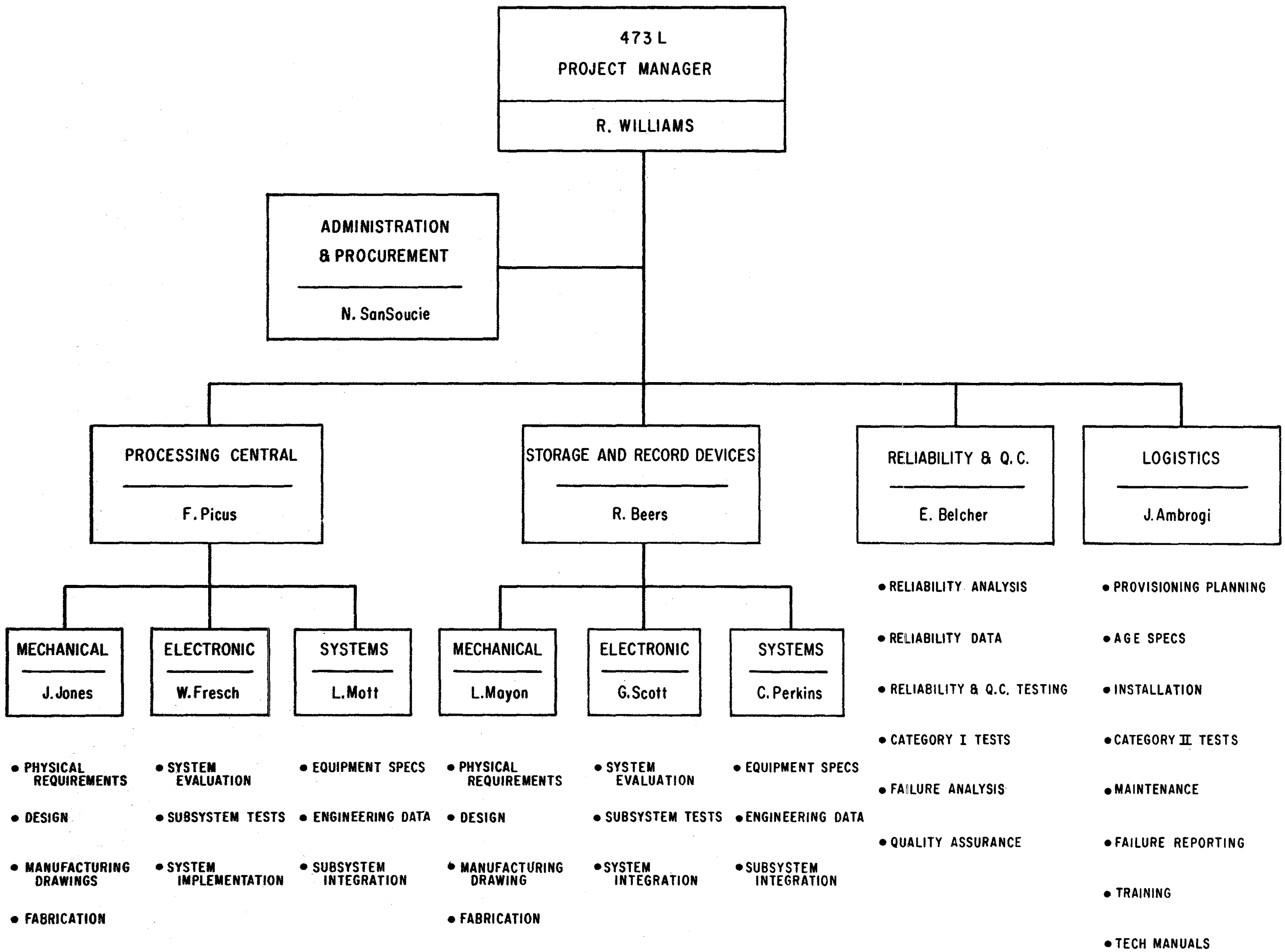


Figure 14. System 473L Data Processing Equipment Project Organization

STRUCTURE

The 473L Project will be organized as shown in Figure 14. Engineering will be performed by an autonomous team organized specifically for 473L.

Project business administration and supporting services will be absorbed within the existing organizational framework of Burroughs Laboratories through the coordination of a project administrator.

Fabrication will be accomplished by personnel selected from the force presently completing assembly of the D825 for NRL.

Logistic support will be provided by personnel from Burroughs' Military Field Service Division.

PROJECT PERSONNEL

Personnel selected for the 473L team have extensive experience on data processing systems. The key engineering personnel will be Mr. Williams, Mr. Fred Picus, Mr. Richard Beers, Mr. Edward Belcher, and Mr. Joseph Ambrogi.

Mr. Williams, in addition to directing the D825 project, previously directed design and development of the Polaris Stabilization Data Computer, D202 and NADAC airborne digital computers. He was a key member of the planning staff credited with developing the initial scheme for the NADAC computer. Earlier, as a project engineer, he was responsible for development of the peripheral equipment for a large-scale commercial digital data processing system, including logical, circuit, and packaging design. Mr. Williams is a registered Professional Engineer in the Commonwealth of Pennsylvania. He has approximately 18 years of experience in electronics engineering.

Mr. Picus, who will head the 473L DPS engineering group, was project engineer on the Polaris SDC prototype, Atlas and Regulus prelaunch data computer programs prior to heading the D825 development engineering group. He has approximately 11 years of experience in electronics engineering.

Mr. Beers, who will head the 473L peripheral equipment engineering group presently is acting in the same capacity for the D825 Project. He formerly was in charge of input-output design and development for an airborne computer application. He has had estensive experience in the design of systems and circuits involving high-speed analog-to-digital and digital-to-analog conversion of inputs and outputs to digital airborne and prelaunch computers. He has approximately 12 years of experience in electronics engineering.

Mr. Edward Belcher, who will head the reliability and quality control group, is presently supervising the reliability and quality control program for the ALRI Maintenance Ground Equipment, which is in the final stages of fabrication. He was previously responsible for design evaluation of the Atlas Guidance Computer System and was instrumental in formulating criteria for standard reliability and environmental tests performed on electronic equipments developed at Burroughs Laboratories. He has eight years of reliability engineering experience.

Logistic support personnel selected for the 473L team have acquired many years of experience on installation, testing, and maintenance of data processing systems at SAGE, Atlas, and ALRI operational bases. Administrative and other supporting personnel, likewise, have solid backgrounds on military contracts.

The logistic support program for installation, testing, and maintenance of the IOC sybsystem will be headed by Mr. Joseph Ambrogi, who has been engaged in developing, staffing, and direction of logistic support operations at all depots and sites in the SAGE system. He has eight years of electronic engineering experience, of which six have been in the area of logistic support.

INTEGRATION OF EFFORTS

Implementation and control of military projects at Burroughs Laboratories have attained a high level of efficiency. Procedures governing project operations have evolved through experience on numerous and varied military contracts during the past seven years. The effectiveness of Burroughs' system for integration of efforts has been demonstrated repeatedly by the Corporation's highly successful performance on such prominent programs as SAGE (AN/FST-2 Data Processor), Atlas (AN/GSQ-33 Guidance Computer System), and Polaris (Stabilization Dat Computer).

Further program planning, reporting, and management control capability is reflected in Burroughs' experience in the use of "Program Evaluation Research Task" (PERT). Burroughs is presently employing PERT on the 425L Program and has been using the device since March 1961 in connection with its responsibilities on the Mauler Program in collaboration with General Dynamics.

On 473L the entire project will be administered within the existing overall organizational structure of Burroughs Laboratories, and no problems of divisional integration are anticipated.

PURCHASING AND SUBCONTRACTING

The responsibility for initiating and following up purchase orders in connection with 473L components and shelf items will be delegated to the project administrator. He will coordinate his activities and operate within the existing integrated procurement organization at Burroughs Laboratories. In this position the administrator can participate from the start in planning involving make-or-buy decisions, value analyses, and selection of subcontractors or vendors.

The 473L Project administrator will be Mr. Norman San Soucie. He is presently responsible for administration of the D825 project. His previous administrative assignments include the Polaris SDC, PADRE, and NADAC computer development projects. He has six years of experience in administrative engineering on military contracts.

Policies and Procedures

Upon completion of equipment specifications, work statements are prepared and a make-or-buy analysis performed. On Make items, a division of Burroughs is selected. On buy items, RFQ's are issued to qualified bidders for new equipments, and awards are made on the basis of their proposals. In the case of standard components and off-the-shelf items, vendors are selected on the basis of quality, price, and delivery.

Corporate policy requires special consideration of small business and depressed area concerns, and awards are made to such concerns whenever possible, consistent with program objectives.

Ground rules for the administration of subcontracts are defined in Burroughs' Corporate Purchasing Manual. Policies and procedures are stated to account for such areas as: subcontractor selections, subcontractor relations, legal aspects, authorization to purchase, corporate coordinated purchases, contract implementation, technical assistance to subcontractors, defense security requirements, and audit requirements. These policies and Burroughs' procurement procedures have been reviewed and approved by USAF procurement survey teams.

LABOR RELATIONS

Throughout its 75-year history, the Burroughs Corporation has enjoyed peaceful labor relations. Not one instance of work stoppage has ever been recorded.

PRODUCTION

PLANNING

The 423L Data Processing Equipment will be fabricated at Burroughs' Great Valley Laboratory. Only two equipments will be required which do not already exist in the D825 data processing system -- the line printer and the disc file. These items are available and will be purchased.

Definitive specifications for the fabrication of each equipment will be submitted to the SPD for review and approval. These specifications will include requirements for special production processes, component qualification, quality control, reliability testing, and electromagnetic interference. Equipment acceptance tests as well as subsystem verification tests will be performed at GVL prior to delivery.

The quality and success of Burroughs' production planning is indicated by its recorded ability to meet schedules. Another indication is Burroughs' outstanding record of product quality. The Atlas Guidance Computer System, for example, has logged more than 50,000 hours of operation, establishing a mean-time-between-failure record 450 percent in excess of contractual requirements. SAGE AN/FST-2 Radar Data Processors have been operating continuously, 24 hours a day for several years, in numerous installations throughout the world at an average down time of less than 1 1/2 percent.

PRODUCTION EXPERIENCE

Burroughs has been developing and manufacturing electronic systems and equipments for 25 years. Data processing systems produced or in development by Burroughs which reflect experience similar to that required for the 473L project include:

- System 425L
- NRL D825 Modular Processor System
- Mauler Track Evaluation Computer
- Mauler Target Data Processor
- FAA Beacon Video Processor
- Polaris Stabilization Data Computer
- Atlas Guidance Computer System
- SAGE AN/FST-2 Radar Data Processor

- ALRI Airborne Radar Data Processor
- NADAC Naval Digital Airborne Computer
- CORDAT Coordinate Data Set
- MADDAM Macro-Module Digital Differential Analyzer
- B5000 Information Processing System
- B301 Sorter-Lister-Converter System
- E101 Desk-Size Computer
- MATABE Strategy and Tactics Analyzer
- D202 Airborne Bombing and Navigation Computer
- ALRI Maintenance Ground Equipment
- B220 Electronic Computer
- B205 Electronic Computer
- B251 Visible Record Computer
- F604M Proof and Distribution System

SCHEDULE RECORD

On all military programs, Burroughs has consistently met its major milestone commitments within contracted costs and schedules. On Polaris, for example, Burroughs delivered the prototype SDC in eight and one-half months, two weeks ahead of a schedule recognized as being extremely stringent to begin with, and the ALRI Radar Data Processor was developed and accepted by the USAF 45 days ahead of a 7 1/2-month schedule commitment.

PROJECT REPORTS

Throughout the duration of the 473L Project, Burroughs will submit the reports specified in Exhibit "A" in accordance with stipulated schedules, as shown in Figure 15. Technical notes will be prepared in accordance with RADC-3002 and submitted as required, and technical reports will be submitted to the SPD on the operation and maintenance functions of the Data Processing Equipment. Oral progress reports will be delivered by Burroughs at the Contracting Officer's request.

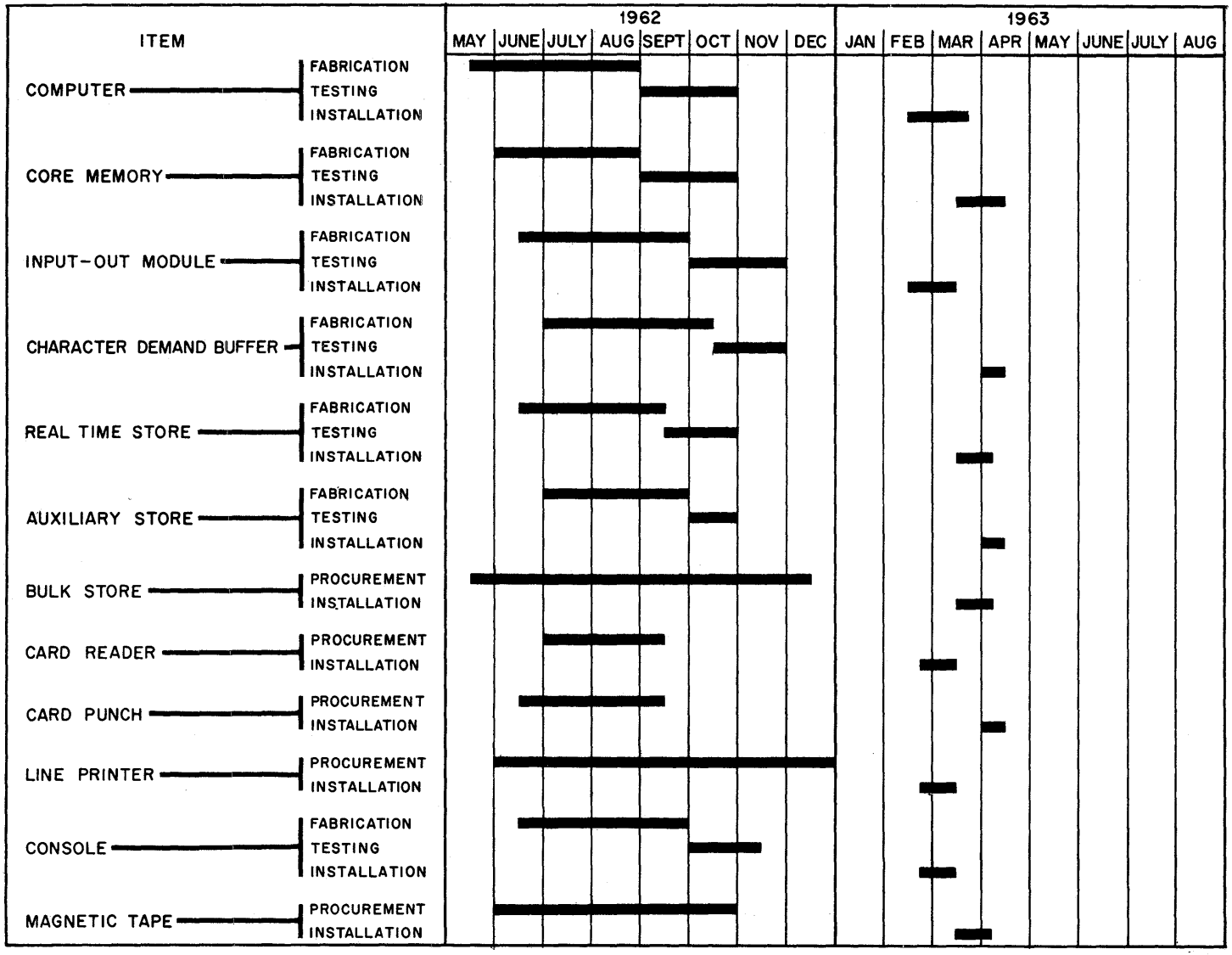


Figure 15. D825 System Schedule for System 473L
(Sheet 1 of 2)

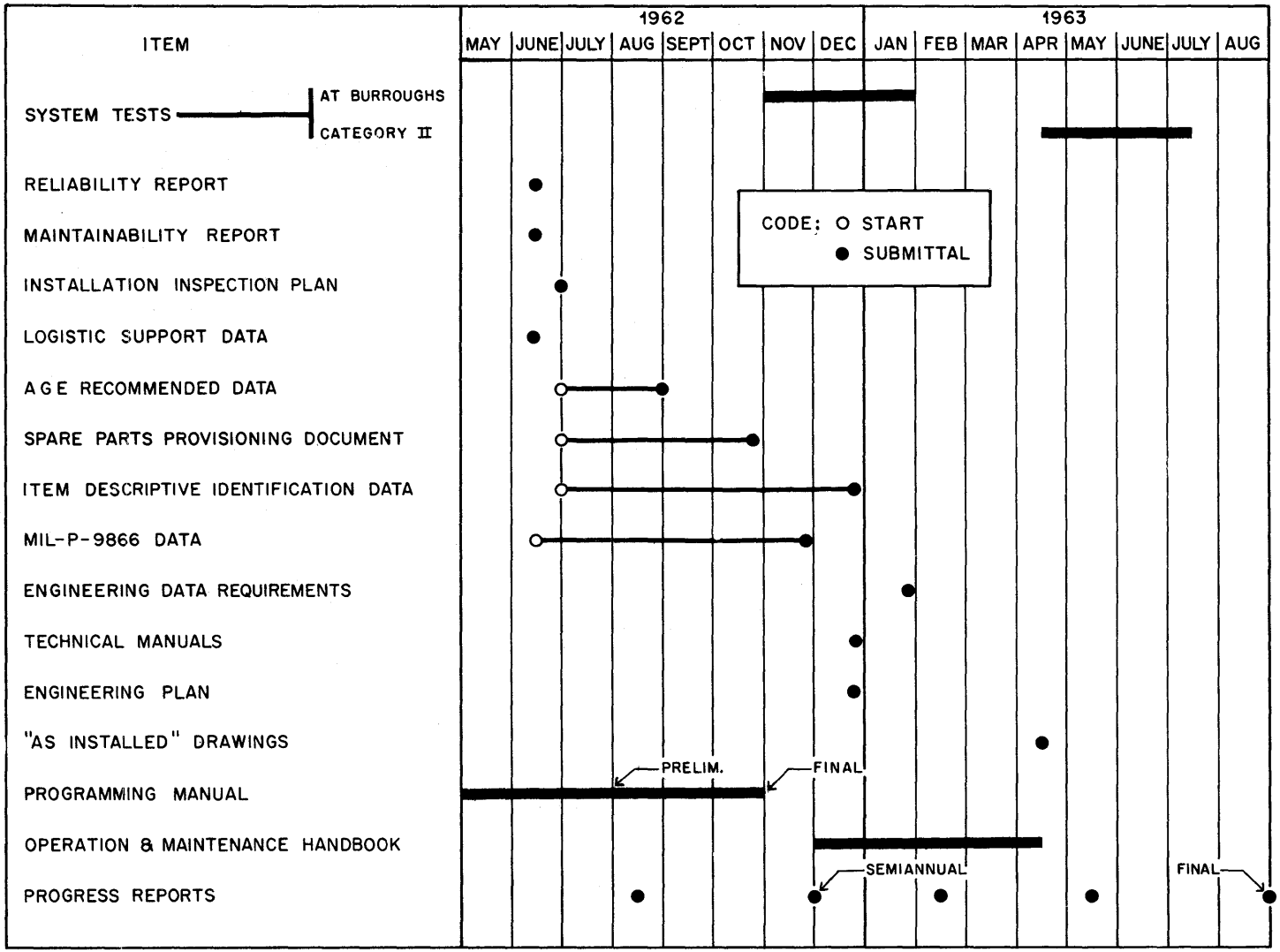


Figure 15. D825 System Schedule for System 473L
(Sheet 2 of 2)

RELIABILITY AND QUALITY CONTROL

Traditionally, assurance of high quality in the end product has been of paramount concern to Burroughs. To implement this concern, Burroughs enforces rigid quality assurance procedures. At Burroughs, the quality control function is combined with reliability efforts within an integrated Reliability and Quality Assurance Program. The effectiveness of this organization is evidenced by the fact that military electronic equipments developed by Burroughs have established unprecedented reliability records. The overall reliability factor of Atlas Ground Guidance Computers, for example, is 0.9985, and SAGE AN/FST-2 Radar Data Processors have compiled a reliability factor of 0.995 in continuous operation.

For the 473L DPS project, a senior reliability engineer will be assigned to plan, direct, and coordinate quality control efforts. He will be responsible for compliance with Specification MIL-R-26674.

Reliability data will be furnished in compliance with MIL-R-27542, and detailed progress reports of the reliability effort will be submitted as required by MIL-R-26474. Inspection records will be maintained and will be available for USAF examination. Workmanship certificates will be provided in accordance with MIL-W-27076.

TESTS

Preproduction tests will be performed at Great Valley Laboratory in accordance with the provisions of MIL-I-27113, and acceptance tests will ascertain compliance of the Data Processing Equipment with all specified performance requirements. The D825 system has been designed to operate in environmental conditions such as those to which System 425L will be subjected and to satisfy conditions similar to those specified in MIL-E-4970, MIL-I-26600, and MIL-R-26474. Test reports will be prepared in accordance with MIL-T-9107.

FACILITIES

Ample facilities for the 473L DPS are available at Burroughs Laboratories. An estimated 4,000 square feet of space will be required for engineering, 4,500 square feet for assembly and test, and 1,000 for administrative offices. Present and projected programs at Burroughs Laboratories will occupy 280,000 square feet of a total area of 315,000 square feet, leaving more than sufficient space for 473L. All of the essential laboratory, fabrication, assembly, and test equipment is available. No additional facilities or equipment will be required.

MAKE-OR-BUY INTENTIONS

Burroughs' make-or-buy intentions, based on a preliminary analysis of 473L DPS requirements, are reflected below.

EQUIPMENT	TYPE	MAKE	TYPE
Computer Module	D825	X	
Memory Module	D825	X	
I/O Control Module	D825	X	
Character Demand Buffer	D825	X	
Real Time Store	D825	X	
Auxiliary Store Device (Drum)	D825	X	
Bulk Store Device (Disc)	Telex 1A		X
Card Reader	Bur B122	X	
Card Punch	Bur B303	X	
Line Printer	Analex 300		X
Operator's Console	D825	X	
Magnetic Tape	BC422	X	
Data Synchronizer	D825	X	

LOGISTICS

PLANNING FOR LOGISTIC SUPPORT

An integrated logistics program is proposed for installation, testing, and maintenance of the 473L Data Processing Subsystem. This program will be carried out by Burroughs' Military Field Service Division. The major program tasks during the IOC phase are:

- Pre-installation inspection of facilities.
- Preparation and Implementation of Installation-Engineering Plan.
- Preparation and Implementation of Installation-Inspection Plan.
- Maintenance during installation and 3-month Category II testing period.
- Supply of repair parts during installation and 3-month Category II testing period, and compliance with MCP 71-673 requirements.
- Quality control of installation and maintenance.
- Training in accordance with Item 6, Operational Performance Characteristics, Criteria Format Supplement.
- Preparation of technical manuals required by MCMSP 1-9.

The Installation-Engineering Plan will contain the engineering data necessary for placing of equipment, interconnection of data processor and associated equipment, turn-on, alignment, and adjustment procedures, and subsystem performance tests. The Installation-Inspection Plan will specify the tests required to verify compliance of the installation with the I-E Plan.

Burroughs will provide office space for its personnel in the vicinity of the 473L Operation Center as well as all essential tools and equipment required during the installation and test phases.

PLANS FOR COC PHASE

Installation-Engineering plans for the COC phase will be essentially the same in concept as for the IOC phase. Performance tests will be made of the additional equipments incorporated in the COC Data Processing Subsystem.

QUALITY CONTROL

Burroughs' Military Field Service Division will employ a quality control program in accordance with Specification MIL-Q-9858. This program will provide objective inspection records covering installation, maintenance, and testing and will include the following:

- Receiving inspection of functional and physical characteristics.
- In-process inspection.
- Final subsystem inspection and documentation, including complete Break of Inspection.
- Generation and evaluation of inspection/failure reports.
- Termination inspection and Government Property audit.

SUPPLY

Complete provisioning documentation will be provided in accordance with Specification MCP 71-673 in addition to data specified in MIL-D-9412C. MFSD will establish a supply and maintenance level compatible with 473L needs.

Provisioning

Upon receipt of the Statement of Provisioning and the Programming Check List, provisioning action will commence in compliance with the following specifications:

- MIL-D-9412C -- Applicable data will be submitted to permit early planning for 473L AGE.
- MCP 71-650 -- Selection and supply of ground support equipment and spare parts will conform to the provisions of this document. Every effort will be made to use standard AGE, which can be obtained from USAF supply.
- MCP 71-666 and 669 -- These procedures will be followed if required.
- MCP 71-673 -- Automatic data processing and print-out techniques will be used for preparation of the production list, bulk items list, priced spare parts lists, and other supporting documents so that complete and timely information will be available for USAF review.
- MIL-I-27615 -- Early in the program, descriptive and stock numbering information will be submitted for items other than those in USAF inventories. Fed-Std 5 will be utilized in preparing item descriptions.

MAINTENANCE

Maintenance and parts replacement will be delegated to a maintenance and supply area. Replacement parts will be stocked for repairable items and rotable spares. In addition to all maintenance, this area will be responsible for central stock control, maintenance plans, stock control reports, failure data, and updating of spare parts lists. During the installation and test phases, stand-by spares will be stored for high-turn-around black boxes at the Burroughs facility in Washington, D.C. Depot Maintenance repair can be performed at the Burroughs Depot in Philadelphia, if desired. This facility conforms to USAF regulations for a supply and support system.

Burroughs will be accountable for any government furnished equipment. Inventory of GFE items by Burroughs will include a visual inspection with the participation of a government inspector.

Maintainability will meet the requirements of MIL-M-26512. Certification tests, evaluation, repairs, and calibration will be performed in accordance with AF Regulations 80-14 and 74-2.

TRAINING

Burroughs' Technical Training Department will conduct courses for USAF personnel on operation, programming, and maintenance of the Data Processing Subsystem during the IOC phase. Assistance will be provided, in cooperation with the 473L SPD, in development of the training concept, utilizing such analytical data as the Personnel Equipment Data and QQPRI. Training plans will be consistent with program milestones. Drafts of training plans, standards, and course outlines will be submitted for USAF review well in advance of the start of training. Air Force Skill Levels will be so arranged that USAF personnel can participate in Category II testing.

Burroughs assumes that training will be conducted in the vicinity of the 473L Operational Center. However, training facilities are available at MFSD, should the USAF desire that any part of the training be conducted there. The Training Department includes 17 classrooms, 5 laboratories, an audio-visual aid room, and two computer rooms.

TECHNICAL MANUALS

Technical manuals will be prepared as required by MCMSP 1-9. Manuals will be available prior to the start of training. Burroughs' Technical Publications Department is a completely integrated service which combines the experienced personnel and physical facilities capable of performing the complete publishing cycle -- from research, writing, and illustrating through to printing and binding.

ACCOUNTING PROCEDURES

ABILITY TO NEGOTIATE FIXED-PRICE CONTRACTS

Burroughs' financial status is such that it can readily assume the financial burden and responsibilities attendant upon a fixed-price government contract of the magnitude of 473L. This is substantiated by the ALRI contract (AF 33(600) 40540), a fixed-price, incentive-type contract valued at $69,012,000 and now in its third year.

FINANCIAL REPORTS

Burroughs will submit quarterly reports (Form DD 1097), based on its own internally generated reports of fund expenditures and commitments, to the 473L Contracting Officer, as shown in Figure 15.

MILESTONE CONTROL PROVISIONS

Burroughs has developed an internal control system which has proved to be highly successful on military programs, particularly as regards the effective handling of start, stop, change, or accelerate program orders. The basic philosophy of this system is that of dividing the total program into definable tasks and gathering project performance information to compare against budgets and schedules. Typical program control forms utilized in this system include:

- Program Interdivision Request for Quotation
- Program Estimated Manpower, Material, and Services
- Program Project Schedules
- Program Expenditure Authorization
- Financial Management Report (DD Form 1097)
- Program Financial Status Report
- Internal Control Flow Diagram
- Program Request for Quotation
- Program Summary of Estimated Costs
- Program Contract Release Notice
- Program Project Forecast Summary
- Program Project Performance Report
- Program Engineering Projects Progress Report
- Contract Accountability Report

These controls are processed in the following manner. Each corporate activity participating in a program responds to a definitive statement of work by submitting schedules and cost estimates. Program budgets are then formulated which establish the predicted expenditure rate per month by operating unit, task, and cost element (classification or type of direct labor, burden, material cost, travel and subsistence, and other direct charges). In parallel, a master schedule is prepared which incorporates the various major program phases -- design, development, fabrication, and test -- leading to the deliverable item.

Project Orders are issued to the various participating departments to implement action on specific technical tasks. PO's stipulate man-hour allotments and a detailed schedule for task completion. Close administrative surveillance of progress on technical tasks is maintained week by week, employing an accounting system which utilizes electronic accounting machines. Progress on each task is projected into the overall technical and cost picture.

This system of control enables timely and accurate reporting and presents a complete and continuous profile of the project's status.

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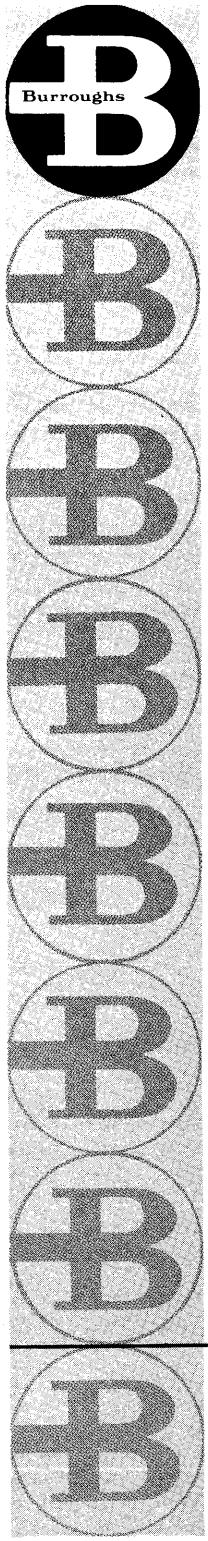

ERRATA TO
TECHNICAL PROPOSAL

SYSTEM 473L
DATA PROCESSING EQUIPMENT

SUBMITTED TO
UNITED STATES AIR FORCE
HEADQUARTERS, ELECTRONIC SYSTEMS DIVISION
AIRFORCE SYSTEMS COMMAND
LAURENCE G. HANSCOM FIELD
BEDFORD, MASSACHUSETTS

Burroughs Corporation

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ERRATA
SUPPLEMENTARY INFORMATION
TECHNICAL PROPOSAL
SYSTEM 473L
DATA PROCESSING EQUIPMENT

OPERATOR, PROGRAMMER AND MAINTENANCE TRAINING

The Technical Training Department, located at Burroughs Military Field Service Division, will conduct courses of training on the Data Processing Subsystem Equipment during the Interim Operational Capability Phase. Separate courses will be prepared and conducted for USAF personnel concerned with the operation, programming, and maintenance of the Data Processing Subsystem.

Course Length and Complexity

Operator: Will be trained to operate and check out equipments listed in the Data Processing Subsystem IOC configuration. Will become proficient in Start, Stop and operating procedures. Will be taught necessary preventive maintenance routines. The operator training course would be two months in length, of which six weeks will be on actual equipment.

Programmer: Will be taught the function of all programs basic to the Data Processing Subsystem; will understand their relationship to efficient operation and maintenance of the subsystem. A two-month course for programmers is indicated. When the complete system object program is written, an additional one month of training would be required to round out the programmer training.

Maintenance Technician: Will be taught in detail: the operation, preventive and corrective maintenance routines associated with the Data Processing Subsystem. This will include all equipments listed in the IOC configuration. The course of training would be four months.

Plan of Operation

Working in close cooperation with SPO, Systems Project Office, and drawing upon such analytical data as the Personnel Equipment Data and the Qualitative, Quantitative Personnel Requirement Information (QQPRI), the Technical Training Department will assist in development of the Training Concept. Assistance will also be given in expanding the Training Concept into Training Plans. These plans will be submitted in accordance with the established milestone charts.

Drafts of the training plans, standards and course outlines will be submitted for approval well in advance of the scheduled start of training. Training scheduling will be accomplished so that USAF personnel can participate in Category II Testing.

Availability of Air Force Skills

Course content and training standards will be written to make use of existing Air Force Skill levels. AFSC's that are particularly applicable are 30571, Electronic Digital Data Processing Maintenance Technicians; 68570, Data Processing Machine Supervisor; 68550 Data Processing Machine Operator; 68770, Programming Technicians.

In-House Training Capabilities

Military Field Service Division, Technical Training Department has a complete capability for providing training services. The Training Department occupies 40,000 square feet of floor space in a modern facility. This area includes 17 classrooms, 5 laboratories, an audio-visual aid room, a dynamic training aid room, two computer rooms, and office space for the staff.

The instructors have previous teaching experience in military schools, technical institutes, public schools, and various institutes of higher learning . Staff members are attending colleges and graduate schools to further enhance their education.

In addition to its core of experienced instructors, the Technical Training Department includes professional level psychologists. They participate in preparing studies and quotations

for new programs. As the programs develop, they give professional assistance in such studies as the QQPRI, Task Equipment Analysis, and Training Equipment Planning.

Over the past five years the Technical Training Department has been actively engaged in programs involving personnel research including selection and training, tests and measurements, system analysis, and training evaluation for several Data Processing Systems, such as those for SAGE and Atlas. Training on these systems has taken place at both MFSD Headquarters and at government facilities.

Burroughs Corporation

Detroit 32, Michigan

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