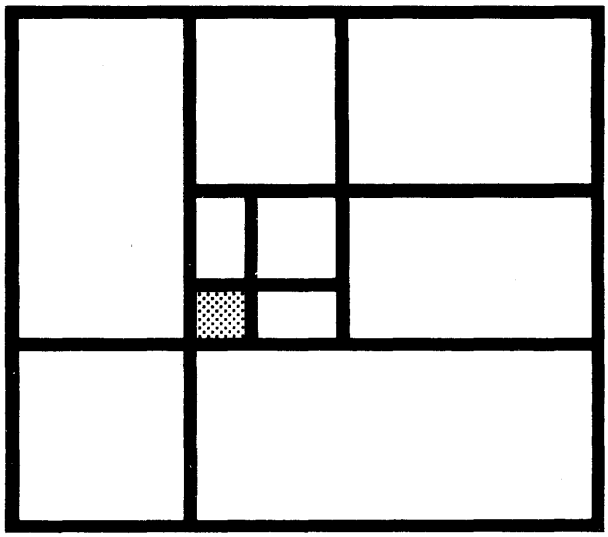
PCSI- 650

PROCESS COMPUTER

GEPAC® 4010



GENERAL ELECTRIC

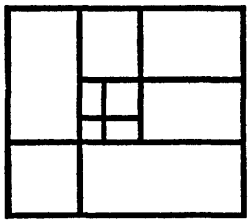
UTILITY AND PROCESS AUTOMATION
PRODUCTS DEPARTMENT
PHOENIX, ARIZONA

GE-NPGCD CAROLINA I (AZNA) REQN: 282-L3285

The GE PAC® 4010 Process Computer System

VOLUME II

PROCESS I/O



This instruction book is provided as a basic source of technical information on this system. If problems arise in installation, operation, or maintenance that are not covered in these instructions, the matter should be referred to General Electric Company, Process Computer Products Department, Phoenix, Arizona, U.S.A. Attn: Technical Publications.

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GENERAL ELECTRIC

1400A/B PROCESS DIGITAL I/O SUBSYSTEM

TABLE OF CONTENTS

INTRODUCTION

The Process Digital Input/Output Subsystem provides a means of monitoring and controlling process functions and operator consoles. The input function reads the status of logic variables (yes/no, true/false, set/reset, open/closed, on/off) from various process system devices such as switches, valves, relays, and motors. The output function provides program controlled contact closures, and optional analog signals and stepping motor pulses for controlling the process.

The Process Digital I/O Subsystem described in this publication may be used in a GE-PAC[1] 4010 and future Process Computer Systems. Fig. INT. 1 illustrates the basic signal flow and functional modules associated with the digital inputs/outputs in a GE-PAC 4010 System. The signal flow in future systems will be similar and illustrated in the System Logic drawing supplied with the system. The location of the functional modules within the GE-PAC 4010 Central Systems Unit is shown in Fig. INT. 2. The location of these modules in the Auxiliary Systems Unit (ASU) is shown on the System Configuration diagram supplied with each system.

Input/output connections with the process and operator consoles are made through termination cabinets. The termination cabinets contain termination points, signal conditioning, and selection gates for digital inputs, and termination points and output relays for digital outputs. Digital inputs may be either 28 volts or 125 volts and may optionally be connected to change detector circuits. Digital outputs may be latched, momentary, decimal display, or applied through analog generators. For each Process Digital Controller, up to sixty-four groups, each having 24 contacts per group of digital inputs, may be connected to the system. For each Process Digital Controller, up to sixty-four groups, each having 16 contacts per group of digital outputs, may be connected to the system.

Program control of the digital input/output subsystem is via the execution of GEN 2 commands or TIM/TOM. Each OUT command (26.5 μsec) controls the status of one digital output group of 16 contacts as specified by a data/control word in the A Register. Upon satisfactory (no fault) completion of each output operation, an automatic program interrupt is generated. Each IN command (26.5 μsec) places the status ("1" for closed, "0" for open) of 24 contacts in the A Register corresponding to the input group specified by the K1, 0 bits of the command.

To protect the process and the subsystem hardware, the digital I/O subsystem contains error checking circuits which monitor the digital output portion of the hardware. Detection of an error disables output relay operation and delays the ready interrupt until the error condition has been cleared.

The digital I/O subsystem contains extensive test and maintenance hardware permitting off-line testing to isolate failures using a diagnostic program.

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MODEL NUMBER/OPTIONS

The following table lists the model numbers and options associated with the digital I/O subsystem. All model numbers listed may not be available on all process computer systems. Options contained in a particular system are shown on the System Configuration Diagram, Special System Logic drawing, etc. supplied with each system.

Process Digital Controller

4DP4846*

A(or B**)S01 - Special purpose option containing the S02, S03, and S04 options described below. That is, this option defines a system having 16 digital input groups, 16 digital output groups and the basic common hardware. Other options (adders) may of course be added to expand the system.

S02 - Basic hardware for digital inputs and outputs.

S03 - Adder for input groups 1 - 16 (Adds the control PWBs and cables for digital input groups 1 thru 16 to the basic hardware specified by the S02 option.)

S04 - Adder for output groups 1 - 16 (Adds the control PWBs and cables for digital output groups 1 thru 16 to the basic hardware specified by the S02 option.)

S05 - Adder for input groups 17 - 64 (Adds control PWBs and intra-cabinet cables to expand the digital inputs of a system containing an S01 or S04 option from 16 to 64 groups.)

S06 - Adder for output groups 17 -32 (Adds control PWBs and intra-cabinet cables to expand the digital outputs of a system containing an S01 or S04 option from 16 to 32 groups.)

S07 - Adder for output groups 33 - 64 (Adds control PWBs and intra-cabinet cables to expand the digital outputs of a system containing an S06 option from 32 to 64 groups.)

S08 - Pulse Source Initiator Adder - (Adds Pulse Source Initiator printed wiring board, SPIA5.)

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* Instead of 4846, the model number for future systems is 4430. The options are the same as those shown above except that intra-cabinet cables are not included with the 4430 model number.

** A is for PDC in CSU cabinet.
B is for PDC in ASU cabinet.

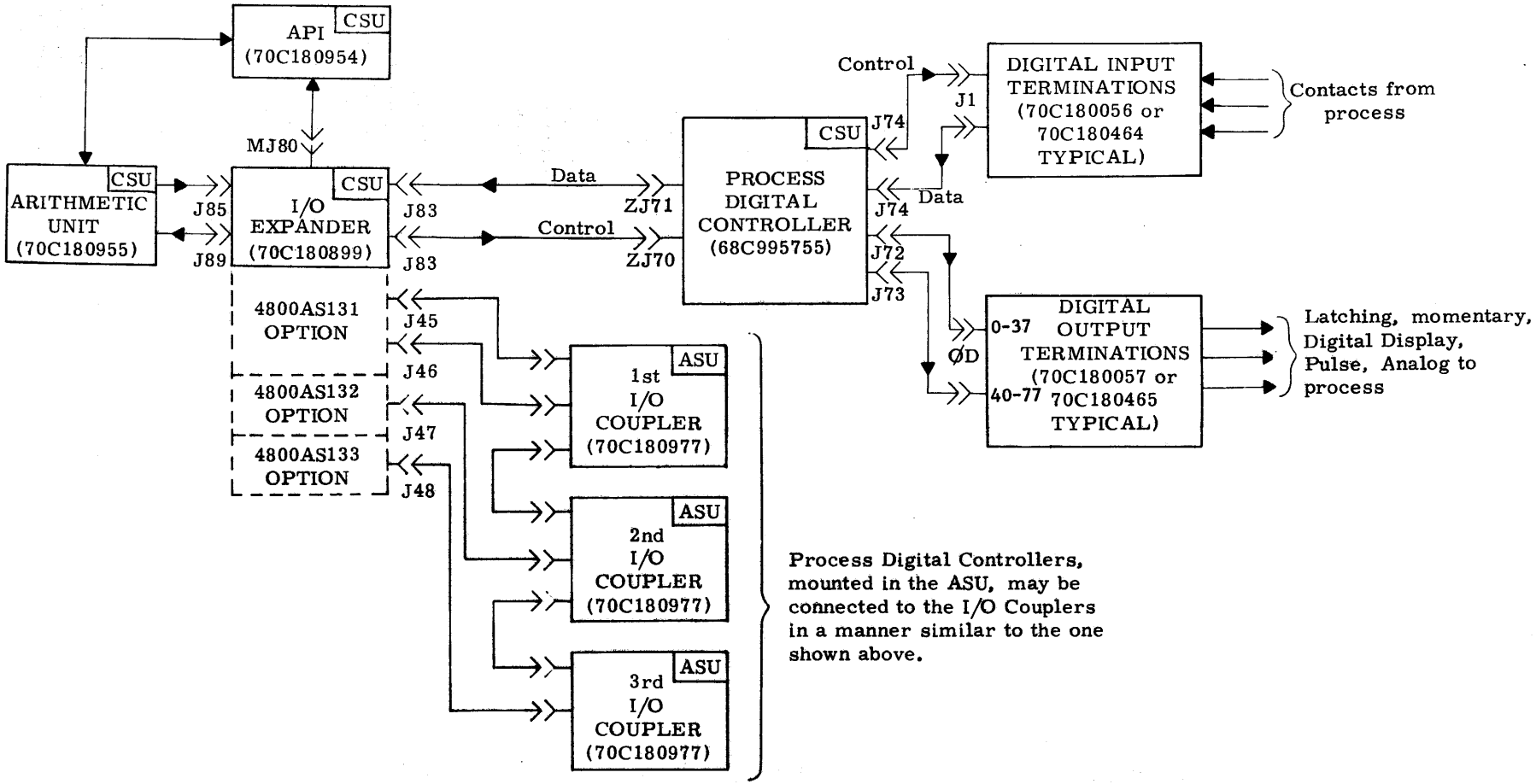


Fig. INT. 1 Digital Input/Output Block Diagram

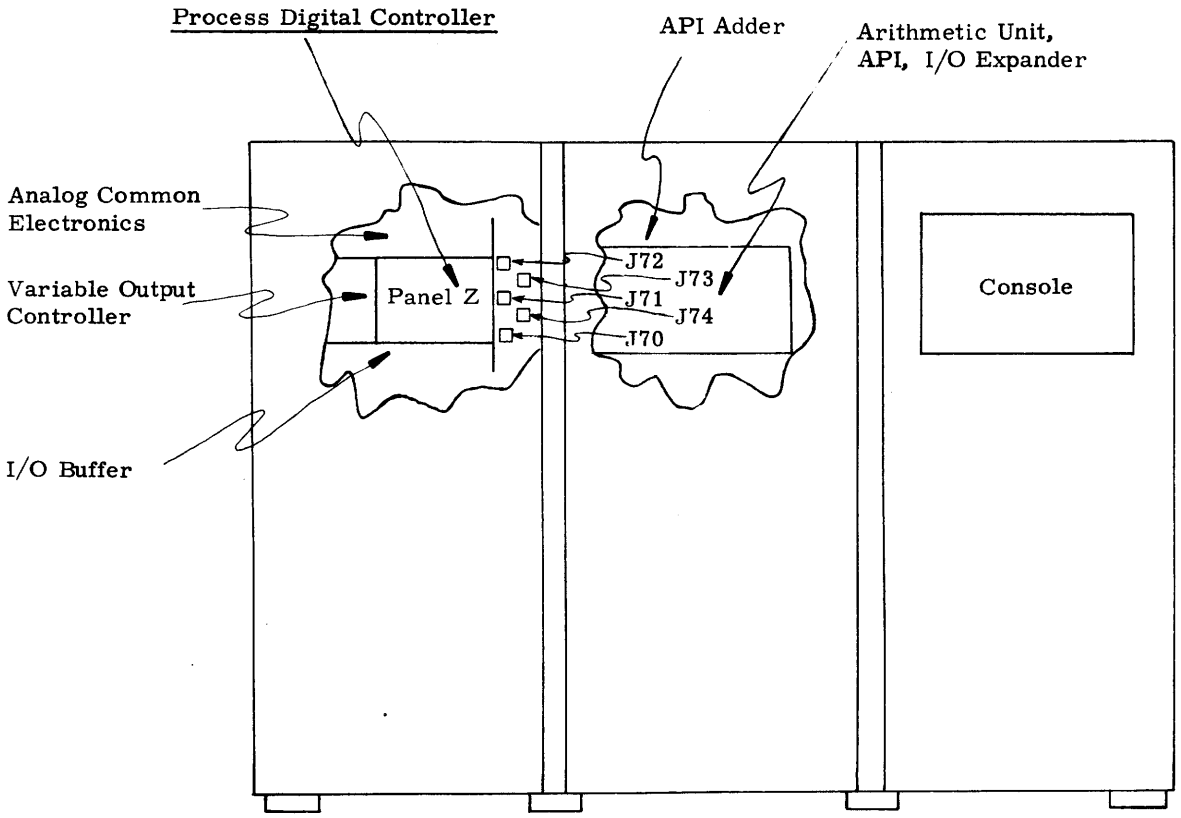


Fig. INT. 2 4010 Central Systems Unit

Digital I/O Cabinets (Typical):

4DP4847AS01 - Basic Digital Input Cabinet

02 - Digital Input Distributor (wiring harness)

03 - Digital Output Distributor (wiring harness)

04 - 28V (4290A) and 12V (See Theory 4847A-04) Dig. In. Power Supply

05 - 125V Dig. In. Power Supply (4491A)

06 - 28V Dig. (4290A) Out Power Supply

07 - 42V (4396A) Analog Gen. Power Supply

08 - Dig. In. 28V, 192 Pt. Term.

09 - Dig. In. 125V, 192 Pt. Term.

10 - Dig. Out 64 Pt. Termination

11 - Pulse Source Initiator Interposer Relay Assembly

Termination Boards (Typical):

Input

PX2000ICFA1 - 28V, 48 pt., 1 Msec, Filter

PX2000ICFB1 - 28V, 48 pt., 22 Msec, Filter

PX2000ICFC5 - 28V, 48 pt., Thumbwheel Sw. Read-in

PX2000ICFC2 - 125V, 48 pt., 15 usec, Filter

PX2000ICFB2 - 125V, 48 pt., 22 Msec, Filter

PX2000ICCA4 - 125V, 24 pt., Change Detection

PX2000ICCA2 - 28V, 24 pt., Change Detection

Output

PX2000IHBA1 - 100V Latching, 16 pt., 1.25A, 150VDC

PX2000IHBA2 - 100V Latching, 16 pt., 1A 120VRMS

PX2000IHBB1 - 5VA Latching, 16 pt., 1A, 50VDC

PX2000IHBC1 - 250VA Latching, 8 pt., 1A, 50VDC

PX2000IHBC2 - 250VA Latching, 8 pt., 2A, 120VRMS

PX2000IHBD1 - 20VA Latching, 8 pt., .2A. 100VDC

PX2000IHSA 1 - 100VA Momentary, 16 pt., 1.25A, 150VDC

PX2000IHSA 2 - 100VA Momentary, 16 pt., 1A, 120VRMS

PX2000IHSB 1 - 5VA Momentary, 16 pt., .1A, 50VDC

PX2000IHSC 1 - 250VA Momentary, 8 pt., 1A, 200VRMS

PX2000IHSO 2 - 250VA Momentary, 8 pt., 2A, 120VRMS

PX2000IHSD1 - 20VA Momentary, 8 pt., .2A, 120VRMS

PX2000IDDB1 - Dig. Display Drive (4 Digit, Series 10)

PX2000IDDA1 - Dig. Display Drive (4 Digit, Series 120/220)

PX2000IDAA1 - 8 Bit Analog Generator (2 per PWB)

PX2000IDAB1 - 8 Bit Analog Generator (Biased 20% offset))

Jumper Pin

The following options are implemented by changing, adding, or removing printed wiring board jumper pins in the Process Digital Controller.

K3, K2 Process Digital Controller Address: The K3, K2 address is determined by the position of jumper pins on the SIOA5 board in A03-FK as shown on sheet 4 of the PDC logic, 68C995755.

Output Relay Energizing Time: The normal output delay time ($A_7 = 0$) is 3 Msec. if a jumper pin on the ISSB5 board in A03-FK is in the top black jack or is 8 Msec. if a jumper pin is in the bottom black jack. The long delay ($A_7 = 1$) is 8 - 40 Msec. (trimpot adjustable) if a jumper pin is in the top green jack or is 40 to 200 Msec. (trimpot adjustable) if a jumper pin is in the bottom green jack. Sheet 16 of the PDC logic, 68C995755, illustrates these connections.

The 3 (3.3 $\pm$ 10%) Msec. energizing time is normally used for 100VA latching relays; the 8 (9.0 $\pm$ 10%) Msec. time is normally used for 250VA latching relays or short momentary 100VA relays. The long operate time is normally used for momentary relays.

Pulse Source Initiator Operation: Sheet 34 of the PDC logic illustrates these jumper pin connections which are located on the SPIA5 board in A12-AE.

a. Input Frequency: A jumper pin in the top red jack selects the input signal from the Arithmetic Unit or in the bottom red jack selects an external signal. Further jumper pin selection of the Arithmetic Unit input is provided for either the line frequency input or the adjustable pulse generator (optional) input on the ILDC5 board in B29-FK as shown on sheet 96.2 of the 4022 logic, 70C180955.

b. Output Frequency: A jumper pin (SPIA5 board) in the top green jack selects the output frequency at one-half the input frequency or in the bottom green jack selects the output frequency equal to the input frequency of the PSI.

c. Deadman Timer: A jumper pin in a yellow jack selects the duration of the deadman timer at 1 (top), 2 (middle) or 3 (bottom) seconds.

   The deadman timer will abort the pulse source initiator if it is left enabled longer than the time interval selected by the jumper pin.

d. Output Signal Type: A jumper pin in the top black jack selects a pulse output signal equal to the output frequency selected or in the bottom black jack selects an output that is enabled for the duration that the PSI is enabled.

Optional Pulse Source Interposer: Sheet 14 of the Digital Outputs logic illustrates these jumper pin connections. These jumper pins determine R/C suppression and contact form. The positions of the jumper pins are specified by the Requisition Engineer.

REFERENCE DOCUMENTS

Logic

68C995755 - Process Digital Controller

70C180056 and 70C180464 - Digital Input Logic (Typical)

70C180057 and 70C180465 - Digital Output Logic (Typical)

Interface Module Logic

70C180955 - 4022D Arithmetic Unit

70C180899 - 4078B I/O Expander

70C180954 - 4032D Automatic Program Interrupt

70C180977 - ASU I/O Coupler

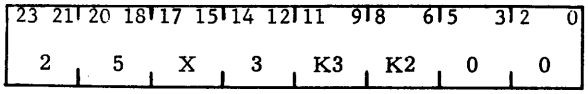
Maintenance

Computer Maintenance Manual

INSTRUCTIONS

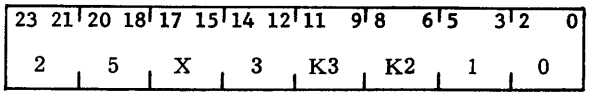
The following GEN 2 instructions, when addressed to the Process Digital Controller (PDC), affect the Process Digital I/O Subsystem as described in the following paragraphs. Fig. INS. 1 illustrates the format of the GEN 2 command and the basic Process Digital I/O control.

ABT - Abort PDC



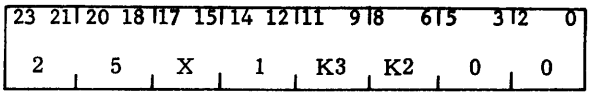
ABT with K1 = 0 initializes the entire PDC, terminating any operation in progress, and releasing the PDC for a subsequent operation. Pushing the ON/INIT switch on the Programming and Maintenance console when in the MANual mode and the console enabled has the same effect.

ABT - Abort Pulse Source Initiator



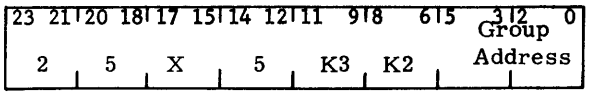
ABT with K1 = 1 deactivates the optional (AS08) Pulse Source Initiator if it is activated. This instruction has no other effect on the PDC and may be used to deactivate the Pulse Source Initiator without affecting any other operation in progress.

ACT - Activate



ACT generates a PDC ready interrupt by temporarily moving the ready line from "ready" to "not ready" and back to "ready". If the PDC is "not ready" (busy) when ACT is executed, the instruction has no effect.

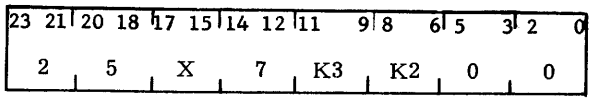
IN - Input



IN replaces the contents of the Arithmetic Unit A Register with the binary status (1 for closed, 0 for open) of the digital input group specified by the K1, 0 bits. Refer to the Digital Inputs section of this publication for further details.

If the PDC is in the Test Mode, the IN instruction replaces the contents of the A Register with the contents of the PDC Output Buffer Register. Refer to the Test Mode description contained later in this section.

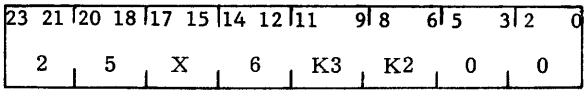
JNE - Jump No Error



JNE tests the PDC error line to determine if a fault occurred in a previous digital output or test operation. If an error exists, the error indication is cleared permitting further operations and program control is transferred to the first sequential (P+1) instruction. If no error indication exists, program control is transferred to the second (P+2) instruction.

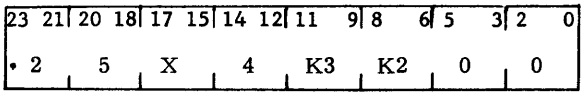
A detailed discussion of error detection is provided in the Output Fault Checking and Test Mode sections of this publication.

JNR - Jump Not Ready



JNR tests the busy or ready status of the PDC. If the PDC is ready, program control goes to the next sequential location (P+1). If the PDC is busy, program control goes to the second sequential location (P+2). The PDC is busy during an output operation and held busy if a fault (error) is detected.

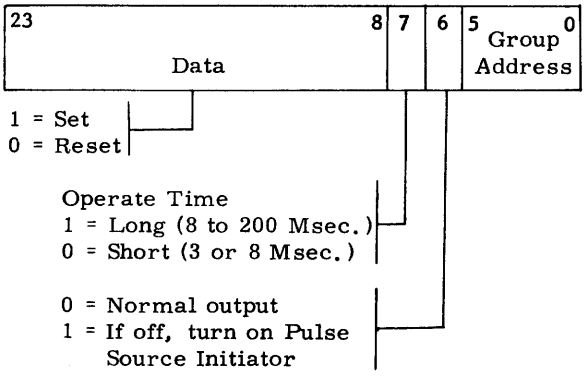
OUT - Output (Normal)



An OUT command executed when the PDC is in the normal mode (not test mode) and "ready", transfers the contents of the A Register to the PDC and initiates the output operation. The A Register must contain a Control/Data Word corresponding to the format shown below. Refer to the digital Output section for details.

An OUT command with K1 equal to 0 executed when the PDC is in the test mode (following a previous SEL 10 command) is ignored.

Control/Data Word (A-Register)



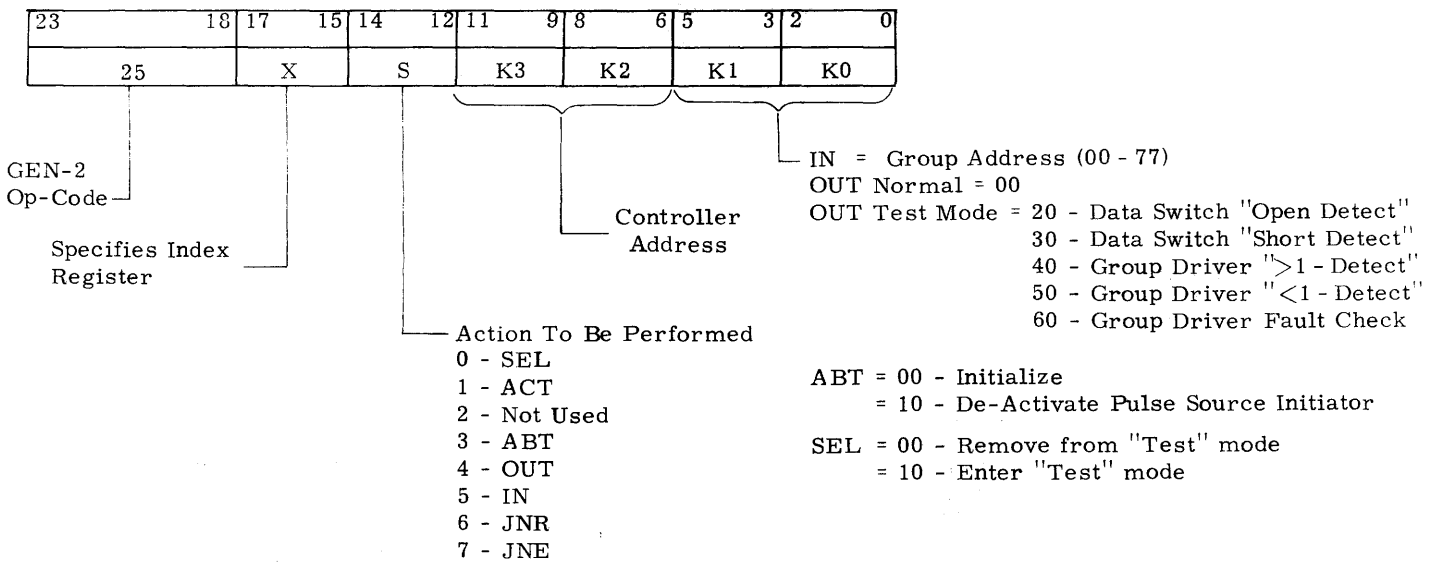
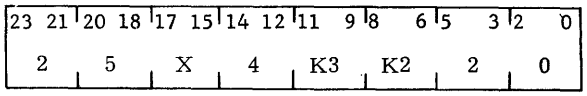


Fig. INS. 1 GEN2 Format

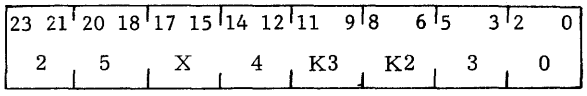
OUT - Data Switch Open Detector Check (Test Mode)



Executing this instruction in the Test Mode with one or more data bits in the A Register control/data word a "0" causes an output fault if the Data Switch Open detector is functioning properly and there are no shorted data switches. Executing this instruction in the Test Mode with all data bits in the control/data word "1" causes no output fault if there are no open data switches. To test all data switches in a system containing more than 37_8 groups, the command must be executed twice; once with bit 5 a "one" and once with bit 5 a "zero".

Refer to the Test Mode description contained later in this section for further details.

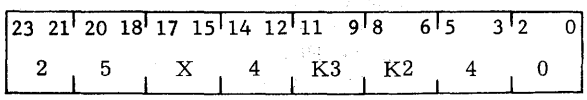
OUT - Data Switch Short Detector Check (Test Mode)



Executing this instruction in the Test Mode with one or more data bits in the A Register control/data word a "1" causes an output fault if the Data Switch Short detector is functioning properly and there are no open data switches. To check all data switches in a system with more than 37_8 groups, this command must be executed twice; once with bit 5 a "one" and once with bit 5 a "zero". Executing this instruction with all control/data word bits "zero" causes no output fault if there are no shorted data switches.

Refer to the Test Mode description contained later in this section for further details.

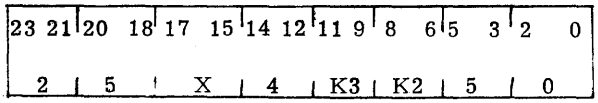
OUT - More Than One Group Driver On Detector Check (Test Mode)



Executing this instruction in the Test Mode generates an output fault if the More Than One Group Driver On Detector is functioning properly and there are no open group drivers. The data field is ignored during the execution of this command.

Refer to the Test Mode description contained later in this section for further details.

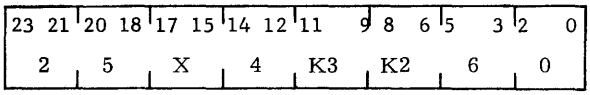
OUT - No Group Driver On Detector Check (Test Mode)



Executing this instruction in the test mode causes an output fault if the No Group Driver On Detector is functioning properly and there are no shorted group drivers.

Refer to the Test Mode description contained later in this section for further details.

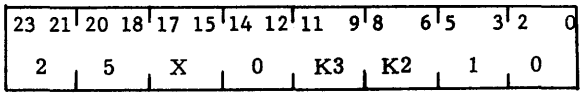
OUT - Group Driver Fault Check (Test Mode)



Executing this instruction in the test mode causes no output fault if there are no faulty group drivers. To check all group drivers it must be executed twice, one with bit 4 = 1 and once with bit 4 = 0. Executing an IN command addressed to the PDC following the execution of the OUT60 commands loads the A Register with the contents of the Output Buffer Register which should correspond to the contents of A when the OUT command was issued. If not, either the data path between the AU and the PDC is faulty, or the Output Buffer Register in the PDC is faulty.

Refer to the Test Mode description contained later in this section for further details.

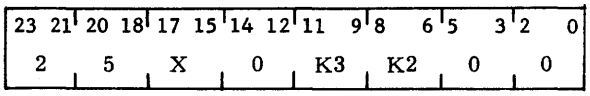
SEL - Select Test Mode



Executing SEL with K1 = 1 when the PDC is ready, places the PDC in the test mode. In the test mode, no output relays can be energized (unless a hardware fault exists).

Refer to the Test Mode description contained later in this section for further details.

SEL - Select Normal Mode



Executing the SEL command with K1 = 0 when the PDC is ready removes the PDC from the test mode.

Refer to the Test Mode description contained later in this section for further details.

DIGITAL INPUTS

The operation of the digital input portion of the subsystem is controlled by the execution of an IN command addressed to the Process Digital Controller (K3, K2) and to a digital input group (K1, K0). Executing the IN command when the PDC is not in the test mode replaces the contents of the A Register with the status of the 24 digital input signals connected to the addressed input group. Each A Register bit set corresponds to a closed digital input contact or a "true" input logic level.

Executing an IN command when the Process Digital Controller is in the test mode replaces the contents of the A Register with the status of the Process Digital Controller Output Buffer Register. The test mode of operation is described later in this section.

The digital input operation is completed during the execution (26.5 μsec.) of the IN command. Therefore, the digital input subsystem is always ready and does not require a ready test function (JNR). There is no hardware error checking associated with the input function. Many systems, however, provide validity checking using software and by connecting one input of each 24 input group to the digital input power supply. This is described in more detail in the Digital Input Terminations section that follows.

Fig. DIN. 1 contains a detailed block diagram of the digital input portion of the subsystem illustrating the basic data flow and selection logic. As illustrated, the logic levels or contacts from the process are connected to the termination cabinet. These digital input contacts are normally supplied from either a 28VDC or a 125VDC power supply in the termination cabinet. Therefore, when a digital input contact is closed, either 28VDC or 125VDC is connected to the input termination. From the termination, the signal is routed through a signal conditioning circuit and then to a group selection gate. This group selection gate is enabled only when the K1, K0 address portion of the IN command being executed corresponds to the input group of the signal. The K1, K0 bits of the IN command are decoded within the PDC providing the select signal to the group selection gate. From the group selection gate the signal is applied through an isolation amplifier (line driver) to the Process Digital Controller. The S=5 bits and K3, K2 address bits of the IN command, enable the signal through the I/O Expander to the Arithmetic Unit, A Register. Operation of the Arithmetic Unit is the same for all IN commands as described in the Arithmetic Unit Theory publication contained in this book set.

INPUT SELECTION

Fig. DIN. 2 illustrates the format of the GEN 2 IN command and the bits associated with enabling and selecting a digital input group. The S and K bits of the GEN 2 command are applied from the Arithmetic Unit, throuth the I/O Expander to the Process Digital Controller. The PDC decodes these bits, selects the input group and enables the digital input function.

The K3, K2 address of the PDC is optional and pin selected on the SIOA5 board in slot A03. The K3, K2 address selected by the jumper pins and the S bits are decoded on sheets 4 and 6 of the PDC logic (68C995755) to enable the Read In Digital Input Driver (D0ING1). The Read In Digital Input Driver enables decoding of the K1, K0 bits for group selection and gates the input data from the termination cabinet through the Line Receivers (M0DB00 - 23, sh. 10 and 11) to the I/O Expander for application to the Arithmetic Unit.

Selection of a digital input group occurs by enabling one minor select line and one major select line corresponding to the K1, K0 bits of the IN command. These minor and major select lines are applied to the termination cabinets where they are ANDed to select a particular group. The group address matrix decode scheme, using the minor and major select lines, is shown by the table on sheet 5 of the PDC logic. This table illustrates both the 4 x 4 matrix required for a 16 group input system (AS03 option) and the 8 x 8 matrix required for a 64 input group system (AS05 option). The mnemonics listed in the matrix scheme table correspond to the mnemonics assigned to the decode logic elements shown on logic sheets 6 thru 9.

Fig. DIN. 3 illustrates the group select matrix scheme in a slightly different form showing the general interconnections and selection within the termination cabinet. This figure also illustrates the bit configuration associated with the mnemonics of the various decode logic elements. The mnemonics are formed as shown in the following examples:

Major Selects: I24X = bit 4, and 2 are both "1"
- Value of K0=4 bit
- Value of K1=1 and K1-2 bits

Minor Selects: IX41 = bit 5 and bit 0 are both "1"
- Value of K0=1 and K0=2 bits
- Value of K1=4 bit

The major and minor select lines to the termination cabinet are open for true and 0V for false.

INPUT TERMINATIONS

The maximum input capacity of each Process Digital Controller provides for 64 groups of 24 contacts per group or 1536 contact inputs. As described in Model Number/Options section, control for no input groups, 16 input groups, or 64 input groups may be selected for a system.

All digital inputs are connected to a termination cabinet. Although the logic drawing number (70C170056) is subject to change, the general input termination cabinet configuration illustrated in Fig. DIN. 1 should apply. The digital input logic drawing for a particular system will be referenced on the Digital Termination Cabinet Index for the system.

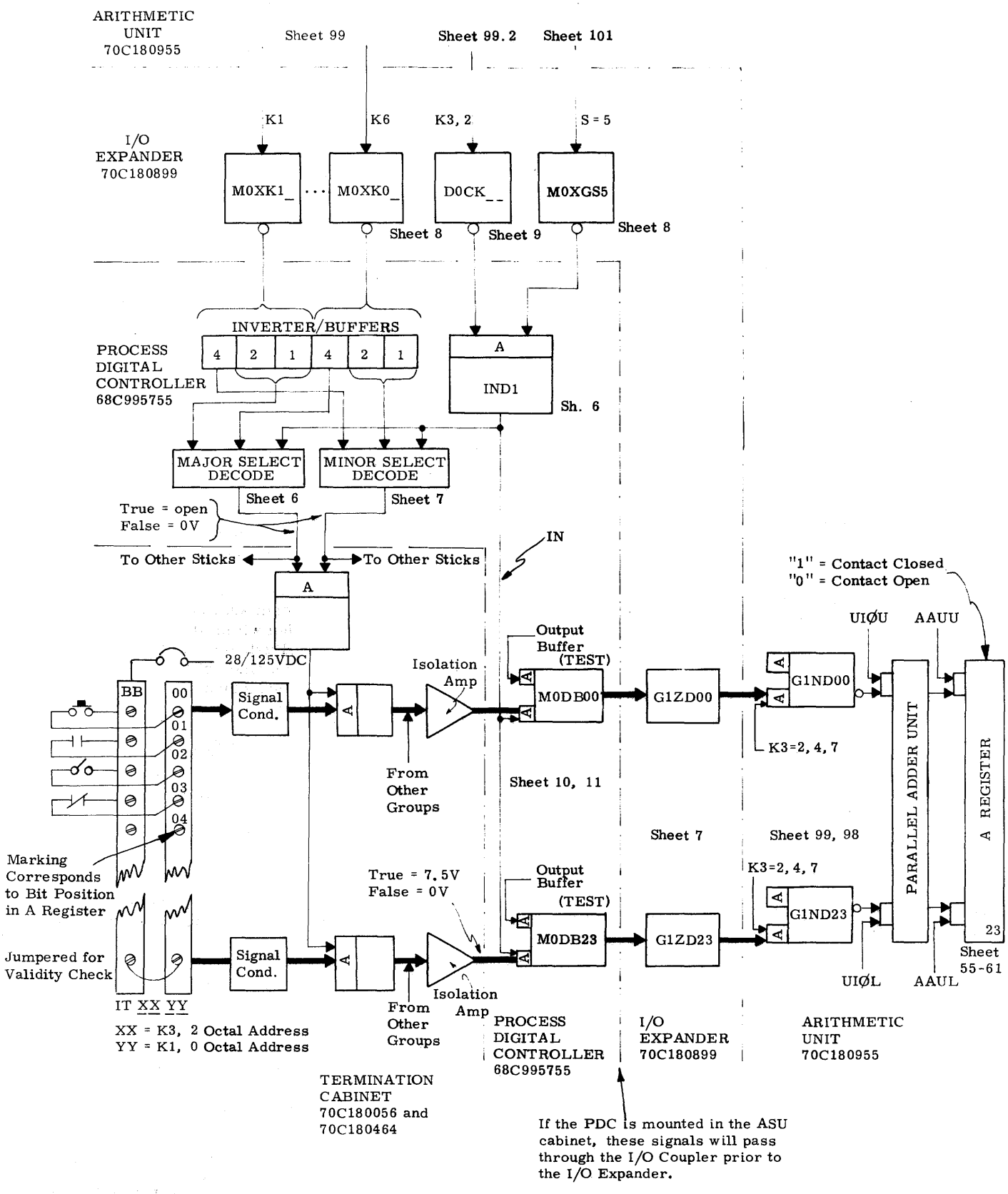


Fig. DIN. 1 Digital Inputs

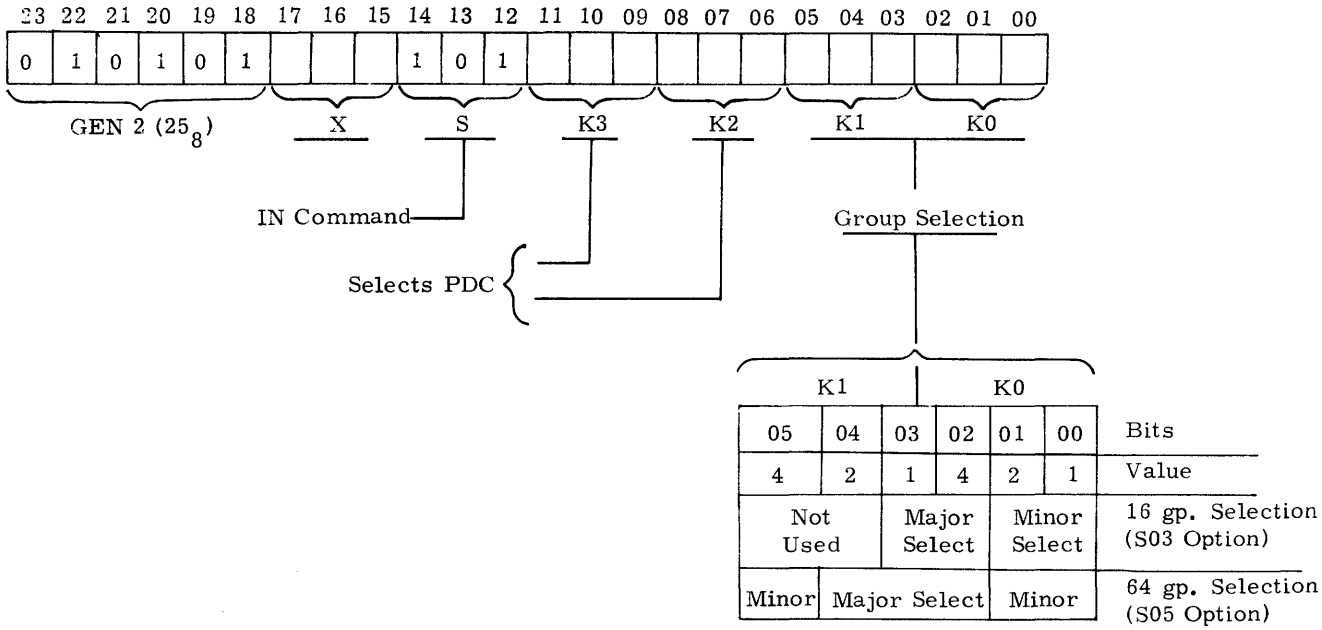


Fig. DIN. 2 IN Command Format

The digital inputs are terminated on sticks within the termination cabinet. Each stick is divided into digital input termination groups of 24 inputs (points) and labeled:

ITxxyy

Where: xx = K3·K2 octal address

yy = K1·K0 octal address

The System Hardware Address Summary drawing supplied with each system identifies the digital input signals and their termination points.

Power is supplied from a buss bar (BB) in the termination cabinet to the digital input contacts. Normally +28VDC is supplied, however, where the contacts are operated in an environment that may be contaminated easily, +125VDC may be used. The Model Number Option associated with the power supply is described earlier in this section.

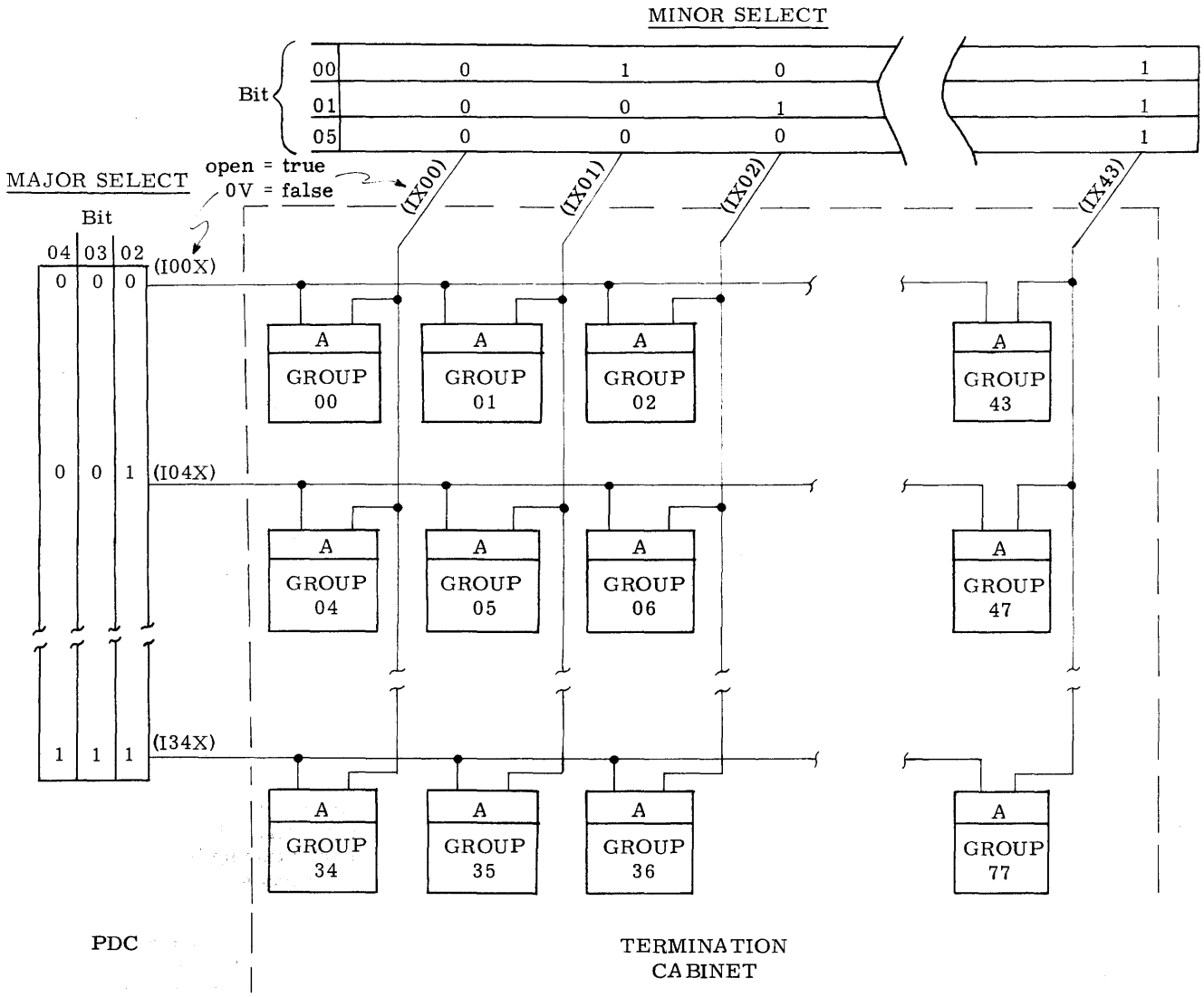
In many systems, the power supply voltage on the buss bar is jumpered directly to the data input termination point for bit 23. This serves as a validity bit indicating that the circuit breaker and power supply are providing power to the system contacts when bit 23 is a "one".

From the termination sticks, the digital input signals are applied through signal conditioning circuits. These signal conditioning circuits convert the digital inputs to a form suitable for input to standard logic circuits. From the signal conditioning circuits, the signals are applied to gating circuits which are enabled according to the group addressed by the IN command. The signal conditioning circuits and gates are contained on a single printed wiring borad which is selected according to the signal input type. A partial list of these signal conditioning boards is provided in the Model Number/Options section.

Optionally, change detection signal conditioning circuit boards may be contained in the system. These signal conditioning boards provide pulse outputs suitable for use as API input signals when: (1) any contact in a group opens, (2) any contact in a group closes, or (3) when any contact in a group changes state (opens or closes).

Fig. DIN. 4 illustrates the basic logic of a Change Detector signal conditioning board. Although it illustrates a Change Detector board connected for +28V/+125V (depending on system option) switching by the digital input contacts, the board may be connected for GND switching.

When a digital input contact changes state, a relay within the Change Detector also changes state. If any relay within the group changes from de-energized to energized, a pulse is coupled from its d/dt circuit resulting in an output at the U and W pins for use as an automatic program interrupt. If the relay changes from energized to de-energized, the d/dt couples a pulse to the V and X output for use as an automatic program interrupt. These outputs may be connected together providing a signal that indicates either change. The status of the group contacts may be read-in to the A Register by addressing the digital input group.



NOTES: (1) The group address corresponds to the K1, K0 octal address.

(2) The input termination groups are marked:
IT $\overline{XX}$ $\overline{YY}$
$\overline{XX} = \overline{K3} \cdot K2$ Octal Address
$YY = K1 \cdot K0$ Octal Address

Fig. DIN. 3 Input Group Selection

The signal conditioning boards with change detection have 24 inputs (on group) per board instead of 48 inputs for other signal conditioning boards. Each group of 24 change detection inputs require two groups of input stick capacity.

From the signal conditioning boards the selected data group is routed through isolation amplifiers which act as buffers and line drivers. The isolation amplifier provides sufficient drive to send data to the PDC in the Central Systems Unit. Twenty-four isolation amplifier circuits are contained by one printed wiring board (PX1000IIAA1orB1). Since only one group (24 inputs) is enabled at any one time, only one board is required in a system. The data inputs from the selection circuitry are daisy-chained to the isolation amplifier input. The output from the isolation amplifier is at +7.5 volts for a true signal (data bit = 1) and at 0 volts all other times.

CSU DATA FLOW

The twenty-four data bits of the addressed group are routed from the isolation amplifier in the Termination Cabinet to the Process Digital Controller located in the CSU.

As shown on sheets 10 and 11 of the PDC logic, 68C995755, data from the isolation amplifiers are

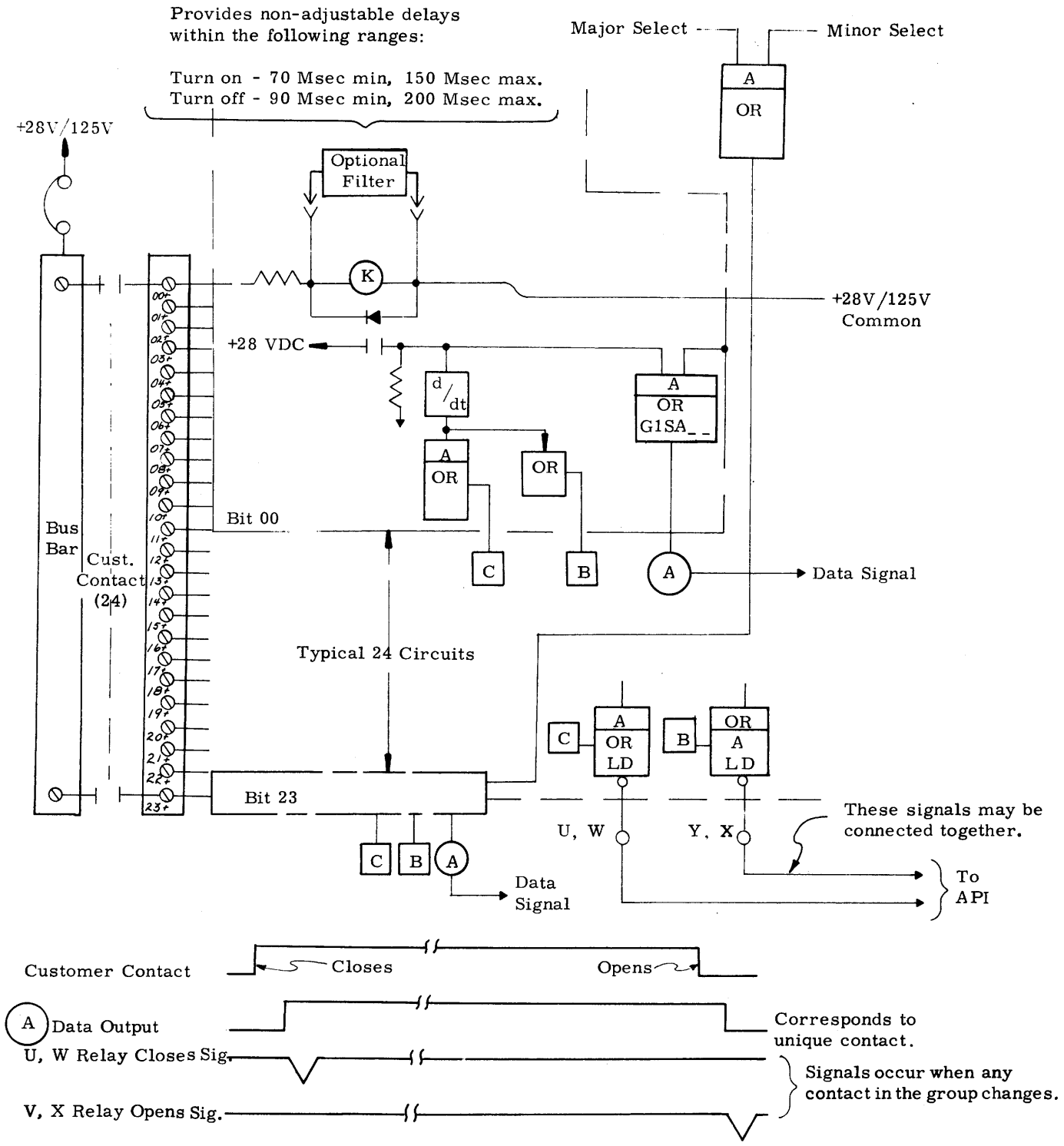


Fig. DIN. 4 Change Detectors

applied to line receiver circuits, (M0DB23 - 00). Data are gated through these line receivers by the decoded S and K3, K2 bits of the IN command. Decoding S=5 and the K3, K2 bits equal to the pin selected address enables D0IND1 (sheet 6) and D1DNIN1, 2, 3, 4, to perform the gating function. The output from the line receivers is at 0 volts for a closed or true data bit and at 5 volts for a open or false data bit.

The data from the PDC are routed to drivers and line receivers in the I/O Expander. From the I/O Expander, the data signals at 0 volts for true and 3.5 volts for false are gated through the I/O Input gates and the parallel adder unit to the A Register. The operation of the Arithmetic Unit during the execution of IN commands is described in the Arithmetic Unit Theory description contained in this book set.

DIGITAL OUTPUTS

Fig. DOUT. 1 illustrates the basic output control and signal flow within the Digital I/O Subsystem. Operation of the optional Pulse Source Initiator (AS08 option) is described later in this section.

> NOTE
>
> Logic element mnemonics and sheet numbers contained in paranthesis in the following text refer to the Process Digital Controller (PDC) logic, 68C995755, unless otherwise specified.

The following steps illustrate the general operating sequence of the digital output logic in the normal (non-test) mode.

1. If the PDC is not busy from a previous operation, an OUT command addressed to the PDC (K3, K2) with K1, K0 equal to 00 initiates the digital output operation. The contents of the Arithmetic Unit A Register (Data/Control Word) are transferred to the Output Buffer Register (F1OB23-00, sheets 18 - 23).

> NOTE
>
> A software timer using a clock API may be set at this time. If this time period elapses, an Echo API will indicate an error.

2. The PDC is placed in the busy state (F1SMXB, sheet 15) causing the ready line (G0AJNR, sheet 14) for JNR monitoring to go not ready.

3. The following checks are performed to determine if a fault exists in the digital output subsystem.

   a. All 17 data switches (least or most significant depending on the group being addressed) are enabled (F1SFDS, D0SDSF, sheet 15) and then the data switch outputs are checked (Y1ETO1, G0EDET, sheet 31) to determine if all 17 are on (i.e., no open data switches).

   b. The Enable 17 data switches signal (D0SDSF) is disabled, and prior to enabling the data bits to the switches, a check (Y1EDSO sheet 31) is made to determine if all data switches are off (i.e., no shorted data switches).

   c. During the time the output relays are energized, the PDC checks (Y1ETO1, G0EDET, sheet 31) to determine that one and only one group driver is on (i.e., that the addressed group driver is not open and that no other group drivers are shorted).

   d. After the output relay energization time has elapsed, the data switches are disabled and then checked (Y1EDSO, sheet 31) to determine that no data switches remain on.

   Detection of an output fault places the JNE line (G0AJNE, sheet 14) in the "error" state, disables the output relay current (P0EBSO, sheet 31), holds the ready line (G0AJNR, sheet 14) "not ready", and lights (D0AERR, sheet 14) the FAULT indicator. No output relay energization can occur until the error condition is cleared. The error condition can be cleared by executing a JNE command (N1ES07, sheet 31), or manually by pressing the ALARM CLEAR switch or the ON/INT switch on the Programming and Maintenance Console when the console is enabled and being operated in the manual mode.

   Refer to the Output Fault Checking portion of this section for further details.

4. If no output fault is detected, the group driver corresponding to the address (A_{5-0}) is enabled (28 Volt Common) and the data switches corresponding to the data bits (A_{23-8}) are enabled, (+28V) energizing the corresponding output relays. Current is applied to the relays for the time interval specified by A_7 and the position of a jumper pin. If A_7 = 0, the short operate time of 3 or 8 milliseconds, depending on the position of a jumper pin (T0SNRM, sheet 16) will occur. If A_7 = 1, the long operate time of 8 to 40 milliseconds (adjustable) or 40 to 200 milliseconds (adjustable) depending on the position of another jumper pin (T0SALT, sheet 16) will occur.

   Latching relays will of course remain in the state dictated by the associated data bits and are normally enabled for the short operate time (A_7 = 0). Momentary relays remain in the set state, if dictated by the associated data bits, for the approximate duration of the energizing current and then revert to the reset state. Momentary relays are normally enabled for the long operate time (A_7 = 1).

   Fig. DOUT. 1 illustrates the connections and operation of both latching and momentary output relays. In addition to the data switch output (+28V = 1) and the group driver output (28 V Com when enabled), a Clear Signal (+28V) is also applied to latching relays during relay energization time. If the data switch output is disabled representing a "zero" data bit, current will flow through the reset relay. If, however, the data bit is a "one", the data switch will be enabled and current will flow through the set relay.

5. When the operating time specified by bit 7 and the jumper pins has elapsed and if no fault has occurred, the ready line reverts to the ready state for JNR monitoring and generating an Automatic Program Interrupt normally to complete the output operation.

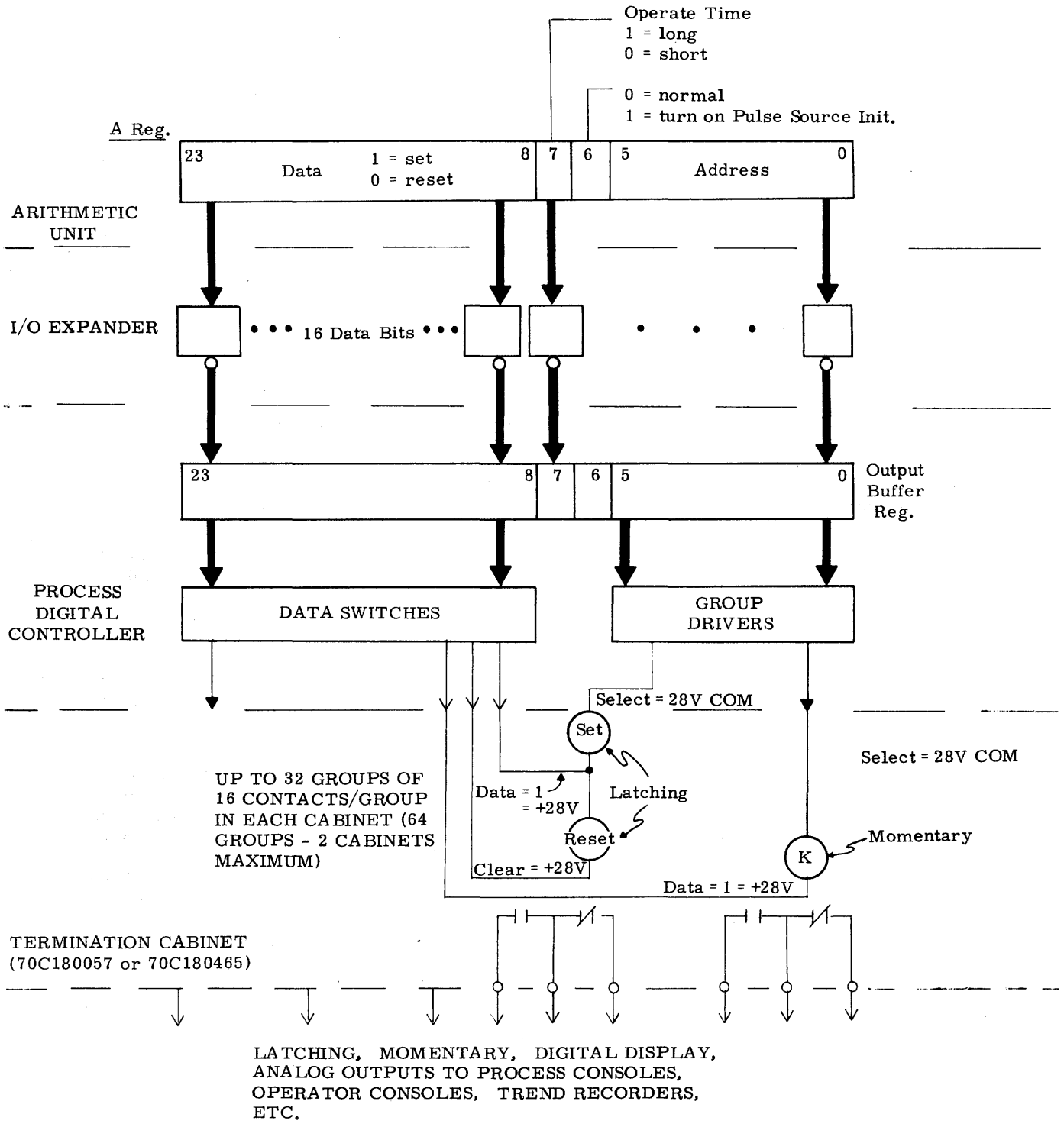


Fig. DOUT. 1 Digital Output Signal Flow

OUTPUT SEQUENCING AND CONTROL

The output sequencing and control portion of the PDC is shown on sheets 15, 16, and 17 of the PDC logic. Fig. DOUT. 2 illustrates some of the control functions performed and Fig. DOUT. 3 contains a timing diagram of the primary control signals.

The normal OUT command addressed to the PDC with K1·K0=00, causes the data from the Arithmetic Unit A Register to be loaded into the Output Buffer Register (F1OB23-00, sh. 18-21). Data is loaded (G0SLOD) into the Output Buffer Register during Phase A time of the OUT command when the PDC is ready.

G0DLOD = AS04 · APHA · SRDY

Enabling G0SLOD sets F1SFDS forcing on all 17 least significant data switches (DCLL, D08L - 16L, sh. 22, 23) or most significant data switches (DCLM, D08M - 16M) depending on the status of address bit 5. If address bit 5 is a "one" the most significant group is enabled and if bit 5 is a "zero" the least significant group is enabled. The least significant data switches control relay groups 00_8-37_8. The most significant data switches control relay groups 40_8-77_8 and are only contained in systems with the AS07 option. The output of the data switches are monitored to determine if 17 are "on". If 17 data switches are not enabled, the Fault (F1EFLT) and Error (F1ERRH) flip-flops are set and no output relays will change state. A detailed discussion of fault detection is described later in this section.

Phase B of the OUT command sets the Matrix Busy (F1SMXB) flip-flop disabling the ready line for JNR monitoring. This signal is also applied to the API module and when the PDC goes ready at the end of the operation, an interrupt will be initiated. At the end of Phase B, the Arithmetic Unit is free to execute other instructions. If another OUT to the PDC is executed it will be ignored until the PDC is ready. A JNR command may be executed for this purpose or an interrupt will occur when the operation is complete.

After the fault check to determine if all 17 data switches can be turned on, the Force Data Switches signal (D0SDSF) is disabled and the Enable Group Drivers flip-flop (F1SEGD) is set. Setting F1SEGD enables the Group Drivers that correspond to the group address (A_{4-0}).

Setting F1SEGD also provides an input to a 110 Microsecond delay circuit, T0SHCH (sheet 16). The output of this delay circuit enables a fault check to determine that no data switches are on. If a data switch is on, a fault exists and operation of the group drivers is inhibited preventing any relays from changing state. A detailed discussion of fault detection is described later in this section.

The timer circuit, T0SHCH, also sets the Enable Data Switches flip-flop (F1SEDS) after expiration of the 110 μsec. delay. Setting the Enable Data Switches flip-flop enables the data switches corresponding to address bit 5 and the status of the data bits. Enabling the data switching, in conjunction with the enabled group drivers, will energize the digital output relays.

The Enable Data Switches flip-flop also applies a signal to the time delay circuits, T0SNRM and T0SALT, that determine the time duration that current will be applied to the relays. Time delay circuit T0SNRM establishes this time interval when bit 7 of the control word from the AU is "0". When the time interval determined by bit 7, and the setting of the delay circuit has elapsed, the Matrix Busy flip-flop also applies a signal to a 110 μsec. time delay circuit, T0SHCH (sheet 16). T0SHCH, after the 110 μsec. delay, enables G1CODS (sheet 17) to verify that no data switches remain on, and clears the Enable Group Drivers flip-flop, F1SEGD. Clearing the Enable Group Drivers flip-flop turns off the group drivers and enables the ready line, G0SRDY, triggering an automatic program interrupt and providing a ready signal for JNR monitoring. This ready signal, however, cannot be enabled if an error was detected in any of the fault checks. A fault check error enables N0ERRH (sheet 31) which inhibits the ready signal, G0SRDY. If no error is detected, the ready signal is enabled completing the digital output operation. A subsequent OUT command may be executed to initiate another digital I/O operation.

OUTPUT SELECTION

Fig. DOUT. 2 illustrates the basic output selection scheme in the Process Digital I/O Subsystem. Address bits 0 thru 4 of the control/data word from the AU are decoded to enable a unique Group Driver, (GDxx where xx is equal to the octal value of address bits 0 thru 4). Address bit 5 is used in systems with more than 37_8 output groups to select a particular group of output data switches. When bit 5 is a "zero", the Least Significant Data Switches (DCLL, D08L - 16L, sheet 22, 23) are enabled according to the data bits of the control/data word. When bit 5 is a "one", the Most Significant Data Switches (DCLM, D08M - 16M sheet 28, 29) are enabled. The Least Significant Data Switches control relay groups 00 thru 37_8 (bit 5 = 0) and the Most Significant Data Switches control relay groups 40 thru 77_8 (bit 5 = 1).

Fig. DOUT. 4 illustrates the control and current flow associated with the selection of a particular relay. P0EBSO (sheet 31) is enabled applying 28V Common to the Group Drivers provided no output fault exists. If a fault is detected, 28V Common is removed from the Group Drivers and no relay select current can flow. A detailed discussion of fault detection is described later in this section.

A particular Group Driver is enabled during the output operation according to address bits 0 thru 4. Enabling a Group Driver (P0GD00 in Fig. DOUT. 4) applies the 28 Volt Common signal to one relay group (16 relays) controlled by the Least Significant Data Switches (Groups 00 thru 37_8) and one relay group controlled by the Most Significant Data Switches (Groups 50 thru 77_8) if more than 37_8 groups are contained in the system.

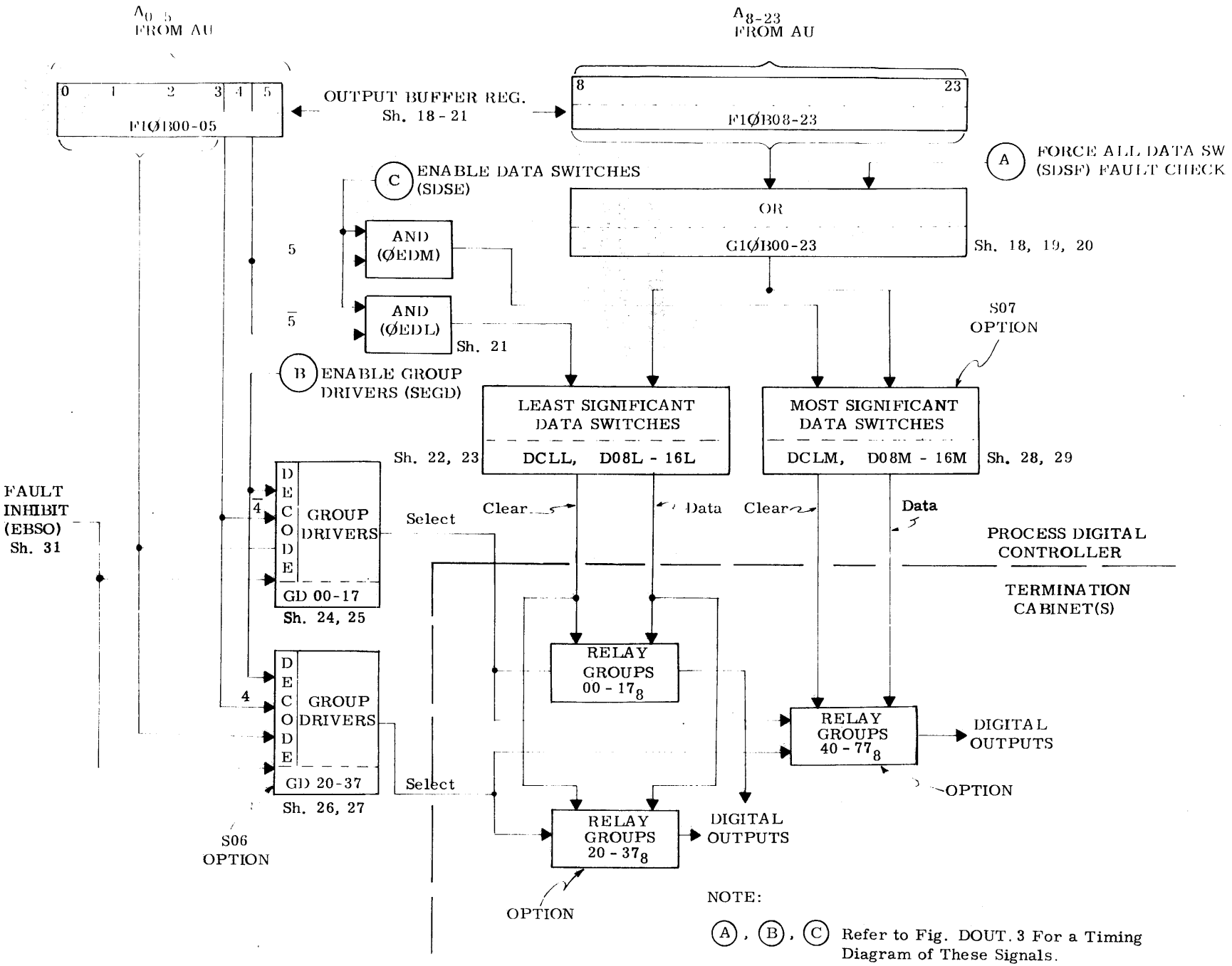


Fig. DOUT. 2 Digital Output Block Diagram

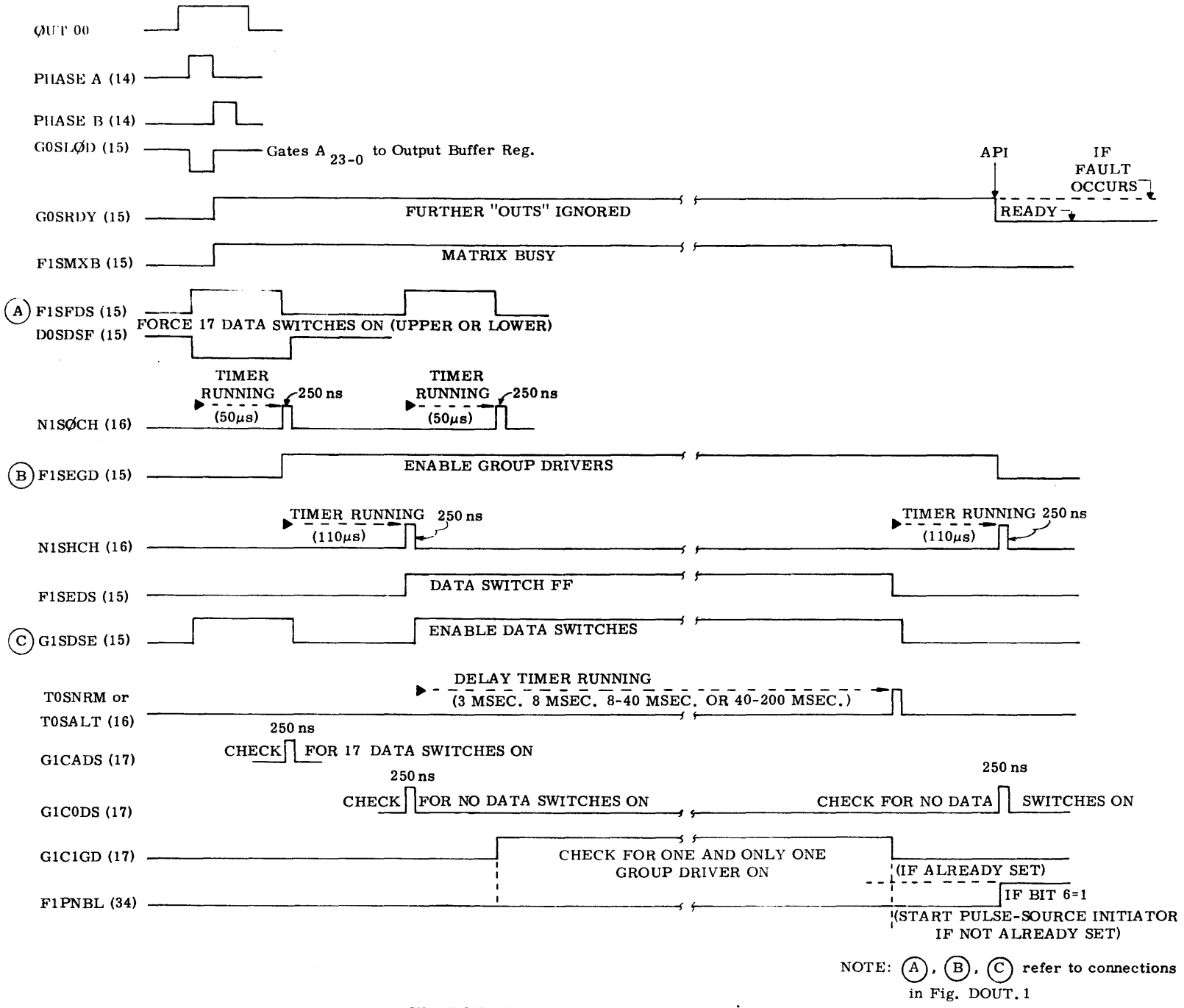


Fig. DOUT. 3 Digital Output Timing Diagram

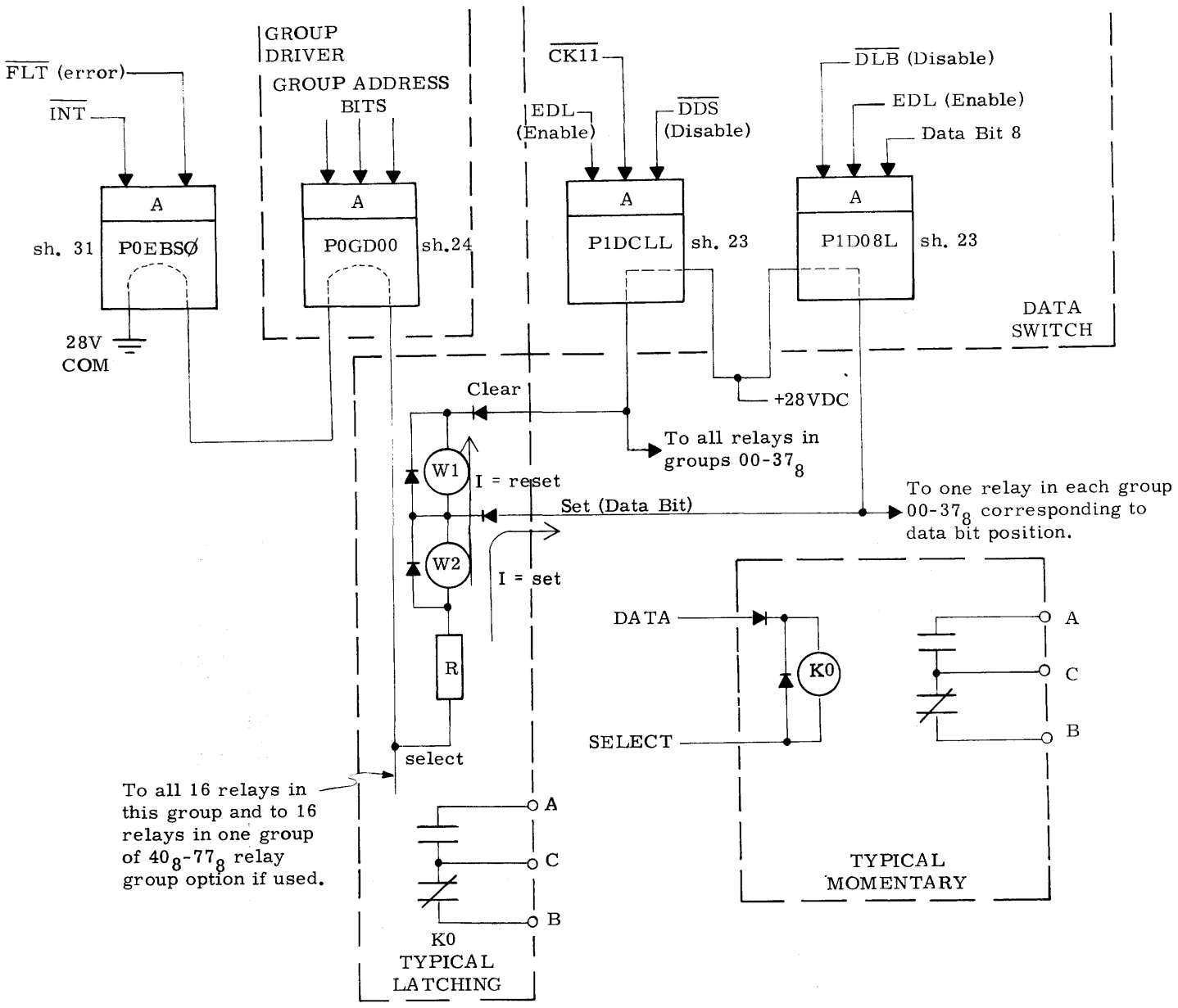
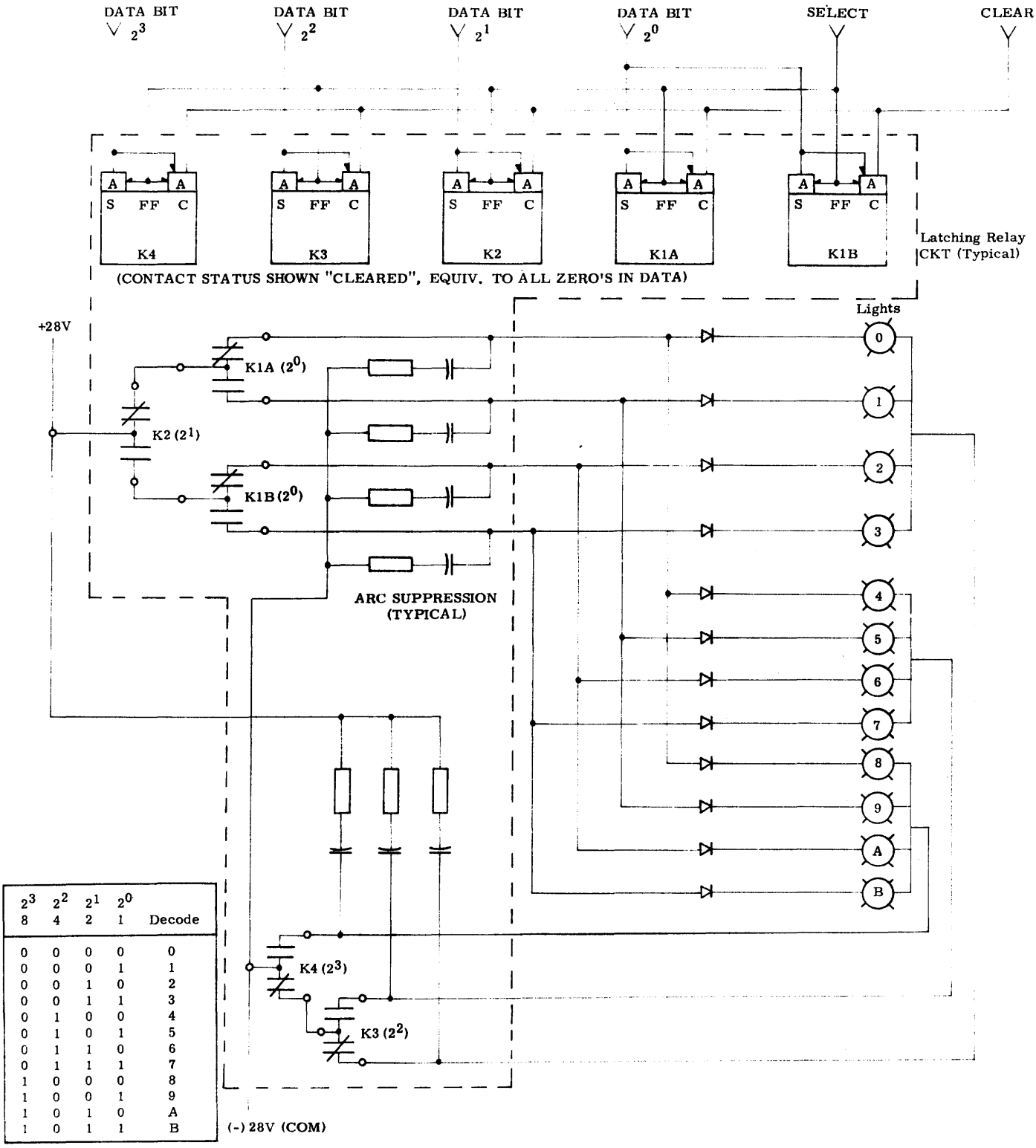


Fig. DOUT. 4 Output Relay Selection

The Data Switches, which are enabled according to the data bits of the data/control word from the AU, apply +28 volts to the relay in each group that corresponds to the bit position. Therefore, the relay group having the 28 volt common signal enabled to it will be controlled by the data switches.

Control of latching relays and momentary relays is slightly different. As shown in Fig. DOUT. 4, three lines are connected to a latching relay. In addition to the Group Driver output and the Data Switch output, a Clear line is required for latching relays. The Clear line is always enabled during the time the Data Switches are enabled. To understand the operation of a latching relay, consider the following two conditions while referring to Fig. DOUT. 4. First, consider that the Select line from the Group Driver is enabled applying 28V Common to the bottom of the latching relay and the corresponding data bit (8 in Fig. DOUT. 4) is a "one". Since the corresponding data bit is a "one", +28 volts is enabled to the top of the W2 portion of the latching relay. Therefore, current will flow through the W2 portion setting the relay. Notice that no current will flow through the W1 portion even though the Clear line is enabled applying +28 volts to the top of W1, since the bottom of W1 is at +28 volts from the enabled data line. Second, consider that the corresponding data bit is a "zero". Since the data bit is a "zero", an open will be present on the Data line.



2^3 8	2^2 4	2^1 2	2^0 1	Decode
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B

Fig. DOUT. 5 Decimal Display Output

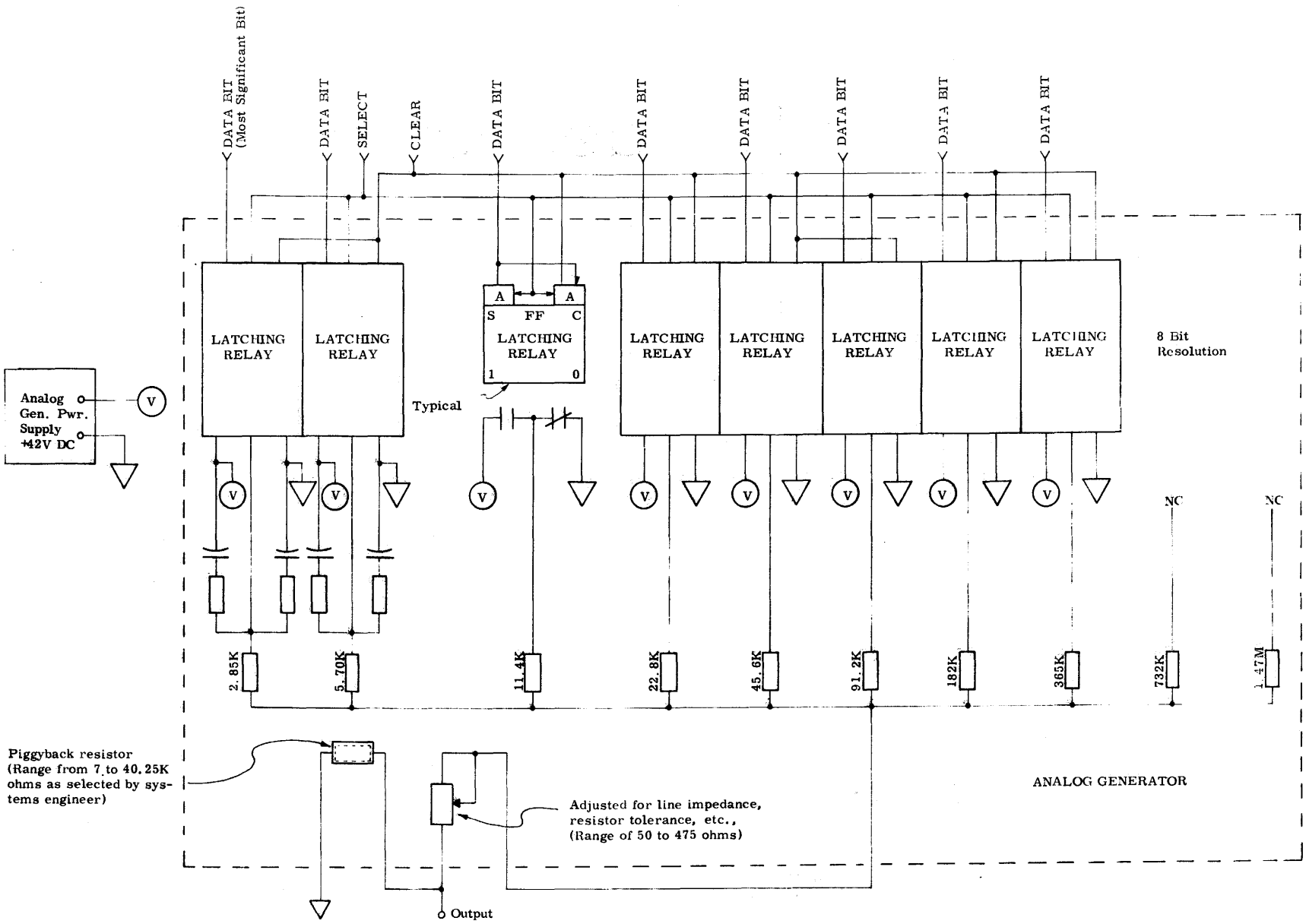


Fig. DOUT.6 Analog Generator Output

Since the Select line is enabled and the Clear line is always enabled, current will flow through both W1 and W2. The current flow through W1 will reset the relay. Therefore, the latching relay is set by a "1" data bit and remains in that state until changed by a "0" data bit.

Momentary relays remain in the set state only during the time (approximate) that current flows through them. Therefore, momentary relays are normally enabled by a long operate time (bit 7 of the control/data word = 1) of 8 to 40 or 40 to 200 milliseconds as selected by a jumper pin and variable adjustment. Since the momentary relays return to the reset state when current is removed, the clear signal is not required for these relays. The select line enables the 28 Volt Common line to the addressed momentary relay group and +28 Volts is enabled to only those relays that have a corresponding data bit equal to "1". Therefore, current will only flow through those relays that correspond to the address and "1" data bits in the data/control word. These relays will be set, but only for the duration of the output energization current.

OUTPUT TERMINATIONS

As previously mentioned, the maximum output capacity for each Process Digital Controller is 64 groups having 16 points per group or 1024 digital output points.

The output contact rating may be either 100VA or 250VA depending on the application. Up to 32, 100VA output groups or 16, 250VA output groups may be installed in a single output termination cabinet. As previously mentioned, the outputs may be momentary or latching.

Decimal Displays

Digital output groups capable of driving four decimal displays are available. Fig. DOUT. 5 illustrates the operation of a typical display output using 4 data bits. Since the relays are latching, the display will remain until changed by a subsequent digital output addressed to the group. The 16 bit data format of the data/control word is capable of controlling four such displays.

Analog Outputs

Any latched contact output group may be used to control an analog generator providing an analog voltage or current corresponding to the data field. Either 8 or 10 bit analog generators may be used. Two 8-bit analog generators are incorporated in one output group. The output voltage or current range is determined by the application and adjustment of the generators. Fig. DOUT. 6 illustrates the typical operation of an 8-bit analog generator. An analog output requires a stable +42 VDC power supply in the output termination cabinet. The status of the individual relays, and consequently the output, depends on the status of the individual data bits of the data/control word.

The resistor values in the analog generator are in a binary progression from the most significant to the least significant data bit. In an 8-bit analog generator, resolution of 1 part in 255 is provided. In a 10-bit analog generator, resolution of 1 part in 1023 is provided. Enabling a digital output relay parallels the associated resistor with any other resistor that may be enabled between the common power supply and the output point.

OUTPUT FAULT CHECKING

In order to protect the process and the subsystem hardware, the PDC contains error checking hardware which monitors the digital output portion of the subsystem. During the execution of each digital output operation, the fault check logic determines if any one of the following errors exist:

1. Open data switch - All 17 data switches (least or most significant if more than 37_8 groups are contained in the system) are enabled and then checked to determine if all 17 are on.

2. Shorted data switch - Prior to enabling the data switches addressed by the data/control word, the data switches are checked to determine that all of them are off.

3. Selected group driver failing to turn on - During the time the addressed relay group is to be energized, a check is performed to determine that one group driver is on.

4. More than one group driver turning on - During the time the addressed relay group is to be energized, a check is performed to determine that only group driver is on.

5. A short occurred in the data switch during this operation - After the relay drive current has been disabled, a check is performed to determine if any data switch remains on.

Detection of any of the above errors sets an Output Fault (F1EFST) flip-flop and a Error Hold (F1ERRH) flip-flop. While the Output Fault flip-flop is set, relay energization current is disabled. While the Error Hold flip-flop is set, the PDC ready line is held in the "not ready" (busy) state for JNR monitoring and preventing another digital output operation. The Error Hold flip-flop in the set state also enables the error line for JNE monitoring. The Error Hold flip-flop may be reset by any one of the following means:

1. Execution of JNE (after previously initiated operate time has elapsed).

2. Execution of an ABT command with K1, 0 = 00.

3. Pressing the ON/INIT switch on the Programming and Maintenance Console to initialize the system.

4. Pressing the ALARM CLEAR switch on the Programming and Maintenance console.

F1ERRH = G0ESFF = error detected

$\overline{\text{F1ERRH}}$ = G0ECEH

G0ECEH = S07 · PHB + INT

N1ES07 = JNE command

G1IENT = Initialize + ABT with K1=0 + ALARM CLEAR

The Output Fault flip-flop (F1EFLT, sheet 31), when set, disables output relay energization by disabling F0EBSO (sheet 31) as shown in Fig. DOUT. 4. The Output Fault flip-flop is cleared by ABT with K1 = 0, pressing the ALARM CLEAR switch or INIT/ON switch, or by an OUT command that is executed following the clearing of the Error Hold flip-flop by a JNE command.

A1EFLT = G0ESFF = error detected

$\overline{\text{F1EFLT}}$ = G0ECFF

G0ECFF = INT + ELOD

N1ELOD = SLOD = OUT command execution and "ready"

G1IENT = Initialize + ABT with K1=0 + ALARM CLEAR

Fig. DOUT. 7 illustrates the operation of the error detection gate, G0EDET, for all error checks. The timing diagram illustrated in Fig. DOUT. 3 shows the timing of the various error control signals (G1CODS, G1CIGD, and G1CADS).

The data switch short check, which checks for no data switches on, is enabled by G1CODS prior to relay energization time. The detector, Y1EDSO, provides a "one" output when any input is at +28 volts. The output data switches are tied to the input (P1DANY) of Y1EDSO. If all output data switches are disabled, P1DANY will be at 0 volts. If any data switches are on, the output of P1DANY will be near 28 volts indicating an error when G1CODS is enabled.

The check to determine that one and only one group driver is on is enabled by G1CIGD during relay energization time when one group driver corresponding to the data/control word should be enabled. The detector, Y1EOT1, provides a "zero" output indicating that only one group driver is enabled when the P0GANY input is at +28 volts and when the P0GTWO input only has one 2.4K ohm resistor connected to ground. Any other condition indicates that no group drivers are enabled (P0GANY = 0) or that more than one group driver is enabled.

Near the beginning of the digital output operation, an open data switch check is performed by forcing (D0SDSF) the upper or lower 17 data switches on for a short period of time (50 μsec.) and checking to determine that they are all on. This check is enabled by G1CADS and the status detected by Y1ENAL. The P1DALL input to Y1ENAL, is at approximately +28 volts when all data switches are on or is at approximately 0 volts when any data switches are off. A 0 volt input indicates an error condition, enabling Y1ENAL, which enables G0EDET to set the fault and error hold flip-flops.

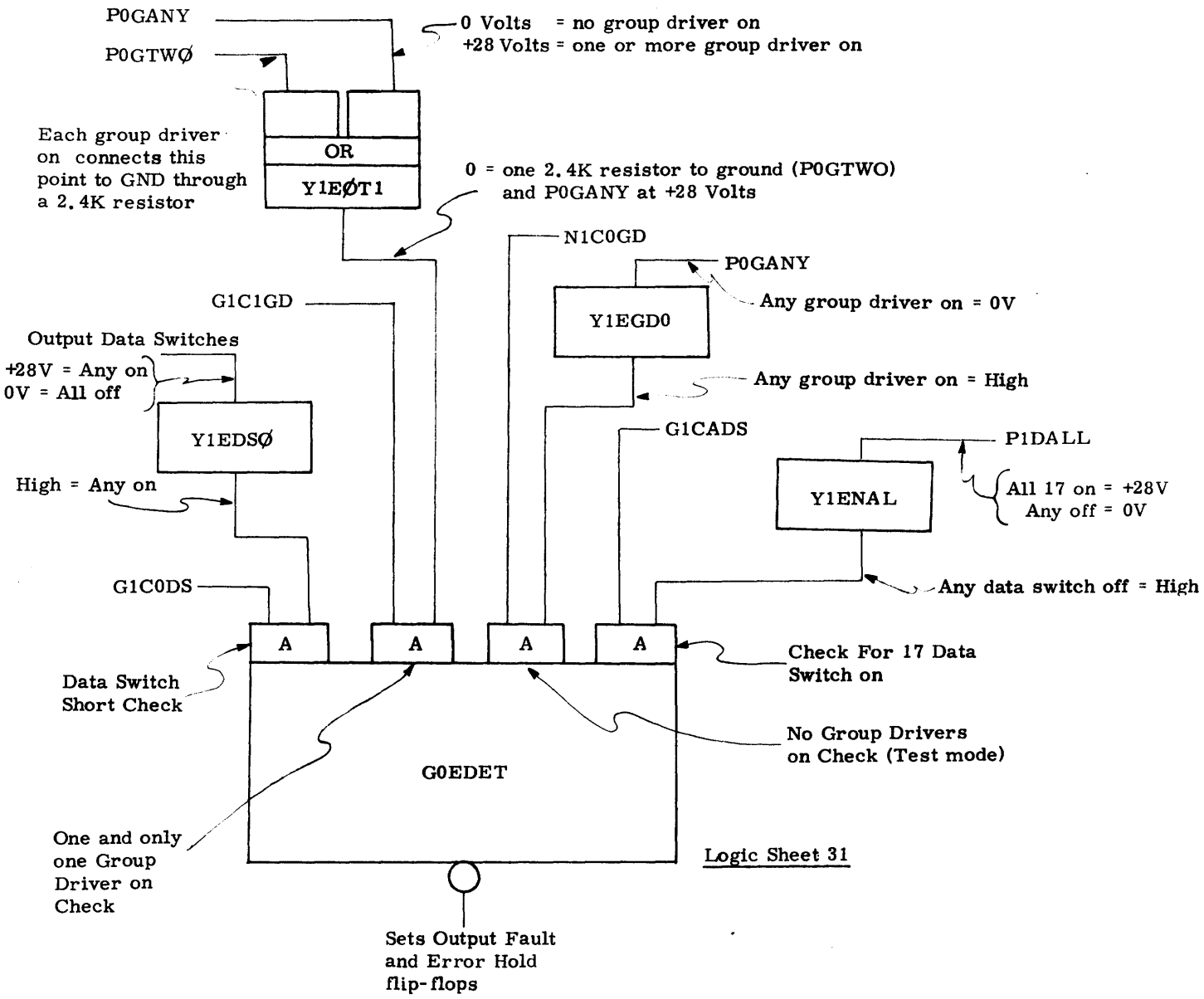


Fig. DOUT.7 Error Detection Block Diagram

PULSE SOURCE INITIATOR (OPTION)

The optional (4846 A(B)S08) Pulse Source Initiator (PSI) provides drive pulses to control digital set point stations. The PSI may be selected for compatibility with any of the following (or similar) stations:

1. General Electric Co.GE-MAC* 543-16 Control Unit.
2. Foxoboro Co. 62HM and 67 CE/CP series controllers.
3. Leads and Northrup Co. Sigma "Cyclomone" stepping motor.
4. Moore Computer-Set Synchro or Mini-Synchro Controller.

The PSI is started and stopped under program control. It is enabled or started by executing an OUT command with bit 6 of the data/control word in the A Register = 1. It is disabled or stopped by executing an ABT command.

As shown in Fig. PSI. 1 the output from the PSI may be either a square wave (pulse) or a single pulse (duration). The frequency of the square wave may be equal to the input frequency or one-half the input frequency. The input frequency may be selected from the line frequency or the adjustable pulse generator in the CSU or from an external system source. Each pulse from the PSI triggers an automatic program interrupt providing automatic program control of the duration of the output signal.

The PSI output may be applied to one or more control stations by latching relays or the output may be used to control an interposing relay (4847AS11 as shown in Fig. PSI. 3) to interrupt an AC wavetrain or DC pulse train at the PSI output rate. The PSI output, AC wavetrain or DC pulse train may be directed to one or more control stations by digital output latching relays in the termination cabinet.

Program control of the Pulse Source Initiator normally occurs in the following manner:

1. A memory location is loaded with the count, minus one, of the desired number of pulses to be outputted. This location will be decremented by an API generated from each output pulse. When the memory location is decremented from 0 to -1, a non-inhibitable ECHO API is generated which results in an ABT command being executed to disable the pulse source initiator.
2. An OUT command addressed to the PDC initiates a normal digital output operation. It performs the normal fault checks and if no faults exist closes the addressed relay(s). With bit 6 of the OUT command a "one" the PSI output operation (pulses) is initiated. The fall of each output generates an API which contains a DMT command of the memory location loaded in step 1 above.
3. The PSI continues to output pulses until the DMT ECHO occurs signifying that the desired number of output pulses have occurred. This ECHO generates another API which contains an ABT command to deactivate the PSI. The ECHO generates another interrupt which may be used to branch to a subroutine that updates the DMT memory location and data/control word, and initiates the next operation.

SEQUENCING AND CONTROL

Executing an OUT command with bit 6 of the control/data word a "one" operates the same as any other digital output operation, as previously described, until the PDC goes ready. That is, executing the OUT command cycles the PDC to not ready, performs the fault check, and if no fault exists, sets the relays to the configuration specified by the data/control word. The output relays associated with the pulse source initiator outputs are normally latching relays.

As shown in Fig. DOUT. 3, the PDC again goes ready, and bit 6 equal to a "one" sets the Pulse Source Initiator Enable flip-flop, F1PNBL. When set, F1PNBL enables the output from the pulse source initiator. Clearing F1PNBL disables the pulse source initiator inhibiting the pulse output. F1PNBL may be cleared by executing an ABT command, the deadman timer timing out, or by manually initializing the system. The deadman timer is used to abort PSI operations if it is enabled for a time longer than the pin selected time interval of 1, 2, or 3 seconds. The ABT command with K1 = 1 only de-activates the PSI while an ABT command with K1 = 0 initializes the entire PDC.

F1PNBL = G0SEND · N0OB06

$\overline{\text{F1PNBL}}$ = G0ACPE + D0AZRO + T0PDMN

G0ACPE = ABT with K1 = 1

D0AZRO = Initialize + ABT with K1 = 0

T0PDMN = F1PNBL plus a pin selectable 1, 2, or 3 second delay.

Fig. PSI. 2 illustrates the basic timing of the pulse source initiator. The frequency of the source input is selectable by pin option. As previously mentioned it may be at the power input frequency (50 or 60 Hz), from the adjustable pulse generator option (200 to 2000 Hz), or from an external source. The output from the pulse source initiator may be equal to or one-half the input frequency, or the output may be enabled (duration) until turned off. The pulse output may be phase adjusted (T0PHSE) from 1 to 10 milliseconds by a trimpot.

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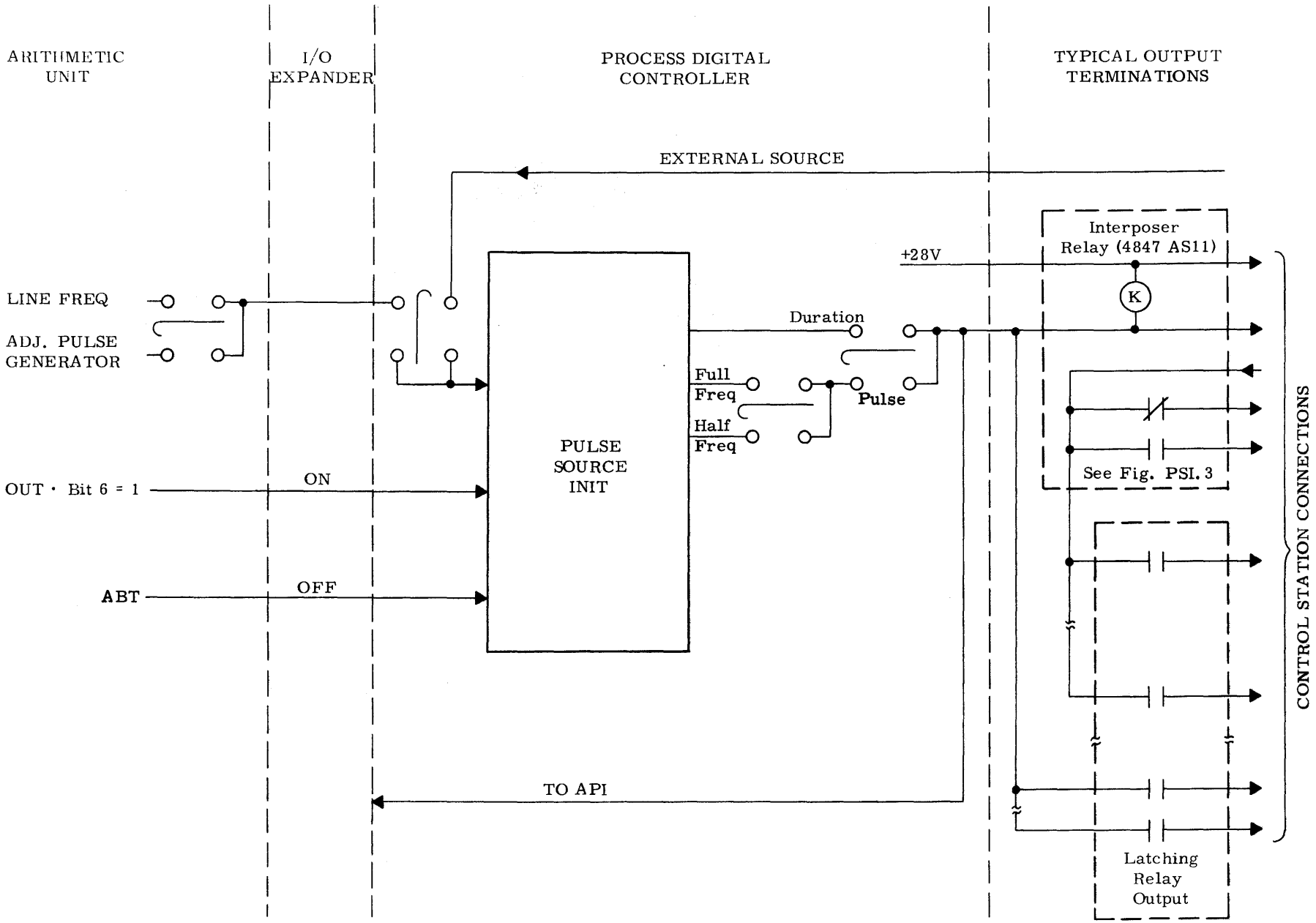


Fig. PSI. 1 Pulse Source Initiator, Block Diagram

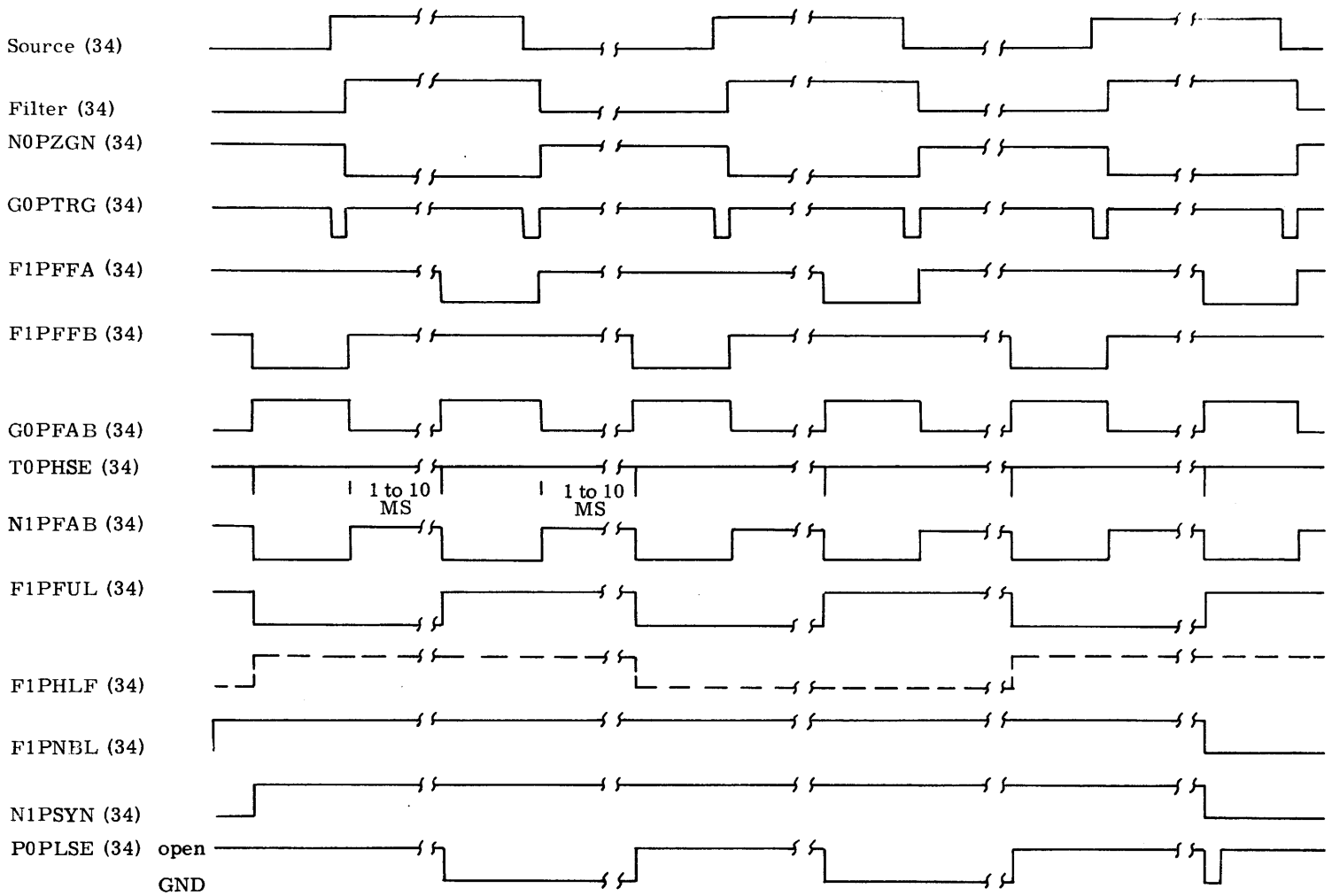
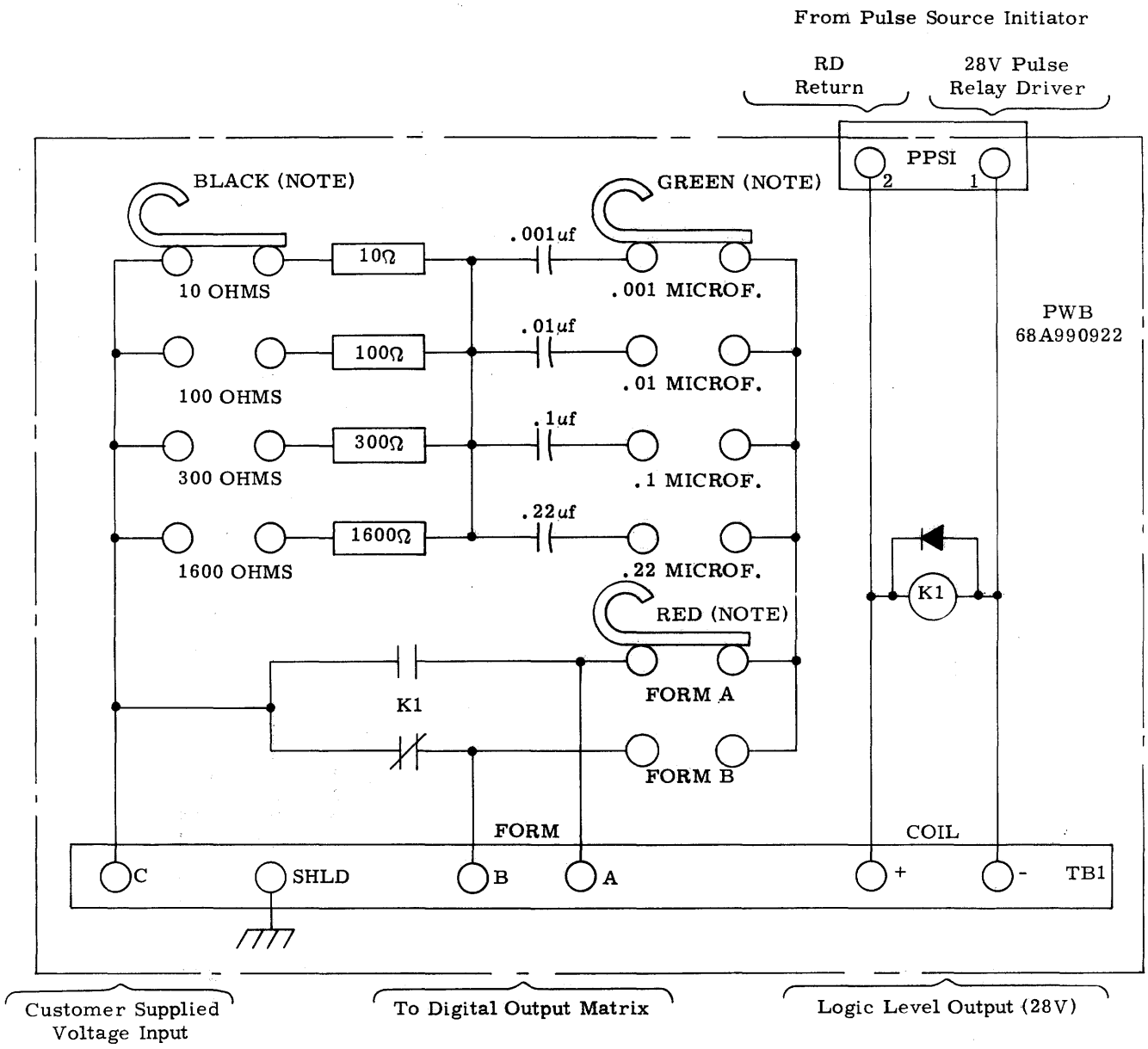


Fig. PSI. 2 Pulse Source Initiator Timing



NOTE: Position of pins for R/C suppression and contact form determined by requisition engineer. More than one pin can be used in black and green pin jacks to provide added combinations of R/C suppression. (PWB supplied with pins in all resistor and capacitor positions.)

Fig. PSI.3 Pulse Source Interposer (4847AS11)

TEST MODE

Hardware is included in the PDC to permit off-line testing using a software test program. In the test mode, the relay group drivers, data switches, and fault detectors may be tested using an off-line program.

The following paragraphs describe the operation of the hardware when the test mode commands are executed.

SEL - SELECT

The Process Digital Controller is placed off-line and in the test mode by executing an SEL (S bits = 0) command with K1 = 1, while the PDC is "ready". While in the off-line test mode, no relays can be energized (unless a hardware fault exists).

Executing an SEL command with K1 = 1 sets the Test Mode flip-flop, F1TEST (sh. 32). F1TEST is reset, removing the PDC from the Test Mode by executing an SEL command with K1 = 0 when the PDC is ready, an ABT command with K1 = 0, or by pressing the ON/INIT switch to initialize the system.

F1TEST = G0TSTF

G0TSTF = K1 = 1·SEL command· "Ready"

$\overline{\text{F1TEST}}$ = G0TCTF + D0AZRO

G0TCTF = K1 = 1· SEL command · "Ready"

D0AZRO = ABT with K1 = 0 + Initialize

The status of the Test Mode flip-flop is displayed by a white indicator on the IDOA5 board slot A09-FK.

A normal OUT command executed with K1 = 0 is ignored when the PDC is in the Test Mode. The OUT with K1 = 0 command is disabled in G1AS04 (sheet 14) by disabling G0AES4.

$\overline{\text{G0AES4}}$ = TEST· C110 + $\overline{\text{TEST}}$· $\overline{\text{CK10}}$

While in the Test Mode, the program may make several tests by executing OUT commands with the K1 bits encoded to specify the test operation. The following paragraphs describe these tests.

OUT - K1·KO =20

Executing this instruction in the test mode will cause a fault indication if any group driver is on or if less than 17 data switches are on. The group drivers are disabled by the OUT20 instruction and the data switches are controlled by bits 8 thru 23 of the data/control word contained in the A Register. Therefore, if A Register bits 8 thru 23 are all "ones" and there are no shorted group devices, no fault indication should occur. If bits 23 thru 18 of the A Register are not all "ones", a fault indication should occur following the execution of this instruction.

The OUT20 instruction disables all group drivers by enabling G0CNON (sheet 17). Enabling G0CNON enables G1CB00 (sheet 24) and disables G0GB00 (sheet 25). Enabling G1CB00 indicates address bit 0 = 1 which disables all even numbered group drivers (e.g., P0GD00, 2, 4, 6 ...). Disabling G0GB00 indicates that address bit 0 is a "zero" which disables all odd numbered group drivers (e.g., P0GD01, 3, 5, ...).

G0CNON = $\overline{\text{CK14}}$· TEST

G1CB00 = CNON

$\overline{\text{G0GB00}}$ = CNON

$\overline{\text{P0GD00, 2, 4, ...}}$ = CB00

$\overline{\text{P0GD01, 3, 5, ...}}$ = $\overline{\text{GB00}}$

To Verify No Group Drivers On gate, N1C0GD (sheet 17), is enabled which samples the output of detector Y1EGD0 (sheet 31) to determine if a fault exists. Since the group drivers are disabled by G0CNON, no fault should exist. Fig. DOUT. 7 illustrates the operation of Y1EG00.

N1C0GD = CTED· $\overline{\text{CK14}}$

The Verify 17 Data Switches On gate, G1CADS (sheet 17), is enabled which samples the output of detector Y1ENAL (sheet 31) to determine if all 17 data switches are on. As previously described, if bits 8 thru 23 of the A Register are all "ones", they should all be "on" and no fault should be detected. If, however, OUT20 was executed with one or more "zeros" in bits 8 thru 23 of the data/control word, a fault should occur. Fig. DOUT. 7 illustrates the operation of Y1ENAL.

G1CADS = CADT

G0CADT = C2+6· CDEL· $\overline{\text{CK14}}$· TEST

OUT - K1·KO = 30

Executing this instruction in the test mode will cause a fault indication if any group drivers are "on" or if any data switches are "on". The group drivers are disabled by the OUT30 instruction in the same manner as the OUT20 instruction. The data switches are controlled by bits 8 thru 23 of the data/control word in the A Register. Therefore, if the A Register contains all "zeros", no output fault should occur. If, however, A Register bits 8 thru 23 contain one or more "ones", a fault indication should occur.

The OUT30 instruction disables all group drivers by enabling G0CNON (sheet 17). Enabling G0CNON enables B1CB00 (sheet 24) and disables G0GB00 (sheet 25). Enabling G1CB00 indicates address bit 0 is a "one" which disables all even numbered group drivers (e.g. P0GD00, 2, 4, 6 ...). Disabling G0GB00 indicates that address bit 0 is a "zero" which disables all odd numbered group drivers (e.g. P0GD01, 3, 5 ...).

$G0CNON = \overline{CK14} \cdot TEST$

$G1CB00 = CNON$

$\overline{G0GB00} = CNON$

$\overline{P0GD00, 2, 4, \ldots} = CB00$

$\overline{P0GD01, 3, 5, \ldots} = \overline{GB00}$

The Verify No Group Drivers On gate, N1C0GD (sheet 17), is enabled which samples the output of detector Y1EGD0 (sheet 31) to determine if a fault exists. Since the group drivers are disabled by G0CNON, no fault should exist. Fig. DOUT.7 illustrates the operation of Y1EG00.

$N1C0GD = CTED \cdot \overline{CK14}$

The Verify No Data Switches On gate, G1C0DS (sheet 17), is enabled which samples the output of detector Y1EDSO (sheet 31) to determine if all data switches are off. As previously described, if bits 8 thru 23 in the A Register are all "zeros" no fault should occur. If one or more of these bits are "one", a fault should occur. Fig. DOUT.7 illustrates the operation of Y1EDSO.

$G1C0DS = CTED \cdot \overline{C2+6}$

The Clear Data Switch drivers (P1DCLL, M) are disabled by N0CK11 (sheet 17).

OUT - K1·KO = 40

Executing this instruction in the test mode should cause a fault indication. Two group drivers are forced "on" and the output of the more than one group driver detector (Y1EOT1) is checked for the error indication. The OUT40 instruction disables all data switches and checks the output of the Data Switch Short Check detector (Y1EDSO) indicating a fault of any data switches are on.

The Disable Data Switches gate, G1CDDS (sheet 17), is enabled disabling all output data switches (P1D23L -00L, P1D23M-00M). The Verify No Data Switches On gate, G1C0DS (sheet 17) is enabled which samples the output of a detector (Y1EDSO) to determine if any data switches are on. Fig. DOUT.7 illustrates the operation of Y1EDSO.

$G1CDDS = CK14$

$G1C0DS = CK14 \cdot CTED$

The Force Two Group Drivers gate, G0CTWO (sheet 17), is enabled forcing two group drivers on by disabling D0GB00 and enabling D1GB00. The Verify Only One Group Driver on gate, G1C1GD is enabled to check the output of the One and Only One Group Driver On detector (Y1EOT1) which should provide an output fault. Fig. DOUT.7 illustrates the operation of Y1EOT1.

$G0CTWO = CK14 \cdot \overline{CK12} \cdot TEST \cdot \overline{CK11}$

$G1C1GD = CK14 \cdot CTED$

OUT - K1·KO = 50

Executing this instruction should cause a fault indication. All group drivers are disabled and the output of the One and Only One Group Drive On detector (Y1EOT1) is sampled which should provide the fault indication. Executing OUT50 also disables all data switches and samples the output of the Data Switch Short Check detector (Y1EDSO) providing a fault indication if any data switches are on.

The OUT50 instruction disables all group drivers by enabling G0CNON (sheet 17). Enabling G0CNON enables G1CB00 (sheet 24) and disables G0GB00 (sheet 25). Enabling G1CB00 indicates address bit 0 = 1 which disables all even numbered group drivers (e.g. P0GD00, 2, 4, 6 ...). Disabling G0GB00 indicates that address bit 0 is a "zero" which disables all odd numbered group drivers (e.g. P0GD01, 3, 5 ...).

$G0CNON = \overline{CK14} \cdot TEST$

$G1CB00 = CNON$

$\overline{G0GB00} = CNON$

$\overline{P0GD00, 2, 4, \ldots} = CB00$

$\overline{P0GD01, 3, 5, \ldots} = \overline{GB00}$

The Verify Only One Group Driver On gate, G1C1GD (sheet 17) is enabled to sample the output of the One and Only One Group Driver On detector (Y1EOT1) which should provide an output fault indication since no group drivers are on. Fig. DOUT.7 illustrates the operation Y1EOT1.

$G1C1GD = CK14 \cdot CTED$

The Disable Data Switches gate, G1CDDS (sheet 17), is enabled disabling all output data switches (P1D23L -00L, P1D23M-00M). The Verify No Data Switches On gate, G1C0DS (sheet 17) is enabled which samples the output of a detector (Y1EDSO) to determine if any data switches are on. Fig. DOUT.7 illustrates the operation of Y1EDS0.

$G1CDDS = CK14$

$G1C0DS = DK14 \cdot CTED$

OUT - K1·KO = 60

Executing this instruction in the test mode should not cause an output fault. All data switches are disabled and the Verify No Data Switches On detector (Y1EDSO) output is monitored. Operation of the Group Drivers is controlled by the address bits (0 thru 4) of the control/data word in the A Register. The output of the One and Only One Group Driver On detector (Y1EOT1) is sampled to determine if only one is enabled. By selecting address bit configurations, an individual faulty group driver may be found and identified.

The Verify Only One Group Driver On gate, G1C1GD is enabled to sample the output of the One and Only One Group Driver On detector (Y1EOT1). Since the

address should enable one group driver no fault should be detected. Fig. DOUT.7 illustrates the operation of Y1EOT1.

G1C1GD = CK14·CTED

The Disable Data Switches gate, G1CDDS (sheet 17), is enabled disabling all output data switches (P1D23L -00L, P1D23M-00M). The Verify No Data Switches On gate, G1C0DS (sheet 17) is enabled which samples the output of a detector (Y1EDSO) to determine if any data switches are on. Fig. DOUT.7 illustrates the operation of Y1EDSO.

G1CDDS = CK14

G1C0DS = CK14·CTED

IN

An IN command addressed to the PDC, when in the test mode, loads the A Register with the contents of the PDC Output Buffer Register. IN is normally executed following an OUT60 command. This should load the A Register with the same value as it contained prior to execution of OUT60. If not, either the data path between the AU and the PDC is faulty or the Output Buffer Register is faulty.

Executing an IN command in the test mode enables D0INOB (sheet 7). Enabling D0INOB enables the contents of the Output Buffer Register (F10B23-00) thru the Test Output Buffer Gates (G1TB23-00, sheet 12) to the Arithmetic Unit in the same manner as the data from a normal digital input operation.

TEST INDICATORS

The following indicators are provided in the process digital controller as an aid in testing and isolating component failures. These indicators are located on the edge of the printed wiring boards listed.

READY - This green indicator located on the IDOA5 board in slot A09-FK indicates the status of the ready line used for digital output JNR monitoring and for API generation. It is shown on sheet 14 of the PDC logic.

FAULT - This red indicator located on the IDOA5 board in slot A09-FK is lighted when the PDC detects a fault whether it is operating in the test mode or in the normal digital output mode. It is shown on sheet 14 of the PDC logic.

TEST MODE - This white indicator located on the IDOA5 board in slot A09-FK is lighted following the execution of an SEL 10 command which places the PDC in the off-line or test mode. The light is extinguished following the execution of a SEL 00 or, an ABT 00 command, or when the ON/INIT switch is pressed to initialize the system. It is shown on sheet 32 of the PDC logic.

GROUP DRIVERS ENABLED - This indicator located on the ISSB5 board in slot A08-FK is lighted whenever the output group drivers are enabled. It is shown on sheet 32 of the PDC logic.

DATA SWITCHES ENABLED - This indicator located (top) on the ISSB5 board in slot A08-FK is lighted whenever the output data switches are enabled. It is shown on sheet 32 of the PDC logic.

OUTPUT BUFFER REGISTER - The IDDA/C1 display printed wiring board, used for various test purposes, may be inserted in slot A11-AK to display the status of the PDC Output Buffer Register. The logic is shown on sheet 33 of the PDC logic.

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1100 A/B ANALOG INPUT SUBSYSTEM

TABLE OF CONTENTS

INTRODUCTION

This section describes the Model 4DP1100A/B Analog Input Subsystem (AIS) which is the analog input device, commonly called the "Analog Scanner", for the GE-PAC* 4010 and 4020 Computer Systems.

This subsystem is composed of combinations of the following functional modules:

4812A/B	Analog Common Electronics (ACE)
4103A	Analog Input Controller
4128A	Gain Ranging Amplifier
4132A	Analog/Digital Converter
4741A	Maintenance Panel
4952A/53A (4815A)	Analog Input Termination Cabinets
4129A	Fixed Gain Amplifier
4152A/B	Signal Conditioning
4189A	Analog Termination & Multiplexer
4813A	Reference Power Supply Package
4814A	Cold Junction Reference Package
4161A/B	Thermocouple Termination/Reference

SPECIFICATION SUMMARY

- Number of Inputs, maximum: 2048 (up to 24 inputs, 2 or 3 per channel, dedicated to internal AIS use).
- Scan Rate, maximum: Single Channel - 100 pps
  Channel Scan (N channels) - 80N pps
- Resolution: 12 bits plus sign bit (negative values in 2's complement)
- Common Mode Rejection Ratio: 10^6:1 (dc - 60 Hz - 100 ohm unbalance)
- Common Mode Voltage, maximum: 250 volts ($\pm$ dc or ac peak)
- Gain Range, Fixed Gain Amplifier: 7 manual gains (500, 250, 125, 62.5, 31.25, 15.625, 7.8125)
  Gain Ranging Amplifier: X1, X2, X4 (programmable)
- Input Resistance, minimum: Signal Levels
  $>$ 640 millivolts - 60K ohms min.
  $\leq$ 640 millivolts - 1M ohms
- Standard Errors: Signal Levels
  $\leq$ 40 millivolts - To .3% FS
  40 - 640 millivolts - To .1% FS
  .64 - 500 volts - To .2% FS

(Signal Conditioning and thermocouple reference errors not included.)

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GENERAL DESCRIPTION

The primary function of the Analog Input Subsystem (AIS) is to generate a digital representation of the magnitude and sign of various physical quantities such as temperatures, pressures, flows, etc., which have been transduced to a representative voltage, current or resistance. Conditioned analog inputs are selected, scaled, digitized and transferred under program control.

The following discussion describes the AIS and it's operation in a GE-PAC system. Fig. GEN DESC.1 is a block diagram of the AIS showing the interconnection of the various functional modules. The diagram does not show timing, sequencing or control organization. Reference is made to logic drawing 70C180050 for the 4010 system and 70C179818 for the 4020 systems.

ANALOG COMMON ELECTRONICS (ACE)

Basically, the ACE consists of an Analog Input Controller, Gain Ranging Amplifier (GRA), Analog/Digital Converter, and a Maintenance Panel. With the exception of discrete portions of the maintenance panel logic, the entire ACE is implemented with integrated circuits on PX1000 series printed wire boards which occupy one full card module (Panel W) in the Central System Unit (CSU).

Controller

The controller provides digital interfacing between the CSU (via the maintenance panel) and the rest of the AIS. It contains a holding register (H), time counter, sequence control logic, channel control logic, decode selectors, output drivers, and error detection logic. Once the controller receives a properly coded GEN-2 command and the scanner control word (SCW), it functions independently of the CSU to sequence an AIS operation and signal its status. Fig. GEN DESC.2 is a block diagram of the controller showing principal signals and functions. The function and sequencing of controller generated signals will be discussed in detail in subsequent sections.

Gain Ranging Amplifier (GRA)

The GRA functions to select one of eight channel inputs, or one of eight test voltages, amplify and isolate these inputs, and provide an output to the A/D Converter. This area of the ACE logic contains the channel multiplexer, test voltage multiplexer, a variable gain amplifier, operational amplifier, reference voltage power supply, and mode switch relay.

With the exception of the converter input select relay (COV), all multiplexing within the GRA is done with TRANSISTOR P CHANNEL ENHANCEMENT MODE MOS FET devices (Metal-Oxide-Silicon Field-Effect Transistor). In addition to the advantages of solid-state voltage switching, the MOS FET offers virtually complete isolation of input to output with bi-directional current flow.

Fig. GEN DESC.3 is a block diagram of the Gain Ranging Amplifier showing principal signals and functions. When the AIS is operated in normal mode, the controller selects the proper gain and 750 μsec later selects one of eight input channels (WMO - 7). After the proper channel has been turned on, the analog signal from the I Cabinet is amplified by the variable gain amplifier POAAMP. After 150 μsec, the output of the amplifier has settled to its required accuracy and is ready to be digitized by the A/D converter. After conversion (approximately 55 μsec), the selected channel is turned off. If two or more channels were specified in the same SCW, the next channel would be selected 10 μsec after the first channel switch was turned off.

When the AIS is operated in the test mode, the controller selects one of eight test voltages. If the selection was made from the lower order (bit-15 - 18) channel select field, the selected test voltage is routed to the variable gain amplifier. If selection was made from the upper order (bit-19 - 22) channel number field, relay K1 is energized and the selected test voltage will by-pass the amplifier and go directly to the A/D converter. The relay is energized 8.75 ms before the test channel switch is turned on.

Since the ramp generator runs continuously, test voltage channels 6 and 7 must be selected in sequence when it is desired to test the A/D converter using the ramp as an input. Test bit 23 and channel 6 (Bit 21) is selected to initialize the ramp generator, then test bit 23 and 22 (channel 7) will start conversion on the ramp. Once initialized the ramp output voltage approaches its final value -10.5V at a rate of 1 mv/5 ms.

The input lines to each channel (analog and test voltage) are clamped to $\pm$12V so that the output voltage of the multiplexer switch cannot exceed that value. The amplifier includes circuitry which will automatically change the gain if the amplifier tries to saturate as long as its input is less than $\pm$12V. Therefore, under normal operating conditions, the amplifier cannot be driven into saturation.

Analog/Digital Converter (ADC)

The ADC converts the analog voltage output of the GRA to an equivalent 12-bit plus sign digital value. The converter uses the successive approximation method of conversion, and holds the results in its C register for transfer to the CSU. Conversion time is equal to or less than 55 μsec.

The ADC includes logic which: (1) Detects positive or negative overflow conditions and generates an overflow alarm signal. (2) Generates converter busy status signal. (3) Provides a gated buffer for the C register.

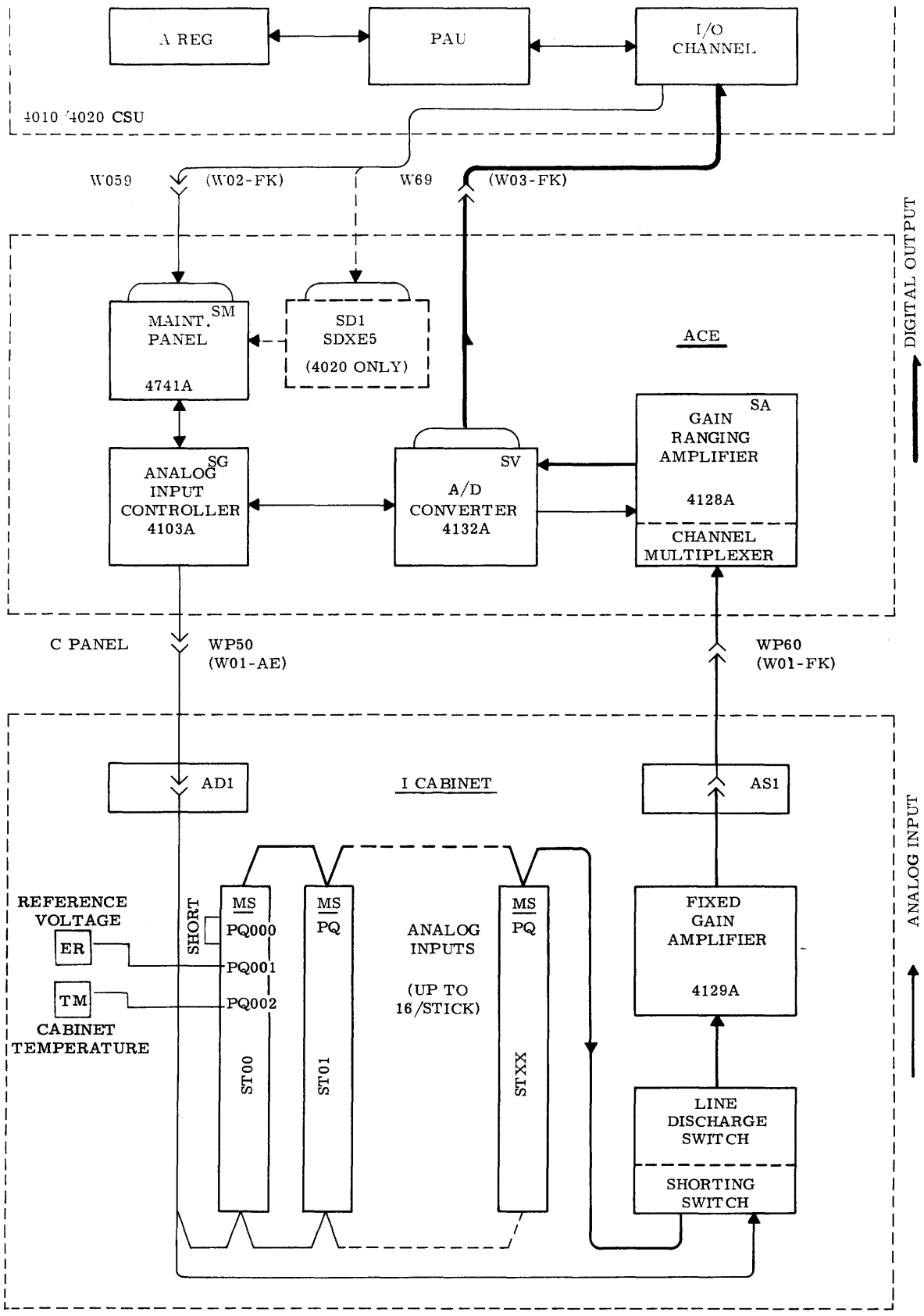


Fig. GEN DESC. 1 AIS Block Diagram

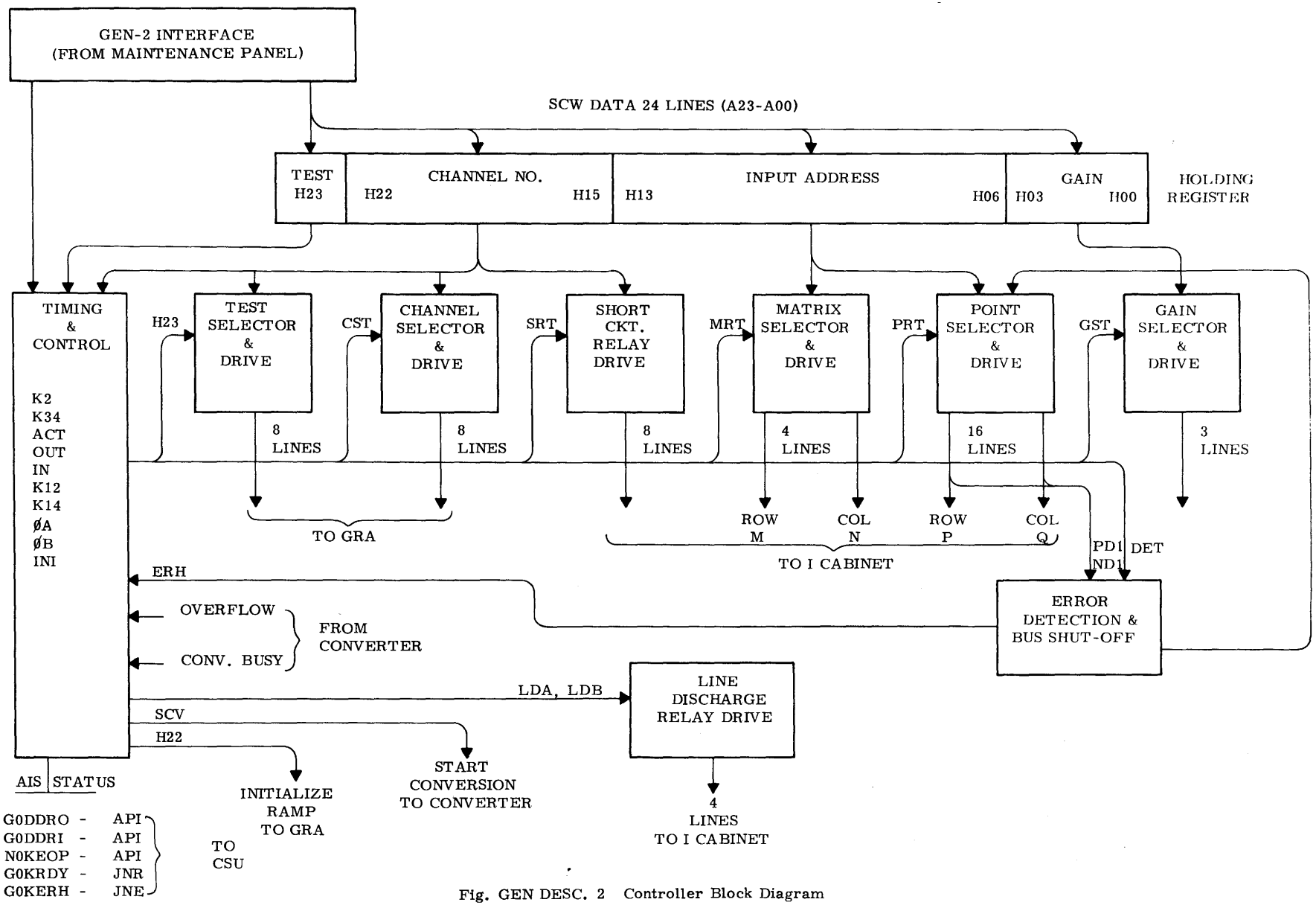


Fig. GEN DESC. 2 Controller Block Diagram

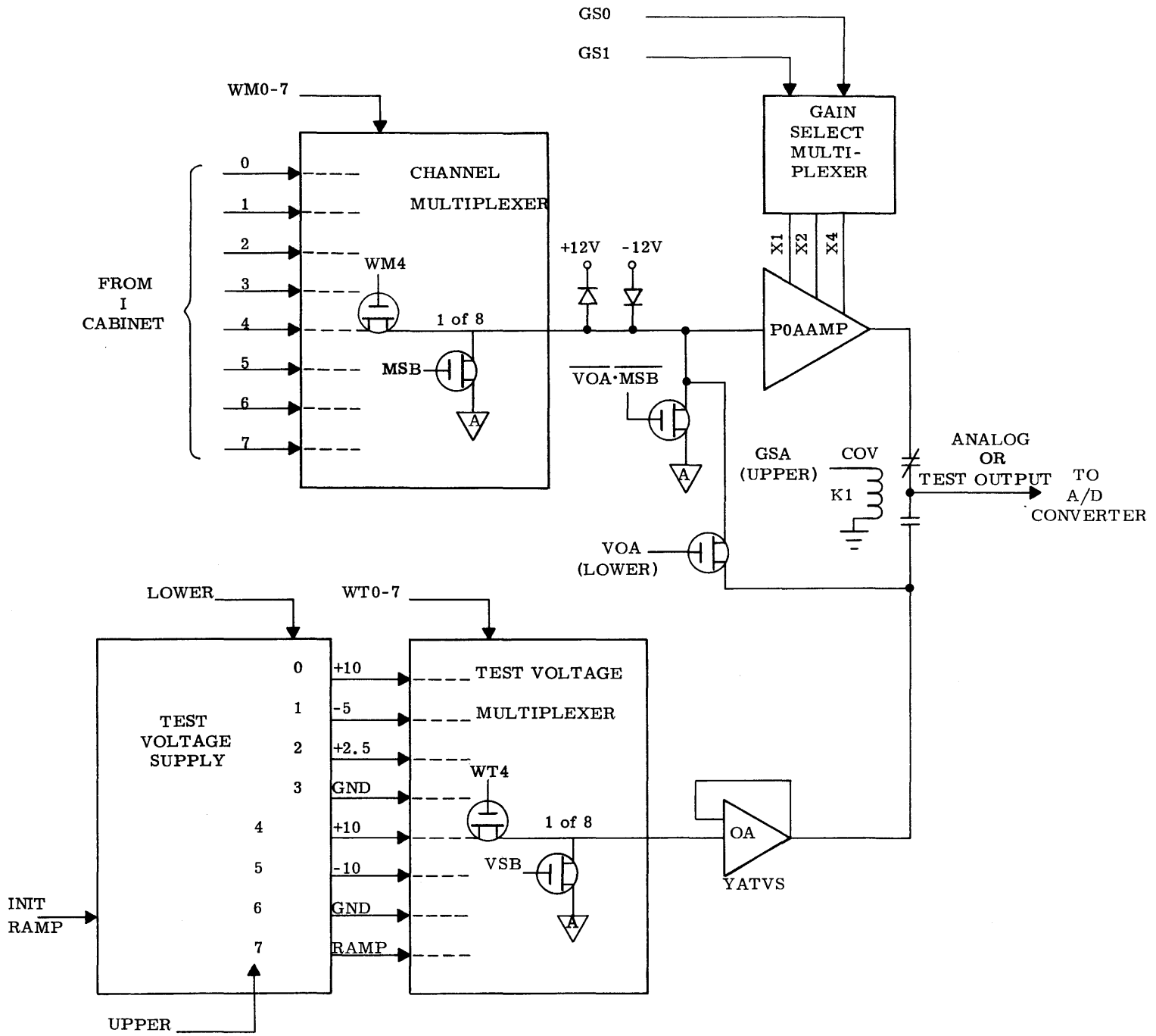


Fig. GEN DESC. 3 Gain Ranging Amplifier Block Diagram

Upon receipt of a start signal N0CSTA, the C register is cleared, converter status is set busy, and the converter asynchronously performs the conversion. During the conversion period, the "converter busy" signal is true and the data in the C register is indeterminate. At the end of conversion, the busy signal goes false and the data is stored in the C register where it remains up until the next start signal. If an overflow matrix overload condition is detected, the converter busy signal remains true for an additional 10 μsec to permit the error signal to be recognized by the controller.

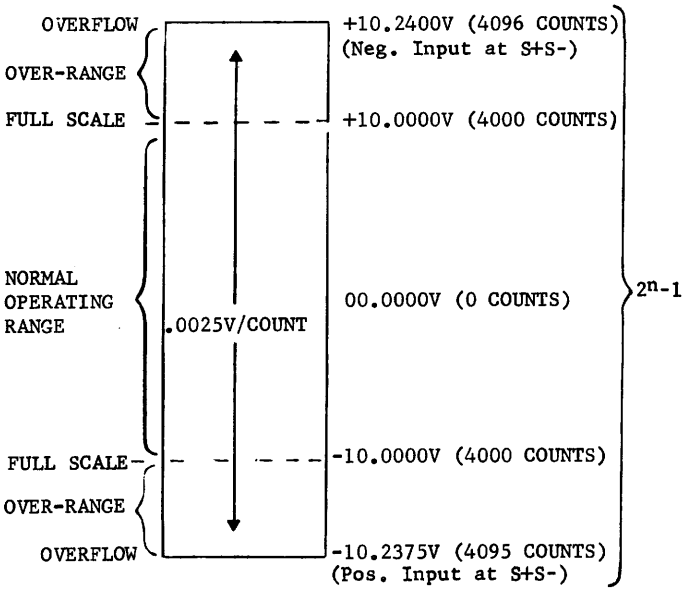
The binary coded output data is stored in the C register with 12-bits of significance plus sign (See Fig. GEN DESC, 4). With input to output signal inversion, a positive voltage on the input to the ADC is represented by the two's complement, and negative voltage on the input is represented by straight binary progression.

Input to output scaling for normal range of operation is based on:

$$\frac{FSV}{4000_{10}} \text{ or } .0025V/COUNT$$

where: FSV = full scale voltage of $\pm$10.000V

Over-range operation is possible within the limits shown on the graph since the C register may approach a count of 4096 before overflow is detected.



The error hold flip-flop will set when the input equals or exceeds the overflow voltage levels shown on the graph. If overflow occurs, the C register will not increment beyond the count at which the overload was detected.

Maximum analog input voltage without damage to the converter is $\pm$50V dc.

Maintenance Panel

The Maintenance Panel (See Fig. GEN DESC, 5) is a unique feature of the AIS which permits on or off line fault isolation and calibration by displaying selected data, enabling manual operation, and providing test points of pertinent signals.

The maintenance panel console is mounted on the card module, overlaying the SGSA1, IDDB1, and IDDC1 printed wire boards. The following switches and indicators are an integral part of the PWBs.

- ON-LINE/OFF-LINE switch. In the ON-LINE position, this manual jumper switch disables operation of the AIS from the maintenance panel. The switch is accessable by removing the panel section or by using needle nose pliers. In the OFF-LINE position, OR gates are enabled which permit GEN II simulation from the panel.
- Panel Switches S00 - S23. These 24 toggle switches are used to simulate A00 - A23 digital inputs to the AIS. Off-line switch status is read into the data holding register (H) to generate the SCW during manual operation. On-line switch status is limited to address comparison for display of conversion results on a desired point address.
- SELECT C or H display switch (S5). This switch can be used on or off line to enable the display register to select the H or C lines for display.
- CLEAR C switch (S6). This switch may be used at any time to clear the display of C register data. It has no effect on the C register.
- ADDRESS COMPARE switch (S12). This switch can be used at any time to force address comparison. In the normal position, the display register is loaded with the contents of C each time conversion is complete (DRI). In the COMP. position, the display register is loaded with the contents of C only when there is an address compare signal and DRI. The address compare signal G1AADC (logic sheet 18) goes true when the point address in the panel H REG switches agree with the address in the data holding register.
- S=1 switch (SE1). This switch is used off-line to simulate the ACT command.
- S=4 switch (SE4). This switch is used off-line to simulate the OUT command.
- S=5 switch (SE5). This switch is used off-line to simulate the IN command.

	DATA												
	M. S. B.												L. S. B.
	C14	C13	C12	C11	C10	C09	C08	C07	C06	C05	C04	C03	C02
ANALOG* INPUT VOLTAGE	SIGN												
	2's Compliment (- Count Values)												
+10.2400	1	0	0	0	0	0	0	0	0	0	0	0	0
+10.0000	1	0	0	0	0	0	1	1	0	0	0	0	0
+05.1200	1	1	0	0	0	0	0	0	0	0	0	0	0
+02.5600	1	1	1	0	0	0	0	0	0	0	0	0	0
+01.2800	1	1	1	1	0	0	0	0	0	0	0	0	0
+00.6400	1	1	1	1	1	0	0	0	0	0	0	0	0
+00.3200	1	1	1	1	1	1	0	0	0	0	0	0	0
+00.1600	1	1	1	1	1	1	1	0	0	0	0	0	0
+00.0800	1	1	1	1	1	1	1	1	0	0	0	0	0
+00.0400	1	1	1	1	1	1	1	1	1	0	0	0	0
+00.0200	1	1	1	1	1	1	1	1	1	1	0	0	0
+00.0100	1	1	1	1	1	1	1	1	1	1	1	0	0
+00.0050	1	1	1	1	1	1	1	1	1	1	1	1	0
+00.0025	1	1	1	1	1	1	1	1	1	1	1	1	1
	True Binary (+ Count Values)												
00.0000	0	0	0	0	0	0	0	0	0	0	0	0	0
-00.0025	0	0	0	0	0	0	0	0	0	0	0	0	1
-00.0050	0	0	0	0	0	0	0	0	0	0	0	1	0
-00.0100	0	0	0	0	0	0	0	0	0	0	1	0	0
-00.0200	0	0	0	0	0	0	0	0	0	1	0	0	0
-00.0400	0	0	0	0	0	0	0	0	1	0	0	0	0
-00.0800	0	0	0	0	0	0	0	1	0	0	0	0	0
-00.1600	0	0	0	0	0	0	1	0	0	0	0	0	0
-00.3200	0	0	0	0	0	1	0	0	0	0	0	0	0
-00.6400	0	0	0	0	1	0	0	0	0	0	0	0	0
-01.2800	0	0	0	1	0	0	0	0	0	0	0	0	0
-02.5600	0	0	1	0	0	0	0	0	0	0	0	0	0
-05.1200	0	1	0	0	0	0	0	0	0	0	0	0	0
-10.0000	0	1	1	1	1	1	0	1	0	0	0	0	0
-10.2375	0	1	1	1	1	1	1	1	1	1	1	1	1

* Polarity of signal going into the A/D Converter.
NOTE: This is an inversion of the signal polarity at the matrix point switch.

Fig. GEN DESC. 4 Data Coding Format, A/D Input/Output

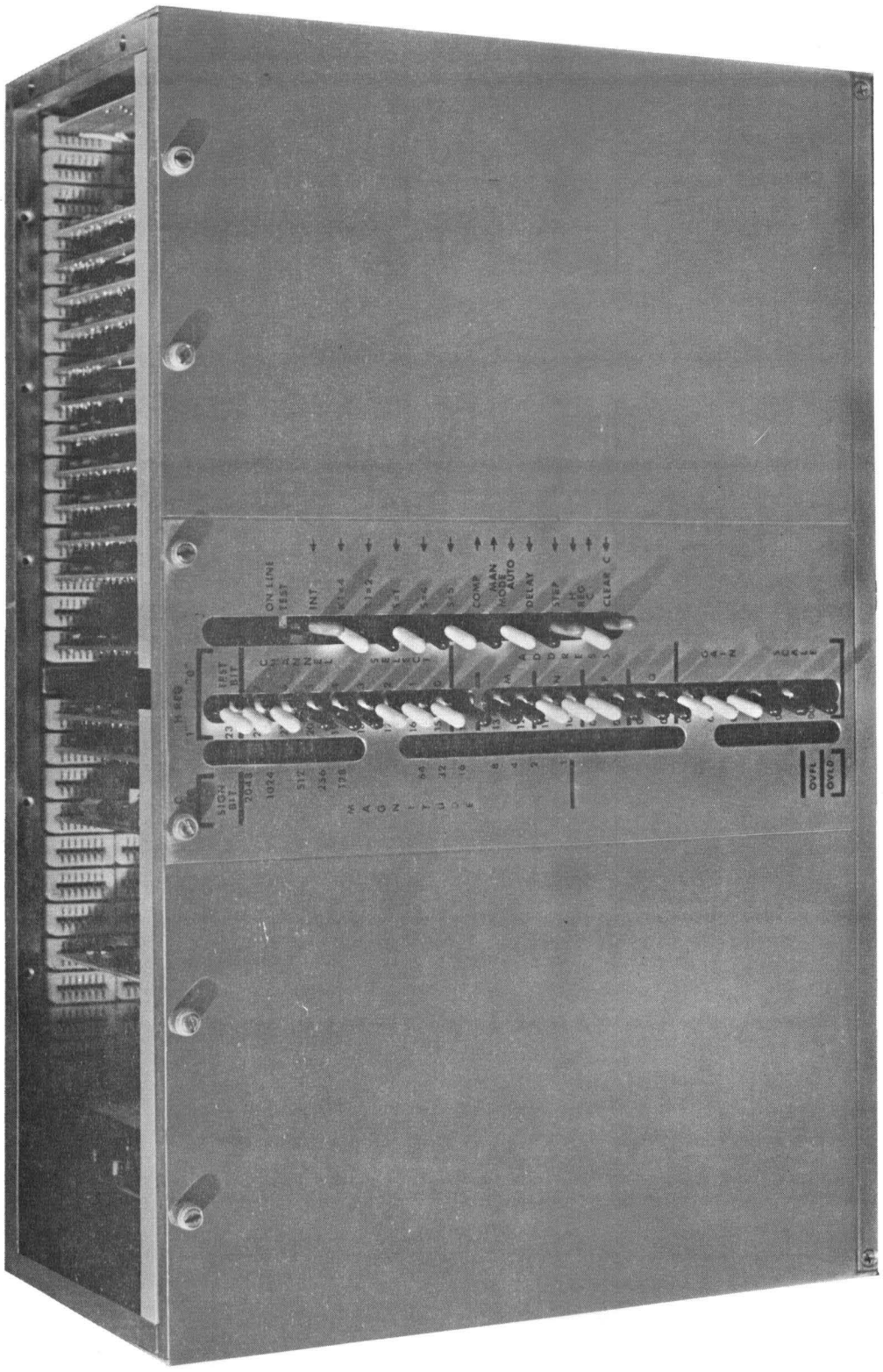


Fig. GEN DESC. 5 Maintenance Panel

- K1=2 switch (SK2). This switch is used off-line to simulate the JCB command.

- K1=4 switch (SK4). This switch is used off-line to simulate the JDR command.

- INT switch (S11). This switch is used off-line to simulate system initialize, and clear the mode and control logic.

- MODE switch (S2). This switch, as shown on sheet 24 of the logic, is used to select the desired off-line mode of operation. In the MAN position, the output of N1SCYL is held positive so that G0SSCYL is enabled when the STEP switch is operated (see STEP switch). Also, the positive voltage from S3 (AUTO) will allow the step 2 flip-flop F1SST2 to reset and inhibit G0SSCY after completion of a single cycle.

  In the AUTO position, the output of N1SATO is held positive so that G0SCYL is enabled each time that the ready signal G1SRDY goes true. Since F1SST2 cannot reset, the selected operation will cycle continuously at maximum rate.

- DELAY switch (S3). This switch is used off-line and with the MODE switch in AUTO to enable N1SDLY. This makes the enabling of G0SCYL dependent upon the status of the time delay cycle flip-flop F1STDC. The time delay element CKT1 prevents F1STDC from clearing until 750 msec after end of cycle.

- STEP switch (S4). This switch is used off-line to initiate a selected operation in either AUTO or MAN mode. When the switch is closed and STEP is executed, F1SST1 will set. The next clock will set F1SST2. As the switch is released, F1SST1 will reset, enabling G0SSCY to set F1SCYL and enable the time counter. If the mode switch was in MAN, the next clock would reset F1SST2 allowing the operation to end after generation of the phase A, B signals.

- Display Register Lamps (I00 - I23). The 24 register display lamps operate at any time to display either the contents of the H register or the contents of the C register. Selection is made by operating the Select C or H display switch. Maintenance panel operation is discussed in detail in subsequent sections.

ANALOG INPUT TERMINATION CABINET (I CABINET)

The I Cabinet contains the relay multiplexer, signal conditioning, stick support and cable termination hardware, the fixed gain amplifier and line discharge/shorting circuits (See Fig. GEN DESC.6).

Cabinet arrangement and stick layout depends on the number of channels per system. Fig. GEN DESC.1 illustrates a single channel per cabinet arrangement which enables a maximum of 256 addressable points per channel with up to eight cabinets per AIS (2048 points maximum). An optional arrangement permits four channels per cabinet (64 points per channel) with a maximum of two cabinets per AIS (512 points maximum). In each case, 2 or 3 addressable points are reserved for the following system functions:

00 ⟶ OFFSET, S.C.

01 ⟶ F.V. TEST VOLTAGE POINT

02 ⟶ CABINET TEMPERATURE (optional)

Relay Multiplexer

The relay multiplexer, commonly called the scanner, provides selective switching, signal conditioning and termination for the analog input signal lines. Mercury-wetted relays are used to implement the switching function. Relay selection is organized as illustrated in Fig. GEN DESC.7.

Multiplexer sequencing is such that the matrix switch (MS) is selected first: It's N drive (column or vertical) and M drive (row or horizontal) lines are decoded to select one of up to 16 sticks (vertical relay mounting hardware) in each channel. Next, the line discharge switch A contacts followed by the B contacts are dropped out, ungrounding the signal lines.

Now, point switch selection is made: It's Q drive (column or vertical) and P drive (row or horizontal) lines are decoded to select one of up to 16 points on the selected stick for all channels in the system. Finally, the shorting switch is energized, removing the short circuit and switching the selected analog input to the fixed gain amplifier.

The output of the amplifier is routed via TRIAX cable to the analog channel multiplexer in the ACE module. Channel selection is discussed elsewhere in this document. Standard stick layout and drive distribution is shown in drawing 70C180120 single channel, or 70C180562 4-channel logic.

Signal Conditioning

Each input termination point accomodates a plug-in signal conditioning circuit which filters and/or attenuates the input signal to a form suitable for application to the fixed gain amplifier in the channel for which it is a member.

Where inputs are derived from slidewires (potentiometers) or resistance/temperature devices (RTDs), the I cabinet includes the optional 4813 power supply. Where the input signal is an analog current or resistance, the signal conditioning circuit converts the signal to a voltage which is within the selected full

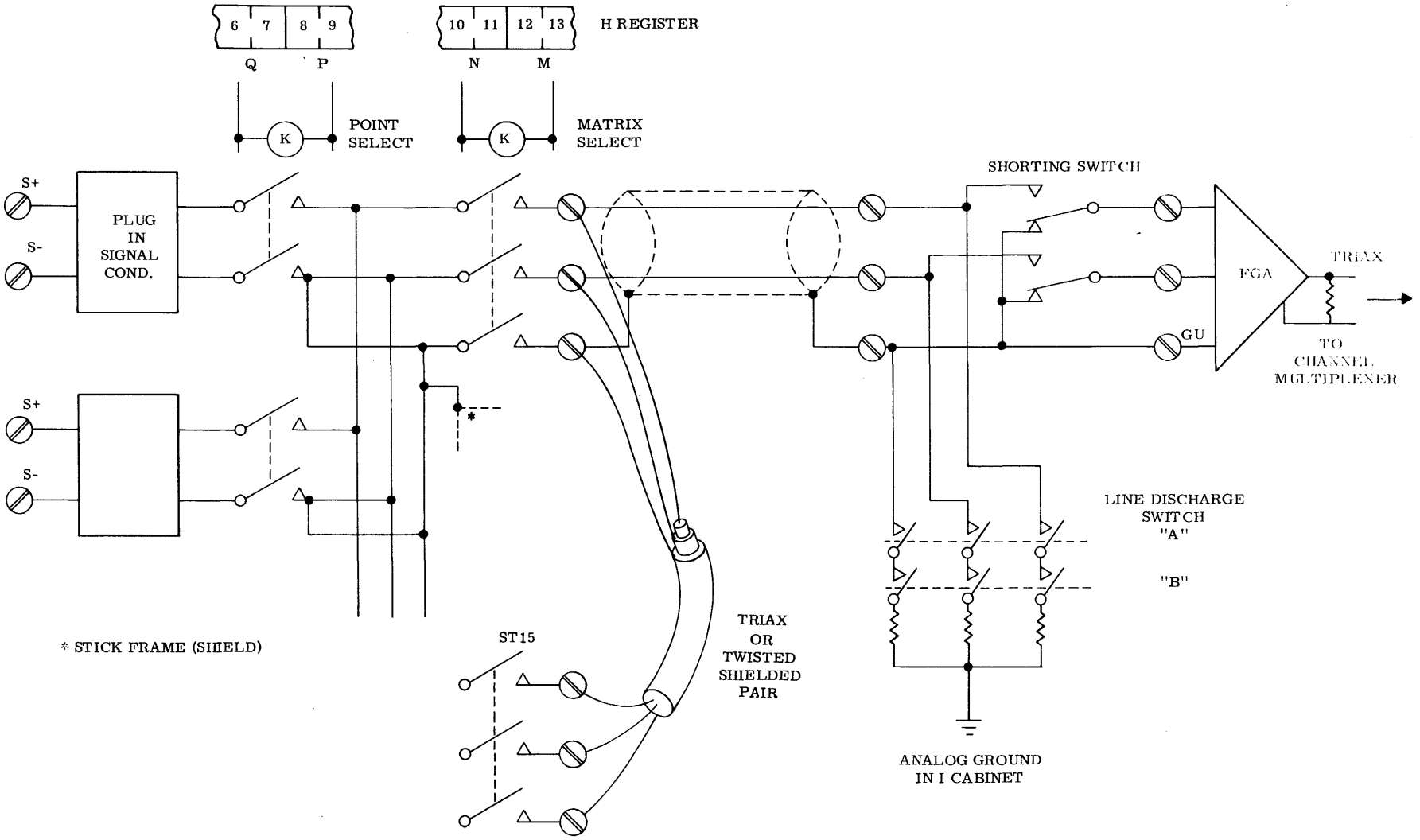


Fig. GEN DESC. 6 Termination (I) Cabinet Schematic (Single Channel)

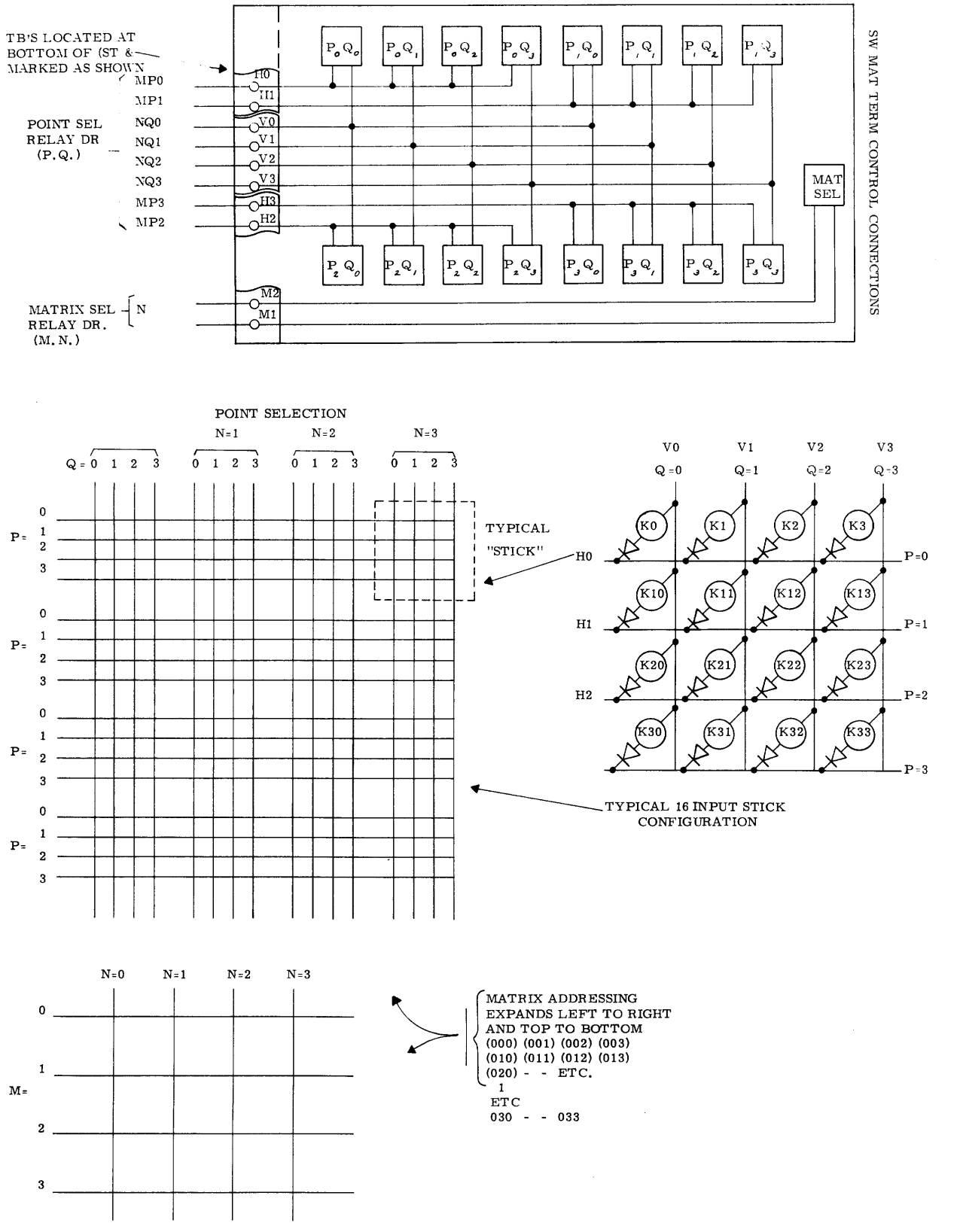


Fig. GEN DESC. 7 Relay Multiplexer Termination Control

scale gain option of the amplifier. The AIS will accept the following standard range of inputs:

- Voltages with full scale values as low as ±10 millivolts and as high as ±500 volts.
- Currents ranging from 1 to 5 ma, 4 to 20 ma, or 10 to 50 ma.
- Thermocouple signals from all common types. A cold junction reference is provided.

Fixed Gain Amplifier (FGA)

The FGA is a passive-guard differential amplifier which provides the function of signal isolation and scale changing. Full scale output is ±10 volts and ±100 milliamps. A front panel gain selector switch permits manual selection of up to seven gain positions: 500, 250, 125, 62.5, 31.25, 15.625, 7.8125.

Summary of specifications:

- Settling time - 1700 microseconds
- Gain Linearity - ±.01%
- Maximum common mode voltage - ±250 volts DC or AC peak
- Power Requirements - 105 to 125V 50 to 400 Hz 10 watts

For detailed information, refer to Maintenance Manual, Section 6.

Thermocouple Reference

Systems having remote thermocouple sensors as analog inputs require that all thermocouple (TC) extension leads be terminated at a reference junction which is at a known temperature. Since standard TC curves are based on a reference junction temperature of 32°F, the temperature of the immediate area at which the TC leads are terminated (in the AIS) is monitored in order to calculate the final volt/temperature relationship. Two optional thermocouple referencing methods are discussed:

Standard Precision

This method uses the I Cabinet input point terminals as the thermocouple wire-to-copper-wire junction. Reference junction error for class A environment is ±1/2°C nominal and ±2°C worst case.

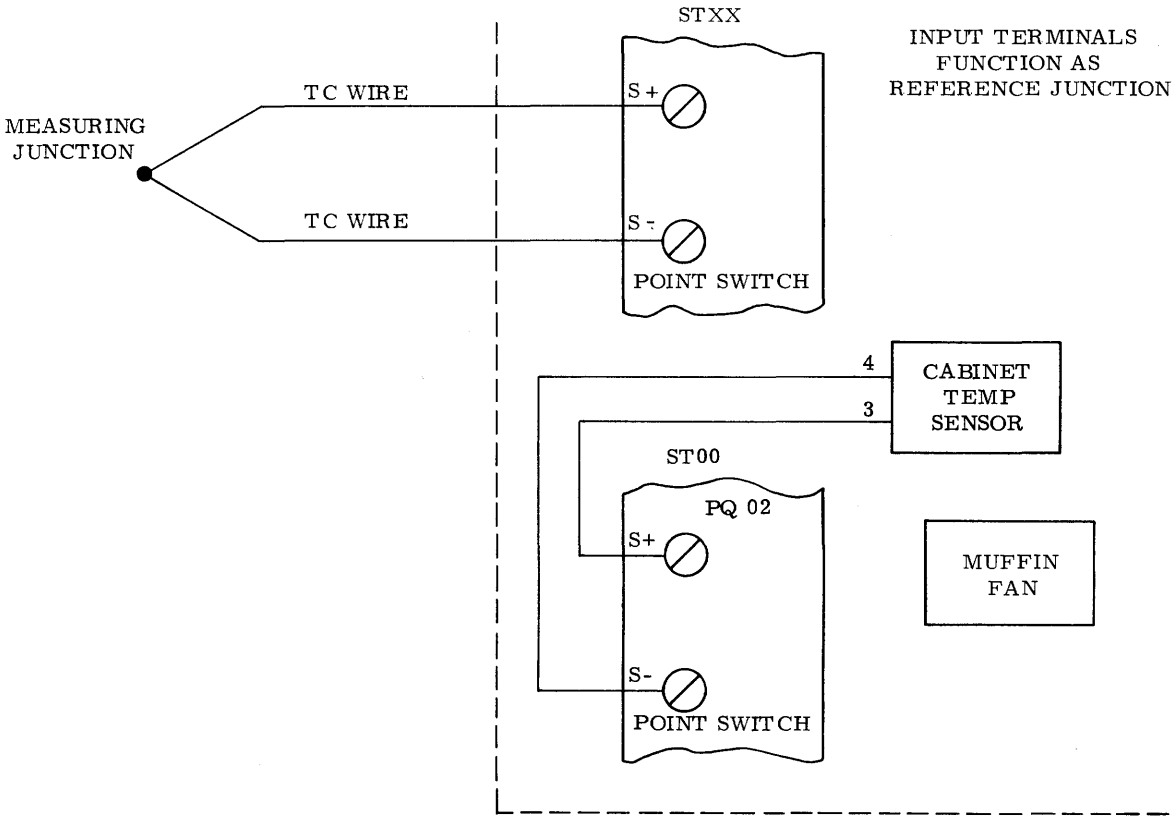
The standard precision thermocouple package as called for in the Analog Input Cabinet Model List consists of a fan for circulating internal cabinet air and an RTD bridge for measuring cabinet air temperature. The user may terminate any type of thermocouple to any standard "EMF" point in the cabinet.

The output of the RTD bridge is read as an EMF input and is used by the computer program to compensate for the difference between actual reference temperature and the reference temperature constants for each type of thermocouple in the system. The bridge is calibrated at the factory to provide an output of 0 mv ±0.001 mv at 0°C and 48.82 mv ±0.10 mv at 50°C. Fig. GEN DESC.8 illustrates a typical standard precision TC circuit.

High Precision

This method uses an enclosed input termination panel (heat sink) where thermocouple-wire-to-copper-wire reference junctions for up to 64 inputs is accomplished at the approximate same temperature. Reference junctions error for class A environment is 0.2°C nominal, 1/2°C worst case.

The high precision thermocouple reference package 4161A consists of an enclosure suitable for wall mounting, a fan, RTD bridge, and input termination panel. The enclosure may be located anywhere between the process and the computer system. The fan keeps air circulating continuously over the panel (heat sink) and within the enclosure. The RTD bridge monitors the temperature of the termination panel and provides an EMF input in the same manner as described for the Standard Precision. Fig. GEN DESC.9 illustrates a typical high precision TC circuit.



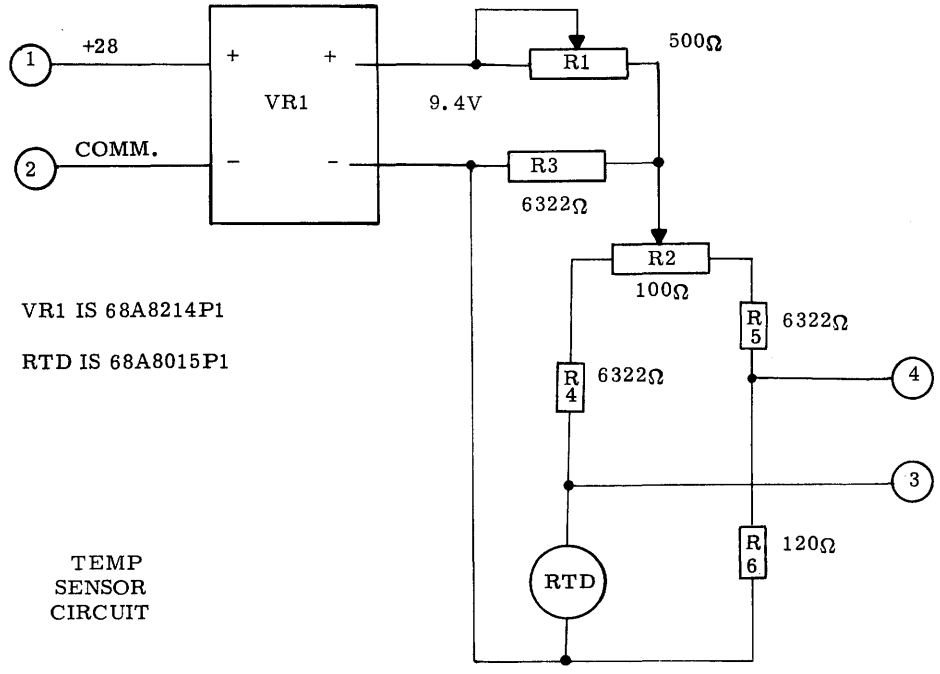


Fig. GEN DESC. 8 Standard Precision TC Reference

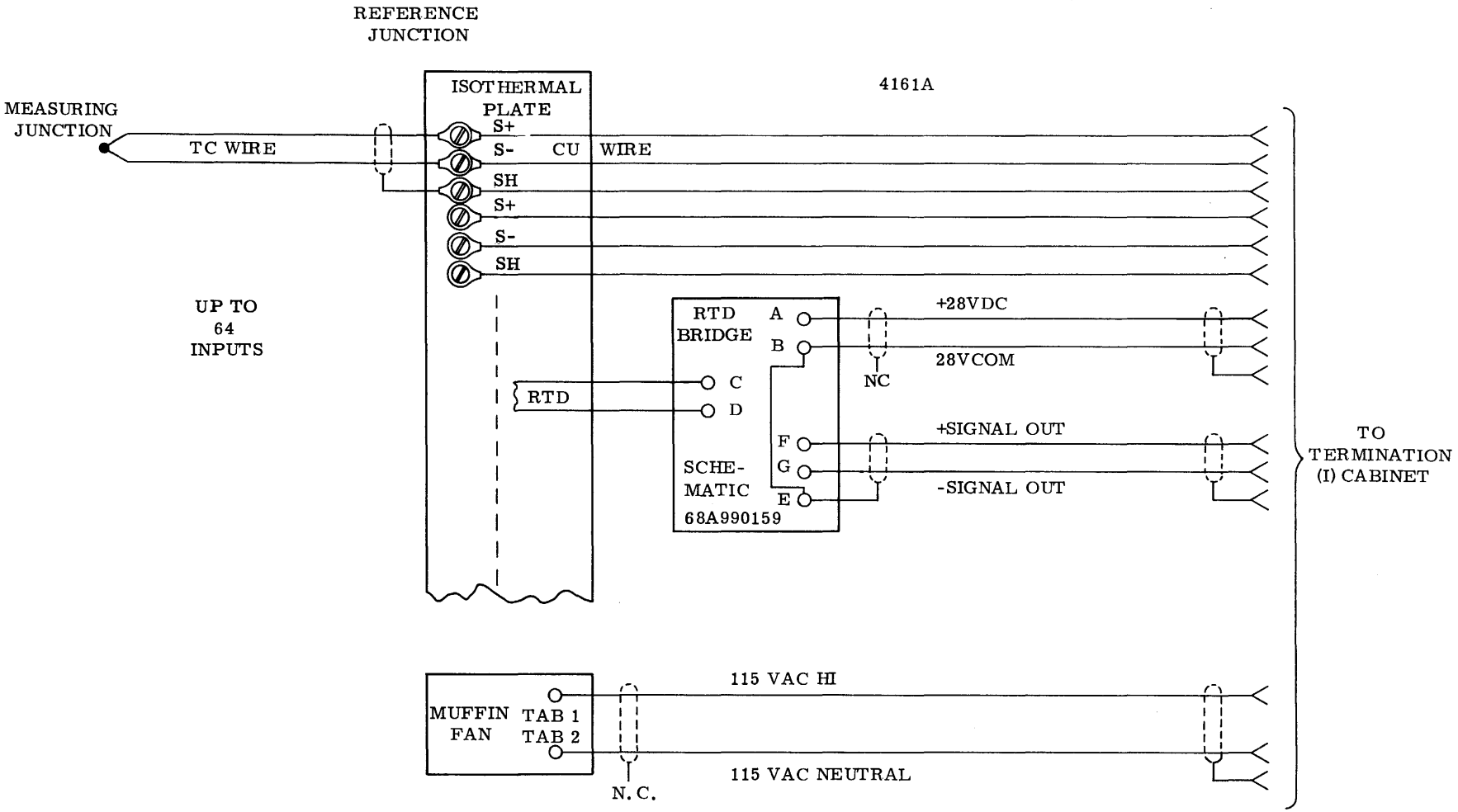


Fig. GEN DESC. 9 High Precision TC Reference

OPERATION

The basic GEN-2 instructions, OUT, IN, ACT, JCB, and JDR are used to control the AIS. Upon receipt of an OUT command, a scanner command word (see Fig. OP. 1) is transferred from the computer, via the maintenance panel to a holding register in the controller. The controller decodes the SCW and causes an analog signal at the specified point address to be selected; the specified gain range amplifier scale to be selected; and initiate a conversion on the specified channel input. At the conclusion of the conversion, the digitized data is held in the converter C register and a signal is generated (G0DDRI) to notify the computer that input data is ready.

The computer normally responds to the data ready input API with an IN command which transfers the contents of the C register and advances the channel selector. If no additional channels are specified for conversion, an end of operation signal (N0KEOP) is generated indicating the completion of the total operation specified in the SCW. If additional channels were specified, the controller causes the next sequential channel to be selected and converted. The DRI signal is generated for each new conversion and the computer responds with an IN command for each data transfer.

The controller responds to the ACT command by causing the data ready input API to go not ready and back to ready. If the conversion is not ready, the ACT command is ignored.

Three API lines and two Jump lines are available to the CSU to determine the status of the AIS and enable program control.

The API lines are:

- Data Ready Output (G0DDRO) - This signal goes true (0V) indicating end of operation, on line, and no errors. The computer may use this interrupt for the TOM function. A program entry always starts with the OUT instruction.

- Data Ready Input (G0DDRI) - This signal goes true (0V) when the converter goes not busy indicating that data in the C register is ready for transfer. The computer may use this interrupt for the TIM function. Data Ready Input is reset by subsequent IN instructions. After the last channel is converted and inputted, the input ready interrupt will remain reset (+3.6V). This interrupt may be activated with the ACT instruction prior to the End Of Operation after which it has no effect.

- End Of Operation (N0KEOP) - This signal goes true (0V) after the last channel specified in the SCW is serviced. The program may use this interrupt as an echo to modify the TOM function.

The Jump Lines are:

- Ready (G0KRDY) - This test line may be activated with the JNR, JDR, or JCB instrutions at any time to check the ready or busy status of the AIS. A busy or not ready signal (+3.6V) indicates that data is not ready for transfer, an operation is in progress, or an error has occurred. The ready line will go busy immediately following an OUT and remain busy until Data Ready Input or End Of Operation go true.

  A JDR instruction addressed to the AIS will enable the Ready line and execute a jump if Data Ready Input is true (set). A JCB will enable the Ready line and execute a jump if End Of Operation is false (reset).

- Error Hold (G0KERH) - This test line may be sampled with the JNE instruction at any time to check the error status of the AIS. If the error hold flip-flop is set by either a scanner overload or converter overflow, the error line goes true, the JNR Ready line goes busy, and the Data Ready Output API is inhibited.

  The error hold flip-flop may be cleared by system initialize or by executing another OUT instruction.

OUT COMMAND

Upon receipt of an OUT command, the AIS operates independently of the computer to:

A. Select one of 16 sticks or relay matrices as specified in SCW-10 - 13 and start matrix relay timing MRT (see Fig. OP. 2).

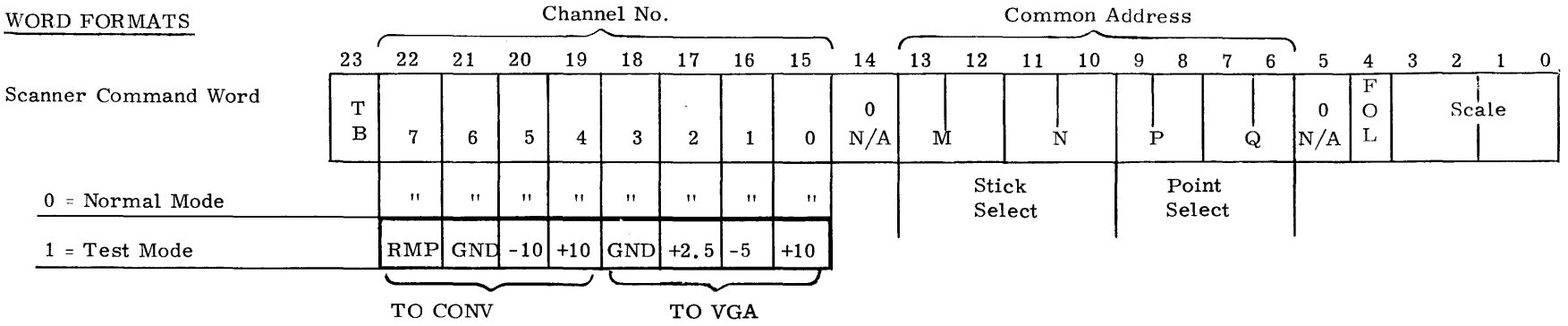
B. Start line discharge "A" timing LDA. This will arm the line discharge switch by closing the A contacts (see Fig. OP. 3).

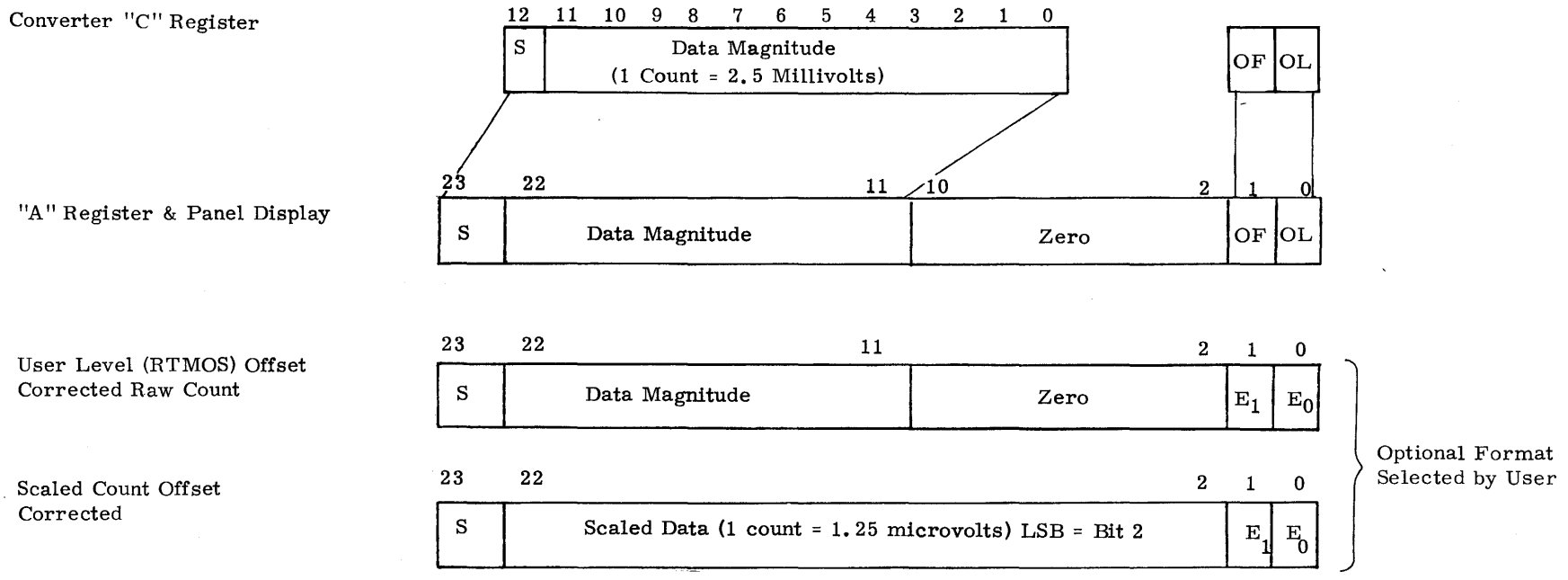
C. Start line discharge "B" timing LDB. This will close the B contacts and line discharge will occur during this interval.

D. End LDA to drop out line discharge A contacts.

1100A ANALOG INPUT SUBSYSTEM

WORD FORMATS



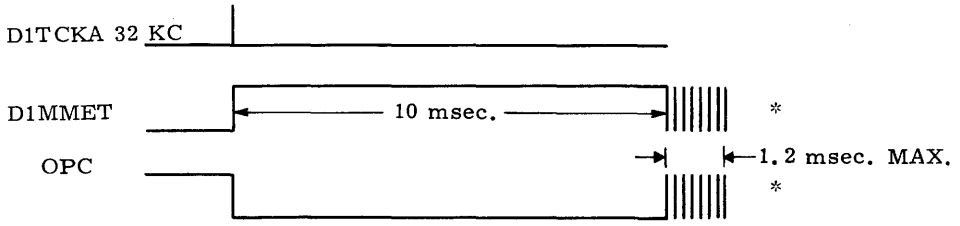


E_1 E_0
- 00 Data Valid
- 01 Data Marginal (Marginal Reference)
- 10 Data Bad (OF)
- 11 Data Bad (Sat. OF or OL or bad reference value)

TB Test Bit
FOL Force Overload
Scale 0000 x 4
0001 x 2
0010 x 1

S Sign
OF Overflow
OL Overload
N/A Spare (Not Used)
Negative data in two's complement form.

Fig. OP.1 Word Formats



* RESET BY END OF OPERATION WHICH VARIES WITH NUMBER OF CHANNELS SCANNED.

150 μsec PER CHANNEL.

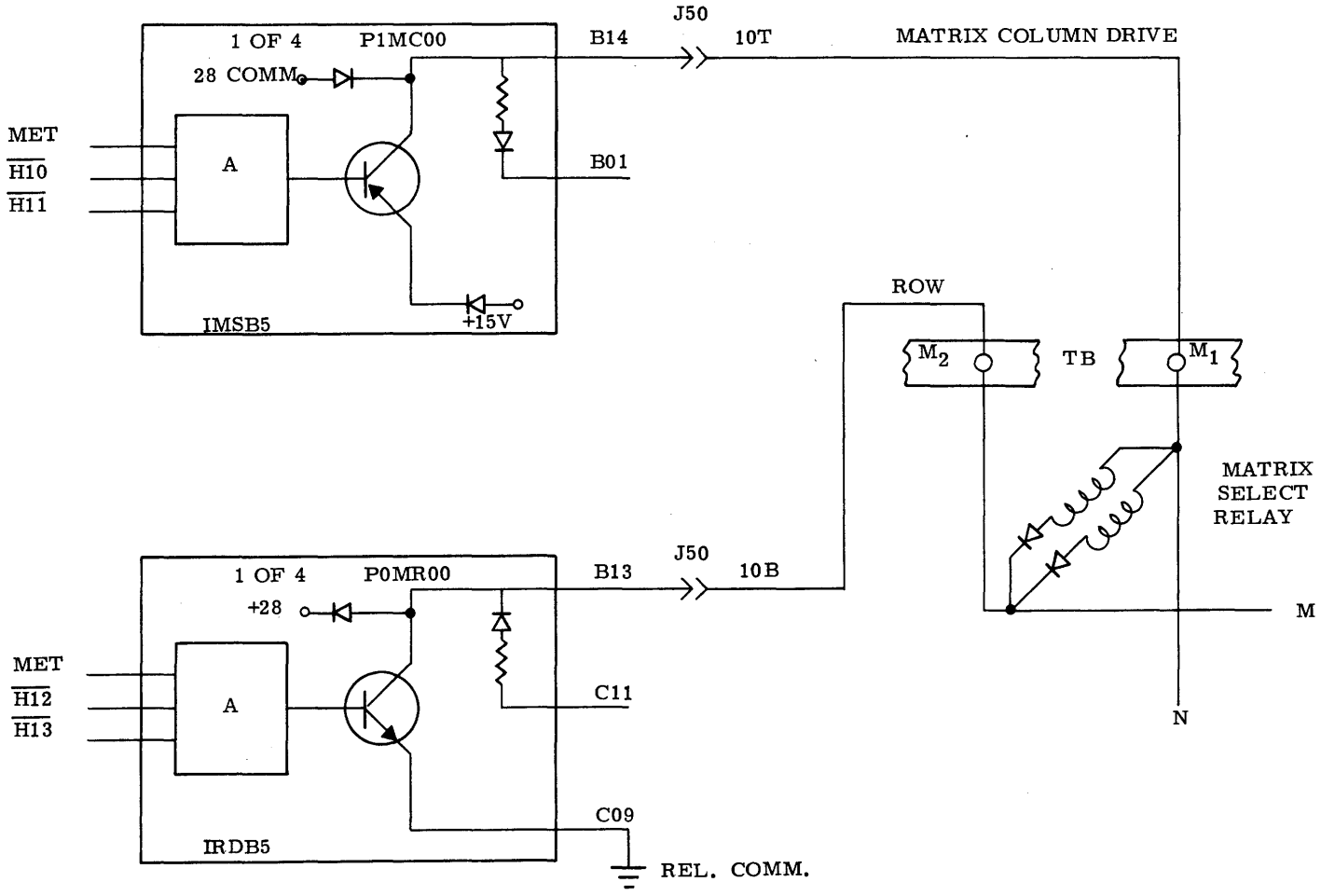


Fig. OP. 2 MATRIX Relay Drive and Timing

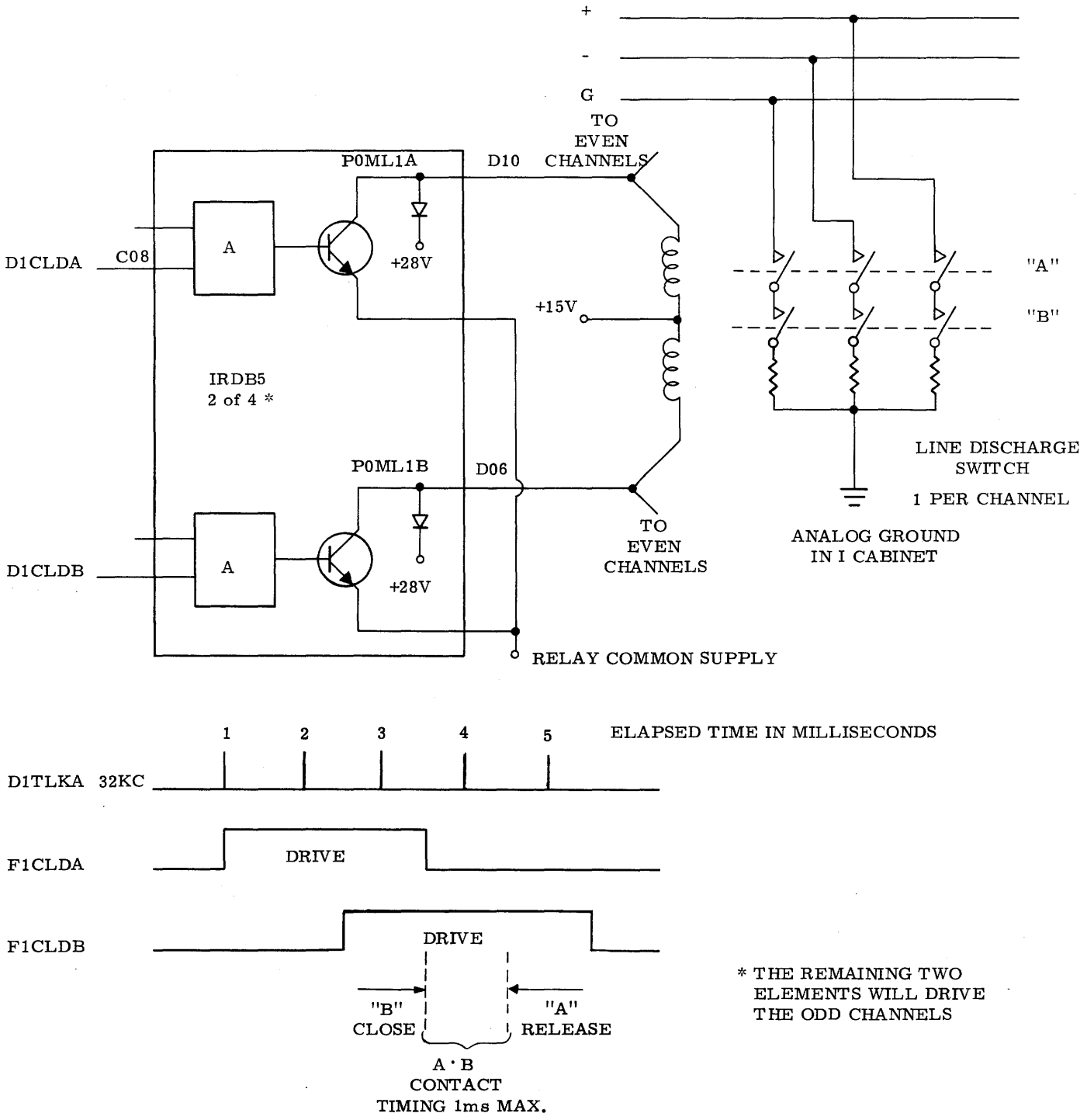


Fig. OP. 3 Line Discharge Timing and Drive

E. Select one of 16 points from the selected stick as specified in SCW-6 - 9 and start point relay timing PRT.

F. End LDB to drop out line discharge B contacts.

G. Start short circuit relay timing SRT. This will drop out the shorting switch so that the analog signal on the selected point now appears on the input of the fixed gain amplifier.

H. Select one of three gain ranges as specified in SCW-0 & 1 and start gain select timing GST.

I. Select the first of up to seven channels as specified in SCW-15 - 22 and start channel select timing CST. If SCW-23 (test bit) was set, the first test signal will be selected.

J. Start conversion SCV.

The following is a list of logical events which take place during Phase A of the OUT Command. The signal name which directly initiates the action is shown in brackets [ ], followed by the logic page number. Sequencing and timing is related to the timing chart in the logic drawing and Fig. OP.4.

- Gate SCW to Data Holding Register [D0CLDH] 45
- Clear End Of Operation flip-flop F1KEOP [D0CLDH] 42
- Clear Data Ready Input flip-flop F1KDRI [G1KRRI] 42
- Clear Channel Switch Drop flip-flop F1KDRP [D0TIC1] 44
- Clear Channel Control Shift Register F1KSR0 - SR7 [D0TIC1] 41
- Set Disable Time Counter flip-flop F1TDTC [D0TIC1] 35
- Clear Timing Counter flip-flops F1TB00 - B08 [D0TIC2] 37, 38
- Clear Frequency Divider flip-flops F1TT00 - T05 [G1TINC] 36
- Clear Point Relay Timing flip-flop F1CPRT [N0CIN1] 39
- Clear Short Relay Timing flip-flop F1CSRT [N0CIN1] 39
- Clear Line Discharge B Timing flip-flop F1CLDB [N0CIN1] 39
- Clear Line Discharge A Timing flip-flop F1CLDA [N0CIN2] 40
- Clear Martix Relay Timing flip-flop F1CMRT [N0CIN2] 40
- Clear Gain Relay Timing flip-flop F1CGST [N0CIN2] 40
- Clear Overload flip-flop F1EOLD [G1EOLD] 59
- Clear Channel Select Timing flip-flop F1ECST [N0EINT] 59
- Clear Error Hold flip-flop F1EERH [G0EREH] 59

The following is a list of logical events which take place during and after Phase B of the OUT Command. Sequencing and timing is related to the timing chart in the logic drawing and Fig. OP.4.

- Enable Start Sequencing gate G0CSTS [G1CKPB] 39
- Clear Disable Time Counter flip-flop F1TDTC [G0CSTS] 35
- Enable Timing Pulses GOTCK2 [N1TETP] 35
- Preset Channel Control 0 flip-flop F1KSR0 [N1KPSR] 41
- Set F1CMRT, enables matrix drive [D1TCKA] 40
- Set F1CLDA, enables line discharge drive A [D1TCKA] 40
- Set F1CLDB, enables line discharge drive B [D1TB02] 39 (2.5 ms after ETP)
- Clear F1CLDA, disable line discharge drive A [D1TB04] 40 (3.5 ms after ETP)
- Set F1CPRT, enable point select drive [F1TB07] 39 (4 ms after ETP)
- Clear F1CLDB, disable line discharge drive B [F1TB04] 39 (5.5 ms after ETP)
- Set F1CSRT, disable short circuit drive [F1TB04] 39 (6.75 ms after ETP)
- Set F1CGST, enable gain select drive [F1TB08] 40 (8 ms after ETP)
- Set F1ECST, enable channel select timing [N1ESCT] 59 (8.75 ms after ETP)

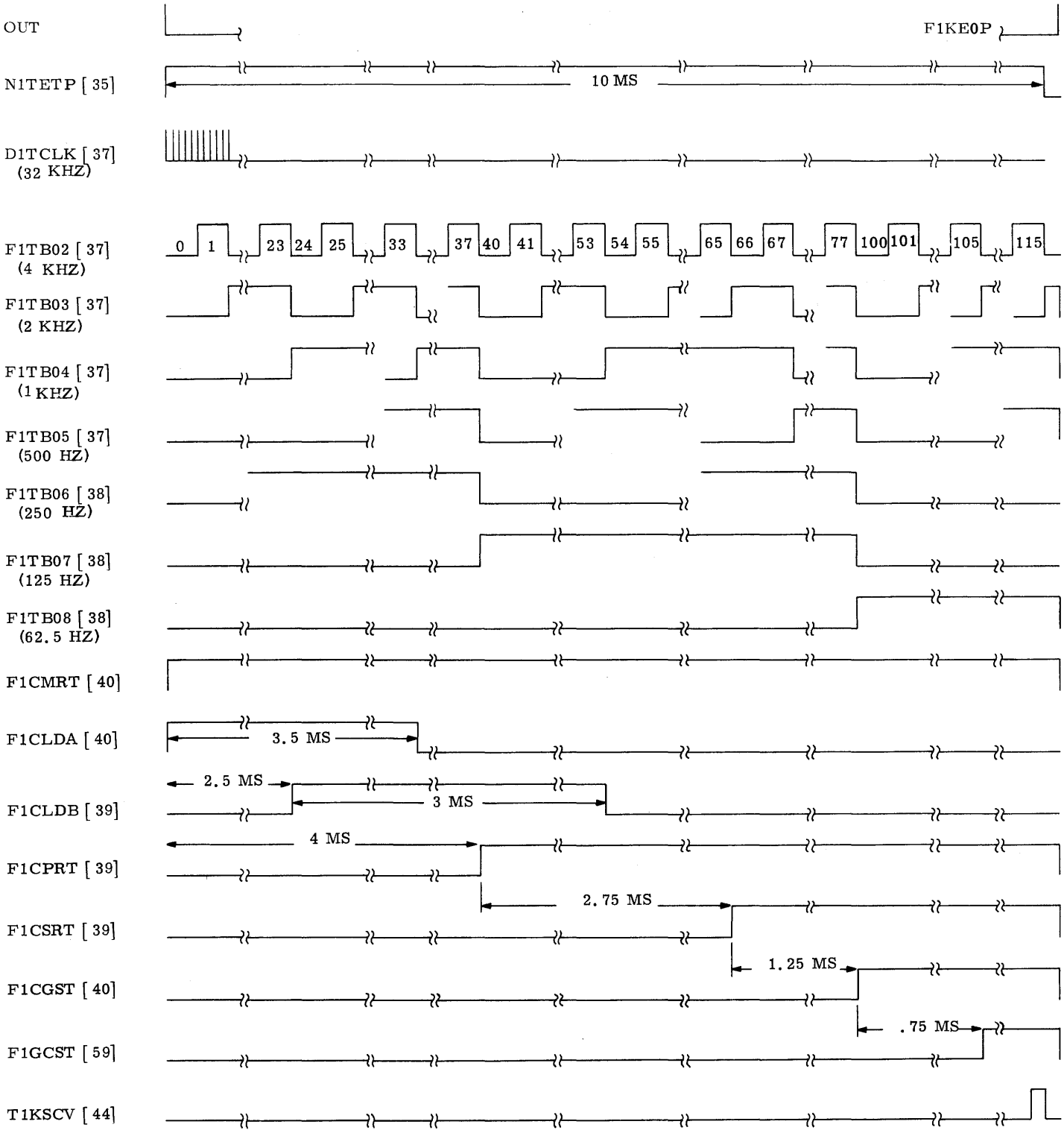


Fig. OP.4 Sequence Control Timing

- Start Analog Conversion G0KSTA enabled [T1KSCV] 44 (9.75 ms after ETP).

IN COMMAND

The IN Command is executed in response to a Data Ready Input interrupt. The address bits (K32) gate the contents of the A/D Converter C register to the computer A register. The S bits (S05), during Phase A will advance the channel control (D1KADV) and set the channel drop flip-flop which inhibits further channel selection.

During Phase B, S05 clears the data ready input flip-flop. If another channel was specified in the SCW, an enable pulse G1KENP is generated which enables channel selection and starts another conversion. When the converter goes not busy, the data ready input flip-flop is set and another interrupt is enabled. The IN cycle repeats until the last channel is searched. At this time End Of Operation flip-flop is set and the AIS goes not busy.

CHANNEL CONTROL

The OUT command will always clear the channel control shift register (F1KSR0 - SR7) and then set the channel 0 flip-flop so that the channel control enable gates G0KEN1 - EN2 must look at channel 0 first. If channel 0 was selected (SCW bit 15 set), an enable pulse G1KENP will start conversion on that channel and inhibit the step channel trigger T1KSTC from advancing the shift register. If channel 7 only were selected then a series of 100 NSEC pulses (T1KSTC) would be enabled to advance the shift register until F1KSR7 is set. At this time ENP will inhibit the STC pulse and start a conversion on channel 7.

SEQUENCE TIMING

The basic timing signals used to sequence the ACE are derived from the crystal controlled, 5.760 MHz (1.75 ns), clock generator shown on sheet 35 of the logic. The free-running generator output is divided by four to supply the 1.44 MHz (350 ns), F1TCK2 clock which is used to sequence maintenance panel operation and when enabled by N1TETP drives the frequency divider shown on sheet 36 of the logic.

During N1TETP, the frequency divider operates on the 45th submultiple of F1TCK2 to furnish the 32 KHz (31 us), D1TCLK clock which is used to drive the binary timing counter B1TB00 - 08. The outputs of F1TB02 - 08 are used to sequence all events which occur during the first ten milliseconds following the execution of an OUT command (See Fig. OP.4).

The enable timing pulse gate N1TETP is enabled when the start sequence, G0CSTS, signal clears the disable time flip-flop F1TDTC. Sequence start is generated during phase B of the OUT command. When the binary time counter holds 115_8, sequencing is terminated. This count will set F1TDTC, disable N1TETP and inhibit the D1TCLK clock. However, the binary counter and frequency divider are not reset until F1KEOP sets, signaling the end of operation.

ERROR DETECTION

Error detection circuits within the AIS controller will react to two error conditions: Overload (OL) and Overflow (OF). Either error will disable the Ready test line and enable the Error test line. Both error status bits are transferred to the A register for display, as well as, to the maintenance panel C register display. The error detection circuits, ready line, and error line are reset by system initialize or by executing the next OUT command. Fig. OP-5 shows a simplified schematic of the error detection scheme.

Overload: An overload will occur if more than one row (horizontal) or column (vertical) point drive line within the same matrix (stick) is energized during a scan cycle. This possibility of picking up two point relays on the same stick is sensed and prevented by the error detection and matrix disable circuits shown on sheet 59 of the logic. Also shown on sheet 59 is a +28 V power detector which sets the overload anytime (without N1PDET) the 28 V relay or peripheral power supply is interrupted. This circuit prevents point relays on a selected matrix from energizing, should the downed supply provide a circuit path to ground.

Overload detection N1PDET is enabled 250 μsec after point relay timing (PRT) is enabled which is sufficient time to abort the cycle before any relays can operate. A positive overload Y1EPOL is enabled when more than one matrix switch driver element is turned on. A negative overload Y1ENOL is enabled when more than one relay driver element is turned on. A test overload will occur anytime an OUT command is executed with SCW-4 set.

When a positive or negative overload, test overload, or +28 V failure is detected, both the overload F1EOLD and error hold F1EERH flip-flops will set. F1EOLD will initiate the following:

- Inhibit bus shut off driver P0EBSO which opens the 15V relay common supply to the point select drive lines.
- Inhibit amplifier shorting switch control G1SMSC. This prevents any fixed gain amplifier from being unshorted during SRT.

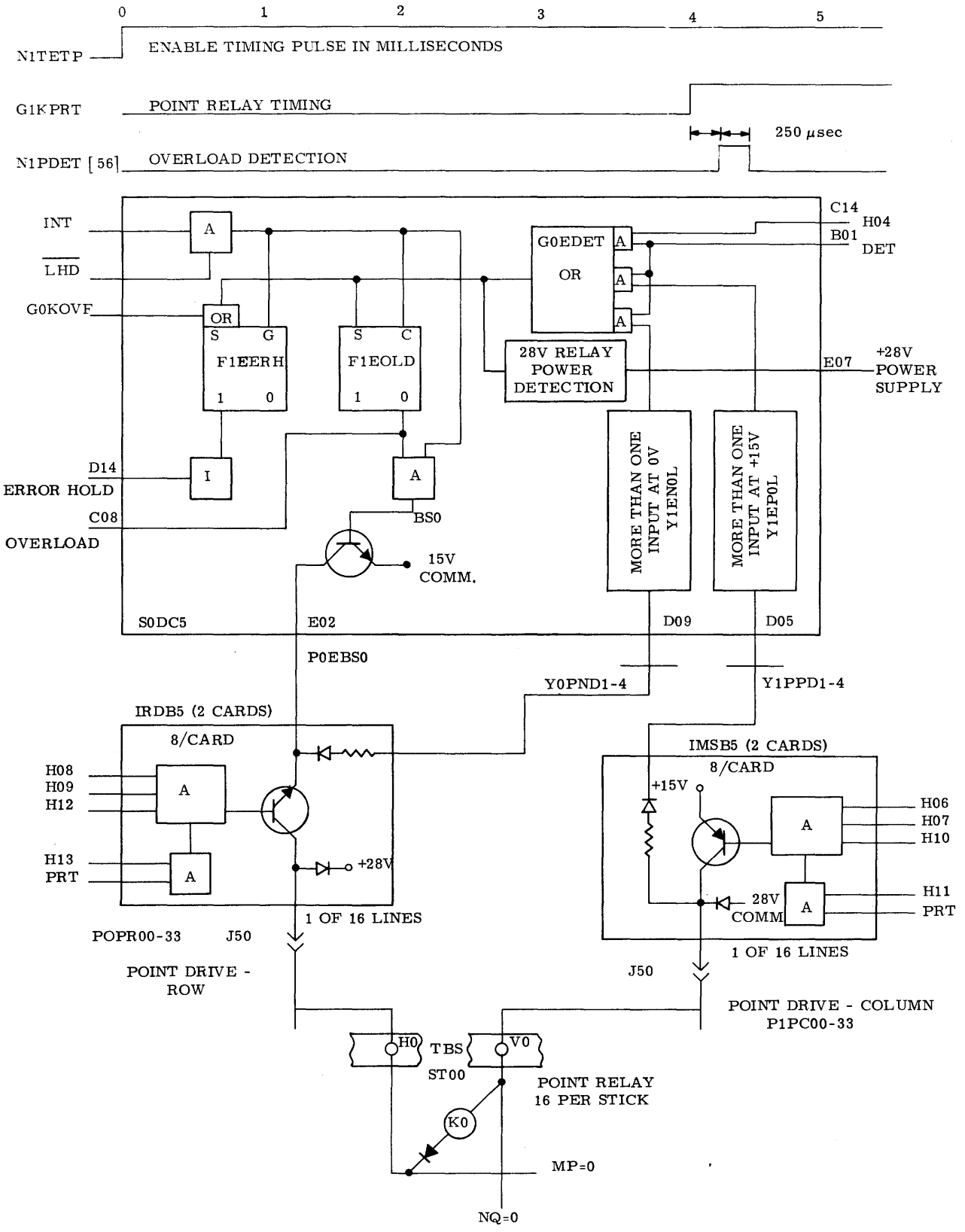


Fig. OP.5 Error Detection, Simplified Schematic

- Enable matrix overload display N1SMOL which turns on maintenance panel display bit I00.
- Enable overload alarm test line for A register display.

F1EERH will initiate the following:

- Inhibit decode ready G0KDRD which drives the JNR ready test line false.
- Inhibit data ready output G0KDRO which drives the data ready output API line false.
- Enable error hold N1KERH which drives the JNE error test line false.

OVERFLOW: An overflow error will occur anytime the A/D converter generates a count which is beyond the capacity of it's C register. More specifically: If the analog input during a conversion is equal to or exceeds +10.24 V dc (4096 counts), the overflow is positive (sign bit = 1). If the analog input to the converter is equal to or exceeds -10.2375 V dc (4095 counts), the overflow is negative (sign bit = 0). The overflow error is sensed and alarmed as shown on sheet 65 of the logic.

If a positive or negative overflow is sensed during converter busy G1ABSY, the overflow gate G0COFA is enabled. As a result:

- Maintenance panel display bit S01 is turned on.
- A register bit A01 is enabled when C register data is inputted.
- The error hold F1EERH flip-flop is set. F1EERH will initiate the same action as described for Overload.
- G1CBSY is delayed for 10 μsec to allow the controller sufficient time to recognize the error.

TEST MODE OPERATION

The test mode feature of the AIS allows simple accuracy and fault isolation checks to be made at any time without altering the system or using test equipment.

The test mode of operation may be initiated from the computer or the maintenance panel by enabling SCW-23 (TB = 1) and selecting the desired test signal(s) in the SCW channel select field SCW-15 - 22 (see Fig. OP.1). All other SCW bit positions become irrelevant except the scale field SCW-0 - 3 which become functional when any of the lower order test signals, SCW-15 - 18, are selected.

When the SCW with bit 23 set is transferred to the "H" register, the normal mode logical events which occur at phase B time are modified as follows:

- The maintain short circuit gate G1SMSC [F0DH23] 50 is enabled. This signal is used to inhibit amplifier short circuit control G0SDSC during SRT. The shorting switch in the I Cabinet (see Fig. Gen Desc.6) will remain de-energized keeping the input to the fixed gain amplifier shorted. Note, an overload F0EOLD will hold the amplifier shorted in the same manner.

- The enable W-test switch gate G0XEWT [F1DH23] 52 is enabled while channel selection control is inhibited G0WEWM [F0DH23] 51. Test voltage selection is enabled during CST as in normal mode. The test voltage multiplexer, shown on sheet 61 of the logic, will switch the selected test voltage to operational amplifier Y1ATVS. The output of Y1ATVS will go to the variable gain amplifier P0AAMP if SCW-15 - 18 was selected; however, if any of the upper channel switches SCW-19 - 22 was selected; the output of Y1ATVS will go directly to the A/D Converter.

- The gain select amplifier isolation gate G0KGSA [F1DH23] 43 is enable if any of the upper channel switches SCW-19 - 22 have been selected. When enabled, GSA will in turn enable relay driver P0GGSA which energizes relay K1, shown on sheet 63 of the logic. This relay opens the output of the variable gain amplifier and connects the output of the operational amplifier directly to the A/D converter as explained above.

- The ramp initialize gate D0DRMP [F1DH23] 48 is enabled providing SCW-21 was selected and the A/D converter is ready to start conversion.

  Since the ramp generator, shown on sheet 64 of the logic, runs continuously, it is desireable to initialize or drive its output to zero prior to selecting RMP (SCW-22) as a test input.

  The $\overline{\text{D0DRMP}}$ signal is inverted and ANDed with SCW-22 to enable G0KRMP which will initialize the ramp generator. At the same time, test voltage multiplexer switch Y1AS15 is enabled and analog ground is switched to the A/D converter input via the operational amplifier.

MAINTENANCE PANEL OPERATION

The Maintenance Panel must be enabled for off-line operation or disabled for on-line operation by jumpering the proper switch. The following text describes the functional capabilities of the panel in each type of operation.

On-line Operation (Panel not enabled): The panel is normally operated in the on-line mode to continuously display the contents of either the H or C registers. The display format is shown in Fig. OP.1. Selection is made by operating the C REG H switch S5.

When the C register is selected for display, the address COMP switch S12 becomes functional. In the normal or no compare position, the display register is loaded with the contents of the C register each time the Data Ready Input DRI signal goes true. Should the program be scanning a number of points, the display will follow each output at the same scan rate. However, in the COMP position, the display is loaded only when there is an address compare signal G1AADC and DRI (see logic sheet 24).

In order to generate address compare, the H register (bits H06 - H23) must hold the same digital configuration as panel switches S06 - S23. Note, S00 - S05 must remain cleared ("0" position). Now, should the program be scanning a number of points, only the point whose address has been placed in the panel switches will be displayed after conversion. A new address or SCW can be selected at any time while the program is running. All other switches are disabled while operating on line.

Off-line Operation (Panel enabled): The panel may be used as required to check, calibrate, or troubleshoot the AIS without interrupting other CSU functions. Three modes of operation are described:

- Single Step Mode. Any one of the GEN-II command switch selections (S=1, S-4, S=5) may be single stepped or cycled through an operation by: (1) Placing the MODE switch in MAN. (2) Load the desired SCW in the H register switches. (3) Select the desired command switch. (4) Initialize the panel. (5) Operate the STEP switch.

  A single command will be cycled each time the STEP switch is operated in the same manner as if the command originated from the CSU. The selected command, along with the address bits and phase A, B are ORed into the controller via the logic shown on sheet 17. The SCW bits are enabled via the logic on sheets 15 & 16.

- Auto Mode. Any of the GEN-II command switch selections may be cycled continuously at maximum possible rate by: (1) Loading the desired SCW in the H register switches. (2) Select the desired command switch(s). (3) Initialize the panel. (4) Place the MODE switch in AUTO. (5) Operate the STEP switch.

  Command switches and H register switches may be changed to generate a new command or SCW without stopping the operation. To stop the operation, place the MODE switch in MAN. The C or H display and address compare feature may be used as described under Off-line Operation.

  The S=4 and S=5 command switches may both be selected. In this case, the OUT command will be executed followed by the necessary number of IN commands. After the "end of operation" signal ($\overline{\text{N1SEOP}}$), the OUT/IN cycle will repeat on the same or new SCW. The timing diagram for the single channel auto mode is shown on sheet 14 of the logic.

- Auto Delay Mode. This mode is selected in the same manner as described above, except that the DELAY switch S3 is also turned on. The selected command(s) will be cycled continuously but with a delay of 750 ms between interrupts (DRI or EOP). This built-in time delay is used, in effect, the same as a programmed delay making it possible to read the C or H display without stopping the program.

  In the auto delay mode, G0SCYL is enabled via it's right side gate (see logic sheet 24). The cycle flip-flop F1SCYL is set and the counter enabled in the same manner as in the Auto Mode. The setting of F1SCYL will force F1STDC to set, triggering the time delay element CKT1 which holds F1STDC set for 750 ms; thereby, inhibiting G0SCYL for that period of time. When the time counter completes it's timing of phase A, B, the G0SEND signal will clear F1SCYL. This will allow CKT1 to reset or initialize F1STDC after it times out. Thereby, removing the inhibit from G0SCYL. The ready signal G1SRDY may now initiate the next cycle.

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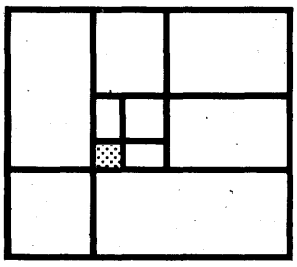

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