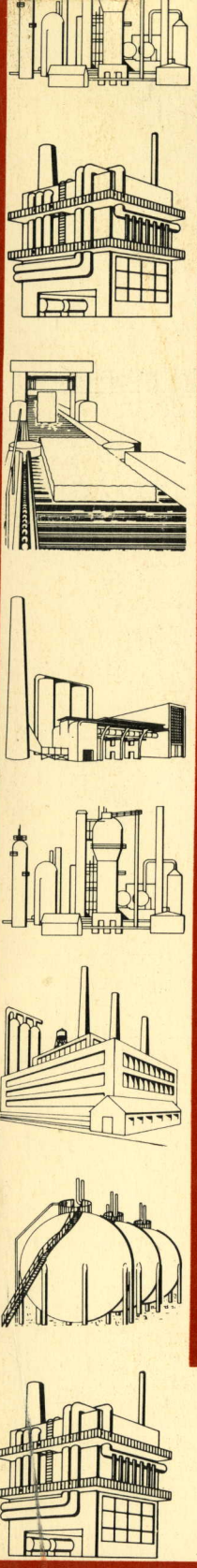
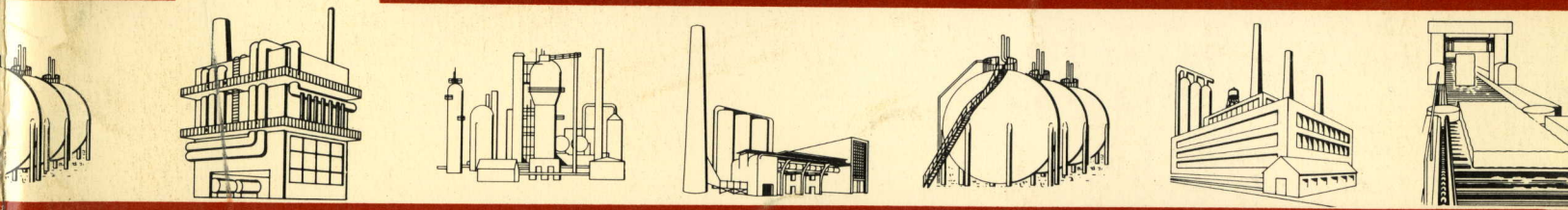
PCP 49
GET 3008



# GE 412
# SYSTEM MANUAL



PROCESS COMPUTER SECTION
INDUSTRY CONTROL DEPARTMENT
PHOENIX, ARIZONA

GENERAL ELECTRIC

# GE 412

# SYSTEM MANUAL

PROCESS COMPUTER SECTION
INDUSTRY CONTROL DEPARTMENT
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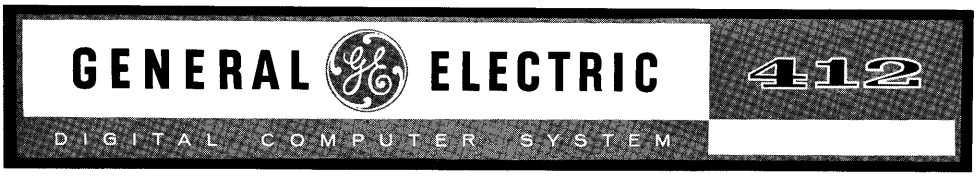

## PREFACE

This manual presents an overall view of the GE 412 Process Control and Monitoring Computer System, and the services General Electric provides to system users. Described are the system's central processor, input-output units, and program instructions. Considered briefly are system application, special features, quality of operation, programming aids and services, and equipment installation.

A complete coverage of programming techniques, including programming examples, will be found in the GE 412 Programming Manual. More detailed information on system application, and equipment operation will be covered in separate publications.

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# LIST OF ILLUSTRATIONS

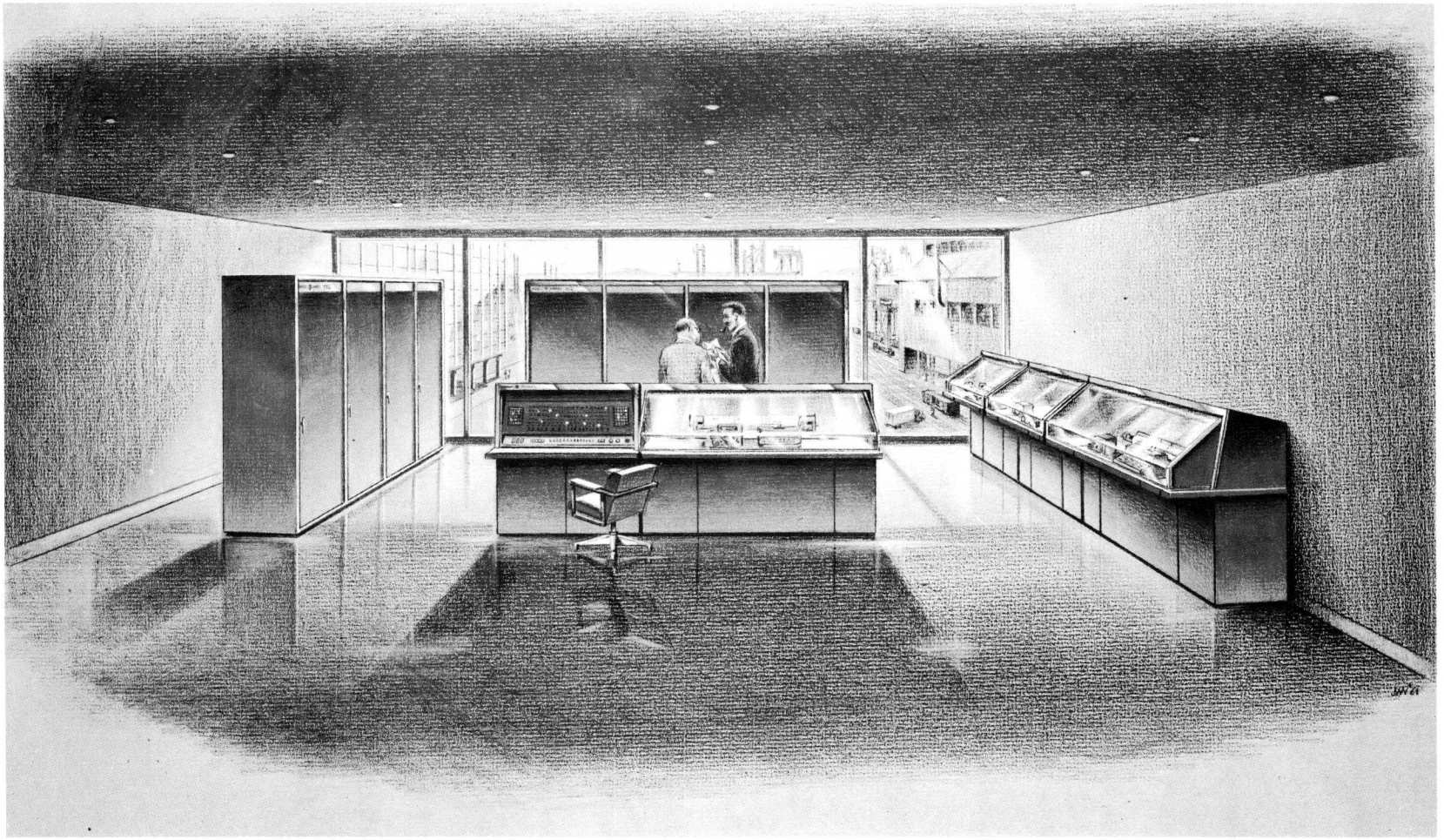


Figure 1. GE 412 Process Control and Monitoring System

# I. INTRODUCTION

The GE 412 Process Control and Monitoring Computer System is a system of advanced design incorporating latest digital computer technology plus those characteristics that have made the GE 312 the popular leader in industrial automation. The GE 412 System has been designed for logging, monitoring, and control of industrial processes.

The binary number base computer system features time-shared magnetic core storage, magnetic drum backup bulk storage, solid state circuitry throughout, over 100 basic computer commands, parallel operation, automatic program interrupt, variable time counters, and rugged construction for industrial environments.

The GE 412 Computer may be used:

1. As the central processor for a data logging, monitoring, data processing, and control system.

2. In conjunction with the typewriter, paper tape punch and reader options, as an off-line computer for scientific and engineering calculations.

3. As a dispatcher in a multicomputer or computer equipment system.

GE 412 Systems are highly adaptable to processes and other functions in industries such as electric and gas utilities, steel mills, cement, mining, glass making, chemical, petroleum, and petrochemical. This unique versatility is achieved by means of a fast, microcoded binary central processor, a wide array of peripheral input-output devices, and logic circuitry that form a multi-plexer which acts as a "traffic controller" for input-output devices which must communicate with computer memory. Design emphasis is on the total systems concept and flexibility of hardware organization as the answer to the increasing complexity of today's industrial applications.

Digital computers used in industrial applications must operate reliably during the same period of time that the process is operating. GE 412 Systems are designed to meet this requirement. To gain the required reliability and availability, the GE 412 features solid state components operated well below their rated capacity, field proven circuits, magnetic drum backup memory, built-in checking features, integral air conditioning, and rugged industrial-type cabinets.

In summary, GE 412 Process Control and Monitoring Computer Systems can assume many different configurations for various industrial applications. They are custom-adapted, both hardware and program-wise, to particular applications to provide the user with easy-to-apply and trouble-free automation.

# II. GE 412 SYSTEM CONFIGURATIONS

GE 412 Computer Systems are generally used in one of the following four application classes:

Data logging and monitoring

Data logging, monitoring, and control

Utility system dispatching and economic operation

Dispatcher for a multicomputer system

The system configurations which follow are typical of each of the four classes. The applications shown and briefly described are also typical; the same hardware configuration could be applied with little or no modification to many different processes of the same application class.

## A. DATA LOGGING AND MONITORING

The typical functions of a GE 412 System for steam plant data processing are data logging and alarm, performance calculations, and monitoring of startup and shutdown sequences. Figure 2 is a diagram of this application.

Scanning, alarming, and logging are inter-related functions. Normally, each point is scanned according to a prescribed sequence and frequency. After each point is scanned, the value is compared against the high/low limits for alarm purposes. These limits are stored in the memory of the computer and may be changed by an authorized operator. When a point is out of limits, the computer initiates an alarm printout and annunciates an alarm. Continuous scanning proceeds at all times and is not interrupted when an on-demand log is required or when it is time for the regular periodic log.

The computer performs the necessary calculations to present the most recent set of scanned and computed values to determine quality of operation for an on-demand or periodic log. Performance calculations which give a current indication of the operating status of any steam plant can be computed by an on-line process computer and provide accurate, meaningful, and timely information to guide system and plant operations. The on-line computation of the performance calculations permits much closer observation and control of the process variables, and thereby results in increased plant efficiency.

The GE 412 System can also provide startup and shutdown monitoring which aids the operator during startup and shutdown to insure safe and methodical manual operation of the boiler, turbine, generator, and auxiliary equipment. The computer does not actuate or perform any of the startup or shutdown functions, but it monitors the manual operations and provides indications to the system operator during this critical period.

## B. DATA LOGGING, MONITORING, AND CONTROL

The addition of control to the computer application means that the computer operates directly without going through the operator. The minute-by-minute instructions normally given to the operator become the set-point signals and contact closures which the computer sends out to the controllers and control devices.

Figure 3 diagrams the application of a GE 412 System to a hot strip mill for the steel industry. This equipment configuration is typical of a large complex data logging, monitoring, and control application. As represented, the hot strip mill application consists of six major functions which are automated:

mill pacing

temperature control

mill setup

mill data logging and drift correction

slab tracking

production and quality data log

As illustrated in the figure, the paper tape reader (upper left corner) reads into the computer the mill schedule for a specified period of time, such as one hour. The computer then takes over and paces the mill by indicating when to push slabs out of the furnaces. As the slabs progress through the hot strip mill, they are sized, rolled, and carefully controlled by the GE 412 System and the existing gage control system. The high speed, large capacity, and great flexibility of the GE 412 System allow it to keep track of and control all slabs in the reheat furnaces and the several slabs that will simultaneously be in the hot strip mill being processed. Production data is punched out on paper tape and sent to mill accounting.

## C. UTILITY SYSTEM DISPATCHING AND ECONOMIC OPERATION

This application of the GE 412 Computer System (diagramed in figure 4) provides the following:

Immediate information on system operating conditions

Automatic logging of system data

Automatic alarming of overload or abnormal conditions

Interconnection billing

Economic loading of transmission lines and generating units

The application not only relieves the system dispatcher of many routine operations, but offers considerable savings by continually monitoring the system operation.

Inputs to the system are voltage signals representing area requirements, system generation, and interconnection flows which are scanned directly from telemetering channels. Digital telemetering of interchange billing meters or system loads may also be scanned and entered directly into the computer for billing calculations. The output of the system may be electrical analog signals proportional to unit megawatt loads, digital data for logging typewriters, digital data for alarm printers, digital data for billing printout on a typewriter, or digital data punched on paper tape for reentry to the computer.

The calculation procedure for both the economic dispatching of power systems and the transient gas flow dispatching programs is an iterative solution of a set of equations defined to balance the flow of power or gas throughout the system. These calculations are continuously being made at short time intervals to either control or monitor system operation. Other calculations such as: interconnection billing of power and gas, generation unit commitments, monitoring of spinning reserve, indication of line overloadings, system simulation, energy accounting calculations, and load forecasting are normal system operating routines that can be automatically calculated on a time-shared basis with the normal scanning, logging and dispatching routines. System dispatchers can insert information directly into the computer through the media of the operators console or paper tape reader.

## D. DISPATCHER FOR A MULTICOMPUTER SYSTEM

The GE 412 System may be used as a director, coordinator, and controller of a large chemical complex. This application emphatically illustrates the flexibility and the far reaching capabilities of the GE 412 System. As shown in figure 5, GE 412 Systems 2, 3, and 4 are used as data loggers, monitors, and process controllers for specific processes in the chemical plant. The process variables are flows, temperatures, compositions, pressures, and levels which the GE 412 must sample at frequent intervals. These variables are checked for off-limits, updated in memory, logged on typewriters, and used by each computer as part of the control for the individual plant processes. Because it is recognized that the plant processes are not independent but that each strongly affects and is influenced by other processes in the plant, an over-all director or integrating computer is needed. For example, the output of the feed preparation process serves in part as an input to the reaction section. The reaction section in turn helps determine the type and quantities which are needed from the feed preparation unit. Thus, the individual plant process must be coordinated in an optimum manner for plant efficiency, production, and costs.

Computer system number 1 receives summary data from computer systems 2, 3, and 4 periodically. Based on this data, system number 1 performs calculations using a mathematical model of the overall process stored in its memory, and transmits via communication lines the necessary information to coordinate the activities of systems 2, 3, and 4 in an overall optimum manner. The high speed and large capacity of the GE 412 allows system number 1 to perform this directing function while simultaneously controlling and monitoring activities in the steam plant and keeping track of plant inventories.

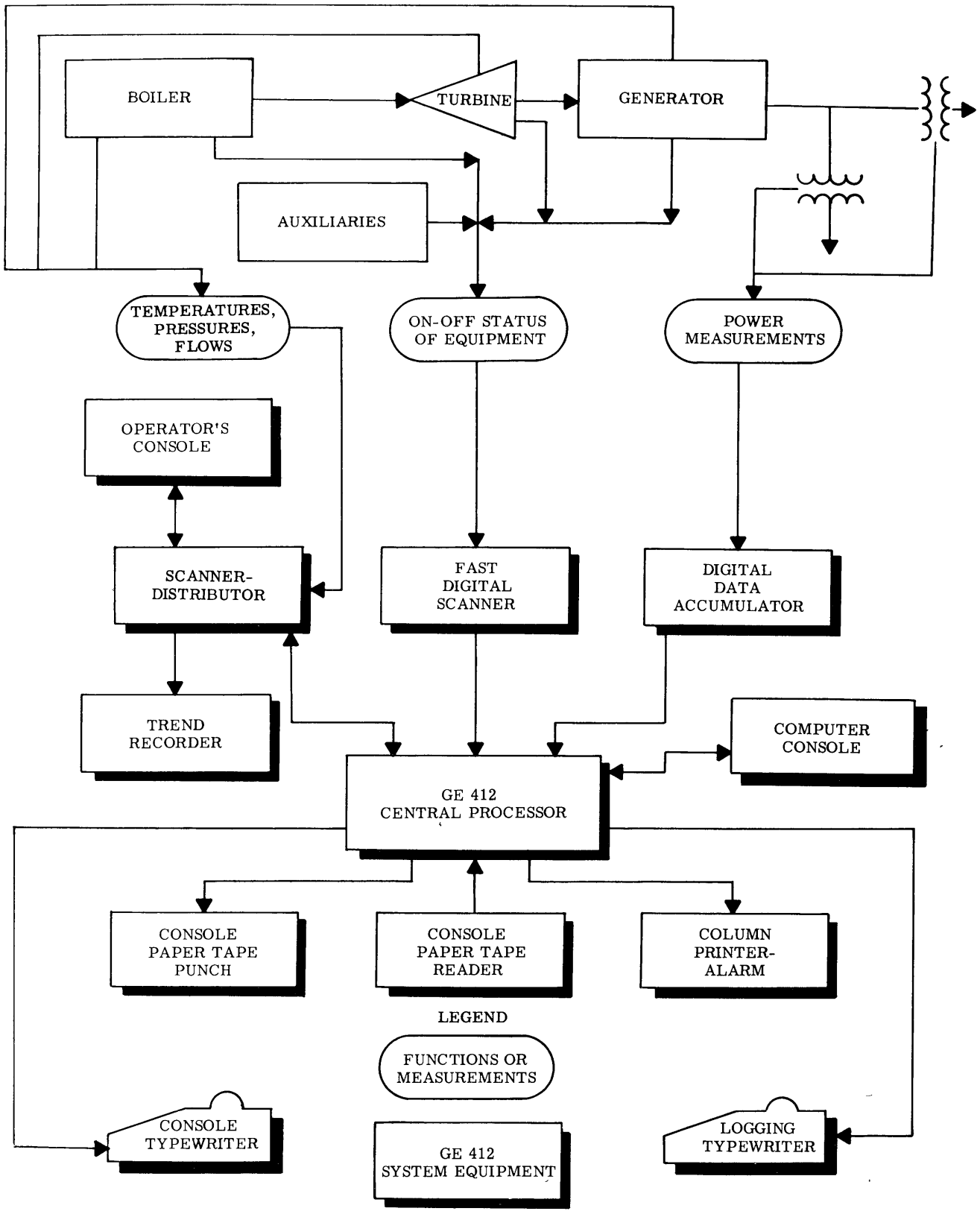



Figure 2. Typical GE 412 Data Logging and Monitoring System
(Utility — power plants)

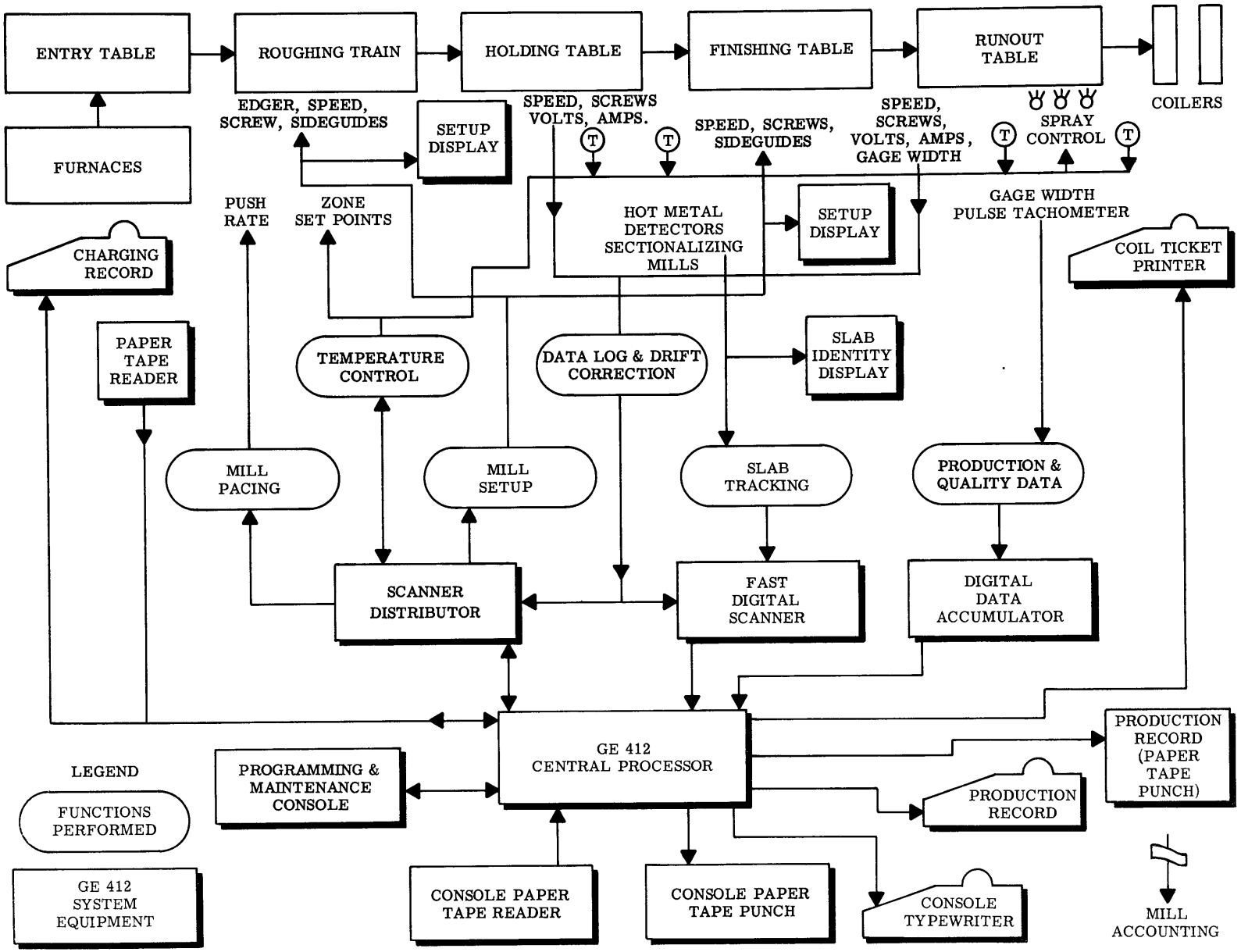



Figure 3. Typical GE 412 Logging, Monitoring, and Control System
(Steel — strip mill application)

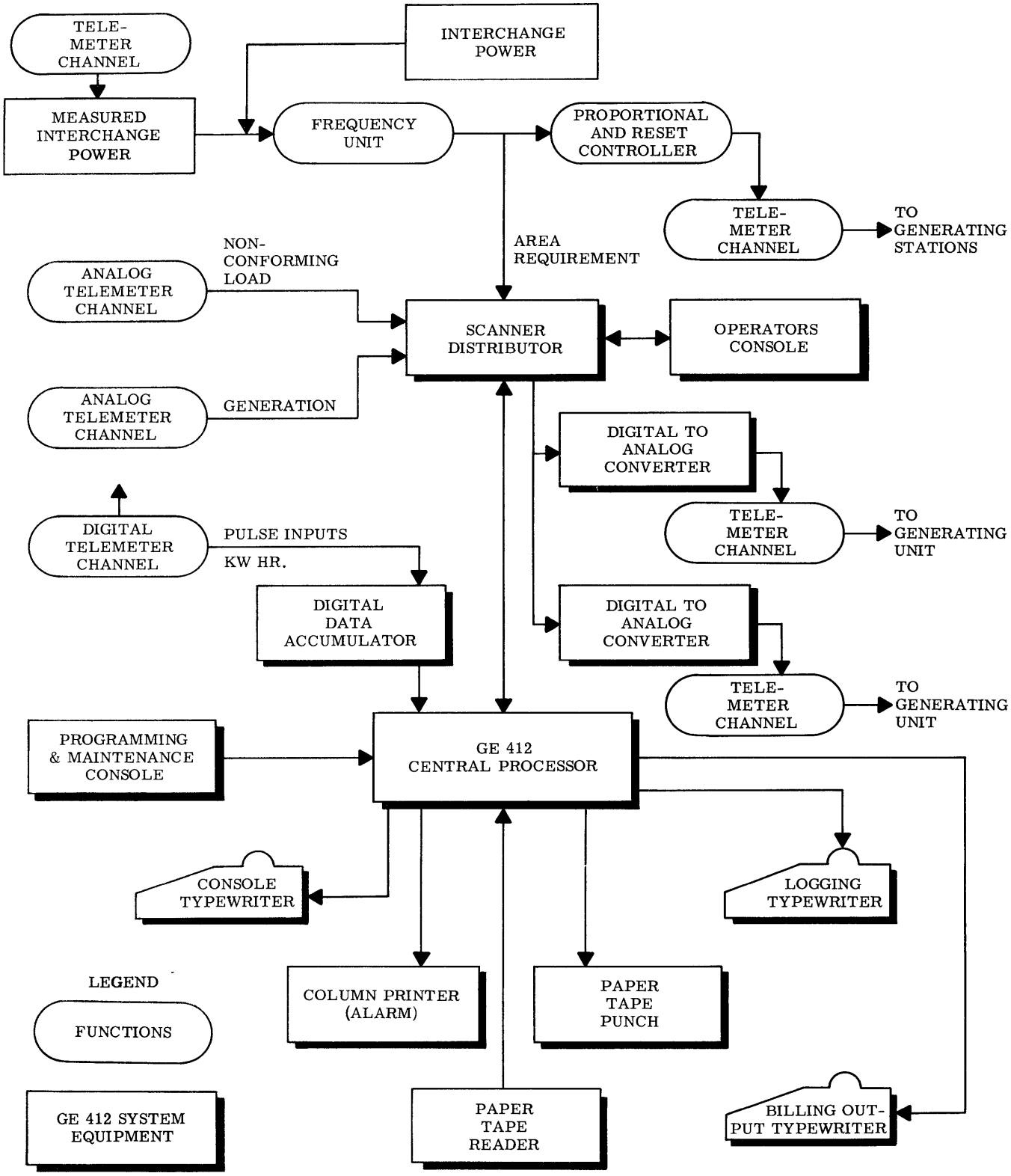



Figure 4. Typical Utility System Dispatching and Economic Operation

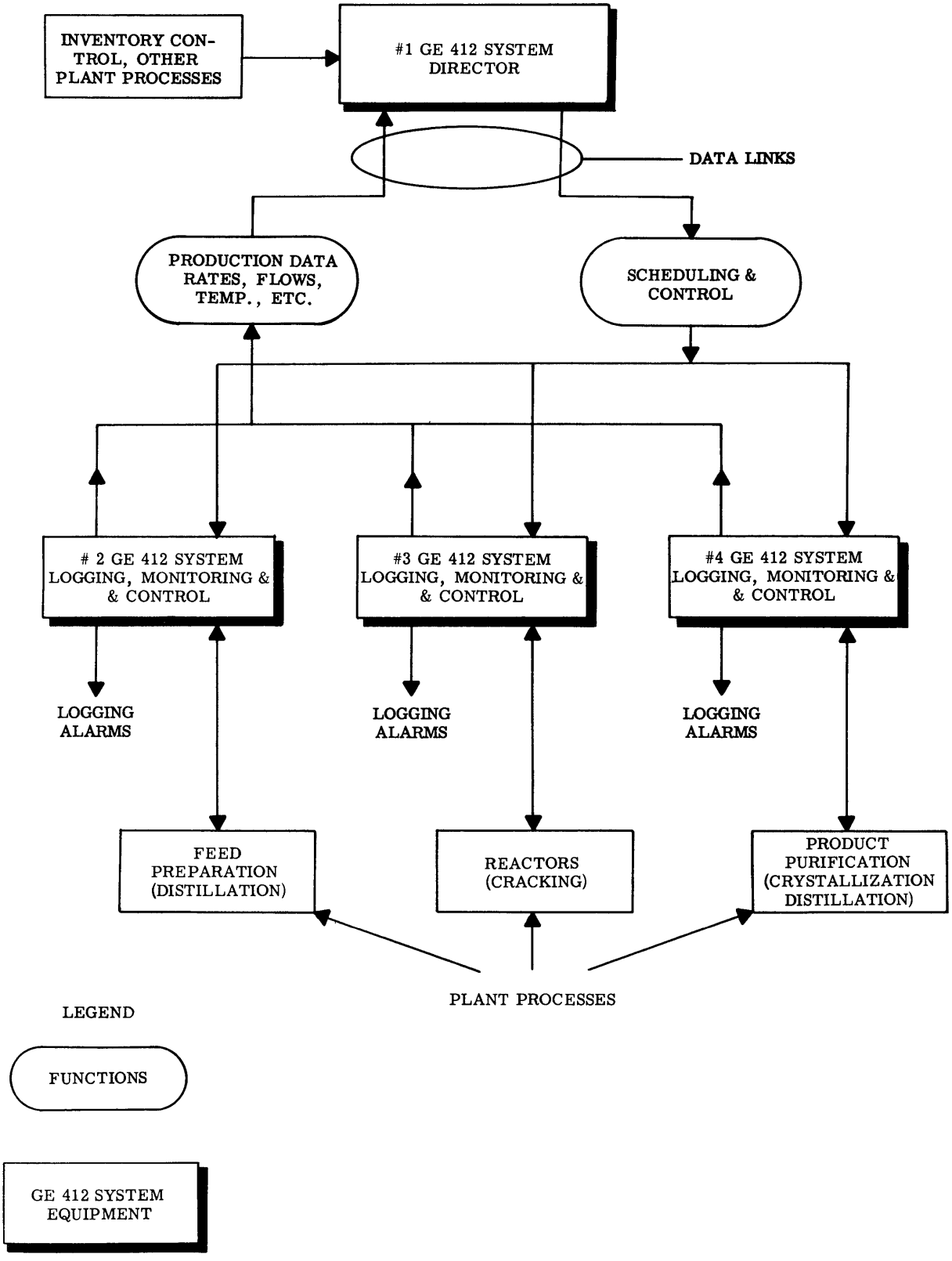



Figure 5. A Typical GE 412 Director (or Dispatcher) for a Multicomputer System (Integrated automation of chemical complex)

# III. THE GE 412 SYSTEM'S CENTRAL PROCESSOR

The heart of the GE 412 Process Computer System is the central processor. Figure 6 shows the relationships of its main sections. The central processor contains the computer's storage sections and sections for arithmetic computation and control functions. It operates in a fixed point, true binary form, and can process both alphanumeric and binary information. Normally, instructions are executed sequentially: the next instruction is read from storage after the execution of the current instruction. The program address register (P register) is a sequence control counter, and contains the address of the next instruction to be executed. In order for the central processor to fetch and execute program instructions in an orderly manner, it is necessary to provide a definite time base for these operations. The effective pulse frequency for all central processor operations is 400 kilocycles. The time between these basic pulses is 2.5 microseconds. Eight of these pulses comprise another basic unit of time, known as a "word time", which is of 20 microseconds duration. A word time is the time required to read one word out of memory, transfer this

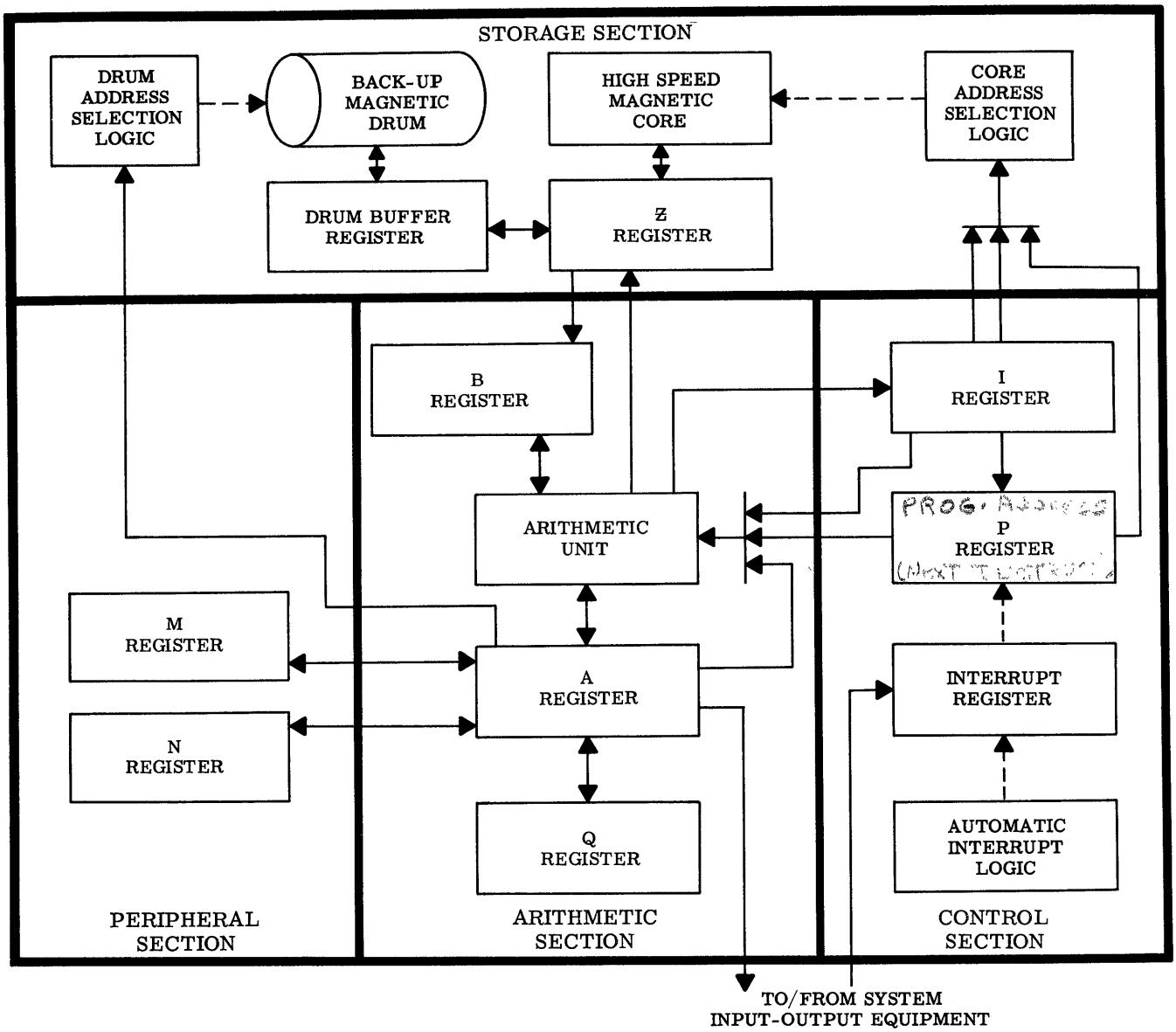



Figure 6. Relationship of Main Sections of the GE 412 Central Processor

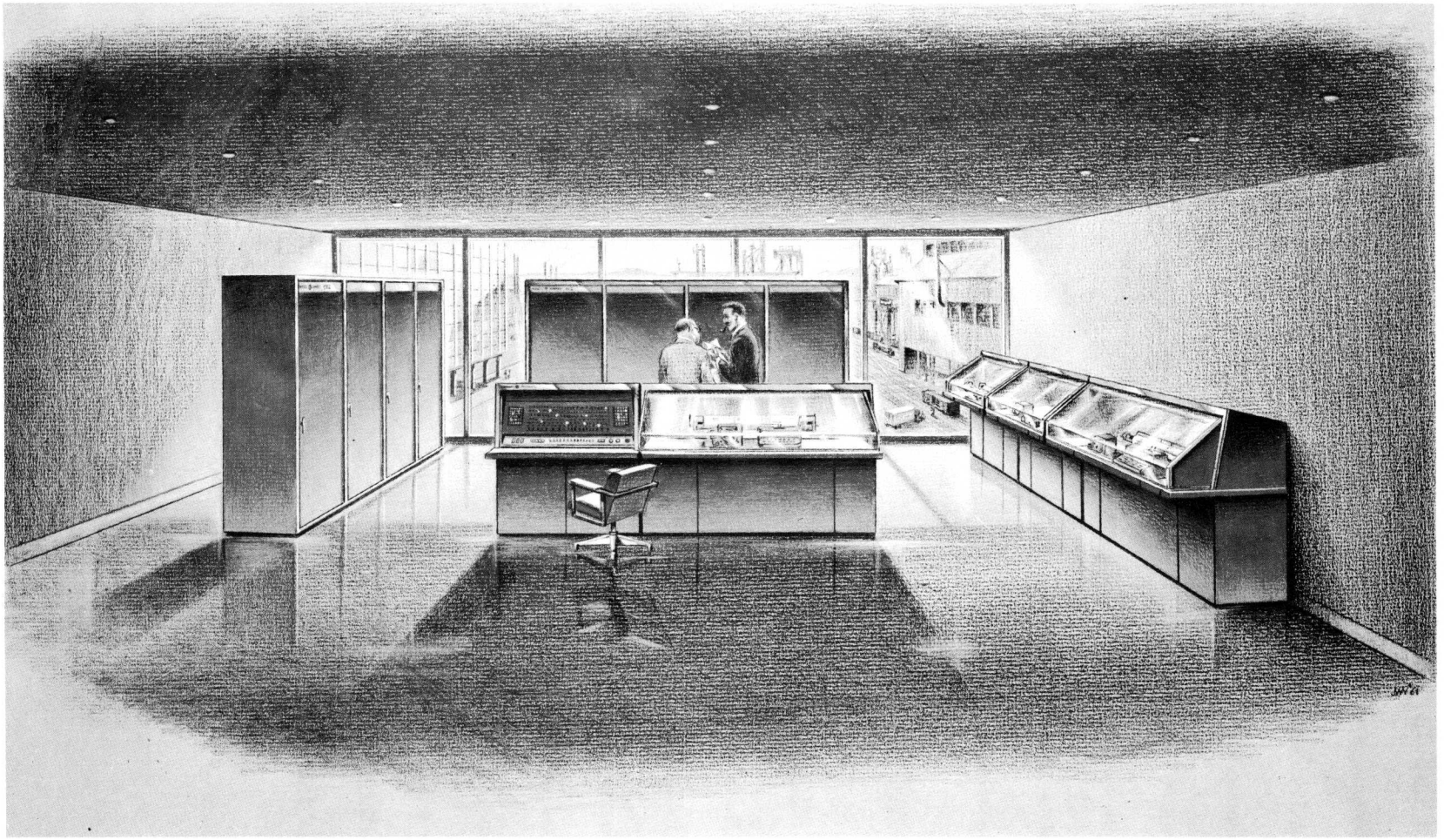


Figure 1. GE 412 Process Control and Monitoring System

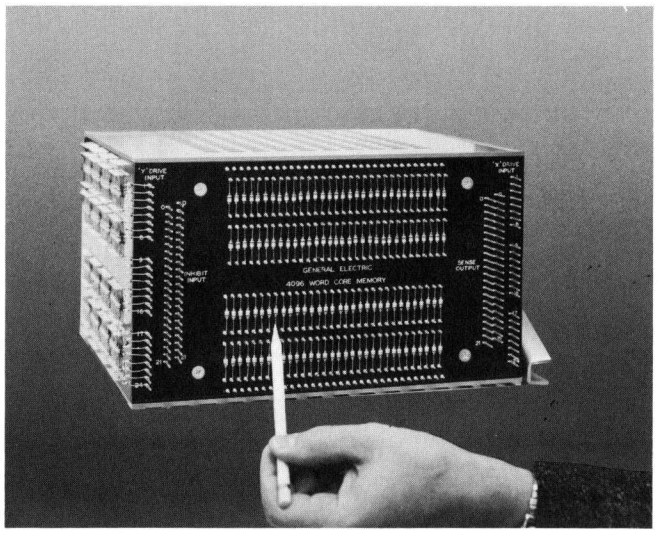



Figure 8. High-Speed Storage Unit

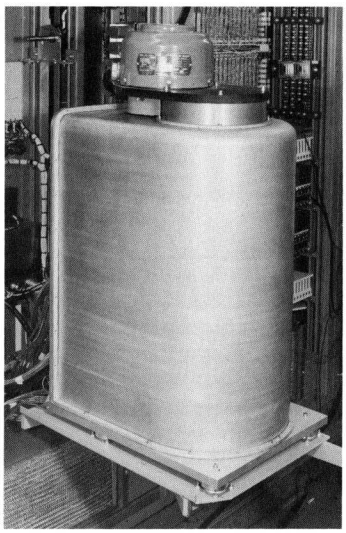


Figure 9. Backup Storage Unit

word to the appropriate register or registers, and rewrite the word in memory. Thus, one word time will be required to fetch an instruction out of memory, and one word time will normally be required to look up the operand associated with the instruction and perform all operations necessary for its proper execution. Some instructions such as multiply and divide require more than one word time for their complete execution. (See Section IX for exact word times.)

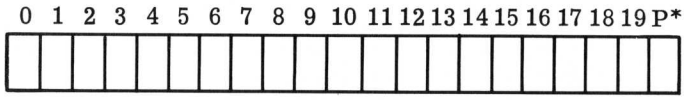
Although the central processor is described under the headings of storage, arithmetic, and control units, it should be understood that there is an interrelation in the functioning of these units.

## A. STORAGE

Both high-speed, random-access core units and backup, bulk-storage magnetic drum units are available for the GE 412 System (Figures 8 and 9).

1. High-Speed Core Storage

The high-speed storage unit is made up of magnetic cores, each of which can be magnetized to represent either a binary "1" or a binary "0". A group of 20 binary digits forms the basic unit of addressable information, called a word; a word may be either data constants, or computer instructions. When a word is placed in storage, a parity bit is added, making it 21 bits long. The parity bit is used to check the validity of information as it is transferred out of storage. The bit positions of a word are shown in the following diagram. Items (bits) of information are referenced by the positions they occupy in the word.




*P = parity bit (present in storage unit only).

The magnetic core storage has numeric designations (addresses) referring to storage location; each storage location contains one word. Core storage units are available in two sizes: 4096 words, and 8192 words.

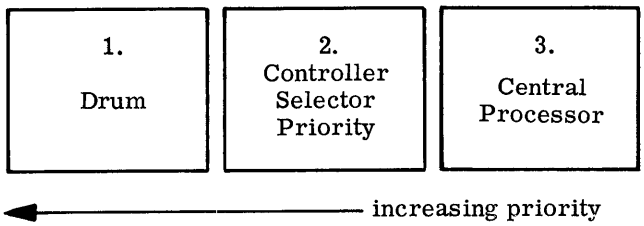
2. Backup Magnetic Drum Storage

There is a choice of four sizes of rotating magnetic drum storage units. These act not only as backup (protective) storage, but they effectively increase the on-line storage capacity by 16,384; 32,768; 40,960 or 57,344 words. This additional storage may be used to store data, tables, or special subroutines which can be quickly transferred to core storage. The magnetic drum rotates at 3600 rpm and is asynchronous to computer timing. Allowance is made for the magnetic drum storage to have automatic access to core storage when a read or write command is given. The drum and central processor have access to core storage on a time-shared basis, thus the central processor calculations proceed at approximately 84% of maximum speed while reading from or writing on the magnetic drum. A data word in drum storage is identical to a word in core storage. The drum is divided into divisions called tracks, and each track contains 128 words. A read-write (sensing or magnetizing) head is associated with each track. Data may be transferred by command between drum and core storage in

blocks of from one to eight consecutive tracks at the rate of over 7,500 words a second. A "transfer complete" command indicates the conclusion of the branch.

3. Basic Internal Priority

The design of the GE 412 System permits the core memory to serve the dual function of: (1) main memory and (2) input-output buffer. Thus, two or more asynchronous operations may be performed simultaneously; for example, drum reading or writing while computing at the standard 400 kilocycle repetition rate. Processor computation and access to the memory will have to be interrupted on demand to allow information to be entered or taken out of storage at the request of the input or output devices currently in operation. Since several requests for access to storage might be made at the same time, a provision is made to permit only one such request during a particular word time. The permitting of a request for access to storage is dependent upon the priority assigned (built into the computer).




Priority is determined by the repetition rate of pulses (information) going to or coming from the input-output device. Thus, if a request for access is received from two input-output devices simultaneously, the one with the higher repetition rate will have top priority, hence be granted first access. The other device will wait for one word time. The central processor will always have the lowest priority (to prevent loss of information being transferred).

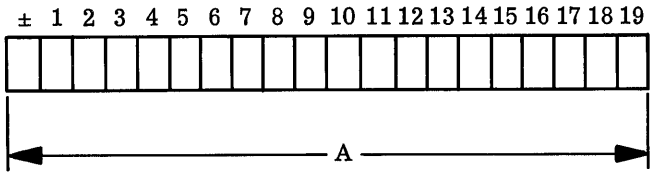
4. Stored Program

The GE 412's process monitoring and control function is accomplished as a result of automatically executing many instructions at high speeds. The set of instructions (the program) is stored on the storage units. Paragraph C2 of this section describes program execution sequencing. Conditional control endows the program with a decision-making ability. As a result of test or branch instructions the program can determine the alternate paths of instructions to follow without manual intervention.

## B. ARITHMETIC COMPUTATION

The arithmetic unit (figure 6) performs addition, subtraction, multiplication, and division. It also makes logical decisions by comparing the magnitude of numbers including algebraic signs. Three registers designated A, Q, and B, each 20 bits in length, are integral to arithmetic operations. The A and Q registers can operate independently or together as a 38 bit register plus sign.

1. The A Register




The A register serves as the accumulator for arithmetic operations. Its contents are directly displayed on the programming and maintenance console, and may be loaded manually from 20 console switches; for example, in initial program startup when it is necessary to get the first instruction into the machine. The contents of the A register may be interrogated for positive values, negative values, zero quantities, odd or even numbers, and for logical program branches. The functions which the A register performs in the arithmetic process are the following:

Holds the augend during addition.

Holds the sum after addition.

Holds the minuend during subtraction.

Holds the result after subtraction.

Holds the most significant half of the product after multiplication.

Holds the most significant half of the dividend before division.

Holds the quotient after division.

Holds the most significant half of the double length word after the execution of all double word length instructions.

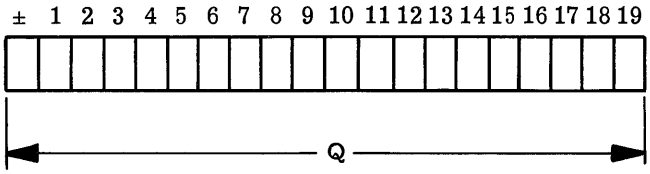
Holds the word on which extraction is performed during the execution of the extract instruction.

Carries the word to be shifted during various shift instructions.

Holds a word which is to be transferred to another register or which is to be modified in some way during the execution of various data transfer commands.

Holds the word which determines future action during the execution of various branch instructions.

2. The Q Register




The Q register acts as an accumulator when combined with the A register to form 38-bit words during the execution of double word length instructions.

Information is not transferred directly from memory into the Q register, but is transferred through the A register into the Q register. The functions which the Q register performs are the following:

Holds the least significant half of the double length word during the execution of double length load and store instructions.

Holds the least significant half of the result after multiplication.

Holds the least significant half of the dividend prior to division.

Holds the remainder after division.

Holds the least significant half of the augend prior to double addition and the least significant half of the sum afterwards.

Holds the least significant half of the minuend prior to double subtraction and the least significant half of the result afterwards.

Holds the least significant half of the information to be shifted during double shift instructions.

Can be shifted right or left along with the N and A registers in special shift instructions.

3. The B Register

The B register serves as a buffer between the arithmetic and Z registers. All information transferred from core storage (via the Z register) to other internal registers and components of the central processor must first pass through the 20-bit B register. This permits storage and Z register to be free to be accessed and utilized simultaneously with central processor operations which do not require the use of storage, such as during multiply and divide instructions, after initial memory access. The B register is used in the execution of certain data transfer commands, and in arithmetic operations it:

Holds the addend during addition

Holds the subtrahend during subtraction

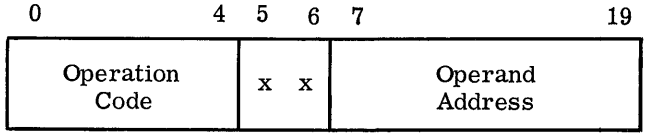
Holds the multiplicand during multiplication

Holds the divisor during division

## C. CONTROL

The control unit governs the logical order of execution of the individual commands of the program. It consists of three registers for automatic control address modification capability, and computer console for manual control. Connected with control are two input-output buffer registers.

1. The I Register




The I register is the instruction register, for it holds the 20 bits of the instruction word during execution of a computer command.

In the instruction format, as indicated above, bit positions 0 through 4 designate the operation which is to be performed. Positions 5 and 6 indicate whether the instruction will be automatically modified before its execution. When an instruction involves reading an operand from memory, bit positions 7 through 19 designate the operand address. When an operand address is not required, positions 7 through 19 have various meanings, as indicated in the instruction list, Section IX.

2. The P Register

The program address register (P register) is the location counter which controls the sequential execution of instructions; it holds the memory address of the next instruction to be executed. Its 13 bits, positions 7 through 19, are indicated by thirteen display lights on the computer console. The P register is incremented by one before the execution of an instruction so that it normally indicates the address of the next instruction in sequence. When programmed to do so, the address of the I register can be transferred to the P register.

3. The Z Register

The Z register is a focal point for information transfers among GE 412 units and internal registers. All information written into or out of the central processor's magnetic core storage must first pass through the Z register. The 21 bits of the Z register include 20 information bits and the parity check bit. When a

word (20 bits) enters the register in preparation for writing into storage, the number of 1 bits is counted. If the total is an even number, a 1 bit is generated and placed in the 21st. bit position. If the total is odd, a zero is generated, and the 21 bits are then placed in storage. When a word is read from storage into the Z register, another bit count is made to determine whether there is still an odd number of 1 bits in the word. If this check reveals an even number of 1's, a parity error will be indicated by a light on the console. The occurrence of a parity error may also be sensed by a branch instruction in the computer program. The parity error may or may not cause the program to halt, depending upon the corresponding switch position.

4. Automatic Address Modification

Address modification is achieved by utilizing three core storage locations: 0001, 0002, and 0003. Bit positions 5 and 6 of an instruction word indicate which of the three index locations, if any, are to be used. The address porition (bits 7 through 19) of the instruction to be modified and bits 7 through 19 of the index location selected are sent through the adder where they are added. The changed address is then returned to the I register, and the instruction is executed. One additional word time (20 microseconds) is required when automatic address modification is specified.

5. The Programming and Maintenance Console

The programming and maintenance console (figure 10) provides an indicating control center for the programmer and product service engineer. It permits manual control in contrast to automatic or program control. Manual control is used when initially loading the program into memory, to start program execution, to monitor the progress of the program, and occasionally to stop the program for maintenance and trouble shooting. The central processor's operating status can be seen from the display lights on the console panel. Among those indicated are the A register, I register, and P register. Twenty switches on the console permit direct loading into or changing data in the accumulator. The console has parity and overflow alarm lights and an automatic-manual key lockout switch. The console can be remotely located a distance of 50 cable-feet from the central processor.

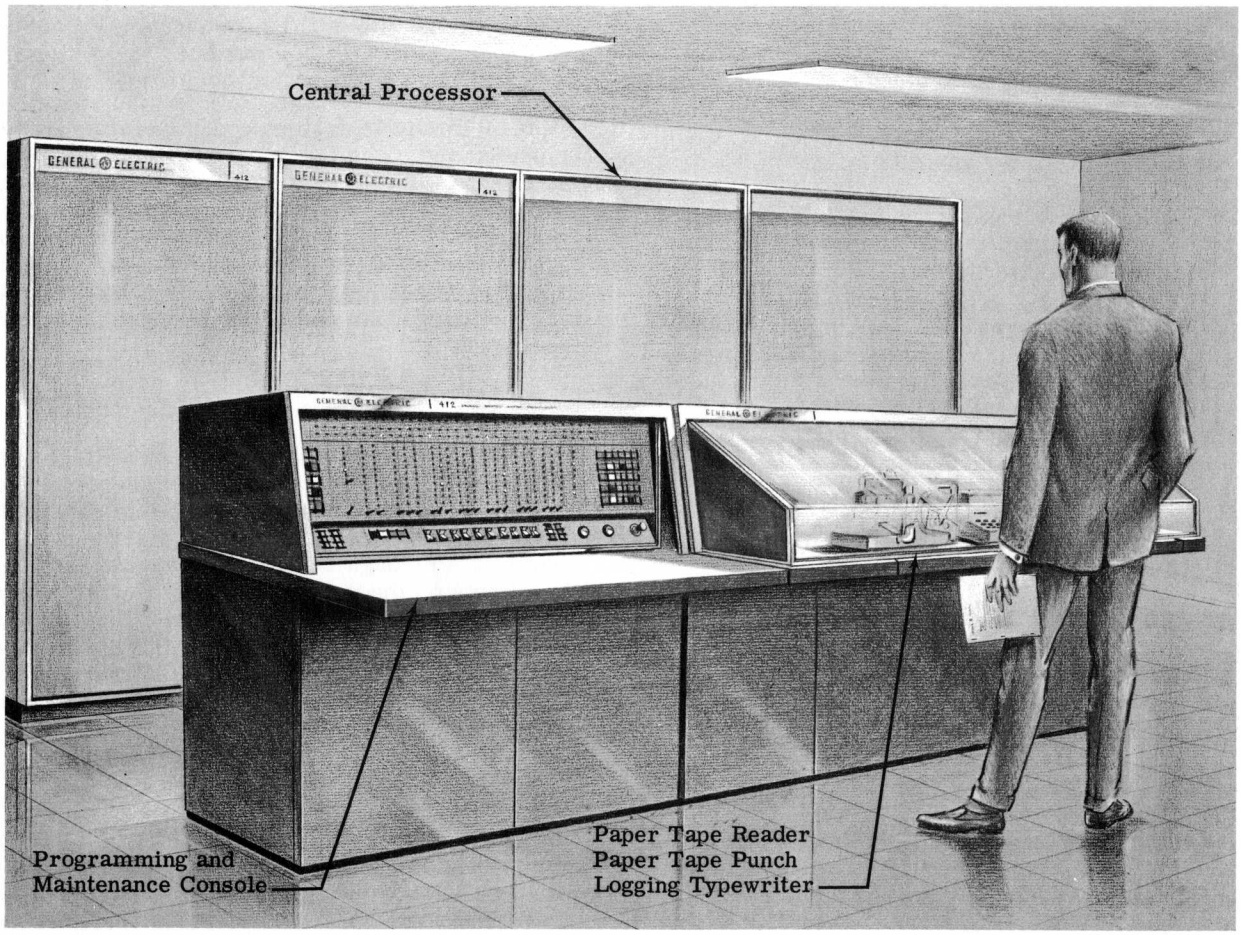



Figure 10. GE 412 Programming and Maintenance Console

## D. SPECIAL FEATURES OF THE CENTRAL PROCESSOR FOR PROCESS CONTROL

1. Automatic Program Interrupt

The feature of automatic program interrupt permits immediate execution of priority functions. It allows the computer system to keep under constant surveillance critical points in a process without consuming computer time by constantly scanning the points. Certain phases of a process may occur at random, but when they do occur, it is important that the computer immediately recognize the occurrence and promptly take whatever action may be required.

As an example, if it is desired to produce an alarm or set a control point when a power demand meter exceeds a certain point: the computer system continues its normal course of action without consuming time checking this point until the power demand point is exceeded. When this occurs, the computer branches out of its normal program to a predetermined address in core storage. The subroutine thus entered identifies the excessive power demand and directs the program accordingly. The computer returns to its normal program after solving the "crisis".

Inputs may be connected directly into the computer via the automatic program interrupt. The computer scans the interrupt at every instruction access time (not word access time), and if an interrupt signal has been received, the program is automatically branched to an appropriate subroutine.

The basis of the automatic program interrupt is the priority interrupt register. This is a 12-bit register divided equally into three priority levels for use in the event more than 1 of the possible 12 inputs alarms simultaneously. Under program control, the computer may allow:

No interrupts

Only priority I interrupts

Only priority I and II interrupts

Priority interrupts I, II, and III.

If an interrupt bit is present in an enabled priority level, the data in the P register will be stored in a fixed location in core storage and the program will branch to one of 12 predetermined locations. In case two or more priority levels have been actuated simultaneously, the highest level priority is acted upon first.

2. Program Variable Timing Control

Elapsed time counters provide another powerful tool to the programmer. Four 8-bit counters can be set by the program to count intervals of elapsed time in increments of 3 1/8 milliseconds, 17 milliseconds, 1 second, and 1 minute. The four available increments are divided among the four counters so that each increment is available to two counters. The program can preset the counters from the A register and indicate the end of selected intervals by branch commands; there is one branch command for each counter. The completion of any elapsed time in a counter may be determined under program control.

Elapsed time counters may be used in conjunction with the automatic program interrupt. When presetting the counters, the program may select whether or not a counter will cause program interrupt at the conclusion of its count. A typical example of the use of counters and program interrupt is the scanning of a point in a process at a set time interval, such as every five minutes. The elapsed time counter counts to five minutes, then uses the automatic program interrupt feature to break into the computer program.

## E. PERIPHERAL INPUT-OUTPUT REGISTERS, N AND M

Two 7-bit registers serve as input-output buffers and provide for simultaneous operation of two peripheral devices. They permit overlapping of certain computer functions without loss of time or facility. Input-output activities and internal processing such as arithmetic, making logical decisions, and shifting can be performed simultaneously.

The registers receive and transmit one character at a time. When a character is being inserted into the N or M register from the paper tape reader, or is being sent to a typewriter or punch, it may be either numeric (0-9), alphabetic (A-Z), or some special character. The use of dual peripheral input-output registers in the GE 412 allows a considerable speed-up in performing such output functions as typewriter logging and punching information on paper tape when more than one of the peripheral devices is used.

# IV. INPUT-OUTPUT AND PERIPHERAL UNITS FOR THE GE 412 SYSTEM

Input-output and peripheral units make communication possible between the process, its operators, and the computer system. See figure 11 for a diagram of the GE 412 System input-output and peripheral equipment configuration, Instructions, process data, and manually inserted constants are some of the inputs to the system. Typical outputs are: the log of process variables and calculated results, visual display lights, and control signals in either analog or digital form. The complement of input-output equipment should be selected to most appropriately fill the needs of a particular application.

The various input-output and peripheral equipments will be described under the following three classifications:

Peripheral equipment for computer operation

Peripheral equipment for system operation

Analog and digital input-output

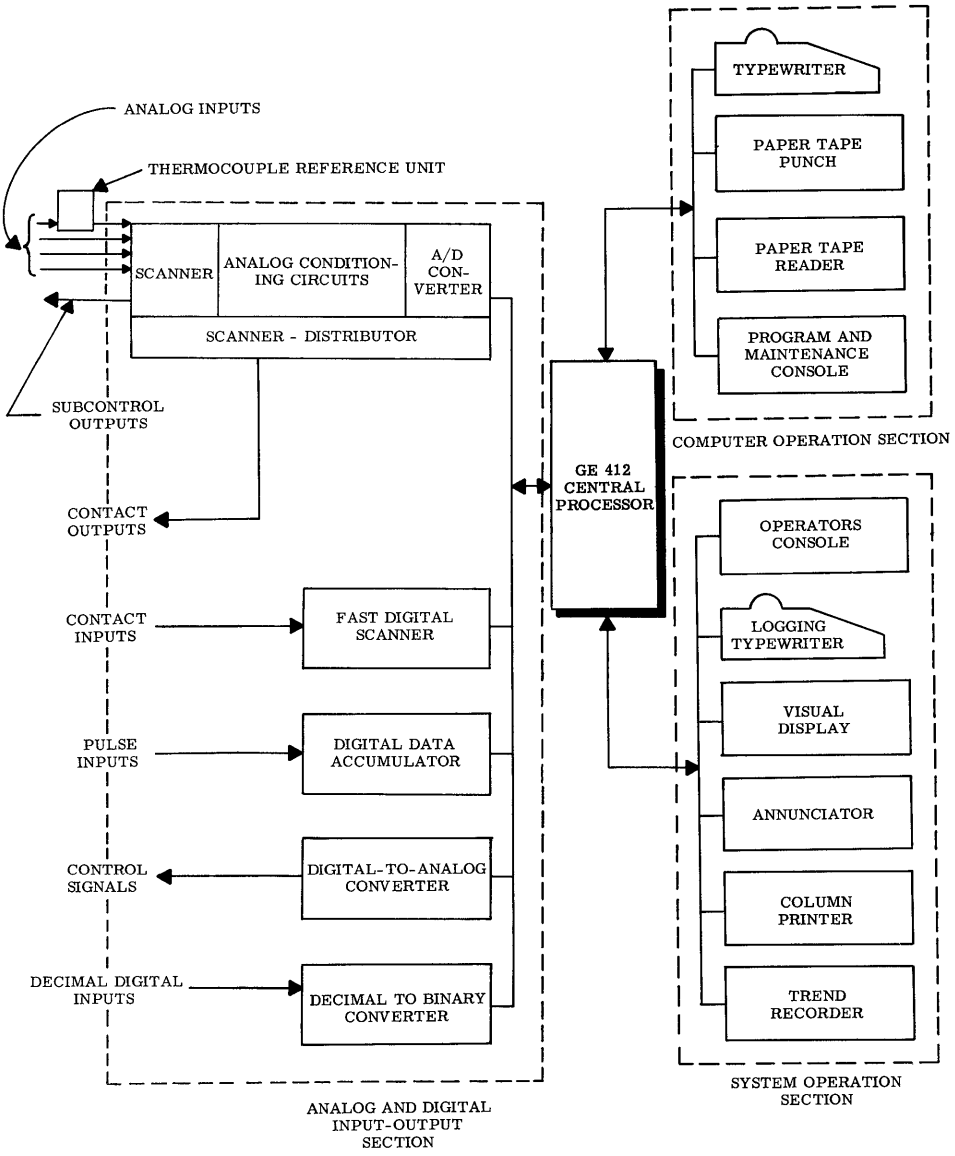



Figure 11. GE 412 System Input-Output Functional Configuration

## A. PERIPHERAL EQUIPMENT FOR COMPUTER OPERATION

Readers, punches, and typewriters are used by the programmers and product service engineers for communication to and from the central processor: for loading, checking, and modifying the programs. These peripheral units are generally located in the same general area as the central processor.

1. Paper Tape Readers

Two types of readers are used for input with the GE 412 System.

a. High Speed Paper Tape Reader

This reader reads standard 8-channel code, punched paper tape at a rate up to 100 characters per second. Programs for the computer are read in by the paper tape reader with special loading routines. The reader inserts information, one character at a time, into the N or M registers. Instructions and data can also be read into the computer by the reader under program control without interrupting normal process monitoring and controlling operations.

b. Low Speed Paper Tape Reader

This reader reads at the rate of 20 characters per second. In all other respects, it is identical to the high speed reader described in paragraph 1a above.

2. Paper Tape Punches

Two types of paper tape punches are used for output with the GE 412 System.

a. High Speed Paper Tape Punch

This paper tape punch produces a standard 8-channel code paper tape record. It is capable of punching on-line at a rate up to 100 characters per second. It operates under program control. Data may be information from the process which is to be analyzed by an off-line computer for additional data processing.

b. Low Speed Paper Tape Punch

This punch operates at the rate of 20 characters per second and can be slaved to the typewriter. In all other respects, it is identical to the high speed punch described in paragraph 2a above.

3. Electric Typewriters

Two types of typewriters are available as output for the GE 412 System. One has alphanumeric printout and the other has only numeric printout.

a. Alphanumeric Typewriter

This typewriter prints both numeric and alphabetic information supplied by the computer at the average rate of 8 characters per second and maximum rate of 10 characters per second. Information and format are both under program control, which means that related information can be printed in easily readable columns. There is a choice of three carriage sizes: 12 inch, 20 inch, and 30 inch. Remote operation of 1000 feet is possible.

b. Numeric Typewriter

The typewriter prints only numeric information. In all other respects it is identical to the alphanumeric typewriter described in paragraph 3a above.

## B. PERIPHERAL EQUIPMENT FOR SYSTEM OPERATION

The input-output equipment described in this section is used mainly in communication between the GE 412 System and the operator.

1. Operators Console

The operators console provides a means of communication between the operator and the process via the computer. Three general types of consoles are available: one designed for office type environment, one of rugged construction for factory use, and one for general purpose. See figures 12, 13, and 14.

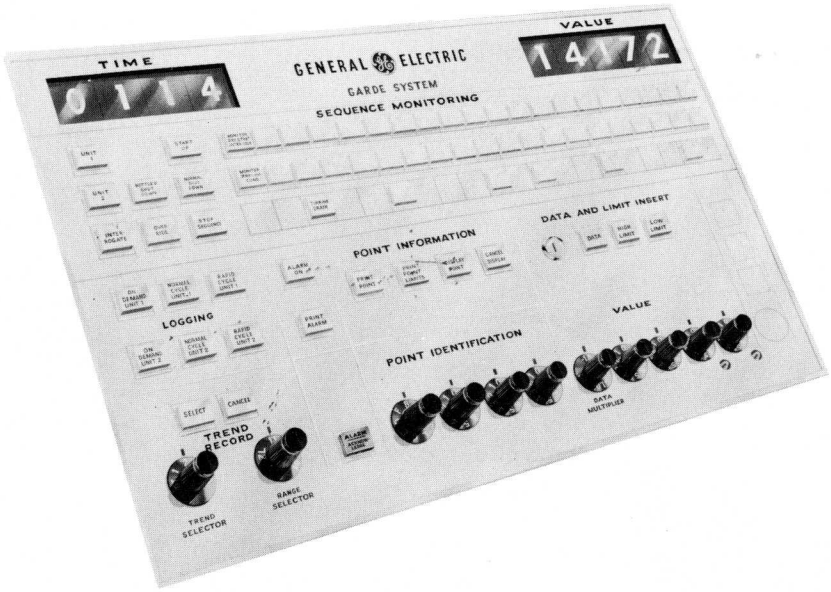



Figure 12. Typical Operators Console, Office Type

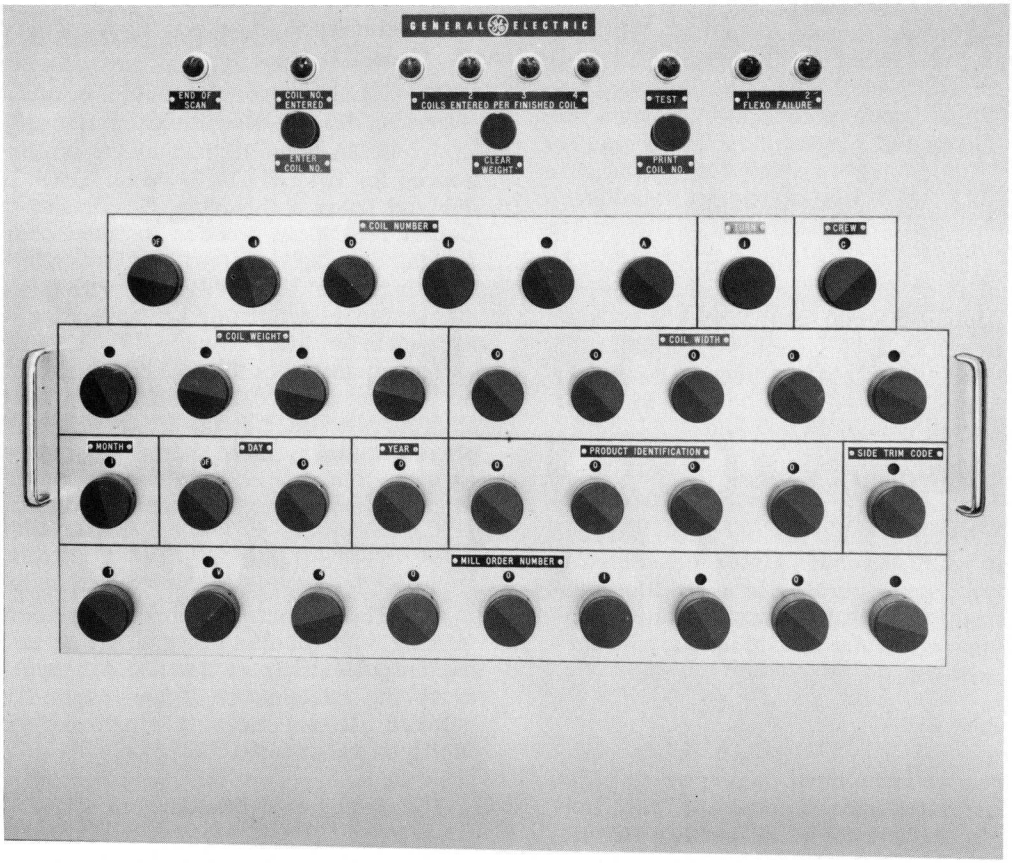



Figure 13. Typical Operators Console, Factory Type


Figure 14. Typical Operators Console, General Purpose Type

2. Column Printers

a. Parallel Entry Column Printer

This printer permits program controlled, line-by-line printout of 11 characters of numerical information per line. Special characters may also be included. It prints in parallel entry fashion at the rate of five lines per second. It is used particularly to print alarm values, but may also be used to log or tabulate other selected values on demand.

b. Serial Entry Column Printer

This printer is used for the same purpose as is the parallel entry column printer described in paragraph 2a above, and operates in a similar manner, with the exceptions that it prints serially at approximately 2 lines a second and prints a 10-character line.

3. Card Reader

The card reader is an input device which reads alphanumeric information into the computer from Hollerith punch cards at the rate of 60 cards a minute, stack fed. The reader has both feed-check and out-of-cards check alarms.

4. Digital Clock

A 24-hour digital clock is used as the time source for the GE 412 System. Clock input pulses are derived from a 60-cycle alternating current source. Output is 6 binary coded decimal characters representing hours, minutes, and seconds. Time may be transferred to the A register with one command. An electronic reset of the seconds counters is provided for synchronizing purposes. Pushbutton step switches are provided for both hour counters and minute counters. A branch command informs the computer when a valid read-in can be obtained. The clock is displayed in binary fashion in the computer racks. If an external display is required, it can be obtained via the scanner and digital display circuitry.

5. Trend Recorders

The computer program can control both graphic (analog) and tabular (digital) trend recorders. Analog output signals of the GE 412 System are used to drive the recorders. Types range from one single-colored pen recorder to single or variable-colored multipen recorders.

6. Peripheral Enclosures

A complete line of enclosures is available. See illustrations, figures 1, 7, and 10.

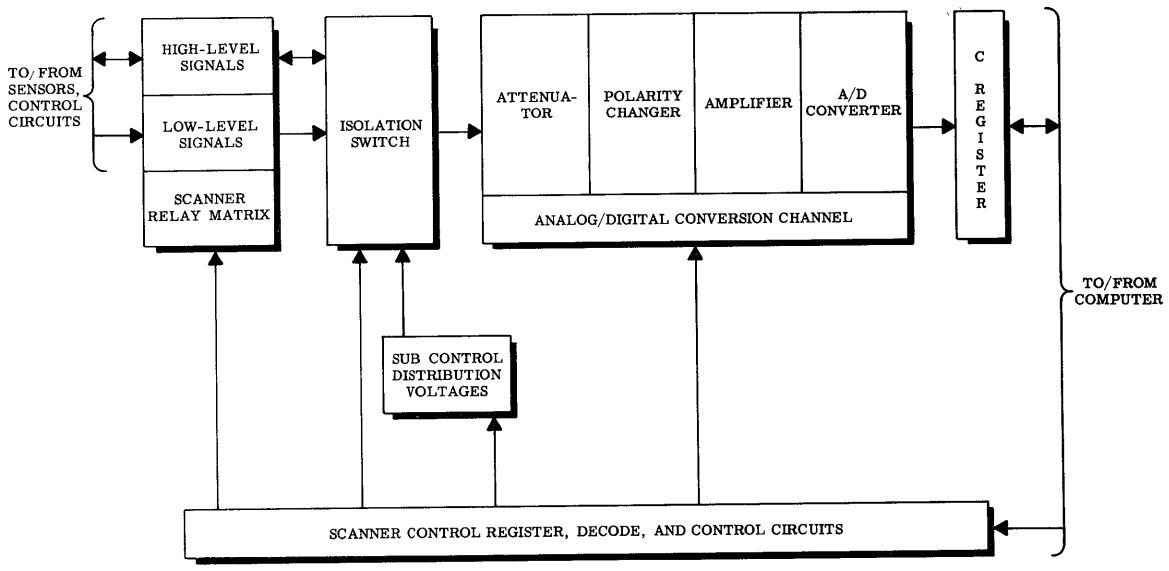



Figure 15. Scanner-Distributor Operation

## C. ANALOG AND DIGITAL INPUT-OUTPUT

The input-output equipment described in this section is used for communication between the process and the computer.

1. Scanner-Distributor

The scanner-distributor is the major input-output device used for communication between the process and the computer. It mates the digital computer to process instruments and controllers for on-line data processing and control. It has basically two modes of operation: analog-to-digital (input), and subcontrol (output). The block diagram, figure 15, illustrates its operation.

The exact employment of the scanner-distributor is dependent on the system of application, but flexibility and facility make it compatible with almost any process sensing and controlling equipment.

As an input device operating under computer program control, the scanner-distributor selects one of many analog inputs from sensors to be scanned, and converts the analog signal to binary digital form for use in the computer. In subcontrol mode, operating under computer program control, it distributes a selected voltage to one of many peripheral devices connected to the system. This distributed voltage will enable the read-in of information from decimal switches and other devices. It also may be used to select and activate outputs from the GE 412 System, such as controlling of analog outputs, contact closure outputs, and visual displays.

The scanner-distributor contains one or more relay matrices. Variation in size permits from 192 to 3072 single input or output contacts. Since analog sensor inputs are two-wire inputs, they each require two scanner contacts, permitting a maximum of 1536.

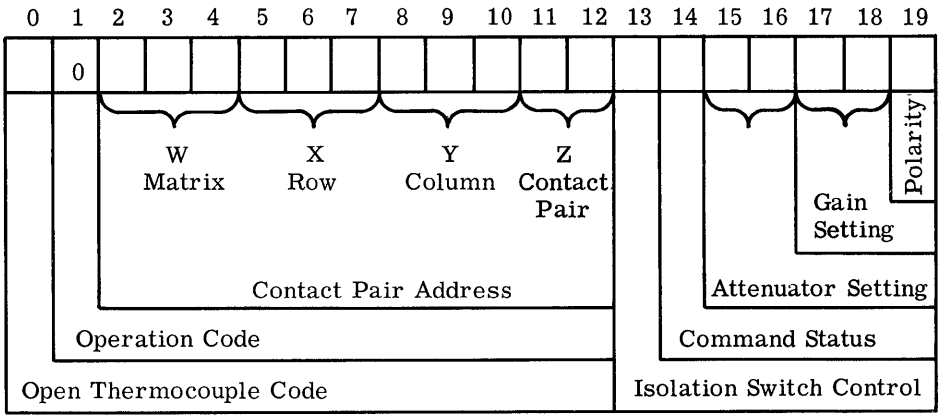



Figure 16. Scanner Command Format for Analog-to-Digital Mode

a. Analog-to-Digital Mode

The characteristics of an analog sensor such as matrix position, polarity, and range are specified by a scanner-command word supplied to the scanner-distributor by the computer. Once the scanner-distributor receives this command, its execution of the operation is independent of the computer, and it thus frees the computer to perform other tasks. The format of the scanner command word for analog-to-digital mode is shown in figure 16.

Bit position 0 is used to control the use of the open thermocouple detection circuitry in the scanner-distributor. Bit position 1 is the operation code and is always a "0" for analog-to-digital operation. Bit positions 2 through 12 specify the position of the relay contact pair that is to be selected. Bit position 13 controls and isolation switch used to separate high level and low level signal inputs. Bit position 14 specifies whether the command status is a new command or a repeat of the previously selected input. It is used to minimize the time required to take several readings of the same point in order to get an average value. Bit positions 15-16 specify one of four attenuator settings, and bit positions 17-18 specify one of four gain settings. This gives a total of 16 different attenuator-gain settings which may be selected. The characteristics of each of the settings are given in table 1. Bit position 19 specifies the polarity of the analog sensor voltage.

The selection and digitizing of an analog sensor input requires approximately 50 milliseconds, or 20 points per second. If a faster scanning speed is required, the scanner-distributor can have 4 or 8 amplifier channels. These options give maximum scanning speeds of 72 and 114 points per second, respectively.

Table 1. Attenuator Gain Setting Characteristics

| Attenuator Setting | Gain Setting | Input Range, Full Scale (Volts dc) |
|---|---|---|
| 00 | 00 | 256 |
| 00 | 01 | 128 |
| 00 | 10 | 64 |
| 00 | 11 | 32 |
| 01 | 00 | 16 |
| 01 | 01 | 8 |
| 01 | 10 | 4 |
| 01 | 11 | 2 |
| 10 | 00 | 1 |
| 10 | 01 | 0.500 |
| 10 | 10 | 0.250 |
| 10 | 11 | 0.125 |
| 11 | 00 | 0.080 |
| 11 | 01 | 0.040 |
| 11 | 10 | 0.020 |
| 11 | 11 | 0.010 |

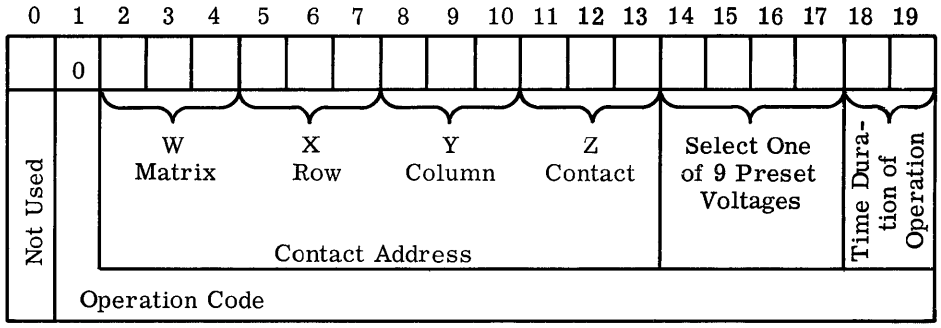



Figure 17. Scanner Command Format for Subcontrol Mode

b. C Register

The C register is physcially a part of the analog-to-digital converter. Functionally, it is dual purpose:

(1) While functioning as an integral part of the analog-to-digital converter, the C register holds the "count" proportional to the input analog voltage. The count range is 0 to 1023 and is indicated in 10 bit positions of the register.

(2) In its other function, the C register serves as a 12-bit computer output register. Acting as a buffer, it holds set-up information for electronic or relay drivers for performing such operations as controlling analog outputs or visual displays.

c. Subcontrol Mode

The scanner-distributor functions as a distributor when it allocates or distributes the proper amplitudes of voltage to selected process controllers. These analog output control signals may be used in the GE 412 System to control the various phases of the process being monitored.

The characteristics of the voltage to be distributed, the duration of distribution, and the desired relay contact is specified in the scanner command. The format of the scanner command for subcontrol operation is shown in figure 17. Bit position 0 is not used. Bit position 1 is the operation code and is a "1" for subcontrol operations. Bit positions 2 through 13 specify the matrix, row, column, and contact position of the distribution point desired. Bit positions 14 through 17 specify one of nine present voltages available for distribution. Bit positions 18 and 19 specify one of four time durations of subcontrol operation. The durations can be 3 1/8 to 100 milliseconds in increments of 3 1/8, depending on system requirements.

Using subcontrol mode of operation, the scanner-distributor can activate many operations. It can activate the conversion of a binary number stored in the C register to an analog signal to be applied to a process controller or trend recorder. It can activate the read-in of digital switches, digital counters, special digital sensors, and similar devices. It can also close or open a relay in order to turn on or off equipment such as a motor. Designated voltages may also be used to step a stepping-switch control device.

A maximum of 3072 points is available as output through the scanner-distributor because the output requires only one contact point, not two as does an analog input.

2. Fast Digital Scanner

The fast digital scanner is an input device which samples the open-closed status of sensor contacts selected at random, in groups of from 1 to 64, at electronic speeds. Each group has 16 contacts, thus a maximum of 1024 contacts is possible.

The fast digital scanner is used where it is desirable to sense the open or closed positions of contacts at very high speeds. Typical applications are the scanning of two-condition elements such as a high-low pressure sensor, high-low temperature sensor, valve open or closed, motor on or off, and brakes open or closed.

3. Digital Data Accumulator

With the digital data accumulator it is possible to count such things as prime feet, damaged feet, off-gage feet, and off-color feet of steel being processed in a continuous strip, or kilowatt-hour counts in steam-electric plants. The accumulations are then read into the computer and used to up-date cummulative totals. The sequential readout of these counters can be accomplished very rapidly to prevent loss of data. See figure 18.

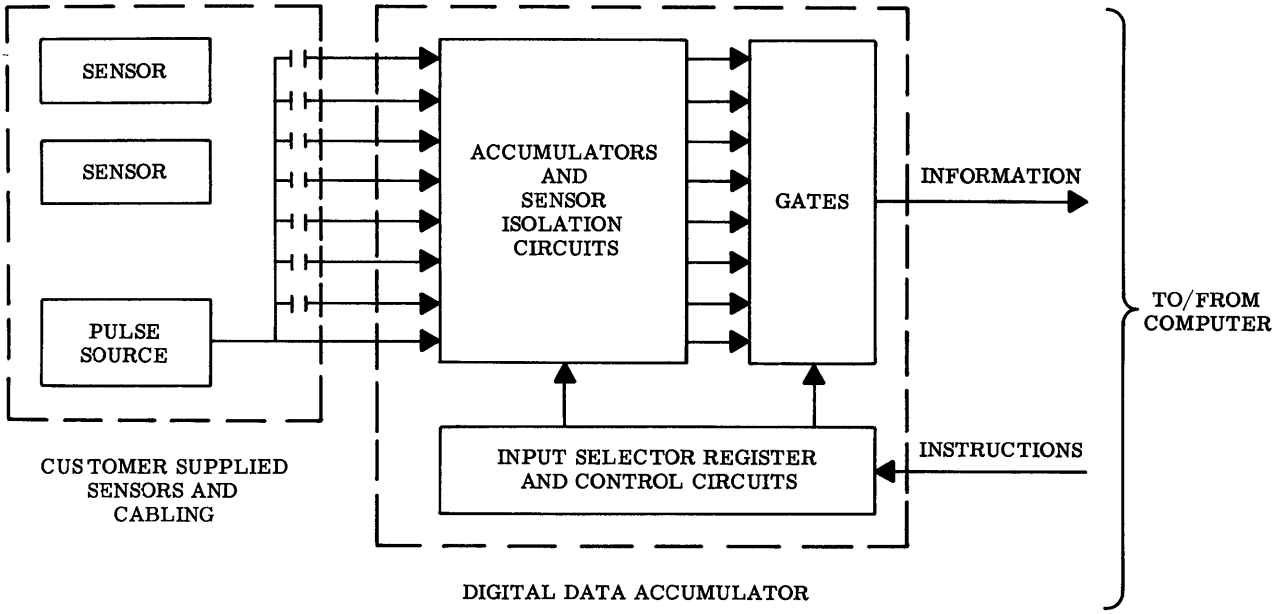



Figure 18. Digital Data Accumulator Block Diagram

4. Digital-to-Analog Converter

The digital-to-analog converter, as the name implies, provides an analog value as a result of a computer operation. It also operates in conjunction with the scanner-distributor to mate the computer to controllers for on-line control. A typical application is the set-point control of various regulators and trend recorder devices.

5. Thermocouple Reference Unit

A thermocouple cold reference junction is available for applications which use thermocouples as sensors. The reference is of a special GE floating design which provides an extremely accurate temperature measurement. The programmer can use this cold reference temperature in calculation of the actual temperature measured by the signal thermocouples.

6. Data Mating Function

Provision is made for the addition of electronics for those applications which require high speed peripheral devices.

# V. QUALITY OF OPERATION

The following features characterize the progress General Electric has made in providing continuous accurate and reliable computer operation in industrial environments:

1. Reliability

Fundamental reliability of basic components of the GE 412 System is assured by rugged industrial design, numerous self-checking features, 100% transistorization, and by conservative circuit design which permits components to operate well below their nominal ratings. For example, transistors are used which have a nominal rating of 50 to 150 milliwatts, but a reduced use rating of 5 to 50 milliwatts.

2. Availability

Equipment availability is even more important than reliability for it includes not only failure rate, but speed of failure diagnosis and speed of equipment or program repair. Most of the GE System's components are capable of being failure-diagnosed by on-line diagnostic routines. System design allows for ready access to test, remove, and replace components. Readily available spare parts and trained personnel permit fast action in returning the system to full operation.

3. Checking Features

a. Open Thermocouple Detection

Normal scanning of a thermocouple doesn't always give an indication of the validity of the signal received from the thermocouple. It is therefore desirable to periodically check the condition of the thermocouple. The most command failure is an open circuit. Under program control, a constant power source may be placed on the thermocouple, and if the circuit is open, the voltage generated will saturate the input amplifier and cause the analog-to-digital converter to overflow. Under normal conditions this constant current source will cause a relatively low additional input voltage and not cause the overflow condition in the converter. The GE 412 System therefore provides for automatic open thermocouple detection under program control.

b. Fail-Safe Outputs

All contact outputs are electrically isolated from each other and from the computer system. All set-point or contact outputs will remain at their set value indefinitely, or until reset under computer program control.

c. Guarded Memory

Write-disconnect switches enable selected portions of drum storage to be electrically disconnected from the write-amplifier circuitry, and thus positively prevent any disturbance of programs or other data stored in those locations.

d. Parity Checks (internal)

To insure error free operation, parity checks are automatically generated or checked for all information flow to or from core and drum storage. A parity error will also stop computer sequencing if the switches in the central processor racks are in proper position.

e. System Alarms

Both stall alarms and overheat alarms are provided to give immediate indication of malfunctioning. An alarm printer prints out time and point identification when an alarm condition occurs, and again when it returns to normal. The computer can be programmed to act on the data sensed by the system and, for example, provide automatic shutdown under certain alarm conditions.

# VI. PROGRAMMING AIDS AND SERVICES

Complete and comprehensive technical services and training courses are available for the GE 412 System.

## A. PROGRAMMING AIDS

Extensive development work has been done and is continually being done to prepare routines to facilitate the writing of process control programs. A programming aids library is set up to assist in the exchange of subroutines and other process computer programming aids. Standard functions which are common from program to program have been written in subroutine form and are available through the library. Basic subroutines which are used frequently in a program may be stored in sections of the computer's storage units, and when the subroutines are needed, a jump can be made to the appropriate location. The subroutine is performed, and upon completion, a return is made to the next instruction of the main program.

1. The General Assembly Program

The most useful of the programming aids is the "General Assembly Program" (GAP). Programming is simplified with this, for the programmer writes his GE 412 program employing symbolic notation for the operation code and address rather than the absolute code of the computer. The symbolic notation is a mnemonic code which is carefully chosen to provide maximum significance to the user. The assembly program translates these mnemonic codes into the code of the computer and produces a program which is ready to read into storage for execution. Such time-critical functions as scanning and logging can be handled in the language of GAP. Symbolic addressing, relative addressing, and pseudoinstructions, as described below, are features of this program.

a. Symbolic Addressing

Symbolic Addressing provides a means of further simplifying GE 412 programming, for it permits storage addresses to be assigned a convenient symbolic notation, then the assembly program automatically assigns storage locations to the symbols. For example, the result of a calculation may give a temperature for Process A. This could be TEMPA. The programmer need only specify the starting address into which the first instruction for the program is to be stored.

b. Relative Addressing

Further programming simplification is achieved through the use of relative addressing. By use of this, a word in memory may be addressed by giving its location relative to some starting point. Thus, if the symbol A has been defined as a particular location in storage, the storage location ten words beyond A can be addressed simply as A+10.

c. Pseudoinstructions

Pseudoinstructions are symbols which resemble actual machine instructions, but instead of being executed by the computer, as a normal instruction would be, are used only by the GAP to provide information for assembling a program. ORG, for example, is recognized by the computer as a pseudoinstruction which indicates the starting point of a program. Use of pseudoinstructions greatly simplifies the writing of a program.

2. The General Compiler

The General Compiler (GECOM) is a unique concept in computer communication which can translate a statement of the program in English or mathematical form into the GAP language. This permits programs to be written in familar terminology rather than in machine code. Use of GECOM permits faster and more efficient programming, and cuts debugging time. It makes a permanent record of the program in its original source language, and lists in detail its transformation to machine instructions. GECOM actually consists of four source languages. One, two, or any combination of these languages may be selected for use.

COBOL — Common Business Oriented Language -- concerned mainly with English language statements related to business data processing.

ALGOL — ALGOrithmic Lanugage -- concerned with algebraic expressions and descriptions of computational processes in mathematical terms. It is of prime importance to the scientist, engineer, and mathematician. Its notations are being accepted internationally.

TABSOL — TABular Systems Oriented Language -- depicts, by means of tables, the relationships of logical decisions which are written in terms of the conditions to be satisfied and the subsequent action to be taken. It is applicable to such diverse fields as manufacturing methods, cost accounting, product engineering, and product control.

FRINGE — File and Report INformation processing GEnerators -- applicable to such uses as incorporating data from various sources into master files of information and extracting the data in various sequences onto printed reports.

The actual translation from GECOM to the GAP language must be done on a GE 225 Computer. GE 225's are available in General Electric's Computing Centers in most major cities throughout the United States. Thus, GECOM can be used to write some of the more general parts of a process control program, while the more tailored special functions can be written in the GAP language.

3. List of Additional Aids

Some of the other service programs or progamming aids are:

a. Service Routines

Decimal to Binary Input Routine

Binary to Decimal Output Routine

Selective Program Trace Routine

Paper Tape Load Routine

Selective Drum Dump Routine

b. Mathematical Routines

General Mathematical Routines such as square root, sine, cosine, log, exponential, and others

Double Precision Arithmetic Routines for Division and Multiplication

c. Diagnostic Routines

## B. TRAINING

Several GE 412 courses are available, each designed to suit a particular type of user need.

1. The GE 412 Programming Course

The purpose of this course is to present the fundamentals of computer programming for the GE 412. The individual subjects covered include: characteristics of a computer system, binary and octal number systems, flow charting, GE 412 commands, equipment configurations, techniques of programming the GE 412 System, programming aids, and class problems. The prerequisite for the programming class is a BS in a technical field, or equivalent, but no prior computer knowledge is required.

The duration of the course is three weeks -- 120 hours of class work. The course is taught at the customer site, at local Industrial Sales Operation or Electric Utility Sales Operation offices of General Electric, or at the Process Computer Section Headquarters at Phoenix, Arizona.

2. The GE 412 Product Service Training Course

The purpose of this course is to train an individual to maintain a GE 412 System. Subjects covered include: computer fundamentals, i.e., number systems, logical design, basic circuits, logic of GE 412 circuitry; execution of commands; operation of input-output equipment; diagnostic programs; and machine fault diagnosis.

Prerequisites for the course include:

a. An electrical engineering degree, or

b. A minimum of two years of formal fundamental electronic training plus two years experience maintaining and servicing electronic systems such as radar, etc., or

c. Six years experience maintaining electronic systems other than computers,

d. Or equivalent.

The duration of this course is fourteen weeks -- 500 hours of class time. The course is taught at the Process Computer Section Headquarters in Phoenix, Arizona.

3. The Concepts Course

The purpose of this course is to describe a basic process computer system, the advantages of automatic control, how this automatic control is accomplished, introduction to computer programming, and a description of a typical GE 412 System. This course is designed for executives, engineers and other plant personnel who desire to gain familiarity with the use of the GE 412 System in process control. The course is of three days duration -- 18 to 20 hours of classroom time. It can be taught at the customer site, at local Industrial Sales Operation or Electric Utility Sales Operation offices of General Electric, or at the Process Computer Section Headquarters in Phoenix, Arizona.

# VII. GENERAL ELECTRIC LIAISON AND INSTALLATION ASSISTANCE

To insure a successful installation and application of an integrated system, liaison, installation, and checkout services by experienced General Electric representatives are available. These include the following:

## A. COMPUTER APPLICATION ENGINEERING LIAISON

An experienced computer application engineer will be assigned for liaison for each GE Computer System. His services will continue from the time of contract initiation through the successful installation and operation of the system.

He provides assistance in preparing system functional and design specifications and in performing analytical and preliminary programming. By describing solutions from an overall standpoint of system reliability, flexibility, and compatibility through tie-in with instrument-controllers and other plant devices, he ensures that the process computers are utilized in as efficient a manner as possible. When required, he conducts or participates in feasibility studies on process control applications and techniques.

## B. ON-SITE CONSULTATION AND INSPECTION

Prior to a GE engineer's visit to the customer plant site, equipment lists, outline drawings, and cable connection drawings will be submitted to the contractor for approval. During site preparation (approximately 90 days before the anticipated equipment delivery), a GE engineer will visit the plant for consultation and inspection service. This will enable installation problems to be resolved and installation and plant erection schedules will be reviewed. A GE installation engineer will provide supplemental advice and surveillance of:

Plant cable routing and handling

System ground technique

Unloading and handling facilities

Availability of system power

## C. SYSTEM INSTALLATION AND CHECKOUT

The installation and checkout of the computer system requires highly trained personnel with extensive computer experience, and thorough familiarity with the customer's system. To this end, personnel assigned to the job during factory test will follow the system through factory acceptance, and then into the field for installation and site testing. All necessary adjustments will be made for on-site operation.

## D. MAINTENANCE SERVICES

Experienced General Electric representatives can provide both preventive and corrective maintenance to assure optimum utilization of the GE System at all times. This service is available on a contract basis.

# VIII. INSTALLATION CONSIDERATIONS

## A. POWER REQUIREMENTS AND CABLING PRACTICES

The successful installation of a GE 412 System requires close adherence to established practices in regard to system power, grounding, and cabling requirements.

The importance of adhering to established practices in cabling installation cannot be overemphasized. Appendix D of this manual contains a complete summary of recommended cabling procedures and considerations. Recommended cabling practices are necessary to insure maximum analog conversion accuracy.

The acceptable grounding configuration requires grounding all components in one place in an attempt to prevent ground loops. All peripheral equipment signal grounds are terminated in the computer, and their routing is accomodated through the system interconnecting cable. The ground bus in the computer will then be connected to a plant grounding grid or copper rod located conveniently near the computer.

## B. HANDLING AND MOUNTING OF GE SYSTEM COMPONENTS

1. Handling

Cabinet assemblies are capable of being moved by:

a. Crane or hoist

Four eyebolts located in the top of each cabinet are provided for lifting the cabinet assemblies by crane or hoist. Spacer bars must be used with the crane hooks to insure a straight upward lift.

b. Dollies (or similar devices)

Whenever dollies (or other rolling devices) are used, the cabinet(s) should be lifted just far enough to place the dolly under each end of the assembly, then the assembly should be either pushed or towed.

2. Mounting

a. Mounting Holes

The cabinet base has mounting holes provided for bolting the cabinet assembly to the floor.

b. Door Clearance

Clearance of 33 inches is required in front of the cabinet(s) in order to have access (by the front door) to remove and replace plug-in cards. Thirty-three inches of clearance are also required in the rear of the cabinet(s) for servicing.

c. Cabling Aid

Covered access slots in the base of each cabinet assembly are located in the front, rear, and ends (under the cabinet). These can be used to assist the installer in pulling cable into the cabinet(s).

# IX. INSTRUCTIONS FOR THE GE 412

The GE 412 operates under the programmed control of over 100 instructions. These instructions are classified into the following categories:

Arithmetic
Data Transfers
Logical
Shift Operations
Unconditional Branches
Conditional Branches
Address Modification
Console Operation and Peripheral Equipment
Clock and Timer Control
Automatic Interrupt
Magnetic Drum
Process Input-Output Equipment
Controller Selector
External Registers
External Effects

The following list defines each instruction and describes its execution. More extensive explanations of instructions and sample problems will be found in the GE 412 Programming Manual. Several rules and explanations apply to the instruction list.

1. In the heading above each instruction is: a three-lettered mnemonic code; the letter(s) Y, K, X, or J; and the execution time as indicated in the following example:

**SUB Y 3**

SUB-- the mneumonic operation code. It is an abbreviated form of the title which, in this case is "SUBTRACT."

Y -- implies the use of an operand address which is located in storage. Some instructions do not require an operand, so for these, no entry is found.

K -- in the "Y" position specifies that a constant is used, such as length of shift or amount of address modification.

X -- specifies that one of the X storage locations must be used in the execution of the instruction. It appears in the heading with Y or K.

J -- specifies the constant, either "1" or "2", used with branch instructions.

3 -- is the word times for execution, and includes the time for the fetching of instruction. One word time is 20 microseconds. Address modification always adds one word time.

2. Descriptions of instructions use the following terminology:

a. Single letter abbreviations refer to registers and storage locations, for example, "A register."

b. Single letters in parentheses preceded by a "C" designate the contents of a register or storage location, for example, "C(A)". Unless specified otherwise, reference is to the total contents, including the sign.

c. Subscripts refer to individual bit positions of a register or storage location, or the contents of those positions. Subscripts are used only when less than the entire register or its contents is intended. For example, "$C(A)_{S,\ 1-17}$" means "the sign and contents of positions 1 through 17 of the A register".

| Abbreviation | Designation | Size and Bit Positions |
|---|---|---|
| A | Arithmetic Register | $A_{(s,\ 1-19)}$, or $A_{(0-19)}$ |
| Q | Auxiliary Register | $Q_{(s,\ 1-19)}$ or $Q_{(0-19)}$ |
| N | Peripheral Register | $N_{(1-7)}$ |
| M | Peripheral Register | $M_{(1-7)}$ |
| X | Automatic modification location | $X_{(7-19)}$ |
| I | Instruction Register | $I_{(S,\ 1-19)}$ or $I_{(0-19)}$ |
| C | Converter Register | $C_{(8-19)}$ |
| P | Program Address Register | $P_{(7-19)}$ |
| Y | Core Storage Location | $Y_{(s,\ 1-19)}$ or $Y_{(0-19)}$ plus parity bit |

3. When a register or part of a register is "cleared" the cleared part is reset to zero.

4. Unless specified otherwise, all instructions can be automatically modified.

5. In all instructions involving the bringing of a word from memory, the word in memory remains unchanged. In all instructions involving the transfer of information from registers, the condition of the register after execution is unchanged unless otherwise stated.

## ARITHMETIC INSTRUCTIONS

The capacity of the A register may be exceeded in execution of Add or Subtract instructions, resulting in a condition known as "overflow". In this event, the overflow indicator is turned on, the high-order (most significant) bit of the result is lost, and the sign of the result is reversed.

**ADD** **Y** **2**

ADD. C(Y) are added algebraically to C(A). The result is placed in A. Y is unchanged.

**SUB** **Y** **3**

SUBTRACT. C(Y) are algebraically subtracted from C(A). The result is placed in A. Y is unchanged.

**DAD** **Y** **3**

DOUBLE LENGTH ADD. If Y is even, C(Y) and $C(Y+1)_{1-19}$ are algebraically added to C(A) and $C(A)_{1-19}$. If Y is odd, C(Y) and $C(Y)_{1-19}$ are algebraically added to C(A) and $C(Q)_{1-19}$. The result is placed in A and $Q_{1-19}$. The sign of Q is set to agree with the sign of A. Y and Y+1 are unchanged. If this instruction is automatically modified, the address after modification determines the result as indicated above.

**DSU** **Y** **5**

DOUBLE LENGTH SUBTRACT. If Y is even, C(Y) and $C(Y+1)_{1-19}$ are algebraically subtracted from C(A) and $C(Q)_{1-19}$. If Y is odd, C(Y) and $C(Y)_{1-19}$ are algebraically subtracted from C(A) and $C(Q)_{1-19}$. The result is placed in A and $Q_{1-19}$. The sign of Q is set to agree with the sign of A. Y and Y+1 are unchanged. If this instruction is automatically modified, the address after modification determines the result as indicated above.

**MPY** **Y** **22 maximum**

MULTIPLY. C(Y) are algebraically multiplied by C(Q). The result is placed in A and $Q_{1-19}$ with the most significant half in A. The sign of Q is the same as the sign of A after multiplication. If A is not set to zero before the MPY command is given, C(A) are added algebraically to the least significant half of the product. Thus, with proper scaling, it is possible to form the value ab + c.

**DVD** **Y** **30**

DIVIDE. C(A) and $C(Q)_{1-19}$ are algebraically divided by C(Y). The quotient is placed in A; the remainder is placed in Q. The sign of the remainder is the sign of the dividend. The magnitude of the divisor must be greater than the magnitude of A. If not, the overflow indicator is turned ON and control is immediately transferred to the next instruction in sequence.

**ADO** **3**

ADD ONE. Plus one is added algebraically to $A_{19}$. If the capacity of A is exceeded, the overflow indicator is turned ON.

**SBO** **3**

SUBTRACT ONE. One is subtracted algebraically from $A_{19}$. If the capacity of A is exceeded, the overflow indicator is turned ON.

## DATA TRANSFER INSTRUCTIONS

**LDA** **Y** **2**

LOAD A. C(Y) replace C(A). Y is not changed.

**STA** **Y** **2**

STORE A. C(A) replace C(Y). A is not changed.

**DLD** **Y** **3**

DOUBLE LENGTH LOAD. If Y is even, the C(Y) and C(Y+1) replace C(A) and C(Q). If Y is odd, C(Y) replace C(Q) and C(A). Y and Y+1 are unchanged. If this instruction is automatically modified, the address after modification determines the result as indicated above.

**DST** **Y** **3**

DOUBLE LENGTH STORE. If Y is even, C(A) and C(Q) replace C(Y) and C(Y+1). If Y is odd, C(Q) replace C(Y). The contents of A and Q are unchanged. If this instruction is automatically modified, the address after modification determines the result as indicated above.

**STO** **Y** **3**

STORE OPERAND ADDRESS. $C(A)_{7-19}$ replace $C(Y)_{7-19}$. $A_{S,\ 1-6}$ and $Y_{S,\ 1-6}$ are unchanged.

**LQA** **3**

LOAD Q FROM A. C(A) replace C(Q). A is unchanged.

**LAQ** **3**

LOAD A FROM Q. C(Q) replace C(A). Q is unchanged.

**XAQ** 3

EXCHANGE A AND Q. C(A) and C(Q) are interchanged.

**MAQ** 3

MOVE A TO Q. C(A) replace C(Q). Zeros replace C(A).

**LDZ** 3

LOAD ZERO INTO A. A is loaded with zeros.

**LDO** 3

LOAD ONE INTO A. A is cleared, and a "1" is placed in $A_{19}$.

**LMO** 3

LOAD MINUS ONE INTO A. A is loaded with "1"s.

**CPL** 3

COMPLEMENT A. Each bit in A is inverted; that is, each "1" is replaced by a zero and each zero is replaced by "1".

**NEG** 3

NEGATE A. The 2's complement (negative value) of A replaces A. If the capacity of A is exceeded, the overflow indicator will be turned ON.

**CHS** 2

CHANGE SIGN OF A. The sign of A is changed. Positions 1-19 of A are unchanged.

**NOP** 3

NO OPERATION. Zero is added to A.

## LOGICAL INSTRUCTIONS

**ORY** **Y** **3**

OR A INTO Y. Each bit of A is examined. If there is a "1" bit in A in a given position, a "1" bit is placed in Y in that position. C(A) and other bit positions of Y are unchanged.

**EXT** **Y** **3**

EXTRACT. Each bit of Y is examined. If there is a "1" bit in Y in a given position, a zero is placed in the corresponding position of A. If there is a zero in a given position of Y, the corresponding position in A is left unchanged. Y is unchanged.

**ANA** **Y** **3**

AND Y TO A. Corresponding bits of A and Y are compared. If the corresponding positions in both A and Y contain a "1", a "1" is placed in that position of A. If either contain a zero, a zero is placed in that position of A.

**ERA** **Y** **3**

EXCLUSIVE OR TO A. Corresponding bits of A and Y are compared. If the corresponding positions in A and Y are alike, a zero is placed in that position of A. If they are unlike, that position is set to a "1".

## SHIFT OPERATIONS INSTRUCTIONS

The shift instructions shift the contents of the A register to the right or left serially (bit by bit) either alone or with C(N), C(M) and/or C(Q). A maximum of 31 places can be shifted. All shift commands vary between two and 12 word times, depending upon the length of the shift. Two word times are required for a shift of 3 bit positions or less. One additional word time is required for each additional 3 bit shift or fraction thereof.

**SRA** **K** **2+**

SHIFT RIGHT A. $C(A)_{1-19}$ are shifted right K places. If A is plus, zeros are inserted in the vacated positions. If A is minus, "1"s are inserted in the vacated positions. Bits shifted out of position 19 are lost. The sign of A is unchanged.

**SLA** **K** **2+**

SHIFT LEFT A. $C(A)_{1-19}$ are shifted K places. Vacated positions of A are filled with zeros. If a non-zero bit is shifted out of position 1, the overflow indicator will be turned ON, and the bit is lost. The sign of A is unchanged.

**SCA** **K** **2+**

SHIFT CIRCULAR A. $C(A)_{1-19}$ are shifted right K places in a circular fashion; that is, the bit shifted out of position 19 is inserted in position 1, replacing the bit shifted out of position 1. The sign of A is not affected.

**SRD** **K** **2+**

SHIFT RIGHT DOUBLE. $C(A)_{1-19}$ and $C(Q)_{1-19}$ together are shifted K places to the right. Bits shifted out of $A_{19}$ shift into $Q_1$. Bits shifted out of $Q_{19}$ are lost. If the sign of A is plus, zeros fill the vacated positions; if the sign of A is minus, "1"s fill the vacated positions. The sign of Q is replaced by the sign of A. The sign of A is unchanged.

**SLD** **K** **2+**

SHIFT LEFT DOUBLE. $C(A)_{1-19}$ and $C(Q)_{1-19}$ together are shifted K places to the left. Bits shifted out of $Q_1$ shift into $A_{19}$. The vacated positions of Q are filled with zeros. If a non-zero bit is shifted out of $A_1$, the overflow indicator is turned ON, and the bit is lost. The sign of Q replaces the sign of A. The sign of Q is unchanged.

**SCD** **K** **2+**

SHIFT CIRCULAR DOUBLE. $C(A)_{1-19}$ and $C(Q)_{1-19}$ together are shifted K places to the right in a circular fashion. Bits shifted out of $A_{19}$ shift into $Q_1$ and those from $Q_{19}$ shift into $A_1$. The sign of A replaces the sign of Q. The sign of A is unchanged.

**SAN** **K** **2+**

SHIFT A AND N RIGHT. $C(A)_{1-19}$ and $C(N)_{1-7}$ together are shifted K places to the right. Bits shifted out of $A_{19}$ shift into $N_1$. Bits shifted out of $N_7$ are lost. If the sign of A is plus, zeros fill the vacated positions of A; if the sign of A is minus, "1"s fill the vacated positions of A. The sign of A is unchanged.

**SNA** **K** **2+**

SHIFT N AND A RIGHT. $C(N)_{1-7}$ and $C(A)_{1-19}$ together are shifted K places to the right. Bits shifted out of $N_7$ shift into $A_1$. Vacated positions in N are filled with zeros. Bits shifted out of $A_{19}$ are lost. The sign of A is unchanged.

**NAD** **K** **2+**

SHIFT N INTO A DOUBLE. $C(N)_{1-7}$, $C(A)_{1-19}$ and $C(Q)_{1-19}$ together are shifted K places to the right. Bits shifted out of $N_7$ shift into $A_1$. Bits shifted out of $A_{19}$ shift into $Q_1$. Bits shifted out of $Q_{19}$ are lost. Vacated positions of N are filled with zeros. The sign of A is unchanged and the sign of A replaces the sign of Q.

**ANQ** **K** **2+**

SHIFT A INTO N AND Q. $C(A)_{1-19}$ are shifted K places to the right into both N and Q. Bits shifted out of $A_{19}$ enter both $Q_1$ and $N_1$. Bits shifted out of $N_7$ and $Q_{19}$ are lost. If the sign of A is plus, the vacated positions of A are filled with zeros. If the sign of A is minus, the vacated positions are filled with "1"s. The sign of A replaces the sign of Q. The sign of A is unchanged.

**SAM** **K** **2+**

SHIFT A AND M RIGHT. $C(A)_{1-19}$ and $M_{1-7}$ together are shifted K places to the right. Bits shifted out of $A_{19}$ shift into $M_1$. Bits shifted out of $M_7$ are lost. If the sign of A is plus, zeros fill the vacated positions of A; if the sign of A is minus, "1"s fill the vacated positions of A. The sign of A is unchanged.

**SMA** **K** **2+**

SHIFT M AND A RIGHT. $M_{1-7}$ and $A_{1-19}$ together are shifted K places to the right. Bits shifted out of $M_7$ shift into $A_1$. Vacated positions in M are filled with zeros. Bits shifted out of $A_{19}$ are lost. The sign of A is unchanged.

**MAD** **K** **2+**

SHIFT M INTO A DOUBLE. $C(M)_{1-7}$, $C(A)_{1-19}$, and $C(Q)_{1-19}$ together are shifted K places to the right. Bits shifted out of $M_7$ shift into $A_1$. Bits shifted out of $A_{19}$ shift into $Q_1$. Bits shifted out of $Q_{19}$ are lost. Vacated positions of M are filled with zeros. The sign of A is unchanged and the sign of A replaces the sign of Q.

**AMQ** **K** **2+**

SHIFT A INTO M AND Q. $C(A)_{1-19}$ are shifted K places to the right into both M and Q. Bits shifted out of A enter both $Q_1$ and $M_1$. Bits shifted out of $M_7$ and $Q_{19}$ are lost. If the sign of A is plus, the vacated positions of A are filled with zeros; if the sign of A is minus, the vacated positions are filled with "1"s. The sign of A replaces the sign of Q. The sign of A is unchanged.

**ANM** **K** **2+**

SHIFT A INTO N AND M. $C(A)_{1-19}$ are shifted K places to the right into both N and M. Bits shifted out of $A_{19}$ enter both $N_1$ and $M_1$. Bits shifted out of $N_7$ and $M_7$ are lost. If the sign of A is plus, the vacated positions of A are filled with zeros; if the sign of A is minus, vacated positions are filled with "1"s.

**NAM** **K** **2+**

SHIFT N TO A TO M. $C(N)_{1-7}$, $C(A)_{1-19}$, and $C(M)_{1-7}$ are together shifted K places to the right. Bits shifted out of $N_7$ shift into $A_1$, and bits shifted out of $A_{19}$ shift into $M_1$. Zeros are shifted into $N_1$, and bits shifted out of $M_7$ are lost.

**MAN** **K** **2+**

SHIFT M TO A TO N. $C(M)_{1-7}$, $C(A)_{1-19}$, and $C(N)_{1-7}$ are together shifted K places to the right. Bits shifted out of $M_7$ shift into $A_1$, bits shifted out of $A_{19}$ shift into $N_1$ and bits shifted out of $N_7$ are lost. Zeros fill the vacated positions of M.

**NOR** **K** **2+**

NORMALIZE A. If R, the number of leading zeros of $A_{1-19}$ is less than K, $C(A)_{1-19}$ are shifted left R places, and K-R replaces $C(0000)_{15-19}$. If R is greater than or equal to K, $C(A)_{1-19}$ are shifted left K places, and zeros replace $C(0000)_{15-19}$. C(0000)s, 1-14 are always set to zero. Vacated positions of A are filled with zeros. The sign of A is unchanged.

**DNO** **K** **2+**

DOUBLE LENGTH NORMALIZE. If R (the number of leading zeros of A) is less than K, $C(A)_{1-19}$ and $C(Q)_{1-19}$ are shifted left R places, and K-R replaces C(0000) 15-19. If R is greater than or equal to K, $C(A)_{1-19}$ and $C(Q)_{1-19}$ are shifted left K places and zeros replace $C(0000)_{15-19}$. C(0000)s, 1-14 are always set to zero. Bits shifted out of $Q_1$ shift into $A_{19}$. Vacated positions of Q are filled with zeros. The sign of Q replaces the sign of A. The sign of Q is unchanged.

## UNCONDITIONAL BRANCH INSTRUCTIONS

**BRU** **Y** **1**

BRANCH. Control is transferred to the instruction located at Y; i.e., Y becomes the address of the next instruction. $C(I)_{7-19}$ are transferred to $C(P)_{7-19}$.

**SPB** **Y, X** **2**

STORE P AND BRANCH. $C(P)_{7-19}$, replace $C(X)_{7-19}$, and control is transferred to the instruction located at Y, i.e., Y becomes the address of the next instruction. This instruction can not be automatically modified since bits 5 and 6 are used to identify the particular X location.

## CONDITIONAL BRANCH INSTRUCTIONS

A conditional branch instruction will transfer the program control to one of two locations relative to the location of the branch instruction itself. Control will be transferred to either the first or second sequential instruction. Each conditional branch instruction must specify a constant J which can equal 1 or 2. The presence or absence of the specified condition and the constant C determine the next instruction to be executed. With the branch instruction located at location L, the following indicates the location of the instruction to which control is transferred.

| J | Condition | Location of Next Instruction | |
|---|---|---|---|
| 1 | Present | L+1 | Normal Branch |
| 1 | Absent | L+2 | Alternate Branch |
| 2 | Present | L+2 | Normal Branch |
| 2 | Absent | L+1 | Alternate Branch |

**BPL** **J** **2**

BRANCH ON PLUS. Branch to location L + J if the sign of A is plus. (Zero is considered to be plus.) Take the alternate branch if the sign of A is minus. A is unchanged by this instruction.

**BZE** J 2

BRANCH ON ZERO. Branch to location L + J if C(A) are zero. Take the alternate branch if C(A) are not zero. A is unchanged by this instruction.

**BEV** J 2

BRANCH ON EVEN. Branch to location L + J is A is even. A is even if $C(A)_{19}$ are zero. Take the alternate branch if A is odd. A is unchanged by this instruction.

**BOV** J 2

BRANCH ON OVERFLOW. Branch to location L+J if the overflow indicator is on. Take the alternate branch if the overflow indicator is off. This instruction turns the overflow indicator off.

**BPC** J 2

BRANCH ON PARITY, CORE. Branch to location L + J if the core parity error indicator is ON and the core parity error circuit is set. The parity error circuit will then be reset but the indicator will remain ON. Take the alternate branch if the core parity error circuit is not ON.

**BPD** J 2

BRANCH ON PARITY, DRUM. Branch to location L + J if the drum parity error indicator is ON and the drum parity error circuit is set. The parity error circuit will then be reset but the indicator will remain ON. Take the alternate branch if the drum parity error circuit is not ON.

**BPN** J 2

BRANCH ON PARITY, READER N. Branch to location L + J if the paper tape N parity error indicator is on, and turn the indicator off. Take the alternate branch if the paper tape N parity error indicator is off. This instruction turns the indicator off.

**BPM** J 2

BRANCH ON PARITY, READER M. Branch to location L + J if the paper tape M parity error indicator is on, and turn the indicator off. Take the alternate branch if the paper tape M parity error indicator is off. This instruction turns the indicator off.

## ADDRESS MODIFICATION INSTRUCTIONS

**INX** **K, X** **3**

INCREMENT X BY K. K, $C(I)_{7-19}$, is added absolutely to $C(X)_{7-19}$, and the result replaces $C(X)_{7-19}$. Any carry from position 7 of X is lost. This instruction can not be automatically modified, since bit positions 5 and 6 are used to identify the particular address modification word.

**BXH** **—K, X** **3**

BRANCH IF X IS HIGH OR EQUAL. If $C(X)_{7-19}$ are larger than or equal to K, the computer takes the next sequential instruction; if $C(X)_{7-19}$ are less than K the computer skips the next instruction and executes the second sequential instruction. X is not changed. This instruction can not be automatically modified since bits 5 and 6 are used to identify the particular index location. (Note: K is required to be the 2's complement of the desired test value. This requirement is automatically taken care of by the General Assembly Program.)

**BXL** **—K, X** **3**

BRANCH IF X IS LOW. If $C(X)_{7-19}$ are less than K, the computer takes the next sequential instruction; if $C(X)_{7-19}$ are larger than or equal to K, the computer skips the next instruction and executes the second sequential instruction. X is unchanged. This instruction can not be automatically modified since bits 5 and 6 are used to identify the particular X location. (Note: K is required to be the 2's complement of the desired test value. This requirement is automatically taken care of by the General Assembly Program.)

## CONSOLE OPERATION AND PERIPHERAL EQUIPMENT INSTRUCTIONS

The GE 412 has two independent input-output lines, line M and line N, which operate through the registers M and N. A given peripheral is attached to either line M or line N, and operates only by instructions which refer to its line.

**RCS** **2**

READ CONTROL SWITCHES. Each of the 20 manually "set A" control switches is examined. If a switch is DOWN (on), a "1" bit is placed in the corresponding position of A; otherwise the corresponding position in A is not altered. A should normally be cleared before this instruction is given.

**BRD** J 2

BRANCH ON DEMAND. Branch to location L + J if the "Demand" button on the computer console has been depressed. Take the alternate branch if the button has not been depressed.

**OFN** 2

PERIPHERALS ON LINE N OFF. All selected peripheral devices connected to register N are dropped out. This operation requires 100 milliseconds.

**OFM** 2

PERIPHERALS ON LINE M OFF. All selected peripheral devices connected to register M are dropped out. This operation requires 100 milliseconds.

**TYN** 2

TYPE ON LINE N. This instruction will cause the 7-bit coded character in N to be typed or typed and punched, depending upon which device or combination of devices is connected to the computer.

**TYM** 2

TYPE ON LINE M. This instruction will cause the 7-bit coded character in M to be typed or typed and punched, and depending upon which device or combination of devices is connected to the computer.

**RPN** 2

READ PAPER TAPE ON LINE N. N is cleared and one 7-bit coded character is read into N. This command is used to read paper tape or punched cards.

**RPM** 2

READ PAPER TAPE ON LINE M. M is cleared and one 7-bit coded character is read into M. This command is used to read paper tape or punched cards.

**PPN** 2

PUNCH PAPER TAPE ON LINE N. The 7-bit coded character in N is punched, providing a paper tape punch was selected by the SEL instruction. N is not changed. This command is not used when a paper tape punch is driven by a typewriter.

**PPM** 2

PUNCH PAPER TAPE ON LINE M. The 7-bit coded character in M is punched, providing a paper tape punch was selected by the SEL instruction. N is not changed. This command is not used when a paper tape punch is driven by a typewriter.

**BNR** J 2

BRANCH ON N REGISTER READY. Branch to location L + J if N is available for input-output (if the last TYN, RPN, PPN, SEL, or OFN instruction has been completed). Take the alternate branch if N is not available.

**BMR** J 2

BRANCH ON M REGISTER READY. Branch to location L + J if M is available for input-output (if the last TYM, RPM, PPM, SEL, or OFM instruction has been completed). Take the alternate branch if M is not available.

**SEL** 2

SELECT PERIPHERAL DEVICE. This command selects a peripheral device (typewriter, paper tape reader, paper tape punch) specified by $C(N)_{2-7}$. $C(N)_1$ must be a zero. Although this command operates through the N register, it is used to select devices for both the N and M registers. The N register is unavailable for use until a BNR is received. (Approximately 80 ms.) The selected device is unavailable for use until approximately 100 ms.

## CLOCK AND TIMER CONTROL INSTRUCTIONS

**LT1** 2

LOAD TIME COUNTER 1. $C(A)_{7,\ 10,\ 12-19}$ are loaded into elapsed time counter 1, and count initiated.

**LT2** **2**

LOAD TIME COUNTER 2. $C(A)_{7, 10, 12-19}$ are loaded into elasped time counter 2, and count initiated.

**LT3** **2**

LOAD TIME COUNTER 3. $C(A)_{7, 10, 12-19}$ are loaded into elapsed time counter 3, and count initiated.

**LT4** **2**

LOAD TIME COUNTER 4. $C(A)_{7, 10, 12-19}$ are loaded into elapsed time counter 4, and count initiated.

**RCL** **2**

READ DITIGAL CLOCK. The 20 bits defining the time indicated by the real-time digital clock are read into $A_{0-19}$. The command should be preceded by a successful BCL command.

**BCL** **J** **2**

BRANCH ON CLOCK READY. Branch to location L + J if a valid read-in can be obtained from the digital clock. Take the alternate branch if not.

**BT1** **J** **2**

BRANCH ON TIME COUNTER 1 OVERFLOW. Branch to location L + J if elapsed time counter 1 has completed its count. Take the alternate branch if the counter has not.

**BT2** **J** **2**

BRANCH ON TIME COUNTER 2 OVERFLOW. Branch to location L + J if elapsed time counter 2 has completed its count. Take the alternate branch if the counter has not.

**BT3** J 2

BRANCH ON TIME COUNTER 3 OVERFLOW. Branch to location L+J if elapsed time counter 3 has completed its count. Take the alternate branch if the counter has not.

**BT4** J 2

BRANCH ON TIME COUNTER 4 OVERFLOW. Branch to location L + J if elapsed time counter 4 has completed its count. Take the alternate branch if the counter has not.

## AUTOMATIC INTERRUPT INSTRUCTIONS

**AI1** 2

SELECT AUTOMATIC INTERRUPT 1. This command enables only priority level 1 interrupt. Interrupts cannot occur until PAI command has been executed.

**AI2** 2

SELECT AUTOMATIC INTERRUPT 2. This command enables only priority level 1 interrupts and priority level 2 interrupts. Interrupts cannot occur until a PAI command has been executed.

**AI3** 2

SELECT AUTOMATIC INTERRUPT 3. This command enables priority level 1, priority level 2, and priority level 3 interrupts. Interrupts cannot occur until a PAI command has been executed.

**PAI** 2

PERMIT AUTOMATIC INTERRUPT. This instruction permits the previously selected priority level (AI1, AI2, AI3 instructions) to initiate automatic interrupt after the execution of the next instruction.

**IAI** **2**

INHIBIT AUTOMATIC INTERRUPT. This instruction forces the computerto ignore all interrupts. Interrupt conditions will not be lost, but will be stored in the interrupt register until such time as a PAI instruction is executed.

**SSA** **2**

SET STALL ALARM. This instruction is used to periodically set a time delay device. When the time delay expires, an alarm condition prevails. The time delay device can be set manually.

## MAGNETIC DRUM INSTRUCTIONS

**LDC** **2**

LOAD DRUM CONTROL REGISTER. The drum controller command register is loaded from C(A) with a drum command word. The command word specifies the beginning drum track, the number (8 or less) of consecutive tracks to be accessed, the starting core memory address, and whether reading or writing is to be performed and initiates transfer. The first address which the magnetic drum accesses in the core must be one of the 128 fixed addresses.

**BDC** **J** **2**

BRANCH ON DRUM OPERATION COMPLETE. Branch to location L + J if the drum controller is ready. Take the alternate branch if the drum controller is not ready.

## PROCESS INPUT-OUTPUT EQUIPMENT INSTRUCTIONS

**LSC** **3 or 4**

LOAD SCANNER CONTROL REGISTER. The scanner control register is cleared and then loaded with C(A). A is not changed. The loading will initiate a new scanner-distributor operation.

**BSC** **J** **2**

BRANCH ON SCANNER OPERATION COMPLETE. Branch to location L + J if the scanner-distributor has completed its operation. Take the alternate branch if the operation is not complete.

**BCO** **J** **2**

BRANCH ON CONVERTER OVERFLOW. Branch to location L + J if the analog-to-digital converter overflow indicator is on. Take the alternate branch if the overflow indicator is not on. The LSC instruction will reset the overflow condition.

**RCV** **3 or 4**

READ CONVERTER. $C(C)_{10-19}$ replace $C(A)_{10-19}$. C(C) are not changed unless in multichannel operation.

**RDG** **2**

READ DIGITAL INPUT. Two 4-bit binary coded decimal input characters selected by the scanner are read into $A_{0-7}$ with $A_0$ holding the most significant bit. The RDG command should be preceded by a successful BSC command. The initial contents of $A_{0-7}$ must be zero.

**LCA** **2**

LOAD CONVERTER REGISTER FROM A. $C(A)_{8-19}$ (with $A_{19}$ containing the least significant bit) are transferred to C. C is automatically cleared by this instruction prior to the transfer. A is not changed.

**LDS** **3 or 4**

LOAD DIGITAL SCAN CONTROL REGISTER. Select the digital fast scanner and disconnect any previously selected fast access device. $C(A)_{14-19}$ replace the contents of the digital fast scan control register. A is not changed. The contents of the control register in turn initiate the selection of a fast scan digital group. A RFA instruction is required to read this group into $A_{0, 4-19}$. The group consists of 16 bits in position 4-19 plus a validity bit in the zero position. A validity bit of zero means that the group is not valid. The digital fast scanner remains selected until disconnected.

**LAC** **3 or 4**

LOAD ACCUMULATOR SCAN CONTROL REGISTER. Select the digital data accumulator and disconnect any previously selected fast access device. C(A) replace the contents of the digital data accumulator scan control register. A is not changed. The contents of the control register in turn initiate the selection of an accumulator register. A RFA instruction is required to read the count from this accumulator into A. The digital data accumulator remains selected until disconnected.

**LXX** **3 or 4**

LOAD FAST ACCESS DEVICE CONTROL REGISTER. (This represents any instruction to be added as necessary for additional fast-access devices.) Select the input-output device and disconnect any previously selected device. C(A) replace the contents of the device's control register. A is not changed. The contents of the control register in turn initiate the selection of an external register. A RFA instruction is required to read the contents of this register into A. The device remains selected until disconnected.

**RFA** **3 or 4**

READ FAST ACCESS DEVICE. The contents of the register selected by the fast access device replace the C(A). When used with some devices, the control register is incremented, then it selects the next register so that registers may be read sequentially by repeated RFA instructions.

**OFA** **2**

FAST ACCESS DEVICE OFF. Any selected fast access device is disconnected.

## CONTROLLER SELECTOR INSTRUCTIONS

This class of instructions initiates and controls direct communication between the GE 412 core storage and specific peripheral devices.

**LCS** **D** **3 or 4**

LOAD CONTROLLER SELECTOR. Load the control registers of controller selector D from the next two sequential core locations. The constant D specifies which of 4 controller selectors to use. This command initiates the transfer of information between core storage and the device(s) connected to the controller selector.

**BCS** **E+J, D** **2**

BRANCH ON CONTROLLER SELECTOR. Branch to location L + J if the condition specified by E is true for controller selector D. Take the alternate branch if condition E is false. E specifies one of 8 conditions applicable to the controller selector D.

## EXTERNAL REGISTER INSTRUCTIONS

An unspecified number of external registers may be used as part of the GE 412 System. Instructions are available for each register to:

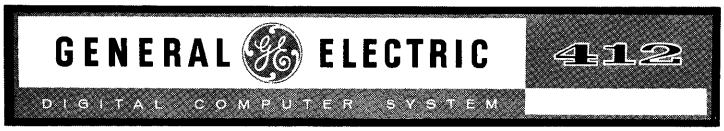
Read external register

Branch on external condition

Load external register.

## EXTERNAL EFFECTS INSTRUCTIONS

A number of unassigned external effects instructions are available for general use.



# APPENDIX A TABLE OF INSTRUCTIONS

| Mnemonic Code | Command | Operand or Constant | Execution Time (Word-Times) | Can Be Auto. Modified | Page No. Reference |
|---|---|---|---|---|---|
| ADD | Add | Y | 2 | x | 34 |
| ADO | Add one | | 3 | | 35 |
| AI1 | Select automatic interrupt 1 | | 2 | | 48 |
| AI2 | Select automatic interrupt 2 | | 2 | | 48 |
| AI3 | Select automatic interrupt 3 | | 2 | | 48 |
| AMQ | Shift A into M and Q | K | 2+ | x | 41 |
| ANA | And Y to A | | 3 | | 38 |
| ANM | Shift A into N and M | K | 2+ | x | 41 |
| ANQ | Shift A into N and Q | K | 2+ | x | 40 |
| BCL | Branch on clock ready | J | 2 | | 47 |
| BCO | Branch on converter overflow | J | 2 | | 50 |
| BCS | Branch on controller selector | E+J, D | 2 | | 51 |
| BDC | Branch on drum operation complete | J | 2 | | 49 |
| BEV | Branch on even | J | 2 | | 43 |
| BMR | Branch on M register ready | J | 2 | | 46 |
| BNR | Branch on N register ready | J | 2 | | 46 |
| BOV | Branch on overflow | J | 2 | | 43 |
| BPC | Branch on parity, core | J | 2 | | 43 |
| BPD | Branch on parity, drum | J | 2 | | 43 |
| BPL | Branch on plus | J | 2 | | 42 |
| BPM | Branch on parity, reader M | J | 2 | | 43 |
| BPN | Branch on parity, reader N | J | 2 | | 43 |
| BRD | Branch on demand | J | 2 | | 45 |
| BRU | Branch | Y | 1 | x | 42 |
| BSC | Branch on scanner operation complete | J | 2 | | 49 |
| BT1 | Branch on time counter 1 overflow | J | 2 | | 47 |
| BT2 | Branch on time counter 2 overflow | J | 2 | | 47 |

| Mnemonic Code | Command | Operand or Constant | Execution Time (Word-Times) | Can Be Auto. Modified | Page No. Reference |
|---|---|---|---|---|---|
| BT3 | Branch on time counter 3 overflow | J | 2 | | 48 |
| BT4 | Branch on time counter 4 overflow | J | 2 | | 48 |
| BXH | Branch if X is high or equal | -K, X | 3 | | 44 |
| BXL | Branch if X is low | -K, X | 3 | | 44 |
| BZE | Branch on zero | J | 2 | | 43 |
| CHS | Change sign of A | | 2 | | 37 |
| CPL | Complement A | | 3 | | 37 |
| DAD | Double length add | Y | 3 | x | 35 |
| DLD | Double length load | Y | 3 | x | 36 |
| DNO | Double length normalize | K | 2+ | | 41 |
| DST | Double length store | Y | 3 | x | 36 |
| DSU | Double length subtract | Y | 5 | x | 35 |
| DVD | Divide | Y | 30 | x | 35 |
| ERA | Exclusive or to A | Y | 3 | x | 38 |
| EXT | Extract | Y | 3 | x | 38 |
| IAI | Inhibit automatic interrupt | | 2 | | 49 |
| INX | Increment X by K | K, X | 3 | | 44 |
| LAC | Load accumulator scan control register | | 3 or 4 | | 50 |
| LAQ | Load A from Q | | 3 | | 36 |
| LCA | Load converter register from A | | 2 | | 50 |
| LCS | Load controller selector | D | 3 or 4 | | 51 |
| LDA | Load A | Y | 2 | x | 36 |
| LDC | Load drum control register | | 2 | | 49 |
| LDO | Load one into A | | 3 | | 37 |
| LDS | Load digital scan control register | | 2 | | 50 |
| LDZ | Load zero into A | | 3 | | 37 |
| LMO | Load minus one into A | | 3 | | 37 |
| LQA | Load Q from A | | 3 | | 36 |
| LSC | Load scanner control register | | 3 or 4 | | 49 |

| Mnemonic Code | Command | Operand or Constant | Execution Time (Word-Times) | Can Be Auto. Modified | Page No. Reference |
|---|---|---|---|---|---|
| LT1 | Load time counter 1 | | 2 | | 46 |
| LT2 | Load time counter 2 | | 2 | | 47 |
| LT3 | Load time counter 3 | | 2 | | 47 |
| LT4 | Load time counter 4 | | 2 | | 47 |
| LXX | Load fast access device control register | | 2 | | 51 |
| MAD | Shift M into A double | K | 2+ | x | 40 |
| MAN | Shift M to A to N | K | 2+ | x | 41 |
| MAQ | Move A to Q | | 3 | | 37 |
| MPY | Multiply | Y | 22 max. | x | 35 |
| NAD | Shift N into A double | K | 2+ | x | 40 |
| NAM | Shift N to A to M | K | 2+ | x | 41 |
| NEG | Negate A | | 3 | | 37 |
| NOP | No operation | | 3 | | 37 |
| NOR | Normalize A | K | 2+ | x | 41 |
| OFA | Fast Access Device off | | 2 | | 51 |
| OFM | Peripherals on line M off | | 2 | | 45 |
| OFN | Peripherals on line N off | | 2 | | 45 |
| ORY | Or A into Y | Y | 3 | x | 38 |
| PAI | Permit automatic interrupt | | 2 | | 48 |
| PPM | Punch paper tape on line M | | 2 | | 46 |
| PPN | Punch paper tape on line N | | 2 | | 46 |
| RCL | Read digital clock | | 2 | | 47 |
| RCS | Read control switches | | 2 | | 44 |
| RCV | Read converter | | 3 or 4 | | 50 |
| RDG | Read digital input | | 2 | | 50 |
| RFA | Read fast access device | | 3 or 4 | | 51 |
| RPM | Read paper tape on line M | | 2 | | 45 |
| RPN | Read paper tape on line N | | 2 | | 45 |
| SAM | Shift A and M right | K | 2+ | x | 40 |

| Mnemonic Code | Command | Operand or Constant | Execution Time (Word-Times) | Can Be Auto. Modified | Page No. Reference |
|---|---|---|---|---|---|
| SAN | Shift A and N right | K | 2+ | x | 39 |
| SBO | Subtract one | | 3 | | 35 |
| SCA | Shift circular A | K | 2+ | x | 39 |
| SCD | Shift circular double | K | 2+ | x | 39 |
| SEL | Select peripheral device | | 2 | | 46 |
| SLA | Shift left A | K | 2+ | x | 39 |
| SLD | Shift left double | K | 2+ | x | 39 |
| SMA | Shift M and A right | K | 2+ | x | 40 |
| SNA | Shift N and A right | K | 2+ | x | 40 |
| SPB | Store P and branch | Y, X | 2 | | 42 |
| SRA | Shift right A | K | 2+ | x | 38 |
| SRD | Shift right double | K | 2+ | x | 39 |
| SSA | Set stall alarm | | 2 | | 49 |
| STA | Store A | Y | 2 | x | 36 |
| STO | Store operand address | Y | 3 | x | 36 |
| SUB | Subtract | Y | 3 | x | 34 |
| TYM | Type on line M | | 2 | | 45 |
| TYN | Type on line N | | 2 | | 45 |
| XAQ | Exchange A and Q | | 3 | | 37 |

# APPENDIX B CABLING PRACTICE

Proper functioning of the GE 412 Process Computer System is dependent upon adherence to established practices in cabling installation. A summary of recommended procedures and considerations is provided in the following paragraphs.

## A. SYSTEM CABLING

Cabling should always be installed in the best manner to protect it from excessive heat, moisture, and mechanical damage. It should be run in conduit or troughs so that it is completely supported and is not subjected to excessive flexing or bending. The troughs may be constructed or expanded metal. If conduit is required, the conduit runs should be laid out to avoid low points where moisture can accumulate.

All system units and cabling must be mounted and located to avoid coupling to sources of high intensity electric transients. Thyratron and ignitron equipment and cables are especially noisy and are to be avoided. While considerable design effort has been applied to the GE 412 computer to obtain electrical noise immunity, good engineering practice dictates that wherever possible, such noise interference be suppressed at the source.

1. Categories of Cabling

Intercabling may be subdivided into three major categories. Each category may require somewhat different treatment and will require isolation from other categories to avoid interference problems. The categories are:

Power wiring

Control and intra-system wiring

Analog data wiring

2. Equipment

All troughs or conduits should be bonded together with good low resistance joints. The conduits should be connected to the industrial or building ground system.

3. Shielding

All digital inputs, controls, intra-system, and analog data cables between the various units of the industrial computer equipment and the associated signal sources which feed into and out of it must be shielded. The shield must be covered with an insulated sheath appropriate to the environment to which each cable is exposed. It is important that the shields of all cables be insulated from ground and other potentials at all points except for one single tie to a common ground. The location of this ground point will be noted on each specific cable description. Each cable shield must be continued as an unbroken electrical path from the ground point to the opposite end of the cable run.

4. Cable Entrances

The exact equipment configurations are the subject of each individual job requirement. Because of this, and because the cables are frequently prepared by the customer or on the job site, the exact cable entrance to each equipment will be determined at the time of installation. (The bottom of each equipment has an area available for cable entrance.) After installation, each cable entrance is to be sealed off to minimize the infiltration of dust into the various equipments. To facilitate the cable handling, it is recommended that there be a cable trench under each electronic equipment cabinet.

5. Power Wiring

Each system will specify the cabinet or cabinets that will be wired to the power mains. In each case the volt-ampere service and other characteristics will be specified. Power wiring will be in accordance with the various local and national codes. However, in planning the layout of cabling it should be recognized that power wiring is capable of inducing noise and interference especially in the low-level analog data wiring and to a degree in digital control wiring. Therefore, power wiring should be run in separate conduit and into separate cable entrances to equipment.

6. Analog Data Wiring

In order to avoid erroneous signals due to ground loops (or resistive coupling due to multiple currents in a common ground), the analog input chain of the system uses a two-wire, differential input system for all voltages. The levels of analog signals vary considerably from sensor to sensor, and it is necessary to further sub-divide them by signal level.

a. Low Level: defined as less than 100 millivolts full scale. This category includes such sensors as thermocouples, strain gages, radiation pyrometers, thermal converters and others.

b. Medium Level: defined as greater than 100 millivolts but less than 20 to 30 volts full scale.

c. High Level: defined as all signals which have full scale voltages in excess of 30 volts.

## B. ANALOG INPUT WIRING

Analog sensors and their respective extension leads are highly susceptible to capacitive and inductive coup-

ling of periodically varying voltages into the d-c intelligence of the sensor. Precautionary measures can minimize the possibility of noise pickup.

1. Thermocouples

Use grounded thermocouples as extensively as possible. It is also recommended that thermocouple extension leads be twisted shielded pair, the shield to be grounded at the thermocouple end. If the thermocouples can be conveniently grouped, a multiconductor cable with a common shield will suffice. Again, the shield is grounded at the thermocouple end.

2. Transducers

Extension cables from the transducers to respective computer should have a common shield grounded at the computer. Further, each transducer must be grounded only at one point; it is recommended that this be at the respective computer. Undesirable circulating ground currents will be minimized in this manner.

3. Special Precautions for Low-Level Analog Data Wiring

The layout and arrangement of conduits for all low-level analog data wiring should be given careful consideration. The conduit routes should avoid strong magnetic fields (such as power transformers or motors) and should avoid paralleling or running in close proximity of power wiring. Low-level analog data wiring should have the signal pair twisted to minimize the induced pickup. It will be shielded with an isolated shield to minimize the capacitive pickup, and the two wires should stay in close proximity to each other and pass through adjacent points on terminal strips or connector pins to avoid thermally induced emfs. To avoid corrosion voltages due to voltaic action between dissimilar materials exposed to electrolytes, terminal boards and junction boxes should be clean and dry. It is even more important in the low-level analog wiring that the shields of all cables be insulated from ground and other potentials at all points except for one signel reference point. (Note: The shield of low-level analog signals will not always be at ground since the signals may be at some common mode voltage other than ground.) The location of this one reference point will be noted on each specific cable description.

4. Cables for Use on Specific Signal Types

a. Low level (less than 100 millivolts)

(1) Thermocouples

The extension wire should be of the correct type for the thermocouple materials used. Polarity of leads must be strictly observed throughout the run of each thermocouple circuit.

Thermocouple extension wire should be twisted pairs with a single braid shielding around the pair. An insulating layer should surround the shield. In cases where the physical layout allows multiple pair extension leads, these may be used with a common shield overall. The thermocouple reference block terminals accept size 16AWG wire only.

(2) Thermal Converter Outputs

Use individual twisted pairs for each converter.

(3) Strain Gage Bridge Outputs

Use individual twisted shielded quads for each sensor.

(4) Miscellaneous Low-Level Signals -- Two Wire

Use individual twisted shielded pairs for each transducer.

b. Medium-level Analog Signals (100 millivolts to 20-30 volts)

(1) Resistance Temperature Devices

The three wire connection is used in all cases. Balance of the lead wire resistances is important so leads should all be the same length.

(2) Current Inputs (from pneumatic to current transducers and similar devices).

Most transducers of this type work over a reasonably wide resistance range and/or have lead wire and load compensation potentiometers. Therefore, wire size is not a significant factor for reasonable cable lengths. Shielded twisted pairs are used in general, but where physical layout permits, multiple pairs with common shield are also practical.

(3) Others - Analytical X-ray Gages, Operational Amplifiers in Other Control Equipments and Other Two-Wire Inputs.

Use individual twisted shielded pairs in general. Multiple conductor cables can be used in special cases where a large number of inputs come from one equipment.

c. High - Level Analog Signals (20 to 30 volts and up).

Signals in this category will require shielding to prevent coupling to other medium and low-level signals rather than to reduce pickup into the high-level signal. Many signals in the category are derived from sources with high volt-ampere capabilities and it will be necessary that all inputs of this type be fused at the source to prevent possible physical damage in the computer electronics cabinets. The input impedence to signals below 256 volts full scale is somewhat greater than 100,000 ohms, therefore, the input current when a point is scanned will be less than 2.5 ma. Type 8AF fast action instrument fuses may be used (Note: maximum rated voltage 250 volts). In cases of higher voltages, it is desirable to make special high impedence dividers to be mounted at the source that will reduce the voltage and limit the volt-ampere capability. Most voltages of this category are considered fatal and will require special handling. Signals in this category usually are not affected significantly by drops in common ground paths; however, to preserve the symetry of the already established pattern and as an added precaution, two circuits will be used.

5. Standard Cables for General Usage

Following is a standard list of instrumentation and control cables. It is highly desirable to use these standard cables wherever possible. If the wiring between two devices would require more than one of these cables and there would be no interference, the specific cable description might specify that the two cables could be run in the same conduit, but they will be composed of separate cables for standardization reasons.

a. Single Shielded Twisted Pair

Two conductor, #16 AWG (19/.0117), GE Wire and Cable Dept. spec. CW-1370, type III, or equivalent, tinned copper, .025 inch wall polyethlene insulation; Colors: one black, one white, twisted, tinned copper wire wrapped shield, jacket 3/64 black polyvinyl chloride, 600 volt.

b. Multiple Twisted Individually Shielded Pairs

GE Wire and Cable Dept. spec. CW-1370, type III, or equivalent. Conductors #16 AWG (19/.0117) tinned copper, .025 inch wall, polyethylene insulation. Fully color coded twisted pairs shielded with tinned copper wire wrap with PVC jacket over each shield. Cable tape over the cabled jacketed shielded pairs with PVC jacket overall.

c. Multiple Conductor, Shield Overall

GE Wire and Cable Dept. spec. CW-1370, Type IV, or equivalent. Conductor #16 AWG (19/0.017) .025 inch polyethylene insulation, fully color coded, cable type over insulated conductors followed by copper shielding tape, black PVC jacket overall, 600 volts.

| | |
|---|---|
| 7 cond/cable | OD 0.470" |
| 12 cond/cable | OD 0.630" |
| 19 cond/cable | OD 0.720" |
| 27 cond/cable | OD 0.880" |
| 37 cond/cable | OD 0.960" |

d. Multiconductor Logic Cable (Intra-System Cabling).

Conductor #20 AWG (10-#30), .010 inch polyethylene insulation, fully color coded pairs, overall shield of #34 tinned copper braid to provide 80% shielding coverage, tan PVC overall jacket, 22 mmfd/ft nominal capacity between basic wires in a pair with all other wires open circuited and shield grounded.

| | |
|---|---|
| 10 prs/cable | OD .510" |
| 20 prs/cable | OD .700" |
| 30 prs/cable | OD .840" |

IN THE CONSTRUCTION OF THE EQUIPMENT DESCRIBED, GENERAL ELECTRIC COMPANY RESERVES THE RIGHT TO MODIFY THE DESIGN FOR REASONS OF IMPROVED PERFORMANCE AND OPERATIONAL FLEXIBILITY.

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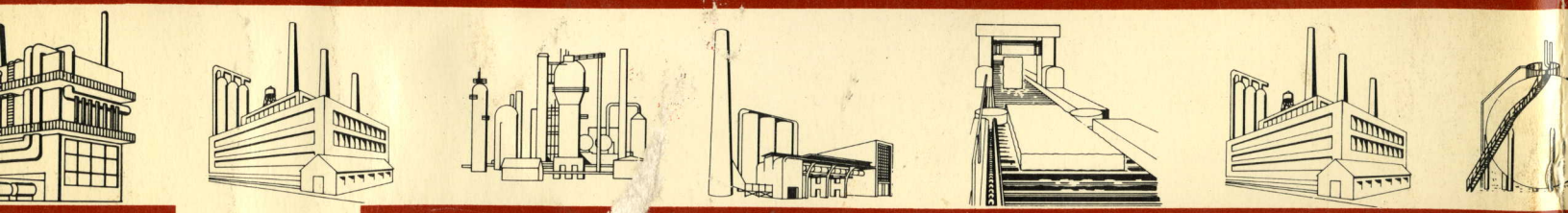

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