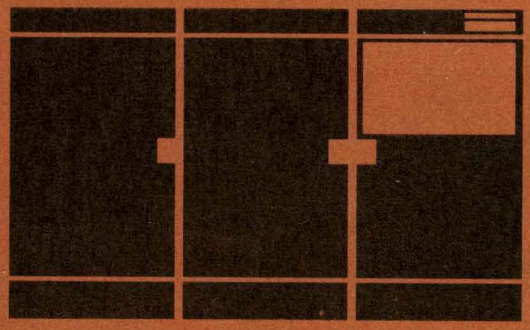
GENERAL ELECTRIC
COMPUTERS

CPC930
Common Peripheral Channel
for DATANET-30



GENERAL ELECTRIC

CPB-1254A

CPC930
COMMON PERIPHERAL CHANNEL FOR DATANET-30

REFERENCE MANUAL

Appendix G to DATANET-30 Programming Reference Manual (CPB-1019)

October 1965

Rev. July 1967

CPB-1254A

GENERAL ELECTRIC

INFORMATION SYSTEMS DIVISION

PREFACE

This revised manual describes the operation and programming of the DATANET-30 Common Peripheral Channel (CPC930). Changes in technical content are indicated by a bar in the margin opposite the change.

This manual was originally published as Appendix G to the DATANET-30 Programming Reference Manual, CPB-1019, and the identification number CPB-1254 did not appear on the cover.

Suggestions and criticisms relative to form, content, purpose, or use of this manual are invited. Comments may be sent on the Document Review Sheet in the back of this manual or may be addressed directly to Documentation Standards and Publications, B-90, Computer Equipment Department, General Electric Company, 13430 North Black Canyon Highway, Phoenix, Arizona 85029.

(750 10-67)

CONTENTS

ILLUSTRATIONS

COMMON PERIPHERAL CHANNEL (CPC930)

GENERAL DESCRIPTION

One DATANET-30* Common Peripheral Channel (CPC930) allows data transfer to or from memory between the DATANET-30 and one of the following peripheral devices:

DSU204 disc storage unit (DSU) with all options
MTC201, MTC301, MTH311, or MTH404 Magnetic tape controller
PRT200 or PRT201 printer
CRZ200 or CRZ201 card reader
CPZ100 (100cpm), or CPZ200 or CPZ201 (300cpm) card punch
PS6010 Programmable Peripheral Switch

Each CPC occupies two option module spaces and can be installed in rack 2, 3, or 4. Each CPC is assigned an address on the buffer selector. The address is specified by the address plug for the CPC.

From one to four CPC's can be installed in a DATANET-30. The maximum is determined by the fact that only four CPC's can be installed in rack 2 or by the number of memory interrupt cycles used. Five memory interrupt cycles are available for assignment to the following equipment.

NAME	CYCLES	CYCLE NO.
Controller selector unit (CSU931)	2	1 and 3
Processor interrupt unit (PIU930)	1	2
CPC with DSU	2	x,x
CPC with magnetic tape units	1	x
CPC with printer	1	x
CPC with card reader	1	x
CPC with card punch	1	x

Data Transfer

Data is transferred via the CPC one character at a time to or from the peripheral and one DATANET-30 word at a time to or from the DATANET-30. The CPC contains the necessary shift circuitry to accumulate characters into words or to separate sequential characters, depending on the direction of transfer. Data transfer is illustrated in Figure G-1.

---

* DATANET-Reg. Trademark of the General Electric Company.

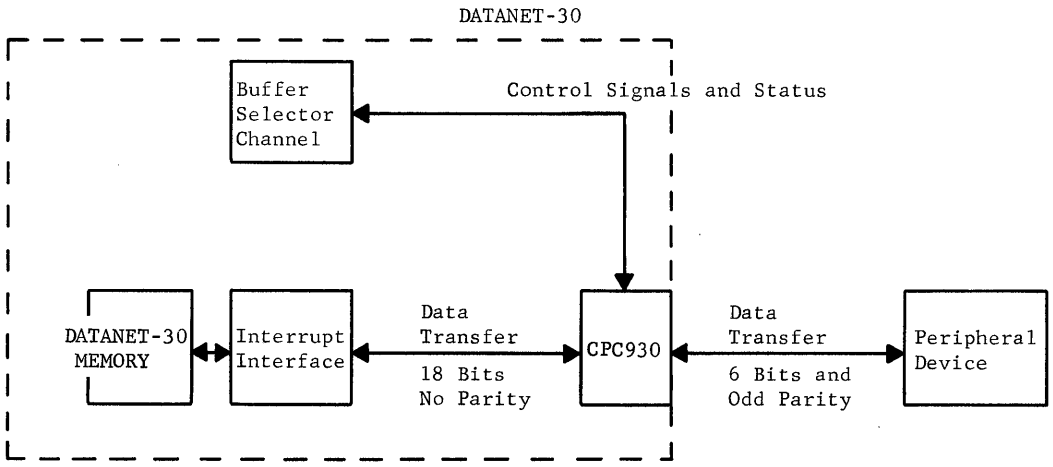


Figure G-1. Data Transfer Through a CPC930

When data is transferred from the CPC to the peripheral device, the most significant character of the DATANET-30 word is transferred first and the least significant, last.

Characters received by the CPC from the peripheral equipment are assembled into three-character words. The first character is shifted to the most significant part of the DATANET-30 word, and the third character is transferred as the least significant part.

If a Terminate signal is received from the peripheral before a full three-character word is shifted into the CPC, the character or characters in the shift register are shifted to the most-significant position. The CPC inserts zeros in the unfilled character positions before the word is transferred to memory.

Transfer Capacity

The CPC can transfer any number of characters from 1 to 49,152 (16,384-word memory at three characters/word) between a peripheral and the DATANET-30 memory. Any starting address within a 16k memory may be specified. It is not necessary to specify the number of characters in multiples of 3. The CPC accesses memory sequentially under memory interrupt control.

Block Diagram

Figure G-2 shows the basic configuration of the CPC. It contains a shift register, two 18-bit word buffers, an address counter, a character counter, peripheral status registers, and command-sequence and data-transfer control logic.

The CPC has three interfaces: (1) common peripheral interface (CPI), (2) DATANET-30 buffer selector, and (3) DATANET-30 interrupt interface.

The common peripheral interface provides the necessary data, status, and control logic to allow operation of the standard line of peripherals. The peripherals detect no difference between a common peripheral channel on a GE-400 or GE-625/635 computer and the CPC on the DATANET-30.

The DATANET-30 buffer selector interface presents peripheral and CPC status to the program and accepts control signals and command words from the program. One of the 127 possible buffer channel addresses must be assigned.

The DATANET-30 interrupt interface is used for data transfer between the CPC and the DATANET-30 memory locations specified by the address counter. The interrupt cycles to be assigned to a peripheral device (the CPC) are switch selectable and should not coincide with interrupts assigned to another device.

Character Counter

The character counter is used for read and write operations. It is counted down 1 each time a character is transferred to or from the CPC. An End Data Transfer signal is generated and sent to the peripheral device when the counter equals a count of zero.

The character counter is a straight binary counter. When loading the counter, the binary ones complement must be transferred to the counter. Therefore, the number (CW3) must be complemented before it is loaded into the character counter. The counter is loaded with the third LDT instruction of the initializing instructions sequence.

Address Counter

The CPC addresses memory sequentially, according to the address in the address counter. The address counter is counted up 1 each time a DATANET-30 word is transferred to or from memory. The address counter must be loaded with the starting memory address of data to be transferred or received. The counter is loaded by the second LDT instruction in the sequence of instructions to the CPC.

Parity

Parity (odd) is generated on each character before being transferred to the peripheral device. Parity is checked by the CPC on each character received from the peripheral device. In case of an error, NES 5 is set. A parity error does not affect CPC operation. NES 5 is reset by the next instruction to the CPC.

Controls and Indicators

The interrupt cycle select switches and the MANUAL RESET switch on the control panel of the DATANET-30 are the only manual controls for the CPC. Pressing the MANUAL RESET switch of the DATANET-30 also resets the peripheral device connected to the CPC. All other controls and indicators are by program or are on the control panels of the peripheral equipment.

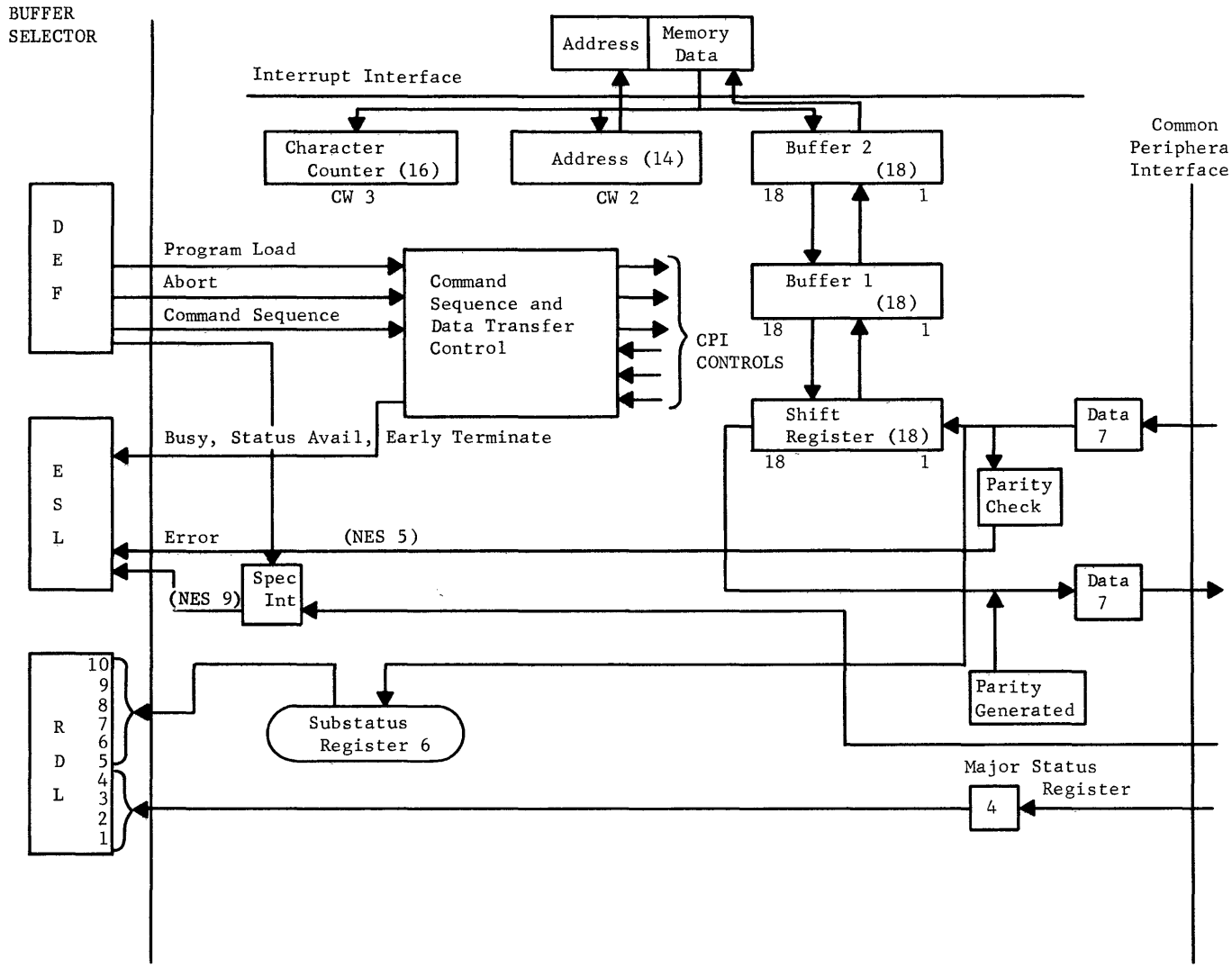


Figure G-2. Block Diagram

Interrupt Cycles

The CPC operates only with a DATANET-30 which has the interrupt interface (Mod III). The interrupt interface uses the DATANET-30 timing to create groups of five memory cycles which, in turn, can be individually assigned to devices such as the CPC. Therefore, when the CPC needs a memory cycle to transfer data, it can obtain the assigned cycle and be guaranteed no interference.

Five toggle switches on the connector bracket (Figure G-3) assign cycles to the CPC. Any one switch allows a transfer rate up to 86.4kc. Any two switches allow a transfer rate up to 172.8kc. The selected switch designates which interrupt cycle will be available to the CPC for data transfer.

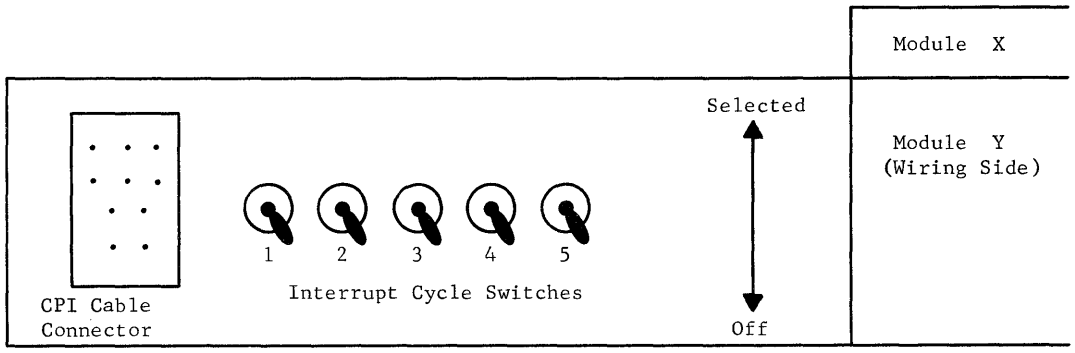


Figure G-3. Cable Connector and Switch Bracket

Cycle Assignment

To assign cycles to a CPC, the following procedure is used: (1) determine the maximum transfer rate of the peripheral, (2) determine the number of cycles to be assigned (1 cycle up to 86.4kc, 2 cycles up to 172.8kc), and (3) assign the cycles by lifting the proper switches on the bracket.

If two cycles out of the five are needed for a peripheral, do not assign two consecutive cycles. This is necessary to avoid losing data when an interrupt is not granted in time. Use combinations 1-3, 1-4, 2-4, 2-5, or 3-5. If a Controller Selector Unit (CSU931) is also connected to the DATANET-30, cycles 1 and 3 are assigned to the CSU. These cycles cannot be used by the CPC.

Normally, the same memory interrupt cycle number is not assigned to two different CPC modules or other modules connected to the interrupt interface, such as the Controller Selector Unit (CSU931) or the Processor Interrupt Unit (PIU). With careful programming, two peripherals can be assigned the same cycle if a program interlock prevents using both peripherals at the same time.

Status and Substatus

Status conditions are presented to the DATANET-30 on received data lines 1 through 10.

Receive Data Line	10	9	8	7	6	5	4	3	2	1
	2^5	2^4	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
	Substatus						Major Status			

Major status lines 1, 2, and 3 are set by the peripheral equipment and remain set until the first LDT instruction of a new command sequence.

Major status line 4 (Busy) changes as the busy status of the peripheral changes.

Substatus indicated at the CPC does not change immediately with substatus changes at the peripheral. Substatus is set in the substatus register after each command sequence and command termination and remains set until changed as a result of another command sequence or a Request Status instruction. The substatus of a peripheral may change many times without this change being indicated at the CPC.

When the program desires the status of the peripheral and NES 4 indicates status available, a register transfer instruction from R to any register (such as TRA R, B) transfers the last presented major status and the last presented substatus information into the register for examination. Current status may be obtained by issuing a Request Status (RQS) command prior to the register transfer instruction.

The NES instructions provide status information regarding overall operation of the CPC and the peripheral device.

The various major status and substatus conditions for the different peripheral equipment are summarized later in this manual.

Refer to the applicable equipment manual for additional information on status.

Special Interrupt

A Special Interrupt signal (NES 9) is generated by the peripheral equipment for various reasons. This does not cause a program interrupt but sets NES 9 to nonzero. Programming considerations for the peripheral dictate action required when a special interrupt occurs. Refer to the applicable peripheral manual for the conditions relating to the Special Interrupt signal. A DEF 9 is used to reset NES 9.

INSTRUCTION REPERTOIRE

The instructions are classified under two groups: the buffer selector instructions for the DATANET-30 and the peripheral command words. The buffer selector instructions are the Drive External Function (DEF), External Status Lines (NES), and Register Transfer (TRA and LDT) instructions. The rules for using these instructions are the same as those for using other DATANET-30 buffer selector instructions. The peripheral command words are used with the LDT instruction of the DATANET-30.

DATANET-30 Instructions

DEF INSTRUCTIONS. The Drive External Function instructions are as follows:

DEF 1-2 - Not Assigned

DEF 3 - Program Load

DEF 4-7 - Not Assigned

DEF 8 - Abort

DEF 9 - Reset Special Interrupt

DEF 0 - Command Sequence (Do not use)

DEF 3 - Program Load--Activates the program load line to the peripheral. (Refer to the applicable peripheral manual for results.) The DEF 3 instruction must always be preceded by manual reset or a Request Status operation in order to clear the address and character counters in the CPC. The information from the peripheral is then entered into memory, starting with address 0.

DEF 8 - Abort--Causes the immediate termination of any command in progress by forcing an EDT, if given immediately after the command sequence. If the instruction is given during data transfer, the EDT is not issued until the end of any third character (end of word) is transferred in or out of the shift register. This instruction also results in a pseudo "manual clear" to the CPC, and all CPC registers are cleared to zero. The early terminate line is activated if all the data has not been transferred.

DEF 9 - Reset Special Interrupt--Used by the program to reset a special interrupt (NES 9) signal.

DEF 0 - Command Sequence--Activated automatically by the LDT instruction used for initiating commands. The program cannot use DEF 0.

NES INSTRUCTIONS. Nonzero indicates the following:

NES 1 - Busy

NES 4 - Status Available

NES 5 - Receive Data Error

NES 8 - Early Termination

NES 9 - Special Interrupt

NES 0 - Not Assigned

NES 2-3 - Not Assigned

NES 6-7 - Not Assigned

Nes 1 - Busy--A 1 indicates the CPC is not available to receive a new command. The CPC reflects the busy state after CW 1 is given and until the 2^3 major status bit (peripheral busy) from the peripheral is reset or until buffer 1 and buffer 2 are empty on a read operation.

Ready--A zero indicates the CPC can receive a new command.

NES 4 - Status Available--Indicates the program can transfer the current major status and the last substatus information into a DATANET-30 register for examination. The status is not available when the CPC is transferring commands to the peripheral.

NES 5 - Receive Data Error--Indicates a parity error was detected on the data received from the peripheral during the last command.

NES 8 - Early Termination--Indicates the last data transfer was terminated by the peripheral before all characters were transferred and before the character counter reached zero.

NES 9 - Special Interrupt--Indicates the peripheral activated the special interrupt line. This signal must be reset by DEF 9.

The NES signals for Status Available, Receive Data Error, and Early Termination are reset by the next command word.

REGISTER TRANSFER INSTRUCTIONS. The Register Transfer instructions are as follows:

TRA From, TØ Major status and substatus are transferred from the CPC.

TRA R,

LDT This instruction is used to transfer command words 1, 2, and 3 to the CPC.

TRA B,T Not used.

Example:

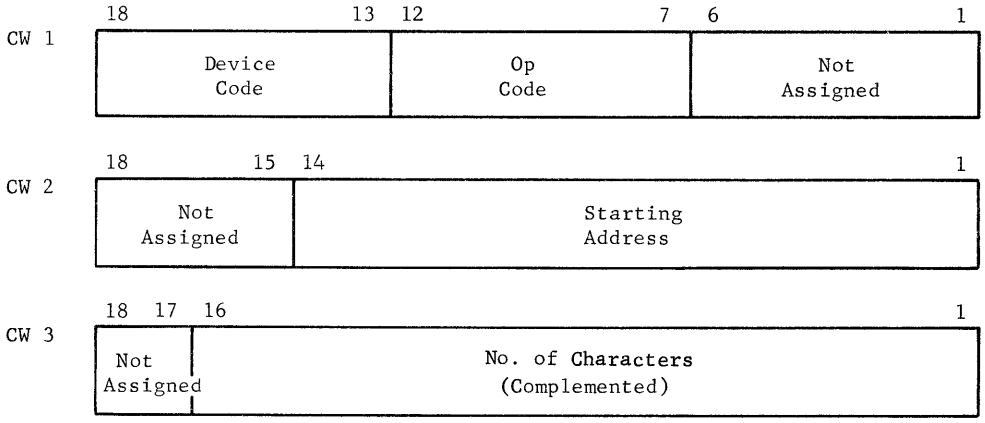
```
NES  4      Is status available?
BZE  *-1    No wait.
TRA  R,B    Transfer major status and substatus to B-register.
```

Command Words

Peripherals respond to two types of commands: data transfer and nondata-transfer. Refer to the applicable programming manual for the specific instructions to use.

DATA TRANSFER COMMANDS. The CPC requires three command words to initiate and execute a data transfer command. The command words are provided to the CPC by three LDT instructions. For data transfer, the command words must be given in the sequential order of CW 1, CW 2, and CW 3.

The formats of the command words are as follows:



Command Word 1--Bits 7-12 contain the operation code. Bits 13-18 contain the device code. Bits 1-6 are not assigned and may be used by the program.

Command Word 2--Bits 1-14 contain the starting address from or to which data transfer is to take place. Bits 15-18 are not assigned and may be used by the program.

Command Word 3--Bits 1-16 contain the ones complement of the number of characters to be transferred. Bits 17-18 are not assigned and may be used by the program.

On receipt of CW 3, the CPC initiates the I/O sequence to send the device code and the operation code to the peripheral. The Busy external status line indicates busy until termination of the command. Termination may occur for one of five reasons:

1. The character counter indicates all the characters have been transferred.
2. The peripheral sends a Terminate signal indicating it has reached the end of a record, card, or other unit of data as prescribed for the particular peripheral device.
3. The peripheral sends a Terminate signal indicating some error or alert condition has occurred which requires stopping the data transfer.
4. The program issues an Abort command.
5. The DATANET-30 enters Hardware Load.

On receipt of the Terminate signal for any of the first three reasons during a read command, the CPC left-justifies the characters in the shift register prior to transferring the word to memory. On a write command, data transfer stops immediately. An Abort or Hardware Load causes termination, with no further data transfers to memory. Coding to initiate a data transfer command is as follows:

```
PIC CPCADD      Select CPC channel
NES 1           Test busy line
BNZ Busy
LDT CW1         Load CW 1
LDT CW2         Load CW 2
LDT CW3         Load CW 3
NES 4           Test status available
BZE NOT
TRA R,B         Pick up status for examination
```

Since the CPC interfaces with different types of peripheral equipment, any additional command information needed by a peripheral device must be contained in the first words transferred to the peripheral.

NONDATA-TRANSFER COMMANDS. A nondata-transfer command requires only CW 1 from the program. The CPC decodes the nondata-transfer condition and initiates the I/O sequence without requiring CW 2 and 3. The command, by definition, terminates at the end of the I/O sequence. The busy line indicates busy during the I/O sequence. The coding is as follows:

```
PIC CPCADD      Select CPC channel
NES 1           Test busy
BNZ Busy
LDT CW1         Load CW 1
NES 4           Test status availale
BZE NOT
TRA R,B         Pick up status for examination
```

The nondata-transfer command operation codes may be recognized by the fact that either the high-order bit = 1 or the four low-order bits = zero (1x0000).

Programming Considerations

In programming the CPC, the following factors must be considered:

1. The frequency for checking the special interrupt line should be determined for each peripheral.

2. The program must reset the Special Interrupt signal.

3. Status recovery procedures depend upon the peripheral equipment.

4. When Request Status and Reset Status are used, the rules of the peripheral in use must be followed. Request Status cannot be given during data transfer.

5. The peripheral instructions are not recognized by the assembly program in mnemonic form. The instruction mnemonics are included for reference only. Each peripheral instruction must be established in memory in octal form (machine language). Command words may then be referred to symbolically for the instruction desired.

6. The extra information required by the peripheral equipment not contained in CW 1 must be located in the first memory location(s) transferred to the peripheral.

7. The instructions for the various peripheral devices are included here for reference only. Refer to the applicable manual for detailed explanation of the instructions and additonal information.

General Electric Standard Character Set

Standard Character Set	GE-Internal Machine Code	Octal Code	Hollerith Card Code	Standard Character Set	GE-Internal Machine Code	Octal Code	Hollerith Card Code
0	00 0000	00	0	↑	10 0000	40	11-0
1	00 0001	01	1	J	10 0001	41	11-1
2	00 0010	02	2	K	10 0010	42	11-2
3	00 0011	03	3	L	10 0011	43	11-3
4	00 0100	04	4	M	10 0100	44	11-4
5	00 0101	05	5	N	10 0101	45	11-5
6	00 0110	06	6	O	10 0110	46	11-6
7	00 0111	07	7	P	10 0111	47	11-7
8	00 1000	10	8	Q	10 1000	50	11-8
9	00 1001	11	9	R	10 1001	51	11-9
[	00 1010	12	2-8	-	10 1010	52	11
#	00 1011	13	3-8	$	10 1011	53	11-3-8
@	00 1100	14	4-8	*	10 1100	54	11-4-8
:	00 1101	15	5-8	)	10 1101	55	11-5-8
>	00 1110	16	6-8	;	10 1110	56	11-6-8
?	00 1111	17	7-8	'	10 1111	57	11-7-8
ъ	01 0000	20	(blank)	+	11 0000	60	12-0
A	01 0001	21	12-1	/	11 0001	61	0-1
B	01 0010	22	12-2	S	11 0010	62	0-2
C	01 0011	23	12-3	T	11 0011	63	0-3
D	01 0100	24	12-4	U	11 0100	64	0-4
E	01 0101	25	12-5	V	11 0101	65	0-5
F	01 0110	26	12-6	W	11 0110	66	0-6
G	01 0111	27	12-7	X	11 0111	67	0-7
H	01 1000	30	12-8	Y	11 1000	70	0-8
I	01 1001	31	12-9	Z	11 1001	71	0-9
&	01 1010	32	12	←	11 1010	72	0-2-8
.	01 1011	33	12-3-8	,	11 1011	73	0-3-8
]	01 1100	34	12-4-8	%	11 1100	74	0-4-8
(	01 1101	35	12-5-8	=	11 1101	75	0-5-8
<	01 1110	36	12-6-8	"	11 1110	76	0-6-8
\	01 1111	37	12-7-8	!	11 1111	77	0-7-8

DISC STORAGE UNIT (DSU) SUBSYSTEM

Information on the DSU204 Disc Storage Unit (DSU) subsystem not provided in this discussion may be found in the DSU204 subsystem reference manuals.

DSU Subsystem Instructions

The DSU204 subsystem instructions are summarized in the following chart.

INSTRUCTION	MNEMONIC	CODE (OCTAL)
Seek File	SF	34
Seek/Read File	SRF	14
Read File	RF	54
Seek/Read File and Release Seek	SRFR	15
Read File and Release Seek	RFR	55
Seek/Read File and Increment Address	SRFI	16
Read File and Increment Address	RFI	56
Seek/Write File	SWF	10
Write File	WF	50
Seek/Write File and Release Seek	SWFR	11
Write File and Release Seek	WFR	51
Seek/Write File and Increment Address	SWFI	12
Write File and Increment Address	WFI	52
Seek/Write File and Verify	SWFV	13

INSTRUCTION	MNEMONIC	CODE (OCTAL)
Write File and Verify	WFV	53
Read File Continuous	RFCR	25
Write File Continuous	WFCR	31
Write File Continuous and Verify	WFCV	33
Seek/Compare	SCPR	17
Compare	CPR	57
Seek/Link	SLNK	35
Link	LNK	75
Accept Buffer Address	ABA	32
Read Buffer	RB	24
Write Buffer	WB	30
Load Buffer for Compare	LBFC	36
Move Data	MVDT	37
Request Status	RQS	00
Reset Status	RSS	40

Physical Organization of DSU Subsystem

Data flow in a DSU subsystem is shown in Figure G-4.

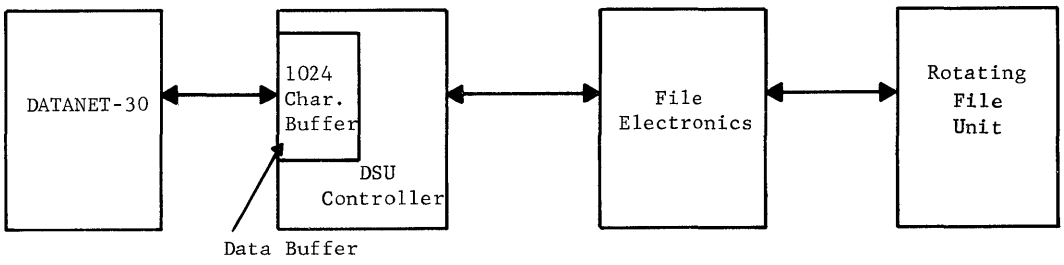


Figure G-4. Block Diagram of Data Flow of DSU Subsystem

DSU CONTROLLER. The controller is a single free-standing enclosure. This unit links the DSU to the DATANET-30. Up to four DSU's can be connected to one DSU controller (one to four devices).

DSU. A DSU consists of a rotating assembly subunit (file unit) and a file electronics subunit. The rotating assembly subunit houses the rotating discs. The file electronics houses the electronics necessary for direct control of the file unit.

Logical Organization of DSU Controller

The DSU controller is organized around a 1024-character core buffer made up of four data blocks.

The logical subdivision of the buffer must be clearly understood by anyone concerned with programming the DSU subsystem.

The following table relates the buffer addresses (in octal) and their functions:

Addresses	Function
0000-0357	Buffer section W data block storage; contains one data block.
0360	Check character for data block in buffer section W.
0361-0377	Buffer section W control block storage. Control characters for the DSU on file channel 1, (device 1) are stored here. The first nine addresses (0361-0371) contain storage for file electronics subunit 1. The remaining six addresses (0372-0377) contain the control characters for device 1. (See Figure G-5.)
0400-0757	Buffer section X data block storage.
0760	Check character for data block in buffer section X.

Addresses	Function
0761-0777	Buffer section X control block storage. Used by device 2 (control characters stored in 0772-0777).
1000-1357	Buffer section Y data block storage.
1360	Check character for data block in buffer section Y.
1361-1377	Buffer section Y control block storage. Used by device 3 (control characters stored in 1372-1377).
1400-1757	Buffer section Z data block storage.
1760	Check character for data block in buffer section Z.
1761-1777	Buffer section Z control block storage, used by device 4 (control characters stored in 1772-1777).

The check character is generated when a record is written on a disc. It is a modulo-64 count of the number of 1-bits in the data block being written. During read operations, the check character is transferred to an applicable check character section of the buffer.

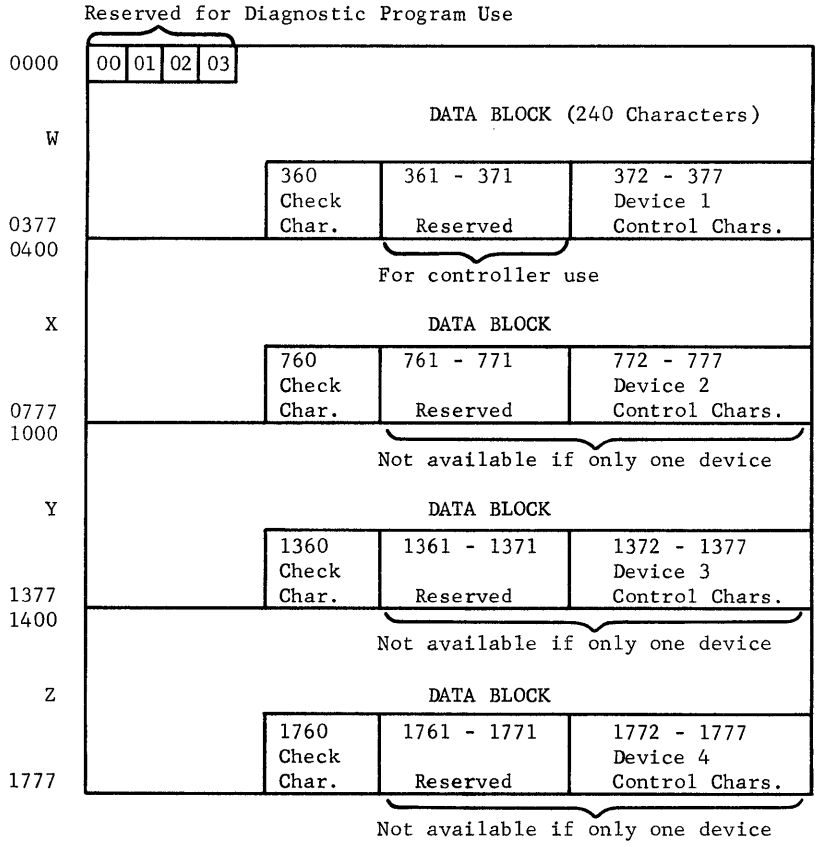


Figure G-5. Buffer Addresses and Functions of the 1024-Character Buffer

When a command requiring control characters is addressed to a particular device, the applicable control block section of the buffer is used, as shown below:

File Unit 1	Buffer section W control block
File Unit 2	Buffer section X control block
File Unit 3	Buffer section Y control block
File Unit 4	Buffer section Z control block

Note that the buffer section data blocks are not restricted to any one device. Thus, device 1 can read or write to any or all of the buffer section data blocks. Once a write or read operation is initiated, the controller logic commits the applicable buffer section data blocks to the particular device being used. When the operation is completed, the buffer sections are released for the commitment. Thus, buffer sections Y and Z can be used for device 1, while buffer sections W and X are being used for device 2.

Note: A special core checkout switch (the SPCCIR switch) has been added for testing the DSU buffer. When this switch is ON, the buffer is logically just a 1024-character buffer. The various addresses and functions noted above are overridden.

The first four consecutive data blocks starting at address 00 should never be considered as data block addresses for operating programs. These addresses are used by diagnostic programs.

Device Code

The DSU204 subsystem requires a device code character indicating the specific file unit to which the instruction is directed. The device code characters are defined as follows:

Device Code	Meaning
00	Instruction involves controller only *
01	Instruction is addressed to file unit 1
02	Instruction is addressed to file unit 2
03	Instruction is addressed to file unit 3
04	Instruction is addressed to file unit 4

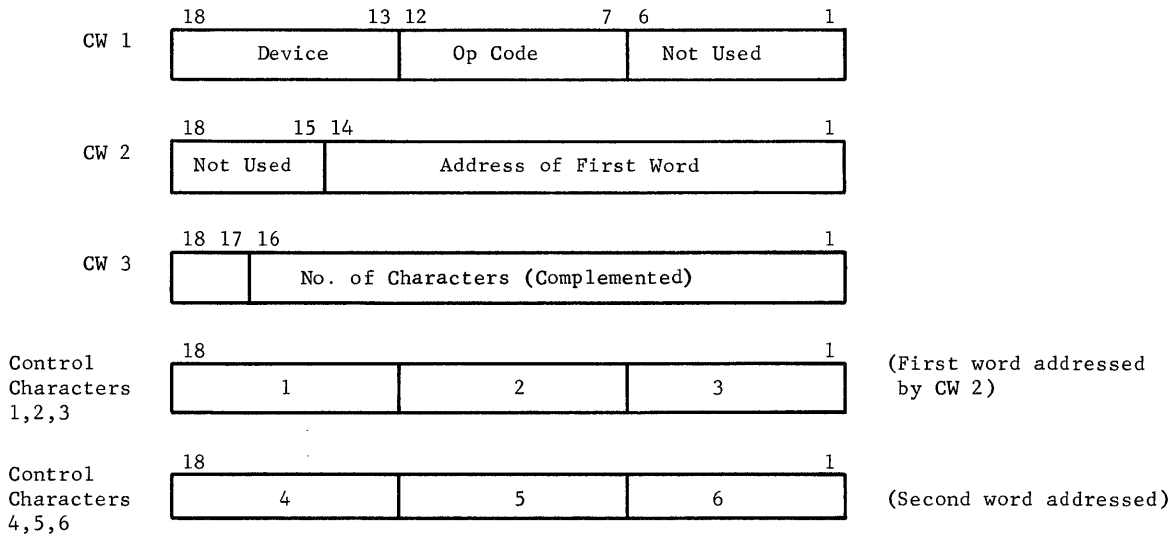
*Instructions not involving a specific file unit ignore the device code character.

Control Characters

The six control characters which are stored in the 1024-character buffer of the DSU controller must be placed there as a part of the DATANET-30 command sequence. An example of this command sequence is shown below.

The six control characters are contained in two DATANET-30 words. These words are transferred to the DSU following the command sequence (CW 1, 2, 3). The control characters must be considered as part of the command sequence for the DSU204 subsystem.

For example:



Command Sequence

Since the character counter contains the count of 6, the command sequence ends at the DATANET-30. The controller then executes the command.

PROGRAM EXAMPLE.

```
                PIC   CPCADR      CPC CHANNEL ADDRESS
                NES   1          CHANNEL BUSY
                BNZ   *-1        YES, WAIT
                LDT   D20CMD     COMMAND WORD
                LDT   CARADD     LOCATION OF CONT. CHAR. 1,2,3
                LDT   CMP#CH     NO. CONTROL CHARS. COMPLEMENTED
                NES   4          STATUS OF COMMAND SEQ. AVAILABLE
                BZE   *-1        NO, WAIT
                 .                .
                 .                .
                 .                .
D20CMD          OCT   011400     FILE 1 - SEEK READ FILE COMMAND
CHRADD          IND   *+1        ADDRESS OF CONTROL CHARACTER
                OCT              DISC ADDR. - CONTROL CHARS 1,2,3
                OCT   001010     BUFFER BLOCK W TO W - CHARS 4,5,6
CMP#CH          OCT   777771     COMPLEMENT OF NO. OF CHARS. (SIX)
```

The command sequence for programming the DSU204 has three general forms:

1. Commands requiring no control characters, for example Request Status (RQS) and Reset Status (RSS).

2. Commands which address a file unit.

3. Commands which move data to or from the character buffer and the DATANET-30 or within the buffer.

The required control characters for item 2 above are provided as a part of the command sequence. The address location of the control characters is provided by Command Word 2.

The control characters for 3 above must have already been provided, that is, they must be in the character buffer. The address provided by Command Word 2 in this case is the starting address for the data in DATANET-30 memory. The final difference is that Command Word 3 is the DATANET-30 address of the number of data characters (complemented) to be moved.

These three command sequences do not correspond with the three modes of disc operation (on-line only, off-line only, and combined on-line/off-line).

COMBINED ON-LINE/OFF-LINE COMMANDS. Combined on-line/off-line instruction execution involves a time on line while address-definition (control) characters are being transferred from computer memory to the controller and into a buffer control block. The remainder of execution time is off line, using the address-definition characters stored in the buffer control block assigned to the file unit being addressed by the instruction.

The seek instructions listed below result in a combined on-line/off-line type of operation:

Seek File
Seek/Read File
Seek/Read File and Release Seek
Seek/Read File and Increment Address
Seek/Write File
Seek/Write File and Release Seek
Seek/Write File and Increment Address
Seek/Write File and Verify
Seek/Compare
Seek/Link

Upon receipt of an on-line/off-line instruction, the controller reverts to a subsystem Busy status and initiates a request for six control characters from the central processor. The control characters are stored in the controller in the last six character positions of the control block of the buffer section assigned to the file unit being addressed by the instruction.

All six control characters must be received by the DSU204 subsystem. If it receives the End Data Transfer signal before all control characters are received, instruction execution ends, and the Data Alert, Invalid Control Character status condition is set in the controller.

If all control characters are received and stored in the buffer and no errors are detected, the controller reverts to a Ready status and transmits a 'not busy signal to the central processor to indicate that the on-line portion of instruction execution is complete.

The control characters are encoded as follows:

Characters 1, 2, and 3	- These characters indicate the address of the file sector to be accessed during execution of the instruction.
Characters 4, 5, and 6	- The encoding of these characters is determined by the instruction being used.

CONTROL CHARACTERS 1, 2, and 3.

Sector Addressing. There is no format restriction of the 240 data characters within a sector of data. These characters are generated by the central processor. Sectors are continuously addressable within each individual file unit. Up to 32 contiguous sectors are continuously addressable before an actuator arm movement occurs.

The check character is generated by the controller during a write operation and is automatically written on the file unit as the last (241st) character of each sector being written. The controller generates the check character by making a modulo-64 count of the number of 1-bits in the sector being written. The modulo-64 check character represents the remainder obtained by dividing the number of 1-bits stored in the sector by 64.

The check character is never transmitted to the central processor during a normal read operation. However, the check character may be transferred to the central processor by first issuing an Accept Buffer Address and then a Read Buffer instruction.

The bit configuration for a data sector address within any one file unit is illustrated in Figure G-6.

This configuration of address bits provides for continuous sector addresses through an entire file unit. For any one specified disc and actuator position, a zone code of 00 addresses the 32 sectors under the four heads covering both the upper and lower surfaces of the disc in the inner zone. A zone code of 01 addresses the 32 sectors under the two heads covering the upper surface of the disc in the outer zone. A zone code of 10 addresses the 32 sectors under the two heads covering the lower surface of the disc in the outer zone.

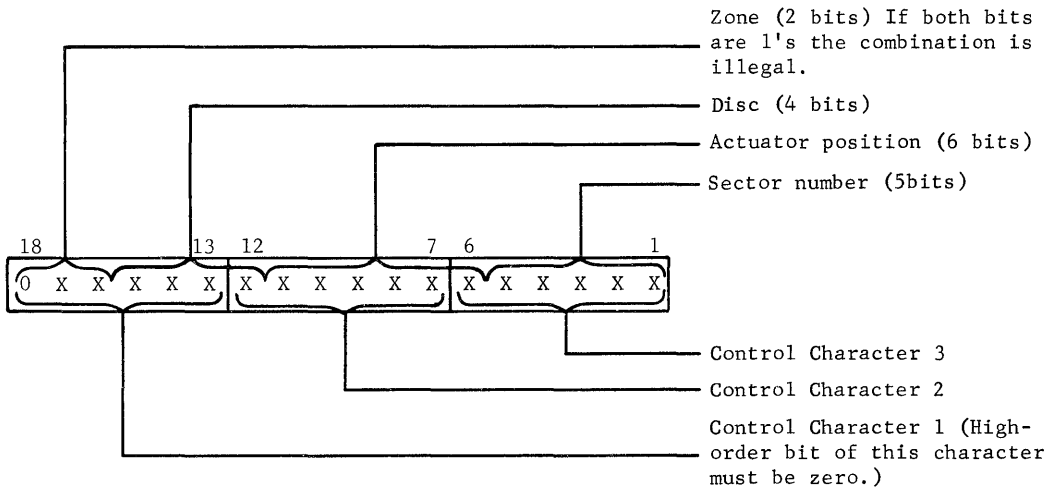


Figure G-6. Sector Address Control Character Format

Any data sector whose address contains a 1 in all five low-order bit positions is the last consecutively addressable sector available from a file unit without requiring repositioning of the actuator. Instruction execution always ends after the last consecutive sector is accessed.

The four consecutive data sectors on each file unit, starting at address 00 0000 000000 00000, are reserved for diagnostic program purposes and should not be used by the programmer. Although there is no hardware to prevent a reserved diagnostic sector from being accessed, in using these sectors there is considerable risk of having a diagnostic program overwrite the contents of the reserved sectors.

Fast-Access Disc Addressing. Each disc used in a fast-access option is addressed by expressing its number, in binary form, in the four disc bits of the file address. Discs 12 through 15 are used for fast-access option 1, and discs 8 through 15 are used for fast-access option 2. The six actuator position bits of the file address must be zero when addressing a fast-access disc. Each fast-access disc contains three groups of data, one group for each of the three legal combinations of zone codes in the file address. Each of the three groups contains 32 sectors of data.

The central processor must transmit the sector address to the DSU204 subsystem to indicate which data sectors are to be accessed.

The following charts show the coding used for control characters 1, 2, and 3 as defined in Figure G-6.

DISC BITS 12-15

Code	Disc
0000	0
0001	1
0010	2
0011	3
⌇	⌇
1000	8
⌇	⌇
1111	15

SECTOR (BLOCK) NUMBER BITS 1-5

Code	Sector
00000	0
00001	1
⌇	⌇
01000	8
⌇	⌇
10000	16
⌇	⌇
11111	31

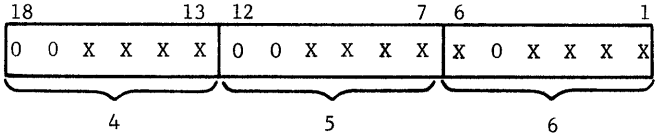
ZONE BITS 16,17

Code	Zone
00	Inner Zone Both
01	Outer Zone Top
10	Outer Zone Bottom
11	Illegal

ACTUATOR POSITION BITS 6-11

Code	Position
000000	0
000001	1
000010	2
⌇	⌇
001000	8
⌇	⌇
010000	16
⌇	⌇
100000	32
⌇	⌇
111111	63

CONTROL CHARACTERS 4, 5, AND 6. The details for encoding characters 4, 5, and 6 (see sketch, below) cannot be generalized. The encoding for these characters is determined by the command to be executed.



Input/Output Control

Before a read or write operation can be executed, a seek operation must be done to position the actuator properly for the segment being addressed.

Upon completion of the seek, the read or write operation can be executed.

Data read from the disc is stored in the data buffer.

Upon completion of the read, the data is transferred from the data buffer to memory of the DATANET-30.

Examples of the instruction sequence for a read are shown in Figure G-7. The write operation is essentially the reverse of the read.

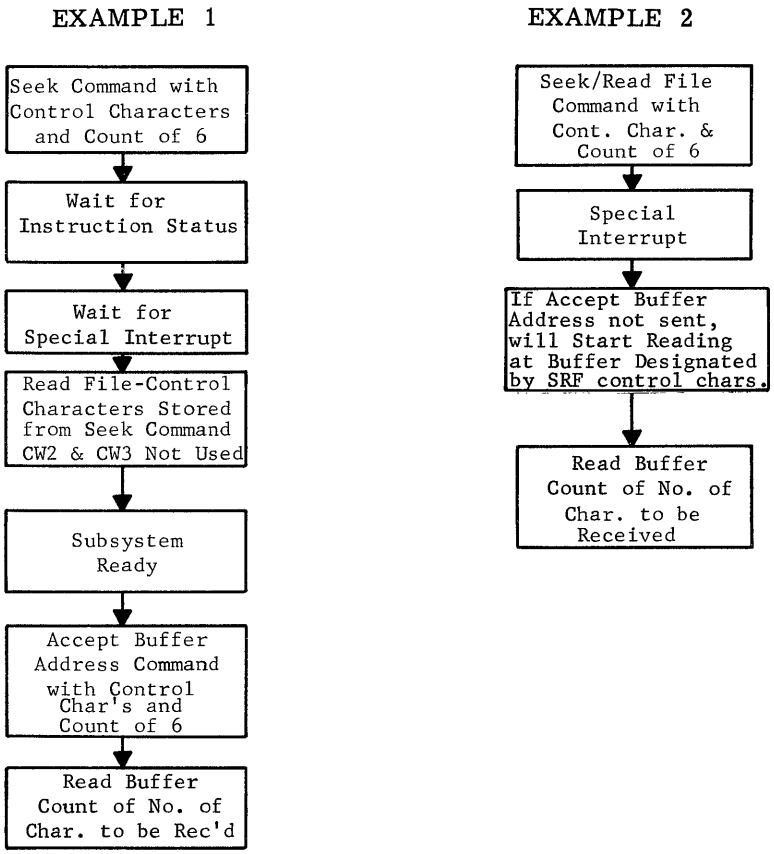


Figure G-7. Examples of Instruction Sequence for a DSU204 Read Instruction

The off-line portion of instruction execution begins as soon as the Subsystem Not Busy signal is sent to the CPC. The off-line operation to be executed is defined by the control characters stored in the assigned buffer control block.

If an error is detected in the control characters during the on-line portion of instruction execution, the off-line portion is not initiated. Instead, the controller reverts to the appropriate error status condition and sends the not busy signal to the central processor. The outcome of instruction execution can be determined by issuing a Request Status instruction.

As soon as the off-line portion of an instruction is executed, the DSU sends a Special Program Interrupt signal to the central processor. When the Special Program Interrupt signal is received by the central processor, the outcome of execution of the off-line portion of the instruction can be determined by addressing a Request Status instruction to the file unit involved.

While an instruction is being executed off-line, the controller is free to accept and execute other instructions, provided that execution of these other instructions does not require the use of a file unit previously committed to an off-line operation.

Combined on-line/off-line instructions, with the exception of Seek File, are the only instructions that cause the buffer sections involved to be committed. The involved buffer sections remain committed until the off-line portion of instruction execution ends. The Seek File instruction does not commit the involved buffer sections.

Instructions Requiring Transfer of Control Characters

The commands requiring transfer of control characters as part of the command sequence are again divided as follows:

Controller Only.

MNEMONIC	CODE (OCTAL)	DESCRIPTION
ABA	32	Accept Buffer Address Sends buffer address to controller. Control characters: Characters 1 and 2 contain the buffer address. Characters 3, 4, 5, and 6 are ignored.
MVDT	37	Move Data Moves up to 240 characters from one address to another. Control characters: Characters 1 and 2 contain "to" address. Characters 3 and 4 contain number of characters. Characters 5 and 6 contain "from" address.

File Only.

SF	34	Seek File Seeks the block specified by control characters 1, 2, and 3. Control Characters: Characters 1, 2, and 3 contain the block address. Characters 4, 5, and 6 are not pertinent to this command, but may be significant to subsequent commands.
SRF	14	Seek/Read File Seeks the block specified by control characters 1, 2, and 3. When the block is found, blocks are read into the buffer sections specified by control characters 5 and 6. From one to four blocks can be read. Control Characters: Characters 1, 2, and 3 contain the block address. Character 4 is not pertinent. Character 5 indicates the buffer sections into which file blocks are to be read: 1 in 2^0 position indicates buffer section Z 1 in 2^1 position indicates buffer section Y 1 in 2^2 position indicates buffer section X 1 in 2^3 position indicates buffer section W

MNEMONIC	CODE (OCTAL)	DESCRIPTION
		Character 6 indicates the buffer section into which the first data block read is to be placed: 1 in 2^0 position indicates buffer section Z 1 in 2^1 position indicates buffer section Y 1 in 2^2 position indicates buffer section X 1 in 2^3 position indicates buffer section W The two high-order bits of character 6 must be zero.
SRFR	15	Seek/Read File and Release Seek Identical with the SRF command until termination of the command is reached. At this time, the power to the actuator involved is dropped. Control Characters: Same as those for SRF.
SRFI	16	Seek/Read File and Increment Address Indentical with the SRF command until termination of the command is reached. At this time, the block address in the control characters is counted up to the next consecutive address. Thus, if two blocks were read, the original block address is counted up by two. Control Characters: Same as those for SRF.
SWF	10	Seek/Write File Seeks the block specified by control characters 1, 2, and 3. When the block is found, blocks are written from the buffer sections specified by control characters 5 and 6. From one to four blocks can be written. Control Characters: Characters 1, 2, and 3 contain the block address. Character 4 is not applicable. Character 5 indicates the buffer sections from which data is to be written on the file. (Character 5 coding is identical with that for character 5 for the SRF command.) Character 6 indicates the buffer section from which the first data block to be written is taken. (Character 6 coding is identical with that for character 6 for the SRF command.)
SWFR	11	Seek/Write File and Release Seek Identical with the SWF command until termination of the command is reached. At this time, the power to the actuator involved is dropped. Control Characters: Same as those for SWF.
SWFI	12	Seek/Write File and Increment Address Identical with the SWF command until termination of the command is reached. At this time, the block address in the control characters is counted up to the next consecutive address. Thus, if three blocks were read, the original block address is counted up by 3. Control Characters: Same as those for SWF.

MNEMONIC	CODE (OCTAL)	DESCRIPTION
SWFV	13	Seek/Write File and Verify Seeks the block specified by control characters 1, 2, and 3. When the block is found, blocks are written from the buffer sections specified by control characters 5 and 6. From one to four blocks can be written. At the conclusion of the write operation, a latency is incurred and the blocks written on the file are compared bit by bit with the original block information stored in the buffer. Control Characters: Same as those for SWF.
SCPR	17	Seek/Compare Seeks the block specified by control characters 1, 2, and 3. When the block is found, it is compared to the buffer section specified by control character 6. Comparison is made on the basis of "fields." A field is defined as a group of sequential characters bounded by Ignore characters (octal 17) or bounded by an Ignore character and the beginning of the data block or bounded by an Ignore character and the end of the block. A field may contain as many fields as desired within the limits defined above. The compare operation is considered a success if any one field of the buffer data block compares exactly with the corresponding field of the file data block. If the compare is not successful, the next sequential file block is read and compared. This continues until the last consecutive block has been read or a successful compare is made. If the compare is successful, blocks are read into the buffer sections specified by control character 5. The block address of the file block for which the successful compare was made will replace control characters 1, 2, and 3 in the file control block. Control Characters: Characters 1, 2, and 3 contain the block address. Character 4 is not applicable. Character 5 indicates the buffer sections into which blocks are to be written if a compare is made. (Character 5 coding is identical with that for character 5 for SRF command.) Character 6 indicates the buffer section to which the file blocks are to be compared and, if a comparison is being made, indicates the first buffer section into which the first file data block read is to be placed. (Character 6 coding is identical with that for character 6 for the SRF command.)
SLNK	35	Seek/Link Seeks the block specified by control characters 1, 2, and 3. When the block is found, it is read from the file and written in the buffer section indicated by control character 6. At this time, three characters are pulled from the buffer, starting at the buffer location specified in control characters 4 and 5. If the high-order bit of the first character read is a 1, the operation is terminated. If, however, the high-order bit is a 0, the three characters are stored in the applicable control block section of the buffer, replacing the three characters of file address (that is, control characters 1, 2, and 3).

Control Characters:
Characters 1, 2, and 3 contain the block address. Characters 4 and 5 contain the buffer address of the first of the three characters to be checked for link. Character 6 indicates the buffer section into which the file block is to be read. (Character 6 coding is identical with that for character 6 for the SRF command.)

Instructions Not Requiring Transfer of Control Characters

The commands that require certain control characters but do not request control characters as part of the command sequence from the DATANET-30 are divided as shown below.

The control characters needed by each of the following commands must be part of the command preceding it:

Controller Only.

MNEMONIC	CODE (OCTAL)	DESCRIPTION
RB	24	Read Buffer Read the buffer, using a stored address as the starting address. Data read is sent to the DATANET-30 memory.
WB	30	Write Buffer Writes the buffer, using the stored address as the starting address.
LBFC	36	Load Buffer For Compare Writes up to 240 characters in one data block. If there are fewer than 240 characters in one data block, the rest of the block is filled with characters (octal 17).
RSS	40	Reset Status
RQS	00	Request Status

File Only.

RF	54	Read File The applicable control block section of the buffer provides the control characters for this command. The control characters were placed there by a previous command. Once the control characters are obtained, the command is identical with the SRF command.
RFR	55	Read File and Release Seek Identical with the RF commands until termination of the command is reached. At this time, the power to the actuator involved is dropped.

MNEMONIC	CODE (OCTAL)	DESCRIPTION
RFI	56	Read File and Increment Address Identical with the RF command until termination of the command is reached. At this time, the block address in the control characters is counted up to the next consecutive block.
WF	50	Write File The applicable control block section of the buffer provides the control characters for this command. The control characters were placed there by a previous command. Once the control characters are obtained, the command is identical with the SWF command.
WFR	51	Write File and Release Seek Identical with the WF command until the termination of the command is reached. At this time, the power to the actuator involved is dropped.
WFI	52	Write File and Increment Address Identical with the WF command until termination of the command is reached. At this time, the block address in the control characters is counted up to the next consecutive address.
WFV	53	Write File and Verify The applicable control block section of the buffer provides the control characters for this command. The control characters were placed there by a previous command. Once the control characters are obtained, the command is identical with the SWF command.
RFCR	25	Read File Continuous The applicable control block section of the buffer provides the control characters for this command. The command seeks the block specified by control characters 1, 2, and 3. At the completion of the seek command, the block is read into buffer section W. As soon as W is filled, the data is transferred to the DATANET-30 memory. The next sequential file block is then read into buffer section X. As soon as X is filled, the data is transferred to the DATANET-30 memory. This continues in serial fashion until one of the following occurs: 1. An error condition is detected. 2. The last consecutive block is read. 3. The CPC sends an End Data Transfer. (Note that 32 blocks can be read in this fashion.)

MNEMONIC	CODE (OCTAL)	DESCRIPTION
WFCR	31	Write File Continuous The applicable control block section of the buffer provides the control characters for this command. The control characters were placed there by a previous command. Once the control characters are obtained, the command seeks the block specified by control characters 1, 2, and 3. At the completion of the seek command, buffer section W is filled with data from the external user. As soon as buffer section W is filled, the data is transferred to the file block. Buffer section X is then filled and the next sequential file block is written from X. This continues in a serial fashion until one of the combinations listed under the RFCR command occurs. (Note that 32 blocks can be written in this fashion.)
WFCV	33	Write File Continuous and Verify This command is identical with the WFCR command, with the following exception: after all blocks are written a file latency occurs and all blocks which were written are read, and the check character for each block is verified.
CPR	57	Compare The applicable control block section of the buffer provides the control characters for this command. The control characters were placed there by a previous command. Once the control characters are obtained, the command is identical with the Seek/Compare command.
LNK	75	Link The applicable control block section of the buffer provides the control characters for this command. The control characters for this command were placed there by a previous command. Once the control characters are obtained, the command is identical with the Seek/Link command.

Status and Substatus

Status should be checked (1) at the time the instruction or command sequence is issued, and (2) when the operation is completed. The two statuses reflect different conditions and appear at different times; however, if the first is not checked at the time the instruction is issued, the status at a time when the operation should have completed could be a status indicating an invalid command and that the operation was never initiated.

Status of the CPC is always available in the R-register. To interrogate the status of the disc controller, a Request Status (RQS) command must be issued.

The major status and substatus conditions associated with the DSU204 disc storage subsystem are summarized in Figure G-8.

FUNCTION	Bits 4-1	Bits 10-5
Status and Substatus	Major Status Code	Substatus Code
CHANNEL READY	0000	
DEVICE BUSY	0001	
Overridable		000000
Not Overridable		000001
ATTENTION	0010	
DATA ALERT	0011	
Transfer Timing Alert		000001
Transmission Parity Alert		0xxx10
Invalid Control Character		0xx1x0
Internal Alert		xx1xx0
Check Character Alert		x1xxx0
Block Compare Alert		1xxxxx
Buffer Committed		11xxxx
END OF FILE	0100	
COMMAND REJECTED	0101	
Invalid Operation Code		0000x1
Invalid Device Code		00001x
Illegal Buffer Address, or Buffer Committed		00x1xx
Internal Error		001xxx
INTERMEDIATE	0110	
CHANNEL BUSY	1000	
CHANNEL ABSENT	1001	
CHANNEL ALERT	1010	

x = 0 or 1

Figure G-8. Status and Codes for the DSU204 Subsystem

NOTE: CHANNEL READY, CHANNEL BUSY, CHANNEL ABSENT, and CHANNEL ALERT are status conditions of the CPC. All other status conditions listed in Figure G-8 pertain to the disc storage unit or disc storage controller.

MAGNETIC TAPE UNITS

Detailed information on the programming and operation of magnetic tape units may be found in the reference manuals pertaining to magnetic tape subsystems.

Magnetic Tape Instructions

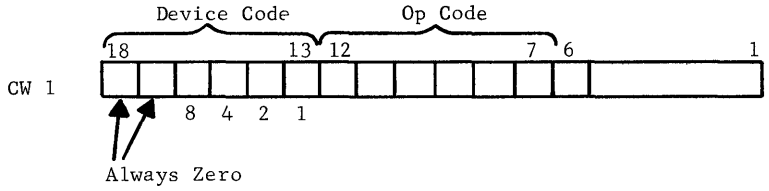
Brief functional descriptions of magnetic tape instructions are given below.

Instruction	Mnemonic	Op Code (Octal)
Read Tape	RT	05
Read Tape Decimal	RTD	04
Reread Tape	RR	07
Special Reread	SRR	06
Write Tape	WT	15
Write Tape Decimal	WTD	14
Write End-of-File Record	WEF	55
Forward Space One Record	FSR	44
Forward Space One File	FSF	45
Backspace One Record	BSR	46
Backspace One File	BSF	47
Erase	ERS	54
Set Density High	SDH	60
Set Density Low	SDL	61
Rewind	RWD	70
Rewind/Standby	RWS	72
Request Status	RQS	00
Reset Status	RSS	40

Instructions	Mnemonic
READ TAPE: Reads one tape record in the binary (standard) format.	RT
READ TAPE DECIMAL: Reads one tape record in the special decimal (BCD) format.	RTD
REREAD TAPE: Rereads binary records at normal, high, and low gain.	RR
SPECIAL REREAD TAPE: Rereads decimal records at normal, high, and low gain.	SRR
WRITE TAPE: Writes one tape record in the binary (standard) format.	WT
WRITE TAPE DECIMAL: Writes one tape record in the special decimal (BCD) format.	WTD
WRITE END-OF-FILE RECORD: Writes an end-of-file record on tape.	WEF
BACKSPACE ONE RECORD: Moves the tape backward without data transfer over one record and positions the tape to read or write the record passed over.	BSR
BACKSPACE ONE FILE: Moves tape backward without data transfer until end-of-file record is detected and positions the tape to again read or write the file just passed over.	BSF
FORWARD SPACE ONE RECORD: Moves tape forward over one record without data transfer and positions the tape to read or write over the next sequential record.	FSR
FORWARD SPACE ONE FILE: Moves tape forward without data transfer until an end-of-file record is detected and positions the tape to read or write the record following the detected end-of-file record.	FSF
ERASE: Erases approximately 8-1/2 inches of tape, beginning at the tape's position when the instruction is received.	ERS
SET DENSITY HIGH: Sets the addressed tape unit to the high-density mode.	SDH
SET DENSITY LOW: Sets the addressed tape unit to the low-density mode.	SDL
REWIND: Moves tape backward without data transfer until the beginning-of-tape marker is sensed.	RWD
REWIND/STANDBY: Moves tape backward without data transfer until the beginning-of-tape marker is sensed and puts the tape unit in a standby status.	RWS
REQUEST STATUS: Obtains and stores the status existing within the addressed tape unit or subsystem.	RQS
RESET STATUS: Resets all resettable status in the related subsystem controller then stores the status of the addressed tape unit at the specified second address after the reset operation.	RSS

Command Words

Command words 1, 2 and 3 to the CPC will contain the information defined for the command words. However, the device code field of CW 1 needs further definition.



The device code is right justified and contains the binary number for the tape unit being addressed.

Status and Substatus

The major status and substatus associated with the magnetic tape subsystem are summarized in Figure G-9.

Condition	Major Status Code	Substatus Code
CHANNEL READY	0000	
Tape Unit Write Inhibited		0000x1
Tape Reel on Load Point		00001x
DEVICE BUSY	0001	
ATTENTION	0010	
Tape Write Inhibited		0xxxx1
No Such Tape Unit		0xxx1x
Tape Unit Standby		0x01xx
Tape Unit Check		0x10xx
Blank Tape on Write *		01xxxx
DATA ALERT	0011	
Transfer Timing Alert		000001
Blank Tape on Read		xxxx10
Transmission Parity Alert		xxx1x0
Lateral Parity Alert		xx1xx0
Longitudinal Parity Alert		x1xxx0
End of Tape		1xxxx0
Bit Detected During Erase		xxxx11
END OF FILE	0100	
Single Data Character		xxxxxx
Data Alert		111111
COMMAND REJECTED	0101	
Invalid Operation Code		0xxxx1
Invalid Device Code		0xxx1x
Parity Alert on Device Operation Code		0xx1xx
Tape on Load Point		0x1xxx
Read After Write on Same Unit		01xxx
LOAD OPERATION COMPLETE	0111	
CHANNEL BUSY	1000	
CHANNEL ABSENT	1001	
CHANNEL ALERT	1010	

x = 0 or 1

* Blank Tape on Write also causes Tape Unit Standby; combined code will be 01x1xx, unless an instruction has reset the Blank Tape on Write.

Figure G-9. Status and Codes for Magnetic Tape Subsystem

PRINTER

Additional information for the PRT200 and PRT201 printers may be found in their reference manuals.

Printer Instructions

Printer instructions are shown in the chart below.

Instruction	Op Code (Octal)
Print in the Edit Mode--No Page Control Information	30
Print in the Edit Mode--Advance Single Line	31
Print in the Edit Mode--Advance Double Line	32
Print in the Edit Mode--Advance to Top of Page	33
Print in the Nonedit Mode--Advance No Lines	10
Print in the Nonedit Mode--Advance Single Line	11
Print in the Nonedit Mode--Advance Double Line	12
Print in the Nonedit Mode--Advance to Top of Page	13
Advance Single Line	61
Advance Double Line	62
Advance to Top of Page	63
Request Status	00
Reset Status	40

Command Words

CW 1 to the CPC contains the operation code for the printer operation. CW 2 contains the starting address of the characters to be printed. CW 3 contains the count of the number of characters in the print line.

For each print line, the CPC must be given a new sequence of command words. When print and line control commands are combined, the printing is always executed first. If any page advancement other than single line, double line, or top of page is desired, a special line control character must be used, preceded by a print in edit mode command.

End Print Line

The computer system must indicate that print-line data is complete by transmitting the End Data Transfer signal. The End Data Transfer signal is generated by the character counter in the CPC. When the character counter counts to zero, an End Data Transfer signal is sent to the printer. Depending upon the nature of the print line, the counter may have to be changed for each line.

Print in Edit Mode

Additional information required by the printer must be contained in the print line data. The additional information is in the form of five special characters when printing in the edited mode.

Special Characters

The special characters are Escape, Ignore, Space, Skip and Line Control (Slew).

Character	Symbol	Binary	Octal
Escape	!	111111	77
Ignore	?	001111	17
Space	/b	010000	20
Skip	None	10xxxx	Varies
Line Control (Slew)	None	0xxxxx	Varies

ESCAPE CHARACTER. When the Escape character (111111) is received by the printer, special consideration is given to the character that follows. If only one Escape character is used, the Escape character and the character that follows are both deleted from the print line. When two consecutive Escape characters are used, both characters are deleted; and the character that follows the two Escape characters is printed. Thus the Escape character can be used to delete or force printing of the special characters discussed below.

IGNORE CHARACTER. An Ignore character (001111) not preceded by an Escape character will be deleted from the print line; and the succeeding characters will be printed left-justified. An Ignore character preceded by one Escape character is treated as a Line Control character (advance 15 lines by countdown). An Ignore character preceded by two consecutive Escape characters will be printed as a ?; both Escape characters will be deleted.

SPACE CHARACTER. The Space character (010000) used without Escape characters will cause a blank the width of a print character to be inserted in the print line. As many Space characters as desired can be used to achieve a true spacing effect, and they can be used in combination with the Skip character, the Space character becomes a Line Control character (advance to top of page by VFU tape). When the Space character follows two consecutive Escape characters, the Space character is printed as a /b; both Escape characters are deleted.

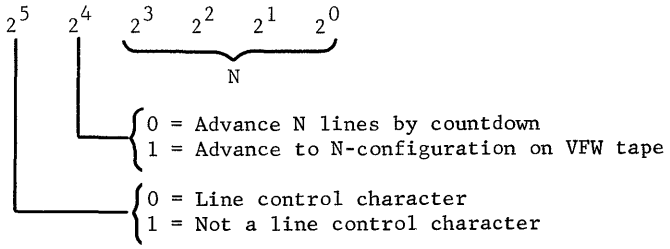
SKIP CHARACTER. When one Escape character is followed by a Skip character (10xxxx), the printer inserts in the print line the number of spaces indicated by the pattern of 1-bits in the four low-order positions of the Skip Character. The bits are read in multiples of 8 as follows:

Bit	Meaning
2^5 - 1 2^4 - 0	Indicate skip character
2^3 ---	Insert 64 spaces
2^2 ---	Insert 32 spaces
2^1 ---	Insert 16 spaces
2^0 ---	Insert 8 spaces

A minimum of 8 spaces and a maximum of 120 spaces can be inserted with one Skip Character. It can be combined with Space characters to achieve numbers which are not multiples of 8. These characters spaces must be counted as print-line characters when figuring the maximum of 136 characters per line.

LINE CONTROL CHARACTER. Any character which has a zero in the high-order bit and is immediately preceded by an Escape character is treated as a Line Control character. The four low-order bits contain the line control information, referred to as N. The next-to-highest-order bit tells the printer whether to advance the page by countdown or by VFU tape.

The meaning of each bit is illustrated below:



The 00xxxx configuration calls for an advancement of N lines by countdown, using a 4-bit counter in the logic to keep track of the number of lines advanced. In this case, the four low-order bits are read as a binary value to represent the number of lines to be advanced. Paper can be advanced from 0 to 15 lines by countdown.

The 01xxxx configuration causes the printer to advance the page until the VFU detects a punched configuration on the VFU tape that matches the configuration in the N-portion of the line control character. Fifteen unique configurations can be used on the VFU tape per form page. The character 010000 is interpreted as an advancement to top of page.

The printer interprets the receipt of a line control character as an indication that the transfer of print-line data has been completed. Also, a line control character transmitted with print-line data will always override any line control information in a line control command.

SUMMARY OF SPECIAL CHARACTERS. Eleven possible configurations of the special editing characters are summarized in Figure G-10. These are presented in binary for simplicity, since some characters cannot be converted to octal until X-values are filled in.

Print in Nonedit Mode

The four print commands for the nonedit mode are similar to those for printing in the edit mode, except that special editing characters are not recognized by the printer logic. Line control information must be included as part of each command.

Character and Sequence			Deleted from Print Line	Printed	Other Action
No. 1	No. 2	No. 3			
111111	11xxxx		Both		None, unless No. 2 is an Escape character
111111	111111	xxxxxx	No. 1 & 2	No. 3	Prints any No. 3 character
111111	00xxxx		Both		Advancd xxxx (N) lines by countdown
111111	01xxxx		Both		Advance to xxxx (N) on VFU tape
111111	10xxxx		Both		Insert xxxx character spaces in print line in multiples of 8
001111			No. 1		Prints remaining characters left-justified
111111	001111		Both		Ignore; treated as advance 15 lines by countdown
111111	111111	001111	No. 1 & 2	No. 3	Prints Ignore as a question mark
010000				No. 1	Prints as a blank character space
111111	010000		Both		Space character treated as advance to top of page by VFU tape
111111	111111	010000	No. 1 & 2	No. 3	Space character prints as a ♂

Figure C-10. Summary of Special Characters Used in Edit Mode

Special characters that are deleted from the print line in the edit mode are printed in the nonedit mode. Escape is printed as an exclamation point, Ignore as a question mark, and Space as a blank character space. Line Control and Skip will print as one of the 64 characters of the standard character set, depending on the octal value assigned by the programmer. Because the Line Control character is not recognized in this mode, it is possible to advance only one line, two lines, or to top of page, by command. The Line Control character cannot be substituted for an End Data Transfer signal to indicate the end of the print line.

Automatic Page Advancement

Automatic starting and stopping of page advancement from punches in channels 5 and 6 of the VFU tape loops require special consideration by the programmer. The action of the printer depends on the method of giving line control information and the circumstances under which the punches are encountered.

When advancing the page by a program, if a punch is detected in channel 5, paper moves until the channel-6 punch stops the automatic page advancement. The printer continues counting lines while the automatic page advancement is in effect. If the countdown is satisfied before the channel-6 hole is reached, the page advancement continues to the automatic-stop punch in channel 6. If the countdown page advancement is not completed, then it continues until all lines called for by countdown are advanced.

If the command calls for advancement to N on the VFU tape, a channel-5 punch causes automatic advancement to take over until the channel-6 punch is reached. If the N-configuration on the tape has not been reached after the automatic advancement, the advancement resumes until N is reached. If the N-configuration is reached before the automatic advancement stop hole is reached, the automatic advancement continues until the channel-6 punch is detected.

In both types of command page advancement, the rule to remember is that paper advances to the farthest spot before the combination of programmed and automatic page advancement is considered complete.

As mentioned in the discussion of Line Control characters, automatic page advancement is ignored when advancement is accomplished by a Line Control character. However, if the Line Control character causes the paper to stop on a channel-5 punch, then the automatic advancement to the channel-6 punch occurs.

Controls and Indicators

The MANUAL CLEAR button on the DATANET-30 control panel also resets the printer. The OPERATE/RESET button on the printer must be pressed after manual clear to return the printer to the operate mode.

Status and Substatus

Major status and substatus associated with the PRT200 and PRT201 printers are shown in Figures G-11 and G-12.

Status and Substatus	Major Status Code	Substatus Code
CHANNEL READY	0000	
Attention	0010	
Out of Paper		00xxx1
Manual Halt		00xx1x
VFU Alert		00x1xx
Check		001xxx
DATA ALERT	0011	
Transfer Timing Alert		000011
Alert Before Printing Started		xxxx1x
Alert After Printing Started		xxx1xx
Paper Low		xx1xxx
Line Control Alert		x1xxxx
Top of Page Echo		1xxxxx
COMMAND REJECTED	0101	
Invalid Operation Code		xx0001
Line Control Alert		x1000x
Top of Page Echo		1x000x
CHANNEL BUSY	1000	
CHANNEL ABSENT	1001	

x = 0 or 1

Figure G-11. Status Codes for PRT200 Printer

Status and Substatus	Major Status Code	Substatus Code
CHANNEL READY	0000	
Normal/Halt		000000
Print One Line		000001
Forward Space		000010
Forward T.O.P.		000011
Invalid Line		000100
Reverse/Rewind		000101
Back Space		000110
Back Space T.O.P.		000111
ATTENTION	0010	
Out of Paper		00xxx1
Manual Halt		00xx1x
VFU Alert		00x1xx
Check		001xxx
DATA ALERT	0011	
Transfer Timing Alert		xxx011
Alert Before Printing Started		xxx01x
Alert After Printing Started		xxx100
Paper Low		0x1xxx
Line Control Alert		x1xxxx
Top of Page Echo		1x0xxx
COMMAND REJECTED	0101	
Invalid Operation Code		xx0001
Line Control Alert		x1000x
Top of Page Echo		1x00xx
CHANNEL BUSY	1000	000000
CHANNEL ABSENT*	1001	000000

x = 0 or 1
* Returned by I/O channel of GE-400 Series only

Figure G-12. Status and Codes for PRT201 Printer

CARD READER

For further information refer to the reference manuals pertaining to card readers.

Card Reader Instructions

Following are descriptions of CRZ200 and CRZ201 card reader instructions.

INSTRUCTION	MNEMONIC	OP CODE (OCTAL)
Read Card Binary	RCB	01
Read Card Decimal	RCD	02
Read Card Mixed	RCM	03
Request Status	RQS	00
Reset Status	RSS	40

INSTRUCTION	DESCRIPTION
Read Card Binary	Data from the top half of each column (rows 12-3) is transmitted first, supplemented by an odd parity bit. Data from the lower half of the column (rows 4-9) is transmitted second. One and one-half card columns fill each memory locations. Columns 1-79 fill the first 53 memory words. The 54th word contains the first character of data from column 80.
Read Card Decimal	The contents of each card column punched in the Hollerith format are converted to the equivalent 6-bit character and transmitted with an odd parity bit. In addition, a check is made to see that the punches in each column represent a valid character of the General Electric standard character set. Three card columns of data fill one memory word. Thus, columns 1-78 occupy 26 locations of memory. Word 27 contains data from columns 79 and 80.
Read Card Mixed	As each card is read, column 1 is examined to determine the type of card and, thus, how the data is to be handled. If the "7" and "9" of column 1 are punched, regardless of what other punches occur in the column, the card is read in the binary mode. If either or both of these two punches are missing, the card is read in the alphanumeric mode. In either case, the full 80 columns of card information are transmitted, including column 1. No Hollerith characters are represented by both the 7 and 9 punches, either with or without other punches. Therefore, the card reader interprets a punch configuration in column 1 with the special identifying 7 and 9 punches as a binary card.

Timing Considerations

Reading is done on a single-card-per-instruction basis. A new instruction must be given for each card. To maintain reading at the rate of 900 cards per minute (15 cards per second), a new read instruction must be given within 1 millisecond after the card reader generates a Terminate signal for the previous card. If the card reader does not receive a new read instruction within this time, speed drops in proportion to the delay.

Data Transfer

The sequence for reading characters from a card in the binary mode is shown in Figure G-13.

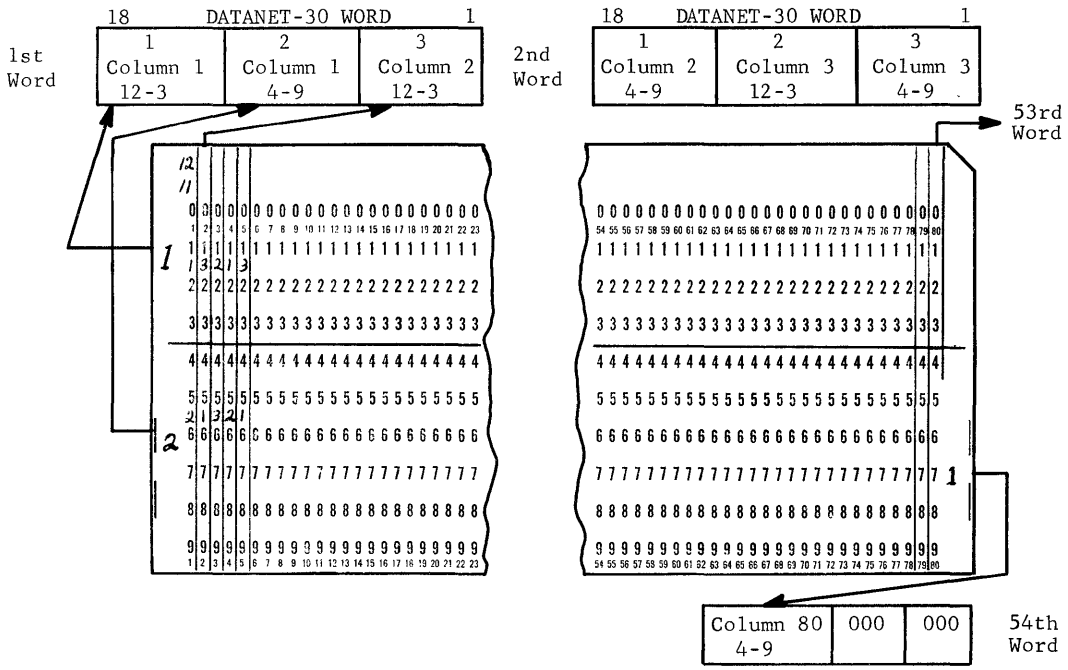


Figure G-13. Character Sequence for Read Card Binary Instruction

The sequence for reading characters from a card in the decimal mode is shown in Figure G-14.

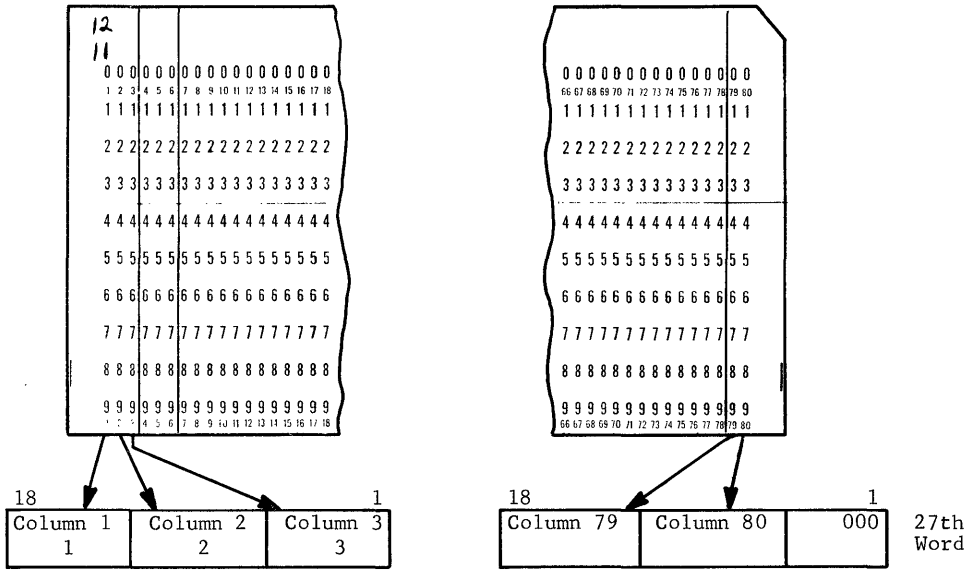


Figure G-14. Character Sequence for Read Card Decimal Instruction

Program Load

The DEF 3 instruction to the CPC is sent to the card reader as a program load command. The card reader will read one card in binary and halt. A Not Busy major status is returned to the CPC.

Status and Substatus

The major status and substatus associated with the CRZ200 and CRZ201 card readers are shown in Figure G-15.

Condition	Major Status Code	Substatus Code
CHANNEL READY	0 0 0 0	
ATTENTION	0 0 1 0	
Hopper/Stacker Alert		x x x x x 1
Manual Halt		x x x x 1 x
Last Batch		x x x 1 x x
Feed Alert		x x 1 x x x
Card Jam		x 1 x x x x
Read Alert		1 x x x x x
DATA ALERT	0 0 1 1	
Transfer Timing Alert		0 0 0 0 0 1
Validity Alert		0 0 0 0 1 0
COMMAND REJECTED	0 1 0 1	
LOAD OPERATION COMPLETE	0 1 1 1	
CHANNEL BUSY	1 0 0 0	
CHANNEL ABSENT	1 0 0 1	
CHANNEL ALERT	1 0 1 0	

x = 0 or 1

Figure G-15. Status and Codes for CRZ200 and CRZ201 Card Readers

CPZ100 CARD PUNCH

Additional information for the CPZ100 (100 cards per minute) card punch may be found in the GE-200 Series Punched Card Subsystems reference manual, CPB-302.

CPZ100 Card Punch Instructions

INSTRUCTION	MNEMONIC	OP CODE (OCTAL)
Punch Card Binary	PCB	11
Punch Card Decimal	PCD	12
Punch Card Edited Decimal	PCE	13
Request Status	RQS	00
Reset Status	RSS	40

INSTRUCTION	DESCRIPTION
Punch Card Binary	Two 6-bit binary characters are punched into each card column. The first character goes into card rows 12-3 (row 12 contains the most-significant bit). The second character is punched into card rows 4-9 (row 4 is the most-significant bit). The third and fourth characters are punched in column 2, etc.
Punch Card Decimal	Each 6-bit data character received is converted into the standard Hollerith punch code and punched into a single card column.
Punch Card Edited Decimal	Identical with the alphanumeric mode, but with the additional feature of allowing the punch to delete any Ignore characters (octal 17) which it may receive. Whenever an Ignore character is deleted, the next valid character received is punched, with no blank column intervening.

Command Words

Command words 1, 2, and 3 to the CPC must contain the operation code, starting address, and character count, as applicable. To punch a card, the same command sequence and data must be transferred to the punch 12 times.

Timing Considerations

As described above, a punch command must be received for punching each of the 12 rows of the card. The same set of punch data is transmitted to the punch for each row. The punch picks out the applicable bit from each data character, based on the row to be punched. The DATANET-30 must issue each punch command and data in time to punch each row. Approximately 600 milliseconds are required to punch each card.

There are 28.4 milliseconds between rows in which to give the punch command and complete data transfer. The punch circuitry requires 3.2 milliseconds to complete the data transfer. Therefore, the DATANET-30 must issue the command sequence to the punch for the next row within 25.6

milliseconds after each Terminate signal. The punch command sequence can be transferred to the CPC only after each Terminate signal from the punch. The punching time for each row is 14.4 milliseconds. Following this, there are 4.4 milliseconds for reading the corresponding row of the preceding card. Parity is generated and started as each row is punched. When the row is read, parity is checked. If parity does not check, the error is indicated after the card following the one being checked has been punched.

After all the cards have been punched, the last card is still in the punch. Two more cards must be fed through the punch either manually or by program in order to clear the punch mechanism of all punched cards. The card punch timing cycle is shown in Figure G-16.

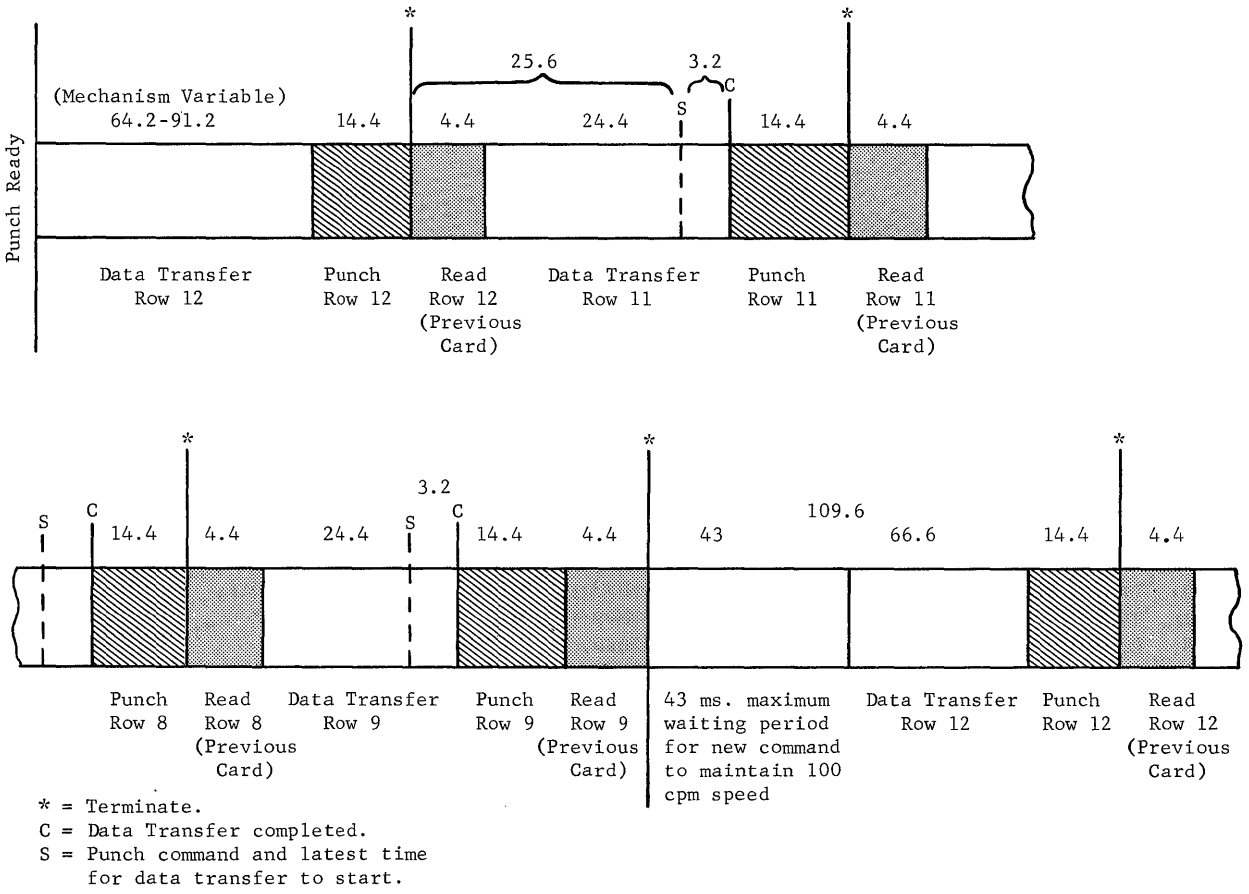


Figure G-16. Card Punch Timing Cycle (in Milliseconds)

After the last row of the card is punched and row 9 of the preceding card is read, a punch command may be received for row 12 of the next card within 43 milliseconds. This permits the 100 card-per-minute punching rate to be maintained. If the new command is received during this 43-millisecond interval , approximately 66 additional milliseconds are available for the transfer of punch data for the first row. If a punch command is not received during this period, there is a 7-card-per-minute reduction in the over-all card punching rate. There will be an additional 7-card-per-minute reduction in speed for every additional 43 milliseconds of delay in receiving this first command.

Data Transfer

The sequence for punching characters into a card in the binary mode is shown in Figure G-17.

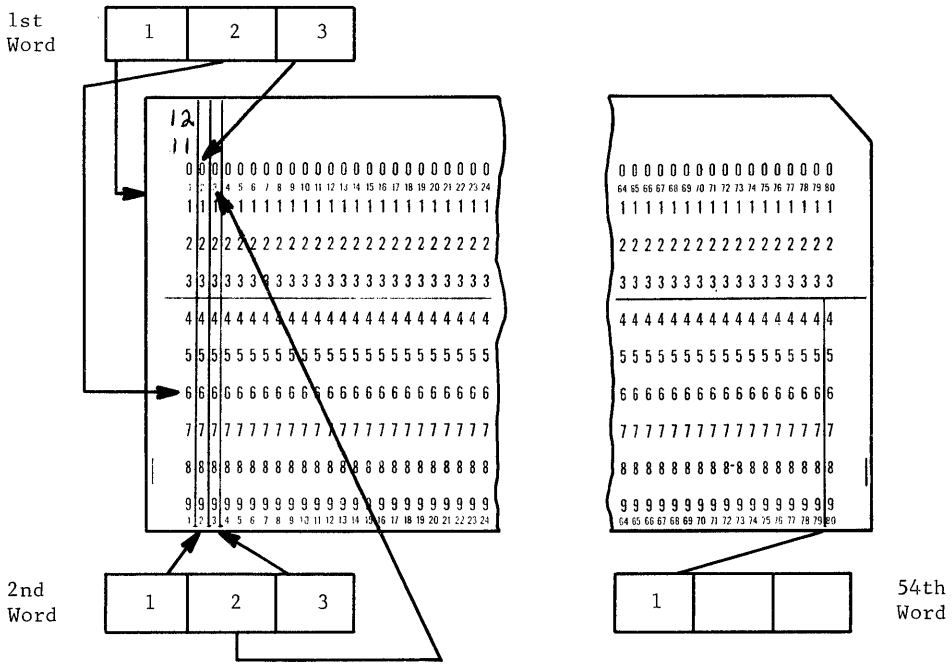


Figure G-17. Character Sequence for Punch Card Binary Instruction

The sequence for punching characters into a card in the decimal mode is shown in Figure G-18.

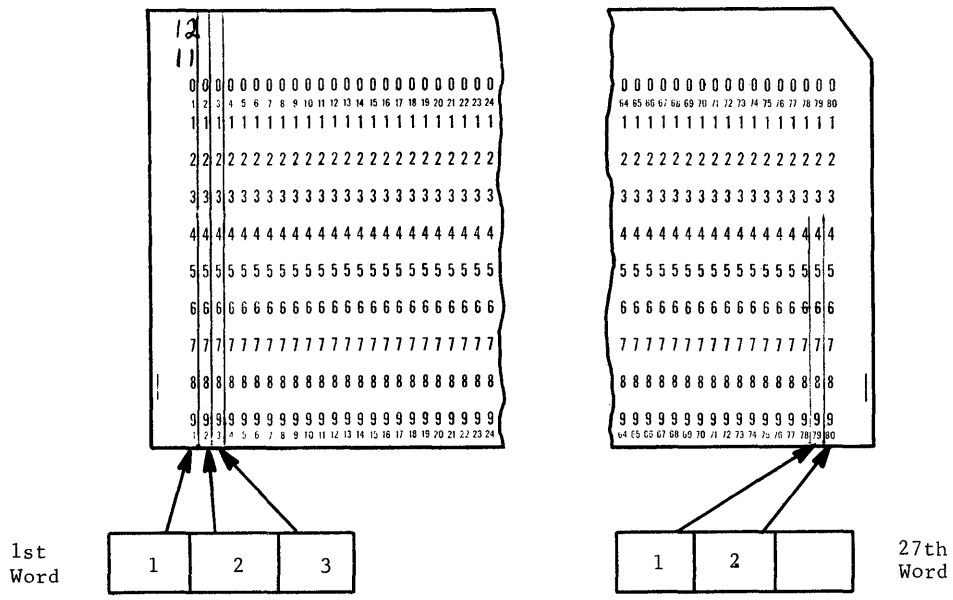


Figure G-18 Character Sequence for Punch Card Decimal Instruction

Status and Substatus

Major status and substatus for the CPZ100 card punch are listed in Figure G-19.

Status and Substatus	Major Status Code	Substatus Code
CARD PUNCH READY	0000	
ATTENTION	0010	
Hopper/Stacker Alert		0xxxx1
Manual Halt		0xxx1x
Chad Box Full		0xx1xx
Feed Alert		0x1xxx
Card Jam		01xxxx
DATA ALERT	0011	
Transfer Timing Alert		000xx1
Transmission Parity Alert		000x1x
Punch Alert		0001xx
COMMAND REJECTED	0101	
INTERMEDIATE	0110	
CHANNEL BUSY	1000	
CHANNEL ABSENT	1001	

x = 0 or 1

Figure G-19. Status and Codes for CPZ100 Card Punch

CPZ200 AND CPZ201 CARD PUNCHES

Additional information for the CPZ200 and CPZ201 300-card-per-minute punches may be found in the applicable reference manuals.

CPZ200 and CPZ201 Card Punch Instructions

Instructions for the CPZ200 and CPZ201 card punches are described below.

INSTRUCTION	MNEMONIC	OP CODE (OCTAL)
Punch Card Binary	PCB	11
Punch Card Decimal	PCD	12
Punch Card in Edited Mode	PCE	13
Request Status	RQS	00
Reset Status	RSS	40

INSTRUCTION	DESCRIPTION
Punch Card Binary	Two 6-bit binary characters are punched into each card column. The first character goes into card rows 12-3 (row 12 contains the most-significant bit). The second character is punched into card rows 4-9 (row 4 contains the most-significant bit). The third and fourth characters are punched in column 2, etc.
Punch Card Decimal	Each 6-bit data character is converted into the standard Hollerith punch code and punched into a single card column.
Punch Card in Edited Mode	Identical with the alphanumeric mode, but with an additional feature--the punch deletes any Ignore characters (octal 17) from the data. Whenever an Ignore character is deleted, the next valid character is punched, with no blank column intervening.

Command Words

Command Words 1, 2 and 3 to the CPC must contain the operation code, starting address, and character count as applicable. To punch a card, the command sequence and data transfer are transferred to the punch once.

Functional Description

The subsystem becomes busy when a punch command is received and accepted. When the punch becomes busy, it requests data for the card. Data is transmitted, character by character, from the processing system to the card image buffer of the punch controller. The parity of each character is checked as it is received. If the command is Punch Card Decimal the character is converted by the controller to Hollerith code before the data enters the buffer.

As row 12 of the first card passes over the punch dies, the control electronics extract the row-12 information from the card image buffer and activate the punching mechanism. The punch remains

in the busy state, punching data row by row until the last row of the card is completed. It then transmits a Terminate signal, indicating to the processing system that the punch has completed the operation.

The first card is checked while the second card is being punched. As row 12 of the second card enters the punch area, row 12 of the first card starts through the read head. There, row parity is compared against the parity established for the row when the data was first received by the card image buffer. If the two parity checks do not agree, a punch alert signals the discrepancy. After the second card is punched, the results of the read check of the first card are transmitted to the processing system. When the last row has been read and checked, the card continues to the output stacker.

Timing Considerations

The punch controller requires that a punch command and all data for the card image buffer be received before a card is fed and punched. No command or data will be accepted for the next card until a card has been completely punched.

A complete cycle of transferring data to the punch and punching a card requires 200 milliseconds. This is illustrated in Figure G-20. The time is divided into two phases. Phase I is transfer of the command and data to the punch. Phase 2 is the punch operation. After the punch controller has received the punch command and all the data, a signal to feed a card is given. The card is punched and a Not Busy status is indicated in the CPC. When the CPC goes not busy, another punch command sequence must be given for the next card.

The transfer of the command and all data to the punch requires approximately 20.5 milliseconds. Since 29 milliseconds are allowed to complete data transfer, a new command sequence must be issued to the CPC (punch) within approximately 8.5 milliseconds after the CPC goes not busy.

If the CPC command sequence is not issued in time to complete the data transfer within the 29 milliseconds, the punch mechanism continues to cycle (at 200 ms/cycle) and will punch a card the next feed cycle time.

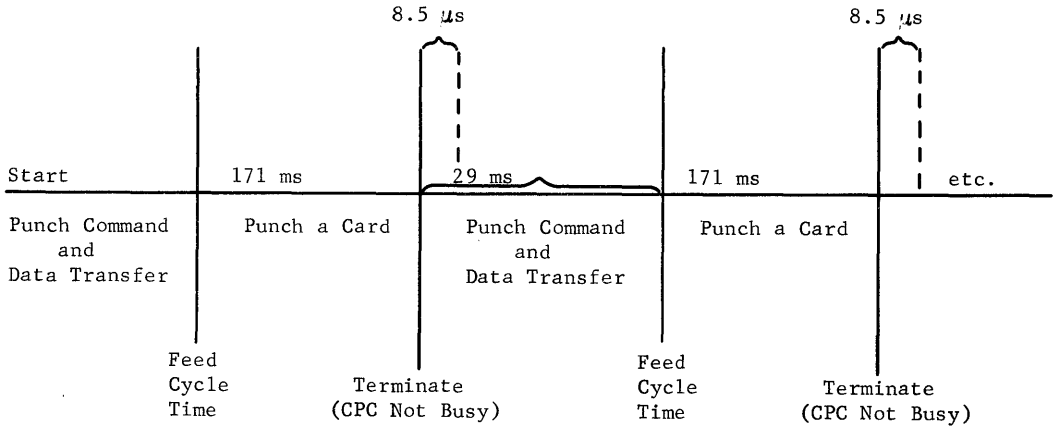


Figure G-20. CPZ200/CPZ201 Punch Cycle

Status and Substatus

Major status and substatus for the CPZ200 and CPZ201 card punches are shown in Figure G-21.

Status and Substatus	Major Status Code	Substatus Code
CARD PUNCH READY	0000	
ATTENTION	0010	
Hopper/Stacker Alert		0xxxx1
Manual Halt		0xxx1x
Chad Box Full		0xx1xx
Feed Alert		0x1xxx
Card Jam		01xxxx
DATA ALERT	0011	
Transfer Timing Alert		000xxx
Transmission Parity Alert		000x1x
Punch Alert		0001xx
COMMAND REJECTED	0101	
INTERMEDIATE	0110	
CHANNEL BUSY	1000	
CHANNEL ABSENT	1001	

x = 0 or 1

Figure G-21. Status and Codes for CPZ200 and CPZ201 Card Punches.

PS6010 PROGRAMMABLE PERIPHERAL SWITCH

The PS6010 Programmable Peripheral Switch is used to connect alternately either of two processors to a single peripheral subsystem controller. Each processor may be a GE-400 Series central processor or a DATANET-30 data communications processor.

Refer to the PS6010 Programmable Peripheral Switch reference manual, CPB-1106, for information regarding programming and operating the switch.

DOCUMENT REVIEW SHEET

TITLE: CPC930 Common Peripheral Channel for DATANET-30

CPB #: 1254A

FROM:

Name: _____

Position: _____

Address: _____

_____

Comments concerning this publication are solicited for use in improving future editions. Please provide any recommended additions, deletions, corrections, or other information you deem necessary for improving this manual. The following space is provided for your comments.

COMMENTS: _____

Please cut along this line

NO POSTAGE NECESSARY IF MAILED IN U.S.A.
Fold on two lines shown on reverse
side, staple, and mail.

STAPLE STAPLE

FOLD

FIRST CLASS
PERMIT, No. 4332
PHOENIX, ARIZONA

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

POSTAGE WILL BE PAID BY

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
13430 NORTH BLACK CANYON HIGHWAY
PHOENIX, ARIZONA - 85029

ATTENTION: DOCUMENTATION STANDARDS AND PUBLICATIONS B-90

FOLD

Progress Is Our Most Important Product

GENERAL ELECTRIC

INFORMATION SYSTEMS DIVISION

LITHO U.S.A.

84.1