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FABRI-TEK INC.
COMPUTER SYSTEMS

PRODUCT DESCRIPTION

MODEL 4511

CACHE

MEMORY BUFFER

From Seattle.

FABRI-TEK® INC.
COMPUTER SYSTEMS

MODEL 4511 MEMORY BUFFER

A high speed Semiconductor Memory designed to increase the apparent or effective speed of Core Memory.

For the

DIGITAL EQUIPMENT CORPORATION PDP 11/45 COMPUTER

☐ ACHIEVE TWICE THE COMPUTER PERFORMANCE: BY OPERATING THE MODEL 4511 HIGH SPEED MEMORY BUFFER IN CONJUNCTION WITH THE COMPUTER CORE MEMORY, YOUR EFFECTIVE PROCESSING SPEED CAN BE INCREASED UP TO TWICE YOUR PRESENT RATE. THAT COMPARES IN SPEED TO THE D.E.C. MOS MEMORY.

☐ ALL *UNIBUS MEMORY ADDRESS LOCATIONS ARE BUFFERED: EVERY AVAILABLE CORE MEMORY ADDRESS LOCATION ON THE *UNIBUS IS UNDER BUFFER CONTROL WHICH ACCOMPLISHES UNEXCELLED PERFORMANCE THROUGHOUT THE ENTIRE 0-124K ADDRESS FIELD OF THE PDP 11/45. THIS ELIMINATES THE NEED FOR HIGH PRICED MOS MEMORY WITH LIMITED (32K max.) ADDRESS STORAGE.

☐ ON/OFF LINE SWITCH: A SWITCH IS PROVIDED WITHIN THE MEMORY BUFFER TO ALLOW FOR EASE OF ON-LINE OR OFF-LINE OPERATION.

☐ PERFORMANCE VERSUS PRICE: THERE IS NO OTHER PRODUCT AVAILABLE ON THE MARKET WHICH CAN YIELD THIS IMPROVED PERFORMANCE FOR SUCH A SMALL PERCENTAGE OF YOUR OVERALL SYSTEM PRICE.

☐ PLUG-IN COMPATIBILITY: THE ENTIRE MEMORY BUFFER IS CONTAINED ON THREE PRINTED CIRCUIT ASSEMBLIES WHICH CAN BE INSTALLED IN A MATTER OF MINUTES INTO THE PDP 11/45 FAST BUS. A +5.0VDC POWER SUPPLY IS ALSO PROVIDED TO OPERATE THE BUFFER.

☐ NON-VOLATILITY: IN CONTRAST TO SEMI-CONDUCTOR MEMORY THE MODEL 4511 MEMORY BUFFER GUARANTEES PROTECTION OF DATA AGAINST UNEXPECTED AC POWER FAILURE AND POWER TURN ON/OFF.

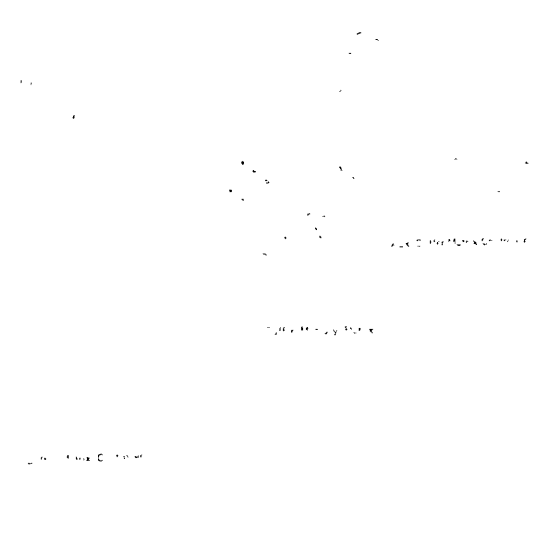
☐ DELIVERY: "OFF-THE-SHELF".

The FABRI-TEK Model 4511 Memory Buffer System has been designed to provide Digital Equipment Corporation PDP 11/45 users the opportunity of achieving twice their present computer performance for a fraction of the original overall system price.

FABRI-TEK can also supply the fastest Add-On Core Memory System for the PDP 11 Series Computer, so no matter what memory performance you desire, why not check with "The Leader in Memory Technology".

*UNIBUS is a trademark of Digital Equipment Corporation.

MODEL 4511 BUFFER SPECIFICATIONS



Model 4511 Buffer Memory System (Individual Components)

PRINCIPLES OF OPERATION

The Buffer System utilizes a write through algorithm. On all CPU DATI Operations (Read from Memory) the address and its corresponding data is mapped into the Buffer from the Unibus. On all successive CPU Fetches (Reads) to this address the data will be in the Buffer and available to the Fastbus of the PDP 11/45. All CPU DATO operations (Write into Memory) take place on the Unibus for any address selected in Core Memory and the Buffer will update itself simultaneously with Core if the selected address is in the Buffer. In this way the Data in the Buffer is identical to that of Core at the same address at all times.

BUFFER ELECTRICAL CHARACTERISTICS

Storage Media
Semiconductor - Bipolar

Word Capacity
512 Words

Word Length
16 Bits

Cycle Time
Compatible with the 300 NS CPU Cycle Time

INTERFACE (Plug Compatible)

The Buffer, which consists of three (3) P.C. Assemblies, is designed to plug directly into the Fastbus (Semiconductor Memory Area) of the PDP 11/45 Computer. Installing the Model 4511 Buffer into this Semiconductor Memory Area restricts the maximum allowable Bipolar or MOS Memory to either 4K or 16K words respectively. Installing the Buffer also requires that Unibus A & B are tied together.

POWER REQUIREMENTS

DC - +5.0VDC Power Supply is provided with the Model 4511 Buffer and installs in location K of the lower H742 Power Supply. This supply is designed to operate from 25VAC±5VAC @ 3.0A and measures 2.75" x 5.25" x 8.40".

BUFFER MECHANICAL CONFIGURATION

The Buffer is contained on three (3) Printed Circuit Assemblies designed to plug directly into PDP 11/45 slot locations No. 21 designated M8110-MEM, No. 22 designated MOS/BIP and No. 24 designated MOS/BIP.

ASSY. NAME	CPU LOCATION	ASSY DIMENSION
Buffer - Matrix Controller	No. 21	15.70" x 8.40" x 0.50"
Buffer - Memory Matrix	No. 22	15.70" x 8.40" x 0.50"
Buffer - Aux. Mat. Controller	No. 24	5.20" x 8.40" x 0.50"

* ALL SPECIFICATIONS SUBJECT TO CHANGE.

FABRITEK INC.
COMPUTER SYSTEMS

5901 SO. COUNTY ROAD 18, MINNEAPOLIS, MINNESOTA 55436

PHONE 612/935-8811

TWX 910-576-2913

Boston 617/969 5077
Chicago 312/437-4116
Dallas 214/661-3155
Denver 303/753-0631
Long Beach 213/420-2493
New Jersey 201/964-4770
San Jose 408/246-8391
Detroit 313/348-2161
Orlando 305/857-1050
Hong Kong K331383
United Kingdom Maidenhead 37321-4
Tokyo (03)432-6901

detailed competitive analysis of both the Fabritek and Cambridge Memory products follows:

brit x Cache Analysis:

e Fabritek model 4511 add-in cache provides 11/45 performance that is approximat equal to a MOS 11/45. When used without memory management it generally provid rfo: ance that lies between MOS and Bipolar. When used with memory management, pr ides performance that is about equal to non-memory-managed MOS and is 10% t % s ower than the Bipolar 11/45. In certain programs (see FFT 45 Benchmark Pro- am Results) it provides performance that is only slightly better than CORE. In sten s with a lot of UNIBUS I/O activity, wither MOS or Bipolar will out-perform e cache, because the CPU will not have to wait for UNIBUS availability as it mus enever there is a cache "miss."

e Fabritek Cache is a very simple 512 word direct mapping cache that fits into a chine that was not designed for a cache in the first place. The 11/70 cache wi s 32-bit memory and dual 512 word mapping scheme was carefully optimised to give ximum processor performance. If a customer feels a cache would help him, he is obvious 11/70 candidate.

britek Cache Pricing:

11,800 when bundled with 8K of Fabritek core. It is believed they will sell the che un-bundled, but no prices are known.

nchmarks have been run on an 11/45 with the Fabretek cache. The results of some them are:

Program Name	Execution Time in Seconds: CPU Memory Type: Bipolar	Fabritek Cache	MOS*	CORE*
FFT 45	4.3	5.9	4.7	6.0
GAUSS	2.5	2.68	2.7	3.1
SINGLE	3.5	3.7	4.0	4.9
HANOI	22.0	28.02	41.0	71.0

* with KT 01

te that in FFT 45, the cache is hardly better than a Core 45, while Bipolar is 3 ster.

mbridge Memories FasBUS 11^R Analysis:

sBUS 11^R MOS from Cambridge Memories is a product that is very similar to our ow 11-BT MOS. It is slightly faster because it uses newer technology chips. It nsists of a control card similar to our own MS11-BC and up to four matrix boards th 4K of parity memory per board (like our MS11-BT), that plug into the solid st mory slots in the 11/45 backplane. They also provide a 5¼" rack mounted power pply that will power up to 32K of their memory in an 11/45.

rformance-wise the FasBUS 11^R Memory is 10% faster than our MOS and 45% slower an our bipolar. A comparison table of memory speeds is given below:

Memory System Speeds: (without Memory Management)

		FASTBUS Cycle Times:	FASTBUS Access Times:
DEC MS11-BT	MOS	510 nsec (max.)	360 nsec
CMI FasBUS 11^R	MOS	450 nsec *	310 nsec *
DEC MS11-AP	Bipolar	330 nsec (max.)	190 nsec

sing, at best they may be able to make 420 nsec times. Thus the 450 nsec should be their real specification.

ASTBUS ACCESS TIMES are meaningless as CPU performance is limited by FASTBUS TIMES!!

S 11^R Pricing:

are pricing the FasBUS 11 at $ 10,500 for 16K.

esent their Memory offers no performance advantage over Bipolar and only a t performance advantage over MOS.

pricing is competitive. Counter this by selling DEC reliability, maintenance ipolar performance as a total solution to their needs.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION I
GENERAL INFORMATION AND SPECIFICATIONS

SCOPE

This manual applies to the FABRI-TEK Model 4511 Cache Memory Buffer.

I GENERAL INFORMATION AND SPECIFICATIONS
II INSTALLATION AND TEST ADJUSTMENTS
III PRINCIPLES OF OPERATION

GENERAL SYSTEM DESCRIPTION

The Model 4511 is a high speed, 512 x 16 Memory Buffer which installs in the PDP 11/45 computer system. Figure 1-1 illustrates the 4511 system. The purpose of the FTI Memory Buffer is to combine the best advantages of core and semi-conductor memories:

- Non-volitility of core memory.
- Low cost of core memory.
- High speed of MOS memory throughout the entire address range of 0-124K as opposed to the 32K maximum address block of MOS memory.

The FTI Memory Buffer combines these advantages by utilizing the two-bus structure of the DEC PDP 11/45 processor in an optimum way to reduce CPU processing time. When desired, up to 16 k of MOS or 4 k of bipolar memory can be installed concurrently with the Buffer on the Fastbus*. In this case the Model 4511 still buffers only the core memory and has no effect on the semiconductor memory.

PHYSICAL DESCRIPTION

The 4511 Memory Buffer consists of the following major assemblies:

—Buffer Matrix Controller module (BMC).
—Auxiliary Buffer Matrix Controller module (ABMC).
—Buffer Memory Matrix module (BMM).
—FTI Model 1744 +5-V d-c Power Regulator module.

The printed circuit modules plug into the semiconductor memory and Unibus A and B slots in the PDP 11/45 chassis. Normally, only minor changes are necessary to the computer. The +5-V d-c

*Registered Trademark of Digital Equipment Corporation.

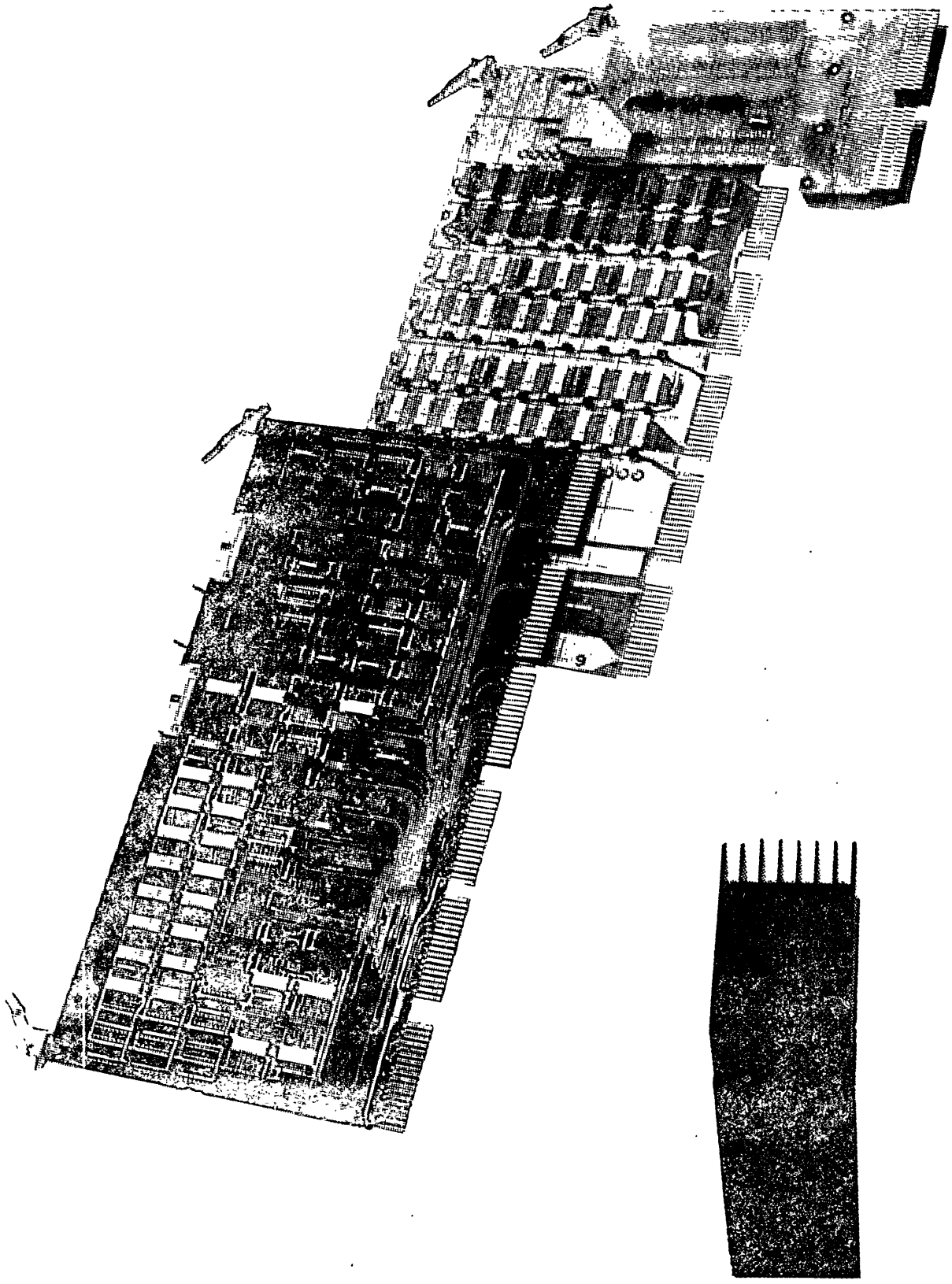


Figure 1-1
MEMORY BUFFER SYSTEM

Power Regulator module installs in location K of the lower "H742" Power Supply. Refer to Section II for physical locations and installation instructions.

Figures 1-2 through 1-5 are photographs of the printed circuit modules and the Power Regulator module. These photographs illustrate significant assembly features.

SPECIFICATIONS AND INTERFACE SCHEMATIC

Table 1-1 summarizes the general 4511 Memory Buffer specifications. Figure 1-6 illustrates the CPU-to-Memory Buffer interface characteristics.

Table 1-1.—SPECIFICATIONS

DATA CAPACITY	
Address	512 Addresses
Word Length	16 Bits
PRINTED CIRCUIT DIMENSIONS (inches) H x D	
Buffer Matrix Controller	15.70 x 8.40
Buffer Memory Matrix	15.70 x 8.40
Auxiliary Buffer Matrix Controller	5.20 x 8.40
Power Regulator	5.10 x 6.50
COOLING	Forced Air
ENVIRONMENT PARAMETERS	
Operating	$0^{o}C$ to $+70^{o}C$
Non-Operating	$-55^{o}C$ to $+100^{o}C$
Humidity (No Condensation)	95%
INTERFACE LOGIC VOLTAGES	
Logic One In	+2.4V to +5.5V
Logic One Out	+2.4V to +5.5V
Logic Zero In	-0.5V to +0.8V
Logic Zero Out	-0.5V to +0.8V
DC POWER REQUIREMENTS	
+5 V dc at 10 Amps Maximum	

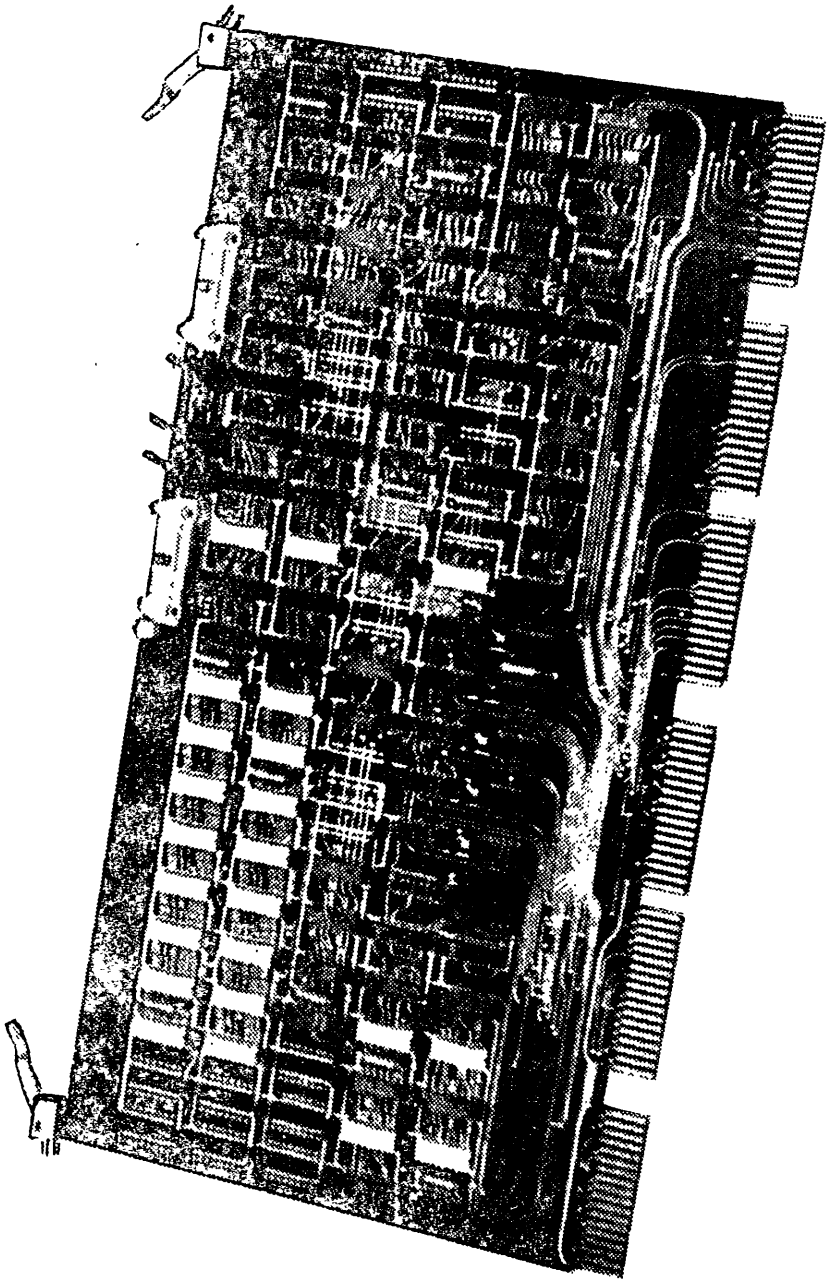


Figure 1-2
BUFFER MATRIX CONTROLLER MODULE

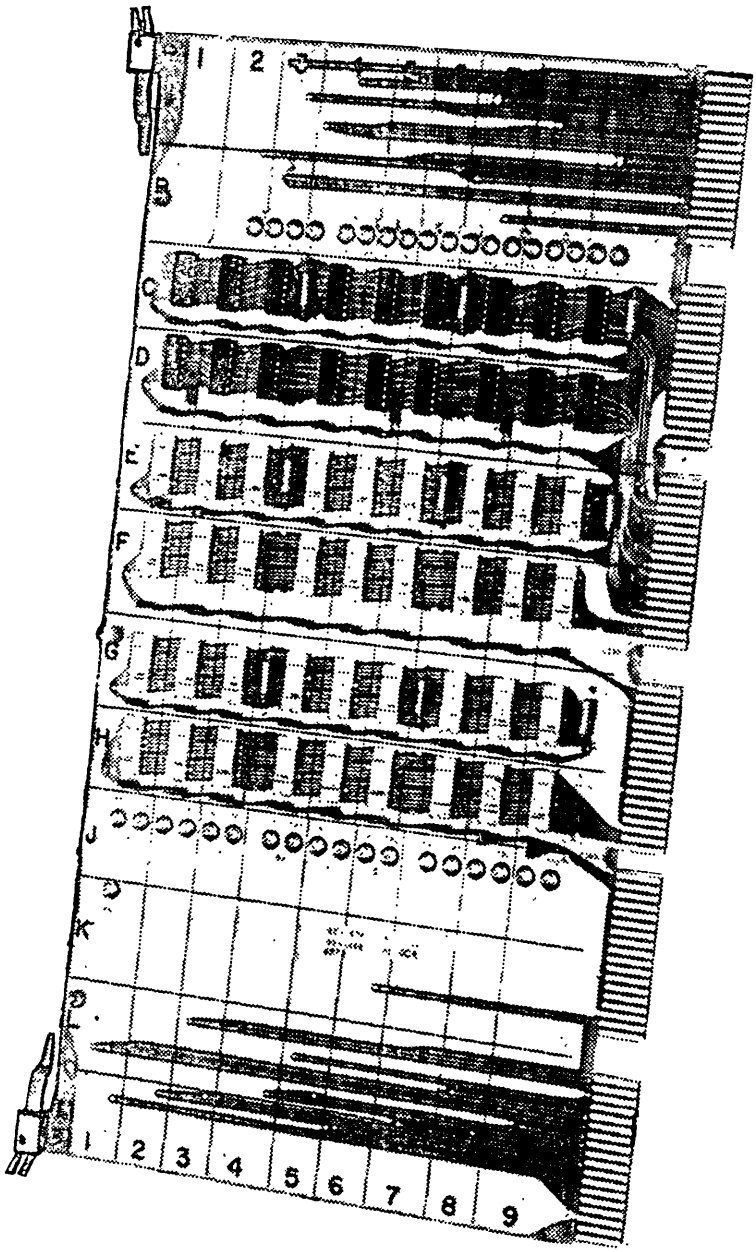


Figure 1-3
BUFFER MEMORY MATRIX MODULE

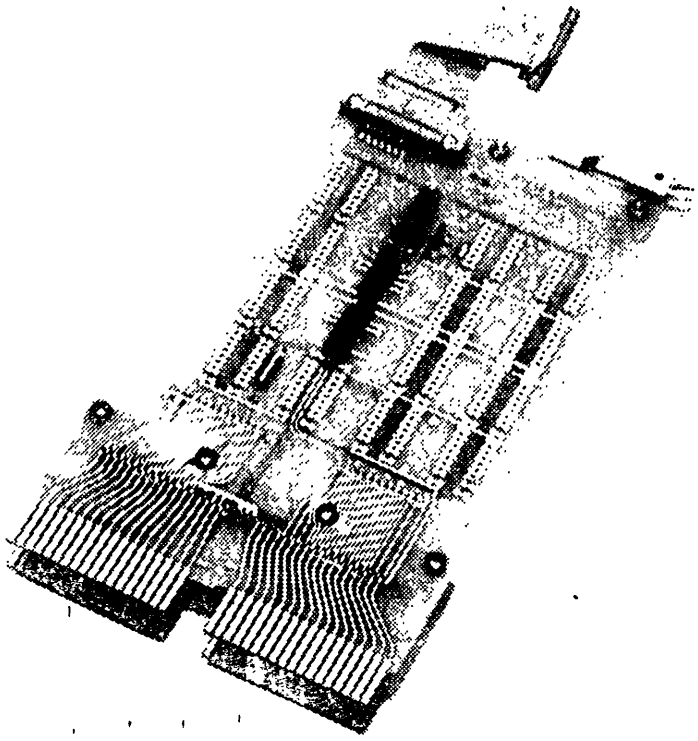


Figure 1-4
AUXILIARY BUFFER MATRIX CONTROLLER MODULE

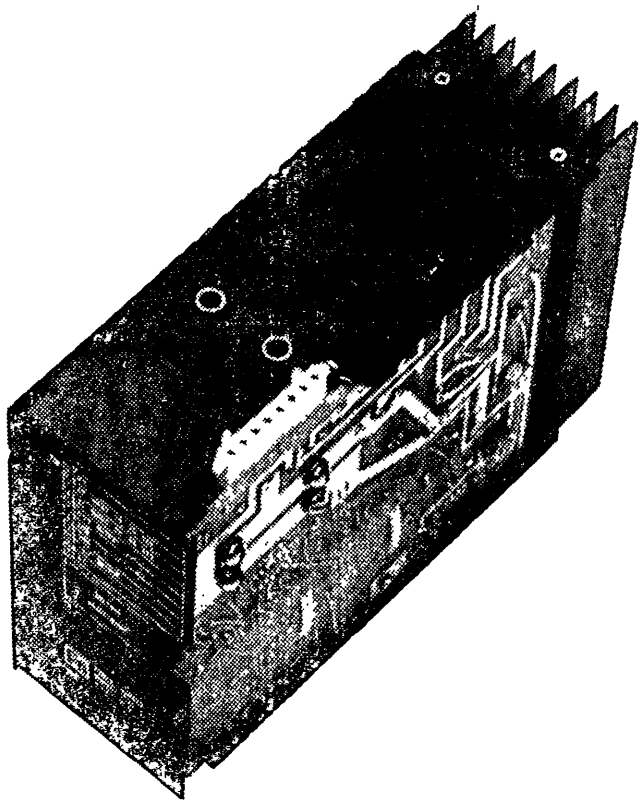


Figure 1-5
MODEL 1744 POWER REGULATOR MODULE

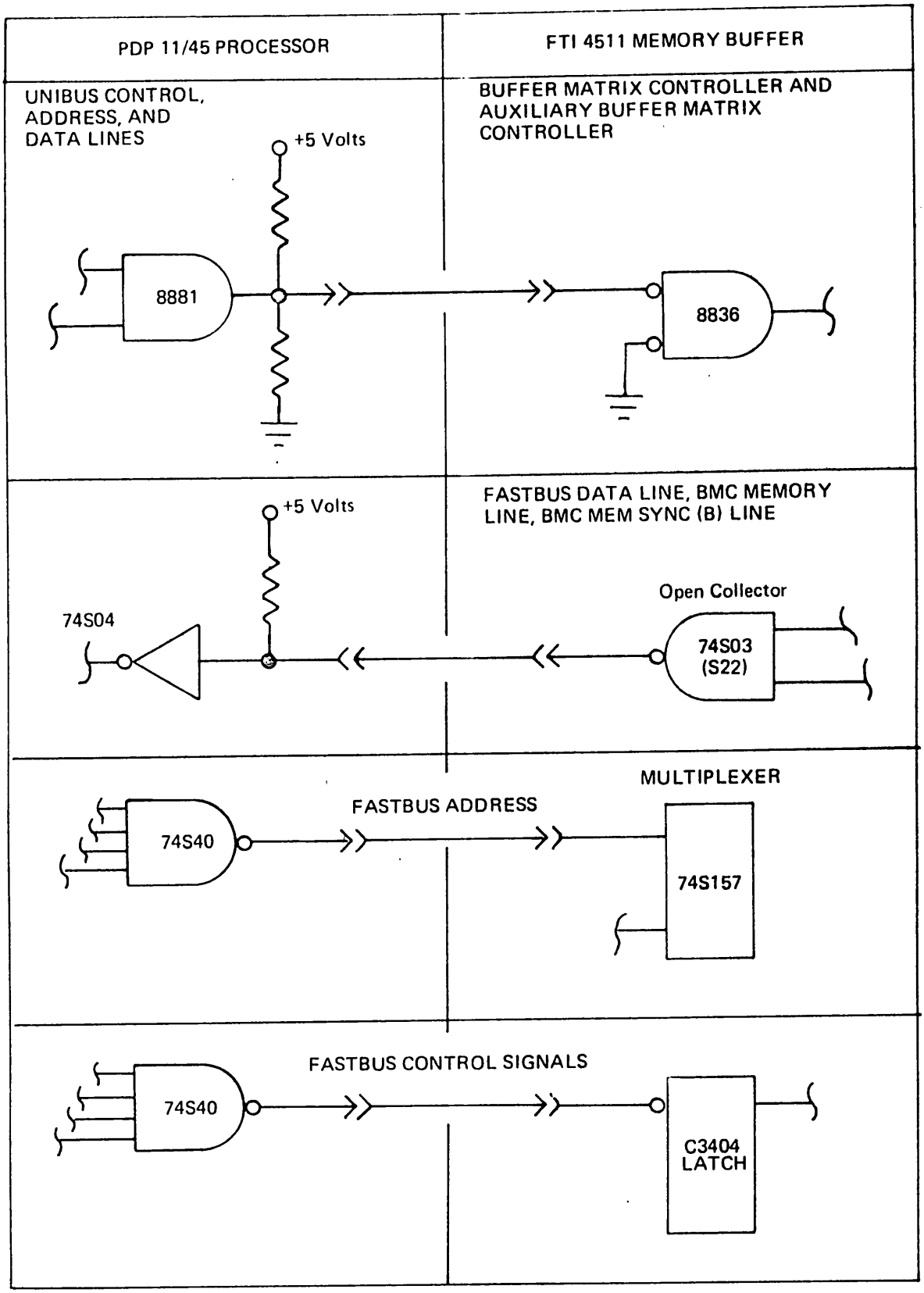


Figure 1-6
CONTROL, ADDRESS, AND DATA INTERFACE SCHEMATIC

SECTION II
INSTALLATION AND TEST ADJUSTMENTS

INTRODUCTION

The DEC PDP 11/45 and the FTI Model 4511 Memory Buffer are integrated by installing the FTI Power Regulator and Memory Buffer modules into the DEC computer. This section contains the installation procedures and test adjustments necessary to install the Memory Buffer into any PDP 11/45. It is important to read and understand the information in this section prior to installation because the memory configuration and power regulator complement at each computer site can vary with customer needs. If there is any doubt about the original status of the PDP 11/45, contact DEC Field Service personnel prior to installing the Memory Buffer. The illustrations and instructions in this section provide information for all installation steps which include:

- Initial Inspection
- Preparation for Installation
- Power Regulator Installation
- Memory Buffer Module Installation
- Final Adjustment and Test Procedures

INITIAL INSPECTION

Initial inspection includes unpacking, inventory, and inspection of all essential assemblies of the Memory Buffer. After removing the packing material, inventory all items with the list below. Inspect for shipping damage. Report all discrepancies to the Computer Systems Division of FABRI-TEK INCORPORATED. Before preparing for the installation of the Memory Buffer, verify that all of the following items are available:

1. Buffer Matrix Controller (BMC) module – FTI Part No. 190-1665-00.
2. Buffer Memory Matrix (BMM) module – FTI Part No. 190-1666-00.
3. Auxiliary Buffer Matrix Controller (ABMC) module – FTI Part No. 190-1767-00.
4. Buffer Cable Assembly – FTI Part No. 262-0317-00.
5. FTI Model 1744 Power Regulator – FTI Part No. 261-0124-00.

PREPARATION FOR INSTALLATION

Preparation for installation consists of identifying the existing DEC semiconductor memory configuration, selecting the correct FTI Memory Buffer configuration, and preparing the CPU with the aid of a preparation flowchart. Computer preparation is necessary before the actual installation of the Model 4511 Memory Buffer because:

—each PDP 11/45 computer contains one of several semiconductor memory configurations and accompanying power regulator arrangements.

—the Memory Buffer requires the use of CPU slots 21 through 27 (slots 23 through 25 are left empty).

—The +5-volt power sources for CPU slots 21 through 25 must be installed properly.

The extent of CPU preparation depends on the type of installation and can include memory module reconfiguration, power cabling modification, and power regulator installation; in some installations only one of these preparation steps is necessary.

WARNING

To prevent accidental shocks, power down the Model 11/45, de-energize any external d-c voltage inputs to the Model 11/45, and disconnect the main power cable from the line source BEFORE performing the following modification and installation procedures.

EXISTING DEC SEMICONDUCTOR MEMORY CONFIGURATIONS

All PDP 11/45 computers have Fastbus slots 16 through 25 populated in one of the configurations listed in Table 2-1. Verify the DEC memory configuration before selecting the Memory Buffer configuration.

Table 2-1.—POSSIBLE PDP 11/45 SEMICONDUCTOR MEMORY CONFIGURATIONS

CONFIG. NO.	MEMORY TYPE	SLOTS 16-20	SLOTS 21-25	TOTAL
1	None	Empty	Empty	———
2	MOS	4 k-16 k	4 k-16 k	32 k Max.
3	MOS	4 k-16 k		20 k Max.
	BIP		1 k-4 k	
4	BIP	1 k-4 k	1 k-4 k	8 k Max.

FTI MEMORY BUFFER CONFIGURATIONS

Installation of the FTI 4511 Memory Buffer results in the combination of DEC semiconductor memory and the Memory Buffer into one of the configurations listed in Table 2-2.

Table 2-2.–POSSIBLE DEC SEMICONDUCTOR MEMORY AND FTI MEMORY BUFFER CONFIGURATIONS

CONFIG. NO.	MEMORY TYPE	SLOTS 16-20	SLOTS 21-27	TOTAL
1	None	Empty	BUFFER	-----
2	MOS	4 k-16 k	BUFFER	16 k Max.
3	BIP	1 k-4 k	BUFFER	4 k Max.

CPU PREPARATION FLOWCHART

The CPU preparation procedure is illustrated by the CPU Preparation Flowchart, Figure 2-1. Use the flowchart by referencing the following explanation of the flowchart procedure steps to prepare the CPU for installation of the Memory Buffer.

Step No. 1 – Is any Fastbus semiconductor memory present (in CPU slots 16 through 25)?
NO – Branch to (C).
YES – Proceed to Step No. 2.

Step No. 2 – Are CPU slots 21 through 25 empty?
NO — Remove the modules from these slots and reconfigure MOS or BIP memory into slots 16 through 20 per Table 2-2. Reference the DEC PDP 11/45 Maintenance Manual for detailed MOS and BIP reconfiguration instructions.
YES – Proceed to Step No. 3.

Step No. 3 – Is +5 volts present at CPU slots 21 through 23?
NO – This implies that either the jumper between J5 pins 3 and 4 is disconnected, or that a fault exists at the power source. Proceed to Step No. 4.
YES – Branch to (B).

Step No. 4 – Is the jumper between J5 pins 3 and 4 disconnected?
NO – Consult DEC Field Service.
YES – Proceed to Step No. 5.

Step No. 5 – Is a DEC H744 +5-V Regulator installed in slot K of the lower H742 Power Supply?
NO – Branch to (C).
YES – Consult DEC Field Service.

POWER REGULATOR INSTALLATION

Installation of the FTI Model 1744 Power Regulator includes mounting the power regulator in the DEC H742 Power Supply chassis, CPU backplane power modification, and an initial power regulator adjustment check. Figure 2-2 illustrates the location of the 1744 Power Regulator when it is installed.

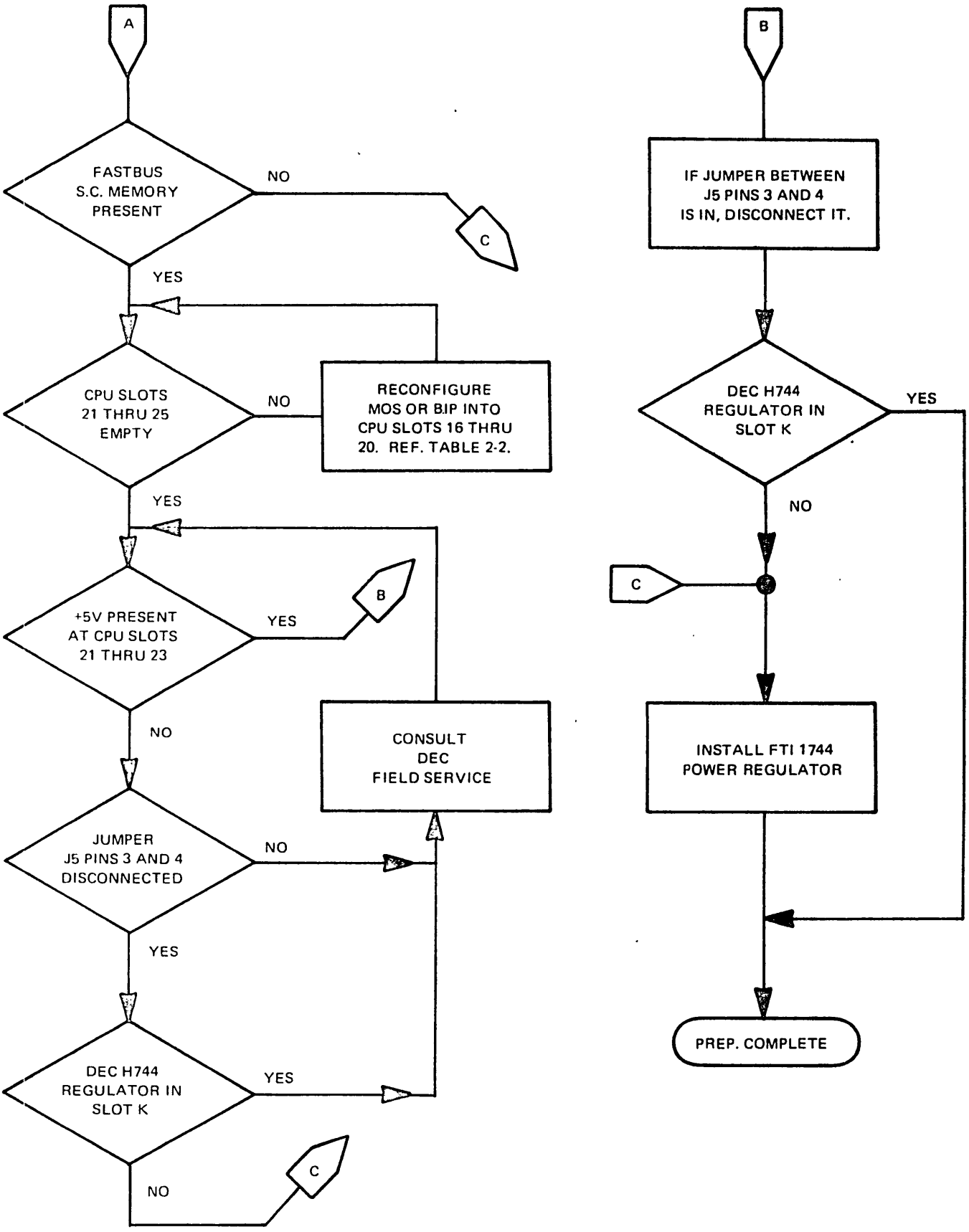


Figure 2-1
CPU PREPARATION FLOWCHART

UPPER H742 POWER SUPPLY (SWITCHED)

E	D	C	B	A	BULK SUPPLY A REGULATORS
+15V CPU -15V TO 1, 2, 15	+5V INTERNAL OPTIONS				A, B, C, D, E SWITCHED +15V TO REGS E,F
INTERNAL OPTIONS -15V TO SLOTS 26, 27, 28 CONSOLE	+5V TO SLOTS 26, 27, 28 SYSTEM UNITS	+5V CPU	+5V CPU	+5V FLOATING POINT	+15V TO SLOT 13 CONSOLE +8V TO SLOT 1 FOR MAINT MODULES
SYSTEM UNITS -15V TO SYSTEM UNITS NOS. 1, 2	+5V TO SYSTEM UNITS NOS. 1, 2, 3	+5V TO SLOTS 10 THRU 15	+5V TO SLOTS 1, 6, 7, 8, 9	+5V TO SLOTS 2, 3, 4, 5	50/60 Hz SIG 0 TO +5V TO SLOT 1 FOR CLOCK MODULE

LOWER H742 POWER SUPPLY (NOT SWITCHED)

L	K	J	H*	F	
+5V BIPOLAR MEMORY +5V TO SLOTS 24, 25	+5V BIPOLAR MEMORY +5V TO SLOTS 21, 22, 23	+5V IF BIPOLAR MEMORY IS INSTALLED +5V TO SLOTS 19, 20 H744 P27	+5V IF BIPOLAR MEMORY IS INSTALLED +5V TO SLOTS 16, 17, 18 H744 P31	-15V SYSTEM UNITS -15V TO SYSTEM UNIT NO. 3	BULK SUPPLY B REGULATORS F, H, J, K, L NOT SWITCHED
		+5V IF MOS MEMORY IS INSTALLED +5V TO SLOTS 16 THRU 25	+19V, +23V, -5V IF MOS MEMORY IS INSTALLED		
H744 P29	FTI MODEL 1744 POWER REGULATOR P28	H744 P27	H746 P26	H745 P25	
J29	J28	J27	J26/J31	J25	

*Regulator in location H will be either a +5V or MOS Voltage Regulator.

Figure 2-2
FTI MODEL 1744 POWER REGULATOR LOCATION

POWER REGULATOR INSTALLATION PROCEDURE

Use the following installation procedure to mount the 1744 Power Regulator in the DEC H742 Power Supply chassis:

1. Remove the screw which mounts the P28 connector to the H742 Power Supply chassis.

2. Slide the FTI Model 1744 Power Regulator into slot K of the lower H742 Power Supply chassis. In this slot, the female connector on the 1744 Power Regulator is identified as J28.

3. Install the two screws which fasten the 1744 Power Regulator to the H742 Power Supply.

4. Connect P28 to J28 at the 1744 Power Regulator.

CPU BACKPLANE POWER MODIFICATION

Installation of a power regulator in the lower H742 Power Supply makes it necessary to modify the CPU backplane power cabling as follows: reference Figure 2-3 and locate the jumper wire between J5 pins 3 and 4, remove one end of the jumper wire, wrap the disconnected end with insulating tape, as as an alternate approach either cut the jumper wire or remove it entirely.

INITIAL POWER REGULATOR ADJUSTMENT CHECK

The Initial Power Regulator Adjustment Check is necessary only when an FTI or DEC Power Regulator is connected at slot K of the lower H742 Power Supply. Prior to installing the Memory Buffer modules, perform the procedure below to adjust the Power Regulator output voltage. Each regulator in the lower H742 Power Supply has a voltage adjustment potentiometer on the front of the Power Regulator case. Final voltage adjustments will be made with all the Memory Buffer modules inserted during the final adjustment and test procedures in this section.

1. If the jumper wire between J5 pins 3 and 4 is installed, remove all printed circuit modules from CPU slots 16 through 25. If the jumper wire is disconnected, remove all printed circuit modules from CPU slots 21 through 25.

2. Connect a VOM between CPU location A21A2 and A21C2 (ground). Figure 2-3 illustrates the location of these test points.

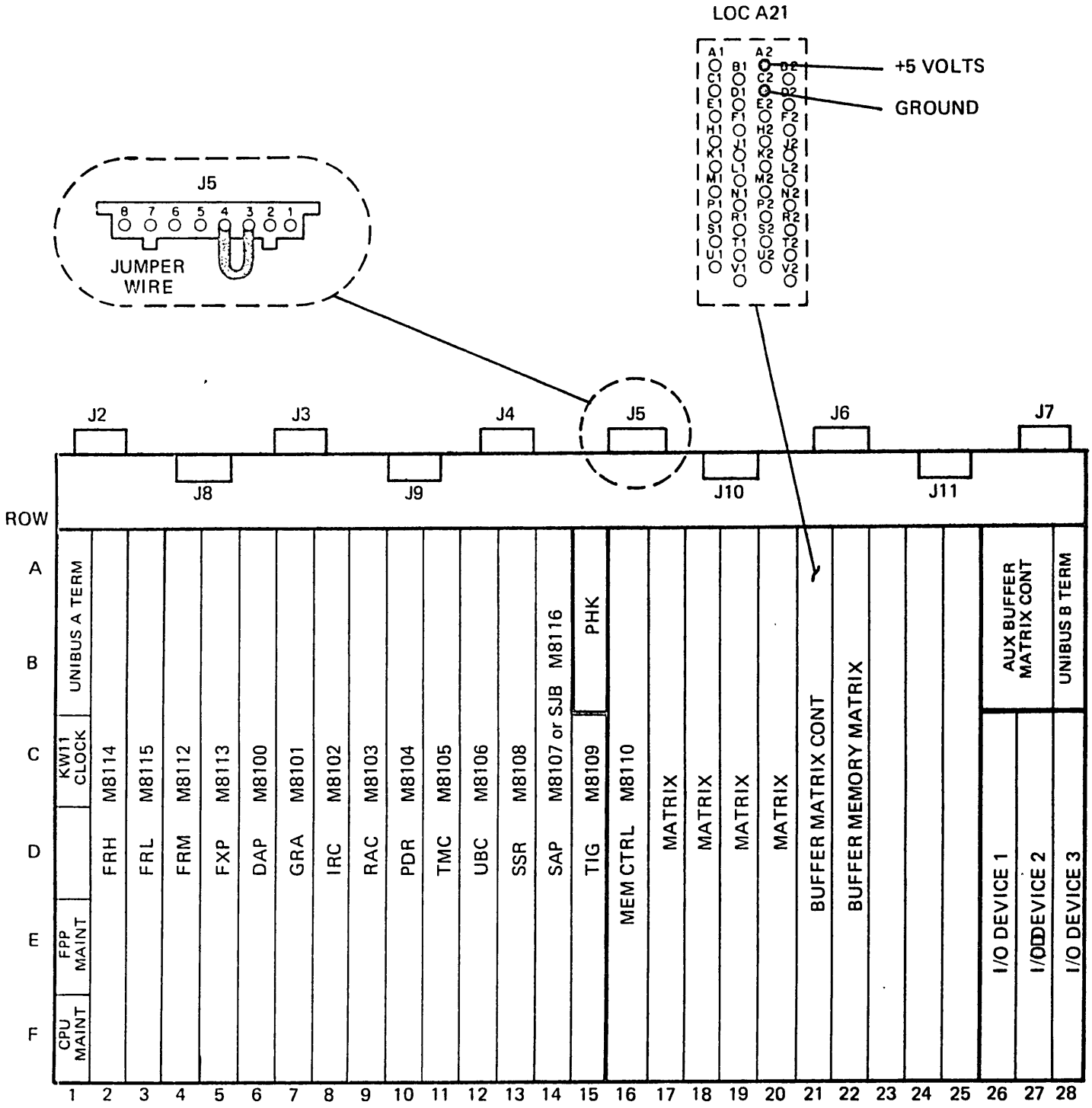


Figure 2-3
CPU BACKPLANE
J5 JUMPER WIRE AND +5 VOLT TEST POINTS

3. Toggle the Power Supply circuit breakers to ON.

4. Check for a voltage reading of +5.2 V dc. Rotating the voltage adjustment potentiometer in a clockwise direction at the appropriate power regulator increases the output voltage.

5. Toggle the Power Supply circuit breakers to OFF.

6. Re-install the printed circuit modules into their correct CPU slots.

EXISTING MEMORY VERIFICATION TEST

Perform the DEC 0-124 k Memory Exerciser Diagnostic Test prior to installing the Memory Buffer modules. This test will verify the operation of the existing MOS, bipolar, and core memory. If a fault occurs, locate and correct any malfunctions until memory operation is error-free.

MEMORY BUFFER MODULE INSTALLATION

Figures 2-4 and 2-5 illustrate the location of the Memory Buffer modules in the CPU. Slide each module into its correct location and lock the module into the back panel connectors by pressing the locking levers at the edge of each module. Install the modules as follows:

– Slide the Buffer Matrix Controller module into CPU slot 21.

NOTE

The Buffer Matrix Controller module is jumper-programmed at the factory to buffer a 0-124 k address range. It is not necessary to alter this setting. Option: if desired, the maximum address range may be changed at this time by referencing Table 2-3, Figure 2-6, and the final adjustment and test procedures in this section. Do not set the jumpers to include the I/O address space (125 k - 128 k).

– Slide the Buffer Memory Matrix module into CPU slot 22.

– Slide the Auxiliary Buffer Matrix Controller module into CPU slots 26 and 27. This module replaces the DEC M9200 module.

– Connect the Buffer Cable Assembly, FTI Part No. 262-0317-00, between the Auxiliary Buffer Matrix Controller module and the female connector J1 at the Buffer Matrix Controller module. This completes the installation of the Memory Buffer modules.

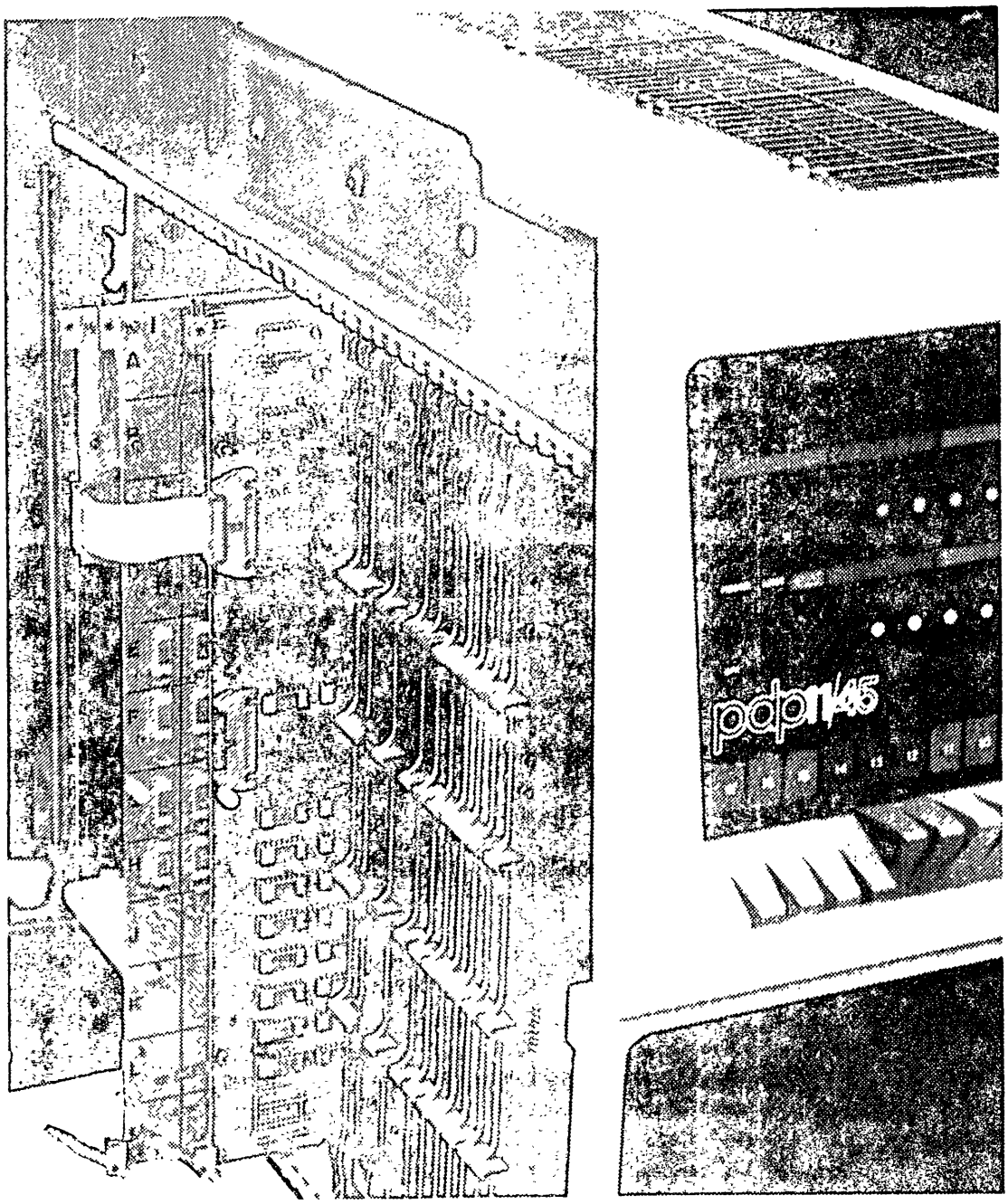


Figure 2-4
MEMORY BUFFER MODULE INSTALLATION (SIDE VIEW)

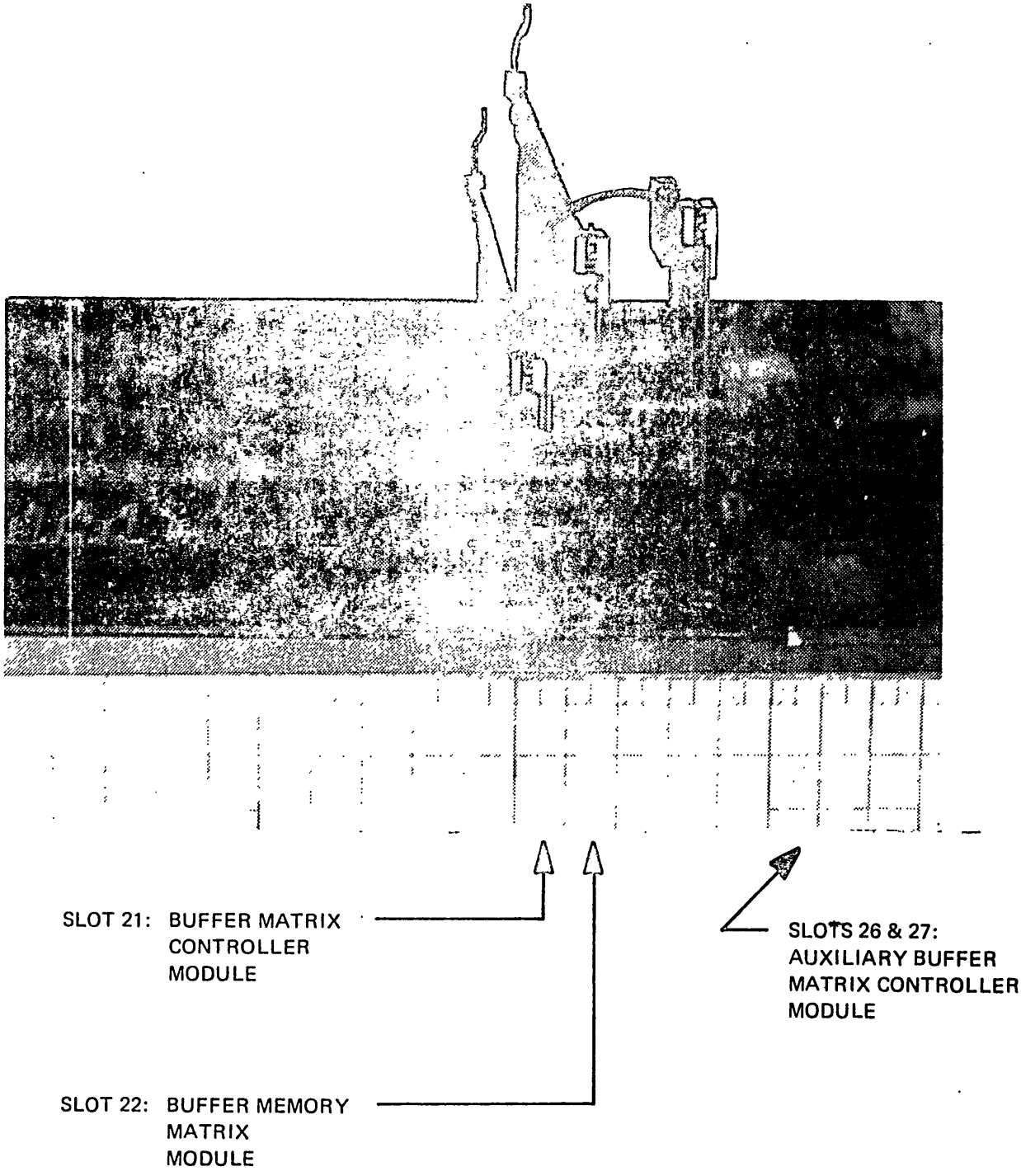


Figure 2-5
MEMORY BUFFER MODULE INSTALLATION (MUL STRIP TOP VIEW)

Table 2-3.–MAXIMUM ADDRESS JUMPER CONFIGURATIONS

	DECIMAL ADDRESS WORDS NOTE 1	OCTAL ADDRESS BYTES NOTE 2	JUMPER POSITION 17	16	15	14	13	12	11	DECIMAL ADDRESS WORDS NOTE 1	OCTAL ADDRESS BYTES NOTE 2	JUMPER POSITION 17	16	15	14	13	12	11
I/O ADDRESS SPACE NOTE 3	127K	774K	–	–	–	–	–	–	–	95K	574K	–	J	–	–	–	–	–
	126K	770K	–	–	–	–	–	–	J	94K	570K	–	J	–	–	–	–	J
	125K	764K	–	–	–	–	–	J	–	93K	564K	–	J	–	–	–	J	–
	124K	760K	–	–	–	–	–	J	J	92K	560K	–	J	–	–	–	J	J
	123K	754K	–	–	–	–	J	–	–	91K	554K	–	J	–	–	J	–	–
	122K	750K	–	–	–	–	J	–	J	90K	550K	–	J	–	–	J	–	J
	121K	744K	–	–	–	–	J	J	–	89K	544K	–	J	–	–	J	J	–
	120K	740K	–	–	–	–	J	J	J	88K	540K	–	J	–	–	J	J	J
	119K	734K	–	–	–	J	–	–	–	87K	534K	–	J	–	J	–	–	–
	118K	730K	–	–	–	J	–	–	J	86K	530K	–	J	–	J	–	–	J
	117K	724K	–	–	–	J	–	J	–	85K	524K	–	J	–	J	–	J	–
	116K	720K	–	–	–	J	–	J	J	84K	520K	–	J	–	J	–	J	J
	115K	714K	–	–	–	J	J	–	–	83K	514K	–	J	–	J	J	–	–
	114K	710K	–	–	–	J	J	–	J	82K	510K	–	J	–	J	J	–	J
	113K	704K	–	–	–	J	J	J	–	81K	504K	–	J	–	J	J	J	–
	112K	700K	–	–	–	J	J	J	J	80K	500K	–	J	–	J	J	J	J
	111K	674K	–	–	J	–	–	–	–	79K	474K	–	J	J	–	–	–	–
	110K	670K	–	–	J	–	–	–	J	78K	470K	–	J	J	–	–	–	J
	109K	664K	–	–	J	–	–	J	–	77K	464K	–	J	J	–	–	J	–
	108K	660K	–	–	J	–	–	J	J	76K	460K	–	J	J	–	–	J	J
	107K	654K	–	–	J	–	J	–	–	75K	454K	–	J	J	–	J	–	–
	106K	650K	–	–	J	–	J	–	J	74K	450K	–	J	J	–	J	–	J
	105K	644K	–	–	J	–	J	J	–	73K	444K	–	J	J	–	J	J	–
	104K	640K	–	–	J	–	J	J	J	72K	440K	–	J	J	–	J	J	J
	103K	634K	–	–	J	J	–	–	–	71K	434K	–	J	J	J	–	–	–
	102K	630K	–	–	J	J	–	–	J	70K	430K	–	J	J	J	–	–	J
	101K	624K	–	–	J	J	–	J	–	69K	424K	–	J	J	J	–	J	–
	100K	620K	–	–	J	J	–	J	J	68K	420K	–	J	J	J	–	J	J
	99K	614K	–	–	J	J	J	–	–	67K	414K	–	J	J	J	J	–	–
	98K	610K	–	–	J	J	J	–	J	66K	410K	–	J	J	J	J	–	J
	97K	604K	–	–	J	J	J	J	–	65K	404K	–	J	J	J	J	J	–
	96K	600K	–	–	J	J	J	J	J	64K	400K	–	J	J	J	J	J	J

DECIMAL ADDRESS WORDS NOTE 1	OCTAL ADDRESS BYTES NOTE 2	JUMPER POSITION 17	16	15	14	13	12	11	DECIMAL ADDRESS WORDS NOTE 1	OCTAL ADDRESS BYTES NOTE 2	JUMPER POSITION 17	16	15	14	13	12	11
63K	374K	J	–	–	–	–	–	–	31K	174K	J	J	–	–	–	–	–
62K	370K	J	–	–	–	–	–	J	30K	170K	J	J	–	–	–	–	J
61K	364K	J	–	–	–	–	J	–	29K	164K	J	J	–	–	–	J	–
60K	360K	J	–	–	–	–	J	J	28K	160K	J	J	–	–	–	J	J
59K	354K	J	–	–	–	J	–	–	27K	154K	J	J	–	–	J	–	–
58K	350K	J	–	–	–	J	–	J	26K	150K	J	J	–	–	J	–	J
57K	344K	J	–	–	–	J	J	–	25K	144K	J	J	–	–	J	J	–
56K	240K	J	–	–	–	J	J	J	24K	140K	J	J	–	–	J	J	J
55K	334K	J	–	–	J	–	–	–	23K	134K	J	J	–	J	–	–	–
54K	330K	J	–	–	J	–	–	J	22K	130K	J	J	–	J	–	–	J
53K	324K	J	–	–	J	–	J	–	21K	124K	J	J	–	J	–	J	–
52K	320K	J	–	–	J	–	J	J	20K	120K	J	J	–	J	–	J	J
51K	314K	J	–	–	J	J	–	–	19K	114K	J	J	–	J	J	–	–
50K	310K	J	–	–	J	J	–	J	18K	110K	J	J	–	J	J	–	J
49K	304K	J	–	–	J	J	J	–	17K	104K	J	J	–	J	J	J	–
48K	300K	J	–	–	J	J	J	J	16K	100K	J	J	–	J	J	J	J
47K	274K	J	–	J	–	–	–	–	15K	74K	J	J	J	–	–	–	–
46K	270K	J	–	J	–	–	–	J	14K	70K	J	J	J	–	–	–	J
45K	264K	J	–	J	–	–	J	–	13K	64K	J	J	J	–	–	J	–
44K	260K	J	–	J	–	–	J	J	12K	60K	J	J	J	–	–	J	J
43K	254K	J	–	J	–	J	–	–	11K	54K	J	J	J	–	J	–	–
42K	250K	J	–	J	–	J	–	J	10K	50K	J	J	J	–	J	–	J
41K	244K	J	–	J	–	J	J	–	9K	44K	J	J	J	–	J	J	–
40K	240K	J	–	J	–	J	J	J	8K	40K	J	J	J	–	J	J	J
39K	234K	J	–	J	J	–	–	–	7K	34K	J	J	J	J	–	–	–
38K	230K	J	–	J	J	–	–	J	6K	30K	J	J	J	J	–	–	J
37K	224K	J	–	J	J	–	J	–	5K	24K	J	J	J	J	–	J	–
36K	220K	J	–	J	J	–	J	J	4K	20K	J	J	J	J	–	J	J
35K	214K	J	–	J	J	J	–	–	3K	14K	J	J	J	J	J	–	–
34K	210K	J	–	J	J	J	–	J	2K	10K	J	J	J	J	J	–	J
33K	204K	J	–	J	J	J	J	–	1K	4K	J	J	J	J	J	J	–
32K	200K	J	–	J	J	J	J	J	0K	0K	J	J	J	J	J	J	J

Note 1: In Decimal Word Address, K = 1024_{10}

Note 2: In Octal Byte Address, K = 1000_8

Note 3: Do not set jumpers to include I/O Address space.

A "J" in the Jumper Position column indicates the presence of a jumper, which is equivalent to a logic Zero. Any jumper configuration defines the first address to be excluded from the Buffer. For example: to set in a maximum address of 124 K_{10} install jumpers in the slots for bits 11 and 12 only.

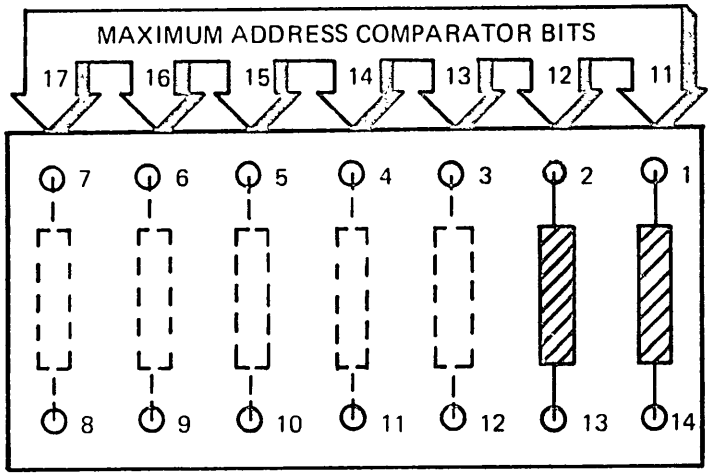
FINAL ADJUSTMENT AND TEST PROCEDURES

Final adjustment includes defining the maximum address capability of the Buffer, measuring the Power Regulator output voltages with the Memory Buffer installed, and setting the Buffer card edge switches to the correct position. A Manual Operation Test and diagnostic testing confirm error-free operation.

MAXIMUM ADDRESS JUMPER SELECTION

The configuration of the jumpers on the Buffer Matrix Controller module determines the maximum address space that the Buffer will map into itself. Reference Table 2-3 to determine the proper jumper configuration for the desired address space. Figure 2-6 illustrates the physical location of the Maximum Address Jumpers.

The factory setting defines the maximum address space that the Buffer will buffer to be 0-124 k words, which will allow proper operation with any PDP 11/45 memory. Note that this means that the I/O address space 125 k-128 k words is not buffered. These jumpers should not be set higher than 124 k, but could for some special reason, be set to a lower address space. The address space always starts at 0, with the portion being occupied by DEC semiconductor memory automatically excluded from buffering.



LOCATION T5 OF BUFFER MATRIX CONTROLLER MODULE

NOTE: The location of the shaded jumpers illustrated above, for bits 11 and 12, is the factory setting for 0-124 k. This setting is suitable for any size main memory up to 124 k, and normally will not need changing.

Figure 2-6
MAXIMUM ADDRESS JUMPERS

FINAL POWER SUPPLY OUTPUT ADJUSTMENT

With all Memory Buffer modules installed in their correct locations, adjust the output voltage of the +5-V d-c Power Regulator in slot K of the lower H742 Power Supply to +5.0 ± 0.1 volts while measuring at the backpanel. Because of the memory reconfiguration, checking the output voltage of the +5-V regulators for CPU slots 16 through 20 is recommended. Readjust, if necessary, to +5.0 ± 0.1 volt.

CARD EDGE SWITCH SETTINGS

The Buffer Matrix Controller Module contains three card-edge test switches. Figure 2-7 illustrates the position of the switches and describes their functions. In normal operation, all switch handles must be in the UP position.

Initialization switch H1S1 is a momentary contact switch used only for troubleshooting. Toggling the switch to the INIT position initializes the Memory Buffer.

Line switch J1S1 is a two-position toggle switch. Toggling the switch to the ON position places the Memory Buffer in the On-Line condition and disables the Copy switch K1S1. Toggling the switch to the OFF position places the Memory Buffer in the Off-Line condition, prevents the Memory Buffer from responding on the Fastbus, and enables the Copy switch K1S1.

Copy switch K1S1 is a two-position toggle switch used only for troubleshooting. This switch is enabled only when the Line switch J1S1 is in the OFF position. Toggling the Copy switch to the ON position allows the Memory Buffer to update itself. Toggling the Copy switch to the OFF position prevents updating of the Memory Buffer.

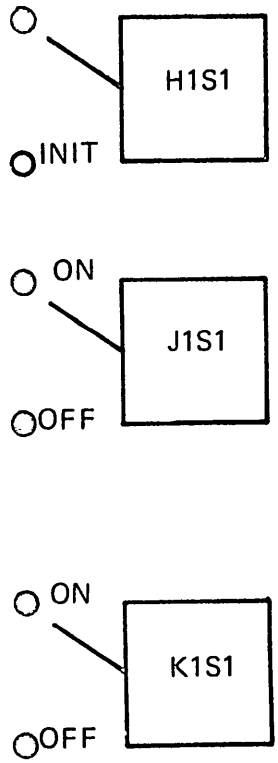


Figure 2-7
CARD-EDGE SWITCHES

MANUAL OPERATION TEST

The Manual Operation Test verifies the operation of the Memory Buffer, without the use of a scope or program, prior to diagnostic testing. When the Memory Buffer is completely installed in the PDP 11/45, perform the Manual Operation Test by using the Buffer Matrix Controller card-edge switches illustrated in Figure 2-7 and the CPU front panel switches and indicators as follows:

1. Halt the CPU.
2. Toggle H1S1 to INIT.
3. Toggle J1S1 to ON.
4. Toggle K1S1 to OFF.
5. Select an address.
6. Load all zeros into the selected address.
7. Examine the contents of the selected address. The contents should be all zeros. The Memory Buffer now contains the same address and data. The CPU front panel is displaying the data from the Unibus (core memory).
8. Press the Examine switch again. The contents of the selected address should be all zeros again. The CPU front panel is displaying the data from the Fastbus (Memory Buffer).
9. Toggle J1S1 and K1S1 to OFF.
10. Load all ones into the same selected address.
11. Examine the contents of the selected address. The CPU front panel should display all ones.
12. Toggle J1S1 to ON.
13. Press the Examine switch again. The CPU front panel should display all zeros to indicate correct Memory Buffer operation.

NOTE

Whenever the data in the Memory Buffer differs from the data in the same address in core memory, it is necessary to Initialize the Memory Buffer before restarting the CPU with the Memory Buffer On-line. This operation prevents the use of invalid data.

DIAGNOSTIC TESTS

The diagnostic tests are the final steps necessary to verify correct operation of the Memory Buffer in the PDP 11/45. Perform the DEC 0-124 k Memory Exerciser Diagnostic. In case of a fault, recheck the installation instructions in this section.

SECTION III
PRINCIPLES OF OPERATION

INTRODUCTION

This section describes the operating theory and basic functions of the FTI Model 4511 Memory Buffer. The text describes the integration of the Memory Buffer into the PDP 11/45, Memory Buffer functions, principles and types of Buffer operation, and interface signal requirements. A system block diagram illustrates the integration of the 4511 Memory Buffer with the Fastbus/Unibus structure of the PDP 11/45. A Memory Buffer block diagram illustrates the interrelationship of each of the major sections of the Memory Buffer. Additional tables and illustrations support the description of Buffer operations and the discussion of Interface, Internal and Control circuits.

INTEGRATION OF THE MEMORY BUFFER INTO THE PDP 11/45

Installation of the Memory Buffer modules unites the FTI 4511 with the Fastbus/Unibus structure of the PDP 11/45. The Memory Buffer is a two-port device consisting of a Fastbus port and a Unibus port. Figure 3-1 illustrates the integration of the FTI 4511 with the PDP 11/45. Note by the direction of the arrows that the Memory Buffer Unibus port is unidirectional since it is capable of only receiving the Unibus address, data, and control signals. The Memory Buffer Fastbus port only receives the address signals from the Memory Management Unit, only transmits the data signals to the semiconductor memory and CPU, but transmits and receives the control signals between the semiconductor memory and CPU.

MEMORY BUFFER FUNCTIONS

Figure 3-2 illustrates the signal flow and organization of the Model 4511 Memory Buffer. It consists of the following major sections:

- Control Logic
- Valid Bit Register
- Directory (Register)
- Buffer Memory Matrix (Register)
- Match Circuit
- Initialization Circuit

CONTROL LOGIC

The Control Logic section provides interfacing for:

– Receiving and transmitting Unibus and Fastbus Control signals.
– Generating Internal Timing signals.

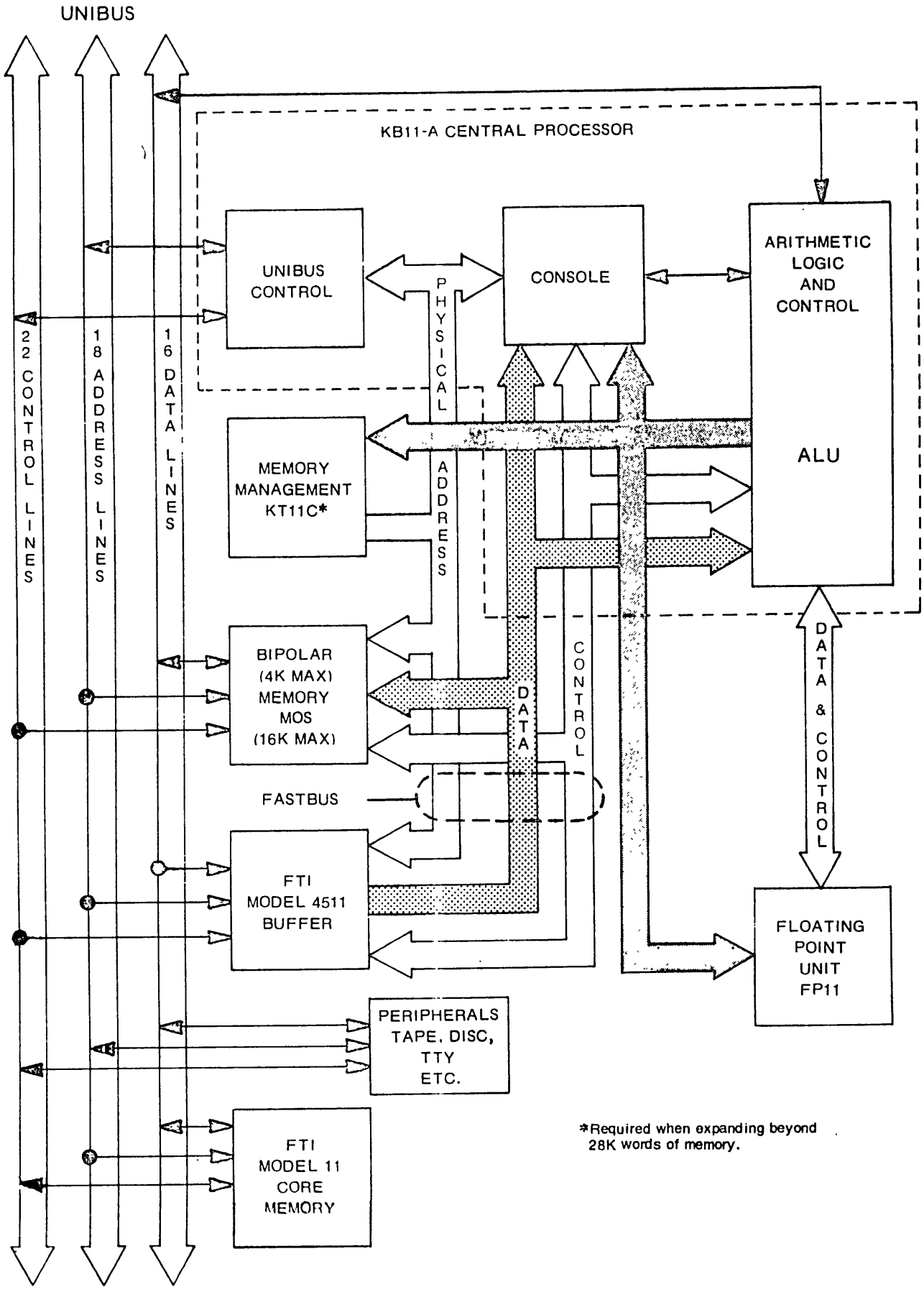


Figure 3-1

FABRI-TEK MODEL 4511 MEMORY BUFFER WITH THE PDP 11/45 COMPUTER

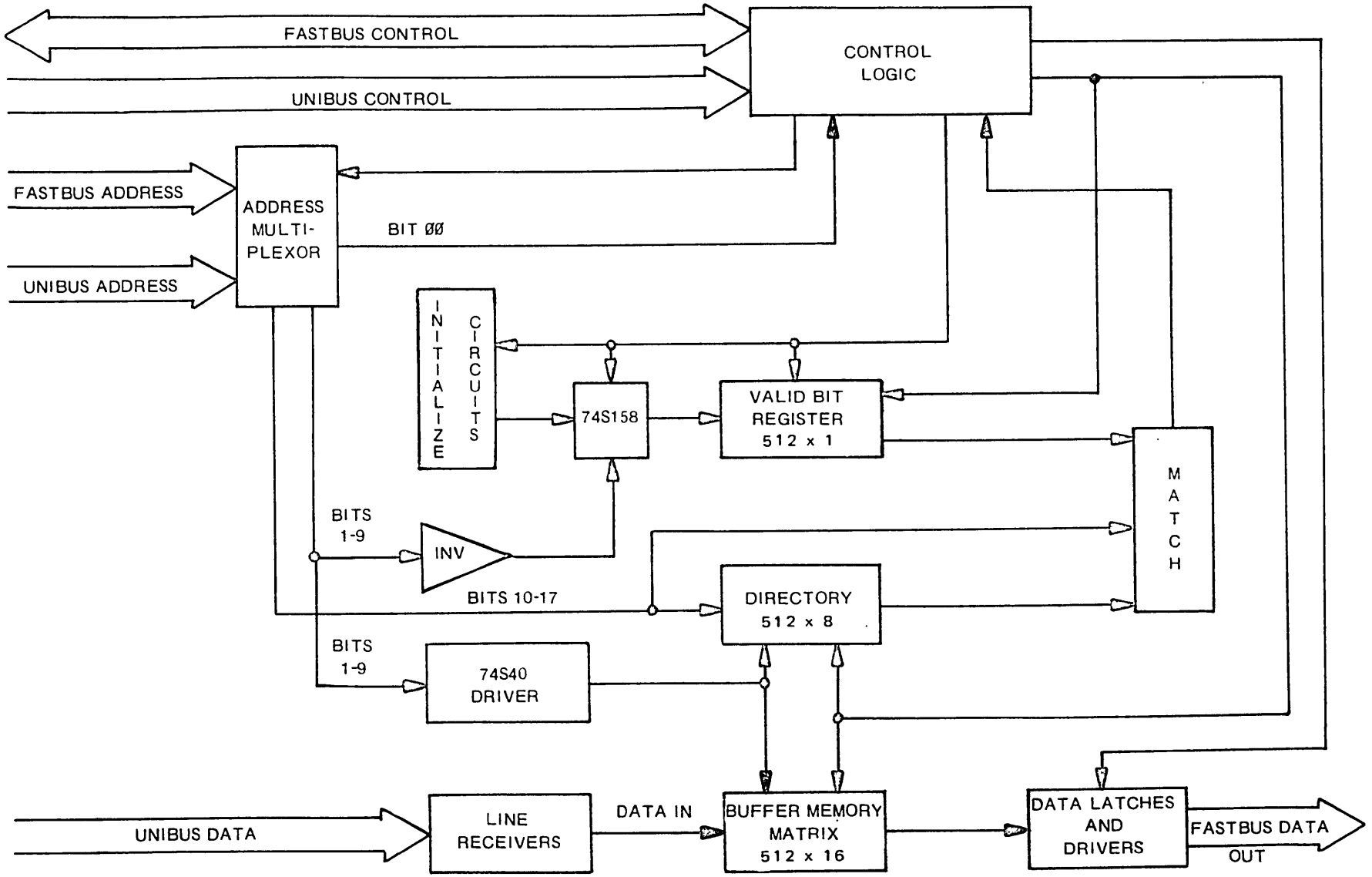


Figure 3-2
FTI MODEL 4511 MEMORY BUFFER BLOCK DIAGRAM

– Generating External Control signals.
– Write Control.
– Maximum Address.
– DMA Cycles.

VALID BIT REGISTER

The Valid Bit Register is a 512 x 1 register containing a flag bit for each address in the Directory. The purpose of this register is for initialization; so that on start-up, e.g., when power is first applied and the contents of the Directory are random values, a coincidental address match will not cause a Buffer response to a CPU request. On start-up, the Initialization circuitry causes all the addresses in the Directory to be flagged as Invalid. When a word is loaded into the Buffer Memory Matrix, and the upper half (address bits <17:10>) of the address is loaded into the Directory, the corresponding one-bit word in the Valid Bit Register is set high (Valid). Bus address bits 1 through 9 are decoded to specify one of 512 locations in this register.

DIRECTORY

The Directory is a 512 x 8 matrix of Bipolar Random Access Memories (RAMs) organized as a Content Address Memory (CAM). The Directory is decoded by address bits 1 through 9. The number of bits per Directory word (eight) plus the number of bits required to address any word in the Directory (nine) equals the number of bits required (17) to address any of the 131,072 (128 k) words in the PDP 11/45 address space. The eighteenth bit, 2^0, is used for byte control. This addressing format allows the Memory Buffer to use a Direct Mapping Scheme to buffer any address within the 128 k word address space of the PDP 11/45. The address space of the PDP 11/45 may be less than 128 k if the setting of the maximum address jumpers defines a lower address range for the maximum address comparator in the Control Logic section. Refer to Table 2-3 and Figure 2-6.

BUFFER MEMORY MATRIX

The Buffer Memory Matrix is a 512 x 16 matrix of high-speed bipolar RAMs which store a word of data. These data, by using a Write-Through Algorithm, are always a current copy of the data stored in the corresponding addresses in core memory.

MATCH CIRCUIT

The Match circuit uses eight exclusive/NOR gates to compare the contents of the Directory with the corresponding incoming address bits <17:10>. This process is conditioned by the corresponding Valid Bit Register flag to determine if valid data for the specified address are in the Buffer Memory Matrix.

INITIALIZATION CIRCUIT

The Initialization Circuit consists of four one-shot generators connected together as an oscillator and three counters connected together as a 9-bit address generator. The oscillator circuit generates a pulse train which cycles through all 512 addresses in the Valid Bit Register to write a zero into each address. Writing zeros into each address of the Valid Bit Register invalidates the contents of the entire Buffer Memory Matrix and Directory. This process occurs upon the removal (switching to a high logic level) of either the BUSA INIT L signal or the PWRS MEM DC L signal.

PRINCIPLES OF BUFFER OPERATION

The 4511 Memory Buffer is a communication link between the CPU and memory. The Memory Buffer increases the effective speed of the PDP 11/45 core memory by using a Direct Mapping Scheme during Read operations and a Write-Through Algorithm during Write operations.

DIRECT MAPPING SCHEME

The Direct Mapping Scheme is explained with the aid of Figure 3-3. In this figure the term "address space" is defined as the set of all word addresses that can be specified by a given number of address bits. For example, the set of all word addresses in the PDP 11/45 is 131,072, is referred to as the address space of the PDP 11/45, and is represented by the sectioned column at the left in Figure 3-3. Any address in this set can be specified by address bits <17:01>. Similarly, the Buffer address space shown at the right side of Figure 3-3, designed with an address space of 512, is specified by address bits <09:01>.

It is useful to mentally subdivide the PDP 11/45 address space into 256 blocks of memory called Block Numbers. Each of the 256 Block Numbers corresponds to a subset of 512 Block Addresses. The Block Numbers are addressed by address bits <17:10>. The contents of each Block Address are specified by address bits <09:01>.

The Direct Mapping Scheme basically involves a many-to-one correspondence concept. This means that words with the same Block Address but with different Block Numbers will directly map from the PDP 11/45 address space into the corresponding address in the Buffer address space. In other words, old addresses and corresponding data with a given Block Address are simply replaced by a new address and corresponding data having the same Block Address.

WRITE-THROUGH ALGORITHM

The Write-Through Algorithm is implemented by performing all Write operations immediately in core memory and, if the address is in the Buffer, simultaneously updating the corresponding data in the Buffer. Use of the Write-Through Algorithm provides a definite advantage since data are always safe in non-volatile core memory if a-c line power fails.

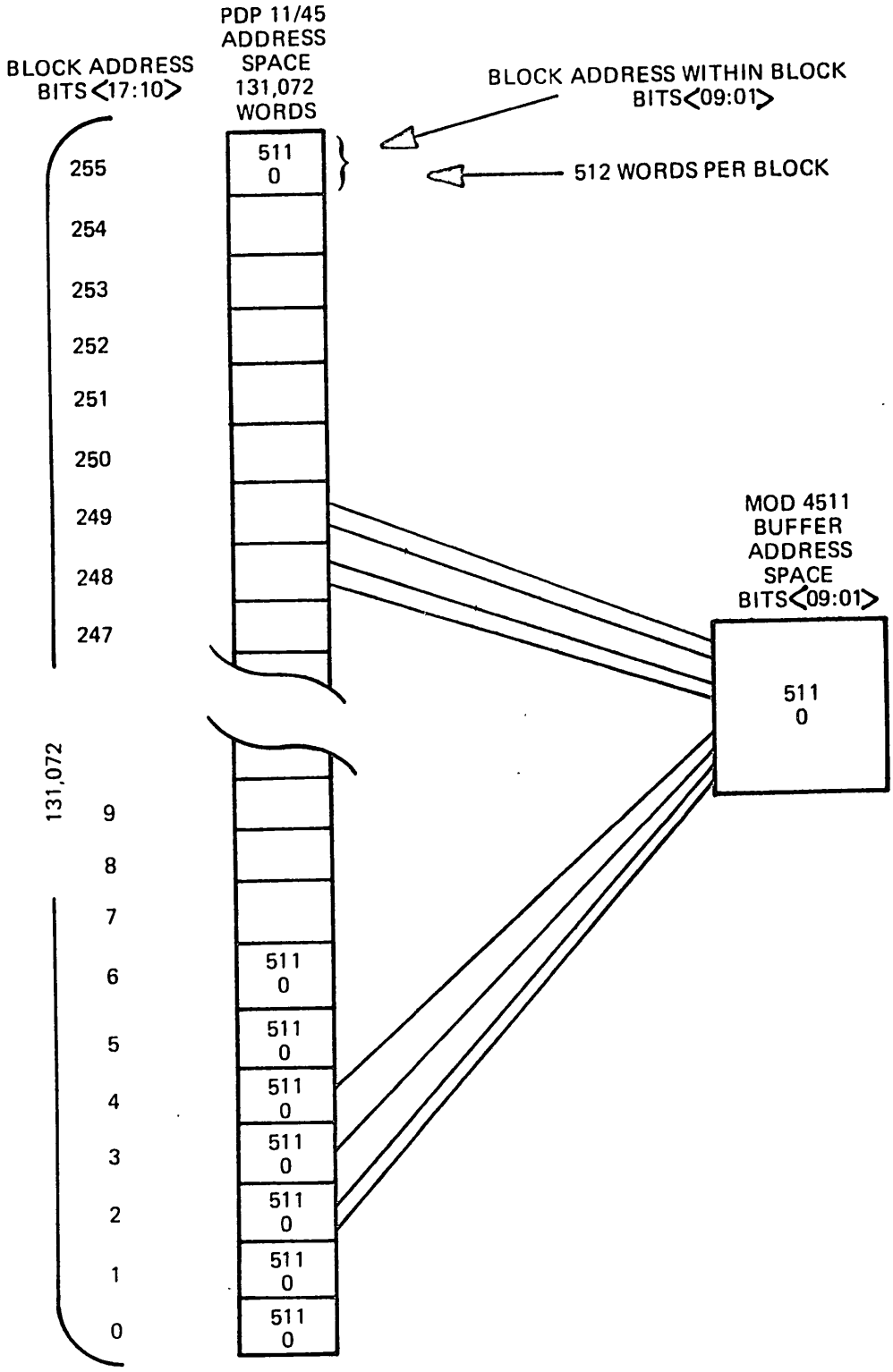


Figure 3-3
DIRECT MAPPING SCHEME

TYPES OF OPERATION

The Memory Buffer has two basic types of operation: DATI-Read, and DATO-Write. Control interface signals on the Fastbus and Unibus determine the selection of the type of operation. Refer to Figures 3-4 and 3-5 in the following discussions.

DATI OPERATION

The Buffer uses the Direct Mapping Algorithm illustrated in Figure 3-4 during DATI operations. During each DATI operation, the CPU logic determines if the specific address on the Fastbus address lines is in the Buffer and waits for approximately 150 nanoseconds before responding with the next instruction. This response indicates whether the desired data are in or out of the Buffer. The probability that an address being fetched will be in the Buffer is called the Hit Ratio.

The Memory Buffer Direct Mapping Algorithm illustrated in Figure 3-4 causes the following sequence of logical events to occur when the desired data are <u>in</u> the Buffer.

- The Buffer searches the Directory for the specific address.
- The Buffer determines that the data at the specific address are in the Buffer and are valid.
- The Buffer responds to the CPU before 150 nanoseconds with a BMC MEM L signal on the Fastbus to inhibit the CPU from performing the DATI cycle on the Unibus.
- The CPU responds with a UBCA CONTROL OK H signal, confirming that the UBCC MEM BUS C0 L and UBCC MEM BUS C1 L control signals are valid. The CPU is now ready to receive the data from the Buffer.
- The Buffer sends the CPU ABMC MEM SYNC (B) L signal, indicating that the data from the Buffer are ready. This signal is the Fastbus version of BUSA SSYNC1 L.
- The CPU drops the UBCA CONTROL OK H signal, indicating that the CPU has the data and has finished its cycle.
- The Buffer drops the BMC MEM SYNC (B) L signal and terminates the Fastbus cycle.

The following sequence of logical events occurs when the desired data are <u>out</u> of the Buffer.

- The Buffer searches the Directory for the specific address.
- The Buffer determines that the data at the specific address are not in the Buffer or are not valid.
- The CPU decides after 150 nanoseconds that it must fetch the desired data from core memory on the Unibus.

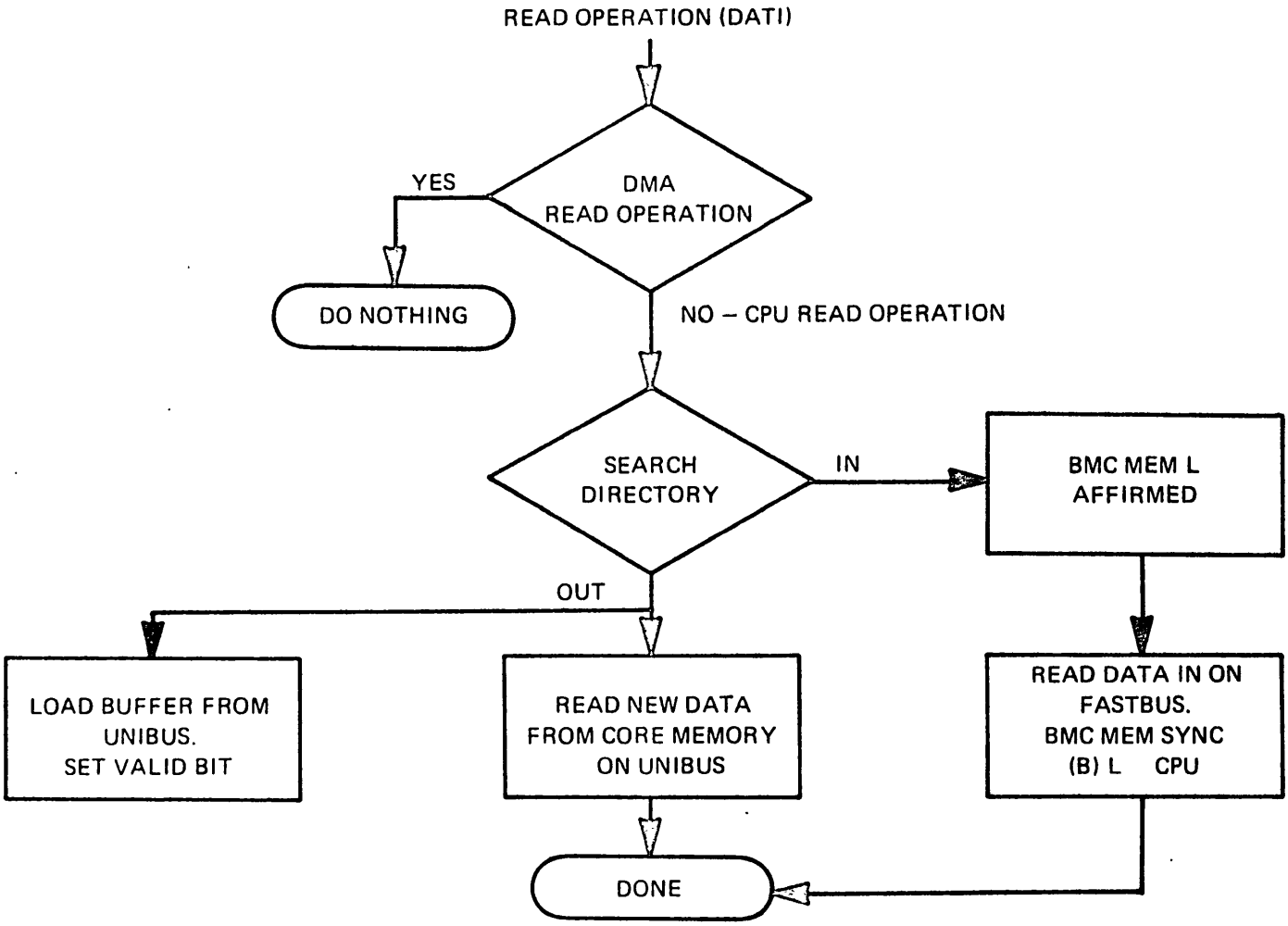


Figure 3-4.–DIRECT MAPPING ALGORITHM (READ)

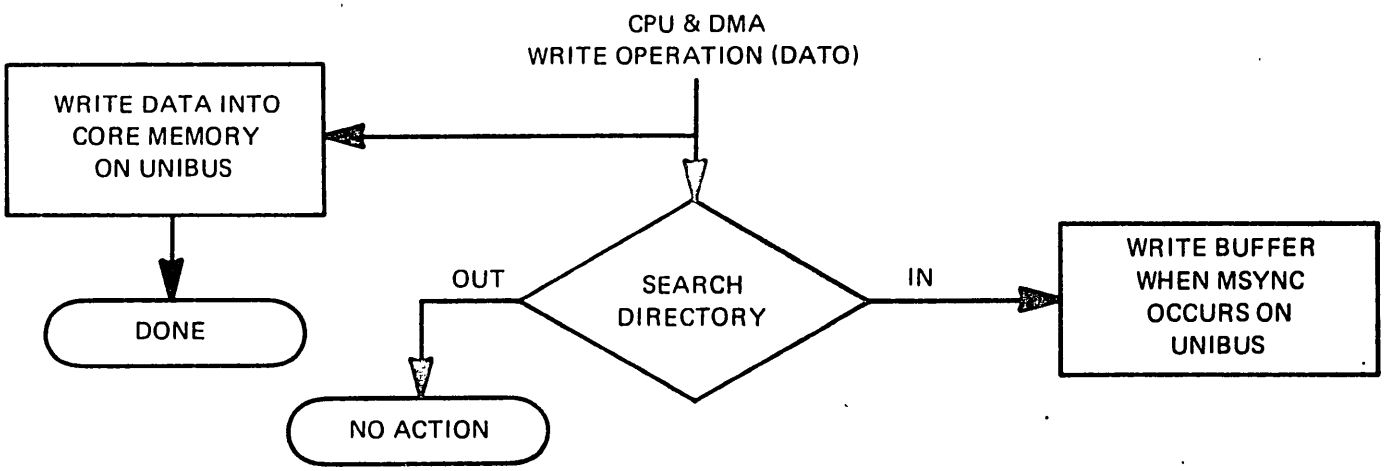


Figure 3-5.–WRITE-THROUGH ALGORITHM (WRITE)

– The core memory receives a BUSA MSYNC L signal.

– The core memory reads back the desired data and transmits a BUSA SSYNC L signal to indicate that the signals on the data lines are steady.

– The CPU and the Buffer receive the data.

– The CPU drops the BUSA MSYNC L signal.

– The core memory drops its BUSA SSYNC L signal, terminating the cycle.

When the CPU receives the data, the Buffer senses the negative-going edge of the BUSA SSYNC L signal and writes the Unibus data into the Buffer Memory Matrix. When the Buffer senses the positive-going edge of the BUSA MSYNC L signal, it terminates the Write Command signal to the Buffer Memory Matrix. Note that on the first time through a new program loop, the CPU encounters the Out of Buffer condition at each successive address and is forced to go out to the Unibus for each word of the loop. Repeating this loop a number of times allows the CPU to receive its data much faster than the first time, resulting in a significant performance improvement.

DATO OPERATION

The Buffer uses the Write-Through Algorithm illustrated in Figure 3-5 during DATO operations. During each DATO or DATOB operation, the Buffer does not respond with a BMC MEM L signal, thus forcing the CPU to "write-through" the Buffer by going out to core memory on the Unibus. This happens regardless of whether or not the specific address is in the Buffer. When the memory address is contained in the Buffer, the Buffer copies the data from the Unibus when it is written into core memory.

INTERFACE SIGNALS AND REQUIREMENTS

The Memory Buffer System interfaces externally with the Fastbus and Unibus and internally between Buffer modules. The interface lines transfer address, data, and control signals between the CPU and the Memory Buffer.

UNIBUS INTERFACE SIGNALS

All Unibus interface lines are unidirectional from the Unibus to the Buffer only. The Buffer receives Unibus address, data, and control signals.

BUSB A <17:00> L. The logic levels of the BUSB Address A00 through A17 L signals represent the Unibus address information. These signals enter the Buffer Matrix Controller on 18 interface lines.

BUSB MSYNC L. A low level Bus Master SYNChronization L signal initiates a Unibus data transfer by the selected slave device. This signal enters the Buffer Matrix Controller on a single interface line.

BUSB C0 L and BUSB C1 L. The BUSB Control Zero L and BUSB Control One L signals determine the type of Unibus memory operation. These signals enter the Buffer Matrix Controller on two interface lines. Table 3-1 illustrates the four logic level combinations which select one of four Unibus memory operations.

Table 3-1.—UNIBUS MEMORY OPERATION SELECT

C0	C1	MEMORY OPERATION
HIGH	HIGH	DATI
LOW	HIGH	DATIP
HIGH	LOW	DATO
LOW	LOW	DATOB

BUSB SSYNC L. A low level BUSB Slave SYNChronization L signal from the Unibus slave device either indicates that valid data are available during a DATI operation or acknowledges acceptance of Unibus data for a DATO operation. This signal enters the Buffer Matrix Controller on a single interface line.

BUSB D <15:00> L. The logic levels of the BUSB Data D00 through D15 signals represent the Unibus data information. These signals enter the Buffer Matrix Controller on 16 interface lines.

BUSB INIT L. A low level BUSB INITialize L signal initializes the Buffer while under program control, during a power down condition, or when the CPU Start switch is pressed. This signal enters the Buffer Matrix Controller on a single interface line.

BUSB DCL0 L. A low level BUSB DCL0w L signal protects data in memory when the d-c voltages drop below nominal values. This signal enters the Buffer Matrix Controller on a single interface line.

BUSA SACK L. A low level BUSA Selection ACKnowledge L signal from an interrupting device indicates that the device has received either a Bus Grant or Non-Processor Grant signal. The next Unibus cycle will be an Interrupt cycle. The BUSA SACK L signal enters the Auxiliary Buffer Matrix Controller on a single interface line.

BUSA BBSY L. A low level BUSA Bus BuSY L signal from the Bus Master device prevents other devices from gaining access to the Unibus by indicating that the Unibus is busy. This signal enters the Auxiliary Buffer Matrix Controller on a single interface line.

FASTBUS INTERFACE SIGNALS

The Fastbus Interface lines are unidirectional; the Buffer receives all Fastbus address signals, transmits Fastbus data out signals, but transmits and receives Fastbus control signals. All Fastbus interface signals enter or leave the Buffer at the Buffer Matrix Controller.

BMC MEM D <15:00> H. The logic levels of the BMC MEMory Data D00 through D15 signals represent the Fastbus Data Out information. These signals transfer from the Buffer to the Fastbus on 16 interface lines.

SAPJ PA <17:06> H and DAPB BAMX <05:00> H. The logic levels of the SAPJ PA 06 through 17 and DAPB BAMX 00 through 05 signals represent the Fastbus address information. The Buffer receives these signals from the Fastbus on 18 interface lines.

BMC MEM SYNC (B) L. A low level BMC MEMory SYNChronization signal indicates that the data in the Buffer are ready for transfer. This signal transfers from the Buffer to the CPU on a single interface line.

BMC MEM L. A low level BMC MEMory L signal indicates that the Buffer has searched the Directory, has determined that the Directory contains the specific address, and has determined that the data for the specific address are valid. This signal inhibits the CPU from performing a Unibus DATI cycle and transfers from the Buffer to the CPU on a single interface line.

UBCA CONTROL OK H. A high level UBCA CONTROL OK H signal indicates that the Memory bus control lines are valid and that the CPU is ready to receive the data from the Fastbus. This signal transfers from the CPU to the Buffer on a single interface line.

UBCC MEM BUS C0 L and UBCC MEM BUS C1 L. The UBCC MEMory BUS Control Zero L and UBCC MEMory BUS Control One L signals determine the type of Fastbus memory operation. These signals transfer from the Fastbus to the Buffer on two interface lines. Table 3-2 illustrates the four logic level combinations which select one of four Fastbus memory operations.

Table 3-2.—FASTBUS MEMORY OPERATION SELECT

C0	C1	MEMORY OPERATION
HIGH	HIGH	DATI
LOW	HIGH	DATIP
HIGH	LOW	DATO
LOW	LOW	DATOB

TMCE BUS OUT L. A low level TMCE BUS OUT L signal from the CPU determines if any Fastbus memory device has the address specified on the Fastbus address lines. This signal transfers from the CPU to the Buffer on a single interface line.

TMCE BEND CLR L. A low level TMCE BEND CLeaR L signal cancels the current Fastbus cycle. This signal transfers from the CPU to the Buffer on a single interface line.

PWRS MEM DC LO L. A low level PWRS MEMory DC LOw L signal is sent by the PDP 11/45 power supply when the DC power to the Fastbus drops below nominal value. This signal transfers from the power supply to the Buffer on a single interface line.

INTERNAL SIGNALS

The Buffer internal interface lines transfer address, data, and control signals between the Buffer Memory Matrix, Buffer Matrix Controller, and Auxiliary Buffer Matrix Controller modules of the Buffer.

MBB MEM SA<17:00>H. The Buffer Memory Matrix module transmits the SA00 through SA17 data signals to the Buffer Matrix Controller module for transfer to the Fastbus.

BMC MAD<08:01>H and BMC QTR K SEL H. The Buffer Matrix Controller module transmits the MAD01 through MAD08 and BMC QTR K SEL signals to the Buffer Memory Matrix module to select any one of 512 words.

BMC MTRX 2 SEL L and BMC MTRX 0 SEL L. These signals are permanently grounded to enable the Buffer Memory Matrix module.

BMC WRITE PULSE HIGH L. The Buffer Matrix Controller module transmits a low level BMC Write Pulse High L signal to the Buffer Memory Matrix module to enable Write operations in the upper byte.

BMC WRITE PULSE LOW L. The Buffer Matrix Controller module transmits a low level BMC Write Pulse Low L signal to the Buffer Memory Matrix module to enable Write operations in the lower byte.

BMC MEM DATA<17:00>H. The BMC MEMory DATA 00 through 17 signals are the 18 bits of data to be written from the Buffer Matrix Controller module into the Buffer Memory Matrix module.

ABMC DMABREQ H. The Auxiliary Buffer Matrix Controller module transmits a high level ABMC DMABREQ H signal to the Buffer Matrix Controller module to indicate that the next Unibus cycle will be an interrupt cycle.

ABMC DMA IN PROC L. The Auxiliary Buffer Matrix Controller module transmits a low level ABMC DMA IN PROCess L signal to the Buffer Matrix Controller module to indicate that the current Unibus cycle is an interrupt cycle.

BMC PWR CLR L. The Buffer Matrix Controller module transmits a low level BMC PoWeR CLear L signal to initialize the circuitry in the Auxiliary Buffer Matrix Controller module.

SECTION IV
MAINTENANCE

INTRODUCTION

Most Memory Buffer malfunctions develop characteristic symptoms. This section presents detailed maintenance information and recommendations in the form of tables and illustrations. The maintenance illustrations include an Error Classification Guide which directs the technician to the source of the malfunction in a logical manner. This section isolates FTI malfunctions to a modular level. Troubleshoot malfunctions in DEC equipment with appropriate DEC publications.

TEST EQUIPMENT RECOMMENDATIONS

EQUIPMENT	MANUFACTURER	TYPE
Oscilloscope	Tektronix	454A Series or equivalent
Voltage Probe	Tektronix	10:1 Attn. or equivalent
Digital Multimeter	Fairchild	Model 7050 or equivalent
VOM	Triplett	630-NA or equivalent

PREVENTIVE MAINTENANCE

The Model 4511 Memory Buffer system has no scheduled preventive maintenance requirements. The CPU environment may determine a need for additional maintenance.

CORRECTIVE MAINTENANCE

Corrective maintenance identifies the malfunctioning equipment and returns the system to error-free operation by means of the following four-step process:

1. Malfunction Analysis – Examining the error, its elements, and its relationship to the overall system operation. Is the error in the CPU, Interface lines, or Memory Buffer?

2. Error Classification – Isolating the source of the error to either DEC or FTI equipment by using the Error Classification Guide.

3. Maintenance Procedures – Attempting the fastest remedy to correct the error. Next, if necessary, systematic tracing of the error in a logical order to locate the source of the error.

4. Repair – Correcting the cause of the error and returning to normal operation.

MALFUNCTION ANALYSIS

The probability of circuit failure in the more complex CPU equipment is greater than in the Memory Buffer System. However, a failure in the Memory Buffer modules must be an initial consideration. Begin the Malfunction Analysis of the complete system installation by performing the DEC 0-124 K Memory Exerciser Diagnostic. Record the address location of any errors. Many apparent system errors are actually the result of faulty interface signals, program, or timing errors. Another frequent cause of system malfunctions is the power source.

Check the interface logic voltages and d-c power at the Memory Buffer inputs. The voltages must meet the requirements of Table 1-1 during dynamic and steady-state operation. Refer to the Power Supply Adjustment Procedure in Section II. If these preliminary checks indicate that the source of the malfunction may be in the Memory Buffer, proceed to Error Classification.

ERROR CLASSIFICATION

Memory Buffer errors have two major classifications: errors occurring after initial set up, and errors occurring after a period of error-free operation. The source of the error can be either in the CPU or in the Memory Buffer. Use the Error Classification Guide, Figure 4-1, to isolate the source of the error to either DEC or FTI equipment. The Error Classification Guide also contains diagnostic tests and maintenance procedures which locate the source of the error and expedite the return of the system to error-free operation.

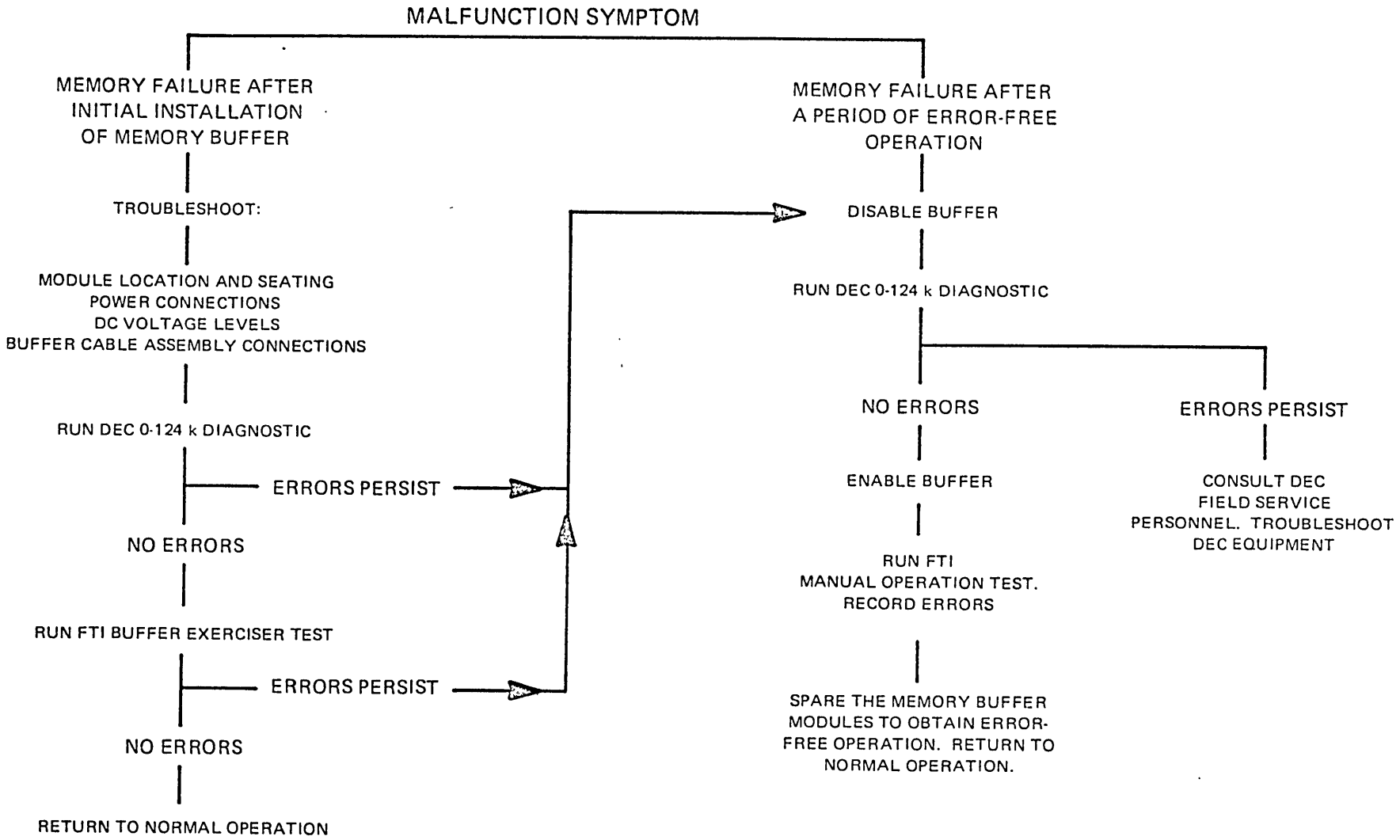


Figure 4-1
ERROR CLASSIFICATION GUIDE

SECTION V
REPLACEMENT PARTS LIST

INTRODUCTION

This section contains the Replacement Parts Lists for each assembly of this product. Each parts list is identified by the assembly title and parts list number. Each component is identified by the FABRI-TEK part number, part description, and reference designation. The reference designation corresponds to the schematic component designation.

ORDERING PARTS FROM FABRI-TEK

When ordering from the replacement parts list; specify the model number, the assembly part number, the FABRI-TEK component part number, and the reference designation. Order parts from:

FABRI-TEK INCORPORATED
5901 South County Road 18
Minneapolis, Minnesota 55436

FABRI-TEK INCORPORATED

TITLE	SHEET		SIZE	PARTS LIST	CODE	LTR.	STAT.
BU ASSY BUFFER MATRIX CTRL	02	09/30/74	D	190-1665-00	00	D	F

FIND NO.	DWG SIZE	PART NUMBER	REV. CODE	QUANTITY PER ASSY.	U/M	PART DESCRIPTION	REFERENCE DESIGNATION LINE	A	B	C	D	P.C.	REL.
001	D	130-1880-00	00	1.0	E	P.C. BOARD BUFFER MATRIX CTRL							F01C
002	A	134-0321-00	00	1.0	E	INT. CKT 13 INPUT NAND	01	K2U1					F999
003	A	134-0209-00	00	6.0	E	IC HEX INVERTERS	01	D2U1	E2U1	N3U1			F999
							02	P3U1	T3U1	U3U1			
004	A	134-0205-00	00	1.0	E	IC DUAL-4 INP POS-NAND BFR/DVR	01	F2U1					F999
005	A	134-0357-00	00	3.0	E	IC BUFFER QUAD-2-INPUT BUFFER	01	H3U1	N1U1	N2U1			F999
007	A	134-0294-00	00	2.0	E	IC COMPTR 4-BIT MAGNITUDE 7485	01	U4U1	U5U1				F999
009	A	134-0320-00	00	3.0	E	IC TTL SYNC. 4 BIT CTR	01	K1U1	J1U1	J2U1			F999
010	A	134-0167-00	00	1.0	E	IC GATE TRIPLE 3-INPUT NAND	01	E1U1					F999
011	A	134-0198-00	00	4.0	E	IC DUAL MO NOSTABLE MV W/CLEAR	01	E4U1	F1U1	H1U1	A2U1		F999
012		134-0207-00	00	4.0		IC GATE QUADR-2-INP NAND	01	B2U1	C3U1	J4U1	J5U1		F999
013	A	134-0244-00	00	1.0	E	IC NAND OPEN-COL OP 74S22	01	F5U1					F999
015	A	134-0213-00	00	3.0	E	IC GATE TPL 3 INP POS-AND	01	D3U1	E5U1	J3U1			F999
016	A	134-0236-00	00	1.0	E	IC GATE TRIPLE 3-INP NAND	01	L5U1					F999
017	A	134-0192-00	00	2.0	E	INTEG CKT HEX INVERTER T2L	01	C1U1	B3U1				F999
018	A	134-0322-00	00	18.0	E	INT. CKT. 256 BIT BIPOLAR RAM	01	L1U1	L2U1	P1U1	P2U1		F999
							02	R1U1	R2U1	S1U1	S2U1		
							03	T1U1	T2U1	U1U1	U2U1		
							04	V1U1	V2U1	W1U1	W2U1		
							05	X1U1	X2U1				
019	A	134-0308-00	00	11.0	E	IC TTL QUAD 2 INPUT NOR	01	B4U1	B5U1	C4U1	C5U1		F999
							02	D5U1	K5U1	M5U1	N5U1		
021	A	134-0325-00	00	8.0	E	IC SEL/MUX QUAD 2-TO-1-LINE	03	P5U1	R5U1	S5U1			F999
							01	L3U1	M1U1	M2U1	M4U1		
022	A	134-0243-00	00	5.0	E	IC NAND OPEN-COL OP 74S03	02	N4U1	P4U1	R4U1	S4U1		F999
							01	C2U1	V4U1	V5U1	Z4U1		
023	A	134-0352-00	00	2.0	E	IC TTL A BIT QUAD EXCL. OR	02	Z5U1					F999
							01	V3U1	W3U1				
024	A	134-0335-00	00	5.0	E	IC LATCH 6 BIT HIGH SP C3404C	01	L4U1	W4U1	W5U1	Y4U1		F999
							02	Y5U1					
025	A	023-0117-00	00	13.0	E	CAP TANT 6.8 MFD 35V 10%	01	B1C1	C3C1	D5C1	F2C1		F999
							02	K3C1	K4C1	N5C1	P1C1		
							03	S2C1	W3C1	X1C1	X4C1		
							04	Z5C1					
026	A	023-0455-00	00	88.0	E	CAP FIXED 0.01UF 20% 50V	01	A1C1	A2C1	A3C1	A4C1		F999
							02	B1C2	B2C1	B3C1	B4C1		
							03	C1C1	C2C1	C3C2	C4C1		
							04	D1C1	D2C1	D3C1	D4C1		
							05	E1C1	E2C1	E3C1	E4C2		
							06	F1C2	F2C2	F3C1	F4C1		

DETACHED PARTS LIST

CHECKED

DATE

APPROVED

DATE 10-1-74

FABRI-TEK INCORPORATED

TITLE	SHEET		SIZE	PARTS LIST	CODE	LTR.	STAT.
BD ASSY BUFFER MATRIX CTRL	03	09/30/74	D	19C-1665-00	C0	D	F

FIND NO.	DWG SIZE	PART NUMBER	REV. CODE	QUANTITY PER ASSY.	U/M	PART DESCRIPTION		REFERENCE DESIGNATION LINE	A	B	C	D	P.C.	REL.
								07	H1C3	H2C1	H3C1	H4C1		
								08	J1C2	J2C1	J3C1	J4C1		
								09	K1C1	K2C1	K3C2	K4C2		
								10	L2C1	L3C1	L4C1	M1C1		
								11	M2C1	M3C1	M4C1	N1C1		
								12	N2C1	N3C1	N4C1	P1C2		
								13	P2C1	P3C1	P4C1	R1C1		
								14	R2C1	R3C1	R4C1	S1C1		
								15	S2C2	S3C1	S4C1	T1C1		
								16	T2C1	T3C1	T4C1	U1C1		
								17	U2C1	U3C1	U4C1	V1C1		
								18	V2C1	V3C1	V4C1	W1C1		
								19	W2C1	W3C2	W4C1	X1C2		
								20	X2C1	X3C1	X4C2	Y1C1		
								21	Y2C1	Y3C1	Y4C1	Z1C1		
								22	Z2C1	Z3C1	Z4C1	J1C1		
029	A	134-0174-00	00	4.0	E	IC GATE	8-BIT PARITY GEN/CHK	01	A4U1	A5U1	X4U1	X5U1		FC1C
030	A	134-0177-01	00	1.0	E	IC GATE	QUAD 2-INPUT NOR	01	D4U1					FD1C
031	A	134-0218-00	00	3.0	E	IC GATE	QUAD 2-INPPOS NAND	01	B1U1	D1U1	A1U1			FC1C
032	A	134-0350-00	00	2.0	E	IC, TTL	DUAL D-TYPE FF	01	E3U1	E4U1				FD1C
033	A	134-0206-00	00	1.0	E	IC GATE	DUAL-4-INPUT NAND	01	H5U1					FC1C
034	A	108-0432-00	00	1.0	E	RES FIXED	4.3K 5% 1/4WCC	01	E4R3					F999
035	A	108-0102-00	00	11.0	E	RES FIXED	1K 5% 1/4WCC	01	B1R1	D1R1	C1R1	T4R1		F999
								02	T4R2	T4R3	T4R4	T4R5		
								03	T4R6	T4R7	E4R1			
036	A	108-0512-00	00	5.0	E	RESISTOR	5.1K 1/4W 5%	01	F1R1	F1R2	H1R1	H1R2		F999
								02	A3R4					
037	A	108-0471-00	00	2.0	E	RESISTOR	470 OHMS 5% 1/4W CC	01	K2R1	D5R1				F999
038	A	108-0331-00	00	9.0	E	RES FIXED	330 OHMS 5% 1/4W CC	01	C2R1	C2R2	E4R2	N2R1		F999
								02	U5R1	W3R1	E3R1	B2R1		
								03	A3R3					
039	A	108-0151-00	00	1.0	E	RES C	150 OHM 1/4W 5%	01	D5R2					FD1C
040	C	025-0201-00	00	2.0	E	SWITCH TGL	PC MTG 2 POS ON - ON	01	J1S1	K1S1				FD1C
041	C	025-0201-01	00	1.0	E	SWITCH TGL	PC MTG 2POS ON - MOM	01	H1S1					F999
042	C	049-0091-00	00	1.0	E	EJECTOR	CARD LEFT SIDE							FC1C
043	C	049-0091-01	00	1.0	E	EJECTOR	CARD RIGHT SIDE							FD1C
044	C	011-2194-00	00	1.0	E	BRACKET	EJECTOR MTG L SIDE							FD1C
045	C	011-2194-01	00	1.0	E	BRACKET	EJECTOR MTG R SIDE							FD1C
046		007-0384-00	00	4.0	E	SCREW	440X3/16 FH SST							F999
047	G	000-0036-00	00	4.0	E	WASHER	#4 FLAT SST							FD1C

DETACHED PARTS LIST

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DATE 10-1-74

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TITLE	SHEET		SIZE	PARTS LIST	CODE	LTR.	STAT.
BD ASSY BUFFER MATRIX CTRL	04	09/30/74	D	190-1665-00	00	D	F

FIND NO.	DWG SIZE	PART NUMBER	REV. CODE	QUANTITY PER ASSY.	U/M	PART DESCRIPTION	REFERENCE DESIGNATION LINE	A	B	C	D	P.C.	REL.
048	G	010-0057-00	00	4.0	E	LOCK-NUT #4-40							F01C
049		015-0132-00	00	2.0	E	PIN 1/8X3/8 SST							F010
050	C	138-0019-62	00	1.0	E	SCHEMATIC BUFFER MATRIX CTRL							F01C
051	A	024-1677-00	00	2.0	E	CONNECTOR 20 POS. RT. ANGLE MT	01	E1	L1				F999
052	A	077-0016-00	00	4.0	E	JUMP WIRE 22GA SOLID COPPER	01	T5J1	T5J2	D2J1	F4J1		F999
053	C	024-1459-01	00	1.0	E	SOCKET IC 14 DUAL IN LINE	01	T5					F01C
054	C	015-0259-01	00	24.0	E	PIN CONN .025 SQ	01	B2TP1	C1TP1	C4TP1	D2TP1		F999
							02	D3TP1	D3TP2	E1TP1	E4TP1		
							03	F3TP1	F4TP1	F5TP1	H5TP1		
							04	J3TP1	J3TP2	K5TP1	K5TP2		
							05	L4TP1	L4TP2	L4TP3	P1TP1		
							06	T4TP1	V1TP1	Z4TP1	C2TP1		
055	G	023-0179-00		2.0	E	CAP FIXED 220PF 10% 200V CER	01	C1C2	H1C2				*01C
056	G	023-0181-00	00	2.0	E	CAPACITOR CERAMIC, 100PF, 200V	01	F1C1	A3C3				F999
057		023-0206-00	00	3.0	E	CAP CER 33P200V 10%	01	H1C4	H1C1	E5C1			F999
058		108-0000-99	00	3.0	E	RES FIXED 1/4W SELECTED VALUE	01	E4R4	D4R1	A3R5			F999
059	C	116-0676-00	00	1.0	E	SUPPORT BAR							F999
060	G	009-1395-00	00	1.0	E	SPACER RND 4-40 1/4ODX375LG NYL							F999
061	A	082-2996-00	00	REFERENCE	E	CHART CONN BUFFER CONT							F999
062	G	007-1352-00	00	1.0	E	SCREW FH NYLON, 4-40XO.500,							F999

DETACHED PARTS LIST

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DATE

APPROVED

DATE 10-1-74

FABRI-TEK INCORPORATED

TITLE	SHEET		SIZE	PRTS	CODE	LIN.	STAT.
BD ASSY BUFFER MEMORY MATRIX	02	03/29/74	D	190-1666-00	00	CB	F

FIND NO.	DWG SIZE	PART NUMBER	REV. CODE	QUANTITY PER ASSY.	U/M	PART DESCRIPTION	REFERENCE DESIGNATION LINE	A	B	C	D	P.C.	REL.
001	D	130-1661-00	00	1.0	E	PC BOARD BUFFER MEMORY MATRIX							F008
002	A	134-0322-00	00	36.0	E	INT. CKT. 256 BIT BIPOLAR RAM	01	E1	E2	E3	E4		F001
							02	E5	E6	E7	E8		
							03	E9	F1	F2	F3		
							04	F4	F5	F6	F7		
							05	F8	F9	G1	G2		
							06	G3	G4	G5	G6		
							07	C7	G8	G9	H1		
							08	H2	H3	H4	H5		
							09	H6	H7	H8	H9		
003	A	134-0209-00	00	6.0	E	IC HEX INVERTERS	01	C3	C5	C6	C7		F999
							02	C8	D9				
004	A	134-0209-00	00	12.0	E	IC DUAL-4 INP POS-NAND BFR/DVR	01	C1	C2	C4	C9		F002
							02	D1	D2	D3	D4		
							03	D5	D6	D7	D8		
005	A	023-0117-00	00	9.0	E	CAP TANT 6.8 MFD 35V 10%	01	C4C1	C7C1	C9C1	E4C1		F999
							02	E7C1	E9C1	G4C1	G7C1		
							03	G9C1					
006	A	023-0429-00	00	24.0	E	CAP FIXED 0.01UF 20% 50V	01	C1C1	C2C1	C3C1	C4C2		F002
							02	C5C1	C6C1	C7C2	C8C1		
							03	C9C1	D1C1	D2C1	D3C1		
							04	D4C2	D5C1	D6C1	D7C2		
							05	D8C1	D9C1	E1C1	E2C1		
							06	E3C1	E4C2	E5C1	E6C1		
							07	E7C2	E8C1	E9C1	F1C1		
							08	F2C1	F3C1	F4C2	F5C1		
							09	F6C1	F7C2	F8C1	F9C1		
							10	G1C1	G2C1	G3C1	G4C2		
							11	G5C1	G6C1	G7C2	G8C1		
							12	G9C1	H1C1	H2C1	H3C1		
							13	H4C2	H5C1	H6C1	H7C2		
							14	H8C1	H9C1				
007	A	108-0331-00	00	2.0	E	RES FIXED 330 OHMS 5% 1/4W CC	01	D5R1	D7R1				F002
008	A	108-0102-00	00	2.0	E	RES FIXED 1K 5% 1/4WCC	01	D1R1	F9R1				F002
009	A	377-0010-00	00	1.0	E	JUMPER WIRE 22GA SOLID COPPER	01	F9J1					F999
010	A	352-0123-04	00	1.0	E	INDICATOR LED PCB EDGE VIEW							F002
011	C	349-0091-00	00	1.0	E	EJECTOR CARD LEFT SIDE							F008
012	C	349-0091-01	00	1.0	E	EJECTOR CARD RIGHT SIDE							F008
013	C	311-2194-00	00	1.0	E	BRACKET EJECTOR MTG L SIDE							F008
014	C	311-2194-01	00	1.0	E	BRACKET EJECTOR MTG R SIDE							F008

MICROFILMED

DETACHED PARTS LIST

CHECKED	DATE	APPROVED	DATE
		W.D. Howell	9-4-74

FABRI-TEK INCORPORATED

TITLE	SHEET		SIZE	PARTS LIST	CODE	LTR.	R STAT.
BD ASSY BUFFER MEMORY MATRIX	03	08/29/74	D	190-1066-00	00	C	F

FIND NO.	DWG SIZE	PART NUMBER	REV. CODE	QUANTITY PER ASSY.	U/M	PART DESCRIPTION	REFERENCE DESIGNATION LINE	A	B	C	D	P.C.	REL.
015	A	007-1189-00	00	4.0	E	SCREW FLH 4-40X7/16 82 CSK SST							F999
016	G	008-0036-00	00	4.0	E	WASHER 4 FLAT SST							F008
017	G	010-0057-00	00	4.0	E	LOCK-NUT #4-40							F008
018		015-0132-00	00	2.0	E	PIN 1/8X3/8 SST							F008
019	C	116-0075-00	00	1.0	E	SUPPORT BAR							F999
020	G	009-1395-00	00	1.0	E	SPACER RND 4-40 1/40DX375LG NYL							F999
021	G	007-1352-00	00	1.0	E	SCREW FH NYLON,4-40X0.500,							F999
022	A	062-2997-00	00	REFERENCE	E	CHART CONN BUFFER MEMORY							F999
100	C	130-0019-03	00	REFERENCE	E	SCHEMATIC BUFFER MEMORY MATRIX							F002

MICROFILMED DETACHED PARTS LIST

CHECKED	DATE	APPROVED	DATE
			9-4-74

FABRI-TEK INCORPORATED

TITLE	SHEET		SIZE	PARTS LIST	CODE	LTR.	N STAT.
BOARD ASSY POWER SUPPLY	02	01/21/75	D	190-1747-00	C0	-B	F

FIND NO.	DWG SIZE	PART NUMBER	REV. CODE	QUANTITY PER ASSY.	U/M	PART DESCRIPTION	REFERENCE DESIGNATION LINE	A	B	C	D	P.C.	REL.
001	D	130-1974-00	00	1.0	E	P.C. BOARD POWER SUPPLY							F001
002	A	022-0299-00	00	4.0	E	DIODE RECTIFIER 3.0A	01	CR1	CR2	CR3	CR4	012	F001
003	G	022-0334-00	00	1.0	E	DIODE ZENER, 15V, 1WATT	01	CR9				010	F001
004	G	022-0258-00	00	1.0	E	DIODE	01	CR8				011	F001
005	A	022-0163-00	00	1.0	E	DIODE SI SWITCHING LOGIC	01	CR6				010	F001
006	A	021-0213-00	00	2.0	E	TRANSISTOR PNP 100V 400MA	01	Q1	Q4				F001
007	A	021-0250-00	00	1.0	E	TRANSISTOR PNP, SILICON PWR	01	Q3					F001
008	A	021-0137-00	00	1.0	E	TRANSISTOR SIMILAR TO 2N3725	01	Q5					F001
009	A	021-0251-00	00	1.0	E	TRANSISTOR UNIJUNCTION, PROG.	01	Q6					F001
010		134-0305-00	00	1.0	E	IC REG. PRECISION VOLT. REG.	01	U1					F001
011	A	023-0105-00	00	1.0	E	CAP FIXED 15UF 10% 20V	01	C8				076	F001
012	G	023-0262-00	00	3.0	E	CAP CER 0.01UF +-20% 200V	01	C4	C5	C9		044	F001
013	A	023-0461-00	00	2.0	E	CAP DISC 1500 PF 20% 500 VDC	01	C3	C12			044	F001
014	A	023-0549-00	00	1.0	E	CAPACITOR COMPUT.GDE. 2500C,UF	01	C1					F001
015	A	023-0547-00	00	2.0	E	CAPACITOR COMP GDE 5000UF, 10V	01	C6	C7				F001
016	A	023-0087-00	00	2.0	E	CAP 33 PF	01	C10	C11			044	F001
017	G	023-0014-00	00	1.0	E	CAP CER 0.1UF+100%-20% 30V	01	C2					F001
018	G	085-0034-00	00	2.0	E	CABLE TIE NYLON NATURAL 15IN L							F999
019	C	019-0200-00	00	2.0	E	CHOKE 150 UH 12A	01	L1	L2				F001
021	G	070-0150-00	00	2.0	E	FUSEHOLDER PHOSPHOR BRONZE CLIP	01	USE	WITH F1				F001
022	G	070-0040-00	00	1.0	E	FUSE 15A 250V CERAMIC	01	F1					F001
023	A	077-0016-00	00	2.0	E	JUMP WIRE 22GA SOLID COPPER	01	R14	R15				F999
024	C	052-0128-00	00	1.0	E	INDICATOR AMBER CAP 5V 20MA	01	DS1					F999
025	A	026-0136-02	00	1.0	E	POT 200 OHM PC BD MTG	01	R27					F001
026		103-0392-00	00	1.0	E	RES FIXED 3.9 K 5% 1WCC	01	R2				012	F001
027	A	103-0821-00	00	1.0	E	RES C 820 OHM 1W 5%	01	R3				012	F001
028	A	103-0100-00	00	1.0	E	RES C 10 OHM 1W 5%	01	R11				010	F001
029	A	108-0100-00	00	1.0	E	RES C 10 OHM 1/4W 5%	01	R10				010	F999
030	G	108-0270-00	00	4.0	E	RES C 27 OHM 1/4W 5%	01	R5	R7	R13	R23	010	F001
031	A	108-0101-00	00	2.0	E	RES FIXED 100 OHMS 5% 1/4W CC	01	R12	R25			010	F001
032	A	108-0151-00	00	2.0	E	RES C 150 OHM 1/4W 5%	01	R8	R9			010	F001
033	A	108-0102-00	00	2.0	E	RES FIXED 1K 5% 1/4WCC	01	R6	R21			010	F001
034	A	108-0152-00	00	1.0	E	RES C 1.5 K 1/4W 5%	01	R18				010	F001
035		108-0752-00	00	1.0	E	RESISTOR 7.5K 1/4W 5%	01	R20				010	F001
036	A	108-0103-00	00	1.0	E	RESISTOR 10K OHMS 5% 1/4WCC	01	R19				010	F001
037		108-0123-00	00	1.0	E	RES C 12 K 1/4W 5%	01	R16				010	F001
038	A	108-0183-00	00	2.0	E	RES C 18 K 1/4W 5%	01	R17	R22			010	F001
039		108-0474-00	00	1.0	E	RESISTOR .47 MEG 1/4W 5%	01	R24				010	F001
040		202-5110-00	00	2.0	E	RESISTOR 649 1/4W 1%	01	R26	R28			010	F001
041	G	106-0486-00	00	2.0	E	RES WW PWR .05 OHM 1% 5 WATT	01	R1	R4				F001

DETACHED PARTS LIST

CHECKED	DATE	APPROVED	DATE
C. Madsen	1-22-75	J. Spangler	1-22-75

FABRI-TEK INCORPORATED

TITLE	SHEET		SIZE	PARTS LIST	CODE	LTR.	STAT.
BOARD ASSY POWER SUPPLY	03	01/21/75	D	190-1747-00	00	-B	F

FIND NO.	DWG SIZE	PART NUMBER	REV. CODE	QUANTITY PER ASSY.	U/M	PART DESCRIPTION	REFERENCE DESIGNATION LINE	A	B	C	D	P.C.	REL.
042	C	024-1666-00	00	1.0	E	CONNECTOR 8 POS SOCKET HSG							F001
043	A	013-0031-00	00	8.0	E	CONTACT RECEPT.,PCB,.062 BD							F001
044	G	014-0047-00	00	4.0	E	RIVET 3/32X1/4 OV HD AL							F001
045		016-0521-00	00	.5	F	WIRE 14AWG WHITE							F001
046	G	007-0164-00	00	1.0	E	SCREW 4-40X5/16							F001
047	G	010-0017-00	00	1.0	E	NUT HEX 440 NC2-B SST							F001
048	G	061-0045-00	00	2.0	E	TERM-CRIMP ON SPR SPADE INS #10							F001
049	C	138-0020-56	00	REFERENCE	E	SCHEMATIC POWER SUPPLY							F001
050	A	108-0391-00	00	1.0	E	RES FIXED 390 OHMS 5% 1/4WCC	01	CR5					F999

DETACHED PARTS LIST

CHECKED	DATE	APPROVED	DATE
C. Madsen	1-22-75	J. Straughan	1-22-75

FABRI-TEK INCORPORATED

TITLE	SHEET	08/29/74	SIZE	ITS-L	CODE	LIR.	STAT.
BOARD ASSY AUX BUFFER MATRIX	02		D	190-1707-00	00	BA	F

FIND NO.	DWG SIZE	PART NUMBER	REV. CODE	QUANTITY PER ASSY.	U/M	PART DESCRIPTION	REFERENCE DESIGNATION LINE	A	B	C	D	P.C.	REL.
001	D	190-1994-00	00	1.0	E	P.C. BOARD AUX BUFFER MATRIX							F012
002	D	190-1995-00	00	1.0	E	P.C. BOARD AUXBFR MATRIX JUMPER							F012
003	A	134-0350-00	00	2.0	E	IC, TTL DUAL D-TYPE FF	01	C1U1	D1U1				F999
004	A	134-0209-00	00	1.0	E	IC HEX INVERTERS	01	C2U1					F999
005	A	134-0306-00	00	1.0	E	IC TTL QUAD 2 INPUT NOR	01	C3U1					F012
006	A	023-0455-00	00	3.0	E	CAP FIXED 0.01UF 20% 50V	01	C1C1	C2C1	C3C1			F012
007	A	023-0117-00	00	1.0	E	CAP TANT 0.8 MFD 35V 10%	01	C4C1					F012
008	A	100-0471-00	00	1.0	E	RESISTOR 470 OHMS 5% 1/4W CC							F012
009	C	049-0091-01	00	1.0	E	EJECTOR CARD RIGHT SIDE							F012
010	C	011-2194-01	00	1.0	E	BRACKET EJECTOR MTG R SIDE							F012
011	G	007-0149-00	00	2.0	E	SCREW 440X3/8 FH SST							F012
012	G	008-0035-00	00	2.0	E	WASHER 4 FLAT SST							F012
013	G	010-0057-00	00	2.0	E	LOCK-NUT #4-40							F012
014		015-0132-00	00	1.0	E	PIN 1/8X3/8 SST							F012
015	A	024-1077-00	00	1.0	E	CONNECTOR 20 POS. RT. ANGLE MT							F012
016	A	060-0090-39	00	.2	F	CABLE MULTICOND 28 GA FLAT							F012
017	C	002-0295-00	00	1.0	E	BLOCK P.C. BOARD MTG							F012
018	G	007-0107-00	00	6.0	E	SCREW 032X1/4 PH SST							F999
019	G	008-0040-00	00	8.0	E	WASHER FLAT #8							F012
020		008-0100-00	00	8.0	E	WASHER 8 FLAT NYLON							F012

MICROFILMED

DETACHED PARTS LIST

CHECKED

DATE

APPROVED

DATE 9-3-74

FABRI-TEK INCORPORATED

TITLE	SHEET		SIZE	PARTS LIST	CODE	LTR.	STAT.
ASSY POWER SUPPLY MODEL 1744	02	01/23/75	.0	201-0124-00	0	-E	F

FIND NO.	DWG SIZE	PART NUMBER	REV. CODE	QUANTITY PER ASSY.	U/M	PART DESCRIPTION	REFERENCE DESIGNATION LINE	A	B	C	D	P.C.	REL.
001	D	190-1747-00	00	1.0	E	BOARD ASSY POWER SUPPLY							F006
002	D	048-0030-00	00	1.0	E	HEATSINK POWER SUPPLY							F006
003	A	021-0216-00	00	1.0	E	TRANSISTOR NPN 60VOLT 12AMP							F006
004	A	022-0333-00	00	1.0	E	DIODE RECT 20A,200V,FAST RECOV.							F006
005	A	030-0019-00	00	1.0	E	SCR 50V,25 AMP, SILICON							F006
006		007-1065-00	00	2.0	E	SCREW 440X7/16 PH BRS							F999
007	G	006-0043-00	00	4.0	E	WASHER #4 LOCK EXT TOOTH STL							F006
008	G	010-0017-00	00	2.0	E	NUT HEX 440 NC2-B SST							F006
009	D	033-0245-00	00	1.0	E	HOUSING POWER SUPPLY							F006
010	G	007-0115-00	00	2.0	E	SCREW 440X3/8 PH SST							F006
011	G	007-0141-00	00	6.0	E	SCREW 440X5/16 FH SST							F006
012	C	042-0741-00	00	1.0	E	COVER POWER SUPPLY							F006
013		016-0631-00	00	.5	F	WIRE 16 GA WHITE TEFLON							F006
014	B	062-0306-00	00	1.0	E	BLOCK DIODE MTG							F999
015		009-0401-00	00	4.0	E	SPACER #03/8X.125 1/4H NYL							F999
016	A	129-0005-00	00	REFERENCE	E	ADHESIVES SILICONE HEAT SINK							F999
017	C	130-0020-00	00	REFERENCE	E	SCHEMATIC POWER SUPPLY							F999
018	A	017-0197-03	00	1.0	E	NAME PLATE PREFERRED							F999
019	G	007-0159-00	00	3.0	E	SCREW 1032X1/2 FH SST							F999
020	G	006-0011-00	00	3.0	E	WASHER 10 INT TOOTH STL							F999
021		032-0420-00	00	1.0	E	INSULATOR TRANSISTOR , TO-3							F999

DETACHED PARTS LIST

CHECKED	DATE	APPROVED	DATE

SECTION VI
REFERENCE DOCUMENTS

INDEX

CHARTS

LOGICS

SCHEMATICS

SYM	DESCRIPTION	DATE	APPR
00A	EC 20629 REL MANDATORY	8-8-74	

F

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REVISION																												
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REVISION																												
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REVISION INDEX

PREPARED	FABRI-TEK
CHECKED	
APPROVED Ronald N. Monroe	TITLE: BUFFER MATRIX CONTROL CONNECTOR CHART
DATE 26 June 74	PART NUMBER: 082-2996-00
SHEET 1 OF 7	USED ON: PDP 11/45

PIN	I/O	FROM	TO	SIGNAL	TITLE	H/L
A1	O	BMC	BMM	BMC	MEM DATA 06	H
A2	I	P.S	BMC	+5V		
B1	O	BMC	BMM	BMC	MEM DATA 08	H
B2						
C1	O	BMC	BMM	BMC	MEM DATA 11	H
C2	I	P.S	BMC		GND	
D1	O	BMC	BMM	BMC	MEM DATA 07	H
D2	O	BMC	BMM	BMC	MEM DATA 02	H
E1	O	BMC	BMM	BMC	MEM DATA 17	H
E2	O	BMC	BMM	BMC	MEM DATA 03	H
F1	O	BMC	BMM	BMC	MEM DATA 13	H
F2	O	BMC	BMM	BMC	MEM DATA 01	H
H1						
H2	O	BMC	BMM	BMC	MEM DATA 15	H
J1	O	BMC	BMM	BMC	MEM DATA 04	H
J2	O	BMC	BMM	BMC	MEM DATA 14	H
K1	O	BMC	BMM	BMC	MEM DATA 12	H
K2	O	BMC	BMM	BMC	MEM DATA 00	H
L1	O	BMC	BMM	BMC	MEM DATA 16	H
L2						
M1	O	BMC	BMM	BMC	MEM DATA 10	H
M2						
N1	O	BMC	BMM	BMC	MEM DATA 09	H
N2	I	P.S	BMC		GND	
P1	O	BMC	BMM	BMC	MEM DATA 05	H
P2						
R1						
R2						
S1	O	BMC	BMM	BMC	WRITE PULSE HIGH	L
S2	O	BMC	BMM	BMC	WRITE PULSE LOW	L
T1	I	P.S	BMC		GND	
T2						
U1	O	BMC	BMM	BMC	CENABLE	L
U2						
V1	I	P.S	BMC		+5V	
V2						

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR A | SHEET 2 OF 7 | MODEL NUMBER

DRAWN

CHECKED

APPROVED

PRODUCT | DATE

FABRI-TEK

TITLE

BUFFER MATRIX CONTROL

CONNECTOR CHART

PART NUMBER 082-2996-00

REV. A

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PIN	I/O	FROM	TO	SIGNAL	TITLE	H/L
A1						
A2	I	P.S.	BMC		+5V	
B1						
B2						
C1						
C2	I	P.S.	BMC		GND	
D1						
D2						
E1	O	BMC	BMM	BMC	MAD 02	H
E2	O	BMC	BMM	BMC	MAD 01	H
F1						
F2						
H1						
H2						
J1						
J2						
K1						
K2						
L1						
L2						
M1	I	BUSB	BMC	BUSB	D04	L
M2	O	BMC	CPUC	BMC	MEM SYNC (B)	L
N1	I	BUSB	BMC	BUSB	D07	L
N2	I	P.S.	BMC		GND	
P1	I	BUSB	BMC	BUSB	D03	L
P2	I	BUSB	BMC	BUSB	D02	L
R1	I	BUSB	BMC	BUSB	D11	L
R2	I	BUSB	BMC	BUSB	D12	L
S1	I	BUSB	BMC	BUSB	D10	L
S2	I	BUSB	BMC	BUSB	D15	L
T1	I	P.S.	BMC		GND	
T2	I	BUSB	BMC	BUSB	D09	L
U1	I	BUSB	BMC	BUSB	D08	L
U2	I	CPUC	BMC	PWRS	MEM DC LO	L
V1	I	P.S.	BMC		+5V	
V2						

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR B | SHEET 3 OF 7 | MODEL NUMBER

DRAWN

CHECKED

APPROVED

PRODUCT | DATE

FABRI-TEK

TITLE

BUFFER MATRIX CONTROL

CONNECTOR CHART

PART NUMBER 082-2996-00

REV. A

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PIN	I/O	FROM	TO	SIGNAL	TITLE	H/L
A1	I	BUSB	BMC	BUSB	SSYNC	L
A2	I	P.S.	BMC		+5V	
B1	I	BUSB	BMC	BUSB	D13	L
B2	I	CPUC	BMC	UBCA	CONTROL OK	H
C1	I	BUSB	BMC	BUSB	D01	L
C2	I	P.S.	BMC		BND	
D1	O	BMC	BMM	BMC	MAD05	H
D2	I	BUSB	BMC	BUSB	D00	L
E1						
E2	I	BUSB	BMC	BUSB	IN1T	L
F1						
F2	I	BUSB	BMC	BUSB	D05	L
H1						
H2	I	BUSB	BMC	BUSB	D06	L
J1	I	BUSB	BMC	BUSB	D14	L
J2	I	BUSB	BMC	BUSB	A01	L
K1	O	BMC	BMM	BMC	MAD04	H
K2	I	FBUS	BMC	TMCE	BUST OUT	L
L1						
L2	I	BUSB	BMC	BUSB	C1	L
M1	O	BMC	BMM	BMC	MAD08	H
M2	I	BUSB	BMC	BUSB	A08	L
N1	O	BMC	BMM	BMC	MAD03	H
N2	I	P.S.	BMC		GND	
P1	O	BMC	BMM	BMC	MAD07	H
P2	I	CPUC	BMC	UBCB	PERF ACKN	L
R1	O	BMC	BMM	BMC	MAD06	H
R2	I	BUSB	BMC	BUSB	A00	L
S1						
S2	I	BUSB	BMC	BUSB	C0	L
T1	I	P.S.	BMC		GND	
T2						
U1						
U2						
V1	I	P.S.	BMC		+5V	
V2						

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR C	SHEET 4 OF 7	MODEL NUMBER
	DRAWN	FABRI-TEK
	CHECKED	TITLE: BUFFER MATRIX CONTROL CONNECTOR CHART
	APPROVED	PART NUMBER: 082-2996-00
PRODUCT	DATE	REV.: A

Form 607 7-70

PIN	I/O	FROM	TO	SIGNAL	TITLE	H/L
A1	I	CPUC	BMC	TMCE	BEND CLR	L
A2	I	P.S.	BMC		+5V	
B1						
B2	I	FBUS	BMC	SAPJ	PA13	H
C1	I	FBUS	BMC	SAPJ	PA14	H
C2	I	P.S.	BMC		GND	
D1	I	FBUS	BMC	DAPB	BAMX03	H
D2	I	FBUS	BMC	DAPD	BAMX02	H
E1	I	CPUC	BMC	UBCC	MEM BUS C0	L
E2	I	CPUC	BMC	UBCC	MEM BUS C1	L
F1	O	BMC	CPUC	BMC	MEM	L
F2	I	BUSB	BMC	BUSB	A02	L
H1						
H2	I	BUSB	BMC	BUSB	A13	L
J1	I	BUSB	BMC	BUSB	A03	L
J2	I	BUSB	BMC	BUSB	A14	L
K1	I	BUSB	BMC	BUSB	A17	L
K2	I	BUSB	BMC	BUSB	MSYNC	L
L1	I	BUSB	BMC	BUSB	A15	L
L2	I	BUSB	BMC	BUSB	A16	L
M1	I	BUSB	BMC	BUSB	A06	L
M2						
N1						
N2	I	P.S.	BMC		GND	
P1	O	BMC	CPUC	BMC	PERF	L
P2	I	FBUS	BMC	SAPJ	PA15	H
R1	O	BMC	CPUC	BMC	PE HALT	L
R2						
S1	I	BUSB	BMC	BUSB	A11	L
S2						
T1	I	P.S.	BMC		GND	
T2						
U1	I	BUSB	BMC	BUSB	A12	L
U2						
V1	I	P.S.	BMC		+5V	
V2						

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR D | SHEET 5 OF 7 | MODEL NUMBER

FABRI-TEK

DRAWN

CHECKED

APPROVED

PRODUCT | DATE

TITLE

BUFFER MATRIX CONTROL

CONNECTOR CHART

PART NUMBER 082-2996-00

REV. A

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PIN	I/O	FROM	TO	SIGNAL	TITLE	H/L
A1	I	BUSB	BMC	BUSB	A10	L
A2	I	P.S.	BMC		+5V	
B1	I	BUSB	BMC	BUSB	A09	L
B2	I	P.S.	BMC		-15V	
C1	I	BUSB	BMC	BUSB	A07	L
C2	I	P.S.	BMC		GND	
D1	I	BUSB	BMC	BUSB	A05	L
D2	O	BMC	FBUS	BMC	MEM D06	H
E1	I	BUSB	BMC	BUSB	A04	L
E2	I	FBUS	BMC	DAPB	BAMX 01	H
F1	O	BMC	FBUS	BMC	MEM D08	H
F2						
H1						
H2	O	BMC	FBUS	BMC	MEM D09	H
J1	O	BMC	FBUS	BMC	MEM D05	H
J2	O	BMC	FBUS	BMC	MEM D03	H
K1	O	BMC	FBUS	BMC	MEM D04	H
K2						
L1	I	FBUS	BMC	SAPJ	PA09	H
L2	I	FBUS	BMC	DAPB	BAMX 00	H
M1	I	FBUS	BMC	SAPJ	PA 11	H
M2	I	FBUS	BMC	SAPJ	PA10	H
N1	I	FBUS	BMC	SAPJ	PA12	H
N2	I	P.S.	BMC		GND	
P1	I	FBUS	BMC	DAPB	BAMX 04	H
P2	O	BMC	FBUS	BMC	MEM D01	H
R1	I	FBUS	BMC	SAPJ	PA06	H
R2						
S1	I	FBUS	BMC	SAPJ	PA07	H
S2	I	FBUS	BMC	DAPB	BAMX05	H
T1	I	P.S.	BMC			H
T2	I	FBUS	BMC	SAPJ	PA08	H
U1	I	BMM	BMC	BMM	MEM SA13	H
U2						
V1	I	P.S.	BMC		+5V	
V2						

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR E | SHEET 6 OF 7 | MODEL NUMBER

DRAWN

CHECKED

APPROVED

PRODUCT | DATE

FABRI-TEK

TITLE

BUFFER MATRIX CONTROL

CONNECTOR CHART

PART NUMBER 082-2996-00

REV. A

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PIN	I/O	FROM	TO	SIGNAL	TITLE	H/L
A1	I	BMM	BMC	BMM	MEM SA14	H
A2	I	P.S.	BMC		+5V	
B1	I	BMM	BMC	BMM	MEM SA02	H
B2	I	BMM	BMC	BMM	MEM SA03	H
C1						
C2	I	P.S.	BMC		GND	
D1	I	BMM	BMC	BMM	MEM SA04	H
D2	I	FBUS	BMC	SAPJ	PA16	H
E1	I	BMM	BMC	BMM	MEM SA15	H
E2	O	BMC	FBUS	BMC	MEM D07	H
F1	I	BMM	BMC	BMM	MEM SA17	H
F2	I	BMM	BMC	BMM	MEM SA01	H
H1	I	BUSB	BMC	BUSB	DCLO	L
H2	I	BMM	BMC	BMM	MEM SA00	H
J1	I	BMM	BMC	BMM	MEM SA12	H
J2	I	BMM	BMC	BMM	MEM SA16	H
K1	I	BMM	BMC	BMM	MEM SA07	H
K2	I	BMM	BMC	BMM	MEM SA11	H
L1	I	BMM	BMC	BMM	MEM SA10	H
L2	I	BMM	BMC	BMM	MEM SA06	H
M1	I	BMM	BMC	BMM	MEM SA05	H
M2	I	BMM	BMC	BMM	MEM SA09	H
N1	I	BMM	BMC	BMM	MEM SA08	H
N2	I	P.S.	BMC		GND	
P1	O	BMC	FBUS	BMC	MEM D15	H
P2	I	FBUS	BMC	SAPJ	PA17	H
R1	O	BMC	FBUS	BMC	MEM D14	H
R2	O	BMC	FBUS	BMC	MEM D00	H
S1	O	BMC	FBUS	BMC	MEM D10	H
S2	O	BMC	FBUS	BMC	MEM D02	H
T1	I	P.S.	BMC		GND	
T2	O	BMC	FBUS	BMC	MEM D12	H
U1	O	BMC	FBUS	BMC	MEM D11	H
U2	O	BMC	FBUS	BMC	MEM D13	H
V1	I	P.S.	BMC		+5V	
V2	I	BUSA	BMC	BUSA	DCLO	L

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR F	SHEET 7 OF 7	MODEL NUMBER .	
	DRAWN	FABRI-TEK	
	CHECKED	TITLE BUFFER MATRIX CONTROL CONNECTOR CHART	PART NUMBER 082-2996-00 / REV. A
	APPROVED		
PRODUCT	DATE		

Form 607 7-70

SYM	DESCRIPTION	DATE	APPR
00A	EC 20703 REL MAND.	8-16-74	

SHEET	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	
REVISION																												
SHEET	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	
REVISION																												
SHEET	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	
REVISION																												
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
REVISION	A	A	A	A	A	A	A																					

REVISION INDEX

PREPARED

CHECKED

APPROVED Ronald N. Monroe

DATE 26 June 74

SHEET 1 OF 7

USED ON 190-1666-00

FABRI-TEK

TITLE (BMM)

BUFFER MEMORY
MATRIX
CONNECTOR CHART

PART NUMBER

082-2997-00

PIN	I/O	FROM	TO	SIGNAL	TITLE	H/L
A1	I	BMC	BMM	BMC	MEM DATA 06	H
A2	I	PS			+5V	
B1	I	BMC	BMM	BMC	MEM DATA 08	H
B2						
C1	I	BMC	BMM	BMC	MEM DATA 11	H
C2	I	PS			GND	
D1	I	BMC	BMM	BMC	MEM DATA 07	H
D2	I	BMC	BMM	BMC	MEM DATA 02	H
E1	I	BMC	BMM	BMC	MEM DATA 17	H
E2	I	BMC	BMM	BMC	MEM DATA 03	H
F1	I	BMC	BMM	BMC	MEM DATA 13	H
F2	I	BMC	BMM	BMC	MEM DATA 01	H
H1						
H2	I	BMC	BMM	BMC	MEM DATA 15	H
J1	I	BMC	BMM	BMC	MEM DATA 04	H
J2	I	BMC	BMM	BMC	MEM DATA 14	H
K1	I	BMC	BMM	BMC	MEM DATA 12	H
K2	I	BMC	BMM	BMC	MEM DATA 00	H
L1	I	BMC	BMM	BMC	MEM DATA 16	H
L2						
M1	I	BMC	BMM	BMC	MEM DATA 10	H
M2						
N1	I	BMC	BMM	BMC	MEM DATA 09	H
N2	I	PS			GND	
P1	I	BMC	BMM	BMC	MEM DATA 05	H
P2						
R1						
R2						
S1	I	BMC	BMM	BMC	WRITE PULSE HIGH	L
S2	I	BMC	BMM	BMC	WRITE PULSE LOW	L
T1	I	PS			GND	
T2						
U1	I	BMC	BMM	BMC	CENABLE	L
U2						
V1	I	PS			+5V	
V2						

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR	SHEET	MODEL NUMBER
A	2 OF 7	190-1666-00

	DRAWN	(BMM) FABRI-TEK	
	CHECKED	TITLE BUFFER MEMORY MATRIX	PART NUMBER
	APPROVED	CONNECTOR CHART	082-2997-00
PRODUCT	DATE		REV. 00 -A

Form 607 7-70

PIN	I/O	FROM	TO	SIGNAL TITLE	H/L
A1					
A2	I	PS		+5V	
B1					
B2					
C1					
C2	I	PS		GND	
D1					
D2					
E1	I	BMC BMM	BMC	MAD 02	H
E2	I	BMC BMM	BMC	MAD 01	H
F1					
F2					
H1					
H2					
J1					
J2					
K1					
K2					
L1					
L2					
M1					
M2					
N1					
N2	I	PS		GND	
P1					
P2					
R1					
R2					
S1					
S2					
T1	I	PS		GND	
T2					
U1					
U2					
V1	I	PS		+5V	
V2					

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR B | SHEET 3 OF 7 | MODEL NUMBER 190-1666-00

DRAWN

CHECKED

APPROVED

PRODUCT | DATE

(BMM) FABRI-TEK

TITLE BUFFER MEMORY MATRIX

CONNECTOR CHART

PART NUMBER 082-2997-00

REV. 00 A

Form 607 7-70

PIN	I/O	FROM	TO	SIGNAL TITLE	H/L
A1					
A2	I	PS		+5V	
B1					
B2					
C1					
C2	I	PS		GND	
D1	I	BMC	BMM	BMC MAD 05	H
D2					
E1	I	BMC	BMM	BMC MTRX 2 SEL	L
E2					
F1					
F2					
H1					
H2					
J1					
J2					
K1	I	BMC	BMM	BMC MAD 04	H
K2					
L1	I	BMC	BMM	BMC QTR K SEL	H
L2					
M1	I	BMC	BMM	BMC MAD 08	H
M2					
N1	I	BMC	BMM	BMC MAD 03	H
N2	I	PS		GND	
P1	I	BMC	BMM	BMC MAD 07	H
P2					
R1	I	BMC	BMM	BMC MAD 06	H
R2					
S1	I	BMC	BMM	BMC MTRX 1 SEL	L
S2					
T1	I	PS		GND	
T2					
U1					
U2					
V1	I	PS		+5V	
V2					

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR C | SHEET 4 OF 7 | MODEL NUMBER 190-1666-00

DRAWN

CHECKED

APPROVED

PRODUCT | DATE

(BMM) FABRI-TEK

TITLE BUFFER MEMORY MATRIX

CONNECTOR CHART

PART NUMBER 082-2997-00

REV. 00 A

Form 607 7-70

PIN	I/O	FROM	TO	SIGNAL TITLE	H/L
A1					
A2	I	PS		+5V	
B1					
B2					
C1					
C2	I	PS		GND	
D1					
D2					
E1					
E2					
F1					
F2					
H1					
H2					
J1					
J2					
K1					
K2					
L1					
L2					
M1					
M2					
N1					
N2	I	PS		GND	
P1					
P2					
R1					
R2					
S1					
S2					
T1	I	PS		GND	
T2					
U1					
U2					
V1	I	PS		+5V	
V2					

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR	SHEET	MODEL NUMBER
D	5 OF 7	190-1666-00

DRAWN (BMM)

CHECKED

APPROVED

PRODUCT

DATE

FABRI-TEK

TITLE

BUFFER MEMORY MATRIX

CONNECTOR CHART

PART NUMBER 082-2997-00

REV. 00 A

Form 607 7-70

PIN	I/O	FROM	TO	SIGNAL TITLE	H/L
A1					
A2	I	PS		+5V	
B1					
B2					
C1					
C2	I	PS		GND	
D1					
D2					
E1					
E2					
F1					
F2					
H1					
H2					
J1					
J2					
K1					
K2					
L1					
L2					
M1					
M2					
N1					
N2	I	PS		GND	
P1					
P2					
R1					
R2					
S1					
S2					
T1	I	PS		GND	
T2					
U1	O	BMM	BMC	BMM MEM SA 13	H
U2					
V1	I	PS		+5V	
V2					

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR E | SHEET 6 OF 7 | MODEL NUMBER 190-1666-00

DRAWN

CHECKED

APPROVED

PRODUCT | DATE

(BMM) FABRI-TEK

TITLE BUFFER MEMORY MATRIX

CONNECTOR CHART

PART NUMBER 082-2997-00

REV. 00 A

Form 607 7-70

PIN	I/O	FROM	TO	SIGNAL	TITLE	H/L
A1	O	BMM	BMC	BMM	MEM SA 14	H
A2	I	PS			+5V	
B1	O	BMM	BMC	BMM	MEM SA 02	H
B2	O	BMM	BMC	BMM	MEM SA 03	H
C1						
C2	I	PS			GND	
D1	O	BMM	BMC	BMM	MEM SA 04	H
D2						
E1	O	BMM	BMC	BMM	MEM SA 15	H
E2						
F1	O	BMM	BMC	BMM	MEM SA 17	H
F2	O	BMM	BMC	BMM	MEM SA 01	H
H1						
H2	O	BMM	BMC	BMM	MEM SA 00	H
J1	O	BMM	BMC	BMM	MEM SA 12	H
J2	O	BMM	BMC	BMM	MEM SA 16	H
K1	O	BMM	BMC	BMM	MEM SA 07	H
K2	O	BMM	BMC	BMM	MEM SA 11	H
L1	O	BMM	BMC	BMM	MEM SA 10	H
L2	O	BMM	BMC	BMM	MEM SA 06	H
M1	O	BMM	BMC	BMM	MEM SA 05	H
M2	O	BMM	BMC	BMM	MEM SA 09	H
N1	O	BMM	BMC	BMM	MEM SA 08	H
N2	I	PS			GND	
P1						
P2						
R1						
R2						
S1						
S2						
T1	I	PS			GND	
T2						
U1						
U2						
V1	I	PS			+5V	
V2						

PIN	SIGNAL TITLE

MATES WITH

CONNECTOR F	SHEET 7 OF 7	MODEL NUMBER 190-1666-00
	DRAWN	(BMM) FABRI-TEK
	CHECKED	TITLE BUFFER MEMORY MATRIX CONNECTOR CHART
	APPROVED	PART NUMBER 082-2997-00
PRODUCT	DATE	REV. 00 A

Form 607 7-70

SYM	DESCRIPTION	DATE	APPR

SHEET	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	
REVISION																												
SHEET	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	
REVISION																												
SHEET	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	
REVISION																												
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
REVISION																												

REVISION INDEX

PREPARED

CHECKED R. N. Monroe

APPROVED R. N. Monroe

DATE 26 Sep 74

SHEET 1 OF 3

USED ON 190-1767-00

FABRI-TEK

TITLE

AUXILIARY BUFFER
MATRIX CONTROLLER
CONNECTOR CHART

PART NUMBER

082-3015-00

PIN	SIGNAL TITLE			PIN	SIGNAL TITLE
A1	BUSA	INIT	L		
A2	POWER (+5V)				
B1	BUSA	INTR	L		
B2	GROUND				
C1	BUSA	D00	L		
C2	GROUND				
D1	BUSA	D02	L		
D2	BUSA	D01	L		
E1	BUSA	D04	L		
E2	BUSA	D03	L		
F1	BUSA	D06	L		
F2	BUSA	D05	L		
H1	BUSA	D08	L		
H2	BUSA	D07	L		
J1	BUSA	D10	L		
J2	BUSA	D09	L		
K1	BUSA	D12	L		
K2	BUSA	D11	L		
L1	BUSA	D14	L		
L2	BUSA	D13	L		
M1	BUSA	PA	L		
M2	BUSA	D15	L		
N1	GROUND				
N2	BUSA	PB	L		
P1	GROUND				
P2	BUSA	BBSY	L		
R1	GROUND				
R2	BUSA	SACK	L		
S1	GROUND				
S2	BUSA	NPR	L		
T1	GROUND				
T2	BUSA	BR7	L		
U1	BUSA	NPG	H		
U2	BUSA	BR6	L		
V1	BUSA	BG7	H		
V2	GROUND				

MATES WITH

CONNECTOR A | SHEET 2 OF | MODEL NUMBER 4511 MEMORY BUFFER

DRAWN

CHECKED

APPROVED

PRODUCT

DATE 26 Sep 74

FABRI-TEK

TITLE AUXILIARY BUFFER
MATRIX CONTROLLER
CONNECTOR CHART

PART NUMBER 082-3015-00

REV.

Form 607 7-70

PIN	SIGNAL TITLE			PIN	SIGNAL TITLE
A1	BUSA	BG6	H		
A2	POWER (+5V)				
B1	BUSA	BG5	H		
B2	GROUND				
C1	BUSA	BR5	L		
C2	GROUND				
D1	GROUND				
D2	BUSA	BR4	L		
E1	GROUND				
E2	BUSA	BG4	H		
F1	BUSA	ACLO	L		
F2	BUSA	DCLO	L		
H1	BUSA	A01	L		
H2	BUSA	A00	L		
J1	BUSA	A03	L		
J2	BUSA	A02	L		
K1	BUSA	A05	L		
K2	BUSA	A04	L		
L1	BUSA	A07	L		
L2	BUSA	A06	L		
M1	BUSA	A09	L		
M2	BUSA	A08	L		
N1	BUSA	A11	L		
N2	BUSA	A10	L		
P1	BUSA	A13	L		
P2	BUSA	A12	L		
R1	BUSA	A15	L		
R2	BUSA	A14	L		
S1	BUSA	A17	L		
S2	BUSA	A16	L		
T1	GROUND				
T2	BUSA	C1	L		
U1	BUSA	SSYN	L		
U2	BUSA	C0	L		
V1	BUSA	MSYN	L		
V2	GROUND				

MATES WITH

CONNECTOR B | SHEET 3 OF 3 | MODEL NUMBER 4511 MEMORY BUFFER

FABRI-TEK

DRAWN

CHECKED

APPROVED

PRODUCT | DATE

TITLE AUXILIARY BUFFER
MATRIX CONTROLLER
CONNECTOR CHART

PART NUMBER 082-3015-00

REV.

Form 607 7-70

EC HIST 00A EC 20019

REVISION STATUS OF SHEETS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	00A	/	00A																				

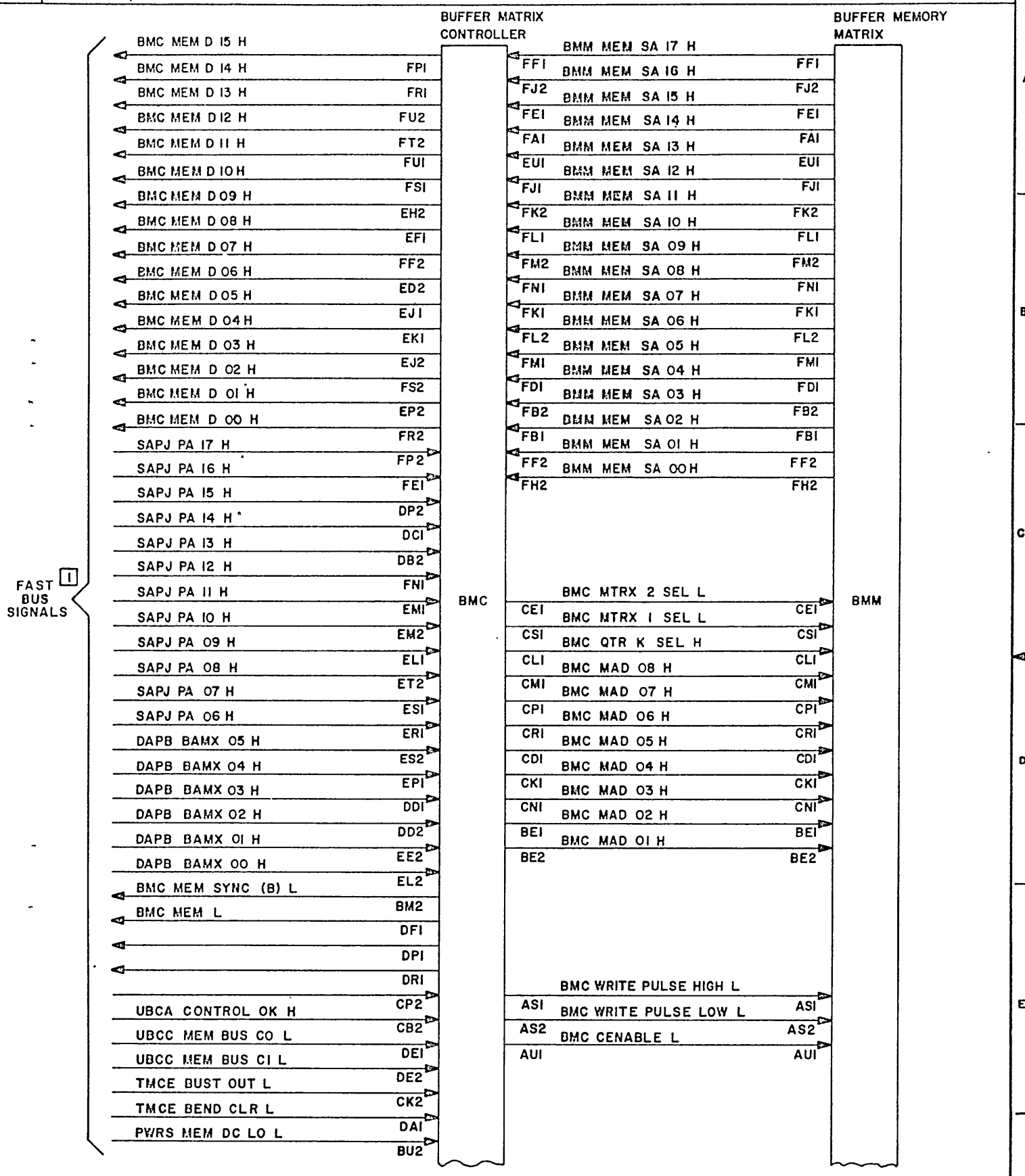
		DATE
DRAWN	C. CZAR	6-18-74
CHECKED		
APPROVED	[signature]	6 JUN 79

FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

TITLE LOGIC , MEMORY BUFFER

DWG NO	TYPE	VERS	PAGE
C 139-0004-17	960-0506-00		1 OF 3

E.C. 00A EC 20818
HIST.

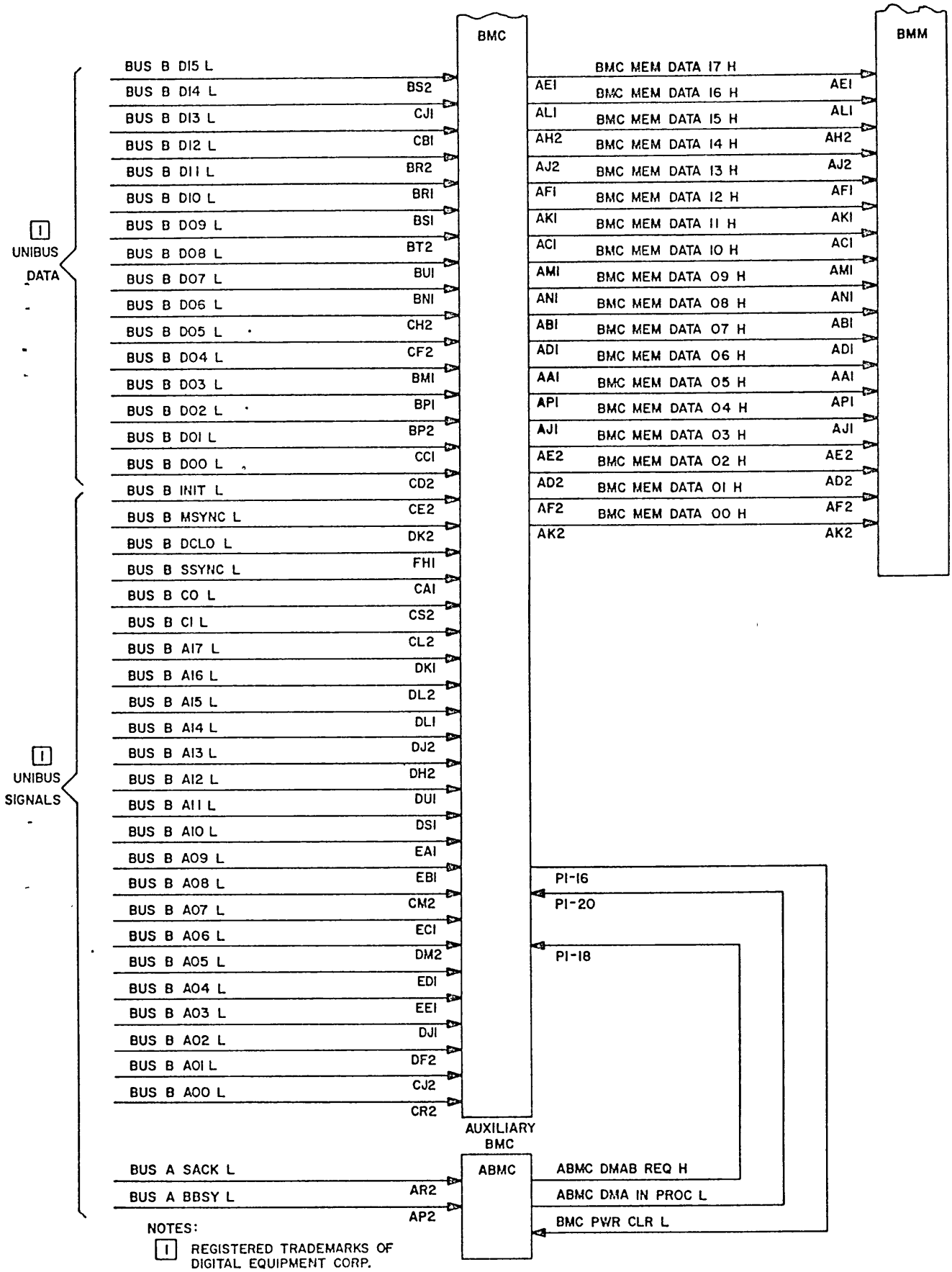


NOTES:

[1] REGISTERED TRADEMARKS OF DIGITAL EQUIPMENT CORP.

FABRI-TEK INC. MEMORY PRODUCTS DIVISION	TITLE: LOGIC , MEMORY BUFFER			
	DWG. NO.: C 139-0004-17	TYPE	VERS.	PAGE: 2

E.C.
HIST.



NOTES:

[1] REGISTERED TRADEMARKS OF DIGITAL EQUIPMENT CORP.

FABRITEK INC.
MEMORY PRODUCTS DIVISION

TITLE: LOGIC, MEMORY BUFFER

DWG NO.	TYPE	VERS.	PAGE
C 139-0004-17			3

EC HIST	00A EC 20818

NOTES. APPLICABLE THROUGHOUT THIS SCHEMATIC.

1 UNLESS OTHERWISE STATED.
- A RESISTANCE VALUES ARE IN OHMS RESISTORS ARE 5% TOLERANCE, 1/4 WATT.
- B. CAPACITANCE VALUES ARE IN MICROFARADS

2 JEDEC OR MANUFACTURER'S PART NUMBERS ARE FOR REFERENCE ONLY FOR EXPLICIT DESCRIPTION OF THE DEVICE CHARACTERISTICS, REFER TO THE FABRI-TEK SPECIFICATION FOR THE FABRI-TEK PART NUMBER.

REVISION STATUS OF SHEETS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
00A	/	/	00A	/	00A	/	/	/	/	/	00A	/	/	/							

	DATE
DRAWN CARL T. CZAR	7-2-74
CHECKED [illegible]	7-8-74
APPROVED [illegible]	19SEP74

FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

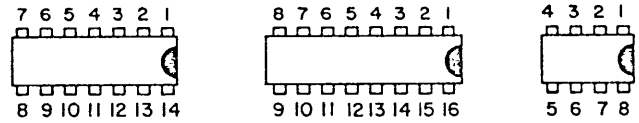
TITLE: SCHEMATIC, BUFFER MATRIX CONTROLLER

DWG NO	TYPE	VERS	PAGE
C 138-0019-62		190-1665-00	1 OF 15

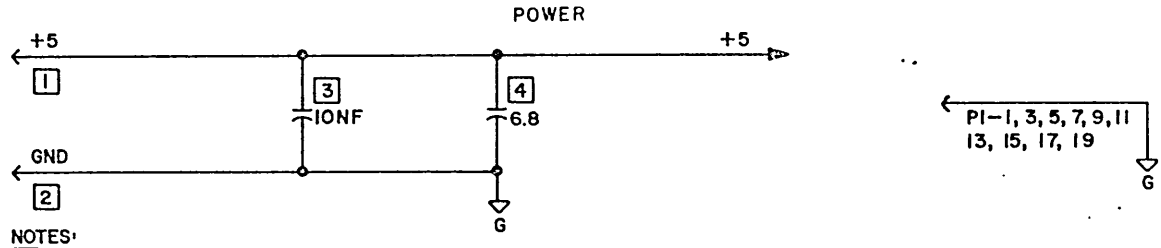
EC HIST

MODULE CODE TABLE

CODE	VENDOR	VENDORS P/N	DESCRIPTION	+5V	GND	TOTAL NO OF PINS
H00	T I	SN74H00	QUAD 2-IN POS NAND	14	7	14
S00	T I	SN74S00	QUAD 2-IN NAND	14	7	14
02	T I	SN7402	QUAD 2-IN NOR	14	7	14
S03	T I	SN74S03	QUAD 2-IN NAND OC	14	7	14
04	T I	SN7404	HEX INVERTER	14	7	14
S04	T I	SN74S04	HEX INVERTER	14	7	14
S10	T I	SN74S10	TRIPLE 3-IN NAND	14	7	14
S11	T I	SN74S11	TRIPLE 3-IN POS-AND	14	7	14
S20	T I	SN74S20	DUAL 4-IN NAND	14	7	14
S22	T I	SN74S22	DUAL 4-IN NAND OC	14	7	14
S37	T I	SN74S37	QUAD 2-IN NAND BFR	14	7	14
S40	T I	SN74S40	DUAL 4-IN NAND BFR	14	7	14
S74	T I	SN74S74	DUAL D-TYPE FLIP FLOP	14	7	14
85	T I	SN7485	4-BIT MAGNITUDE COMP	16	8	16
123	T I	SN74123	DUAL MONO MV W/CLEAR	16	8	16
S133	T I	SN74S133	13-IN NAND GATE	16	8	16
S157	T I	SN74S157	QUAD 2-1 LINE SEL	16	8	16
S158	T I	SN74S158	QUAD 2-1 LINE SEL	16	8	16
161	T I	SN74161	SYNCH 4-BIT COUNTER	16	8	16
180	T I	SN74180	O/E PARITY GENERATORS	14	7	14
3404	INTEL	C3404	6-BIT LATCH	16	8	16
3106A		C3106A	256-BIT BIP RAM	16	8	16
8836		DM8836	QUAD 2-IN NOR RCVR	8	1	14
S42		N82S42	QUAD 2-IN XNOR GATE	14	7	14



CODE	REF DESIG	OUTPUT TERMINAL NO
UNUSED MODULE ELEMENTS		

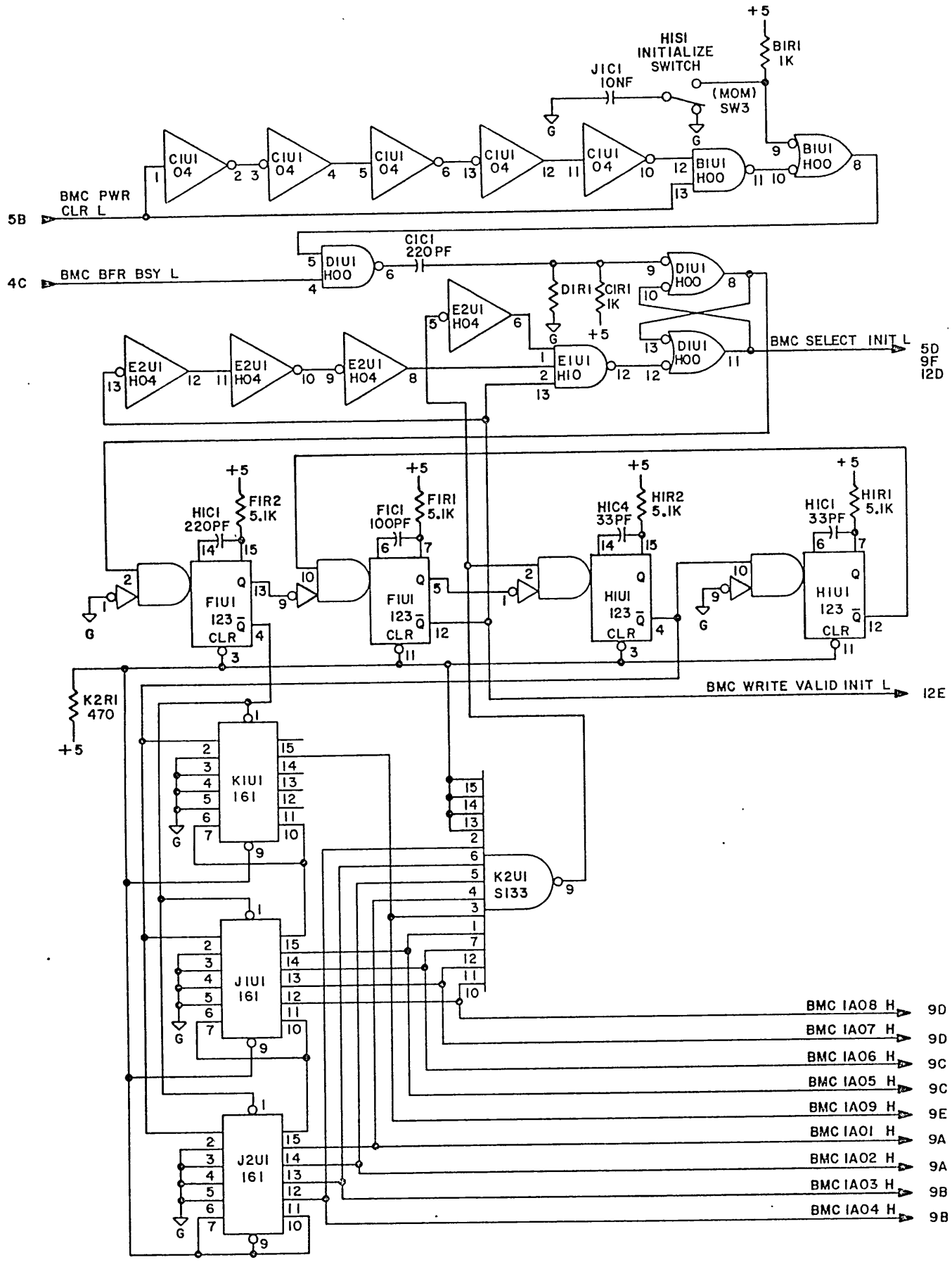


NOTES:

1. TYPICAL OF PIN AV1, BV1, CV1, DV1, EV1, FV1, AA2, BA2, CA2, DA2, EA2, FA2.
2. TYPICAL OF PIN AC2, BC2, CC2, DC2, EC2, FC2, AH1, BH1, CH1, DH1, EH1, FH1, AN2, BN2, CN2, DN2, EN2, FN2, AT1, BT1, CT1, DT1, ET1, FT1.
3. TYPICAL OF CAPACITOR A1C1, A2C1, A3C1, A4C1, B1C2, B2C1, B3C1, B4C1, C1C1, C2C1, C3C2, C4C1, D1C1, D2C1, D3C1, D4C1, E1C1, E2C1, E3C1, E4C2, F1C2, F2C2, F3C1, F4C1, H1C3, H2C1, H3C1, H4C1, J1C2, J2C1, J3C1, J4C1, K1C1, K2C1, K3C2, K4C2, L2C1, L3C1, L4C1, M1C1, M2C1, M3C1, M4C1, N1C1, N2C1, N3C1, N4C1, P1C2, P2C1, P3C1, P4C1, R1C1, R2C1, R3C1, R4C1, S1C1, S2C2, S3C1, S4C1, T1C1, T2C1, T3C1, T4C1, U1C1, U2C1, U3C1, U4C1, V1C1, V2C1, V3C1, V4C1, W1C1, W2C1, W3C2, W4C1, X1C2, X2C1, X3C1, X4C2, Y1C1, Y2C1, Y3C1, Y4C1, Z1C1, Z2C1, Z3C1, Z4C1.
4. TYPICAL OF CAPACITOR B1C1, P1C1, X1C1, F2C1, S2C1, C3C1, K3C1, W3C1, K4C1, X4C1, D5C1, N5C1, Z5C1.

FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

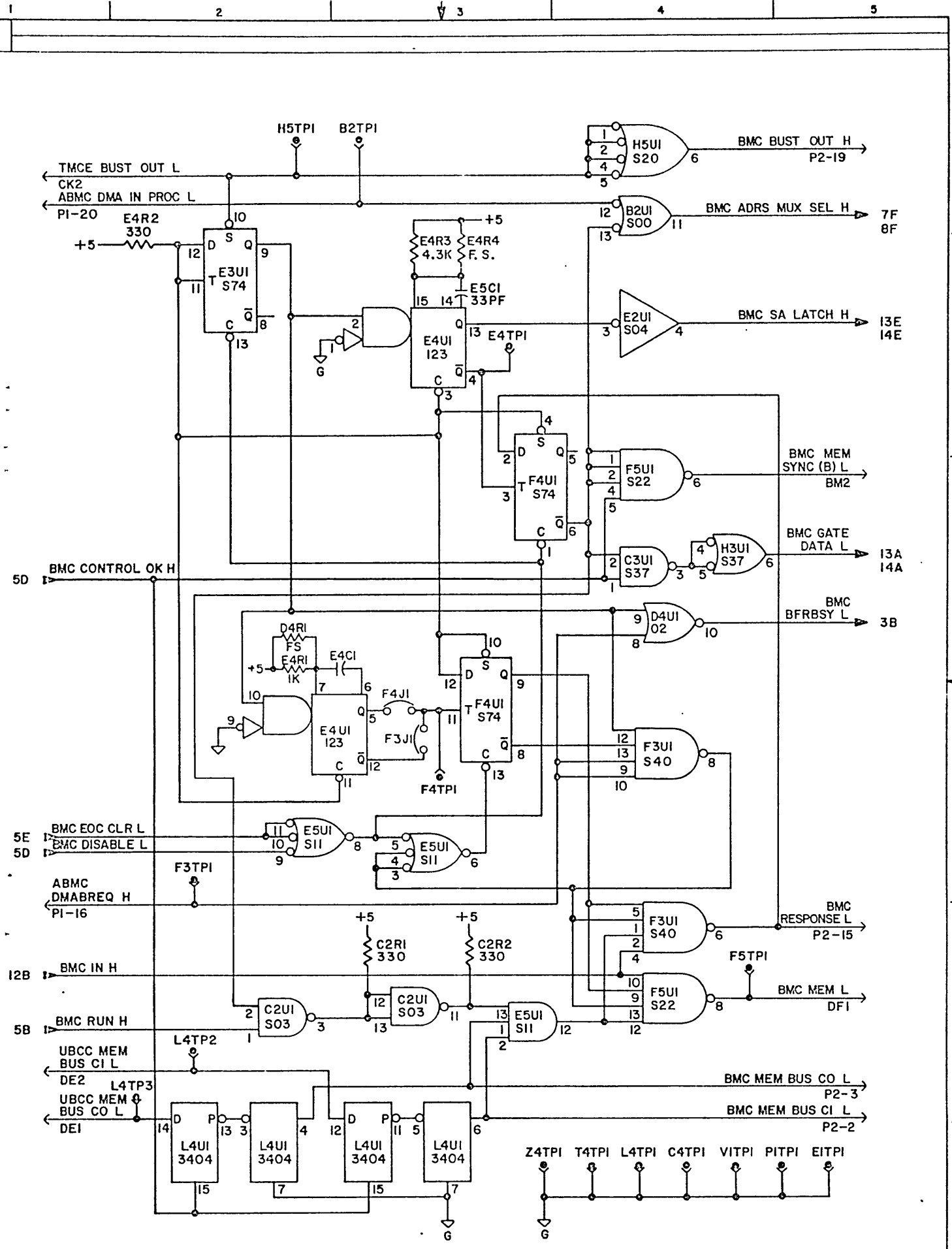
TITLE	SCHEMATIC, BUFFER MATRIX CONTROLLER			
DWG NO C	138-0019-62	TYPE	VERS	PAGE 2



FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

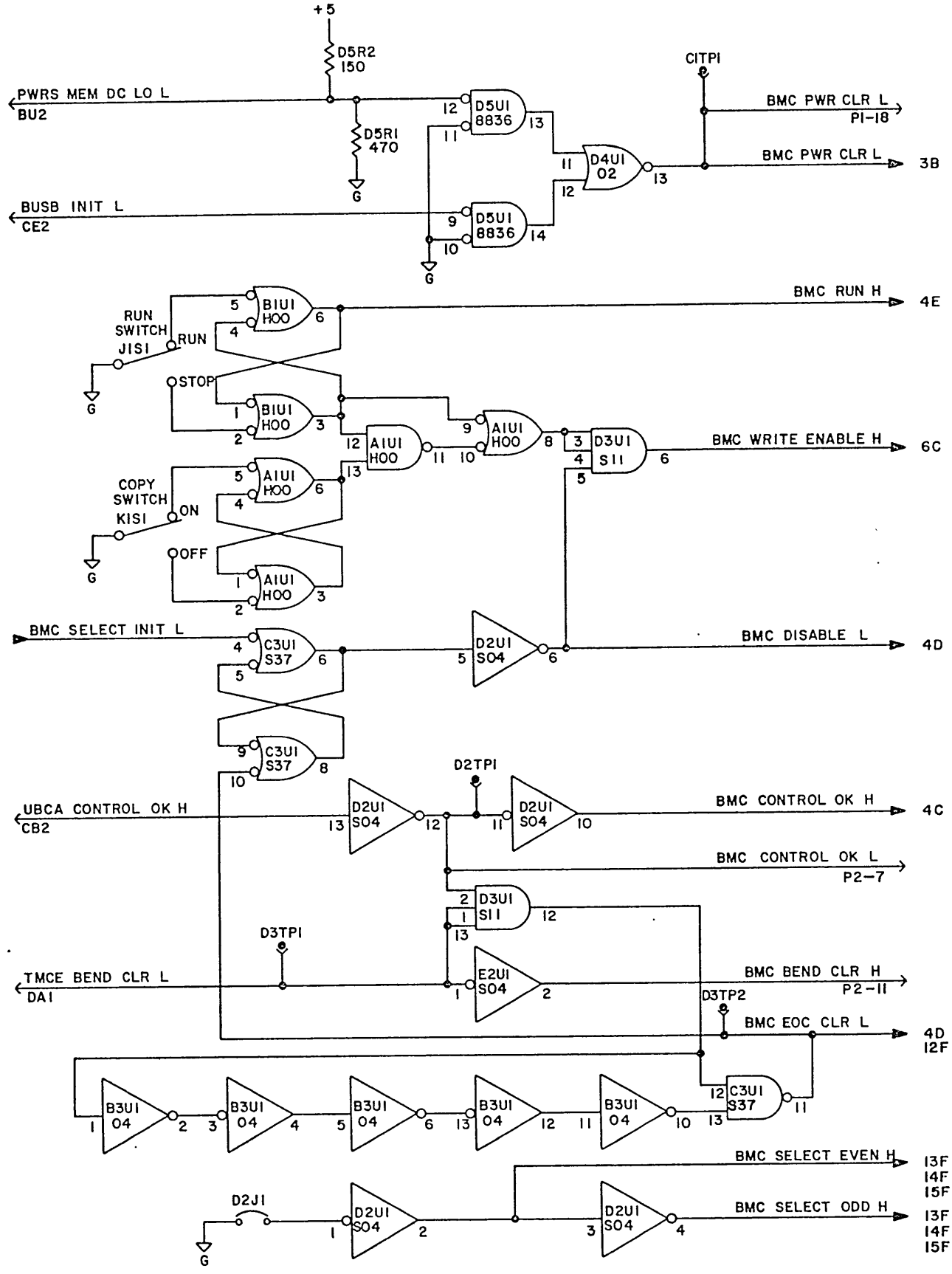
TITLE: SCHEMATIC, BUFFER MATRIX CONTROLLER

DWG. NO. C 138 -0019-62 | TYPE | VERS. | PAGE 3



FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

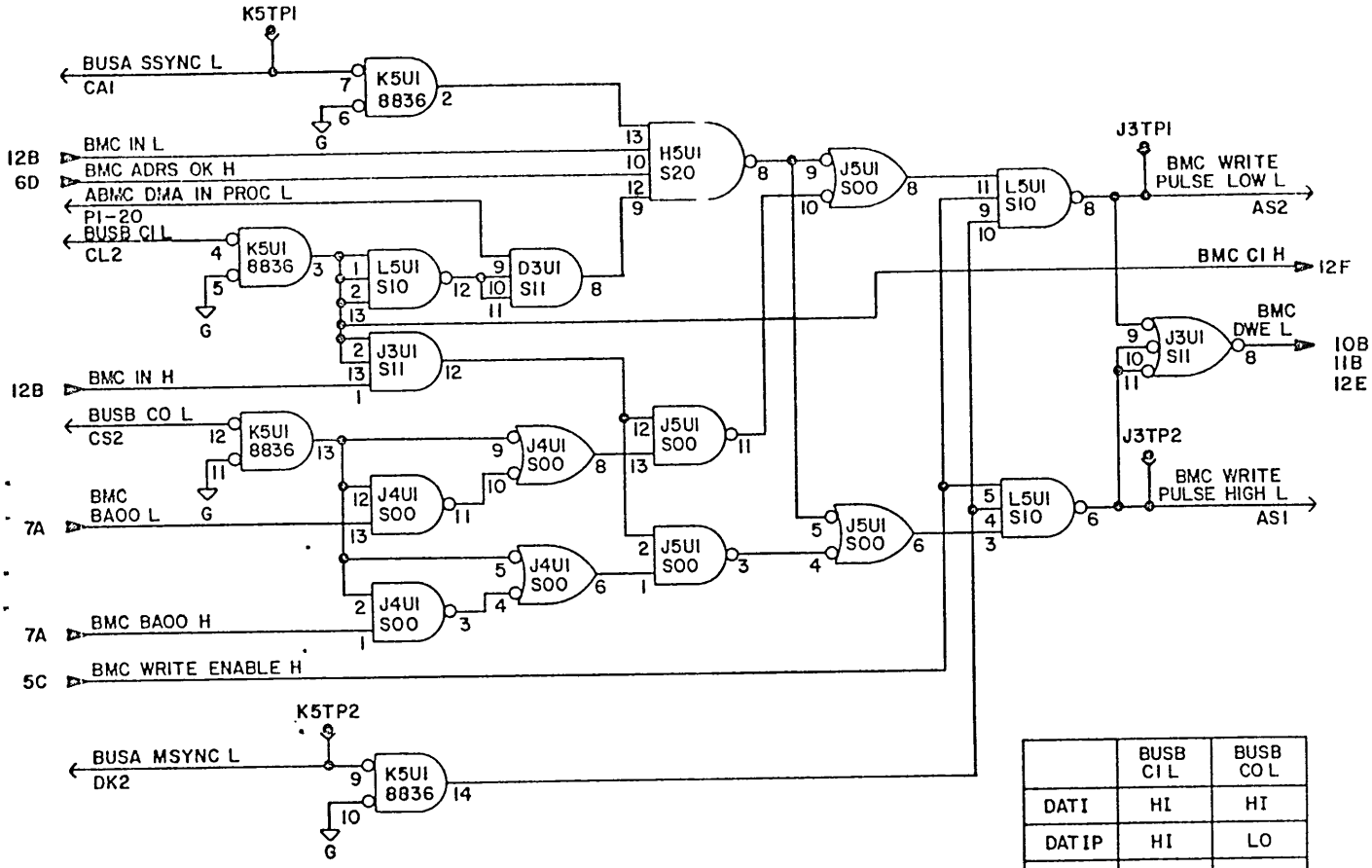
TITLE	SCHEMATIC, BUFFER MATRIX CONTROLLER			
DWG NO. C	138-0019-62	TYPE	VERS.	PAGE 4



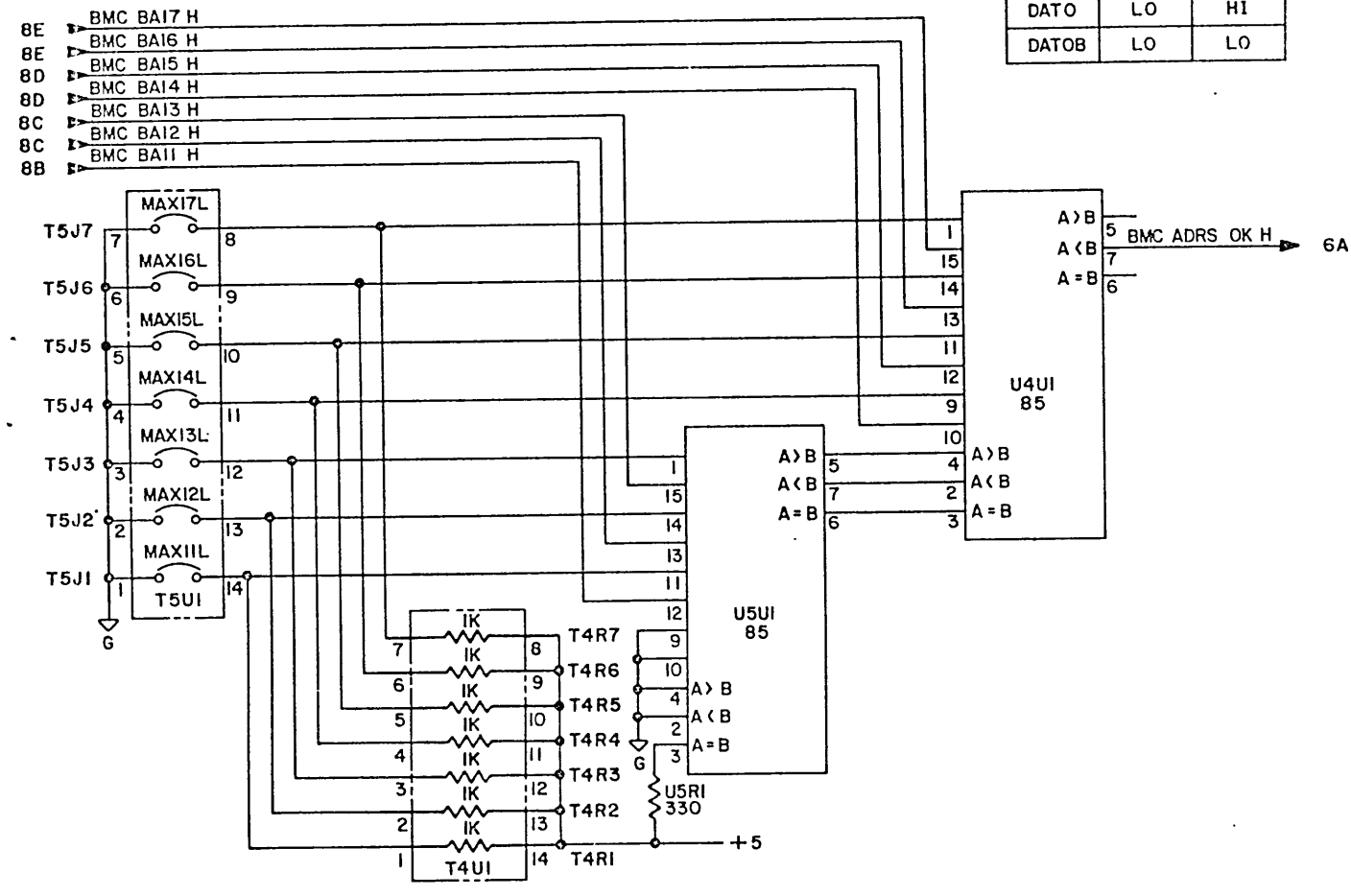
FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

TITLE: SCHEMATIC, BUFFER MATRIX CONTROLLER

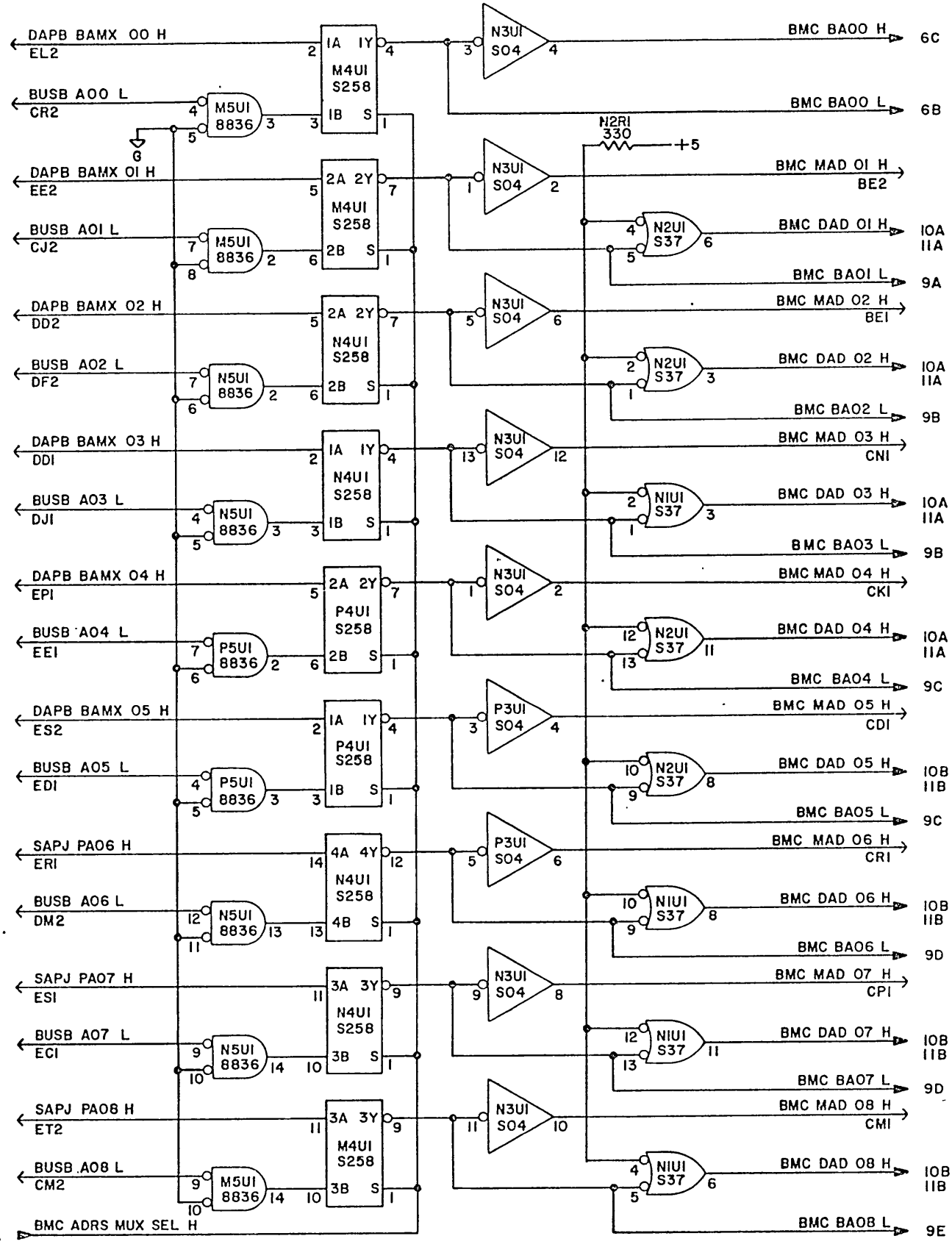
DWG NO.	TYPE	VERS.	PAGE
C 138-0019-62			5



	BUSB CI L	BUSB CO L
DATI	HI	HI
DATIP	HI	LO
DATO	LO	HI
DATOB	LO	LO



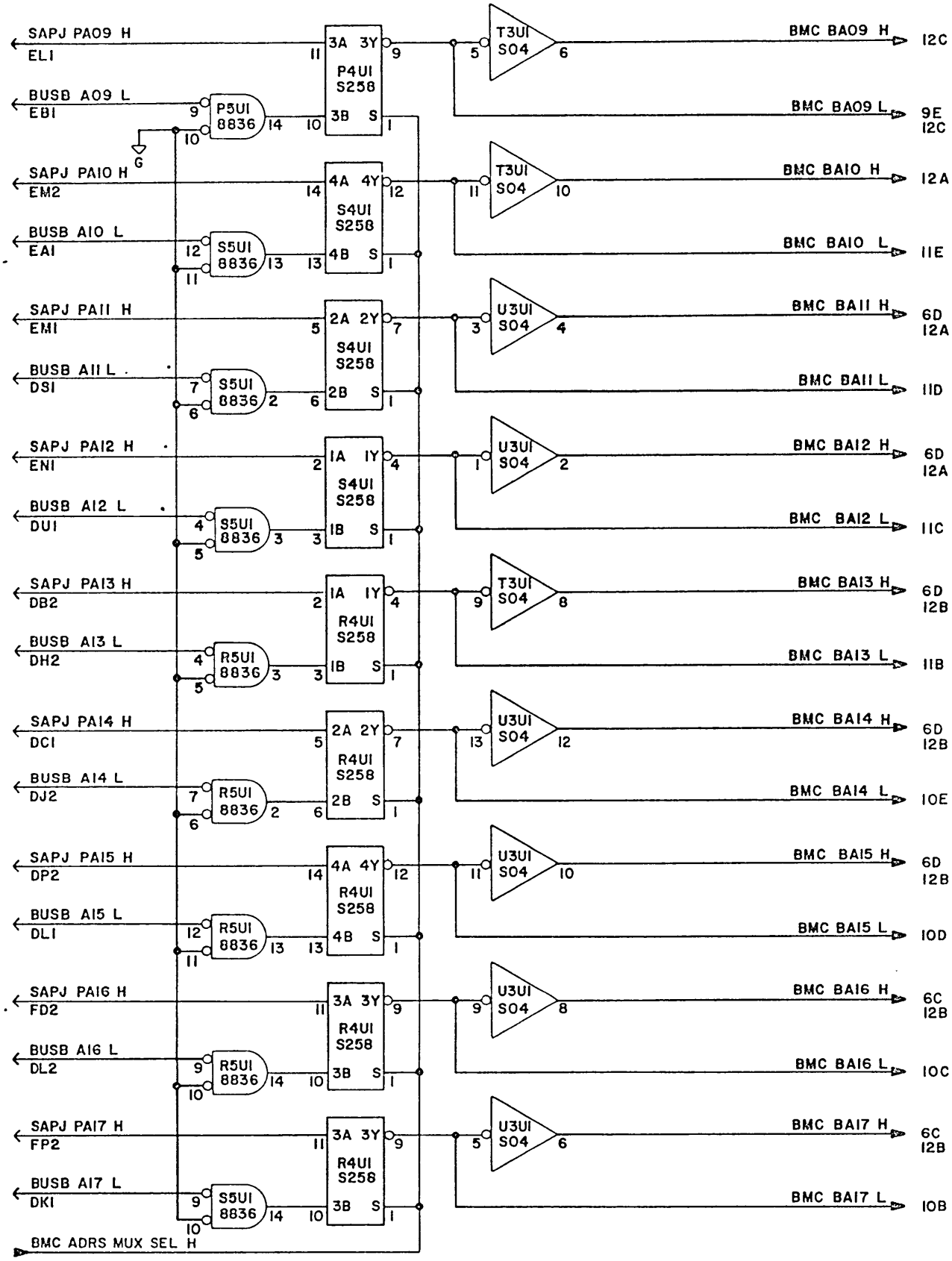
FABRI-TEK INC. MEMORY PRODUCTS DIVISION	TITLE	SCHEMATIC, BUFFER MATRIX CONTROLLER		
	DWG NO. C	138-0019-62	TYPE	VERS.
				PAGE 6



NOTE: PIN 15 (STROBE INPUT) TO EACH S258 IS GROUNDED.

FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

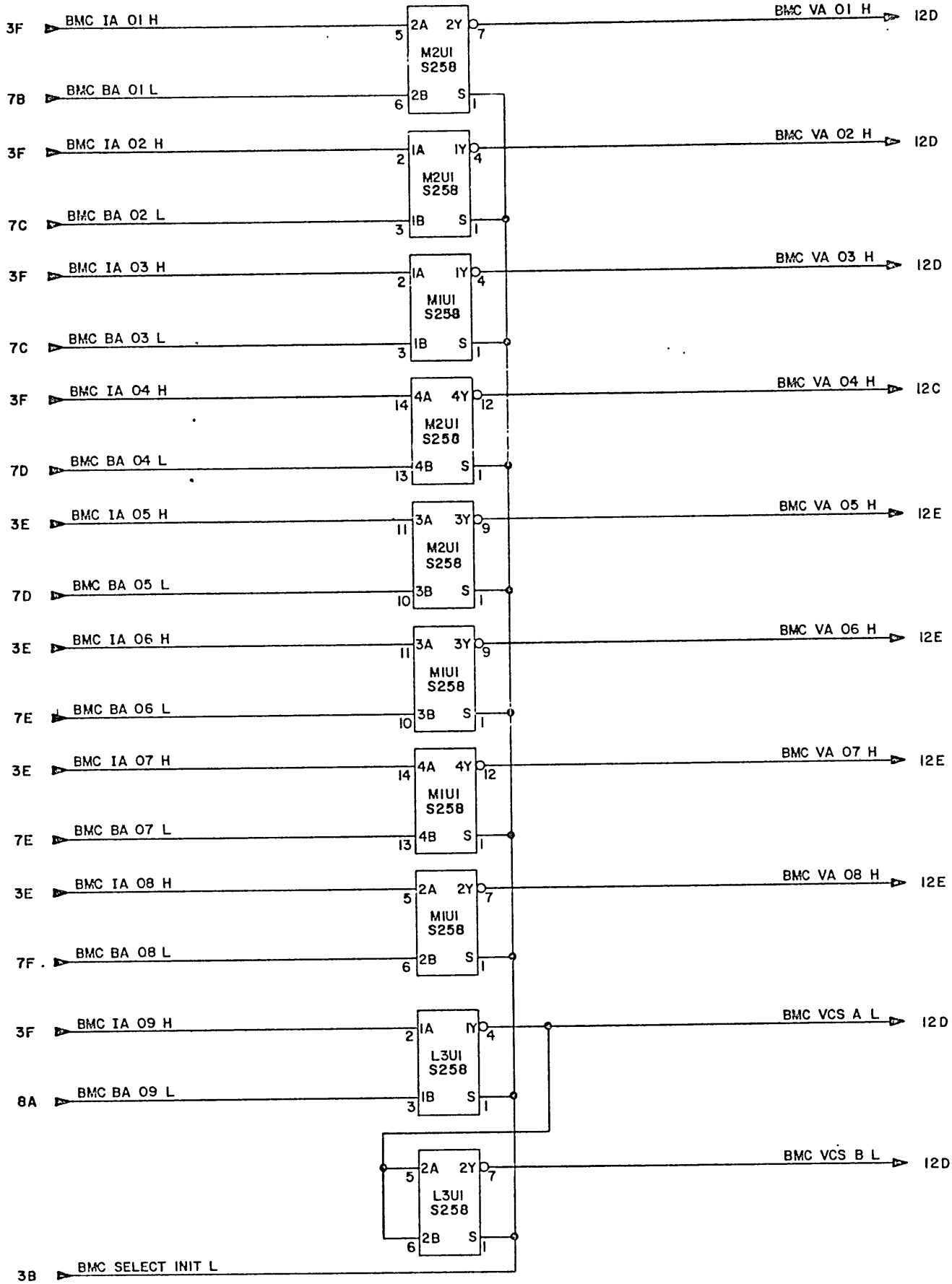
TITLE	SCHEMATIC, BUFFER MATRIX CONTROLLER			
DWG. NO. C 138-0019-62	TYPE	VERS.	PAGE 7	



NOTE: PIN 15 (STROBE INPUT) TO EACH S258 IS GROUNDED.

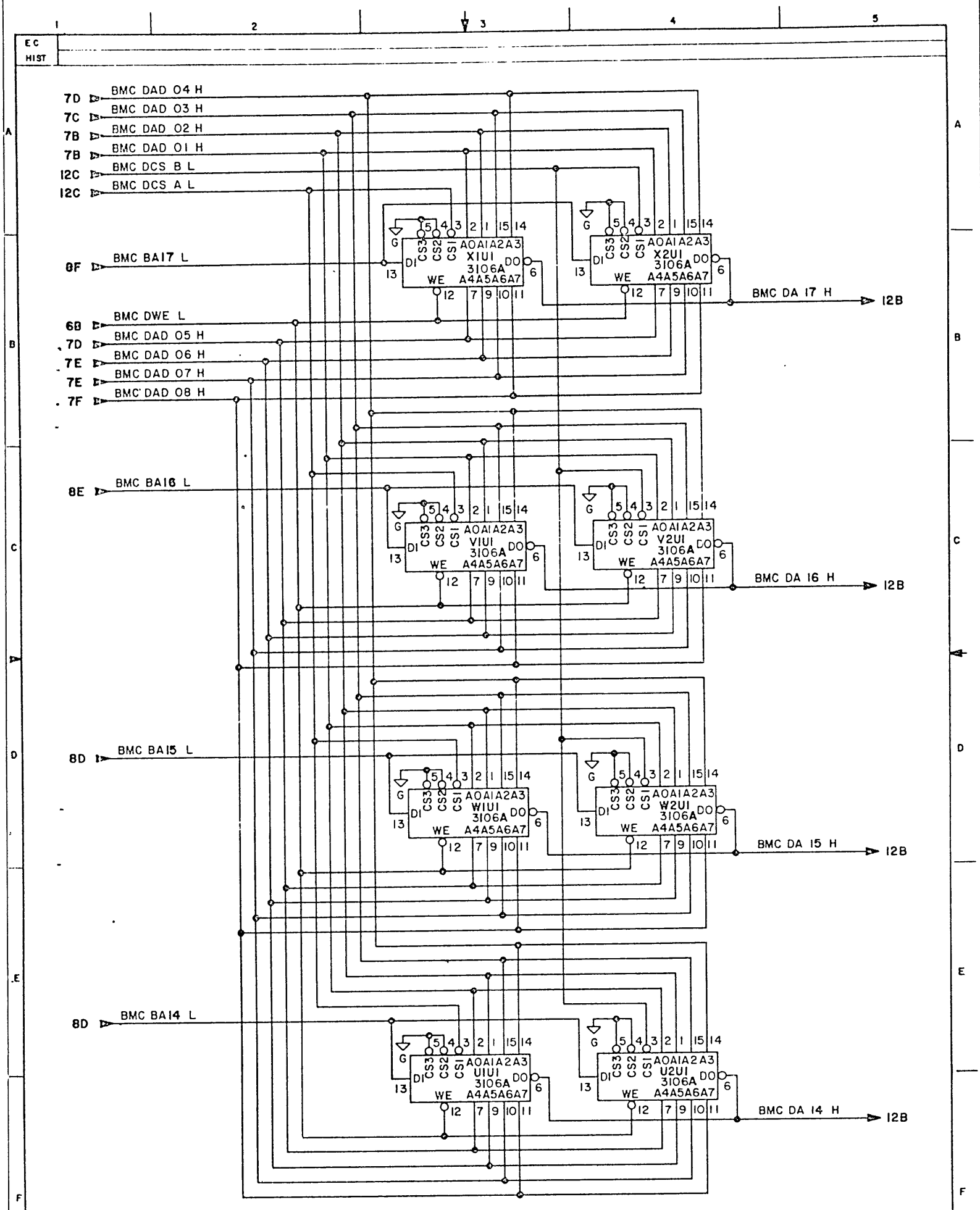
FABRITEK INC. MEMORY PRODUCTS DIVISION	TITLE SCHEMATIC, BUFFER MATRIX CONTROLLER				
	DWG. NO. C 138-0019-62	TYPE	VERS.	PAGE 8	

E.C.
HIST.



NOTE : PIN 15 (STROBE INPUT) TO EACH S256 IS GROUNDED.

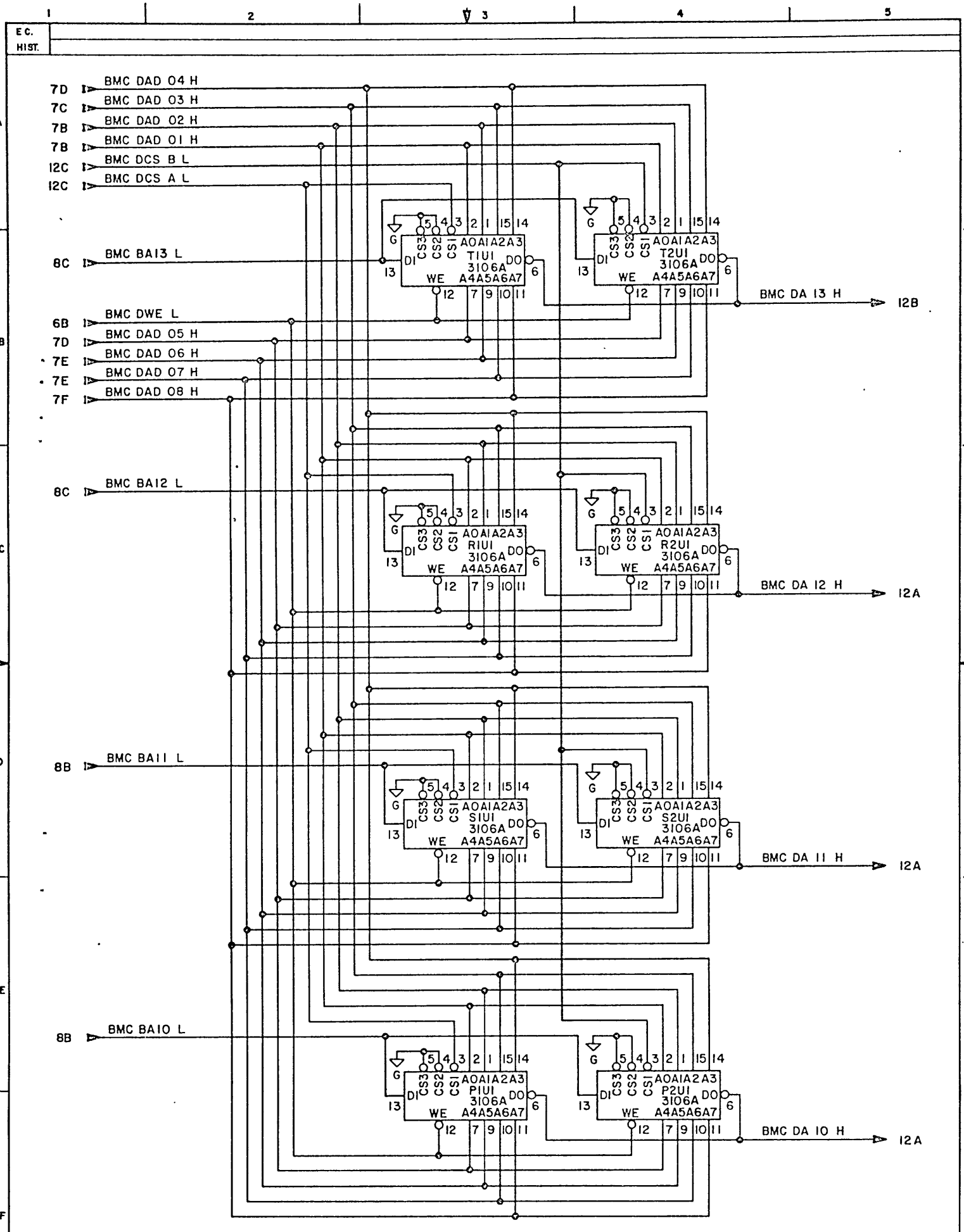
FABRITEK INC. MEMORY PRODUCTS DIVISION	TITLE: SCHEMATIC, BUFFER MATRIX CONTROLLER				
	DWG NO. C 138-0019-62	TYPE	VERS.	PAGE 9	



FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

TITLE SCHEMATIC, BUFFER MATRIX CONTROLLER

DWG NO.	TYPE	VERS	PAGE
C 138-0019-62			10

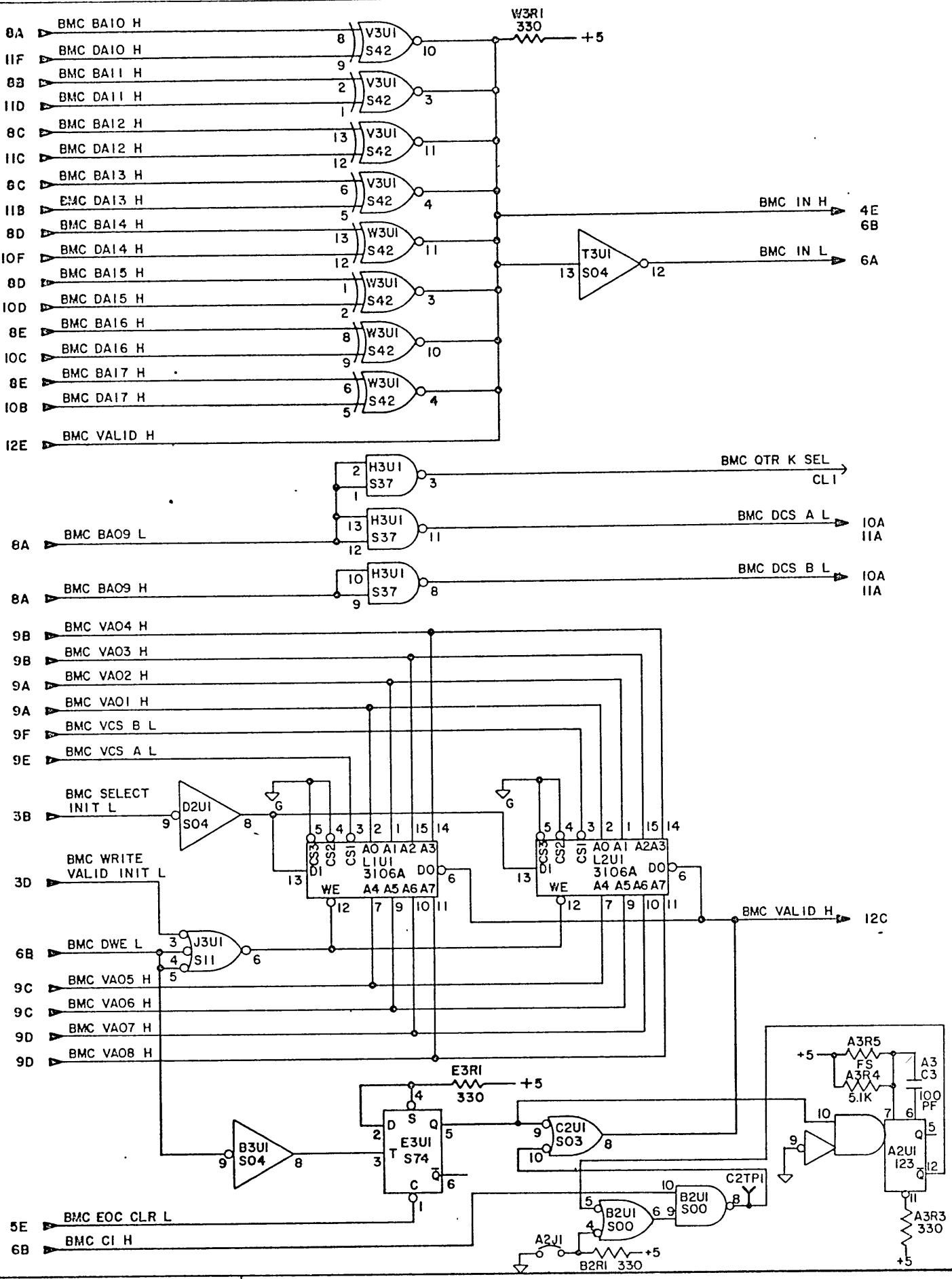


FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

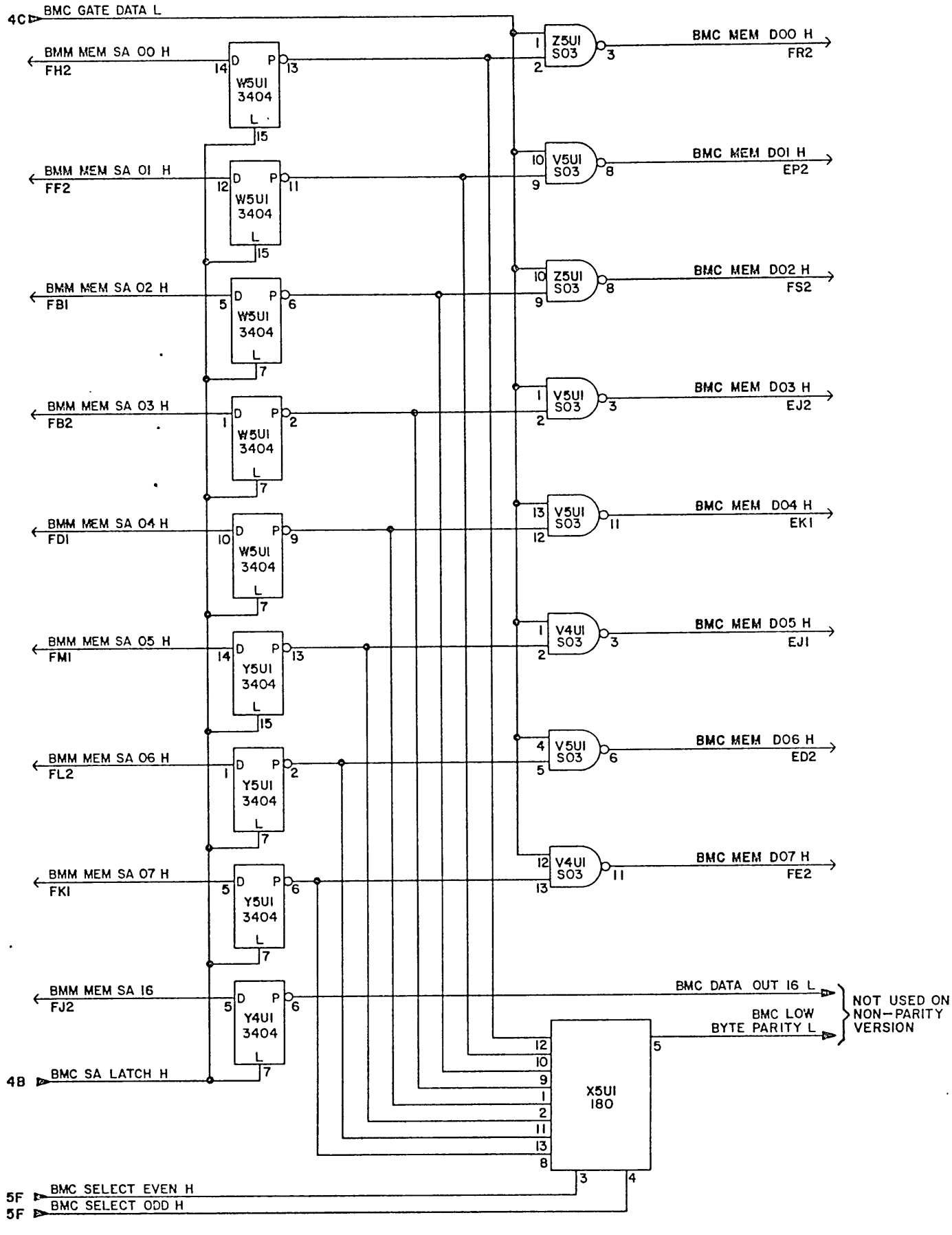
TITLE SCHEMATIC, BUFFER MATRIX CONTROLLER

DWG NO.	TYPE	VERS.	PAGE
C 138-0019-62			11

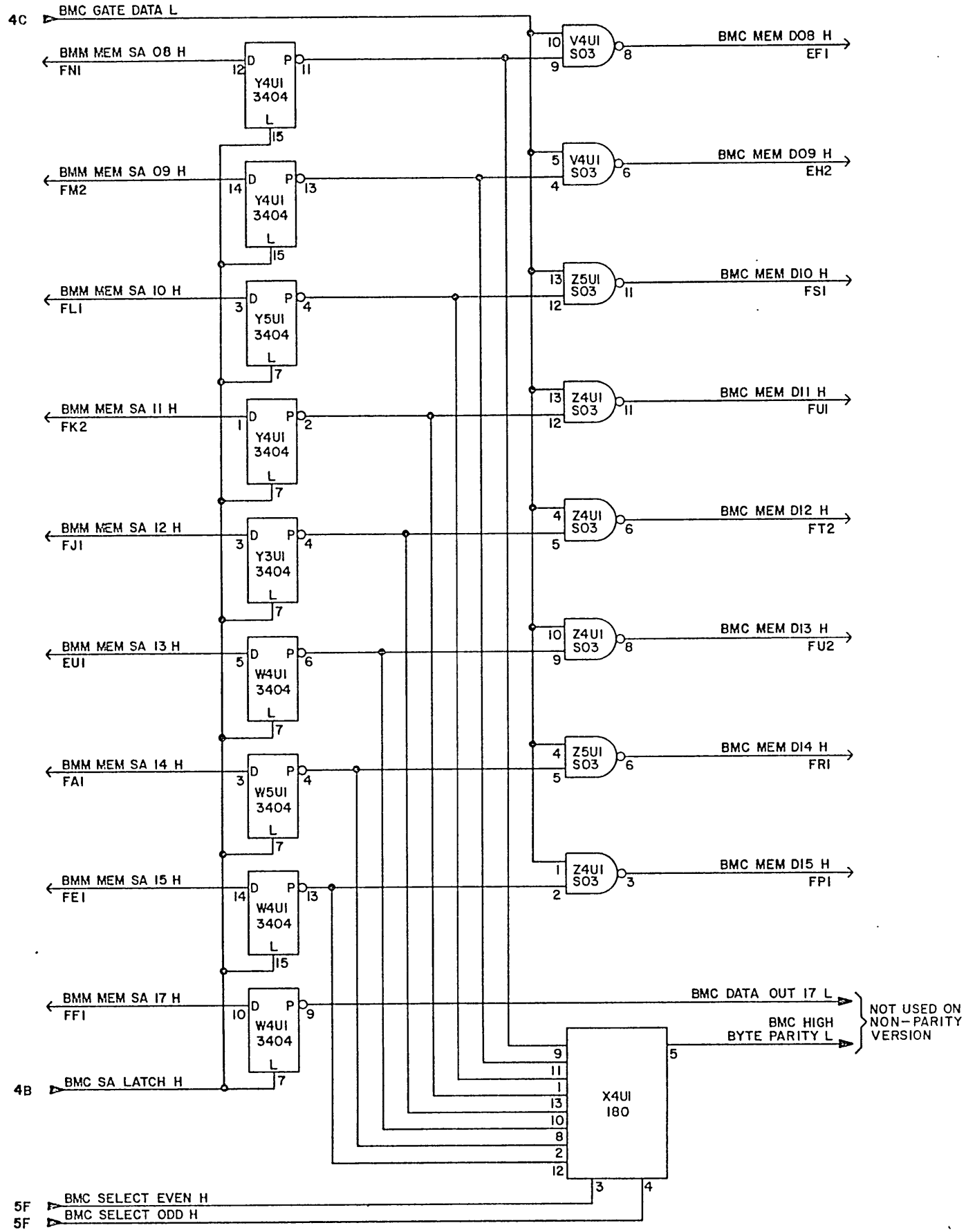
E.C.
HIST.



FABRITEK INC. MEMORY PRODUCTS DIVISION	TITLE SCHEMATIC, BUFFER MATRIX CONTROLLER				
	DWG. NO. C 138-0019-62	TYPE	VERS.	PAGE 12	



FABRI-TEK INC. MEMORY PRODUCTS DIVISION	TITLE	SCHEMATIC, BUFFER MATRIX CONTROLLER			
	DWG NO C	138-0019-62	TYPE	VERS	PAGE 13



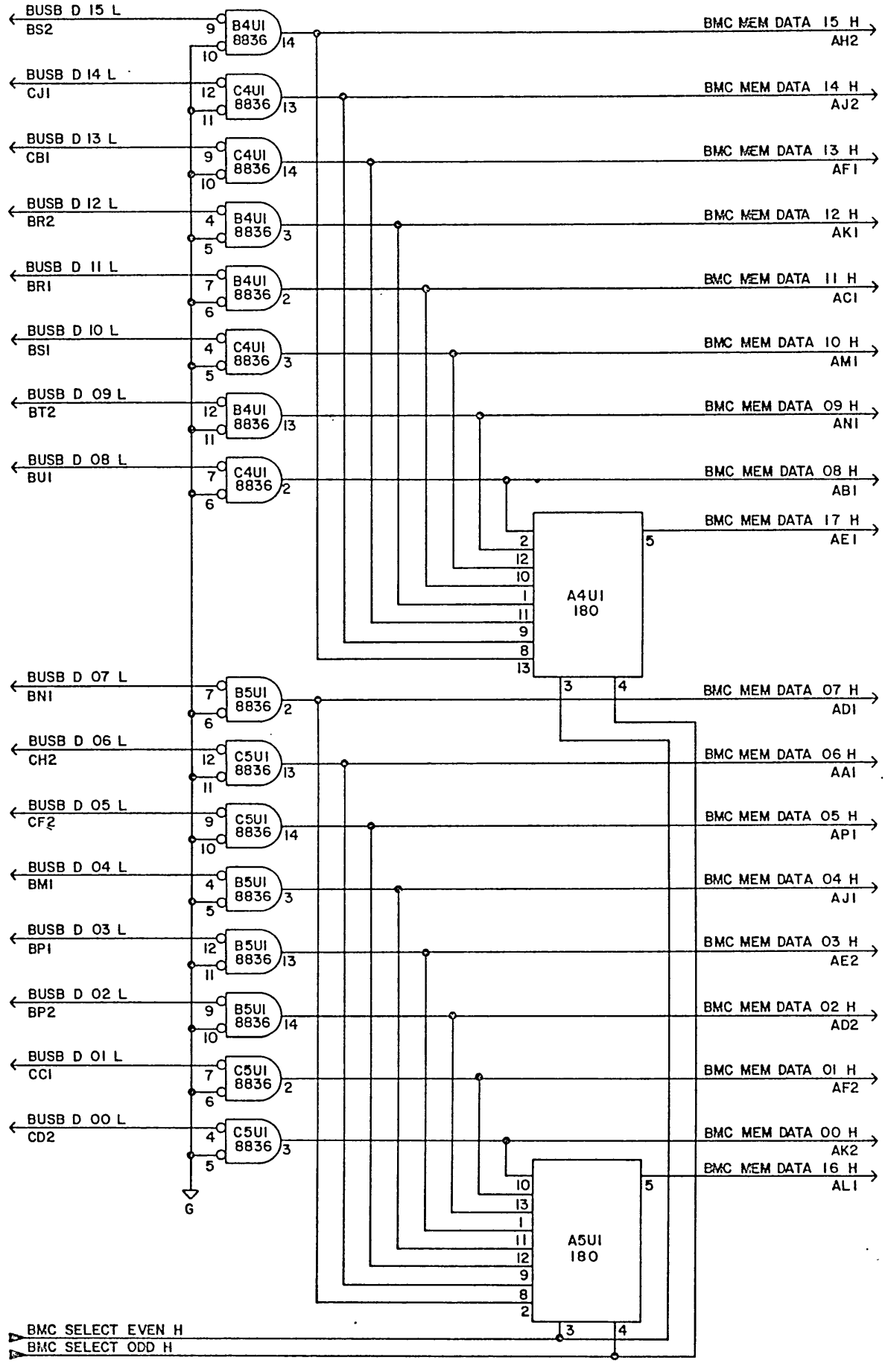
E.C.
HIST.

FABRITEK INC.
MEMORY PRODUCTS DIVISION

TITLE: SCHEMATIC, BUFFER MATRIX CONTROLLER

DWG NO. C 138-0019-62 | TYPE | VERS. | PAGE 14

E.C.
HIST.



FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

TITLE: SCHEMATIC, BUFFER MATRIX CONTROLLER

DWG NO. C 138-0019-62 | TYPE | VERS. | PAGE 15

EC 00A LC 20703
HIST

NOTES: APPLICABLE THROUGHOUT THIS SCHEMATIC.

1 UNLESS OTHERWISE STATED:
A. RESISTANCE VALUES ARE IN OHMS RESISTORS ARE 5% TOLERANCE, 1/4 WATT.
B. CAPACITANCE VALUES ARE IN MICROFARADS.

2. JEDEC OR MANUFACTURER'S PART NUMBERS ARE FOR REFERENCE ONLY. FOR EXPLICIT DESCRIPTION OF THE DEVICE CHARACTERISTICS, REFER TO THE FABRI-TEK SPECIFICATION FOR THE FABRI-TEK PART NUMBER.

REVISION STATUS OF SHEETS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
	00A			00A																		

		DATE
DRAWN	ANDY HO	5-1-74
CHECKED		
APPROVED		17 JUN 74

FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

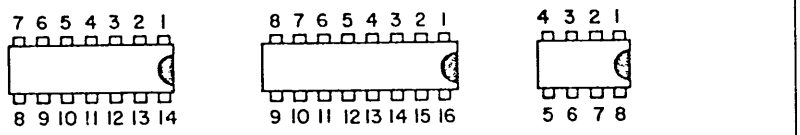
TITLE: SCHEMATIC, BUFFER MEMORY MATRIX

DWG NO C 138-0019-63 | TYPE 190-1866-00 | VERS | PAGE 1 OF 9

EC HIST	

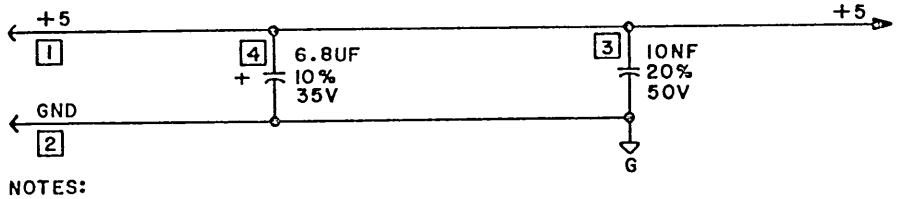
MODULE CODE TABLE

CODE	VENDOR	VENDORS P/N	DESCRIPTION	+5V	GND	TOTAL NO OF PINS
S04	T.I.	SN74S04	HEX INVERTER	14	7	14
S40	T.I.	SN74S40	DUAL 4-INP POS-NAND BUFFERS	14	7	14
3106A	INTEL	C3106A	256 BIT BIPOLAR RAM	16	8	16



CODE	REF DESIG	OUTPUT TERMINAL NO
UNUSED MODULE ELEMENTS		

POWER

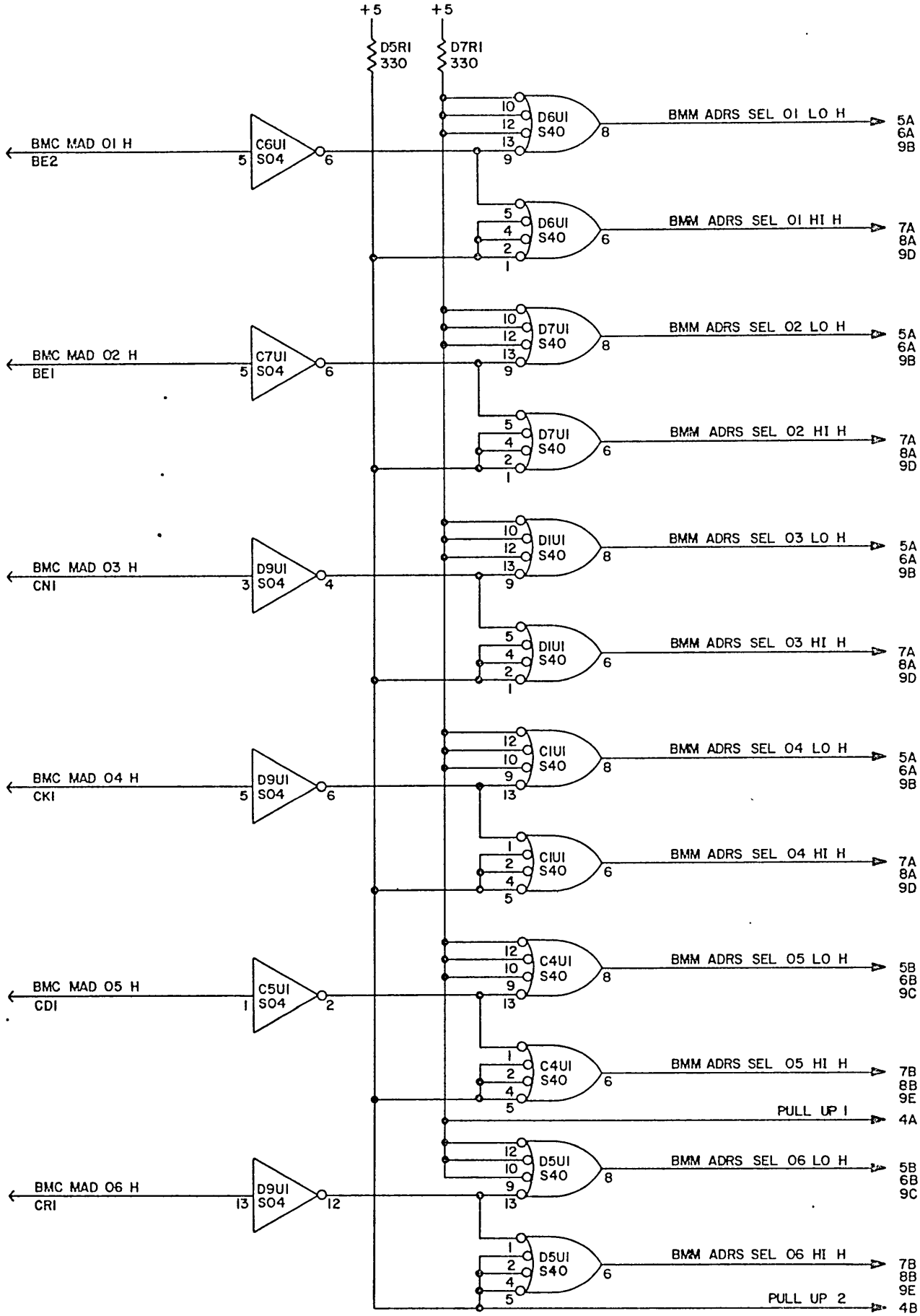


NOTES:

1. TYPICAL OF PIN AA2, AV1, BA2, BV1, CA2, CV1, DA2, DV1, EA2, EV1, FA2, FV2.
2. TYPICAL OF PIN AC2, AN2, AT1, BC2, BN2, BT1, CC2, CN2, CT1, DC2, DN2, DT1, EC2, EN2, ET1, FC2, FN2, FT1.
3. TYPICAL OF CAPACITOR C1C1, C2C1, C3C1, C4C2, C5C1, C6C1, C7C2, C8C1, C9C1, D1C1, D2C1, D3C1, D4C2, D5C1, D6C1, D7C2, D8C1, D9C1, E1C1, E2C1, E3C1, E4C2, E5C1, E6C1, E7C2, E8C1, E9C1, F1C1, F2C1, F3C1, F4C2, F5C1, F6C1, F7C2, F8C1, F9C1, G1C1, G2C1, G3C1, G4C2, G5C1, G6C1, G7C2, G8C1, G9C1, H1C1, H2C1, H3C1, H4C2, H5C1, H6C1, H7C2, H8C1, H9C1.
4. TYPICAL OF CAPACITOR C4C1, C7C1, C9C1, F4C1, E7C1, E9C1, G4C1, G7C1, G9C1.

FABRI-TEK INC. MEMORY PRODUCTS DIVISION	TITLE	SCHEMATIC, BUFFER MEMORY MATRIX		
	DWG NO C	138-0019-63	TYPE	VERS
				PAGE 2

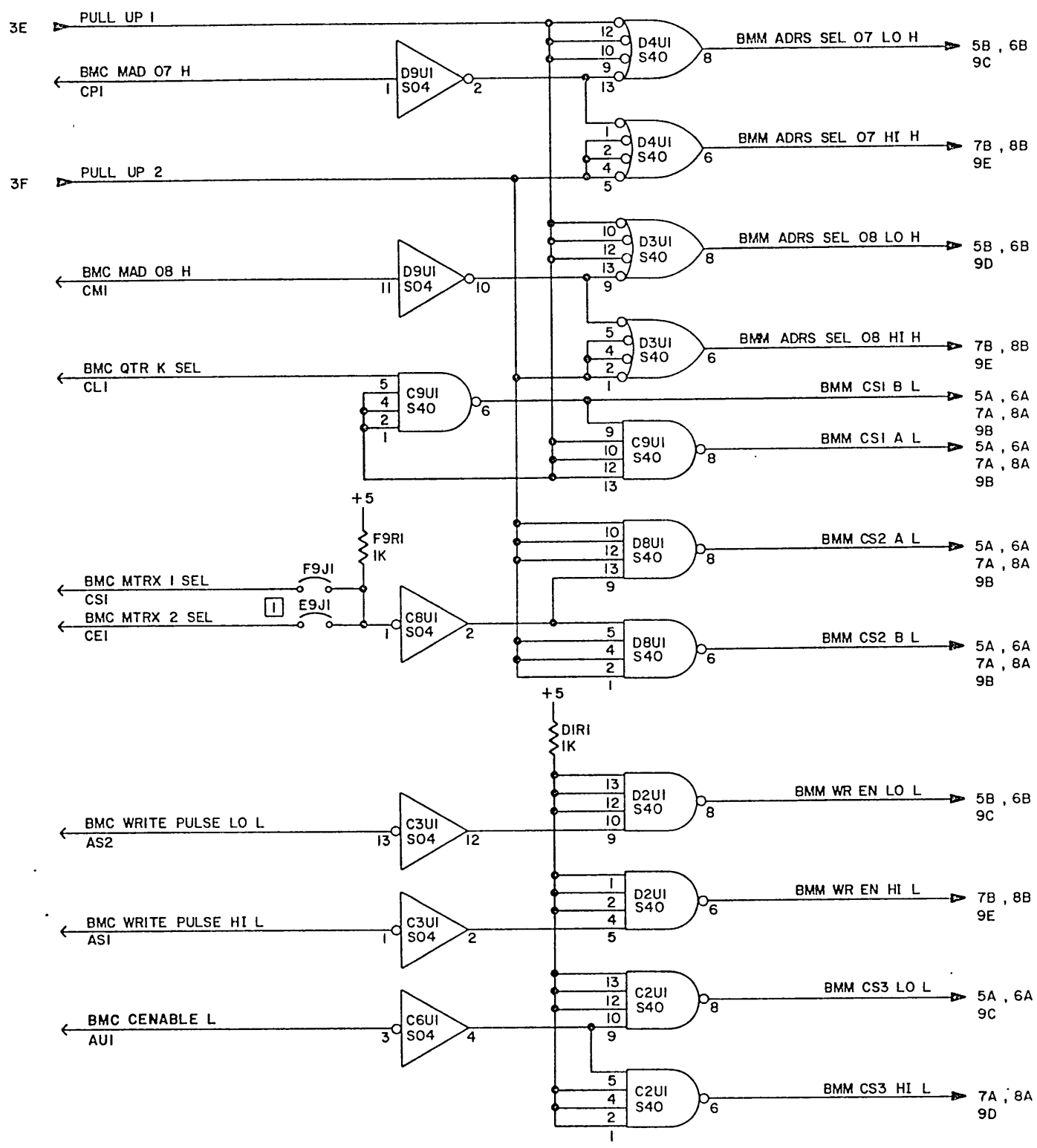
EC.
HIST



FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

TITLE	SCHEMATIC, BUFFER MEMORY MATRIX			
DWG. NO. C 138-0019-63	TYPE	VERS.	PAGE 3	

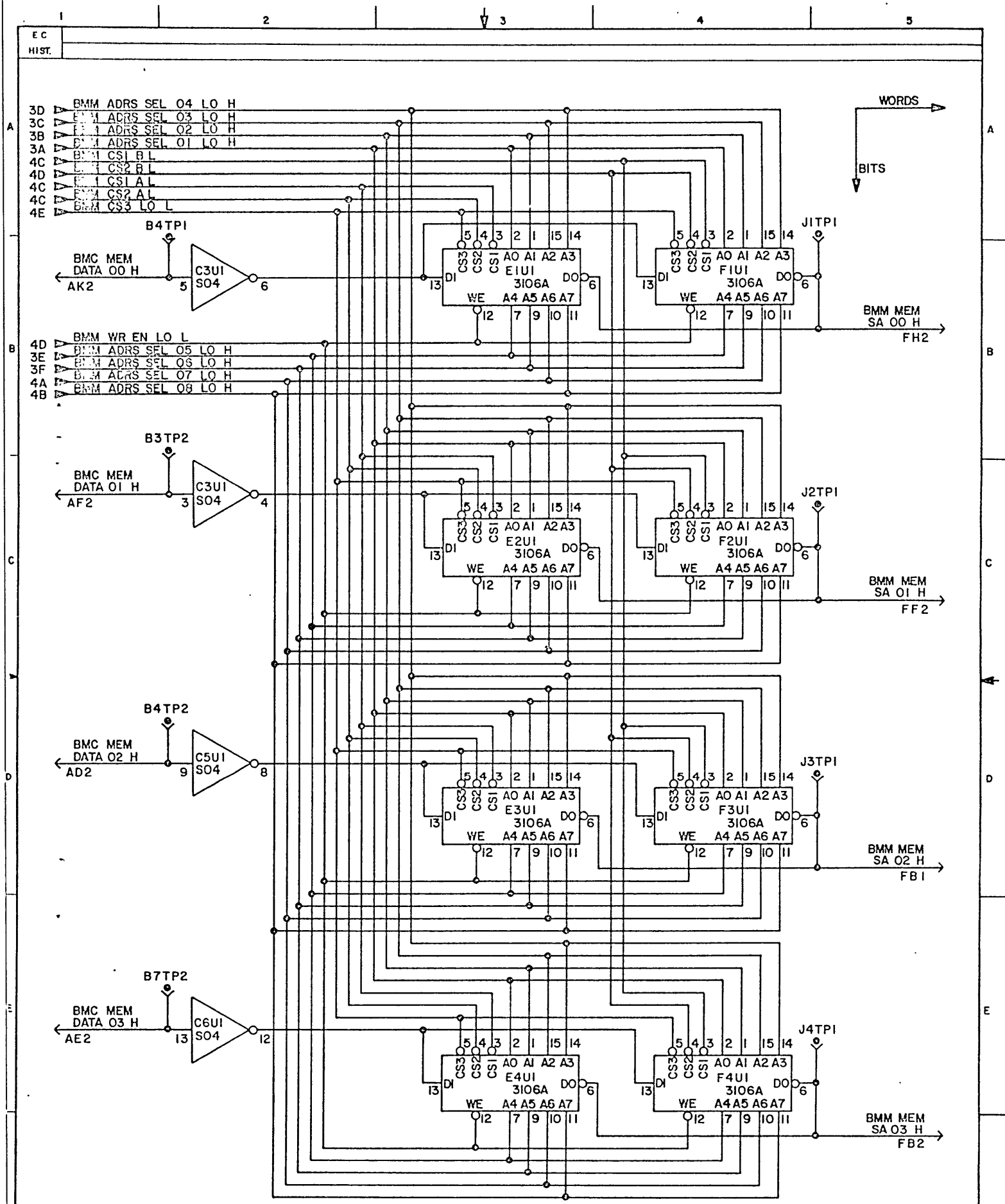
EC HIST.	00A



NOTE:

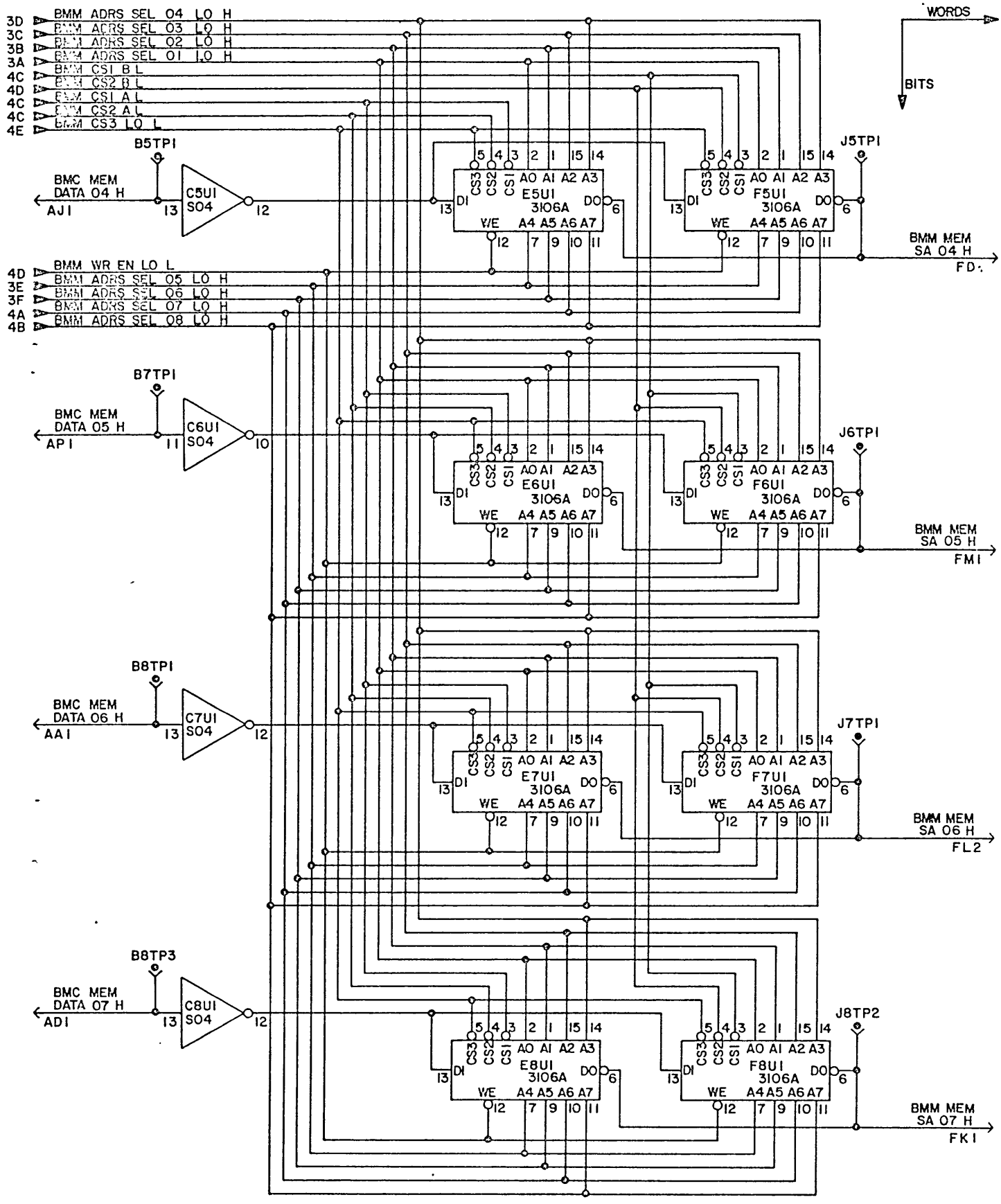
[1] JUMPER F9JI IS PUT IN FOR NORMAL INSTALLATION OF BMM IN SLOT ADJACENT TO BMC. IF BMM IS INSTALLED TWO SLOTS AWAY FROM BMC, USE JUMPER E9JI INSTEAD.

FABRI-TEK INC. MEMORY PRODUCTS DIVISION	TITLE	SCHEMATIC, BUFFER MEMORY MATRIX			
	DWG. NO.	139-0019-63	TYPE	VERS.	PAGE 4



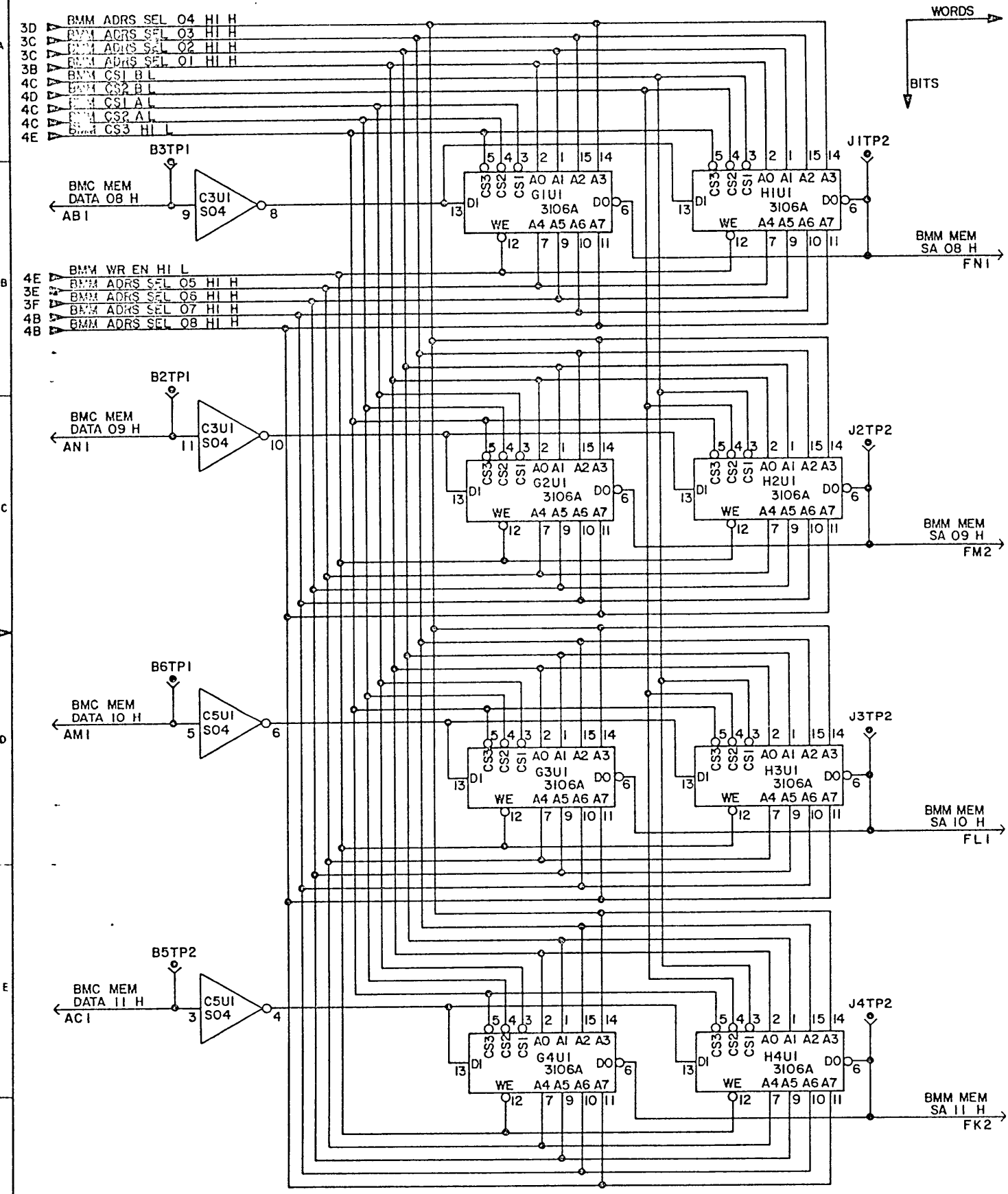
FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

TITLE	SCHEMATIC, BUFFER MEMORY MATRIX			
DWG NO. C	138-0019-63	TYPE	VERS.	PAGE 5

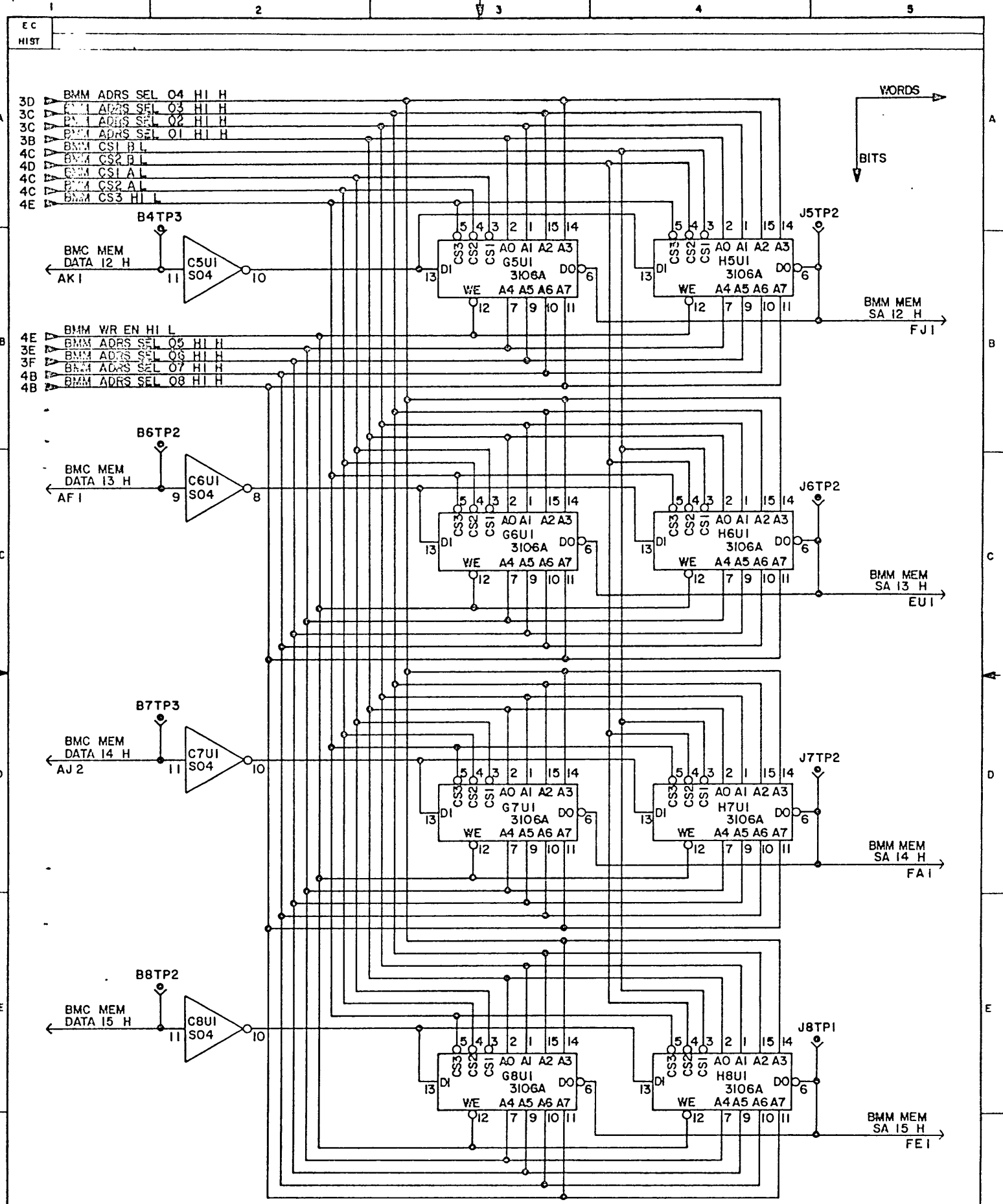


FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

TITLE	SCHEMATIC, BUFFER MEMORY MATRIX			
DWG NO C	138-0019-63	TYPE	VERS.	PAGE 6

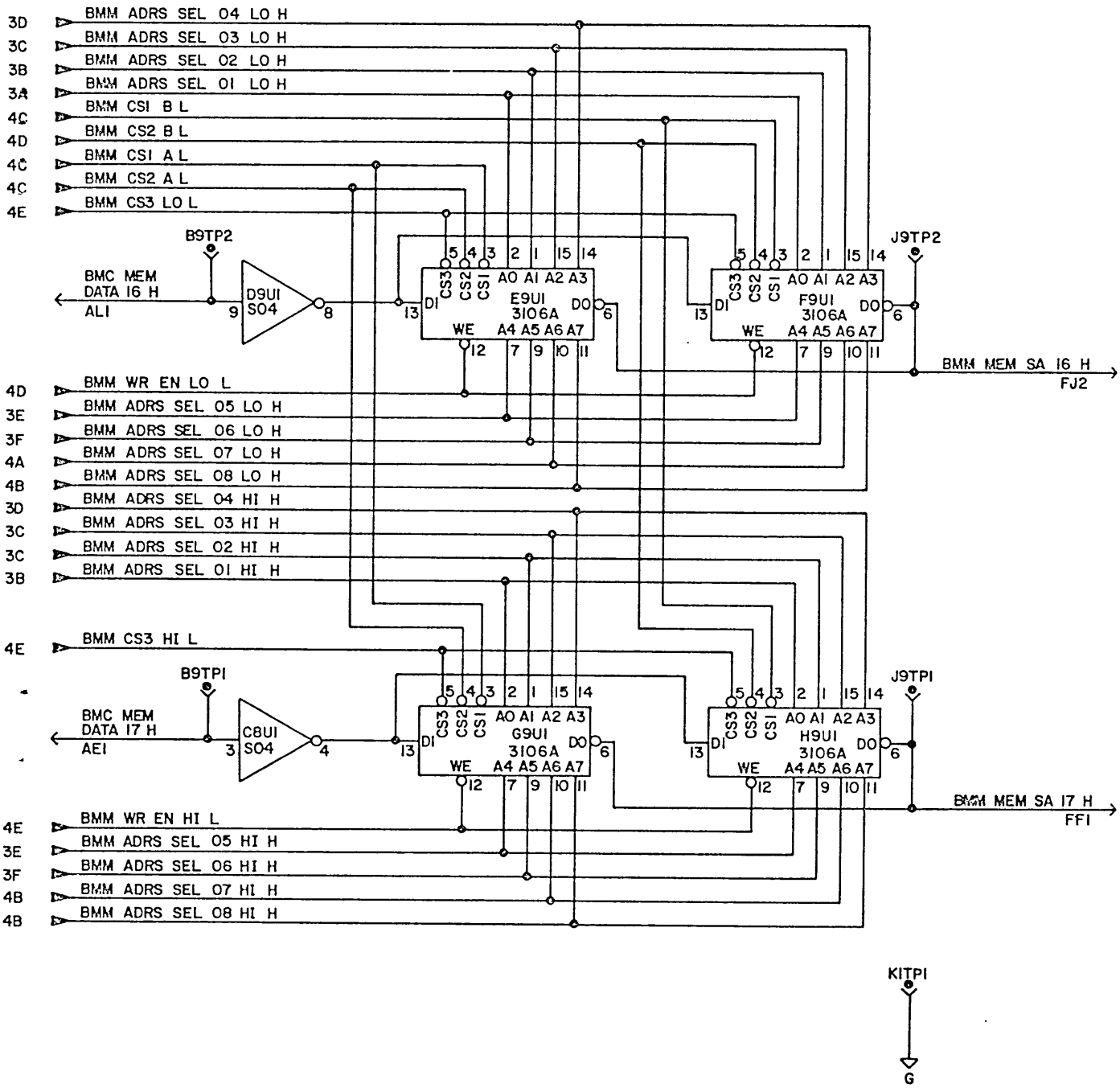


FABRI-TEK INC. MEMORY PRODUCTS DIVISION	TITLE	SCHEMATIC, BUFFER MEMORY MATRIX			
	DWG NO C	138-0019-63	TYPE	VERS	PAGE 7



FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

TITLE	SCHEMATIC, BUFFER MEMORY MATRIX			
DWG NO. C	138-0019-63	TYPE	VERS.	PAGE 8



FABRI-TEK INC. MEMORY PRODUCTS DIVISION	TITLE SCHEMATIC , BUFFER MEMORY MATRIX				
	DWG NO C 138-0019-63	TYPE	VERS	PAGE 9	

1	2	3	4	5

EC HIST	

NOTES: APPLICABLE THROUGHOUT THIS SCHEMATIC.

1. UNLESS OTHERWISE STATED:
   A. RESISTANCE VALUES ARE IN OHMS RESISTORS ARE 5% TOLERANCE, 1/4 WATT.
   B. CAPACITANCE VALUES ARE IN MICROFARADS.

2. JEDEC OR MANUFACTURER'S PART NUMBERS ARE FOR REFERENCE ONLY. FOR EXPLICIT DESCRIPTION OF THE DEVICE CHARACTERISTICS, REFER TO THE FABRI-TEK SPECIFICATION FOR THE FABRI-TEK PART NUMBER.

REVISION STATUS OF SHEETS																					
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

	DATE
DRAWN	
CHECKED	10-16-4
APPROVED	10-16-4

FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

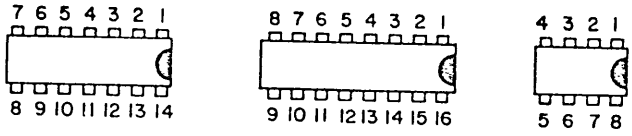
TITLE SCHEMATIC, POWER SUPPLY

DWG NO	TYPE	VERS	PAGE
C 138-0020-56			1 OF 3

E.C.	
HIST	

MODULE CODE TABLE

CODE	VENDOR	VENDORS P/N	DESCRIPTION	+5V	GND	TOTAL NO OF PINS
723		UA723	PRECISION VOLTAGE REGULATOR			14

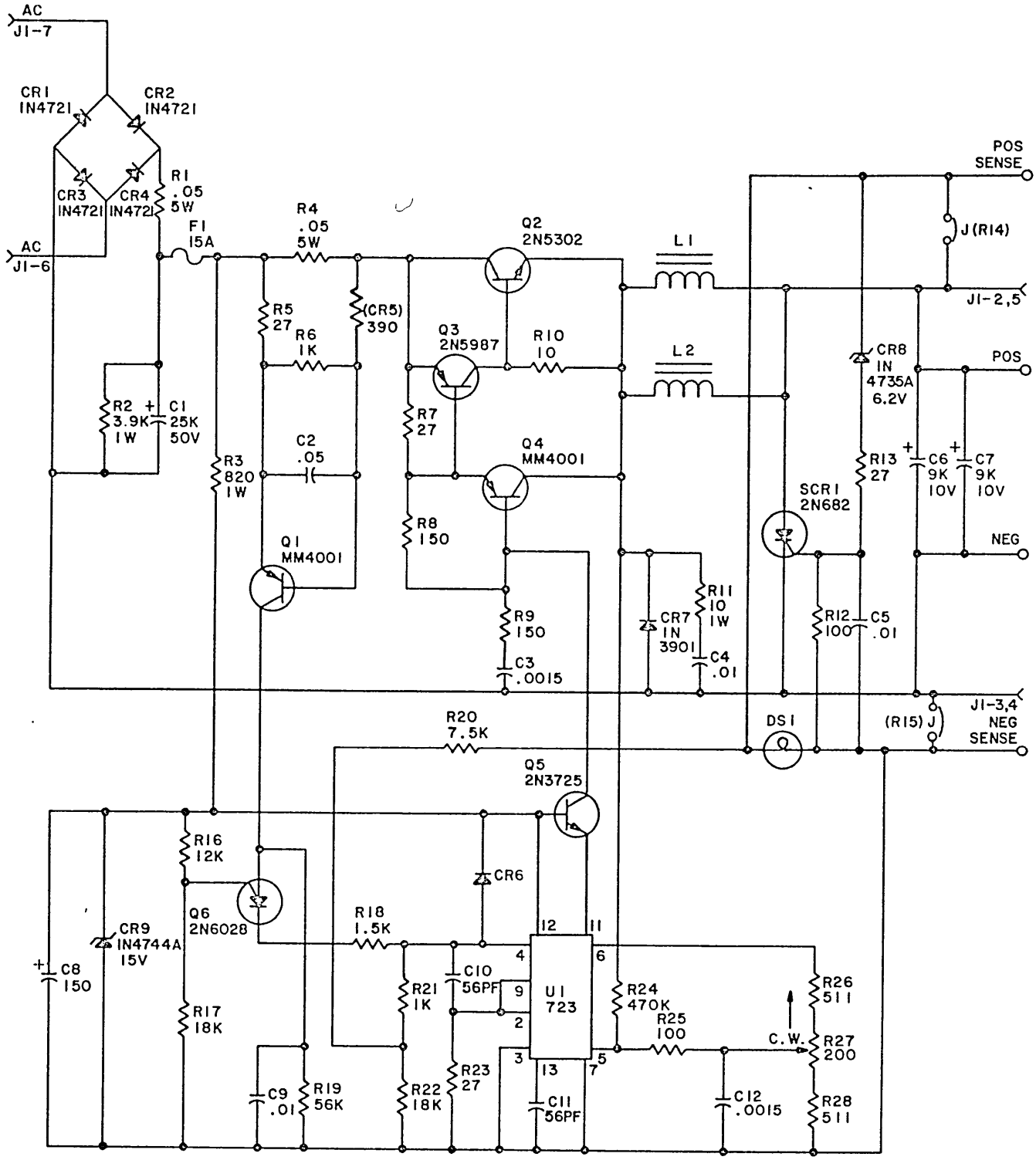


CODE	REF DESIG	OUTPUT TERMINAL NO
UNUSED MODULE ELEMENTS		

POWER

FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

TITLE	SCHEMATIC, POWER SUPPLY			
DWG NO	C 138-0020-56	TYPE	VERS	PAGE 2



FABRI-TEK INC. MEMORY PRODUCTS DIVISION	TITLE SCHEMATIC, POWER SUPPLY				
	DWG. NO. C 138-0020-56	TYPE	VERS.	PAGE 3	

EC	00A EC-20704
HIST	F

NOTES APPLICABLE THROUGHOUT THIS SCHEMATIC.

1 UNLESS OTHERWISE STATED.
- A RESISTANCE VALUES ARE IN OHMS RESISTORS ARE 5% TOLERANCE, 1/4 WATT.
- B. CAPACITANCE VALUES ARE IN MICROFARADS.

2 JEDEC OR MANUFACTURER'S PART NUMBERS ARE FOR REFERENCE ONLY. FOR EXPLICIT DESCRIPTION OF THE DEVICE CHARACTERISTICS, REFER TO THE FABRI-TEK SPECIFICATION FOR THE FABRI-TEK PART NUMBER.

REVISION STATUS OF SHEETS																						
	00A	/	00A																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

	DATE
DRAWN HONG KONG	6-1-74
CHECKED	
APPROVED	

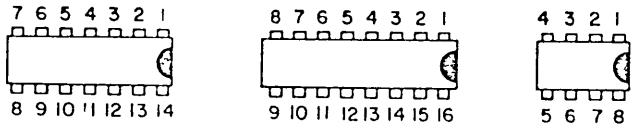
FABRI-TEK INC.
MEMORY PRODUCTS DIVISION

TITLE SCHEMATIC, AUXILIARY BUFFER MATRIX CONTROLLER

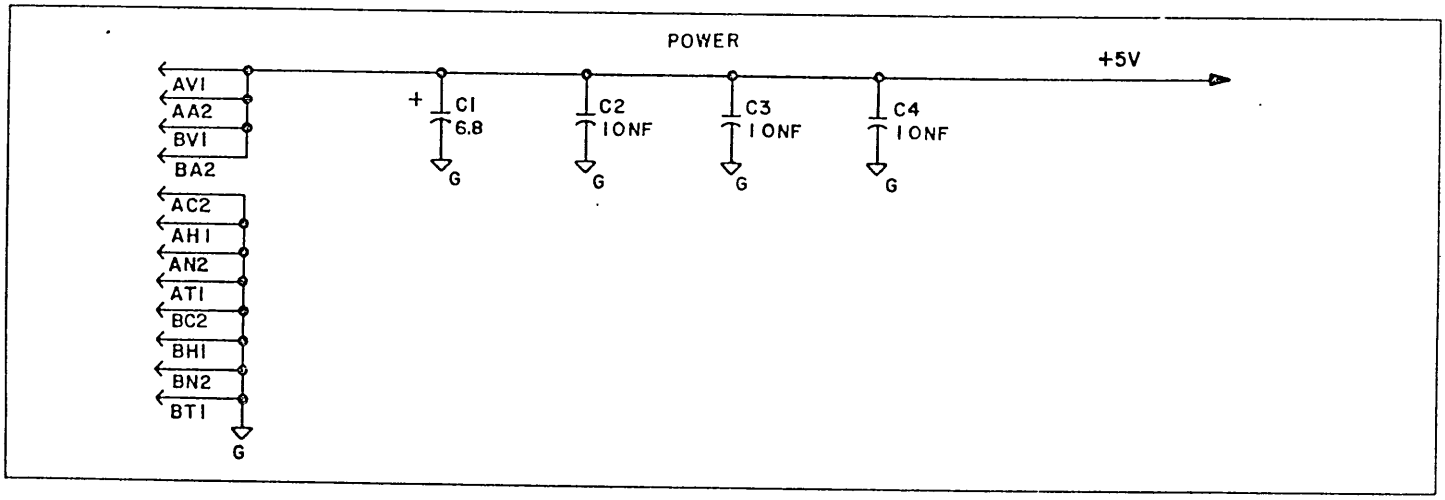
DWG NO	TYPE	VERS	PAGE
C 138-0020-69	960-0506-00		1 OF 3

EC HIST

MODULE CODE TABLE						
CODE	VENDOR	VENDORS P/N	DESCRIPTION	+5V	GND	TOTAL NO OF PINS
S04	T. I.	SN74S04	HEX INVERTER	14	7	14
S74	T. I.	SN74S74	DUAL D-TYPE F F	14	7	14
8836	N. S.	DM8836	QUAD 2-IN NOR RCVR	8	1	14



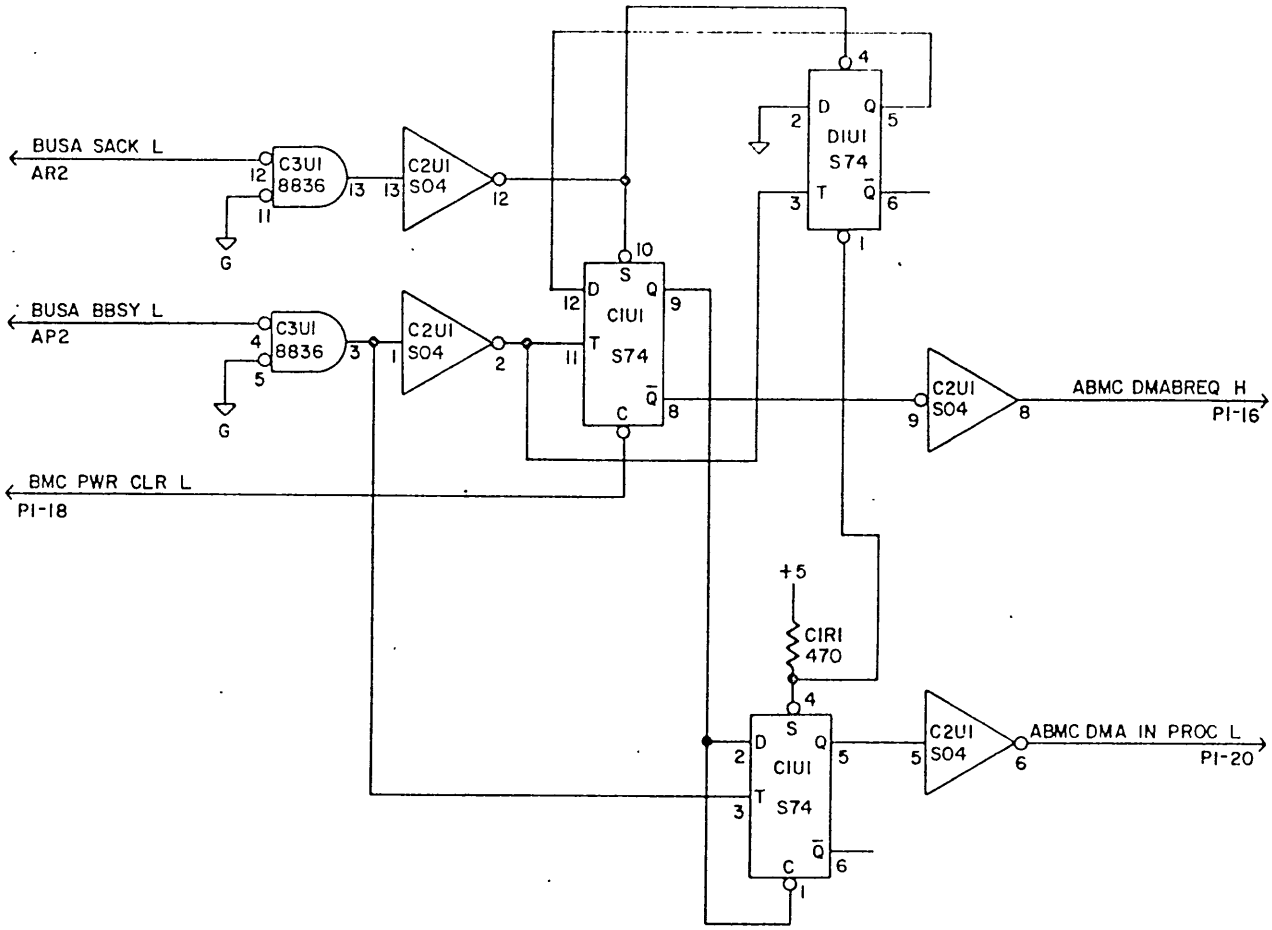
CODE	REF DESIG	OUTPUT TERMINAL NO
UNUSED MODULE ELEMENTS		



FABRI-TEK INC
MEMORY PRODUCTS DIVISION

TITLE	SCHEMATIC, AUXILIARY BUFFER MATRIX CONTROLLER			
DWG NO C	138-0020-69	TYPE	VERS	PAGE 2

EC	00A
HIST	



FABRI-TEK INC. MEMORY PRODUCTS DIVISION	TITLE	SCHEMATIC , AUXILIARY BUFFER MATRIX CONTROLLER			
	DWG NO C	138-0020-69	TYPE	VERS	PAGE 3

COMMENT SHEET

Manual Title: _____

Publication Number: _____ Title Page Revision Letter: _____

From: Name _____

Business Address _____

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FABRI-TEK welcomes your comments and evaluation of this publication. Use this postage paid mailer to record errors, to note deficient areas, and to make general comments. Reference specific subjects and page numbers whenever possible.