8. ARITHMETIC SECTION

a. GENERAL. - The Arithmetic Section, located in the 10,000 Cabinet, uses special procedures derived from the fundamental processes of binary arithmetic to perform all the arithmetic and logical operations involved in the execution of instructions. The section performs a single fundamental operation, addition. It performs all of the other arithmetic and logical operations as forms of addition. Besides its primary function, the section performs several auxiliary functions, as follows:

(1) ~~It assembles the six-digit word groups presented to it by the Photoelectric Tape Reader and distributes them, as complete words, to the Storage Section.~~

(2) It serves as the switching center for most of the internal transmissions of data.

(3) It assembles and disassembles words as they pass to and from the Magnetic Tape System.

(4) It provides the computer with the two storage classes A and Q. Each of these classes provides rapid-access storage for a single 36-bit word.

The arithmetic section is composed of three registers, the X-Register, the Q-Register, and the Accumulator, and the Arithmetic Sequence Control. The following subparagraphs discuss the characteristics of each of the three registers, the special procedures of binary arithmetic which adapt these registers to the performance of arithmetic and logical operations, and the characteristics of the Arithmetic Sequence Control and the manner in which it directs the performances of the arithmetic and logical operations by the arithmetic registers.

b. X-REGISTER. - The X-Register, X, is a simple storage register capable of holding a single 36-bit word. It stores the addend, subtrahend, multiplicand, and divisor during the corresponding arithmetic operations and serves as a switching register during most of the internal transmissions of data. The register consists of 36 stages, each composed of a flip-flop, with multiple inputs to its "1" and "0" sides, and several gates, enabled by either of the flip-flop outputs. Each stage holds one of the digits of a word, the digit having been stored there by a pulse

applied to the proper one of the flip-flop inputs. The digit is read from the stage by probing one of the gateswith a second pulse. If the gate is attached to the "1" output of the flip-flop, the pulse transmits only a "1" digit out of the stage. If the gate is attached to the "0" output, the pulse transmits only a "0" digit from the stage.

The X-Register is prepared for receipt of a word by the signal CLEAR X. This signal effectively clears X of its contents by setting each of the flip-flops to the "0" state. A number held in X is complemented by the signal COMPLEMENT X. This signal, applied to the trigger input of each flip-flop in X, reverses the state of the flip-flop regardless of its initial content. The signals which transmit words into X are as follows:

(1) Q' → X'. - The stages of X must be initially set to "1" by the signals CLEAR X and COMPLEMENT X in succession. Q' → X' inserts the word held in Q into X by transmitting the "0" digits from Q into the respective "0" inputs of X.

(2) A_R → X. - This signal inserts the number held in the lower-order 36 stages of A into X by transmitting the "1" digits from A_R into the respective "1" inputs of X.

(3) SET X to 1. - This signal inserts the number 1 into X by setting its lowest-order flip-flop to "1" and all of its other flip-flops to "0".

(4) SAR → X. - This signal inserts an address held in SAR into the 15 lower-order stages of X by transmitting the "1" digits from SAR into the respective "1" inputs of X.

(5) INITIATE READ MD. - This signal results in the transmission of the "1" digits from a specified MD address into the respective "1" inputs of X.

(6) INITIATE READ ES. - This signal results in the transmission of the "1" digits from a specified ES address into the respective "1" inputs of X.

The pulses which transmit words out of X are as follows:

(1) X → Q. - This signal inserts the word held in X into Q by transmitting the "1" digits from X into the corresponding "1" inputs of Q.

(2) $X' \rightarrow A_R$. - This signal performs the first step in the addition of a number in X into A. The pulse reverses the state of those flip-flops of A_R whose corresponding flip-flops in X hold "0"s.

(3) $X \rightarrow PCR$. - This signal inserts an instruction, held in X, into PCR by transmitting the "1" digit from X into the corresponding "1" inputs of UAK, VAK, and MCR.

(4) INITIATE WRITE MD_{0-14}, INITIATE WRITE MD_{15-29}, INITIATE WRITE MD_{0-35}. - Any one of these signals initiates the transmission of "1" digits from X to a specified MD storage address. The group of digits which is transferred, in each case, is indicated by the subscript numbers.

(5) INITIATE WRITE ES_{0-14}, INITIATE WRITE ES_{15-29}, INITIATE WRITE ES_{0-35}. - Any one of these signals initiates the transmission of "1" digits from X to a specified ES storage address. The group of digits which is transferred, in each case, is indicated by the subscript numbers.

(6) $X_{0-11} \rightarrow$ 0BK, $X_{0-11} \rightarrow$ 1BK, $X_{0-11} \rightarrow$ 2BK, $X_{0-11} \rightarrow$ 3BK. - Each of these signals transmits "1" digits from the twelve lower-order stages of X to a different one of the four Block Counters in the MT Storage System.

(7) $X_{0-5} \rightarrow$ TWR. - This signal transmits the six lower-order digits of X into the thyratron Typewriter Register.

(8) $X_{0-5} \rightarrow$ HPR. - This signal transmits the six lower-order digits of X into the thyratron High Speed Punch Register.

c. Q-REGISTER. - The Q-Register is a 36-stage storage register similar to X. It has the added property, however, of left circular shift, i.e. a word in Q may be shifted one place to the left, with the highest order digit entering the lowest order stage, by the introduction of a single control pulse. Q holds the multiplier, quotient, and logical multiplier in the corresponding operations. As internal storage class Q, it provides rapid-access one-word storage during the performances of other operations.

Q is cleared by the signal CLEAR Q, which sets each of its flip-flops to the "0" state. The signals which transmit words into Q are as follows:

(1) $X \rightarrow Q$. - This signal, discussed in the previous paragraph, transmits the word held in X into Q.

(2) PT FEED PULSES. - Each of these signals, during loading, transmits six bits of a word stored on the punched tape into six lower-order stages of Q.

(3) MTO → Q_{0-1}. - This signal transmits the two bits stored in the magnetic tape output register into the two lower-order stages of Q.

(4) SET Q_0 TO 1. - This signal sets the lowest-order flip-flop of Q to its "1" state.

A word stored in Q is shifted one stage to the left by the signal QL 1. This signal transmits the digit stored in each stage of Q into the flip-flop of the next higher-order one, with the digit in the highest-order stage being transmitted into the lowest-order flip-flop. The signal $Q_{35} \rightarrow Q_0$, generated during the division process, transmits the contents of the highest order stage (Q_{35}) into the lowest order stage (Q_0). The signals which transmit words out of Q are as follows:

(1) Q' → X'. - This signal, discussed in the previous paragraph, transmits the word held in Q into X.

(2) Q_{0-1} → MTI. - This signal transmits the digits held in the two lower-order stages of Q into the Magnetic Tape Insertion Register.

d. ACCUMULATOR

(1) FUNCTIONAL CHARACTERISTICS. - The Accumulator is a 72-stage flip-flop register, with subtracting and shifting properties. It forms the sum in addition, the difference in subtraction, the product in multiplication and holds the dividend and remainder in division. As internal storage class A, it provides rapid-access one-word storage during the performances of other operations. The 36 lower-order stages of A, designated A_R, are numerically equivalent to the stages of X and Q. The 36 higher-order stages, designated A_L, provide the accumulator with double precision properties and the capacity to handle double length numbers. Numbers are transferred into A exclusively from X. During the transfer, the numbers are automatically converted from the modulus of X ($2^{35}-1$) to the modulus of A ($2^{72}-1$). The accumulator is basically subtractive, that is, it subtracts a number entered into it from the number it already holds. It is made functionally additive by providing automatic complementing of the number during its transmission from X. As a result, a number is

always added into A; subtraction is performed by complementing the number before the transmission and automatic complementing takes place.

The sections of the accumulator, A_R and A_L, are cleared by the respective signals CLEAR A_R and CLEAR A_L, each of which sets the flip-flops in the designated section to the "0" state. A number in A is shifted to the left one place by the signal ALl. A number in X is added into A by the four signals $X' \rightarrow A_R$, AR PROBE, A_L INPUT, and A_L PROBE. The specialized function which each of these pulses perform during the addition is discussed in the succeeding subparagraph which discusses the arithmetic properties of the accumulator. A number in A_R is transferred into X by the signal $A_R \rightarrow X$, discussed in a previous paragraph.

(2) ARITHMETIC PROPERTIES.

(a) GENERAL. - The basic arithmetic operation performed is a sequence termed "Add X to A". Since most arithmetic subroutines contain this fundamental operation, it is imperative that "Add X to A" be well understood.

There are two factors that tend to complicate the comprehension of this operation: one is the subtractive nature of the Accumulator and the other is the double length of the Accumulator. To perform addition in a subtractive Accumulator the complement of the contents of the X-Register is subtracted from the Accumulator. The transfer of the complement of (X) is achieved simply by transmitting from the "0" side of each X stage to the corresponding stage in A. The double length of the Accumulator presents a problem in the handling of the algebraic sign. Since the sign in the X-Register is held in the highest-order stage, X_{35}, and the sign in the Accumulator is held in the highest-order stage of A_L, A_{71}, a means must be provided to transmit the sign information into the upper half of A. By assuming the existance of an imaginary upper-order X-Register consisting of X_{36} through X_{71} which will be referred to as X_L, the difficulty can readily be resolved. X_L actually is represented by a single stage X_{35}. If $X_{35}=0$, all stages of X_L would hold zeros; if $X_{35}=1$, all stages of X_L would hold ones. Then we can assume that a transmission from X_L to A_L would be carried out exactly like the transmission from X to A_R. All that need be done is to sense the value in X_{35} and treat all stages of A_L in accordance with this value.

The circuitry between X and A actually carries out addition in two distinct steps: the first is the transmission from X to A, and the second is the generation of borrows which have the dual purpose of completing the subtraction and correcting the algebraic sign. To perform these steps, three rules must be formulated:

1. A bit in an Accumulator stage is changed from "0" to "1" or from "1" to "0" (complemented) only if the corresponding bit in the X-Register is "0".

2. A BORROW from the next higher-order stage is necessary if a bit in an Accumulator stage is changed from "0" to "1".

3. A RAPID-BORROW from the next higher-order stage is necessary if any borrow changes the bit in an Accumulator stage from "0" to "1".

Consider the case in which a positive number in X is to be added to zero in A. The first step consists of transmitting the complement of the number in X to A. Since in this case $X_{35}=0$, the non-existent X_L will contain all zeros. The transmission of the complement will result in A containing ones wherever a zero is present in X. The partial sum effected by this transmission will appear as a negative number in A because A_L will contain all ones and the sign is determined by a "1" in A_{71}. However, the second step, in which BORROWS are generated, will rectify the apparent errors by changing the ones to zeros in A_L as well as correcting the sum in A_R. The final sum, therefore, appears as a positive number ($A_{71}=0$) and the number in A_R will be identical with that in X. This operation is shown in the following example in which a basic register length of four stages is used.

	(A_L)	(A_R)	(X)
Initial Condition:	0000	0000	0101

In assuming that the X-Register is also of double length, X would appear as:

(X_L)	(X)
0000	0101

STEP 1. The transmission of the complement of (X) results in the following partial sum:

(A_L)	(A_R)
1111	1010

Note that this sum appears negative since $A_7=1$

STEP 2. Those stages of A which were changed from "0" to "1" necessitate borrows from the next higher order stage (an oblique solid arrow indicates a BORROW, a horizontal broken arrow indicates a RAPID-BORROW):

(A_L)	(A_R)
1 1 1 1	1 0 1 0

The final result after all borrows are completed is as follows:

(A_L)	(A_R)
0000	0101

The final sum is now the sum of (X) and (A), 5+0, and is positive since $A_7=0$.

This operation is effected by four signals: two transmissive signals, X'→ A_R and A_L INPUT, and, later, two borrow signals, A_R PROBE and A_L PROBE. The signals X'→ A_R and A_R PROBE are always produced in an "Add X to A" operation, but the signals A_L INPUT and A_L PROBE are produced only when the number in X is positive ($X_{35}=0$).

Each accumulator stage contains, in addition to transfer and shift gates, a "borrow" gate and a "rapid-borrow" gate. In A_R, the "borrow" gate is enabled whenever the stage stores a "1" and the corresponding stage of X stores a "0". The signal A_R PROBE passes the enabled gate and enters the next higher-order stage as a BORROW signal. In A_L, the "borrow" gate is enabled when the stage holds a "1". The signal A_L PROBE then passes the gate and enters the next higher-order stage as a BORROW signal. A BORROW signal always performs two functions in the stage it enters:

1. It probes the "rapid-borrow" gate.
2. It reverses the state of the flip-flop.

A "rapid-borrow" gate in either A_R or A_L is enabled when the stage with which it is associated stores a "0". The BORROW signal passes the enabled gate and enters the next higher-order stage as a RAPID-BORROW signal. The RAPID-BORROW performs the same functions as the BORROW.