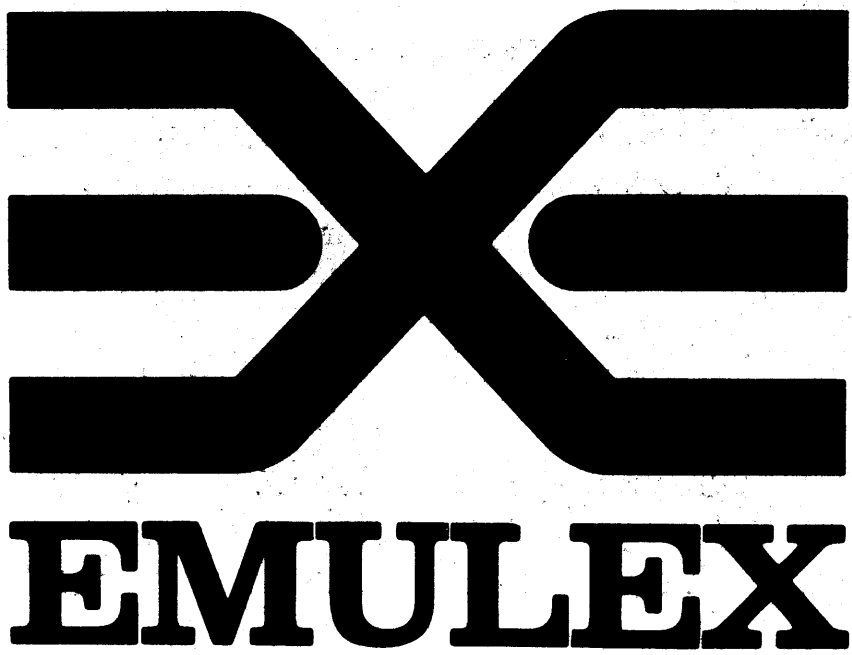
RH70

SC71/B1 SC70/B3

(RM02/RM03/RM05 COMPATIBLE)

DISK CONTROLLER

TECHNICAL MANUAL



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INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC71/B1 and SC70/B3 Disk Controllers. In addition, this manual provides diagnostics and application information.

1.2 OVERVIEW

1.2.1 General Description

The SC71/B1 Disk Controller is a three-board imbedded controller for PDP-11/70 computer manufactured by Digital Equipment Corporation. This controller can be used to interface any large disk having a Storage Module Drive (SMD) interface. The SC71/B series of controllers is capable of emulating the DEC Massbus disk subsystems. The SC71/B1 emulates the DEC RWM03 disk subsystem while the SC71/B2 emulates the DEC RWP06 disk subsystem. These controllers are capable of operating with disk drives having different characteristics from those used in the DEC disk subsystems. The SC71/B controllers provide the capability of operating with a mixture of disks having storage capacity of 5-600 megabytes.

1.2.2 Controller Models

The various SC71/B and SC70/B models performing RM02/RM03/RM05 emulations are described below:

SC71/B1 - Basic RM emulation with configuration PROM for drive size. Drives may be of different size.

SC70/B3 - Same as SC71/B1, except that there are eight built-in drive sizes and all drives must be of the same size.

1.3 FEATURES

1.3.1 Microprocessor Design

The SC71/B1 design incorporates a unique (patent pending) 16-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement

features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various sizes.

1.3.2 Packaging

The SC71/B1 is constructed on three hex-size multi-layer PC board which plug directly into the PDP-11/70 chassis. No cabling is required between the computer and the disk controller. The controller obtains its power from the PDP-11/70.

1.3.3 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the FAULT LED on and the controller cannot be addressed from the CPU.

1.3.4 Buffering

The controller contains a 1K x 16 high-speed RAM buffer used to store the device registers of the controller and drive being emulated and for two sectors of data buffering. Because of the buffering and the strategies used to employ it, data late situations are not possible.

1.3.5 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting single error bursts of up to 11 bits in length and detecting bursts of longer length. The controller determines the location of the error and the error pattern and passes this information to the PDP-11 which performs the actual correction. A 16-bit CRC is employed with the header of every sector.

1.3.6 Option and Configuration Switches

The controller has switches for configuring the disk size, the Unibus address and vector address and various controller options.

1.3.7 Dual-Port Capability

The controller can operate with disk drives having dual-port capability which allows a second controller to have access to the drive on a priority basis.

1.3.8 Fixed Head Capability

The SC71/B1 controller supports the fixed head storage found on some Winchester type disk drives.

1.4 FUNCTIONAL COMPATABILITY

1.4.1 Media Compatability

The SC71/B1 is media compatible with the DEC RM02/RM03 packs when using a CDC 9762 drive or equivalentand with the DEC RM05 when using CDC 9766 drive or equivalent.

1.4.2 Disk Mapping

For an 80 MB disk drive, the mapping is the same as the DEC RM02. When drives of different sizes are used, the mapping is done in a straight forward manner with only the number of heads and/or number of cylinders being varied. In all cases, the disk drive is configured for 32 sectors.

1.4.3 Diagnostics

The controller executes the following standard DEC RM02/RM03 diagnostics:

ZRMA - Formatter
ZRMB - Performance Exerciser
ZRMC - Functional Controller, Part I *
ZRMD - Functional Controller, Part II
ZRME - Functional Controller, Part III *
ZRMF - Extended Drive Test
ZRMI - Drive Compatibility Test

The diagnostics marked with an asterisk require certain patches to correct coding problems or bypass unsupported maintenance mode functions. All diagnostics require patches to run with drive sizes other than that of a standard RM02/RM03.

1.4.4 Operating Systems

The SC71/B1 controllers are compatible with DEC operating systems without modification when operating with an 80 MB disk drive having 823 cylinders and 5 tracks. Patches are required to the operating system when operating with other than standard size disks. These patches numerically redefine the logical drive capacity to the operating system and generally do not involve modification to program instructions.

Table 1-1

GENERAL SPECIFICATIONS

Functional	
Emulation	DEC RM02, RM03, and RM05
Media Compatability	DEC RM02, RM03, and RM05 when using appropriate disk drives.
Drive Interface	SMD
Drive Ports	4
Error Control	32-bit ECC for data and 16-bit CRC for headers. Correction of single data error burst of up to 11 bits.
Sector Size	256 words (512 bytes)
Sectors/Track	32
Tracks/Cylinder	SC71/B: Selectable for each drive. SC70/B: Selectable for all drives.
Cylinders/Drive	SC71/B: Selectable for each drive. SC70/B: Selectable for all drives.
Drive Type Code	SC71/B: Selectable for each drive. SC70/B: 24
Computer Interfaces	Unibus and Cache Bus
Unibus Address	Switch selectable
Vector Address	Switch selectable
Priority Level	BR5
Data Bufferring	SC71/B: 2 Sectors (512 words) SC70/B: 3 Sectors (768 words)
Data Transfer	32-bit transfer via Cache Bus
Self-Test	Extensive internal self-test on powering up.
Indicators	READ, WRITE, FAULT, BUFFER PARITY ERROR

Table 1-1 (cont'd)

Design	High-speed bipolar microprocessor using 2901 bit-slice components.
Physical	
Packaging	Three DEC hex-size board.
Mounting	Any set of RH70 slots in PDP-11/70.
Connectors	One 60-pin A cable flat connector and four 26-pin B cable connectors. (Flat cable type.)
Electrical	
Unibus Interface	DEC approved line drivers and receivers.
Drive Interfaces	Differential line drivers and receivers. A cable accumulative length to 100 feet. B cable length to 50 feet.
Power	+5 v, 11 Amp. max. -15 v, 1 Amp. max.

2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC71/B1 controller is shown in Figure 2-1. The controller is organized around a 16-bit high-speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with four 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with 12 2K x 4 PROM's.

The controller incorporates a 1K x 16 high-speed RAM buffer which is used to store the controller's device registers and three sectors (768 words) of data buffering.

The A Cable Register (ACR) provides the storage of all A cable signals going to the disk drives. The inputs from the selected drive are testable by the microprocessor.

Serial data from the drive is converted into 16-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data access from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used in a 16-bit CRC mode for the headers. The actual ECC polynomial operation is done independent of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

The Unibus interface consists of a 16-bit bi-directional set of data lines and an 18-bit set of address lines. The Unibus interface is used for programmed I/O and CPU interrupts. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all data transfers between the buffer and the PDP-11/70 memory via the Cache Bus.

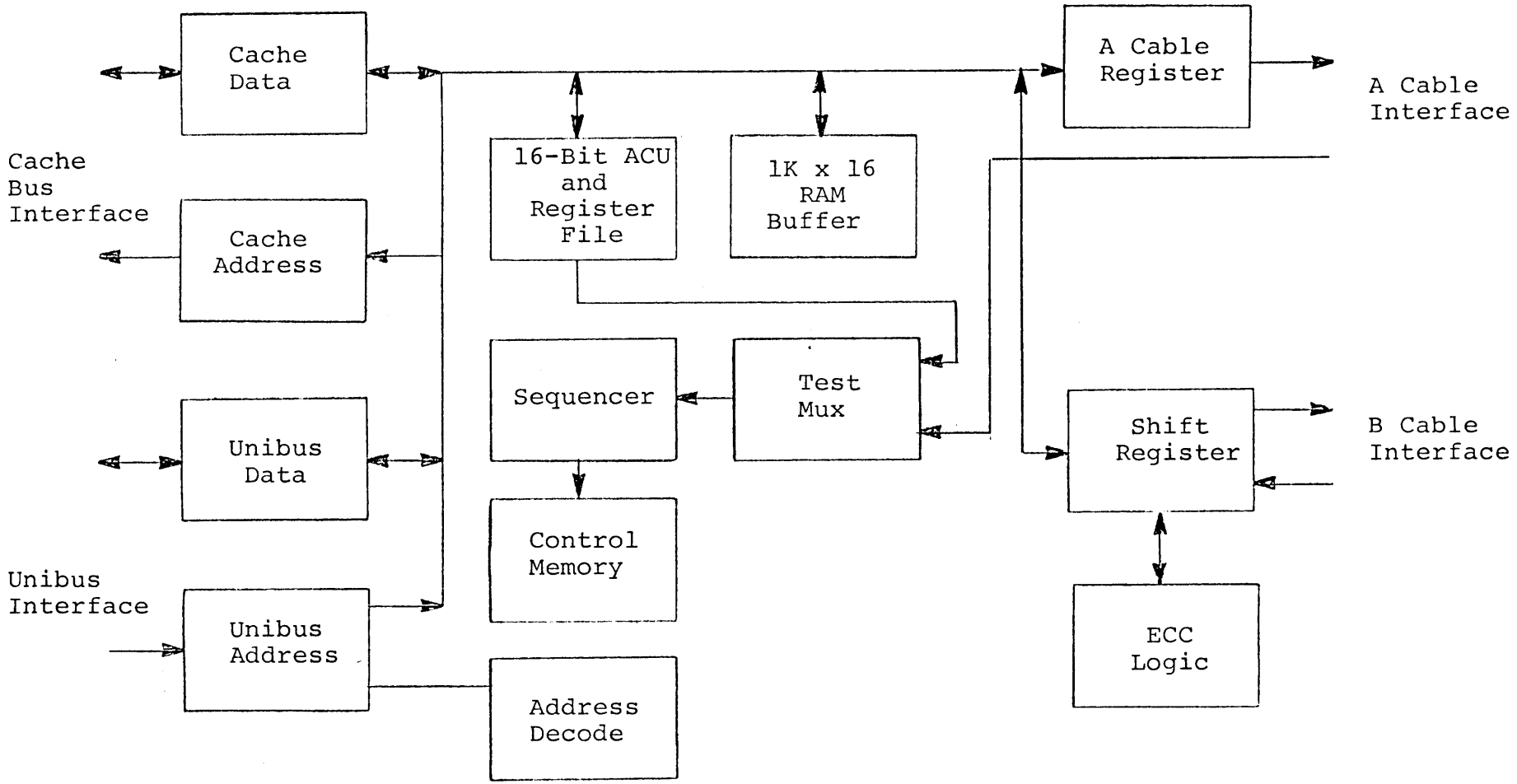


Figure 2-1
SC71 Block Diagram

2.2 PHYSICAL DESCRIPTION

The SC71 controller consists of three hex size boards and a small interconnect board, all of which plug directly into the RH70 slots of the PDP-11/70.

2.2.1 A Board

The A board of the controller is Part Number SU7010401 or SU7010405. This board contains the high-speed bipolar microprocessor, the A cable interface and the Unibus interface. The A board is shown in Figure 2-2. It is the rear board of the four board controller and fits into the PDP-11/70 slot 27, 31, 35, or 39 which are used by the BCT board of the RH70.

The board is a 4-layer pcb with power and ground planes in the inner layers and interconnection on the outer layers. The board dimensions are 15.7 inches high x 8.7 inches wide. The 18 pins of each connector row are designated A through V - excluding the letters G, I, O, and Q from the right to the left. The component side pins are designated 1 and the bottom side pins are designated 2.

2.2.1.1 A Cable Connector

The A board has a 60-pin flat cable connector labeled J1 at the top edge of the board. This connector is for the A cable which daisy-chains control and status information to all the drives. Pin 1 of the connector is located on the outside board edge.

2.2.1.2 Test Connectors

Connectors J2 and J3 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.1.3 Switches

The four DIP switches are used for controller options and configuration, Unibus device register starting address and range, and interrupt vector address. The Unibus address switches are described in Section 4.2 and the option switches in Appendix A. These switches are identified in Table 2-1.

Table 2-1
DIP Switches

Switches	Location	Use
SW1	U62	Option and configuration
SW2	U72	Unibus address range
SW3	U94	Unibus starting address
SW4	U77	Vector address

2.2.1.4 Indicators

The four indicators at the top front edge of the board show the state of the BBSY, SACK, SSYN, and BGIN Unibus signals. These same indicators are available on the BCT board of the RH70 and show Unibus hang-up problems.

2.2.1.5 Toggle Switch

The small toggle switch located along the front edge of the board is a three position switch with the center position being the normally OFF position. In the lower position the extended functions (including format) are enabled. The upper position is not used in most SC71 models and should not be used. For normal operation, the switch should be in the center position.

2.2.1.6 PROM's

The A board has 24 PROM locations along the front edge of the board used by the Control Memory. These are labeled locations U1 to U24. Normally only 12 2K x 4 PROM's are used in the odd locations; the other locations being unused and without sockets. The sequence numbers on the PROM's should be in the same order as the U numbers on the board.

The SC71 can have control memory size other than 2K. By use of 4K-bit and 8K-bit PROM sizes, control stores of 1024 to 4096 words may be achieved as shown in Table 3-1. Pins A, B, and C located by U34 and pins D, E, and F located by U25 must be jumpered accordingly.

Table 2-2
Control Memory Configurations

Words	Jumper	Size	Locations	Address
1024	A - D & E - F	1024 x 4 -	Odd	0-1023
2048	A - D & E - F	1024 x 4 1024 x 4	Odd Even	0-1023 1024-2047
2048 (normal)	A - C & D - E	2048 x 4 -	Odd	0-2047
3072	A - C & D - E	2048 x 4 1024 x 4	Odd Even	0-2047 2048-3071
4096	A - C & D - C	2048 x 4 2048 x 4	Odd Even	0-2047 2048-4095

2.2.2 B Board

The B board of the controller is Part Number SU7010402 and incorporates all of the disk data circuitry, four B cable drive interfaces and the Cache bus address interface. Also included is a -5 volt power supply for the A cable and B cable transmitter and receiver circuits.

The B board is shown in Figure 2-3. The board is a two sided pcb with the same dimensions and backplane connector arrangement as the A board. The board plugs into slot 26, 30, 34, or 38 of the PDP-11/70 backplane which are used by the AWR board of the RH70.

2.2.2.1 B Cable Connectors

The B board contains four 26-pin flat cable connectors labeled J1, J2, J3, and J4. These connectors are for the radial B cables to each of four physical drives which may be attached to the controller. Pin 1 of these connectors is located at the left end of the connector adjacent to the J numbers. They are all interchangeable.

2.2.2.2 LED Indicators

The B board contains four LED indicators which provide the following information:

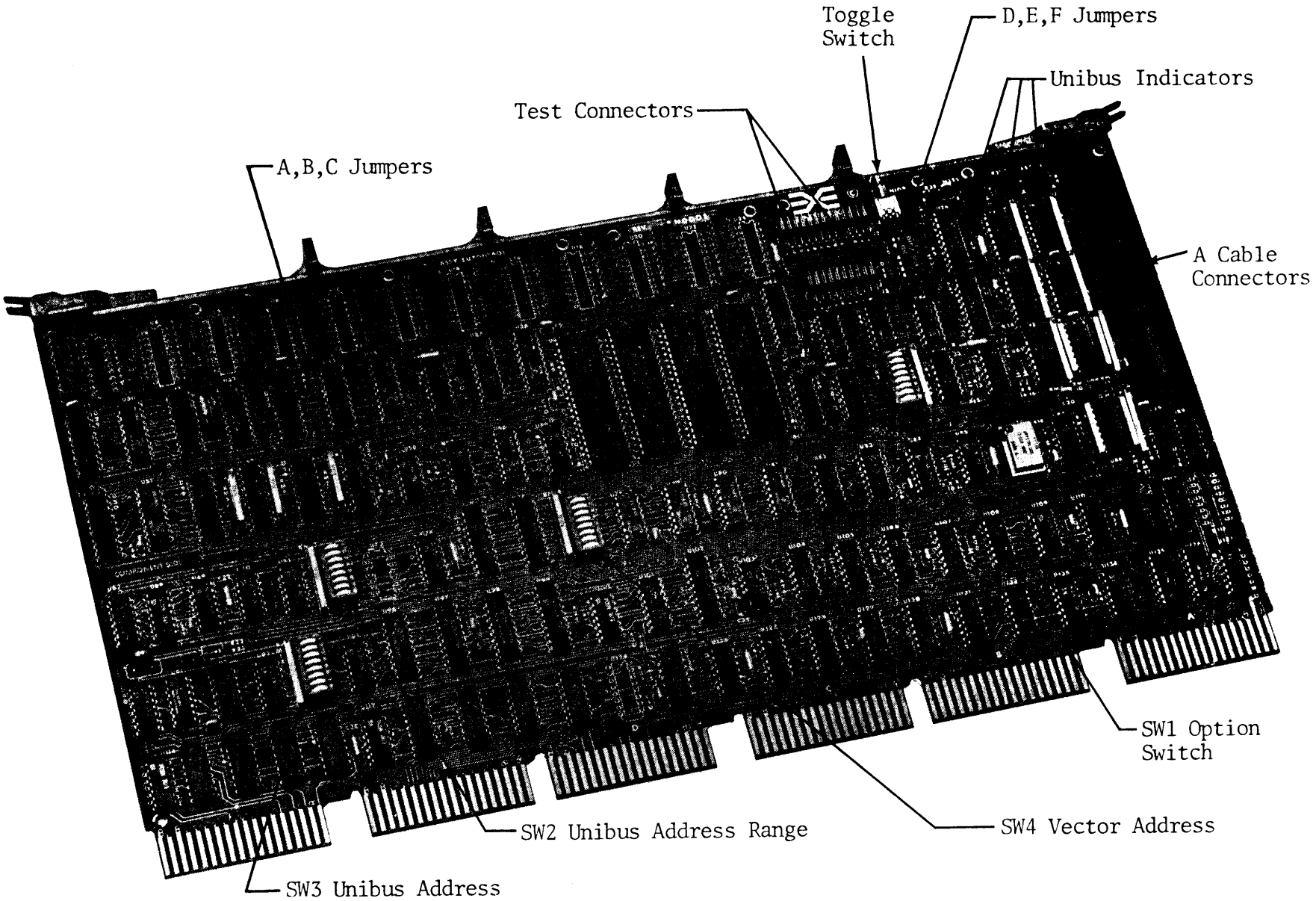
FAULT	-	Indicates controller fault or no drive
DIAGNOSTIC MODE	-	Indicates controller in self-test mode
WRITE	-	Indicates disk write activity
READ	-	Indicates disk read activity

2.2.3 C Board

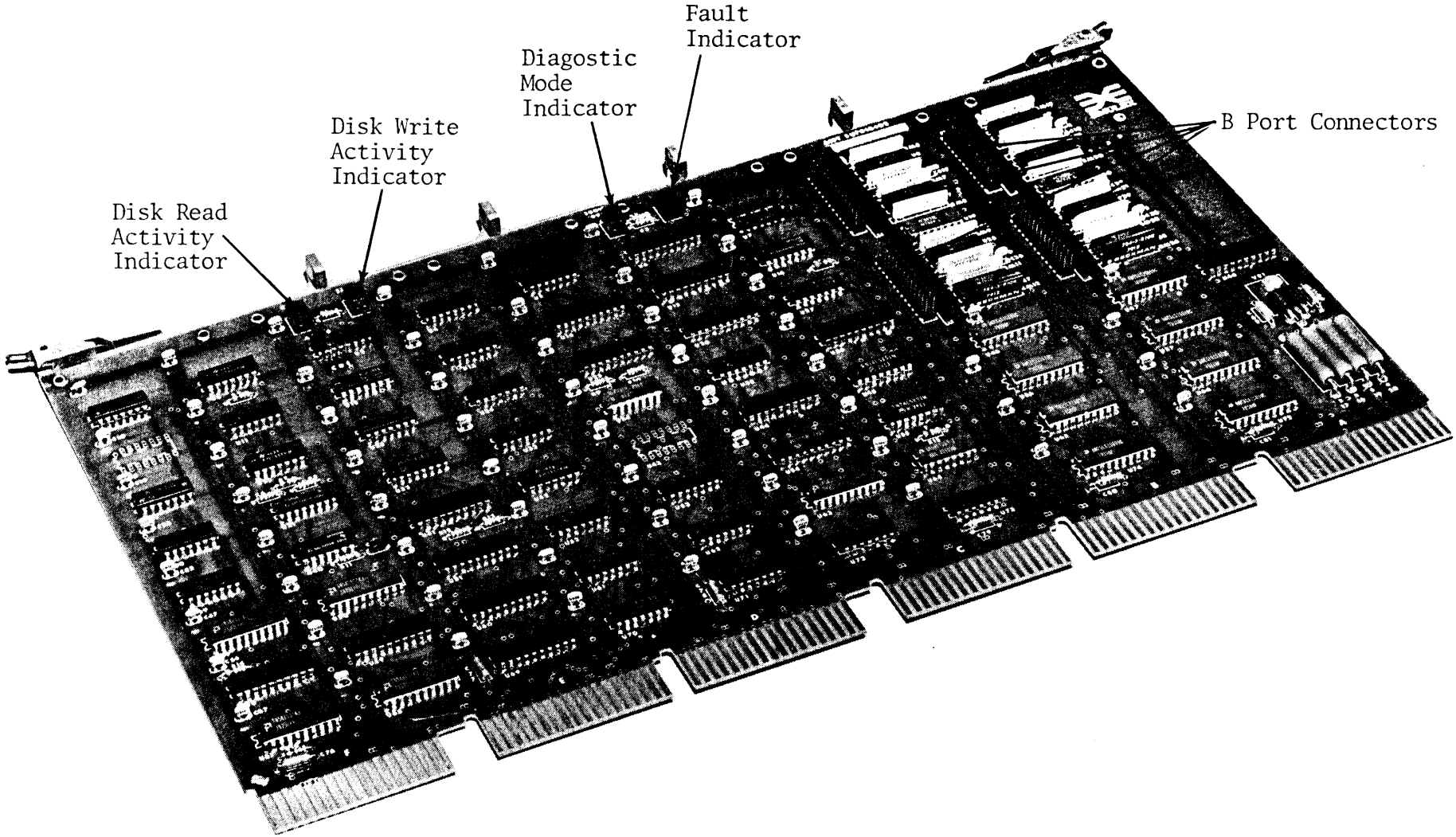
The C board of the controller is Part Number SU7010403 and SU7010406, and contains the 1K buffer and the Cache bus data interface including the Cache control and status information. The C board is shown in Figure 2-4. The board is a two sided pcb with board dimensions and backplane connector arrangement the same as the A board. The board plugs into slot 24, 28, 32, or 36 of the PDP-11 backplane which are used by the MDP board of the RH70. There are no switches or connectors on this board. A single LED indicator indicates when a parity error occurs in the buffer.

2.2.4 CST Board

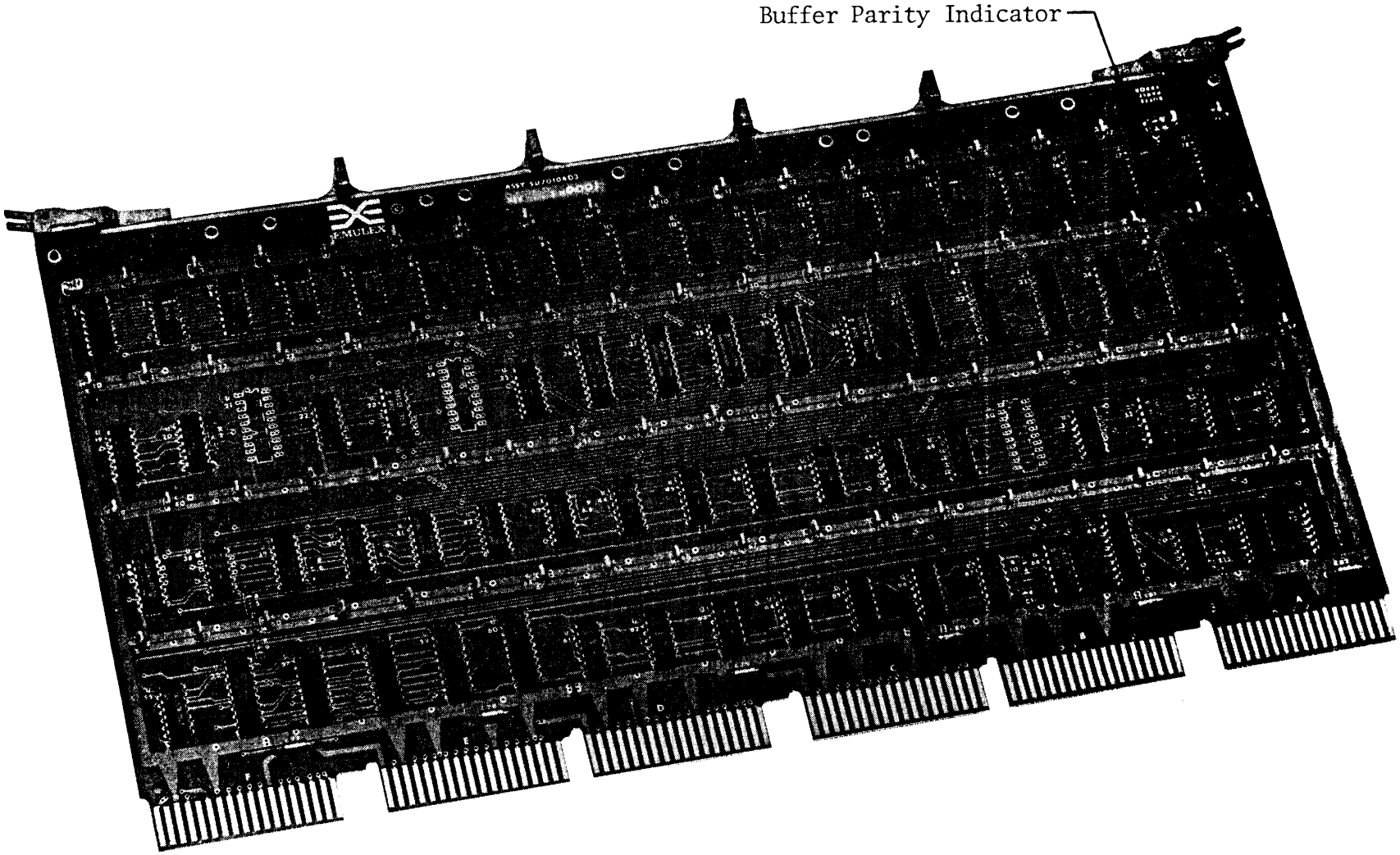
The small interconnect board is used to pick up several RH70 signals in an otherwise unused RH70 slot and to retransmit them to one of the three hex boards. This board is inserted into the D, E, and F connectors of slot 25, 29, 33, or 37 which are normally used by the CST board of the RH70. The board is shown in Figure 2-5.



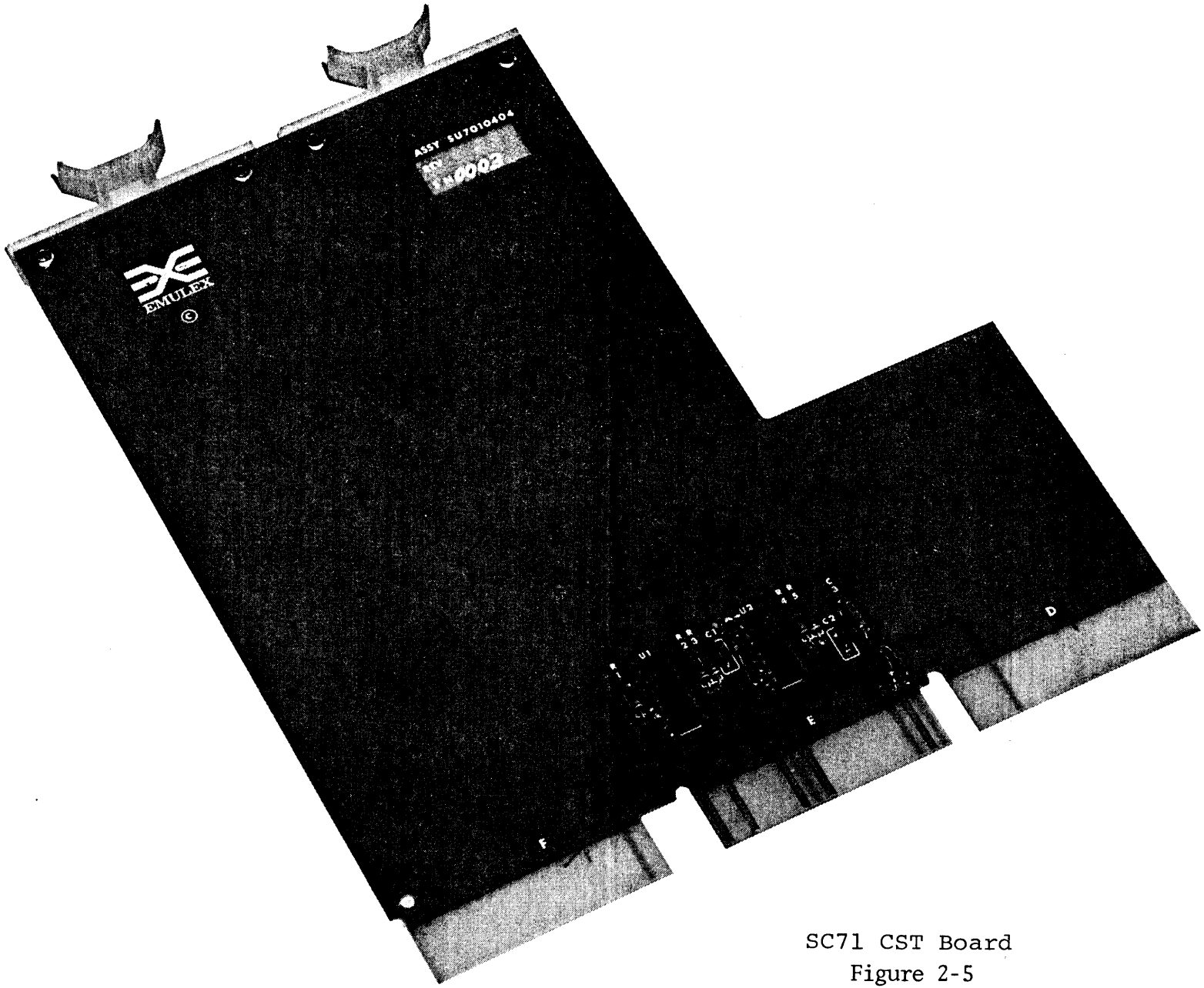
SC71 A Board
Figure 2-2



SC71 B Board
Figure 2-3



SC71 C Board
Figure 2-4



SC71 CST Board
Figure 2-5

2.3 INTERFACES

2.3.1 Disk Interface

The controller's disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD interface and is compatable with these drives electrically and in timing.

The following defines the electrical interface and the recommended cables.

2.3.1.1 Drivers and Receivers

The drivers for the A and B cables are MC3453, which are equivalent to the 75110A. The receivers are MC3450 quad differential receivers, which are equivalent to 75108 receivers. The lines of the A cable are terminated with 82 ohms to ground. The lines of the B cable are terminated with 56 ohms to ground.

2.3.1.2 A Cable

The 60-conductor A cable is daisy-chained to all drives and terminated at the last drive. The signals in this cable are listed in Table 2-3 along with their function when the control tag (Tag 3) is asserted. The A cable should be 30 twisted pair flat cable with an impedance of 100 ohms and an accumulative length of no greater than 100 feet.

2.3.1.3 B Cable

The 26-conductor B cable is radial to all drives and contains the data and clock signals. The signals and grounds in this cable are listed in Table 2-3. The B cable should be 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 50 feet.

2.3.2 Unibus Interace

The controller interfaces to the PDP-11/70 via the RH70 slot and not an SPC slot as with a Unibus type controller. The Unibus consists of 18 address lines and 16 bi-directional data lines, plus control signals for data and interrupt vector address transfer and for becomming bus master for interrupts.

2.3.2.1 BR (Interrupt) Priority Level

The controller is hardwired for BR5. The other three Bus Grant signals are jumpered through.

Table 2-3
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	Address Mark Found		From
21,51	Busy (dual-port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Hold		To
59	Power Sequence Pick		To
B Cable:			
8,20	Write Data		To
6,16	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
10,23	Seek End		From
22,9	Unit Selected		From
12,24	Index		From
13,26	Sector		From

2.3.2.2 Register Address

DIP switches are provided on the A board for assigning the starting address of the address block to be used by the controller and the range of addresses. SW3 located at U94 selects a block of 64 word addresses. SW2 located at U72 selects the starting address in the block of 64. The high-order five bits of the Unibus address (A17-A13) are always decoded as 1-bits and the low-order two bits are "don't care" conditions. Table 2-4 shows the switches for establishing the starting address of a block of 32, 16, 8 or 4 registers. Table 2-5 gives the switch settings to establish the basic block size, while Table 2-6 gives switch settings for smaller block sizes. If SW2-5 is ON, SW2-6 must also be ON; if SW2-4 is ON, SW2-5 and SW2-6 must be ON. For example, placing SW2-7 ON with SW2-4, SW2-5 and SW2-6 all OFF, estblishes a register block size of 22 (32 - 10) registers.

2.3.2.3 Interrupt Vector Address

The DIP switch SW4 located at U77 sets the interrupt vector address. Bits 15-9 of the address are assumed to be zeros, so the vector address range is 0-774. The low-order two bits are also assumed to be zero, since the vector address must start on a double word address. Table 2-7 gives the switch assignments for the remainder of the vector address.

2.3.2.3 DCLO and INIT Signals

The DCLO and INIT signals both performed a controller clear. The self-test is performed only if DCLO has been asserted.

2.3.3 Cache Interface

The Cache Bus address and control signals are on the B board and allow for a 22-bit memory address and control for writing and reading a single or double word to or from memory. The Cache Bus 32-bit data interface is on the C board.

Table 2-4
Register Block Starting Address

Unibus Address Bit	Address Switch	Comments
A12	SW3-7	Switch ON = 1
A11	SW3-6	Switch OFF = 0
A10	SW3-5	
A09	SW3-4	
A08	SW3-3	
A07	SW3-2	
A06	SW3-1	
A05	SW2-3	(SW2-6 ON)
A04	SW2-2	(SW2-6, -5 ON)
A03	SW2-1	(SW2-6, -5, -4 ON)

Table 2-5
Register Block Size

Block Size	Switches ON	Switches OFF
32		SW2-6, SW2-5, SW2-4
16	SW-6	SW2-5, SW2-4
8	SW2-6, SW2-5	SW2-4
4	SW2-6, SW2-5, SW2-4	

Table 2-6
Register Block Limit

Inhibit Function	Switch	Function
A04 * A03 (Switch ON=Inhibit)	SW2-8 ON	Subtract last 8 words from block
A05*(A04+A03) (Switch ON=Inhibit)	SW2-7 ON	Subtract last 10 words from block

Table 2-7
Interrupt Vector Address Switches

Unibus Data Bit	Vector Address Switch	Comments
D08	SW1-8	Switch OFF = 0
D07	SW1-7	Switch ON = 1
D06	SW1-6	
D05	SW1-5	
D04	SW1-4	
D03	SW1-3	
D02	SW1-2	(not used)

2.4 DISK FORMAT

2.4.1 Disk Organization

The SC71/B1 handles only one logical RM drive per physical drive, Except one fixed heads of Winchester drives are involved. The number of cylinders and tracks for each drive can be configured by the Configuration PROM. The number of sectors is always 32.

2.4.2 Sector Organization

Figure 2-6 shows the sector format used by the controller. Each track of 20,160 bytes is divided into 32 sectors of 630 bytes. The four byte header is preceeded by a preamble of 30 bytes ending in the sync byte and is followed by a two byte CRC. The 256 word data field is preceeded by a preamble of 20 bytes ending in the sync byte, and is followed by four bytes of ECC. This format is compatible with that of the DEC RM02/RM03/RM05.

If the actual size of the useful data information is less than 256 words, the remainder of the data field will be filled with 0's until 256 words have been written. During disk formatting procedures, each data track is located and recorded with header information by means of the Write Header and Data command. A disk pack should be formatted and the format verified before any real data is written on it. Once formatted, individual or groups of sectors should not be reformatted unless absolutely necessary.

2.4.3 Header

2.4.3.1 Header Description

Figure 2-7 shows the header format, which consists of the following three words:

Word One -

This word contains the cylinder address. It also contains a 1-bit in bit 12 to identify 16-bit format to the software and 1-bits in bit positions 14 and 15 to identify a good sector.

Word Two -

The low-order five bits of this word contain the sector address. Each track on the drive contains 32 sectors. The least significant six bits of the upper byte of this word contain the track address.

Word Three -

This is the CRC word which is generated and checked by the controller logic. This word is not available to the software.

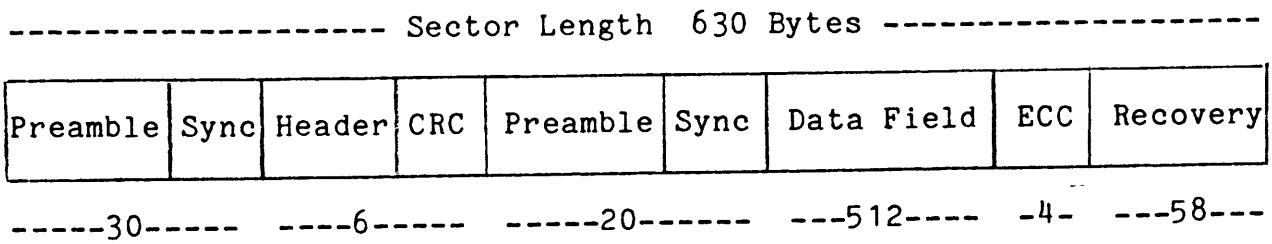
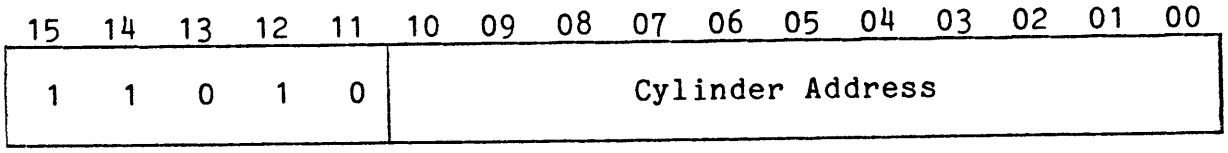
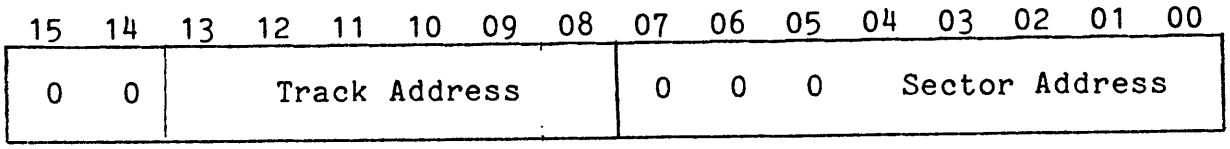


Figure 2-6
Sector Format

Header Word 1:



Header Word 2:



Header Word 3:

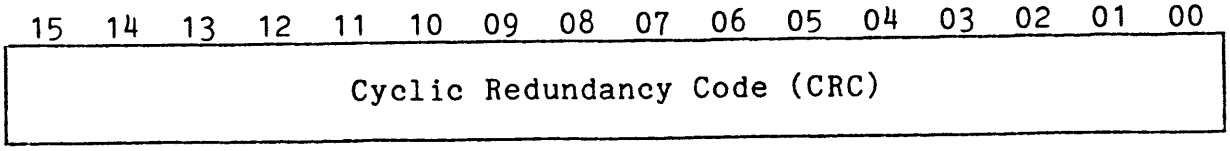


Figure 2-7
Header Format

2.4.3.2 Header Field Handling

After the drive reports that it is on cylinder, the controller locates the desired sector by means of the sector counters for each drive that are maintained in the controller. The controller compares the first two words of the header against the desired track, sector and cylinder and then checks the CRC word for errors. An error in the header field is indicated by turning on the appropriate error bit in the error register (format error, header compare error, bad sector error or CRC error). A header error is only valid when the sector count field of the RMLA register and the sector field of the RMDA have already matched. It is immaterial where a CRC error occurs in the header field since the controller cannot determine its location in the field. However, software may read the header to memory by means of a Read Header and Data command. The header compare may be inhibited by setting the HCI bit in the RMOF register.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Clearing the Controller

The controller has the following clearing methods:

a. Controller Clear - Controller Clear is performed by writing a 1-bit into the CLR bit (bit 5 of RMCS2) or Unibus INIT. This causes the following to be cleared:

   - RMCS1 bits 0-6, 8-9, 12-15; RMCS2 bits 0-5, 7-15; RMBA; RMBAE; RMCS2 bits 4-15. Sets RMCS2 bit 6 and RMCS1 bit 7.

   - In all drives: RMER1; RMER2; RMDA; RMAS ATA bit; RMEC2; RMDS ATA, ERR and LST bits; RMMR1 bits 0-2, 4-15. Sets bit 3 of RMMR1.

b. Error Clear - The Error Clear is performed by writing a 1-bit into the TRE bit (bit 14 of RMCS1). This causes a clearing of RMCS1 bits 13 and 14, and bits 8 through 15 of RMCS2. Also clears the SC bit (bit 15 of RMCS1) if RMAS=0.

c. Drive Clear - The Drive Clear is a command. (Code 11.) This causes the following registers in the drive selected by U2-U0 to be cleared:

   - RMER1; RMER2; RMAS ATA bit; RMEC2; RMDS ATA and ERR bits; RMMR1 bits 0-2, 4-15. Sets bit 3 of RMMR1.

2.5.2 Interrupt Conditions

The controller generates an interrupt on the following conditions:

a. Upon termination of data transfer if interrupt enable is set when the controller becomes ready.

b. Upon assertion of attention or occurence of a controller error (SC being set) while the controller is not busy and the interrupt enable is set.

c. When the program writes 1 into IE and RDY at the same time. Note that this can be done by Read-Modify-Write instructions (BIS, BIC, etc.) which set the IE bit.

2.5.3 Termination of Data Transfers

A data transfer which has been successfully started may terminate in the following ways:

a. Normal Termination - Word count overflows to 0 and the controller becomes ready at the end of the current sector.

b. Controller Error - An error occurs in the RMCS2 register bits 8 through 15. Any of these errors sets TRE which terminates the data transfer immediately and makes the controller ready.

c. Drive Error - The ERR bit in the RMDS register and at least one bit in an RMER1 or RMER2 register are set. TRE is also set and the controller becomes ready. The ATA for the drive doing the data transfer becomes asserted.

d. Program-Caused Abort - By performing a Controller Clear or a RESET instruction, the program can cause an abort of any operation. Status and error information is lost when this is done, and the controller and drive become ready immediately.

2.5.4 Ready Bits

RDY is the ready indicator for the controller. When RDY = 1, the controller is ready to accept a data transfer command. RDY is reset when the controller is doing a data transfer command. DRY is the ready indicator for the selected drive and is the complement of the drive's GO bit. To successfully initiate a data transfer command, both of these bits must be asserted. However, a non-data transfer command (Search, Drive Clear) may be issued to a drive at any time DRY is asserted regardless of the state of the RDY bit.

When a data transfer command is successfully initiated, both RDY and DRY become negated. When a non-data transfer command is successfully initiated, only DRY bit becomes negated.

The assertion of RDY after the execution of a data transfer command will not occur until the DRY bit is set and the controller is done. RDY is asserted on the completion of the last memory cycle (or at the time of an abort condition) and the last disk transfer.

If any command other than Drive Clear is issued to a drive which has ERR asserted, the command is ignored by the drive. If a Data Transfer command is issued to a drive which has ERR asserted, the drive does not execute the command and the missed transfer error (MXF, bit 9 in RMCS2 register) is set.

2.6 DUAL CONTROLLER OPERATION

SMD drives may be equipped with a dual port option which provides the capability for two controllers (generally on separate computers) to access the drive. The SC71/B1 controller supports this type of operation as a standard feature. Most of the dual-port funtions of the DEC controller being emulated are supported, and those which are not should be transparent to a properly written dual-port driver.

2.6.1 Dual-Port Drives

The two drive ports are known as Channel I and Channel II. Each channel has a disable switch which disables the port and prevents the computer from having access to it. Access to the drive in dual-port operation is switched back and forth between the two controllers under program control of the two computers involved in a manner described in the following sections. Table 2-3 summarizes the register responses in dual-port operation.

2.6.2 Unseized State

The unseized state is when the drive is not connected to either controller. The CPU must issue a request for the controller to seize the drive. This request is done in one of the following ways:

a. Writing into any drive register, including read-only registers.

b. Reading any drive register except RMCS1.

c. Writing a one-bit into the drive's ATA bit in RMAS.

2.6.3 Seized State

The drive is seized when it is logically connected to one of the controllers. At that time the DVA (RMCS1, bit 11) is set indicating that the drive is ready to communicate with the controller which has seized it. If the drive is seized by the other controller, the DVA bit is reset and all the drive registers read as 0's and any write to a register is ignored. Any attempt to seize a drive which is busy with the other port will cause the request to be remembered and acted upon when the drive is released

by the other controller.

2.6.4 Returning to the Unseized State

The drive is released and returned to the unseized state by issuing a release command. In addition, a one second timer in the controller will timeout and release the drive if one of the events listed in section 2.6.2 for seizing the drive is not performed periodically to keep resetting the timeout timer.

When the controller sees a previously busy drive becoming unseized, it checks its request flag. If the drive had been previously requested while busy on the other port, the controller will seize the drive, set the DVA bit and set the ATA causing an interrupt to the CPU if the IE bit is set. If the CPU does not respond to the attention within one second the drive will be released, but the ATA remains set.

2.6.5 DEC Compatability

The SC21/B controller differs from the equivalent DEC controller in three important areas. First, there is no neutral state. Since the controller does not have instantaneous access to all drives at the same time (a limitation of the daisy-chained A cable and the microprocessor organization of the controller), then if the drive is not currently seized the controller assumes it is busy on the other port. The DEC controllers can switch from neutral to seized state within the time required to do a single read or write of a drive register. In that case no ATA is set and the drive would appear to have been already seized.

Second, the release command is not instantaneous since the controller takes a few microseconds to execute the command. During this time the drive will appear to be still seized and the GO bit will be set.

Third, during a data transfer the timeout timers will not operate and the drives can not be polled to see if they are not busy. Therefore no drives are seized or released during the execution of a data transfer.

The software driver should not issue a Release command and then attempt to save the current status of a drive, since the Release command has a drive clear implied within it, and the reading of the drive's registers will set the seize request. In order to allow the other controller time to poll the drive, the CPU should not communicate with any of the released drive's registers until required to seize the drive again.

2.6.6 Dual-Port Drives in Single-Port Mode

When using an operating system which does not have dual-port drive software support, it may still be advantageous to use dual-port drives while operating in the controller in single-port mode. This

will allow for a non-dynamic type of operation between two CPU's. In this type of operation the controller does not unseize the drive and, in effect, it is seized by both controllers all the time.

The one second timeout timer (and the release command) operate exactly as stated in Paragraph 2.6.4. Even when released a drive will still appear to be seized to the releasing controller. No attention is generated when the other controller finds the drive not busy. Should a command be issued to a controller while a drive is busy on the other port, the controller will wait until the drive becomes unbusy before executing the command. No timer exists in this case.

The mode of operation eliminates the need for manually switching the drive from one controller to another.

2.7 FIXED HEAD OPERATION

Certain Winchester type non-removal type disks have an optional one or two megabytes of fixed head storage. This is useful for special applications such as swapping storage, since the zero seek time means quicker access time to the fixed head storage. This fixed head option feature is supported only by the SC71/B1 controller.

2.7.1 Drive Numbering

Drives having the fixed head option will have two logical RM disks per physical drive. The movable head portion will have unit numbers 0 to 3 and the corresponding fixed head portion will have unit numbers 4 to 7. Unit 4 is on the same drive as unit 0 and has an A cable address of 0.

2.7.2 Drive Characteristics

The fixed head drive has the same number of tracks (heads) as the movable head drive. The number of cylinders will depend on the size of the fixed head option. In some configurations the last cylinder may not have a full number of heads.

Table 2-8
Register Access on Dual Controller Operation

Controller Action / Drive State:	Response With Respect To Action On Ch. I
Read RMCS1	
Drive Not Seized:	Reads the controller portion of the RMCS1 only. The drive's portion is read as all zeros. No request flag is set.
Drive Seized by Ch. I:	DVA = 1; reads the register.
Drive Seized by Ch. II:	DVA = 0; reads all zeros for the drive's portion of the register. No flags set.
Write RMCS1	
Drive Not Seized:	The function code is ignored, and a port request flag is set.
Drive Seized by Ch. I:	Loads the function code. (Switches to unseized if the function is a Release).
Drive Seized by Ch. II:	The function code is ignored, and a port request flag is set.
Read RMDS	
Drive Not Seized:	Reads all zeros and sets request flag.
Drive Seized by Ch. I:	Reads the status bits; PGM = 1; DPR = 1.
Drive Seized by Ch. II:	Reads all zeros and sets request flag.
Read any other drive register	
Drive Not Seized:	Reads all zeros and sets request flag.
Drive Seized by Ch. I:	Reads the register.
Drive Seized by Ch. II:	Reads all zeros and sets request flag.
Write any drive register	
Drive Not Seized:	The write is ignored, and a port request flag is set.
Drive Seized by Ch. I:	Loads the register.
Drive Seized by Ch. II:	The write is ignored, and a port request flag is set.

Section 3
INSTALLATION

This section describes the step-by-step procedure for installation of the SC71/B1 Disk Controller in a PDP-11/70 system.

3.1 INSPECTION

A visual inspection of the board is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROM's should be examined carefully to insure that they are firmly and completely seated in the sockets.

3.2 DISK DRIVE PREPARATION

The disk drive must be configured for the proper number of sectors, and have an ID plug or address selection switches properly configured.

3.2.1 Sectoring

The disk drive must be configured for 32 sectors which is equivalent to a sector size of 420 dibits. The exact method of entering this 420 count into the logic of the drive will differ from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure.

For CDC drives, a value of 419 should be entered into the sector length switches by closing switches 0, 1, 5, 7, and 8.

3.2.2 ID Plug

An ID plug in the range of 0-3 should be placed in the drive. Be careful that no two drives have the same number. Some drives have their address selected by means of switches on one of the logic cards and do not use an ID plug.

3.2.3 Sector and Index Modifications

It may be necessry to move the sector and index signals from the A cable to the B cable. See Section 3.3.3. Instructions for doing this for commonly used drives is included in Appendix C.

3.3 CONTROLLER SETUP

Several configuration setups must be made on the controller before inserting it into the chassis.

3.3.1 Controller Address Selection

Register address location and range is setup by means of DIP switches SW2 located at U72, and SW3 located at U94 on the A board.

The normal address of 776700 is obtained by placing switches SW3-6, 7, 8, 10, 11 and 12 ON and switch SW2-7 ON. The alternate address of 776300 is the same except SW3-8 is left OFF. Refer to Section 2.3.2.2 for detailed information on these switch settings. The SC71/B1 controller requires 22 registers with the address of the first register having the low-order six bits equal to zero.

3.3.2 Interrupt Vector Address

The interrupt vector address is programmed by means of switch SW4 located at U77 on the A board. The normal controller vector address of 254 is obtained by placing switches 2, 3, 5, 7 ON. The alternate vector address of 150 is obtained by placing switches 3, 5, and 6 ON. Refer to Section 2.3.2.3 for detailed information on these switches.

3.3.3 Index and Sector Pulse Selection

The SC71/B1 controllers are designed to have the Index and Sector signals on the B cable from each physical drive. The signals are necessary for proper operation of the sector counters associated with each drive. The RM emulation requires an updated sector counter which can be read by the PDP-11. Failure to have a valid sector counter may cause incorrect operation of rotational position sensing software.

Depending on the disk drive, the index and sector pulse signals may not be on the B cable. For example, the CDC drives standardly provide the index and sector signals only on the A cable, but they may be moved to the B cable by minor rewiring of the drive backplane or by ordering this configuration from the factory.

It is possible to operate with the index and sector signals on the A cable. When operating in this manner there is some loss of capabilities and performance including: the Search command operates as a Seek; the sector counter in RMLA will be incorrect; and each transfer must wait for an index pulse to sync-up the sector counter. Also, some of the lower level diagnostics will produce some errors.

The controller is configured at the factory for the Sector and Index on the B cable. It can be changed to A cable operation by leaving out jumper F - G on the B board and installing jumpers G - H and J - K on the A board.

3.4 PHYSICAL INSTALLATION

3.4.1 RH70 Slot Selection

The SC71/B1 controller may be placed into any one of the available RH70 positions. There are four prewired RH70 positions in the PDP-11/70 computer. RH70 A (forward controller position) is powered by its own supply. RH70 B and C are powered by the same supply. The RH70 D is powered along with the SPC Unibus slots.

Figure 3-1 shows the PDP-11/70 computer chassis with a single SC70 installed in slots 24, 25, 26 and 27. Cache Bus request priorities between RH70 positions is described on page VI-4-13 of the DEC KB 11 Processor Manual.

3.4.2 Mounting

The controller board should be plugged into the PDP-11/70 backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the boards with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly in the throat of the connector before attempting to seat the board by means of the extractor handles.

The following procedure should be used in installing the four boards and the drive cables:

1) Remove the bus grant card in the slot 27, 31, 35, or 39 to be used by the SC71 A board.

2) Insert A board fully into the slot.

3) Plug the drive A cable into the connector on the tip of the A board. The A cable should lie in the cableway at the top of the PDP-11/70 chassis underneath the memory cables from the processor. The cable should pass through the strain relief at the rear of the chassis, and pin 1 of the A cable connector should be toward the outside of the chassis. Pin 1 end of the connector will have some type of identification mark. If twist-and-flat cable is used, the borwn-brown followed by the red-brown colored twists are on the pin 1 side of the cable.

4) Insert B board three-quarters of the way into the slot in front of the A board.

5) Connect B cables. B cables should lie in the cableway above the A cable, and should pass through the cable strain relief at the back of the chassis. Pin 1 of the B cable connector (black stripe edge of the cable) should be toward the outside of the chassis. The B cables may be plugged into any one of the four B cable connectors as they are all identical in function.

6) Fully insert B board and properly dress B cables into cableway.

7) Install CST board into slot in front of B board.

8) Insert C board into slot in front of the CST board.

3.5 CABLING

The subsystem cabling of the drives and controller is shown in

Figure 3-2.

3.5.1 A Cable

The 60-wire A cable should be plugged into the connector on the A board of the controller and wired to the first drive. If more than one drive is used, it is then daisy-chained to the other drives. The last drive on the A cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board connector is on the left. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cable will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The cable will normally egress to the rear of the controller.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.

3.5.2 B Cable

Each drive must have a 26-wire B cable wired from the drive to one of the B ports of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe.

NOTE: Observe the same caution on connector reversal given in paragraph 3.5.1.

3.5.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

3.6 TESTING

3.6.1 Self-Test

When power is applied to the CPU, the controller will automatically execute a built-in self-test. This self-test is not executed with every bus INIT but only on powering-up. If the self-test has been executed successfully, the FAULT LED on the top edge of the controller board will be OFF or flashing. The FAULT LED flashes when the controller cannot properly address at least one drive after successfully executing its self-test. This will occur if the A and B cables are not properly plugged in, a drive is not powered-up with a code plug, or two drives have an identical code plug. If the FAULT LED is ON steadily the controller did not pass its self-test and the controller cannot be addressed from the CPU.

3.6.2 Register Examination

After powering-up the CPU and noting that the FAULT indicator is not ON steadily, a quick check should be made to ensure that the controller registers can be read from the computer console. The RMCS1 register will contain 004200 if the drive is available and 000200 if it is not. If the CPU has a console emulator all the registers of the controller should be examined.

3.6.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing headers and zero data in all sectors of the disk. This format does not verify the data or headers and does not write a Bad Sector File on the last track of the last cylinder.

If the drive is on-line, the formatting is carried out as follows:

1) INIT the controller from the PDP-11 console.

2) Deposit the drive number (if other than 0) in RMCS2 at 776710 or 776310.

3) Deposit a 000021_8 (Read-in Preset command) in RMCS1 at 776700 or 776300. This sets Volume Valid.

4) Deposit a 177777_8 in RMHR at 776736 or 776336 to enable the optional Format command. This step is not necessary with a SC70/B3.

5) Deposit a 000077_8 (Format command) in RMCS1 at 776700 or 776300. (The Format toggle switch on the A board must be in the down position on a SC70/B3.) The WRITE activity indicator on the left side of the board will flash as long as the formatting is underway.

6) Examine RMDS at 776712 or 776312 to see if the drive's ERR (Bit 14) is set indicating an error. If there is an error resulting from the format operation, RMER1 and RMER2 should be examined to determine the cause of the error and RMDA and RMDC should be examined to see how far the formatting

progressed.

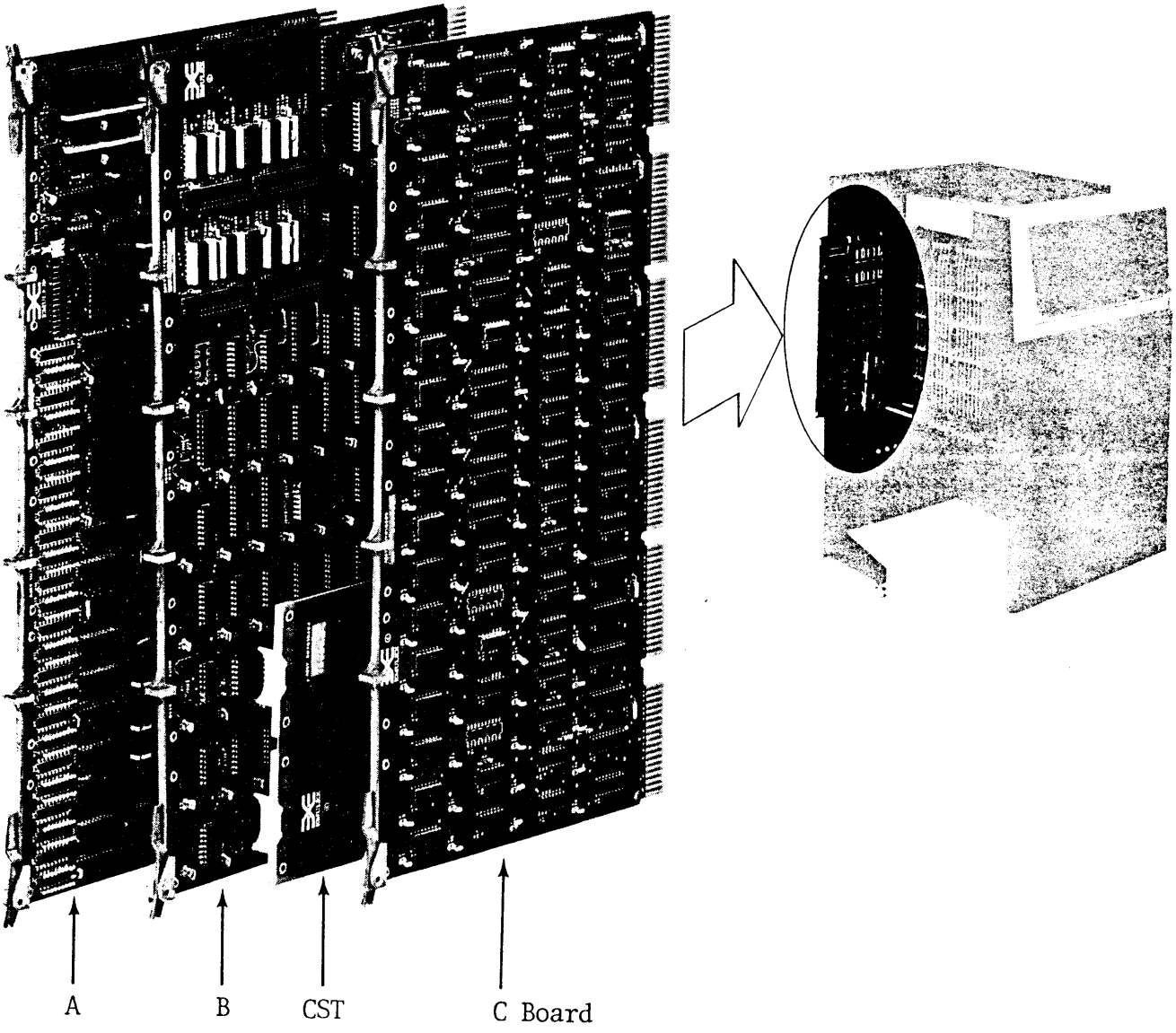
3.6.4 Diagnostics

The DEC RM02/RM03 diagnostics should be run. Generally it will be necessary to run only the Formatter and the Performance Exerciser. If the drive is other than an 80 megabyte with 823 cylinders and 5 tracks it will be necessary to patch the diagnostics as shown in Section 6. Section 6 also describes how to run the diagnostics.

If the Formatter diagnostic is run on an unformatted disk, it will report five errors in trying to read the Bad Sector File before it will proceed.

3.7 OPERATING SYSTEM PATCHES

If the disk drive is a size different than that of the DEC disk for the selected Drive Type Code, it will be necessary to patch the operating system. RSTS/E patches can be found in Appendix D and RSX-11M patches can be found in Appendix E.



SC71 Board Set
Figure 3-1

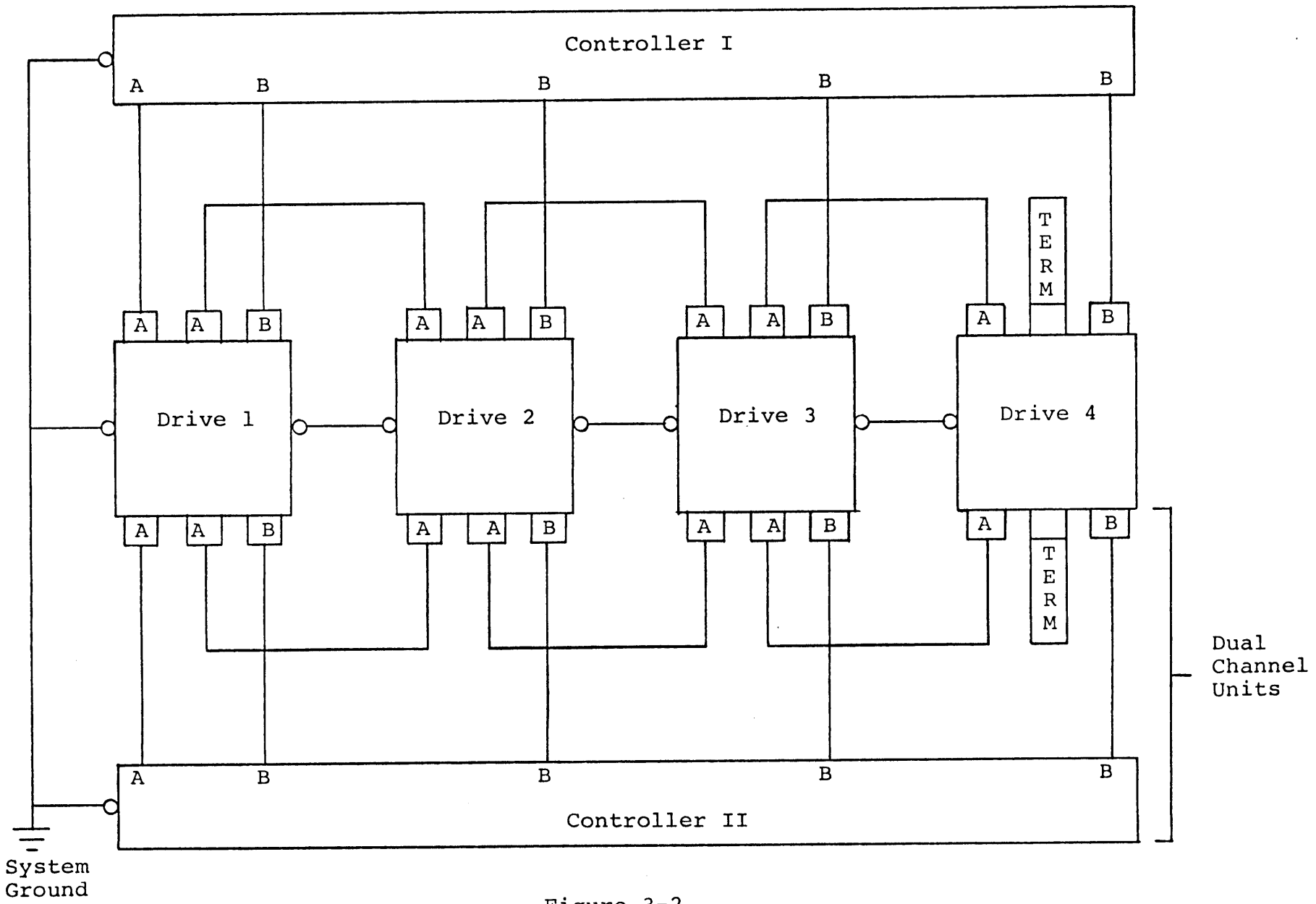
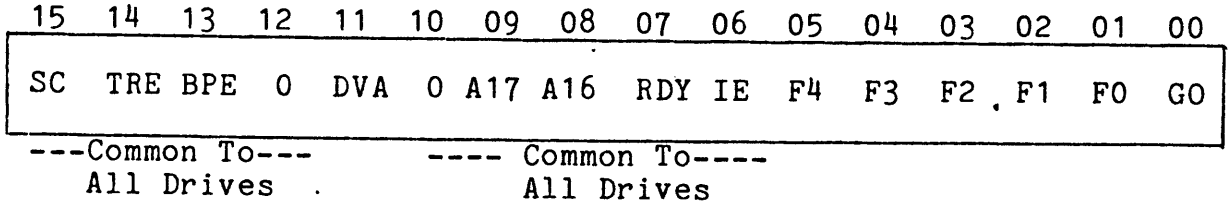


Figure 3-2
Unit Cabling

There are 22 device registers in the SC71/B1. These are used to interface the controller to the drives and the computer. The registers are loaded and/or read under program control in order to initiate selected disk commands and monitor status and error conditions. Most registers can be written into with word or byte operations.

The RMWC, RMBA, RMCS2, RMDB, RMBAE, RMCS3 and bits 15-12 and 10-6 of RMCS1 are common to all drives. Loading and reading of these registers is independent of the unit selected. A separate set of the other registers and bits 11 and 5-0 of RMCS1 exists for each of the drives. Loading and reading of these registers is dependent on the drive selected by the unit number in RMCS2. In addition, the eight ATA bits in RMAS are each associated with an individual drive. Any attempt to write into the drive registers (except RMAS) while the drive's GO bit is asserted will cause a register modification refused error and the register is not modified.

4.1 CONTROLLER/STATUS REGISTER 1 (RMCS1) 776700



The RMCS1 register can be read or written by program control, and is used to store the current disk command function code and operational status of the controller. Setting the GO bit will cause the controller to recognize the function code in the register and initiate the operation for the corresponding drive. The actual start of execution of the command does not begin when the function code is loaded into the control register but commences when the controller has finished any previous operation and polls through the drive RMCS1's in search of a command needing initiation.

Special Condition (SC) - Bit 15

This read only bit is set as long as TRE in RMCS1 or any of the drive's ATA bits are set. This bit causes a CPU interrupt if IE is also set.

Transfer Error (TRE) - Bit 14

This read/write bit is set by BPE, DLT, WCE, UPE, NED, NEM, PGE, MXF, or a drive error during a data transfer. Writing a 1 into the bit causes the transfer error bits to be cleared. They are also cleared at the start of every data transfer operation.

Buffer Parity Error (BPE) - Bit 13

The read-only bit is set if the controller detects a parity error when accessing its own internal buffer. It can be cleared only with an INIT.

Drive Available (DVA) - Bit 11

This read-only bit is set when the drive is seized by the controller. When not in dual-port mode, the drive is seized as long as it is powered-up.

Extended Bus Address (A16, A17) - Bits 8, 9

Upper extension of the RMBA register. This two-bit counter is incremented by one everytime RMBA overflows. These bits cannot be altered if RDY = 0 and no error results when attempted.

Ready (RDY) - Bit 7

This read-only bit is reset when the controller starts a Data Transfer Command (codes 51 - 77) and is set at the termination of the data transfer.

Interrupt Enable (IE) - Bit 6

When IE is set an interrupt can be generated when RDY is asserted at the end of a data transfer or by any ATA being asserted. It is reset automatically when the interrupt is accepted by the CPU. When a zero is written into IE by the program, any pending interrupts are cancelled. An interrupt is generated by writing 1's into IE and RDY at the same time. Same as bit 6 in RMCS3.

Function Code (F4-F0) - Bits 5-1

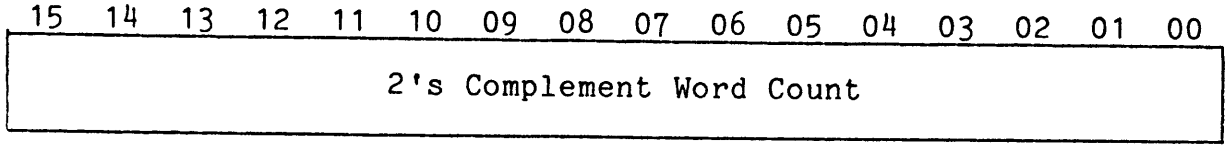
F4-F0 and the GO bit make up the function (command) code which determine the action to be performed by the controller and drive as shown below:

01	No Operation	51	Write Check Data
05	Seek Command	53	Write Check Header and Data
07	Recalibrate	61	Write Data
11	Drive Clear	63	Write Header and Data
13	Release	71	Read Data
15	Offset Command	73	Read Header and Data
17	Return to Centerline	75	Boot (Optional)
21	Read-in Preset	77	Format (Optional)
23	Pack Acknowledge		
31	Search Command		

GO (GO) - Bit 0

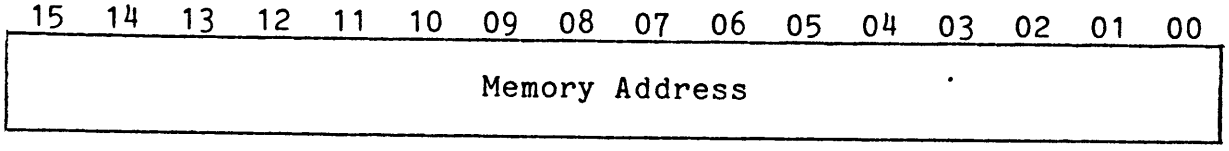
The GO bit must be set to cause the controller to respond to a command. The GO bit is reset after command termination.

4.2 WORD COUNT REGISTER (RMWC) 776702



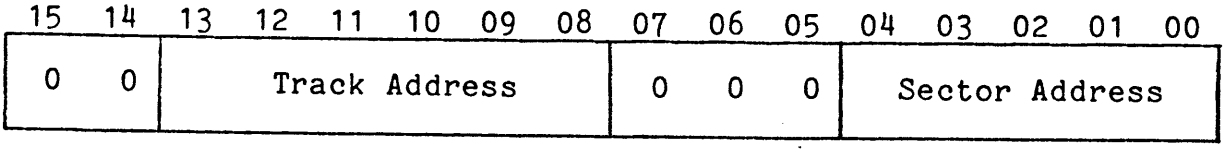
The RMWC register is loaded with the 2's complement of the number of data words to be transferred to or from main memory. The register is incremented by 1 after each word transferred, and accommodates a maximum transfer of 65,536 words. The RMWC register is not cleared by INIT or controller clear.

4.3 BUS ADDRESS REGISTER (RMBA) 776704



The RMBA register is initially loaded with the low-order 16 bits of the memory address for a data transfer. The low-order bit (0) is always forced to a 0. The RMBA register is incremented by 2 after transfer of a word to or from memory, unless the BAI bit is set.

4.4 DISK ADDRESS REGISTER (RMDA) 776706



This register is used to address the sector and track on the disk to or from which a transfer is desired. It can only be loaded as a word. The RMDA is incremented each time a sector of data is transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred. At the end of a transfer, RMDA contains the address of the sector following the last one involved in the data transfer.

The RMDA contains a 5-bit sector counter providing 32 sectors per track. The register also contains a 6-bit track counter which is incremented by one everytime the sector counter overflows. When the sector address and the track address reach their maximum counts, they are reset to 0 and the RMDC is incremented by one. The invalid address error (IAE, RMER1, bit 10) is set if the address in the RMDA is invalid when a data transfer, Seek, or Search function is initiated. The maximum track address is obtained from the selected configuration.

4.5 CONTROL/STATUS REGISTER 2 (RMCS2) 776710

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

The RMCS2 register can be read or written under program control and is used to store the current drive select code and controller operational status. In addition, the register can initiate a controller clear operation.

Data Late (DLT) - Bit 15

This bit cannot normally be set because of the two (three in SC70) sector buffer in the controller. It can be set by accessing RMDB without the appropriate status bit (6 or 7) in RMCS2 set to a 1. This is a read-only bit.

Write Check Error (WCE) - Bit 14

Set when the controller is performing a write check operation and a word from the disk does not match the corresponding word in memory. When the mismatch occurs, the reading of the disk terminates and the WCE bit is set. The memory address displayed in RMBA is the address of the double word following the one which did not match (if BAI is not set). The mismatched data word on the disk is displayed in the data buffer (RMDB). This is a read-only bit.

Unibus Parity Error (UPE) - Bit 13

Set if a parity error occurs in the Unibus memory while the controller is performing a write or write check command. When the error occurs, the RMBA register contains the address of the double word following the word with the parity error (if BAI is not set). This is a read-only bit.

Nonexistent Drive (NED) - Bit 12

Set when the program reads or writes a device register associated with a drive (selected by U2-U0) which is not recognized because of a wrong code plug, not powered up, or is non-existent. This is a read-only bit.

Nonexistent Memory (NEM) - Bit 11

Set when the controller is performing data transfer and the memory does not respond within 10 microseconds. The memory address displayed in RMBA is the address of the double word following the memory location causing the error. This is a read-only bit.

Program Error (PGE) - Bit 10

Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. This is a read-only bit.

Missed Transfer (MXF) - Bit 9

Set if a data transfer cannot be executed (RMDS ERR bit = 1). This is a read-only bit.

Massbus Data Bus Parity (MDPE) - Bit 8

This read-only bit is always a zero.

Output Ready (OR) - Bit 7

Set when a word is present in RMDB and can be read by the program. Cleared by reading RMDB. Any attempt to read RMDB register before OR is asserted will cause a DLT error. This is a read-only bit.

Input Ready (IR) - Bit 6

This read-only bit is always a 1.

Controller Clear (CLR) - Bit 5

When a 1-bit is written into this bit position, the controller is initialized (Paragraph 2.6.1). This is a write-only bit. It is always read as a zero.

Parity Test (PAT) - Bit 4

This read-write bit has no effect on any controller operation. (For diagnostic compatability.)

Unibus Address Increment Inhibit (BAI) - Bit 3

When BAI is set, the controller will not increment the RMBA register during data transfer, causing all data words to be read from or written into the same memory location. This is a read/write bit.

Unit Select (U2-U0) - Bits 2, 1, 0

These bits select one of eight drives for communicating with the CPU. The unit select bits can be changed at any time without interfering with the current operations. These are read/write bits.

4.6 DRIVE STATUS REGISTER (RMDS) 776712

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	OFM

This register contains various status indicators for the drive selected by the unit number in RMCS2. The register is a read-only register.

Attention Active (ATA) - Bit 15

An attention condition will set the ATA bit in this register and the Attention Summary register (RMAS). It is cleared by INIT, controller clear, loading a command with the GO bit set or loading a 1-bit in RMAS register coresponding to the drive's unit number. The last method of clearing the ATA bit will not clear the error indicators.

An attention condition is caused by: an error in the error registers; the completion of a positioning operation; the change of state of the MOL bit; dual-port operation with the drive presently available if previously not available; correct sector identification for the Search command.

Error (ERR) - Bit 14

Set when one or more of the errors in the error registers (RMER1 or RMER2) for a selected drive is set. While ERR is asserted, commands other than Drive Clear are not accepted.

Positioning in Progress (PIP) - Bit 13

Set when a positioning command is accepted. These commands are: Seek, Recalibrate, and Search. Cleared when the moving function is completed at the time the DRY and ATA bits are set. Also set if MOL is reset.

Medium On-Line (MOL) - Bit 12

Set when the unit ready line from the drive is asserted indicating that the drive is up to speed, the heads are positioned over the recording tracks and no fault condition exists within the drive. Cleared when the spindle is powered down or the drive is off-line. Whenever the MOL bit changes state, the ATA bit is set.

Write-Lock (WRL) - Bit 11

Set when the write protected line from the drive is asserted as enabled by a switch located on the drive. A write command on a write-locked drive will cause the write-lock error (WLE, bit 11 of RMER1) to be set.

Last Sector Transfer (LST) - Bit 10

Set when the last addressable sector on the disk pack has been read or written. Cleared when a new write to RMDA is received.

At the time LST is set, the RMDA register is reset to 0 and the RMDC register increments by 1 to the first illegal cylinder address. If the RMWC register is not 0, a mid transfer seek is aborted which will cause the AOE status bit (RMER1, bit 9) to be set indicating that the desired cylinder register overflowed during a read or write.

Programmable (PGM) - Bit 9

This bit is set when dual-port operation is enabled.

Drive Present (DPR) - Bit 8

This bit is set if the controller has seized the drive and is reset when the other controller has seized the drive. This bit is a reflection of the DVA bit in RMCS1.

Drive Ready (DRY) - Bit 7

Set at the completion of every command and cleared at the initiation of a command. When set, this bit indicates the readiness of the drive to accept a command. If a mechanical movement command was initiated, the ATA bit will also be set when DRY is set. This bit is the complement of the drive's GO bit.

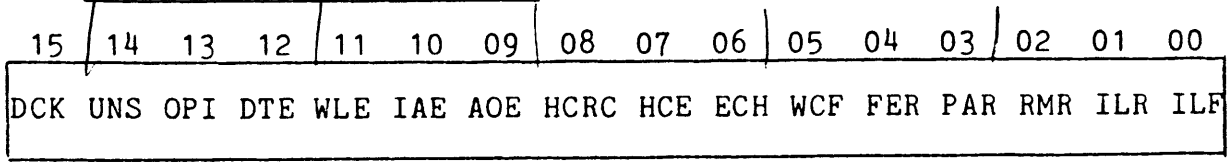
Volume Valid (VV) - Bit 6

Set by the Pack Acknowledge or Read-in Preset commands. Cleared whenever the drive cycles up from the OFF state. When reset, this bit indicates that the drive has been off-line and a disk pack may have been changed.

Offset Mode (OFM) - Bit 0

Set by the offset command to indicate that a read will be done with the heads in the offset position as determined by RMOF Bit 7. Cleared by a Read-in Preset, Return-to-Centerline, Recalibrate or write command, or a mid-transfer seek.

4.7 ERROR REGISTER 1 (RMER1) 776714



The RMER1 register is a read/write register that is used to store the error status of the drive whose unit number is in RMCS2. The RMER1 register can only be written as a word. Any attempt to write a byte will cause an entire word to be written. If the program attempts to write into this register while the drive is busy, an RMR (RMER1 register, bit 2) error is set, and the contents of the register are not otherwise modified. Writing 0's into this register should not be used as the normal way of clearing errors. The Drive Clear command should be used instead.

Data Check (DCK) - Bit 15

Set during a read operation when the ECC hardware detects an ECC error. The data transfer terminates with the current sector. If the Error Correction Inhibit (ECI) bit is off, the controller will go into the error correction process, and the RDY bit will not be set until the end of the process. If ECI bit is on, the error correction process is inhibited, the data transfer continues until the RMWC is zero and DCK is not set.

Unsafe (UNS) - Bit 14

This bit is a composite error bit of the unsafe and seek incomplete error conditions in the RMER2 register. With UNS set, correct results on any operation cannot be guaranteed. Some faults must be cleared by manual intervention at the drive.

Operation Incomplete (OPI) - Bit 13

Set when a read or write command involving header search cannot find the physical sector within three index pulses. Also set during a search operation where a sector count match is not made within three index pulses. When OPI is set, the GO bit is cleared and the RDY bit is set.

Drive Timing Error (DTE) - Bit 12

Set when either the header or data sync pattern is not found. When DTE is set, the GO bit will be cleared and the RDY bit set. Also set if a sector pulse occurs before the end of a sector's data field.

Write Lock Error (WLE) - Bit 11

Set when a write command is issued to a write-locked drive.

Invalid Address Error (IAE) - Bit 10

Set when the address in RMDC or RMDA is invalid and a Seek, Search or data transfer command is initiated.

Address Overflow Error (AOE) - Bit 9

Set when the RMDC register overflows during a read or write operation indicating that the address has exceeded the cylinder address limit. With AOE set, the controller will terminate the operation when the last sector of the last cylinder has been read or written.

Header CRC Error (HCRC) - Bit 8

Set by a CRC error in the header. If a CRC error is detected during a read or write command, the controller will not make any data transfer. In the event of a CRC error during a read header and data command, the entire sector will be transferred with the HCRC bit set.

Header Compare Error (HCE) - Bit 7

Set when the first two words of the header read at the sector whose count is equal to the desired sector field of RMDA do not match the contents of RMDC and RMDA. If the HCE bit is set during a read or write command, the controller will not perform any data transfer. In the event of a read header and data command, the entire sector will be transferred with the HCE bit set.

ECC Hard Error (ECH) - Bit 6

Set when the error correction procedure indicates that the error was a non-correctable ECC error. DCK (Bit 15) is also set.

Write Clock Fail (WCF) - Bit 5

This bit is normally a zero unless written into.

Format Error (FER) - Bit 4

Set if the FMT16 bit in RMOF does not match bit 12 in word 1 of a sector's header. Although the controller implements both 30 and 32 sector formats, all sectors contain 256 16-bit words in either format. If FER is set, then HCE may not be set.

Parity Error (PAR) - Bit 3

Set if the optional checksum feature is enabled and a bad checksum compare is found during a write operation.

Register Modification Refused (RMR) - Bit 2

Set when a write is attempted to any drive register (except RMAS)

with DRY=0. The drive will continue to execute the command in progress.

Illegal Register (ILR) - Bit 1

This bit is normally a zero unless written into.

Illegal Function (ILF) - Bit 0

Set when the function code in RMCS1 is illegal and the GO bit is set.

4.8 ATTENTION SUMMARY REGISTER (RMAS) 776716

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

The RMAS register allows the program to examine the attention status of all drives with only one register read operation. It also provides a means of resetting the attention logic in a selected group of drives. The eight low-order bits of this register correspond to the ATA bits in the RMDS of the drive having the same unit number as the bit position of this register.

A drive's ATA bit can be reset by loading a 1 into the bit position corresponding to the drive's unit number. Loading a 0 has no effect. For a program to use the RMAS without losing status information, the program must use MOV instructions for all writes to this register. An instruction that does a read-restore (such as BIS) may cause bits that became asserted between the read and the restore to be lost. This register can be read or written at any time.

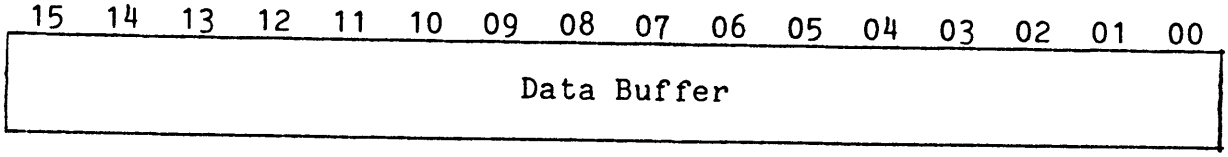
A persistant error, just like any error condition, will cause the ATA bit to be reasserted. Attempts by the controller to clear the error will not work in this case.

4.9 LOOK-AHEAD REGISTER (RMLA) 776720

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Sector Counter					0	0	0	0	0	0

The RMLA register contains the drive sector counter and is used to present the angular position of the disk relative to the read/write heads for the disk whose unit number appears in RMCS2. The purpose of this register is to provide the programmer with a means of optimizing disk accesses by minimizing rotational delays. The counter counts from 0 to 31.

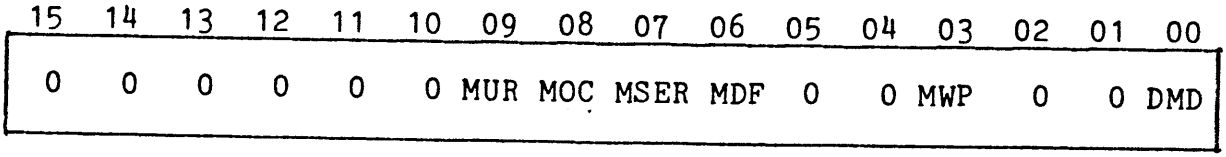
4.10 DATA BUFFER (RMDB) 776722



The RMDB register provides a maintenance tool to check the controller data paths. The IR (input ready) and OR (output ready) status indicators in RMCS2 registers are provided so that the programmer can determine when words can be read from or written into RMDB.

RMDB is used as an access to the Silo Buffer for an RM02. This controller has no Silo Buffer. All writes to this register are ignored. If a write-check error occurs, the data word as read from the disk is placed in RMDB and the OR bit in RMCS2 is set. Reading RMDB resets OR. Any further attempts to read RMDB will create a DLT error.

4.11 MAINTENANCE REGISTER 1 (RMMR1) 776724



RMMR1 is a read/write register that allows a program to simulate various signals from the disk for diagnostic testing of the controller. The DMD bit must be set before any other bit has an effect on the controller. This register may be written into as a word or a byte. Writing to RMMR1 can occur at any time regardless of the status of the drive. A drive or controller clear resets this register except for bit 3, which is set.

Maintenance Unit Ready (MUR) - Bit 9

Set by a diagnostic program to simulate the Unit Ready signal from the drive.

Maintenance On Cylinder (MOC) - Bit 8

Set by a diagnostic program to simulate the On Cylinder signal from the drive.

Maintenance Seek Error (MSER) - Bit 7

Set by a diagnostic program to simulate the Seek Error signal from the drive.

Maintenance Drive Fault (MDF) - Bit 6

Set by a diagnostic program to simulate the Fault signal from the drive.

Maintenance Write Protect (MWP) - Bit 3

Set by a diagnostic program to simulate the Write Protect signal from the drive.

Diagnostic Mode (DMD) - Bit 0

Set by the diagnostic program to reconfigure the drive into maintenance mode. None of the other bits in this register have any effect on the controller unless DMD is 1. Before a drive can be set to maintenance mode, it must first be ready and not busy. No positioner motion is initiated for a Seek, Home, Search or Implied Seek and all data transfer commands are ignored.

4.12 DRIVE TYPE REGISTER (RMDT) 776726

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DPM	0	0	0	Drive Type Code							

Moving-Head (MOH) - Bit 13

This bit is always a 1 indicating that the drive is a moving head device.

Dual-Port Mode (DPM) - Bit 11

This bit signifies that the drive is operating in dual-port mode as enabled by SW1-6.

Drive Type Code - Bits 7-0

This code specifies the type of drive as follows:
24 - RM03, 25 - RM02, 27 - RM05.

4.13 SERIAL NUMBER REGISTER (RMSN) 776730

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW1 -8	SW1 -7	SW1 -6	SW1 -5	SW1 -4	SW1 -3	SW1 -2	SW1 -1	Firmware Rev.				Port No.			

The purpose of the RMSN register was to distinguish a drive from similar drives attached to the controller by means of a four decade serial number. Here it consists of the controller port number for which the drive is attached, the firmware revision level, and the eight SW1 switch settings.

4.14 OFFSET REGISTER (RMOF) 776732

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	FMT 16	ECI	HCI	0	0	OFS 7	0	0	0	0	0	0	0

The RMOF register contains two inhibit bits and the drive offset direction bit. The offset direction bit determines if a read will be done with the heads advanced or retarded from normal centerline position. The actual offset determination is done by the status of RMDS bit 0. All bits of this register are cleared by Read-in Preset command.

Format Bit (FMT 16) - Bit 12

Set for 32 sector (16-bit) mode and reset for 30 (18-bit) sector mode. Since the controller only handles 16 bits/word format, this bit should always be a 1.

Error Correction Code Inhibit (ECI) - Bit 11

Set to inhibit error correction when an ECC error is detected.

Header Compare Inhibit (HCI) - Bit 10

Set to inhibit header compare and CRC check. With HCI set, the controller depends only on the sector count for sector identification. It is recommended that the HCI bit be reset during a write operation.

Offset Direction (OFS7) - Bit 7

Set under software control to select the direction of positioner offset. A one retards the heads and a zero advances the heads.

4.15 DESIRED CYLINDER REGISTER (RMDC) 776734

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Desired Cylinder Address										

The RMDC register contains the address of the cylinder to which the positioner is to move. The RMDC register will be cleared by the Read-in Preset command. Following an initial load, the value in the RMDC register will be incremented by 1 whenever the RMDA register is reset to 0 during a data transfer. When the RMDC register is incremented and the RMWC register is not equal to 0, a mid-transfer seek is initiated by the controller.

The Invalid Address Error (IAE) bit will be set when, upon asserting the GO bit, the RMDC register contains an address greater than the largest addressable cylinder.

4.16 HOLDING REGISTER (RMHR) 776736

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RMHR is a read-only register that always returns a zero when read except as follows: If the register is written into with one of the values listed below, it is possible to read out the configured size of the selected disk from the same register.

100027 - Maximum cylinder address
100030 - Maximum track address
100031 - Maximum sector address

4.17 MAINTENANCE REGISTER 2 (RMMR2) 776740

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
11777_8															

RMMR2 is a read-only register that always returns 11777_8 when read.

4.18 ERROR REGISTER 2 (RMER2) 776742

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	OPE	IVC	LSC	LBC	MDS	DCU	DVC	ACU	0	0	DPE	0	0	0

Error Register 2 is a read/write register that contains status information relating to the electromechanical performance of the drive whose unit number is in RMCS2. This register may be written as either a word or a byte. If any bit is set in this register, then the ERR bit in RMDS is also set. In some cases, the UNS bit in RMER1 will also be set. Writing zeros into this register should not be used as the normal way of clearing errors. A drive clear or a controller clear should be used instead. If the program attempts to write into this register while the drive is busy, the RMR bit in RMER1 will be set and the write will be ignored.

Bad Sector Error (BSE) - Bit 15

Set whenever the controller detects a zero in bit 14 or 15 of the first header word and the HCI bit in RMOF = 0. HCE in RMER1 is also set.

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if SKI is set.

Operator Plug Error (OPE) - Bit 13

Set whenever the drive's address plug is removed and then reinstalled. Can be cleared by cycling the drive down and up or by issuing a drive clear.

Invalid Command (IVC) - Bit 12

Set whenever any command is issued to a drive with MOL = 0. Set whenever any command except a Read-in Preset or a Pack Acknowledge is issued to a drive with VV = 0.

Loss of Sector Clock (LSC) - Bit 11

Set when the controller detects more than 63 sector pulses without an Index pulse, with Sector and Index on B cable.

Loss of Bit Clock (LBC) - Bit 10

Set if the controller does not detect at least 16 servo clocks within 3.0 microseconds.

Multiple Drive Select (MDS) - Bit 9

Set when more than one drive responds to a logical address on the A cable. This bit cannot be set by a program.

D.C. Power Unsafe (DCU) - Bit 8

Set if the -5 VDC power supply to the cable drivers and receivers is not proper. This bit cannot be set by a program.

Device Check (DVC) - Bit 7

Set if a Fault indication is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Fault is detected.

AC Power Unsafe (ACU) - Bit 6

Set if an ACLO indication is received from the Unibus.

Data Parity Error (DPE) - Bit 3

This bit is normally a zero unless written into.

4.19 ECC POSITION REGISTER (RMEC1) 776744

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	ECC Position												

The Error Correction Code (ECC) Position register is a read-only register that contains the position of the error pattern as determined by the ECC correction procedure. The error position is the number of bit positions from the beginning of the sector's data field to (and including) the right most bit position of the error pattern stored in RMEC2. If the detected error is not correctable using ECC, the ECH error bit in RMER1 will be set.

4.20 ECC PATTERN REGISTER (RMEC2) 776746

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Error Pattern										

The Error Correction Code (ECC) Pattern register is a read-only register that contains the 11-bit error correction pattern obtained from the ECC correction procedure. A 1 in the error pattern indicates a bit of the data in memory from the last read sector which is in error. The error pattern may straddle two 16-bit words in memory. The bit displacement to the right most bit of the pattern is determined by the bit count in RMEC1. The actual correction is done by an exclusive-OR of the error pattern and the data in memory.

4.21 BUS ADDRESS EXTENSION (RMBAE) 776750

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16

This register contains the upper 6 bits of the memory address which is combined with the lower 16 bits in RMBA to form the complete 22-bit address. The 6-bit field is incremented each time the RMBA overflows. Note that A16 and A17 are replicated in RMCS1. Writing in either affects both.

4.22 CONTROL/STATUS REGISTER 3 (RMCS3) 776752

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
APE	DPE HI	DPE LO	WCE HI	WCE LO	DBL	0	0	0	IE	0	0	IP 3	IP 2	IP 1	IP 0

Address Parity Error (APE) - Bit 15

Set if memory detected a parity error on address and/or control during memory transfer. Also sets UPE in RMCS2.

Data Parity Error (DPE) - Bits 14 and 13

Set if parity error is detected on data read from memory when performing a write or write check command. Also sets UPE in RMCS2.

Write Check Error (WCE) - Bits 12 and 11

Set if data fails to compare between memory and the disk on a write check command. Also sets WCE of RMCS2.

Double Word (DBL) - Bit 10

Set if the last memory transfer was a double-word operation.

Interrupt Enable (IE) - Bit 6

When IE = 1, an interrupt may occur due to RDY or SC being asserted. Cleared when the interrupt is recognized. Writing 0 into IE by the program cancels any pending interrupts. This bit is replicated in RMCS1. Writing into either affects both.

Inverted Parity Check (IPCK) - Bits 3 to 0

When set causes the corresponding byte to have its parity logic inverted during write and write check operations. The bits correspond to the 4-byte Cache Bus transfers as follows:

IPCK0 - Even word, even byte
IPCK1 - Even word, odd byte
IPCK2 - Odd word, even byte
IPCK3 - Odd word, odd byte

Should a Data Parity Error or a Write Check Error occuring during a 32-bit cache transfer (DBL = 1), then RMBA will be either + 2 or + 4 bytes ahead of the word that caused the error and RMWC will have incremented once or twice after the error. The user must examine RMCS3 to determine the actual address of the error. If DBL = 0, then RMBA = actual address + 2. If DBL = 1 and either WCE LO or DPE LO = 1, then RMBA = actual address + 4. If DBL = 1 and either WCE HI or DPE HI = 1, then RMBA = actual address + 2.

Operations are initiated on the drive selected by the unit select bits in RMCS2 by loading the function code and GO bit into RMCS1. The function code specifies a specific command. The commands can be divided into three categories: data transfer commands, positioning commands, and housekeeping commands. Commands and their corresponding function codes (always odd since the GO bit must be asserted to execute the command) are described below:

5.1 DATA TRANSFER COMMANDS

These commands involve data transfers to or from the disk and are designated by function codes 51 through 77.

All data transfer commands have seek and sector search functions implied. When the desired cylinder does not equal the current cylinder during the execution of the data transfer, a seek will be issued to the desired cylinder. The controller will then search the desired track for the desired sector and, when found, will start the data transfer. On all commands except the Write Header and Data command (which is the format operation) and Read Header and Data command, a match of the sector header must be made before the data transfer is started. If the header compare inhibit (HCI bit 10 in RMOF) is set, the header will not be compared or checked and, like the Write Header and Data command, the transfer will be started based on the pre-recorded sector pulses. With the HCI bit set, header errors will not be reported. With the HCI bit cleared, the transfer will be aborted if a header error is detected. The Read Header and Data command aborts only the transfers following the sector that caused the error.

The desired sector, track and cylinder addresses are updated after the transfer of a sector. Therefore, at the end of a transfer, the disk is set up to transfer the next sequential sector. This allows multiple sector transfers and spiral transfers across tracks and cylinders. When the desired cylinder address changes during a transfer, the implied seek is performed and is termed a mid-transfer seek.

The data transfer commands are described below:

5.1.1 Write Check Data (51)

This command reads data from the selected drive and compares it on a word by word basis with that obtained from memory. If the data fails to compare, the WCE status bit is set and the command is terminated immediately. For additional information on write check errors see Section 4.10 and the WCE bit in Section 4.5.

5.1.2 Write Check Header and Data (53)

This command reads the header field and data field from the selected drive and compares it on a word by word basis with data obtained from memory. If the header and data fail to compare, the WCE status bit is set and the command is terminated immediately.

5.1.3 Write Data (61)

This command writes the 256-word data field of the selected sector with words obtained from memory. A two word ECC is appended to each sector. If the word count in RMWC goes to zero during the sector, the rest of the sector is zero filled. After a sector transfer the word count in RMWC is checked, and if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit.

5.1.4 Write Header and Data (format operation) (63)

This command writes the 2-word header field and the 256-word data field of the selected sector with words obtained from memory. A one word CRC is appended to each header field, and a two word ECC is appended to each data field. After a sector transfer the word count in RMWC is checked, and if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit. If RMWC goes to zero during the sector, the rest of the sector is zero filled.

5.1.5 Read Data (71)

This command reads the 256-word data field from the selected sector and transfers the data to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RMWC is checked; if not zero, the data transfer operation is repeated with the next sector. If RMWC goes to zero during the sector, the rest of the sector is not transferred.

5.1.6 Read Header and Data (73)

This command transfers the 2-word sector header field and the 256-word data field from the selected sector to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RMWC is checked; if not zero the data transfer operation is repeated with the next sector.

5.2 POSITIONING COMMANDS

Positioning commands are mechanical movememt commands used to position the heads over the disk pack and take milliseconds to complete. Upon initiating the positioning commands, the controller will set the PIP bit and reset the DRY bit. Upon completion of the positioning operation, the controller resets the PIP and GO bits, sets the DRY bit and sets the ATA bit. The positioning commands are described below:

5.2.1 Seek Command (5)

This command causes the heads to be moved to the cylinder address specified by the contents of RMDC. When the controller sees the Seek command with the GO bit set, it sends the cylinder address to the corresponding drive. Any attempt to write into RMDC while the seek is in progress will cause the RMR bit to be set and RMDC will not be modified. Upon completion of the seek operation, the ATA and DRY bits in RMDS are set, and the GO bit is reset. If the drive is unable to complete a move within 500 milliseconds or if it has moved the carriage to a position outside the recording field, the drive asserts the seek error signal and the controller sets the SKI error bit in RMER2 and the ERR, ATA and DRY bits in RMDS. The controller will automatically issue a Fault Clear and a Return-to-Zero to the drive so that Drive Clear command can clear the error.

5.2.2 Recalibrate (7)

This command will cause the drive positioner to position the heads over cylinder 0. A Return-to-Zero is automatically performed with each head load sequence, and whenever a Fault or Seek Error is detected. This command clears the OFM bit in RMDS.

5.2.3 Offset Command (15)

This command causes the OFM bit in RMDS to be set. Subsequent reads will be done with the heads offset from track centerline in the direction specified by RMOF bit 7. This operation offers additional data recovery attempts over that provided by the ECC capability when an ECC error is detected. If an ECC hard error occurs, two offset positions should be used. At the completion of the offset command, the ATA bit is set indicating that a read command should be issued to the cylinder and track in order to recover data.

The OFM bit in RMDS will be cleared by any one of the following:

a. Seek to another cylinder by means of implied or mid-transfer seek.
b. Write command.
c. Return-to-centerline command.
d. Recalibrate command.
e. Read-in preset command.

5.2.4 Return-to-Centerline Command (17)

This command is used to clear the OFM bit and set the ATA bit in RMDS.

5.2.5. Search Command (31)

The search command causes the controller to first perform a seek to the desired cylinder and then compare the sector counter with the desired sector in the RMDA register. When they match, it sets the ATA bit causing an interrupt to the computer if IE in RMCS1 is set. An unsuccessful completion of a search command occurs when a sector count and desired sector address match is not made during the interval of three index pulses, in which case the OPI bit is set.

5.3 HOUSEKEEPING COMMANDS

Housekeeping commands are used to place drive logic into a known or initialized state and usually takes only a few microseconds to execute. The housekeeping commands are listed below.

5.3.1 NO OP (1)

This command does not perform any operation, except to clear the ATA bit.

5.3.2 Drive Clear (11)

This command causes the following registers and conditions associated with the drive selected by the unit select bits in RMCS2 to be cleared: ATA and ERR in RMDS, RMER1, RMER2, RMEC2, RMMR1 (except bit 3 which is set) and ATA bit in RMAS.

5.3.3 Release Command (13)

This command performs a drive clear function and releases the drive for use by the other port when in dual-port mode of operation.

5.3.4 Read-In Preset (21)

This command sets the VV (volume valid) bit, clears the RMDC and RMDA registers, clears the RMOF register, and clears the OFM bit in the RMDS register.

5.3.5 Pack Acknowledge (23)

This command sets the VV bit for the command controller. This command or a Read-in Preset command must be issued before any data transfer or positioning command can be given if the pack has gone off-line and then on-line (i.e., MOL change of state). It is primarily intended to avoid unknown pack changes.

5.4 OPTIONAL COMMANDS

The Boot and Format commands can be executed only after writing a 177777 into RMHR. (With SC70/B3, the toggle switch on the A board must be in the down position.)

5.4.1 Boot (75)

This command executes a Return-to-Zero; clears RMDC and RMDA; sets the FMT16 bit in RMOF; set the Volume Valid bit in RMDS; and reads sector 0 of track 0 and cylinder 0 into memory starting at location 0. The bank of memory that the data is to be read into is determined from the memory extension bits.

5.4.2 Format (77)

This command executes a Return-to-Zero; clears RMDC, and RMDA; and formats the entire pack in standard format. Each sector has bits 15, 14, and the FMT16 bit set in Header Word 1 and an all 0's data field. RMDC will be set to the last cylinder number plus one at completion, and the LST bit in RMDS will be set, and the FMT16 bit in RMOF will be set.

5.4.3 DMA Bandwidth Set (25) (Not available with SC71 and SC70)

This command requires option switch SW1-7 to be ON. The switch has a dual purpose: it activates the DMA bandwidth control during DMA transfers, and it makes this command code legal. This command allows the program to alter the amount of delay time between DMA bursts on a drive-by-drive basis. If ERR = 0 and DRY = 1 for the drive selected via RMCS2, then this op code takes the contents of RMWC, treats it as an unsigned 16-bit positive number, and saves it for use during subsequent data transfer operations. Each count equals a delay of 0.6 microseconds with a count of 0 = 1.5 microseconds. Any number in the range 0-65535(10) is legal. This results in a delay range of 1.5 microseconds to 39.33 microseconds in 0.6 microsecond increments. Each drive is individually programmable, and a default count of nine (6.9 microseconds) is preset at power-up time.

The /B1 controllers execute all DEC RM02/RM03 diagnostics. Several of the lower level diagnostics require patching to by-pass unsupported maintenance mode functions.

This section describes how to patch the DEC diagnostics for non-standard disk sizes with "t" tracks and "c" cylinders. All locations and contents are in octal.

6.1 ZRMA-C0 FORMATTER (August 1977)

6.1.1 Modifications to Correct Programming Errors

The following modifications correct some minor programming errors:

Loc.	From	To
12632	10011	1
23630	13746	12746
27154	1750	1503
27512	10164	110164
31602	10164	110164
32772,32774	5702,1426	4737,34676
32776,33000	4737,34676	5702,1424

6.1.2 Modifications For Number of Cylinders

Loc.	From	To	Loc.	From	To	Loc.	From	To
01320	1466	c-1	10006	1466	c-1	15202	1466	c-1
05652	1467	c	10736	1466	c-1	15404	1466	c-1
05666	1467	c	10754	1466	c-1	16432	1466	c-1
05704	1467	c	11270	1466	c-1	16504	1467	c
05730	1467	c	12532	1466	c-1	20072	1466	c-1
05754	1467	c	11512	151466	15000+c-1			

6.1.3 Modification For Number of Tracks

01324	4	t-1	10014	4	t-1	15212	4	t-1
05660	5	t	10500	4	t-1	15412	4	t-1
05674	5	t	11262	4	t-1	16412	4	t-1
05712	5	t	12562	5	t	16442	4	t-1
05736	5	t	12614	5	t	20100	4	t-1
05762	5	t	11522	2000	(t-1)*256.			

6.1.4 Formatter Operation

The Formatter program writes either all zeros, all ones or a worst case pattern in every sector, and at the same time it writes the headers. It does this by writing the complete track at one time. The program will print out five errors while attempting to read the

Bad Sector File on the last track of the disk if the pack has not been previously formatted. After the errors it will continue in a normal manner and will put a Bad Sector File on the pack. The program will ask for a pack I.D. if none already exists in the Bad Sector File.

The program can be loaded by XXDP. The normal starting location is 200_8, but should be started at 204_8 initially if it is desired to change the Unibus address or vector.

The program will type:

MODE (C OR F)

C should be typed for check and F for format, followed by a carriage return. Format mode does one pass, check mode does three passes with a rotating worst-case data pattern.

The program will then ask:

OPERATE IN 32 SECTOR (16 Bit) MODE (Y or N)

Y followed by carriage return should be typed.

The program will then ask for a drive:

DRIVE:

Enter the number (0-7) of the drive to be formatted followed by a carriage return.

The program will ask for address limits:

ENTER ADDRESS LIMITS:

Min and max sector, track and cylinder numbers may be entered in decimal followed by a carriage return. Just a carriage return will use the normal values. A period followed by a carriage return will terminate this phase.

The program will then ask for data pattern to which a carriage return should be typed to select worst-case. No pattern is asked for in Check mode.

The program will then type:

STARTING FORMAT (CHECK) ON DRIVE N

The program will list all errors and will indicate when it is done. The Bad Sector File is written just prior to the done message. During the format, typing a Control-O will display the current cylinder and track being formatted.

6.2 ZRMB-B0 PERFORMANCE EXERCISER (August 1977)

6.2.1 Modifications to Correct Programming Errors

The following modifications correct some minor programming errors.

Loc.	From	To
11134,11136	400,46116	100000,46144
32144	13746	12746
35130	1750	1503
35466	10164	110164
37556	10164	110164
41036,41040	5702,1426	4737,34676
41042,41044	4737,34676	5702,1424

6.2.2 Modifcations For Number of Cylinders

Loc.	From	To	Loc.	From	To	Loc.	From	To
01446	1465	c-2	25666	1465	c-2	26216	1466	c-1
06366	1465	c-2	13560	151466	150000+c-1			

6.2.3 Modifications For Number of Tracks

01444	4	t-1	16674	4	t-1	22616	4	t-1
13540	5	t	16702	5	t	26224	4	t-1
16656	5	t						

6.2.4 Performance Exerciser Operation

This program has the ability to do various operations on one to four drives. The Formatter must be run before this program can be run so as to provide proper patterns and a Bad Sector File.

A carriage return can be given to the requests for date and operator I.D. The program will then type:

ENTER PARAMETERS:

A carriage return should be given since it is normally not necessary to change the program parameters and the full instructions would be needed. After listing the availability of the eight drives the program is started with those drives that are on-line if started at location 200. Starting at 204 requires further keyboard commands as follows:

The program can be commanded from the keyboard by typing Control-C. It will then respond with ENTER COMMANDS. The command letter followed by the drive number (or the letter A for all drives) and a carriage return should be typed. The commands are:

T - Do normal random testing on drives.

D - Deassign a drive from testing.

W - Write data pattern starting at min address and proceeding to max address. Headers and Bad Spot File are not written.

R - Read data starting at min address and proceeding to max address.

WT - Same as write command, but then does test command.

S - Summary of current status.

Most of the commands will ask for min and max address limits. Sector, track and cylinder numbers may be entered in decimal, or a carriage return will give normal values. A period followed by a carriage return will terminate the requests.

The program will then ask for a Drive I.D. A 0-6 character I.D. followed by a carriage return should be entered. The I.D. is used during the status summary printouts that occur every 5 minutes.

Once the I.D. has been entered the program begins execution.

6.3 ZRMC-B0 FUNCTIONAL TEST - PART 1 (August 1977)

6.3.1 Modifications For Correct Operation

Loc.	From	To	
25024,25026	4737,43216	137,25622	DEC ECO
10730	40001	0	Drive clear in normal mode.
13062	1012	412	Bypass a maint. mode test.
26600	1007	407	Bypass a maint. mode test.
27014	1011	411	Bypass Massbus P.E. test.
35570	1406	406	Bypass 18-bit mode test.
45152	4	10	Incorrect offset
60000	7	1405	Incorrect value
66074	13746	12746	Incorrect addressing mode
10356,10360	5007,110102	11102,105002	
10362	1	240	

6.3.2 Modifications For Number of Cylinders

Loc.	From	To	Loc.	From	To	Loc.	From	To
27502	1466	c-1	33346	1467	c	51226	1467	c
31374	1466	c-1	33664	1467	c	51342	1467	c
32024	1466	c-1	40034	1467	c	52242	1466	c-1
32242	1466	c-1	40332	1467	c	57734	1466	c-1

6.3.3 Modifications For Number of Tracks

Loc.	From	To	Loc.	From	To	Loc.	From	To
32732	2400	t*256	37700	4000	40000	51152	240	t*32
33224	3400	37400	37726	2400	t*256	51200	5	t
33252	2400	t*256	51140	240	t*32	51212	5	t
37440	2400	t*256	51114	177770	177700			
52310	4	t-1	60002	4	t-1			

6.4 ZRMD-B0 FUNCTIONAL TEST - PART 2 (August 1977)

6.4.1 Modifications for Correct Operation

Loc.	From	To	
40452	4	10	Incorrect offset
63360	13746	12746	Incorrect addressing mode

6.4.2 Modifications For Number of Cylinders

Loc.	From	To	Loc.	From	To	Loc.	From	To
20376	1466	c-1	25130	1467	c	44526	1467	c
23016	1466	c-1	34770	1466	c-1	44642	1467	c
23100	1466	c-1	36430	1466	c-1	45542	1466	c-1
23376	1466	c-1	36520	1466	c-1	53766	1466	c-1

6.4.3 Modifications For Number of Tracks

17516	2037	256*(t-1)+37	36500	4	t-1
22274	2000	256*(t-1)	36770	4	t-1
23106	2037	256*(t-1)	44414	177770	177700
23404	2037	256*(t-1)+37	44440	240	t*256
24410	2400	256*t	44452	240	t*256
25066	3400	37400	44500	5	t
34762	2000	256*(t-1)	44512	5	t
35774	2012	256*(t-1)+12	45610	4	t-1
36410	4	t-1	54004	4	t-1

6.5 ZRME-B0 FUNCTIONAL TEST - PART 3 (August 1977)

6.5.1 Modifications For Correct Operation

Loc.	From	To	
31032	42702	52702	Bypass a DEC patch.
30070,30072	404,240	402,0	
30076,30100	137,30470	5237,1336	
30416,30420	404,240	402,0	
30424,30426	137,30470	5237,1336	
44472	4	10	Incorrect offset
67364	13746	12746	Incorrect addressing mode

6.5.2 Modifications For Number of Cylinders

Loc.	From	To	Loc.	From	To	Loc.	From	To
20042	1466	c-1	42450	1466	c-1	50662	1467	c
20446	1466	c-1	42540	1466	c-1	51562	1466	c-1
41010	1466	c-1	50546	1467	c	60006	1466	c-1

6.5.3 Modifications For Number of Tracks

Loc.	From	To	Loc.	From	To
22100	2037	256*(t-1)+37	50434	177770	177700
32712	2037	256*(t-1)+37	50460	240	t*32
36724	2037	256*(t-1)+37	50472	240	t*32
41002	2000	256*(t-1)	50520	5	t
42014	2012	256*(t-1)+12	50532	5	t
42430	4	t-1	51630	4	t-1
42520	4	t-1	60024	4	t-1
43010	4	t-1			

6.6 ZRMF-B0 EXTENDED DRIVE TEST (August 1977)

6.6.1 Modifications for Correct Operation

Loc.	From	To
21464	13746	12746
27722-27726	5737,4322,1011	32737,100000,4350
27730-27734	32737,100000,4350	1405,12737,177777
27736-27742	1405,12737,177777	1446,137,30370
27744-27750	1446,137,30370	5737,4322,1401
37246	1750	1503
37604	10164	110164
41674	10164	110164
43064,43066	5702,1426	4737,44770
43070,43072	4737,44770	5702,1424

All of the above correct programming errors.

6.6.2 Modifications For Number of Cylinders

The following locations have 1466 and are patched to c-1:

1672, 1674, 1676, 1700, 1702, 1754, 2022, 2066, 2110, 2132, 2154, 2174, 2214, 2252, 2302, 2420, 2466, 2532, 2554, 2576, 2620, 2640, 2660, 2716, 2746, 17576.

The following locations have 1465 and are patched to c-2:

2342, 2374, 3006, 3040.

6.6.3 Modifications For Number of Tracks

Loc.	From	To	Loc.	From	To	Loc.	From	To
1704	4	t-1	2350	4	t-1	17224	4	t-1
1706	4	t-1	2624	4	t-1	17604	4	t-1
1710	4	t-1	3014	4	t-1	20314	5	t
2160	4	t-1	17024	5	t	33532	5	t

6.7 ZRMI-B0 DRIVE COMPATABILITY TEST (August 1977)

6.7.1 Modifications For Correct Operation

Loc.	From	To	
2100	13746	12746	Incorrect addressing mode

There are no other modifications to this test since the program never accesses any cylinder above 800 or any track above 4.

Appendix A

CONFIGURATION SWITCHES

SC71/B1 CONFIGURATION SWITCHES

Switch	Function
SW1-1	
SW1-2	
SW1-3	
SW1-4	
SW1-5	CMD Fixed Volume Select (Emulex Test Mode)
SW1-6	Dual-port drive mode enable
SW1-7	Century Trident Compatability enable
SW1-8	Checksum feature enable

SC70/B3 CONFIGURATION SWITCHES

Switch	Function
SW1-1	Drive Configuration
SW1-2	Drive Configuration
SW1-3	Drive Configuration
SW1-4	Drive Type Code 27 (rather than 25)
SW1-5	CMD Fixed Volume Select (Emulex Test Mode)
SW1-6	Single-port drive mode enable
SW1-7	Century Trident Compatability enable
SW1-8	Checksum feature enable

Configuration Select Table

SW1-3	SW1-2	SW1-1	Drive Size
O	O	O	823 cylinders, 5 tracks
O	O	C	823 cylinders, 10 tracks
O	C	O	823 cylinders, 19 tracks
O	C	C	842 cylinders, 40 tracks
C	O	O	1646 cylinders, 5 tracks
C	O	C	1348 cylinders, 19 tracks
C	C	O	64 cylinders, 4 tracks
C	C	C	(not used)

C = closed; O = open

APPENDIX B

DRIVE CONFIGURATION SETTINGS

B.1 EXPANATION

The SC21 is configurable as to drive size characteristics and drive type code by means of a PROM located at U129. Each PROM contains 32 configurations as tabulated in the following sections of this appendix. Selection is made by means of SW2-1 through SW2-5.

The table below shows the drive size and applicable manufacturer's model numbers for different drives which are configurable by the PROM.

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
80C	823	5	32	9762, 9730-80, 980, T82RM
80F	19	5	32	9730-80F - 1.92 mb. fixed head opt.
80E	9	5	32	9730-80F - 0.96 mb. fixed head opt.
160C	823	10	32	9730-160
160F	9	10	32	9730-160F - 1.92 mb. fixed head opt.
160E	4	10	32	9730-160F - 0.96 mb. fixed head opt.
160A	1646	5	32	9160
300C	823	19	32	9766, 9300, T302RM
500T	1348	19	32	T602
600C	842	40	32	9775
5F	64	4	32	9733-5

B.2 DRIVE CONFIGURATION PROM NO. 1143

Table entries: Key / Drive Type Code

C = sw. closed; O = sw. open

	SW2								
Octal	-5	-4	-3	-2	-1	Drive 0	Drive 1	Drive 2	Drive 3
00	O	O	O	O	O	80C/25	80C/25	80C/25	80C/25
01	O	O	O	O	C	160C/25	160C/25	160C/25	160C/25
02	O	O	O	C	O	160A/25	160A/25	160A/25	160A/25
03	O	O	O	C	C				
04	O	O	C	O	O	300C/25	300C/25	300C/25	300C/25
05	O	O	C	O	C	300C/27	300C/27	300C/27	300C/27
06	O	O	C	C	O				
07	O	O	C	C	C				
10	O	C	O	O	O				
11	O	C	O	O	C				
12	O	C	O	C	O				
13	O	C	O	C	C				
14	O	C	C	O	O				
15	O	C	C	O	C				
16	O	C	C	C	O				
17	O	C	C	C	C				
20	C	O	O	O	O				
21	C	O	O	O	C				
22	C	O	O	C	O				
23	C	O	O	C	C				
24	C	O	C	O	O				
25	C	O	C	O	C				
26	C	O	C	C	O				
27	C	O	C	C	C				
30	C	C	O	O	O				
31	C	C	O	O	C				
32	C	C	O	C	O				
33	C	C	O	C	C				
34	C	C	C	O	O				
35	C	C	C	O	C				
36	C	C	C	C	O				
37	C	C	C	C	C				

APPENDIX C

DRIVE MODIFICATIONS

This appendix provides modifications to commonly used drives for moving the Sector and Index signals from the A cable to the B cable.

C.1 CDC 9762

Remove (Ch. I)	Add (Ch. I)
B01-06B to JA82-18B	B01-06B to JA82-43B
B01-06A to JA82-18A	B01-06A to JA82-44A
B01-05B to JA82-25B	B01-05B to JA82-45B
B01-05A to JA82-25A	B01-05A to JA82-45A

Remove (Ch. II)	Add (Ch. II)
B03-06B to JA83-18B	B03-06B to JA83-43B
B03-06A to JA83-18A	B03-06A to JA83-44A
B03-05B to JA83-25B	B03-05B to JA83-45B
B03-05A to JA83-25A	B03-05A to JA83-45A

Rework transmitter card FTVV in location B01 (Ch. I) and B03 (Ch. II). Locate jumper at center bottom of board (as viewed with connector on the right). Remove jumper and reinsert one set of holes lower (i.e., from center hole to hole below original jumper). Remove the letter "F" from the card type designation FTVV and mark a "G" in its place so that the card type becomes GTVV.

NOTE - SLtarting with S/N 78,989 CDC will ship units with an enhancement feature which will allow easy switchover to the B cable as follows: Remove the jumper plug on (B07) of the logic chassis backpanel.

C.2 CDC 9730

Rework transmitter-receiver card CFAX in location A04 (Ch. I) and B04 (Ch. II). When veiwing card with connector on the right, locate four jumpers to the left of the I/O connectors and above the terminator ground lug. The bottom end of the jumpers must be removed from the holes to which they are soldered and moved to the holes immediately above. Next, find the small jumper to the right of the third IC from the connector edge of the board on the bottom row of ICs. This jumper must be removed and reinserted so that it connects the top and middle holes rather than the original connection of the bottom and middle. This connection ungates the sector and index driver.

Remove the letter "C" from the card type designation CFAX and mark a "D" in its place so that the card type becomes DFAX.

C.3 CDC 9766

Remove (Ch. I)		Remove (Ch. II)	
Sector +	J4-55	Sector +	J4-55
Sector -	J4-25	Secotr -	J4-25
Index +	J4-48	Index +	J4-48
Index -	J4-18	Index -	J4-18

Move Wire (Ch. I)	Orgin	From	To
Sector +	PA01-5B	J3-55	J2-26
Sector -	PA01-5A	J3-25	J2-13
Index +	PA01-6B	J3-48	J2-24
Index -	PA01-6A	J3-18	J2-12

Move Wire (Ch. II)	Orgin	From	To
Sector +	PA03-5B	J3-55	J2-26
Sector -	PA03-5A	J3-25	J2-13
Index +	PA03-6B	J3-48	J2-24
Index -	PA03-6A	J3-18	J2-12

Rework transmitter card FTVV in location A01 (Ch. I) and A03 (Ch. II). Locate the jumper at center bottom of board (as viewed with connector on the right). Remove jumper and reinsert one set of holes lower (i.e., from center hole to hole below original jumper). Remove the letter "F" from the card type designation FTVV and mark "G" in its place so that the card type becomes GTVV.

NOTE - Starting with S/N 15,382 CDC will ship u;nits with an enhancement feature which will allow easy switchover to the B cable as follows: Cut the cable tie securing PD90 to the I/O cable and plug PD90 into JD90 pins 13 and 14 (Ch. I) and pins 11 and 12 (Ch. II) as indicated on the top of the connector.

C.4 CDC 9448

Sector and Index are on both the A and B cables.

C.5 TRIDENT DRIVES

Sector and Index are on both the A and B cables.

C.6 FUJITSU DRIVES

Sector and Index are on both the A and B cables.

APPENDIX D

RSTS/E V7.0

D.1 MIXED DISK CONFIGURATIONS

Usually each type of disk requires a separate controller. Frequently, two similar types of disks may share the same controller and, in addition, two controllers having the same type disks may be used. This section describes the possibilities using DEC RH11 and SC21/B1 controllers.

D.1.1 RM and RP Disks On the Same Controller

Although RM and RP drives can be mixed on an RH11 controller, this is not possible with an SC21/B which is configured for either an RM emulation or an RP emulation, but not both. When disks are mixed on an RH11 the type of drive having the lowest unit number determines whether the drives on the controller are known as DR or DB disks.

D.1.2 RM and RP Disks On Separate Controllers

When an SC21/B1 with RM emulation is added to a system which already has RP disks, the SC21/B1 is placed at the non-standard CSR of 776300 (with a vector of 150) and the disks will be known as DR type. The only disadvantage of this arrangement is that the RM disks can not be booted with the hardward bootstrap. If it is desired to boot the RM disks, the arrangement must be reversed with the RH11 at the non-standard CSR address and the SC21 at the standard CSR address of 776700 (with a vector of 254).

D.1.3 RM Disks On Two Separate Controllers

When an SC21/B1 is added to a system which already has an RH11 with RM disks, the controller must be placed at the non-standard CSR address of 776300 (with a vector of 150) and the disks will be known as DB type. Likewise, if two SC21/B1 controllers are put on a system, one will be placed at the standard CSR address and the disk will be known as DR type, while the other SC21/B1 is placed at the non-standard CSR address and the disk type is DB.

D.1.4 Bootstrapping

With existing hardware bootstaps it is possible to boot only drives on the controller at the CSR address of 776700 regardless of drive type or by what name the disks are known. The disk boot is DB. The BOOT option in INIT.SYS can be used to boot with mixed configurations, except that if two disks of the same drive type and same unit number are on separate controllers, only the disk on the controller at the CSR address of 776700 can be booted. It is possible to get around this problem by using different unit numbers on the two controllers or disabling the interferring unit on the

controller at the 776700 CSR address.

D.1.5 Sysgen

When answering the question "RP04/RP05/RP06's?", indicate the number of drives on the controller called DB, regardless of the actual drive type. Similarly, the answer to the question "RM02/RM03's?" is the number of drives on the controller called DR. If there are both DB and DR controllers, the the SYSGEN will use both the DBDSK (or DBSEEK for overlapped seeks) and the DRDSK (or DRSEEK for overlapped seeks) drivers. The two drivers are identical and can handle both RM and RP disks.

D.2 PATCHES FOR NON-STANDARD SIZE RM DISK

The five sets of patches that must be applied to RSTS/E for non-standard disk sizes are covered in this section. The "Change To" column indicates the value that should be placed in the location. If no D.T. is indicated, apply the patch; if a D.T. is indicated, apply the patch out of each group for the D.T. to be used.

D.2.1 INIT.SYS Patches

BASE	OFFSET	IS	CHANGE TO	D.T.(1)	
SATBUF	014362	000002	M.S. Max Block	24	(2)
SATBUF	014364	000002	M.S. Max Block	25	
SATBUF	014442	001100	L.S. Max Block	24	
SATBUF	014444	001100	L.S. Max Block	25	
SATBUF	014522	000004	Cluster Size	24	(3)
SATBUF	014524	000004	Cluster Size	25	
DSIDAT	000064	151466	150000 + Max Cyl.	24	(4)
DSIDAT	000072	151466	150000 + Max Cyl.	25	
DSIDAT	000066	002037	Max Track:Max Sec.	24	(5)
DSIDAT	000074	002037	Max Track:Max Sec.	25	
ROOT	005556	002440	No. Tracks:No. Sec.	24	(6)
ROOT	005560	002440	No. Tracks:No. Sec.	25	
COPY	002252	000240	Sectors/Cylinder	24,25	(7)
DBDSK	000036	000240	Sectors/Cylinder		
DBDSK	000710	002400	No. Tracks * 256.		(8)

D.2.2 SYSGEN.SIL Monitor Driver Patches

Driver is in module RSTS.

DRDSK	000036	000240	Sectors/Cylinder
DRDSK	000710	002400	No. Tracks * 256.

D.2.3 Target Monitor (RSTS) Driver Patches

Driver is in module DSK if drivers are in separate phase; otherwise it is in module RSTS. Patches are applied to DRDSK if using non-overlap seek driver and to DRSEEK if using overlap seek driver. If the controller is known as DB type then the patches must be applied to bases DBDSK or DBSEEK rather than DRDSK or DRSEEK.

BASE	OFFSET	IS	CHANGE TO	D.T.
DRDSK	000036	000240	Sectors/Cylinder	
DRSEEK	000004	000240	Sectors/Cylinder	
DRDSK	000710	002400	No. Tracks * 256.	
DRSEEK	001042	002400	No. Tracks * 256.	

D.2.4 HOOK.SAV Patches

002564	000000	000240	Sectors/Cylinder	

D.2.5 SAVRES.SAV Patches

GGB	001172	000240	Sectors/Cylinder	

Notes:

(1) The Drive Type (D.T.) octal codes are as follows: 24 - RM03, 25 - RM02, 27 - RM05.

(2) The maximum block size for an RM disk on RSTS is: (Cylinders * Tracks * 32.) - 32. L.S. is the 16-bit least-significant part of the maximum block size and M.S. is the most significant part.

(3) The number of clusters must be less than 65,536.

(4) Maximum cylinder address OR-ed with 150000_8.

(5) Maximum track address in upper byte; 37 in lower byte.

(6) Number of tracks in upper byte; 40 in lower byte.

(7) Sector/Cylinder = No. Tracks * 32.

(8) No. of Tracks in upper byte; 0 in lower byte.

D.3 PATCH PROCEDURE

This section describes how to do the patches to RSTS/E assuming that the only peripherals available are the non-standard disk (which has a subset which is an RM02) and a tape unit.

1) Check the following conditions for the RSTS system to be used for initial patching procedures:

   - Sufficient storage to run utilities under the RT11 RTS
   - RT11 RTS installed (defaulted or added through (1,2) UTILTY.BAC
   - RT11 utilities (1,2) PIP.SAV and (1,2) HOOK.SAV resident system library account (1,2)

2) Use (1,2) REACT.BAC to create a temporary privileged account SY: (1,2).

3) Use (1,2) PIP.SAV to copy the following files from the DEC system distribution medium to the temporary account:

   (0,1) INIT.SYS
   (0,1) ERR.ERR
   (0,1) SYSGEN.SIL
   (0,1) RT11.RTS
   (1,2) ONLPAT.SAV

4) Apply patches to SY:(1,X) INIT.SYS per D.2.1 and to SY:(1,X) SYSGEN.SIL per D.2.2.

5) Mount a scratch volume (tape or disk) on a secondary drive. Use (1,2) PIP.SAV to initialize the tape.

6) Use (1,2) HOOK.SAV to generate a bootable patched system generation volume as follows:

   dev: (0,1) INIT.SYS,SY: (1,X) INIT.SYS (patched)

7) Use (1,2) PIP.SAV to copy the remaining files in strict sequential order (starting with the last file if the temporary medium is a disk volume with the NEW FILES FIRST option enabled):

   (0,1) ERR.ERR
   (0,1) SYSGEN.SIL (patched)
   (0,1) RT11.RTS

8) Use (1,2) SHUTUP.BAC to terminate the current timeshare session.

9) Set controller to non-standard disk configuration.

10) Boot the patched system generation medium and proceed with normal system generation except as noted below.

11) Use INIT option DSKINT to initialize the new non-standard disk with patched code.

12) Use INIT option COPY to save all system files mentioned above, and install the patched SYSGEN.SIL as the current monitor.

13) Apply the patches per D.2.3 to the driver of the customized target monitor before terminating the timesharing session under SYSGEN.SIL.

14) Proceed with the remaining system build activities.

15) Using ONLPAT.SAV patch (1,2) HOOK.SAV per D.2.4 and (1,2) SAVRES.SAV per D.2.5.

16) Finally, generate a new system recovery volume using the patched version of (1,2) SAVRES.

APPENDIX E

RSX-11M V3.2

E.1 EDIT TO SYSTB.MAC

Perform a normal SYSGEN, as if building a system to include one or or more RM03 drives. Before performing the final system build, edit the system table file SYSTB.MAC. In RSX-11M the Max Block Size = No. Cylinders * No. Tracks * 32.

For the number of DB drives specified in the SYSGEN dialog, edit lines 11 and 12 after the DBn:: label of the DR UCB so as to change from:

```
.WORD    2                    to:  .WORD    M.S. Max Block Size
.WORD    1140                      .WORD    L.S. Max Block Sise
```

E.2 EDIT TO DRDRV.MAC

Now edit the driver DRDRV.MAC for "t" tracks as follows:

At 2 lines after label 15$:, change from:

```
MOV     #5*32.,R1          to:  MOV     #"t"*32.,R1
```

At 4 lines after label 160$:, change from:

```
CMP     #5.*256.,R0        to:  CMP     #"t"*256.,R0
```

At 6 lines after label 160$:, change from:

```
SUB     #5.*256.,R0        to:  SUB     #"t"*256.,R0
```

E.3 BINARY PATCHES TO TASKS

The SYSGEN may continue to completion, but should be stopped before SAVing the new system, so the following patches may be applied. The LOAD MAPs for the files to be patched must be saved. The patches are applied by ZAP with the /LI option, except or BAD.TSK which uses /AB. SET /UIC= 1,54 .

FILE	LOCATION	IS	CHANGE TO
INI.TSK	INIBAB+2162	000002	M.S. Max Block Size
INI.TSK	INIBAD+2164	001140	L.S. Max Block Size
INI.TSK	INIBAD+2170	000005	No. Tracks
SAV.TSK	SAVSUB+132	000002	M.S. Max Block Size
SAV.TSK	SAVSUB+134	001140	L.S. Max Block Size
SAV.TSK	$DRDRV+130	000005	No. Tracks
BOO.TSK	$DRDRV+130	000005	No. Tracks
BAD.TSK	6:662	000002	M.S. Max Block Size
BAD.TSK	6:664	001140	L.S. Max Block Size

E.4 BINARY PATCHES TO STANDALONE PROGRAMS

Patch standalone programs using ZAP and /AB option. SET /UIC 1,51 .

DSCS8.SYS	021362	000240	Sectors/Cylinder
DSCS8.SYS	022600	112712	000401
DSCS8.SYS	034560	000002	M.S. Max Block Size
DSCS8.SYS	034562	001140	L.S. Max Block Size
DSCS8.SYS	034616	000002	M.S. Max Block Size
DSCS8.SYS	034620	001140	L.S. Max Block Size
DSCS8.SYS	055252	000753	000752 (Program Bug)
DSCS8.SYS	057236	000002	M.S. Max Block Size
DSCS8.SYS	057244	001140	L.S. Max Block Size
DSCS8.SYS	113370	000002	M.S. Max Block Size
DSCS8.SYS	113376	001140	L.S. Max Block Size
BADSYS.SYS	023750	000240	Sectors/Cylinder
BADSYS.SYS	036050	000002	M.S. Max Block Size
BADSYS.SYS	036052	001140	L.S. Max Block Size
BADSYS.SYS	053170	000002	M.S. Max Block Size
BADSYS.SYS	053176	001140	L.S. Max Block Size
BADSYS.SYS	045734	000002	M.S. Max Block Size
BADSYS.SYS	045736	001140	L.S. Max Block Size
BADSYS.SYS	045740	000005	No. Tracks
BADSYS.SYS	045750	000240	Sectors/Cylinder

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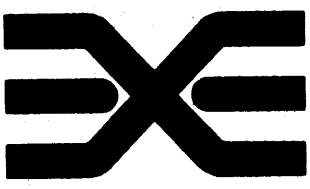

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