XEROX

Diablo Systems Incorporated
A Xerox Company

HyTerm Communications Terminal

Model 1641

Maintenance Manual

PREFACE

This manual contains only Theory of Operation (Section 2) and Maintenance (Section 3) information, and schematics and logic drawings (Section 4). Refer to the Product Description manual, no. 400082, for operation instructions, specifications, functional description, interface information and installation instructions.

This is a preliminary edition. Comments and suggestions on this manual and its use are welcome. Please address comments to the System Products Division of Diablo Systems, Inc., 545 Oakmead Parkway, Sunnyvale, California 94086.

Diablo Systems, Inc., reserves the right to make improvements to products without incurring any obligation to incorporate such improvements in units previously sold.

WARRANTY

The Diablo HyTerm Communications Terminal Model 1641 is warranted against defects in materials and workmanship for 90 days from the date of shipment. Any questions with respect to the warranty should be directed to your Diablo sales represenative. All requests for repairs should be directed to the Diablo repair depot in your area. This will assure you of the fastest possible service.

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Figure 1-1. HyTerm Communications Terminal Model 1641

Section 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The Model 1641 HyTerm Communications Terminal, Figure 1-1, transmits data to and receives data from a host computer or remote terminal over a communications link via an EIA RS-232-C interface. It communicates using either ASCII or the IBM 2741 terminal codes and protocol.

The HyTerm comprises a Diablo HyType II printer with microprocessor-driven electronics and an integral power supply, all contained in an attractive table-top unit. Standard features enable the 1641 to adapt to virtually any communications situation. A full complement of optional features, including forms tractor, pin-feed platen, carbon ribbon, interchangeable type fonts, etc., is available.

1.2 SCOPE

This manual provides information on theory of operation, maintenance, and module replacement. It also includes data covering the electronic components used and explanations of the logic symbology and drawing conventions used. It does not include operating instructions, installation procedures, or information on the functional operation of the HyTerm; these are all contained in the Product Description manual listed in the related documents.

1.3 RELATED DOCUMENTS

(1) HYTERM COMMUNICATIONS TERMINAL, MODEL 1641, PRODUCT DESCRIPTION. Diablo Systems, Inc. Publication No. 400032-01.

(2) SERIES 1300 HYTYPE II PRINTER PARTS CATALOG, August, 1976. Diablo Systems, Inc. Publication No. 82404.

(3) INTERFACE BETWEEN DATA TERMINAL EQUIPMENT AND DATA COMMUNICATION EQUIPMENT EMPLOYING SERIAL BINARY DATA INTERCHANGE. EIA Standard RS-232-C, August, 1969. Engineering Dept., Electronic Industries Assn., 201 Eye St. N.W., Washington, D.C. 20006.

(4) USA STANDARD CODE FOR INFORMATION INTERCHANGE, USAS X3.4-1968. American National Standards Institute, 1430 Broadway, New York, N.Y. 10018.

(5) DATA SET 103A INTERFACE SPECIFICATION, February, 1967, Engineering Director, Data Communications, American Telephone and Telegraph Co. Publication No. 41101.
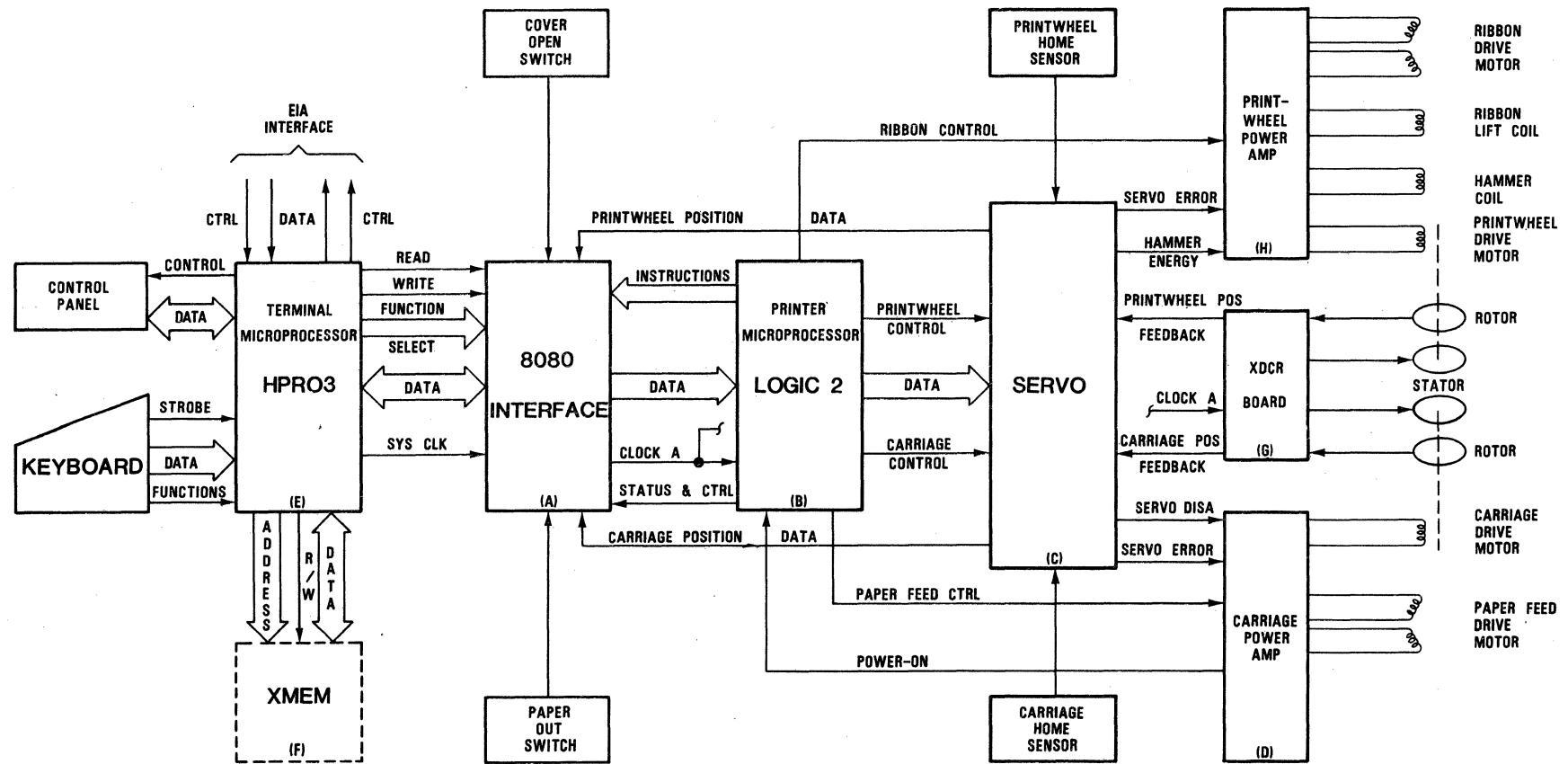
Figure 2-1. Model 1641 System Block Diagram

Section 2

THEORY OF OPERATION

2.1 INTRODUCTION (Figure 2-1)

The 1641 employs two separate, asynchronous, processing systems. One, called the "printer microprocessor," is an integral part of all HyType II printers. The other, called the "terminal microprocessor," provides the additional functions that transform a HyType II printer into a 1641 communications terminal.

The terminal microprocessor, located on the HPRO3 board, controls the overall terminal functions of sending and receiving data over the EIA interface, receiving data from the keyboard, and monitoring the control panel. It also communicates with the printer microprocessor, contained on the LOGIC-2 board. This second microprocessor system initiates movement of the printer carriage, printwheel, paper, and ribbon, and monitors feedback from the carriage and printwheel circuits to effect proper execution of these motion commands. It also maintains a record of the printwheel's absolute position at all times, it provides printer status information to the terminal microprocessor, and it performs other "housekeeping" functions.

The XMEM board is not part of all 1641 terminals. It is used during engineering development in early production models and when requirements exceed the memory available on the HPRO3 board.

The 8080 INTERFACE board is located logically between the two microprocessors. It provides temporary storage for data and status information, and synchronizes the transfer of data from the terminal microprocessor to the printer microprocessor, and the transfer of status information back. It also contains some control logic for the servo feedback system and provides the CLOCK A signal that drives the printer microprocessor.

The SERVO board receives printwheel and carriage motion commands from the printer microprocessor in digital form and converts these to analog signals representative of the distance and direction to be moved. These servo "error" signals are passed on to the printwheel and carriage power amplifiers, which drive their respective servo motors. Feedback signals, derived from the printwheel and carriage rotary transducers, are amplified by the XDCR board, and passed through the SERVO board to the 8080 INTERFACE board. Here they are available to the printer microprocessor, which uses them to regulate the error signals. The SERVO board also converts digital hammer-energy signals into their analog counterparts.

The PRINTWHEEL POWER AMPLIFIER provides drive for the printwheel servo motor, the ribbon step motor, and the hammer fire and ribbon-lift magnet coils.

The CARRIAGE POWER AMPLIFIER drives the carriage servo motor and the paper feed step motor. It also monitors the input voltages and develops the POWER ON signal to initiate the Restore operation.
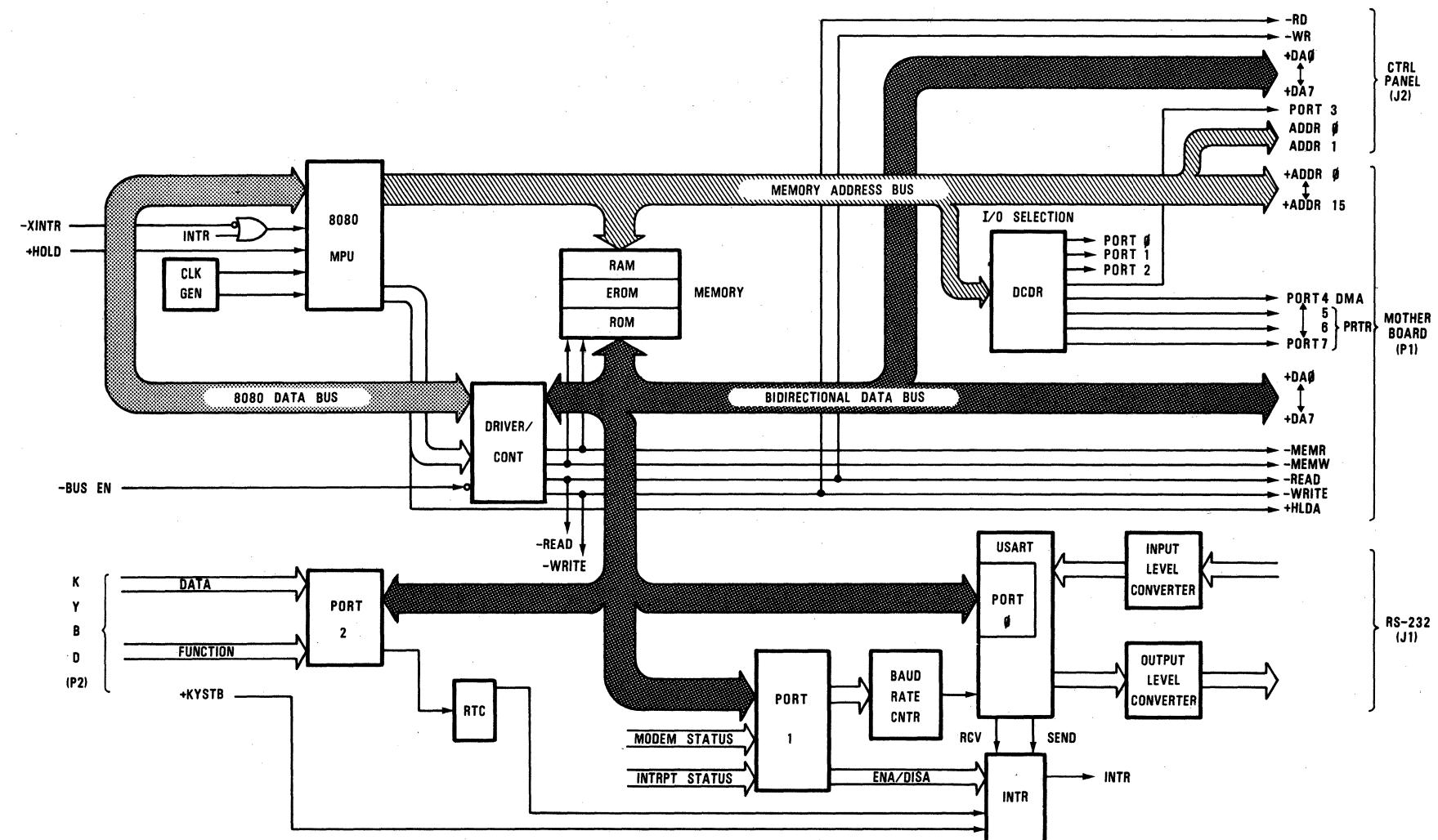
Figure 2-2. Block Diagram, HPRO3 Board

2.2 PROCESSOR (HPRO3) BOARD (Figure 2-2)

The HPRO3 board contains the terminal microprocessor system. This includes the 8080A Microprocessing Unit (MPU), Memory, several Input/Output (I/O) ports, the Universal Synchronous/Asynchronous Receiver/Transmitter (USART) and its associated RS-232 interface components, and all control electronics.

<div align="center">

NOTE

Throughout this manual, two terms will be used
extensively: *terminal microprocessor* refers mainly
to the entire HPRO3 circuit board, whereas *MPU* refers
to the 8080A integrated circuit.

</div>

2.2.1 General Operation

The terminal microprocessor is actually a miniature computer. It receives its instructions from Read Only Memory (ROM), either locally or located on the XMEM board. These instructions are arranged to form a "microprogram." As it executes this microprogram, the MPU receives data from the various input ports and stores it in memory, or reads data out of memory and sends it to the various output ports. Between input and output instructions, the MPU may perform other operations on the data, make logical decisions concerning the data, or "jump" to a different portion of its program.

2.2.1.1 Input/Output

Data can enter or leave the HPRO3 board via any of four channels. First, in the case of the keyboard, data enters the board over the "keyboard data bus" and is held in Port 2 until the MPU is ready for it. Then the MPU "reads" the data from Port 2, and the data is transferred to the MPU over the bidirectional data bus.

Second, data may enter (or leave) over the EIA interface, and be held temporarily in the USART (Port 0). The data is transferred between the MPU and the USART over the bidirectional data bus.

Third, data may enter or leave the board over the 8-bit bidirectional data bus through the J2 connector (normally used for the control panel). In this case, an "I/O port" or its equivalent must be located on another board cable-connected to the HPRO3 board via J2. This port is addressed as Port 3.

Fourth, data may enter or leave the board over the 8-bit bidirectional data bus through the mother board connector (P1). Again, an I/O port of some type must be located on another circuit board plugged into the printer mother board. The port must be addressed as Port 4 through 7.

In this fourth case, the data transfer can be either between the MPU and the external port, or it can be directly between the memory and the external port, bypassing the MPU. If direct memory access is used, the external port or device must provide the necessary signals to delay, or "hold," the MPU while the data transfer is taking place.

Note that the MPU can also address Port 1 for either input or output. This port, however, is contained fully on the HPRO3 board, and does not transfer data onto or off the board. It is used for local control of the baud rate and interrupt enable/disable, and to monitor interrupt status.

When the XMEM board is supplied, it is addressed in the same manner as HPRO internal memory via address lines on the mother board. Data is also transferred via the mother board.

2.2.1.2 Interrupts

The normal microprogram instruction sequence can be interrupted when necessary to enable the transfer of data to or from an I/O device, or for other purposes. Generally, when an interrupt occurs, the MPU completes the instruction it is presently performing, and then jumps to its interrupt servicing routine, which begins at memory location 0056_{10}. This routine first determines what type of interrupt is occurring, and then performs the steps necessary to service the interrupt. If two or more interrupts occur simultaneously, the interrupt service routine in the microprogram determines which will be serviced first.

There are five types of interrupts, all of which can be individually enabled or disabled by the microprogram. The first four types can be independently enabled or disabled on the HPRO3 board, whereas the last type (External) must be disabled on the circuit board on which it is initiated (some external circuit board). The five types of interrupts are as follows:

(1)	USART receive:	the USART has received a character from the data link and is waiting to transfer it to the MPU.
(2)	USART send:	the USART has shifted a character out to the data link and is ready to accept a new character for transmission.
(3)	Keyboard:	a data character has been received from the keyboard (or parallel data interface) accompanied by a strobe, and is waiting to be read by the MPU.
(4)	Real-Time Clock:	the Real-Time Clock has timed out, denoting that 10 ms has elapsed since it was activated.
(5)	External:	an interrupt can be generated by logic on a different circuit board and applied to the HPRO3 board via -XINTR.

2.2.1.3 Memory

Either random-access memory (RAM), read-only memory (ROM), or erasable read-only memory (EROM) ICs (or all three) may be used. Maximum capacity of the HPRO3 board is 4K bytes of ROM, 1K of EROM, and 512 bytes of RAM. Additional memory on the XMEM board can be utilized by placing the necessary address on the memory address bus; data is transferred over the bidirectional data bus.

2.2.1.4 Real-Time Clock

A 10-ms one-shot is used as a real-time clock, to allow the MPU to poll various I/O ports (e.g., the control panel) at regular intervals.

2.2.1.5　Special Voltage Supplies

The HPRO3 board also contains local voltage regulators to convert the $\pm15V$ from the main power supply to $\pm12V$ and $-5V$ needed by the EIA interface, some of the memory ICs, the MPU, and some external circuits and devices.

2.2.2　8080A Microprocessing Unit (MPU)

The 8080A is an 8-bit microprocessor contained in a single 40-pin integrated circuit (IC) package. It has an 8-bit wide bidirectional data bus used for both input and output. It has a 16-bit address bus, capable of addressing up to 65,536 memory locations. The MPU's instructions are located in memory, from where they are fetched and executed sequentially. There are over 100 separate instructions possible, although many are similar, the difference being only in the various MPU internal registers specified.

2.2.2.1　Architecture
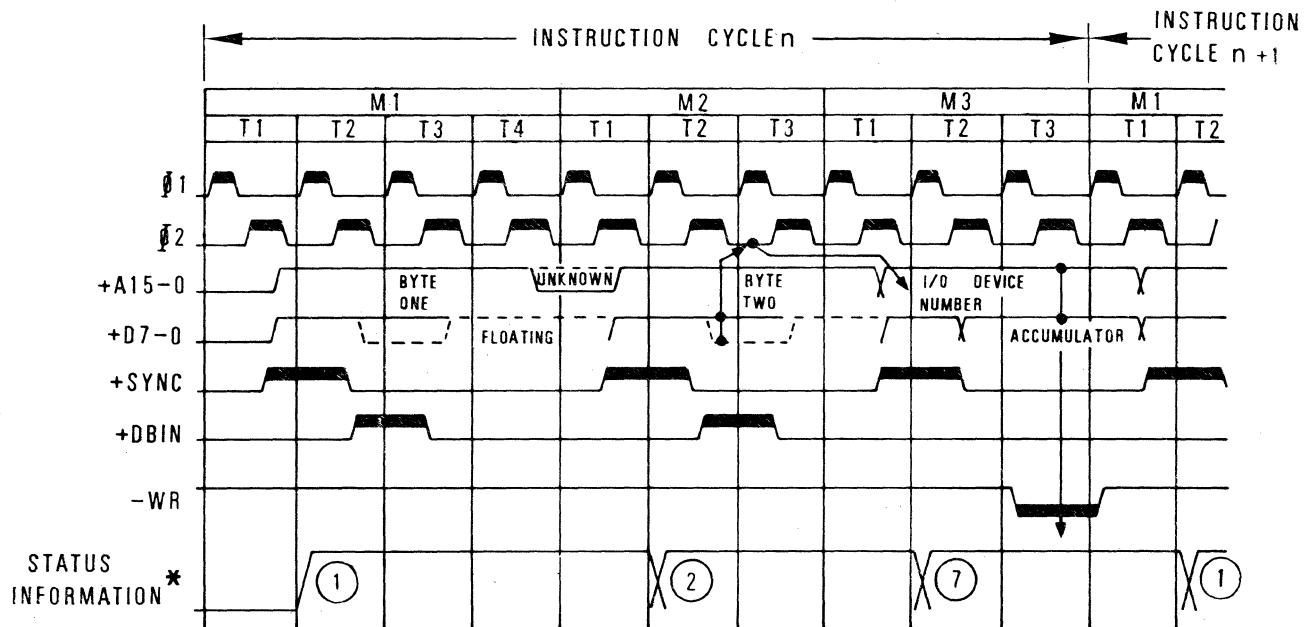
To understand the operation of the terminal microprocessor, it is only necessary to know that the MPU contains an instruction register, a program counter, a memory address register, a stack pointer, and other registers and logic elements. The instruction register contains the 8-bit instruction op code. The program counter contains the 16-bit memory address of the next instruction to be fetched. The memory address register is made up of two 8-bit registers, referred to as the H and L register pair. It is used to address memory for memory read and memory write instructions. Other internal MPU registers can also be used to address memory. The stack pointer is generally used to "remember" the address of the next sequential main program instruction while an interrupt subroutine is being executed. Still other elements internal to the MPU perform the arithmetic and logic operations and control the input and output over the data bus.

This is admittedly a very brief description of the MPU architecture, but this background should be sufficient to allow understanding of the material to follow. Further information on the MPU can be found in the integrated circuit information presented in the Schematics/Reference section of this manual.
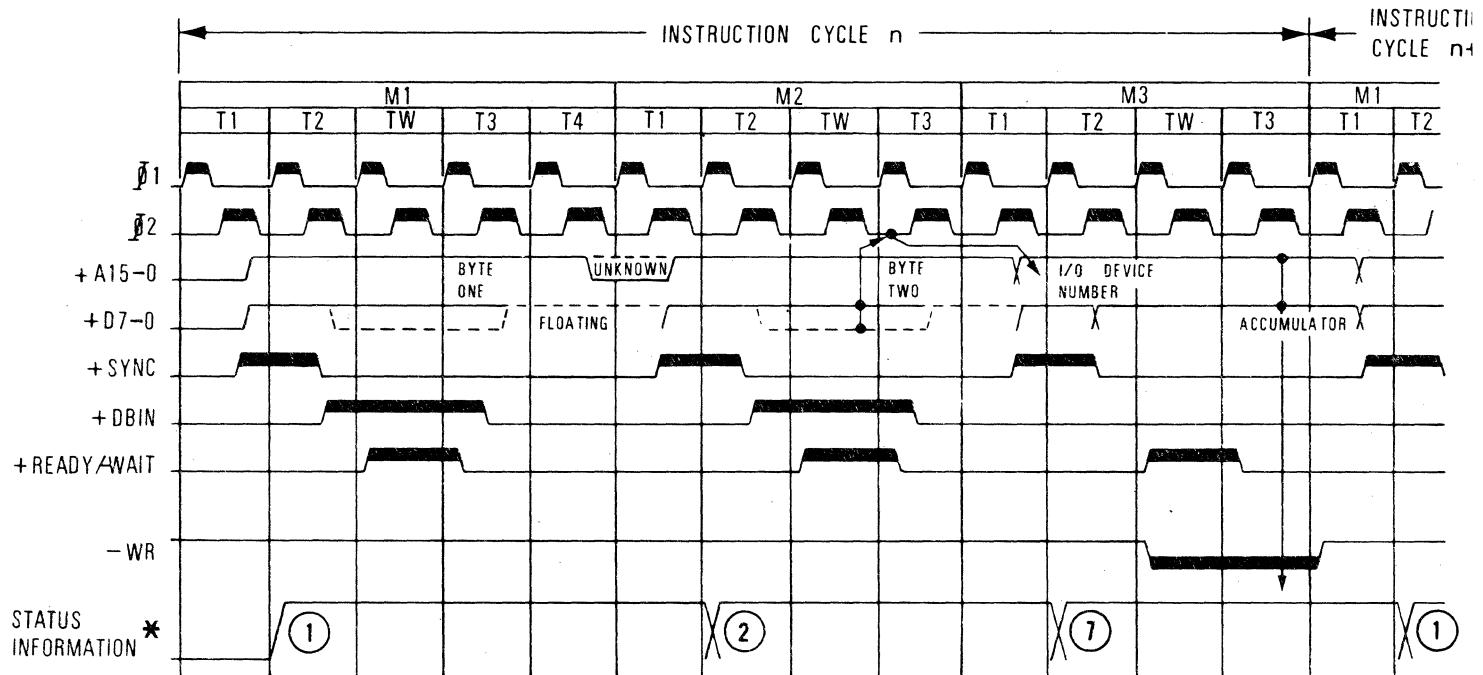
2.2.2.2　Timing

Timing is controlled by two 12V (nominal) non-overlapping clocks, $\Phi1$ and $\Phi2$. These clocks are provided at a frequency of 2 MHz by a Clock Generator IC.

A. Without WAIT State

B. With WAIT State

*Numbers in circles refer to types of machine cycles.

Figure 2-3. Typical Instruction Cycle (Output Instruction)

2.2.2.3 Basic Processor Operation

MPU operation is divided into time periods called "cycles" and "states."
There are two types of cycles: instruction cycles and machine cycles. The
material that follows is summarized in the timing chart in Figure 2-3.

2.2.2.3.1 <u>Instruction Cycle</u>. An instruction cycle includes both the fetching
of the instruction from memory and the execution of the instruction. Each
instruction may contain one, two, or three 8-bit bytes. Multiple byte instruc-
tions must be stored in successive memory locations. Figure 2-4 illustrates
the three instruction formats. The actual bit configuration of the op code is
not important to the understanding of the terminal processor operation.

One Byte Instructions

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | OP CODE

Two Byte Instructions

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | OP CODE

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DATA or ADDRESS

Three Byte Instructions

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | OP CODE

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DATA or

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ADDRESS

Figure 2-4.   MPU Instruction Format

2.2.2.3.2 <u>Machine Cycle</u>. A machine cycle is required each time an I/O array
or the memory is accessed. Each instruction cycle can contain from one to
five machine cycles. There are ten different types of machine cycles possible,
as follows:

    (1)   Instruction Fetch
    (2)   Memory Read
    (3)   Memory Write
    (4)   Stack Read
    (5)   Stack Write
    (6)   Input
    (7)   Output
    (8)   Interrupt Acknowledge
    (9)   Halt Acknowledge
   (10)   Interrupt Acknowledge While in Halt

2.2.2.3.3 <u>States</u>. A state is defined as the time interval (500 ns) from
leading edge to leading edge of the Φ1 clock. There are six possible states,
numbered T1 through T5 and TW (representing "wait"). All machine cycles
include T1, T2, and T3. When the jumper wire is installed between pins 24
(WAIT) and 23 (RDY) of the 8080A, TW follows T2. This is to slow down the MPU
so that slower memory ICs may be used. T4 and T5 are omitted during execution
of instructions not requiring them.

2.2.2.3.3.1   T1. During state T1 either a memory address or an I/O port number is placed onto the memory address bus. Also, the MPU places eight bits of status information on the data bus which identify the type of machine cycle being performed. Following the rising edge of Φ2 the SYNC signal is produced by the MPU, which identifies the beginning of a machine cycle. See Figure 2-3.

2.2.2.3.3.2   T2. During state 2 the MPU monitors its RDY input. If it is high, the MPU goes on to state 3; if it is low, the MPU goes on to the Wait state.

During machine cycles that bring data into the MPU (Instruction Fetch, Memory Read, Stack Read, Input, and Interrupt Acknowledge), the Data Bus In signal, DBIN, is developed at Φ2 during T2. DBIN remains high through TW and into T3. This signal develops -READ and -MEMR at the proper time to provide the input data needed by the MPU. (This is covered more fully in 2.2.4.)

2.2.2.3.3.3   TW. The wait state provides the MPU delay required for proper memory access. No internal processing occurs during this state. The MPU monitors its RDY input, and if it is low, it remains in the Wait state; if it is high, the MPU goes on to state 3. If the RDY input is connected to the WAIT output, the MPU goes on to T3 after one state time (500 ns) in TW.

During machine cycles in which the MPU outputs data (Memory Write, Stack Write, Output), it develops the WR (Write) signal during TW or T3 and holds it low until after the end of T3. This signal is used by other logic on the HPRO3 board or another board to strobe the output data to memory or the selected output port.

2.2.2.3.3.4   T3. During state T3 the data or instruction byte is actually transferred between the MPU and memory or an I/O port. The source and destination of the byte is determined by the type of machine cycle being performed. For example, during an instruction fetch cycle, the source of the data (instruction byte) is the memory location addressed during state 1; the destination is the MPU. During an Output machine cycle, the source is the MPU and the destination is the I/O port selected (addressed) in state 1.

2.2.2.3.3.5   T4 and T5. These two states are used only when required for manipulation of data within the MPU.

2.2.2.3.4 Hold. When the +HOLD signal goes high, it causes the MPU to stop operation at the end of the instruction currently being executed. This is used during direct memory access; when DMA is not used, the +HOLD line is held low by a jumper wire to GND.

2.2.3   Clock Generator (8224)

The clock generator is contained in a single integrated circuit that provides several functions. First, it provides the two non-overlapping 12V signals, Φ1 and Φ2, required by the MPU. The frequency of these signals (2 MHz) is controlled by an external quartz crystal. A TTL equivalent of the Φ2 signal, +TΦ2, is also developed for use in timing other functions.

Second, the 8224 converts the MPU's SYNC signal into the Status Strobe signal, STSTB. This signal is used to load the status information, put out by the MPU at the beginning of each machine cycle, into the Bus Driver/System Controller IC. This is covered more fully in 2.2.4.

Third, at power-on, the clock generator IC develops +CLR, which is used to reset and initialize the entire HPRO3 board.

The 8224 has other capabilities not utilized by the terminal microprocessor.

2.2.4   Bus Driver/System Controller (8228)

This module is another single IC that performs three basic functions: bi-directional bus control, system logic control, and initial interrupt request processing.

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE	⑨ HALT ACKNOWLEDGE	⑩ INTERRUPT ACKNOWLEDGE WHILE HALT
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

CONTROL SIGNALS:
- INTA
- (NONE)
- INTA
- I/O W
- I/O R
- MEM W
- MEM R
- MEM W
- MEM R
- MEM R

Figure 2-5.   MPU Status and Resultant Control Signals

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2.2.4.1   Bus Control

The 8228 provides a buffer between the MPU and the memory and I/O ports.
Controlling the two 8-bit data buses on the HPRO3 board involves not only
switching the data on and off in the proper direction at the right time, but
also in providing the required voltage and current levels.   Since the MPU is
an MOS device, it requires a voltage of at least +3.3 volts for a "logic 1" or
"true" indication on its data inputs.   The 8228 provides a minimum of +3.6
volts on the 8080 Data Bus, which is substantially higher than can be guaran-
teed by standard TTL devices.   For output data, the MPU can provide only 1.9
mA of current drive.   With many I/O ports and the memory connected to the bi-
directional data bus, this value could easily be exceeded, so the 8228 is used
to provide over 10 mA to satisfy this requirement.   The buses can be "turned
off" (forced into the high-impedance state) when direct memory access is used.
See 2.2.4.4.   The direction of data flow on the buses is controlled internally
by the same signals that furnish the system control function performed by this
IC.

2.2.4.2   System Logic Control

At the beginning of each machine cycle, the MPU issues "status" information on
the 8080 data bus that indicates the type of cycle about to be performed.   At
the same time, the clock generator module develops STSTB, which loads this
status information into a status latch inside the 8228.   This status latch
output is decoded [along with DBIN, WR, and HLDA (Hold Acknowledge) from the
MPU] into the system control signals MEMR (Memory Read), MEMW (Memory Write),
READ (I/O Read), and WRITE (I/O Write).   (These decoded signals also provide
the internal control of the bus driver.)   Note that these signals are not
levels, but that they are gated by DBIN or WR from the MPU at the proper time.
The status information provided by the MPU, and the system control signals
developed for each of the ten types of machine cycles are shown in Figure 2-5.

2.2.4.3   Interrupt Handling

The 8228 is capable of handling interrupts in either of two different ways. Only one of these methods is used in this terminal, in which the Interrupt Acknowledge pin (23) is connected to +12V through a resistor. Connected this way, when the MPU is interrupted (by an input from the keyboard or USART, for example), it performs an INTERRUPT ACKNOWLEDGE machine cycle, and the 8228 automatically forces an RST 7 (Restart 7) instruction into the MPU.   This instruction causes the MPU to fetch its next instruction from memory location 56_{10}, which begins the routine needed to service the interrupt.

2.2.4.4   Direct Memory Access

The BUS ENable input (pin 22) must be low for normal operation. When direct memory access is used, the DMA circuitry on another board drives this signal high, forcing all 8228 outputs into their high-impedance state. This allows the bidirectional data bus and the MEMR and MEMW signals to be controlled by the DMA logic. If the DMA feature is not used, -BUS EN is held low by a jumper wire to GND.

2.2.5   Memory

Maximum memory capacity of the HPRO3 board is 4K ROM, 512 bytes of RAM, and 1K of EROM. ROM memory consists of one or two 2K x 8-bit mask-programmed ROM ICs containing the terminal microprogram. RAM memory consists of two 256 x 4-bit ICs for each 256 bytes. The EROM portion can be either a 512 x 8-bit or 1K x 8-bit EROM IC. The EROM would normally contain keyboard position encoding data or similar data for terminals built in small quantities--too small to justify masked-ROM changes. When the XMEM board is supplied, the terminal microprogram can be stored there. See paragraph 2.3.
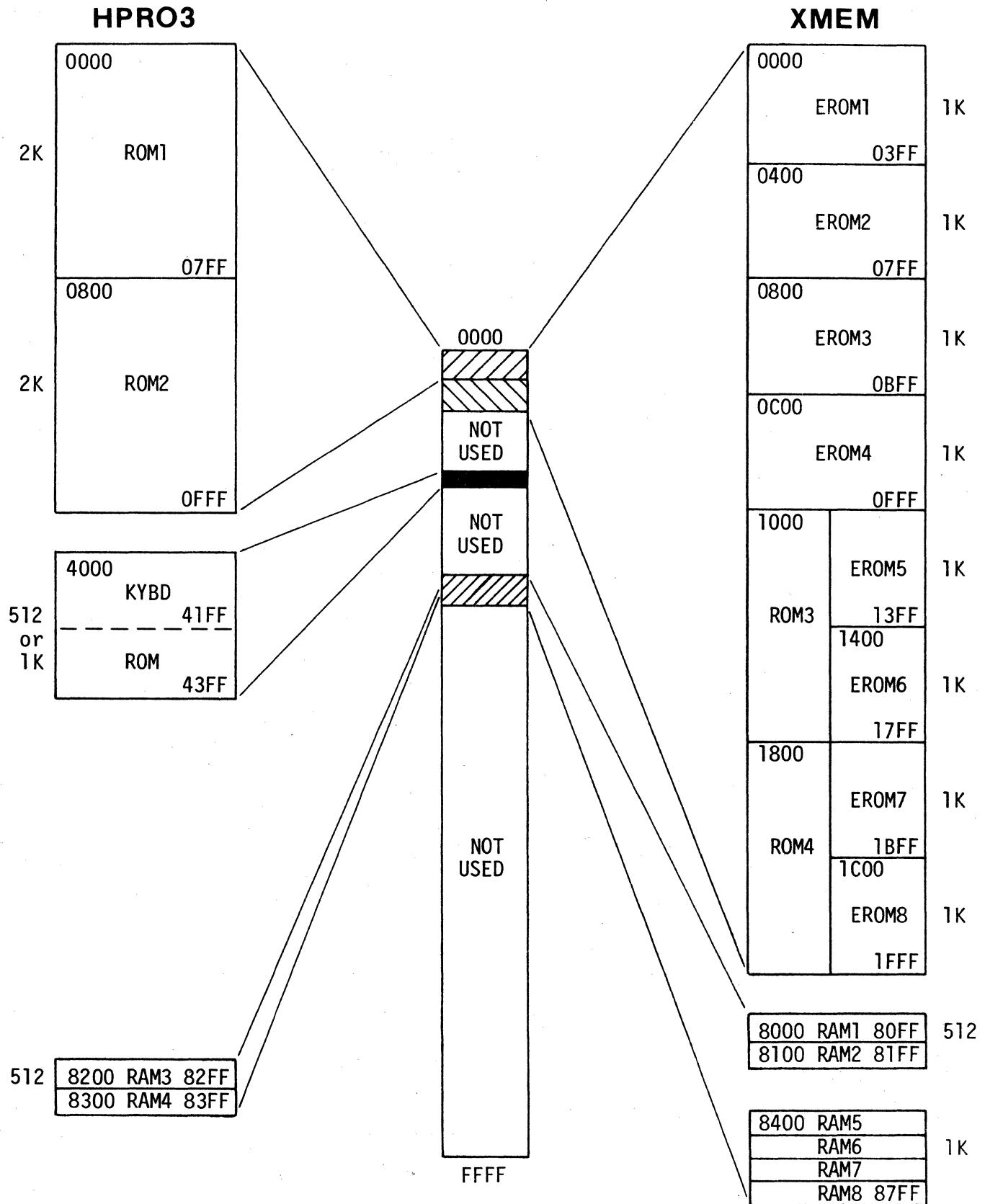
2.2.5.1   Addressing

The memory map in Figure 2-6 shows the relationship of the various memory elements to their addresses.

The memory ICs on the HPRO3 board are addressed by the low-order bits of the memory address bus. The higher-order bits A9, A10, A11, A14, and A15 are used to select, through a decoder, whether RAM, ROM, or EROM will be addressed. In the case of RAM, the state of the A8 line determines which pair of ICs will be addressed. For ROM, the A11 line selects which of the two possible ICs will be used. (Note that A11 goes to both ROM ICs; the internal programming of the ICs is such that one of the ICs will be activated when A11 is low and the other when A11 is high.)

Since the memory address bus is available on the HPRO3 board outputs, external memory can assume any memory address, so the terminal designer must assure that only one memory location exists for each address. For example, during program development, the microprogram can be contained in external memory beginning at location 0000. In this case, the HPRO3 board cannot have ROMs installed. After the microprogram is perfected, it can be "burned" into masked ROMs, which can be installed on the HPRO3 board, and the external memory board can be eliminated.

The memory address bus being available on the HPRO3 board's plug also enables the entire memory to be addressed from an external source, as is the case when the DMA function is utilized.

HPRO3

	0000	
2K	ROM1	
		07FF
	0800	
2K	ROM2	
		0FFF

	4000	
512 or 1K	KYBD	41FF
	ROM	43FF

512 | 8200 RAM3 82FF |
| 8300 RAM4 83FF |

XMEM

	0000		
	EROM1		1K
		03FF	
0400	EROM2		1K
		07FF	
0800	EROM3		1K
		0BFF	
0C00	EROM4		1K
		0FFF	
1000	ROM3	EROM5	1K
		13FF	
		1400	
		EROM6	1K
		17FF	
1800	ROM4	EROM7	1K
		1BFF	
		1C00	
		EROM8	1K
		1FFF	

| 8000 RAM1 80FF | 512 |
| 8100 RAM2 81FF | |

8400 RAM5	1K
RAM6	
RAM7	
RAM8 87FF	

NOTES: 1. First 4K can be either ROMs on HPRO3 or EROMs on XMEM.
        2. Second 4K can be either ROMs or EROMs on XMEM.

Figure 2-6. Memory Map

2.2.5.2 Reading

All memory ICs are three-state devices. This means that the outputs remain in the high-impedance, or "off" state, at all times when the IC is not selected. (This allows the memory address bus to be used for addressing I/O devices; the address lines can assume any configuration, but there will be no input to or output from memory without the proper system control signals.) The MEMR signal is connected to the "output disable" input of the RAMs (pin 9). This maintains the RAM outputs in their high-impedance state at all times other than during a memory read. MEMR is also one of the inputs to the memory type decoder. This allows ROM and EROM to be selected only during a read operation.

2.2.5.3 Writing

When memory write is performed, the RAM output remains disabled (MEMR is high), and MEMW being low allows information on the bidirectional data bus to be written into the addressed RAM location. Note that each pair of RAMs operates in parallel, one IC servicing the low-order four bits of the bi-directional bus, and the other taking care of the high-order four bits.
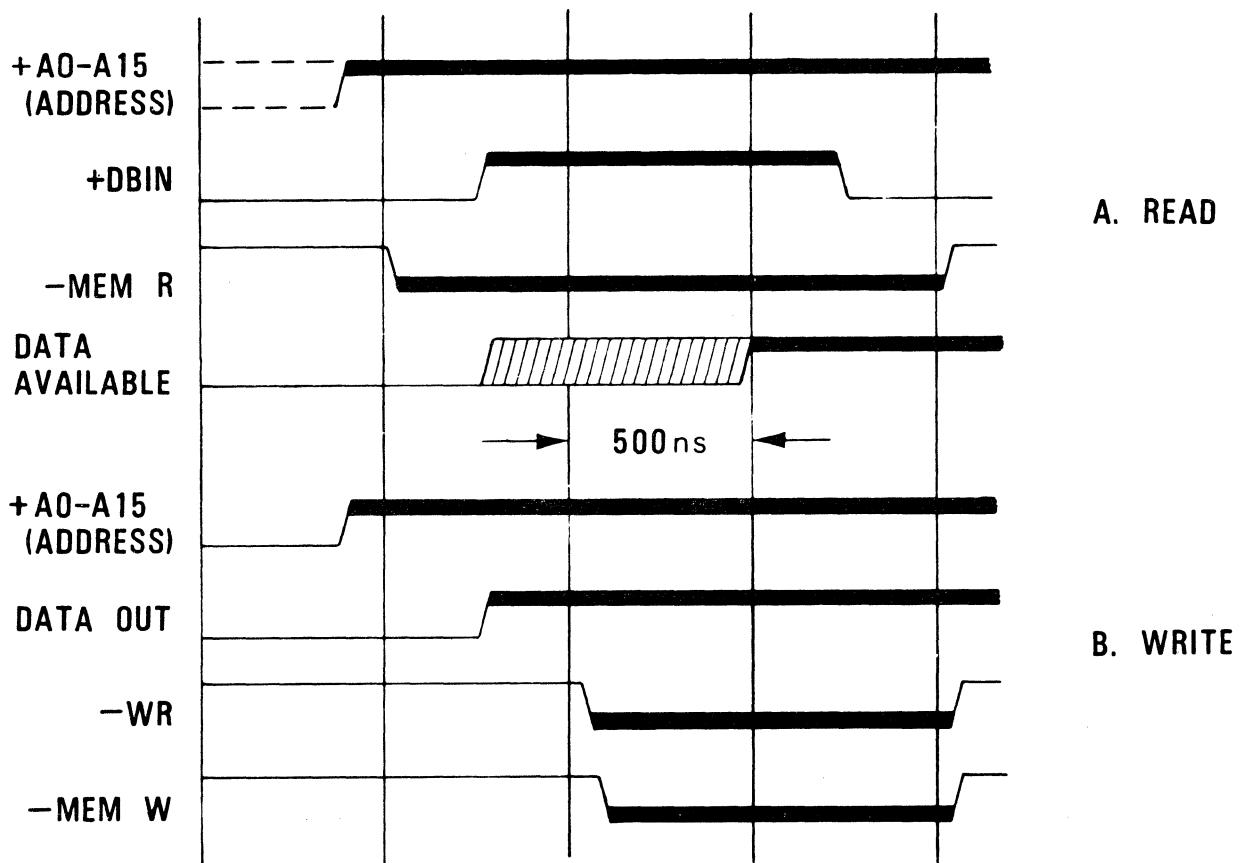
Figure 2-7. Memory Timing

2.2.5.4   Timing

Typical idealized timing waveforms are shown in Figure 2-7. Specific timing requirements for each of the memory IC types can be found in the IC information in the schematic/reference section. In all cases, the timing shown in Figure 2-7 is within the timing constraints of the individual ICs.

2.2.5.5   Direct Memory Access

When the DMA function is utilized, it conforms to the following general sequence:

    (1)   DMA circuitry on another board raises the +HOLD line to the MPU.

    (2)   The MPU finishes the instruction it is presently performing, and then raises its HLDA (Hold Acknowledge) line. It then suspends operations, and holds all data and address lines in their high-impedance state.

    (3)   The DMA circuitry receives the hold acknowledgement and drives -BUSEN low. This forces the 8228 to place all of its outputs, both data and control signals, into their high-impedance state.

    (4)   The external DMA circuitry then places the desired address on the memory address bus, and drives either -MEMR or -MEMW low. The data is then transferred over the bidirectional data bus.

    (5)   When the DMA circuitry is finished, it raises -BUSEN and lowers +HOLD, and the MPU resumes processing at its next sequential instruction.

2.2.6   Input/Output

The terminal microprocessor can address up to eight I/O ports. These ports, or "devices," such as keyboard, control panel, etc., are addressed over the Memory Address Bus, and data is transferred to and from the MPU over the bidrectional data bus. An I/O channel or device is first addressed by the MPU, which then develops the -READ or -WRITE signal to transfer the data. On output, for example, the MPU first addresses a particular output device, then places the output data on the bidirectional data bus, and finally develops -WRITE. Although the data is available to all "devices" on the bus, only the one that had been addressed can accept the data. Input is similar: only the addressed device places data onto the bus. All other devices are "observers."

The five low-order bits of the memory address bus are used for I/O device selection. Bits 2, 3, and 4 are applied to a decoder, the outputs of which (-PORT 0 through -PORT 7) are used to select one of the eight possible ports. Each port can comprise up to four 8-bit bytes, and bits 0 and 1 are used to select one of the four bytes.

Three of the eight possible I/O ports are located on the HPRO3 board. The rest of the ports may or may not be used in a particular terminal or printer. The possible ports and their typical functions are as shown in Table 2-1.

2.2.6.1   USART (Port 0)

The type 8251 USART (Universal Synchronous/Asynchronous Receiver/Transmitter) IC accepts an 8-bit byte of data from the MPU in parallel format and converts it to a serial stream of data for transmission over the communications link.

Similarly, it receives data characters from the link in serial format and converts them into parallel data bytes for the MPU. During transmission, the USART adds start, stop, and parity bits. During reception, it strips these bits and also checks parity, if desired. It also checks for data framing errors and overrun errors, and can monitor modem status. It has other capabilities that are not generally used (synchronous transmit/receive, character lengths down to 5 bits, etc.).

Table 2-1. I/O Ports

Port No.	Function
0	USART
1	Baud Rate, Interrupt Enable/Disable & Status
2	Keyboard
3	Control Panel
4	DMA

2.2.6.1.1 Addressing. The CS (Chip Select) input is driven low whenever the MPU addresses Port 0. No information can be transferred between the USART and the MPU until the USART is selected.

The USART also has a C/D input, which is connected to the +ADDR $\emptyset$ line of the Memory Address Bus. When this line is high, control information is transferred; when it is low, data is transferred. The USART does not utilize the +ADDR 1 line.

2.2.6.1.2   Timing. Refer to the baud rate counter discussion in 2.2.6.2.1.2.

2.2.6.1.3   Information Transfer. Two inputs, RD and WR, determine the direction of information transfer. When RD is low, the USART places data or status information (determined by the C/D input) on the bidirectional data bus for input to the MPU. When WR is low, data or control information from the MPU is taken off the data bus and loaded into the USART. The RD and WR inputs are controlled by -READ and -WRITE, respectively, from the 8228 bus driver/system controller.

Note that all information transfer between the MPU and the USART is over the bidirectional data bus, through a bidirectional, 3-state buffer within the USART. Information transfer between the USART and the data link is over individual lines for Send Data, Receive Data, and each of the modem status and control lines, through a voltage level converter, to (or from) the modem. (Refer to the integrated circuit data in the Schematics/Reference section for information on the level converter ICs.)

2.2.6.1.3.1 Read Data. When the USART receives a character from the data link, it raises its RXRDY (Receiver Ready) line, which goes to the interrupt logic. If USART interrupts are enabled, +INTR is developed and sent to the MPU. In servicing this interrupt, the MPU performs a sequence of instructions, one of which is an input from Port ∅. With CS low, RD low, and C/D low, the USART puts an 8-bit byte of data onto the bidirectional data bus, from where it is accepted by the MPU. The USART, having presented the data byte to the bus, resets its RXRDY line, until the next character is received and the entire sequence repeats.

As the data is received from the data link, the USART strips off the start and stop bits, checks the parity bit (if parity checking is enabled--see 2.2.6.1.3.4), and checks for framing errors (lack of a stop bit at the proper time). If an error is detected, a bit is set in the internal Status Register. the USART also checks to see that the previous character has been accepted by the MPU--if RXRDY is still high (has not been reset by the MPU having read the previous character), the overrun status bit is set.

2.2.6.1.3.2 Write Data. When the MPU wishes to send data to the USART, it addresses Port 0, places the data character on the bidirectional data bus, and develops -WRITE. This combination (CS, WR, and C/D all low) loads the character into the USART, which then adds the start, stop, and parity bits, and immediately begins to shift the character out, one bit at a time through the level converter IC to the data link.

There are two status bits pertaining to data transmission: TXE (Transmitter Empty) and TXRDY (Transmitter Ready). Both of these become reset when a character is loaded into the USART from the MPU. If a relatively long time has passed since the previous character was loaded, TXRDY sets again almost immediately. This allows a second character to be loaded, even though the first has not been fully shifted out. TXRDY again resets as the second character is loaded, but this time it remains reset until the first character is completely shifted out. Then it sets again, allowing another character to be loaded. When all data characters have been fully transmitted, TXE again sets.

2.2.6.1.3.3 Read Status. When the MPU wishes to know the status of the USART, it performs an input from Port 0 with +ADDR ∅ high. This occurs after any interrupt, since the MPU needs to know if it is the USART that is interrupting, and before every data output to the USART, because the MPU must check to see that the USART is able to accept the data character.

When Port 0 is addressed, the -PORT ∅ signal enables the USART by driving its CS input low, and +ADDR ∅ drives the USART's C/D input high, which directs the USART to transfer control/status information. -READ again directs the USART to output information onto the bidirectional data bus, but because the C/D input is high, the USART outputs status information instead of data.

2.2.6.1.3.4 Write Control. A control write is used to program the USART for parity checking, byte length, number of stop bits, etc. When the MPU outputs control information for the USART, it addresses Port 0 while holding

+ADDR $\emptyset$ high. However, complete control of the USART requires more than 8
bits of information. The USART is designed to accept two different control
bytes, a "Command" byte and a "Mode" byte. It accepts the Mode byte only as
the first control instruction following a reset. All subsequent "control
writes" are accepted as Command bytes. Each of the individual bits in the
Command and Mode bytes is defined in the IC data for the 8251 in the Schem-
atics/Reference section of this manual.

2.2.6.2   I/O Port IC (8255)

The other two I/O ports on the HPRO3 board, Ports 1 and 2, utilize an 8255
Programmable Interface IC. This type of IC may also be used for ports located
on other circuit boards. This is a 40-pin IC having eight pins connec-
ted to the bidirectional data bus and three more sets of eight pins each that
can interface to various "peripheral" devices. The balance of the pins are
used for power supply connections and control signals.

The 8255 contains three 8-bit registers called A, B, and C, each of which can
be used for either input or output. The C register can even be split into two
4-bit registers, each individually programmable for input or output, or for
control and status signals.

There are three possible modes of operation, selected by a control word issued
by the MPU. This control word is a part of the firmware microprogram stored
in ROM, so it can be different for each 8255, and it can even change at
different points in the execution of the program. (This control word can also
be used to alter individual bits in Register C, while leaving the other seven
bits unchanged.) The three possible modes are as follows:

    Mode 0:   Simple input or output for each register
              Two 8-bit and two 4-bit registers
              Outputs are latched
              Inputs are not latched

    Mode 1:   Strobed input or output for Registers A and B
              Register C used as control/status for the other two registers
              Inputs and outputs all latched

    Mode 2:   Strobed bidirectional bus (not used in HPRO3)

Each 8255 IC has the following connections to the terminal microprocessor:

    D0-D7:   The bidirectional data bus, over which all data transfer
              occurs between the MPU and the 8255.
    CS: Chip Select Input. One of the decoded "port" signals is used to
              select only one 8255 at a time. Only -PORT 1 and -PORT 2
              select 8255s on the HPRO3 board. The other port signals may
              select 8255s on other circuit boards.
    AO&A1:   ADDRESS $\emptyset$ and ADDRESS 1 Inputs. The two low-order lines of the
              Memory Address Bus (ADDR $\emptyset$ and ADDR 1) are used to select which
              of the three registers is to be used, or to specify that a
              control word is being sent out by the MPU.

```
              ADDR 1      ADDR 0
               (A1)        (A0)

                 0           0       Register A
                 0           1       Register B
                 1           0       Register C
                 1           1       Control Word
```

RD: Read Input. When low, specifies a read <u>(into</u> the MPU) is
           occurring. This is considered "input."
WR: Write Input. When low, specifies a write <u>(from</u> the MPU) is
           occurring. This is considered "output."

Further details of the 8255 IC's operation can be found in the Schematics/
Reference section.

2.2.6.2.1 <u>Port 1.</u> Port 1 is enabled by the -PORT 1 signal. It is generally
operated in Mode 0. The control word from the MPU programs the port for input
through Register A and output through Registers B and C.

2.2.6.2.1.1   Status Inputs. The six bits of Register A that are used provide
status to the MPU of the following:

                 Bit 2   EIA option 3
                 Bit 3   EIA option 2
                 Bit 4   Carrier Detect
                 Bit 5   Clear to Send
                 Bit 6   Keyboard Interrupt
                 Bit 7   Real-Time Clock Interrupt

2.2.6.2.1.2   Baud Rate Counter. This counter produces a square wave at 1,
16, or 64 times the baud rate frequency. The USART clock frequency require-
ments vary according to the USART programming (the "mode" instruction) and
the desired baud rate. The mode instruction determines whether this clock
must be 1, 16, or 64 times the baud rate. (64 is generally used for baud
rates below 1200.) A factor is loaded into Register B of the 8255 by the MPU,
and the counter, driven by $\Phi T2$ is counted up until it overflows. When this
happens, the same factor is reloaded and the counting resumes. The overflow
also toggles a D-type flip-flop, which further divides the count by 2 and
makes the output symmetrical.

The USART clock can also be supplied by an external source via board pin 4,
when the correct jumper wire is installed. Furthermore, during synchronous
data transmission/reception, the USART's receive clock is provided by the
modem. In this case, a jumper on the HPRO3 board must be changed to separate
the transmit and receive clocks.

2.2.6.2.1.3   Interrupt Enable/Disable. Each of the four types of interrupts
that can be generated on the HPRO3 board can be individually enabled or
disabled. A "1" loaded into the C Register enables, while a "0" disables, as
follows:

                 Bit 4   USART receive
                 Bit 5   USART send
                 Bit 6   Keyboard
                 Bit 7   Real-Time Clock

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2.2.6.2.2 <u>Port 2.</u> Port 2 is selected by the -PORT 2 signal, and is generally operated in Mode 1. The control word from the MPU programs the port for input through Registers A and B. The Register C bits are used mostly for control/status in Mode 1, but two bits, PC6 and PC7, are still available for I/O, and in this port they are used for output.

2.2.6.2.2.1 Keyboard (Parallel) Input. Data, in the form of 8-bit parallel bytes on the -DATA∅ through -DATA7 lines, is continually applied to the Register A inputs. As long as the Register A strobe input, which is PC4 (pin 13) in the Mode 1 configuration, is low, this data is loaded into Register A. +KYSTB is normally high, so after it drops low and then goes high again, the KEYBOARD INTERRUPT flip-flop sets on the trailing (positive-going) edge. As soon as this flip-flop sets, it latches the data into Register A; at this point the eight parallel inputs may be removed or changed without altering the data in the register.

When the KEYBOARD INTERRUPT flip-flop sets, it also presents an interrupt to the MPU (provided keyboard interrupt has been previously enabled). When the MPU recognizes the interrupt, part of its interrupt service routine is an instruction to read from Register A, to input the data to the MPU. Following this, it also performs a pair of "bit set/reset" instructions: the first to put a "low" on PC6 to clear the KEYBOARD INTERRUPT flip-flop; the second   to put a "high" back on PC6 to enable the flip-flop to be set again by the next +KYSTB. The MPU also reads the function key status from Register B as part of this interrupt service routine.

Note that +BUSY is driven high when the KEYBOARD INTERRUPT flip-flop sets, and remains high until after the flip-flop is cleared and reenabled. This signal can be used by an 8-bit parallel input device as a ready/not ready indicator; when +BUSY is high, it indicates that +KYSTB signals will not be accepted. The 8-bit parallel input device should present +KYSTB only when +BUSY is low.

2.2.6.2.2.2 Function Key Status. The keyboard function key signals, as well as the status of the three options, are continually applied to Register B. In Mode 1, the Register B strobe is received on PC2 (pin 16). The +SYNC signal from MPU thus latches the status of the function keys and jumper options into Register B.

These signals do not produce an interrupt. Instead, their status is read from Register B by the MPU each time it services an interrupt caused by +KYSTB.

2.2.6.2.2.3 Real-Time Clock One-Shot. The Real-Time Clock one-shot is controlled by the individual bit set/reset feature of the 8255. Bit 7 in the C Register (PC7, pin 10) is controlled by the MPU: when it goes high, the one-shot fires; when it goes low, the one-shot is enabled to fire again. PC7, when high, must first go low, then return to high to start the 10 ms timer.

2.2.6.3 Off-Board I/O

Input from or output to logic circuits external to the HPRO3 board can be accomplished in either of two ways: programmed I/O or direct memory access. Programmed I/O can occur either through the mother board connector (P1) or the control panel connector (J2). DMA transfer can occur only through the mother board.

2.2.6.3.1 <u>Programmed I/O</u>. This is accomplished in the same manner used for on-board I/O. An I/O port, #3 through #7, is addressed, and -READ or -WRITE is developed. If necessary, +ADDR ∅ and +ADDR 1 may be used to further define the address (as when an 8255 IC is used). All data is transferred between the MPU and the off-board port over the bi-directional data bus.

Port 3 must be accessed through the control panel connector. (-READ and -WRITE are passed through the drivers, and become -RD and -WR.) Ports 4 through 7 must be accessed through the mother board. Port 4 is generally reserved for DMA, and Ports 5, 6, and 7 are generally used for the printer.

2.2.6.3.2 <u>Direct Memory Access</u>. Data can be transferred directly between memory and an external device following the procedure outlined in 2.2.5.5. In this case, data is transferred directly between memory and the external device over the bidirectional data bus; the MPU stops in a "Hold" condition while the transfer takes place.

2.2.7   <u>Miscellaneous Circuitry</u>

2.2.7.1   3-Terminal Voltage Regulators

There are three 3-terminal voltage regulator ICs, shown on sheet 1 of the HPRO3 logic drawing, that provide the source of -5V, -12V, and +12V. These voltages are derived from the $\pm$15V provided by the power supply, which also provides +5V.

2.2.7.2   Level Converters

The input and output voltage level converters provide the interface between the TTL inputs and outputs of the USART and the 12V (nominal) requirements of RS-232-C.

More information concerning these ICs (75150 and 75154) can be found in the integrated circuit information in the Schematic/Reference section of this manual.

2.2.7.3   Options

There are four options on the HPRO3 board that provide variations in operation. These are covered in detail in the installation section.

2.3 8080 INTERFACE BOARD, Part No. 40644-03

The 8080 INTERFACE board contains I/O Ports 5, 6, and 7, which transfer data and control/status information between the terminal microprocessor and the printer microprocessor. It also contains logic that receives and temporarily stores carriage and printwheel position feedback signals from the SERVO board and supplies this data to the printer microprocessor when requested. Other circuits provide option jumper status to the printer microprocessor and develop the CLOCK A signal used by the printer microprocessor.

2.3.1 I/O Ports 5, 6, and 7

Ports 5, 6, and 7 are used to synchronize the transfer of information between the two processors. When the terminal microprocessor performs an output instruction to port 5, 6, or 7, the output information is stored on the 8080 INTERFACE board, where it is available to the printer microprocessor. The printer microprocessor periodically "reads" the 8080 INTERFACE board to see if there is any information that it should process. Similarly, as the printer microprocessor goes through its steps of controlling the printer, it provides status information to the 8080 INTERFACE board. This status is monitored by the terminal microprocessor prior to each output command.
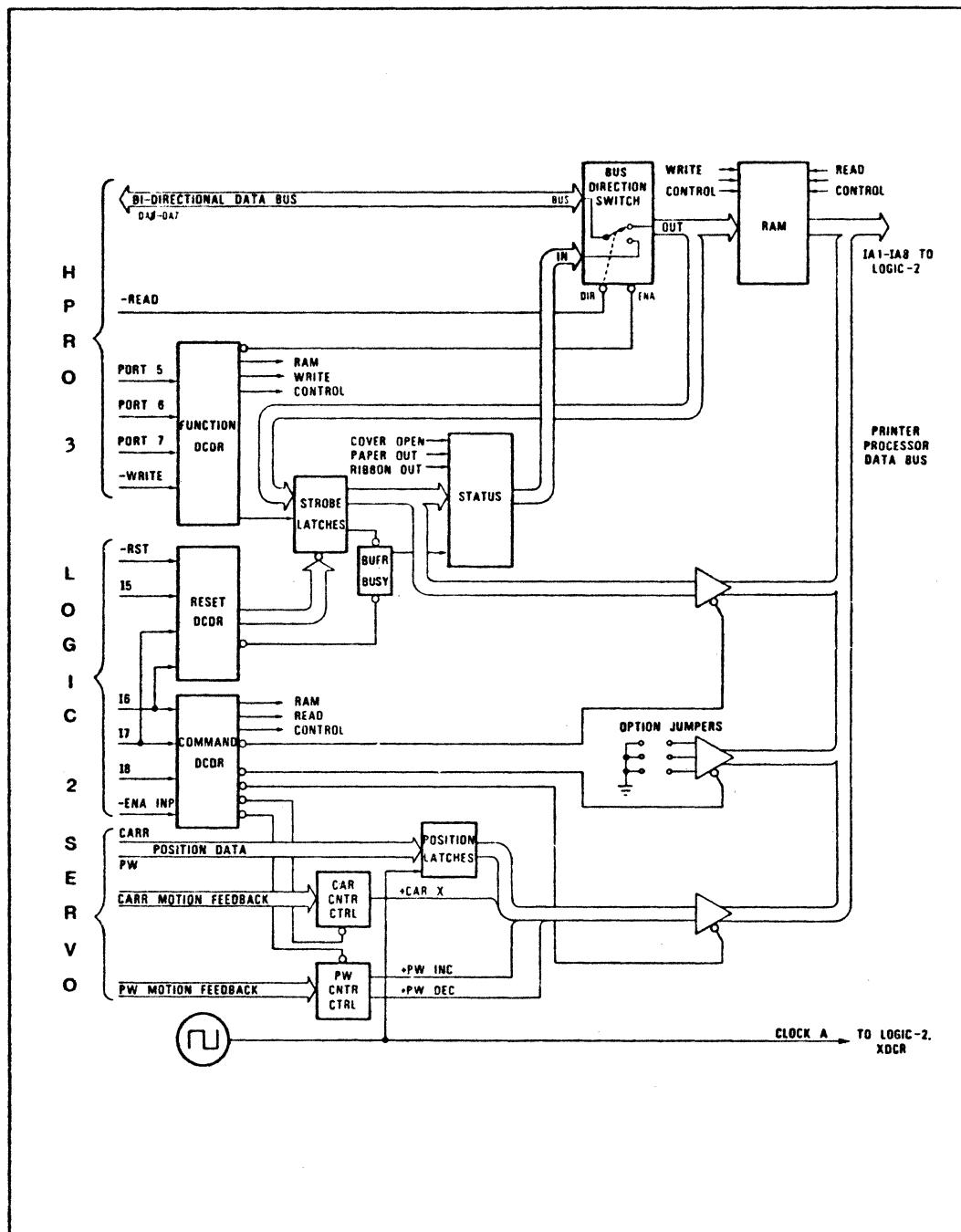

Figure 2-8. Block Diagram, 8080 INTERFACE Board

2.3.1.1 TRANSFER OF INFORMATION TO THE PRINTER

The transfer of a printer command from the terminal microprocessor to the printer microprocessor involves the following steps (refer to Figure 2-8):

(1) Terminal microprocessor "writes" low-order eight bits to port 6 (stored in RAM).

(2) Terminal microprocessor "writes" high-order bits (and direction bit) to port 7 (stored in RAM).

(3) Terminal microprocessor "writes" control word, containing strobe bit, to port 5 (stored in STROBE LATCHES), and sets BUFFER BUSY flip-flop.

(4) Printer microprocessor "reads" STROBE LATCHES to determine nature of command.

(5) Printer Microprocessor reads high-order bits and direction bit from RAM.

(6) Printer microprocessor reads low-order eights bits of data (from RAM), resets BUFFER BUSY.

2.3.1.1.1 WRITE to Ports 6 and 7.

When a write command is executed to either port 6 or 7, the data appears on the bi-directional data bus simultaneously with the development of the −WRITE signal and −PORT 6 or −PORT 7. The FUNCTION DCDR block in Figure 2-8 contains random logic which both enables (turns on) the BUS DIRECTION SWITCH, and addresses the RAM according to the I/O port selected. Since −READ is high at this time, the BUS DIRECTION switch allows data to flow from its "bus" connection to its output, from where it is written into the RAM.

2.3.1.1.2 WRITE to Port 5.

The control word, containing the strobe bit (or control bit, in the case of printer control functions) appears on the bi-directional data bus as −WRITE and −PORT 5 are developed. Data flow through the BUS DIRECTION SWITCH is again from the "bus" connection to the output, only this time the information on the output is not written into RAM. Instead, it is clocked into the STROBE LATCHES. Normally, only one of these latches is set at a time. The BUFFER BUSY flip-flop also sets at this time.

2.3 1.1.3 Read Strobe Latches.

The printer microprocessor, as part of its normal processing loop, reads the contents of the STROBE LATCHES. It provides the conditions on the I5 through I8 lines (along with the −ENABLE INP signal) to gate the contents of the latches onto the IA1-IA8 bus, from where the information is received by the printer microprocessor on the LOGIC-2 board.

Depending upon the nature of the information it receives from the STROBE LATCHES, the printer microprocessor performs different operations. For example, should the RC (Ribbon Control) or RSTR (Restore) latch be set, the printer microprocessor will immediately execute the appropriate control action. On the other hand, if either the CAR (Carriage), PW (Printwheel), or PF (Paper Feed) latch is set, the printer microprocessor will go through the steps necessary to read in data from RAM storage: (The OPT latch is not used.)

2.3.1.1.4 Read RAM Data.

After sensing either a carriage, a paper-feed, or a printwheel strobe, the printer microprocessor is directed to the steps in its microprogram that allow it to read the data stored in the RAM. The storage locations read are the same in all three instances. It reads the high-order bits first by supplying the correct combination of signals on the I5-I8 lines. It then reads the low-order eight bits from the other RAM location, and finally, it resets the BUFFER BUSY flip-flop.

2.3.1.2 TRANSFER OF INFORMATION FROM THE PRINTER

The only information received from the printer is status information. It is received by the terminal microprocessor when it performs a READ instruction from port 5. Ports 6 and 7 are not used for input to the terminal microprocessor.

The −PORT 5 signal, through the FUNCTION DCDR, turns on the BUS DIRECTION SWITCH. This time, however, −READ, being low, guides status information on the switch's input to the "bus" connection, where it is placed on the bi-directional data bus and provided to the terminal microprocessor. In addition to the contents of the STROBE LATCHES, this status information also provides COVER OPEN, PAPER OUT, and BUFFER BUSY status.

2.3.2 Carriage and Printwheel Position Data

This portion of the 8080 INTERFACE logic is identical to that found on a standard HyType II LOGIC-1 board. It consists basically of two groups of logic, the "position latches" and the counter control flip-flops.

2.3.2.1 POSITION LATCHES

On earlier boards (40644-01 and -02), there are four position latches, one each for the carriage and printwheel "even" signals, and one each for the carriage and printwheel "home" signals. These four signals occur at random in relation to the printer microprocessor operation, so they are synchronized to the microprocessor by clocking the latches with +CLOCK A. On later boards (40644-03) those latches are eliminated because other circuit changes and printer microprocessor program alterations make them unnecessary.
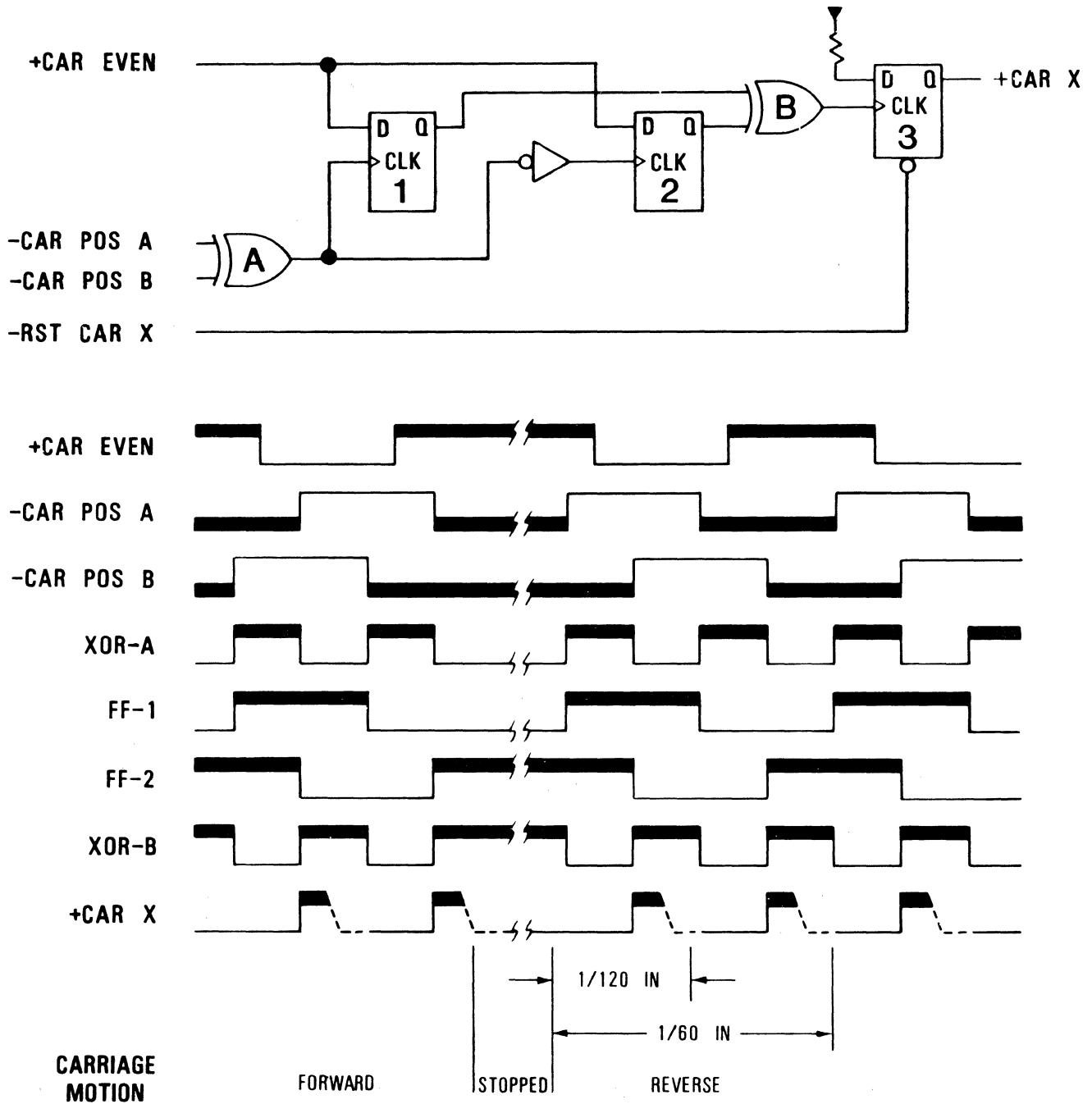
Figure 2-9. Carriage Counter Decrement Control.

DATA FROM
8080 INTERFACE
BOARD

{ IA1
  ↕
  IA8 }

B

REG

TABLE

ROM

ADDER/

COMPAR-
ATOR

RAM

ADDR

A

REG

PRGM

CNTR

PRGM

ROM

OUTPUT

LATCHES

ADDR

DCDR

— — — DATA PROCESSING
—·—·— PROGRAM CONTROL
·········· DATA OUTPUT

DATA & CONTROL
SIGNALS TO OTHER
PRINTER BOARDS

I5
↕
I8

} INSTRUCTIONS TO
  8080 INTERFACE
  BOARD

} CONTROL SIGNALS
 FOR THIS BOARD
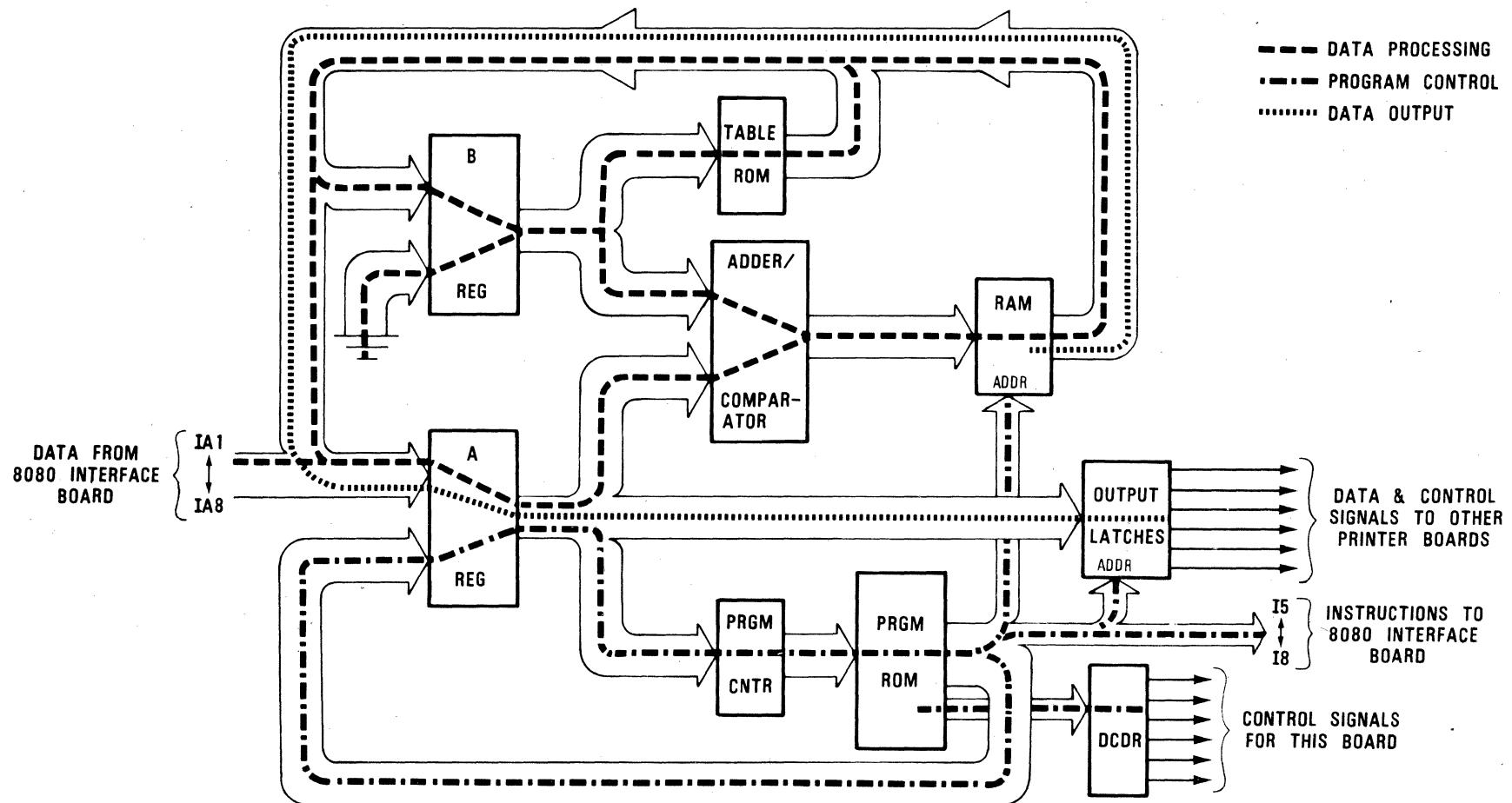
Figure 2-10. Block Diagram, LOGIC-2 Board

2.3.2.2 CARRIAGE COUNTER CONTROL

When a carriage movement command is received, the printer microprocessor loads a value, representing the number of 1/120-inch increments the carriage is to move, into a "difference counter" (in RAM). It then initiates the carriage movement, the amount of drive current fed to the carriage motor being controlled by the printer microprocessor according to the value in the difference counter. Signals fed back from the carriage motor's rotary transducer are used to decrement the difference counter for each 1/120-inch of movement. When the difference counter is decremented to zero, the carriage movement is complete, and the microprocessor terminates the operation.

The CAR EVEN (Carriage Even), CAR POS A, and CAR POS B (Carriage Position A and B) signals are developed on the SERVO board; they are derived from signals fed back from the carriage motor's rotary transducer. Their timing relationships are shown in Figure 2-9, along with waveforms of the 8080 INTERFACE board circuitry that they drive. These three input signals each make one full "cycle" for each 1/60 inch of carriage movement, which results in a single pulse on the +CAR X line for each "half cycle," or 1/120-inch increment of carriage travel.

Once it has initiated carriage movement, the printer microprocessor "reads" the +CAR X line periodically to monitor the carriage movement. When it finds +CAR X high, it decrements the difference counter, and issues an instruction to reset the counter control flip-flop. Since the response time of the printer microprocessor will vary, the length of the +CAR X pulse in Figure 2-9 is shown by a dotted line.

2.3.2.3 PRINTWHEEL COUNTER CONTROL

The printer microprocessor maintains a running log of printwheel position in its "printwheel absolute position counter," located in RAM. Thus, the microprocessor always "knows" the current printwheel position, and when it receives a command to print a new character, it calculates the shortest direction and the distance to be moved to access the new character. It then initiates printwheel movement, and uses feedback signals from the printwheel motor's transducer to update the absolute position counter. Since the printwheel can move in either direction, the counter can be either incremented or decremented. Each time the microprocessor increments or decrements the counter, it compares the counter with the desired destination; when the two are equal, it removes printwheel motor drive current and steps to the hammer-fire sequence. (This logic also keeps track of printwheel position should the wheel be turned by hand.)

Logic on the 8080 INTERFACE board receives the three feedback signals from the SERVO board, PW EVEN (Printwheel Even), PW POS A and PW POS B (Printwheel Positions A and B). Depending upon the sequence in which the position signals appear (determined by printwheel direction of rotation), either +PW INC (Printwheel Increment) or +PW DEC (Printwheel Decrement) will be developed. The printer microprocessor continually monitors these two signals and, finding one or the other high, it makes the appropriate change to the printwheel absolute position counter, and outputs an instruction back to the 8080 INTERFACE board to clear the PW INC or PW DEC flip-flops.

The logic that develops +PW INC and +PW DEC is very similar to that which produces +CAR X, shown in Figure 2-9. The major difference is that there are six flip-flops instead of three, because both increment and decrement pulses must be developed. Only three flip-flops set/reset during each printwheel movement, depending upon the direction of rotation; the other three remain static.

2.3.3 Option Jumpers

There is provision for three jumpers to be installed on the 8080 INTERFACE board. Jumper H67, providing terminal microprocessor control of printwheel addressing and hammer energy, must be installed. Jumper H70, providing terminal microprocessor control of ribbon advance, must not be installed. Jumper H73 provides for $\frac{1}{2}$ the normal ribbon advance; it may be installed if carbon film ribbons will not be used.

2.3.4 Oscillator

A simple LC feedback oscillator provides the CLOCK A signal at 5 MHz, ±10%. This signal controls circuitry on the 8080 INTERFACE board and on the XDCR board, and provides the basic clock for the printer microprocessor on the LOGIC-2 board.

2.4 LOGIC-2 BOARD, PART NO. 40510-4X

The LOGIC-2 board contains the printer microprocessor. Refer to the block diagram in Figure 2-10. The wide buses represent 8-bit bytes of data, and the narrow buses represent three or four bits. The Output Latches provide over 30 separate signals to the other printer boards.

The A and B registers provide temporary storage for data. Both are 8-bit registers with the capability of accepting data from either of two 8-bit data sources (although one of the B-register's sources is hard-wired to provide all zeros). The Table ROM contains up to 512 8-bit factors (e.g., hammer intensity values) used by the microprogram; the Program ROM provides up to 512 16-bit instructions. The computation logic contains an adder and a comparator. When necessary to simply pass data through the adder to the RAM, the microprogram adds zero to the data. RAM capacity is 32 8-bit bytes. RAM output is the complement of its input data. The output latches store over 30 bits of output data, but a maximum of eight of them can be changed at any one time.

The buses are connected to form three interrelated loops: a Program control loop, a Data Processing loop, and a Data Output loop. The Program Control loop components control the other two loops. Thus they control all data movement on the LOGIC-2 board, as well as all data movement to and from the board.

2.4.1 Program Control Loop

After initialization, the Program Counter is reset, and first addresses location zero of the Program ROM. This ROM acts as both Program Memory and Instruction Register. That is, it contains all printer microprocessor instructions, and, when addressed by the Program Counter, outputs the current instruction for as long as necessary for completion.

For sequential program execution, the complete Program Control loop is not used. Instead, the Program Counter, the Program ROM, and the decoder are all that is needed to control data flow in the other two loops. The A register is still used, however, to feed "immediate" data from the Program ROM to the Data Processing loop. The Program Control loop is completed when it becomes necessary for the program to "branch" or "jump" to a non-sequential location. When this occurs, the new instruction address is first loaded into the A-register, and then transferred to the Program Counter. The next instruction executed is that located in the Program ROM at the new address.

2.4.2 Data Processing Loop

The data processing loop receives data from one or two of four possible sources, performs some mathematic operation on this data, and stores the result in RAM.

The sources of data are (1) the 8080 INTERFACE board, (2) the Table ROM, (3) the RAM, and (4) the Program ROM. The A and B registers are used as working registers, to temporarily hold the two 8-bit data bytes being manipulated. Possible operations include adding the two bytes together, subtracting the A register byte from that in the B register, comparing the two bytes to see if they are equal, complementing the RAM data, and passing data through unchanged.

2.4.3 Data Output Loop

Data is read from RAM, loaded into the A register, and then loaded into the Output Latches, where it is continually available to the rest of the printer. Note that since the RAM output is inverted, the complement of the desired output data must be stored in RAM by some previous instruction.

This loop is used only for printer control data. Output to the 8080 INTERFACE board is in the form of instructions (on the I5-I8 lines) which are decoded on that board to provide the desired action.

2.4.4 Basic Operation

Refer to Figure 2-11. Instruction execution is divided into two halves, called phase 1 and phase 2. The op code is present on the I1-I3 lines during both phases. The "from" address, or data source, is on the I5-I12 lines during phase 1, and the "to" address, or destination, is on the I5-I8 lines during phase 2. The I9-I12 lines are not used during phase 2.

The I4 line is used primarily to extend the ROM addressing capability; the I5-I8 lines are used for the basic RAM address, and the I4 line selects which of two sets of RAMs will be used.

2.4.5 Timing

Figure 2-12 illustrates the basic timing involved in the operation of the printer microprocessor. Two clock signals, +B and +C, are derived from the −CLOCK A signal (from the 8080 INTERFACE board) once +POWER ON goes high. The +C clock is used to divide the instruction execution into the two phases, and the +B clock provides intermediate timing. The A Register is loaded at the end of every phase 1, when −C goes low. The B Register is loaded at the midpoint of every phase 2, when +B goes low. The final waveforms in Figure 2-12 illustrate the timing of several important signals relative to the B and C clocks; note that these final signals do not occur in <u>every</u> instruction cycle, but only in those requiring them.

2.5 SERVO BOARD, PART NO. 40520-XX

As shown in Figure 2-13, this board logically follows the 8080 INTERFACE board and the LOGIC-2 board. It has four functions. First, it receives strobed processed command data from the LOGIC-2 board, and converts this digital data input to a voltage level representative of the absolute value of the desired velocity at which the carriage or printwheel is to be moved. Since incoming data is multiplexed, this D-to-A converter part of the circuit is common, with the printwheel and carriage functions being steered to nearly identical but separate sample and hold circuits. The voltage level output from the sample and hold circuit is then switched in polarity to control the direction of movement, and the resultant polarized voltage is
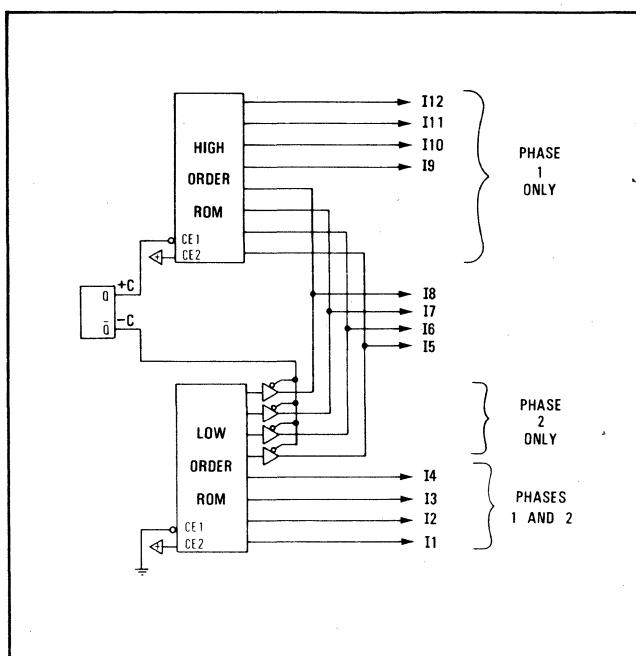
Figure 2-11. Basic Operation, Printer Microprocessor

presented to a summing amplifier. This represents the velocity command signal. Second, dual tachometer circuits convert incoming analog position signals to a voltage level which represents the actual servo velocity. Three digital position signals are derived from the analog position signals by a series of comparators. These digital position signals represent distance moved, and are supplied back to the 8080 INTERFACE board where they are used to generate increment and/or decrement counts for the position mem-

ories on the LOGIC-2 board. Third, the voltage level of velocity is summed with the velocity command signal to generate a 0 to 7 volt maximum servo error signal used to develop the actual servo motor drive current. Fourth, the D-to-A converter output is used on a multiplexed basis to process print hammer energy commands.

Refer to Figure 2-13 and to the schematic diagram to aid in understanding the following discussions.
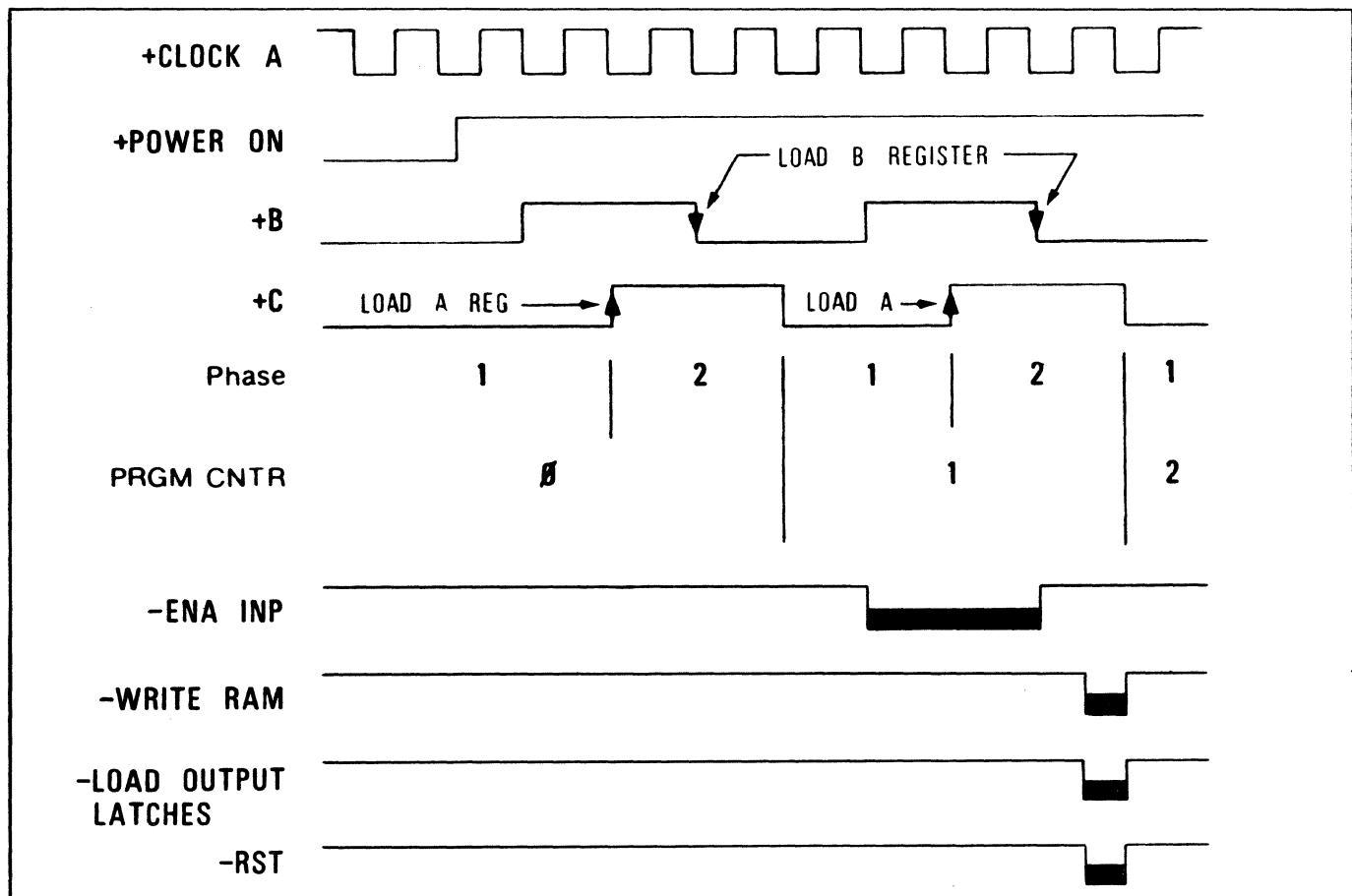
Figure 2-12. Basic Timing, Printer Microprocessor
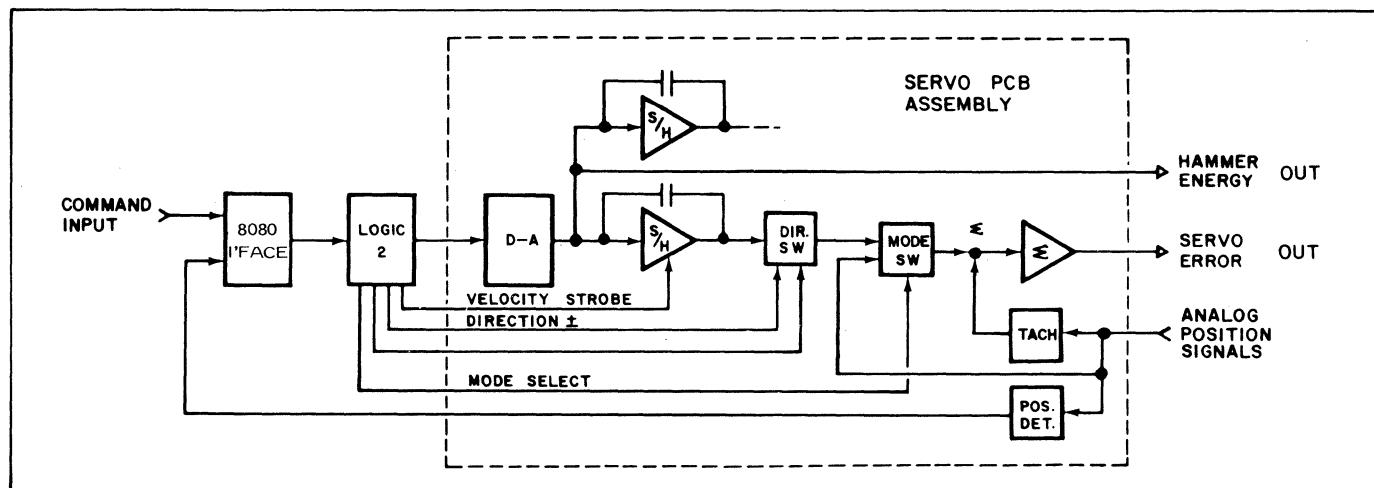
Figure 2-13. Block Diagram, SERVO Board

2-27

2.5.1 D-A Converter Circuit

This common input stage serves both the carriage and printwheel channels as well as the print hammer circuit. It consists of an 8-bit D-A converter, an operational amplifier, a buffer/driver transistor, and associated components as shown in Figure 2-14.

A reference current generator, consisting of resistors F9 and F10 and noise suppressing capacitors F6 and F7, provides a reference current for the D-A Converter G12, a monolithic 8-bit digital-to-analog converter. It supplies an output current which is the product of the 8-bit digital word input and the reference current input. This output consists of the decimal equivalent of the binary weighted value of the digital input divided by 256 such that if ALL inputs were high (=255), the output current would equal 255/256 or 99.6% of the reference current.

The output of G12 is supplied to operational amplifier E12-6. This amplifier, with its associated components, comprises a current-to-voltage converter. Buffer/driver transistor E6 in its feedback loop provides a drive current source for the stages following, through resistors D10 and F23. The output level from transistor E6 is 0 volts (all inputs low) to approximately +9.95 volts (all inputs high).

During hammer-fire sequences, this circuit is utilized to provide a time/amplitude profiled output to the hammer drive circuits which serves to regulate the print hammer energy synchronized with the character to be printed, where some characters, such as periods and commas, require much less printing energy than others, such as the M.

2.5.2 Sample and Hold Circuit

Figure 2-15 illustrates a typical Sample and Hold circuit with the basic timing involved. As shown, the circuit consists of an input switching FET, an operational amplifier (A) coupled to a buffer/driver transistor (Q), and associated components.

In operation, the output of the D-A Converter is presented to the switching FET through a resistor R1 (shown as resistors D10 and F23 on the schematic diagram). Approximately 6 microseconds after the arrival of data on the data bus input to the D-A Converter, the printer microprocessor issues a 2-microsecond Velocity Strobe pulse through an inverter and voltage divider network to turn on the switching FET. When on, the FET couples the output voltage from the D-A Converter to

holding capacitor C in the feedback circuit of amplifier A. Capacitor C holds this voltage until the printer microprocessor again strobes the D-A output. The microprocessor's cycle rate is such that it may update the charge on the capacitor 100-200 times before it actually modifies the data. The processor can modify this data only when the associated transducer has experienced a "track crossing", which occurs each time the carriage or printwheel has moved one increment. Amplifier A follows and inverts the charge on capacitor C, to produce a 0-to-negative-going voltage which represents the velocity command for the associated servo. Transistor Q buffers the amplifier's output, and provides drive current for the circuits following.

2.5.3 Servo Direction Switching

Refer to the schematic diagram. The carriage and printwheel Sample and Hold circuits are nearly identical. Each contains two paths. One path goes through a 2K resistor to a switching FET, while the other path goes through an inverting operational amplifier to a second switching FET, with the output of both FETs tied together. This means that the negative-going output of the Sample and Hold circuit is supplied as a negative-going voltage to one FET and as a positive-going voltage to the other FET. The gates of these FETs are controlled by inputs from the printer microprocessor, labeled FWD and REV, through inverters and voltage divider networks. The microprocessor can then select the correct polarity of signal to be presented to the summation circuit to control ultimate direction of servo movement.

During those times in printer operation when carriage and/or printwheel motion has stopped, and before the hammer-fire sequence is complete, the associated servo must be detented to hold its position. To accomplish this, a signal called LINEAR POS SIG is generated on the XDCR board and presented to a third switching FET whose output is also tied to the summation circuit. This FET is A12-7 for the carriage circuit, and A32-15 for the printwheel circuit. The input to the gates of these FETs comes from the printer microprocessor through the normal inverter/divider network, and is labeled LINEAR MODE. This associated servo system is detented when the microprocessor gates the LINEAR POS SIG to the summation point, while at the same time holding the two associated position switching FETs in their off state.

30 ms after gating in the LINEAR POS SIG following the last position command strobe, the printer microprocessor activates the SERVO DISABLE signal. This turns off the power amplifier and effectively removes current flow through the servo while it is at rest. This is called the "Float Mode".

In the printwheel circuit, the absolute counter is maintained in synchronization with printwheel position at all times, even if the printwheel is manually moved or should drift. In this way, printwheel movement in response to the next command can start from wherever the printwheel happens to be when the command is received.

Carriage position information is not maintained within the printer circuits. Any carriage drift or non-commanded movement would desynchronize the terminal microprocessor's carriage position information. Any carriage movement, therefore, triggers a response to remove the "float mode" and drive the carriage back to its last commanded position.
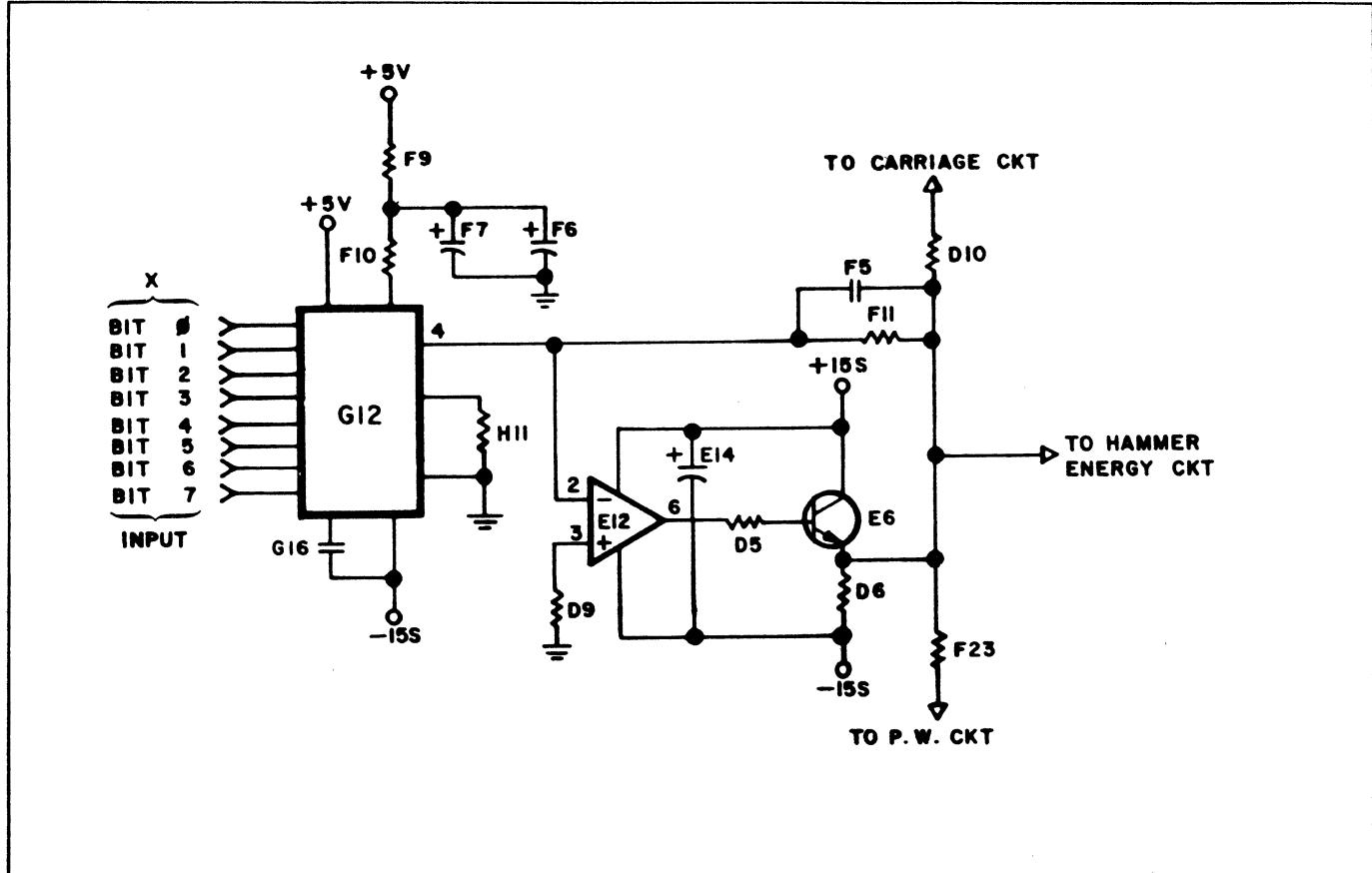
Figure 2-14. D-A Converter
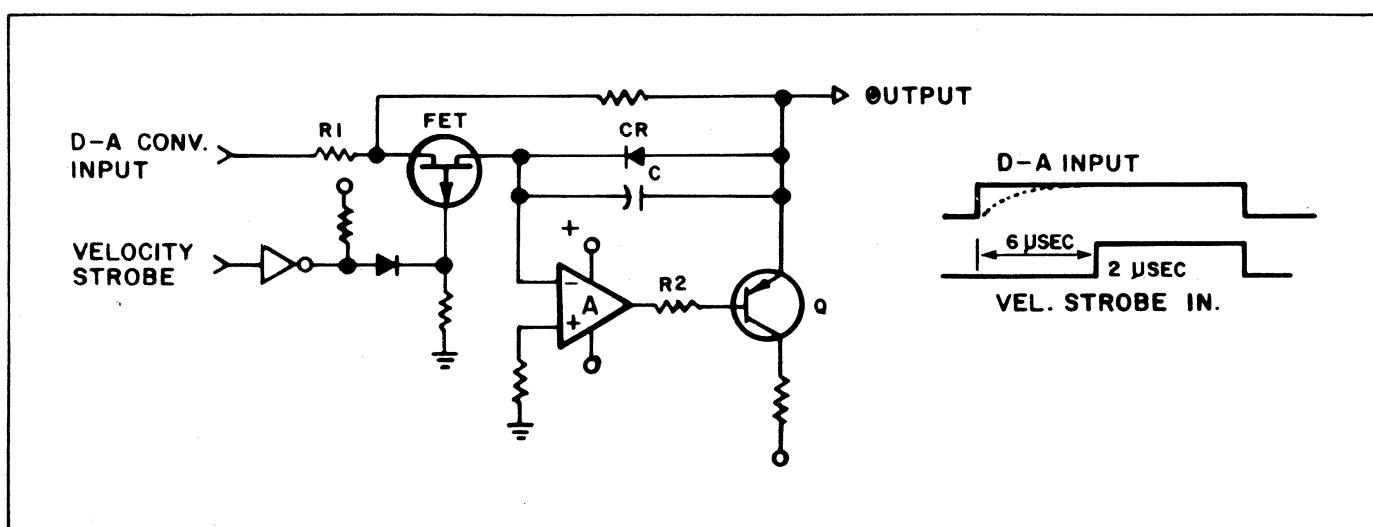
Figure 2-15. Typical Sample and Hold Circuit

2-29

2.5.4 Servo Tachometer Circuits

Refer to Figures 2-16, 2-17, and to the schematic diagram. The representative waveshapes shown in Figure 2-16 illustrate the development of the four signals $\phi 1$, $\phi 2$, $\phi 3$, and $\phi 4$ from the three POS SIG inputs from the XDCR board. The illustration also includes representations of those parts of the tachometer circuit which produce the waveforms.

Figure 2-17 then traces the development of the composite position waveform at the summation junction of the switching FETs from the POS SIG inputs using the four ϕ signals described above.

In operation, three phase-modulated triangular waveshapes are generated by the XDCR board circuits in response to movement of the associated servo motor shaft, and are supplied to this circuit as POS SIG 1, POS SIG 2, and POS SIG 3. One input, POS SIG 3, is applied to an inverting operational amplifier to produce the fourth signal used, —POS SIG 3. Each of these four position signals is fed through a differentiating R-C network to a switching FET. The three primary POS SIG inputs are also applied as inputs to two operational amplifiers to produce square wave outputs called C and D which are 90° out of phase with each other. These two square waves pass through a network of inverters and NAND gates to produce the four FET gating signals mentioned above, $\phi 1$, $\phi 2$, $\phi 3$, and $\phi 4$. These four signals turn the FETs on in sequence, as shown in Figure 2-17, gating through the differentiated position signal.
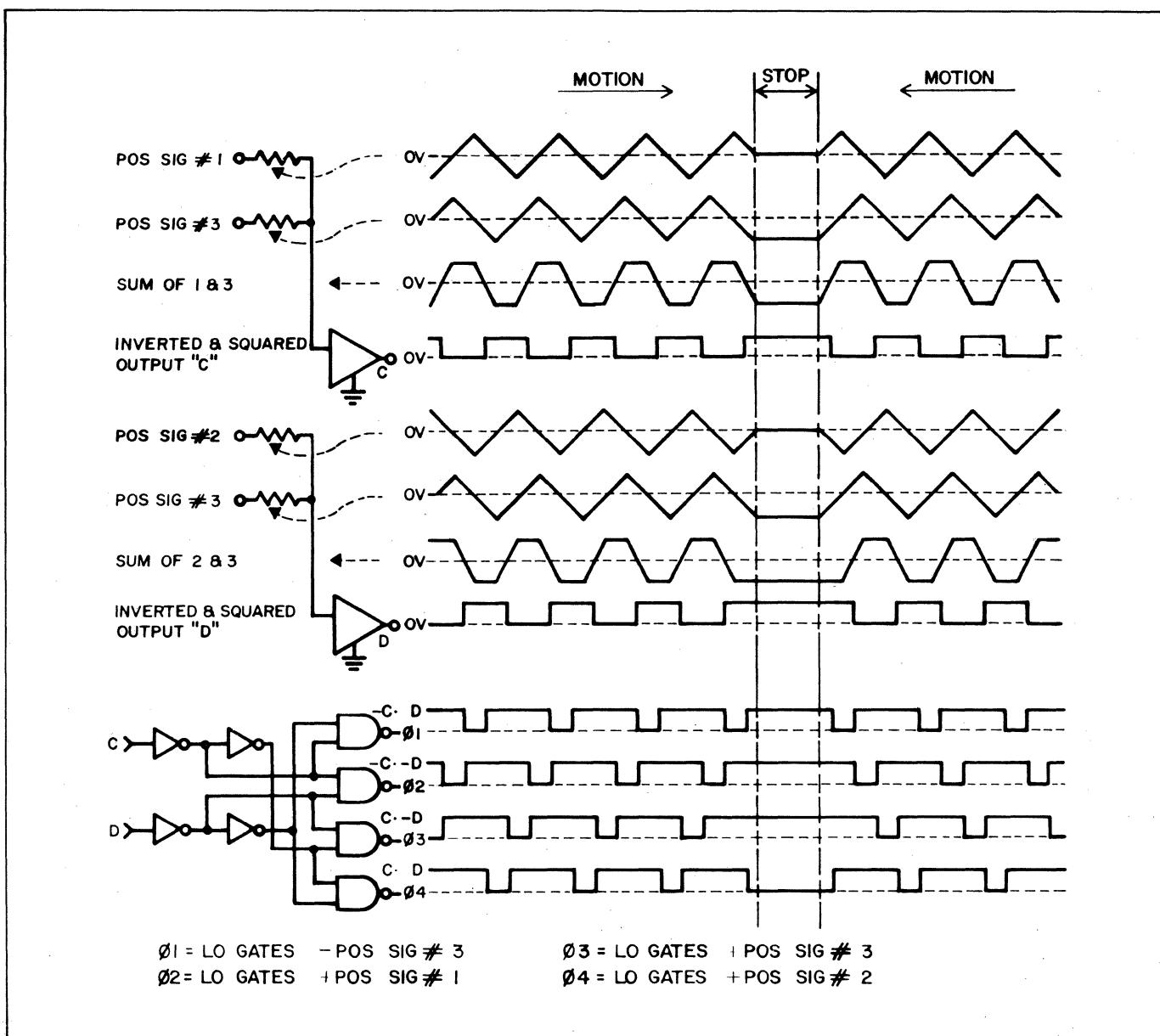
Figure 2-16. Servo Tachometer Waveforms A

The velocity input to each switching FET is derived by an R-C network, as mentioned above, which has the effect of differentiating the waveform portion gated through. All four such FET outputs are then multiplexed into an operational amplifier (C60-12 for carriage, and C48-10 for printwheel) whose output is then connected through a resistor to the summing junction of the velocity summing amplifier.

The waveforms shown in Figure 2-16 and 2-17 depict a forward and reverse motion at a constant velocity. Servo velocities of less than that indicated would produce a lower differentiated input to the tachometer output amplifier, while velocities greater than this would produce a higher input. As a result, the output from this circuit to the velocity summing amplifier is a voltage whose level is proportional to the actual servo velocity.

—C and —D square waves taken from the FET $\emptyset$ gate circuits along with the squared and reinverted —POS SIG 3 signal are also transmitted to the 8080 INTERFACE board for use in the position counter increment and/or decrement circuits. The —C output is labled —CAR or —PW POS A, the

—D output is labeled —CAR or —PW POS B, while the output of amplifier E72-7 for Carriage and E48-12 for printwheel is labeled +CAR or +PW EVEN.

2.5.5 Servo Summation Amplifier

This amplifier, C24-10 for carriage and C36-12 for printwheel, is the output of the servo velocity command circuit. It is an operational amplifier with a compensating capacitor, zener clamp diodes, and a gain resistor in its feedback loop. The back-to-back 6.2 volt zener diodes, plus their normal voltage drop, provide a bi-directional voltage clamp which limits the amplifier output to +7 volts. Since each volt of signal output here produces a fixed value of drive current later on in the servo motor, it is necessary to establish this voltage limit to safeguard the servo motor.

The input to this amplifier is then either the sum of actual velocity and velocity command voltages, or the LINEAR POS SIG input and velocity signal. The output is a voltage which is directly proportional to the desired amount of servo drive current. The output is labeled SERVO ERROR.
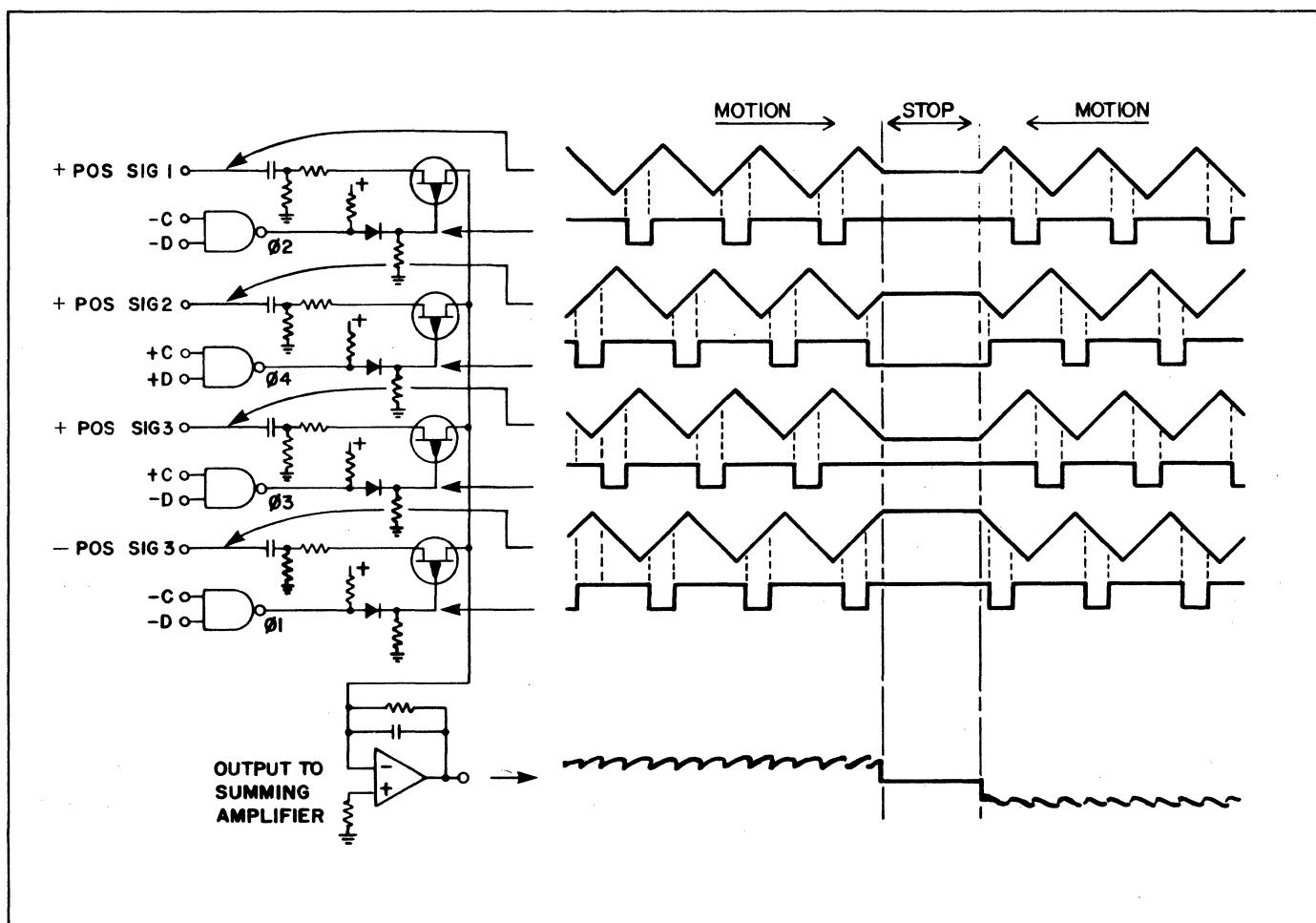
Figure 2-17. Servo Tachometer Waveforms B

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2.6 TRANSDUCER (XDCR) BOARD, PART NO. 40515-XX

This assembly contains all the circuits necessary to generate the sine wave drive for the carriage and printwheel transducer stator windings, to demodulate the resultant phase-modulated carrier coming from the transducer rotor winding, and to produce three triangular position signals and one linear position signal each for the carriage and printwheel tachometer circuits on the SERVO board. Refer to Figure 2-16.

2.6.1 Sine-Wave Drive Generator

Refer to Figure 2-18, and to the schematic diagram. The 6 MHz —CLOCK A input from the 8080 INTERFACE board is used to clock the H24 and H48 Shift Registers.

The outputs of these two modules, shown in the upper half of Figure 2-18, are channeled into a network of inverters, pull-up resistors, and load resistors. Each register output goes alternately high and low. The connected inverters act as switches, and when their outputs are low (register high), current can flow through their load resistor to two or more of the connected output lines of CAR 1, CAR 3, PW 1, or PW 3. As shown, seven of the eleven outputs are switched on and off progressively for each of the four output lines. This progressive switching adds and removes parallel current paths for the lines, generating a stepped or pyramidal current waveform. The values of the several load resistors are selected to "weight" the parallel inputs to form a generally sinusoidal envelope for the output. A capacitor across the output network helps smooth this curve further. Figure 2-19 shows actual waveforms which are typical of those found throughout this circuit.

Figure 2-18. Typical Theoretical Waveforms, Sine-Wave Drive Generator

2.6.2 Servo Position Transducer

The Servo Position Transducer consists of rotor and stator members made up as flat disks with "windings" laminated on adjacent surfaces. The rotor is mounted on the free end of the servo motor shaft, with the stator mounted over it and fastened to the motor casing. Output signals from the rotor are picked up by means of an axially mounted rotary transformer.

As shown in Figure 2-20, the stator has an eight-segment "winding," with alternate segments connected together to form two groups of four. The segments of one group are displaced laterally from the other group by a distance equal to one-half a winding width. This displacement is equal to a 90° phase difference. The rotor has one symmetrical winding.
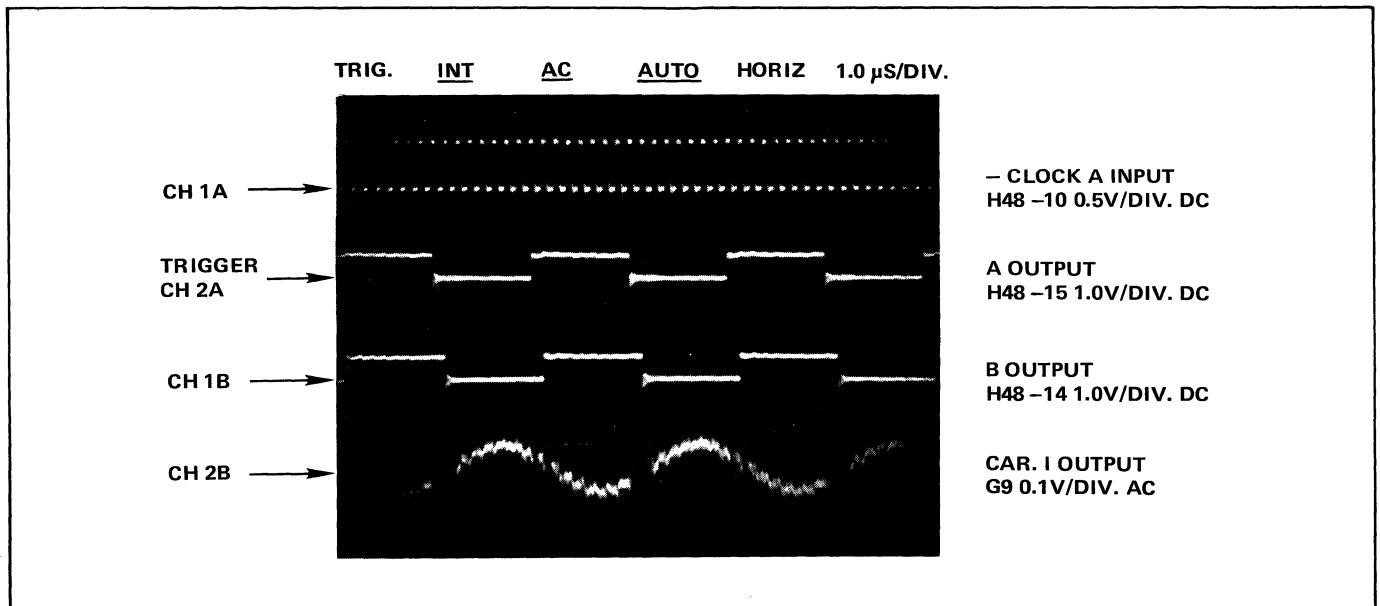
Figure 2-19. Actual Waveforms
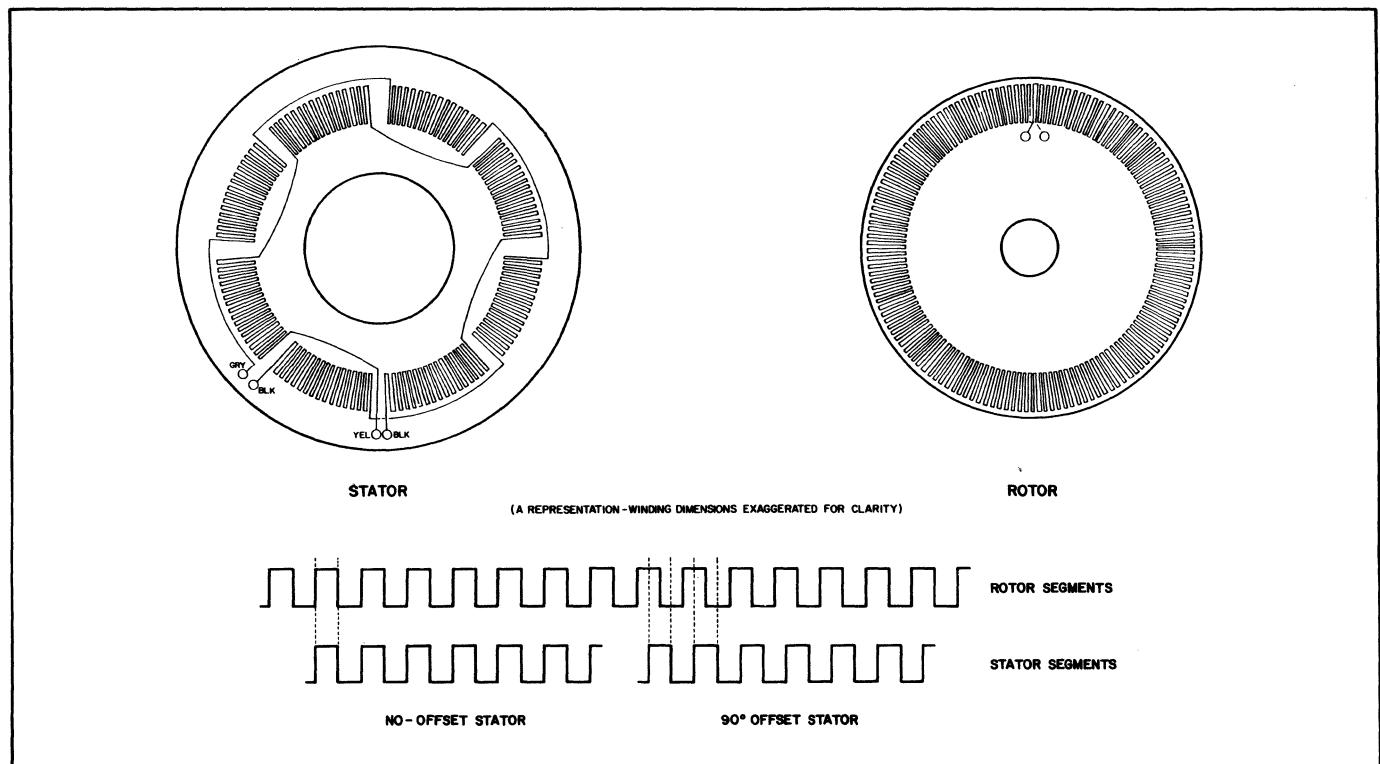
Figure 2-20. Servo Position Transducer

2-33
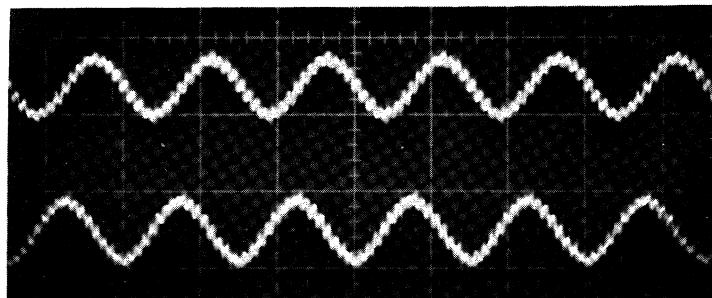
Figure 2-21. Typical Transducer Input Waveforms
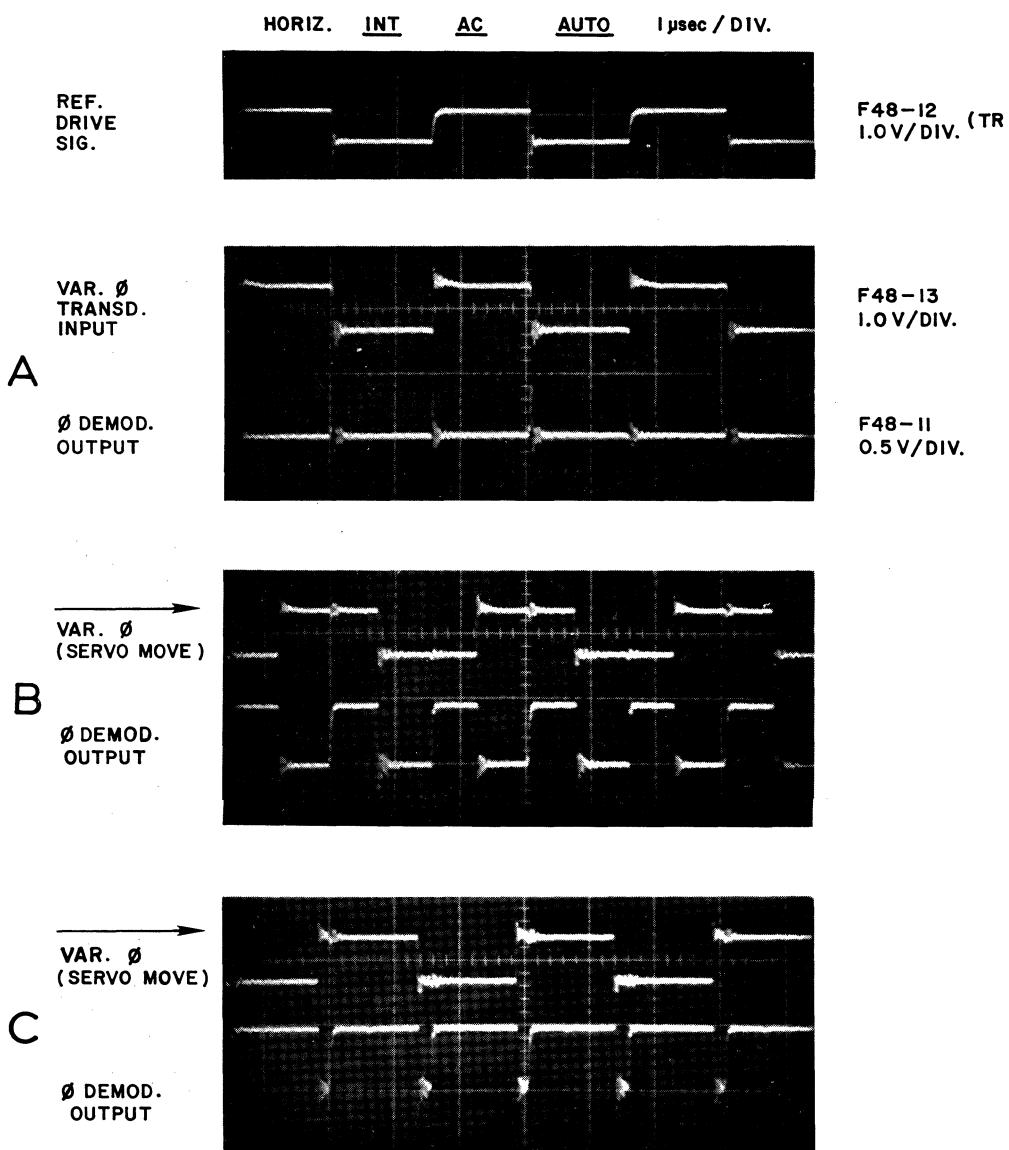
Figure 2-22. Typical Demodulator Waveforms

The two sinusoidal outputs from the Sine-Wave Drive Generator for a particular servo are introduced into the transducer's stator windings. Figure 2-21 shows a typical pair of these waveforms.

The phase-modulated output from the transducer is coupled to a circuit consisting of a two-stage RF amplifier and a squaring circuit. The output of this circuit, at F10-12 for the carriage transducer and F21-12 for the printwheel transducer, is a square wave whose phase with respect to the reference servo drive signal contains the servo position information.

This phase-variable square wave is placed on the input of an exclusive-OR gate, along with a reference square wave from the sine-wave generator. The resultant output is a pulse whose width varies with the phase difference between the two inputs. Figure 2-22 illustrates the development of this pulse.

The variable-width pulse trains from the carriage and printwheel exclusive-OR gates are connected into a network of integrating circuits followed by operational amplifiers and emitter-follower drivers. The integrating circuits develop a triangular position waveform from the exclusive-OR gate output. The network then produces the amplified triangular waveforms of POS SIG 1, 2, 3, and LINEAR for use in the Servo Tachometer circuits.

2.7 CARRIAGE POWER AMPLIFIER BOARD, PART NO. 40525-XX

This assembly includes the Carriage Servo Power Amplifier, the Paper Feed Drivers, and the Power Monitor circuits. It is located in board slot D, and has a finned heat sink attached to it, to help cool the several driver transistors.

NOTE

DO NOT stand the HyType II Printer on its rear heat sink panels. The finned heat sinks are mounted on plug-in circuit boards which can be easily damaged by this practice.

2.7.1 Carriage Power Amplifier Circuit

NOTE

This circuit is nearly identical to the Printwheel Power Amplifier Circuit described in Section 2.8.1

This circuit supplies and controls current flow to the carriage servo drive motor. It is designed as an "H" bridge, allowing all current to flow through the motor from supply to supply instead of through circuit ground, to avoid circuit noise problems. Figure 2-23 illustrates the basic circuit in simplified form, where certain transistors in the actual circuit are represented as switches. Closing switches S1 and S4 will cause current to flow through the motor and resistor R right to left, while closing switches S2 and S3 will cause current to flow left to right.

Referring to the schematic diagram and Figure 2-23 will aid in understanding the operation of the circuit itself. Since the amplifier is composed of several similar circuits, only one path will be discussed.

Assume a CAR SERVO ERROR signal input of +1 volt for a commanded motor current of 1 ampere. The output of operational amplifier B55-6 will be low, and this will place a low potential on the base of transistor G58 and on the emitter of transistor G73. G73 will turn off. G73 being off turns transistor E70 off, which turns transistor E65 on to turn on PULSE REV transistor F63.

The error signal is also supplied to amplifier A50-6, the output of which is zero volts with a positive input. This will turn off transistor D42, which turns D45 off and E44 on, which turns on DRIVE REV transistor D48.

Referring to Figure 2-23, transistor D48 is shown as switch S2, while transistor F63 is shown as switch S3. Turning these two transistors on establishes a current path from the +15 volt supply through D48, resistor C53, the drive motor, and F63 to the -15 volt supply.
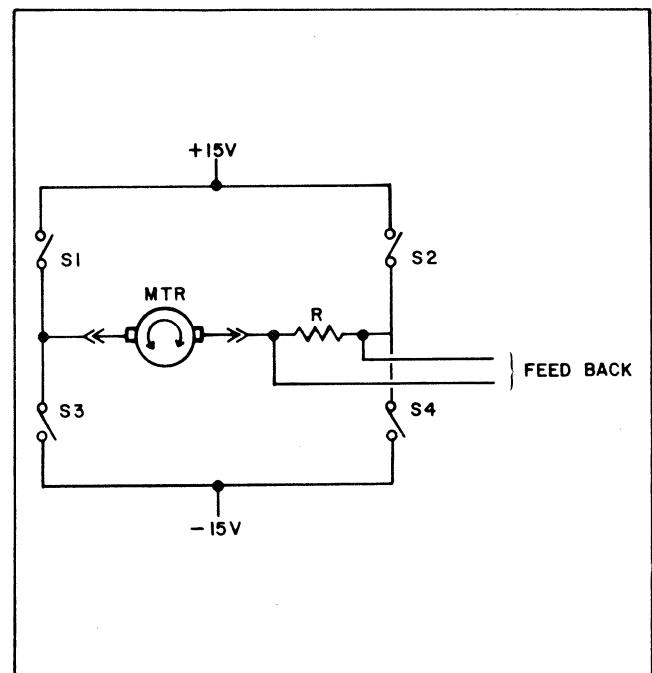
Figure 2-23. Simplified Diagram, Carriage Power Amplifier
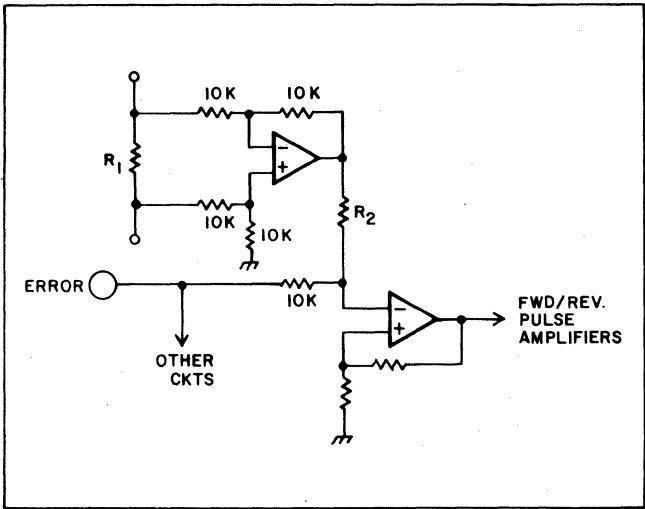
Figure 2-24. Feedback Instrumentation Circuit

Figure 2-24 is a simplified schematic diagram of the feedback circuit. This circuit includes the 0.1 Ohm resistor C53 located in one of the lines to the servo motor, across which is connected a precision balanced 10K Ohm resistor network and difference amplifier B62-10. The value of resistor C53 is such that its voltage drop to current ratio is 1 to 10 (0.1 volt drop equals 1.0 ampere of motor current). Difference amplifier B62-10 inverts this voltage, and presents the result to the servo error input terminal 2 of amplifier B55-6. The two signals are summed at a ratio of 10 input to 1 feedback. As current through the drive motor approaches the command level, the output of B55-6 will diminish. When motor current matches command current, the PULSE REV transistor F63 will be turned off. This removes motor current, which removes feedback voltage, and F63 is turned back on again. The circuit will oscillate in this manner to maintain motor current at the commanded level.

Should the Power Monitor circuit detect an input voltage error, it will turn transistor E77 on, turning off PULSE FWD and PULSE REV transistors F47 and F63 to disable carriage servo movement.

2.7.2 Power Monitor Circuit (Figure 2-25)

The purpose of this circuit is to inhibit paper feed, printwheel movement, and carriage movement by generating a series of disabling signals any time one or more of the three supply voltages drops below a level where incorrect operation might result. These signals also reset all printer microprocessor program and logic circuits to their initial or zero condition.

The circuit operates as follows. As power is turned on, the base of transistor B12 takes a negative value, and transistors B12 and B13 are off. Three divider networks begin to sample the voltage levels being supplied: zener

diode B5 and resistor A11 sample the +5 volt input; zener diode A7 and resistor A9 sample the +15 volt input; and zener diode B7 and resistor B6 sample the −15 volt input. As these voltages approach their appropriate values, diodes A12, A8, B8, and B9 (operating as an AND gate) are reverse-biased. The base of transistor B12 becomes slightly positive, and transistors B12 and B13 turn on. Up to this time, transistor B16 had been on. When transistors B12 and B13 turn on, transistor B16 turns off, capacitor A22 begins to charge through resistor A24, and transistor B22 is biased off. The time constant of the resistor/capacitor circuit is about 68 ms. With transistor B22 off, transistors A30, B23, C36, and C34 are all biased on, and their outputs are all clamped low. This condition disables the printer functions as outlined above.

At the end of the 68 ms delay, when all supply voltages have risen to their proper levels, transistor B22 is biased on, turning transistors A30, B23, C36, and C34 off, allowing their outputs to all go high. This removes the circuit disable clamps, starts the LOGIC-2 program counter, and initiates a Restore sequence.

Any subsequent interruption in, or decrease of, any of the three input voltage levels sampled will disable the input AND circuit leading to discharge of capacitor A22. This clamps the output low again to disable the printer. Complete restoration of power recycles this circuit, putting the printer in a proper condition to resume operation.

2.7.3 Paper Feed Drive Circuit

The Paper Feed Drive circuit consists of two identical channels A and B. Figure 2-26 shows typical input and output waveforms for each channel for a clockwise rotation of the drive motor (upward paper movement).

The A and B inputs (see Figure 2-26), 90° out of phase, are presented to type 747 operational amplifiers F18-10/-12, where they are squared and amplified. The output of these amplifiers is coupled to current amplifiers D15/18-C12/20 for channel A, and D22/24-E12/21 channel B, where the drive for the paper feed step motor (waveforms A' and B') is developed.

The information in Figure 2-27 further illustrates the development of step motor rotation from the two out-of-phase inputs.

2.8 PRINTWHEEL POWER AMPLIFIER BOARD, PART NO. 40530-XX

This assembly includes the Printwheel Servo Power Amplifier, the Ribbon Lift and Ribbon Feed Drivers, the End-of-Ribbon sensor amplifier, and the Hammer Energy Control and Driver circuits. It is located in Printer board slot H, and has a finned heat sink attached to it, to help cool the several drive transistors.

NOTE

DO NOT stand the HyType II Printer on its rear heat sink panels. The finned heat sinks are mounted on plug-in circuit boards which can be easily damaged by this practice.

2.8.1 Printwheel Power Amplifier Circuit

NOTE

This circuit is nearly identical to the Carriage Power Amplifier circuit described in Section 2.7.1.

This circuit supplies and controls current flow to the printwheel servo drive motor. It is designed as an "H" bridge, allowing all current to flow through the motor from supply to supply instead of through circuit ground, to avoid circuit noise problems. Figure 2-23 illustrates the basic circuit in simplified form, where certain transistors in the actual circuit are represented as switches. Closing switches S1 and S4 will cause current to flow through the motor and resistor R right to left, while closing switches S2 and S3 will cause current to flow left to right.

Referring to the schematic diagram and Section 2.7.2 will aid in understanding the operation of the circuit itself. Since the amplifier is composed of several similar circuits, only one path will be discussed.

Assume a PW SERVO ERROR signal input of +5 volts for a commanded motor current of 1 ampere. The output of operational amplifier A31-6 will be low, and this will place a low potential on the base of transistor H18 and on the emitter of transistor H35. H35 will turn off. H35 being off turns transistor F32 off, which turns transistor E30 on to turn on PULSE REV transistor G26.

The error signal is also supplied to amplifier A19-7. The output of amplifier A19-7 will be zero volts with a positive input, which will turn transistor C4 off. This will turn transistor D5 off and transistor E6 on to turn on DRIVE REV transistor C10.
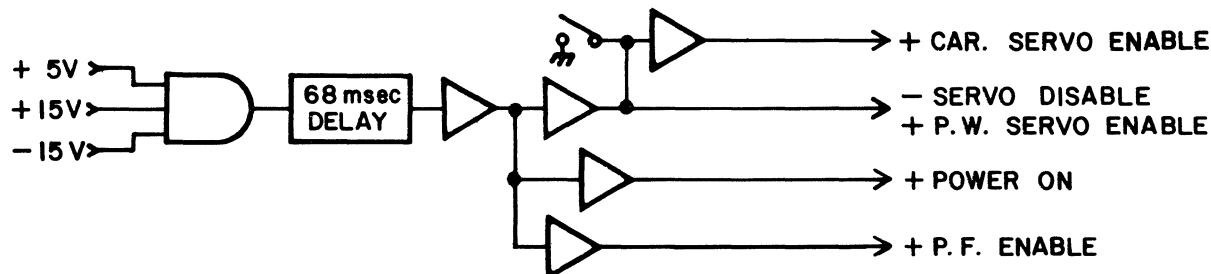
Figure 2-25. Block Diagram, Power Monitor Circuit

Figure 2-26. Paper Feed Drive Circuit
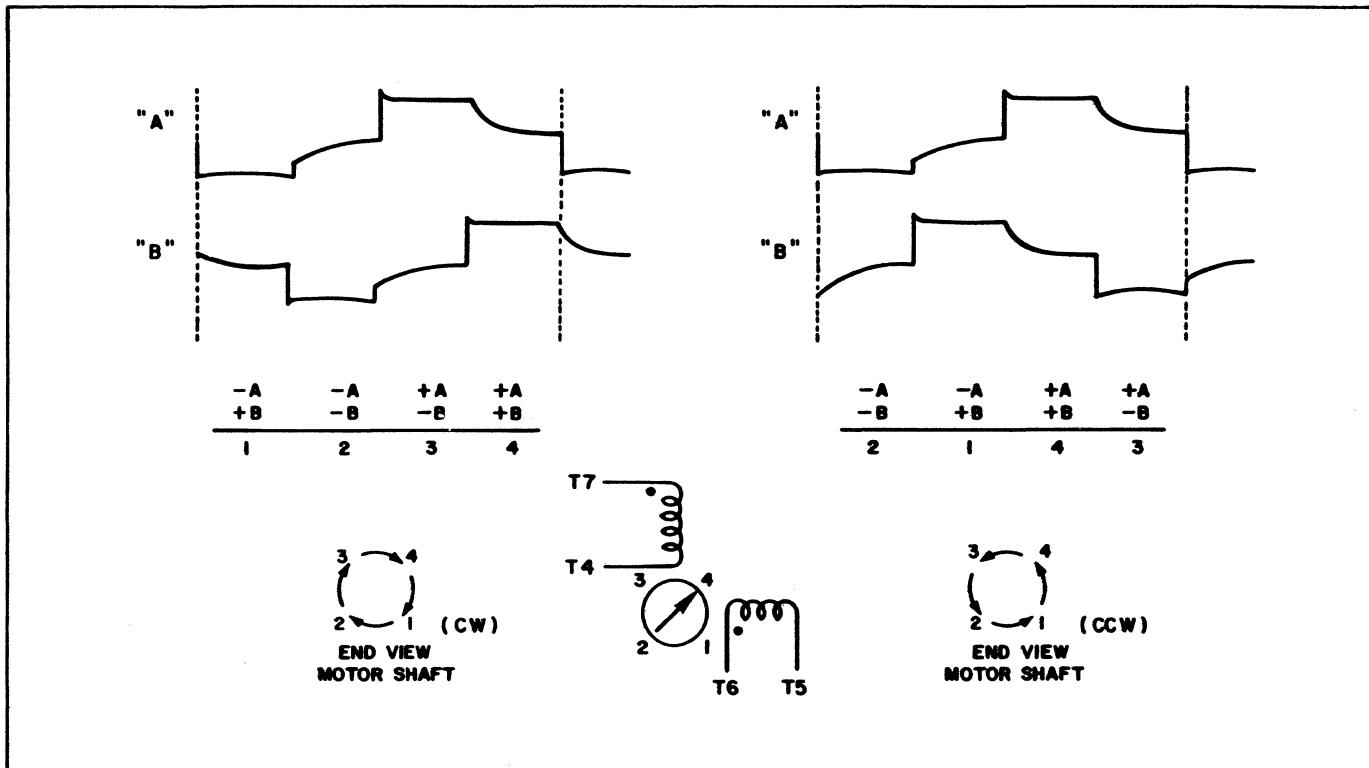
Figure 2-27. Step Motor Rotation
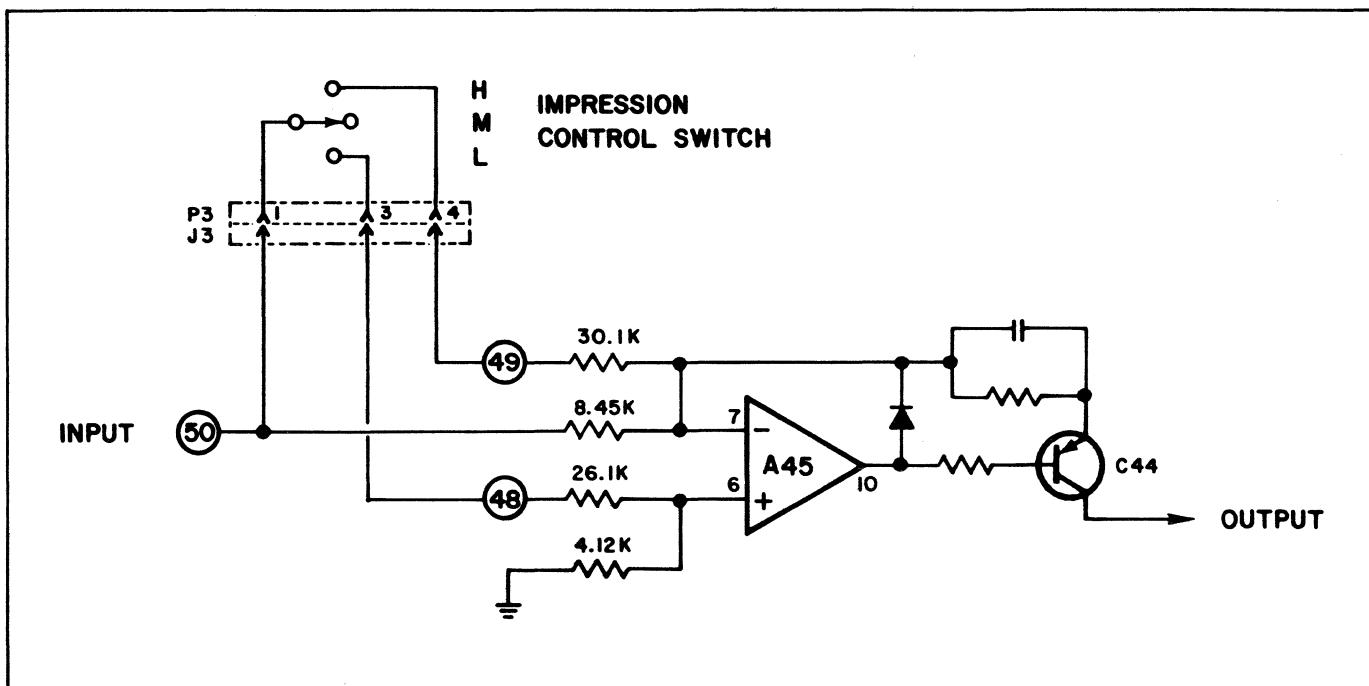
Figure 2-28. Hammer Energy Control Circuit

Referring back to Figure 2-23, transistor C10 is shown as switch S1, while transistor G26 is shown as switch S4. Turning these two transistors on establishes a current path from the −15 volt supply through G26, resistor G23, the drive motor, and C10 to the +15 volt supply.

Figure 2-24 is a simplified schematic diagram of the feedback circuit. This circuit includes a 1.0 Ohm resistor G23 located in one of the lines to the servo motor, across which is connected a precision balanced 10K Ohm resistor network and difference amplifier A45-12. The value of resistor G23 is such that its voltage drop to current ratio is two-to-one (2-volt drop equals 1 ampere of motor current). Difference amplifier A45-12 inverts this voltage and presents the result to the servo error input terminal 2 of amplifier A31-6. The two signals are summed at a ratio of 10 input to 1.6 feedback, so that as motor current approaches the command level, the output of A31-6 will diminish. When motor current matches command current, the PULSE REV transistor G26 will be turned off. This removes motor current, which removes feedback voltage, and G26 is turned back on again. The circuit will oscillate in this manner to maintain motor current at the commanded level.

Should the Power Monitor circuit detect an input voltage error, it will drive the +PW SERVO ENABLE signal low. This will turn transistor E35 on, turning off PULSE FWD and PULSE REV transistors G10 and G26 to disable printwheel servo movement.

2.8.2 Ribbon Lift Driver Circuit

This circuit consists of two subcircuits; one for ribbon lift and one for ribbon hold. The ribbon lift portion includes transistors G67 and H59. The −RIBBON LIFT signal turns G67 on to apply a ground potential to the base of H59. H59 turns on, applying −15 volts to one side of the ribbon lift coil. The opposite side of the coil is connected to +15 volts. The coil is then energized with a potential of 30 volts, to provide maximum power to rapidly lift the ribbon. At the end of the ribbon lift sequence, the printer microprocessor removes the −RIBBON LIFT signal and replaces it with the −RIBBON HOLD signal. The ribbon hold portion of the circuit includes transistors H67 and H61. The −RIBBON HOLD signal turns on transistor H67 applying a ground potential to the base of H61. H61 turns on, applying a ground potential to one side of the ribbon lift coil. The coil is then maintained in its energized state (ribbon lifted) with a potential of 15 volts.

2.8.3 Ribbon Feed Drive Circuit

NOTE

This circuit is nearly identical to the Paper Feed Drive circuit described in Section 2.7.3.

Refer to Figures 2-26 and 2-27. The Ribbon Feed Drive circuit consists of two identical channels, A and B. Figure 2-26 shows typical input and output waveforms for each channel.

The A and B inputs, 90° out of phase, are presented to type 747 operational amplifiers E74-12/-10 where they are squared and amplified. The output of these amplifiers is coupled to current amplifiers of F48/D50-D43/F45 for channel A, and F64/D64-D58/E58 for channel B, where the drive for the ribbon feed step motor is developed.

The information in Figure 2-27 further illustrates the development of the step motor rotation from the two out-of-phase inputs. It should be noted, however, that unlike the paper feed operation, ribbon feed is in one direction only.

2.8.4 Hammer Energy Control and Drive Circuit

Figure 2-28 is a simplified schematic diagram of the Hammer Energy Control circuit. The HAMMER ENERGY CONTROL signal from the D-A Converter on the SERVO board is the input to this circuit. This is a signal whose instantaneous level depends on the character to be printed. The normal range of this signal is 0 to +10 volts.

The input is applied to board pin 50 and to the wiper arm of the operator's Impression Control Switch. The output of the amplifier A45-10 is then dependent on the position of this switch, i.e., whether a portion of the Impression Control Switch input is added to or subtracted from the Hammer Energy Control input.

The −HAMMER FIRE pulse from the printer microprocessor turns transistor H50 on, to drive the hammer enabling circuits. The hammer-fire pulse from H50 is compared with the hammer energy level in comparator A64-7, and also enables transistor C65. The output of C65 switches driver transistor C73, and also establishes its output level to control the amount of current flowing to the hammer coil.

2.9 XMEM (EXTRA MEMORY) BOARD, Part no. 23926-XX

When the 4K bytes of ROM, 1K of EROM, and 512 bytes of RAM on the HPRO board are adequate for the programming application, the XMEM board is not supplied. When additional memory is required, the XMEM board is installed in slot F, directly behind the HPRO board; no connections other than plugging into the mother board are required. The XMEM board can contain up to 1.5K bytes of RAM, 4K of ROM, 8K of EROM, or a combination of memory types.

2.9.1 Applications

During program development, programs are stored on EROMs so they can be debugged, erased, and rewritten. When the program has been tested and validated, it is burned into masked ROMs, which are installed on the HPRO board.

EROMs on the XMEM board are used to store development programs. Because of the time involved in manufacturing masked ROMs, early production terminals are often shipped with programs on EROMs on the XMEM board instead of on masked ROMs on the HPRO board. Also, when a program is larger than 4K bytes, additional memory chips, either ROMs or EROMs, are installed on the XMEM board to store part of the program. ROMs and EROMs on the XMEM board are addressed in the same manner as ROMs and EROMs located on the HPRO board. For applications requiring more than 512 bytes of working read/write memory, up to 1.5K bytes of RAM can be installed on the XMEM board.

2.9.2 Basic XMEM Board

The basic XMEM board (Dwg. No. 23926-XX) contains an address buffer, address decoders, and voltage regulators. IC memory chips of the required type and number are added to suit a specific application.

2.9.3 XMEM Configurations

The XMEM can have the following numbers of memory chips installed:

    12 Type 2111A-4, 256 x 4-bit RAMs
     2 Type 8316A, 2K x 8-bit masked ROMs
     8 Type 8708, 1K x 8-bit EROMs

While it is possible to have all these memories installed (physically) on the same XMEM board, it is logically impractical, because both ROMs and EROMs use the same addresses, and two EROMs must be eliminated for each ROM installed. there is no address interference between RAMs and ROMs or EROMs, so a full complement of RAMs can be installed regardless of the number of ROMs and/or EROMs installed.

2.9.4 Addressing

Figure 2-6 shows the memory addressing scheme used by the MPU to access the entire memory, both on the HPRO board and on the XMEM board. Note that HPRO ROMs #1 and #2, and XMEM ROMs #3 and #4 use the same address areas as the EROMs on the XMEM board, so the EROMs can not be used when the masked ROMs are installed. This is done intentionally, so that a program can be written electrically into EROMs, tested and corrected as often as necessary, and when approved, the program can be used to generate masked ROMs without need for address modification. When masked ROMs are in production, the EROMs can be eliminated, and, if the program is less than 4K, the two ROMs containing the program can be installed on the HPRO board. If there is no need for the additional RAM storage, the XMEM board can be eliminated. If the program is larger than 4K, two additional ROMs can be installed on the XMEM board, along with as many RAMs as are required.

ROMs and EROMs can be mixed, as long as there is no direct address conflict. For example, it would be possible to use EROMs 5, 6, 7, and 8 with HPRO ROMs 1 and 2, but these EROMs could not be used with XMEM ROMs 3 and 4. Since RAMs use an entirely different address area, their use is independent of ROM/EROM configuration.

2.9.5 Additional Applications

- EROMs can be used in terminals produced in quantities too small to justify the expense of preparing masked ROMs.

- A mixture of ROMs and EROMs can be used in applications requiring special programs.

- RAMs can provide additional working memory.

2.10   KEYBOARD (UP/DOWN STROKE), Schematic No. 400094-01

2.10.1   Keyswitch

The keyswitch used on the keyboard is a linear saturable ferrite core with two preformed wires snapped through it. One wire, called the drive wire, is periodically driven by a current pulse. The response to the drive pulse appears, through transformer action, on the second wire called the sense wire. This core module assembly is snapped into the switch housing together with the plunger and return spring. Into the plunger are molded a pair of magnets. In the undepressed position the magnets are saturating the core. Since the core is saturation, signals which are present on the drive wire are not coupled to the sense wire. As the plunger is depressed, the magnets clear the core, bringing it out of saturation and allowing the drive signals to be coupled to the sense wire. These sense signals are translated into digital pulses.

2.10.2   Circuit Description

2.10.2.1   Microprocessor

The 128 key non-programmed MOS/LSI microprocessor integrated circuit with external electronics is used for sequential interrogation. This microprocessor can be logically divided into the following sections:

        a)   timing section

        b)   count register section

        c)   data section

        d)   strobe section

2.10.2.1.1   Timing section. The timing section generates a main clock signal train which drives the scanning counter and generates clock phases $\emptyset 1$, $\emptyset 2$, & $\emptyset 3$, ($\emptyset 2$ is used internally only). The scanning counter provides the address for each key and its position code. The position code is the address of the keyswitch latched into the output data latch. $\emptyset 1$ is used as the interrogation enable signal. $\emptyset 2$ generates the strobe and loads the data into the data latch. The strobe is updated one time per depression of a keyswitch. Phase $\emptyset 3$ is used in the external electronics. The input to the timing section (TPC) is a pulse train of 10 µs square waves.

2.10.2.1.2   Count Register Section. The count register section consists of one binary counter seven bits in length. The first four bits are used to scan in the "X" direction and the last three bits are used to scan in the "Y" direction. This counter provides 128 unique position codes, each of which corresponds to a unique location of the key in the matrix.

2.10.2.1.3   Data Section. The output data consists of a seven bit data latch and a shift register. Each of the seven bits of the counter is latched into the data latch with $\emptyset 2$, if the key is depressed, and with the signal $\emptyset 1 \cdot \overline{CLK}$ if the key is released. A 128 bit shift register is used to provide past key history to the data latch, to the strobe section, and to the external amplifier for hysteresis.

2.10.2.1.4   Strobe Section. All keys that are detected will enter into the N-key rollover scheme. During $\emptyset 2$, the input shift register is "anded" with the inverted output of the shift register to detect a down stroke of the keyswitch which is presently being interrogated, and the strobe is generated.

2.10.3   External Electronics

2.10.3.1   Keyswitch Array

Each keyswitch is assigned to a particular location in the matrix (see organization chart, dwg. no. 400094-01, sht. 2.) The first four lines (A1 - A4) of the microprocessor are gated with $\emptyset 1$ to scan in the "X" direction and the last three lines (A5 - A7) are used to scan in the "Y" direction. If the keyswitch is depressed, a signal appears on the sense line, which is amplified and latched into the keyswitch latch. The detected signal in the keyswitch latch is called "Shift Register In" (SRIN) and represents a depressed keyswitch in the matrix location.

2.10.3.2   Output Code

The microprocessor will generate a binary code to identify the key station location in the given matrix when the key is depressed, and a modified key code when the key is released. This modified key code consists of regeneration of bits D0 through D6, and the inversion of bit D7. The diagnostic positions generate down stroke codes only.

There are two diagnostic positions installed on the keyboard. All keyboard memories are erased when -POR is low. When -POR goes high, the diagnostic codes and the codes of any depressed keys will appear at the interface. The sequence in which these codes appear depends upon the location of the key in the matrix, and on the time of removal of -POR.

2.10.3.3   Output Strobe Logic

A strobe signal -KYSTB is generated each time a key is depressed or released. (This signal is generated by the microprocessor, gated with $\emptyset 1$.) The +BUSY signal goes high after the terminal microprocessor receives the strobe signal. The strobe will go high after +BUSY returns low. As long as -KYSTB and +BUSY are both high, the scan cycle stops, and any new key depressions will be ignored.

PRIMARY REFERENCED TO COMMON RETURN ◇ | OUTPUT CIRCUIT REFERENCED TO SIGNAL GROUND ⏚

AC

INPUT CURRENT LIMITING

RFI FILTER

FULL-WAVE RECTIFIER

F1

POWER SWITCH

REVERSE BIAS →

LOCAL +15V SUPPLY

LC FILTER

SWITCHING REGULATOR AMPLIFIER

+ FEEDBACK

SPIKE CATCHER

+15V RECTIFIER & FILTER

+15VOLT OUTPUT

− FEEDBACK →

INVERTER DRIVE

INVERTER SWITCH TRANS-FORMER

+5V RECTIFIER & FILTER

+5VOLT OUTPUT

OVERVOLTAGE PROTECTION

INVERTER CURRENT LIMITING

−15V RECTIFIER & FILTER

−15VOLT OUTPUT

OUTPUT CURRENT LIMITING

OPTO-ISOLATOR

+5V ERROR AMPLIFIER

Figure 2-29.   Block Diagram, Power Supply

2.11 POWER SUPPLY, Part No. 26021-XX

The regulated power supply is provided in either of two input voltages, 115 or 220 volts. Variation of input voltage can be $\pm$15% for either supply. Line frequency can be 47 to 63 Hz. An AC line fuse is located inside the desk at the bottom, and is accessible by removing the desk front panel. The POWER switch is at the right side of the keyboard.

+5V @ 4A (8A surge)

+15V @ 4A (10A surge)

-15V @ 4A (10A surge)

Foldback current limiting is provided on all ouput voltages (11A$\pm$2A for 5V, 13A$\pm$2A for 15V) as well as on the inverter primary. Overvoltage protection takes over when the +5 volt output reaches approximately 5.6 volts. The primary circuit, which may generate switching transients, is electrically isolated from the secondary (output) circuit.

The power supply operates on the principle of switching regulation, using a power transistor as a pulse-width-modulated switch controlled by a negative feedback loop from the output circuit. AC line voltage is rectified, chopped, smoothed, inverted at 20 kHz, then finally rectified for output to the terminal circuits. Operation at this frequency, rather than at 60 Hz, permits the use of much smaller, lighter transformers and inductors that dissipate far less heat.

2.11.1 General Description

Refer to the block diagram, Figure 2-29 and the schematic diagram, Drawing No. 26021-xx in the Schematics/Reference Section of this manual. A thermistor in the power supply input line limits power-up inrush of current to charge a large capacitor in the rectifier circuit. An input radio frequency interference (RFI) filter prevents switching transients generated by the power supply from being reflected back onto the AC line. A full-wave bridge rectifier produces approximately 100 volts DC. A portion of the rectifier output is tapped off through a resistance network to supply a local 15 volt regulated power supply that furnishes power to the primary circuit. An internal fuse at the output of the rectifier protects it from catastrophic failure of circuit elements in the primary. Raw DC from the rectifier is applied to a power transistor driven at 20 kHz by a switching regulator amplifier. Chopped DC from the power switch is smoothed in an L/C filter network. A positive feedback loop from the filter to the switch driver maintains self-oscillation. Voltage regulation is imposed by a negative feedback loop from the output circuit. The duty cycle of the power switch is varied in response to the feedback signal, providing more "on" time to increase the average voltage from the L/C filter, less "on" time to decrease the average voltage. Current limiting signals from both the primary circuit and the output circuit are fed back through this same loop.

A "spike catcher" between the L/C filter and the inverter switch suppresses large transients that may be generated if conduction of the two transistors in the inverter switch overlaps. The inverter switch is two power transistors that are driven at 20 kHz, conducting alternately. The output of the inverter switch is fed to the transformer. Current is fed to each half of the transformer primary alternately in opposite directions. The inverter operates on a 50% duty cycle, producing square waves.

Each output voltage has its own full-wave rectifier and filter circuit. A coil in the toroidal transformer of each output is used to sense current in the circuit. This inductive coupling to the output current limiting circuit serves to isolate the output voltages from the primary side of the power supply, while establishing a feedback loop to the switching regulator amplifier. If current in any output tends to rise excessively, the negative feedback signal causes the switching regulator to decrease the "on" time of the power switch, reducing the average voltage applied to the inverter switch, which results in a reduction of the current through the transformer. The +5 volt output is compared to a reference voltage, and the difference is amplified and applied to the switching regulator amplifier via an opto-isolator, which isolates the output circuit from the primary circuit. The error signal is used to modify the duty cycle of the switch regulator in much the same way as in the current limiting circuit. Coupling between windings in the inverter transformer makes it possible to regulate all outputs by monitoring any one.

Overvoltage protection is provided by a silicon controlled rectifier connected across the +15 volt output. Under normal operating conditions, the SCR presents a very high resistance, but if the regulating circuit fails and a preselected limit is exceeded (nominally 5.6 volts on the +5 volt output), the SCR is fired, placing a short across the +15 volt output. This effectively shorts the entire transformer secondary. Current limiting then takes over automatically to protect the power supply.

2.11.2 Isolation

The primary circuits of the power supply are electrically isolated from the secondary, or output circuits. Note from the schematic diagram that there is no common ground reference between the primary and secondary circuits. While outputs are returned to the normal signal ground, primary circuits are returned to a "common return", NOT GROUND, indicated by a diamond on the schematic ($\diamond$). The only interfaces between the primary and secondary circuits are the inverter transformer (inductive), the output current limiter (inductive), and the optoisolator (optical).

WARNING

Hazardous voltages are present in the primary circuit.

CAUTION

When troubleshooting the primary side of the power supply under power, do not use test instruments having a third-wire ground, or damage to the instrument will result. Make measurements between circuit elements and the primary circuit common return, NOT ground.

2.11.3 Theory of Operation

The following paragraphs present a more detailed description of the operation of the power supply. Refer to the schematic diagram, No. 26021-xx, in the Schematics/Reference Section.

2.11.3.1 Input Current Limiting

When AC power is initially applied, electrolytic filter capacitor C23 demands a high rate of charging current. To protect the diodes in the rectifier, thermistor RT1 is inserted in the line. This thermistor has a negative coefficient of temperature, initially offering a relatively high resistance, then lowering resistance when current passing through it raises the temperature. The initial high resistance limits the charging rate of C23 to a safe level. When the temperature of RT1 rises, the resistance drops to a very low value. The AC ripple component from the rectifier is sufficient to keep the thermistor above the ambient temperature and at a low resistance.

2.11.3.2 Input RFI Filter

Switching power supplies tend to generate sharp transients, which can be reflected onto the power line. The purpose of the RFI filter is to suppress these switching transients. Inductor L1, the RFI filter has two windings with a common magnetic core. The two windings develop a higher Q and provide better filtering of both sides of the power line than two single inductors.

2.11.3.3 Full-Wave Bridge Rectifier

The full-wave rectifier, consisting of diodes CR1 through CR4 connected in a bridge configuration, converts the off-the-line AC directly into DC. Capacitor C23 provides filtering and storage of the rectified voltage. The cathode of C23 defines the primary circuit common return. Note that the rectifier is returned to the primary circuit common return, NOT to signal ground. Fuse F1, at the output of the rectifier, protects the diodes in the event of a catastrophic failure in the primary circuit. The output of the rectifier is then applied to the power switch, Q1, and to the local +15 volt power supply via a resistor-network.

2.11.3.4 Local +15 Volt Power Supply

Transistors Q5 and Q6 are the basic components of the local +15 volt regulated power supply that powers the switching regulator amplifier IC, U1. Zener diode VR1 and resistors R12, R13, and R14 provide a reference voltage that is compared by Q5 to the sampled voltage. The error signal developed is used to control Q6, the series-pass element, producing the required regulation.

2.11.3.5 Power Switch and Switching Regulator Amplifier

Power transistor Q1, the power switch, is controlled by Type 723 switching regulator amplifier U1, an integrated circuit voltage regulator, through a chain of power-boosting transistors. The switching signal generated within the IC at approximately 20 kHz turns the power switch on and off. Regulation is effected by modifying the duty cycle of the switch in response to feedback signals from the +5 volt output. Low output voltage results in increasing "on" time; high output causes a reduction in "on" time. Modifying the duty cycle raises or lowers the average voltage delivered to the inverter.

The output of U1 is boosted by transistor Q7 to drive complementary Darlington stage Q3. Q3, a PNP transistor, in turn drives Darlington-connected Q2, the immediate driver stage of Q1, the power switch. The 20 kHz chopped DC output from the power switch is applied to an LC filter for smoothing. The switch output signal is fed back to pin 4 of U1 via inductor L2 and resistors R27 and R17 to maintain self-oscillation. To overcome the effect of charge storage,

reverse emitter-base bias is injected into the power switch from a secondary
winding on inductor L2. The reverse bias signal is applied via a network of
resistors R2, R3, and R5, capacitor C5, and diode CR5. The phasing of the
secondary of L2 causes a pulse of turn-off bias to be applied to both Q1 and
Q2 at the termination of the switch "on" period. Turnoff of the switch be-
comes regenerative, and is greatly accelerated.

2.11.3.6 LC Smoothing Filter

The regulated, pulsed DC is applied to a filter network made up of inductor L2
and capacitor C10. Diode CR6 maintains output current flow during switch
"off" periods by providing a current path to discharge the energy stored in
the magnetic field of the inductor during "on" periods. CR6 is reverse-biased
when the power switch is "on" to prevent upsetting DC conditions. The smoothed,
regulated DC output of the filter is applied to the inverter via a "spike
catcher" network.

2.11.3.7 Spike Catcher

The purpose of the spike catcher network, inductor L3, diode CR10, resistors
R29 and R48, and capacitor C11, is to suppress large current spikes that can
be generated when conduction of the two inverter transistors overlaps. This
is not a common occurrence, but can happen during start-up or during recovery
from an overload condition. This suppression not only reduces RFI radiation,
but also protects the inverter transistors and the power switch transistor.
Diode CR10 is polarized to damp production of counter emf's in L3 should
transients occur in the inverter.

2.11.3.8 Inverter

The smoothed DC input is chopped at 20 kHz by the two power transistors, Q10
and Q11, which conduct alternately, feeding current to the two halves of the
non-saturating output transformer T1 in opposite directions. Supporting
circuitry consists of a saturating transformer, T2, diodes CR11 through CR15,
resistors R29 through R32, and capacitor C12. The transformer is a self-
excited type.

2.11.3.9 DC output Circuits

Each output has its own full-wave center-tap rectifier and low-pass LC filter.
In addition, there are two electrolytic filter capacitors across the entire
output from +15 volts to -15 volts. There is a bleeder resistor across the
entire outpout, and one across the +5 volt supply to discharge the capacitors
when power is turned off. The filters remove the high-frequency ripple compo-
nent, mostly 40 kHz, from the output voltages.

The rectifier for the +15 volt supply is made up of transformer T6, diodes
CR17 and CR22, and capacitors C35 and C38. Inductor L4 and capacitor C18
provide filtering. The -15 volt supply uses transformer T5, diodes CR18 and
CR21, and capacitors C36 and C37. Filtering is provided by inductor L6 and
capacitor C20. The +5 volt filter is a pi type consisting of inductor L5 and
capacitors C39 and C43. The +5 volt filter is a pi type consisting of induc-
tor L5 and capacitors C19 and C25. R54 is the +5 volt bleeder resistor.
Filter capacitors C32 and C33, and bleeder resistor R51 are connected between
the +15 and -15 volt outputs.

2.11.3.10 +5 Volt Error Amplifier

The +5 volt output is sampled by a voltage divider, resistors R43 and R44, and applied to the non-inverting input of Type 723 voltage regulator IC U2 via resistor R41. The adjustable reference voltage is derived from potentiometer R40 and applied to the inverting input of the voltage regulator via resistors R39 and R38. The two voltages are compared within U2, and the difference is applied to the Opto-isolator, U3. Only the +5 volt output is adjustable and regulated. The close electro-magnetic coupling in the transformer secondary makes it possible to control all output voltages by controlling any one.

2.11.3.11 Opto-isolator

The Opto-isolator, U3, consists of a solid-state lamp and a phototransistor. The output of the error amplifier is applied to the lamp, illuminating it in proportion to the error. The optical energy is read by the phototransistor, which has no electrical connection to its base. The output of the phototransistor is fed back through resistor R33 to the switching regulator amplifier, U1, where the signal is used to modify the duty cycle of the power switch, regulating the voltage. Since there is no direct electrical connection through the Opto-isolator, and the phototransistor output is returned to the primary circuit common return, the output circuit is effectively isolated from the primary.

2.11.3.12 Output Current Limiting Sense Amplifier

Current in a winding of a toroidal transformer in each output is monitored and fed back to the switching regulator amplifier to modify the switch duty cycle. Resistor R58 is connected across a winding of transformer T4 in the +5 volt circuit. Current through the transformer develops a voltage drop across the resistor. Transistors Q14 and Q15 sense and amplify the voltage drop. In the -15 volt supply, Resistor R59 is across the winding of T5, and transistors Q16 and Q17 are the sense amplifiers. In the +15 volt output, the circuit elements are transformer T6, resistor R60, and transistors Q18 and Q19. The collectors of all the transistors are connected to the base of transistor Q13 through resistor R70. Q13 amplifies the error signal, which can originate in any of the outputs, and applies it to the switching regulator amplifier along with the voltage regulation feedback signal. As current increases, the duty cycle of the switch regulator, and of the power switch, is modified to reduce switch "on" time, reducing the average voltage applied to the inverter, limiting current through the inverter transformer. A shorted output will reduce current to a very low level that can be tolerated indefinitely.

2.11.3.13 Overvoltage Protection

Overvoltage protection is provided primarily to protect the loads in the event of failure of the regulating circuit. Silicon controlled rectifier SCR1 is connected across the +15 volt output. The gate circuit of SCR1 monitors the +5 volt output through zener diode VR2, which has a 5.6 volt breakdown rating. If the +5 volt supply exceeds the zener breakdown voltage, the diode conducts, firing SCR2, which places a direct short across the +15 volt output. In effect, this "crowbars" all outputs because of the close coupling of the inverter transformer secondary. To protect the power supply, the current limiting circuit takes over, reducing the power switch output to a safe level. Once fired, the SCR will continue conducting until power is turned off. When the condition causing the overvolt condition is corrected and power is applied, the overvolt protect circuit is automatically restored to normal.

3.1   INTRODUCTION

Maintenance of the HyTerm is generally divided into two broad categories: module replacement and adjustments, and detailed troubleshooting and repair of circuit boards. Since some troubleshooting is also involved in locating the faulty module before it can be replaced, there is no clear-cut dividing line between these categories, and overlap will occur in many areas.

This section is generally divided so that those performing module replacement will use the next three sub-headings, (3.2) PREVENTIVE MAINTENANCE, (3.3) MODULE REPLACEMENT, and (3.4) ADJUSTMENTS. The remainder of this section contains component location/identification information that will be useful in troubleshooting.

NOTE

Preventive Maintenance, when performed according to the procedures listed here, will not affect the Diablo warranty. However, any module replacement or adjustment unsuccessfully attempted will render the warranty null and void. All time and material required to restore the HyTerm to working order will be billed at the prevailing rates.

3.1.1   General Rules

There are a few general rules that should always be observed:

(1)   Never remove or install any circuit boards, or connect or disconnect any plugs, while power is on.

(2)   Applying power to the HyTerm initiates a printer Restore sequence, which includes carriage movement. Make sure the carriage is free to move to the left before applying power.

(3)   Whenever the access cover is removed, be careful not to brush against the cover-open switch: operating this switch could allow the carriage to move suddenly, which could cause an injury. When operating the HyTerm with the access cover removed (and the cover-open switch in the "override" position), keep fingers, hair, etc., away from the printer.

(4)   Never remove the top cover without first disconnecting the power cord from the wall outlet.

(5)   When tipping the HyTerm up to gain access to its underside, first position the power cord and the EIA cable to the sides so they will not be in the way. Make sure the surface behind the HyTerm is flat and free of any foreign objects. Then tip the HyTerm up approximately 70 degrees so that it balances on the rear edge of its bottom cover. Do not allow the table surface or any objects to apply pressure to the finned heat sinks on the rear; since these heat sinks are mounted on the power amplifier boards, any pressure could damage the circuit boards or the mother board and its connectors. Also, while the HyTerm is tilted up in this manner, hold onto it with one hand to prevent it from failing.

(6)   Do not use alcohol to clean the platen, the paper feed rollers, or any other rubber parts. Alcohol dries out the rubber and hardens it, eventually resulting in paper feed problems. Use "Fedron Platen Cleaner" or its equivalent.

CAUTION

Fedron Platen Cleaner and similar products are flammable, and have a very low flash point.

(7)   Take care not to touch plastic parts with platen cleaner. These products are usually harmful to plastics. Use alcohol to clean plastic parts.

3.1.2   Top Cover Removal

Removal of the top cover is a prerequisite to most HyTerm maintenance procedures. Proceed as follows:

(1)   Unplug the power cord from the wall.

(2)   Raise or remove the access cover. Remove the plastic skirts over the ends of the platen shaft.

(3)   Remove the platen: grasp the platen knobs in both hands, press down the platen latches with your thumbs, and lift the platen straight up.

(4)   Release the top cover by pulling forward on the two latches inside the cover at the sides, just in front of the platen. Lift the cover straight up.

3.1.3 Tools

A basic hand tool assortment, including regular and Phillips screwdrivers, small open-end wrenches, pliers, and Allen set-screw wrenches is needed for any maintenance. Tools such as screw starters, offset screwdrivers, etc., are not essential, but will make some jobs much easier. In addition, the following tools are needed for driving and removing the special screws used in the HyTerm and for performing printer adjustments.

	Description	Diablo Part No.
(1)	T15 TORX® Screwdriver	70826-03
(2)	T9 TORX Screwdriver	70826-04
(3)	T15 TORX Key Wrench	70826-05
(4)	T9 TORX Key Wrench	70826-06
(5)	Circuit Board Extender	40539-03
(6)	Combination Adjustment Tool	40795
(7)	Tensiometer, Electromatic Equipment Co. Model DXX-IKD or equivalent, calibrated for Diablo cable.	N/A

For detailed troubleshooting and repair of circuit boards, the usual oscilloscope, soldering iron, etc., are needed, plus the following special tools:

	Description	Diablo Part No.
(1)	Transducer Cable Extender	40666
(2)	Carriage Motor Cable Extender	40667

3.2 PREVENTIVE MAINTENANCE

3.2.1 Supplies

The following lubricants and supplies are necessary for proper preventive maintenance (numbers are Diablo part numbers):

(1) Fedron Platen Cleaner, or equivalent.

(2) #70655 light oil, Shell Turbo 27, or equiv. (2 drops/appl.)

(3) #70654 Polyoil (light white grease)

(4) #70825 Grease

(5) #99000-01 Alcohol Pads (91% Isopropyl alcohol) or equiv.

(6) Lint free wipers

TORX® is a registered trademark of Camcar Screw & Mfg.

(7) #70870-01 Permabond 240™ adhesive, 1 oz. (printwheel home sensor tab only)

#70847-01 Vibratite™ adhesive, 8cc (all locations required other than printwheel home sensor tab)

CAUTION

1. *Do not use alcohol on rubber items.*
2. *Do not use platen cleaners on plastic items.*
3. *Platen cleaners are flammable, and have a very low flash point.*

3.2.2 Cleaning and Inspection

It is difficult to state specific rules concerning the frequency of preventive maintenance inspections, because of differences in the hours of usage and other environmental considerations from one machine to another. It is recommended, therefore, that the following preventive maintenance procedure be performed at least every 500 hours of printing time, or every six months, whichever occurs first:

(1) Remove power from the terminal. Raise the access cover and remove the top cover as noted in Section 3.1.2.

(2) Inspect the printer for signs of wear and loose or broken hardware. Check carriage cable for signs of wear, and cable pulleys for loose bearings. Check platen for looseness or wobble. Check platen drive gears for looseness. Check the carriage for looseness, wobble, or accumulations of foreign material on the rails which might cause uneven movement of the carriage.

(3) Remove the platen, paper cradle, ribbon cartridge, and printwheel. Inspect for signs of wear.

(4) Clean the printer thoroughly, using alcohol saturated cleaning pads, and wipers. Remove accumulations of paper residue, ink, dust, etc., with special attention to the carriage rails and pulley grooves.

(5) Clean the platen, paper bail tires, and paper feed rollers with a good platen cleaner which is non-injurious to rubber products, such as "Fedron" Platen Cleaner. Do not use alcohol.

*(6) Clean the rest of the HyTerm as required — remove all dust and foreign material.

*(7) Inspect the entire machine for loose hardware and frayed wires or cables.

*(8) Check to be certain that the fan is operating.

(9) Check all power supply voltages (see 3.4.3).

Items above marked with an asterisk (*) should be checked on every machine visit, not only at the P.M. inspection.

3.2.3 Lubrication

Lubricate the various parts of the cleaned and inspected printer according to the following schedule. DO NOT exceed this schedule. Too much lubricant is often worse than none at all!

(To be done every six months or if printer has not been used for more than a week.)

3.2.3.1 CARRIER SYSTEM (Figure 3-1)

(1) Paper Feed Roller Shaft Pins (A) — Lightly grease the 8 pressure roller shaft pins with No. 70825 grease.

(2) Platen Position Lever Detent Plate (B) — Lightly grease the inside of this plate with No. 70825 grease.

(3) Platen Position Slide Plates (Carrier Frame) (C) Lightly grease exposed slide surfaces (lever moved limit to limit), and all points of contact with pivots, eccentrics, guides, etc., with No. 70825 grease.

(4) Platen Position Torque Shaft Ends, Bearing Surfaces, and Spring Loops (D) — Lightly grease these points with No. 70825 grease.

(5) Paper Release Lever Tab Ramp and Shaft Pivots (E) — Lightly grease these points with No. 70825 grease.

(6) Paper Release Torque Shaft Pivots and Arm Slots (F) — Lightly grease these points with No. 70825 grease.

(7) Paper Bail Pivots (G) — Lightly grease these two points with No. 70825 grease.

3.2.3.2 CARRIAGE SYSTEM (Figure 3-2)

(1) Carriage Rails (A) — Clean these items only with alcohol wipers.

(2) Carriage Rail Bearings (B) — Put 4 or 5 drops of #70655 oil on each side of carriage rails and move carriage back and forth slowly by hand, allowing oil to saturate the felts.
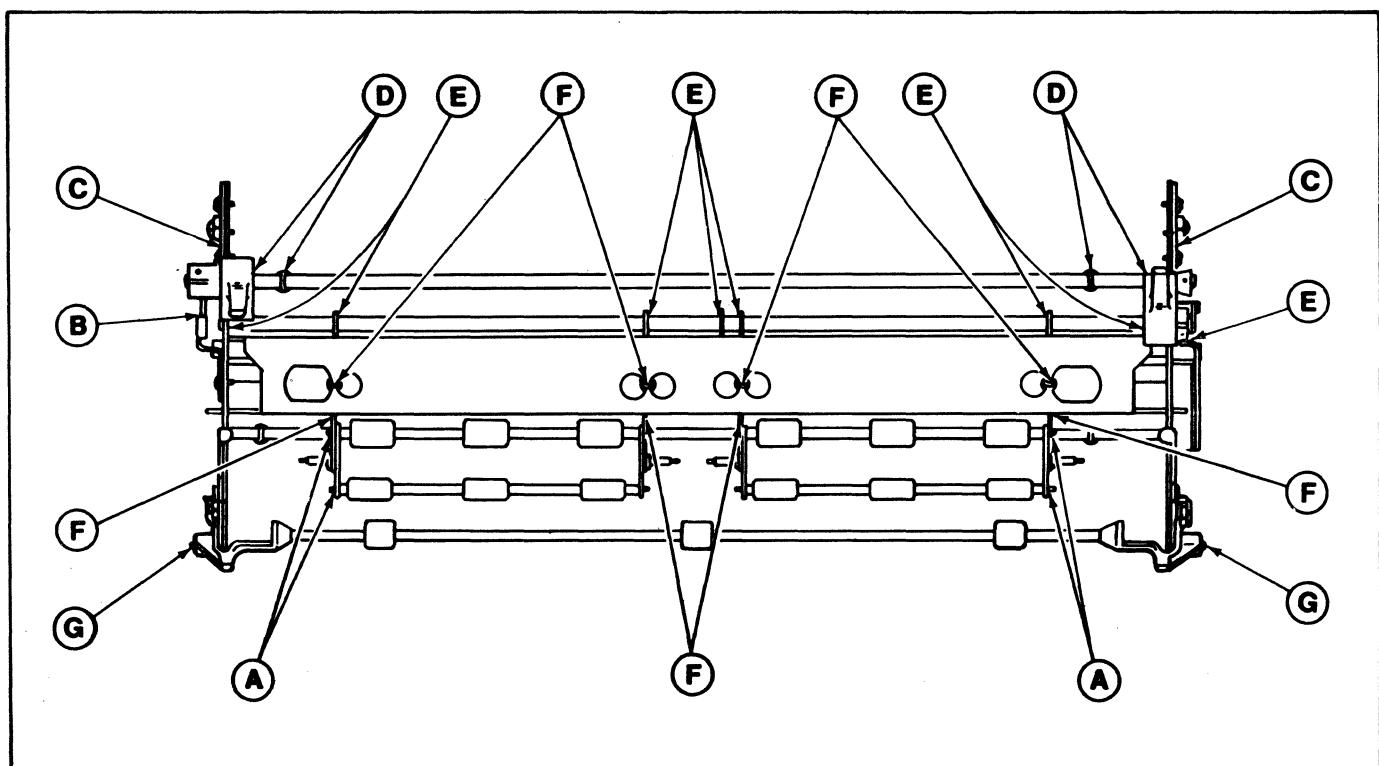
Figure 3-1. Carrier System Lubrication Points
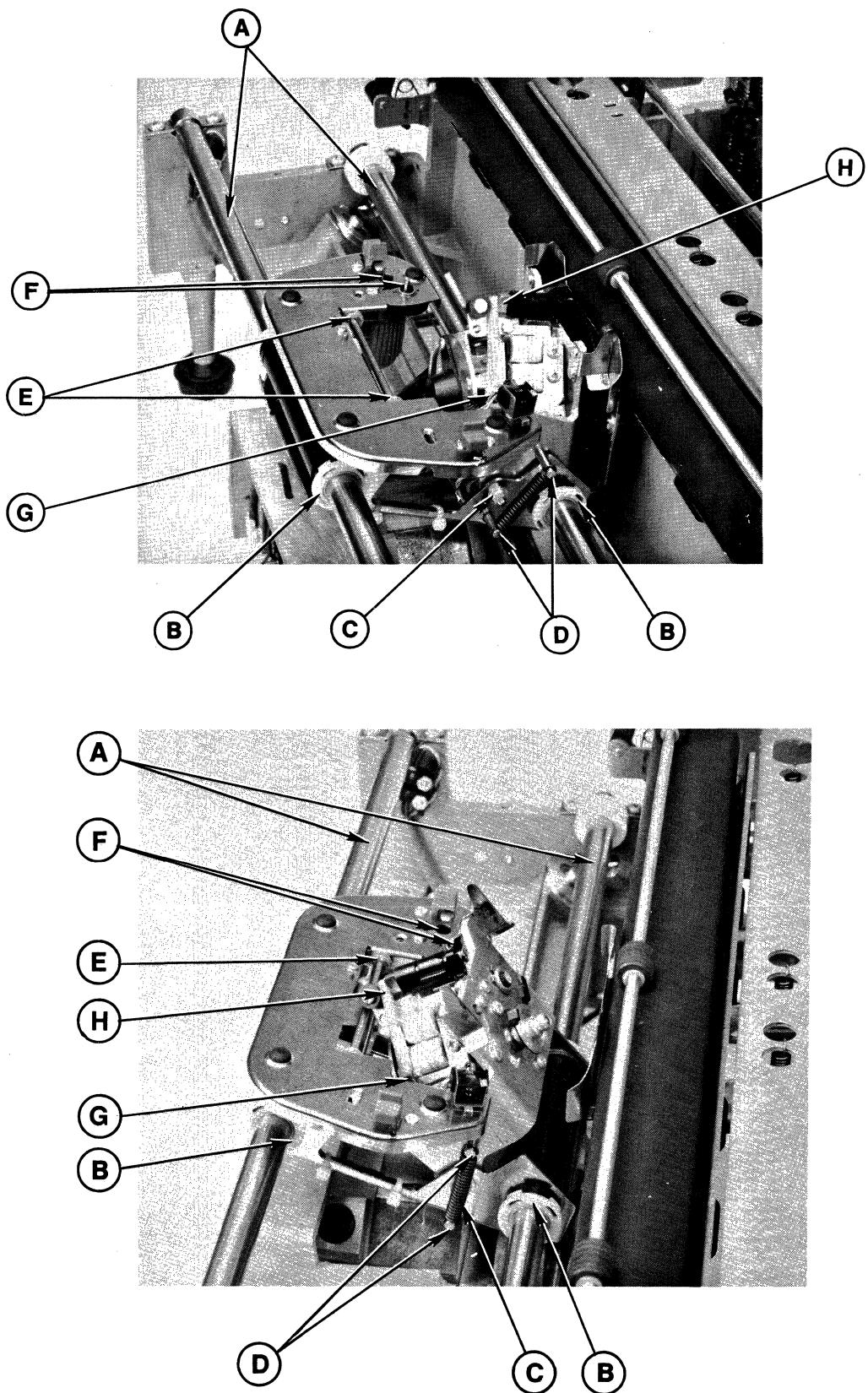
Figure 3-2. Carriage System Lubrication Points

(3)   Carriage Pivots (C) — Apply one drop of No.70655 oil to the pivot on each side of the carriage frame.

(4)   Carriage Pivot Spring Loops (D) — Lightly grease the end loops and posts of the pivot spring on each side of the carriage frame with No. 70825 grease.

(5)   Ribbon Base Plate Pivots (E) — Saturate the felt washer on each end of the base plate pivot shaft with No.70655 oil.

(6)   Ribbon Drive System (F) — Apply one drop of No. 70655 oil to the drive and idler gear shafts, and to the drive key slot.

(7)   Hammer Armature Pivots (G) — Remove the two rubber cups, and fill the grease chambers with No. 70654 Polyoil grease. Replace the rubber cups.

(8)   Print Hammer (H) — DO NOT lubricate this item. If cloth ribbon is used, insure that hammer is clean.

3.2.3.3   PLATEN SYSTEM (Figure 3-3)

(1)   Paper Feed Idler Gear (A) — Inspect the large felt washer behind this gear. If it is becoming white in color, saturate with No. 70654 Polyoil.

(2)   Platen Latches (B) — Lightly grease the contact area between these arms and the carrier side frames.

(3)   Platen Hubs (C) — Apply one drop of No. 70655 oil to the bore of the hub at each end of the platen.
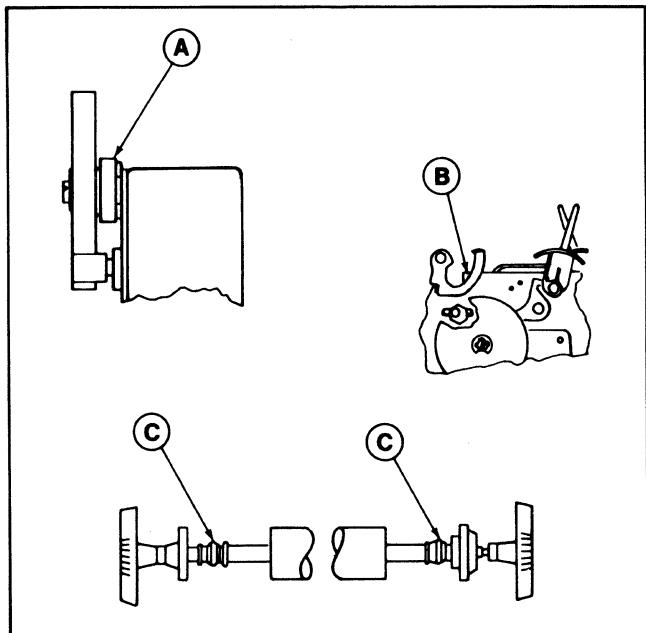
Figure 3-3. Platen System Lubrication Points

3.2.4   Covers and Switches

Reassemble the HyTerm and note the following items:

(1)   Replace printer top cover. Check for proper keyboard and control panel alignment. If any keys or switches rub against the cover, reposition the keyboard, control panel, and/or cover.

(2)   Check for proper operation of the paper-out switch.

(3)   Check for proper operation of the cover-open switch. If the access cover fits too loosely, adjust and/or form its clamping springs.

(4)   Replace all covers and test. Operate all keys and switches in Local mode and verify proper HyTerm operation. If facilities are available, establish a remote data link and test transmit/receive capabilities.

3.3   MODULE REPLACEMENT

Always make sure power is off before attempting to replace any components or modules.

All modules have been assigned "assembly numbers" according to the system adopted by the American National Standards Institute (ANSI) in their standard no. Y32.16, "Reference Designations for Electrical and Electronics Parts and Equipments". Table 3-1 lists all major assemblies, and the smaller assemblies that are normally considered replaceable as modules, along with their reference designations. These designators are used in the remainder of this section and in the schematics and wiring diagrams, to identify the various assemblies.

Table 3-1.   Major Assemblies and Modules

Assembly No. (Reference Designator)	Description
A1	HyType II printer
A1A1	8080 INTERFACE board
A1A2	LOGIC-2 board
A1A3	SERVO board
A1A4	CAR PWR AMP board
A1A5	HPRO3 board
A1A6	XMEM1 board
A1A7	XDCR board
A1A8	P/W PWR AMP board
A2	Power Supply
A3	Keyboard
A4	Control Panel

3.3.1 Circuit Boards

CAUTION

Never remove or insert circuit boards or
plugs with the power on.

REMOVAL

(1) Turn off power to the HyTerm.

(2) Remove paper or forms from the printer. Remove tractor feed if so equipped. Raise or remove the printer access cover. Remove the platen (refer to Section 2.4.3 of the Product Description manual if necessary).

(3) Remove the top cover (3.1.2).

(4) Using a Phillips screwdriver, loosen the single screw in the center of the circuit board clamp (Figure 3-4) and remove the clamp.

(5) Locate the board to be removed. See Figure 3-4.

(6) Grasp the board firmly at the two upper corners and pull it straight up.

(7) Disconnect any remaining cables from the board.

PWR AMP (H)
XDCR (G)
XMEM (F)
HPRO3 (E)
(D) CAR PWR AMP
(C) SERVO
(B) LOGIC – 2
CIRCUIT BOARD CLAMP SCREW
(A) 8080 INTERFACE
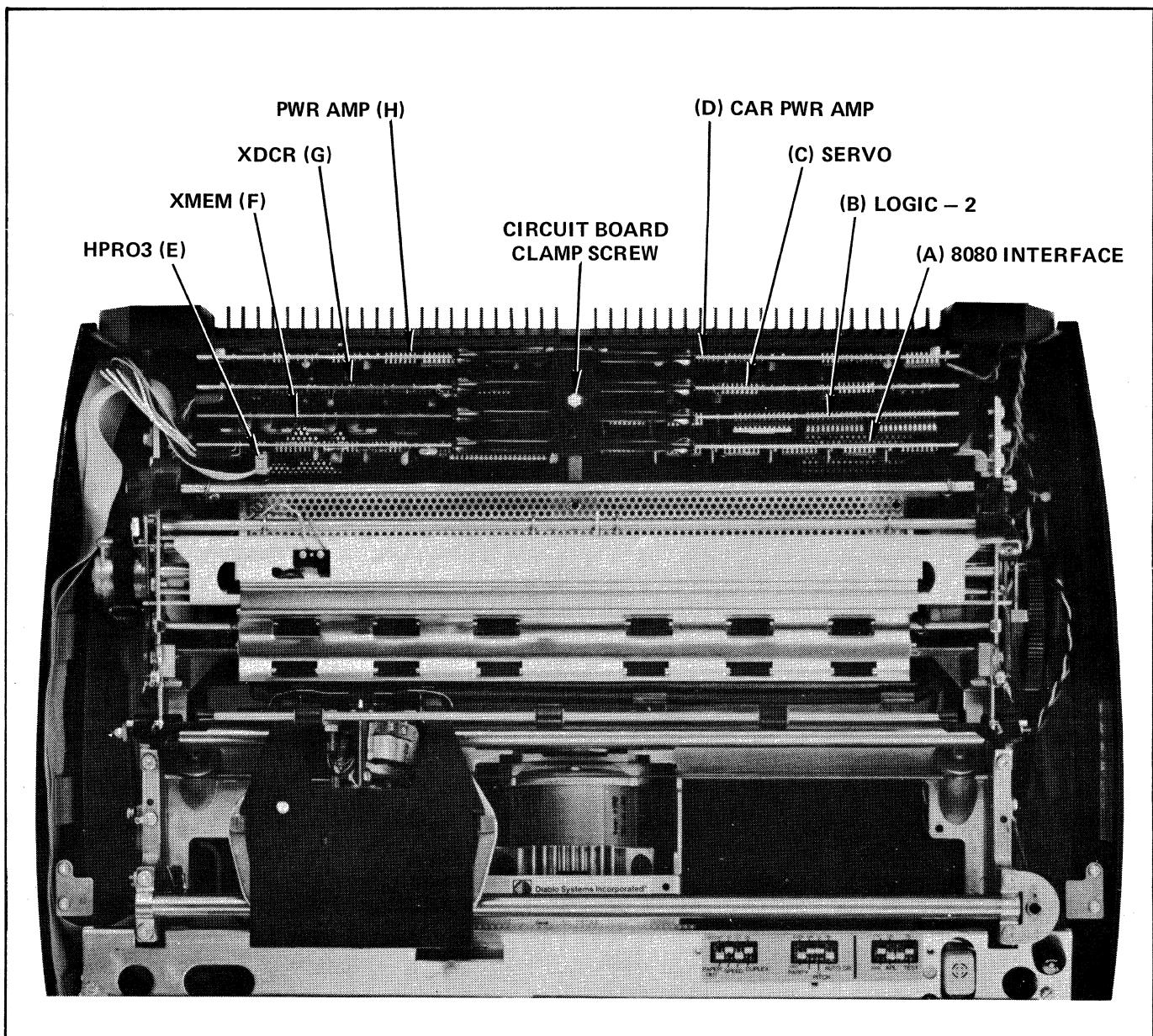
Figure 3-4. Circuit Board Location

INSTALLATION

(1) If the HPRO board is being installed, first attach the keyboard cable to the P2 connector on the circuit board.

(2) Holding the board with the components toward the front of the machine (toward the platen), insert the board into the guides and slide it all the way in.

(3) Using firm, equal pressure on both upper corners of the board, push it in so that it is fully seated into the socket. If excessive resistance is encountered, check first to make sure the proper board is being installed in the socket: all boards are keyed so they will not fit in the wrong socket. Refer to Figure 3-4.

(4) Reconnect any remaining cables. Make sure the lower plug (J8B) on the XDCR board and the control panel plug (J2) on the HPRO3 board are not turned over; it is possible to install these plugs upside down.

(5) Replace the platen, insert a sheet of paper, and test the HyTerm briefly.

(6) After determining that the HyTerm is operating properly, remove the platen, replace the circuit board clamp, the top cover, and the platen, and test again.

3.3.2 Power Supply

REMOVAL

(1) Make sure the HyTerm is disconnected from its power source.

(2) Move the HyTerm to a location where both the top and bottom will be accessible when the machine is tilted up.

(3) Remove the access cover, the platen skirts, the platen, the paper cradle (located directly underneath the platen) and the printer top cover (see 3.1.2).

(4) Remove the 4 screws holding the power supply assembly to its aluminum cover screen and the printer frame. This will allow the power supply to drop slightly, but it will still be held in place by its bottom cover.

(5) Tilt the HyTerm up so it is resting on the rear edge of the bottom cover.

CAUTION

When tipping the HyTerm up, be certain to use a flat surface, with no foreign objects in the way. Any small objects could cause pressure to be applied to the rear heat sinks, which are mounted on the power amplifier boards. Excess pressure on these boards could damage the boards and/or the mother board.

CAUTION

Whenever the HyTerm is tilted up in this manner, hold on to it with one hand to prevent it from falling over.

Remove the screen-like bottom pan from the HyTerm by loosening the rear three screws, removing the remaining five screws, and lifting the bottom pan off the machine.

(7) Swing the power supply out to access the terminal strip. Disconnect the wires. Set the power supply assembly safely aside and tilt the HyTerm down onto its feet.

INSTALLATION

(1) Tilt the HyTerm up and connect the wires to the new supply as per Figure 3-5. Observe the cautions about tilting the HyTerm noted in step (5) of the removal procedure.

(2) Swing the power supply into position inside the printer casting. Make sure all wires and cables are positioned securely.

(3) Holding the power supply in position, insert the mounting screws through the top cover screen and the printer casting and start them into the threads in the power supply frame. Start all 4 mounting screws.

(4) Tilt the HyTerm down onto its feet. Tighten all 4 power supply mounting screws securely.
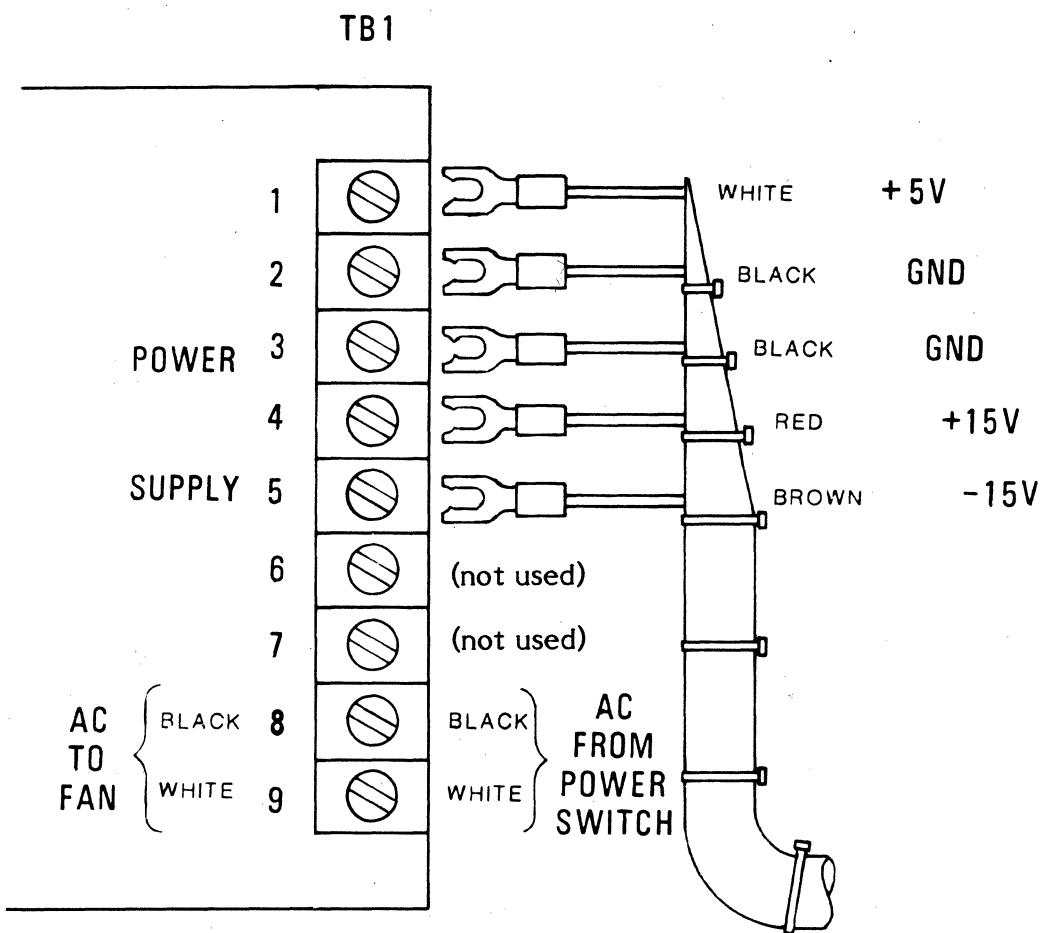
Figure 3-5. Power Supply Connections

(5) Remove the XMEM board from slot (F), if installed, and install a circuit board extender into slot (F) behind the HPRO board.

(6) Plug the HyTerm into the wall outlet.

WARNING

When the HyTerm is connected to a power source, line voltage is present at the POWER switch terminals. To avoid a dangerous shock when power is applied and the top cover is not in place, keep your fingers away from the POWER switch terminals.

Turn on power and verify that a printer restore operation occurs. Use a digital voltmeter, if available, to measure the voltage between pins 1-4 and the following locations on the circuit board extender:

Pins 5-6	+5.0V ± .1V
Pins 41-42	+15.25V ± .75V
Pins 49-50	+15.25V ± .75V
Pins 23-24	-15.25V ± .75V
Pins 31-32	-15.25V ± .75V

WARNING

While power is on, do not tip the HyTerm up except to make a power supply adjustment. If this is necessary, be extremely careful not to touch any part of the power supply, because extremely high voltages (200-300 volts) are present. Use only non-metallic tools.

If the +5 volt measurement is outside its tolerance, adjust the +5 volt supply using the procedure outlined in Section 3.4.3. If any 15 volt measurement is still outside its tolerance after the +5V supply has been adjusted properly, the source of the problem must be located; either the power supply is defective, or some printer malfunction is causing an unusual current drain. A current foldback condition in any supply will affect the other outputs as well.

(7) Test the HyTerm briefly to verify proper operation. Issue a few carriage movement and paper movement commands and observe the operation. Unplug the power cord from its outlet.

(8) Tilt the HyTerm back up. Install the fiber bottom cover.

(9) Replace the screen-like bottom pan: slide in under the rear screws first, then install the remaining five screws.

(10) Tilt the HyTerm down onto its feet. Remove the circuit board extender and reinstall the XMEM board, if used. Install the top cover, the paper cradle, the platen, the platen skirts, and the access cover. Insert paper, apply power, and test thoroughly.

3.3.3 Control Panel

REMOVAL

(1) Unplug the HyTerm from its power source.

(2) Remove the access cover, the platen skirts, the platen, and the top cover.

(3) Remove the keyboard mask: pull up on front of mask until it pops free; then lift mask from machine.

(4) Remove the four control panel mounting screws. Flip the control panel over and disconnect the edge connector (P1) and the ac lines at the POWER switch and at the fuse.

(5) Lift the control panel off the machine.

INSTALLATION

(1) Connect all the ac lines to the POWER switch and to the fuse. Connect the edge connector (P1) to the keyboard.

(2) Install the four control panel mounting screws and tighten them down.

(3) Replace the keyboard mask: push down on front of the mask until it snaps into place.

(4) Replace the top cover, the platen, the platen skirts, and the access cover.

(5) Apply power and test for proper operation.

3.3.4 Keyboard

REMOVAL

(1) Unplug the HyTerm power cord from the ac outlet.

(2) Remove the access cover, the platen skirts, the platen and the top cover.

(3) Remove the keyboard mask: lift up on the front of the mask until it pops loose; then lift entire mask off keyboard.

(4) Disconnect the keyboard edge connector visible through an access hole in the left side of the control panel.

(5) Remove the four keyboard mounting screws from the keyboard mounting brackets.

(6) Lift out the keyboard and set it aside where it will not be subject to damage.

INSTALLATION

(1) Position the new keyboard in place on the mounting brackets. Start all four mounting screws. Position the keyboard in its approximate final position and tighten one screw on each end.

(2) Attach the keyboard cable plug to the keyboard.

```
WARNING

When the HyTerm is connected to a
power source, line voltage is present at
the POWER switch terminals. To avoid a
dangerous shock when power is applied
and the top cover is removed, keep
fingers away from the POWER switch
terminals.
```

(3) Replace the keyboard mask: set the mask in place and push down on the front of the mask until it snaps into position.

(4) Apply power and test the keyboard in the following manner: temporarily install the platen and a sheet of paper, then pull the cover-open switch to its override position (all the way up), depress the RESET key, and key characters from the keyboard. If keyboard operates properly, remove power and the platen from the HyTerm.

(5) Carefully install the top cover in place, while checking for proper clearance between the keytops and the cutout in the keyboard mask.

(6) Replace the platen and the platen skirts. Plug in the power cord, turn on power and test the HyTerm again.

3.3.4.1 Keyswitch Replacement

Once the keyboard has been removed, individual keyswitches can be replaced, using a soldering iron and long needle-nose pliers.

CAUTION

When removing the press-to-latch modules, be certain that the key is in its released or up position to avoid damaging the module.

(1) Remove the keytop from the module being replaced, by lifting or prying upward with a padded tool. Remove the keytops from the modules on either side of the one to be replaced. It may be necessary to remove other adjacent keytops to provide adequate work space.

(2) Unsolder the four module terminals from the circuit board. Use a solder removal tool to remove all solder from the pin holes in the circuit board.

(3),(4) Using the needle-nose pliers, gently squeeze the retaining spring tabs on the module and pull it straight out.

(5) Install the replacement module. Before snapping it into place, make sure it is oriented properly and that all four pins are through the circuit board.

(6) Solder the new switch terminals, using 60/40 rosin core solder and a 750°F soldering iron with a 1/8″ chisel tip.

CAUTION

Never hold the soldering iron to the module pins for more than four seconds.

(7) The solder joints may be cleaned (on the bottom of the circuit board) with mild solvent. Be careful not to get any solvent on the switch modules or keytops.

(8) Replace all keytops. Make sure they are replaced on the right key and that the legends are properly oriented.

3.4 ADJUSTMENTS

Any necessary tests and/or adjustments should be performed in the sequence outlined in this section, because some adjustments affect others. No adjustments should be attempted unless a malfunction indicates a specific need.

3.4.1 Printer

Several printer adjustments can be made using the Combination Adjustment Tool, Diablo part no. 40795.

NOTE

In the following procedures you are often told to tilt the carriage forward or rearward: forward means toward the keyboard, the operator, the front of the terminal; rearward means toward the platen. The carriage will detent in either position. To move it forward, first remove the ribbon cartridge. Then simply grasp it by the "ears" near the ribbon guides and pull it away from the platen. To move it rearward, simply push it back up toward the platen.

3.4.1.1 PRINT QUALITY TEST

The print quality test can provide an indication as to possible needed adjustments. Proceed as follows:

(1) Print a full line of capital letter "H"s.

(2) Refer to Figure 3-6 and compare the test results with the illustration.
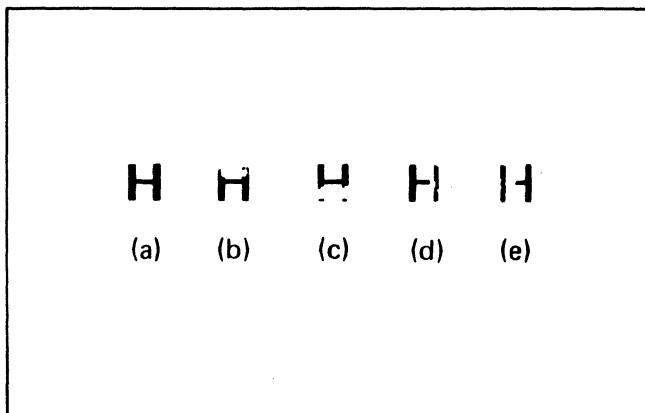
Figure 3-6. Print Quality Standards

(a) Impressions similar to this with uniform density and good edge definition indicate proper adjustment of the printer. A gradual change in density (lighter or darker) from one end of the line to the other indicates a Platen-to-Printwheel adjustment may be required.

(b) Impressions similar to this indicate Platen Height adjustment may be required for platen too low.

(c) Impressions similar to this indicate Platen Height adjustment may be required for platen too high.

(d,e) Impressions similar to this indicate that a Printwheel-to-Hammer adjustment may be required.

3.4.1.2 PAPER CARRIER SYSTEM

3.4.1.2.1 Carrier Assembly.

(1) Carrier Assembly Bias Shaft, Figure 3-7, item (A). Check for axial movement = .001 in. ± .0005 in. (.03 mm ± .01 mm). Adjust the collar at (A) as required to achieve this dimension.

(2) Platen Position Torque Shaft, Figure 3-7, item (B). Check that the setscrews in the eccentric collars (C), at each end of this shaft are aligned vertically with each other when the platen position lever is full forward, and that the shaft end play = .002 in. + .001 in. (.05 mm + .03 mm). Adjust the collars for the proper clearance. Note, however, that failure of the collars to align vertically indicates a twisted shaft, which will affect several platen adjustments.

(3) Platen Position Lever, Figure 3-7, item (D). Move the lever back and forth. A positive detenting force must be felt for all positions. Adjust the detent plate (E), as necessary to achieve an even detenting action. The carrier assembly must move equally at both ends in increments of .005 in. ± .002 in. (.13 mm ± .05 mm) between detent positions.
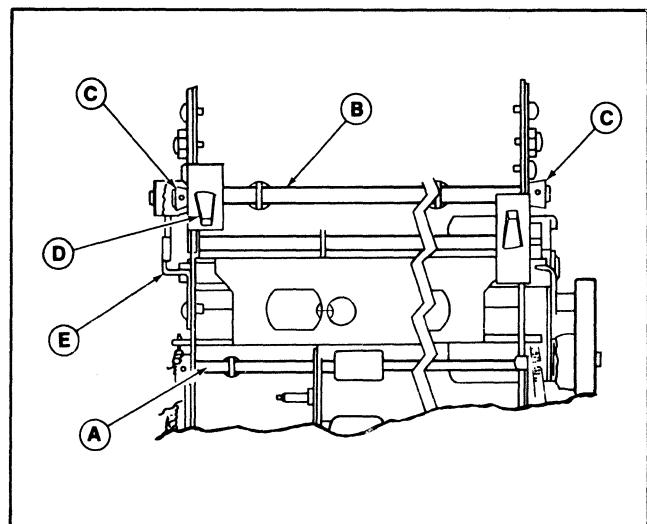
Figure 3-7. Carrier Assembly Adjustment

3.4.1.2.2 Paper Feed Rollers. Refer to Figure 3-8. With the paper release lever (A) fully forward, the paper feed rollers (G) must clear the platen (E) by a minimum gap of .080 in. (2 mm). To achieve this, and other goals, adjust the paper feed system as follows:

(1) Insert 4 sheets of standard form paper (.012 in. or .3 mm) and move the paper release lever fully rearward.

(2) Ensure that the torque shaft arm tabs (B) are touching the lower edge of the feed roller support arm slots (C).

(3) Ensure that the paper release actuator (D) is touching the ramp on the paper release lever. Loosen the actuator's setscrew and adjust the actuator to achieve this condition, then retighten the setscrew.

(4) Remove the 4 sheets of paper, and insert one strip of paper 1 in. wide (or a .004 in. shim) between the front paper feed rollers and the platen. Check that both platen and rollers rotate when the strip (or shim) is pulled free. Repeat for all rollers front and rear. If no rotation occurs, the torque shaft arm tabs (B) have been pushed down too low.

3.4.1.2.3 Paper Feed (Platen) Drive. Refer to Figure 3-9. With paper feed motor drive gear (A) locked, platen drive gear (B) must have a .0005 in. to .002 in. (.013 mm to .05 mm) play (total play includes idler gear (C)).

(1) Loosen the paper feed motor mounting screws (D).

(2) Rotate eccentric (E) counterclockwise ONLY (clockwise will not allow the platen to be installed properly), until a minimum backlash is obtained with no binding effect when rotating idler (C) a full 360°.

(3) Install the platen. Rotate the paper feed motor clockwise about mounting screw (D1) to remove backlash between platen gear (B) and idler gear (C). Tighten all screws.

3.4.1.2.4 Platen Knob End Play. Refer to Figure 3-10. End play should be .002 in. (.05 mm) maximum, as shown. Adjust for proper clearance by loosening the setscrews in the platen release gear hub (A) and moving the hub. Retighten the setscrews.

Figure 3-8. Paper Feed Adjustments
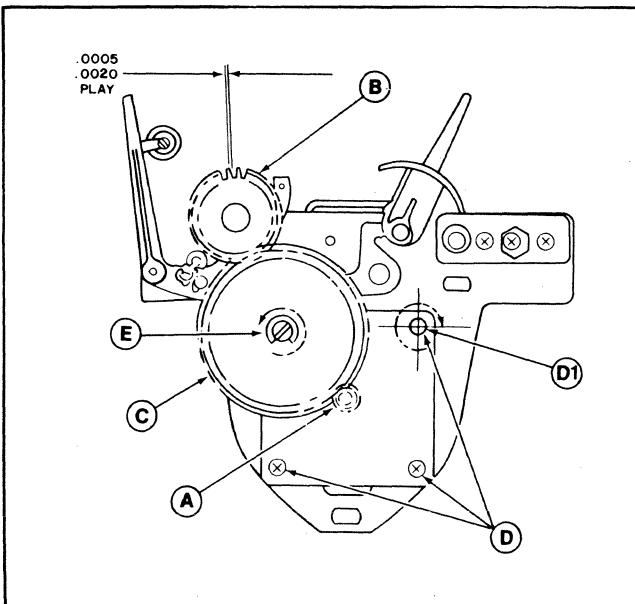
Figure 3-9. Paper Feed (Platen) Drive Adjustments
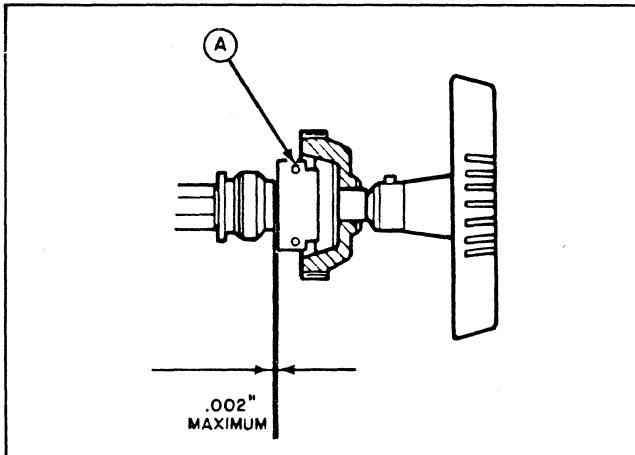
Figure 3-10. Platen Knob End Play Adjustment

3.4.1.3 CARRIAGE DRIVE CABLE (Figure 3-11)

(1) With the carriage positioned against the left hand mechanical stop, check the cable tension midway along the exposed cable for a force of 16.5 ± 3.3 lbs. (7.5 ± 1.5kg) necessary to distort the cable as shown.

NOTE

If the Tensiometer, listed in Section 3.1.3, is not used, the dimensions between force points must be carefully followed.

(2) Adjust cable tension by tightening or loosening cable tension nut (B).

CAUTION

The square shank on the end of the cable (A), must not rotate while adjusting nut (B).

After adjusting the nut (B), move the carriage back and forth several times to redistribute cable tension, and recheck.

3.4.1.4 PRINT QUALITY ADJUSTMENTS

Either of two alignment tools, 40795 or 40795-01, may be used in making these adjustments. In most cases, the procedures are the same with either tool, but in some cases two separate procedures are listed. The following adjustments are included in this group:

(1) Platen-to-Printwheel Position
(2) Printwheel-to-Hammer
(3) Card Guide Position
(4) Ribbon Height
(5) Carriage Home

Figure 3-12 identifies the several alignment/adjustment features of the alignment tools by a number-letter designator. These designations are used in the procedures that follow.

3.4.1.4.1 Conditions of Test and Alignment.

(1) Power

Power is to be applied to the HyTerm while making these adjustments. It is used to electrically detent the printwheel and carriage servo motors, and for cycling the printer through a Restore sequence when required.

(2) Platen

Platen Carrier adjustments are to be made with a platen installed whose surface is in good condition and free from wear or defects.

(3) Controls

The Platen Position (manifold) lever is to be brought fully forward for these tests and adjustments.

(4) Precautions

Always remove the alignment tool from the printwheel motor shaft before initiating a Restore sequence, to prevent damage to the printer. Also always ensure that the tool is properly seated prior to making any measurement. When it is necessary to move the carriage with the alignment tool installed, first tilt the carriage forward, away from the platen. This will avoid possible damage to the platen.

3.4.1.4.2 Printwheel-to-Hammer. Refer to Figure 3-13. Proceed as follows:

(1) Preparation

(a) Apply power to the printer, and verify completion of a Restore sequence.
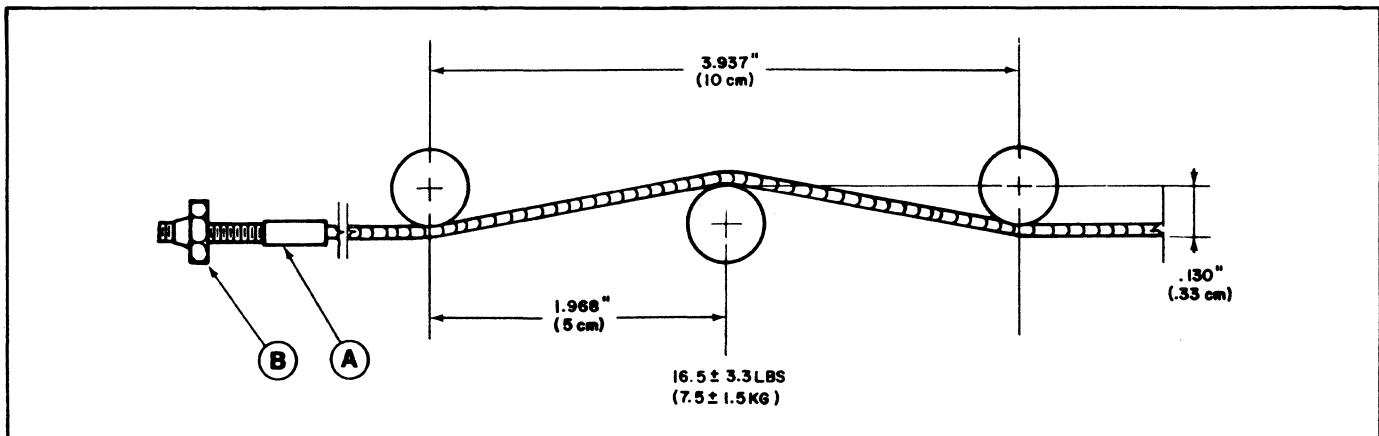
Figure 3-11. Carriage Drive Cable Adjustment
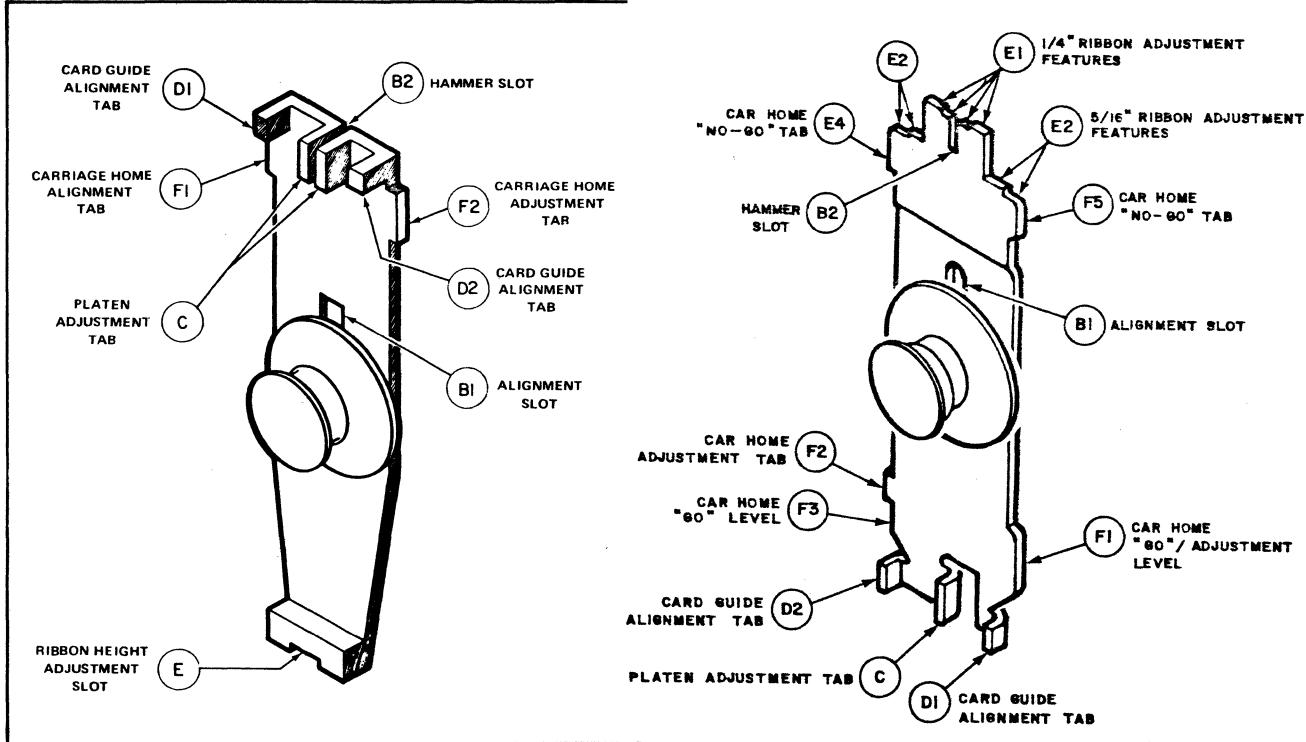
Figure 3-12. Alignment Tools

(b) Remove any paper from the carrier, remove the ribbon cartridge, and remove the printwheel.

(c) Install the tool firmly on the printwheel motor shaft, and ensure that it is properly seated with its Alignment Slot B1 centered over the printwheel alignment tab. Rotate the printwheel motor and tool to bring the tool's Hammer Slot B2 to the top in front of the print hammer.

(d) Block the carriage home sensor (insert a piece of dark paper in its slot) to detent the printwheel motor.

(2) Alignment Check

Refer to Figure 3-13. Manually push the hammer forward lightly, until its face enters Hammer Slot B2 on the tool. If the hammer slides easily into the tool slot without contacting the sides of the slot, printwheel-to-hammer alignment is correct; remove the carriage home sensor block and skip to Step 5. If the hammer face contacts the tool surface, continue with this procedure.

(3) Printwheel Alignment

Place a 1/4" open end wrench on the printwheel motor shaft's nut to prevent the shaft from turning. Move the tool as necessary to achieve proper alignment with the hammer.

CAUTION

In this step, the tool is moving the printwheel locator/sensor on the motor shaft, where these parts have been previously bonded together with adhesive. DO NOT flex or bend the printwheel locator/sensor – USE THE TOOL to apply the pressure to break the bond and move the part. Rebond with Permabond when alignment has been completed.

NOTE

Permabond 240^{TM} must be kept properly stored (at 50 degrees F) and used while fresh ONLY for proper bonding. The material deteriorates rapidly after exposure (container opened) or after its temperature is allowed to rise.

(4) Final Check

Repeat Step 2 to verify proper Printwheel-to-Hammer alignment. Remove the carriage home sensor block.

3-14
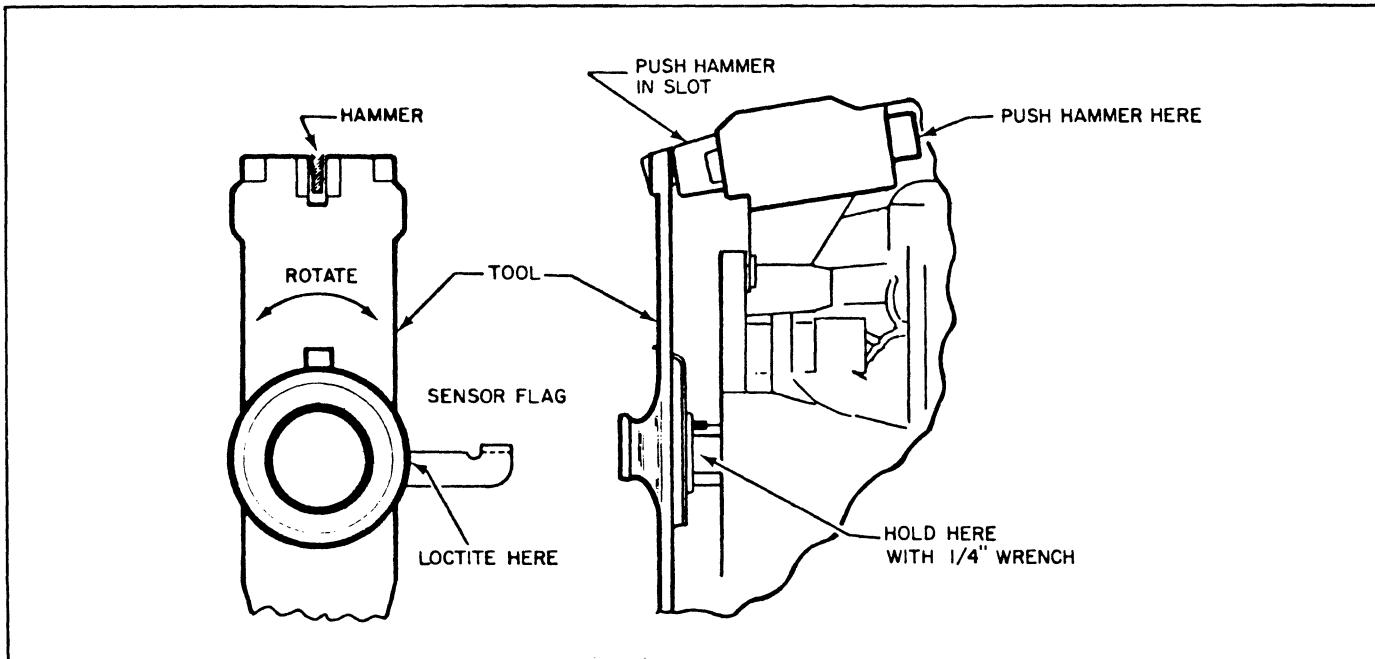
Figure 3-13. Printwheel-to-Hammer Alignment

(5) Printwheel Home Adjustment (Figure 3-14). Tilt the printwheel motor forward, away from the platen, and remove the alignment tool. Install a printwheel and initiate a RESTORE sequence. The printwheel logic includes a safety feature called "retry." This feature helps, during the RESTORE sequence, to ensure that the printer microprocessor has the right count in its absolute counter for printwheel position. The printwheel is allowed to stop only at those points where the signal +PW EVEN is high, which occurs only once per printwheel position, or "petal" position. If the printwheel fails to stop in a position where +PW EVEN is high, the microprocessor will reissue the printwheel portion of the RESTORE sequence. The printwheel restore sequence will retry stopping the printwheel in a proper position. If the microprocessor is unable to obtain the correct condition after 8 consecutive attempts (retries), it will issue a CHECK command to stop the printer. This situation normally indicates that a printwheel home adjustment is needed.

After a RESTORE sequence, the capital "E" must be positioned squarely in front of the print hammer. If it is not, a printwheel home adjustment is needed. Proceed as follows:

(a) Use a 7/16" open end wrench to adjust the home sensor eccentric (A) as follows: move the eccentric slightly, in either direction, and RESTORE the printer. Continue adjusting the eccentric in that direction, a little at a time, until the printwheel spins (8 revolutions) and the printer goes into its CHECK mode. Note this eccentric position.

(b) Move the eccentric in the opposite direction in the same manner until the printer goes into CHECK again. Note this eccentric position.

Figure 3-14. Printwheel Home Adjustment

(c) The two extremes noted above may be as much as 180 degrees apart. Adjust the eccentric to the approximate midpoint between these two extremes.

(d) If the printwheel spins continuously (8 revolutions), the sensor (B) may be located too far from the printwheel home sensor flag (C). Loosen nut (D) and rotate the sensor clockwise until the printwheel stops on the first revolution. Use a plastic shim to verify .003" to .007" (.08-.18mm) clearance between the surface of the sensor and the edge of the flag. Retighten nut (D).

(e) The electrical signal out of the sensor should be at least .4 volts peak. Figure 3-14 illustrates this signal, as seen at the input to the Printwheel Home Sensor amplifier on the SERVO board.

3.4.1.4.3 Platen-to-Printwheel. Refer to Figure 3-15. Proceed as follows:

(1) Preparation

NOTE

It will be necessary to readjust platen height for print quality, and the card guide after completion of this procedure.

(a) Loosen the card guide mounting screws, and lower the guide as far as it will go.

(b) Tilt the printwheel motor forward, away from the platen, and install the Alignment Tool. Make sure the tool is fully seated. Tilt the motor rearward and verify that the tool clears the card guide completely. Tilt it forward again.

(c) Place the carriage servo switch, located near the top edge of the CAR PWR AMP board, slot D, in its off position.

(d) Loosen the front eccentric on each end of the carrier assembly, and set each to its mid-range (lobe facing rearward) with a 7/16" open end wrench. Retighten the eccentric lock screws.

(2) Alignment Check

Move the carriage as far left as it will go. Tilt the printwheel motor rearward and verify that .0002" - .003" (.005-.076 mm) clearance exists between tabs C of the tool and the platen surface. Tilt the printwheel motor forward (away from the platen) and move the carriage as far right as it will go. Tilt the printwheel motor rearward again, and check the platen-to-tool relationship. If the platen adjustment is within these linits, AND is equal for both ends of the platen, no adjustment is necessary. If these criteria are not met, continue with this procedure.
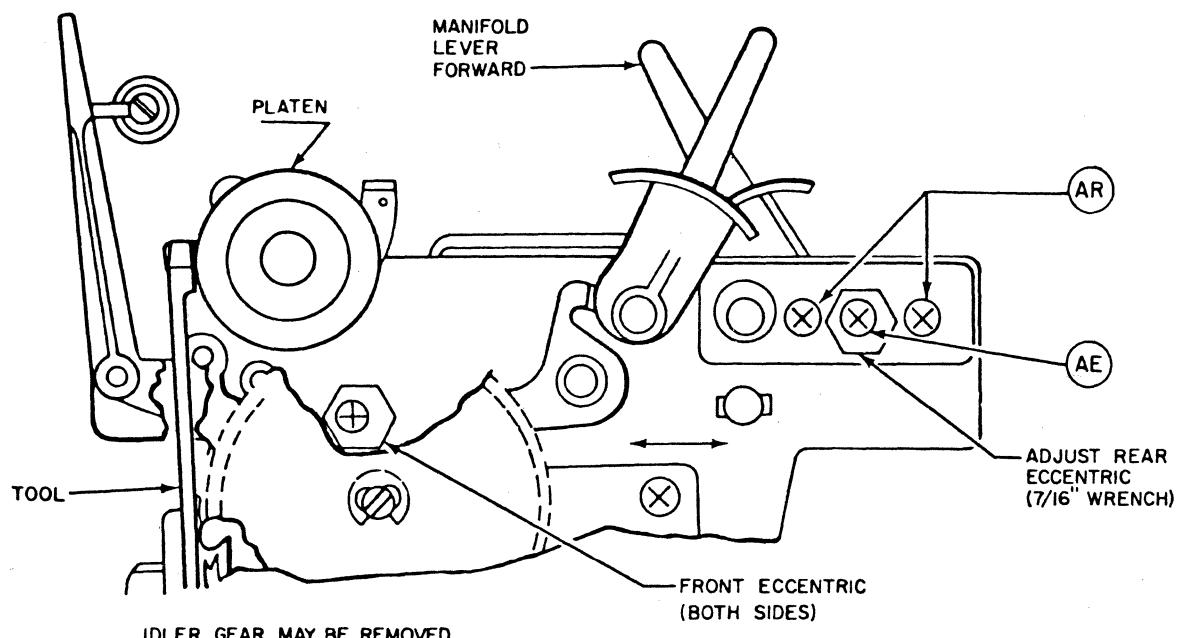
Figure 3-15. Platen-to-Printwheel Adjustment

(3)   Platen Adjustment (Repeat for each end)

Loosen the two rear eccentric slide clamp screws (AR) and the screw for the rear eccentric itself (AE). Adjust the rear eccentric, using a 7/16 in. open end wrench, to bring the platen clearance to within the limits specified. Tighten the slide clamp screws. Move the carriage to the opposite end of the platen and check for proper clearance. Repeat these steps until the clearances on each end are within the limits specified, and are equal. Tighten the rear eccentric slide clamp screws when this adjustment has been completed, and then tighten eccentric screws.

When this adjustment has been completed, be certain to perform the Platen Height adjustment (3.4.1.4.4) and the Card Guide adjustment (3.4.1.4.5).

3.4.1.4.4   Platen Height. Refer to Figure 3-15. Proceed as follows:

(1)   Preparation

Make sure the Platen-to-Printwheel adjustment (3.4.1.4.3) is correct. Install the printwheel normally used.

(2)   Adjustment Check

All characters should print with equal darkness on top and bottom all across the print line. Check with a line of capital "H"s. Refer to the print quality check (3.4.1.1) and Figure 3-6.

(3)   Platen Height Adjustment

Loosen the clamp screws on the front eccentric on each end of the carrier assembly. Turn the eccentrics as required to obtain the proper print quality uniformly along the length of the platen. Tighten the clamp screws and recheck the print quality.

3.4.1.4.5   Card Guide Height and Position. Refer to Figure 3-16. Proceed as follows:

(1)   Preparation

If the card guide is loose from the preceding adjustment, go on to step (3). If not, remove the alignment tool, install a printwheel and a sheet of paper, and type a series of identical characters along one line.

(2)   Alignment/Adjustment Check

The bottom edge of the triangular openings (A1) must be in line with the bottom lines of a series of identical characters within .000 in. to .005 in. (.00 mm to .13 mm).

(3)   Card Guide Alignment/Adjustment

Install the alignment tool on the print-wheel motor shaft, making sure it is firmly seated. The procedure from this point is slightly different depending upon which alignment tool is used.

(a)   Tool No. 40795:

Push the print hammer into the Hammer Slot B2 on the tool, and hold it there. Raise the card guide gently, until its top edge contacts the undersides of Card Guide Alignment Tabs D1 and D2 with equal pressure. Release the hammer and, while holding the card guide in contact with the tool, tighten the two mounting screws.

(b)   Tool No. 40795-01:

Raise the card guide until its top edge contacts the undersides of Adjustment Tool Tabs D1 and D2. Gently move the tool slightly from side to side while raising the card guide until it contacts the tabs with EQUAL pressure. Hold the card guide firmly in this position, and tighten the two card guide mounting screws.

Using a .005 in. plastic shim, check for no-drag shim clearance between the card guide and the ribbon guide posts on both sides of the carriage. Normally, this dimension is set by the depth of the ribbon guide post tabs. Shim drag indicates the card guide has become tilted, in which case its support arms should be gently reformed to achieve proper clearance around the ribbon guide posts.

Using the .005 in. plastic shim, check for no-drag clearance between the card guide and the platen along the full length of the platen.

3.4.1.4.6   Ribbon Height. Refer to Figure 3-17. Proceed as follows:

(1)   Preparation

Install a carbon ribbon on the carriage, and rotate the Alignment Tool to bring Ribbon Height Adjustment Slot E to the top.

(2)   Adjustment Check

Push upon the ribbon plate arm as shown, and observe the top edge of the exposed ribbon through Slot E in the adjustment tool. The top edge of the ribbon should be visible <u>within</u> the slot, and should not be visible <u>above</u> the top of the tool.
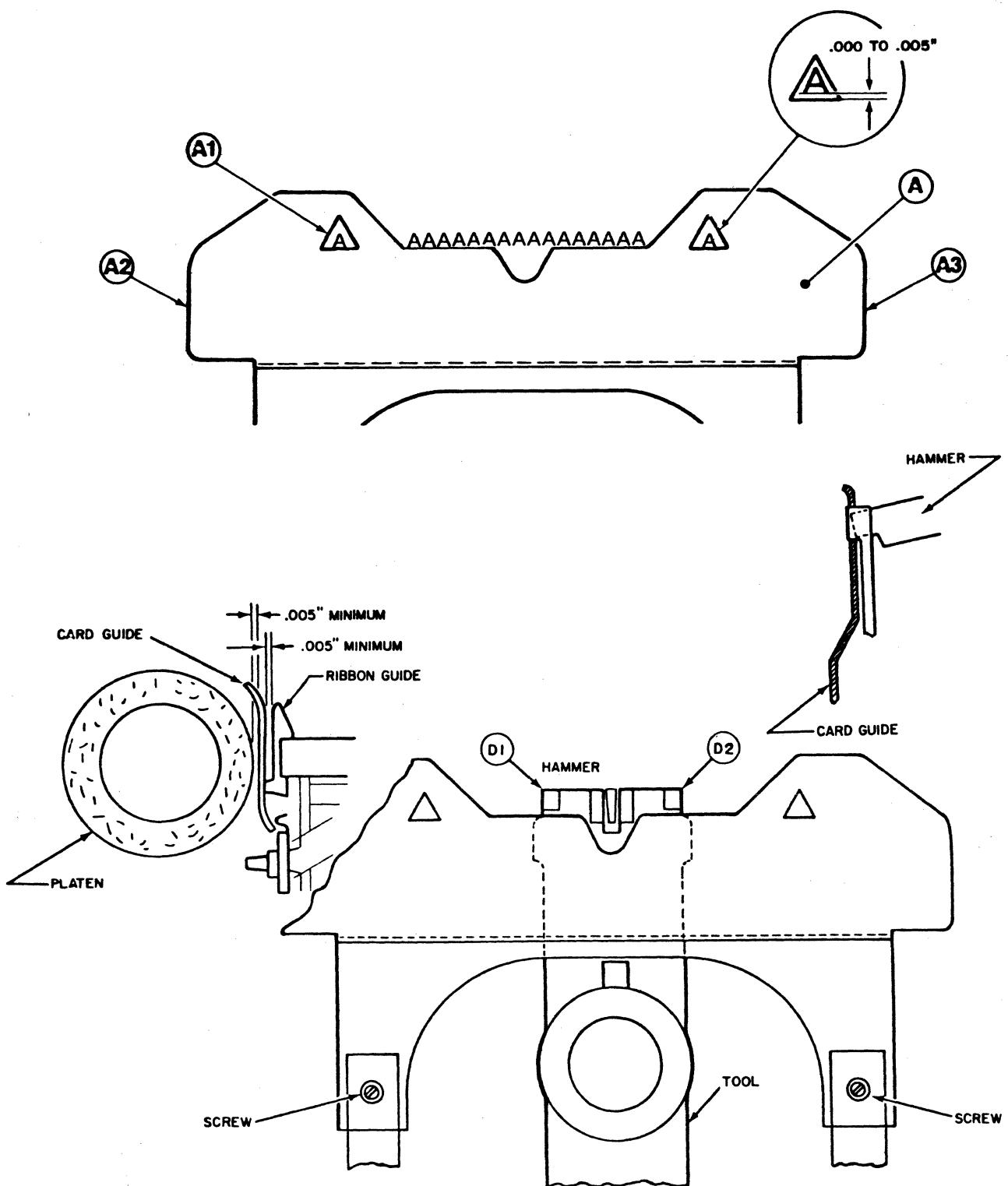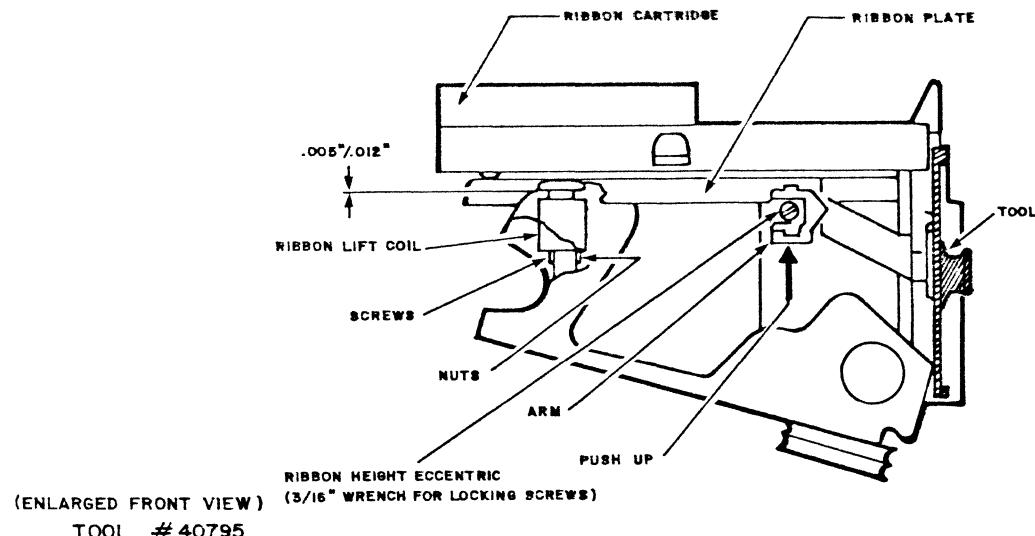
Figure 3-16. Card Guide Adjustments

RIBBON CARTRIDGE   RIBBON PLATE

.005"/.012"

RIBBON LIFT COIL

SCREWS

NUTS

ARM

PUSH UP

RIBBON HEIGHT ECCENTRIC
(3/16" WRENCH FOR LOCKING SCREWS)

TOOL

(ENLARGED FRONT VIEW)
TOOL #40795

RIBBON (CARBON)

E

TOOL #40795-01

E1   E1   TOP EDGE
E1

1/4"
RIBBON
5/16"

E2   BOTTOM EDGE   E2
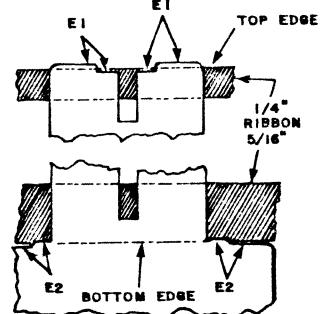
Figure 3-17. Ribbon Height Adjustment

(3) Ribbon Height Adjustment

(a) Tool No. 40795:
Loosen the ribbon height eccentric locking screw. Adjust this eccentric as required to move the ribbon height to within the tool limits. Note that it may be necessary to reform the ribbon plate arm slightly in some cases to achieve proper ribbon height limits. Tighten the eccentric locking screw.

(b) Tool No 40795-01:
Either 1/4" or 5/16" ribbon may be used in making the adjustment with this tool.

1/4" ribbon:
Ribbon height is adjusted using Tool features E1. Adjust ribbon height as outlined above to place the TOP EDGE of the ribbon between the high and low planes of features E1 as shown.

5/16" ribbon:
Ribbon height is adjusted using Tool features E2. Adjust ribbon height as outlined above to place the BOTTOM EDGE of the ribbon between the high and low planes of features E2 as shown.

3.4.1.4.7 Ribbon Lift. Refer to Figure 3-17. This adjustment should be checked whenever the ribbon height is altered.

(1) Preparation

Make sure the ribbon height adjustment is correct.

(2) Adjustment Check

Lift up on the right front corner of the ribbon platform so that the yoke is against the bottom of the ribbon height eccentric. There must be .005 to .012 in. (.13 to .30 mm) clearance between the ribbon coil armatures and the ribbon platform.

(3) Ribbon Lift Adjustment

Loosen the ribbon lift coil mounting screws. Place a .005 in. plastic shim between the ribbon lift coil armatures and the ribbon platform. Energize the ribbon coils with 12-15 volts and lift the right front corner of the ribbon platform so that the yoke is against the bottom of the ribbon height eccentric. Hold the platform in this position, and raise the ribbon coils so they are firmly and equally seated against the platform. Tighten the coil mounting screws and remove the shim.

3.4.1.4.8 Hammer. There are two hammer adjustments: hammer coil position and armature stop eccentric. These adjustments are simplified when tool no. 40796 is used, but they can be performed without it if necessary. Refer to Figure 3-18.

(1) Preparation

The following conditions should be present: power off; printwheel installed; ribbon removed; platen position lever fully forward.

(2) Adjustment Check (the Platen-to-Print-wheel adjustment, 3.4.1.4.3, must be correct before checking hammer adjustments.)

To check hammer coil position, first rotate the printwheel to place one of the larger characters (M, W, E, etc.) in front of the hammer. Then insert the mid-diameter portion of tool no. 40796 between the armature (A) and the anvil of the print hammer (C), and push the armature against the hammer coils (F). This will force the hammer (C) in to nestle the selected printwheel petal (D) lightly against the platen (E). Gently rock the printwheel slightly back and forth, and verify that the petal can move with a very slight drag. Repeat this check, rotating the platen and/or moving the carriage each time, to check the entire printing surface.

If tool no. 40796 is not available, hold the armature against the hammer coils while pushing the hammer against the printwheel to obtain the relationship noted above, and measure the clearance between the armature and the hammer anvil. It should be .073 in. to .083 in. (1.85 mm to 2.10 mm).

To check the armature stop eccentric, hold the armature (A) against the hammer coils (F), and check the clearance between the armature and the stop (B). There should be .042 in. to .048 in. (1.07 mm to 1.22 mm) clearance, or the smallest diameter of tool no. 40796 should fit with very light resistance.
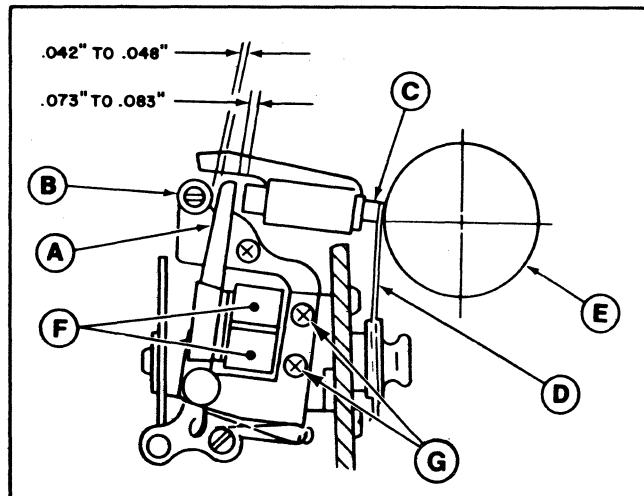
Figure 3-18. Hammer Adjustments

(3) Hammer Coil Adjustment

Loosen the hammer coil mounting screw (G) and reposition the coils to obtain th proper relationship between the hamme and the platen as noted above. Retighte the screws. Recheck the armature sto eccentric adjustment.

(4) Armature Stop Eccentric Adjustment

Loosen the lock nut slightly, and turn th screw until the desired clearance is ob tained. Prevent the screw from turning a the lock nut is retightened.

3.4.1.5 CARRIAGE HOME (Figure 3-19)

(1) Preparation

With power applied to the printer, initiate a Restore sequence.

(2) Adjustment Check

(a) Tool No. 40795:

Insert the tool between the left sid of the printer's main frame castin and the carriage frame, just abov the carriage home sensor. Th maximum clearance between too Tabs F1/F2 and the printer assem blies should be .017 in. (.43 mm).
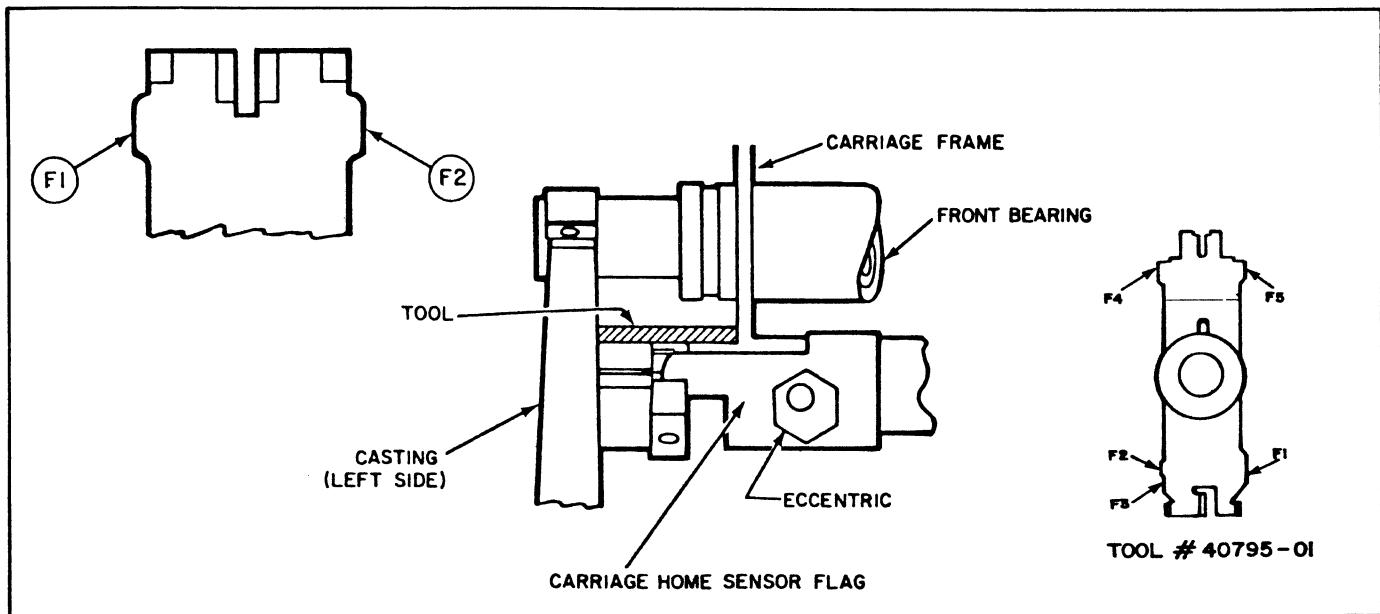
Figure 3-19. Carriage Home Adjustment

(b) Tool No. 40795-01:

Insert the tool between the left side of the printer's main frame casting and the carriage frame, just above the carriage home sensor. Using tool tabs F1-F5, check for proper clearance as follows:

Tabs F1/F3 should pass (go)
Tabs F4/F5 should <u>not</u> pass (no go)

(3) Carriage Home Sensor Flag Adjustment

Unlock the carriage home sensor flag eccentric, and adjust it to move the flag LEFT for "not enough" clearance, or RIGHT for "too much" clearance. After each movement of the eccentric, remove the alignment tool, turn off power, move the carriage to the right, restore power, and cycle the printer through the RESTORE sequence. When this adjustment is being changed, try to achieve a clearance as close as possible to tool Tabs F1/F2 (either tool). Tighten the eccentric clamp screw when the adjustment is complete.

3.4.1.6 BOTTOM-FEED PAPER CHUTE (Figure 3-20)

This is an optional feature, not found on all HyTerms.

(1) Preparation

(a) Make sure the following adjustments are correct:

Paper Feed Rollers	3.4.1.2.2
Platen Position	3.4.1.4.3
Platen Height	3.4.1.4.4
Card Guide	3.4.1.4.5

(b) Turn off power. Raise or remove the access cover, and remove the platen. Remove any paper.

(2) Adjustment Check

(a) The top edge of the paper chute (B) must be in line vertically within .030 in. (.76 mm) of the top 45-degree bend of the card guide (C). This must not vary more than .030 in. (.76 mm) over the entire length of the carriage travel.

(b) There should be .040 in. to .060 in. (1.0 mm to 1.5 mm) clearance between the paper chute and the front pressure rollers. Clearance should be equal at both ends.

(c) The paper-out bail should touch the chute at both ends.

(3) Paper Chute Adjustments

NOTE

If any of these adjustments are performed, be certain to check the bottom-feed paper-out switch adjustment (3.4.6.2).

(a) To adjust the height of the chute, loosen screws (D) and (F), position the chute properly, and tighten screws (D). Then perform adjustment (b).

(b) To adjust the paper chute/pressure roller clearance, loosen screws (F), position the chute properly, and tighten screws (F).

(c) To adjust the paper-out bail, loosen the set-screws in the hubs at both ends of the bail, form the bail slightly, if needed, and tighten the setscrews.

3.4.2 Control Panel

The only adjustment on the control panel is a volume control adjustment for the audible alarm.

3.4.2.1 Volume Control

Remove the access cover from the HyTerm. With a small screwdriver, turn the adjusting potentiometer until the desired volume is obtained. The potentiometer is accessible through a hole in the right side of the control panel near the buzzer. To sound the audible alarm after each adjustment, operate the RESET key and then attempt to to print a character. The alarm will sound for an cover-open error.

3.4.3 Power Supply

There is only one adjustment that can be made on the power supply, the +5 voltage adjustment. This adjustment will have a small effect on the other voltages, but if the +5 volt supply is properly adjusted, all other supplies should fall within their operating limits. If they do not, some malfunction is present and will have to be corrected.

All voltages should be checked whenever the power supply or one of its components is replaced, when one of the voltage regulator ICs on the HPRO board is replaced, and any other time that power supply problems are suspected. The tolerances given in the following procedure are for adjustment purposes only. That is, if a voltage is slightly outside the limits listed, but the HyTerm is operating properly, no adjustment is required. On the other hand, if a voltage is within the specified limits, but at the
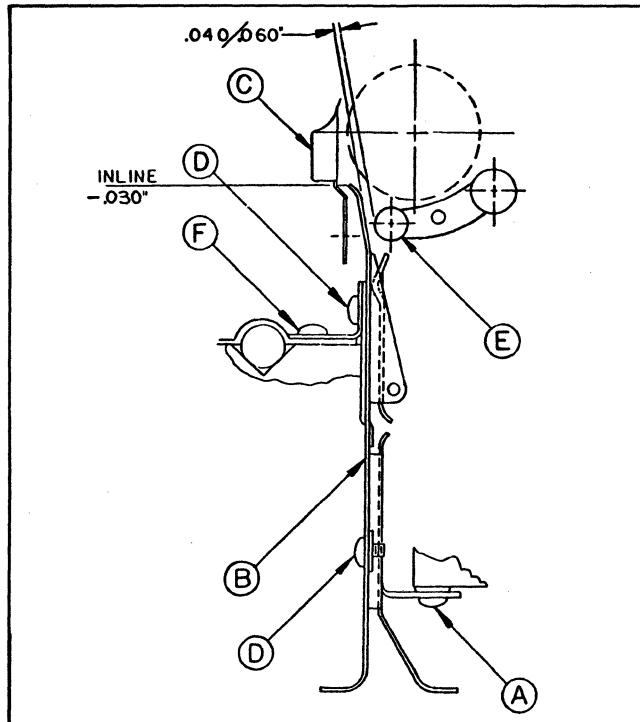
Figure 3-20. Paper Chute Adjustment

fringe, and power supply problems are suspected, an adjustment should be performed. The use of a digital voltmeter is recommended because of the more precise readings obtainable. Proceed as follows:

(1) Unplug the HyTerm from its power source. Raise or remove the access cover. Remove the platen. Remove the top cover (3.1.2).

(2) Remove the XMEM board (if installed) from slot(F) and install circuit board extender into slot (F).

(3) Plug the HyTerm power cord into the wall outlet.

WARNING

When the HyTerm is connected to a power source, line voltage is present at the POWER switch terminals. To avoid a dangerous shock when power is applied with the top cover removed, keep your fingers away from the POWER switch terminals.

Turn on power and measure the voltage between pins 1-4 and the following pins on the circuit board extender:

Pins 5-6	+5.0V ± .1V
Pins 41-42	+15.25V ± .75V
Pins 49-50	+15.25V ± .75V
Pins 23-24	-15.25V ± .75V
Pins 31-32	-15.25V ± .75V

(4) If the +5 volt supply is correct and some other supply is not, a malfunction is present and must be corrected. If the +5 volt supply is not correct, proceed with step (5).

(5) Turn off power. Tilt the HyTerm up so that it is resting on the rear edge of its bottom cover.

CAUTION

When tipping the HyTerm up, be certain to use a flat surface, with no foreign objects in the way. Any small objects could cause pressure to be applied to the rear heat sinks, which are mounted on the power amplifier boards. Excess pressure on these boards could damage the boards and/or the mother board.

CAUTION

Whenever the HyTerm is tilted up in this manner, hold on to it with one hand to prevent it from falling over.

(6) Remove the screen-like bottom pan from the HyTerm by loosening the rear three screws, removing the remaining five screws, and lifting the bottom pan off the machine.

(7) Fasten the voltmeter probe firmly to pins 5 and/or 6 of the circuit board extender.

WARNING

In the following step, be very careful not to touch any part of the power supply, because extremely high voltages (200-300 volts) are present.

(8) Turn on power. Using a non-metallic screwdriver, adjust the power supply potentiometer to provide +5 volts, ± .1 volt, at pin 5.

(9) Turn off power. Replace the bottom plate. Tilt the HyTerm back down onto its feet, remove the board extender, replace the top cover and the platen. Test the HyTerm for proper operation.

3.4.4 Keyboard

The only keyboard adjustment is the positioning of the keyboard for proper top cover fit. This is normally required only when the keyboard has been removed or when a different top cover is installed. This adjustment entails trial-and-error positioning of the keyboard followed by installation of the top cover. See 3.3.4 for details.

3.4.5 Cover-Open Switch

Before making any adjustment, be sure that the top cover fits the bottom cover properly, and that the access cover fits the top cover properly and is tight. Adjust and/or form the access cover clamp springs (replace if necessary) to tighten the access cover. If switch adjustment is still necessary, loosen the cover-open switch operating bracket (fastened to the inside lower edge of the access cover), move the bracket up or down slightly, and retighten the lock screw. Check the adjustment by making sure the switch operates each time the access cover is opened or closed.

3.4.6 Paper-Out Switch

The procedure for adjusting the paper-out switch varies, depending upon whether the standard top-feed or the optional bottom-feed paper supply is used.

3.4.6.1 TOP-FEED

This switch is functional only when a forms tractor or pin-feed platen is used. When a friction-feed platen is used (without forms tractor), the switch is held in its non-operated (paper in) position by the paper release lever's being in its rearward position. When the paper release lever is moved to its forward position, the switch operating mechanism is unlocked and allowed to sense the paper-out condition.

Before starting this adjustment, be certain that the Paper Feed Rollers adjustment (3.4.1.2.2) and the Platen Position (3.4.1.4.3) and Platen Height (3.4.1.4.4) are correct. Perform the adjustment with the platen installed and the paper release lever in its rearward position (pressure applied). Referring to Figure 3-21, proceed as follows:

(1) Using a .050 in. Allen setscrew wrench, loosen the setscrew (1) in the bell crank on the end of the paper-out bail pivot shift (2). The front edge of the bail should touch the platen surface squarely within .003 in. (.08 mm). [A gap of .010 in. (.25 mm) maximum due to bowed paper-out bail is permissible.] If necessary to adjust, loosen the setscrew (3) at either end (or both), adjust, and tighten the screw(s).

(2) Loosen the switch mounting screws (4), and adjust the switch to transfer when the bail is .010-.020 in. (.2-.5mm) away from the platen. Tighten the screws.
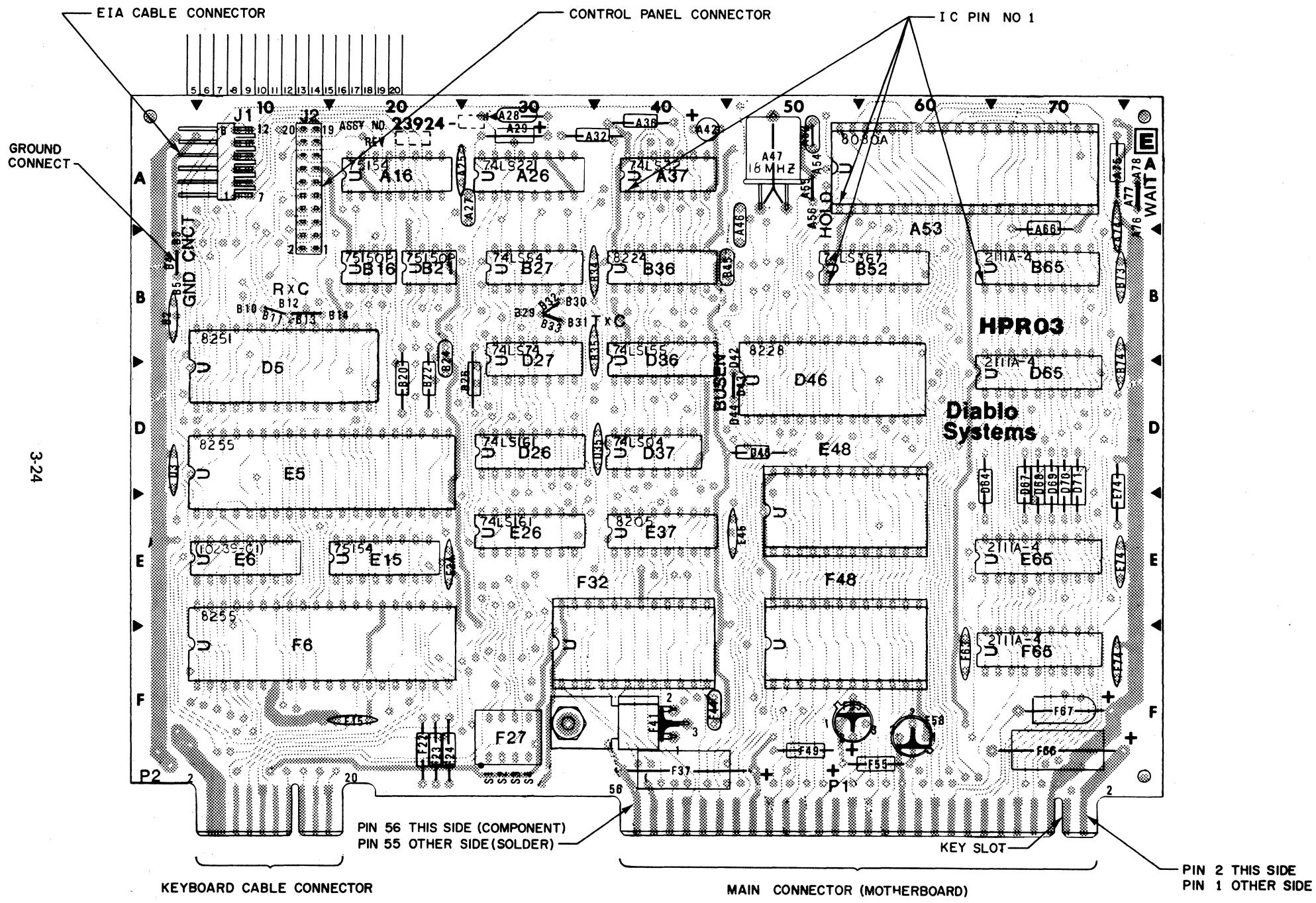
Figure 3-22. Circuit Board Component Location and Pin Numbering

(3) Move the bail back away from the platen fully. The bail legs must bottom against the printer "comb" frame, and not against the switch. If necessary, form the switch arm to allow the switch to transfer sooner, and reposition the switch to obtain the proper adjustment as noted in step (2).

(4) Remove the platen, and move the bail rearward until its legs come within .030 in. (.76 mm) of the comb. Hold the bail in this position and rotate bellcrank (5) until its ear (6) rests against the actuator lever arm (7). Tighten setscrew (1). After tightening the screw, the shaft (2) should pivot freely with .005 in. (.13 mm) maximum end play. Install the platen, move the pressure release lever back and forth several times, and stop with the lever in the rearward position. There must be at least .090 in. (2.3 mm) clearance between the bail and the platen.

3.4.6.2 BOTTOM-FEED (OPTIONAL)

This switch is functional only when the enable/override switch, mounted to the left of the front carriage rail, is in the ON position (toward the rear). When the enable/override switch is OFF, it overrides the paper-out switch, making it non-functional.

Before adjusting the bottom-feed paper-out switch, make sure the Bottom-feed Paper Chute (3.4.1.6) is adjusted properly.

The paper-out switch should transfer when the paper-out bail is .025-.040 in. (.63-1.0 mm) away from the front paper chute. Loosen the switch mounting screws and reposition the switch to obtain this adjustment. Tighten the screws. If adjusting the switch limits the movement of the paper-out bail to less than .100 in. (2.5 mm), form the switch arm to allow the switch to transfer sooner, and reposition the switch to obtain the proper adjustment.

3.5 COMPONENT IDENTIFICATION

There are two methods used to identify components within the HyTerm. The first is an extension of the reference designator system used to identify replaceable modules (Section 3.3). The second is a coordinate system used to identify components on the plug-in circuit boards. Also, closely related to component identification is the location of connectors and the numbering of connector pins.

3.5.1 Reference Designator System

The reference designator system is used to identify individual components mounted to the printer frame, as well as components on the control panel, in the power supply, and on the keyboard. Table 3-2 defines the class letters used on schematics and wiring diagrams to refer to various items. On the control panel and keyboard, the reference designators for each component are etched on the circuit board. To locate a particular component in the power supply, you will first need to locate it on the power supply assembly drawing, and then find it on the power supply.

3.5.2 Coordinate System

Components are identified on the logic drawings as to type and location. The location information consists of a letter and a number, each representing coordinates on the circuit board. Refer to Figure 3-22. Letters are printed on the circuit board in the approximate center of the area they refer to, whereas numbers appear at the beginning of their respective area. As an example, to locate resistor E62, follow the "E" row horizontally to where it intersects the "60" column. Below the "60" and a little to the right (at "62") you will find resistor E62. Coordinates given for IC chips are the approximate location of pin no. 1. Coordi-
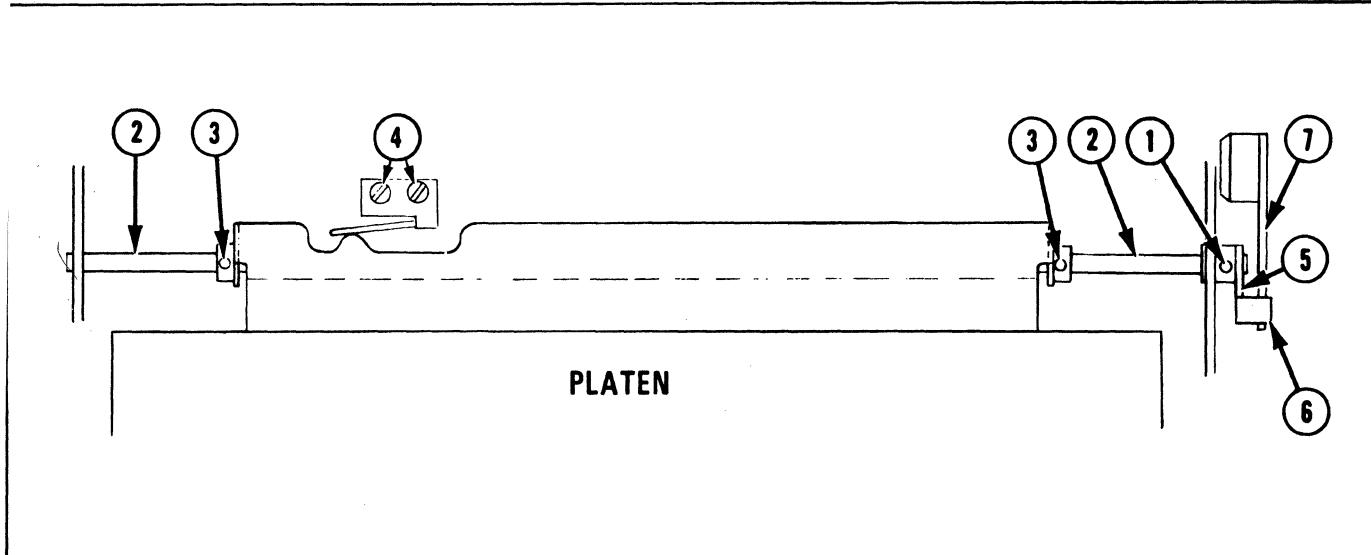
Figure 3-21. Paper-Out Switch Adjustment
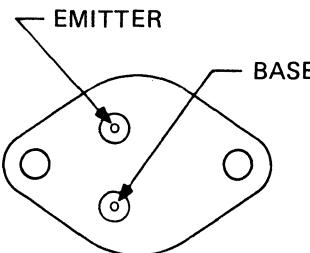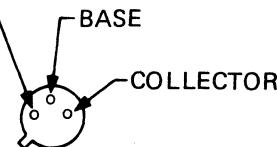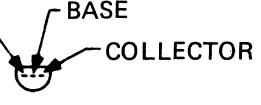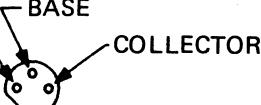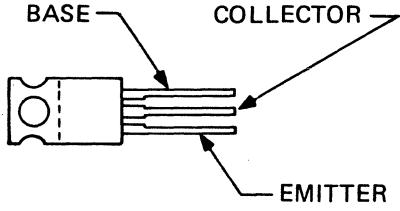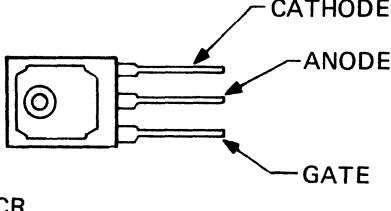
OUTLINE (BOTTOM VIEW)	DIABLO PART NUMBER	INDUSTRY TYPE NUMBER
EMITTER, BASE (COLLECTOR CONNECTED TO CASE)	42190–29 42190–30 USE SJ7280 USE 2N6545 USE SJ7280 42190–71	SJ7280 SJ7280 (Matched Pair) 2N6306 (SJ7280) 2N6308 2N6544 2N6545
EMITTER, BASE, COLLECTOR	10443-01 10444-01	2N3439 2N5320 2N5322
EMITTER, BASE, COLLECTOR	10105 42190–26 13013 42190–21 USE MPS-U60 42190–28 42190–60	2N3644 2N4126 2N4401 MPS-A43 MPS-A93 MPS5172 MPS6516
EMITTER, BASE, COLLECTOR	10105	2N3644
BASE, COLLECTOR, EMITTER	10445-01 13063 13064 42190–27 42190–70 13007	2N6103 TIP41A TIP42A TIP47 TIP49 TIP125
CATHODE, ANODE (+), LED	14005-01	MV5753
CATHODE, ANODE, GATE, SCR	42190–43	C122F (50316)

Figure 3-23. Semiconductor Lead Identification

Table 3-2. Reference Designators

Designator	Description
A	Assembly
B	Fan (blower)
C	Capacitor
CR	Diode (including bridge rectifiers, LEDs)
DS	Alarm (buzzer)
E	Individual terminal
F	Fuse
FL	Filter
J	Jack (connector, stationary portion)
L	Inductor (coil)
P	Plug (connector, movable portion)
Q	Transistor
R	Resistor
RT	Resistor, temperature-sensitive (thermistor)
S	Switch
T	Transformer
TB	Terminal board
TP	Test point
U	Integrated circuit
VR	Voltage regulator (zener diode)
W	Cable
X	Circuit board socket, fuseholder

nates for other "horizontally mounted" components (as in Figure 3-22) refer to the location of the leftmost lead. Letter coordinates for vertically mounted components that overlap rows usually refer to the row in which the largest portion of the component is located.

Pin no. 1 of each IC is easily identified from the bottom (solder) side of the board by its square solder pad. This lessens the chance of errors in counting pin numbers.

The mother board, the keyboard, and the control panel circuit boards do not use the coordinate system because of the small number of components involved. These boards use standard reference designators, which are silkscreened or etched onto the board, and referenced on the schematics.

3.5.3 Pin Numbering

Industry standards are followed for pin numbering of integrated circuits. Pin identification for all integrated circuits, including metal-can ICs, can be found in Section 4.

3.5.3.1 DISCRETE SEMICONDUCTORS

Pin identification for most discrete semiconductors is presented in Figure 3-23.
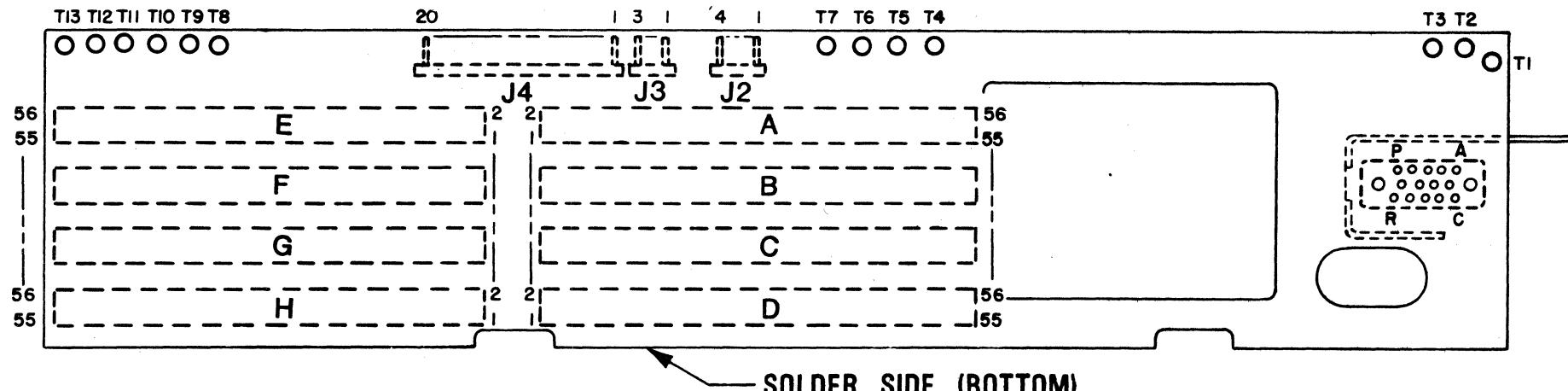
NOTE

Components in Figure 3-23 that are listed by Diablo part number should not be replaced by standard industry types. They should be ordered by Diablo part number because in some cases there are more stringent tolerances for the Diablo parts, and restrictions as to approved manufacturers, due to reliability and functional differences.

3.5.3.2 CIRCUIT BOARDS AND MOTHER BOARD

Pin numbering of circuit boards that plug into the left-hand half of the HyTerm is shown in Figure 3-22. Circuit boards on the right side are mirror images, so pin no. 1 is on the left side; pin no. 56 on the right. This is also shown in Figure 3-24.

The numbering of all mother board pins is shown in Figure 3-24. Signal names for all points, including power connections, are shown on schematic no. 40614.

TI3 TI2 TII TIO T9 T8   20 | 3 | '4 | T7 T6 T5 T4   T3 T2

J4   J3   J2

56   E   A   56
55   55

F   B

G   C

56   H   D   56
55   55

SOLDER SIDE (BOTTOM)

COMPONENT SIDE (TOP)

55   H   D   55
56   56

G   C

F   B

55   E   A   55
56   56

J4   J3   J2

TI3 TI2 TII TIO T9 T8   20 | 3 | 4 | T7 T6 T5 T4   T3 T2

TI
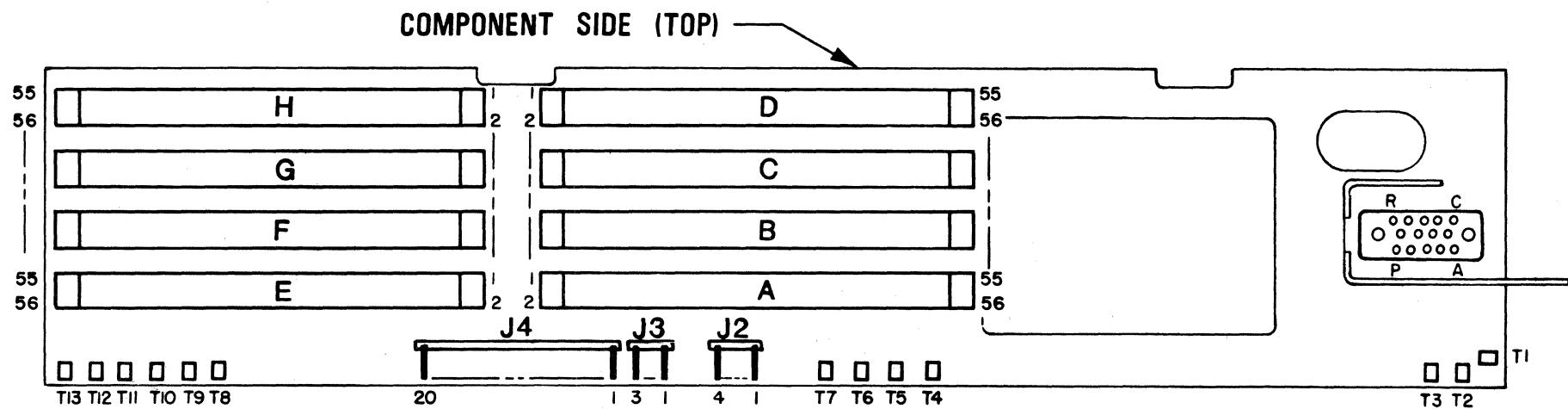
Figure 3-24.   Mother Board Pin Numering

3.5.3.3 KEYBOARD CABLE

Pin numbers are shown in Figure 3-25. Pin numbers and signal names are the same at both ends. Odd-numbered pins are on the top (component side) of the keyboard and the back (solder side) of the HPRO board; even-numbered pins are on the bottom (solder side) of the keyboard and the front (component side) of the HPRO board. Signal names are listed in Table 3-3.

Table 3-3. Keyboard Signal Names

Pin No.	Signal Name
1	+5 volts
2	SIGNAL GND
3	+5 volts
4	SIGNAL GND
5	Unassigned
6	Unassigned
7	Unassigned
8	-POR
9	-READY
10	Unassigned
11	-12 volts
12	+KYSTB
13	-DATA0
14	-DATA7
15	-DATA6
16	-DATA1
17	-DATA5
18	-DATA2
19	-DATA4
20	-DATA3
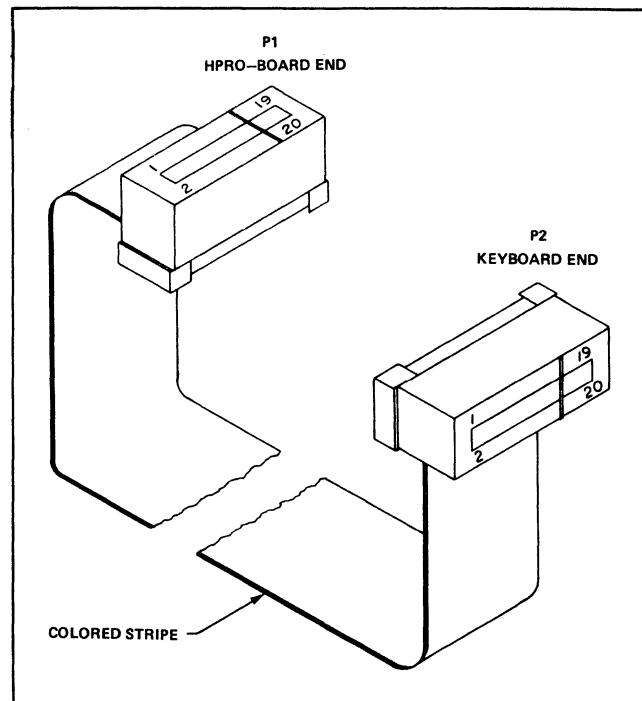
Figure 3-25. Keyboard Cable

3.5.3.4 CONTROL PANEL

The control panel cable is permanently mounted to the control panel circuit board, and connects it to the J2 connector on the HPRO3 board. There is no key in the control panel cable plug, so care must be taken to plug it in correctly. The colored stripe on the cable should be toward the bottom as the plug is installed on the HPRO3 board. See Figure 3-26 for pin numbering.

The control panel schematic no. 400056-01 shows the wiring for the circuit board and the cable. Cable signals are also identified on the Signal Cable Interconnection Diagram, no. 400089-01.
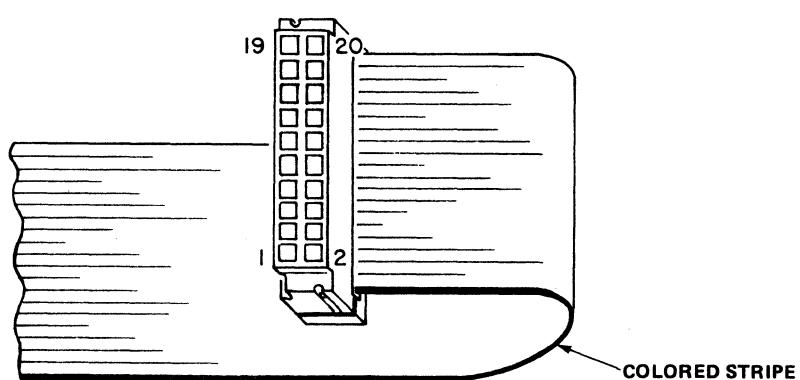
Figure 3-26. Control Panel Cable Pin Numbering

3.5.3.5 EIA CABLE

Complete information on the wiring of the EIA cable is given in Figure 3-27. Note that the male EIA connector is shown; the female connector on the modem or acoustic coupler is a mirror image of this. Note also that the J1 connector on the HPRO board is a mirror image of the P1 connector shown.

3.5.3.6 POWER SUPPLY

Figure 3-28 shows the wiring of the power supply cable and the connections to the power supply. Note that there are some unused pins in the female connector (P1), but that the J1 connector on the mother board that mates with it has all pins connected in some manner. The mother board schematic, no. 46080, lists all power connections.

NOTE

Do not disconnect terminal lugs from mother board in an attempt to read power supply voltages,–with no load on power supply, the readings will be erroneous. Use procedure given in 3.4.3.

WIRING LIST		
COLOR	EIA	P1
GREEN	1	6
RED	2	5
ORANGE	3	7
YELLOW	4	4
BROWN	5	9
BLUE	6	8
PURPLE	7	1
WHITE	8	10
BLACK	20	3
SLATE	23	2

✻ SPECIAL ORDER ONLY, SLATE WIRE NORMALLY CUT OFF AT JACKET
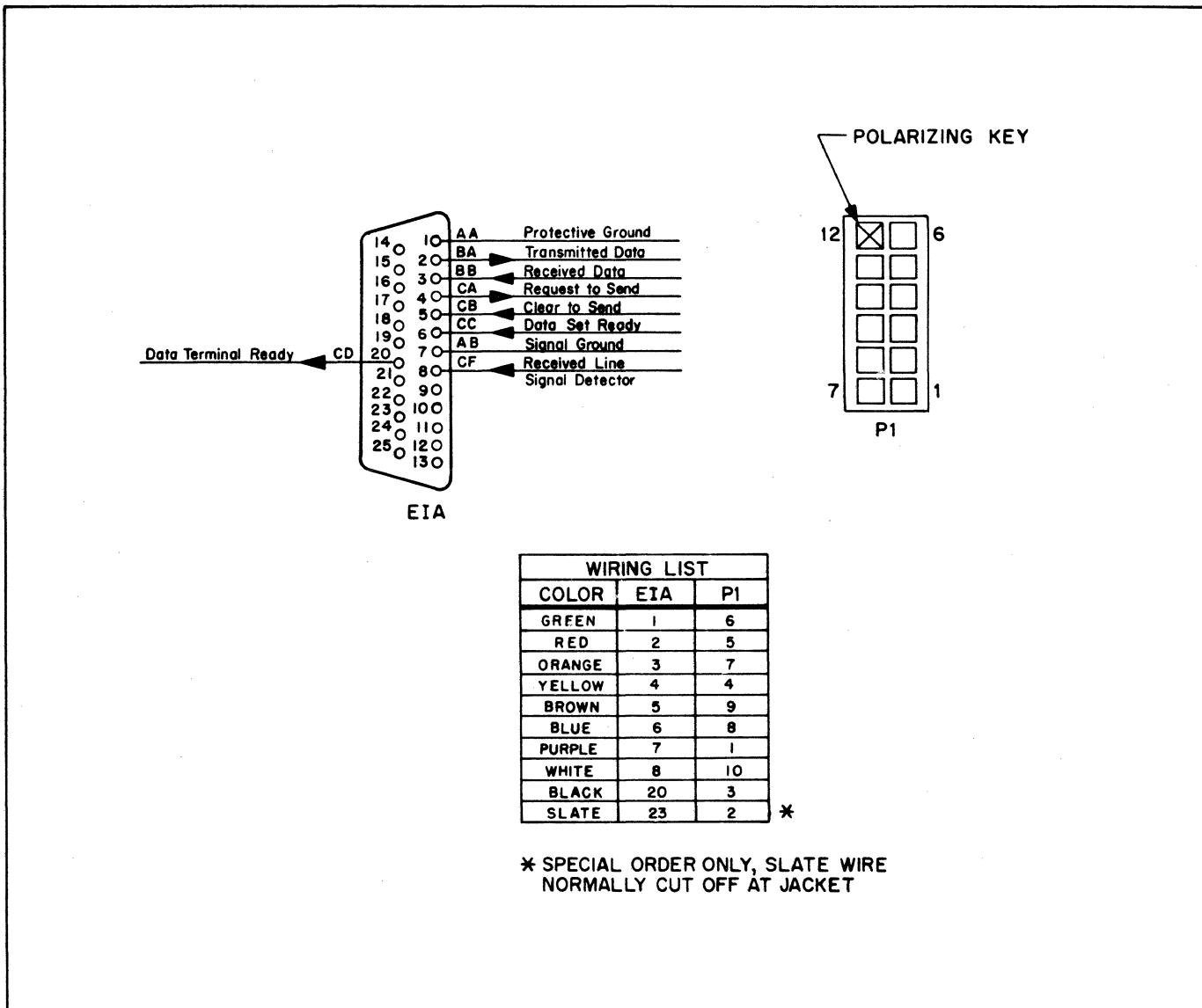
Figure 3-27. EIA Cable Pin Identification

TB1

POWER

SUPPLY

1 — WHITE — +5V L,J

2 — BLACK — GND A,B

3 — BLACK — GND C

4 — RED — +15V E,K

5 — BROWN — -15V P,R

6 (not used)

7 (not used)

AC TO FAN { BLACK 8   WHITE 9 }

BLACK } AC FROM POWER SWITCH WHITE }

T15 T14 T13 T12 T11

WHITE BLACK BLACK RED BROWN
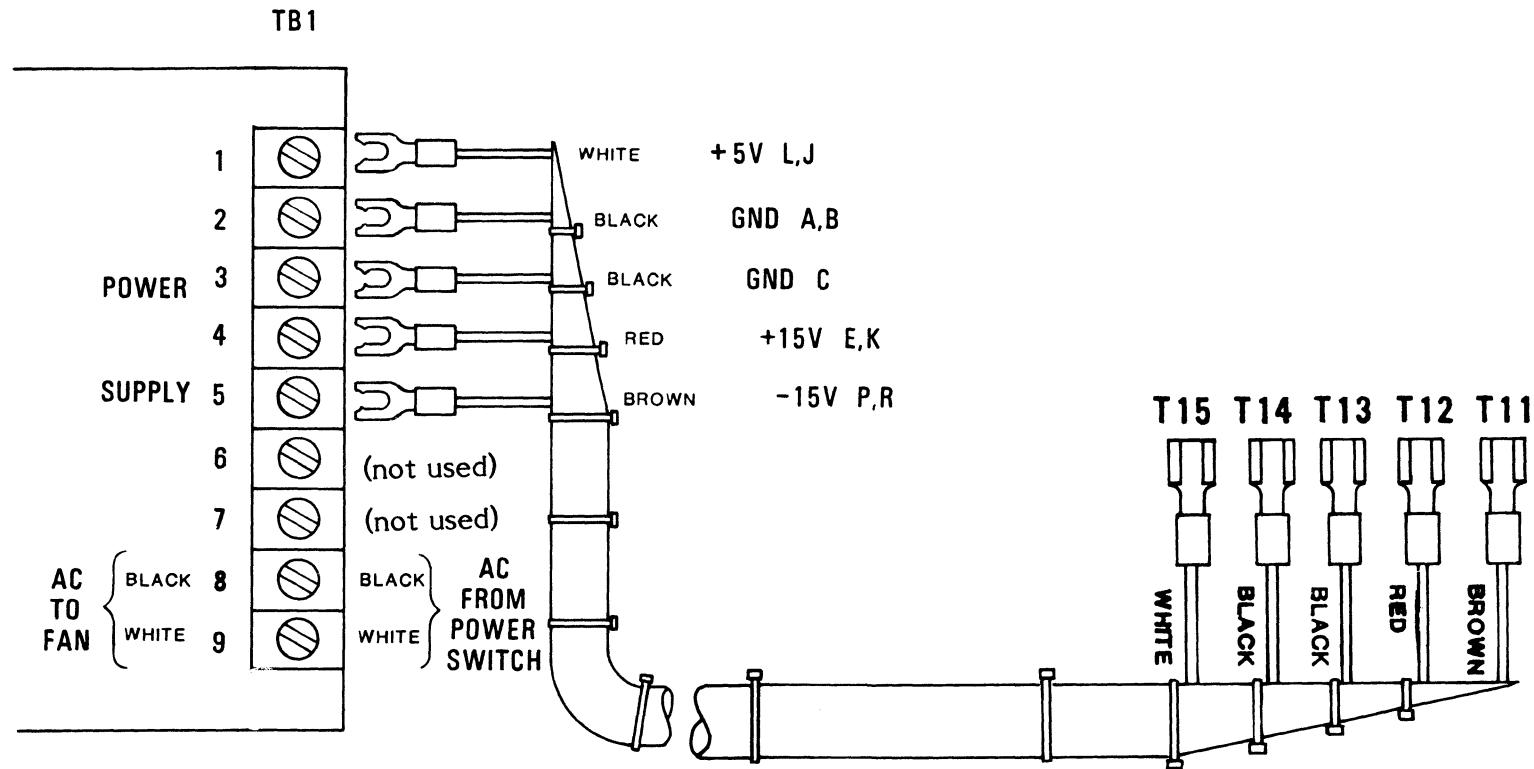
Figure 3-28. Power Supply Connections

Section 4

SCHEMATICS AND REFERENCE INFORMATION

4.1 INTRODUCTION

This section contains information on logic symbology and drawing conventions used in the schematic and logic diagrams, and information on the integrated circuits used.

4.2 FUNCTIONAL LOGIC

The logic diagrams are primarily intended for use by field service personnel as troubleshooting aids. As such, the first responsibility of a set of logic diagrams is to illustrate a design's principles of operation. For this reason, Diablo Systems logic diagrams emphasize the functions performed by the logic elements rather than the kinds of devices used to implement the functions.

For example, a NAND gate may appear on a logic diagram as either a positive logic AND function with the output inverted (NAND), or as a negative logic OR

AND FUNCTION

(POSITIVE LOGIC NAND)

OR FUNCTION

(NEGATIVE LOGIC NOR)

A	B	C	F
L	L	L	H
H	L	L	H
L	H	L	H
H	H	L	H
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	L

H = +5V   L = 0V
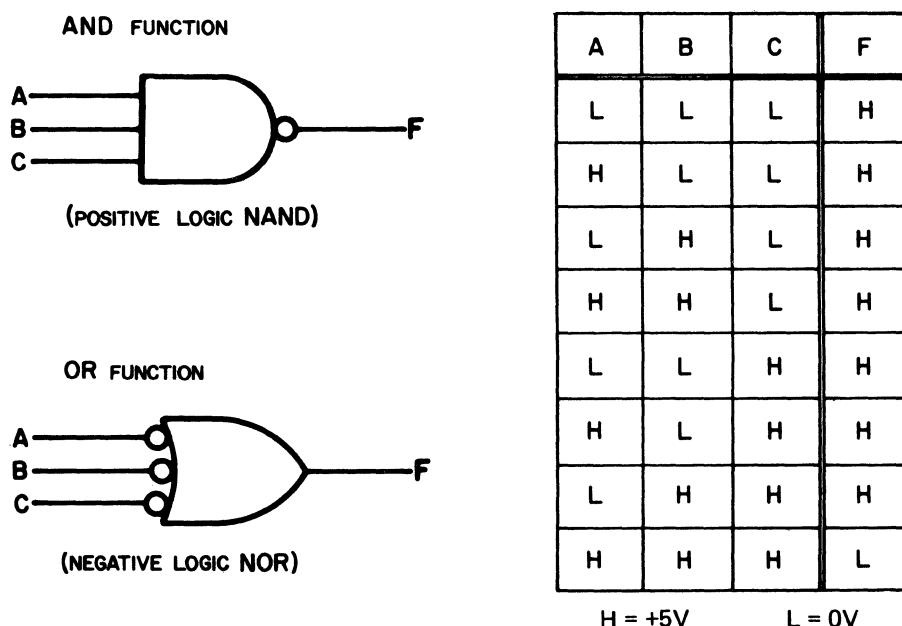
Figure 4-1   Example of Functional Logic

4-1

function with the inputs inverted (NOR). See Figure 5-1. This practice runs
contrary to some logic drawing standards, which require the use of the NAND
symbol for both functions. But, in Diablo Systems diagrams, different symbols
are used to distinguish between the two functions because the functional
elements are considered to be more relevant to the design theory than symbolic
representation of the kinds of devices used.

4.3   SIGNAL NOMENCLATURE

The active level of each logic signal is assigned a descriptive name. A
signal is considered active when it either causes or represents some logic
event that is significant to the progress of an operation. Consequently, the
name given a signal usually provides one of two kinds of functional
information:

(1)   Describes the effect that the signal's active level has on the logic it
      feeds; for example, -ENABLE INP allows data to be brought into the
      printer microprocessor.

(2)   Represents a condition or event that develops elsewhere in the logic;
      for example -FUN SWITCH 4 is the name of the signal that is active
      whenever the number 4 function switch (FORM FEED) is operated.

A plus sign (+) or a minus sign (-) generally precedes each signal name to
identify which of the two voltage levels used in the logic system is consider-
ed to be that signal's active level. The + sign represents the relatively
higher logic level and the - sign, the relatively lower level. (This means
relatively higher or lower with respect to each other; the signs do not always
indicate signal polarity with respect to ground.) For example, if -RESET is
low (0 volts), it means Reset is active; if -RESET is high (+5 volts), the
Reset function is inactive. If +USART INTERRUPT is high, it means the USART
has received a character from the data link and is ready to forward it to the
MPU; if +USART INTERRUPT is low, it means the USART has not received any data
from the data link that has not already been accepted by the MPU.

The actual voltage levels represented by the signs will depend on the logic
family being used. For example, in TTL circuits, the signal identified by
-RESET is active when it is at 0V (nominal) and inactive at +5V (nominal).

Sometimes a signal serves as the input to both positive logic and negative
logic elements. Ordinarily in such cases, the sign preceding the signal name
agrees with the active level indicated at the output of the logic element that
produced the signal.

Signal names appearing in the text are printed in all capital letters to
distinguish them from functions being performed. For example, '-RESET'
refers to an actual signal name, whereas 'Reset' refers to the reset operation
in general.

4.4   LOGIC SYMBOLOGY

The logic function symbols used in Diablo Systems logic diagrams conform
closely to those set forth in MIL-STD-806. Most small-scale integration

(SSI) circuits are represented by function symbols. Medium-scale integration (MSI) devices, such as shift registers and counters, may be represented by rectangles with functional labels.

Generally, a circle drawn at an input to a symbol indicates that the input is active when it is low (OV nominal). The absence of a circle at an input means that input is logically active when it is high (+5V nominal). The presence or absence of a circle at a symbol output has similar meanings for the active level of that output. Usually, all logic symbols are drawn with inputs on the left and outputs on the right. Symbols for all integrated circuits used are shown in the IC data contained in this section.

4.5   INTEGRATED CIRCUITS

Table 5-1 summarizes all integrated circuits used in the 1340A. All of the ICs listed were used at some point in the manufacturing process, but all will not be found in current production machines. Further information is contained in the following several pages. IC data on the following pages is arranged the same order as listed in Table 5-1, so the table can be used as an index when looking for data on a particular IC.

Table 4-1. Integrated Circuits

Digital:

Type	Description	Diablo Part No.
7400	TTL Quad 2-Input NAND Gate	10134
7402	TTL Quad 2-Input NOR Gate	10135
7404	TTL Hex Inverter	10136
74LS04	TTL Hex Inverter, Low Power Schottky	10209-01
7406	TTL Hex Inverter Buffer/Driver	10460
7408	TTL Quad 2-Input AND Gate	10119
7410	TTL Triple 3-Input NAND Gate	10133
7411	TTL Triple 3-Input AND Gate	10301
7414	TTL Hex Schmitt-trigger Inverter	10299-01
7416	Hex Inverter Buffer/Driver with Open Collector, High Voltage	10390
7420	TTL Dual 4-Input NAND Gate	10125
7426	TTL Quad 2-Input NAND High-Voltage Interface Gate	10120
7432	TTL Quad 2-Input OR Gate	10302
74LS32	TTL Quad 2-Input Positive OR Gates, Low Power Schottky	13082
74LS42	TTL BCD-To-Decimal Decoder, Low Power Schottky	13083
7451	TTL Dual AND-OR-INVERT Gate	10280
7453	TTL 4-wide Expandable AND-OR-INVERT Gate	10192
74LS54	TTL Expandable 4-Wide 2-Input AND – OR Invert Gates	42408-01
74LS74	TTL Dual D Flip-flop, Low Power Schottky	13085
74LS83	TTL 4-Bit Binary Full Adder, Low Power Schottky	13086
7486	TTL Quad 2-Input Exclusive OR Gate	10303
3101A/ 74S289	TTL 16 x 4-Bit RAM, Open Collector Schottky	13088
74107	TTL Dual J-K Master-Slave Flip-flop	10305
74LS107	TTL Dual J-K Master-Slave Flip-flop, Low Power Schottky	13089
74LS155	TTL Dual 2:4 Decoder, Low Power Schottky	13090
74161	TTL 4-Bit Synchronous Binary Counter	10335
74LS161	TTL Synchronous 4-Bit Counter, Low Power Schottky	13091
74LS170	TTL 4 x 4-Bit RAM, Low Power Schottky	13092
74LS174	TTL Hex D Latch, Low Power Schottky	13093
74LS123	TTL Dual One-Shot with Schmitt-Trigger Inputs, Low Power Schottky	42313-01
74LS259	TTL 8-Bit Addressable Latch, Low Power Schottky	13094
74298	TTL Quad 2-Input Multiplexer/Register	10196
74367	TTL Hex Bus Driver, Three-State	10197
74LS367	TTL Hex Bus Driver, Three-State, Low Power Schottky	13096
8080A	MOS 8-Bit Microprocessing Unit	42338
8205	TTL 3-Line to 8-Line Decoder	42355
8212	TTL 8-Bit I/O Port, Schottky	42337
8216	TTL 4-Bit Bi-directional Bus Driver	42339
8224	TTL Clock Generator/Driver, Schottky	10215
8228	TTL Bus Driver/System Controller, Schottky	42331

Table 4-1. Integrated Circuits (Continued)

Type	Description	Diablo Part No.
8251	MOS USART, Programmable Communications Interface	42336
8255	Universal Communication Interface	42407-01

Interface:

Type	Description	Diablo Part No.
75150P	Dual Line Driver	10353
75154	Quad Line Receiver	10354

Linear:

Type	Description	Diablo Part No.
LM319	Dual High-Speed Voltage Comparator	10168
LM320H-5	Voltage Regulator, 3-Terminal	42155-05
LM320H-12	Voltage Regulator, 3-Terminal	42155-12
LM320T-5	Voltage Regulator, 3-Terminal Negative	42152-05
LM340T-12	Voltage Regulator, 3-Terminal Positive	10284-03
LM341P-12	Voltage Regulator, 3-Terminal Positive	42154-12
LM723CD	Voltage Regulator	10321
LM733C	Differential Video Amplifier	10124
MC174SCP1	Op Amp, High Slew Rate	10167
72747	Dual Op Amp, General Purpose	10165
72747	Dual Op Amp, Selected	13072
72748	Op Amp	10166

Memories:

Type	Description	Diablo Part No.
2111A-4	MOS 1024-Bit, 256 x 4 RAM (450 ns)	42334-11
82S115	TTL 512 x 8-Bit pROM, Three State	
8316A	TTL 2K x 8-Bit ROM, Three-State	
8708	MOS 1K x 8-Bit EROM, Three-State	42329
NOTE:	Any Diablo Part numbers given here are for the "raw" (unprogrammed) IC. When a ROM contains a program or data, it is assigned a new part number reflecting the program or data it contains.	

Miscellaneous/Special Purpose:

Type	Description	Diablo Part No.
MCT2	Phototransistor Opto-Isolator	42190-01
8041	Quad FET	10190
1408L-6	Digital-to-Analog Convertor	13060
	Resistor Netowrk, 1K (15 resistors)	10239-01
	Resistor Network, 1K (13 resistors)	10761
	Resistor Network, 10K (8 resistors)	13044

TTL Quad 2-Input NAND Gate   Part No. 10134   Type 7400
TTL Quad 2-Input NAND Gate, Low Power Schottky   Part No. 13077   Type 74LS00
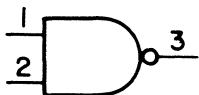
Logic Symbol   Alternate Symbol   Truth Table

A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

VCC-14, GND-7

Loading:
    Inputs   1 Unit Load (.2 for 74LS00)
    Outputs   10 Unit Loads (5 for 74LS00)

TTL Quad 2-Input NOR Gate   Part No. 10135   Type 7402

Logic Symbol   Alternate Symbol   Truth Table

A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

VCC-14, GND-7

Loading
    Inputs   1 Unit Load
    Outputs   10 Unit Loads
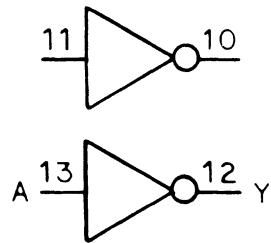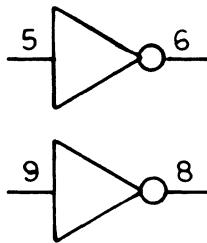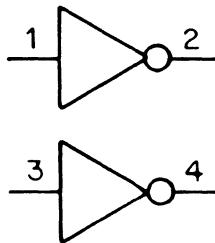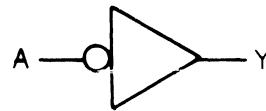
TTL Hex Inverter	Part No. 10136	Type 7404
TTL Hex Inverter, Low Power	Part No. 10389	Type 74L04
TTL Hex Inverter, Low Power Schottky	Part No. 10209	Type 74LS04

Logic Symbol   Alternate Symbol

VCC-14, GND-7

Loading:
    Inputs   1 Unit Load (.1 for 74L04, .2 for 74LS04)
    Outputs   10 Unit Loads (2 for 74L04, 5 for 74LS04)
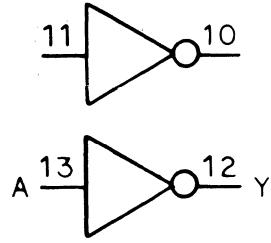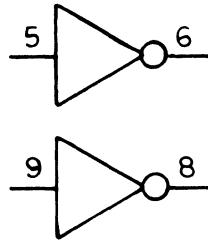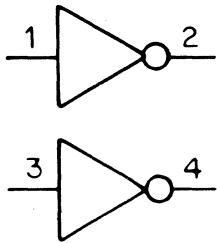
TTL Hex Inverter Buffer/Driver   Part No. 10460   Type 7406
   These drivers have high-voltage (up to 30V) open-collector outputs for interfacing with high-level circuits or for driving high-current loads.
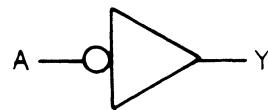
Logic Symbol   Alternate Symbol

VCC-14, GND-7

Loading:
    Inputs   1 Unit Load
    Outputs   25 Unit Loads

TTL Quad 2-Input AND Gate   Part No. 10119   Type 7408
TTL Quad 2-Input AND Gate, Low Power Schottky   Part No. 10210   Type 74LS08

Logic   Symbol   Truth Table

A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

VCC-14, GND-7

Loading:
     Inputs   1 Unit Load (.2 for 74LS08)
     Outputs   10 Unit Loads (5 for 74LS08)

TTL Triple 3-Input NAND Gate   Part No. 10133   Type 7410
TTL Triple 3-Input NAND Gate, Low Power Schottky   Part No. 13080   Type 74LS10
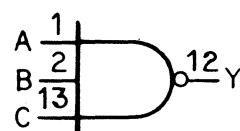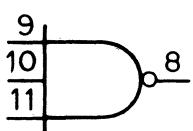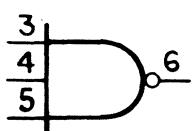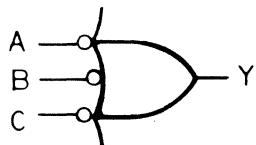
Logic Symbol   Truth Table

A	B	C	Y
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

VCC-14, GND-7

Alternate Symbol
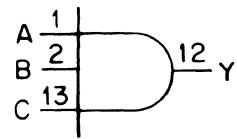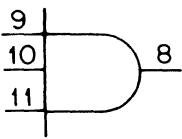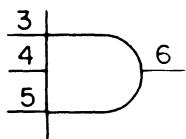
Loading:
     Inputs   1 Unit Load (.2 for 74LS10)
     Outputs   10 Unit Loads (5 for 74LS10)

TTL Triple 3-Input AND Gate   Part No. 10301   Type 7411
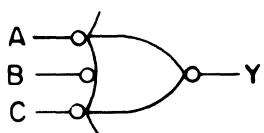
Logic Symbol

VCC-14, GND-7

Alternate Symbol

Loading:
- Inputs   1 Unit Load
- Outputs   10 Unit Loads

Truth Table

A	B	C	Y
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H
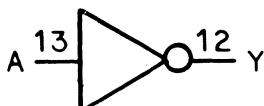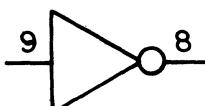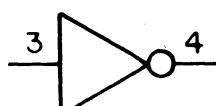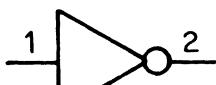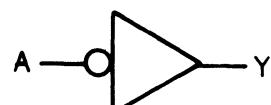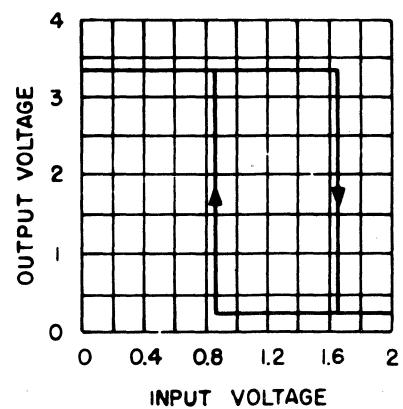
TTL Hex Schmitt-trigger Inverter   Part No. 10299-01   Type 7414

Logically, these gates act like ordinary inverters but because of the Schmitt action, each gate has different input threshold levels for positive- and negative-going signals. The hysteresis, which is the difference between the two levels, is typically 800 mV.

Logic Symbol

VCC-14, GND-7

Alternate Symbol

Waveforms

Loading:
- Inputs   .75 Unit Load
- Outputs   10 Unit Loads
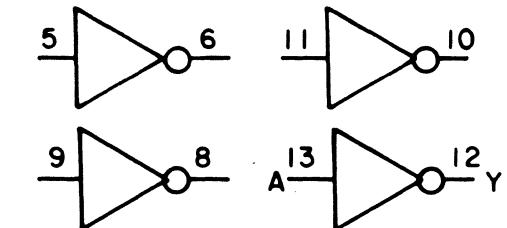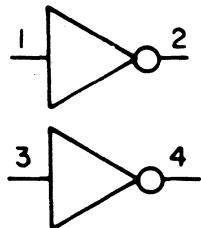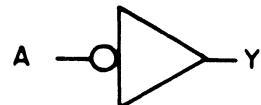
TTL Hex Inverter Buffer/Driver Part No. 10390 Type 7416

These drivers have high-voltage (up to 15V) open-collector outputs for interfacing with high-level circuits or for driving high current loads.

Logic Symbol

Alternate Symbol
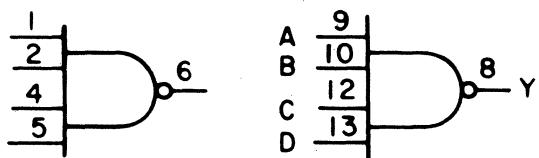
Loading:
Inputs   1 Unit Load
Outputs   25 Unit Loads

TTL Dual 4-Input NAND Gate Part No. 10125 Type 7420
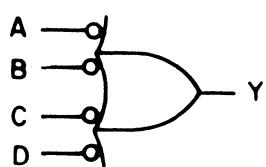
Logic Symbol

VCC-14, GND-7. Pins 3 & 11 not used.

Alternate Symbol

Truth Table
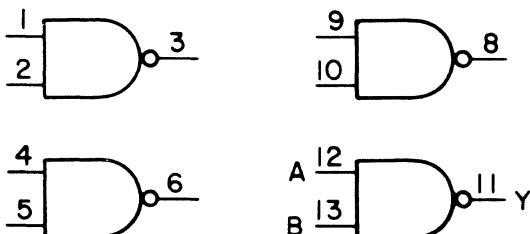
A	B	C	D	Y
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	H
L	H	L	H	H
L	H	H	L	H
L	H	H	H	H
H	L	L	L	H
H	L	L	H	H
H	L	H	L	H
H	L	H	H	H
H	H	L	L	H
H	H	L	H	H
H	H	H	L	H
H	H	H	H	L

Loading:
Inputs   1 Unit Load
Outputs   10 Unit Loads

TTL Quad 2-Input NAND High-Voltage Interface Gate   Part No. 10120   Type 7426

These gates have high-voltage (up to 15V) open-collector outputs for interfacing with high-level circuits.

Logic Symbol

VCC-14, GND-7

Alternate Symbol

Truth Table

A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

Loading:

     Inputs   1 Unit Load

     Outputs   10 Unit Loads

TTL Quad 2-Input OR Gate   Part No. 10302   Type 7432
TTL Quad 2-Input OR Gate, Low Power Schottky   Part No. 13082   Type 74LS32
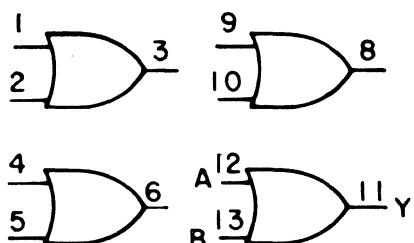
Logic Symbol

VCC-14, GND-7

Alternate Symbol

Truth Table

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

Loading:

     Inputs   1 Unit Load (.25 for 74LS32)

     Outputs   10 Unit Loads (5 for 74LS32)
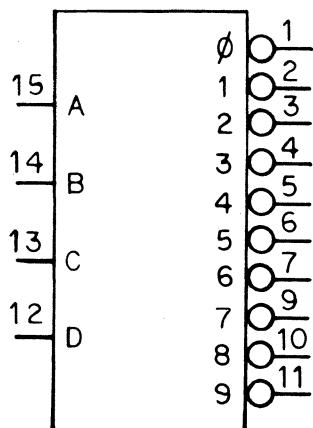
TTL BCD-To-Decimal Decoder   Part No. 10146   Type 7442A
TTL BCD-To-Decimal Decoder, Low Power Schottky   Part No. 13083   Type 74LS42

Logic Symbol

VCC-16, GND-8

A1-A8 = Binary address input
0-9 = Decimal output

Loading:
Inputs   1 Unit Load (.25 for 74LS42)
Outputs   10 Unit Loads (5 for 74LS42)

Truth Table

D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

TTL Dual AND-OR-INVERT Gate   Part No. 10280   Type 7451

Logic Symbol

VCC — 14, GND — 7

(Make no connections to pins 11 and 12.)

Loading:
Inputs   1 Unit Load
Outputs   10 Unit Loads

Truth Table

A	B	C	D	Y
L	X	L	X	H
L	X	X	L	H
X	L	X	L	H
X	L	L	X	H
H	H	X	X	L
X	X	H	H	L

$$Y = \overline{AB + CD}$$

Up to four type 7460 expander gates may be connected to the expander inputs. Both expander inputs must be used simultaneously. If the expander inputs are not used, they should be left open.

Logic Symbol

Input	Pin
A	13
B	1
C	2
D	3
E	4
F	5
G	9
H	10

Outputs: 8 Y, 11 X, 12 X̄

VCC-14, GND-7

$$Y = \overline{AB+CD+EF+GH+X}$$

Loading:
- Inputs   1 Unit Load
- Outputs   10 Unit Loads

Logic Symbol

Input	Pin
A	1
B	2
C	3
D	4
E	5
F	9
G	10
H	11
I	12
J	13

Output: 6 Y

$$Y = \overline{AB+CDE+FGH+IJ}$$

VCC-14, GND-7

Loading:
- Inputs   .25 Unit Load
- Outputs   5 Unit Loads
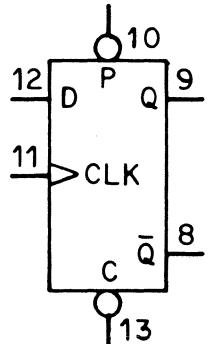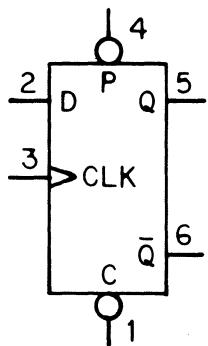
The 7474 contains two D-type edge-triggered flip-flops with direct preset and clear inputs. A low level on the preset or clear input will set or reset the flip-flop, respectively, regardless of other input conditions. When both the preset and clear are high, the logic level on D is transferred to Q on the positive-going edge of the clock.
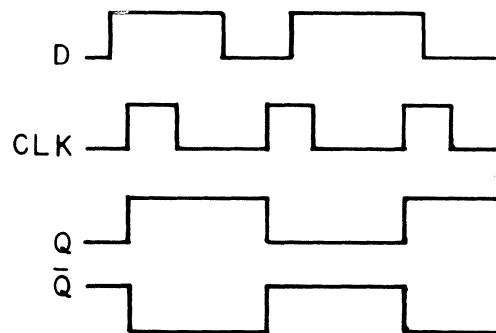
Logic Symbol

Timing Waveforms

VCC-14, GND-7

P   = Preset input
D   = Data input
CLK = Clock input
C   = Clear input
Q,Q̄ = Data outputs

Loading:

		Unit Loads 7474	Unit Loads 74LS74
Inputs	CLK	2	.5
	D	1	.25
	P	1	.5
	C	2	.75
Outputs	Q,Q̄	10	5

Truth Table

Function	Inputs Preset	Inputs Clear	Inputs Clock	Inputs D	Outputs Q	Outputs Q̄
Preset	L	H	X	X	H	L
Clear	H	L	X	X	L	H
Clear	L	L	X	X	H	H*
Set	H	H	▲	H	H	L
Reset	H	H	▲	L	L	H
Set Up	H	H	L	X	No Change	

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high level).
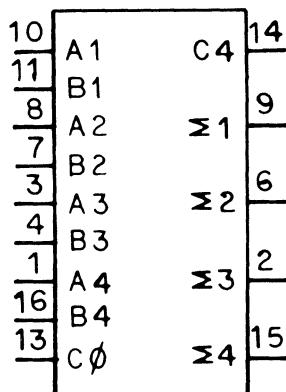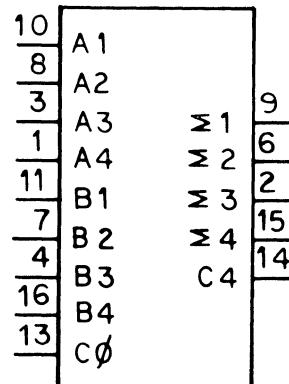
| TTL 4-Bit Binary Full Adder | Part No. 10140 | Type 7483A |
| TTL 4-Bit Binary Full Adder, Low Power Schottky | Part No. 13086 | Type 74LS83 |

This device adds two 4-bit binary numbers and a carry (Cø input). The sum (Σ) outputs are provided for each bit and the carry output (C4) is obtained from the fourth bit. Note the non-standard VCC and GND connections to this device.

Logic Symbol

NOTE: VCC-5, GND-12

Alternate Symbol

Truth Table

Inputs				Outputs When Cø=L		When C2=L	When Cø=H		When C2=H
A1 / A3	B1 / B3	A2 / A4	B1 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE: Input conditions at A1, B1, A2, B2, and Cø are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Loading:
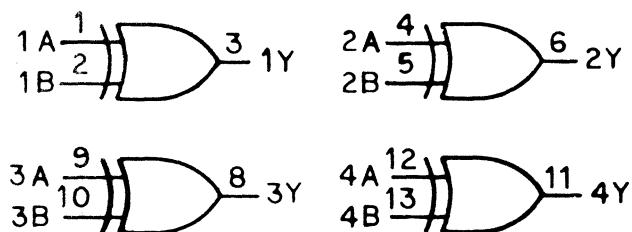
						Unit Loads	
						7483A	74LS83
Inputs	A1,	A3,	B1,	B3,	Cø	1 or 2*	1
	A2,	A4,	B2,	B4		1 or 2*	.25
Outputs	Sum 1-4					10	5
	C4					5	5

*Depending upon manufacturer.

Logic Symbol

VCC-14, GND-7

Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Loading:

Inputs	1 Unit Load
Outputs	10 Unit Loads

TTL 16 x 4-bit Random Access Memory, Open Collector   Part No. 10193   Type 3101/7489
TTL 16 x 4-bit Random Access Memory, Three-State   Part No. 10334   Type 8599/74S189
TTL 16 x 4-bit Random Access Memory, Open Collector Schottky   Part No. 13088   Type 3101A/74S289
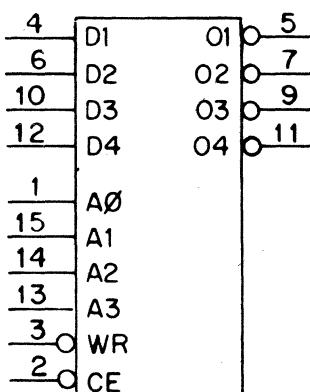
Logic Symbol

VCC-16, GND-8

Function Table

Inputs		Outputs	Function
CE	WR		
L	L	H*	Write
L	H	Complement	Read
		of stored data	
H	X	H*	Inhibit

H* = high for open-collector, high-impedance for three state. Some manufacturers specify this as indeterminate.

Loading:

Inputs (7489, 8599)	1 Unit Load
Others	.16 Unit Load (.25 ma)
Outputs	10 Unit Loads
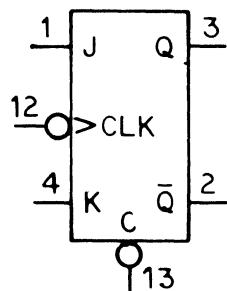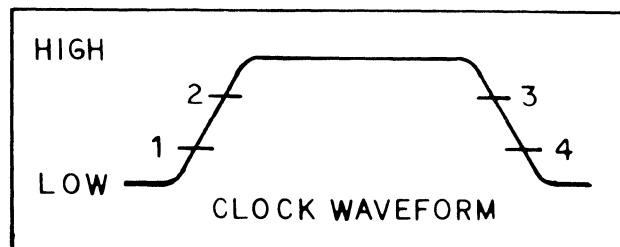
Logic Symbol
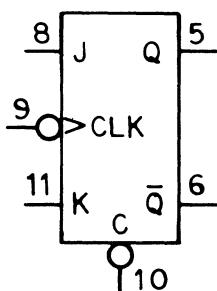
Timing Waveform

1. Isolate slave from master
2. Enable entry of data from J and K inputs to master
3. Disable entry of data from J and K inputs
4. Transfer information from master to slave

J, K = Data inputs
CLK = Clock inputs
C = Clear inputs
$Q, \bar{Q}$ = Data outputs

VCC-7, GND-14

Truth Table

(Each Flip-Flop)

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

t_n = time when clock is high (2-3)

t_{n+1} = time after clock goes low (4)

Loading:
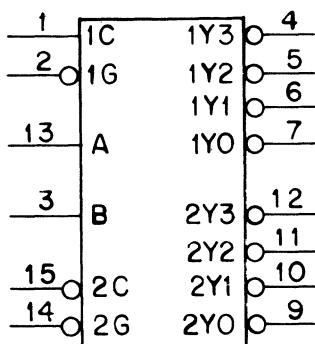
C, CLK	2 Unit Loads (.5 for 74LS107)
J, K	1 Unit Load (.25 for 74LS107)
Outputs	10 Unit Loads (5 for 74LS107)

TTL Dual 2:4 Decoder   Part No. 10194   Type 74155
TTL Dual 2:4 Decoder, Low Power Schottky   Part No. 13090   Type 74LS155

Logic Symbol   Truth Table

```
    1  ┌──────────┐  4
   ────┤1C    1Y3 ├o────
    2  │          │  5
   ──o─┤1G    1Y2 ├o────
       │          │  6
       │      1Y1 ├o────
   13  │          │  7
   ────┤A     1Y0 ├o────
       │          │
    3  │          │ 12
   ────┤B     2Y3 ├o────
       │          │ 11
       │      2Y2 ├o────
   15  │          │ 10
   ──o─┤2C    2Y1 ├o────
   14  │          │  9
   ──o─┤2G    2Y0 ├o────
       └──────────┘
```

VCC-16, GND-8

Inputs				Outputs			
Select		Gate	Data				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H
		2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

Loading:

Inputs   1 Unit Load (.25 for 74LS155)
Outputs   10 Unit Loads (5 for 74LS155)
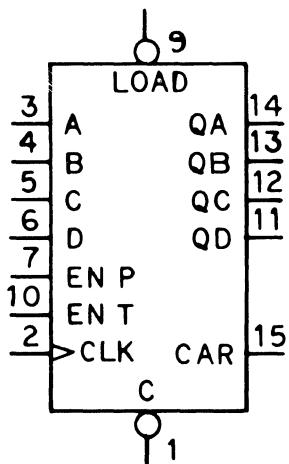
4-18

All flip-flops in this chip are clocked simultaneously, so all output changes occur simultaneously. A low on the Clear input overrides other inputs, and drives all outputs low.
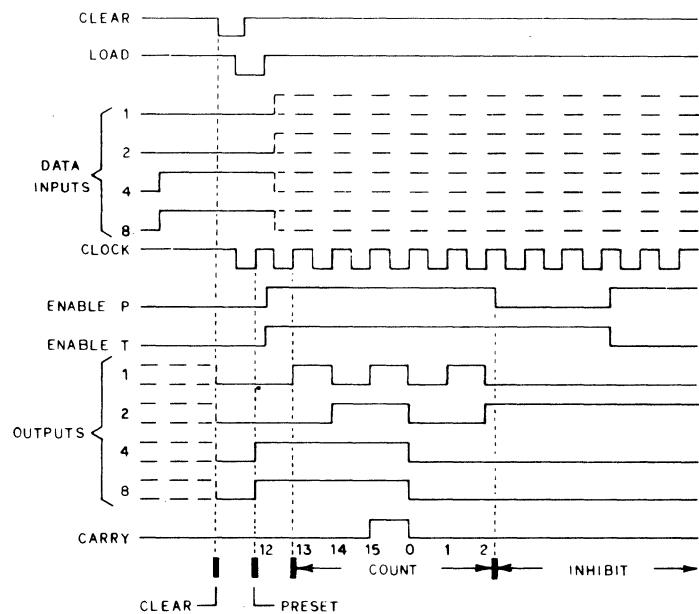
Logic Symbol

VCC-16, GND-8

Loading:

		Unit Loads	
		74161	74LS161
Inputs	LOAD	1	.5
	CLK, EN-T	2	.5
	Other	1	.25
Outputs		10	5

Timing Waveforms

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit

Truth Table

INPUTS						OUTPUTS
CLK	EN-P	EN-T	LOAD	C	A,B,C,D	
H	X	X	X	X	X	No Change
L	X*	X*	X*	X	X	No Change
X	X	X	X	L	X	All LOW
↑	X	X	L	H	DATA	Preset to A,B,C,D, input data
↑	L	L	H	H	X	No Change
↑	H	L	H	H	X	No Change
↑	L	H	H	H	X	No Change
↑	H	H	H	H	X	Count Up

*Avoid changes to inputs while CLK is low.
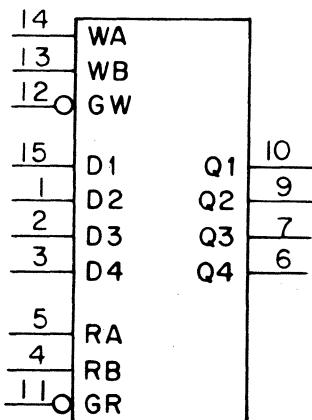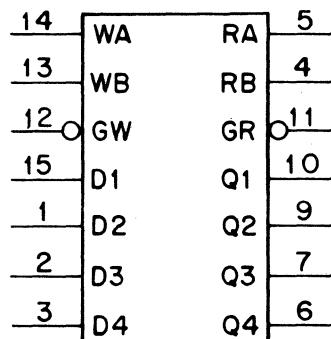
TTL 4 x 4-bit RAM   Part No. 10195   Type 74170
TTL 4 x 4-bit RAM, Low Power Schottky   Part No. 13092   Type 74LS170

This RAM has independent read and write addressing and gating, which allows simultaneous reading and writing to/from different addresses. Outputs are open-collector.

Logic Symbol

VCC-16, GND-8

Alternate Symbol

Write Function Table

Write Inputs			
GW	WB	WA	Function
L	L	L	Write Word 0
L	L	H	Write Word 1
L	H	L	Write Word 2
L	H	H	Write Word 3
H	X	X	No Change
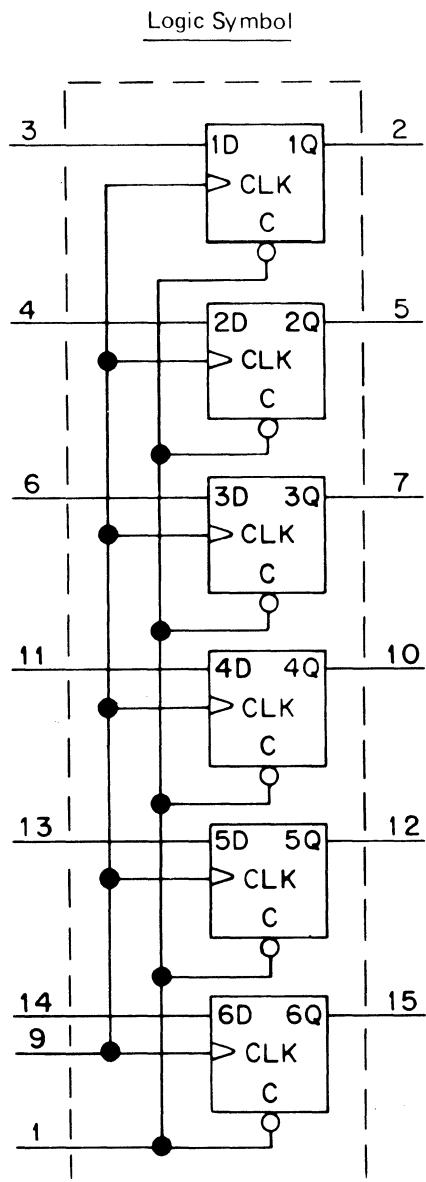
Read Function Table

Read Inputs			
GR	RB	RA	Function
L	L	L	Read Word 0
L	L	H	Read Word 1
L	H	L	Read Word 2
L	H	H	Read Word 3
H	X	X	All Outputs High

Loading:

		Unit Loads	
		74170	74LS170
Inputs	Any D,R,W	1	.25
	GR, GW	1	.5
Outputs	Q1-Q4	10	5

TTL Hex D Latch   Part No. 10336   Type 74174
TTL Hex D Latch, Low Power Schottky   Part No. 13093   Type 74LS174

All flip-flops in this chip are clocked or cleared
simultaneously. A low on the clear input overrides all
other inputs.

Logic Symbol

VCC-16, GND-8

Truth Table
(Each Flip-Flop)

INPUTS			OUTPUT
C	CLK	D	Q
L	X	X	H
H	▲	H	H
H	▲	L	L
H	L	X	No Change

H = High level
L = Low Level
X = Irrelevant
▲ = Transition from low to
    high level

1D – 6D = Data Inputs
CLK   = Clock Input
C   = Clear
1Q – 6Q = Data Outputs

Loading:

Inputs   1 Unit Load (.25 for 74LS174)
Outputs   10 Unit Loads (5 for 74LS174)

       Part No. 10145   Type 74123
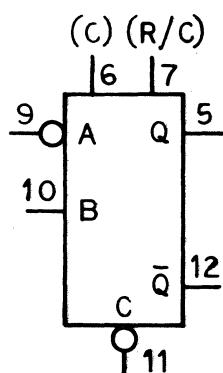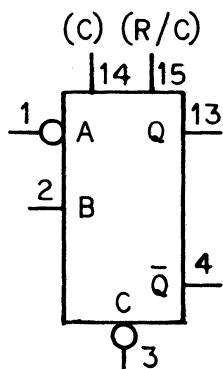
Part No. 42313-01   Type 74LS123

Either of the one-shots in this package can be triggered by a positive-going or a negative-going input, providing the other input is already in the proper state. At least one of the inputs must be removed and re-applied in order to retrigger the device. A low on the C input terminates the output pulse immediately. The length of the output pulse is dependent upon external timing components.
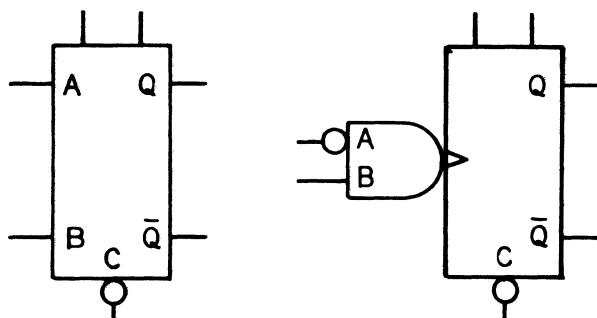
Logic Symbol

Alternate Symbols

VCC-16, GND-8

Truth Table

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↑	H	⊓	⊔
↑	L	H	⊓	⊔

Loading: 74123   74LS123

	74123	74LS123
Clear	2 Unit Loads	.25 Unit Load
Other Inputs	1 Unit Load	.25 Unit Load
Outputs	10 Unit Loads	5 Unit Loads

TTL 8-bit Addressable Latch
TTL 8-bit Addressable Latch, Low Power Schottky

Part No. 10339
Part No. 13094

Type 9334
Type 74LS259

This is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with high-active outputs. It incorporates a low-active common clear for resetting all latches, as well as a low-active enable.
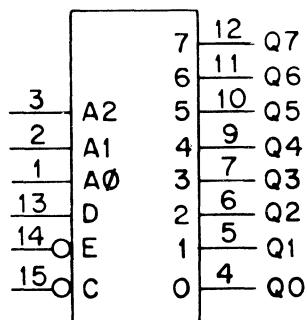
There are two modes of operation, shown in the Function Table. In the addressable latch mode, when E is LOW, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input, with all nonaddressed latches remaining in their previous states. When E is HIGH all latches

remain in their previous state and are unaffected by the data or address inputs. When operating as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while E is HIGH.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input, with all other outputs in the LOW state.

When E is HIGH and C is LOW all outputs are LOW and unaffected by the address and data inputs.
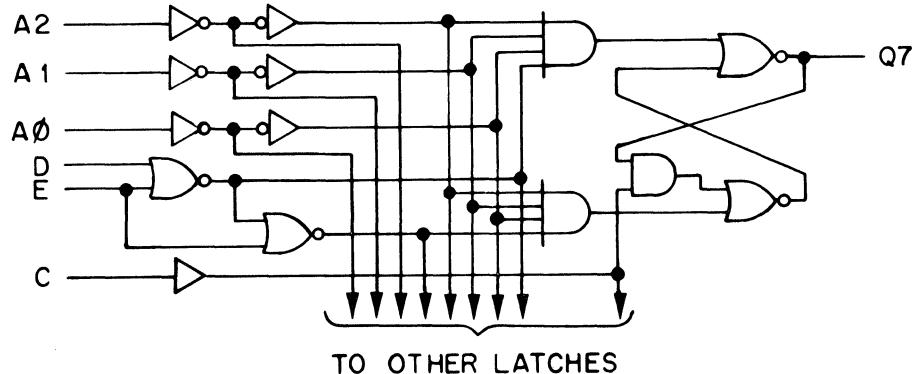
Logic Symbol

VCC-16, GND-8

Logic Diagram

ONLY ONE LATCH SHOWN FOR CLARITY

TO OTHER LATCHES

Function Table

Inputs			Outputs		
C	E	D	Addressed Latch	Others	Mode
L	L	L	L	L	} Demultiplexer
L	L	H	H	L	
L	H	X	L	L	Clear
H	L	L	L	No Change	} Addressable
H	L	H	H	No Change	} Latch
H	H	X	No Change	No Change	

Loading:

		Unit Loads	
		9334	74LS174
Inputs	E	1.5	.25
	Other	1	.25
Outputs		6	5
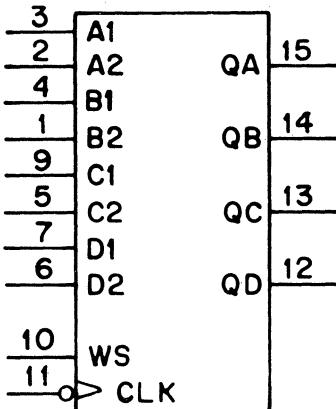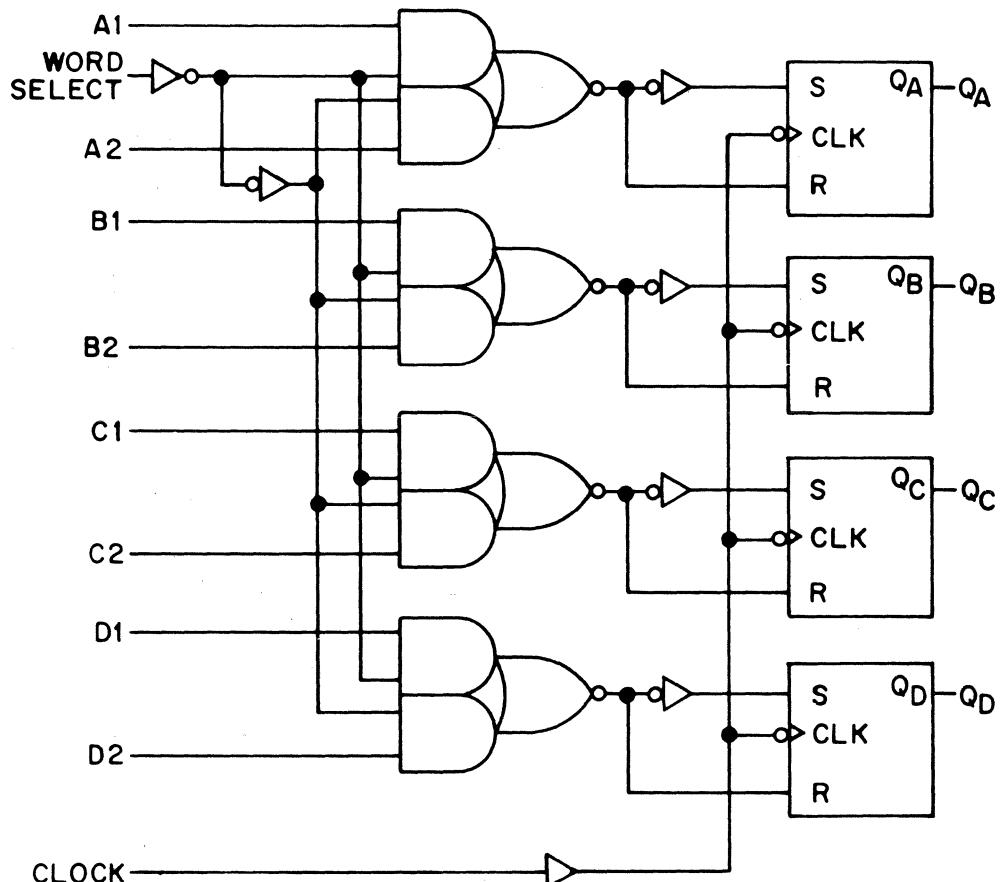
Data is stored on the negative-going edge of the CLK. With WS low, word 1 (A1, B1, C1, D1) is stored; with WS high, word 2 is stored.

Logic Symbol

VCC-16, GND-8

Logic Diagram

Loading:

	Unit Loads	
	74298	74LS298
Inputs	1	.25
Outputs	10	5
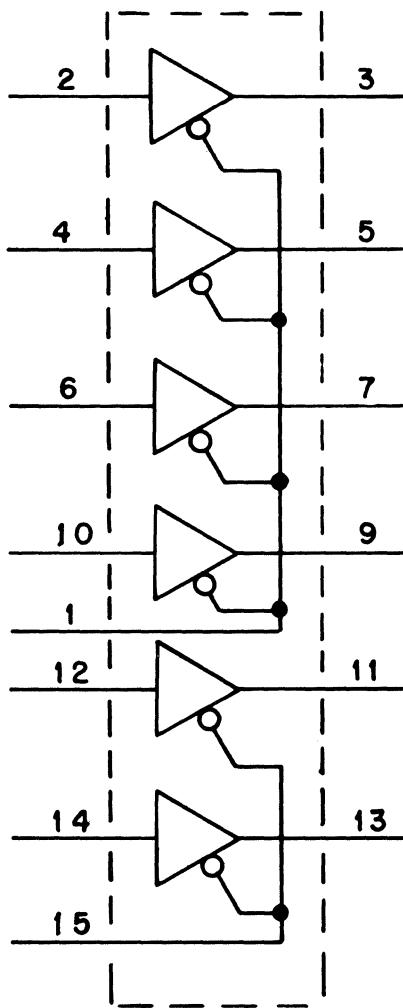
Logic Symbol

VCC-16, GND-8

Loading:

	Unit Loads	
	74367	74LS367
Inputs (Gate enabled)	1	.25
Outputs	20	10

This is a single chip 8-bit parallel microprocessor which forms a microcomputer system when interfaced with any type or speed of standard semiconductor memory up to 64K 8-bit words and an I/O device. The MPU inputs and outputs data over an 8-bit bi-directional three-state data bus (D0-D7). It addresses memory and I/O devices over a 16-bit three-state memory address bus (A0-A15). It is driven by two 12-volt non-overlapping clocks, ∅1 and ∅2. There are four input signals, INT (Interrupt), RDY (Ready), HOLD, and RST (Reset). Output signals include INTE (Interrupt Enable), DBIN (Data Bus In), WR (Write), SYNC, WAIT, and HLDA (Hold Acknowledge).

The 8080A contains a register array made up of six 16-bit registers: a Program Counter, a Stack Pointer, and four register "pairs," each made up of two 8-bit registers. One of these is the Temporary Register, called W/Z, which is used for the internal execution of instructions. The other three are working registers, called B/C, D/F, and H/L. The six general purpose registers can be used as either single 8-bit registers or 16-bit register pairs; W/Z is not program addressable.
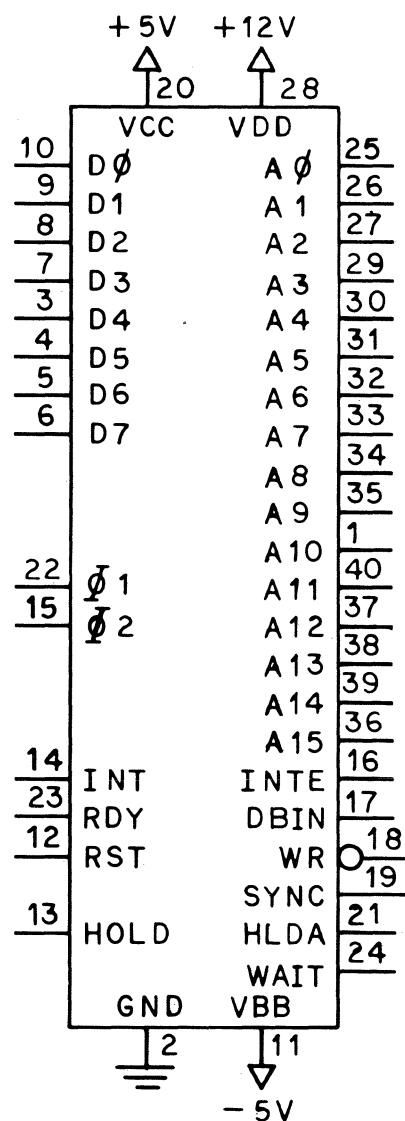
The 8080A also contains an Arithmetic and Logic Unit (ALU), containing an 8-bit accumulator (ACC), an 8-bit temporary accumulator (ACT), an 8-bit temporary register (TMP), and a 5-bit flag register. All arithmetic and logic instructions are performed in this section.

The third major part of the 8080A contains the Instruction Register, Instruction Decoder, and all timing and control logic. The last major portion is the Data Bus Buffer, a 3-state bi-directional 8-bit latch that serves to isolate the the MPU's internal data bus from the external bus.

The instruction set consists of over 100 different instructions, which provide conditional and unconditional branching, decimal and binary arithmetic, and logical, register-to-register, stack control, memory reference, and I/O instructions. Up to 256 input ports and 256 output ports can be addressed. Instructions may be either one, two, or three 8-bit bytes in length. Memory can be referenced four ways: direct, register, register indirect, and immediate. Non memory-reference instructions can be executed in 2 microseconds when a 2 MHz clock is used. The sequential program execution can be interrupted by driving the INT input high.

The 8080A uses its internal stack pointer to access external memory, allowing it to handle multiple-level priority interrupts. This also allows adequate subroutine nesting.

Logic Symbol

	+5V	+12V		
	20	28		
	VCC	VDD		
10	D∅	A∅	25	
9	D1	A1	26	
8	D2	A2	27	
7	D3	A3	29	
3	D4	A4	30	
4	D5	A5	31	
5	D6	A6	32	
6	D7	A7	33	
		A8	34	
		A9	35	
		A10	1	
22	∅1	A11	40	
15	∅2	A12	37	
		A13	38	
		A14	39	
14		A15	36	
23	INT	INTE	16	
12	RDY	DBIN	17	
	RST	WR	18/19	
13	HOLD	SYNC	21	
		HLDA	24	
		WAIT		
	GND	VBB		
	2	11		
		-5V		

Loading:

Outputs   1.2 Unit Loads

1. The first memory cycle (M1) is always an instruction fetch; the first (or only) byte, containing the op code, is fetched during this cycle.

2. If the READY input from memory is not high during T2 of each memory cycle, the processor will enter a wait state (TW) until READY is sampled as high.

3. States T4 and T5 are present, as required, for operations which are completely internal to the CPU. The contents of the internal bus during T4 and T5 are available at the data bus; this is designed for testing purposes only. An "X" denotes that the state is present, but is only used for such internal operations as instruction decoding.

4. Only register pairs rp = B (registers B and C) or rp = D (registers D and E) may be specified.

5. These states are skipped.

6. Memory read sub-cycles; an instruction or data word will be read.

7. Memory write sub-cycle.

8. The READY signal is not required during the second and third sub-cycles (M2 and M3). The HOLD signal is accepted during M2 and M3. The SYNC signal is not generated during M2 and M3. During the execution of DAD, M2 and M3 are required for an internal register-pair add; memory is not referenced.

9. The results of these arithmetic, logical or rotate instructions are not moved into the accumulator (A) until state T2 of the next instruction cycle. That is, A is loaded while the next instruction is being fetched; this overlapping of operations allows for faster processing.

10. If the value of the least significant 4-bits of the accumulator is greater than 9 or if the auxiliary carry bit is set, 6 is added to the accumulator. If the value of the most significant 4-bits of the accumulator is now greater than 9, or if the carry bit is set, 6 is added to the most significant 4-bits of the accumulator.

11. This represents the first sub-cycle (the instruction fetch) of the next instruction cycle.

12. If the condition was met, the contents of the register pair WZ are output on the address lines (A_{0-15}) instead of the contents of the program counter (PC).

13. If the condition was not met, sub-cycles M4 and M5 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

14. If the condition was not met, sub-cycles M2 and M3 are skipped; the processor instead proceeds immediately to the instruction fetch (M1) of the next instruction cycle.

15. Stack read sub-cycle.

16. Stack write sub-cycle.

17. CONDITION

		CCC
NZ	— not zero (Z = 0)	000
Z	— zero (Z = 1)	001
NC	— no carry (CY = 0)	010
C	— carry (CY = 1)	011
PO	— parity odd (P = 0)	100
PE	— parity even (P = 1)	101
P	— plus (S = 0)	110
M	— minus (S = 1)	111

18. I/O sub-cycle: the I/O port's 8-bit select code is duplicated on address lines 0-7 (A_{0-7}) and 8-15 (A_{8-15}).

19. Output sub-cycle.

20. The processor will remain idle in the halt state until an interrupt, a reset or a hold is accepted. When a hold request is accepted, the CPU enters the hold mode; after the hold mode is terminated, the processor returns to the halt state. After a reset is accepted, the processor begins execution at memory location zero. After an interrupt is accepted, the processor executes the instruction forced onto the data bus (usually a restart instruction).

SSS or DDD	Value	rp	Value
A	111	B	00
B	000	D	01
C	001	H	10
D	010	SP	11
E	011		
H	100		
L	101		

MNEMONIC	OP CODE		M1[1]					M2		
	D7 D6 D5 D4	D3 D2 D1 D0	T1	T2[2]	T3	T4	T5	T1	T2[2]	T3
MOV r1,r2	0 1 D D	D S S S	PC OUT STATUS	PC = PC +1	INST→TMP/IR	(SSS)→TMP	(TMP)→DDD			
MOV r, M	0 1 D D	D 1 1 0				x[3]		HL OUT STATUS[6]	DATA→DDD	
MOV M, r	0 1 1 1	0 S S S				(SSS)→TMP		HL OUT STATUS[7]	(TMP)→DATA BUS	
SPHL	1 1 1 1	1 0 0 1				(HL)→SP				
MVI r, data	0 0 D D	D 1 1 0				x		PC OUT STATUS[6]	B2→DDDD	
MVI M, data	0 0 1 1	0 1 1 0				x			B2→TMP	
LXI rp, data	0 0 R P	0 0 0 1				x			PC = PC + 1 B2→r1	
LDA addr	0 0 1 1	1 0 1 0				x			PC = PC + 1 B2→Z	
STA addr	0 0 1 1	0 0 1 0				x			PC = PC + 1 B2→Z	
LHLD addr	0 0 1 0	1 0 1 0				x			PC = PC + 1 B2→Z	
SHLD addr	0 0 1 0	0 0 1 0				x		PC OUT STATUS[6]	PC = PC + 1 B2→Z	
LDAX rp[4]	0 0 R P	1 0 1 0				x		rp OUT STATUS[6]	DATA→A	
STAX rp[4]	0 0 R P	0 0 1 0				x		rp OUT STATUS[7]	(A)→DATA BUS	
XCHG	1 1 1 0	1 0 1 1				(HL)←→(DE)				
ADD r	1 0 0 0	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ADD M	1 0 0 0	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA→TMP	
ADI data	1 1 0 0	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→TMP	
ADC r	1 0 0 0	1 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)+CY→A	
ADC M	1 0 0 0	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA→TMP	
ACI data	1 1 0 0	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→TMP	
SUB r	1 0 0	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)→A	
SUB M	1 0 0	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA→TMP	
SUI data	1 1 0 1	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→TMP	
SBB r	1 0 0 1	1 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)-(TMP)-CY→A	
SBB M	1 0 0 1	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA→TMP	
SBI data	1 1 0 1	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2→TMP	
INR r	0 0 D D	D 1 0 0				(DDD)→TMP (TMP) + 1→ALU	ALU→DDD			
INR M	0 0 1 1	0 1 0 0				x		HL OUT STATUS[6]	DATA→TMP (TMP)+1→ALU	
DCR r	0 0 D D	D 1 0 1				(DDD)→TMP (TMP)+1→ALU	ALU→DDD			
DCR M	0 0 1 1	0 1 0 1				x		HL OUT STATUS[6]	DATA→TMP (TMP)-1→ALU	
INX rp	0 0 R P	0 0 1 1				(RP) + 1→RP				
DCX rp	0 0 R P	1 0 1 1				(RP) - 1→RP				
DAD rp[8]	0 0 R P	1 0 0 1				x		(rl)→ACT	(L)→TMP (ACT)+(TMP)→ALU	ALU→L, CY
DAA	0 0 1 0	0 1 1 1				DAA→A, FLAGS[10]				
ANA r	1 0 1 0	0 S S S				(SSS)→TMP (A)→ACT		[9]	(ACT)+(TMP)→A	
ANA M	1 0 1 0	0 1 1 0	PC OUT STATUS	PC = PC +1	INST→TMP/IR	(A)→ACT		HL OUT STATUS[6]	DATA→TMP	

M3			M4			M5				
T1	T2[2]	T3	T1	T2[2]	T3	T1	T2[2]	T3	T4	T5
HL OUT STATUS[7]	(TMP) → DATA BUS									
PC OUT STATUS[6]	PC = PC + 1 B3 → rh									
	PC = PC + 1 B3 → W		WZ OUT STATUS[6]	DATA ──── A						
	PC = PC + 1 B3 → W		WZ OUT STATUS[7]	(A) ──── DATA BUS						
	PC = PC + 1 B3 → W		WZ OUT STATUS[6]	DATA ──── L		WZ OUT STATUS[6]	DATA → H			
PC OUT STATUS[6]	PC = PC + 1 B3 → W		WZ OUT STATUS[7]	(L) ──── DATA BUS WZ = WZ + 1		WZ OUT STATUS[7]	(H) → DATA BUS			
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)→A									
[9]	(ACT)+(TMP)+CY→A									
[9]	(ACT)+(TMP)+CY→A									
[9]	(ACT)-(TMP)→A									
[9]	(ACT)-(TMP)→A									
[9]	(ACT)-(TMP)-CY→A									
[9]	(ACT)-(TMP)-CY→A									
HL OUT STATUS[7]	ALU → DATA BUS									
HL OUT STATUS[7]	ALU → DATA BUS									
(rh)→ACT	(H)→TMP (ACT)+(TMP)+CY→ALU	ALU→H, CY								
[9]	(ACT)+(TMP)→A									

MNEMONIC	OP CODE		M1[1]					M2		
	D7 D6 D5 D4	D3 D2 D1 D0	T1	T2[2]	T3	T4	T5	T1	T2[2]	T3
ANI data	1 1 1 0	0 1 1 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
XRA r	1 0 1 0	1 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)+(TPM)→A	
XRA M	1 0 1 0	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
XRI data	1 1 1 0	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
ORA r	1 0 1 1	0 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)+(TMP)→A	
ORA M	1 0 1 1	0 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
ORI data	1 1 1 1	0 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
CMP r	1 0 1 1	1 S S S				(A)→ACT (SSS)→TMP		[9]	(ACT)-(TMP), FLAGS	
CMP M	1 0 1 1	1 1 1 0				(A)→ACT		HL OUT STATUS[6]	DATA	→TMP
CPI data	1 1 1 1	1 1 1 0				(A)→ACT		PC OUT STATUS[6]	PC = PC + 1 B2	→TMP
RLC	0 0 0 0	0 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RRC	0 0 0 0	1 1 1 1				(A)→ALU ROTATE		[9]	ALU→A, CY	
RAL	0 0 0 1	0 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
RAR	0 0 0 1	1 1 1 1				(A), CY→ALU ROTATE		[9]	ALU→A, CY	
CMA	0 0 1 0	1 1 1 1				(Ā)→A				
CMC	0 0 1 1	1 1 1 1				C̄Y→CY				
STC	0 0 1 1	0 1 1 1				1→CY				
JMP addr	1 1 0 0	0 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2	→Z
J cond addr[17]	1 1 C C	C 0 1 0				JUDGE CONDITION		PC OUT STATUS[6]	PC = PC + 1 B2	→Z
CALL addr	1 1 0 0	1 1 0 1				SP = SP - 1		PC OUT STATUS[6]	PC = PC + 1 B2	→Z
C cond addr[17]	1 1 C C	C 1 0 0				JUDGE CONDITION IF TRUE, SP = SP - 1		PC OUT STATUS[6]	PC = PC + 1 B2	→Z
RET	1 1 0 0	1 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA	→Z
R cond addr[17]	1 1 C C	C 0 0 0			INST→TMP/IR	JUDGE CONDITION[14]		SP OUT STATUS[15]	SP = SP + 1 DATA	→Z
RST n	1 1 N N	N 1 1 1			φ→W INST→TMP/IR	SP = SP - 1		SP OUT STATUS[16]	SP = SP - 1 (PCH)	→DATA BUS
PCHL	1 1 1 0	1 0 0 1			INST→TMP/IR	(HL) ————→ PC				
PUSH rp	1 1 R P	0 1 0 1				SP = SP - 1		SP OUT STATUS[16]	SP = SP - 1 (rh)	→DATA BUS
PUSH PSW	1 1 1 1	0 1 0 1				SP = SP - 1		SP OUT STATUS[16]	SP = SP - 1 (A)	→DATA BUS
POP rp	1 1 R P	0 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA	→r1
POP PSW	1 1 1 1	0 0 0 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA	→FLAGS
XTHL	1 1 1 0	0 0 1 1				X		SP OUT STATUS[15]	SP = SP + 1 DATA	→Z
IN port	1 1 0 1	1 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2	→Z, W
OUT port	1 1 0 1	0 0 1 1				X		PC OUT STATUS[6]	PC = PC + 1 B2	→Z, W
EI	1 1 1 1	1 0 1 1				SET INTE F/F				
DI	1 1 1 1	0 0 1 1				RESET INTE F/F				
HLT	0 1 1 1	0 1 1 0				X		PC OUT STATUS	HALT MODE[20]	
NOP	0 0 0 0	0 0 0 0	PC OUT STATUS	PC = PC + 1	INST→TMP/IR	X				

M3			M4			M5						
T1	T2[2]	T3	T1	T2[2]	T3	T1	T2[2]	T3	T4	T5		
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)+(TMP)→A											
[9]	(ACT)-(TMP); FLAGS											
[9]	(ACT)-(TMP); FLAGS											
PC OUT STATUS[6]	PC = PC + 1 B3 →W										WZ OUT STATUS[11]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1 B3 →W										WZ OUT STATUS[11,12]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1 B3 →W		SP OUT STATUS[16]	(PCH) ——►DATA BUS SP = SP - 1		SP OUT STATUS[16]	(PCL)—►DATA BUS				WZ OUT STATUS[11]	(WZ) + 1 → PC
PC OUT STATUS[6]	PC = PC + 1 B3 →W[13]		SP OUT STATUS[16]	(PCH) ——►DATA BUS SP = SP - 1		SP OUT STATUS[16]	(PCL)—►DATA BUS				WZ OUT STATUS[11,12]	(WZ) + 1 → PC
SP OUT STATUS[15]	SP = SP + 1 DATA →W										WZ OUT STATUS[11]	(WZ) + 1 → PC
SP OUT STATUS[15]	SP = SP + 1 DATA →W										WZ OUT STATUS[11,12]	(WZ) + 1 → PC
SP OUT STATUS[16]	(TMP = 00NNN000) ——►Z (PCL)——►DATA BUS										WZ OUT STATUS[11]	(WZ) + 1 → PC
SP OUT STATUS[16]	(rl) ——►DATA BUS											
SP OUT STATUS[16]	FLAGS ——►DATA BUS											
SP OUT STATUS[15]	SP = SP + 1 DATA ——►rh											
SP OUT STATUS[15]	SP = SP + 1 DATA ——►A											
SP OUT STATUS[15]	DATA →W		SP OUT STATUS[16]	(H) ——————►DATA BUS		SP OUT STATUS[16]	(L) ——►DATA BUS		(WZ) ——►HL			
WZ OUT STATUS[18]	DATA ——►A											
WZ OUT STATUS[18]	(A) ——►DATA BUS											

Mnemonic	Description	D7	D6	D5	D4	D3	D2	D1	D0	Clock[2] Cycles
MOV r1,r2	Move register to register	0	1	D	D	D	S	S	S	5
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11

Mnemonic	Description	D7	D6	D5	D4	D3	D2	D1	D0	Clock[2] Cycles
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart (3)	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4

Notes:

1)

	Register							
	A	B	C	D	E	H	L	Mem
DDD or SSS	111	000	001	010	011	100	101	110

2) Two possible cycle times (11/17 or 5/11) indicate instruction cycles dependent on condition flags.

3) After a Restart instruction, the next instruction is fetched from memory at the address eight times AAA.

Logic Symbol

```
        1   ┌─────────┐
    ────────┤ A∅    0∅├o── 15
        2   │         │o── 14
    ────────┤ A1    01│
        3   │       02│o── 13
    ────────┤ A2      │o── 12
            │       03│o── 11
        4   │       04│
    ───o────┤ E1    05│o── 10
        5   │         │o── 9
    ───o────┤ E2    06│o── 7
        6   │       07│
    ────────┤ E3      │
            └─────────┘
```

VCC-16, GND-8
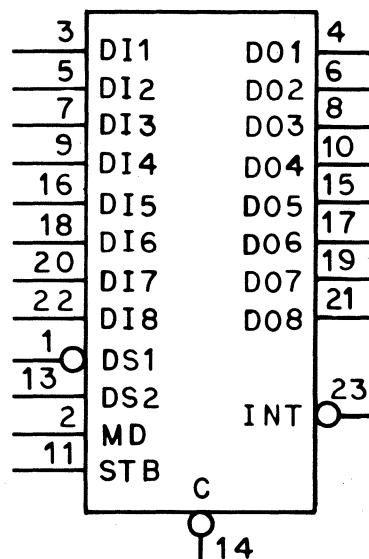
Truth Table

Inputs						Outputs							
A0	A1	A2	E1	E2	E3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H
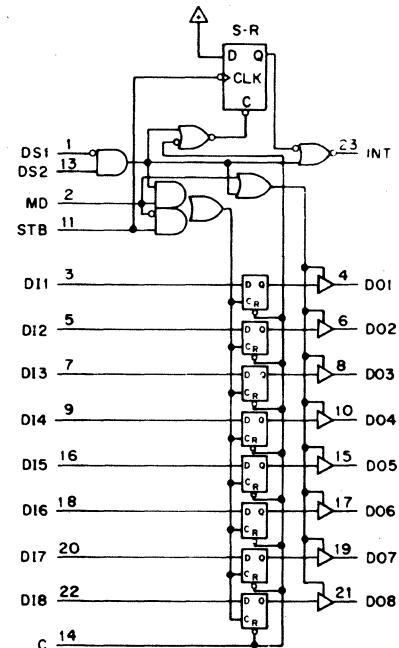
Loading:	8205	25LS138
Inputs	.16 Unit Load	.25 Unit Load
Outputs	6 Unit Loads	5 Unit Loads

4-33

This device contains an 8-bit latch with three-state output buffers and logic to allow independent control of input and output. It also has an internal Service Request flip-flop for generating interrupts for the MPU.

Logic Symbol

VCC-24, GND-12

Logic Diagram

Function Table
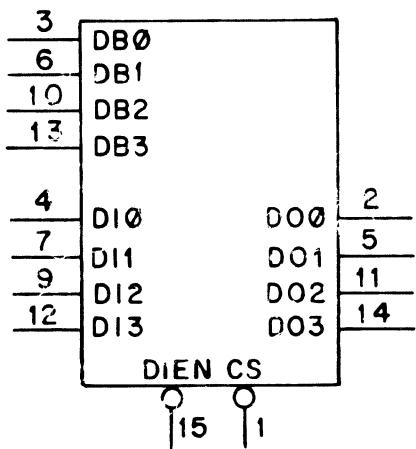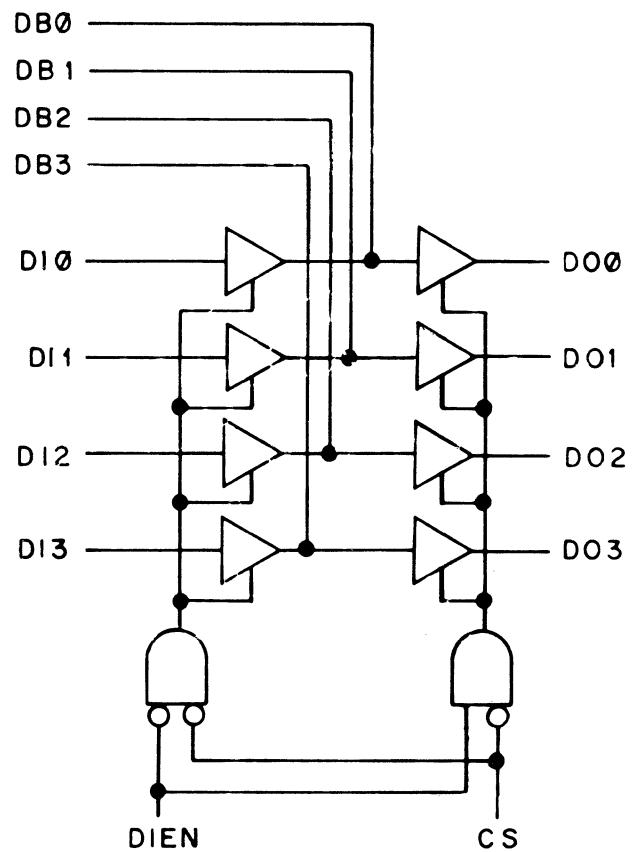
| Mode | Inputs | | | | Outputs | Internal |
	MD	DS1=L DS2=H	STB	DI1-8	DO1-8	Latches
Input	L	No	L	X	Hi-Z	No Change
	L	No	H	L	Hi-Z	Load L
	L	No	H	H	Hi-Z	Load H
	L	Yes	L	X	Previous H/L	No Change
	L	Yes	H	H	H	Load H
	L	Yes	H	L	L	Load L
Output	H	No	X	X	Previous H/L	Read
	H	Yes	X	H	H	Load H
	H	Yes	X	L	L	Load L

Loading:

Inputs
  C, DS2, DI1-8, STB   .16 Unit Load
  MD   .46 Unit Load
  DS1   .62 Unit Load

Outputs   9 Unit Loads

Interrupt Generation

| Inputs | | | Output | |
DS1=L DS2=H	C	STB	S-R ff	INT
No	L	L	L	H
No	H	L	No Change	
No	H	↓	H	L
Yes	X	X	X	L

Logic Symbol

Logic Diagram

VCC-16, GND-8

Loading:
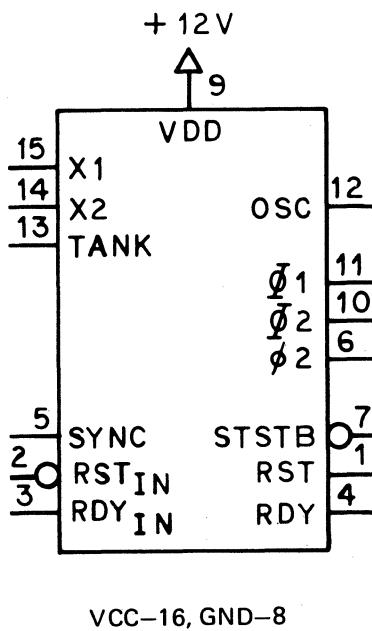
Inputs
CS,DIEN   .31 Unit Load
DI,DB   .16 Unit Load

Outputs
DB   33 Unit Loads
DO   9 Unit Loads

The device provides the 12 volt, non-overlapping clocks required by the 8080 MPU. The frequency of the output signals is determined by an external crystal (crystal frequency = 9 times clock frequency). It also provides power-up Reset and Status Strobe functions.

Logic Symbol

+12V

9

VDD

15 X1
14 X2   OSC 12
13 TANK

ϕ1 11
ϕ2 10
ϕ2 6

5 SYNC   STSTB 7
2 RST$_{IN}$ RST 1
3 RDY$_{IN}$ RDY 4

VCC—16, GND—8

Clock Generator

The clock generator provides the 12 volt ϕ1 and ϕ2 signals needed by the 8080, plus a ϕ2 TTL signal for related logic.

Status Strobe

The SYNC signal from the 8080 is used to generate STSTB (low active) at the earliest possible moment that the 8080 status data is stable on the MPU data bus (at the beginning of each 8080 machine cycle). This STSTB signal is used by the 8228 System Controller IC. STSTB is also developed when RST is produced.

Reset

A pulse is developed automatically at turn-on when power reaches a minimum predetermined value. A level is produced when the RST-IN input is driven low.
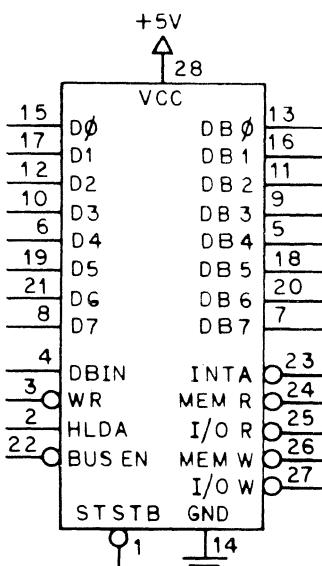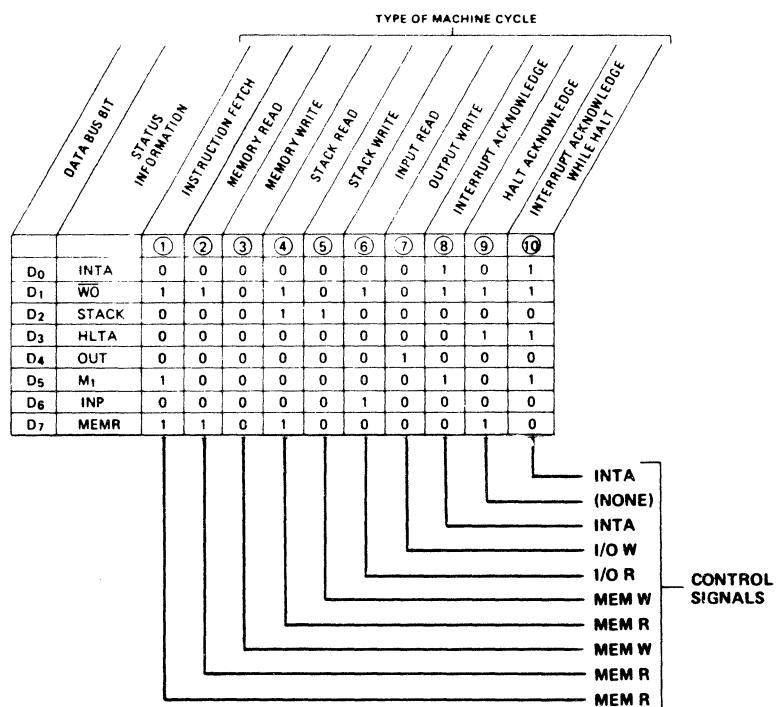
Ready

The RDY input to the 8080 must meet certain critical timing requirements. An asynchronous signal can be applied to the 8224 on the RDY-IN input, and the RDY output of the 8224 will be synchronized properly with the 8080.

Loading:

Inputs   .16 Unit Load
Outputs
  RDY,RST,STSTB   1.5 Unit Loads
  ϕ2,OSC   9 Unit Loads

This is a combination bi-directional 8-bit bus driver and system controller for use with the 8080 MPU.
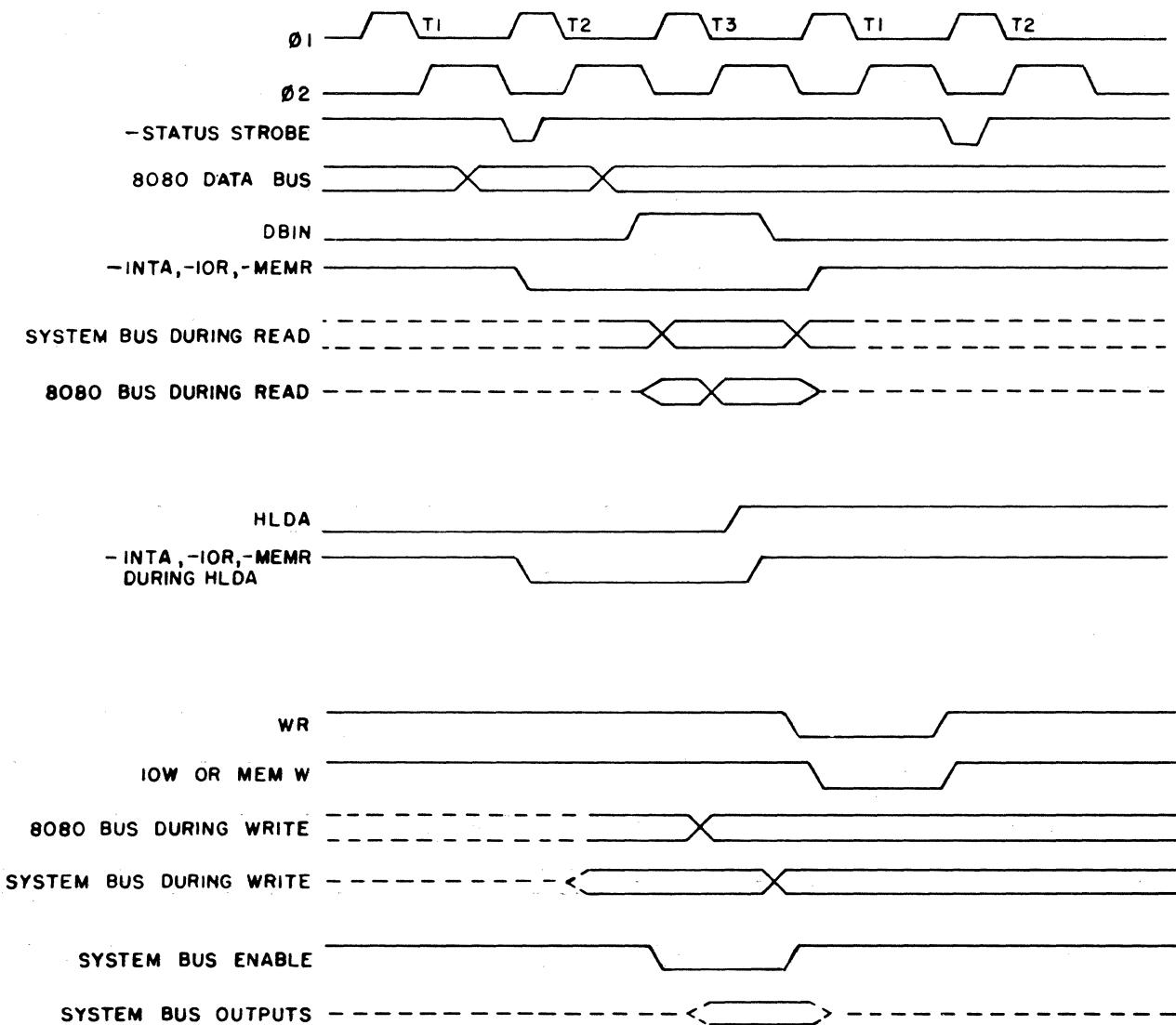
Logic Symbol

Status Word Chart

DATA BUS BIT	STATUS INFORMATION	① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE	⑨ HALT ACKNOWLEDGE	⑩ INTERRUPT ACKNOWLEDGE WHILE HALT
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

CONTROL SIGNALS:
- INTA
- (NONE)
- INTA
- I/O W
- I/O R
- MEM W
- MEM R
- MEM W
- MEM R
- MEM R

Bus Driver

When driving into the 8080 MPU, this device provides a minimum of +3.6 volts, well above the +3.3 volts required by the 8080. On 8080 output, this device provides 10 ma of drive current, as opposed to the 8080's 1.9 ma. The direction of data flow on the bus is controlled by the System Controller portion of this IC. The BUS EN input turns the bus driver on and off; when BUS EN is high, the bus outputs are in the three-state high-impedance condition.

System Controller

At the beginning of each 8080 machine cycle, the status information from the 8080 is loaded into a 6-bit latch inside the 8228. The STSTB signal from the 8224 IC strobes this latch. The outputs of this latch are then gated by the DBIN, WR, and HLDA outputs from the 8080 to produce the system control outputs MEM R, MEM W, I/O R, I/O W, and INTA. Interrupt Acknowledge (INTA) is normally used to gate instruction data from the peripheral circuitry onto the data bus after the MPU has been interrupted. A special feature of this IC allows an RST7 (Restart 7) instruction to be gated into the MPU automatically whenever the MPU is interrupted. This is accomplished by connecting the INTA output to +12 volts through a 1K resistor.

Type 8228
Timing Waveforms

Ø1

Ø2

−STATUS STROBE

8080 DATA BUS

DBIN

−INTA,−IOR,−MEMR

SYSTEM BUS DURING READ

8080 BUS DURING READ

HLDA

−INTA,−IOR,−MEMR
DURING HLDA

WR

IOW OR MEM W

8080 BUS DURING WRITE

SYSTEM BUS DURING WRITE

SYSTEM BUS ENABLE

SYSTEM BUS OUTPUTS

Loading:
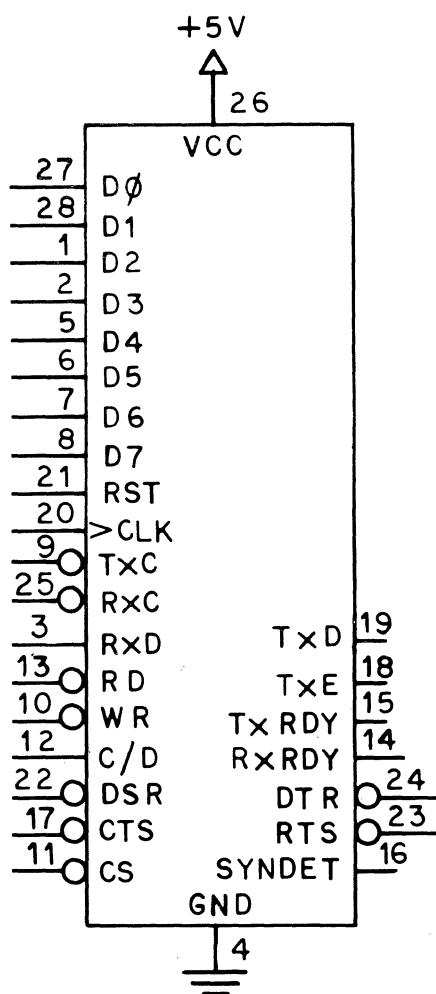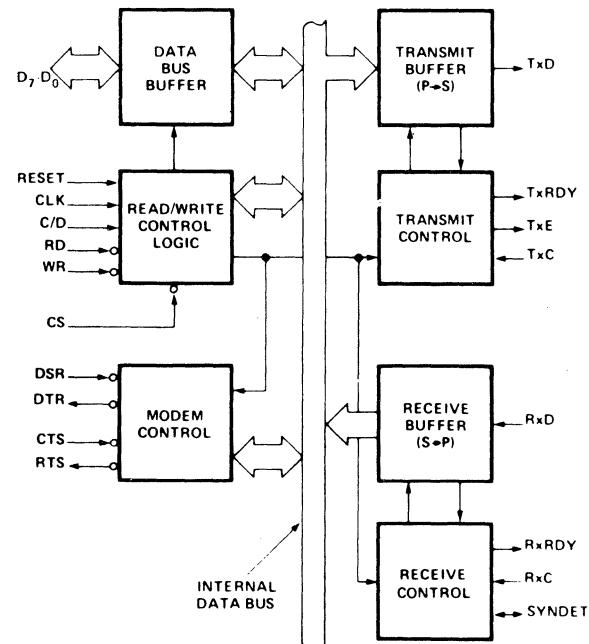
Inputs
D2,D6   .46 Unit Load
STSTB   .31 Unit Load
Others   .16 Unit Load

Outputs
D0-D7   1.25 Unit Loads
Others   9 Unit Loads

The USART is used to interface the serial data channel of a terminal or communications device to the parallel data channel of a computer or terminal. The transmitter section converts parallel data into serial words with start bits, stop bits, and (if desired) parity bits. The receiver section converts serial data into parallel words, while stripping off the start bits and stop bits, checking word length, and, if desired, checking parity. Both the receiver and transmitter are double buffered. Parallel words can contain up to eight bits. Serial word length can be 5, 6, 7, or 8 bits. Parity can be even or odd, or parity checking and generation can be inhibited. The number of stop bits can be either one or two (or 1-1/2 when word length = 5 bits). Transmitting and receiving can occur simultaneously (full-duplex). Transmit and Receive Clocks must be supplied at 1, 16, or 64 times the desired baud rate.

Logic Symbol

Block Diagram

Loading:

Outputs   1 Unit Load

Data Bus Buffer

This is a three-state, bidirectional, 8-bit buffer used to interface the 8251 to the MPU system data bus. Data, control words, command words, and status information are transferred through this buffer.

Read/Write Control Logic

Control inputs from the MPU system are received and stored here. Control/command bits stored here influence subsequent 8251 operation.

RST (Reset). A high on this input forces the 8251 into an "idle" condition, where it remains until a Mode instruction is received.

CLK (Clock). This input is normally driven by the ∅2 (TTL) output of the 8224 Clock Generator, to provide timing for internal operations. This clock must be greater than 30 times the RxC and TxC frequency for synchronous operation and 4.5 times for asynchronous operation.

WR (Write). A low on this input signals the 8251 that the MPU is writing (outputting) to the 8251.

RD (Read). A low on this input signals the 8251 that the MPU is reading (inputting) from the 8251.

C/D (Control/Data). This input, along with the WR and RD inputs, informs the 8251 whether the word on the data bus is a data, control, or status word.

C/D	WR	RD	Function
L	X	X	Data
H	H	L	Status
H	L	H	Control

CS (Chip Select). A low on this input enables the 8251. A high disables all reading and writing and drives all outputs into the high-impedance state.

Modem Control

These inputs and outputs can be used to interface to the modem, or they can be used for other functions as desired.

DSR (Data Set Ready). This input is normally used to test modem conditions such as Data Set Ready. Its condition is tested by the MPU performing a status read operation.

CTS (Clear to Send). A low on this input enables the 8251 to transmit serial data if the TxN bit in the command byte is set to a 1.

DTR (Data Terminal Ready) and RTS (Request to Send). These two outputs can be set low by programming the appropriate bits in the command instruction word. They are normally used for modem control.

Transmit Buffer

This buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits, and outputs a composite serial stream of data on the TxD pin. It consists essentially of two buffers, a transmit buffer and a holding register.

Transmit Control

This section controls the Transmit Buffer and provides the signals necessary to synchronize transmission with the MPU.

TxRDY (Transmit Ready). This output goes high to inform the MPU that the transmit holding register is ready to accept the next character. The MPU can also check this condition by performing a status read operation. This output goes low (at least momentarily) when a character is received from the MPU, and returns high when the character is transferred from the holding register to the transmit buffer.

TxE (Transmitter Empty). This output goes high when the transmitter has no more characters to transmit. It goes low when a character is received from the MPU.

TxC (Transmit Clock). The signal applied to this input controls the rate of data transmission. In synchronous transmission, the baud rate is the same as the TxC rate. In asynchronous transmission, the TxC rate can be 1, 16, or 64 times the baud rate, determined by the Mode instruction. The serial data is shifted out of the 8251 on the falling edge of TxC.

Receive Buffer

This buffer accepts serial data from the RxD input, converts it to parallel format, checks for bits or characters according to the established mode and control words, and provides this data to the MPU.

Receive Control

This section controls the Receive Buffer and provides the signals for synchronizing it with the MPU.

RxRDY (Receiver Ready). This output goes high to inform the MPU that the 8251 has a character ready to be input to the MPU. This condition can also be checked via a status read operation. The output is driven low when the character is received by the MPU (when RD is driven low).
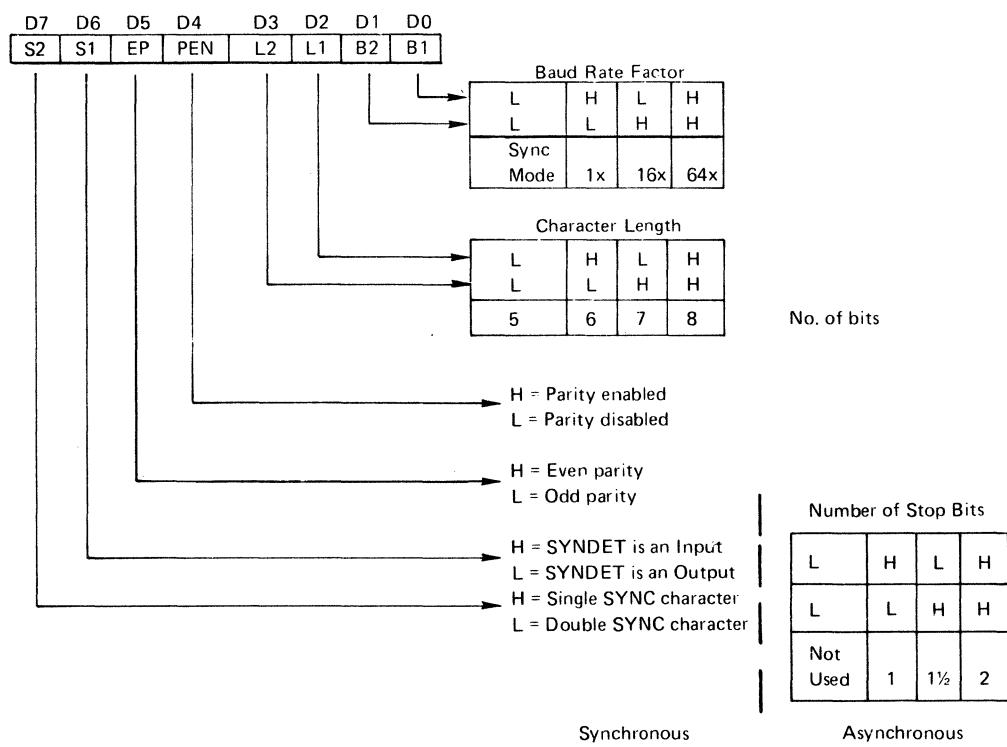
RxC (Receiver Clock). The signal applied to this input controls the rate of data reception. In synchronous mode, the RxC rate must be the same as the baud rate. In asynchronous mode, the RxC rate can be 1, 16, or 64 times the baud rate, as determined by the Mode instruction. The data on the RxD input is sampled and shifted into the 8251 on the rising edge of RxC.

SYNDET (SYNC Detect). This pin is used in synchronous mode only, and it can be used as either an input or an output, programmable through the Control word. When used as an output, it goes high to indicate that the 8251 has received a SYNC character. If the 8251 is programmed to use double SYNC characters, then SYNDET goes high in the middle of the last bit of the second SYNC character. The condition of this output is also available to the MPU via a status read operation, which automatically resets the SYNDET condition.

SYNDET may be used as an input if the check for synchronization is made by external logic. In this case, when SYNDET is driven high, the 8251 begins assembling serial input data into characters on the falling edge of the next RxC.
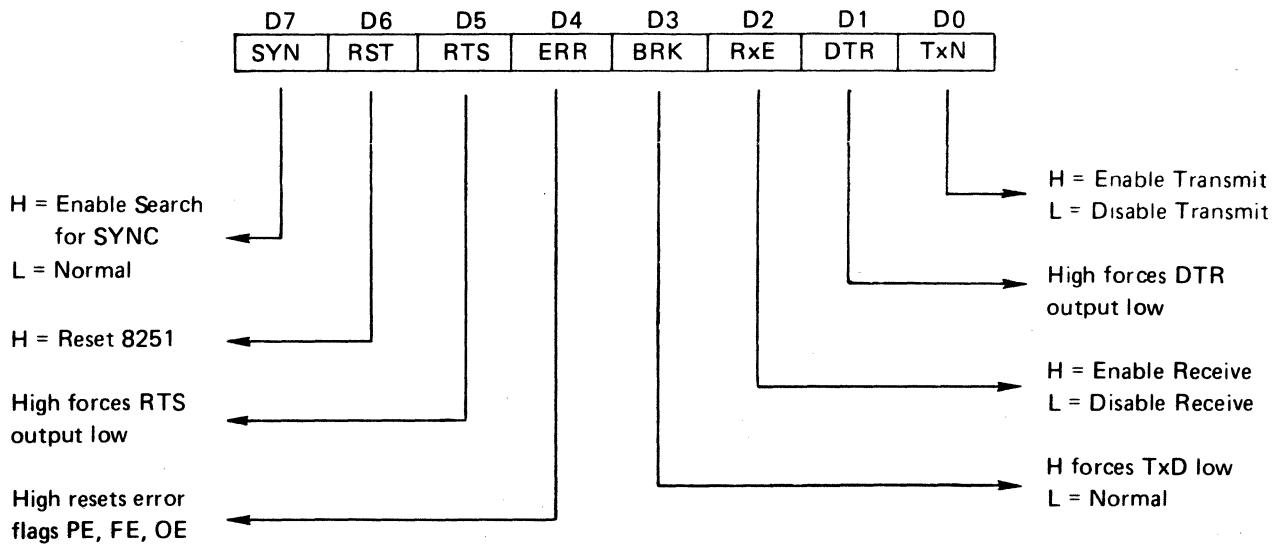
Mode Instruction

The first "control" (C/D high) write after a Reset loads the Mode instruction into the 8251. Any subsequent control writes load Command instructions. The Mode instruction format is as follows:

D7	D6	D5	D4	D3	D2	D1	D0
S2	S1	EP	PEN	L2	L1	B2	B1

Baud Rate Factor

L	H	L	H
L	L	H	H
Sync Mode	1x	16x	64x

Character Length

L	H	L	H
L	L	H	H
5	6	7	8

No. of bits

H = Parity enabled
L = Parity disabled

H = Even parity
L = Odd parity

H = SYNDET is an Input
L = SYNDET is an Output

H = Single SYNC character
L = Double SYNC character

Number of Stop Bits

L	H	L	H
L	L	H	H
Not Used	1	1½	2

Synchronous   Asynchronous

4-41
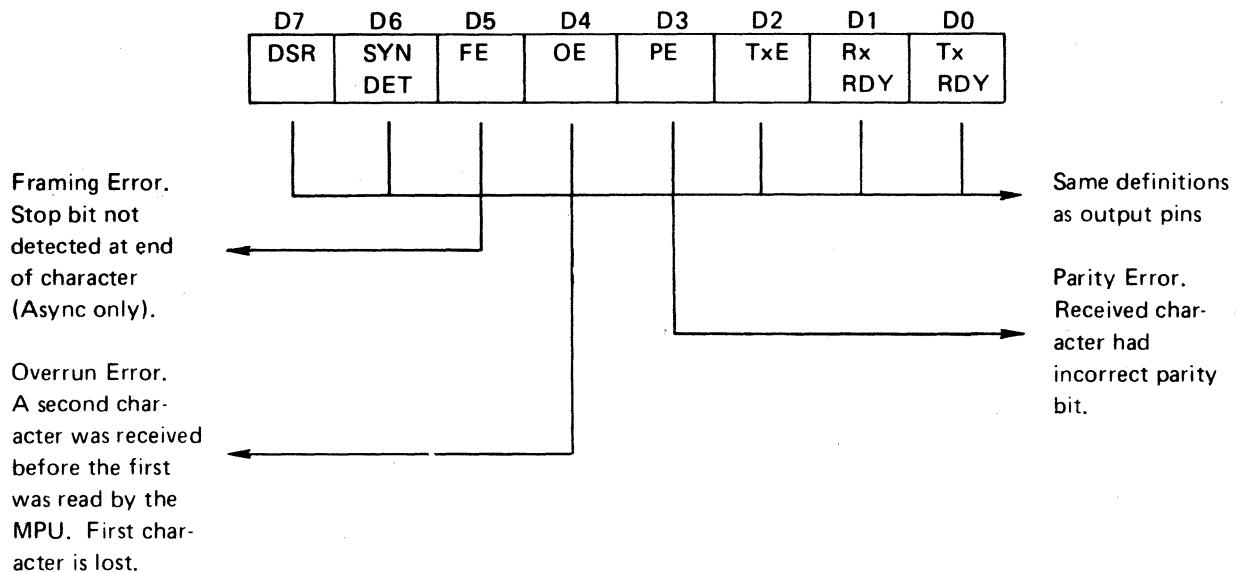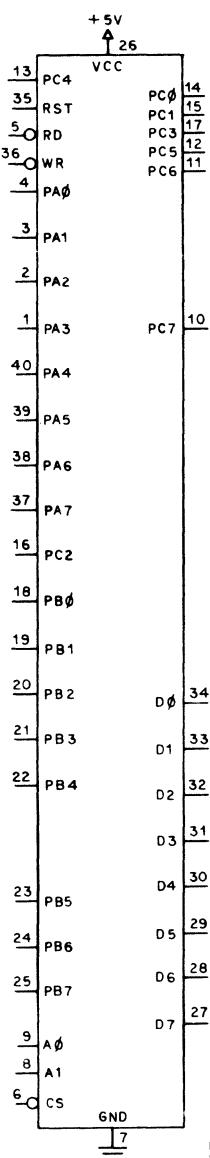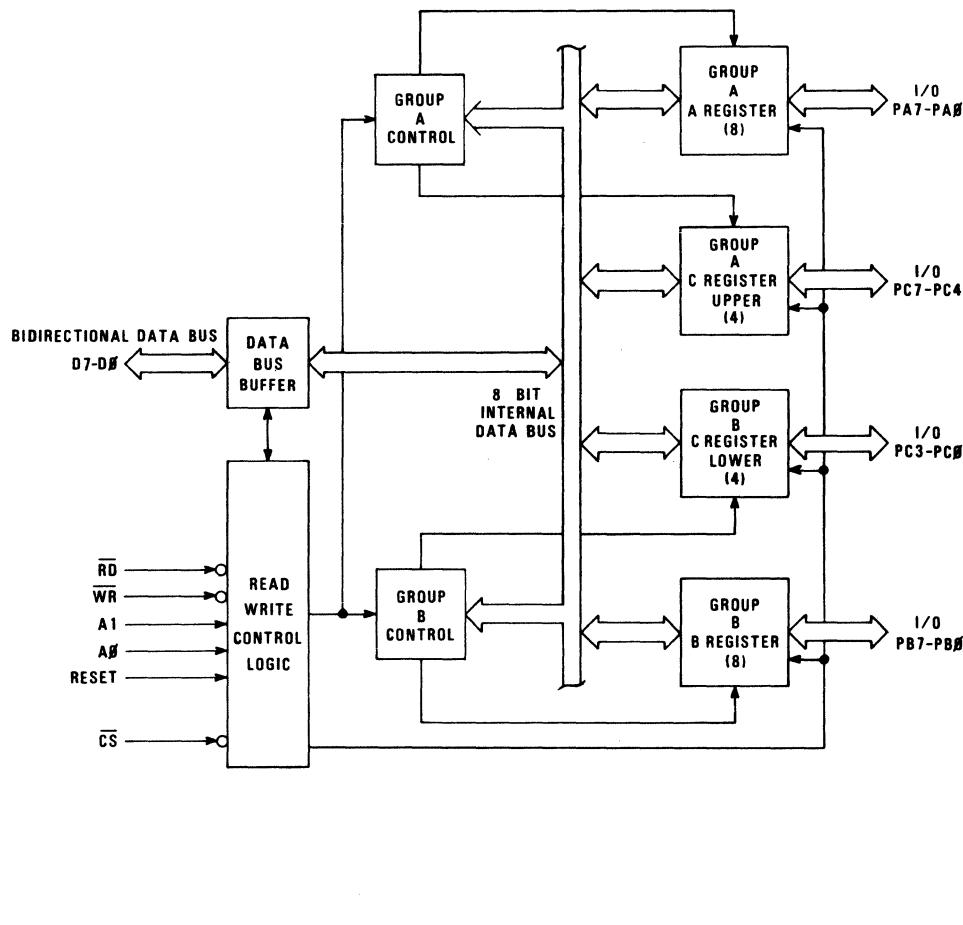
Command Instruction

After the mode instruction has been loaded, subsequent control writes load the Command instruction, as follows:

D7	D6	D5	D4	D3	D2	D1	D0
SYN	RST	RTS	ERR	BRK	RxE	DTR	TxN

H = Enable Search
   for SYNC
L = Normal

H = Reset 8251

High forces RTS
output low

High resets error
flags PE, FE, OE

H = Enable Transmit
L = Disable Transmit

High forces DTR
output low

H = Enable Receive
L = Disable Receive

H forces TxD low
L = Normal

Status Read

When a Read operation is performed with the C/D input high, status is provided to the MPU on the parallel data bus as follows:

D7	D6	D5	D4	D3	D2	D1	D0
DSR	SYN DET	FE	OE	PE	TxE	Rx RDY	Tx RDY

Framing Error.
Stop bit not
detected at end
of character
(Async only).

Overrun Error.
A second char-
acter was received
before the first
was read by the
MPU. First char-
acter is lost.

Same definitions
as output pins

Parity Error.
Received char-
acter had
incorrect parity
bit.

Logic Symbol

Block Diagram

PIN NAMES

D7 - D0	DATA BUS (BIDIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT INPUT
RD	READ INPUT
WR	WRITE INPUT
A0,A1	REGISTER ADDRESS
PA7-PA0	A REGISTER (BITS)
PB7-PB0	B REGISTER (BITS)
PC7-PC0	C REGISTER (BITS)
V_{CC}	15 VOLTS
GND	0 VOLTS

The 8255 is a general purpose, programmable interface designed for use with 8080 microprocessor systems to provide communication between the 8080 and a variety of peripheral devices. An eight-bit bidirectional data bus buffer interfaces the 8080 system bus with the 8255 internal data bus. Three eight-bit registers — called A, B, and C — can be connected directly to the peripheral device. The three registers can be configured by system software or firmware to suit the input/output requirements of a specific peripheral device. The C register can be split into two four-bit registers, and can also be used for control and status signals in applications requiring them. The microprocessor can read from or write to any of the three registers via the data bus buffer.

Communication between the microprocessor and the interface is maintained over the eight bidirectional data bus lines, four control lines, and two address lines. The microprocessor selects the 8255 operating mode by sending a Control Word over the data bus lines. The Control Word is also used to define registers as being input, output, bidirectional, or control. Only the A register can be bidirectional, and only the C register can be used for control. Individual bits of the C register can be set or reset by a Control Word.

There are three operating modes. Registers are controlled in two groups of 12 bits each. Control Group A controls the eight bits of the A register and the four high-order bits of the C register (C7 — C4); Control Group B controls the eight bits of the B register and the low-order half (C3 — C0) of the C register. Since the structure of the Control Word permits separate programming of the two groups, the 8255 can operate in two modes simultaneously. Operating mode is set during system initialization, and can be changed during program execution by sending a new Control Word over the data lines.

The operating modes are as follows:

Mode 0 — Basic Input/Output. The A and B registers can be separately defined as input or output. The C register can be split into two four-bit registers, one input and the other output, or it can be used for all input or all output. Sixteen different register configurations are available. No strobes or handshaking are involved.

Mode 1 — Strobed Input/Output. The A and B registers can be individually programmed for input or output. Six bits of the C register are used as control and status bits for the A and B registers; the remaining two bits of the C register can be programmed as either input or output.

Mode 2 — Strobed Bidirectional Input/Output. The A register can be used for two-way communication with a peripheral device. Five bits of the C register are used for control and status for the A register; the remaining three bits of the C register can be used for input, output, or control, depending on the mode of the B register. When the B register is in Mode 0, the C register bits could be input or output. In mode 1, the three bits of the C register would be used for control and status of the B register.
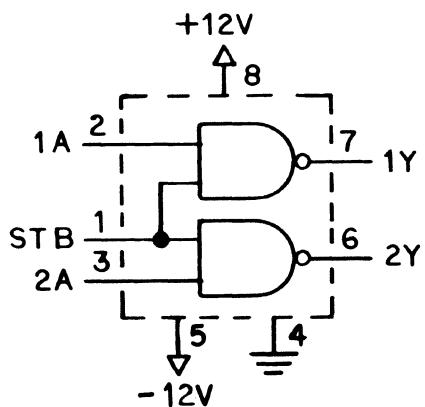
In Mode 1 or Mode 2, when the C register is used for control and status, the peripheral device is permitted to interrupt the 8080. The 8080 program can enable/disable interrupts by setting/resetting individual C register bits.

Loading:

When a register is programmed for output, up to eight output buffers, selected randomly from the B and C registers, can furnish 1mA at 1.5 volts to drive Darlington type or similar circuits. Other outputs can drive 1 unit load.
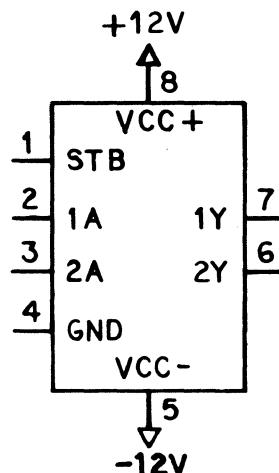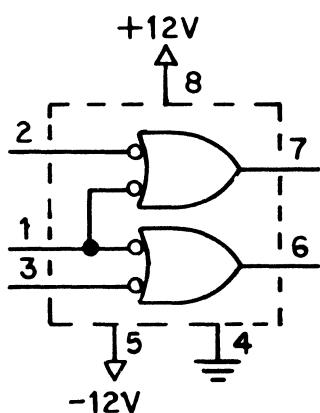
This line driver is commonly used to interface data terminal equipment to data communication equip- ment utilizing the EIA Standard RS-232-C. Input is TTL/DTL compatible, and output is ±12V.

Logic Symbol

Truth Table

| INPUTS | | OUTPUT |
STB	A	Y
L	X	+12
H	L	+12
H	H	-12
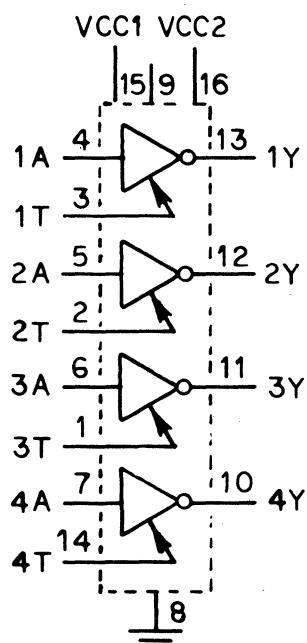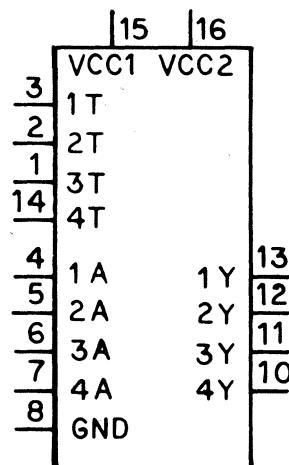
L = 0V
H = +5V
X = Irrelevant

Alternate Symbols

Loading:

Inputs	1 Unit Load
Strobe	2 Unit Loads

This receiver satisfies the requirements of the interface between data communication equipment and data terminal equipment as defined by EIA Standard RS-232-C. Input is from +25V to -25V, and output is either 0V or +5V. For normal operation, the threshold control terminal is connected to VCC1. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold levels. In this mode of operation, if the input voltage goes to zero (or open-circuit), the output will remain either low (0V) or high (+5V) as determined by the previous input. For fail-safe operation, the threshold terminal is left floating. This reduces the hysteresis loop, causing the negative-going threshold to be above 0V. The positive-going threshold is unchanged. In this mode, if the input voltage goes to 0V or is open-circuited, the output goes high (+5V) regardless of the previous input condition. VCC can be either +5V or +12V. Pin 9 should not be connected externally.
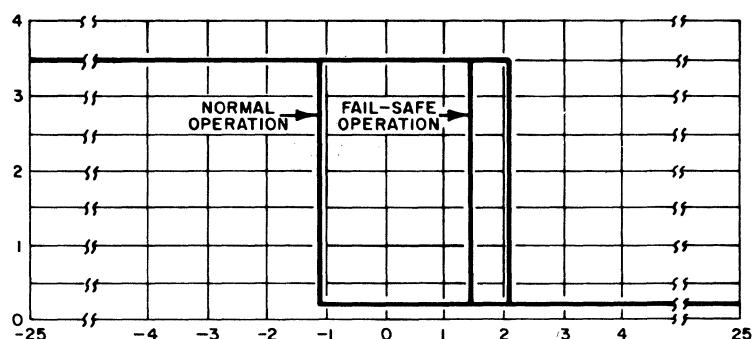
Logic Symbol

Alternate Symbol

A = input
Y = output
T = threshold
    control
VCC1 = +5V
VCC2 = +12V

Truth Table
(each receiver)

INPUT A	OUTPUT Y
-12	H (+5)
+12	L (0)
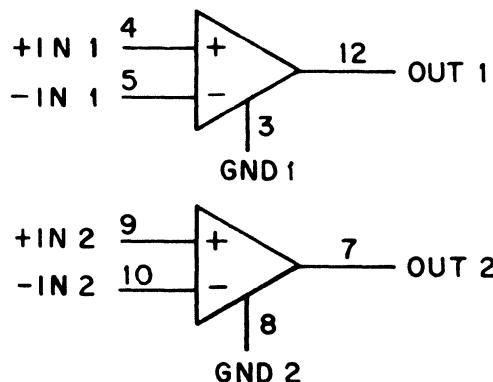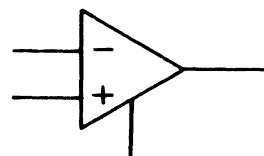
Waveforms

Loading:
    Outputs   10 Unit Loads

This device can operate on voltage supplies up to ±15V, but can also operate off of a single +5V supply, depending upon the application. Note the non-standard voltage connections.

Logic Symbol   Alternate Symbol
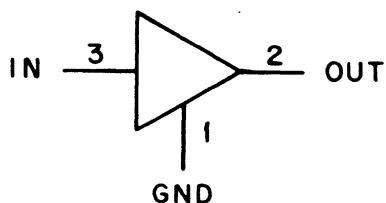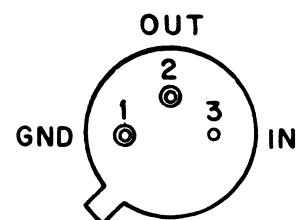
+IN 1 —4—|+   12— OUT 1
-IN 1 —5—|−
          |3
        GND 1

+IN 2 —9—|+   7— OUT 2
-IN 2 —10—|−
           |8
         GND 2

V+, pin 11
V-, pin 6

3-Terminal Negative Voltage Regulator, 5 Volt   Part No. 42155-05   Type LM320H-5
3-Terminal Negative Voltage Regulator, 12 Volt   Part No. 42155-12   Type LM320H-12

This series of negative regulators provides precision regulation of output currents up to .5A, while also providing current limiting and thermal overload protection.

Logic Symbol   Pinout
                                                  (Bottom View)

                                                     OUT

IN —3—| |2— OUT
         |1
       GND   GND   IN

Maximum Voltages
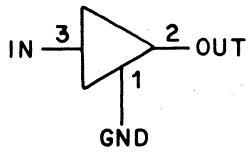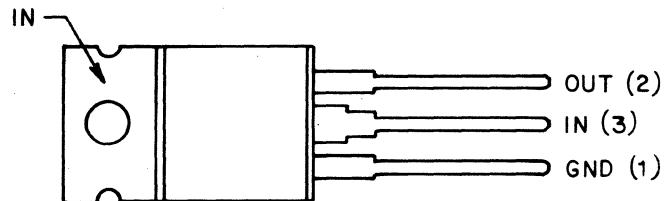
	-05	-12
IN	-7 to -25	-14 to -35
OUT	-4.8 to -5.2	-11.6 to -12.4

3-Terminal Negative Voltage Regulator, 5 Volt

Part No. 42152-05   Type LM320T-5

This series of negative regulators provides precision regulation of output currents up to 1.5A, while providing current limiting and thermal overload protection.

Logic Symbol

IN —3— ▷ —2— OUT
1
GND

Connection Diagram

IN
OUT (2)
IN (3)
GND (1)

Input   = −7.5V to −25V
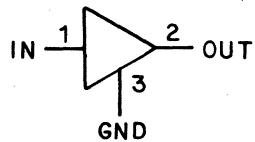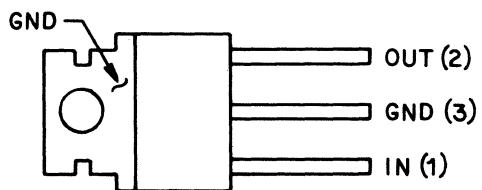
Ouput   = −4.75V to −5.25V

3-Terminal Positive Voltage Regulator, 12 Volt

Part No. 10284-03   Type LM340T-12

This series of positive regulators provides precision regulation of output currents up to 1A, while providing current limiting and thermal overload protection.

Logic Symbol

IN —1— ▷ —2— OUT
3
GND

Connection Diagram

GND
OUT (2)
GND (3)
IN (1)

Input   = +14.4 to +27.5V
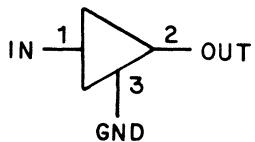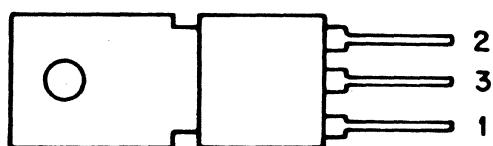
Output = +11.4 to +12.6V

3-Terminal Positive Voltage Regulator, 12 Volt

Part No. 42154-12   Type LM341P-12

This series of positive regulators provides precision regulation of output currents up to .5A, while also providing current limiting and thermal overload protection.

Logic Symbol

IN —1— ▷ —2— OUT
3
GND

Pinout
(Top View)

2
3
1

Input (1)   = +14.8 to +27V

Output (2) = +11.4 to +12.6V
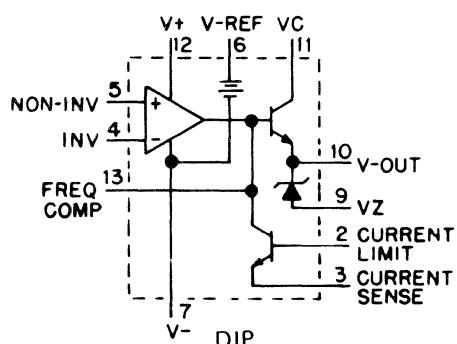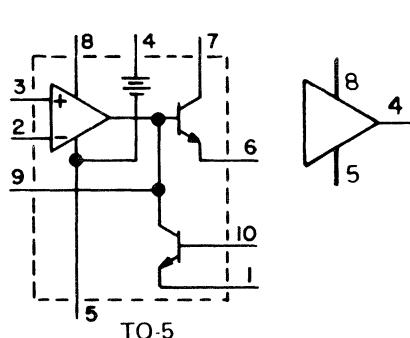
This device is used primarily in series regulator applications. It can supply output current up to 150 ma, but larger currents can be controlled by using the output to drive external transistors. It features extremely low standby current drain, provision for either linear or foldback current limiting, up to 40V maximum input voltage, and an output voltage range of 2V to 37V. It contains a 7V reference source, which can be utilized through suitable external resistors to provide any desired output voltage. An external reference can also be used, if desired. The Vz output is not provided in the TO-5 package: if required, a 6.2V zener diode should be connected in series with V-OUT.
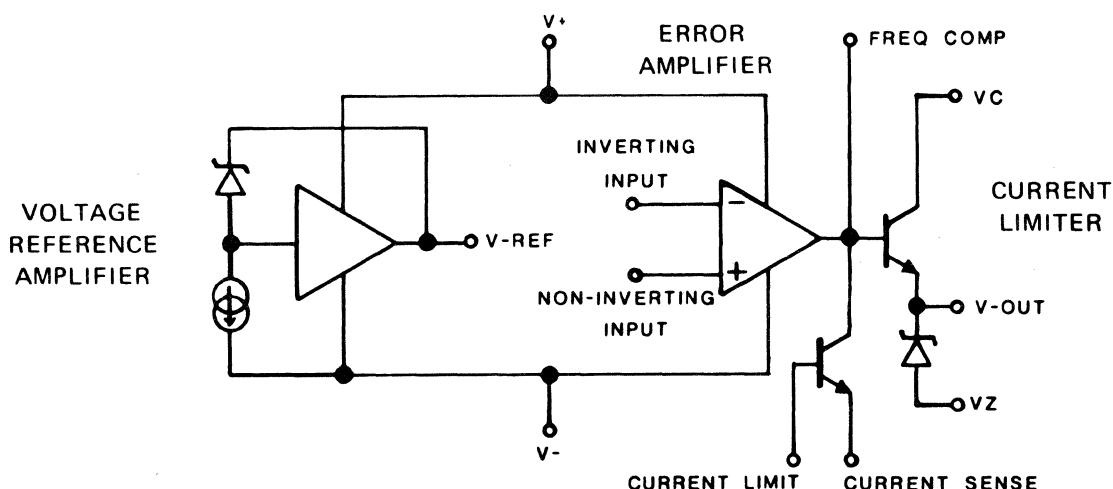
Logic Symbols
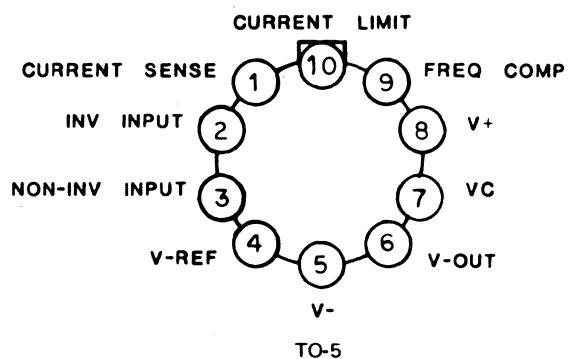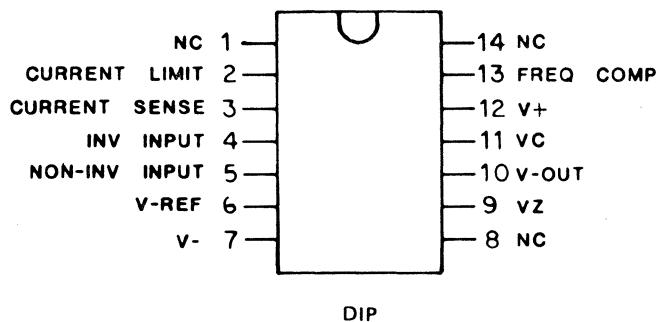
Alternate Symbol

Logic Diagram

VOLTAGE
REFERENCE
AMPLIFIER

ERROR
AMPLIFIER

V+

FREQ COMP

INVERTING
INPUT

NON-INVERTING
INPUT

V-REF

V-

CURRENT LIMIT   CURRENT SENSE

CURRENT
LIMITER

VC

V-OUT

VZ

Pinouts
(Top Views)

NC 1 — — 14 NC
CURRENT LIMIT 2 — — 13 FREQ COMP
CURRENT SENSE 3 — — 12 V+
INV INPUT 4 — — 11 VC
NON-INV INPUT 5 — — 10 V-OUT
V-REF 6 — — 9 VZ
V- 7 — — 8 NC

DIP

CURRENT LIMIT
CURRENT SENSE   FREQ COMP
INV INPUT   V+
NON-INV INPUT   VC
V-REF   V-OUT
V-
TO-5
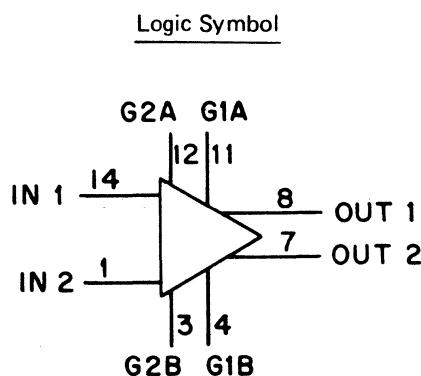
Differential Video Amplifier   Part No. 10124   Type LM733C

This differential-input/differential-output amplifier provides selectable gains of 10, 100, and 400.

Logic Symbol

G2A G1A

IN 1 14

IN 2 1

12 11

8 OUT 1
7 OUT 2

3 4

G2B G1B

V+, 10
V-, 5
(No connection to pins 2, 6, 9, and 13)

Gain Selection

Gain	Connection
10	None
100	G1A to G1B
400	G2A to G2B

OP Amp, High Slew Rate   Part No. 10167   Type MC1741SCP1

This device exhibits fast settling time, a high slew rate (10V/microsecond min.), low power consumption, and short-circuit protection. It is housed in an 8 pin DIP.

Logic Symbol

VCC
7

+IN 3 +

-IN 2 −

6 OUT

4
VEE
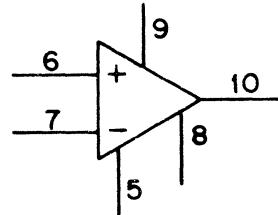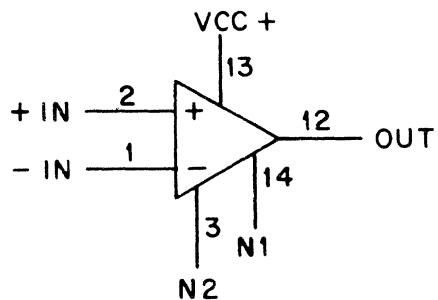
Pin 1 = Offset null
Pin 8 No connection

VCC = +15V
VEE = -15V

Dual Op Amp, General Purpose   Part No. 10165   Type 72747
Dual Op Amp, Selected   Part No. 13072   Type 72747

Logic Symbol

VCC +
13
+ IN ── 2 ── + ── 12 ── OUT
− IN ── 1 ── −
3   14
N2   N1

9
6 ── + ── 10
7 ── −   8
5

VCC-4, No Connection -11
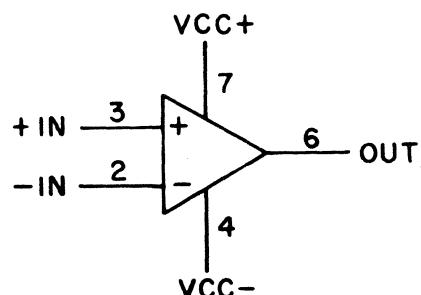
Op Amp, General Purpose   Part No. 10166   Type 72748

This single op amp is housed in an 8-pin DIP.
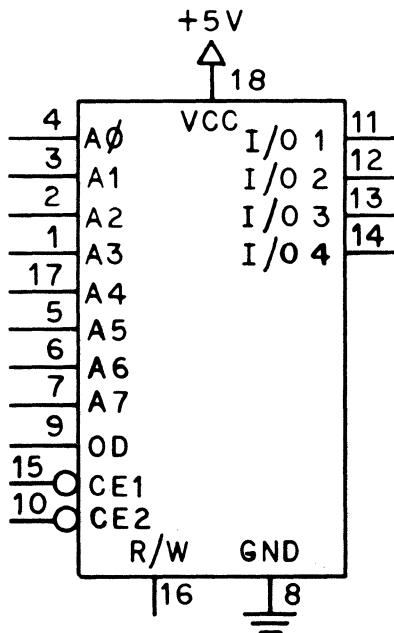
Logic Symbol

VCC+
7
Pin 1 = Offset null/Comp   + IN ── 3 ── + ── 6 ── OUT
Pin 5 = Offset null (N2)   − IN ── 2 ── −
Pin 8 = Comp   4
VCC−
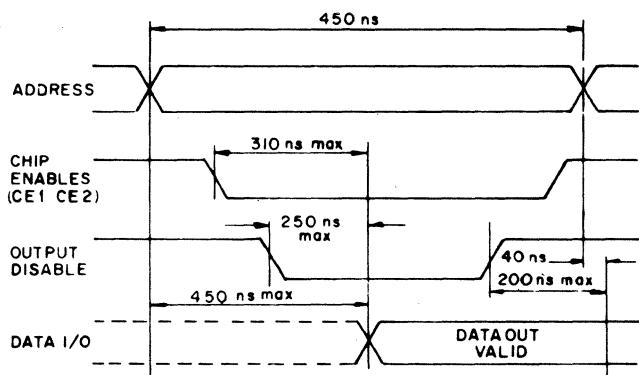
This is the 450 ns member of a family of random-access memories available in several speed ranges. The Output Disable pin (9), when high, drives the Input/Output pins to their high-impedance state.

Logic Symbol

```
                      +5V
                       │
                      18
          ┌──────────────────────┐
      4   │ A∅      VCC   I/O 1   │  11
      3   │ A1            I/O 2   │  12
      2   │ A2            I/O 3   │  13
      1   │ A3            I/O 4   │  14
     17   │ A4                    │
      5   │ A5                    │
      6   │ A6                    │
      7   │ A7                    │
      9   │ OD                    │
     15   │ CE1                   │
     10   │ CE2                   │
          │ R/W         GND       │
          └──────────────────────┘
            16          8
```
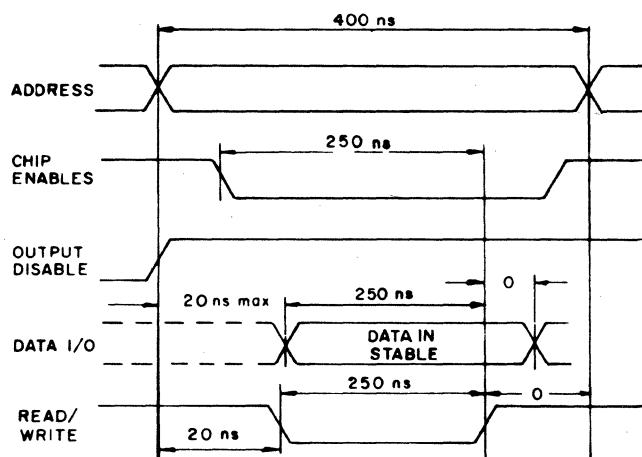
Timing Waveforms
(All times are minimum unless noted)

Read Cycle

```
              450 ns
ADDRESS

CHIP          310 ns max
ENABLES
(CE1 CE2)

              250 ns max
OUTPUT
DISABLE                       40 ns
              450 ns max      200 ns max

DATA I/O              DATA OUT
                      VALID
```

Write Cycle

```
              400 ns
ADDRESS

CHIP          250 ns
ENABLES

OUTPUT
DISABLE
              20 ns max   250 ns       0

DATA I/O          DATA IN
                  STABLE
                      250 ns       0
READ/
WRITE     20 ns
```
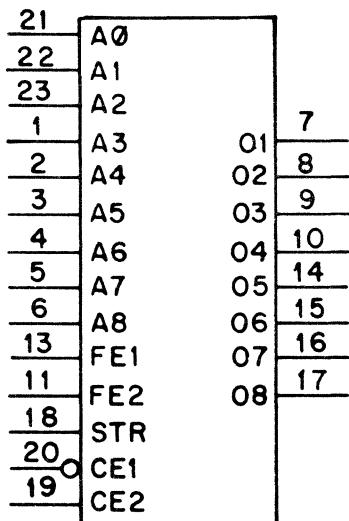
Loading:

Outputs   1.25 Unit Loads

These devices are Programmable Read-Only memories which are normally programmed by the vendor. No truth table appears here because each program requires a separate table. Note that the part number above is the Diablo number for the unprogrammed pROMs: a new number is assigned when the pROM is programmed. Part numbers for programmed pROMs appear on the schematic. Access time is typically 35 ns (60 ns maximum).

There are two modes of operation. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers are controlled solely by CE1 and CE2 lines.

In the LATCHED READ mode, outputs are held in their previous state (1, 0, or Hi-Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the Hi-Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

Logic Symbol

VCC-24, GND-12

A∅-A8	=	Address Inputs
FE1, FE2	=	Programming Inputs
STR	=	Strobe Input
CE1, CE2	=	Chip Enable Inputs
O1-O8	=	Data Outputs

Loading:

| Inputs | .1 Unit Load |
| Outputs | 6 Unit Loads |
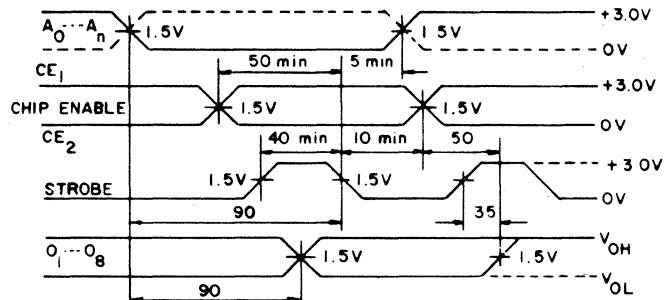
Waveforms
(Times shown are maximum unless noted)
(Times shown are in nanoseconds)

Latched Read
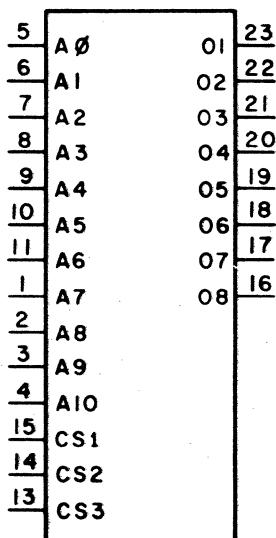
This is a Read-Only Memory that is programmed during manufacture. No part number is given because each program requires a separate part number. Part numbers are given on the schematics. Outputs are 3-state, controlled by three programmable chip-select inputs. Any combination of high- or low-active chip select inputs can be defined, and the desired chip select code is programmed into the chip during manufacture. Maximum access time is 1.5 μs. Only a single power supply voltage (+5V) is required.
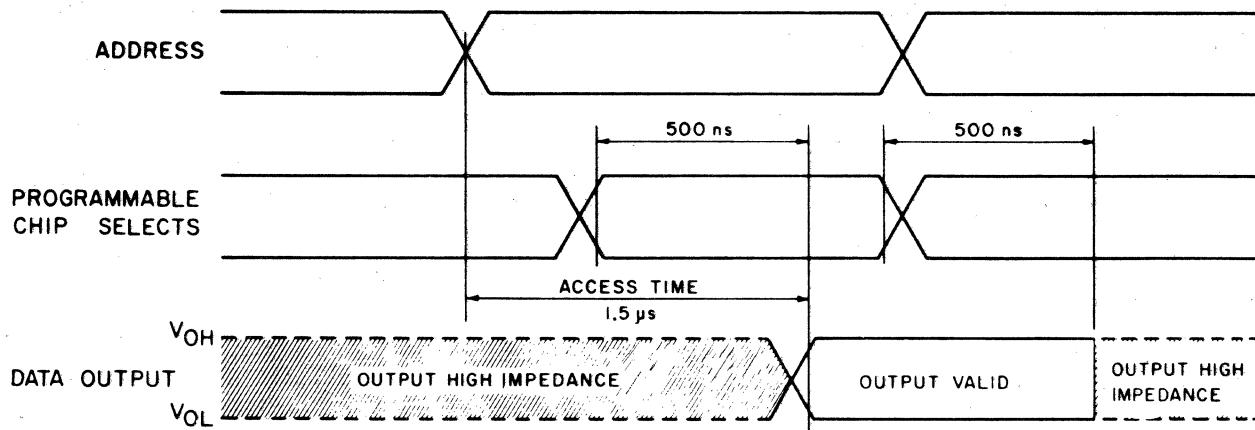
Logic Symbol

5 — AØ	O1 — 23
6 — A1	O2 — 22
7 — A2	O3 — 21
8 — A3	O4 — 20
9 — A4	O5 — 19
10 — A5	O6 — 18
11 — A6	O7 — 17
1 — A7	O8 — 16
2 — A8	
3 — A9	
4 — A10	
15 — CS1	
14 — CS2	
13 — CS3	

VCC-24, GND-12

Waveforms
(All times shown are maximum)

ADDRESS

PROGRAMMABLE CHIP SELECTS

500 ns   500 ns

ACCESS TIME
1.5 μs

DATA OUTPUT V_{OH} OUTPUT HIGH IMPEDANCE   OUTPUT VALID   OUTPUT HIGH IMPEDANCE
               V_{OL}
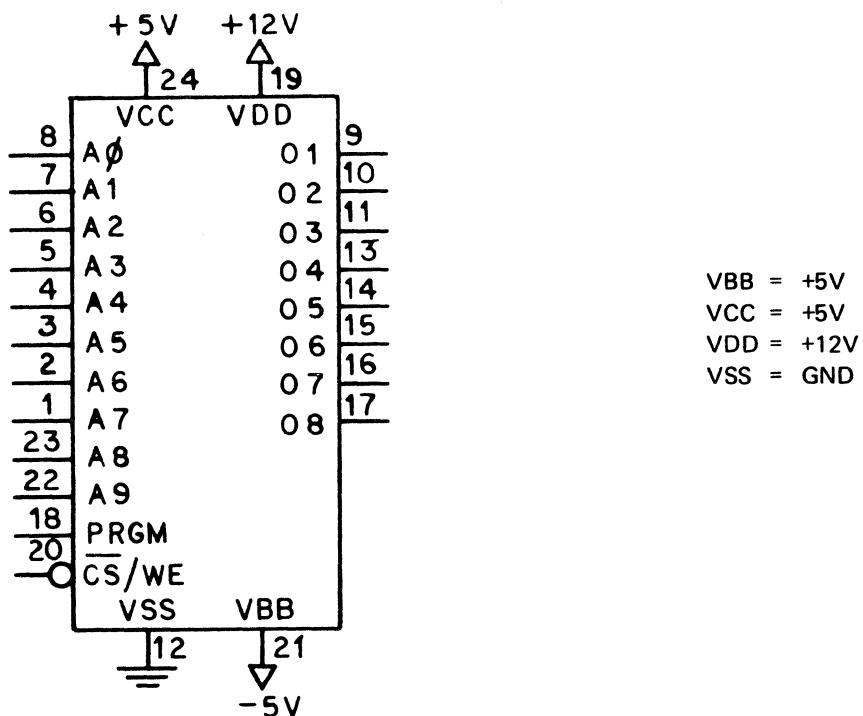
Loading:
        Outputs   1.1 Unit Loads
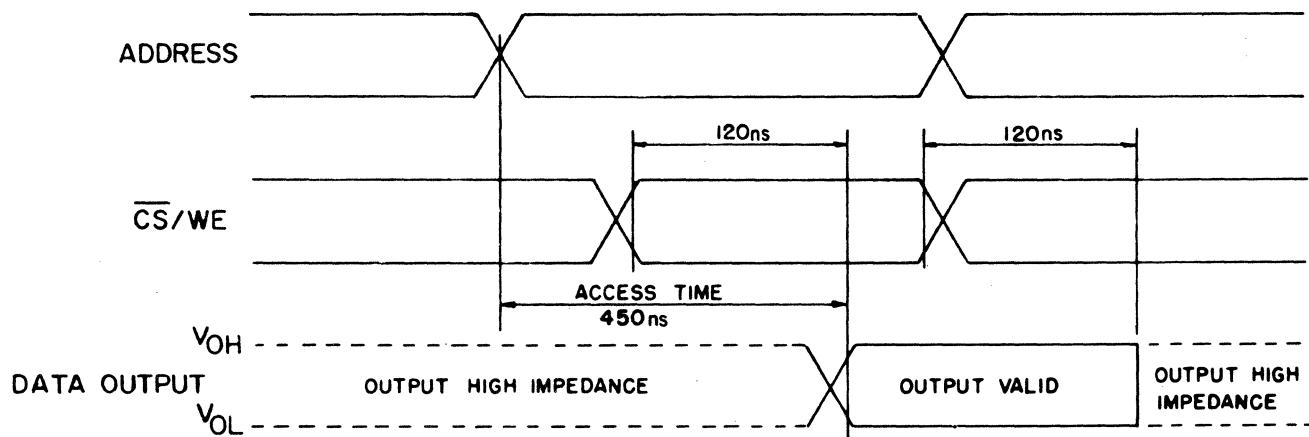
This Read-Only Memory is programmed at the Diablo factory. It has a transparent quartz lid which allows exposure to ultraviolet light to erase the bit pattern. It is electrically compatible with the type 8308 ROM. Access time is 450 ns. Outputs are 3-state, controlled by the Chip Select (CS) input.

Logic Symbol
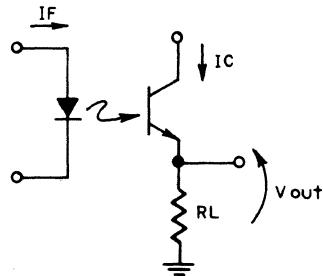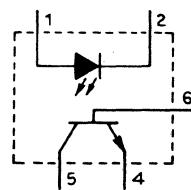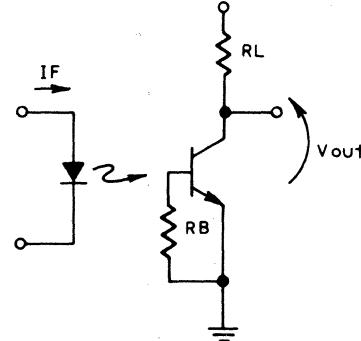
+5V   +12V

24   19

VCC   VDD

Pin			Pin
8	A∅	O1	9
7	A1	O2	10
6	A2	O3	11
5	A3	O4	13
4	A4	O5	14
3	A5	O6	15
2	A6	O7	16
1	A7	O8	17
23	A8		
22	A9		
18	PRGM		
20	CS/WE		

VSS   VBB

12   21

-5V

VBB = +5V
VCC = +5V
VDD = +12V
VSS = GND

Waveforms
(All times shown are maximum)

ADDRESS

CS/WE   120ns   120ns

ACCESS TIME
450ns

V_{OH} -

DATA OUTPUT   OUTPUT HIGH IMPEDANCE   OUTPUT VALID   OUTPUT HIGH IMPEDANCE

V_{OL} -

Loading:

Outputs   1 Unit Load
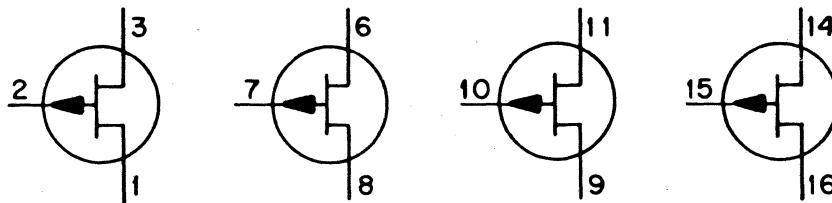
This circuit element consists of a solid-state gallium arsenide diode lamp optically coupled to an NPN silicon planar phototransistor. It is mounted in a six-lead plastic DIP. Its function is to couple two circuits optically, while isolating them electrically. The base can be left floating as in Circuit 1 or connected as shown in Circuit 2.

Logic Symbol

Circuit 1

Circuit 2

Quad Field Effect Transistor (FET)

Part No. 10190
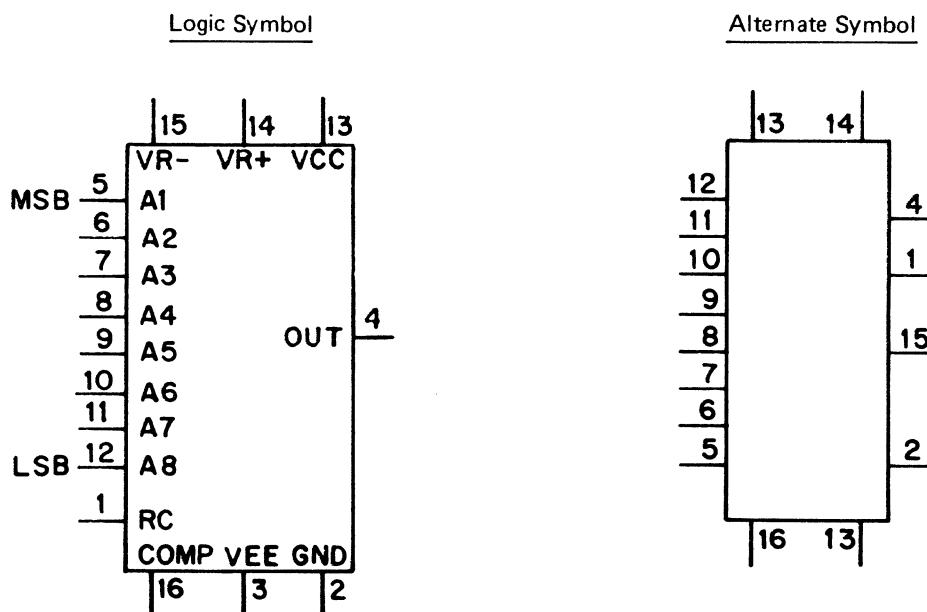
Type 8041

This IC contains four independent p-channel FETs.

Logic Symbol

This eight-bit multiplying D-to-A converter provides a current output which is the product of a digital word (applied to the A1-A8 inputs) and an analog reference voltage (applied to the VR+ and VR- inputs). Digital inputs are TTL and CMOS compatible. Output voltage swing is +0.5V to -0.6V with the Range Control (pin 1) grounded; leaving pin 1 open enables the negative voltage swing to reach -5V when maximum power supply voltages are applied. Frequency compensation capacitors are connected to pin 16. Note the non-standard VCC and GND connections.

Logic Symbol   Alternate Symbol

NOTE: VCC-13, GND-2
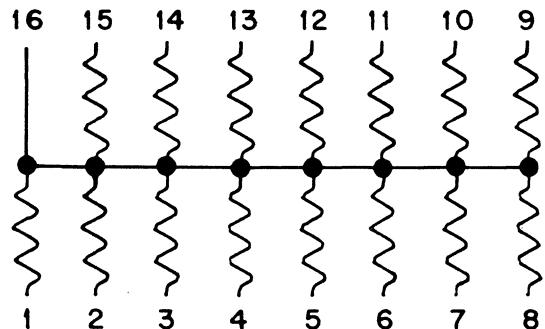
VCC = +5V
VEE = -5V to -15V (current source)
VR- = -15V (max.)
VR+ = +5V (max.)

Loading:

Inputs (digital)   1 Unit Load
Output   2.0 ma.

Resistor Network, 1K x 15   Part No. 10239-01

Pinout

```
16   15   14   13   12   11   10   9
```

Resistor Network, 1K x 13   Part No. 10761

Pinout

```
14   13   12   11   10   9    8
```
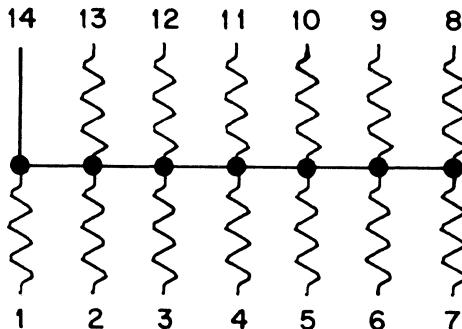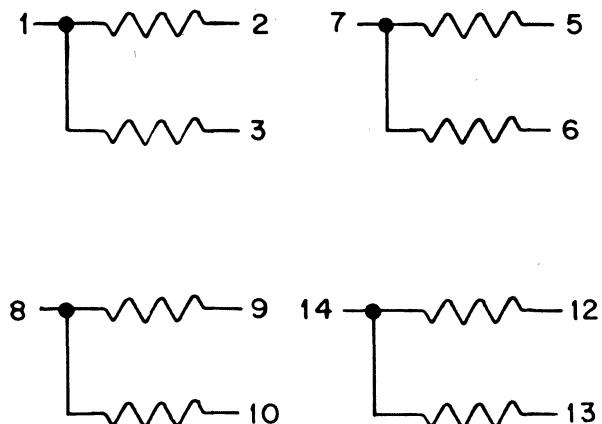
Resistor Network, Quad 10K x 2   Part No. 13044

Pinout

```
1 ——〜〜〜—— 2      7 ——〜〜〜—— 5
        └——〜〜〜—— 3              └——〜〜〜—— 6

8 ——〜〜〜—— 9      14 ——〜〜〜—— 12
        └——〜〜〜—— 10             └——〜〜〜—— 13
```

(Pins 4 and 11, no connection)

4.6 CODE CHARTS

Applicable code charts are presented in Figure 4-2.

4.7 SCHEMATICS AND LOGIC DRAWINGS

Figure 4-3 explains the meaning of the various notations contained on the logic drawings and schematics. For more information on component locations and connector pin numbers, etc., see Section 3.

Table 4-2 lists the schematics and logic drawings contained in the remainder of this manual.

Table 4-2. Schematics and Logic Drawings

Drawing Number	Description
23924-99	HPRO3 Board
23926-XX	XMEM1 Board
400296-01	8080 INTERFACE Board
40510-XX	LOGIC-2 Board
40520-04	SERVO Board
40515-03	XDCR Board
40525-05	CAR PWR AMP Board
40530-06	PW PWR AMP Board
46080-01	Mother Board
400056-01	Control Panel Assy.
400094-01	Keyboard Assy.
26021-XX	Power Supply
400089-01	Signal Cables
400183-01	Power Distribution
24471	Printer Cables

1968 ASCII: American Standard Code for information Interchange. Standard No. X3.4-1968 of the American National Standards Institute.

Bits — b7→ / b6→ / b5→ COLUMN→		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4 b3 b2 b1	↓ROW↓	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL	DLE	SP	0	@	P	`	p
0 0 0 1	1	SOH	DC1	!	1	A	Q	a	q
0 0 1 0	2	STX	DC2	"	2	B	R	b	r
0 0 1 1	3	ETX	DC3	#	3	C	S	c	s
0 1 0 0	4	EOT	DC4	$	4	D	T	d	t
0 1 0 1	5	ENQ	NAK	%	5	E	U	e	u
0 1 1 0	6	ACK	SYN	&	6	F	V	f	v
0 1 1 1	7	BEL	ETB	'	7	G	W	g	w
1 0 0 0	8	BS	CAN	(	8	H	X	h	x
1 0 0 1	9	HT	EM	)	9	I	Y	i	y
1 0 1 0	10	LF	SUB	*	:	J	Z	j	z
1 0 1 1	11	VT	ESC	+	;	K	[	k	{
1 1 0 0	12	FF	FS	,	<	L	\	l	:
1 1 0 1	13	CR	GS	−	=	M	]	m	}
1 1 1 0	14	SO	RS	.	>	N	^	n	~
1 1 1 1	15	SI	US	/	?	O	_	o	DEL

All characters in these two columns and SP (Space) are non-printing. DEL (Delete) does not print in Remote mode, but prints logical NOT symbol (¬) when entered on keyboard in Local mode. (Logical NOT is also printed in place of characters received with parity, overrun, or framing error.)

When UPPER CASE ONLY is used, shaded lower case characters (columns 6 & 7) from keyboard are converted to their upper case equivalents (columns 4 & 5) before being printed or transmitted.

Figure 4-2a. ASCII Code Chart

Lower Case	N/A	B	A	8	4	2	1	Upper Case
IBM	C	B	A	8	4	2	1	
.	C	B				2		.
;	C	B	A		4		1	:
,		B	A		4	2	1	,
'	C	B			4			"
!		B						]
=		B	A			2		+
-		B	A	8		2	1	
/		B	A	8				?
1							1	+
2						2		@
3	C					2	1	#
4				8				$
5					4			%
6	C				4	2		[
7	C				4		1	&
8					4	2	1	*
9 (EOA, Ⓓ)				8		2	1	(
0	C			8			1	)
a	C	B			4	2	1	A
b	C		A	8		2	1	B
c	C		A		4	2	1	C
d			A		4		1	D
e	C		A		4			E
f	C	B	A			2	1	F
g		B	A				1	G
h			A	8			1	H
i		B			4	2		I
j	C	B	A					J
k			A		4	2		K
l	C		A	8				L
m	C	B					1	M
n	C		A			2		N
o	C	B		8				O
p		B	A		4			P
q	C	B	A		4	2		Q
r		B			4		1	R
s		B		8			1	S
t			A					T
u			A			2	1	U
v		B				2	1	V
w	C	B		8		2	1	W
x	C		A				1	X
y	C	B	A	8			1	Y
z	C			8		2		Z

Non-Printing Codes								
SP	C							Space
HT		B	A	8	4		1	Horizontal Tab
BS	C	B		8	4	2		Backspace
NL	C	B		8	4		1	New Line
LF	C		A	8	4		1	Line Feed
PN	C			8	4			Punch On
BY			A	8	4			Bypass
RES		B		8	4			Restore
PF	C	B	A	8	4			Punch Off
RS				8	4		1	Reader Stop
EOB	C		A	8	4	2		End of Block
EOT (Ⓒ)	C			8	4	2	1	End of Transmission
PRE			A	8	4	2	1	Prefix
IL		B		8	4	2	1	Idle
UC				8	4	2		Upper Case
LC		B	A	8	4	2		Lower Case
DEL	C	B	A	8	4	2	1	Delete
UN1			A	8		2		Unspecified
UN2		B		8		2		Unspecified
UN3	C	B	A	8		2		Unspecified

Figure 4-2b. IBM Correspondence Code

		Bit Number						
Internal Data Bus (HPR03)	N/A	DA0	DA1	DA2	DA3	DA4	DA5	
IBM	C	B	A	8	4	2	1	
Lower Case								**Upper Case**
.		B	A	8		2	1	¬
,	C		A	8		2	1	|
# (EOA, Ⓓ)				8		2	1	"
$	C	B		8		2	1	!
&	C	B	A					+
-		B						
/	C		A				1	?̄
@			A					¢
1							1	=
2						2		<
3	C					2	1	;
4					4			:
5	C				4		1	%
6	C				4	2		'
7					4	2	1	>
8				8				*
9	C			8			1	(
0	C			8		2		)
a		B	A				1	A
b		B	A			2		B
c	C	B	A			2	1	C
d		B	A		4			D
e	C	B	A		4		1	E
f	C	B	A		4	2		F
g		B	A		4	2	1	G
h		B	A	8				H
i	C	B	A	8			1	I
j	C	B					1	J
k	C	B				2		K
l		B				2	1	L
m	C	B			4			M
n		B			4		1	N
o		B			4	2		O
p	C	B			4	2	1	P
q	C	B		8				Q
r		B		8			1	R
s	C		A			2		S
t			A			2	1	T
u	C		A		4			U
v			A		4		1	V
w			A		4	2		W
x	C		A		4	2	1	X
y	C		A	8				Y
z			A	8			1	Z
Non-Printing Codes								
SP	C							Space
HT		B	A	8	4		1	Horizontal Tab
BS	C	B		8	4	2		Backspace
NL	C	B		8	4		1	New Line
LF	C		A	8	4		1	Line Feed
PN	C			8	4			Punch On
BY			A	8	4			Bypass
RES		B		8	4			Restore
PF	C	B	A	8	4			Punch Off
RS				8	4		1	Reader Stop
EOB	C		A	8	4	2		End of Block
EOT (Ⓒ)	C			8	4	2	1	End of Transmission
PRE			A	8	4	2	1	Prefix
IL		B		8	4	2	1	Idle
UC				8	4	2		Upper Case
LC		B	A	8	4	2		Lower Case
DEL	C	B	A	8	4	2	1	Delete
UN1			A	8		2		Unspecified
UN2		B		8		2		Unspecified
UN3	C	B	A	8		2		Unspecified

Figure 4-2c. IBM PTTC/EBCD Code

| Internal Data Bus (HPR03) | N/A | \multicolumn{6}{c}{Bit Number} | Upper Case |

Lower Case	N/A	B	A	8	4	2	1	Upper Case
IBM (C)	C	B	A	8	4	2	1	
.	C	B				2		:
[	C	B	A		4		1	(
,		B	A		4	2	1	;
]		B			4			)
←		B						→
×		B	A			2		÷
+		B	A	8		2	1	-
/		B	A	8				\
1							1	¨
2						2		¯
3	C					2	1	<
4				8				≤
5					4			=
6	C				4	2		≥
7	C				4		1	>
8					4	2	1	≠
9 (EOA, Ⓓ)				8		2	1	∨
0	C			8			1	∧
A	C	B			4	2	1	∝
B	C		A	8		2	1	⊥
C	C		A		4	2	1	∩
D			A		4		1	⌊
E	C		A		4			ε
F	C	B	A			2	1	_
G		B	A				1	∇
H			A	8			1	Δ
I		B			4	2		⍳
J	C	B	A					○
K			A		4	2		'
L	C		A	8				⎕
M	C	B					1		
N	C		A			2		⊤
O	C	B		8				○
P		B	A		4			*
Q	C	B	A		4	2		?
R		B			4		1	⍴
S		B		8			1	⌈
T			A					∼
U			A			2	1	↓
V		B				2	1	∪
W	C	B		8		2	1	ω
X	C		A				1	⊃
Y	C	B	A	8			1	↑
Z	C			8		2		⊂

Non-Printing Codes

	N/A	B	A	8	4	2	1	
SP	C							Space
HT		B	A	8	4		1	Horizontal Tab
BS	C	B		8	4	2		Backspace
NL	C	B		8	4		1	New Line
LF	C		A	8	4		1	Line Feed
PN	C			8	4			Punch On
BY			A	8	4			Bypass
RES		B		8	4			Restore
PF	C	B	A	8	4			Punch Off
RS				8	4		1	Reader Stop
EOB	C		A	8	4	2		End of Block
EOT (Ⓒ)	C			8	4	2	1	End of Transmission
PRE			A	8	4	2	1	Prefix
IL		B		8	4	2	1	Idle
UC				8	4	2		Upper Case
LC		B	A	8	4	2		Lower Case
DEL	C	B	A	8	4	2	1	Delete
UN1			A	8		2		Unspecified
UN2		B		8		2		Unspecified
UN3	C	B	A	8		2		Unspecified

Figure 4-2d. IBM Correspondence Code (APL)

		Bit Number						
Internal Data Bus (HPR03)	N/A	D A 0	D A 1	D A 2	D A 3	D A 4	D A 5	
IBM	C	B	A	8	4	2	1	
Lower Case								**Upper Case**
.		B	A	8		2	1	:
,	C		A	8		2	1	;
] (EOA, Ⓓ)				8		2	1	)
[	C	B		8		2	1	(
×	C	B	A					÷
+		B						−
/	C		A				1	\
←			A					→
1							1	¨
2						2		¯
3	C					2	1	<
4					4			≤
5	C				4		1	=
6	C				4	2		≥
7					4	2	1	>
8				8				≠
9	C			8			1	∨
0	C			8		2		∧
A		B	A				1	α
B		B	A			2		⊥
C	C	B	A			2	1	∩
D		B	A		4			⌊
E	C	B	A		4		1	∈
F	C	B	A		4	2		_
G		B	A		4	2	1	∇
H		B	A	8				∆
I	C	B	A	8			1	⍳
J	C	B					1	○
K	C	B				2		'
L		B				2	1	□
M	C	B			4			|
N		B			4		1	⊤
O		B			4	2		○
P	C	B			4	2	1	*
Q	C	B		8				?
R		B		8			1	⍴
S	C		A			2		⌈
T			A			2	1	~
U	C		A		4			↑
V			A		4		1	∪
W			A		4	2		ω
X	C		A		4	2	1	⊃
Y	C		A	8				↑
Z			A	8			1	⊂
Non-Printing Codes								
SP	C							Space
HT		B	A	8	4		1	Horizontal Tab
BS	C	B		8	4	2		Backspace
NL	C	B		8	4		1	New Line
LF	C		A	8	4		1	Line Feed
PN	C			8	4			Punch On
BY			A	8	4			Bypass
RES		B		8	4			Restore
PF	C	B	A	8	4			Punch Off
RS				8	4		1	Reader Stop
EOB	C		A	8	4	2		End of Block
EOT (©)	C			8	4	2	1	End of Transmission
PRE			A	8	4	2	1	Prefix
IL		B		8	4	2	1	Idle
UC				8	4	2		Upper Case
LC		B	A	8	4	2		Lower Case
DEL	C	B	A	8	4	2	1	Delete
UN1			A	8		2		Unspecified
UN2		B		8		2		Unspecified
UN3	C	B	A	8		2		Unspecified

Figure 4-2e. IBM PTTC/EBCD Code (APL)
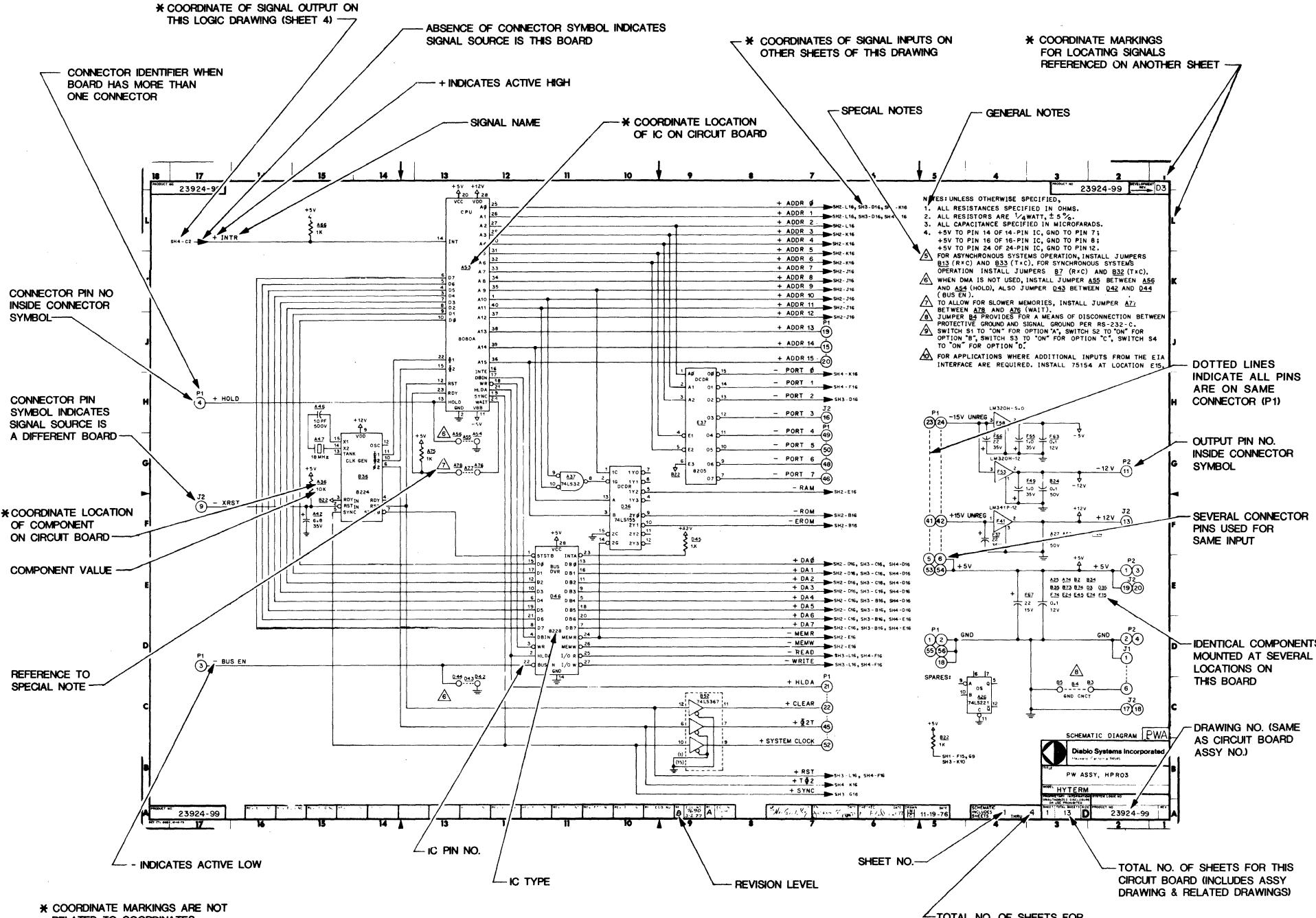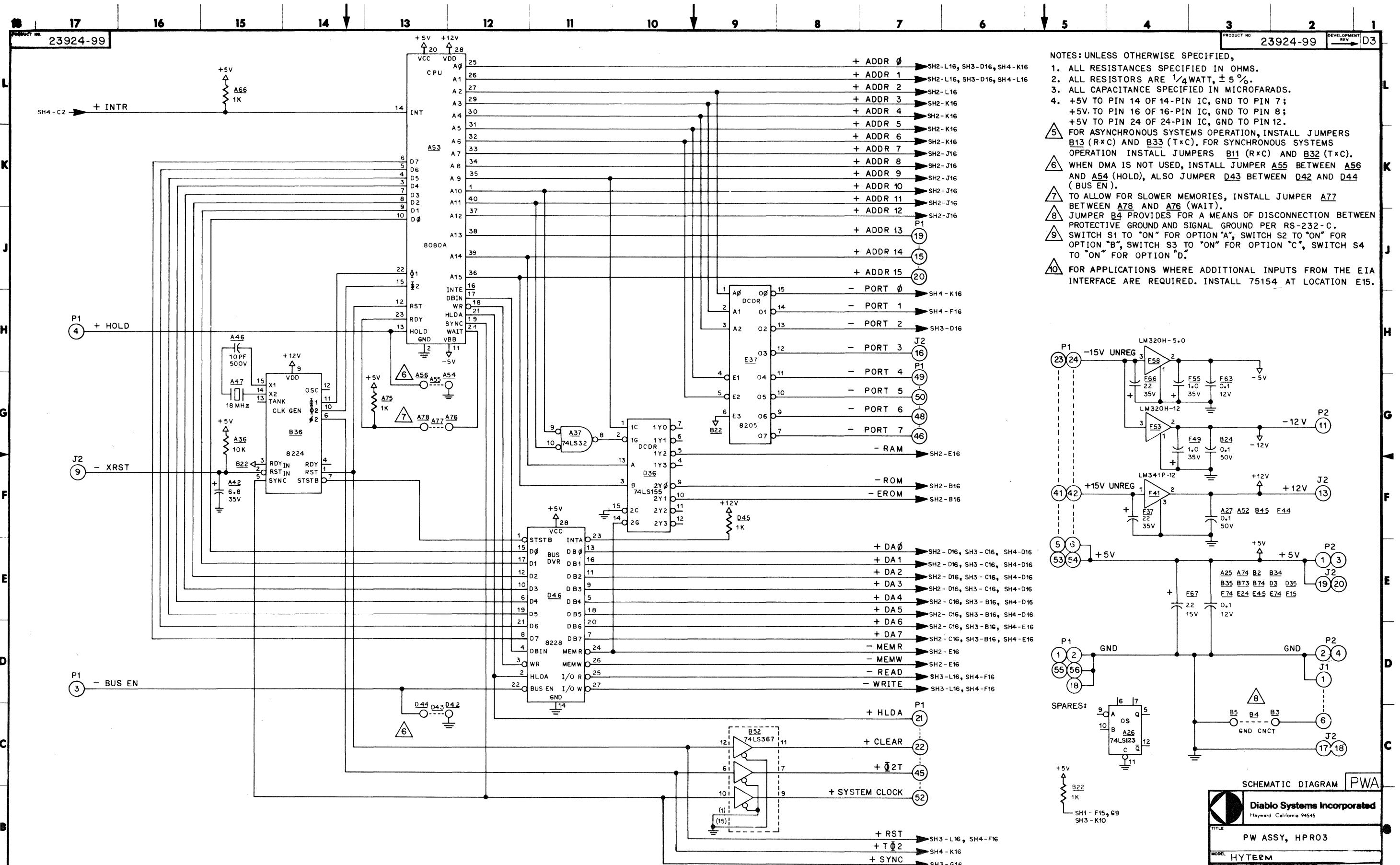
Figure 4-3. Logic Drawing Notation

4-64

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE ¼ WATT, ± 5 %.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8;
   +5V TO PIN 24 OF 24-PIN IC, GND TO PIN 12.
5. FOR ASYNCHRONOUS SYSTEMS OPERATION, INSTALL JUMPERS
   B13 (R×C) AND B33 (T×C). FOR SYNCHRONOUS SYSTEMS
   OPERATION INSTALL JUMPERS B11 (R×C) AND B32 (T×C).
6. WHEN DMA IS NOT USED, INSTALL JUMPER A55 BETWEEN A56
   AND A54 (HOLD), ALSO JUMPER D43 BETWEEN D42 AND D44
   (BUS EN).
7. TO ALLOW FOR SLOWER MEMORIES, INSTALL JUMPER A77
   BETWEEN A78 AND A76 (WAIT).
8. JUMPER B4 PROVIDES FOR A MEANS OF DISCONNECTION BETWEEN
   PROTECTIVE GROUND AND SIGNAL GROUND PER RS-232-C.
9. SWITCH S1 TO "ON" FOR OPTION "A", SWITCH S2 TO "ON" FOR
   OPTION "B", SWITCH S3 TO "ON" FOR OPTION "C", SWITCH S4
   TO "ON" FOR OPTION "D".
10. FOR APPLICATIONS WHERE ADDITIONAL INPUTS FROM THE EIA
    INTERFACE ARE REQUIRED. INSTALL 75154 AT LOCATION E15.
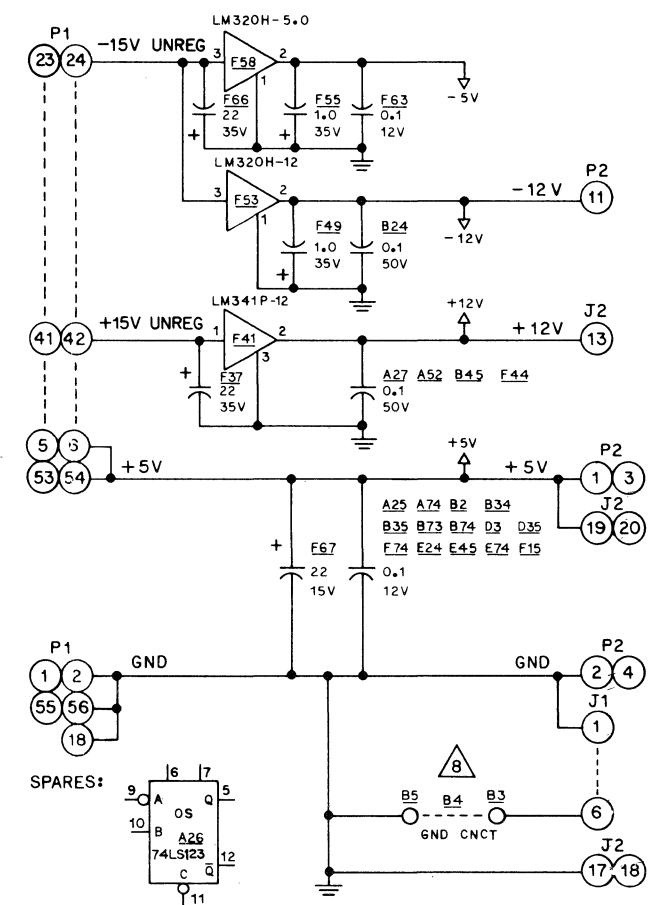
SCHEMATIC DIAGRAM PWA

Diablo Systems Incorporated
Hayward California 94545

TITLE
PW ASSY, HPRO3

MODEL
HYTERM

PRODUCT NO. 23924-99

DEVELOPMENT REV. D3

SHEET 1 TOTAL SHEETS 4 1 13 D

DATE 11-19-76

P1

SH1-L7 →	+ ADDR Ø	+ ADDR Ø	35
SH1-L7 →	+ ADDR 1	+ ADDR 1	36
SH1-L7 →	+ ADDR 2	+ ADDR 2	33
SH1-L7 →	+ ADDR 3	+ ADDR 3	34
SH1-L7 →	+ ADDR 4	+ ADDR 4	29
SH1-K7 →	+ ADDR 5	+ ADDR 5	27
SH1-K7 →	+ ADDR 6	+ ADDR 6	25
SH1-K7 →	+ ADDR 7	+ ADDR 7	43
SH1-K7 →	+ ADDR 8	+ ADDR 8	44
SH1-K7 →	+ ADDR 9	+ ADDR 9	40
SH1-K7 →	+ ADDR 10	+ ADDR 10	38
SH1-K7 →	+ ADDR 11	+ ADDR 11	28
SH1-J7 →	+ ADDR 12	+ ADDR 12	26

RAM — D65 — 2111A-4
RAM — F65 — 2111A-4
RAM — B65 — 2111A-4
RAM — E65 — 2111A-4
ROM — E48 — 8316
ROM — F48 — 8316
EROM — F32 — 2704/2708

D37 — 74LSØ4

P1

SH1-D7 →	– MEMR	– MEMR	7
SH1-D7 →	– MEMW	– MEMW	17
SH1-G7 →	– RAM		
SH1-E7 →	+ DA Ø	+ DA Ø	9
SH1-E7 →	+ DA 1	+ DA 1	12
SH1-E7 →	+ DA 2	+ DA 2	11
SH1-E7 →	+ DA 3	+ DA 3	13
SH1-E7 →	+ DA 4	+ DA 4	8
SH1-E7 →	+ DA 5	+ DA 5	10
SH1-D7 →	+ DA 6	+ DA 6	14
SH1-D7 →	+ DA 7	+ DA 7	16
SH1-F7 →	– ROM		
SH1-F7 →	– EROM		

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

TITLE: PW ASSY, HPRO3
MODEL: HYTERM

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

TITLE
PW ASSY, HPR03

MODEL
HYTERM
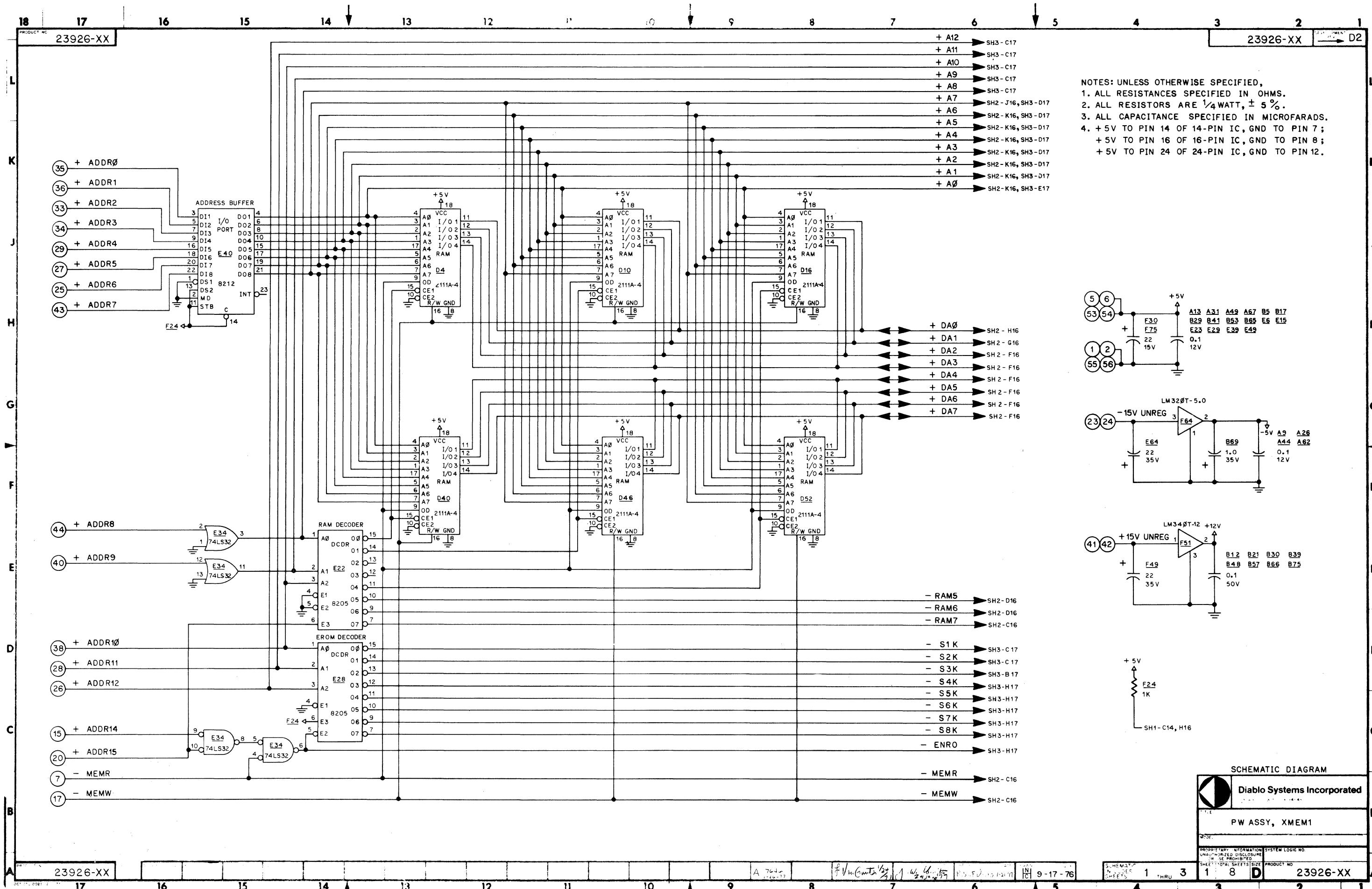
REVISION HISTORY - #23924-XX HPRO3 Board

Rev. A   ECO#   7648   As released.

     B   7690   Change resistor F24 from 1K to 8.2K; add resistor F25 from
                          -OPTION D to +5V.

   C   7759   Correct error on bill of material (diode A28 omitted); add
                          "on" indication to S1-S4 on sheet 3 of schematic; correct
                          note 5 on sheet 1 of schematic—specified "B7," should be
                          "B11." No changes to board.

     D   7771   Replace 74LS221 at A26 with 74LS123. Change resistor (A32)
                          and capacitor (A29), and remove diode (A28). Provides more
                          stable real-time clock.

     E   7816   Allow use of plastic ICs, No schematic changes.
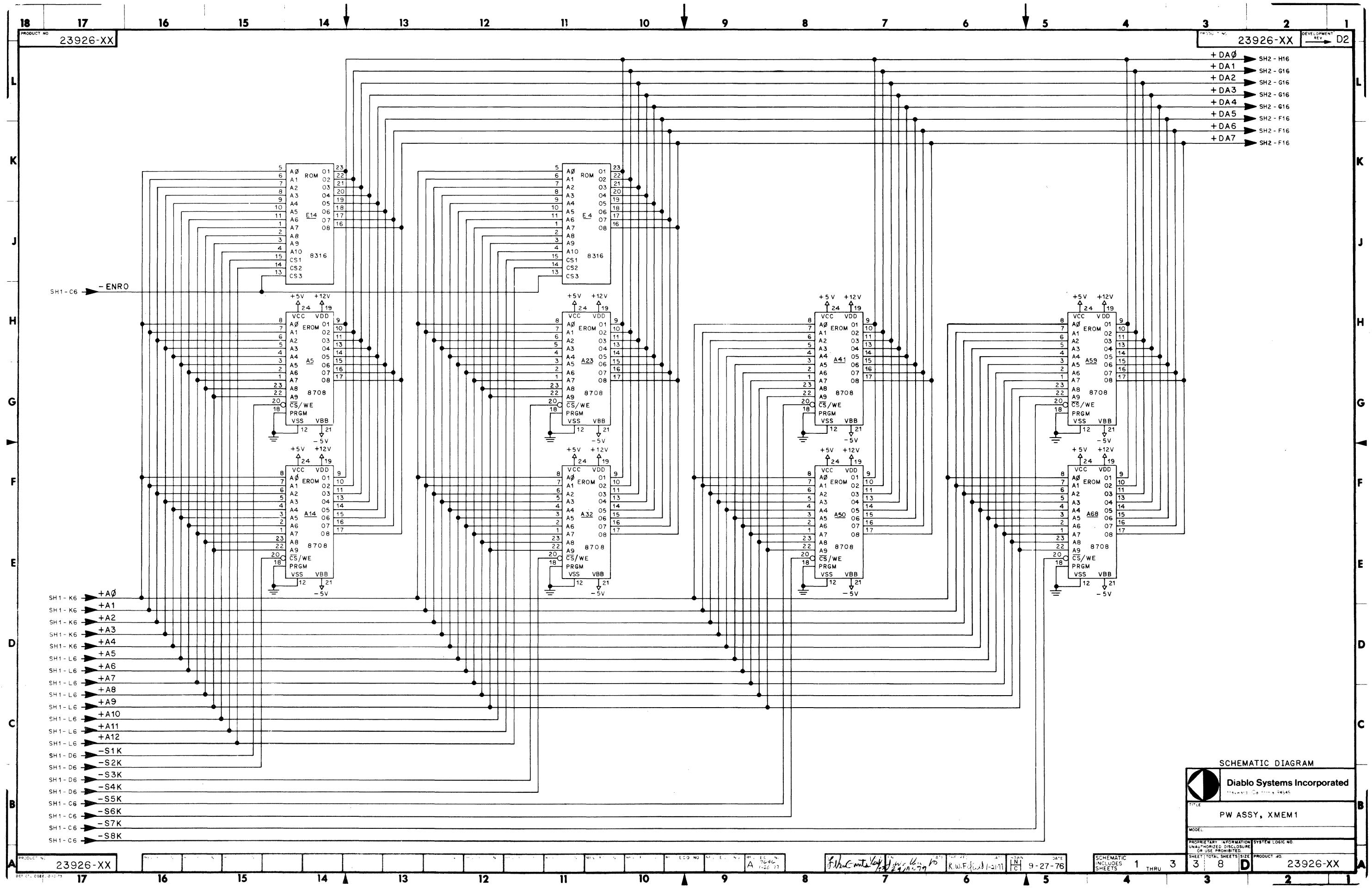
SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, XMEM1

23926-XX

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE ¼ WATT, ± 5 %.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. + 5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   + 5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8;
   + 5V TO PIN 24 OF 24-PIN IC, GND TO PIN 12.

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

TITLE

PW ASSY, XMEM1

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, XMEM1
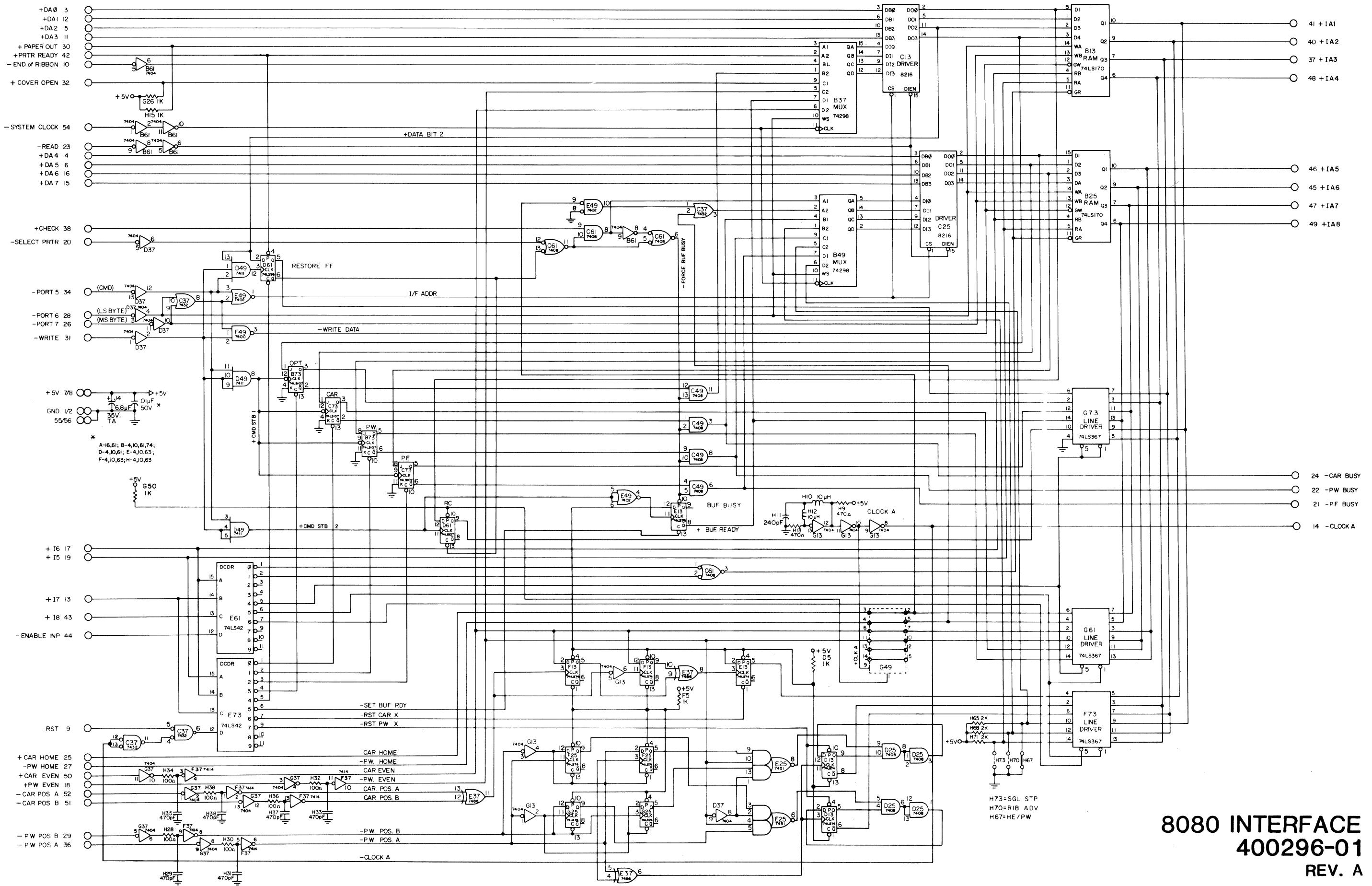
23926-XX

REVISION HISTORY - #23926-XX XMEM1 Board

Rev. A   ECO#   7646   As released.

     B   7852   Add dash numbers for 1641, 1660. No schematic changes.

8080 INTERFACE
400296-01
REV. A

REVISION HISTORY – $\frac{\text{\#40644-XX}}{\text{400296-01}}$ 8080 INTERFACE Board

40644-01

Rev. A   ECO#   9879   As released.

B   A1076   Jumper added from E15-3 to bottom end of inductor D6 to
                       allow oscillator to function: missing trace on circuit board.

C   A1096   (1) Add inverter on CLK input to Buffer Busy flip-flop to
                            delay setting until trailing edge of -WRITE pulse.
                       (2) Add gate to qualify -RST input to Reset Decoder with
                            CLOCK A.
                       (3) Change source of -SET BUF READY from Command
                            Decoder to Reset Decoder (from $\overline{16} \cdot \overline{17} \cdot \overline{18}$ to $\overline{15} \cdot 16 \cdot$
                            17): required due to microprogram change on LOGIC-2.
                       (4) Change clear of Ribbon Control flip-flop from Reset
                            Decoder to reset output of RSTR flip-flop: to drop
                            ribbon on Restore operation.

                                    NOTE

                       Rev. C or later requires Rev. K or later LOGIC-2 board (40510-43).

40644-03

Rev. D   ECO#   A1120   Circuit board revised: all IC locations changed; 74174 eliminated;
                          7404, 7414, and 7432s added to CAR & PW inputs for noise
                          immunity; CAR & PW CNTR CTRL circuits modified to allow
                          printwheel to turn without loss of PW position in memory.

40644-04
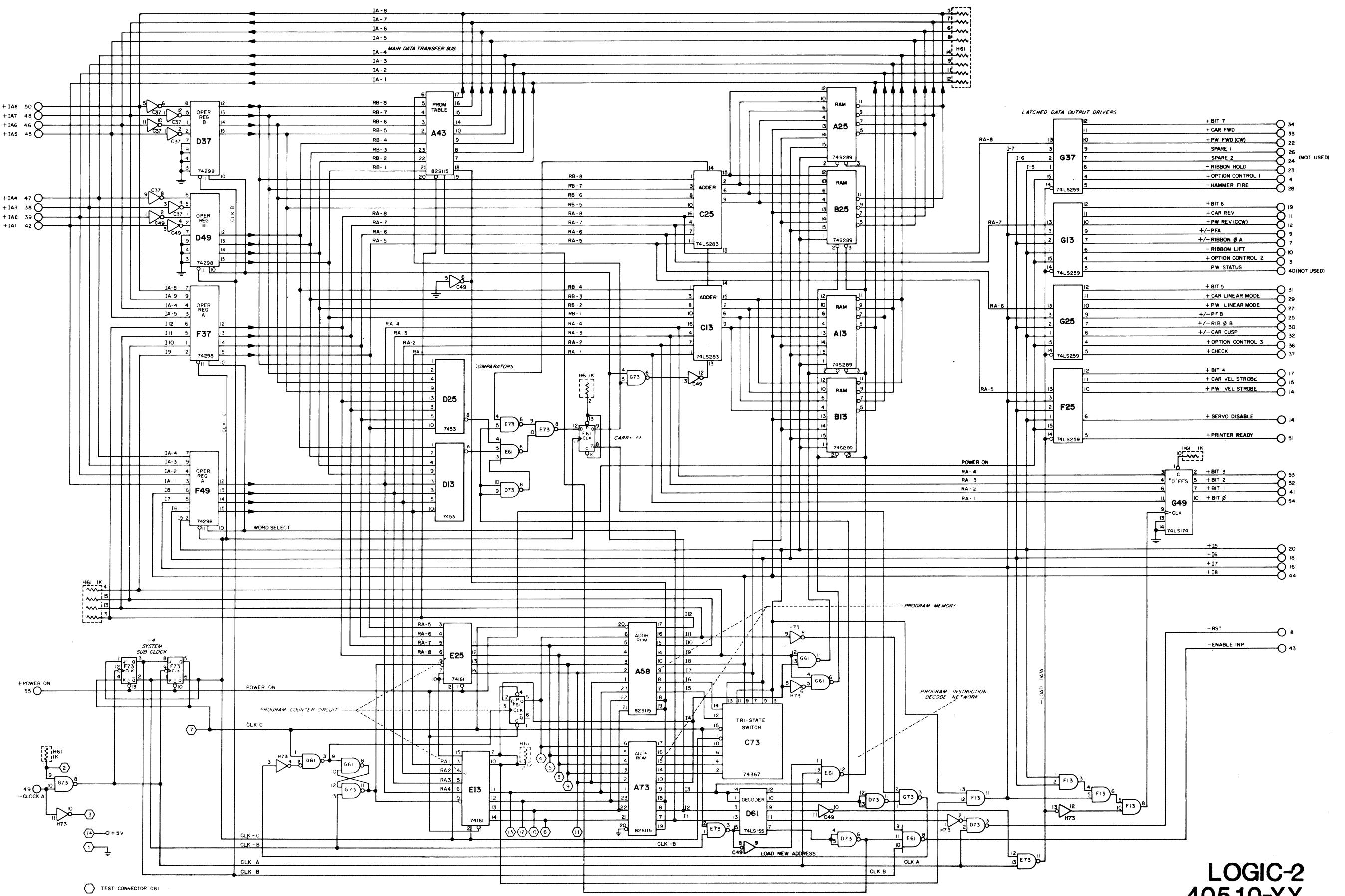
Rev. A   ECO#   A3103   Rework board to reroute +PW DECR signal (D13-6) away from data
                          bus to prevent crosstalk. No schematic changes.

40644-05

Rev. A   ECO#   A3103   Make circuit etch changes to reroute +PW DECR signal away
                          from data bus. No schematic changes.

400296-01

Rev. A   ECO#   7911   Same board as 40644-05 with jumper H67 added (to allow
                          direct addressing of printwheel position and hammer energy).

LOGIC-2
40510-XX
REV. Z

Rev. M	ECO#9988	Revise documentation and assembly to move ROM's for heat consideration; change to axial lead bypass capacitors; revise RESET logic; and improve fan out.
N	A1274	Revise PROM program to correct problem of failing to recognize PBV command.
P	A1247	(1) Change circuit to enable Table ROM (A43-19) only when it is to be read (was previously enabled also when RAM was accessed); lengthen IC life.
		(2) Add delay (via H73-12) to eliminate possible race condition on Bit 0 — Bit 3 output latches.
		(3) Add delay (via C49-9) to increase RAM address hold time from $\approx$ 5 ns to $\approx$ 20 ns.
Q	A1444	
R	A1523	
S	A1501	ROM changes for other HyType II models; not applicable to 1340A. No
T	A1578	schematic changes.
U	A1622	
V	A1841	
W	A1879	
X	A1945	
Y	A1977	ROM change to lower maximum carriage/paper feed velocity slightly, to prevent possible missing of incr/decr pulse.
Z	A3093	Allow use of ceramic ROMs to improve reliability; ROM changes for other HyType II models. No schematic changes.
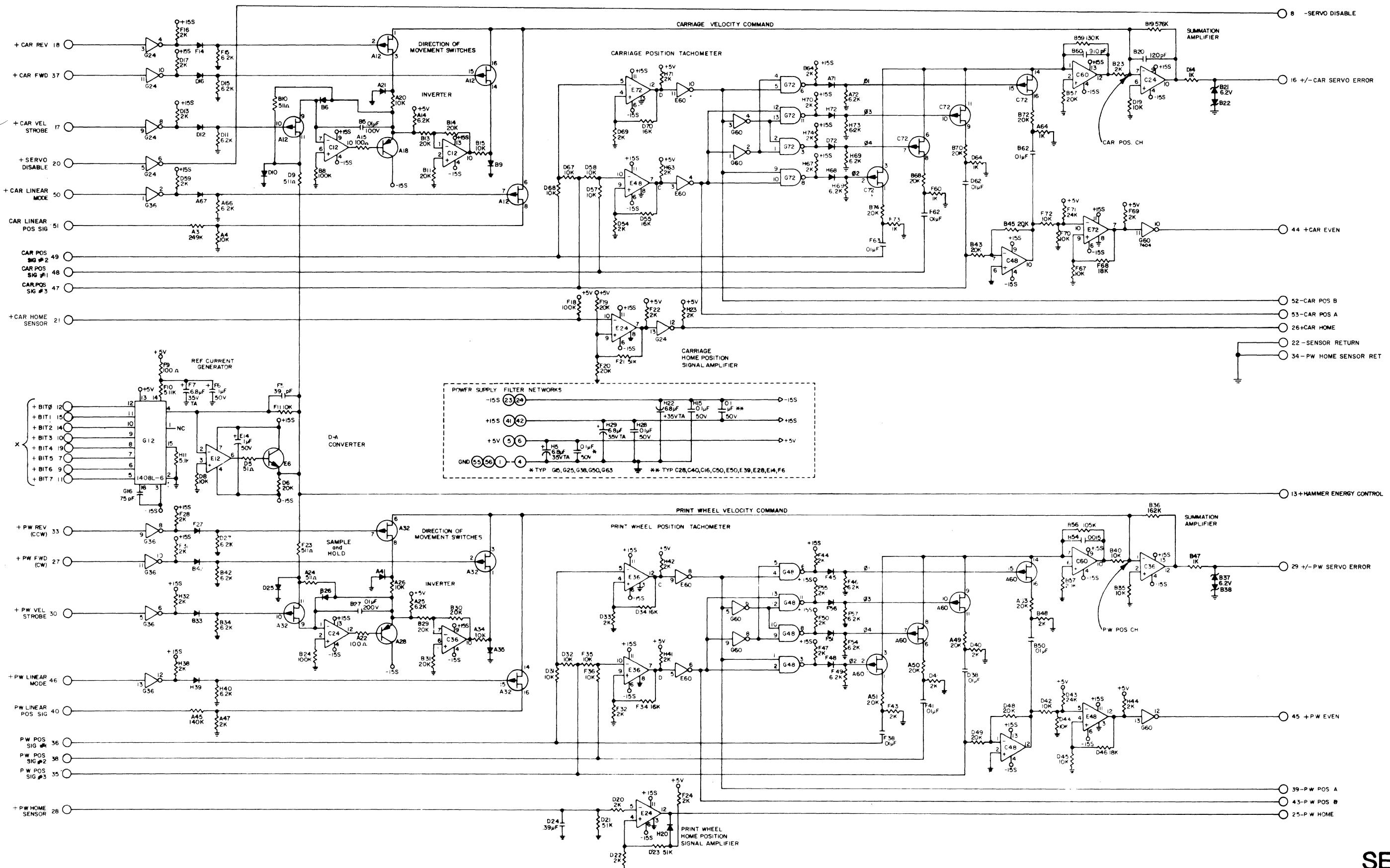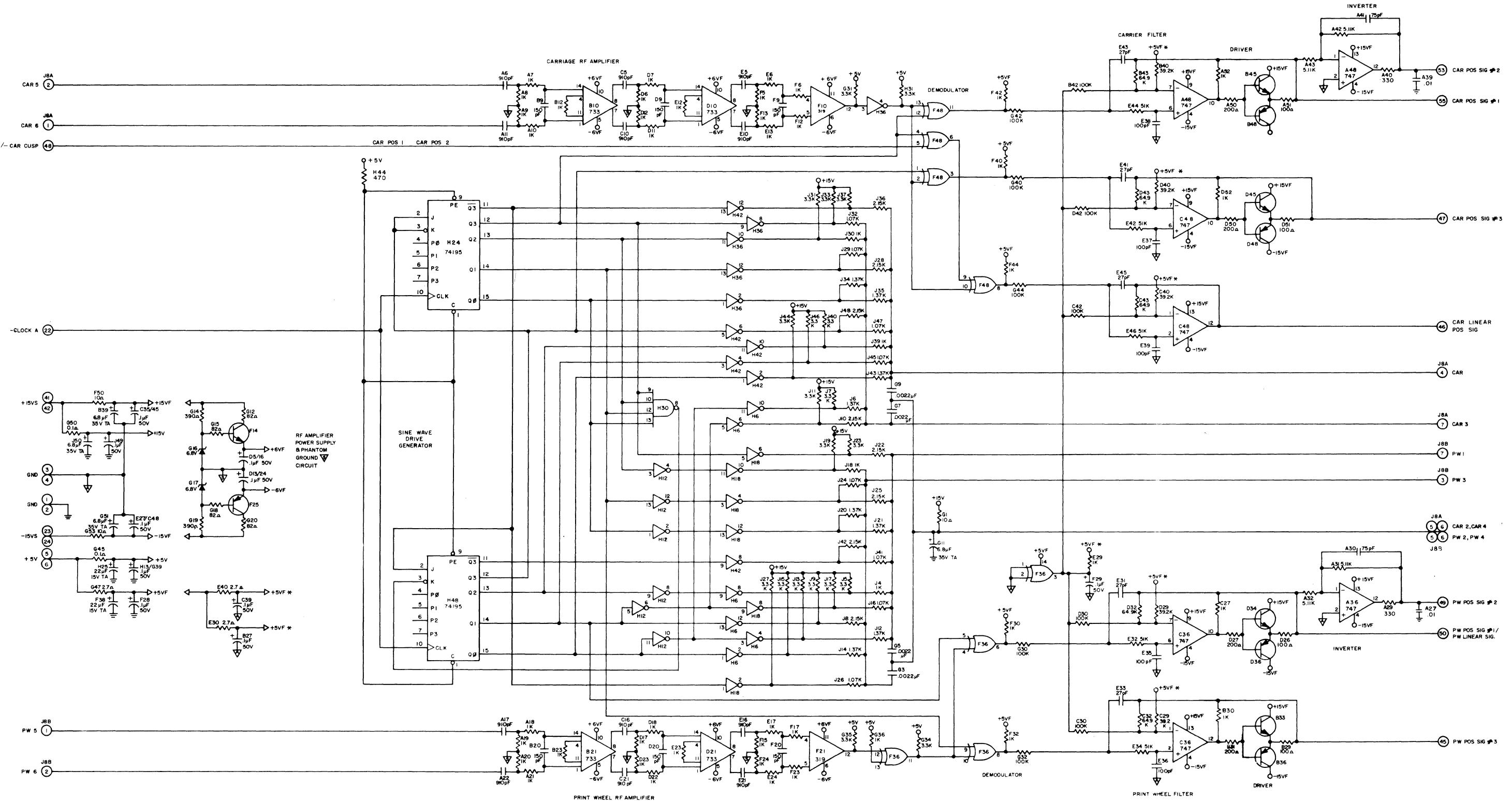
SERVO
40520-04
REV. N

Rev. M   ECO#9923   New artwork, minor component changes; prevents possible motor burnout following component failure.

     N   A1504   Remove assembly number from etch; this circuit also used for other assemblies. No schematic changes.

XDCR
405 15-03
REV. A

REVISION HISTORY — #40515-01 TRANSDUCER BOARD
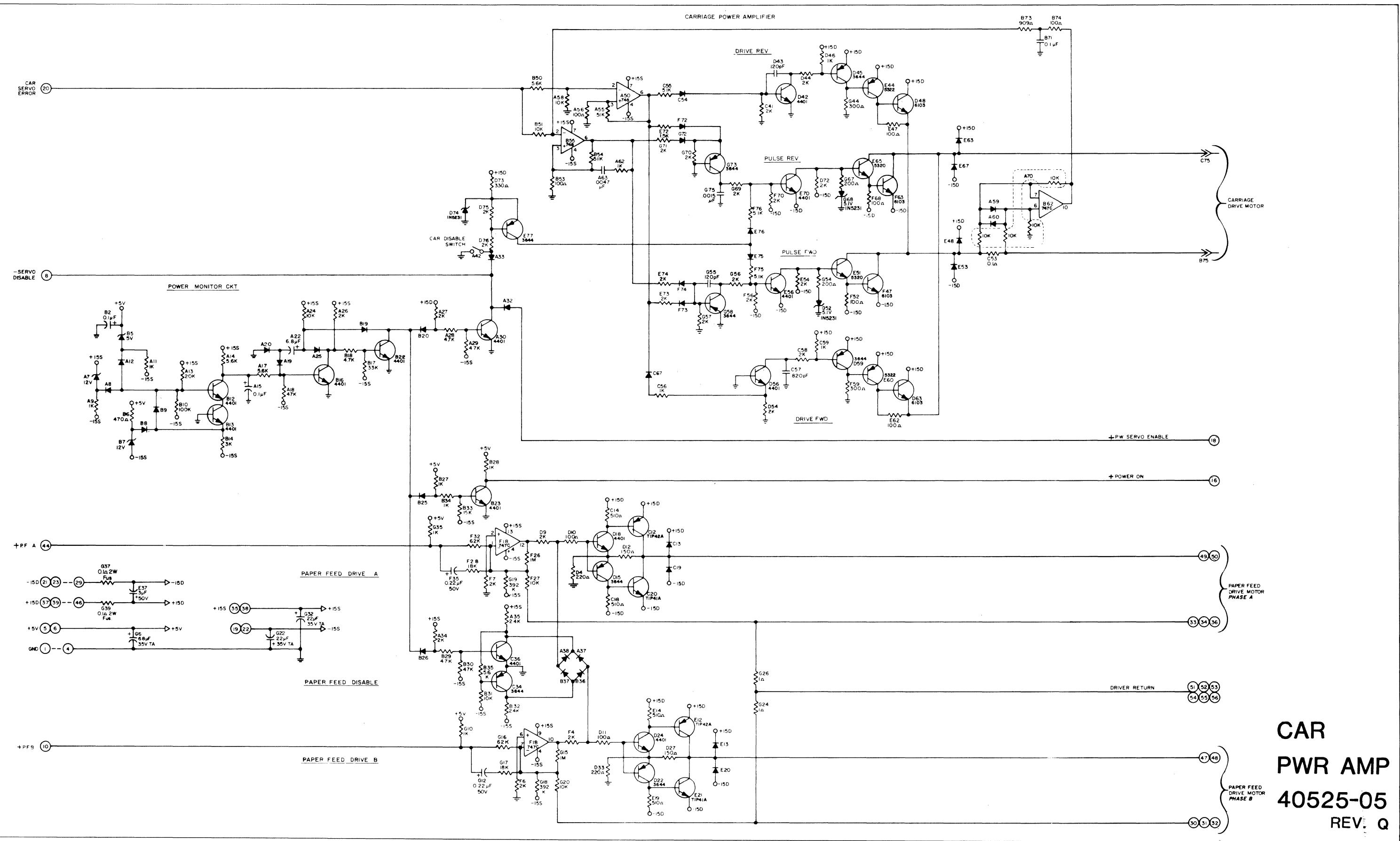
Rev. A   ECO#9742   B/M and Assembly as Released.

      B   9830   Revise documentation and Assembly to change resistor type at G1 from film to composition. Cut "Key" pins on connectors J8A and B.

      C   A1483   Change transistor at F25 from 2N5322L to 2N5322. Correct several schematic errors.

#40515-02

Rev. A   ECO#A1695   Add .01 μf capacitors from CAR POS SIG #2 (pin 53) and PW POS SIG #2 (pin 49) to GND. Change series resistors A40 and A29 (same circuits) to 330 ohms. To increase noise immunity of op amps; eliminate printwheel retry. Change -01 to -02; change revision level to Rev. A.

#40515-03

Rev. A   ECO#A1720   Change circuit board and artwork to accomodate changes incorporated in -02 (ECO#A1695). Change location of capacitor A28 to A27.

CAR
PWR AMP
40525-05
REV. Q

REVISION HISTORY - # 40425-05 CARRIAGE POWER AMPLIFIER PCB ASSEMBLY

Rev. N   ECO#   A1260   Revise schematic, documentation and assembly. Change

        B33   from 75K to 15K
  F32/G16   from 82K to 62K
  G18/G19   from 523K to 392K
      G56   from   2K to 1K
Label G52 and G68 5.1V. Remove -5.1V line from
junction G52 and G54.
Change from -XX to -05.
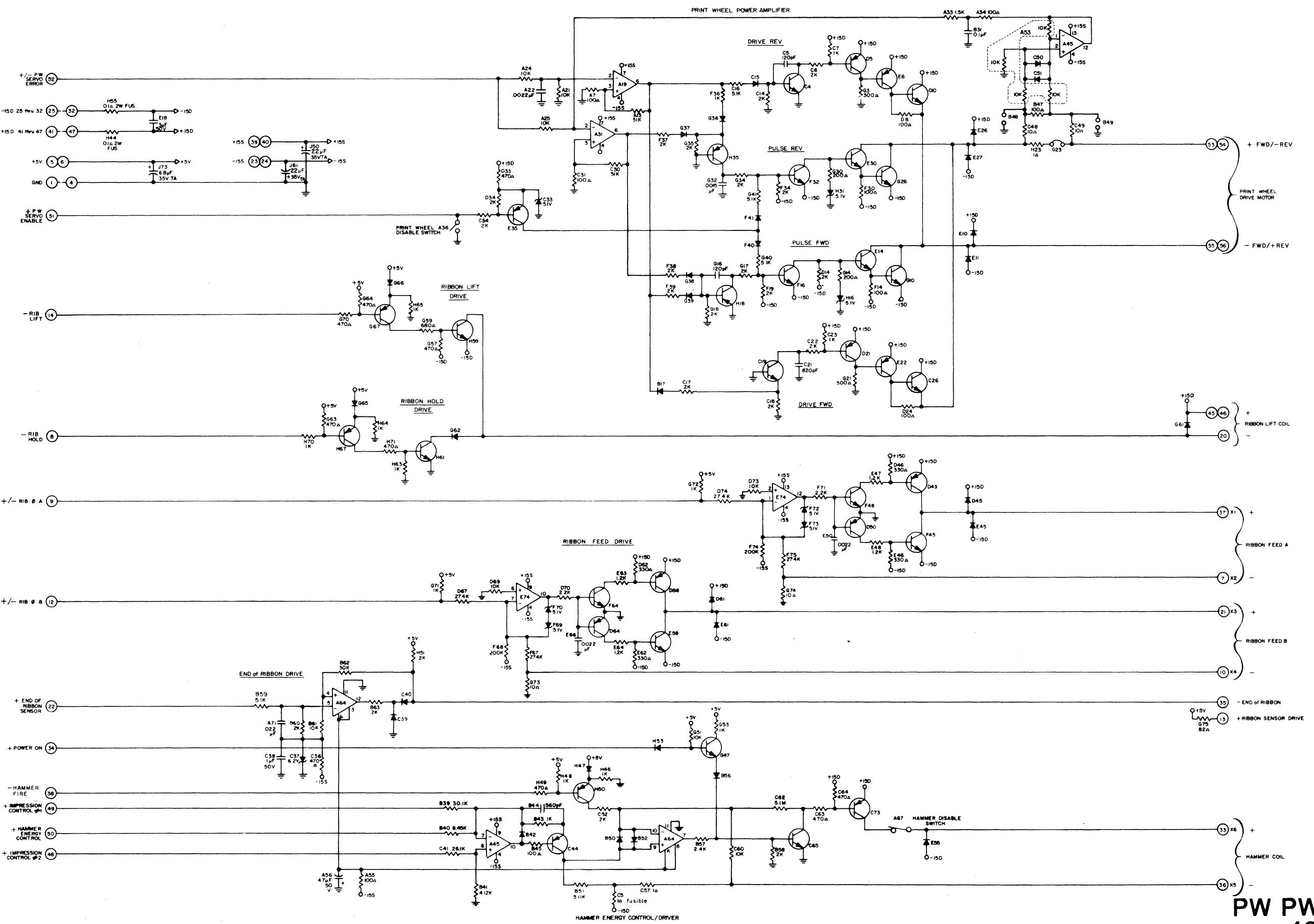
P   A1260A   Correct error on B/M. No schematic or part changes.

Q   A1565   Correct error on B/M. No schematic or part changes.

#40525-06

Rev. A   ECO#   A3128   Change circuit board and artwork to accomodate changes
                           for the other HyType IIs. Only schematic changes
                           are in the following locators:

WAS	IS
C54	B46
C55	B47
C56	B44
C57	A44
D54	A45
D56	A47
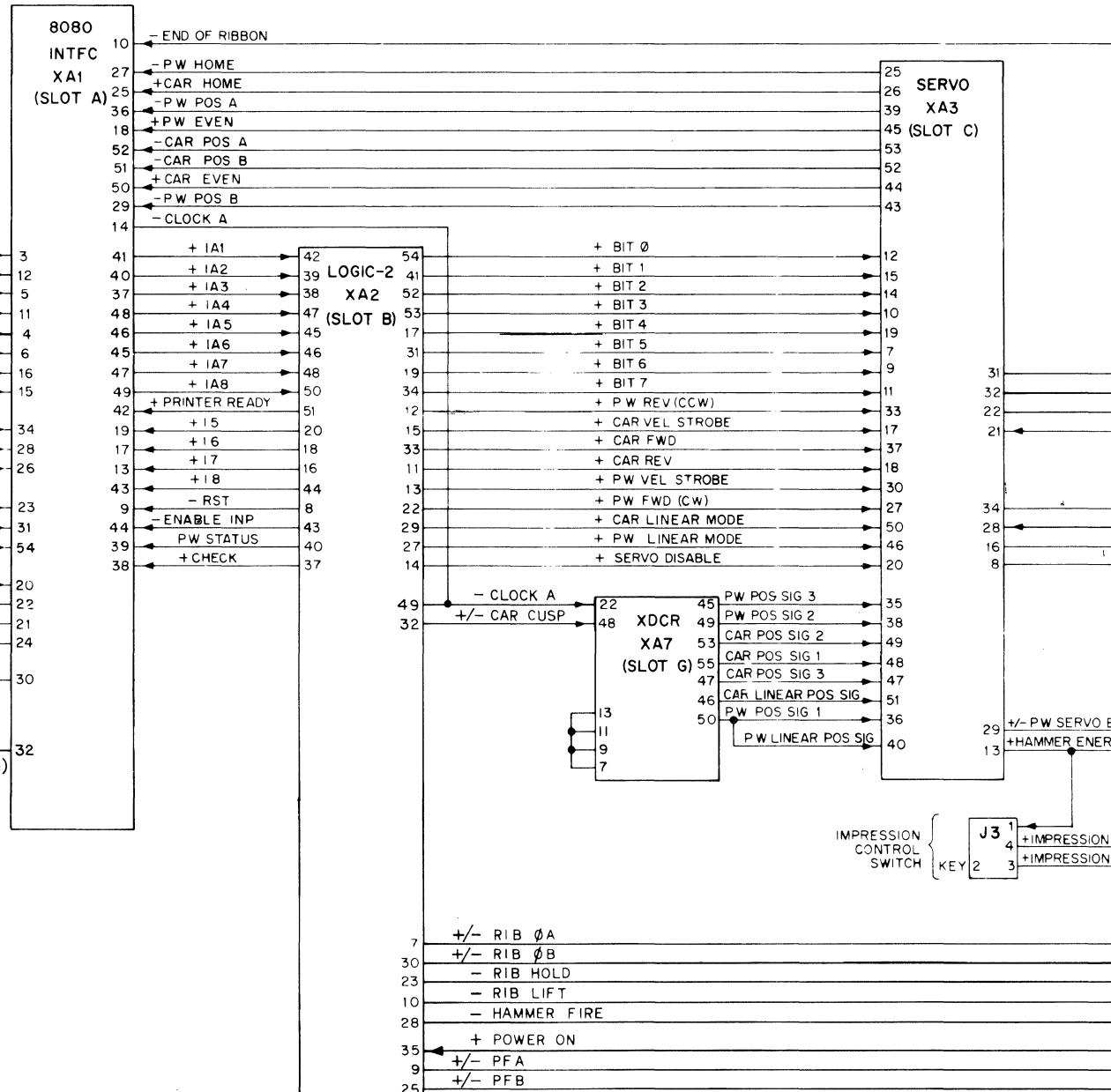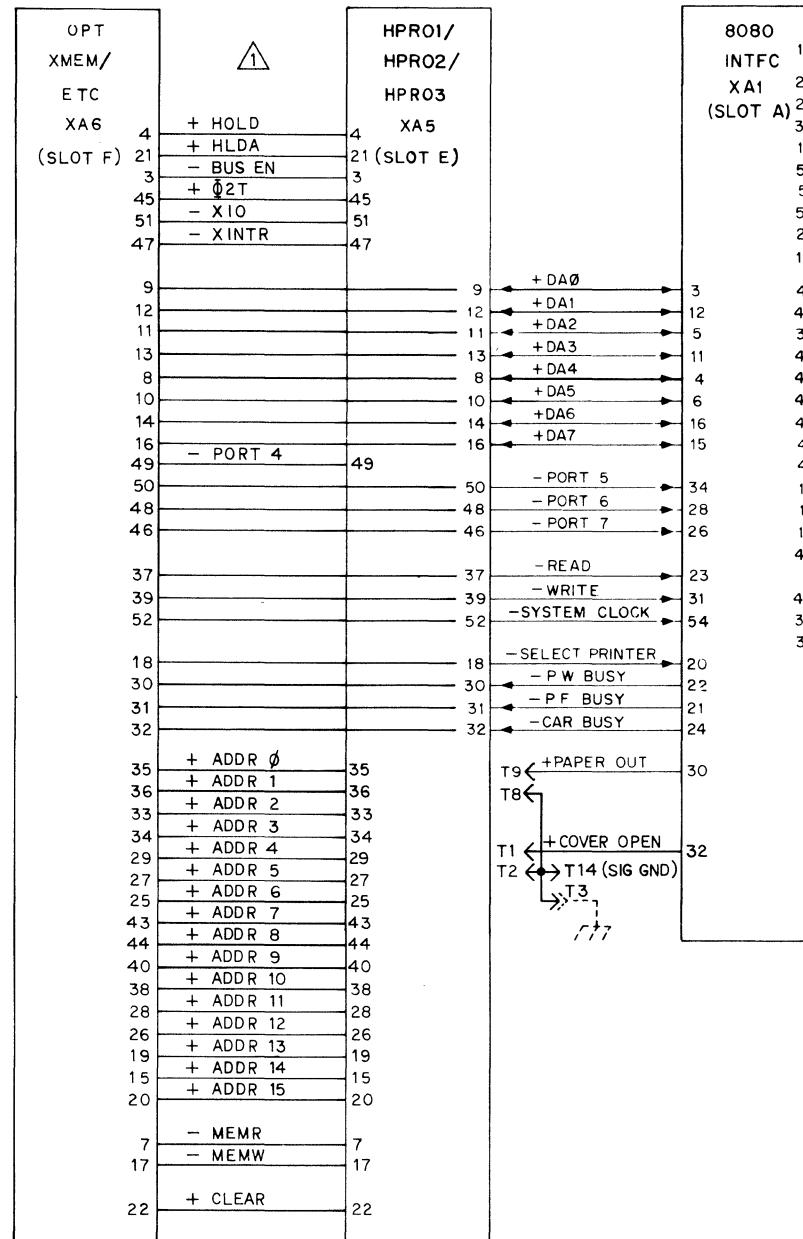
PW PWR AMP
40530-06
REV. R

REVISION HISTORY — # 40530-06 PRINT WHEEL POWER AMPLIFIER PCB ASSEMBLY

Rev. M   ECO#A1030   Revise documentation and assembly to allow use of # 40531-06 PCB for # 40530-02 Assembly.

     N   A1050   Revise documentation and assembly to change Zener Diode C37 from a 6.8 volt ½W to a 6.2 volt 1W device.

     P   A1123   Revise documentation and assembly. Change C34 from 5.1K to 2K. Allow power up sequencing when using power supplies with a low current foldback.

     Q   A1230   Revise documentation and assembly. Delete C68, D68, D72, D75, E75 and F66. Change F67 and F75 from 10K to 27.4K. Correct ribbon drive problems. Change drawing No. from 40530-XX to 40530-06.

40530-07

Rev. R   ECO#A1413   Remove .01 μ f capacitors from B46, B49 (printwheel drive motor feedback circuit). To help eliminate printwheel retries.

POWER DISTRIBUTION

CONNECTOR
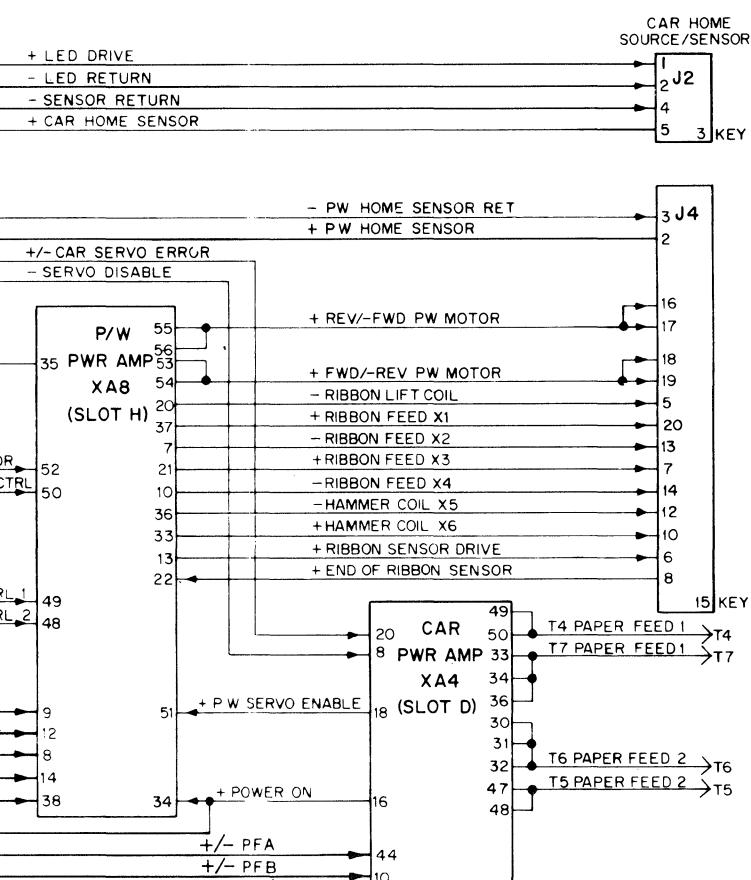
VOLTAGE	J4	XA1	XA2	XA3	XA4	XA5	XA6	XA7	XA8	TERM
SIGNAL GROUND	11 —	1,2 33,35 55,56	1,2 55,56	1-4 55,56	—	1-2 55,56	1-2 55,56	1-4	—	T2,T3 T8,T14
+5V	—	7,8	5,6 21	5,6	5,6	5,6 53,54	5,6 53,54	5,6	5,6	T15
+15VS	—	—	—	41,42	35,38	41,42	41,42	41,42	39,40	T12
-15VS	—	—	—	23,24	19,22	23,24	23,24	23,24	23,24	T11
+15VD	4,9	—	—	—	37,39-43, 45,46	—	—	51,52	41-47	T12
-15VD	—	—	—	21,23-29	—	—	—	27,28	25-32	T11
ANALOG GND	—	—	—	1-4	—	—	—	—	1-4	T13
DRIVER RETURN	—	—	—	51-56	—	—	—	—	—	T14

NOTES:

⚠ All pins of XA5 connected to corresponding pin # of XA6.

2 Pin designations start at center of motherboard, with even numbers on the component side of the board.

MOTHER BOARD 46080-01
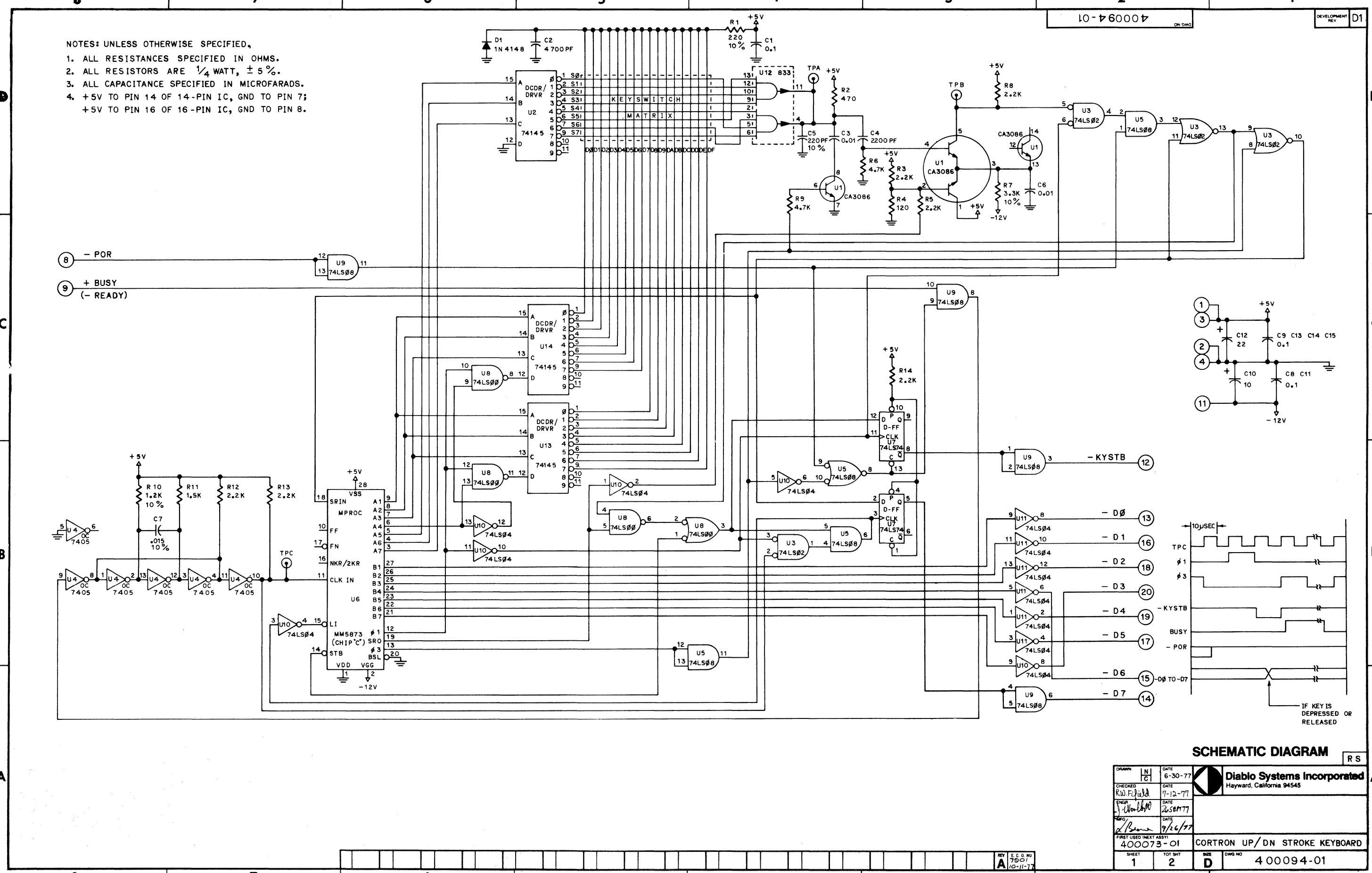
REVISION HISTORY — #46080-01 MOTHER BOARD

Rev. A   ECO#A1759   As released.

B   A1869   Correct error in part no. on bill of material. No change to board.

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE ¼ WATT, ± 5 %.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
5. ALL LIGHT EMITTING DIODES ARE MV5753
   OR EQUIVALENT, EXCEPT CR13 WHICH IS A
   5082-4955 OR EQUIVALENT.

6. REFERENCE SCHEMATIC PACKAGE FOR
   SPECIFIC ASSIGNMENTS OF LEDS
   AND SWITCHES.

+5V
(19)(20) +5V
(17)(18) GND
C1 22 15V
C2,C3, C4 0.1 12V
R13 150
CR13 POWER
+5V

U2 1K

+5V 26 VCC
I/O INTFC
U1
8255
GND 7

SW 1 PA0 4
SW 2 PA1 3
SW 3 PA2 2
SW 4 PA3 1
SW 5 PA4 40
SW 6 PA5 39
SW 7 PA6 38
SW 8 PA7 37
SW 9 PC0 14
SW 10 PC1 15
SW 11 PC2 16
SW 12 PC3 17

S3 S2 S1

D0 34 + DA 0 (3)
D1 33 + DA 1 (2)
D2 32 + DA 2 (7)
D3 31 + DA 3 (8)
D4 30 + DA 4 (6)
D5 29 + DA 5 (5)
D6 28 + DA 6 (10)
D7 27 + DA 7 (12)

PB0 18
PB1 19
PB2 20
PB3 21
PB4 22
PB5 23
PB6 24
PB7 25
PC4 13
PC5 12
PC6 11
PC7 10

7416 (U4, U5)

CR9 LED 1   R9 150
CR8 LED 2   R8 150
CR7 LED 3   R7 150
CR6 LED 4   R6 150
CR5 LED 5   R5 150
CR4 LED 6   R4 150
CR3 LED 7   R3 150
CR2 LED 8   R2 150
CR10 LED 9 R10 150
CR11 LED 10 R11 150
CR12 LED 11 R12 150
+5V

E5 DS1 BUZZER E6
C5 22 35V
R1 1K
CW
CR1 1N4454

(1) - CLR   1 U3 2 35 RST 74LS04
(11) - RD   5 RD
(4) - WR   36 WR
(14) + ADDR 0 9 A0
(15) + ADDR 1 8 A1
(16) - PORT 3 6 CS

(13) + 12V

SPARES:
5 U3 6 74LS04
3 U3 4 74LS04
9 U3 8 74LS04
11 U3 10 74LS04
13 U3 12 74LS04

REVISION HISTORY - #400056-01 CONTROL PANEL ASSY.

Rev.	A	ECO#	7788	As released.
	B		7838	Wire S1-1 direct to U1-17; S1-15 to GND; remove quick disconnect terminals E1-E4: simplifies wiring of Cover-Open and Paper-Out switches. Other mechanical changes to assy. Requires firmware change.
	C		7894	Correct drawing errors on sheet 2. No schematic changes.

SCHEMATIC DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE ¼ WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.

SCHEMATIC DIAGRAM

				S0	S1	S2	S3	S4	S5	S6	S7	
BIT 7 →				0	0	0	0	1	1	1	1	SENSE ADDRESS
BIT 6 →				0	0	1	1	0	0	1	1	
BIT 5 →				0	1	0	1	0	1	0	1	

B4↓	B3↓	B2↓	B1↓	⊠	S0	S1	S2	S3	S4	S5	S6	S7	
0	0	0	0	D0	⊠	35	37	39	45	43	41	32	ALPHA/NUMERIC OUTPUT B7=0
0	0	0	1	D1		52	54	56	TEST CORE D2 61	63	58	50	
0	0	1	0	D2	⊠	36	38	40	46	44	42	34	
0	0	1	1	D3	17	21	23	25	31	29	27	19	
0	1	0	0	D4	⊠	20	22	24	30	28	26	18	
0	1	0	1	D5	1	5	7	9	15	13	11	3	
0	1	1	0	D6	2	6	8	10	16	14	12		
0	1	1	1	D7	47	51	53	55	62	59	57	SHIFT SHIFT SHIFTLOCK 33 49 60	
1	0	0	0	D8								76	RIGHT HAND PAD OUTPUT B7=1 B3=0
1	0	0	1	D9	73	70	67	64				77	
1	0	1	0	DA	74	71	68	65				78	
1	0	1	1	DB	75	72	69	66				79	
1	1	0	0	DC	90	87	84	81				93	LEFT HAND PAD OUTPUT B7=1 B3=1
1	1	0	1	DD	91	88	85	82				94	
1	1	1	0	DE				TEST CORE D1 48				95	
1	1	1	1	DF	89	86	83	80				92	

DRIVE ADDRESS
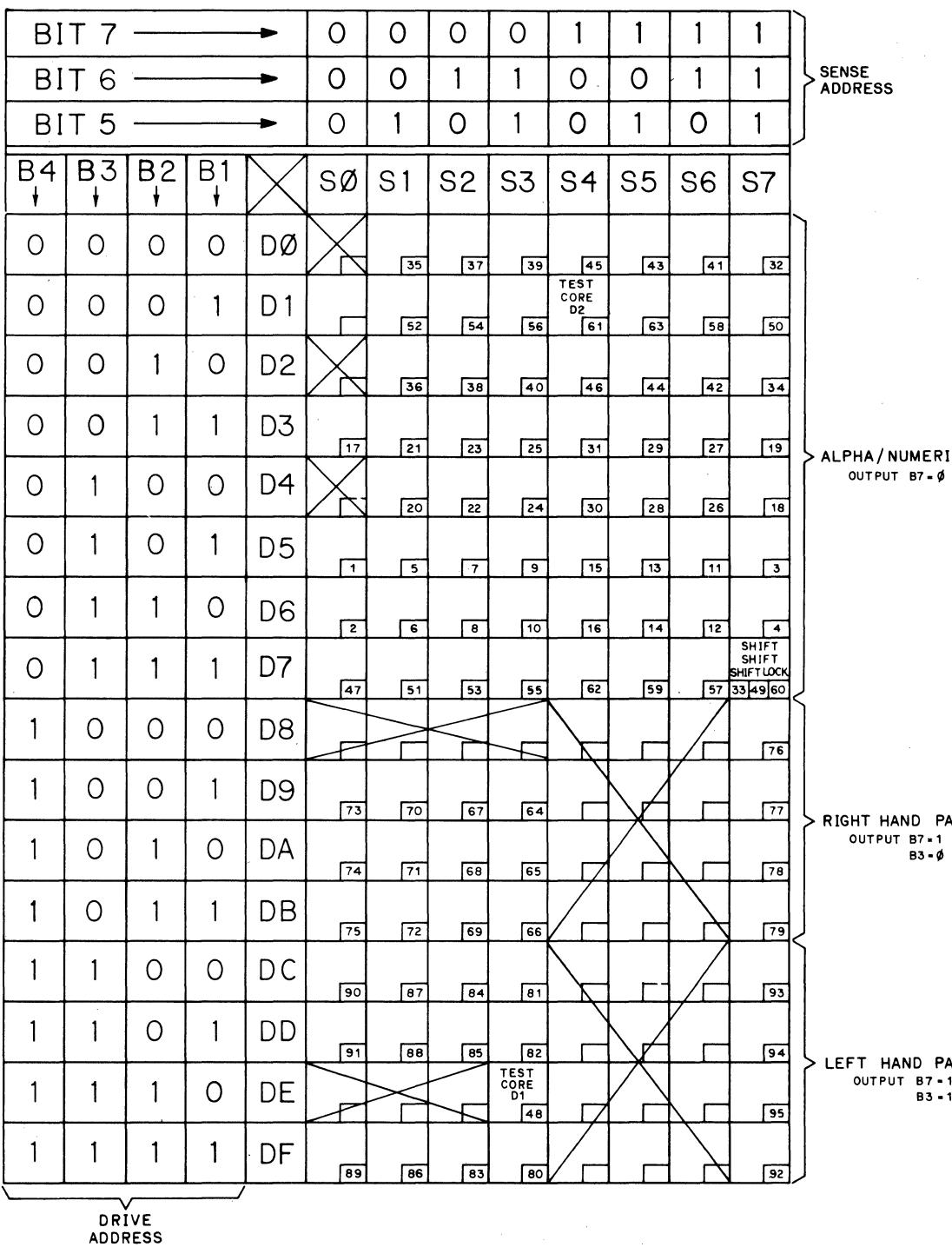
NOTE:

MATRIX	OUTPUT CODE
B1	B1
B2	B2
B3	B3
B7	B4
B5	B5
B6	B6
B4	B7

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

TITLE
POWER SUPPLY, BOSCHERT U.L.,
115V/220V

MODEL
1610 / 1620

DRAWINGS FURNISHED BY BOSCHERT ASSOCIATES
FOR MAINTENANCE PURPOSES ONLY.

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. ◇ DENOTES PRIMARY CIRCUIT COMMON RETURN.
5. SELECT TEST RESISTOR.
6. INSTALL JUMPER FOR 115V (-01) OPERATION ONLY.
7. INSTALL COMPONENTS FOR 220V (-02) OPERATION ONLY.
8. USE COMPONENT VALUES IN PARENTHESES FOR 220V (-02) OPERATION ONLY.
9. USE ONLY UNGROUNDED TEST INSTRUMENTS WHEN TROUBLE-SHOOTING PRIMARY CIRCUITS
   (ALL CIRCUITS OTHER THAN OUTPUT RECTIFIER AND FILTER, OVER VOLTAGE AND +5V ERROR AMPLIFIER).
10. ALTERNATE REFERENCE DESIGNATORS SHOWN IN PARENTHESES ((CR8), (A1), ETC.)
    REFER TO SILKSCREENED INFORMATION ON SOME CIRCUIT BOARDS.

REFERENCE DESIGNATION

LAST USED	NOT USED
C45	C15,16,21,24, 26,27,28,29
CR28	CR23, 24,25,26
F1	
L6	
Q20	Q12
R70	R21,37,42, 50,52,53,55
RT1	
SCR1	
T6	T3
U3	
VR2	

NOTES:
1. CIRCUITRY (BACKGROUND) SHOWN IS LOCATED ON FAR SIDE.
2. DRAWINGS FURNISHED BY BOSCHERT ASSOCIATES FOR MAINTENANCE PURPOSES ONLY.

115V A.C. VERSION
(26021-01)

TB1
1 [+5V]
2 [GND]
3 [GND]
4 [+15V]
5 [−15V]
6 [N.C.]
7 [CHAS GND]
8 [A.C. HOT]
9 [A.C. NEUT.]

ASSEMBLY DRAWING

DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE
LINEAR · ANGULAR ·
MATERIAL
HEAT TREAT
FINISH

DRAWN MATSUMOTO 11/11/76
CHECKED
ENGR
NEXT ASSY. 26022

Diablo Systems Incorporated
Hayward, California 94545

POWER SUPPLY
BOSCHERT, U.L.

SCALE NONE   SHEET 3   TOT SH 4
SIZE D   26021-XX

NOTES:
1. CIRCUITRY (BACKGROUND) SHOWN IS LOCATED ON FAR SIDE.
2. DRAWINGS FURNISHED BY BOSCHERT ASSOCIATES FOR MAINTENANCE PURPOSES ONLY.

(P1)

TB1
1 [+5V]
2 [GND]
3 [GND]
4 [+15V]
5 [−15V]
6 [N.C.]
7 [CHAS GND]
8 [A.C. HOT]
9 [A.C. NEUT.]

220 V.A.C. VERSION
(26021-02)
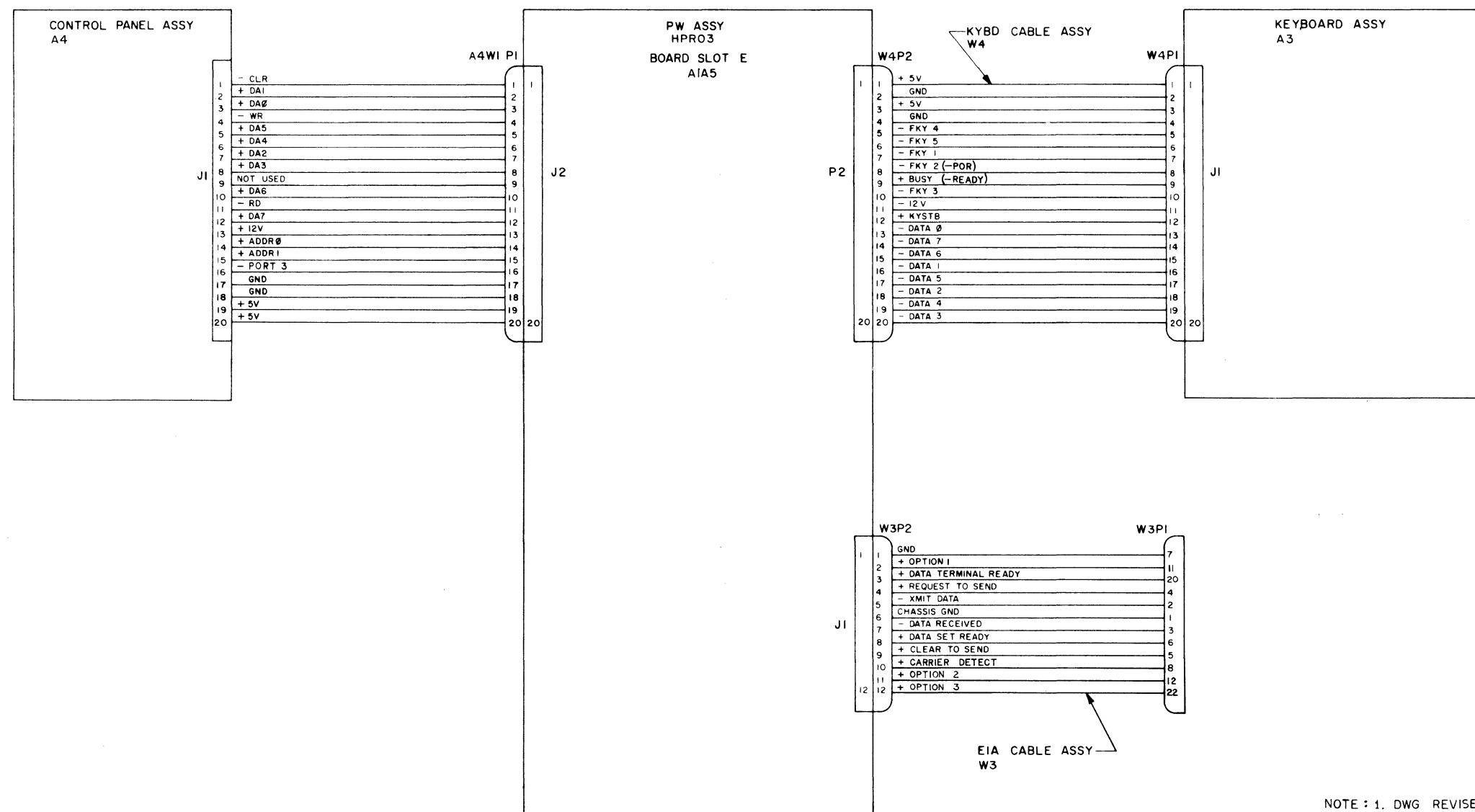
ASSEMBLY DRAWING

REVISION HISTORY - #26021-XX POWER SUPPLY

Rev.   A   ECO#   7472   As released

          B   7504   Add requirement for label containing part number, serial number, and mfg. date code.

          C   7587   Add special label to 220V units.

          C1   7631   Add schematic and assembly drawings to part no.

          C2   7700   Correct minor schematic errors, add alternate reference designators.

          C3   7758   Correct error on connection drawing, sheet 1.

          C4   7899   Move cathode of diode CR27 from input to output of L4; reduces 5V ripple.
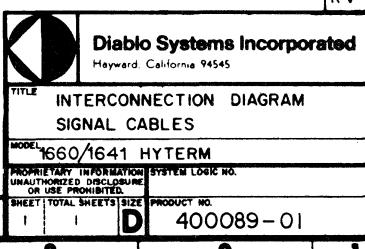
Make the following component changes:
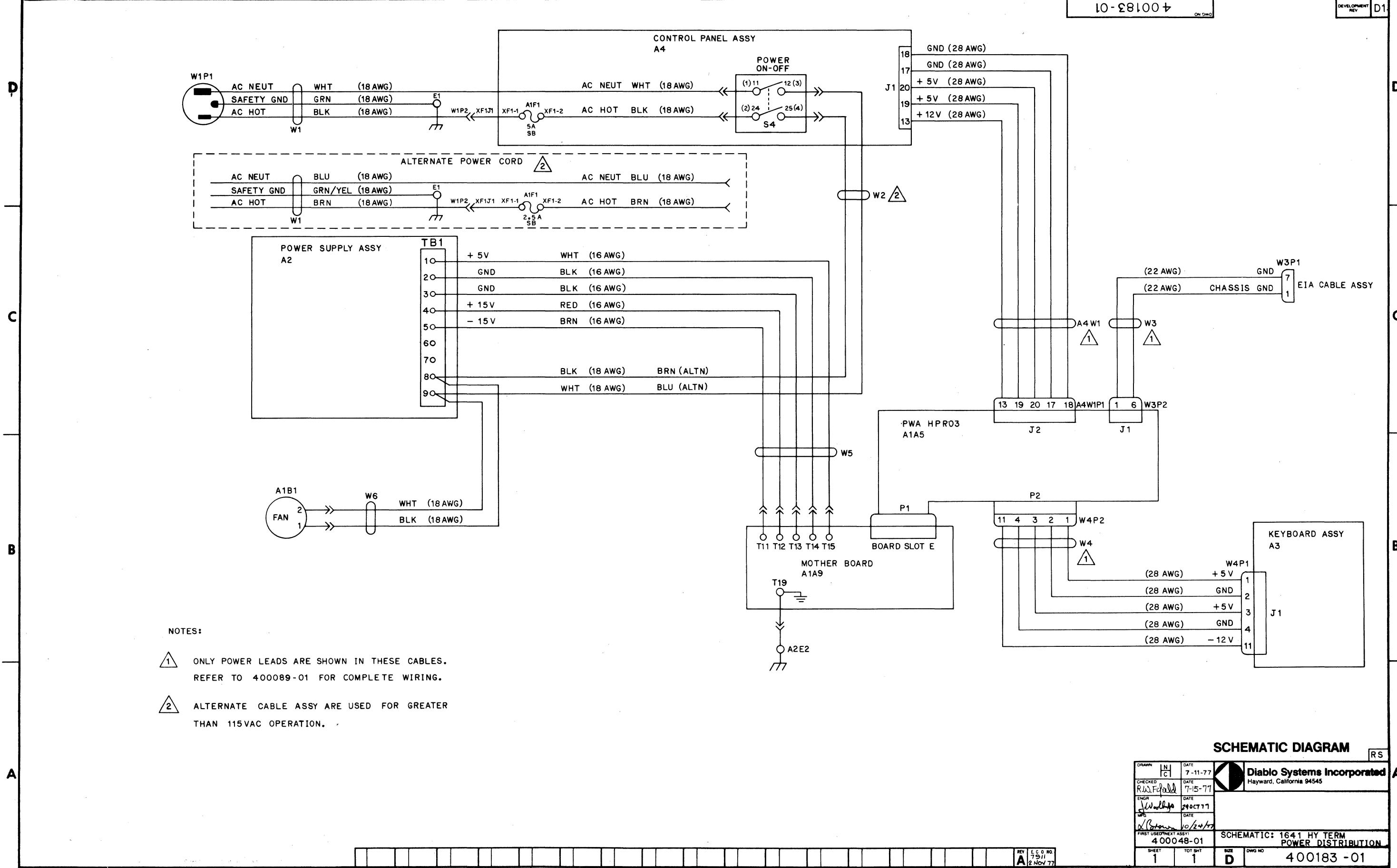
Component	Was	Is
R3,R4,R5	¼ Watt	1 Watt
Q1	SJ7280(2N6308)	SJ7280(2N6545)
Q3,Q4	MPSA93	MPSU60
CR19,CR20	1N3889	SR3142
R8	22K	39K
R9	22K	22K(39K)
R19	160(33)	160(68)
R22	10(2.2)	10(4.7)

NOTE: Component values in parentheses are for 220V operation

CONTROL PANEL ASSY
A4

PW ASSY
HPRO3

BOARD SLOT E
A1A5

A4W1 P1

J1			J2
1	− CLR	1	2
2	+ DA1	2	3
3	+ DA0	3	4
4	− WR	4	5
5	+ DA5	5	6
6	+ DA4	6	7
7	+ DA2	7	8
8	+ DA3	8	9
9	NOT USED	9	10
10	+ DA6	10	11
11	− RD	11	12
12	+ DA7	12	13
13	+ 12V	13	14
14	+ ADDR0	14	15
15	+ ADDR1	15	16
16	− PORT 3	16	17
17	GND	17	18
18	GND	18	19
19	+ 5V	19	20
20	+ 5V	20	20

KYBD CABLE ASSY
W4

KEYBOARD ASSY
A3

W4P2   W4P1

P2			J1
1	+ 5V	1	2
2	GND	2	3
3	+ 5V	3	4
4	GND	4	5
5	− FKY 4	5	6
6	− FKY 5	6	7
7	− FKY 1	7	8
8	− FKY 2 (−POR)	8	9
9	+ BUSY (−READY)	9	10
10	− FKY 3	10	11
11	− 12 V	11	12
12	+ KYSTB	12	13
13	− DATA 0	13	14
14	− DATA 7	14	15
15	− DATA 6	15	16
16	− DATA 1	16	17
17	− DATA 5	17	18
18	− DATA 2	18	19
19	− DATA 4	19	20
20	− DATA 3	20	20

W3P2   W3P1

J1			
1	GND	1	7
2	+ OPTION 1	2	11
3	+ DATA TERMINAL READY	3	20
4	+ REQUEST TO SEND	4	4
5	− XMIT DATA	5	2
6	CHASSIS GND	6	1
7	− DATA RECEIVED	7	3
8	+ DATA SET READY	8	6
9	+ CLEAR TO SEND	9	5
10	+ CARRIER DETECT	10	8
11	+ OPTION 2	11	12
12	+ OPTION 3	12	22

EIA CABLE ASSY
W3

NOTE : 1. DWG REVISED 11-77 SHOWING CORRECTED
ASSY REF DESIGNATORS. ECO PENDING.

RV

Diablo Systems Incorporated
Hayward, California 94545

TITLE
INTERCONNECTION DIAGRAM
SIGNAL CABLES

MODEL 1660/1641 HYTERM

REV	E.C.O. NO.
A	7901 10-11-77

MFG DATE 9/26/7 ENG J. Woolf DATE CHECKED R.W.Fifield 6/27/ DATE DRAWN R.L. 15 JUNE 77 DATE

SCHEMATIC INCLUDES SHEETS   THRU

SHEET 1 TOTAL SHEETS 1 SIZE D PRODUCT NO. 400089-01

SCHEMATIC DIAGRAM

NOTES:

⚠1 ONLY POWER LEADS ARE SHOWN IN THESE CABLES.
REFER TO 400089-01 FOR COMPLETE WIRING.

⚠2 ALTERNATE CABLE ASSY ARE USED FOR GREATER
THAN 115 VAC OPERATION.

DRAWN	N C	DATE 7-11-77	Diablo Systems Incorporated
CHECKED R.W.F...		DATE 7-15-77	Hayward, California 94545
ENGR J.W...		DATE 24 OCT 77	
MFG X.B...		DATE 10/24/77	
FIRST USED/NEXT ASSY 400048-01			SCHEMATIC: 1641 HY TERM POWER DISTRIBUTION
SHEET 1	TOT SHT 1	SIZE D	DWG NO 400183-01

REV A ECO NO 7911 2 NOV 77

REVISION HISTORY — MISCELLANEOUS WIRE & CABLE ASSEMBLIES
(Including 24471 Rev. C)

Rev. A   ECO=9684   As Released.
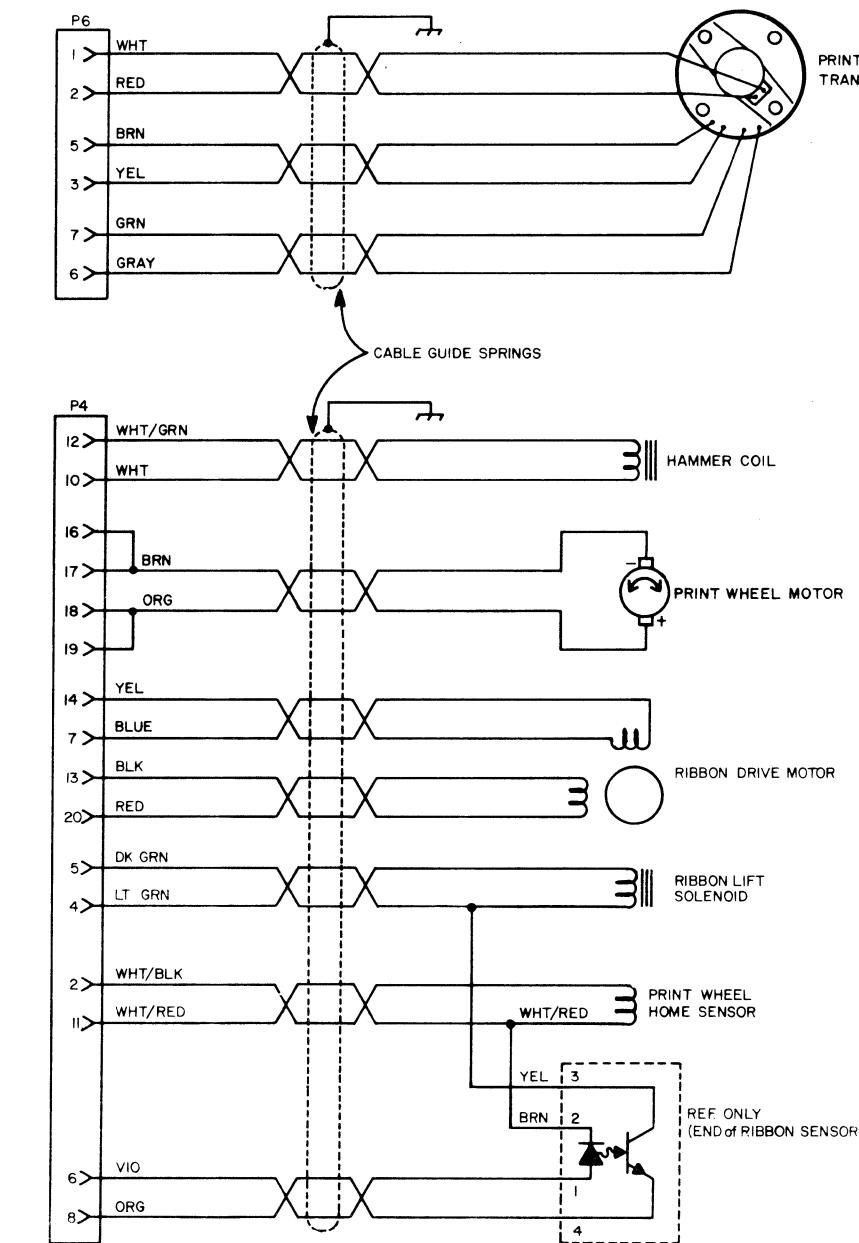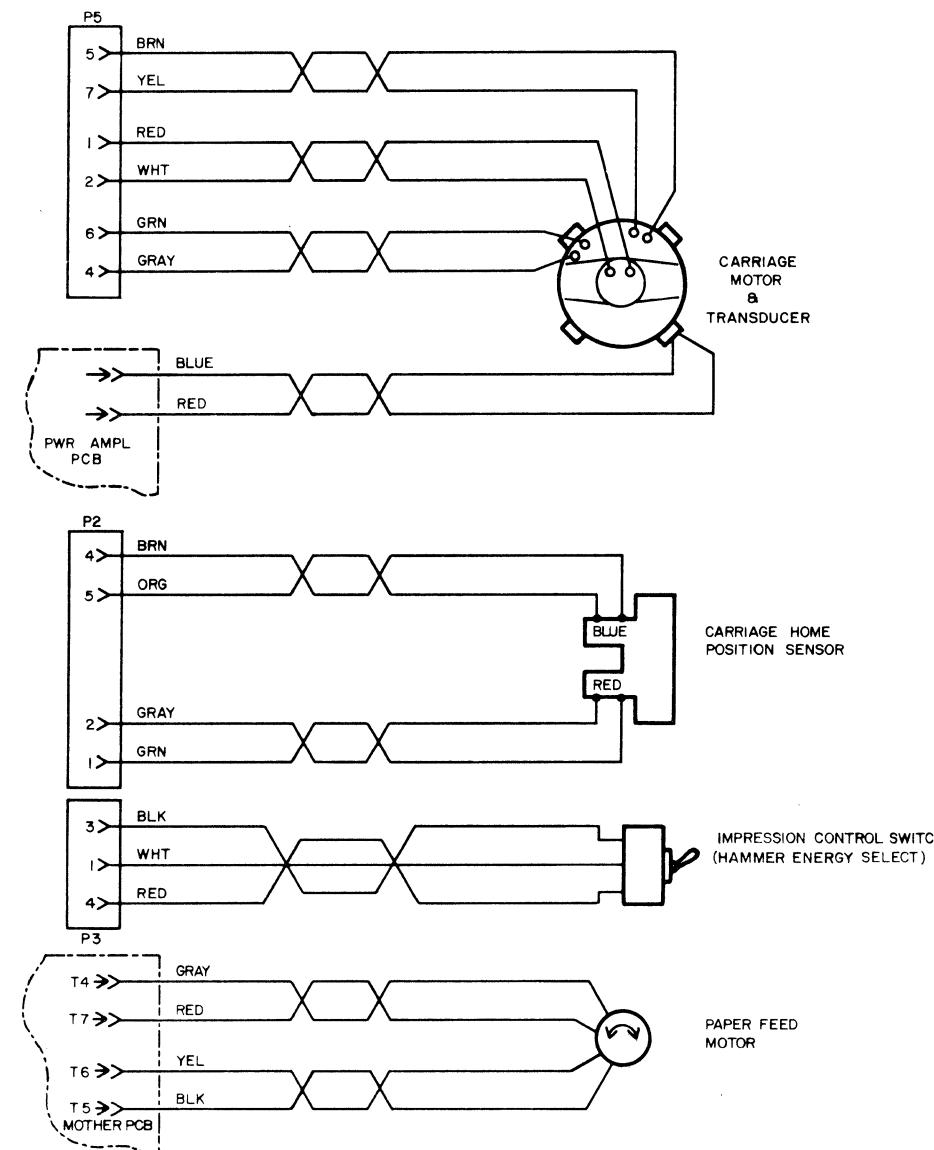
   B   9797   Revise documentation and assembly to remove two wires from cable spring to improve flexibility.

   C   9901   Revise documentation and assembly to prevent wire breakage in cable spring.

D   A1102   Add wiring for l.h. paper feed (split platen) motor. (Not applicable to HyTerm.)

E   A1244   Correct schematic error: swap wires on T10 & T12. (Not applicable to HyTerm.)

F   A1582   Gray and green wires on P2-1&2 interchanged: gray to pin 2, green to pin 1.


PRINTER CABLES

24471

REV. F

4-98

XEROX

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- [ ] Very Poor

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