Technical Manual

4046 MOVING HEAD DISK CONTROLLER AND 4047 & 4049 DISK CARTRIDGE ADAPTERS VOLUME 1

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FOREWORD

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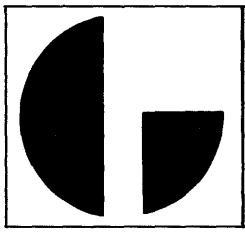

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SECTION I

GENERAL DESCRIPTION

1-1 INTRODUCTION

Data General Moving Head Disk Controller No. 4046 is designed to operate a wide variety of Moving Head Disk Drives, and is a basic component for each Moving Head Disk system. The Controller is functionally positioned between any Nova or Supernova Processor and the appropriate Moving Head Disk Adapter unit. Data General provides two types of Adapters for Disk Cartridge systems, each engineered specifically to interface with one of the two Disk Cartridge Drive units offered by Data General. From a general design point of view, Adapters 4047 and 4049 are similar in that they both operate the same type of Disk Drive equipment. (The basic difference is that the 4047 Adapter has a smaller power supply facility than the 4049 Adapter.) Adapters 4047 and 4049 are designed to interface with both the Data General Model 31 Disk Drive and the Data General Model 33 Disk Drive, and whereas the Adapter Supplies ± 15 Volt dc power to the Disk Drive; the 4047 Adapter is designed to handle two Model 31 Drives or one Model 33 Drive. The 4049 Adapter on the other hand, is designed to handle four Model 31 Drives or two Model 33 Drives. From herein all technical references to Adapter 4047 will be applicable to Adapter 4049 also, unless the 4049 Adapter is called out specifically.

The appropriate technical and maintenance manuals for either Model Disk Drive ordered from Data General are packed and shipped with the selected equipment. Thus, the information provided in this manual is intended to supplement these publications and will describe only the required Controller and Adapter equipment. Additional information concerning the operation of the Data General standard Processor Data Channels may be referenced in the "How to Use the Nova Computers" reference manual, published by Data General under separate cover.

This manual is divided into five sections: General Description, Installation, Operation, Theory of Operation, and Maintenance. It is supported by a set of engineering drawings listed below, and an Illustrated Parts List document number 005-000804-00.

It is assumed that the reader has a thorough understanding of TTL logic and the fundamentals of computers.

Disk Pack Control I/O	001-000122(Sheet 1)
Disk Pack Control Timing	001-000122(Sheet 2)
Disk Pack Control Registers	001-000122(Sheet 3)
4047 Plug Interface	001-000142
4047 Logic Interface	001-000143
4047 Disk Power Supply	001-000186
External Cable Adapter (4047 or 4049) to Computer	005-000468

1-1.1 Disk Cartridge System Components

The basic Disk Cartridge system components are shown on Figure 1-1, and consists of the Disk Controller 4046 PCB assembly, one Disk Cartridge Adapter, and a Disk Cartridge Drive. This illustration, like the previous figure, shows only one drive in the interest of simplifying the illustration, but more than one drive can be installed. As mentioned previously two types of Disk Cartridge drives are available, either a model 31 or a model 33, and if Adapter 4047 is installed the configuration will support one model 33 drive or two model 31 drives. Mixing is not possible on the 4047 Adapter without exceeding the capabilities of the Adapter power supply. If the Adapter 4049 is installed the Adapter will provide sufficient power for two model 33 drives or four model 31 drives. Mixing is allowed on this Adapter as long as the total number of drives does not exceed the equivalence of four model 31 drives. In other words, one model 33 drive is equal (loadwise) to two model 31 drives. Therefore a configuration of one model 33 drive and two model 31 drives can be installed. An installation of three model 31 drives and one model 33 drive, or two model 33 drives and one model 31 drive would exceed the capabilities of the Adapter (4049) power supply. The difference between the two drives is storage capacity. (1.247 million 16-Bit words for the model 31 drive, and 2.494 million 16-Bit words for the model 33 drive.) The connector facilities for Adapter 4047 and Adapter 4049 are similar, with the sole exception that the 4047 Adapter has a maximum of two DC cables (left rear of the chassis) whereas the 4049 Adapter has a maximum of four DC cables (also left rear of the chassis). Each Adapter unit contains its own power supply which operates from standard 115 Volt, 50 or 60 Hertz lines. A line cord is provided in the lower left section of the connector panel mounted in the rear of the Adapter chassis for connecting the Adapter to standard 115 Volt single phase power. Either Adapter provides (in addition to DC cables) a signal bus line, which for multiple drive configurations is daisy-chained between drives. This signal bus must be terminated at the last drive in the chain.

Figure 1-2 is a block diagram of the various possible configurations comprising Disk Cartridge systems. This figure is included here for reference purposes, and diagrammatically summarizes the configuration descriptions of this paragraph. The 4046 Controller and 4047 Adapter combination are shown in solid lines as being one typical system. The remain blocks are shown in dotted lines as representing other system configurations that can be installed with the Nova or Supernova Processor and 4046 Controller PCB assembly.

Figure 1-3 shows a typical dual Processor Disk Cartridge system. In this particular configuration the Adapter (either 4047 or 4049) is shared between two Processors. Each

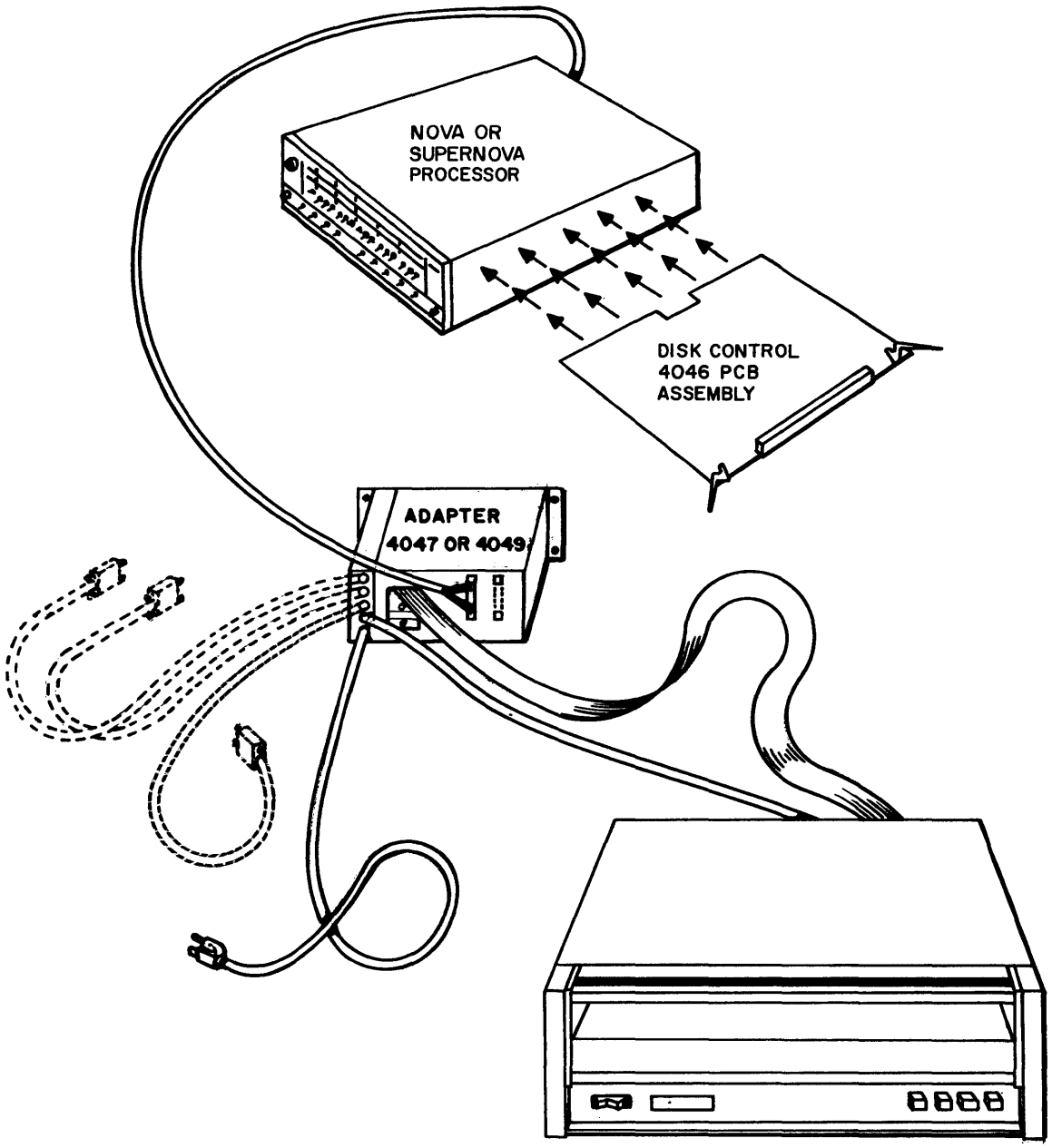


Figure 1-1. Basic Disk Cartridge System
for Adapter 4047 or Adapter 4049

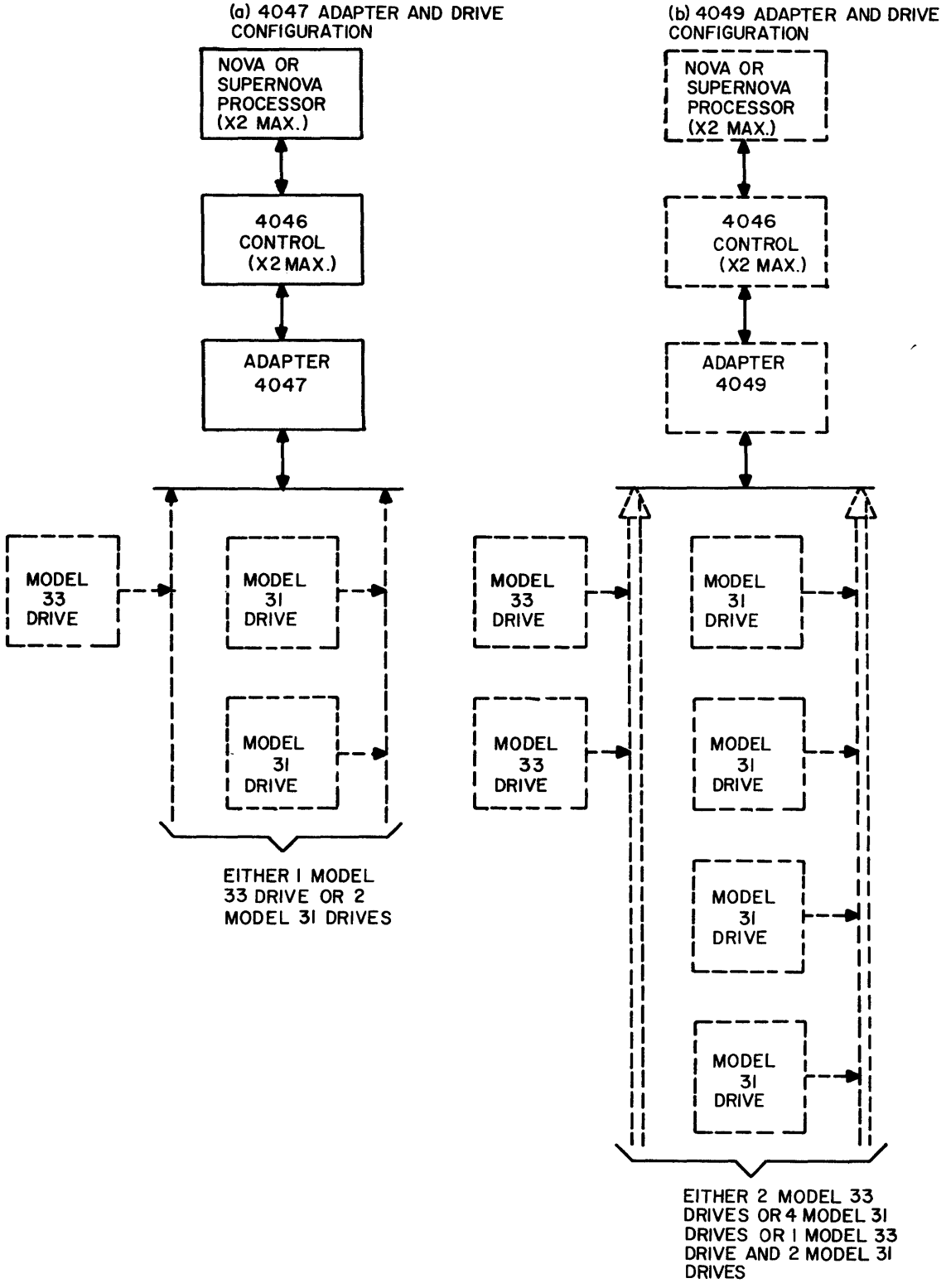


Figure 1-2. Component Configurations for Data General Disk Cartridge Systems

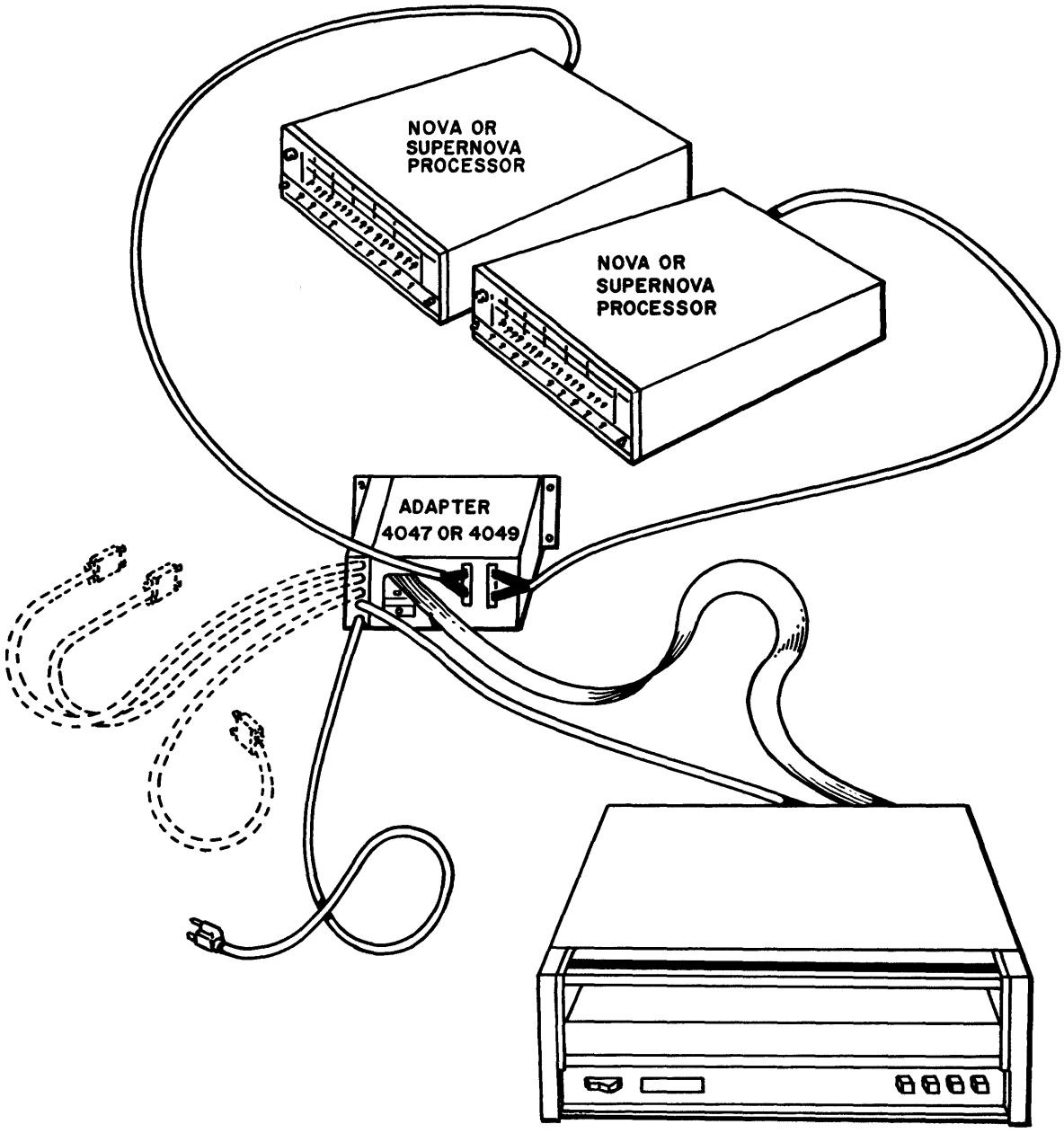


Figure 1-3. Typical Dual Processor Disk Cartridge System

Processor contains a 4046 Controller PCB assembly, which is selected alternately for control by the Adapter logic. (However, each Controller can communicate with one Adapter only.) The number of Disk Cartridge Drives included in the dual Processor system are exactly as described previously (and as shown on Figure 1-2).

Figure 1-4 is a block diagram of a dual Processor or Secondary 4046 Controller configuration that may be used to form a Disk Cartridge system. It suffices to say that the ground rules governing the number and type of Disk Cartridge Drives connected to the appropriate Cartridge Adapter are exactly the same as described previously. As mentioned above either type Cartridge Adapter (4047 or 4049) contains control logic which selectively alternates transfer operations between Processors (through the facilities of each 4046 Controller). It is also possible to have two 4046 Controllers in one Processor (each with a unique Device Select Code). In this configuration, like the dual Processor configuration, each control can communicate with One Adapter only, with all of the previously described configuration rules still applicable. A configuration with one computer housing two Controllers, with each Controller connected to a separate Adapter will support up to 8 model 31 Disk Drive units.

1-2 GENERAL FUNCTIONAL DESCRIPTION

Data General's Disk Cartridge systems are composed of devices which provide direct-access storage of data on a removable Disk Cartridge. Functional descriptions concerning the operation of the Disk Cartridge Drive supplied by Data General can be referenced from the installation and operation manual shipped with each drive. The functional descriptions of the remaining system components are presented in this paragraph starting with the 4046 Controller, which is followed by a brief description of the function of the Adapter unit. As mentioned previously all references to the 4047 Adapter are also applicable to the 4049 Adapter.

1-2.1 Disk Controller Model 4046

The general functional relationships between the 4046 Controller and the other components of a Disk Cartridge system are shown on Figure 1-5. The 4046 Controller assembly as shown, consists of three major logic sections; the I/O section, the Registers section, and the Timing section. The I/O section received I/O instructions from the Nova or Supernova Processor in the form of DATO (data out) and DATI (data in) instructions. The data out instructions load various control registers within the assembly with command and control data, whereas the data in instructions read the contents of the various control registers in the assembly back into the Processor. The I/O section also receives the Device select code from the Processor via the DS lines. The 4046 Controller assembly recognizes Device Code 33. If two 4046 Controllers are installed in the same Processor, the second Controller is conditioned to recognize Device Code 73. The I/O section also receives and transmits the various Data Channel control signals used to control the exchange of sector data. The remaining I/O bus interrupt, request, and priority signals exchange between the Processor and the Controller are also handled by the I/O section. The operation and function of the I/O bus and Data Channel signals are described in Data General publication "How to use the Nova Computers," (available under separate cover) and consequently will not be repeated in this discussion. Specific instruction data pertinent to Disk Cartridge systems are described at the end of this main paragraph.

The I/O bus data lines $\overline{\text{DATA0}}$ through $\overline{\text{DATA15}}$ are terminated in the Registers section for both receiving and transmitting data transfer Operations. Data being received by the 4046 Controller Assembly is inverted by a group of buffer inverters and sent to the I/O section as DATA0 through DATA 15. These signals load the various operation control registers in the I/O section (e.g., Unit, Sector, Head, Sector Count, and Cylinder registers) with control data governing the upcoming operation. The I/O section contains the core Address (CA) register or address counter, which can be examined under program control. The outputs from the CA register, CA0 through CA15 are routed through the Registers section, which provides the logical manipulation for placing the CA contents onto the I/O bus lines. The I/O section also generates an accompanying $\overline{\text{CA EN}}$ (CA Enable) signal which enables this logic to selectively output the data present on the CA output lines (CA0 through CA15) to the I/O bus lines. The I/O section also produces a basic EN signal for output transmissions of either CA data or stored data read from the Disk. Operational and Error status signals from the Timing section are also routed through the Registers section for transmission to the Processor via the I/O bus lines. Operational status data, e.g., contents of Unit, Head, Sector, and Sector Count registers is read back to the Processor under program control by the DATIC instruction. Error status data is read back to the Processor under program control by the DATIA instruction. The selective signals either $\overline{\text{DP DATIC}}$ or $\overline{\text{DP DATIA}}$ are derived from the standard DATIA and DATIC bus signals in the I/O section and perform the selected output enabling function in the Registers section.

In addition to multiplexing address, operational status, and error status signal into the I/O bus data lines, the Registers section assembles serial data read from the Disk for transfer back to the Processor, and disassembles parallel input data from the Processor to be written serially onto the Disk. The 4046 Controller transfers two (16 bit) words at a time, hence the assembly or disassembly is performed on a double word (32 bit) basis for any one data transfer operation. Serial data to be written onto the Disk is transmitted from the Registers section to the 4047 logic interface via the $\overline{\text{COMP DATA}}$ (Computer Data) line. Serial data to be assembled into words and sent back to the Processor is transmitted from the 4047 logic interface to the Registers section via the READ DATA line. The $\overline{\text{Write}}$ and $\overline{\text{Load}}$ signals from the I/O section to the Registers section together enable the 32 bit shift register (functioning as a series-to-parallel, parallel-to-series converter for the Disk data) to be parallel loaded with the next two words to be written on the Disk. The CLK SHIFT signal is also produced in the I/O section and being derived from the basic Data Strobe signal (from the 4047 logic interface) functions as a shift clock for the shift register during read and write operations.

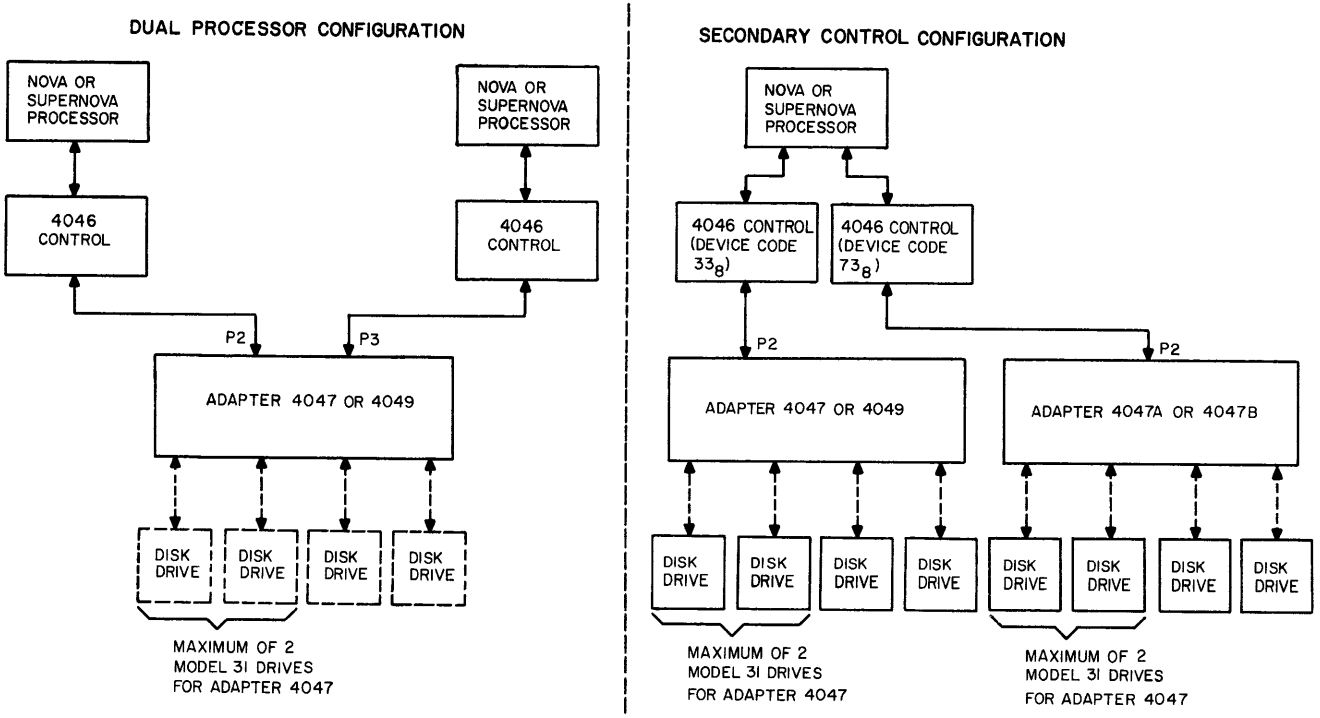


Figure 1-4. Components of a Dual Processor or a Secondary Control Configuration

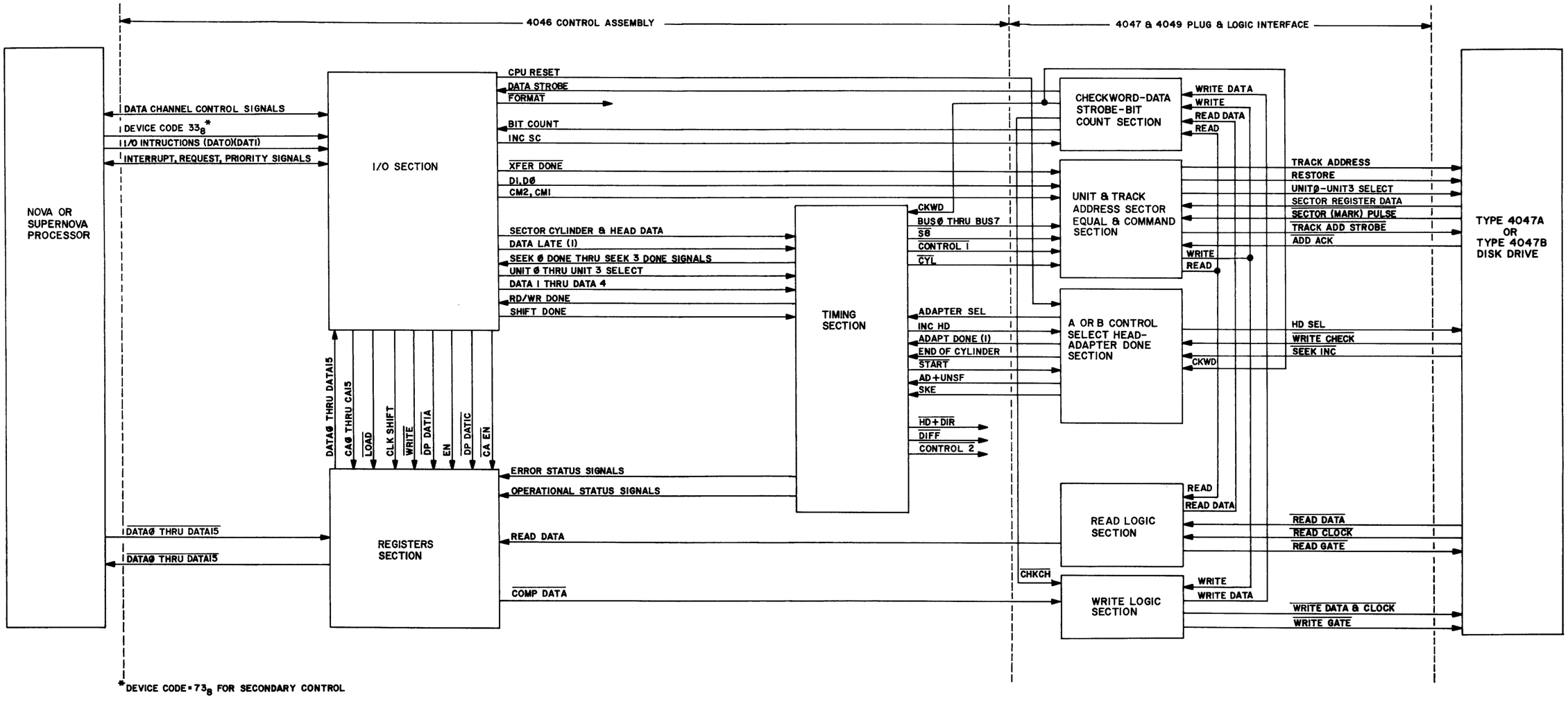


Figure 1-5. General Functional System Block Diagram
For the 4046 Disk Controller and Adapter 4047 or Adapter 4049

The I/O section transmits the INC SC, XFER DONE, D1, D0, CM1 and CM2 signals to the 4047 logic interface. The INC SC signal (Increment Sector Counter) steps the Sector Counter within the I/O section. It also actuates the Checkword logic in the 4047 logic interface for either writing the assembled checkword during a write operation or comparing the assembled checkword with that written at the end of the sector during a read operation. $\overline{\text{XFER DONE}}$ is a signal informing the 4047 Adapter (both the plug and logic interface thereof) that the present transfer operation is finished. The D0 and D1 signals to the 4047 logic encode the address of the Disk Drive to be used during the upcoming operation. The CM1 and CM2 signals to the 4047 logic interface encode the commanded operation that the system is to perform (i.e., seek, read, write, or recalibrate). The BIT COUNT signal from the 4047 logic interface is used to increment the Bit Counter within the I/O section. This counter keeps track of the number of data bits transferred and counts up to 32, the capacity of the shift register.

The I/O section also exchanges a group of significant signals with the Timing section. The I/O section sends functional signals SECTOR, CYLINDER and HEAD DATA, UNIT 0 through UNIT 3 SELECT, DATA1 through DATA4, SHIFT DONE and LATE (1). The SECTOR, CYLINDER and HEAD DATA is multiplexed in the Timing section onto interassembly lines BUS0 through BUS7, to the 4047 logic interface. Sector register bit 8, S8, is transmitted directly to the 4047 logic interface over a single line, and hence is not multiplexed. The UNIT0 through UNIT3 Select signals are used in conjunction with the Seek control logic of the Timing section and indicate which one of the four possible Disk Drive units have been selected. This same logic section sends SEEK DONE0 thru SEEK DONE3 signals back to the I/O section to indicate that the selected Disk Drive (UNIT0 thru UNIT3) has finished the commanded (track) seek operation. The DATA1 thru DATA4 signals are those bits which reset the Seek control logic of the selected unit. (DATA0 clears the Read/Write Done interrupt indicator, however this flag is in the I/O section.) The SHIFT DONE signal performs an important function relative to both the read and write modes. The SHIFT DONE signal sent to the Timing section is allowed to trigger a one shot, in the read mode, which in turn loads the disk data contained in the Shift Register (in the Register section) into the Data Storage Register (also in the Registers section) in preparation for multiplexing onto the I/O bus lines to the Processor.

SHIFT DONE also performs a clocking for the DP Flag and Data Late flip-flops in the I/O section. (The Data Late flip-flop becoming set, sets the Stop flip-flop, which in turn (providing the "Read Done" one shot is not cycling) produces a $\overline{\text{DONE}}$ signal. $\overline{\text{DONE}}$ in turn drives an OR gate to produce $\overline{\text{XFER DONE}}$ which terminates the transfer.) A momentary digression at this point to explain the basic function of Data Late will serve to clarify later detailed discussion of this logic. The DP (Data) Flag flip-flop is set (during write operations) initially on a start of a write operation. This Flag is cleared when the Data Channel Acknowledgement from the second Data Channel Request is received at the Control assembly. Two (16 bit word) requests are required as 32 bits are written as one word by the Control assembly. If the Flag flip-flop is set and a SHIFT DONE signal occurs the Data Late flip-flop will be set. This condition indicates that for some reason the Processor did not respond to the Data Channel Request in time to load (or finish loading) the Shift Register before it finished a 32 bit shifting (and writing) sequence. Hence, a data error condition will exist and the transfer will be terminated. Initially the (Data) Flag flip-flop is set by the WRITE and START ADAPTER signals. It is cleared by CLR FLAG (derived from DCHP IN, DCHR, DCH SEL, and DCHA) and the resetting of the REQ1 flip-flop (indicating second request has been acknowledged). The (Data) Flag flip-flop is clocked to the set state during the remainder of the writing operation (as long as the Busy flip-flop remains set) by each SHIFT DONE signal. Setting the Flag flip-flop causes the next $\overline{\text{DCHR}}$ to be issued (if requests are enabled). The Flag flip-flop is cleared during the remainder of the write operation exactly as described above. Hence, during the writing operation a "window" exists between SHIFT DONE pulses during which the Flag flip-flop is set (requesting the next two 16 bit data words from the Processor), to which the Processor must respond by servicing the request (long before SHIFT DONE can occur in normal operation). The worst case (Processor response delay) condition exceeding the width of the time window (between subsequent SHIFT DONE pulses) defines the Data Late error condition.

The Timing section sends a RD/WR DONE signal back to the I/O section. This signal is derived from the ADAPT DONE (1) signal from the 4047 Adapter to indicate the Adapter has completed (or terminated) the command operation. RD/WR DONE sets the Done flip-flop in the I/O section.

The Timing section receives the CKWD, ADAPT SEL, ADAPT DONE (1), END OF CYLINDER, AD+UNSF, and SKE signals from the 4047 Adapter (Plug and Logic Interface). Four of these signals, CKWD, END OF CYLINDER (EOC), AD+UNSF, and SKE are errors indicators. The CKWD signal is generated in the Checkword section of 4047 logic to indicate a Checkword error has been detected. The EOC signal is generated in the Head Select section of the 4047 logic whenever an attempt to increment to a non-existent head is detected, i.e., increment beyond the number of heads available in the Disk Drive. AD+UNSF is derived from a $\overline{\text{WRITE CHECK}}$ signal produced in the Disk Drive unit electronics and indicates that a condition exists within the drive unit that will interfere with writing valid data on the Disk, or possible damage to other records already written on the Disk will occur if writing is attempted. SKE is the Seek Error signal, which is derived from the $\overline{\text{SEEK INC}}$ signal from the Disk Drive unit. $\overline{\text{SEEK INC}}$ denotes SEEK INComplete, and indicates the failure of the present seek operation to successfully position the heads over the selected cylinder. Signal ADAPT SEL is produced in the A or B Control Select section of the 4047 logic and indicates that an operational connection has been established between the 4046 Control assembly and the 4047 Adapter. The Adapter is designed to select one of two possible 4046 Control assemblies for operation (if the Control has been started and is waiting for service). The ADAPT DONE(1) signal, as described previously, is produced in the Adapter Done section of the 4047 logic, and causes the DP Done flip-flop (of the I/O section of the 4046 Control) to become set (via the RD/WR DONE signal function).

The Timing section contains a Seek Timing Generator, which provides a precise sequence of signals used to control the various calculations and mechanical selections involved in moving the Disk heads to the selected cylinder position. There signals are CONTROL1, CYL, HD+DIR, DIFF, and CONTROL2, of which only CONTROL1 and CYL are used by the 4047 Adapter. CONTROL1 is used as one of the enabling signals for setting up the RD/WR (read/write) control logic in the Unit and Track Address section of the 4047 logic. CONTROL1 is also gated together with RECAL (Recalibrate) to implement the Track Address logic to command repositioning of the Disk heads back at the 000 starting location. Signal CYL is also used, independently, to trigger the Track Address logic. When CYL occurs the Track Address register is loaded with the Cylinder address data. This data is subsequently sent to the (selected) 4047A or 4047B Disk Drive unit electronics where it is positionally interpreted as track address data. It is pointed out here as a matter of clarification, that both CONTROL1 and CYL will be produced in the Timing section if a SEEK command is present. For all other commands (RECAL, READ, WRITE) only CONTROL1 will be produced by the Timing section. Hence, in a sense CYL and RECAL (and all other commands except SEEK) are operationally mutually exclusive. (RECAL is decoded in the 4047 logic to generate a RESTORE signal. This signal clears the track address register in the Disk Drive unit to 000, and commands the head positioner to locate the heads over track 000. In the event of a Seek Error a RESTORE command is required by the Disk Drive electronics before it will remove the SEEK INCOMPLETE level from the interface line.)

The Timing section also sends the INC HD and START signals to the Head Select and the A or B Control Select sections of the 4047 logic. The INC HD signal will increment read or write operations to the next numerically selectable head in the Disk Drive unit. Since the 4047A and 4047B Disk Drive units each contain two heads, incrementing (without an End of Cylinder error) is not possible beyond head 1, selected by placing a 1 on the BUS7 line (which results from coding a 1 in bit 7 of the Accumulator selected for the DATOC instruction). The INC HD signal is generated when the Sector Register reaches a count of 12 (S8 and S4 = 1), and an Increment Sector Counter (INC SC) signal is present. This function facilitates the 12 sector format established for the 4047A and 4047B Disk Drive units. Therefore after Sector No. 12, the 4046 Control assembly logic automatically advances or increments the head to operate on the 12 sectors on the opposite side of the Disk (in the same track location). INC HD also implements logic within the 4046 Control to clear out the Sector register. It should be emphasized that it is Sector No. 12 not necessarily the 12th sector that causes the INC HD signal to be produced. Normally the Sector register is loaded with the number of the sector in which the specified operation will be performed, and the Sector register will be incremented from this point on up to Sector No. 12. The START signal, on the other hand, is simply representative that the 4046 Control has been started by either an I/O "P" (Pulse) control function for either a SEEK or RECAL operation, or an I/O "S" (Start) control function for the other (Read or Write) operations. After transmitting the START signal the 4046 Control must wait for the 4047 Adapter to respond with an ADAPTER SEL before operation can proceed.

1-2.2 Adapter Model 4047

The Adapter Model 4047 is functionally located between the 4046 Control assembly and the 4047A or 4047B Disk Drive unit (or units). Functionally, the Adapter contains the following five logic sections:

1) Check-Data Strobe-Bit Count section.
2) Unit and Track Address-Sector Equal and command section.
3) A or B Control Select-Head-Adapter Done section.
4) Read Logic section.
5) Write Logic section.

The Checkword-Data Strobe-Bit Count section produces the CKWD, DATA STROBE and BIT COUNT signals. The Checkword logic of this section forms the 16 bit checkword during read and write operations. The assembled checkword is the last word written into each sector. The assembled checkword is transmitted serially from the checkword shift register to the Write logic section via the CHKCH line, where it is gated out to the Disk Drive unit via the WRITE DATA and CLOCK line. The checkword assembled during a read operation is compared with the checkword written on the Disk for equality at the end of the read operation. Comparison is performed on a bit-by-bit basis. As each bit (of the recorded checkword) is read in from the Disk, it is compared with the least significant bit of the Checkword register. Each bit of the recorded checkword read in (after the first comparison) also causes the Checkword register to be (right) shifted for the comparison. The recorded checkword bit is presented to the checkword logic via the READ DATA line. READ DATA also provides the information required to form the checkword during the read operation. (It is noted that READ DATA is also the information line which carries the data read from Disk to the Register section.) Likewise, the WRITE DATA line provides the Checkword logic with the information required to form the checkword during a write operation. The READ and WRITE are Commands decoded from the signals on the CM1 and CM2 lines.

A WRITE GATE or READ GATE signal is produced by the appropriate (write or read) logic section for the Disk Drive unit. The WRITE GATE signal turns on write current and erase current simultaneously in the selected Disk head, therefore WRITE GATE is held on (or true) for the entire write operation. The READ GATE signal, on the other hand, enables the READ CLOCK and READ DATA outputs from the Disk Drive unit electronics, and also is held on (or true) for the entire read operation.

The READ CLOCK line from the Disk Drive electronics provides pulses that represent clock signals which have been separated from data signals (within the Disk Drive unit) during reading. Conversely the READ DATA line from the Disk Drive electronics provides pulses that represent data signals which have been separated from clock signals (within the Disk Drive unit) during reading. The READ CLOCK signal is used to synchronize and control the Read logic and Checkword logic

during the read operation. During the write mode of operation the Write logic and Checkword logic are synchronized by the outputs from a two stage ring counter driven by the 5.75 MHz Adapter oscillator, which together function as the write clock.

Sector register data from the Disk Drive unit is compared, in the Sector Equal logic, with the Sector Address data transmitted from the 4046 Control via BUS lines 0 thru 2, and the $\overline{S8}$ lines. This comparison is basically a four bit binary exclusive OR comparison to determine equality. The output from the comparison logic is tested upon the arrival of each $\overline{\text{SECTOR (MARK) PULSE}}$ from the Disk Drive unit. SECTOR MARKS are generated within the Disk Drive unit as each sector slot (on the Disk shaft assembly) as it rotates by the sector transducer. The leading edge of this pulse provides a mechanical reference as to the start of the associated sector. (The SECTOR MARK also increments the Sector Address register within the Disk Drive unit.) An equality signal from the comparison logic together with a $\overline{\text{SECTOR PULSE}}$ (a slight nomenclature change to this signal line occurs as it passes through the interface between the Disk Drive unit and the 4047 Adapter, i.e., SECTOR MARK becomes $\overline{\text{SECTOR PULSE}}$) will allow the commanded read or write operation to begin.

The data loaded into the Track Address register of the Track Address logic section is transmitted to the Disk Drive unit via eight interface lines (binary lines 1 thru 128). Initially and after the data has been loaded into the Track Address and given a chance to settle, a $\overline{\text{TRACK ADD STROBE}}$ signal is sent to the Disk Drive unit. The Disk Drive unit interprets this signal as a command to sample either the eight TRACK ADDRESS lines or the RESTORE line. The $\overline{\text{TRACK ADD STROBE}}$ signal and the TRACK ADDRESS data must be held in their specified states until the $\overline{\text{ADD ACK}}$ (ADDress ACKnowledge) signal is issued by the Disk Drive unit. This requires a holding interval between 22.5 and 37.5 microseconds. The $\overline{\text{TRACK ADD STROBE}}$ is released as soon as $\overline{\text{ADD ACK}}$ is received.

As described previously, the 4047A and 4047B Disk Drive units contain two heads. The HD SEL (Head Select) line allows selection of either head relative to the logic level presented on this interface line. A logic 0 (0 volt nominal) signal selects the upper head whereas a logic 1 (+5 volts nominal) signal selects the lower head. The selected level placed on the HD SEL line is held for the entire duration of the read or write operation.

1-2.3 Instructions

The I/O instructions for the Disk Control Model 4046 are provided in other Data General publications (e.g., Nova Disk Pack Drive Option Bulletin), and are included here for general reference purposes. The Device Select code for the 4046 Control is octal 33.

1-2.3.1 Seek Instructions. The SEEK instruction is initiated with an I/O "P" pulse. It has no effect on BUSY or DONE but does require 50 microseconds to initiate (for the 4047A or 4047B Disk Drive units). The Adapter will hold the SEEK for 6 seconds or until READ or WRITE DONE occurs.

If no READ or WRITE instruction follows a SEEK, the Adapter will accept another SEEK. This prevents consecutive SEEK instructions with no READ or WRITE from tying up an Adapter. SEEK DONE is set at the completion of a SEEK, and will cause an interrupt on the control initiating the SEEK.

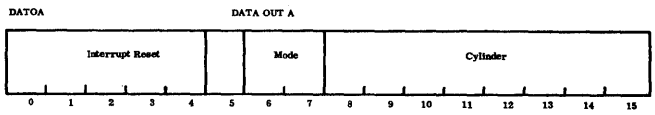
1-2.3.2 Read/Write Instructions. The disk control is placed into operation to READ or WRITE with the I/O "S" pulse. If the Adapter is busy or the Disk Drive is not ready, BUSY is set, and the READ/WRITE instruction is held.

The setting of DATA LATE indicates the transfer rate of the disk was greater than that of the I/O channel during peak periods of I/O traffic. If this condition exists, the program will automatically reposition the READ/WRITE heads to cylinder 000, SEEK and try again.

If there is no error condition, the control waits until the selected track sector is encountered and then processes the information in the block making data channel requests whenever it has a word ready for memory in READ or when one of the buffers is ready for WRITE.

In READ, if the checkword read from the disk does not agree with that computed by the control, data transfer is halted and the head and sector in error may be read via DIC. During the transfer of several sectors, if the end of the cylinder was detected and the sector count was not zero, END CYLINDER will be set and no automatic SEEK to the next cylinder takes place.

1-2.3.3 Function and Format

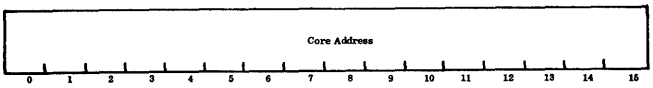


Load Interrupt-Reset Register, Mode and Cylinder address into the disk control. Perform the function specified by F.

The mode bits (6 and 7) generate the disk pack command as follows:

BIT	6	7	FUNCTION
	0	0	READ
	0	1	WRITE
	1	0	SEEK
	1	1	RECALIBRATE

DATOB DATA OUT B

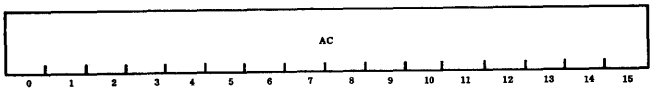


Load the contents of AC 1-15 into the Core Address Register with the STARTING Core Address.

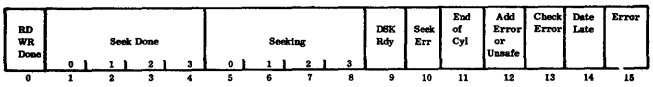
DATOC DATA OUT C

Load the contents of AC 1-15 into the disk UNIT, HEAD, SECTOR and SECTOR COUNT address register. Select the UNIT, HEAD and SECTOR from which data is to be transferred initially, and select the two's complement number of consecutive sectors to be transferred.

DATIA DATA IN A



Read the status of the disk system into the AC bits 0-15 as shown.



AC bits 0-9 indicate status of the drive. Bits 10-15 indicate error conditions.

AC 10 Selected disk drive did not complete a SEEK.

AC 11 The HEAD address register has incremented beyond the last HEAD of the cylinder. This condition will cause a consecutive sector READ or WRITE to stop transfer.

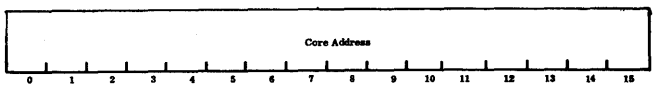
AC 12 The disk selected by the program is unsafe for operation or the address selected on the disk does not agree. Address errors are a mismatch between the header data and the cylinder head being sought.

AC 13 In READ, the cyclic checkword read from the disk surface did not agree with the checkword computed by the control.

AC 14 The data channel failed to respond in time to a request for access. (This can occur because of a long instruction or channel pre-emption by a faster device.)

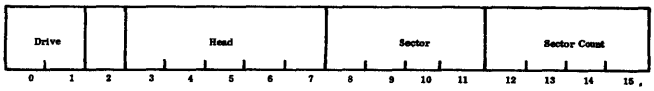
AC 15 The "OR" condition of bits 10-14 exists.

DATIB DATA IN B



Read the contents of the Address Counter into AC bits 0-15. NOTE: Core Address Register (C) = Starting Core Address + 256N + 2, where N = Number of Sectors Written.

DATIC DATA IN C



Read the present contents of the UNIT, HEAD address, SECTOR address, and SECTOR COUNT registers into AC bits 1-15.

1-3 PHYSICAL DESCRIPTION

The Disk Control Assembly Model 4046 is a 15 X 15 inch printed circuit board (PCB) Assembly designed for plug mounting in the multiple printed circuit board connector located within the Nova or Supernova Enclosure Chassis. The 4046 Control Assembly PCB is inserted horizontally into the Enclosure Chassis and on a plane with the particular slot previously wired for this assembly. An outline drawing typical of the standard printed circuit boards provided by Data General is provided in Appendix A of the "How to use the Nova Computers" reference manual.

The physical and electrical specifications for the 4047 and 4049 Adapters are listed in Table 1-1. An outline drawing of the Adapter enclosure is shown on Figure 1-6. The performance specifications for Data General Disk Drive types, 4047A & 4047B are presented in the Drive publications under separate cover.

1-4 PERTINENT DOCUMENTS

The following documents serve as source material and complement the information in this manual. Publications available from sources other than Data General are listed with the address of the alternate source. Publications listed without an alternate source address are available only from Data General.

How to Use the Nova Computers

Series 30 Disk Drives
Product Description No. D3031-670

Diablo Systems Incorporated
24500 Industrial Blvd.
Hayward, California 94545

Maintenance Manual
For Model 31 Disk Drive No. D3140-171
Diablo Systems Incorporated
24500 Industrial Blvd.
Hayward, California 94545

Moving Head Disk Control
Diagnostic DGC Manual 097-000039

Moving Head Disk
Reliability Program
DGC Manual 097-000038

1-5 ABBREVIATIONS

Listed below are the most commonly used abbreviations of registers, operations, components, instructions, and signal names. It will be noted that this listing has been compiled in alphabetical-numeric order to facilitate referencing.

Table 1-1. Specification Data-Adapters 4047 and 4049

	Physical Data Adapter 4047	Adapter 4049
Enclosure Height	7 inches (nominal)	7 inches (nominal)
Enclosure Width (Mounting)	19 inches (nominal)	19 inches (nominal)
Enclosure Width (Enclosure)	16 15/16 inches	16 15/16 inches
Enclosure Depth	19 5/8 inches	19 5/8 inches
Weight	30 Lbs.	55 Lbs.
	Electrical Data	
Power Requirements	115V or 230V *Single phase, ± 20% 47 to 63 Hz. Maximum Current 2 amperes, 230 watts.	115V or 230V *Single phase, ± 20% 47 to 63 Hz. Maximum Current 4 amperes, 460 watts.
Power Supply Outputs**		
+15 volt	8 amperes (Max.)	17 amperes (Max.)
-15 volt	5 amperes (Max.)	10 amperes (Max.)
+ 5 volt	3 amperes (Max.)	3 amperes (Max.)
Logic Signals	Low = 0 volts to +.4 volt nominal	Same as 4047
	High = +2.5 volts to +3.5 volts nominal	Same as 4047

* 230 volt on special order

** Maximums specified are based on maximum configurations as defined in Paragraph 1-1.1 of this manual.

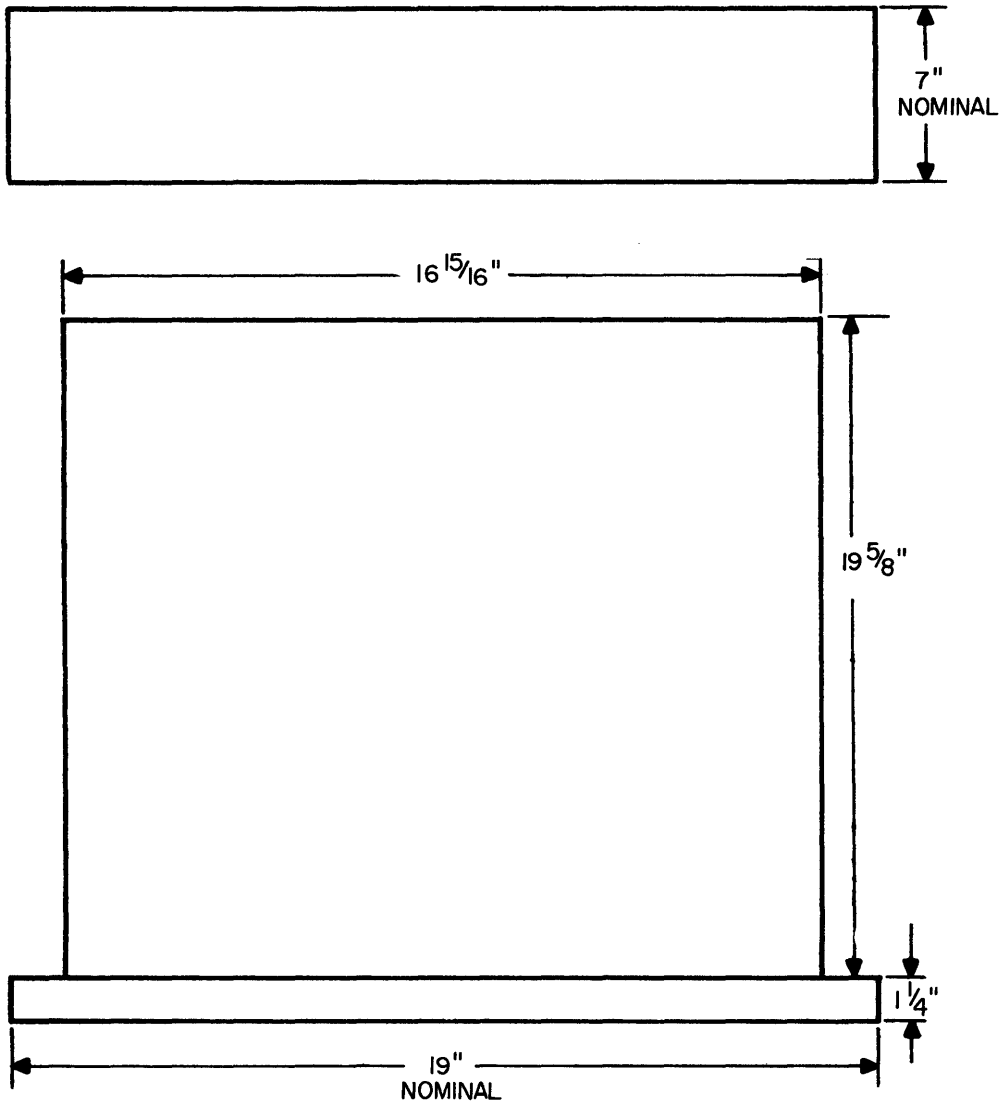


Figure 1-6. Outline of Adapters 4047 and 4049

ABBREVIATIONS

ADAPT DONE (1)....Adapter Done (flip-flop output)
ADAPTER SEL....Adapter Select
AD+UNSF....Addressing (error) or Unsafe
$\overline{\text{AD+UNSF}}$ (1)....Addressing (error) or Unsafe (flip-flop output)
ADV HD....Advance Head
$\overline{\text{ADV HD}}$....(Complement of above)
ATTEN0-ATTEN3....Attention Line 0 thru Attention Line 3
BIT COUNT....(Increment the Bit Counter)
BUS0-BUS7....Bus Line 0 thru Bus Line 7 (to Disk Units)
CA0-CA15....Current Address Register Outputs 0 thru 15
CKWD (1)....Checkword (flip-flop output)
$\overline{\text{CKWD}}$ (1)....(Complement of above, flip-flop output)
CLEAR ALL....Clear All (logic reset function)
$\overline{\text{CLEAR ALL}}$....(Complement of above)
CLEAR....Clear (logic reset function)
$\overline{\text{CLEAR}}$....(Complement of above)
CLEAR C....Clear (Bit and Word) Counter
CLEAR P....Clear Pulse (strobes DONE and ADV HD)
$\overline{\text{CLK A}}$....Clock A (load function-Data Storage register)
CLK B....Clock B (load function-Data Storage register)
$\overline{\text{CLK B}}$....(Complement of above)
$\overline{\text{CLEAR STATUS}}$....Clear (error) Status flip-flops
CLK SHIFT....Clock Shift (for 32 bit Shift register)
$\overline{\text{CLK SHIFT}}$....(Complement of above)
$\overline{\text{CLK DSA}}$....Clock Data Storage A (load function-Data Storage register)
CLK DSB....Clock Data Storage B (load function-Data Storage register)
$\overline{\text{CLK DSB}}$....(Complement of above)
$\overline{\text{CLR FLAG}}$....Clear (Data Request) Flag
CM1....(Operation select) Command Line 1
CM2....(Operation select) Command Line 2
CONTROL1....(Start Adapter function) Control 1
$\overline{\text{CONTROL1}}$....(Complement of above)
CONTROL2....(Seek Timing function) Control 2*
$\overline{\text{CONTROL2}}$....(Complement of above)
CLR....(I/O Bus signal) Clear
$\overline{\text{CLR REQ}}$....Clear (DP Data Channel) Request
CYL....Cylinder (Seek Timing function)
$\overline{\text{CYL}}$....(Complement of above)
CYL1, CYL2, CYL4, CYL8, CYL16,
CYL32, CYL64, CYL128....Cylinder Register outputs
$\overline{\text{DATA}}$....(Computer) Data (to be written on disk)
$\overline{\text{DATA LATE}}$ (1)....Data Late (flip-flop output)
DATA LATE (1)....(Complement of above, flip-flop output)
DATA STROBE....Data Strobe (controls serial-parallel, parallel-serial movement of data)
D0-D1....Disk (unit select) Lines 0 and 1
$\overline{\text{DATA0-DATA15}}$....(I/O Bus signals) Data0 thru Data15
DATA0-DATA15....(Complement of above)
DATIA....(I/O Bus Signal) Data In A
DATIB....(I/O Bus Signal) Data In B
DATIC....(I/O Bus Signal) Data In C
DATOA....(I/O Bus Signal) Data Out A
DATOB....(I/O Bus Signal) Data Out B
DATOC....(I/O Bus Signal) Data Out C
$\overline{\text{DCHA}}$....(I/O Bus signal) Data Channel Acknowledge
DCHI....(I/O Bus signal) Data Channel In
$\overline{\text{DCHM0}}$....(I/O Bus signal) Data Channel Mode

*Not used with Adapters 4047 and 4049

ABBREVIATIONS (Continued)

DCHO ..... (I/O Bus signal) Data Channel Out
DCHP IN ..... (I/O Bus signal) Data Channel Priority In
$\overline{\text{DCHP IN}}$ ..... (Complement of above)
DCHP OUT ..... (I/O Bus signal) Data Channel Priority Out
DIFF ..... (Seek Timing function, address) Difference*
$\overline{\text{DIFF}}$ ..... (Complement of above)
$\overline{\text{DONE}}$ ..... (Stop function indicating 4046 Control is) Done
$\overline{\text{DP}}$ ..... Disk Pack (mnemonic for 4046 Control)
DP BUSY (1) ..... Disk Pack Busy (flip-flop output)
DP BUSY ..... Disk Pack Busy (flip-flop)
$\overline{\text{DP DATIA}}$ ..... Disk Pack Data In A
$\overline{\text{DP DATIB}}$ ..... Disk Pack Data In B
DP DATIC ..... Disk Pack Data In C
$\overline{\text{DP DATIC}}$ ..... (Complement of above)
$\overline{\text{DP DATOA}}$ ..... Disk Pack Data Out A
$\overline{\text{DP DATOB}}$ ..... Disk Pack Data Out B
DP DCHA ..... Disk Pack Data Channel Acknowledge
DP DCHI ..... Disk Pack Data Channel In
$\overline{\text{DP DCHI}}$ ..... (Complement of above)
DP DCHO ..... Disk Pack Data Channel Out
$\overline{\text{DP DCHO}}$ ..... (Complement of above)
DP DCH REQ ..... Disk Pack Data Channel Request
DP DONE ..... Disk Pack Done (flip-flop)
$\overline{\text{DP DONE}}$ (1) ..... Disk Pack Done (flip-flop output)
DP FLAG ..... Disk Pack Flag (flip-flop)
DP FLAG (1) ..... Disk Pack Flag (flip-flop output)
DP INT ..... Disk Pack Interrupt
DP INT DISABLE ..... Disk Pack Interrupt Disable
$\overline{\text{DP INT REQ}}$ ..... Disk Pack Interrupt Request (flip-flop)
DP INT REQ (1) ..... Disk Pack Interrupt Request (flip-flop output)
$\overline{\text{DP IOP}}$ ..... Disk Pack IO Pulse
DP SELECT ..... Disk Pack Select
$\overline{\text{DP START}}$ ..... Disk Pack Start (derived from I/O Bus STRT function)
DP START ..... (Complement of above)
DS0-DS31 ..... Data Storage Register Outputs 0 thru 31
$\overline{\text{DS0-DS5}}$ ..... Device Select lines 0 thru 5
DUR ..... (Selected) Disk Unit Ready
$\overline{\text{EN}}$ ..... Enable (multiplexer to I/O Bus)
$\overline{\text{EN CA}}$ ..... Enable Current Address data (multiplexer to I/O Bus)
EOC ..... End of Cylinder (flip-flop)
EOC (1) ..... End of Cylinder (flip-flop output)
$\overline{\text{ERR}}$ ..... Error (common signal for all error conditions)
$\overline{\text{F DONE}}$ ..... Format (writing on disk) Done
$\overline{\text{FORMAT}}$ ..... Format (the disk mode of operation)
FORMAT ..... (Complement of above)
HD1, HD2, HD4, HD8, HD16 ..... Head Register outputs
$\overline{\text{HD + DIR}}$ ..... Head and Direction (Seek Timing function)*
HD + DIR ..... (Complement of above)
$\overline{\text{INC CA}}$ ..... Increment Current Address Register
INC HEAD ..... Increment Head Register
$\overline{\text{INC SC}}$ ..... Increment Sector Counter
INC SC ..... (Complement of above)
INTA ..... (I/O Bus signal) Interrupt Acknowledge
$\overline{\text{INTERRUPT}}$ ..... (Present operation done, request) Interrupt
$\overline{\text{INTP IN}}$ ..... (I/O Bus signal) Interrupt Priority In
$\overline{\text{INTP OUT}}$ ..... (I/O Bus signal) Interrupt Priority Out

*Not used with Adapters 4047 and 4049

ABBREVIATIONS (Continued)

$\overline{\text{INTR}}$	(I/O Bus signal) Interrupt Request
IOPLS	(I/O Bus signal) IO Pulse
IO RST	(I/O Bus signal) IO Reset
$\overline{\text{LOAD}}$	Load (Shift Register from Data Storage Register)
$\overline{\text{MSKO}}$	(I/O Bus signal) Mask Out
RD+WR	Read or Write (operation)
RD/WR DONE	Read or Write (operation) Done
$\overline{\text{READ}}$	Read (Command decode)
READ	(Complement of above)
READ DATA	Read Data (from the disk)
$\overline{\text{RECAL}}$	Recalibrate (command decode)
RECAL	(Complement of above)
RESET	Reset (derived from I/O Bus IORST)
$\overline{\text{RESET}}$	(Complement of above)
RESET S (1)	Reset Sector Register (One-shot output)
REQ1	(First data request or) Request 1
$\overline{\text{RQENB}}$	(I/O Bus signal) Request Enable
SEEK	Seek (Command decode)
$\overline{\text{SEEK}}$	(Complement of above)
SEEK DONE	Seek (operation) Done
SEEK DONE0 (1)	Seek (operation) Done (Disk Unit 0) (flip-flop output)
$\overline{\text{SEEK DONE0}}$ (1)	(Complement of above, flip-flop output)
$\overline{\text{SEEK DONE1}}$ (1)	Seek (operation) Done (Disk Unit 1)(flip-flop output)
$\overline{\text{SEEK DONE1}}$ (1)	(Complement of above, flip-flop output)
$\overline{\text{SEEK DONE2}}$ (1)	Seek (operation) Done (Disk Unit 2)(flip-flop output)
$\overline{\text{SEEK DONE2}}$ (1)	(Complement of above, flip-flop output)
$\overline{\text{SEEK DONE3}}$ (1)	Seek (operation) Done (Disk Unit 3) (flip-flop output)
SEEK DONE3 (1)	(Complement of above, flip-flop output)
SEEKING0	(Disk Unit 0) Seeking (indicator flip-flop)
SEEKING1	(Disk Unit 1) Seeking (indicator flip-flop)
SEEKING2	(Disk Unit 2) Seeking (indicator flip-flop)
SEEKING3	(Disk Unit 3) Seeking (indicator flip-flop)
$\overline{\text{SEEKING0}}$ (1)	Seeking 0 (flip-flop output)
$\overline{\text{SEEKING1}}$ (1)	Seeking 1 (flip-flop output)
$\overline{\text{SEEKING2}}$ (1)	Seeking 2 (flip-flop output)
$\overline{\text{SEEKING3}}$ (1)	Seeking 3 (flip-flop output)
$\overline{\text{SELB}}$	(I/O Bus signal) Selected Busy
$\overline{\text{SELD}}$	(I/O Bus signal) Selected Done
SHIFT DONE	(32 bit Shift Register) Shift Done
SHIFT0-SHIFT31	(32 bit) Shift Register Outputs
SKE	Seek Error
$\overline{\text{SKE}}$	(Complement of above)
$\overline{\text{START}}$	Start (Adapter signal function)
START	(Complement of above)
$\overline{\text{START}}$ (1)	Start (flip-flop output)
START ADAPTER (1)	Start Adapter (one-shot output)
$\overline{\text{START SEEK}}$	Start Seek (strobe-sets corresponding unit Seeking flip-flop)
STOP(0)	Stop (flip-flop output)
STRT	(I/O Bus signal) Start
S0, S1, S2, S4, S8, $\overline{\text{S8}}$	Sector Register outputs
SC1, SC2, SC4, SC8	Sector Counter outputs
TS ENABLE	Time State Enable (flip-flop)
TS ENABLE (1)	Time State Enable (flip-flop output)
$\overline{\text{UNIT0}}$	(Disk) Unit 0 (Select)
$\overline{\text{UNIT1}}$	(Disk) Unit 1 (Select)
$\overline{\text{UNIT2}}$	(Disk) Unit 2 (Select)
$\overline{\text{UNIT3}}$	(Disk) Unit 3 (Select)

ABBREVIATIONS (Continued)

WRITE	Write (Command decode)
$\overline{\text{WRITE}}$	(Complement of above)
XFER DONE	Transfer (of data) Done
2nd Request	Second (data) Request (from 4046 Control to Processor)

SECTION II

INSTALLATION

2-1 GENERAL

This section provides detailed information and procedures for installing the Data General Disk Cartridge System. The Disk Drive unit (4047A or 4047B) is packed and shipped in a special reusable container which may be retained for reshipment use. Place the shipping container right side up and open the center flaps. Exercise care when opening the container to prevent damage to the finished surfaces of the unit. The equipment manuals and unpacking instructions should now be accessible from the carton. Follow the unpacking and installation procedures as listed. It is recommended that three people be used to remove the Disk Drive unit, two people to lift the unit from the carton, and one person to assist in clearing away the empty carton. The next important step in unpacking the Disk Drive unit is to remove the shipping clamp from inside the unit. This should be done as soon as the unit is removed from its shipping carton, to eliminate the possibility of damage due to any inadvertent attempt to operate the unit with the shipping clamp still in place within the unit. The top cover will have to be removed from the unit first to provide access to the Shipping Clamp. The clamp holds the head positioner over track 0. The presence of this clamp prevents the insertion of a cartridge. No other shipping clamps are included. Inspect the unit both internally and externally for evidence of shipping damage. If any damage is present do not attempt to operate or connect power to the unit, rather notify Data General Field Service and the carrier company immediately. If no visible damage is present reinstall the top cover and complete the rest of the installation procedures for the Disk Drive unit.

The Disk Adapter unit, 4046 Control assembly and cables, are shipped together in one container. This container actually consists of two protective containers which are packaged in the form of a box within a box. The inside container rather than a box is a special styrofoam container used to hold the Disk Adapter unit and cables. The 4046 Control Assembly is wrapped in a cardboard container and packaged on top of the styrofoam container. The cables are packed inside the styrofoam container in the rear of the Adapter unit. Inspect both shipping containers for any visible intransit damage such as would result from dropping or being punctured or crushed. Contact the carrier and Data General Field Service immediately if any damage is discovered, specifying the nature and extent of damage.

2-2 INSTALLATION AND CHECKOUT PROCEDURES

The following paragraphs describe the proper method of unpacking the Disk Adapter unit and 4046 Control assembly, and procedures for verifying, operationally, and proper installation. It is recommended that all shipping hardware, packing material and cartons be saved and stored (after unpacking) in the event the Adapter unit and 4046 Control assembly are ever reshipped.

2-2.1 Installation Procedures

The following procedures are used in unpacking and installing the Disk Adapter unit and 4046 Control assembly:

a) Place the shipping container right side up and open center flaps. Figure 2-1 shows the relative positions of the outer and inner carton.
b) Remove top layers of cardboard.
c) Remove the 4046 Control assembly and Document packages from top of the styrofoam container.
d) Remove the four foam cushions from each corner. These cushions are used both to secure the inner box in position and absorb shock and vibration during shipment.
e) Open the 4046 Control assembly package and examine the PCB assembly closely for any possible shipping damage. If any damage is evident do not install the PCB assembly in the Processor, rather notify Data General Field Service immediately.
f) If no visible damage is present install the 4046 Control assembly into the Multiple PCB Connector slot (within the Nova or Supernova) prewired for the 4046 Disk Control.

CAUTION:

MAKE SURE ALL POWER HAS BEEN REMOVED FROM THE PROCESSOR BEFORE INSTALLING THE 4046 CONTROL PCB ASSEMBLY, OR ATTACHING THE COMPUTER-TO-ADAPTER CABLE.

g) At this point it is assumed that the Disk Drive unit has been removed from its carton, the shipping clamp has been removed, and the unit has been inspected. Preparatory to installing the unit into a standard 19" rack, each supporting slide rail for the unit must be mounted to the rack cabinet. The procedures for securing the slide rails and subsequent mounting of the unit onto these rails are as follows:

1) Slide rail dimensions are 20 9/16" from (mounting) face to face.
2) See the Installation drawing, Figure 2-2 for the proper placement of nut plate and speed nut clip hardware. The amount of clearance required between the top of the Disk Drive unit and any panel or equipment located immediately above it in the rack is also specified on the Installation drawing. Use the (12) #10/32 machine screws shipped in the container along with the Disk Drive unit to fasten the slide rails to the rack cabinet.
3) Verify rails are opened to the stop position and remain in this position while the Disk Drive unit is being placed onto the rails. This is required to facilitate alignment of the holes in the rear of the drive unit enclosure

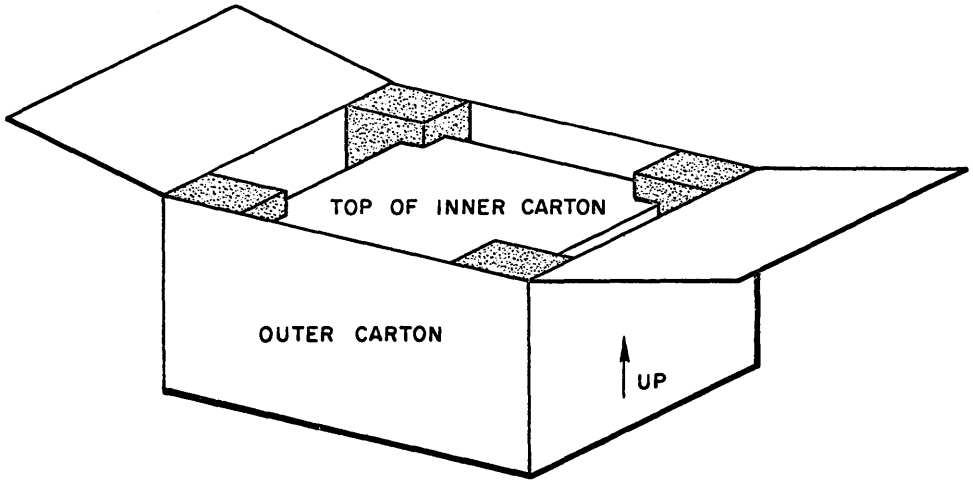


Figure 2-1. Relative Positions of Outer and Inner Shipping Cartons.

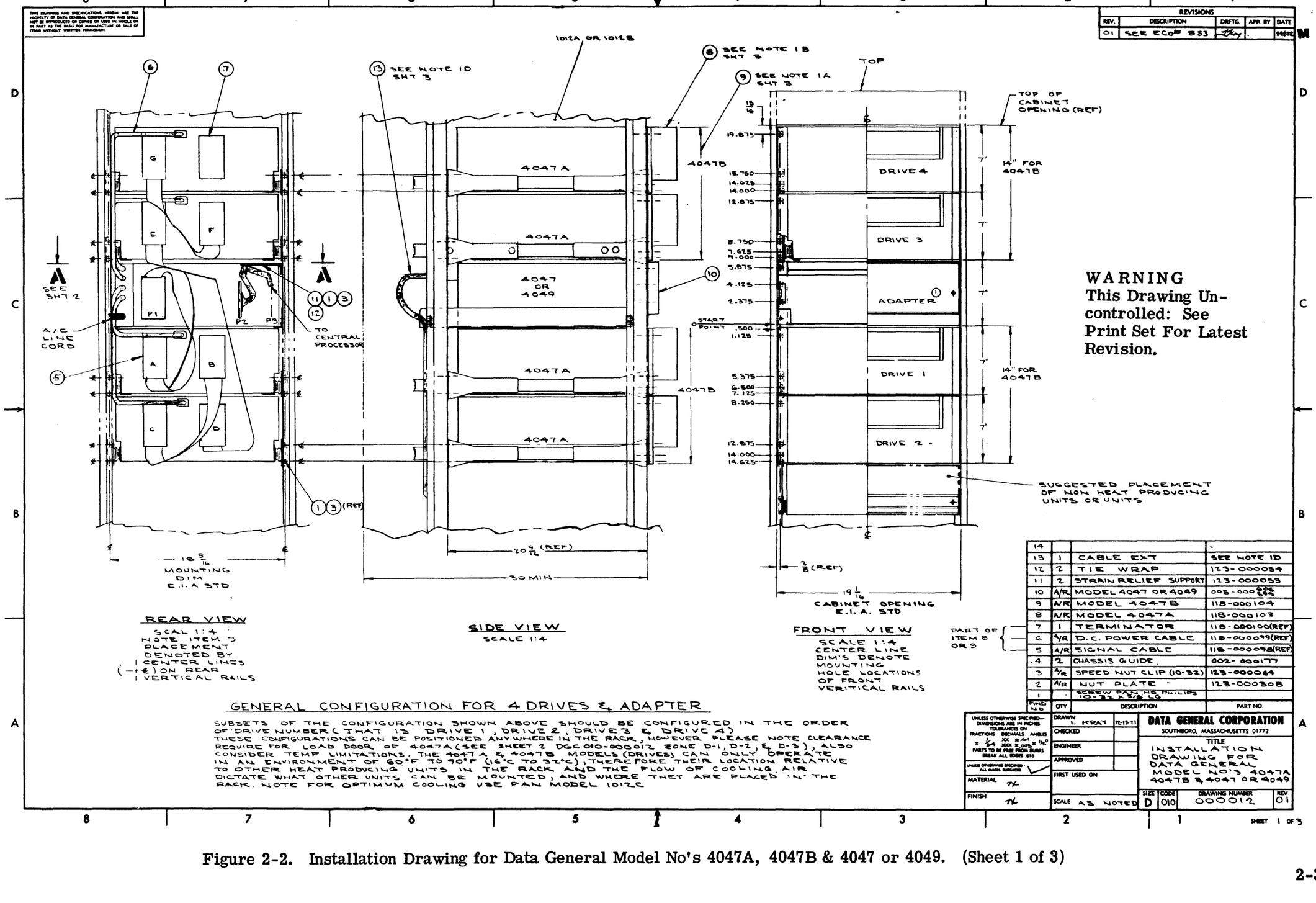


Figure 2-2. Installation Drawing for Data General Model No's 4047A, 4047B & 4047 or 4049. (Sheet 1 of 3)

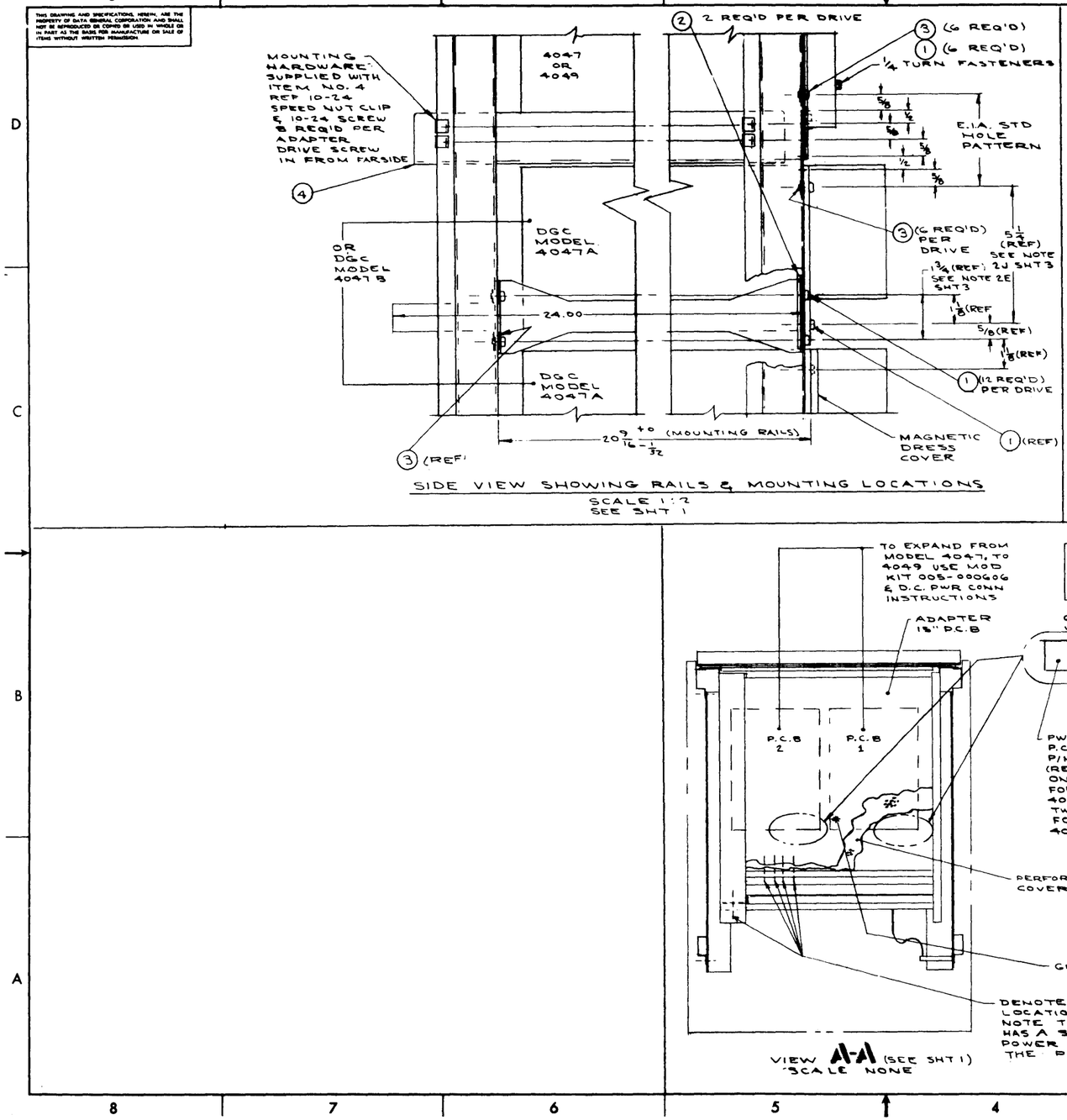


Figure 2-2. Installation Drawing for Data General Model No's 4047A, 4047B & 4047 or 4049. (Sheet 2 of 3)

NOTES:

1. CONFIGURATION GUIDE

   A. Model 4047B is shipped as two separate drives.

   B. If Model 4047B is used mount removable Disk Cartridge Drive below fixed Disk Cartridge Drive so that swing radius of the load door on Disk Drive doesn't create a configuration problem. (See sheet 2 DGC 010-000012 in zone D-1, D-2, and D-3).

   C. P3 on Adapter (4047 or 4049) is only used for dual processor mode. (See Figure 1-4 in DGC instruction manual).

   D. Cable or cables used to interface Adapter (4047 or 4049) to Central Processor or processors are supplied with Model 4046 control (these are DGC P/N 005-000468 or 005-000803).

   E. Unit placement in the rack & cooling guide (See DGC 012-000012, Sheet 1).

2. SUGGESTED INSTALLATION PROCEDURE

   A. Remove side panels from cabinet, DGC Model No. 1012A or 1012B.

   B. Establish "Start Point" for particular configuration (See DGC 010-000012, Sheet 1) and install (item 4) (two places as shown) using Mounting hardware supplied.

   C. Install clip nuts in specified locations per DGC DWG 010-000012, Sheet 1 & Sheet 2 (NOTE ALL hardware dimensions shown are typical for both front vertical mounting rails.)

   D. Remove slides from 4047A or 4047B and attach mounting clips to stationary portion of slides, 20-9/16 inches apart (See DGC DWG 010-000012, Sheet 1 & Sheet 2)

   E. Mount slides as shown on DGC DWG 010-000012 Sheet 2 (As required). Note that the slide mounting hardware is located on 1-3/4" centers. Extends slides forward until slide lock is engaged.

   F. Insert Model 4047A or 4047B into slides, engaging guide bullets in back of slides, then engage friction fasteners at bottom of slides.

   G. CAUTION: At this time remove top cover of 4047A or 4047B and remove clamp that is holding Head Positioner over track 0 (this clamp is used for shipping only) then replace top cover. This step is a necessary prerequisite before Disk Cartridge (Model 4047C) can be inserted.

   H. Unlock slides and push Model 4047A or 4047B into the rack until they stop against the front vertical mounting rails.

   J. Secure Model 4047A or 4047B with 10-32 screws as denoted on Sheet 2, DGC 010-000012, then mount magnet dress covers over hardware.

   K. Slide adapter (Model 4047 or 4049) onto guides (item 4) and secure to front vertical mounting rails with 10-32 screws, mount console and secure console using 1/4 turn fasteners.

   L. Install cables as denoted on Sheet 1 DGC 010-000012 (NOTE DAISY-CHAIN OF SIGNAL CABLING.) For expansion of 4047, 4047A or 4047B, See DGC power cable connection instruction on Sheet 2, zone B-1 (DGC 010-000012).

WARNING
This Drawing Uncontrolled
See Section VII
For Latest Revision.

REVISIONS				
REV	DESCRIPTION	DEPTL	APP BY	DATE

DRAWN	L KRAY	4-3-79	DATA GENERAL CORPORATION
CHECKED			SOUTHBORO, MASSACHUSETTS 01772
ENGINEER			TITLE
APPROVED			
FIRST USED ON			
SCALE			SIZE D · CODE 010 · DRAWING NUMBER 000012 · REV 06

1 3 of 3

Figure 2-2. Installation Drawing for Data General Model No's 4047A, 4047B & 4047 or 4049. (Sheet 3 of 3)

with the alignment studs located on the rear of the slide shaft. The two holes in the bottom of the drive unit enclosure should also align with nylon expansion washer. (This washer is expanded by compression and is screw adjusted as part of the Disk Drive unit securing hardware.)

4) Push the unit back into the cabinet. Remove magnetic covers from the sides of the front panel. Secure front panel of unit to rack with hardware supplied, making sure that the nut place and speed nut clips are in the proper position (as shown on the installation drawing) before inserting the screws.

h) Release the straps on the styrofoam container, and remove the cover from the container.

i) Using three people (two to lift the unit from the container, and one person to remove the container once the equipment has been lifted clear) remove the Adapter unit from its container.

j) Verify that the source end of the Disk Drive dc power cable is connected inside the Adapter unit as follows:

1) Remove the logic interface board from the Adapter enclosure. The perforated cover should now be exposed.

2) Peek through the perforated cover and verify that the Disk Drive dc cable is connected to the screw terminals located on the rear edge of the power supply Printed Circuit board.

3) Verify that the dc power cable is connected as follows; the two blue wires connect to the HV (or BLU) screw terminal. The two red wires connect to the +HV (or RED) screw terminal. The braided ground wire connects to the GND (or BLK/BRN) screw terminal. Screw terminal markings identified above are etched onto the printed circuit board. Additional dc power cable connection data may be found on the Installation drawing referenced above. (The Data General part No. for the dc power cable is 118-000099.)

4) After verifying that the dc power cable is properly connected, reinstall the logic interface board back into its original position within the Adapter enclosure. If the dc power cable is not connected notify Data General Field Service.

5) Insert key into Power lock switch on Adapter front panel, and verify lock switch is in the "Off" or far left rotational position. Plug in the 110 volt ac line cord. Turn key, rotationally, to the far right, or "On" position and verify that the Fan within the unit comes on. Do not attempt further installation if the Fan is inoperative.

k) Using the same number of personnel mount the Adapter in a standard 19" rack, securing it into position as follows:

1) The supporting rails for the Adapter unit and hardware are shipped in the Adapter container and should be installed as shown on the Installation drawing referenced above.

2) Position speed nut clips as shown on Installation drawing.

3) Place Adapter unit on rails and slide into position in the cabinet. (A rear stop is provided for the unit.)

4) Secure Adapter to rack with hardware supplied.

5) Install console panel, secure by the two 1/4 turn fasteners.

l) Connect the Adapter unit dc cable into the power connector on the rear panel of the Disk Drive. Figure 2-3 is a simplified drawing showing cable installation

m) Connect (Adapter to Drive) ribbon type signal cable (Data General #118-000098) to Adapter connector P1 (Plug Interface back panel in rear of Adapter.) Connect other end of cable to Disk Drive unit. (If this is a single Drive installation connect terminator card (Data General #118-000100) into opposite input/output connector. Reference Figure 2-2, the Installation drawing, for proper daisy-chaining of input/output cabling in multiple drive installations.

Note; Model 4047B will require one level of daisy-chaining to be installed. An additional ribbon type signal cable is provided for this purpose. Terminate unit the end of the daisy-chain as described above.

n) Connect Computer I/O Cable (#005-000468) into Connector P2 of the Plug Interface back panel (located in the rear of the Adapter unit. The connector should be installed with the ground tabs pointing toward the ground tabs of connector P3 (also on the back panel PCB). Secure connector ground tabs with two #4/40 Phillips head screws. Connect other end of cable into the designated 50* pin mating connector located in rear of the processor enclosure.

o) Set the LOAD RUN switch on the Disk Drive unit to the LOAD connect position. Adapter ac line cord to a standard 110 volt outlet. Insert key into POWER lock switch on Adapter front panel and turn to the ON position. (The key is removable when the lock is turned to the far right rotational (ON) position.)

p) Verify POWER indicator of Disk Drive unit or (units) comes on. Do not attempt to operate until all power distribution is verified.

q) Verify that the LOAD indicator of the Disk Drive unit is also illuminated and the READY indicator (of the Disk Drive unit) is extinguished.

r) Open the cartridge receiver door, insert a Cartridge. Close the cartridge receiver door and press the LOAD RUN switch to the RUN position. Verify that the READY light comes on approximately one minute after switching to RUN. Verify the CHECK indicator on the Disk Unit drive is extinguished. If CHECK comes on with READY switch back to LOAD, wait until the drive stops, then switch to RUN again. If this still fails to clear CHECK perform these procedures again using a different Cartridge. If this fails to clear CHECK discontinue further operation and notify Data General Field Service.

s) After the Disk Drive has been loaded with a Cartridge and is READY (with CHECK extinguished) power may be applied to the Processor in preparation for performing the checkout procedures.

* 100 pin connector for 4 and 10 slot 800 and 1200 Computers.

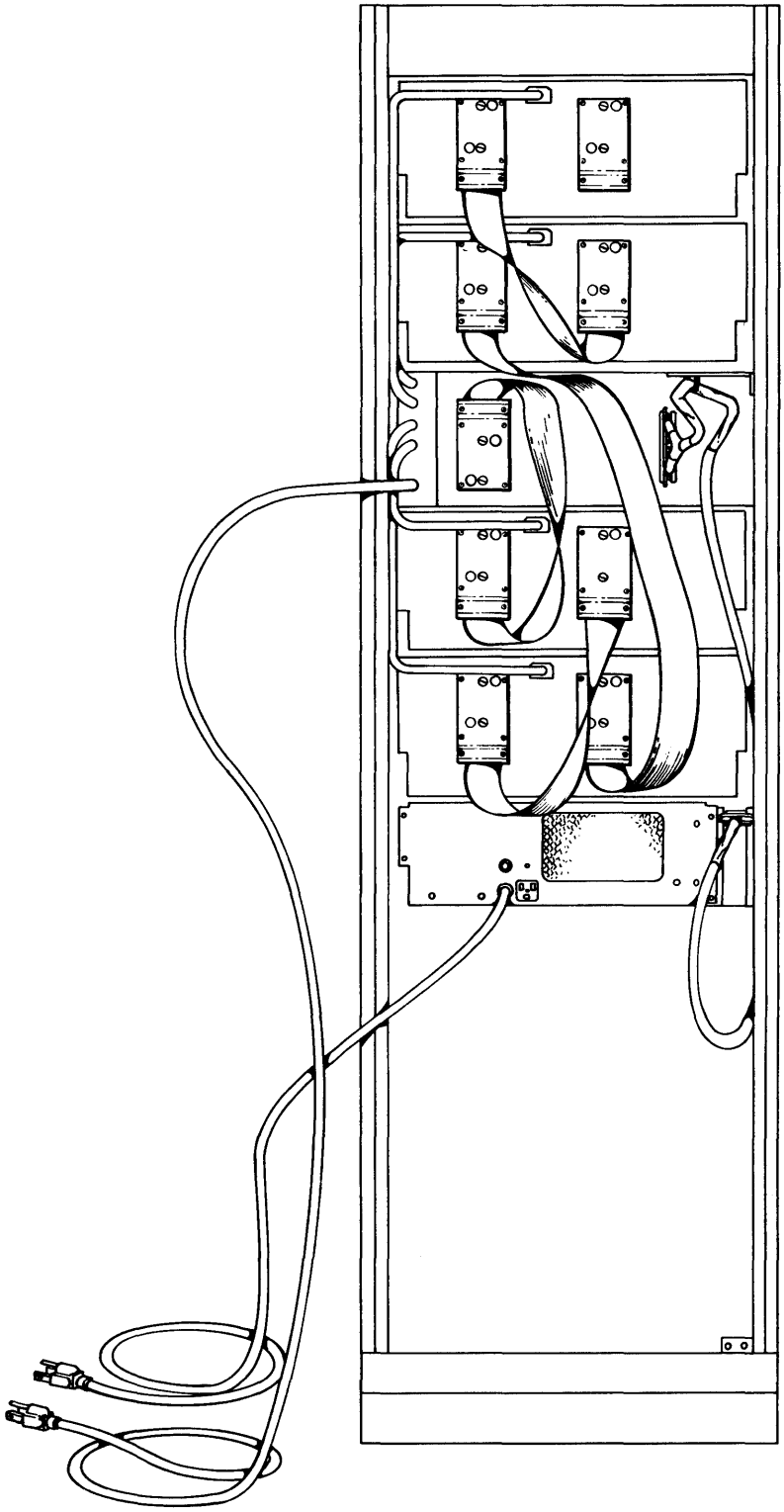


Figure 2-3. Inter-Unit Cabling for Controller 4046 and Adapter 4047 or 4049

2-2.2 Checkout Procedures

The following procedures are used in initial start-up and operational checkout of the Disk Cartridge System installation.

a) Using the Binary Loader load the Moving Head Disk Control Diagnostic test (DGC Tape #095-000069) into the Processor through the teletype or high speed reader. Review the test description presented in DGC document #097-000039.

b) Start the program at location 000002_8. Teletype will request input data as to type and Disk Unit number of system under test:

Teletype: "TYPE 0 FOR CARTRIDGE
1 FOR 10 SURFACE DISK PACK
2 FOR 20 SURFACE DISK PACK"

User Response: 0

Teletype: "TYPE UNIT NUMBERS (0-3) TO TEST"

User Response: n Carriage Return

Where n is the Unit number of the Disk Drive to be used during the test.

c) Program takes approximately 5 minutes running time and prints out the word PASS upon the successful conclusion of the test. The test will continue as long as it is allowed to run. Verify test is completed successfully.

d) If the program fails to conclude successfully, reference Sections 3 and 4 of DGC Manual #097-000039 for the various control options provided by the test program when proceeding from an error halt.

NOTE: Special entrances to the test program in the form of Starting Addresses SA4 or SA5 are provided to set the Device Select Address data into the program. This information defines the Control under test as being wired to respond to Device code 33_8 (as a primary control) or 73_8 (as a secondary control). The program comes to a halt after entering from either SA4 or SA5 and will enter a Jump loop if continued from the halt. Therefore, after using either SA4 or SA5 to change the above mentioned program data, enter the program from SA400, or enter from SA2 if a different unit is to be tested. When the test is entered from SA2, the program assumes the Control is wired for Device code 33_8 and will automatically proceed to SA400, the starting location of the diagnostic tests.

e) Load the Moving Head Disk Reliability test program (DGC Tape #095-000068) into the Processor through the teletype or high speed reader. Review the test description presented in DGC document #097-000038.

f) Start program at location 000002_8. Program will output through teletype:

"TYPE THE NUMBER OF DISK SURFACES"

User Response: 2 Carriage Return

g) Program requires approximately 24 minutes running time for the Nova 1200 and approximately 15 minutes running time for the Nova 800 and Supernova Processors.

h) Program types "PASS" on each successful completion and will run continuously. The operator may actuate any key on the teletype to obtain a report of the number of words written and read, and the number of errors during random testing.

i) In the event the program fails to complete successfully, the various diagnostic and error options may be referenced from the program reference manual DGC #097-000038.

NOTE: This program also provides 18 special entrance starting address locations which may be used for a variety of tests and unique functions, e.g., the Command String Interpreter. Starting address locations 4 and 5 can be used to change the Device address of the Control as described previously in the Note under step d of this procedure, with the added flexibility of using any of the other 16 special entrance address locations between 400 and 417 after this operation has been completed.

SECTION III

OPERATION

3-1 GENERAL

Only one switch is used to supply power to both the Adapter unit and the Disk Drive unit. This switch is labeled POWER and is located on the left side of the Adapter front panel. A key is required to both operate the lock portion of the switch, and to turn the switch to its ON and OFF rotational positions. Description of the Disk Drive controls, interlocks, and indicators may be referenced in document D3031-670 shipped with the Disk Drive unit. Operation and programming information for the Nova or Supernova Processor may be referenced in Data General publication "How to Use the Nova Computers".

SECTION IV
THEORY OF OPERATION

4-1 INTRODUCTION

This section contains detailed information describing the functional operation of the Controller type 4046, and the 4047 (and 4049) Adapter Logic Interface. A brief description of the Adapter power supply is also included at the rear of this section. The logic diagrams for the 4046 Controller (Drawing #001-000122, sheets 1-3), the 4047 Plug Interface, (Drawing #001-000142), the 4047 & 4049 Logic Interface, (Drawing #001-000143), and the 4047 Disk Power Supply (Drawing #001-000186) are found in the print set of this manual. These diagrams should be referenced when reviewing the detailed logic descriptions of this section. The functional discussion of this chapter is divided into to two sections, the first of which describes the operation of the 4046 Controller. A description of the functional operation of the 4047 & 4049 Logic Interface is provided in the second half of this chapter. Both descriptions are supported by Figure 4-1, which is a detailed functional block diagram of the 4046 Controller and the 4047 & 4049 Logic Interface.

4-1.1 Logic Notation

Certain logic notations, used on both the engineering logic drawings and Figure 4-1, may possibly require a brief explanation as to proper functional interpretation. The signal outputs from flip-flop and one shot terminals are designated as follows:

a) The signal output from the set terminal of the device is designated with the signal name and a (1) following to designate the set terminal and the logic 1 signal that will be available at that terminal when the device has been electrically switched internally to the set state (or in the case of a one shot when the device is cycling).

b) The signal output from the reset terminal of the device is designated with the signal name and a (1) following, but also with a bar over the entire expression to designate the reset terminal and the logic 0 signal that will be available at that terminal when the device has been electrically switched internally to the set state (or in the case of a one shot when the device is cycling).

For example consider the Data Late flip-flop. If the flip-flop is set it will provide a logic 1 on the DATA LATE (1) line from the set terminal of the device, and a logic 0 on the $\overline{\text{DATA LATE}}$ (1) from the reset terminal of the device. Obviously, the logical complement of the signals described above will be displayed on the associated terminal lines when the device is in the reset state. These designations are helpful when one reviews the engineering logic diagrams, in that they assist in differentiating between signals produced by individually functional bistable or monostable devices and signals produced by the remaining logical elements and storage devices.

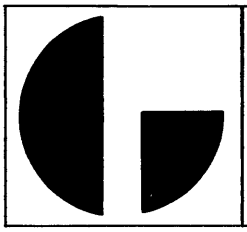
4-2 CONTROL TYPE 4046 FUNCTIONAL DESCRIPTION

The 4046 Control is divided into three major logic sections; the I/O section, the Register section, and the Timing section. As shown on Figure 4-1, the Processor interfaces primarily with the I/O section and the Register section. The 4047 (& 4049) Logic Interface exchanges signals with all three sections of the Control. Some of these signals are routed through a 2 Channel, 24 bit Multiplexer in the Adapter Interface, and are shown on Figure 4-1 as signal flow lines interrupted by the Multiplexer block. The remaining interface signals completely bypass the Multiplexer and are shown on Figure 4-1 as signal flow lines non-interrupted by and passing directly thru the Multiplexer block. This illustrating convention was used in the preparation of Figure 4-1 as a means of differentiating between interface signals switched by the Multiplexer, and those signals wired directly across the interface. The Multiplexer channel selection is controlled by an ADAPTER SEL A signal, which selectively enables signal lines between the Adapter and one of two possible 4046 Controls (designated "A" and "B"). When ADAPTER SEL A is at the logic 1 or high level the signal lines from Control assembly "A" (connected into P3 of the back panel) are selected. Conversely, the low or logic 0 level on the ADAPTER SEL A selects the signal lines from Control assembly "B" (connected into P2 of the back panel). The switching of the Adapter Multiplexer is discussed further in the second half of this chapter. However, it is assumed that the "B" Control assembly has been selected (by the Adapter Multiplexer) as a means of expediting the discussion concerning the Operation of the 4046 Control assembly. The operations of the three logic sections of the Control assembly will each be described in the course of the following discussion.

4-2.1 Typical Instruction Sequence & Logical Operations

Each I/O communication between the Processor and the 4046 Control must contain the Device Select code. Device Select code 33 is called out on Figure 4-1, however Device Select code 73 is required for the second Control assembly if two Control assemblies are located within one Processor. The proper Device Select code (either 33 or 73 depending on the configuration) causes a DP SELECT signal to be produced, which effectively removes an inhibit from the I/O Control Input gates. At this time the I/O bus (instruction) signal function accompanying the Device Select code will be gated into the I/O section to enable the proper logic for implementing the instruction. DP SELECT also removes an inhibit from the SELB (Selected Busy) and the SELD (Selected Done) output gates. In the uninhibited state these gates provide information (for the Processor) as to whether the Control is busy or done. At this point the discussion will describe an example series of I/O instructions designed to facilitate and implement a write operation, and will describe the particular operations invoked by these instructions. It is pointed out here that the sequence of instructions used in the example do not constrain the programming for this equipment to the order described or infer any other such restrictions on the use and control of the Disk system.

The first instruction issued in the example sequence will be a DATOC which loads the drive, head, sector and sector count data (from the specified accumulator) for the upcoming operation. Sector Count is loaded with 2's complement of total consecutive sectors to be written. (It is necessary to load the unit code into the Controller prior to checking the status of DSK Ready.) The next instruction issued in the se-



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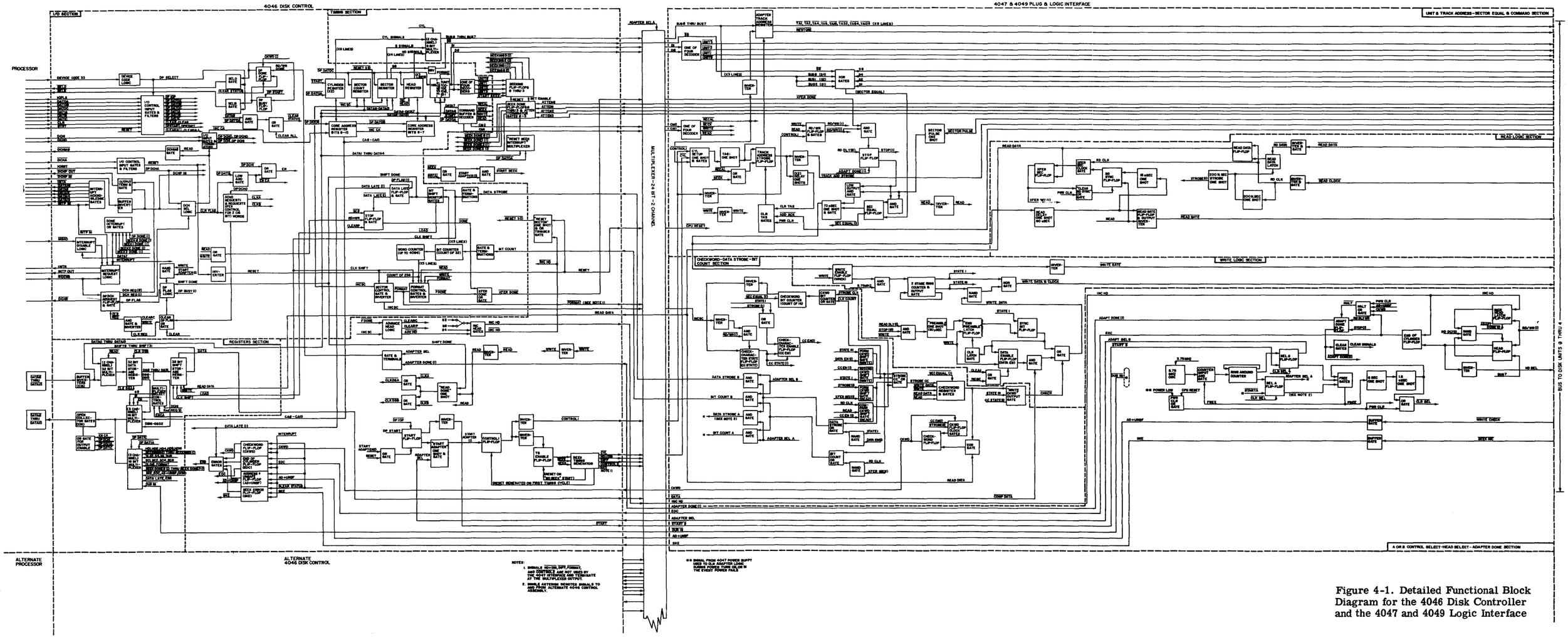

Figure 4-1. Detailed Functional Block Diagram for the 4046 Disk Controller and the 4047 and 4049 Logic Interface

quence will be a DATIA which will read the status word back into the specified Processor Accumulator. At this time, the Processor program will check the various status bits to determine if the unit is ready to perform a transfer Operation. The next instruction issued (assuming the unit is ready) will be a DATOA which will load the cylinder address and command mode data from the specified accumulator. The command mode bits 6 and 7 of this data will be set to a 10 configuration for a SEEK operation. The DATOA instruction function bits 8 and 9 will be set to a 11 configuration to issue an IOPLS to the Control. The SEEK operation is started by the IOPLS function. The interrupt logic of the I/O section can be disabled by the Processor "Mask Out" I/O instruction with a 1 set into bit 7 of the specified accumulator. However, for this discussion it is assumed that interrupts are enabled. Therefore, when the SEEK operation has been completed, the Control will issue an INTR to the Processor, which in turn will issue an INTA to the Control. INTA (providing the DP INT REQ and INTP IN signals are present) will allow the Control to place its Device Select code on the I/O Data bus. After receiving the Device Select code, the Processor will (to continue the example) issue a DATOA instruction, which will provide data (from the specified accumulator) for resetting the interrupt. This accumulator data will also encode bits 6 and 7 into a 01 configuration for a WRITE command. The last instruction in the example sequence is a DATOB which will load the Core Address register with data from the accumulator specified. The DATOB instruction function bits 8 and 9 will be set to a 01 to issue a STRT (I/O bus) signal to the Control. Now that the I/O instruction sequence has been specified, along with their general functions, the following discussion will describe the incremental flow of operations through the Control upon receipt of each instruction starting with the DATOC defined as the first I/O instruction of the example sequence.

The DATOC bus signal, together with the Device Select code for the Control will produce a $\overline{\text{DP DATOC}}$ signal, which will enable the Sector Count, Sector, Head, Format, and Unit Code registers to be loaded from the output of the 16 buffer inverters (Registers section) being driven by the DATA 0 thru $\overline{\text{DATA15}}$ I/O bus lines. The next instruction, DATIA, together with the Device Select code for the Control will produce a $\overline{\text{DP DATIA}}$ signal, which enables a 2 channel, 16 bit Multiplexer to place the system status microcoded word on the I/O bus lines ($\overline{\text{DATA0}}$ thru $\overline{\text{DATA15}}$ via the 16 open collector gates. As shown on the Figure, the 2 channel, 16 bit Multiplexer and 16 open collector gates are located in the Registers section, and are both enabled (for outputting the status word) by the $\overline{\text{DP DATIA}}$ signal. The open collector gates are normally inhibited by the output an OR gate, and any one of four logic 0 signals (including $\overline{\text{DP DATIA}}$) will cause the OR gate to release the inhibit level on the 16 open collector gates driving the I/O bus. As a side note to the discussion, the 2 channel, 16 bit Multiplexer can be enabled to select the opposite channel by a $\overline{\text{DP DATIC}}$ signal (derived from the DATIC I/O bus signal). This channel provides microcoded information as to the values contained in the Unit, Head, Sector and Sector Count registers. $\overline{\text{DP DATIC}}$ as a logic 0 signal also causes the OR gate to release the inhibit level on the 16 open collector output gates, placing the data from the four registers mentioned above onto the I/O bus lines. This facility allows the Processor to recall this information (under program control) either prior to a transfer (or Seek) operation or upon the conclusion of a transfer (or Seek) operation as reference data for the operational program.

To return to the example instruction sequence, it is assumed that the operational program finds (through the data of the status word) that the selected Disk Drive unit is ready to perform an operation. The next instruction in the sequence is a DATOA, which will load both the Cylinder register with the cylinder address and the Command buffer (and decoder) with the (10) SEEK code preparatory to performing a Seek operation. Since the Seek operation is started by an IOPLS, this signal function will also accompany the DATOA bus signal. Both signals present on the I/O bus with the proper Device Select code for the Control will enable the I/O Control Input gates to produce a $\overline{\text{DP DATOA}}$ signal (from the input DATOA) and a $\overline{\text{DP IOP}}$ signal (from the input IOPLS). The $\overline{\text{DP DATOA}}$ loads the Cylinder register and Command buffer from the outputs from 10 of the buffer inverters (located in the Registers section) being driven by the data on the I/O bus lines ($\overline{\text{DATA6}}$ thru $\overline{\text{DATA15}}$). The Command buffer is physically part of the 10 bit Cylinder register, using the two most significant stages of the register, with the cylinder data stored in the remaining eight least significant stages. The outputs of the Command buffer CM1 & CM2 are decoded to place a logic 0 enabling signal on one of the four command lines, $\overline{\text{RECAL}}$, $\overline{\text{SEEK}}$, $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$. (The five most significant bits of the accumulator data specified by the DATOA command are used to clear the error status flip-flop, clear the Done flip-flop, and clear the Seek Done (interrupt) flip-flops. However, at this point in the example discussion it is assumed all of the 4046 Controller logic was initialized during turn-on. The use of these clearing bits in the DATOA instruction will be described further on in this discussion.) The $\overline{\text{DP IOP}}$ in the logic 0 state is used to enable the direct set input of the Start flip-flop of the Timing section, the set output of which causes an inverter to place a logic 0 signal on the $\overline{\text{START}}$ line to the A or B Controller Select logic of the Adapter Interface.

The $\overline{\text{START}}$ signal from the Controller (under discussion) is wired into the "B" computer connector (P2) of the Adapter Plug Interface, and hence becomes a $\overline{\text{START B}}$ signal within the Adapter. The $\overline{\text{START B}}$ signal is essentially a request from the Controller, that it be connected (via the Adapter 2 channel Multiplexer) with the Adapter. If the Adapter is not busy with the "A" Control (if an "A" Control exists) the SEL B flip-flop in the Adapter will become set and transmit a logic 1 ADAPTER SEL B signal back to the Controller. (ADAPTER SEL B becomes ADAPTER SEL through the computer connector, P2. ADAPTER SEL B switching to the logic 1 state also indicates the 2 channel Adapter Multiplexer has been switched to connect the Adapter interface signal lines with the "B" Controller.) The logic 1 ADAPTER SEL signal provides the remaining enable signal required by a trigger gate driving the "Start Adapter" one shot (in the Timing section of the Controller). As the one shot enters its cycle it produces a logic 1 START ADAPTER (1) signal which performs three important functions; i. e., sets the Control 1 flip-flop, pro-

vides one of the enabling signals for the START SEEK function, and resets the Start flip-flop.

As mentioned previously a SEEK command decode signal is present and enables an OR gate (Timing section) to provide one of the requirements for producing a logical START SEEK signal. The other requirement is provided by the logic 1 START ADAPTER (1) signal. (It is noted here aside from the discussion that a RECAL command decode is the other OR signal that is capable of producing, in conjunction with START ADAPTER (1), a START SEEK logic 0 signal. Therefore, all of the START SEEK functions described below are repeated during a RECAL operation.) The logic 0 START SEEK signal strobes four AND gates each of which is associated with a dual flip-flop, dual gate logic configuration reserved as Seek indicators for each one of the four (possible) Disk Drive units connected with the system. The particular unit decode signal produced in the Controller (either UNIT0, UNIT1, UNIT2, or UNIT3) will be present and fully enable the associated AND gate. The logic 0 output from this gate in turn will enable the direct-set input of one of the associated (Seeking) flip-flops. The output from this flip-flop provides a signal indicating that the corresponding drive unit is presently "Seeking." For example, if a UNIT 0 signal is present when START SEEK occurs, the "Seeking 0" flip-flop will be set, and a SEEKING0 (1) logic 0 signal will be available to the 2 channel, 16 bit Multiplexer for reading (under control of an I/O DATIA instruction). The logic 1 set output from the Seeking 0 flip-flop, enables the D input of the Seek Done 0 flip-flop so that when the ATTEN0 signal from Disk Drive unit 0 is received (indicating that the Seek operation has been completed) the Seek Done 0 flip-flop will become set. The logic 1 set output from the Seek Done 0 flip-flop is fed back to the C input of the Seeking 0 flip-flop and provides an automatic reset for Seeking 0. The logic 0 reset output from the Seek Done 0 flip-flop, SEEK DONE0 (1), will be available to the 2 channel, 16 bit Multiplexer for reading (under control of an I/O DATIA instruction). Each of the other remaining Seeking, Seek Done logic groups (for UNIT1, UNIT2, and UNIT3) function exactly as described in the UNIT0 example above. A point to remember is that the Seek operation head positioning requires access time anywhere from 15 milliseconds to 135 milliseconds depending on the distance between the present track position and the track to be accessed. On this time scale the computer is capable of performing thousands of operations while waiting for a Seek operation to be completed. Hence, the Seeking and Seek Done logic provide a valuable monitoring function for the Processor. The Seek Done flip-flop also provide a logic 1 (set output) signal to the Done Interrupt OR gates in the I/O section of the Controller. A logic 1 on either of the four SEEK DONE lines (SEEK DONE0–SEEK DONE3) will initate a Processor interrupt (providing interrupts have not been disabled). In servicing the interrupt, the Processor should first clear the Seek Done interrupt by transmitting a DATOA instruction, which has an accumulator with bits 1 thru 4 configured such that it will clear the Seek Done flip-flop producing the interrupt. The interrupt functions for the Control are described further on in the discussion.

As mentioned previously the other logic function simultaneously enabled with the START SEEK function by the logic 1 START ADAPTER (1) signal is the CONTROL1 function. The START ADAPTER (1) signal unconditionally sets the Control 1 flip-flop. The logic 1 set output from the Control 1 flip-flop is used to drive two parallel inverters, one of which provides a logic 0 signal for the CONTROL1 line to Adapter Track Address logic section. The output from the other inverter is used to enable the direct set input of the TS (Time States) Enable flip-flop (in the Timing section of the Control), placing it in the set state. The set output from the TS Enable flip-flop is gated with a feedback signal from the ring-around timing one shots of the SEEK Timing Generator (Timing section of the Control) used to synchronize the firing order of the two series one shots.

The SEEK Timing Generator consists of the above mentioned two series one shots, and a four bit shift register. As long as the TS Enable flip-flop remains set the two series one shots will be allowed to sequentially cycle. The series one shot loop is triggered initially when TS Enable becomes set, and the logic set output from the second one shot in the loop strobes gating which will automatically reset the Control 1 flip-flop. This gating will also reset the TS Enable flip-flop if a logic 0 SEEK signal is present (indicating a SEEK command has not been decoded). However, in this example a logic 0 SEEK decode signal is present, and the TS Enable flip-flop will remain set to permit generation of the CYL, HD+DIR, DIFF and CONTROL2 signals via the periodic shifting of a 1 bit through the shift register on each cycle on the series one shot loop. Since a logic 0 SEEK signal is present a logic 1 will be set into the first stage of the shift register during the first cycle of the series one shot loop producing a logic 0 CYL signal. This 1 bit is advanced on each subsequent cycle producing the HD+DIR, DIFF, and CONTROL2 signals until it reaches the fourth stage of CONTROL2 stage where it (thru an inverter) resets the TS Enable flip-flop, ending the time states sequence.

As shown on the Figure 4-1, only the CYL output from the SEEK Timing Generator is used by the 4047 and 4049 Adapter logic interface. CYL triggers the CYL Setup one shot of the Track Address section of the Adapter logic. This one shot initiates a chain of logic which loads the cylinder data into the Adapter Track Address register, and sets up a Strobe line to the Disk Drive unit as a signal to read the data on the interface lines from the Track Address register. (A RECAL command decode present with a CONTROL1 signal are gated together to also produce a trigger for the CYL Setup one shot, however during a RECAL operation data in the Track Address register is ignored, and the heads are homed to track address 000.) All of the servo positioning calculations such as the head direction, difference between present head location and the new head location, are all performed within the Disk Cartridge Drive unit, and when the movement has been completed the unit responds by placing a logic 1 on its ATTEN line to the Adapter. The ATTEN signal is wired directly into the Control where it sets the associated Seek Done flip-flop, and produces a Processor interrupt (if interrupts are enabled).

As mentioned previously a logic 1 present on anyone of the four lines from the Seek Done flip-flops enables the Done Interrupt OR gates in the I/O section of the Controller. The Processor can disable interrupts by transmitting a Mask Out I/O instruction with bit 7 set in the specified accumulator. However, if interrupts are enabled, two other interrupt functions must be present in order to produce the INTR to the

Processor. The first function is provided by the Processor which samples interrupt requests at the start of each memory cycle by placing a RQENB signal on the I/O bus. The second function is provided by the Control Done Interrupt OR gates, which indicates when any Seek or Read/Write operation is done by placing a logic 1 on the INTERRUPT line. Thus, if interrupts are not disabled (i.e. the DP INT Disable flip-flop is not set) and an INTERRUPT signal is present (all operations Seek-Read or Write, are done), the next RQENB pulse generated by the Processor will set the DP INT REQ flip-flop placing an INTR signal on the I/O bus back to the Processor. Setting DP INT REQ will also place a logic 1 signal on the INTP OUT from the Controller (indicating that the Controller has priority). When the Processor acknowledges the interrupt it will respond with an INTA I/O bus signal. This signal will allow (if the DP INT REQ flip-flop is set) the Controller to place its Device code on I/O bus lines DATA10 thru DATA15. Upon receipt of the Controller's Device code, the Processor will respond (according to the example instruction sequence being described) with a DATOA I/O instruction which will specify an accumulator configured to load the Interrupt Reset register with data to clear the interrupt, and

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with mode bits 6 and 7 set to 01 for a WRITE command decode.

After the Processor transmits the WRITE encoded DATOA instruction, it will transmit a DATOB instruction, which will specify an accumulator holding the address data to be loaded into the Core Address register of the Control. The DATOB instruction will be configured such that bits 8 and 9 will be

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set to 01 as an I/O Start control function. Under these conditions the Processor will also generate an STRT I/O bus signal along with the I/O DATOB bus signal. The DATOB signal causes the I/O Control Input gates (of the I/O section) to produce a logic 0 DP DATOB signal which is used to load the outputs from the 16 buffer inverters (Registers section), being driven by I/O bus lines DATA0 thru DATA15, into the Core Address register. The STRT I/O bus signal causes the I/O Control Input gates (of the I/O section) to produce the logic 0 DP START and a logic 1 DP START signals. The logic 0 DP START signal provides a direct-set for the DP Busy flip-flop. (The DP Busy flip-flop at the start of all operations except for the first Read or Write operation after the Control has been cleared. Seek Done functions do not effect the DP Done flip-flop.) The logic 1 DP START pulse enables the C input of the Start flip-flop, providing an unconditional set function for the flip-flop. The logic 1 set output from the Start flip-flop drives an inverter, which in turn places a logic 0 on the START line to the Adapter. The START signal functions in the A or B Control Select section of the Adapter exactly as described previously, and results (after selection) in an ADAPTER SEL signal being sent back to trigger the "Start Adapter" one shot. The logic 1 set output from the "Start Adapter" one shot, START ADAPTER (1) in addition to resetting the Start flip-flop, sets the Control 1 flip-flop, and causes the two parallel inverters driven by the set terminal of the flip-flop to place logic 0 signals on the CONTROL1 lines. As described previously (for Seek operations), the output from one inverter sets the TS Enable flip-flop, which will release the series one shot loop (within the Seek Timing Generator) for one cycle. Since the SEEK signal is not present, both the TS Enable and Control1 flip-flops will automatically be reset on the leading edge of the second one shot in the loop. However, since CONTROL1 is true for 1.6 microseconds, the discussion will briefly consider the CONTROL1 logic functions within the Adapter logic interface for a WRITE command decode. Decoding of the Command mode bits is performed both in the Controller and in the Adapter, and in the case of the example under discussion a WRITE logic 0 enabling signal will be decoded. The logic 0 WRITE signal together with an inverted CONTROL1 signal are used to set the RD/WR flip-flop in the Command section of the Adapter logic. The RD/WR and WRITE signals within the Adapter are primary control signals for the write operation and will be discussed later on in the course of describing the write operation.

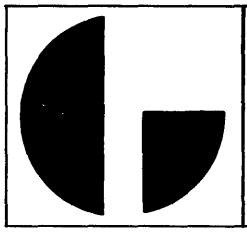
The WRITE logic 0 signal decoded in the Controller is inverted and gated with the logic 1 START ADAPTER (1) signal (in the I/O section) to produce a direct-set for the DP Flag flip-flop. The set output from this flip-flop places a logic 1 on the DP FLAG (1) line to enable the D input of the DP DCH REQ flip-flop. The next RQENB (I/O bus) signal from the Processor will drive an inverter to produce a logic 1 clock pulse for the DP DCH REQ flip-flop. The set terminal of the flip-flop, drives an open collector inverter, which when the flip-flop is in the set state will place a logic 0 on the DCHR bus line to the Processor. The logic 1 output from the DP DCH SEL flip-flop also provides one of the enabling inputs for the DCHP IN gate, with the other input enable provided by the output from an inverter driven by the DCHP IN I/O bus signal. If the Controller has issued a Data Channel request (DP DCH REQ flip-flop is set) to the Processor and it receives both a Data Channel Priority (by an input logic 0 DCHP IN signal) and a Data Channel Acknowledge (by an input logic 0 DCHA signal); the consequence of all three logic requirements being present is to set the DP DCH SEL (Data Channel Select) flip-flop. Setting this flip-flop indicates the Controller has been selected for a Data Channel transfer. Thus, the logic 1 set output from the DP DCH SEL flip-flop simultaneously releases four functional Data Channel gates for operation. The output from one gate so released is then dependent on whether a logic 1 READ signal is present or not. The output from the gate drives the DCHM0 I/O bus line to the Processor and will place a logic 0 signal on this line if READ is present. This low signal informs the Processor that the Data Channel operation is a Data Channel operation is a Data Channel In, and will thereby cause the Processor to generate a DCHI signal to transfer the assembled data from the Controller to the Processor. However, since the operation under discussion is a WRITE, the READ line into this gate will be at a logic 0 level allowing the gate to continue to hold the DCHM0 line to the logic1 level. This high signal informs the Processor that the Data Channel operation is a Data Channel Out, and will thereby cause the Processor to generate a DCHO signal to transfer word data from the Processor to the Controller. The second and third gates released by the set condition of the DP DCH SEL flip-flop are the receiving gates for the DCHI and DCHO gates, which when the appropriate bus signal arrives will produce the respective DP DCHI signal (and DP DCHI through an inverter) or a DP DCHO signal (and DP DCHO through an inverter).

The fourth Data Channel gate released by the DPDCH SEL flip-flop has two other logic 1 signal requirements; the logic 1 output from the AND gate monitoring the set output of DP DCH REQ flip-flop and the DCHP IN priority line, and the DP DCHA line from the bus receiver gate. All three logic 1 signal present will enable the fourth gate, thereby producing a logic 0 CLR FLAG signal. CLR FLAG as a logic 0 performs several important functions one of which is to drive a (low input) OR gate to place a logic 0 on the EN CA line (to the Registers section). The logic 0 on the EN CA line also drives another OR gate (in the I/O section) to place a logic 1 on the EN line (to the Registers section). EN CA as a logic 0 signal together with EN as a logic 1 enable the Contents of the Core Address register to be placed on the I/O DATA0 thru DATA 15 lines. This data defines (in the case of a WRITE operation) the core memory address location the contents of which are to be transferred to the Controller and subsequently recorded on the disk. The logic 1 EN signal is a common enable for the 3 channel 16 bit Multiplexer. The logic 0 EN CA signal together with the fact that a DP DCHI signal is not present (DCHI, as mentioned above, is transmitted from the Processor only if DCHM0 defines a READ operation, therefore since this is a WRITE operation DCHI will not be issued) produces an S0, S1 configuration causing the Multiplexer to place the contents of the Core Address register, CA0 thru CA15, onto the inputs of the 16 open collector bus gates. The logic 0 EN CA signal also drives an OR gate, the output of which releases an inhibit level on the open collector bus gates, thereby placing the data on the I/O bus lines DATA0 thru DATA15. The Multiplexer input control signals and the outputs produced by them are summarized in Table 4-1 below.

Table 4-1. 3 Channel Multiplexer Control Signals

CONTROL SIGNALS				MULTIPLEXER
EN	DP DCHI	2ND REQ(0)	$\overline{\text{EN CA}}$	OUTPUT
1	0	X	1	0
1	1	1	1	DS0 -DS15
1	1	0	1	DS16-DS32
1	0	X	0	CA0 -CA16

X = Don't Care Condition



The other important function of the logic 0 $\overline{\text{CLR FLAG}}$ signal is to toggle the REQ1 and 2nd REQ flip-flops, and to reset the DP Flag flip-flop when the second data word is received from the Processor. To digress for a moment, the parallel to serial, serial to parallel Control shift register is 32 bits long, and thus requires two Processor (16 bit) words to become filled. The logic responsible for monitoring each transfer in the form of two computer word groups is shown in the I/O section of Figure 4-1 as the DP Flag logic. (This logic consists of the above mentioned DP Flag, REQ1, and 2nd REQ flip-flops.) When the Controller is initialized all three flip-flops are placed in the reset state by a $\overline{\text{CLEAR}}$ signal, and as mentioned earlier, the WRITE and START ADAPTER (1) signal placed the DP Flag flip-flop in the set state. The outputs of the 2nd REQ flip-flop alternately enable either a $\overline{\text{CLK A}}$ gate or a $\overline{\text{CLK B}}$ gate, when the DP DCHO signal occurs and since at this time the flip-flop is in the reset state (due to $\overline{\text{CLEAR}}$ initialization), the $\overline{\text{CLK A}}$ will be enabled when the DP DCHO signal occurs (derived from the Processor's DCHO I/O bus signal.

Under these conditions the first $\overline{\text{CLR FLAG}}$ signal generated will set the REQ1 flip-flop while leaving the 2nd REQ flip-flop undisturbed. When the Processor has retrieved the first 16 bit word from the (CA register) specified memory location and placed it on I/O bus lines $\overline{\text{DATA0}}$ thru $\overline{\text{DATA15}}$, it will also transmit a DCHO pulse to signal the data is ready on the bus. The DCHO signal causes the series combination of a receiver gate and an inverter to produce a logic 1 DP DCHO signal, which in turn will enable the $\overline{\text{CLK A}}$ gate to place a logic 0 on its output signal line to the Timing section. The logic 0 $\overline{\text{CLK A}}$ signal enables an OR gate in this section to produce a $\overline{\text{CLK DSA}}$ logic 0 signal. $\overline{\text{CLK DSA}}$, in turn, as a logic 0 signal is used in the Registers section to enable the most significant half of the Data Storage register to be loaded with the data word from the Processor. The I/O data word present on input lines $\overline{\text{DATA0}}$ thru $\overline{\text{DATA15}}$ is routed in parallel to the Data Storage register through the series combination of the 16 buffer inverters followed by the 2 channel 32 bit Multiplexer. The Multiplexer is used for both the writing and reading data paths and is controlled by a $\overline{\text{READ}}$ signal, which in the logic 0 state switches the Multiplexer to provide a path for the SHIFT 0 through SHIFT 32 inputs. However, since this is a WRITE operation the Multiplexer provides two duplicate 16 bit paths to the 32 bit Data Storage register, one 16 bit path to the most significant half of the register, the other path to the least significant half. Thus $\overline{\text{CLK DSA}}$ loads DATA0 thru DATA15 into DS0 thru DS15, while alternate signal $\overline{\text{CLK DSB}}$ loads the data present on DATA0 thru DATA15 (when $\overline{\text{CLK DSB}}$ occurs upon receipt of the second computer word) into DS16 thru DS32. The $\overline{\text{DP DCHO}}$ signal (complement of the DP DCHO used to generate the $\overline{\text{CLK A}}$ signal described above) is used to drive an OR gate the output of which places a logic 0 on the $\overline{\text{INC CA}}$ line. This signal is used to increment the Core Address register in preparation for the Processor's DCHA signal which will be sent on the next Processor Data Channel break.

Since the DP DCH REQ flip-flop (I/O section) is still set after DS0 thru DS15 (Registers section) becomes loaded, the $\overline{\text{DCHR}}$ request will remain on the line and the DP DCH SEL flip-flop will also remain set when the Processor responds with the next $\overline{\text{DCHA}}$ acknowledgement. The next Processor DCHA signal will produce the $\overline{\text{EN CA}}$ and EN signals for reading the (updated) Core Address register out to the Processor exactly as described previously. This $\overline{\text{DCHA}}$ will also generate another $\overline{\text{CLR FLAG}}$ signal, which will clock the 2nd REQ flip-flop to the set state (due to the logic 1 placed on its D input by the set output from the REQ1 flip-flop) while clocking the REQ1 flip-flop to the reset state. (REQ1 toggles on this and all subsequent $\overline{\text{CLR FLAG}}$ signals.) Due to the fact that REQ1 was in the set state when this particular $\overline{\text{CLR FLAG}}$ occurred, $\overline{\text{CLR FLAG}}$ will be able to enable an AND gate which in turn will provide a logic 1 enable for an OR gate driving the reset input of the DP Flag flip-flop. Thus, the second $\overline{\text{CLR FLAG}}$, occurring with REQ1 in the set state will reset the DP Flag flip-flop. At this time the set terminal of the DP Flag flip-flop will place a logic 0 on the DP FLAG (1) line to the D inputs of the DP DCH REQ and Data Late flip-flops. The next $\overline{\text{RQENB}}$ bus signal will thus clock the DP DCH REQ flip-flop to the reset state, removing the logic 0 signal from the $\overline{\text{DCHR}}$ bus lines. Resetting the DP DCH REQ flip-flop also causes the gate driving the D input of the DP DCH SEL flip-flop to place a logic 0 on the line to the D input. Thus, the leading edge of the next bus $\overline{\text{DCHA}}$ will reset the DP DCH SEL flip-flop. It should be noted this $\overline{\text{DCHA}}$ can be generated (by the Processor) as a result of any other Data Channel device requesting service, and since DCHA is approximately 600 nanoseconds wide the leading edge of the DCHA (to some other peripheral Data Channel device) will have cleared the DP DCH SEL flip-flop to the reset state, and removed the Control's $\overline{\text{DCHM0}}$ signal from this bus line well in advance of the Processor reading the state $\overline{\text{DCHM0}}$ line to determine direction of data transfer. If no other Data Channel devices beside the single 4046 Controller are present in the Processor peripheral configuration, the DP DCH SEL flip-flop will remain set.

To return to the discussion, it was mentioned previously that the $\overline{\text{CLR FLAG}}$ signal also clocked the 2nd REQ flip-flop to the set state. This state will allow the subsequent DP DCHO signal to produce a CLK B signal, which in turn will produce a $\overline{\text{CLK DSB}}$ signal. This signal will load the least significant half of the Data Storage register (DS16 thru DS32) with the data present on I/O bus lines $\overline{\text{DATA0}}$ thru $\overline{\text{DATA15}}$ (via the 16 buffer inverters and the 2 channel 32 bit Multiplexer). It is noted that the next $\overline{\text{CLR FLAG}}$ (first DCHA of the next transfer) will switch the 2nd REQ flip-flop to the reset state. Thus, the $\overline{\text{CLK A}}$ gate will be enabled when the first DCHO (of the next transfer) arrives.

The logic 1 DP FLAG (1) signal from the DP Flag flip-flop is applied to the D input of the Data Late flip-flop. The clock input of the Data Late flip-flop is under control of a gate monitoring SHIFT DONE and the reset terminal of the (Data Late) flip-flop itself. If the Processor fails to complete the transfer of both words (and clear DP Flag) before a 32 bit shifting cycle is completed; the end of the 32 bit shifting cycle, denoted by a logic 1 SHIFT DONE signal, will enable the gate and set the Data Late flip-flop. This state of the Data Late flip-flop sets the Stop flip-flop and forces a $\overline{\text{XFER DONE}}$ which in turn results in termination of the operation.

To summarize at this point in the discussion, the Data Storage register is loaded with data to be written on the disk. The outputs from this register, DS0 thru DS32, are automatically loaded into the 32 bit shift register by the combined presence of logic 0 $\overline{\text{LOAD}}$ signal together with a logic 0 $\overline{\text{WRITE}}$

signal. $\overline{\text{LOAD}}$ is at the logic 0 level whenever the Bit Counter (count of 32) of the I/O section is reset or cleared. Meanwhile, the Adapter logic would be comparing the address data in the Control's Sector register with the sector address data from the Disk Drive unit as a means of locating the selected sector the data is to be written into. Once the proper disk sector is located, the Adapter logic will set the Write Enable flip-flop in its Write logic section, which in turn enables the $\overline{\text{WRITE GATE}}$ line driver while turning on the STATE I-STATE III counter (which functions as a write clock). The details concerning the logical operation of the Write logic section of the Adapter Interface are presented in paragraph 4-3.2 and hence only the generalities of the Adapter operations will be discussed here. The Adapter logic generates the DATA STROBE and BIT COUNT signals which are transmitted across the interface to the Controller. DATA STROBE, generated in the Adapter at STATE I time, produces (in the I/O section) a CLK SHIFT signal, which is used to shift the 32 bit shift register (Registers section). BIT COUNT generated in the Adapter at STATE III time drives the Bit Counter in the I/O section of the Control. The general relationship of these signals may be stated as follows: The STATE I timing signal used to write the Clock pulse on the disk. STATE I (or Clock writing time) also produces the DATA STROBE signal which (is sent across the interface to the Control's I/O section where it) produces a signal (CLK SHIFT) used to shift the next bit of the 32 bit shift register to the $\overline{\text{DATA}}$ terminal. The 32 bit shift register is shifted at STATE I time in preparation for writing (across the interface) the bit (in the most significant position of the register) onto the disk at STATE III time. AT STATE III time the Adapter Write logic section writes the bit on the disk, and increments the Bit Counter (in the I/O section of the Control) via the BIT COUNT interface line. Each bit written on the disk is also XORed (by a special algorithm) into the Checkword register in the Adapter logic to form the 16 bit checkword, which written on the disk as the last sector data word. The checkword is formed during any (write or read) data transfer operation. Each Checkword formed during a read operation is checked against the Checkword written on the disk to validate the transfer. The operation of the Checkword logic is detailed in paragraph 4-3.2.

After 32 bits have been shifted out, the Bit Counter upon reaching a count of 32 will allow a logic 1 SHIFT DONE signal to be generated. SHIFT DONE clocks the Data Late and DP Flag flip-flops, and since the DP Busy flip-flop is still set, the DP Flag flip-flop will be set (due to the logic 1 held on its D input by DP BUSY (1)). Setting the DP Flag flip-flop in turn places a logic 1 on the DP FLAG (1) line to the D input of the DP DCH REQ, so that the next $\overline{\text{RQENB}}$ signal from the Processor (via the I/O bus) will set the DP DCH REQ flip-flop and place a logic 0 signal on the $\overline{\text{DCHR}}$ line, requesting the next two computer data words. All of the previous Data Channel logic operations described above are repeated until such time as the Word Counter (driven by the overflow from the Bit Counter) overflows and produces an INC SC (Increment Sector Counter) signal.

The Word Counter is unique in that it performs two functions; counts number of words written into a Sector, counts number of words of Format data written on one track during special control operations used (to format the disk prior to recording) in Disk Pack systems. (Formatting is not required for Disk Cartridge systems.) The word counter is a basic binary counter which monitors the number of words written into each sector. Bit 9 of the counter (binary = 256) is connected into an AND gate which also requires a logic 1 on the $\overline{\text{FORMAT}}$ line (indicating that this is not a Formatting operation) and a logic 1 on the CLK SHIFT line. (Counter testing is done by CLK SHIFT as CLK SHIFT is derived from DATA STROBE. DATA STROBE in turn is generated in the Adapter at STATE I time, which is the time the Clock pulse is written on the disk track. Therefore, the logic monitoring the outputs from the Bit and Word counters is checked during the time the Clock pulse is being written on the disk.) All three signals (256, $\overline{\text{FORMAT}}$, and CLK SHIFT) present in the logic 1 state will enable the gate, which in turn will place a logic 0 on the $\overline{\text{INC SC}}$ line. The logic 0 $\overline{\text{INC SC}}$ signal also drives an inverter the output of which places a logic 1 on the INC SC line. The logic 0 on the $\overline{\text{INC SC}}$ line also drives the Sector and Sector Count registers (I/O section) to increment both registers simultaneously. (The Sector Count register is loaded prior to the start of the operation with the 2's complement of the total number of consecutive sectors to be written or read.) The logic 1 INC SC signal provides an input trigger transition for the Advance Head logic of the Timing section. The one shot of this logic section provides a 4 microsecond cycle, and generates a logic 0 $\overline{\text{CLEAR C}}$ pulse, which provides a common clear for both the Bit and Word Counters (of the I/O section) in preparation for writing or reading the next sector. The one shot also generates a logic 1 CLEAR C pulse, which in the WRITE mode enables gating logic, and thereby resets the DP DCH REQ and the DP Flag flip-flops. Thus, upon reaching the end of the current sector the Data Channel transfer request control logic is cleared in preparation for writing. Though digressive, the CLEAR P signal (generated by the 4 microsecond one shot) will be discussed briefly here. CLEAR P is produced by a differentiating network driven by the $\overline{\text{CLEAR C}}$ terminal of the one shot. CLEAR P is used to pulse the set output gate associated with the Stop flip-flop, and if Stop is set generate a $\overline{\text{DONE}}$ pulse for OR gate driving the $\overline{\text{XFER DONE}}$ line to the Adapter. Thus, if Stop becomes set (either normally by the Sector Count register overflowing during a Read/Write operation, or abnormally by $\overline{\text{DATA LATE}}$ (1)) at the end of the current sector the differentiated CLEAR P signal will be able to pulse the DONE line. $\overline{\text{XFER DONE}}$ sets the Stop flip-flop in the Adapter logic. To return to the discussion of the INC HEAD gates the logic 1 INC SC signal produced by these gates is also transmitted to the Write logic section of the Adapter logic interface, where it is used to enable an OR gate which provides a direct-reset for the Data EN flip-flop. Thus, DATA STROBE and BIT COUNT pulses will be inhibited until the preamble of the next sector is written. At that time the Data EN flip-flop will be set and lift the inhibit from the DATA STROBE and BIT COUNT interface gates, so that the first SHIFT DONE after the Preamble will set the DP Flag (assuming the Busy flip-flop is still set) and initiate another Data Channel request (via the DP DCH REQ flip-flop).

When all sectors on one particular track have been written either the next head (within the same cylinder) must be selected or the current write operation must be terminated in order to Seek a new cylinder (or track) location. The Controller is designed to operate with Disk Drive units with either

6 sector or 12 sector recording media. Disk Cartridge systems are exclusively 12 sector devices, whereas Disk Pack systems may be either, i.e., Data General Disk Drive type 4057A is a 12 sector device, whereas Data General Disk Drive type 4048A is a 6 sector device. The INC HEAD gates shown in the Timing section have three input signal requirements to generate a logic 0 $\overline{\text{INC HEAD}}$ signal. One of the inputs S4 represents the third most significant bit of the Sector (Binary) register, and represents a binary count of four. The second input is jumper selected between the S2 or S8 inputs also from the Sector register. Jumper W7 is inserted to connect S2 for a 6 sector disk (binary 4 plus binary 2=count of 6). Jumper W8 is inserted to connect S8 for a 12 sector disk (binary 4 plus binary 8=count of 12). When the appropriate count is present, along with a logic 0 $\overline{\text{ADV HD}}$ signal (from the Advance Head logic) will produce an INC HD (and $\overline{\text{INC HEAD}}$ through inverter) signal. The logic 0 $\overline{\text{INC HEAD}}$ signal is used within the Controller to perform two functions; increments the Head register in the I/O section and triggers the "Reset Sector" one shot in the Timing section. The $\overline{\text{RESET S}}$ (1) pulse from this one shot clears out the Sector register in the I/O section. The logic 1 INC HD signal is transmitted to the Adapter where it implements the head control logic. The Adapter head control logic is discussed in paragraph 4-3.2.

The transfer operation is ended when SC8, the most significant bit of the Sector Count register, completes a 1 to 0 transition indicating the register has overflowed. Therefore, the (2's complement of the) specified number of sectors have been written (or read). This 1 to 0 transition causes an inverter clocking the Stop flip-flop to produce a 0 to 1 transition, which sets the Stop flip-flop. (The D input of the Stop flip-flop is held to a logic 1 throughout the Read or Write operation by the RD·WR output from an OR gate that is enabled by either a $\overline{\text{WRITE}}$ or $\overline{\text{READ}}$ command mode decode signal.) The differentiated CLEAR P signal derived from the 4 microsecond one shot in the Advance Head logic pulses the gate conditioned by the set output from the Stop flip-flop, and generates a $\overline{\text{DONE}}$ pulse $\overline{\text{DONE}}$ enables an OR gate which in turn places a logic 0 on the $\overline{\text{XFER DONE}}$ line to the Adapter logic. $\overline{\text{XFER DONE}}$, in conjunction with a $\overline{\text{RD/WR}}$(1) signal to indicate a read or write operation is present, sets the Stop flip-flop in the Adapter logic. The Adapter Stop flip-flop performs several functions; the logic 0 (reset terminal) output is ANDed with the next cycle of the "Sector Pulse" one shot to generate trigger the 70 microsecond one shot, enables the D input of the Adapt Done flip-flop with a logic 1 STOP (1) signal (from its set terminal). After the 70 microsecond one shot finishes its cycle it triggers the Read Delay one shot, and the trailing edge of the Read Delay cycle clocks the Adapt Done flip-flop (via the RD DLY(0) line) to the set state. The Adapt Done flip-flop issues CLEAR signals within the Adapter which reinitializes the Adapter logic sections. The Adapt Done flip-flop will also place a logic 1 on the ADAPT DONE (1) line to the Timing section of the Controller. ADAPT DONE(1) enables a gate (since the ADAPTER SEL signal is also present at this gate throughout the execution of the specified operation) to generate a 0 to 1 transition for the clock input of the DP Done flip-flop of the I/O section (via the RD/WR DONE line). Since the logic 1 set output from the Busy flip-flop has been held on the D input of the Done flip-flop, this transition on the RD/WR DONE line will set the Done flip-flop. When Done sets it produces a logic 1 signal which automatically clocks Busy to the reset state. These last two operations conclude the transfer operation.

The Format function mentioned previously will be described briefly here as a basic prerequisite to condition a new Disk Pack recording media for operation in the system. The Format function is applicable only to Disk Pack Drive units and is selected by placing a 1 in bit 2 of the accumulator specified by the DATOC I/O instruction. This bit (DATA2) is subsequently stored into one stage of a register which also holds the Unit Code data (D0 and D1). The output signal from this stage, FORMAT, is a logic 1 when the stage has been set and implements an expanded AND gate to monitor the Word Counter outputs. Two jumpers, W9 and W10, are associated with one of the inputs to the expanded AND gate for selecting the formatting word density for either a high density or low density disk. These jumpers are installed at the factory and W9 is installed for a high density disk and W10 installed for a low density disk. The binary count ANDed with W9 in position is as follows:

W10= 1024 + 512 + 256 $\pm$ 64 (depending on Read or Write) = approx. 1700 words

W 9 = 1024 + 512 + 2048 $\pm$ 64 (depending on Read or Write) = approx. 3600 words

It should be noted here that the entire Format operation is performed under the control and execution of a Processor program written specifically by Data General for this task.

4-2.2 Read Operations

Most of the logical operations described in the previous paragraph are applicable to READ command operations. In fact the same sequence of example I/O instructions discussed in the previous paragraph may be assumed again for this discussion with the exception that the command mode bits 6 and 7 of the accumulator (selected by the DATOA instruction) will be set to a 00 configuration for a READ command function. The loading of the Core Address register and Start I/O bus functions may be assumed to occur exactly as described earlier. The READ logic 0 command signal will be decoded in both the Controller and the Adapter logic (instead of the $\overline{\text{WRITE}}$ signal) and enable all of those associated read logic functions. All of the functions relating to setting the Start flip-flop and generation of the START ADAPTER and CONTROL1 signals are the same, except for the DP Flag flip-flop and the RD/WR flip-flop in the Adapter logic. During a READ operation both the DP Flag and DP DCH REQ flip-flops remain reset until 32 bits of data have been read from the disk. Thus, START ADAPTER will not be able to set the DP Flag flip-flop during a READ operation. The RD/WR flip-flop in the Adapter logic is set during a READ operation by the combination of the READ and CONTROL1 signals.

The sector address search-compare operations in the Adapter logic are the same as described for the WRITE operation. When SECTOR EQUAL does occur it triggers a 70 microsecond one shot which in turn enables the Read logic section of the Adapter logic to set the Read Gate flip-flop, placing a logic 0 enabling signal on the $\overline{\text{READ GATE}}$ line to the Disk Drive unit. Enabling this line allows the electronics of the Disk Drive to start sending $\overline{\text{READ DATA}}$ and $\overline{\text{READ CLOCK}}$ signals back to the Adapter logic. $\overline{\text{READ CLOCK}}$ signals back

to the Adapter logic. READ CLOCK signals set up the Read logic section of the Adapter so that upon detection of the logic 1 sync bit (written on the disk at the end of the Preamble) it places a logic 1 on the XFER SEC (1) line to Data Strobe-Bit Count sections of Adapter logic. Each input READ CLOCK signal generates a RD CLK which in turn triggers a one shot chain (in the Read logic section of the Adapter) which produces (after a 200 nanosecond delay) a STROBE(1) signal. XFER SEC(1) is gated with RD CLK to ultimately produce a BIT COUNT signal for the Control. XFER SEC(1) is also gated with STROBE(1) to ultimately produce a DATA STROBE signal for the Control, and as mentioned previously DATA STROBE produces CLK SHIFT for the 32 bit shift register (Registers section). Hence, once the Read logic section of the Adapter issues XFER SEC(1) the Controller will begin to receive BIT COUNT and DATA STROBE signals. The information line from the Read logic section carrying disk read data is identified as the READ DATA line and after crossing the interface is terminated at the (least significant stage) input of the 32 bit shift register. Thus, the effect of all three signals from the Adapter logic, load the LSB of the shift register, step the Bit Counter, and shift the Shift register.

When the Bit Counter reaches a count of 32, the Bit Shift Monitor gates will produce a SHIFT DONE logic 1 signal, which (since the DP Busy flip-flop is set, i.e., DP BUSY(1) = logic 1) will set the DP Flag flip-flop. SHIFT DONE also (with READ present as a logic 1) triggers the "Read Done" one shot (in the Timing section of the Controller) the output of which enables a pair of parallel OR gates to produce the (logic 0) CLK DSA and CLK DSB signals. Referencing the Registers section of Figure 4-1 in the READ mode, the parallel outputs of the 32 bit shift storage register are fed back around to the inputs of the 2 channel 32 bit Multiplexer, which (with a logic 0 on the READ line controlling the Multiplexer switch selection) will apply the shift storage output data to the inputs of the 32 bit Data Storage register. This data is actually loaded into all 32 bits of the Data Storage register (after 32 bits have been stored in the shift register) by CLK DSA and CLK DSB.

It was mentioned above that the logic 1 SHIFT DONE signal also set the DP Flag flip-flop. From the set state the DP Flag flip-flop will place a logic 1 on the D input of the DP DCH REQ flip-flop (via the DP FLAG(1) line), so that the next RQ ENB I/O bus signal to occur will enable an inverter, the output of which will clock the DP DCH REQ flip-flop to the set state. Setting the DP DCH REQ flip-flop produces an output logic 0 DCHR bus signal to the Processor, and enables (if the DCHP IN priority is present) the D input of the DP DCH SEL flip-flop. The line enabling the D input of the DP DCH SEL flip-flop also provides one of the inputs for the CLR FLAG gate. Thus, the next DCHA I/O bus signal to arrive will produce DP DCHA which will clock the DP DCH SEL flip-flop to the set state. As described in paragraph 4-2.1, setting the DP DCH SEL flip-flop enables three functional Data Channel gates within the Controller. One of these gates controls the DCHM0 I/O bus line and under the conditions of a READ operation will place a logic 0 on this line to the Processor. This logic signal indicates that the transfer is from the Controller to the Processor. The DP DCHA also enables the CLR FLAG which in turn generates the EN CA and EN signals. EN CA and EN, as described in paragraph 4-2.1, gate the contents of the Core Address register out to the I/O Data bus lines. CLR FLAG also will clock REQ 1 to the set state (assuming both REQ 1 and 2nd REQ are in the reset state at the start of the READ operation). The Processor after receiving the Core Address data and the logic 0 on the DCHM0 line will place (since DCHM0 defines the transfer as from device to Processor) a logic 1 on the DCHI I/O bus line. DCHI produces, in turn both a DP DCHI logic 1 signal and a DP DCHI logic 0 SIGNAL. DP DCHI as a logic 0 enables an OR gate to produce a logic 0 INC CA signal used to increment the Core Address register. DP DCHI also (through an OR gate) removes the operational inhibit from the 16 open collector gates driving the I/O Data lines DATA0 thru DATA15. The logic 1 DP DCHI and the fact the 2nd REQ flip-flop is in the reset state (2nd REQ (0) = logic 1) allows the Multiplexer Select Control gates (in the Registers section of the Control) to encode the S0, S1 Multiplexer select lines such that the DS0 thru DS15 outputs from the Data Storage register are placed on the inputs to the 16 open collector (bus driver) gates. (It was mentioned above that the Data Storage register was loaded previously with data from the Shift Storage register by the CLK DSA and CLK DSB signals derived from the SHIFT DONE signal.) The relative signal configurations on the DP DCHI and 2nd REQ lines which allow the Multiplexer to select either the DS0-DS15 outputs or the DS16-DS32 outputs for final transmission back to the Processor (via the DATA0 thru DATA15 lines are listed in Table 4-1.

Since, as described in paragraph 4-2.1, two 16 bit computer words define one Data Channel transfer operation, the DP DCH REQ flip-flop will remain set, holding the DCHR signal on the bus to the Processor. The next DCHA will produce another CLR FLAG which will reset the REQ1 and DP Flag flip-flops, and sets the 2nd REQ flip-flop. As listed in Table 4-1 the set state of 2nd REQ (2nd REQ(0) = logic 0) will gate out the data on the DS16-DS32 lines to the I/O Data bus upon receipt of the Processor DCHI signal. Clearing the DP Flag flip-flop will reset the DP DCH REQ flip-flop when the next RQENB signal is received, removing the logic 0 signal from the DCHR bus lines. (The next subsequent Bus DCHA will clear the Controller DP DCH SEL flip-flop as mentioned in paragraph 4-2.1.)

The data reading, shifting and Data Channel transfer continue in this manner, with the Sector and Head register incrementing performed exactly as described in paragraph 4-2.1. The READ operation is normally terminated in the same manner described in paragraph 4-2.1, i.e., the Sector Count register overflow sets the DP Stop, which in turn sets the Stop flip-flop in the Adapter, subsequently producing an ADAPT DONE signal. The ADAPT DONE signal is transmitted from the Adapter to the Controller to generate a RD/WR DONE, which sets the DP Done flip-flop of the Controller.

4-3 4047 & 4049 ADAPTER UNIT FUNCTIONAL DESCRIPTION

As mentioned previously, descriptions pertaining to the 4047 Adapter are also applicable to the 4049 Adapter, except where noted differently. Therefore all reference and functional descriptions under this paragraph are applicable to both the 4047 and 4049 Adapters, and each reference below to the "4047 Adapter" includes the 4049 Adapter. The Adapter logic is made up of a collage of interface and control logic elements, and since the Adapter is functionally located between the 4046 Controller and the Disk Drive, signals from both equipments

are routed through the Adapter. (Reference drawings 001-000142 and 001-000143) of the print set. The Adapter consists of three major functional sections; the 4047 Plug Interface (and Back Panel printed circuit assembly), the Power Supply section, and the 4047 Logic Interface. A line drawing showing the components mounted on the 4047 Adapter Plug Interface and Back Panel Assembly appears in Figure 4-2.

4-3.1 4047 Plug Interface and Back Panel

(Reference drawing 001-000142 while reviewing this discussion.) Three plugs are mounted on the back panel of the 4047 Adapter, two of which are formed of fixed pins bonded to the printed circuit etch of the panel. These two connectors are designated A and B respectively and terminate signal cables from one or two computers. The cable to each computer connects to a connector mounted in the rear of the computer which has been wired to the slot of the multiple printed circuit connector (within the computer) designated for the location of the 4046 Controller assembly. It is suggested that in single computer configurations the computer cable be connected to the B computer plug which is etch marked on the back panel as P2. (Computer connector A is etch marked on the back panel as P3.) The signals from the A and B computer plugs are multiplexed (U3 through U5, U8, U9, and U11) from connectors P2 and P3.

The multiplexer IC packages along with the Controller assembly selector logic IC's are mounted on the 4047 Plug Interface PCB. The signals from the A (P3) and B (P2) computer plugs are multiplexed by U3 through U5, U8, U9, and U11, the outputs of which are etch wired up to connector J4. Connector J4 is a 100 pin edge type connector for printed circuit boards and is wired to receive the Adapter logic board. Signals transferred between the Adapter logic board and the Disk Drive are routed via the wiring from connector J4 to connector P1. The top section of connector P1 as shown on drawing 001-000142, sheet 1, accommodates signals from the Disk Drive (ATTEN1, $\overline{\text{WR PROT IND}}$, etc.) whereas the bottom section of connector P1 accommodates signals to the Disk Drive.

The 4047 Adapter is capable of being operated by either of two Moving Head Disk Controller assemblies and contains logic used to alternately select either Control for operation. A pair of flip-flops SEL A and SEL B, and a ring-around (Johnson type) counter are used to implement the selection mechanism. The counter is driven by the Adapter logic clock at a 5.75 MHz rate and provides a progressive sequence of four pulses. (See the A or B Control logic section on Figure 4-1.) The leading edge of the second pulse of any sequence is used to clock the SEL A flip-flop, whereas the leading edge of the fourth pulse of any sequence clocks the SEL B flip-flop. A $\overline{\text{START A}}$ signal must be present at the D input of the SEL A flip-flop before it can become set by the edge of the second counter pulse. Likewise a $\overline{\text{START B}}$ signal must be present at the D input of the SEL B flip-flop before it can become set by the edge of the fourth counter pulse. The $\overline{\text{START A}}$ and $\overline{\text{START B}}$ signals originate in their respective Control Assemblies simply as $\overline{\text{START}}$ signals and are polarized as $\overline{\text{START A}}$ or $\overline{\text{START B}}$ by their connection to the A or B computer plug mounted in the rear of the Adapter.

Each $\overline{\text{START}}$ signal is produced in its respective Control assembly whenever the Start flip-flop (Timing Section) becomes set by a DP START pulse (for a Read/Write operation) or by a DP IOP pulse (for a Seek operation). The ring-around counter working in conjunction with the two flip-flops (SEL A and SEL B) guarantees that only one flip-flop will become set at any one time. Setting either flip-flop causes gating logic to place a logic 0 on the FREE line. One of the functions of this line is to enable or disable the clock signal input gate to the counter, and in the 0 state it disables the clock input gate. Therefore as soon as either SEL flip-flop is set, the counter is stopped by disabling the clock signal input gate.

The 1 to 0 transition of the FREE line also triggers a 6 second one shot which after it times out, triggers a 1.6 microsecond one shot which drives a gate to generate a logic 0 $\overline{\text{CLRSEL}}$ signal. This signal clears both the SEL A and SEL B one shot simultaneously. This function prevents the adapter from becoming hung up if the selected Control assembly experiences some sort of operational malfunction.

An ADAPT DONE (1) signal from Adapt Done flip-flop of the Adapter logic is normally produced when the Read/Write transfer is completed (and the Stop flip-flop is set). ADAPT DONE (1) enables an OR gate which in turn drives the direct reset input of the 6 second one shot, immediately clearing the one shot. Resetting the 6 second one shot triggers the 1.6 microsecond one shot, which clears the SEL A and SEL B flip-flops and raises the FREE line, thereby allowing the counter to resume operation. The Adapt Done flip-flop can be set immediately by a $\overline{\text{HALT}}$ signal resulting from detection of an EOC, AD + UNSF, CKWD error condition or during a PWR CLR. The same PWR CLR signal also enables the OR gate producing $\overline{\text{CLR SEL}}$ which resets both the SEL A and SEL B flip-flops.

It is pointed out here that a SEEK operation causes the Start flip-flop to be set by a $\overline{\text{DP IOP}}$ pulse. (See the Timing Control section of Figure 4-1.) This in turn will select the Control originating the START (as directed by the state of the ring-counter. The end of the SEEK does not deselect the selected Control. The Control will remain selected for subsequent SEEK operations until either a $\overline{\text{XFER DONE}}$ of a $\overline{\text{RD/WR}}$ (Read/Write) operation is completed and an ADAPT DONE (1) is generated, or the 6 second one shot times out. Either event will clear the Selected flip-flop (SEL A or SEL B) and FREE the counter, thereby implementing the mechanism for selecting the alternate Control. If the alternate Control has no $\overline{\text{START}}$ signal present, it will not be selected and the counter will remain FREE to be driven by clock pulses, thereby allowing the originally selected Control to be reselected again later on in the course of the counter sequence (if it is Started).

4-3.2 4047 Logic Interface

(Reference drawing 001-000143 while reviewing this discussion.) Assuming most transfer operations are initially begun with a SEEK command, the $\overline{\text{SEEK}}$ command signal is decoded from the states of the CM1 and CM2 command lines and enables control logic within the interface. The command lines CM1 and CM2 are also decoded within the Control assembly, and enables the $\overline{\text{CYL}}$, $\overline{\text{HD + DIR}}$, $\overline{\text{DIFF}}$, and $\overline{\text{CONTROL2}}$ signals to be generated. The logic 0 CYL signal is transmitted from the Control to the CY1 Setup one shot of the 4047 Logic Interface, where it functions as a low level trigger for the one shot. The trailing edge of this one shot in

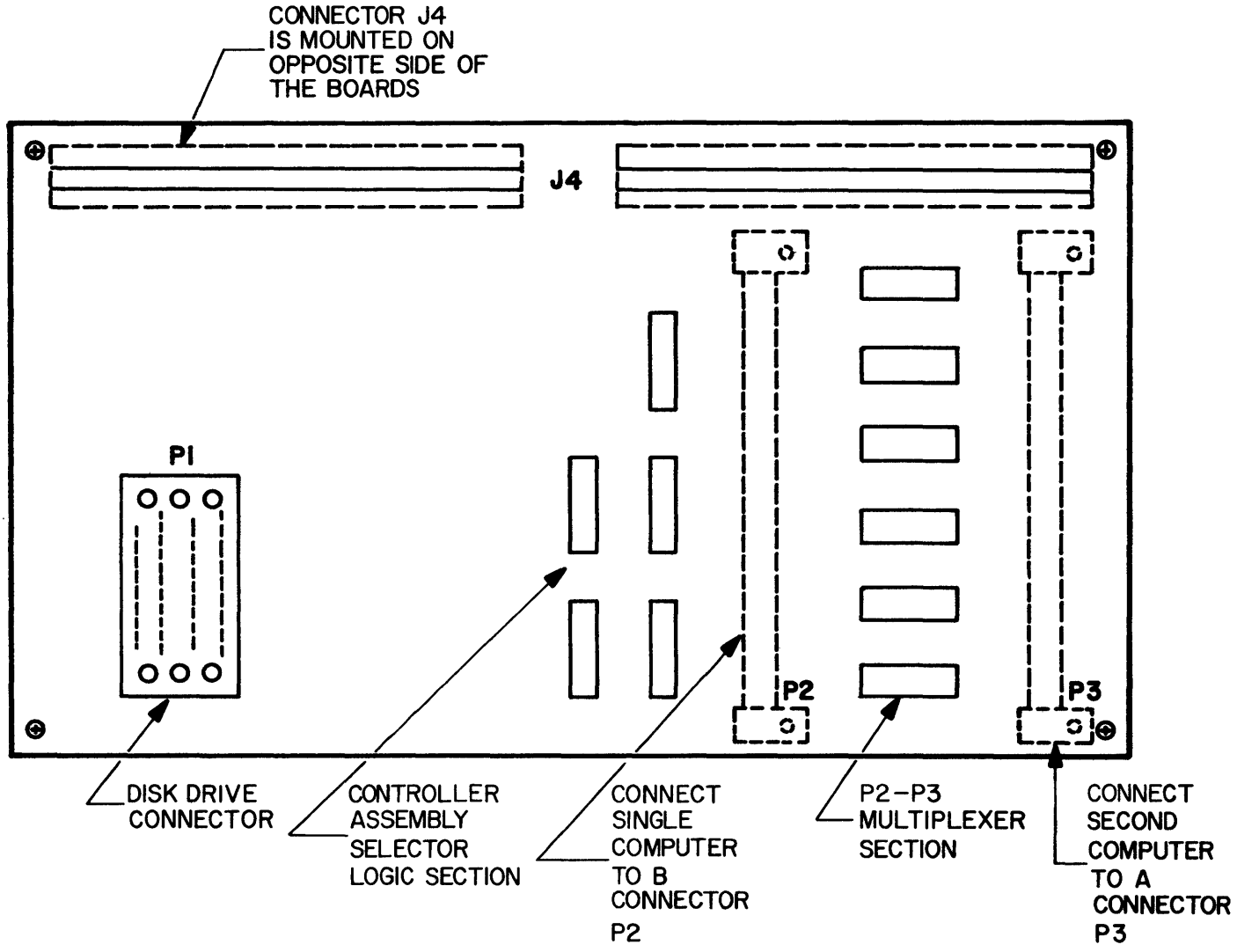


Figure 4-2. 4047 Adapter Plug Interface and Back Panel

turn triggers the TAG one shot. The trailing edge of the TAG one shot, in turn sets the Track Address Strobe (TAS) flip-flop. The reset output from the TAG one shot enables (during its cycle) the track address data present on BUS lines 0 through 7 to be gated into the Track Address register. (See the Unit and Track Address-Sector Equal and Command logic of Figure 4-1.)

It will be noted that if this was a RECAL (Recalibrate is a command to position the heads over track Address 000) operation, the decoded RECAL signal is also gated into the Track Address register as a RESTORE bit. Setting this bit causes the Disk Drive logic to ignore the rest of the data in the Track Address register and zero position the heads.

To return to the discussion of the SEEK operation, signal $\overline{\text{TAG}}$ (1) loads the Track Address register from the BUS lines. After the TAG one shot times out, the TAS flip-flop becomes set and enables an inverter to send a logic 0 $\overline{\text{TRACK ADD STROBE}}$ to the Disk Drive. This signal informs the Disk Drive logic that the track address signals are present and settled on the eight TA lines ($\overline{\text{TA1}}$, $\overline{\text{TA2}}$, $\overline{\text{TA4}}$, $\overline{\text{TA8}}$, $\overline{\text{TA16}}$, $\overline{\text{TA32}}$, $\overline{\text{TA64}}$, $\overline{\text{TA128}}$). The Disk Drive logic requires that Track Address data be present on the TA lines for quite a long period while it performs the differential addressing calculations. When the Disk Drive logic finishes its calculations it responds by transmitting a logic 0 $\overline{\text{ADD ACK}}$ signal back to the Adapter interface logic. $\overline{\text{ADD ACK}}$ enables an OR gating configuration, which in turn directly resets the TAS flip-flop. A pair of series one shots are provided to make sure the TAS flip-flop is reset after a nominal (set) interval. The first one shot is 80 microseconds in duration and is triggered by the set transition of the TAS flip-flop. The trailing edge of the first one shot triggers the second one shot which in turn produces a logic 1 CLR TAS (1) signal to reset the TAS flip-flop.

The seek operation is completed by a signal on the ATTEN line from the selected Disk Drive unit. (The unit is selected by the code appearing on the D1 and D0 lines, which is decoded in the logic interface to select one of four possible Units.) The ATTEN lines from the four drive units are labeled ATTEN1 through ATTEN 4 as transmitted from the drive units and pass through the Adapter (via connectors P1, P2, and P3). However, these lines terminate in the Timing Section of the Control assembly as ATTEN0 through ATTEN3, with the ATTEN1 line relabeled as ATTEN0, ATTEN2 relabeled as ATTEN1, ATTEN3 relabeled as ATTEN2, and ATTEN4 relabeled as ATTEN3. This minor change in signal wire nomenclature was required to expand the versatility of the 4046 Control Assembly in terms of operating with other Adapters and Disk Drive units. The appropriate ATTEN signal sets its associated SEEK DONE flip-flop in the Control assembly, which in turn will produce a computer interrupt (providing interrupts are not disabled).

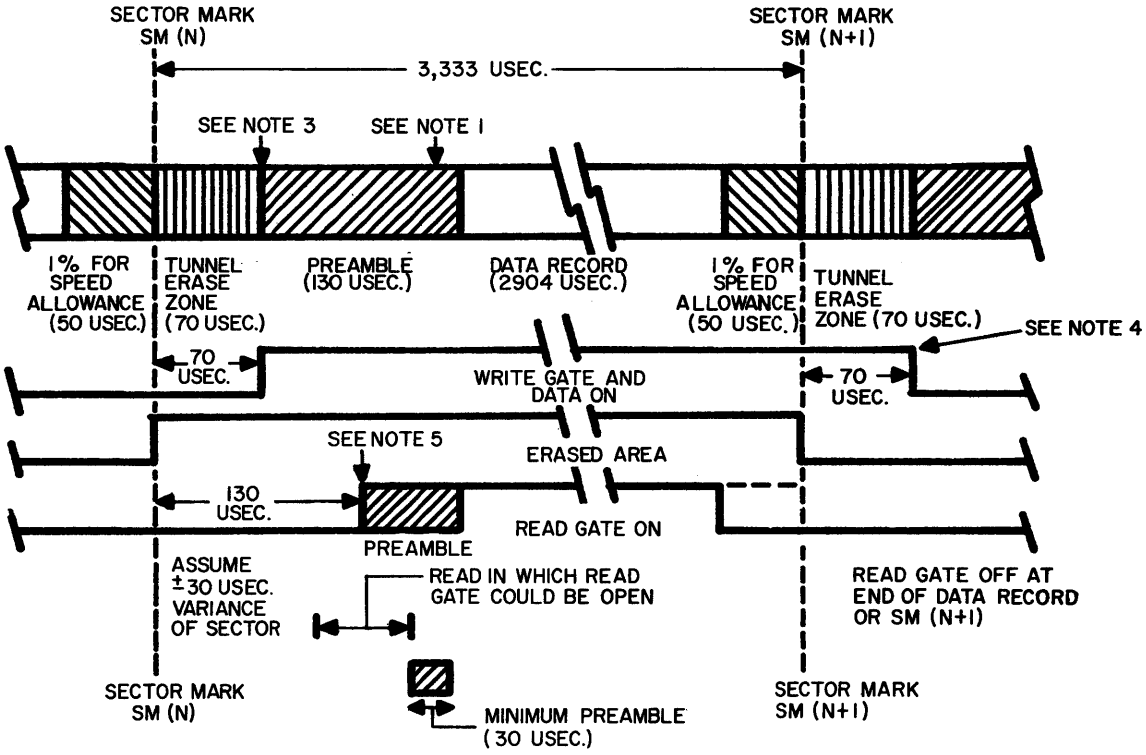
The timing for Read/Write operations is shown on Figure 4-3. Operations (read or write) start in the 4047 logic upon receipt of the $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ (CM1 and CM2 codes) and $\overline{\text{CONTROL1}}$ signals from the Control Assembly. To order the discussion, a description of the 4047 logic during a Write operation will be presented first, and be followed by a description of a Read operation.

The presence of the $\overline{\text{WRITE}}$ and $\overline{\text{CONTROL1}}$ signals will set the RD/WR flip-flop. The outputs of this flip-flop are used throughout the 4047 logic as primary control signals. Setting RD/WR removes the direct reset being held on the Sec Equal flip-flop by an OR gate. This allows sector sensing to become operational. (It is assumed that the heads were positioned over the addressed track during the seek operation. The Sector address signals from the Control assembly are exclusive OR'ed with the $\overline{\text{SA}}$ (Sector Address) signals from the Disk Drive. A $\overline{\text{SECTOR PULSE}}$ is transmitted from the Disk Drive as a signal that the next sector is about to pass under the selected head. This $\overline{\text{SECTOR PULSE}}$ triggers a one shot, the trailing edge of which sets the Sec Equal flip-flop (if the specified sector address is equal to the actual sector address). When the Sec Equal flip-flop becomes Set it generates a 0 to 1 transition which triggers a 70 microsecond delay one shot. (Setting the Sec Equal flip-flop also causes its reset terminal to place a logic 0 on the $\overline{\text{SEC EQUAL}}$ (1) line, which clears the Checkword register and the checkword bit counter in preparation for the transfer of sector data.) The trailing edge of the 70 microsecond one shot triggers the 60 microsecond Read Delay one shot. Read Delay is triggered for both Write or Read operations, and is basically part of the Sector Equal timing chain. Read Delay provides control signals used in other sections of the 4047 logic.

The trailing edge of the 70 microsecond one shot also triggers the Write Enable (WREN) flip-flop with a logic 0 signal present at the inverter controlling the D input of the WREN flip-flop. (See the Write Logic section of Figure 4-1.) The logic 0 output from the reset terminal of the WREN flip-flop turns on and AND gate being driven by the 5.75 MHz Adapter clock signal ($\overline{\text{5.75 MHz}}$). The output from this gate drives a two stage ring-around counter which provides a sequence of 10, 11, 01, and 00. The 01 state of the counter enables a gate to produce a STATE III signal, whereas the 10 state of the counter enables a pair of gates to produce a STATE I signal. This form of switching (STATE I, STATE III) is used in Write timing because of the low noise properties inherent in this type of counter. The $\overline{\text{STATE I}}$ signal essentially writes the Clock pulse on the disk track. The $\overline{\text{STATE III}}$ signal writes the Data on the Disk track. Since STATE I and STATE III are each separated by two other counter states (namely 11 and 00) normal operation will write a Clock, then write the Data, write the Clock, write the Data etc.

Another important function of the WREN flip-flop (in the set state) is to produce a logic 0 $\overline{\text{WRITE GATE}}$ signal for the Disk Drive unit. This signal turns on the WRITE (GATE) current amplifiers in the Disk drive unit electronics. This signal in conjunction with the $\overline{\text{WRITE DATA \& CLOCK}}$ line performs the actual data recording.

At this point in the discussion, the WREN flip-flop is set, the STATE I - STATE III ring-around counter is operating, and the $\overline{\text{WRITE GATE}}$ signal is present. Referencing the timing diagram, the next stop in the Write operation is to write the Sector Preamble, the writing of which lasts for 130 microseconds, and consists of a continuous string of zeroes concluded by a single 1 bit. This function is performed by a 130 microsecond delay one shot, followed by two flip-flops connected in series. The 130 microsecond one shot is triggered by the output from an AND gate, which is enabled by logic 1 READ DLY (1), STOP (0), and WRITE signals. This functionally indicates the Read Delay one shot is cycling, the Stop flip-flop has not been set, (thus, the selected sector is present),



NOTES 1. Preamble consist of all zeroes concluded by a single one.
2. Write and erase gate turned on together - 70 microseconds after SM (N).
3. Start writing preamble concurrent with write and erase gate.
4. Continue writing zeroes until 70 microseconds after SM (N+1); then turn-off write and erase gates.
5. Read gate open 130 microseconds after SM (N).

CAUTION

After a head select or the termination of a write operation, allow 100 microseconds for read amplifier recovery; this maybe wholly or partly over-lapped with other delays.

Figure 4-3. Data Format

and a WRITE operation has been commanded. During the cycling period of the 130 microsecond one shot, the Data Enable flip-flop (in the initialized reset state) inhibits the gating path for the Computer data (COMP DATA) signals from the connector (pin B70) to the WRITE DATA & CLOCK output. Therefore, for 130 microseconds zeroes will be written at STATE III time (with Clocks still being written at STATE I time).

The trailing edge of the 130 microsecond delay one shot sets an "End of Preamble" latch flip-flop. (This flip-flop's D input is enabled by a logic 1 WRITE signal.) The logic 1 set output from this flip-flop in turn set enables the D input of the Sync Bit flip-flop, which will then set on the next STATE I signal generated. The function of the "End of Preamble" latch flip-flop (positioned between the 130 microsecond one shot and the Sync Bit flip-flop) is to hold a logic 1 on the D input of the Sync Bit flip-flop until STATE I occurs. When Sync Bit sets, it enables an OR gate which automatically resets the "End of Preamble" latch flip-flop. The logic 0 from the reset terminal of the Sync Bit flip-flop enables the WRITE DATA (OR) gate (a logic 1 WRITE DATA signal) is AND'ed with a logic 1 STATE III signal. Both signals present will enable the NAND gate, which in turn will drive the output from the WRITE DATA & CLOCK (OR) gate to a logic 0, writing the 1 on the End of the Preamble.

As mentioned above the "End of Preamble" latch flip-flop is cleared when the Sync Bit flip-flop became set. This causes a logic 0 to be placed on the D input of the Sync Bit flip-flop, hence on the next CLOCK I (which naturally follows in the Counter sequence two counts after the CLOCK III count which write Sync Bit onto the Disk) the Sync Bit flip-flop will be reset. The reset terminal of the Sync Bit flip-flop then provides a 0 to 1 transition which sets the Data Enable flip-flop (with the D input of the flip-flop set enabled by a logic 1 WRITE signal present). At this time Data Enable provides a logic 0 from its reset terminal which functions as one of the enable inputs for the COMP DATA gate. The other logic 0 enable input is provided by signals on the DATA (COMP DATA in the Adapter logic) line from the Control Assembly. The output from this gate is a logic 0 when the gate is in the enabled state, and drives the output of the WRITE DATA (OR) gate to a logic 1. This signal, as mentioned previously, is gated with a logic 1 STATE III signal to produce a logic 0 WRITE DATA & CLOCK signal (to the Disk unit electronics) to write a 1 on the Disk. Therefore at this time, and for subsequent STATE III signals, the state of the WRITE DATA & CLOCK line is under the control of the COMP DATA input line. Needless to say, the other OR function for the WRITE DATA & CLOCK gate, the STATE I function will continue to write Clock pulses (at STATE I time). A summary of the events from setting the Sync Bit flip-flop is as follows;

a) STATE III writes single 1 bit on End of Preamble.
b) STATE I clears Sync Bit flip-flop and writes Clock.
c) STATE III writes Data.
d) STATE I writes Clock.
e) STATE III writes Data.
f) steps d and e continue for remainder of data record.

One additional timing consideration is the generation and function of the DATA STROBE and BIT COUNT signals. Both of these signals are primarily functional within the Control Assembly, where they are used to synchronize the transfer of data between the Control Assembly and the Adapter. DATA STROBE shifts the Shift Register in the Control Assembly, and BIT COUNT increments the Bit Counter in the Control Assembly. These signals are produced initially in the 4047 logic when the Data Enable flip-flop becomes set. STATE I is gated with DATA EN (1) to generate a DATA STROBE signal. STATE III is gated with DATA EN (1) to generate a BIT COUNT signal. (These signals pass thru additional gating which switch the signals to the input lines of either Control Assembly A or B depending on which is selected by the Adapter.) Therefore, STATE I produces a DATA STROBE signal which shifts the next bit of the Control Assembly shift register to the DATA terminal. This is done at STATE I time in preparation for writing the bit at STATE III time. At STATE III time two operations occur, the bit is written on the Disk and the Bit Counter is incremented. During a write operation when the Bit Counter in the Control Assembly reaches a count of 32 it sets a Flag which in turn (if Data Channel Request are enabled) produces a Data Channel Request for the next two (16 bit) words from the computer.

In addition to producing BIT COUNT, STATE III and DATA EN (1) (that is the logic 0 output of their AND gate) enables an OR gate to produce a logic 1 STROBE CC (Strobe Check Character) signal. (See the Checkword-Data Strobe-Bit Count logic of Figure 4-1.) This signal shifts the Check Character generator used to form the checkword by XORing the state of BIT 15 (of the Checkword register with state of the input bit (as indicated by the state of the WRITE DATA LINE) to determine the least significant Checkword bit. The state of Bit 15 is also XORed with the state of Bit 8 to determine the state of the bit to be loaded into Checkword 9. When the Control Assembly finishes writing data in the present sector it transmits an INC SC (Increment Sector Count). This signal is inverted and gated with a logic 0 RD/WR (1) signal from the reset terminal of the RD/WR flip-flop (in the set state). Both signals present enable a gate to produce a direct set for the CC (Check Character) State flip-flop. The logic 1 set output from this flip-flop enables the D input of the CC (Check Character) EN (Enable) flip-flop, which will become set on the next STATE I signal generated. Setting the CC EN flip-flop provides one of the requirements for a gate driven by STATE I. The output of this gate (at STATE I time) provides a logic 0 enable for the STROBE CC (OR) gate. Hence, each STATE I pulse will generate a STROBE CC shift pulse for the Checkword generator as long as the CC EN flip-flop is set. The serial output from the Checkword

register is applied to a gate for ANDing with CC STATE (1) (from the CC State flip-flop) signal and a STATE III signal. The output of this gate drives the CHKCH line to the WRITE DATA (OR) gate. Therefore at STATE III time Bit 15 of the Checkword register will be written on the Disk, and at STATE I time a STROBE CC pulse will be generated to shift the Checkword register. The logic 0 output from the CC EN (1) and STATE I gate also generates a CLK COUNT signal (in addition to the STROBE CC pulse). The CLK COUNT signal drives an OR gate, the output of which drives a binary counter. When the counter reaches a count of 16 (as signified by bit 8 of the counter producing a 1 to 0 transition) it enables an inverter to generate a 0 to 1 transition at the Cinput of the CC State flip-flop. Since the D input of this flip-flop is grounded, this 0 to 1 transition on the C input clears the (CC State) flip-flop. Resetting the CC State flip-flop in turn places a logic 0 on the D input of the CC EN flip-flop, allowing the next STATE I pulse generated to reset the CC EN flip-flop. When the CC State flip-flop becomes reset the set terminal will also place a logic 0 on the CC STATE (1) line to inhibit the CHKCH gate. To summarize the Checkword writing function:

a) The Checkword register is shifted at STATE I time.

b) Each Checkword bit is written on the Disk at STATE III time.

c) Checkword writing is terminated automatically after 16 bits have been written.

The following will review the functions of a Read operation. (See the Read logic section of Figure 4-1). READ and CONTROL1 set the RD/WR flip-flop. The Sector Equal function and the 70 microsecond and 60 microsecond one shots function as previously described for the Write operation. The trailing edge of the Read Delay one shot triggers the Read Gate flip-flop which is set enabled by a logic 1 signal READ signal held on its D input. Setting this flip-flop produces a logic 0 READ GATE signal for the Disk Drive unit electronics READ GATE enables the Read Clock and Read Data outputs within the Disk Drive unit. READ CLOCK is transmitted from the Disk Drive as a logic 0 signal, and after termination in the 4047 logic is inverted to place a logic 1 on the RD CLK line. RD CLK performs several functions, one of which triggers a 200 nanosecond one shot. This one shot performs two functions, the first of which clears out a Read Data latch flip-flop. The second function occurs on the trailing edge of the one shot timing cycle and triggers the Strobe one shot. The Strobe one shot is used to generate a DATA STROBE pulse for the Control Assembly (after the XFER SEC flip-flop becomes set). The same trailing edge triggers a 15 microsecond one shot, which in turn times out and sets the RD SYNC flip-flop. RD SYNC enables a gate driven by RD CLK, the output of which clocks the XFER SEC flip-flop. XFER SEC cannot become set until the first data bit is received (as indicated by a logic 1 READ DATA signal). Since the data is written at a different time than the clock READ CLOCK pulses are used to clock the Read Data flip-flop. As mentioned previously the 200 nanosecond one shot triggered by RD CLK cleared out the Read Data latch. After the one shot has timed out, and upon receipt of a logic 0 READ DATA signal a RD DATA logic 0 signal is generated as a direct set for the Read Data latch. The logic 1 output from this latch enables the D input of the Read Data flip-flop. The next RD CLK clocks the flip-flop and (if the latch was set previously) sets the Read Data flip-flop. The 200 nanosecond one shot is also recycled at this time (by RD CLK) and clears out the Read Data latch. However, the Read Data flip-flop cannot be reset until the next RD CLK. Hence, if between READ CLOCK pulses another READ DATA signal occurs, the Read Data latch will be set again, and the Read Data flip-flop will remain set. Figure 4-4 is a sample timing diagram of the READ DATA, READ CLOCK functions. To summarize: a data bit must occur between two clock pulses, and once occurring requires two subsequent clock pulses to clear from the logic. If another data bit occurs before the second subsequent clock, the clearing of the logic is deffered to the next two subsequent clock pulses. This logic configuration (considering of the READ DATA, READ CLOCK gates, the 200 nanosecond one shot, the Strobe one shot, the Read Data latch, and the Read Data flip-flop) can be quickly checked during any troubleshooting procedures by reading all 1's off of the Disk. An input data train consisting of all 1's will cause the Read Data flip-flop to remain set, hence the output READ DATA line to the Control Assembly will be held to a constant logic 1 level for the duration of the 1's transfer.

The first data bit to be received (in this case the 1 written on the end of the Preamble) allows the XFER SEC flip-flop to be set. Setting this flip-flop clears out the RD SYNC flip-flop and sets up one of the enabling condition for a pair of gates, one of which is driven by RD CLK and the other driven by STROBE (1) (from the Strobe one shot). The gate driven by STROBE (1) generates a DATA STROBE which shifts the Control Assembly 32 Bit Shift register. The gate driven by RD CLK generates a BIT COUNT. Therefore since STROBE occurs after RD CLK (200 nanoseconds later) the read timing is such that a BIT COUNT is given first to increment the Bit Counter in the Controller Assembly, then a DATA STROBE is produced to shift the 32 Bit Shift register. The set terminal of the Read Data flip-flop drives the READ DATA line to the Controller Assembly 32 Bit Shift register input.

The Checkword is formed in the same manner (XOR Bit 15 with the input data bit, XOR Bit 8 with Bit 15) during the Read operation as during the Write Operation. In the case of a Read operation, (enabling) signal READ is gated with the READ DATA signals to drive the Checkword input XOR gate. The Checkword register shift pulse, STROBE CC, is generated (while the Checkword is being formed, i.e. Read Data is in the process of being received) by the output from the

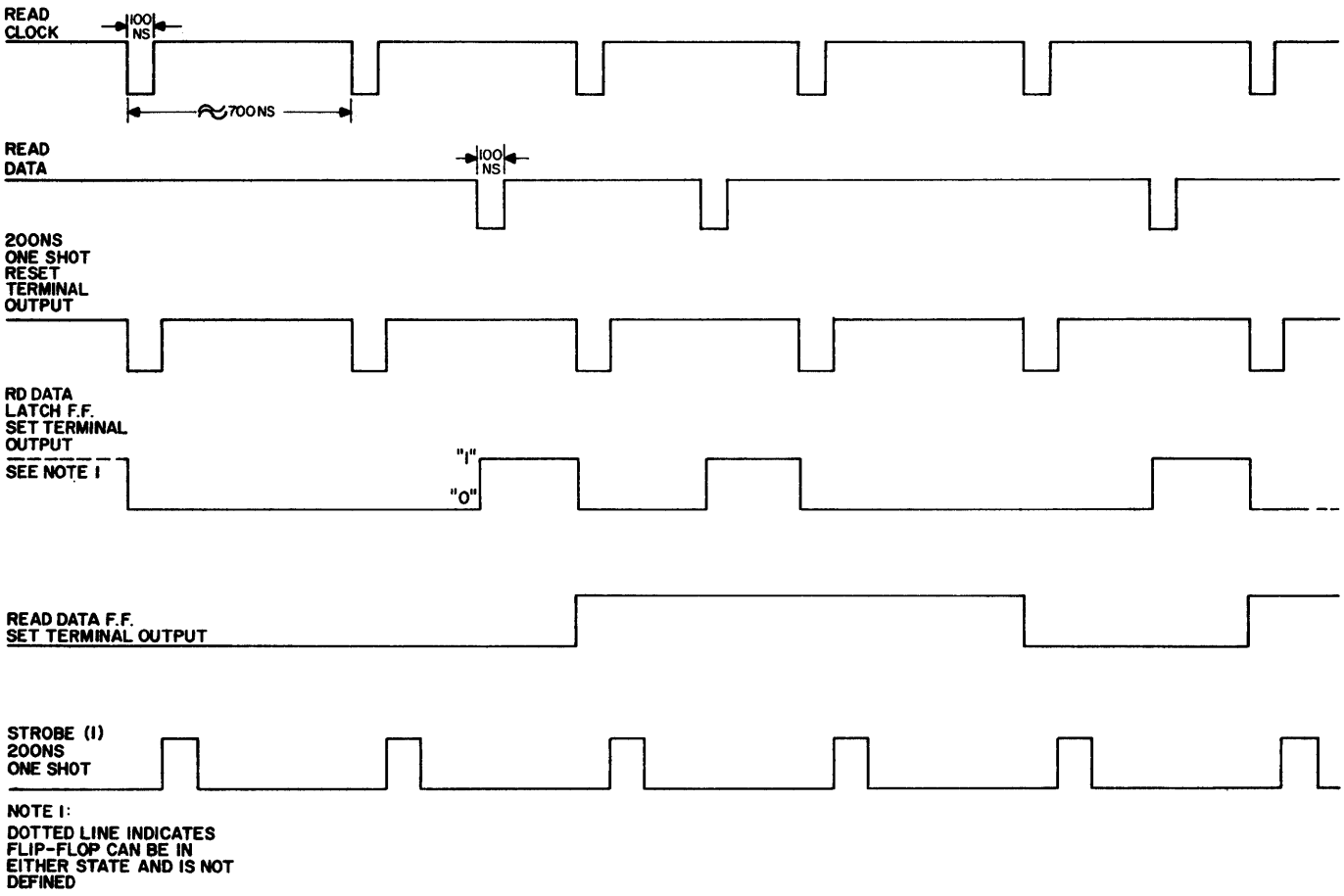


Figure 4-4. Read Data Timing Example for 01101 Input Data Series

same (STROBE (1) and XFER SEC (1)) gate producing the DATA STROBE pulse. Thus, a STROBE CC pulse is generated each time a DATA STROBE pulse is produced. When a complete sector has been Read from the Disk an INC SC is transmitted from the Controller Assembly, and this signal together with the enabling RD/WR (1) signal (from the RD/WR flip-flop) sets up the CC State flip-flop, thereby enabling the CC EN flip-flop to be set by the next STROBE (1) signal from the (RD CLK) Strobe one shot.

At the conclusion of the sector transfer during a Read operation, the Checkword assembled in the Checkword register during the data transfer is compared with the Checkword written on the Disk. Each input Checkword bit from the Disk is compared with the corresponding bit of the Checkword register, and monitored by the CKWD (Error) flip-flop. The logic mechanism for shifting out the Checkword register is derived from a NAND gate which is enabled by the RD CLK, READ, and CC EN (1) signals. The output from this gate, STROBE CLK, performs two functions; drives the STROBE CC (OR) gate and increments the Checkword bit counter. Therefore, each RD CLK (with the CC EN flip-flop set) generates a STROBE CLK to shift the Checkword register and increment the Checkword bit counter. READ DATA signals (from the Read Data flip-flop) are XOR gated with the state of bit 15 of the Checkword register. The output from the XOR gate controls the D input of the CKWD (Error) flip-flop. The clock input of the flip-flop is controlled by selective gating of the following signals: a feedback signal from the set output terminal of the CKWD (Error) flip-flop, CC EN (1) and STROBE (1). These signals require that the CKWD (Error) flip-flop be in the reset state, that the CC EN flip-flop be in the set state, and that the (RD CLK) strobe one shot is cycling. If a difference between the state of the bit in the Checkword register and the state of the corresponding input (READ DATA) bit is detected by the XOR gate the D input of the CKWD flip-flop will be set enabled so that 200 nanoseconds after the next RD CLK, the Strobe one shot will fire and clock the CKWD (Error) flip-flop to the set state. The CKWD (Error) flip-flop remaining in the reset state verifies equality between the Checkword formed during the Read operation and the Checkword formed and written on the Disk during the Write operation. This verification validates the data transfer.

Three flip-flops are included in the 4047 logic for monitoring the Head incrementing and End of Cylinder (EOC) conditions. The Disk Drive unit designed to operate with the 4047 logic interface has two heads, the selection of which is monitored by the Head flip-flop. (See the A or B Control Select-Head Select-Adapter Done logic of Figure 4-1.) When the Head flip-flop is reset one head is selected, when the Head flip-flop is set the other head is selected. The output from the set terminal of the Head flip-flop controls an inverter driving the HD SEL line to the Disk drive electronics. Thus when the Head flip-flop is set, the HD SEL line is at the logic 0 level, selecting the upper head or head 1. When the Head flip-flop is reset, the HD SEL line is at the logic 1 level, selecting the lower head or head 0. An attempt to increment beyond the 1 head will produce an EOC condition, and an error status. The Head flip-flop's D input is controlled by the signals on the BUS7 line from the Controller Assembly, hence head 0 or 1 may be selected directly (with incrementing permitted only from the 0 head selection). The INC HD signal from the Controller Assembly is stored in a flip-flop which in turn will direct set the Head flip-flop, if the Head flip-flop is currently in the reset state, and the Read Delay one shot is cycling. As mentioned previously setting the Head flip-flop switches the level on the output HD SEL line to the Disk Drive unit. Setting the Head flip-flop also places a logic 1 on the D input of the EOC flip-flop. Under these conditions another INC HD signal from the Controller Assembly will set the EOC flip-flop thereby establishing the error condition. EOC, in addition to being transmitted to the Controller Assembly, from the logic 1 state, enables the Halt OR gate to produce a logic 0 HALT signal. This signal provides a direct set for the Adapt Done flip-flop, which immediately informs the Controller Assembly that the Adapter is done (via the ADAPT DONE (1) line). The Halt OR gate can be driven by either of two other possible error conditions, AD + UNSF and CKWD, or by a PWR CLR (Power Clear) signal. Either condition occurring will produce a HALT signal to set the Adapt Done flip-flop.

The Adapt Done flip-flop is normally set at the conclusion of a transfer operation as defined by the Controller Assembly, and indicated by the state of the XFER DONE line. XFER DONE is generated by the Controller Assembly after data from a specified number of sectors has been transferred. XFER DONE and RD/WR (1) both present at the logic 0 level will enable a gate to direct set the Stop flip-flop. The logic 0 from the reset terminal of the Stop flip-flop is gated with the logic 0 from the Sector Pulse one shot, which is cycled on the next sector mark after the Stop flip-flop became set. This synchronizes the end of the transfer operation with the sector mark. Both logic 0 signals present enables a gate to trigger a 70 microsecond one shot. The trailing edge of the 70 microsecond one shot in turn triggers the 60 microsecond Read Delay one shot. Read Delay cycles and produces a 0 to 1 transition of the READ DLY (0) line at the end of its cycle. This trailing edge function performs two operations; clocks the Adapter Done flip-flop to the set state (assuming the Stop flip-flop is set), and clocks the Stop flip-flop to the reset state. Hence, an ADAPT DONE (1) signal is produced, and the Stop flip-flop is cleared in preparation for the next transfer or seek operation.

The Stop flip-flop is also cleared by an a logic 0 ADAPT DONE (1) signal when the Adapter Done flip-flop becomes set. This function is included to make sure the Stop flip-flop is cleared in the event a Checkword error occurs. A Checkword error (or any other error producing a HALT signal) immediately sets the Adapter Done flip-flop. Adapter Done FREE's the Adapter (SEL A and SEL B) select ring-around counter

allowing it to select the alternate Adapter, thereby deselecting the present Disk Drive unit. Underthese conditions the next sector mark used to trigger the 70 microsecond one shot (and subsequently the 60 microsecond and Read Delay one shot) will not be sensed by the Adapter logic, and as a consequence the Stop flip-flop will not be clocked to the reset state (by the trailing of READ DLY0). ADAPT DONE (1) prevents this from occurring during a Checkword error condition by immediately clearing the Stop flip-flop via its direct reset terminal.

Two error indicator signals from the Disk Drive unit electronics are terminated and gate isolated from their logical functions in the 4047 logic and the 4046 Controller Assembly. One error indicator is the SEEK INC, which produces an SEK (Seek error) signals for the 4046 Controller Assembly. This signal is sensed as part of the input status word. The other error indicator is WRITE CHECK which produces an AD + UN SF signal. AD + UNSF is used both in the 4046 Controller Assembly and the 4047 logic. WRITE CHECK at the logical 0 level indicates the presence of certain conditions, within the Disk Drive unit, that are likely to interfer with the recording of valid data on the Disk. Therefore AD + UNSF is used to produce (via the HALT gate) an immediate ADAPT DONE (1) ending the present transfer operation. SEEK INC (Seek Incomplete) on the other hand is not catastrophic but indicates the Seek was not completed. The SEEK INC state is cleared when a (Programmed) RESTORE command is issued.

4-4 4047 DISK POWER SUPPLY FUNCTIONAL DESCRIPTION

The reader should reference drawing 001-000186 bound into the print set when reviewing the descriptions presented in this paragraph. Source power for the power supply may be either standard 117 VAC lines or 220 VAC lines regulated to ±20%, and capable of supplying 230W. The power supply output voltages and maximum currents are listed in Table 4-2 below.

The power supply is composed of five separate, functional parts, +30 VNR @ 15 amp generation, +30 volt @ 4 amp generation, +5 volt regulator, +15 volt regulator, -15 volt regulator and associated circuitry.

Table 4-2. Power Supply Outputs

Voltage	MAX Current	Primary Use	Remarks
+15v(+HV)	8 Amperes	Disk Drive DC Power	short-circuit & over-voltage protected
-15v(-HV)	4 Amperes	Disk Drive	short-circuit protected
+5v	3 Amperes	IC logic	short-circuit & over-voltage protected

The power supply is composed of five separate, functional parts, + 30 VNR @ 15 amp generation, +30 volt @ 4 amp generation, +5 volt regulator, +15 volt regulator, -15 volt regulator and associated circuitry.

4-4.1 +30 VNR @ 15 amps Generation

+30 VNR @ 15 Amps is a filtered non-regulated voltage which is used by the +15 volt and +5 volt regulators. At nominal line voltages, +30 VNR will be between +32 volt and +35.5 volts depending upon the load. The two transformer primaries are wired in parallel for 117 VAC operation, and in series for 220 VAC operation. The fan is always wired in parallel with the BLK-BRN primary, causing it to be effectively wired into an autotransformer during 220 VAC operation.

4-4.2 +5 Volt Regulator

A self-oscillating, switching regulator is used to generate the +5 volt output. (A simplified diagram of the regulator appears in Figure 4-5 below.) The operation of this type of regulator is described briefly in the following discussions. A reference voltage is compared with the output voltage. If the output voltage is less then the reference voltage, a series pass transistor drives an LC filter. When the pass transistor turns on, the output voltage of the filter rises linearly until the output voltage equals the reference voltage. At this point the pass transistor is turned off. The field across the inductor now reverses, allowing the inductor to recover through the commutating diode. The output current is now drawn from the energy stored in the LC filter. When the output voltage falls below the reference voltage, the cycle repeats. The output voltage will be sawtooth waveform, centered around the nominal output voltage.

The +5 volt regulator consists of chip U2 and its associated circuitry. U2 contains circuits which generate a reference voltage, a voltage comparator, and disable circuits used by the short-circuit protection circuits. The reference voltage at pin 6, nominally 7.15 volts, is divided down to 5 volts and applied to one input of the comparator at pin 5. The output voltage is brought directly to the other side at pin 4. When the output voltage is less than 5.2 volts approximately, pin 11 will drop to + 6 volts, turning both the predriver, GE D43C5, and the pass transistor, TIP36, on. When the output voltage reaches 5.4 volts, the voltage at pin 11 switches to approximately + 30 VNR, turning both transistors off. The difference in switching points is due to the hysteresis added by returning the collector of the TIP36 through a 220K resistor to pin 5. The frequency of oscillation will vary with load. As the load increases, the frequency increases, reaching a maximum of about 25 KHz at full load.

Over-voltage protection is provided by an SCR 2N 4441. When + 5 volts rises above approximately 7.5 volts the SCR turns on, blowing the 15 ampere fuse which removes + 30 VNR from the regulator.

Short circuit protection is provided by R19, CR4, and C7 which are connected between pins 2 and 3 of U2. The comparator circuit (μA723) requires the voltage at Pin 3 to always be higher than at Pin 2. When the output is at the μ 5 volt level pin 3 is higher (voltagewise) than pin 2 by the forward drop of diode CR4. If the + 5 volt output becomes shorted to ground, then pin 3 for that instant will be at or close to ground. Pin 2 on the other hand, will be at an approximate + 0.5 volt level due to the series divider network composed of Zener diode VR3, and resistors R18 and R19. This causes the comparator to open circuit the output voltage. Capacitor C7 is incorporated (in parallel with CR4) to provide dampening for any high frequency surges that may appear on the + 5 volt output lines.

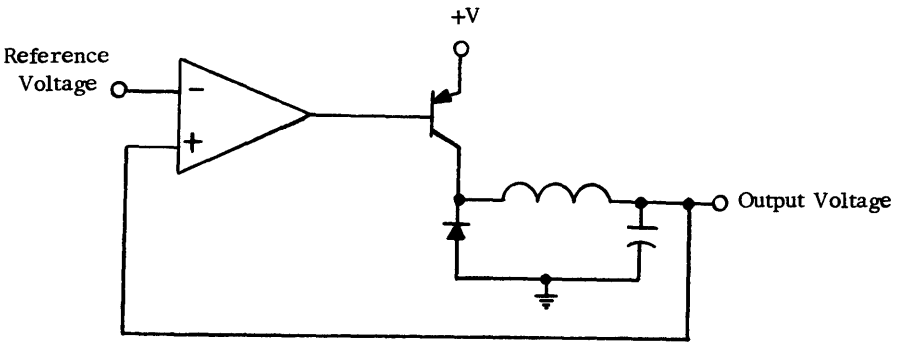


Figure 4- 5. +5 Volt Regulator Functional Diagram

4-4.3 + 15 Volt Regulator

The + 15 volt regulator differs from the + 5 volt regulator in only one respect. The output voltage, rather than the reference voltage is divided down, before being applied to the voltage comparator. The short circuit protection and the over-voltage protection is the same as described for the + 5 volt regulator as both regulators are powered by the + 30 VNR@ 15 amp line, and incorporate similar circuitry between pins 2 and 3 of the comparator.

4-4.4 + 30 Volt @ 4 amps Generation

The + 30 volt @ 4 amps source is a filtered non-regulated voltage used exclusively by the - 15 volt regulator. At nominal line voltages the rectifier and filter output will also be between + 32 and + 35.5 volts depending on the load conditions. A 4 amp fast blow fuse provides protection between the filter output and the - 15 volt regulator.

4-4.5 - 15 Volt Regulator

The main difference between the -15 volt regulator and the other two regulators is that the output from the regulator filter (L1 and C10) is grounded with the -15 line taken from the normal ground bus of the circuit (pin 7 of the comparator). This output connection and the separate 30 volt rectifier-filter source are the only differences between the + 15 volt regulator and the - 15 volt regulator. It is noted that the - 15 volt regulator is not overvoltage protected by the 2N441 SCR circuit. Zener diode VR4, resistors R4, R3, diode CR3, and capacitor C2 are connected between the + 30 volt (4 amp) source and pins 2 and 3 of comparator U1 (and ground) to provide short circuit protection in the exact same manner described for the + 5 volt circuit.

4-4.6 Power Low Monitor Signal Generation

Transistor Q6 monitors the level on the + 30 VNR line to determine when a power failure is in process. The output from this transistor controls the POWER LOW line to the Adapter Plug and Logic Interface. The + 30 VNR line is monitored by VR2 which has a nominal 24 volt Zener characteristic @ 5.2 milliamperes). Thus, as long as + 30 VNR remains at or above Zener level the voltage drop across R28 will be sufficient to keep Q6 in saturation, thereby holding the POWER LOW line to 0 volts. Once the Zener extinguishes Q6 will cease conduction and allow the POWER LOW line to swing to the + 5 volt level or logic 1 level. This level causes the Adapter logic to initiate a string of clearing functions. POWER LOW also produces a direct-set for the ADAPT Done flip-flop, which in turn implements logic to immediately set the DP Done flip-flop within the Controller.

The wires used to connect the power supply output voltage terminals (located near the rear edge of the power supply PCB assembly) with the Adapter Plug and Logic Interface sections are identified and described in Chapter 5 of this manual.

SECTION V

MAINTENANCE

5-1 GENERAL

The Diagnostic test programs supplied by Data General are bi-functional from a maintenance point of view, in that they are used both to verify that the Disk installation is completely operational, while they may also be used for fault isolation. Preventative maintenance scheduling of the Disk diagnostic tests depend on the operation schedules established by the user and will vary from installation to installation. The 4046 Control assembly and 4047 or 4049 Adapter unit require no preventative maintenance such as periodic adjustments or lubrication. However, a general periodic inspection should be given the system IO and power cables for fraying or wear. Check all plugs and connectors for being properly seated in their respective connection locations. Check the cooling fan in the Adapter unit periodically for proper unobstructed operation. Maintenance Procedures for the 4047A or 4047B Disk Drive unit are presented in Manual No. D3140-171 shipped with each unit under separate cover. Thus, the remaining descriptions and procedures of this Chapter are applicable only to the 4046 Controller Assembly and the 4047 or 4049 Adapter unit.

5-2 SPECIAL TOOLS AND TEST EQUIPMENT

The following is a list of special tools and test equipment recommended for servicing the 4046 Control PCB Assembly and the 4047 or 4049 Adapter unit.

MULTIMETER

OSCILLOSCOPE

LONG LEAD PROBES

EXTENDER BOARD

WIRE WRAP TOOL
(24 GAUGE)

IC TEST CLIP

SOLDERING IRON

SIMPSON MODEL 260
OR EQUIVALENT

TEKTRONIX 453
OR EQUIVALENT

TEKTRONIX P6010-10X
OR EQUIVALENT

DGC 107-000007-02

GARDNER DENVER
Model 14AX2
OR EQUIVALENT

MANUFACTURED BY A. P. INC.
Plainesville, Ohio

WELLER ISOLATED
Model W-TCP
OR EQUIVALENT

5-3 DIAGNOSTIC PROGRAMS

The Disk Diagnostics are individual programs which together test all logical operations of a Disk installation. Individually the programs test various logic areas of the 4046 Controller and the Adapter Interface Logic. The majority of the diagnostic routines are capable of diagnosing malfunctions down to the logic level and provide a means of measuring the performance of the system on a repeatable basis. Copies of diagnostic tapes as well as individual program documentation are part of the software package delivered with each Disk Cartridge system. Individual program documentation provides information as to operating procedures, error interpretation, console switch settings and logical areas tested. Certain diagnostics may be scheduled as part of daily and weekly preventive maintenance routines.

DIAGNOSTIC PROGRAMS

PROGRAM	DESCRIPTION
Disk Diagnostic (See DG Document 097-000039 for other details and restrictions.)	The Diagnostic program examines the states of specific functional logic sections within the 4046 Disk Controller on a gate by gate basis. The program requires a Nova or Supernova Processor, a 4046 Disk Controller, a 4047 or 4049 Disk Adapter, 1 to 4 Disk Drive units, and a Teletype (and Teletype Control). The program assumes that the Disk Drive units are all operating properly. Special Operating functions are provided by the program through assignment of special Starting Addresses and Console Switch settings.
Disk Reliability Test (See DG Document 097-000038 for other details and restrictions.)	The Moving Head Disk Reliability program tests and exercises the 4046 Disk Controller and from 1 to 4 Disk Drive units. The program requires the same equipment configuration identified above for the Diagnostic program. The program is designed to be compatible with a Disk Drive configuration shared between two computers. In this particular configuration the Reliability program could be run simultaneously in both computers. The Disk Reliability test writes and reads various data patterns (e.g., Zeroes, Ones, Random) on the disk. The program also performs several address tests along with other sector reading and writing tests. Special operating functions are provided by the program through assignment of special Starting Addresses. The program features a Command String Interpreter (Starting Address 405_8) which may be used as a trouble shooting tool.

5-4 TROUBLE SHOOTING PHILOSOPHY

Effective trouble shooting is accomplished in a minimum of time by following a series of logical steps. The ultimate aim is to effectively pinpoint the actual problem using all information available. Locating the malfunction is then the next step. The following is a suggested plan for effective casualty analysis:

a) Investigation - record the state of the equipment on error occurrence. Look for obvious symptoms including operator error, loose plugs or connectors, blown fuses, etc.

b) Isolation - through the use of diagnostic programs or console trouble shooting techniques attempt to isolate the malfunction to a particular board, i.e., Disk Controller PCB or Disk Adapter logic PCB, or the Disk Drive unit itself.

c) Component Isolation - Isolate the faulty component using an oscilloscope and the diagnostic programs. Selecting the correct oscilloscope external sync is of importance at this point.

d) Replace the faulty component and retest by running the diagnostic that originally failed.

e) Record for future reference, the symptoms, cause, unique trouble shooting method/s used to isolate the malfunction.

5-5 ADAPTER POWER SUPPLY CHECKOUT

The sequence of checks below should be performed to verify that the Adapter power supply is operational after a power malfunction and before ac power is reapplied to the supply. Paragraph 5-5.2 lists the power supply output voltages under load. After completing the preliminary checklist (of paragraph 5-5.1) ac power may be reconnected and turned on. At this time the output dc voltages may be measured (and compared against the data specified) to complete the checkout procedures.

5-5.1 Power Supply Checks with AC Power Disconnected

a) Check continuity of ac (line) connections into the supply.

b) Check for proper transformer connections.

c) Check for correct fuse values.

d) Check for shorts between ac connections, ac connections to ground, dc voltage terminals to ground.

e) Check screw terminals of dc output voltage connections (on the rear of the power supply PCB assembly) for tightness. Verify screws are bound tightly down on the associated connection lugs.

f) Check dc wiring from power supply PCB to back panel of the Adapter Plug Interface. Make sure all connections are present and secure.

5-5.2 Power Supply Outputs Under Load

The specifications listed below pertains to the single power supply built into Adapter 4047. Since Adapter 4049 contains two identical supply units of the type built into Adapter 4047, all current values are twice the values listed.

a) + 5 VDC @ 3.0 Amps + 5.5 to + 4.5 VDC < 150 mv Ripple Max.
b) + 15 VDC @ 8.0 Amps + 16.5 to + 13.5 VDC < 150 mv Ripple Max.
c) - 15 VDC @ 5.0 Amps - 13.5 to - 16.5 VDC < 150 mv Ripple Max.

5-6 IC IDENTIFICATION

Table 5-1 is included in this section to facilitate any trouble shooting procedures that require identification between any IC reference number (U1-Un) and the original manufacturer's part number. The IC list is divided into four columns, the first for the 4046 Disk Controller PCB assembly, the second for the Adapter Logic Interface PCB assembly, the third for the Adapter Plug Interface PCB assembly, and the fourth for the Adapter Power Supply PCB subassembly.

Table 5-1. IC Identification List

IC CHIP	4046 DISK CONTROLLER	4047/4049 ADAPTER LOGIC INTERFACE	4047/4049 ADAPTER PLUG INTERFACE	4047 ADAPTER POWER SUPPLY
U1	9003	7474	9602	μA723
U2	8H90	9016	8271	μA723
U3	9002	9602	9322	μA723
U4	9003	9016	9322	
U5	9003	9002	9322	
U6	9003	9015	7474	
U7	8H90	9321	9015	
U8	9007	9016	9322	
U9	7438	8202	9322	
U10	8H90	9016	9002	
U11	7438	9002	9322	
U12	9003	3001		
U13	7438	9002		
U14	7438	3001		
U15	7438	9602		
U16	7438	7474		
U17	9602	9602		
U18	9002	3003		
U19	7474	3001		
U20	9015	7474		
U21	3001	9602		
U22	7474	7474		
U23	7438	9602		
U24	9002	9015		
U25	9015	7486		
U26	7474	7474		
U27	7474	3003		
U28	7474	9015		
U29	7438	7474		
U30	8H90	9002		
U31	8H90	9003		
U32	8H90	7474		
U33	8H90	3061		
U34	9015	7474		
U35	3001	9016		
U36	9002	8281		
U37	7474	9002		

IC CHIP	4046 DISK CONTROLLER	4047/4049 ADAPTER LOGIC INTERFACE	4047/4049 ADAPTER PLUG INTERFACE	4047 ADAPTER POWER SUPPLY
U38	7474	9004		
U39	9009	9003		
U40	314A	7486		
U41	8291	9328		
U42	3001	7474		
U43	7474	3001		
U44	7474	7474		
U45	8266	9602		
U46	8267	7438		
U47	8291	7474		
U48	8291			
U49	8264			
U50	9322			
U51	9322			
U52	8202			
U53	74198			
U54	7474			
U55	9015			
U56	8271			
U57	9002			
U58	9602			
U59	8291			
U60	3003			
U61	7474			
U62	7474			
U63	9322			
U64	8267			
U65	8291			
U66	8291			
U67	8264			
U68	9322			
U69	9322			
U70	8200			
U71	74198			
U72	9602			
U73	9015			
U74	8H90			
U75	7474			
U76	9002			
U77	8291			
U78	9321			
U79	9002			
U80	8H90			
U81	9322			
U82	8267			
U83	8291			
U84	8291			
U85	8264			
U86	9322			
U87	9322			
U88	8202			
U89	74198			
U90	9003			
U91	9007			
U92	8291			

IC CHIP	4046 DISK CONTROLLER	4047/4049 ADAPTER LOGIC INTERFACE	4047/4049 ADAPTER PLUG INTERFACE	4047 ADAPTER POWER SUPPLY
U93	3001			
U94	8202			
U95	8202			
U96	8267			
U97	8291			
U98	8291			
U99	8264			
U100	9322			
U101	9322			
U102	7474			
U103	74198			