Digital Equipment Corporation
Maynard, Massachusetts

digital

Maintenance Manual
PDP-9/L
Volume II

DEC-9L-HMBA-D

PDP-9/L
Maintenance Manual
Volume II

DIGITAL EQUIPMENT CORPORATION ▫ MAYNARD, MASSACHUSETTS

1st Printing February 1969

The following are registered trademarks of Digital Equipment Corporation, Maynard, Massachusetts:

DEC	PDP
FLIP CHIP	FOCAL
DIGITAL	COMPUTER LAB

ENGINEERING DRAWINGS

GENERAL

This volume contains a complete set of engineering drawings pertaining to the basic PDP-9/L system. A formal set of engineering drawings is also shipped with each PDP-9/L system, including those for all ordered options. Where a discrepancy exists between furnished drawings and those contained in this volume, it must be assumed that the drawings furnished with the machine are correct.

USE OF DRAWING CODES

DEC engineering drawing numbers are encoded as to drawing type, major assembly, and series. A drawing number such as BS-KD09-A-11 contains the following information: BS, block schematic type; KD09, the I/O control section of the PDP-9/L; A, the manufacturing series; 11, the eleventh drawing in the I/O control series, which happens to be the teletype control schematic. In Volume I this drawing is referred to as KD11. The complete glossary of drawing type codes is as follows:

AD	Assembly Drawing
AR	Arrangement Drawing
BD	Functional Block Diagram
BS	Block Schematics
CD	Cable Diagram
CP	Component List
CS	Circuit Schematic
FD	Flow Diagram
IC	Interface Cabling Diagram
LO	Layout Drawing
MU	Module Utilization Drawing
PL	Parts List
RS	Replacement Schematic
SP	Specification Drawing
TD	Timing Diagram
UA	Unit Assembly
WD	Wiring Diagram
WL	Wiring List

DRAWING CONVENTIONS

Block schematics are multipurpose drawings that combine signal flow, logic functions, circuit type, physical location, and other pertinent information. Individual circuits are shown in block form, using special symbols which define the circuit operation. These symbols are explained in the Logic Handbook C105.

SIGNAL MNEMONIC INDEX

All signals originating in the PDP-9/L are listed in alphanumeric order below. The origin column locates the source of each signal to the particular logic drawing.

Signal	Origin	Description
0 → CMA	KC19(1)	Clear the control memory address register
0 → MBI	KC19(2)	Clear the memory buffer input gate
0XEN	KD3(1)	Enable devices 0X
00XXEN	KD3(1)	Enable devices 00XX
+1	KC19(1)	Increment the ADR
1 → ACI	KC19(2)	Set the accumulator register input gate
+1 → CA INH	KD2(2)	Inhibit increment of DCH CA register
1 → MBI	KC19(2)	Set the memory buffer input gate
1 → PCI	KC12	Set the program counter input gate
13 → CMA	KC19(1)	Set CM address to 13
ΔMB	KC19(2)	Change the memory buffer contents
A,B,C	KC10(1)	Program start timing flip-flops
A BUS00-05	KC20(1)	A bus contents
A BUS06-11	KC20(2)	A bus contents
A BUS12-17	KC20(3)	A bus contents
A BUS LINK	KC15	Recirculate LINK status
AC00-05	KC20(1)	Accumulator register contents
AC06-11	KC20(2)	Accumulator register contents
AC12-17	KC20(3)	Accumulator register contents
AC D	CS3	Display the accumulator register contents
ACI	KC19(2)	Accumulator register input gate
ACO	KC19(3)	Accumulator register output gate
AC RD	KD3(3)	Read the accumulator register contents into core memory
AC RD(B)	KC19(2)	Read the accumulator register contents into core memory
AC SIGN	KC15	AC00 status
ADDR SW03-17	CS3	Address switch contents
ADOF	KC15	Add data overflow, ADD instruction and DCH add-to-memory
ADR00-05	KC21(1)	Adder register contents
ADR06-11	KC21(2)	Adder register contents
ADR12-17	KC21(3)	Adder register contents
ADR = 0 SAVE	KC15	ADRA = 0, ADRB = 0 status
ADRA = 0	KC21(1) KC21(2)	ADR00-08 = 0
ADRB = 0	KC21(2 KC21(3)	ADR09-17 = 0

Signal	Origin	Description
ADRL ADRL(B)	KC15	Adder link
ADSO ADSO(G)	KC19(2) KD7(1)	Address switches output gate
AM GRANT	MC1(2)	Grant core memory access to DMA channel
AM STROBE	MC2	Core memory strobed for DMA channel access
AM SYNC AM SYNC(1)B AM SYNC BUS	MC1	Synchronization for DMA cycle
AND	KC19(1)	AND instruction gate
API D	CS3	Display the optional API channel activity
API IO CLR	KD3(2)	
API ON BUS	KD7(1)	Gate optional API activity onto I/O bus (B)
API 0,1,2,3 RQ	KD2(2)	Request API channel break
AR00-05	KC20(1)	Arithmetic register contents
AR06-11	KC20(2)	Arithmetic register contents
AR12-17	KC20(3)	Arithmetic register contents
ARD	CS3	Display the arithmetic register contents
ARI	KC19(2)	Arithmetic register input gate
ARO	KC19(3)	Arithmetic register output gate
ARO RESTORE	KC12 KC10(2)	Restore the arithmetic register output gate
AROS	KC10(2)	Save the arithmetic register output gate
AUT INX	KC14	Increment the contents of indirectly addressed core memory register 00010-17
AXS	KC19(2)	ADD, XOR, SAD instruction gate
B BUS00-05	KC21(1)	B bus contents
B BUS06-11	KC21(2)	B bus contents
B BUS12-17	KC21(3)	B bus contents
BK	KD3(2)	Start program break process
BK CA	KC10(1)	CA cycle of DCH break (memory extension control)
BK0 BK0(0)B BK0(1)B BK1 BK1(0)B	KD3(3)	Break cycle counter
BK1(1)B	KC10(1)	
BK SYNC	KD3(2)	Synchronize program break entry
BS SW3-4	MC2	Core memory bank selection switches

Signal	Origin	Description
CAF EN CAF EN(B)	KD3(1)	Clear all flags enable
CAL	KC12	CAL instruction gate
CI17	KC14	Initiate a carry into ADR17
CJIT	KC12 KC19(3)	CAL/JMS/Interrupt Transfer gate
CLK	KC10(1)	Main clock pulse
CLK(B)	KD3(2)	
CLK DLY'D	KD3(3)	Main clock pulse delayed 500 ns
CLL	KC13	Clear the LINK
CLR	KC16	Clear the +1, ACO gates, set the SAO, ARO gates
CLR I	KC19(2)	Clear the MBO, ACI, ARI, PCI, MQI gates
CLR PUN	KD10(1)	Clear the punch buffer and punch flag
CLR RDR	KD9(1)	Clear the RDR FLG, RDR 1, RDR 2 flip-flops
CMA00-05	KC19(1)	Control memory address register contents
CM CLK	KC10(1)	Main clock pulse to control memory
CM CURRENT	KC16	Turn on control memory address selectors
CMG00-07	KC17	Control memory current lines
CML	KC13	Complement the LINK
CMPL	KC13	Complement the ADR contents
CMP00-07	KC17	Control memory current lines
CMSL00-35	KC17 KC18(2)	Control memory sense lines
CM STROBE A,B,C,D	KC16	Strobe the control memory
CM STROBE DLYD	KC16	
CONT	KC19(1)	Continue gate
CO00-05	KC21(1)	Carry out of ADR00-05
CO06-11	KC21(2)	Carry out of ADR06-11
CO12-17	KC21(3)	Carry out of ADR12-17
DASO	KC13	Data switches output gate
DATA OFLO	KC15	DCH add-to-memory data overflow
DATA SW00-17	CS3	Data switch contents
DB RESTORE	KD3(1)	
DBR DBR(B)	KD3(1) KC15	Debreak and restore the interrupted program
DCH	KC19(1)	
DCH BK DLY	KD3(1)	Illuminate the DCH display indicator

Signal	Origin	Description
DCH EN	KD3(1)	Enable the DCH Multiplexer W104
DCH GRANT	KD3(1)	Grant core memory access to the DCH
DCH GRANT P		
DCH INX	KD3(3)	Increment the DCH WC or CA register
DCH RQ	KD2(2) KD3(2)	DCH break request
DCH SYNC SAVE	KD3(2)	Save the DCH SYNC status
DEI	KC19(1)	Initiate the defer or execute cycle
DIGIT READ DRIVE	MC1(2)	Turn on core memory address selectors
DIGIT READ ON	MC2	Turn on DIGIT READ DRIVE, DIGIT READ SINK
DIGIT WRITE DRIVE	MC1(2)	Turn on core memory address selectors
DIGIT WRITE SINK	MC1(2)	Turn on core memory address selectors
DLY	KD3(3)	Clock pulse delayed 500 ns
DONE DONE(1)B	KC19(1) KD3(2)	Instruction DONE gate
DPY D	CS3	Display x, y buffers of optional 34H Display
DPY ON BUS	KD7(1)	Gate x, y buffers of optional 34H Display onto the IO Bus(B)
DS00-05	KD3(1)	Device select bits
DS00P-05P		
EAE	KC19(1)	Optional extended arithmetic element gate
EAE D	CS3	Not wired
EAE-P EAE-R	KC19(1)	Optional extended arithmetic element gate
EAE STROBE DLYD	KC16	CM STROBE delayed for optional extended arithmetic element
END BIT 0	KC15	LINK to ADRL to AC17. Also for optional extended arithmetic element gating
END BIT 17	KC15	Optional extended arithmetic element gating
EXT EXT(1)B	KC19(3) KD3(3)	External transfer gate (program breaks)
FEED HOLE	KD9(2)	Reader no-tape sensor
FWD FD and NDX	KD10(1)	Punched tape drive power
GO DLY	KD9(1)	Reader enable delay
IND CLK	KC10(1)	Gate CP register contents for display
IN CLR	KC16	Generate CLR I
INC V DCH	KD3(2)	Enter DCH or RTC WC cycle

Signal	Origin	Description
IND EN	KC10(1)	Enable console display selector switch
INC MB	KD2(2) KD3(3)	Increment the memory buffer contents
IN LAST UNIT	KD11(1)	Last keyboard code unit shifted into input buffer
INPUT IO RESTART	KD8 KD3(3)	Restart control memory after manual read-in, EAE, or IOT instruction
INT RD RQ BUS	KD3(3)	Internal read request bus
INT SKP RQ BUS	KD3(1) KD9(1) KD10(1) KD11(1) KD11(2)	Internal skip request bus
IO0 IO1	KD3(3)	Input/output transfer cycle counter
IO ADDR 03-17 IO ADDR 03(B)-17(B)	KD2(2) KD5	DCH and optional API channel address
IO ADDR 12,16,17	KD5	Optional API channel address
IO ADDR D	CS3	Display DCH or optional API address
IO ADDR ON BUS	KD7(1)	Gate DCH or optional API address onto I/O bus (B)
IO BUS00-05 IO BUS06-11 IO BUS12-17 IO BUS00-17	KC21(1) KC21(2) KC21(3) KD2(1)	I/O bus contents
IO BUS00(B)-08(B) IO BUS09(B)-17(B)	KD7(1) KD7(2)	I/O bus buffered
IO BUS ON	KC19(3)	ADR to I/O bus gate
IO CLK(B)	KD3(3)	Main clock pulse
IO CLK POS	KD3(2)	Main clock pulse
IO CLR	KD3(2)	Clear PROG SY, PROG SYNC, BK
IO OFLO	KD3(2)	DCH or RTC operations completed
IOP1	KD3(1) KD3(3)	Input/output pulse 1
IOP2	KD3(1) KD3(3)	Input/output pulse 2
IOP4	KD3(1) KD3(3)	Input/output pulse 4
IOP1P	KD3(3)	Input/output pulse 1
IOP2P	KD3(3)	Input/output pulse 2
IOP4P	KD3(3)	Input/output pulse 4

Signal	Origin	Description
IO PWR CLR IO PWR CLR POS	KD3(1) KD3(1)	I/O power clear pulse
IO RESTART	KD3(3)	Restart control memory after manual read-in, EAE, or IOT instruction execution
IO RUN(1)	KD3(1)	Computer RUN condition to I/O devices
IO SKIP	KD3(3)	Skip next instruction on SKIP RQ from I/O device
IO SYNC	KD3(1)	Synchronize program break entry
IO SYNC IN	KD3(2)	Synchronize program break entry
IO SYNC POS	KD3(2)	Synchronize program break entry
IO SYNC SP	KD3(1)	Synchronize optional API break entry
IOT	KC12	Input/output transfer gate
IOT0002 IOT0004 IOT0102 IOT0104 IOT0204 IOT0302 IOT0404 IOT3344	KD3(1) KD3(1) KD9(1) KD9(1) KD10(1) KD11(1) KD11(2) KD3(1)	IOT command
IOT(B)	KD3(1)	Input/output transfer gate
IOT OR ARO	KC12	Set ARO gate for programmed output transfer
IOT PWR CLR	KD3(1)	
IR00-04	KC12	Instruction register contents
IRI	KC19(1)	Instruction register input gate
ISZ	KC12	ISZ instruction gate
KBD FLG	KD11(1)	Keyboard flag
KBD SEL KBD SEL(B)	KD11(1)	Keyboard select
KCT KCT(B)	CS3 KC10(1)	CONTINUE key
KDN	CS3	DEPOSIT NEXT key
KDP	CS3	DEPOSIT key
KDPDN	KC10(1)	DEPOSIT/DEPOSIT NEXT key
KDPDN V RI	KC19(3)	DEPOSIT/DEPOSIT NEXT key or READ-IN key
KDPM	CS5	DEPOSIT key (maintenance)
KEY	KC19(2)	Key gate
KEY BUS KEY BUS(B)	KC10(1)	Key bus
KEY DLY	KC10(1)	Delay key-activated RUN condition

Signal	Origin	Description
KEY INIT POS	KC10(1)	Initiate key operations
KEYΛ KDPDN	KC13	
KEN	CS3	EXAMINE NEXT key
KEYS	CS5	
KEX	CS3	EXAMINE key
KIO	CS3	I/O RESET key
KIOA3, A4, A5	KC10(1)	Key process address to control memory
KMT	CS5	Key (maintenance)
KRI	CS3	READ-IN mode key
KSP	CS3	STOP key
KST	CS3	START key
KXDM	CS5	EXAMINE/DEPOSIT key (maintenance)
LAR	KC15	Arithmetic register link
LI	KC19(1)	LINK input gate
LINK	KC15	Accumulator register link
LIO	KC13	Load I/O data onto I/O bus
LOCK	CS5	Lock the console controls
LOT	KC12	LAW/OPR/IOT instruction gate
MA05-13 MA14A-17A MA14B-17B	MC1(1)	Memory address register contents
MA06(0) Λ MA07(0)	MC1(1)	Memory address register bits decoded for address selection
MA06(0) Λ MA07(1) MA06(1) Λ MA07(0) MA06(1) Λ MA07(1) MA10(0) Λ MA11(0) MA10(0) Λ MA11(1) MA10(1) Λ MA11(0) MA10(1) Λ MA11(1) WR(1) Λ MA05(1) V WW(1)Λ MA05(0) WR(1) Λ MA05(0) V WR(1) Λ MA05(1)		
MA JAM DIGIT MA JAM PAR MA JAM WORD	MC1(1)	Strobe address into memory address register
MAS03-04	MC2	Memory address bits decoded for expanded memory

Signal	Origin	Description
MB00-05 MB06-11 MB12-17	KC21(1) KC21(2) KC21(3)	Memory buffer register contents
MBI MBI(1)B	KC19(2) KC28	Memory buffer input gate
MBO	KC19(3)	Memory buffer output gate
MBS00-17	MC3	Core memory input mixer bits
MEM DONE MEM DONE(1)B	MC1(2)	Core memory cycle done
MEM STROBE MEM STROBE(B)	MC2 KC28	Core memory strobed for CP access
MK	CS5	
MODE	MC1(2)	Core memory access mode
MQ00-05 MQ06-11 MQ12-17	KC20(1) KC20(2) KC20(3)	Optional multiplier/quotient register contents
MQ D	CS3	Display the optional multiplier/quotient register contents
MQI	KC19(2)	Optional multiplier/quotient input gate
MQO	KC19(3)	Optional multiplier/quotient output gate
NDX	KD10(1)	Punch the tape feed holes
NOSH	KC13	NO SHIFT gate
O BUS00-05 O BUS06-11 O BUS12-17 O BUS00-17	KC20(1) KC20(2) KC20(3) KC22	O bus contents
O BUS L OFLO OFLO	KC15 KC14 KC15	LINK status to optional EAE DCH, RTC word count overflow ADD instruction overflow
OP	KC12	OPR instruction gate
OR ACI	KC12	Set the ACI gate for programmed input transfer
OR MBO	KC12	Set the MBO gate for LAW instruction
PB10-17	KD10(1)	Punch buffer contents
PC05 PC06-17 PC012-17	KC20(1) KC20(2) KC20(3)	Program counter contents
PC D	CS3	Display the program counter contents
PCI	KC19(2)	Program counter input gate
PCO	KC19(3)	Program counter output gate
PCO RESTORE	KC10(2)	Restore the PCO gate

Signal	Origin	Description
PCOS	KC10(2)	Save the PCO gate
PIE	KD3(2)	Program interrupt enable
PIE(0)	KD3(2)	Program interrupt disable
PK CLR	KC10(1)	Power and key clear pulse
PK CLR(B)	MC2	
POST CLK	MC2	Main clock delayed/strobe the MODE flip-flop
PRE-STROBE	MC2	Generate MEM STROBE, STROBE SAL, STROBE SAR
PRE-WRITE OFF	MC2	Set MEM DONE, issue AM GRANT
PROG INT RQ	KD2(1) KD3(2) KD9(2) KD10(1) KD11(1) KD11(2)	Program interrupt request
PROG SY PROG SY(1)B PROG SYNC PROG SYNC(1)B	KD3(2)	Synchronize program interrupt entry
PUN	KD10(1)	Punch mechanism operating
PUN ACT	KD10(1)	Actuate punch mechanism
PUN FEED	KD10(2)	Punch feed holes manually
PUN FLG	KD10(1)	Punch flag
PUN HOLE 1-8	KD10(1)	Punch buffer bits to punch solenoids
PUN LINE	KD10(1)	Enable punch solenoid drivers
PUN NO TAPE	KD10(1)	Punch out of tape
PUN PWR	KD10(1)	Punch power
PUN PWR ON	KD10(1)	Punch power on
PUN SEL	KD10(1)	Punch select
PUN SPD	KD10(1)	Punch motor up to speed
PUN SYNC	KD10(2)	Punch motor in punching position
PV	KC12	Memory protection violation
PWR(B)	KD9(1)	Reader power on
PWR CLR POS	KC10(1)	Power clear pulse
RB00-17	KD9(2)	Reader buffer contents
RD HOLE 1(B)-7(B)	KD9(2)	Punched tape contents
RD HOLE 7(C)	KD9(2)	Punched hole 7
RD HOLE 8(B)	KD9(2)	Punched hole 8
RD HOLE 8P V ALPHA	KD9(2)	Reader binary or alpha mode
RD IO BUS	KD7(1)	
RDR 1	KD9(1)	Read first line of tape into reader buffer
RDR 2	KD9(1)	Read second line of tape into reader buffer
RDR A RDR A(0)B RDR A(1)B	KD9(1) KD9(2) KD9(2)	Reader line index count
RDR ALPHA	KD9(1)	Reader alpha mode
RDR B RDR B(0)B RDR B(1)B	KD9(1) KD9(2) KD9(2)	Reader line index count
RDR CLK	KD9(1)	Reader clock pulse
RDR CLK EN	KD9(1)	Reader clock enable
RDR COUNT	KD9(1)	Reader line index count
RDR D	CS3	Display the reader buffer contents
RDR FEED	KD9(2)	Feed tape manually without reading
RDR FLG RDR FLG(B)	KD9(1) KD8	Reader flag
RDR GO	KD9(1)	Enable reader clock
RDR INDEX	KD9(1)	Reader clock pulses
RDR NO TAPE	KD9(1)	Reader out of tape
RDR ON BUS	KD7(1)	Gate reader buffer contents onto I/O bus (B)
RDR PWR	KD9(1)	Reader power
RDR RUN	KD9(1)	Generate RUN
RDR SEL RDR SEL(B)	KD9(1)	Reader select
RD RQ RD RQ(B)	KD2(1) KD3(3)	Read request from I/O device
RD START RQ	KC10(1)	Read manually entered tape word into core memory
RD STATUS	KD11(1)	Read teletype status
R12(1)B	KD8	Manually entered tape word count
RQ MBI	KC19(2)	Turn on memory buffer input gate
RSB	KD8	Select reader binary mode
RUN	KD9(1)	Set RDR GO
RUN RUN(1)B	KC10(1)	Computer program started
RUN(0)	KC10(1)	Computer program stop
SA00-17	MC6	Sense amplifier contents
SAO SAO(0)B	KC19(3) KC15	Sense amplifier output gate

Signal	Origin	Description
SD00-01 SD00P-01P	KD3(1)	Special device select bits
SEN SEN(1)B	KC10(2) KC10(1)	Computer RUN sensor
SHIFT	KC15	Shift ADR contents enable
SHL1	KC13	Shift ADR contents left one position
SHL2	KC13	Shift ADR contents left two positions
SHR1	KC13	Shift ADR contents right one position
SHR2	KC13	Shift ADR contents right two positions
SKIP	KC14	Skip next instruction gate
SKIP RQ	KD2(1)	Skip request from I/O device
SKPI	KC19(1)	Skip input gate
SM	KC19(2)	Start memory gate
SPEED 2,3,4	CS3	Repeat speed selections
SPEED WIPER	CS3	Repeat speed switch wiper
STATUS D	CS3	Display the I/O device status bits
STATUS ON BUS	KD7(1)	Gate the I/O device status bits onto I/O bus (B)
STOP DLY	KD9(1)	Decelerate the reader motor
$\overline{\text{STOP DLY}}$	KD9(1)	Permit reader motor to restart
STOP DLY POS	KD9(1)	Disable reader clock
STROBE DLYD	KC16	Control memory strobe delayed
STROBE SAL	MC2	Strobe the left hand sense amplifiers
STROBE SAR	MC2	Strobe the right hand sense amplifiers
SW EXD	CS3	Optional memory extend mode switch
SW SGL INST	CS3	Single instruction switch
SW PARITY	CS3	Optional memory parity switch
SW PRTCT	CS3	Optional memory protect switch
SW REPT	CS3	Repeat switch
SUB	KC19(1)	Subtract gate
SYNC CLK	MC2	Set AM SYNC if AM RQ is present
TAPE	KD10(2)	Punch out of tape
TI	KC19(1)	Test for indirect address gate
T-PRNTR FLG	KD11(2)	Teleprinter flag
T-PRNTR SEL T-PRNTR SEL(B)	KD11(2)	Select teleprinter
TTI00-07	KD11(1)	Teletype input buffer contents
TTI CLK	KD11(1)	Teletype input clock
TTI D	CS3	Display the teletype input buffer contents
TTI FULL	KD11(1)	Teletype input buffer is full
TTI INITIALIZE	KD11(1)	Initialize teletype input buffer and controls
TTI LOAD	KD11(1)	Load the teletype input buffer
TT IN ACT	KD11(1)	Teletype input circuits active
TTI ON BUS	KD7(1)	Gate teletype input buffer contents onto I/O bus (B)
TT KBD IN TT KBD IN(B)	KD11(1)	Teletype keyboard input
TT LINE	KD11(2)	Actuate teleprinter to generate space or mark
TTO00-07	KD11(2)	Teletype output buffer contents
TTO CLK	KD11(2)	Teletype output clock
TTO EN	KD11(2)	Teletype output enable
TTO EQ	KD11(2)	All teletype output buffer bits serially shifted into teleprinter
TTO LOAD	KD11(2)	Load the teletype output buffer
TTO OUT ACT	KD11(2)	Teletype output circuits active
TT RDR RUN	KD11(1)	Release teleprinter magnet to generate marks and spaces
TTO START	KD11(2)	Start teletype output operations
TTO STOP	KD11(2)	Stop teletype output operations
WORD READ	MC1(2)	Turn on core memory address selectors
WORD READ ON	MC2	Turn on WORD READ
WORD WRITE	MC1(2)	Turn on core memory address selectors
WRITE OFF	MC2	Turn off core memory address selectors
WRITE ON	MC2	Turn on DIGIT WRITE DRIVE, DIGIT WRITE SINK
WR RQ	KD2(2) DK3(3)	Write request from I/O device
$\overline{\text{WR RQ(B)}}$	KD3(2)	

9/L SYSTEM

POWER SUPPLY AND DISTRIBUTION

MEMORY (MC71-A)

MEMORY (MC71-A) (Cont)

CENTRAL PROCESSOR

CENTRAL PROCESSOR (Cont)

I/O

I/O (Cont)

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION 9-L	9-LA
1	E-AD-7005870-0-0	CABINET FRAME 9L	1	1
2	D-UA-712-0-0	POWER SYPPLY 712	1	-
2	D-UA-712-A-0	POWER SUPPLY 712-A	-	1
3	9006073-3	PHL HD TRUSS #10-32 x ½	25	25
4	9007651	WASH EXT TOOTH #10	23	23
5	D-UA-H951-TA-0	H951-TA NARROW DOOR	1	1
6	D-IA-7406731-0-0	LOGO PDP-9L	1	1
7	D-UA-H950-Q-0	H950-Q 19" COVER PANEL 10½"	3	3
8	E-AD-7005875-0-0	9L CONSOLE ASSY	1	1
9	D-AD-7005859-0-0	TABLE ASSEMBLY	1	1
10	D-IA-7406723-0-0	KICK PANEL	1	1
11	9006074-3	PHL HD TRUSS #10-32 x 5/8	2	2
12	9006565	NUT KEPS #10-32 SST	3	3
13	9006082-3	PHL HD TRUSS #10-32 x 2¼	2	2
14	D-UA-H952-A-0	END PANEL H952-A	2	2
15	D-UA-MC71-A-0	4K BASIC MEMORY	1	1
16	9007033	TIE WRAP #SSC-2-B (PANDUIT)	A/R	A/R
17	9006724	WASH EXT TOOTH ¼	11	11
18	D-UA-KC09-C-0	CENTRAL PROCESSOR ASSY KC09-C	1	1
19	D-UA-KD09-C-0	I/O SECTION ASSY KD09-C	1	1
20	9006075-1	PHL HD PAN #10-32 x 3/4 SST	6	6
21	D-UA-H951-B-0	30" FULL DOOR ASSY	1	1

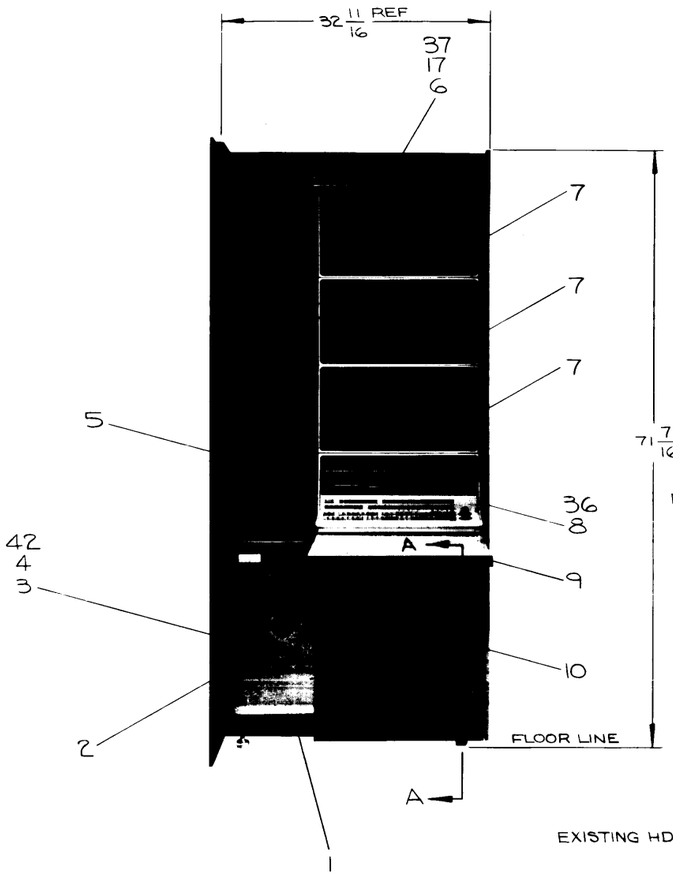
DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

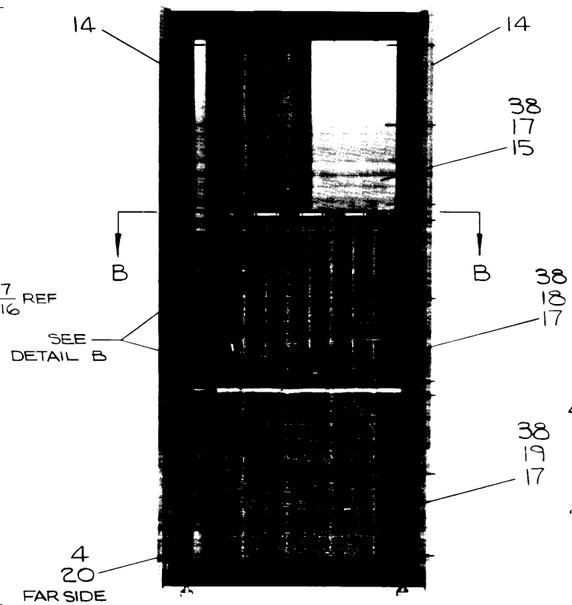
ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION 9-L	9-LA
22	9006056-1	PHL HD PAN ¼-20 x ½ SST	2	2
23	C-AD-7005968-0-0	CABLE SET 9L	1	1
24	C-MD-7406734-0-0	DUCT CABLE	1	1
25	D-MD-7406732-0-0	SUPPORT DUCT	1	1
26	D-IC-9-L-3	POWER WIRING 9L	1	1
27	9006902	TERM STRIP 4-541 CINCH JONES	1	1
28	9006026-1	PHL HD PAN 6-32 x 3/4 SST	4	4
29	9006560	NUT KEPS HEX #6-32 SST	2	2
30	9006851	SPACER ¼ AF x ½ #6-32 AL	2	2
31	B-MD-7404721-0-0	PROTECTION CONVER 541 (4 TERM)	1	1
32	9006020-1	PHL HD PAN #6-32 x ¼	2	2
33	9007032	TIE WRAP #SST-2-B (PANDUIT)	A/R	A/R
34	9006712	WASH .250 I.D.X.375 O.D.X.032THK	A/R	A/R
35	9107240	HELITUBE ¼ O.D.	A/R	A/R
36	9006071-2	PHL HD FLAT #10-32 x 3/8	4	4
37	9006065-1	SCR PHL HD PAN ¼-20 x 2¼ LG	2	2
38	9006062-1	SCR PHL HD PAN ¼-20 x 1½	9	9
39	9006079-3	SCR PHL HD TRUSS #10-32 x 1½	3	3
40	9006046-1	SCR PHL HD PAN #8-32 x 1-3/4 LG	2	2
41		SPACER 3/8 AF x 1-1/2 LG. - #10 HOLE	2	2
42	9007786	SPEED NUT 10-32 TINNERMAN	20	20
43	9006634	WASH INT TOOTH #8	2	2

LEGEND	
NUMBER	VARIATION
9-L	60 HZ
9-LA	50 HZ

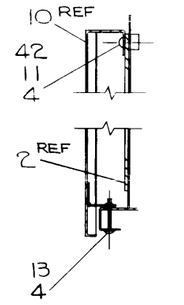
NOTES:

1. TO ASSEMBLE ITEMS NO. 15, 18 & 19 REMOVE EXISTING SCREWS HOLDING FAN HOUSING TO LOGIC. POSITION FAN HOUSING & LOGIC ON INSIDE OF PLENUM BRACKET. USE REMOVED HDW & ITEMS NO. 4, 17, 20 & 38 TO SECURE IN PLENUM AS SHOWN IN SECTION B-B
2. FOR DRAWING INDEX LIST SEE DWG NO. D-DI-9-L-1
3. FOR OPTIONAL EQUIP LAYOUT SEE DWG NO. D-AR-9-L-2
4. USE ITEM #12 & #39 FOR SHIPPING PURPOSES ONLY
5. TO ASSEMBLE ITEM #9 TO ITEM #1 REMOVE BOTTOM SCREW OF GUSSET PLATE. POSITION TABLE IN CAB. USE REMOVED HDW & ITEM #22 TO SECURE TO CABINET
6. FOR ADDITIONAL CABLE CONNECTIONS REFER TO DWG # D-1A-7005987-0-0 & D-1A-7005988-0-0

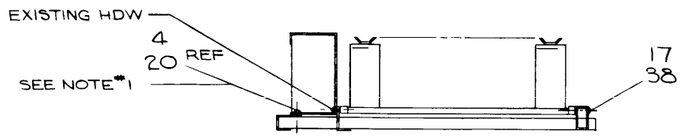




REAR VIEW DOOR REMOVED

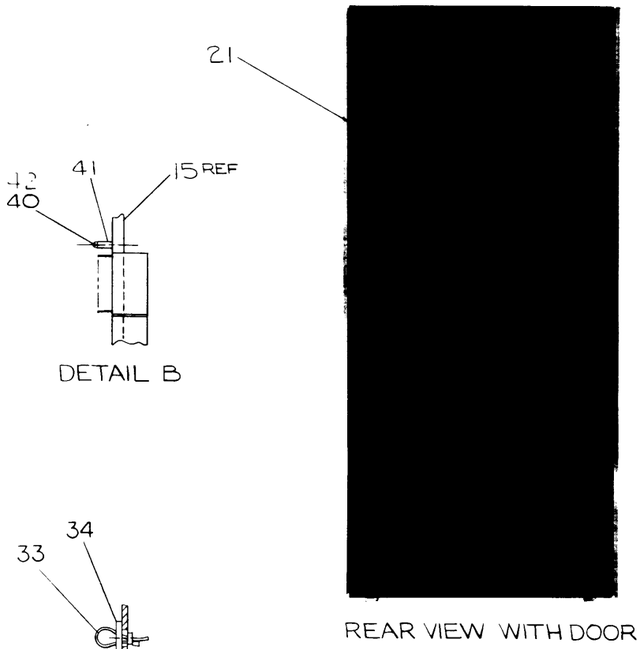


SECTION A-A



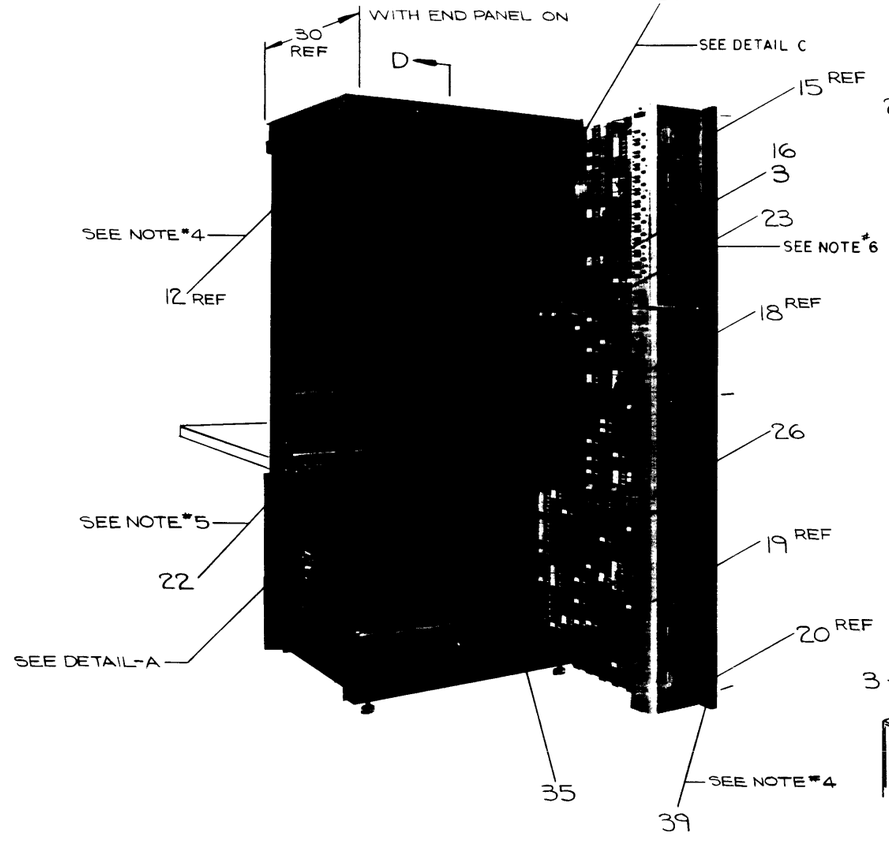
SECTION B-B
END PANELS & DOORS REMOVED

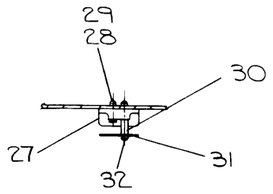
D-UA-9-L-0 PDP-9/L Assembly (Sheet 1)



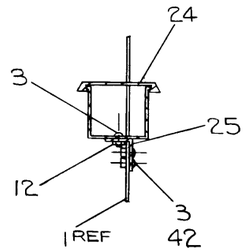
DETAIL B

DETAIL-C

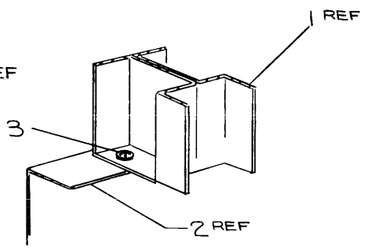




SECTION D-D



SECTION C-C



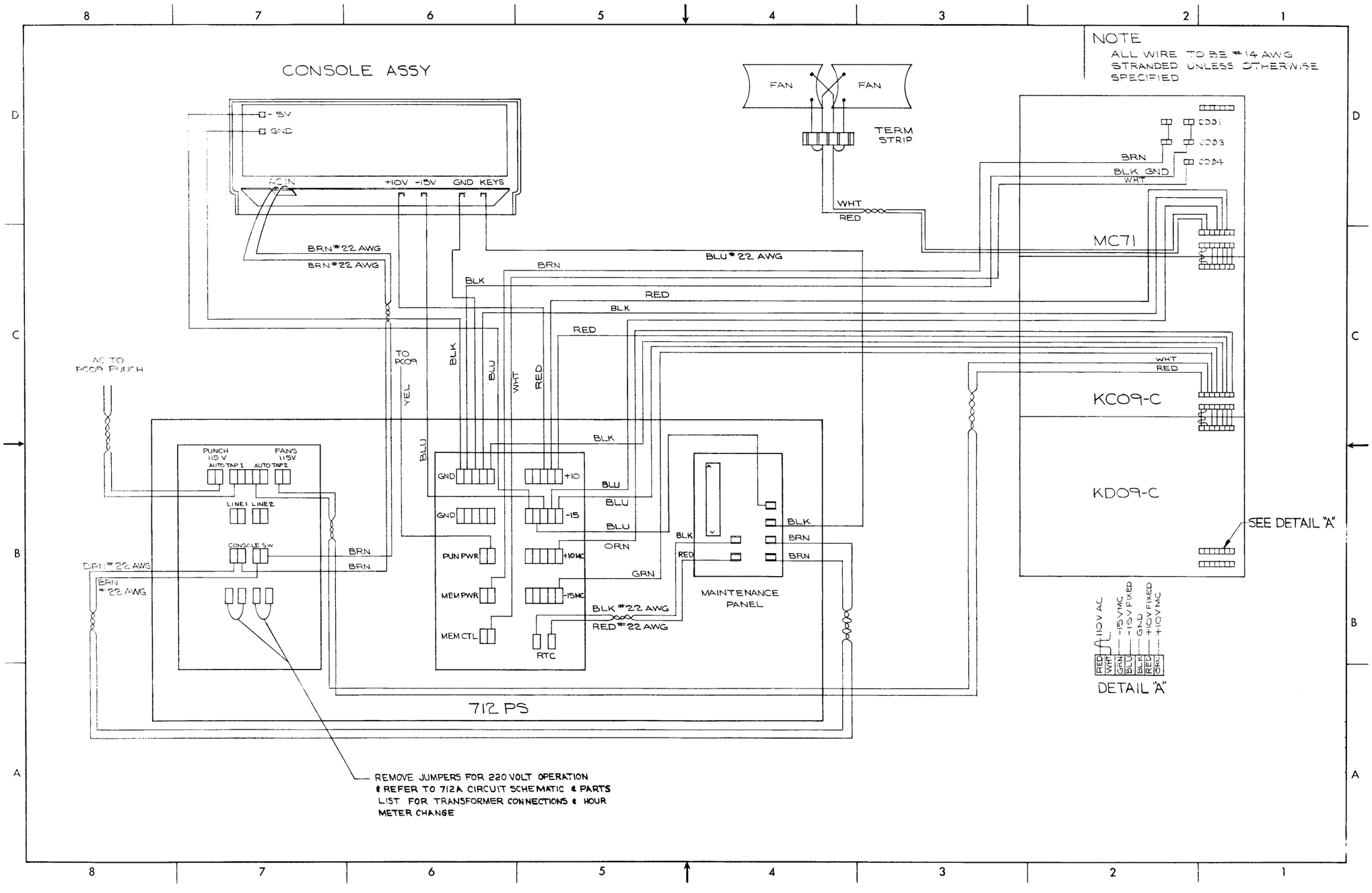
DETAIL-A

D-UA-9-L-0 PDP-9/L Assembly (Sheet 2)

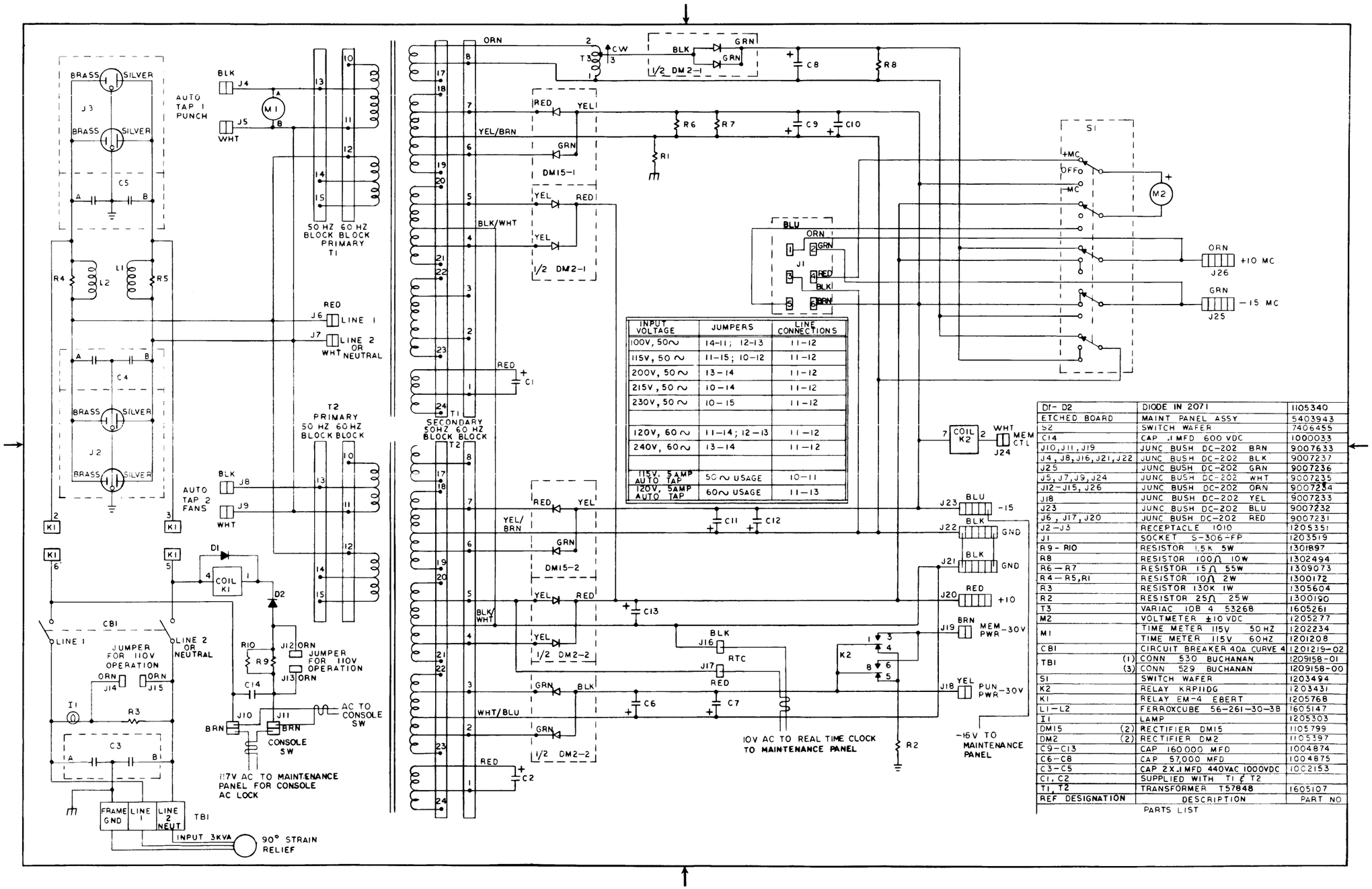
ITEM NO.	PART NO.	LENGTH	CONN TYPE	TO LOCATION	CONN TYPE	TO LOCATION	
1	7405552-5	6	WØ31	CPD4Ø	WØ31	IO DØ1	
↑	↑	↑	↑	CPD39	↑	IO DØ9	
↑	↑	↑	↑	CPE4Ø	↑	IO EØ1	
↑	↑	↑	↑	CPE39	↑	IO EØ2	
↑	↑	↑	↑	CP F4Ø	↑	IO FØ1	
↑	↑	↑	↑	CP F39	↑	IO FØ2	
↑	↑	↑	↑	CP F38	↑	IO FØ3	
↓	↓	↓	↓	CP H4Ø	↓	IO HØ1	
1	7405552-5		WØ31	CP H39	WØ31	IO HØ2	
2	7405554-15		WØ34	CP J4Ø	WØ34	IO JØ1	
2	7405554-15	↓	WØ34	CP J39	WØ34	IO JØ2	
1	7405552-5	6	WØ31	CP J38	WØ31	IO JØ3	
3	7405553-15	49	WØ33	712 PS	WØ33	IO AØ6	
4	7405553-16	61	WØ33	READER	WØ33	IO A17	} OPTIONAL
4	7405553-16	61	WØ33	PUNCH	WØ33	IO A21	}

QTY.	DESCRIPTION	PART NO.	ITEM NO.
2	WØ33 TO WØ33 CABLE (61")	C-1A-7405553-16-0	4
1	WØ33 TO WØ33 CABLE (49")	C-1A-7405553-15-0	3
2	WØ34 TO WØ34 CABLE (6')	C-1A-7405554-15-0	2
10	WØ31 TO WØ31 CABLE (6")	C-1A-7405552-5-0	1

PARTS LIST



D-IC-9-L-3 Power Wiring

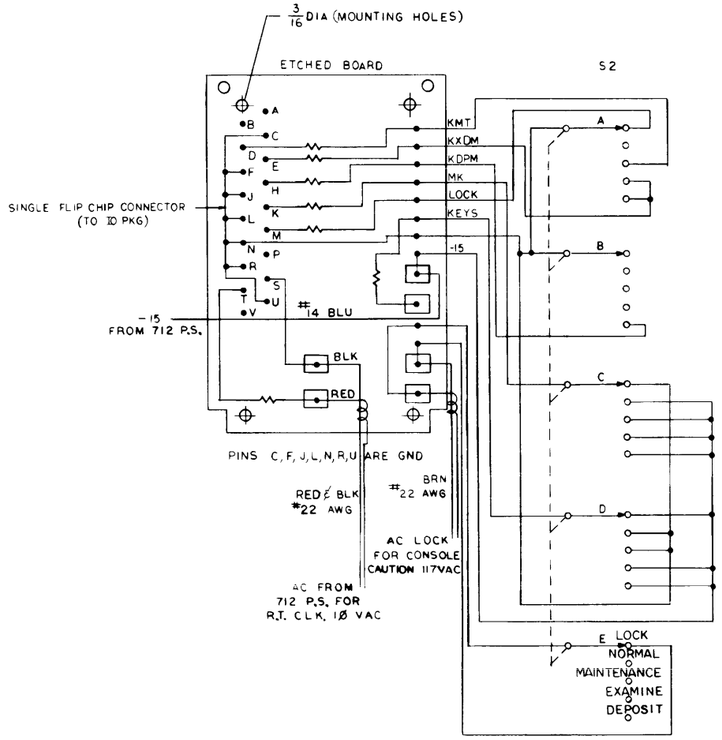


INPUT VOLTAGE	JUMPERS	LINE CONNECTIONS
100V, 50~	14-11; 12-13	11-12
115V, 50 ~	11-15; 10-12	11-12
200V, 50 ~	13-14	11-12
215V, 50 ~	10-14	11-12
230V, 50 ~	10-15	11-12
120V, 60 ~	11-14; 12-13	11-12
240V, 60 ~	13-14	11-12
115V, 5 AMP AUTO TAP	50 ~ USAGE	10-11
120V, 5AMP AUTO TAP	60~ USAGE	11-13

REF DESIGNATION		DESCRIPTION	PART NO
D1- D2		DIODE IN 2071	1105340
ETCHED BOARD		MAINT PANEL ASSY	5403943
S2		SWITCH WAFER	7406455
C14		CAP .1 MFD 600 VDC	1000033
J10, J11, J19		JUNC BUSH DC-202 BRN	9007633
J4, J8, J16, J21, J22		JUNC BUSH DC-202 BLK	9007237
J25		JUNC BUSH DC-202 GRN	9007236
J5, J7, J9, J24		JUNC BUSH DC-202 WHT	9007235
J12-J15, J26		JUNC BUSH DC-202 ORN	9007234
J18		JUNC BUSH DC-202 YEL	9007233
J23		JUNC BUSH DC-202 BLU	9007232
J6, J17, J20		JUNC BUSH DC-202 RED	9007231
J2-J3		RECEPTACLE 1010	1205351
J1		SOCKET S-306-FP	1203519
R9 - R10		RESISTOR 1.5K 5W	1301897
R8		RESISTOR 100Ω 10W	1302494
R6 — R7		RESISTOR 15Ω 55W	1309073
R4 — R5, R1		RESISTOR 10Ω 2W	1300172
R3		RESISTOR 130K 1W	1305604
R2		RESISTOR 25Ω 25W	1300190
T3		VARIAC 10B 4 53268	1605261
M2		VOLTMETER ±10 VDC	1205277
M1		TIME METER 115V 50 HZ	1202234
		TIME METER 115V 60HZ	1201208
CB1		CIRCUIT BREAKER 40A CURVE 4	1201215-02
TB1	(1)	CONN 530 BUCHANAN	1209158-01
	(3)	CONN 529 BUCHANAN	1209158-00
S1		SWITCH WAFER	1203494
K2		RELAY KRP11DG	1203431
K1		RELAY EM-4 EBERT	1205768
L1-L2		FERROXCUBE 56-261-30-3B	1605147
I1		LAMP	1205303
DM15	(2)	RECTIFIER DM15	1105799
DM2	(2)	RECTIFIER DM2	1105397
C9-C13		CAP 160,000 MFD	1004874
C6-C8		CAP 57,000 MFD	1004875
C3-C5		CAP 2X.1MFD 440VAC 1000VDC	1002153
C1, C2		SUPPLIED WITH T1 & T2	
T1, T2		TRANSFORMER T57848	1605107

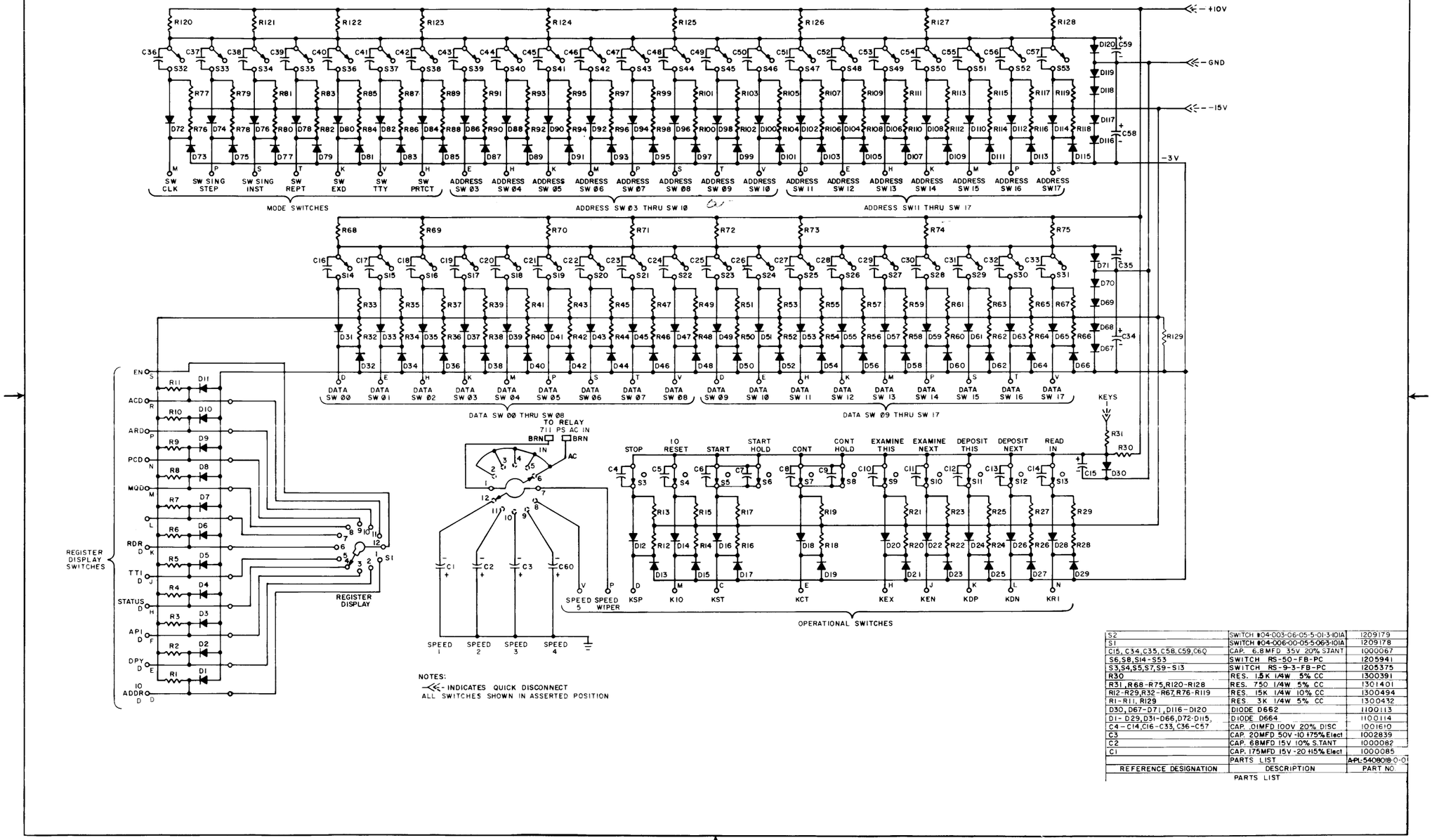
PARTS LIST

D-IC-712-0-1 Power Supply 712 (Sheet 1)



UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 1/2W 10%
CERAMIC CAPS ARE .01 MFD DISK, SPRAGUE
WIRING IS #22 GAUGE (STRANDED)

D-IC-712-0-1 Power Supply 712 (Sheet 2)

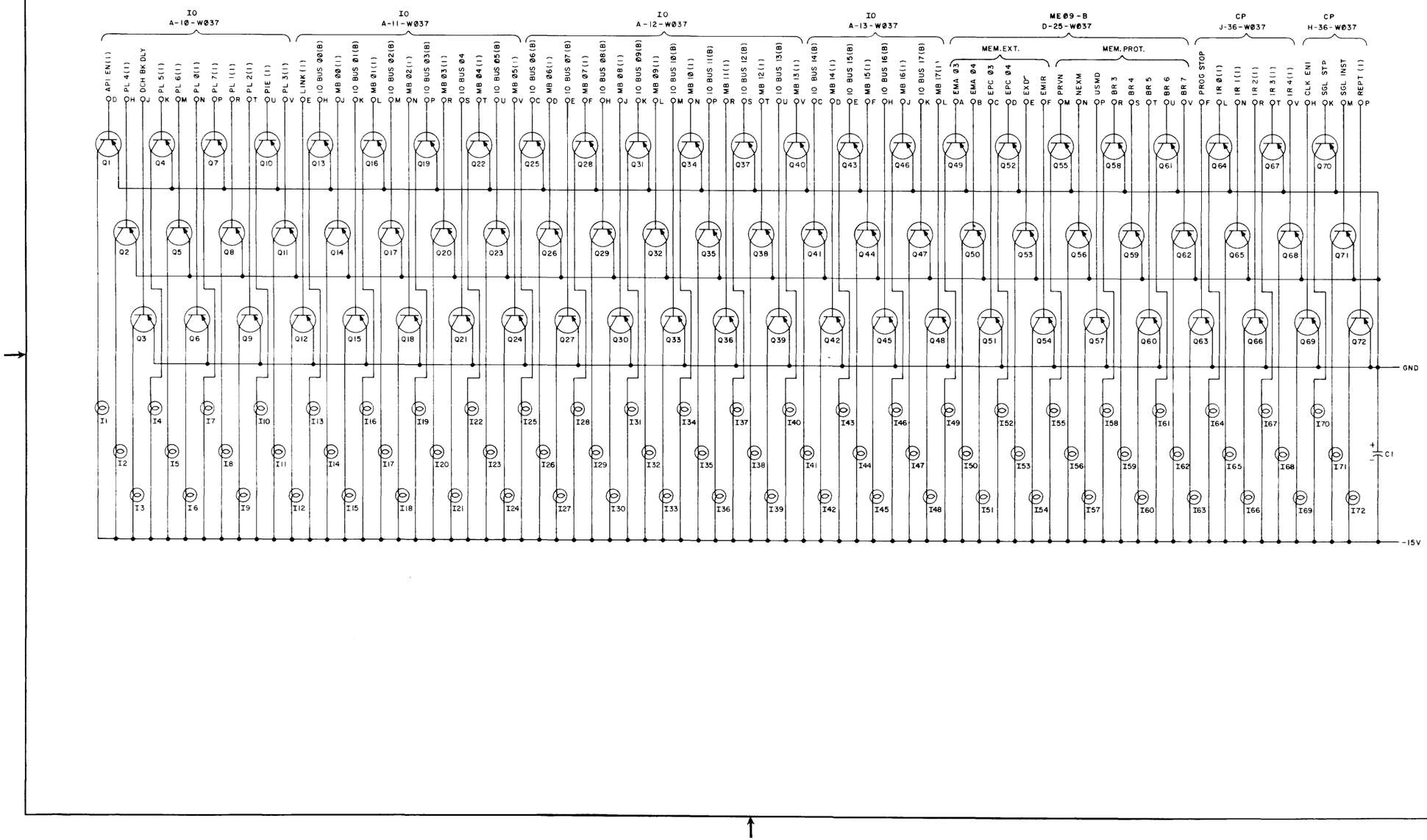


NOTES:
-<<- INDICATES QUICK DISCONNECT
ALL SWITCHES SHOWN IN ASSERTED POSITION

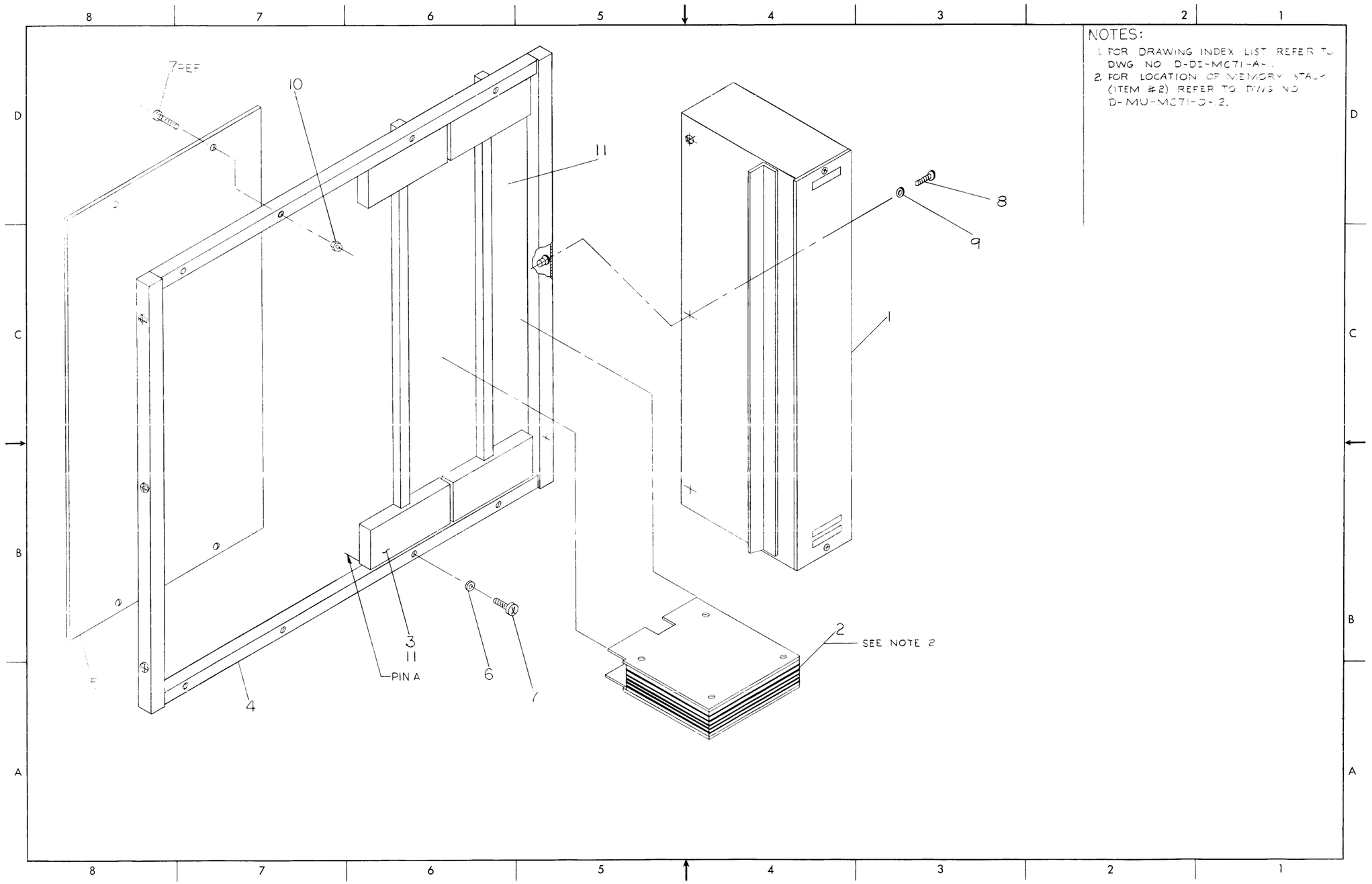
S2	SWITCH #04-003-06-05-5-01-3-101A	1209179
S1	SWITCH #04-006-00-05-5-063-101A	1209178
C15, C34, C35, C58, C59, C60	CAP. 6.8MFD 35V 20% STANT	1000067
S6, S8, S14 - S53	SWITCH RS-50-FB-PC	1205941
S3, S4, S5, S7, S9 - S13	SWITCH RS-9-3-FB-PC	1205375
R30	RES. 1.5K 1/4W 5% CC	1300391
R31, R68 - R75, R120 - R128	RES. 750 1/4W 5% CC	1301401
R12 - R29, R32 - R67, R76 - R119	RES. 15K 1/4W 10% CC	1300494
R1 - R11, R129	RES. 3K 1/4W 5% CC	1300432
D30, D67 - D71, D116 - D120	DIODE D662	1100113
D1 - D29, D31 - D66, D72 - D115,	DIODE D664	1100114
C4 - C14, C16 - C33, C36 - C57	CAP. .01MFD 100V 20% DISC	1001610
C3	CAP. 20MFD 50V -10 175% Elect	1002839
C2	CAP. 68MFD 15V 10% S.TANT	1000082
C1	CAP. 175MFD 15V -20 115% Elect	1000085
	PARTS LIST	~~A-PL-5408018-0-01~~
REFERENCE DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

D-CS-5408018-0-1 PDP-9/L Console Switch Board



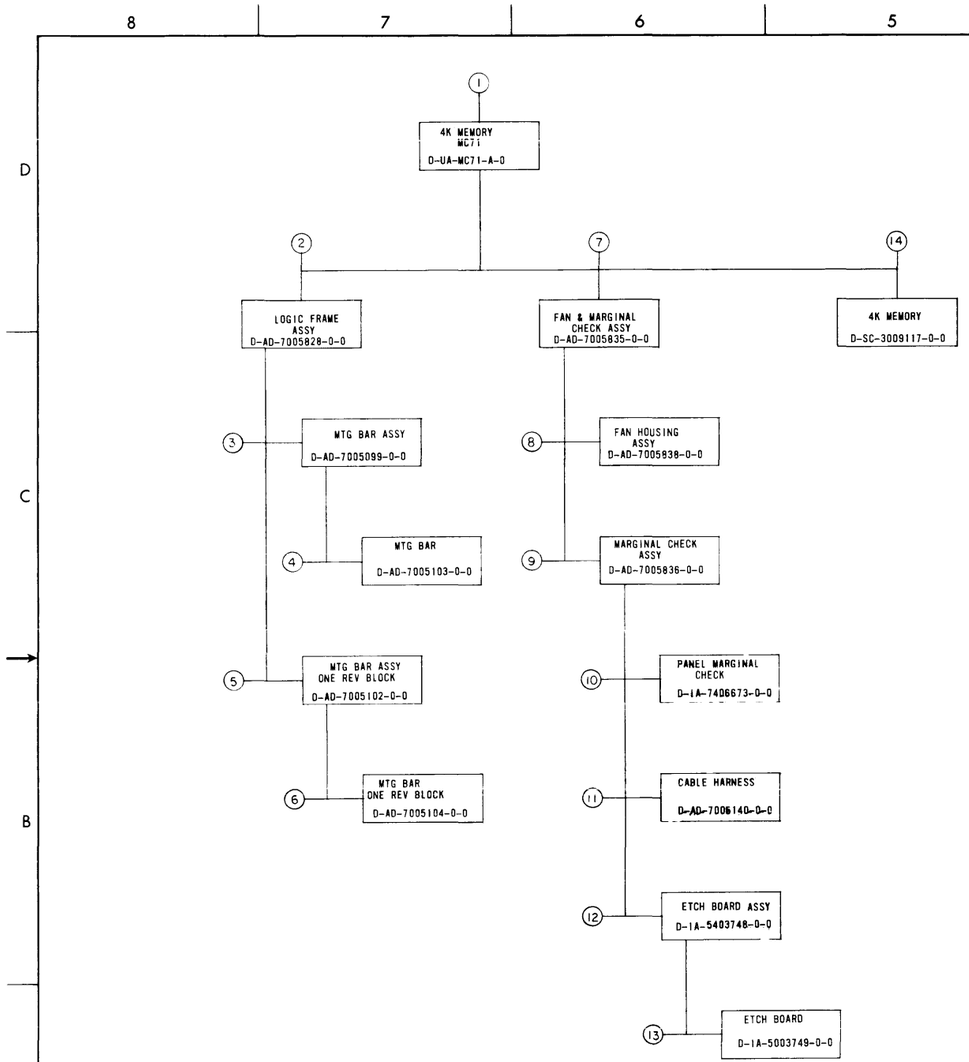
D-CS-5408020-0-1 PDP-9/L Console Light Board


NOTES:
1. FOR DRAWING INDEX LIST REFER TO DWG NO D-DI-MC71-A-0.
2. FOR LOCATION OF MEMORY STACK (ITEM #2) REFER TO DWG NO D-MU-MC71-0-2.
REF
10
11
8
9
1
2
SEE NOTE 2
3
11
PIN A
4
6
7
5

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

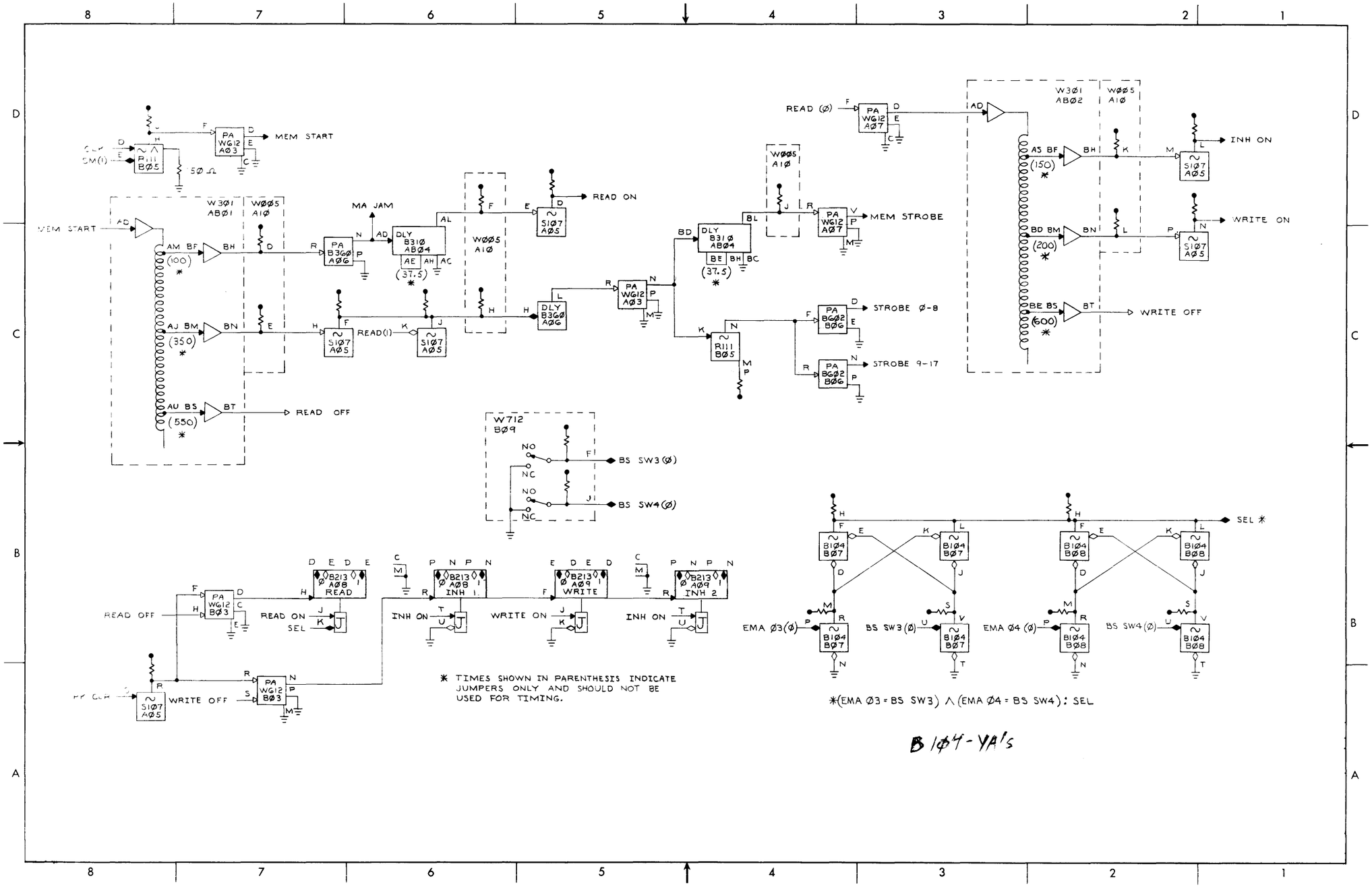
PARTS LIST

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION
1	D-AD-7005835-0-0	FAN & MARGINAL CHECK ASSY	1
2	D-SC-3009117-0-0	MEMORY STACK 4K	1
3	D-AD-7005828-0-0	LOGIC FRAME ASSY	1
4	E-IA-7405034-0-0	DOOR FRAME	1
5	D-MD-7406660-0-0	FILLER,LOGIC	1
6	9006634	WASHER INT TOOTH #8	4
7	9006043-1	SCR PH HD PAN #8-32 x 1"	8
8	9006058-1	SCR PH HD PAN #¼-20 x 3/4	1
9	9006637	WASHER INT TOOTH #¼-20	1
10	9006563	NUT KEPS #8-32	4
11	B-AD-7005900-0-0	CABLE SET MC71-A	1
	D-MU-MC71-0-12	MODULE UTILIZATION	REF

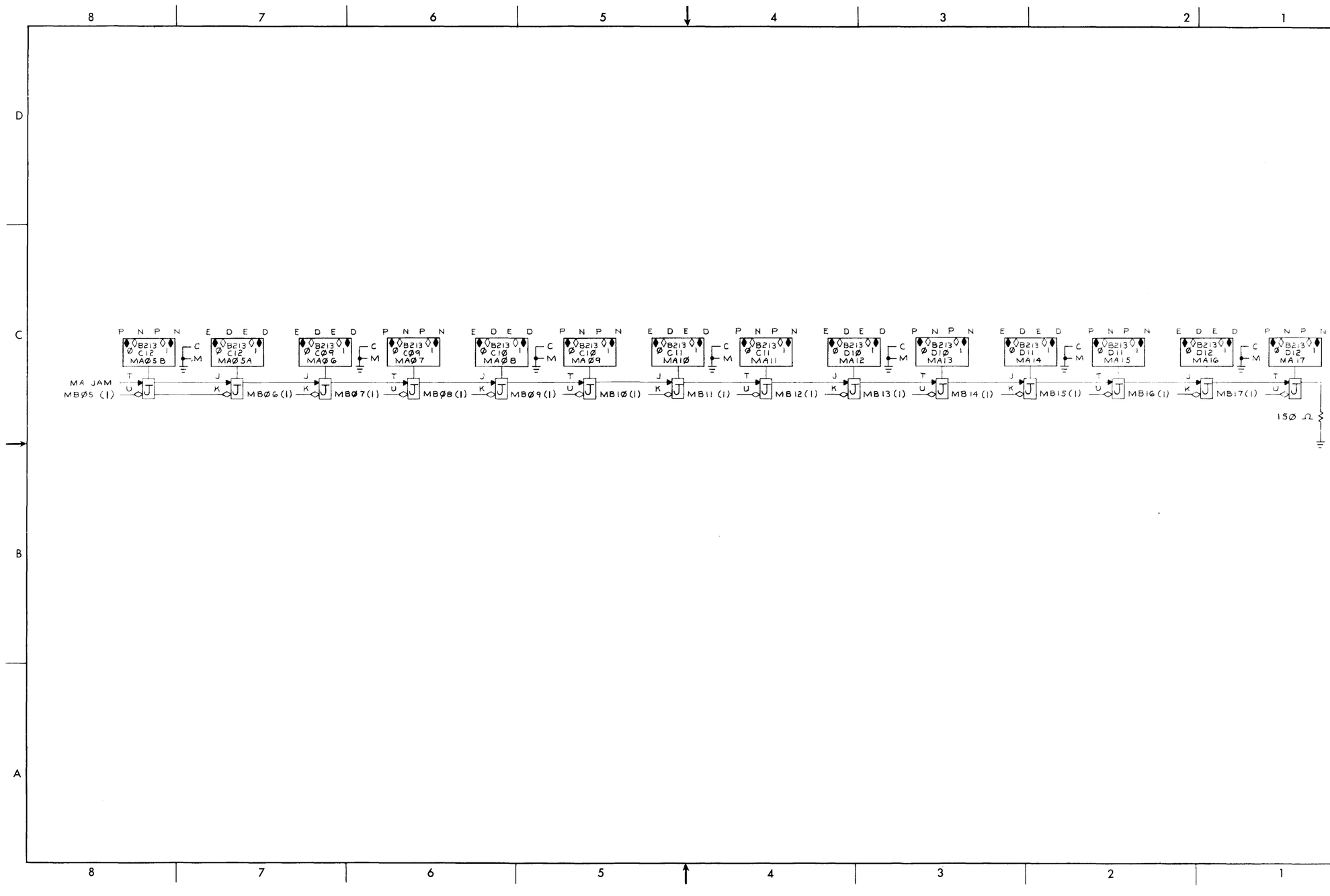


FIND NO.	DESCRIPTION	PART NO.	DEPT. USAGE PROD	CUST	F/C
1.	4K BASIC MEMORY	D-UA-MC71-A-0			
	4K BASIC MEMORY (PL)	A-PL-MC71-A-0			
	FILLER LOGIC	D-MD-7406660-0-0			
	DOOR FRAME	C-1A-7405034-0-0			
	DOOR FRAME (PL)	A-PL-7405634-0-0			
	CABLE SET MC71-A	B-AD-7005900-0-0			
	CABLE SET MC71-A (PL)	A-PL-7005900-0-0			
2.	LOGIC FRAME ASSY	D-AD-7005828-0-0			
	LOGIC FRAME ASSY (PL)	A-PL-7005828-0-0			
3.	MTG BAR ASSY (IO BLOCK)	D-AD-7005099-0-0			
	MTG BAR ASSY (PL)	A-PL-7005099-0-0			
4.	MTG BAR STD	D-AD-7005103-0-0			
	MTG BAR	C-MD-7405035-0-0			
5.	MTG BAR ASSY (ONE REV)	D-AD-7005102-0-0			
	MTG BAR ASSY (PL)	A-PL-7005102-0-0			
6.	MTG BAR REV	D-AD-7005104-0-0			
	MTG BAR	C-MD-7405035-0-0			
7.	FAN & MARGINAL CHECK ASSY	D-AD-7005835-0-0			
	FAN & MARGINAL CHECK ASSY (PL)	A-PL-7005835-0-0			
8.	FAN HOUSING ASSY	D-AD-7005838-0-0			
	FAN HOUSING ASSY (PL)	A-PL-7005838-0-0			
	TERMINAL STRIP	C-1A-7405083-0-0			
	CHASSIS FAN HOUSING	E-1A-7406682-0-0			
	AIR BAFFLE	D-MD-7406674-0-0			
9.	MARGINAL CHECK ASSY	D-AD-7005836-0-0			
	MARGINAL CHECK ASSY (PL)	A-PL-7005836-0-0			
	TERM TAB BUSSING WIRE (GRN)	C-MD-7405089-1-0			
	TERM TAB BUSSING WIRE (BLU)	C-MD-7405089-2-0			
	TERM TAB BUSSING WIRE (BLK)	C-MD-7405089-3-0			
	TERM TAB BUSSING WIRE (RED)	C-MD-7405089-4-0			
	TERM TAB BUSSING WIRE (ORN)	C-MD-7405089-5-0			
	AC BUSSING TO FAN	B-MD-7405091-0-0			
	TERM TAB BUSSING WIRE (GRN)	C-MD-7405379-1-0			
	TERM TAB BUSSING WIRE (BLU)	C-MD-7405379-2-0			
	TERM TAB BUSSING WIRE (BLK)	C-MD-7405379-3-0			
	TERM TAB BUSSING WIRE (RED)	C-MD-7405379-4-0			
	TERM TAB BUSSING WIRE (ORN)	C-MD-7405379-5-0			
	AC BUSSING TO FAN	B-MD-7405090-0-0			
10.	PANEL MARGINAL CHECK	D-1A-7406673-0-0			
	SILK, SCREEN	C-SS-7406673-0-1			
11.	CABLE HARNESS	D-AD-7005140-0-0			
	CABLE CONNECTOR	W071			
12	ETCH BOARD ASSY	D-1A-5403748-0-0			
13.	ETCH BOARD	D-1A-5003749-0-0			
	PC LAYOUT	PC-5403748-0-1			
	BOARD GLASS EPOXY	1405110-0-0			
14.	4K MEMORY	D-SC-3009117-0-0			
	A DIODE BOARD	G610			
	B DIODE BOARD	G611			
	BLANK BOARD	W990			

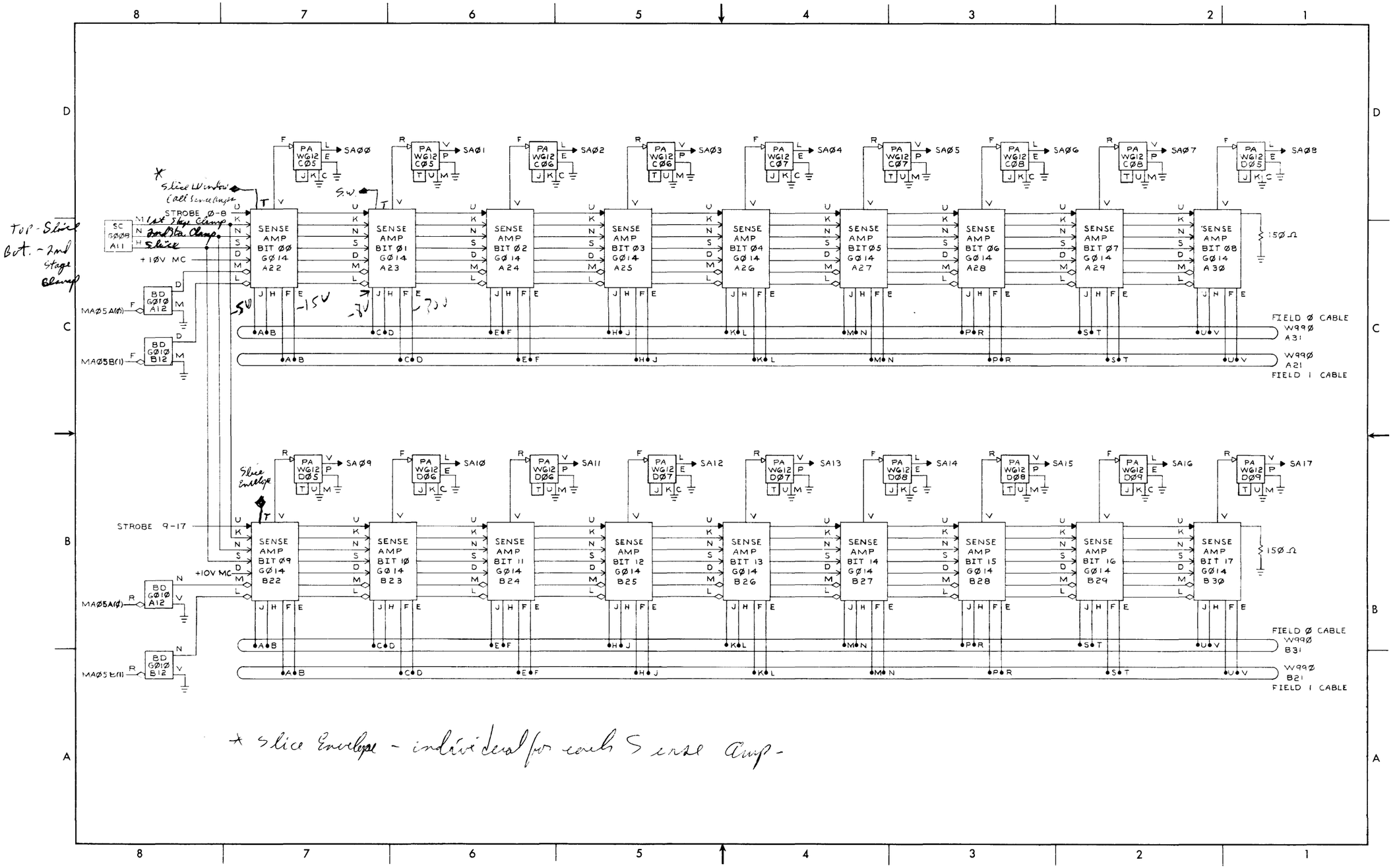
FIND NO.	DESCRIPTION	PART NO.	DEPT. USAGE PROD	CUST	F/C
1.	4K BASIC MEMORY	A-ML-MC71-A			
	MEMORY CONTROL	D-BS-MC71-0-1			
	MA FLIP FLOPS	D-BS-MC71-0-2			
	SENSE AMPS & PA'S	D-BS-MC71-0-3			
	FILED 0 INH DRIVERS	D-BS-MC71-0-4			
	FILED 1 INH DRIVERS	D-BS-MC71-0-5			
	FLD 0 X AXIS	D-BS-MC71-0-6			
	FLD 0 Y AXIS	D-BS-MC71-0-7			
	FLD 1 X AXIS	D-BS-MC71-0-8			
	FLD 1 Y AXIS	D-BS-MC71-0-9			
	VOLT REG & X-Y DRIVE	D-BS-MC71-0-10			
	MEM - CP INTERFACE	D-IC-MC71-0-11			
	MODULE UTILIZATION MC71	D-WL-MC71-0-12			
	MODULE UTILIZATION MC71	A-PL-MC71-0-12			
	TIMING DIAGRAM MC71	D-TD-MC71-0-13			
	MC SWITCH CONFIGURATION	D-SP-MC71-0-15			
	WIRE LIST MC71	K-WL-MC71-0-16			
	EXTERNAL COMP. LIST	A-CP-MC71-0-17			
2.	LOGIC FRAME ASSY	D-AD-7005828-0-0			
	LOGIC FRAME ASSY (PL)	A-PL-7005929-0-0			
7.	FAN & MARGINAL CHECK ASSY	D-AD-7005835-0-0			
8.	FAN HOUSING ASSY	D-AD-7005838-0-0			
9.	MARGINAL CHECK ASSY	D-AD-7005836-0-0			
11.	CABLE HARNESS	D-AD-7005140-0-0			
13.	PC LAYOUT	PC-5403748-0-1			
14.	4K MEMORY STACK	D-CS-3009117-0-1			
	4K MEMORY STACK	D-CS-3009117-0-2			
	4K MEMORY STACK	D-CS-3009117-0-3			



D-BS-MC71-0-1 Memory Control



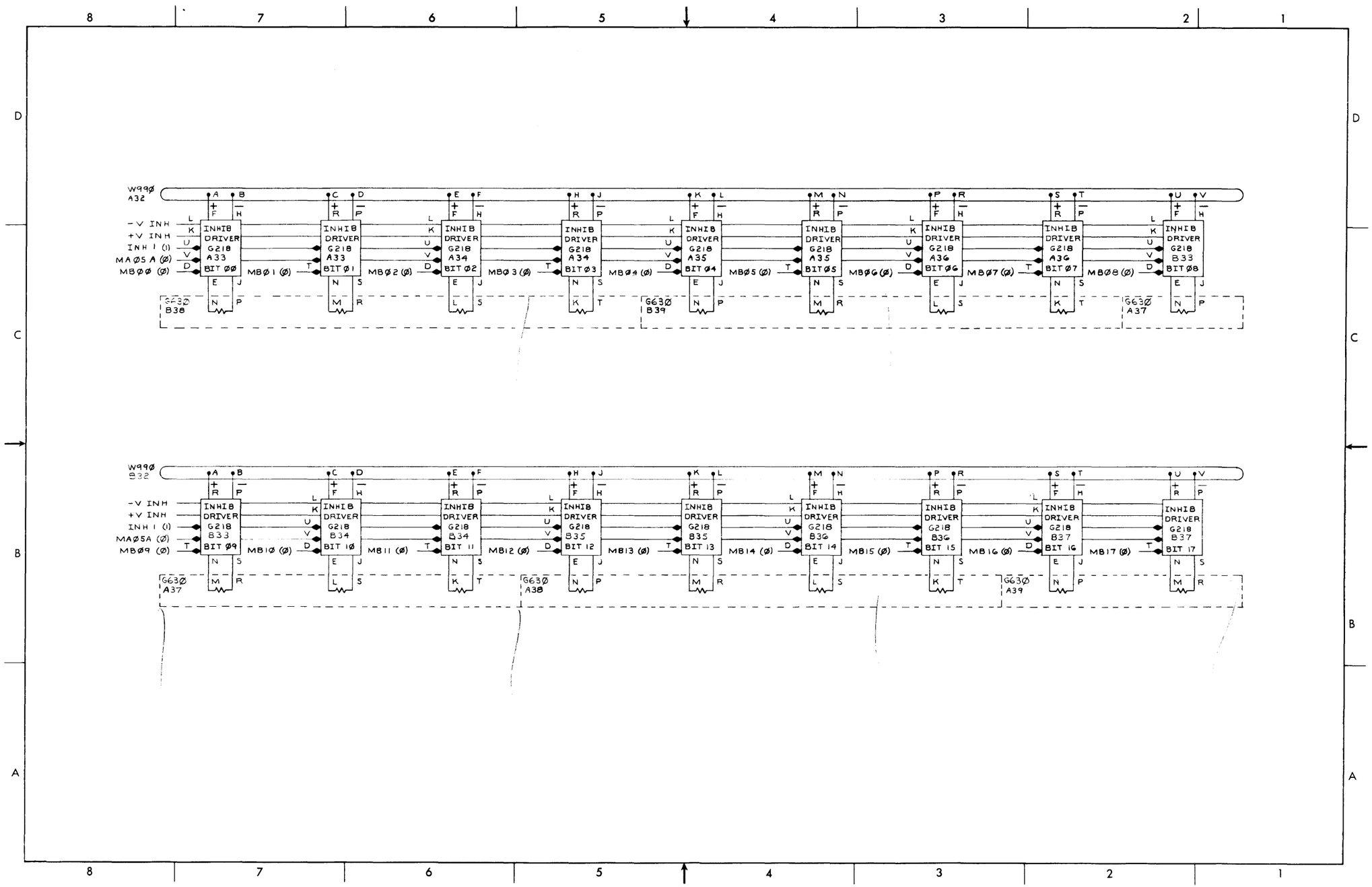
D-BS-MC71-0-2 MA Flip-Flops



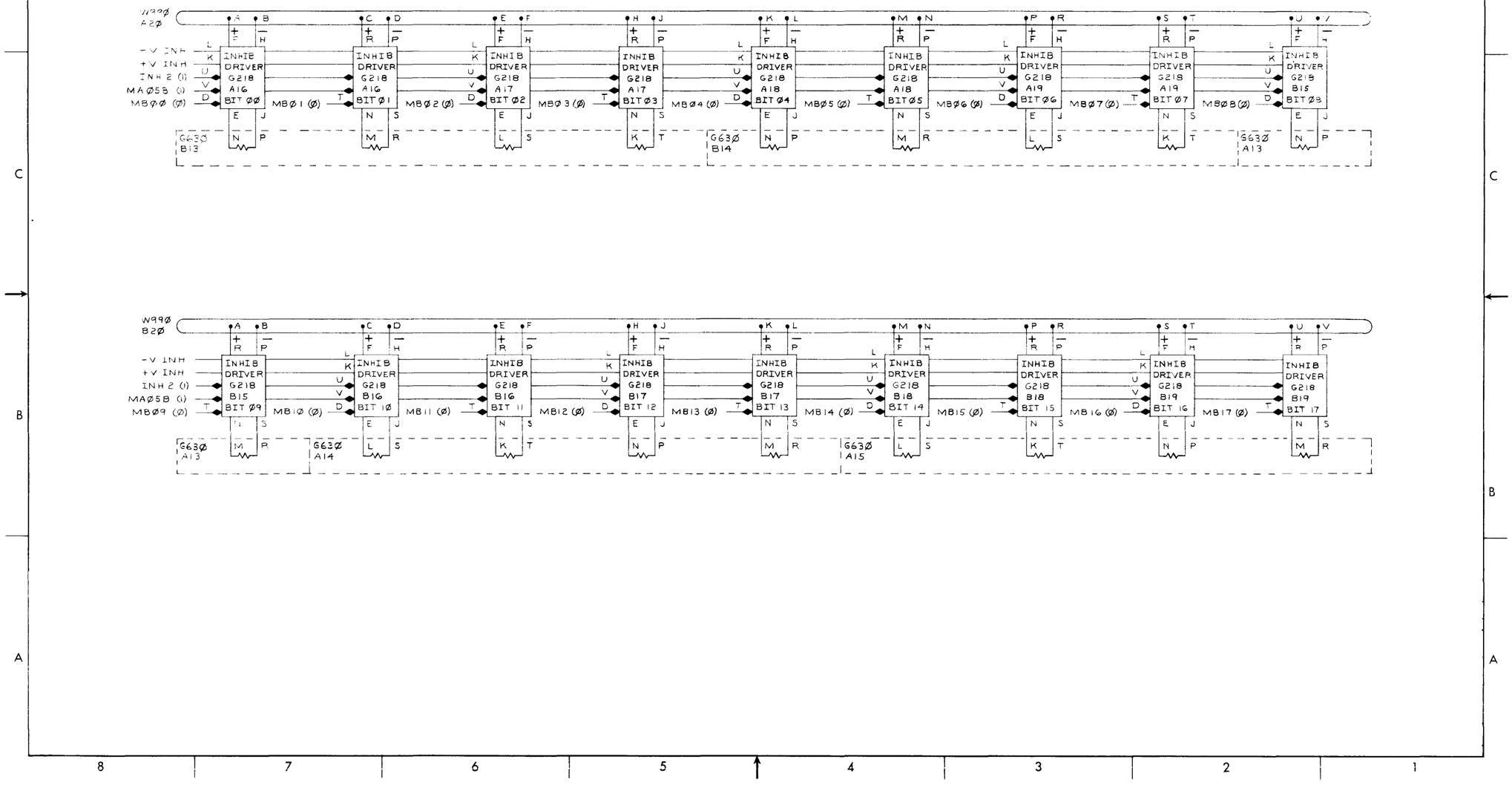
Top - Slice
Bot. - 2nd Stage Clamp

* Slice Envelope - individual for each Sense Amp -

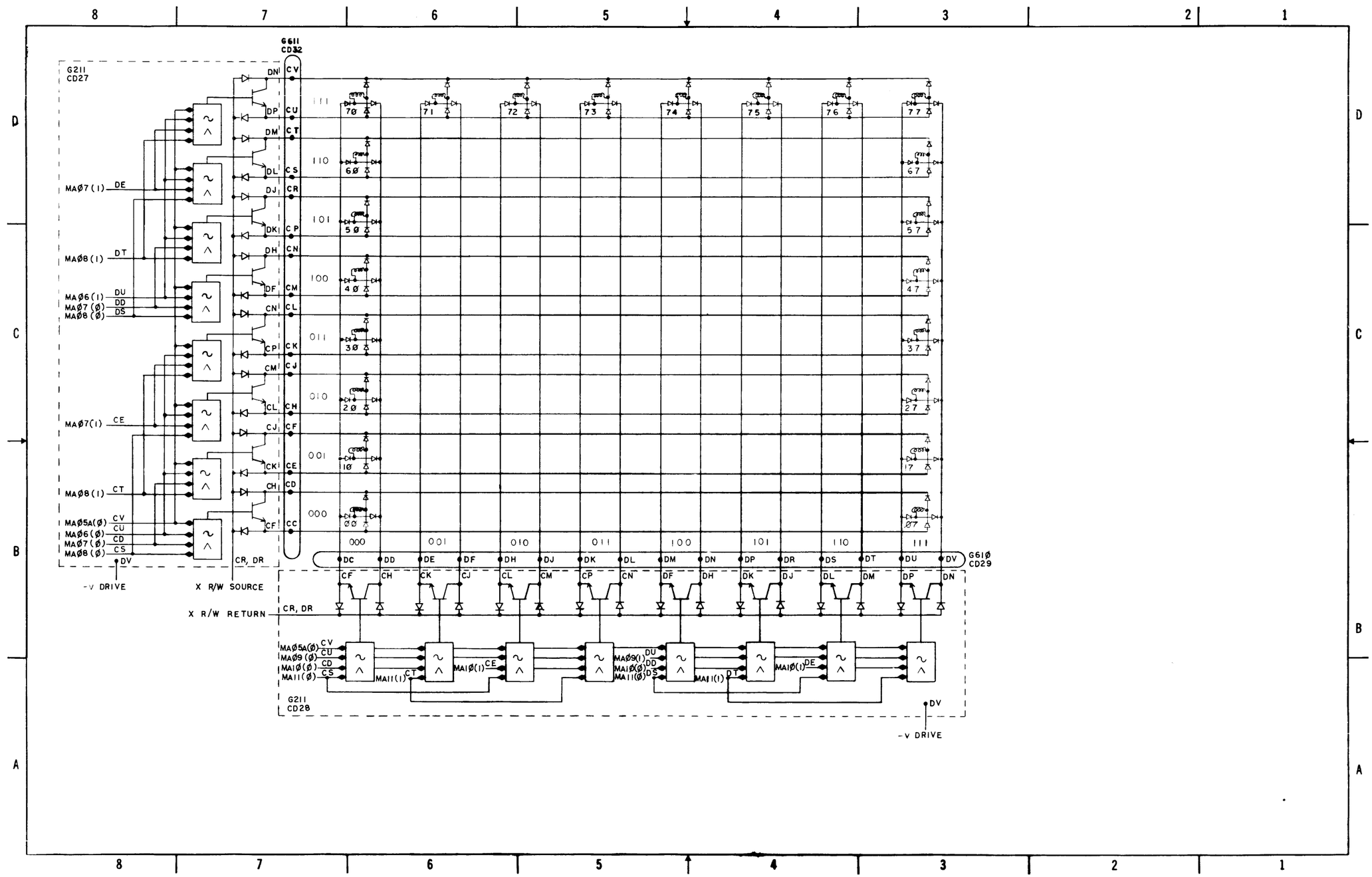
D-BS-MC71-0-3 Sense Amps and PA's



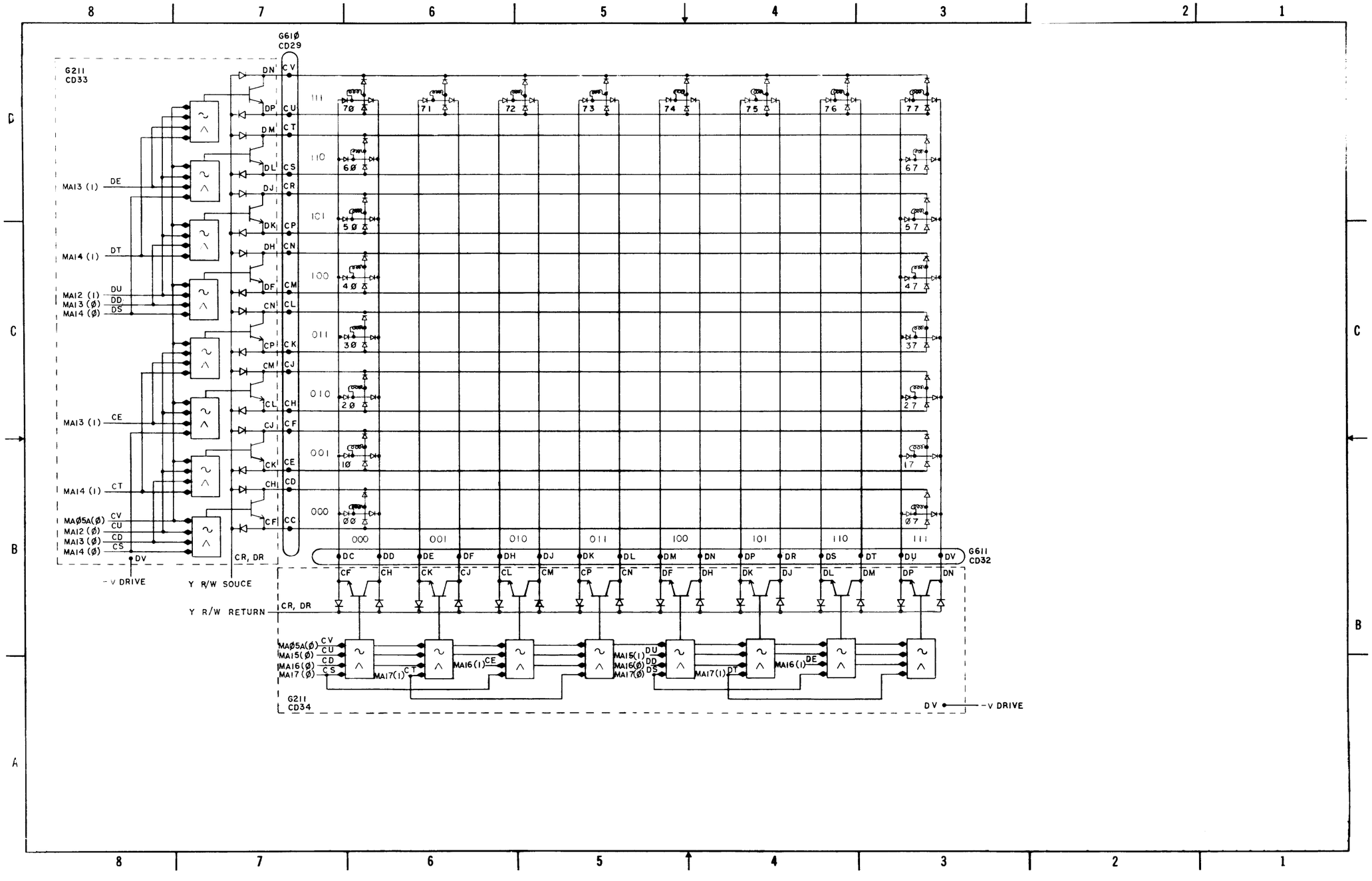
D-BS-MC71-0-4 Inhibit Drivers Field 0



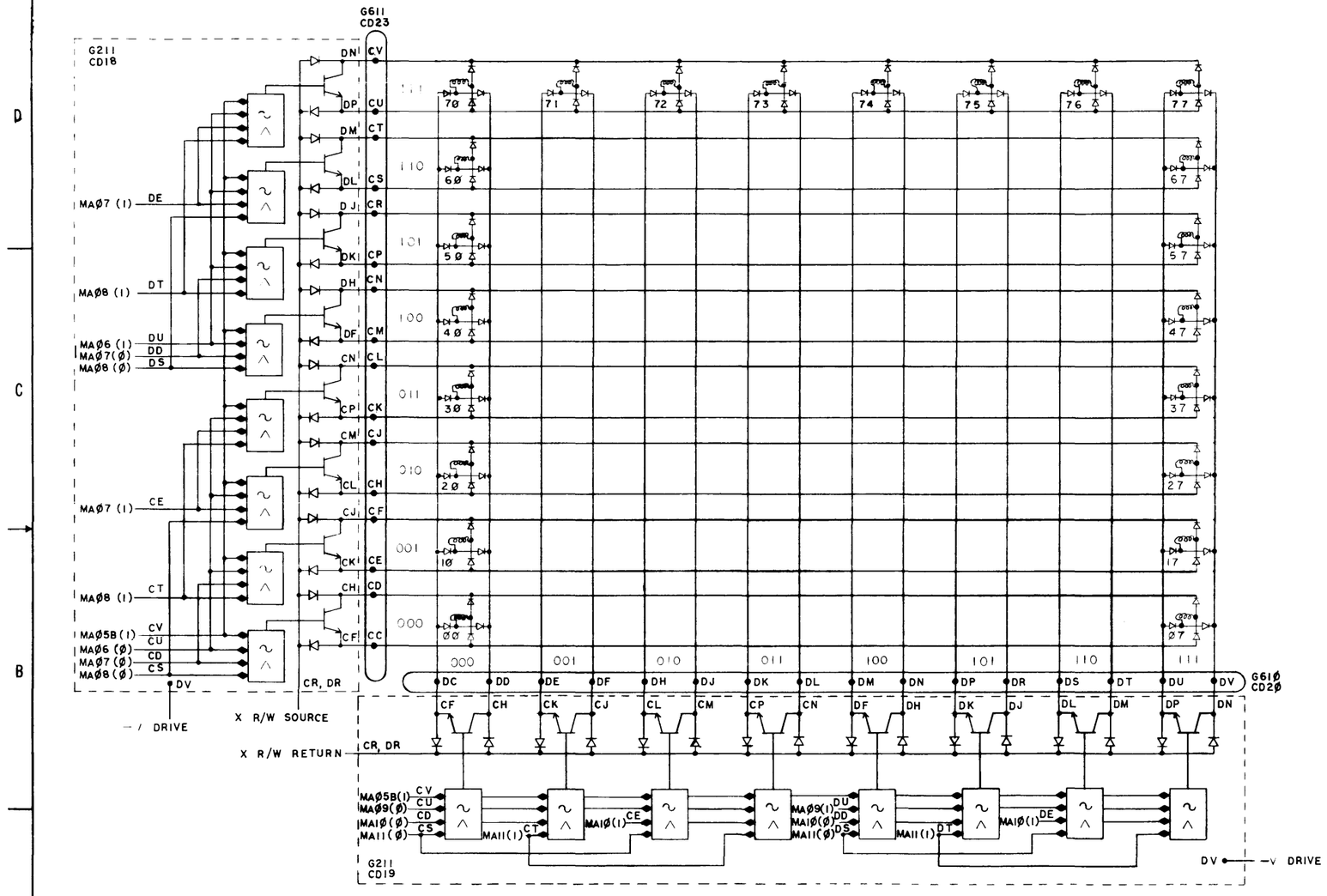
D-BS-MC71-0-5 Inhibit Drivers Field 1



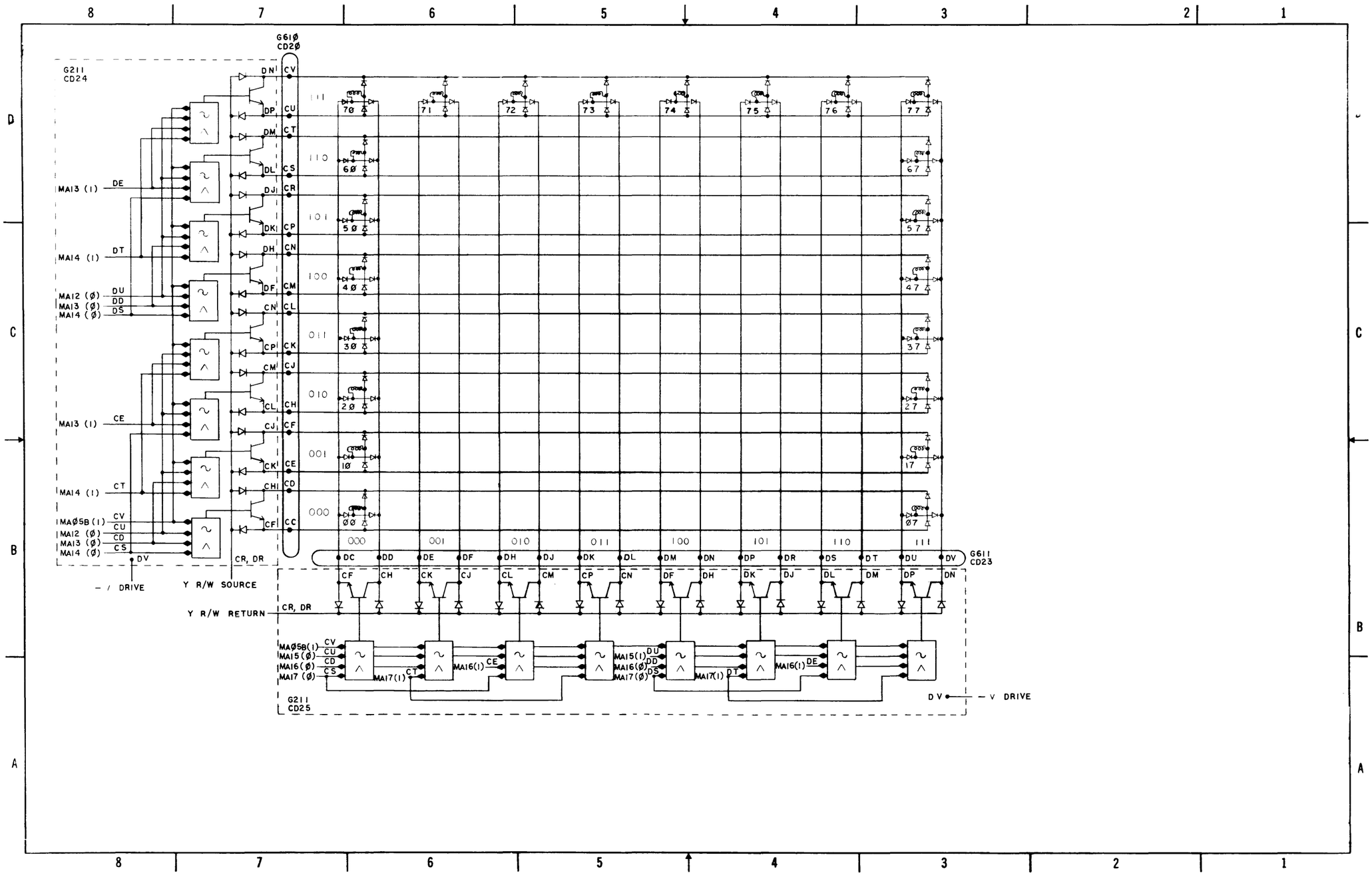
D-BS-MC71-0-6 X Axis Field 0



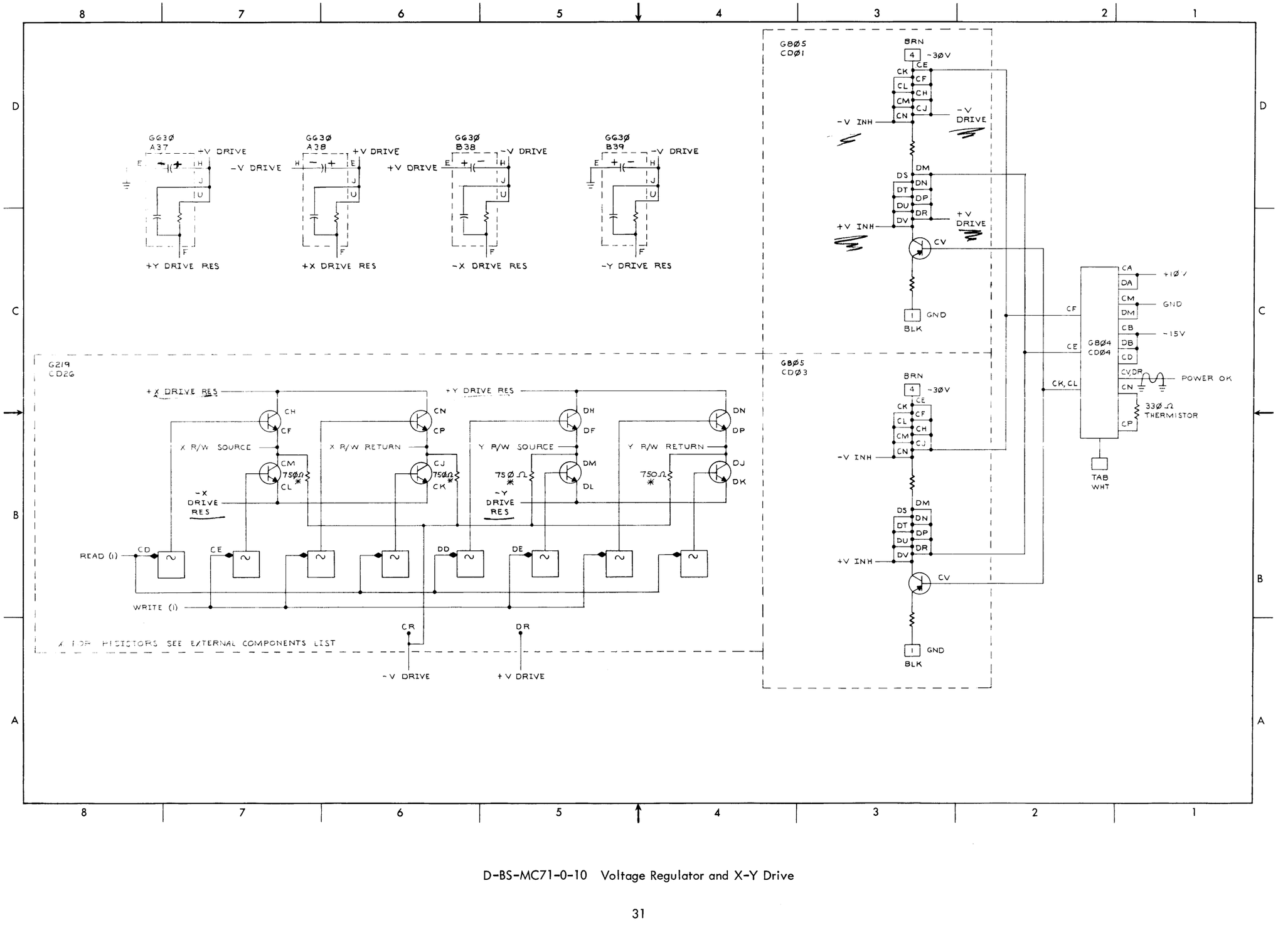
D-BS-MC71-0-7 Y Axis Field 0



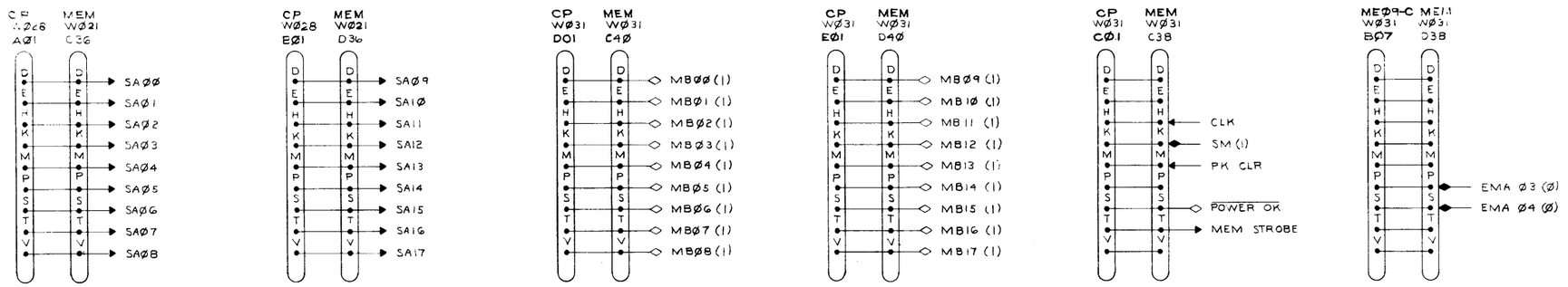
D-BS-MC71-0-8 X Axis Field 1



D-BS-MC71-0-9 Y Axis Field 1

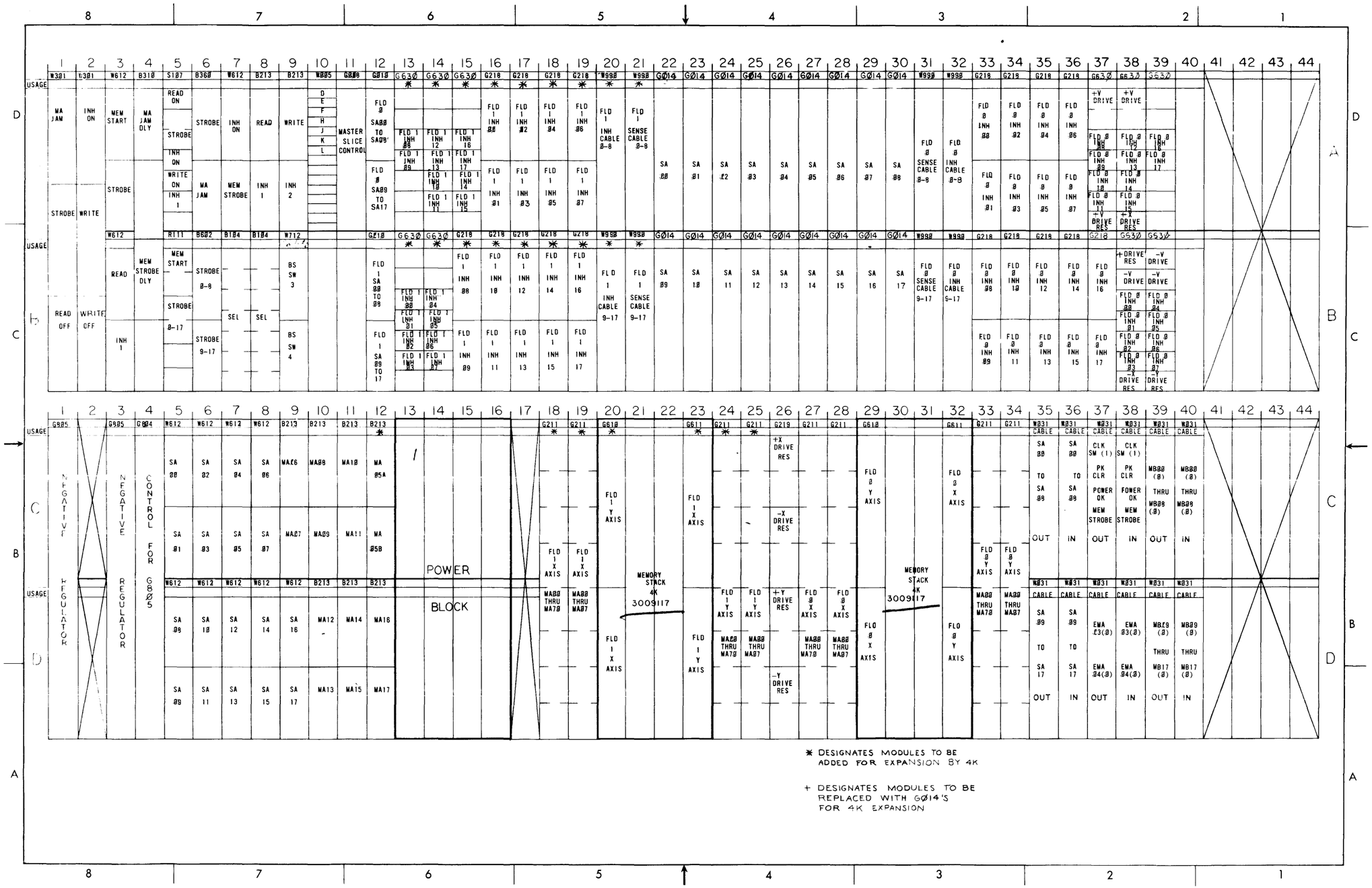


D-BS-MC71-0-10 Voltage Regulator and X-Y Drive



GND PINS C, F, J, L, N, R, U ON ALL WØ31 CONNECTORS

D-IC-MC71-0-11 Memory - CP Interface



D-MU-MC71-0-12 Module Utilization

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

ITEM NO.	DWG. NO.	DESCRIPTION	QUANTITY MC71A	QUANTITY MC71B
	B1Ø4	INVERTER	2	0
	B213	JAM FLIP-FLOP	8	1
	B36Ø	DELAY WITH PULSE AMPLIFIER	1	0
	B31Ø	DELAY	1	0
	B6Ø2	PULSE AMPLIFIER	1	0
	W712	Board Select Sense	1	0
	GØØ8	MASTER SLICE CONTROL	1	0
	GØ1Ø	SENSE AMP SELECTOR	2	0
	GØ14		18	0
	G211	CURRENT DRIVER	4	4
	G218	INHIBIT DRIVER	9	9
	G219	MEMORY SELECTOR	1	0

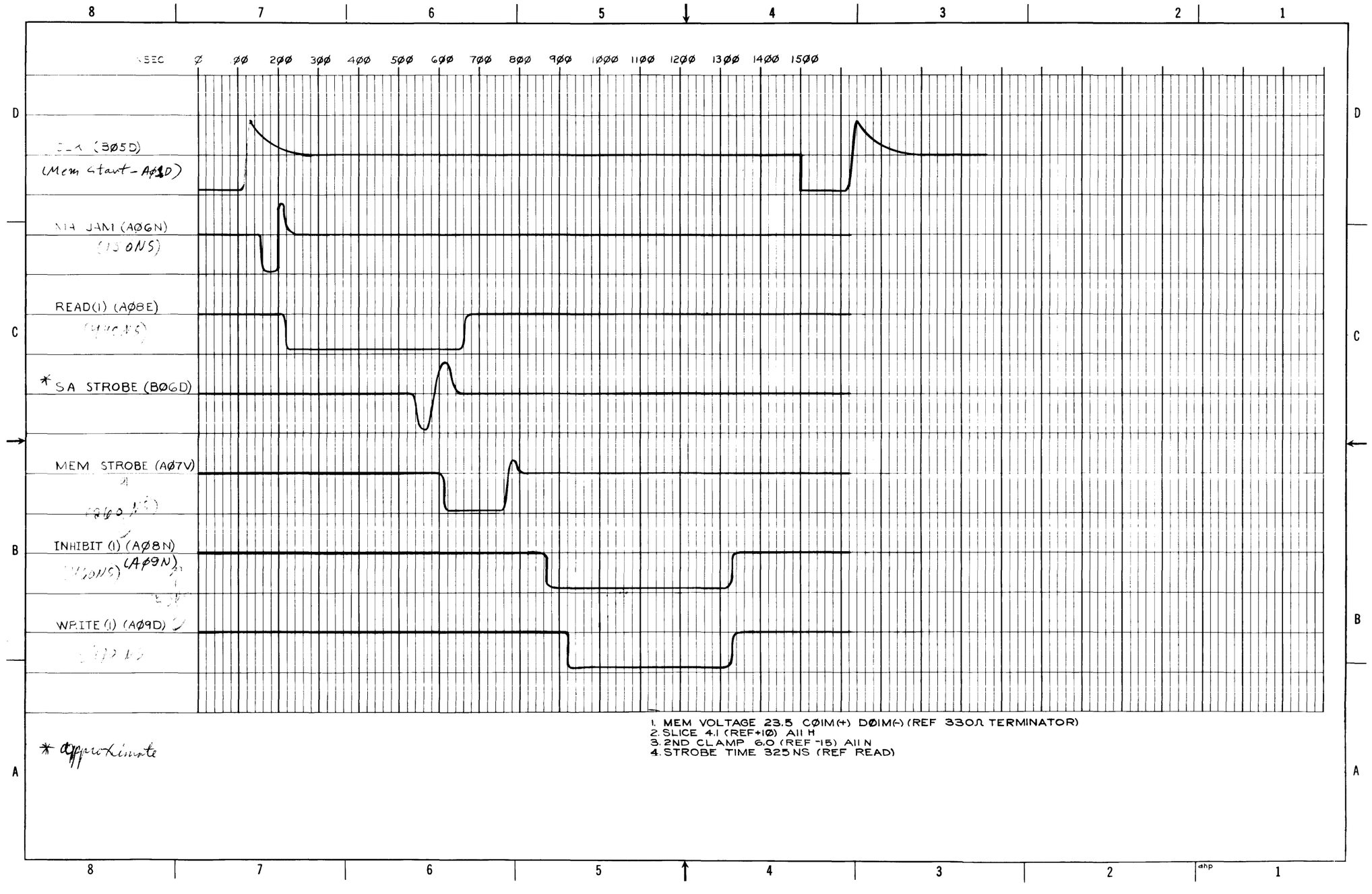
A-PL-MC71-0-12 Module Utilization List (Sheet 1)

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

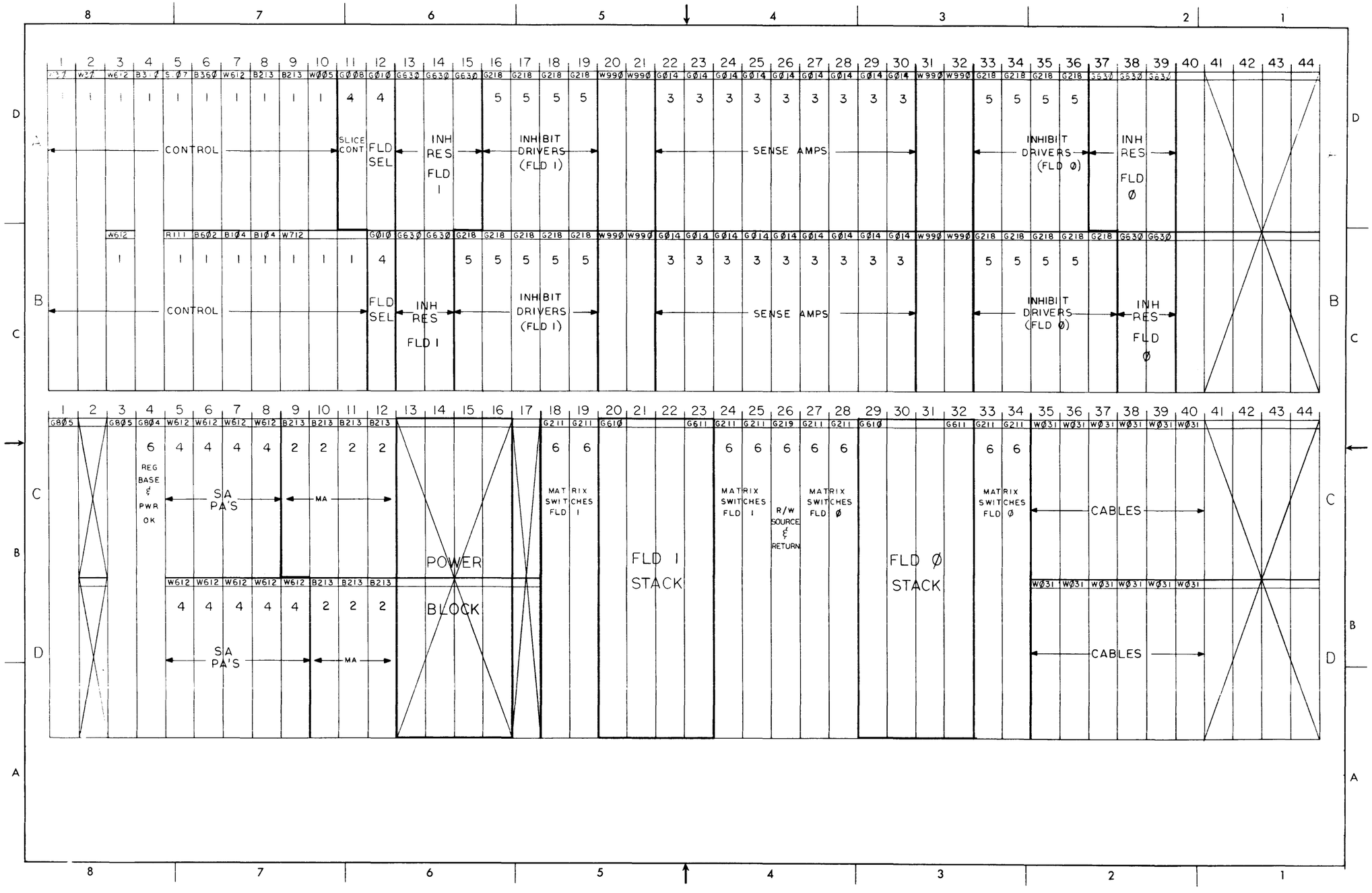
PARTS LIST

ITEM NO.	DWG. NO.	DESCRIPTION	QUANTITY MC71A	QUANTITY MC71B
	G53Ø	RESISTOR BOARD	5	5
	G8Ø4	CONTROL FOR G8Ø5	1	0
	G8Ø5	NEGATIVE REGULATOR	2	0
	R111	EXPANDABLE NAND/NOR GATE	1	0
	S1Ø7	INVERTER	1	0
	WØØ5	CLAMPED LOAD	1	0
	W3Ø1	DELAY LINE	2	0
	W612	Pulse Amp	12	0
	D-SC-3009117-0-0	MEMORY STACK 4K	1	1

A-PL-MC71-0-12 Module Utilization List (Sheet 2)



D-TD-MC71-0-13 Timing Diagram



D-SP-MC71-0-15 MC Switch Configuration

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
STACK CLAMP	750 OHM 1W 5%		C26F	C22F	
STACK CLAMP	750 OHM 1W 5%		C26J	C22J	
STACK CLAMP	750 OHM 1W 5%		D26F	D22F	
STACK CLAMP	750 OHM 1W 5%		D26J	D22J	
CLK	150 OHM ¼W 5%		BØ5D	C05C	
STROBE	150 OHM ¼W 5%		A30U	B30C	
STROBE	150 OHM ¼W 5%		B30U	B30C	
MA JAM	150 OHM ¼W 5%		D12T	D12M	
MEM STROBE	1KΩ ¼W 5%		C38T	C38C	
*MA05A(Ø) ◆	JUMPER		C12E	A1ØU	
*MA05A(Ø) ◇	JUMPER		C12D	C12C	
*MA05B(Ø) ◆	JUMPER		C12P	A1ØV	
*MA05B(Ø) ◇	JUMPER		C12N	C12M	
* JUMPERS TO	BE ADDED	FOR	4K OPERATION		
REMOVE FOR	8K OPERATION				

A-CP-MC71-0-17 MC71 Memory Panel

NOTES:

1. ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN.
2. CONNECTIONS ON ITEMS #3 & #4 TO BE LOCATED & SOLDERED AT MINIMUM PRACTICAL HEIGHT ABOVE BLOCK.
3. USE YEL WIRE, ITEM #5 FOR MACHINE WRAPPED WIRING & BLU WIRE, ITEM #6 FOR HAND WRAPPED WIRING.
4. USE FRAME # E-IA-7405384-0-0 FOR JIG ON WIRE WRAP MACHINE. FOR FINAL MCTI-A ASSEMBLY LOGIC MUST BE SHIFTED TO LOWER HALF OF FRAME.

FRAME IN PHANTOM SEE NOTE 4

SEE DETAIL "A"

REVERSED BLOCK DECALS

SEE DETAIL B

1 2 3 4 5 6 7 8 9

DETAIL A
8 PLACES
SEE NOTE #1 & 2

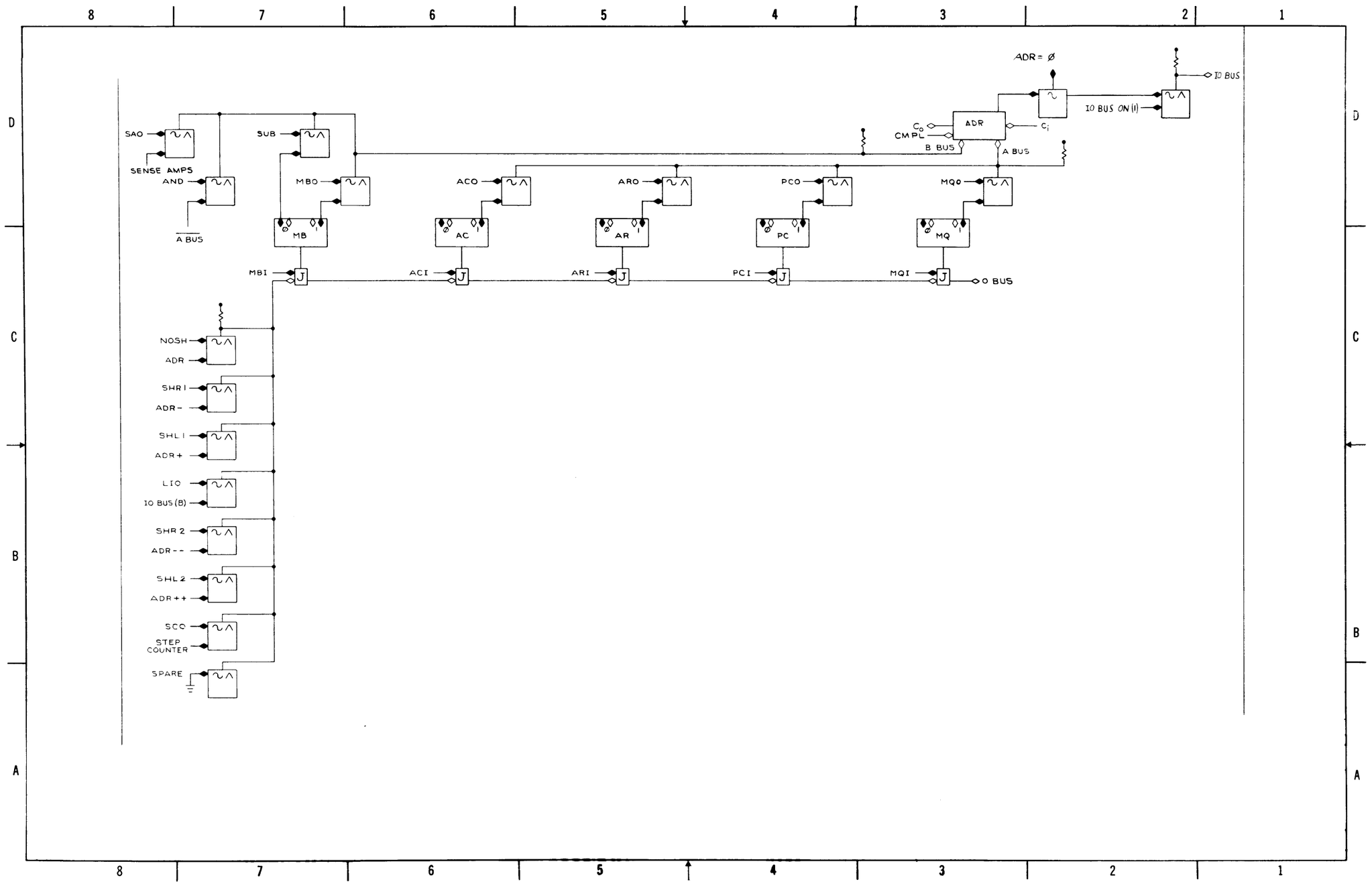
DETAIL B
2 PLACES
SEE NOTE #1 & 2

SECTION A-A

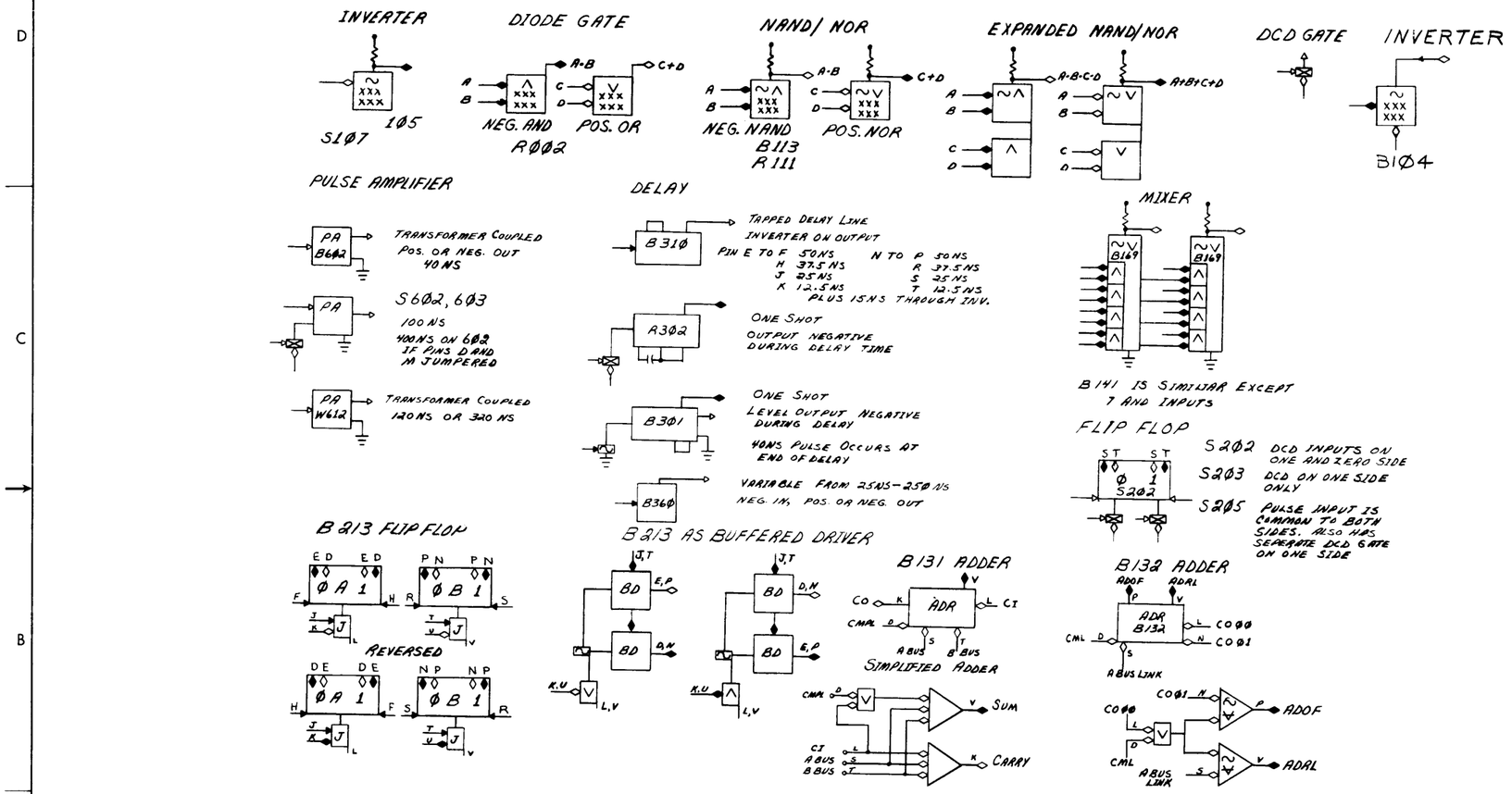
D-AD-7005828-0-0 Logic Frame Assembly

PARTS LIST	DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.
1	D-AD-7005099-0-0	1	MTG BAR ASSY (10 CONN BLOCKS)	7005099
2	D-AD-7005102-0-0	1	MTG BAR ASSY (ONE REV BLOCK)	7005102
3		A/R	VOLTAGE CHAIN	1202188
4		A/R	#24 AWG SOLID KYNAR WHT	9107470-1
5		A/R	#24 AWG SOLID KYNAR YEL	9107470-5
6		A/R	#24 AWG SOLID KYNAR BLU	9107470-10
7	K-WL-MC71-0-16	REF	WIRE LIST MC71	
8	A-CP-MC71-0-17	REF	EXTERNAL COMPONENT LIST MC71	
9	A-DC-7406747-0-0	REF	DECALS, REVERSE BLOCK	7406747

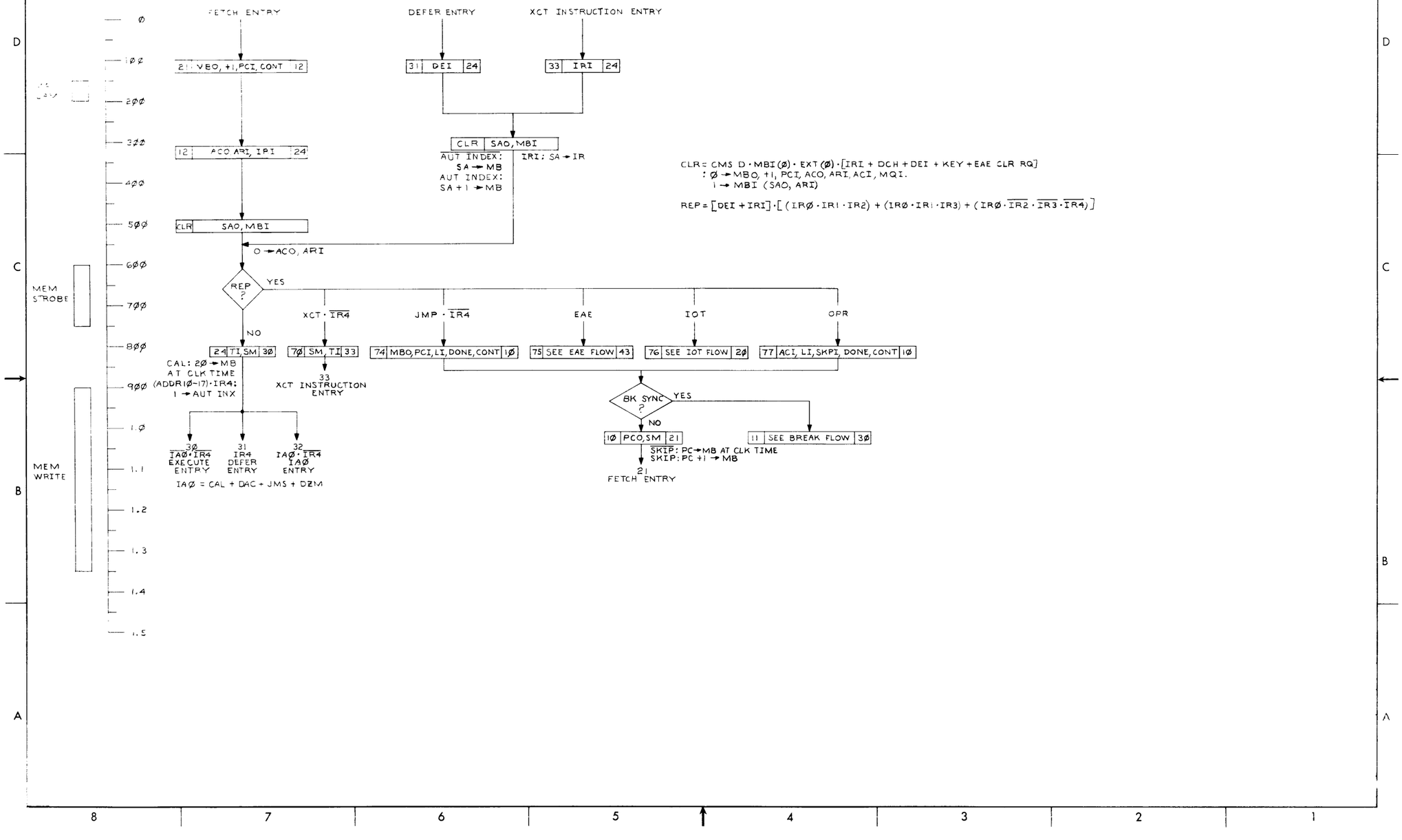
A-PL-7005828-0-0 Logic Frame Assembly



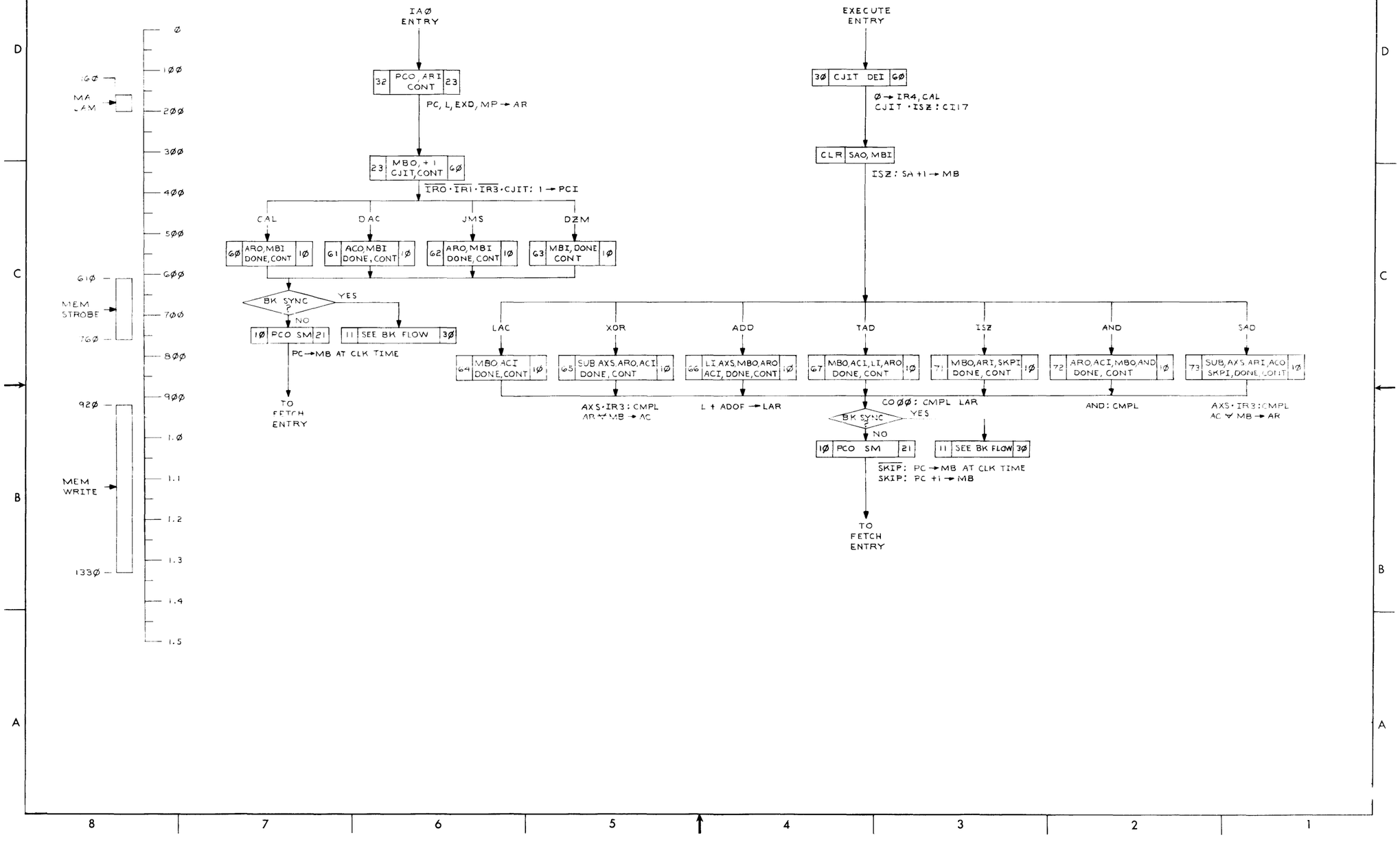
D-BS-KC09-C-1 Register Configuration



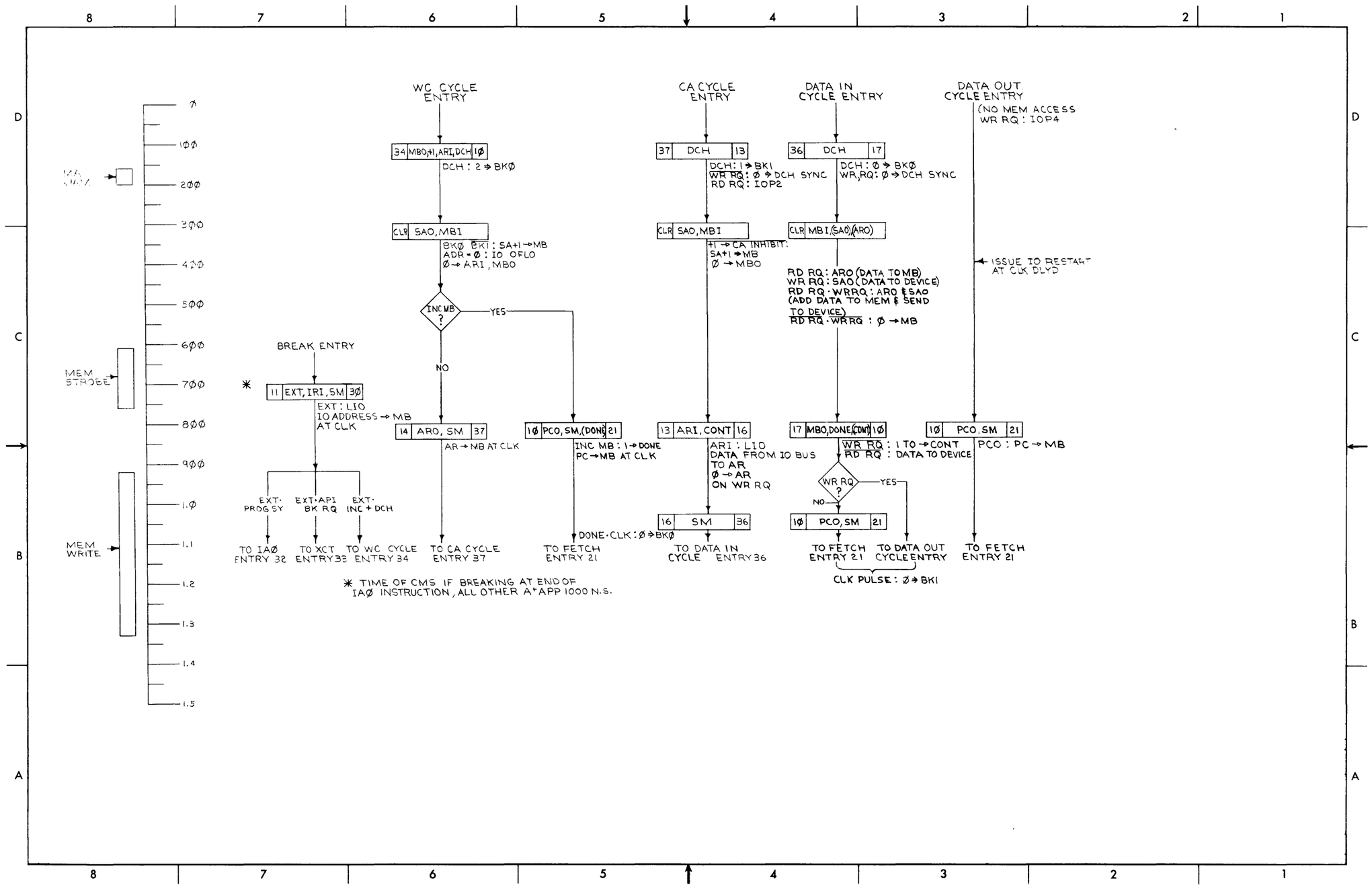
D-BS-KC09-C-2 Special Modules



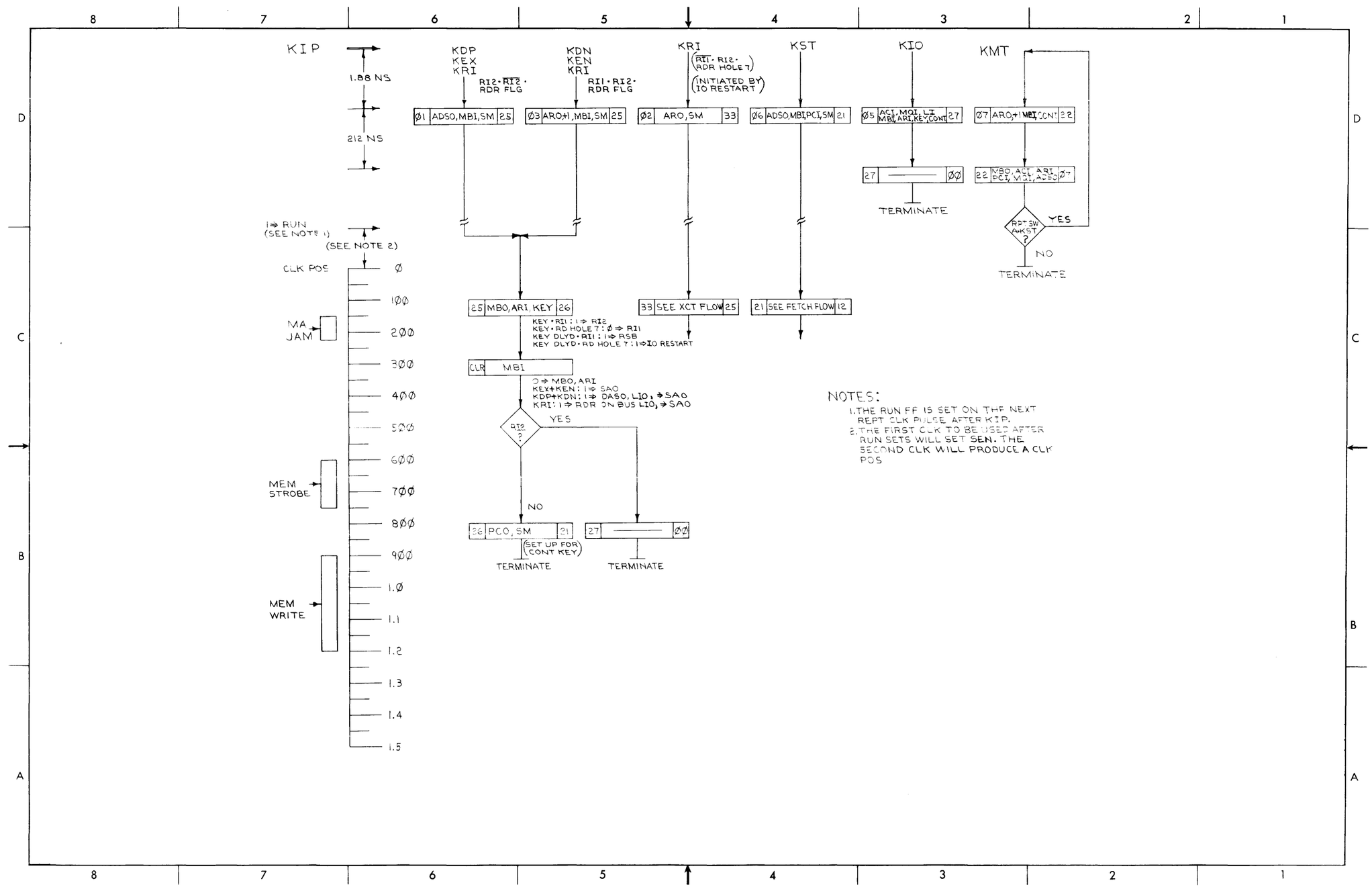
D-TD-KC09-C-3 Fetch Flow



D-TD-KC09-C-4 Execute Flow



D-TD-KC09-C-5 Break Flow



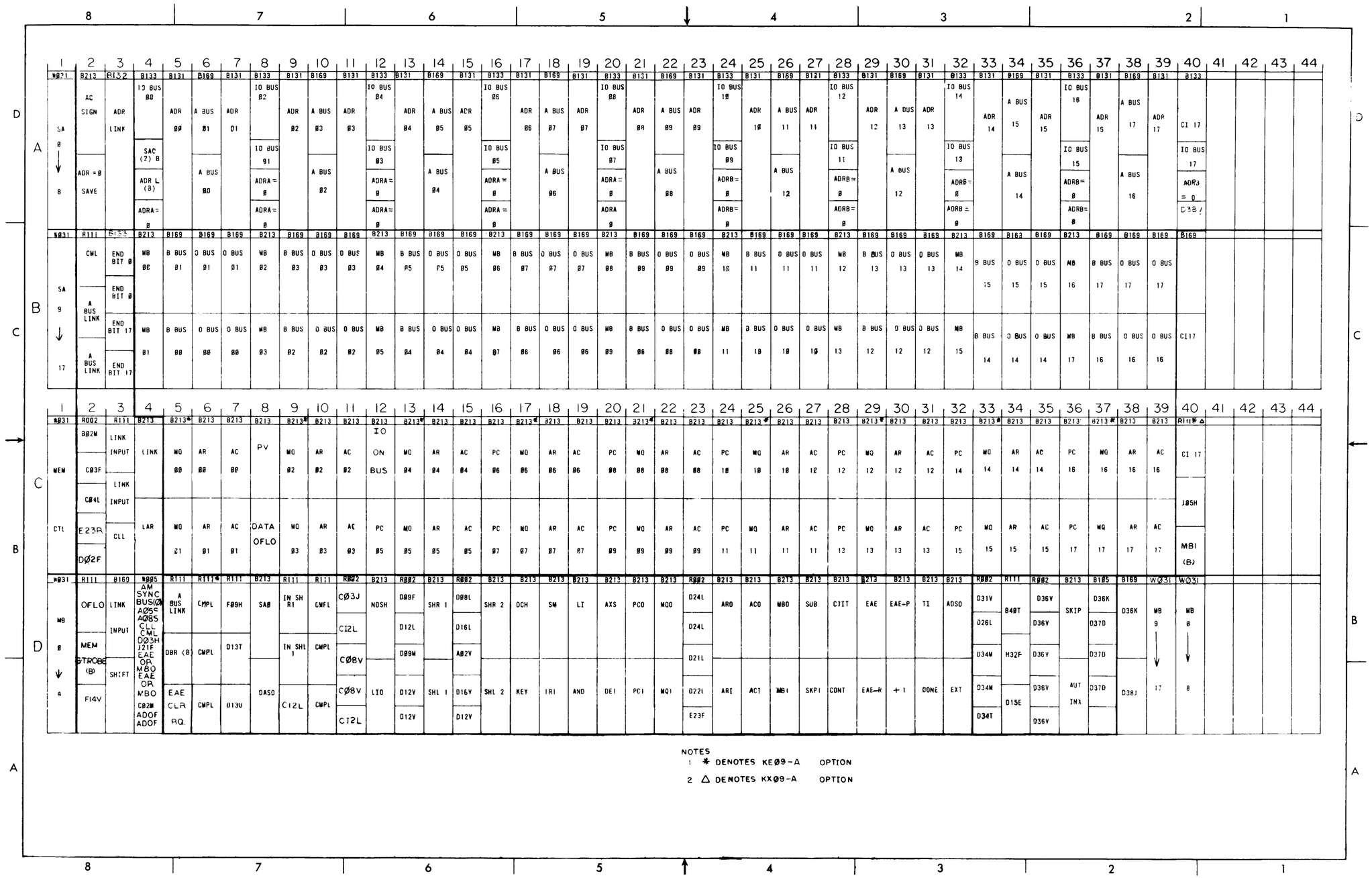
D-TD-KC09-C-6 Key Flow

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

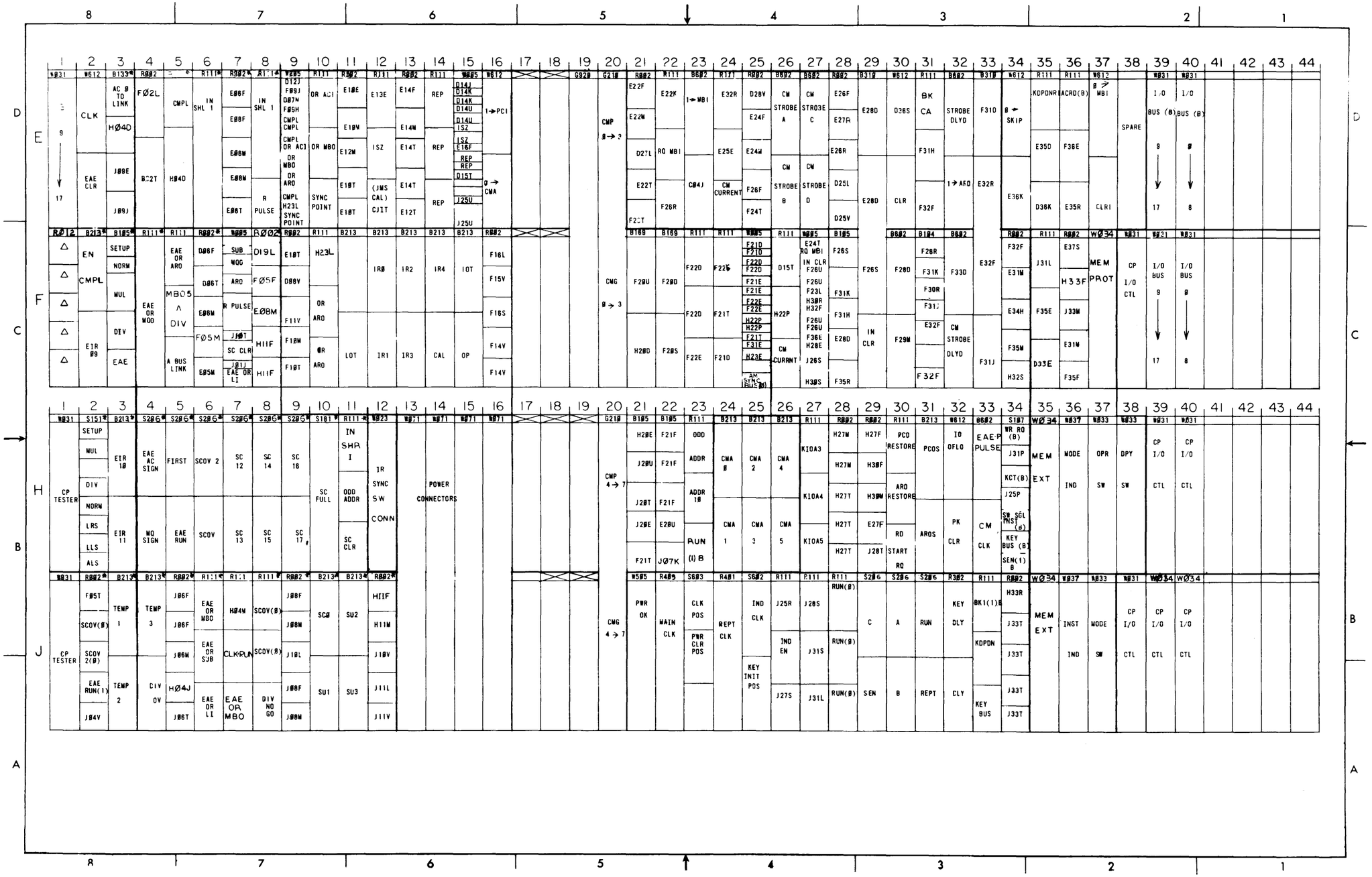
ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION
	B104	INVERTER	1
	B105	INVERTER	4
	B131	ADDER	18
	B132	LINC ADDER	1
	B133	DIODE GATE	11
	B169	INVERTER	41
	B213	JAM FLIP FLOP	75
	B310	DELAY	2
	B602	PULSE AMPLIFIER	7
	G210	CONTROL MEMORY DRIVER	2
	(G920) MC09	CONTROL MEMORY	1
	R002	DIODE NETWORK	20
	R012	DIODE CLUSTER	1
	R111	EXPANDABLE NAND/NOR GATE	30
	R302	DUAL DELAY MULTIVIBRATOR	1
	R401	VARIABLE CLOCK	1
	R409	CRYSTAL CLOCK 1.5 MHz	1
	S107	INVERTER	1
	S206	DUAL FLIP FLOP	3
	S602	PULSE AMPLIFIER	1
	S603	PULSE AMPLIFIER	1
	W005	CLAMPED LOAD	5

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION
	W505	LOW VOLTAGE DETECTOR	1
	W612	PULSE AMPLIFIER	5
	S151		
	S181		

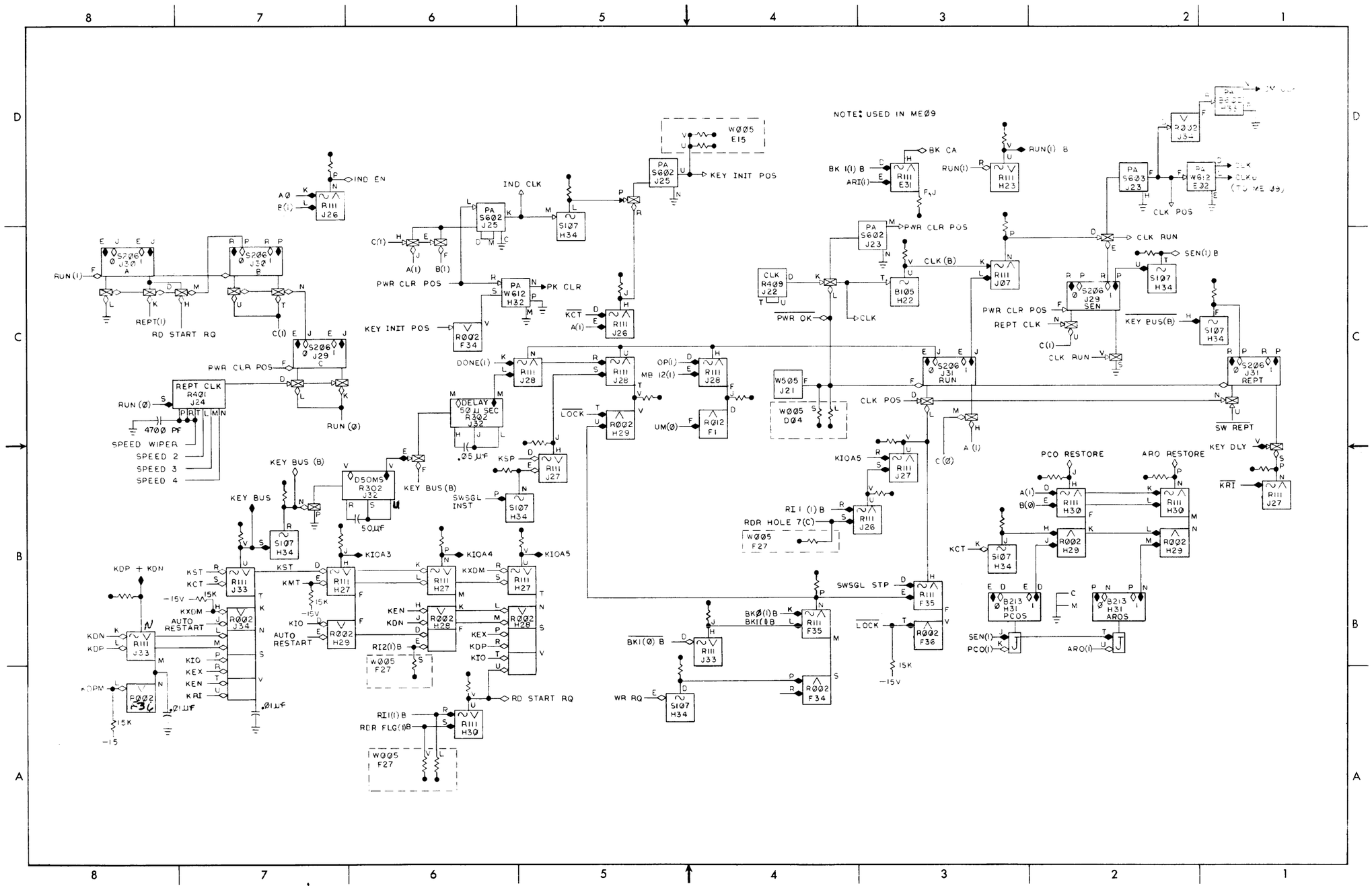


D-MU-KC09-C-8 CP Module Utilization (Sheet 1)



D-MU-KC09-C-8 CP Module Utilization (Sheet 2)

D-SP-KC09-C-9 CP MC Switch Configuration

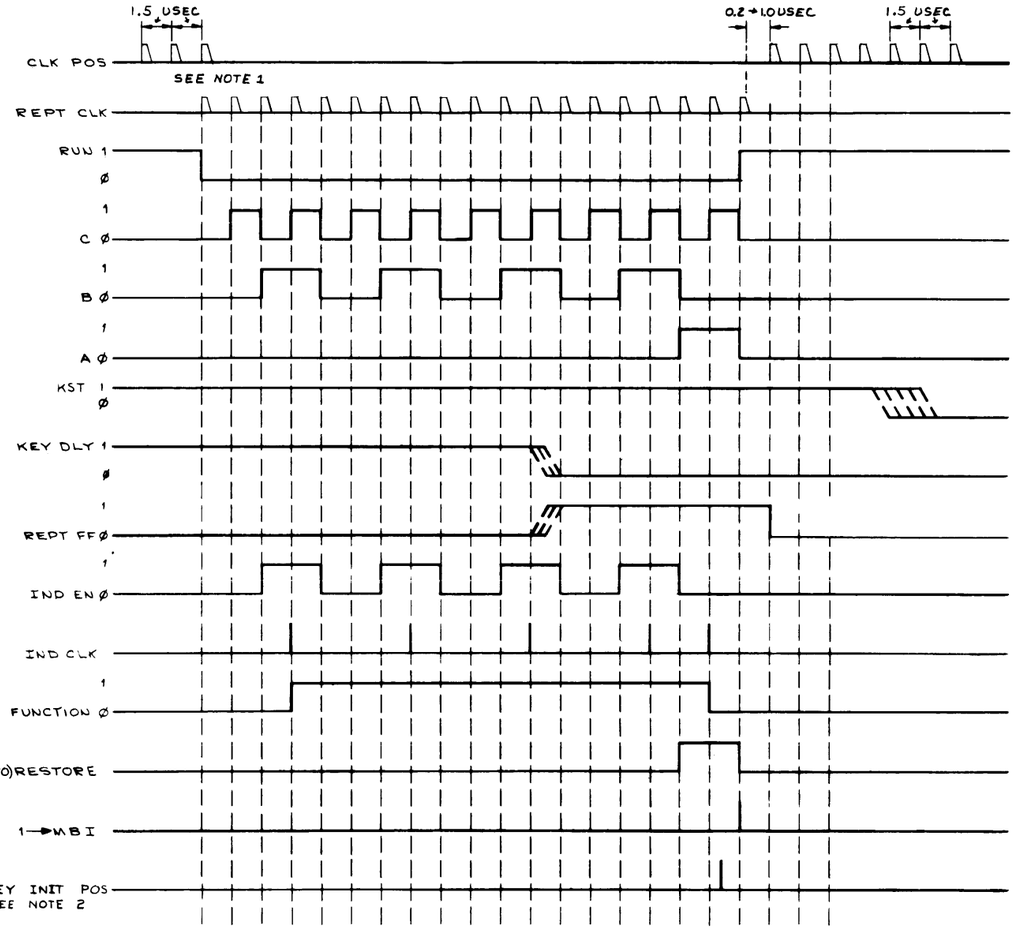


D-BS-KC09-C-10 Clock and Run and Display

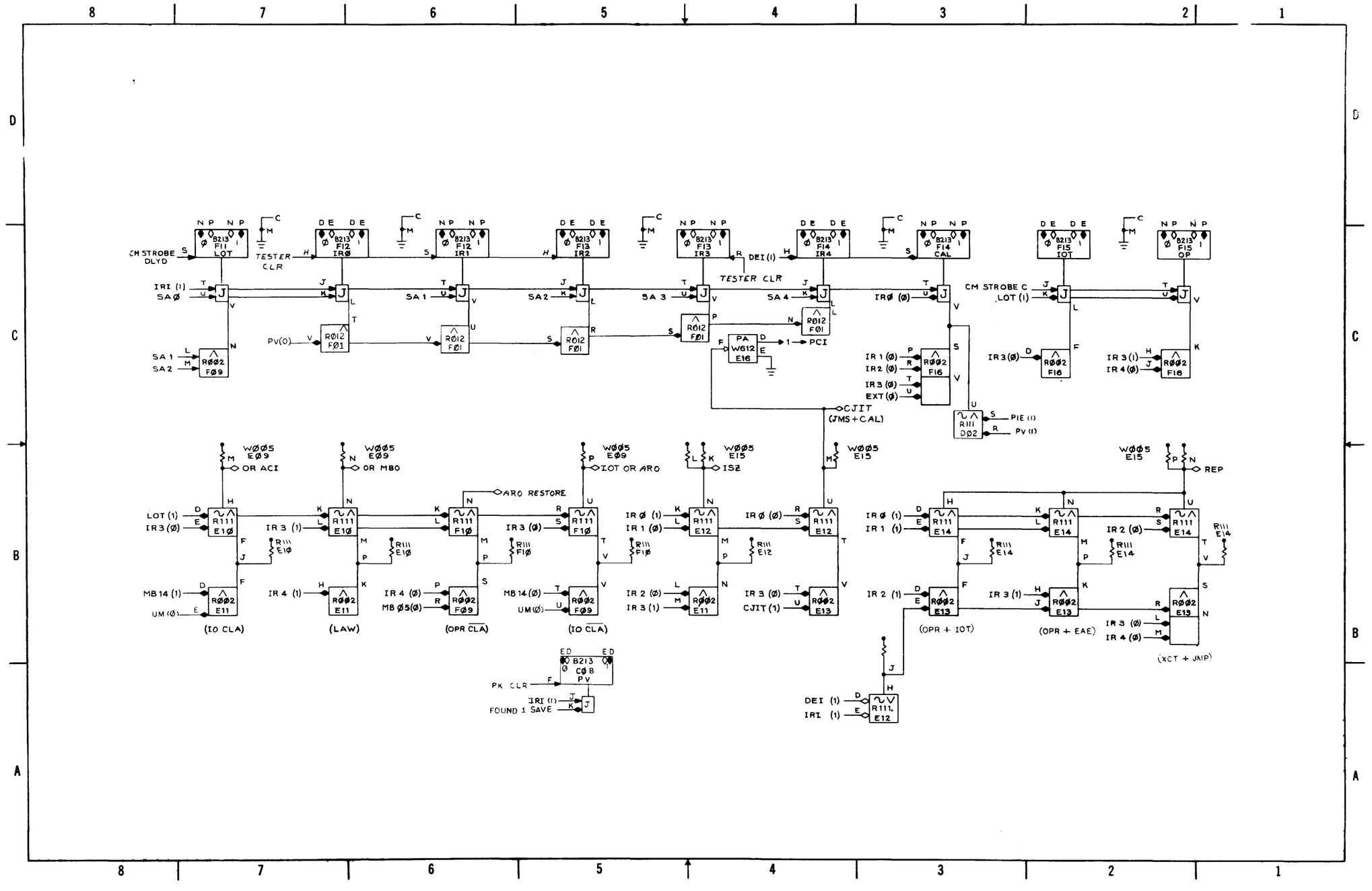
NOTES:
1. REPEAT SWITCH DETERMINES PERIOD OF REPT CLK. APPROXIMATE TIME AS FOLLOWS:

REPT SW. POS.	PERIOD
3	APPROX. 2US
4	APPROX. 40MS
5	APPROX. 150MS
6	APPROX. 450MS
7	APPROX. 1SEC

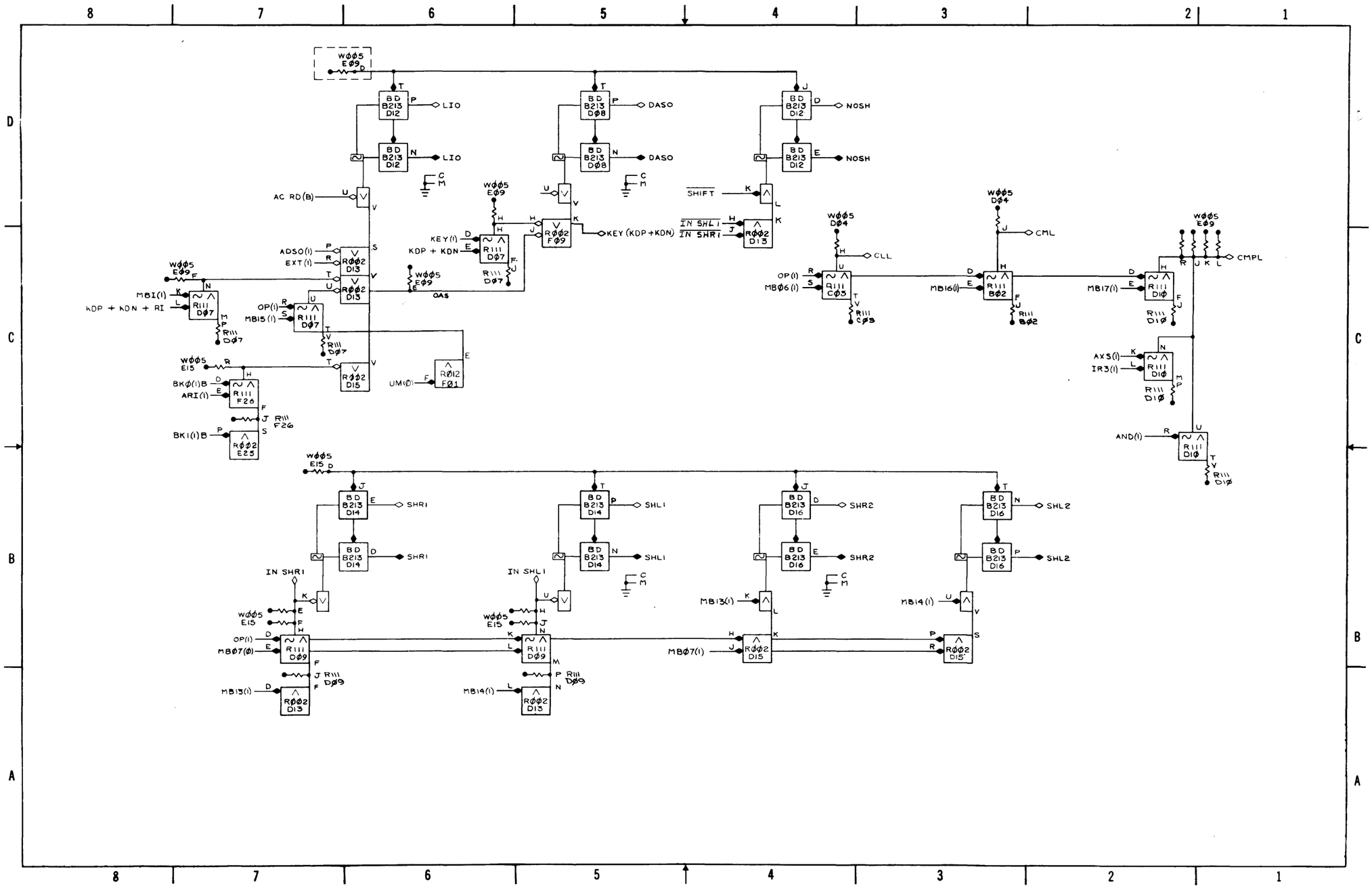
2. NOT GENERATED FOR KCT.



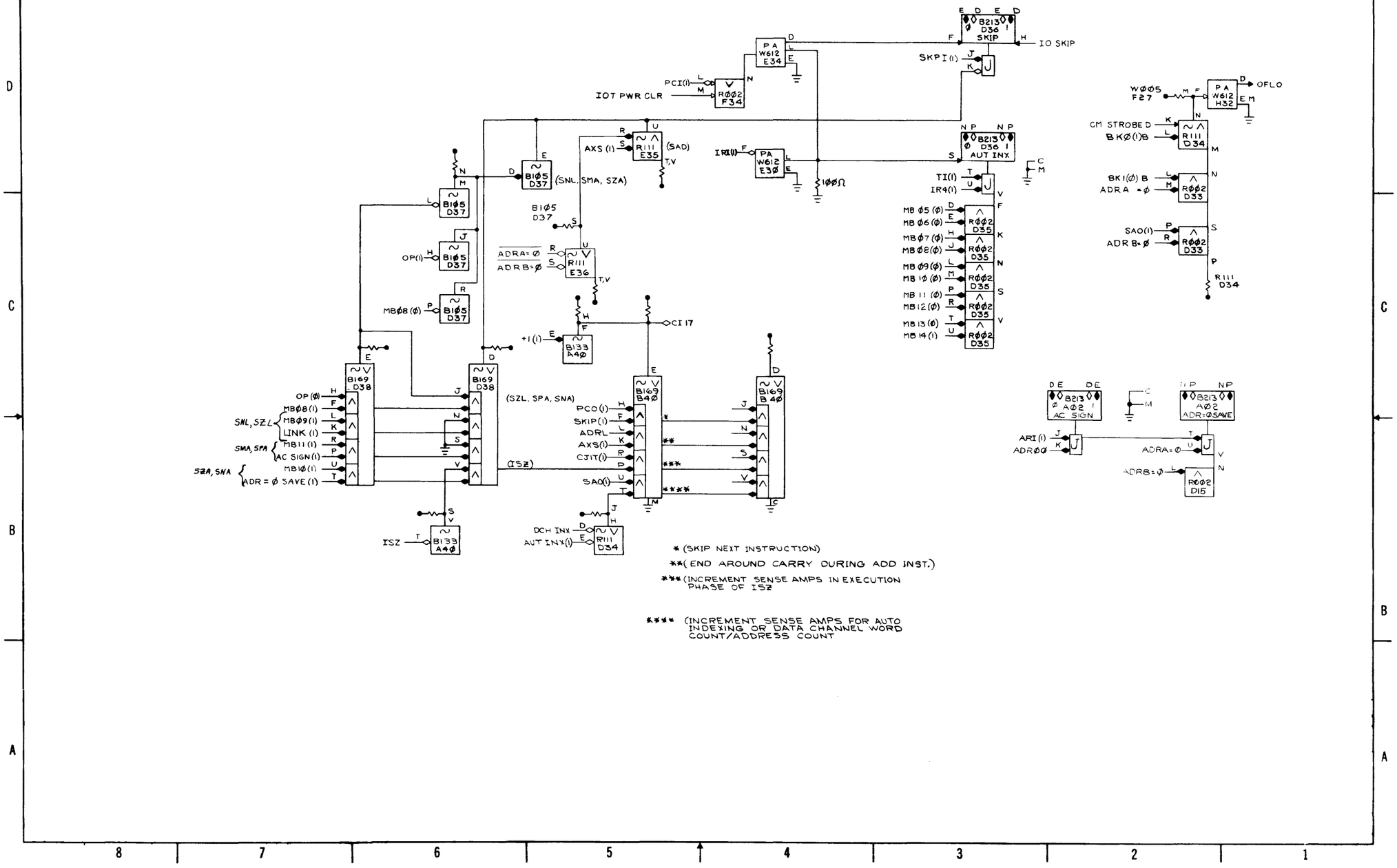
D-TD-KC09-C-11 Clock and Run and Display Timing Diagram



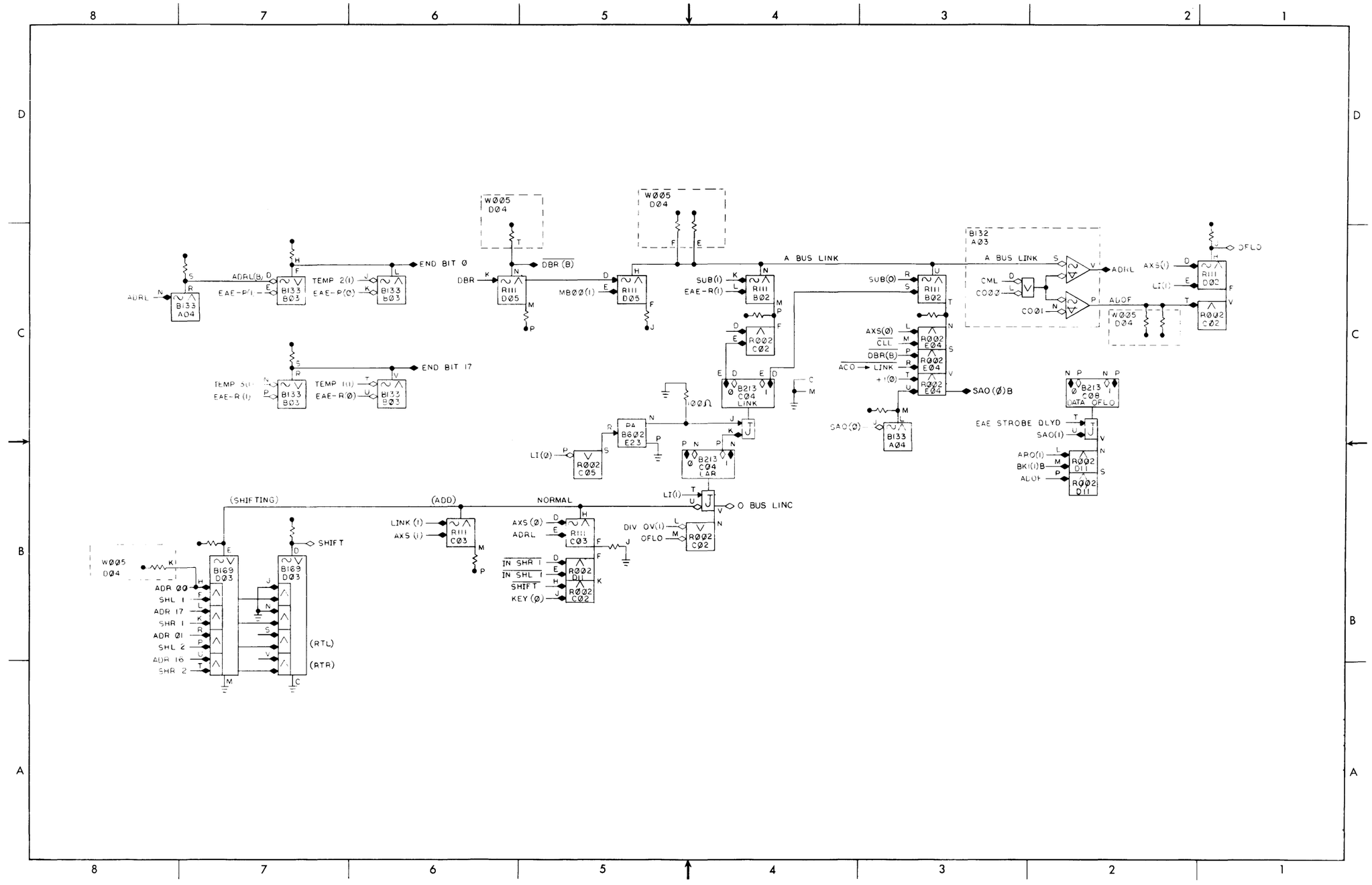
D-BS-KC09-C-12 IR



D-BS-KC09-C-13 Operate Control

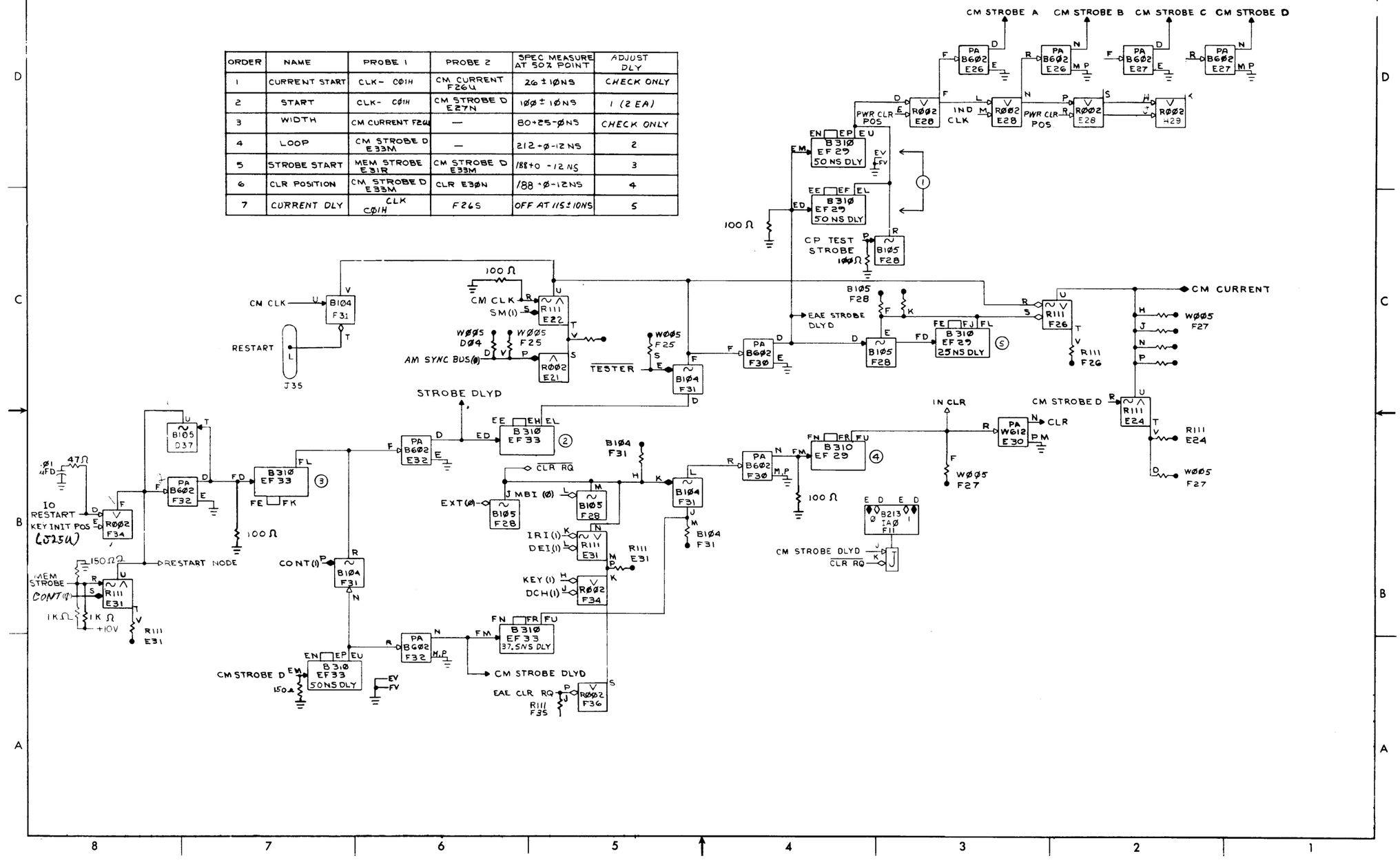


D-BS-KC09-C-14 SKIP and CI17

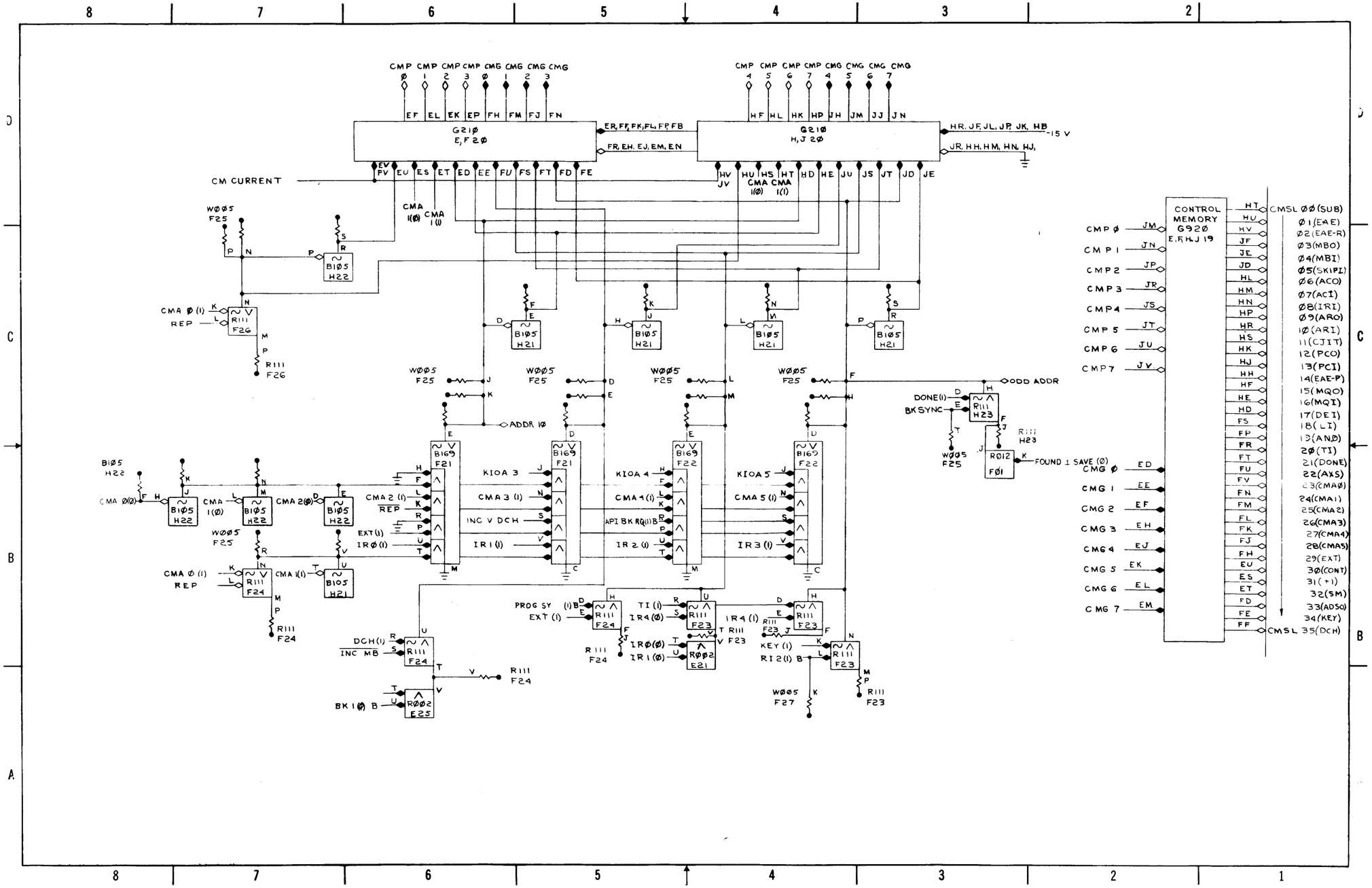


D-BS-KC09-C-15 Link Control

ORDER	NAME	PROBE 1	PROBE 2	SPEC MEASURE AT 50% POINT	ADJUST DLY
1	CURRENT START	CLK- C01H	CM CURRENT F26U	26 ± 10NS	CHECK ONLY
2	START	CLK- C01H	CM STROBE D E27N	10Ø ± 10NS	1 (2 EA)
3	WIDTH	CM CURRENT F26U	—	80+25-ØNS	CHECK ONLY
4	LOOP	CM STROBE D E33M	—	212-Ø-12 NS	2
5	STROBE START	MEM STROBE E31R	CM STROBE D E33M	188+0 -12 NS	3
6	CLR POSITION	CM STROBE D E33M	CLR E30N	188 -Ø-12NS	4
7	CURRENT DLY	CLK C01H	F26S	OFF AT 115±10NS	5



D-BS-KC09-C-16 CM Timing

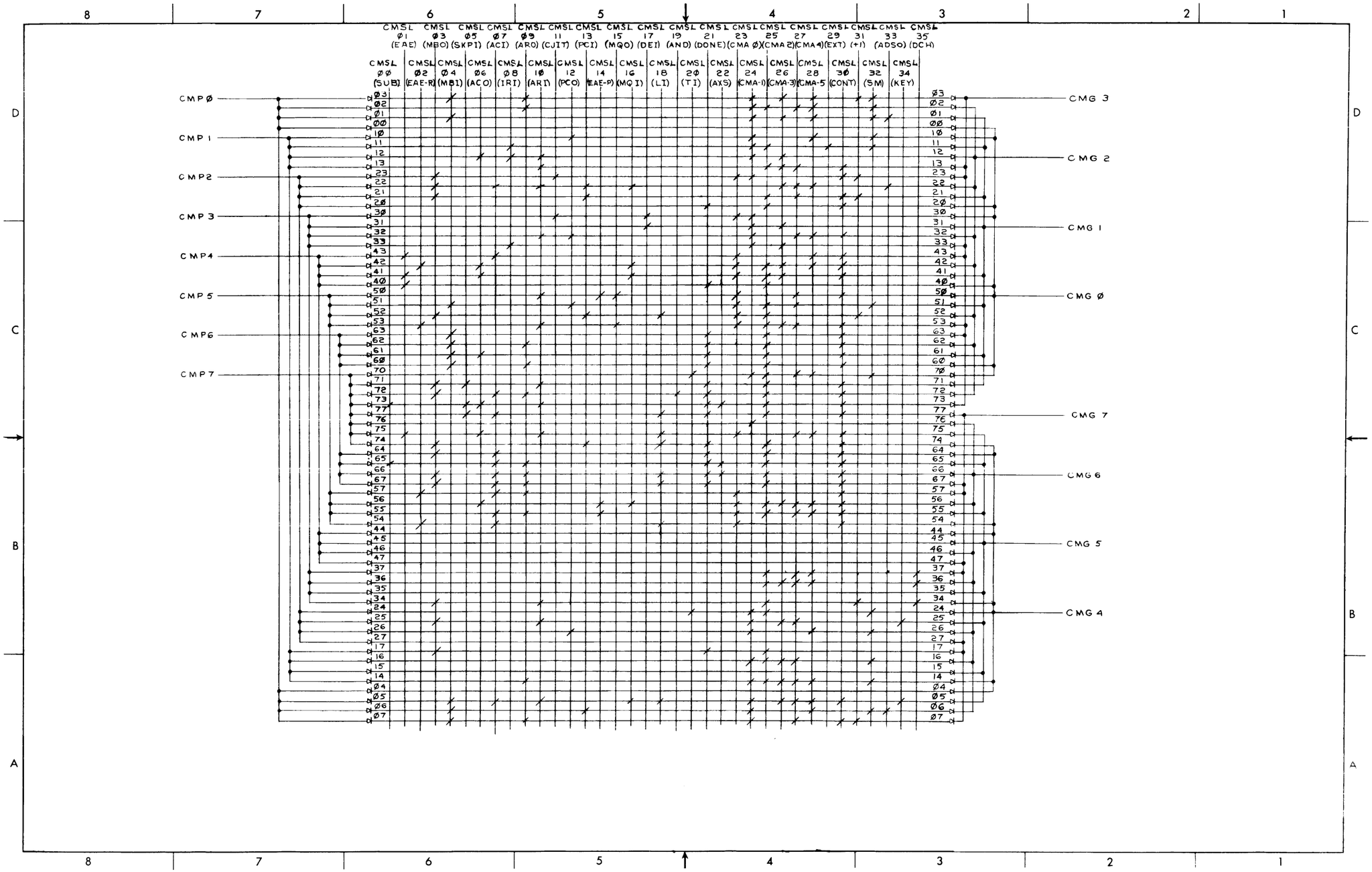


D-BS-KC09-C-17 CM Addressing

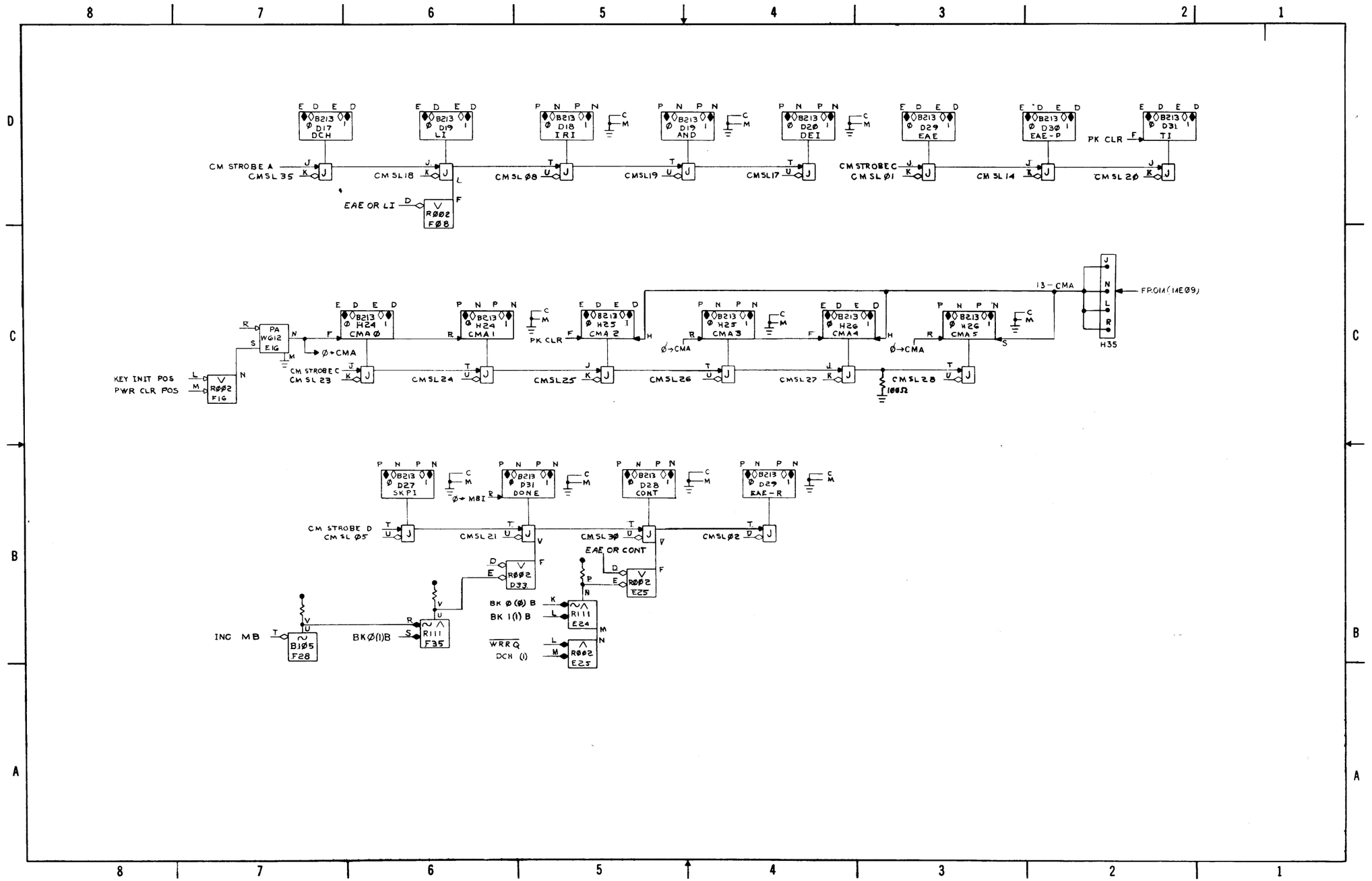
LOC	TAG	BITS	SYNC	JMP
00	KEY NOP			00
01	RI1·RDR FLG-KEY-KDP	AOSO, WBI	SM	25
02	RI 2	ARO	SM	33
03	KEN·KDN·(RI1·RI2·RDR·FLG)	ARO,+ 1, WB I	SM	25
04				
05	KIO	AOI,MQI,LI,KEY,WBI,ARI	CONT	27
06	KST	ADSO, WBI, PCI	SM	21
07	KMT	ARO,+ 1, WBI	CONT	22
10	BGN	PCO	SM	21
11	BREAK ENTRY	EXT, IRI	SM	30
12		ACO, ARI, IRI		24
13		ARI	CONT	16
14		ARO	SM	37
15				
16			SM	36
17		WBO, DONE		10
20		DONE	CONT	10
21	FETCH ENTRY	WBO,+ 1, PCI	CONT	12
22		WBO,ACI,ARI,PCI,MQI,ADSO		07
23		WBO,+ 1, CJ,T	CONT	60
24		TI	SM	30
25		WBO, ARI, KEY		26
26	KEY·RI2	PCO	SM	21
27	KEY·RI2			00
30	EXECUTE ENTRY	CJIT DEI		60
31	DEFER ENTRY	DEI		24
32	IAØ ENTRY	PCO, ARI	CONT	23
33	XCT ENTRY	IRI		24
34	DCH SYNC+CLK SYNC	WBO,+ 1, ARI, DCH		10
35				
36	DATA IN/OUT ENTRY	DCH		17
37	CA ENTRY	DCH		13

LOC	TAG	BITS	SYNC	JMP
40		EAE,DONE		1Ø
41		ACO MQI EAE	CONT	54
42		ACO, MQI, EAE-R	CONT	55
43		ACI , EAE	CONT	41
44				
45				
46				
47				
50		MQO, ARI, EAE-P	CONT	42
51		PCO, MBI	CONT	52
52		MBQ,+1,PCI,LI		5Ø
53		MQO, ARI, EAE-R	CONT	56
54		ACI, EAE-R,	CONT	4Ø
55		ARO ACI, EAE-P	CONT	53
56		ACO, MQI, EAE-P	CONT	57
57		ARO ACI, EAE-R	CONT	4Ø
60	CAL	ARO, WBI, DONE	CONT	10
61	DAC	ACO, WBI, DONE	CONT	10
62	JMS	ARO, WBI, DONE	CONT	10
63	DZM	WBI DONE	CONT	10
64	LAC	WBO, ACI, DONE	CONT	10
65	XOR	SUB,AXS,ARO,ACI,DONE	CONT	10
66	ADD	WBO,ARO,ACI,AXS,LI,DONE	CONT	10
67	TAD	WBO,ARO,ACI,LI,DONE	CONT	10
70	XCT	TI	SM	33
71	ISZ	WBO, SKPI, ARI, DONE	CONT	10
72	AND	ARO WBO,ACI,AND DONE	CONT	10
73	SAD	SUB,ACO,AXS,SKPI ARI,DONE	CONT	10
74	JMP	WBO, PCI DONE, LI	CONT	10
75	EAE	ACO, ARI, EAE, LI	CONT	43
76	IOT			20
77	OPR	ACI, LI, SKPI, DONE	CONT	10

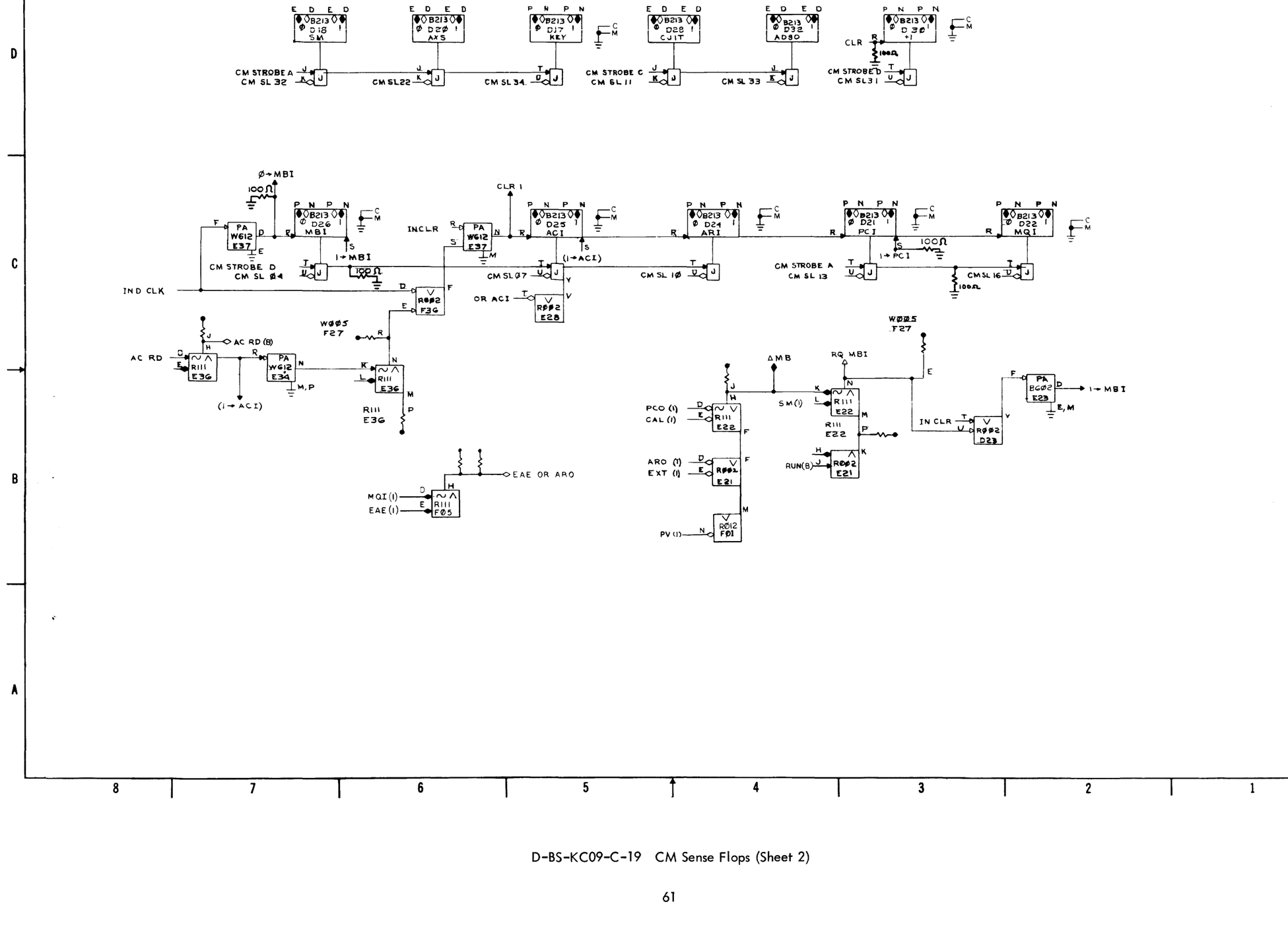
D-FD-KC09-C-18 CM Wiring Matrix and Program (Sheet 1)



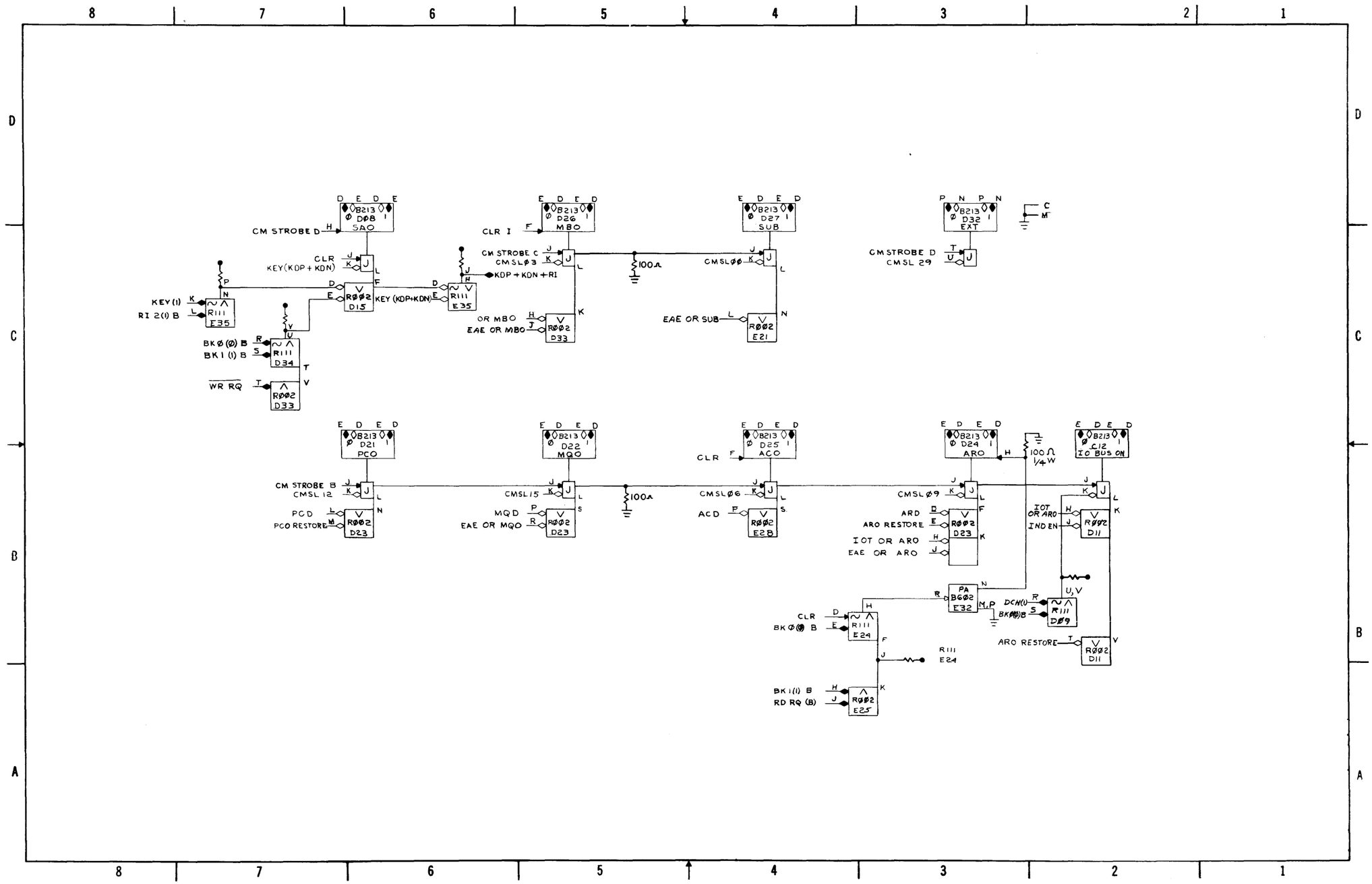
D-FD-KC09-C-18 CM Wiring Matrix and Program (Sheet 2)



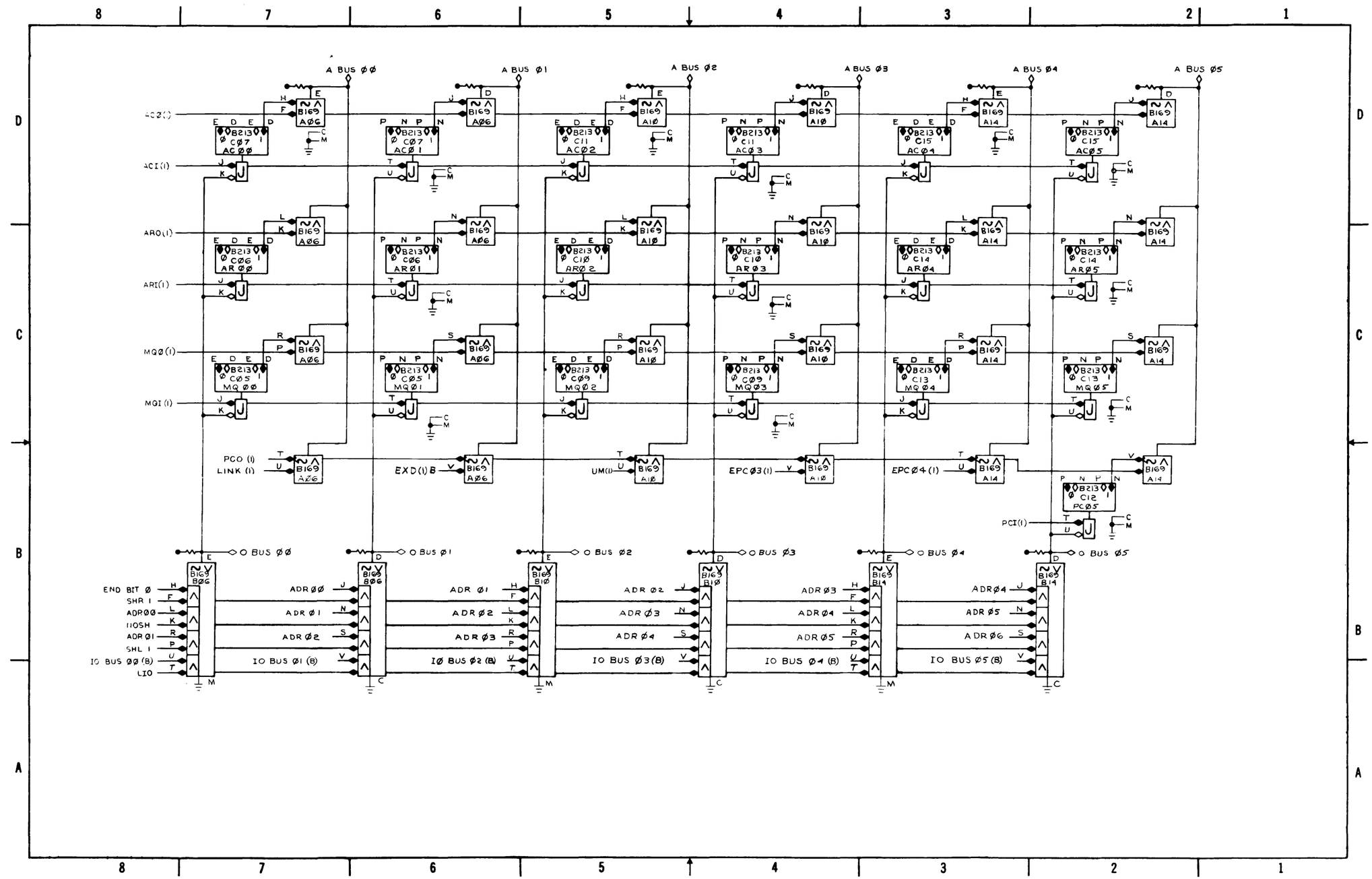
D-BS-KC09-C-19 CM Sense Flops (Sheet 1)



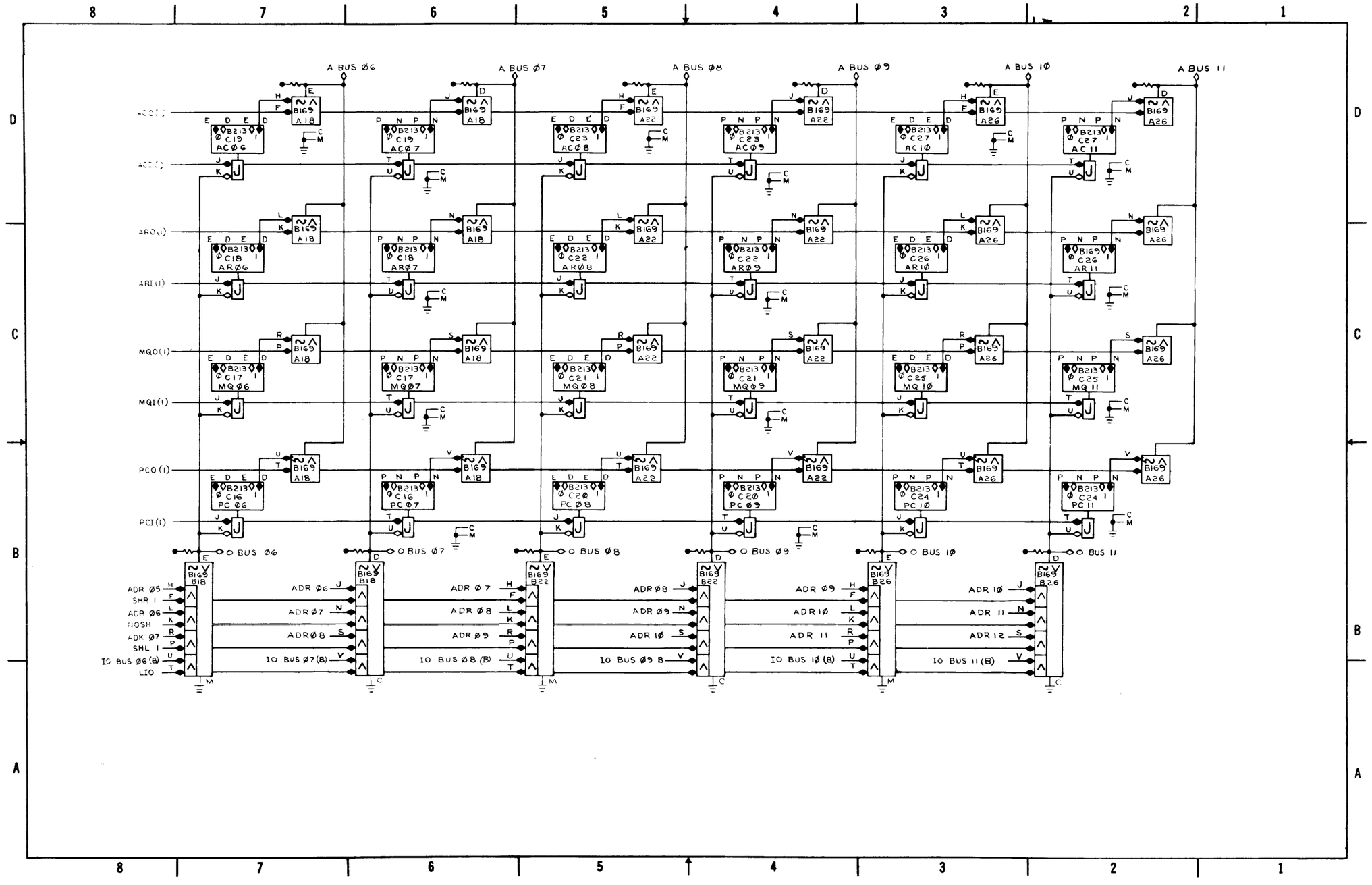
D-BS-KC09-C-19 CM Sense Flops (Sheet 2)



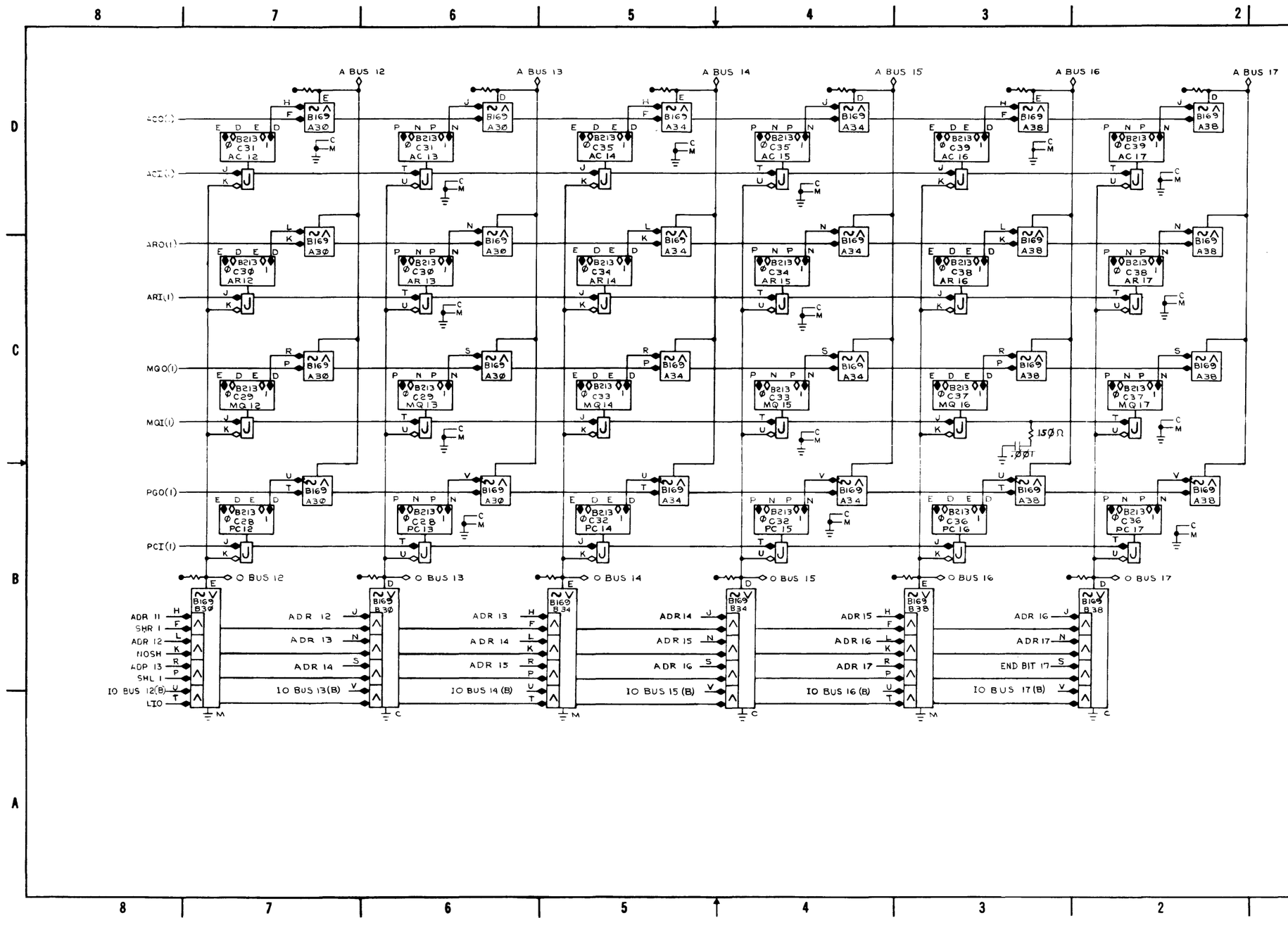
D-BS-KC09-C-19 CM Sense Flops (Sheet 3)



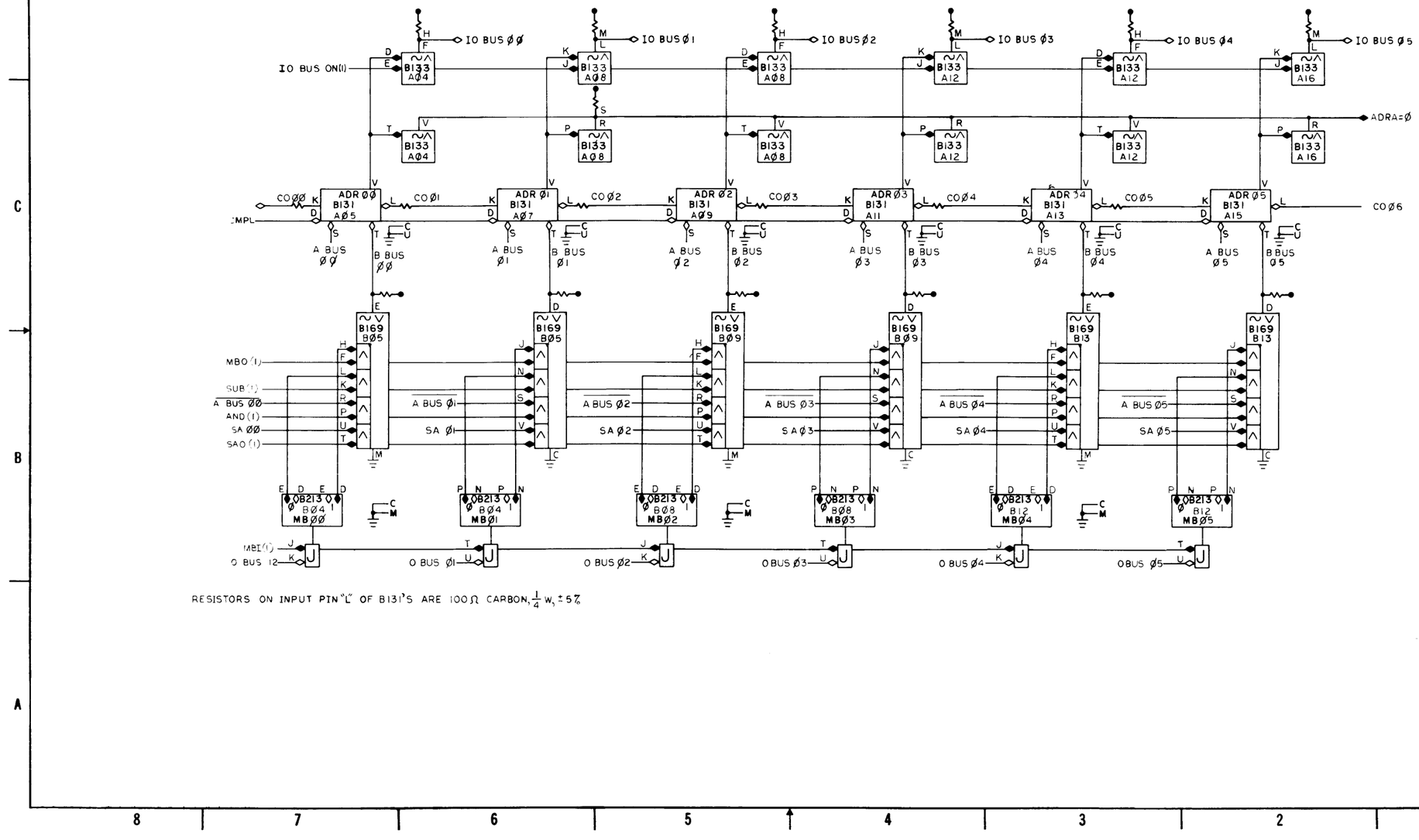
D-BS-KC09-C-20 AC, AR, MC, PC (Sheet 1)



D-BS-KC09-C-20 AC, AR, MC, PC (Sheet 2)

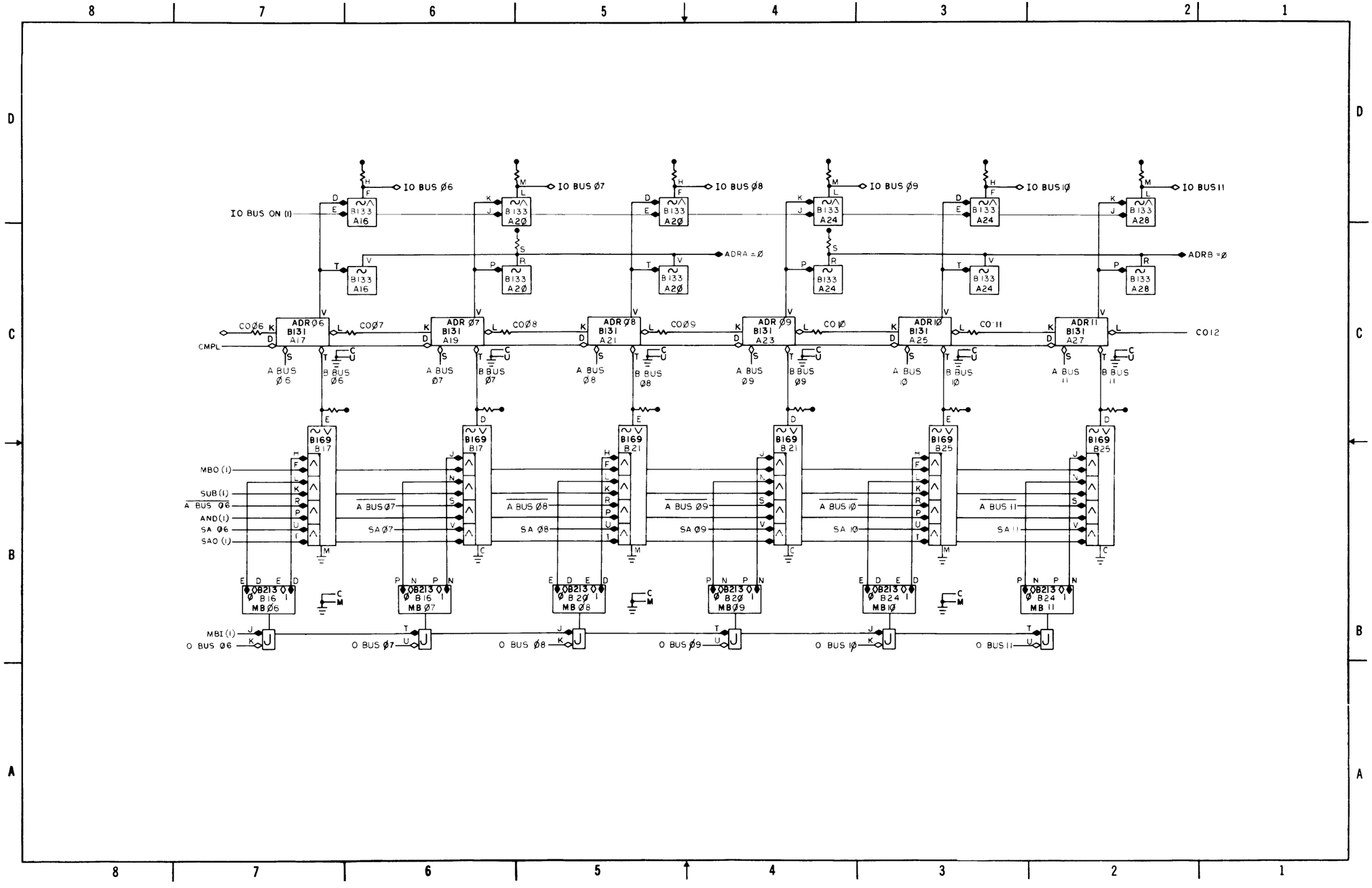


D-BS-KC09-C-20 AC, AR, MC, PC (Sheet 3)

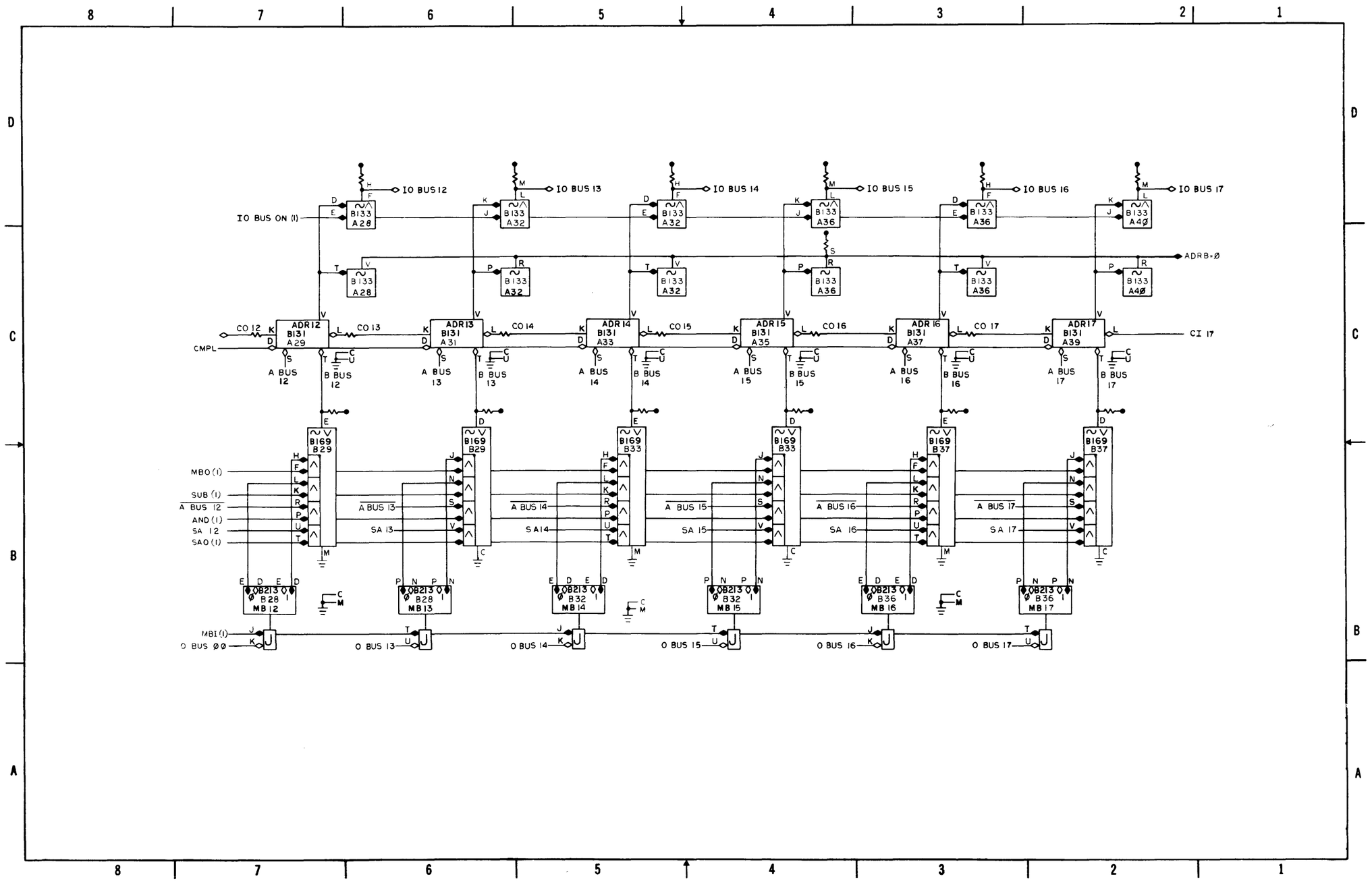


RESISTORS ON INPUT PIN "L" OF B131'S ARE 100Ω CARBON, $\frac{1}{4}$ W, ± 5%

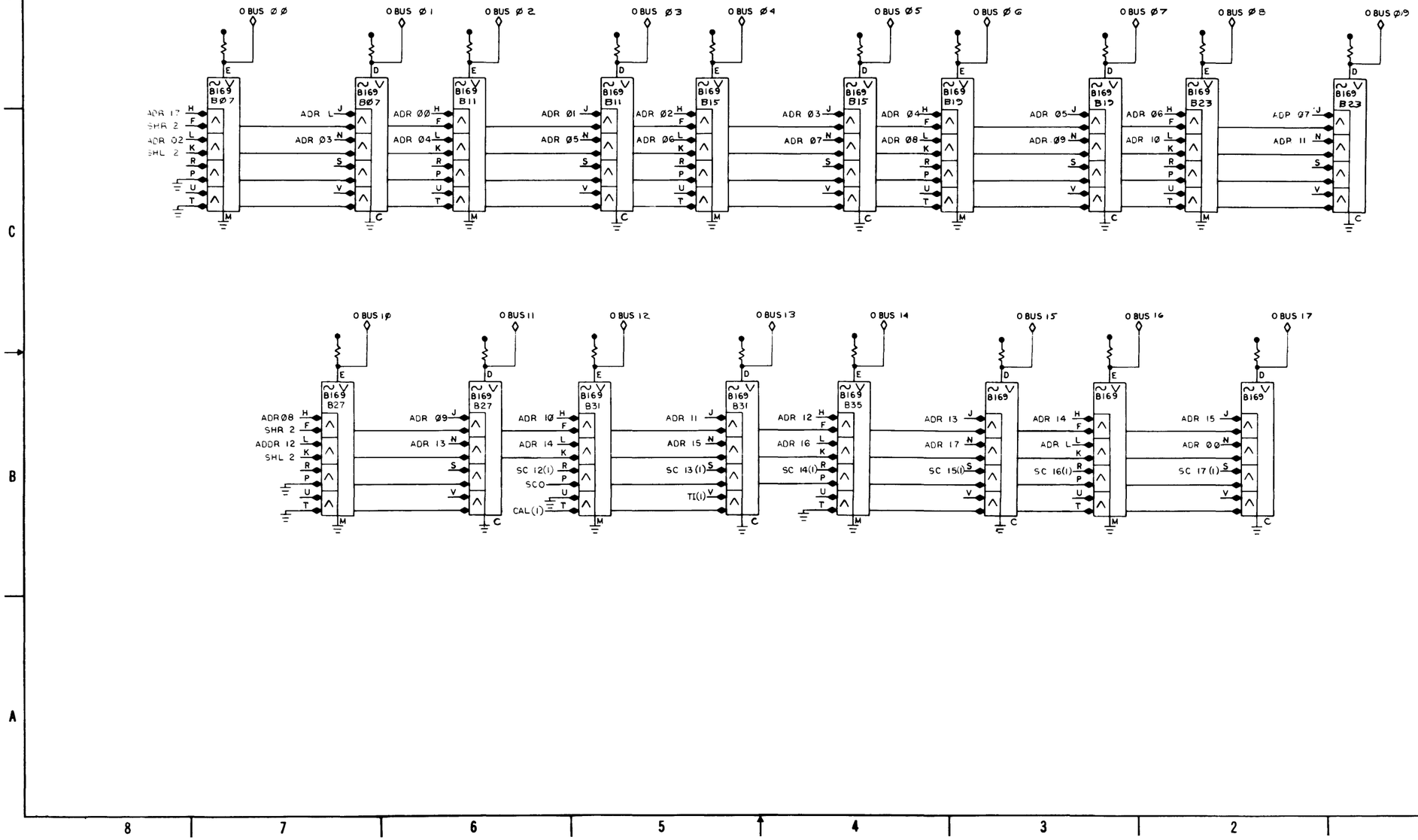
D-BS-KC09-C-21 MB and Adder (Sheet 1)



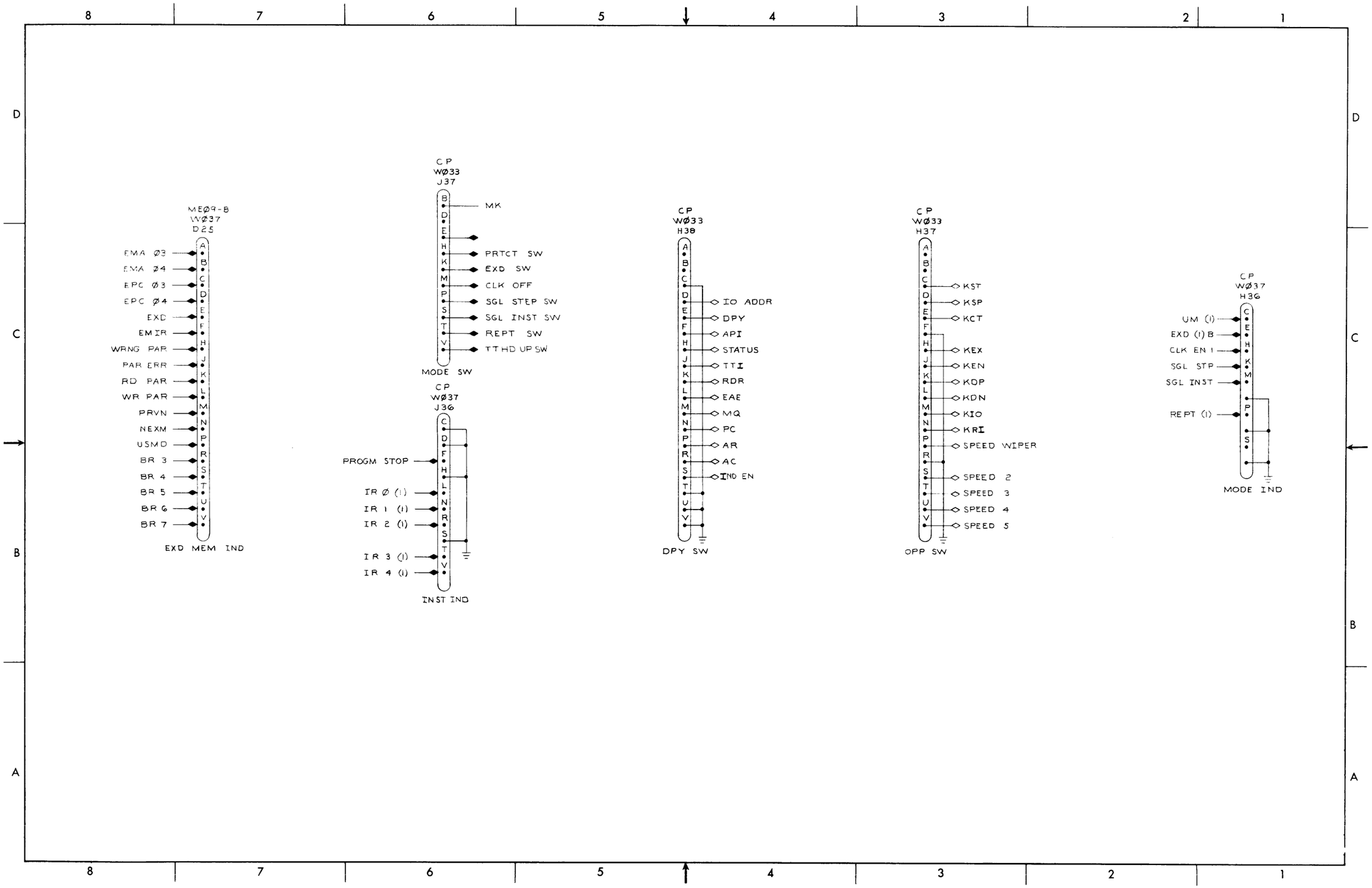
D-BS-KC09-C-21 MB and Adder (Sheet 2)



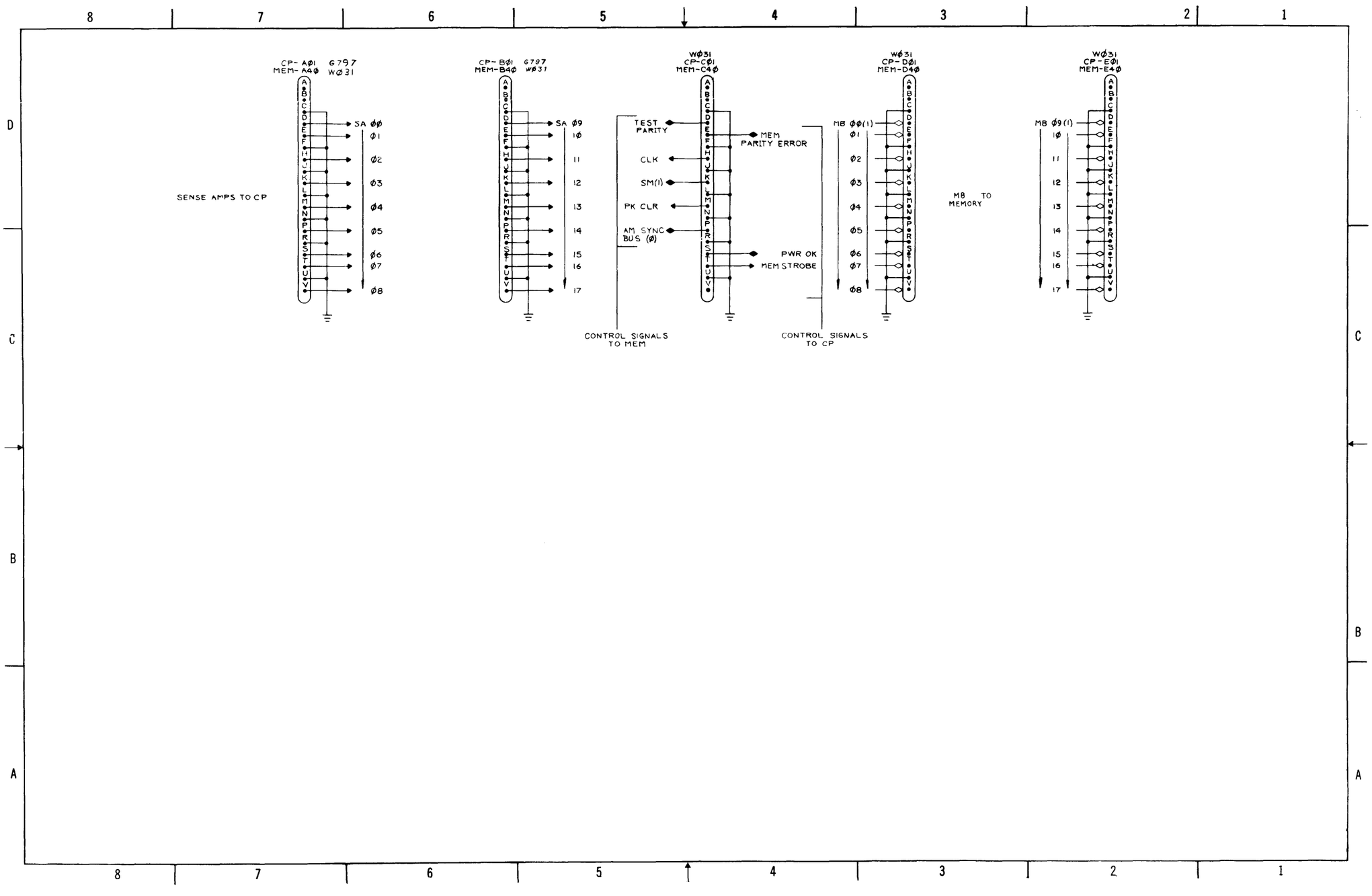
D-BS-KC09-C-21 MB and Adder (Sheet 3)



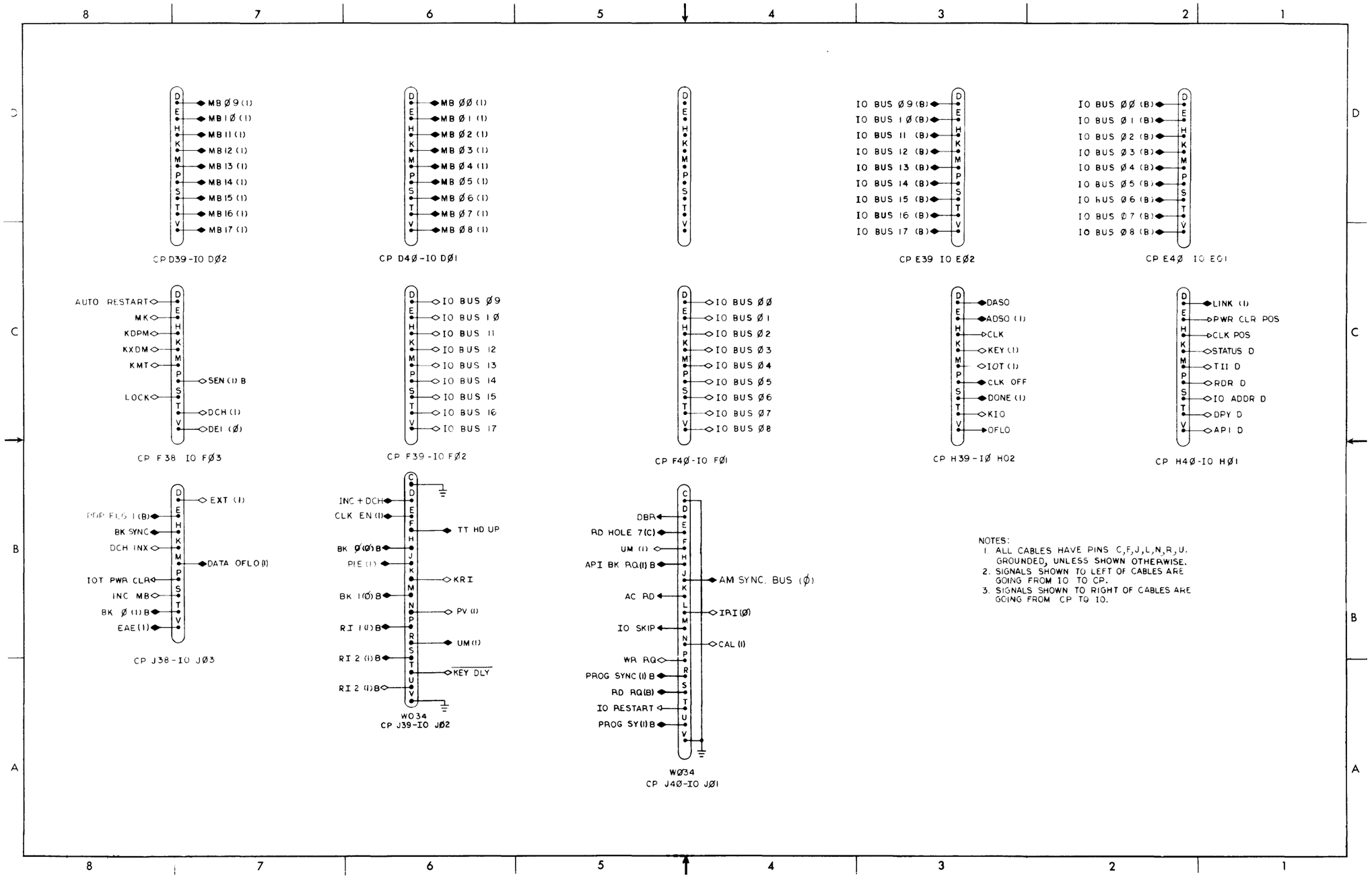
D-BS-KC09-C-22 Shift X2 Gates



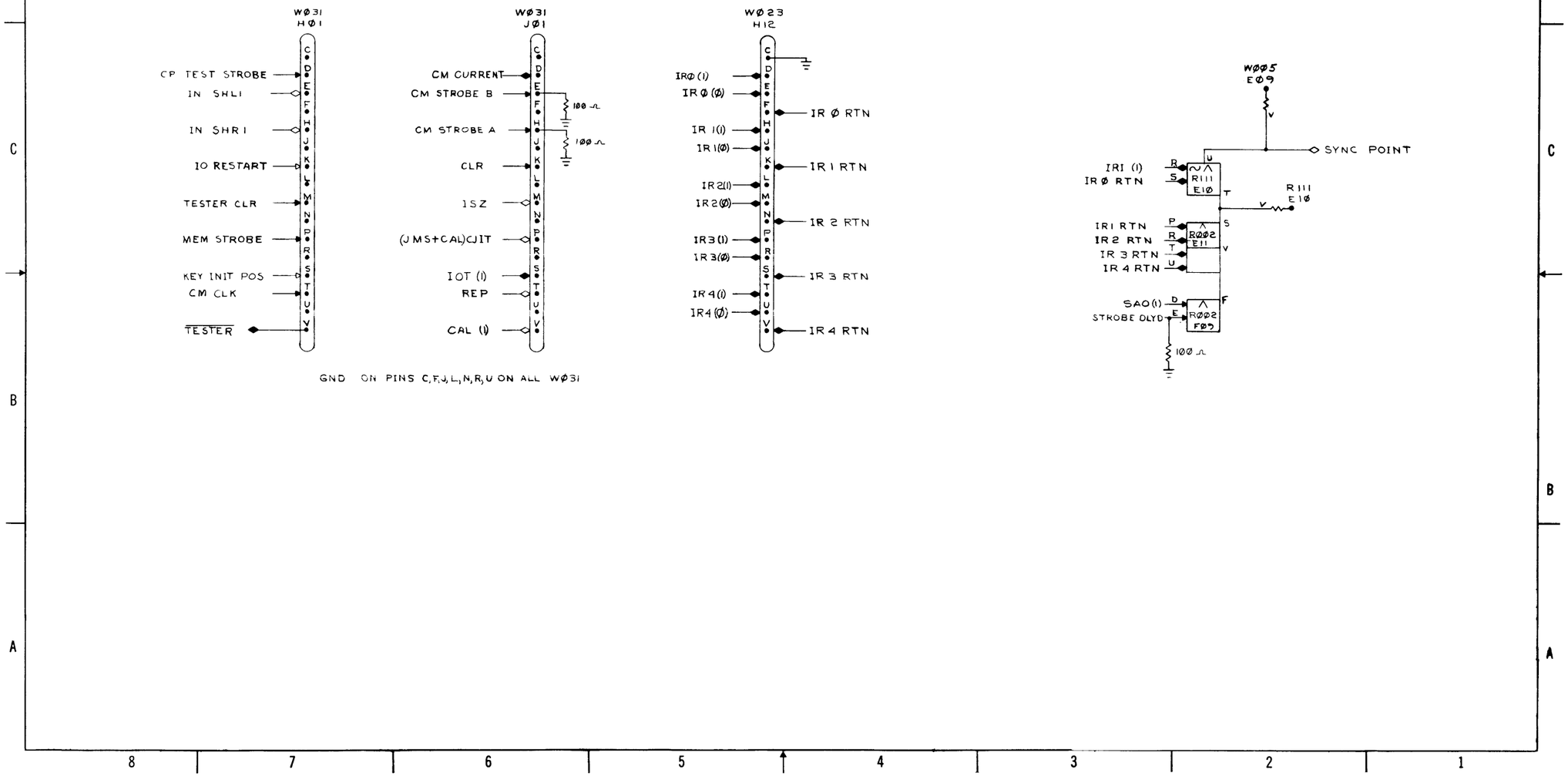
D-IC-KC09-C-23 CP - Console Interface



D-IC-KC09-C-24 CP - Memory Interface



D-IC-KC09-C-25 CP-IO Cable Interface



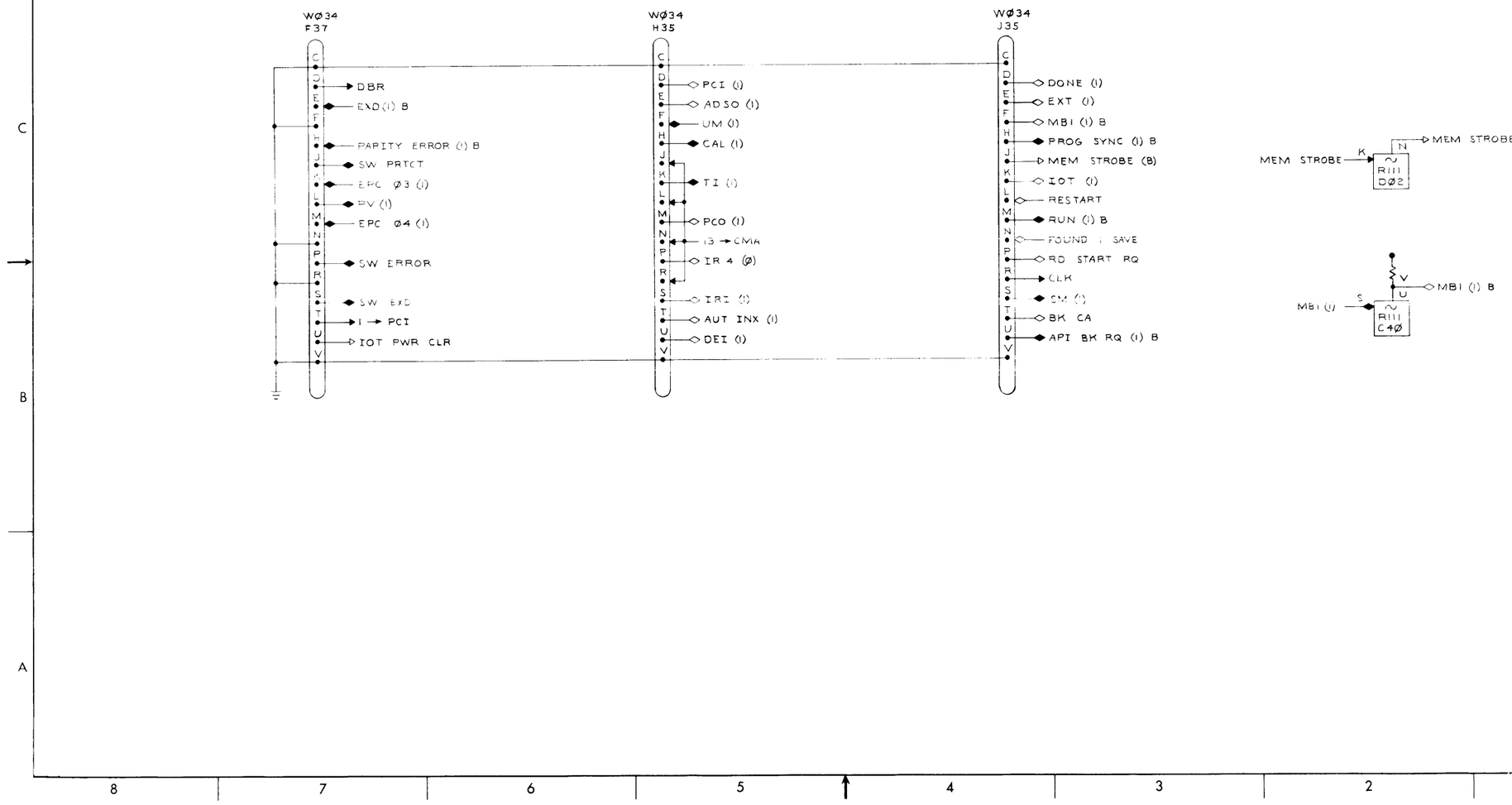
D-BS-KC09-C-26 CP Tester Interface

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
* JUMPER TEMP. 1 (1)	JUMPER		B03T	B03C	
* JUMPER SCO (1)	JUMPER		B31P	B31C	
CM STROBE DLYD	100Ω ½W		F11J	F11C	
CM STROBE D	150Ω ½W		D08H	D08C	
CM STROBE A	100Ω ½W		D22T	D22C	
CM STROBE B	100Ω ½W		D25J	D25C	
CM STROBE C	100Ω ½W		D32J	D32C	
Ø MBI	100Ω ½W		D26R	D27C	
ACI	.001 MFD & 150Ω		J12P	J12C	
F30D	100Ω ½W		E29D	E29C	
CM CLK	100Ω ½W		H01T	H01C	
CM STROBE D	150Ω ½W		E33M	E33C	
STROBE DLYD	100Ω ½W		F09E	F09C	
CP TEST STROBE	100Ω ½W		F28P	F28C	
F30N	100Ω ½W		F29M	F29C	
F32D	100Ω ½W		F33D	F33C	
I/O RESTART	47Ω & .01 MFD		F34D	F34C	
F36N	.010FD 50V		F36N	F36C	
KDPM	15K ½W		F36L	F36B	
LOCK	15K ½W		F36T	F35B	
MEM STROBE	1K ½W		H01P	H01A	
CM STROBE C	100Ω ½W		F15J	F15C	
KMT	15K ½W		H27S	H27B	
CM STROBE B	100Ω ½W		J01E	J02C	
CM STROBE A	100Ω ½W		J01H	J01C	
CLR	100Ω ½W		J01K	H01U	
KXDM RES	15K		J34H	-15V	
KMT RES	15K		H27E	-15V	
E34L RES	100½W & OHMS 10%		E34L	GND	
1 → PCI	100Ω ½W		D21S	D21C	

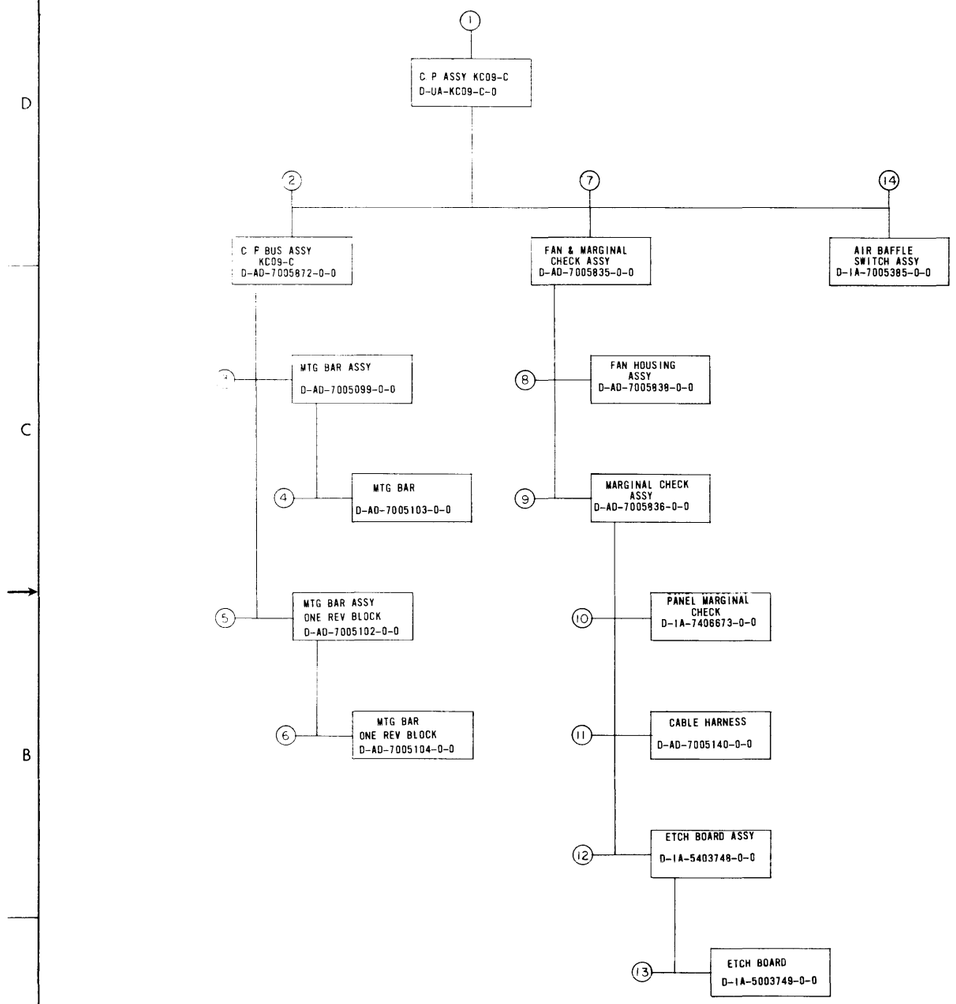
A-CP-KC09-C-27 External Components List for KC09-C (Sheet 1)

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
* JUMPER ADRL (B)	JUMPER		B02D	B03T	
* ACO → LINK	15K ½W		E04R	E04E	
SPEED WIPER	4700PF		J24T	J24C	
MEM STROBE	150Ω ½W		E31R	E31C	
**EXD (1) B	JUMPER		F37E	F36C	
**EPCO3 (1)	JUMPER		F37K	F37C	
**EPCO4 (1)	JUMPER		F37M	F38C	
E32N	100Ω ½W		D24H	D24C	
*F05T	JUMPER		F05T	F05C	
***API BK RQ	JUMPER		F22R	F22C	
EAE-P-PULSE	100Ω ½W		F02J	F02C	
E23N	100Ω ½W		C04J	C04C	
ACI	.001MFD & 150Ω		J12P	J12C	
*** JUMPERS REMOVED WHEN API IS INSTALLED					
** JUMPERS REMOVED WHEN KG09 MEM EXT CONTROL IS INSTALLED					
MEM STROBE	1K ½W		C01T	C01A	
MQI	.001MFD & 150Ω		C37T	C37C	

A-CP-KC09-C-27 External Components List for KC09-C (Sheet 2)



D-BS-KC09-C-28 CP - Memory Extended Parity Interface



MECHANICAL

FIND NO	DESCRIPTION	PART NO	DEPT USAGE PROD	CUST	F/C
1	C/P ASSY KC09-C C/P ASSY KC09-C (PL) C P SWITCH ASSY DECALS	D-UA-KC09-C-0 A-PL-KC09-C-0 A-SS-7405842-0-0			
2	C/P BUS ASSY KC09-C C/P BUS ASSY KC09-C (PL)	D-AD-7005872-0-0 A-PL-7005872-0-0			
3	MTG BAR ASSY 10 BLOCKS MTG BAR ASSY PL	D-AD-7005099-0-0 A-PL-7005099-0-0			
4	MTG BAR STD MTG BAR	D-AD-7005103-0-0 C-MD-7405035-0-0			
5	MTG BAR ASSY ONE REV MTG BAR ASSY (PL)	D-AD-7005102-0-0 A-PL-7005102-0-0			
6	MTG BAR REV MTG BAR	D-AD-7005104-0-0 C-MD-7405035-0-0			
7	FAN & MARGINAL CHECK ASSY FAN & MARGINAL CHECK ASSY (PL)	D-AD-7005835-0-0 A-PL-7005835-0-0			
8	FAN HOUSING ASSY FAN HOUSING ASSY (PL) TERMINAL STRIP CHASSIS FAN HOUSING AIR BAFFLE	D-AD-7005838-0-0 A-PL-7005838-0-0 C-1A-7405083-0-0 E-1A-7406682-0-0 D-MD-7406674-0-0			
9	MARGINAL CHECK ASSY MARGINAL CHECK ASSY (PL) TERM TAB BUSSING WIRE GRN TERM TAB BUSSING WIRE BLU TERM TAB BUSSING WIRE BLK TERM TAB BUSSING WIRE RED TERM TAB BUSSING WIRE ORN AC BUSSING TO FAN (SINGLE) TERM TAB BUSSING WIRE GRN TERM TAB BUSSING WIRE BLU TERM TAB BUSSING WIRE BLK TERM TAB BUSSING WIRE RED TERM TAB BUSSING WIRE ORN AC BUSSING TO FAN (DOUBLE)	D-AD-7005936-0-0 A-PL-7005836-0-0 C-MD-7405089-1-0 E-MD-7405089-2-0 C-MD-7405089-3-0 C-MD-7405089-4-0 C-MD-7405089-5-0 B-MD-7405091-0-0 C-MD-7405379-1-0 C-MD-7405379-2-0 C-MD-7405379-3-0 C-MD-7405379-4-0 C-MD-7405379-5-0 B-MD-7405090-0-0			
10	PANEL MARGINAL CHECK SILK SCREEN	D-1A-7406673-0-0 C-SS-7406673-0-1			
11	CABLE HARNESS CABLE CONNECTOR	D-AD-7005140-0-0 W071			
12	ETCH BOARD ASSY	D-1A-5403748-0-0			
13	ETCH BOARD PC LAYOUT BOARD GLASS EPOXY	D-1A-5003749-0-0 PC-5403748-0-1 1405110-0-0			
14	AIR BAFFLE SWITCH ASSY W023 FLTP CHIP CONN CABLE CLAMP PLATE SWITCH	D-1A-7005385-0-0 5002726-0-0 1202704 B-1A-7405606-0-0			

ELECTRICAL

FIND NO	DESCRIPTION	PART NO	DEPT USAGE PROD	CUST	F C
1	C P SECTION KC09-C REGISTER CONFIGURATION SPECIAL MODULES FETCH FLOW EXECUTION FLOW BREAK FLOW KEY FLOW WIRE LIST KC09-C C P MODULE LIST C/P MODULE LIST C/P & MC SWITCH CONFIGURATION CLOCK,RUN & DISPLAY CLOCK,RUN & DISPLAY TIMING DIAGRAM INSTRUCTION REGISTER OPERATE CONTROL SKIP & C117 LINK CONTROL C M TIMING C M ADDRESSING C M WIRING MATRIX & PROGRAM C M SENSE FLOPS AC,AR,MQ,PC MB & ADDER SHIFT X2 GATES C/P CONSOLE INTERFACE C/P MEMORY INTERFACE C/P-I/O CABLE INTERFACE C/P TESTER INTERFACE EXTERNAL COMPONENTS LIST C/P MEMORY EXTENSION PARITY INTERFACE SIGNAL INDEX THREE CYCLE DCH BREAK FOUR CYCLE DCH BREAK	A-ML-KC09-C D-BS-KC09-C-1 D-BS-KC09-C-2 D-FD-KC09-C-3 D-FD-KC09-C-4 D-FD-KC09-C-5 D-FD-KC09-C-6 K-ML-KC09-C-7 D-MU-KC09-C-8 A-PL-KC09-C-9 D-IC-KC09-C-9 D-BS-KC09-C-10 D-TD-KC09-C-11 D-BS-KC09-C-12 D-BS-KC09-C-13 D-BS-KC09-C-14 D-BS-KC09-C-15 D-BS-KC09-C-16 D-BS-KC09-C-17 D-FD-KC09-C-18 D-BS-KC09-C-19 D-BS-KC09-C-20 D-BS-KC09-C-21 D-BS-KC09-C-22 D-IC-KC09-C-23 D-IC-KC09-C-24 D-IC-KC09-C-25 D-BS-KC09-C-26 A-CP-KC09-C-27 D-CP-KC09-C-28 D-AP-KC09-C-30 D-TD-KC09-C-31 D-TD-KC09-C-32			
	C/P BUS ASSY				
7	FAN & MARGINAL CHECK ASSY	D-AD-7005835-0-0			
8	FAN HOUSING ASSY	D-AD-7005838-0-0			
9	MARGINAL CHECK ASSY	D-AD-7005936-0-0			
11	CABLE HARNESS	D-AD-7005140-0-0			
13	PC LAYOUT	PC-5403748-0-1			
14	AIR BAFFLE SWITCH ASSY	D-1A-7005385-0-0			

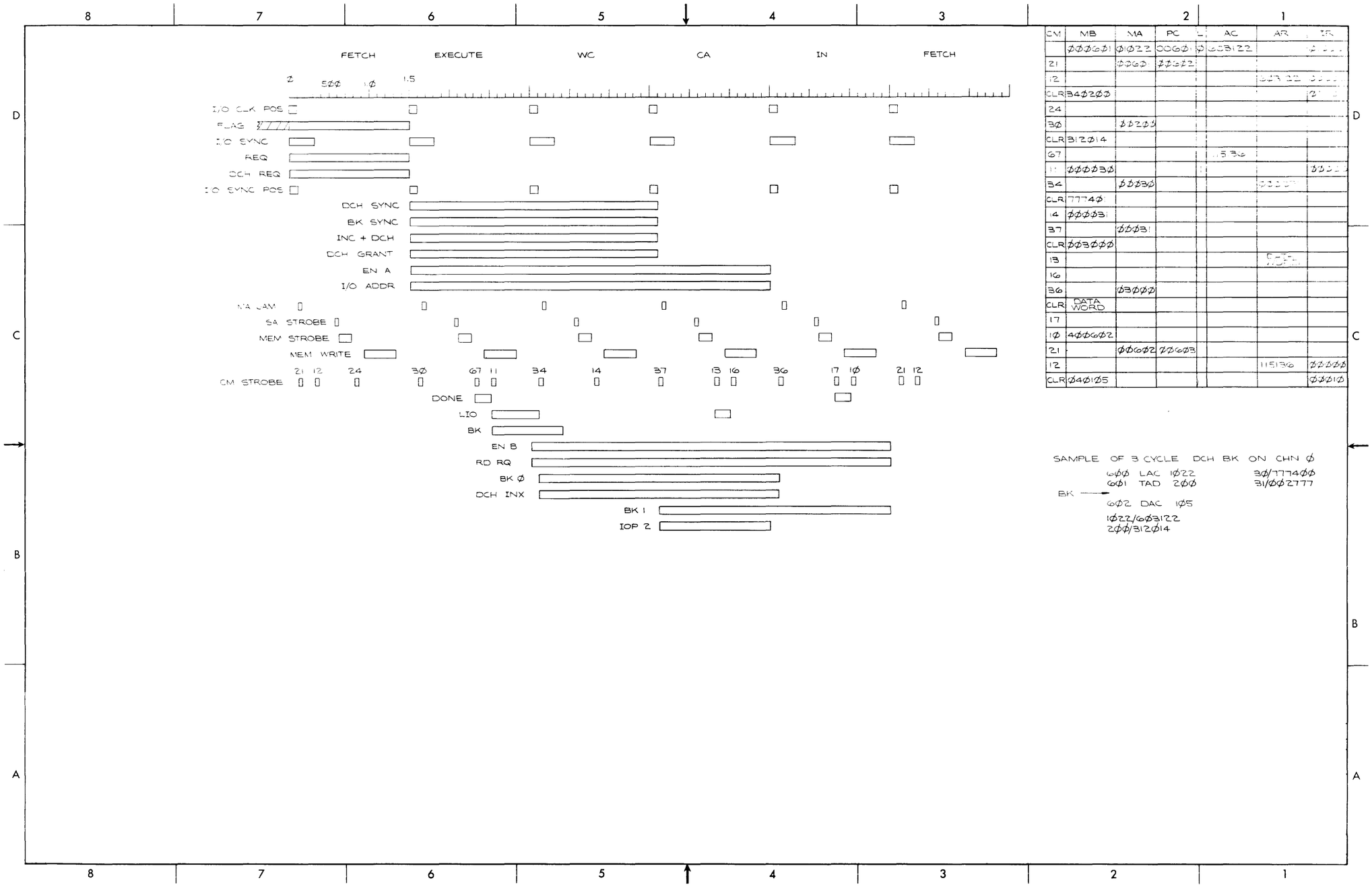
SIGNAL NAME	ORIGIN	DESTINATION
A	10	
A BUS LINK	15,3	
A BUS (00-05)	20-1	
A BUS (06-11)	20-2	
A BUS (12-17)	20-3	
AC RQ	INTERFACE-FROM IO	19-2,25(INTERFACE)
AC SIGN	15	14
AC 0 TO LINK	3	15
AC (00-05)	20-1	3
AC (06-11)	20-2	
AC (12-17)	20-3	
ACD	9-0-3	19-3,23(INTERFACE)
ACI	19-2	3,20-1,20-2,20-3
ACO	19-3	3,20-1,20-2,20-3
AC RQ (B)	19-2	13
ADDR 10	17 3	
ADGF	15	
ADR EQ 0 SAVE	15	14
ADRL	15	22,3,4
ADRL (B)	15	3,
ADR (00-05)	21-1	22,20-1,15
ADR (06-11)	21-2	20-2,22,20-1
ADR (12-17)	21-3	22,20-2,20-3
ADRA (0:5	21-1,21-2	14,15
ADRB (4:5	21-2,21-3	14,15
ADSD	19-2	13,25(INTERFACE)
AM SYNC BUS(0)		25,24(INTERF),16
AND	19-1	21-1-2-3,13
API BK RQ(1:3		17,25(INTERFACE)
API 0	9-0-3	23,25(INTERFACE)
ARD	9-0-3	23(INTERF) 19-3
AR (00-05)	20-1	
AR (06-11)	20-2	
AR (12-17)	20-3	
ARI	19-2	20-1-2-3,15,13, 10- 12-
ARO	19-3	19-3
ARO RESTORE	10-	
AROS	10	
AUT INX	14	
AXS	19-2	14,13,15
B	10	
B BUS (00-05)	21-1	
B BUS (06-11)	21-2	
B BUS (12-17)	21-3	
BK SYNC		25(INTERF),17
BK D(0)B		19-1,19-3,25 (INTERFACE)
BK D(1)B		25(INTER),19-1,13, 14,10
BK 1(0)B		14,25(INTER),17, 10
BK 1(1)B	10	10,19-3,13,15
CAL	12	22,25(INTERF), 26(INTERF)
CI 17	3,14	
CJIT	19-2	14,12
CLK	10	24&25(INTERFACE)
CLK D		
CLK (B)	10	
CLK EN		25&23 (INTERF)
CLK POS	10	25(INTERFACE)
CLK*RUN	10	10
CLL	13	15
CLR	16	26(INTERF),19-3, 19-2
CLRI	19-2	19-3
CM CLK	10	16,26(INTERF)
CM CURRENT	16	26(INTERF),17
CM STROBE A	16	26(INTERF),19-1-2
CM STROBE B	16	26(INTERF),19-3
CM STROBE C	16	19-1-2-3,12
CM STROBE D	16	19-1-2-3,14
CM STROBE DLYD	16	12
CMA (00-05)	19-1	17
CMG (0-7)	17	15
CML	13	

SIGNAL NAME	ORIGIN	DESTINATION
CMP (0-7)	17	
CMPL	13	21-1-2
CMSL (20-35)	17	19-1-2-3
CONT	19-1	3,16
DD Ø1		15
CLR RQ	16	
DASO	13	25(INTERFACE)
DATA OFLO (1)		25(INTERFACE)
DBR		15,25(INTERFACE)
DBR (B)	15	
DCH	19-1	25(INTERF),16,17
DCH INX		25(INTERFACE),14
DEI	19-1	25(INTERFACE),12,16
DMB	19-2	
DIV	4	3
DIV NO GO		3,2
DIV OV	3	2,15
DONE	19-1	10- 17,25(INTERFACE
DPY D	9-0-3	25&23(INTERFACE)
EAE	19-1	25(INTERFACE),3
EAE CLR RQ	3	16
EAE D		23(INTERFACE)
EAE OR ARO	3	19-3
EAE OR MQO	3	19-3
EAE OR SUB	3	19-3
EAE PWR CLR	3	3
EAE RUN	3	3,4
EAE SIGN	3	
EAE STROBE DLYD	16	2,15
EAE OR CONT		19-1
EAE OR LI	3	19-1
EAE OR MBO	3	19-3
EAE P	19-1	2,15,3,4
EAE R	19-1	2,3,15,4
EIR (09-11)	4	
EN CMPL	3	
END BIT 0	15	20-1
END BIT 17	15	20-3
EXT	19-3	25(INTERF),13,16,17, 1 2
FIRST	3	2,4
IAØ	16	
IN CLR	16	19-2
IN SHLI	4,13	26(INTERFACE),15
INC WB		19-1,17,25(INTERFACE)
INC + DCH		17,25(INTERFACE)
IND CLK	10	19-2,16
IND EN	10	23(INTERFACE),9-0-3
IO ADDR D		25&23(INTERFACE)
IO BUS ON	19-3	21-1-2-3
IO BUS (00-05)	21-1	25(INTERFACE)
IO BUS (06-11)	21-2	25(INTERFACE)
IO BUS (12-17)	21-3	25(INTERFACE)
IO BUS (00-05)B		20-1,25(INTERFACE)
IO BUS (06-11)B		20-2,25(INTERFACE)
IO BUS (12-17)B		20-3,25(INTERFACE)
IO RESTART		16,25&26(INTERFACE)
IO SKIP		14,25(INTERFACE)
IOT	12	25&26(INTERFACE)
IOT OR ARO	12	19-3
IOT PWR CLR		14,3,25(INTERFACE)
IR Ø	12	17,26&23(INTERFACE)
IR 1	12	17,26&23(INTERFACE)
IR 2	12	17,26&23(INTERFACE)
IR 3	12	13,26,23(INTERFACE)
IR 4	12	14,17,26(INTERFACE)
IRI	19-1	14,12,16,26,4, 25(INTERFACE)
ISZ	12	14,26(INTERFACE)
+1	19-2	14,15

SIGNAL NAME	ORIGIN	DESTINATION
KCT	9-0-3	10 ,23(INTERFACE)
KCT(B)	10	10 ,23(INTERFACE)
KDN	9-0-3	10 ,23(INTERFACE)
KDP	9-0-3	10 ,23(INTERFACE)
KDP + KDN	10	13
KDP + KDN + RI	19-3	13
KDPW	9-0-5	10 ,25(INTERFACE)
KEN	9-0-3	23(INTERFACE),10
KEY	19-2	16,15,13,17, 25(INTERFACE)
KEY BUS	10	
KEY BUS(B)	10	
KEY DLY	10-	25(INTERFACE)
KEX	9-0-3	10 ,23(INTERFACE)
KEY INIT POS	10	19-1,26(INTERF),16
KEY(KDP + KDN)	13	19-3
KIO	9-0-3	10 ,25&26(INTERF)
KIOA3	10	17
KIOA4	10	17
KIOA5	10	17
KMT	9-0-5	10
KRI	9-0-3	10 ,23&25(INTERF)
KSP	9-0-3	10 ,23(INTERF)
KST	9-0-3	10 ,23(INTERF)
KXDM		25(INTERF),10
LAR	15	15
LI	19-1	15,3
LINK	15	15,25(INTERF),20-1
LIO	13	20-1-2-3
LOCK	9-0-5	25(INTERF),10
LOT	12	
LRS		4
MB(00-05)	21-1	25&24 (INTERF),3, 14,15,12
MB(06-11)	21-2	14,24&25(INTERF), 3,13
MB(12-17)	21-3	24&25(INTERF),2, 10 ,13
MBI	19-2	21-1-2-3,13,16
MBI(1)B		
MBO	19-3	21-1-2-3
MEM STROBE		16,24&26(INTERF)
MEM STROBE(B)	28	
MQ D	9-0-3	19-3,23(INTERF)
MQ SIGN	3	
MQI	19-2	3,20-1-2-3
MQO	19-3	20-1-2-3
MUL	4	3
NORM	4	2
NOSH	13	20-1-2-3
O BUS L	15	3
O BUS(00-05)	20-1,22	21-1,2
O BUS(06-11)	20-2,22	21-2
O BUS(12-17)	20-3,22	21-3
O BUS 17(B)	3	3
ODD ADDR	17,3	
OFLO	14,15	25(INTERF),15
OP	12	13,10-
OR ACI	12	19-2
OR MBO	12	19-3
PC D	9-0-3	19-3,23(INTERF)
PC 05	20-1	
PC(06-11)	20-2	20-2
PC(12-17)	20-3	
PCI	19-2	20-1-2-3,14
PCO	19-3	20-1-2-3,10
PCO RESTORE	10-	19-3
PCOS	10	
PIE		25(INTERF),12

SIGNAL NAME	ORIGIN	DESTINATION
PKCLR	10	19-1,12,24(INTERF)
PROG SY(1)B		25(INTERF)
PROG SYNC(1)B		25(INTERF)
PV	12	12,25(INTERF),19-2
PWR OK	10	24(INTERF)
RD RQ(B)		19-3,25(INTERF)
RD START RQ	10	10
RDR D	9-0-3	23&25(INTERF)
RDR FLG(B)		10 ,25(INTERF)
RDR HOLE 7C		10 ,25(INTERF)
REP	12	26(INTERF),17
REPT	10	10 ,23(INTERF)
REPT CLK	10	
RESTART		16
RESTART MODE	16	
RI 1(1)B		10 ,25(INTERF)
RI 2(1)B		10 ,19-3,17, 25(INTERF)
RQ MBI	19-2	
R-PULSE	2	
RUN	10	
RUN(1)B	10	
SA(00-04)		12
SA(00-05)		21-1,24(INTERF)
SA(06-11)		21-2,24(INTERF)
SA(12-17)		21-3,24(INTERF)
SAO	19-3	21-1-2-3,26,15,14
SAO(B)B	15	
SC CLR	2	2
SC FULL	2	
SC(12-17)	2	2,22
SCD	2	22
SCDV	2	2,3,4
SCOV 2	2	4,3
SEN	10	10
SEN(1)B	10	23&25(INTERFACE)
SET UP	4	2 3
SHIFT	15	15,13
SHL 1	13	15,20-1-2-3
SHL 2	13	15,22
SHR 1	13	15,20-1-2-3
SHR 2	13	15,22
SKIP	14	14
SKP I	19-1	14
SM	19-2	16,24(INTERF)
SPEED WIPER		10 ,23(INTERF)
SPEED (2-4)		10 ,23(INTERF)
STATUS D	9-0-3	23&25(INTERF)
STROBE DLYD	16	26
SU (1-3)	3	2,3
SUB	19-3	3,21-1-2-3,15
CLK OFF		23&25(INTERF)
SW ERROR		23(INTERF)
SW EXD		23(INTERF)
SW PRTCT		23(INTERF)
SW REPT		23(INTERF),10
SW SGL INST		23(INTERF),10
SW SGL STP		23(INTERF)
SYNC POINT	26	
TEMP 1	3	15
TEMP 2	3	15
TEMP 3	3	15
TEST PARITY		24(INTERF)
TESTER		16,26(INTERF)
TESTER CLR		12,(INTERF)
TI	19-1	17,22,14
TTI D	9-0-3	23&25(INTERF)
TT HD		23 & 24(INTERF)
UM	12	10 ,23&25(INTERF)

SIGNAL NAME	ORIGIN	DESTINATION
WR RQ		19-1-3,10- 25(INTERF)
Ø TO CMA		19-1
Ø TO MBI	19-2	19-1
1 TO MBI	19-2	
1 TO PCI	12	19-2
13 TO CMA		19-1

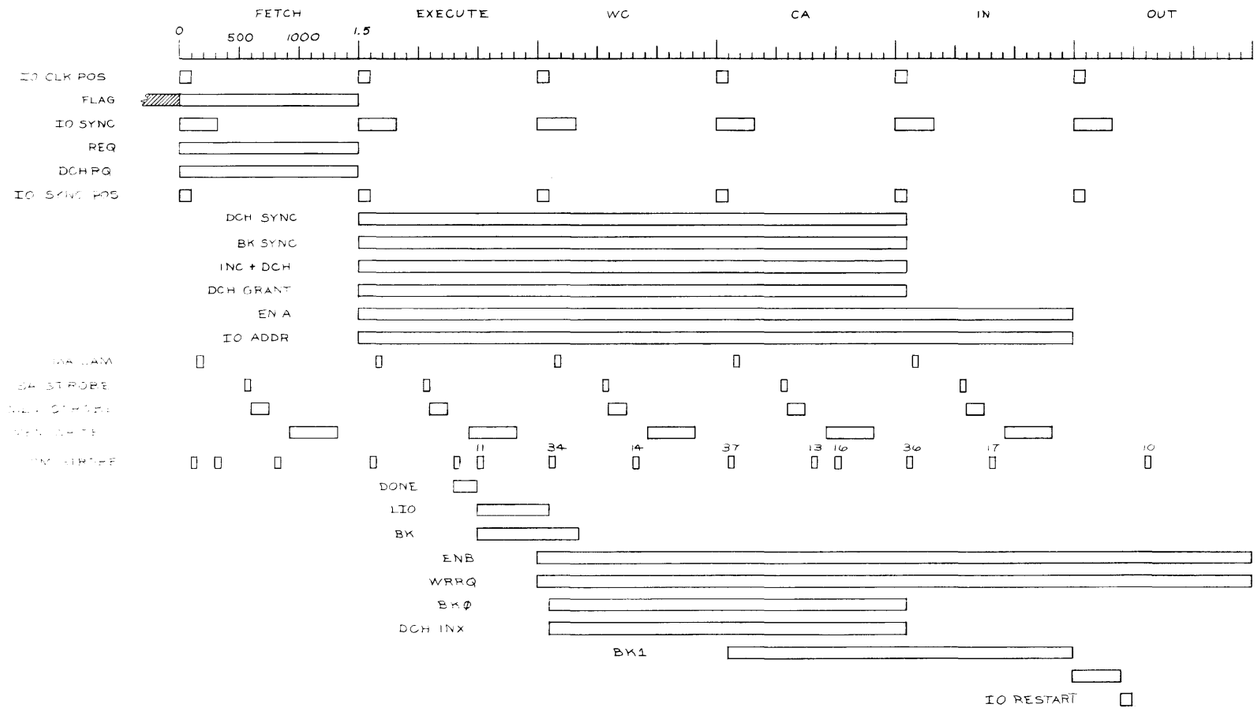


CM	MB	MA	PC	L	AC	AR	IR
	ØØØ6Ø1	Ø1Ø22	ØØ6Ø1	Ø	6Ø3122		Ø [illegible]
21		ØØ6Ø1	Ø1Ø22				
12						6Ø3122 [illegible]	
CLR	34Ø2ØØ						Ø [illegible]
24							
3Ø		ØØ2ØØ					
CLR	312Ø14						
67					1536		
11	ØØØØ3Ø						ØØ22 [illegible]
34		ØØØ3Ø				Ø22 [illegible]	
CLR	77774Ø						
14	ØØØØ31						
37		ØØØ31					
CLR	ØØ3ØØØ						
13						[illegible]	
16							
36		Ø3ØØØ					
CLR	DATA WORD						
17							
1Ø	4ØØ6Ø2						
21		ØØ6Ø2	ØØ6Ø3				
12						115136	ØØØØØ
CLR	Ø4Ø1Ø5						ØØØ1Ø

SAMPLE OF 3 CYCLE DCH BK ON CHN Ø

6ØØ LAC 1Ø22 — 3Ø/7774ØØ
6Ø1 TAD 2ØØ — 31/ØØ2777
BK → 6Ø2 DAC 1Ø5
1Ø22/6Ø3122
2ØØ/312Ø14

D-TD-KC09-C-31 Three Cycle DCH Break



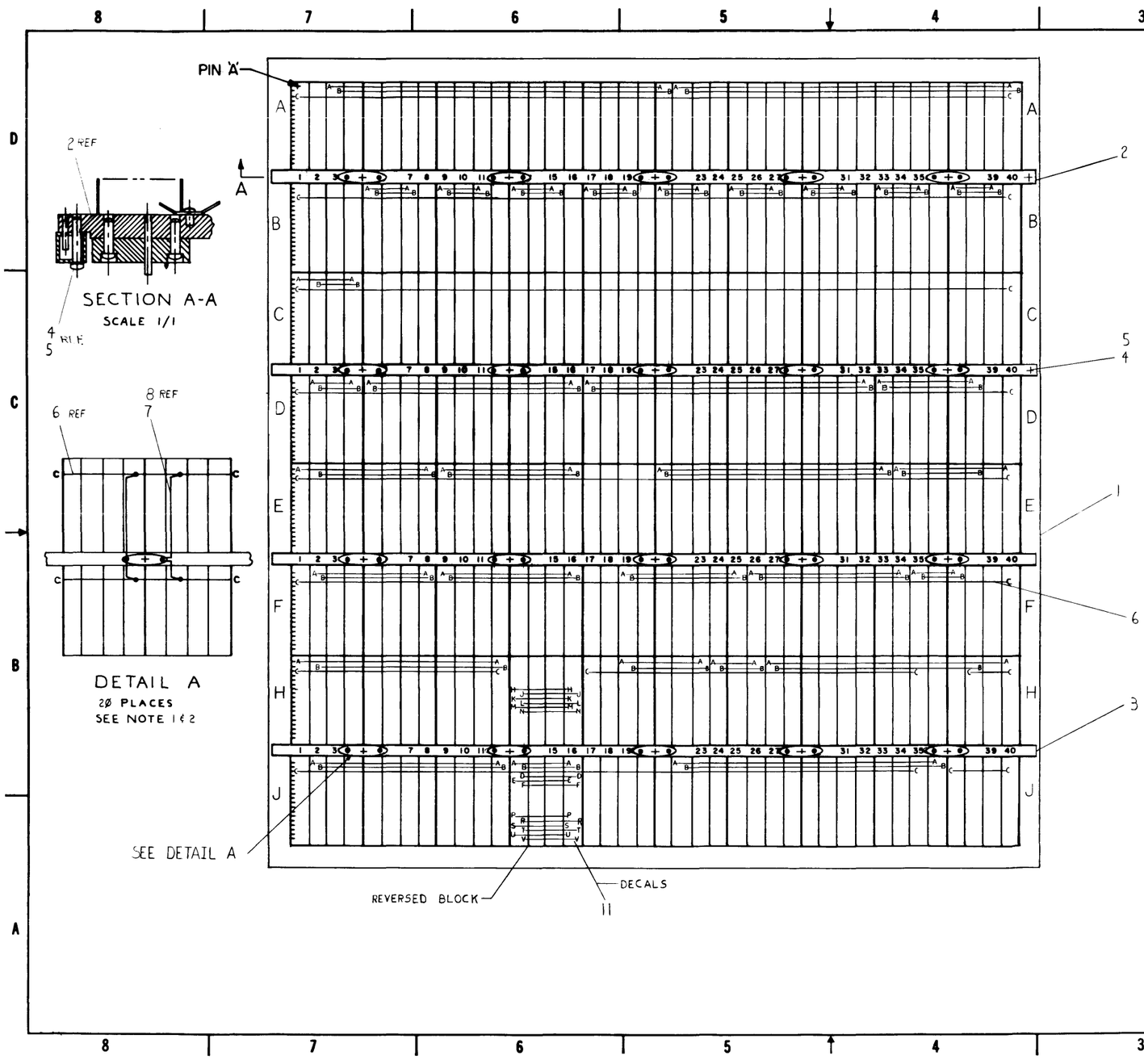
D-TD-KC09-C-32 Four Cycle DCH Break

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION
1	E-IA-7405034-0-0	DOOR FRAME	1
2	D-AD-7005099-0-0	MTG BAR ASSY (CONN. BLOCKS)	3
3	D-AD-7005102-0-0	MTG BAR ASSY (ONE REVERSE BLOCK)	1
4	9006043-1	SCREW PHIL PAN HD #8-32 x 1 SST	8
5	9006634	WASHER LOCK INT TOOTH # SST	8
6	1202188	VOLTAGE CHAIN	A/R
7	9107560-1	#22 AWG SOLID WIRE	A/R
8	9107265	#22 AWG SLEEVING (WHT)	A/R
9	9107470-5	#24 AWG SOLID KYNAR YEL	A/R
10	9107470-10	#24 AWG SOLID KYNAR BLU	A/R
11	A-DC-7406747-0-0	DECALS, REVERSED BLOCK	A/R
	KC09-C-7	WIRE LIST KC09-C	REF
	KC09-C-27	EXTERNAL COMPONENTS LIST	REF

A-PL-7005872-0-0 Central Processor Bus Assembly



NOTES:

1) ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN
2) CONNECTIONS ON ITEMS #6+7 TO BE LOCATED & SOLDERED AT MINIMUM PRACTICAL HEIGHT ABOVE BLOCK.
3) USE YELLOW WIRES, ITEM #9 FOR MACHINE WRAPPED WIRING & BLUE WIRE ITEM #10 FOR HAND WRAPPED WIRING.

EXTERNAL COMPONENT WIRING

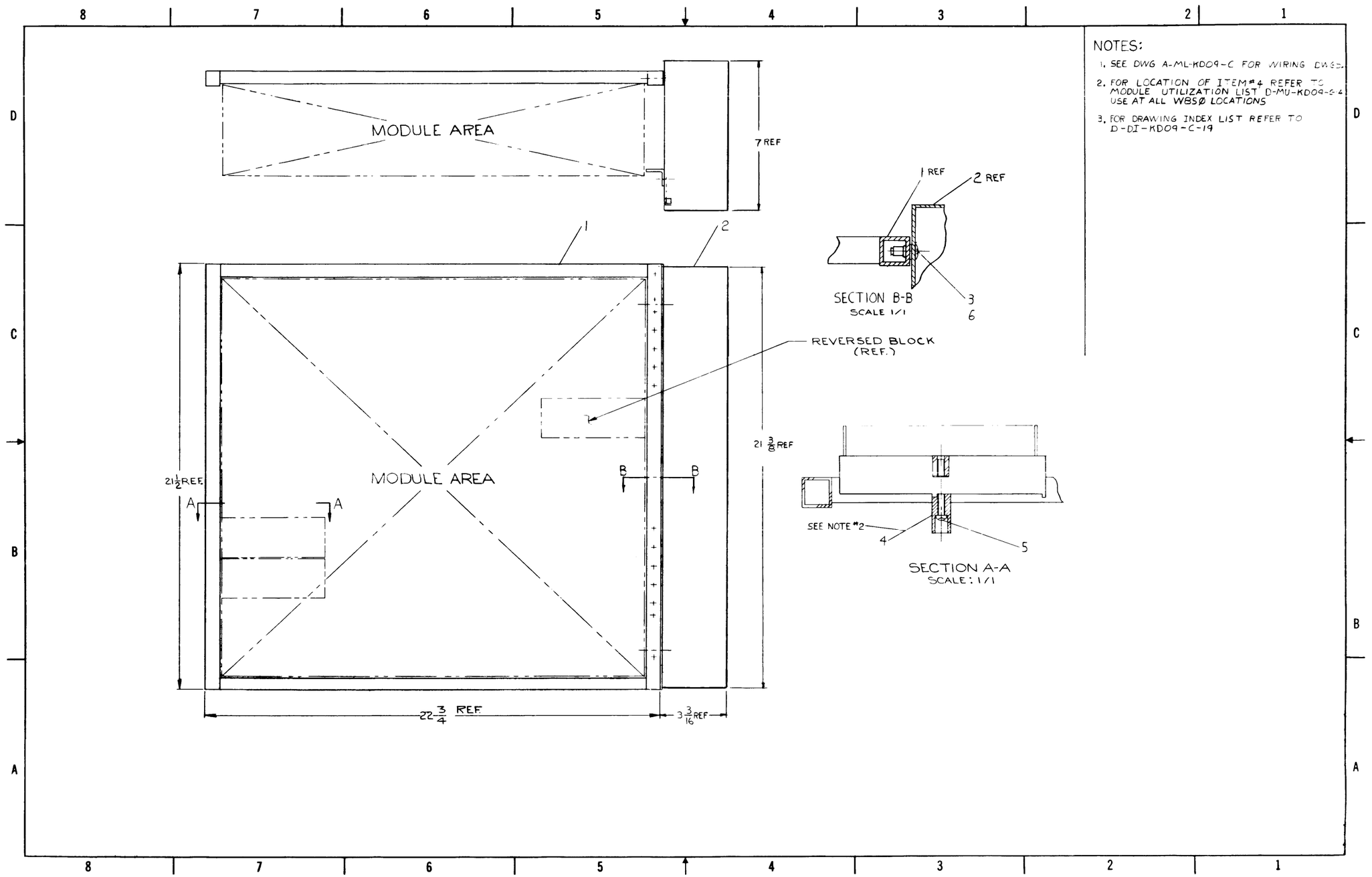
FROM: PIN	TO: PIN	RESISTOR		
A03L	A05K	100Ω	1/4W	5%
A05L	A07K			
A07L	A09K			
A09L	A11K			
A11L	A13K			
A13L	A15K			
A15L	A17K			
A17L	A19K			
A19L	A21K			
A21L	A23K			
A23L	A25K			
A25L	A27K			
A27L	A29K			
A29L	A31K			
A31L	A33K			
A33L	A35K			
A35L	A37K			
A37L	A39K	100Ω		
A39L	A40H	180Ω	1/4W	5%

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

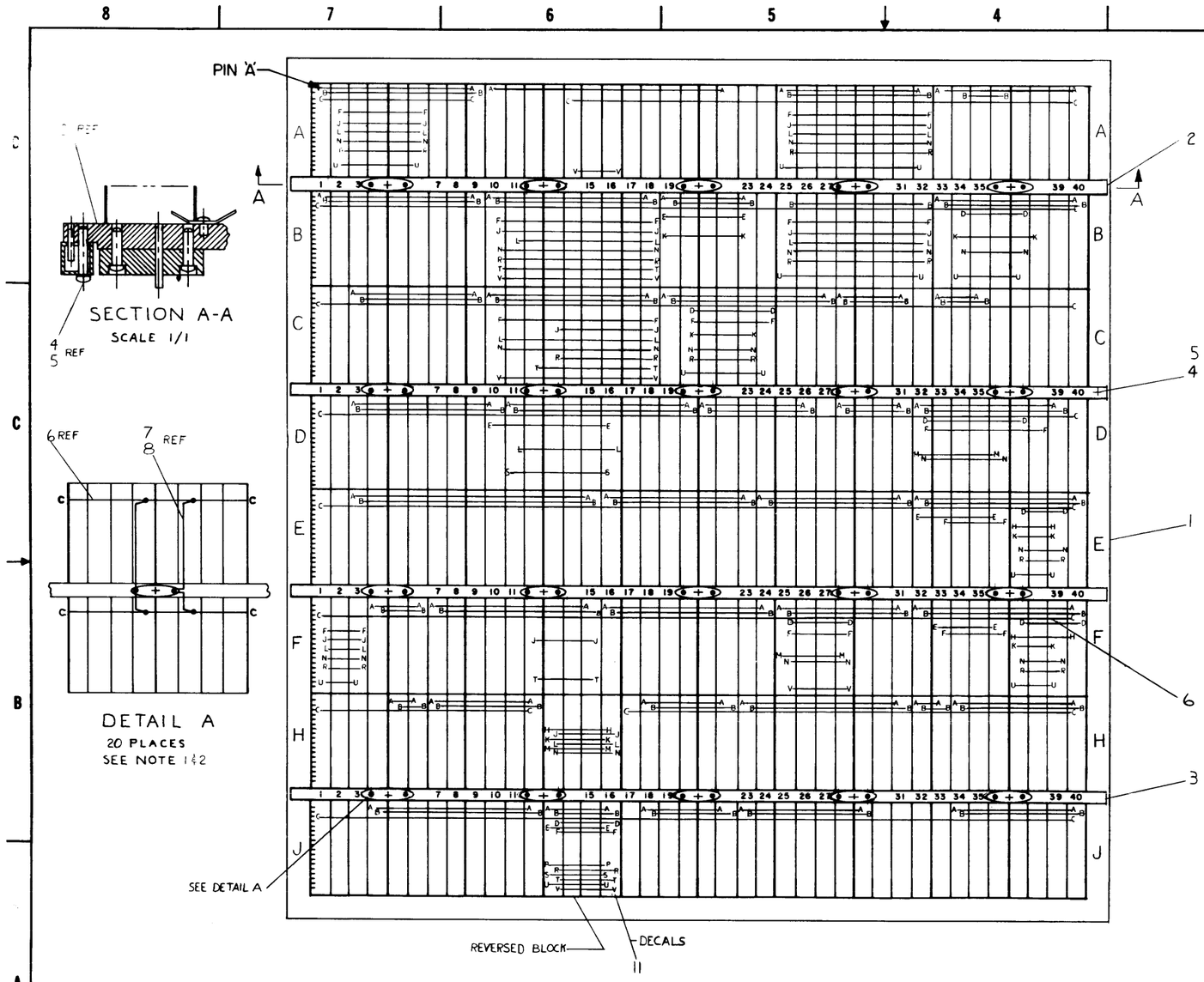
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION
1	D-AD-7005873-0-0	I/O BUS ASSY KD09-C	1
2	D-AD-7005835-0-0	FAN & MARGINAL CHECK ASSY	1
3	9006058-1	SCR PHL HD PAN ¼-20 x 3/4 LG.	1
4	B-MD-7406047-0-0	BLOCK RETAINER	1
5	9007800	SCR POSIDRIVE FILL HD #8-32 x ½	2
6	9006637	INT TOOTH LOCK WASHER	1

A-PL-KD09-C-0 I/O Assembly KD09-C



NOTES:

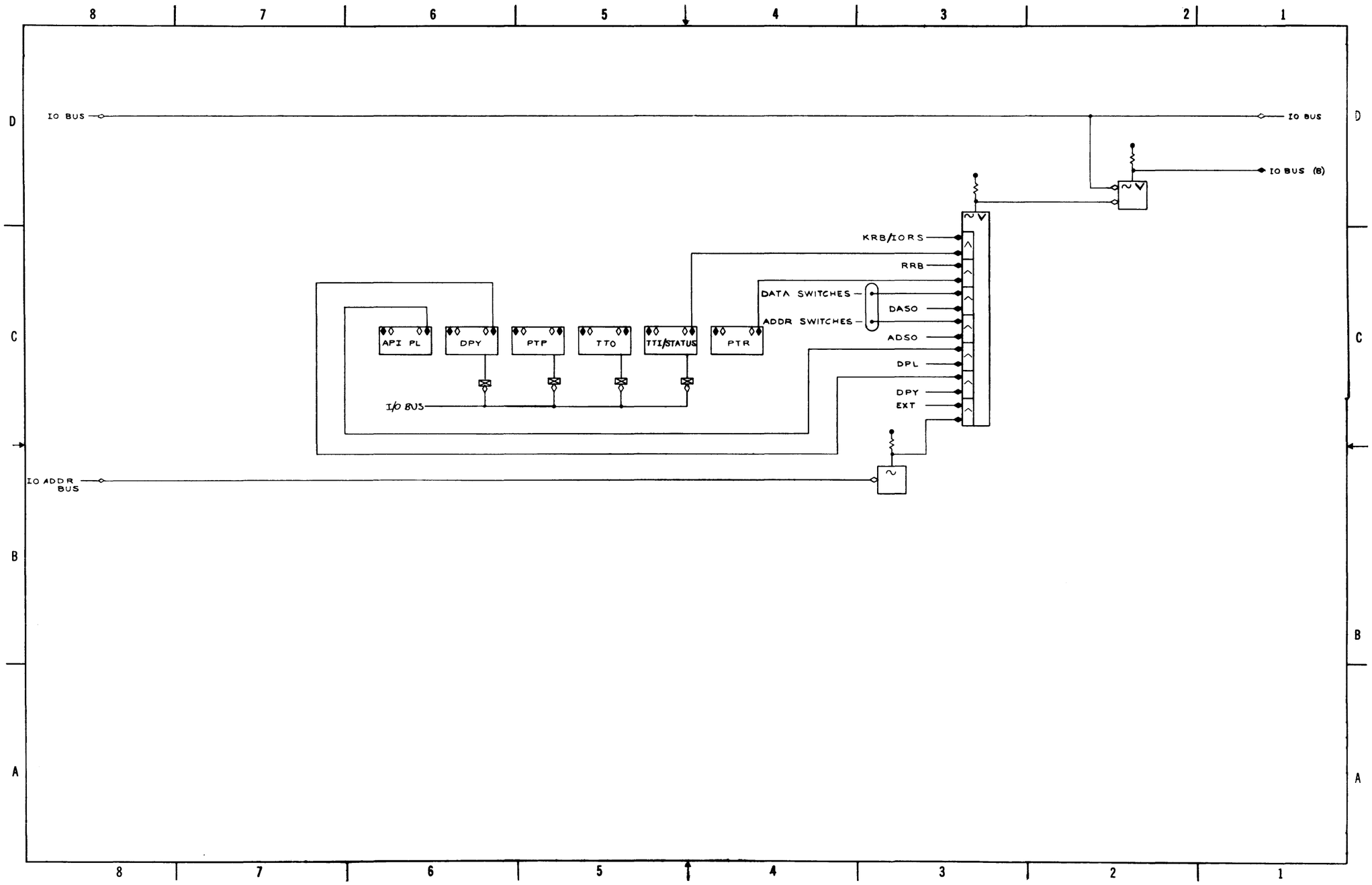
1. SEE DWG A-ML-KD09-C FOR WIRING DWGS.
2. FOR LOCATION OF ITEM #4 REFER TO MODULE UTILIZATION LIST D-MU-KD09-S-4 USE AT ALL WBSØ LOCATIONS
3. FOR DRAWING INDEX LIST REFER TO D-DI-KD09-C-19


PIN 'A'
A
A
SECTION A-A
SCALE 1/1
4 REF
5 REF
6 REF
7 REF
8 REF
DETAIL A
20 PLACES
SEE NOTE 1&2
SEE DETAIL A
REVERSED BLOCK
DECALS
11
2
5
4
1
6
3
NOTES:
1. ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN
2. CONNECTION ON ITEMS #6 & 7 TO BE LOCATED & SOLDERED AT MIN PRACTICAL HEIGHT ABOVE BLOCK
3. USE YELLOW WIRE ITEM #9 FOR MACHINE WRAPPED WIRING & BLUE WIRE ITEM #10 FOR HAND WRAPPED WIRING

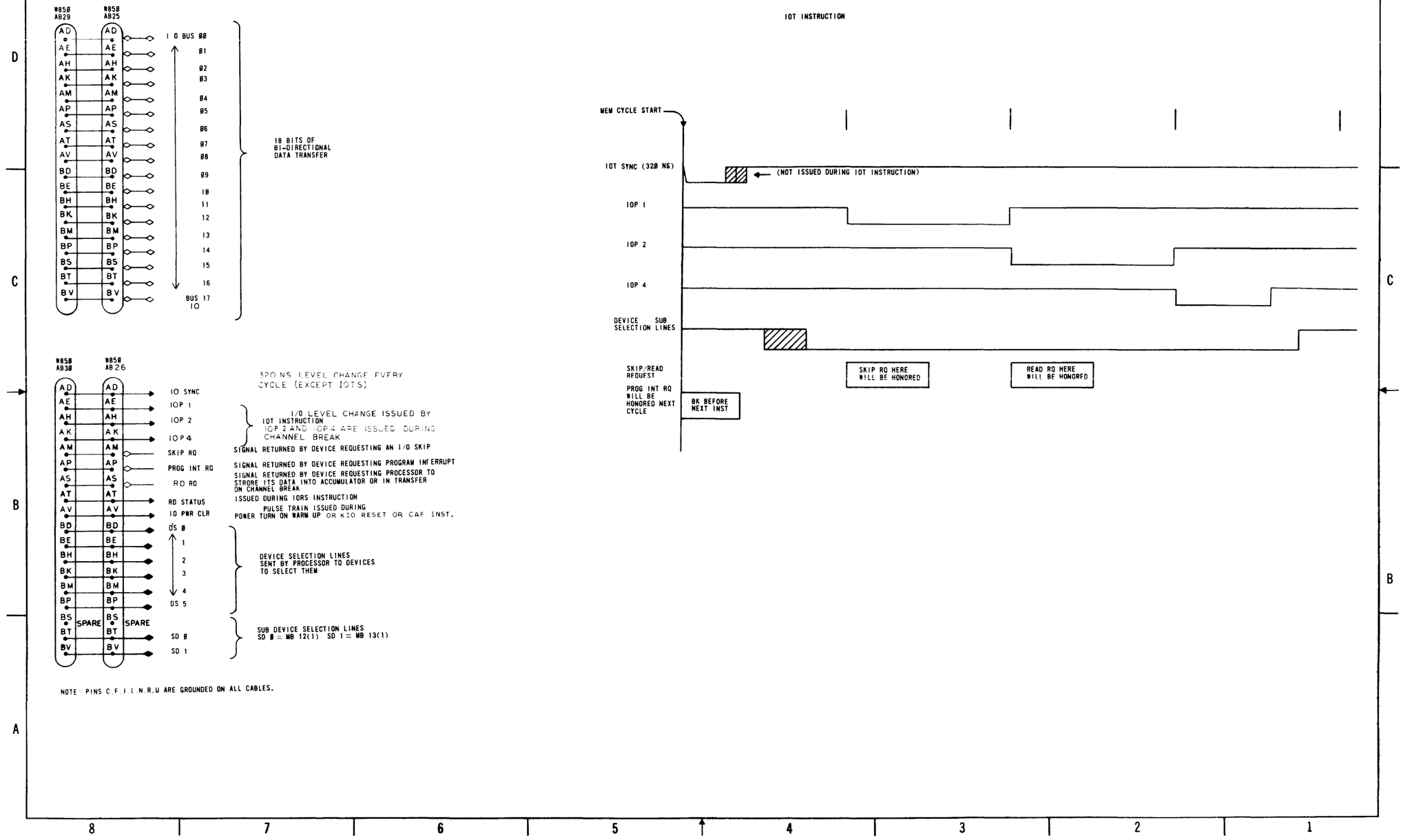
DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION
1	E-IA-7405034-0-0	DOOR FRAME	1
2	D-AD-7005099-0-0	MTG BAR ASSY (CONN.BLOCK)	3
3	D-AD-7005102-0-0	MTG BAR ASSY (ONE REVERSE BLOCK)	1
4	9006043-1	SCREW PHIL PAN HD #8-32 x 1 SST	8
5	9006634	WASHER LOCK INT TOOTH # SST	8
6	1202188	VOLTAGE CHAIN	A/R
7	9107560-1	#22 AWG SOLID WIRE	A/R
8	9107265	#22 AWG SLEEVING (WHT)	A/R
9	9107470-5	#24 AWG SOLID KYNAR YEL	A/R
10	9107470-10	#24 AWG SOLID KYNAR BLU	A/R
11	A-DC-7406747-0-0	DECALS,REVERSED BLOCK	A/R
	K-WL-KD09-C-15	WIRE LIST KD09-C	REF
	A-CP-KD09-C-16	EXTERNAL COMPONENTS LIST	REF

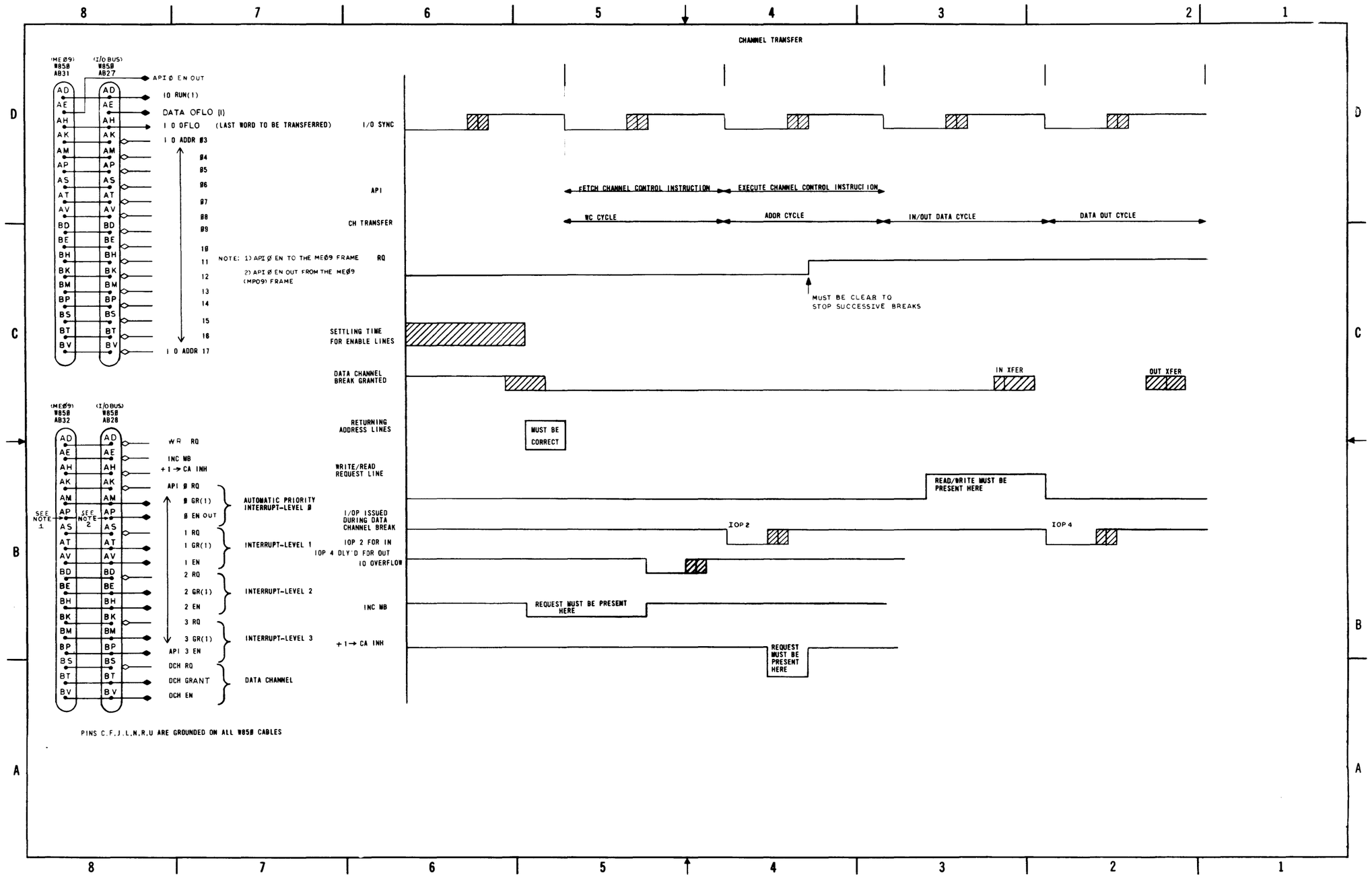
A-PL-7005873-0-0 I/O Bus Assembly KD09



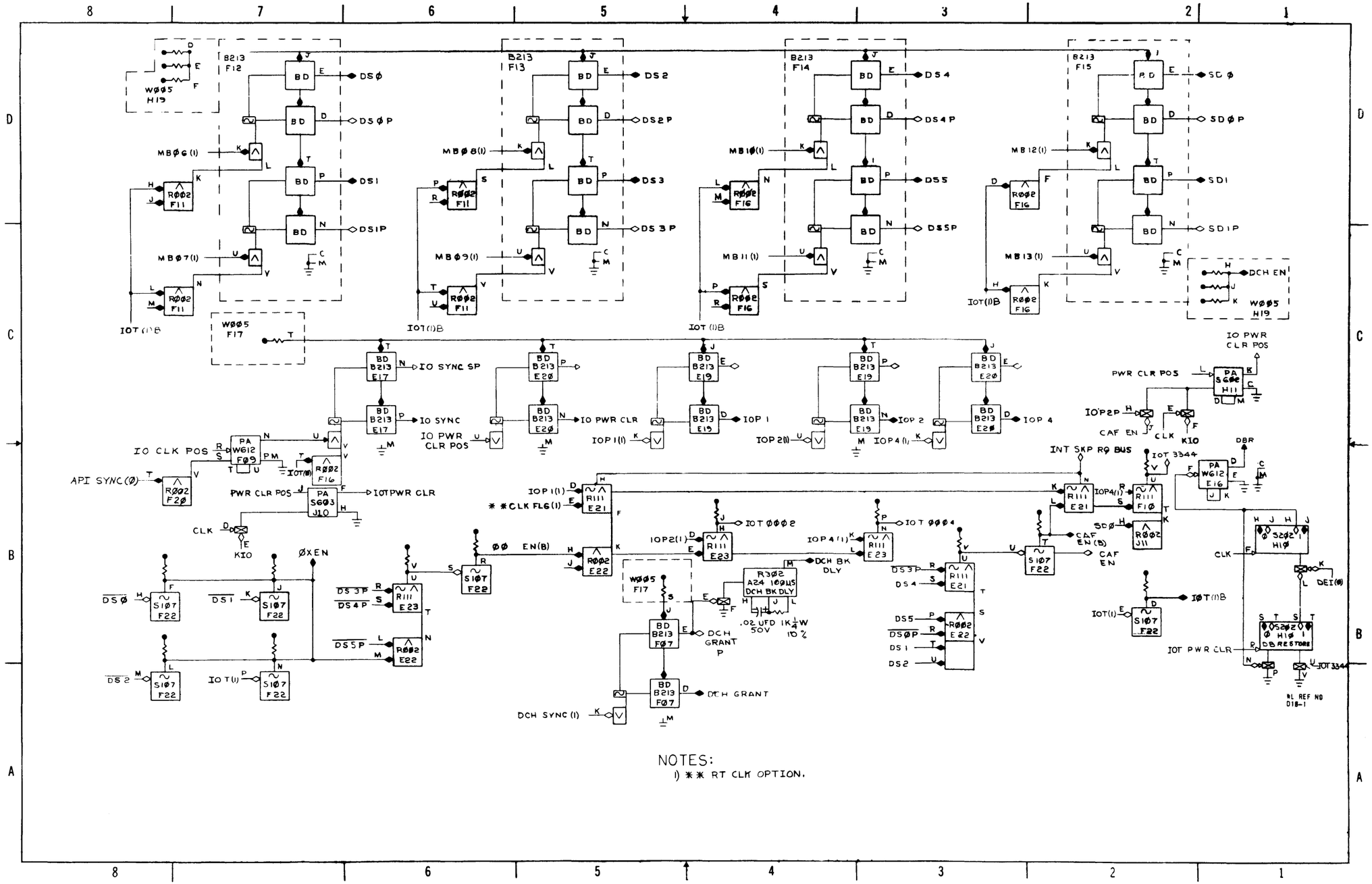
D-BS-KD09-C-1 IO Configuration



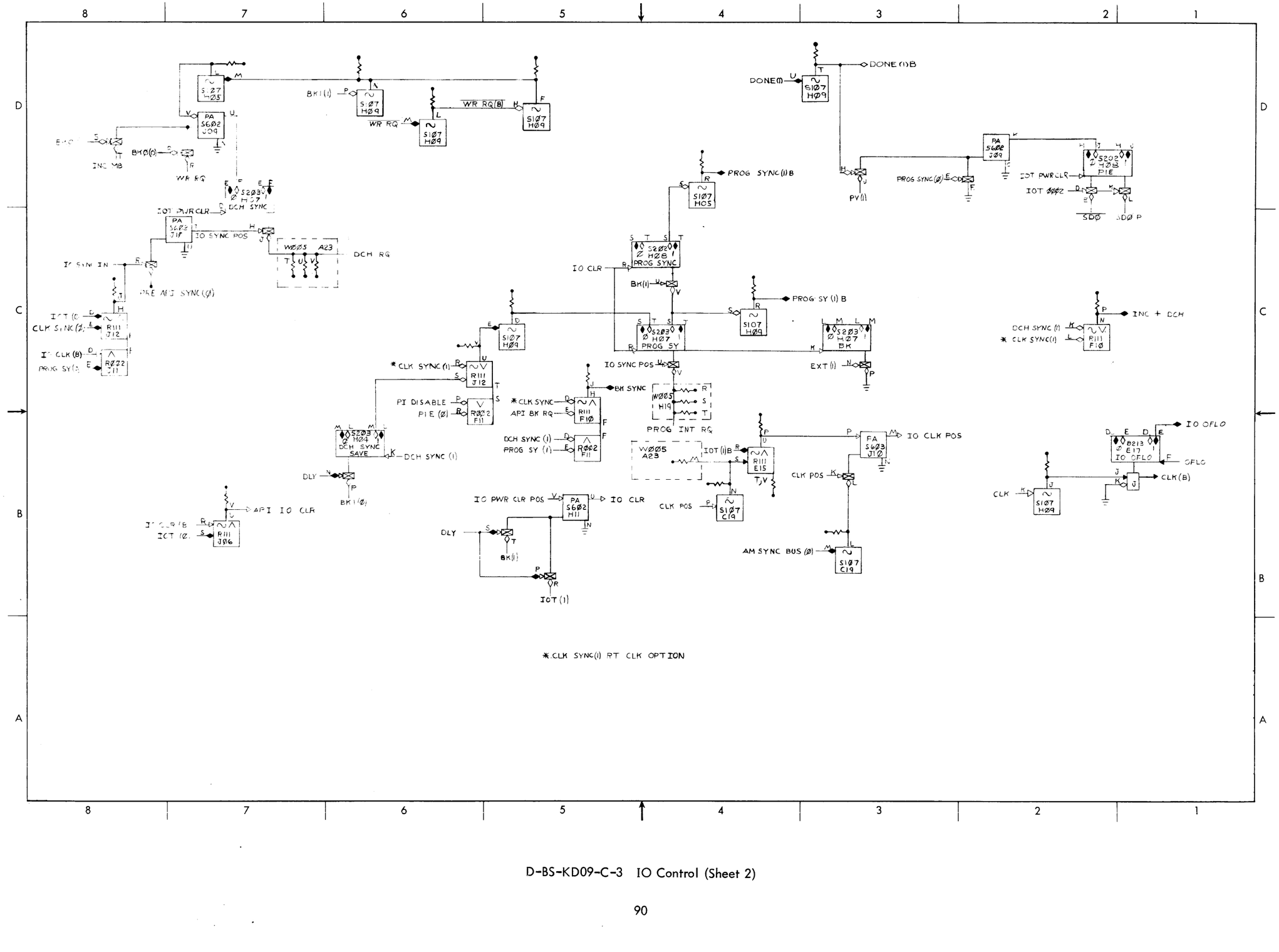
D-TD-KD09-C-2 IO Bus Interface (Sheet 1)



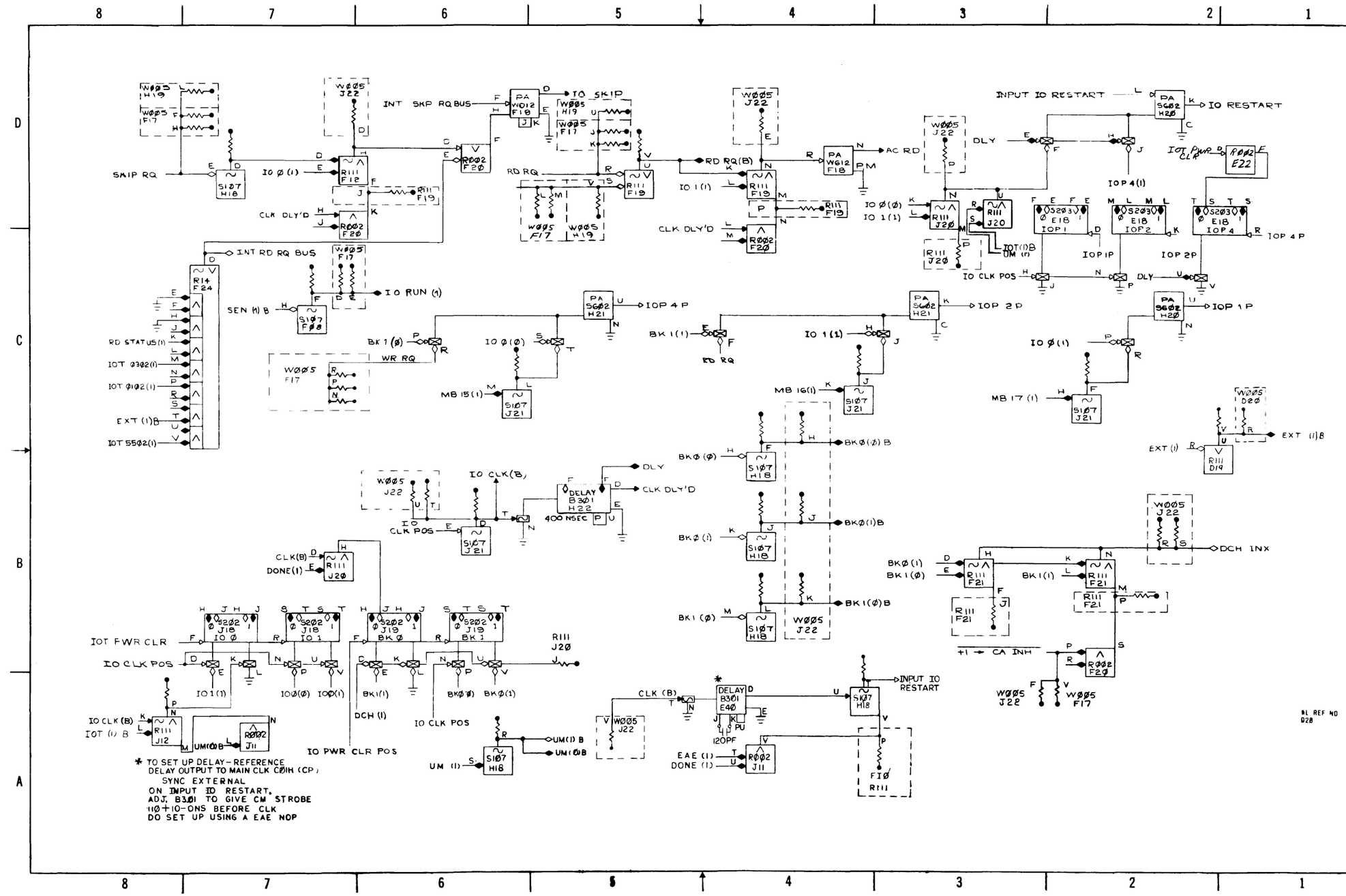
D-TD-KD09-C-2 IO Bus Interface (Sheet 2)



D-BS-KD09-C-3 IO Control (Sheet 1)

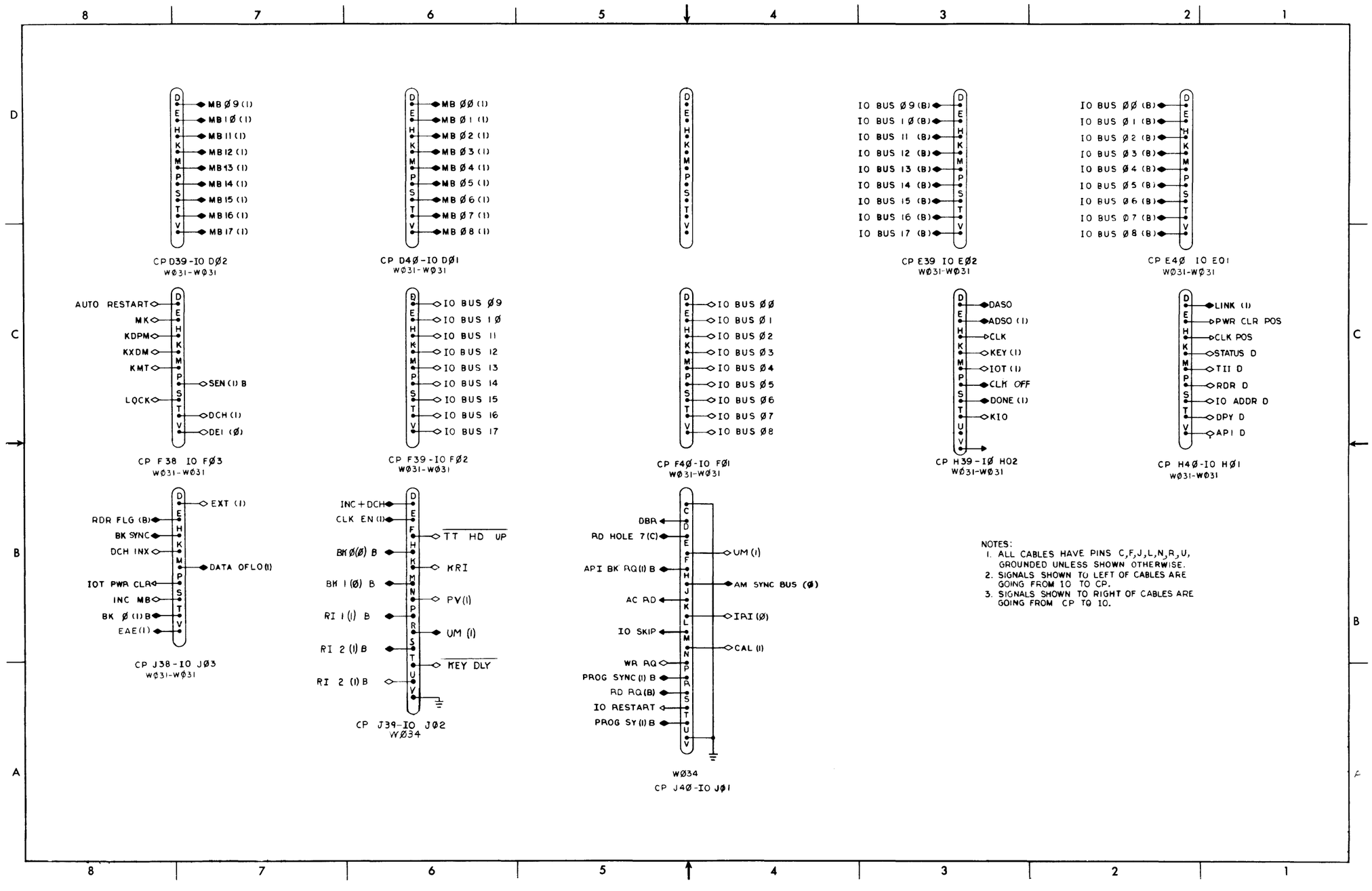


D-BS-KD09-C-3 IO Control (Sheet 2)



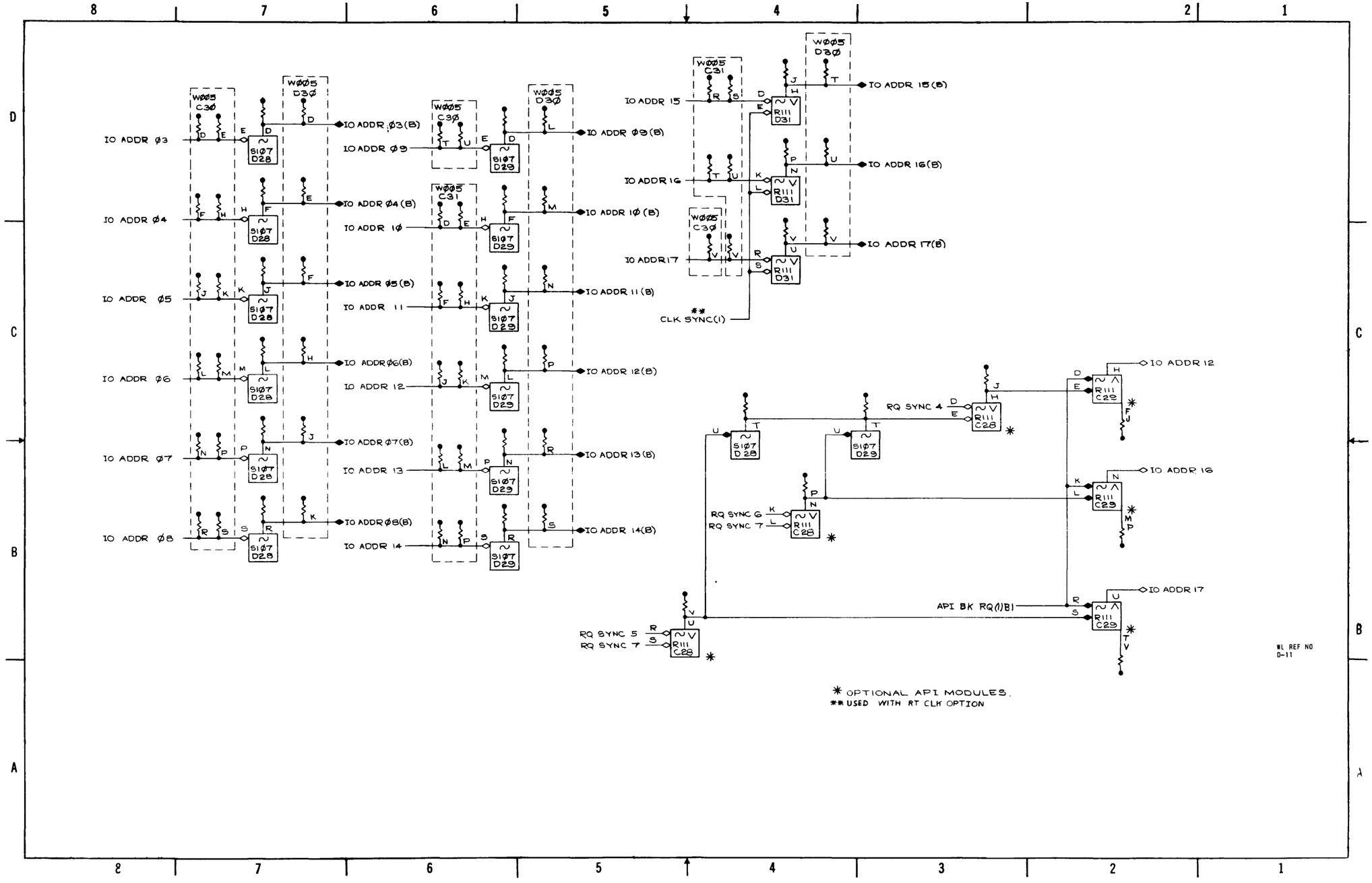
* TO SET UP DELAY-REFERENCE
DELAY OUTPUT TO MAIN CLK COIH (CP)
SYNC EXTERNAL
ON INPUT IO RESTART,
ADJ. B3Ø1 TO GIVE CM STROBE
11Ø+1Ø-ONS BEFORE CLK
DO SET UP USING A EAE NOP

D-BS-KD09-C-3 IO Control (Sheet 3)

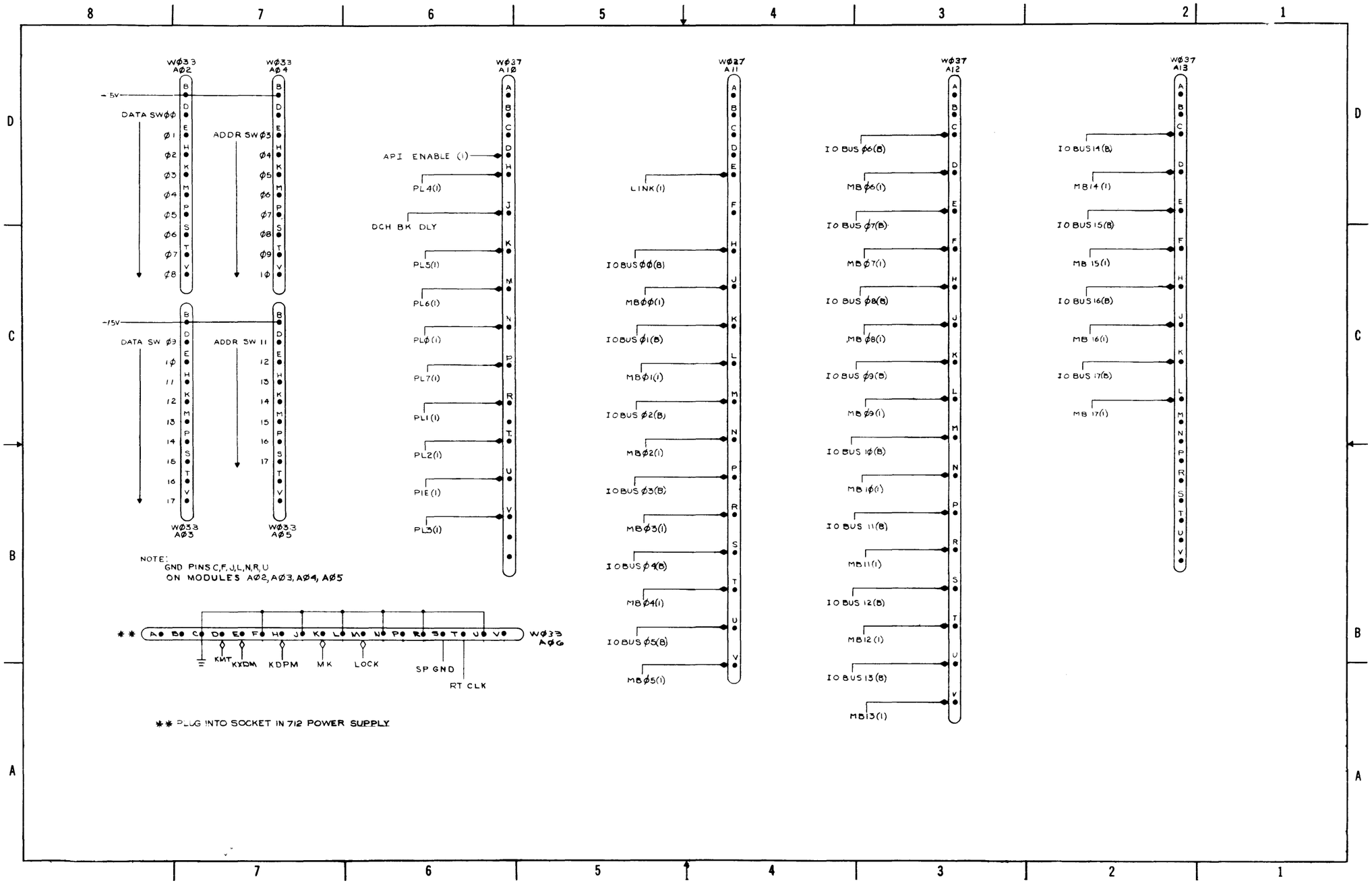


NOTES:
1. ALL CABLES HAVE PINS C,F,J,L,N,R,U, GROUNDED UNLESS SHOWN OTHERWISE.
2. SIGNALS SHOWN TO LEFT OF CABLES ARE GOING FROM IO TO CP.
3. SIGNALS SHOWN TO RIGHT OF CABLES ARE GOING FROM CP TO IO.

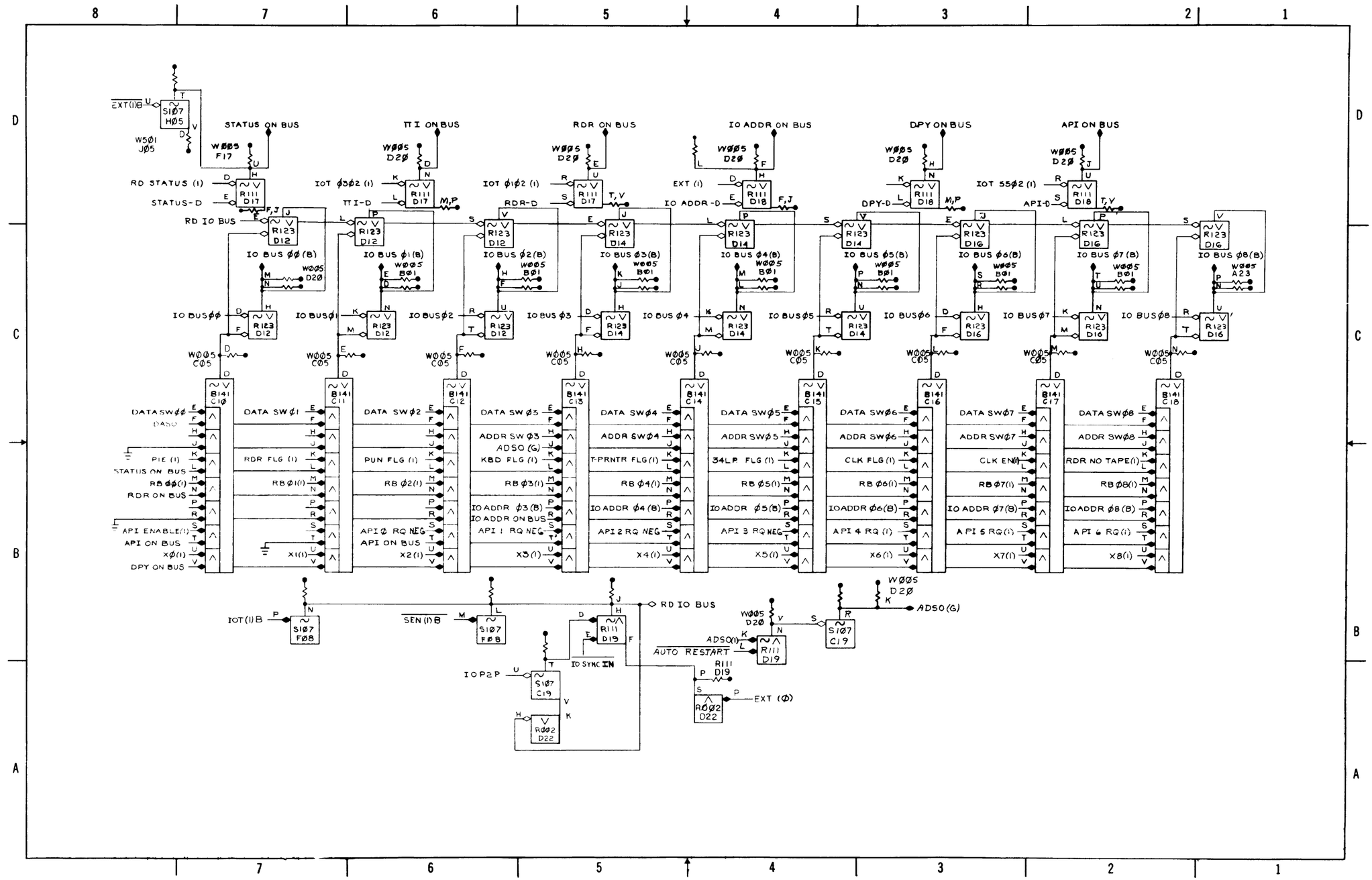
D-IC-KD09-C-4 CP - IO Cable Interface



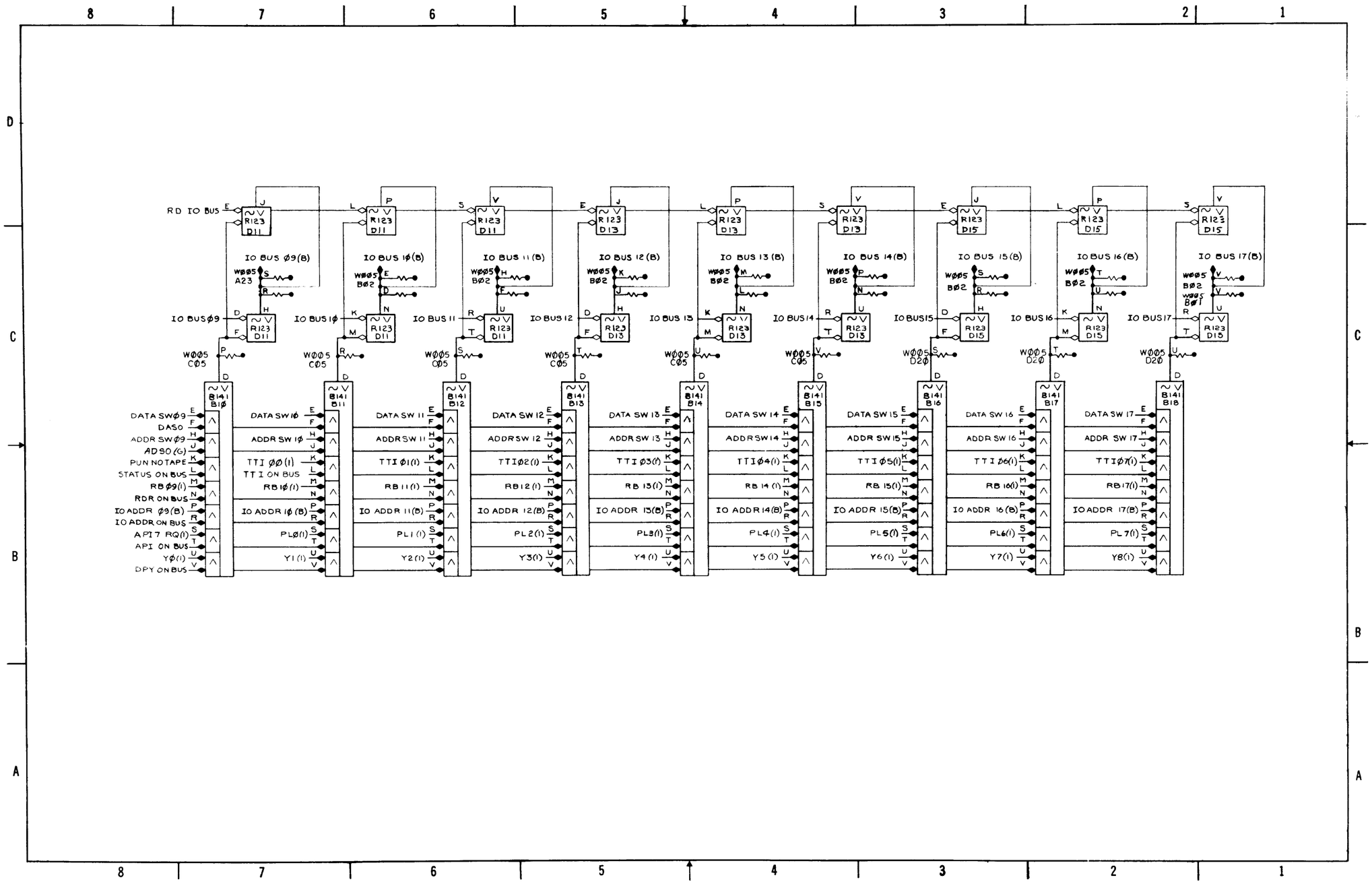
D-BS-KD09-C-5 ADDR Bus



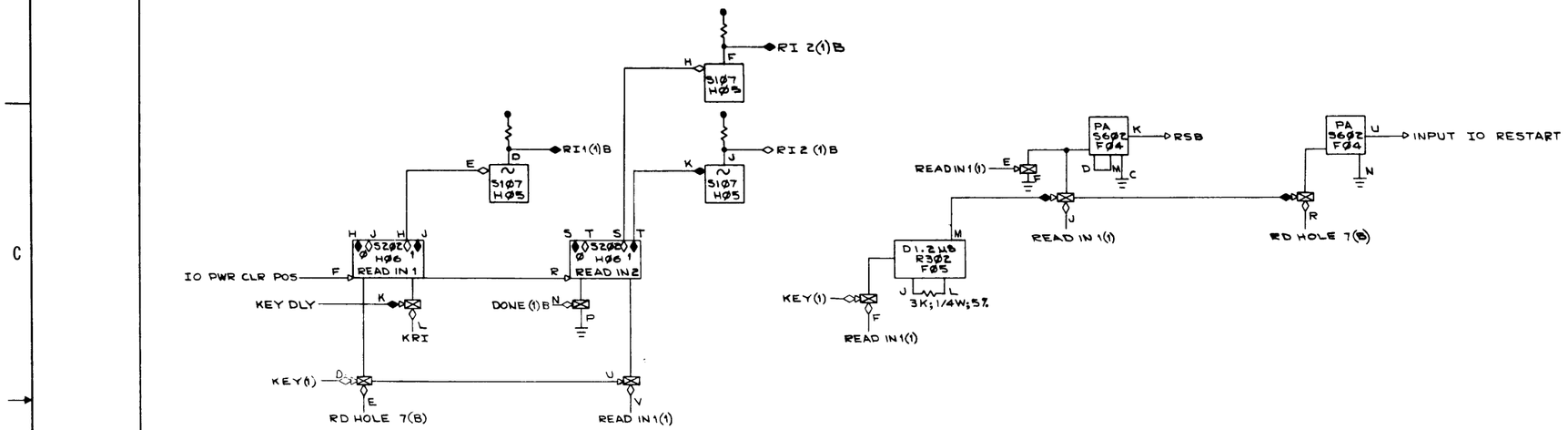
D-BS-KD09-C-6 IO/Console Interface



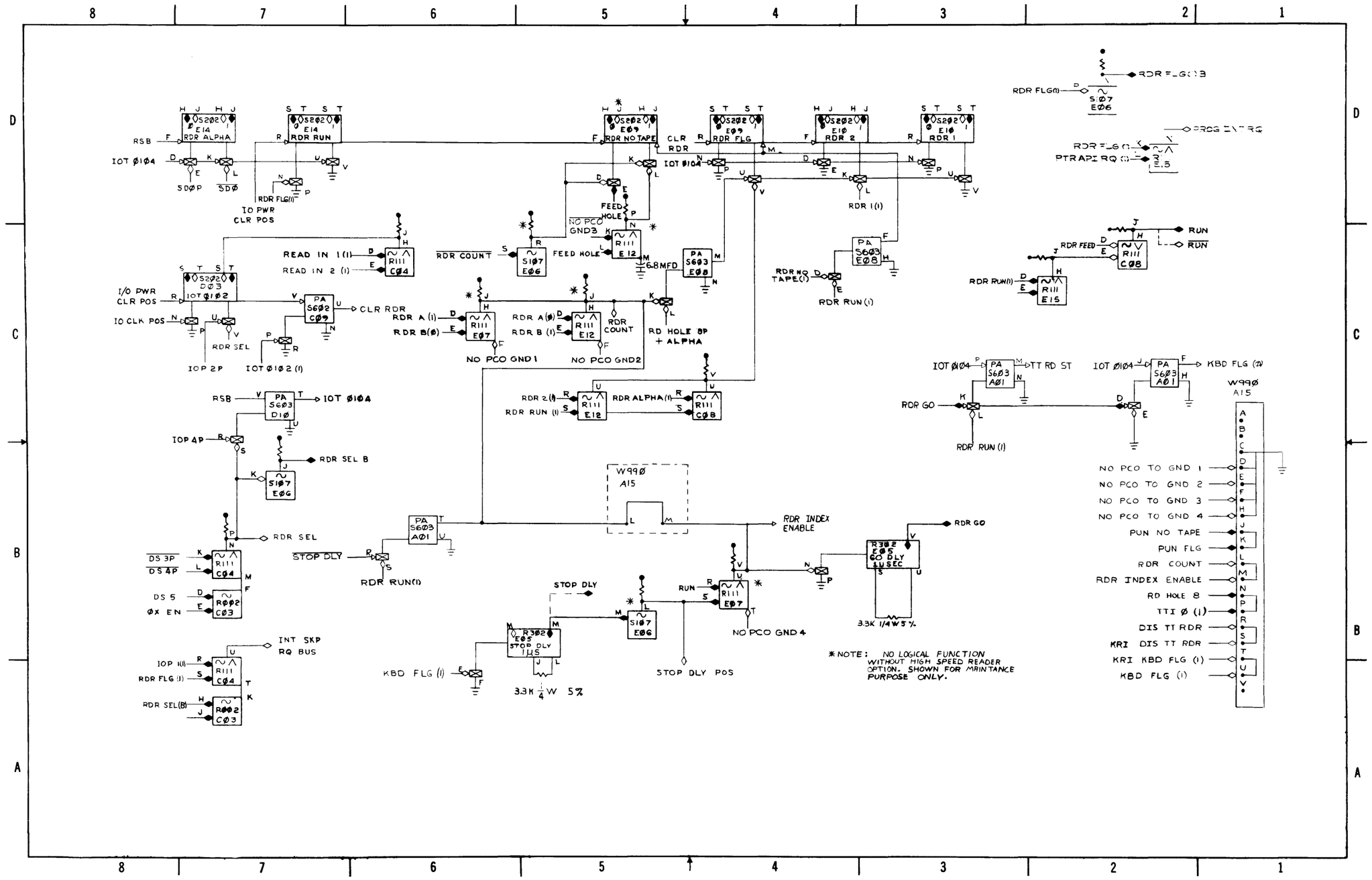
D-BS-KD09-C-7 Input Mixer (Sheet 1)



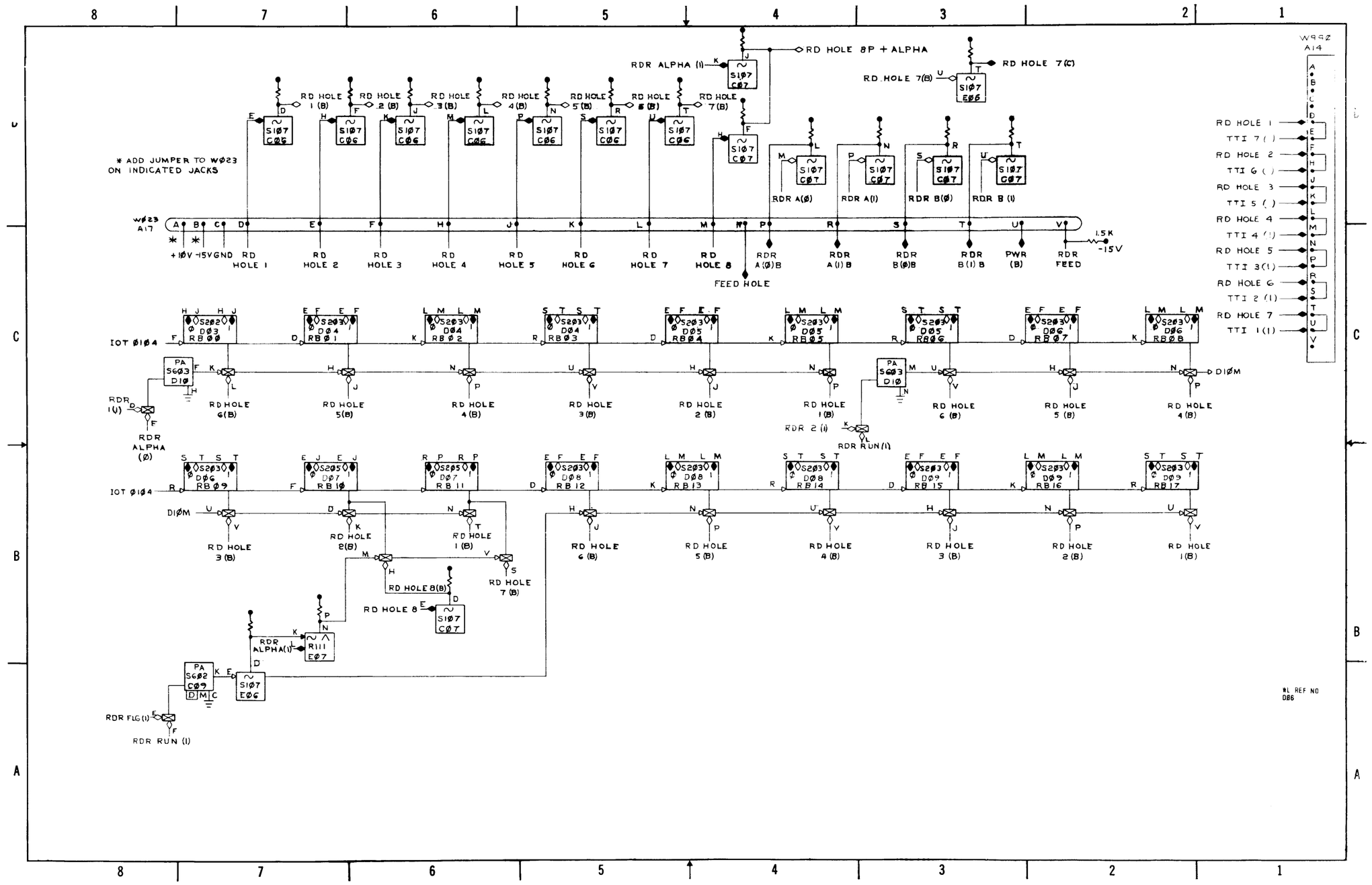
D-BS-KD09-C-7 Input Mixer (Sheet 2)



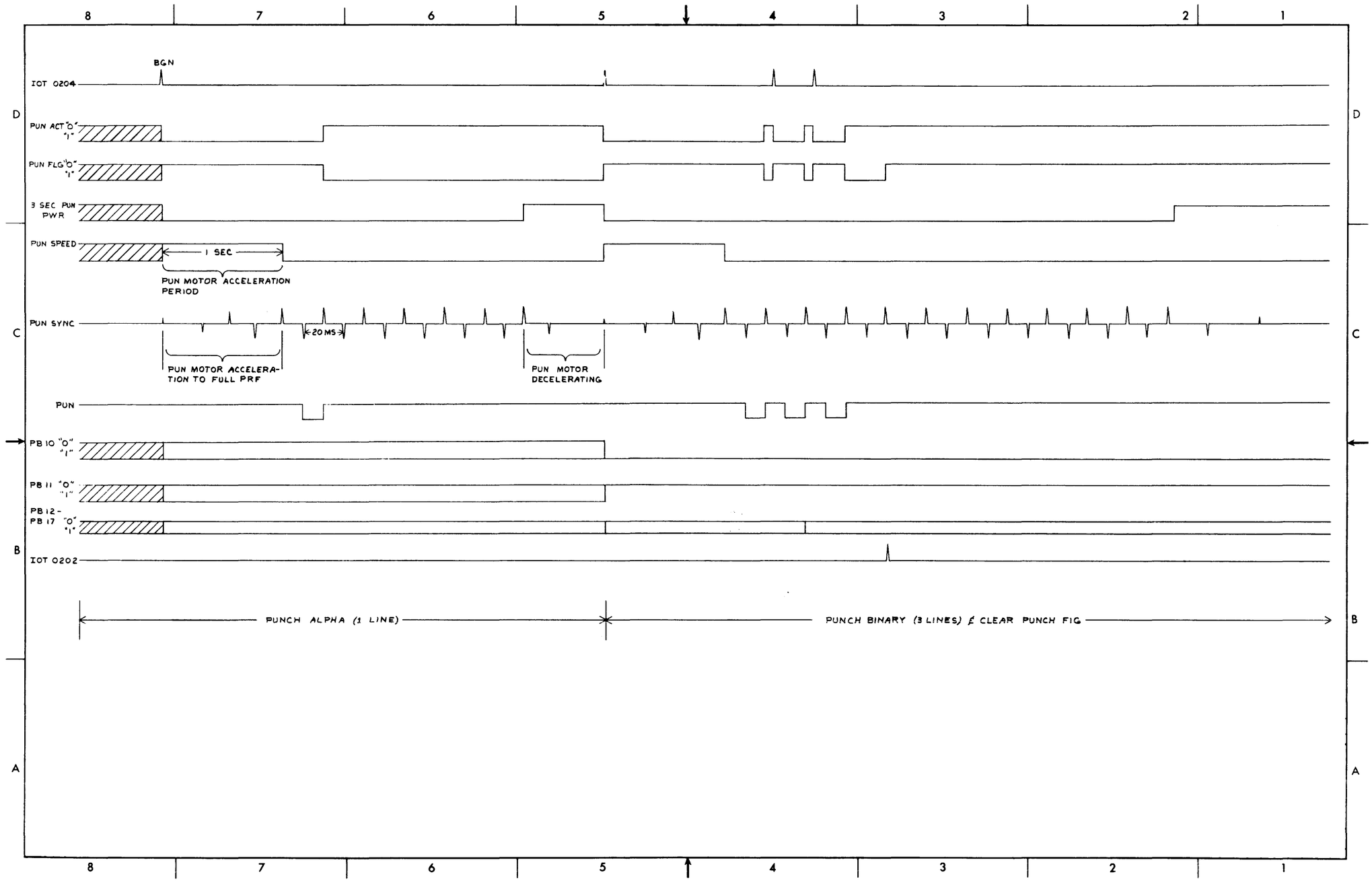
D-BS-KD09-C-8 Read In Mode



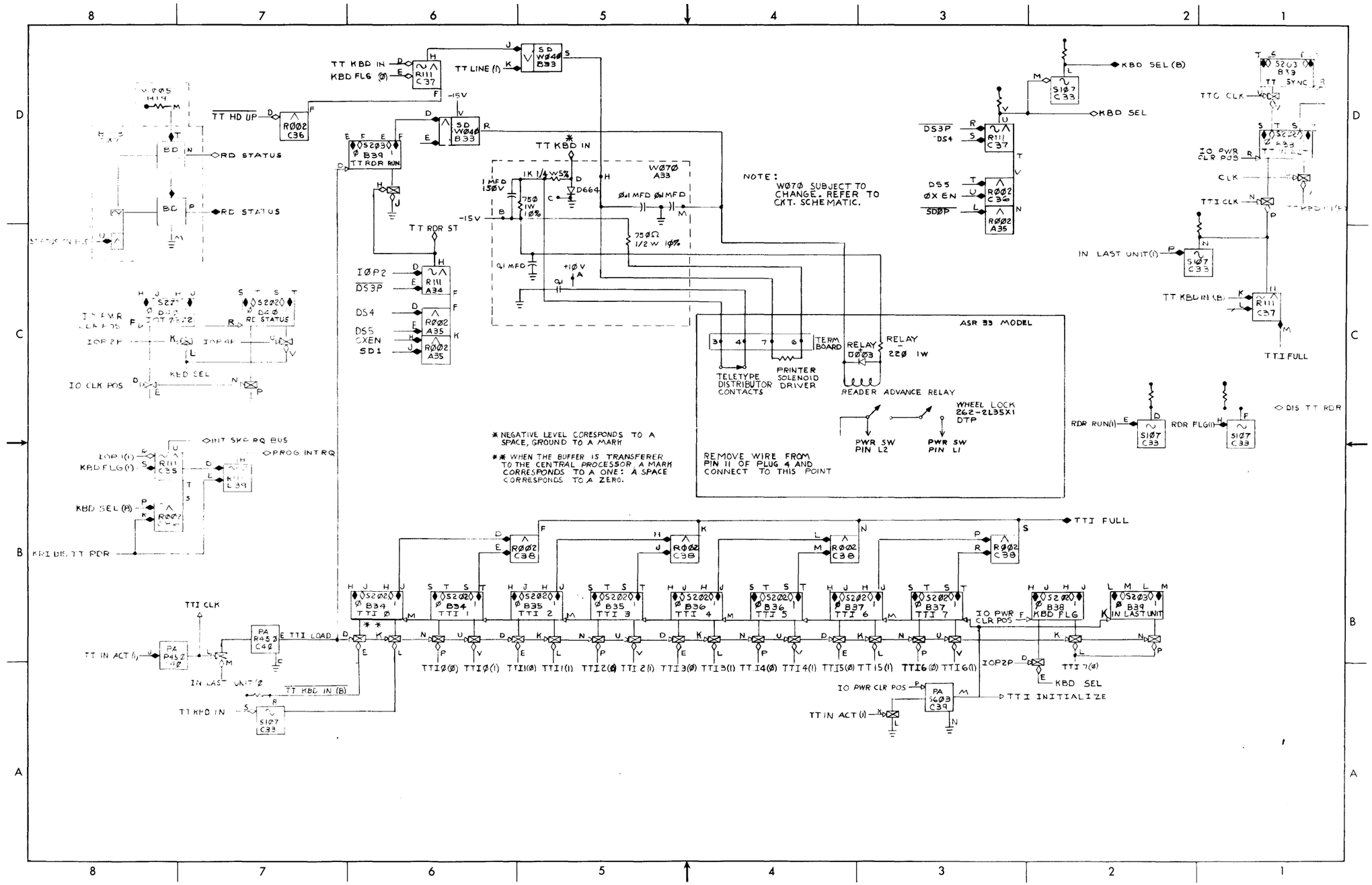
D-BS-KD09-C-9 Reader Control (Sheet 1)



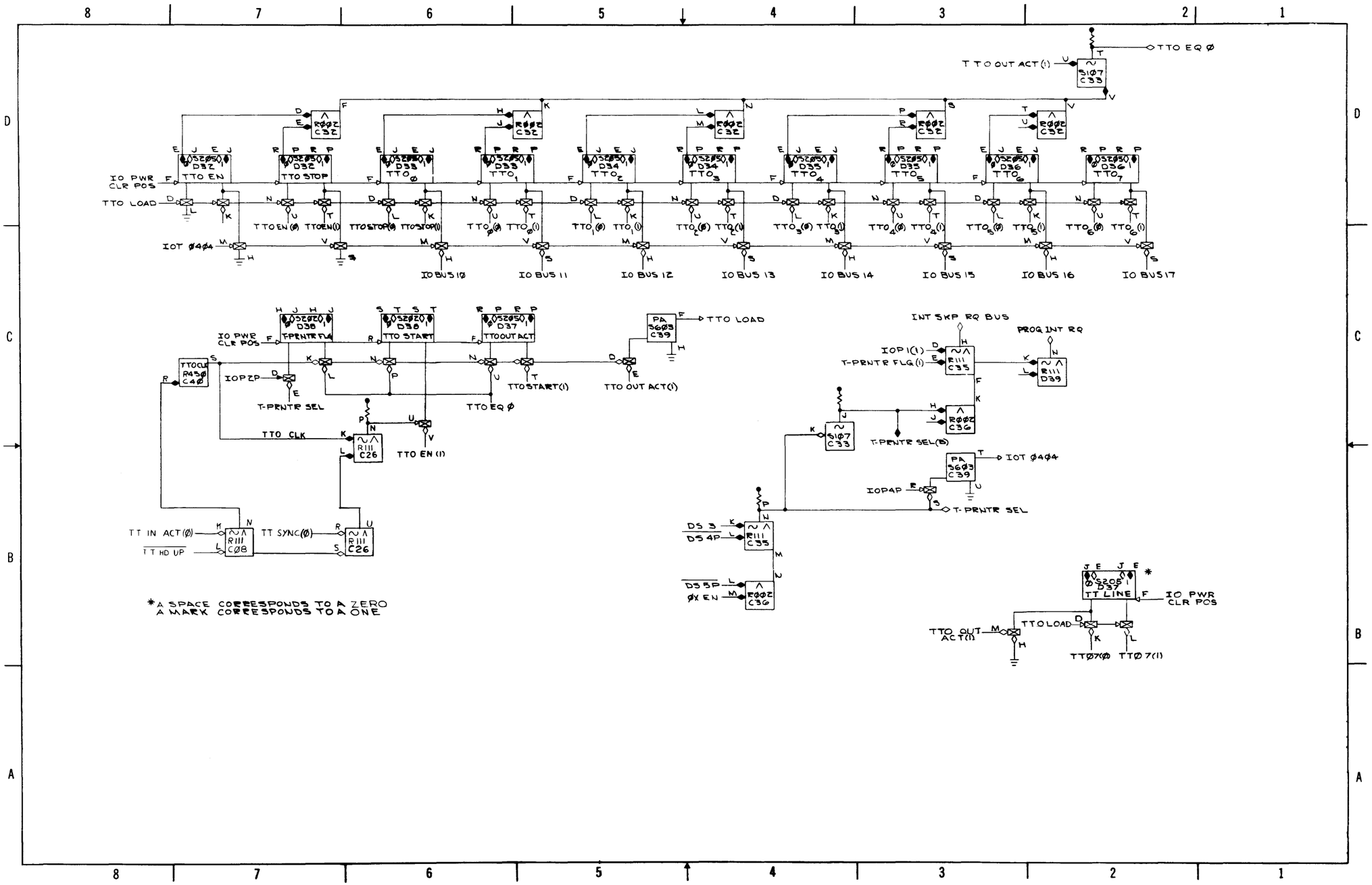
D-BS-KD09-C-9 Reader Control (Sheet 2)



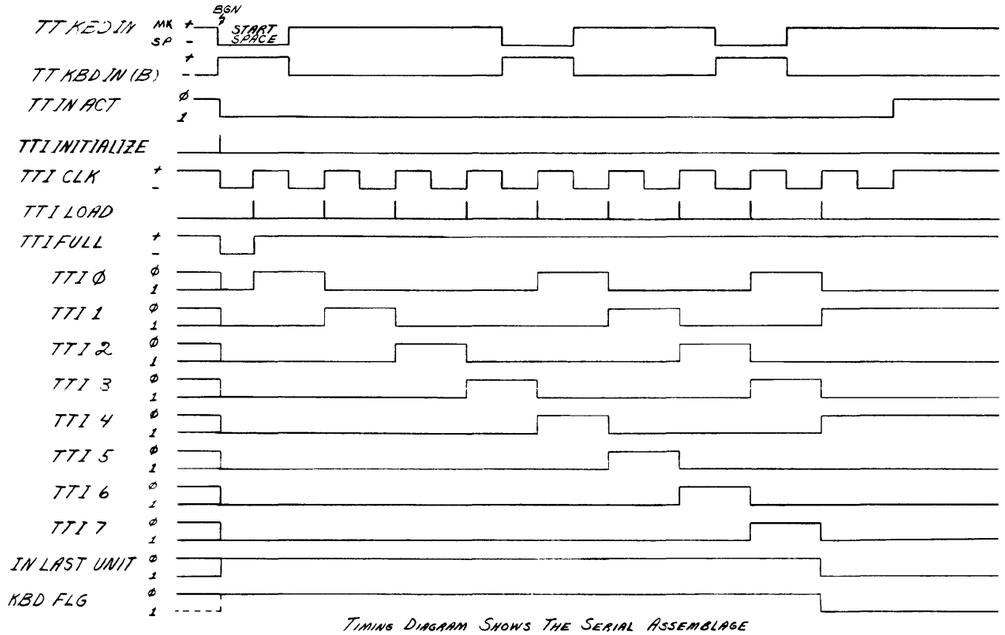
D-TD-KD09-C-10 Punch Control Timing Diagram



D-BS-KD09-C-11 Teletype Control (Sheet 1)

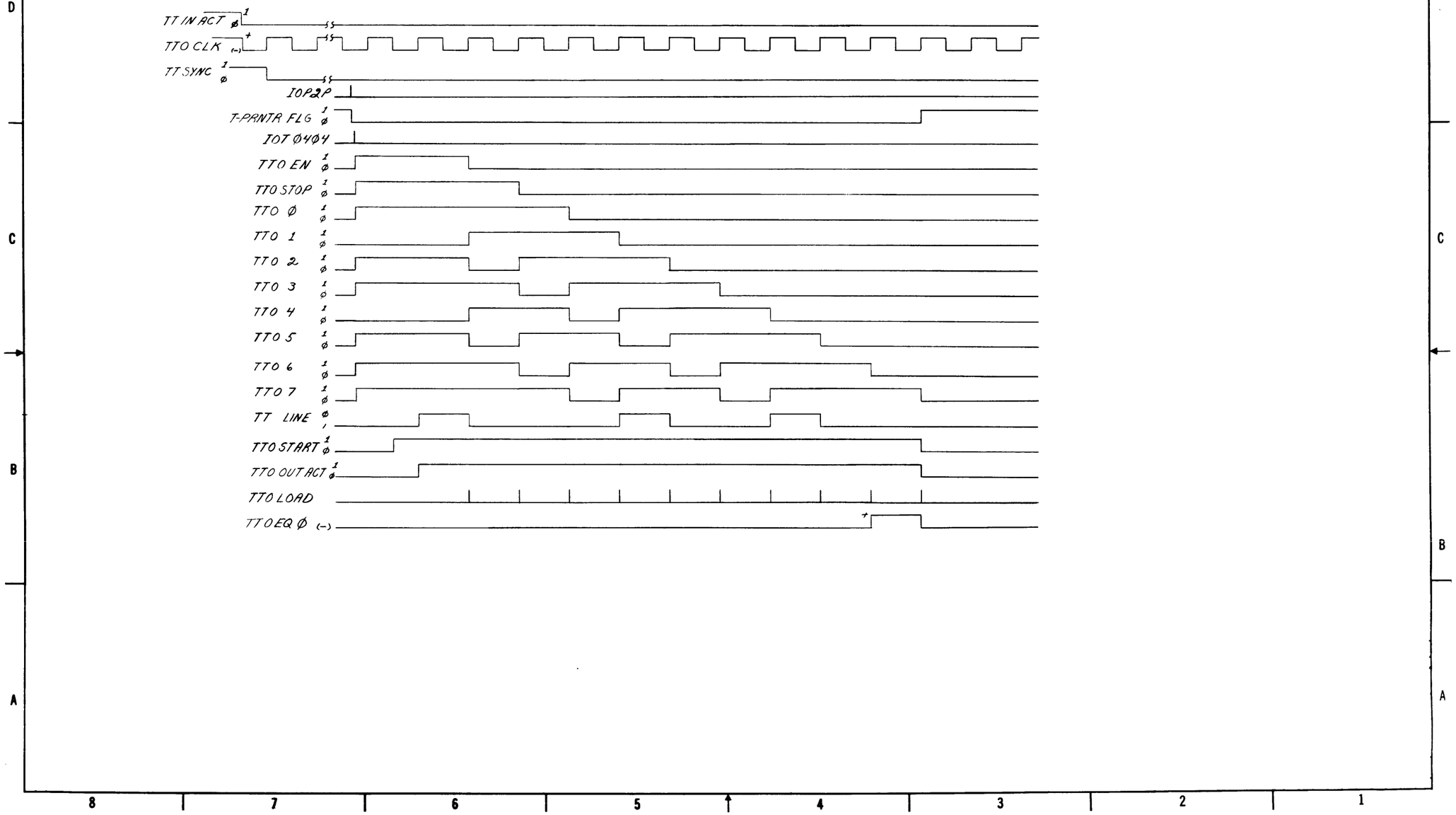


D-BS-KD09-C-11 Teletype Control (Sheet 2)

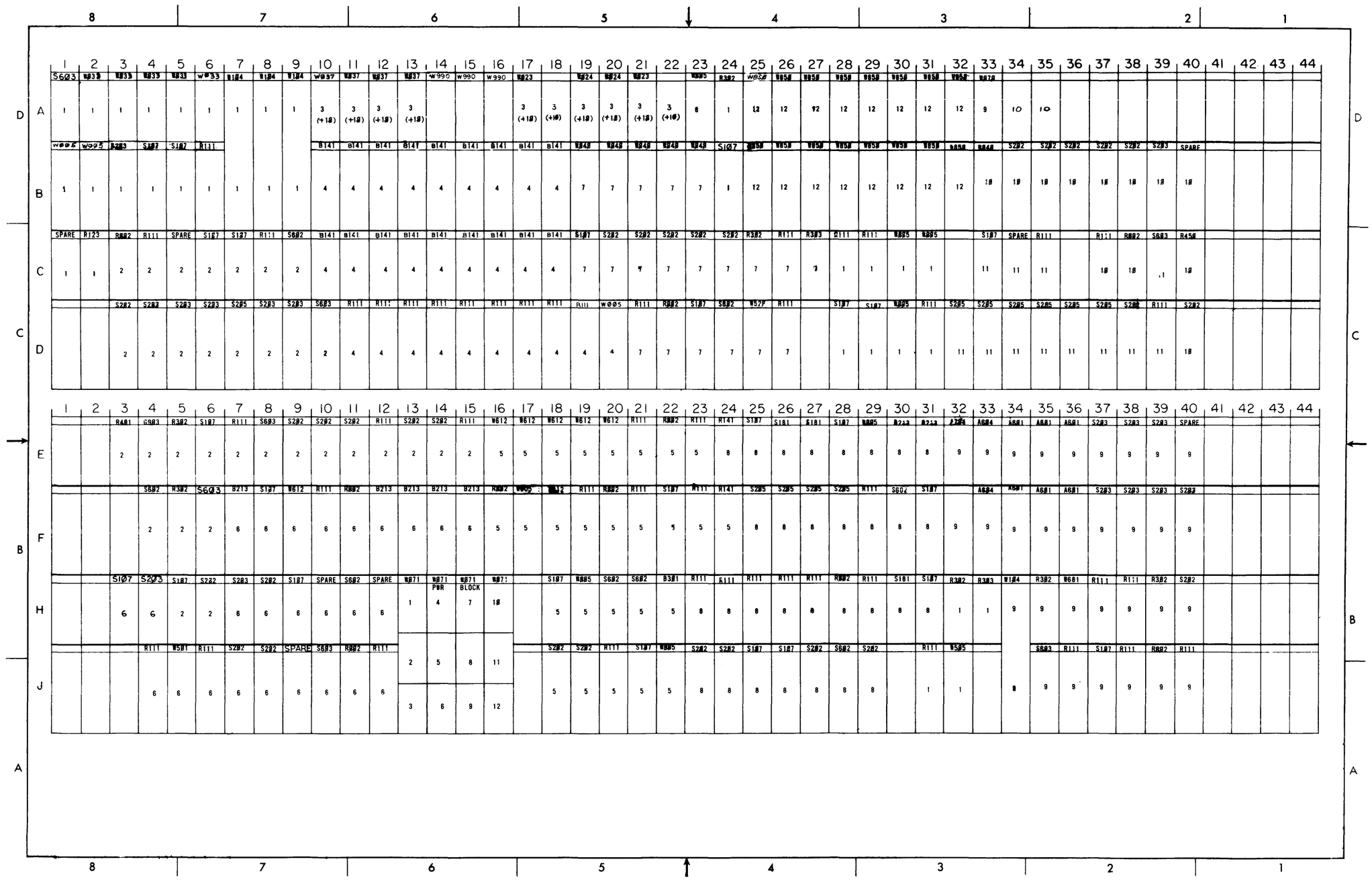


Timing Diagram Shows The Serial Assemblage Of The A.S.C.I.I Code For The Numeral 7 (267_8)

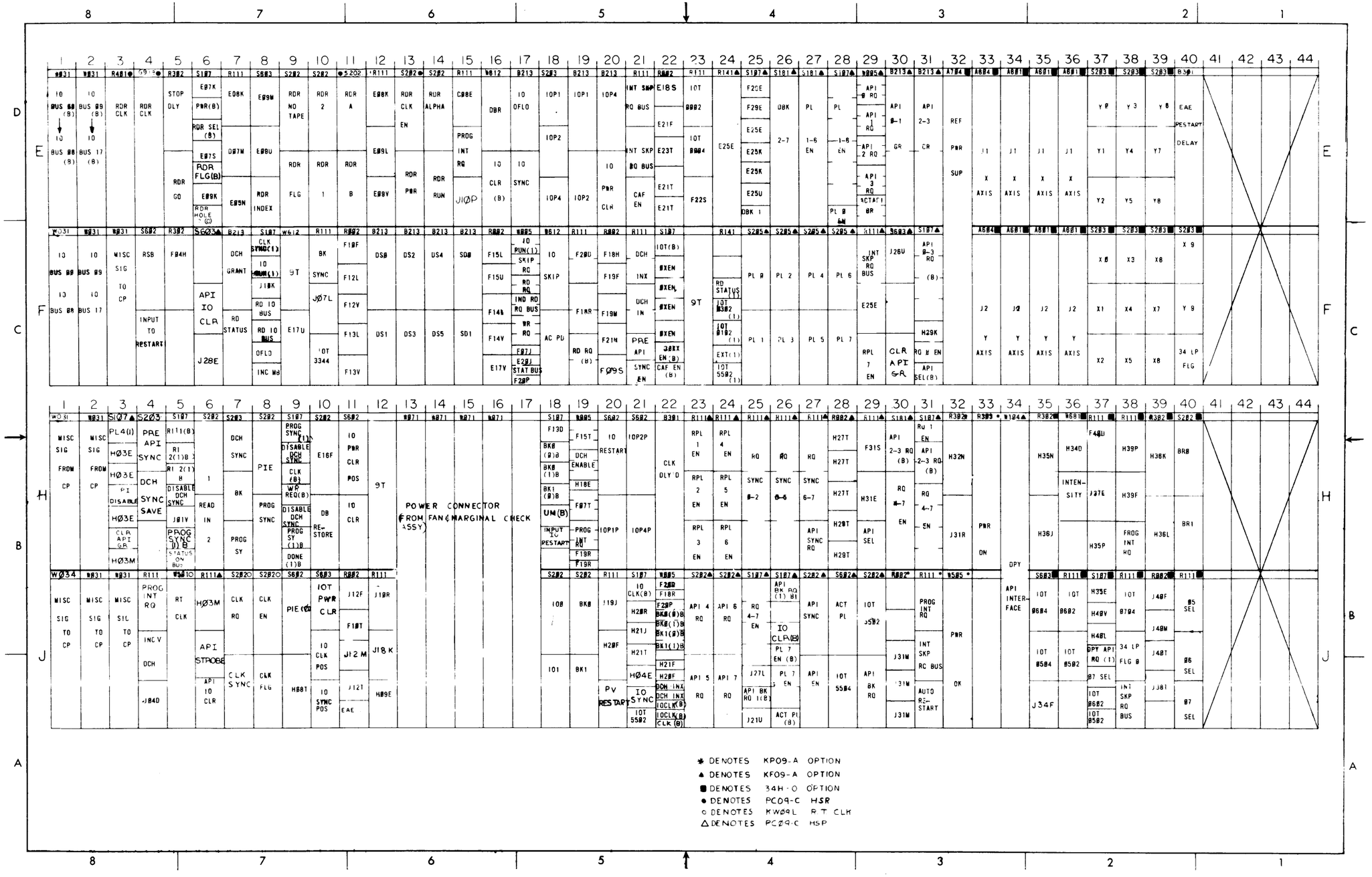
D-TD-KD09-C-12 Teletype Control Time (Keyboard) (Sheet 1)



D-TD-KD09-C-12 Teletype Control Time (Keyboard) (Sheet 2)



D-SP-KD09-C-13 MC Switch Configuration



D-MU-KD09-C-14 PDP-9/L IO Module List

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

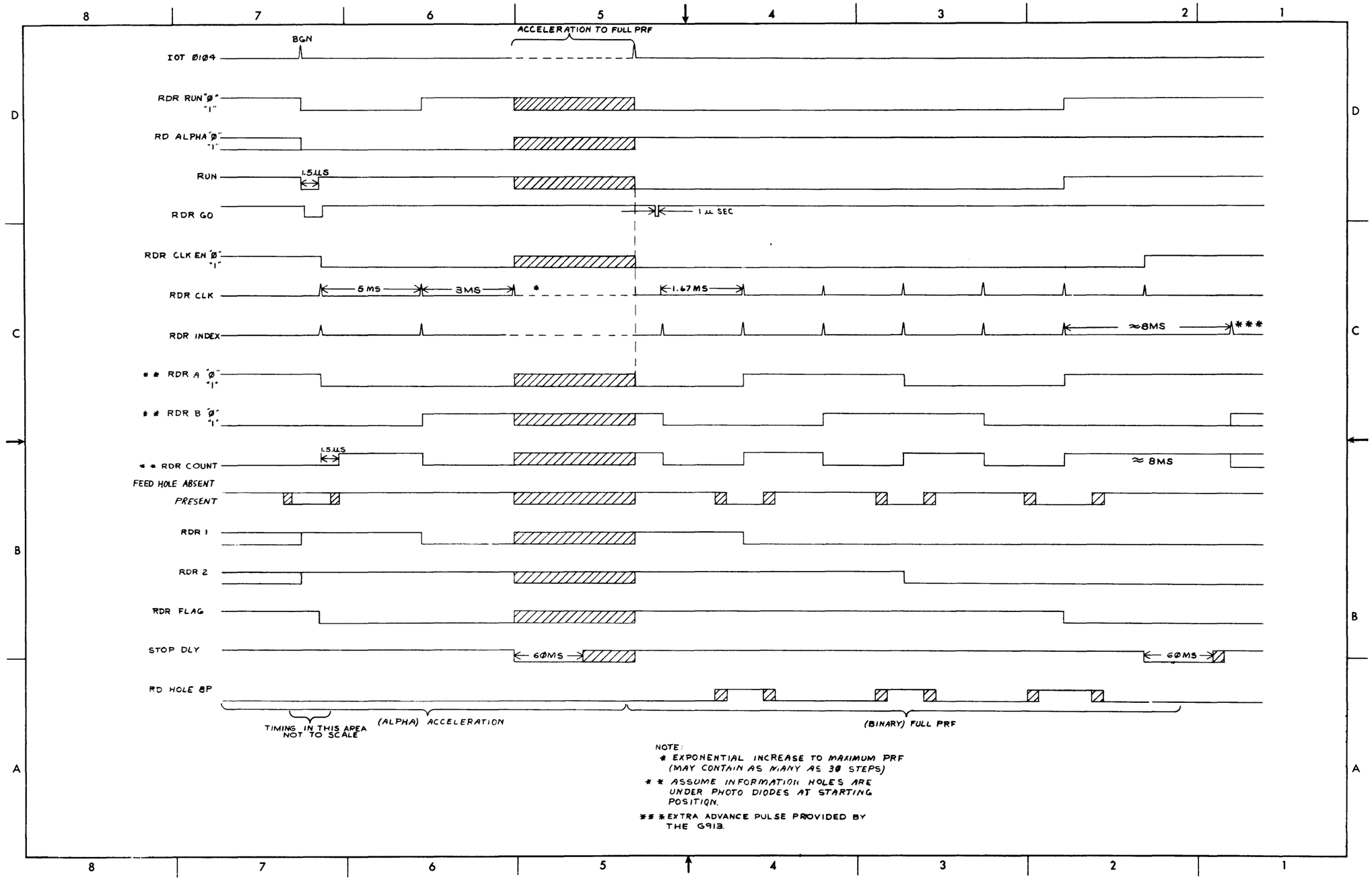
PARTS LIST

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION
	S6Ø3	PULSE AMPLIFIER	5
	S6Ø2	PULSE AMPLIFIER	6
	S2Ø2	DUAL FLIP FLOP	16
	S2Ø3	TRIPLE FLIP FLOP	9
	S205	DUAL FLIP FLOP	7
	S107	INVERTER	13
	RØØ2	DIODE NETWORK	11
	R111	EXPANDABLE NAND/NOR GATE	22
	R123	INPUT BUS	6
	R3Ø2	DELAY (ONE SHOT)	3
	R45Ø	VARIABLE CLOCK	1
	R141	AND/NOR GATE	1
	B141	DIODE GATE	18
	B213	JAM FLIP FLOP	8
	B3Ø1	DELAY	2
	WØØ5	CLAMPED LOAD	11
	WØ4Ø	SOLENOID DRIVER	1
	W612	PULSE AMPLIFIER	3
	W99Ø	BLANK MODULE	2
	W501	Schmitt Trigger	
	W5Ø1	Comparator	
	S181	Pulse Amplifier	
	W505	Pulse Amplifier	

A-PL-KD09-C-14 PDP-9/L IO Module List

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
CAPACITOR	2.2 MFD	-	C25H	C25J	+
RESISTOR	2.7K 5% ¼W		C25J	C25L	
CAPACITOR	0.01 MFD	-	D25E	D25C	+
RESISTOR	4.7K 10% ¼W		D26K	D26B	
RESISTOR	10K ¼W 10%		A21T	B21B	
CAPACITOR	175MFD 10%	-	C27J	C27C	+
RESISTOR	20K ¼W 5%		C27P	C27S	
CAPACITOR	39 MFD 10%	-	C25R	C25S	+
RESISTOR	24K ¼W 5%		C25S	C25U	
CAPACITOR	0.02 MFD 50V	-	A24H	A24J	+
RESISTOR	3K ¼W 5%		FØ5J	FØ5L	
RESISTOR	1.5K ¼W		A17V	B17B	
RESISTOR	1K ¼W 10%		A24J	A24L	
RESISTOR	3K ¼W 5%		D21P	D21B	
CAPACITOR	6.8 MFD	-	E12M	E12C	+
CAPACITOR	270 PF 5%		E4ØJ	E4ØK	
RESISTOR	3.3K ¼W 5%		EØ5S	EØ5U	
RESISTOR	3.3K ¼W 5%		EØ5J	EØ5L	
*PRE API SYNC	JUMPER		J1ØS	J1ØC	
**34 DISPLAY	JUMPER		F4ØT	F4ØC	
***WIRE JUMPER			A32P	A28P	
****CLK SYNC (1) JUMPER			FØ8C	FØ8U	
*REMOVE JUMPER WHEN API IS INSTALLED					
**REMOVE JUMPER WHEN 34 DISPLAY IS INSTALLED					
***REMOVE JUMPER WHEN ME09 IS INSTALLED					
**** REMOVE JUMPER WHEN KW09-L IS INSTALLED					

A-CP-KD09-C-16 External Component List I/O PDP-9/L



D-TD-KD09-C-17 Reader Timing Diagram Alpha and Binary Mode

SIGNAL NAME	ORIGIN	DESTINATION
AC RQ	3-3	4-1
ACT API GR	KF 1-1	KF 1-3
ACT PL	KF 1-1	
ADDR SW(03-17)	6-1	7-1 7-2
ADSO	4-1	7-1
ADSO(G)	7-1	7-2
AN SYNC BUS(0)	4-1	3-2
API D	4-1	7-1
API BK RQ	KF 1-3	KF 1-1 3-2
API BK RQ 1(B)	KF 1-1	4-1 5-1
API ENABLE	KF 1-3	KF 1-2 7-1 12-2
API IO CLR	KF 1-3	KF 1-1
API IO CLR	3-2	
API ON BUS	7-1	7-2
API SEL	KF 1-3	
API STROBE	KF 1-3	
API SYNC	KF 1-1	12-2
API SYNC RQ	KF 1-1	
API 0 EN	KF 1-4	2-2
API 0 EN OUT	2-2	3-3
API 0 GR	KF 1-3,1-4	2-2
API 0 RQ	KF 1-4,1-1	2-2
API 0 RQ(B)	KF 1-1,1-2	
API 0 RQ NEG	KF 1-1	7-1
API(4-7)RQ	KF 1-1	KF 1-2,7-1,7-2,12-2
API 1 EN	KF 14	2-2
API 1 GR	KF 1-3	KF 1-4,2-2
API 1 RQ	KF 1-4	KF 1-2,1-1,2-2
API 1 RQ(B)	KF 1-1	KF 1-2
API 1 RQ NEG	KF 1-1	7-1
API 2 EN	KF 1-4	2-2
API 2 GR	KF 1-3	KF 1-4,2-2,34H,1-2
API 2 RQ	KF 1-4	KF 1-1,1-2,2-2
API 2 RQ(B)	KF 1-1	
API 2 RQ(B)	KF 1-2	
API 2 RQ NEG	KF 1-1	7-1
API 3 EN	KF 1-4	2-2
API 3 GR	KF 1-3	KF 1-4,2-2
API 3 RQ	KF 1-4	KF 1-2,1-1,2-2
API 3 RQ(B)	KF 1-1	
API 3 RQ(B)	KF 1-2	
API 3 RQ NEG	KF 1-1	7-1
API(4-7)RQ(1)B	KF 1-2	KF 1-1
AUTO RESTART	KF 1-1	4-1,7-1
BK	3-2	12-2
BK SYNC	3-2	4-1
BK 0	3-3	3-2
BK 0(0)B	3-3	4-1
BK 0(1)B	3-3	4-1
BK 1	3-3	3-2
BK 1(0)B	3-3	4-1
BR 0	34H 1-1	
BR 1	34H 1-1	
CAF EN	3-1	KF 1-2,1-1,1-3
CAF EN(B)	3-1	KF 1-1
CAL	4-1	KF 1-3
CLK	4-1	3-2,3-1,11-1
CLK DLY D	3-3	
CLK EN	3-2	7-1
CLK FLG	3-2	7-1,3-1,KF 1-4
CLK POS	4-1	3-2
CLK RQ	2-2	
CLK SYNC	3-2	5-1,11-2,3-3
CLK (B)	3-2	3-3
CLR API GR	KF 1-3	
CLR API GR	KF 1-1	
CLR RUN	10-1	
CLR RDR	9-1	
COY API RQ	KF 1-4	3-2
DASO	4-1	7-1,7-2
DATA OFLO	2-2	4-1
DATA SW(00-17)	6-1	7-1,7-2
DB RESTORE	3-1	
DBK(01-07)	KF 1-2	KF 1-1
DBR	3-1	4-1
DCH	4-1	3-3
DCH BK DLY	3-1	6-1
DCH EN	3-1	2-2
DCH GRANT	3-1	2-2
DCH GRANT P	3-1	
DCH INX	3-3	4-1
DCH RQ	2-2	3-2
DCH SYNC	3-2	3-1,12-2
DCH SYNC SAVE	3-2	

SIGNAL NAME	ORIGIN	DESTINATION
DEI	4-1	3-1
DLY	3-3	3-2
DONE	4-1	3-2,3-3
DONE(1)B	3-2	8-1
DPY 0	4-1	7-1
DPI API RQ	34H 1-2	KF 1-4,34H,1-1
DPY ON BUS	7-1	7-2
DS 0	3-1	KF 1-3,2-1
DS 0 P	3-1	KF M
DS 1	3-1	2-1,KF 1-1
DS 1 P	3-1	KF 1-3
DS 2	3-1	2-1,KF 1-3,1-1
DS 3	3-1	2-1,11-2,KF 1-3, 34H 1-2
DS 3 P	3-1	9-1,11-1,10-1, KF 1-1
DS 4	3-1	11-1,10-1,2-1,KF 1-1,34H 1-2
DS 4 P	3-1	11-2,8-1,KF 1-3 34H 1-2
DS 5	3-1	2-1,11-1,9-1,KF 1-3,34H 1-2
DS 5 P	3-1	10-1,11-2,KF 1-1, 34H 1-2
EAE	4-1	3-3
EXT	4-1	7-1,3-3,3-2
EXT(1)B	3-3	KF 1-1,7-1
FEED HOLE	4-2	9-1
FWD FD AND NDX	10-1	
H 10	3-1	
IN LAST UNIT	11-1	12-1
INC WB	3-3	2-2,4-1,3-2
INC + OCH	3-2	4-1,KF 1-1
INPUT IO RESTART	3-3	
INPUT IO RESTART	8-1	
INT RQ RQ BUS	3-3	
*INT SKP RQ BUS	12-1	12-2,9-1,11-2,11-1, 10-1,3-1,KF 1-3, KF 1-1,34H 1-2,3-3
INTENSITY	34H 1-1	
IO ADDR 0	4-1	7-1
IO ADDR ON BUS	7-1	7-2
IO ADDR(03-17)	2-2	5-1
IO ADDR(12,14,16, 17)	KF 1-4	5-1
IO ADDR(03-05,16, 17)B	5-1	7-1,7-2
IO ADDR(06-15)B	5-1	7-1,7-2
IO BUS(00-17)	4-1	7-1,7-2,2-1,KF 1-1, KF 1-3,34H 1-1,10-1 11-2
IO BUS(00-17)B	7-1	7-2,6-1,4-1,10-1 KF 1-3 KF 1-1
IO CLK POS	3-2	3-1 3-3,4-1,KF 1-3, KF 1-1
IO CLK(B)	3-3	KF 1-3,3-2
IO CLR	3-2	12-2,KF 1-3
IO CLR(B)	KF 1-3	3-2
IO OFLO	3-2	2-2,12-2
IO PWR CLR	3-1	2-1
IO PWR CLR NEG	KF 1-4	34H 1-2
IO PWR CLR POS	3-1	3-2,3-3,8-1,9-1, 10-1,11-1,11-2,KF 1-1,KF1-3,KF 1-4, 34H 1-1
IO RESTART	3-3	4-1
IO RUN	3-3	2-2
IO SKIP	3-3	4-1
IO SYNC	3-1	2-1
IO SYNC IN	3-2	7-1
IO SYNC POS	3-2	KF 1-1
IO SYNC SP	3-1	KF 1-4
IO SYNC SP(B)	KF 1-4	34H 1-2
IOP 0	3-3	
IOP 1	3-1	2-1,KF 1-3,KF 1-1 34H 1-2
IOP 1	3-3	
IOP 1 P	3-3	12-2
IOP 2	3-1	2-1,34H 1-2
IOP 2	3-3	
IOP 2 P	3-3	3-1,7-1,9-1,11-1, 11-2,12-1,12-2,KF 1-3,10-1 2-1,34H 1-2
IOP 4	3-1	9-1,10-1,11-1,11-2,
IOP 4	3-3	12-1,12-2,34H 1-2,
IOP 4 P	3-3	KF 1-1,KF 1-3
IOT	4-1	3-1,3-2
IOT PWR CLR	3-1	3-2,3-3,4-1,KF 1-3

*ALL EXCEPT 3-3 ARE SOURCES

SIGNAL NAME	ORIGIN	DESTINATION
IOT(1)B	3-1	3-3,3-2,7-1
IOT 0002	3-1	3-2,12-2
IOT 0004	3-1	3-2,12-2
IOT 0102	9-1	7-1,12-1,3-3
IOT 0104	9-1	9-2
IOT 0204	10-1	
IOT 0302	11-1	7-1,12-1,3-3
IOT 0304	11-2	
IOT 0502	34H 1-2	34H 1-1
IOT 0504	34H 1-2	34H 1-1
IOT 0602	34H 1-2	34H 1-1
IOT 0604	34H 1-2	34H 1-1
IOT 0704	34H 1-2	34H 1-1
IOT 3344	3-1	
IOT 5502	KF 1-3	7-1,12-2,3-3
IOT 5504	KF 1-3	KF 1-4,KF 1-1
IRI	4-1	KF 1-4
T TO CA INH	2-2	3-3
KBD FLG	11-1	12-1,7-1,9-1
KBD SEL	11-1	12-1
KBD SEL(B)	11-1	
KDPM	4-1	6-1
KEY	4-1	8-1
KEY PLY	4-1	9-1
KIO	3-1	4-1
KMT	6-1	4-1
KRI	4-1	8-1
KXDM	6-1	4-1
LINK	6-1	4-1
LOCK	6-1	KF 1-1,3-2,4-1
LP OUT	34H 1-1	
LP STB	34H 1-1	12-2
MB(00-17)	4-1	6-1,3-1,3-3
MM	6-1	4-1
OFLO	4-1	3-2
PB(10-17)	10-1	12-1
PF API RQ(1)	KF 1-4	
PI DISABLE	KF 1-3	12-2,3-2
PIE	3-2	12-2,7-1
PL(00-07)	KF 1-1	KF 1-2,7-2,6-1
PL(00-02)EN	KF 1-1	KF 1-2,1-3
PLE EN P	KF 1-1	
PLS CONTROL 0	KF 1-4	
PLS CONTROL 1	KF 1-4	
PRE API SYNC	KF 1-1	
PRE API AYNC EN	KF 1-1	
*PROG INT RQ	2-1	9-2,10-1,11-1,34H 1-1,KF 1-1,3-2,11-2
PROG SY	3-2	
PROG SY(1)B	3-2	4-1
PROG SYNC	3-2	12-2
PROG SYNC(1)B	3-2	4-1
PTR API RQ	KF 1-4	4-1
PTR GR	KF 1-4	
PUN	10-1	12-1
PUN ACT	10-1	
PUN FEED	10-1	
PUN FLG	10-1	12-1,7-1,9-1
PUN HOLE(1-8)	10-1	
PUN LINE	10-1	12-1
PUN NO TAPE	10-1	7-1,12-1,9-1
PUN PWR	10-1	
PUN PWR ON	10-1	12-1
PUN SEL	10-1	12-1
PUN SPD	10-1	12-1
PUN SYNC	10-1	
PV	4-1	3-2
PWR CLR POS	4-1	3-1
PWR ON	KF 1-1	KF 1-4
PWR OR	KF 1-1	
PWR(B)	9-1	9-2
RB(00-17)	9-2	12-1,7-1,7-2
RD HOLE(1-8)	9-2	
RD HOLE(1-8)B	9-2	8-1
RD HOLE 7(B)	9-2	4-1
RD HOLE 7 (C)	9-2	12-1,9-1
RD HOLE 8	9-2	
P + ALPHA		
RD IO BUS	7-1	7-2
RD RQ	2-1	3-3
RD RQ(B)	3-3	4-1
RD STATUS	11-1	2-1,12-1,3-3,7-1
RDR A	9-1	12-1
RDR ALPHA	9-1	12-1,9-2
RDR A(0)B	9-1	
RDR A(1)B	9-1	
RDR B	9-1	12-1
RDR B(0)B	9-1	
RDR B(1)B	9-1	
RDR CLK	9-1	
RDR CLK ENABLE	9-1	12-1

*ALL EXCEPT 3-2 ARE SOURCES

SIGNAL NAME	ORIGIN	DESTINATION
RDR COUNT	9-1	
RDR FEED	9-1	9-2
RDR FLG	9-1	12-1,7-1,9-2, KF 1-4
RDR FLG(B)	8-1	4-1
RDR GO	9-1	12-1
RDR INDEX	9-1	12-1
RDR NO TAPE	9-1	12-1,7-1
RDR ON BUS	7-1	7-2
RDR PWR	9-1	
RDR RUN	9-1	9-2,12-1
RDR SEL	9-1	
RDR SEL(B)	9-1	
RDR 1	9-1	9-2,12-1
RDR 2	9-1	9-2,12-1
RDR D	4-1	7-1
READ IN 1	8-1	
READ IN 2	8-1	
RI 1(1)B	8-1	4-1
RI 2(1)B	8-1	4-1
RPL(1-7)EN	KF 1-1	
RQ SYNC(0-7)	KF 1-1	KF 1-1,1-3,5-1
RQ 00 EN	KF 1-2	KF 1-1
RQ 01 EN	KF 1-2	KF 1-1
RSB	8-1	9-1
RT CLK	6-1	3-2
RUN	9-1	12-1
SD 0	3-1	9-1,3-2,2-1
SD 0 P	3-1	9-1,3-2,10-1,34H 1-1
SD 1	3-1	2-1
SD 1 P	3-1	
SEL(0-2)	KF 1-4	
SEN(1)B	4-1	3-3,7-1
SKIP RQ	2-1	3-3
STATUS ON BUS	7-1	7-2
STATUS D	4-1	7-1
STOP DLY	9-1	12-1
SW CLK	4-1	3-2
TAPE	10-1	
T-PRINTER FLG	11-2	7-1,12-1
T-PRINTER SEL	11-2	12-1
T-PRINTER SEL(B)	11-2	
TT IN ACT	11-1	12-1
TT KBD IN	11-1	12-1
TT KBD IN(B)	11-1	
TT LINE	11-2	11-1,12-1
TT OUT ACT	11-2	12-1
TT RDR RUN	11-1	
TT SYNC	11-1	11-2
TTI CLK	11-1	
TTI FULL	11-1	12-1
TTI INITIALIZE	11-1	
TTI LOAD	11-1	12-1
TTI ON BUS	7-1	7-2
TTI(0-7)	11-1	7-1,12-1
TTI D	4-1	7-1
TTO CLK	11-2	11-1
TTO EN	11-2	12-1
TTO EO 8	11-2	12-1
TTO LOAD	11-2	
TTO START	11-2	12-1
TTO STOP	11-2	12-1,9-1
TTO(0-7)	11-2	3-3
UM	4-1	4-1
UM(0)B	3-3	3-2,3-3,4-1
WR RQ	2-2	
WR RQ(B)	3-2	7-1
X(0-9)	34H 1-1	7-2
Y(0-9)	34H 1-1	9-1,10-1,11-1,11-2
OXEN	3-1	12-1,34H 1-1,12-2
00 EN(B)	3-1	34H 1-1,7-1,
(05-07)SEL	34H 1-2	12-2
(05-07)SEL(B)	34H 1-2	
34 LP FLG	34H 1-2	

SIGNAL NAME	ORIGIN	DESTINATION
KR DIS TT RDR		
KR KBD FLG		
RDR INDEX ENABLE		
TT HDUP		
TT RD ST		
NO PCO TO GND 1		
NO PCO TO GND 2		
NO PCO TO GND 3		
NO PCO TO GND 4		