INSTRUCTION MANUAL

# DM09A
## ADAPTER/MULTIPLEXER

# PDP-9

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

DEC-09-I9AA-D

# DM09A

# ADAPTER/MULTIPLEXER

# INSTRUCTION MANUAL

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TABLES

# 1. INTRODUCTION

The DM09A Adapter/Multiplexer an option to the PDP-9 manufactured by Digital Equipment Corporation (DEC), provides an interface through which three I/O devices may gain access to the PDP-9 memory via the DMA channel. A basic system block diagram is given in Figure 1-1.

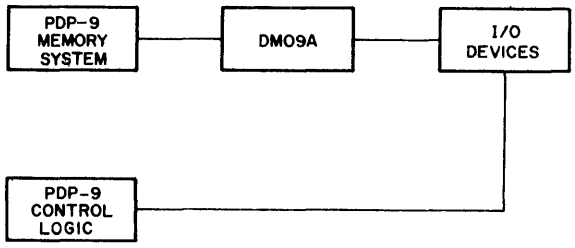



Figure 1-1 Basic DM09A System Block Diagram

This document and the documents referenced herein provide the information necessary for installation, operation and maintenance of the option. The level of discussion assumes that the user is familiar with the basic PDP-9.

## 1.1 Related Documentation

The DEC documents listed in Table 1-1 contain material which supplements information in this document.

Table 1-1
Reference Documents

| Title | Document Number | Description |
|---|---|---|
| PDP-9 User Handbook | F-95 | Operation and programming information for the PDP-9. |
| PDP-9 Maintenance Manual Volumes I and II | F-97 | Operation and maintenance information for the PDP-9 including basic PDP-9 engineering drawings. Basic DM09A theory of operation. |
| DIGITAL Logic Handbook | C-105 | Specifications and descriptions of most FLIP CHIP modules used in the DM09A. |

## 1.2 Engineering Drawing References

Engineering drawings will be referenced using an abbreviated code. As an example, drawing D-BS-DM09-A-2, DMA Adapter Multiplexer Control, sheet 1 of 2, will be referenced as [DM-2(2)].

# 2. SPECIFICATIONS

## 2.1 Environmental

The DM09A consists entirely of modules of the type used in the PDP-9 central processor. Therefore, PDP-9 environmental specifications apply to the DM09A.

## 2.2 Power Requirements

The option obtains all necessary operating power from the PDP-9 power supply system. No additional power supplies, power control or fan assemblies are necessary.

## 2.3 Physical

The DM09A consists entirely of modules which are housed by two DEC standard 1943 mounting panels, thus requiring 10-1/2 in. of mounting space. Placement of these panels is given in Section 3, INSTALLATION.

## 2.4 Controls and Indicators

No controls or indicators are associated with the DM09A. The option is entirely under the control of the PDP-9 and the I/O devices.

## 2.5 Performance

The multiplexer operates at two speeds. I/O devices with 10 mHz logic may request the high speed and thus achieve a 1 μs/transfer rate; I/O devices with low speed logic should request the low speed of 3 μs/transfer to permit sufficient data-line settling time. It should be remembered that the speed range applies only to the DM09A. The PDP-9 DMA channel and the memory require only 1 μs/transfer.

## 3. INSTALLATION

Implementation of the option involves installing the option modules into their preassigned, prewired locations in the basic PDP-9 cabinet. The location in which the option mounts is shown in Figure 3-1.

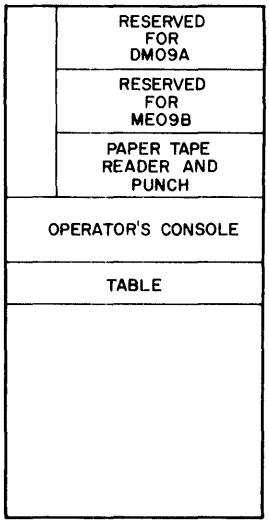



Figure 3-1 Installation Diagram

The following engineering drawings provide all necessary interface information.

| Drawing Number | Title | Description |
|---|---|---|
| D-CD-DM09-A-9 (Rev. A) | Memory Interface | Interface between the DM09A and the basic PDP-9 memory. |
| CD-D-DM09-A-10 | Interface Cabling DM09 Memory | Interface between the DM09A, ME09A memory extension control and MM09A extended memory bank. |
| CD-D-DM09-A-11 | Cabling DMA Inter-Memory | Interface between the MC70B basic PDP-9 memory and MM09A, B and C extended memory banks. |

## 4. PRINCIPLES OF OPERATION

### 4.1 Basic

A basic description of DM09A logic operation can be obtained from Section 3.8.3, DMA Channel Transfers, of the PDP-9 Maintenance Manual, Volume 1. A detailed DM09A block diagram is also contain in that section.

This document describes in detail the operation of the DM09A DMA Adapter/Multiplexer.

## 4.2 Detailed

A variety of transfer type combinations are possible with the DM09A. To avoid excessive repetition, only three types will be described herein; Single-Fast-Input cycle, Single-Slow-Output cycle and Double (Back to Back)-Fast-Output cycles.

Certain DM09A operations are executed regardless of transfer type; namely, control circuitry initialization via power turn-on and internal DM09A control pulse train generation. Transfer type descriptions assume I/O device 0 is being acted upon. All reference will be made to I/O device 0. Similar operations will result when any other device is acted upon.

All transfer types can be thought of as consisting of a number of "time states" each commencing with a PDP-9 CLK pulse. Single transfers consist of time states in which either an I/O device is made ready, in which a device is synchronized to the PDP-9, or in which a data transfer takes place. With multiple transfers, synchronization is established during the previous data transfer.

When reading the logic descriptions, the user should refer to the engineering drawings referenced on the signal flow tables. In addition, DM09A timing diagrams, drawings DM-8(1) and DM-8(2) should be referenced for specific timing information.

### 4.2.1 Power Turn-On

When the system is first turned on, PK CLR (power and key clear) pulses arrive at the DM09A control logic and produce PWR CLR POS (power clear positive) pulses to condition the control logic. The operations performed are as follows:

Clear SYNC 0

Clear SET A0

Clear SET D0

Clear DEV 0 CONT

Clear SLOW CYCLE A

### 4.2.2 Internal Control Pulse Train

Following PK CLR, CLK (clock) pulses arrive at the DM09A control logic and are used to generate an internal DM09A control pulse train via the circuitry of Figure 4-1.

Time relationships are illustrated in Figure 4-2. The pulse train is generated whenever the system is operating.

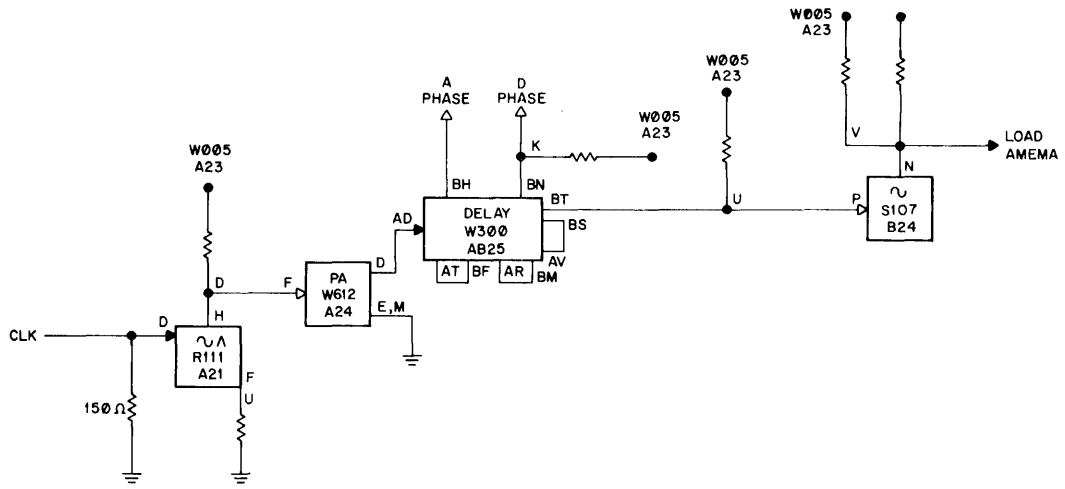



Figure 4-1 Control Pulse Train Circuitry

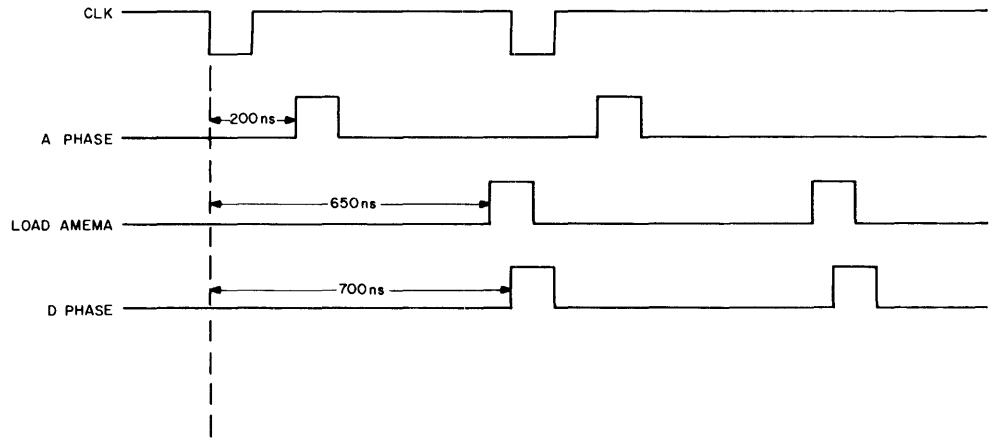



Figure 4-2 Control Pulse Train Time Relationship

### 4.2.3 Single-Fast-Input Cycle

The DM09A adapter/multiplexer is utilized during the memory read/write cycle. During this time the I/O device break request flag is set providing the DM09A with a CH 0 BK RQ level. Referring to Table 4-1 and the referenced engineering drawings, internal control logic operations serve to generate an AM RQ level. This level is applied to the PDP-9 memory control circuitry shown on drawing D-BS-MC70-B-1 (sheet 2). A CLK pulse marking the beginning of the SYNCING time state is then produced. During SYNCING, the central processor has access to core memory. CLK, delayed 100 ns, generates SYNC CLK to set the AM SYNC flip-flop in memory control via AM RQ(1). AM

SYNC(1) produces AM SYNC(1)B and AM SYNC BUS(1). AM SYNC(1)B is utilized by CM (control memory) timing to prevent SM(1) from restarting the CM on the next CLK pulse which marks the beginning of the DATA XFER time state.

The DATA XFER time state is entered via another PDP-9 CLK pulse. CLK, delayed 50 ns, is POST CLK and resets the MODE flip-flop conditioned by AM SYNC(1). MODE(0) signifies AM access to memory while MODE(1) signifies CP access to memory. PRE-WRITE OFF of the previous core memory cycle (SYNCING) sets the MEM DONE flip-flop and produces AM GRANT. If an EAE or an IOT instruction immediately precedes the DM09A request, AM GRANT is not produced. In this case AM SYNC(1)B is delayed to generate AM GRANT SMLTD (simulated).

During the current time state, I/O device 0 address bits are present at the input gating circuitry of the AM REGISTER (refer to drawing DM-3(2)). Address bits utilized by a PDP-9 with basic memory are designated CH 0 ADDR BIT 05 through CH 0 ADDR BIT 17. The bits are applied to the inverter modules shown. ADDR 0, the result of DEV 0 CONT(0) and SET D0(1), allows the address bits access to the jam input gates of the AM REGISTER as LAM 05 through LAM 17.

An AMI (adapter multiplexer input) pulse jam transfers the 13-bit address into the register. AMI is the result of AM GRANT* or AM GRAND SMLTD. The flip-flops designated AMEMA 03 and AMEMA 04 are used with PDP-9 systems containing extended memory banks. Inverter inputs are CH 0 ADDR BIT 03 and SET A0(1) for AMEMA 03 and CH 0 ADDR BIT 04 and SET A0(1) for AMEMA 04. LOAD AMEMA jam transfers the extended memory addressing bits into their respective flip-flops. This pulse is produced 650 ns after CLK by the control pulse train circuitry described in Section 4.2.2.

Following memory addressing, an 18-bit data word is jam transferred into the AM REGISTER. I/O device 0 data word consists of CH 0 DATA BIT 00 through CH 0 DATA BIT 17. The data word is also applied to a network of inverter modules. The enabling signal is DEV 0. The data word is jam transferred into the AM REGISTER by a second AMI pulse which is produced by AM STROBE.

### 4.2.4 Single-Slow-Output Cycle

Table 4-2 illustrates the signal flow associated with a Single-Slow-Output cycle. The I/O device is programmed to indicate that an output transfer is to take place, the number of words to be transferred and the address of the first word, DM09A control logic operations which result from this type of data transfer are basically similar to those of the Single-Fast-Input cycle. The I/O device requests multiplexer service via CH 0 BK RQ. The control logic proceeds to generate AM RQ and AM RQ NEG. SYNC 0(1) and $\overline{\text{CH 0 FAST RQ}}$ condition the set DCD gate of the SLOW CYCLE A

*Both may be present but the circuit is a logical OR.

flip-flop which is set by the positive going transition of AM RQ NEG. Following logic operations in the multiplexer and in the PDP-9, an AM GRANT pulse is issued to produce AMI. With input transfers, this pulse jam transfers the device supplied address into the AM register. This is not necessary with the current type of transfer.

Following further DM09A control logic operations, similar to those of Single-Fast-Input cycle, PDP-9 AM STROBE arrives at the DM09A. This pulse is gated with $\overline{\text{CH 0 RQ IN}}$ and SET D0(1) to produce SAI (sense amplifier input) thus allowing PDP-9 sense amplifier bits SA 00 through SA 17 access to the jam input gates of the AM register. A second AMI pulse is produced at this time to jam transfer these bits into the AM register.

### 4.2.5 Double (Back to Back)-Fast-Output Cycles

Signal flow for the current transfer type is given in Table 4-3. Initial signals sent to the DM09A control logic are CH 0 BK RQ, CH 0 FAST RQ and $\overline{\text{CH 0 RQ IN}}$. CH 0 BK RQ signals the DM09A that service is requested. This signal and internal SLOW CYCLE A(0) produce SYNC 0 EN to condition the set DCD gate of the SYNC 0 flip-flop. The D PHASE pulse preceding the SYNCING 1 time state sets SYNC 0 to establish device priority. This conditions the CH 0 FAST CLR and sets the DCD gate to produce AM RQ and AM RQ NEG. AM RQ signals the PDP-9 that a DMA cycle is desired; the computer responds with AM SYNC(1) B.

The A PHASE pulse of SYNCING 1 sets SET A0 and generates CLR SYNC. This clears SYNC 0. SET A0(1) and AM SYNC(1)B generate SET D0 EN which conditions the set DCD gate of the SET D0 flip-flop.

The following D PHASE pulse sets SET D0. SET A0(1) and SET D0(1) produce CLR SLW CYC EN which with A PHASE, maintains SLOW CYCLE A(0), a characteristic of fast transfers. SYNC 0 is set again because SLOW CYCLE A(0) and CH 0 BK RQ are still present. Setting SYNC 0 generates another AM RQ signal. Because this signal is applied to the PDP-9 AM SYNC flip-flop prior to SYNC CLK, the flip-flop remains set.

The PDP-9 produced AM GRANT arrives at the multiplexer control circuitry as the DATA XFER 1 and SYNCING 2 time states are entered. The pulse jam-transfers address information into the AM REGISTER. During these time states the data transfer associated with the preceding syncing operations, and syncing operations for the next data transfer take place.

AM STROBE arrives from the PDP-9 and generates SAI and AMI, thus allowing the sense amplifier bits, SA 00 through SA 17, access through the AM register gating circuitry and into the AM register.

DATA XFER 2 is entered. SET A0 is cleared and operations similar to DATA XFER 1 take place to jam transfer the data bits of the second word into the AM register. The D PHASE pulse at the end of the current time state clears SET D0.

Table 4-1
Single-Fast-Input Cycle Signal Flow

| Time State | Control Pulse | Signal | Conditions | Drawing Number |
|---|---|---|---|---|
| | | SYNC 0 EN | CH 0 BK RQ * SLOW CYCLE A(0) | DM-2(2) |
| | D PHASE | SYNC 0(1) | D PHASE * SYNC 0 EN | DM-2(1) |
| | | AM RQ | SYNC 0(1) | DM-2(2) |
| | | AM SYNC(1)B | From PDP-9 | MC-1(2) |
| SYNCING | A PHASE | SET A0(1) | A PHASE * SYNC 0(1) | DM-2(1) |
| | | CLR SYNC | A PHASE * AM SYNC(1)B(B) | DM-2(2) |
| | | SET D0 EN | AM SYNC(1)B * SET A0 (1) | DM-2(2) |
| | | CH 0 FAST CLR | CLR SYNC * SYNC 0 (1) | DM-2(1) |
| | | SYNC 0(0) | SYNC 0(1) * CLR SYNC | DM-2(1) |
| | D PHASE | SET D0(1) | D PHASE * SET D0 EN | DM-2(1) |
| | | CLR SLW CYC EN | SET A0(0) * SET D0(1) | DM-2(1) |
| | | AM GRANT | From PDP-9 | MC-1(2) |
| DATA XFER | A PHASE | CH 0 ADDR ACC IN | A PHASE * SET A0(1) * SET D0(1) | DM-2(1) |
| | | DEV 0 CONT(1) | CH 0 ADDR ACC IN * SET D0(1) | DM-2(1) |
| | | DEVICE 0 | DEV 0 CONT(1) * SET D0(1) * CH 0 RQ IN | DM-2(2) |
| | | SET A0 (0) | A PHASE * SYNC 0(0) * SET D0(1) | DM-2(1) |
| | | CH 0 ADDR ACC | CH 0 ADDR ACC IN | DM-2(1) |
| | | SLOW CYCLE A(0) | A PHASE * CLR SLW CYC EN | DM-2(1) |
| | | AM STROBE | From PDP-9 | MC-2 |
| | D PHASE | CH 0 DATA RDY IN | D PHASE * SET D0(1) * SLOW CYCLE D(0) | DM-2(2) |
| | | INH 0 DAP(0) | CH 0 DATA RDY IN | DM-2(2) |
| | | CH 0 DATA RDY | CH 0 DATA RDY IN | DM-2(2) |
| | | CH 0 DATA ACC | D PHASE * CH 0 RQ IN * INH 0 DAP(0) * SET D0(1) | DM-2(1) |
| | | SET D0(0) | D PHASE * SET A0(0) * SLOW CYCLE D(0) | DM-2(1) |

Table 4-2
Single-Slow-Output Cycle Signal Flow

| Time State | Control Pulse | Signal | Conditions | Drawing Number |
|---|---|---|---|---|
| | SYNC | SYNC 0 EN | CH 0 BK RQ * SLOW CYCLE A(0) | DM-2(2) |
| | D PHASE | SYNC 0(1) | D PHASE * SYNC 0 EN | DM-2(1) |
| | | AM RQ | SYNC 0(1) | DM-2(2) |
| | | SLOW CYCLE A(1) | SYNC 0(1) * $\overline{\text{CH 0 FAST RQ}}$ * AM RQ NEG → 0 | DM-2(1) |
| | | AM SYNC(1)B | From PDP-9 | MC-1(2) |
| SYNCING | A PHASE | SET A0(1) | A PHASE * SYNC 0(1) | DM-2(1) |
| | | CLR SYNC | A PHASE * AM SYNC(1)B(B) | DM-2(2) |
| | | SET D0 EN | AM SYNC(1)B * SET A0(1) | DM-2(2) |
| | | CH 0 FAST CLR | CLR SYNC * SYNC 0 (1) | DM-2(1) |
| | | SYNC 0(0) | CLR SYNC * SYNC 0(1) | DM-2(1) |
| | D PHASE | SET D0 (1) | D PHASE * SET D0 EN | DM-2(1) |
| | | AM GRANT | From PDP-9 | MC-1(2) |
| DATA XFER | A PHASE | CH 0 ADDR ACC IN | A PHASE * SET A0(1) * SET D0(1) | DM-2(1) |
| | | DEV 0 CONT(1) | CH 0 ADDR ACC IN * SET D0(1) | DM-2(1) |
| | | SET A0(0) | A PHASE * SYNC 0(0) * SET D0(1) | DM-2(1) |
| | | CH 0 ADDR ACC | CH 0 ADDR ACC IN | DM-2(1) |
| | | CLR SLW CYC EN | SET A0(0) * SET D(1) | DM-2(1) |
| | | SLOW CYCLE A(0) | A PHASE * CLR SLW CYC EN | DM-2(1) |
| | | AM STROBE | From PDP-9 | MC-2 |
| | | AMI | AM STROBE + $\overline{\text{AM GRANT}}$ | DM-2(2) |
| | | SAI | AM STROBE * $\overline{\text{CH 0 RQ IN}}$ * SET D0(1) | DM-2(2) |
| | D PHASE | SET D0(0) | D PHASE * SET A0(0) * SLOW CYCLE D(0) | DM-2(1) |

Table 4-3
Double (Back to Back)-Fast-Output Cycles Signal Flow

| Time State | Control Pulse | Signal | Conditions | Drawing Number |
|---|---|---|---|---|
| | | SYNC 0 EN | CH 0 BK RQ * SLOW CYCLE A(0) | DM-2(2) |
| | D PHASE | SYNC 0(1) | D PHASE * SYNC 0 EN | DM-2(1) |
| | | AM RQ | SYNC 0(1) | DM-2(2) |
| | | AM SYNC(1)B | From PDP-9 | MC-1(2) |
| SYNCING 1 | A PHASE | CLR SYNC | A PHASE * AM SYNC(1)B(B) | DM-2(2) |
| | | CH 0 FAST CLR | CLR SYNC * SYNC 0(1) | DM-2(1) |
| | | SET A0(1) | A PHASE * SYNC 0(1) | DM-2(1) |
| | | SET D0 EN | SET A0(1) * AM SYNC(1)B | DM-2(2) |
| | | SYNC 0(0) | CLR SYNC * SYNC 0(1) | DM-2(1) |
| | D PHASE | SET D0(1) | D PHASE * SET D0 EN | DM-2(1) |
| | | SYNC 0(1) | D PHASE * SYNC 0 EN | DM-2(1) |
| | | AM RQ | SYNC 0(1) | DM-2(2) |
| | | AM GRANT | From PDP-9 | MC-2(1) |
| DATA XFER 1 SYNCING 2 | A PHASE | CH 0 ADDR ACC IN | A PHASE * SET A0(1) * SET D0(1) | DM-2(1) |
| | | CH 0 ADDR ACC | CH 0 ADDR ACC IN | DM02(1) |
| | | DEV 0 CONT (1) | SET D0(1) * CH 0 ADDR ACC IN | DM-2(1) |
| | | AM STROBE | From PDP-9 | MC-2 |
| | | SAI | $\overline{\text{CH 0 RQ IN}}$ * SET D0(1) * AM STROBE | DM-2(2) |
| | | SYNC 0(0) | CLR SYNC * SYNC 0(1) | DM-2(1) |
| | | CH 0 FAST CLR | CLR SYNC * SYNC 0(1) | DM02(1) |
| | D PHASE | CH 0 DATA RDY IN | D PHASE * SET D0(1) * $\overline{\text{SLOW CYCLE D(0)}}$ | DM-2(2) |
| | | CH 0 DATA RDY | CH 0 DATA RDY IN | DM-2(2) |
| | | AM GRANT | From PDP-9 | MC-2(1) |
| | | CLR SLW CYC EN | SET A0(0) * SET D0(1) | DM-2(1) |
| DATA XFER 2 | A PHASE | SLOW CYCLE A(0) | A PHASE * CLR SLW CYC EN | MC-2(1) |
| | | CH 0 ADDR ACC IN | A PHASE * SET A0(1) * SET D0(1) | DM-2(1) |
| | | CH 0 ADDR ACC | CH 0 ADDR ACC IN | DM-2(1) |
| | | AM STROBE | From PDP-9 | MC-2 |
| | | SAI | $\overline{\text{CH 0 RQ IN}}$ * SET D0(1) * AM STROBE | DM-2(2) |
| | D PHASE | SET D0(0) | D PHASE * SET A0(0) * SLOW CYCLE D(0) | DM-2(1) |

## 5. ACCEPTANCE TEST PROCEDURE

Acceptance testing of the DM09A option consists of executing Test Procedure DM09A-0 with the DM09A Tester at both normal operating conditions and the voltage margins specified below.

| Trial | Test | Aggravation Condition |
|---|---|---|
| 1 | DM09A-0 | None |
| 2 | DM09A-0 | Margin rack A |
| 3 | DM09A-0 | Margin rack B |

Minimum margin specifications for rack A and rack B are listed below.

Margin

| +10V | | -15V | |
|---|---|---|---|
| +6V | -6V | +4V | -4V |

## 6. MAINTENANCE

### 6.1 General

The general maintenance procedures described in the PDP-9 maintenance manual also apply to the DM09A option.

### 6.2 Delay Adjustments

Adjust the R302 Delay at A27 according to the data given on engineering drawing DM-2(2).

### 6.3 Module Complement

Table 6-1 lists the module complement of the DM09A option.

Table 6-1
Module Complement

| DEC Type | Module Type | Quantity | Recommended Spare Quantity |
|---|---|---|---|
| B169 | Inverter | 17 | 2* |
| B213 | Jam Flip-Flop | 14 | 1* |
| R002 | Diode Cluster | 2 | 1* |
| R111 | Diode Gate | 12 | 1* |
| S107 | Inverter | 2 | 1* |
| S202 | Dual Flip-Flop | 7 | 1* |
| S203 | Triple Flip-Flop | 1 | 1* |
| S603 | Pulse Amplifier | 5 | |
| W005 | Clamped Loads | 3 | 1* |
| W300 | Delay Line | 1 | 1 |
| W612 | Pulse Amplifier | 8 | |
| R302 | One-Shot Delay | 1 | 1* |

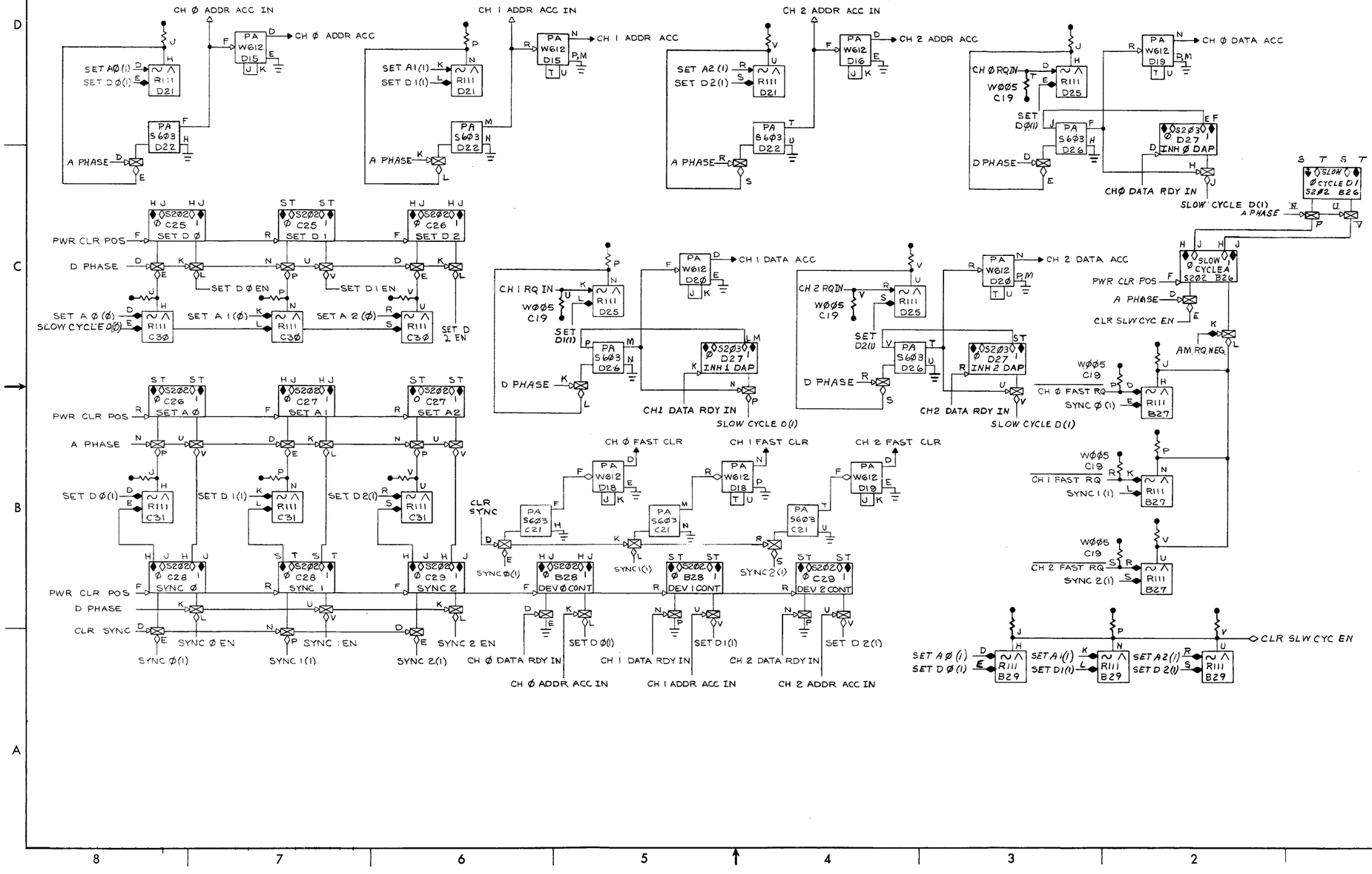
*Contained in the basic processor spare parts kit.

## 7. ENGINEERING DRAWINGS

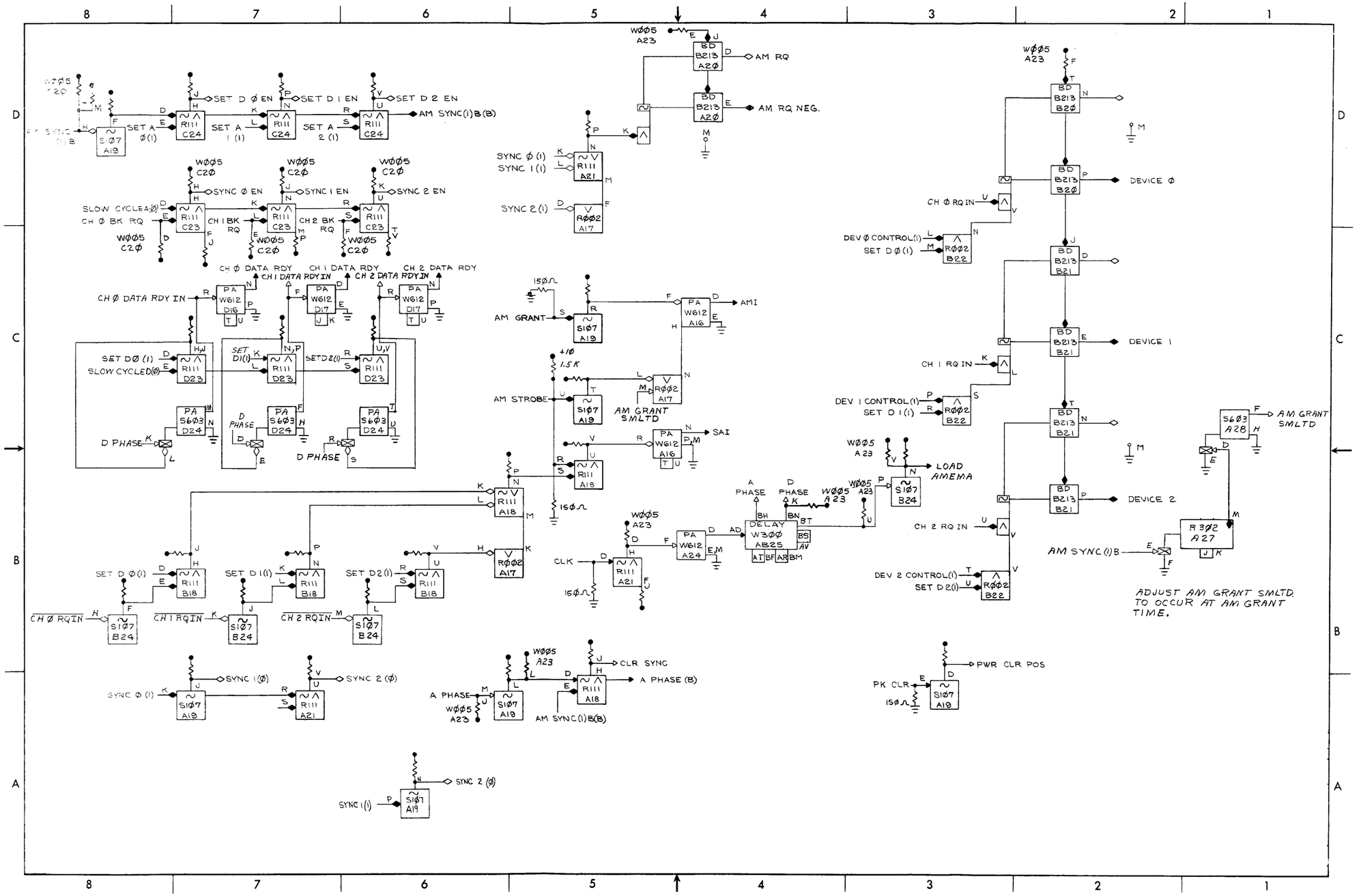
Table 7-1 lists the DEC engineering drawings associated with the DM09A option.

Table 7-1
Engineering Drawings

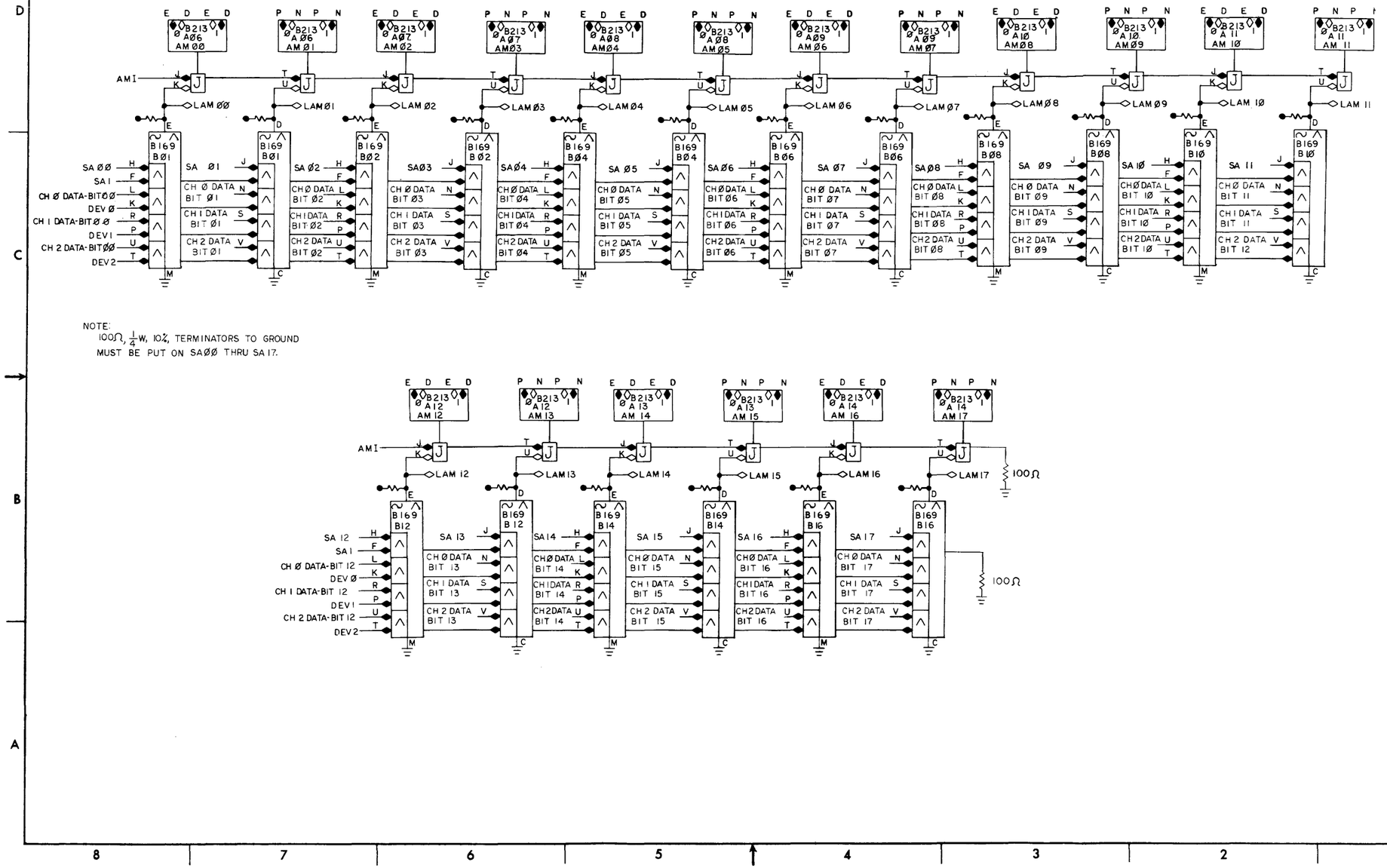
| Drawing Number | Title | Revision |
|---|---|---|
| DM-2(1) | DMA Adapter Multiplexer Control BS-DM09-A-2 Sheet 1 of 2 | J |
| DM-2(2) | DMA Adapter Multiplexer Control BS-DM09-A-2 Sheet 2 of 2 | J |
| DM-3(1) | AM Register BS-DM09-A-3 Sheet 1 of 2 | B |
| DM-3(2) | AM Register BS-DM09-A-3 Sheet 2 of 2 | B |
| DM-4(1) | Cable Diagram BS-DM09-A-4 Sheet 1 of 2 | O |
| DM-4(2) | Cable Diagram BS-DM09-A-4 Sheet 2 of 2 | A |
| DM-5 | Module Utilization MU-DM09-A-5 | H |
| DM-8(1) | DM09A Timing Diagram TD-DM09-A-8 Sheet 1 of 2 | O |
| DM-8(2) | DM09A Timing Diagram TD-DM09-A-8 Sheet 2 of 2 | O |




BS-DM09-A-2 Sheet 1 of 2 DMA Adapter
Multiplexer Control

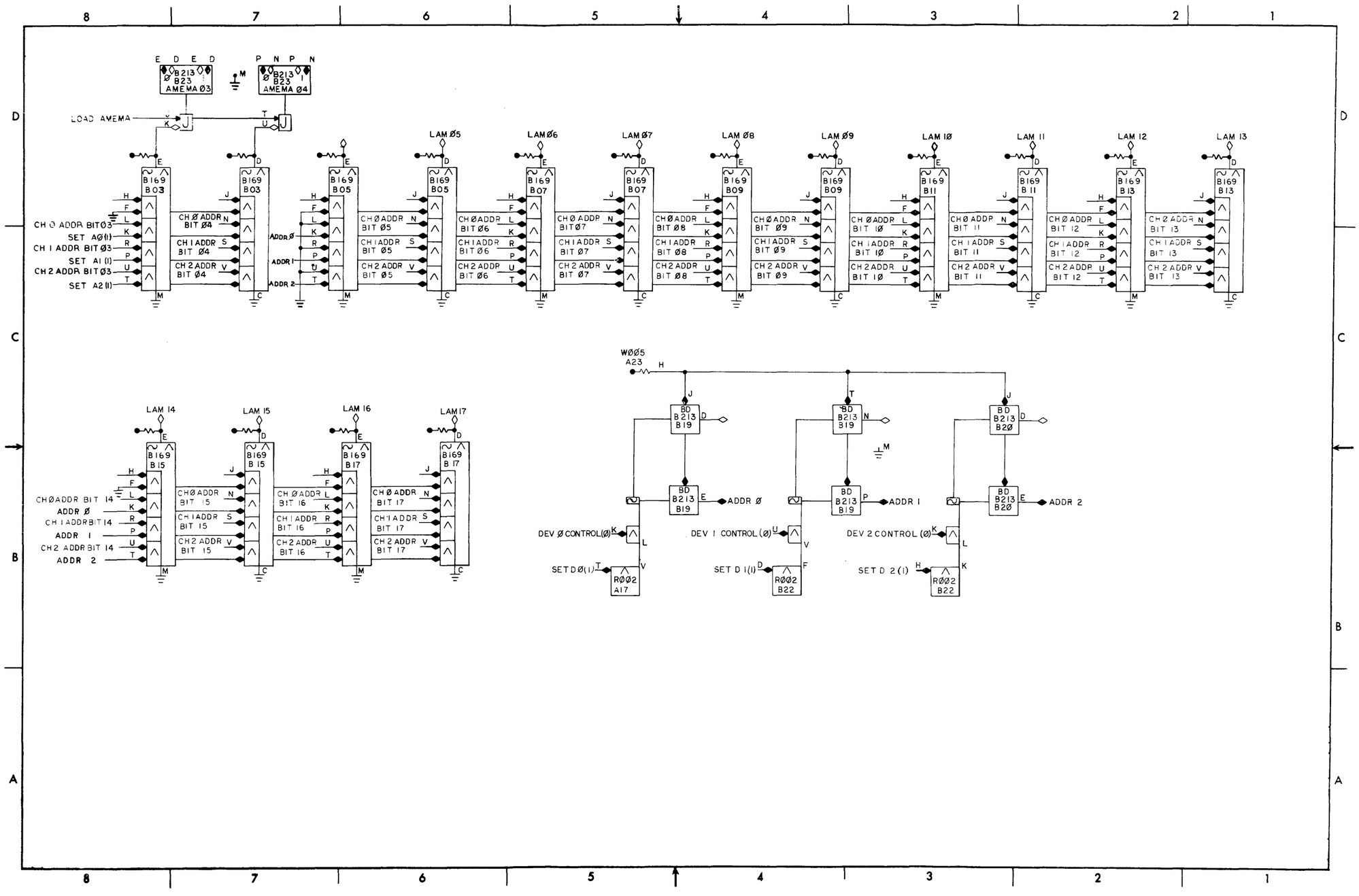



BS-DM09-A-2 Sheet 2 of 2 DMA Adapter
Multiplexer Control




NOTE:
100Ω, $\frac{1}{4}$W, 10%, TERMINATORS TO GROUND MUST BE PUT ON SAØØ THRU SA 17.

BS-DM09-A-3 Sheet 1 of 2 AM Register


LOAD AMEMA
AMEMA Ø3
AMEMA Ø4
LAM Ø5
LAM Ø6
LAM Ø7
LAM Ø8
LAM Ø9
LAM 1Ø
LAM 11
LAM 12
LAM 13
CH Ø ADDR BIT Ø3
SET A0(1)
CH 1 ADDR BIT Ø3
SET A1 (1)
CH 2 ADDR BIT Ø3
SET A2 (1)
LAM 14
LAM 15
LAM 16
LAM 17
CH ØADDR BIT 14
ADDR Ø
CH 1 ADDR BIT 14
ADDR 1
CH2 ADDR BIT 14
ADDR 2
WØØ5 A23
ADDR Ø
ADDR 1
ADDR 2
DEV Ø CONTROL(Ø)
DEV 1 CONTROL (Ø)
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SET D 1(1)
SET D 2(1)
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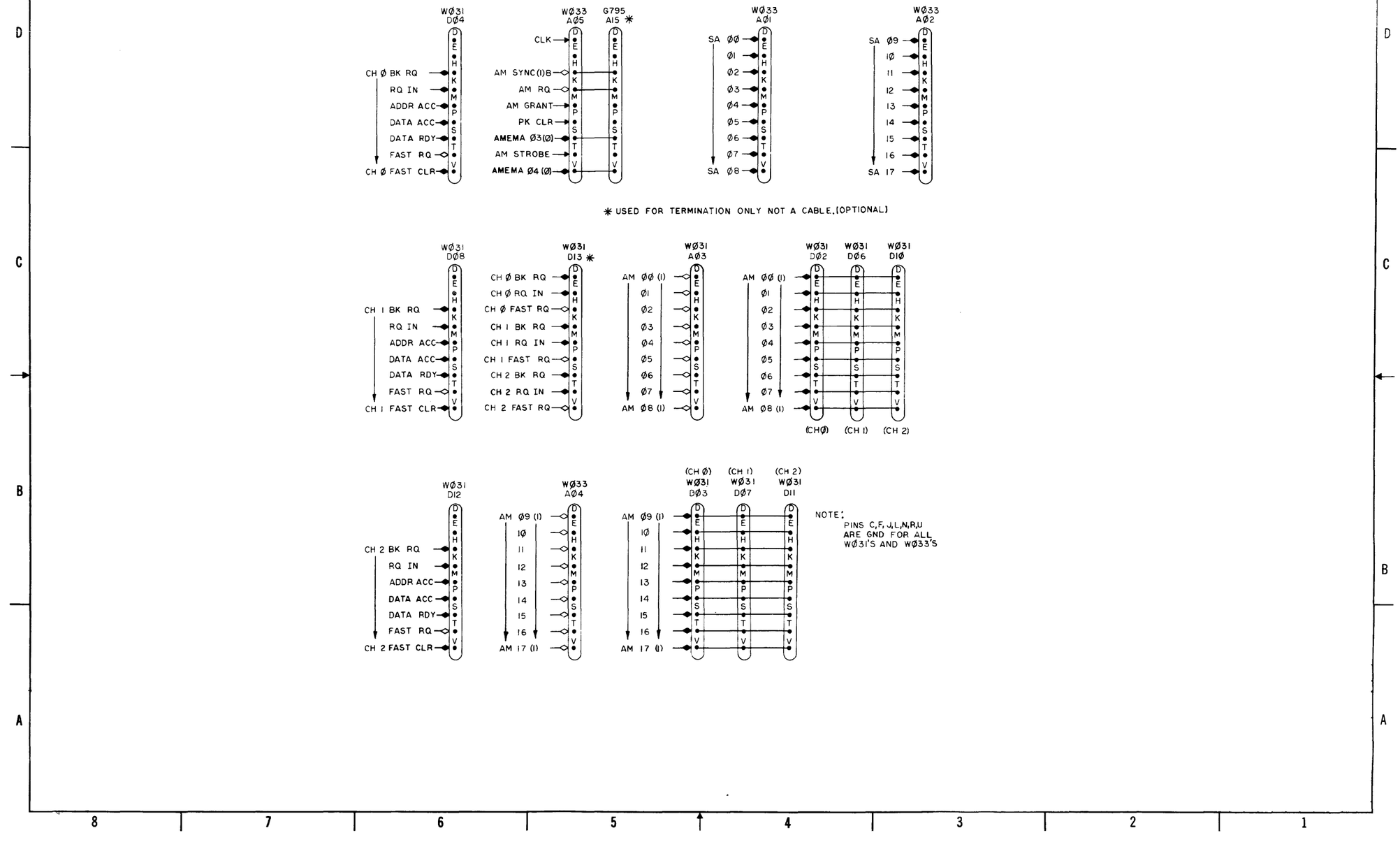
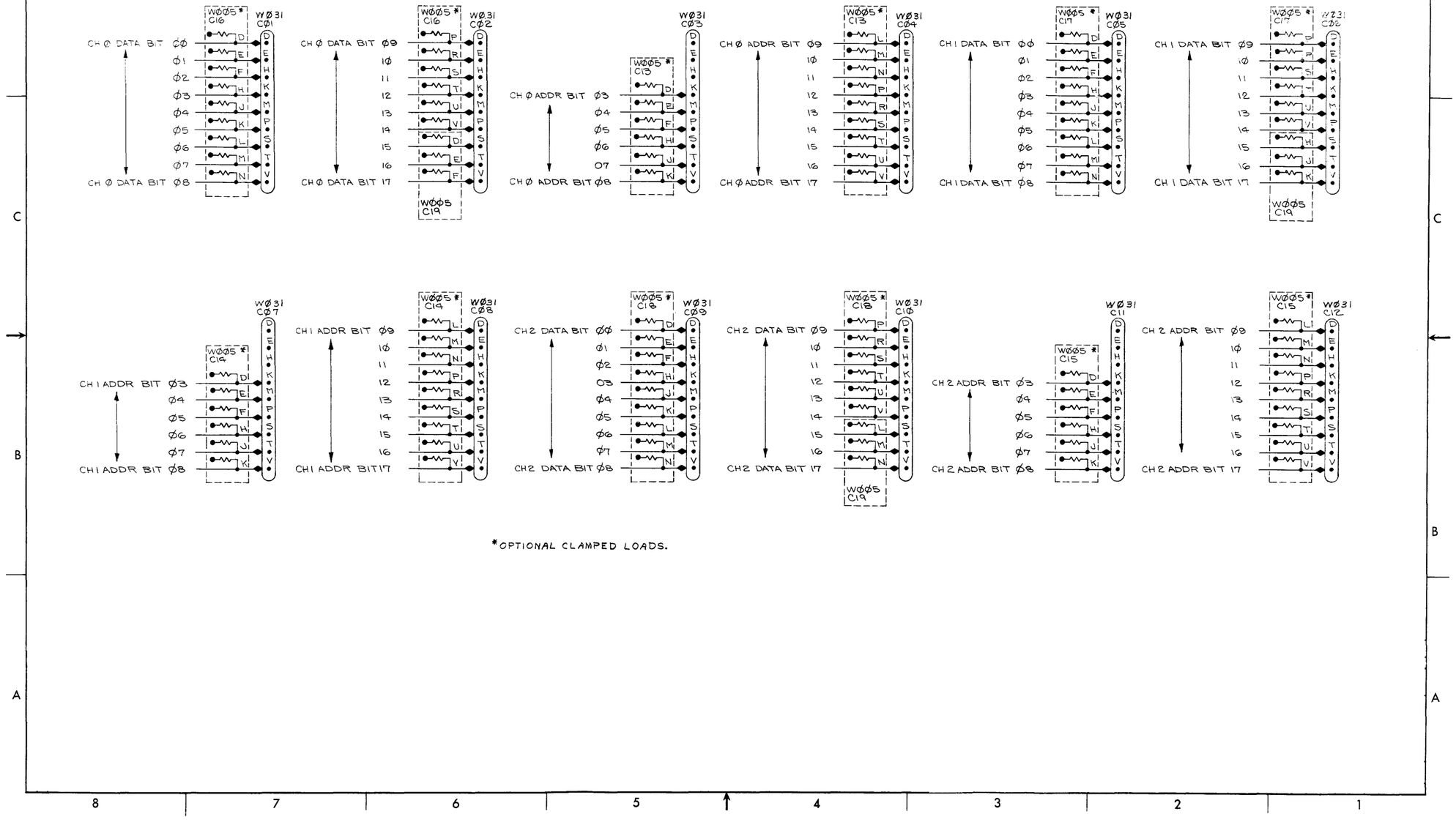
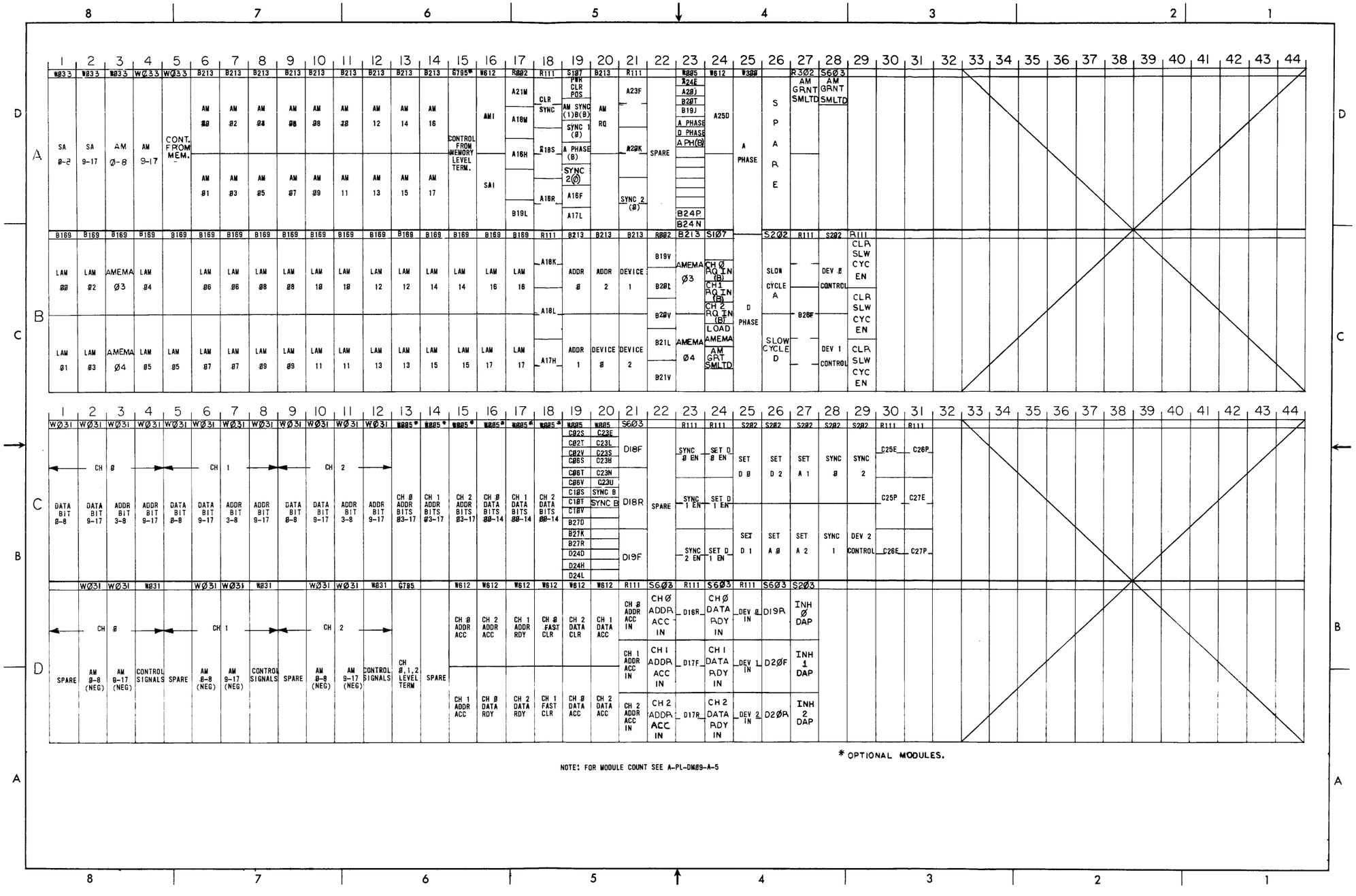
RØØ2 B22
RØØ2 B22

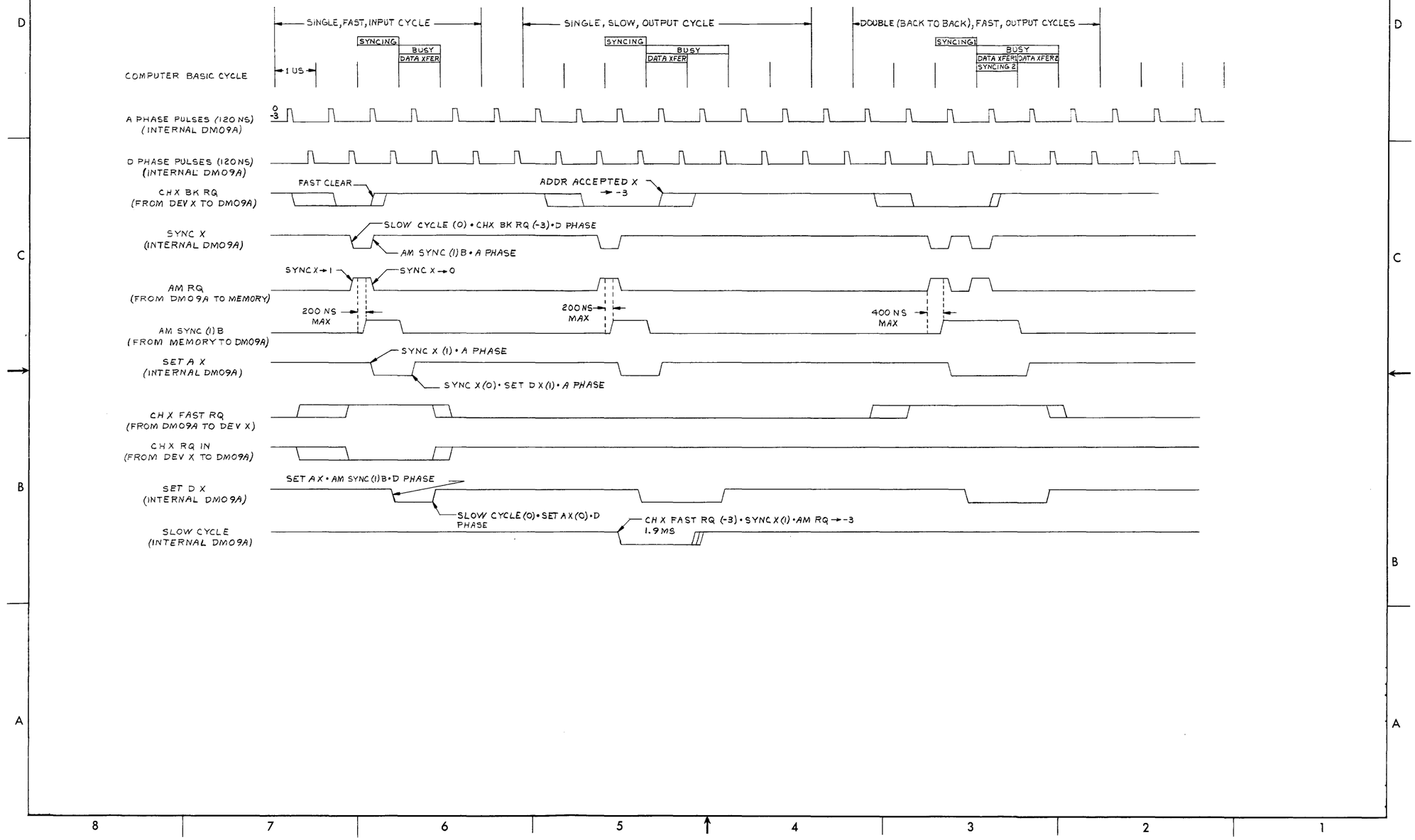



BS-DM09-A-4 Sheet 1 of 2 Cable Diagram

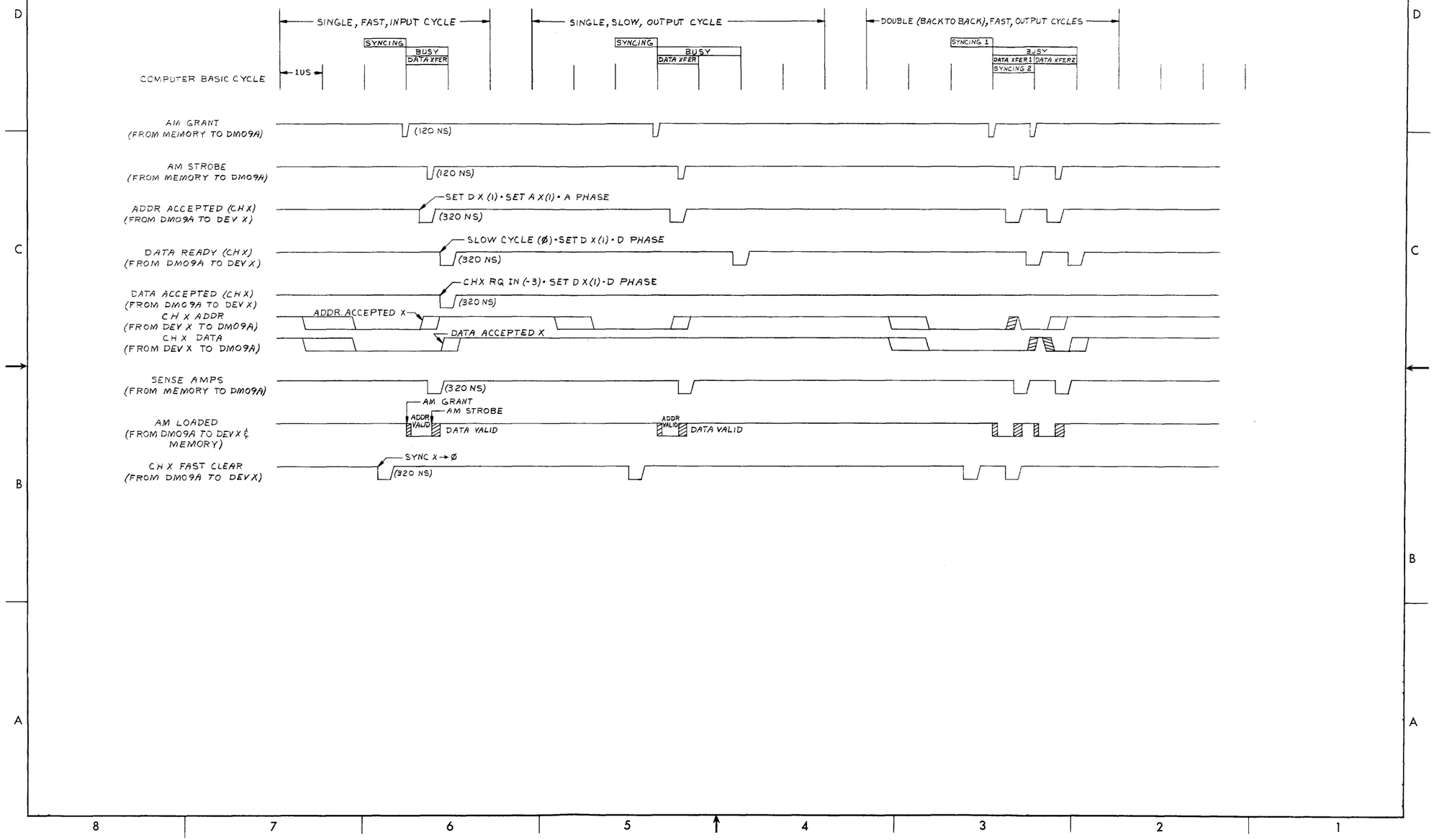



BS-DM09-A-4 Sheet 2 of 2 Cable Diagram

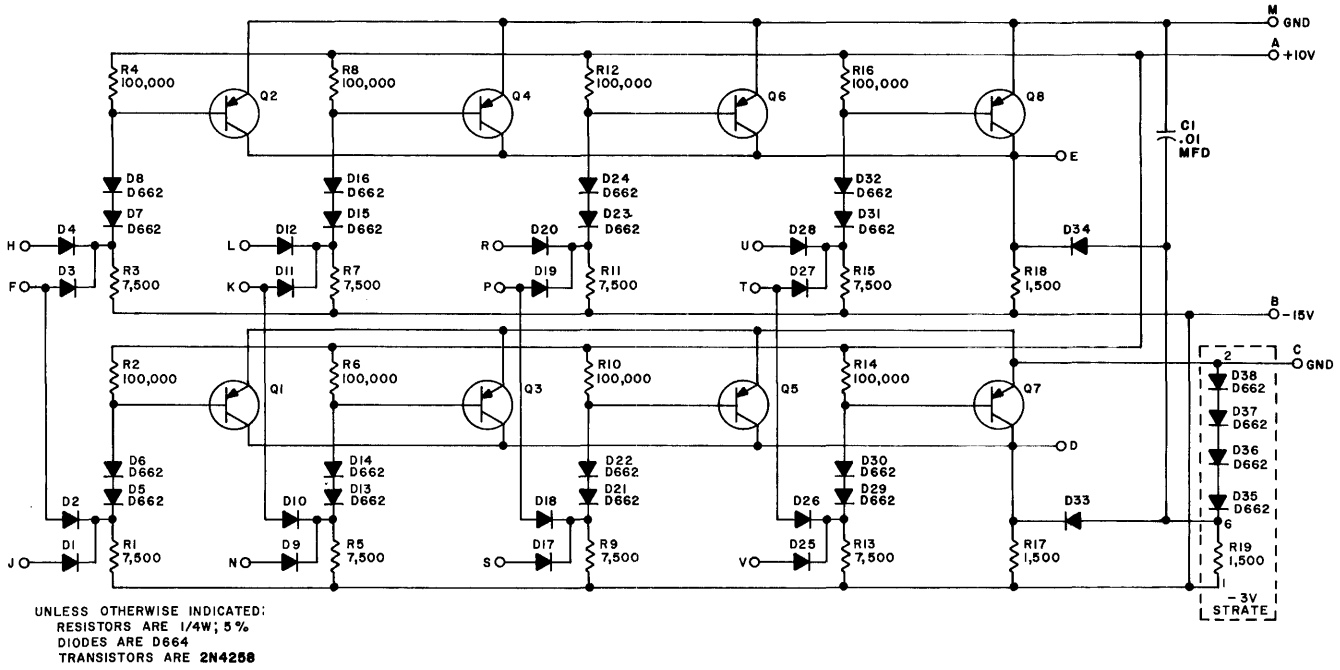

* OPTIONAL MODULES.
NOTE: FOR MODULE COUNT SEE A-PL-DM09-A-5



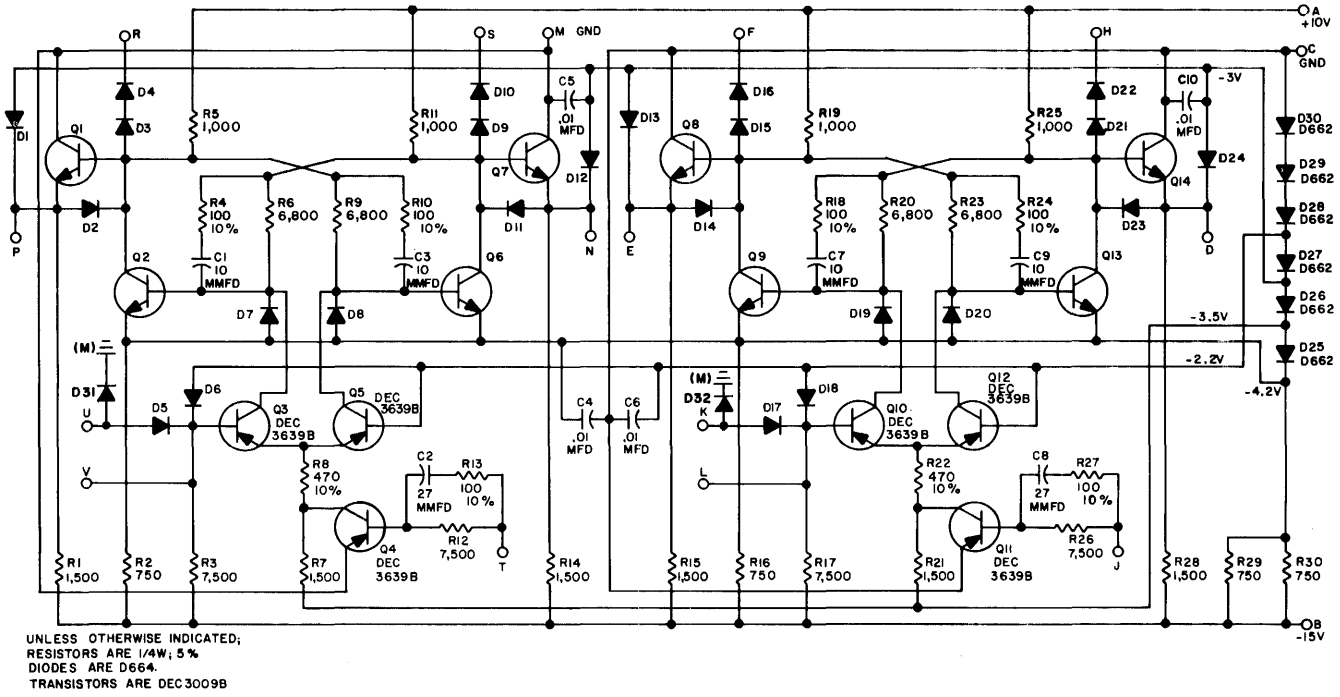

TD-DM09-A-8 Sheet 1 of 2 DM09A
Timing Diagram



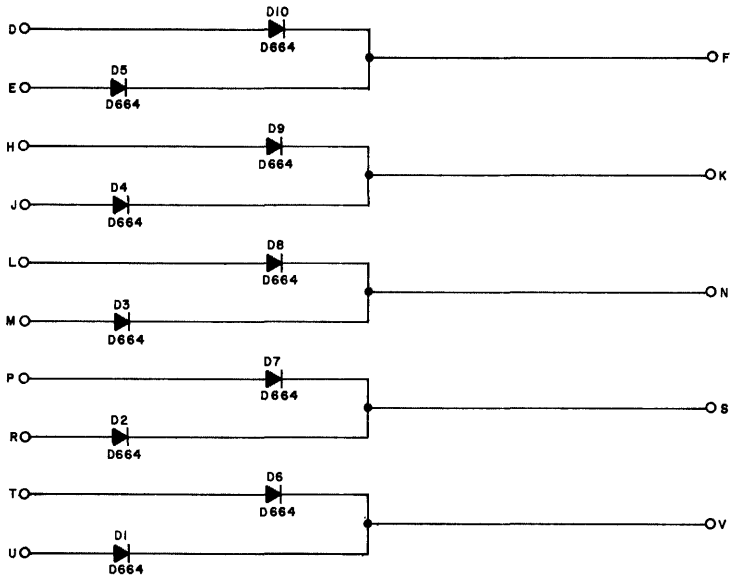

TD-DM09-A-8 Sheet 2 of 2 DM09A
Timing Diagram



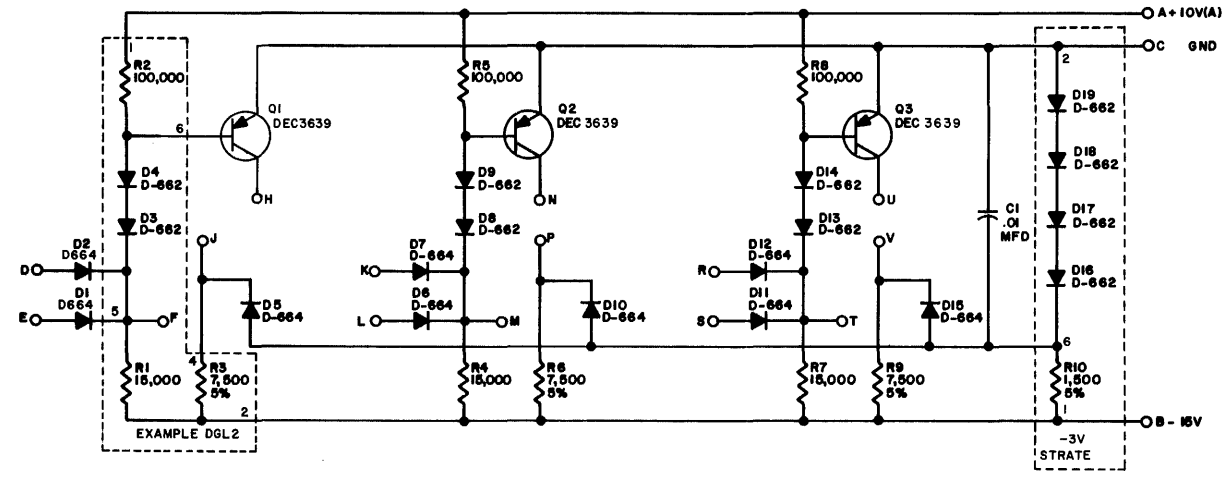

B-CS-B169-0-1 Inverter




B-CS-B213-0-1 Jam Flip-Flop

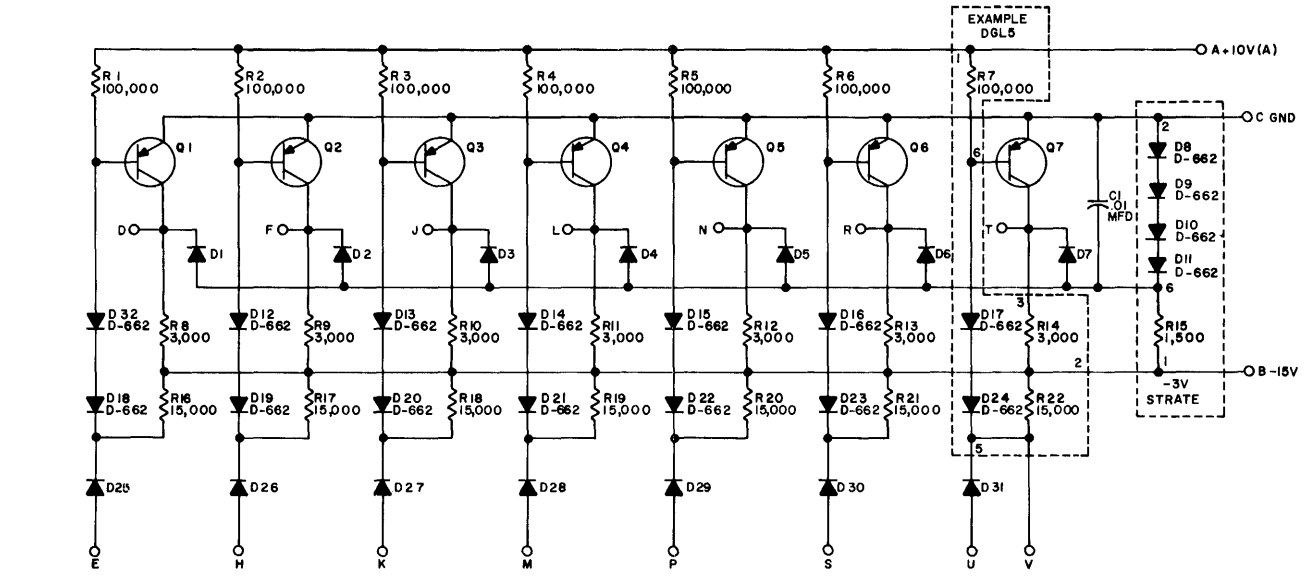



B-CS-R002-0-1 Diode Cluster



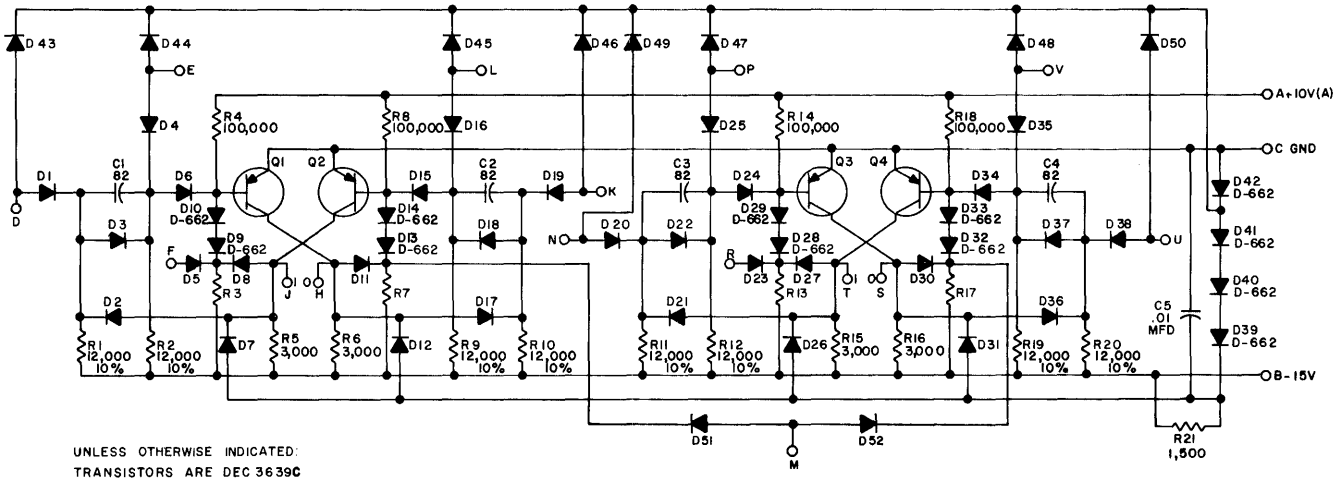

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIB

B-CS-R111-0-1 Diode Gate



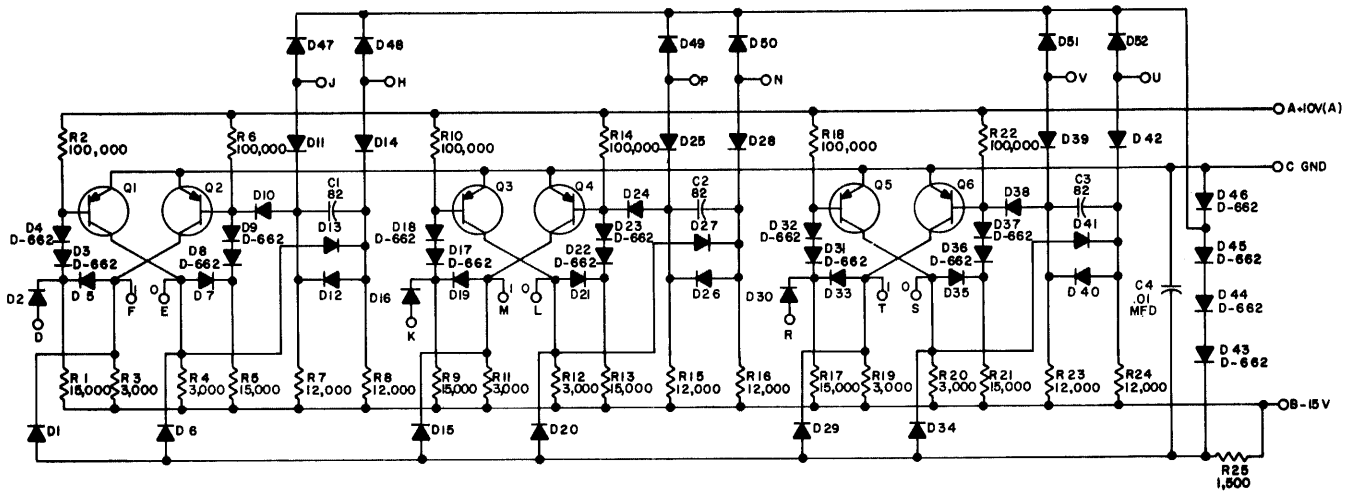

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W;5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639B
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

B-CS-S107-0-1 Inverter



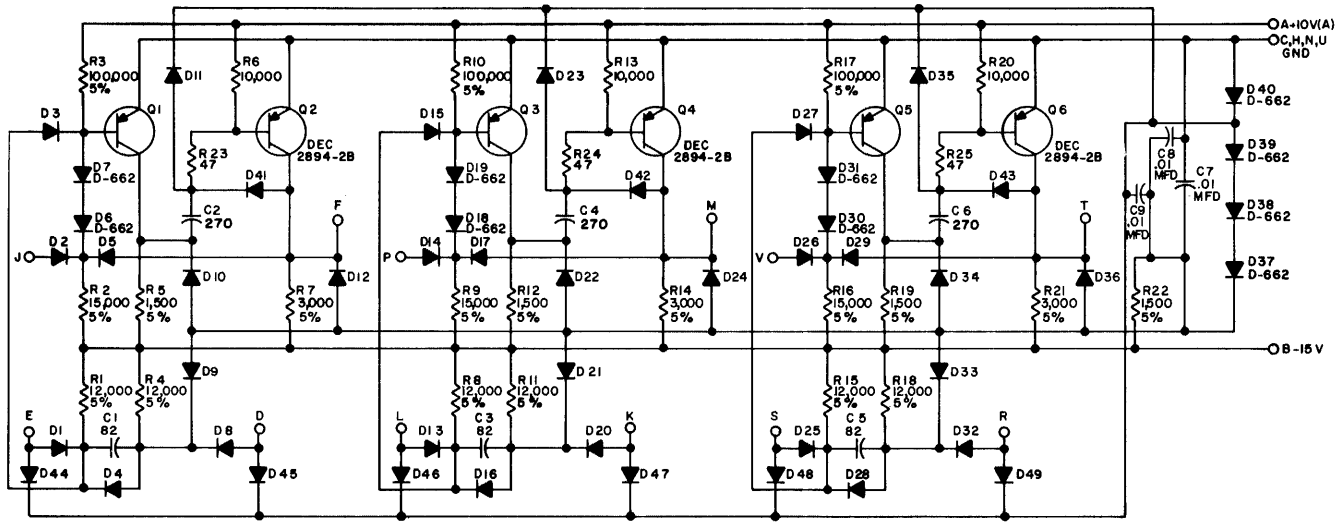

UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639C
RESISTORS ARE 15,000
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

B-CS-S202-0-1 Dual Flip-Flop



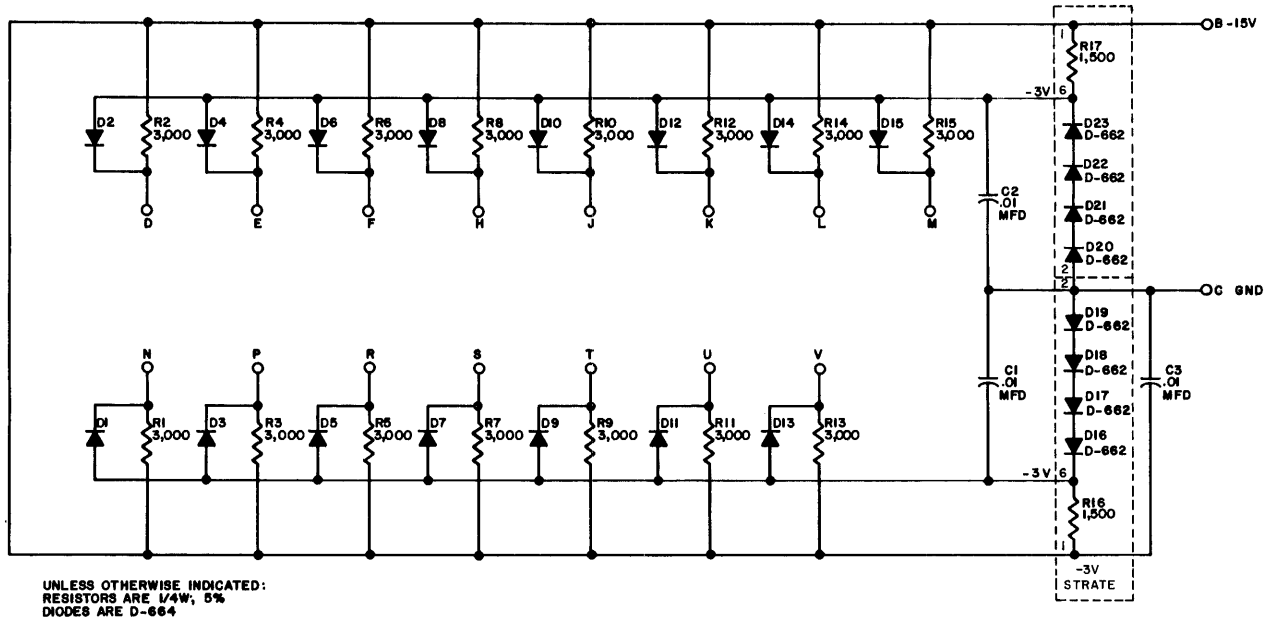

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639C

B-CS-S203-0-1 Triple Flip-Flop

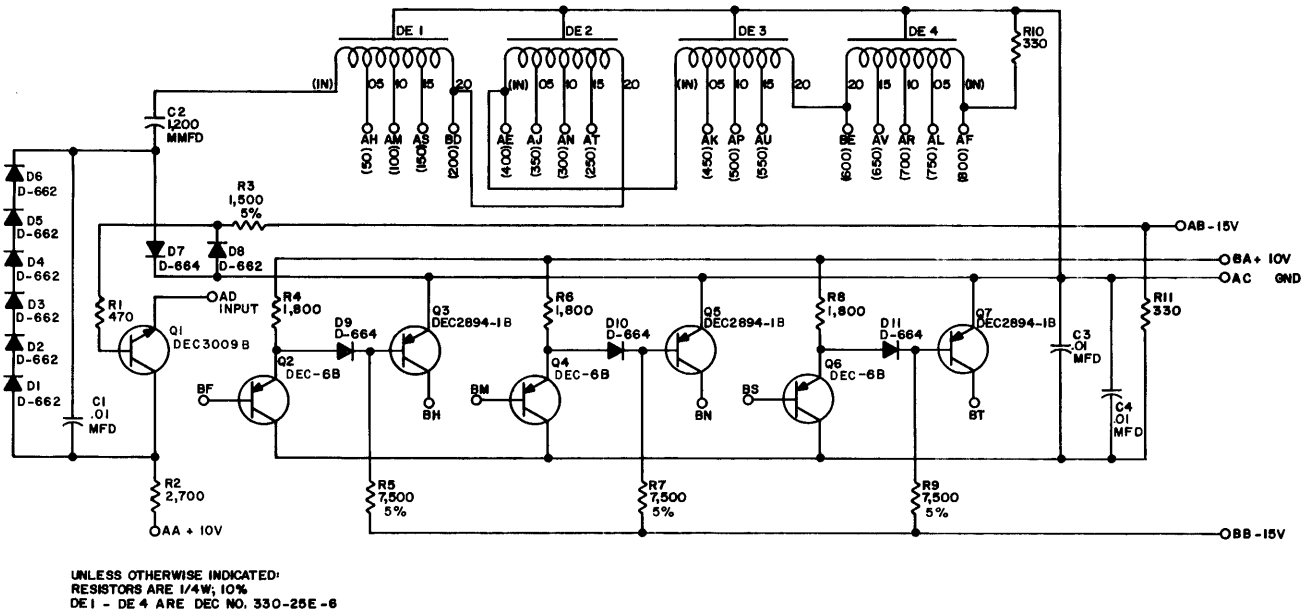



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639-C

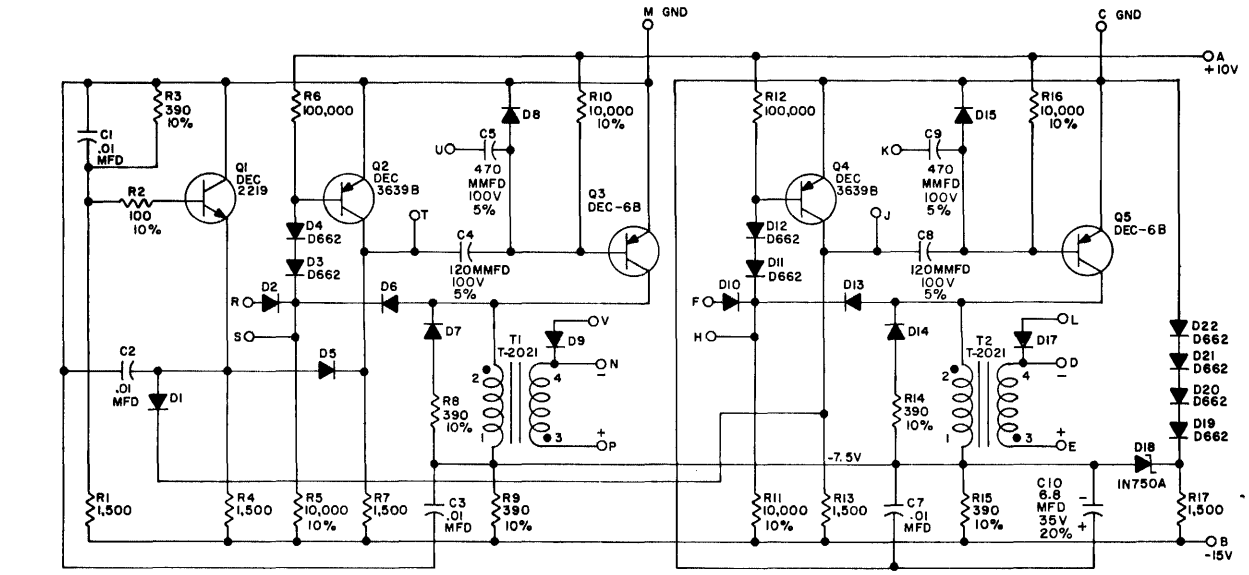
B-CS-S603-0-1 Pulse Amplifier




B-CS-W005-0-1 Clamped Loads

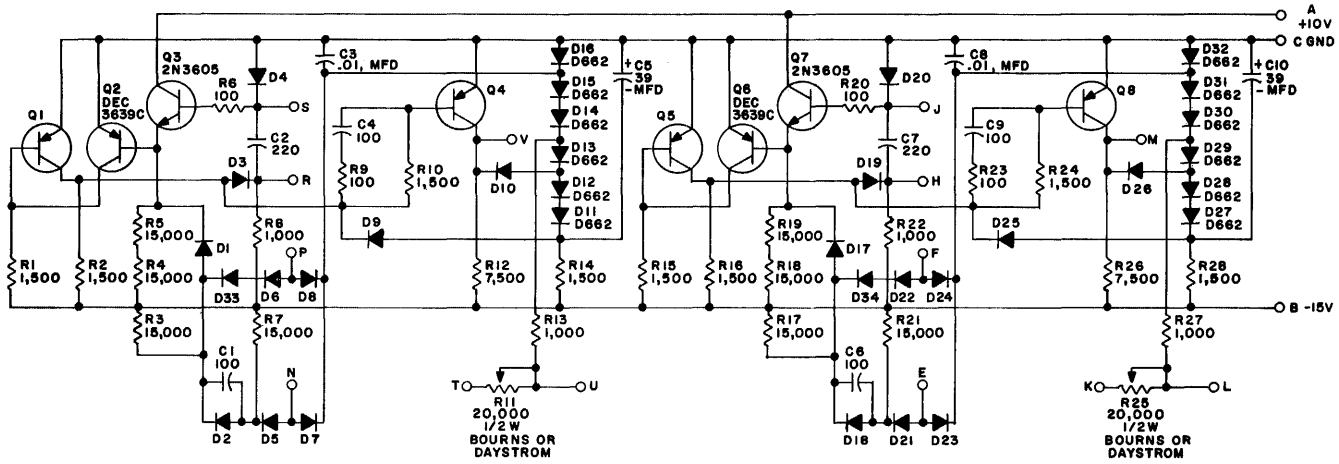



B-CS-W300-0-1 Delay Line




UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D664

B-CS-W612-0-1 Pulse Amplifier




UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D664
TRANSISTORS ARE DEC3639

B-CS-R302-0-1 One-Shot Delay

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