PROGRAMMED
DATA PROCESSOR-4
MAINTENANCE MANUAL

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CHAPTER 1

INTRODUCTION

1-1 PURPOSE AND SCOPE

The purpose of this instruction manual is to aid personnel in the installation, operation and maintenance of the DEC programmed data processor, PDP-4. The manual contains complete descriptions of all portions of the standard PDP-4, and also describes several optional additions to the PDP-4 input-output system.

1-2 CHAPTER SUBJECTS

A brief summary of system use and application is presented in Chapter 2, General Description. This chapter also contains a listing of system specifications and physical characteristics.

Chapter 3, Installation, provides instructions for initial installation and set-up of the system.

Chapter 4, System Function, provides a full functional description of all system operations. This chapter is written at a block diagram level, and explains what the system does, rather than the way in which its functions are implemented in terms of hardware. Also included in Chapter 4 is an explanation of the flow diagrams which show the actual operations performed by the computer in the execution of the various program instructions and console functions.

Chapter 5, Operating Procedures, explains the use of all controls and indicators on the computer control panels. This chapter also outlines the basic procedures to be followed for normal computer operation.

Four chapters contain a detailed description of system logical design. The first of these is Chapter 6, Control, which covers the computer timing system, the control of computer states, and program control. Chapter 7, Arithmetic Unit, is a detailed description of the accumulator and the associated logic required for logical and arithmetic computer operations. Chapter 8, Memory, covers the operation of the computer core memory system. Chapter 9, Input-Output System, explains the control of the standard photoelectric tape reader, furnished with the basic PDP-4. This chapter also describes three optional additions to the input-output system:

the real time option, the control unit for the paper tape punch, and the control unit for the keyboard/printer.

Chapter 10, Circuit Description, explains the function, specifications, and theory of operation of the circuit modules used in the PDP-4 system.

Chapter 11, Maintenance, contains information useful for the adjustment, calibration, troubleshooting and repair of the computer.

1-3 FIGURES

This manual includes three general classes of figures: logic diagrams, circuit schematics, and miscellaneous figures such as photographs and block diagrams. The complete system logic is shown in logic drawings for Chapters 6, 7, 8 and 9. The circuit schematics accompany Chapter 10. The block diagrams and photographs illustrate Chapters 2, 3, 4, 5, 9 and 11. Also included in Chapter 11 are various layout drawings, and cabling and wiring diagrams.

All figures are assembled in numerical order at the back of the manual. Figure references to all illustrations except the circuit schematics are of the form "Figure 5-1" (i.e., the first figure referred to in Chapter 5). This circuit schematics are arranged in order by circuit type designation.

CHAPTER 2

GENERAL DESCRIPTION

2-1 PURPOSE OF SYSTEM

The DEC Programmed Data Processor -4 is a compact solid-state stored program digital computer. The PDP-4 is designed explicitly to bring to special purpose systems the flexibility, economy, and reliability of a production model general purpose machine. The basic function of the PDP-4 is to collect information from, and distribute information to a wide variety of peripheral devices according to a predetermined set of instructions. The computer may also be used to advantage for many test and training applications.

The PDP-4 is a single address, general purpose computer, operating on 18-bit binary numbers. A random access magnetic core memory with a complete cycle time of eight microseconds achieves a computation rate of 62,500 additions per second. The computer can, with single instructions, perform both 1s complement and 2s complement addition.

The PDP-4 includes all essential elements for optimum performance as a systems component. The standard machine consists of:

An Internal Processor, which performs all computational operations, controls the memory, and handles information entering and leaving the machine;

An Operator Console, which contains all controls needed to observe and modify the status of the internal processor;

A 1024 or 4096 Word Memory, which provides storage for information being collected or distributed and instructions for the internal processor; and

A Paper Tape Reader, which permits information and instructions to be read from five-, seven- or eight-hole perforated tape into the internal processor at the rate of 300 characters per second.

A broad assortment of optional input-output equipment may be controlled by the computer through the installation of a real time control. The PDP-4 is easy to install, operate and maintain, since it runs on ordinary 60 cycle, 117 volt current, features simplified controls, and contains built-in marginal checking to facilitate preventive maintenance. The standard

computer is housed in two DEC equipment frames. No special wiring, subflooring or air conditioning is required.

2-2 STANDARD EQUIPMENT

The equipment included in the standard PDP-4 is shown above the horizontal bar in Figure 2-1. The internal processor contains both the control unit and the arithmetic unit.

The PDP-4 is available in two standard froms, depending upon the size of the core memory. The core memory in the PDP-4A has a storage capacity of 1024 18-bit words. The core memory in the PDP-4B has a storage capacity of 4096 18-bit words. Instructions are carried out by the control circuits in multiples of the eight-microsecond memory cycle time. For example, add, deposit, and load are two-cycle instructions requiring 16 microseconds. The control unit contains all of the registers and control circuits necessary to execute the various instructions in the program, and to handle the transfer of information between memory and the registers within the internal processor.

The arithmetic unit includes an accumulator, a link register, and the control circuits necessary to execute all arithmetic and logical operations. The link provides a one-bit extension to the accumulator. It greatly simplifies the programming of double precision arithmetic, and allows the construction of products and quotients in multiplication and division by subroutine.

The standard PDP-4 includes one input-output device, a photoelectric paper tape reader. The reader is governed directly by the internal processor through the reader control unit.

Mounted on one of the bays in the standard PDP-4 is an operator console. The contents of all registers in the internal processor are displayed in the indicator lights on the console. This panel also includes the keys and switches that control the mode of operation of the computer, and the initiation of all operations within the computer.

2-3 EQUIPMENT OPTIONS

Some of the options which may be added to the standard PDP-4 are shown below the horizontal bar in Figure 2-1. The memory capacity of the PDP-4B may be expanded to 8192 18-bit words by adding the Type 17 Memory Option. This option includes a 4096 word core memory identical to that used in the PDP-4B, as well as several plug-in units which must be added to the internal processor to control the second memory module.

An assortment of input-output equipment may be added to PDP-4 by installing the Type 25 Real Time Option. This option includes a device selector which decodes the microinstruction portion of the in-out transfer instruction into in-out pulses. These pulses control the transfer of information between the in-out device control units and the internal processor. The in-out pulses also control the initiation of all operations within the device control units, and can sense the status of in-out devices for program control purposes. In addition to the device selector, the real time control also includes an information collector, an information distributor, an in-out skip facility, and an interrupt control.

The interrupt control allows program, clock and data interruptions. In a program interruption, a signal from an external device can interrupt the main program, transferring control to an appropriate subroutine. Clock interruptions allow the computer to count pulses on a 60 cycle clock so that the computer can be synchronized to durations in real time. In a data interruption, the program pauses for one memory cycle, while an external device gains direct access to memory.

A wide variety of input-output options is available for use with PDP-4. Two of the most common options are the following:

Keyboard/Printer and Control Type 65. The Type 65 is a Teletype Model 28 Keyboard and Printer, with an input and printing speed of ten characters per second.

Paper Tape Punch and Control Type 75. The Type 75 is a Teletype BRPE Punch, with an operating speed of 63.3 lines or characters per second. It punches eight-hole tape. However, the punch may be modified to punch five-hole tape or seven-hole tape, if desired by the user.

2-4 SYSTEM OPERATING SPECIFICATIONS

SYSTEM CHARACTERISTICS

Application	General purpose
Timing	Synchronous
Operation	Parallel processing

COMPUTER WORDS

Word length	18 bits
Number length	Sign: 1 bit; magnitude: 17 bits

Instruction length	
Memory reference	Instruction code: 4 bits Indirect addressing: 1 bit Address: 13 bits
Augmented	Variable instruction code; maximum length: 18 bits
Instruction type	Single address

ARITHMETIC UNIT

Internal number system	Binary
Operation	Fixed point
Number range	$-(1 - 2^{-17}) \leq n \leq (1 - 2^{-17})$
Addition time	16 microseconds, including both instruction and operand access

STORAGE

Media	Magnetic cores
Cycle time	8 microseconds
Capacity	1024 words, or 4096 words expandable to 8192 words

INPUT-OUTPUT SYSTEM

Photoelectric Tape Reader	300 characters/second 5-, 7- or 8-hole paper tape
Paper Tape Punch	63.3 characters/second 5-, 7- or 8-hole paper tape
Keyboard/Printer	10 characters/second

2-5 PHYSICAL CHARACTERISTICS

CONSTRUCTION

Internal processor, memory, and control units for in-out devices are housed in standard DEC bays (all steel construction). Control panel is aluminum.

MODULES

Standard DEC system plug-in units, series 1000 and series 4000.

POWER EQUIPMENT

Power supplies series 700; power controls series 800.

LOGIC

Solid-state. Transistors and crystal diodes utilizing static logic levels (0 vdc and -3 vdc).

DIMENSIONS

Standard PDP-4 (excluding table)

Height 69 1/2 inches

Length 42 inches

Width 27 inches

Computer table

Height 27 inches

Width 80 inches

Depth 23 inches

Reader

Height 8 1/2 inches

Width 19 1/2 inches

Depth 18 inches

Standard PDP-4 including table and reader

Weight 940 pounds

Reader and punch

Height 23 inches

Width 19 1/2 inches

Depth 18 inches

Weight 90 pounds

Keyboard/printer

Height 15 3/4 inches (29 1/4 inches with top up)

Width 20 1/2 inches

Depth 23 1/2 inches

Weight 90 pounds

PDP-4 with table, reader, punch and keyboard/printer

Weight 1090 pounds

Memory expansion type 17

Requires extra bay, increasing length to 62 inches.

Weight 250 pounds

2-6 POWER REQUIREMENTS

LINE VOLTAGE INPUT

105 to 125 volts, 60 cycle, single phase

CURRENT CONSUMPTION

Standard PDP-4B	8 amperes; 940 watts
Memory expansion type 17	1.5 amperes
Reader	1.0 ampere; 125 watts
Keyboard/printer type 65	1.2 amperes; 60 watts
Punch type 75	1.2 amperes; 75 watts

NOTE: With reader, punch and keyboard/printer in use, the computer requires less than 12 amperes. However, because the punch draws a 9-ampere surge at turn-on, the computer should be connected to a 25-ampere line.

2-7 EQUIPMENT LISTING

The Standard PDP-4 and many of its options are housed in standard DEC bays. The front of each bay can accommodate up to twelve horizontal 19-inch mounting panels. Each panel can hold up to 25 of the standard DEC plug-in logic modules. Inside the double doors at the back of each bay is an inner plenum door. The required power supplies and power control panels are mounted on this door.

a BAYS - The PDP-4 with reader, punch and keyboard/printer is shown in Figure 2-2. The logic for the basic computer is contained in two DEC bays bolted together. As shown in the figure, the operator console is at the front of the computer (mounted at the side of bay 1). The rear of the bays is at the left side of the console. The inner plenum doors which hold the power equipment are inside the double doors shown in the figure.

In addition to the standard equipment, the real time option and the control units for the punch and keyboard/printer can be mounted in bays 1 and 2. The type 17 memory option

and most in-out options must be housed in separate units.

b LOGIC PANELS AND POWER EQUIPMENT - The mounting panels and logic wiring of PDP-4 are shown in Figure 2-3. Bay 1, containing the internal processor, the console and the control units for reader, punch and keyboard/printer, is at the left. Bay 2, containing the memory logic and the real time option is at the right. Below the real time option is a mounting panel for in-out plugs to connect the computer to peripheral equipment. Space for control units of optional devices is available below the in-out plugs.

Figure 2-4 shows the plenum doors on the backs of the bays. In the center of bay 2 are the large resistors for the memory power supply. At the top of bay 2 are the main power circuit breakers and the memory power switch. In the lower part of each bay are the type 728 power supplies. Each of these supplies provides +10 and -15 volts dc required by the plug-in modules.

Marginal check power supply controls are located at the top of bay 1. Behind these controls is a variable power supply type 734. The output of this unit can be varied from 0 to 20 vdc and can be applied to either the +10 or -15 volt lines in any logic panel for marginal checking the plug-in unit components.

Figure 2-5 shows the interior of bay 2. At the left are the backs of the logic panels; at the right is the inside of the plenum door. The plug-in units in the four panels at the top are logic circuits for core memory. The third memory panel also contains the core bank. Below the memory are three panels which contain the logic circuits for real time option. In-out plugs are located below the real time option.

At the bottom of the plenum door is a type 728 power supply which provides power for the logic in the bay. Above the 728 supply is the memory power supply type 735. At the top of the door is the power control panel containing delays and isolating circuits for the power switches.

A complete logic layout and power equipment layout of the PDP-4 is shown in Figure 2-6. The figure shows six type 728 power supplies -- four of which are required for the standard computer. The bottom supply in each bay is for optional equipment.

The following table lists the mounting panel and power equipment requirements for the standard PDP-4 and four options: Memory Expansion Type 17, Real Time Option Type 25,

Keyboard/Printer Type 65, and Punch Type 75.

(1) Standard PDP-4

Space requirement	2 bays
Logic panels	
Internal processor	6 mounting panels 1914 (1A to 1F)
Core memory	4 mounting panels 1914 (2A to 2D)
Reader control	1 mounting panel 1914 (1K)
Power equipment	4 power supplies 728
	1 variable power supply 734
	1 power supply 735
	1 power control panel 813
	1 marginal check switch panel

(2) Optional Equipment

Memory expansion type 17	
Space requirement	1 bay
Logic panels	4 mounting panels 1914
Power equipment	1 power supply 728; 1 power supply 735
Real time option type 25	
Logic panels	1 mounting panel 1914 (2E)
	2 mounting panels 1909 (2F, 2H)
Keyboard/printer control type 65	
Logic panels	1 mounting panel (1M)
Power equipment	1 power supply 728*
Punch control type 75	
Logic panels	1 mounting panel 1914 (1L)
Power equipment	1 power supply 728*

* If punch and keyboard/printer are both installed, only one extra power supply 728 is required.

c MODULE LIST - The following list includes all the plug-in modules required by the internal processor, the 1K and 4K core memories, reader control, memory option type 17, real time option type 25, keyboard/printer control type 65, and punch control type 75.

(1) Internal Processor - Numbers at the right are for the internal processor of PDP-4B. Negative numbers in parentheses indicate plug-in units that are removed for the PDP-4A. Positive numbers in parentheses indicate plug-in units that must be added to the internal processor if the type 17 memory option is installed.

Type	Quantity
Delay line 1310	2 (1)
Delay line 1311	1 (1)
Pulse amplifier 1607	1 (1)
Plug adapter 1956	3
Inverter 4105	3
Inverter 4106	6
Diode 4111	2
Diode 4112	3
Diode 4113	5
Diode 4114	5
Diode 4115	1
Capacitor-diode 4127	10
Capacitor-diode 4129	4
Binary-to-octal decoder 4150	4
Flip-flop 4203	19
Dual flip-flop 4204	21 (2) (-2)
Quadruple flip-flop 4214	1
Quadruple flip-flop 4218	2
Delay 4301	1
Integrating one-shot 4303	1
Clock 4401	1
Pulse generator 4410	1
Pulse amplifier 4604	17

(2) Core Memory - Plug-in unit requirements for the type 17 memory expansions are equal to the plug-in unit requirements for the 4K memory, plus the plug-in units that must be added to the internal processor (see (1) page 2-9)

Type	Quantity	
	PDP-4A (1K)	PDP-4B (4K)
Inverter 1103	6	7
Inverter 1104	1	1
Quadruple flip-flop 1213	1	1
Sense amplifier 1540	18	18
Pulse amplifier 1607	1	1
Power supply control 1701 (in power supply 735)	1	1
Read/write switch 1972	16	32
Memory driver 1973	2	2
Resistor 1976	8	16
Resistor 1978	3	3
Inhibit driver 1982	5	5

(3) Reader Control

Inverter 4105	1
Inverter 4106	3
Diode 4112	1
Capacitor-diode 4127	1
Quadruple flip-flop 4218	5
Pulse generator 4410	1
Pulse amplifier 4604	1

(4) Real Time Option Type 25

Bus driver 1690	8
Inverter 4102	1
Inverter 4105	1
Diode 4114	1

Type	Quantity
Diode 4115	1
Capacitor-diode 4127	1
Capacitor-diode 4129	20
Quadruple flip-flop 4218	2
Pulse generator 4410	1
Pulse amplifier 4604	9
Pulse amplifier 4605	3*

(5) Keyboard/Printer Control Type 65

Inverter 4105	1
Inverter 4106	1
Diode 4114	1
Capacitor-diode 4127	1
Capacitor-diode 4128	3
Quadruple flip-flop 4214	2
Four-bit counter 4215	4
Quadruple flip-flop 4216	2
Clock 4407	1
Pulse amplifier 4604	2
Pulse amplifier 4605 (added to device selector)	1
Solenoid driver 4681	1

(6) Punch Control Type 75

Inverter 4105	1
Diode 4113	2
Quadruple flip-flop 4216	2
Delay 4301	1
Pulse generator 4410	1
Pulse amplifier 4604	1

* For interrupt logic, status and reader; add 1 for each additional device.

Type	Quantity
Pulse amplifier 4605 (added to device selector)	1
Solenoid driver 4681	6

CHAPTER 3

INSTALLATION

3-1 GENERAL

This chapter provides the information needed to install the standard PDP-4 computer system and the more common in-out device options. Installation and inspection procedures are described, together with general information on initial testing and use of the checkout programs.

3-2 INSTALLATION OF THE STANDARD COMPUTER

The standard PDP-4 consists of a two-bay central frame, a photoelectric paper tape reader, and a separate table for the reader. The two most common items of optional in-out equipment are a paper tape punch and a keyboard/printer. The central frame is shipped fully assembled. The in-out equipment items are packed separately and must be installed before the system is ready for use.

a SITE SELECTION - Before installing the PDP-4 system, a suitable location must be selected. Space requirements for the system depend upon the quantity of optional equipment to be used. The floor area occupied by the central frame and the table is shown in Figure 3-1. The central frame is 69-1/2" high. At least 3 feet clearance should be allowed on all sides of the central frame for ease of access during maintenance.

Because the computer is mounted on casters, a level floor is required. The floor should be capable of supporting 150 pounds per square foot.

The system is designed to operate efficiently over an ambient temperature from 50° to 104°. The plug-in modules are cooled by blowing air out the front of the bays. Intake fans are mounted in the floor of each bay. All necessary fans and blowers are installed at the factory. No additional cooling equipment is required.

The user may elect to operate PDP-4 on either 110 or 220 vac. The internal power control connections for one type of line voltage or the other are made at the factory before shipment. Although the computer, including punch and keyboard/printer draws less than 12

amperes (at 110 vac) while in operation, turn-on surges in the in-out equipment (particularly the punch) may momentarily exceed this value. A 25 ampere line is therefore recommended if the punch is included in the system. (Additional power must be provided for other optional peripheral equipment.)

b UNPACKING AND HANDLING - The central frame is shipped on a skid, and may be crated or not, depending on the mode of transportation. For truck shipment it may be left uncrated. A crate is furnished for air shipment. The crate containing the central frame is approximately 74 inches high, 3 feet wide and 4-1/2 feet long. The table and tape reader are separately crated for all types of shipment.

(1) If the central frame is crated, carefully remove all crating and strapping, and any packing material. If the computer is shipped uncrated, remove any protective padding.

(2) The plenum doors at the rear of the central frame bays have spring catches. To reinforce these doors during shipment two bolts are used to hold each door shut. Remove these bolts and store them in the plastic loops provided.

(3) Remove any packing material, shipping blocks, etc. from the inside of the computer.

(4) The plug-in modules are taped into the logic panels to prevent damage in shipment. Remove the tape.

(5) Unpack the computer table and place it in front of the console (See Figure 2-2).

(6) Below the table is a panel of power plugs for the in-out equipment. On the floor of bay 1 is a power cable with a female plug. Run the cable through the hole in the bay floor and plug it into the single male socket in the power panel. The power cables for the in-out devices may be plugged into any of the four female sockets.

NOTE: If the user plans to reship the computer (or move it more than a short distance) in the near future, special packing materials should be saved for reuse. The containers for the reader, punch and keyboard/printer in particular, have been designed especially to accommodate the equipment, and are the safest means of packing it for reshipment.

c INSTALLATION OF TAPE READER - The single standard in-out device is a photoelectric paper tape reader. The reader is mounted in a cabinet, and the entire assembly is shipped in a single container. If the computer also includes a tape punch, the two devices are installed together (see paragraph 3-3a). For installation of the reader alone, follow the procedure listed below.

(1) Uncrate the reader and place it on the computer table. Remove the cabinet top by unscrewing the three Phillips screws on each side of the cabinet. Inspect the reader to make sure that nothing has come loose during shipment.

(2) The reader power and data cables are coiled inside the reader cabinet. Run the cables through the hole in the bottom of the cabinet, over the edge of the computer table, and through the trough connected to the underside of the table. The data connection from the reader to the computer is through a 22-pin Amphenol connector. Run the data cable into bay 1 through the hole in the computer floor, and plug it into the socket at the end of mounting panel 1K. Plug the power cable into one of the female sockets in the power plug panel.

(3) Replace the cabinet top.

3-3 INSTALLATION OF OPTIONAL EQUIPMENT

Two of the more common optional devices used with the PDP-4 are a paper tape punch and a keyboard/printer. If the punch is included in the system, the punch and the reader are installed together.

a READER AND PUNCH - The tape reader is mounted in a cabinet, and the entire assembly is shipped in a single container. The punch and its cabinet are shipped in separate containers. Packed inside the punch cabinet are the power and data cables, the punch cover, the tape catcher, and the chad box.

(1) Uncrate the punch cabinet and place it on the computer table. Open the door on the right side of the cabinet, and remove the punch cover, the tape catcher and the chad box. Coiled inside the cabinet are the power and data cables; these cables are attached to the switches on the front of the cabinet.

(2) Uncrate the tape reader. Place the reader cabinet on top of the punch cabinet, so that the hole in the bottom of the reader cabinet is directly above the hole in the top of the punch cabinet. Remove the top of the reader cabinet by unscrewing the three Phillips screws on each side. Inspect the reader to make sure nothing has come loose during shipment. Attach the reader cabinet to the punch cabinet by screwing down the two captive bolts at each side of the reader.

(3) The reader data and power cables are coiled inside the reader cabinet. Run these cables through the hole in the floor of the reader cabinet into the punch cabinet. Replace the top of the reader cabinet.

(4) Carefully uncrate the punch and remove all packing material. Check for loose wires, screws etc. Place several magazines or other such flat objects on the computer table under the open door of the punch cabinet. Place the punch on the open door.

(5) Attach the punch power and data cables to the punch. The power cable has a Twist-Lok connector; the data cable has an Amphenol type 57-30240 connector.

(6) Run the data and power cables for both the reader and the punch through the hole in the bottom of the punch cabinet, over the edge of the computer table, and through the trough attached to the underside of the table. The data cables are connected to the computer with 22-pin Amphenol connectors. Run the data cables into bay 1 through the hole in the computer floor. Plug the reader cable into the socket at the left end of mounting panel 1K. Plug the punch cable into the socket at the left end of mounting panel 1L.

(7) Place the cover on the punch. Note the two aluminum seating studs on the floor of the punch cabinet. The two mounting plates fit over these studs. Place the punch on the seating studs and determine that it is securely in position.

(8) Place the tape catcher in position and secure it to the cabinet floor by screwing down the two captive bolts. Hang the chad box in position on the front of the punch, and close the cabinet door.

(9) Plug the reader and punch power cables into the female sockets in the power plug panel.

b KEYBOARD/PRINTER - The keyboard/printer is shipped in a single container. The power and data cables are already connected to the unit, and are coiled under the unit inside the container.

(1) Uncrate the keyboard/printer, and place it on the computer table.

(2) Run the power and data cables over the edge of the table and through the trough attached to the underside of the table. The data cable is connected to the computer through a 22-pin Amphenol connector. Run the data cable into bay 1 through the hole in the computer floor, and plug it into the socket at the left end of mounting panel 1M. Plug the power cable into one of the female sockets in the power plug panel.

3-4 INSPECTION AND ADJUSTMENT

The PDP-4 system is thoroughly tested and checked before it leaves the factory. However, it should be inspected and checked again after installation to make sure that no damage has occurred during shipment.

a VISUAL INSPECTION - After the computer has been unpacked and the in-out equipment is in place, the system should be inspected visually. Check the following:

(1) Have all the shipping blocks, packing materials, tape, etc. been removed? If not, remove them.

(2) Are all plug-in units inserted firmly in position? Secure any that are loose.

(3) Are there any loose nuts or bolts? If so, tighten them.

(4) Are there any loose or broken wires? (Refer to Chapter 11 for repair of wiring.)

(5) Are the in-out device power and data cables plugged in?

(6) Make sure console POWER switch is off (left).

(7) Plug in system power cable (the coiled cable is on the floor of bay 2). The cable is equipped with a Miller Electric Type 034-2 connector.

CAUTION

Unless the system has been modified for use with 220 vac, the power cable must be plugged into a 110 volt outlet.

(8) Are the three MAIN POWER circuit breakers on the type 813 power control panel on? If not, turn them on (up). Make sure the MEM POWER switch is off (down).

b METER READINGS - Before starting to run the test program, all machine voltages should be checked with a meter.

(1) With the computer connected to its power source but with MEM POWER off, turn on the POWER switch on the console. The associated indicator should light.

(2) The type 728 power supplies each have three output lines: +10 vdc, ground, and -15 vdc. The output voltages should be checked for each type 728 supply before operating the computer. Measure these voltages at mounting panels 1A, 1F, and 2A. If the computer includes the optional real time control, also measure the voltages at mounting panel 2F. All A pins in each mounting panel are bussed together. Similarly, the B pins, the C pins, and the D pins are also bussed together. Pins A and B are at +10 vdc; pin C is at -15 vdc; pin D is at ground.

(3) Now turn on MEM POWER. This switch can now be left on permanently.

c PREOPERATIONAL CHECKOUT - The PDP-4 program library includes a set of DEC Maintenance Programs. These programs are designed to check out different portions of the computer to ensure that they are functioning correctly. Maintenance programs are a powerful aid in diagnosing computer malfunctions.

The test programs usually run at installation include Instruction Test, Checkerboard, Reader and Punch Test, and Teleprinter Input-Output Test. All of these programs are included in CONTEST, the consolidated maintenance test. Because all computer operations, including the running of test programs, depend on proper functioning of the instructions, the Instruction Test should be run first. After the computer has passed the Instruction Test, the memory Checkerboard should be run, followed by the Reader and Punch Test. The Teleprinter Input-Output Test should be run last.

More detailed instructions concerning use and applications of the PDP-4 maintenance programs are furnished in the maintenance chapter of this manual, Chapter 11.

CHAPTER 4

SYSTEM FUNCTION

4-1 LOGICAL ORGANIZATION

The logical configuration of the PDP-4 is shown in Figure 4-1. The computer logic is divided into four parts: control unit, arithmetic unit, memory and input-output system. The control unit and arithmetic unit together constitute the internal processor.

a CONTROL UNIT - The control unit of the computer governs the timing of all computer operations, the information transfers between the internal processor and the memory or input-output system, and the operation of the various registers. The control unit includes three internal registers, IR, PC and MA, and two console switch registers, AS and ACS.

The instruction code of each instruction is decoded from the four-bit instruction register, IR, to govern the execution of the instruction. Each instruction word is retrieved from the memory location specified by the contents of the 13-bit program counter, PC. During the execution of each instruction the program counter is advanced one position; consecutive instructions are thus taken from consecutive memory locations.

Every memory access is made to the location specified by the contents of the 13-bit memory address register, MA. The MA register is loaded from the program counter for instruction retrieval; it is loaded from the address portion of the instruction word (in the memory buffer) for either deferred address retrieval or memory reference. The operator can manually provide addresses and data words for use by the computer through two switch registers on the console control panel: the address switches, AS, and the accumulator switches, ACS.

In addition to these registers the control unit also includes the operating switches, the operating keys, and the control logic. The operating switches govern the mode of operation of the computer; the operating keys start and stop the specific computer operations. The control logic contains those control flip-flops and logic nets that govern computer states, information transfers, and the operation of computer registers. The control logic

also contains the timing system of the computer.

Most elements of the control unit are described in paragraph 4-3. However, those elements of control that are directly associated with the arithmetic unit or the memory are described in conjunction with those units (paragraphs 4-4 and 4-5 respectively).

b ARITHMETIC UNIT - The arithmetic unit includes two 18-bit registers, AC and MB, and a 1-bit register, L.

The memory buffer, MB, serves two distinct functions: a memory function, and an arithmetic function. All transfers of information between memory and the other parts of the computer are made through MB. The memory buffer is used in the arithmetic unit as a passive register, that is, it serves only to hold the operand in arithmetic and logical instructions. However, all indexing (i.e., incrementing by 1) is done directly in MB without using AC.

The accumulator, AC, is the major register in the arithmetic unit. It serves both as an accumulator and as an in-out register. The accumulator input logic includes transfer, rotate, logical, and arithmetic gating. The accumulator is used in the execution of all two-term logical and arithmetic instructions. Furthermore, the result of all such instructions always appears in the accumulator. The AC input gating allows the computer to perform the logic functions AND, exclusive OR, and negation, as well as arithmetic operation of addition. All other arithmetic operations must be programmed by using combinations of negation and addition. The inclusive OR function must be programmed by combining negation and conjunction.

The bits of AC can be rotated in either direction. The ends of the register are connected through the 1-bit link, L, and the 19-bit combination is rotated. Besides functioning as a computational register, AC also serves as the in-out register. All transfers of information between the computer and low-speed or programmed peripheral devices are made through AC.

The link, L, extends the capability of the accumulator. This 1-bit register connects the ends of AC so that the 19-bit combination of L and AC can be rotated as a single register. The programmer can use the link to construct products and quotients one bit at a time.

c MEMORY - Two versions of the standard PDP-4 are available, depending upon the type of memory module. The memory module of the PDP-4A provides storage for 1024 words; the memory module for the PDP-4B provides storage for 4096 words. Both modules are magnetic-core, coincident-current memories which store 18-bit words. The memory of PDP-4B can be expanded to 8192 words by adding the type 17 memory option. This option includes a 4096 word memory module and the necessary controlling circuits for the internal processor.

The lengths of the program counter and memory address register vary with the type of memory included in the computer. These registers may be 10, 12 or 13 bits in length, depending upon whether a 1K, 4K or 8K memory is used. During each 8-microsecond memory cycle, access is made to the memory location specified by the contents of MA. The addresses of the core registers in memory are always given in the octal number system so that the addresses are the same as the configuration of bits (taken three at a time) displayed in the console indicators. Addresses may therefore vary from 0 to 1777, 7777 or 17777 depending on memory capacity.

The word read from memory is transferred into the memory buffer by a strobe. Since the read operation is destructive, the word contained in MB must be written back into the core memory during the same cycle. In preparation for the deposit of new information in memory, the strobe is inhibited so the information read from the core register does not reach MB. New information is then transferred into MB from the internal processor, and written into the addressed memory location by the write portion of the memory cycle.

d INPUT-OUTPUT SYSTEM - The input-output system in the standard computer includes one input device--a paper tape reader with its associated control unit. The control unit is governed directly from the internal processor by in-out pulses generated from instructions in the in-out transfer group. All transfers of data between the reader buffer and the computer are made through the accumulator.

A large number of optional in-out devices may be added to the computer. Two of the more common optional devices are the paper tape punch for output, and the keyboard/-printer for both input and output. Whenever any optional in-out equipment is added to the computer, the real time option must also be installed. Then all devices (including the

reader) are controlled from the internal processor through the real time option. This option includes a device selector, an information distributor, an information collector, an in-out skip facility, and an interrupt control.

The device selector, DS, decodes the device code portion of the in-out transfer instruction (bits 6 to 11) and switches the in-out pulses from the internal processor to the control unit of the selected device. Transfers of data between the computer and the control unit buffers are made through the accumulator. Input information is gathered from various control units by the information collector, IC; output information is distributed to the various control units by the information distributor, ID. During in-out operations data transfers between a device and its associated control unit are performed automatically.

The interrupt control allows various external signals to interrupt the program sequence. A program break saves the current program address and transfers control to an appropriate subroutine. A clock break may be used to keep track of real time and thus correlate internal operations to real time. A data break causes the program to pause for one memory cycle while a high-speed automatic device makes direct access to memory. For example, with the automatic tape control unit, control information goes through the accumulator, but data is transferred directly between the memory buffer and the control unit through a direct access channel.

4-2 PROGRAMMING

This paragraph describes the programming characteristics and the instruction repertoire of PDP-4.

a NUMBER SYSTEM - PDP-4 is a fixed-point machine using binary arithmetic. Negative numbers are represented as either the ones complements or the twos complements of the positive numbers. Bit 0 is the sign bit, which is 0 for positive numbers. Bits 1 through 17 are magnitude bits, bit 17 being the least significant. The actual position of the binary point may be assigned arbitrarily to best suit the problem at hand. Two common conventions in the placement of the point are:

The binary point is placed to the right of the least significant bit; all numbers then represent integers.

The binary point is placed to the right of the sign bit; all numbers then represent fractions between -1 and +1.

Subroutines can automatically perform both the conversion of decimal numbers into binary for use in the computer, and also the output conversion of binary numbers into decimal. Operations for floating-point numbers are handled by interpretive programming or subroutines.

b INSTRUCTION FORMAT - There are two classes of PDP-4 instructions: memory reference instructions and augmented instructions.

Memory reference instructions need access to memory for an operand, and therefore require two memory cycles for execution. Augmented instructions, on the other hand, have no operand, and for this reason are performed in one memory cycle. The bits used to address the operand in the memory reference instructions are instead used, in the augmented instructions, to augment the control capability of the instructions. Accordingly, the augmented instructions are those instructions having augmented instruction codes.

There are also two instructions which fall into neither of these classes. These instructions, Jump and Load Accumulator with n, use their own address portions as operands and thus are executed in a manner similar to the memory reference instructions. However, because these two instructions require no actual access to memory, they are executed in a single cycle.

Memory reference instructions include arithmetic instructions, logical instructions, data handling instructions, and program control instructions. The augmented instructions are divided into two groups, the operate group and the in-out transfer group. Each group is actually a class of microinstructions produced by microprogramming the non-instruction code portion of the instruction word.

The instruction words for memory reference instructions require both an instruction code and a memory address. The instruction code (bits 0 through 3) specifies the particular instruction to be performed. The location in memory to which reference must be made is specified by the memory address portion, Y (bits 5 through 17).

Bit 4 of the instruction is the indirect address bit. This bit is normally 0. If bit 4 is a 1,

the original address Y of the instruction is not used to locate the operand, jump location, deposit location, etc. of the instruction. Instead, the address portion of the instruction is used to locate a memory register that contains a new address. The new address is used in place of the address portion of the original instruction. This indirect addressing technique frequently expedites the programming task.

Furthermore, address indexing may be combined with indirect addressing, avoiding the need for separate indexing instructions. For this purpose, memory registers 10 through 17 are available as index registers. Whenever an instruction is indirectly addressed to one of these memory index registers, the direct address is indexed before being written back into memory. The indexed direct address is then used for the required memory reference. In this way, a single indirectly addressed instruction of a program loop may refer to a successive memory location in each iteration of the loop.

An instruction which uses an indirect address is called a "deferred" instruction because the actual operation which the instruction performs is deferred until the new address is retrieved from memory. Thus in a deferred instruction, Y is not the location of the operand, but the location of the location of the operand. All memory reference instructions except law can be indirectly addressed. Load AC with n must have a 1 in bit 4 because it used the same primary four-bit code as the augmented instructions in the operate group.

Augmented instruction words use the entire word for the instruction code. Thus the entire class of augmented instructions uses only two of the available sixteen primary codes to perform a very large number of instructions. The instructions under each primary code are referred to as an instruction group. For example, in the operate instructions, the group is specified by the standard four-bit code in bits 0 to 3 plus a 0 in bit 4, while the specific instruction within the group is specified by the configuration of bits 5 to 17. The instructions in the operate group include skips, rotations of the accumulator, and various other logical operations.

The code for the in-out transfer group is bits 0 to 3 of the instruction word, while the generation of in-out pulses and the clearing of the accumulator for in-out transfers are controlled by bits 14 to 17. In the standard computer the in-out pulses are applied directly to the reader control unit. If the type 25 real time option is installed, each device is selected according to the configuration of the device code (bits 6 to 11). Bits 4, 5, 12

and 13 may be used to form subfunctions in the device code or they may be used for other control purposes.

c COMPUTER STATES - All instructions and interrupt operations are performed in multiples of the basic 8-microsecond memory cycle. The computer performs every memory cycle in one and only one of four major states. These states are fetch, execute, defer and break. The first three of these major computer states (fetch, execute, and defer) are program states, i.e., whenever the computer is in one of these states, it is performing those operations necessary for the execution of an instruction in the program. The fourth major state of the computer, the break state, is that state in which the computer performs all interrupt operations.

Whenever the computer is in one of the three program states, fetch, execute, or defer, it must also be in one of the minor computer states. This means that the computer must be performing some specific instruction. These minor states correspond to individual memory reference instructions, and to groups of augmented instructions.

During the fetch cycle of each instruction, the instruction word is retrieved from memory. Augmented instructions are completed during this single memory cycle. Note, however, that during the fetch cycle of an in-out transfer instruction, the internal processor merely generates the appropriate in-out pulses. These pulses either are applied to the device control unit or else transfer information from the control unit into the internal processor. Actual operations within the control unit and the transfer of information to the control unit may occur much later.

If an instruction is deferred (indirectly addressed) the computer goes into a defer cycle at the completion of the fetch cycle. During this defer cycle, the address portion of the instruction is used to retrieve a new address for the instruction operand.

In memory reference instructions, the fetch cycle (or the defer cycle, if the instruction is indirectly addressed) is followed by an execute cycle. During the execute cycle, the operand is retrieved from or depositied in memory, and the operations required by the instruction are completed.

An instruction may be completed in any of the three program cycles, depending upon the type of instruction. Augmented instructions are always completed in a fetch cycle. The

instruction Jump may be completed either in a fetch cycle or in a defer cycle. All memory reference instructions are completed in an execute cycle. After an instruction is completed, the program sequence may be interrupted by an external signal through the interrupt logic. When this occurs, the computer enters the break state. There are three types of break cycles; these are for a data break, a clock break, or a program break.

In a data break, the main program pauses for one memory cycle while a high-speed device, such as magnetic tape, gains direct access to memory. At the beginning of the cycle, the device control unit provides an address to MA. If information is requested by the device, the word read from memory is made available to the control unit. If information is being transferred into the computer, the strobe is disabled, and new information is transferred into the memory buffer.

In a clock break, the computer indexes the word contained in memory location 7. If this index operation increments the word to zero (in twos complement arithmetic), the clock flag is set. The program may therefore count external time signals by checking the clock flag. In a program break, a signal from an external device can break the normal program sequence and transfer control to a subroutine appropriate to the device. When a program break occurs, the address in the program counter is deposited in memory location 0, and program control is transferred to memory location 1.

d CONSOLE CONTROL - The states of all internal processor registers and control devices are shown in indicator lights on the console. The console control panel also includes the switches through which the operator exercises control over the computer. These switches allow the operator to start and stop computer operations, control the mode of operation, and specify words and addresses to be used by the computer. The initiation of any operation from the console is timed by a chain of special pulses, SP0 through SP4. After completion of this special pulse chain, the regular memory cycle timing system of the computer begins.

The computer has four modes of operation: normal, single step, single instruction, and repeat. In the normal program-running mode, one memory cycle follows another without interruption until the computer is halted by either the program or the operator. There are two manual-operate modes: single step and single instruction. These are controlled by the

single step and single instruction switches. In a manual mode, operations are begun from the console in the normal manner but the computer halts at the end of the first memory cycle (single step) or the end of the first complete instruction (single instruction). During any operation the computer must be in one, and only one, of the above three modes (normal, single step, or single instruction). Furthermore, while in any of these three modes, the computer may also be in a fourth mode -- the repeat mode. While the repeat switch is on, the operation associated with any console key that is held on is repeated at a rate determined by the setting of the speed switches.

Console control of computer operations is exercised through seven operating keys. Six of these console functions initiate computer operations; the seventh halts the computer. In all of these functions except Continue and Stop, the special pulse SP1 produces the BEGIN pulse. BEGIN clears various registers and flip-flops to prepare the computer for operation. The console functions are as follows:

Start

The computer starts normal operation in the fetch state. The first instruction is taken from the memory location addressed by the address switches. Start also initiates the first cycle of operation in the manual modes.

Continue

The computer resumes normal operation at the state indicated by the console lights. In the manual modes, continue also initiates each cycle or instruction after the first.

Examine

The contents of the memory register addressed by the address switches are displayed in the accumulator and memory buffer lights on the console. The address contained in the address switches is transferred to the program counter and incremented by 1.

Examine Next

The contents of the memory register addressed by the program counter are displayed in the accumulator and memory buffer lights on the console. The contents of the program counter are incremented by 1.

Deposit

The word contained in the accumulator switches is deposited in the memory location addressed by the address switches. The address contained in the address switches is transferred to the program counter and incremented by 1.

Deposit Next

The word contained in the accumulator switches is deposited in the memory location addressed by the program counter. The contents of the program counter are incremented by 1.

Stop

The computer halts at the end of the current memory cycle.

e INSTRUCTION LIST - This list includes the title of the instruction, the normal execution time (i.e., without indirect addressing), the mnemonic code, the octal representation of the instruction code, and a short description of the instruction. In the following list, the contents of a register are indicated by C( ). Thus C(Y) means the contents of memory location Y; C(AC) means the contents of the accumulator. A specific bit of a register is indicated by a subscript number following the symbol for the register. Thus MB_{17} represents bit 17 of the memory buffer.

For memory reference instructions the octal instruction codes are given as two digits. The more significant digit represents the first three bits of the four-bit instruction code. The second octal digit (with one exception) is either 0 or 4, depending upon whether the fourth bit of the instruction code is 0 or 1. Thus the two-digit octal code is equal to the first two digits of the octal instruction word, assuming that bits 4 and 5 of the word are both 0. In memory reference instructions, bit 4 is the indirect address bit, and bit 5 is the most significant bit of the 13-bit address. Therefore, the second digit of a six-digit instruction word whose instruction code ends in 0 may be 0, 1, 2 or 3 while the second digit of an instruction word whose code ends in 4 may be 4, 5, 6 or 7, depending upon the configuration of bits 4 and 5.

The one exception to this convention is the nondeferable instruction law. This instruction requires a 1 in bit 4 because both law and the operate of augmented instructions use the

the same primary four-bit instruction code. Thus, law has a five-bit code represented by octal 76 (111 11) while the primary portion of the augmented codes for the operate group is represented by octal 74 (111 10). The in-out transfer group is represented by octal 70 (111 0) but the second digit in the instruction word varies according to the configuration of bits 4 and 5, which are part of the augmented code. For all augmented instructions (comprising the two groups, opr and iot) the entire six-digit octal code is given.

Memory Reference Instructions:

Call Subroutine (16 μsec) ..... cal Instruction Code 00

This instruction is equivalent to the instruction jms 20. The address portion, Y, is ignored. Call Subroutine may be used as part of a master routine to call subroutines. The address 20 may be interpreted as an indirect address -- that is, cal indirect is equivalent to jms 20 indirect.

Deposit Accumulator (16 μsec)..... dac Y Instruction Code 04

The C(AC) replace C(Y) in memory. The C(AC) are unchanged, the original C(Y) are lost.

Jump to Subroutine (16 μsec) ..... jms Y Insturction Code 10

The C(PC) replace C(Y) in memory. When the transfer takes place, the program counter holds the address of the instruction following the jms in normal sequence. The program then executes the instruction in memory location Y + 1. The original C(Y) are lost.

Deposit Zero in Memory (16 μsec)..... dzm Y Instruction Code 14

The contents of memory location Y are replaced by zero (i.e., memory location Y is cleared). The original C(Y) are lost.

Load Accumulator (16 μsec) ..... lac Y Instruction Code 20

The C(Y) are placed in the accumulator. The C(Y) are unchanged; the original C(AC) are lost.

Exclusive OR (16 μsec)..... xor Y Instruction Code 24

The bits of C(Y) operate on the corresponding bits of C(AC) to form the exclusive OR. The result is left in the accumulator. The C(Y) are unaffected.

Ones Complement Add (16 μsec)..... add Y Instruction Code 30

The final C(AC) are the sum of the C(Y) and the original C(AC); C(Y) are unchanged. The addition is performed in 1s complement arithmetic. If the sum exceeds the capacity of the accumulator, the link is set.

In 1s complement arithmetic, a negative number is represented by the complement of the corresponding positive number. Thus a positive number is changed to a negative number by changing the sign bit to 1, and changing all the 0s to 1s and all the 1s to 0s in the magnitude portion of the number. Since the complement of a single bit is equivalent to subtracting the bit from 1, complementing the binary integer n is equivalent to subtracting n from $2^n - 1$. Thus the number -n is represented in 1s complement arithmetic as $-(2^n - n - 1)$. This convention results in two representations for the number zero: all 0s (+0), or all 1s (-0). Minus zero results from adding -0 to -0, or adding -n to +n.

Twos Complement Add (16 μsec)..... tad Y Instruction Code 34

The final C(AC) are the sum of the C(Y) and the original C(AC); C(Y) are unchanged. The addition is performed in 2s complement arithmetic. If there is a carry out of bit 0 of the accumulator, the link is set. This feature is useful in multiple precision arithmetic.

In 2s complement arithmetic, a negative number is represented by adding 1 to the complement of the corresponding positive number. Thus the number -n is represented in 2s complement arithmetic as $-(2^n - n)$.

Execute (8 μsec plus time of instruction executed)..... xct Y Instruction Code 40

The instruction in memory location Y is executed. The program counter remains unchanged (unless a jump or skip were executed). Execute acts exactly as though the instruction being executed replaced the Execute instruction in the program. Execute may be indirectly addressed, and the instruction being executed may also use indirect addressing. An xct instruction may execute other xct commands.

Index and Skip if Zero (16 μsec)..... isz Y Instruction Code 44

The C(Y) are replaced by the C(Y) + 1. The C(AC) are unaffected by this instruction. The addition is performed in 2s complement arithmetic. If the sum is zero, the program

counter is advanced one extra position and the next instruction in sequence is skipped.

Logical AND (16 μsec)..... and Y Instruction Code 50

The bits of C(Y) operate on the corresponding bits of C(AC) to form the logical AND. The result is left in the accumulator. The C(Y) are unaffected.

Skip if Accumulator and Y Differ (16 μsec).sad Y Instruction Code 54

The C(Y) are compared with the C(AC). If the two numbers are different, the program counter is indexed one extra position and the next instruction in sequence is skipped. The C(AC) and the C(Y) are unchanged.

Jump (8 μsec)..... jmp Y Instruction Code 60

The address Y replaces C(PC). The next instruction in the program is then taken from memory location Y. The original C(PC) are lost.

Load Accumulator with n (8 μsec)..... law n Instruction Code 76

The instruction word replaces C(AC). The original C(AC) are lost. Since the instruction code is all 1s, the binary word in AC is interpreted as a negative number ($AC_0 = 1$), and consequently the magnitude of the address portion is equivalent to the magnitude of the entire word. As a result, the programmer may load a negative number -n (where $n \quad 2^{13}$) into the accumulator by placing the negative representation of n in the address portion of a law instruction.

Augmented Instructions:

Operate Group (8 μsec)..... opr Instruction Code 74

The instructions in this group perform miscellaneous logical operations primarily up on the registers in the arithmetic unit. The group also includes the conditional skip instructions. All instructions in the group require 8 microseconds.

In these instructions the instruction code is 18 bits. The primary code (bits 0 to 4) specifies the operate group while the address portion specifies the operation to be performed or the skip condition to be sensed. The various operations can be microprogrammed -- that is, the addresses of the different instructions may be combined to form the union of the functions. For example, instruction 740403 causes the computer to skip the next instruc-

tion, if the link is 1 at the beginning of the operate, and complements both the accumulator and the link.

Included in the operate group are the rotate and skip instructions. Rotate is a cyclic shift. A shift is an information transfer from bit to bit in a single register. Transfer of $C(AC_n)$ into AC_{n-1} is a left shift: $C(AC_n)$ into AC_{n+1} is a right shift. In a cyclic shift the two ends of the accumulator are logically joined together through the link and information is rotated through the 19-bit combination as though it were a ring.

The skip instructions sense various elements in the arithmetic unit and cause the computer to skip the next instruction in sequence if the addressed condition is satisfied. The intent of any skip instruction is determined by the programming of bit 8 of the instruction word. For example, the instruction 740200 is Skip on Zero Accumulator, while 741200 is Skip on Nonzero Accumulator.

The logical operations specified by the operate instructions are performed by one or the other of two operate pulses, OP1 and OP2. These pulses occur at different times during the memory cycle. Not only can the programmer combine several operate instructions to perform operations on different elements but, because of the time interval between the two pulses, the programmer can also combine operate instructions in such a way as to perform two operations on the same element at different times. In the following list, the time of occurrence is given for the arithmetic unit operations. The skip instructions cause a skip by incrementing the program counter at OP1 if, at that time, the skip condition is satisfied. The instruction Halt clears flip-flop RUN at OP1, but before stopping, the computer completes the cycle.

No Operation..... nop Instruction Code 740000

The state of the computer is unaffected by this operation and the program counter continues in sequence.

Clear Accumulator..... cla Instruction Code 750000

Clears AC at OP1.

Clear Link..... cll Instruction Code 744000

Clears L at OP1.

Complement Accumulator..... cma Instruction Code 740001

The $\overline{C(AC)}$ replace C(AC) at OP2.

Complement Link..... cml Instruction Code 740002

The $\overline{C(L)}$ replace C(L) at OP2.

Rotate Accumulator and Link Left..... ral Instruction Code 740010

Rotates the contents of AC and L left one place at OP2.

$AC_n = AC_{n-1}$, $AC_0 = L$, $L = AC_{17}$.

Rotate Accumulator and Link Right..... rar Instruction Code 740020

Rotates the contents of AC and L right one place at OP2.

$AC_n = AC_{n+1}$, $AC_{17} = L$, $L = AC_0$.

Rotate Twice Left..... rtl Instruction Code 742010

Rotates the contents of AC and L left two places. $AC_n = AC_{n-2}$, $AC_1 = L$, $AC_0 = AC_{17}$, $L = AC_{16}$.

Rotate Twice Right..... rtr Instruction Code 742020

Rotates the contents of AC and L right two places. $AC_n = AC_{n+2}$, $AC_{16} = L$, $AC_{17} = AC_0$, $L = AC_1$.

Inclusive OR AC Switches with AC..... oas Instruction Code 740004

The inclusive OR function of C(ACS) with C(AC) replace C(AC) at OP2. If AC is cleared at OP1 by combining cla with oas (750004), at the end of the instruction C(AC) = C(ACS).

Halt..... hlt Instruction Code 740040

Stops the computer.

Skip on Plus Accumulator..... spa Instruction Code 741100

Skip if AC_0 is 0.

Skip on Minus Accumulator..... sma Instruction Code 740100

Skip if AC_0 is 1.

Skip on Zero Accumulator..... sza Instruction Code 740200

Skip if all accumulator bits are 0.

Skip on Nonzero Accumulator..... sna Instruction Code 741200

Skip if any accumulator bit is 1.

Skip on Zero Link..... szl Instruction Code 741400

Skip if L is 0.

Skip on Nonzero Link..... snl Instruction Code 740400

Skip if L is 1.

Skip..... skp Instruction Code 741000

Skip the next instruction unconditionally.

In-out Transfer Group (8 μsec)..... iot Instruction Code 70

All in-out transfer instructions use instruction code 70 (111 0) in bits 0 to 3 of the instruction word. The programmer specifies the in-out device and the specific operations to be performed by microprogramming the rest of the instruction word. In-out transfers are governed by a set of three in-out pulses, PIO1, PIO2 and PIO4. The programmer controls the generation of these pulses during the execution of an iot by programming 1, 2 or 4 respectively, as the final octal digit in the instruction word.

The first PIO pulse is generated after the iot instruction is retrieved from memory in a fetch cycle. The second pulse is generated 2.0 microseconds later. The third pulse then follows at the beginning of the next cycle 1.3 microseconds later. Since the pulses occur at different times, a single instruction may use more than one pulse; but only those pulses specified by the instruction are actually generated.

In addition to microprogramming specific operations within the iot instruction, the programmer must also specify the device by placing a device code in bits 6 to 11 of the in-

struction word. In the standard computer, the PIO pulses are applied directly to the reader control unit and no device code is necessary. If the computer includes the type 25 real time option, the device selector decodes the device code and switches the PIO pulses onto the lines appropriate to the specified device. The pulses for each device are named according to the configuration of the instruction code producing them. For example, the three PIO pulses for the reader (device code 01) are IOT0101, IOT0102 and IOT0104 respectively.

Completion of most in-out operations requires a definite minimum time. This minimum time is usually very long compared to the computer memory cycle. The iot instructions serve merely to initiate operations in the device control units -- the control unit then carries out operations automatically while the computer may continue executing other instructions. When the entire operation is completed, the program must resynchronize the device and the computer either by utilizing the interrupt logic or by sensing the device flag.

In all iot's, PIO1 is used to sense a device flag, while PIO2 usually clears the flag. For input devices, PIO4 initiates operations in the device control unit. After the operation is completed, the programmer may clear the accumulator by programming a 1 in bit 14 of an iot instruction word, and can then transfer information from the device buffer to the accumulator with PIO2. For output devices, PIO2 clears the device flag and the device buffer. A PIO4 pulse in the same instruction may then transfer information to the device buffer and begin operation of the control unit.

In addition to the device code in bits 6 to 11, and the standard coding of bits 14 to 17 of the instruction word, the programmer may use bits 4, 5, 12 and 13 to produce subfunctions in the device code or for other control purposes. For example, in reader instructions the state of bit 12 specifies whether the tape is to be read in alphanumeric mode or in binary mode. The following list includes only the standard instructions for governing the real time control, the reader, the punch, and the keyboard/printer. The programmer may, of course, generate other instructions for these devices by varying the configuration of bits 14 to 17. Each iot requires only either microseconds of internal processor time; however, the time given with each instruction is the time required for the device to complete the entire operation.

Interrupt Off (8 μsec)..... iof Instruction Code 700002

Clear program enable flip-flop, preventing program breaks from interrupting the normal program sequence.

Interrupt On (8 μsec)..... ion Instruction Code 700042

Set program enable flip-flop, allowing the normal program sequence to be interrupted by program breaks through the interrupt logic.

In-out Read Status (8 μsec)..... iors Instruction Code 700314

This instruction sets specific bits of the accumulator according to the status of the various in-out devices. The meaning of the information transferred into AC is as follows:

AC Bit	If Set
0	Program interruptions are being allowed.
1	Tape reader buffer has been loaded but not yet read by an rrb.
2	Tape punch ready for output.
3	Keyboard key struck and not yet read by a krb.
4	Teleprinter ready for output.
5	Displayed point sensed by light pen.
6	Clock count is complete.
7	Clock interruptions are being allowed.

The rest of the AC bits are used for the status of other optional equipment.

Clock Skip on Flag (8 μsec)..... csf Instruction Code 700001

Skip of clock flag is on, indicating that a clock count has been completed.

Clock Off (8 μsec)..... cof Instruction Code 700004

Clear clock enable flip-flop, preventing further clock interruptions of the normal sequence, and clear clock flag.

Clock On (8 μsec)..... con Instruction Code 700044

Set clock enable flip-flop, allowing clock to interrupt the normal program sequence, and clear clock flag.

Reader Skip on Flag (8 μsec)..... rsf Instruction Code 700101

Skip if reader flag is on, indicating that reader buffer contains information not yet read by an rrb.

Reader Start in Alphanumeric (3.3 ms).... rsa Instruction Code 700104

Clear reader buffer and reader flag. Start reader operation in alphanumeric mode. All eight holes of a single line on the tape are read into the reader buffer. When reading is completed, reader flag goes on.

Reader Start in Binary (10 ms)..... rsb Instruction Code 700144

Clear reader buffer and reader flag. Start reader operation in binary mode. Holes 1 to 6 in each of three lines on the tape are read and assembled into a full computer word in the reader buffer. A line is recognized in binary mode only if hole 8 is punched, i.e., lines with no eighth hole are skipped. Hole 7 is ignored. The reader flag goes on when a full word has been assembled.

Reader Read Buffer (8 μsec)..... rrb Instruction Code 700112

Transfer contents of reader buffer into accumulator and clear reader flag.

Punch Skip on Flag (8 μsec)..... psf Instruction Code 700201

Skip if punch flag is on, indicating that the punch is ready for output.

Punch Load and Start (5.0 to 15.8 ms).... pls Instruction Code 700206

Clear punch flag and load punch buffer from AC_{10-17}. Punch one line of tape. If AC_{17} is 1, hole 1 is punched; if AC_{16} is 1, hole 2 is punched; and so on to AC_{10} which controls the punching of hole 8. When punching is completed, punch flag goes on. Time required to punch is 5 milliseconds; time between lines is 15.8 milliseconds. If a punch instruction follows immediately after punching is completed, 15.8 milliseconds are available for the program.

Punch Clear Flag (8 μsec)..... pcf Instruction Code 700202

Clear punch flag.

Keyboard Skip on Flag (8 μsec)..... ksf Instruction Code 700301

Skip if keyboard flag is on, indicating that keyboard buffer contains a character not yet read by a krb.

Keyboard Read Buffer (8 μsec)..... krb Instruction Code 700312

Clear keyboard flag and transfer a character from keyboard buffer to AC_{13-17}.

Teleprinter Skip on Flag (8 μsec)..... tsf Instruction Code 700401

Skip if teleprinter flag is on, indicating that the teleprinter is ready for output.

Teleprinter Load and Start (100 ms)..... tls Instruction Code 700406

Clear teleprinter flag and print character specified by AC_{13-17}.

Teleprinter Clear Flag (8 μsec)..... tcf Instruction Code 700402

Clear teleprinter flag.

4-3 CONTROL

This paragraph describes those elements of the control unit which are not discussed under arithmetic or memory. These control elements include the timing system, state control, program control, and the transfer logic. The symbols used in the drawings to represent the logic elements are also described.

a TIMING SYSTEM - The fundamental timing system of the computer is based upon a sequence of seven time pulses, T1 to T7. These time pulses occur at irregular intervals chosen so as to optimize memory operations. There is no repetitive standard clock pulse providing a fundamental time unit for the computer. The seven time pulses follow each other in a chain covering one memory cycle of eight microseconds. Each time pulse is triggered through a delay from the previous time pulse. The transition from one cycle to the next is controlled by flip-flop RUN. If RUN is 1 the final time pulse in one cycle triggers the first time pulse for the beginning of the next cycle. When RUN is cleared, the computer

halts at the end of the current memory cycle because the final pulse in the cycle cannot trigger the first pulse of the following cycle.

The organization of a single memory cycle is shown in Figure 4-2. The seven irregularly spaced time pulses are shown from left to right across the 7.9-microsecond cycle. During each such cycle a single memory access is executed. The specific actions performed at each time pulse depend upon the particular operation in which the memory cycle occurs.

The functions that control the actual memory access during each cycle are also shown in the figure. Each memory module contains four flip-flops which control a set of four functions. Three of these, the read, inhibit and write functions, are levels that control core driving. These functions are shown by the horizontal lines in the figure. The fourth function, the strobe, is a pulse that samples the output at the core memory sense amplifiers 0.7 microsecond after the initiation of the read function.

b STATE CONTROL - Major states of the computer are controlled by a quadristable device; minor states are controlled by the instruction register. The major states device, MS, has four outputs -- F, D, E and B; these outputs represent fetch, defer, execute and break. At the end of each cycle, one of the four inputs to MS is pulsed. This asserts the corresponding output (and negates the other three outputs) so that the computer performs the next cycle in the appropriate major state.

When the computer is in one of the program states, fetch, defer or execute, it must also be in one of the minor states -- that is, the computer must be performing a specific instruction. During each fetch cycle, the memory strobe transfers an instruction word from memory into the memory buffer. The instruction code (bits 0 to 3) is then transferred to the instruction register IR. Although for programming purposes the instruction codes are given as two-digit octal numbers, for control purposes the contents of IR are decoded by a binary-to-quaternary decoder. In the two-digit octal code, the more significant digit represents the binary number contained in IR_{0-2}. The second octal digit is 0 or 4, depending upon whether bit 3 of the instruction word (IR_3) is 0 or 1.

For the instruction register, however, the four bits are decoded into a pair of levels giving a quaternary representation of the instruction code. The contents of bits 0 and 1 are decoded into one of the IA levels, IA0 to IA3. The contents of bits 2 and 3 are decoded into one of the IB levels, IB0 to IB3. The execution of each specific instruction is con-

trolled by the pair of asserted levels from the instruction decoder. Furthermore, operations common to entire groups of instructions may be controlled by a single IA or IB level. For example, all instructions whose binary codes begin with 00 deposit information in memory; thus, IA0 disables the memory strobe.

If the computer is performing an augmented instruction, the appropriate pulses are produced during the remainder of the fetch cycle. The operate pulses are generated at T5 and T7; the programmed in-out pulses are generated at T5, T7 and T1.

Any one-cycle instruction that is not deferred is completed during the fetch cycle. The computer then remains in the fetch state to retrieve another instruction word from memory. If the instruction is deferable, a 1 in MB_4 causes T7 to put the major states device into the defer state. The computer then retrieves a new operand address from memory. In a two-cycle instruction, the fetch state or defer state is followed by the execute state, during which the required operand reference is made to memory. At the completion of an instruction (which may occur in the fetch, defer or execute state), if a break is requested the computer enters the break state. In this state the required type of cycle is performed, depending upon whether the break is a data break, a clock break or a program break. At the completion of all requested breaks, the computer returns to the fetch state.

c PROGRAM CONTROL - At the beginning of each fetch cycle the contents of the program counter are transferred into the memory address register. The current instruction in the program is then retrieved from the memory location addressed by the contents of MA. After the address transfer, the contents of the program counter are incremented by 1. This causes the next instruction to be taken from the succeeding memory location during the following fetch cycle.

During a skip instruction, if the skip condition is satisfied, the program counter is advanced one extra position. This causes the program to skip the next instruction in normal sequence. The opr skip instructions can sense the states of arithmetic unit elements; the iot skip instructions can sense flags associated with the in-out devices.

Program control is transferred to a new location by loading a new address into the program counter. The counter is loaded from the memory buffer on jmp; it is loaded from the address switches for console operations; and it is loaded from the memory address register for

subroutine-calling transfers.

d LOGIC SYMBOLS - The symbols used on the logic drawings are shown in Figure 4-3. Note that in the rectangle which represents a flip-flop, the 0-out terminal E and the 1-out terminal F are shown twice. Over the "0" the two terminals are shown with the polarities they have when the flip-flop is in the 0 state; over the "1" the two terminals are shown with the polarities they have when the flip-flop is in the 1 state. Therefore, the "0" and "1" in the rectangle represent both the output terminals and the contents of the flip-flop. In the normal convention the "0" is at the left of the rectangle and the 0-out terminal is represented by the left diamond in both pairs.

The two gatable inputs are shown at the bottom of the rectangle with the 0-in terminal at the left. Ungatable direct pulse inputs are always shown at the sides of a flip-flop. In the example in the figure a direct clear input is shown at the left.

Some flip-flops also have complement inputs. Such inputs are shown at the bottom center of the rectangle. A carry out of a flip-flop is shown at the left side. A direct carry into a flip-flop is shown at the right, while a gated carry in is shown in the usual complement position.

Instead of representing a binary digit, a flip-flop sometimes represents a pair of mutually exclusive logic functions. In such a case the outputs are often labeled with the names of the functions rather than with usual "0" and "1". For example, the states of the read mode the flip-flop in reader control are read binary (RD BIN) and read alphanumeric (RD ALPHA).

The principal advantage of having four logical outputs to represent two output terminals at two assertion levels is that there is never any need to invert a signal name which appears as an input to a logic net. Even though the computer uses inverter logic, all logical conditions appear in the drawings with correct truth values. When a flip-flop output is used as the input to a logic net, the signal name indicates the correct state of the flip-flop that enables the net.

To determine the physical source of the signal (i.e., the output terminal to which the signal line is connected) one must consider both the signal name and the assertion level. For example, the signal A^1 at the negative assertion level actually originates at the 1-out terminal of flip-flop A; the signal A^1 at the ground assertion level actually originates at

the 0-out terminal of flip-flop A. The signal designation A^1 can thus refer to the output signal generated at either terminal of flip-flop A, when that flip-flop is in the 1 state.

e TRANSFER LOGIC - All information transfers must take place between two information-storing devices. In most cases the transfer is made from one flip-flop register to another. A bit of information contained in a specific flip-flop of the source register is transferred to a corresponding flip-flop in the receiving register.

In memory access, information is transferred between the memory buffer flip-flops and the ferrite cores within the memory core-bank registers. In rotate operations information is transferred from one flip-flop to another in the same register.

The operation of a 1 transfer is shown in Figure 4-4A. In the example shown, the 1s in register K are transferred to the corresponding flip-flops in register M. An initial pulse, M CLEAR, clears every flip-flop in M and then the transfer pulse, K1→M, sets each bit M_n in the corresponding bit K_n is 1. After both pulses have occurred C(M) = C(K). Note that if a 1 transfer is executed without a prior clear the final contents of M equal the OR function of the previous contents of M and the contents of K. That is, after the pulse K1→M, a bit M_n is 1 if M_n was already 1 or if K_n is 1.
A 0 transfer is shown in Figure 4-4B. The pulse K0 → M clears M_n if K_n is 0. This type of transfer produces the AND function of C(K) and the original C(M) because a bit M_n is 1 after the transfer only if M_n was originally 1 and K_n is 1.

If a 0 transfer and a 1 transfer are executed simultaneously, the result is a jam transfer. No clear pulse is required in this case because M_n is set if K_n is 1, and M_n is cleared if K is 0. The jam transfer is used in PDP-4 to shift information from one bit to another of the same register; for example, in the rotation of the accumulator. In a left rotation, information is transferred from M_n to M_{n-1}; in a right rotation, information is transferred from M_n to M_{n+1}.

A typical example of the 1 input gating to a flip-flop in a register is shown in Figure 4-4C. Information may be transferred into the receiving register from any of several source registers whenever the appropriate transfer pulse is applied to the corresponding capacitor-diode gate. If the output of the source is already in pulse form (e.g., the output of the sense amplifiers in memory), information may be transferred into the receiving register without a

gating level. The transfer is effected by the line labeled "direct" in the figure. A separate pulse is required for each flip-flop in the receiving register unless the pulse is clearing or complementing the entire register. A direct input pulse may be shown in the logic drawings as it is in Figure 4-4C, or alternatively, it may be shown at either side above the capacitor-diode gates.

In the logic drawings, the name of each transfer pulse is preceded by a symbol that indicates the drawing on which the signal is generated. For example, the pulse that transfers information from MB to PC is generated on the PC drawing, so the pulse is labeled PCMB1 PC.

4-4 ARITHMETIC UNIT

The arithmetic unit includes two full-word, 18-bit registers, a 1-bit link register, and associated control circuits. The two full-word registers are the accumulator and the memory buffer. The memory buffer is a passive register in arithmetic unit operations -- that is, MB holds the operand in all two-term arithmetic and logical operations. The memory buffer is active only in indexing operations which are performed independently of the accumulator.

The accumulator is active in all arithmetic unit operations. In either 1s complement or 2s complement addition, the contents of MB and AC are added together; the result appears in AC.

a ACCUMULATOR - The accumulator is the major register in the arithmetic unit. Transfers to AC may be made from the memory buffer, the reader buffer, and the console accumulator switches. If the computer includes the real time control, the reader buffer connections are replaced by connections from the information collector. In this case, information from the reader buffer and all other input devices is transferred into the accumulator through the information collector. All transfers into the accumulator are 1 transfers requiring a prior clear.

The accumulator and the link may be rotated either right or left. In rotate operations, AC and L together form a 19-bit circular register with AC_0 linked to AC_{17} through L. The link may therefore be considered to be to the left of AC_0 and to the right of AC_{17}.

The arithmetic unit can perform three logic functions. These are: logical negation, AND (conjunction), and exclusive OR. The program may produce the inclusive OR between the

contents of MB and AC by using the negation and conjunction. In all cases, the result appears in AC. The exclusive OR function and the AND function can be performed only with the contents of MB; the inclusive OR function may be produced from any source register except MB, by programming a 1 transfer from the register into AC without first clearing AC.

The addition operation in 1s complement or 2s complement arithmetic is carried out in two stages. First, a partial sum is produced by the logical exclusive OR between MB and AC; second, a carry function changes the exclusive OR result into the true arithmetic sum. The number in AC at the end of the operation is the sum of the previous contents of AC plus the contents of MB. In 1s complement arithmetic, the negative of a number is formed by complementing it. In 2s complement arithmetic, the negative of a number is formed by complementing the number and then adding 1.

b LINK - The link, L, is a one-bit register that extends the capabilities of the accumulator. It may be cleared or complemented, or rotated as part of the accumulator. It is used as an overflow flip-flop for 1s complement arithmetic, and as a carry link for 2s complement arithmetic. The state of the link can be sensed by skip instructions so that the programming of multiple precision arithmetic is somewhat simplified. Since L can be sensed it is available as a general program flag. Products and quotients may be constructed, one bit at a time, by utilizing the link in appropriate subroutines.

c ARITHMETIC UNIT CONTROL - The control circuits for the arithmetic unit include the operate logic, the overflow logic, and the transfer and arithmetic pulse logic for the accumulator and the link. The operate logic includes the operate skip logic, the generation of the pulses that clear or complement AC or L, and the generation of the pulses that rotate AC and L to the left or right. Use of L as an overflow flip-flop is controlled by the overflow logic. The transfer logic controls the transfer of information into AC; the arithmetic logic generates the pulses that perform addition.

4-5 MEMORY

During every eight-microsecond memory cycle, the memory address register addresses a single core register in the computer memory. The memory cycle is divided into two portions, a read portion and a write portion. During the read portion of the cycle, a single 18-bit computer word is read from the addressed core register into the memory buffer. During the write portion

of the cycle, the word contained in the memory buffer is written back into the addressed core register. For both the read and write portions of the memory cycle, the addressed core register is specified by the contents of the memory address register.

a MEMORY ADDRESS REGISTER - a 10-, 12- or 13-bit address is transferred into MA at the beginning of every memory cycle. This address controls memory access throughout the entire cycle. All operations occurring in the memory during the cycle affect only the single core register addressed by the contents of MA. At the end of each memory cycle, MA is cleared in preparation for use during the next cycle.

Included with the memory address register in the internal processor are four binary-to-octal decoders. For 12- or 13-bit address decoding, each of these four memory address decoders decodes a three-bit section of MA. For a 13-bit address, the extra bit (MA_5) selects the memory module while the outputs of the decoders are applied to both memory modules. In 10-bit address decoding, each pair of decoders decodes five bits. In each pair, one decoder decodes the less significant three bits binary-to-octal; the other decodes the more significant two bits binary-to-quaternary. For all addressing the decoder outputs are applied to memory instead of the binary information in MA.

b MEMORY BUFFER - At the beginning of every memory cycle the memory buffer is cleared. During the read portion of the cycle a word is read out of the memory and transferred into MB by the strobe. If new information is to be deposited in memory during the cycle then the strobe is disabled so the read merely clears the addressed core register. New information can then be transferred into MB. During the write portion of the cycle the contents of MB (whether new or old) are written into the addressed memory location. In indexing operations the word read from memory is indexed in MB before being written back into the core register from whence it came.

At the same time that a word is being written into memory the word is also available to the rest of the computer from MB. During logical or arithmetic instructions, the operand in MB is used by the accumulator input gating. During an iot instruction bits 14 through 17 control the in-out operations from MB and bits 6 through 11 are decoded by the device selector.

If MB contains an operate instruction word, bits 5 through 17 control the execution of the instruction directly from MB. However, if MB contains a memory reference instruction

word, the address portion of that word is transferred to MA at the beginning of the next memory cycle.

c MEMORY MODULE - The memory module contains a 4096 word core bank or a 1024 word core bank. It also includes associated logic circuits for addressing memory locations, for reading information out of memory and for writing information into memory. In the 4096 word core bank the core registers are arranged in a 64-by-64 matrix; in the 1024 word core bank the registers are arranged in a 32-by-32 matrix.

The outputs of the memory address decoders are applied to the memory module. At the module, these outputs select a single core register for use during the current memory cycle.

The memory control pulses from the control unit are applied to a four-bit shift register in the memory module. The memory timing functions (see Figure 4-2) are generated from the outputs of this shift register. The read function makes information from the addressed core register available to the 18 sense amplifiers. This information is sampled by the strobe, which transfers it to the memory buffer.

Prior to the write function, the inhibit function applies inhibit current to all bits of the core register that correspond to 0s in MB. The write function then writes a 1 into each of the remaining (uninhibited) core bits.. Information is thus written into the addressed core register by a 1 transfer. The write function writes 1s into all bits of the core register except those bits which are kept in the 0 state by an inhibit current.

4-6 INPUT-OUTPUT SYSTEM

The input-output system in the standard computer includes one input device only -- a paper tape reader. Other in-out devices may readily be added to the system by installing the type 25 real time control.

a REAL TIME OPTION TYPE 25 - The real time option includes five sections. These are: device selector, information distributor, information collector, interrupt logic, and in-out skip facility. All in-out operations in PDP-4 are initiated by the programmed in-out pulses PIO1, PIO2, and PIO4. These three pulses are applied to the device selector. A specific set of three pulse lines is selected according to the device code of the in-out instruction word. The three in-out pulses become iot pulses on the selected output pulse lines. The

device selector thus behaves as a 3-pole selector switch whose position is determined by bits 6 through 11 of the in-out instruction.

Each set of three iot pulse lines controls a particular in-out device. For control purposes, the interrupt logic is treated as a device. In some cases a complex device such as magnetic tape requires a larger number of control pulses. Such a device is therefore treated as several devices having several device codes.

The information distributor includes a set of bus drivers through which the 18 bits of the accumulator are made available to taper pin panels for connection to in-out devices. The information collector is essentially an 18-channel pulse amplifier. Information from any device buffer is transferred through the collector to the accumulator whenever the appropriate iot pulse is applied to the IC input gating.

The interrupt logic allows the computer to perform breaks in the normal sequence of program instructions to accommodate the needs of high-speed in-out devices, real time synchronization, and so forth. Three types of break are available -- data break, clock break, and program break. The computer does not perform breaks routinely; the break must be requested by specific external conditions. Data breaks may be requested only by high-speed in-out devices such as magnetic tape equipment. The real time clock break is requested at the 60-cycle power line frequency (every 16.6 milliseconds). A program break may be requested by any in-out device; however, high-speed in-out devices use the program break only for control purposes.

Whenever any kind of break is requested, the computer goes into the break state after completing the current instruction. Then all break requests are granted before the computer returns to the fetch state to begin the next instruction. If several breaks are requested simultaneously, the data request has first priority, followed by the clock request and, finally, by any program requests.

For a high-speed data transfer, the device must request a data break and provide a memory address. For data output, the computer retrieves the addressed word from memory and makes it available to the device. For data input, the computer clears the addressed location and transfers the word provided by the device into the memory buffer.

The programmer can turn the real time clock on and off by adjusting the state of the clock

enable flip-flop. As long as the clock is enabled, a clock request is made automatically every 1/60 second. Each time the request is granted, the computer indexes the number contained in memory location 7. If the number becomes 0 as a result of the indexing operation, the clock flag is set. The flag then requests a program break to indicate that the clock count is complete.

The programmer may also turn the program interrupt system on and off by adjusting the state of the program enable flip-flop. A program interruption may be requested by any in-out device. The inputs to the program interrupt system are the flags of the in-out devices (11 input lines are available in the standard type 25). When a program request is granted, the computer deposits C(L) and C(PC) in memory location 0 and then executes the instruction contained in location 1. When entering a program break, the computer automatically disables the program interrupt system. Nested program breaks can occur only if the program enables the interrupt system within the routine that begins in location 1. Note that the programmer should clear all device flags before initially enabling the program interrupt system; otherwise, a device flag that is still 1 after some previous in-out operation immediately makes a spurious program request.

The type 25 real time option also provides an in-out skip facility. The flags of all in-out devices (up to a maximum of 16) may be sensed by in-out skip instructions. If the addressed flag is on, the program counter is forthwith directly incremented by 1.

b READER CONTROL - The control unit for the tape reader includes an 18-bit buffer register RB. This buffer is loaded as information is read from the tape. When the type 25 real time option is used, transfers to the accumulator from the buffer are made through the information collector. When the reader is used alone, the buffer is connected directly to the accumulator input gates. The reader may operate in two modes: alphanumeric and binary. If the reader is operating in alphanumeric mode, a single line of eight holes on the tape is read. The eight data bits from this line are loaded into RB_{10-17}.

If the reader is operating in binary mode, only holes 1 through 6 are read, but the reader reads three lines from the tape. The six data bits from the first line are loaded into RB_{12-17}. As each of the two subsequent lines is read, the data in RB is shifted left six places and the six data bits from the new line are also read into RB_{12-17}. In binary mode,

a line of tape is read only if hole 8 is punched. If hole 8 is not punched, the reader skips the line. Therefore, to construct a full word in binary, the reader reads the first three lines in which hole 8 is punched.

Each line is moved past the reader photodiodes by engaging the reader clutch. When a signal is picked up from the feed hole, the output of the photodiodes is strobed and data is read into the reader buffer. In alphanumeric mode the reader flag goes on after a single character (line) is read. However, in binary mode a two-bit counter counts the characters read from the tape and the reader flag goes on only after three characters have been read.

Two in-out pulses, iot2 and iot4, control the reader logic. Pulse iot2 clears the reader flag and causes a 1 transfer from RB into AC. Pulse iot4 starts the reader; clears the flag, the buffer, and the line counter; and adjusts the state of the read mode flip-flop according to the state of bit 12 of the iot. The reader logic then loads the buffer from information on the tape, in binary or alphanumeric mode depending upon the state of the read mode flip-flop.

When RB is loaded, the reader flag goes on and the program may transfer C(RB) into AC with an iot2 pulse. The accumulator may be cleared before the transfer by programming a 1 in bit 14 of the iot.

c PUNCH CONTROL TYPE 75 - The punch control unit contains an eight-bit buffer PB. The punch logic is controlled by two in-out pulses, iot2 and iot4. The first of these pulses clears the punch buffer and turns off the punch flag. The second (iot4) transfers the eight least significant bits of the accumulator into the buffer, and starts the punch. Both in-out pulses are generated by the single instruction, pls.

After receiving pulse iot4, the punch control unit waits for a synchronizing signal from the punch motor. During the 5-millisecond interval after receiving this synchronizing signal, the control unit punches one line on the tape. It does this by energizing appropriate solenoids corresponding to the contents of the punch buffer. At the same time, the control unit advances the tape to the next position. When punching is completed, the punch flag goes on.

d KEYBOARD/PRINTER CONTROL TYPE 65 - The keyboard/printer is actually two inde-

pendent in-out devices. The keyboard section and the printer section are separately controlled and separately addressed. The two control systems, line unit outgoing (LUO) for the printer and line unit incoming (LUI) for the keyboard, function independently except for a common timing system.

The signal provided by the keyboard and required by the printer is the standard five-element start/stop teletype code. An element in the code may be either a mark (current flow) or a space (absence of current). The character to be printed or the printer operation to be performed is determined by the configuration of marks and spaces that make up the five elements of the code. Figure 4-5 shows the timing relationships of the start impulse, the stop impulse, and the five code-element impulses in the standard teletype code.

When a key is struck at the keyboard, a five-bit keyboard buffer (LUI_{1-5}) is loaded, one bit at a time, with the five elements of the incoming teletype signal. As soon as the keyboard buffer is fully loaded, the LUI flag goes on. In-out pulse iot2 clears the flag and causes a 1 transfer of the contents of the keyboard buffer into the accumulator. As usual, the programmer may clear AC prior to the transfer by programming a 1 in bit 14 of the iot.

The printer control logic also includes a five-bit buffer (LUO_{1-5}). In-out pulse iot4 transfers the least significant five bits of the accumulator into the printer buffer and initiates one cycle in the printer control logic. During the printer cycle, the printer logic generates the five-element teletype code from the information in the buffer. At the end of the printer cycle, the buffer is clear and the LUO flag goes on. In-out pulse iot2 clears the flag, as is required before each printer cycle. Both printer pulses (iot2 and iot4) are generated by the single instruction, tls.

4-7 FLOW CHARTS

Paragraph 4-8 describes the specific operations that can be executed by the computer. Each computer operation is a chronological sequence of events. Each individual event is a change in the state of the computer.

The flow charts show the operations as sequences of events. The major states flow charts (Figure 4-6) show the sequences that make up the various computer cycles. Each sequence begins at the top of a flow chart. Time is represented by horizontal bars on a nonlinear scale. Each horizontal bar represents the occurrence of a time pulse. The time pulses are written in

the left hand column. The true time scale is shown in the drawing of the computer memory cycle (Figure 4-2).

Each vertical path on a flow chart represents a sequence of events for a specific operation. Arrows indicate the direction of flow. At various time pulses the line of flow is broken by a rectangle in which is written the specific event that occurs at the corresponding time pulse. All events that are written within a single horizontal bar along a single flow line occur at the same instant in time. For purposes of clarity, certain simultaneous events may be shown in separate rectangles.

Note that in many cases the state of a flip-flop (or register) is sensed by the same time pulse that changes the state of the flip-flop being sensed. This is possible because of the delay inherent in the flip-flop or its input gating; i.e., the change in state of the flip-flop outputs lags behind the pulse applied to the input gating. Therefore the present state of a flip-flop can be sensed at the same time that the flip-flop is cleared, and the outputs of a register can be used at the same time that new information is transferred into the register.

If a specific event in a given line of flow depends only upon time; then that event is written alone in the rectangle. However, if other conditions which may or may not be fulfilled also govern the specific event, then these other conditions are also written in the rectangle. The conditions are written to the left of a colon; the specific event caused by the conditions is written to the right of the colon.

In some cases several sequences of events may begin with the same partial sequence. In this case the entire group of sequences is represented by a single flow line showing the common events. A branch point which distributes the flow into several separate sequences indicates the point at which the several sequences diverge. For example, in a fetch cycle all instructions are retrieved from memory by the same set of events. However, after the instruction code is transferred to the instruction register, the sequence diverges depending upon whether the instruction requires one cycle or two cycles. Each diverging line then has further branch points depending upon other conditions.

Movement along any specific branch must depend upon the fulfillment of some specific condition. The appropriate conditions are written on the individual branch lines. In all

two-cycle instructions the state of MB_4 is checked. If MB_4 is 1, the major states device, MS, is put into the defer state; if MB_4 is 0, MS goes into the execute state. With the time pulse at which this event occurs, the line of flow branches into two possible sequences. One branch is followed if MB_4 is 1; the other branch is followed if MB_4 is 0.

In some cases separate branches may join, indicating that the events following the intersection point are the same for both sequences. Whenever a branch point or an intersection point occurs, arrows are drawn on all incoming lines.

A single path from top to bottom of any flow chart represents a single computer cycle. The path is entered at the top of the chart, according to the conditions listed. At the bottom of the chart each path is terminated by a reference to the cycle that follows the completed sequence.

In the major states flow charts only those events that are peculiar to an individual sequence are shown in the line of flow through the chart. The events that are common to all cycles are listed in a column at the left of the charts. These common events include the events that make up the standard memory cycle. Also common to all cycles are those events that synchronize the interrupt logic to the main timing system.

The major states flow charts show all of the operations executed within computer memory cycles. Other internal processor operations are shown at the right of Figure 4-6. A flow chart of the chain of special pulses (SP0 to SP4) is shown in the upper right of the figure. Below the flow chart are the logical equations which define various other pulses and control levels. In the lower right is a table of instruction decoding.

The PDP-4 input-output operations are shown in a different form. The events produced by the in-out pulses are listed in Table 4-1. This table provides the link between the fetch cycle in-out transfer flow line and theflow chart of the individual in-out operations (Figure 4-7). The sequences of events making up the in-out operations do not depend upon any sequence of time pulses. Instead, they depend upon signals from the in-out devices or delays included within the control unit logic. Delays between the various events in each sequence are shown by breaks in the line of flow; the length of the delay is written in the break.

4-8 COMPUTER OPERATIONS

The operations performed by the computer are those that make up the special pulse console functions, the memory cycle, the instruction and break sequences in the major states, and the transfer of information between the computer and in-out devices.

a SPECIAL PULSE OPERATIONS - The operations governed by special pulses are shown in the upper right of Figure 4-6. When power is first applied to the computer logic, the initial state of the various computer flip-flops is indeterminate. As a result it is possible for the initial states of flip-flops at power turn-on to cause information losses by generating unwanted information transfers. A power clear pulse is used to prevent such information losses. Whenever the main power switch is operated, the power clear pulse clears the control flip-flops in the memory and in the in-out equipment control units.

All other special pulses result from using the operating keys on the console. The events produced by these pulses are shown in the flow chart in the upper right of Figure 4-6. Whenever any operating key is turned on, a logic level is asserted in the internal processor. For all console operations except Stop, the OR function (KEY MANUAL) generates a manual pulse which in turn triggers the chain of special pulses SP0 to SP4. This chain of special pulses times the execution of the appropriate operation. In all special pulse chain operations except Continue, SP1 also generates the initial clear pulse BEGIN. This pulse prepares the computer for operations by clearing various registers and control flip-flops throughout the system.

At the end of the chain, SP4 begins the memory cycle by triggering T1. If the computer is operating in the repeat mode, SP0 triggers a variable delay whose duration is determined by the setting of the console speed switches. If the operating key is still on at the end of the delay, the special pulse chain is again initiated by triggering SP0.

b MEMORY CYCLE - Most of the events required for the basic memory cycle are common to all cycles and are shown in a column at the left of Figure 4-6. The memory cycle begins at T1, with the clearing of the memory buffer and the transfer of an address to the memory address register. The latter event is not shown as common to all cycles. Instead, address transfer is shown in each individual cycle flow chart because the source of the address varies, depending upon the major state of the computer.

At T2 the read level is enabled by setting flip-flop R. Just prior to T3, flip-flop RS is set. This produces the strobe which transfers a word from the addressed memory location to the memory buffer. At T4, the read level is disabled by clearing flip-flop R. At the same time, flip-flop W is set.

If the computer is operating in single step mode or the stop key is on, T5 clears flip-flop RUN. This flip-flop is also cleared if the computer is operating in single instruction mode and is performing the final cycle of an instruction provided that no break has been synchronized in a previous cycle. Pulse T5 synchronizes the interrupt logic to the computer timing system. If a break has already been synchronized, the break cycle is included in the current instruction. If the break is synchronized in the final cycle of an instruction, the computer halts before performing the break cycle.

Time pulse T5 also begins the assertion of the inhibit level by setting flip-flop I. Immediately following T5, RS is cleared. The 0 state of RS in conjunction with the 1 state of W enables the write level.

At T7, both inhibit and write levels are disabled by clearing flip-flops I and W. If the computer is going to continue in normal operation, MA is cleared in preparation for the next memory cycle. If flip-flop RUN is 0, the computer halts. The halt takes precedence over any other flow line shown leaving T7 in the flow charts.

c MAJOR STATES - Events that occur in the cycles for each of the four major states are shown in the main portion of Figure 4-6. Fetch cycle events (at the left) occur in two distinct groups. The standard program control and instruction retrieval operations are in the first half of the cycle. Operations required for individual instructions are executed in the second half of the cycle.

If a previously executed instruction was an iot, the last in-out pulse is generated at the same time that the normal fetch cycle events occur. The normal events include the clearing of IR, the transfer of an address from the program counter to the memory address register, and the incrementing of the program counter. After the instruction is retrieved from memory, the instruction code is transferred from the memory buffer to the instruction register. This transfer does not require a transfer pulse. Instead, the setting of flip-flops in MB causes the immediate transfer of information on into IR. This type of "transition" trans-

fer is indicated by the letter "T" in the flow charts.

After the instruction code is transferred to IR, the flow branches into two main sequences. The flow line for the one-cycle instructions goes to the left; the flow line for the two-cycle instructions goes to the right. The specific events required for the execution of the one-cycle instructions are shown at the left of the figure. In addition to the time pulses, several control levels are involved in the execution of these instructions. These control levels are defined by the equations shown at the right of Figure 4-6. The flow line for the in-out transfer instructions shows the generation of the in-out pulses according to the configuration of bits 15 to 17 of the iot instruction word. The actual operations produced by these pulses, and the decoding of the device code, are given in Table 4-1.

From the final time pulse the flow lines continue to a defer cycle or an execute cycle in the case of the two-cycle instructions and the deferred Jump. For the nondeferable one-cycle instructions, the flow line returns to another fetch cycle unless the normal program sequence is being interrupted.

To the right of the fetch cycle is the flow chart of the defer cycle. During defer, the address of the instruction is used to retrieve another address from memory. For a Jump, this address is used as the operand and the computer returns to the fetch state. For a two-cycle instruction, this address is used to retrieve the true operand, and the computer enters the execute state.

For all two-cycle instructions, the required memory reference is made in the execute cycle. For most of these instructions, the strobe transfers the operand from memory to MB just prior to T3. However, if the instruction is depositing information in memory, the assertion of IA0 disables the strobe and new information is transferred into MB at T3. At the end of the cycle, the computer returns to the fetch state unless a break is requested.

The break cycle is shown in the flow chart at the right. The line of flow diverges into three branches, depending upon whether a data break, a clock break, or a program break has been requested. At the end of the cycle the computer returns to the fetch state unless another break is requested.

d IN-OUT TRANSFERS - When the instruction code for the in-out transfer group appears in IR, bits 15 to 17 are decoded into the three in-out pulses. The operations executed by

these in-out pulses are shown in Table 4-1.

Table 4-1 includes all of the iot instructions for the type 25 real time option, the reader, the punch and the Model 28 keyboard/printer. The pulses governing in-out information transfers usually serve only to initiate operations in a specific device control unit by clearing various control flip-flops. After operations are initiated, the computer continues with other instructions while the device control unit proceeds independently with its own operations.

The input-output operations of the control units are shown in a separate in-out flow chart (Figure 4-7). All in-out operations except keyboard input are initiated by the in-out pulses. The keyboard input sequence is initiated by striking a key. There is no sequence of timing pulses for the input-output operations; each individual event in an in-out sequence either is triggered by a delay from some previous event or else is triggered by a signal received from the in-out device.

TABLE 4-1 TIMING CHART: IN-OUT TRANSFER INSTRUCTIONS

Instruction Decoding iot = instruction code 70

iot MB^1_{14} T5: AC CLEAR

iot MB^1_{15} T1: PIO4

iot MB^1_{16} T7: PIO2

iot MB^1_{17} T5: PIO1

Device Selection

Interrupt Logic: 00

PIO1 CLOCK FLAG: PC+1

PIO2 MB^1_{12}: 1 ⟶ PROG ENABLE

MB^0_{12}: 0 ⟶ PROG ENABLE

PIO4 0 ⟶ CLOCK FLAG

MB^1_{12}: 1 ⟶ CLOCK ENABLE

MB^0_{12}: 0 ⟶ CLOCK ENABLE

Reader Logic: 01

PIO1 RD FLAG: PC+1

PIO2 C(RB) V C(AC) ⇒ C(AC)

0 ⟶ RD FLAG

0 ⟶ RD RUN

PIO4 0 ⟶ RD FLAG

RB CLEAR

0 ⟶ $RD_{1,2}$

1 ⟶ RD RUN

TABLE 4-1 TIMING CHART: IN-OUT TRANSFER INSTRUCTIONS

(Continued)

Reader Logic (cont'd):	01	
	MB_{12}^{1}: RD BIN ⟶ RD MODE	
	MB_{12}^{0}: RD ALPHA ⟶ RD MODE	
	(see Figure 4-7)	
Device Selection (cont'd)		
Punch Logic:	02	
	PIO1	PUN FLAG: PC+1
	PIO2	PUN CLEAR
		assert PUN IDLE
		(negates PUN FLAG)
	PIO4	assert PUN ACTIVE
		(negates PUN FLAG and PUN IDLE)
		$C(AC_{10-17})$ V C(PB) ⇒ C(PB)
		(see Figure 4-7)
Keyboard (LUI):	03	
	PIO1	LUI FLAG: PC+1
	PIO2	negate LUI FLAG
		C(LUI) V C(AC) ⇒ C(AC)
IO Status:	03	
	PIO4	C(STATUS WORD) V C(AC) ⇒ C(AC)

TABLE 4-1 TIMING CHART: IN-OUT TRANSFER INSTRUCTIONS

(Continued)

Teleprinter (LUO): 04

PIO1	LUO FLAG: PC+1
PIO2	0 ⟶ LUO FLAG
PIO3	C(AC) ⇒ C(LUO)
	START
	(See Figure 4-7)

4-9 USE OF DRAWINGS

The complete system logic is shown in logic drawings illustrating Chapters 6, 7, 8 and 9. Reference to these drawings is essential in understanding the detailed operation of the system. Because these drawings are the most frequently used source of troubleshooting information, it is important to be familiar with the symbols and conventions which they employ.

The standard DEC logic symbols used on the logic drawings are explained in the DEC Digital Logic Handbook. Additional symbols used in PDP-4 drawings are shown in Figure 4-3. Each circuit included in the logic drawings is identified by type as well as by its physical location in the computer.

Circuit type is always shown as a four-digit number. This number is the same type number used to identify the circuit in the DEC catalog.

Examples:

4105 . . . . . 5 inverters (500-kc series)
1105 . . . . . 5 inverters (5-mc series)
1607 . . . . . 3 pulse amplifiers (5-mc series)

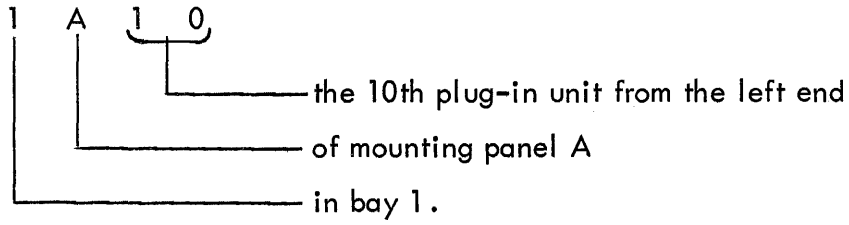
All circuits other than logic nets are shown as blocks on the logic drawings. Besides the four-digit type number, these blocks usually include a two-letter mnemonic abbreviation of the circuit function.

Examples:

DE . . . . . delay
PA . . . . . pulse amplifier
PG . . . . . pulse generator
SD . . . . . solenoid driver
BD . . . . . bus driver

The circuit location code is lettered directly below the circuit type number. Circuit location code is shown as a single letter preceded by one digit and followed by one or two digits.

Example:



Terminal designations are formed by adding the pin letter to the plug-in unit location code described above.

Example:

1A10M ——— pin M of the connector in position 1A10

Each logic drawing is laid out with rectangular map coordinates. The horizontal coordinates are 1 to 8 (from left to right) and the vertical coordinates are A to D (from top to bottom). Because a single drawing may contain a number of networks, coordinates are usually included in figure references to specific networks within a logic drawing. For example, a reference to the circuit "in Figure 6-3B4" would mean that the circuit is located at coordinates B4 of logic diagram 6-3 (the third diagram referred to in Chapter 6 of this manual).

Schematic diagrams for all computer circuits are bound into the back of the manual. These schematics are arranged in numerical order by circuit type designation. All circuits illustrated are described in Chapter 10.

CHAPTER 5

OPERATING PROCEDURES

5-1 GENERAL

The purpose of this chapter is to provide the operator with the information needed to operate the PDP-4 computer system. Descriptions of all controls and indicators are included, together with the instructions covering the operation of the standard in-out equipment. In addition, this chapter provides general instructions for manual loading and for operating the computer under normal conditions. These general instructions supplement the special instructions included in each program write-up.

5-2 CONSOLE CONTROLS AND INDICATORS

All of the controls and indicators of the PDP-4, except those associated with the in-out equipment, are located on the console operator control panel. This panel is divided into two sections: a panel face, which contains all the indicators and some of the operating switches; and a panel shelf at the bottom, which contains the operating keys and the rest of the operating switches.

When any console indicator is lit, the associated flip-flop is in the 1 state, or the associated function is true. Most toggle switches on the operator control panel are pushed up for on (or 1) and down for off (or 0). The operating switches are either toggle switches or rotary switches. The toggle switches are pushed to the right for on and to the left for off. The operating keys on the panel shelf are two- or three-position momentary-contact switches with a center off position. All of the keys produce operations when pressed down; only three of them produce operations when lifted up.

The operator panel is shown in Figure 5-1. Functionally, various switches and indicators on the panel may be divided into the following four groups:

(1) Registers (described in a below). Six sets of register indicators and two switch registers. These are located in the left two-thirds of the panel face, except for the 1-bit link register, which is located at right center.

(2) State indicators (b below). Four indicators located in the upper right of the panel face. Also included is the indicator for the run flip-flop.

(3) Operating switches (c below). Four toggle switches with associated indicators, located on the lower right of the panel face, and two rotary switches, located at the right of the panel shelf.

(4) Operating keys (d below). Five momentary-contact switches, located at the left of the panel shelf. The three two-position switches on the left are single logical keys -- that is, each produces a single logical operation. The two three-position switches on the right are dual logical keys -- each switch may produce either of two operations, depending upon whether it is lifted up or pushed down.

a REGISTERS -

Register indicators:

PROGRAM COUNTER (PC)

This 13-bit register contains the address of the next instruction in the program.

INSTRUCTION (IR)

Four-bit register which contains the instruction code of the instruction being performed or just performed.

MEMORY ADDRESS (MA)

This 13-bit register contains the address of the previous memory access. When the computer has stopped, these lights display the last address used. This is because the normal end-of-cycle clearing of MA is inhibited immediately prior to the halt.

MEMORY BUFFER (MB)

All transfers into or out of core memory take place through this 18-bit register. The MB register also holds the operand for all computational instructions. Furthermore, indexing is done directly in MB. When the computer has halted, MEMORY BUFFER indicates the word contained in the memory location addressed by MEMORY ADDRESS.

ACCUMULATOR (AC)

This 18-bit register is the major arithmetic and operating register in the computer and is involved in most computer operations. In computational instructions, the operand from

MB operates on the contents of AC. The results of computations always appear in AC. During in-out operations, AC is used as a buffer for transferring data between the computer and an in-out device control unit.

LINK (L)

This one-bit register is an extension of the accumulator for the construction of products and quotients. LINK also serves as an overflow flip-flop for 1s complement arithmetic, a carry link for 2s complement arithmetic, and may be used by the programmer as a general program flag.

Switch registers:

ADDRESS (AS)

A 13-bit toggle switch register through which the operator provides the memory address for the console functions Start, Examine, and Deposit.

ACCUMULATOR (ACS)

Lifting DEPOSIT transfers the contents of this 18-bit toggle switch register into the memory location addressed by the ADDRESS switches. Pressing DEPOSIT NEXT transfers the contents of ACS into the memory location addressed by PROGRAM COUNTER. During the instruction, Inclusive OR of AC Switches with AC (oas), the C(AC) are replaced by the inclusive OR function of the C(ACS) with C(AC).

b STATE INDICATORS -

RUN (RUN)

Lit while the computer is running in normal mode. Whenever the run flip-flop is cleared, the computer stops at the end of the current memory cycle.

FETCH (F)

When lit, indicates that the next cycle to be performed will be utilized to retrieve an instruction word from the memory location addressed by PC.

DEFER (D)

When lit, indicates that the next cycle to be performed will be utilized to retrieve a deferred address from the memory location addressed by the least significant 13 bits of MB.

EXECUTE (E)

When lit, indicates that the next cycle to be performed will be utilized to retrieve an operand from, or deposit an operand in, the memory location addressed by the least significant 13 bits of MB.

BREAK (B)

When lit, indicates that the next cycle to be performed will be utilized to execute a data break, a clock break or a program break.

c OPERATING SWITCHES -

POWER

Pushing this toggle switch to the right turns on computer power and lights the associated indicator. After turning POWER on, the operator must wait 5 seconds to allow the memory power supply to turn on before starting computer operations. When power is switched off, memory power turn-off is immediate but computer power remains on for another 5 seconds.

This switch normally applies power to the entire system unless a piece of in-out equipment is turned off individually.

SINGLE STEP

If this switch is pushed to the right the computer enters the single step mode, lighting the associated indicator. In this mode, the computer executes a single memory cycle when START is operated. Subsequent cycles in this mode are executed, one at a time, each time CONTINUE is operated.

SINGLE INST.

If this switch is pushed to the right the computer enters the single instruction mode, lighting the associated indicator. In this mode, the computer executes a single instruction when START is operated. Subsequent instructions in this mode are executed one at a time each time CONTINUE is operated. Note that if both SINGLE STEP and SINGLE INST. are on, the single step mode has preference.

REPEAT

Pushing this switch to the right lights the associated indicator, and causes operations

initiated by an operating key to be repeated as long as the key is held on. The operations are repeated at a rate determined by the setting of the SPEED switches.

SPEED

These switches allow the operator to vary the repeat interval from 40 microseconds to 8 seconds in five overlapping ranges. The switches include a five-position rotary switch and a potentiometer knob.

d OPERATING KEYS - All of the following keys except STOP and CONTINUE produce the BEGIN pulse at SP1. BEGIN clears various registers and flip-flops to prepare the computer for operation.

START

Pressing this key causes the computer to begin normal operation in the fetch state. The first instruction executed is taken from the location addressed by the ADDRESS switches.

STOP

Pressing this key clears the run flip-flop, causing the computer to halt at the end of the current memory cycle.

CONTINUE

Pressing this key causes the computer to resume normal operation, starting at the point indicated by the console lights. For use in the repeat mode, this key has a catch in the up position. Lifting the key causes the same operation as pressing it, but the key remains on until pushed off by the operator.

EXAMINE (EX)

When this key is lifted, the contents of the memory location addressed by the ADDRESS switches are displayed in both the ACCUMULATOR and MEMORY BUFFER lights. At the completion of Examine, the MA lights display the address of the memory location examined, and the PC lights display the address of the next consecutive location.

EXAMINE NEXT (EXN)

When this key is pressed, the contents of the memory location addressed by PROGRAM COUNTER are displayed in both the AC and MB lights. At the completion of Examine Next, the MA lights display the address of the memory location examined, and the PC

lights display the address of the next consecutive location.

DEPOSIT (DP)

Lifting this key deposits the contents of the ACCUMULATOR switches into the memory location addressed by the ADDRESS switches. At the completion of Deposit, the word deposited is displayed in the AC and MB lights. The MA lights display the address of the memory location holding the information and the PC lights display the address of the next consecutive location.

DEPOSIT NEXT (DPN)

Pressing this key deposits the contents of the ACCUMULATOR switches into the memory location addressed by PROGRAM COUNTER. At the completion of Deposit Next, the word deposited is displayed in the AC and MB lights. The MA lights display the address of the memory location holding the information, and the PC lights contain the address of the next consecutive location.

5-3 POWER CONTROLS AND INDICATORS

Alternating line voltage is distributed to the various computer power supplies through the type 813 power control panel located on the top of the bay 2 plenum door. A separate panel is provided for control of marginal check voltage. This panel (located at the top of the bay 1 plenum door) includes switches for applying marginal check voltage to specific portions of the computer. In addition, individual marginal check toggle switches are located on the front of each logic panel.

a POWER CONTROL PANEL TYPE 813 - Computer power is controlled by the POWER switch on the operator control panel (paragraph 5-2c). Turning this switch on activates the power control panel type 813 at the top of the bay 2 plenum door.

The type 813 power control panel (Figure 5-2) contains an elapsed-time meter, three MAIN POWER circuit breakers, and a MEM POWER toggle switch. An extra pair of circuit breakers is included for special applications. The elapsed-time meter counts the number of hours main computer power is on. The circuit breakers and toggle switch are normally left on at all times. The three MAIN POWER circuit breakers provide overload protection to the computer power supplies. Line voltage for the entire computer goes through these three circuit breakers.

The 813 control delays memory power turn-on. This delay turns on memory power 5 seconds after main power is turned on, to ensure that turn-on transients in the computer do not affect the memory. The MEM POWER switch on the type 813 panel permits turning off this delayed line-voltage input to the memory power supply. Memory power can thus be turned off separately from the rest of the computer for maintenance or troubleshooting purposes. If the system includes more than one memory module, the MEM POWER switch controls the delayed line voltage to all the memory power supplies.

For computer turn-off another set of delays is included in the power input to the computer. While memory power turn-off is immediate, the turn-off delay keeps main computer power on for 5 seconds after the console POWER switch is turned off.

b MARGINAL CHECK CONTROLS - The variable power supply type 734 furnishes marginal check voltages to the computer. It is located at the top of the bay 1 plenum door. This power supply provides voltages which can vary from 0 to -20 or +20 vdc, depending on the setting of the associated polarity switch. Output values between 0 and 20 volts are controlled by a variac and monitored on the MARGINAL CHECK voltage meter (Figure 5-3). Line voltage for the type 734 power supply is supplied directly from the power control panel with no intervening switch. Therefore, the marginal check power supply is on whenever the rest of the computer is on.

The plug-in unit pins to which marginal check voltage is applied are selected by three toggle switches (at the left of each logic panel on the front of the bays, Figure 5-4) and an associated three-position polarity switch (on the marginal check switch panel, Figure 5-3). To make positive marginal check voltage available to the computer, the polarity switch is set to +10MC. Marginal voltage can then be applied to the A lines of any panel by pushing up the top toggle switch on that pane, and to the B lines by pushing up the center toggle switch. For marginal check of the -15 vdc lines, the polarity switch is set to -15 MC and the bottom toggle switch of each panel being tested is pushed up. Note that all lines not being marginal checked receive their normal voltages automatically.

Although no marginal voltage can be applied to the computer if all three toggle switches on every panel are off (down), it is also possible to disconnect all marginal voltage inputs by turning the polarity switch to the OFF position. This applies normal voltages throughout the computer regardless of the settings of the toggle switches.

There are five toggle switches to the right of the three-position polarity switch on the marginal check switch panel (Figure 5-3). For all these switches, the up position is on; down is off. Only the first three switches on the left are used; the two on the right are spares.

The SENSE AMP switch applies marginal voltages to the memory module sense amplifiers. These sense amplifiers take up only a portion of panel 2D. For ease in troubleshooting, the sense amplifiers are isolated from the rest of the panel and are checked independently by the SENSE AMP switch. The rest of the plug-in units in panel 2D are marginal checked in the usual way by the switches on the mounting panel.

Marginal checking of the sensing circuits in the photoelectric tape reader is done with the FEED HOLE and INFO HOLES switches. To facilitate troubleshooting, separate switches are provided for feed-hole and information-hole sensing circuits. When one of these switches is pushed up, marginal voltage is applied to the +10 vdc lines in the corresponding circuit if the setting of the polarity switch is +10MC.

5-4 OPERATION OF IN-OUT EQUIPMENT

The three in-out devices most commonly used with the PDP-4 are a photoelectric paper tape reader, a paper tape punch, and a Teletype keyboard/printer. Manufacturer's manuals for these devices are provided with the PDP-4 computer. In addition, some special instructions and precautions are included below regarding the use of these devices as part of the PDP-4 system.

a PHOTOELECTRIC PAPER TAPE READER - The tape reader (Figure 5-5) is used by the computer as an input device. The reader is described in the manual for the Digitronics Perforated Tape Reader, Model 2500.

(1) Reader Controls - Operator control over the reader is exercised through two switches. The reader motor is turned on by pushing up the toggle switch located to the left of the read head cover. In front of the cover is the ready/load switch. Turning this switch to the right (load) releases the brake so that the operator may load or unload tape. Turning the switch to the left (ready) energizes the brake so that the reader may be controlled from the computer. The operator must also adjust the ready/load switch for the width of the tape loaded into the reader. For five-hole tape, the

switch must be pushed in all the way; for eight-hole tape, the switch must be pulled out as far as it will go.

(2) Loading - Before loading or unloading the reader, the ready/load switch must be turned to the right. This releases the brake and prevents damage to the tape. When loading the reader, the tape must be oriented so that it unfolds from the top of the fan-fold stack and with the edge nearer the feed holes, away from the operator. The unfolded stack is placed in the right-hand tape bin.

(3) Operation - Once the tape is properly loaded, energize the brake by turning the ready/load switch to the left. A reader iot can then control the reader by generating appropriate signals in the reader logic. The reader run signal closes the pinch rollers, causing the tape to move past the sensing photocells.

CAUTION

Before running a program including any reader iot's, the reader must be turned on and the brake must be energized. Failure to turn on the reader will cause the computer to hang up at the point where the reader flag is sensed. When this occurs, the program must be run again from the beginning. Failure to energize the brake will allow the tape to slide when a line is read, turning further information into gibberish.

(4) Unloading - After the reader has finished reading a tape, turn the ready/load switch to the right. The tape may then be removed from the left tape bin.

(5) Coding - When reading tape in binary mode, the reader reads only the six least significant bits of each character that has the eighth hole punched, and assembles three such characters into an 18-bit computer word. When reading tape in alphanumeric mode, the reader reads all eight bits in each character. The information read from the tape may be in any code. The code used by the keyboard/printer is listed in Table 5-1.

b PAPER TAPE PUNCH - The tape punch, used by the computer as an output device, is mounted inside a cabinet below the reader. The punch mechanism faces the door on the right of the cabinet (Figure 5-6). The fan-fold tape is fed to the punch from a container.

After punching, the tape is fed into the tape catcher. A slot on the front of the cabinet (below the tape reader, see Figure 5-5) allows access to this tape catcher without opening the cabinet door. Punch operation is as follows.

(1) Punch Controls - Operator control over the punch is exercised through two switches on the front of the punch cabinet. The punch motor is turned on by pushing the toggle switch up. Located above the toggle switch is a red button. Holding this button down feeds tape through the punch with only the feed hole punched.

(2) Loading - Turn off the punch motor, then load the tape into the punch as shown in Figure 5-6. After the tape has been properly positioned through the device, turn the punch on, and hold down the tape feed button long enough to feed approximately 18" of leader. Make sure the tape is feeding and folding properly in the tape catcher.

CAUTION

Before running a program including any punch iot's, the punch must be turned on. Failure to do this will cause the computer to hang up at the point where the punch flag is sensed. When this occurs, the program must be run again from the beginning.

(3) Unloading - To remove a length of punched tape from the tape catcher, first hold down the tape feed button long enough to provide an adequate leader at the end of the tape (and also at the beginning of the next length of tape).

Reach into the tape catcher slot and remove the fan-fold tape. Tear off the tape at a point within the leader area (that portion of the tape with only feed holes punched). After removal from the catcher, the stack of folded tape should be turned over so that the beginning of the tape is on top, and then labeled.

Make sure enough leader is left in the tape catcher to make at least three folds, with the first fold towards the catcher opening. This ensures that the tape will stack properly inside the bin. If necessary, hold down the tape feed button to provide additional leader.

c TELETYPE KEYBOARD/PRINTER - The keyboard/printer is two devices: the keyboard for input, and the printer for output. In most cases the operator communicates with the

computer through the keyboard/printer, especially when debugging a program.

The keyboard/printer motor is controlled by a toggle switch mounted on the cabinet at the right of the keyboard. Pushing the switch to the right turns on the motor. Complete instructions for installing paper and ribbon in the printer are given in Teletype Specification 5759S.

Figure 5-7 shows the keyboard. The code for the Teletype characters is listed in Table 5-1. Operating any of the regular keys on the keyboard prints the corresponding character and sends the corresponding code into the computer. Operating the figure shift key (FIGS) causes the keys to print figures and symbols. The letter shift key (LTRS) returns the machine to alphabetic printing. Operating the unmarked key in the lower right of the keyboard sends the code 00 into the computer. The computer or keyboard can lock the keyboard by sending the code 00 twice in succession.

The special keys located across the top of the keyboard do not send signals into the computer. The keyboard lock key (KBD LOCK) locks all of the regular keys on the lower part of the keyboard. The keyboard may be unlocked by pressing KBD UNLK.

Holding down the repeat key (REPT) causes any regular key that is hit to repeat continuously until REPT is released.

TABLE 5-1 TELETYPE CODE

Character		Octal Code	Character		Octal Code
A	-	30	Q	1	35
B	?	23	R	4	12
C	:	16	S	Bell	24
D	$	22	T	5	01
E	3	20	U	7	34
F	!	26	V	;	17
G	&	13	W	2	31
H	#	05	X	/	27
I	8	14	Y	6	25
J	'	32	Z	"	21
K	(	36	Space		04
L	)	11	Carriage Return		02
M	.	07	Line Feed		10
N	,	06	Figure Shift		33
O	9	03	Letter Shift		37
P	0	15			

Holding the local line feed key (LOC LF) causes continuous paper feedout. This feedout is about three times as fast as the standard line feed key repeated.

CAUTION

Before running a program that includes any printer iot's, the printer must be turned on. The logic for the outgoing line unit generates its own completion pulses. Failure to turn on the printer will cause the computer to execute the entire program without actually printing anything.

5-5 COMPUTER OPERATION

The computer may operate in any one of the following three modes: normal mode, or either of the two manual modes, single step or single instruction. Furthermore, the computer may simultaneously be in the repeat mode. In this mode the computer repeats any operation initiated by an operating key as long as the key is held down.

In addition to the three operating modes, the computer performs four independent console operations: Examine, Examine Next, Deposit, and Deposit Next. These operations are initiated by the corresponding operating keys, and may be performed in the repeat mode. The operator must utilize these operations for manual loading.

a MANUAL LOADING - In order to begin operations with an empty memory, the operator must load initial information into the computer manually. Manual loading utilizes the ACCUMULATOR and ADDRESS switches, and the DEPOSIT and DEPOSIT NEXT keys. Information so deposited may be examined by using the EXAMINE and EXAMINE NEXT keys.

Although the operator may load any desired instructions or data into the computer, a simple, 11-instruction manual loader is listed in paragraph 5-6a. This loader reads perforated tape in a special format and is usually utilized to read in a larger block format loader. The larger loader then may be used to read in full programs and data.

The manual loader reads the tape in binary mode. The first set of three lines and every odd-numbered set of three lines on the tape are control words. The second and all even-numbered sets of three lines on the tape are data words. If a control word is a dac instruction, the loader deposits the following data word in the location addressed by the control word.

Following the final data word is an extra control word. If this instruction is jmp, the computer enters normal operation at the location specified by the jmp address. The instruction may also be hlt. The final control word must be followed by a dummy last word if the programmer wishes the tape to stop after termination of the manual loader.

The operator should put the manual loader in the top of the memory. In this position, the routine is less likely to be destroyed during normal operation.

b NORMAL OPERATION - The START key initiates normal mode operation. It is also used, in conjunction with the manual mode toggle switches, to initiate operations in a manual mode. When START is pressed the computer starts in the fetch state; the first instruction access is made to the location specified by the ADDRESS switches.

When the computer is operating in normal mode, it can be halted by pressing STOP. Always press STOP before operating any other key.

If the computer has been halted while in normal mode, it can be restarted by pressing CONTINUE. This causes the program to continue where it left off. Note, however, that whenever a halt is followed by any operation that changes the state of the computer (such as Examine or Deposit), the computer must be started as at the beginning of normal mode operation. The address of the next instruction must be set into the ADDRESS switches before START is operated.

5-6 OPERATOR'S CHECKLISTS

The following checklists are provided for the operator's convenience. Checklists are included for loading the manual loader, and for operating the computer in normal mode, in either manual mode, and in repeat mode. Special instructions for running a particular program may be found in the write-up of that program.

a MANUAL LOADER - To place the manual loader in the top of the memory, follow the steps below in the order given:

(1) Turn off all ADDRESS and ACCUMULATOR switches. Make sure the mode switches SINGLE STEP, SINGLE INST. and REPEAT are all off.

(2) Set address 7762 into the ADDRESS switches. Lift DEPOSIT.

(3) Load the octal code 700101 into the ACCUMULATOR switches, and press DEPOSIT NEXT. Continue this process for all of the instructions in the manual loader. For each instruction, set the octal code into the ACCUMULATOR switches and press DEPOSIT NEXT. The manual loader routine is as follows:

Location	Octal Code	Mnemonic	Remarks
7762/r,	0	---	/ stored address
7763/	700101	rsf	/ reader wait loop
7764/	607763	jmp.-1	/ wait for word
7765/	700112	rrb	/ read buffer
7766/	700144	rsb	/ read another word
7767/	627762	jmp i r	/ exit subroutine
7770/	700144	rsb	/ enter here, start reader in binary
7771/g,	107762	jms r	/ get control word
7772/	047775	dac out	/ deposit control word
7773/	407775	xct out	/ execute final control word
7774/	107762	jms r	/ get data word
7775/out,	0	---	/ stored control word
7776/	607771	jmp g	/ continue

(4) Examine the memory locations containing the manual loader to make sure that the routine was inserted properly. Set address 7762 into the ADDRESS switches and lift EXAMINE. The contents of the addressed memory location are displayed in the MB and AC lights. Each successive memory location may then be examined by pressing EXAMINE NEXT.

b NORMAL MODE - To operate the computer in normal mode, follow the steps below in order given. This checklist assumes that the computer already contains a program which may be the manual loader (a above).

(1) Turn off all ADDRESS and ACCUMULATOR switches. Make sure the mode switches SINGLE STEP, SINGLE INST. and REPEAT are all off.

(2) Check program write-up for in-out equipment needed for the current program run. Where needed, load the equipment with the required tapes, etc.

(3) Turn on all in-out equipment to be used during program run. Failure to do this will cause the computer to hang up or run without actually performing the required information transfers The entire program must then be repeated from the beginning.

(4) Set address of first instruction into the ADDRESS switches.

(5) Press START.

(6) Check program write-up for any special instructions to be followed during the program run.

(7) To halt the computer, press STOP. To continue with the program, press CONTINUE. However, if the state of the computer has been changed after the halt (such as by an examine or deposit operation), proceed as for starting, from step 4.

c MANUAL MODES - To operate the computer in either of the manual modes, follow the steps below in the order given. This list assumes that the computer is already loaded with an appropriate program.

(1) Turn off all ADDRESS and ACCUMULATOR switches. Make sure the mode switches are all off.

(2) Turn on the appropriate manual mode switch, SINGLE STEP or SINGLE INST. Note that if both switches are on simultaneously, single step mode takes preference.

(3) Check program write-up for in-out equipment needed for the current program run. Where needed, load the equipment with the required tapes, etc.

(4) Turn on all in-out equipment to be used during program run. Failure to do this will cause the computer to hang up. The entire program must then be repeated from the beginning.

(5) Set address of first instruction into the ADDRESS switches.

(6) Press START. The computer will perform a single memory cycle if SINGLE STEP is on, or a single instruction if SINGLE INST. is on.

(7) For each subsequent cycle or instruction, press CONTINUE. The computer will stop after every cycle or instruction.

(8) To leave the manual mode, turn off the manual mode switch that is on. To complete the program in normal mode, press CONTINUE. However, if the state of the computer has been changed after leaving the manual mode, proceed as for normal mode starting (b above, step 4).

d REPEAT MODE - If an examine or deposit operation is being repeated, no stored program is necessary. If repeating in normal mode or in a manual mode, it is assumed that the computer is already loaded with an appropriate program. When repeating in single step or single instruction, the computer will halt after each memory cycle or each instruction, respectively. If repeating in normal mode, halting of the computer must be handled by the program.

(1) Turn off all ADDRESS and ACCUMULATOR switches. Make sure the mode switches are all off.

(2) Set the SPEED switches to the desired repeat interval.

(3) If repeating in a manual mode, turn on the appropriate manual mode switch, SINGLE STEP or SINGLE INST.

(4) If repeating program operations (i.e., in normal manual mode) prepare the in-out equipment as stated in b and c above.

(5) Set address for first memory access into the ADDRESS switches.

(6) To repeat Examine, turn on REPEAT and then lift and hold EXAMINE.

To repeat Deposit, set the desired word into the ACCUMULATOR switches, turn on REPEAT, and then lift and hold DEPOSIT.

To repeat Examine Next, lift and release EXAMINE. Then turn on REPEAT, and hold down EXAMINE NEXT.

To repeat Deposit Next, set the desired word into the ACCUMULATOR switches, and lift and release DEPOSIT. Then turn on REPEAT and hold down DEPOSIT NEXT. To clear the entire memory, set the SPEED switches to the shortest repeat interval, turn off all ACCUMULATOR switches, turn on REPEAT and hold down DEPOSIT NEXT. This procedure will clear the 4K memory in less than 1/5 second.

To repeat Start, turn on REPEAT; then press and hold START.

To repeat Continue, press and release START; then turn on REPEAT and lift CONTINUE. The up position of the CONTINUE key has a catch, so the operator need not hold the key on.

(7) To leave the repeat mode, turn off REPEAT.

CHAPTER 6

CONTROL

6-1 GENERAL

The control unit of the PDP-4 computer includes all the logic used to govern the following functions: timing of operations within the computer, transfer of information within the central processor, execution of the program and of individual instructions within the program, operation of the various registers, and storage and retrieval of information from memory. The present chapter describes those portions of the control logic that provide overall control of computer operations, including console control, timing, control of computer states, in-out transfer control, and program control.

Certain portions of the control unit are discussed in other chapters. The arithmetic unit control circuits, which govern all computational operations and accumulator transfers, are included in the discussion of the arithmetic unit (Chapter 7). The memory address register and the pulse logic that controls the core memory and the address and data transfers are included in the system (Chapter 8).

The control elements described in the present chapter are shown in three logic drawings, Figures 6-1, 6-2, and 6-3. For information on the use and organization of these drawings, refer to paragraph 4-9.

6-2 GENERAL CONTROL FUNCTIONS

General control functions of PDP-4 are shown in Figure 6-1. These functions control the operating mode of the computer and the initiation, timing, and halting of computer operation.

a CONSOLE CONTROL - The operator may control the computer through the keys and switches located on the console. The keys start and stop computer operations, while the switches allow the operator to turn the computer on and off and to control the mode of computer operation.

The power-clear logic associated with the power switch is shown in the lower right of

Figure 6-1. Relays D1 and D2 are located in the type 813 power control panel. When the power switch is turned on, terminal F of plug-in unit 1B16 is temporarily grounded. While pin F is at ground, pulses are produced by the power clock. The first power clock clears the run flip-flop so that the application of power to the computer cannot cause it to go into normal operation. While pin F is at ground and RUN is 0, the power clock generates power-clear pulses. These pulses clear various control flip-flops in the memory and the in-out equipment in order to prevent accidental information transfers.

When power is turned off, pin F is again grounded temporarily, producing the power clock and the power-clear pulses as at power turn-on. The clearing of RUN causes the computer to stop at the end of a memory cycle, so that no information is lost from memory even if power is turned off accidentally while the computer is running, such as, for example, by pulling the plug out of the wall.

The inputs to the logic from all the keys and several of the switches are shown in the lower left of Figure 6-1. The computer uses levels derived directly from most of the keys and switches, but the input logic also generates a number of functions from combinations of the switches in order to govern events that are required by two or more operations.

There are seven logical keys derived from five momentary-contact switch levers. This is because two of the switches may produce one or the other of a pair of operations, depending on whether the lever is lifted up or pushed down. Of the seven key functions, six initiate operations within the computer, while the seventh halts the computer. Five OR functions are generated from the initiating keys to control operations common to two or more keys. For example, a word is retrieved from memory on both of the operations Examine and Examine Next, while a word is deposited in memory on both of the operations Deposit and Deposit Next. KEY MANUAL is the OR function of all the six initiating keys. This function triggers both the special pulse chain and the main timing chain. The other OR functions generated by the input logic are as follows.

EXEXN

DPDPN

EXEXN + DPDPN

START + EX + DP

The stop key is ORed with the level from the single step switch to produce RUN STOP. Whenever the RUN STOP level is asserted, the computer is stopped at the end of the current memory cycle by clearing the run flip-flop. The stop switch asserts RUN STOP in order to end normal operation. The key function is asserted only when the momentary-contact stop lever is pressed. However, RUN STOP is asserted continuously when the single step toggle switch is on, so that the computer stops at the end of every memory cycle that is initiated by a key. The single instruction switch also generates RUN STOP, but only during the final cycle of any instruction. This is effected by the function F SET which indicates that the next cycle the computer is to perform is a fetch cycle and, therefore, that the current cycle must be the final cycle of the instruction being performed. In single instruction mode, a break cycle may be performed as part of either the preceding instruction or the following instruction, depending upon the time of break request synchronization.

The output of the repeat switch is inverted and used with the speed control (B6). The speed control includes both a five-position switch and a pot which allow the operator to vary the repeat interval from 40 microseconds to 8 seconds.

b SPECIAL PULSES - The initiation of any operation from the console is controlled by a chain of special pulses, SP0 through SP4. The logic governing this pulse chain is shown in Figure 6-1, B5 to B8. If any initiating key (ie any key other than stop) is turned on, the assertion of KEY MANUAL triggers pulse generator 1B09 which in turn produces SP0. This special pulse clears RUN and triggers the ten-microsecond delay in 1B13.

This delay allows the computer to complete the current memory cycle, in case an initiating key should be operated while the computer is running. After the computer has stopped, the positive pulse output of the delay, SPIP, triggers the remainder of the special pulse chain, SP1 through SP4. These are all negative pulses, one microsecond apart. Note, however, that the pulse amplifiers in the chain produce both the pulses and the delays between them. Each pulse amplifier is set to produce a one-microsecond output pulse. The falling edge of the output is the special pulse; the rising edge, one microsecond later, triggers the next pulse amplifier in the chain.

The chain of special pulses, SP0 through SP4, initiates computer states before the regular memory-cycle timing chain begins at SP4. In Examine, Examine Next, Deposit, and

Deposit Next the computer executes only one memory cycle following the special pulse chain; in Start and Continue the computer enters the normal operating mode.

In addition to producing individual functions for the specific console operations, SP1 also triggers the BEGIN pulse on all initiating operations except Continue (A2). BEGIN is an initial clear which prepares the computer for operation. Since Continue initiates operations according to the present state of the computer, no initial clear is required.

In repeat mode, the operation produced by any initiating key is repeated over and over again as long as the key is held on. If the repeat switch is on, the termination of the ten-microsecond level from delay 1B13 triggers the integrating one-shot, INT. This delay remains in the 1 state for an interval determined by the setting on the console speed switches. At the end of the delay interval INT returns to the 0 state, triggering SP0, provided one of the initiating keys is on (KEY MANUAL). Thus the operation initiated by a particular key is repeated over and over at a rate determined by the operator.

c TIME PULSES - The main timing system of the computer is a chain of time pulses, T1 through T7. These time pulses occur at irregular intervals throughout the 7.9-microsecond memory cycle. The time pulses are generated from the chain of time gate flip-flops, TG_1 through TG_7 (Figure 6-1, A3 to A7). An extra time gate, TGPC, enables the execute-cycle incrementing of the program counter during the isz instruction.

When operations are initiated from the console the special pulses control the various functions that must precede the first memory cycle. These functions include the clearing of the time gates by SP1P. Once the initial operations are complete, the memory cycle is started by SP4. This final special pulse sets TG_1, generating T1. The first time pulse, delayed by 1.0 microsecond in delay line 1A09 (B2) and the various gates, clears TG_1 and sets TG_2. The setting of TG_2 generates T2. In this way, a single 1 bit is rotated through the chain of time gates, successively generating each pulse in the chain.

The seven time pulses and the times at which they occur in the memory cycle are listed above the time gates in Figure 6-1. These time pulses are also shown in the diagram of the memory cycle, Figure 4-2. Each pulse in the chain triggers the TIME ROTATE pulse through one or both of the delays shown in B1 and B2. TIME ROTATE produces the next time pulse by clearing the single time gate that is in the 1 state and setting the next time

gate. The intervals between the time pulses are all either 1.0 microsecond or 1.3 microseconds, depending on whether only one or both of the delay lines are used. Time pulses 1, 2, 5 and 6 are delayed 1.0 microsecond; time pulses 3, 4 and 7 are delayed 1.3 microseconds.

The memory cycle is repeated over and over, by rotating the 1 from TG_7 back into TG_1, the entire cycle requiring 7.9±0.1 microseconds. However, T7 produces TIME ROTATE only if RUN is 1. The computer is halted by clearing the run flip-flop (d below). This prevents repetition of the memory cycle. Note, however, that the timing chain can be broken only at T7. Therefore, no matter when RUN is cleared, the computer halts only at the end of a full cycle.

As well as the seven time gates that control the time pulse chain, an additional time gate is provided to control the incrementing of the program counter. The same TIME ROTATE that produces T3 also sets TGPC. The TIME ROTATE that produces T5 also clears TGPC. The only way in which the memory buffer can be cleared between T3 and T5 of the execute cycle of isz, is by being incremented to zero. Thus if MB_0 is cleared while the condition $E \cdot ISZ \cdot TGPC^1$ is asserted, the program counter is incremented (paragraph 6-5b).

d RUN CONTROL - The computer operates in the normal mode with one memory cycle following another while the run flip-flop is 1. Each time the memory cycle ends, T7 triggers T1 of the next cycle, causing the computer to continue. Whenever RUN is cleared, the current cycle is completed and the timing chain ends at T7.

Initially RUN is cleared by the power clock, to prevent the computer from going into normal operation when power is turned on. The flip-flop is also cleared by SP0 so that the computer always halts before beginning any operation initiated from the console.

The operations Start and Continue put the computer into normal operation by setting RUN at SP3. Because none of the examine or deposit operations use the normal mode, RUN remains clear for the single memory cycle of these four operations.

When the computer is operating, RUN may be cleared by the operate instruction Halt ($OP1 \cdot MB_{12}^1$) or by T5 if RUN STOP is asserted. RUN STOP governs the halting of the computer in the single step and single instruction modes, but it is also asserted whenever the stop key is operated.

6-3 MAJOR STATES

Every memory cycle that the computer performs must be performed in one and only one of four major states. These states are fetch, execute, defer and break. The state that the computer is in during any given memory cycle depends on the state of the four-state device shown in the upper left of Figure 6-2. This major states device, MS, has four inputs and four outputs. Whenever a positive-going pulse appears at any input, the corresponding output is asserted and the other three outputs are negated.

The state of MS is stabilized by the four type 4115R diode gates in 1C01. Each of these gates is an OR gate for ground levels, and an AND gate for negative levels. A positive-going pulse on a single input asserts the corresponding output and negates the other three outputs by satisfying the OR-gate condition at the diode gates to the other three sections of the device. Satisfying the OR gates in these other three sections generates three negative levels which satisfy the AND-gate condition in that section of the device whose output is asserted. Satisfying this AND gate continues to assert the corresponding output even after the input pulse has disappeared.

For example, if the computer is next to perform a fetch cycle, one of the input gates in B2 must be satisfied, producing a positive-going pulse at 1D03P. This cuts off transistor 1C02F, asserting the output level F, and satisfying the diode OR gates in the other three sections of the device at inputs 1C01U, P and F. The ground outputs of these diode gates cut off transistors 1C01V, R and K, producing negative levels which disable outputs E, D and B, and satisfy the AND-gate conditions at the fourth diode gate, 1C01W, X and Y. The negative output of this fourth diode gate turns on transistor 1C01Z, holding 1C02F at ground, and continuing to assert F.

The conditions that cause the computer to enter each of the major states are described in a through d below. The computer normally changes state at the end of the memory cycle, ie at T7.

a FETCH - When MS asserts the output F, the computer is in the fetch state and the current memory cycle is utilized to retrieve an instruction word from memory. The conditions that cause the computer to perform a fetch cycle are shown in Figure 6-2, B1 and C1.

In the console operation Start, normal operation of the computer begins with the fetch

cycle. In normal operation, the computer enters the fetch state at the completion of every instruction (ie, if no difer cycle or execute cycle is called for) provided there is no break request. The computer also returns to the fetch state, from T1 of the execute cycle of the instruction Execute. In this fetch cycle, the computer interprets the operand of Execute as an instruction to be executed.

b EXECUTE - When MS asserts the output E, the computer is in the execute state, and the current memory cycle is utilized for the memory reference of a two-cycle instruction. The conditions that cause the computer to perform an execute cycle are shown in Figure 6-2, C2 and C3.

The computer enters the execute state on any of the examine or deposit console operations. This is because the memory cycles performed in these two types of operations are performed as the execute cycle of the instructions Load Accumulator and Deposit Accumulator, respectively. In normal program operation, the computer enters the execute state at the completion of the fetch cycle of any two-cycle instruction that is not indirectly addressed ($\overline{IA3} \cdot MB_4^0$). If a two-cycle instruction is indirectly addressed, then the computer automatically enters the execute state after the defer cycle is completed.

c DEFER - When MS asserts the output D, the computer is in the defer state, and the current memory cycle is utilized to retrieve a deferred address from memory. The conditions that cause the computer to enter the defer state are shown in Figure 6-2C3. The computer enters the defer state following the fetch cycle of a deferrable instruction if the indirect address bit MB_4 is 1. The deferrable instructions include all of the two-cycle instructions ($\overline{IA3}$) and the one-cycle instruction Jump (which is included in the condition by ORing IB0 with $\overline{IA3}$).

d BREAK - When MS asserts the level B the computer is in the break state and the current memory cycle is utilized to perform a data break, a clock break, or a program break. The conditions that cause the computer to perform a break cycle are shown in Figure 6-2C4. The computer enters the break state if a break request is received from the interrupt logic and the current memory cycle is the final cycle of the instruction being performed (ie, the computer is not entering either the defer state or the execute state).

6-4 INSTRUCTION CONTROL (MINOR STATES)

When the computer is in any of the three major states fetch, execute, or defer, it must also be in one of the minor states; that is, the computer must be performing some specific instruction. The minor state of the computer is determined by decoding the contents of the instruction register. This register contains the four-bit code of the instruction currently being executed.

In addition to the levels provided by the instruction decoder, the augmented instructions are further decoded into sets of pulses which perform the indicated microinstructions. The in-out transfer pulses are described here (c below); the operate pulses, however, are described with the operate logic (paragraph 7-5b).

a INSTRUCTION REGISTER - When the computer is in one of the major program states, the minor state is defined by the contents of the instruction register. The computer is put into a specific minor state by loading the instruction code into the instruction register during the fetch cycle. The computer then remains in the same minor state until the next fetch cycle, unless a break cycle occurs first.

The instruction register and associated control circuits are shown in Figure 6-2, C5 to C7. The instruction register is cleared initially by BEGIN. It is then cleared at T1 of every fetch cycle and break cycle. In the latter case, the register is left clear throughout the cycle. The instruction register is also cleared at T1 of the execute cycle of the instruction Execute; since the computer is returned to the fetch state at the same time that IR is cleared, the instruction code portion of the operand retrieved during the memory reference of xct is loaded into the instruction register by the fetch cycle.

The four-bit instruction part of any word that is retrieved from memory during a fetch cycle (ie an instruction word) is loaded into the instruction register. The transfer of information from MB to IR is not performed on a time pulse. Instead, both registers, IR and MB, are cleared at the beginning of the fetch cycle. Then, if any bit of MB is set during the fetch cycle, the drop in the 1 output of the MB bit sets the corresponding bit of IR. In this way the instruction code that is loaded into MB by the memory strobe is then loaded immediately into IR without waiting for a time pulse.

In addition to loading an instruction code during every fetch cycle, codes are also loaded into IR for certain console operations and for the instruction Call Subroutine. In an

examine operation, IR_1 is set, producing the instruction code for Load Accumulator (20). In a deposit operation, IR_3 is set, producing the instruction code for Deposit Accumulator (04).

Immediately following the fetch cycle of cal, IR_2 is set by 20—→ MA, producing the instruction code for jms. Thus at the same time that address 20 is loaded into MA, the minor state switches from cal to jms and the computer completes the instruction as jms 20.

b INSTRUCTION DECODER - The outputs of the IR flip-flops are applied to the diode decoder shown in the upper right of Figure 6-2. This decoder produces two sets of four levels each. The four levels, IA0 through IA3, correspond to the four numbers that may be contained in the two more significant bits of IR (IR_0, IR_1). The four levels IB0 through IB3 correspond to the four numbers that may be contained in the two less significant bits of IR (IR_2, IR_3).

The instruction decoder does not produce command levels that correspond to individual instructions. Instead, each of the eight levels IA0 through IA3 and IB0 through IB3 corresponds to a group of four instruction codes. For example, IA0 is asserted when IR_0 and IR_1 contain 00. Level IA0 thus represents those instructions with octal codes 00, 04, 10 and 14 (corresponding to four-bit codes 000 0, 000 1, 001 0 and 001 1 respectively). The more significant digit in the octal code corresponds to the octal number contained in IR_{0-2}. The less significant digit in the octal code is either 0 or 4, depending upon whether the least significant bit of the four-bit instruction code is 0 or 1.

Accordingly, the octal codes for the instructions do not correspond to the potput levels from the instruction decoder. The numbers as the ends of the level designations correspond to the four-bit codes expressed in a quaternary number system. In the control circuits that execute the various operations within an instruction, the single instruction must be indicated by ANDing one of the IA levels with one of the IB levels. In other words, the final decoding into individual instructions is done in the control circuits, rather than at the instruction decoder.

However, the level outputs from the decoder are in many cases used to control operations common to a group of instructions. For example, in all one-cycle instructions IR_0 and IR_1 are both 1. As a result, the computer may enter the execute state only on the condition

$\overline{IA3}$. Information is deposited in memory during the execute cycle of any instruction in which both IR_0 and IR_1 are 0; consequently the memory strobe is disabled by the assertion of the level IA0.

Both IA0 and $\overline{IA3}$ are needed by the computer logic in polarities opposite to those in which they are produced by the instruction decoder. The inversion of these two levels is shown in D7. Buffering of the 0 output of IR_3 is also shown. This level is buffered for use in arithmetic unit control.

c IN-OUT TRANSFER CONTROL - All transfer of information between the computer and in-out devices is controlled by microprogramming within the iot instruction. This control is exercised through the in-out pulses and the clear-accumulator level (Figure 6-2, D2 to D4). When the instruction code for an in-out transfer is loaded into IR, decoder levels IA3 and IB2 are asserted. This enables the diode gates in the iot logic.

The programmer determines which in-out pulses (PIO) are generated by adjusting the configuration of bits 15 through 17 of the iot instruction word. If bit 17 is a 1, the first in-out pulse is generated by T5. Similarly, bits 16 and 15 generate PIO2 and PIO4 at T7 and T1, respectively. The clear-AC level PIOC1 is generated by a 1 in bit 14. This level is applied directly to accumulator control (paragraph 7-5c). In preparation for the transfer of information into the accumulator, PIOC1 causes T5 to clear AC.

If the real time option type 25 is included in the computer, the device selector (paragraph 9-2a) decodes bits 6 through 11 of the iot instruction word to determine the in-out device that is addressed. The device selector actually selects the device by switching PIO pulses 1, 2 and 4 into iot pulse lines 1, 2 and 4 for the specified device.

In the standard computer, no decoding of bits 6 through 11 is required because the single iot instruction controls only the reader. In this case, the PIO pulses are applied directly to the reader control unit. Furthermore, PIO2 is applied directly to the input gating of the accumulator (paragraph 7-2a). Since the standard machine contains no information collector, the outputs of the reader buffer are applied directly to the accumulator input gates.

6-5 PROGRAM CONTROL

The program control elements comprise the program counter and the associated count logic and transfer logic. Each instruction in the program is retrieved from the memory location addressed by the contents of the program counter. The program counter is stepped one position during each fetch cycle. This causes instructions to be taken from consecutive memory locations.

The programmer controls the program sequence by means of the skip instructions and the jump instructions. The skip instructions cause the computer to skip one instruction in the normal sequence if a specified condition is satisfied. The skip is implemented by advancing the program counter one extra position. The jump instructions can transfer program control to any chosen location. This transfer is accomplished by loading a new address into the program counter.

a PROGRAM COUNTER - The program counter is shown in the upper half of Figure 6-3. This counter is composed of type 4204 dual flip-flops that are connected in the carry configuration.

Flip-flops in the counter are numbered to correspond to bits in the address portion of the instruction word. The configuration of the counter as shown is that required for use with an 8K memory. In this case, PC_4 is not used, while PC_{5-17} holds the required 13-bit address. For use with a 4K memory, plug-in unit 1D15 (bits 4 and 5) is removed, and PC_{6-17} then specifies a 12-bit address. For use with a 1K memory, plug-in units 1B15 and 1B16 (bits 4 through 7) are removed and the remainder of the register holds the required 10-bit address.

Normal counting and skipping in the program counter are produced by the pulse PC + 1. This counting pulse increments the program counter because the program counter flip-flops are connected in a carry configuration. This means that whenever a carry pulse changes PC_n from 1 to 0, PC_n generates a carry pulse that complements PC_{n-1}.

Prior to the transfer of any information into the program counter through the gated set inputs, PC must be cleared through the direct clear inputs. Addresses may be transferred into the program counter from bits 5 through 17 of the memory buffer, the memory address register, and the address switches.

b PROGRAM COUNT LOGIC - The program counting pulse PC + 1 is generated by the

logic shown in the lower right of Figure 6-3. This pulse increments the counter both for ordinary counting and for skipping. To count memory locations in the program, in a program break, in certain console operations, and in the subroutine-calling jump, the program counter is incremented by PC + 1. The standard program counting occurs at T1 of every fetch cycle. In any examine or deposit operation PC + 1 is pulsed by SP4. Thus after performing one Examine or Deposit operation, the operator may examine the contents of the next memory location or deposit information into the next memory location without operating the address switches.

In a program break or a subroutine-calling jump, program control is always transferred to the location that follows the deposit location of the address of the interrupted program. For this reason, the program counter is incremented at T5 in the execute cycle of Jump to Subroutine or Call Subroutine, or in a program break cycle.

All other advances of the program counter cause the computer to skip an instruction. In an operate group skip instruction, if the addressed condition is satisfied, PC is incremented by OP1 (paragraph 7-5b). During indexing operations PC is incremented if the index number becomes zero during the instruction. This condition is indicated to the program count logic by a change in MB_0 from 1 to 0 while TGPC is 1 during the execute cycle of isz.

The time gate is asserted from T3 to T5. The only way in which MB_0 can change from 1 to 0 between these two time pulses (while E·ISZ is asserted) is by incrementing the memory buffer to zero. The other two-cycle skip instruction, sad, causes a skip if the contents of the accumulator differ from the contents of the addressed memory location. After the first exclusive OR is executed in sad, PC +1 is pulsed by T5 if the accumulator does not contain zero.

The gate that controls in-out skips depends upon whether or not the real time option is installed. In the standard computer a skip is produced by PIO1 if the reader flag is on. But if the computer includes the type 25 option, PC is incremented by the pulse from the in-out skip logic (paragraph 9-2e).

c PROGRAM TRANSFER LOGIC - All transfers of program control are effected by clearing the program counter and transferring a new address into it. Following the transfer, PC counts successive memory locations in the usual manner. The program counter transfer

logic utilizes the following four pulses (lower left, Figure 6-3):

PC CLEAR

The program counter is cleared immediately prior to the transfer of an address into it. Any of the conditions that produce an address transfer (see below) clears the counter at the time pulse or special pulse immediately preceding the transfer.

PCMB1 ——>PC

An address is transferred from the memory buffer to the program counter at T6 of Jump.

PCMA1 ——>PC

An address is transferred from the memory address register to the program counter at T4 in the execute cycle of jms or cal, or in a program break cycle. This causes a routine to begin at the memory location that follows the deposit location of the address of the interrupted program.

PCAS1 ——>PC

An address from the console address switches is provided to the program counter at SP2 of the operations Start, Examine, and Deposit.

CHAPTER 7

ARITHMETIC UNIT

7-1 GENERAL

The standard PDP-4 arithmetic unit includes two full-word (18-bit) registers and a link. The link is a one-bit register that extends the capability of the accumulator. The two full-word registers are the accumulator, AC, and the memory buffer, MB. In two-operand arithmetic and logical operations, the memory buffer is a passive register. Although MB makes one of the operands available to the accumulator input gating and the arithmetic unit control logic, MB itself is not affected by the operation. All operations performed on the operands during two-operand instructions are actually executed in the accumulator. However, in single-operand instructions, both arithmetic registers are active; logical negation is performed in AC, and indexing is performed in MB.

This chapter describes the accumulator, the link, and associated control circuits. The memory buffer is described in detail as part of the memory system (paragraph 8-3). The control elements associated with the arithmetic unit and described in this chapter are the overflow logic, the operate logic, and the logic nets that generate the various control pulses for the accumulator and the link.

The arithmetic unit is shown in two logic drawings, Figures 7-1 and 7-2. For information on the use and organization of these drawings, see paragraph 4-9.

7-2 ACCUMULATOR

The accumulator is composed of 18 type 4203 flip-flops (Figures 7-1 and 7-2). Each of these 18 flip-flops has a gated complement input as well as the usual 0 and 1 gated inputs. In the figures, three inverters and ten capacitor diode gates are shown associated with each accumulator flip-flop. These inverters and gates are all contained within the flip-flop module. As well as the usual buffered 0 and 1 outputs, each accumulator flip-flop also has both a carry output and an indicator output. The carry output is an unbuffered 0 output. The fall of this output is used as a pulse for the bit-to-bit "ripple" carry in addition operations (d below).

Except for ripple carry connections and single-bit pulse connections from the information collector, every accumulator control pulse is applied to the input gates of all bits in the register. The ripple carry output for each bit is applied only to the next more significant bit of the register. Level gates for transfers from the memory buffer, the reader buffer, and the console accumulator switches are applied to each accumulator bit from the corresponding bit of the source register.

If the machine includes a type 25 real time option, the reader buffer connections are replaced by single-bit pulse inputs from the information collector. Each bit of the accumulator also receives outputs from the stages on either side as level gates for rotate operations. The accumulator and link are rotated together as one 19-bit register; thus, for rotate operations, both AC_0 and AC_{17} receive level gates from the link.

The outputs of the accumulator flip-flops are used for arithmetic and transfer operations as well as for rotate operations. The 0 outputs of the AC bits are applied to the AC arithmetic input gating, while the 1 outputs are applied to the transfer input gating of MB. If the real time option is installed, the 1 outputs of AC are also available to the output equipment through the information distributor.

Four types of accumulator input gating are described in the present paragraph. These are: 1) transfer gating, 2) rotate gating, 3) logic gating, and 4) arithmetic gating.

a TRANSFER GATES - Transfers to the accumulator may be made from the memory buffer, the reader buffer, and the console accumulator switches. If the computer includes the real time option, the reader buffer connections are replaced by connections from the information collector. In this case, information from the reader buffer and all other input devices is transferred into the accumulator through the information collector. Since all transfers into the accumulator are 1 transfers, a prior clear is required. The AC CLEAR pulse clears the entire register by pulsing the 0 input of every flip-flop (Figure 7-1B6).

The 1 transfer of the contents of MB into AC utilizes the pulse AC XOR MB. This pulse complements a bit of AC if the corresponding bit of MB is 1 (B6). This operation produces the exclusive OR function of the contents of MB and AC (c below). However, in the instructions lac and law, AC is automatically cleared before AC XOR MB is pulsed. Accordingly, the exclusive OR pulse sets any bit of AC which corresponds to a 1 in MB,

thereby effectively producing a 1 transfer.

The 1 transfer of the contents of the console accumulator switches into AC is produced through the bottom row of input gates by the pulse ACS1 → AC (Figure 7-1C6). In either of the console deposit operations, this transfer pulse is automatically preceded by a clear, as required. However, as part of an operate instruction, ACS1→AC actually produces the inclusive OR of the contents of ACS and AC unless the programmer microprograms the operate instruction to include a prior clear.

In the standard machine, the 1 transfer of the contents of the reader buffer into AC is produced by the in-out pulse P1O2 (C6). However, if the computer includes the real time option, the reader buffer connections are removed and all transfers from input equipment to AC are made through the information collector. All gating is performed in the collector so that the transfer of information from IC to AC is made by single-bit pulse inputs through column 6 of the taper pin block that is shown below the accumulator input gating. Each pulse from a bit of IC sets the corresponding bit of AC. Note that the standard transfer from RB as well as all transfers through the real time option are 1 transfers requiring a prior clear. This clear is not automatic and must be provided by the programmer through microprogramming the in-out transfer instruction.

b ROTATE GATES - Two rotate pulses are applied to the accumulator input gating. These are AC RIGHT ROTATE, and AC LEFT ROTATE (Figure 7-1C6). Each of these pulses produces a cyclic one-place shift of the contents of the accumulator: one to the right, the other to the left. In rotate operations, the accumulator is a 19-bit circular register with AC_0 linked to AC_{17} through the link (paragraph 7-3). As a result, for rotate purposes, the link may be considered to be to the left of AC_0 and to the right of AC_{17}.

Both rotate pulses are applied to both the 0 and 1 input gates of all flip-flops in the accumulator. On a right rotation, the gating levels to a specific bit of AC are provided by the next more significant bit. In a left rotation, the gating levels to a specific bit of AC are provided by the next less significant bit. The rotate pulses produce a bit-to-bit jam transfers in AC. For example, on a right rotation, AC_2 is set if AC_1 is 1, while AC_2 is cleared if AC_1 is 0.

The pulse AC RIGHT ROTATE transfers the contents of AC_n into AC_{n+1}. The right rotate

operation also transfers the contents of AC_{17} into the link, and the contents of the link into AC_0. The pulse AC LEFT ROTATE transfers the contents of AC_n into AC_{n-1}. The left rotate operation also transfers the contents of AC_0 into the link, and the contents of the link into AC_{17}.

c LOGIC GATES - The computer can perform three logic functions; these are logical negation, AND (conjunction), and exclusive OR. The program may produce the inclusive OR of two words by using negation and conjunction. However, the augmented instructions that transfer information into AC from the accumulator switches or input devices do not include an automatic prior clear. Failure to microprogram the required clear causes these instructions to produce the inclusive OR of the contents of AC and the source register. These instructions, however, can transfer information into AC only from external sources, not from memory.

The accumulator complement pulse AC CMA produces the logical negation of the word in the accumulator. Pulse AC CMA changes the state of each bit in the accumulator by pulsing the complement input. In 1s complement arithmetic, logical negation is equivalent to the arithmetic negative. If the contents of the accumulator are interpreted as a number, the complement pulse produces the 1s complement negative of that number.

The other two logic pulses produce the logic function of two words; one in the accumulator, the other in the memory buffer. The result appears in the accumulator. The exclusive OR function of the contents of MB and the contents of AC is produced by the pulse AC XOR MB (Figure 7-1B6). The exclusive OR function is produced by complementing a bit of AC if the corresponding bit of MB contains 1. The state of an AC bit after AC XOR MB depends upon the initial state of that bit and the state of the corresponding bit of MB as follows:

MB	AC (original)	AC (final)
0	0	0
0	1	1
1	0	1
1	1	0

As can be seen from the table above, the complementing of a bit of AC (if the corresponding bit of MB is 1) produces the exclusive OR function.

If all bits in the accumulator are originally 0, the final contents of AC are the same as the contents of MB; thus, if AC is cleared prior to the exclusive OR operation, AC XOR MB effects a 1 transfer of the contents of MB into AC (see a above). AC XOR MB is also the first of a pair of pulses which produce addition in the accumulator. Addition is produced by partial addition followed by a carry function. The partial addition is equivalent to the exclusive OR function (d below).

The AND function of the contents of MB and the contents of AC is produced by the 0 transfer AC MB0→AC. This pulse clears those bits of the accumulator which correspond to bits of MB containing 0. An AC bit contains 1 after AC MB0→AC only if it contained 1 before the pulse occurred and corresponds to a bit in MB which also contains 1. In this way the 0 transfer produces the bit-by-bit logical AND function of MB and AC.

d ARITHMETIC GATES - The accumulator includes two arithmetic gates. One of these enables the bit-to-bit ripple carry chain. This gate is used both in 1s complement and 2s complement addition operations, and is applied to all bits in the accumulator. The other arithmetic gate is used only in 1s complement addition, and is applied only to AC_{17}.

The addition operation is carried out in two stages. The first is a partial addition; the second is a carry function. The partial addition is performed by the AC XOR MB pulse which produces the exclusive OR function of the contents of MB and the contents of AC (c above). After the partial sum (ie the result of the partial addition) has been formed the full register carry pulse, AC CARRY, changes the exclusive OR into the true arithmetic sum. At the end of the operation, the number represented in the accumulator is the previous contents of the accumulator plus the contents of the memory buffer.

The partial sum is equal to the true arithmetic sum for any bit which does not receive a carry. If a sum of two binary numbers is considered on a bit-by-bit basis, the exclusive OR function of the two numbers is actually the correct sum in a given bit if there is no carry into that bit. For example, the sum of two 0s is 0. The sum of 1 and 0 is 1. The partial sum, ie the exclusive OR function, of two 1s is 0 (this last example, however, does require that there be a carry into the next more significant bit).

A given bit of the partial sum is valid as a bit of the true arithmetic sum provided that no carry into the bit is present. But if there is a carry into the bit, then that bit of the

partial sum is the opposite of the correct bit of the arithmetic sum. After the partial sum is produced, the full-register carry function changes the states of all those bits of the partial sum which are incorrect as bits of a true arithmetic sum.

The full-register carry pulse, AC CARRY, produces the correct carry function both by complementing certain bits in the accumulator and by initiating the ripple carry at those bits that it complements. The full register carry complements (ie carries into) a bit of the partial sum if the next less significant bits of the summands were both 1.

The computer cannot sense the previous state of a flip-flop, so instead it senses the corresponding configuration of the partial sum. This produces the same result because AC XOR MB, which produces the partial addition, changes the state of AC_n only if MB_n is 1. If after the partial addition there is 0 in AC_n and 1 in MB_n, then both bits must originally have been 1. The carry therefore complements AC_{n-1} if MB_n is 1 and AC_n is 0 after the exclusive OR is formed.

If AC CARRY changes an accumulator bit from 1 to 0, the carry output of that bit (an unbuffered 0 output) becomes asserted negative. The carry output of each AC bit is applied to a gate at the complement input of the next more significant bit. The drop in the carry output acts as a pulse at the capacitor-diode input gate. The gating level for these complement input gates is AC CARRY ENABLE. This gating level is applied to the ripple carry complement input gates in all AC bits.

In addition operations, the AC CARRY pulse is generated while AC CARRY ENABLE is asserted. Thus the partial addition of two 1s in the given bit of the accumulator produces a carry pulse into the next more significant bit. The carry pulse ripples up the register until a 0 bit is complemented. The complement pulse from either type of carry function (AC CARRY or the carry pulse produced by a bit changing state) complements a bit whether it is 0 or 1, but a 0 inhibits the ripple carry from propagating to the next bit.

Addition in the accumulator is performed in the following manner: The MB XOR AC pulse produces in the accumulator a partial sum of the contents of MB and AC. The carry pulse then initiates the carry chain at each place in the partial sum where the next less significant bit is a 0 resulting from the partial addition of two 1s. Each section of the carry chain propagates as far as is necessary to produce the correct sum of the contents of MB

and the original contents of AC.

The second arithmetic gate is the AC ADD ENABLE gate. This gate is applied only to AC_{17}. It is asserted only in 1s complement addition when AC_0 is 0. In the last stage of the accumulator, AC_{17}, the gating level for AC CARRY is asserted whenever AC ADD ENABLE is asserted and MB_0 is 1. In 1s complement arithmetic, the addition of two negative numbers requires that 1 be added to the least significant bit of the accumulator. If AC_0 is 0 and MB_0 is 1 after the exclusive OR pulse, then these bits must both have been 1 originally. In other words, the numbers in AC and MB were both negative before the addition. In this case AC CARRY complements AC_{17}, adding 1 to the least significant bit as required.

The ripple carry applied to AC_{17} is the AC END CARRY. In 1s complement addition operations, this pulse is generated by the ripple carry output of AC_0. If the state of AC_0 changes from 1 to 0 as the result of either the full-register carry or the ripple carry during a 1s complement addition, AC END CARRY complements AC_{17}, adding 1 to the least significant bit of the accumulator. That this arithmetic logic does in fact produce the correct sum of two binary numbers is proved in paragraph 7-4 below.

7-3 LINK

The link, L, is a type 4203 flip-flop module containing a basic flip-flop and ten capacitor-diode input gates. It is used to extend the capabilities of the accumulator. It may be cleared, complemented, or rotated as part of the accumulator. The link serves as an overflow flip-flop for 1s complement arithmetic, and as a carry link for 2s complement arithmetic. Since the state of the link may be sensed by skip instructions, the programming of multiple precision arithmetic is greatly simplified.

The link is cleared by BEGIN whenever any operation is initiated from the console. Program control over the link individually is exercised through two operate instructions: Clear Link and Complement Link. These are represented in the link logic by the conditions $OP1 \cdot MB_6^1$ and $OP2 \cdot MB_{16}^1$, respectively. Since the programmer can control the state of L, and can also sense its state through operate skip instructions, the link is available as a general program flag.

The program may also control the link as part of the accumulator through the two operate rotate

instructions. The AC rotate pulses are gated into the 0 and 1 link inputs by levels from AC_0 and AC_{17}. On AC rotations to the right, the rotate pulse is gated by the state of AC_{17}. Thus, L is set or cleared in a right rotation if AC_{17} is 1 or 0, respectively. On the other hand, the left rotate pulse adjusts the state of L according to the state of AC_0.

Three arithmetic gates affect the link. First, in 1s complement addition, if the accumulator overflows, the AC ONE COMP OV level is asserted. With this level asserted, T1 complements L if it is 0. The effect is to set L at T1 of the cycle following a 1s complement addition when the accumulator has overflowed.

The second arithmetic gate applied to L is the AC CARRY ENABLE level. This level, asserted in both 1s complement and 2s complement addition, gates the link carry pulse, L CARRY, into 1 input of the link. This carry pulse is generated only in 2s complement addition when the state of AC_0 changes from 1 to 0. In other words, the link is set if, as a result of a 2s complement addition, the sign of the accumulator changes from negative to positive.

The third arithmetic gating level gates AC CARRY into the link 1 input. This level, L TAD ENABLE, is asserted only during 2s complement addition when AC_0 is 0, and MB_0 is 1. The assertion of this level at the time of AC CARRY implies that, before the exclusive OR pulse, both AC_0 and MB_0 were 1. In other words, in 2s complement arithmetic, if the signs of both MB and AC are negative prior to the addition, the full register carry sets the link.

The three arithmetic gates for the link together have the following result: (1) L is set by a 1s complement addition overflow; (2) L is set if a 2s complement addition changes the sign of the accumulator from negative to positive; (3) L is set by the 2s complement addition of two negative numbers.

7-4 ADDITION ALGORITHM

Both 1s complement and 2s complement addition are possible in the PDP-4. The two algorithms corresponding to these operations are described in a and b below.

a ONES COMPLEMENT ADDITION - Assume that originally the accumulator contains A, and that the memory buffer contains B. Assume further that PS is the partial sum produced in AC by the AC XOR MB pulse, and that S is the arithmetic sum of A and B. For

convenience, first consider the simple case where A and B are both positive binary fractions whose sum is less than 1 (ie there is no overflow).

After the AC XOR MB pulse, a bit of the partial sum PS_n is equal to a bit of the sum S_n if, and only if, there is no carry into S_n. Should there be a carry into S_n, then the partial sum bit PS_n equals the complement of S_n. Because both signs are plus and there is no sign change, there is no carry into PS_{17}. Therefore $PS_{17} = S_{17}$.

To understand the operation of the two carry functions (full register carry, and ripple carry), divide PS into sections, starting at the right. The first section starts with PS_{17} and ends at the first bit PS_k which satisfies the conditions $PS_k = 0$, $A_k = B_k = 1$. The second section starts with PS_{k-1} and extends to the next bit that satisfies the same conditions as PS_k. Proceed in this way through the entire partial sum.

Since there can be no carry into it, the least significant bit of the partial sum must be correct. If this bit is 1, or if it is 0 resulting from the partial addition of two 0s, then there is no carry out generated. Because no carry exists, the next bit of the partial sum must also be correct. Proceed with each more significant bit of the partial sum until a bit PS_k is reached which is 0 resulting from the partial addition of two 1s. Bit PS_k is also correct; therefore, all bits of the partial sum in the first section are correct.

Because the partial sum in PS_k generates a carry, PS_{k-1} is not correct. A 1 from the first section is carried into PS_{k-1} by the full-register carry pulse AC CARRY. If PS_{k-1} is 1 (resulting from the partial addition of 0 and 1), then there must be a carry into PS_{k-2}. This carry is provided by the ripple carry which complements PS_{k-2} when PS_{k-1} changes from 1 to 0. In this way, the ripple carry propagates up the register until a 0 bit is encountered. If this 0 is the result of the partial addition of two 0s, then no further carry is generated. All further bits are correct up to the next 0 that results from the partial addition of two 1s; that is, up to the end of the section.

If the 0 that terminates the ripple carry results from the partial addition of two 1s, then there must be a carry into the next bit. However, the partial addition of two 1s is the condition that ends the section. The full-register carry pulse then begins a new ripple carry in the next section. The carry operation complements all incorrect bits of the partial sum. At the completion of the carry operation the result S is the correct sum of

A and B.

The preceding example shows that the addition algorithm works for the simple special case of two positive numbers. Before proving the algorithm for the remaining cases (including negative operands) four further necessary facts should be understood:

1) The sign bits are included in the partial addition -- that is, the partial sum of two minus signs (1s) is a plus sign (0).

2) Both carry functions are applied to the accumulator sign bit (AC_0). The sign bit is treated precisely as though it were a next more significant bit of AC.

3) The full register carry complements AC_{17} if two negative numbers are added.

4) If the sign changes from minus to plus in the carry operation, the ripple carry propagates into AC_{17}. This is an end-around carry.

Assume that the binary point is to the left of the most significant bit -- that is, all computer numbers are 17-bit fixed-point fractions. The computer representation of the positive number x is therefore

$$+.[x]$$

where the brackets enclose the number contained in AC_{1-17}. The sign of this number is contained in AC_0.

In 1s complement arithmetic the negative of a number is produced by subtracting the number from a number that is all 1s. This is done by changing the sign and subtracting the magnitude from $(1 - 2^{-17})$. The computer representation of the number -x is therefore

$$-.[1 - x - 2^{-17}]$$

Let x and y be positive 17-bit fractions. Four different cases of addition are possible:

Case one: $x + y$

Case two: $(-x) + (-y)$

Case three: $x + (-y)\ ;\ y \leq x$

Case four: $x + (-y)\ ;\ y > x$

Case one, the addition of x and y, is discussed above in the basic description of the addition algorithm. Addition proceeds as follows:

$$\begin{array}{l} +.[x] \\ \underline{+.[y]} \\ +.[x+y] \end{array}$$

If $(x + y) \geq 1$, the overflow changes the sign during the carry operation. Consequently, if the addition of two positive numbers results in a negative answer, it is apparent that the sum has exceeded the capacity of the accumulator. When such an overflow occurs, the contents of AC represent the number

$$-.[x + y - 1]$$

In case two, the addition of (-x) and (-y), the partial addition and all carries except the sign-bit carry operations would produce the following result:

$$\begin{array}{l} -.[1 - x - 2^{-17}] \\ \underline{-.[1 - y - 2^{-17}]} \\ +.[1 + 1 - x - y - 2^{-17} - 2^{-17}] \end{array}$$

The partial addition of two 1s in the sign bit causes the full register carry to complement AC_{17}, adding 2^{-17} to the contents of the accumulator. If $(x + y) < 1$, the carry overflows into the sign bit. The complete result is:

$$-.[1 - (x+y) - 2^{-17}]$$

which is the computer representation of $-(x+y)$.

If $(x + y) \geq 1$, there is no carry into the sign bit. In case two (two negative operands), the absence of a carry into the sign bit indicates that the result of the addition overflows, ie, that the sum exceeds the capacity of the accumulator. Consequently, if the addition of two negative numbers results in a positive answer, it is evident that the sum has exceeded the capacity of the accumulator. The accumulator then contains the number:

$$+.[1 - (x + y - 1) - 2^{-17}]$$

The sign is plus, and the magnitude is the complement of $(x + y - 1)$.

In case three, the addition of x and (-y), where y is less than x, the partial addition and all carries except the sign-bit carry operations would produce the following result:

$$\begin{array}{l} +.[x] \\ \underline{-.[1 - y - 2^{-17}]} \\ -.[1 + x - y - 2^{-17}] \end{array}$$

Because $y \leq x$, it follows that $(1 + x - y) \geq 1$. Therefore the carry overflows into the sign change (- to +) causes an end-around carry. The complete result is:

$$+.[x - y]$$

Since, in case three addition, the signs of the operands are different, the sum can never

exceed the capacity of the accumulator. This is also true of case four addition, for the same reason.

In case four, the addition of x and (-y), where y is greater than x, the partial addition and all carries except the sign-bit carry operations would produce the following result:

$$\begin{array}{l} +.[x] \\ \underline{-.[1 - y - 2^{-17}]} \\ -.[1 + x - y - 2^{-17}] \end{array}$$

Because $y > x$, it follows that $(1 + x - y) < 1$. As a consequence, there is no overflow or end-around carry and the above result is the computer representation of the negative number $x - y$, ie $-(y - x)$.

b TWOS COMPLEMENT ADDITION - As in the discussion of 1s complement arithmetic above, assume that originally the accumulator contains A, and that the memory buffer contains B. Assume further, that PS is the partial sum produced in AC by the AC XOR MB pulse, and that S is the arithmetic sum of A and B.

The function of the full-register carry, AC CARRY, and the ripple carry is exactly the same as described above for 1s complement addition. In other words, the algorithm described above for the addition of two positive numbers in 1s complement arithmetic is identical to the algorithm in 2s complement arithmetic for the addition of two positive numbers. In 2s complement arithmetic, however, addition involving negative operands differs. Before proving the algorithm for the cases including negative operands three further characteristics of 2s complement addition should be understood:

1) The sign bits are included in the partial addition -- that is, the partial sum of two minus signs (1s) is a plus sign (0).

2) Both carry functions are applied to the accumulator sign bit (AC_0). The sign bit is treated precisely as though it were a next more significant bit of AC.

3) Neither carry function affects AC_{17}. The full register carry, AC CARRY, is not applied to AC_{17}; and there is no end-around carry from AC_0 into AC_{17}.

Assume that the binary point is to the left of the most significant bit -- that is, all computer numbers are 17-bit fixed-point fractions. In 1s complement arithmetic, the negative of a number is produced by subtracting the number from a number that is all 1s. In 2s

complement arithmetic, however, the negative of a number is produced by subtracting the number from a number that is all 0s. This is done by changing the sign and subtracting the magnitude from 1. The computer representation of the number - x is therefore:

$$-.[1 - x]$$

The four possible cases of addition of two positive 17-bit fractions are:

Case one: $x + y$

Case two: $(-x) + (-y)$

Case three: $x + (-y);\ y \leq x$

Case four: $x + (-y);\ y > x$

Case one, the addition of x and y, is discussed in the basic description of the addition algorithm for 1s complement arithmetic (a above). The contents of AC after addition represent the number $+.[x + y]$. If $(x + y) \geq 1$, the overflow changes the sign during the carry operation. Consequently, if the addition of two positive numbers results in a negative answer, it is apparent that the sum has exceeded the capacity of the accumulator. When such an overflow occurs, the contents of AC represent the number

$$-.[x + y - 1]$$

In case two, the addition of (-x) and (-y), the partial addition, and all carries except the sign bit carry operations would produce the following result:

$$\begin{array}{l} -.[1 - x] \\ \underline{-.[1 - y]} \\ -.[1 + 1 - x - y] \end{array}$$

If $(x + y) < 1$, the carry overflows into the sign bit. The complete result is:

$$-.[1 - x - y]$$

which is the computer representation of $-(x + y)$.

If $(x + y) \geq 1$, there is no carry into the sign bit. In case two (two negative operands), the absence of the carry into the sign bit indicates that the result of the addition overflows, ie, that the sum exceeds the capacity of the accumulator. Consequently, if the addition of two negative numbers results in a positive answer, it is evident that the sum has exceeded the capacity of the accumulator. The accumulator then contains the number

$$+.[1 - (x + y - 1)]$$

In case three, the addition of x and (- y), where y is less than x, the partial addition and all carries except the sign bit carry operations would produce the following result:

$$\begin{array}{l} +.[x] \\ \underline{-.[1-y]} \\ -.[1+x-y] \end{array}$$

Since $y \leq x$, it follows that $(1 + x - y) \geq 1$. Therefore the carry overflows into the sign, and the complete result is

$$+.[x-y]$$

Because, in case three addition, the signs of the operands are different, the sum can never exceed the capacity of the accumulator. This is also true of case four addition, for the same reason.

In case four, the addition of x and (- y), where y is greater than x, the partial addition and all carries except the sign bit carry operations would produce the following result:

$$\begin{array}{l} +.[x] \\ \underline{-.[1-y]} \\ -.[1+x-y] \end{array}$$

Because $y > x$, it follows that $(1 + x - y) < 1$. As a consequence, there is no overflow, and the above result is the computer 2s complement representation of the number $x - y$, ie $-(y - x)$.

7-5 ARITHMETIC UNIT CONTROL

Arithmetic unit control includes all the logic nets that generate the control pulses for the accumulator and the link. Also included is the overflow logic for 1s complement addition, the carry link logic for 2s complement addition, and a diode decoder net that allows the computer to sense the accumulator for zero contents.

a ACCUMULATOR DECODER - The diode decoder which senses whether or not the accumulator contains zero is shown in Figure 7-1A2. The 0 outputs of all 18 accumulator bits are brought to the inputs of this diode decoder. If all the bits of the accumulator contain 0, this decoder generates the level AC = 0 at both ground and negative assertion levels. The accumulator is sensed both for zero contents and for nonzero contents by the OP SKIP logic (b below). The output of the decoder, asserted at ground level, provides the

negatively asserted AC $\neq$ 0 level required by the OP SKIP logic. Note that the decoder does not assert the AC = 0 level when the accumulator bits are all 1s (representing -0 in 1s complement arithmetic). In 1s complement arithmetic, the decoder asserts an "AC = +0" level only.

b OPERATE LOGIC - The levels and pulses developed during an operate instruction (opr, code 74) are generated by the operate logic. This paragraph describes the generation of the two special time pulses which time all the events in operate instructions, as well as the logic that generates the OP SKIP level. Three accumulator pulses (the two rotate pulses and the complement pulse) are also described here since these pulses are produced only by operate instruction.

The two instructions opr and law both correspond to the same four-bit instruction code in IR (1111 = IA3·IB3). The execution of law is governed by the level OP LAW (Figure 7-1D1) which corresponds to the opr/law configuration of IR and the condition that MB_4 is 1 (code 76). The execution of the opr instructions is governed by the operate time pulses OP1 and OP2 (D3). These pulses are generated by T5 and T7, respectively, when IR is in the opr/law configuration and MB_4 is 0 (code 74). All operations within the operate group instructions are executed by OP1 and/or OP2.

In an operate skip instruction, bits 8 to 11 of the augmented instruction code determine the condition for the skip. The skip logic is shown in Figure 7-1, B2 and C2. Bits 9 to 11 address the individual skip condition or skip conditions. The 1 states of bits 9, 10 and 11, respectively, address the 1 state of the link, zero contents in the accumulator, and negative contents in the accumulator (ie, the 1 state of AC_0). Whenever the addressed condition is satisfied, the level OP SKIP COND is asserted.

In an operate skip instruction, OP1 increments the program counter (paragraph 6-5b) if the level OP SKIP is asserted. This level is equivalent to OP SKIP COND if MB_8 is 0, but if MB_8 is 1, the truth value of OP SKIP is opposite to that of OP SKIP COND. Thus, when a 0 is programmed in bit 8 of the instruction word, the skip occurs if the addressed condition is satisfied; on the other hand, a 1 programmed in bit 8 causes the skip if the addressed condition is not satisfied. If no condition is addressed, MB_8^0 produces an absolute no-skip, while MB_8^1 produces an absolute skip.

The following three register control pulses are generated only by operate instructions:

AC RIGHT ROTATE, AC LEFT ROTATE

A pulse on either of these lines (B5, C5) rotates the contents of the accumulator and the link one place in the direction indicated. The directional pulses are produced by the AC ROTATE pulse according to the configuration of bits 13 and 14 of the instruction word. A right rotation is specified by MB^{1}_{13}; a left rotation is specified by MB^{1}_{14}. Each rotate instruction may produce a one-place or two-place rotation, depending upon the state of bit 7 of the instruction word. AC ROTATE is automatically produced by OP2 (B1); however, it is also produced by OP1 if MB_7 is 1. Thus, the programmer determines the direction of rotation by adjusting bits 13 and 14, and determines the number of rotations by adjusting bit 7.

AC CMA

The accumulator is complemented only by the operate instruction, Complement Accumulator. The cma instruction is represented by the condition $OP2 \cdot MB^{1}_{17}$ (A5).

c TRANSFER LOGIC - The logic that generates the four accumulator transfer pulses is shown in Figure 7-1. These four pulses include the AC clear pulse and three pulses that transfer information into AC from other registers.

AC CLEAR

The net that governs the clearing of the accumulator is shown in Figure 7-1D2. At the initiation of operations from the console, BEGIN clears AC. This is done primarily to prepare AC for use in the deposit operations. The accumulator is also cleared automatically by any instruction that loads information into AC from MB. This occurs at T1 in the execute cycle of lac, and at T5 in the single cycle of law. The programmer controls the clearing of AC through the operate instruction Clear Accumulator ($OP1 \cdot MB^{1}_{5}$) and through programming a 1 in bit 14 of any in-out transfer instruction ($T5 \cdot PIOC1$).

AC XOR MB

This pulse produces the exclusive OR of MB and AC as a logic function, as partial addition, and as a comparison function. It also produces the 1 transfer of information from MB to AC if AC is cleared first. The logic governing AC XOR MB is shown in Figure 7-1, D3 to D5. The exclusive OR function is produced at T4 in the execute cycle of any instruction

whose instruction code begins with 2 or 3 (IA1). This includes both addition instructions and the instructions Exclusive OR and Load Accumulator. AC XOR MB also produces a 1 transfer at T6 in the single cycle of law. In the instruction sad, AC XOR MB produces a comparison function. The first exclusive OR at T4 clears AC if the contents of MB and AC are identical. At T5, the program count logic (paragraph 6-5b) increments the program counter if the accumulator does not contain zero -- that is, if the original contents of MB and AC were different. At T6, a second exclusive OR pulse restores the original contents of AC.

AC MBO→AC

This pulse (C4) is generated at T5 in the execute cycle of the instruction and. The pulse clears each AC bit which corresponds to an MB bit containing 0, generating the bit-by-bit logical AND function between the contents MV and the original contents of AC.

ACS1→AC

The 1 transfer of a word to AC from the console accumulator switches (D4) occurs in two situations: in the operate instruction oas ($OP2 \cdot MB_{15}^{1}$) and in either of the console deposit operations (SP2·KEY DPDPN). Although the accumulator is cleared automatically prior to the transfer in console operations, the clear is not automatic in the case of the operate instruction. Thus, when the program loads information into AC from the switches, the program must clear AC prior to the transfer.

d ARITHMETIC LOGIC - Arithmetic operations utilize three levels and five pulses. Two of the pulses, AC CMA and AC XOR MB, are described in b and c above. This paragraph describes the three levels and the remaining three pulses. The generating logic elements are shown in Figure 7-1.

These levels and pulses, plus AC XOR MB, perform the addition algorithms. The six signals are grouped in three pairs. The first pair, a level and a pulse, performs the principal carry function for both 1s and 2s complement addition. The other two pairs, a pair of levels and a pair of pulses, govern the carry effects derived from the sign bits. The first pair is associated with the full register carry; the second pair, with the ripple carry. In each pair of signals, one is for 1s complement and the other is for 2s complement. Since the addition instruction codes differ only in bit 3, the two types of addition are differentiated in the logic by the state of IR_3.

AC CARRY ENABLE, AC CARRY

The AC CARRY ENABLE level is asserted while TG_3 is 0 during the execute cycle of either of the addition instructions (B4). The level is therefore asserted throughout the execute cycle of add or tad except between pulses T3 and T4. At T4, when AC XOR MB produces in the accumulator the partial sum of the contents of MB and AC, the carry enable level is not yet asserted. Because of the delay in the inverters, AC CARRY ENABLE is asserted shortly after T4.

The full register carry pulse, AC CARRY, is produced at T5 while the carry enable level is asserted. The two-stage addition operation (in either 1s or 2s complement) is always produced in the following manner: First, the exclusive OR function produces the partial sum at T4; then AC CARRY ENABLE is asserted; and finally AC CARRY is pulsed at T5.

AC ADD ENABLE, L TAD ENABLE

These two levels differentiate the effect of the full register carry for 1s and 2s complement addition. The logic developing these levels is shown in C3 and C4. The effect of AC CARRY on AC_n depends upon the configuration of bit n+1 of both AC and MB. At the input gating to AC_{17} the condition AC_0^0 is replaced by AC ADD ENABLE. This level is equivalent to AC_0^0 during 1s complement addition (IRB_3^0). Thus AC CARRY can affect AC_{17} only during 1s complement addition.

In either type of addition, a given bit AC_n is complemented by AC CARRY when the condition $AC_{n+1}^0 \cdot MB_{n+1}^1$ is true. In 2s complement addition (IRB_3^1) the equivalent condition for the sign bits (ie $AC_0^0 \cdot MB_0^1$) produces the level L TAD ENABLE. This level gates AC CARRY into the 1 input of L. Consequently, when two negative numbers are added in 2s complement arithmetic, the full register carry sets the link.

L CARRY, AC END CARRY

These two pulses determine the effect of the ripple carry from AC_0 (A4). In 1s complement addition, an end-around carry is required if the sign bit changes from 1 to 0. The AC_0 carry out, $ACCP_0$, is therefore gated to produce AC END CARRY when IRB_3 is 0. In 2s complement arithmetic, however, no end-around carry is desired. So, instead, $ACCP_0$ is gated by IRB_3^1 to produce L CARRY. Both the link carry and the end-around carry are further gated by AC CARRY ENABLE, so that they have no effect except in addition operations. In 1s complement addition, the ripple carry from AC_0 complements AC_{17}; in 2s

complement addition, the carry has no effect on AC_{17} but, instead, sets the link.

e OVERFLOW LOGIC - Overflow logic is provided for use only in 1s complement addition. The logic elements that check for overflow in the accumulator are shown in Figure 7-1, B3 and A4. The overflow logic includes two inverters cross connected as flip-flop AC POSS OV, and a diode-transistor logic net. The setting of the flip-flop indicates that overflow may occur in an addition. The output level of the logic net, when asserted, indicates that an overflow actually has occurred.

If two numbers of opposite signs are added together, the magnitude of the result must be less than the magnitude of the larger number. As a result, no overflow can occur when the signs of the operands differ. The overflow possible flip-flop is set by the accumulator full register carry if AC_0 is 0 after the partial addition. In other words, the overflow possible flip-flop is set in any addition operation (1s or 2s complement) if, before the addition, the signs of MB and AC are the same.

When two numbers of like sign are added together, the result should also have the same sign. To ensure that this is the case, the states of the sign bits are again checked after the addition is performed. This check is performed in the logic net. If an overflow is possible during 1s complement addition and if, after the addition, the sign bits of MB and AC are different, then the AC ONE COMP OV level is asserted. This level causes T1 to set the link at the beginning of the following cycle. The link thus acts as an overflow flip-flop for 1s complement addition. The overflow possible flip-flop is cleared by BEGIN and subsequently by T1 at the beginning of every cycle. As a result, the same time pulse that sets the link in the case of an overflow also clears AC POSS OV, disabling the 1s complement overflow gate.

CHAPTER 8

MEMORY

8-1 GENERAL

The core memory system of PDP-4 consists of a memory address register and decoders, a memory buffer, and a memory module. A choice of two types of memory module are available: a 1K memory module, providing storage for 1024 eighteen-bit words; or a 4K memory module, providing storage for 4096 eighteen-bit words. Both modules are composed of a coincident-current core bank and associated read/write logic, sense amplifiers, and timing circuits. Memory capacity may be further expanded by adding a second 4K memory module to the computer, providing a total storage of 8192 eighteen-bit words. In all memory systems, regardless of capacity, provision is included for direct external access to memory through the data interrupt logic.

The 1K memory module uses a 10-bit address, while the 4K memory module requires a 12-bit address. If a second 4K memory module is added to the system both modules share the same memory addressing element and memory buffer. The memory address register includes an extra flip-flop which selects the module, while the location within the selected module is specified by the usual 12-bit address. Both types of memory module are described in the present chapter. The two modules are similar in operation. They differ only in the number of cores in each core plane, and in the logic that selects the address windings.

The memory system is shown in five logic drawings, Figures 8-1 through 8-5. Figures 8-1 apply to the 4K and 8K memories. Figures 8-1, -2, -4, and -5 apply to the 1K memory. For information on the use and organization of these drawings, see paragraph 4-9.

8-2 MEMORY ADDRESS LOGIC

The memory addressing element of the computer is composed of the memory address register, four binary-to-octal memory address decoders, and the input logic associated with the address decoders, and the input logic associated with the address register.

a MEMORY ADDRESS REGISTER - The memory address register is shown in Figure 8-1. The flip-flops in the register are labeled MA_4 to MA_{17}. Flip-flop MA_4 is not used. The designations of the remaining flip-flops correspond to the memory address portion of the instruction word. Each memory access is made to the location specified by the contents of the MA register.

The configuration of the register shown in Figure 8-1 is for use with an 8K memory. The 12-bit address contained in MA_{6-17} specifies one of the 4096 (2^{12}) locations within a single memory module, while MA_5 selects the module. For use with the 4K memory, plug-in unit 1C15 is removed and MA_{6-17} then contains a standard 12-bit address. For use with the 1K memory, plug-in units 1C15 and 1C16 are removed. Then the contents of MA_{8-17} provide the 10-bit address necessary to specify one of the 1024 (2^{10}) locations within the 1K memory module. The 10-bit address or the 12-bit address is decoded by the memory address decoders to select a particular pair of X and Y windings within the core bank. Each core register within a memory module corresponds to a single pair of X and Y windings.

All transfers into the memory address register are 1 transfers requiring a prior clear. The MA register may be cleared by pulsing the direct clear inputs to the Type 4204 flip-flops. Addresses may be transferred into MA from either the program counter or the memory buffer. In the instruction cal, the address 20 is loaded into MA by directly setting MA_{13} (B6). For use in data interruptions, address lines from a high-speed in-out control unit may be connected to the bottom row of capacitor-diode input gates through column 4 of the taper pin block shown below the register. An address from the address lines is loaded into MA by the pulse DBA1 → MA, which is equivalent to the ADDRESS → MA pulse from the interrupt logic (paragraph 9-2d). In a clock break, the pulse 7 → MA (applied to MA_{15-17} through column 6 of the tape pin block) loads address 7 into the register.

b ADDRESS TRANSFER LOGIC - In normal operation, an address is transferred into MA at the beginning of every memory cycle, and MA is then cleared at the end of the cycle in preparation for the next cycle. The logic that governs the transfer of addresses within the internal processor is shown at the lower left of Figure 8-1. Prior to the first memory cycle when an operation is initiated from the console, MA is cleared

by SP1. It is then cleared at the end of every memory cycle, while the computer continues in normal operation (RUN = 1). The computer halts at the end of any memory cycle in which RUN is cleared. The clearing of RUN inhibits the clearing of MA at the end of the cycle. Then, after the computer has halted, the memory address indicators on the console display the address to which access was made during the final cycle of operation.

An address is transferred into MA at T1 of every memory cycle. In a fetch cycle, the address is provided by the program counter for instruction retrieval. In execute and defer cycles, the address is provided by the memory buffer for retrieval of the operand or a deferred address. In the instruction Call Subroutine the transfer pulse MB1→MA loads address 20 into MA by generating the pulse 20→MA. The MB inputs to the MA gating do not affect the transfer because MB is cleared at the end of the preceeding cycle. The internal processor does not control the transfer of an address to MA at the beginning of a break cycle. In a data break or clockbreak, the transfer is provided by the interrupt logic (a above). In a program break access is always made to address O, so no actual address transfer is necessary. Since MA is previously cleared, the absence of an address transfer is equivalent to the transfer of address 0.

c MEMORY ADDRESS DECODERS - Memory addresses in MA are decoded to select a single core register from the total number of registers available in the computer memory. With an 8K memory, MA_5 is decoded directly by memory control to select a single memory module for use during the cycle (paragraph 8-4a). For either a 4K or an 8K memory, MA_{6-17} contains a 12-bit address, specifying a single location in one memory module. With a 1K memory, MA_{8-17} contains a 10-bit address specifying a single location in the 1K memory module.

That part of the address in MA which specifies a single location in one memory module is decoded to select X and Y windings corresponding to the addressed memory location. The decoding is accomplished in two stages: first, the 10-bit or 12-bit address in MA is decoded by four type 4150 binary-to-octal decoders, MADA through MADD (figure 8-1). Second stage decoding is accomplished by applying the decoder outputs (including four asserted outputs) to the read/write switches in the memory module. The connections between MA and the decoders, and the meaning of the decoder output

depend upon whether a location is being addressed in a 4K module or a 1K module.

(1) Twelve-bit Address Decoding - In the 4K memory module, the core registers are arranged in a 64-by-64 matrix (64 x 64 = 4096). A single core register is selected by selecting one out of 64 X windings and one out of 64 Y windings. The selected register is located at the intersection of the selected X and Y windings (paragraph 8-4b).

To select one X winding and one Y winding, the 12-bit address in MA is divided into two 6-bit portions. The six-digit binary number in MA_{6-11} is decoded into a two-digit octal number by MADA and MADB. Similarly, the six-digit binary number in MA_{12-17} is decoded into a two-digit octal number by MADC and MADD. Each of the four decoders receives outputs from three bits of MA and asserts one of eight output levels. The octal output level asserted by a given decoder corresponds to the binary contents of the three associated MA bits.

The four decoders have a total of 32 outputs. Of these 32 outputs, four outputs (one from each decoder) are asserted. The asserted outputs from MADA and MADB address a single Y winding from the 64 Y windings in the core bank. Similarly, the asserted outputs from MADC and MADD address a single X winding from the 64 X windings in the core bank. Selection of the appropriate X and Y windings, addressed from the memory address decoders, is performed by the read/write switches in the memory module (paragraph 8-4c). In an 8K memory system, the outputs of the memory address decoders are applied to both memory modules.

(2) Ten-bit Address Decoding - In the 1K memory module, the core registers are arranged in a 32-by-32 matrix (32 x 32 = 1024). A single core register is selected by selecting one out of 32 X windings and one out of 32 Y windings. The selected register is located at the intersection of the selected X and Y windings (paragraph 8-4b).

To select one X winding and one Y winding, the ten-bit address in MA is divided into two 5-bit portions. The five-digit binary number in MA_{8-12} is decoded into a two-digit octal number by MADA and MADB. Similarly, the five-digit binary in MA_{13-17} is decoded into a two-digit octal number by MADC and MADD.

Decoders B and D each receive outputs from three bits of MA (MA_{10-12} and MA_{15-17}) and assert one of eight output levels. The octal output levels asserted by a given decoder respond to the binary contents of the three associated MA bits. The other two decoders, A and C, receive outputs from only two bits of MA_{8-9} and MA_{12-13} respectively) and thus used as binary-to-quarternary decoders. This is done by grounding inputs E and F of these two decoders so that only output 0, 1, 2 or 3 can be asserted. In this manner, the contents of two MA bits are decoded into octal, but 3 is the largest octal digit that can result. The entire ten-bit address is therefore decoded into a pair of two-digit octal numbers. Each number can range from 00 to 37.

The four decoders therefore have a total of 24 outputs. Of these 24 outputs, four outputs (one from each decoder) are asserted.

The asserted outputs from MADA and MADB address a single Y winding from the 32 Y windings in the core bank. Similarly, the asserted outputs from MADC and MADD address a single X winding from the 32 X windings in the core bank. Selection of the appropriate X and Y windings addressed from the memory address decoders is performed by the read/write switches in the memory module (paragraph 8-4c).

8-3 MEMORY DATA TRANSFERS

The 18-bit memory buffer is the only register that functions in all four sections of the computer logic: control, arithmetic, in-out and memory. Although instruction codes are decoded from the instruction register, all other instruction or control information is utilized directly from MB. In memory reference instructions, only the indirect address bit provides control information, but in the augmented instructions, all bits provide control information.

In most cases, single bits of MB gate specific operations; but in the addressing of in-out devices, MB_{6-11} is decoded to provide octal information (paragraph 9-2a). The MB register also functions as an element of the arithmetic unit in arithmetic and logical instructions. In most such instructions, MB holds the operand and the MB outputs provide the necessary levels to the arithmetic and logical gating of the accumulator. However, all indexing operations are

performed directly in MB.

In data interruptions, MB serves as an in-out register, bypassing AC. The outputs of MB are available directly to the data-out lines, and information can be transferred directly into MB through the data-in lines. As an element of the memory system, MB serves as the buffer between the memory module and the rest of the computer. All transfers of information between the internal processor and core memory must be made through the memory buffer.

a MEMORY BUFFER - The 18-bit memory buffer is shown in Figure 8-2. This register is composed of type 4204 dual flip-flops that are connected in the carry configuration. This type of connection allows indexing operations to be performed directly in MB rather than requiring transfers to AC.

During every memory cycle, a full-length computer word is read from or written into memory through the memory buffer. At the beginning of every cycle, MB is cleared by pulsing the direct clear inputs to all the flip-flops in the register. In most instructions, a word is read from the addressed memory location, and that same word is written back into memory while it is being used for the execution of the instruction. Information read from the cores by the memory strobe (paragraph 8-4e) is transferred from the sense amplifiers into the memory buffer through the Cannon connector shown below the register. The gating for this transfer is done directly in the sense amplifiers by the strobe. Information is loaded into MB as single-bit pulse inputs, each of which sets a corresponding bit of the register.

During the second half of the memory cycle, the word contained in MB is written back into the same memory core register from which it came (paragraph 8-4f). At the same time that the word in MB is being written back into the addressed core register, it is also used in MB by the rest of the computer. During a fetch cycle, the instruction code is transferred from MB to IR. Following both fetch cycles and defer cycles, the address portion of the word is transferred from MB either to MA or PC. In execute cycles, the word in MB is available to the transfer, logical and arithmetic gating of the accumulator. The word in MB can thus be used for all instruction operations. However, during indexing operations, the number in MB is indexed by the MB +1 pulse before being written back into memory. Therefore, the number written into

memory during the cycle is 1 greater than the number read out at the beginning of the cycle.

In those instructions for which new information is deposited in memory, the strobe is disabled so that the memory register is cleared, but no information is transferred into MB from the core bank. If information is transferred into MB from some other part of the computer, the new information is then written into the vacated core register in place of the old. If no new information is made available from MB then nothing is written back into the core register, and it is left clear.

Information may be transferred into MB from either the accumulator or the program counter. Both transfers are 1 transfers requiring a prior clear, but MB is cleared at the beginning of every memory cycle. Whenever the address of an interrupted program is deposited in memory from the program counter, the state of the link is also preserved by transferring the contents of L into MB_0. In data breaks, information may be transferred into MB from the data-in lines (through column 4 of the taper pin block shown below the register). The information transfer is made on the pulse DB11 →MB, which is equivalent to the INFO→MB pulse from the data interrupt logic (paragraph 9-2d).

If the data break access is being made for the retrieval of the information from memory, both the 0 and 1 outputs of the MB flip-flops are available to the data-out lines through the connectors shown above the register.

b DATA TRANSFER LOGIC - The logic that governs the transfer of information to MB from other registers in the internal processor is shown in the lower left of Figure 8-2. At the initiation of operations from the console, MB is cleared by BEGIN. The register is then cleared at the beginning of every memory cycle by T1. However, in Call Subroutine, MB is cleared at the end of the fetch cycle so that the state of MB cannot affect the transfer 20→MA at the beginning of the next cycle (paragraph 8-2b).

A word is transferred from AC to MB at T3 in the execute cycle of the instruction Deposit Accumulator. Whenever the program sequence is interrupted and an eventual return to the interrupted program is desired, the current program address is stored in

memory. The address is transferred from PC to MB at T3 in a program break cycle, and in the execute cycle of Jump to Subroutine or Call Subroutine.

The transfer of an address from PC to MB is also made at SP3 in any examine or deposit operation. However, this transfer is not made for the deposit of information in memory. In all examine and deposit console operations, the one memory cycle that is performed is performed as an execute cycle. Thus the transfer of PC to MB at SP3 is made merely to utilize the subsequent normal transfer of MB to MA at T1 of every execute cycle (paragraph 8-2b).

c INDEX LOGIC - Three types of indexing operations are provided in PDP-4. The programmer may use the instruction Index and Skip on Zero to count program loops. The programmer may also index addresses in order to perform an instruction or set of instructions on a whole sequence of operands. Address indexing is combined with indirect addressing. Automatic indexing is performed in clock breaks to keep track of real time.

The logic that governs the incrementing of the memory buffer is shown in the lower left of Figure 8-2. For counting program loops, the line MB+1 is pulsed by T4 in the execute cycle of an isz instruction (D1). The network shown in D3 provides address indexing in defer cycles. During any defer cycle, if the indirect address is between 10 and 17, T4 pulses MB+1. With this procedure, each time a deferred address is retrieved from a memory index register (locations 10 to 17), the deferred address is incremented before it is written back into memory. The next time the address is retrieved, it addresses the next consecutive memory location. In each clockbreak, the number contained in memory location 7 is indexed (paragraph 9-2d). When this number is indexed to zero, the clockflag is set.

8-4 CORE MEMORY LOGIC

The two PDP-4 memory modules, 4K and 1K, are shown in Figures 8-3, 8-4 and 8-5. Both modules, are composed of a coincident current core bank, and associated timing, driving and sensing logic. The core bank of the 4K module has a capacity of 4096 eighteen-bit words; the core bank of the 1K module has a capacity of 1024 eighteen-bit words.

Since both modules contain the same number of core planes (that is, the core registers in both modules are 18 bits in length) the timing, write inhibit driving, and read sensing logic for both modules is identical (Figure 8-4). However, the two modules contain a different number of core registers and hence require different numbers of read/write switches to select the X and Y windings. The X and Y selection for the 4K memory module is shown in Figure 8-3; the X and Y selection for the 1K memory module is shown in Figure 8-5.

The description of the core memory logic given in this paragraph is for the 4K memory. Wherever the 1K memory differs from the 4K memory, the differences are explicitly mentioned in the text. The memory module furnished with the standard computer is located at the top of bay 2. If a second 4K memory is added to the system, it is mounted in an extra bay. Internal processor control over the memory module is described in a below. The memory module logic is described in b through f below.

a MEMORY CONTROL- The internal processor controls the operation of the memory module through the control signals shown in Figure 8-1D6. Three of the signals are pulses that control the timing of operations within the core memory. The fourth signal is a level which disables the memory strobe if the information being read from the addressed core register is not wanted by the computer.

The memory clear pulse (which clears the memory control flip-flops in preparation for each memory cycle) is produced initially by the power clear, and subsequently by the final time pulse of every memory cycle. By shifting control information through the four control flip-flops in the memory module, the memory control pulses and the memory inhibit pulse together time the memory cycle operations. The memory control pulses are all applied to the same line, since flip-flops R, RS, W and I are included in a single shift register plug-in unit with all pulses applied to the same input pin. Because flip-flop I is set out of sequence in the memory timing shift register, the inhibit pulse is generated separately from the memory control pulses.

There are four memory control pulses. The first three control pulses are produced at T2, at 0.7 microsecond after T2, and at T4. The memory inhibit pulse is then produced at T5 and the final (fourth) memory control pulse follows the inhibit pulse by 0.2 microsecond.

The memory read operation destroys the contents of the addressed memory register. While the read is taking place, information from the core register is transferred to the memory buffer by the strobe. In any cycles during which new information is being deposited in memory, the strobe is disabled. The addressed core register is then cleared, but no information is loaded into MB. The memory strobe is also disabled during the execute cycle of any instruction that deposits information in memory (IA0). In a program break, the strobe is disabled so that the current program address may be deposited in memory. The strobe is also disabled during a data break, if the break is being utilized for data input.

If the memory system is expanded to two 4K memory modules, the plug-in units shown in the lower right of Figure 8-1 are added to the internal processor. These units duplicate the memory control and memory inhibit pulses. With two memory modules, the memory strobe disable and memory clear signals are applied to both modules. However, the memory control and memory inhibit pulses are applied only to the module selected by MA_5. If MA_5 is 0, pulses from 1A25 are applied to the first memory module, but if MA_5 is 1, pulses from 1A19 are applied to the second memory module. If the computer contains only one memory module, the MA_5^0 input in D6 is still connected to the 1 output of the MA_5 plug-in unit. However, the 1 output terminal of that plug-in unit is tied to ground.

b CORE BANK - The memory core bank is composed of 18 core planes. In the 4K memory module, each plane contains 4096 ferrite cores (64 rows x 64 columns); while in the 1K memory module, each plane contains 1024 ferrite cores (32 rows x 32 columns). Every memory core is threaded by four windings; X and Y selection windings, an inhibit winding, and a sense winding. The following description applies directly to the core bank for the 4K memory module. (Whenever the number of elements differs for the 1K memory, the appropriate number is written in parentheses following the number that applies to the 4K memory.)

The 64 (32) X and 64 (32) Y windings each thread a row or column of 64 (32) cores in each of the 18 core planes. A single X or Y winding continues from one core plane to the next, threading the same row or column in every one of the 18 planes. A single X winding and a single Y winding intersect at a single memory location

containing an 18-bit core register. During each memory cycle information is read from or written into the single addressed core register. This addressed register is selected from among the 4096 (1024) registers in the core bank by selecting the single X winding and the single Y winding that intersect at the corresponding memory location.

There are 18 inhibit windings and 18 sense windings; one inhibit winding and one sense winding for each core plane. Both the inhibit windings and the sense windings thread all 4096 (1024) cores in the plane with which they are used. Individual cores within the addressed register are selected by the sense windings during reading, and by the inhibit windings during writing.

> NOTE: The core bank actually includes an extra core plane which is completely wired in. There are therefore 19 planes, and 19 inhibit and sense windings. The extra 19th plane is not ordinarily used, but is provided in case it is wanted for some special application. The following discussion refers only to the 18 core planes that are ordinarily used.

c X AND Y SELECTION - Each of the 4096 locations in the 4K memory core bank is specified by a particular 12-bit address in the memory address register. The memory module selection logic selects one of the 64 X windings and one of the 64 Y windings, corresponding to the contents of MA. For the 1K memory module, each of the 1024 locations in the core bank is specified by a particular 10-bit address in MA. The memory module selection logic then selects one of the 32 X windings and one of the 32 Y windings according to the contents of MA. In either case, the two selected windings intersect at the same relative location on each of the 18 core planes; the 18 cores located at these intersection points make up the addressed memory register.

The X and Y selection logic for the 4K memory is shown in Figure 8-3. The X and Y selection logic for the 1K memory is shown in Figure 8-5. The layout of the two drawings is similar. They differ only in the number of logic elements shown. The X selection logic is shown in the upper half of both Figures; the Y logic in the lower half. The outputs of the memory address decoders are applied to the switching logic through the inverters shown below the switches. The outputs of the switches are applied to the core bank through the memory stack sockets shown above the switches. The following description applies directly to the X and Y selection for the 4K memory. (Whenever the

number of elements differs for the 1K memory, the appropriate number is written in parentheses following the number that applies to the 4K memory.)

The 32 (24) outputs from the memory address decoders (paragraph 8-2c) are applied to the inverters shown in B and D in the figure (Figure 8-3 for the 4K memory, Figure 8-5 for the 1K memory). From the inverters, the 16 (12) X-selection levels are applied to the Type 1972 read/write switches shown at the top of the figure. Similarly, the 16 (12) Y-selection levels are applied to the read/write switches shown at the bottom of the figure. Only four of these 32 (24) selection levels are asserted during any given memory cycle; two Y levels from MADA and MADB and two X levels from MADC and MADD.

The two asserted Y levels enable one of 64 (32) Y read/write switches, and thereby permit the associated Y winding to be pulsed by the output of the read or write bus. Similarly, the two asserted X levels enable one of the 64 (32) X read/write switches, and thereby permit the associated X winding to be pulsed by the output of the read or write bus. In this way, the two sets of read/write switches select one X winding and one Y winding, and thereby select the addressed core register for reading or writing.

A Type 1972 plug-in unit includes four read/write switches. A detailed circuit description of the read/write switches is included in paragraph 10-7c. There are 64 (32) switches in each of the two sets; both sets are identical in function. Each switch is controlled by an AND-gate input. Each AND gate receives one of the eight (four) more-significant-digit selection levels and one of the eight less-significant-digit selection levels. Only the AND gates that receive two asserted selection levels are enabled. During any memory access, these AND gates correspond to the single X and Y windings designated by the contents of MA.

When both inputs to a read/write switch AND gate are at ground, the switch closes, completing the current path between one end of the associated winding and the read bus. Since the other end of the winding is permanently connected to the write bus, the read/write switch permits application of the bi-polar core-drive pulses to the two selected windings. (One polarity corresponds to a read pulse; the other polarity corresponds to a write pulse).

The Type 1976 resistor cards located between the read/write switches and the core bank provide the necessary loading to produce a core-drive current of appropriate magnitude. Nominal value of the half-read and half-write currents is 190 ma. A single half-current is not sufficient to change the state of a core. However, the intersection of two half currents at the cores of the addressed register is sufficient to switch these cores (see f and g below).

d MEMORY TIMING FUNCTIONS - The timing for the memory cycle read and write operations is controlled by the shift register containing flip-flops R, RS, W and I (Figure 8-4, B1 and B2). This shift register is in turn controlled by pulses from memory control (a above). During a memory cycle, timing control information is shifted through the shift register by the memory control pulses. The entire register is cleared at the end of each cycle by the memory clear pulse (T7). This prepares the register for the next cycle.

The control data shifted through the register is self-contained. No external gating levels are applied to the register. The register starts the memory cycle in a cleared state. Because the outputs of the second stage (RS) are applied to the opposite input gates of the first stage (R), the first shift pulse following the memory clear automatically sets R. At the second shift, R^1 sets RS, asserting the condition RS^1. This causes the third shift to set W and clear R. The condition R^0 in turn clears RS at the fourth pulse. Thus a 0 is shifted through the first three stages of the register two pulses behind the 1.

The final stage of the shift register (I) is set early by the inhibit pulse (T5). This grounds the 0 output of flip-flop I. Although the fourth shift clears RS, this pulse does not affect I.

The four timing functions, read, write, inhibit, and strobe, cause the read and write operations to be performed. The read, write, inhibit functions are levels; the strobe function is a pulse. State changes in the ferrite cores of the memory core bank occur much more slowly than changes of state in the computer logic elements. The core-driving pulses are therefore of relatively long duration (approximately two microseconds). The duration of these pulses is much longer than the duration of computer

logic pulses. The core driving pulses are in fact produced from computer logic levels.

The memory timing functions are generated from the shift register outputs (A1 to A3, C2). The logical conditions for these functions are as follows:

Read:	R = 1
Strobe:	1→RS
Inhibit:	I = 1
Write:	(RS = 0).(W = 1)

The strobe is produced by the fall in the 1 output of RS, when RS is set (C2). However, if the memory strobe disable level is asserted, the strobe is not produced. This prevents information read from the core register from being transferred into MB. Thus the read operation merely clears the core register so that new information can be read into it during the same cycle.

Operation of the memory timing network is summarized in Table 8-1 below. This table shows the states of the four shift flip-flops after each time pulse. The shaded columns at the right of the table show the duration of the timing functions. Note, however, that these functions are shown relative to the irregularly spaced time pulses. Therefore, the length of each shaded column is not necessarily proportional to the actual duration of the associated pulse. The true duration of these functions is shown in the diagram of the memory cycle (Figure 4-2).

TABLE 8-1

MEMORY TIMING

Time	Timing Flip-flops				Timing Functions			
	R	RS	W	I	Read	Strobe	Inhibit	Write
Initial State	0	0	0	0				
T2	1	0	0	0				
T2 + 0.7 μs.	1	1	0	0				
T4	0	1	1	0				
T5 (Inhibit)	0	1	1	1				
T5 + 0.2 μs.	0	0	1	1				
T7 (Clear)	0	0	0	0				

e READ AND WRITE DRIVERS - The Type 1973 current drivers in the memory module provide the read and write currents applied to the core bank windings (Figure 8-4D4). These two currents are identical in magnitude, but of opposite polarity. A detailed description of the Type 1973 current driver is included in paragraph 10-7d.

When the read driver is enabled by the -3 vdc read level, a core drive read current is applied to the selected X and Y windings. This read current flows through the following path: terminal V of the read driver (-13 vdc), the read bus, the two closed read/write switches (these two switches provide parallel paths, one for X and one for Y), the selected X winding and Y winding corresponding to the two closed read/write switches, the write bus, and terminal V of the write driver (-3 vdc).

Conversely, when the write driver is enabled by the -3 vdc write level, current is applied to the same X and Y windings, but in the opposite direction. Terminal V of the write driver is then at -13 vdc, and terminal V of the read driver is then at -13 vdc. The current path is exactly the same for both the read pulse and the write pulse. However, during the read pulse, the voltage at the read bus is 10 volts more negative than that at the write bus, while during the write pulse, the write bus is more negative. The Type 735 memory power supply furnishes the -3 vdc and -13 vdc used by the Type 1973 drivers. Circuit description of this power supply is treated in paragraph 10-11c. A separate power supply is required for each memory module because of possible temperature-induced variations in the core characteristics.

f READ SENSING - When a memory core is magnetized in the 1 direction, it is said to contain a 1. When magnetized in the opposite direction, it is said to contain a 0. During the read operation, a full-read current (ie, two half-read currents, one on the selected X winding, and one on the selected Y winding) is applied to magnetize the memory cores in the addressed memory register. The full read current tends to magnetize the memory cores in the 0 direction, and hence has no effect on those cores of the addressed register which were initially in the 0 state.

However, when the full-read current is applied to a core containing a 1, the core magnetization changes polarity, and the core is switched from the 1 state to the 0 state. This change of state induces an output voltage on the sense winding that threads the core. (The same sense winding threads all 4096 (1024) cores in the plane containing the

affected core). The two ends of this sense winding are connected to the two input terminals of a Type 1538 or Type 1540 sense amplifier. Circuit descriptions of these sense amplifiers are provided in paragraphs 10-7a and b respectively.

There are 18 sense amplifiers used in the memory, one for each of the 18 core planes (Figure 8-4, C2 to C7). The sense amplifiers are differential amplifiers which reject common-mode signals but amplify difference signals. This tends to prevent noise voltages on the sense windings (from half-selected cores, etc.) from being erroneously sensed as valid 1 output signals. The actual output signal from a 1 state core which has been switched to the 0 state by a full-read applies a difference signal of approximately 60 millivolts to the sense amplifier inputs.

The sense amplifiers sample the core outputs by means of a 70-nanosecond strobe pulse. This strobe is regulated to occur approximately 0.7 microsecond after the beginning of the read level. At this time the sense winding is likely to produce the best signal-to-noise ratio. If the addressed core in a given core plane contains a 1, the read pulse causes it to apply a difference signal output to the sense winding.

The strobe samples this output signal, and causes the sense amplifier to generate a standard logic pulse output (provided that the core output exceeds the required 1-signal threshold at the time of the strobe). This logic pulse output sets the corresponding flip-flop of the memory buffer register.

The transfer of information from the memory to the memory buffer is a 1 transfer. The memory buffer is cleared prior to the read-out from the addressed core register. At read-out, the sense amplifiers corresponding to the 1-state cores of the addressed register set the corresponding bits of MB.

g WRITE INHIBIT DRIVING - The read operation is destructive; read-out leaves all cores of the addressed register in the 0 state. During writing, a full-write current (ie, two half-write currents, one on the selected X winding, and one on the selected Y winding) is applied to all 18 cores in the addressed memory register. The full-write current tends to magnetize the memory cores in the 1 direction. Cores that receive only a full-write current are switched from the 0 state to the 1 state of magnetization.

To write a word from MB into the addressed core register, it is necessary to prevent

(or inhibit) this change of state for just those cores of the addressed register that correspond to 0 bits in MB. This is done by applying an inhibit current of opposite polarity (the equivalent of a half-read current) to only those cores which are to remain in the 0 state. Net current to these cores is then equivalent to only one half-write current. Because this current is not sufficient to drive the cores beyond the "knee" of the hysteresis loop, they do not change state, but remain in the 0 state.

The inhibit currents which prevent the writing of 1s into the 0 bits of the addressed register are applied to the core planes through the 18 inhibit windings, each of which threads all cores in a single core plane. Each inhibit winding therefore threads one of the 18 bits in the addressed register. The Type 1982 inhibit drivers (Figure 8-4, A4 to A7) determine which of the 18 inhibit windings are to be pulsed. Circuit description of the 1982 inhibit drivers is treated in paragraph 10-7g.

The inhibit drivers are switching circuits which are enabled by two ANDed inputs. The inhibit level (d above) is ANDed with the 0 signals from the bits of MB, enabling those inhibit drivers corresponding to MB bits that contain 0. This allows inhibit current to flow through the associated inhibit windings. Inhibit current flows from the inhibit common line (always at -3 vdc) through the enabled inhibit drivers to the inhibit reference line (always at -13 vdc).

While the inhibit level is asserted, current paths are completed from the common line through the enabled drivers and the associated inhibit windings to the reference line. The resulting inhibit currents cause the appropriate bits of the addressed core register to remain in the 0 state.

CHAPTER 9

INPUT-OUTPUT SYSTEM

9-1 GENERAL

The input-output system of the standard PDP-4 computer contains a single input device, a photoelectric paper tape reader. The reader control unit is controlled directly by the in-out pulses from the internal processor.

Other in-out devices may readily be added to the system by installing a type 25 real time option. When this option is installed, the control units for the reader and all other in-out devices are governed through the device selector. This selector decodes the device code portion of the iot instruction word (bits 6 through 11) and translates the in-out pulses into iot pulses for the specified device.

The present chapter includes detailed descriptions of the real time control and the control units for three in-out devices. These devices are the standard photoelectric tape reader and two options, the paper tape punch and the keyboard/printer. The equipment described in this chapter is shown in seven logic drawings, Figures 9-1 through 9-7. For information on the use and organization of these drawings, see paragraph 4-9.

9-2 REAL TIME OPTION, TYPE 25

The real time option governs the control units of the reader and all optional in-out devices. The device selector decodes the device code section of an iot instruction word, and changes the in-out pulses into iot pulses for the appropriate control unit (including the interrupt control). Information is made available to output devices through the information distributor, while information is brought into the computer from input devices through the information collector. The type 25 option also includes the interrupt logic and the in-out skip logic.

a DEVICE SELECTION - The device selector is shown in Figure 9-1. The inputs to the selector (at the left) are the in-out pulses (PIO1, 2 and 4) and the outputs of bits 6 to 11 of memory buffer.

In an in-out transfer instruction, the individual in-out device is addressed by bits 6 to 11 of the iot instruction word. The device code is decoded by the type 4605 pulse amplifier modules. The logical configuration of this module is shown in the lower right of the figure. The diode decoder inputs in the module are prewired to respond to a particular configuration of MB_{6-11}, ie to a particular device code. When the diode inputs to a given 4605 plug-in unit are enabled, any in-out pulses generated by the instruction word are switched onto the iot lines for the corresponding device.

For example, the first type 4605 unit at the left (2F06) is wired for the code 00 to control the interrupt logic. In this way, whenever an instruction of the form 7400XX appears in the program, the in-out pulses generated in the internal processor are applied to the interrupt logic as iot pulses. The in-out pulses are provided by in-out transfer control according to the configuration of bits 15 to 17 of the instruction word (paragraph 6-4c).

The number of type 4605 pulse amplifiers included in the device selector depends upon the number of in-out devices driven by the computer. More options may be readily controlled from the computer merely by adding more type 4605 units to the selector.

b INFORMATION DISTRIBUTION - Information is distributed to the various output devices through the distributor shown in Figure 9-2. The 1 outputs of the accumulator flip-flops are buffered by type 1690 bus drivers and made available to the output devices through taper pin panels. The contents of AC_{10-17} are made available to the punch buffer and the contents of AC_{13-17} are made available to the teleprinter buffer (LUO) at the taper pin positions shown in the figure. Connections for other options are also shown, while tie points for further equipment may be made as desired.

Both outputs of MB_{12} are also made available to in-out devices through the information distributor. Besides the device code in bits 6 to 11, bit 12 of an iot instruction word may also be used for control purposes. For example, in controlling the reader, bit 12 specifies whether the tape is to be read in alphanumeric mode or in binary mode.

The information distribution capacity of the real time option may be increased as desired merely by adding more distributors in series with the one shown.

c INFORMATION COLLECTION - Information from input devices is transferred into the

accumulator through the information collector, IC (Figure 9-3). This collector includes 18 pulse amplifiers and associated input gating. The output of each pulse amplifier is applied to the set input gate of the corresponding bit of the accumulator (paragraph 7-2a).

The 18 bits of the reader buffer are connected to the first row of gates in the collector. The five bits of the incoming line unit are connected to gates 13 to 17 in the second row. Information from these two buffers is loaded into AC through the collector on iot 2 of the corresponding iot instruction. Row 3 of the collector is used for the instruction In-out Read Status, with the flags for the various devices connected to the IC gates as shown. Tape unit status information is loaded into AC through the left half of row 2.

The magnetic tape control and the card reader are also connected to the IC gates as shown; additional input devices may be connected as desired. The information collection capacity of the real time option can be increased merely by adding more information collectors in series with the one shown.

d INTERRUPT LOGIC - The logic that governs interruptions in the normal program sequence is shown in Figure 9-4. The three types of interruptions, data, clock and program, are synchronized by the flip-flops shown across the top of the figure. The flip-flops are cleared initially by BEGIN and synchronization occurs at T5 in the memory cycle. Whenever any of the synchronizing flip-flops is set, the break request level is asserted (B5). This causes the computer to enter the break state at the end of the current instruction (paragraph 6-3b).

The data interrupt logic is shown at the left in Figure 9-4. The control unit of the high-speed device that utilizes the data interrupt logic must provide two levels, one which requests a data break and one which specifies the direction of information flow. When a data request is made, T5 sets the synchronizing flip-flop. Then the computer asserts the data break level when it enters the break state. The data break level causes the program to pause for one memory cycle while the high-speed device makes direct access to memory. At T1, an address is transferred into the memory address register (paragraph 8-2a) The ADDRESS $\rightarrow$MA transfer pulse also signals the device that access to memory has been granted. If the break is for data output, the word read from memory by the strobe is available to the device from the memory buffer. However, if the level DATA IN is asserted, the break is used to deposit information in memory. DATA IN disables the memory strobe

(paragraph 8-4a) and transfers information from the device into MB at T3 (paragraph 8-3a).

The programmer controls the clock interrupt logic (left center, Figure 904) by programming PIO4 for the interrupt logic (device code 00). Pulse IOT0004 clears the clock flag and adjusts the state of the clock enable flip-flop according to bit 12 of the iot instruction word. The 60-cycle clock is produced through a pulse generator from a filament transformer mounted on the 813 power control panel. While the clock is enabled, each clock pulse sets the clock count request flip-flop. Whenever this flip-flop is set, T5 sets the synchronizing flip-flop, causing the computer to enter the break state. This break cycle is a clock break, provided no data break is being requested simultaneously.

A clock interruption merely causes the program to pause for one memory cycle while the number contained in memory location 7 is indexed. If this number becomes zero as a result of the indexing operation, the clock flag is set, indicating that the clock count has been completed. In the clock break cycle, T1 produces the pulse 7⟶MA (D4). This pulse loads address 7 directly into MA (paragraph 8-2a) and clears the clock count request flip-flop. After the contents of location 7 are retrieved from memory, the index logic increments the word in MB by 1 (paragraph 8-3c). If the carry initiated by MB+1 ripples through the entire register, MB_0 changes state from 1 to 0, setting the clock flag. This is conditioned by the 0 state of the clock count request flip-flop to prevent the initial clearing of MB at the beginning of the break cycle from setting the clock flag.

The program interrupt logic is shown in the upper right of Figure 9-4. Program control over program interruptions is exercised through PIO2 of the interrupt iot. Pulse IOT0002 adjusts the state of the program enable flip-flop according to bit 12 of the iot instruction word. Eleven device flags may be connected to the program request logic (A7). Any of these device flags may make a program request provided program breaks are allowed, and provided the computer is not currently in a break cycle. When a program request is made, T5 sets the synchronizing flip-flop (A4) causing the computer to enter the break state at the end of the current instruction (B5). If no data break or clock break is being requested simultaneously, the break cycle is utilized for a program break.

This type of interruption actually ends the current program sequence by transferring program control to a subroutine. The computer saves information necessary for a subsequent return

to the interrupted program by depositing the contents of the program counter and the link in memory location 0. The program then executes the routine that starts with the instruction in memory location 1.

Operations necessary for the program break cycle are conditioned by the level PROG·B (see paragraphs 8-4a, 8-3b and 6-5b, c). This level also prevents further program interruptions of the break routine by causing T5 to clear the program enable flip-flop.

e IN-OUT SKIP LOGIC - The programmer may check the status of any device by conditioning a skip on the appropriate device flag. To address the device flag, the program uses PIO1 in the in-out transfer instruction for the particular device (lower right, Figure 9-4). The device flag is addressed through the device selector (a above). For example, if the punch flag is on, PIO1 in a punch iot (IOT0201) generates IO SKIP. This pulse increments the program counter one extra step (paragraph 6-5b), causing the computer to skip the next instruction in normal sequence.

9-3 READER CONTROL

The control unit for the photoelectric paper tape reader is shown in Figure 9-5. The 18-bit reader buffer is at the top of the figure. The control logic and control flip-flops are at the lower left; and at the lower right is a block diagram of the reader control unit.

a READER BUFFER - The 18-bit reader buffer, RB, is composed of 18 type 4218 flip-flops. Each flip-flop has a direct clear input and gated 0 and 1 inputs. The input gating to the flip-flops is provided by capacitor-diode gates contained within the flip-flop plug-in unit.

When information is read, the presence of a hole in the tape is indicated by a -3 vdc level. Consequently, the ground level utilized by the input gates indicates the absence of a hole. To compensate for this polarity, the input signals are applied directly to the clear input gates, and through inverters to the set input gates, of the reader buffer bits.

The reader can read the tape in either of two modes, binary or alphanumeric. If the computer is reading in alphanumeric mode, only a single line on the tape is read, and the entire line is loaded into reader buffer bits 10 through 17. If the reader is operating in binary mode, holes 7 and 8 on the tape are ignored, but three lines are read from the tape. In binary mode, data from holes 6 through 1 is loaded into RB_{12-17}. The contents of

RB_{12-17} are then shifted into RB_{6-11}, and the data from holes 6 through 1 of the second line on the tape are loaded into RB_{12-17}. The contents of the buffer are then again shifted left six places, and the third line from the tape is read into RB_{12-17}.

The read shift pulse, RD SHIFT, is applied to both the set and clear gates of all bits in the buffer. This single pulse accomplishes both the shifting and the loading operations. From RB_0 to RB_{11}, the RD SHIFT pulse to each bit is gated by levels from the bit six places to the right. The read shift transfers the contents of any six bits of RB into the next more significant six bits. However, the gating levels for the input gates of RB bits 12 through 17 are the input signals from holes 6 through 1 on the tape. Thus RD SHIFT loads RB_{12-17} with information from holes 6 through 1 of the tape. In binary mode, an entire 18-bit computer word is assembled in the buffer by three read shifts.

When reading in binary mode, each read shift transfers the contents of RB_{16} and RB_{17} into RB_{11}. However, in alphanumeric mode, RD SHIFT instead loads RB_{10} and RB_{11} with information from holes 8 and 7 on the tape.

b CONTROL LOGIC - The logic nets and control flip-flops of the reader control unit are shown at the lower left of Figure 9-5. The five reader control flip-flops are the 2-bit read counter, RD_1 and RD_2; the run flip-flop, RD RUN; the reader flag, RD FLAG; and the read mode flip-flop, RD MODE.

When the run flip-flop is set, the reader clutch is engaged through the network shown in B4, moving the tape. When RD RUN is cleared, the clutch is disengaged and the brake is engaged, stopping the tape. The read mode flip-flop controls the acceptance of information from the tape. If RD MODE is in the RD ALPHA state, the control unit accepts the first line encountered on the tape and information from all eight holes is loaded into the reader buffer. If RD MODE is in the RD BIN state, the reader accepts information only from lines in which hole 8 is punched. In this case, information from holes 1 through 6 is loaded into the buffer while holes 7 and 8 are ignored. The read counter controls the execution of a reader instruction by counting the number of lines read from the tape.

The in-out pulse that initiates operations in the reader control unit is PIO4 in the standard machine, or IOT0104 if the type 25 real time option is used. The difference is only one of nomenclature; the two pulses have exactly the same effect. Similarly, the in-out pulse

PIO2, which clears the reader flag, is relabeled IOT0102 if the type 25 option is used.

Pulse PIO4 sets the reader run flip-flop but clears the read counter, the reader flag, and the entire reader buffer. If MB_{12} is 0, PIO4 puts RD ALPHA into RD MODE, while if MB_{12} is 1, PIO4 instead puts RD BIN into RD MODE.

The run flip-flop engages the clutch in the reader, starting the tape. When the feed hole on the tape is encountered, pulse generator 1K14 (B4) produces the RD STROBE pulse. If RD RUN is 1, the read strobe produces the read shift (C2), provided either the tape is being read in alphanumeric mode or hole 8 on the tape is punched. When reading in binary mode, the reader runs until three lines, in which hole 8 is punched, have been read from the tape into the buffer, regardless of how many characters are encountered.

In a binary mode instruction MB_{12} is 1, so PIO4 asserts RD BIN. This enables the 0-input shift gates to bits RB_{10} and RB_{11} -- that is, it applies the 0 outputs of $RB_{16,\ 17}$ to the 0 input gates of $RB_{10,11}$ (D3, B5). The first read shift loads the information contained in holes 6 through 1 into RB bits 12 through 17, and sets RD_1. The second read shift transfers the information contained in RB_{12-17} into RB_{6-11}, simultaneously loads the information contained in holes 6 through 1 on the tape into RB_{12-17}, and sets RD_2 (without clearing RD_1). The third read shift transfers the information contained in RB_{6-17} into RB_{0-11}, simultaneously loads the information contained in holes 6 through 1 on the tape into RB_{12-17}, and sets the reader flag.

The negatively asserted 1 output of the flag is applied through a capacitor-diode gate (C3) to clear the run flip-flop. This disengages the clutch and applies the reader brake, stopping the tape. Since RD RUN is now 0, no further strobe or shift pulses are generated. Three lines of tape have been read, the buffer contains a full 18-bit computer word, and the reader flag is on, indicating that RB contains new information. When the information is retrieved by PIO2, the flag is cleared.

In an alphanumeric mode instruction MB_{12} is 0, so PIO4 asserts RD ALPHA. This disables the 0-input shift gates to RB_{10} and RB_{11} (D3, B5) preventing RD SHIFT from shifting 0s into these bits. At the same time, RD ALPHA enables the transfer into RB_{10} and RB_{11} from holes 8 and 7.

The first (and only) read shift loads information from holes 8 through 1 into RB_{10-17} and

also sets the reader flag. The 1 output of the flag falls to its negative assertion level, clearing the run flip-flop. This disengages the clutch and applies the reader brake, stopping the tape. Since RD RUN is now 0, no further strobe or shift pulses are generated. One alphanumeric character has been loaded into RB_{10-17} and the reader flag is on, indicating that RB contains unretrieved information. When the information is retrieved by PIO2, the flag is cleared.

9-4 PUNCH CONTROL, TYPE 75

The punch control unit is shown in Figure 9-6. The control unit includes an eight-bit punch buffer, PB, drivers to power the solenoids in the punch, and two control circuits. The control circuits comprise the three-state punch status device (D2, D3), and the punch synchronizing and timing logic (B2, B3). At the upper left is a block diagram of the punch control unit. The real time option supplies two iot pulses to the punch control unit. These are IOT0202, which clears the punch buffer and turns on the punch flag; and IOT0204, which loads the eight-bit buffer from AC_{10-17} (through ID) and initiates the punch cycle.

The three inverters shown at the lower left of the figure are connected as a three-state device, the punch status marker. This device has three inputs and three outputs. Pulsing any one of the inputs asserts the corresponding output, and negates the remaining two outputs. The three states of the marker are punch active, punch idle, and punch flag. The punch start pulse (IOT0204) is inverted to momentarily assert the punch active level. This level, asserted at ground, turns off both the center and left transistors. The negative output of the center and left transistors maintains conduction through the right transistor, so that the punch active level remains asserted.

In a similar manner, the punch clear pulse (IOT0202) turns on the center transistor and turns off the two end transistors, asserting the punch idle level and negating the punch active level. The punch done pulse turns on the left hand transistor, asserting the punch flag, and negating both the punch idle and the punch active levels.

As long as the punch motor is running, a synchronizing pulse is generated every 15.8 milliseconds. To punch a line on the tape, the solenoids must be energized at this synchronizing pulse, in order to avoid punching the tape while it is advancing to the next line. These SYNC PUN pulses are generated once each revolution of the punch shaft, regardless of

whether a line is currently being punched on the tape.

The punch start pulse (IOT0203) asserts the punch active line, and at the same time transfers the contents of AC_{10-17} into the buffer. The first subsequent synchronizing pulse is applied through a pulse generator to a type 4301 delay. Since asserting punch active disables punch idle and punch flag, this delay immediately asserts a five-millisecond level. This level gates the 1 outputs of the PB flip-flops through inverters into the solenoid drivers, energizing the feed-hole solenoid and those data-hole solenoids which correspond to PB bits containing 1. The feed-hole solenoid is also energized continuously whenever the tape feed button on the punch cabinet is held down. This allows the operator to punch blank tape for leaders.

At the end of the five-millisecond delay, the level output of the delay is disabled and a terminating pulse is developed at pin E. This is the punch done pulse, which puts the punch status marker into the punch idle state. The concurrent disabling of the punch active line prevents subsequent synchronizing pulses from triggering another punch cycle. At this point, a single line has been punched on the tape from the data contained in bits 10 through 17 of the accumulator, and PUNCH IDLE is asserted, indicating that the punch cycle has been completed.

After completion of the punch cycle, the first subsequent punch clear pulse (IOT0202) clears PB and switches the punch status marker from the punch idle state to the punch flag state. The transfer of information into the buffer is a 1 transfer, which means that PB must be cleared prior to the punch start pulse. The flag, when asserted, indicates that the punch control unit is ready for the initiation of another punch cycle.

9-5 KEYBOARD/PRINTER CONTROL, TYPE 65

The two control units for the Teletype Model 28 Keyboard/Printer are shown in Figure 9-7. The outgoing line unit shown at the top of the figure develops the teletype signal that controls the printer. Incoming teletype signal from the keyboard is decoded by the incoming line unit shown at the bottom of the figure. Timing signals are provided by the clock circuits shown at the left. Except for the clock, which is common to both, the two control units function independently.

Signals both to and from the keyboard/printer are in the standard five-element teletype code. An element in the code may be either a mark or a space. A mark is denoted by current flow

in the teletype line; a space is denoted by the absence of current flow. The character to be printed or the printer operation to be performed is determined by the configuration of marks and spaces which make up the five elements of the code.

The keyboard/printer also requires (and provides) two additional impulses: the start impulse and the stop impulse. The start impulse is always a space; it precedes the five code-element impulses. The stop impulse is always a mark; it follows the fifth code-element impulse. Normally the start and stop impulses are used to synchronize teletype sending and receiving equipment. Neither the start nor the stop impulse conveys information; but both these impulses must nevertheless be provided to the printer by the outgoing line unit. The incoming line unit must also accept both the start and stop impulses as part of the signal from the keyboard.

The keyboard/printer operates at a speed of ten characters per second. The printing rate determines the duration of each impulse in the composite teletype signal. The start impulse and each of the five code element impulses are of equal duration: 13.3 milliseconds. The duration of the stop impulse has no upper limit, but must not be less than 18 milliseconds.

All printer operations are controlled by the printer selector magnets shown in A8. As long as current is maintained through the printer selector magnets, the printer is idle. This situation corresponds to a teletype stop impulse of indefinite duration. The start impulse at the beginning of a character-code signal interrupts the current flow, releasing the printer selector magnets. This action initiates one printer cycle. During the remainder of the cycle, the printer selector magnets act as an electromechanical decoder for the five code-element impulses representing the character to be printed. After the fifth code-element impulse, the stop impulse again causes current flow through the printer selector magnets. If this current flow is maintained past the completion of a printer cycle, the printer stops. The printer then remains idle until the next start impulse. The printer selector magnets, therefore, act as both start/stop control and as signal decoders for the printer.

The duration of the stop signal may be considered as the duration of the mark (current flow) between the last code-element impulse of the present teletype-character signal, and the start impulse of the next teletype-character signal. In continuous printing, the stop impulses provided by the outgoing line unit are 20 milliseconds long. This 20-millisecond duration ensures that the printer completes a print cycle before subsequent signals are provided to it.

In the incoming line unit, the start impulse provided from the keyboard initiates the process of loading the keyboard buffer. The stop impulse provided by the keyboard inhibits further operation of the incoming line unit. The duration of the keyboard stop impulse is determined by the rate at which the operator depresses the keys. In the model 28, the keys cannot be struck at a rate faster than 10 characters per second.

a TIMING - Timing signals for both the outgoing and the incoming line units are supplied by the clock shown at the left of Figure 9-7. A 9.6-kilocycle clock drives the complement input of the first flip-flop in a divide-by-16 flip-flop chain. As each flip-flop in this chain changes state from 1 to 0, it complements the following flip-flop in the chain. Both the 1 and the 0 outputs of the fourth flip-flop in the chain, $LUFD_3$, supply a 600-cycle square wave. This output, the LUI CLOCK, provides timing for the incoming line unit.

The LUI CLOCK also drives an additional divide-by-4 flip-flop chain. The output of the last flip-flop in this chain, $LUFD_5$, is a 150-cycle square wave. This output is the LUO CLOCK, which provides timing for the outgoing line unit.

At ten characters per second, the composite teletype signal representing one character or printer operation has a duration of 100 milliseconds. This 100-millisecond interval is divided into the 20-millisecond stop impulse and six additional 13.3-millisecond impulses, the start impulse and the five code-element impulses. The LUO CLOCK is asserted twice during the start impulse and twice during each of the five subsequent code-element impulses. This timing relationship is used by the outgoing line unit to generate teletype signals for the printer.

The reader, on the other hand, is an asynchronous device. The incoming line unit cannot know when an operator is about to strike a key. If a 150-cycle clock were used to time the incoming line unit, a situation could easily arise in which the logic were trying to sample the level of the incoming teletype signals just as that level were changing. In order to avoid this situation, a 600-cycle clock is provided.

A 600-cycle square wave is asserted eight times during each 13.3-millisecond code-element impulse. The incoming line unit samples the level of the incoming teletype signal at the beginning of the fifth LUI CLOCK cycle subsequent to the start impulse generated by the keyboard. Thus, the operator can strike a key at any time; the incoming line unit

nevertheless always samples the incoming teletype signal at some instant between eight and ten milliseconds after the start of an impulse.

b OUTPUT LOGIC - The outgoing line unit consists of a six-bit shift register, LUO, three control flip-flops, a timing counter, and two timing counter decoders.

The iot pulse that initiates a printing operation is IOT0404. This pulse effects a 1 transfer of AC bits 17 through 13 into the first five bits of the six-bit shift register (LUO_{1-5}). At some time subsequent to this pulse, the timing counter and associated circuits produce a start pulse. This start is followed by six consecutive shift pulses. The first shift pulse comes 13.3 milliseconds after the start pulse. The interval between shifts is also 13.3 milliseconds. The sixth shift coincides with the end pulse, which is also produced by the counter and timing circuits. The first start pulse subsequent to IOT0404 sets the sixth bit of the shift register.

This sixth shift-register bit, LUO_6, is the flip-flop that produces the waveform of the composite teletype signal. The 0 output of LUO_6 is gated into a solenoid driver provided no key is currently depressed at the keyboard. The printer prints the character corresponding to a key struck at its keyboard, so that while the keyboard is being used as an input device, the printer is not free to print output characters. In order to avoid conflicting signals to the printer selector magnets, the 0 output of LUO_6 is gated to the solenoid driver by a level which is asserted only when the keyboard is free.

When the 0 output of LUO_6 is asserted, the solenoid driver causes current flow in the line, energizing the printer selector magnets. When LUO_6 is clear, current flows in the line; when LUO_6 is set, no current flows in the line. The first start pulse subsequent to IOT0404 sets LUO_6, interrupting current flow in the line. This interruption of current is the beginning of the start impulse.

After the 13.3-millisecond duration of the start impulse, the first of the six shift pulses is produced by the timing circuits. Each pulse shifts the entire contents of the shift register one place to the right. This is a normal shift in LUO_{1-5}; however, the shift from LUO_5 to LUO_6 is a complement shift, ie if LUO_5 is 1 before the shift, then 0 is shifted into LUO_6. The first shift, occurring 13.3 milliseconds after LUO START, changes the state of LUO_6 to represent the first of the five teletype code-element impulses designating the

character to be printed. The second shift pulse, 13.3 milliseconds later, again changes the state of LUO_6 to represent the second teletype code-element impulse. The third, fourth and fifth shift pulses, provided at 13.3-millisecond intervals, change the state of LUO_6 to produce the third, fourth and fifth teletype code-element impulses.

Suppose, for example, that AC 13-17 contain the five-bit code representing the letter F, 10110. Pulse IOT0404 transfers the five AC bits into LUO_{5-1}. The first subsequent start pulse produced by the timing circuits sets LUO_6, producing the teletype start impulse. The first shift, 13.3 milliseconds later, clears LUO_6, producing current flow (a mark) in the teletype line. This is the first code-element impulse in the character F. The next four shifts respectively set, clear, clear, and set LUO_6. This action produces the remaining four code-element impulses of the character F: space, mark, mark, space, in that order. The result of the output operations up to this point has been to develop the teletype start impulse and the five code-element impulses representing the character F, by successively shifting the five code bits contained in LUO_{1-5} to the right into LUO_6. Since the contents of LUO_{1-5} have been shifted out, these bits are now clear.

The sixth shift provided by the timing circuits coincides with the LUO END pulse. Since LUO_5 is now clear, this sixth shift pulse sets LUO_6, initiating current flow in the teletype line. This new current flow denotes the beginning of the teletype stop impulse. Simultaneously, LUO END sets LUO FLAG. The flag, when on, indicates that the outgoing line unit is ready for the initiation of another printer cycle. This flag may be cleared by IOT0402.

The timing and control circuits for the outgoing line unit include the two flip-flops LUO ON and LUO IBT (A7), the four-bit LUO counter, and two associated counter decoders. When IOT0404 transfers information into the first five bits of the shift register, it also sets LUO ON. In changing state from 0 to 1, LUO ON clears LUO FLAG. The asserted 1 output of LUO ON gates the first subsequent LUO START pulse to set LUO IBT and LUO_6. The shift pulses to all six bits of the shift register are gated by the 1 output of LUO IBT. The end pulse, concurrent with the sixth shift, not only sets LUO FLAG but also clears both LUO ON AND LUO IBT. Flip-flop LUO ON is therefore set from IOT0404 until LUO END.

However, LUO IBT is 1 only during the generation of the teletype start impulse and the

five teletype code-element impulses. Both these flip-flops are cleared by LUO END, at the beginning of the teletype stop impulse.

The 150-cycle LUO CLOCK is applied both to a gated complement input to LUO counter bit CT3, and to the capacitor-diode gate at the set input of LUO counter bit CT2. This counter thus counts 15 LUO CLOCK pulses, by gating the first pulse to set CT2 and gating the remaining 14 pulses to complement CT3. Since the first LUO CLOCK sets CT2, the counter already contains the number 2 after only the first pulse. The second and all subsequent LUO CLOCK pulses complement CT3. The counter then functions as an ordinary binary counter. Since after the first clock the counter contains 2, it is cleared by the 15th clock. This count-to-15 process is repeated over and over again. LUO START is produced by the first LUO CLOCK subsequent to the interval during which the counter contains 3. The LUO START pulses are therefore produced at intervals of 100 milliseconds (corresponding to 10 characters per second).

The least significant bit of the counter, CT3, changes state from 1 to 0 seven times during this 100-millisecond interval. The first clearing of CT3 occurs when the counter is changing from 3 to 4. Each subsequent time CT3 clears, it produces a LUO SHIFT pulse. The first of the six shifts therefore occurs about 13.3 milliseconds after the start pulse. Subsequent shifts follow at intervals of 13.3 milliseconds.

When the counter clears (ie, has counted 15 pulses), the change in state from 1 to 0 in the most significant bit of the counter, CT0, produces LUO END. This pulse signals the beginning of the stop impulse. After 20 milliseconds, a new LUO START pulse is generated. It is followed by a new group of six shifts and a new LUO END pulse (concurrent with the sixth shift). Again, 20 milliseconds later, another LUO START pulse is generated. This process is performed over and over again.

If an information transfer at IOT0404 occurs during the 20-millisecond interval between LUO END and LUO START, then the new character is printed immediately after the last at the maximum printing rate. If no new transfer occurs between the end and start pulses, then a full 100-millisecond printer cycle must elapse before the printing of another character.

A timing chart (Figure 9-8) shows the operation of the counter, the four control flip-flops,

and the shift register. This timing chart also shows all the pulses generated by the outgoing line unit.

c INPUT LOGIC - The teletype line input from the keyboard is shown in Figure 9-7D4. A 10K resistor bleeds the -15 vdc supply to the teletype keyboard generator contacts. These contacts are closed when the keyboard is idle. Since the contacts are closed, current flows in the line, representing a teletype stop impluse of indefinite duration. When a key is struck the keyboard generator contacts generate a teletype signal that corresponds to the depressed key. This teletype signal includes both the start and the stop impulses.

When the operator strikes a key, the keyboard generator contacts first open for 13.3 milliseconds, representing the start impulse. Following this, the keyboard generator contacts produce the five code-element impulses representing the appropriate character or printer operations. Finally, after the fifth code-element impulse, the keyboard element contacts close once more, representing the stop impulse. The duration of this final stop impulse has no upper limit, but must not be less than 18 milliseconds. Duration of the stop impulse is determined by the frequency with which the operator strikes keys at the keyboard. The stop impulse provided from the keyboard cannot be shorter than approximately 18 milliseconds because the keyboard is interlocked to prevent the operator from typing at a speed faster than 10 characters per second. The operator may, however, type at any rate slower than 10 characters per second.

The incoming line unit includes a six-bit shift register, a three-bit timing counter, two control flip-flops, and associated gating circuits. The first bit of the six-bit shift register, LUI_5, is connected to sample the level of the incoming teletype line at a shift pulse. If at the time of a shift, current is flowing in the line (mark), LUI_5 is cleared. On the other hand, if current is not flowing in the line (space), then the shift sets LUI_5.

The first subsequent shift transfers the state of LUI_5 into LUI_4, and simultaneously loads LUI_5 with the next mark (or space) impulse. The effect produced by subsequent shifts is the same, ie each shifts the contents of the register to the right one place and simultaneously loads LUI_5 according to the present level of the teletype signal.

The timing system for the incoming line unit provides six shifts. These shifts are provided between eight and ten milliseconds after the start of each incoming teletype impulse,

including the start impulse. Since the start impulse is always a space (no current flow) the first of the shift pulses always sets LUI_5. The five subsequent shift pulses shift the 1 originally contained in LUI_5 five places to the right. The result, after all six shifts have occurred, is that the 1 originally loaded into LUI_5 by the start impulse is now contained in the sixth bit of the register, LUI DONE. This flip-flop indicates that the shift register loading process is complete.

After the sixth shift, the contents of LUI_{5-1} are the complement of the five-bit code representing the character corresponding to the key that was struck. The sixth bit of the register, LUI DONE, contains 1. Bits 5 through 1 contain the complement of the teletype code because bit 5 is cleared when sampling a mark impulse and set when sampling a space impulse. To compensate for the complement representation, the 0 outputs of LUI_{5-1} are provided as 1-transfer lines to the information collector.

The timing circuits for the incoming line unit are the three-bit counter LUI CTR, the two control flip-flops LAST and NO CHAR, and the pulse gates shown at the left of the shift register. The 600-cycle LUI CLOCK is supplied to the gated complement input of the least significant counter bit, CTR2. This complement gate is shown in the figure as a circle, and is different from the usual pulse gate. When the negative level input to this gate is asserted, input pulses behave as though they were applied to a direct clear input. In other words, if the gating level is asserted, input pulses applied to this complement gate may complement CTR2 from 1 to 0, but cannot complement CTR2 from 0 to 1. If the gating level is negated, then incoming complement pulses may complement CTR2 in either direction.

Whenever the teletype keyboard generator contacts are closed, the generator idle level, LUI IDLE, is asserted (D4). LUI IDLE is a negatively asserted level and is equivalent to the negation of the positively asserted level LUI RUN. If the incoming teletype signal is idle, ie the keyboard generator contacts have been closed for some time, then the timing counter (CTR) and flip-flop LAST are clear. Flip-flop NO CHAR is set, however, indicating that no signal is presently being received from the keyboard.

When a key is struck, the start impulse (a space) interrupts the flow of current in the line. The interruption of current asserts the LUI RUN level at ground. Since flip-flop NO CHAR is 1 and LUI RUN is now asserted, the capacitor-diode gate for LUI CLOCK pulses is enabled (C4). The first subsequent LUI CLOCK is gated through a pulse amplifier to clear

NO CHAR and all six bits of the shift register. In clearing, NO CHAR disables the negative inhibit level at the complement input gate of CTR2.

Since the first clock is used to clear NO CHAR, the counter actually begins counting with the second clock. The counter contains 1 after the second clock, and therefore must contain 4 after the fifth clock. Consequently, it is the fifth LUI CLOCK which sets the most significant bit of the counter, CTR0. The fall in the negatively asserted 1 output of CTR0 is interpreted as a pulse by the capacitor-diode gate shown in D4. If flip-flop LAST is not yet set, this pulse is gated to produce the first of the six shifts for the shift register. Since CTR0 is set by the fifth 600-cycle LUI CLOCK pulse, the interval between the beginning of the incoming start impulse and the shift is between 8 and 10 milliseconds.

Subsequent shifts are produced each time CTR0 is set. Every eighth LUI CLOCK sets CTR0, producing a 13.3-millisecond interval between shifts. When the sixth shift loads 1 into LUI DONE, the change in state from 0 to 1 sets LAST. After 6.6 milliseconds, CTR0 clears. The clearing of CTR0 clears LAST, which in turn sets NO CHAR. The 1 output of NO CHAR again asserts the inhibit level at the clock input to the counter. At this point, the five teletype character code-elements produced by the keyboard generator are represented by the contents of the first five bits of the shift register, LUI_{1-5}. Flip-flops LUI DONE and NO CHAR are set; the timing counter and flip-flop LAST are clear.

The device flag is produced by ANDing the 1 outputs of DONE and NO CHAR. Since both these flip-flops are set, LUI FLAG is asserted, indicating that the keyboard buffer contains an unretrieved character. Pulse IOT0302 clears LUI DONE, turning off the FLAG, and at the same time transferring the contents of LUI_{1-5} into AC_{13-17}.

Figure 9-9 is a timing chart showing the operation of the shift register, the two most significant bits of the timing counter, and flip-flops LAST, NO CHAR, and DONE. Figure 9-9 also shows all pulses generated by the incoming line unit.

A new loading cycle begins whenever the operator again strikes a key. At the instant the key is struck, the incoming start impulse gates in the first LUI CLOCK to clear NO CHAR and initiate a new loading cycle. Initiation of a new loading cycle proceeds regardless of whether or not the five bits representing the previous character have been transferred to the accumulator. If the operator types at the maximum keyboard speed of 10 characters

per second, the interval during which transfer to AC is possible may be as short as 15 milliseconds. All PDP-4 programs involving keyboard input must therefore sense the LUI flag at intervals which are sufficiently short to ensure data transfer to AC within 15 milliseconds from the time the flag goes on.

CHAPTER 10

CIRCUIT DESCRIPTION

10-1 GENERAL

This chapter describes the function and operation of the circuits used in the standard PDP-4 computer and in the following three options: the real time option, the punch and the keyboard/printer. All circuits except power supplies and the type 813 power control are plug-in modules; ie, all components are mounted on DEC standard etched circuit boards.

Schematic diagrams are included for all circuits, except that any module which includes a final "R" in its type number shares the same schematic with the unit having the same type number with the "R." Inverters 4106 and 4106R are an example of such a pair. The additional connections of the R type are indicated by dotted lines in the common schematic. The schematic diagrams are grouped at the rear of the manual, in order by type number. No figure reference is made in individual unit descriptions, but references to the applicable schematics are implied.

10-2 INVERTERS

The inverter modules used in PDP-4 are made up of combinations of three basic circuits: a -3 vdc supply, a diode-clamped load resistor, and a basic inverter. The clamped loads and the -3 vdc supplies are all identical. In inverter 1103R, diode D1 and resistor R13 make up a typical clamped load, while diodes D7, D8, D9, and D10, and resistor R19, form a typical -3 vdc supply.

There are two types of basic DEC inverter, differing in speed of operation. These are the high-speed (5 mc) inverter and the low-speed (500 kc) inverter. Module 1103R contains a typical high-speed inverter composed of transistor Q1, resistors R1 and R2, and capacitor C1. Module 4105 contains a typical low-speed inverter, composed of Q1, R1, R2 and C1. The two inverter types differ only in transistor type, and in the value of the base input by-pass capacitor (C1). These two differences affect only the switching speed of the circuit. The delay time of the high-speed 1000 series is 20 nanoseconds, while that of the low-speed 4000 series is 0.3 microseconds. Both types of inverter are used as level gates or pulse gates, and both are driven by DEC standard levels and negative pulses.

The inverter transistors are operated in two modes: saturation and cut-off. When an inverter transistor is in the saturated state, collector-emitter impedance is very low. Conversely, at cut-off, collector-emitter impedance is very high. If the emitter is at ground, and the collector is connected to a -3 vdc clamped load, the collector output level (or pulse) is an inversion of the base input level (or pulse). For example, if the base input level is ground, the transistor is cut-off. The output is then -3 vdc, determined by the clamping voltage. However, if the base input level is -3 vdc, the transistor saturates. The ground level at the emitter is then also present at the output.

Base input loading is determined by the 3K base resistor. With -3 vdc present at the base input and the emitter at ground, a saturating current of 1 ma flows through the transistor. The base input by-pass capacitor provides overdriving current to speed transistor switching. When the base input is at ground, the 68K resistor to +10 vdc supplies I_{co} to achieve good dc cut-off of the transistor. This 68K resistor also acts as a voltage divider with the 3K input resistor to shift the base positive, thereby preventing accidental transistor turn-on by noise pulses.

The diode in the clamped load limits the negative voltage at the inverter outputs. It does this by providing a low impedance path from the -3 vdc supply when the output voltage at the collector of the inverter transistor is more negative than -3 vdc. The clamping diode thus supplies whatever current is needed to maintain a 12-volt rise (from -15 vdc) across the 1.5K load resistor. This current is a maximum of 8 ma under no-load conditions, and decreases to zero as the current drawn from the external load increases to 8 ma. The value of the clamped-load resistor thus determines the maximum external load current at which the inverter can maintain a regulated -3 vdc output.

The -3 vdc supply is established by the four 0.75 vdc forward voltage drops across four series-connected 1N645 silicon diodes. Current flows from ground through the four diodes and then through the parallel combination of the supply load and the 560-ohm resistor. This resistor accepts enough current to maintain a -3 vdc diode voltage even under minimum-load conditions.

a INVERTER 1103R - This 5 mc module contains six basic inverters, six clamped loads, and a -3 vdc supply. All logic terminals (base input, emitter, and collector) are accessible at the output pins of the module. The clamped loads are internally connected to the output terminals of the basic inverters. The 1103R circuit is accurately represented by the

1103 schematic provided that the dotted lines between the clamped loads and the output terminals are understood to be wiring connections.

b INVERTER 1104 - This 5 mc module contains four basic inverters, four clamped loads, and a -3 vdc supply. Both the logic terminals and the clamped-load terminals are accessible at the output pins of the module. Bias return for transistors Q1 and Q2 is to +10 vdc (A). For transistors Q3 and Q4, bias return is to +10 vdc (B). This division permits submodular marginal testing and thus facilitates troubleshooting.

c INVERTER 4102R - This 500 kc module contains nine basic inverters, nine clamped loads, and a -3 vdc supply. Each inverter has its emitter internally connected to ground, and each inverter collector is internally connected to a clamped load. The base and collector logic connections of each inverter are brought to the external connector.

d INVERTER 4105 - This 500 kc module contains five basic inverters, three clamped loads, and a -3 vdc supply. All logic and clamped-load terminals are accessible at the output pins of the module. Bias return for transistors Q1 and Q2 is to +10 vdc (A). The bias return for Q3, Q4 and Q5 is to +10 vdc (B).

e INVERTER 4106 - Except that no internal connections are made between transistor collectors and associated clamped loads, this module is the 500 kc equivalent of inverter 1103 R (a above).

f INVERTER 4106R - This module is the 500 kc equivalent of inverter 1103R (a above).

10-3 DIODES

The diode modules in PDP-4 contain one or more diode logic gates. Diode modules 4112, 4112R, 4114 and 4114R contain negative OR gates (OR gates for negative levels). Diode modules 4111, 4113, 4113R and 4115R contain positive OR gates (AND gates for negative levels). Each gate is internally connected to an inverter base input. A clamped load is provided for each inverter. A single -3 vdc supply (described in paragraph 10-2) is included in each diode module. With the exception of diode 4111, inputs can be driven either by DEC standard levels or by 0.4-microsecond negative pulses. Only levels may be applied to the inputs of diode 4111.

a DIODE 4111 - This module contains two identical six-diode positive OR gates (composed of diodes D1-D6 and D7-D12, respectively). The following description of a six-diode positive OR gate (an AND gate for negative levels) refers to the circuit containing diodes D1 to D6 (inputs K to R), but applies equally to the circuit containing diodes D7 to D12.

Gate current is returned to -15 vdc through resistor R1. Any diode that is connected to a ground input is forward-biased. Consequently, the gate output is at ground, less the small forward voltage drop across the diode. Voltage divider D13, D14 and R3 shifts the gate output sufficiently positive to ensure that Q1 is cut off. Therefore, if any input is at ground, the output (pin J) is at -3 vdc (assuming the inverter collector is connected to a clamped load, such as R5-D17).

When all inputs are at -3 vdc, the gate output disconnects from the gate input. The negative gate output voltage is determined by current flowing from the base of Q1 through D13 and D14. This current saturates Q1, grounding the output at the collector of Q1. Capacitor C3 furnishes overdriving current to the base of Q1, speeding transistor switching. Switching delay averages 0.4 microseconds.

Bias resistors R3 and R4 are connected to separate +10 vdc (A and B) lines to permit independent marginal testing of the two diode gates contained in the module.

b DIODE 4112 - This module consists of six identical two-diode negative OR gates. Six clamped loads are also included in the 4112 module but are not used. The six pairs of gating diodes are D1-D2, D3-D4, D7-D8, D9-D10, D13-D14 and D15-D16. The following description of a two-diode negative OR gate refers to the circuit containing diodes D3-D4, but applies equally to the other diode circuits.

The gate is driven by +10 vdc (A and B) applied through resistors R3, R4 and R8. This voltage forward-biases the diodes. The voltage drop across the diodes is low. As a result, the voltage at the base-input resistor R3 approaches the lowest voltage present at either of the gate inputs (E or F).

If one or both of the inputs is a negative logic level (-3 vdc), a negative level is applied to the base input of the inverter transistor Q1. This turns Q1 on, causing the collector output of Q1 to rise to ground.

The inverter transistor is cut off only in the event that none of the inputs are negative (ie, only if both inputs are ground levels). A ground level is then applied to the base input of the inverter. Switching delay is no more than 0.3 microseconds.

Resistors R4 and R8 are connected to the A and B +10 vdc lines, respectively. This prevents excessive sensitivity of transistor operation to the marginal test.

c DIODE 4112R - This module is identical to diode 4112 (b above) except that each of the six clamped loads is jumpered to the collector output of the corresponding gate transistor.

d DIODE 4113 - This module consists of six identical two-input positive OR gates. Six clamped loads are also included in the 4113 module but are not used.

The two-diode positive OR gate functions in a similar manner to the six-diode positive OR gates described in a above (module 4111). If a ground level is applied to either of the two input terminals, then the inverter transistor is turned off. The inverter transistor is turned on only when negative logic levels (-3 vdc) are applied to both input terminals.

The six positive OR gates contained in the 4113 module have a switching delay of approximately 0.16 microseconds. A speed-up capacitor in the base circuit of each gate (shunting the two series-connected silicon diodes) accelerates the turn-off of the transistor when one or more of the gate inputs is raised to a ground level. The base resistors of three of the six gates are connected to the A supply; the base resistors of the remaining three gates are connected to the B supply. This permits submodular marginal checking of the 4113 circuit.

e DIODES 4113R and 4113X - The 4113R module is identical to the 4113 (d above) except that each of the six clamped loads is jumpered to the collector output of the corresponding gate transistor.

The 4113X module is also identical to the 4113 except for internal connections between the collector outputs and the clamped loads. In the 4113X, outputs H, T and W are ORed by connecting these three outputs to a single clamped load. Similarly, outputs P and Z are ORed by common connection to a second clamped load. Output L is connected to a third clamped load, as in the 4113R. The remaining three clamped loads are not used.

f DIODE 4114 - This module contains two identical four-input negative OR gates and two identical three-input negative OR gates. Four clamped loads are also included in the 4114 module but are not used. The three-diode and four-diode negative OR gates function in a similar manner to the two-diode negative OR gates described in b above (module 4112). If -3 volts is applied to any one of the inputs of a gate, the inverter transistor associated with that gate is turned on. The inverter transistor is turned off only when all of the inputs are at ground.

Maximum switching delay of each circuit is 0.3 microseconds. The gate puller resistors (R1 and R3, for example) are returned to separate +10 vdc lines, making gate operation less critical with respect to marginal variations in the +10 vdc lines.

g DIODE 4114R - This module is identical to diode 4114 (f above) except that each of the four clamped loads is internally connected to the collector of the corresponding gate transistor.

h DIODE 4115R - This module contains two identical four-input positive OR gates and two identical three-input positive OR gates. The module also contains four clamped loads which are internally connected to the collector of an associated gate transistor. Except for the number of inputs, the operation of both the four-diode and three-diode gates is similar to the operation of the two-diode gate described in d above (module 4113). If a ground level is applied to any one of the inputs of a gate, the inverter transistor associated with that gate is turned off. The output is then at the clamping voltage (-3 vdc). The inverter transistor is turned on, grounding the output, only when all of the inputs are at -3 vdc.

Maximum switching delay of each circuit is 0.16 microseconds. The bias resistors (R2 and R8) of transistors Q1 and Q3 are connected to +10 vdc (A); the bias resistors (R5 and R11) of Q2 and Q4 are connected to +10 vdc (B). This permits submodular testing of the gate circuits.

i BINARY-TO-OCTAL DECODER 4150 - Both outputs of each of three flip-flops are applied to the input terminals of the binary-to-octal decoder. The decoder has eight out-

put terminals numbered 0 through 7. For any given combination of states of the three flip-flops which furnish the decoder inputs, one specific output of the decoder is a -3 vdc level and the remaining seven decoder outputs are ground levels.

The binary-to-octal decoder module is composed of eight identical parts. Each of these parts is a three-diode negative OR gate (which is logically equivalent to a positive AND gate). Except for the number of gate diodes, each of these gates is identical to one of the negative OR gates included in diode module 4112 (b above).

The eight decoder output terminals shown in the 4150 schematic represent, from left to right, the octal numbers 0 through 7. The output signals generated by the decoder always include a single -3 vdc level at one of these eight terminals. The remaining seven outputs are then at ground. The -3 vdc level is generated at a specific output terminal -- that terminal which represents the octal equivalent of the binary number in the three input flip-flops.

The eight diode gates are each connected to a different set of input lines (refer to the lower portion of the 4150 schematic). These connections are arranged so that each of the eight gates responds to one of the eight possible combinations of 0s and 1s that can be generated by three flip-flops.

As in the case of diode module 4112 (b above), a given gate transistor is cut off, thereby producing a -3 vdc output, only when ground levels are applied to all of its gate input diodes. Because of the gate input configuration, only one of the eight gates receives ground levels at all three input diodes. The remaining seven gates must each have at least one negative input level (-3 vdc). Consequently, the seven associated transistors remain saturated, thereby producing ground output levels at all but one of the decoder outputs.

Each of the eight sets of three-diode gate inputs is connected to one output terminal (either the 0 terminal or the 1 terminal) of each of the three input flip-flops. When a flip-flop is in the 1 state, its 0 and 1 outputs are at ground and -3 vdc, respectively. For the 0 state of the flip-flop, the polarity of the outputs is reversed. The decoder logic senses the 1 state of an input flip-flop as a ground level taken from the 0 output of the flip-flop. Conversely, a ground level from the 1 output asserts the 0 state of the flip-flop.

The output terminals of the flip-flop representing the least significant of the three binary digits being decoded are connected to inputs L (1 out) and K (0 out). The flip-flop outputs

for the next more significant digit are similarly connected to J and H, while those for the most significant digit are applied to F and E. Because the 1 state of a flip-flop is asserted by a ground level from its 0 output, the input connections for each gate are the complement of the three-digit binary number being decoded. For example, the gate which decodes octal 7 (= binary 111) is connected to the 0 outputs of all three flip-flops. These three terminals are all at ground when the three flip-flops contain the binary number 111. With all three diodes at ground, the gate transistor is cut off and the 7 output terminal of the binary-to-octal decoder drops to -3 vdc.

10-4 CAPACITOR-DIODE GATES

The capacitor-diode modules contain pulse gates. Standard 0.4 microsecond negative DEC pulses or negative-going level changes drive the pulse inputs of these gates. Logic levels are applied to the gating inputs. The polarity of the logic level applied to a specific pulse gate determines whether or not that gate will generate an output pulse when an input pulse is applied to it.

The 4128 capacitor-diode module contains pulse gates which have an inverter input stage, and an output gating stage. This module is used for reading information into unbuffered flip-flops (type 4214). The pulse gates in the 4127 and 4129 capacitor-diode modules are constructed differently. These two modules have an input gating stage and an output inverter stage. The 4127 and 4129 modules are used for sampling the outputs of unbuffered flip-flops or any other logic level. The flip-flop output is used as a gating level. The contents of the flip-flop can then be sampled by applying a standard DEC pulse to the pulse input of the capacitor-diode gate.

a NEGATIVE CAPACITOR-DIODE GATE 4127 - The 4127 module contains six identical pulse gates. Each gate has an inverter at the gate output. The following description refers to the gate containing transistor Q1, but applies equally to the other five gates of the module.

Type 4127 pulse gates are used to sample any logic level. The level is applied to input F of the gate, and a standard 0.4 microsecond negative DEC pulse is applied to input E. If the gating level is negative (-3 vdc) the gate is enabled. The negative input pulse then

generates a positive-going output pulse at terminal H. If the gating level is at ground, the gate is inhibited and no output pulse is generated.

A logical delay is built into the circuit to prevent logical race problems. Delay is necessary to avoid splitting pulses when an unbuffered flip-flop is sampled at the same time it is pulsed. Because of the built-in delay, the gating level must be present one microsecond before the arrival of the input pulse.

The pulse gate is composed of capacitor C1, diode D1 and resistor R2. Through R5, the output of the gate is referenced to a dc level of -3.75 vdc. This voltage source is provided by an additional series-connected diode, D25, which is added to the -3 vdc supply in the module. Diode D2 and resistor R1 are included to prevent the pulse gate input from being driven more negative than -3 vdc. Should the input be driven too negative, D1 might be forward-biased, causing spurious turn-on of transistor Q1 (without the arrival of a pulse at input E).

When the gate is enabled by the application of a -3 vdc level to input F, capacitor C1 charges to -3 vdc through R1 and R2. Diode D1 is still reverse-biased, because its anode is at -3.75 vdc. But, when a negative pulse is applied to pulse input E, and is differentiated by C1, diode D1 is forward-biased. The resulting negative pulse at the junction of D1 and R5 is coupled through C2 to the base of Q1. This turns on the transistor, causing output terminal H to rise to ground potential.

At the trailing edge of the input pulse, D1 is cut off. Some rise in voltage is coupled through C2 before D1 cuts off. However, the base of Q1 is clamped to ground through D3, so no excessive back-bias is applied to the base of Q1.

The clamped loads in the 4127 module (D4 and R4, D8 and R9, etc.) are not used. No connections are made from the output pins of the module to these loads.

b NEGATIVE CAPACITOR-DIODE GATE 4127R - The 4127R module differs from the 4127 in only one respect. In the 4127R each of the six clamped loads is internally connected to the collector output of the corresponding inverter.

c POSITIVE CAPACITOR-DIODE GATE 4128 - This module contains two identical units. Each of these units is composed of a single inverter and four capicator-diode pulse gates.

The following description refers to the pulse gate with pulse input terminal P and output terminal E, but applies equally to the other seven gates of the module. Terminal F is the gate level input of this pulse gate. The terminal P input pulse is shared with three other gates having output terminals H, K and M.

The circuit is triggered by applying a standard negative DEC pulse to input P. This input pulse is inverted by transistor Q1. The resulting positive-going pulse at the collector of Q1 is applied to the gate through C4. If the gate is enabled, the differentiated rising edge of the pulse is applied to the output of the circuit. The negative spike created by differentiation of the trailing edge of the pulse never appears at the output of the circuit but is instead discharged through R8.

The logic level applied to gating input F determines whether or not the pulse gate will pass the positive spike generated by the leading edge of the input pulse. A negative gating level (-3 vdc) prevents the generation of an output pulse by providing dc back-bias to diode D2. A ground gating level permits the generation of an output pulse.

When a -3 vdc level is applied to gate terminal F, the junction of C4 and D2 drops from ground to -3 vdc. The delay required for this change in voltage is determined by the time constant of R8 and C4. The gate is inhibited when the anode of D2 is at -3 vdc. With the gate inhibited, no positive pulse of less than three volts can cause the junction of C4 and D2 to rise above ground to forward-bias D2. Therefore, no pulse can be applied to the load at output E (which is normally at ground potential).

When a ground level is applied to gate terminal F, the junction of C4 and D2 rises from -3 vdc to ground. The delay required for this change in voltage is determined by the time constant of R8 and C4. The pulse gate is enabled when the anode of D2 is at ground. Any positive pulse is then sufficient to forward-bias D2; consequently any positive pulse is passed through D2 to the load.

The 4128 module is used to read information into a type 4214 unbuffered flip-flop. For this use the pulse output of the gate is connected to either the 0 or the 1 input of the flip-flop. The positive output pulses from the pulse gate then set or clear the flip-flop. The delay built into the capacitor-diode circuits is useful for preventing logical race problems (refer to a above). Because of the delay built into the circuit, the ground gate enabling

level must be present at least 1.5 microseconds before a shift or jam transfer, and at least 4.5 microseconds before a standard read-in operation.

d NEGATIVE CAPACITOR-DIODE GATE 4129 - This module contains two identical units. Each of these units is composed of four pulse gates ORed into an inverter output stage. These gates are identical to the gates used in the 4127 module (a above). A DEC 0.4-microsecond negative pulse, applied to a pulse input, is enabled by a -3 volt level input and is inhibited by a ground level input. A 68K resistor returns each gate level inp to +10 vdc. This prevents any unused gates from affecting the rest of the circuit. The 4129 module also includes a negative dc supply identical to the supply in module 4127. (This supply provides both -3 vdc and -3.75 vdc outputs.)

The pulse gates of the 4129 module may be used to sample the outputs of unbuffered flip-flops. The flip-flop output is applied to the level input of the gate, and a standard 0.4 microsecond negative DEC pulse is applied to the pulse input. Because of the logical de built into the circuit, the gating level must be present one microsecond before the arriva of the input pulse.

e NEGATIVE CAPACITOR-DIODE GATES 4129R and 4129X - The 4129R module diffe from the 4129 in only one respect. In the 4129X each of the clamped loads is internally connected to the collector output of the corresponding inverter.

The 4129 module is also similar to the 4129X except for one variation. The collectors of both inverters in the 4129X are internally connected to one of the clamped loads included in the module. The other clamped load is left unconnected and is not used.

10-5 FLIP-FLOPS

There are seven different flip-flop modules used in the PDP-4. The 4203 module contains one flip-flop, the 4204 module contains two flip-flops. The remaining five PDP-4 flip-flop modu (1213, 4214, 4215, 4216 and 4218) each contain four flip-flops. All flip-flops change state when an on transistor is turned off by a positive pulse applied to its base. The collectors of the nonconducting transistors are clamped to -3 vdc. Each module includes a -3 vdc supply for clamping voltage.

a FLIP-FLOP 1213 - This module contains four identical flip-flops (1 through 4), eight capacitor-diode gates, one inverter, and a -3 vdc supply. The four flip-flops are designed to operate as a unit. With slight changes in external pin connections, the module can operate as a four-stage shift register or as a four-bit buffer register. Both types of operation are described below. A negative pulse applied to terminal E is inverted by transistor Q1 and brought out to terminal F. This positive-going pulse may be used to drive the shift-one and shift-zero pulse inputs (S and V) to all four flip-flops. The eight capacitor-diode gates are used to set and clear each flip-flop. Note that only flip-flop #1 has an external connection for a 0 input (P). The other three flip-flops in the module have internally connected 0 inputs, but no 0 terminal is brought out to the module connector. A clear input (M) is used to clear all four flip-flops simultaneously. Each flip-flop has individual 1 and 0 outputs.

Silicon diodes D17 through D20 make up the -3 vdc supply. Resistor R28 to -15 vdc, in series with the diodes, furnishes sufficient current to keep the diodes forward-biased, thus providing a constant -3 vdc source.

When the module is used as a buffer register, terminal F (pulse out) is externally connected to S (shift one). A 70 nanosecond negative pulse applied to E initiates a parallel 1s transfer into the four flip-flops of the module. Just those flip-flops are set to which ground levels are applied at the time of the pulse.

The 70-nanosecond negative pulse is inverted by Q1 and then applied to F and S as a positive pulse referenced to -3 vdc. This positive pulse is applied from S to the 1 input gates of all four flip-flops. Gating capacitors C11, C13, C15 and C17 differentiate the pulse and reference it to the level present at the one-in terminals of the four flip-flops (pins N, R, T and U). This level may be either -3 vdc or ground.

Since the cathode voltages of diodes D2, D6, D10 and D14 are close to ground, the pulse can pass these diodes only when the corresponding one-in terminals are at ground. For example, suppose that flip-flop #1 is in the 0 state (Q2 on, and Q3 off). Then, if the one-in terminal of the flip-flop (N) is at ground, a pulse through S can pass D2, cutting off conduction through Q2. The cut-off of Q2 turns on Q3, switching the flip-flop to the 1 state. In contrast, if the one-in terminal of the flip-flop is at -3 vdc when S is pulsed, no change in state can occur.

While the module is used as a buffer register, no individual 0 transfers occur. A 70-nanosecond pulse applied to M clears the entire register. This clear operation is carried out berore the parallel is transfer described above. The flip-flop side of C3 is returned to -0.75 vdc to provide noise immunity for the clear input.

When the module is used as a shift register, F is externally connected to both S and V. The 0 outputs of flip-flops #1, #2 and #3 are each externally connected to the 1 inputs of the next more significant stage (J to R, L to T, and X to U). These external connections parallel the existing internal connections from the 1 outputs of flip-flops #1, #2 and #3 to the individual 0 inputs of flip-flops #2, #3 and #4 respectively. Although only flip-flop #1 has an external 0 input, all four flip-flops have identical clear capacitor-diode gates. These gates are pulsed through the shift-zero line.

As a shift register, flip-flop module 1213 operates in the following manner. Assume all four flip-flops are initially in the 0 state. The first 70-nanosecond negative pulse arriving at E is inverted by Q1 and appears as a positive pulse on both the shift-one and shift-zero lines. This pulses the 0 and 1 inputs to all four flip-flops. If ground is present at the one-in terminal of flip-flop #1 (N) and -3 vdc is present at the zero-in terminal (P), flip-flop #1 is set to the 1 state. This causes the 0 output of that flip-flop to rise to ground (J). Because J is connected to R, the 1 input of flip-flop #2, the second shift pulse sets flip-flop #2. The effect of the second pulse on flip-flop #1 is independent of the change in state of flip-flop #2 and depends only on the levels applied to the input gates of flip-flop #1.

The third shift pulse sets flip-flop #3 to the state of flip-flop #2. If the preceding pulse cleared flip-flop #1, its 1 output is at ground. This ground output causes the third shift pulse to clear flip-flop #2. The 1s and 0s injected at flip-flop #1 thus propagate through the entire shift register on successive shift pulses. Each stage assumes the state of the next less significant stage. The delay of the capacitor-diode input gates in accepting level changes prevents any ambiguity in the flip-flop outputs at pulse time. This delay is small compared to the pulse rate.

It is possible to set or clear any of the four flip-flops individually without pulsing the shift lines. For instance, to clear flip-flop #4 independently, the collector of an inverter is connected to the 1 output of the flip-flop. When flip-flop #4 is in the 1 state, Q8 is off and Q9 is on. The flip-flop remains in the 1 state because the collector load of Q8 draws

sufficient current through R26 to keep Q9 saturated. The level shift produced by R23 from the collector of Q9 to the base of Q8 reverse-biases Q8, holding it cut off.

If the emitter of the inverter is at ground and the inverter is driven to saturation, its collector (together with pin Y) will rise to ground. This causes Q9 to be cut off. The collector voltage of Q9 falls to the clamp voltage and turns on Q8. The flip-flop is then stable in the 0 state. The flip-flop can be set in the same way by grounding its 0 output. A change of state produced in this manner does not affect the other flip-flops in the module, and can occur independently of the shift pulses. The emitters of inverters used for this purpose must be directly connected to ground.

b FLIP-FLOP 4203 - This module consists of a single buffered flip-flop, 3 pulse inverters, 13 negative and 2 positive capacitor-diode gates, a two-diode negative AND gate, and a negative dc supply.

Each negative capacitor-diode gate is similar to those contained in module 4127 (paragraph 10-4a). Each positive capacitor-diode gate is similar to those in module 4128 (paragraph 10-4c). The negative supply generates -3 vdc in the same manner as do the supplies contained in the inverter modules. However, an additional series diode, D36, is added to the supply, generating -3.75 volts. Terminals are located at the front and back of the module. Those located at the back have an asterisk added to the letter denoting the terminal (A*, for example).

Type 4203 flip-flops make up the PDP-4 accumulator. Flip-flop pulse inputs include set (K*, S and X), clear (E* and F*) shift (J* and H*) and complement (K, A*, B* and C*). Except for inputs A*, F* and S, all pulse inputs are gated by an associated level input. These levels are asserted at -3 volts. Accordingly, the register may be loaded in parallel, have its contents shifted left or right, or be complemented, with a minimum of external circuitry.

A carry output (H) permits connection of the register bits so that the register may be used as a counter. The 0 and 1 outputs are at F and R, respectively. A -3 volt level at F and ground at R indicates the 0 state, while the opposite polarity, ground at F and -3 volts at R, indicates the 1 state. Terminal L provides a 1 output for a console panel indicator.

Capacitor-diode gates provide all input gating. The logical delay built into this type of gate permits the input levels to be sensed at the same time that the flip-flops which generate these levels are changing state. With the exception of the carry input (K), standard DEC 0.4 microsecond pulses drive all inputs. The carry input is driven by a level drop from ground to -3 volts (generated when the next less significant accumulator bit goes from the 1 to the 0 state).

The flip-flop is set by a negative pulse at K* or X, provided that level input W or T, respectively, is at -3 vdc. A negative pulse at S always sets the flip-flop, since the level return of the capacitor-diode input gate is internally connected to -3 vdc through R45. The following description of the setting of the flip-flop by a pulse at K* also describes the operation of the flip-flop in response to signals at all three set inputs.

Prior to the application of a pulse at K*, the cathode of diode D30 is at the voltage applied to W (ground or -3 vdc). Regardless of the cathode voltage, D30 is back-biased, since its anode is connected to -3.75 vdc through R37. Capacitor C19 blocks the -3.75 vdc from the base of transistor Q6; this transistor is held off by a positive voltage at its base, from voltage divider R38-D31.

Assume that the flip-flop is in the 0 state; then Q4 is cut off and Q5 is on. The 0 output buffer, Q2, is held off by the ground at the collector of Q5, so the 0 output at F is -3 vdc. The 1 output buffer, Q7, is held on by the -3 vdc at the collector of Q4, so the 1 output, R, is at ground.

A 2.5-volt negative set pulse applied to K* is coupled to the cathode of D30 by C18. If the quiescent level at the cathode of D30 is ground (a ground input level at W) the diode is not forward-biased by the set pulse. The pulse is then inhibited at this point. However, if the quiescent level is -3 vdc, D30 is forward-biased, passing the pulse to the base of Q6 through C19. Transistor Q6 inverts the pulse, momentarily grounding the collector of Q4. Voltage divider R33-R34 shifts the base of Q5 positive, turning Q5 off. The collector of Q5 is then clamped at -3 vdc by D21 and R22. The -3 vdc is coupled to the base of Q4 by R23 and C14, turning Q4 on. The turn-on of Q4 holds its collector at ground after the termination of the set pulse. The flip-flop is then in the 1 state.

The turn-on of transistor Q4 holds the 1 output buffer (Q7) off, so that the 1 output at R

is at -3 vdc, and the light-driver output at L is energized through R44. The turn-off of Q5 turns on the 0 output buffer, Q2; consequently the 0 output, F, is at ground.

The flip-flop is cleared by a 2.5-volt negative pulse applied to E* or F* in a manner similar to that described above. The clear pulse switches the flip-flop to the 0 state by momentarily grounding the collector of Q2. A pulse at E* is gated by the level applied to M. The input at F*, like the set input at S, is always enabled.

The flip-flop may be either set or cleared by a negative pulse at either J* or H*. A pulse at J* is directed to the set or clear side of the flip-flop by a -3 vdc assertion level at terminal U or P, respectively. Similarly, a pulse at H* is gated by the levels at V and N. These assertion levels are derived from the adjacent bits of the accumulator so as to jam transfer the state of the adjacent bit into the flip-flop (a shift operation). Except that the set and clear gates of the flip-flop are pulsed simultaneously, the operation of these inputs is similar to the operation of a set input descrived above, since only one of the pair of gates is enabled at any time.

Terminals A*, B*, C* and K are the complement inputs to the flip-flop. A negative pulse at C*, or a falling level at K complements the flip-flop provided that J or D*, respectively, is at -3 vdc. In order for a pulse at B* to complement the flip-flop, both level inputs Z and Y must be at -3 vdc. A pulse at A* always complements the flip-flop, since the associated capacitor-diode gate level return is internally connected to -3 vdc through R6. The following description of flip-flop complementing by means of a pulse at B* also describes the operation of the flip-flop in response to a signal at any of its four inputs.

Prior to the application of a pulse to B*, the cathode of D4 is at the highest voltage of either input Y and Z. (These two inputs are ANDed for negative levels by diodes D1 and D2, diode D3 limits the maximum negative gate output to -3 vdc.) Whether this voltage is ground or -3 vdc, D4 is back-biased because its anode is returned to -3.75 vdc through R8. Capacitor C5 isolates the -3.75 vdc from the base of Q1. This transistor is held off by a positive voltage on its base, determined by voltage divider R10-D10.

The collector of Q1 is clamped to -3 vdc by D12 and R9. Capacitors C13 and C15 isolate this voltage from the anodes of D22 and D28, respectively. The voltage at the anodes is determined by the voltages on the collectors of flip-flop transistors Q4 and Q5, through

R29 and R26, respectively. Neither D22 nor D28 is forward-biased (their cathodes are approximately at ground), and the flip-flop remains stable in either state.

The leading edge of a negative pulse input at B* is differentiated to a negative pulse at the cathode of D4. This negative pulse is superimposed on the quiescent level. If the quiescent level is -3 vdc (both Z and Y at -3 vdc), D4 passes the negative pulse to the base of Q1 through C5. Transistor Q1 inverts the pulse; the inverted pulse is then applied to capacitor-diode gates C13-D22-R29 and C15-D28-R26.

The pulse is directed by the gates to the base of the on transistor. For example, if the flip-flop is in the 0 state, Q4 is off and Q5 is on. The level at the anode of D28 is ground, so D28 is forward-biased by the pulse and passes the pulse to the base of Q5. The level at the anode of D22 is -3 vdc, and the pulse does not have sufficient amplitude to forward-bias D22. Consequently, the pulse is blocked from the base of Q4. When the pulse turns the on transistor off, the flip-flop changes state.

c FLIP-FLOP 4204 - This module contains two buffered flip-flops, two pulse inverters, eight negative and four positive capacitor-diode gates, and a series-string silicon diode negative dc supply. The negative capacitor-diode gates are similar to those of module 4127, while the positive capacitor-diode gates are similar to those of module 4128 (paragraphs 10-4a and c, respectively). Four series-connected diodes (D18 to D21) generate -3 vdc as in the supply contained in the inverter modules (paragraph 10-2). In the type 4204, a fifth diode (D17) is added to the series-string, generating -3.75 vdc. The supply is also tapped between diodes D20 and D21 to provide -0.75 vdc. Except for the number and arrangement of input and output terminals, each of the two flip-flops contained in the module is similar to the flip-flop in module 4203 (b above).

Type 4204 flip-flops make up various registers of the PDP-4. Gated set pulse inputs at L, M and N are shared by both flip-flops. Common set pulses at these inputs are gated into flip-flop A by levels at inputs J, H and F respectively. The same set pulses are gated into flip-flop B by levels at inputs W, X and Y respectively. Inputs K and U provide separate direct set inputs to flip-flops A and B, respectively. All set inputs accept DEC standard 2.5-volt, 0.4-microsecond negative pulses. Assertion levels for the gating level inputs are -3 vdc.

The counting inputs (S for flip-flop A and the corresponding unlettered terminal, shown in the center of the schematic, for flip-flop B) are used only in module 4204X (d below). Flip-flop A has its 1 and 0 outputs at P and E, respectively; flip-flop B has its 1 and 0 outputs at Z and R.

Both flip-flops share a common clear input at terminal T. Unlike the clear input of flip-flop 4203 (in which an additional pulse inverter accepts a negative pulse) input T of the type 4204 requires a DEC 0.4-microsecond positive pulse. This pulse is ac coupled by capacitor C3 to the bases of A and B flip-flop transistors Q2 and Q7, respectively. For example, when a positive pulse is applied to T, capacitor C3 references the pulse to the level at the anodes of D6 and D14. This level is -0.75 vdc, determined by the connection through R34 to the negative supply. The small negative voltage prevents noise pulses from passing through D6 and D14, which would cause spurious clearing of the flip-flops. However, a standard DEC positive pulse at T generates a sufficiently positive voltage to forward bias D6 and D14, and pass to the bases of Q2 and Q7. These transistors cut off, and the two flip-flops assume the 0 state.

d FLIP-FLOP 4204X - This module is identical to flip-flop 4204 (c above), except that the collector output of transistor Q8 (corresponding to the 1 output of flip-flop A) is internally connected to the counting (complementing) input of flip-flop B. The schematic of flip-flop 4204 also represents modules 4204X if the dotted line in the center of the schematic is assumed to be a wiring connection.

Flip-flops of the 4204X module make up the bits of PDP-4 registers that are also counters. In addition to the inputs described in c above, flip-flop A has a counting input (S). The carry output of flip-flop A and the count input of flip-flop B are connected inside the module. Terminal V is the carry output of flip-flop B, available for connection to the next more significant type 4204X module. The count pulse input to S may be a 0.4 microsecond positive pulse, as it is when flip-flop A is the least significant bit of a counter. Terminal S also accepts the rising level from carry output V of the next less significant counter bit when this bit changes from 1 to 0. The clear pulse at T must be 1.0-microsecond wide so that the pulse does not end before the carries die out.

e FLIP-FLOP 4214 - This module contains four identical flip-flops (#1 through #4) and a -3 vdc supply. Each flip-flop has 0 and 1 inputs and outputs. Moreover, each pair of flip-flops shares a common clear input: P for flip-flops #1 and #2, and R for flip-flops #3 and #4. A standard DEC 0.4-microsecond positive pulse, applied to P or R, clears both associated flip-flops. Because all four flip-flops are identical, the following description of flip-flop #1 also applies to the other three flip-flops.

When flip-flop #1 contains 0, transistor Q1 is on and transistor Q2 is off. The flip-flop is stable in this state because the negative collector voltage of Q2 is coupled to the base of Q1 by R2. The current flow through R2 is enough to keep Q1 saturated. The collector of Q1 is therefore at ground; thus the voltage divider, R5 and R6, biases Q2 off.

To set the flip-flop to the 1 state, the pulse output of a positive capacitor-diode gate is applied to H (one in). This pulse turns off transistor Q1. The resulting negative voltage at the collector of Q1 drives Q2 into saturation. The collector of Q2 rises to ground potential, keeping Q1 cut off. Silicon diodes D3 and D4 have a forward-bias threshold of more than 0.5 volts, and thus block smaller noise-pulse inputs from the transistor bases. The flip-flop is cleared in a similar way by a positive pulse at E (zero in). The clear pulse turns Q2 off, returning Q1 to saturation.

The bases of the two transistors in each flip-flop are returned to separate +10 vdc lines to allow more precise trouble localization through marginal testing.

f FOUR-BIT COUNTER 4215 - This module contains four flip-flops for use as counter bits. The four flip-flops, A, B, C and D, are logically independent. The flip-flops may therefore be connected in any logical configuration. When the flip-flops are connected as a counter, the significance of each flip-flop as a counter bit is determined only by the external connections. The module also contains 12 positive capacitor-diode gates (C14-R30-D1 and C1-R7-D5 are two examples) and a negative dc supply. The supply, consisting of diodes D21 to D24 and resistor R29, is similar to the -3 vdc supply contained in module 1103R (paragraph 10-2a), except that -0.75 vdc is tapped from the junction of D21 and D22.

Flip-flops B, C and D have complement inputs at terminals R, K and E, respectively. Flip-flop A has separate set and clear inputs, but may be complemented by applying a

signal to both inputs simultaneously. Flip-flop C has an inhibit level input at M. When the inhibit is enabled, flip-flop C cannot be complemented from 0 to 1, although it may still be complemented from 1 to 0.

Positive pulses (either a standard 0.4 DEC pulse or the positive-going output of a pulse inverter) or a positive 3-volt step (such as the 1 output of a less significant counter bit when that flip-flop goes from 1 to 0) drive the complement and clear inputs. A -3 vdc level at M enables the inhibit to flip-flop C. Carry propagate time per bit is 50 nanoseconds. The following description of flip-flop A also describes the other three flip-flops.

A positive pulse applied to W (set one) or V (set zero) reaches the base of the associated flip-flop transistor only if the transistor is on. The positive pulse changes the state of the flip-flop by turning the on transistor off. When flip-flop A is 1, a positive pulse at input V passes through capacitor-diode gate C15-R31-D4 to the base of Q2, turning Q2 off. The flip-flop switches to the 0 state. Positive pulses at V now have no further effect, since capacitor-diode gate C15-R31-D4 is disabled when flip-flop A is 0. However, gate C14-R30-D1 is enabled when flip-flop A contains 0, so that a positive pulse at W passes to the base Q1, turning Q1 off, and switching flip-flop A to the 1 state.

If W is jumpered to V, the resulting combined input is a complement input. When this input is pulsed, gates C14-R30-D1 and C15-R31-D4 steer the pulse to the base of the on transistor, turning it off, so that the flip-flop switches state. Gate C1-R7-D5, associated with terminal X, is permanently enabled because R7 is returned to -0.75 vdc. Thus a positive pulse at X clears flip-flop A directly. Resistor R7 is returned to -0.75 vdc rather than to ground in order to prevent spurious noise from affecting the flip-flop. Since signal voltages are greater than -0.75 vdc, they pass through D5, but small noise signals are blocked. The gate time constant (R7 x C1) is longer than that of the other two capacitor-diode input gates because a 1.0-microsecond pulse is used to clear the counter. This allows carried to die out before the pulse ends.

Terminal R (add FFB) is the complement input to flip-flop B. A positive pulse at R is applied simultaneously to two capacitor-diode gates. These gates, C16-R32-D6 and C17-R33-D9, steer the pulse to the base of the on transistor, turning it off. When flip-flop B is 1, gate C17-R33-D9 is enabled, and a positive pulse at R clears FFB. Conversely, when FFB is 0, gate C16-R32-D6 is enabled, and a positive pulse at R sets it. The complement input to

flip-flop D, terminal E (add FFD), operates similarly.

Terminal K (add FFC) is the complement input to flip-flop C. Pulses at K are gated by two capacitor-diode gates, like the two input gates of flip-flop B, described above. One of the two input gates of flip-flop C is returned to the collector of Q6. This gate, C19-R35-D14, is enabled when FFC is 1. If FFC is 1, a positive pulse at K is gated to the base of Q6, turning it off, and clearing the flip-flop. The other capacitor-diode gate, C18-R34-D11, is returned to the output of a negative OR gate, of which the collector of Q5 is one input, rather than directly to the collector of Q5.

This OR gate, composed of D25, D26, and puller resistor R38, functions similarly to the gates described in paragraph 10-3b (diode 4112). The anode of D11 is at the more negative level of either the collector voltage of Q5 or the inhibit level at terminal M. When the input at M is ground, flip-flop C functions as the others in the module, and is complemented by each positive input pulse at K. However, if the input at M is -3 volts, the pulse at K cannot reach the base of Q5, even though the collector of Q5 is ground (the flip-flop is in the 0 state). On the other hand, the path to the base of Q6 is not affected by the input at M, so the flip-flop may be complemented from 1 to 0 regardless of the inhibit level.

g FLIP-FLOP 4216 - This module contains 4 flip-flops, 2 pulse inverters, 12 positive capacitor-diode gates, and a series-string silicon diode negative dc supply. The four flip-flops have internal output to input connections between consecutive flip-flops so that the four flip-flops constitute a four-bit shift register package. Four capacitor-diode gated inputs are provided for parallel read-in of 1s.

Flip-flops A, B, C and D include transistors Q9-Q10, Q7-Q8, Q5-Q6, and Q3-Q4, respectively. Except for the number and arrangement of inputs, these flip-flops are similar to those of module 4215. Transistors Q1 and Q2 are the two pulse inverters. All 12 capacitor-diode gates are used at the inputs of the flip-flops; each gate (C2-R6-D3, for example) is similar to the positive capacitor-diode gates of module 4128 (paragraph 10-4c). Diodes D28 to D31 and resistor R44 make up the negative supply. This supply is similar to those contained in the inverter modules (see paragraph 10-2).

For shift operation, the shift pulse input is through terminal R to the base of Q1.

Complementary input levels at J and F gate the inverted pulse at the collector of Q1 to the set or clear side of flip-flop D. For parallel read-in of 1s, the read-in pulse is applied to P, to the base of Q2. The input levels at H, M, T and Y gate the inverted pulse at the collector of Q2 to the set sides of flip-flops D, C, B and A, respectively. A pulse at X clears all four flip-flops simultaneously. Pulse inputs are DEC standard 0.4 microsecond pulses, negative for inputs R and P, and positive for clear input X. Level inputs are ground for assertion. Input-output delay for each flip-flop is 50 nanoseconds.

Assume that all flip-flops are clear prior to a shift operation. A negative pulse at R is inverted by Q1, appearing as a positive pulse at the collector of Q1. The positive pulse is ac coupled to the anodes of diodes D4 and D11 by capacitors C4 and C10 respectively. The voltage at the anode of D4 is the sum of the positive pulse and the level at terminal J, while the voltage at the anode of D11 is the sum of the positive pulse and the level at F. If F is ground, and J is -3 vdc (read in 0), only D11 is forward-biased, passing the pulse to the base of Q4, tending to cut Q4 off. However, Q4 is already cut off, thus flip-flop D remains in the 0 state.

The pulse from the collector of Q1 is also applied to the 1 and 0 inputs of flip-flops C, B and A, through capacitors C8, C15, C13, C20, C18 and C23. However, the pulses are gated only to the clear side of all flip-flops, because each 0 input gate return is to the 1 output of the flip-flop to the left. Since all flip-flops are initially clear, the 1 outputs are at ground, enabling the 0 input gates. The 1 input gates of flip-flops C, B and A are disabled by the -3 volt assertion levels at the 0 outputs of flip-flops D, C and B. For example, C15 couples the pulse to the anode of D17. Diode D17 is forward-biased because the level return of gate C15-R21-D17 is to the grounded collector of Q3. The same pulse is coupled through C8 to the anode of D9, but D9 is reverse-biased by the -3 volt level asserted by the 0 output of flip-flop D. Therefore the shift pulse tends to clear flip-flop C, rather than to set it; so that flip-flop C remains clear after the shift pulse.

If, at the shift pulse, J is at ground and F is at -3 vdc (read-in 1), diode D4 passes the pulse to base of Q3. Transistor Q3 is cut off, and flip-flop D goes to the 1 state. The level at the anode of D9 goes to ground after a delay approximating the time constant C8 x R12. Therefore the next shift pulse passes through D9 to the base of Q5, setting flip-flop C. In a similar manner subsequent pulses shift the 1 through the register.

Parallel read-in to the four flip-flops is accomplished by a negative pulse applied to terminal P. The pulse at P is inverted at the collector of Q2. This positive pulse from Q2 is gated to the bases of the odd numbered transistors of flip-flops D through A by capacitor-diode gates. In this case, the enabling levels that select the flip-flops to be set are present at inputs H, M, T, and Y. For example, a positive pulse from the collector of Q2 is ac coupled to the anode of D3 by capacitor C2. The pulse forward-biases D3 and passes on to the base of Q3 only if input H has been at ground for several time constants. If the pulse reaches the base of Q3, this transistor is cut off and flip-flop D is set.

A positive pulse at terminal X clears the register by turning off all the even numbered transistors of flip-flops D through A. A four-output positive capacitor-diode circuit (C6-R36-D10-D16-D22-D26) couples the pulse to the transistor bases. The gate return connection to -0.75 volts prevents noise pulses from affecting the flip-flops.

h FLIP-FLOP 4218 - This module contains four flip-flops, a pulse inverter, eight positive capacitor-diode gates, and a negative dc supply. Depending on external connections, type 4218 flip-flops may be used as bits of shift registers or buffer registers with a jam-transfer parallel read-in. Flip-flops #1, #2, #3 and #4 include transistors Q2-Q3, Q4-Q5, Q6-Q7, and Q8-Q9, respectively. Transistor Q1 is the pulse inverter.

All inputs are through positive capacitor-diode gates; each of these gates is similar to the gates described in paragraph 10-4c (module 4128). The negative dc supply, consisting of diodes D17 to D20, and resistor R28 is similar to the -3 vdc supply described in paragraph 10-2 (inverters). However, the supply in module 4218 has a -0.75 volt tap at the junction of diodes D17 and D18, and a -2.25 volt tap at the junction of diodes D19 and D20.

The read-in pulse input at terminal P is a DEC standard 0.4-microsecond negative pulse. Levels at terminals E, H, S and V gate the pulse to the set side, and levels at F, K, U and X gate the pulse to the clear side of flip-flops #1 through #4, respectively. Gating levels are asserted at ground. All four flip-flops are cleared simultaneously by a DEC standard 0.4 microsecond positive pulse at R. Input-output delay for each flip-flop is 50 nanoseconds.

The four flip-flops become a shift register if the 0 output (L) and 1 output (J) of flip-flop #1 are connected as gating levels to the 1 input (H) and 0 input (K), respectively, of

flip-flop #2; and similar connections are made between flip-flops #2 and #3, and #3 and #4. The resulting four-bit shift register is comparable to module 4216 (g above) except that it lacks gated parallel 1 inputs. A positive pulse at R clears the register, and a negative pulse at P reads into flip-flop #1. Subsequent pulses shift the 1 through flip-flops #2, #3 and #4.

When the four flip-flops are used as a buffer register with jam-transfer parallel read-in, the external connections are made differently from the above. In this case, both 1s and 0s are transferred (the register need not be previously cleared) into the flip-flops of module 4218 in a simultaneous parallel transfer from corresponding bits of another register. The 1 and 0 gating level inputs of flip-flop #2, for example, are connected to the 0 and 1 outputs, respectively, of an associated bit in another register. When this associated bit is 1, the negative assertion level at its 1 output disables the 0 input gate of flip-flop #2; and the level at the 0 output of the associated bit, asserted at ground, enables the 1 input gate of flip-flop #2. Conversely, when the associated bit is 0, the 1 input gate of flip-flop #2 is disabled and the 0 input gate is enabled. Similar connections are made to the 1 and 0 input gate terminals of the other three 4218 flip-flops. A negative pulse at P causes each flip-flop to assume the state of the corresponding bit in the associated register.

The response of the flip-flops of the type 4218 module to the read-in pulse is similar to the response of the flip-flops of the type 4216 module (g above).

10-6 AMPLIFIERS

This section describes seven modules which serve to provide power amplification for PDP-4 logic pulses and levels. Pulse amplifiers 1607, 4604, 4605, 4606 and 4606R power amplify and standardize DEC logic pulses. Bus driver 1690 inverts and amplifies logic levels. Solenoid driver 4681 is basically a switch which enables a small amount of input power at logic level voltages to control larger amounts of power at higher voltages for use in external circuits.

a PULSE AMPLIFIER 1607 - This module contains three inverters and a -3 vdc supply. The three pulse amplifiers include transistors Q2-Q3, Q5-Q6 and Q8-Q9. The inputs to the three amplifiers are pins H, L and P, while the outputs are E-F, J-K, and M-N, respectively. The three inverters are Q1, Q4 and Q7. Diodes D16 through D19 make up the -3 vdc supply.

A pulse amplifier generates an output pulse whenever its input is grounded. The input may be grounded by connecting it to the collector of one or more pulse gates (such as the Q1 circuit). The input to the combined circuit is then the base input of the pulse gate. Normally the signal applied to the input is a DEC 70-nanosecond negative pulse. However, the input requirement is satisfied by any 2 to 5 volt negative pulse having a fall time less than 50 nanoseconds, and a width of at least 50 nanoseconds at -2 volts. When the input is pulsed by a signal meeting these specifications, the output generates a DEC standard 70-nanosecond pulse delayed by 25 nanoseconds. This pulse is capable of driving 16 units of pulse load, or 20 units, if the loads are near by.

Because all three pulse amplifiers are identical, the following description of the amplifier including transistors Q2 and Q3 applies equally to the other two amplifiers in the module.

Assume that the emitter of Q1 is grounded (Z) and that the collector of Q1 (X) is connected to the emitter of Q2 (H). In the quiescent state, transistors Q1, Q2 and Q3 are cut off. The collector of Q1 and the emitter of Q2 are connected to the junction of resistor R3 and silicon diode D1, and are therefore at approximately -4 vdc. Resistor R3 and diode D1, together with R4 and D2, form a voltage divider between -15 vdc and -3 vdc (with the diodes forward-biased). The base of Q2 is connected to the voltage divider at the junction of D1 and D2, and is held at approximately -3.3 vdc.

Another voltage divider is formed by the series combination of R11 and R16. This voltage divider holds the collectors of Q2 and Q3 at approximately -8 vdc. Diode D4 is forward-biased, so that the collector voltages of Q2 and Q3 are separated by only 0.3 volts. The base and emitter of Q3 are at ground. There is no voltage across outputs E and F.

When an input pulse appears at the base of Q1 (Y), this transistor saturates and grounds the emitter of Q2. This causes Q2 to saturate; resistor R4 limits the base current. The collector of Q2 drops from -8 vdc to ground. This drop immediately appears across the primary of T1. Initially this voltage remains fairly constant because of the low-resistance voltage divider R11 and R16. When the transformer starts drawing more current than originally flowed through R6, D4 disconnects the collector circuits from R11-R16. The voltage across T1 begins to decrease. Capacitor C2 tunes the circuit to give the correct output pulse width. When the transformer voltage has dropped to zero the output pulse ends. Resistor R5 and diode D3 clamp the overshoot in the primary of T1.

The Q3 circuit (including R8, T2, D5, R7 and C4) amplifies the pulse from the secondary of T1 (see b below). The output pulse may be made negative by grounding terminal F of the secondary of T2; or positive, by grounding E. A terminating resistor in the range of 82 to 220 ohms is used at the ends of cable distribution lines to prevent signal reflections.

b PULSE AMPLIFIER 4604 - This module contains three identical pulse amplifiers. The first pulse amplifier includes transistors Q1 through Q3, and has its inputs at terminals E and F. Outputs are at J and H. The second pulse amplifier is composed of Q4, Q5 and Q6; inputs are M and N; and outputs are S and T. The third pulse amplifier includes Q7 through Q9, with inputs at Y and Z; and outputs at V and X. An additional pair of control terminals is associated with each of the three pulse amplifiers. For the first pulse amplifier, these control connections are K and L. Shorting K to L with an external jumper connects an internal capacitor in the circuit of the first pulse amplifier. When connected, this additional capacitance legthens the duration of the output pulse to 1 micorsecond. The corresponding control connections for the second and third pulse amplifiers are terminal pairs P and R; and U and W, respectively.

Negative going signals with an amplitude of 2.5 to 4 volts, a fall time of less than 0.5 microseconds, and a width greater than 60 nanoseconds drive inputs E, N and Z. Positive-going signals with an amplitude of 2.5 to 4 volts, a rise time of less than 0.5 microseconds, and a width greater than 60 nanoseconds drive inputs F, M and Y.

When properly driven, each amplifier produces a DEC standard 0.4-microsecond pulse across its outputs. If the external jumpers are added to the circuits, the outputs produce 1-microsecond pulses. Because all three amplifiers are identical, the following description of the amplifier including Q1, Q2 and Q3 applies to each amplifier.

The pulse amplifier consists of a monostable multivibrator (Q1 and Q2), and an output pulse amplifier (Q3). Capacitor-diode C4-D6 couples a negative input at E to the base of Q2. Capacitor-diode C3-D3 couples a positive input to the primary of transformer T1. This transformer inverts the positive input, and D5 couples the resulting negative pulse to the base of Q2. An appropriate pulse at either input thus provides a negative pulse at the base of Q2. This negative pulse triggers the multivibrator. The multivibrator generates a negative output pulse, which is amplified by the circuit of Q3. The output is a negative

pulse at terminal J if H is grounded, or a positive pulse at H if J is grounded.

In the quiescent state Q1 is on, and Q2 and Q3 are off. Base current for Q1 flows through R1, holding Q1 in saturation. Voltage divider R7-R9 shifts the slightly negative Q1 collector voltage positive at the base of Q2, keeping Q2 at cut-off. Diode D1 clamps the collector of Q2 to -3 vdc. Voltage divider R8-R10-R13 biases the base of Q3 positive, holding Q3 off. The collector of Q3 is somewhat more negative than -7 volts, as determined by voltage divider R11-R14. No current flows in the primary of T2, and there is no output across the secondary.

When a negative pulse is applied to input E, C4 differentiates the leading edge of this input signal, generating a negative pulse at the cathode of D6. This pulse forward biases D6, and passes to the base of Q2. Transistor Q2 turns on, and its collector voltage jumps from -3 volts to ground. This positive step is coupled by capacitor C2 (or C1 in parallel with C2, if pins K and L are jumpered), to the base of Q1. Transistor Q1 cuts off and its collector voltage drops to -3 volts. Current flows from the base of Q2 through R7, holding Q2 on even though the input pulse has ended. The multivibrator remains in this state until the coupling capacitance (C2, or C1 and C2) from the collector of Q2 to the base of Q1 discharges. This discharge time is proportional to the capacitance. Hence, the multivibrator stays in its temporary state 0.4 microsecond if only C2 is in the circuit, or 1 microsecond if both C1 and C2 are in the circuit. After the appropriate time, Q1 turns on, cutting Q2 off. The multivibrator is back in its quiescent state.

The negative pulse generated at the Q1 collector turns on Q3. The Q3 collector rises to ground level, placing approximately 7 volts across the primary of T2. Resistors R11, R14 and capacitor C6 stabilize the voltage at terminal 1 of T2 so that the primary voltage does not diminish appreciably during the pulse. The output voltage at the secondary is proportional to the primary voltage. The pulse terminates when the multivibrator returns to its quiescent state, cutting off Q3. Diode D8 and resistor R12 damp the overshoot in the primary of T2. Diode D7 clips the overshoot at -15 volts, so that excessive voltage is not applied to the collector of Q3.

A positive pulse at terminal F triggers the same chain of events to produce an output pulse across J and H. However, the pulse is inverted by T1 before being applied to the base of Q2. Diode D2 and resistor R5 damp the transformer during recovery. Diode D5 blocks the

positive recovery pulse from the base of Q2.

c PULSE AMPLIFIER 4605 - This module contains three identical pulse amplifiers, a negative diode AND gate, and an inverter. The first of the three pulse amplifiers includes transistors Q1 and Q3. Transistor Q2 is the inverter. The second pulse amplifier includes Q4 and Q5; the third, Q6 and Q7. Diodes D1 through D6 make up the negative AND gate. Except that a pair of input pins is provided for each gating diode (M and N are alternative inputs to D6, for example) the diode gate and inverter combination is similar to one of the type 4111 circuits (paragraph 10-3a).

Terminals F, J and L are the inputs to the three pulse amplifiers; the respective outputs are E, H and K. Whenever Q2 is saturated (grounding the emitters of Q1, Q4 and Q6), a DEC standard 0.4 negative pulse applied to an amplifier input generates a similar pulse at the amplifier output. Negative DEC levels at all six diode gate inputs are required to saturate Q2. Because all three pulse amplifiers are alike, the following description of the amplifier containing Q1 and Q3 applies to the other two.

In the quiescent state the voltage at the base of Q1 is more positive than the emitter voltage. As a result, Q1 is cut off. No current flows through the primary of transformer T1, and there is no voltage across secondary. The secondary of T1 grounds the base of Q3, holding Q3 off. No current flows in the primary and there is no output a pin E. Voltage divider R8-R11 holds the collector voltages of Q1 and Q3 at approximately -7.5 volts. The Q3 collector is directly connected to the voltage divider while the Q1 collector is clamped to the divider by R7 and D9.

Assume that negative levels are present at the anodes of D1 through D6, saturating Q2. The Q2 collector is then at ground, enabling all three pulse amplifiers.

When a negative pulse, meeting the input requirements, is applied to F, Q1 saturates. This grounds terminal 2 of T1. The other end of the primary, at terminal 1, remains at -7.5 volts since the voltage source is of fairly low impedance. The voltage induced in the secondary of T1 is proportional to the voltage appearing across the primary.

Increasing current flows in the primary of T1. However, the voltage across the primary remains nearly constant until the transformer starts drawing more current than originally flowed through R7. At this time, D9 disconnects the collector of Q1 from the voltage

divider. Capacitor C3 tunes the primary winding of T1 to give the proper pulse width. When the voltage across the transformer drops to zero, the output pulse ends. Resistor R5 damps the overshoot.

In a similar manner, the circuit of Q3 further amplifies and shapes the pulse. This circuit consists of Q3, an emitter degenerating resistor R12, output transformer T2, damping components R9 and D10, and bypass capacitor C4. The output pulse is negative at terminal E.

d PULSE AMPLIFIER 4606 - This module contains three identical pulse amplifiers. Each of the three contains a basic multivibrator and pulse amplifier output circuit identical to that of the type 4604 (b above). However, the input circuits of the type 4606 differ in the following three respects:

(1) Transistor inverters are used for positive input pulses, replacing the input pulse transformers of the 4604.

(2) A capacitor-diode gate, similar to those of the type 4127, provides an additional negative pulse input to each amplifier in the type 4606.

(3) The input and output terminals are as follows:

	TERMINALS		
INPUTS	PA_1	PA_2	PA_3
Direct Positive Pulse:	F	N	V
Direct Negative Pulse:	E	M	U
Gated Negative Pulse:	K	S	Y
Negative Gating Level:	L	T	Z
OUTPUTS (same as for type 4604)			
Positive Pulse Out:	J	R	X
Negative Pulse Out:	H	P	W

e PULSE AMPLIFIER 4606R - The 4606R pulse amplifiers are identical to those of the 4606 module except that inputs F, N and V are internally connected to clamped loads. As a result, these inputs are gateable and are driven by positive-going pulses from collectors of inverter pulse gates.

f BUS DRIVER 1690 - This module contains four inverting level amplifiers, and a -3.75 vdc supply. Each amplifier output provides logic levels at low impedance, for use in heavily loaded logic lines. The output rise and fall times of level changes are extended to 1.0 microsecond. This slow-switching characteristic makes the 1690 amplifiers useful in circuits where rapid changes of level could produce unwanted ringing.

Logic levels (0 and -3 volts) are applied at inputs K, M, U and S. The corresponding outputs at L, N, T and R are the inversion of the input levels. Each input represents approximately one-half unit of 5-megacycle base load. The maximum output capability per amplifier is 15 units of base load. Each amplifier is identical. The amplifier with input K and output L is described below.

When a -3 volt level is applied to input K, transistor Q1 turns on and its collector rises to ground. This voltage rise cuts off D1, and allows R4 and R5 to bring the bases of Q2 and Q3 toward +10 vdc. The positive-going rise ends at ground when D1 again conducts. Transistors Q2 and Q3 are complementary emitter followers. One of these two transistors always conducts (Q2 when the output current flows to the load, Q3 when the current flows from the load). Output L at the emitters of Q2 and Q3 also rises to ground.

When ground level is applied to input K, the circuit switches state. Transistor Q1 cuts off, and the Q1 collector voltage falls toward -15 vdc. However, D1 and D3 clamp the voltage at -3.75 vdc. The -3.75 volt level is applied to the bases of Q2 and Q3. Output follows the base voltage applied to Q2 and Q3. Consequently, the output at L falls to approximately -3.5 volts.

Capacitor C2 delays the changes in output levels. When the input rises from -3 vdc to ground, C2 must charge through R3 and D1. Conversely, when the input drops from ground to -3 vdc, C2 must discharge through R4 and R5. Diode D1 prevents the low collector resistance of Q1 at saturation from shunting the discharge of C3. Diode D2 compensates for the level shift introduced by D1.

g SOLENOID DRIVER 4681 - This module contains three identical driver circuits. Each circuit operates as a switch, capable of switching a 500-milliampere current in a 70-volt (maximum) circuit. Switch control inputs are standard DEC logic levels. Each solenoid driver can control an inductive load, such as punch solenoids or typewriter relays.

The three switch inputs are terminals K, M and R. The corresponding outputs are L, N

and P. Terminal E is connected to the external load return voltage source. Because all three solenoid drivers are identical, the following description of circuit 1 applies to the other two drivers.

When the solenoid driver is in the quiescent condition, the input at K is -3 vdc. Since the emitter of Q1 is at ground potential, Q1 is saturated, and its collector is at ground. The emitter of Q2 is at -2.25 volts (the forward voltage drop across diodes D1 through D3). The base of Q2, at ground, is positive with respect to its emitter, so that Q2 is cut off. Under these conditions, the load circuit is open. Diode D4 connects the Q2 collector to the external negative supply, protecting Q2 from highly negative transient voltages resulting from switching inductive loads. No current flows in the external circuit, and the output is at the load return voltage.

When input K is grounded, Q1 cuts off. The collector voltage of Q1 drops toward -15 volts, turning on Q2. This completes the load circuit, allowing current to flow.

10-7 MEMORY ELEMENTS

This paragraph describes seven memory plug-in units: sense amplifier 1538, sense amplifier 1540, read/write switch 1972, memory driver 1973, resistor board 1976, resistor board 1978, and inhibit driver 1982. Sense amplifiers 1538 and 1540 perform similar functions. One or the other, but not both, is used in a PDP-4 memory module.

The sense amplifier determines when memory cores change state (refer to paragraph 8-4f). Read/write switch 1972, memory driver 1973, and resistor board 1976 are used in series with the X and Y core windings to form the read-write current path (paragraph 8-4e). Inhibit driver 1982 and resistor board 1978 are used in series with the inhibit windings to form the inhibit current path (paragraph 8-4g).

a SENSE AMPLIFIER 1538 - This module contains a difference preamplifier, a rectifying slicer, and a gated pulse amplifier. A balanced input, generated when a memory core changes state, is applied to the input of the preamplifier. Here the input is amplified enough to reach the slicing voltage. The preamplifier also discriminates against common-mode noise signals. Differential signal gain of the preamplifier is 20, while the common-mode gain is 0.

The pulse amplifier gate is enabled when the preamplifier output reaches a predetermined slice level. A strobe pulse is applied to the pulse input of the amplifier during the specific time interval when the memory cores are read and may change state. An output pulse from the sense amplifier indicates that during the strobe time a core changed state, and thereby produced a slice level which enabled the pulse amplifier gate.

The strobe permits sampling the memory sense winding at the particular instant of the read operation when the signal-to-noise ratio is best. This accurate timing increases the certainty that every time a memory core being read actually switches from the 1 state to the 0 state, this change of state will indeed be sensed; and conversely, that spurious noise signals will not be wrongly interpreted as a change in core state.

The two ends of the memory sense winding are connected to sense amplifier inputs H and F. The output pulses induced on the sense winding when the memory cores change state are applied across these two inputs. A 70-nanosecond standard DEC negative pulse is applied to strobe input R. The polarity of the sense amplifier output depends upon the output terminal wiring. When L is grounded, a positive output pulse appears at P; conversely, when P is grounded, a negative output pulse appears at L. The preamplifier outputs (T and V), the slicer test point (S) and the gating level output (M) are used only for troubleshooting.

Balance potentiometer R1 adjusts the virtual ground of the sense winding for minimum recovery time from the noise generated by the inhibit current. Potentiometer R8 is the zero set of the direct-coupled compound-connected amplifier Q2-Q3-Q4, while potentiometer R5 varies the threshold level at which the pulse amplifier is enabled. This threshold level can be varied from 0 to 50 millivolts (referred to the preamplifier inputs). Procedures for making these adjustments are discussed in paragraph 11-4c.

Before the memory cores are read, no input is applied to the sense amplifier from the memory sense winding. The two bases of Q2 are held at ground by potentiometer R1 and resistors R2-R3. Assuming that potentiometer R8 is set so that the differential preamplifier is in balance, the collector current through both sides of Q2 depends on the setting of potentiometer R5. This current, in turn, determines the voltages on the bases of slicer transistors Q5 and Q6. In normal operation, R5 is set so that these base voltages are more positive than the base voltage of slicer transistor Q7 (silicon diodes D11 through D14 hold the base of Q7 at approximately +7 vdc). Consequently, the emitter voltage of Q5, Q6

and Q7 which follows the voltage at the base of Q7, biases Q5 and Q6 off.

Since Q7 is conducting, the voltage at the base of Q8 is clamped by D10 at 0.3 vdc. As a result, Q8 is cut off, and voltage divider R22-R23 holds the emitter of Q9 at -3 vdc. The output pulse amplifier is thus inhibited, since a negative pulse at terminal R cannot trigger the amplifer by saturating Q9.

When a memory core changes state, a voltage is induced on the sense winding. Input voltages of opposite polarity are applied from inputs H and F to the bases of Q2. For out of phase signals, R31 provides the principal Q2 emitter impedance, while the common mode emitter resistance consists primarily of the relatively high collector resistance of Q1. Consequently, the differential signal is amplified substantially more than a common mode input. Transistors Q3 and Q4, in compound connection with the two channels of Q1 raise the Q2 input impedance while maintaining stage voltage gain.

The applied differential signal is amplified and inverted by the preamplifier, and drives the base of either Q5 or Q6 negative. When this base becomes more negative than the base of Q7, the latter cuts off. Transistor Q8 saturates, grounding the emitter of Q9. The output pulse amplifier is now enabled. Thus, if R is pulsed during the time the input exceeds the slice voltage, a pulse is generated across output terminals P and L. The operation of the pulse amplifier is similar to that of the type 1607 pulse amplifier described in paragraph 10-6a.

Switch S1 allows marginal check voltage on the +10A line to be applied individually to each 1538 sense amplifier.

b SENSE AMPLIFIER 1540 - This module is used in place of the 1538 sense amplifier in some PDP-4 computers. It is functionally similar to the 1538 (a above), containing a differential preamplifier, slicer and output pulse amplifier. The preamplifier differential gain is 20, while the common mode gain is 0.5.

The sense winding inputs are H and F; R is the strobe input. The outputs, at P and L, generate either a positive or negative standard DEC 70-nanosecond pulse. When L is grounded, a positive output pulse appears at P; conversely, when P is grounded, the output pulse is negative at L. The preamplifier outputs (S and U), and the gating level output (M) are used only for troubleshooting.

Balance potentiometer R2 adjusts the virtual ground of the sense winding for minimum recovery time from the noise generated by the inhibit current. Slice potentiometer R12 varies the predetermined threshold level at which the pulse amplifier is enabled. This threshold level can be varied from 0 to 50 millivolts (referred to the input). Procedures for making these two adjustments are given in paragraph 11-4c.

Before the memory cores are read, no input is applied to the sense amplifier from the memory sense winding. Therefore the bases of transistors Q1 and Q2 are grounded by R1, R2 and R3. The collectors of Q1 and Q2 are at -5 volts. Capacitors C3 and C4 isolate this voltage from the bases of Q3 and Q4. The quiescent voltage at the bases of Q3 and Q4 is determined by the setting of slice potentiometer R12. Generally R12 is set so this voltage is slightly positive. Transistors Q3 and Q4 are cut off.

Transistor Q5, which shares a common emitter connection with Q3 and Q4 is saturated since its base is at ground. Since Q5 is saturated, the Q5 collector and therefore the Q6 base are slightly positive, holding Q6 off. Voltage divider R18-R19 keeps the emitter of Q7 sufficiently negative to prevent the generation of an output pulse.

When a memory core changes state, a voltage is induced in the sense winding. Input voltages of opposite polarity are applied from inputs H and F to the bases of Q1 and Q2. For out-of-phase signals, C1, C2 and R28 bypass emitter resistors R5 and R7. As a result, the Q1-Q2 preamplifier stage produces a voltage gain for such difference input signals. But for in-phase input signals, the emitter resistance of the preamplifier stage is less than unity. The common-mode noise rejection feature of the sense amplifier circuit is due to the low common mode gain of the preamplifier stage.

At the arrival of the sense-winding input signal, an amplified negative voltage swing is capacitor coupled to the base of either Q3 or Q4 (depending upon the direction of the core's change of state).

When the base of Q3 becomes more negative than the emitter, Q3 conducts. If the base of Q4 becomes more negative than the emitter, Q4 conducts. In either case, the voltage at the emitter of Q5 follows the base voltage of the conducting transistor (Q3 or Q4). This turns off Q5. Turn-off of Q5 causes a drop in the base voltage of Q6, saturating Q6, and thereby grounding the emitter of Q7. The emitter ground at Q7 enables the pulse amplifier

input gating. Pulse amplifier operation is similar to that of the 1607 pulse amplifier (paragraph 10-6a).

The pulse amplifier remains enabled until the preamplifier output returns to its normal quiescent level. During the time the gate is enabled, a pulse applied to strobe input R generates an output pulse across terminals P and L. Although the pulse amplifier is enabled when the memory core changes state in either direction (during write operations as well as read operations) the strobe occurs only during read operations. Consequently, the sense amplifier generates an output pulse only during read operations.

c READ/WRITE SWITCH 1972 - This module contains four identical switch circuits with outputs numbered 1 through 4. Each circuit is a switch with an AND-gate input, which controls the application of drive current to a memory core winding. The following description refers to read/write switch #1 (with gate inputs E and F), but applies also to the other three switches in the module.

When -3 vdc is present at either gate input, the circuit acts as an open switch, preventing the flow of core drive current. However, when both the E and F gate inputs are grounded, the switch is enabled, permitting core drive current to flow through the associated memory core winding. The core drive current then flows between bus terminal V and output #1 (W).

If one or both of the gate inputs is at -3 vdc, the D1-D2 AND gate causes grounded-emitter transistor Q1 to saturate. The comparatively small size of resistor R1 provides fast turn-on. For fast turn-off, germanium diode D4 limits the excursion of Q1 into saturation.

When Q1 is conducting, its collector is at about -1 vdc. This voltage is direct-coupled to the base of Q2, holding Q2 off. This opens the forward-bias current path between -35 vdc and transistors Q3 and Q4. These two transistors can then be held off by back-bias diodes D5 and D6 respectively. With Q3 and Q4 cut off, the switch is open, and the drive current path between V and W is interrupted.

The switch is enabled by grounding both the E and F gate inputs. This causes the D1-D2 AND gate to cut off Q1. At the cut-off of Q1, its collector drops to a voltage more negative than the higher voltage at either V or W. During selection both of these pins are returned to -3 volts.

Transistors Q2, Q3 and Q4 turn on. The circuit between V and W closes, permitting a read or write current to flow. During the read portion of a memory cycle, V is at -13 vdc and W is returned through the memory core winding to -3 vdc. Core drive current then flows primarily through Q4. During the write portion of the memory cycle, the polarity is reversed; V is at -3 vdc and W is returned to -13 vdc through the core winding. The core drive current flows primarily through Q3 during this portion of the cycle.

d MEMORY DRIVER 1973 - Each PDP-4 memory includes two identical type 1973 memory driver modules. These drivers serve as both sources and sinks for the memory core-drive currents. The core-drive current path runs from one 1973 module (the read driver) through the enabled 1972 read/write switches (b above) and their associated 1976 resistor board circuits (d below) and core windings, to the second 1973 module (the write driver).

In the quiescent state, the input of either driver is a ground level and the output is -3 vdc. When a -3 vdc level is applied to the input of a driver (ie, to the read driver during the read portion of the cycle or to the write driver during the write portion of the cycle), the output falls to -13 vdc. A 10-volt potential then exists between the enabled driver and the quiescent driver. This potential causes a core-drive current to flow through the specific X or Y memory winding selected by the read/write switches. The logic level input is applied to input J of the memory driver. The -3 vdc or -13 vdc output is taken from output V.

In the quiescent state, a ground level is applied to input J. This input cuts off grounded-emitter transistor Q1. The resulting drop in the collector voltage of Q1 permits current through R3 to turn on Q2. The Q2 emitter current in turn saturates parallel transistors Q5 and Q7.

Current through R3 also saturates Q3, thereby grounding both the base of Q4 and the anode of diode D3. The ground at the base of Q4 turns off Q4. Diode D3 supplies cut-off current to parallel transistors Q6 and Q8, turning these transistors off also.

With parallel transistors Q5 and Q7 conducting, and parallel transistors Q6 and Q8 cut off, output terminal V is coupled to the -3 vdc source at R (and isolated from the -13 vdc source at W). The memory driver output in the quiescent state is therefore -3 vdc.

In the active state, a -3 vdc level is applied to input J. Transistor Q1 then saturates, grounding the base of Q2 and the anodes of D1 and D2. The ground at the base of Q2 turns off Q2. Diodes D1 and D2 supply cut-off current to parallel transistors Q5 and Q7, turning these transistors off.

The ground at the collector of Q1 also turns off Q3. Resistor R9 can then drive Q4 into saturation. The Q4 emitter current in turn saturates Q6 and Q8.

With parallel transistors Q6 and Q8 conducting, and parallel transistors Q5 and Q7 cut off, output V is coupled to the -13 vdc source at W (and isolated from the -3 vdc source at R). The memory driver output in the active state is therefore -13 vdc.

e. RESISTOR BOARD 1976 - This module contains eight 50-ohm, 3-watt resistors with 1/2% tolerance. A capacitor and resistor are added in parallel with each of the 50-ohm resistors.

Each of the eight parallel combinations shown on the schematic is connected as a termination load to a single X or Y winding of the memory core bank. The other end of the parallel combination is connected to one of the 1972 read/write switch outputs. The relatively high impedance of this load (compared to the impedance of the core winding) helps to ensure a constant core drive current regardless of the magnetization states of the cores threaded by a single winding.

f. RESISTOR BOARD 1978 - This module contains eight 50-ohm, 3-watt resistors with 1/2% tolerance. For use in the PDP-4 memory, only six of these eight resistors are used (resistors MT and NS are not used). The six resistors that are used have a capacitor and resistor added in parallel with each of the original 50-ohm resistors. This capacitor and resistor are connected in series; they are shown by dotted lines on the schematic. The capacitor is 4700 pf with 3% tolerance. The series resistor is 47 ohms with 1% tolerance.

Each of these parallel combinations is connected to -3 vdc (at terminal P) by 220-ohm 1% resistor. A 39 μf capacitor, C9, provides an ac shunt to ground. Each of these circuits is connected as a termination load to a single inhibit winding of the memory core bank. The other end of the parallel combination is connected to the corresponding inhibit driver.

g INHIBIT DRIVER 1982 - Each PDP-4 memory contains 18 identical inhibit drivers. Each of these inhibit drivers is a switch with an AND-gate input, which controls the application of current to the inhibit winding of a single memory core plane. Four inhibit drivers are included in each 1982 plug-in module. The following description refers to inhibit driver #1 (with gate inputs E and F), but applies equally to the other three drivers in the module.

The inhibit driver is similar to the type 1972 read/write switch (b above) except that it controls a unidirectional inhibit current only, rather than read and write currents of opposite polarity.

When -3 vdc is present at either gate input, the circuit acts as an open switch, preventing the flow of inhibit current. However, when both the E and F gate inputs are grounded, the switch is enabled, permitting core driver current to flow through the associated memory inhibit winding. The inhibit current then flows between the terminal V inhibit supply and output #1 (W).

If one or both of the gate inputs is at -3 vdc, the D3-D4 AND gate causes grounded-emitter transistor Q2 to saturate. The comparatively small size of resistor R2 provides fast turn-on. For fast turn-off, germanium diode D7 limits the excursion of Q2 into saturation.

When Q2 is conducting, its collector is at about -1 vdc. This voltage is direct-coupled to the base of Q4, holding Q4 off. This opens the forward-bias current path between the base of Q6 and -35 vdc, cutting off Q6. Diode D10 furnishes reverse bias current to Q6. With Q6 cut off, the current path between V and W is interrupted, and the inhibit driver furnishes no inhibit current.

The inhibit driver is enabled by grounding both the E and F gate inputs. This causes the D3-D4 AND gate to cut off Q2. The collector of Q2 is then driven more negative by R6. Furthermore, R6 supplies turn-on current to Q4, and the emitter current of Q4 saturates Q6. With Q6 saturated, the current path between V and W is completed, so that the driver can furnish inhibit current to the inhibit winding.

10-8 DELAY CIRCUITS

The four modules described in this section provide adjustable delays for standard DEC negative pulses. Two of these four units (the 1310 and 1311) are high speed 5 mc circuits. These two

units are used to delay 70-nanosecond pulses. The other two delay units (the 4301 and 4303) are low speed 500 kc circuits. These units are used to delay 0.4-microsecond pulses.

The 1310 and 1311 units generate comparatively short delays by means of delay lines. The 4301 and 4303 delays generate longer delay times by means of monostable multivibrators.

a DELAY 1310 - This module contains a delay line which provides up to 1 microsecond delay in 50-nanosecond steps, and an inverter driven by the delay line output. The inverter output can drive an external pulse amplifier (such as the type 1607, paragraph 10-6a). The inverter terminals are brought to the external connector of the module, so they are available for logical gating.

To trigger the delay, a standard DEC 70-nanosecond negative pulse is applied to terminal X. After a predetermined delay, dependent on the external connections made among terminals J through W, the inverter output at E is temporarily grounded, indicating the end of the delay interval.

The inverter adds 20 nanoseconds to the delay of the line. The line delays described below do not include this 20-nanosecond inverter delay.

Two jumpers are usually used to determine the delay; one for coarse adjustment, the other for fine. The coarse range of the delay is selected by one of the following jumper connections.

Jumpered Terminals	Delay Range
U to N	0 - 0.2 microseconds
V to P	0.2 - 0.4 microseconds
V to R	0.4 - 0.6 microseconds
W to S	0.6 - 0.8 microseconds
W to T	0.8 - 1.0microseconds

Within a coarse delay range, there are available five graduated delays separated by increments of 0.05 microseconds. The fine delay within a given coarse range is selected by one of the following jumper connections.

Jumper Terminals	Delay = Low End of Range Plus:
H to N	Nothing
H to M	0.05 microseconds
H to L	0.10 microseconds
H to K	0.15 microseconds
H to J	2.0 microseconds

For example: To produce a delay of exactly 0.95 microseconds, jumper W and T, and H and K (0.8 + 0.15 = 0.95).

When the circuit is in the quiescent state, resistor R1 furnishes the cut-off current which holds transistor Q1 off. Terminating resistors R2 and R3 prevent signal reflections from the ends of the delay line. By attenuating the short-delay output signals, R4 and R5 compensate for the attenuation of long-delay signals traversing a greater length of line. Diode D1 isolates the input from reflections caused by a mismatch at the output tap.

b DELAY 1311 - This module contains two identical delay lines. The following description refers to the delay containing transistor Q1, but applies equally to the other delay on the module.

The 1311 delay operates in a similar manner to delay 1310 (a above) except that the delay intervals available are limited to the lowest range of the 1310 delay. A delay of 200 nanoseconds (not including the additional 20-nanosecond delay introduced by the inverter) is available in 50-nanosecond steps.

To trigger the delay, a standard DEC 70-nanosecond negative pulse is applied to terminal E. After a predetermined delay dependent upon the external connection made between F and H, J, K or L, the inverter output at N is temporarily grounded, thus indicating the end of the delay interval.

The delays produced by each connection are as follows:

(connections in parentheses refer to the second unit)

Jumpered Terminals	Delay
F to L (S to W)	50 nanoseconds
F to K (S to V)	100 nanoseconds
F to J (S to U)	150 nanoseconds
F to H (S to T)	200 nanoseconds

c DELAY 4301 - This module contains an input pulse gate, a monostable multivibrator, an output level amplifier, and an output pulse amplifier. The pulse gate transistor is Q1; Q2 and Q3 are the multivibrator transistors; Q4 is the level amplifier transistor; and Q5 is the pulse amplifier transistor. Diodes D10 through D13 provide a -3 vdc supply.

Whenever input Y is enabled by a ground level at Z, and triggered by a DEC 0.4-microsecond negative pulse, another 0.4-microsecond pulse is generated at pulse output E or F after a predetermined adjustable delay. If E is grounded, a positive pulse is generated at F. However, if F is grounded, a negative pulse is generated at E.

In addition to its pulse output, the 4301 delay circuit also has a level output at J. This output, which is normally at ground, falls to -3 vdc during the delay. An alternate method of triggering the delay is to ground input X through the collector of an external pulse gate similar to Q1.

Using only internal components, the delay may be varied from 2.5 microseconds to 200 milliseconds in 5 ranges. With U jumpered to T, potentiometer R7 varies the delay within each range. Range selection is determined by jumpering H to one of the terminals L, N, M, P or R, thereby connecting capacitor C4, C5, C6, C7 or C8 into the multivibrator circuit. The delay range with only C4 in the circuit is 2.5 microseconds to 25 microseconds. Connecting each higher valued capacitor in turn raises the delay range by approximately a factor of 10.

Circuit recovery time is 20% of the maximum delay in each range. The connection between H and L is wired internally. If external control of the delay is desired, a potentiometer may be connected between pins S and T. Higher ranges may be added to the delay by connecting an additional capacitor between pins L and K.

Current from the base of Q2 flows through R6 and the parallel combination R7-R8. This current holds Q2 on. With the collector of Q2 close to ground, voltage divider R4-R9 holds Q3 off. The collector of Q3 is then held at about -6 vdc by voltage divider R13-R14. There is no voltage across the primary of transformer T2, and no voltage appears across the secondary.

Current through R13 and R14 saturates Q4. Consequently level output J is at ground. The base of Q5 is grounded through the secondary of T2. This ground holds Q5 off. The output

pulse amplifier remains in its quiescent state. There is no pulse output across E and F.

The 4301 delay is triggered in the following manner. A -2.5-volt, 0.4-microsecond pulse is applied through Y to the base of Q1. If the emitter of Q1 is grounded at Z, enabling the input gate, the transistor saturates, grounding its collector.

Terminal 2 of the T1 primary then becomes positive with respect to terminal 1, and an increasing current flows through the primary. (Capacitor C2 bypasses the primary to prevent input noise from spuriously triggering the circuit.) The increasing current in the primary produces a negative voltage at secondary terminal 4. Diode D1 couples this negative voltage to the base of Q3, thereby turning Q3 on.

The collector of Q3 then applies a ground through diode D7 to the junction of R13 and R14. This cuts off Q4. Output J then drops to -3 vdc, indicating the beginning of the delay interval.

The ground at the collector of Q3 is applied through diodes D5 and D6, resistor R10, and the H to K capacitance to the base of Q2. This ground immediately cuts off Q2, causing its collector voltage to drop. Resistor R4 then draws base current from Q3, holding Q3 on even after the end of the pulse from terminal 4 of transformer T1.

The monostable multivibrator made up of Q2 and Q3 remains in this state (Q2 off and Q3 on) for the time interval required to charge the capacitance in the Q2 base circuit. The RC time constant which determines this interval depends upon the capacitors in use, and the resistance of R6 in series with the parallel combination of R8 and potentiometer R7.

When the time delay capacitors have charged to a sufficiently negative voltage, Q2 turns on. The resulting rise in the collector voltage of Q2 is coupled through R4 and C3 to the base of Q3. This cuts off Q3. The current in the primary of T2 then falls to its quiescent level. The resulting negative pulse in the T2 secondary is applied to the base of Q5, turning Q5 on.

The pulse amplifier composed of Q5 and transformer T3 then generates a standard 0.4-microsecond DEC pulse across outputs E and F. Operation of the pulse amplifier circuit is explained in the description of module 4605 (paragraph 10-6d).

Since, when Q3 turns off, the voltage at the base of Q4 is determined by voltage divider

R13-R14, transistor Q4 then turns on. Output J therefore returns to ground, indicating the end of the delay.

d INTEGRATING ONE-SHOT 4303 - This module contains two monostable multivibrators, two difference amplifiers (slicers), three inverters, a positive capacitor-diode gate and a negative dc supply. These components form a single circuit. The type 4303 has flip-flop type logic level outputs. When the circuit is in the 1 state, the 1 output is asserted at -3 vdc, and the 0 output provides a ground level. In the 0 state, the 0 output is asserted at -3 vdc, and the 1 output provides a ground level. When an input (there are three) is pulsed, the circuit assumes the 1 state, having previously been in the 0 state. The circuit returns to the 0 state after a selected delay, which begins with the termination of the input signal.

The two multivibrators include transistors Q2-Q3 and Q10-Q11 respectively. Transistors Q5-Q6 form one slicer, Q7-Q8 make up the other. The three inverter transistors are Q1, Q4 and Q9. Capacitor C1, resistor R1, and diode D1 compose the positive capacitor-diode gate. The negative dc supply contains diodes D9 through D16 and resistor R28. Voltage levels of -0.75 vdc, -1.5 vdc, -3 vdc, -4.5 vdc, -5.25 vdc, and -6 vdc are tapped from the supply at the cathodes of D16, D15, D13, D11, D10 and D9 respectively.

Three inputs are provided at terminals K, S and R. The signal input at K may be either a DEC standard 0.4-microsecond negative pulse or a negative level. The input at S is a DEC standard 0.4-microsecond positive pulse or positive-going level change; this pulse is gated through to the base of Q2 by a ground level at T. Input R requires a positive pulse such as the output of a positive capacitor-diode gate similar to C1-R1-D1. The 1 and 0 outputs are W and U, respectively.

The delay is variable from 3.4 microseconds to 0.9 seconds in five overlapping ranges. Connection of one of five internally contained capacitors into the circuit determines the delay range. Capacitor C7 is connected internally to give the shortest delay range. Connecting capacitor C6, C8, C9 or C10 (E, F, H or J, respectively) to ground (D) increases the range by successive factors of approximately 10. Potentiometer R10 determines the delay within each range if Y is jumpered to X. Alternatively, the delay may be determined by an external potentiometer connected between Z and X.

In the quiescent state, Q1, Q3, Q4, Q5, Q8, Q9 and Q10 are off. Transistors Q2, Q6, Q7 and Q11 are on. Voltage divider R2-R3 shifts the ground level at input K positive, biasing Q1 off. Multivibrator Q2-Q3 is in its stable state with Q2 held on by base current flowing through R5, and Q3 held off by voltage divider R8-R9. With the collector of Q2 at ground, voltage divider R11-R12 biases Q4 off.

In slicer Q5-Q6, transistor Q5 is off and Q6 is conducting. Diode D6 clamps the collector of Q6 at -0.75 volts, holding Q6 out of saturation. The common emitter connection of NPN transistors Q5 and Q6 follows the voltage (-1.5 volts) at the base of Q6. Consequently Q5 is cut off.

The other slicer transistors, Q7 and Q8, are on and off, respectively. The series combination of potentiometer R10, and resistors R13 and R14 draws sufficient current from the base of Q7 to saturate that transistor, even if the potentiometer is set at its maximum resistance. The saturation of Q7 holds the common emitter connection of Q7 and Q8 at -5.25 volts, the collector voltage of Q7. The more positive voltage (-4.5 volts) at the base of Q8 holds Q8 at cut-off. With Q8 cut off, Q9 is back-biased through R19 so Q9 is cut off, also. Since Q9 is cut off, the voltage divider composed of R23 and the parallel combination of R21 and R24 holds Q10 off. Consequently, multivibrator Q10-Q11 is in its stable state, with Q10 off and Q11 on.

The circuit is triggered from the quiescent state when an appropriate input at K, R or S drives the base of Q2 positive. Multivibrator Q2-Q3 flips to the temporary state with Q2 off and Q3 on. Diode D4 clamps the collector voltage of Q2 at -3 volts. R11 and C5 couple this -3 volt level to the base of Q4, saturating Q4. The saturation of Q4 grounds its collector.

The grounded collector of Q2 drives the bases of Q5 and Q7 positive. The signal divides at the two bases in order to perform two functions. The signal at the base of Q7 goes to output multivibrator Q10-Q11, driving this multivibrator to its temporary state. The base of Q5 forms part of the feedback loop that returns the signal to input multivibrator Q2-Q3, returning this multivibrator to its quiescent, or stable, state.

As the base of Q7 goes positive, Q7 turns off and Q8 turns on. The common emitter connection of the two transistors rises to the base voltage of Q8. Transistor Q8 turns on but

does not saturate because the rising collector voltage of Q8 is clamped at -5.25 volts by the turn-on of Q9. Transistor Q9 does saturate, and its collector voltage drops to -5.25 volts. Resistor R20 couples this voltage to the base of Q10, turning Q10 on. Multivibrator Q10-Q11 flips to the temporary state, with Q10 on and Q11 off. The output is now in the 1 state, with W at -3 volts, and U at ground.

In the feedback loop to input multivibrator Q2-Q3, R14 drives C7 (and any other capacitor that may be in parallel with it) toward ground. This is the charge mode. When this voltage reaches -1.5 volts, Q5 begins to conduct, raising the common emitter voltage of Q5 and Q6. Consequently, Q6 is cut off. The collector voltage of Q6 goes positive, forward-biasing D5 and cutting off Q3. Transistor Q2 turns on, provided that it is not held off by a continuing negative level at K.

The turn-on of Q2 grounds the base of Q4, cutting Q4 off, and beginning the discharge mode. Before the collector of Q6 can return to its quiescent state, C7 (and any additional capacitor which is in parallel with C7) must discharge, through resistor R13 and potentiometer R10, to a voltage more negative than -1.5 volts. At this point Q6 turns on and D5 becomes back-biased, disconnecting R16 and R17 from the base circuit of Q3. However, the grounded collector of Q2 continues to hold Q3 off.

When the base voltage of Q7 becomes more negative than -4.5 volts, Q7 turns on and Q8 turns off. The -6 volts from the negative supply back-biases Q9 through R19, turning Q9 off. The rise in voltage at the collector of Q9 cuts off Q10, returning the output multivibrator to its stable state. The outputs at W and U return to the 0 state (W at ground and U at -3 volts), indicating the end of the delay.

If the input to Q1 is held at -3 vdc, capacitor C7 charges up to ground and stays there. Thus the output remains in the 1 state. The output returns to the 0 state after a fixed interval following the removal of the negative Q1 input. When input pulses arrive at shorter intervals than the delay period, the output similarly remains in the 1 state, returning to the 0 state after a fixed interval following the last pulse.

10-9 PULSE CIRCUITS

Three modules, clock 4401, crystal clock 4407 and pulse generator 4410 are described in this

section. All three modules produce standard DEC 0.4-microsecond pulses, either positive or negative.

The type 4401 and 4407 clocks produce a continuous train of pulses at predetermined frequencies, and serve as timing devices in the PDP-4 equipment. Pulse generator 4410 utilizes a Schmitt trigger to generate an output pulse whenever its input is triggered. The input may be triggered even by slow, and perhaps irregularly changing voltages. This feature makes the 4410 pulse generator useful in converting sine waves and mechanical switch closures to pulses.

a CLOCK 4401 - This module consists of an astable multivibrator, a pulse amplifier-shaper, and an output pulse amplifier. The multivibrator includes transistors Q1 and Q2; the pulse shaper transistor is Q3 and the output pulse amplifier transistor is Q4. The type 4401 clock generates standard DEC 0.4 microsecond pulses across output terminals E and F at any frequency from 5 cycles to 500 kc per second. The interval from 5 cycles to 500 kc is divided into 5 overlapping ranges; within each range the output frequency is continuously adjustable. The output pulse train may be inhibited by applying -3 vdc to V through a diode whose anode is connected to V.

Potentiometer R4 adjusts the frequency within each range. The range is determined by the amount of capacitance between pins T and V. An external jumper connects one of five capacitors contained in the module into the circuit for this purpose. The frequency range for each of these connections is as follows:

Connection	Frequency Range
T to M	5 cycles to 50 cycles
T to R	50 cycles to 500 cycles
T to P	500 cycles to 5000 cycles
T to N	5 kc to 50 kc
T to U	50 kc to 500 kc

Diodes D1 through D6 determine the operating voltages of the multivibrator. These are silicon diodes with a voltage drop of approximately 0.75 volts each. Because they maintain this voltage drop across a wide range of current flow, multivibrator operation is stable and comparatively independent of the -15 vdc supply. Diodes D1 through D6 hold the base of Q1 at -2.25 vdc and fix the Q1 and Q2 collector supply at -3.75 vdc.

Multivibrator feedback is obtained by connecting T to one of M, R, P, N or U, and jumpering X and Y. An alternative arrangement, which extends the multivibrator frequency range, is to connect an external capacitor between V and T. External fine control may be provided by connecting an external potentiometer between Y and Z.

Because the fine control potentiometer R4 varies the operating point of Q1 over a wide range, a dual collector load is provided for Q1. For low operating current resistor R3 is the principal load, and the Q1 gain is sufficient to maintain oscillation. For high operating current, the principal load is through R2, and Q1 is not driven into saturation.

Multivibrator transistors Q1 and Q2 alternate on and off at a rate that is a function of the RC time constant of the range-determining capacitor (one of C3 through C7) and the series combination of resistor R1 and potentiometer R4. An output pulse is generated during each cycle of the multivibrator when Q2 turns off.

Assume that at a given moment Q1 is turning off and Q2 is turning on. The emitter voltage of Q2 follows the negative-going voltage at the collector of Q1. Capacitor C3 (if T is jumpered to M) couples the negative transient to the emitter of Q1. The feedback from the Q1 collector to its emitter rapidly triggers the multivibrator to the astable state with Q1 off and Q2 on. The secondary of T1 generates a positive pulse at the base of Q3. However, this pulse only drives Q3 further into cutoff, and the output pulse amplifier is not affected.

The multivibrator remains stable in this state while C3 charges through R1 and R4. The Q1 emitter voltage rises exponentially towards ground. When the emitter voltage becomes more positive than the -2.25 volts at the base, the transistor begins to turn on. The Q1 collector-emitter feedback triggers the multivibrator to the other state (Q1 on and Q2 off). The multivibrator remains in that state while C3 charges through R5. Note that if terminal V is held at -3 vdc, Q1 cannot turn on. The multivibrator remains stable with Q1 off and Q2 on until the -3 volts is removed.

At the turn-off of Q2, the collapse of current in the primary of transformer T1 causes a negative pulse to be generated at terminal 3 of the T1 secondary. This negative pulse saturates Q3, grounding terminal 2 of the T2 primary. The output pulse amplifier, composed of Q4, T2 and T3 generates a standard DEC 0.4-microsecond pulse across E and F.

Operation of the pulse amplifier is explained in the description of module 4603 (paragraph 10-6c).

b CRYSTAL CLOCK 4407 - This module contains a crystal oscillator, an oscillator output amplifier, a Schmitt trigger circuit, and an output pulse amplifier. The crystal oscillator includes transistors Q1, Q2 and Q3; transistor Q4 is the oscillator amplifier. The Schmitt circuit includes Q5 and Q6. Transistor Q7 is part of the output pulse amplifier.

The 4407 module generates DEC standard 0.4-microsecond pulses, either positive or negative, at a frequency determined by the series resonance of the oscillator crystal. In PDP-4, clock 4407 has a crystal with a series resonance of 9.6 kc.

Terminal E is the negative output, and F is the positive output. If F is jumpered to ground, E produces a 9.6 kc train of negative pulses. Conversely, if E is grounded, F produces a 9.6 kc train of positive pulses.

Positive feedback from the collector to the emitter of Q1 sustains oscillations in the crystal oscillator. The feedback path goes from the collector of Q1 through crystal CR-1, the two emitter followers Q2 and Q3, to the emitter of Q1. The oscillator output is taken from the collector of Q3.

The circuit oscillates (unity gain around the feedback loop) at that frequency such that the highest proportion of signal voltage is fed back to the emitter of Q1. Crystal CR-1 has minimum resistance at series resonance. Thus the positive feedback is maximum at the series-resonant frequency of CR-1. Gain around the feedback loop is less than unity for other frequencies. Oscillation is therefore sustained only at the series-resonant frequency of CR-1, ie 9.6 kilocycles.

The parallel resonant circuit C1-C2-L1 is tuned in the vicinity of 9.6 kc. The increased impedance of this tuned circuit at resonance compensates for the loss of Q1 collector load impedance at the series resonance of crystal CR-1. This compensation near resonance helps to stabilize the gain of Q1, and assists in tuning the oscillator to the desired frequency. Zener diodes D1 and D2 make the operating voltages of the oscillator circuit independent of supply variations.

The oscillator output to the base of Q4 is amplified at the Q4 collector and applied to the

base of Q5. The Schmitt circuit, Q5 and Q6, converts the 9.6 kc sine wave into a 9.6 kc square wave. The output pulse amplifier, Q7, then converts the square wave into a 9.6 kc train of DEC standard 0.4-microsecond pulses.

The Schmitt circuit and output pulse amplifier are similar to the circuit contained in module 4410 (c below). Each time the sinusoidal output from the Q4 collector drives the Q5 base more negative than -2 volts, Q5 turns on and Q6 turns off. The turn off of Q6 generates a pulse at outputs E-F. Since Q6 turns off and on once for each cycle of the oscillator, the pulses are produced at the oscillator frequency.

c PULSE GENERATOR 4410 - This module contains a Schmitt trigger circuit, an output pulse amplifier, and an RC filter. The Schmitt circuit includes transistors Q1 and Q2; the pulse amplifier transistor is Q3; resistors R1 and R2 and capacitor C1 make up the filter.

Module 4410 generates a standard DEC 0.4-microsecond pulse whenever its input voltage drops from a value more positive than -1 volt to a value more negative than -2.0 volts. If no internal filtering is required, the input is applied to terminal S. However, if the internal filter of the type 4410 is needed (for example, when the circuit is used in conjunction with a mechanical switch), S and U are jumpered and the input is applied to Z. The negative trigger input to Z can then be derived by mechanically switching K to Z. The combination of capacitor filtering and the hysteresis of the Schmitt circuit prevents all but the noisiest contacts from generating more than one pulse per switch closure.

The output terminals of the 4410 are E and F. The output pulse may be either positive or negative. Terminal E generates a negative pulse when F is connected to ground; F generates a positive pulse when E is grounded.

Assume that initially the input (at S or Z) is ground, Q1 is off and Q2 is on. The emitters of Schmitt trigger transistors Q1 and Q2 are held about 1.8 volts negative by the Q2 emitter follower action. The Q2 base voltage is determined by voltage divider R5-R7-R10 and and R11. Diode D3 isolates the emitters of Q1 and Q2 from the -1.0 volt level at the junction of R14 and R15. Diode D1 and resistor R4 couple the ground input level to the base of Q1. Since this base is back-biased, Q1 is cut off.

The collector of Q2 is at -4 volts. The current through the primary of transformer T1 is held steady at about 10 ma, and no voltage appears across the secondary. The base of Q3 is

held at ground by the secondary of T1, and Q3 is cut off. The Q3 collector is at approximately -7.5 volts, and there is no output across E and F.

To trigger the circuit, a negative voltage is applied to the input. Schmitt trigger transistor Q1 begins to conduct as soon as its base becomes more negative than its emitter. This occurs when the input falls below about -2.0 volts. When Q1 starts to conduct, its collector voltage rises towards ground.

Resistor R7 and capacitor C2 couple the rising collector voltage of Q1 to the base of Q2, thereby cutting off Q2. Turn-off of Q2 makes the common emitter connection of Q1 and Q2 more positive, speeding the turn-on of Q1. This positive feedback of the Schmitt trigger circuit assures a fast change of state, independent of the fall time of the input signal.

With the turn-off of Q2, the current through the primary of transformer T1 collapses, inducing a negative pulse at terminal 4 of the T1 secondary. This negative pulse is amplified by pulse amplifier Q3 and appears across outputs E and F. The pulse amplifier shapes the output pulse to 2.5 volts in amplitude and 0.4 microsecond in duration. The polarity of the pulse depends on whether E is grounded (for a positive pulse) or F is grounded (for a negative pulse).

When the Q1 base input again rises towards ground, the Q1 emitter follows this voltage until the base is at approximately -1 volt. At this point, D3 again starts to conduct, clamping the emitter voltage. Further rise of the input voltage cuts off Q1. As the Q1 collector goes negative, this voltage drop is coupled through R7 and C2 to the base of Q2, turning Q2 back on, and thereby returning the trigger circuit to the initial state. This reestablishes current through the primary of T1, and induces a positive pulse at terminal 3 of the T1 secondary. This positive pulse, however, only drives Q3 further into cutoff and the output pulse amplifier is unaffected. Diode D2 and resistor R9 prevent ringing in T1.

10-10 PLUG ADAPTERS 1956 AND 1956R

These two plug adapters are plug-in units that have a 10-pin plug at the module back panel (only nine pins are used), in addition to the standard 22-pin plug located at the front panel. Internal wiring connects each pin of the back panel plug to a pin of the front panel plug. Both types of adapters are used to bring the rear plug connections of the 4203 flip-flop to the

front of the mounting panel.

The PDP-4 includes only three adapters. A single 1956 adapter couples the rear plug of the link flip-flop (type 4203) to the front of the mounting panel. Two 1956R adapters couple the accumulator rear plugs (also 4203 flip-flops) to the front. One 1956R adapter is located at each end of the accumulator, and parallel bus connections are made between the rear plugs of the adapters and the register flip-flops.

The 1956R adapter differs from the 1956 adapter in that eight of the nine internal jumpers between the back and front panel plugs are grounded through resistors. These resistors serve as terminating resistances for pulsed lines. All the resistors are 100 ohms, except the two that connect lines C*-L and E*-R to ground. These two resistors are 47 ohms. The connection between D* and N carries levels, not pulses, so it requires no terminating resistor.

10-11 POWER SUPPLIES AND CONTROLS

The PDP-4 power supplies convert standard 110 vac to dc power at the appropriate voltages for the computer circuits. The supplies include type 728, 734 and 735. Power supply control type 1701 and the type 735 supply are functionally a single supply unit. Power control 813 controls the application of power to the computer.

a POWER SUPPLY 728 - This unit supplies the +10 vdc and -15 vdc power required by most of the PDP-4 modules. Two type 728 supplies, with their -15 vdc outputs connected in series, furnish -30 vdc for the 4681 solenoid drivers.

The outputs of the 728 supply are +10 vdc (0 to 7.5 amperes), or -15 vdc (1 to 8.5 amperes). When both outputs are used concurrently, the current limitations are more stringent. All three of the following limitations then apply:

(1) +10 vdc limited to between 0 and 7.0 amps

(2) -15 vdc limited to between 1 and 8.0 amps

(3) Both outputs limited by the relationship:

$$5I_{(+10)} + 6I_{(-15)} \leq 53$$

The +10 volt output is regulated between +9.5 vdc and +11 vdc; the -15 volt output is regulated between -14.5 vdc and -16 vdc. Assuming line voltage variation from 105 to

125 vac, this regulation holds from minimum to maximum load. Output ripple is less than 350 millivolts.

The line voltage is stepped down to 10-0-10 vac and 15-0-15 vac by transformer T1. Diodes D2 and D3 are connected to the 10 volt secondary taps as a positive full-wave rectifier. Capacitors C2 and C4 filter out the ac component of the output. Resistor R1, in parallel with the 10 volt load, keeps the output within regulation tolerances even though the external load is decreased to the no-load condition.

Diodes D1 and D4 are connected to the -15 volt secondary taps of T1, as a negative full-wave rectifier. Capacitors C1, C3, C5 and C6 filter out the ac component.

Special properties of transformer T1 make possible the simple design of the power supply. T1 is a saturated-core transformer which provides inherent overload protection. Even with shorted outputs, only a limited output current can be drawn. This self-limiting secondary current eliminates the need for series impedance elements at the filter inputs. The dc output impedance of the supply is thus kept low, rendering regulating devices unnecessary.

b VARIABLE POWER SUPPLY 734 - This power supply furnishes dc power for marginal checking of PDP-4 modules. For a nominal 110 vac input, output voltage is continuously variable from 0 to 20 vdc (no load). Maximum voltage output drops 3 volts at full-rated load of 2.5 amperes.

Line power at 110 vac is stepped down by transformer T1. (Only the terminal 3 and 4 half of the secondary is used.) The voltage at the secondary is applied to terminals 1 and 5 of Variac M5. By adjusting the position of the terminal 3 tap, any voltage within the range of 0 to 20 vac is available between terminals 3 and 4. Output voltage is increased by rotating the Variac control clockwise. The Variac output is applied to a bridge rectifier (diodes D1 through D4).

The rectifier diodes are oriented so that the dc output of the bridge at the junction of D2 and D4 is positive with respect to the junction of D1 and D3. Parallel capacitor C1 filters the output. Voltage regulation is improved for small load currents by parallel resistor R1. A slow-blow 5-ampere fuse at the positive output protects the supply against overload. The dc output voltage is indicated on a 0-30 vdc meter across the output.

c POWER SUPPLY 735 - This supply provides power to the PDP-4 memory logic. The input voltage requirement is a nominal 110 vac. Outputs are -3 vdc (terminal B), -13 to -16-1/2 vdc (C and D), and -35 vdc (E). A +10 vdc level is generated for use by the internal shunt regulator circuits, and for use by power control 1701. Terminals C and B are the inhibit voltage supply output; D and B are the read/write voltage supply outputs.

Since the read/write and inhibit voltages must be well-regulated, compound connection shunt regulator circuits are used across these outputs. The bases of shunt regulator transistors Q1 and Q3 are brought to terminals F and N (for connection to power control 1701) rather than to their respective output voltage points. Besides regulating the output voltages, the connection to the 1701 control serves two other functions. The 1701 circuitry varies the output voltage in accordance with the temperature of the core stack. Furthermore, the 1701 control permits adjusting the output voltage to the individual requirements of a specific core stack.

The inhibit and read/write supplies are very much alike. They differ, however, in that the inhibit supply output current varies over a wider range. Whereas the read/write supply output current varies only from 0 to 0.4 amperes, the inhibit supply output must vary from 0 to 3.0 amperes. Consequently, both the inhibit supply series dropping resistance (R1-R2) and also the emitter resistor R4 of the principal shunting transistor Q4, are smaller than the corresponding resistors in the read/write supply.

Transformer T1 steps down the 110 vac input to 10-0-10 vac, and to 35-0-35 vac. Diodes D2 and D3 are connected as a positive full-wave rectifier to the 10 volt secondary taps. Capacitor C5 filters the dc output of the rectifier, which is then applied to the emitter circuits of Q1 and Q3, and to terminal A of power control 1701. Diodes D1 and D4 are connected to the 35 vac secondary terminals as a negative full-wave rectifier. Capacitor C3 filters the rectified -35 vdc output at E.

This -35 vdc also provides the negative input to both the inhibit and read/write supplies. The positive input to these two supplies is -3 vdc from terminal B. This voltage is generated by the forward voltage drop across four series-connected diodes D5, D6, D7 and D8. The anode of D5 is connected to the grounded center tap of T1. Because the inhibit and read/write supplies are similar, the following description of the read/write supply also adequately describes the inhibit supply.

The base of shunt-regulator transistor Q1 is biased from terminal F of the 1701 control. The operation of the 1701 control is fully described in f below. However, to understand the regulating action of transistors Q1 and Q2 it can be assumed for the time being that the base of Q1 is biased through a connection to the terminal D output of the supply. Although this connection is in fact made through the 1701 control circuitry, the bias feedback functions in much the same way as if the feedback connection from output D were instead made through a battery, reference diode, or resistance.

If the output voltage rises, either because of an increase in the supply load, or because of a rise in the regulator input voltage, then the base voltage of Q1 also rises. Conduction through Q1 decreases, and the Q1 emitter voltage rises with the base voltage. Consequently, conduction through Q2 also decreases. The decrease in conduction through the two transistors (chiefly Q2) tends to restore the original voltage at D. Similarly, a fall in the output voltage is counteracted by increased conduction in the shunt regulator. Capacitor C6 provides a low output impedance for transient loads.

During normal circuit operation, Zener diode D8 does not conduct. This diode is used solely as a protective device. In the event that conduction through Q1 or Q2 is seriously impaired by a malfunction, the circuit output voltage would, in the absence of D8, tend to fall towards -35 vdc. To avoid such a large negative output voltage, and the resulting possibility of damaging other computer memory elements, Zener diode D8 is used to clamp the terminal D output to a maximum negative value of -17 vdc with respect to terminal B.

d POWER SUPPLY CONTROL 1701 - This unit controls power supply 735. The 1701 module contains two identical circuits. One of these two circuits controls the 735 inhibit supply, and the other controls the 735 read/write supply. Since both the inhibit and read/write supplies function in the same way, the following description of the read/write control circuit (in the lower half of the schematic) applies equally to the inhibit control circuit (top half of schematic).

Terminal E of the 1701 control is connected to the -3 vdc common of the 735 power supply. Terminal H is connected to the nominal -13 vdc output of the read/write supply. Terminal A receives +10 vdc (from the 735 supply). Terminals V and W are control terminals. When V is jumpered to W, the temperature coefficient of the regulation in the 735 supply

is -0.5% per C^{o}. When this connection is left open, the temperature coefficient is -0.8% per C^{o}. The control output is at F.

As an adjunct to the 735 read/write supply, the control circuit performs three functions. First, the terminal F output biases the base of shunt regulator transistor Q1 in the 735 supply. This bias determines the read/write output voltage. The bias, and the resulting read/write output, can be adjusted by a potentiometer.

Second, a thermistor (placed in the environment of the memory core stack) makes the bias temperature-dependent. Because the thermal coefficient of this thermistor is negative (-4.4% per C^{o}), the read/write output voltage is a negative function of temperature. As the temperature of the core stack increases, the read/write voltage and current decrease. This temperature compensation corrects for the fact that the higher the core temperature, the smaller the core winding current that is needed to switch a memory core.

The third function of the control circuit is to compensate for changes in the read/write voltage that are caused by variations in the load and in the supply input voltage. The control circuit serves to further compound the shunt regulator contained in the 735 read/write supply.

Transistors Q4 and Q5 make up a difference amplifier. The change in voltage at the collector of Q5 is proportional to the voltage difference between the bases of Q4 and Q5. Bias control levels from the potentiometer enter the difference amplifier at the base of Q4. Bias control levels determined by changes in the resistance of the thermistor are applied to the base of Q5. The feedback, or regulation signal, also enters the difference amplifier at the Q5 base.

The series combination of control potentiometer R13 and resistor R12 is in parallel with a 6.2 volt Zener reference diode. This double-anode Zener diode provides the basic voltage reference used by the circuit. The reference diode has extremely good temperature stability. Voltage across it remains nearly constant for normal variations in ambient temperature, and for wide variations in current.

Counterclockwise rotation of the potentiometer varies the base voltage of transistor Q4 from -9.2 volts to approximately -6.5 volts. Rotating the potentiometer counterclockwise decreases the read/write output voltage; clockwise rotation increases the output

voltage. The potentiometer controls the output voltage in the following manner. Assume that the potentiometer is rotated counterclockwise. The Q4 base voltage then becomes more positive, decreasing conduction through Q4. Conduction through Q5 then increases, raising the base voltage of NPN transistor Q6. This increases conduction through Q6, and thus lowers the bias output at F. The more negative output at F causes increased conduction in the 735 read/write shunt regulator transistors, thereby decreasing the read/write output voltage. Clockwise rotation of the potentiometer increases the supply output in exactly the opposite manner.

To understand the way in which the control circuit compensates for temperature changes, assume that while the Q4 base voltage remains constant, the temperature increases. The increasing temperature produces a decrease in the value of the thermistor (connected between J and K). As the resistance of the thermistor decreases, the Q5 base voltage also decreases, increasing conduction through Q5. The bias output at F decreases, thus reducing the supply output voltage. Decreases in ambient temperature produce an increased output voltage in exactly the opposite manner.

Connected across the supply output is a voltage divider, comprising the thermistor and resistors R16, R17, R18 and R19. The supply output voltage is fed back to the base of Q5 through this voltage divider, thereby regulating the output over variations in load and input voltage. In a sense, therefore, Q5 provides the first stage of a compound shunt regulator. The final stage of this compound regulator is Q2 (in the 735 supply).

If, for example, the supply voltage becomes more negative, then the base of Q5 also goes negative, increasing conduction through Q5. This causes the Q6 base voltage to rise, and increases conduction through Q6. The output F bias voltage then drops, increasing conduction through the shunt regulator transistors in the 735 supply. This causes the output voltage of the 735 supply to rise to its original correct value. Positive deviations in output voltage are corrected in exactly the opposite manner.

e POWER CONTROL 813 - This unit is the main power control for the PDP-4 equipment The 813 unit applies memory system power separately from the power to the rest of the computer. Delayed relay switching in the control turns on memory power 5 seconds after the turn-on of computer power, and turns off memory power 5 seconds before turning off

computer power. Consequently, turn-on and turn-off transients in the computer equipment cannot disturb memory core states.

The 813 unit also provides two control signals: a timed ground level, and a 6.3 vac timing signal. The ground level is established for 5 seconds at terminal 7, beginning when computer power is turned on, and beginning again when memory power is turned off. This ground level enables the power clock (paragraph 6-2a). The 6.3 vac signal, provided whenever memory power is on, furnishes 60 cycle timing to the real time clock (paragraph 9-2d).

The 813 power control may be used with either 110 vac or 220 vac. If the 813 is used with 110 vac, the two H input terminals are jumpered, and the 110 vac is applied across H and N. For a 220 vac input, N is the ground connection, while the H terminals are the two hot connections to the 220-volt line.

The memory power output is at terminals A-B. All other ac power for the computer is furnished across C-D and D-F. The 6.3 vac output is at terminals 3 and 4. Terminals 5 and 6 are not used.

Four relays, D1, D2, K3 and K4, establish the switching sequence within the 813 control. The D1 contacts close instantaneously, but open after a 5-second delay. The D2 contacts close only after a 5-second delay, but open instantaneously. Both K3 and K4 are instantaneous on-off relays.

Normally ac line voltage is present at inputs H and N. The power control is turned on by closing the power switch on the console. Relay D1 is then energized. Contacts 2-3 of D1 close immediately, energizing K3. All three sets of K3 contacts close at once, applying 110 vac across outputs C-D and D-F. All the computer equipment fed by these outputs is then energized.

Five seconds after the D1 contacts close, D2 contacts 2-4 close. Unless the memory power switch is open, relay K4 then energizes, closing both sets of K4 contacts. This supplies 110 vac to memory power output A-B. Filament transformer T1 steps down the 110 vac at A-B to provide 6.3 vac at output terminals 3 and 4.

During the five seconds while D1 contacts 6-7 are closed and before D2 contacts 6-7 have opened, terminal 7 is grounded. At the end of the five seconds, contacts 6-7 of D2 open,

disconnecting the ground level at pin 7.

When the console power switch on the console is turned off, relays D1 and D2 are de-energized. Contacts 2-4 of D2 open immediately, de-energizing K4. This relay immediately disconnects power output to A and B, thus turning off memory power, and the 6.3 vac output at terminals 3 and 4. Five seconds later, D1 contacts 2-3 open, de-energizing K3. All three K3 contacts open immediately, interrupting power to outputs C-D and D-F and thus turning off the computer.

During the five-second turn-off delay, contacts 6-7 of D1 and 6-7 of D2 are both closed, grounding terminal 7. At the end of the five seconds, contacts 6-7 of D1 open disconnecting the ground at pin 7.

The memory power switch permits the operator to turn off memory power while the rest of the computer power is still on. Circuit breakers CB1, CB2 and CB3 provide overload protection. With a 110 vac input, CB2 limits the combined load at all three power outputs to 50 amperes.

With a 220 vac input, CB1 limits the combined load at A-B and C-D to 25 amperes, while CB3 limits the load at D-F to 25 amperes. Meter M is an elapsed time meter which provides an indication of the total time in hours that computer power is on. Both input and output power line filters are used; these are shown on the print as boxes F1 through F8.

CHAPTER 11

MAINTENANCE

11-1 SPECIAL TOOLS AND TEST EQUIPMENT

The following special tools and test equipment are recommended for the efficient maintenance of the PDP-4 computer.

Multimeter	Simpson Model 260A, Triplett Model 630NA, or equivalent
Subminiature alligator clips	Mueller type 30 or equivalent
Oscilloscope	Tektronix 540 series with type CA plug-in vertical amplifier, or equivalent
Long-lead probes	Tektronix P-6002 or equivalent
Current probe	Tektronix P-6016 or equivalent
Paper tape gauge	Friden type T-18118, or equivalent
Plug-in puller	DEC type 1960*
Plug-in extender	DEC type 1954*
Pigtail plug-in extender	Modified DEC type 1954
Soldering iron	6 vac iron with isolation transformer

* Digital Equipment Corporation furnishes one of each of these units without charge with each PDP-4 computer.

Included in the above list is the pigtail plug-in extender. This maintenance aid can be readily fabricated from a standard DEC type 1954 unit extender. Disconnect the small wire leads to terminals A, B, and C of the unit extender, and solder eight-foot leads to the three terminals. Solder aligator clips to the free ends of the three eight-foot leads. Terminals A and B can then be connected to the 10-volt marginal check power supply. Terminal C can be connected to the 15-volt marginal check supply. This permits convenient marginal testing of an

individual circuit card Either the A or the B portion of the card can be separately checked, thereby permitting submodular testing.

11-2 EQUIPMENT LAYOUT AND WIRING

Figure 11-1 shows the detailed physical layout for all of the logic comprised by the standard PDP-4, the real time option, and the control units for the reader, punch and keyboard/printer. Figure 11-1 shows the position of logic circuits only; locations of power control panels and power supplies are shown in Figure 11-7. Each mounting panel in Figure 11-1 is divided into sections according to logical function. Unlabeled areas bounded by solid lines indicate sections of the mounting panel in which no modules are installed. Areas that are labeled by logic function and separated by dashed lines represent circuits all of which appear on the same logic print (block schematic). Figure references are included as two-part hyphenated numbers at the lower left of each logic section bounded by solid lines.

Two module layout drawings, Figures 11-2 and 11-3, show the module types normally installed in every mounting panel location. Figure 11-2 is the module layout for the standard PDP-4 system, including the memory and the reader control logic. Figure 11-3 is the module layout for the optional equipment: the real time option, the magnetic tape control, the control units for the punch and keyboard/printer, and the adapters for the line printer and card reader. Figure 11-3 also shows the positions of modules that are added to the PDP-4 internal processor when the type 17 memory option is installed.

The console wiring and circuits are shown in Figures 11-4 and 11-5. Figure 11-4 is a schematic of the wiring for the console keys and speed controls. Figure 11-5 shows all indicators, address and accumulator switches, and operating switches. In Figure 11-5, the rear view shows the console terminal strips, giving two-digit numbers (60, 61, etc.), each prefixed by the console panel designation 0G. In cable diagrams, these 0G60-series numbers indicate the cable destinations at the console.

Figure 11-6 is the cable diagram for the entire PDP-4 system, including the real time option, magnetic tape control, and control logic for the paper tape reader and punch, the keyboard/printer, card reader, card punch, CRT display, and high-speed line printer. All mounting panels in the central frame (both bays) are shown with references to prints showing the wiring, cabling and logic contained in each panel. The in-out devices are shown as smaller blocks at

the left in Figure 11-6. The source and destination of all cables are shown, with references to cable lists that show the connections and logical functions of each cable. The diagram also shows the type of connector used to terminate each cable.

The AC and DC wiring diagram, Figure 11-7, shows the power wiring configuration for a PDP-4 that includes the type 25 real time option and the reader, punch, and Model 28 Keyboard/Printer. The -15 vdc line from the type 728 power supply located in 1E rear is wired in series with the -15 vdc line from the type 728 located in 1D rear; this provides the -30 vdc required by the solenoid drivers for the punch and keyboard/printer. In a PDP-4 using only the reader, the 728 supply in 1E rear is not used. The type 728 supply in 2E rear supplies the +10 and -15 vdc for the type 25 real time option and the memory system (panels 2A to 2H). When additional in-out device control units are installed (in panels 2K to 2M), an additional type 728 power supply is required. This additional supply is installed in location 2ER, and supplies power for panels 2E to 2M. When the supply in 2ER is installed, the type 728 supply in location 2DR is reconnected to supply only the memory system, panels 2A to 2D. The power supplies for the type 17 memory expansion are located in bay 3, and are not shown in Figure 11-7.

11-3 LOGS

Properly kept and adequately detailed logs are absolutely necessary to good maintenance. If a malfunction should occur, the first step in troubleshooting is to obtain all the available information about the fault. The machine log is a vital part of the information pertinent to a troubleshooting problem. The standard PDP log format used by DEC, and available from DEC to PDP-4 users, is shown in table 11-1. During normal computer operation, the most important items to be logged are:

(1) The times at which computer power is turned on and off;

(2) The elapsed time meter reading when power is turned off;

(3) The name of the person or department using the computer during normal computing time;

(4) The times at which the user began and finished his use of the computer;

(5) The name or type of program run, or the category of machine use (e.g., program development, debugging, etc.).

The reverse side of the PDP log is reserved for entries in the maintenance record. The main-

tenance record must include every observation about machine performance not already entered as a comment on the front side of the log; and it must include complete descriptions of everything done to the machine, apart from normal operation, for whatever reason. In particular, the maintenance record must at least include the following:

(1) Complete descriptions of machine performance under marginal check, giving the name of the program run, the panels to which margin voltages are applied, the power lines supplied with margin voltages (e.g., +10A, +10B, or -15C), and the margin levels at which failure is observed. Entries describing marginal check performance should be made regardless of the reason for performing the check.

(2) The exact times of beginning and end of computer down-time.

(3) Complete and detailed reasons for computer down-time. This entry should include a description of the malfunction that causes down-time, if any.

(4) In the case of malfunction, a detailed description of the steps taken to trouble-shoot the malfunction.

(5) All steps taken to remedy a fault (e.g., replacements, repairs, etc.)

Maintenance record entries must not necessarily be restricted to the categories given above. It is extremely important to log any machine behavior pattern or symptom, even if it does not seem immediately pertinent to a machine malfunction. For example, if the operator notices excessive vibration in the punch -- even if such vibration is not accompanied by malfunction -- this observation should be noted in the maintenance record. If the operation log (front side) indicates that a particular circuit breaker must be reset frequently over a short period, this should be entered in the maintenance record. Entries of this nature may seem insignificant or frivolous at the time they are noted, but if these symptoms later aid in troubleshooting a related malfunction, the entries do not appear silly in the least.

A properly kept maintenance record reveals at a glance the previous history of failures throughout the entire system. Maintenance record entries often show patterns of consistency among failures that seem totally unrelated. In troubleshooting, completely new lines of attack are often suggested by such patterns of consistency. To take best advantage of previous malfunction experience, the maintenance record must be kept up to date accurately and faithfully.

In any case of doubt as to whether an observation is important enough to put in the maintenance

PDP LOG

POWER	TIME ON					DATE
	TIME OFF					

USER	TIME ON	TIME OFF	COMMENTS	ELAPSED TIME METER READING AT POWER OFF

TABLE 11-1 SAMPLE OPERATION LOG FORMAT

MAINTENANCE RECORD

record, enter it. The maintenance record is the only source of information on the history of machine performance. Information from the maintenance record almost always saves time troubleshooting malfunctions later, but if the information is not entered, the record is useless. Always enter everything in the maintenance record; this way, everything important is sure to be there.

11-4 ADJUSTMENT AND CALIBRATION

All DEC systems are designed for maximum reliability under a wide range of operating conditions. Very little adjustment or calibration is required. The following procedures may be carried out as corrective maintenance if necessary; but they should not be performed as routine periodic checks.

a. ADJUSTABLE TIMING CIRCUITS - There are three types of adjustable timing circuits used in the PDP-4: the types 4301 and 4303 adjustable delays, and the type 4401 clock. All other delay modules used in PDP-4 contain distributed-constant delay lines. Delays of this type cannot be adjusted.

The type 4303 integrating single shot module is used in the timing logic of the PDP-4 (Figure 6-1). Normally the delay range is determined by selecting one of five capacitance values. Pin D is the capacitor selection terminal. The shortest delay range is determined by making no connection to pin D. The four successively longer delay ranges are selected by connecting pin D to pins E, F, H, and J, respectively. Fine adjustment of the delay is made at the screwdriver trimpot behind the access hole in the type 4303 module frame. Delays longer than 0.9 seconds may be obtained by connecting an external capacitor between pins D and M. If desired, an external potentiometer may be used instead of the trimpot; in this case the external potentiometer is connected between pins X and Z. Figure 6-1 shows the type 4303 used in the PDP-4 timing logic. The delay adjustments described above are made by the speed controls at the console.

The type 4401 module is the power clock shown in Figure 6-1 D6. This module is adjusted at DEC to a frequency of about 25 kilocycles. The output frequency of the type 4401 clock may be adjusted at the trimpot behind the access hole in the aluminum frame of the module. The type 4401 should not need adjustment unless it is replaced.

Two type 4301 single-shot delay modules are used in the PDP-4. One provides the 10-microsecond delay between SP0 and SP1P in the timing logic (Figure 6-1). The other provides a 5-millisecond delay in the punch logic (Figure 9-6)

The duration of the delay in the type 4301 module is adjusted by observing the duration of the level output at pin J. Connect an oscilloscope with a calibrated sweep to pin J. Trigger the sweep internally, and set the sweep time per centimeter adjustment so that the entire duration of the level output is displayed. The duration of the negative going level at pin J is adjusted to the required delay by means of the screwdriver trimpot adjustment. An access hole is provided for the screwdriver in the aluminum frame of the type 4301 module.

b POWER SUPPLIES - The PDP-4 contains two types of variable power supply. These are the type 734 marginal check power supply and the type 735 memory power supply. The type 734 power supply provides the marginal check voltage, variable from 0 to 20 vdc. The output polarity of the supply is determined by the setting of the polarity switch on the marginal check switch panel. The voltage adjustment is at the knob at the front panel of the type 734 supply at the top rear of bay 2. This marginal check supply adjustment is used routinely in marginal check procedures.

The type 735 memory power supply adjustments are made at the type 1701 plug-in module (part of the supply). The type 1701 module has two access holes for screwdriver adjustments. The adjustment through the center hole is the read/write current adjustment. The adjustment through the bottom hole is the inhibit current adjustment. For the 8K memory, there are two complete type 735 power supplies, each with its associated type 1701 plug-in control (paragraph 10-11c and d). These 735 supplies are each adjusted independently.

Type 735 memory supply adjustments are always made for current output. Never adjust the 735 supply for voltage output. These current adjustments should not be altered unless there has been trouble with the regulation of the supply; both the inhibit current and the read/write current adjustments are set accurately during manufacuture. Subsequent adjustment is seldom required.

If memory malfunction has been isolated to insufficient or excessive read/write current or inhibit current, the type 735 supply may be adjusted by the following steps.

(1) Set the ACCUMULATOR and ADDRESS switchs to zero. Turn REPEAT on. Set the SPEED controls to the fastest repetition rate. Have someone hold the DEPOSIT key up. (If you are alone and cannot prop up the DEPOSIT key, deposit the instruction "jump to 0000" (60 0000) in location 0000. Press the START key.)

(2) Attach an oscilloscope current probe to the wire originating at pin W of the type 1972 read/write switch in location 2A1. Set the sweep to 1 microsecond per centimeter and trigger the sweep on T1 (available at one of the insulated standoofs in panel 1A). The oscilloscope then displays the read current waveform, followed immediately by the write current waveform which is of opposite polarity.

(3) Adjust the current probe to give a calibrated deflection of convenient amplitude. Check both the read and write current waveforms for the current values given in Table 11-2 below. Do not yet alter the adjustments at the type 735 memory power supply.

(4) Turn on AS_{17}. (If you are alone and cannot prop up the DEPOSIT key, halt the computer and deposit the instruction "jump to 0001" (60 0001) in location 0001. Again press the START key.

(5) Attach the current probe to the wire originating at pin X of the type 1972 read/write switch in location 2A1. Again check the read and write current waveforms against the values given in Table 11-2 below.

(6) If both the read current and write current waveforms as observed at pin W and pin X of the type 1972 read/write switch are both too great or too small by roughly the same amplitude, then the type 735 memory power supply needs adjustment. Adjust the screwdriver trimpot through the center hole of the type 1701 plug-in so that both the read and the write current waveforms have the value shown in Table 11-2 below. This adjustment controls both the read and the write current waveform. The read current may be adjusted two or three milliamps high if necessary to obtain the proper value for write current (or vice versa).

(7) Return AS_{17} to zero. With the current probe, observe the inhibit current waveform at pins W, X, Y, and Z of the type 1982 inhibit driver located in 2C10. The

peak inhibit current amplitude should correspond to the value shown in Table 11-2. The type 735 memory power supply should be readjusted only if the inhibit current at all four pins is too great or too small by the same amount.

(8) If the inhibit current adjustment is required, adjust the screwdriver trimpot through the bottom access hole in the type 1701 power supply control plug-in. The inhibit current amplitude should be checked after adjustment at all inhibit driver output pins.

(9) If you are alone and are using jump instructions to pulse the memory, check the inhibit current at pins W and X (location 2C5) by depositing the instruction jms 0000 (10 0000) in location 0001. Since MB_0 and MB_1 are both 0 in this instruction, the inhibit current levels may be checked at pins 2C5W and 2C5X.

TABLE 11-2 NOMINAL VALUES,* MEMORY READ/WRITE, AND INHIBIT CURRENTS

Core-stack Manufacturer	Read/write Current	Inhibit Current
RCA	180 ma.	165 ma.
Ampex	180 ma.	165 ma.
General Ceramics	180 ma.	165 ma.
Ferroxcube	200 ma.	180 ma.

* Optimum current values are listed on a label at the rear of the core-stack. These values are determined at DEC for best performance under margins.

c SENSE AMPLIFIERS - Each PDP-4 memory system contains 18 sense amplifiers. There are two types: the type 1538, and the type 1540. All 18 sense amplifiers in a memory system are of one of the two types; they are never mixed. The procedures for adjusting the two types are identical; however, the locations of the adjustments differ.

On the type 1538: the BALANCE adjustment is made through the lower access hole;
the SLICE adjustment is made through the upper access hole;
the MARGINAL CHECK toggle switch at the bottom of each

module frame is used to apply margin voltage.

On the type 1538: the BALANCE adjustment is made through the upper access hole; the SLICE adjustment is made through the lower access hole; marginal check voltage is applied to all 18 modules by the SENSE AMP switch on the marginal check switch panel.

The sense amplifier adjustments are made as follows:

(1) Using an oscilloscope with a differential preamplifier, observe pins T and V of the 1538; S and U of the 1540. Set the preamplifier of the oscilloscope to display the differential waveform between the two pins (on Tektronix type CA preamp, set to "add algebraic" and invert one but not both inputs).

(2) Run the memory Checkerboard program. Do not use the worst pattern portion of the Checkerboard program, since this pattern generates severe drift in the scope display.

(3) Set the duration of the scope trace so that one entire memory cycle is displayed: 1 microsecond/centimeter. Sync at T1.

(4) Adjust the BALANCE to minimize the noise injected at T5 and T7. These timing pulses correspond to the turn-on and turn-off times of the inhibit current. As the correct adjustment is approached, the sense preamplifier output broadens and increases in amplitude. Often the strobe pulse, 0.7 μs after T2, may be seen as a pip near the center of the sense preamplifier waveform.

(5) Remove the oscilloscope probes, and using one probe, observe pin M. This pin provides a -3 vdc logic level from the slicer section of the sense amplifier.

(6) Stop the computer and restart at the location corresponding to the memory Checkerboard worst pattern.

(7) At the marginal check switch panel just below the type 734 marginal check power supply, turn on the first switch at the left. This switch applies marginal check supply

voltage to the +10A line for the sense amplifiers. Marginal check voltage is applied to individual type 1538 modules using the toggle switch on the type 1538 module frame. The type 1540 has no such switch; margin voltage is applied to all 18 type 1540 modules by the switch at the marginal check switch panel.

(8) Have someone stand by the type 734 marginal check supply to vary the voltage and call out meter readings. The lower the voltage of the supply, the greater is the likelihood that spurious bits are generated; the higher the voltage of the supply, the greater is the likelihood of losing bits.

Adjust the SLICE control so that bits are lost and "picked up" at marginal check voltages symmetric about the nominal +10 vdc level. As the marginal check voltage is decreased, the duration of the logic level at pin M is seen to increase until eventually a spurious thinner noise burst appears within, representing the spurious 1 level sensed from a core containing 0.

As the marginal check voltage is increased, the -3 volt logic level at pin M narrows, and eventually either falls or becomes so narrow as to exclude the strobe pulse. When this happens, the sense amplifier pulse output is absent regardless of the state of the sensed core; the bit is lost. The SLICE must be adjusted so that the voltages (as provided by the marginal check supply) at which bits are lost and picked up, are symmetric about the nominal +10 volts.

d. TAPE READER AMPLIFIERS - All nine reader amplifiers are mounted on one printed circuit board located on the reader chassis. They are shown in Figure 2-2 of the Digitronics Perforated Tape Reader Model 2500 manual dated June 1962.

Before making adjustments on the reader amplifiers, the reader itself should be checked for proper mechanical operation. The reader amplifier adjustments affect the timing and duration of the reader amplifier output levels. However, the intensity and duration of the light impulse sensed by the reader photodiodes also affect these same output levels. Therefore, before adjusting the reader amplifiers, the following four steps should be performed.

(1) Check the lateral registration of the punched holes in the tape with respect to the

tape edge. Use the Friden tape gauge type T-18118. Insert the gauge pins into the tape feed holes and check that the tape lies in the gauge with the edge nearer the feed holes snug against the raised shoulder of the gauge.

(2) Remove the upper read head cover. Thread the tape through the tape guides on both sides of the read head, but pass the tape over the capstan on the left, and over (not through) the brake assembly on the right. Position the tape lengthwise so that the feed hole of the tape is over the feed hole photodiode in the read head. Set the tape guide knob to READY. Check for lateral registration at the feed holes. The tape feed hole should not be out of registration laterally by more than 10% of its diameter.

(3) With reader power on, check that the exciter lamp has not become yellow. If the light is not white and bright, replace the lamp. Check that the light beam falls directly on the row of photodiodes (the tape need not be loaded). The light beam adjustment procedure is described in paragraph 5.5.3 of the Digitronics Model 2500 manual.

(4) Replace the read head cover.

If the mechanical operation of the reader is satisfactory, the tape reader amplifiers may be adjusted as described below.

Adjustments to the tape reader amplifiers are made at the nine screwdriver trimpots mounted on the amplifier card (LAC).

The amplifier output levels should be observed with an oscilloscope having a dual-trace preamplifier. A closed loop of tape having alternate lines punched with 1s and 0s should be used. The adjustment procedure is as follows.

(1) Sync the oscilloscope sweep to the negative-going leading edge of the waveform at pin S of the pulse generator in location 1K14. This signal is the output of the tape reader feed hole amplifier. Set the sweep to 10 ms/cm so that the signal from three lines on the tape is displayed.

(2) Run the closed tape loop of 1s and 0s continuously. This may be accomplished by

putting the instructions rsa (70 0104), rsf (70 0101), jmp (60 0001), and jmp 0000 (60 0000) in memory locations 0000, 0001, 0002, and 0003, respectively. Start the machine at 0000.

(3) With one oscilloscope channel, observe the waveform at pin 1K14S (in parallel with the sync probe). Three negative-going levels are displayed. These are the feed-hole levels.

(4) Adjust the feed-hole amplifier on the reader chassis to provide negative-going output levels of duration between 1.3 and 1.4 ms.

(5) Set the oscilloscope preamplifier to switch channels on alternate sweeps. With the second scope channel, observe the data channel amplifier outputs (one at a time) at pins F, K, N, S, V, and Y of location 1K09, and at pins U and X at location 1K12. The display should show the two 1.3+ ms. feed-hole levels and one data-channel negative-going level of longer duration, corresponding to the line of holes on the tape.

(6) Adjust the data-channel amplifiers for a logic level duration of 2.3 to 2.4 ms.

(7) Check that the trailing edge of the negative data-channel level is at least 0.3 ms. later than the trailing edge of the feed-hole level. This completes the adjustment procedure.

11-5 RECOMMENDED SPARE PARTS

The most economical quantity of spare parts to be maintained depends on the requirements of the individual user. Spare module stocks for the PDP-4 used one shift per day need not be as large as spare stocks for the PDP-4 used two or three shifts per day. Similarly, in applications that permit only minimal down-time, the stock of spares must be greater than the stock required when more down-time can be tolerated. Paragraphs a, b, and c below discuss recommended spare allowances for modules, circuit components, and in-out equipment, respectively. Paragraph d gives recommended mechanical spare allowances.

a MODULE SPARES - For single shift applications, one spare module of each type usually constitutes a sufficient stock of spares. A spare module of each type permits testing by

substitution during off hours. When a defective module is removed and replaced by the corresponding spare, the defective module can be repaired to create a new spare. Defective transistors, diodes, and other easily detected faulty components can be rapidly removed and replaced. In single shift operations, two modules of the same type very rarely fail during the time required to repair one.

Table 11-3 gives the DEC module types used in the PDP-4, including the 4K and 8K memories; the reader, punch, and typewriter control logic; and the type 25 real time option. The system module list, Figure 11-8, gives the total module count for a PDP-4 system.

For PDP-4 applications in which down-time must be minimized, and for installations used for more than one shift per day, additional stocks of the more complex modules are desirable. The more complex modules may require considerable time for diagnosis and repair of faults. To minimize down-time, insurance (in the form of additional spares) should be provided against the possibility of two failures within the time required for repair. Additional spares are also desirable for module types used in large quantities.

Table 11-4 gives recommended additional spare allowances by module type for PDP-4 applications requiring minimal down-time or multiple shift operation. The spares listed in Table 11-4 are recommended in addition to the minimum stock of Table 11-3. All PDP-4 installations should stock the Table 11-3 listing, but high-usage or high-priority installations should stock the Table 11-4 allowance as well as the Table 11-3 allowance.

For example, the spares allowance of module type 4204 are as follows: in a single-shift installation where moderate down-time can be accepted, only the single 4204 spare listed in Table 11-3 need be stocked. In a multiple-shift installation or in an installation where only minimal down-time can be tolerated, two type 4204 spares are recommended. (The additional spare is listed in Table 11-4.)

TABLE 11-3 RECOMMENDED MODULE SPARES

1103	1973	4114/4114R	4216[4]
1104	1976[2]	4115R	4218
1213	1978[2]	4127/4127R	4301
1310	1982	4128[3]	4303
1311	4102R[1]	4129/4129R	4401
1540	4105	4150	4407[3]
1607	4106/4106R[6]	4203	4410
1690[1]	4111	4204	4604
1701	4112R	4214	4605[5]
1972	4113/4113R	4215[3]	4681[3,4]

NOTES:

1 - required only in the Type 25 Real Time Option.

2 - resistor boards: spares are desirable but not necessary.

3 - required only in the Teleprinter control logic. In emergencies, a type 4401 clock adjusted to 9.6 kilocycles may be used in place of the type 4407.

4 - required only in the high-speed tape punch control logic.

5 - required in the Type 25, the reader control, and the punch control logic.

6 - In emergencies, the types 1103/1103R may replace the types 4106/4106R.

TABLE 11-4 RECOMMENDED ADDITIONAL MODULE SPARES

(For minimal down-time or multiple shift use)

Standard PDP-4 (includes 4K memory and reader control)			
	4203	4204	4604
	1540	1972	1982
Optional Equipment			
The 8K Memory:	1103,	1540,	2-1972
Type 25 Real Time:		4129R,	4604
Tape Punch:	(no additional spares necessary)		
Model 28 Teleprinter	(no additional spares necessary)		

b IN-OUT DEVICE SPARE PARTS - Recommended spare parts allowances for the Digitronics photoelectric paper tape reader, the Teletype BRPE 11 paper tape punch, and the Teletype Model 28 keyboard/printer are presented below.

Table 11-5 gives the recommended spare parts allowance for the Digitronics Type 2500 reader. Installations at which down-time must be minimized should also have a complete Type 2500 reader available for immediate replacement.

TABLE 11-5 RECOMMENDED TAPE READER SPARES

Part Number	Description	Quantity
	P. C. Board "LAC"	1
	P. C. Board "MPC"	1
B-A2909	Motor, 300 char/sec.*	1
B-C1320	Read Head Assembly	1
B-C1142	Brake Assembly	
C-C1924	Pinch Roller Solenoid Assembly	1
Osram 10-6411	Exciter Bulb	2

*The motor is supplied complete with gears for 300 char/sec.

Experience has shown that the teletype BPRE 11 punch is an extremely reliable unit. With proper preventive maintenance and lubrication, trouble-free operation can be expected for long periods of time. It is recommended that punch parts replacement and repairs be performed only by Teletype or DEC personnel.

Certain parts of the punch may require replacement at intervals determined by the speed and type of operation (i.e., idling or punching). These parts are available as Teletype Maintenance Parts Kit 143076, and are illustrated in Teletype Bulletin 1154B. The replacement schedule pertaining to these parts is given in the tape punch technical manual, Teletype Bulletin 215B, page 3-0.

Installations that use the punch frequently or continuously should stock this parts kit. Installations that do not stock this spare parts kit should nevertheless keep one spare timing belt on hand for each punch. For absolute minimum down-time, it is desirable to keep a complete spare punch available. The punch requires two types of lubricant, both available either from the Teletype Corporation or from DEC. These lubricants are Teletype KS7470 oil, and 145867 grease.

The Teletype model 28 keyboard/printer is a particularly complex piece of equipment; however, the model 28 has proved to be unusually reliable. Since keyboard/printer failures are extremely rare, no specific maintenance spare parts kit need be stocked.

All mechanical and electrical parts used in the keyboard/printer are fully described and illustrated in Teletype Bulletin 1149B, supplied with the PDP-4. Bulletin 1149B also describes the modification kits that provide various extra mechanical or electrical features for the model 28. Additional type styles and the associated key-tops for the keyboard are described in Teletype Bulletin 1164B, available from the Teletype Corporation.

Except in PDP-4 installations at which the model 28 is running almost continuously, the only spares which need be stocked for the model 28 are paper and ink ribbons. The keyboard/printer requires two types of lubricant, both available from DEC or from the Teletype Corporation. These two lubricants are Teletype KS-7470 oil, and Teletype KS-7471 grease.

c CIRCUIT COMPONENT SPARES - All circuit components except semiconductor, inductive, and distributive-constant delay components are available through local electronics parts distributors. The semiconductor and inductive components may be ordered directly from DEC.

Replacement of delay lines is not recommended. If a malfunction is directly attributable to a faulty delay line, the module should be returned to DEC for repair.

The recommended quantity of circuit component spares is listed in Table 11-6. The quantities listed under the first three columns (headed Reader) comprise a recommended minimum stock for installations contemplating module repair. The additional spare quantities listed in the next three columns for the three in-out options should be added as appropriate to the basic minimum stock. For example, a PDP-4 installation that includes the type 25 real time option should stock seven 2N 1304 transistors.

TABLE 11-6 RECOMMENDED CIRCUIT COMPONENT SPARES

	Reader 1K Mem	Reader 4K Mem	Reader 8K Mem	Type 25 Option	Punch	Model 28 KSR
TRANSISTORS						
2N 456	1	1	1	-	-	-
2N 501	1	1	2	-	-	-
2N 504	2	2	3	-	-	-
2N 599	3	5	7	-	-	-
2N 1065	3	5	7	-	-	-
2N 1184B	-	-	-	-	2	1
2N 1204	2	2	2	-	-	-
2N 1304	1	1	2	3	-	-
2N 1305	5	5	6	-	-	-
2N 1370	-	-	-	-	2	1
2N 1427	4	5	6	2	-	-
2N 1499	3	5	7	-	-	-
2N 1754	8	8	8	3	2	3
2N 2099	2	2	3	-	-	-
DIODES						
1N 276	10	10	11	7	3	4
1N 645	8	8	9	3	2	2
1N 914	3	3	3	2	1	2
1N 994	2	2	2	1	-	-
1N 1217	-	-	-	-	2	1
1N 1220	-	-	-	-	2	1
1N 1341	2	2	2	-	-	-
1N 3208	2	2	2	1	*	*

TABLE 11-6 RECOMMENDED CIRCUIT COMPONENT SPARES

(continued)

	Reader 1K Mem	Reader 4K Mem	Reader 8K Mem	Type 25 Option	Punch	Model 28 KSR
DIODES (continued)						
1N 3314B (Zener)	2	2	4	-	-	-
PULSE TRANSFORMERS						
Each Type**	1	1	1	-	-	-
T-2003	1	1	2	-	-	-
T-2024	1	1	1	***	1	1

*One additional 1N 3208 spare recommended if either the punch or the Model 28 KSR (or both) is used.

**This category includes the following types: T-2010, T-2018, T-2019, T-2020, T-2021, T-2023, T-2036, T-2037.

***If more than three in-out devices are connected to the Type 25, two spare T-2024 transformers are recommended; otherwise one is sufficient.

Since delay line replacement is not recommended, the delay lines do not appear in Table 11-6. The three power transformers are also omitted from Table 11-6 because power transformer failure is extremely rare. In installations where down-time must be kept to an absolute minimum, it is preferable to stock one complete spare of each power supply type rather than stocking replacement power transformers.

d MECHANICAL SPARES - Table 11-7 gives quantities of mechanical spares recommended

for a PDP-4 installation. Except for the quantity of air filters, which varies with the number of equipment bays, the quantities of spares listed are sufficient for most PDP-4 installations. However, Table 11-7 lists mechanical spares required only for the optional in-out equipment that is mentioned in paragraph 2-3b.

TABLE 11-7 MECHANICAL SPARE PARTS

Part Number and Description	Quantity of Spares
53E168, Type CFG: Rotron fan with #2R blade	1
Rotron Venturi: Muffin fan with mounting clips	1
10" x 10" x 2" EZ Kleen Filters	*
Type 418 Super Filter Coat, Pints	2

*One filter unit required for each bay of the installation.
Example: the standard PDP-4 requires two filters.

11-6 PREVENTIVE MAINTENANCE

This paragraph lists recommended preventive maintenance procedures for the standard PDP-4 installation, for the type 25 real time option, and for two in-out device options -- the punch and the keyboard/printer.

Preventive maintenance procedures should be performed on a rigorously regular basis. By appropriate use of regularly scheduled preventive maintenance techniques, most potential computer malfunctions can be detected before occurrence. In order to minimize computer downtime, this advance detection capability should be used faithfully. Good maintenance is preventive maintenance; corrective maintenance is a costly last resort.

In preventive maintenance procedures involving marginal power levels, the use of the maintenance record is very important. When accurate records are kept, long-term drifts in the values of margin voltage that cause malfunction are readily apparent. It is especially useful to make

an entry noting any temporary mulfunction which may occur during either testing or actual operation. Such entries can be invaluable in isolating intermittent failures. When a malfunction occurs, it is useful to note the portion of the program at which the malfunction is noticed, as well as any control settings and panel indications which may be relevant to the difficulty. Location of an intermittent failure is frequently accomplished by recording two or more malfunctions which intersect at a common defective component.

Component deterioration is often evidenced by malfunction of a particular module at a steadily decreasing margin voltage. Replacement may be indicated when such a long-term drift in margin voltage is detected, even though the margin at which failure occurs has not yet exceeded normal limits. It is always better to perform such preventive replacement before an actual operating malfunction occurs. Prompt replacement of deteriorating modules often forestalls computer errors, thereby reducing both error down-time and diagnostic down-time.

To minimize computer malfunctions, the following schedule of preventive maintenance procedures is strongly recommended.

a EVERY DAY (OPERATOR'S MAINTENANCE):

1) Run the DEC maintenance programs (CONTEST) without margins. Log all error halts, noting the reason for the error halt, if known.

2) Inspect and clean the tape-handling surfaces of the tape reader. These include the read head, tape guides and rollers, the pinch roller, the capstan, and the brake. Use a lint-free cloth or cotton swab (e.g., a Q-tip) moistened with denaturated alcohol, if necessary.

3) If the PDP-4 installation includes a paper tape punch, inspect and clean the tape-handling surfaces. Use a lint-free cloth, a cloth strip, or a soft toothbrush, as convenient. Do not use alcohol or other solvent near the feed pawl or the die block, since such solvents remove the light lubricating film. Empty the chad container.

4) If the installation includes a keyboard/printer, inspect and clean the platen and paper guides, as necessary. (The platen need be cleaned only if typing has run off the page or if the printer has run without paper.) Remove lint and other fouling from ribbon guides; replace ribbon if necessary.

5) Check that all cooling fans (bottom of each bay and back of each memory core-stack) are operating properly. Check for free flow of air.

6) Replace any noncritical malfunctioning components which can be detected by observing the console (e.g., indicator lamps, etc.).

NOTE: The remainder of the scheduled preventive maintenance procedures should be performed by qualified technicians only.

b EVERY WEEK - (In multiple-shift operation, every 80 hours):

1) Check the operator's maintenance logs. Note malfunctions and error halts detected by operator's CONTEST runs. Note noncritical component replacements made by the operator. (Does a particular circuit breaker blow too often? Does an indicator light burn out too often?)

2) Reader inspection: check for effects of vibration and wear of moving parts, especially gearing in the motor assembly. With the reader power off, gently rotate the capstan, feeling for stickiness or bind in bearings. Check the pinch roller-capstan clearance; see section 5.5.1 of the Digitronics manual.

3) Punch inspection: check for the effects of vibration, for tightness of wiring connections, and for tightness of the nuts and screws that lock the adjustments. Check for the presence of oxidized (red) metal dust near bearing surfaces, indicating insufficient clearance; this condition must be rectified immediately. With the punch unit cover removed (by removing the four mounting screws), rotate the main shaft slowly in the normal direction (clockwise, as viewed from the front). During rotation, activate all movable elements checking for freedom of movement. Check that all contact points meet squarely.

4) Keyboard/printer inspection: remove the cover. Visually check for effects of vibration -- tightness of cable plugs, mounting screws, etc. Check the selector magnet coils for signs of overheating, etc. Make sure there is no lubricant or other fouling under the selector armature (if necessary, insert a piece of bond paper between the poles and the armature to soak up lubricant. Make sure the bond paper leaves no lint.)

Replace cover, making sure that the copy light shield does not interfere with the type hammer. Check the operation of the local line feed key (LOC LF), the keyboard lock and unlock keys (KBD LOCK and KBD UNLK), the repeat key (REPT), and the local carriage return (LOC CR).

The keys LOC LF, LOC CR, and KBD UNLK should all be free to operate when the keyboard is locked.

Type a line or two of the alaphabet and figures, and check that the type is even on the line, and of relatively even impression. Replace the ribbon if necessary.

Run the Teleprinter Input-Output Test, noting printer errors, if any. Using the program, check for correct encoding of keyboard input. Log all keyboard/printer errors and the steps taken to correct them in the maintenance record.

5) Memory checkout: run the memory Checkerboard program. Using the worst-case configuration, increase the sense-amplifier +10 A margin until the first bit is lost. Note the meter reading at the type 734 marginal check supply. Decrease the sense-amplifier margin until the first bit is picked up; note the meter reading. The voltage at which the first bit is picked up, and the voltage at which the first bit is lost, should be symmetric about +10 vdc. Log the margin voltage meter readings at which the errors occur in the maintenance record.

If the bit lost at high margin is the same bit as that lost at low margin, the corresponding sense amplifier may be weak. In this case, increase margins slightly further until a second bit is lost and note the reading. Similarly decrease the lower margin further until a second bit is picked up. Again these margins should be symmetric about +10 vdc; however, the difference in margin voltage between the first bit error and the second is the criterion for judging the sense amplifier. If this situation exists, make an entry in the maintenance log giving all pertinent margin voltage readings and stating the panel location of the suspected sense amplifier.

If the margin voltages causing bit errors are not symmetric about +10 vdc, the sense amplifier slice adjustment should be performed. If one sense amplifier appears weak, the sense amplifier balance adjustment should be made before summarily replacing the sense amplifier. Procedures for both adjustments are given in paragraph 11-4c. Be sure to log all the conditions leading to the decision to readjust the sense amplifier in the maintenance record. The entry should give the pertinent margin voltages, the location of the affected sense amplifier, and some indication of the extent to which it was out of adjustment.

6) Finally, enter into the maintenance record your name, the date and time, and the reading of the elapsed-time meter for this weekly checkout.

c EVERY MONTH - (In multiple-shift operation, every 160 hours):

1) Check the operator's maintenance logs. Note malfunctions and error halts detected by operator's CONTEST program runs. Also review noncritical component replacements by the operator, checking for excessive replacement of a particular component.

2) Run all CONTEST programs with margins. The procedure for running CONTEST with margins is discussed in paragraph 11-8 below. It is extremely important to log all malfunctions caused by the application of marginal voltage in the maintenance record.

3) Change and clean the air filters at the bottom of each bay, using the following procedure. Loosen the two thumbscrews holding the fan and filter housing to the floor of the cabinet. Remove the fan and filter housing. The filter can then be taken out of the housing and the clean spare filter installed. Replace the fan and filter housing containing the clean filter, and tighten the two thumbscrews.

Clean the filters by thoroughly flushing them with hot tap-water is a direction opposite to that of airflow. When all dust and lint is removed, shake out excess moisture. Stand the filter on one end for ten or fifteen minutes to allow remaining moisture to evaporate. If the flush water is sufficiently hot, the filter should dry completely in about fifteen minutes. Finally, spray the filter with aerosol Super Filter Coat or an equivalent product. This spray serves both as a dirt-capturing medium and as a detergent which helps wash out the dust and lint during the next reverse flushing.

4) Check all moving parts of the reader for freedom of movement and for wear, particularly the drive motor gearing. Check the outputs of the data channel amplifiers and the sprocket channel amplifier, using the procedure of paragraphs 11-4d. Do this regardless of whether or not the tape reader system passed the CONTEST Reader and Punch Test. Lubricate the drive motor bearings with premium grade SAE 20 or SAE 30 motor oil. If a bearing shows any sign of sticking, it should be replaced. Any signs of noise or stickiness in the moving parts of the reader, and bearing replacement if any, must be entered in the maintenance record.

5) Lubricate the high-speed tape punch according to procedures given in section five of Teletype Bulletin 215B. The teletype lubrication procedures cover lubrication of several different types of punch. It is important to follow the lubrication procedure

that applies to the particular punch tape supplied with the PDP-4. It is particularly important to let no oil or grease accumulate between the armatures and the magnet pole faces, or between contact points. Always wipe of excess lubricant.

6) Finally, enter into the maintenance record your name, the date and time, and the reading of the elapsed-time meter for this monthly checkout.

d EVERY SIX MONTHS - (In multiple-shift operation, every 1500 hours): Perform the complete keyboard/printer lubrication procedure as given in section three of Teletype Bulletin 217B. This is a long and arduous job but it pays off well in terms of long-run keyboard/printer reliability. Follow the instructions literally and carefully. Avoid over-lubrication; in particular, do not get excess lubricant near the selector magnets or the selector magnet armature. Enter into the maintenance record your name, the date and time, and the reading from the elapsed-time meter for this teleprinter lubrication.

11-7 OPERATOR's MAINTENANCE

The computer operator at a PDP-4 installation has three maintenance responsibilities: 1) performing the daily machine checkout; 2) keeping an accurate Operator's Log; 3) acting as an aid to the technician in troubleshooting machine malfunctions.

The daily machine checkout procedure is described in paragraph 11-6a above. Preferably, this checkout procedure should be performed as the first operation after the machine is turned on in the morning. Running the CONTEST programs is the most important part of the daily checkout procedure.

One good reason for running the CONTEST programs every day is that if there is a fault in the computer logic, one of the CONTEST programs is nearly certain to reveal it. This means that the fault in the computer is encountered while running a program which is known to be good. On the other hand, if the fault should occur during the running of a normal operating program later in the day, the fault might easily be dismissed as a program error, on the grounds that the program had not been sufficiently debugged. In this case, the fault in the machine remains undiscovered, and valuable time is wasted debugging a program which might be good.

If trouble occurs during normal computing time, the operator should ensure that the machine

is not at fault by running the CONTEST. If CONTEST discovers a fault, the operator should notify the author of the operating program, so that the author does not waste further time debugging a good program.

For efficient operation, it is obviously desirable to discover faults by running the CONTEST rather than to encounter them during operating programs. Otherwise all computing time, from the start of the operating program which originally encountered the fault until the discovery of the fault, is wasted. During this time the machine produces no useful results.

Another good reason for running the CONTEST as the first operation of the machine shift is that CONTEST test programs have a diagnostic value. If a CONTEST program discovers a fault in the computer logic, it simultaneously gives indications as to the general location of the fault. This is certainly not true of operating programs. A great deal of time that would otherwise be spent in diagnosing the location of a fault can be saved if the fault is first discovered by CONTEST.

The PDP LOG, if kept properly and in sufficient detail, can be a valuable aid in subsequent diagnosis of machine malfunction. During a CONTEST run, the most important items to be logged are:

1) The operator's name, the date and time, and the reading of the elapsed-time meter for this CONTEST run;

2) The names of all programs run in addition to the standard CONTEST, if any;

3) All replacements of minor components made by the operator in the absence of the technician;

4) In case of a fault discovered by CONTEST, the register indications and the settings of the ADDRESS, ACCUMULATOR, and operating switches;

5) If a malfunction is so serious that the machine must go down, the exact times of the beginning and end of down-time;

6) The reason for down-time, and all corrective measures taken by the operator to restore operation.

The PDP LOG format is given as Table 11-1.

In most new computer installations, the operator has an opportunity to become familiar with programming and machine language before the technician. In addition, the operator rapidly becomes familiar with the frequently used operating programs and routines. This knowledge is a valuable aid in troubleshooting malfunctions that develop during normal operation. Since the operator is so often familiar with the internal workings of commonly run programs, he is often able to make a preliminary diagnosis of malfunction location.

Even when a preliminary diagnosis cannot be made, thoughtful observation of register indicators and positions of test word address and sense switches generally enables the operator to eliminate vast sections of computer logic from suspicion. The operator is also in a better position than the technician to discriminate between faults caused by machine logic malfunction and errors caused by program bugs.

In many troubleshooting problems it is convenient to use small program loops containing only a few instructions. These loops may be used either for exercising certain portions of the machine logic, or for diagnostic purposes within a small section of machine logic. Diagnostic and exercise loops are, generally, extremely simple; i.e., an exercise loop could consist of only a single instruction. The adjustment procedure for the type 735 memory power supply, for example, uses three such one-instruction loops (shown in steps 1, 4, and 9 of paragraph 11-4b). Other examples of exercise and diagnostic loops are given in paragraph 11-9d. The operator is often able to aid the technician considerably by producing simple program loops for specific troubleshooting applications.

11-8 MAINTENANCE PROGRAMS

The DEC maintenance programs, including CONTEST, permit effective use of PDP-4 for self-testing. For the majority of possible equipment malfunctions, intelligent use of these programs provides efficient trouble detection and location. Complete descriptions of the PDP-4 maintenance programs and procedures for their use are available from the PDP-4 program library.

Before loading a program tape into the tape reader, the reader brake must be turned off by turning the tape guide lever to the right. This allows the tape to be loaded. The fan-folded tape stack is placed in the right-hand tape bin, oriented so that the tape unfolds from the top of the stack. Tape movement through the reader is from right to left. Looking in the direction of tape movement, the five data holes are to the left of the sprocket hole and the remaining

three data holes are to the right of the sprocket hole. Figure 11-9 shows the appearance of the top surface of the tape and the direction of tape movement when the tape is properly loaded.

a PDP-4 LIBRARY PROGRAM GUIDES - The library program guides are a separate set of self-contained technical memoranda, each of which is designed as an aid to learning the function and application of a single PDP-4 program. For rapid reference, all maintenance program guides are written in the same format.

Each guide contains three major sections:

1) Console operating procedure.

2) Suggested applications of program.

3) Program description.

Both the first and second sections are intended for reference and should usually be consulted each time the test program is used. The third section, program description, is designed as an aid to understanding the program rather than for repeated reference. Each program guide starts with a cover-page abstract which permits convenient identification of the program. Immediately following the abstract is the console operating procedure.

(1) Console Operating Procedure - This section is composed of the following five tables:

Table	Contents
1) Tapes Required for Test	Lists tapes which are required to run the program.
2) Switches	Lists console switches applicable to the program, and specifies appropriate settings.
3) Load Sequence	Gives detailed step-by-step instructions for loading and starting the program.
4) Error Halts	Lists addresses of the programmed error halts, the contents of relevant registers, and the meaning or cause of the error halt.
5) Post-Error Restart Procedures	Specifies correct procedure for restarting the program after each type of error halt.

(2) Suggested Applications of Program - The console operating procedure is followed by a section covering suggested program usage. This section of each program guide presents a generally useful test sequence which the operator may perform. It by no means exhausts the capabilities of the program, and is not intended to limit the freedom of the operator to modify program use where appropriate.

(3) Program Description - The third and final section of each program guide contains a detailed description of program structure and operation. The operator does not need to read this section each time he runs the test. It would in fact be possible to execute the suggested test without understanding the program at all. However, a good understanding of the program yields the ability to modify program usage as required by actual computer malfunctions.

In addition to a detailed description of the program, the third section of each guide also includes a program flow chart and listing.

b USE OF MARGINAL CHECK - Variable power supply type 734 produces all marginal check voltages used in PDP-4. This supply and the associated marginal check switch panel are located at the top of the bay 1 plenum door. The 734 supply furnishes voltages which vary from 0 to -20 vdc, or from 0 to +20 vdc, depending upon the setting of the polarity switch. Voltage amplitude variation between 0 and 20 volts is controlled by the large black knob on the 734 supply. The output voltage is shown by the MARGINAL CHECK voltage meter. Whenever marginal check voltage is applied for any reason, entries must be made in the maintenance record describing the circumstances and results.

Marginal voltage can be applied to the A lines of any mounting panel by pushing up the top toggle switch on that panel. Marginal voltage can be applied to the B lines by pushing up the center toggle switch. When marginal checking the A and B lines, the polarity switch must be in the +10 MC position. To marginal check the C lines (-15 vdc), set the polarity switch to -15 MC and push up the bottom toggle switch at the left front of the panel to be tested.

When the polarity switch is in the OFF position, normal voltages are applied to all three power lines of every panel, regardless of the settings of the toggle switches. The OFF position of the polarity switch is provided as a convenience to the technician during trouble-

shooting, not as a substitute for turning off the toggle switches at the mounting panels. To minimize the effects of unauthorized tampering (for example, someone's inadvertently turning on the 734 supply during an operating program) be sure to turn off all three marginal check toggle switches at the left of every mounting panel at the completion of marginal check procedures.

Marginal check voltages may be applied to a single module alone by means of the pigtail plug-in extender (paragraph 11-10b).

The two +10 vdc power lines are used principally as the base bias supplies for transistor logic. Making the +10 vdc supply more positive checks transistor current gain ( ). Reducing the +10 vdc supply tests for excessive transistor leakage.

The -15 vdc power line is used chiefly as the collector supply. The -15 vdc marginal check line is applied only to pulse amplifiers (module types 16707, 4604, and 4605). Making the -15 vdc supply more negative increases output pulse amplitude; making the -15 vdc supply less negative decreases output pulse amplitude. Marginal voltage should not be applied simultaneously to all -15 vdc supply lines throughout the PDP-4, because the resulting load exceeds the rating of the type 734 supply.

During maintenance program runs, the particular mounting panels to which marginal check voltages might be applied depend upon which maintenance program is selected. Any program, whether used for maintenance purposes or not, consists of instructions which must come from memory locations. Regardless of the particular section of machine logic which a maintenance program tests, it must always depend upon the memory, the timing, and the instruction logic for its operation. Routine maintenance program runs with marginal checking should, therefore, be performed in the CONTEST order:

1) Instruction Test, INSTEP (M-5)

2) Checkboard (M-1)

3) Reader and Punch Test (M-2)

4) Teleprinter Input-Output Test (M-3)

Marginal checking may also be done using the CONTEST (M-4) program. The individual sections of CONTEST parallel the four maintenance programs listed above, in order. However, each of the listed separate programs above is more versatile than the corresponding

section of CONTEST.

When running maintenance programs that test the memory, marginal check voltage should be applied only to the memory module and the memory control logic. The Checkerboard program, for example, primarily tests the core bank and the sense amplifiers. If marginal check voltages were applied to control logic (bay 1) while running the Checkerboard program, control malfunctions might be introduced which the checkerboard program could not diagnose. Conversely, if marginal check voltages were applied to the memory module while running the Instruction Test Program, memory errors might be introduced which the Instruction Test program could not diagnose.

While running a maintenance program to solve a specific troubleshooting problem, the application of marginal check voltage is made at locations determined by the nature of the problem. To aid in selecting mounting panels for marginal checking, the physical location of the various logic sections of the computer, with respect to module location, is shown in Figure 11-1.

c LOG ENTRIES - When running maintenance programs with marginal check voltages, it is extremely important to keep detailed and accurate logs. An accurate maintenance record, when combined with the marginal check production test record (supplied with the PDP-4) makes up a complete operating history of all machine logic under marginal conditions. When accurate and complete maintenance records are kept faithfully, any deterioration of circuit components is easily detected. A deteriorating component is revealed in the record as an error of a particular type which occurs at steadily decreasing margin voltages over a period of months. Without logs, a symptom of this type is likely to pass completely unnoticed.

When accurate logs are kept, a glance at the previous history of the failure pattern in certain sections of computer logic often saves unnecessary replacement of plug-in units. For example, a certain sense amplifier may operate in a completely reliable manner under normal conditions, yet it may fail at a narrower margin than the others. Normally this would indicate that the sense amplifier was weak; however, when a logged history of sense amplifier performance under marginal check voltages is available, it can immediately be determined whether the narrower margin at which this sense amplifier failed is the result

of a gradual drift (indicating weakness) or is merely the voltage at which this sense amplifier has always failed. In the first case, the sense amplifier would be replaced. In the second, however, since no drift in margin voltage is taking place, it can be assumed that the sense amplifier will continue indefinitely to give reliable performance under normal conditions.

11-9 TROUBLESHOOTING

The troubleshooting procedure presented below does not involve the use of malfunction tables or symptom-cause-remedy charts. For a full scale general purpose digital computer like PDP-4, such tables or charts would be so cumbersome and inconvenient as to be useless. Instead, the method suggested depends upon logical thinking, common sense, and an organized step-by-step procedure.

For efficient troubleshooting, the technician must be completely familiar with the PDP-4 system function and machine logic. When confronted with a malfunction, a technician who is not familiar with the machine wastes valuable time poring over prints and elementary system description, thus unnecessarily prolonging down-time. It is essential to have a good underlying knowledge of system function (chapter 4), operation (chapter 5), the machine logic (chapters 6-9), and, to a lesser degree, plug-in unit circuit theory (chapter 10). It is equally important to be familiar with the logic prints (D-size block schematics).

Most people find it impractical to memorize the prints completely; but, after a reasonable learning period, the competent technician will probably know which print contains what logic, and even the approximate area of the print which shows given sections of the logic. All of the machine logic is on the prints. The description of the logic (chapters 6 through 9) is tied to the prints. The flow of logic levels and pulses can be traced from the prints. Location and identification of circuits by mounting panel location, pin connection, and module type is also given on the prints.

This maintenance manual is intended primarily as an aid to learning the prints. Once the system logic is well understood, the prints are usually used much more often then the manual. The prints are the best available source of reference information, and the prudent technician should take the time to become thoroughly at home with them. This is much easier than it sounds; once the function of the machine is well understood, the details of the machine logic follow

quite logically, making the learning task less formidable than the sheer bulk of the data would suggest.

In addition to the prints and this maintenance manual, the technician should have five manufacturer's manuals for the standard in-out equipment: the Digitronics 2500 manual for the paper tape reader; Teletype Bulletin 215B for the punch; and Teletype Bulletins 216B, 217B, and 1149B for the keyboard/printer. It is helpful to read these manuals to learn what information is in them. Much computer down-time can be saved by knowing in advance where to go for information.

When confronting a new malfunction in the machine, the following sequential plan of attack should be followed:

1) Initial investigation: gather all available information on the problem.

2) Preliminary check: see if the malfunction presents obvious physical symptoms.

3) Console troubleshooting: attempt to localize the problem to a particular section of logic; use the maintenance programs. Use marginal checking procedures, if indicated.

4) Logic troubleshooting: further localize the malfunction to a particular module, power supply, or power control unit.

5) Module troubleshooting: locate the specific malfunctioning component inside a particular module or power unit.

6) Testing after repair: ensure that the machine is really back on the line.

7) Logging the trouble: note what went wrong, and how it was fixed.

Steps 1 through 4 are further discussed in paragraphs a through d below. Step 5, module troubleshooting, is treated in 11-10b. Step 6, testing after repair, is explained in e below. Use of maintenance logs (step 7) is covered in f below.

a INITIAL INVESTIGATION - As the first step in troubleshooting a malfunction, before even touching the PDP-4, the technician should find out as much as possible about the nature of the malfunction. Question the operator mercilessly. Consult the operator's log: did the malfunction also occur during the operator's CONTEST runs? Has the operator no-

ticed any unusual machine behavior as a prelude to this malfunction? If this malfunction occurred during a CONTEST run, the operator should have noted the readings of the console indicators and the settings of the test word, address, and sense switches. Also, if the malfunction occurs during a CONTEST run, these indications and settings are very significant and must be carefully noted in the maintenance record.

Look for a possible history of this malfunction among previous entries in the maintenance records. This step is particularly important if more than one technician works on the machine. Has the same malfunction, or one related to it, occurred before? If so, how was it remedied? Look also at the last half-dozen monthly entries for maintenance program runs with marginal check. Is there a deteriorating module (one that fails at steadily decreasing margins) that seems related to this malfunction? If so, compare notes; do the register indications and switch settings for that failure resemble the indications and settings for the present malfunction?

The more information the technician can gather, the more rapidly he can make his diagnosis and the sooner the machine can be returned to operation. Every available source of information should be explored. Do not try to troubleshoot a computer malfunction cold; usually this just wastes time.

b PRELIMINARY CHECK - The second step is to check for physical symptoms of malfunction. Look first at the ACCUMULATOR, ADDRESS, and operating switches. Make sure that the operator is not running the program incorrectly. Open the plenum doors. Look for broken cords or plugs, tripped circuit breakers. Has someone inadvertently placed half the machine on marginal check voltages? Are all modules plugged in all the way? Are all memory cables plugged in all the way? Is there power?

This preliminary check is useful far more often in the case of a catastrophic malfunction than in the case of an intermittent one. Except for cable and plug-in unit connections which may be intermittent, most intermittent malfunctions are due to cold-solder joints, or faulty circuit components. Unless the malfunction is definitely isolated to within two or three modules by the initial investigation (a above), it is poor strategy to start checking arbitrary modules for cold-solder joints or bad components. More sophisticated troubleshooting procedures must then be used (c and d below). Nevertheless, because it eliminates

many common sources of trouble which might otherwise be overlooked, the preliminary check should not be omitted. Few things are more annoying than to go through complex time-consuming troubleshooting procedures only to discover that the malfunction is actually caused by some obvious cable connection not making proper contact.

c CONSOLE TROUBLESHOOTING - In many cases, the initial investigation discloses an appropriate line of attack but does not in itself pinpoint the location of the trouble. The third step in the troubleshooting sequence, troubleshooting from the console, is used to localize the malfunction within a small section of the machine logic.

Console troubleshooting most often requires the use of the maintenance programs (with or without marginal checking, depending on the nature of the malfunction).

Intermittent malfunctions caused by weak components can almost always be aggravated and so transformed to relatively consistent malfunctions by the use of marginal checking. Unfortunately, use of marginal check cannot reveal intermittent connections (such as cold-solder joints or interruptions in cable wiring). Consistent (catastrophic) malfunctions are, however, easy to locate. Simply run the appropriate maintenance program, wait for the error halt, and consult the program guide.

(1) Maintenance Program Selection - Normally the initial investigation (a above) restricts a malfunction to within some large section of machine logic. For example, a particular in-out device does not work properly; or it is impossible to transfer into the accumulator; or some operating program which is known to be good invariably halts at a certain memory location, etc.

Even if the program does not run at all, the malfunction can usually be well localized by initial investigation. In this case the trouble is likely to be located in the general control functions (i.e., in the timing; or in the control logic for the states or memory; or in the instruction register and decoder; or possibly in the program counter and program control logic).

For nearly any computer malfunction, the initial investigation usually determines which of the maintenance programs is the proper one to use. The program used depends on the character of the malfunction. Suppose, for example, that the complaint involves

unexplained halts in operating programs. The operator says that attempts to restart the programs result merely in another unexplained halt, and he then produces a list of memory locations at which the machine frequently halts. An appropriate maintenance program for investigating this malfunction would be the Checkerboard.

(2) Use of Marginal Check - The particular maintenance program most likely to discover a malfunction should first be run without marginal check voltages. If the malfunction is a consistent one, it shows up immediately during this first run. If the malfunction does not show up during the first run without marginal voltages applied, there are two alternate possibilities, one of which probably explains the situation. First, the malfunction may be an intermittent one, for example, a loose connection. Second, there may be some loading condition imposed on the logic circuits which is present during the operating program, but not during the maintenance program.

If the malfunction is caused by loading conditions unique to the operating program, it can nevertheless be detected during a maintenance program run. This is done by applying marginal check voltages to the suspected sections. From the last few entries in the maintenance record, the technician can determine the marginal check voltages which normally cause failure during the selected program. A malfunction that is caused by differences in loading conditions is likely to show up at considerably smaller margins than those listed in the last few log entries.

If the maintenance program discovers the error during application of marginal check voltages, do not restart the computer. First look at the register indications and at the ACCUMULATOR and ADDRESS switch settings for hints locating the malfunction.

(3) Procedure - Console troubleshooting procedures for locating catastrophic malfunctions should be directed toward discovering a pattern of consistency among the errors. Two examples of procedures which locate catastrophic malfunctions through the discovery of error patterns are presented in (4) below.

Location of an intermittent malfunction is extremely difficult using console troubleshooting alone. For this reason, procedures for locating intermittent malfunctions are explained under logic troubleshooting (d below).

Malfunctions (either catastrophic or intermittent) in the power-clear and special pulses, and in other control logic initiated by console keys, can be easily located by using the REPEAT switch and the SPEED controls. All operations except STOP that are initiated by console keys may be repeated indefinitely at repetition rates selected at the SPEED controls. If desired, oscilloscope signal tracing techniques can be used in troubleshooting console operations. The scope may be synchronized on SP0 (available at one of the three insulated standoffs in panel 1A). The SPEED controls should then be set to the fastest repetition rate.

(4) Examples - Two examples illustrating the discovery of error patterns are given; the first a continuation of the memory address trouble hypothesized in (1) above; the second an example of trouble involving the in-out equipment.

In (1) above, the Checkerboard was selected as the maintenance program most likely to give an indication of the malfunction location.

A number of possible malfunction locations may occur to the technician: the X and Y selection inverters, the memory address register, the memory address decoders, the memory address transfer logic, the program counter, etc. However, before running the Checkerboard, the operating program should be closely examined: do the memory locations at which the computer likes to halt all contain the same instruction? If they do, the instruction register or the instruction decoders could be at fault.

In the present example, suppose that examination of the operating program discloses that the troublesome addresses do not all contain the same instructions. The logical first step in console troubleshooting is then running the Checkerboard.

If the Checkerboard program detects an error, the computer halts at location 7740. Pressing CONTINUE then displays the location of the failing memory register. Suppose that this is an intermittent malfunction; i.e., suppose that the entire Checkerboard program proceeds to completion with no error halt.

The fact that the machine completes the test without an error halt suggests that circuit loading conditions during the normal operating program are significantly different from conditions during the test run. Do not despair -- use marginal check!

There is one fortunate characteristic which every malfunction displays. No matter how unusual it may be, there is always a thread of consistency in the errors it produces.

Returning to the present example; suppose that the marginal check voltages cause recurrence of the malfunction, and that every error halt of the Checkerboard program occurs at an address in which bits 9 through 11 contain 5 octal (101). Now there is something to work on.

The binary-to-octal decoder for MA_{9-11} is in location 1C23 (see Figure 8-1). Output level 5 is asserted negative. This level feeds a 50-pin Cannon connector to the memory module. Figure 8-3 shows the level arriving at pin N of the Y selection inverter module in location 2D3. The ground assertion level comes out on pin P of the same module. We can check for the positive assertion level at the memory read/write switches in locations 2B14 and 2B16. Except for an extremely improbable situation (such as simultaneous malfunction of all eight read/write switches in 2B14 and 2B16), the trouble must be located somewhere along the line of connections listed above.

The console troubleshooting procedures illustrated by the foregoing example have isolated the trouble to a manageable section of the computer logic. The technician can now proceed with the signal tracing procedures described in d below.

As a second example, suppose that the operator reports the keyboard/printer types nonsense. It is possible, by spending a great deal of time, to make some sense of the remarks printed out as part of the operating program's output subroutine; however, the data output is entirely meaningless. If the preliminary check discloses nothing useful, the logical first step is to run the Teleprinter Input-Output Test.

The advantage of a specific in-out test program of this sort is that the correct output is known. The correct printout of the test is THE QUICK BROWN FOX, etc. Suppose, however, that the printout looks like this:

```
QTHE QUIIU Z
          TW STY AUHPS TPE
                       THE LAZY ETL WQUE
                                    TYUITP AZIESLHAULH PYZS
                                                        QTHE
```

Four facts are immediately evident:

1. The carriage return does not work at all.

2. The line feed operation is generated spuriously.

3. One of the three operations at the beginning of a line (carriage return, line feed, and letter shift) is interpreted as Q.

4. The figure shift operation does not work at all.

The first step in troubleshooting this failure is to type the expected line of printout at the keyboard:

(Carriage return, line feed, letter shift)

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG

(space, figure shift)

1234567890 -?:$!&#'().,;/"

(bell)

(Carriage return, line feed, letter shift.)

If every character and printer operation works properly from the keyboard, the trouble must be in the keyboard/printer control logic, or in the transfer logic. Suppose, in this example, that the printer does perform correctly from keyboard input.

Table 5-1 gives the octal numbers representing the teletype code for each character and printer operation. The first observation is that the carriage return is absent. The code for carriage return is 02, or 00010. First of all, then, something is evidently wrong with the fourth bit of the teletype code. Now before opening up the machine, check first that the bit 4 failure hypothesis is consistent with the other printout errors. First, one of the printer operations at the beginning of the line is interpreted as Q. The code for Q is 35, or 11101. If the fourth bit is added to this code, the result is 11111, or 37. Code 37 represents the letter shift, one of the operations at the beginning of the line.

Counting printer operations in the bad printout, from the beginning of the line, note that the first spurious line feed occurs as the 15th printer operation. In the correct printout, the 15th operation is the character R in BROWN. The code for R is 12; if bit 4 fails, this code becomes 10 (i.e., 01010 becomes 01000). Code 10 represents line feed. So far, so good... Finally, the figure shift operation was absent from the bad printout. The code for figure shift is 33; if bit 4 fails, this code becomes 31

(i.e., 11011 becomes 11001). Code 31 represents W.

WQUE
TYUITP

stands for (figure shift)

1234567890

when bit 4 is added to the codes for W, line feed, and T.

The trouble now has been narrowed to within a small section of computer logic. The transfer logic must be faulty with respect to the fourth bit. The trouble cannot be in bit 4 of the LUO printer buffer because this buffer acts as a shift register to develop the teletype signal. If a particular stage of this buffer/shift register is defective, the shiftout is incomplete. But this completely disables the printer; there could be no printout at all. So the trouble cannot be in the printer buffer; it must be in the transfer from AC.

Now, finally, knowing in advance where to look for the trouble, go into the machine. The logical places to check for transfer are:

pin 2F4S, AC_{16}^{1} asserted negative;

pin 2F4R, same signal, asserted at ground;

pin 1M18H, same signal, again asserted at ground.

This particular keyboard/printer malfunction will probably never occur. The example presented above is primarily intended to illustrate logical, step-by-step troubleshooting techniques. It is the general analytical process of isolation illustrated by the example that is important, not the specific steps used above to signal-trace a particular unique keyboard/printer malfunction.

d LOGIC TROUBLESHOOTING - After console troubleshooting procedures (c above) have located the trouble to within a small section of the computer, logic troubleshooting methods are employed to isolate the malfunction to within a single module or module connection. Logic troubleshooting is most often done using the oscilloscope and small diagnostic or exercise loops consisting of only a few instructions.

Logic troubleshooting is normally the fourth step in the troubleshooting sequence; it relies heavily upon successful completion of the first three steps. Logic troubleshooting is detail

work, normally performed only on small sections of logic or particular discreet strings of connections between panels. With the possible exception of diagnostic and exercise loops, the procedures outlined in this paragraph are applicable only to small subsystems. These procedures should not be substituted for the console troubleshooting methods outlined in c above. To avoid wasted time from widespread detail work, use console troubleshooting to isolate the malfunction to the smallest possible section of machine logic before logic troubleshooting procedures are begun.

The remaining portions of this paragraph discuss the construction and development of both diagnostic and exercise loops, as well as suggested procedures for logic troubleshooting.

(1) Diagnostic and Exercise Loops - A loop is a set of instructions, one characteristic of which causes the computer to repeat the set of instructions over and over again. A loop may contain any number of instructions, and generally incorporates some method of indexing. The diagnostic and exercise loops discussed here, however, contain only a few instructions and are designed to repeat indefinitely (i.e., no indexing is used).

Exercise loops are specifically designed to pulse some small specific section of the computer logic repeatedly. Some examples of exercise loops, used in adjusting memory circuits, are included in paragraph 11-4b, steps 1, 4, and 9, and in step 2 of paragraph 11-4d.

In general, most exercise loops contain the following three parts:

1. One or more instructions that set up desired initial conditions;
2. The group of instructions which generates the desired pulse or level;
3. A jump instruction, returning control to the beginning of the loop.

The simplest possible exercise loop is the jump instruction alone. A jump instruction becomes a loop when it addresses the location in which it is stored. For example, if the instruction "jump to 0000" (60 0000) is deposited in location 0000, and the computer is started in location 0000, then the computer repeats the jump instruction over and over again. The jump instruction is itself the instruction in the second and third parts of the exercise loop. In step 1 of paragraph 11-4b, the jump instruction is used as a loop which provides read/write currents for adjusting the type 735 power supply.

A disgnostic loop is simply an exercise loop which includes some method of sensing for error. A diagnostic loop can be set up to halt the computer in case of error in such a way that the console indicator lights give some indication of the location of the malfunction causing the error. Good familiarity with the PDP-4 instruction list is required for the development of small exercise and diagnostic loops.

Exercise and diagnostic loops are used generally as a way of keeping some section of computer logic operating repetitively in a predictable manner. When repetitive operation is set up in this way, oscilloscope signal tracing techniques can be used to determine whether the correct pulses and levels are being generated. Diagnostic loops are also used during console troubleshooting procedures as an aid in further narrowing the possible trouble area.

In general, the set of instructions that sets up desired initial conditions should be very short, certainly no more than three instructions. If a particular repetitive operation requires a complicated or involved pattern of initializing, then nearly all the preparation should be done at the console before depositing the exercise loop. Instructions that set up initial conditions in exercise loops are normally taken mainly from the operate group of instructions (cll, oas, cla). For certain applications, the instruction law, and the memory reference instructions dzm and lac, are useful.

The loop instruction or instructions that generate the desired operating pulse or level in an exercise loop naturally depend on the specific repetitive pulse or level desired. For example, the pulse that generates in AC the exclusive OR function between the contents of AC and the contents of MB is produced by a number of instructions -- add, tad, xor, sad, lac.

One of the jump instructions, jmp or jms, must be used to make the exercise routine repeat itself indefinitely. The following example (Table 11-8) illustrates an exercise loop of six instructions and two data words which tests the reaction of each bit of the accumulator to the exclusive OR pulse under each of the four possible initial conditions. In other words, the loop repetitively checks each bit of the accumulator for behavior corresponding to the exclusive OR truth table at the end of paragraph 7-2c.

TABLE 11-8 SAMPLE EXERCISE LOOP

Exclusive OR pulse loop	Instructions	Loc.	Contents
Load AC with all 1s	lac 1s	1000	20 1005
Exclusive OR with all 0s	xor 0s	1001	24 1006
Exclusive OR with all 1s	xor 1s	1002	24 1005
Exclusive OR with all 0s	xor 0s	1003	24 1006
Repeat	jmp load	1004	60 1000
All 1s	1s	1005	77 7777
All 0s	0s	1006	00 0000

Alternatively, the instruction lac could be replaced by the instruction load accumulator from test word switches (lat: 75 0004).

In a diagnostic loop, the set of operations to be repeated includes some instruction or instructions for sensing an error. Generally, these are the skip instructions. All skip instructions are in the in-out and operate groups, except the two memory reference skip instructions sad and isz. Table 11-9 gives an example of a simple diagnostic loop to test the response of accumulator bits to the exclusive OR pulse.

TABLE 11-9 SAMPLE DIAGNOSTIC LOOP

Exclusive OR loop	Instructions	Loc.	Contents
Load AC with test word	lat	1000	75 0004
Deposit AC in TW	dac TW	1001	16 0006
Exclusive OR with TW	xor TW	1002	24 0006
Skip on nonzero AC	sna	1003	74 0200
Jump to "load AC"	jmp lat	1004	60 1000
Halt on an error	hlt	1005	74 0040
Location TW	TW	1006	00 0000

This sample disgnostic loop does not test for all possible combinations of 1s and 0s in AC and MB as did the exercise loop of Table 11-8. However, the loop does halt the computer on an error, and shows the malfunctioning bit of AC in the accumulator indicator lights (that bit which is different from the corresponding bit of the test word switches).

The Table 11-8 and Table 11-9 examples are given only to illustrate form and organization. Diagnostic and exercise loops take on endless variety. A technician should be able to generate applicable loops to troubleshoot any section of the computer.

Although the examples given are typical maintenance loops, they are designed for one specific application. Even if a similar problem should occur, the particular circumstances are not likely to be identical. For example, it may not be necessary to test for every combination of 1s and 0s (as does the exercise loop of Table 11-8). It may not even be necessary to test every bit of the accumulator. If the problem seems confined to the exclusive OR pulse logic alone, and is unrelated to the response of the AC bits, the simple exercise loop composed of the instruction xor, followed by jmp to the location containing xor, would be sufficient. Ingenuity, common sense, and familiarity with the instruction list, enable an alert technician to develop diagnostic or exercise loops to suit any specific troubleshooting problem.

(2) Suggested Procedures - Logic troubleshooting procedures should be undertaken only after the preliminary check or console troubleshooting has isolated the malfunction to a small section of the computer logic.

Logic troubleshooting is performed inside the computer. It always consists of a number of steps designed to narrow down the location of a malfunction to within a particular plug-in unit, connection, or power unit. The specific steps required and the order in which they are carried out always depend on the problem. In general, however, logic troubleshooting steps fall into three broad categories: 1) signal tracing, 2) substitution, and 3) aggravation.

Only one good method of signal tracing is available -- the use of the oscilloscope. Since component troubleshooting has (hopefully) isolated the trouble to within a small section of computer logic, an appropriate exercise or diagnostic loop can be used to

operate the suspected section of logic repetitively. When the machine is running in a closed exercise or diagnostic loop, the desired operating pulse or level is generated at intervals that are always multiples of the 8-microsecond memory cycle, or equal to an in-out device cycle.

The oscilloscope sweep may be synchronized to any of the timing pulses (each generated once per memory cycle). For convenience, the time shift pulse and timing pulses SP0 and T1 are available at insulated standoffs in panel 1A. The duration of the sweep may be set either to 1 microsecond per centimeter (so that the entire sweep displays one memory cycle), or to a value which displays one complete performance of the exercise or diagnostic loop.

Every pulse or level generated in a given section of machine logic is available at some plug-in module output pin. The pin locations are shown on the block schematic for that section of machine logic. In the case of a catastrophic malfunction, the signal tracing method determines with absolute certainty whether a pulse of good quality (amplitude, duration, and rise time) is being generated at the right time. In the case of an intermittent malfunction, this signal tracing technique must be combined with some appropriate form of aggravation (discussed below).

Substitution is the technique which first occurs to most technicians. Usually a spare plug-in module is substituted for a suspected module to see whether the malfunction is thereby cured. When troubleshooting registers and counters, however, it is often more useful to exchange bits of the register or counter rather than substituting a spare module. After the exchange, if the malfunction has moved to the new location, the trouble is probably in the exchanged module. However, if the malfunction still affects the original location, the malfunction is more likely to be in some logic network supplying pulses or levels to that location.

Aggravation, as an electronics maintenance technique, sounds as though it should be scrupulously avoided; it is actually quite useful. In the troubleshooting of intermittent malfunctions, aggravation is often the only technique which gives any indication of malfunction location. The two main types of aggravation are vibration and marginal check. Marginal check voltage application, as a method of finding weak components or malfunctions due to program-linked differences in circuit loading, is discussed in

c above. Vibration, as a malfunction locating technique, is used primarily to locate intermittent connections.

As long as reasonable care is used to avoid inflicting permanent damage, the technician should not hesitate to twist, probe, worry, or poke at connections, cables, plugs, or plug-in units. All connections in PDP-4 are designed for excellent reliability. Connections through plugs and sockets, and through cables, should be immune to any reasonable amount of pulling, twisting, or flexing. If such aggravation produces a computer error, an intermittent logic connection is probably causing the malfunction. Procedures for finding intermittent connections in individual plug-in units are described in paragraph 11-10.

Intermittent failures caused by poor connections cannot be located merely by using marginal check. However, an intermittent connection can often be revealed by vibrating the modules while running an appropriate maintenance program. Often wiping the handle of a plastic screwdriver across the back of the suspected row of modules is a useful technique. The resulting vibration generally interrupts an intermittent connection.

By repeatedly restarting the program and narrowing the area of vibration (tapping fewer and fewer modules) the malfunction can be localized to within one or two modules. After localizing the malfunction in this way, try wiggling the suspected module up and down within the mounting panel. If wiggling the module causes a computer halt, before removing the module closely inspect the associated mounting panel wiring.

Although each PDP-4 system is thoroughly tested before it leaves the factory, nevertheless, a poorly soldered connection may occasionally show up later. This type of malfunction appears as an intermittent failure and is sometimes very difficult to locate. Poorly soldered connections, if any, are more likely to appear in mounting panel or plug and cable connections than within the modules themselves.

e TESTING AFTER REPAIR - After a malfunction has been located and the defective plug-in unit or connection replaced or repaired, a complete test should be made of the entire system.

The procedures described above (console troubleshooting and logic troubleshooting) are

usually followed under the tacit assumption that only one malfunction is present in the machine. As a matter of fact, even after faulty parts related to one malfunction are located and repaired or replaced, the system may still contain other faults. In order to ensure that the PDP-4 is definitely in perfect operating condition, the entire MAINDEC should be run with the application of marginal check voltage after the completion of corrective maintenance procedures. Particular emphasis should, of course, be placed on those portions of MAINDEC which check the originally malfunctioning section of the computer logic.

A record of the computer malfunction and the way in which it was repaired must be entered in the maintenance record.

f MAINTENANCE RECORD ENTRIES - The first step of any troubleshooting procedure is an initial investigation of the malfunction (a above). This entails gathering all available information which might apply to the problem. The maintenance record forms a vital part of that information. It must therefore contain a clear, detailed, accurate description of every computer malfunction, giving the cause of the malfunction, the steps taken to isolate the malfunction, and the way in which the malfunction was finally repaired.

A maintenance log should not be constrained into a standardized rigid format; rather, it should look much like a diary. Computer malfunctions are much too diverse to categorize into any standard-form questionnaire. The date and time of each entry should be followed by comments describing everything that the technician does to the computer for whatever reason.

Accurate logs reveal at a glance the previous history of failures throughout the entire system. No one can be aware of every possible failure pattern of a sophisticated system such as PDP-4. Properly kept maintenance logs often reveal patterns of consistency among failures that seem totally unrelated. In troubleshooting, completely new lines of attack can often be suggested by such patterns of consistency. To take best advantage of this information, the maintenance log must be kept accurately and faithfully. The more information available on a trouble, the less computer down-time required before it is isolated and repaired.

11-10 MODULE REPAIR

When the location of a malfunction has been narrowed to within a specific module or small

group of modules, it may be worthwhile to continue troubleshooting within the unit. In many cases, a minute or two of additional oscilloscope signal tracing can isolate a malfunction to a particular transistor, diode, or connection. Considerable bench testing time can often be saved in this way, even if the module must be replaced. The following portions of this paragraph describe removal and replacement of modules, troubleshooting within modules, and circuit-component replacement.

a REMOVAL AND REPLACEMENT - Plug-in units may be extracted by means of the DEC type 1960 plug-in puller furnished with the PDP-4. Carefully hook the small flange of the puller over the center of the plug-in unit rim, and gently pull the unit out of the mounting panel. Use a straight, even pull to avoid damaging the plug connections or twisting the etched circuit. Since the puller does not fasten to the plug-in unit, prevent the unit from falling by grasping the rim of the unit in your other hand before the unit comes all the way out of the mounting panel.

When replacing a module, always position it so that the component side of the board is to the right, and the printed wiring side of the board is to the left. The aluminum rim of a module extends along the bottom edge beyond the plug. When a module is properly installed, this aluminum extension fits into a matching slot in the mounting panel. Should a module be installed with the bottom edge up, this aluminum extension prevents the plug from making contact with the socket in the mounting panel.

Carefully slide the module in between the guide ridges embossed on the mounting panel surfaces until the plug just begins to make contact with the socket. If the plug and socket are properly aligned, a gentle pressure is sufficient to fully insert the module. If the plug and socket are not aligned, do not force the connections. Occasionaly, slight movements of the module within the guide ridges may be necessary to match the plug with its connector. After a little practice, rapid removal and replacement of modules is very easy.

Connections to the power supply and power controls are made both by connections at barrier terminal strips and by cables terminating in plugs. Although both the wiring and the barrier terminal strip connections are color-coded, color-code markings denoting the proper connections may have rubbed off or become unclear. Before removing or replacing a power unit, clearly mark all ambiguous connections both on the unit to be removed and on the

spare to be installed. After disconnecting the unit, release it by removing the Phillips-head mounting screws on both sides. (The power units are fairly heavy, so get a good hold to avoid dropping them when they are removed.)

b MODULE TROUBLESHOOTING - Locating a malfunction within a single module or power unit can be done in two ways. The first (active circuit troubleshooting) involves use of the plug-in unit extender (DEC type 1954), the pigtail plug-in extender, the oscilloscope, and small two- or three-instruction exercise loops of the type described in paragraph 11-9c.

The second method is bench troubleshooting. This involves use of a suitable multimeter (paragraph 11-1) and other applicable bench test equipment such as an in-circuit transistor and diode checker, a regulated bench power supply, etc.

In complex installations, or in multiple installations, an independent bench module tester may be desirable. A bench tester for DEC plug-in modules can be made up from a type 722 power supply, standard DEC signal-generating plug-in units (clocks, pulse generators), and suitable switching circuits. Such a bench tester, when used with an oscilloscope, can provide active-circuit troubleshooting (signal tracing) independently of the computer.

A desirable addition to the bench module tester is a type 734 power supply. This supply permits marginal checking of plug-in units at the bench.

Information on system design with DEC modules, helpful in assembly of a bench tester, is contained in the Digital Modules Catalog (A-705) and the Digital Logic Handbook (A-400B), both available from DEC without charge.

(1) Unit Extender - The DEC type 1954 plug-in module extender permits troubleshooting a module while the system is operating. Remove the module to be tested and insert the extender in its place. Then plug the module into the exposed end of the extender. The unit is then accessible for active-circuit troubleshooting.

During active-circuit troubleshooting, marginal check voltages may be applied to an individual module by using the pigtail plug-in extender (paragraph 11-1 above). Pins A, B, and C of the exposed module can be furnished appropriate marginal check voltages through the three alligator clip leads of the pigtail extender.

CAUTION

Although DEC circuits are designed with internal safeguards which prevent damage from opening or shorting the output terminals on a single unit, they are not proof against all the accidental shorts which might be produced while testing the unit on an extender card. Care must also be exercised when testing terminals on the wiring side of the racks.

(2) Bench Troubleshooting - If simple inspection fails to reveal the cause of trouble, the use of multimeter resistance readings can usually isolate the trouble to a specific defective component.

Resistance readings may be taken to check the emitter-base and the collector-base diodes of transistors in both the forward and reverse directions. It is essential to determine the internal battery polarity of the multimeter. Often this polarity is opposite to the normal polarity of the leads as used for voltage and current measurements.

Resistance readings for both the emitter-base and collector-base diodes of a transistor should be relatively low in the forward direction, and relatively high in the reverse direction. Note that although incorrect resistance readings are a sure indication that the transistor is defective, correct readings give no guarantee that the transistor is good. It may have other troubles.

Several types of inexpensive in-circuit transistor and diode checkers are on the market. These generally provide a more reliable indication of diode or transistor malfunction.

Damaged or cold-soldered connections can also be located with the multimeter. Set the multimeter to the lowest resistance range and connect it across the suspected connection. Poke at wires and components around the suspected connection with a probe or with the fingers. Alternatively, rap the module sharply (but not too sharply) on a wooden surface.

Often the response time of a multimeter is too slow to detect the rapid transients produced by intermittent connections. Current interruptions of very short duration, caused by intermittent connections, can be detected by placing a 1.5-volt flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope, while probing the connection.

c COMPONENT REPLACEMENT - Use a six-volt soldering iron with an isolating transformer for removal and replacement of defective components. Avoid excessive heat which can cause damage to components and may even cause delamination of the etched wiring. Transistors and diodes require special care. Whenever possible, attach a copper alligator clip or other heat sink to the lead being soldered, thus reducing the amount of heat transferred to the component.

11-11 DRAFTING NUMBER SYSTEM

The numbering system used for DEC documentation is coded for identification and control purposes. This numbering system should always be used when ordering any drawings or lists from DEC. Consistent use of the system can also save you a considerable amount of time when filing and retrieving DEC documentation in your own files. The drawing identification code consists of up to 13 letters and digits making up eight individual data fields. These eight fields are summarized in the eight horizontal lines of Table 11-10 below.

TABLE 11-10 DOCUMENT NUMBER FORMAT

Typical Document Number	BS- D 4 00 01- 3 A- 1		
Field	Designates	Code	Comments
BS-	Document Type	2 letters	
D	Document Size	1 letter	A, B, C, D, or E.
004	Project Number	1, 2, or 3 digits	Initial zeros of the project number are omitted (see typical document number at the top of this table).
00	Serial Number	2 digits	Customer serial number for special equipment. Type numbers for project variations.
01-	Assembly	2 digits	Designates a particular portion of project equipment.

TABLE 11-10 DOCUMENT NUMBER FORMAT

(continued)

Typical Document Number	BS- D 4 00 01- 3 A- 1		
Field	Designates	Code	Comments
3	Subassembly	1 digit	
A-	Revision	1 letter	To indicate system revision.
1	Change	1 digit	To indicate changes in document when a revision letter cannot be used.

a DOCUMENT TYPE - The first two letters of the identification code give the document category. The first of these two letters specifies the content of the document, for example -- B: block, C: circuit, W: wiring, etc. The second letter specifies the form layout or format of the document. For example -- S: schematic, L: list, etc. Most of the DEC document categories are listed below with short descriptions (Table 11-11) .

TABLE 11-11 DOCUMENT CATEGORIES

Code	Category	Description
BD	Block Diagram	Diagram of the components, subassemblies, or complete assemblies of a system showing logical interaction.
CD	Cable Diagram	A block configuration diagram of a system, showing the cabling between assemblies. Gives DS and WD drawing references for each assembly.
FD	Flow Diagram	Represents the logical behavior of a system with respect to a series of states, or with respect to time.
TD	Timing Diagram	Shows the timing relationships of a system containing or controlling some mechanical device.

TABLE 11-11 DOCUMENT CATEGORIES (continued)

Code	Category	Description
WD	Wiring Diagram	Shows the wiring of a subsystem or assembly. Used primarily in manufacture.
CL	Cable List	Gives wire colors, plug and socket pins, and names of signals for a specific cable.
DL	Diode List	Lists terminal points connected by diodes not contained in modules.
ML	Module List	Lists each module used in a system. Often gives logic function of modules.
PL	Parts List	Lists each part of an assembly. Gives part numbers.
RL	Replacement List	Shows all drawing revisions and serial codes for each particular system of a project.
TL	Terminator List	Lists the points at which lines must be terminated by load resistors.
WL	Wiring List	Gives terminal points connected by wires.
BS	Block Schematic	A system layout drawing where symbols are used for logical functions.
CS	Circuit Schematic	The schematic drawing of a particular circuit; shows DEC part numbers.
RS	Replacement Schematic	The schematic drawing of a particular circuit; shows JEDEC part numbers.

b SIZE LETTER - Although many documents are reduced to a size which can be included in a system manual (i.e., 11" by 17" maximum) they are initially drawn and revised on any of five sheet sizes. These sizes are:

A..... 8-1/2" x 11"
B..... 11" x 17" (twice A size)
C..... 17" x 22" (twice B size)

D..... 22" x 34" (twice C size)

E..... All sizes larger than D. Most E-size DEC drawings are 30" x 42".

c PROJECT NUMBERS - Every document applies to a particular project series which is denoted on the document by a number of one, two, or three digits. Since initial 0s are suppressed, project numbers less than 100 appear as two-digit numbers, and project numbers less than 10 appear as single-digit numbers. Project numbers are assigned only to central designs which form the basis for several different systems. Although machines are often modified for particular applications, all machines having a project number are basically similar in design and performance. To date, all project numbers have been single-digit numbers.

Some examples are:

2..... (002) PDP-1

3..... (003) ..... PDP-1 -- for a customer requiring many systems

4..... (004) PDP-4

d SERIAL OR CUSTOMER NUMBER - The serial number is used to denote a change or deviation from the standard documents for a machine. When an assembly or subassembly is modified for a particular customer application, all documents which apply to the modified machine show the two-digit serial number as part of the document number. Normally, all standard machines have the serial number 00, which signifies the standard design. When a particular customer application requires specific additional equipment which operates with the standard machine, documents are identified by the serial number, the assembly number, and the subassembly number taken together.

e ASSEMBLY NUMBER - The two-digit assembly number identifies some portion of a complete system. The size of the assembly may vary, depending upon the size of the system. For PDP-4 documentation, the assembly numbers are as follows:

01- ..... Internal Processor

02- ..... Memory

03- ..... Console and Power

04- .... Real Time Interface (Type 25 of the PDP-4)

05- .... Paper Tape Reader and associated logic

06- .... Paper Tape Punch and associated logic

07- .... Keyboard/Printer and associated logic

08- .... Magnetic Tape and associated logic (Type 54 for PDP-4)

09- .... Card Reader and associated logic

f SUBASSEMBLY NUMBER - The one-digit subassembly number identifies a section of a larger complete assembly. A given assembly may be made up of a large number of electrical and mechanical subassemblies. For example, the subassemblies which form the PDP-4 internal processor assembly are:

01- .... Internal Processor

1..... Timing

2..... States

3..... Arithmetic Unit I

4..... Arithmetic Unit II

5..... Memory Address Register

6..... Memory Buffer

7..... Program Counter

As a second example, the subassembly numbers of the PDP-4 Type 25 real-time option assembly are as follows:

04- .... Real Time Interface (Type 25 in PDP-4)

1..... Real time control logic

2..... Information collection logic

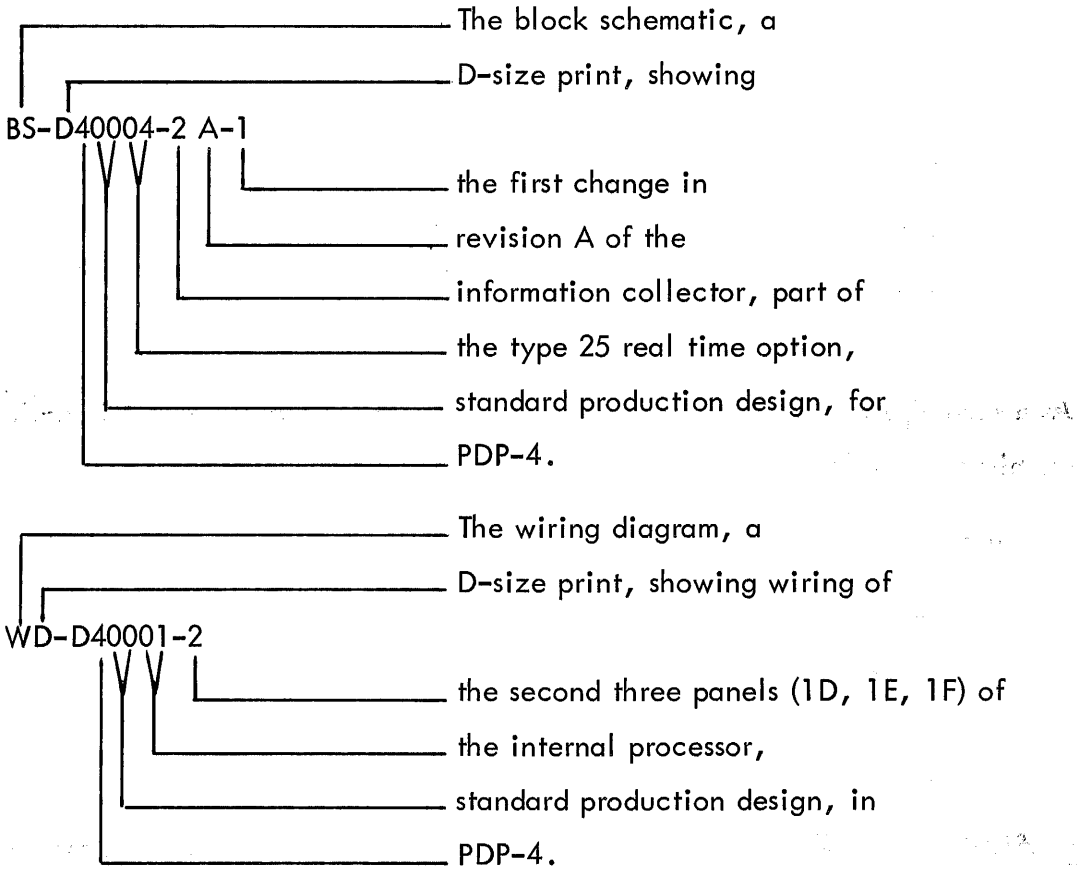
3..... Information distribution logic

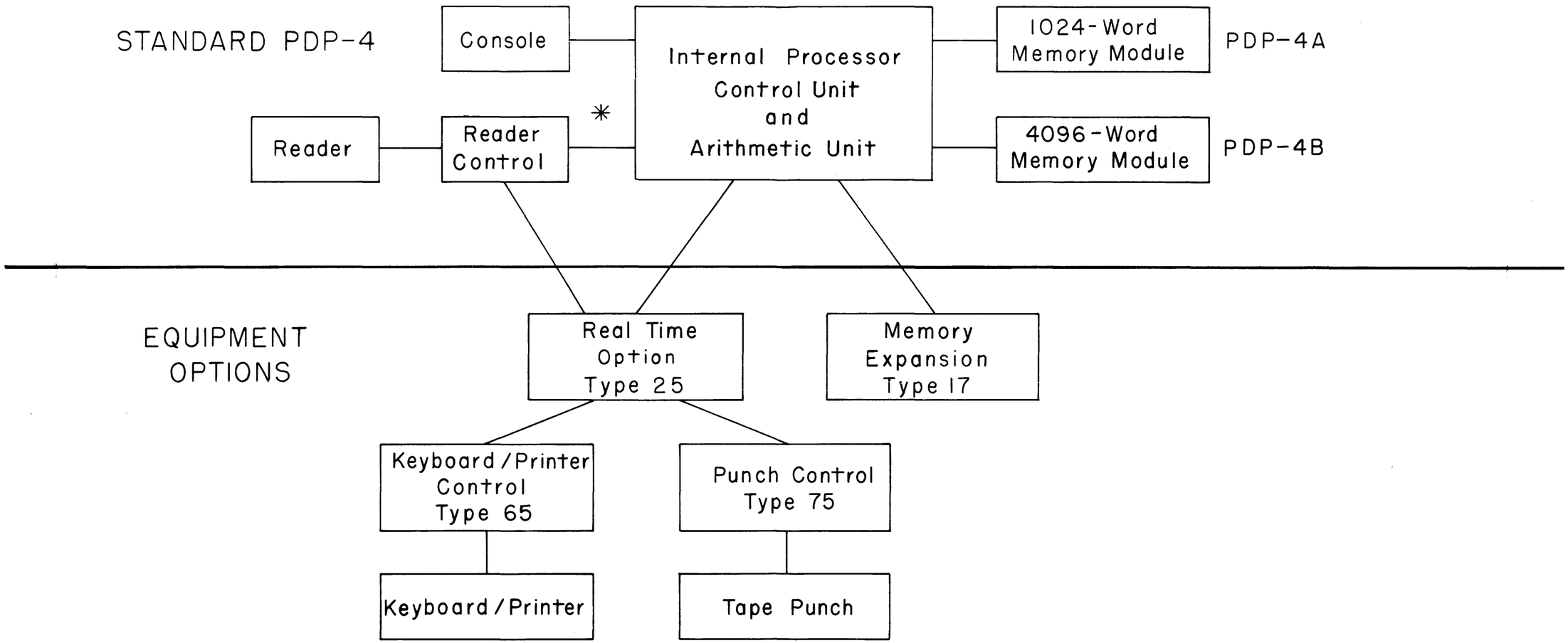
4..... Information source/sink selection logic

g REVISION LETTER AND CHANGE NUMBER - The revision letter signifies that the standard design of a subassembly has been revised or improved. All subsequent machines are constructed from documents bearing the latest revision letter. Normally, a revision letter denotes a change made in the design of all systems in a project.

The change number is used only when a revision letter cannot be used. Change numbers signify changes in the design of a system originally constructed from documents of an early revision. Suppose, for example, that a number of machines have been constructed from documents bearing the revision letter "A", while current production follows the B revision. When an earlier machine is modified to conform to current design, it then carries the "B" label and the B revision documents apply. However, if other modifications are made to an A machine which do not bring the machine to B status, then the revision letter "A" still applies. To show the change, the one-digit change number is added to the revision letter as a suffix, e.g., A-1, A-2, etc.

h FORMAT EXAMPLES - Presented below are two examples of the document number system as applied to documents for PDP-4.





* This Link Omitted if
Real Time Option
Type 25 Installed

Figure 2-1 PDP-4 System Configuration Diagram

Figure 2-2 PDP-4 with Reader, Punch and Keyboard/Printer

Figure 2-2

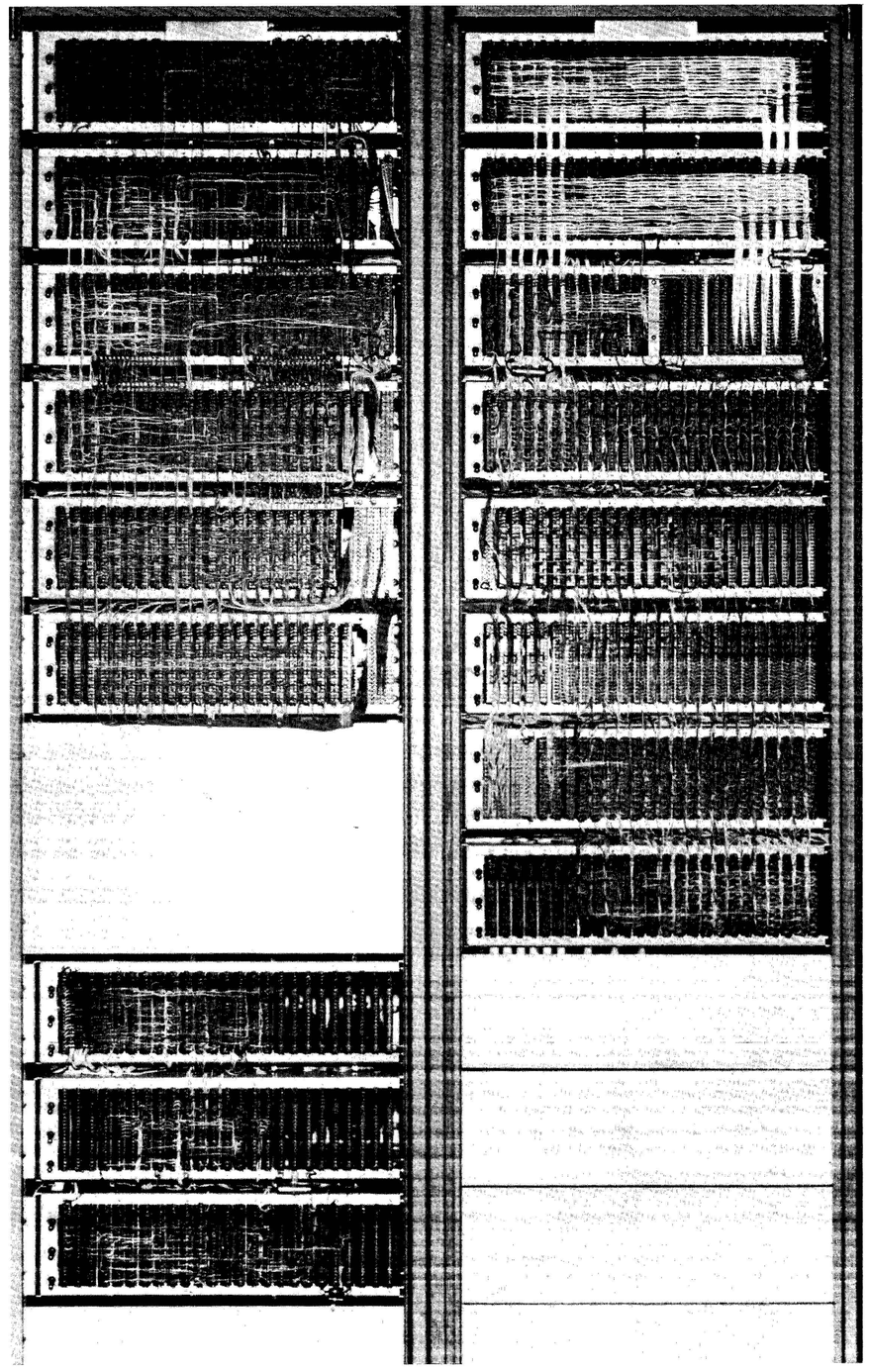


Figure 2-3 PDP-4 Logic Panels

Figure 2-3

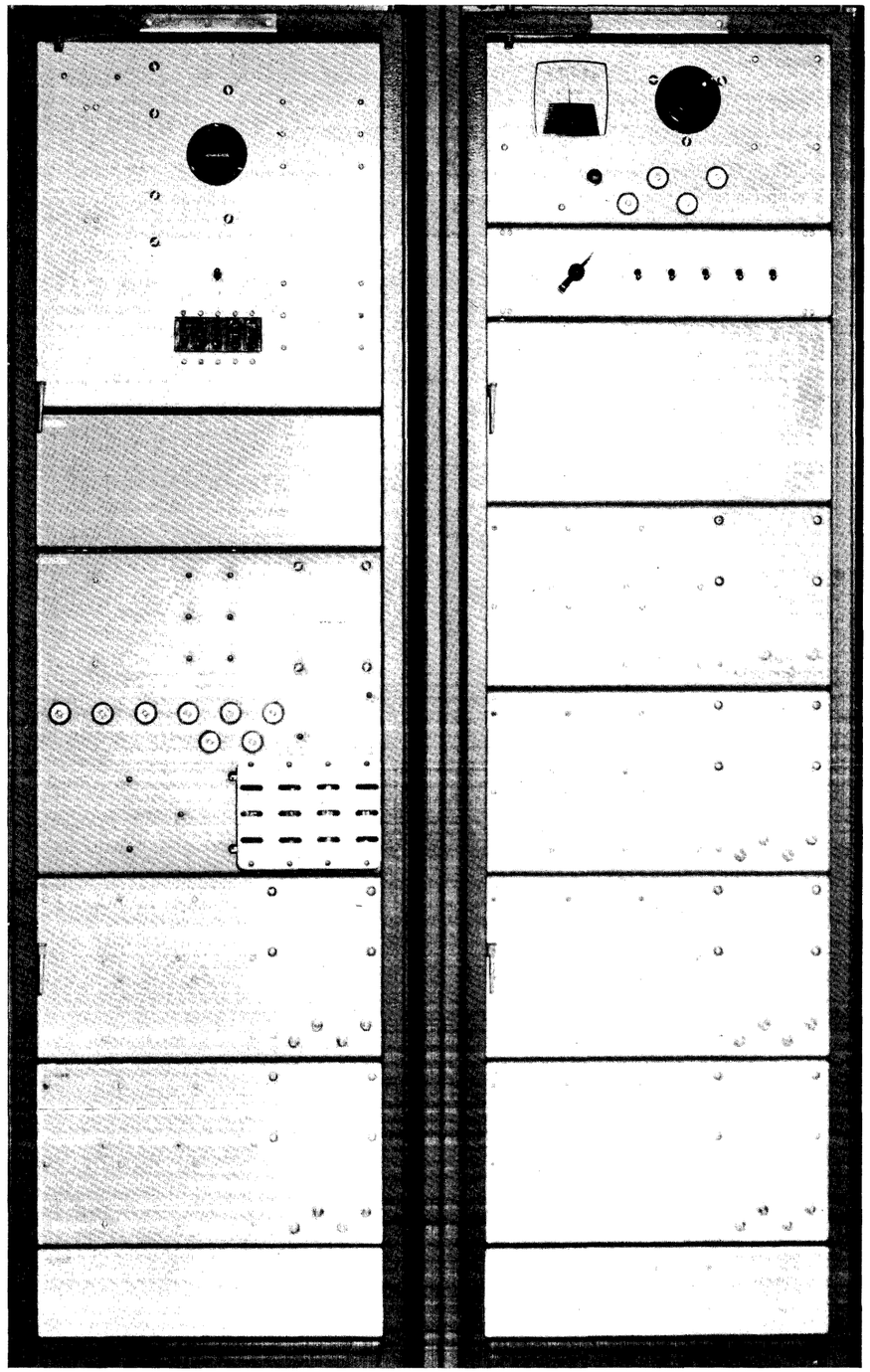


Figure 2-4 Plenum Doors, Back View of PDP-4 Bays

Figure 2-4

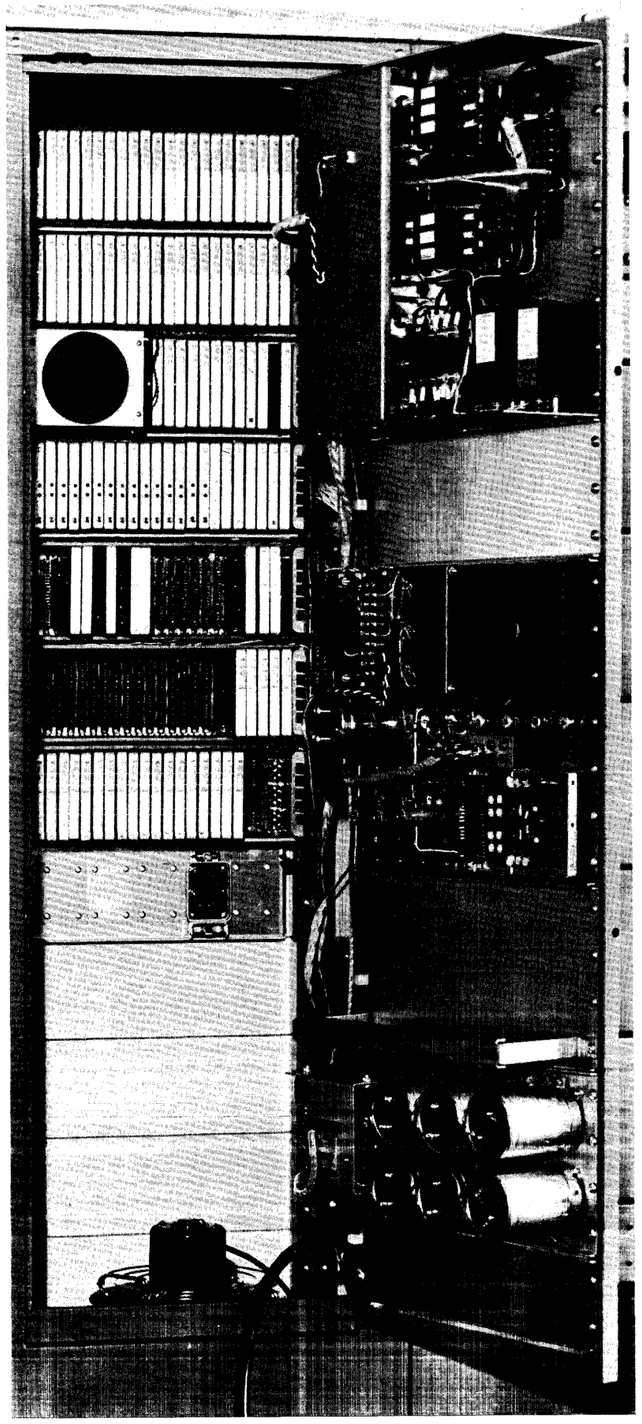


Figure 2-5 Interior of Bay 2

Figure 2-5

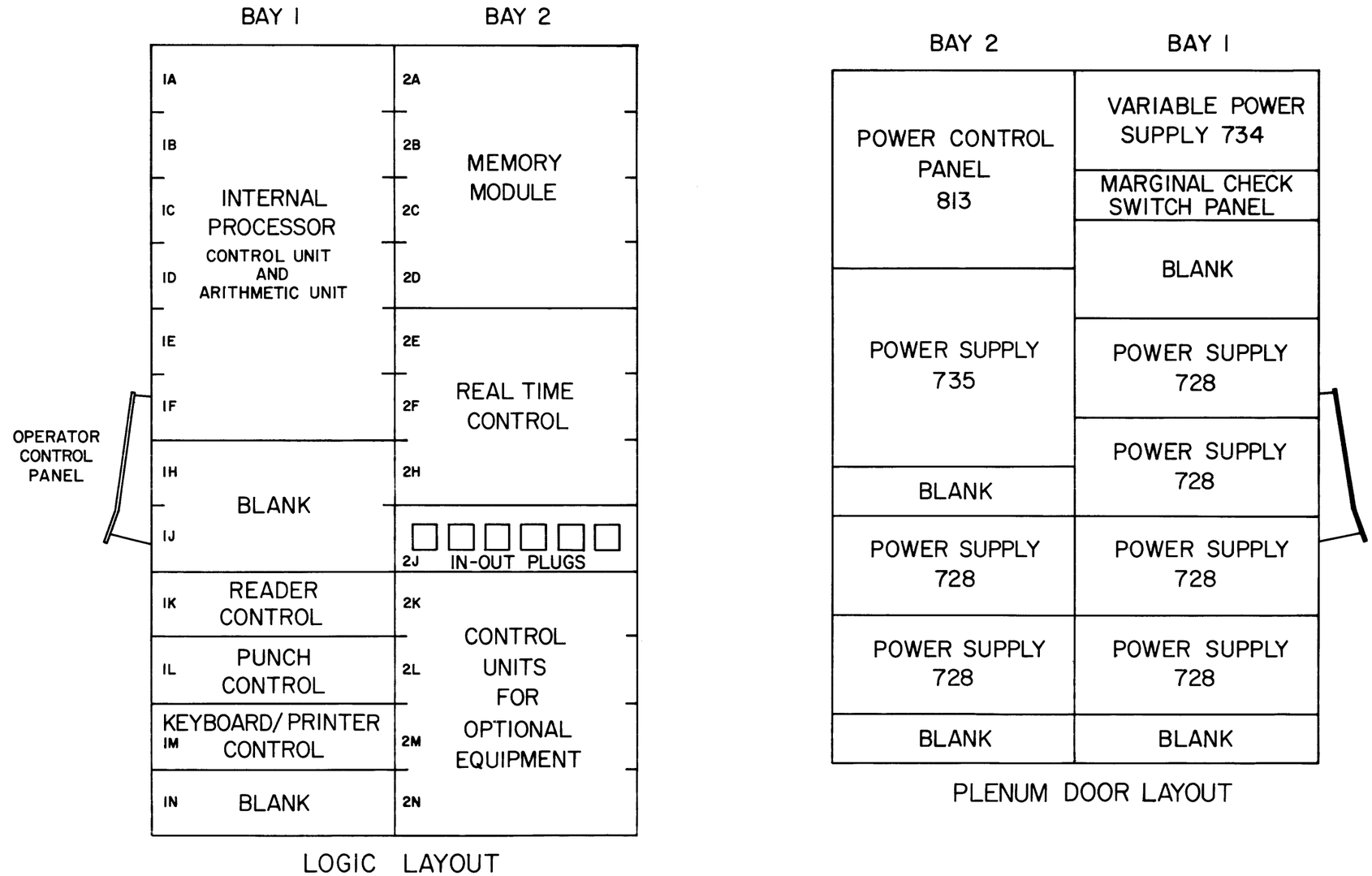


Figure 2-6 PDP-4 Layout Diagram

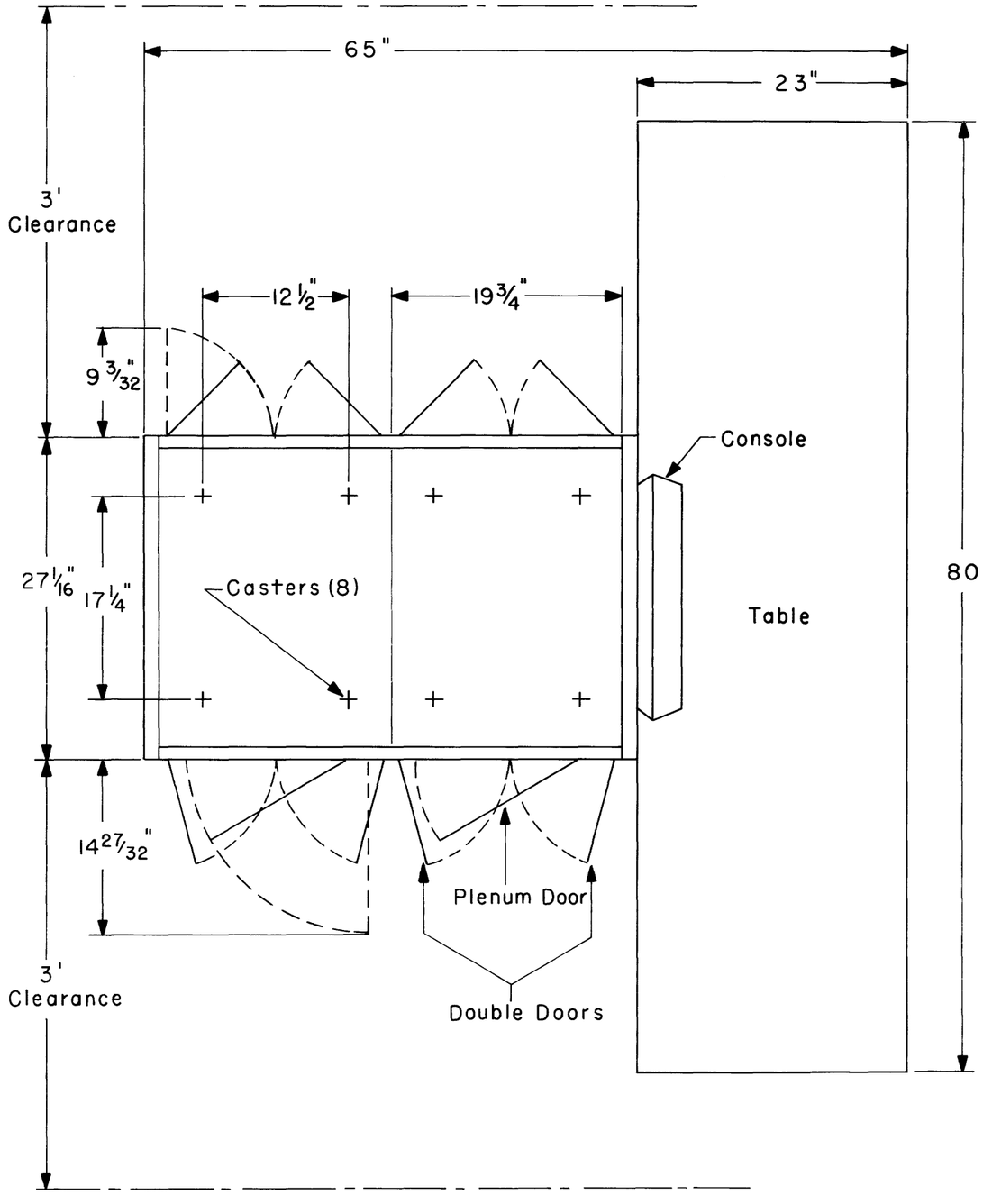


Figure 3-1 PDP-4 Top View

Figure 3-1

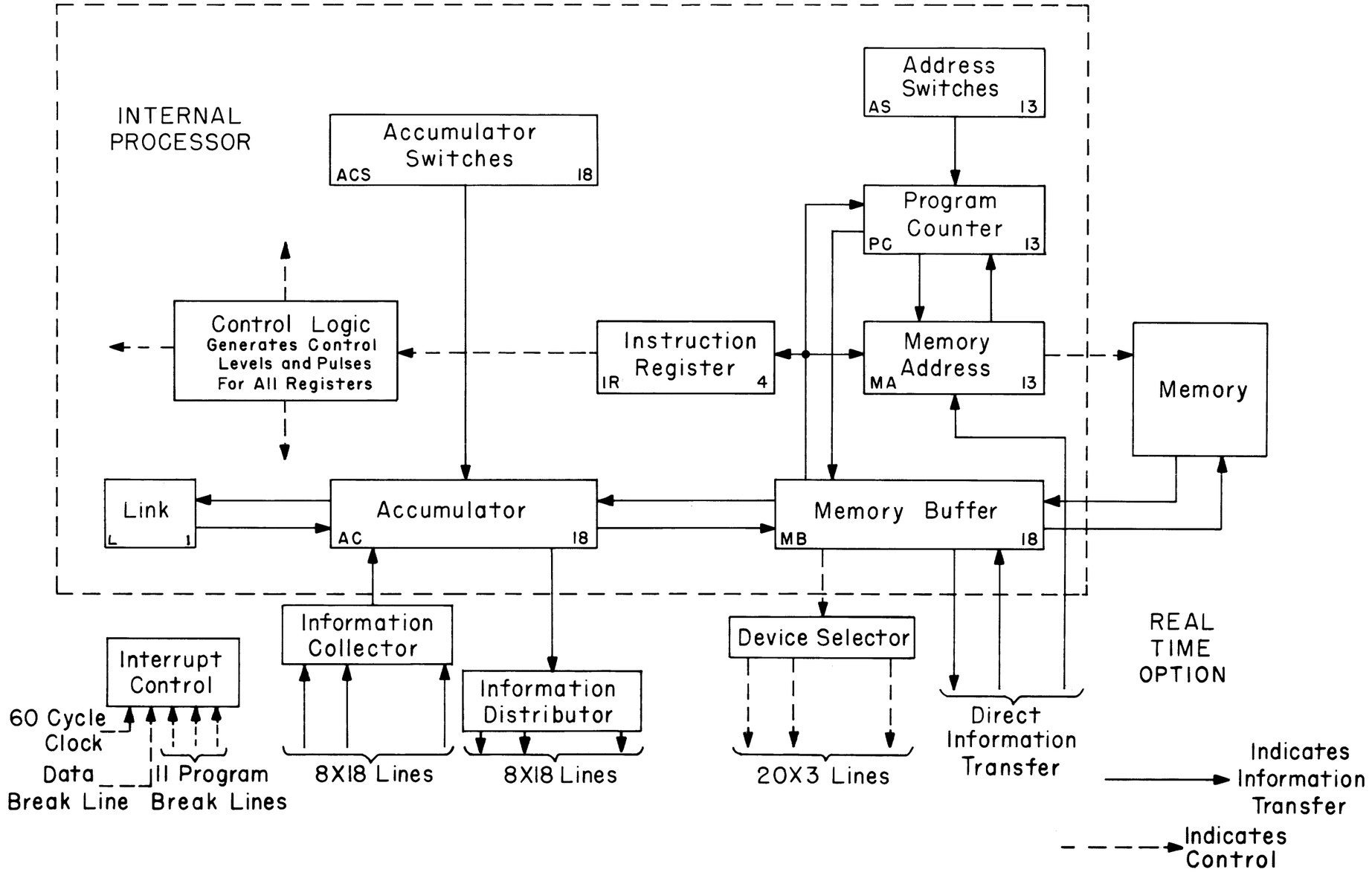


Figure 4-1 PDP-4 Logical Organization

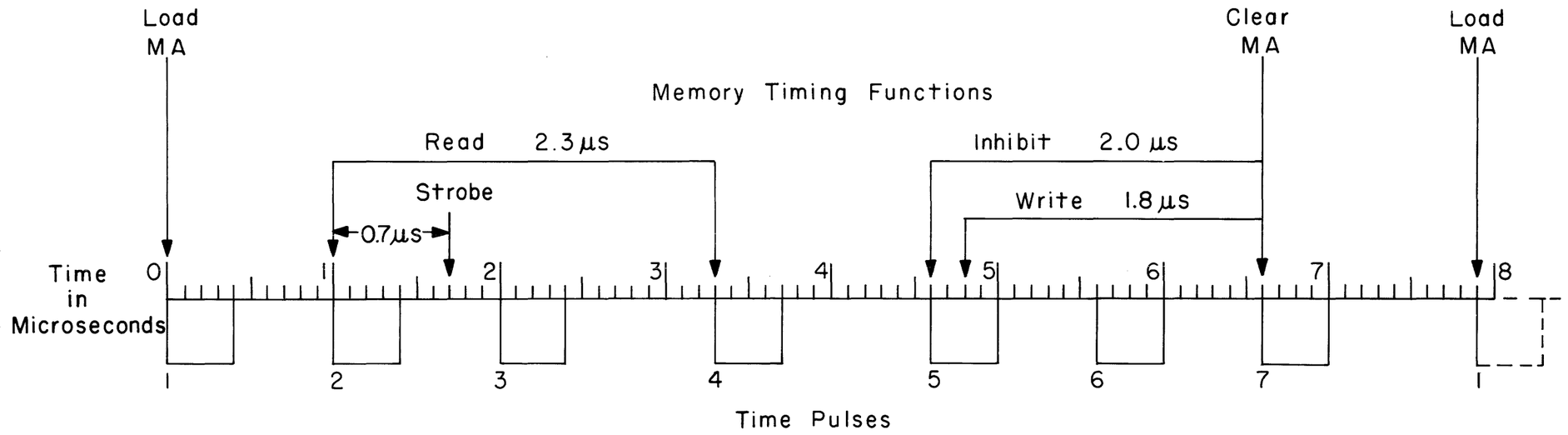


Figure 4-2 Computer Memory Cycle

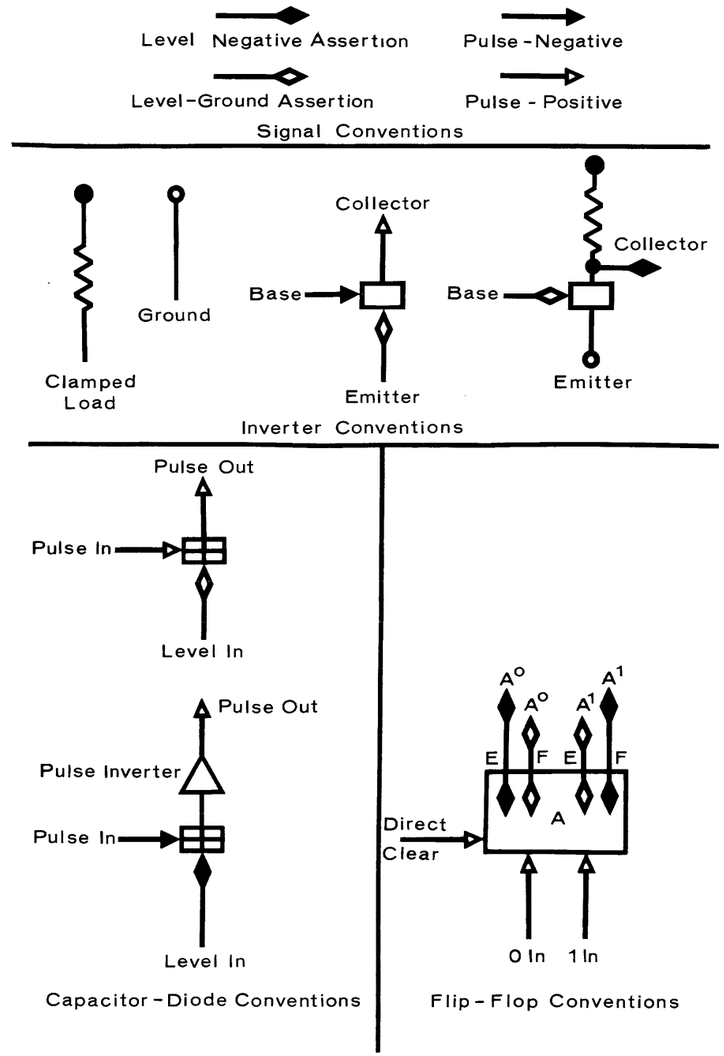


Figure 4-3 PDP-4 Logic Symbols

Figure 4-3

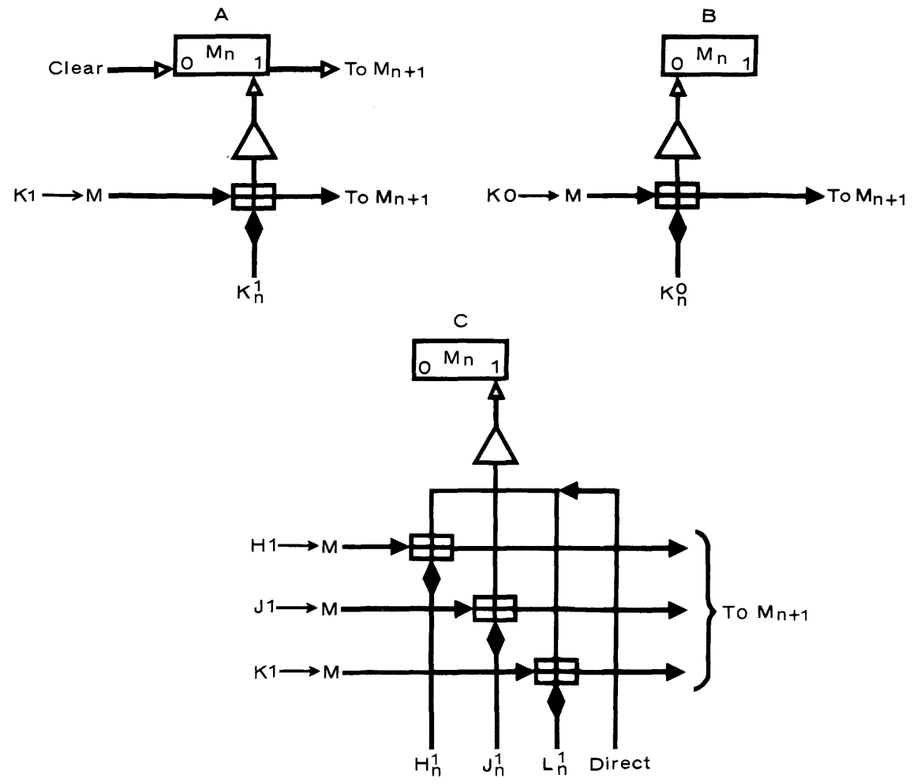
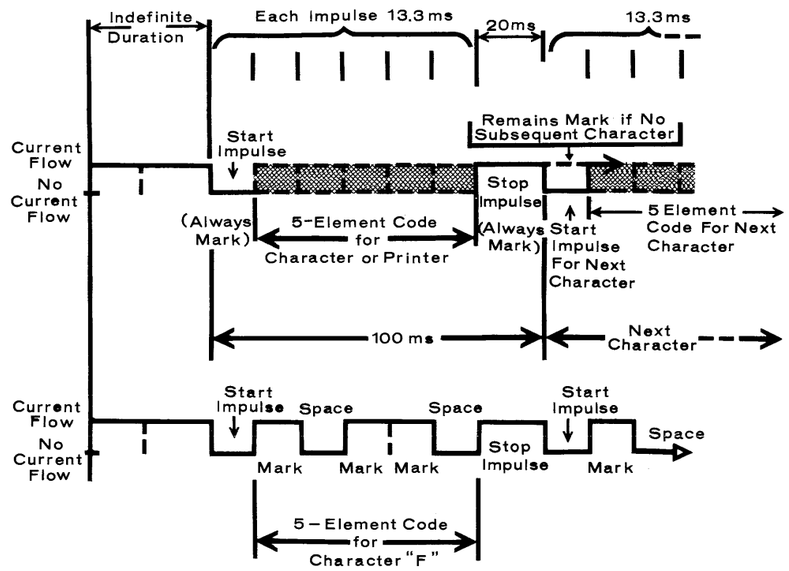


Figure 4-4 Transfer Logic

Figure 4-4



"Mark" Denotes Current Impulse; "Space" Denotes No-Current Impulse

Figure 4-5 Teletype Code Timing

Figure 4-5

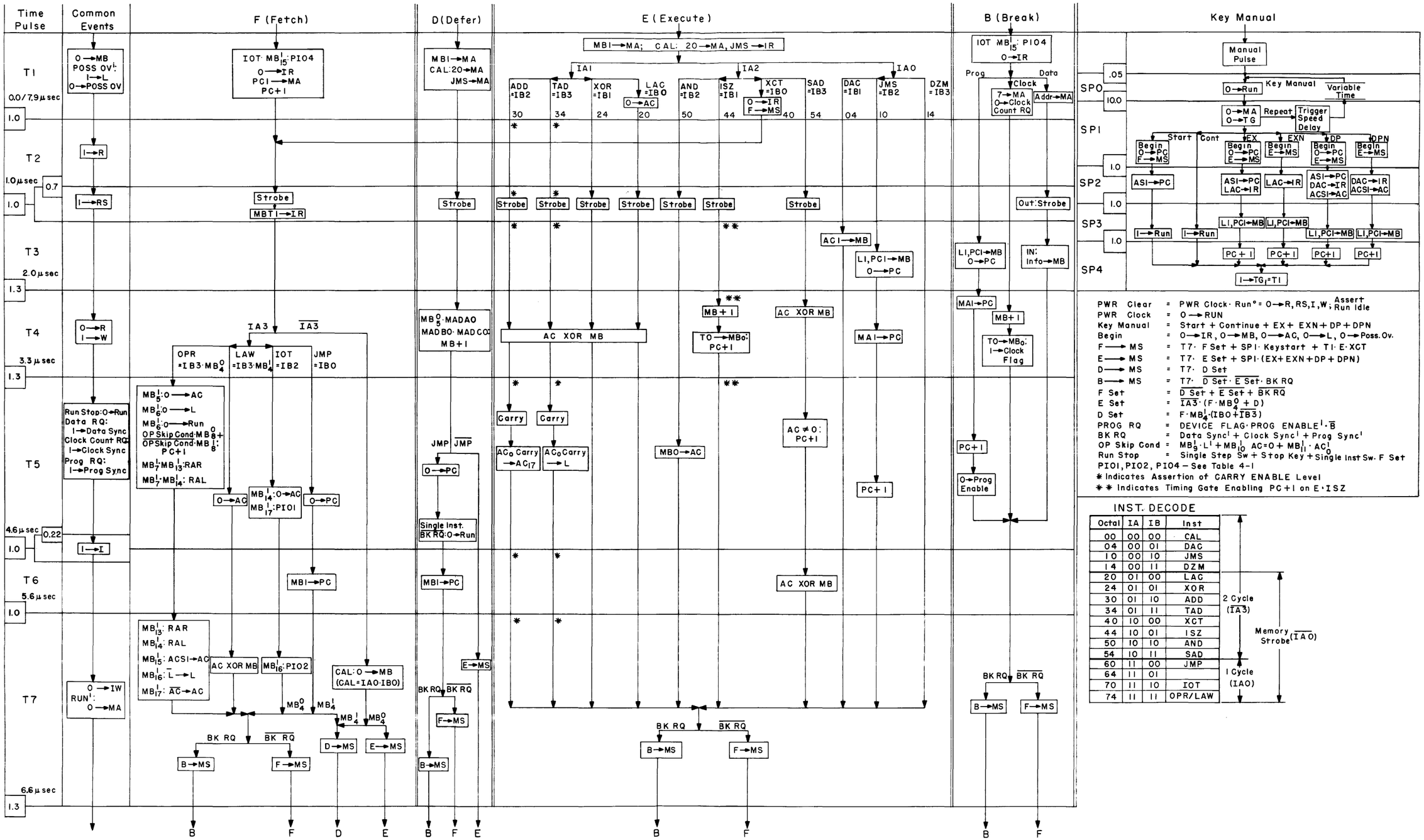


Figure 4-6 Flow Chart: Internal Processor Operations

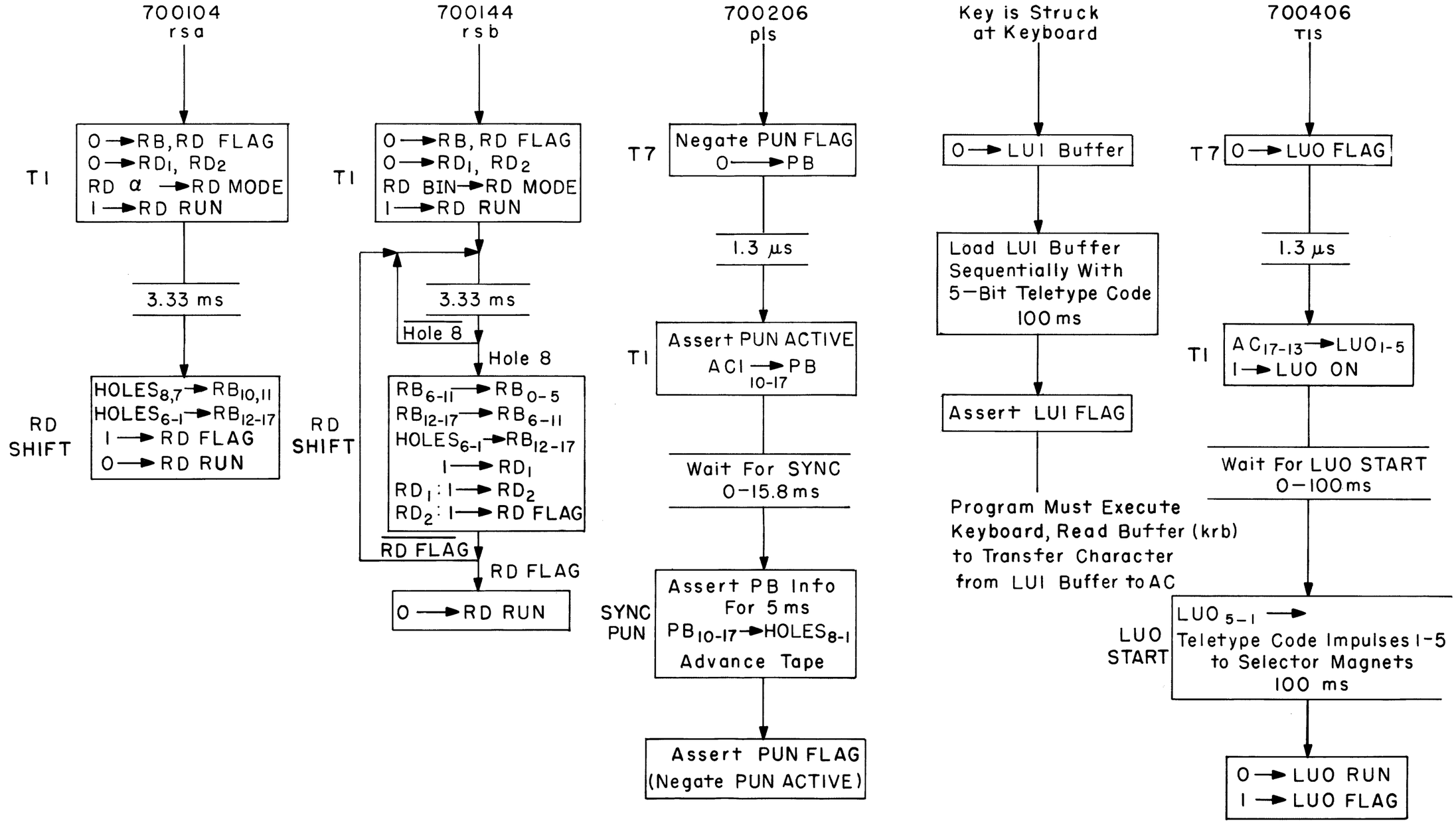


Figure 4-7 Flow Chart: Inout-Output Operations

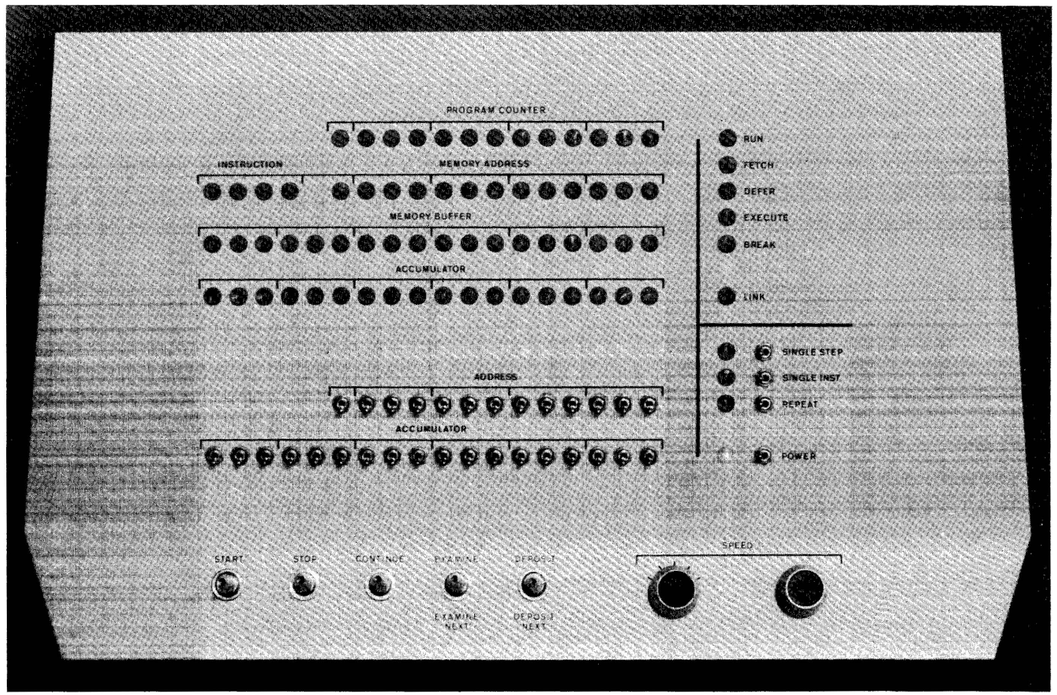


Figure 5-1 Operator Control Panel

Figure 5-1

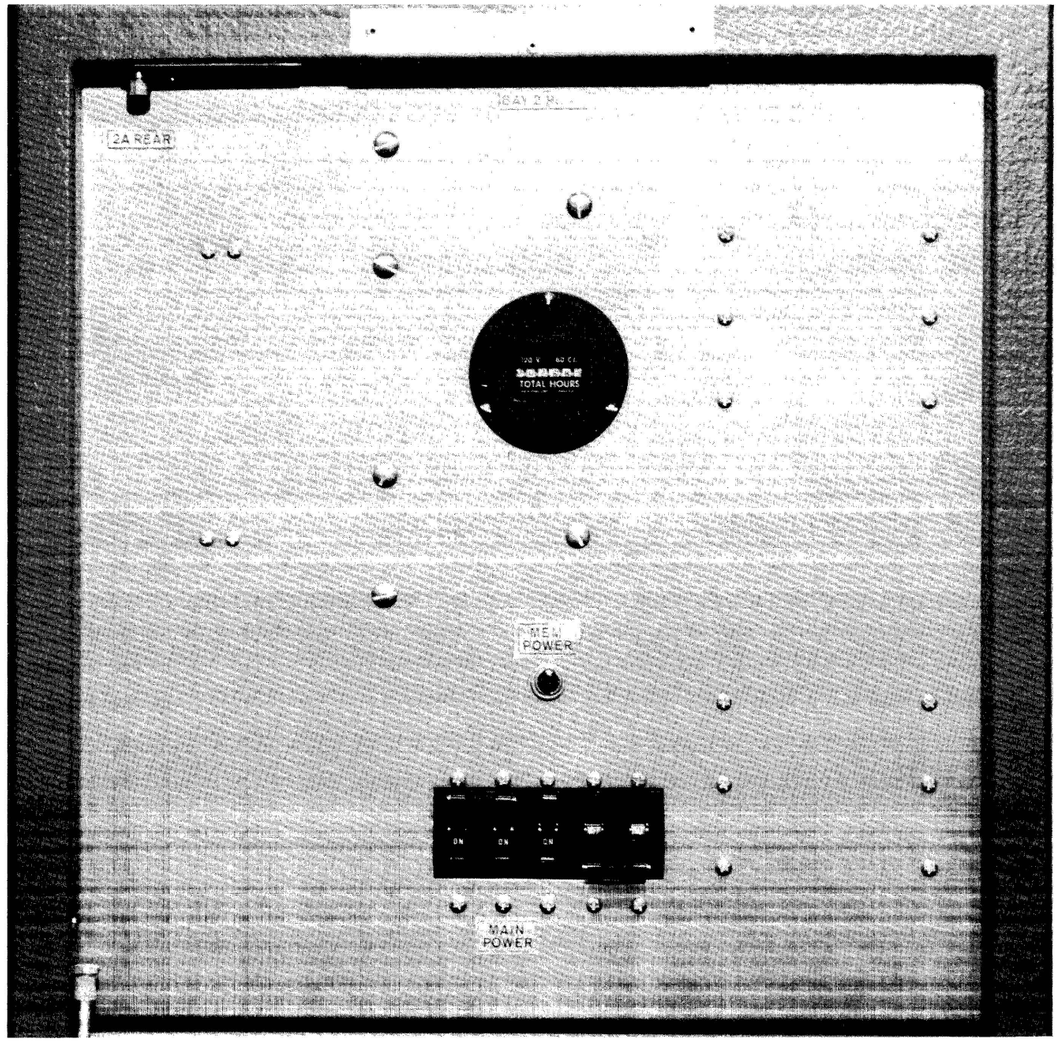


Figure 5-2 Power Control Panel Type 813

Figure 5-2

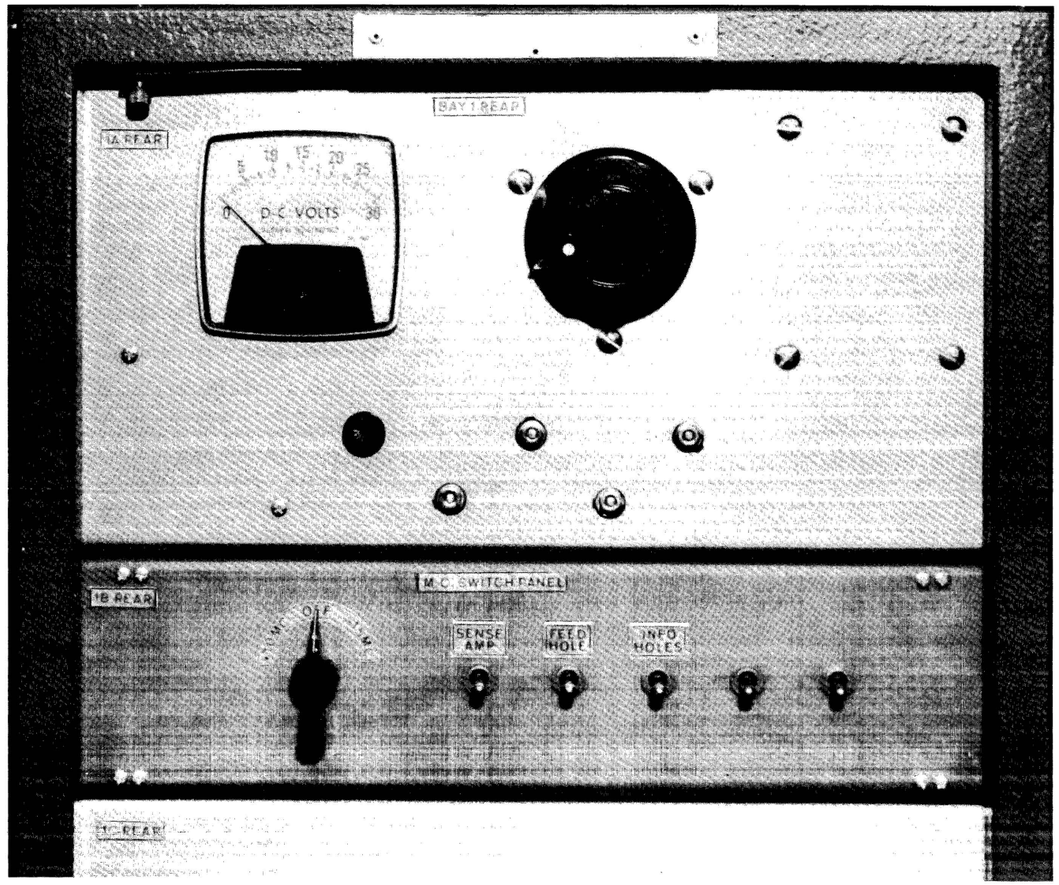


Figure 5-3 Variable Power Supply Type 834 and Marginal Check Switch Panel

Figure 5-3

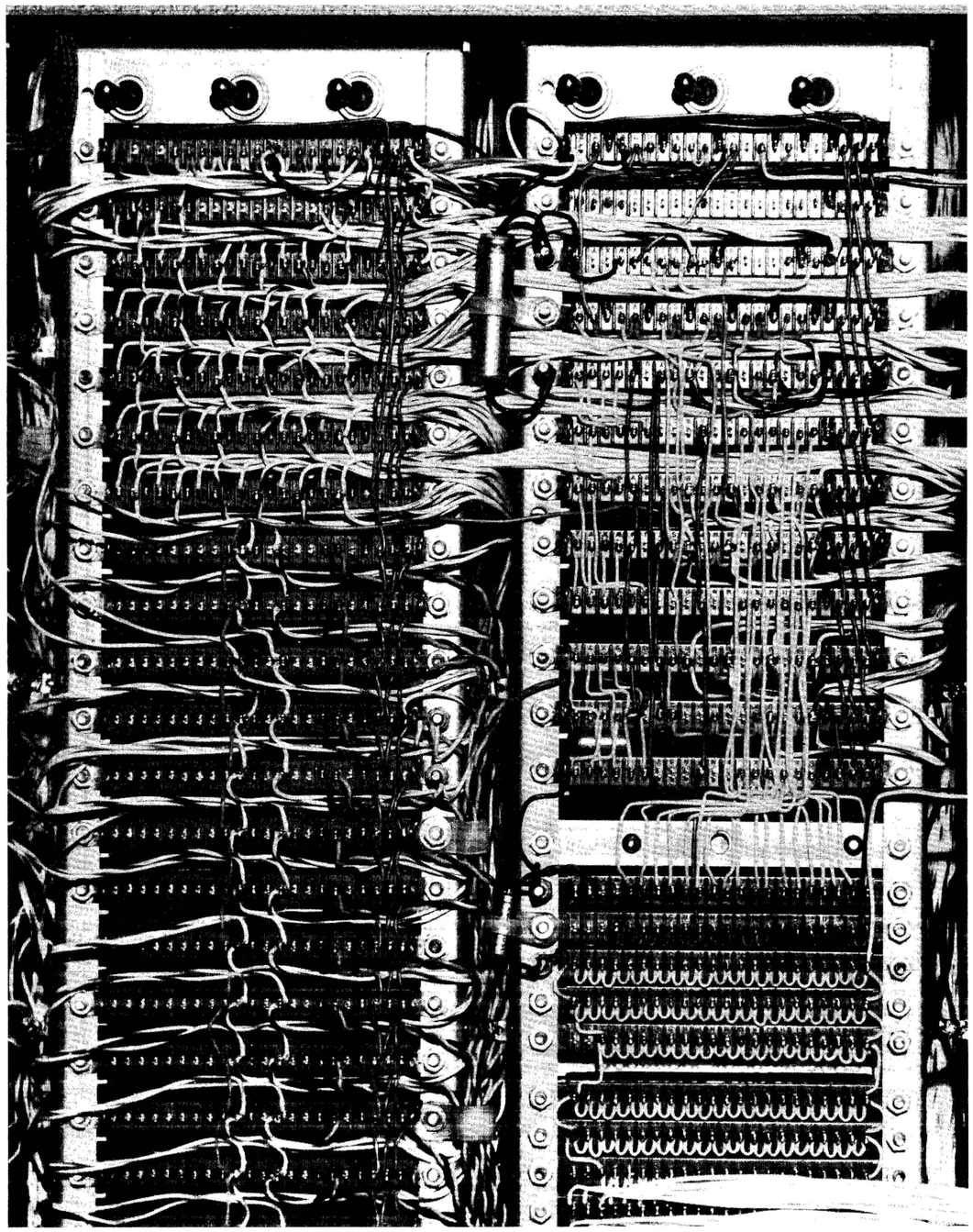


Figure 5-4 Marginal Check Toggle Switches on Mounting Panel

Figure 5-4

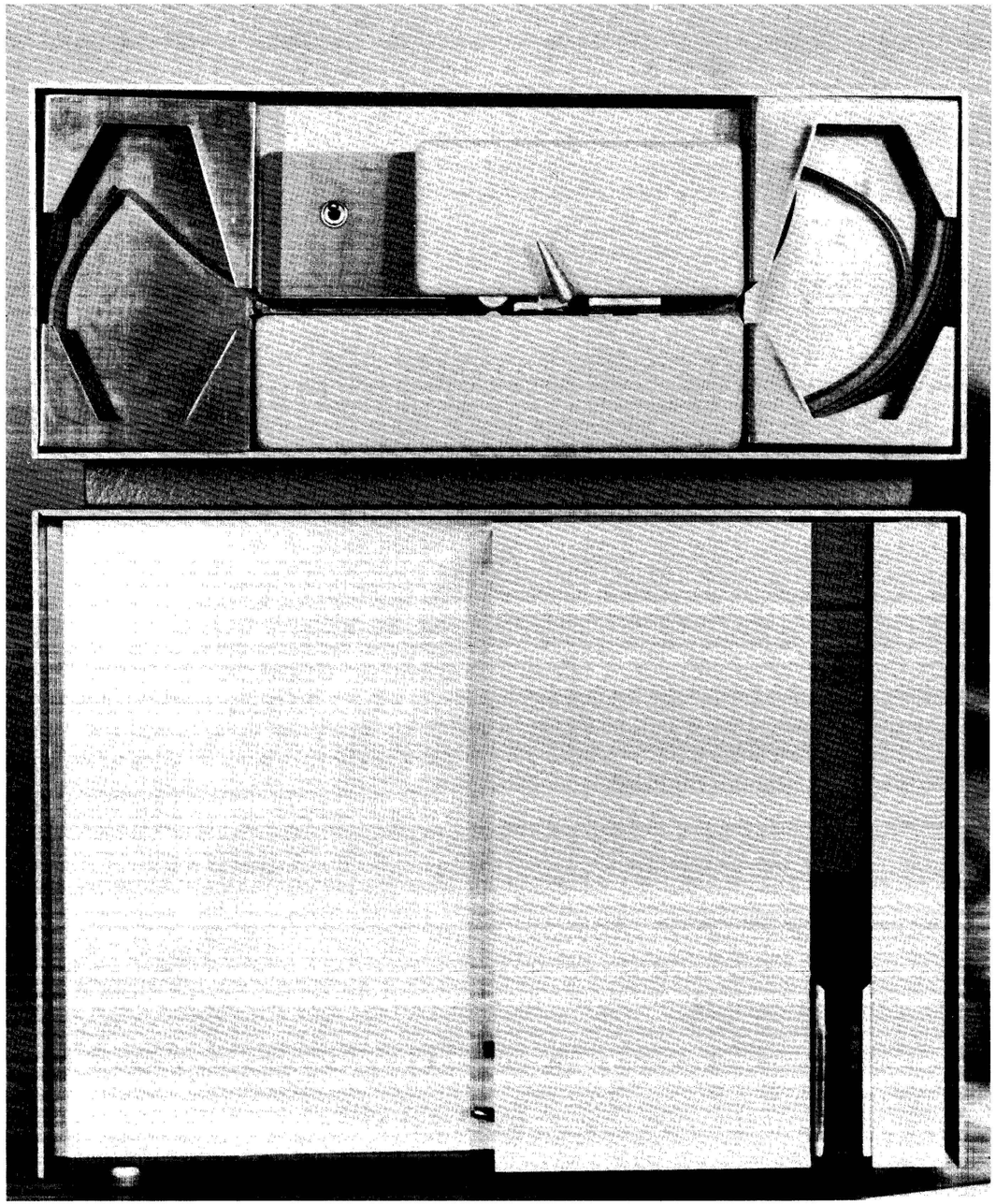


Figure 5-5 Paper Tape Reader (mounted on punch cabinet)

Figure 5-5

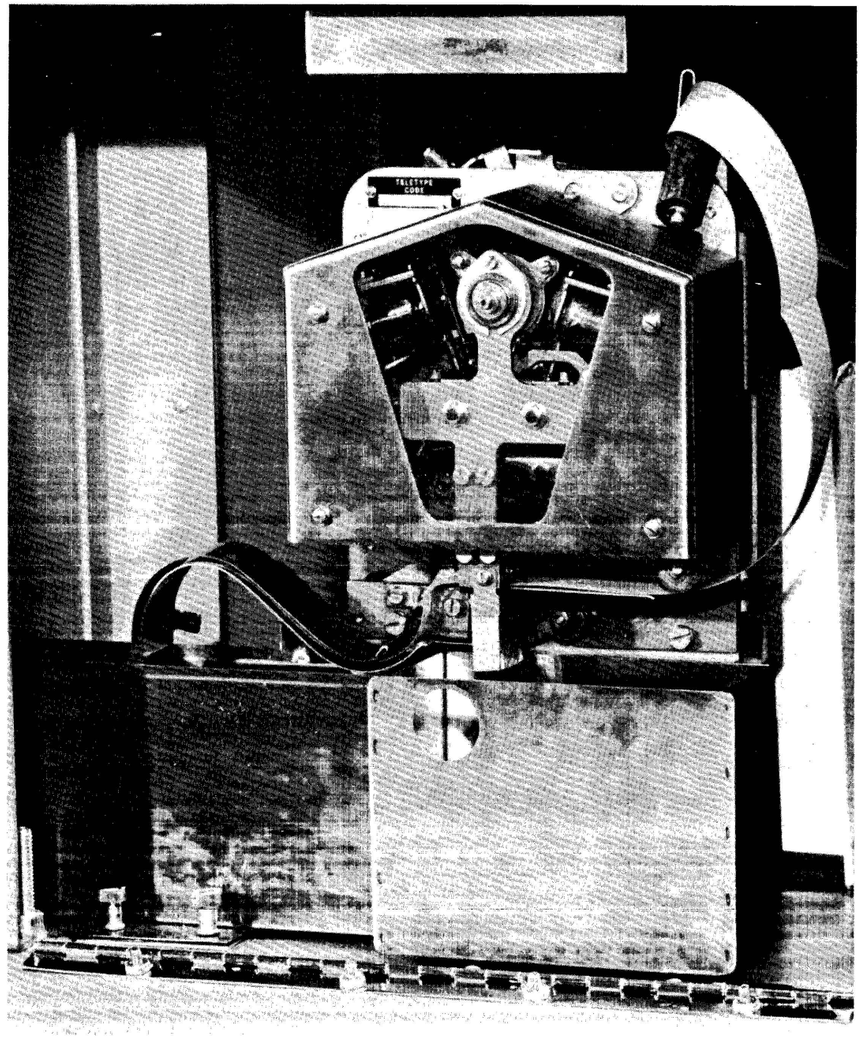


Figure 5-6 Paper Tape Punch

Figure 5-6

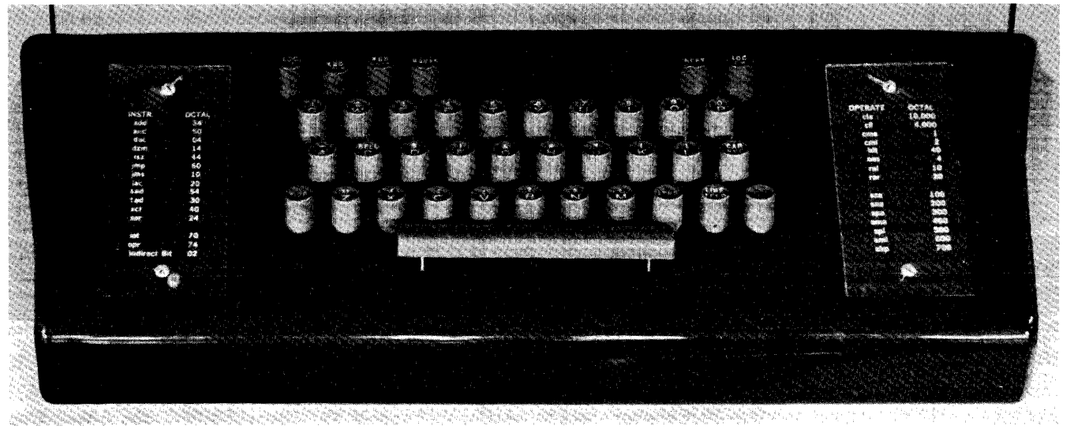


Figure 5-7 Keyboard/Printer

Figure 5-7

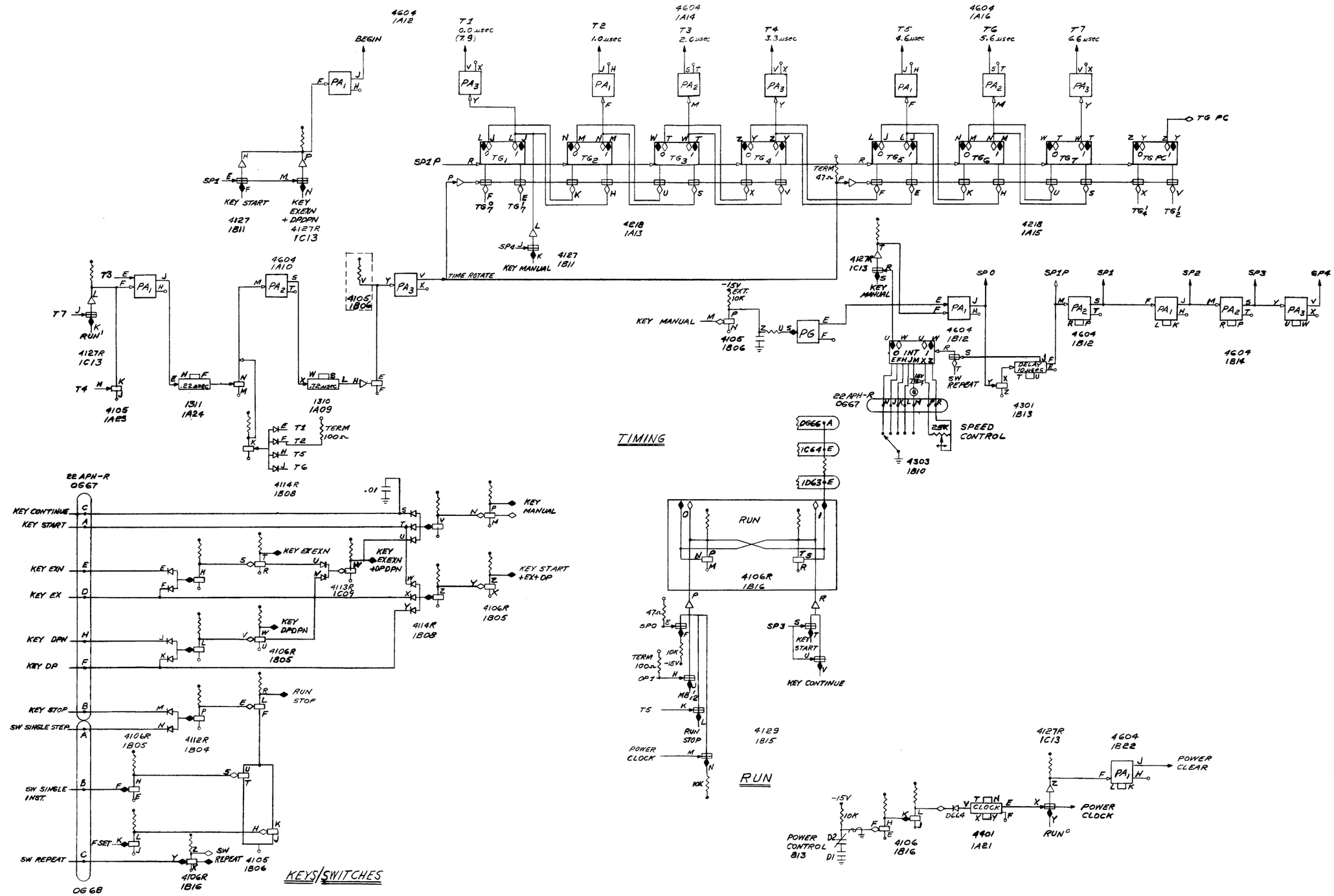


Figure 6-1 Keys, Switches, Time, Run

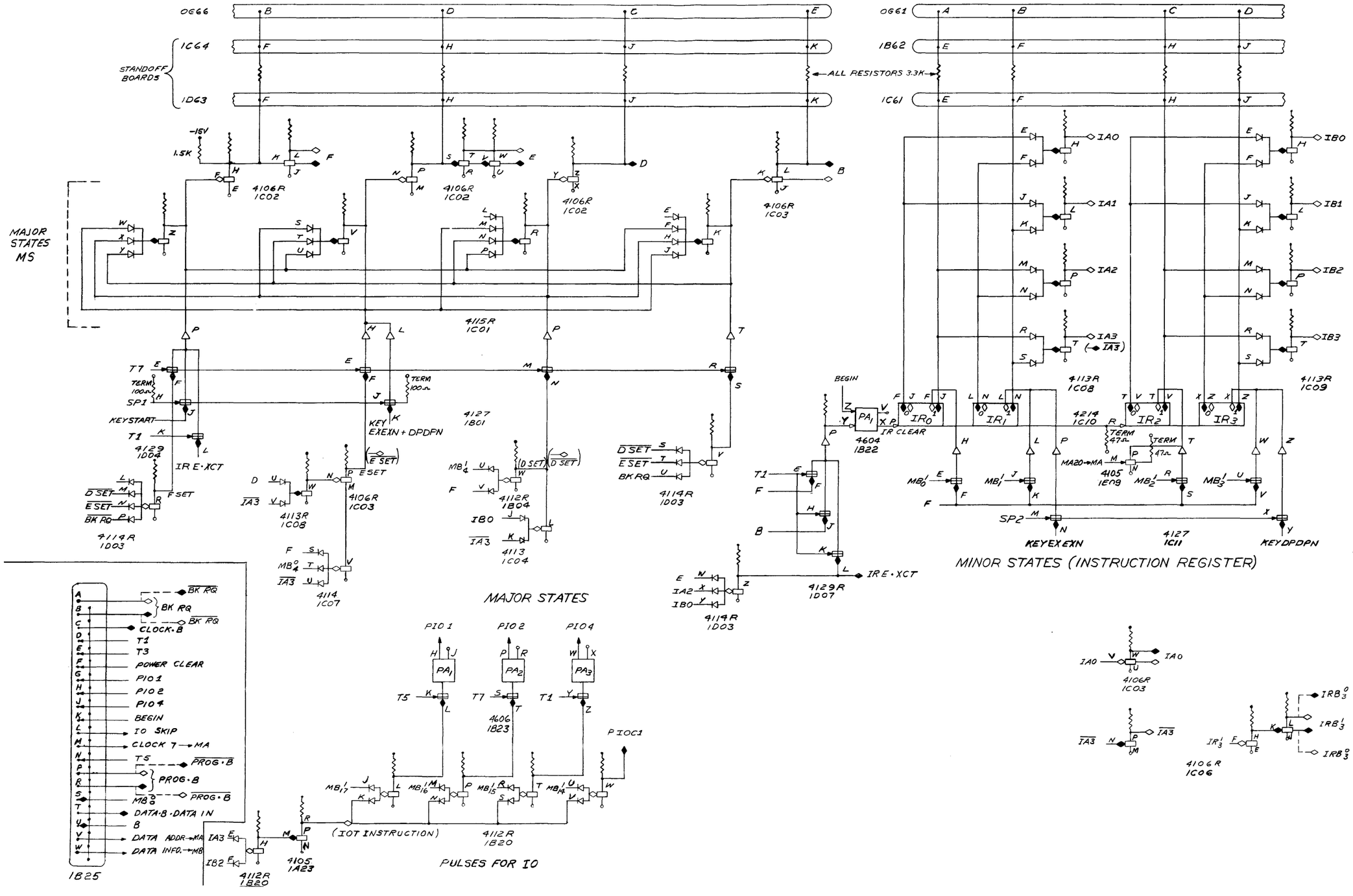
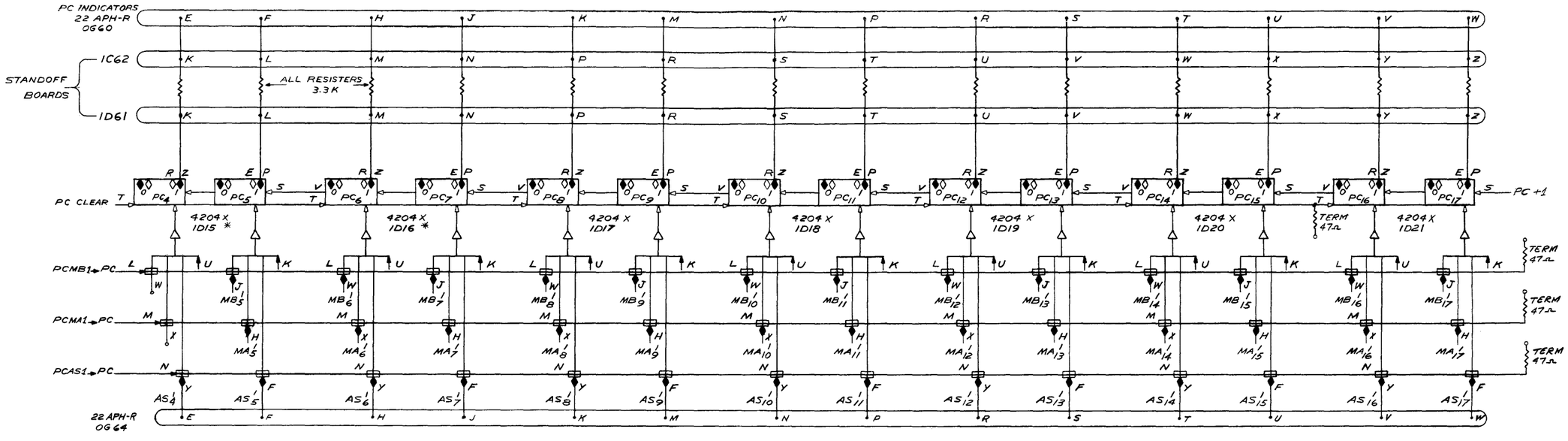
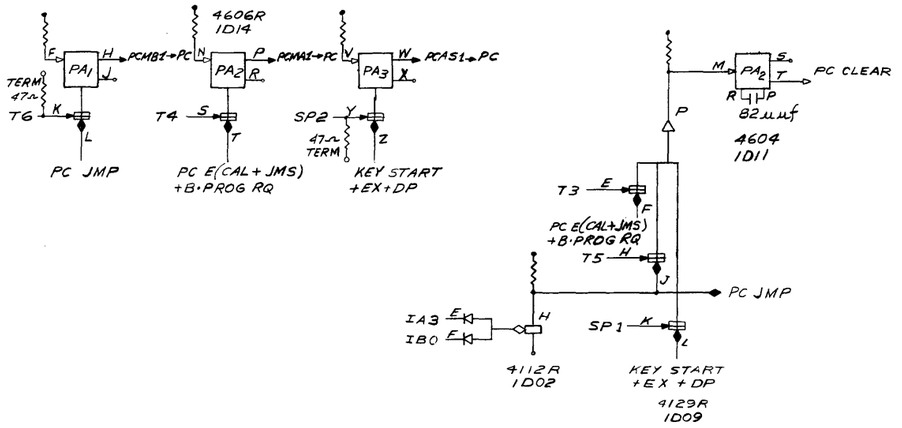


Figure 6-2 States, In-out Transfer Control





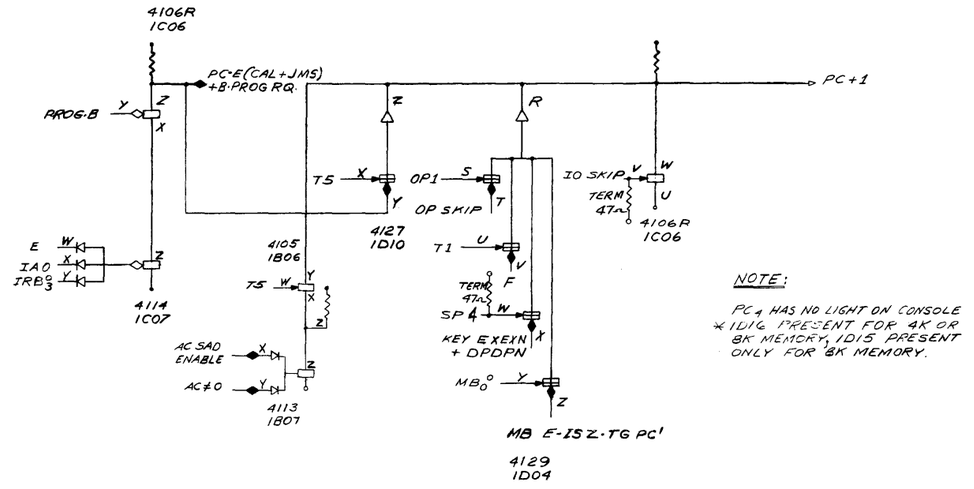


Figure 6-3 Program Control

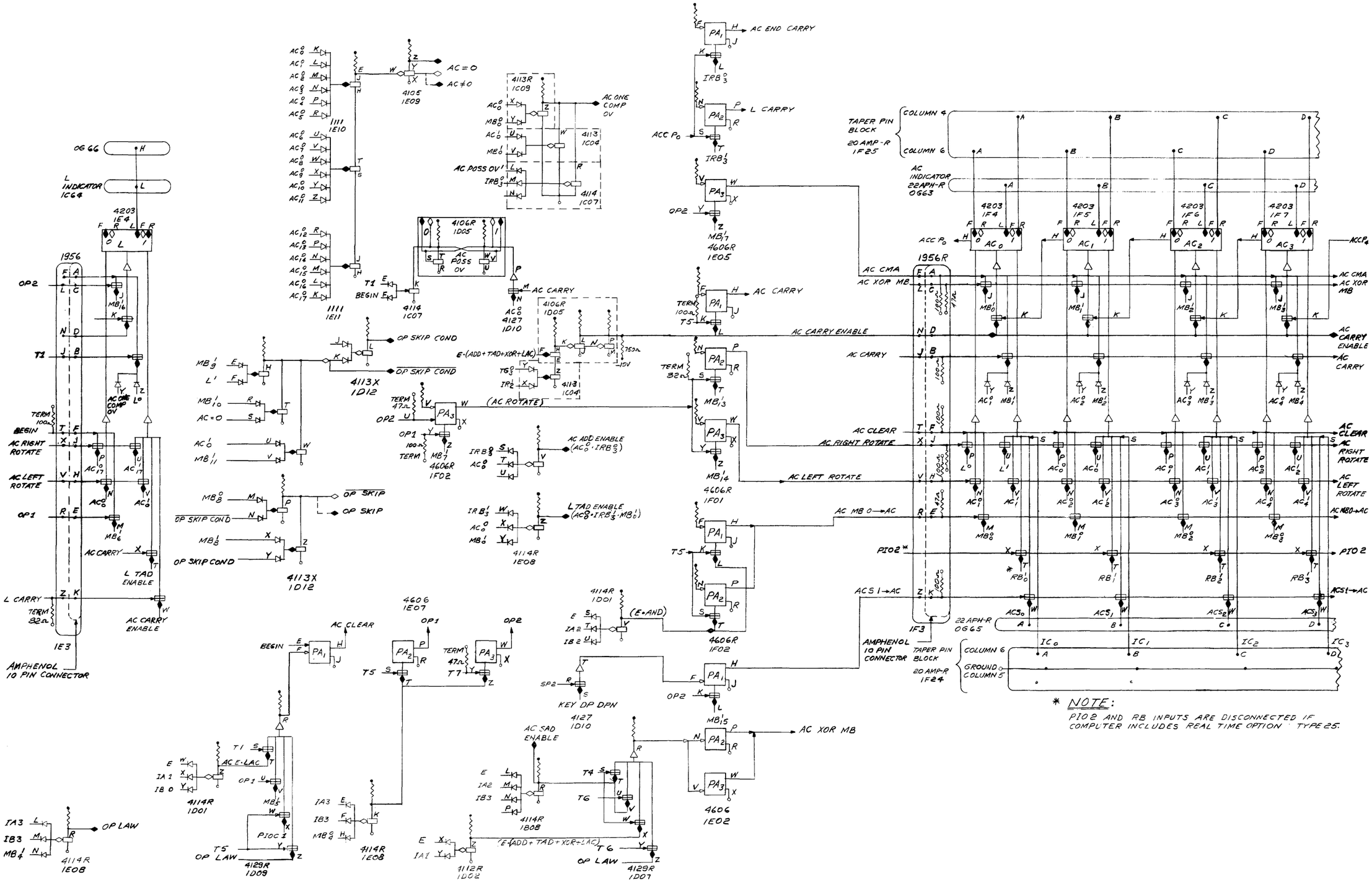
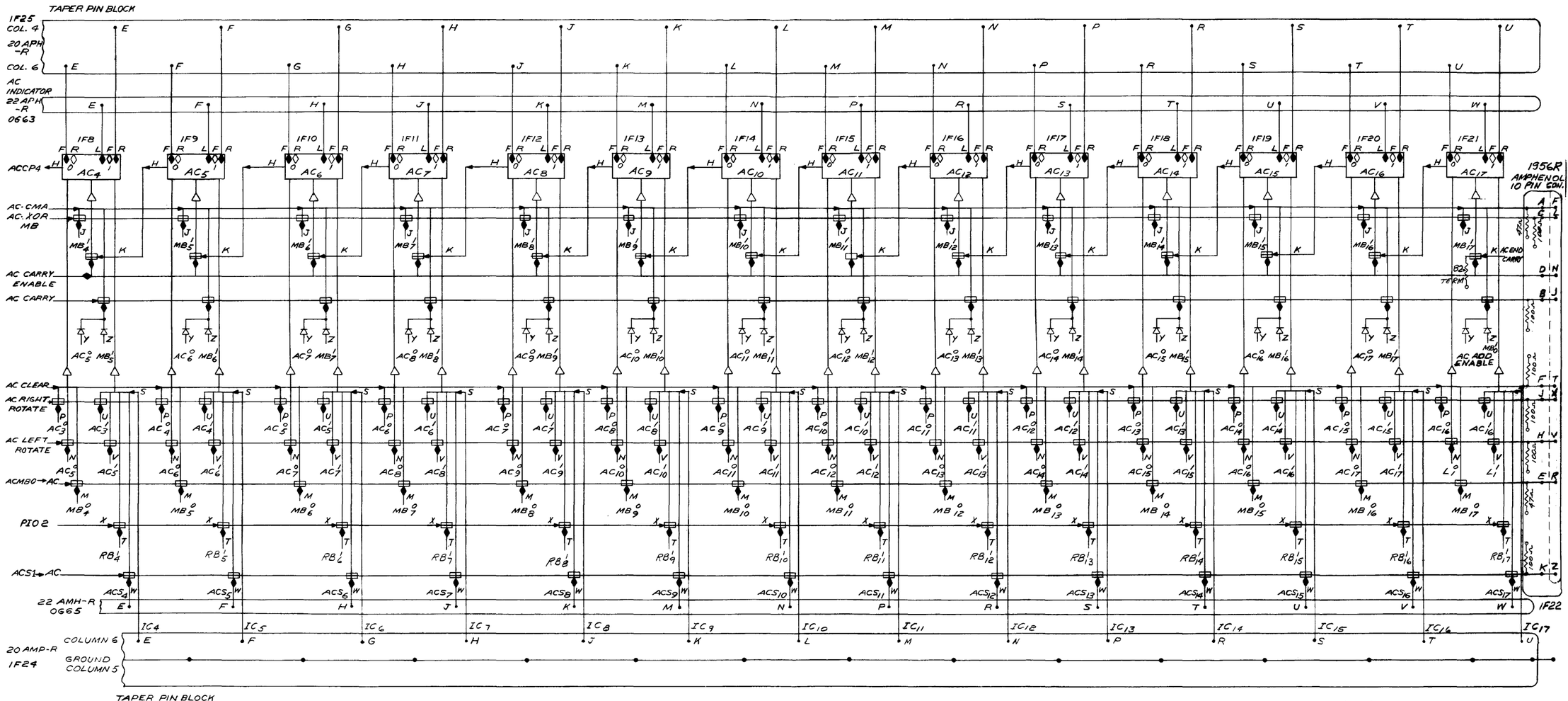


Figure 7-1 Link, Operate, Accumulator 0-3



NOTE:

1. PI02 AND RB INPUTS ARE DISCONNECTED IF COMPUTER INCLUDES REAL TIME OPTION TYPE 25.
2. ALL MODULES ARE 4203

Figure 7-2 Accumulator 4-17

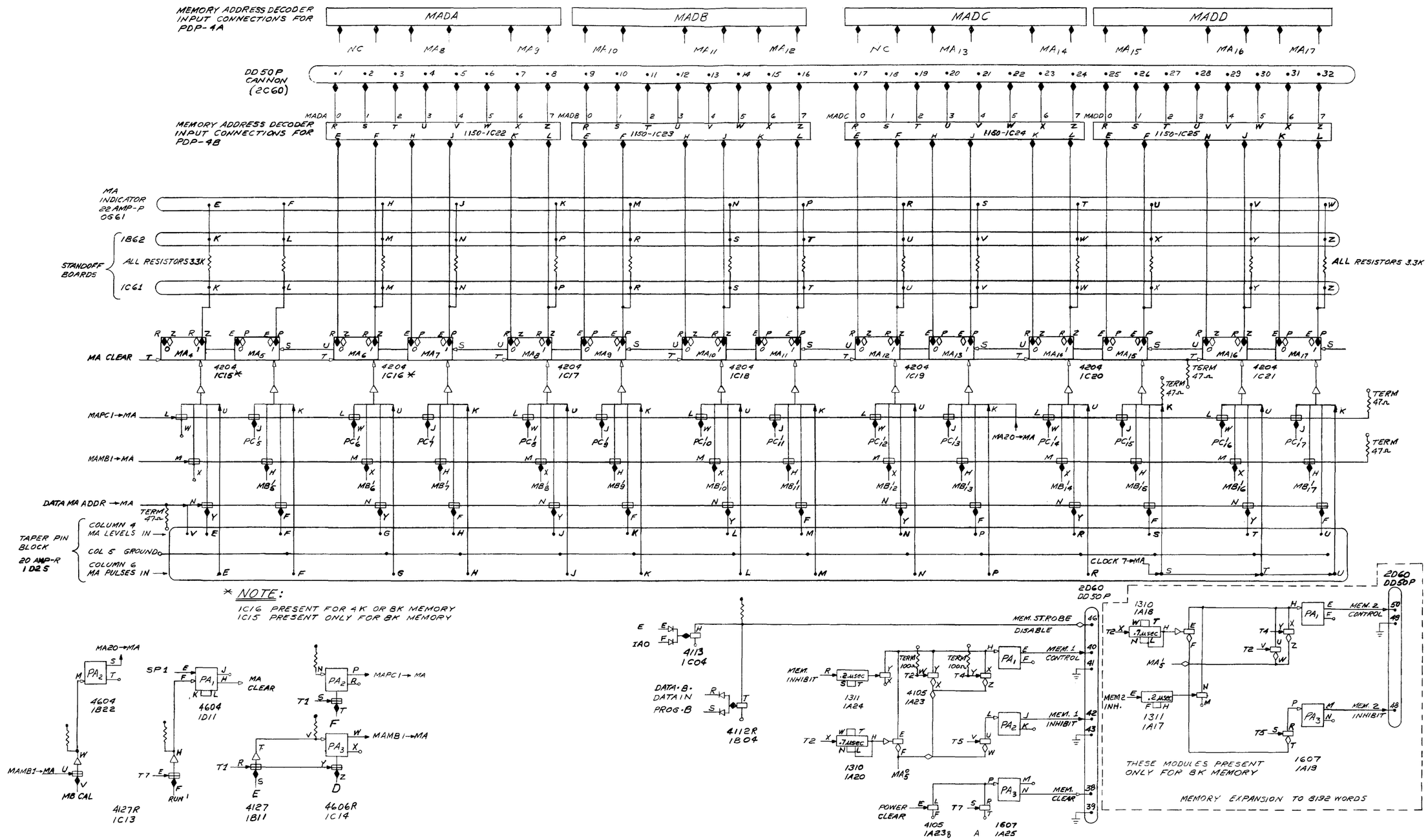


Figure 8-1 Memory Address, Memory Control

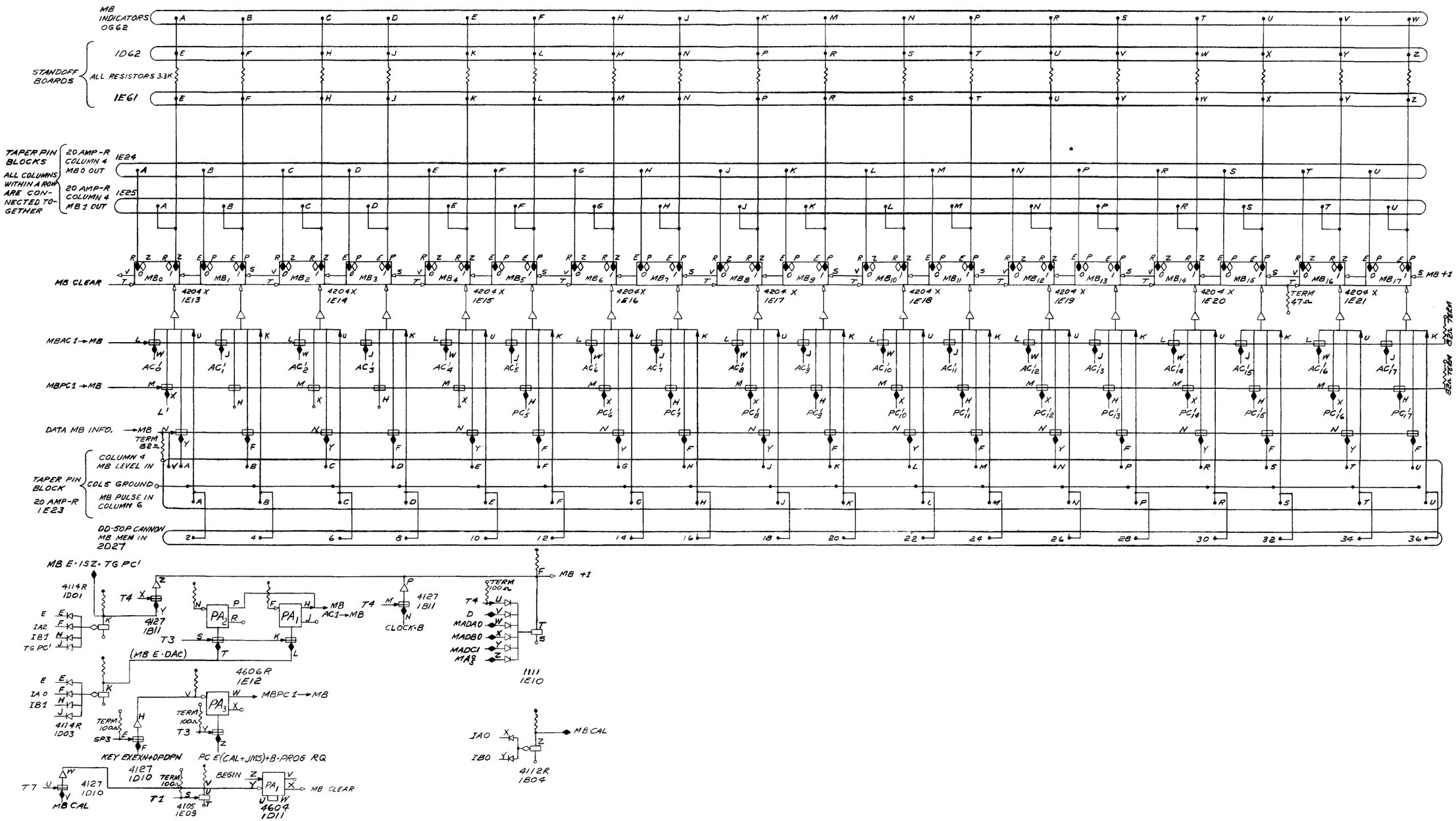


Figure 8-2 Memory Buffer, Index Logic

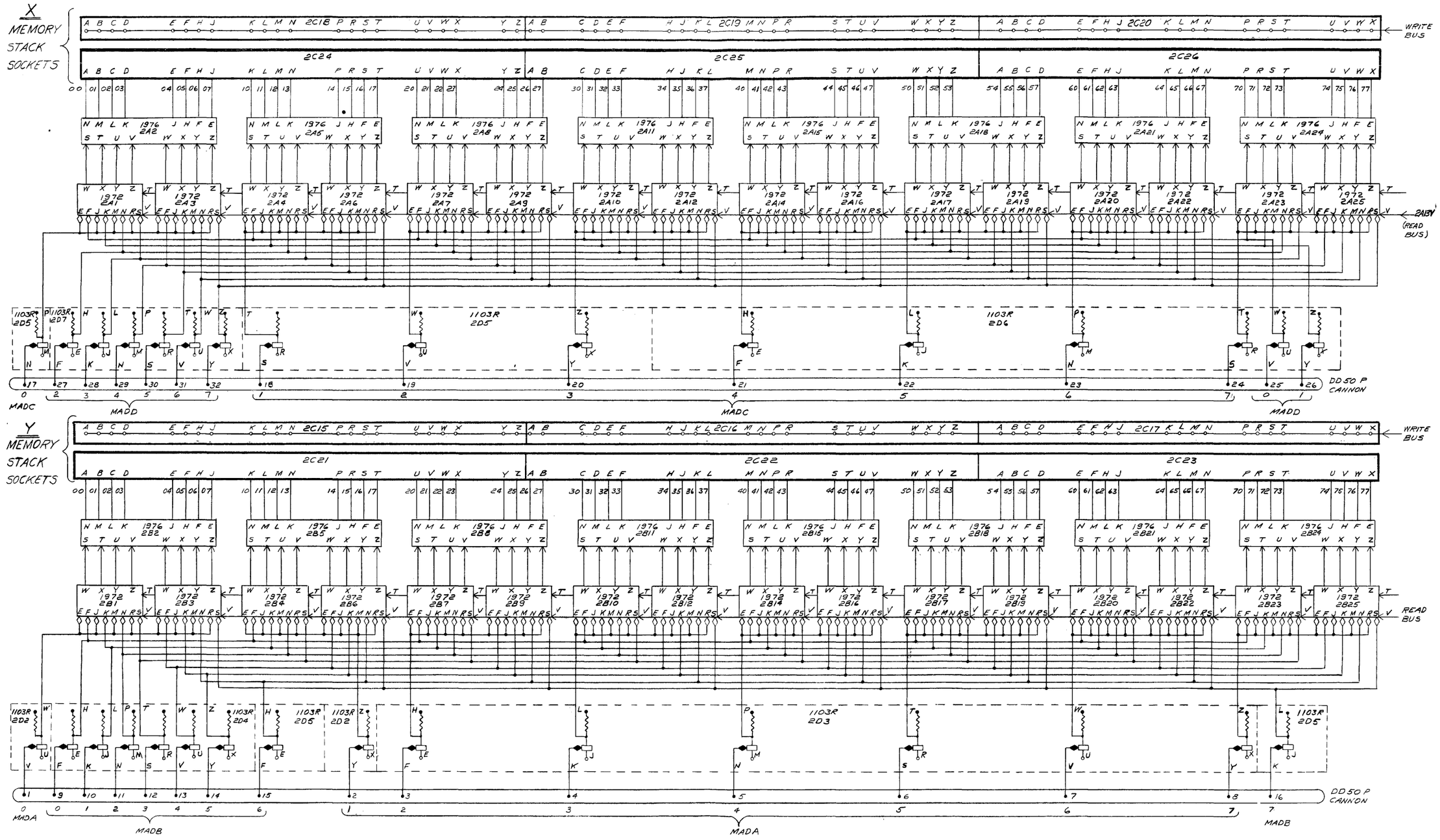
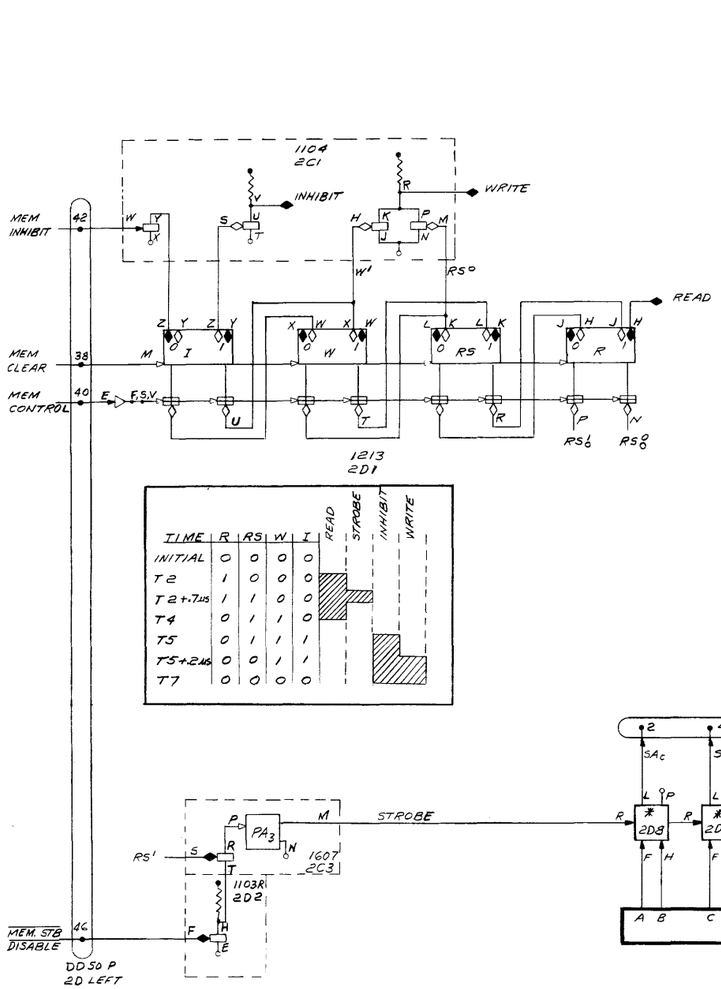
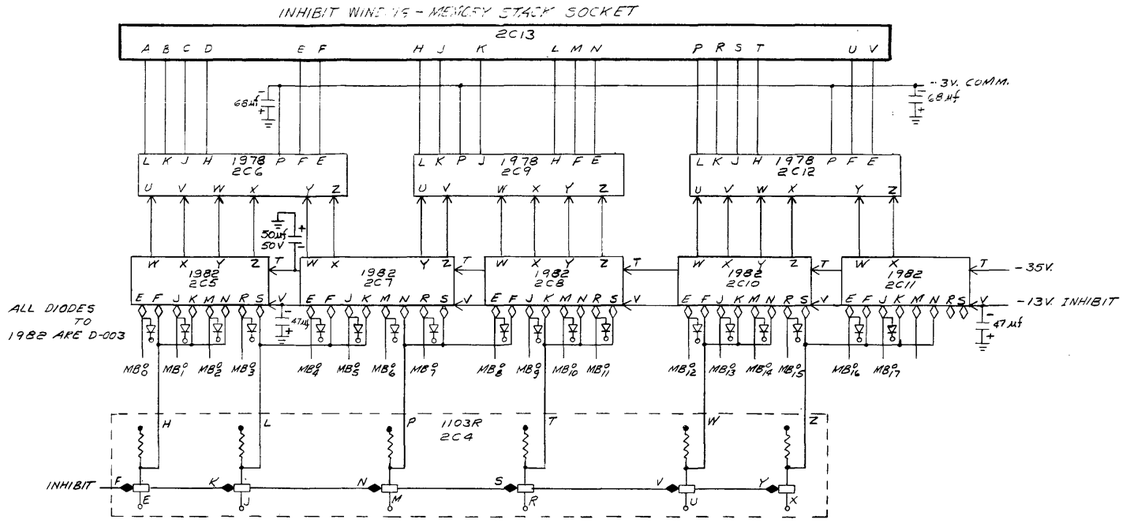


Figure 8-3 Core Register X and Y Selection

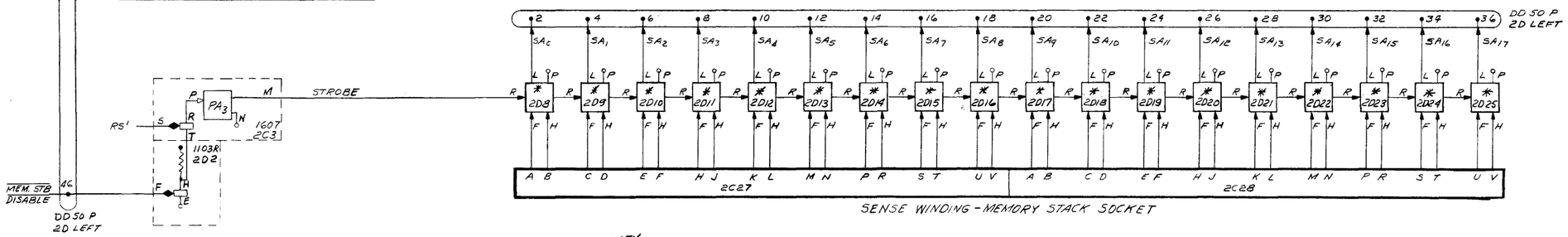


TIME	R	RS	W	I
INITIAL	0	0	0	0
T2	1	0	0	0
T2+.7µs	1	1	0	0
T4	0	1	1	0
T5	0	1	1	1
T5+2µs	0	0	1	1
T7	0	0	0	0

READ
STROBE
INHIBIT
WRITE

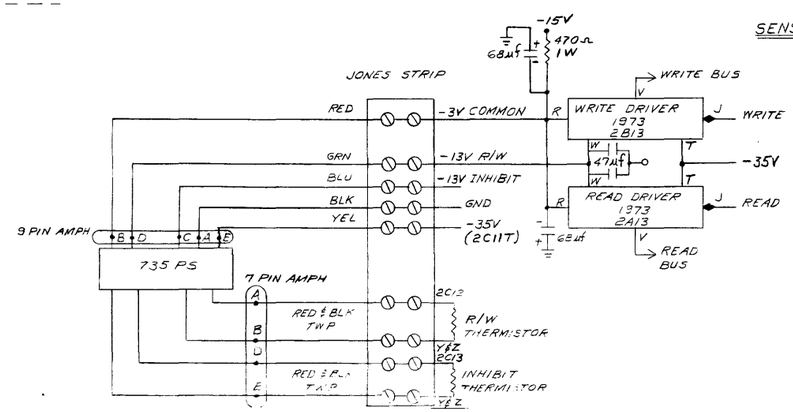


TIMING, INHIBIT



SENSE WINDING - MEMORY STACK SOCKET

SENSE AMPLIFIERS



NOTE:
* MAY BE 1538 OR 1540

Figure 8-4 Memory: Timing, Inhibit Driving, Read Sensing

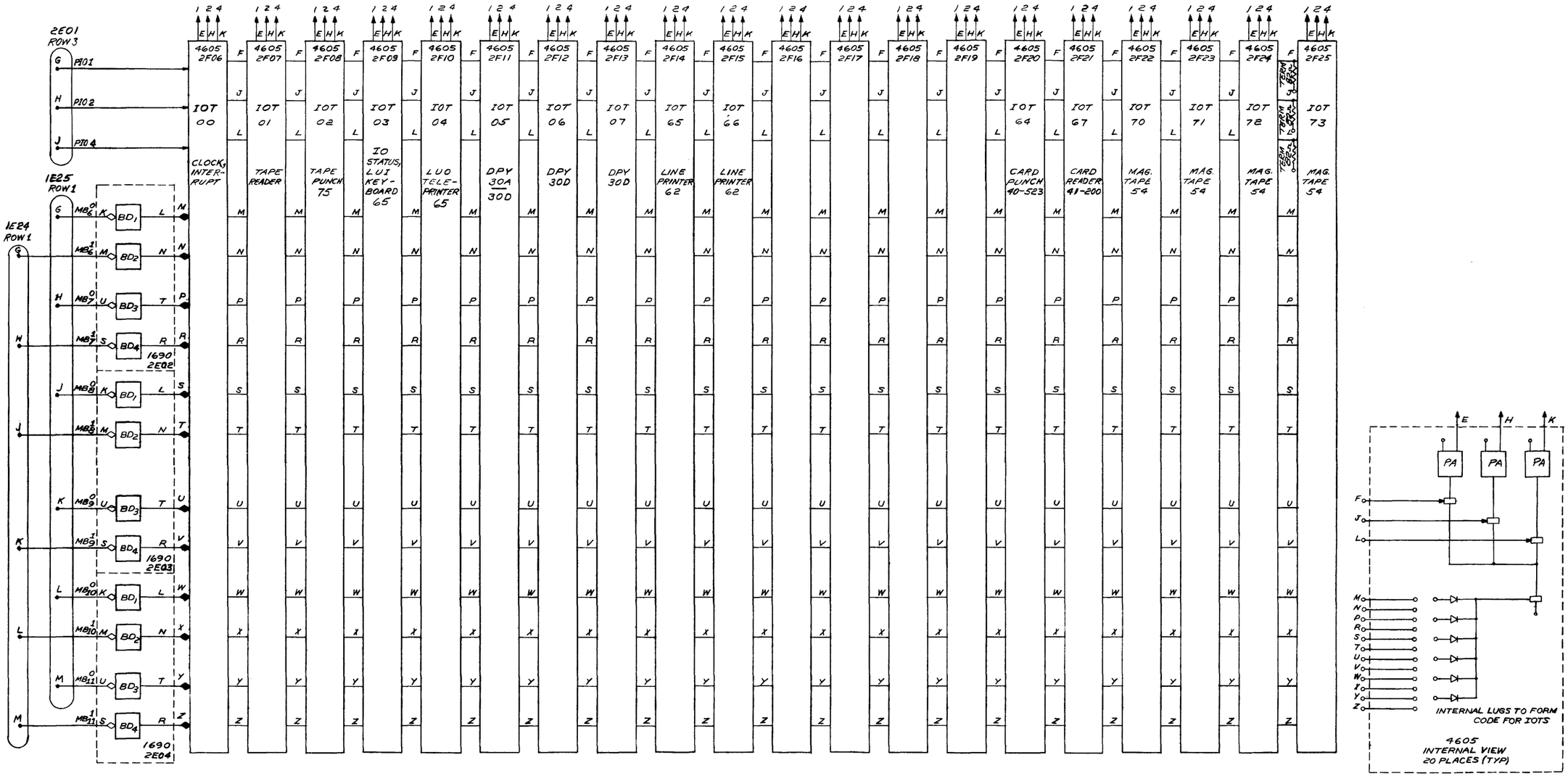


Figure 9-1 Device Selector

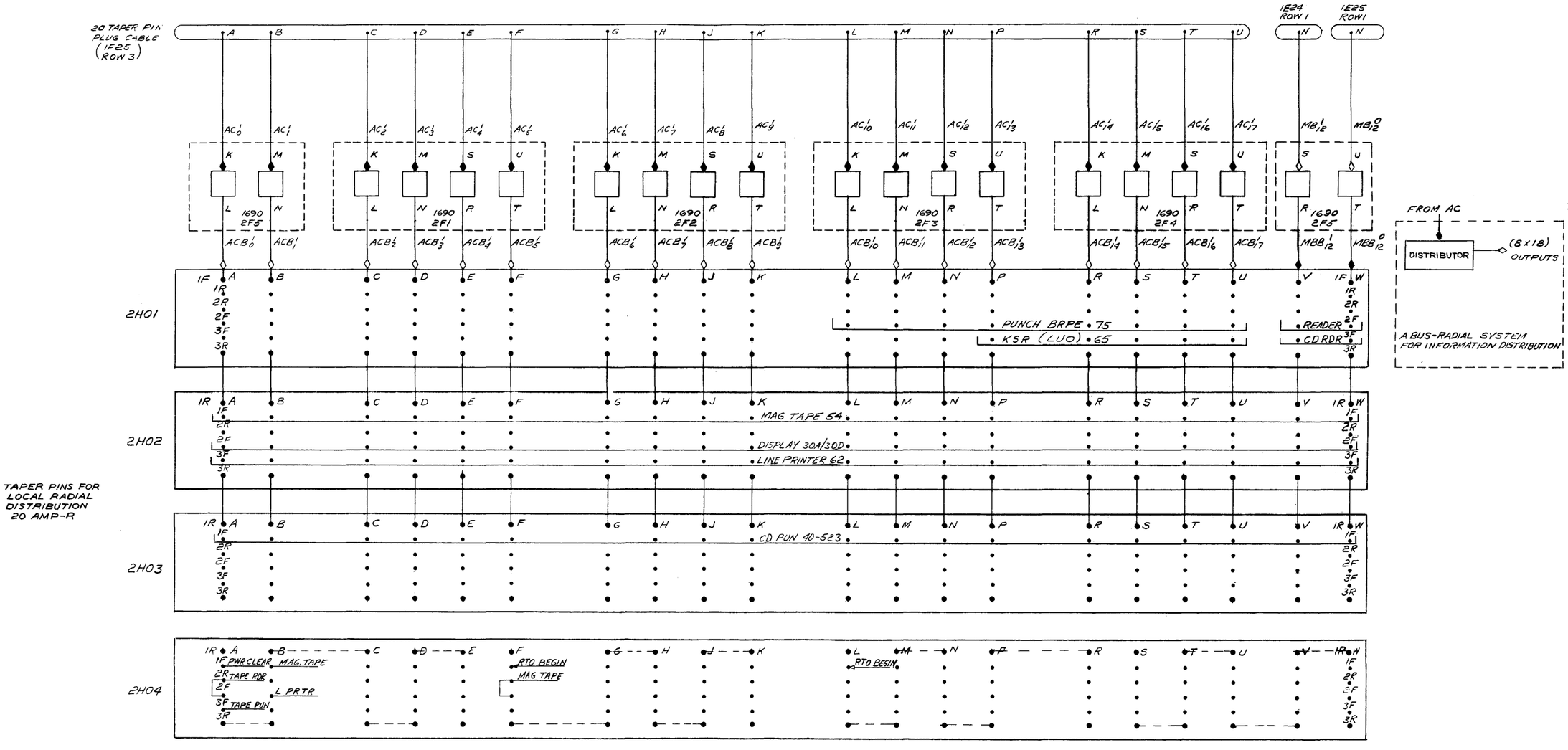


Figure 9-2 Information Distributor

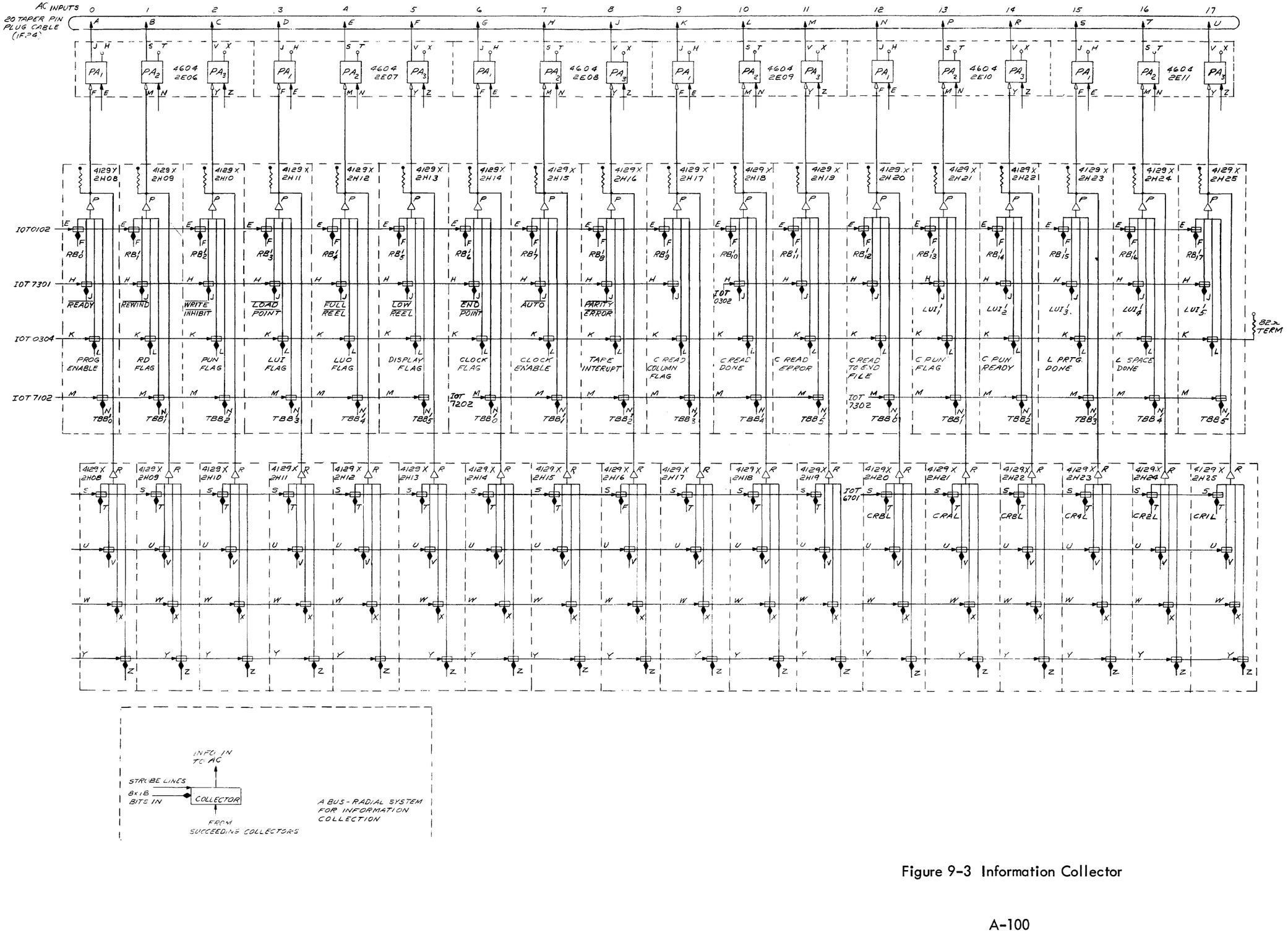


Figure 9-3 Information Collector

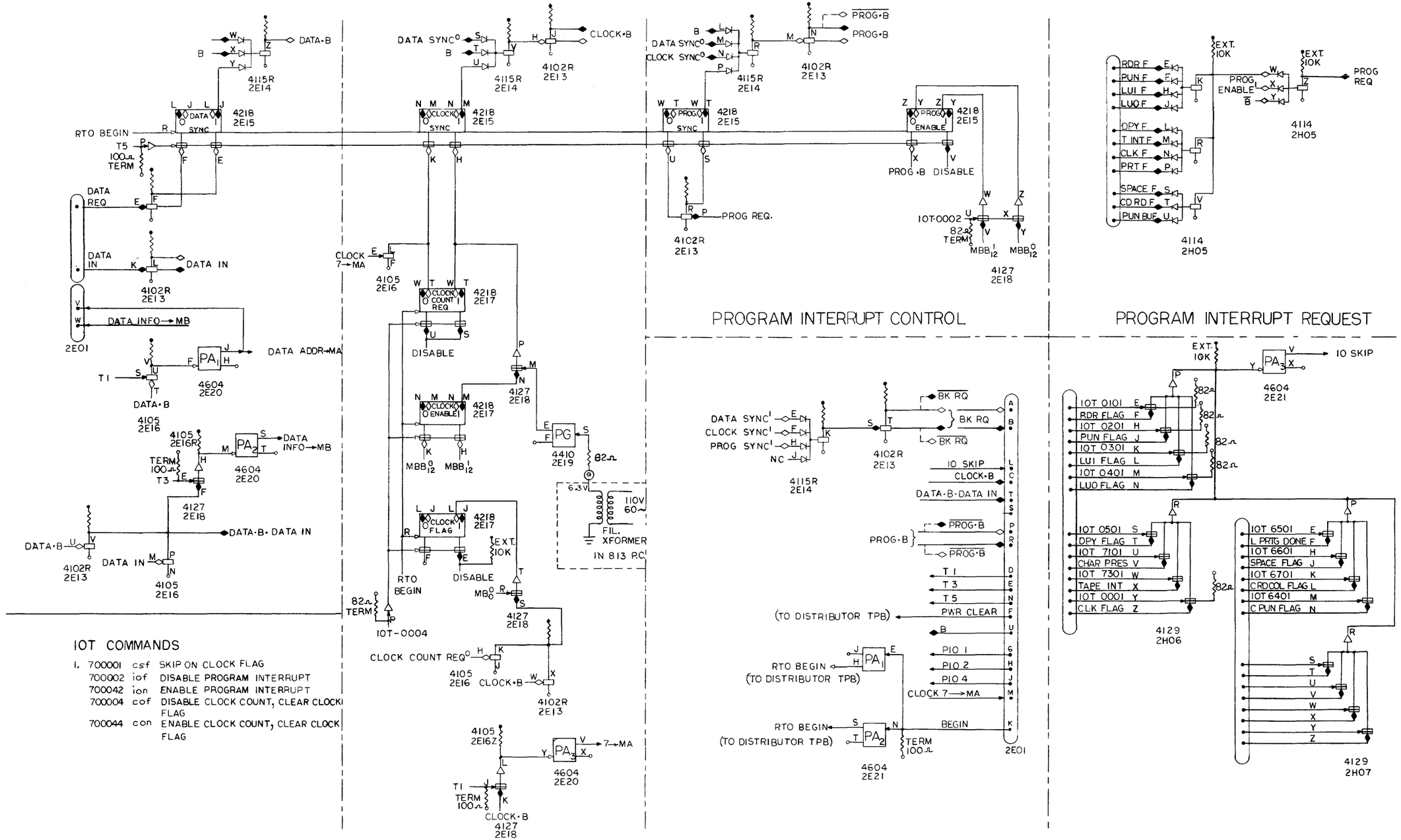
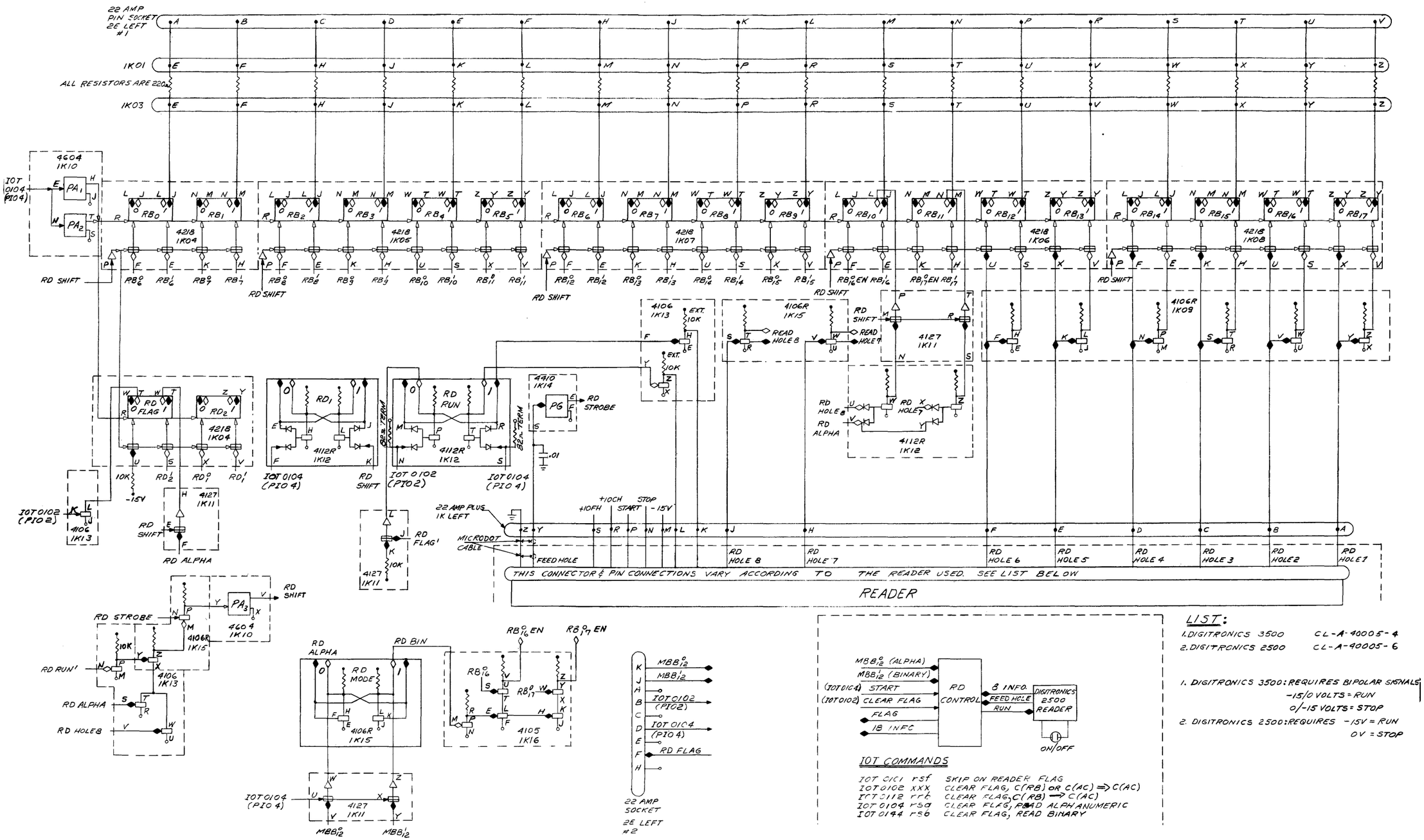


Figure 9-4 Data, Clock and Program Interrupt Logic, In-out Skip Logic



IOT COMMANDS

IOT 0101	rsf	SKIP ON READER FLAG
IOT 0102	xxx	CLEAR FLAG, C(RB) OR C(AC) ⇒ C(AC)
IOT 0112	rrc	CLEAR FLAG, C(RB) ⟶ C(AC)
IOT 0104	rsa	CLEAR FLAG, READ ALPHANUMERIC
IOT 0144	rsb	CLEAR FLAG, READ BINARY

LIST:

1. DIGITRONICS 3500 CL-A-40005-4
2. DIGITRONICS 2500 CL-A-40005-6

1. DIGITRONICS 3500: REQUIRES BIPOLAR SIGNALS
   -15/0 VOLTS = RUN
   0/-15 VOLTS = STOP
2. DIGITRONICS 2500: REQUIRES -15V = RUN
   0V = STOP

Figure 9-5 Reader Control

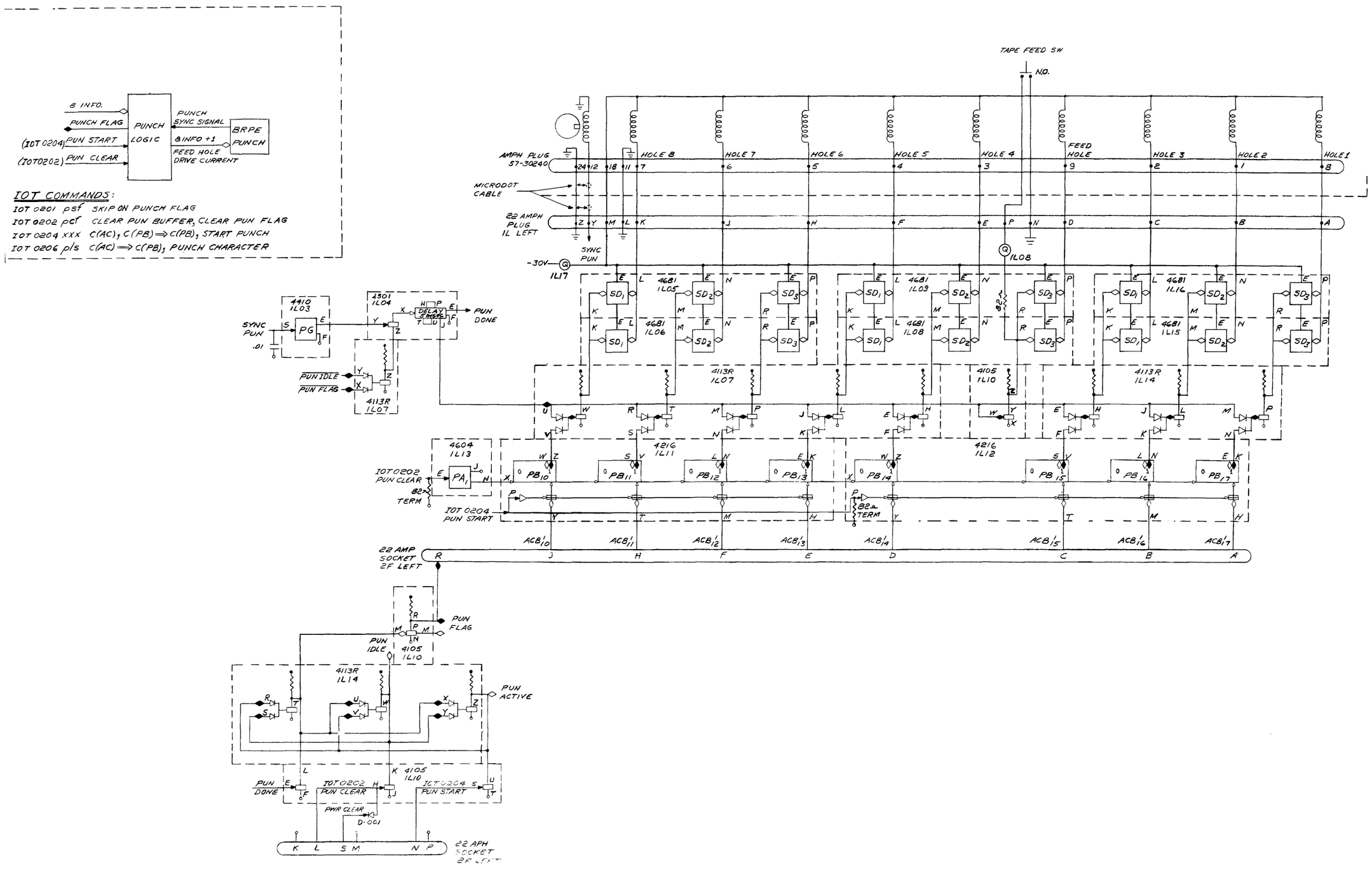
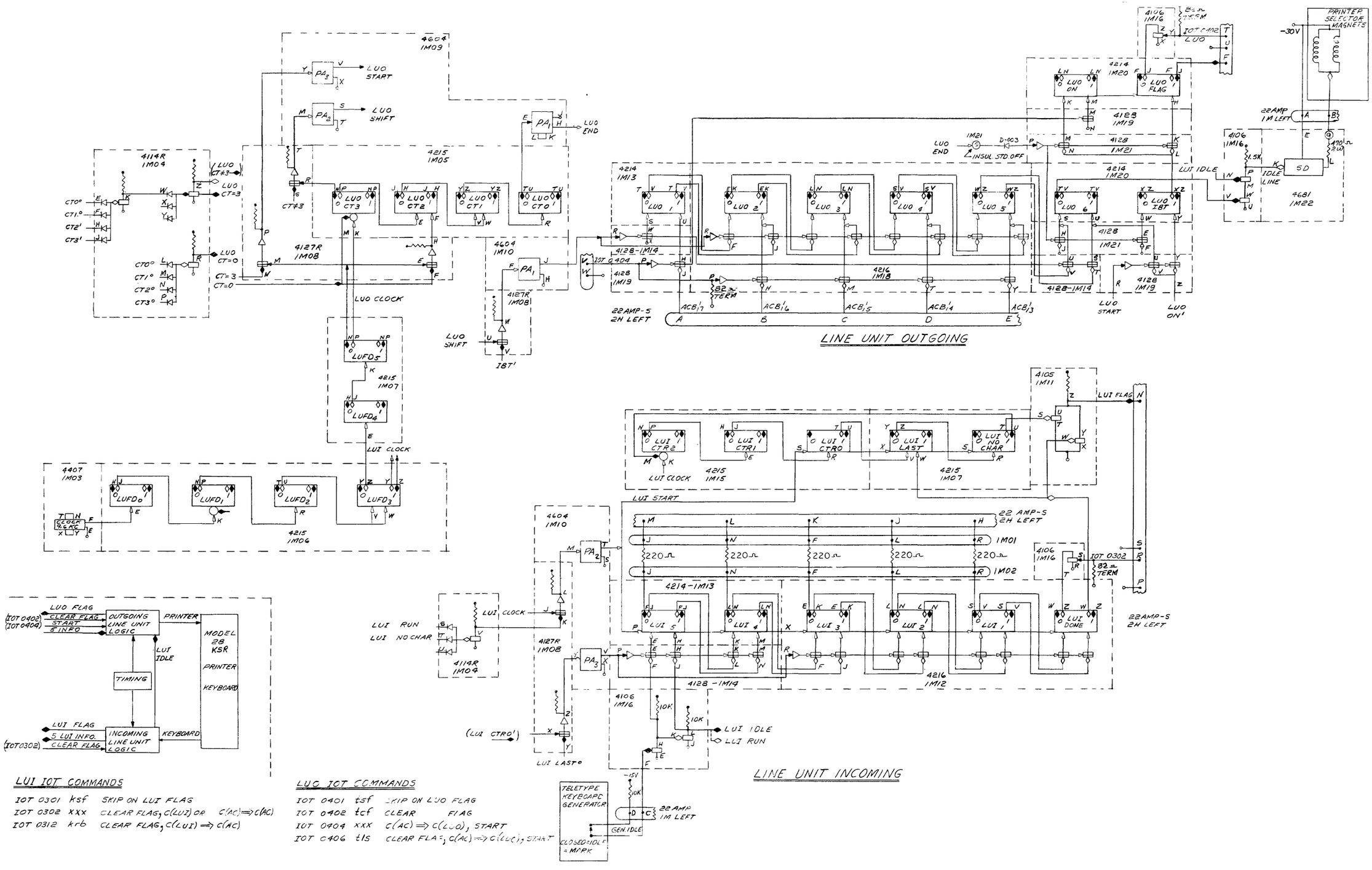


Figure 9-6 Punch Control Type 75



LUI IOT COMMANDS

IOT 0301	ksf	SKIP ON LUI FLAG
IOT 0302	xxx	CLEAR FLAG, C(LUI) OR C(AC) ⟹ C(AC)
IOT 0312	krb	CLEAR FLAG, C(LUI) ⟹ C(AC)

LUO IOT COMMANDS

IOT 0401	tsf	SKIP ON LUO FLAG
IOT 0402	tcf	CLEAR FLAG
IOT 0404	xxx	C(AC) ⟹ C(LUO), START
IOT 0406	tls	CLEAR FLAG, C(AC) ⟹ C(LUO), START

Figure 9-7 Keyboard/Printer control Types 65

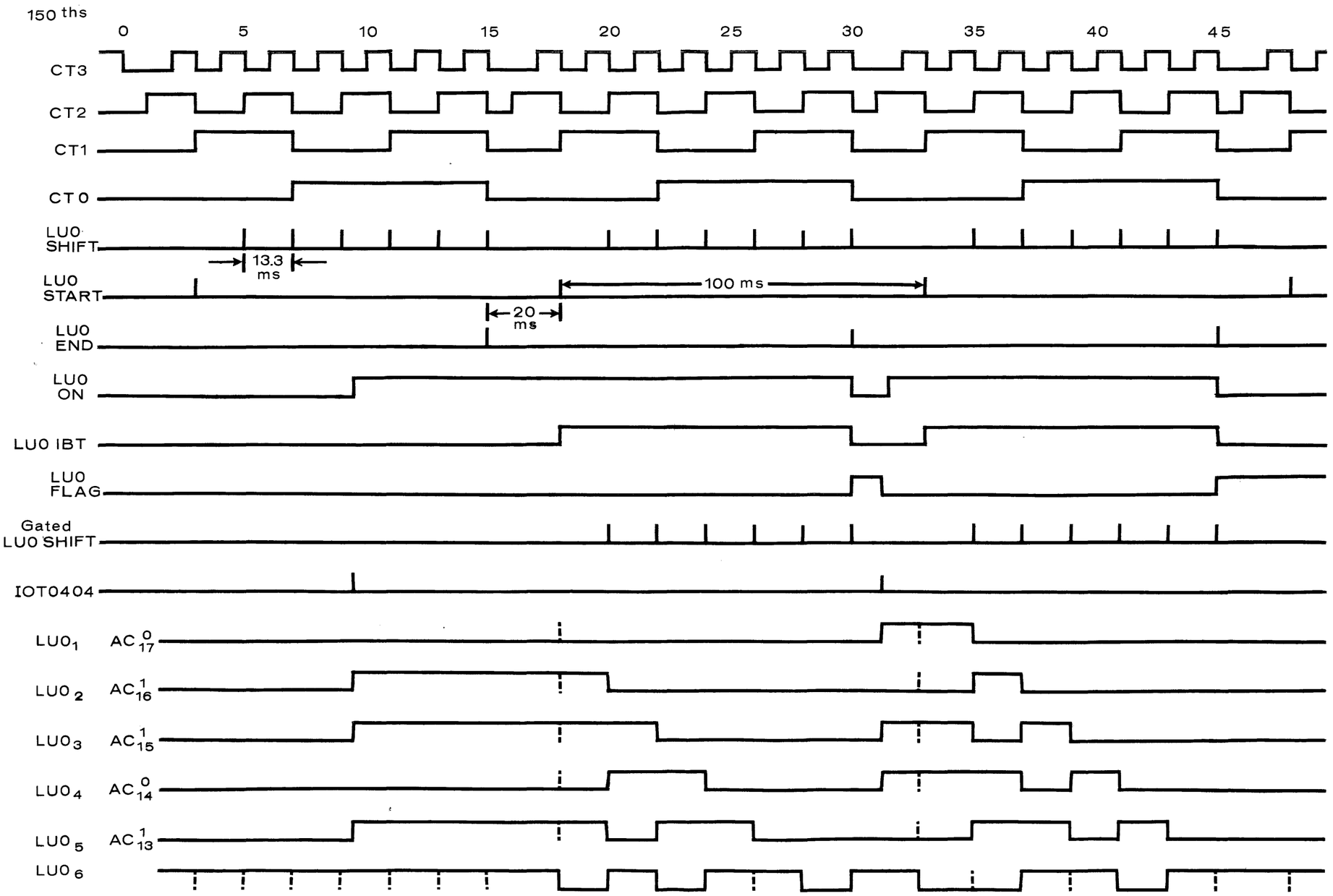


Figure 9-8 Timing Diagram: Outgoing Line Unit

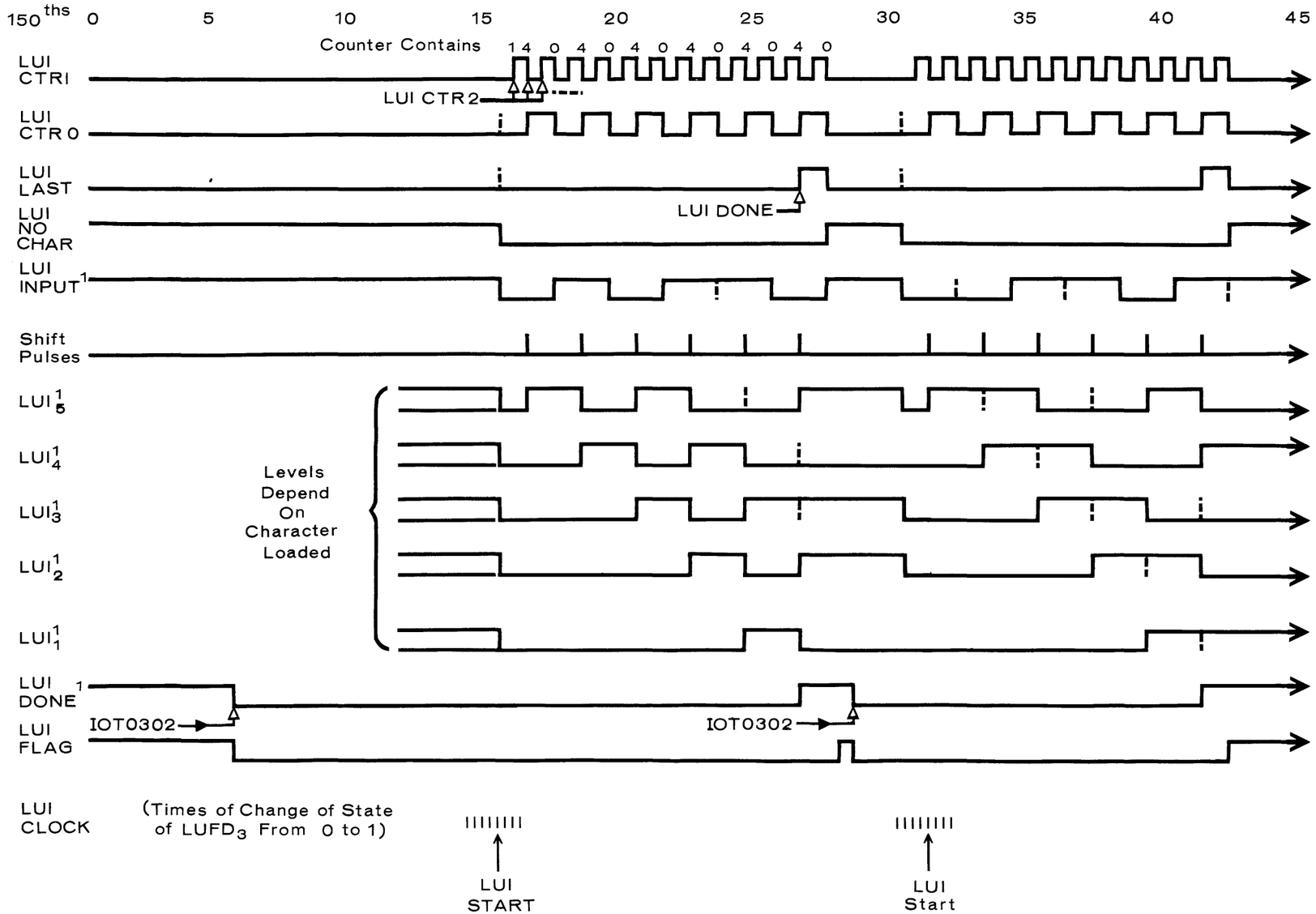
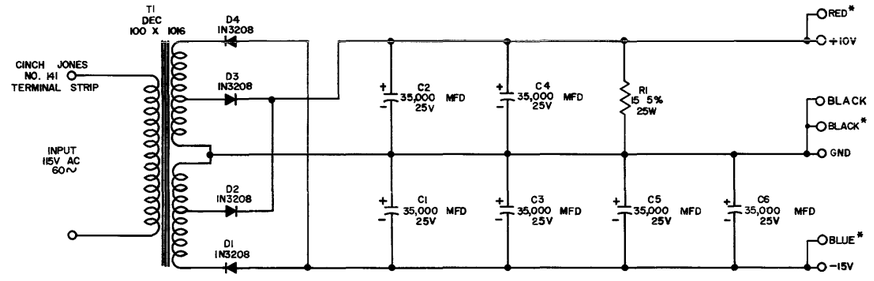


Figure 9-9 Timing Diagram: Incoming Line Unit



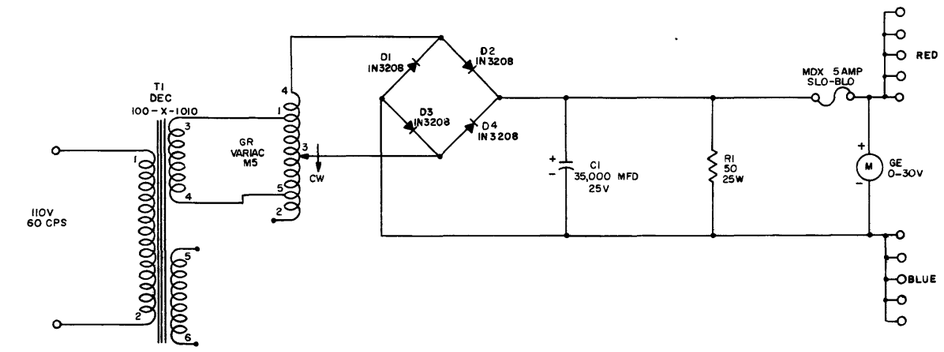
* HEYMAN MFG. CO.
TAB TERMINALS

NOTE
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:

BOTH SIDES LOADED	+10V	.0 TO 7.0 AMPS	
	-15V	1.0 TO 8.0 AMPS	
ONE SIDE LOADED	+10V	.0 TO 7.5 AMPS	
	-15V	1.0 TO 8.5 AMPS	

SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE FOLLOWING EQUATION $5I_{10} + 6I_{15} \leq 53$

POWER SUPPLY 728

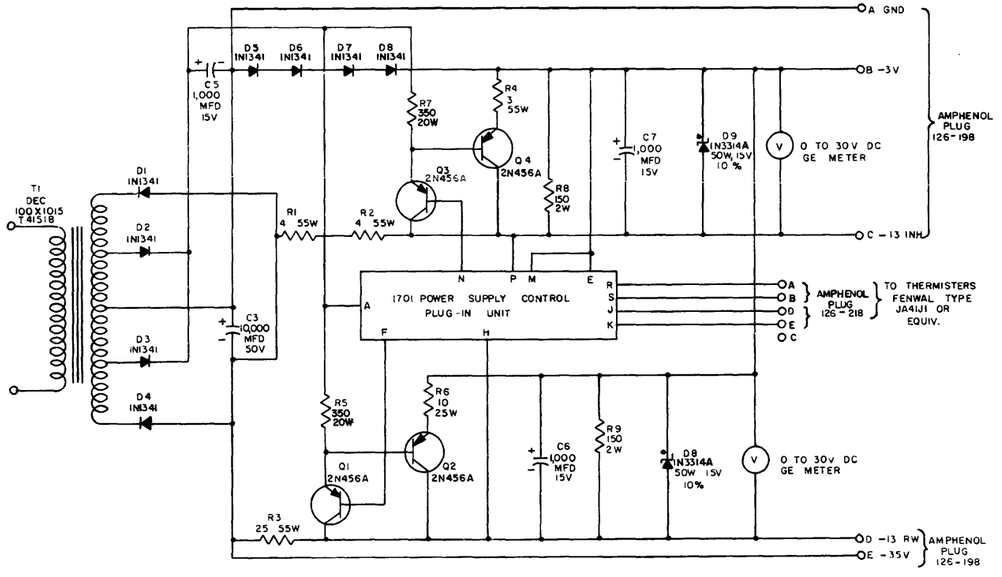


NOTE:
INPUT IS CONNECTED THROUGH JONES NO. 141 TERMINAL STRIP
OUTPUT IS CONNECTED THROUGH HEYMAN TAB TERMINALS

VARIABLE POWER SUPPLY 734

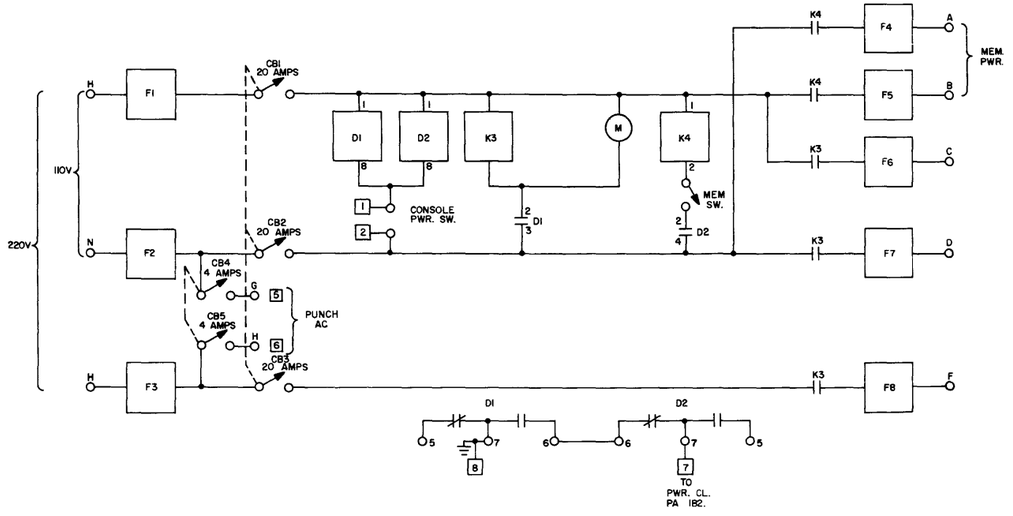
POWER SUPPLY 728

VARIABLE POWER SUPPLY 734



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 10 %

POWER SUPPLY 735



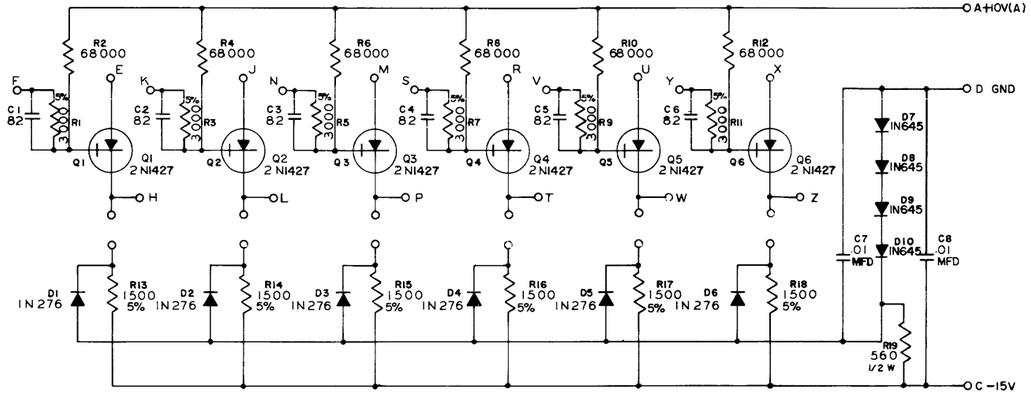
F1-F8 ARE SPRAGUE FILTROL # 3
D1 IS AN AGASTAT TYPE 2122-A-5
D2 IS AN AGASTAT TYPE 2112-A-5
K3 AND K4 ARE ARROW HART # 34321-U, 110V 60 ~
S1 IS A CUTLER HAMMER SPST
CB1-CB3 ARE HEINEMANN AM333 CURVE 4
CB4 AND CB5 ARE HEINEMANN XAM33 CURVE 4
M1 IS A HAYDON ED 71-001

POWER CONTROL 813

POWER SUPPLY 735

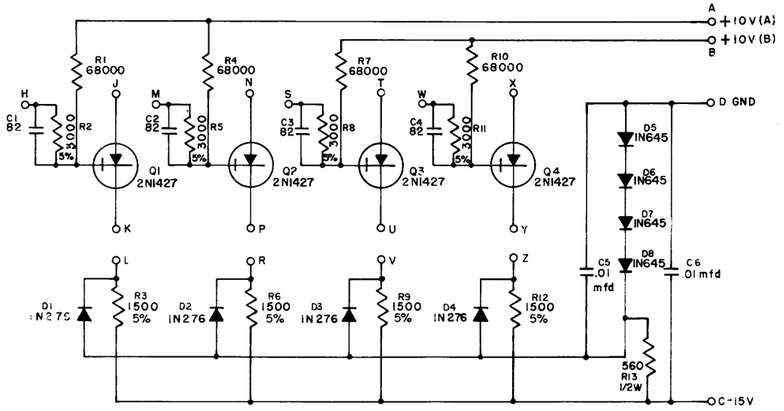
POWER CONTROL 813

A-130



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

INVERTER 1103

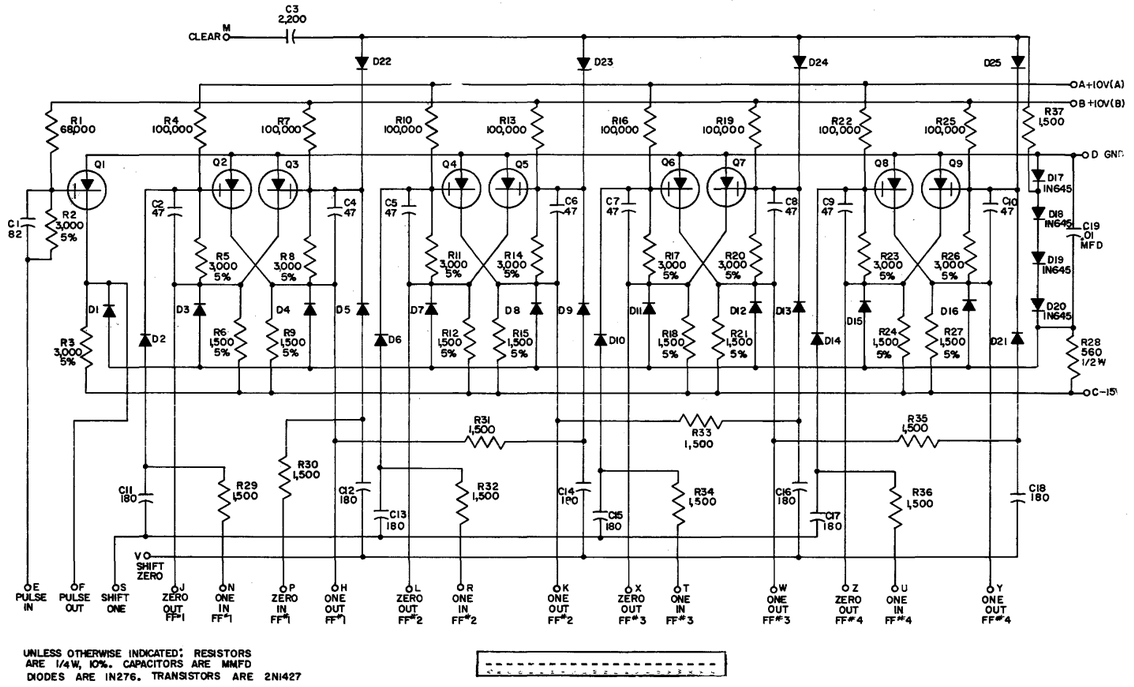


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

INVERTER 1104

INVERTER 1103

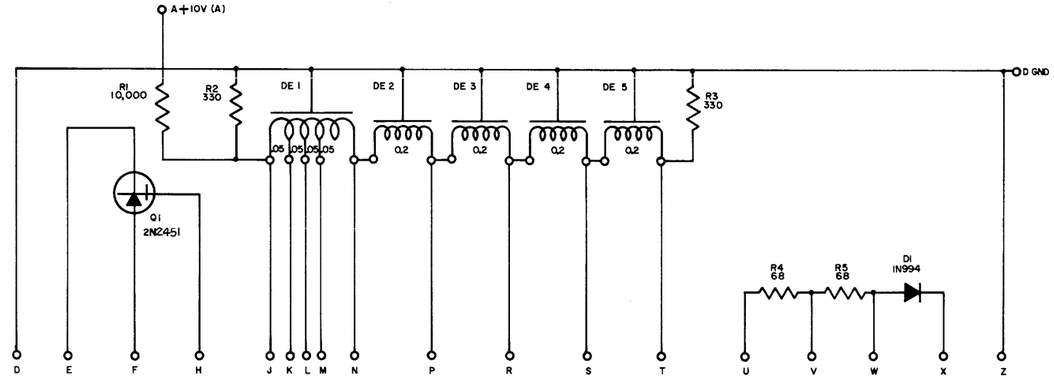
INVERTER 1104



UNLESS OTHERWISE INDICATED: RESISTORS ARE 1/4 W, 10%. CAPACITORS ARE MMFD
DIODES ARE IN276. TRANSISTORS ARE 2N1427

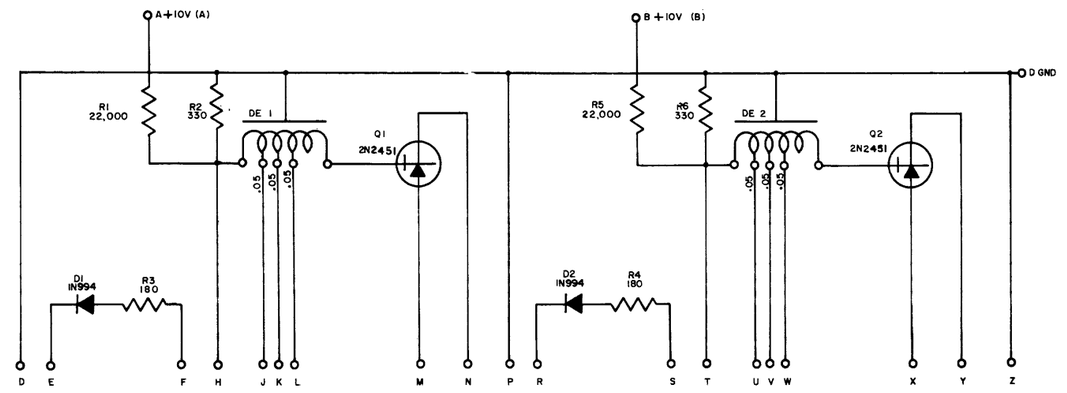
FLIP-FLOP 1213

FLIP-FLOP 1213



UNLESS OTHERWISE INDICATED: RESISTORS ARE 1/2W, 10%
DE 1= 0.2 μ SEC. DELAY LINE 330 OHMS. TAPPED AT 0.05 μ SEC. INTERVAL. DEC # 330-25E-6
DE 2-DE 5 = 0.2 μ SEC. DELAY LINE. DEC # 330-25E-3

DELAY 1310

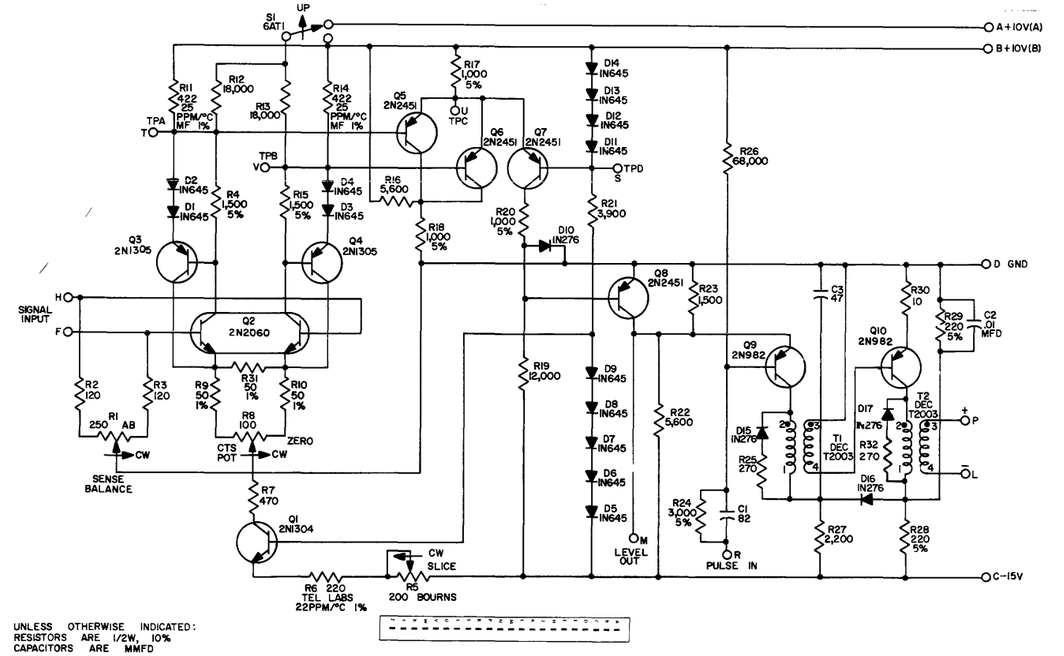


UNLESS OTHERWISE INDICATED: RESISTORS ARE 1/2W, 10%
DE 1 & DE 2 ARE 0.2 μ SEC. DELAY LINE, 330 OHMS TAPPED AT 0.05 μ SEC. DEC # 330-25E-6

DELAY 1311

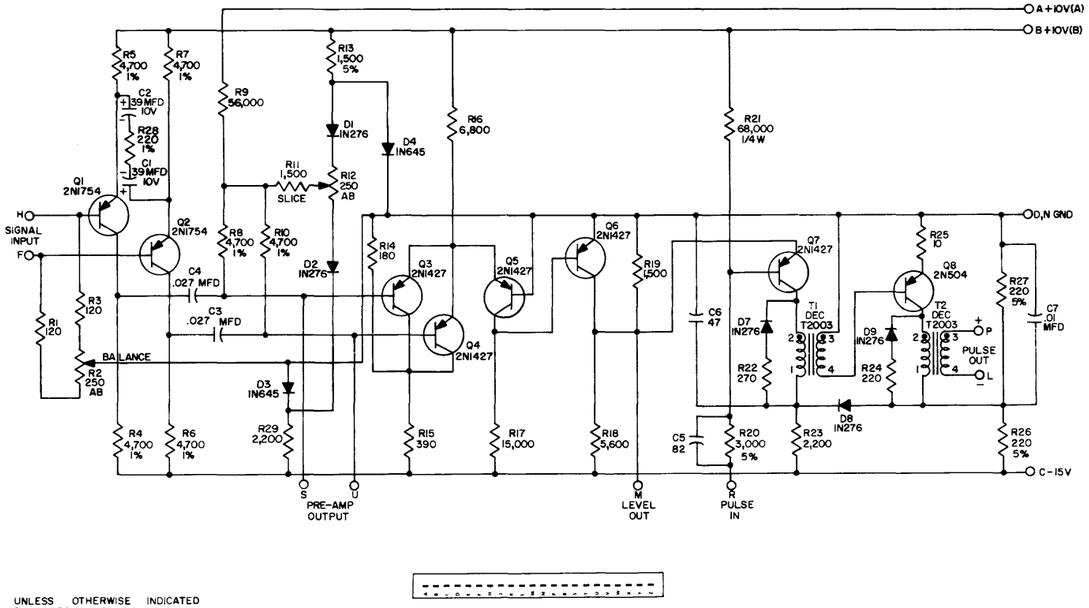
DELAY 1310

DELAY 1311



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD

SENSE AMPLIFIER 1538

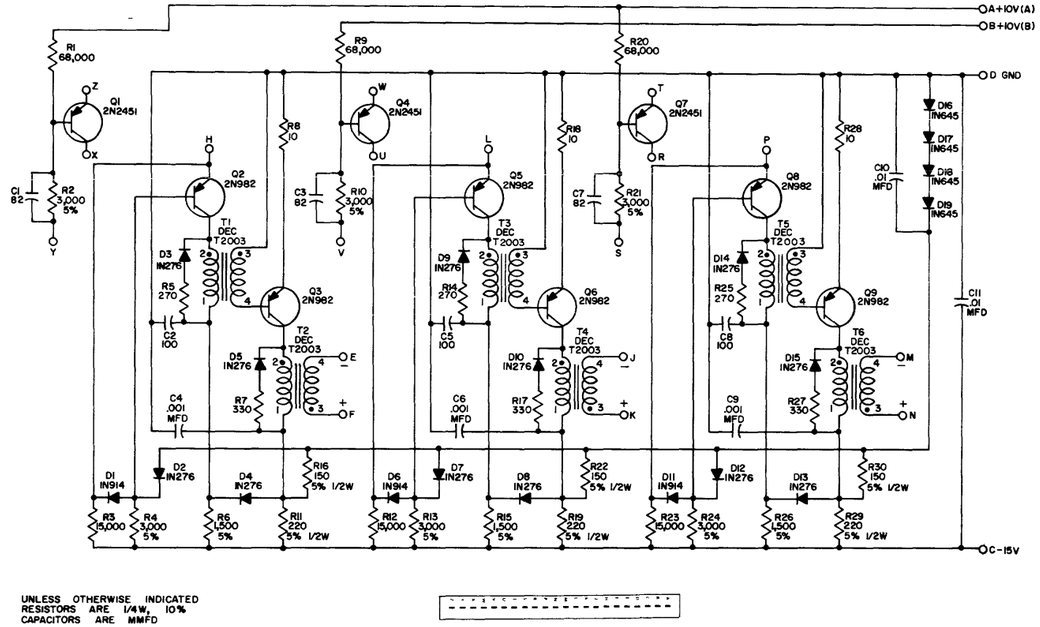


UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD.

SENSE AMPLIFIER 1540

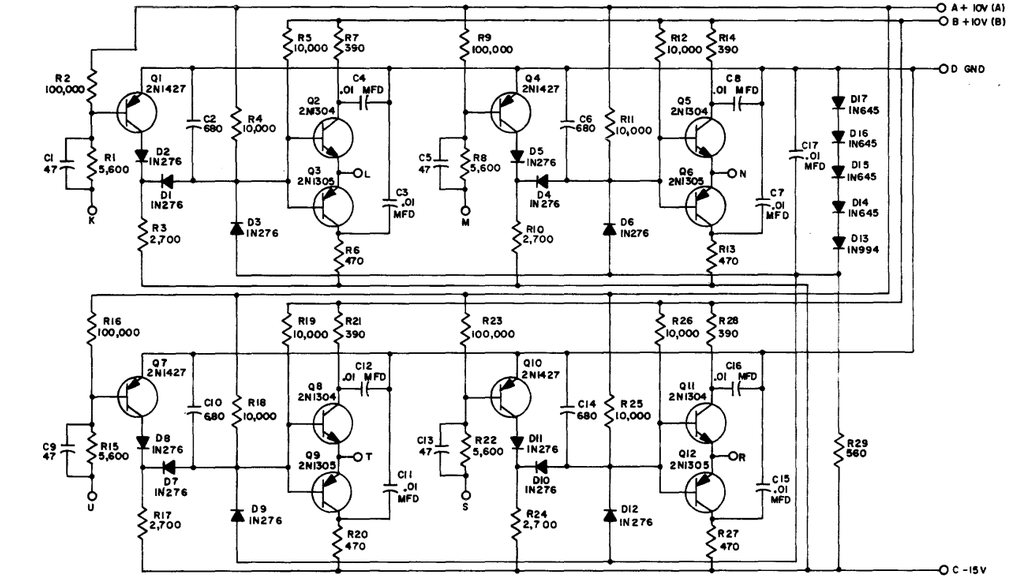
SENSE AMPLIFIER 1538

SENSE AMPLIFIER 1540



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD

PLUSE AMPLIFIER 1607

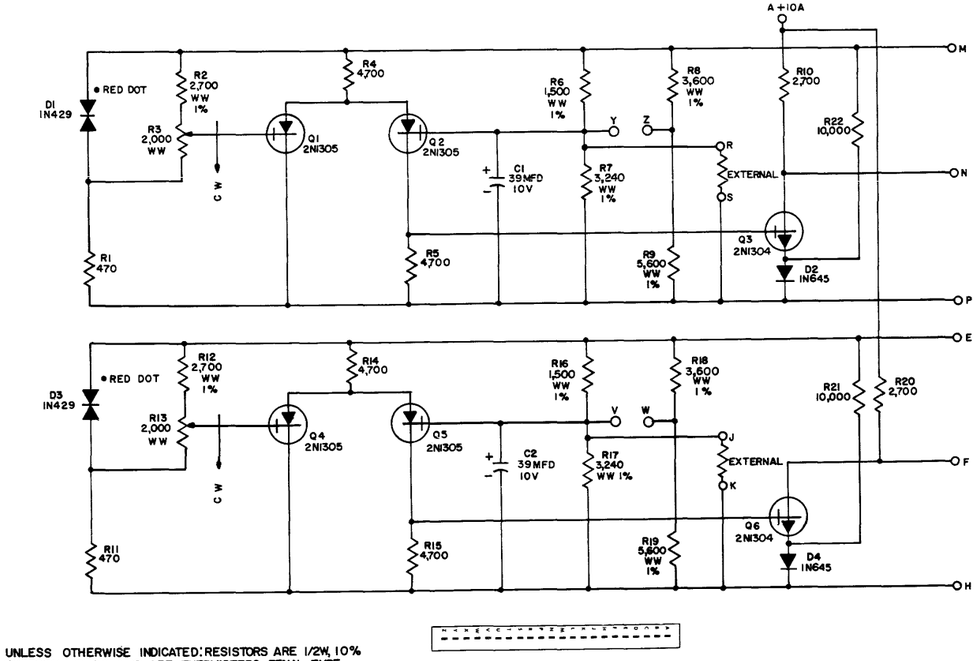


UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2 W, 10%
CAPACITORS ARE MMFD

BUS DRIVER 1690

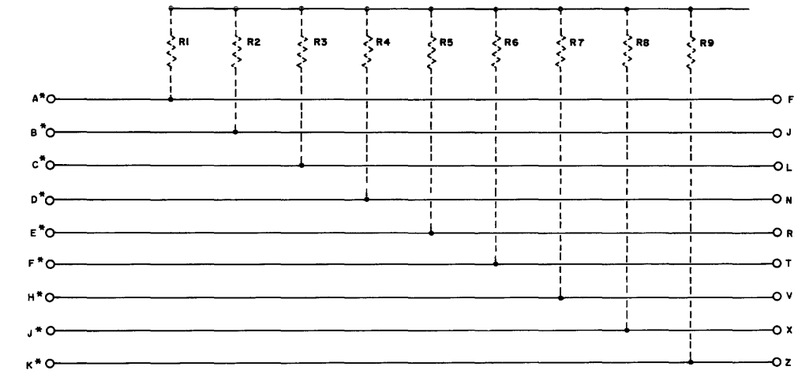
PULSE AMPLIFIER 1607

BUS DRIVER 1690



UNLESS OTHERWISE INDICATED: RESISTORS ARE 1/2W, 10%
EXTERNAL RESISTORS ARE THERMISTERS FENAL TYPE JA41J1 OR EQUIV. 10K @ 25°C. 4.4% /°C

POWER SUPPLY CONTROL 1701



* INDICATES BACK PANEL PLUG
10 PIN AMPHENOL 133-010-21

PLUG ADAPTER 1956

POWER SUPPLY CONTROL 1701

PLUG ADAPTER 1956

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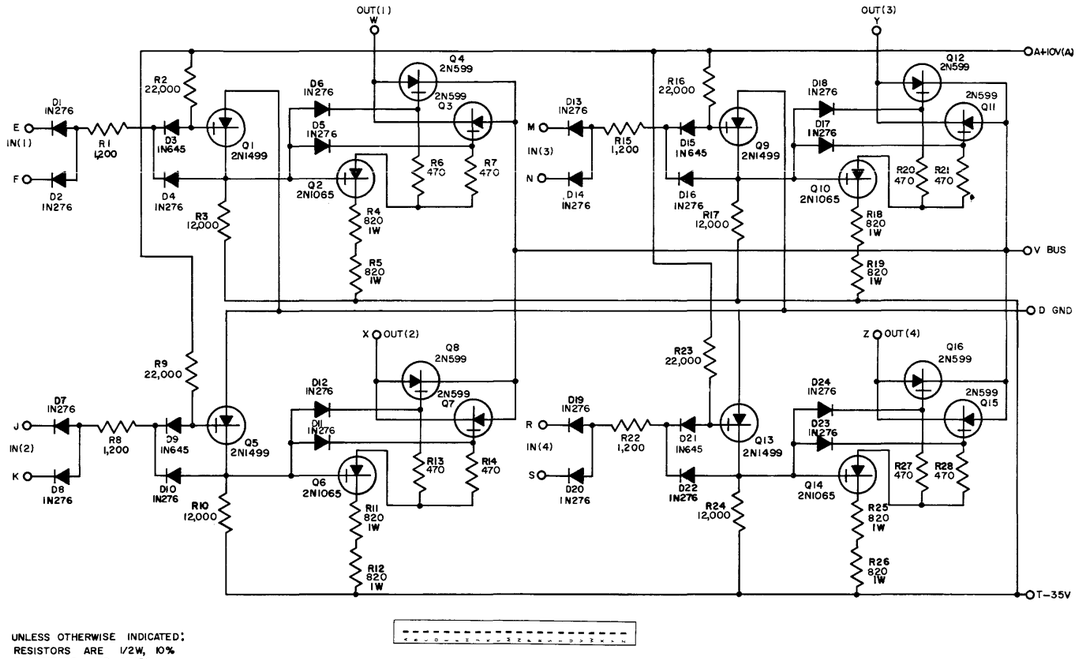
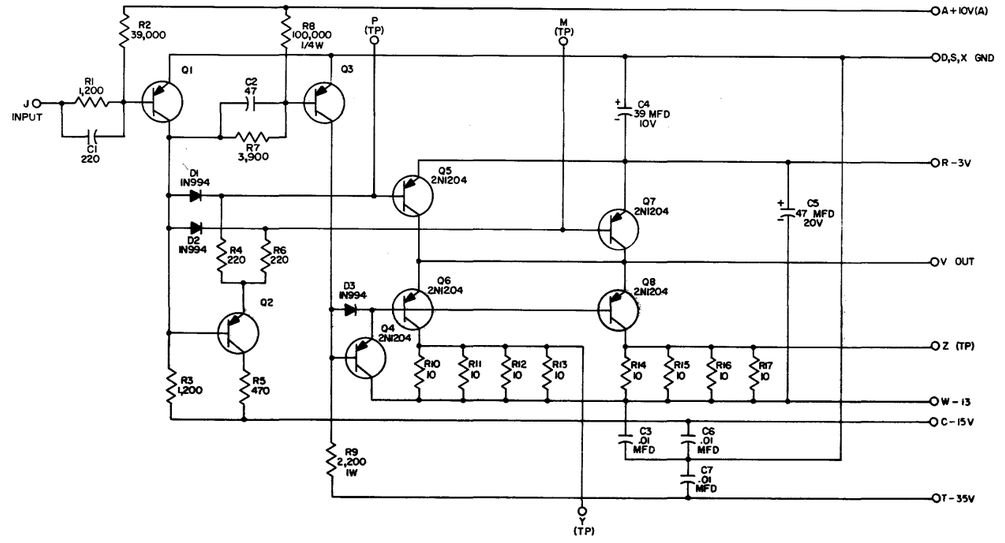


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD

READ/WRITE SWITCH 1972

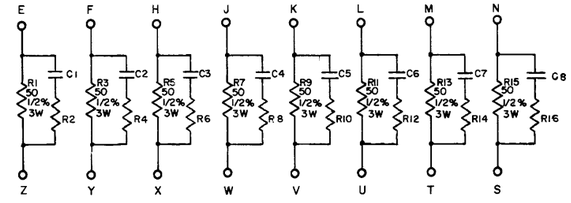


UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE 2N982 SELECTED FOR
IEBO ≤100 μ AMPS AT 4V

MEMORY DRIVER 1973

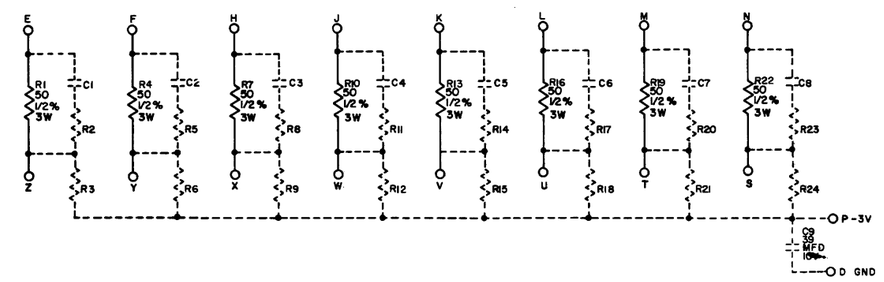
READ/WRITE SWITCH 1972

MEMORY DRIVER 1973



UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 47Ω,J%
ALL CAPACITORS ARE 4700pf, 1%

RESISTOR BOARD 1976

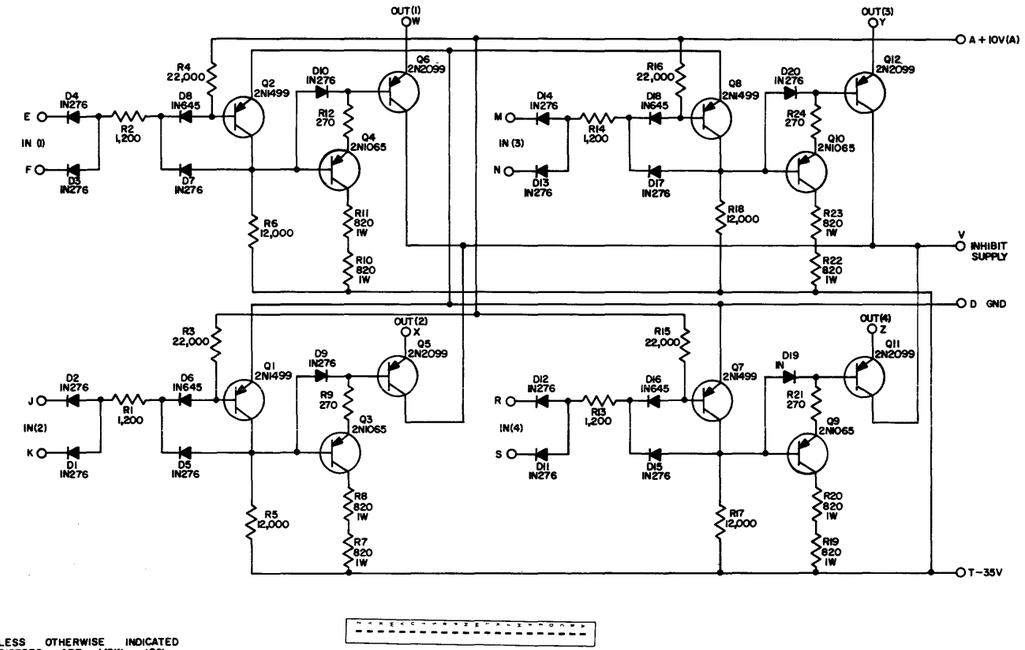


SPECIFICATIONS DEPEND UPON UNLESS CIRCUIT INDICATED APPLICATION

RESISTOR BOARD 1978

RESISTOR BOARD 1976

RESISTOR BOARD 1978



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD.

INHIBIT DRIVER 1982

INHIBIT DRIVER 1982

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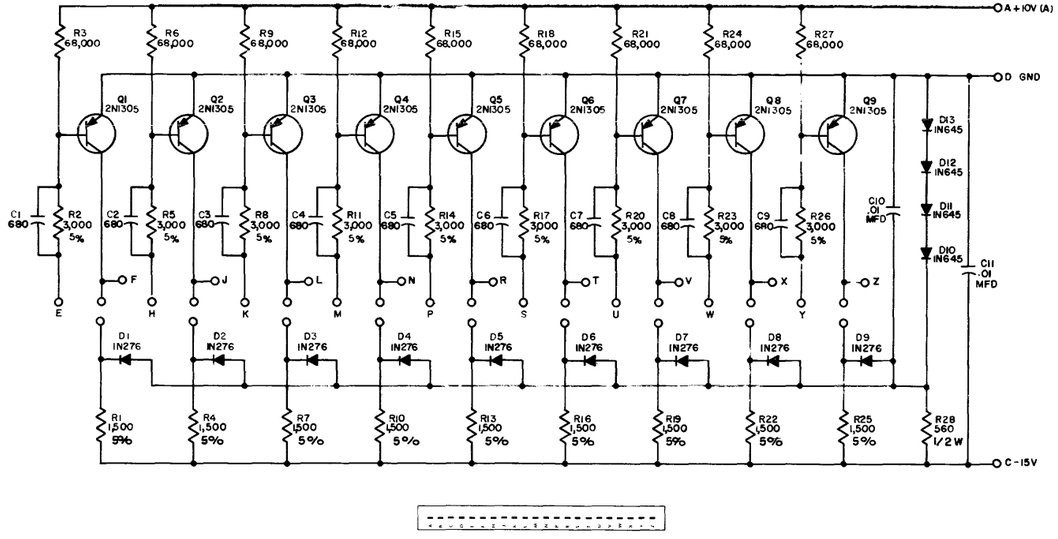
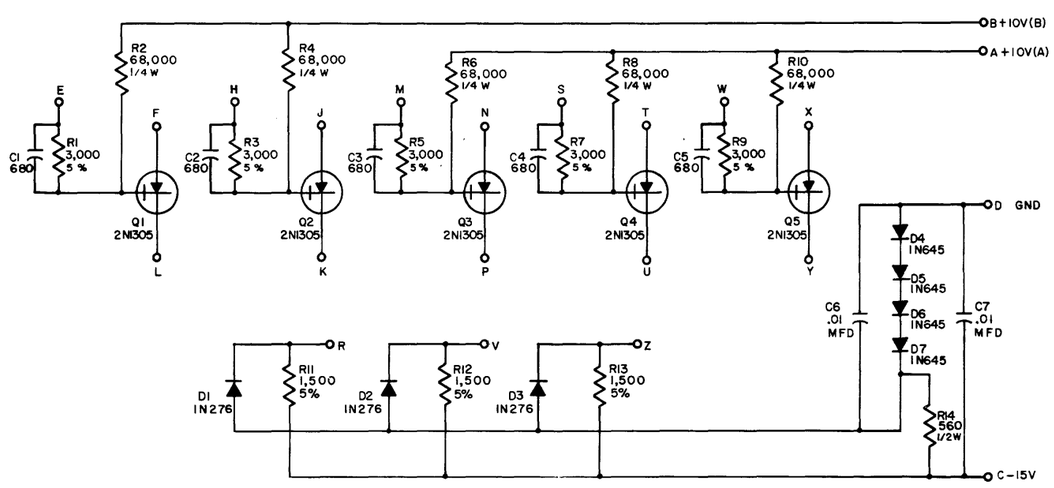


UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W 10%
CAPACITORS ARE MMFD

INVERTER 4102

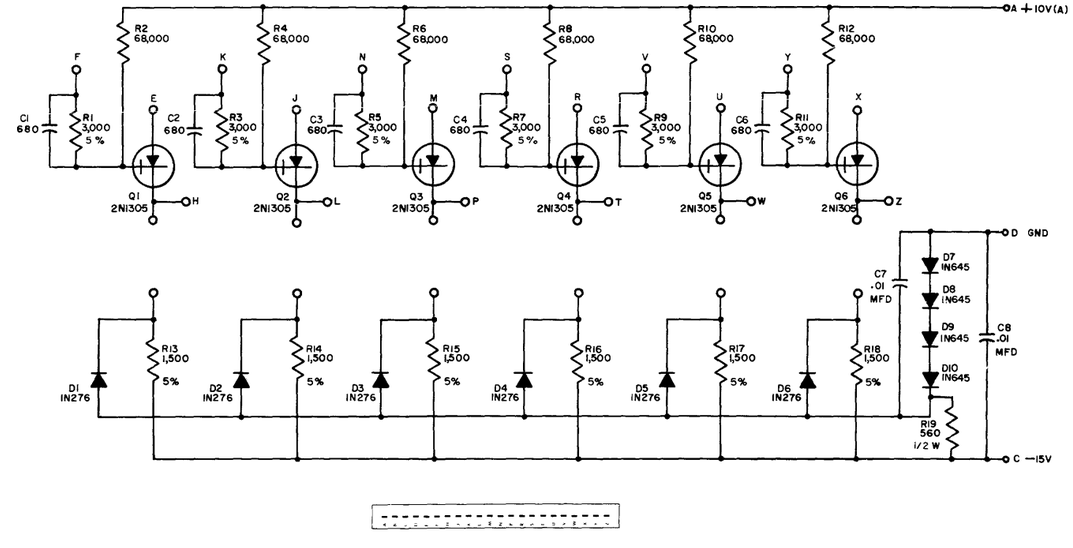


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD.

INVERTER 4105

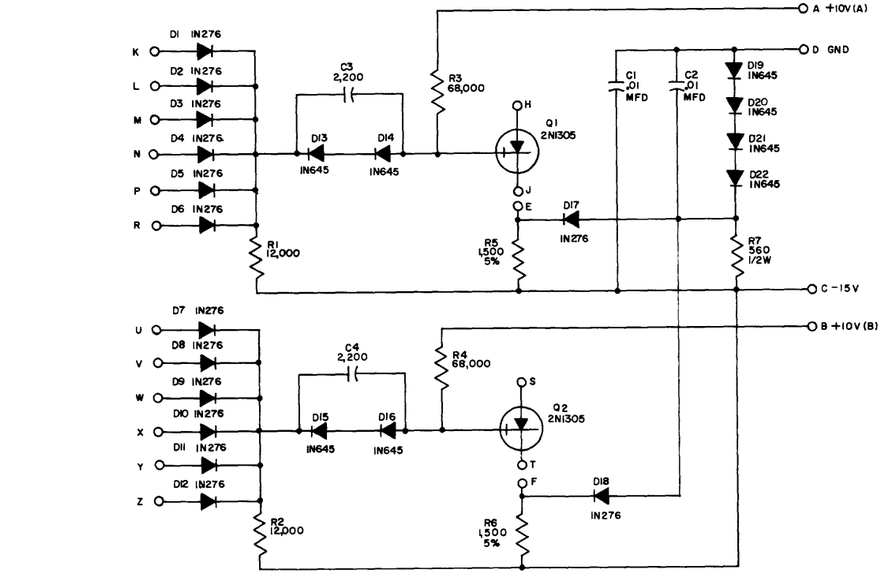
INVERTER 4102

INVERTER 4105



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

INVERTER 4106



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

DIODE 4111

INVERTER 4106

DIODE 4111

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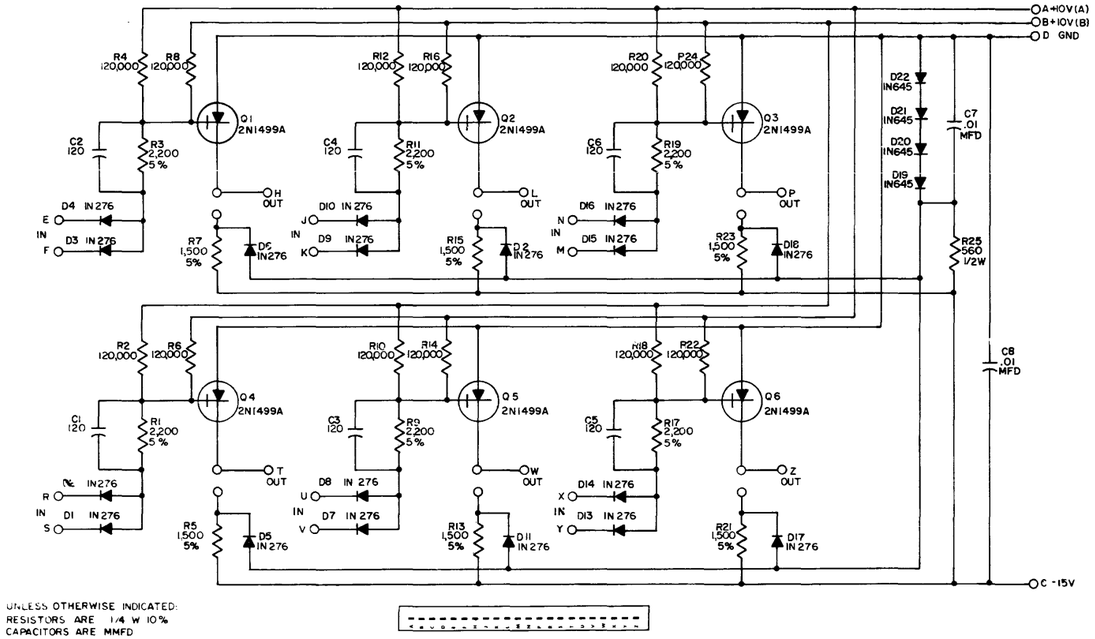
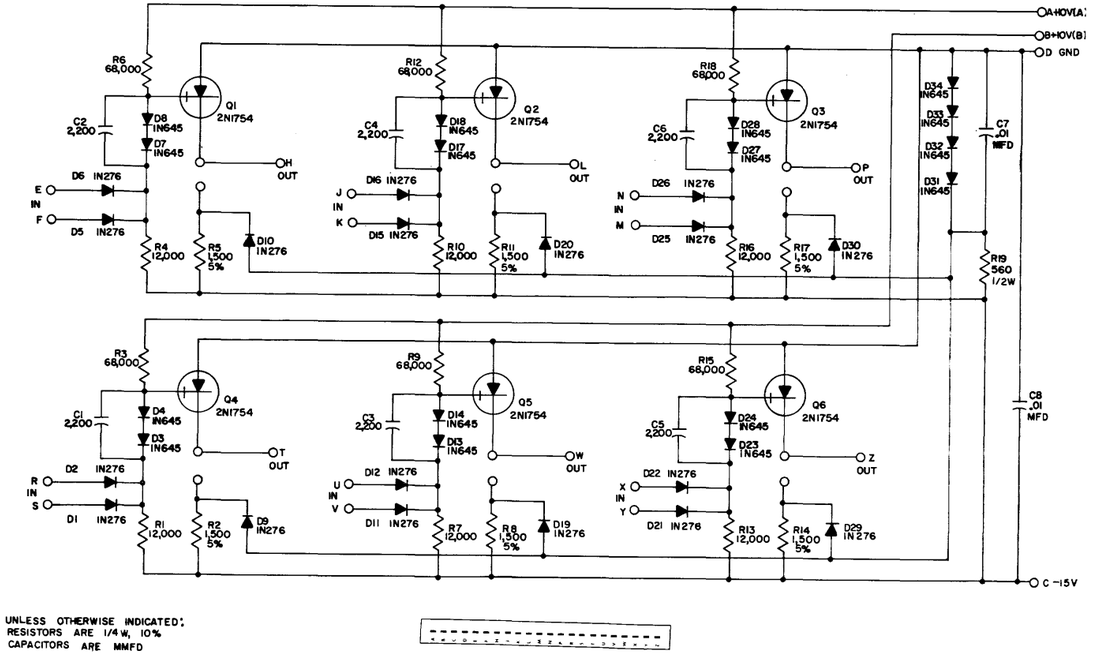


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W 10%
CAPACITORS ARE MMFD

DIODE 4112

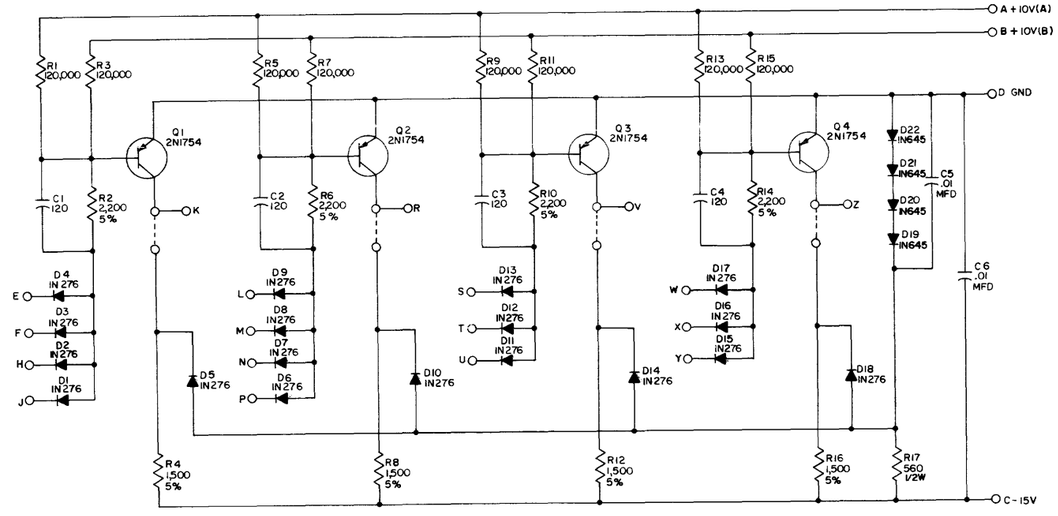


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

DIODE 4113

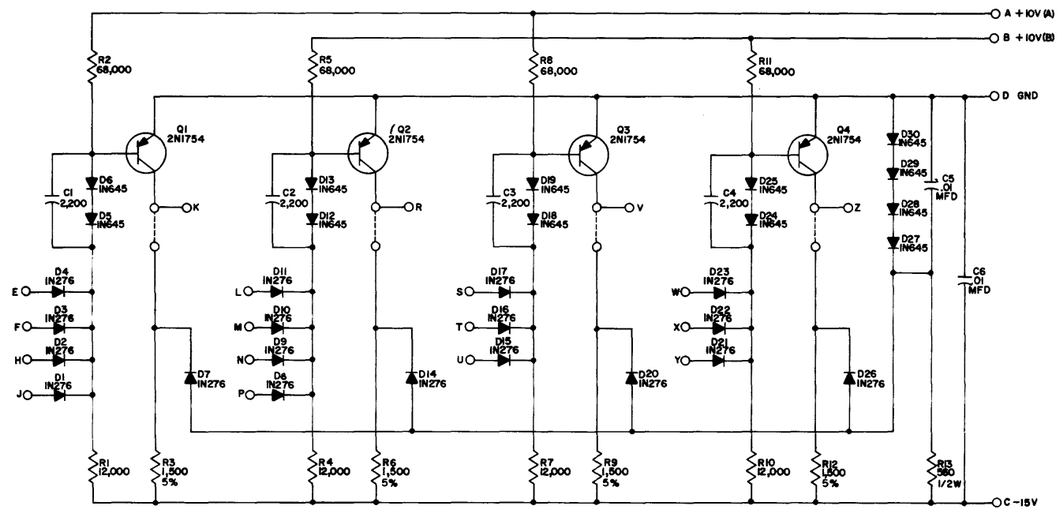
DIODE 4112

DIODE 4113



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD.

DIODE 4114

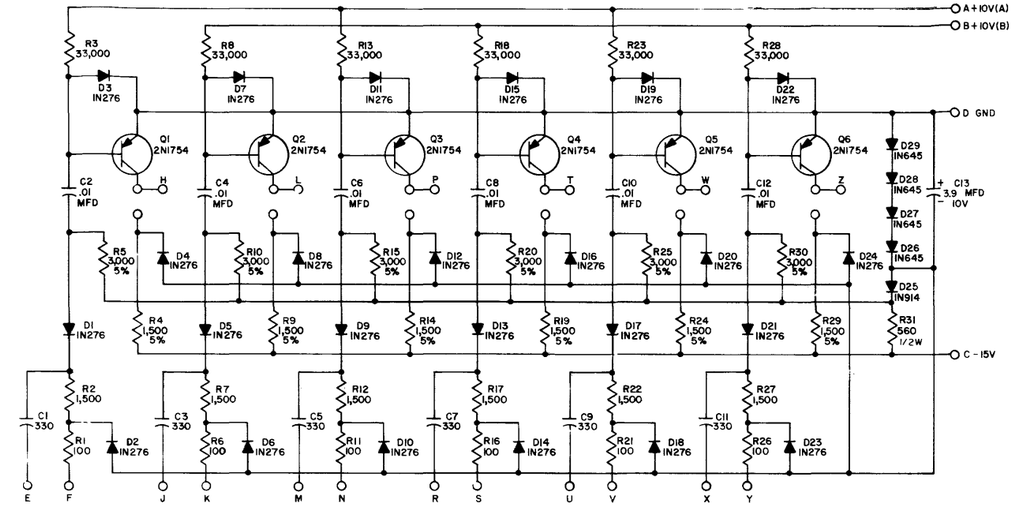


UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

DIODE 4115

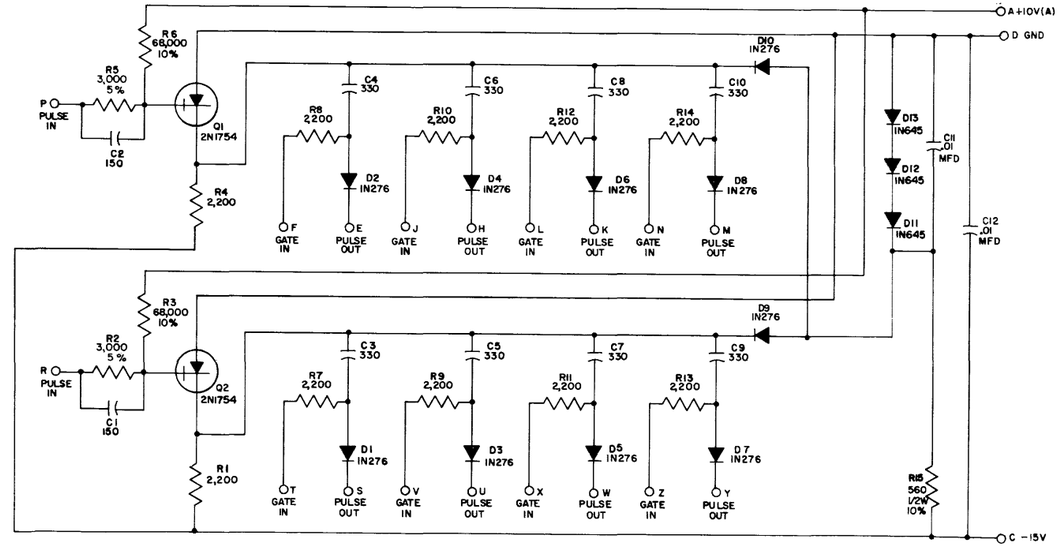
DIODE 4114

DIODE 4115



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

NEGATIVE CAPACITOR-DIODE GATE 4127

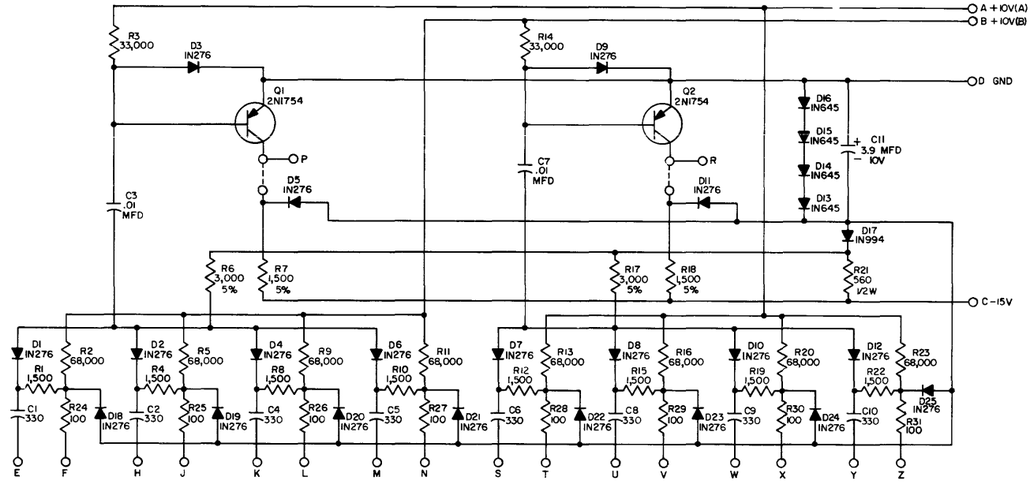


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W 5%
CAPACITORS ARE MMFD.

POSITIVE CAPACITOR-DIODE GATE 4128

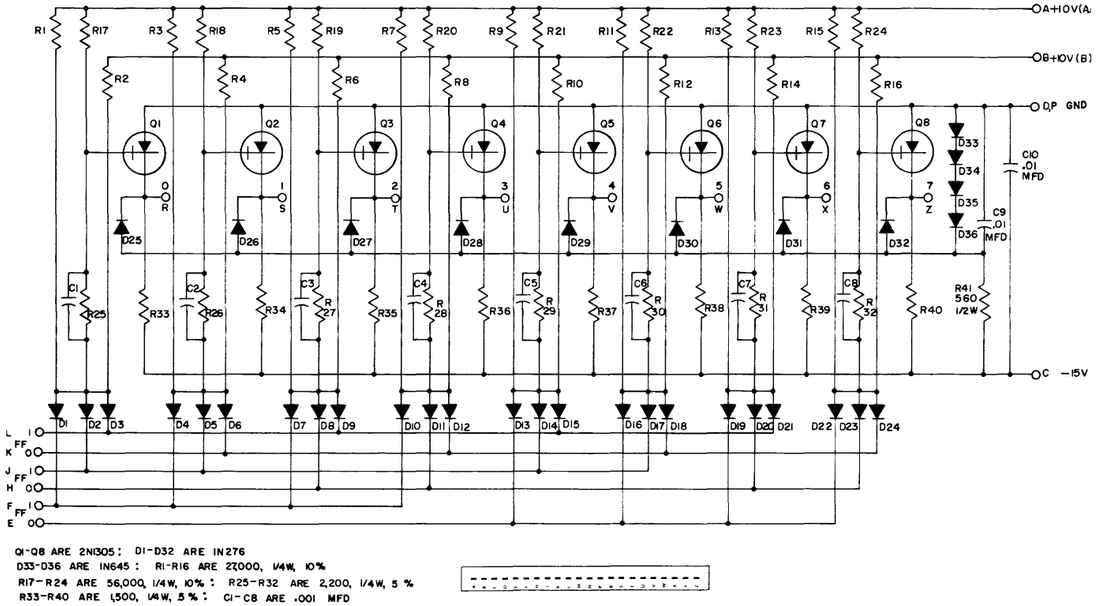
NEGATIVE CAPACITOR-DIODE GATE 4127

POSITIVE CAPACITOR-DIODE GATE 4128



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD

NEGATIVE CAPACITOR-DIODE GATE 4129

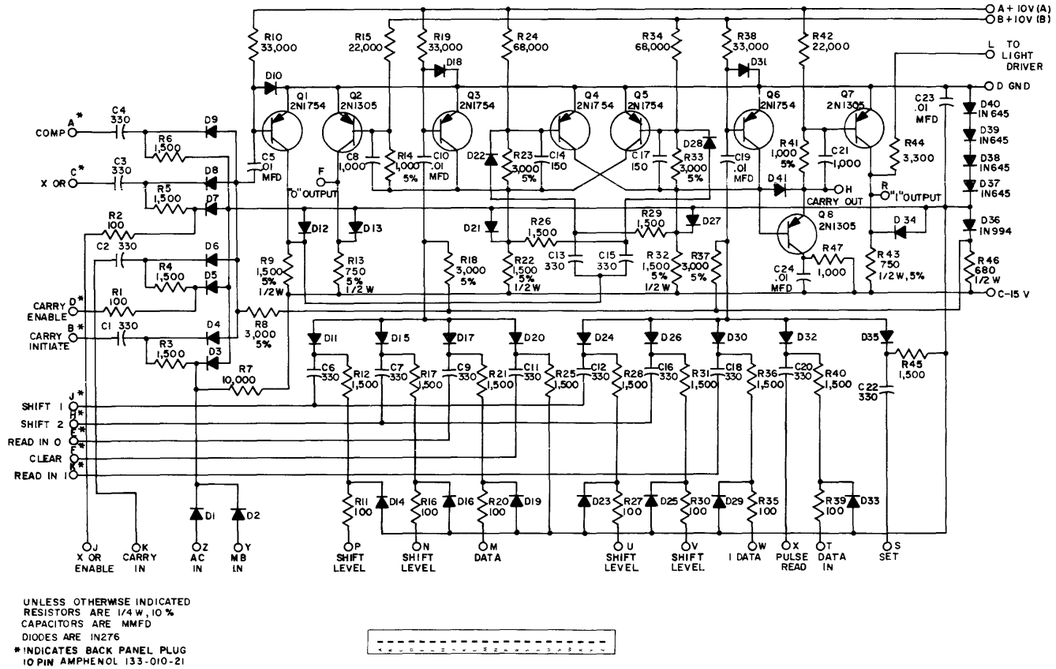


Q1-Q8 ARE 2N1305 ; D1-D32 ARE IN276
D33-D36 ARE IN645 ; R1-R16 ARE 27000, 1/4W, 10%
R17-R24 ARE 56,000, 1/4W, 10% ; R25-R32 ARE 2,200, 1/4W, 5 %
R33-R40 ARE 1,500, 1/4W, 5 % ; C1-C8 ARE .001 MFD

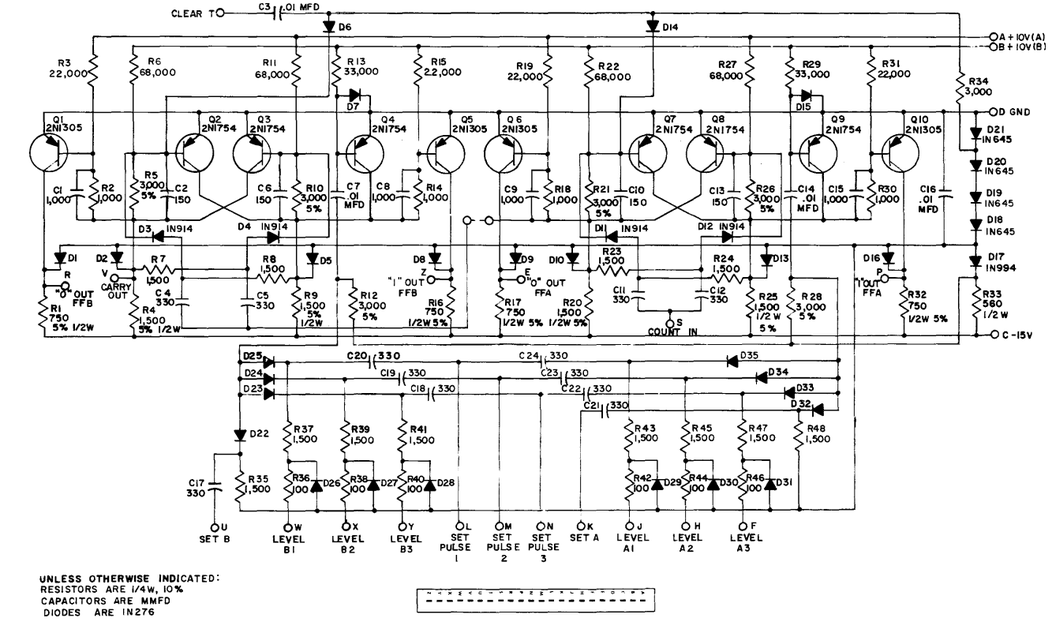
BINARY-TO-OCTAL DECODER 4150

NEGATIVE CAPACITOR-DIODE GATE 4129

BINARY-TO-OCTAL DECODER 4150



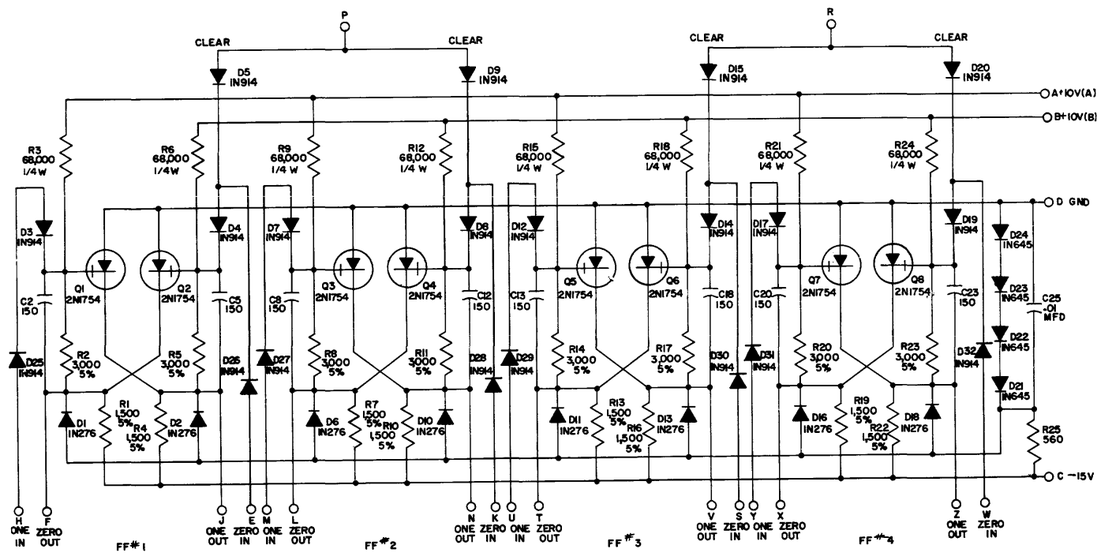
FLIP-FLOP 4203



FLIP-FLOP 4204

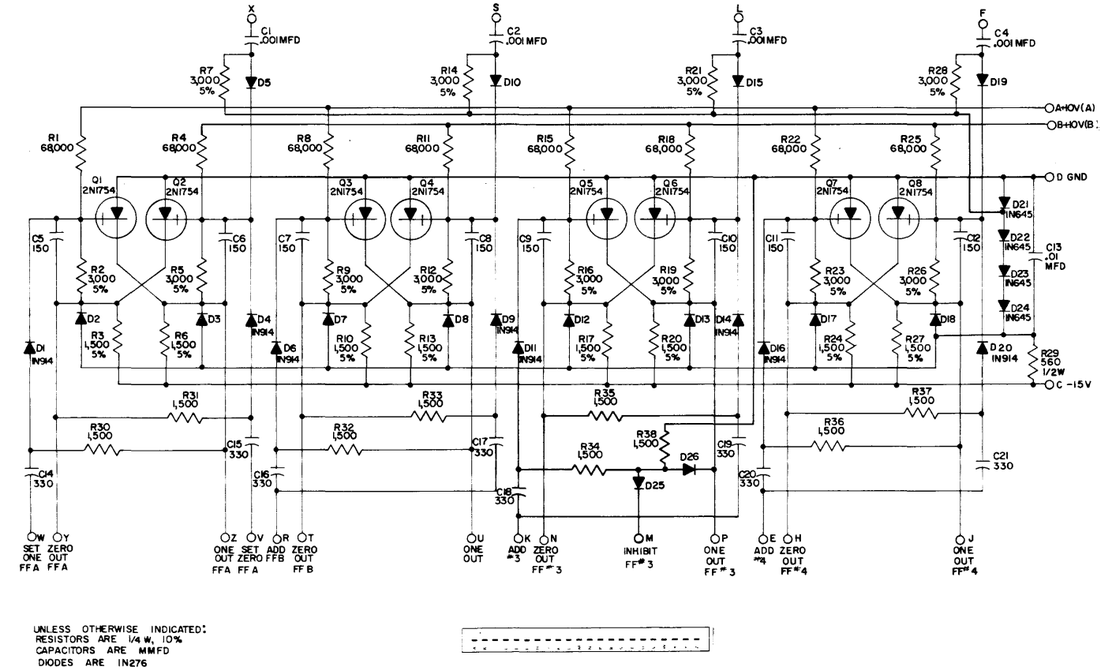
FLIP-FLOP 4203

FLIP-FLOP 4204



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2 W, 10%
CAPACITORS ARE MMFD

FLIP-FLOP 4214

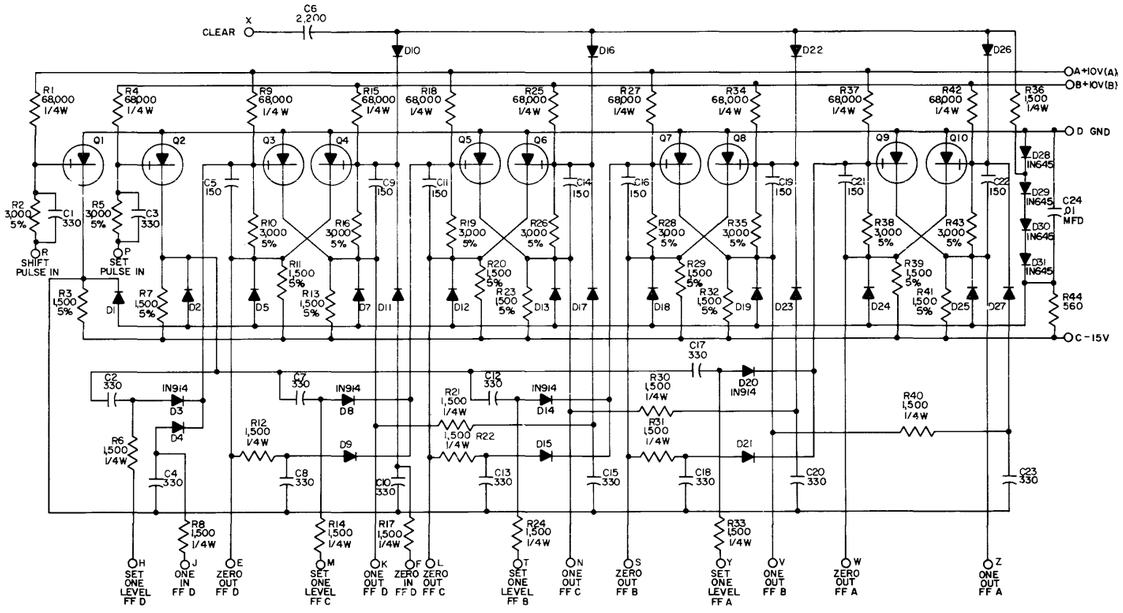


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE IN276

FOUR-BIT COUNTER 4215

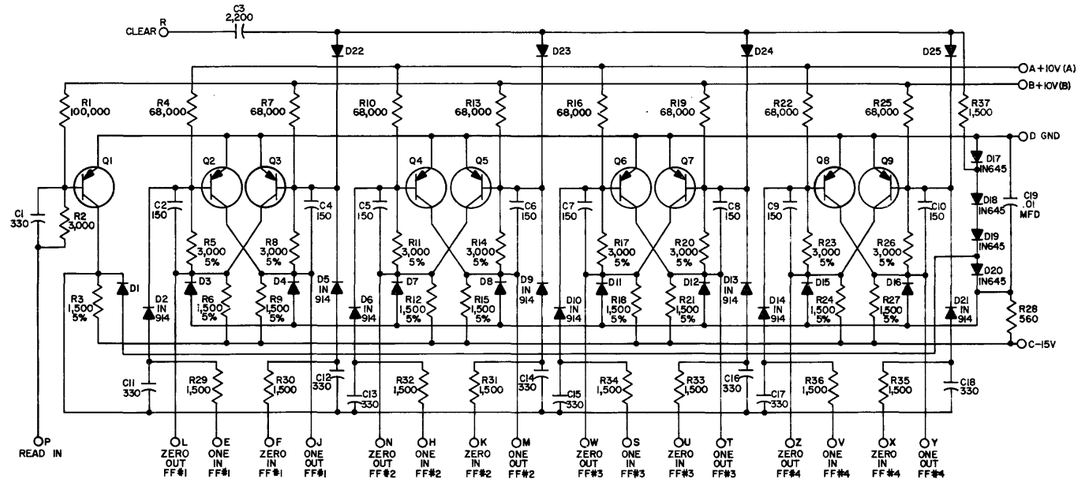
FLIP-FLOP 4214

FOUR-BIT COUNTER 4215



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%.
CAPACITORS ARE MMFD.
DIODES ARE IN276.
TRANSISTORS ARE 2N1499.

FLIP-FLOP 4216

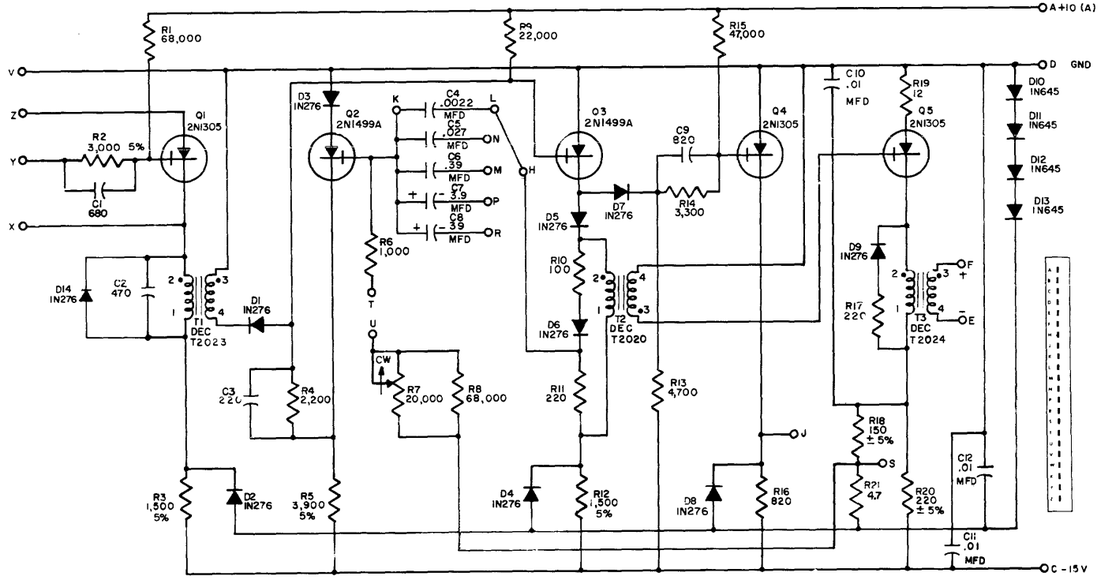


UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE 2N1754
DIODES ARE IN276

FLIP-FLOP 4218

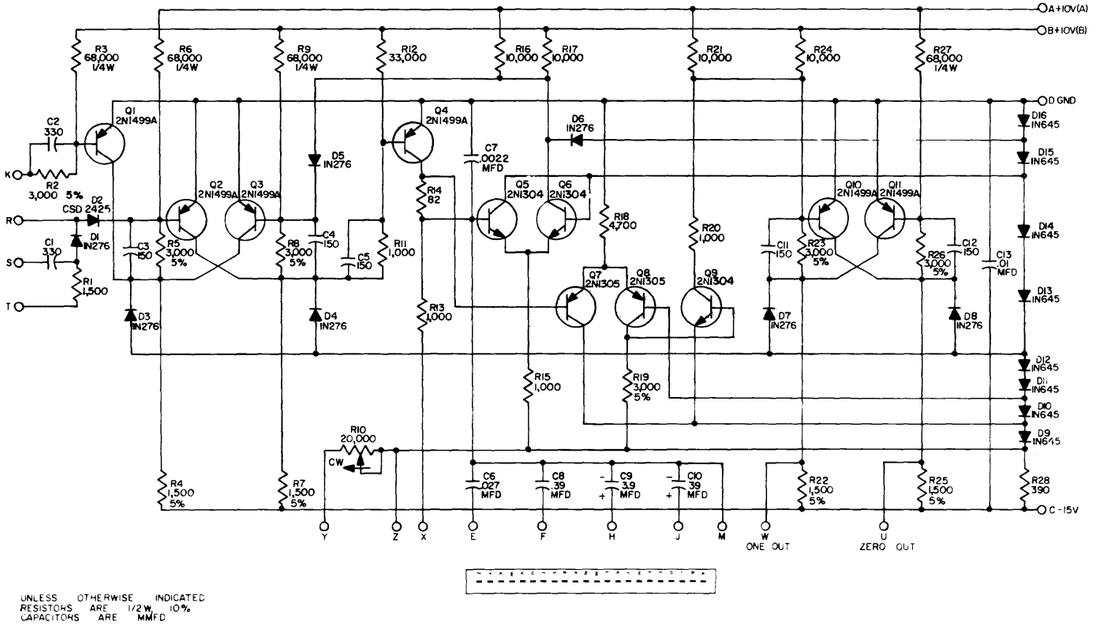
FLIP-FLOP 4216

FLIP-FLOP 4218



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD

DELAY 4301



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2 W, 10%
CAPACITORS ARE MMFD

INTEGRATING ONE-SHOT 4303

DELAY 4301

INTEGRATING ONE-SHOT 4303

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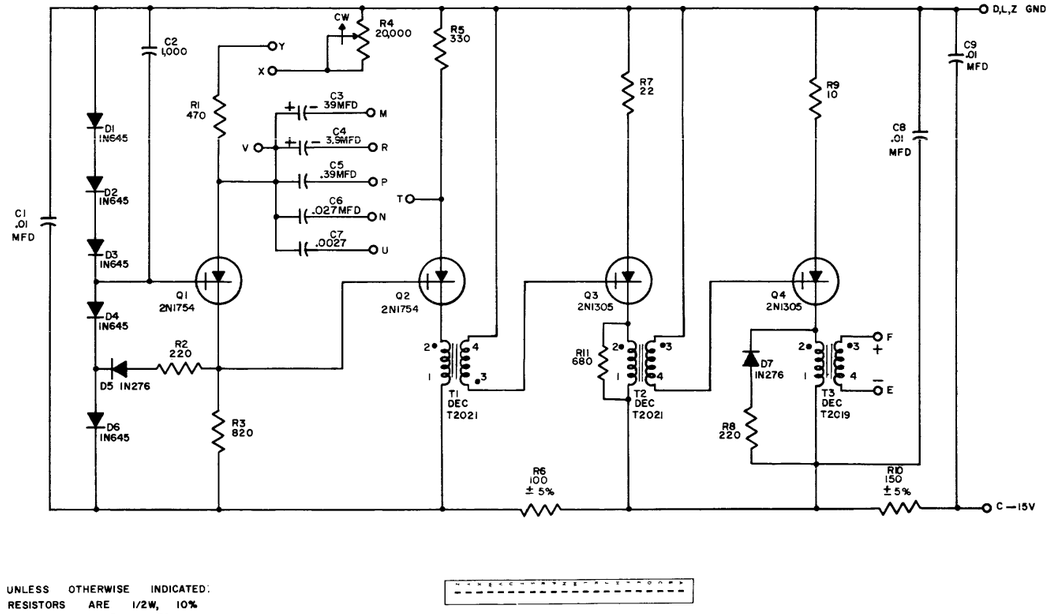
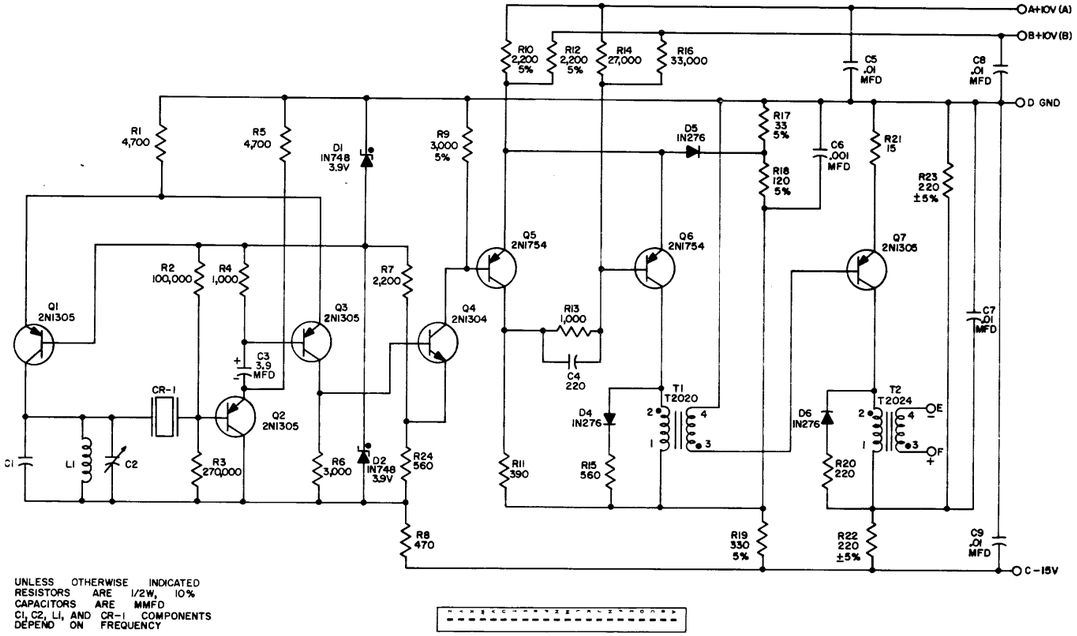


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD

CLOCK 4401

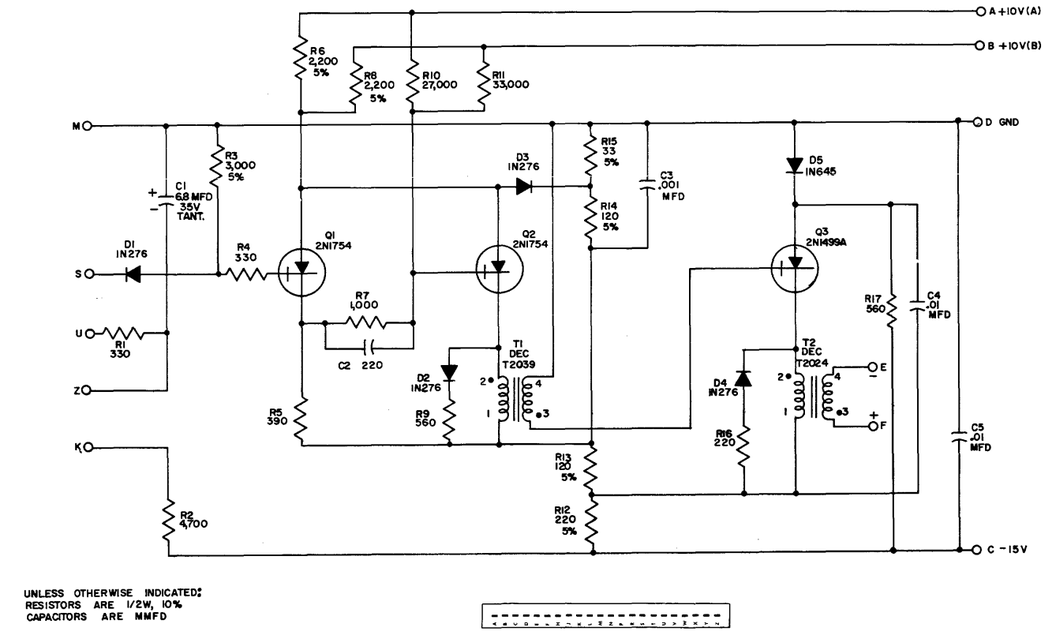


UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD
C1, C2, L1, AND CR-1 COMPONENTS DEPEND ON FREQUENCY

CLOCK 4407

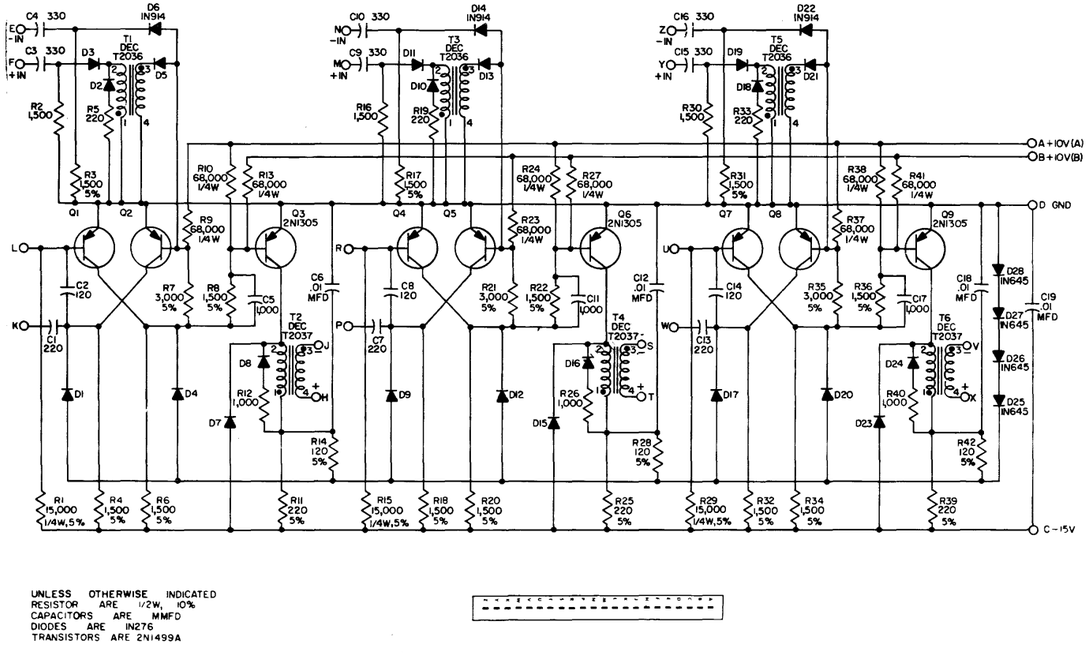
CLOCK 4401

CLOCK 4407



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD

PULSE GENERATOR 4410

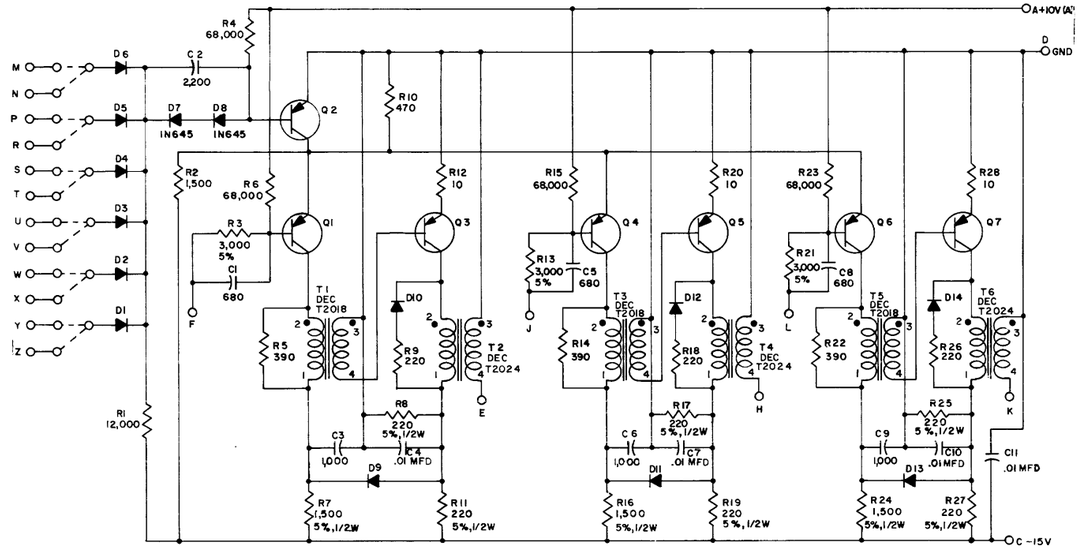


UNLESS OTHERWISE INDICATED
RESISTOR ARE 1/2W, 10%
CAPACITORS ARE MMFD
DIODES ARE IN276
TRANSISTORS ARE 2N1499A

PULSE AMPLIFIER 4604

PULSE GENERATOR 4410

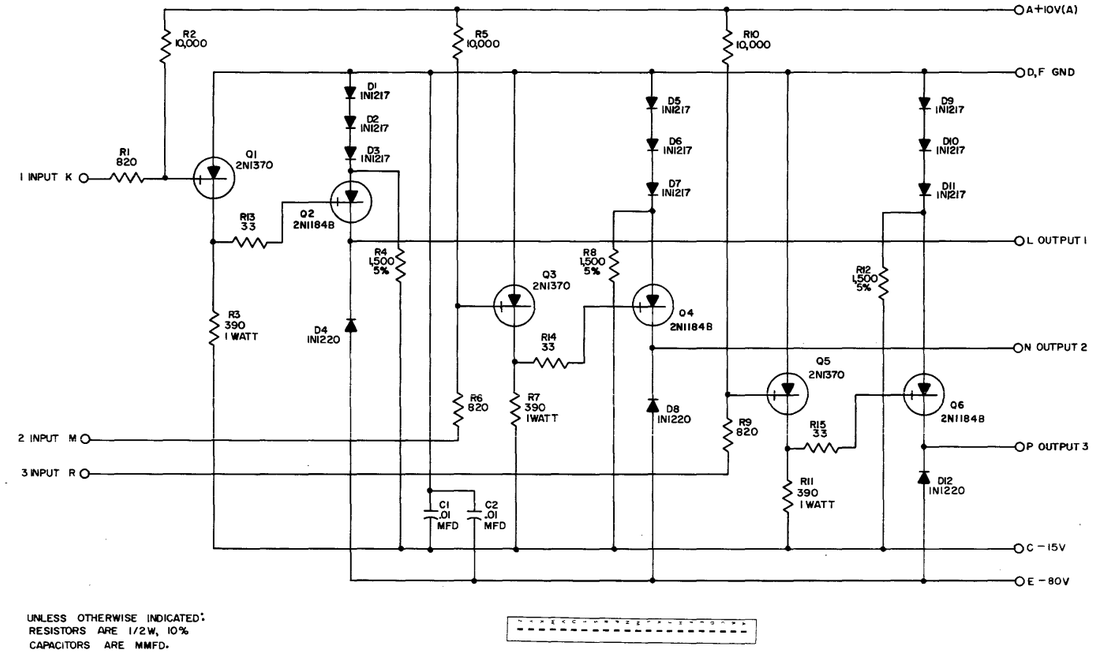
PULSE AMPLIFIER 4604



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W 10%
DIODES ARE IN276
TRANSISTORS ARE 2N1305
CAPACITORS ARE MMFD

PULSE AMPLIFIER 4605

PULSE AMPLIFIER 4605



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD.

SOLENOID DRIVER 4681

SOLENOID DRIVER 4681

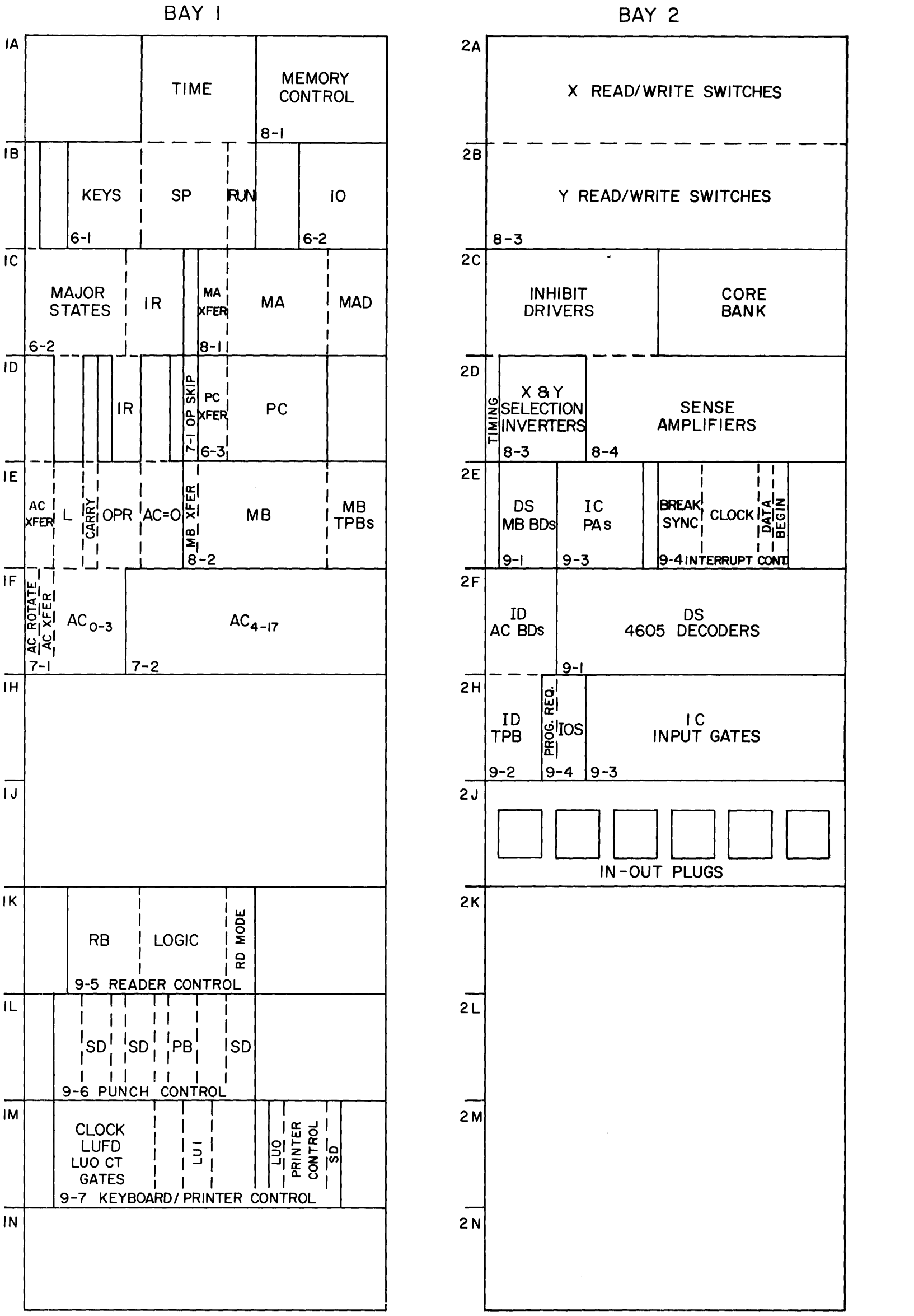


Figure 11-1 PDP-4 Detailed Logic Layout

NOTE: MODULES DESIGNATED (B) ARE REQUIRED FOR PDP-4B ONLY

	N	M	L	K	J	H	F	E	D	C	B	A	
BAY 1							4604	4127R	4114R	4115R	4127		1
							4604	4604	4112R	4106R			2
							1956R	1956	4114R	4106R			3
				4218			4203	4203	4129	4113	4112R		4
				4218			4203	4604	4106R		4106R		5
				4218			4203	4127R		4106R	4105		6
				4218			4203	4604	4129R	4114	4113		7
				4218			4203	4114R	4604	4113R	4114R		8
				4106R			4203	4105	4129R	4113R	4410	1310	9
				4604			4203	4111	4127	4214	4303	4604	10
				4127			4203	4111		4127	4127	4127R	11
				4112R			4203	4604	4113-3R		4604	4604	12
				4106			4203	4204X	4127R	4127R	4301	4218	13
				4410			4203	4204X	4604	4604	4604	4604	14
				4106R			4203	4204X			4129	4218	15
				4105			4203	4204X	4204X(B)	4204(B)	4106R	4604	16
							4203	4204X	4204X	4204			17
							4203	4204X	4204X	4204			18
							4203	4204X	4204X	4204			19
							4203	4204X	4204X	4204	4112R	1310	20
							4203	4204X	4204X	4204	4127R	4401	21
							1956R			4150	4604		22
										4150	4604	4105	23
										4150		1311	24
										4150		1607	25
BAY 2									1213	1104	1972	1972	1
									1103R		1976	1976	2
									1103R	1607	1972	1972	3
									1103R	1103R	1972	1972	4
									1103R	1982	1976	1976	5
									1103R	1978	1972	1972	6
									1103R	1982	1972	1972	7
									1540	1982	1976	1976	8
									1540	1978	1972	1972	9
									1540	1982	1972	1972	10
									1540	1982	1976	1976	11
									1540	1978	1972	1972	12
									1540		1973	1973	13
									1540		1972	1972	14
									1540		1976	1976	15
									1540		1972	1972	16
									1540		1972	1972	17
									1540		1976	1976	18
									1540		1972	1972	19
									1540		1972	1972	20
									1540		1976	1976	21
									1540		1972	1972	22
									1540		1972	1972	23
									1540		1976	1976	24
									1540		1972	1972	25
	N	M	L	K	J	H	F	E	D	C	B	A	

Figure 11-2 Module Layout, Standard Computer

NOTES:

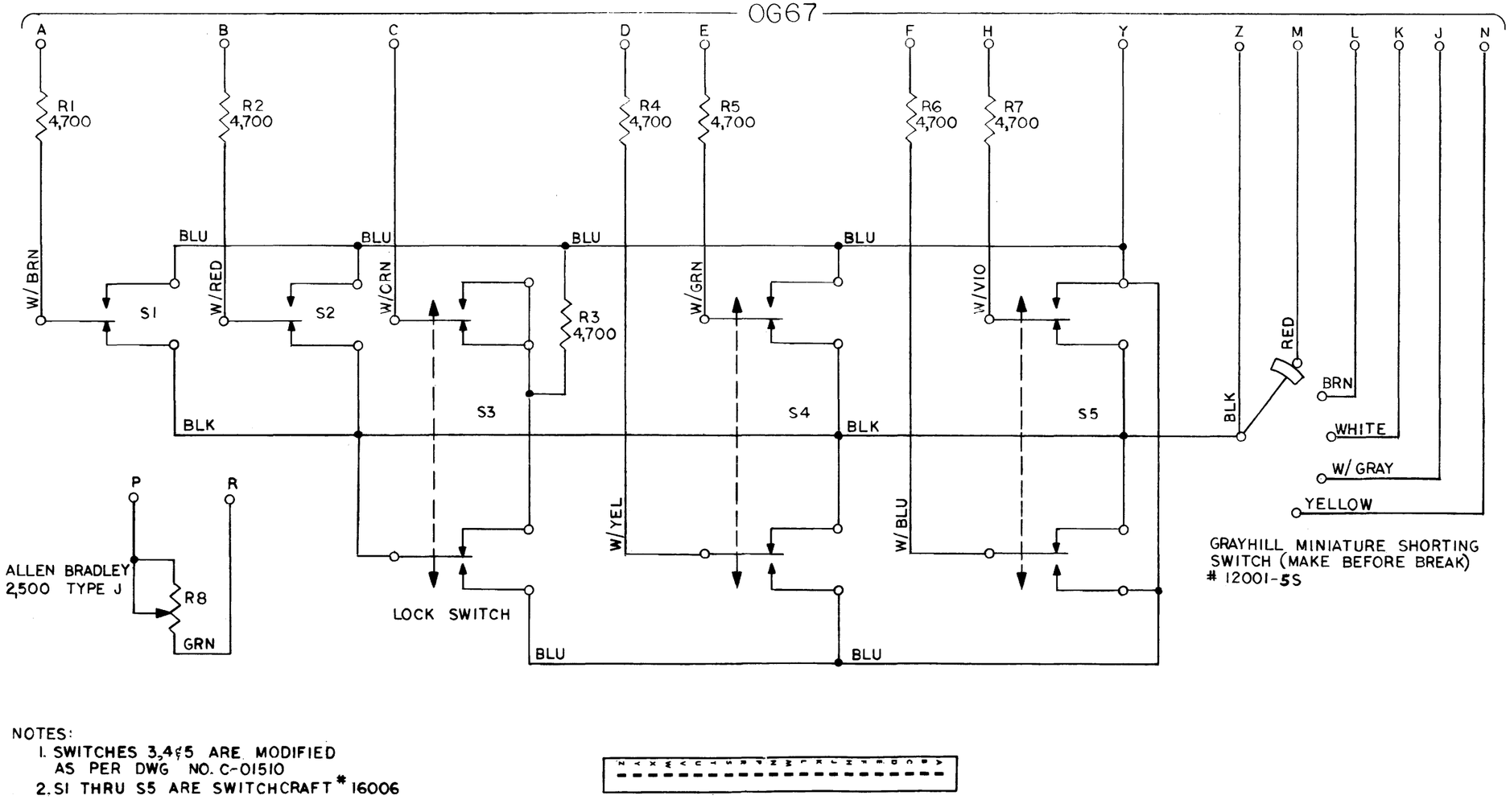
1. OPTION TYPE FOR SINGLE MODULES SHOWN IN PARENTHESES
2. 1L - PUNCH CONTROL TYPE 75 OPTION
3. 1M - KEYBOARD/PRINTER CONTROL TYPE 65 OPTION
4. 2E, 2F, AND 2H - REAL TIME CONTROL TYPE 25 OPTION
5. 2K - TAPE CONTROL TYPE 54 OPTION
6. 2L LEFT - ADAPTER FOR LINE PRINTER CONTROL TYPE 62 OPTION
7. 2L RIGHT - ADAPTER FOR CARD READER CONTROL TYPE 41-200 OPTION

BAY 1

N	M	L	K	J	H	F	E	D	C	B	A
	4407	4410									
	4114R	4301									
	4215	4681									
	4215	4681									
	4215	4113R									
	4127R	4681									
	4604	4681									
	4604	4105									
	4105	4216									
	4216	4216									
	4214	4604									
	4128	4113R									
	4215	4681						4204X (17)	4204 (17)		
	4106	4681									
											1311 (17)
	4216										1310 (17)
	4128										1607(17)
	4214										
	4128										
	4681										
		4604	1539			1690					
		4106R	1539			1690	1690				
		4127	1539			1690	1690				
		4105	1539			1690	1690				
		4410	4129R		4114	1690	4604				
		4410	4129R		4129	4605	4604				
			4129R		4129	4605	4604				
			4303		4129X	4605(75)	4604				
			4215		4129X	4605(65)	4604				
			4215		4129X	4605(65)	4604				
			4106R		4129X	4605(30A,D)	4604				
			4106R		4129X	4605(30D)					
			4113		4129X	4605(30D)	4102R				
			4604		4129X	4605(62)	4115R				
			4111		4129X	4605(62)	4218				
			4106R		4129X		4105				
		4301	4105		4129X		4218				
		4105	4113		4129X		4127				
		4127R	4216		4129X		4410				
			4216		4129X	4605(40)	4604				
		4410	4129		4129X	4605(41)	4604				
		4410	4127R		4129X	4605(54)					
			4106		4129X	4605(54)					
		4112R	4303		4129X	4605(54)					
		4105	4303		4129X	4605(54)					

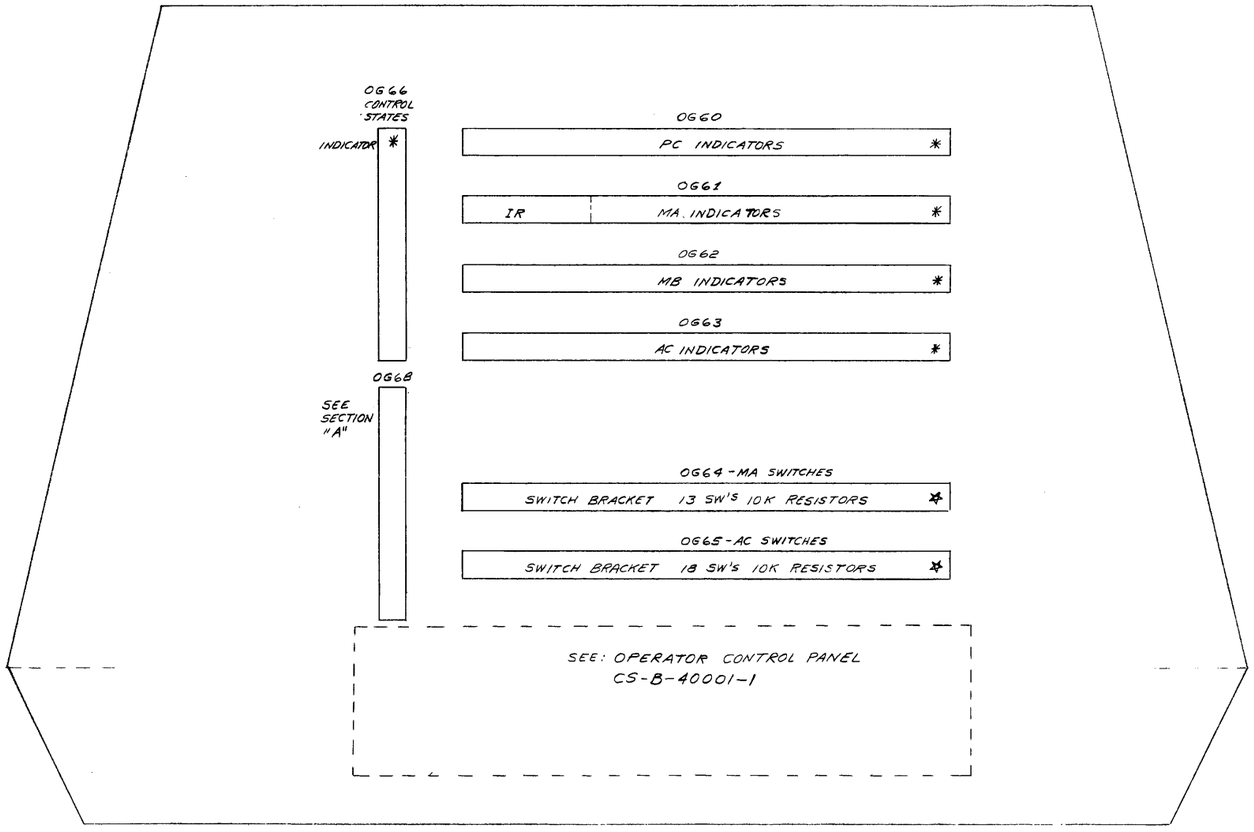
BAY 2

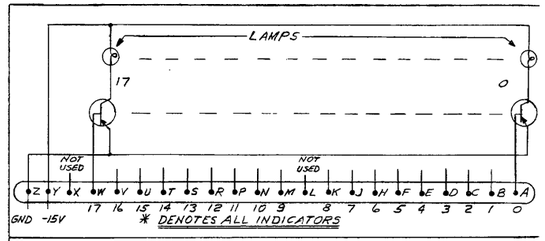
Figure 11-3 Module Layout, Optional Equipment

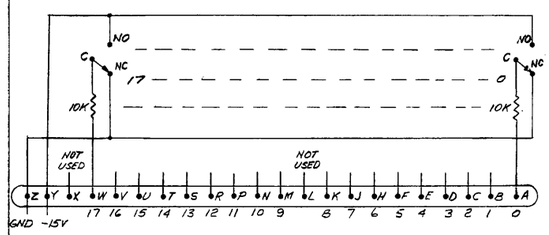


NOTES:
1. SWITCHES 3,4 & 5 ARE MODIFIED AS PER DWG NO. C-01510
2. S1 THRU S5 ARE SWITCHCRAFT # 16006

Figure 11-4 Control Panel







SECTION "A"

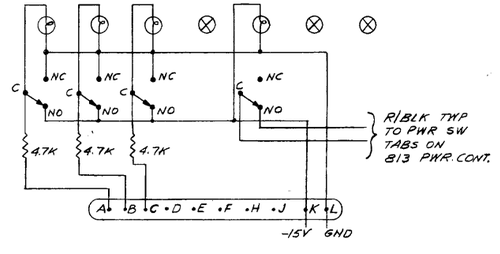


Figure 11-5 Console Circuits

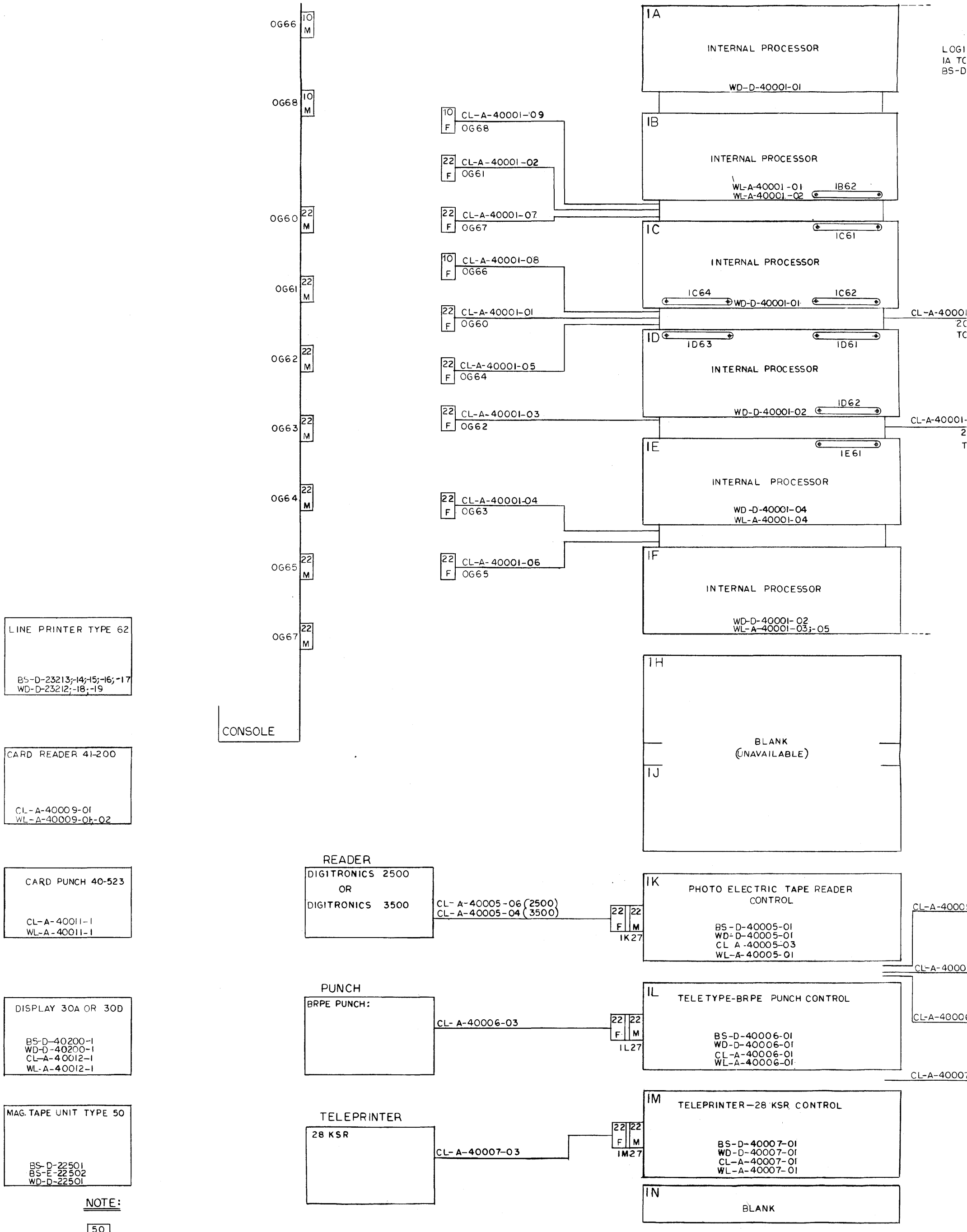


Figure 11-6 Cable Diagram

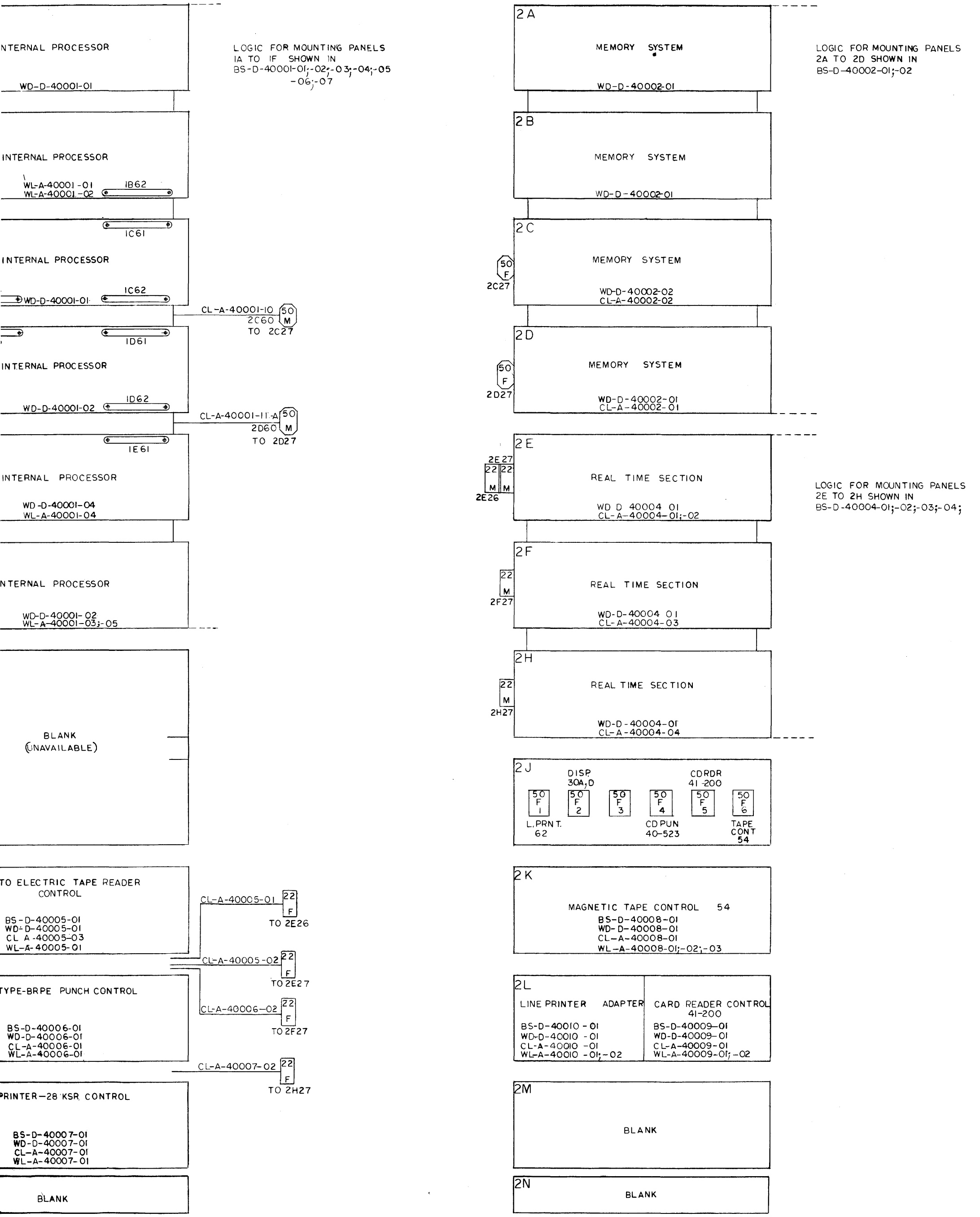
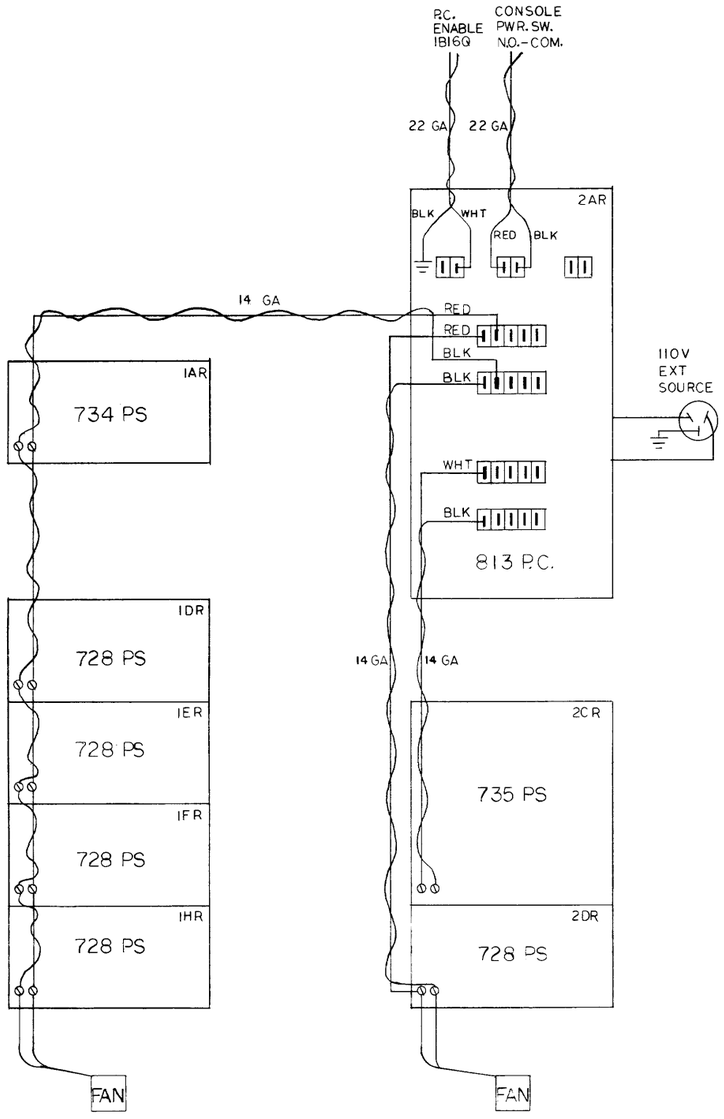


Figure 11-6 Cable Diagram



AC WIRING

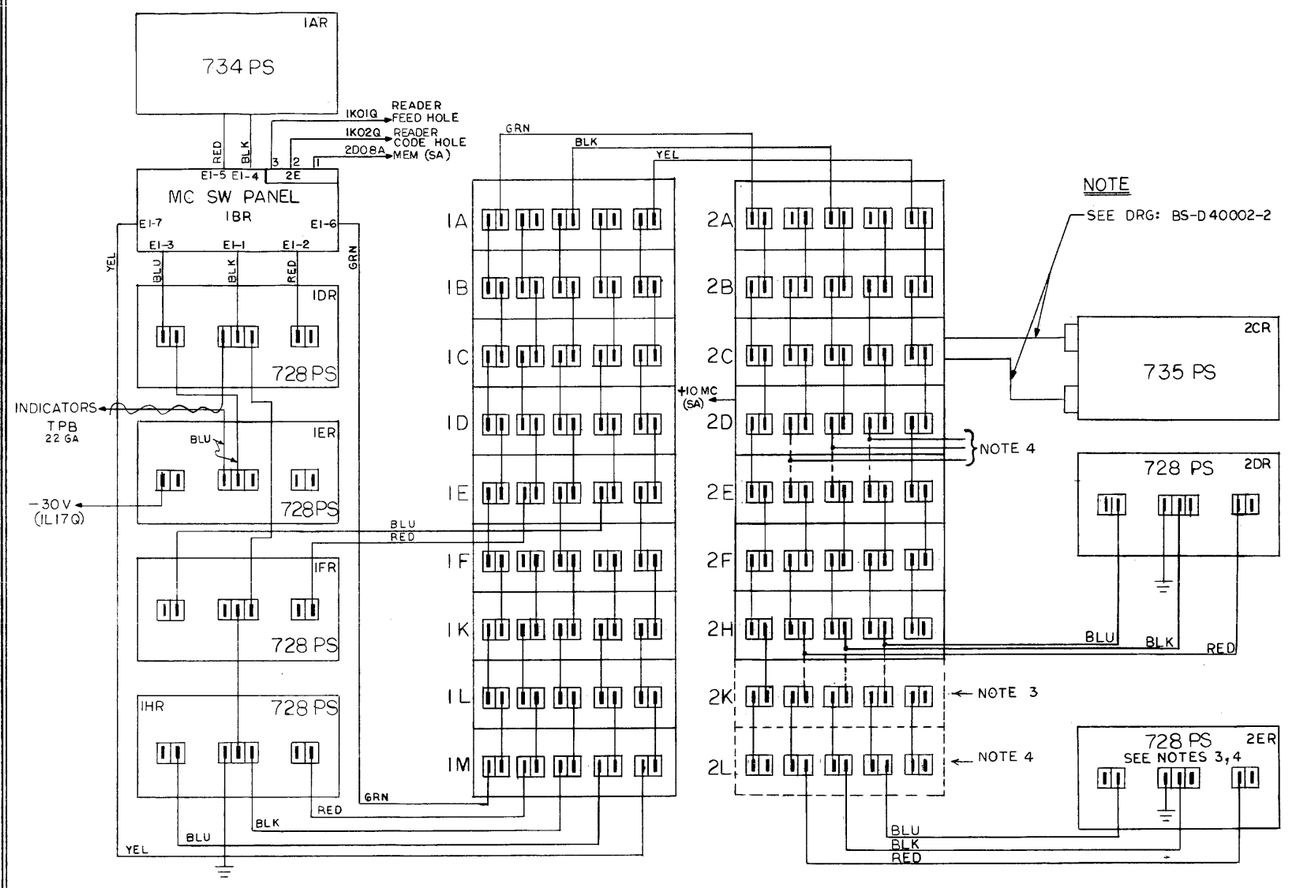


FIGURE 1

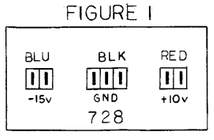
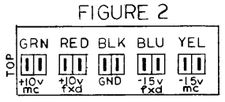


FIGURE 2



NOTE:

1. WIRE COLOR CORRESPONDS TO TAPER TAB COLORS FOR ALL MTG PANELS AS SHOWN IN FIGURE 2. AND FOR ALL POWER SUPPLIES AS SHOWN IN FIGURE 1.
2. ALL DC PWR WIRING EXCEPT TWP TO INDICATOR TPB IS 14 GA
3. WHEN THE REAL TIME OPTION ONLY IS INSTALLED (PANELS 2E TO 2H), THE 728 IN 2DR SUPPLIES PANELS 2A TO 2H—CONNECTION IS MADE AT PANEL 2H. THE 728 IN 2ER IS NOT INSTALLED.
4. WHEN ADDITIONAL IN-OUT DEVICE CONTROLS ARE INSTALLED (PANELS 2K-2M) THE 728 IN 2DR SUPPLIES ONLY PANEL 2A TO 2D-CONNECTION MADE AT PANEL 2D. THE 728 IN 2ER SUPPLIES PANELS 2F TO 2M-CONNECTION IS MADE AT LOWEST PANEL.

Figure 11-7 AC and DC Wiring Diagram

PDP-4

MODULES, POWER SUPPLIES & POWER CONTROLS

TYPE OF UNIT	TOTAL USED	INT PROC	4K MEM	8K MEM	REAL TIME SECTION	TAPE READER	TAPE PUNCH 75		TELE-PRINTER KSR 65	MAG TAPE CONT. 54	MAG TAPE CONT. 50	DPY 30D	LT PEN 32	CARD READER 40-200	CARD PUNCH 41—523	LINE PRINTER 62				
1150		4																		
1111		2																		
1103 R			7	14																
1104			1	2																
1213			1	2																
1310		2		1																
1311		1		1																
1539/										4										
1540/1538			18	36																
1542											3									
1549											4									
1559													1							
1562												1								
1564												2								
1567												2								
1607		1	1	3																
1669											1	3								
1690					8															
1701			1	2																
1703															1					
1705												1								
1956/1956R			1/2																	
1972			32	64																
1973			2	4																
1976			16	32																
1978			3	6																
1982			5	10																
4102/4102R					/1															
4105		3			1	1	1		1	1	5			2	1	6				
4106/4106R		/6				1/2			1	1/3	1				5	/5				
4110																1				
4111										1										
4112/4112R		/3				/1					3			/1						
4113/4113R		3/2					/2			2	2				/14					
4114/4114R		1/4			1				1											
4115/4115R		/1			/1															
4126																2				
4127/4127R		4/1			1	1			/1	/1				/1		/6				
4128									3			1								
4129/4129R		2/2			2/18					1/3										
4139																1				
4150																1				
4151																2				
4201															1					
4202																				
4203		19																		
4204		21		2																
4213												5			21	1				
4214		1							2			1				2				
4215									4	2						5				
4216							2		2	2										
4218		2			2	5														
4301		1					1				1	1		1	1	6				
4303		1								3		1								
4401		1																		
4407									1											
4410		1			1	1	1							2	1	3				
4514											4									
4603															3	15				
4604		8			8	1	1		2	1		1				18				
4605					3		1		1	4		3		1	1	2				
4667																1				
4677												5								
4681							6		1											
4688								*				1								
4700																120				
4606/4606R		2/7																		
728		3	1	2			1*		1*	1	1	1			1	2				
734		1																		
735			1	2																
770												1								
772																1				
NJE 60-6B												1								
811											1	1		1	1	1				
813		1																		
814																				

*ONLY 1 ADDITIONAL 728 REQUIRED FOR BOTH PUNCH AND KSR

Figure 11-8 System Module List

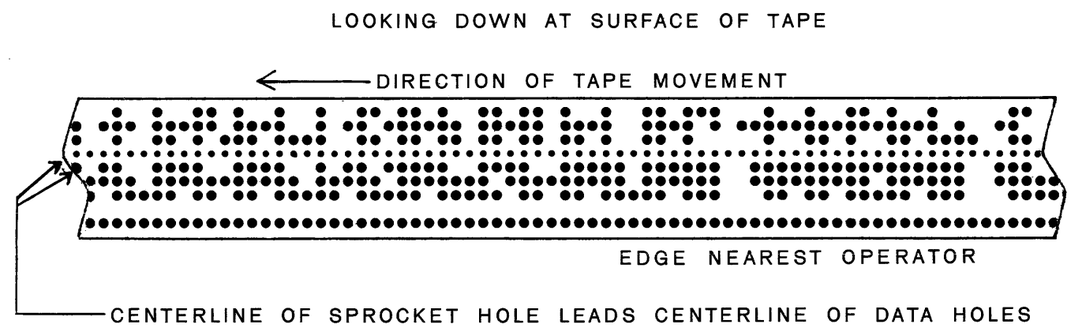


Figure 11-9 Correct Orientation for Loading Paper Tape

Figure 11-9